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IBM Field Engineering Theory of Operation

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9020 D System Introduction

SFN-0104-2

PREFACE

This manual presents those aspects of the IBM 9020D Central Computer Complex (CCC) which can be understood only in terms of the total system and its environment. It is intended for both students and trained maintenance personnel.

The manual is divided into nine chapters as follows:

Chapter 1, Introduction, provides an overview of the 9020D system in terms of the tasks it must perform and the requirements it must meet.

Chapter 2, System Description, provides a brief description of each element and unit in the system.

Chapter 3, Interface Lines, describes the interfacing between system elements/units and defines each interface line.

Chapter 4, Configuration Control, explains the hardware and software implementation provided for the dynamic control of system configuration.

Chapter 5, Storage Addressing, describes the storage-addressing scheme and the address-translation capability of the 9020D system.

Chapter 6, Multisystem Operation, describes those capabilities which are involved in operation of the system with more than one active computing element. These capabilities include: direct control, interrupts, shared storage, and reconfiguration.

Chapter 7, System Monitoring, describes the hardware facilities which permit the program to monitor system operation for malfunctions and abnormal conditions.

Chapter 8, Malfunction Handling, describes error recording, logout, and the manner in which each individual element/unit responds to malfunctions and abnormal conditions.

Chapter 9, System Initialization, describes resets, initial program load (IPL), and restarting operation from the system standpoint.

Two appendices and a glossary are also provided. Appendix A, Comparative Instruction Listing, shows the valid op codes for the CE (in 360 mode and normal 9020 mode) and for the IOCE (in IOCE-processor mode and normal mode). Appendix B, System/360 Mode of Operation, describes the differences in system operation resulting from operation in the 360 mode.

REFERENCE MANUALS

The following manuals are to be used in conjunction with this introduction manual:

General

A27-2734	9020D/E Principles of Operation, SRL
SFN-0105	9020D/E Power Controls and Distribution, FETOM
SY22-2799	Solid Logic Technology Power Supplies, FEMI
SY22-2800	Solid Logic Technology Packaging, FETOM
SY22-2798	Solid Logic Technology Component Circuits, FEMI

7201-02 Computing Element

SFN-0201	7201-02 Computing Element, FETOM
SFN-0202	7201-02 Computing Element, FEMDM
SFN-0203	7201-02 Computing Element, FEMM

Second Edition (June, 1971)

This revision, Form SFN-0104-2, obsoletes the previous edition, Form SFN-0104-1, and incorporates information pertaining to the Direct Access Storage Facility (DASF). This revision also corrects minor errors and incorporates the latest engineering changes. Changed or added text is indicated by a vertical line to the left of the text; changed or added figures are denoted by the symbol ● to the left of the caption.

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7231-02 I/O Control Element

ZZ22-2865	7231-02 I/O Control Element, FETOM
Y22-2866	7231-02 I/O Control Element, Control Panel, FETOM
Z22-2867	7231-02 I/O Control Element, FEMDM
ZZ22-6823	7231-02 I/O Control Element, FEMM

(See 7231-02 FETOM preface for additional references)

7251-09 Storage Element

SFN-0301	7251-09 Storage Element, FETOM
SFN-0302	7251-09 Storage Element, FEMDM
SFN-0303	7251-09 Storage Element, FEMM

7289-02 Peripheral Adapter Module

226-2026	7289-02 Peripheral Adapter Module, FEMI
226-2028	7289-02 Peripheral Adapter Module, FEMDM
226-2027	7289-02 Peripheral Adapter Module, FEMM

7265-02 System Console

226-2040	7265-02 System Console, FEMI
226-2042	7265-02 System Console, FEMDM
226-2041	7265-02 System Console, FEMM

Channels

SY22-2826	System/360 Model 50, Selector Channel, Common Channel, FETOM
SY22-2827	System/360 Model 50, Multiplexer Channel, FETOM

Channel-to-Channel Adapter

Y22-6806	Channel-to-Channel Adapter, Model 6006A, FETMM
Y22-6807	Channel-to-Channel Adapter, Model 6006A, FEMDM

2803A(SLT) Tape Control Unit

SY32-5001	2803A Tape Control Unit, FETOM
SY32-6002	2803A Tape Control Unit, FEMM
Y22-6781	2803, 2803A Tape Controls for 9020 System, FETOM

Magnetic Tape Units

SY22-2819	Magnetic Tape Units 2401, 2402, 2403 Models 1–6; 2404 Models 1–3, FETOM
SY22-2854	2401–2402, 2403 Models 1–3 Magnetic Tape Unit; 2403 Models 1–3 and 2803 Model 1 Tape Control, FEMDM
SY22-6631	Magnetic Tape Units 2401, 2402, 2403 Models 1–6; 2404 Models 1–3, FEMM

Direct Access Storage Facility

SY26-3671	2314 Direct Access Storage Facility, Model 1 and A-Series; 2844 Auxiliary Storage Control FETOM
SY26-0735	2314 Configuration Control Feature for 9020 Systems FETOM
SY26-3672	2314 Direct Access Storage Facility, Model 1 and A-Series; 2844 Auxiliary Storage Control FEMM
SY26-0736	2314 Configuration Control Feature for 9020 Systems FEMM
SY26-4001	2314 Direct Access Storage Facility, Model 1 and A-Series; 2844 Auxiliary Storage Control FEMDM
SY26-0737	2314 Configuration Control Feature for 9020 Systems FEMDM

1052 Printer/Keyboard

S225-3179	1052 Printer/Keyboard and 1053 Printer, FETMM
S225-3353	Selectric® I/O Keyboardless Printer, FETOM
S225-3207	Selectric® I/O Keyboardless Printer, FEMM

2821 Integrated Control Unit

SY24-3359	2821 Integrated Control Unit, FETOM
SY24-3503	2821 Integrated Control Unit, FEMDM
SY24-3383	2821 Integrated Control Unit, FEMM
SY25-3479	2821 Control Unit, Two-Channel Switch, FETOM
SY24-3508	2821 Control Unit, Two-Channel Switch, FEMDM

2540 Card Read/Punch

SY31-0081	2540 Card Read/Punch, FEMI
SY31-0168	2540 Card Read/Punch, FEMDM
SY31-0082	2540 Card Read/Punch, FEMM

1403 Printer

S225-6492	1403 Printers, FEMI
S225-6493	1403 Printers, FEMM

Legend:

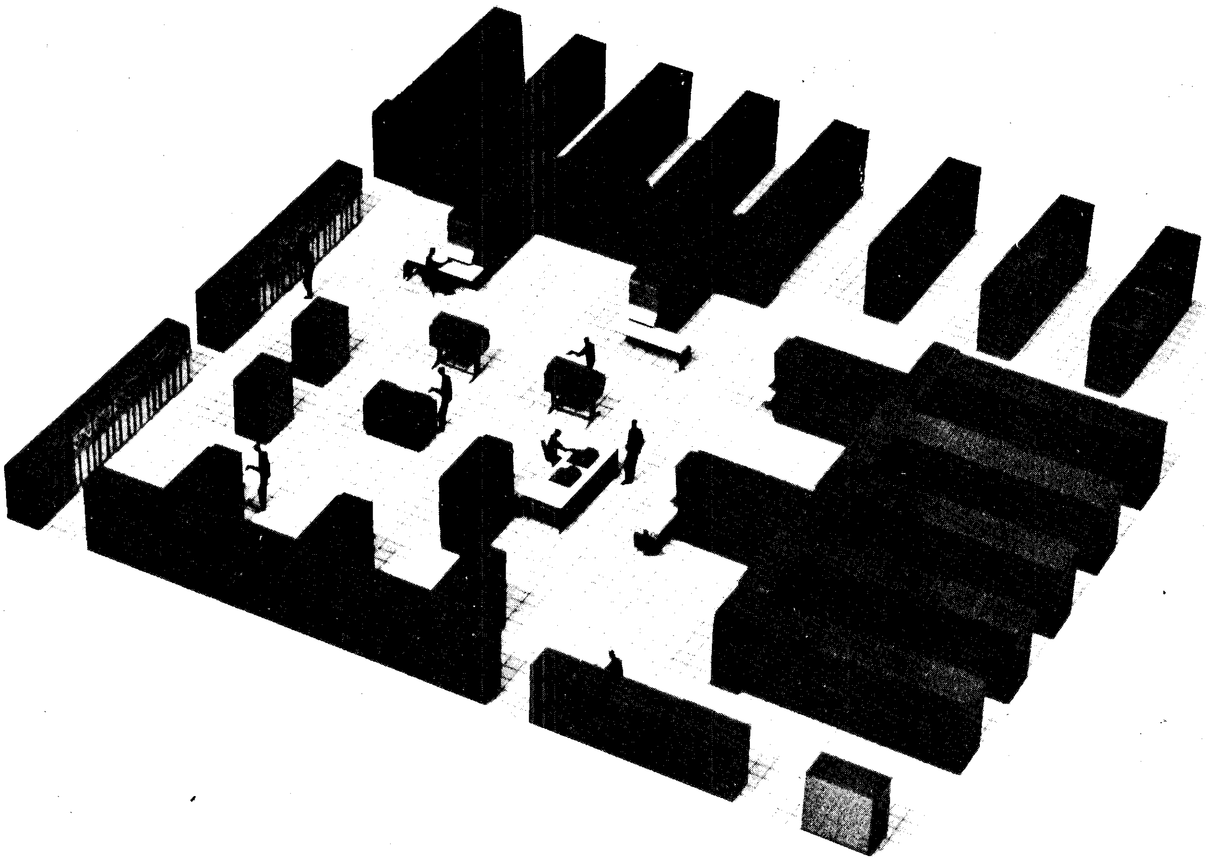
FETOM	- Field Engineering Theory of Operations Manual
FETMM	- Field Engineering Theory and Maintenance Manual
FEMI	- Field Engineering Manual of Instruction
FEMDM	- Field Engineering Maintenance Diagrams Manual
FEMM	- Field Engineering Maintenance Manual
SRL	- System Reference Library

ABBREVIATIONS

AOB	adder out bus
ATC	air traffic control
ATR	address translation register
BSM	basic storage module
CAW	channel address word
CC	condition code
CCC	central computer complex
CCR	configuration control register
CCW	channel command word
CD	common digitizer
CE	computing element
CLU	common logic unit
CSW	channel status word
CTC	channel to channel
CU	control unit
DAR	diagnose accessible register
DARM	diagnose accessible register mask
DASF	direct access storage facility
DCCU	data communication control unit
DCP	display channel processor
DSU	disk storage unit
ELC	element check
EXC	executive control
FDEP	flight data entry and printout
FLT	fault locating test
IA	instruction address
IAR	instruction address register
IC	instruction counter
ILOS	inhibit logout stop
I/O	input/output
IOCE	input/output control element
IPL	initial program load
LOS	logout stop
MACH	maintenance and channel
MC	machine check
MCW	maintenance control word
MPX	multiplexer
NAS	national airspace system
OBS	on-battery signal
OTC	out of tolerance check
PAM	peripheral adapter module
PIR	processor interruption register
PSA	preferential storage area
PSBA	preferential storage base address
PSBAR	preferential storage base address register
PSW	program status word
ROS	read-only storage
RVDP	radar video data processor
SAB	storage address bus
SABR	storage address buffer register
SAR	storage address register
SC	system console
SCCU	system console control unit
SCI	storage control interface
SCU	storage control unit
SD	storage data
SDBI	storage data bus in
SDBO	storage data bus out
SDR	storage data register
SE	storage element
SEL	selector
SE SAR	storage element storage address register
SMMC	system maintenance monitor console
SSU	storage switching unit
TAM	test and monitor
TCU	tape control unit
TU	tape unit

CONTENTS

ILLUSTRATIONS



9020D Central Computer Complex

The IBM 9020D Central Computer Complex (CCC) is the focal system within the total complex of computers and computer-controlled equipment used in the air traffic control (ATC) task. The purpose of this equipment is to acquire accurate and adequate data and to present it for use by the flight controllers in real time. Figure 1-1 shows an overall view of this equipment complex, known as the National Airspace System (NAS) En Route Stage A, and illustrates the role of the 9020D system.

The overall ATC task includes a number of fairly distinct activities, some of which are listed below so that the role of the CCC system may be viewed in perspective:

1. Acquisition of input data directly from its source (flight plans, radar returns, weather information, etc.).
2. Processing of input data (sorting and formatting data, calculating flight paths and arrival times, etc.).
3. Production of flight progress strips.
4. Production and transmission of various operational messages (within the center, to other centers, to airports, etc.).
5. Production of bulk-processed radar data.
6. Storing of flight plans flight progress records, weather information, etc.
7. Updating of stored information.
8. Final preparation of data for display.
9. Display of data for use by the flight controllers (radar data, tabular information, and weather information).

In addition to the ATC-related activities, the NAS complex provides facilities for monitoring its own operation. This enables changing traffic loads to be accommodated, malfunctions to be detected and isolated, and backup equipment to be called into operation when required.

A NAS complex centers about a Central Computer Complex (CCC) which may be an IBM 9020A or 9020D system. Each performs the same functions, but the 9020D has higher speed and greater capacity than the 9020A. The 9020D is the subject of this manual and is the only CCC system discussed.

Data from various sources, including digitized radar, teletype, IBM 1052 I/O writers, and flight data entry equipment, enters the NAS complex via adapters within the CCC which convert all incoming data to a code usable by the computer. This data is processed according to its type and source and is passed along to the appropriate output or is stored until needed.

Data leaves the CCC system as various types of operational messages, flight progress strips, and processed radar and weather information. The messages and flight strips are transferred from the CCC via adapters which translate them into the appropriate transmission code for the particular user. For example, messages to another center might be transmitted via teletype so that an adapter which translates from the computer code to the teletype code would be required.

Processed radar and weather information leaves the CCC system via data channels that connect to the Display Channel Processor (DCP) system or similar computer display channel equipment. The DCP receives this data and continues to process it for display. Once it is processed, the DCP system must interface with the display equipment so that the data can be transferred to the correct display efficiently and automatically. Thus, the DCP system provides the link between the CCC and the display equipment.

Note that both the CCC system and the DCP system interface with a System Maintenance Monitor Console

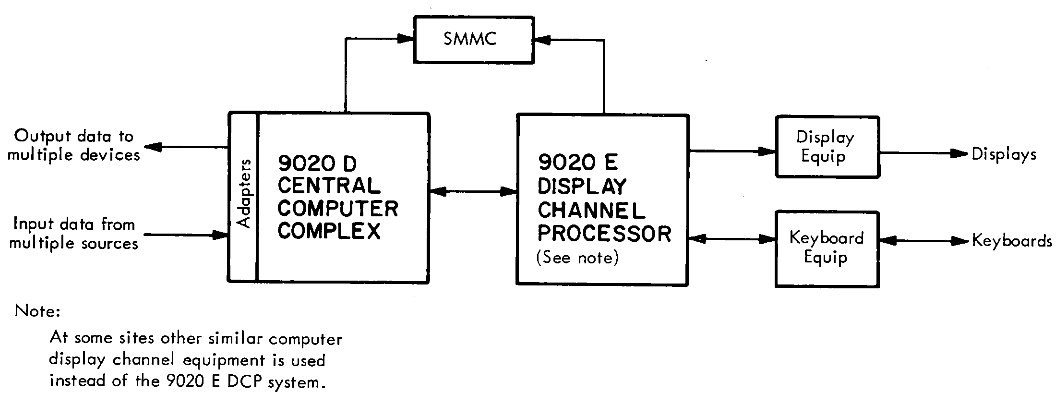


Figure 1-1. Role of 9020D CCC in NAS En Route Stage A Complex

(SMMC) which is external to both systems. The SMMC provides a central location from which maintenance personnel may monitor the overall operation of the NAS complex.

SYSTEM REQUIREMENTS

Because the NAS complex is engaged in the critical, real-time task of air traffic control, it is necessarily designed for maximum reliability. That is, the probability of the entire NAS complex being catastrophically rendered incapable of performing its mission is extremely low. Since all equipment is subject to failures to some extent, provision is made for failures so that they do not catastrophically interfere with the performance of the ATC task; this is achieved partly through the use of highly reliable equipment and partly through a "fail-safe" and "fail-soft" approach. A fail-safe system is one that can perform its entire workload in the presence of any single element malfunction. A fail-soft system is one that is not completely crippled by the presence of a malfunction but, instead, performs only the essentials of its workload, delaying nonessential operations until later.

These concepts of reliability, fail-safe, and fail-soft, which are inherent in the NAS complex, are achieved within the 9020D system as a result of the following:

1. Equipment designed for maximum reliability and minimum downtime.
2. Battery backup power in all major elements which switches in automatically when there is a loss of external power.
3. Redundant (spare) elements provided for each major element.
4. The facility within each element to operate at various levels or states of operational capability.
5. The facility to dynamically reconfigure elements into subsystems which are appropriate to the current workload and which accommodate malfunctioning elements.
6. Elaborate facilities available to the program for monitoring malfunctions and abnormal conditions.
7. The capability of operating under a control program which can provide more rapid responses to changes in workload and system environment than could be provided by manual intervention.

These seven points are enlarged upon in the following text so that it can later be seen how the system requirements give rise to most of the hardware features of the 9020D system which are described in the remaining chapters of this manual.

The 9020D system comprises a number of elements, each of which is a solid-state device that provides high reliability. Elaborate parity-checking is incorporated so that errors may be detected. Downtime is minimized by the inclusion of maintenance features, at both the element and subsystem levels, which facilitate rapid isolation of failures. These features include maintenance panels for standalone testing, fault-location tests in some elements, and diagnostic programs for all elements and units.

Major elements in the CCC system are provided with battery backup power sources which can be automatically switched in when the element senses the loss of external power. Only major elements have this facility since loss of all power at a center results in loss of input data; hence, there is no need for peripheral I/O equipment. Further, loss of power to an individual piece of I/O equipment can be dealt with by substituting a redundant I/O device. However, unexpected loss of power to equipment in which the program is running is intolerable because no logical restarting point can be determined when power is restored. That is, there would be no way to determine what data had been processed and what had not. Extensive and time-consuming reinitialization would be required.

The battery backup power source permits the program to continue operating for approximately 5 seconds after external power loss so that a logical stopping point (check point) can be established by the program. The system can then power down normally. When power is restored, processing can begin where it left off, with very little lost time.

Element redundancy is designed into the 9020D system so that more elements are available than are actually required for the performance of the ATC task. Some redundant elements may be failing elements which have been isolated from the system for maintenance, whereas others are "good" elements capable of being called into the ATC system. The recallable elements may be undergoing preventive maintenance or may be part of a subsystem involved in the maintenance of a particular element. They may also be engaged in the performance of non-ATC tasks, such as program debugging or the running of programs to perform a desired task not directly related to the ATC function.

Each element can operate in any one of four states of operational capability. The state of an element determines the degree of manual control which maintenance or operating personnel may exercise over it. For example, in state 0 (the lowest operational state), virtually all element controls are operational so that maintenance may be performed on the element. In fact, by placing the element in Test mode, the ATC system may be denied use of the element completely. In state 3 (the highest operational state), virtually all manual controls are disabled so that the element can operate in the ATC system without interference. From the larger point of view, element state may be looked upon as the element's degree of availability to the ATC task.

Each element has a configuration control register (CCR) which determines three things for it: (1) with which other elements in the system it may communicate, (2) what element state it is to assume, (3) which other elements may change its configuration. The setting of these CCRs is under direct program control. Thus, it is possible for the program to alter the structure of the system as required. For example, if the traffic load increases, additional elements may be brought into the system; if an element fails, another element may be substituted.

To react to abnormal conditions, the program must be made aware of them. Elaborate monitoring facilities are built into the 9020D system. Provision is made to report the following to the program: logic checks, overtemperature conditions the switching of an element to battery power, failure of an element to have valid data in its CCR, and the inability of an element to continue operation.

Most of the preceding text dealt with the manner in which various abnormal conditions are brought under program control and with the special facilities available to the program to respond to these conditions. All of this presupposes a running program that is capable of controlling the system. This is the reason behind the seventh point listed earlier.

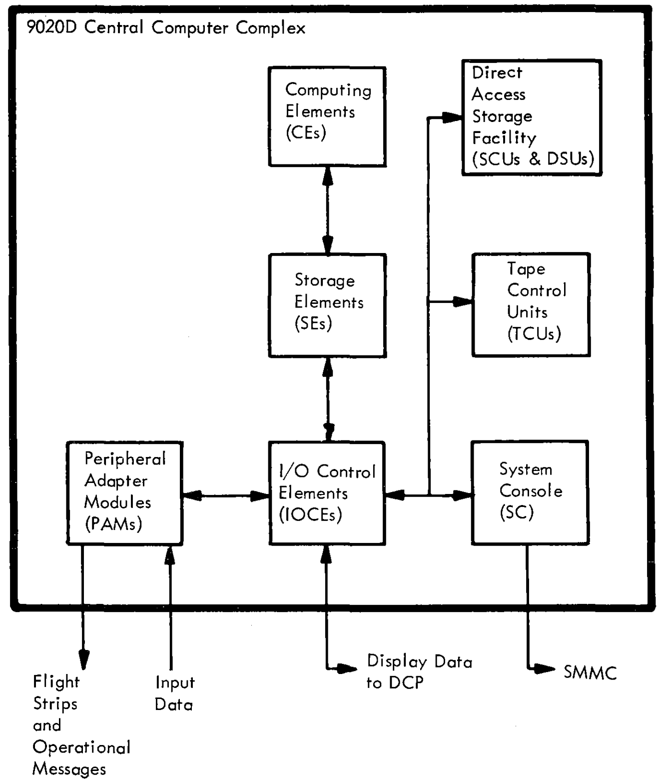
The 9020D system is designed to operate under a control program (sometimes called a CCC "monitor" or "supervisor"). The control program for the 9020 CCC systems is called the executive control (EXC) program. Certain hardware implementation is provided specifically for the control program, e.g., certain instructions (called privileged instructions) are reserved for use only by this program.

As a result of these provisions, the EXC program may control the loading and execution of various subprograms; these subprograms run independently of the EXC program and of each other but may call upon the EXC program for various services. The EXC program is called via an "interruption" capability which is part of the 9020 architecture. This same interruption facility is used to inform the EXC program of various other exceptional or abnormal conditions such as the progress of an I/O operation or a malfunction in an element. This is discussed in further detail in Chapter 6.

In summary, the 9020D system is required to perform the ATC task of processing air traffic data in a reliable, fail-safe, and fail-soft manner. To accomplish this, the system is designed for reliability and quick repair, and is provided with battery backup and the ability to operate under a control program. The latter has available to it redundant elements which can be operated in four different operational states and which can be dynamically reconfigured to accommodate changing workload and malfunctions. Provision is made for the control program to monitor for malfunctions and other exceptional or abnormal conditions.

FUNCTION OF CCC SYSTEM ELEMENTS

Figure 1-2 shows, in simplified form, the internal makeup of the 9020D system. Although the system contains redundant elements for most of the elements shown in Figure 1-2, only one of each type is shown for simplification.



● Figure 1-2. Function of CCC Elements

The computing elements (CEs) form the nucleus of the system, providing the computational and logical capability necessary to execute programs and control the operation of other elements in the system. While only major data interfaces are shown in Figure 1-2, note that the CEs interfaces with almost every element in the system for configuration control and for error and abnormal condition monitoring.

As the prime element responsible for program execution (minor processing tasks can be delegated to the IOCE processors), the CE executes both the EXC program and the subprograms which accomplish the ATC task. These programs and the related data which they process are stored in Storage Elements (SEs). A maximum system can store over five million bytes of data in the SEs. The CEs fetch instructions and data from the SEs and store the processed data back into the SEs.

Input/output (I/O) operations are performed by the IOCEs under control of the CEs. The IOCEs can also perform processing tasks when such tasks are assigned to them by the controlling CE. This capability is referred to as the IOCE processor feature. The primary function of the IOCE is, however, to relieve the CE of the burden of fetching and storing data to be transferred to or from I/O devices. This leaves the CE free for processing tasks. IOCEs have access to the SEs so that this storing and fetching of data may proceed independently of CE operation once an I/O operation has been initiated by the CE.

Each IOCE has channels which connect it to I/O control units. These control units, in turn, control I/O devices either individually or in groups. Channels are of two types: selector and multiplexer. A selector channel can operate with only one I/O device until the operation is completed. This is called burst mode. A multiplexer channel, while it can operate in burst mode also, is designed to operate with a number of devices at the same time, time-sharing its data path with the various I/O devices. This is called multiplex mode. Via these I/O channels, the IOCE communicates with the following elements and devices:

1. Various peripheral equipment via an IBM 7289-02 Peripheral Adapter Module (PAM).
2. A channel of an IOCE in the DCP system or directly to similar computer display channel equipment.
3. Magnetic tape units via a tape control unit (TCU).
4. Disk storage via a storage control unit (SCU).
5. A 1052 Printer Keyboard, via a 1052 adapter housed in the System Console (SC).
6. A number of units via the SC:
   a. Certain indicators, switches, and alarms on the console.
   b. An IBM 2540 Card Read/Punch and an IBM 1403 High-Speed Printer via an IBM 2821 I/O Control Unit.
   c. The System Maintenance Monitor Console (SMMC).

A PAM connects to a multiplexer channel to interface with the IOCE. It contains adapter types that enable it to interface with many kinds of peripheral equipment to transfer data into and out of the CCC system. Adapters are available to interface with teletype lines, 1052's, radar digitizers, and so on. Adapter types are discussed in the PAM section of Chapter 2.

A TCU connects to a selector channel and controls up to eight magnetic tape units (tape drives). Magnetic tape is used for program loading and for bulk storage of data that is not required to be immediately and randomly accessible.

An SCU connects to a selector channel and controls up to five disk storage units (DSUs). The combination of an SCU and its attached DSUs is referred to as a direct access storage facility (DASF). Like tape, disk may be used for program loading. It may also be used for bulk storage of data which must be randomly accessible. Data stored on disk can be retrieved without searching through sequentially stored records as must be done with tape.

A single SC provides a central location for operator monitoring and control of the CCC system. No redundant SC is provided since all critical controls and indicators are duplicated elsewhere in the system.

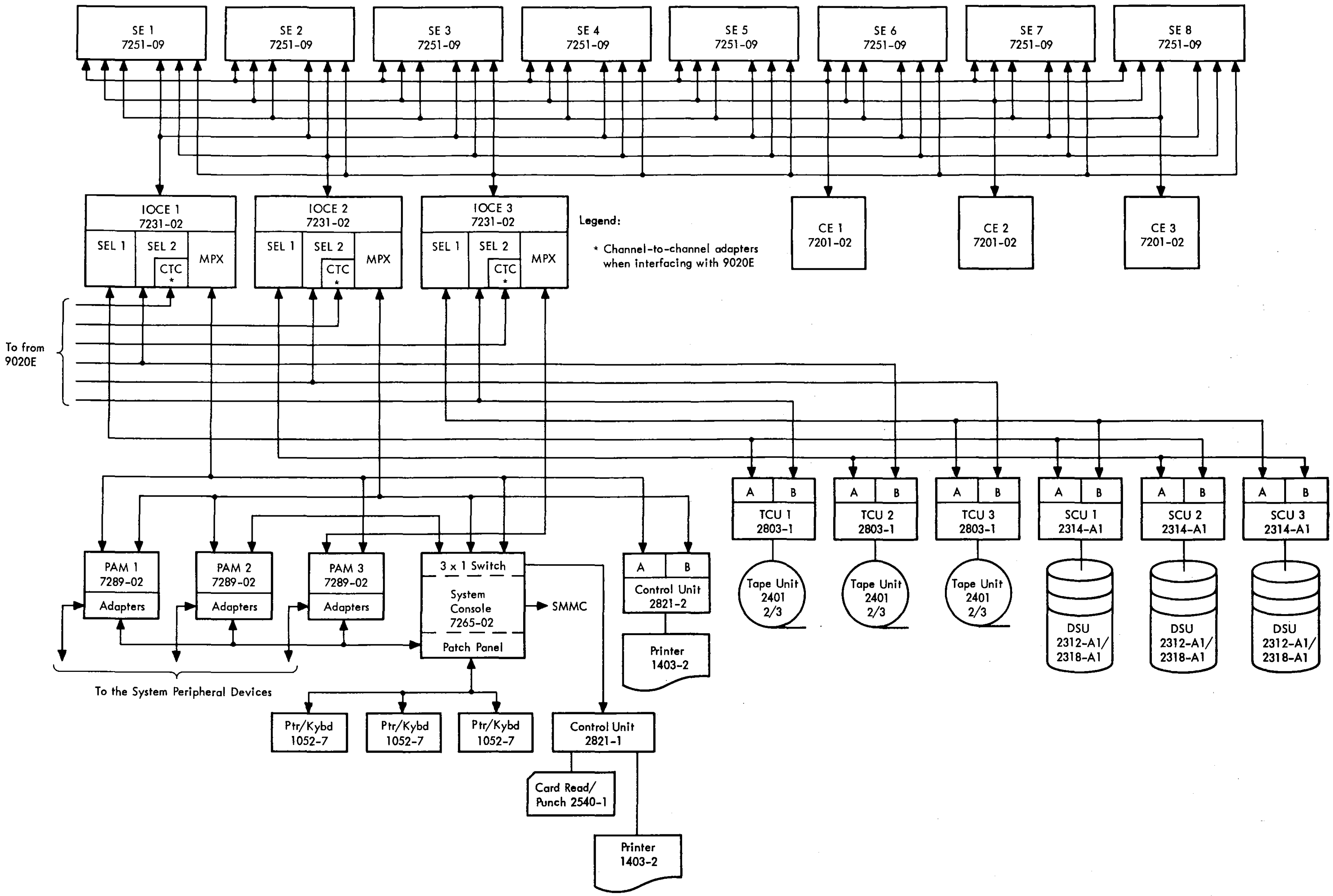
9020D CCC SYSTEM STRUCTURE

Figure 1-3 represents, in simplified form, a typical 9020D system configuration. This system can be expanded. A maximum system includes the following numbers of each element type: 4 CEs, 10 SEs, 3 IOCEs, 3 PAMs, 3 TCUs, 3 SCUs, and 1 SC. Note that, except for the SC, there are more than one of each element type, even in the smaller system shown in Figure 1-3. This system can be configured into as many as three subsystems, each functioning independently but under the ultimate control of the EXC program running in any one of the CEs.

The CCC is a multiprocessing system because more than one processor can be operating at the same time. Further, the processors are capable of communicating with each other without manual intervention. This is a requirement of a true "multisystem" (multiple computing element system). Successful multisystem operation under a single control program requires hardware facilities that make possible communication between CEs and the sharing of storage. These features, together with a control program such as the EXC program, enable the coordinated operation of multiple processors. This subject is covered in detail in Chapter 6.

The system shown in Figure 1-3 can be configured by the EXC program so as to tailor subsystems to particular tasks. The number of elements available is greater than the number required by the heaviest workload, so that a failing element may be replaced by a redundant element. When the workload permits, an entire subsystem may be dedicated to the testing or diagnosing of a malfunctioning unit or to the performance of tasks not directly related to the ATC task. The configuration control facility of the 9020D enables the EXC program to establish these subsystems by prescribing which elements may communicate. By enabling and disabling communication paths between elements, many different configurations may be structured. For example, in Figure 1-3, a subsystem might be configured which uses CE 1, SEs 3 and 4, IOCE 1, TCU 1, SCU 2, and PAM 3. The remaining elements could be configured into a second subsystem or simply left as redundant elements. The configuration control facility and the many interelement interfaces make the 9020D very flexible. Chapter 3 describes all of the interfaces in detail. Chapter 4 describes configuration control.

As noted previously, a failing element can be replaced by a redundant element through reconfiguration. This applies to CEs as well as any other element. Note, however, that a failure in the CE that is executing the EXC program can



● Figure 1-3. Typical 9020D Central Computer Complex also be accommodated by special hardware that permits another CE to automatically assume the task of executing the EXC program. Details of this procedure are in Chapter 7.

Replacement of an SE introduces some special requirements also. First, an alternate SE must be established as soon as the original configuration is formed so that certain critical areas of storage can be kept updated for use should replacement become necessary. This is a program consideration. Another consideration is the fact that each SE represents a fixed block of storage addresses which must be reconciled with the logical addresses from the program when a substitution is made. This is accomplished by a hardware-implemented address translation capability in the CEs and IOCEs. Addresses from the program are automatically translated into the proper physical addresses for the element actually occupying that logical block of addresses. This capability, and storage addressing in general, is described in Chapter 5.

A failure in an IOCE may be accommodated by replacing the IOCE. As can be seen in Figure 1-3, changes in data paths to the various I/O control units or devices are also required.

Malfunctions in IOCE channels, PAMs, I/O control units, or individual devices are allowed for in two different ways. In some cases redundant elements are required and in others multiple data paths are used. For example, control units are usually served by more than one channel; I/O devices are often served by more than one control unit. Depending on the nature of the malfunction, the EXC program can elect the appropriate option to circumvent the failing device or interface and continue operation.

As stated previously, the EXC program has available to it extensive system monitoring facilities. Data paths are provided for system monitoring which are not controlled by the CCR as are normal communication paths. In this way, the EXC program can be alerted to malfunctions and abnormal conditions even though the normal communication paths are blocked. The manner in which these system monitoring facilities are implemented in the 9020D system is described in Chapter 7. Individual element handling of error and abnormal conditions are described in Chapter 8, together with an explanation of how these function together to form an integrated monitoring and malfunction-handling approach.

This chapter has presented an overall view of the 9020D system in the context of the larger ATC environment in which it operates and the tasks it is required to perform. Concepts which underlie the structure of the system have been introduced. The system structure itself has been shown to consist of a number of elements. Chapter 2 enlarges upon the discussion of system structure by describing each of these elements.

This chapter enlarges upon the discussion of system structure presented in Chapter 1 by describing each of the system elements. These descriptions are brief and are intended to provide sufficient background for the system concepts (such as redundancy, reconfiguration, address translation, and system monitoring), discussed in the remainder of this manual. For detailed information about any particular element, refer to the theory manual for that element.

Certain elements described here are identical to elements used within the 9020E DCP system. These are the CE, IOCE, SE, and TCU. Some of the DCP functions of the CE are not used in the 9020D system, but the CE is, nevertheless, physically the same.

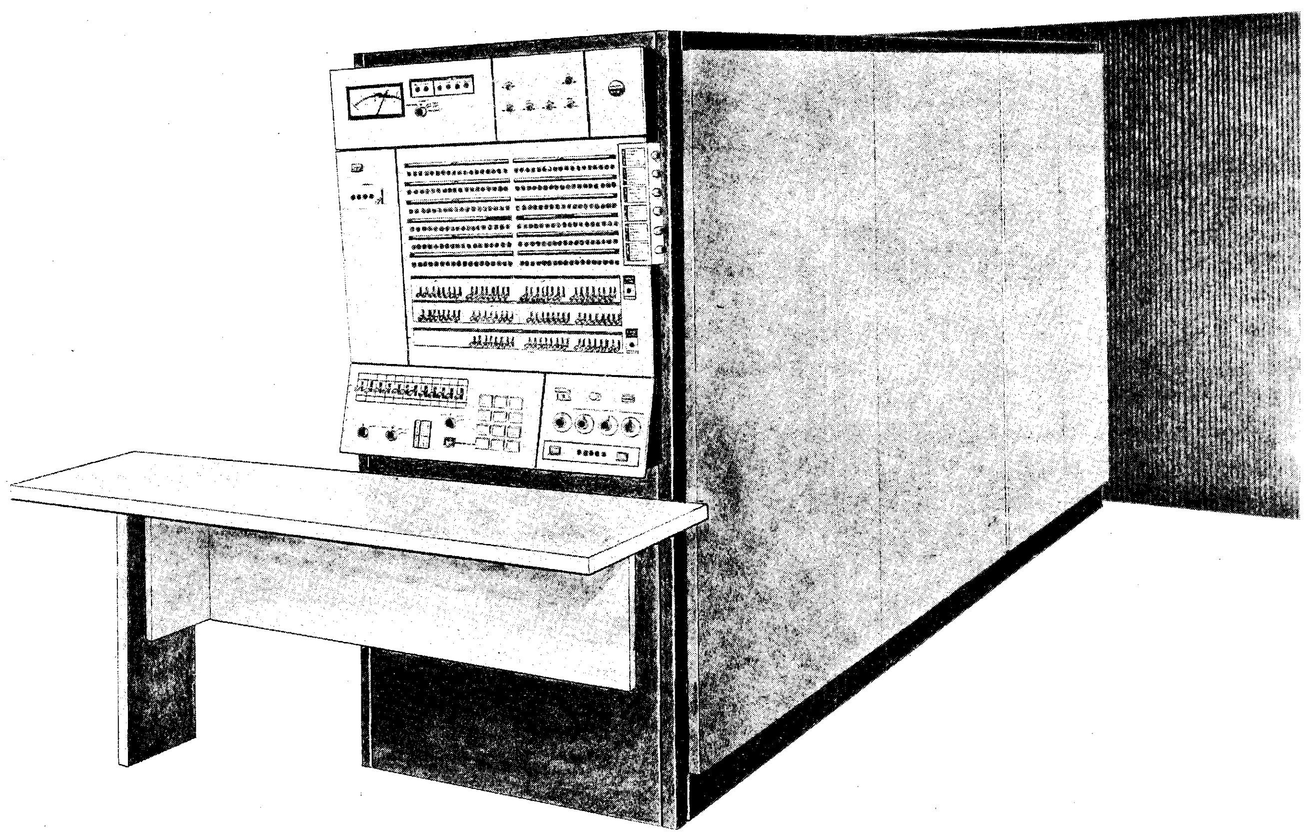
IBM 7201-02 COMPUTING ELEMENT (CE)

- Focal element within 9020D system.
- Maximum of four CEs can be installed.
- Contains no internal main storage.
- Interfaces with IOCEs for I/O operations.
- Self-contained and self-powered.
- Battery backup power.

The IBM 7201-02 Computing Element (CE), shown in Figure 2-1, is the focal element within the 9020D system. It provides the capability to establish and control the multi-element computer system and the facility for computation and logic required to process data for air traffic control.

A maximum of four CEs may be installed in the 9020D system. Each CE is a self-contained element capable of operating the executive control (EXC) program and controlling other CEs or of operating as part of a subsystem under control of another CE. Thus, CEs are interchangeable in case of a malfunction.

The CE contains no internal main storage; it interfaces with standalone storage elements (SEs) for the storage of



instructions and data. The CE interfaces with I/O Control Elements (IOCEs) for all I/O operations so that maximum time is devoted to processing. Interfacing between each CE and every major element and unit in the system makes possible multisystem control and monitoring.

The CE is a self-powered unit and is provided with battery backup power capable of sustaining it for approximately 6.5 seconds in case of loss of external power.

Interfacing

- CE-CE interface for configuration, address translation data, and direct control.

- CE-SE interface for transfer of data.

- CE-TCU, SCU, and PAM for configuration control and error monitoring.

- CE-IOCE interface for configuration, address translation data, and I/O control.

- CE-SC interface for remote monitoring and control.

As the controlling element in the system, the CE interfaces with every major element and unit. Figure 2-2 shows this interfacing in simplified form. Five main types of interfaces are shown:

1. CE-CE
2. CE-SE
3. CE-TCU/SCU/PAM
4. CE-IOCE
5. CE-SC

The CE-CE interface provides data paths for configuration information, address translation information, and direct control. Note that each CE also interfaces with itself for these purposes. Other interface lines conduct the system

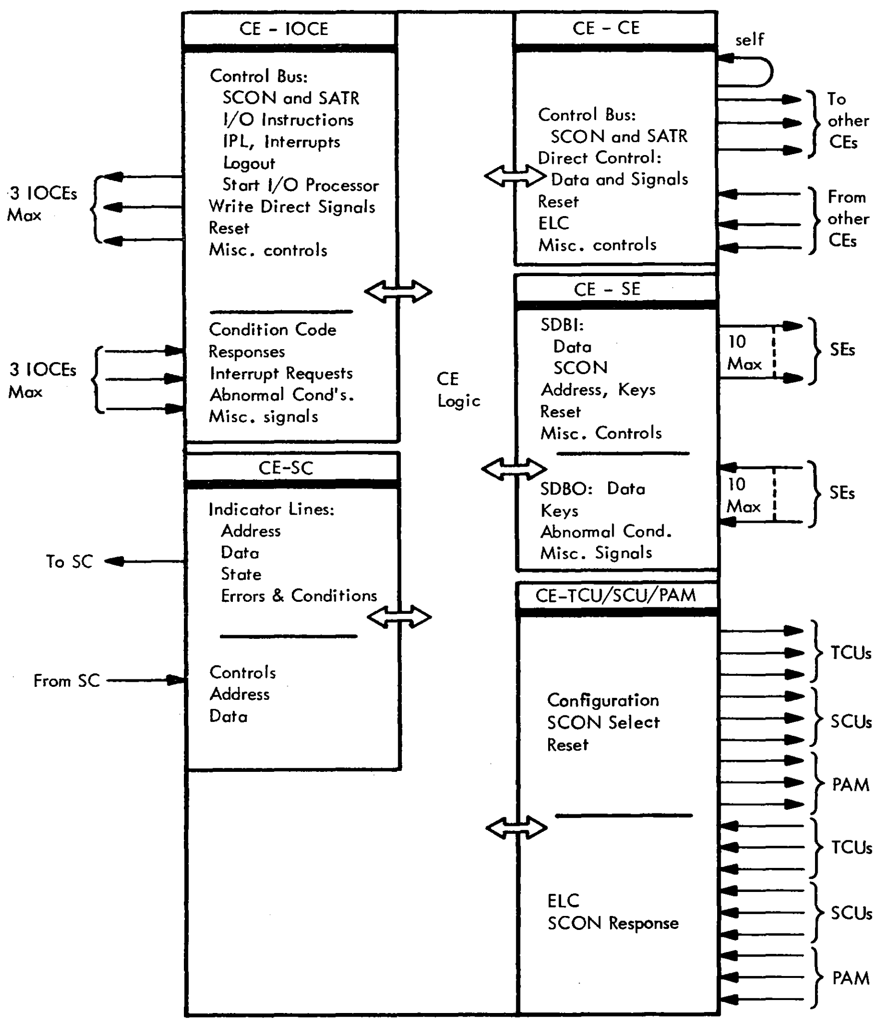


Figure 2-2. Computing Element Interfacing

reset, direct control signals, and the element check (ELC) signal. These control lines enable any CE to monitor the operation of the other CEs and to coordinate them in multisystem operation.

Each CE interfaces with each SE in the system. A storage data bus-in (SDBI) and a storage data bus-out (SDBO) provide for the transfer of data between the CE and storage a doubleword at a time. The SDBI is also used to transfer configuration data to SEs. No separate configuration bus exists to these elements. Separate interface lines are provided for storage addresses and keys. A number of additional interface lines permit synchronized operation and permit the CE to monitor for SE errors and abnormal conditions.

The CE interfaces with TCUs, SCUs, and PAMs. These interfaces are very similar. Provision is made for configuration data to be transferred to these units and for the necessary signals to permit the CE to select the units for configuration and monitor them for errors and abnormal conditions.

The CE-IOCE interface provides for control of the IOCE by the CE but no direct data path exists between the two elements. Shared storage is used for this purpose. The major portion of the CE to IOCE interface consists of a control bus used for the following purposes: configuration and address translation information, I/O instructions, IOCE processor start, initial program load (IPL), interrupts, and logout. The CE's preferential storage base address (PSBA) is placed on the bus to enable the IOCE to locate the CE's preferential storage area (PSA) for I/O instructions, IPL, interrupts, and logout. A CE's PSA is a program-established block of storage set aside for certain status and control information critical to the operation of the automatic interruption facility, IPL, I/O operations, and logout.

The IOCE-to-CE interface lines consist mainly of signal lines which permit CE and IOCE operation to be synchronized when necessary and which enable the CE to monitor for errors and abnormal conditions. Direct control signals are provided between CEs and IOCEs but no direct control data path exists.

The CE interfaces with the System Console (SC) to enable the CE status to be displayed at the console and to enable various CE control panel functions to be controlled remotely from the console.

In all the interfaces mentioned, certain common characteristics exist. Provision is made for the CE to configure all elements and to monitor them for abnormal conditions. A system reset signal is also provided to each element.

Refer to Chapter 3 for a detailed discussion of element interfacing.

Internal Organization

Figure 2-3 shows the internal organization of the CE in simplified form. For purposes of this description, the CE is divided into eight major areas:

1. Control
2. Address translation
3. Storage control interface (SCI)
4. Instruction fetch and operand pre-fetch logic
5. Instruction execution logic
6. Interruptions and exceptional conditions
7. External interfaces
8. Manual controls and maintenance features

Control

- Clock
- ROS
- PSW
- CCR

The control portion of the CE consists primarily of: (1) the clock, (2) read-only storage (ROS), (3) the program status word (PSW) register, and (4) the configuration control register (CCR). The clock and its associated timing circuitry cause the CE to operate on a basic cycle time of 200 ns. The most significant feature of the control circuitry is the ROS, which replaces most conventional sequence triggers and control lines.

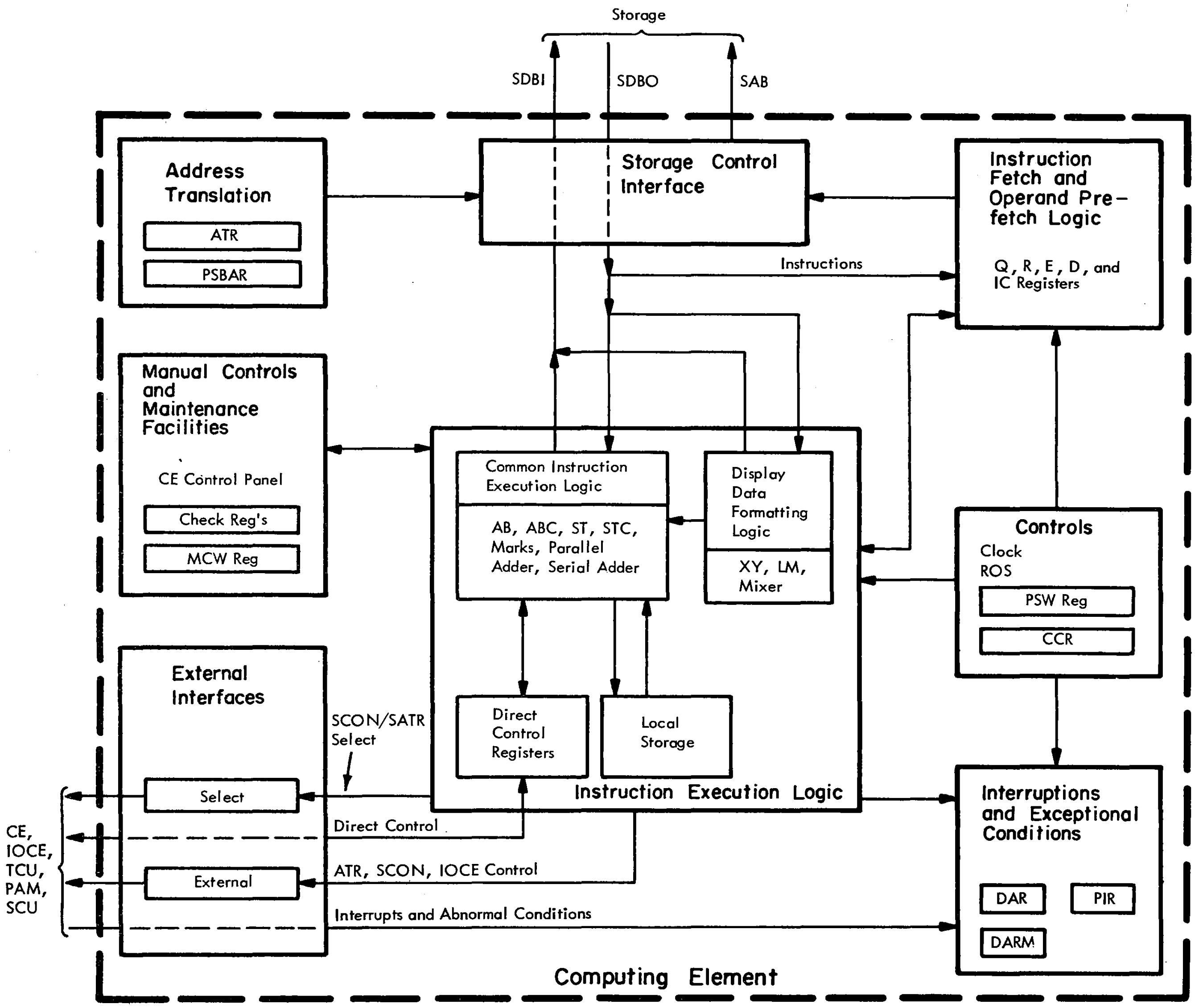
The ROS contains 2816 100-bit words. Each ROS word is divided into 22 control fields. Bit patterns contained in these fields constitute coded micro-orders. Signal lines representing these micro-orders directly control the data flow within the CE. Also coded into the ROS word is the address of the next ROS word to be accessed. This address may be modified by various branching conditions. In this manner, sequences of ROS words are formed into microprograms capable of controlling entire operations or instructions. The data stored in the ROS unit can be modified only by physically changing the components.

To achieve greater speed and efficiency, a number of control functions are hardware-implemented. For example, the fetching of instructions when the doubleword buffer register requires refilling is initiated by hardware while the ROS continues with instruction execution.

The PSW register and the CCR also contribute to the control of the CE by establishing such factors as: which CE instructions can be performed, which interruptions are permitted, with which other elements the CE can communicate, and so on.

Address Translation

- Translation from logical to physical address.



●Figure 2-3. Computing Element Internal Organization

- ATR used for normal access translation.
- PSBAR used for PSA access translation.

The address translation portion of the CE is shown at the upper left in Figure 2-3. This portion provides translated addresses to the storage control interface (SCI) so that logical addresses from the program can be used to access data and instructions from the physical storage which is currently configured. Two registers are primarily responsible for this translation: the address translation register (ATR) and the preferential storage base address register (PSBAR). The ATR translates addresses during normal storage accesses. PSBAR is used to keep track of the CE's PSA location and to translate addresses for PSA accesses. These registers are set by the control program.

Storage Control Interface (SCI)

The SCI contains the logic necessary for handling storage requests. It is responsible for synchronizing the CE operation with storage operation. This ability to synchronize the two rests chiefly on the SCI's ability to stop the CE clock briefly when necessary.

Instruction Fetch and Operand Prefetch Logic

- Instructions sequence through Q, R, and E registers.
- IC and D registers used for addressing instructions and operands.

The CE contains a doubleword instruction buffer called the Q-register which is kept filled via hardware circuitry. Instructions are passed on to the R-register for predecoding and to permit operands to be prefetched so that they are available when the CE has finished executing the current instruction. An E-register is used for storing the instruction currently being executed.

Two registers are provided for addressing storage: the D-register and the instruction counter (IC). In general, though with exceptions, the D-register is used for data addresses and the IC is used for instruction addresses.

Instruction Execution Logic

- Registers and counters.
- Parallel and serial adders.
- Local storage.
- Special logic for display instructions.

As shown in Figure 2-3 the instruction execution logic is divided into four general areas. The common instruction execution logic consists of adders, registers, counters, and the associated data paths. The most salient functional units in this area are the two doubleword registers (AB and ST) and the doubleword parallel adder. The parallel adder provides for rapid processing of binary integers. It is capable of performing certain logical functions as well as arithmetic functions.

A single-byte serial adder enables binary, decimal, or logical functions to be performed. For decimal operations, data may be gated to the serial adder from any byte position of the AB and ST registers.

The common instruction execution logic operates in conjunction with a local storage which contains 16 general-purpose registers (single word), four floating-point registers (doubleword), and one working register. All the local storage registers are available to the programmer except the working register.

Two registers (F and G) provide for single-byte data buffering for direct control functions. This makes possible the direct transfer of data between CEs one byte at a time.

Virtually all of the instructions in the CE's instruction set are performed by the logic discussed so far. The display data formatting logic augments the common instruction execution logic during execution of certain display instructions when the CE is installed in a DCP environment.

Interruption and Exceptional Conditions

- Interruptions detected by hardware.
- PSW enables selective masking of interruptions.
- PIR records IOCE-processor interruptions.
- DAR records interruption requests from other elements.
- DARM provides selective masking of DAR interruption requests.

Logic is provided in the CE to enable five types of interruptions to automatically branch the program to routines programmed to handle them. The status of the CE and of the interrupted program is automatically saved to provide an immediate return after the interruption is handled. These interruptions may result from program errors, subprogram calls to the control program, machine checks, I/O equipment requiring attention, an IOCE processor requiring attention, or a variety of external requests. Bit positions in the PSW enable the program to selectively mask off these interrupt requests so that they may be handled in an orderly fashion.

Additional registers in the CE provide for the special considerations involved in IOCE processor and external interruptions. The processor interruption register (PIR) retains the identity of the IOCE requesting an IOCE processor interruption. The diagnose accessible register (DAR) retains the source of interruption requests originating outside the CE as a result of malfunctions or abnormal conditions in other elements. Certain abnormal conditions occurring within the CE also set bits in the DAR. A DAR mask (DARM) register provides for selective masking of DAR interruption requests.

In addition to interruption requests, hardware and microprogram facilities are provided for handling exceptional conditions that arise during processing.

External Interface

This functional area of the CE contains the line drivers and receivers and the gating circuitry for the many interfaces with other elements in the system. To a large extent the interface gating is derived from the CCR.

Also related to the external interfaces are the select and external registers. Bits set into the select register by the CE determine which elements will be requested to accept configuration or address translation information. Data to be transferred to other CEs, IOCEs, TCUs, SCUs, and PAMs for configuration purposes passes through the external register. The external register is also the source of control buses to the IOCEs over which the CE controls IOCE operation.

Manual Controls and Maintenance Features

- Control panel.

- Parity check logic.
- Scan-in, logout logic, and FLTs.
- Microprogram diagnostics.
- Ripple tests.
- Marginal checking.

This area of the CE includes the control panel and logic for malfunction detection and malfunction isolation. Extensive checking circuitry continually checks for parity errors in instructions or data being transferred within the CE. Check registers are provided to indicate such errors when they occur.

In addition to this checking circuitry, scan-in and logout circuitry permits testing of the CE at the logic block level via fault locating tests (FLTs). The logout facility also permits the status of the CE at the time an error occurs to be stored in main storage for subsequent program analysis.

Other built-in maintenance facilities include a microprogram diagnostic for checking various registers, microprogrammed storage ripple tests for testing the ability of the CE to access main and local storage, and marginal checking facilities which permit certain voltages and timings to be varied to detect circuitry which is operating marginally.

IBM 7231-02 I/O CONTROL ELEMENT (IOCE)

- A maximum of three IOCEs.
- Performs the I/O functions within CCC system.
- Performs IOCE processor operations.
- IOCE functions are initiated by CE.
- Battery backup power.

The IBM 7231-02 I/O Control Element (IOCE) has two major functions: an IOCE processor function and an IOCE channel controller function. The channel controller function enables I/O units to be attached to the 9020 system. The IOCE processor function permits processing to be performed by an IOCE.

I/O control units with their associated devices are attached to the IOCE (Figure 2-4) by one multiplexer

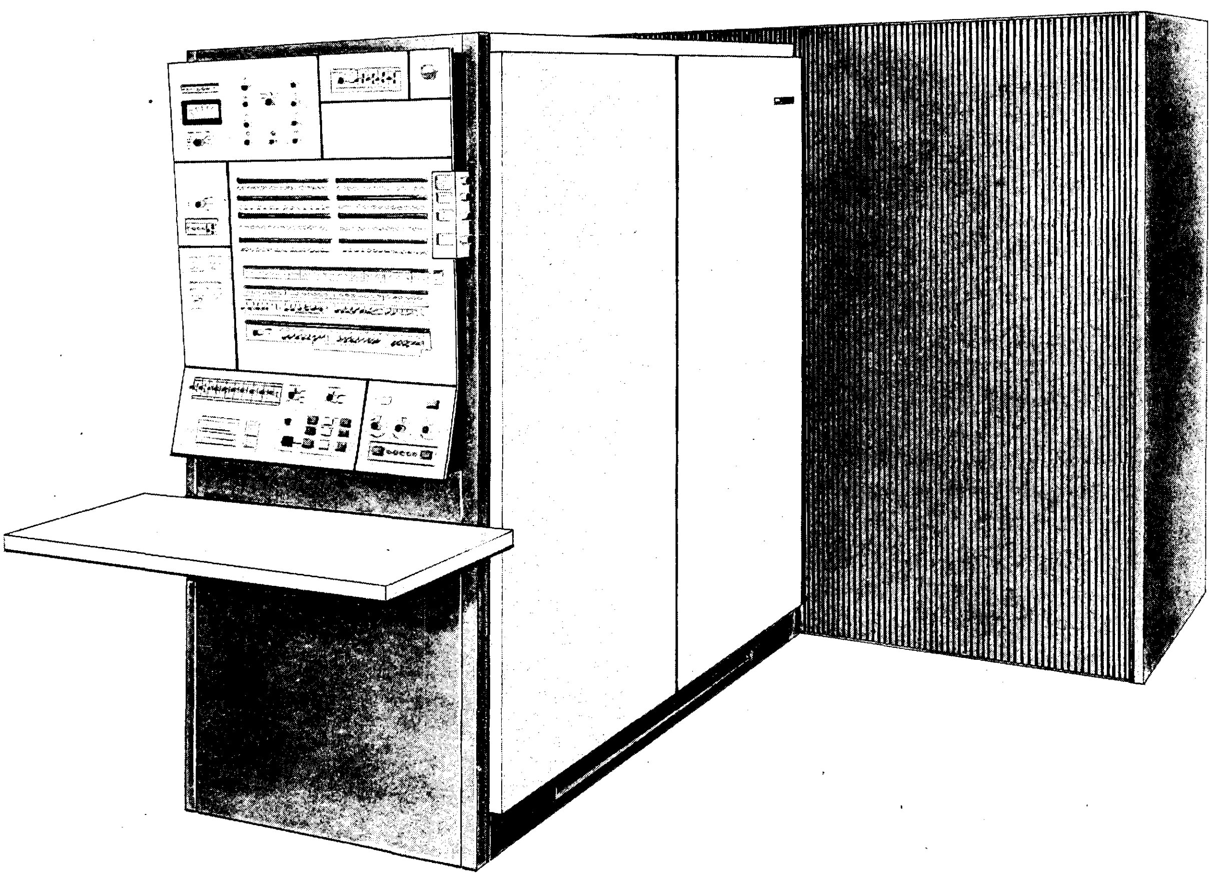


Figure 2-4. IBM 7231-02 I/O Control Element (IOCE)

channel and three selector channels. The 9020 system, however, is restricted to a maximum of eight selector channels: three on IOCEs 1 and 2 and two on IOCE 3.

The IOCE operates in conjunction with the CE and is dependent on the CE for the initiation of all operations.

Up to three IOCEs may be incorporated into the 9020 system. The EXC program assigns (configures) these IOCEs as necessary to meet the demands of the system. This assignment is accomplished by programming and does not require operator intervention.

The IOCE power system is self-contained and is provided with battery backup. The battery backup operation, like that of the CE, can sustain operation of the IOCE for 6-1/2 seconds if there is a loss of external power.

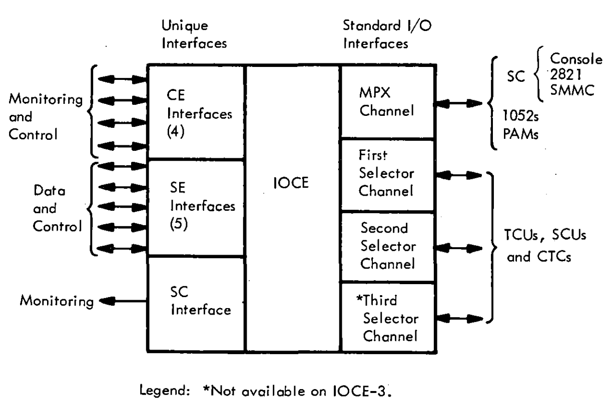
Each IOCE is provided with a master circuit breaker so that ac power can be removed for maintenance purposes. An IOCE can be powered up and down without disturbing other elements in the system.

Interfacing

- Unique interfaces with CE, SE, and SC.

- Selector and multiplexer channels are standard interface.

The IOCE interfaces are shown in Figure 2-5. Some of these interfaces are unique but many are standard I/O interfaces (selector and multiplexer channels). These standard interfaces are described briefly in Chapter 3. The IOCE communicates with CEs, SEs, and the System Console (SC) via unique interfaces. While the SC uses the unique interface for monitoring the IOCE, these two elements are primarily connected via the multiplexer channel which is used for communication between the IOCE and three main areas: (1) the system console indicators and sense switches, (2) the reader/punch and printer and (3) the System Maintenance Monitor Console (SMMC). Refer to Chapter 3 for a detailed discussion of element interfacing.



- Figure 2-5. IOCE Interfacing

Within the 9020D System, the selector channels are used to communicate with magnetic tape via the IBM 2803-01 Tape Control Unit (TCU) and with disk storage units via the IBM 2314-A1 Storage Control Unit (SCU). The selector channels are also used for communication with the 9020E Display Channel Processor (DCP) through the use of channel-to-channel (CTC) adapters. It is via these adapters that display data is transferred to the DCP system. When other computer display channel equipment is used, it connects directly to a selector channel; the CTC is not used in this case.

The CTC adapters provide communication between the CCC system and the DCP system by allowing the rapid transfer of large blocks of data from a storage element in one system to a storage element in the other system. A CTC is physically housed in one of the two channels between which communication paths are required. Figure 2-6 shows an example of CTC adapter usage. In a particular IOCE, up to two CTC adapters may be installed, one in selector channel 1 and one in selector channel 2. The CTC adapter appears to each channel as a standard control unit and is connected by means of the standard I/O interface described in under "Standard I/O Interface Summary" in Chapter 3.

For detailed information, refer to the Channel-to-Channel Adapter, Model 6006A, Theory-Maintenance Manual, and its associated Maintenance Diagrams manual.

Internal Organization

Figure 2-7 shows the internal organization of the IOCE in simplified form. The heavy lines show the major breakdown into channels, common channel, and the common logic unit (CLU). The small arrows show control paths and the broad arrows show major data paths.

Each IOCE contains the logic necessary to:

1. Execute CE-initiated instructions.
2. Control data flow between storage elements and I/O units.
3. Execute the standard instruction set during maintenance or IOCE processor operations.
4. Operate MACH storage within the IOCE.
5. Operate and control one multiplexer channel.
6. Operate and control up to three selector channels.

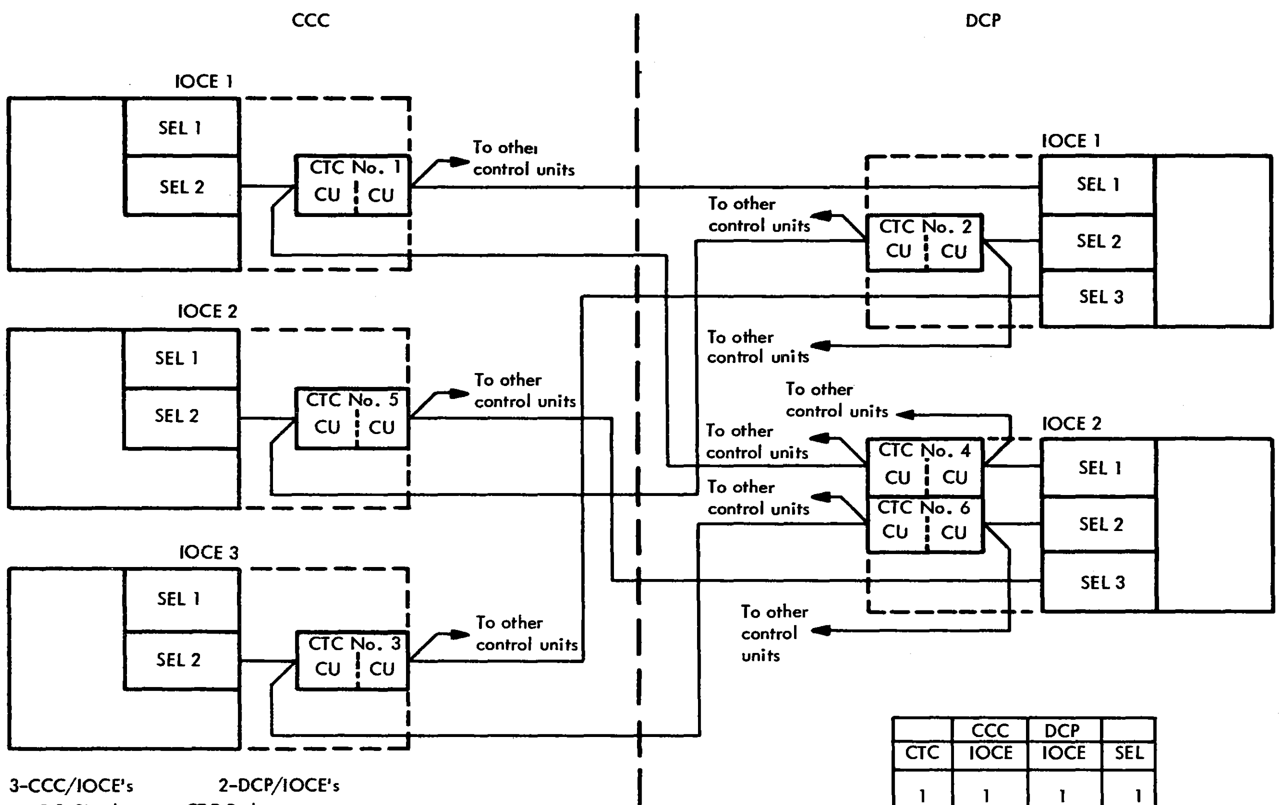
This logic is described in detail in Field Engineering Theory of Operation, 7231-02 Input/Output Control Element. Brief descriptions of major areas of the IOCE follow.

Common Logic Unit (CLU)

- Performs basic arithmetic and logic functions.

- Contains read-only storage (ROS).

- Consists of adder, mover, registers, and data paths.



	CCC	DCP	
CTC	IOCE	IOCE	SEL
1	1	1	1
2	2	1	2
3	3	1	3
4	1	2	1
5	2	2	3
6	3	2	2

3-CCC/IOCE's 2-DCP/IOCE's

- 2-Simultaneous CTC Paths.
- Reconfiguration on 1-subsystem does not require reconfiguration in other but does require that other be notified through programming.
- Dual path maintained.

Figure 2-6. Sample Channel-to-Channel Usage

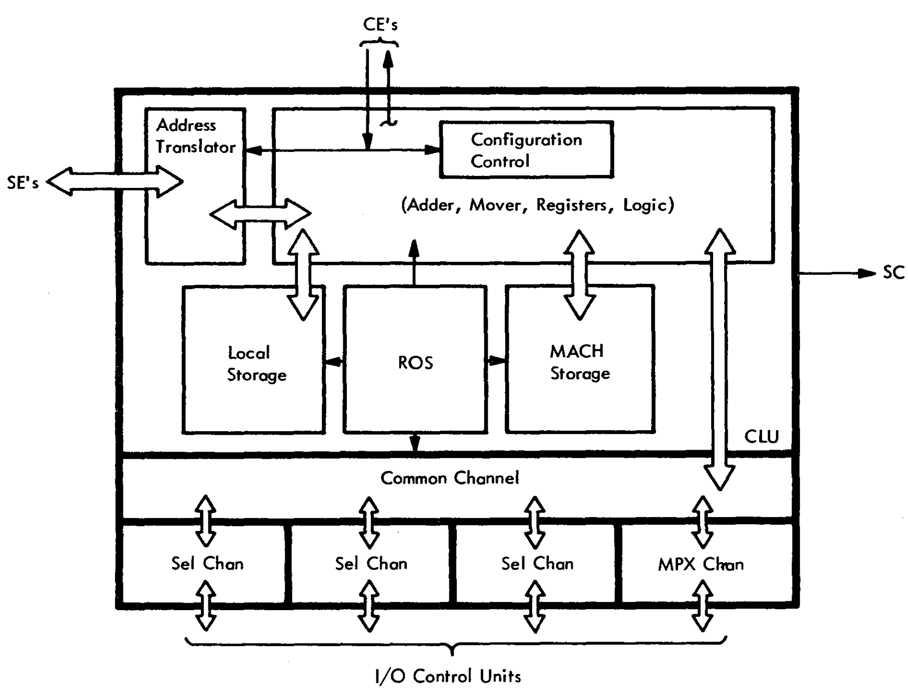


Figure 2-7. IOCE Internal Organization

The common logic unit (CLU) consists of the logic necessary to perform basic arithmetic and logic functions. The CLU includes a ROS used for microprogram control of the IOCE plus an adder, mover, data paths, and registers used for temporary storage of data and control words.

Most of the data transfers within the CLU and to or from a storage element are in full words (32 data bits). Data parity on each eight-bit byte is checked during the transfer.

The CLU contains fullword registers, which are used for storing channel data and control words, located in a 64-word, 0.5-usec local storage. Other locations in local storage are working registers and general registers used in channel, diagnostic, and IOCE processor operations.

Data flow is controlled by a capacitor ROS unit operating on a 0.5-usec cycle. Each 90-bit word is a microinstruction that controls the operation of the IOCE for one 0.5-usec cycle. Groups of microinstructions are linked to form a microprogram. A microprogram controls the entire sequence of cycles forming a complete operation; for example, the transfer of a data word to a channel. The data contained in this unit can be modified only by physically changing the components.

MACH (Maintenance and Channel) Storage

- Contains channel control and status information.

- Can contain instructions and data for an IOCE processor.

- Provides standalone maintenance capabilities.

- Comprises 131,072 bytes of storage.

This 131K byte MACH storage is used as storage for multiplexer channel functions during I/O operations in the active ATC system; MACH also contains data and instructions used during IOCE processor operations.

MACH storage is a coincident-current magnetic core storage unit designed to operate at a cycle time of 2.0 usec. The method of address selection is direct drive of coincident current through each segment of the array. Each plane of the array determines two bits, and results in a 36-bit readout in the 18-plane array.

Addressing of MACH is from bits 15–29 of the storage address register (SAR). The top 4,096 bytes (1,024 words) are addressed by special multiplexer channel micro-orders. This area of MACH is used for multiplexer channel operations and is referred to as "bump" storage. The remaining addresses are used for channel data and for IOCE processor data and instructions.

Multiplexer Channel

- One multiplexer channel per IOCE.

- Has 256 subchannel capability.

Each IOCE contains one multiplexer channel capable of controlling several low- or medium-speed I/O devices simultaneously or one higher-speed unit in burst mode.

Within the limits imposed by its data-transfer capabilities, the multiplexer channel can handle any standard interface device. A maximum of eight control units can be directly attached to the multiplexer channel. Up to 256 subchannels can operate simultaneously. The upper 4096 locations of MACH storage are used to store control words for each of the 256 possible subchannels.

Devices attached to the multiplexer channel include:
IBM 1052 I/O Printer/Keyboard
IBM 2821 Control Unit for the 2540 and 1403
Peripheral Adapter Module (PAM)
System Console

Selector Channel

- Handle high-speed I/O devices.

- Two selector channels per IOCE.

- Expandable to three on first two IOCEs.

Each IOCE contains two selector channels capable of handling high-speed I/O devices. These two selector channels are expandable to three on the first two IOCEs to provide a maximum of eight selector channels within the 9020 system.

A selector channel controls the data flow of only one device at a time (burst mode). A maximum of eight control units may be directly attached to a selector channel. Each channel can address 256 devices. A selector channel can control any standard interface device whose data rate does not exceed that of the channel.

Devices attached to the selector channel include tape control units (TCUs), storage control units (SCUs), and channel-to-channel (CTC) adapters.

IOCE I/O Operations

- IOCEs do not initiate I/O operations.

- I/O data is transmitted between IOCE and storage.

- CE is signaled at end of operation.

In the active ATC system, the IOCEs cannot themselves initiate I/O operations. Instead, they must rely on active CEs to initiate all I/O functions.

The IOCE responds to the following I/O and supervisor instructions initiated by a CE:

Start I/O (SIO)
Test I/O (TIO)
Halt I/O (HIO)
Test Channel (TCH)
Set PCI (SPCI)
Set Configuration (SCON)
Set Address Translator (SATR)

A CE recognizes an I/O instruction and signals an IOCE (over the CE-IOCE interface) to perform the necessary operation. The IOCE obtains the contents of the channel address word (CAW) from the preferential storage area (PSA) of the designated storage element (SE). The CAW defines the location of the channel command word (CCW), which in turn defines the command to be executed, the location in storage where the I/O data bytes are to be transferred, and various data controls such as byte count, flags, etc. This information is stored in either MACH (bump) storage for multiplexer channel operations, or in local storage for selector channel operations.

The IOCE sends the operation to the I/O device and signals the CE with the appropriate condition code and response. The CE is now free to continue the main program while the IOCE simultaneously continues with the data transfers.

Completion of the I/O operation (without CCW chaining) results in an interruption of the CE and the storing of the channel status word (CSW) in the PSA of the designated SE.

Three elements (CE, IOCE, and storage) are directly involved in the overall I/O data transfer operation. The following should be noted with respect to the transfer of control and data information:

1. Control information (indicating one of the five I/O, SATR, or SCON instructions) is transferred between the CE and IOCE.
2. Control information such as CAW, CCW, and PSW is transferred between the IOCE and the designated storage. The CE is not involved at this point, except for having designated the storage and PSA.
3. Data transfers concerning the multiplexer and selector channels are directly between the IOCE and storage. There is no data transfer between the IOCE and CE. In addition to the I/O operations just mentioned, the IOCE will accept signals over the CE-IOCE interface to perform the following special functions:
   a. Initial Program Load (IPL)
   b. Logout
   c. Permit Interrupt

IOCE Processor Operations

The IOCE processor feature permits an IOCE to process data as well as to control I/O operations and units. In processing data, the IOCE uses a subset of the 9020 system instruction set. The subset does not contain floating-point or decimal arithmetic instructions. From the programmer's viewpoint, I/O operations and IOCE processor operations are concurrent with and independent of one another. An IOCE processor operation is started by a controlling CE and is executed by an IOCE. A CE sends a start I/O processor instruction to an IOCE, which loads a PSW from a designated location in MACH or main storage and proceeds with processing in the same manner as in a CE. Data and instructions for a processor come from MACH or main storage (an SE). Once an IOCE processor has been started, the CE can send a write direct command to stop, start, or interrupt the processor. The IOCE processor can execute a write direct command (external interrupt) to the controlling CE, causing an external interrupt in the CE (if masked on). The interrupt condition remains in the processor interruption register of the CE until cleared by the CE through a diagnose instruction.

IBM 7251-09 STORAGE ELEMENT (SE)

- Solid-state core storage unit.
- Capacity of 524,288 bytes of data.
- Ten SEs maximum on 9020D system.
- Self-contained power supplies.
- Battery backup power.
- Store and fetch protection.

The IBM 7251-09 Storage Element (SE) is a solid-state core storage unit (Figure 2-8) capable of storing 524,288 bytes of data. The SEs (maximum of ten) provide the main storage for data being processed by the 9020D system.

The SE uses coincident-current magnetic core storage arrays. The contents of storage are not destroyed under normal poweron/off sequences. Therefore, if the element is not in operation when power is removed, the stored data will be valid when proper power is restored to the element.

Each SE is a completely self-contained unit with its own power supplies. Each is provided with a master circuit

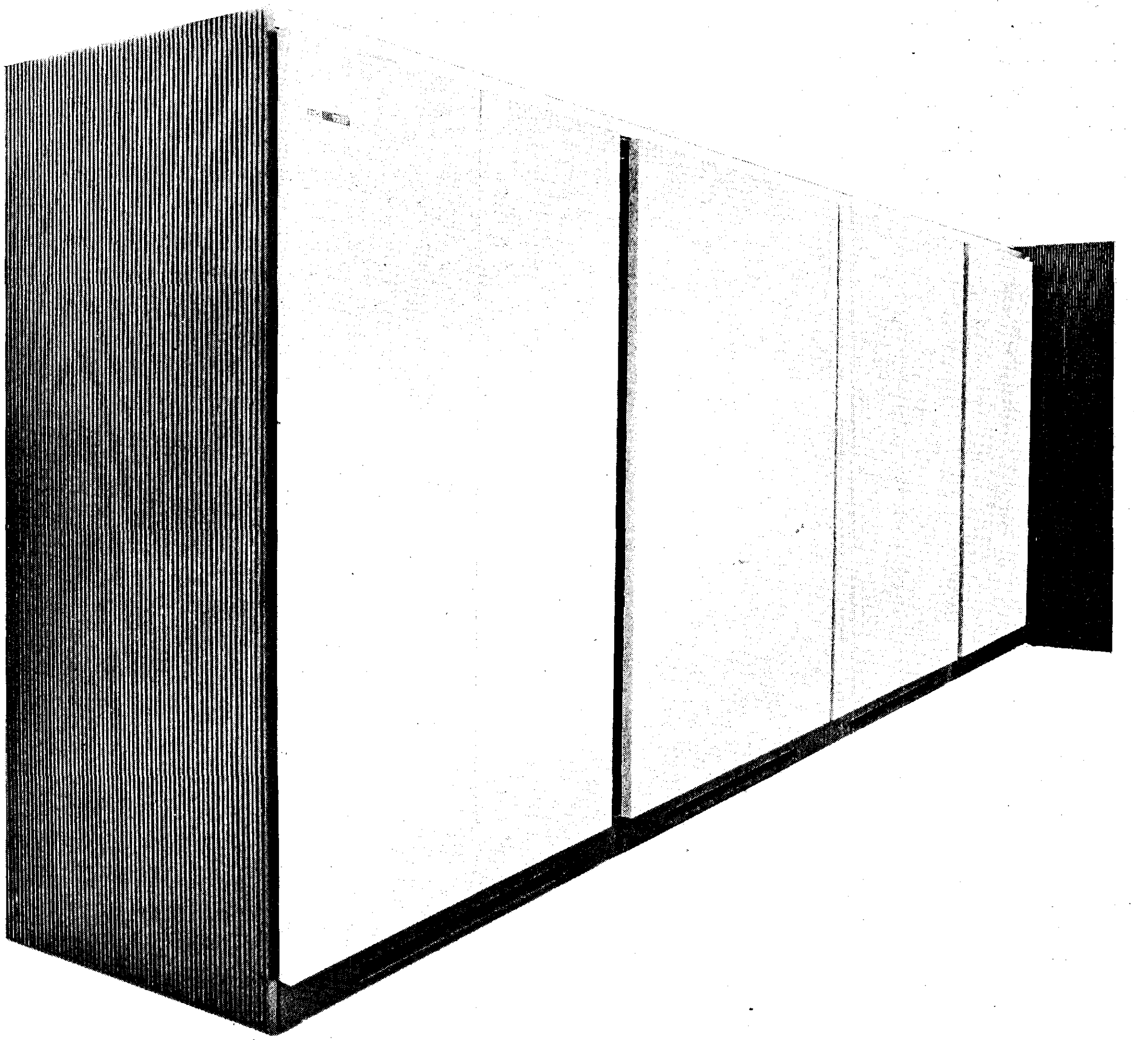


Figure 2-8. IBM 7251-09 Storage Element (SE)

breaker so that AC power can be removed for maintenance purposes. An SE can be powered up or down without disturbing the operation of other elements in the system. Power control and maintenance panels provide for off-line maintenance and testing of an SE without disturbing other elements in the system.

A battery backup power source in each SE permits operation to continue to a logical stopping point (checkpoint) in case of loss of external power. In this manner a normal power-down sequence may occur even after the loss of external power so that data in the SE is preserved. SEs can operate on battery power for 5-1/2 seconds.

Interfacing

Seven interfaces provide interconnection between each SE and the CEs and IOCEs. An additional interface between each SE and the system console makes SE status available for monitoring at the console panel. Refer to Chapter 3 for a detailed discussion of element interfacing.

Storage Addressing

All bytes of the ten SEs are directly addressable by each of four CEs and three IOCEs. Priority and configuration circuits in each SE permit the honoring of asynchronous and simultaneous requests for storage from all configured CEs and IOCEs.

Each SE has a fixed address range which is determined by plug cards which are plugged at the time of installation. The range of addresses for each SE is shown in Figure 2-9. In the event of an SE malfunction, one SE may be substituted for another. The address translation capability of the 9020 system translates logical addresses from the

SE	Decimal Address Range
1	000,000 - 524,287
2	524,288 - 1,048,575
3	1,048,576 - 1,572,863
4	1,572,864 - 2,097,151
5	2,097,152 - 2,621,439
6	2,621,440 - 3,145,727
7	3,145,728 - 3,670,015
8	3,670,016 - 4,194,303
9	4,194,304 - 4,718,591
10	4,718,592 - 5,242,879

Figure 2-9. SE Address Ranges (Bytes)

program to the correct physical addresses for the actual SE occupying that address range.

Storage Protection

Each SE contains a storage protect buffer which provides a protection key for each contiguous block of 2048 bytes of storage. These keys can be set and inspected by executing the Set Storage Key and Insert Storage Key instructions. Storage protection is described more fully in Chapter 5.

Internal Organization

The SE is composed of two logical areas: a storage switching unit (SSU) and a storage section (Figure 2-10).

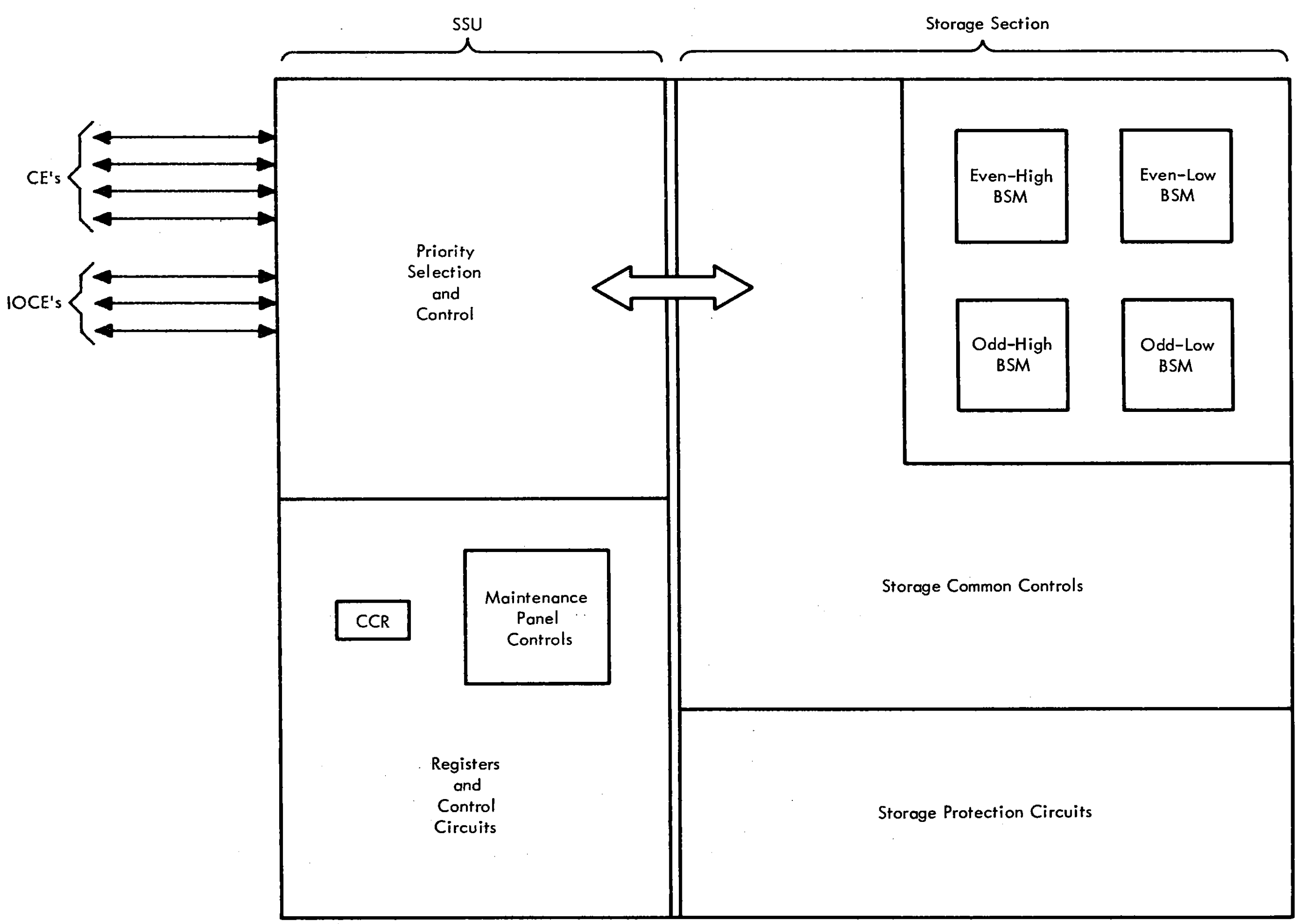


Figure 2-10. Storage Element Organization

Storage Switching Unit

- Establishes request priority.
- Synchronizes CE and IOCE requests.

The SSU controls and synchronizes the usage of the SE's storage section by a maximum of seven users: four CE's and three IOCE's. Two processes are involved. The first is the establishment of priority for each user request, accomplished by the priority selection and control logic. The second process entails adapting the storage section to the different speeds and data bus widths of the two user types. The CE can keep pace with the 750-ns cycle time of the storage section; the IOCE requires a minimum of 2.5 usec. The CE uses a doubleword data bus; the IOCE uses a singleword bus. Further, the IOCE time shares its data bus with addresses rather than use a separate storage address bus as does the CE.

The greater portion of the logic, labeled "Registers and Control Circuits" in Figure 2-10, adapts the storage section to the requirements of the two user types. This portion of the SSU also contains the configuration control register (CCR) for the SE and the maintenance panel controls. Separate maintenance panels are provided for the SSU and the storage section.

Storage Section

- 4 BSMs – 131,072 bytes each.
- 2 BSMs for even doublewords.
- 2 BSMs for odd doublewords.
- Requests interleaved between even and odd BSMs.
- Storage protection provided in 2048-byte blocks.

The storage section of the SE may logically be divided into three functional areas:
1. Basic storage modules (BSMs).
2. Storage common controls.
3. Storage protection circuits.

Basic Storage Modules. Four BSMs, each with a capacity of 131,072 bytes, are contained in the storage section. The BSMs are coincident-current magnetic core storage devices. Each BSM is a completely operational storage module and contains, in addition to the storage arrays, the associated addressing and selection logic, clock, and registers.

Two BSMs provide storage for even-numbered doublewords and two provide storage for odd-numbered doublewords, making possible the interleaving of consecutive even and odd storage cycles to obtain a shorter effective access time. This interleaving consists of starting a cycle for one-half of storage as soon as the fetch portion of the cycle for the other half of storage has been completed.

Storage Common Controls. The storage common controls consist of separate clocks, gating circuitry, and address registers for the even and odd BSMs.

Storage Protection Circuits. This third functional area of the storage section contains the storage protect core array together with the associated clock, registers, and gating logic. This core array provides for storage of a five-bit storage key for each block of 2048 bytes of main storage in the SE.

IBM 7265-02 SYSTEM CONSOLE (SC)

- One System Console.
- System Console is addressable.
- All critical console functions are duplicated elsewhere in the system.

The IBM 7265-02 System Console, (Figure 2-11) is the central monitoring and control position in the 9020D system. The console is divided functionally into four parts: maintenance controls, monitor displays, operator's controls and emergency power-off.

The console is addressable as an I/O device to display the system mode of operation to generate audible alarms, and to display updated system element configurations. The SC contains logic to electronically switch a printer keyboard, a card read/punch, and a printer to the selected multiplexer channel. Switching is under manual control of switches located on the operator's panel. Operator controls which could disrupt the system program or elements are interlocked on the control panel.

All critical console functions are duplicated elsewhere in the system so that there is no requirement for a backup element for the SC. However, manually switchable duplexed power supplies provide backup for most power malfunctions. Only prime power and power control components are not duplexed.

The SC has a control unit which recognizes an address of 01. This address allows the EXC control program to communicate with the SC, to interrogate, or to supply various indications. Interface connections between the SC and other system elements are shown in Figure 2-12.

Several important functional operations associated with the active system may be controlled by six sense switches on the console. The switch settings can be read by the

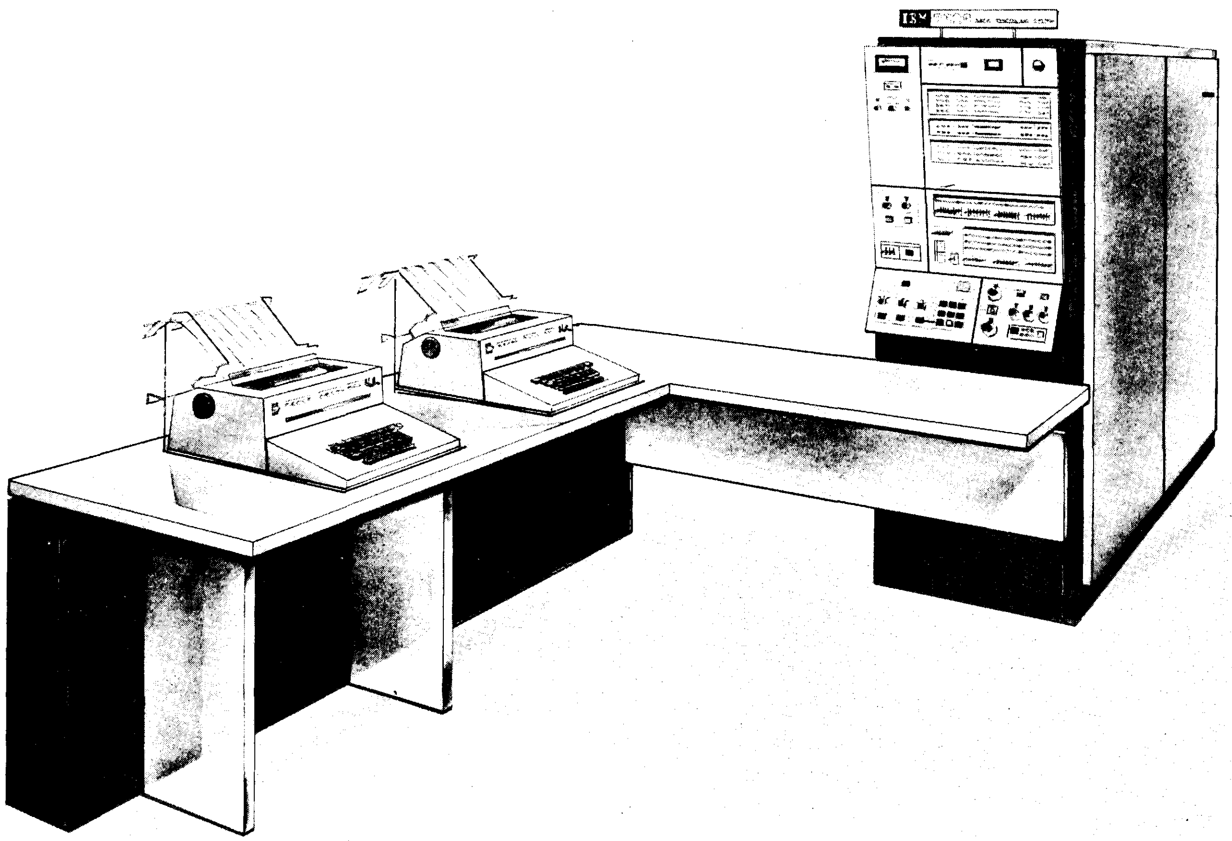


Figure 2-11. IBM 7265-02 System Console (SC)

control program through one of the three IOCEs. Interpretation of the various sense switch settings is defined by the EXC control program.

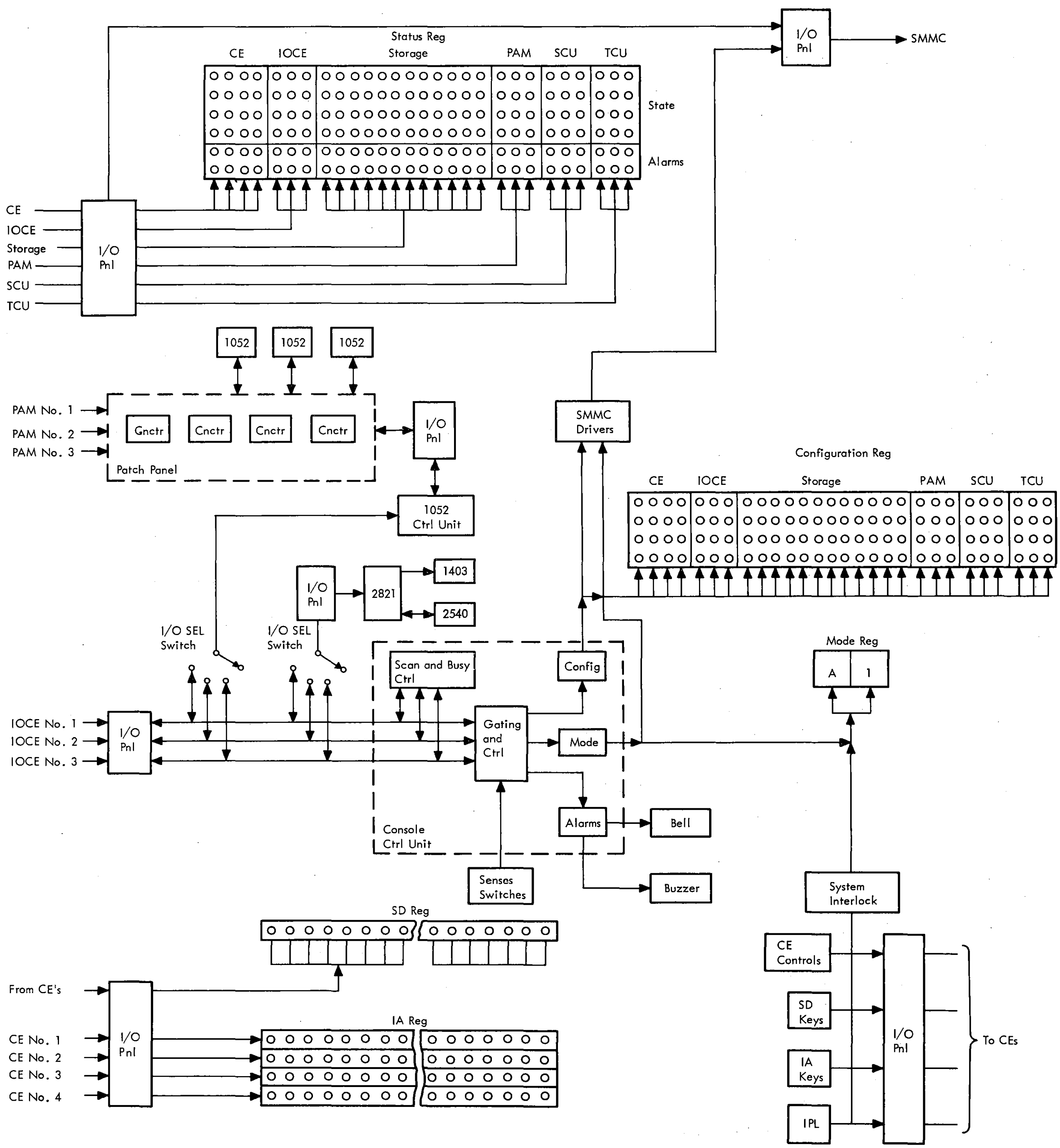
Console indicators continually indicate important states and conditions of the overall system. Some indications represent direct "hardware" connections between the remote element and the system console, while other indications are under program control.

The EXC control program can address the SC as an I/O device to display the system mode of operation, display updated system element configurations, and generate audible alarms.

The present state of each element in the system is also continually displayed on the System Console. Although these element states are dependent on reconfiguration (SCON instruction), their indication is a direct hardware connection.

By means of these and other indications on the system console, the operator always has a current picture of each element's state, status, and logical position in the overall system or subsystem. An interface to the System Maintenance Monitor Console (SMMC) relays the console indicators so that personnel at the SMMC can also monitor system status.

The red "emergency pull" switch located in the upper right corner of the system console will, when pulled, remove power from all IBM 9020 system elements within 2 seconds.



● Figure 2-12. System Console Data Flow and Interfacing

Input/Output

- Two 1052 Printer Keyboards.
- One 2540 Card Read/Punch.
- One 1403 Printer.
- Independently program-addressable.

Two rotary selection switches and two enable pushbuttons are located on the console for the read/punch and printer and for the printer keyboard. These two switches (Figure 2-12) enable the operator to interconnect the selected I/O device to any one of three IOCEs. The switching is accomplished by system console logic with each device independently program-addressable as follows:

I/O Device	Unit Address
1052 Printer Keyboard	02
2540 Card Reader	03
2540 Card Punch	04
1403 Printer	05

The "patch panel" serves to physically reassign the 1052's between the System Console and the PAMs.

IBM 1052-7 Printer Keyboard

- Two 1052 Printer Keyboards.
- Expandable to three 1052's.

Two 1052 Printer Keyboards are located at the System Console for data entry. One 1052 enters data through a control unit in the System Console. The second 1052 enters data through an adapter in a PAM. Additional 1052's for the other PAMs may be added. For maximum flexibility, the 1052 connected through the system console control unit can be manually switched to any of the three IOCEs.

Maintenance and Test Panel

- Allows testing of console control unit, IBM 2821 Control Unit, and 1052 Printer Keyboard control unit.

This maintenance and test panel is used by maintenance personnel to manually test the console control unit, read/punch and printer control unit, and printer keyboard control unit. The panel is located internally on the B-logic gate.

IBM 7289-02 PERIPHERAL ADAPTER MODULE (PAM)

- Maximum of three PAMs within system.
- Attaches remote and local peripheral devices.
- Each device attaches to two PAMs.
- Multiplexed operation.
- Maximum of 240 adapters.
- Eight types of adapter interfaces.

The IBM 7289-02 Peripheral Adapter Module (Figure 2-13) is used for attaching both remote and local peripheral I/O devices to the 9020 system. Interfacings (Figure 2-14) connect each PAM to a maximum of two IOCEs, all existing CEs, and to as many as 159 I/O devices.

Each device is attached to the PAM by an appropriate adapter. Each PAM has a design maximum of 160 adapters, one of which is the test-monitor adapter provided to test the PAM and monitor the common equipment. Each of the other eight types of adapters is designed to interface with a specific type of I/O device. All necessary bit or byte conversions, data control, and matching of signal levels for the device are accomplished in each adapter.

Maximum system reliability is achieved by attaching each I/O device to two PAMs. Each PAM, in turn, is attached (by appropriate controlled interfacing) to two IOCEs (Figures 2-15 and 2-16). In this manner, the failure of any one of the IOCEs or PAMs does not impair system operation.

PAM Addressing

- 240 unique adapter addresses within system.
- 160 adapter addresses per PAM.
- Primary and secondary interfaces in each PAM.
- Half-secondary and full-secondary interface selection under program control.

PAM common, a portion of the unit which contains the control circuits common to all adapters, has provision for 160 unit addresses. These addresses are obtained from any two of the following address groups:

Group A – 16–95
Group B – 96–175
Group C – 176–255

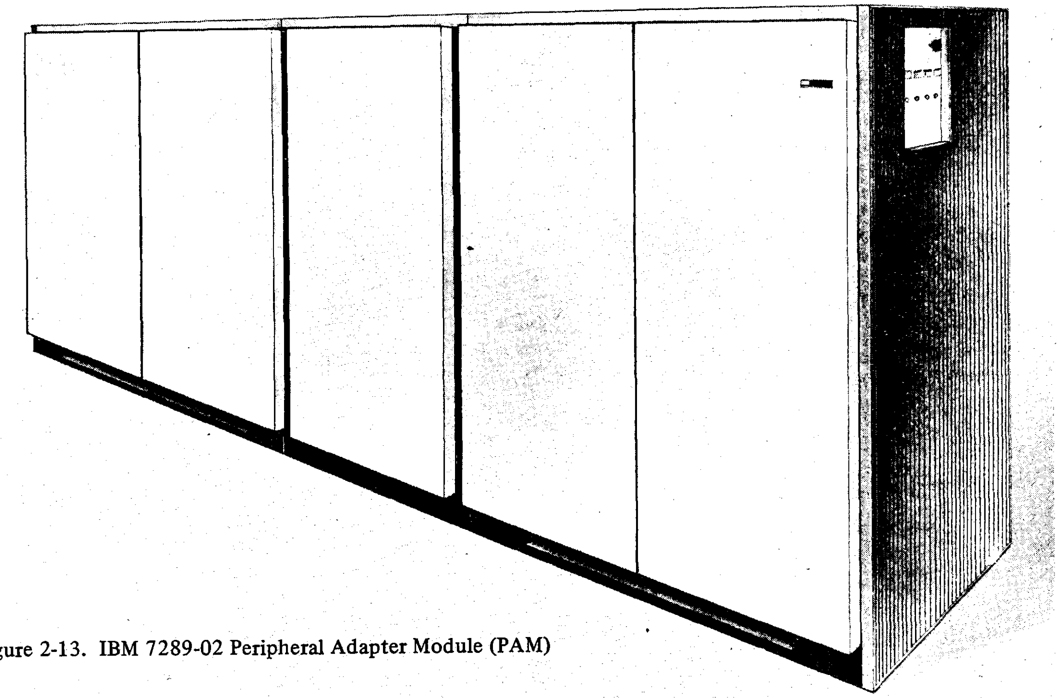


Figure 2-13. IBM 7289-02 Peripheral Adapter Module (PAM)

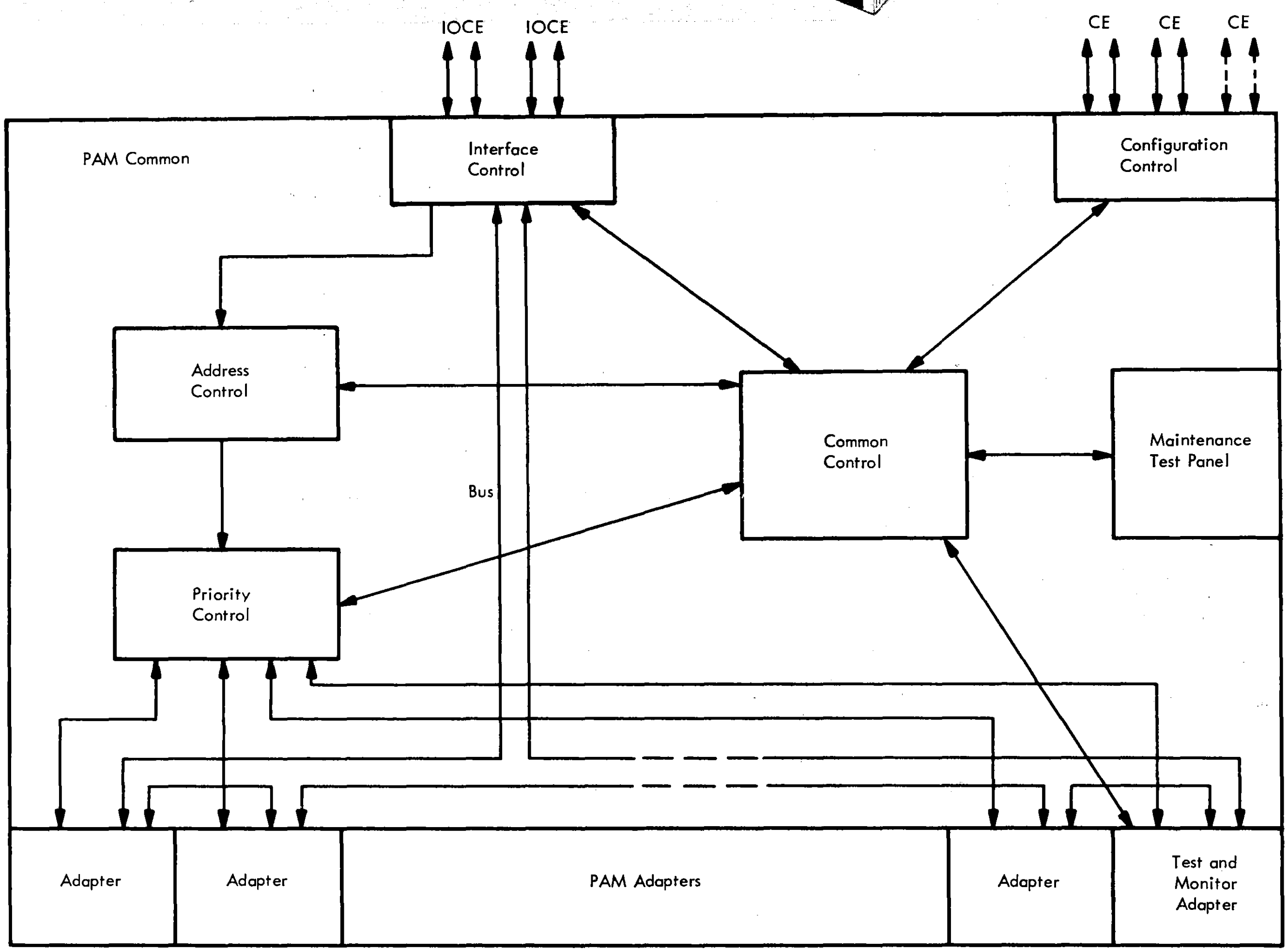


Figure 2-14. PAM Block Diagram

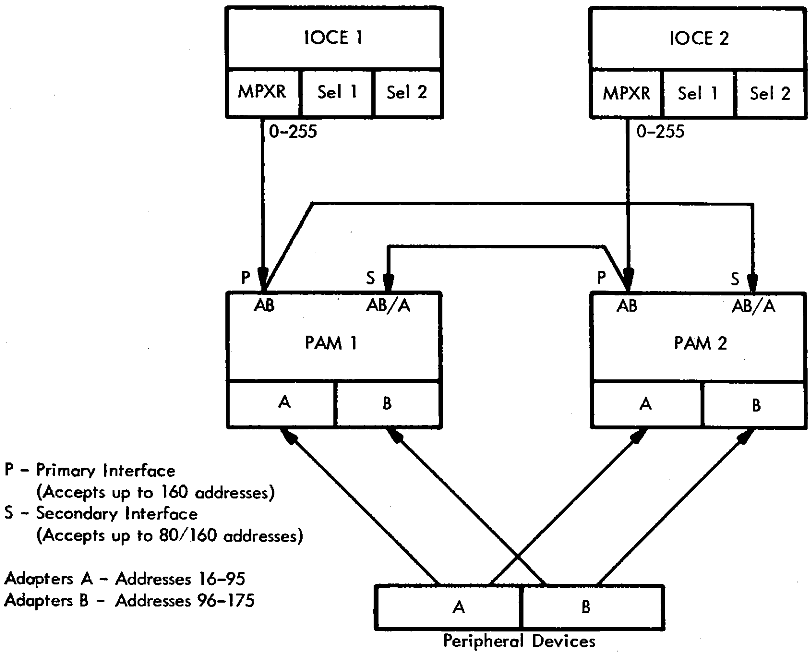


Figure 2-15. Addressing Capability for a 2-PAM System

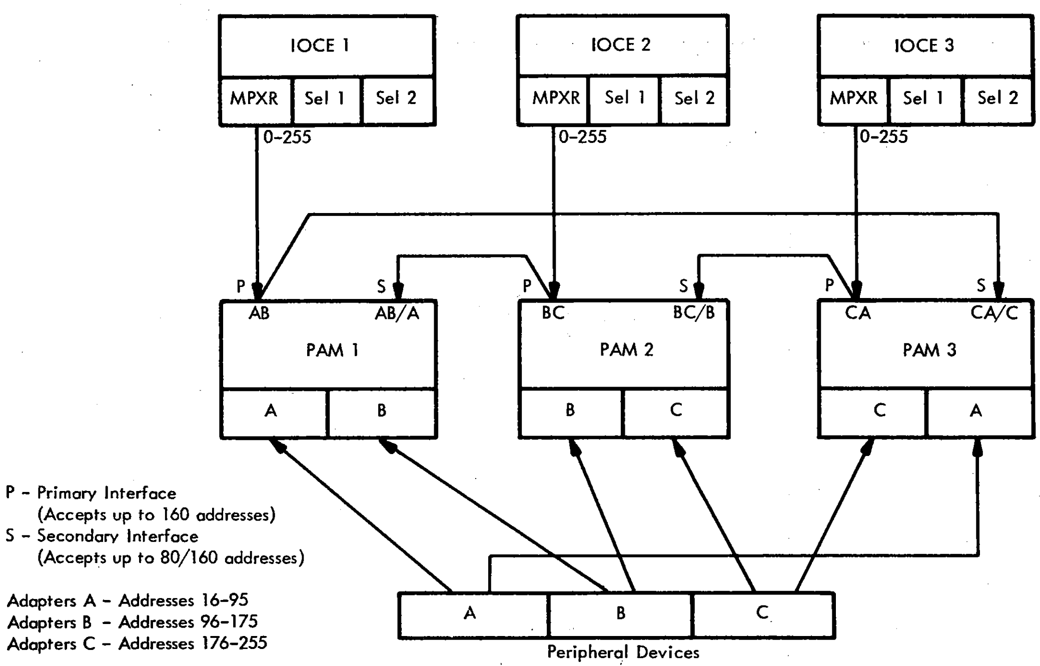


Figure 2-16. Addressing Capability for a 3-PAM System

Selection of these groups (Figures 2-15 and 2-16) is under control of address selection jumper cards which can be changed by maintenance personnel. Assignment of these addresses, as well as priority and configuration, must be consistent between PAMs. Selection options are as follows:

PAM 1 – 16–95 and 96–175
PAM 2 – 96–175 and 176–255
PAM 3 – 176–255 and 16–95

The actual number of addresses accepted by the PAM common circuits is equal to the number of adapters in the PAM. Individual adapter addresses are established by address selection jumper assignments.

Each PAM contains both a primary and secondary IOCE-PAM interface (Figures 2-15 and 2-16). The primary interface is always assigned to two groups of 80 addresses (Figure 2-17). Only one interface can be assigned at a time. Execution of a half-secondary command to the PAM causes the secondary interface to remain selected until a full-secondary command is executed. Use of the secondary interface enables an IOCE to address any I/O device attached to the PAMs.

PAM Designation	Primary	Half Secondary (80 addresses)	Full Secondary (160 addresses)
1	16-175	16-95	16-175
2	96-255	96-175	96-255
3	16-95 176-255	176-255	16-95 176-255

Figure 2-17. PAM Address Assignments

PAM Priority Controls

- Priority can be field-changed.
- Lowest address has highest priority within PAM.

The I/O adapter priority is assigned to the primary and secondary groups within each PAM as shown in Figure 2-18. Note that adapter priority is address-dependent, with the lowest address code to each group (16–95), (96–175), and 176–255) having highest priority. Priority decreases until the highest address code within each group has the lowest priority.

Priority	PAM 1 Addresses (16-95, 96-175)	PAM 2 Addresses (96-175, 176-255)	PAM 3 Addresses (176-255, 16-95)
1	16	96	176
2	96	176	16
3	17	97	177
4	97	177	17
.	..	...	...
.	..	...	...
.	..	...	...
159	95	175	255
160	175	255	95

Figure 2-18. PAM Priority Assignments

The first priority addresses (16, 96, and 176) are assigned to the Test and Monitor Adapter in PAM 1, PAM 2, and PAM 3, respectively. Priority of an adapter and the peripheral device can be changed by maintenance personnel through a different address assignment.

Up to eight control units such as PAM can be attached to the IOCE multiplexer channel, with priority determined by the order of cabling to each control unit. The PAMs should be cabled to have the highest priority of all control units attached. With respect to the IOCE multiplexer channel, the PAM with the primary interface should also have higher priority than the PAM with the secondary interface.

PAM Adapters

- Each adapter services one device.
- Nine I/O adapter types.

Adapters provide the electrical interface suitable for the device or class of devices to be attached to the 9020 system. One adapter in each of two PAMs may be attached to each peripheral device. Each device can interface to a single device. A typical adapter is shown in Figure 2-19. There are nine I/O adapter types:

General Purpose Input Adapter: Receives data bytes in parallel of up to eight bits plus parity and operates on a demand/response basis from a device with matching electrical interface.

General Purpose Output Adapter: Transmits data bytes of up to eight bits plus parity in parallel and operates on a demand/response basis to a device with a matching electrical interface.

Interfacility Input Adapter: Receives data bytes of eight bits plus parity, serially, and operates at 1200 or 2400 bits per second from a standard Lenkurt 26B Modem.

Interfacility Output Adapter: Transmits data bytes of eight bits plus parity, serially, and operates at 1200 or 2400 bits per second into a standard Lenkurt 26B Modem

Teletypewriter, Half Duplex, Long Lines Adapter: Transmits and receives data byte of 7.42 Baudot start/stop code serially at 100 words per minute.

Radar Video Data Processor (RVDP) Adapter: Receives data bytes of six bits plus parity in parallel and operates at 2400 or 7200 bits per second from a Burroughs RVDP.

1052 Adapter: Transmits data bytes of six bits plus parity in parallel and operates at 14.8 characters per second to a 1052 printer. The adapter receives data bytes of six bits plus parity in parallel and operates up to 14.8 characters per second from a 1052 keyboard.

Common Digitizer (CD) Adapter: Receives data serially from one of three channels of the common digitizer data-receiving group. The data messages are received at 2400 bits per second and consist of two or more 12-bit fields. Each field of 12 data bits and 4 tag bits is assembled into two 8-bit bytes and transferred to the multiplexer channel in burst mode.

Flight Data Entry and Printout (FDEP) Adapter: Matches the interface requirements of a modified IBM 1051 Data Communications Control Unit (DCCU). The DCCU operates at 8.33 characters per second in half-duplex mode (75 baud) over telegraph facilities or other common carrier schedule 3 channels.

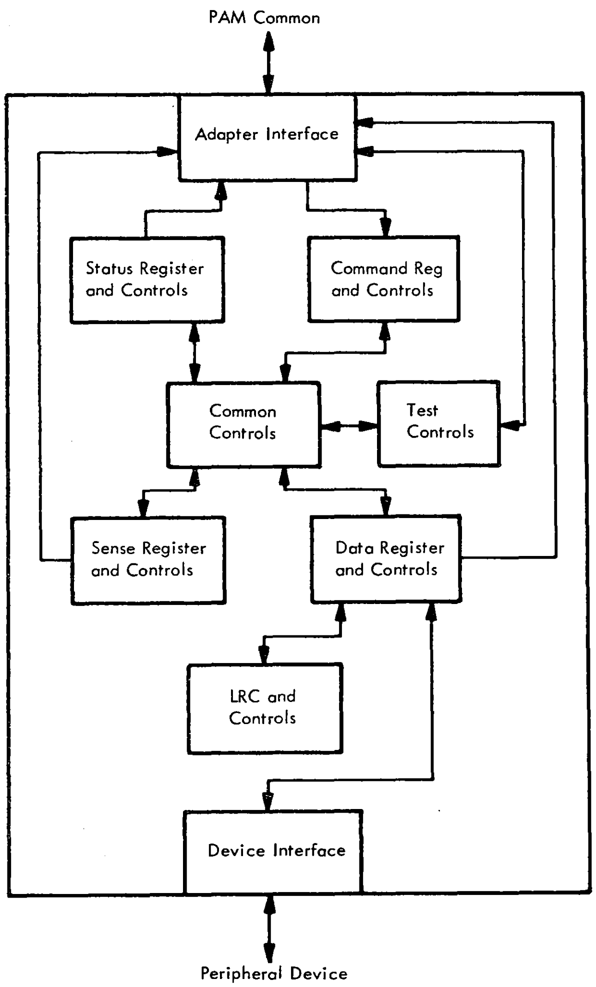


Figure 2-19. Typical PAM Adapter

Internal Organization

The PAM consists of three frames: a PAM frame, a cable entry frame, and an adapter frame. The physical layout of the PAM (Figure 2-20) closely parallels its logical organization (Figure 2-14). All of PAM Common is located on one gate in the PAM frame. The PAM frame also contains the power supplies, maintenance panel, and relays.

The remaining gate in the PAM frame and all the gates in the adapter frame are devoted to adapters. The number of adapters which can be packaged on a particular gate depends on the combination of adapter types.

The cable entry frame provides entry space for cables connecting the PAM with both the other system elements and the I/O peripheral devices.

IBM 2803-01 TAPE CONTROL UNIT (TCU)

- Interfaces with two IOCEs.
- Maximum of eight tape units per TCU.
- Under configuration control.

The IBM 2803-01 Tape Control Unit (TCU) is the I/O control unit for up to eight IBM 2401-02 or IBM 2401-03 Magnetic Tape Units (TCs). The TCU is shown in Figure 2-21. The function of the TCU is to adapt the TU's to the standard I/O interface. The TCU adapts the TUs to the channel in the following three ways:

1. Converts interface line sequences and commands into timed pulses for TU control.
2. Converts times pulses from TUs into interface line sequences.
3. Regulates data transmission between the channel interface and the TUs.

Each TCU has an interface switch feature that permits it to be attached to two selector channels, one on each of two IOCEs. The interface switch provides for two interfaces, a primary and a secondary, which may be enabled by program means. Figure 2-22 shows the typical connection of TCUs on a system with three IOCEs.

Each TCU contains a configuration control register (CCR) and can be configured by any CE in the system via interfaces between the TCU and each CE. Both the interface switch and the configuration interfaces are shown in Figure 2-23.

The TCU has no battery backup and no duplex power source. However, single system may have up to three TCUs providing redundant elements in case of a malfunction. A maintenance panel is provided for off-line testing of the TCU itself and also of the attached TUs.

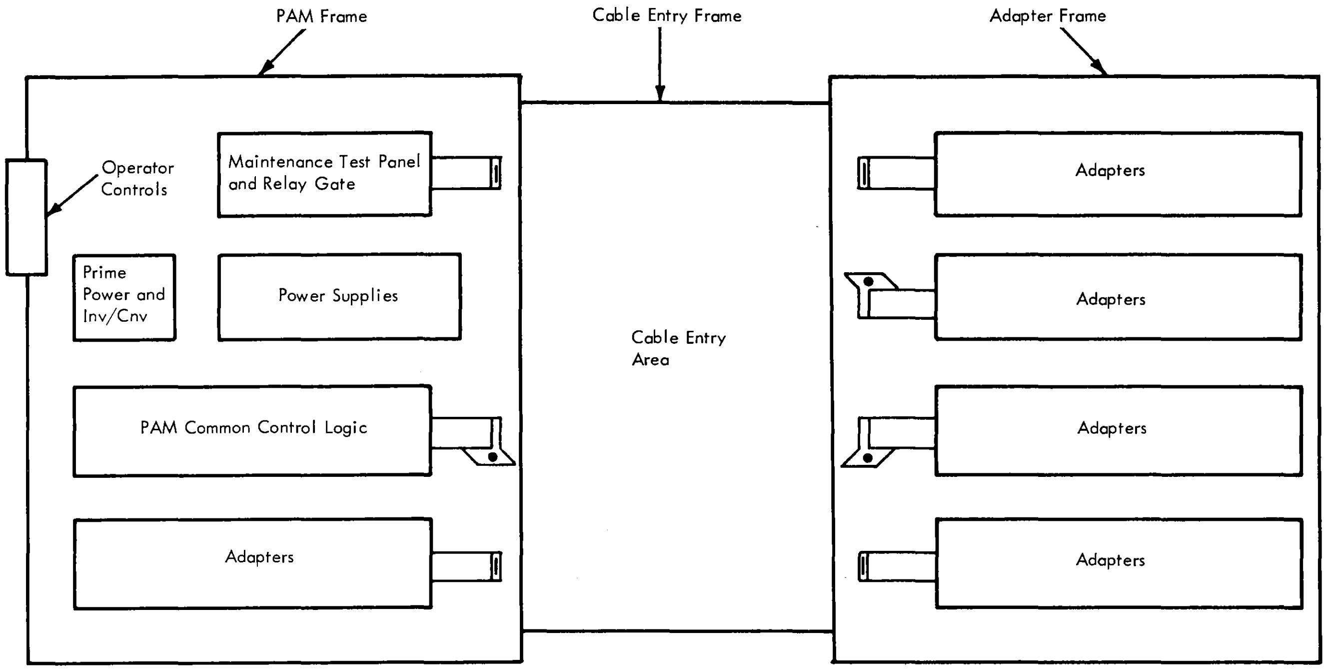


Figure 2-20. PAM Physical Layout

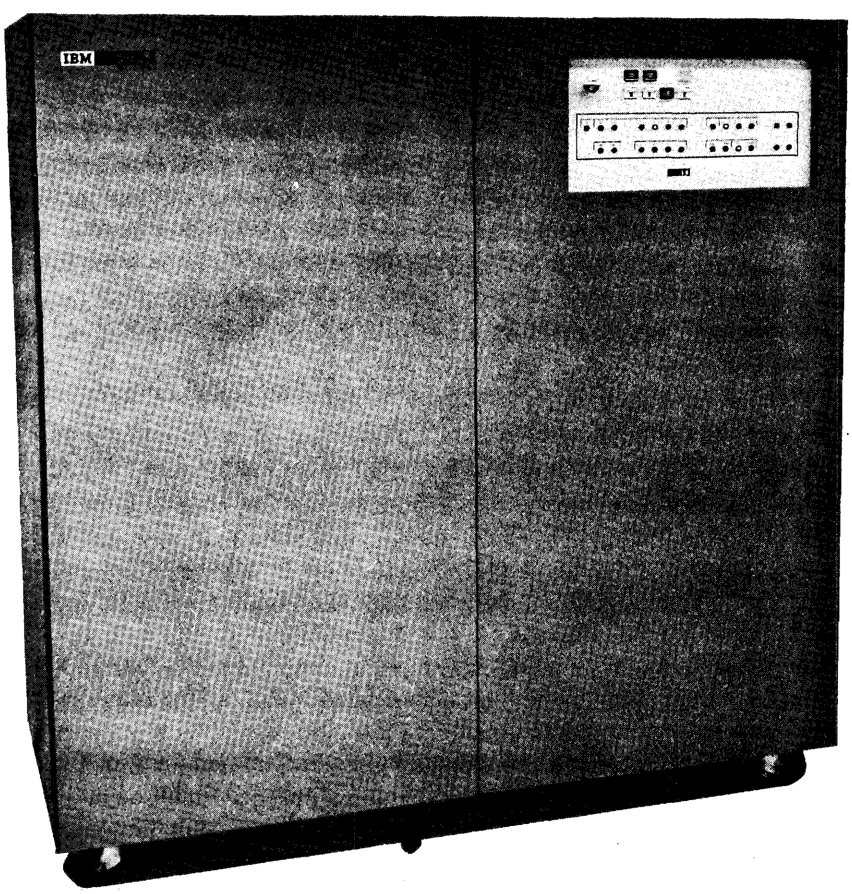
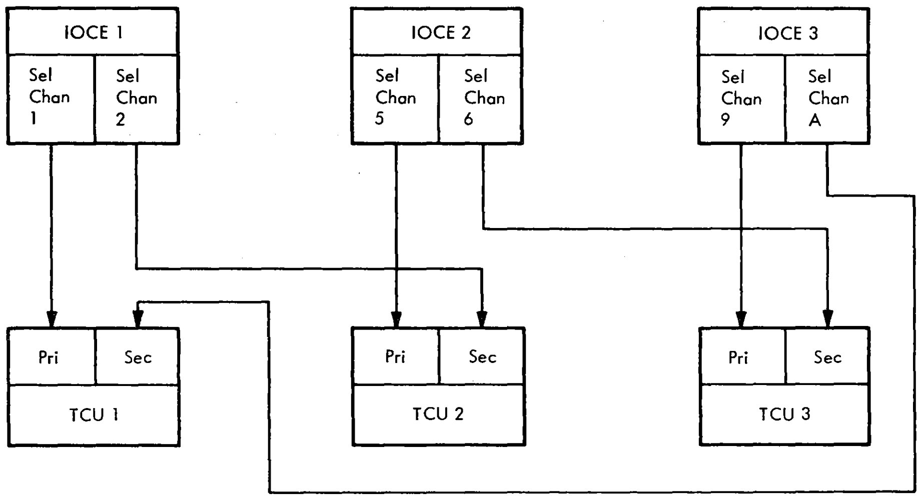


Figure 2-21. IBM 2803-01 Tape Control Unit (TCU)



●Figure 2-22. Typical TCU-IOCE Connection

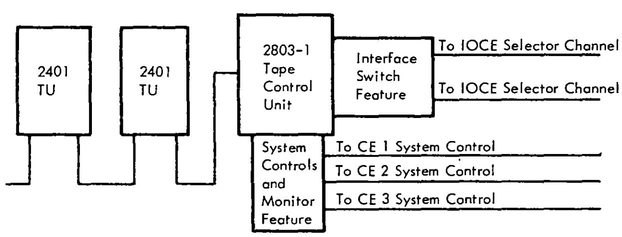


Figure 2-23. TCU-I/O Device Connection

IBM 2314-A1 STORAGE CONTROL UNIT (SCU)

- Controls IBM 2312-A1 and/or IBM 2318-A1 Disk Storage Units (DSUs).
- IBM 2312-A1 DSU contains one disk drive; IBM 2318-A1 DSU contains two disk drives.
- DSUs use IBM 2316-01 Disk Packs for storage of data.
- SCU interfaces with two IOCEs.
- SCU is under configuration control.

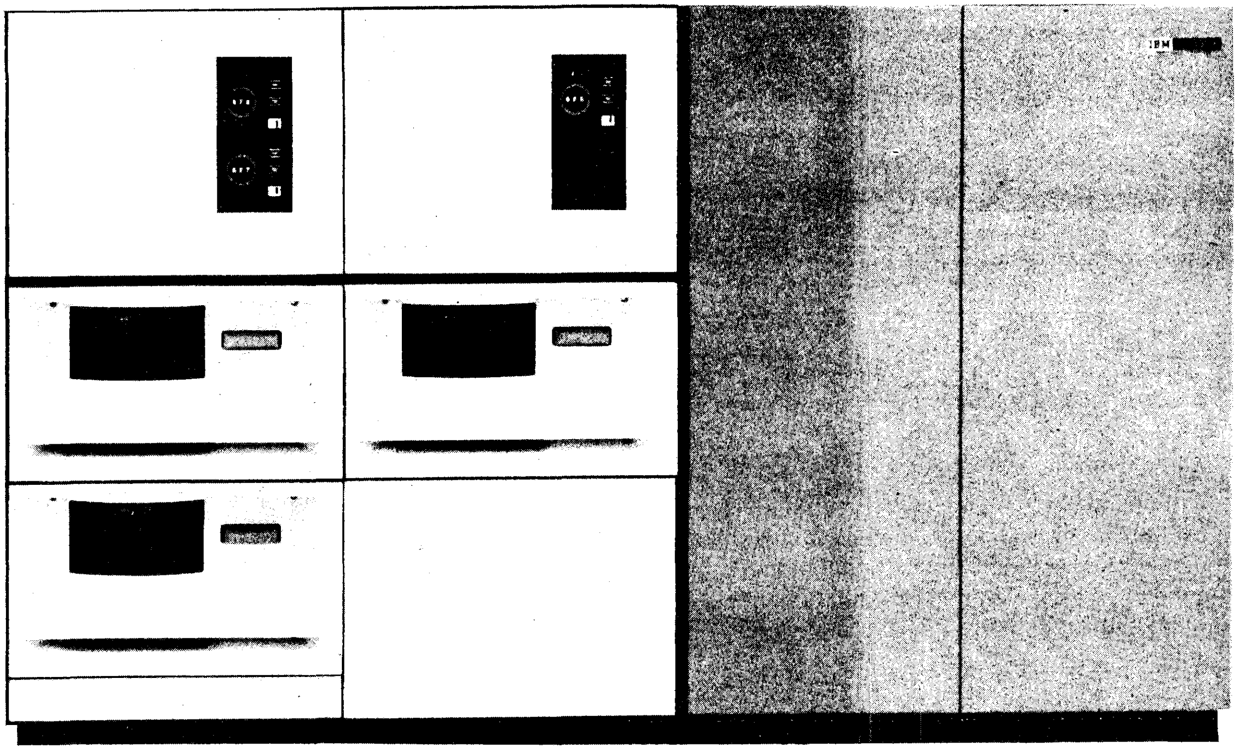
The IBM 2314-A1 Storage Control Unit (SCU) controls IBM 2312-A1 and/or IBM 2318-A1 Disk Storage Units (DSUs). The 2312-A1 DSU contains a single drive for an IBM 2316-01 Disk Pack; the 2318-A1 DSU is a double module containing two drives. Up to nine drives may be attached to an SCU, but only eight may be on-line at any one time. Since a maximum of five DSUs may be attached to one SCU, the maximum number of drives is obtained by attaching four 2318-A1 DSUs and one 2312-A1 DSU. Figure 2-24 shows an SCU with one 2312-A1 DSU and one 2318-A1 DSU attached, thus providing three drives.

The 2316-01 Disk Pack is a removable, interchangeable unit with a storage capacity of 29,176,000 bytes of data. Average access time is 60 ms, with a minimum of 25 and a maximum of 130 ms.

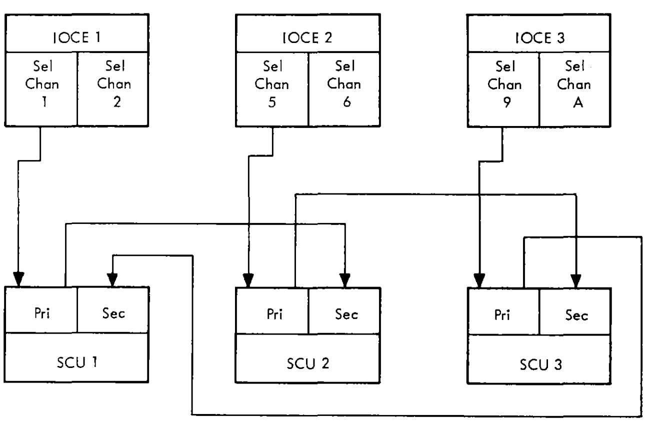
Each SCU has a two-channel switch feature that permits it to be attached to two selector channels, one in each of two IOCEs. The two-channel switch feature provides two interfaces which may be enabled by program means. Figure 2-25 shows typical connection of SCUs on a system having three IOCEs. Figure 2-26 shows typical connection of both SCUs and TCUs to such a system.

Each SCU contains a configuration control register (CCR) and can be configured by any CE in the system via interfaces between the SCU and each CE.

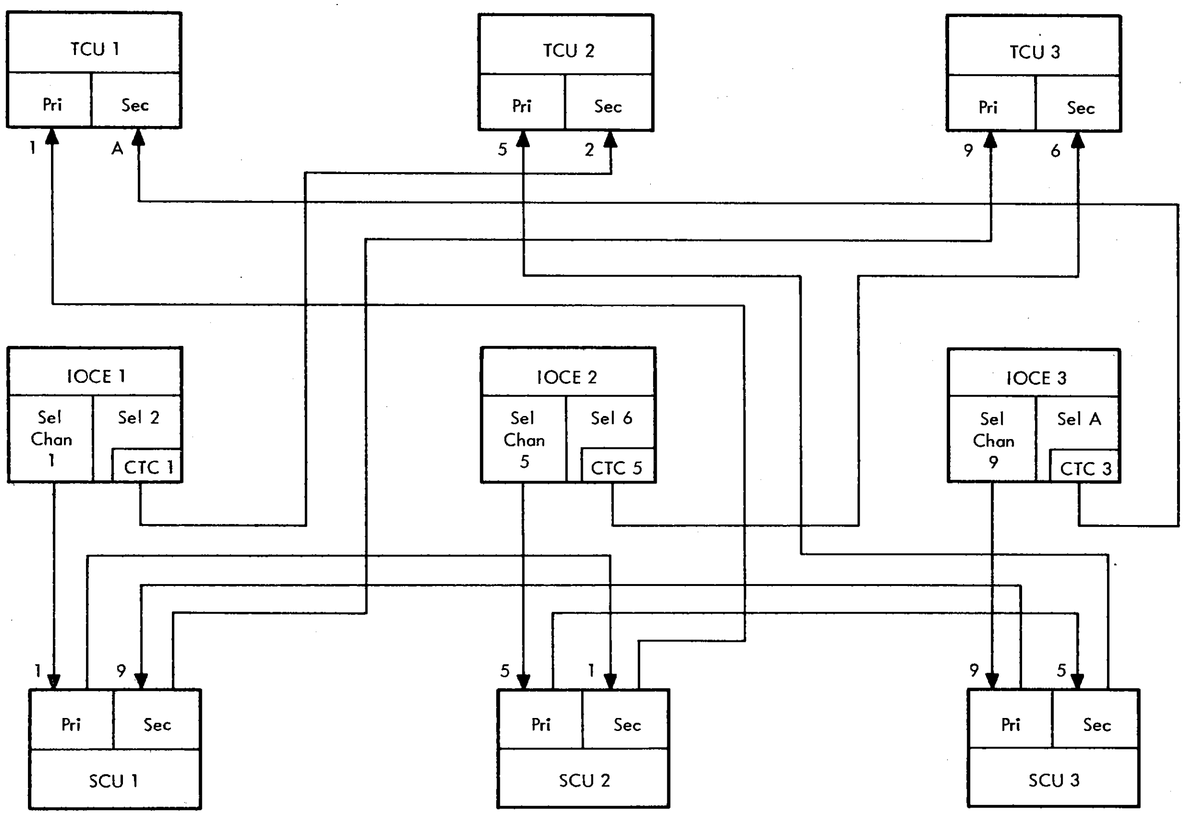
The SCU has no battery backup and no duplex power source. However, single systems may have up to three SCUs providing redundant elements in case of a malfunction. A maintenance panel is provided for off-line testing of the SCU and any attached DSUs. The SCU is a ROS-controlled machine, and a number of microprogram routines are available via the maintenance panel for such off-line testing.



● Figure 2-24. Direct Access Storage Facility (DASF)



● Figure 2-25. Typical SCU-IOCE Connection.



● Figure 2-26. Typical TCU/SCU-IOCE Connection.

- Simplex.
- Distributed simplex.
- Multiple driver simplex.
- Multiplex.

Interfacing provides the means of communication between the various elements in the 9020 system. The data or signals carried on the various interfaces represent a variety of information: data words, configuration assignments, logout data, selection lines, error conditions, condition codes, system masks, resets, and other miscellaneous signals necessary for the successful operation and synchronization of the overall system. Some interface signals are pulses while others are represented by steady-state voltage levels.

Interfacing between elements within the 9020 system is accomplished almost exclusively by 20 conductor coax cables. Some are terminated with interface connectors which accommodate two 20-conductor cables (double body connector) for a total of 40 signals. In some cases an interface connector accommodates only one 20-conductor cable (single body connector) for a total of 20 signals. One connector is mounted in the system element and receives the cable by means of serpent connectors and connects it to 20-conductor flat cables in the element by means of pins.

The interelement interfaces are of two basic types: simplex and multiplex. The simplex interfaces are essentially one-way signals; the multiplex interfaces can carry signals in either direction, depending on the particular driver-receiver combination being used at the time. These combinations are described below:

Simplex, Figure 3-1 (a): These signals originate in one element and terminate in another element. The signal lines are in effect, a direct one-way element-to-element connection.

Distributed Simplex, Figure 3-1 (b): These interface signals originate in one element and are received by a number of receiving elements. The data or control signals are distributed to multiple elements but, in a majority of cases, only one of the receiving elements is

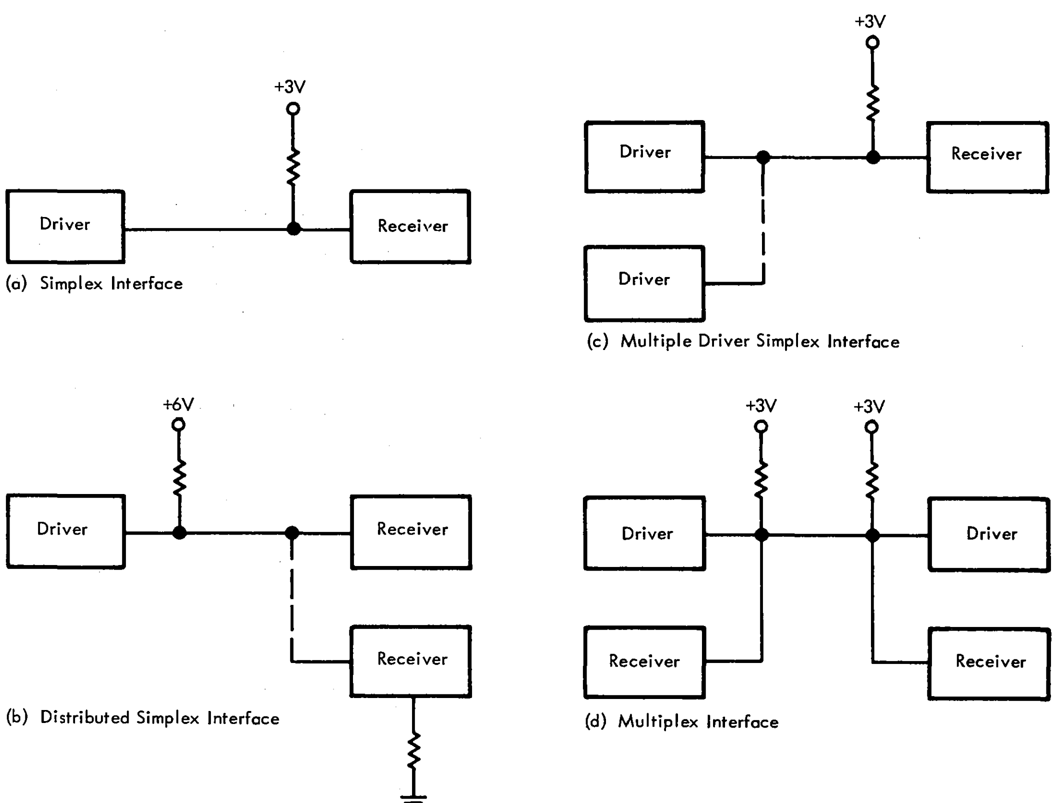


Figure 3-1. Interface Receiver-Driver Combinations

conditioned to accept the information at a particular time. Figure 3-2 shows an example of this distributed simplex usage. A distributed simplex interface with only one receiving element is logically the same as a pure simplex interface.

Multiple Driver Simplex, Figure 3-1 (c): In this case, one receiving element is supplied by drivers in more than one element. Normally, only one driver is active at any given period of time. This type of interface is used between the CEs and the SC. Figure 3-3 shows an example of this type of interface.

Multiplex, Figure 3-1 (d): The multiplex type interface can pass data or signals in either direction.

Interfacing between the IOCE and the I/O equipment is accomplished with the IBM 9020 system I/O interface. The logic levels and timing sequences of the 9020 system I/O interface are identical to those in the standard System/360 I/O interfacing. Interfacing between the CE, SE, IOCE, PAM, SCU, TCU, and System Console (SC) is described in the following pages. These descriptions are meant to include only the logic interfacing and not the power supply interfacing. For additional details, refer to the instruction and maintenance manuals for the corresponding elements.

Figure 3-16, which shows an overall view of interfacing between the various system elements, has been placed at the end of this chapter so that it can be folded out for reference while the chapter is read.

COMPUTING ELEMENT INTERFACING

- Interfacing to and from CEs, SEs, IOCEs, PAMs, SCUs, TCUs, and SC.
- System Control.
- Monitoring.

The CE executes the EXC program and is, therefore, the controlling element in the overall system. Because of this overall system control, the CE is in direct communication with each major system element. The communication takes many forms including data, controls, and indications.

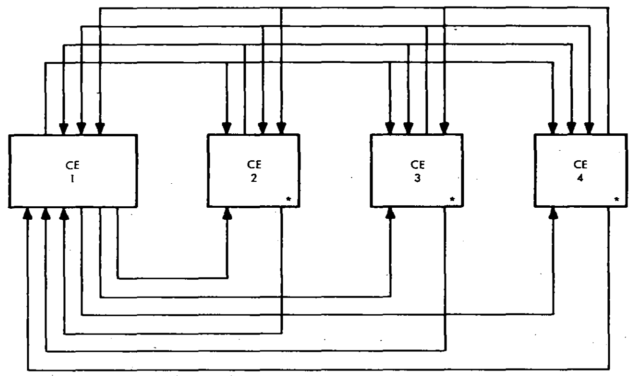
Each signal line or bus which either enters or leaves the CE is described in the following pages.

CE-CE Interfacing

- WRD and RDD direct control.
- Data communication.
- External starts and logouts.
- Error monitoring.

The CE is the only element that directly communicates with other elements of its kind. Figure 3-4 shows the CE-to-CE interface lines.

One set of the distributed simplex lines originates in a given CE, and three identical sets are received from the other CEs. Further, three sets of the simplex lines originate in a given CE and three identical sets are received. This CE-to-CE communication is illustrated below:



*For simplification, not all simplex lines are shown for these CEs. CE 1 is shown complete.

The interface intercommunication is concerned primarily with direct control operations which include data communication (one byte) and external CE starts and logouts. In addition to the direct control function, there are controls for reconfiguration and element check monitoring.

Control Bus: This 36-bit bus is used for both configuration control and ATR assignment. Configuration control (established by the configuration mask) is used to define which elements comprise a subsystem, and to avoid interference between subsystems. The configuration control registers in the various elements contain positions to define the other elements with which any given element may communicate at any given time. The CCR positions, or bits, enable or inhibit data and control paths between elements. Refer to Chapter 4 for further discussion of configuration control.

ATR assignment establishes a correlation between logical addresses referred to by the program and actual storage elements within the system.

System Reset (1, 2): This double-railed signal (2 lines) performs hardware resets. To cause the reset, line 1 must go negative and line 2 must go positive simultaneously. They are normally in the reverse condition. The reset is not gated by the CCR. All bits in the CCR are reset to 0's except the SCON bits which are set to 1's.

Element Check (ELC): The 'element check' signal is sent to all CEs within the system with the exception of itself. This signal may result from a CCR or ATR parity error, from certain PSBAR stepping situations, and from certain hard stops or CE error conditions.

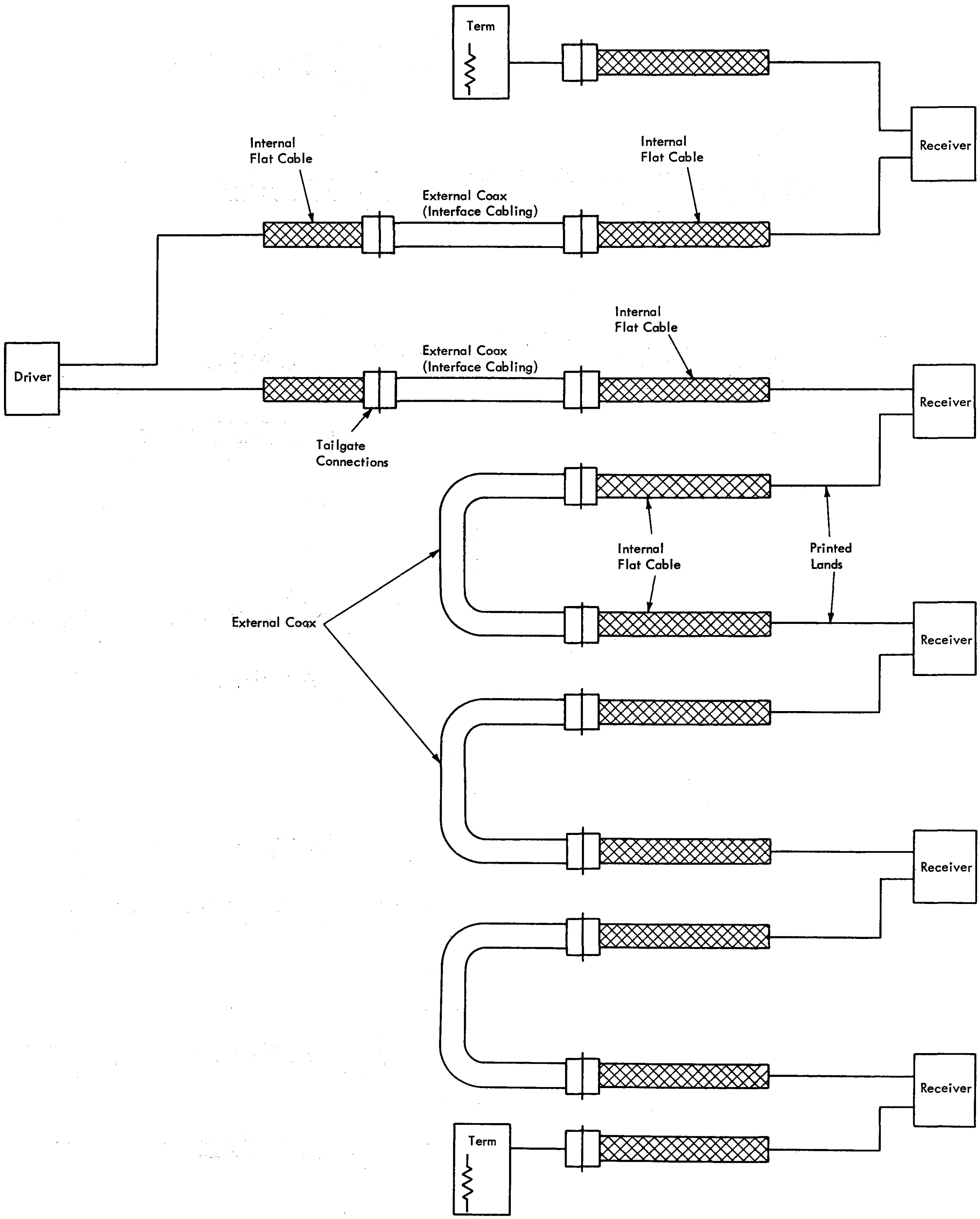


Figure 3-2. Typical Distributed Simplex Interface

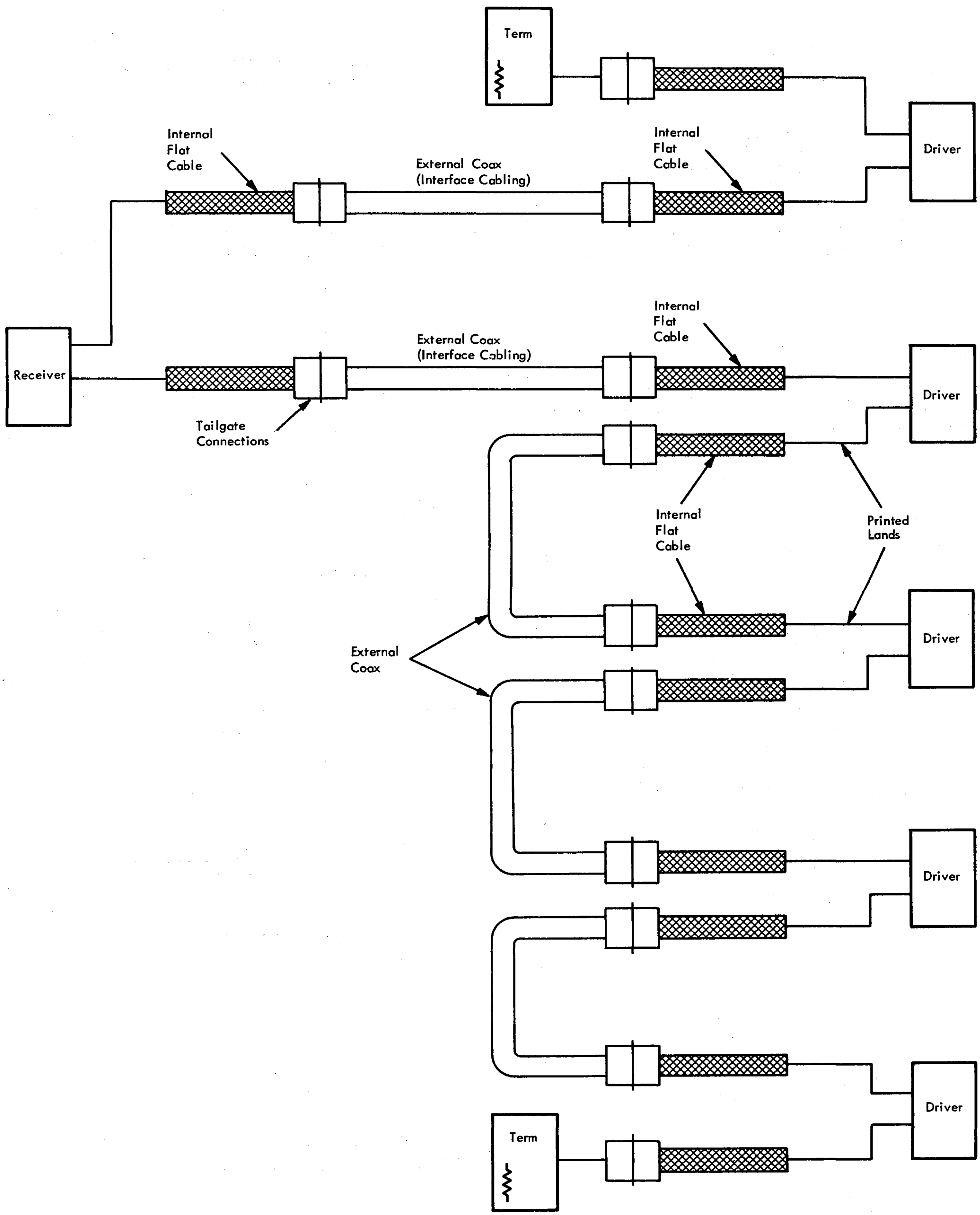
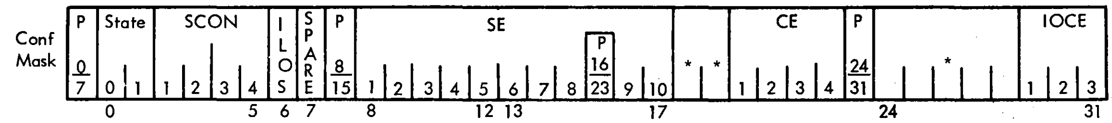


Figure 3-3. Typical Multiple Driver Simplex Interface

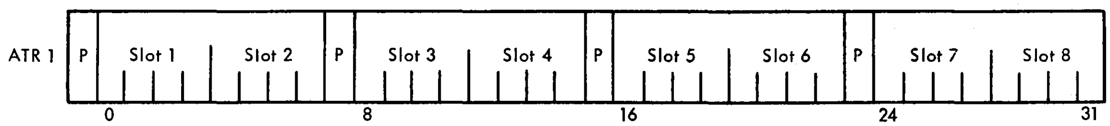
DISTRIBUTED SIMPLEX LINES AND BUSES:

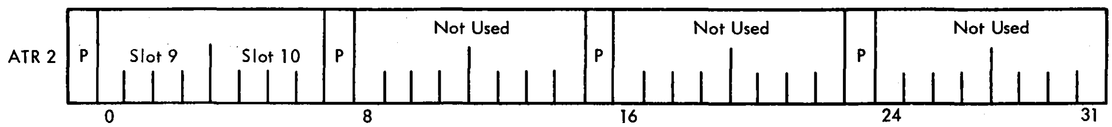
Control Bus:

Data Formats:



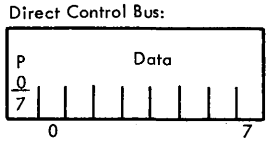
* = not used





Note: The configuration and ATR mask originate from the external register. The configuration mask signals are distributed simplex originating in a CE and received by one or more CE's.
* Not Used

Direct Control Bus:



Note: This data byte is concerned with direct control. The direct data byte and ELC are distributed simplex originating in a CE and received by one or more CE's.

Miscellaneous Control Lines:

System Reset 1
System Reset 2
Element Check

SIMPLEX LINES:

1. Direct Control Signal Lines:
   a. CE Ext. Start Command
   b. CE Ext. Stop Command
   c. CE Logout Command
   d. CE Write Direct Command
   e. CE Read Direct Command
2. Reconfigure Select
3. SCON/SATR Response
4. SATR Select

Note: These simplex signals originate from direct control and configuration control circuitry.

Figure 3-4. CE to CE Interface Lines

Direct Out Lines: During execution of a write direct CE-to-CE data communication, this bus represents eight data bits and one parity bit fetched from an SE. This byte of data remains as static signals until the next write direct instruction is executed.

Signal Out Lines: This set of five lines is used in conjunction with 'direct out lines'. The five commands which follow are sent on these lines:

CE External Start Command: This command is issued by a write direct instruction and causes the receiving CE to start execution after it obtains a new PSW from location 00000 of its PSA. The receiving CE must be properly SCONed to the sending CE to perform the external start operation.

CE External Stop Command: This command is issued by a write direct instruction and causes the receiving CE to perform an element reset and go to the stopped state with the manual light on. The receiving CE must be properly SCONed to the sending CE to execute the external stop operation.

CE Logout Command: This command is issued by a write direct instruction to cause the receiving CE to initiate logout procedures. To perform the logout, the receiving CE must be properly SCONed to the sending CE and must not have machine checks masked off in the current PSW.

CE Write Direct Command: This command is issued by a write direct instruction and indicates a data communication type operation between the sending and receiving CEs. This command causes an external interrupt at the receiving CE by setting a unique bit in its external interrupt register, provided that the receiving CE is properly configured (CCR 20–23) to listen to the originating CE.

CE Read Direct Command: This command is issued by the read direct instruction and indicates that a byte of data has been taken from the direct data bus. The command causes an external interrupt at the addressed CE by setting a unique bit in its external interrupt register. The receiving CE must be properly configured (CCR 20–23) to the originating CE.

Reconfigure Select: This line, carrying a 5.0-usec pulse from the CE to another CE, causes the CE to set into its configuration register the mask on the output bus. The CE will honor the select if the selector's SCON bit is on in the receiving CE's CCR.

SATR Select: This select line signals and conditions the selected CE for receiving the address translation assignment mask on the 36-bit control bus. Three select pulses are required. One for initial selection, and two for transmission of ATR 1 and ATR 2.

SCON/SATR Response: This line is sent to the CEs in response to configuration select, provided that the select was honored and the CCR parity is correct.

This response signal is also used as a SATR response to acknowledge that: (1) the receiving CE was properly SCONed, (2) the ATR 1 and ATR 2 assignment masks were properly received.

CE-SE Interfacing

- Data transfers.
- Control signals.
- Error monitoring.

All main storage is located in SEs that are self-contained units electrically remote from the CE. Because these SEs are self-contained units, a complete set of buses and interlocking control signals must be provided to assure proper synchronization and data transfer.

CE-to-SE Interface

- Addressing.
- Data storing.
- Configuration.
- Control.

The interface from the CE to an SE involves the following distributed simplex buses: storage data bus in (SDBI), storage address bus (SAB), mark bus, inkey bus, three logword number lines, and the two-line system reset. In addition, two groups of control lines are involved; one group is distributed simplex and the other is simplex (Figure 3-5). A description of the individual buses and lines follows.

Storage Data Bus In: This group of 72 lines carries data and configuration information from one CE to up to ten SEs. The accessed SE gates its receivers to accept the signals from the bus. Figure 3-5 shows the formats of the configuration information and storage data on the SDBI. During a SCON operation the CE transmits the SCON mask over the SDBI. Note that only the unshaded portions (Figure 3-5) are used by the SE. The CE communication bits are moved from bits 52–55 to bits 56–59 by the CE. These bits also appear on the bus in their original locations but are not gated in from those positions by the SE. Note that bits 38 and 39 are used only for parity checking at the SE.

Storage Address Bus: The SAB consists of 19 lines labeled 1–19 and a parity bit for bits 1–5. Bits 1–4 specify the particular SE and are called the Box Tag. For this

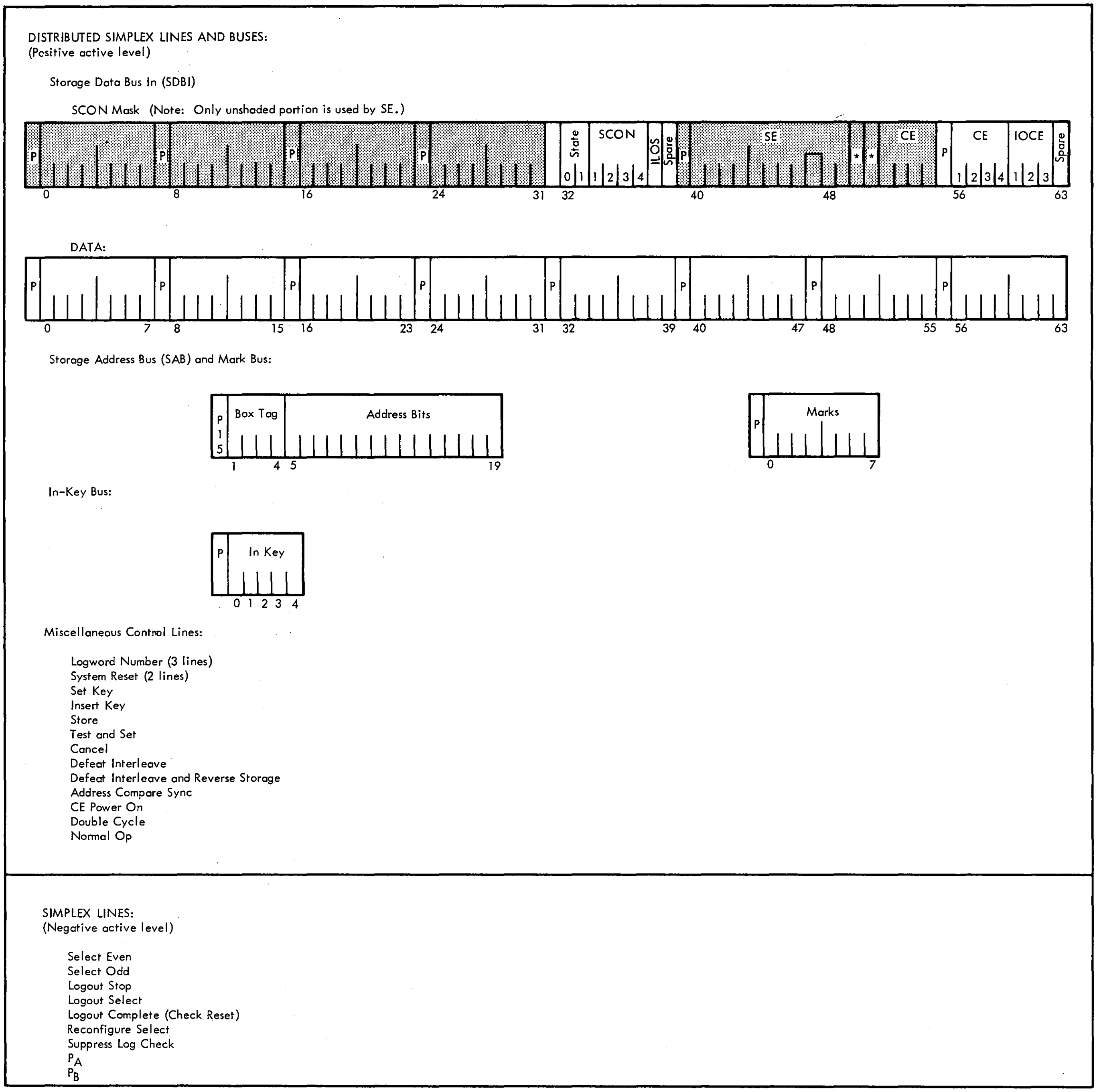


Figure 3-5. CE to SE Interface Lines

reason the P(1–5) bit is sometimes referred to as P_T, for tag parity, even though bit 5 actually specifies high or low storage. Parity for the address lines (bits 6–19) are sent separately on simplex lines labeled P_A and P_B.

Mark Bus: The mark bus consists of eight bits (0–7) plus a parity bit and represents the store or regeneration control lines for each of the eight bytes of the doubleword accessed by the CE.

In-Key Bus: The In-Key bus consists of 5 bits (0–4) plus a parity bit. The high-order four bits are compared to the key bits stored in the storage protection area of the SE. The low-order bit (bit 4) indicates that fetch protection is active.

Logword Number: Three lines carry the logword number from the CE to an SE. The lines gate the logwords on to the SDBO.

System Reset (1, 2): These signals cause a storage reset when a system reset occurs. In addition to resetting the SE itself, the storage reset causes the SE's CCR to be reset to all zeros except for parity and SCON bits which are set to 1's. These reset signals are not gated by the CCR.

Set Key: This signal from the CE causes an SE to perform a set-key cycle; i.e., to set the protection key from the CE into the storage protect array.

Insert Key: This signal causes the SE to place the key from the storage protect array on the outkey bus.

Store: This control line permits the SE to perform a data store.

Test and Set: This signal causes the SE to perform a test-and-set storage cycle in which a doubleword is fetched and regenerated into storage except for the addressed byte which is set to all 1's before being returned to storage.

Cancel: This signal causes the SE to regenerate the data fetched from storage without transferring it to the user element.

Defeat Interleave: This signal indicates to the SE that the DEFEAT INTERLEAVE switch on the CE is active. While the CE reverses SAB bits 6 and 20 to defeat interleaving, the IOCE does not. Therefore, the 'defeat interleave' signal is sent to enable the SE to reverse the roles of IOCE address bits 6 and 20. This is accomplished by: (1) substituting bit 20 for bit 6 when gating the IOCE storage address buffer to SESAR; and (2) sampling bit 6 (bus bit 14) to determine whether the access request is for the odd or even half of storage. See Chapter 5 for a detailed explanation of 'defeat interleaving'.

Defeat Interleave and Storage Reverse: This signal has the same significance as 'defeat interleave' except that IOCE address bit 6 (bus bit 14) is inverted before it is used for selecting odd or even storage.

Address Compare Sync: This signal provides a negative significant sync pulse for scoping when the address switches on the CE control panel match the SAB and when the ADR COMPARE switch is in the normal position.

CE Power On: The 'CE power on' signal is raised during CE power-on reset and falls to ground level prior to power going off. It inhibits the output of the associated communication bits in the CCR of the SE.

Double Cycle: This signal guarantees two sequential even or odd storage cycles by inhibiting priority scanning in the SSU until the second select from the issuing CE. The CE must issue the second select within the SE timeout period or the SE will issued a pulse ELC, reset the priority circuitry, and become available for new requests. The SE does not wait for 'logout stop' and does not reset outstanding selects.

Normal Op: This signal assures that control bus driver or receiver failures do not cause multiple operation execution resulting in lost data. The 'normal op' signal is valid with fetch and store operations only. If it is not sensed with 'fetch or store' or if it is sensed with 'test and set', 'set key', 'double cycle', 'suppress log checks', or 'insert key', an 'address check' is issued to the using CE, the entire SE stops, ELC is issued to all CEs and the SE waits for 'logout stop'.

Select Even: This signal is sent to an SE to request an even storage cycle.

Select Odd: This signal is sent to an SE to request an odd storage cycle.

Logout Stop: This signal sets the 'SE stopped' latch in the SE, causing the SE to halt all activity at the end of the cycle in progress (if not already stopped). The SE issues 'SE stopped' to the using elements and a level ELC to all CEs. It then remains stopped until logged out, reset, or reconfigured.

Logout Select: This signal is sent to the SE to request a doubleword of logout data. The signal is used in conjunction with the three 'logword number' lines which specify the doubleword to be transferred.

Logout Complete (Check Reset): The CE sends 'logout complete' to the SE at the completion of a logout and during a subsystem reset. The SE senses this signal as a check reset and storage is reset. At the completion of the reset sequence, the 'SE stopped' latch is reset.

Reconfigure Select: This signal causes the SE to gate portions of the SDBI into its CCR provided the SE is properly SCONed to the issuing CE. If a CCR parity error exists in the SE when 'reconfigure select' is received or no SCON bits are on and the SE is not in state 0, CCR gating is ignored and the SE accepts the SCON data.

Suppress Log Check: This signal suppresses 'data check' and its associated ELC signal.

P_A and P_B: Parity conversion circuitry in the CE develops the P_A and P_B parity bits for 14 of the SAB bits (bits 6–19) in two groups of seven bits each: P_A for bits 6–12 and P_B for bits 13–19. This parity generation takes into account the bit 20 and bit 6 reversal involved in 'defeat interleave' and the bit 6 inversion for 'storage reverse'.

Because the generation of the parity introduces several nanoseconds of delay, the P_A and P_B are sent separately to each SE via simplex lines rather than with the rest of SAB which uses a distributed simplex bus.

SE-to-CE Interface

- Data fetching.
- Logout data.
- Controls.
- Error monitoring.

The SE-to-CE interface comprises the SDBO, the outkey bus, and two groups of control lines. The buses and one group of control lines are multiple-driver simplex lines. The remaining control lines are simplex. This is shown in Figure 3-6. A description of the SE-to-CE interface buses and lines follows.

Storage Data Bus Out: This 72-bit bus carries eight 8-bit bytes and the associated eight parity bits. The eight bytes consist of data from a normal fetch operation or of logout information during a storage logout operation.

Out-Key Bus: Consists of five key bits and a parity bit. The high-order four bits represent the storage key and the low-order bit is the fetch protect bit. The bus carries the key to the CE during an Insert Key operation.

Advance SDBO: This single multiple-driver simplex line is sent in advance of data on a fetch operation and together with data on all other storage cycle. It is used by the CE as a signal to sample for errors.

Advance Keys: This single multiple-driver simplex line is activated by the Storage Protect feature in the SE during an insert-key cycle to allow the CE to ingate the key from the outkey bus.

Protect Check: This single multiple-driver simplex line is activated by the Storage Protect feature of the SE when the protection key and the storage key do not agree during a normal store or fetch operation.

The following control lines are simplex lines:

Accept: This signal indicates that the SE has received a select from the CE and has started the storage cycle.

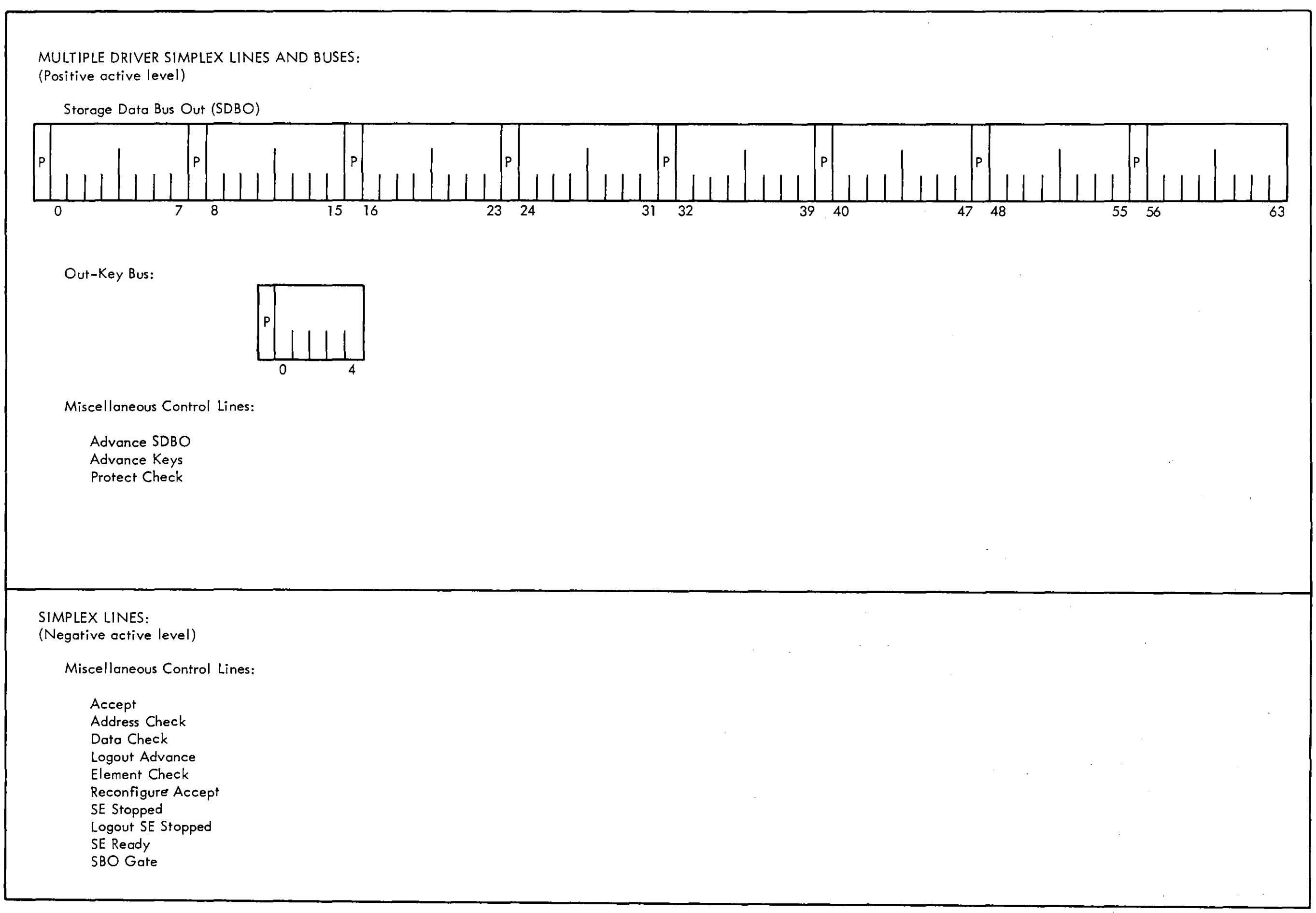
Address Check: This single simplex line is activated by the SE when any of the following addressing errors occur: mark parity, address parity, tag parity, tag mismatch, multi-accept condition, storage protect parity, inkey or outkey parity, or an invalid op error. This signal is always accompanied by a pulse ELC.

Data Check: This single simplex line is activated by a storage data parity error unless inhibited by 'suppress log check'.

Logout Advance: Logout advance is sent to alert the CE that logout data is available on the SDBO.

Element Check (ELC): ELC may be a pulse or a level. It is sent to all CEs regardless of configuration when an error or other abnormal condition occurs at the SE. Pulse ELC is coincident with:

1. CCR parity error.
2. Temperature out of tolerance check (OTC)



•Figure 3-6. SE to CE Interface Lines

3. 'On-battery' signal
4. Storage check, address check, or data check

Level ELC is coincident with:
1. Overvoltage or overcurrent condition.
2. Power off or power check
3. 'SE stopped'.

Reconfigure Accept: This signal indicates to the CE that the SE has loaded the reconfiguration data from the SDBI into the CCR and that good parity exists.

SE Stopped: The 'SE stopped' signal is issued to all configured CEs to indicate that the SE has stopped in response to a 'logout stop' (LOS) signal from a CE or IOCE. This signal inhibits all operations except logout, reconfiguration, and reset.

Logout SE Stopped: This simplex line has the same timing as "SE stopped" except that it is not degated in Diagnose Logout mode. It enables the CE to store the final word of the SE logout and allows correct operation of CE SCI logout controls after the rise of "logout complete".

SE Ready: This signal indicates to the using element that the SE is available; i.e., the SE has power up, is not in test, is properly configured, and is not being reset.

SBO Gate: This signal is used by the CE to identify the SE.

CE-IOCE Interfacing

The 9020D system includes a maximum of three IOCEs, each of which controls one multiplexer channel and up to three selector channels. All system communication (except configuration) with I/O units is accomplished through the IOCEs by means of the following five I/O instructions:

Start I/O
Test I/O
Halt I/O
Test Channel
Set PCI

Because all I/O operations are initiated by I/O instructions, the CE must have control over the IOCEs. Any CE can control any IOCE. One CE may have several IOCEs on-line (configured) at one time. However, the communication between a CE and the IOCEs is in an interleaved manner, allowing an operation between the CE and only one IOCE at a given instant. Any IOCE, on the other hand, may be under control of only one CE at a time.

During I/O operations, certain control signals pass directly between the CE and IOCE via the CE-IOCE interface; control information is passed between the CE and IOCE via main storage. During execution of an I/O instruction, the CE signals the selected IOCE which channel and unit are to be selected and which of the I/O instructions is to be executed. The CE also transmits a quantity called the preferential storage base address (PSBA) which indicates to the IOCE which preferential area contains the CAW, CSW, PSWs, and other critical control information. The CAW and CSW locations are used for CE-IOCE communication. Upon completion of the I/O instruction, the IOCE transmits a value to be placed in the CE's condition code register. Subsequent CE instructions may be used to test the condition code to determine the result of the I/O instruction.

I/O interruptions are also controlled over the CE-IOCE interface. The CE transmits the system mask portion of its current PSW to the IOCE. The IOCE uses the system mask to gate the channel interruption conditions when signaling its controlling CE of an outstanding interruption. At the end of its current instruction, the CE supplies the PSBA and signals the IOCE to proceed with the interruption. At this time the IOCE performs the highest priority pending interruption that is not masked off. After the CSW has been stored, the IOCE stores the associated channel and unit address and a portion of the system mask in the proper location in main storage to partially form the old PSW for the I/O interruption. Upon completion of the channel portion of the interruption, the IOCE signals the CE to complete the interruption.

The CE-IOCE interface is also used to perform other specific functions such as IPL, FLT load, logout, start I/O processor, and direct control.

CE-to-IOCE Interface

- Configuration control.
- ATR control.
- I/O instructions.
- Start I/O processor.
- Direct control.
- IPL controls.
- FLT load controls.
- I/O and MC interrupt controls.
- Logout controls.
- No data transfer.

Interfacing for the CE to IOCE includes a control bus and associated signal lines. The control bus transfers information such as configuration masks, ATR assignment masks, PSBAR indications, IPL and FLT operations, I/O instructions including start I/O processor, and direct control commands such as write direct processor start, stop, or interrupt. The control bus is never used for data transfer. Control signals define the information on the control bus and synchronize the various operations. The various lines and buses are shown in Figure 3-7 and are described in the following paragraphs.

Control Bus: The control bus contains 36 multiplexed lines: 32 bit positions plus 4 parity bits. It services the CCR, ATR, I/O processor, I/O instructions, IPL, logout, interrupt signals, and FLTs.

1. 'Reconfigure select' and 'SATR select' use the bus to set the CCR or ATR.
2. I/O instructions use the bus to transmit the channel and unit address, the PSBA, and the I/O instruction identification.
3. IPL and FLT load use the bus for the channel and unit address and PSBA.
4. Logout uses the bus for PSBA only.
5. 'Permit interruption' uses the bus for PSBA only.
6. 'Start I/O processor' uses bus to transmit a storage key and an address.

System Reset (1, 2): This is a 1 ms signal which precedes a system IPL. The 'system reset' is sent on two lines. These lines are not gated by the CCR.

When active, 'system reset' performs hardware and microprogram resets in the IOCE provided the test switch is not on. 'System reset' causes the CCR to be reset to zeros except for the SCON bits which are set to all 1's.

Subsystem Reset (1 line): This line is activated by the CE to cause the IOCE to do an element reset. To be effective the IOCE must be properly configured to the sending CE. The IOCE does not reset its CCR as a result of 'subsystem reset'.

System Mask Bits 16–19: These lines are sent to all IOCEs and are used in forming the first portion of the PSW byte 2 on channel interrupts. See also 'System Mask' below.

360 Mode Operation: This signal causes the IOCE to operate in the 360 mode.

The following lines are all simplex:

I/O Instruction: This line is sent to a selected IOCE. The PSBA, unit address, channel address, and the decoded I/O instruction are placed on the control bus. The I/O instruction line is then brought up to tell the IOCE to take the information from the control bus. The line remains static until a response is received from the IOCE.

FLT Load: This line is not used by the CE in the 9020D system. The 'initial program load' (IPL) line is used when performing an FLT load from a CE.

Initial Program Load: This line, generated in the same manner as I/O instruction, indicates to the selected IOCE that it is to perform an IPL. The control bus contains the PSBA and the unit and channel address when this line is brought up.

Permit I/O Interrupt: This line is sent to the IOCE in response to an IOCE I/O interrupt request. This signal allows the IOCE to store its CSW and interrupt code field of the PSW.

Logout: This line is issued from a write direct instruction and causes the IOCE to begin a logout operation. The IOCE must be SCONed to the sending CE.

Reconfigure Select: Configuration select is three lines, one to each IOCE. Each line is generated from the select mask and gates the configuration bits from the control bus into the IOCE. The IOCE must be configured to the CE.

System Mask: The system mask lines are static lines from the CE's PSW register bits 0–6 and 16–19. These lines mask the channels in the IOCEs and are distributed as follows:

PSW bits 0–3 to IOCE 1
PSW bits 4–6, 16 to IOCE 2
PSW bits 17–19 to IOCE 3
PSW bits 16–19 to all IOCEs

Bits 16–19 are sent to all IOCEs and are used in forming the first portion of the PSW byte 2 on channel interrupts. These bits (16–19) are sent via distributed simplex lines however.

Permit Machine-Check Interrupt Request: This line is sent to configured IOCE in response to a machine-check interrupt request. This signal allows the IOCE to continue with the logout.

FLT Backspace: This signal causes the IOCE to branch from its wait loop and backspace the FLT tape over one record. When the operation is completed, an FLT complete signal is returned to the CE.

SATR Select: This select line signals and conditions the selected IOCE for receiving the new address translation assignment mask on the 36-bit control bus. Three select pulses are required, one for initial selection and two for transmission of ATR 1 and ATR 2.

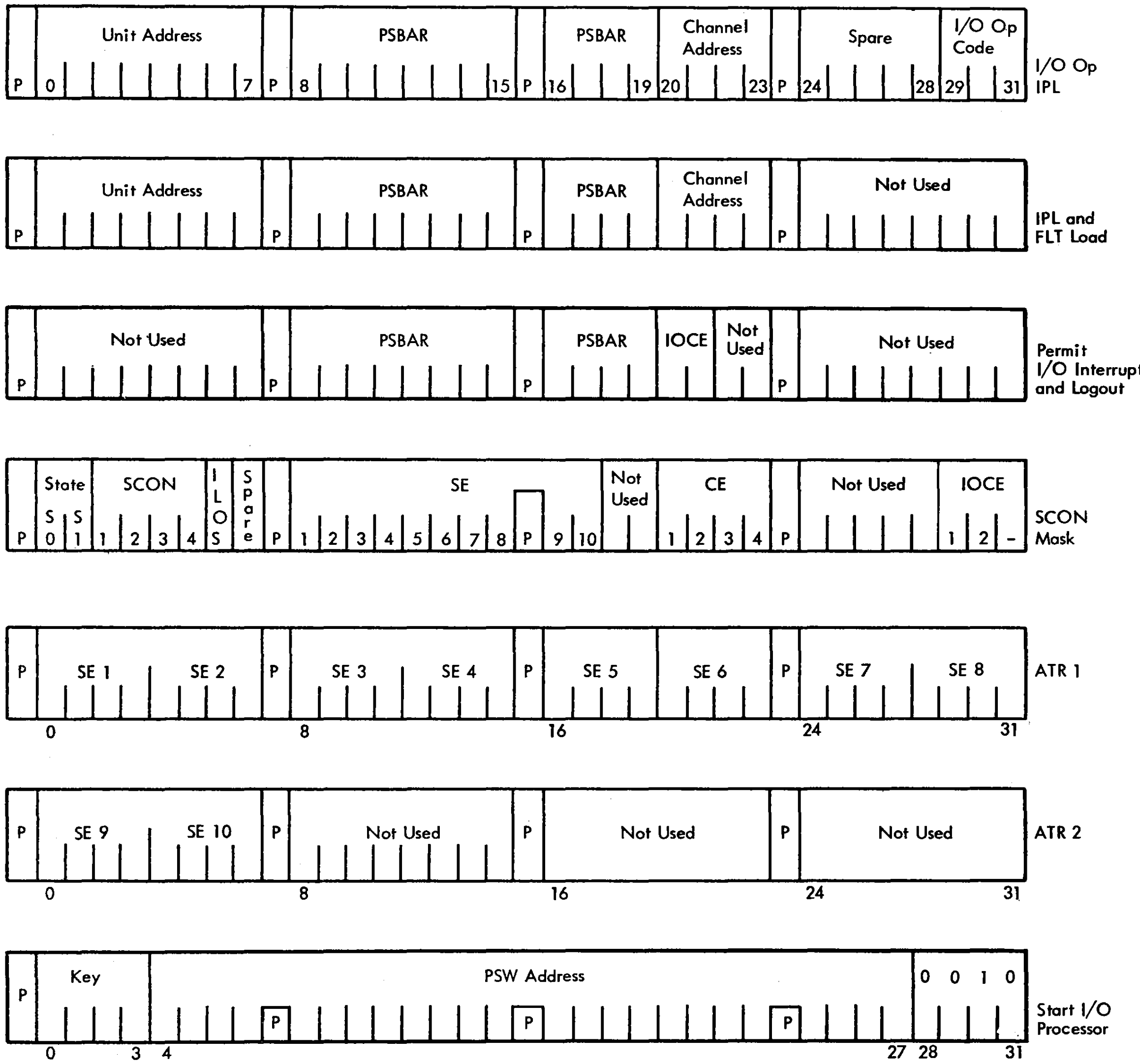
Write Direct Start: This line causes an IOCE processor to leave the stopped state and go to either the running or wait state. This signal is sent to the IOCE when the CE executes an SIOP instruction. When SIOP is sent, the control bus has data in the format labeled "Start I/O Processor" in Figure 3-7.

Write Direct Stop: This line causes an IOCE processor to go to the stopped state at the end of the current processor instruction.

Write Direct Interrupt: This signal causes an external interrupt of an IOCE processor.

DISTRIBUTED SIMPLEX LINES AND BUSES:

Control Bus:



The control bus is 36 bits time-shared by the above formats.

Miscellaneous Distributed Simplex Lines:

System Reset (2 lines)
Subsystem Reset (1 line)
System Mask Bits 16 - 19 (4 lines)
360 Mode

SIMPLEX LINES:

1. I/O Instruction
2. FLT Load (not used in 9020 D/E)
3. Initial Program Load
4. Permit I/O Interrupt
5. Logout
6. Reconfigure Select
7. System Mask Bits
8. Permit Machine Check Interrupt
9. FLT Backspace
10. SATR Select
11. Write Direct Start
12. Write Direct Stop
13. Write Direct Interrupt

Figure 3-7. CE to IOCE Interface Lines

IOCE-to-CE Interface

- Control signals.
- Request signals.
- Error signals.
- No data transfer.

Interfacing from the IOCE to the CE is concerned primarily with control type signals. The control bus used to transfer information from the CE to the IOCE is strictly a one-way bus, and performs no functions in this section. Programming restrictions allow an IOCE to be configured to only one CE at a time. Figure 3-8 shows the IOCE-to-CE interfacing lines.

DISTRIBUTED SIMPLEX LINES: 1. Condition Code 2. SCON/SATR Response 3. Response 4. Check Response 5. Reset ROS Timeout 6. PSA Lockout 7. FLT Complete 8. Write Direct Interrupt 9. TIC 10. Gap 11. Element Check (ELC)
SIMPLEX LINES: 1. On Battery Signal (OBS) 2. Out of Tolerance Check (OTC) 3. I/O Interrupt Request 4. Machine Check Interrupt Request

Figure 3-8. IOCE to CE Interface Lines

Condition Code: These two lines are sent to the CEs as the result of an I/O operation indicating a value to be set into the PSW.

SCON/SATR Response: This response is sent to the CE after the SCON instruction has been accepted and the IOCE has set its CCR without detecting a parity error in the CCR. This response signal is also used as a set address translation response to acknowledge that: (1) the receiving CE was properly SCONed and (2) the ATR 1 and ATR 2 assignment masks were properly received.

Response: This line sent to the CE indicates that: the condition code for an I/O operation is present, IPL is complete, I/O interruption is complete (CSW and the interrupt code field of the old PSW are stored); and machine check interrupt is complete (CLU logout).

Check Response: This signal line to the CE indicates that a parity check has been detected in the IOCE on data from the CE via the control bus.

Reset ROS Timeout: This signal sent to the CE indicates that the IOCE will process the I/O instruction but is presently processing data. The signal resets the CE's countdown loop to its maximum value, preventing it from timing out.

PSA Lockout: This line indicates that the IOCE tried to access the PSA but did not receive a reply from the SE accessed, or that the PSA access was issued to a logout-stopped SE. This signal causes a program interruption in the CE.

FLT Complete: This response to the CE indicates that the FLT backspace request has been completed.

Write Direct Interrupt: This line is used by the I/O processor to signal the CE to take an external interrupt.

TIC: This signal is sent to the CE to indicate that a Transfer in Channel (TIC) command has been encountered in the channel. It is used by the CE when running FLTs.

Gap: This line is sent to the CE to indicate that the channel has encountered an interrecord gap; i.e., the end of a tape record. The CE uses this signal when running FLTs.

Element Check: This signal is issued by an IOCE as a pulse whenever:

1. A parity error is detected in the ATR.
2. An error condition is detected requiring a CLU or selector channel logout.

The 'element check' signal is issued as a level if, during a CLU logout, the IOCE detects a condition which will not permit logout to be performed. The signal causes an external interrupt in the CE.

On-Battery Signal (OBS): This signal, when issued as a static condition to the CE, indicates that the IOCE is operating on its battery supplies. The OBS, which is issued as a pulse whenever a CCR parity is detected during execution of the SCON operation in the IOCE, causes an external interrupt in the CE.

Out-of-Tolerance Check (OTC): This signal to the CE indicates that the IOCE temperature sensing thermals have detected an out-of-bounds temperature. This signal causes an external interrupt in the CE.

I/O Interrupt Request: This signal from the IOCE informs the CE of status changes in the channels or I/O devices. When a status change is detected by the IOCE and the channel is masked on, an 'I/O interrupt request' is sent to the CE. The channel which requested the interrupt waits for a 'permit I/O interrupt' from the CE before storing a channel status word which indicates the reason for the interrupt request.

Also stored are the channel and unit address, IOCE address, and mask bits 16–19 for the old PSW. If the channel control check or the interface control check bit is on in the CSW, a selector channel logout has been performed.

Machine-Check Interrupt Request: The detection of a CLU error by an IOCE causes the IOCE to stop and request a PSBA for logout via the 'machine-check interrupt request'.

A CE engaged in an I/O instruction or interrupt process with the IOCE issuing the machine-check interrupt request terminates the process and proceeds to the next I-fetch. That I-fetch, or any I-fetch, has an exception branch to a special microprogram routine. This routine issues a "permit machine-check interrupt" and enters a timing loop while the IOCE performs a logout. The IOCE holds up "reset time out" while logging out. The CE waits for a response line or, in case of further IOCE error, a time-out. In either case, the CE completes a machine-check interrupt by storing and fetching the correct PSWs. No logout occurs in the CE. The old PSW contains the IOCE identity in the interrupt code as follows:

IOCE	Bit 30	Bit 31
1	0	1
2	1	0
3	1	1

A time-out condition should always be accompanied by an IOCE element check. Simultaneous I/O interrupt requests for MC interrupt from multiple IOCEs are serviced in the following priority: IOCE 3, 2, and 1.

CE-PAM/SCU/TCU Interfacing

Interface lines between the CE and PAM, CE and SCU, and the CE and TCU, for the most part, represent reconfiguration, system resets, and element checks. Other than these lines, there is no control or data flow directly to or from the CE. Figure 3-9 shows interface lines and buses between the CE and the PAM/SCU/TCU.

CE-to-PAM/SCU/TCU Interface

- Configuration.
- System reset.

Configuration Mask: Only the required 11 positions of the overall configuration mask are sent to the PAMs, SCUs, and TCUs. The items sent include the two state bits, the four-bit SCON field for reconfiguration, and the three-bit field to define the controlling IOCEs. Two parity bits are used in the transfer.

DISTRIBUTED SIMPLEX LINES AND BUSES:

Configuration Mask (from CE):

P	State		SCON				P	IOCE		
0–7	0	1	1	2	3	4	24–31	1	2	3
	0	1	2			5		29		31

System Reset (2 lines from CE)

Note: The configuration mask originates from the external register in the CE; the reset lines originate from control circuitry. These lines are distributed simplex origination in one CE and terminating in one or more PAM/SCU/TCU.

SIMPLEX LINES:

Element Check (ELC) (from PAM/SCU/TCU 1, 2, and 3)

MULTIPLEX LINES:

Configuration Select/Response (from PAM/SCU/TCU 1, 2, and 3)

Note: These three lines have both a driver and a receiver at each end of the line.

• Figure 3-9. Interface Lines Between CE and PAM/SCU/TCU

System Reset (1, 2): The 'system reset' signal results from a system IPL. It causes a hardware reset to the PAM, SCU, or TCU. The reset is not gated by the CCR. All bits in the CCR are reset to zeros except the SCON bits which are set to all 1's.

Configuration Select: This line, carrying a 5.0-usec pulse, causes the PAM, SCU, or TCU to set the configuration mask into its CCR. The PAM, SCU, or TCU honors the select if the selector's SCON bit is on in the receiving PAM, SCU, or TCU's CCR.

PAM/SCU/TCU-to-CE Interface

- Element check.
- Configuration response.

Element Check: A level simplex signal is sent from each PAM/SCU/TCU to all CEs when one of the following conditions occur:
1. Parity check in the CCR
2. Power failure

Configuration Response: This line is sent to the CE in response to configuration select if the select was honored and the CCR parity was correct.

CE-System Console (SC) Interfacing

- Switch and indicator lines for control and monitoring of CE from SC.

- Monitoring.

The greater portion of the interface is concerned with sending indication (status) signals from the CE to the SC and control signals from the SC to the CE. The CE cannot initiate any data transfer directly to the SC via the interface. Subsystem configuration indications, for example, which are under program control, are initiated by the CE and handled as a normal I/O operation via the IOCE.

CE-to-SC Interface

- Address indications.
- State indications.
- Register indications.
- Error or condition indications.

Many of the indications from the CE to the SC represent the current status of the CE. The most important dynamic indications include the state of the CE, logic checks, current instruction address, and manual and wait status. The CE to SC lines and buses are shown in Figure 3-10 and are individually described in the following paragraphs.

Data Indicator Lines: These 36 multiple-driver simplex lines provide for the display of four bytes of data from a main or local store location. They originate in the CEs at the T-register.

Load Indicator: This multiple-driver simplex line originates in one or more CEs and turns on a common indicator. The indicator is lit by the respective CE from the time an IPL operation starts until the operation is complete.

Invalid Selection: This multiple-driver simplex line originates in one or more CEs and turns on a common indicator. The selected CE lights the indicator whenever an invalid or illegal storage address is specified by the operator during a manual operation.

Instruction Counter (IC) Indicators: These 27 simplex lines provide data to the SC for the display of the current instruction address at the CE. One set of these lines is indicated at the SC for each CE.

Manual Indicator: These simplex lines originate in each CE and terminate in a unique indicator at the SC to indicate when the associated CE is in the stopped state.

Wait Indicator: These simplex lines originate in each CE and terminate in a unique indicator at the SC to indicate when the wait bit in the associated CE's PSW is set to 1.

State Indicators: These four simplex lines originate in each CE and terminate in unique indicators at the SC. One and only one of these four signals will always be active to reflect the present status of the originating CE.

Logic Check Indicator: These simplex lines originate in each CE and terminate in a unique indicator at the SC to indicate that the CE has detected one of its own logic check conditions.

Power Check: This signal line indicates that the temperature in the CE has drifted to within about 10% of the shutdown tolerance. The signal also indicates the loss of voltage or a normal power-off (but not an element master power-off) condition.

Battery: This signal indicates that the CE has switched to battery power.

SC-to-CE Interface

- Controls to CEs are gated by system interlock.
- Distributed simplex control lines.

All SC controls to the CEs are gated by the system interlock switch which requires a key operation to activate the logic. SC operations require that the CE test switch be off. In addition, all functions going to the CE (except for 'all stop') are further gated in the appropriate CE by a 'select CE' signal originating from the select CE rotary switch on the SC. The interface lines are shown in Figure 3-11 and are described in the following paragraphs.

Address Keys: These 24 signal lines (+3 parity) result from the 24 instruction address keys on the SC and provide addressing of any addressable local store or main storage location.

Data Keys: These 32 signal lines (+4 parity) result from the 32 storage data keys on the SC and provide manual data for storing into any addressable local store or main storage location.

CE Select: These four select lines result from the four-position rotary switch at the SC. Proper CE selection is under switch card control in the receiving CEs. This signal provides the necessary gating in the CEs for all manual operations (except 'all stop') issued from the SC. The SYSTEM INTERLOCK switch must be turned on for this select switch to be enabled.

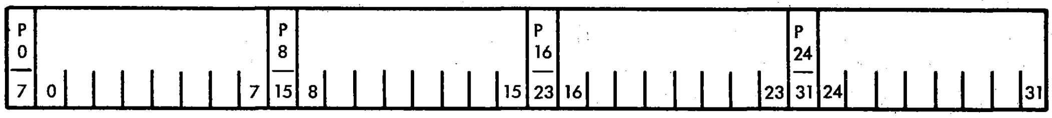
Stop: This signal places the selected CE in the stopped state without desroying its environmental status. The selected CE proceeds to the end of the instruction being executed at the time the stop is initiated. If the current instruction causes a program interrupt, program status words (PSW) will be changed before stopping. An I/O device will be allowed to complete its operation although I/O or external interrupts will not be recognized.

Start: This signal starts the selected CE. If start is issued after a manual stop, the CE continues as if no stop occurred.

Store Select Main: This signal results from the storage select switch being in the main storage position and causes

MULTIPLE-DRIVER SIMPLEX LINES AND BUSES:

Data Indicator Lines (T-Register):

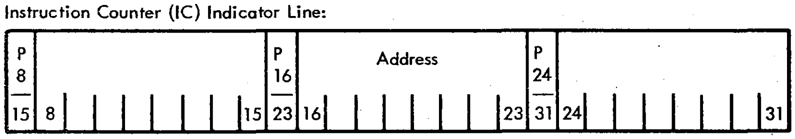


Miscellaneous Lines:

1. Load Indicator
2. Invalid Selection

SIMPLEX LINES AND BUSES:

Instruction Counter (IC) Indicator Line:



Miscellaneous Simplex Lines:

1. Manual Indicator
2. Wait Indicator
3. State Three Indicator
4. State Two Indicator
5. State One Indicator
6. State Zero Indicator
7. Logic Check Indicator
8. Power Check
9. Battery

Figure 3-10. CE to System Console Interface Lines

main storage addressing at the selected CE during either fetch or store manual operations. This signal line is not active with the storage select switch in the local store position, causing local storage addressing at the selected CE.

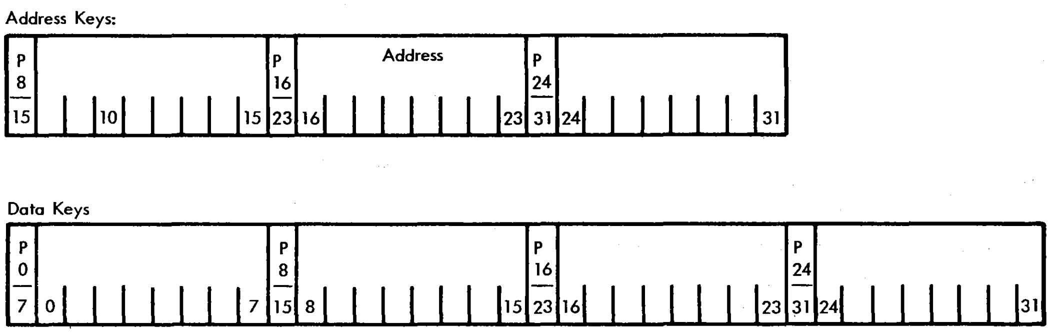
Display: This signal causes the selected CE to place the contents of a storage location specified by the address keys and storage select switch, onto the data indicator lines to the SC.

Store: This signal causes the selected CE to store the contents of the SC storage data keys in the storage location specified by the 24 address keys and the storage select switch.

Set Instruction Counter (IC): This signal transfers the contents of the SC address keys to the instruction counter of the selected CE.

Interrupt: This signal results from depression of the interrupt key and causes a console interrupt signal which sets bit 25 in the PSW of the selected CE.

DISTRIBUTED SIMPLEX LINES AND BUSES:



Miscellaneous Lines:

1. CE Select (4 lines)
2. Stop
3. Start
4. Storage Select Main
5. Display
6. Store
7. Set IC
8. Interrupt
9. Address Compare Stop
10. Address Compare Loop
11. Rate
12. Load
13. Load Unit Address (9 lines)
14. Load Channel Address (5 lines)
15. Load Storage Select (5 lines)
16. Activate
17. Control CE (4 lines)
18. All Stop

Figure 3-11. System Console to CE Interface Lines

Address Compare Stop: This line conditions the selected CE so that any storage access to the address specified in the SC address keys causes the CE to enter the stopped state at the end of the instruction that made the memory reference.

Address Compare Loop: This line causes the selected CE to loop between the address set in the SC address keys and the address set in the storage data keys. When the selected CE makes a storage access to the address specified in the address keys, an unconditional branch is made at the end of the instruction to the address specified in the storage data keys. Programming can establish a loop condition between the two sets of keys.

Rate: This signal operates with the selected CE and the start and stop keys on the SC. With this signal, each depression of the start key results in one complete instruction being executed. Any machine instruction can be executed in this mode.

Load: This signal line initiates an IPL in the selected CE.

Load Unit Address Bits: These eight signal lines (+ parity) result from two of the three rotary-type load unit switches on the SC. These two hexadecimal characters provide an I/O unit address for use during IPL operations.

Load Channel Address Bits: These four signal lines (+ parity) result from one of the three rotary-type load unit switches on the SC. This hexadecimal character selects one of the 11 possible channels on the 9020 system.

Load Storage Select Bit: These four signal lines (+ parity) result from a rotary main storage select switch on the SC. This hexadecimal character represents a main SE to be selected during IPL or manual operations.

Activate: This signal causes the SCON bits at the selected CE to be set according to the setting of the control CE switches on the SC.

Control CE: These four signal lines (+ parity) result from individual switches on the SC and allow manual setting of the SCON bits in the configuration register. Actual setting of the SCON field occurs with depression of the ACTIVATE key on the SC.

All Stopped: This signal causes all CEs to enter the stopped state. The system interlock switch must be turned on to activate the all-stop key, but the setting of the select CE switch does not affect this operation.

I/O CONTROL ELEMENT INTERFACING

- Interfacing to and from: CEs, SEs, PAMs, SCUs, TCUs, and SC.
- I/O control and data transfer.
- Monitoring.

The IOCE is primarily concerned with the movement of data both to and from the I/O equipment. The IOCE is therefore connected to the PAMs, SCUs, TCUs, and SEs to act as a control and synchronizing element in the transfer of data both into and out of the main system.
control, and monitoring of the various I/O operations. This communication is strictly concerned with control; there is no data transfer between the IOCE and CE.

Data transfer is also accomplished between the IOCE and the 1403 Printer, 2540 Card Read/Punch, 1052 Printer Keyboard, and the SC. Each of these devices has an assigned unit address and can be controlled by the main program via the IOCE multiplexer channel.

Control of IOCE processor operations is a secondary function of an IOCE. Interface lines involving the IOCE processor are between the CE and IOCE and have been described previously.

Communication with the SC is also concerned with the static indication of the four IOCE element states and two check conditions on the SC operator's panel.

IOCE-CE Interfacing

All signals and buses which exist between the IOCE and CE have been explained previously under "Computing Element Interfacing". References to this interfacing can be seen in Figures 3-7 and 3-8.

IOCE-SE Interfacing

- Data transfer one word at a time.
- Control signals.
- Error monitoring.

IOCE-SE interfacing, while similar to CE-SE interfacing, is not the same. The differences arise primarily because the IOCE storage data path is one word wide rather than a doubleword like the CE, and because the IOCE time-shares that data path with addresses rather than having a separate address bus as does the CE.

Other differences appear because the IOCE cannot perform certain operations, such as Set Storage Key or SCON, which the CE performs. However, the basic similarity remains in that the interface provides for data transfers and control signals to and from storage and for error monitoring.

IOCE to SE Interface

- Addressing.
- Data storing.
- Control.

The interface from the IOCE to the SE involves a distributed simplex bus, which is time-shared between addresses and data, and a group of distributed simplex control lines. In addition, a group of simplex lines are used for transmitting control signals. The IOCE-to-SE interface lines are shown in Figure 3-12 and are described in the following paragraphs.

Data, Address, Keys In Bus (called "Output Bus" at IOCE: This is a 36-bit distributed simplex bus which is time-shared by two different formats, as shown in Figure 3-12. Note that the address format is shown twice because the bits are relabeled at the SE. The upper format shows the bits as they are labeled at the IOCE; the lower format shows them as they are labeled at the SE. During the initial portion of a storage cycle, the IOCE sends the address to be accessed together with a key (bits 0–3) to be compared with the protect key in the storage protect array in the SE. On a store operation, the data to be stored is sent on the same bus later in the cycle after the IOCE has received Accept from the SE.

During the time the bus is used for address and keys, the unused bits (4–7) are always zero. When the address is for a PSBAR access, the key bits are forced to 0 and the key parity bit is forced to 1 to maintain odd parity in the first byte.

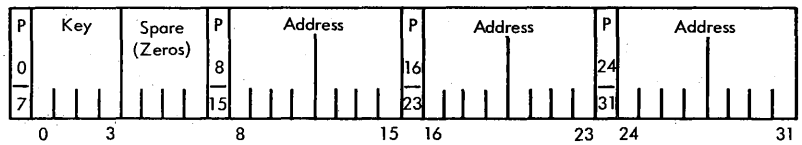
The address consists of 24 bits labeled 0 to 23. Bits 1–4 are Box Tag bits which are compared against a jumper card in the Storage Switch Unit (SSU) portion of the SE to assure that the correct SE has been accessed. Bits 21–23 are used as a three-bit binary code to specify the byte to be set to all 1s during a Test and Set operation.

Normal Op: The 'normal op' line is a distributed simplex line raised by the IOCE whenever a Store or Fetch cycle is requested. It assures that control bus driver or receiver failures do not cause multiple operations to be executed at the same time with attendant loss of data. If it is not sensed with Fetch or Store or if it is sensed with any other

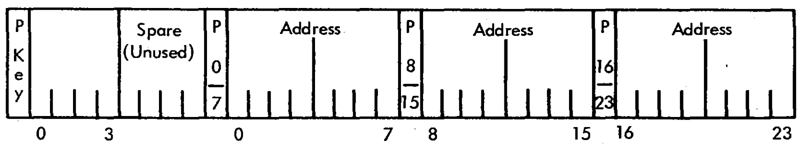
DISTRIBUTED SIMPLEX LINES AND BUSES:
(Positive active level except Normal Op)

Data, Address, Keys in Bus:
(Called "Output Bus" at IOCE)

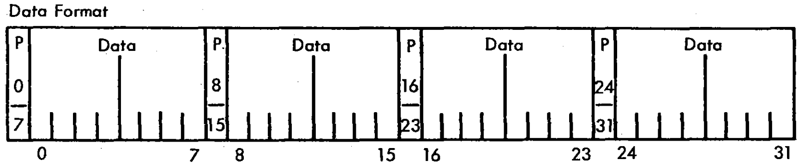
Address Format (IOCE)



Address Format (SE)



Data Format



Notes:

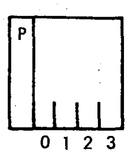
1. When bus is used for keys and address, bit positions 4-7 (first byte) are always 0.
2. During PSBAR access, Key bits are forced to 0 and key parity to 1.
3. During Test and Set operation, address bits 21-23 (SE address format) constitute a three bit binary code indicating which one of the eight bytes is to be fetched and set to all 1's.
4. Address bits 1 to 4 (SE address format) are Box Tag bits supplied for comparison against a jumper card in the SSU portion of the SE.
5. Address format shown for both IOCE and SE because bits are relabled at SE.

Miscellaneous Lines:

1. Normal Op (Negative Active Level)
2. Double Cycle
3. IOCE Power Bit Interlock (Called "IOCE to SE Power Good" at IOCE)

SIMPLEX LINES:
(Negative active level except Store)

IOCE Marks (5 lines):
(Called "Byte Stats"
at IOCE)



Miscellaneous Lines:

1. Access Request
2. Test and Set
3. Split Cycle
4. Logout Stop
5. Ignore Errors
6. Suppress Log Check
7. FLT Load
8. Store

Figure 3-12. IOCE to SE Interface Lines

operation (Test and Set, Suppress Log Check, or Double Cycle) the entire SE is stopped. In this case a storage check is sent to the IOCE and a pulse ELC is sent to all CEs. The wait timeout for Logout Stop will occur.

Double Cycle: This distributed simplex line is activated by the IOCE to request two sequential storage cycles, both even or both odd. This is done during immediate instructions NI, OI, and XI. If the IOCE does not generate the second request within the SE timeout period, a pulse ELC is sent to all CEs. When this occurs, all Access Requests are cleared; the SE does not wait for Logout Stop but becomes immediately available for access.

IOCE Power Bit Interlock (Called "IOCE to SE Power Good" at IOCE): When active, this distributed simplex signal allows the SE to set its request latch and the associated response latch for that IOCE. When power goes down on a configured IOCE, this line goes negative and degates the appropriate IOCE receivers to eliminate errors.

The following IOCE-to-SE lines are simplex:

IOCE Marks (Called "Byte Stats" in IOCE): Five simplex lines convey the four Byte Stats and the Byte Stat parity bit to the SE. These become the IOCE marks and are analogous to the marks sent from a CE. The IOCE marks indicate the bytes to be stored during a store operation. There is no signal on these lines except during a store operation. The IOCE mark parity (byte stat parity) bit maintains odd parity; a parity check from these lines is ORed with SE mark parity check.

Access Request: This simplex line is raised by the IOCE to request priority from the SSU for a storage cycle. It rises at the beginning of the first machine cycle associated with a storage cycle and stays active until the request has been accepted by the SE.

Test and Set: This simplex line signals the SE to fetch the data byte specified by address bits 21, 22, and 23 (bus bits 29, 30, and 31) and, after transmitting the byte to the IOCE, forces it to all 1's on the regeneration cycle. All other bytes are regenerated as read out.

Note: Three bits are requires to specify one of the four bytes addressed by the IOCE because the SE fetches a doubleword at a time and must actually select one of eight bytes.

Split Cycle: This signal is not used by the SE but is terminated by the SE.

Logout Stop (LOS): This simplex line is used by the IOCE to set the 'SE stop' latch at the end of the current storage cycle to allow the CE to proceed with a logout. Higher priority elements are prevented from accessing the SE. The LOS signal is sent from the IOCE when a data check occurs on a fetch or when a storage check occurs.

Ignore Errors: This signal is not used by the 7251-09 SE to alter any storage operation. It is used only in normal op-checking logic.

Suppress Log Check: This signal prevents the SE from sending out error signals resulting from data check logic. No storage check or ELC is sent when a data error is detected and 'suppress log check' is active.

FLT Load: This signal is not used by the SE but is terminated by it.

Store: This line is sent with 'access request' to notify the SE that a store operation is being requested. It must drop before the IOCE can take part in the SE priority scan. The IOCE can participate in the priority scan immediately if the line is inactive (fetch operation requested).

SE-to-IOCE Interface

- Data transfer.
- Control.
- Monitoring.

The SE-to-IOCE interface is primarily concerned with the transfer of data from storage to the IOCE during a fetch operation. A distributed simplex bus provides this data path. In addition, a group of simplex lines provide for control and error monitoring. The interface is shown in Figure 3-13, and the lines and buses are described here.

Data Bus Out (Called "Input Bus" at IOCE): The 'data bus out' consists of 36 lines (32 data bits and 4 parity bits) and is a simplex bus from one SE to each IOCE. It serves to transfer four bytes of data at a time during a fetch operation.

Note: The following lines are all simplex.

Accept: This signal is sent to the IOCE to indicate that the SE has accepted the IOCE access request and to request that the IOCE place data on the bus if the request was for a store operation.

Request Acknowledged: This signal is sent to the IOCE to indicate that the SE has recognized a request from that IOCE and that the SE is properly configured to the requesting IOCE.

Gate Data: This signal indicates to the IOCE that data is available on 'data bus out'.

Storage Check: This signal is sent to the IOCE to indicate that one of the following errors has been detected in the SE:

1. Parity check on IOCE marks (byte stats), key, address, or data.
2. Box Tag mismatch or parity.
3. Invalid operation (normal op check).
4. Multiaccept.

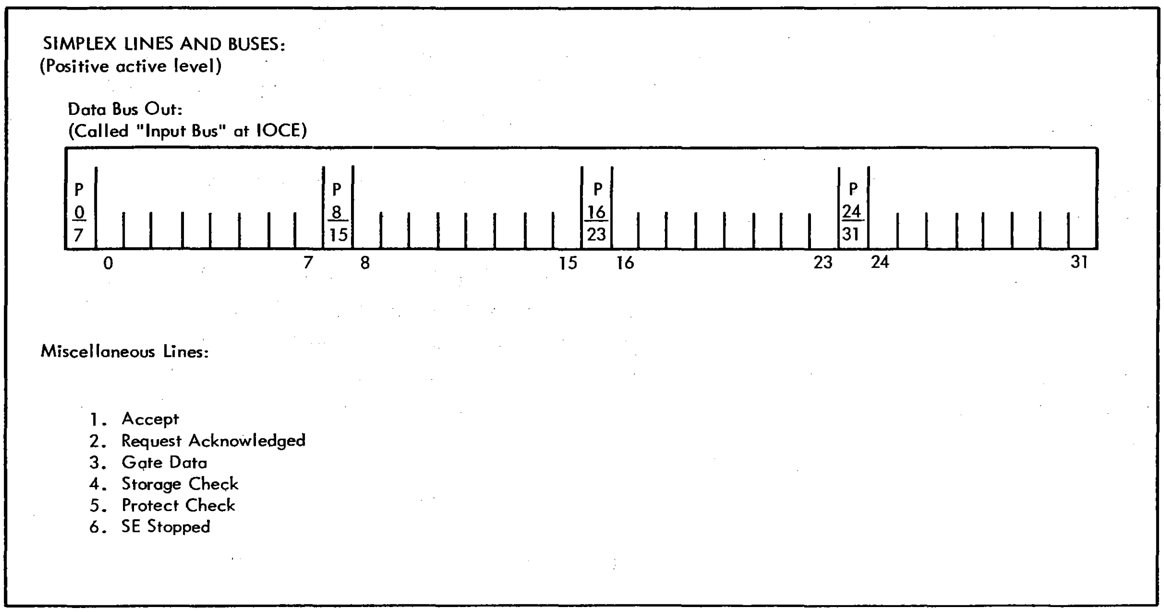


Figure 3-13. SE to IOCE Interface Lines

The 'storage check' also causes a pulse ELC to be sent to all CEs and starts the wait timeout.

SE Stopped: This signal indicates to the IOCE that the SE is being logged out. 'SE stopped' inhibits all operations except logout, reconfiguration, and reset which are CE-initiated operations.

IOCE-PAM/SCU/TCU Interfacing

- Standard I/O interfacing.
- Data transfer.
- Control.

Data transfer and controls between the IOCE and the external devices are via the multiplexer and selector channels and are strictly on the standard I/O interface. Additional information can be found under "Standard I/O Interface Summary" later in this chapter.

IOCE-System Console Interfacing

- Standard I/O interface.
- Data transfer between:
  1403 Printer
  2540 Card Read/Punch
  1052 Printer Keyboard
  System Console
  System Maintenance Monitor Console (external to CCC System)
- Status information to SC.

Two rotary switches and two selection-enable pushbuttons on the SC provide the ability to interconnect the printer, card reader, card punch, and 1052 to any one of the three available IOCE interfaces. Data is transferred to and from these individually addressable devices by the multiplexer channels, using the standard I/O interface.

The SC is also addressable by means of the standard I/O interface. A series of channel commands can, for example, be used to sound a bell or buzzer, set the mode indicator, set the programmable configuration lights, and read the sense switches.

The System Maintenance Monitor Console (SMMC), which is located externally to the CCC system, can also be addressed via the SC. Communication here, too, is via the multiplexer channel.

In addition to the interfacing discussed so far, the following static signals are sent directly to the SC panel:

Element State: Four lines from each IOCE, representing the four element states (0–3), permit the state of each IOCE to be displayed at the SC panel.

Logic Check: This line indicates that a logic check has been detected at the IOCE. It is used to turn on a logic check indicator on the SC panel.

Power Check: This signal is sent to the SC when one of the following occurs:

1. Normal power off.
2. Power down due to power check.
3. Temperature out of tolerance check (OTC) which occurs when the temperature in the IOCE drifts to within about 10% of the shutdown tolerance.

Note: Power check signal is not sent during element master power-off.

Battery: A line from each IOCE is used to signal the SC when an IOCE switches to battery backup power. This line activates a single indicator common to all elements in the system having battery backup. One or more of these elements switching to battery operation cause the indicator to light.

SE INTERFACING

- Interfacing to and from CEs and IOCEs.
- Interfacing to SC.
- Data transfer.
- Monitoring and control.

The storage element (SE), as has been stated in previous sections, is directly interfaced with both the CE and IOCE. This interfacing is concerned primarily with the transfer of information in the form of both data and instructions to and from these two major elements. In addition, control signals provide the proper timing and synchronization for the intercommunications. For information regarding SE-CE interfacing, refer to Figures 3-5 and 3-6 and their associated text. For SE-IOCE interfacing, refer to Figures 3-12 and 3-13 and associated text.

SE-SC interfacing is one way from the SE to the SC, via simplex lines having positive active levels. 'Power check' and 'battery' are 24V signals developed from relay logic. It provides the current status of the SE to the SC for indication on the panel. These indicators represent the status of the SE dynamically and are not under program control. The SE-to-SC interface lines are:

Element State: Four lines from each SE, representing the four element states (0–3), permit the state of each SE to be displayed at the SC panel.

Logic Check: This line indicates that a data check, address check, storage check, or protect check has occurred at the SE.

Power Check: This signal is sent to the SC when one of the following occurs:

1. Normal power off.
2. Power down due to power check.
3. Temperature out-of-tolerance check (OTC) which occurs when the temperature in the SE drifts to 10% of the shutdown tolerance.

Note: 'Power check' is not sent during element master power-off.

Battery: A line from each SE is used to signal the SC when an SE switches to battery backup power. This line activates a single indicator common to all elements in the system having battery backup. One or more elements switching to battery operation cause the indicator to light.

PAM INTERFACING

- Interfacing from and to: CEs, IOCEs, SC, and I/O devices.
- Standard I/O Interface to IOCEs.
- Special interfacing to I/O devices.
- Data transfers.
- Control and monitoring.

PAM interfacing between CEs is concerned primarily with reconfiguration, resets, and element checks. Data bytes are not transmitted directly between the PAM and CE. CE-PAM interface is explained under "CE-PAM/TCU Interfacing" earlier in this chapter.

Interfacing between the PAM and the IOCE is based on the standard I/O interface. Information passed between the PAM and IOCE is on a byte basis and can represent data, commands, and sense and status bits.

Interfacing from the PAM to the SC consists of the following indications:

Element State: Four lines from each PAM, representing the four element states (0–3), permit the state of each PAM to be displayed at the SC panel.

Logic Check: This signal is sent from a PAM to the SC when a logic check is detected in the PAM. It is used to turn on a logic check indicator on the SC panel.

Power Check: This signal is sent to the SC when one of the following occurs:

1. Normal power off.
2. Power down due to power check.
3. Temperature out of tolerance check (OTC) which occurs when the temperature in the PAM drifts to within 10% of the shutdown tolerance.

Note: 'Power check' is not sent during element master power-off.

These signals from the PAM dynamically indicate their respective conditions at the lights on the SC operator's panel. Note that there is no battery backup in the PAM and, therefore, no battery signal.

Communication between the PAM and the I/O devices is based on unique interfacing for each of the various classes of devices. These interfaces differ because of the data rates and formats. Each interface has the necessary data lines and controls to perform the required function. Because the type and number of adapters in the PAMs vary widely from system to system, the various adapter-to-I/O device interfaces are not described here. Refer to IBM 7289-02 Peripheral Adapter Module Manual of Instruction for further information.

TCU INTERFACING

- Interfacing to and from CEs and IOCEs.
- Interfacing to SC.
- Standard I/O interface for IOCE communication.
- Data transfer.
- Control and monitoring.

TCU interfacing with the CEs is concerned primarily with reconfiguration, resets and element checks. Data bytes are not transmitted directly between the TCU and the CE. The appropriate signal lines are explained under "Computing Element Interfacing" in this chapter.

Interfacing between the TCU and the IOCE is based on the standard I/O interface. For further information, refer to "Standard I/O Interface Summary" in this chapter.

Interfacing between the TCU and the SC is on a one-way basis consisting of the following signals:

Element State: Four lines from each TCU, representing the four element states (0–3), permit the state of each TCU to be displayed at the SC panel.

Logic Check: This signal is sent from TCU to the SC when a logic check occurs at the TCU.

Power Check: This signal is sent to the SC when one of the following occurs:

1. Normal power off.
2. Power down due to power check.
3. Temperature out of tolerance check (OTC) which occurs when the temperature in the TCU drifts to within 10% of the shutdown tolerance.

Note: 'Power check' is not sent during element master power-off.

These signals from the TCU dynamically indicate the status of the TCU and are not under program control. Note that because the TCU has no battery backup, there is no 'battery' signal.

SCU INTERFACING

- Interfacing to and from CEs and IOCEs.
- Interfacing to SC.
- Standard I/O interface for IOCE communications.
- Data transfer.
- Control and monitoring.

SCU interfacing is the same as TCU interfacing. The SCU interface with the CE is concerned primarily with reconfiguration, resets, and element checks. Data bytes are not transmitted directly between the SCU and the CE. The appropriate signal lines are explained under "Computing Element Interfacing" in this chapter.

Interfacing between the SCU and the IOCE is based on the standard I/O interface. For further information, refer to "Standard I/O Interface Summary" in this chapter.

Interfacing between the SCU and the SC is one-way, from the SCU to the SC, and consists of the following signals:

Element State: Four lines from each SCU, representing the four element states (0-3), permit the state of each SCU to be displayed at the SC panel.

Logic Check: This signal is sent from SCU to SC when a logic check occurs at the SCU.

Power Check: This signal is sent to the SC when one of the following occurs:

1. Normal power off.
2. Power down due to power check.
3. Temperature out-of-tolerance check (OTC) which occurs when the temperature in the DASF drifts to within 10 percent of the shutdown tolerance.

Note: 'Power Check' is not sent during element master power-off.

These signals from the SCU dynamically indicate the status of the SCU and are not under program control. Note that because the SCU has no battery backup there is no 'battery' signal.

SYSTEM CONSOLE INTERFACING

- Interfacing from and to CEs, IOCEs, SEs, PAMs, SCUs, TCUs, and System Maintenance Monitor Console (SMMC).
- Data transfer.
- Monitoring and control.

Interfacing between the SC and the major elements within the system has been discussed in the preceding sections. Most interface signals take the form of element state and check conditions. Therefore, many of the interfaces are of a oneway nature.

Because the SC is the main control console within the CCC system, many interface lines extend to the CE to enable manual operator intervention for starting, stopping, altering, and monitoring the overall operation. These various functions have been explained under "Computing Element Interfacing". The SC is the only major element in the system which is not duplicated. Therefore, all of the essential SC functions have been duplicated at the CE operator's panel.

The SC is also under limited program control by the EXC control program. Therefore, the standard I/O interface which connects with the IOCE multiplexer channels provides a data path for the console sense switches and for those indicators and alarms which are program addressable. In these cases, the SC is treated as just another I/O device.

An interface also exists between the SC and the System Maintenance Monitor Console (SMMC). The SMMC is external to the 9020D system and uses an interface with characteristics different from interfaces within the CCC. The individual interface lines are listed in Figure 3-14.

The SC-to-SMMC interface consists of three types of signals: configuration lamp signals, mode indicator signals, and power check signals. These signals present the same information to the SMMC as is displayed on the SC operator's panel. Brief descriptions of these signals follow:

Configuration Lamp Signals: These signals are carried on 112 lines representing four rows of lamps with 28 lamps per row. All 28 lines for each row must be programmed by the 9020D even though the maximum number of CEs and SEs are not installed in the system. It is the responsibility of the CCC program or the SMMC to recognize the lack of these elements. Provision is made for 12 SEs in order to remain compatible with the 9020A system (which uses the same SC).

Mode Indicator Signals: These signals are carried by 10 lines divided into three alpha and seven numeric signals. The signals correspond to the two positions of the mode indicator on the SC panel. Only one alpha and one numeric line are active at any one time.

Power Check Signals: These signals are provided for 4 CEs, 3 IOCEs, 12 SEs, 3 PAMs, 3 SCUs, and 3 TCUs, making a total of 28 lines. Provision is made for 12 SEs in order to remain compatible with the 9020A (which uses the same SC). A unit activates its power check signal when any of the following conditions exist at the unit:

1. Normal power off.
2. Overtemperature condition.
3. Catastrophic power supply failure.

1052 ADAPTER-1052 INTERFACE

- One adapter in SC.
- Other adapters housed in PAMs.
- Standard I/O interface with IOCEs.

One 1052 adapter is physically located in the SC and others are located in the PAMs. The adapters are connected to the multiplexer channels in the IOCEs via the standard I/O interface.

The PAM 1052 adapters interface with the 1052's via cables from the PAMs to the patchboard in the SC and the cables from the patchboard to the 1052's.

Note: When working with these cables, remember that the cables have the same type of connectors on each end (type A) and that the lines within the cables do not correspond pin for pin at the two ends. The connector block nearest the adapter has a full complement of pins while the other connector block does not.

Figure 3-15 shows the interface lines between the 1052 adapter and the 1052's.

STANDARD I/O INTERFACE SUMMARY

The I/O interface connects a channel with control units. External cables physically connect all control units in a chain, with the first control unit being connected to the channel. The signal lines of the I/O interface consists of an output and an input bus for passing information between the channel and control units, tag lines for interlocking and for controlling the information on the buses, and selection control lines for scanning or selecting the I/O device.

Line Name	Pin	Line Name	Pin
	01S-S3D2		01S-S3C2
Config Reg-2 Storage-5	B02	Config Reg-1 CE-1	B02
Gnd Return	D02	Gnd Return	D02
Config Reg-2 Storage-6	B03	Config Reg-1 CE-2	B03
Config Reg-2 Storage-7	D03	Config Reg-1 CE-3	D03
Config Reg-2 Storage-8	B04	Config Reg-1 CE-4	B04
Config Reg-2 Storage-9	D04	Config Reg-1 IOCE-1	D04
Config Reg-2 Storage-10	B05	Config Reg-1 IOCE-2	B05
Config Reg-2 Storage-11	D05	Config Reg-1 IOCE-3	D05
Config Reg-2 Storage-12	B06	Config Reg-1 Storage-1	B06
Config Reg-2 PAM-1	D06	Config Reg-1 Storage-2	D06
Gnd Return	B07	Gnd Return	B07
Config Reg-2 PAM-2	D07	Config Reg-1 Storage-3	D07
Config Reg-2 PAM-3	B08	Config Reg-1 Storage-4	B08
Gnd Return	D08	Gnd Return	D08
Config Reg-2 TCU-1	B09	Config Reg-1 Storage-5	B09
Config Reg-2 TCU-2	D09	Config Reg-1 Storage-6	D09
Config Reg-2 TCU-3	B10	Config Reg-1 Storage-7	B10
Config Reg-3 CE-1	D10	Config Reg-1 Storage-8	D10
Config Reg-3 CE-2	B11	Config Reg-1 Storage-9	B11
Config Reg-3 CE-3	D11	Config Reg-1 Storage-10	D11
Config Reg-3 CE-4	B12	Config Reg-1 Storage-11	B12
Config Reg-2 SCU-2	D12	Config Reg-1 SCU-1	D12
Gnd Return	B13	Gnd Return	B13
Config Reg-2 SCU-3	D13	Config Reg-1 SCU-2	D13
Config Reg-3 IOCE-1	G02	Config Reg-1 Storage-12	G02
Gnd Return	J02	Gnd Return	J02
Config Reg-3 IOCE-2	G03	Config Reg-1 PAM-1	G03
Config Reg-3 IOCE-3	J03	Config Reg-1 PAM-2	J03
Config Reg-3 Storage-1	G04	Config Reg-1 PAM-3	G04
Config Reg-3 Storage-2	J04	Config Reg-1 TCU-1	J04
Config Reg-3 Storage-3	G05	Config Reg-1 TCU-2	G05
Config Reg-3 Storage-4	J05	Config Reg-1 TCU-3	J05
Config Reg-3 Storage-5	G06	Config Reg-2 CE-1	G06
Config Reg-3 Storage-6	J06	Config Reg-2 CE-2	J06
Gnd Return	G07	Gnd Return	G07
Config Reg-3 Storage-7	J07	Config Reg-2 CE-3	J07
Config Reg-3 Storage-8	G08	Config Reg-2 CE-4	G08
Gnd Return	J08	Gnd Return	J08
Config Reg-3 Storage-9	G09	Config Reg-2 IOCE-1	G09
Config Reg-3 Storage-10	J09	Config Reg-2 IOCE-2	J09
Config Reg-3 Storage-11	G10	Config Reg-2 IOCE-3	G10
Config Reg-3 Storage-12	J10	Config Reg-2 Storage-1	J10
Config Reg-3 PAM-1	G11	Config Reg-2 Storage-2	G11
Config Reg-3 PAM-2	J11	Config Reg-2 Storage-3	J11
Config Reg-3 PAM-3	G12	Config Reg-2 Storage-4	G12
Config Reg-3 SCU-1	J12	Config Reg-1 SCU-3	J12
Gnd Return	G13	Gnd Return	G13
Config Reg-3 SCU-2	J13	Config Reg-2 SCU-1	J13

● Figure 3-14. SC to SMMC Interface Lines (Sheet 1 of 2)

Line Name	Pin	Line Name	Pin
	01S-S3E2		01S-S3B2
Config Reg-3 TCU-1	B02	Power Check CE-1	B02
Gnd Return	D02	Gnd Return	D02
Config Reg-3 TCU-2	B03	Power Check CE-2	B03
Config Reg-3 TCU-3	D03	Power Check CE-3	D03
Config Reg-4 CE-1	B04	Power Check CE-4	B04
Config Reg-4 CE-2	D04	Power Check IOCE-1	D04
Config Reg-4 CE-3	B05	Power Check IOCE-2	B05
Config Reg-4 CE-4	D05	Power Check IOCE-3	D05
Config Reg-4 IOCE-1	B06	Power Check Storage-1	B06
Config Reg-4 IOCE-2	D06	Power Check Storage-2	D06
Gnd Return	B07	Gnd Return	B07
Config Reg-4 IOCE-3	D07	Power Check Storage-3	D07
Config Reg-4 Storage-1	B08	Power Check Storage-4	B08
Gnd Return	D08	Gnd Return	D08
Config Reg-4 Storage-2	B09	Power Check Storage-5	B09
Config Reg-4 Storage-3	D09	Power Check Storage-6	D09
Config Reg-4 Storage-4	B10	Power Check Storage-7	B10
Config Reg-4 Storage-5	D10	Power Check Storage-8	D10
Config Reg-4 Storage-6	B11	Power Check Storage-9	B11
Config Reg-4 Storage-7	D11	Power Check Storage-10	D11
Config Reg-4 Storage-8	B12	Power Check Storage-11	B12
Config Reg-3 SCU-3	D12	Power Check Storage-12	D12
Gnd Return	B13	Gnd Return	B13
Config Reg-4 SCU-1	D13	Spare	D13
Config Reg-4 Storage-9	G02	Power Check PAM-1	G02
Gnd Return	J02	Gnd Return	J02
Config Reg-4 Storage-10	G03	Power Check PAM-2	G03
Config Reg-4 Storage-11	J03	Power Check PAM-3	J03
Config Reg-4 Storage-12	G04	Power Check TCU-1	G04
Config Reg-4 PAM-1	J04	Power Check TCU-2	J04
Config Reg-4 PAM-2	G05	Power Check TCU-3	G05
Config Reg-4 PAM-3	J05	Power Check SCU-1	J05
Config Reg-4 TCU-1	G06	Power Check SCU-2	G06
Config Reg-4 TCU-2	J06	Power Check SCU-3	J06
Gnd Return	G07	Gnd Return	G07
Config Reg-4 TCU-3	J07	Spare	J07
Mode Ind Alpha-A	G08	Spare	G08
Gnd Return	J08	Gnd Return	J08
Mode Ind Alpha-B	G09	Spare	G09
Mode Ind Alpha-C	J09	Spare	J09
Mode Ind Numeric-1	G10	Spare	G10
Mode Ind Numeric-2	J10	Spare	J10
Mode Ind Numeric-3	G11	Spare	G11
Mode Ind Numeric-4	J11	Spare	J11
Mode Ind Numeric-5	G12	Spare	G12
Mode Ind Numeric-6	J12	Config Reg-4 SCU-2	J12
Gnd Return	G13	Gnd Return	G13
Mode Ind Numeric-7	J13	Config Reg-4 SCU-3	J13

• Figure 3-14. SC to SMMC Interface Lines (Sheet 2 of 2)

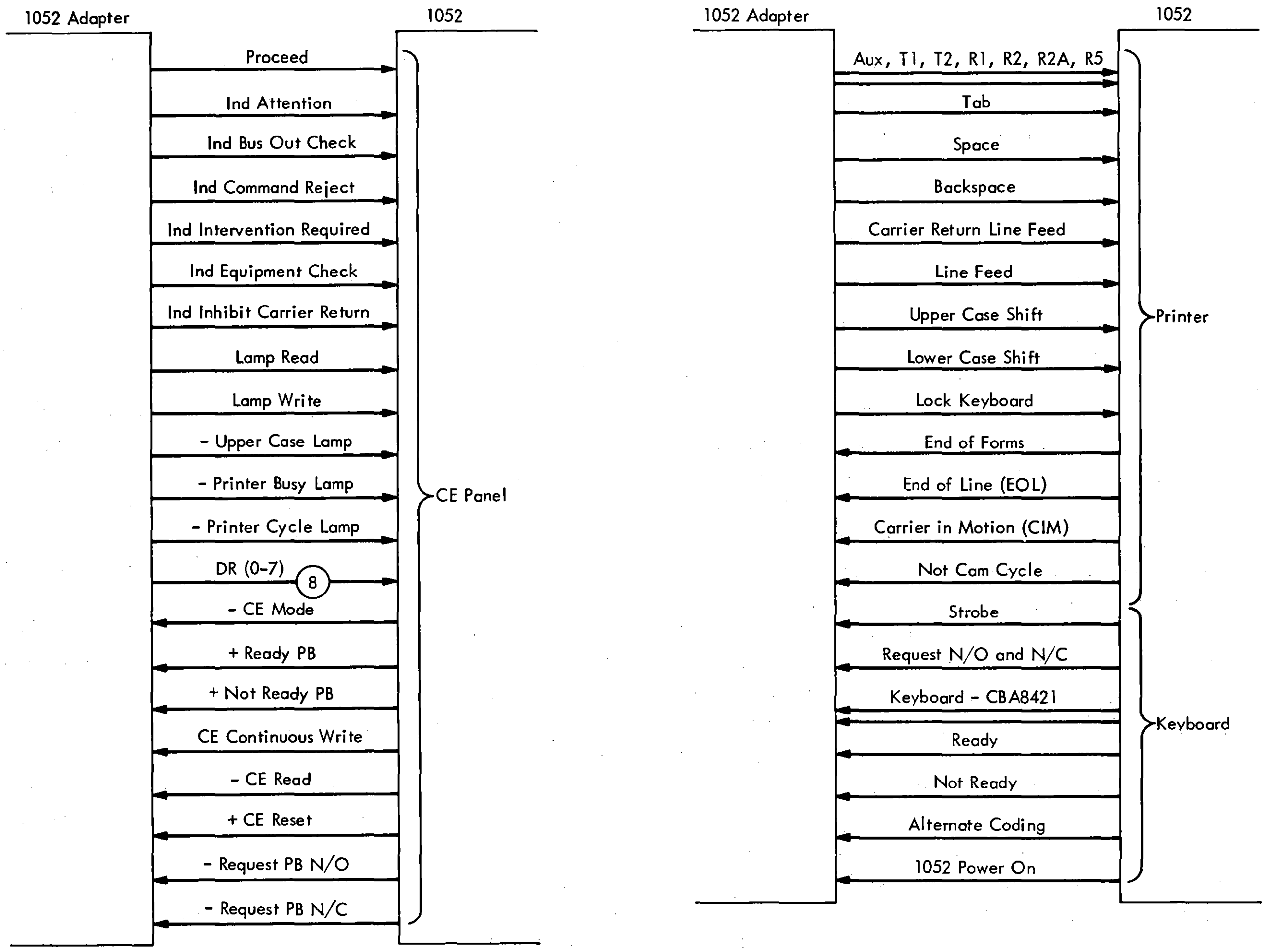


Figure 3-15. 1052 Adapter – 1052 Interface

The signal lines are tabulated below under I/O Interface Lines. Note that the names of the lines include the words "Out" or "In". In every case "Out" describes a line which transmits signals to the control units; "In" describes a line which transmits signals to the channel.

I/O Interface Lines

Name	Abbreviations
Bus Out Position P	Bus Out P
Bus Out Position 0	Bus Out 0
Bus Out Position 1	Bus Out 1
Bus Out Position 2	Bus Out 2
Bus Out Position 3	Bus Out 3
Bus Out Position 4	Bus Out 4
Bus Out Position 5	Bus Out 5
Bus Out Position 6	Bus Out 6
Bus Out Position 7	Bus Out 7
Bus In Position P	Bus In P
Bus In Position 0	Bus In 0
Bus In Position 1	Bus In 1
Bus In Position 2	Bus In 2
Bus In Position 3	Bus In 3
Bus In Position 4	Bus In 4
Bus In Position 5	Bus In 5
Bus In Position 6	Bus In 6
Bus In Position 7	Bus In 7
Address Out	Adr-Out
Address In	Adr-In
Command Out	Cmd-Out
Status In	Sta-In
Service Out	Srv-Out
Service In	Srv-In
Operational Out	Opl-Out
Operational In	Opl-In
Hold Out	Hld-Out
Select Out	Sel-Out
Select In	Sel-In
Suppress Out	Sup-Out
Request In	Req-In

Buses

Each bus is a set of nine lines consisting of eight information lines and one parity line. Unused lines must present logical zeros to the receiving end. The byte must always have odd parity.

Bus Out

Bus Out is used to transmit addresses, commands, control orders, and data to the control units. The type of information transmitted over Bus Out is indicated by the outbound tag lines:

1. When 'address out' is up during the channel initiated selection sequence, Bus Out specifies the address of the device which the channel wants to communicate.
2. When 'command out' is up during the channel initiated selection sequence, Bus Out specifies a command.
3. When 'service out' is up in response to 'service in' during execution of a write or control operation, the nature of the information on Bus Out depends upon the type of operation. For example, during a write operation it will contain data to be recorded by the device. During a control operation, it can specify an order code or a second-level address within the control unit or device.

The period during which information on Bus Out is valid is controlled by the tag lines. During transmission of the device address, information on the bus need be valid from the rise of 'address out' until the rise of 'operational in', 'select in', or, in the case of the control-unit-busy selection sequence, until 'status in' drops. When the channel is transmitting any other type of information, the information on Bus Out is valid from the rise of the signal on the associated outbound tag line until the fall of the signal on the corresponding inbound tag line.

Bus In

Bus In is used to transmit addresses, status, sense information, and data to the channel. A control unit can place and maintain information on Bus In only when its 'operational in' line is up, except in the case of the control-unit-busy sequence.

The type of information transmitted over Bus In is indicated by the inbound tag lines:

1. When 'address in' is up, Bus In specifies the address of the currently selected device.
2. When 'status in' is up, Bus In contains a byte of information describing the status of the device or control unit.
3. When 'service in' is up during execution of a read or sense operation, the nature of the information contained on Bus In depends upon the type of operation. During a read operation, it may contain a byte of data from the record medium. During a sense operation, the bus contains a set of bits describing the detailed status of the device and the conditions under which the last operation was terminated.

Tag Lines

The period during which information on the buses is valid is controlled by the tag lines. These are listed below together with a brief description of each.

Operational Out: This line, which runs from the channel to all attached control units, is used for interlocking purposes. Except for 'suppress out', all lines from the channel are significant only when 'operational out' is up. Whenever 'operation out' is down, all inbound lines from the control unit drop and any operation currently working over the interface is reset.

Request In: This line, which runs from all attached I/O control units to the channel, is used to signal the channel when any control unit has data or status to be serviced. 'Request in' can be signaled by more than one control unit at a time.

Address Out: This line, which runs from the channel to all attached control units, provides two functions:

1. Device selection. 'Address out' signals the control unit to decode the address on Bus Out.
2. Disconnect operations. If either 'select out' or 'hold out' is down and 'address out' is up, the presently connected control unit drops its 'operational in' line, thus disconnecting from the interface.

Select Out: This line extends from the channel to the control unit having higher priority and from any control unit to the control unit next lower in priority. This line, together with 'select in', provides a loop for scanning the attached control units.

Hold Out: This line, which extends from the channel to all attached I/O control units, is used to enable 'select out'. Only when 'hold out' is up can 'select out' be considered active. 'Hold out' gates the 'select out' signal in the control units. 'Hold out' can only be up if 'operation out' is up; for at least 4.0 usec. When used, 'hold out' minimizes the propagation of the fall of 'select out'.

Select In: This line extends 'select out' from the cable terminator block to the channel. It provides a return path (to the channel) for the 'select out' signal. The definition of 'select in' is the same as that for a select-out line emanating from any control unit.

Operational In: This line, which extends from all attached control units to the channel, is used to signal the channel that a device has been selected (except for the control-unit-busy sequence). The selected device is identified by the address byte transmitted over Bus In.

Address In: This line, which runs from all attached control units to the channel, is used to signal the channel that the address of the currently selected device has been placed on Bus In. The channel responds to 'address in' by means of 'command out'. The rise of 'address in' indicates that the address of the currently selected device is available on Bus In.

Command Out: This line, which runs from the channel to all attached control units, is used to signal the selected device in response to a signal on the 'address in', 'status in', or 'service in' line. A signal on the 'command out' line as a response to the 'address in' signal during the initial selection sequence indicates to the selected device that the channel has placed a command byte on Bus Out.

A command-out response to 'address in' means proceed, except during a channel-initiated selection sequence. In the case of a channel-initiated selection sequence, 'command out' indicates that Bus Out defines the operational command to be performed. A command-out response to 'service in' always means stop. A command-out response to 'status in' means stack.

When 'command out' is raised to indicate proceed, stack, or stop, Bus Out must have a command byte of zero, but need not necessarily have correct parity.

Status In: This line, running from all attached control units to the channel, is used to signal the channel when the selected device has placed status information on Bus In. The channel responds with either 'service out' or 'command out', depending upon whether it accepted the status.

Service Out: This line, which extends from the channel to all attached control units, is used to signal the selected device in recognition of a signal on 'service in' or 'status in'. A signal on 'service out' indicates to the selected device that the channel has accepted the information on Bus In or has provided on Bus Out the data requested by 'service in'.

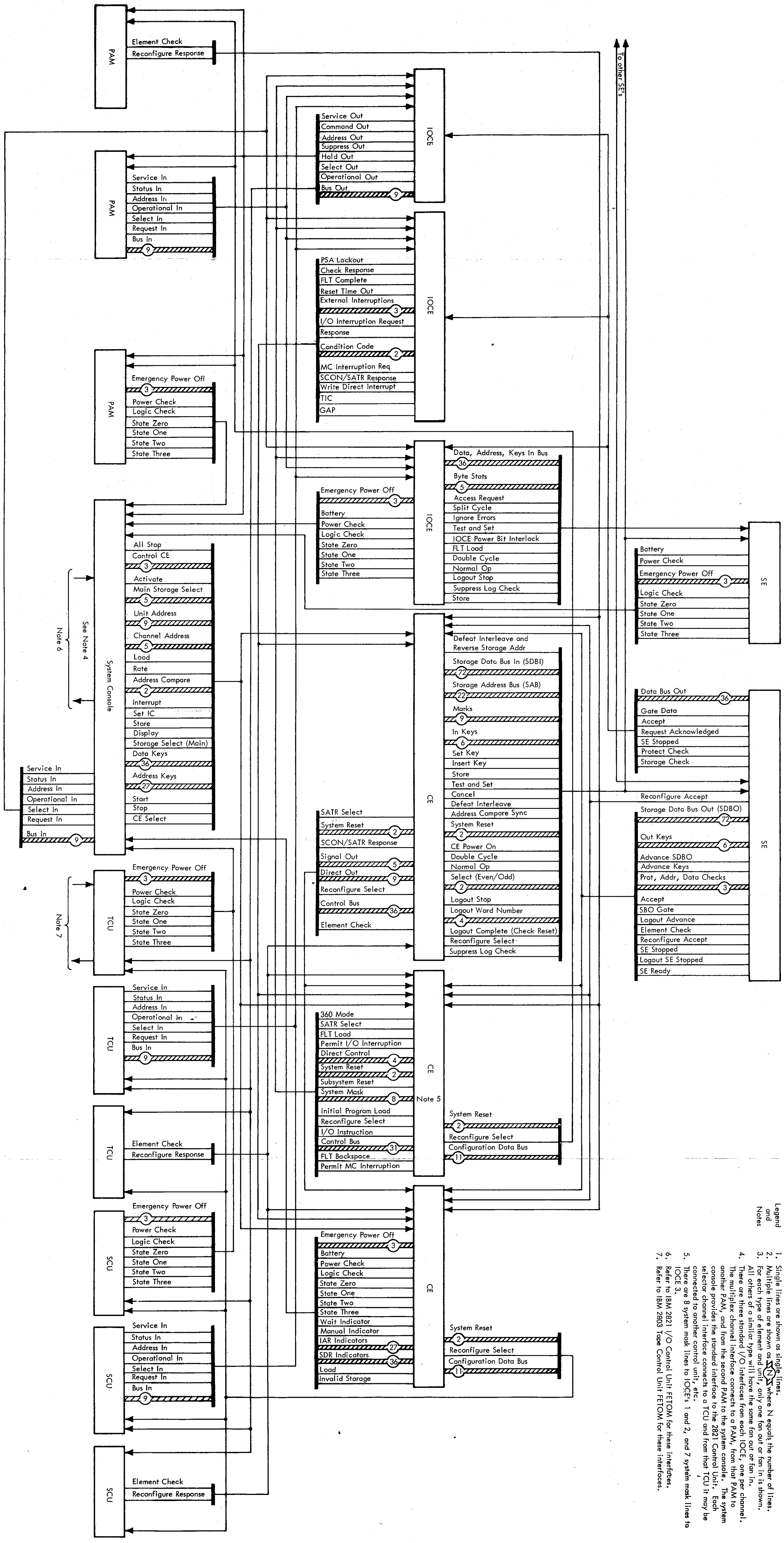
Service In: This line, which runs from all attached control units to the channel, is used to signal to the channel when the selected device wants to transmit or receive a byte of information. The nature of the information associated with 'service in' depends upon the operation and the device. The channel must respond to 'service in' by 'service out', 'command out', or, during an interface disconnect, by 'address out'.

During read, read backward, and sense operations, 'service in' rises when information is available on Bus In. During write and control operations, 'service in' rises when information is required on Bus out.

Suppress Out: This line, running from the channel to all attached control units, is used both alone and in conjunction with the out-tag lines to provide the following special functions: Suppress Data, Suppress Status, Command Chaining, and Selective Reset.

OVERALL INTERFACING

Figure 3-16 provides an overall view of the interfacing in the 9020D System. It has been placed at the end of the chapter and provided with a blank apron so that it can be folded out for reference as the chapter is read.



• Figure 3-16. 9020D Overall Interfacing

Legend and Notes

1. Single lines are shown as single lines.
2. Multiple lines are shown as (N) where N equals the number of lines.
3. For each type of element and unit, only one fan out or fan in is shown. All others of a similar type will have the same fan out or fan in.
4. There are three standard I/O interfaces from each IOCE, one per channel. The multiplex channel interface connects to a PAM, from that PAM to another PAM, and from the second PAM to the system console. The system console provides the standard interface to the 2821 Control Unit. Each selector channel interface connects to a TCU and from that TCU it may be connected to another control unit, etc.
5. There are 8 system mask lines to IOCE's 1 and 2, and 7 system mask lines to IOCE 3.
6. Refer to IBM 2821 I/O Control Unit FETOM for these interfaces.
7. Refer to IBM 2803 Tape Control Unit FETOM for these interfaces.

- Reconfiguration under EXC program control.

- 9020D system may have two or more independent configurations.

- SCON instruction used to configure major elements.

The 9020 system is unique in its ability to be reconfigured dynamically under program control. This capability enables the executive control (EXC) program to respond to a change in tasks or workload by restructuring the system into a more appropriate configuration. Further, a malfunctioning element may be automatically replaced with a redundant element while the ATC task continues.

Certain requirements imposed on the system when forming subsystem configurations are briefly summarized:

1. When units of the 9020D system are actively engaged in performing the ATC operational task, other units not so engaged, or malfunctioning units, must not be permitted to interfere destructively.
2. If units of the 9020D system are not required for the operational task, they should be available for auxiliary tasks or maintenance.
3. Those units of the 9020D system which are not actually malfunctioning or undergoing maintenance should be immediately available to the EXC program to perform the operational task, regardless of their current auxiliary tasks.
4. Units requiring maintenance must be provided with adequate maintenance facilities and effective isolation from the remainder of the operational system.

In the 9020D system there is no inherent master/slave relationship which requires that a specific computing element (CE) have primary control. Any one of the available CEs may be assigned a particular task. Nothing logically distinguishes one CE from another except the load identity (LDI) instruction.

The overall system with its various system elements may be configured into two or more different and independent subsystems for performing necessary tasks. This function of system configuration is under control of the EXC program. It is therefore the responsibility of the EXC program to specify the permissible communications paths between major elements for any given configuration. That is, the EXC program must specify to each major element those other elements to which it can transfer data and from which it can receive data. In addition to specifying data paths, the EXC program must specify to each major element the CE (or CEs) from which it may accept configuration control. Two separate controllable paths are provided for data and configuration information flow between elements.

The ability of the 9020D system to function as two or more subsystems under control of the EXC program is further facilitated by the existence of four operational states in each element. Each major element can assume one of the four possible element states at any given time. The state establishes the degree of availability of the element to the EXC program and the extent of the manual control which operating and maintenance personnel are permitted over the element. Here again the responsibility for assigning the state of each element rests with the EXC program and is part of the configuration control structure of the system.

The primary means of configuration control is via the set of configuration (SCON) instruction. This instruction and the associated hardware enable a CE to establish the configuration of all the major elements in the system. The elements which are included in the primary configuration control structure of the 9020D system are:

1. Computing Elements (CEs)
2. I/O Control Elements (IOCEs)
3. Storage Elements (SEs)
4. Peripheral Adapter Modules (PAMs)
5. Tape Control Units (TCUs)
6. Storage Control Units (SCUs)

These six element types are considered to be major elements of the 9020D system.

SET CONFIGURATION INSTRUCTION (SCON)

- RR format.

- Establishes system configuration.

The Set Configuration (SCON) instruction is the programming means by which the 9020 may be configured into the desired system configurations. The SCON instruction, by means of configuration mask and selection mask located in general purpose registers, establishes the system configuration by specifying to the system elements:

1. The state they are to assume.

2. The CEs from which they can accept future reconfigurations.
3. The system elements from which they are to receive data and control information.

Because the SCON instruction is a vital part of configuration control, many tests, both hardware and program, are made to ascertain that it can be legally issued by a given CE and accepted by other system elements.

Three conditions imposed on the SCON instruction:

1. The SCON instruction can be issued by a CE only when it is in supervisory state. If SCON is attempted in the problem state, a "privileged" interruption results.
2. The SCON instruction can be issued by a CE only when it is in element state three or zero. If SCON is attempted in states two or one, a "specification" interruption results.
3. The SCON instruction must configure a system element so that element will accept a SCON instruction from at least one CE. An automatic check is made to insure this condition and, if the condition is not met, a "specification" interruption occurs.

Configuration Mask

- Specified by R1 of SCON instruction.
- Contains configuration data for selected elements.

The configuration mask [Figure 4-1(a)] is made available to the SCON instruction from the general purpose register specified by R1. The mask is loaded by the SCON instruction into the configuration control register (CCR) of the selected major elements (elements specified in the selection mask). The configuration mask can contain sufficient configuration data for any type of element; however, in most cases only the necessary portions of the mask are sent to the receiving element. The SEs are the exceptions; the complete mask is transmitted to them via the Storage Data Bus In (SDBI). SEs gate in only the required fields. Configuration data sent over the SDBI is in a different format from that of the configuration mask. This is shown in Figure 4-2. Figure 4-3 shows the CCR formats for the major system elements.

Each element selected to receive the SCON checks the data for correct parity and for any other conditions which may make the data invalid for that element. If the configuration data is accepted by the element, it responds to the issuing CE. The response resets the element's bit in the select mask, indicating to the issuing CE that the SCON was accepted. At the completion of the execution of the SCON instruction, the condition code is set to 0 if all elements respond and to 2 if one or more do not respond.

Selection Mask

- Specified by R2 of SCON instruction.
- Designates elements to receive configuration mask.

The selection mask [Figure 4-1(b)] is made available to the SCON instruction from the general purpose register specified by R2. This mask designates the elements to receive the configuration bits contained in the configuration mask issued by the SCON instruction. Multiple CCRs may be set with one SCON instruction when identical masks are to be used in each receiving element.

(a) Configuration Mask

State		SCON						SE												CE									IOCE			
S0	S1	1	2	3	4	ILOS	*	1	2	3	4	5	6	7	8	9	10	*	*	1	2	3	4	*	*	*	*	*	1	2	3	
0	1	2			5	6	7	8									17	18	19	20			23	24				28	29		31	32 … 63

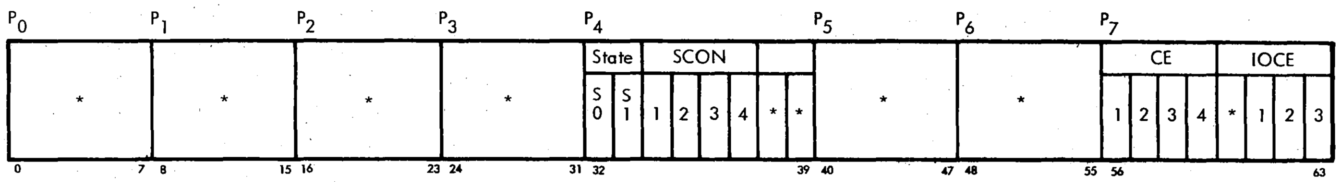
(b) Selection Mask

PAM			TCU					SE												CE				SCU					IOCE		
1	2	3	1	2	3	*	*	1	2	3	4	5	6	7	8	9	10	*	*	1	2	3	4	1	2	3	*	*	1	2	3
0		2	3		5	6	7	8									17	18	19	20			23	24				28	29		31

Notes:

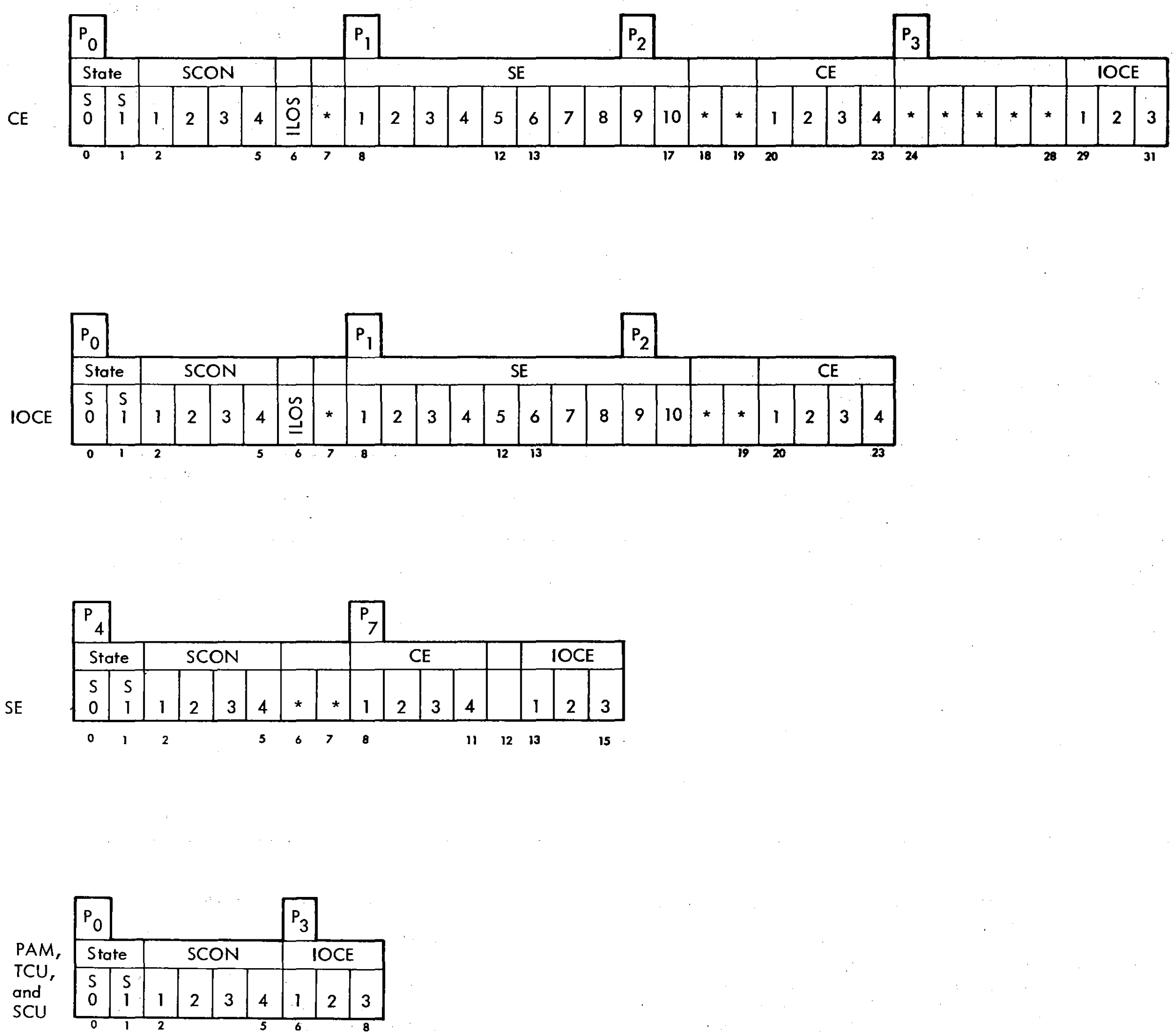
1. * Denotes unused bits which may be zero or one.
2. Maximum configuration is assumed. For lesser systems, any bits not required become spares.

● Figure 4-1. Configuration Mask and Selection Mask Formats



* Denotes unused bits which may be zero or one.

Figure 4-2. SDBI Configuration Data Format



Note: The maximum configuration is assumed. For lesser systems, those bits not required become spares.

Legend:
* Unused bits (may be one or zero).

● Figure 4-3. 9020D Configuration Control Register Formats

CONFIGURATION CONTROL REGISTER (CCR)

- Physical register in each major element.
- Set by SCON instruction.

The CCR is a physical register in each of the major system elements. The CCR is set by a SCON instruction executed by a CE. The CCR in each major system element consists of a state field, SCON field, and a communications field. These fields contain the information necessary to establish the state of the element, the CEs from which it will accept future SCONs, and the other system elements from which it may receive data. Additionally, an inhibit logout-stop (ILOS) bit is contained in each CE and IOCE. Because of the various functions of the system elements, there are differences in the format of their respective CCRs. The CCR format for each of the system elements is shown in Figure 4-3 and each field is described in the following paragraphs.

System Element States

- Four possible states.
- Specified by CCR (0, 1).

Each major system element of the 9020 can be in one of four states. The EXC program establishes these states by setting the state field via a SCON instruction. The state of an element determines the degree of manual control which maintenance or operating personnel may exercise over it. For example, in state 0 (the lowest operational state), virtually all element controls are operational so that maintenance may be performed on the element. Further, by placing the element in Test mode, the ATC system will be denied use of the element completely. In state 3 (the highest operational state), virtually all manual controls are disabled so that the element can operate in the ATC system without interference. From the larger point of view, element state may be looked upon as the element's degree of availability to the ATC task and is, therefore, closely related to the element's immediate role in the system. Figure 4-4 shows an analysis of the effect on element operation for each of the four CE states. Details for each of the other elements are contained in their respective theory manuals.

State Three

- Highest operational state.
- CCR (0, 1) = 1, 1.

	State Bits		Issue SCON[1]	Accept SCON	CE ELC Maskable[6]	Element Controls[7]	Maintenance Controls	System Console Controls	Power and CCR Controls
	S0	S1							
Three	1	1	Yes	Yes[3]	Yes	No	No	Yes[9]	No
Two	1	0	No[2]	Yes[3]	No	No	No	Yes[9]	No
One	0	1	No[2]	Yes[3]	No	Yes	No	Yes[9]	No
Zero TEST Switch Off	0	0	Yes	Yes[3]	No	Yes	No[8]	Yes[9]	No
Zero TEST Switch ON	0	0	Yes[4]	No[5]	Yes	Yes	Yes	No	Yes

Notes:

1. Where Yes is entered, it implies a legal or permissive ability to issue SCON. The issuing CE must have its own SCON bit set and meet all other SCON restrictions.
2. If a CE attempts SCON, a specification check interruption will result. No signals will issue to other elements.
3. Receiving element must have proper SCON bit set.
4. When switch is ON, SCON will not affect any external element. The issuing CE may accept SCON from itself. When TEST switch is ON, it will be possible for a CE to have its state bits changed manually. If the state bits are changed from 00 to 11, SCON may be exercised by the CE, but no element except the issuing CE will respond. If the state bits are changed to 10 or 01, Note 2 applies.
5. SCONs will be rejected regardless of CCR, except that a CE may accept SCON from itself if it has its own SCON bit set.
6. This column applies to receiving CEs. Incoming CE ELCs are masked by SCON bits in receiving CEs. Where Yes is entered, the ELC may also be masked by normal interruption mask controls. Where No is entered, no further masking is possible.
7. These include: LOAD (IPL), INTERRUPT, STORE, DISPLAY, RATE switch, ADDRESS COMPARE, PSW RESTART, SET IC, START, STOP, 360 MODE switch.
8. Maintenance controls are generally disabled except where other truth tables indicate exceptions.
9. System Console SYSTEM INTERLOCK switch ON.

Figure 4-4. Summary of State Definitions

If a major system element is designated as being in state three by the EXC program, the element is presumed to be at the highest operational capability level. Normally the ATC operational task would be run in this state. A CE in state three has the ability to initiate reconfiguration of the existing system structure, subject to the information and control paths established by the EXC program.

State Two

- Capable of being recalled to state three.

- CCR (0, 1) = 1, 0.

A major system element designated by the EXC program as being in state two is considered free of malfunctions and completely capable of performing the ATC operational task, except that a CE in this state cannot initiate a system reconfiguration.

While in state two, a major system element might be employed in performing subsidiary tasks, but it is capable of being immediately recalled by the EXC program to assist other units in an operational task or to replace a malfunctioning unit. It is assumed that any subsidiary programs run while in state two will be debugged and under tight monitor control.

The EXC program may designate a CE as recallable by properly setting the SCON field of that element's CCR. (Refer to "CCR SCON Field.") If a CE has been designated by the EXC program to be recallable, it will automatically interrupt its current tasks and go to state three when certain check signals are received from other CEs.

State One

- Capable of being recalled to state three.

- Certain manual controls enabled.

- CCR (0, 1) = 0, 1.

State one may be considered to be a "quasi-redundant" state. When in state one, an element may be designated as recallable by the EXC program. However, certain operator manual controls are enabled to provide the necessary manual intervention to debug programs and run diagnostic programs. Thus, this state permits a non-malfunctioning unit to be used for various tasks which are not sufficiently predictable to be run in state two with its tight monitor control, yet remain available to the EXC program for operational use.

As in state two, a CE in state one, when designated as recallable, will automatically terminate its current task and go to state three upon receipt of certain check signals from other CEs.

State Zero

- Two substates.

- Useful for subsystem testing.

- Manual controls active.

- Capable of being recalled to state three if test switch is off.

- CCR (0, 1) = 0, 0.

The zero state has been provided to accommodate the maintenance needs of the 9020 system. The zero state is actually composed of two substates which are selected by a test switch.

With the test switch off, the zero state is considered primarily useful for subsystem testing. All manual controls, except those governing the manual setting of CCRs and those which turn off element power, are enabled. An element may, however, be recalled by the EXC program if it has been designated as recallable. If so designated, a CE will go to state three upon receipt of certain check signals from other CEs. Effective subsystem isolation can be retained in this mode if desired. Care must be exercised when in state zero with the test switch off, due to the availability of all manual intervention capabilities of the system. It is assumed that a system performing the ATC task will protect itself, via configuration control, from spurious signals generated by a subsystem under test.

When in state zero with the test switch on, the element is isolated from the remainder of the system to the extent required for its standalone or unit-test operations to be used. In the case of the PAM, SCU, TCU, and SE, this is a blanket isolation; i.e., all system interfaces are closed. For the CE and IOCE, this isolation is primarily achieved by refusing to accept the SCON instruction. Complete isolation is not desirable for these two elements. In this substate, all manual controls including power and manual CCR controls are active. To preclude loss of switch control, the state bits of each element will be reset to 00 whenever the test switch is turned off after having been in the on position.

CCR SCON Field

- Allows reconfiguration from system CEs.

The SCON field, CCR (2–5), in the various system elements is primarily associated with the execution and acceptance of SCON instructions. These positions enable the element to respond to a reconfiguration from one or more specified CEs.

The EXC program has the responsibility of keeping track of the CEs which have the authority to reconfigure the system. This authority is indicated in each element's CCR and only CEs having the authority are allowed to alter the receiving element's CCR.

Figure 4-5 shows a SCON example where CE 1, IOCE 1, SE 1, and SE 2 can each be reconfigured only by CE 1. No other CEs within the system can reconfigure these elements.

If the SCON field is void of all bits, that particular element is unavailable to the system; i.e., can not be reconfigured. Therefore, as a programming precaution, each execution of a SCON instruction is checked to see that at least one bit is on in the SCON field of the configuration mask [Figure 4-1(a)]. If the field is all 0's, the instruction is not completed, and a specification interrupt occurs.

One other precaution is taken with the SCON field to prevent an element from being made unavailable to the system. If the SCON field should become set to all 0's due to maintenance operations in state zero or circuit failures, a special circuit bypasses normal SCON decoding and causes the field to appear set with all 1's.

As mentioned earlier, the EXC program can use the SCON field of a CE to make that CE automatically recallable. For example, suppose a CE in state one has in its CCR SCON field the SCON bit of a CE in the ATC system. Should the CE in the ATC system malfunction, the state one CE would be hardware-forced to state three and would take an external interrupt preparatory to taking over execution of the EXC program. This is further explained in Chapter 7.

CCR ILOS Field in CE and IOCE

- Inhibit logout stop.

No. 1
Storage Element

State		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	0	0	0

No. 2
Storage Element

State		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	1	0	0

No. 1
Computing Element

State		SCON			SE										CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3	1	2	3
1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

No. 1
I/O Control Element

State		SCON			SE										CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3
1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Figure 4-5. CCR Field Examples

- CCR position 6.

- Applicable to CEs and IOCEs.

The inhibit logout stop (ILOS) bit, CCR(6), is applicable only to CE/IOCE operations and controls the issuing of a logout stop signal by either CEs or IOCEs to SEs. This bit is set and reset according to the configuration mask and selection mask used with the particular SCON instruction.

If CCR(6) = 1, the CE/IOCE will not issue a logout stop signal to an SE. If CCR(6) = 0, a logout stop signal will be automatically issued to an SE when the SE has signaled storage checks.

The ILOS bit is intended primarily for malfunction recovery in systems or subsystems which contain only one SE. This bit is also set into CCR(6) of all CEs/IOCEs during a system initial program load operation.

CCR Communication Fields

- Establish interelement communication.

- Provide isolation from elements not in same subsystem.

CCR fields in each major element indicate the other major elements from which this element can receive data. In this manner, elements can be completely isolated into independent subsystems.

A communication bit, when set, enables the interface from the associated unit. In some cases this may involve only the control lines, and in other cases may also involve data lines. In the use of all interfaces, some control action is required before any data bus is examined. If this control action is inhibited, it is unnecessary to further degate the data bus since it will not be examined. Signals to the DAR, which enable CEs to monitor abnormal conditions in the various elements, are not gated by the CCR communication bits because it may be desirable to reconfigure elements without being required to accept other communications from them.

Figure 4-5 shows an example of the use of the communications fields in establishing interelement communications. In order for CE 1 to receive data from SE 2, CE 1 must have the corresponding SE 2 bit on in its CCR. The same SE 2 bit must also be on to allow CE 1 to initiate a storage request or data transmission to SE 2.

On the other end of the interface, SE 2 must have the corresponding CE 1 bit on in its CCR either to receive or send information from/to CE 1. From this example, we see that in order to establish complete communication between two elements, corresponding bits must be on in each of the two elements.

In this same example, IOCE 1 can also successfully communicate with SE 2. IOCE 1 may also initiate communication with SE 1, but SE 1 will not reply because there is no corresponding IOCE 1 bit to complete the interface connection. Being able to break the interface at both ends provides maximum isolation and minimum chance of unwanted interference from elements outside the active ATC system.

COMMUNICATION BIT RESTRICTIONS

Certain hardware and programming restrictions exist on the setting of bits in the communication fields of the CCRs of various elements. For example, it is not feasible to have more than one CE bit set in the CCR of an IOCE since the IOCE would then be unable to return interrupts to the correct CE. Refer to the 9020D/E Principles of Operation Manual for details.

ISOLATION OF MALFUNCTIONING ELEMENTS

The error detection circuitry of the system provides protection from propagation of logic errors. The program may then use configuration control to isolate the malfunctioning unit for maintenance purposes.

Each power supply contains an overvoltage/overcurrent sensor, which when activated will turn the power off in that unit before damage occurs. Configuration control provides degating from other units with normal power status.

The circuitry which directly connects to a distributed simplex interface is designed so that the interface will not be disabled by commonly encountered component failures, unless, of course, the failure occurs in the primary element. The latter case is exemplified by a component failure in the drivers on the CE to 10 SE interfaces, while the former is exemplified by a component failure in an SE receiver in the same interface.

The circuitry which is directly connected to the I/O interface in the PAM, SCU, TCU and SC is designed so that power may be turned on and off in each of these units without disrupting any activity in the interface that does not concern that unit. Also, in the interfaces in the 9020D system of the type exemplified by that from a CE to 10 SEs, turning power on and off in an SE connected to that interface will not disrupt the interface operation. However, to prevent disrupting the activities of the SEs connected to that interface as a result of power being turned on and off in the CE, the SE's must be configured not to accept communications from that CE.

CONFIGURATION EXAMPLES

Two examples of system configuration are presented here which illustrate the use of the SCON instruction and show the resulting contents of the CCRs of the various system elements.

Configuration Example 1

Figure 4-6 shows an example of an ATC configuation. The figure shows simplified representations of the CCRs in the major elements of a typical system. In this example, one CE, one IOCE, four SEs, two PAMs, two TCUs, and one SCU are configured into the active system. The various conditions follow:

1. The state bits of each element in the ATC subsystem are set to state three (11). This is the highest state and the one in which the ATC functions are assumed to be performed.
2. The SCON bit in each element CCR is set to CE 1 so that future reconfigurations can be accomplished by CE 1.
3. In CE 1, the SE field of the CCR is set to allow CE 1 to listen to SEs 1–4. The IOCE field is set to listen to IOCE 1.
4. In IOCE 1, the SE field is set to allow IOCE 1 to listen to SEs 3 and 4, and the CE field is set to listen to CE 1.
5. Each configured SE has its CE bits set to listen to CE 1; SEs 3 and 4 are also set to listen to IOCE 1.
6. Both the configured PAMs and TCUs are set to listen to IOCE 1. In this example, CE 1 may communicate with IOCE 1 and SEs 1–4.
7. SCU 1 is set to listen to IOCE 1.

With its own SCON bit on, and being in state three, CE 1 may execute the SCON instruction and reconfigure the system when necessary.

The SEs are set up so that CE 1 has access to all four while the IOCE is restricted to SEs 3 and 4. This provides the CE with an area of storage free from interference by the IOCE.

Figure 4-7 shows how the configuration in this example could be established by three SCON instructions. Figure 4-7(a) shows the configuration mask and selection mask required for the first SCON instruction. With this first SCON instruction, CE 1 configures itself into state three with the ability to communicate with IOCE 1 and SEs 1–4.

Figure 4-7(b) shows the masks for the second SCON instruction. Here the PAMs, TCUs, SCUs, SEs 3 and 4, and IOCE 1 are selected. The configuration mask sets each element to state three with the SCON bit on to permit future reconfigurations by CE 1. Each selected element is also conditioned to communicate with CE 1. Note that in each of the above cases only the required configuration bits are transmitted to the respective elements. For example, the PAMs, TCUs, SCUs, and SEs do not receive SE bits; the PAMs, SCUs, and TCUs do not receive the CE bit.

Figure 4-7(c) shows the masks for the last SCON instruction. Here SE 1 and 2 are configured to state three with the ability to communicate with CE 1. Again the SCON 1 bit is set in SE 1 to permit future reconfigurations by CE 1.

Configuration Example 2

Figure 4-8 shows the 9020D system as Figure 4-6 but the unused elements of the system have been configured into two additional subsystems. These subsystems are:

Subsystem 2 - A state two subsystem composed of CE 2, IOCE 2, SEs 5, 6, and 7, SCU 2, and TCU 3.

Subsystem 3 - A state zero maintenance subsystem composed of CE 3, IOCE 3, SE 8, SCU 3, and PAM 3.

Each of these two subsystems is below the state three operational level. All of these associated elements are immediately recallable by CE 1 to the active ATC system if the need arises. In the maintenance subsystem, however, complete isolation can be achieved for any of the elements by setting the test switch on that element to the test position. In this state, the element cannot be taken from maintenance personnel without their permission. That is, maintenance personnel must take the element out of the test state before it can be recalled by the EXC program.

Note that these subsystems must be set up by the EXC program which is using CE 1 at this time. CE 1 is the only CE in state three, a state in which the SCON instruction may be executed. The SCON instruction can also be executed in state zero, but the EXC program normally protects the system from SCONs issued in this state by insuring that no active element has the SCON bit set in its CCR for a CE in state zero. Thus, no SCON issued by the state zero CE would be effective.

Three SCON instructions [Figures 4-9(a) through 4-9(c)] can establish subsystem 2 while the maintenance subsystem requires only one SCON instruction [Figure 4-9(d)].

Figure 4-9(a) shows the masks for the SCON instruction which configure CE 2 into state two with the ability to communicate with IOCE 2 and SEs 5, 6, and 7. Note that in CE 2, as well as in all of the other subsystem elements, the SCON field is set to CE 1. This condition allows these elements to accept new SCON reconfigurations from CE 1.

Figure 4-9(b) shows the configuration of IOCE 2, SE 7, SCU 2, and TCU 3 into state two. IOCE 2 is configured to CE 2 and SE 7; SE 7 is configured to CE 2 and IOCE 2; TCU 3 and SCU 2 are configured to IOCE 2. Again, only the applicable bits in the configuration mask are transmitted to the selected elements.

Figure 4-9(c) shows the completion of the state two subsystem configuration. SEs 5 and 6 are set to state two with communication abilities with CE 2.

Figure 4-9(d) shows the masks for the SCON instruction which completely configures the state zero maintenance subsystem (CE 3, IOCE 3, PAM 3, SCU 3, and SE 8). If the test switch is not turned on in these elements after reconfiguration, CE 1 can recall them to the active system or reconfigure them to another subsystem as needed.

No. 1 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	0	0	0

No. 2 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	0	0	0

No. 3 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	1	0	0

No. 4 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	1	0	0

No. 5 Storage Element

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
0	0	0	0	0	0	0	0	0	0	0

No. 6 Storage Element

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
0	0	0	0	0	0	0	0	0	0	0

No. 7 Storage Element

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
0	0	0	0	0	0	0	0	0	0	0

No. 8 Storage Element

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
0	0	0	0	0	0	0	0	0	0	0

No. 1 Computing Element ●

		SCON			SE								CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0

No. 2 Computing Element

		SCON			SE								CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

No. 3 Computing Element

		SCON			SE								CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

No. 1 I/O Control Element ●

		SCON			SE								CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	0

No. 2 I/O Control Element

		SCON			SE								CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

No. 3 I/O Control Element

		SCON			SE								CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

No. 1 PAM ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 2 PAM ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 3 PAM

		SCON			IOCE		
S	S	1	2	3	1	2	3
0	0	0	0	0	0	0	0

No. 1 TCU ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 2 TCU ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 3 TCU

		SCON			IOCE		
S	S	1	2	3	1	2	3
0	0	0	0	0	0	0	0

No. 1 SCU ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 2 SCU

		SCON			IOCE		
S	S	1	2	3	1	2	3
0	0	0	0	0	0	0	0

No. 3 SCU

		SCON			IOCE		
S	S	1	2	3	1	2	3
0	0	0	0	0	0	0	0

Legend:

● State Three ATC Subsystem

● Figure 4-6. Configuration Example No. 1

Configuration Mask

		SCON						SE												CE									IOCE		
S	S	1	2	3	4	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	*	*	*	*	*	1	2	3
1	1	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Selection Mask

PAM			TCU					SE												CE				SCU					IOCE		
1	2	3	1	2	3	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	1	2	3	*	*	1	2	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

(a)

Configuration Mask

		SCON						SE												CE									IOCE		
S	S	1	2	3	4	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	*	*	*	*	*	1	2	3
1	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0

Selection Mask

PAM			TCU					SE												CE				SCU					IOCE		
1	2	3	1	2	3	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	1	2	3	*	*	1	2	3
1	1	0	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0

(b)

Configuration Mask

		SCON						SE												CE									IOCE		
S	S	1	2	3	4	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	*	*	*	*	*	1	2	3
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Selection Mask

PAM			TCU					SE												CE				SCU					IOCE		
1	2	3	1	2	3	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	1	2	3	*	*	1	2	3
0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(c)

● Figure 4-7. SCON Instructions for Configuration Example No. 1

No. 1 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	0	0	0

No. 2 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	0	0	0

No. 3 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	1	0	0

No. 4 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	1	0	0

No. 5 Storage Element ■

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	0	1	0	0	0	1	0	0	0	0

No. 6 Storage Element ■

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	0	1	0	0	0	1	0	0	0	0

No. 7 Storage Element ■

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	0	1	0	0	0	1	0	0	1	0

No. 8 Storage Element ⊠

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
0	0	1	0	0	0	0	1	0	0	1

No. 1 Computing Element ●

		SCON			SE								CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0

No. 2 Computing Element ■

		SCON			SE								CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
1	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0

No. 3 Computing Element ⊠

		SCON			SE								CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1

No. 1 I/O Control Element ●

		SCON			SE								CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	0

No. 2 I/O Control Element ■

		SCON			SE								CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
1	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0

No. 3 I/O Control Element ⊠

		SCON			SE								CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1

No. 1 PAM ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 2 PAM ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 3 PAM ⊠

		SCON			IOCE		
S	S	1	2	3	1	2	3
0	0	1	0	0	0	0	1

No. 1 TCU ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 2 TCU ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 3 TCU ■

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	0	1	0	0	0	1	0

No. 1 SCU ●

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	1	1	0	0	1	0	0

No. 2 SCU ■

		SCON			IOCE		
S	S	1	2	3	1	2	3
1	0	1	0	0	0	1	0

No. 3 SCU ⊠

		SCON			IOCE		
S	S	1	2	3	1	2	3
0	0	1	0	0	0	0	1

Lègend:

- ● State Three ATC Subsystem
- ■ State Two Subsystem
- ⊠ State Zero Maintenance Subsystem

● Figure 4-8. Configuration Example No. 2

Configuration Mask																															
		SCON						SE												CE									IOCE		
S	S	1	2	3	4	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	*	*	*	*	*	1	2	3
1	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Selection Mask																															
PAM			TCU					SE												CE				SCU					IOCE		
1	2	3	1	2	3	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	1	2	3	*	*	1	2	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

(a)

Configuration Mask																															
		SCON						SE												CE									IOCE		
S	S	1	2	3	4	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	*	*	*	*	*	1	2	3
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Selection Mask																															
PAM			TCU					SE												CE				SCU					IOCE		
1	2	3	1	2	3	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	1	2	3	*	*	1	2	3
0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

(b)

Configuration Mask																															
		SCON						SE												CE									IOCE		
S	S	1	2	3	4	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	*	*	*	*	*	1	2	3
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Selection Mask																															
PAM			TCU					SE												CE				SCU					IOCE		
1	2	3	1	2	3	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	1	2	3	*	*	1	2	3
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(c)

Configuration Mask																															
		SCON						SE												CE									IOCE		
S	S	1	2	3	4	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	*	*	*	*	*	1	2	3
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Selection Mask																															
PAM			TCU					SE												CE				SCU					IOCE		
1	2	3	1	2	3	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	1	2	3	*	*	1	2	3
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1

(d)

• Figure 4-9. SCON Instructions for Configuration Example No. 2

- Maximum of 10 SEs on 9020D system.
- Shared by 4 CEs and 3 IOCEs.
- Storage protection in SEs.
- Additional storage internal to each IOCE.

Main storage in the 9020D system consists of a maximum of ten IBM 7251-09 Storage Elements (SEs), each of which is a self-contained, self-powered unit capable of storing 524,288 bytes of data. With all ten SEs installed on the system, storage is provided for approximately 5-1/4 million individually addressable bytes.

Each of the five storage elements can be accessed by four CEs and three IOCEs. Data is transferred to and from CEs in doublewords (eight bytes) and to and from IOCEs in words (four bytes). The SEs have a faster storage cycle than IOCEs. The SE has a basic storage cycle time of 800 ns but can provide a doubleword every 400 ns if accesses are to alternate even and odd doublewords. This matches the speed of the CEs. The IOCE allows 2.5 usec for a storage cycle, however. For this reason, the SE is designed to provide its shorter cycle during the optimum portion of the IOCE cycle. This optimum time is different from store and fetch operations since it is dependent upon the time that data is available to and from the IOCE.

The faster effective storage access time achieved when accesses are to alternate even and odd doublewords is due to storage interleaving which is discussed in detail later in this chapter.

Each SE is equipped with storage protection (including fetch protection) to guard against the accidental destroying of data in storage. To accomplish this storage protection divides each SE into blocks of 2,048 bytes each, the start of each block being at multiples of 2048.

Associated with each of the storage blocks is a five-bit storage key which is contained in a magnetic core storage array. The four high-order (leftmost) bits represent the storage key, while the remaining low-order bit indicates whether fetch protection is to be enforced. Storage protection has no bit assigned as for fetch protection, and is always active except for times when the keys are zero.

A corresponding four-bit protection key is contained in either the current PSW for CE operations or in the channel address word (CAW) for channel operations. During a store operation, for example the four-bit storage key pertaining to the storage address is compared with the four-bit protection key supplied by the accessing element. The comparison results in either a match or mismatch as in the following:

Protection Key	Storage Key	Condition
X	X	Match
X	Y	Mismatch
X	Zero	Match
Zero	X	Match
Zero	Zero	Match

(Where X and Y are not equal to zero)

A match condition allows the store operation to proceed; a mismatch causes the addressed location to remain unchanged and a 'protect check' signal to be returned to the accessing element.

During a fetch operation, the fetch (low-order) bit of the storage key is examined. If a 1-bit, the four high-order storage key bits are compared with the four incoming protection key bits. A successful match condition allows the data to be sent to the accessing element; a mismatch prevents the stored data from being loaded into an addressable register or moved to another storage location, and a 'protect check' signal is returned to the accessing element.

Note that in the 9020 mode of operation, as mentioned above, a match occurs when both keys are equal or when either one is zero. In 360 mode, a match occurs when both keys are equal or when the protection key is zero.

The 9020D system has the capability of replacing a malfunctioning SE through reconfiguration. To provide this capability, each of the ten SE's may occupy any of the ten 524,288 byte blocks of storage addresses between zero and the maximum valid address, which is 5,242,879 (dec). To make possible this substitution of one SE for another, even though each SE responds only to its own block of fixed addresses, an address translation scheme is incorporated into the CEs and IOCEs. It involves the use of address translation registers (ATRs) in each CE and IOCE. The ATR's are set, under program control, according to the current structure, or configuration, of the system. Once address translation is established by the program, it is completely automatic. Accesses to a particular 524K byte area of storage are automatically directed to the SE which is currently occupying that area.

An elaboration of this address translation scheme permits the preferential storage area (PSA) for a particular CE to be located in any position in storage (on 4096 byte boundaries) and to be accessed automatically whenever a CE attempts to access an address smaller than 4096. This, too, is established under program control. It involves the use of preferential storage base address registers (PSBARs) in each CE and IOCE.

In addition to the storage provided by the SEs, each IOCE contains a 32K word storage unit which is used for maintenance and channel operations as well as for IOCE processor operation. The Maintenance And CHannel (MACH) storage unit in any IOCE can be accessed by that IOCE and by no other element. Therefore, the same address range exists in each IOCE. This range is above that of all main storage and is not contiguous with it.

Addresses within MACH begin at 12,582,912 (dec) or C0 00 00 (hex). Since there is no storage internal to the IOCE with address less than C00,000 (hex) it is simpler to look upon C0, 00, 00 (hex) as location zero in MACH. The two high-order bits may be thought of as an indicator enabling the IOCE and the programmer to distinguish which storage is intended, MACH or main.

As stated previously, the MACH storage in an IOCE is used for maintenance purposes when the IOCE is off line. Sufficient storage is available in MACH so that diagnostic programs may be run when no CE is available for a maintenance subsystem. In normal operation on line, however, MACH is used for channel and IOCE processor operation. The uppermost 4096 bytes of MACH are reserved for channel use in storing unit control words. The remainder of MACH storage is available to the IOCE processor. Under control of a CE, the IOCE processor may be assigned processing tasks to perform independently while the CE continues its own processing activity. The IOCE may access any configured main storage to which it has the proper key, as well as its own internal MACH storage. No other element, CE or IOCE, can access that IOCE's MACH storage, however, For this reason no storage protection is provided for MACH.

Figure 5-1 shows the total range of addresses available to the 9020D system with maximum SEs and IOCEs installed. Addresses are shown in both decimal and hexadecimal notation. The column headed "identifier" refers to the identifying character assigned to each SE to denote its particular fixed address range. This identifier is used in the address translation hardware to relate logical and physical addresses depending on the current program-established system configuration.

CE AND IOCE STORAGE ADDRESSING

- CEs and IOCEs access storage differently.
- SSU adapts SE to both CE and IOCE.

Since CEs and IOCEs access storage in different ways, certain background information must be kept in mind before storage addressing can be understood. CEs and IOCEs differ in the manner in which they access storage in five major respects:

1. The IOCE is slower than the CE.
2. The IOCE time shares a single bus with addresses, keys, and data while the CE has a separate bus for each.
3. The address format of the CE and IOCE are different.
4. The IOCE accesses a single word at a time while the CE accesses a doubleword (eight bytes).
5. The IOCE is not designed to operate directly with a "two-way data interleaved" SE as is the CE.

At the SE these five differences are reconciled by the Storage Switching Unit (SSU) portion of the SE. The SSU is also responsible for establishing the priority of requests from the attached IOCEs and CEs and for granting access to these elements according to those priorities. Beyond the SSU, in the storage section of the SE, accesses from both IOCEs and CEs appear the same as a result of the SSU's capability of adapting to both types of elements.

The SSU adapts to the first four major differences by storing the address, key, and data received from the IOCE in separate registers so that it will be available to the faster storage section at the appropriate time. At the same time, differences in format are reconciled. Figure 5-2 shows the address information as it is derived from the original address by the IOCE and the CE, each in its own way. A comparison is shown between address bits as they appear on the bus from the IOCE and on the Storage Address Bus (SAB) from the CE. In the SSU, the IOCE address information is preserved in a Storage Address Buffer Register (SABR). In the SABR the format is similar to that

Storage	Identifier	Address Range	
		Hexadecimal	Decimal
	1	00 00 00 - 07 FF FF	000,000 - 524,287
	2	08 00 00 - 0F FF FF	524,288 - 1,048,575
	3	10 00 00 - 17 FF FF	1,048,576 - 1,572,863
	4	18 00 00 - 1F FF FF	1,572,864 - 2,097,151
	5	20 00 00 - 27 FF FF	2,097,152 - 2,621,439
	6	28 00 00 - 2F FF FF	2,621,440 - 3,145,727
	7	30 00 00 - 37 FF FF	3,145,728 - 3,670,015
	8	38 00 00 - 3F FF FF	3,670,016 - 4,194,303
	9	40 00 00 - 47 FF FF	4,194,304 - 4,718,591
	A	48 00 00 - 4F FF FF	4,718,592 - 5,242,879
-	N/A		
*MACH	N/A	C0 00 00 - C1 FF FF	12,582,912 - 12,713,983

Legend: *The same address range exists in each IOCE. No confusion results from this because MACH is internal to each IOCE and cannot be accessed by any other element.

Note: Shaded area represents unused, therefore invalid, address range.

Figure 5-1. 9020D Storage Address Ranges

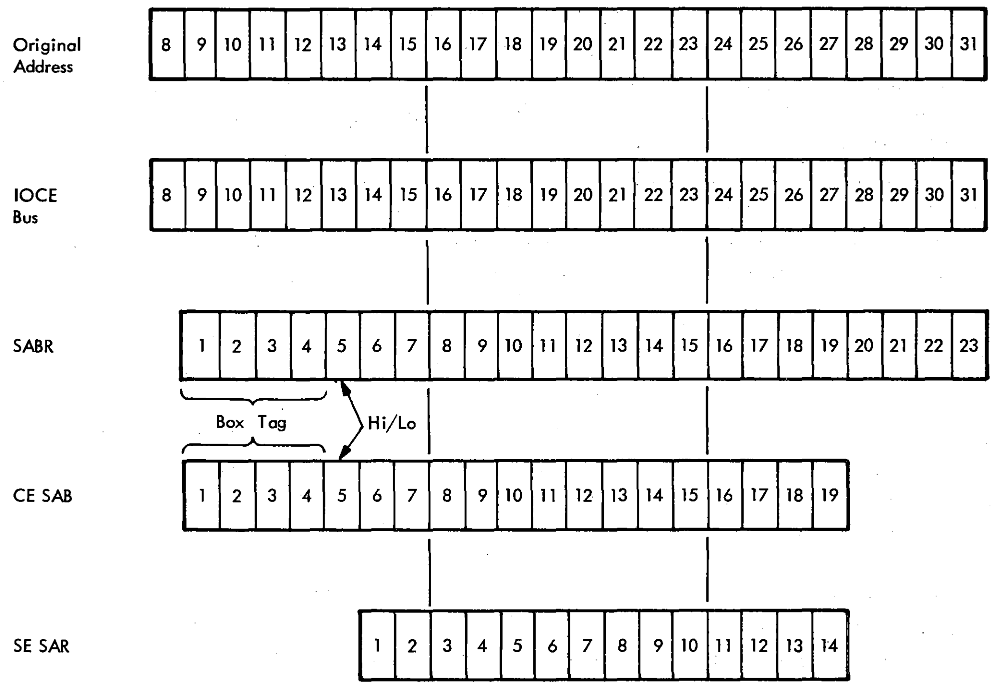


Figure 5-2. Storage Addressing Formats

of the CE SAB, the difference being that bits 20–23 (IOCE bus bits 28–31) are also preserved in SABR.

The fifth difference between the IOCE and CE involves storage interleaving. This is discussed later in this chapter. Again it is the SSU which reconciles the difference so that all accesses appear the same to the storage section of the SE.

Within the storage section, four Basic Storage Modules (BSMs) provide the actual storage capability of the SE. Each BSM has a separate Storage Address Register (SAR) which is usually called SE SAR to differentiate it from the SAR in an IOCE. Figure 5-2 also shows the format of the SARs. Note that the SAR bits are numbered differently from the SAB bits.

Because of the aforementioned differences in the IOCE and the CE, certain differences in nomenclature exist. The bus from the IOCE to the SE is referred to as the "IOCE data, address, keys-in" bus in discussions of the SSU. The address portion is referred to as the IOCE SAB within the SSU. At the IOCE, the bus in called the "Output Bus". Another difference in nomenclature exists with the mark bits that determine which bytes of data are to be stored and which are to be regenerated on a store cycle. At the IOCE these are called "Byte Stats" but at the SE they are called "IOCE Marks". There are four IOCE marks and eight CE marks in keeping with the fact that an IOCE operates on a word basis and a CE operates on a doubleword basis. During a store operation, the mark bits can be considered as part of the addressing scheme since, at that time, bytes must be individually addressable and the marks supply this individual addressing capability.

With this background information in mind, then, storage addressing may be discussed. To avoid confusion, all IOCE address bits are discussed as they appear in SABR. Refer to Figure 5-2 to find the IOCE bus bit corresponding to any SABR bit.

CE Accesses

- SCI synchronizes CE and SE operation.
- Only 19 address bits sent to SE on SAB.
- 1 parity bit sent on SAB and 2 parity bits sent on separate simplex lines.

When a storage access is to be made by a CE, the Storage Control Interface (SCI) portion of the CE generates the necessary signals to be transmitted to an SE. Since the machine cycle time is not directly related to storage speed, the SCI must also synchronize CE and SE operation.

Note that only 19 bits are transmitted over the CE SAB. Bit 0 is not required because it represents an address greater than the maximum available storage. Bits 21–23 are not required because they represent portions of a doubleword and a doubleword is the smallest amount of data which an SE can access. Bit 20 is not sent directly to the SE but is used at the CE for storage addressing as is shown later in the discussion of storage interleaving.

Special parity bits are generated for the SAB at the CE and again at the SE. The generated parity at the SE is then compared with the parity bits received from the CE.

The parity bits for CE SAB consist of P_T for bits 1–5, P_A for bits 6–12, and P_B for bits 13–19. P_T is sent along with the SAB bits, but P_A and P_B are sent on simplex lines to allow time for generating these special parity bits for the seven-bit groups: 6–12 and 13–19.

IOCE Accesses

- 24 address bits plus 3 parity bits sent to SE.

The IOCE transmits all three bytes of the address to the SE. Bit 8 of the IOCE bus is used only for parity checking. The remaining bits are set into SABR, as shown in Figure 5-2. These bits are used by the SSU portion of the SE to perform the same functions performed by the SCI in the CE. In addition, the SSU must examine the low-order bits (bits 21, 22, and 23) to determine which word of the doubleword is to be stored or fetched and to select the correct byte for a Test and Set instruction cycle.

Refer to the 7201-02 Theory of Operations Manual for details of SCI operation and to 7251-09 Theory of Operation Manual for details of SE operation.

SE Addressing Scheme

- SE dividend into even and odd areas.

- CE issues even or odd select signals.

For storage interleaving, the storage section of each SE is divided into an even half and an odd half. Each half consists primarily of two BSMs, high and low. This arrangement is shown in Figure 5-3. As will be shown subsequently, the addressing scheme for locating data within an SE may be altered by changing certain manual controls at the CE. However, to note that from the point of view of the SE there is only one addressing scheme; a given bit pattern on SAB and a given select signal specify one particular doubleword location within the SE.

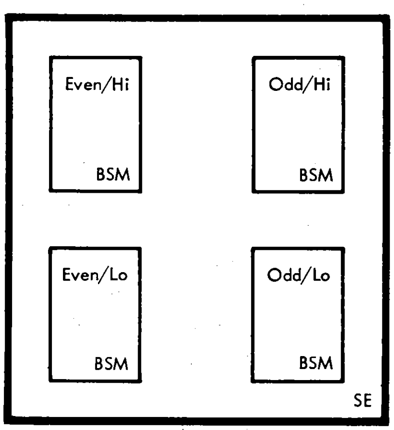


Figure 5-3. Even and Odd Basic Storage Modules

Figure 5-4 illustrates an example in which 'select even' and a SAB-bit pattern of 000 1000 0000 0000 0001 are received at the SE. The manner in which these signals specify a particular doubleword location is as follows:

1. The select signal determines whether the location is in an even or odd BSM pair.
2. Bits 1–4 select the SE originally and are sent to the SE only for verification that the correct SE was selected.
3. Bit 5 determines whether the doubleword is in a high or low BSM.
4. Bit 6 determines whether the doubleword is in the upper or lower half of a BSM. A zero specifies the lower half; a one specifies the upper half.
5. Bits 7–19 determine which doubleword location, within a particular BSM half, is to be accessed.

Thus, for the bit pattern and select signal shown, the SE accesses the doubleword shown by the cross-hatching.

Storage Interleaving

- Consecutive doublewords alternated between even and odd BSMs.

- CE can:
  1. Interleave.
  2. Defeat interleaving.
  3. Defeat interleaving and reverse storage addressing.

- IOCE does not interleave requests.

Storage Interleaving refers to the interleaving of data from different BSMs on the storage buses so that the buses may be used more efficiently. To accomplish this, a storage cycle in one BSM is started before the storage cycle in another BSM has been completed. Because storage common circuitry is not used by a BSM during the write half of the cycle, the read half of one BSM cycle may be overlapped with the write half of another BSM cycle. This provides a shorter effective access time.

Obviously, consecutive accesses to the same BSM cannot be overlapped. To decrease the probability that consecutive accesses will be to the same BSM, the normal addressing scheme is designed to place consecutive doublewords in different BSMs, thus permitting interleaving to occur. That is, even doublewords are placed in an even BSM and odd doublewords are placed in an odd BSM. Even and odd does not refer to addresses, since all doublewords have even

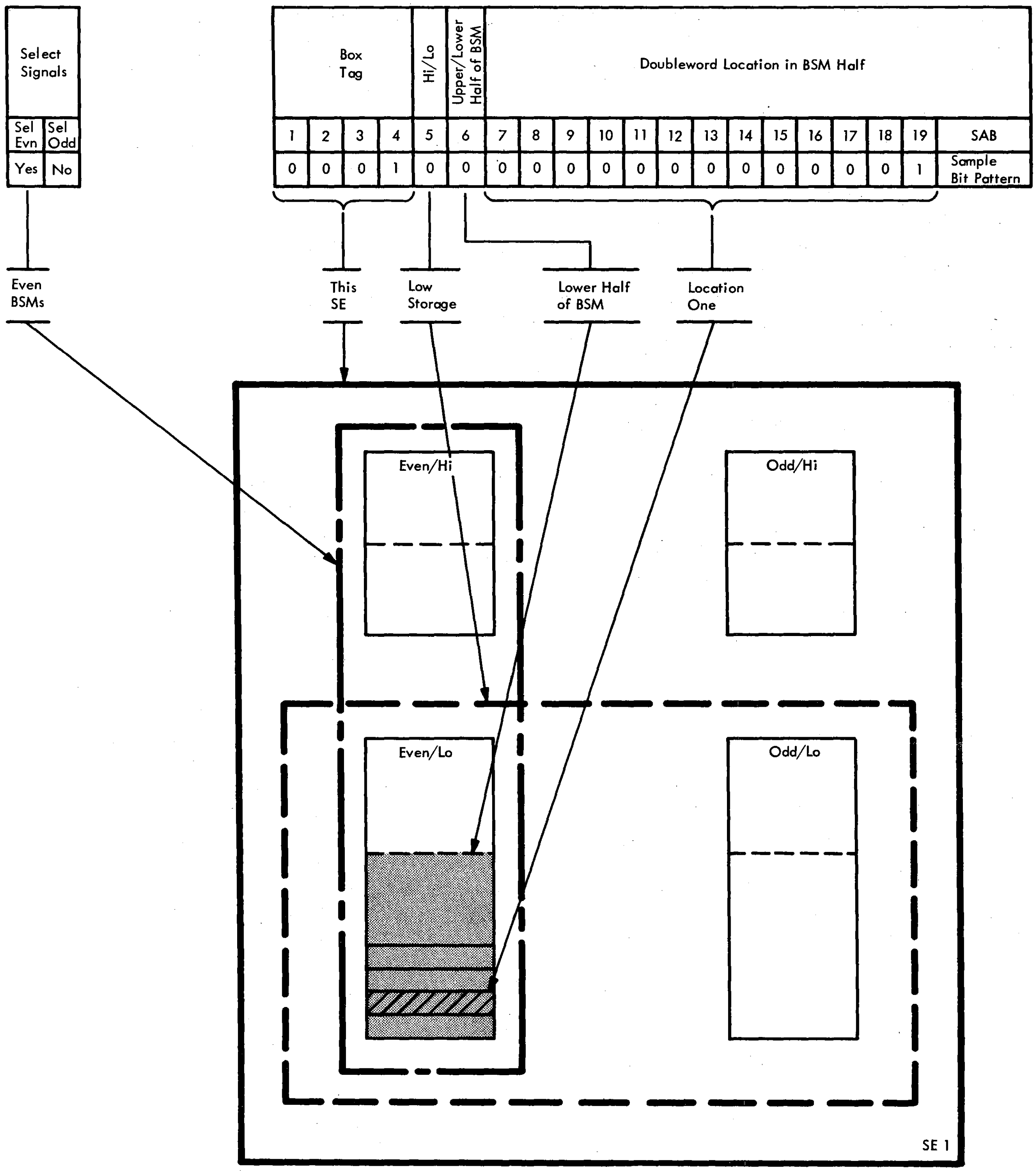


Figure 5-4. SE Doubleword Location Example

addresses. Figure 5-5 shows consecutive doublewords numbered in decimal, starting with doubleword zero. It is this decimal numbering of doublewords that determines whether they are even or odd.

For diagnostic purposes interleaving may be defeated (inhibited) by changing the addressing scheme so that consecutive doublewords are placed in the same BSM, either the odd or the even. This change in the addressing scheme is accomplished at the CE and does not alter the manner in which the SE interprets the SAB and select signals.

From the viewpoint of the CE, however, the addressing scheme takes three different forms: (1) Storage Interleaving, which is the normal mode of operation; (2) Defeat Interleaving; and (3) Defeat Interleaving with Storage Reverse. These three addressing schemes result from manipulation of the address bits at the CE before sending the SAB bits and select signals to the SE. The three addressing schemes are selected from a three-position DEFEAT INTERLEAVING switch on the CE control panel. This switch alters the manner in which the CE interprets address bits 6 and 20 in developing the SAB and select signals. The three addressing schemes are described in the following paragraphs.

Normal Storage Accessing with Interleaving Active

Figure 5-6(a) depicts the manner in which doublewords are placed in the BSMs of an SE when interleaving is active. The arrows show consecutive doublewords being placed in storage, starting with doubleword zero. It must be remembered that the numbering of the doublewords refers to the decimal numbering shown in Figure 5-5.

Figure 5-6(b) shows in simplified form the manner in which the address bits are interpreted at the CE in the development of the SAB and select signals. All address bits except bits 6 and 20 are carried through to become the corresponding SAB bits. Bits 6 and 20 are affected by the DEFEAT INTERLEAVING switch which is shown in the process (PROC) position used in normal operation. Note that bit 20 (the lowest order bit having significance in a doubleword storage) is used to develop the odd and even select signals. This low-order bit represents one doubleword and changes from a 1 to a 0 alternately as consecutive doublewords are addressed. A 1 bit develops a 'select odd' signal and a 0 bit develops a 'select even' signal. This alternation of select signals produces the alternation between BSMs shown by the arrows in Figure 5-6(a).

With the DEFEAT INTERLEAVING switch in the position shown, address bit 6 is carried through to become SAB (6). When the two lower halves of the lower BSMs are filled with data, the address has been incremented to the point that bit 6 becomes a 1. It will be recalled from Figure 5-4 that SAB (6) selects the upper half of a BSM if it is a 1. Thus, the upper halves of the two lower BSMs are filled by subsequent doublewords. When SAB (5) becomes a 1, the two upper BSMs begin to fill in the same interleaved fashion.

Defeat Interleaving

If a malfunction occurs in the odd half of an SE, interleaving can be defeated so that a program can be loaded into the even half only. In this manner a diagnostic may be loaded into the even half and used to test the odd half of the same SE. As will be seen, the low-odd BSM also becomes available if the malfunction is restricted to the high-odd BSM. However, this is normally more storage than is required for testing.

Figure 5-7(a) shows how consecutive doublewords are placed in an SE when the DEFEAT INTERLEAVING switch is in the "no reverse" (NO REV) position at the CE. The significance of the NO REV nomenclature is explained later in this discussion. Note that doubleword 0 is placed in the same location as if interleaving were active; i.e., in the first doubleword location of the even-low BSM. Doubleword 1 (an odd doubleword) is placed in the upper half of the same even BSM, however. The arrows at the right of the even-low BSM show how even and odd doublewords are alternately placed in the upper and lower halves of the BSM. This alternation does not constitute storage interleaving since all accesses are to the same half of storage, and one storage cycle must be completed before another can be started. However, it does reduce electrical noise within the BSM by storing consecutive doublewords in widely separated locations.

Figure 5-7(b) shows the simplified interleaving control logic at the CE with the DEFEAT INTERLEAVING switch in the NO REV position. Note that address bit 6 is now used to develop the odd and even select signals. Since

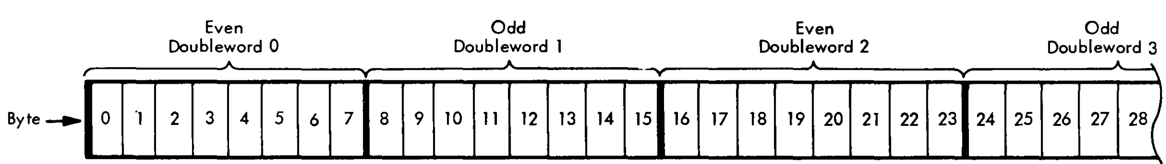
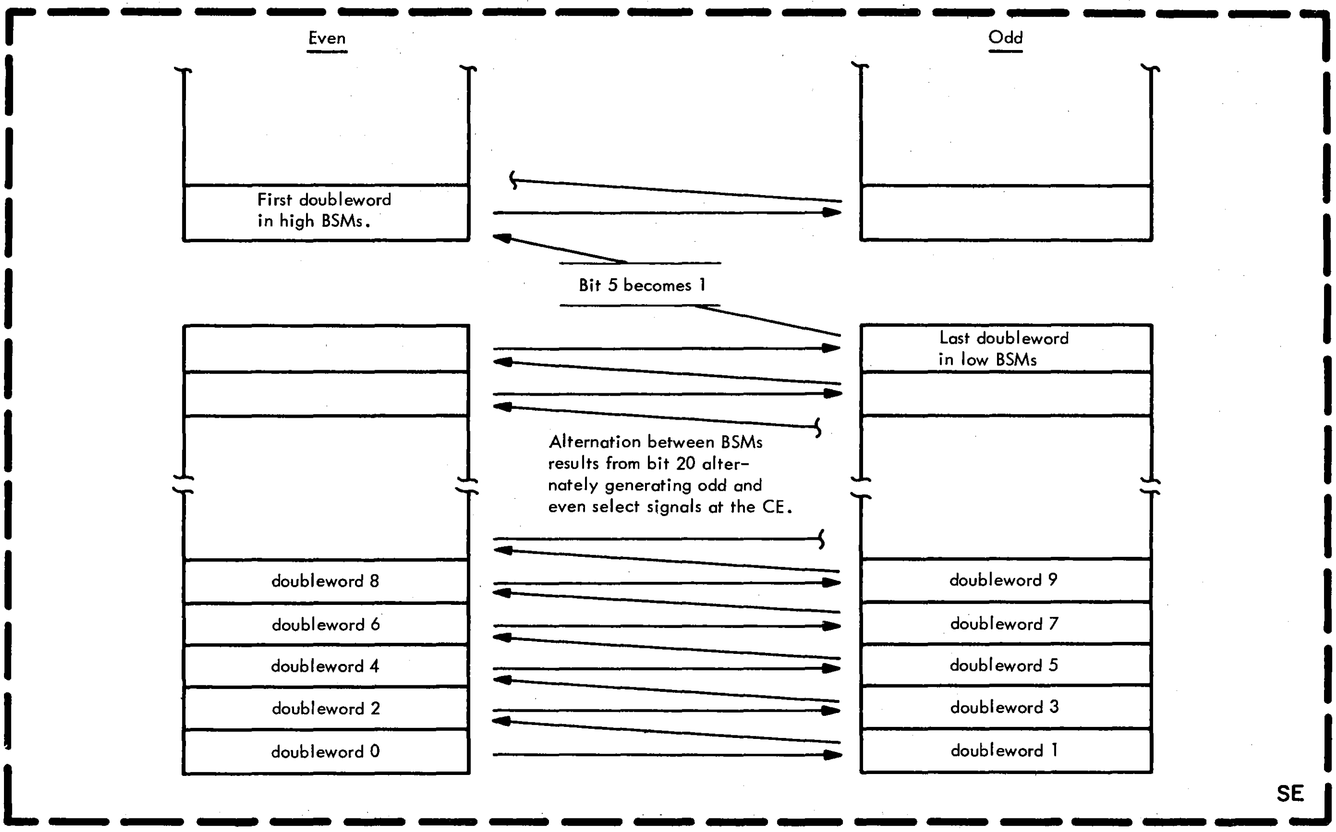
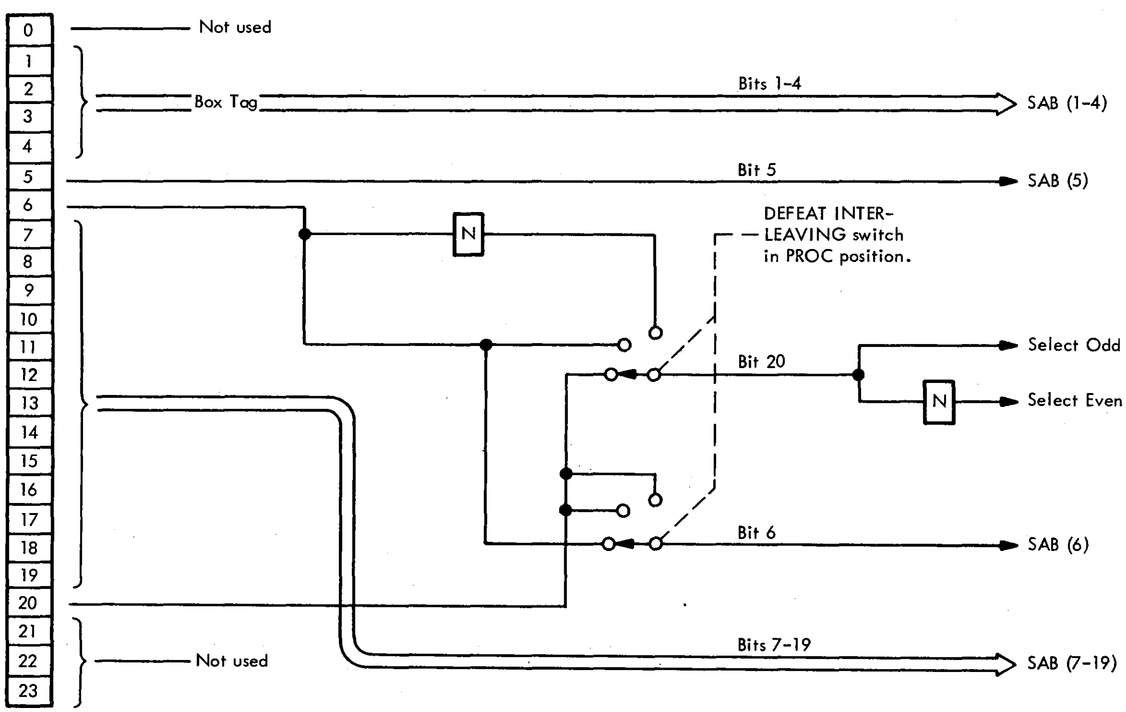


Figure 5-5. Even and Odd Doublewords

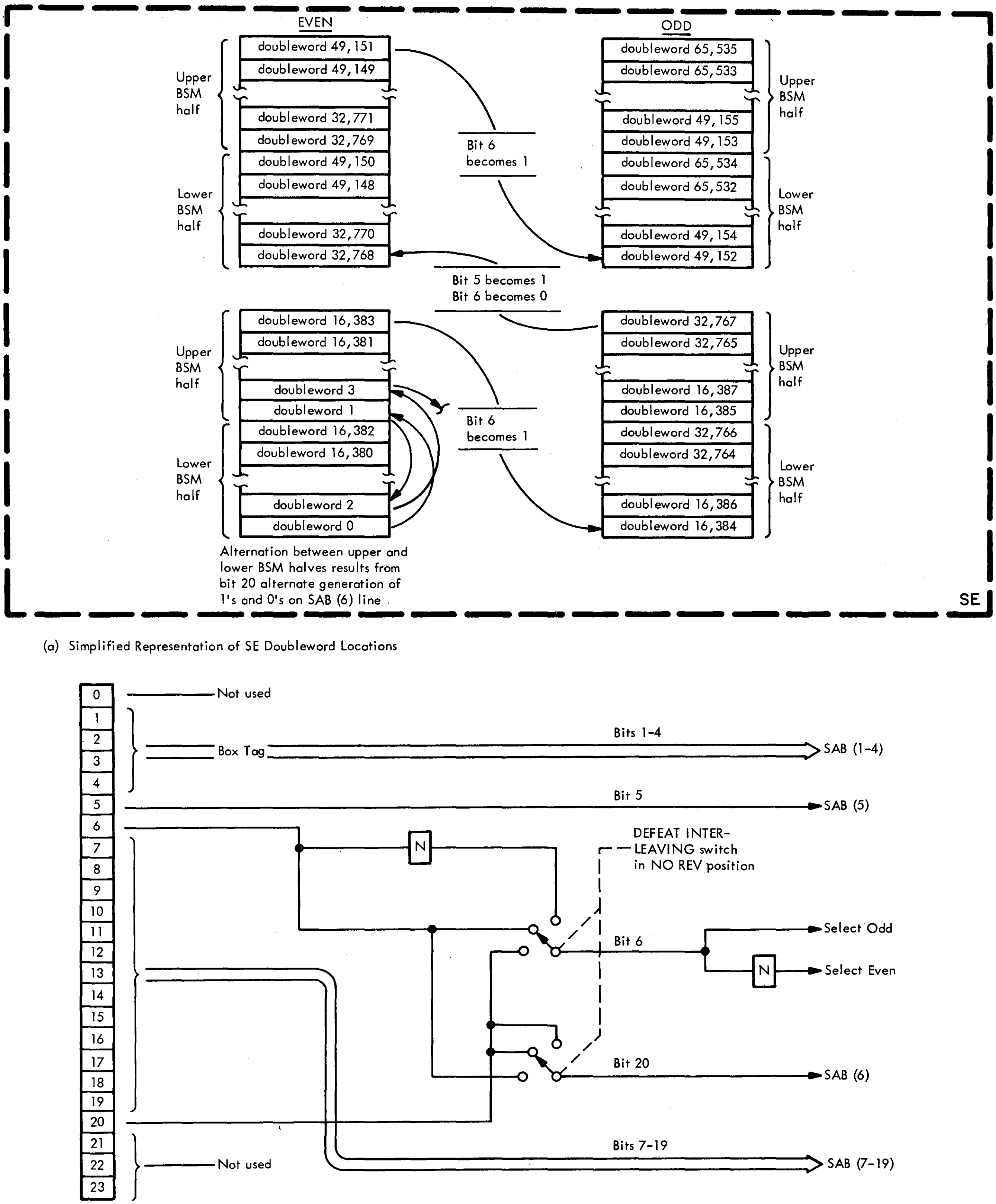


(a) Simplified Representation of SE Doubleword Locations



(b) Simplified Interleaving Control Logic in CE

Figure 5-6. Consecutive Doubleword Locations (Normal Interleaving)



(a) Simplified Representation of SE Doubleword Locations

(b) Simplified Interleaving Control Logic in CE

• Figure 5-7. Consecutive Doubleword Locations (Interleaving Defeated) address bit 6 represents 128K bytes of storage (the amount of storage in one BSM), it does not change until all of the even-low BSM has been filled. Note also that address bit 20 is now substituted for address bit 6 to develop SAB (6). Thus, bit 20, which causes the alternation between even and odd BSMs when interleaving is active, causes the alternation between the upper and lower halves of the same BSM when interleaving is defeated.

Returning to Figure 5-7(a), note that the alternation between upper and lower halves of the even-low BSM continues until the highest-numbered doubleword in the BSM (doubleword number 16,383) is accessed. Bit 6 now becomes a 1, causing the odd half of storage to be selected. Subsequent doublewords are accessed alternately from the upper and lower halves of the odd-low BSM. After the odd-low BSM has been filled, bit 5 (which represents 256K bytes) becomes a 1 and bit 6 again becomes a 0, causing the even-high BSM to be accessed. When bit 6 again becomes a 1, the odd-high BSM is accessed.

Defeat Interleaving with Storage Reversed

Figure 5-8(a) shows the manner in which consecutive doublewords are accessed when the DEFEAT INTERLEAVING switch is placed in the reverse (REV) position. Note that doubleword 0 is placed in the first doubleword location in the odd-low BSM instead of the even-low BSM. This reversal of accesses to odd and even storage permits a program to be loaded into the odd half of storage when a malfunction occurs in the even half. This is the significance of the two positions of the DEFEAT INTERLEAVING switch, NO REV and REV.

The manner in which doublewords are accessed with interleaving defeated and storage reversed can be seen by following the arrows in Figure 5-8(a). Note in Figure 5-8(b) that the DEFEAT INTERLEAVING switch is shown in the REV position. Address bit 20 is still substituted for address bit 6 in the development of SAB (6). Address bit 6 is inverted, however, before it is used to develop the even and odd select signals. This inversion of address bit 6 results in the reversal of storage.

Effect of DEFEAT INTERLEAVING Switch on IOCE Accesses

As noted previously, the IOCE has no internal provision for accessing an interleaved storage. The effect of this appears when the DEFEAT INTERLEAVING switch on the controlling CE is in the REV or NO REV position. Since the SE depends on the accessing element to establish the correct select and SAB signals, IOCE accesses during the time that Defeat Interleaving is active would be to the wrong storage locations if corrective measures were not taken. Two interface lines extend from the CEs to the SEs to inform the SSU if Defeat Interleaving or Storage Reverse are active. These signals enable the SSU to manipulate address bits received from an IOCE so that the appropriate storage location is accessed.

STORAGE ADDRESS TRANSLATION

- Provides dynamic address relocation among SEs.

- Under program control.

A 9020D system can contain as many as 10 SEs. Each CE and IOCE in the system can access any SE. Each physical SE represents a block of addresses of 524,288 bytes. Through programming, the 9020D system can alter its configuration to respond to additional system loads or to replace failing elements. Address translation is the means by which the 9020D system replaces SEs without time-consuming reinitialization of programs. The reinitialization of programs is eliminated by automatically translating storage addresses, principally through the use of an address translation register.

Logical versus Physical Addresses

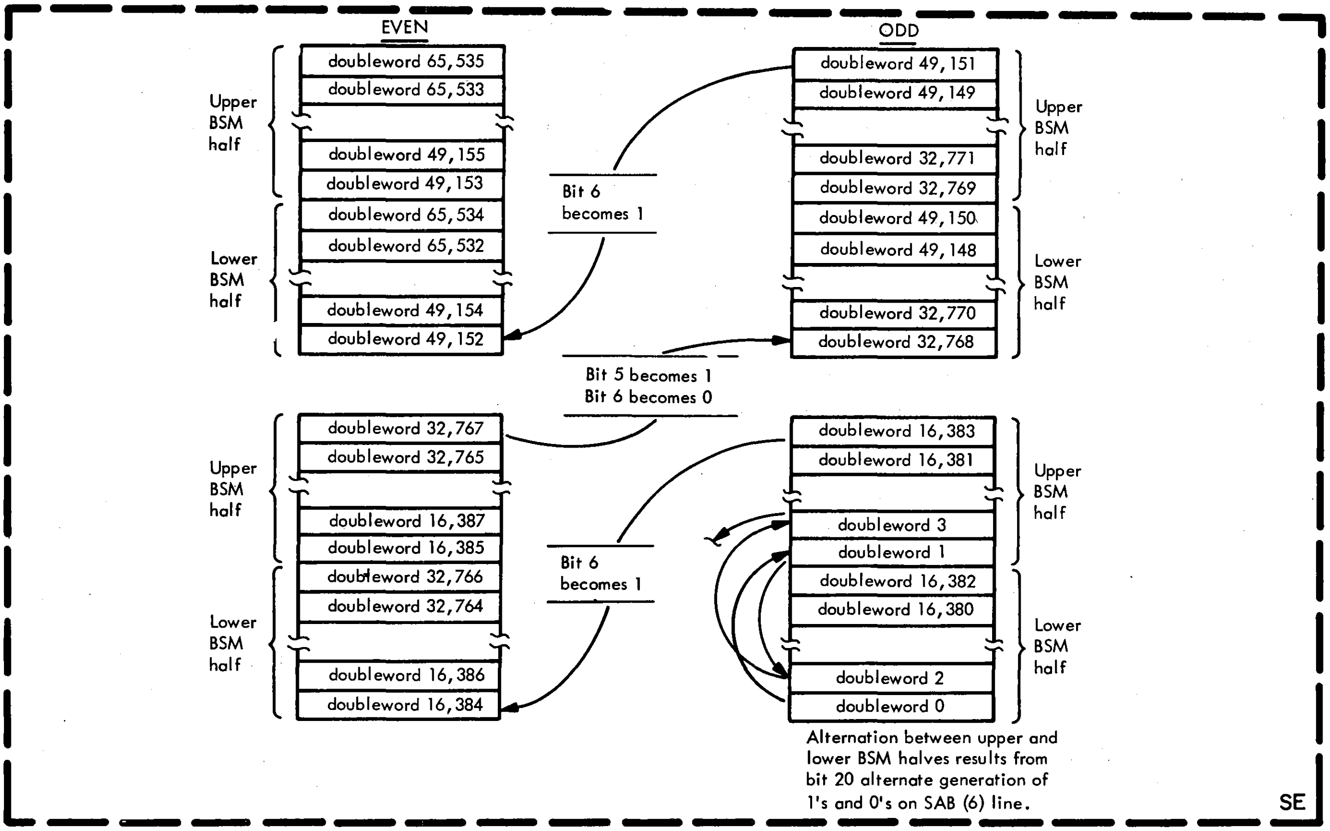
- 5,242,879 bytes of logical addresses.

- ATR slots identify physical SEs.

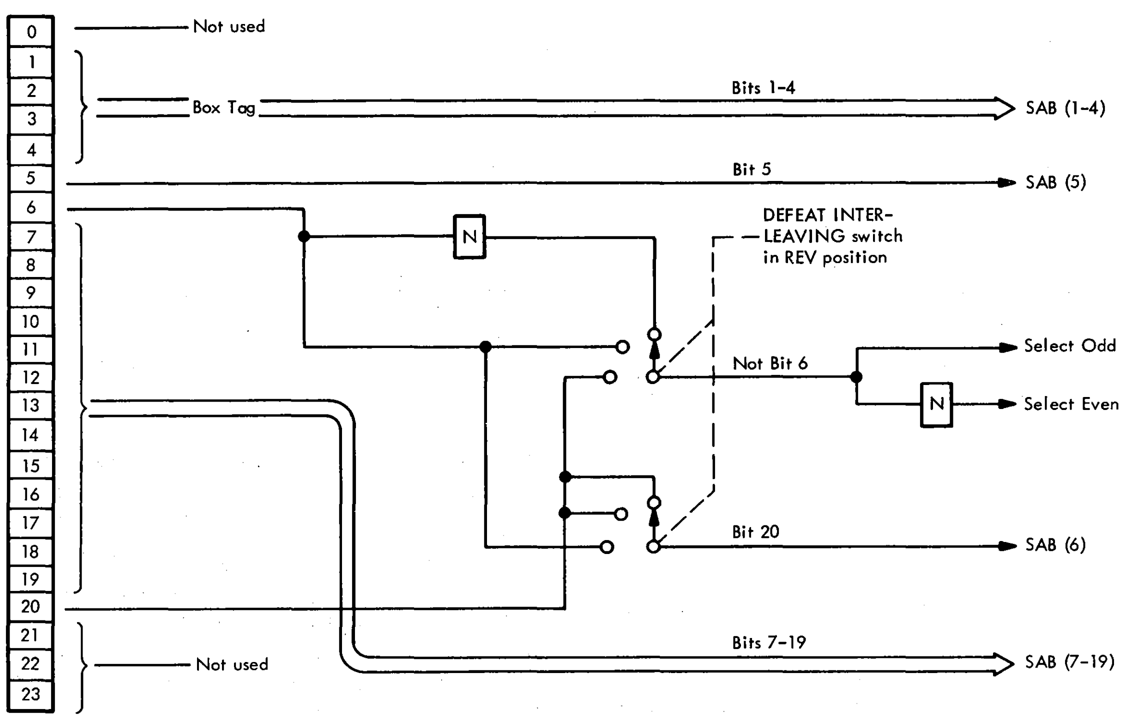
- PSBAR identifies PSA.

The maximum range of logical main storage addresses in the 9020D system is from 0 to 5,242,879 bytes (dec). This logical address range is broken into ten groups of 524,288 bytes each. The physical address range in any given SE is fixed. For example, SE 3 has the range of physical addresses from 1,048,576 (dec) to 1,572,863 (dec). However, this range of physical addresses may be substituted for any of the ten groups of logical addresses via the programmed setting of the ATR. The ATR contains ten "slots" in which physical-SE identifiers may be placed.

For example, if the programmer has placed SE 3 into ATR slot 1 and subsequently wishes to access address 5000 (dec), the physical address 1,053,576 will be sent to SE 3 as a result of address translation. This address is the sum of 5000 and the lowest address in SE 3. Since SE 3 is the lowest configured SE in the ATR, the programmer has accessed a location 5000 up from the bottom of storage, just as he intended.



(a) Simplified Representation of SE Doubleword Locations



(b) Simplified Interleaving Control Logic in CE

Figure 5-8. Consecutive Doubleword Locations (Interleaving Defeated and Storage Reversed)

The programmer, in effect, writes programs using "logical" addresses. However, the 9020 system requires "physical" addresses when accessing an SE. Address translation, therefore, is defined as the conversion of a programmer's logical address into the machine's physical address.

Storage accesses are of two types: (1) normal accesses for data or instructions and (2) accesses for control information (PSW, CAW, CSW) in a preferential area of storage. These two types of accesses are treated differently. The preferential storage area (PSA) is accessed by means of a preferential storage base address register (PSBAR), which is described later.

Normal Data Accesses

- Address bits 8–12 specify logical address of SE.
- Address bits 13–31 specify physical address within SE.

For simplicity, the logical storage address (bits 8–31) may be thought of as divided into two parts:

1. Address bits 13–31, which select an address within a 524K byte logical storage element.
2. Address bits 8–12, which select a particular logical SE.

Essentially, address bits 13–31 go directly from the CE or IOCE to the selected SE. Address bits 8–12, however, must be translated from a logical SE into a physical SE. Translation occurs in the CE/IOCE's address translation register (ATR). Figure 5-9 shows the formation of a physical storage address from a logical storage address. In this example, which is a simplification of the actual logic involved, logical SE 3 points to the third slot in ATR. Slot 3 in ATR contains the bit configuration for physical SE 6. Thus, the physical storage address which is sent out on the CE/IOCE to SE bus is composed of bits from ATR and from a logical storage address.

Programming instructions place the desired information into ATR. Using the Set Address Translator instruction (SATR), the programmer tells the system which physical SE to access when a given logical SE is addressed. Normal accesses for data use only ATR to develop a physical storage address. Normal accesses may be considered non-PSBAR accesses. Accesses into the preferential storage area use physical PSBAR to develop part of the physical storage address.

PSA Accesses

- Logical address bits 8–19 equal 0.
- Physical address sent to SE combined from three sources:
  1. Address bits 20–31 from logical address.
  2. Address bits 13–19 from logical PSBAR.
  3. Address bits 9–12 from physical PSBAR.

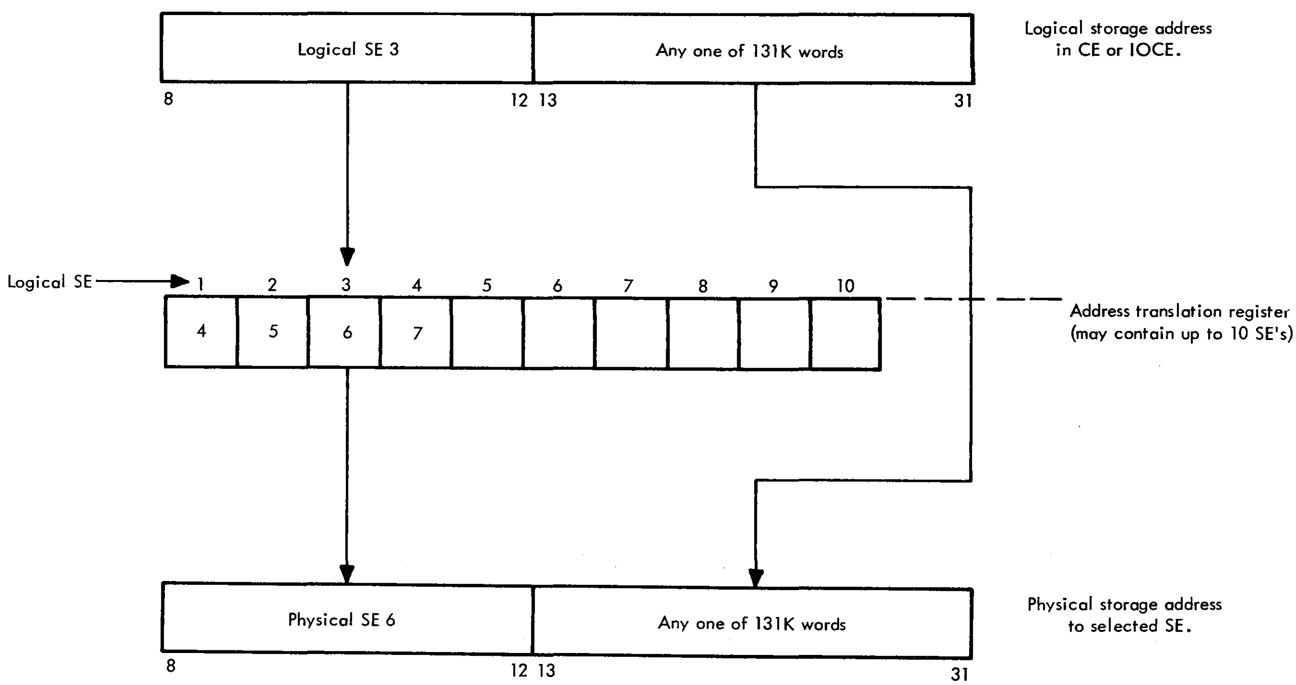


Figure 5-9. Address Translation Simplified

The PSA area contains control information such as logout data, PSW, CAW, and CSW. This PSA area consists of 4K bytes of control data that can be in any of 128 blocks of any SE. A storage access request for the PSA area is defined by a logical address containing all zeros in bits 8–19. (From the programmer's point of view, the lowest 4K bytes of storage are being addressed.) As with a normal access for data, it is necessary to convert the logical address in the CE/IOCE to a physical address sent to an SE.

The programmer determines the SE to contain the PSA area, and which one of the 128 blocks is to be used. The load PSBAR instruction (LPSB) sets into logical PSBAR the high-order bits of the preferential storage base address. Bit 8 is not included in PSBAR since no valid address is available in the 9020D main storage which uses the highest order bit. It is checked to ensure that it is a 0, however. An invalid address check occurs if it is a 1. Physical PSBAR is set at the same time. (Refer to Figure 5-10.) For a PSA access the physical address sent to the SE has three parts:

1. Bits 20–31 from the logical address in the CE/IOCE.
2. Bits 13–19 from logical PSBAR.
3. Bits 9–12 from physical PSBAR.

As with normal data accesses, ATR converts the programmer's logical SE into the system's physical SE. ATR, which is program-loaded, contains 10 four-bit slots that identify the physical SE assigned to each logical SE. In a similar manner, physical PSBAR contains four bits that identify a physical SE, the one containing the PSA area. Physical PSBAR is loaded via ATR from logical PSBAR. This is done whenever logical PSBAR is loaded (LPSB, IPL, PSW restart, or external start) or stepped. Bits 9–12 of logical PSBAR are decoded to obtain the ATR slot, and the contents of the ATR slot are then set into physical PSBAR.

If an SE fails as the PSA is being accessed, the alternate PSA area is used, and the CE automatically steps to the next configured SE and places the PSA data in the same relative PSA (bits 13–19 do not change). On this storage failure, the PSBAR counter steps sequentially through the ATR positions until the next configured SE is found. If no configured alternate is found by the time slot 10 is decoded the second time, stepping stops and the CE hardstops and issues ELC.

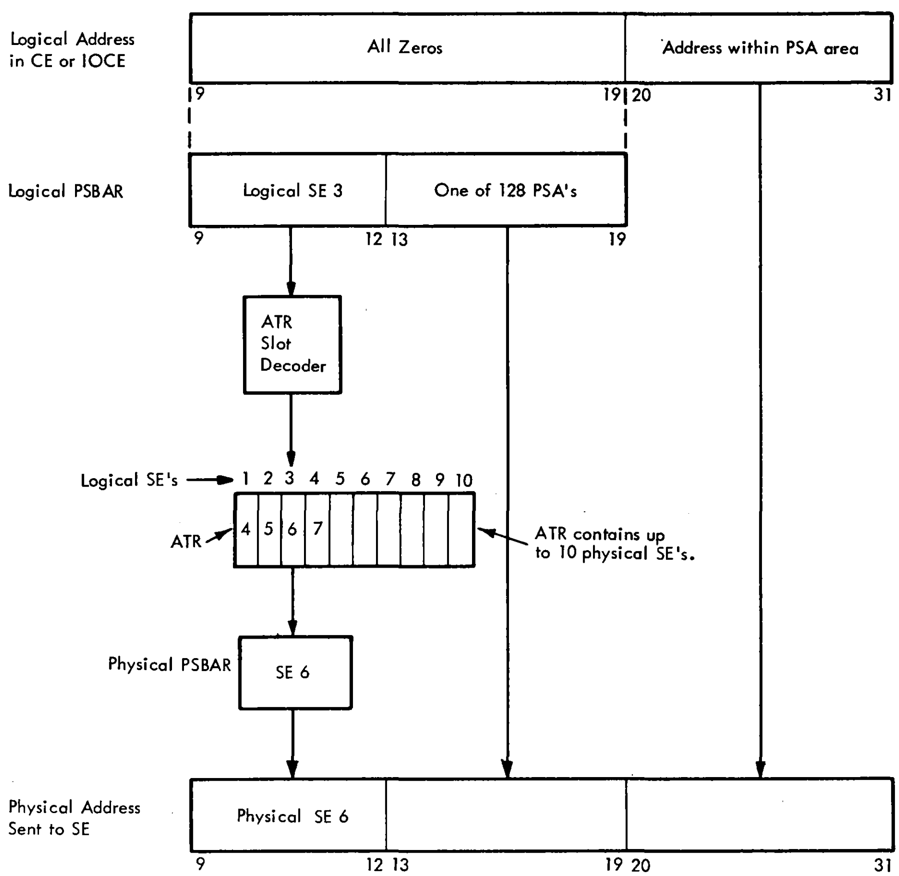


Figure 5-10. Preferential Storage Address (PSA) Formation

Address Translation Register (ATR)

- 40-bit register.
- One register in each CE and IOCE.
- Translates "logical" addresses (SEs) into "physical" addresses (SEs).
- Each of the 10 SEs is represented in ATR.

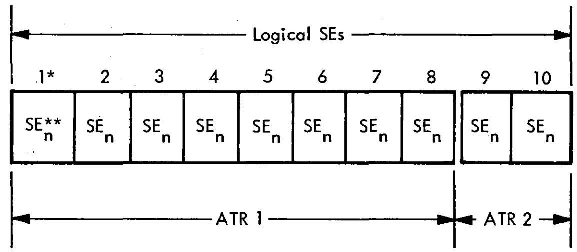
As already mentioned, each CE and IOCE has the capability of accessing each of the 10 SEs within the system. Therefore, to accomplish translation from within the entire system, an address translation register must be located in each of the CEs and IOCEs. Because an expanded system can contain a maximum of 10 SEs, each ATR must be capable of performing address translation to any one of the available elements.

The entire ATR is a 40-bit register (Figure 5-11(a)) and consists of a 32-bit ATR 1 and an 8-bit ATR 2. The entire register logically consists of 40 continuous bits but is divided into ATR 1 and ATR 2 because of the 32-bit data paths of the IOCE.

The ATR is further divided into ten 4-bit sections, or slots. Each slot starting at ATR 1 (0–3) and continuing through ATR 2 (4–7) contains the translation identifier for logical SEs 1-10, respectively. These identifiers consist of the 11 hexadecimal characters 0-A. Character 0 indicates that this logical SE is unassigned (not to be used); characters 1–A represent physical SEs 1–10, respectively; and characters B-F are considered invalid. Figure 5-11(b) shows the identifiers and the corresponding SEs. The corresponding range of actual addresses is shown in Figure 5-1.

Figure 5-11(c) shows a simple, straightforward ATR setting where both the three logical and three physical SEs are the same. The remaining elements are unassigned.

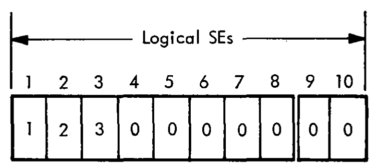
Figure 5-11(d) shows five assigned SEs. In this latter case program references to SEs 2 and 3 will be serviced by SEs 4 and 5, and references to SEs 4 and 5 will be serviced by SEs 2 and 3. All other positions (6-10) are unassigned.



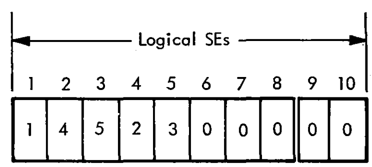
(a) Address Translation Register Format

SE Identifier	Physical Storage Reference
0	***
1	SE1
2	SE2
3	SE3
4	SE4
5	SE5
6	SE6
7	SE7
8	SE8
9	SE9
A	SE10
B	Invalid
C	Invalid
D	Invalid
E	Invalid
F	Invalid

(b) ATR Storage Identifiers



(c) ATR Example, Simple



(d) ATR Example

Legend:

* These 10 positions of the ATR represent the logical storage.
** The identifier character contained in these four bits represents the physical storage which is actually accessed.
*** Indicates an unassigned logical element.

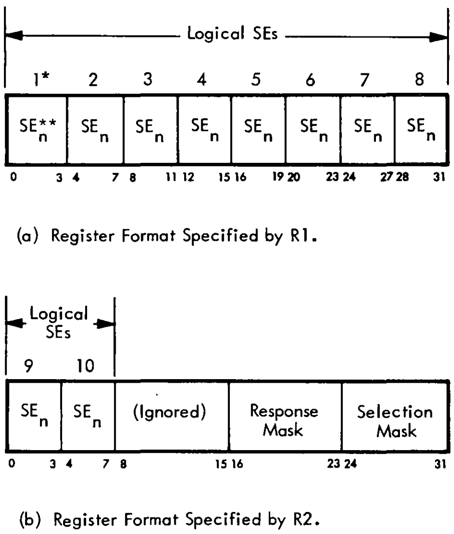
Figure 5-11. Address Translation Register

Set Address Translator Instruction (SATR)

- RR format.
- Establishes system address translation for all CEs and IOCEs.
- Receiving elements are determined by a selection mask.
- Receiving elements must have their SCON bits set to the sending CE. (See "Condition Code - 1".)

By means of the SATR instruction, a CE can establish the appropriate storage assignments for "itself", for the IOCEs, and for other CEs under its immediate control. The assignment is accomplished by loading the 10 proper storage identifier characters into the ATR of each of the selected CEs and IOCEs. These identifier characters were discussed in the previous section and listed in Figure 5-11(b).

The registers specified by R1 and R2 of the SATR instruction contain the necessary data for execution of the operation (Figure 5-12). The 32 bits of R1 plus bit positions 0–7 of R2 represent the 40-bit ATR setting (assignment mask) to be sent to the selected CEs and IOCEs.



Legend:

* These 10 positions of the registers represent the "logical" storage.
** The identifier character contained in these four bits represents the "physical" storage.

Figure 5-12. Register Formats as Specified by R1 and R2 of the SATR Instruction

Selection of the proper elements is designated by a selection mask located in bit positions 24–31 of R2 (Figure 5-13). By means of this selection mask, the issuing CE can select any combination of CEs and IOCEs (including itself) to receive the new ATR setting. Bits 8 to 15 are ignored. Bit positions 16–23 of R2 (Figure 5-13) are initially ignored but will eventually represent a response indication from the selected elements in a manner similar to execution of the SCON instruction.

Element	Response Mask Bit	Selection Mask Bit
CE 1	16	24
CE 2	17	25
CE 3	18	26
CE 4	19	27
(Unassigned)	20	28
IOCE 1	21	29
IOCE 2	22	30
IOCE 3	23	31

Figure 5-13. Selection and Response Mask Formats for the SATR Instruction

At the time of installation, each CE has an assignment card installed which indicates the maximum number of SEs installed on that particular system. By means of the information available from this card, microprogramming tests to make sure that an SE identifier character has been properly assigned and is within the specified range of the system.

Execution of the SATR instruction is subject to internal checking by both microprogramming and hardware. A specification check (interrupt code 110) results from a violation of any one of the following conditions:

1. The issuing CE must be in state three or state zero.
2. The issuing CE must have its own SCON bit on.
3. The identifier characters in the ATR must reference only the valid SEs assigned to the installation. These are determined by the pluggable assignment card installed in the CEs.
4. At least one of the valid identifiers must be a non-zero character. Because a zero identifier character indicates an unassigned storage module, an all-zero ATR would not designate any usable storage.

Two other program interruptions can also occur besides the specification check. An invalid operation interrupt (interrupt code 1) occurs if the CE is in 360 mode instead of 9020 mode. A privileged operation interrupt (interrupt code 10) occurs if the SATR instruction is attempted in the problem state instead of the supervisory state.

In addition to the program interrupts just mentioned, condition code settings also supply the program with additional information, as follows:

Condition Code - 0: Indicates that all selected elements have accepted the new identifier characters (assignment mask) into their ATR. This indicates a successful completion of the SATR instruction. In this case the original contents of the response field (byte 2 of R2) are unchanged.

Condition Code - 1: Indicates that the SATR instruction was not completed because one or more of the selected elements did not respond to the initial selection by the issuing CE.

Before the ATR contents are actually transmitted to the selected elements, the issuing CE tests each element to determine if that element is able to respond. Bit positions 16–23 of R2 represent a response mask similar in format to the select mask in bit positions 24–31 of R2 (Figure 5-6). At the end of this test, any element that fails to respond is indicated by a 1-bit in the corresponding response mask position in byte 2 of R2; all other bits in the response mask are set to zero. By analyzing these bits, the program can determine the element or elements responsible for terminating the instruction.

In order to respond initially to the SATR instruction, the receiving element must have its CCR SCON field set to the sending CE. If the receiving element is another CE, that CE must either be in the wait state or must reach an I-fetch within the selection period in order to respond. If the receiving element is an IOCE, it will respond after finishing the current storage cycle provided that a CE communication bit is on and the element is not in the process of resetting.

Condition Code - 2: Indicates that one or more of the selected elements failed to properly accept the new assignment mask into its ATR. In this case, the element responded to the initial selection, but a parity check or internal logic check prevented it from accepting the new setting. The response mask in R2 (16–23) again allows the program to determine the particular element or elements at fault. The selected elements which do not have a corresponding 1-bit in the response mask have received the new ATR setting. As mentioned previously, a successful response from all elements results in an unchanged response mask and a CC = 0.

If a check condition occurs in a receiving CE, that CE immediately proceeds to logout into its PSA area (provided that PSW 13 is on), and issues an element check (ELC) signal to all CEs within the system.

If a check condition occurs in a receiving IOCE, that IOCE requests a machine check interrupt (for logout) from the issuing CE.

By analyzing the logout data areas for the malfunctioning element, the control program can try to determine why the ATR assignment mask was not accepted.

Condition Code - 3: Indicates a selection mask of all zeros. In this case, no elements (CEs or IOCEs) were designated for selection of the new ATR setting.

As can be seen, extensive testing is performed to make sure that: an authorized CE is issuing the instruction; only authorized elements are receiving the new ATR setting; the translation identifier characters are properly used; and that the settings were successfully received.

Insert Address Translator Instruction (IATR)

- RR format.

- Inserts the 40-bit ATR into R1 and R2.

The IATR instruction places the 40-bit ATR into the two registers specified as R1 and R2 of the instruction. The high-order 32 bits of the ATR (corresponding to SEs 1–8) are placed into R1; the low-order 8 bits (corresponding to SEs 9 and 10) are placed in 0–7 of R2. Bits 8–31 of R2 are set to zeros.

Instruction execution is such that if R1 and R2 are specified as the same register (i.e., R1=R2) the high-order 32 bits of the ATR are inserted in that specified register. An advantage here is that programmers need not disturb a second general-purpose register when executing the IATR instruction for systems containing less than nine SEs.

Note that execution of the IATR only allows the CE to examine its own ATR. If a controlling CE wishes to analyze the ATR of other system elements, it may do so by issuing an external logout to that element by means of the Write Direct (WRD) instruction.

Address Translation Example No. 1

Assume that the overall system is configured into three subsystems as shown in Figure 5-14. In each subsystem, the lowest logical SEs are assigned for use of their operating programs. The state three ATC subsystem is using physical SEs 1–4 in direct correlation to their logical assignments. The state two subsystem is using physical SEs 5–7 and assigning them to logical SEs 1–3, respectively. The state zero maintenance subsystem is using only one SE (SE 8) assigned to logical SE 1.

Programs are generally written starting in low storage areas and overflowing into as many more SEs as necessary. The programs can, therefore, be run in any of the various subsystems relatively independent of the availability of physical elements by simply assigning the available (physical) SEs to the logical elements with low-order numbers.

The diagnostic programs being run in the state zero subsystem will most likely be written to addresses within logical SE 1. In this example, then, SE 8 is assigned as logical SE 1.

To accomplish the three subsystem assignments, three SATR instructions must be executed by the EXC control program. The contents of general-purpose registers R1 and R2 for each assignment are shown in Figure 5-15.

Figure 5-15(a) shows the state three SE assignment mask with its selection mask selecting CE 1 and IOCE 1.

Figure 5-15(b) shows the state two SE assignment mask and its selection mask assignment selecting CE 2 and IOCE 2. Figure 5-15(c) shows the maintenance state zero assignment mask for SE 8 and the selection mask selecting CE 3 and IOCE 3.

Note in Figure 5-14 that for each physical SE assigned to that subsystem, there is a corresponding configuration bit also assigned within the CCR of the CE and IOCE. For example, in the state zero subsystem where logical SE 1 is assigned to physical SE 8, the CCR of both CE 3 and IOCE 3 has been configured with a 1-bit corresponding to SE 8.

Address Translation Example No. 2

From ATR example No. 1, assume that SE 2 shows signs of trouble. The EXC program therefore decides to recall SE 8 from the maintenance subsystem into the state three ATC

No. 1 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	0	0	0

No. 2 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	0	0	0

No. 3 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	1	0	0

No. 4 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	1	0	0

No. 5 Storage Element ■

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	0	1	0	0	0	1	0	0	0	0

No. 6 Storage Element ■

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	0	1	0	0	0	1	0	0	0	0

No. 7 Storage Element ■

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	0	1	0	0	0	1	0	0	1	0

No. 8 Storage Element ☒

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
0	0	1	0	0	0	0	1	0	0	1

No. 1 Computing Element ●

			SCON			SE								CE			IOCE		
CCR	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
	1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0

	Storage Element									
ATR	1	2	3	4	5	6	7	8	9	10
	1	2	3	4	0	0	0	0	0	0

No. 2 Computing Element ■

			SCON			SE								CE			IOCE		
CCR	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
	1	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0

	Storage Element									
ATR	1	2	3	4	5	6	7	8	9	10
	5	6	7	0	0	0	0	0	0	0

No. 3 Computing Element ☒

			SCON			SE								CE			IOCE		
CCR	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1

	Storage Element									
ATR	1	2	3	4	5	6	7	8	9	10
	8	0	0	0	0	0	0	0	0	0

No. 1 I/O Control Element ●

			SCON			SE								CE		
CCR	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
	1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	0

	Storage Element									
ATR	1	2	3	4	5	6	7	8	9	10
	1	2	3	4	0	0	0	0	0	0

No. 2 I/O Control Element ■

			SCON			SE								CE		
CCR	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
	1	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0

	Storage Element									
ATR	1	2	3	4	5	6	7	8	9	10
	5	6	7	0	0	0	0	0	0	0

No. 3 I/O Control Element ☒

			SCON			SE								CE		
CCR	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1

	Storage Element									
ATR	1	2	3	4	5	6	7	8	9	10
	8	0	0	0	0	0	0	0	0	0

Legend:

- ● State Three ATC Subsystem
- ■ State Two Subsystem
- ☒ State Zero Maintenance Subsystem

● Figure 5-14. Address Translation Example No. 1

	Logical SEs							
R1	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
	0 3	4 7	8 11	12 15	16 19	20 23	24 27	28 31

	Logical SEs		Ignored		Response Mask	Selection Mask
R2	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 0 1 0 0
	0 3	4 7	8 11	12 15	16 23	24 31

(a) First SATR Instruction

	Logical SEs							
R1	0 1 0 1	0 1 1 0	0 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
	0 3	4 7	8 11	12 15	16 19	20 23	24 27	28 31

	Logical SEs		Ignored		Response Mask	Selection Mask
R2	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	0 1 0 0 0 0 1 0
	0 3	4 7	8 11	12 15	16 23	24 31

(b) Second SATR Instruction

	Logical SEs							
R1	1 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
	0 3	4 7	8 11	12 15	16 19	20 23	24 27	28 31

	Logical SEs		Ignored		Response Mask	Selection Mask
R2	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	0 0 1 0 0 0 0 1
	0 3	4 7	8 11	12 15	16 23	24 31

(c) Third SATR Instruction

Figure 5-15. SATR Formats for Example No. 1

subsystem, and reassigns SE 2 to the maintenance subsystem for checkout. This reassignment involves the swapping of physical SEs 2 and 8, but the logical assignments remain the same; i.e., the active program storage references are not changed, but a different SE is used in the operation.

To accomplish this reassignment, two SATR instructions are required. The contents of general-purpose registers R1 and R2 for each SATR instruction are shown in Figure 5-16. Figure 5-16(a) shows the state three assignment mask with the identifier character 8 replacing the character 2 in the logical SE 2 position. The selection mask selects CE 1 and IOCE 1. Figure 5-16(b) shows the state zero assignment mask with the identifier character 2 replacing the character 8 in the logical SE 1 position. The selection mask selects CE 3 and IOCE 3. No SEs were reassigned within subsystem two; therefore, no SATR operation is needed for that subsystem.

Figure 5-17 shows the final settings after execution of the SATR instructions. Note that with the reassignment a reconfiguration by means of the SCON instruction is also necessary to configure SE 2 out of the ATC subsystem and into the maintenance subsystem and vice versa.

The SATR instruction can be executed at any time by the EXC control program. It should be noted, however,

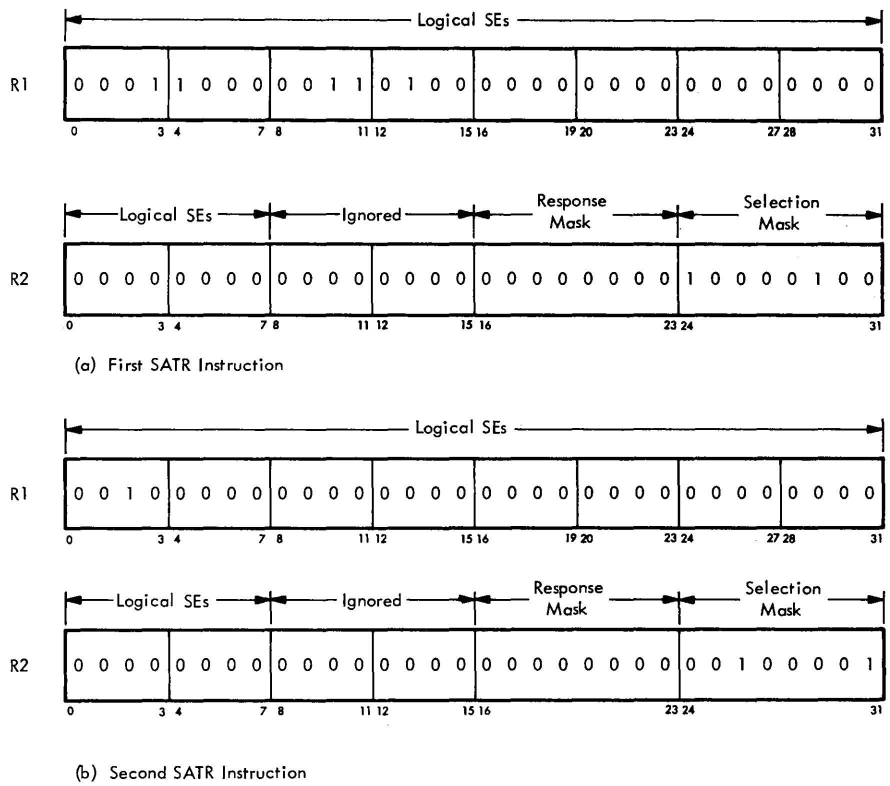


Figure 5-16. SATR Formats for Example No. 2

that this type of programming could have disastrous results if, for example an address reassignment were made in the middle of a program in a CE.

If a CE is in the wait state during receipt of an SATR command, it will return to the wait state at the completion of the reassignment. If the CE was not in the wait state, the reassignment will be performed and the CE will return to I-fetch. This next I-fetch, however, may now fetch the wrong instruction or may try to operate on a data word in some new SE.

To avoid problems of improper execution or loss of data, the EXC program normally stops all elements in the various subsystems before executing new SATR instructions.

PREFERENTIAL STORAGE AREAS (PSAs)

- Unique PSAs available to each processor.
- MACH contains PSA for IOCE processor.
- Each PSA contains 4,096 bytes.
- PSA assignment is under both program and hardware control.

In a system that contains only one processor, all essential control and status information is stored in fixed low-order addresses of the attached storage. This vital information consists of three double words for IPL, old and new PSWs for machine interrupts, CAW and CSW words, timer, and the diagnostic logout area. The low-order portion of storage where this information is stored can be thought of as a PSA.

In a multiprocessing system, each processor must have its own unique PSA. Separate PSAs allow each processor (CE) to service I/O operations and interrupts without interference from other processors within the system. MACH storage contains a PSA area for controlling IOCE processor operations. Both PSAs (in a CE or IOCE) serve the same purpose, but the functions of the PSA in MACH are somewhat limited with respect to those in a CE.

Design of the 9020 system is such that each 524,288-byte SE can be divided into 128 blocks of 4096-byte PSAs (Figure 5-18).

The addressing scheme (Figure 5-19) is such that the 12 low-order bits specify a 4096 block of byte addresses equal to one PSA. The 12 high-order bits can be logically divided into two sections: seven bits (13–19) can indicate any one of 128 4,096-byte blocks (PSAs) within one SE; four bits (9–12) can indicate a specific SE within which the PSA is located. Bit 8 is not used for addressing but is checked to

No. 1 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	0	0	0

No. 2 Storage Element ⧄

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
0	0	1	0	0	0	0	1	0	0	1

No. 3 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	1	0	0

No. 4 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	1	0	0

No. 5 Storage Element ■

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	0	1	0	0	0	1	0	0	0	0

No. 6 Storage Element ■

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	0	1	0	0	0	1	0	0	0	0

No. 7 Storage Element ■

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	0	1	0	0	0	1	0	0	1	0

No. 8 Storage Element ●

		SCON			CE			IOCE		
S	S	1	2	3	1	2	3	1	2	3
1	1	1	0	0	1	0	0	0	0	0

No. 1 Computing Element ●

			SCON			SE								CE			IOCE		
	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
CCR	1	1	1	0	0	1	0	1	1	0	0	0	1	0	0	0	1	0	0

Storage Element

	1	2	3	4	5	6	7	8	9	10
ATR	1	8	3	4	0	0	0	0	0	0

No. 2 Computing Element ■

			SCON			SE								CE			IOCE		
	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
CCR	1	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0

Storage Element

	1	2	3	4	5	6	7	8	9	10
ATR	5	6	7	0	0	0	0	0	0	0

No. 3 Computing Element ⧄

			SCON			SE								CE			IOCE		
	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3	1	2	3
CCR	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1

Storage Element

	1	2	3	4	5	6	7	8	9	10
ATR	2	0	0	0	0	0	0	0	0	0

No. 1 I/O Control Element ●

			SCON			SE								CE		
	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
CCR	1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	0

Storage Element

	1	2	3	4	5	6	7	8	9	10
ATR	1	8	3	4	0	0	0	0	0	0

No. 2 I/O Control Element ■

			SCON			SE								CE		
	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
CCR	1	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0

Storage Element

	1	2	3	4	5	6	7	8	9	10
ATR	5	6	7	0	0	0	0	0	0	0

No. 3 I/O Control Element ⧄

			SCON			SE								CE		
	S	S	1	2	3	1	2	3	4	5	6	7	8	1	2	3
CCR	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1

Storage Element

	1	2	3	4	5	6	7	8	9	10
ATR	2	0	0	0	0	0	0	0	0	0

Legend:

● State Three ATC Subsystem

■ State Two Subsystem

⧄ State Zero Maintenance Subsystem

● Figure 5-17. Address Translation Example No. 2

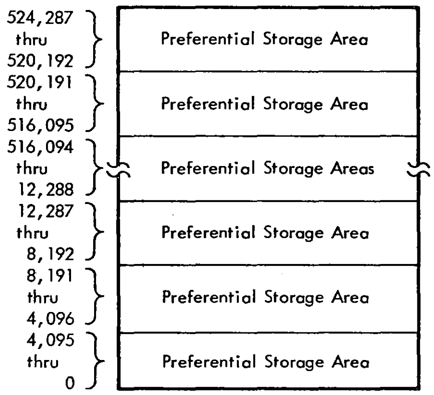
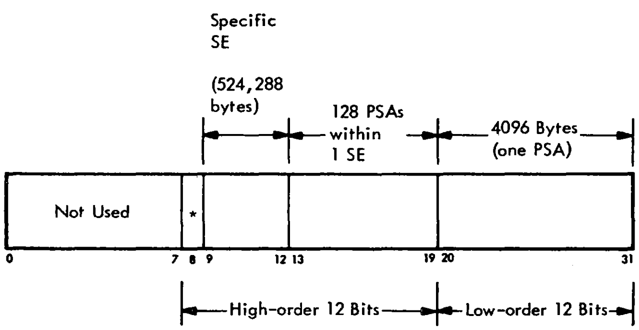


Figure 5-18. Relative PSA Assignments Within an SE



Legend: *Must be zero.

Figure 5-19. 9020 Addressing

ensure that it is zero. An invalid address check occurs if bit 8 is set to 1. The combined high-order bits specify a PSBA to be used during fixed-address machine operations.

A special PSBAR in the CE can be loaded by a load PSBA (LPSB) instruction to specify the particular preferential area to be used by that CE.

Because of the fail-safe/fail-soft requirements of the 9020 system, each CE must be able to relocate its PSA to secondary areas when the primary area (SE) becomes unavailable. This PSA relocation must be under program or automatic control; manual intervention is too slow and is subject to human error.

PSA relocation can actually occur in two ways: under program control by the LPSB instruction, and automatically by hardware. These programming and automatic hardware facilities allow the 9020 system to dynamically adjust itself to changes in available storage due to storage failures (automatic relocation) or to changes in the actual load or load requirements (program-controlled PSA relocation).

Refer to Chapter 8, under "CE Handling of SE Response Errors", for further information about automatic PSBAR stepping in response to a malfunction.

Preferential Storage Base Address Register (PSBAR)

- Two registers: logical PSBAR and physical PSBAR.
- Loaded and stored under program control.
- Effective when the 12 high-order address bits = 0.
- Used primarily for preferential storage references; not normally used for data references.

The PSBAR references the proper PSA currently assigned and associated with the CE or IOCE program. PSA references to old and new PSWs, channel CAWs and CSWs, and to logout areas always refer to low-order fixed addresses starting at location zero. This low-order addressing is automatically recognized by hardware circuits whenever the 12 high-order bits are 0's. When high-order 0's are detected, the 11-bit PSBAR value is ORed with these 0's to produce a reference to the proper PSA area. For example, if an interrupt routine addressed the I/O old PSW at location 38 (hex), the CE would attempt to address location: 0000 0000 0000 0000 0011 1000.

If this CE's assigned PSA is located in the second 4K block of storage (bytes 4,096-8,191) in physical SE 2, the PSBAR value and resultant ORing would be:

0000 0000 0000 0000 0011 1000	(Fixed address)
001 0000 0001	(11-bit PSBA ORing)
0001 0000 0001 0000 0011 1000	(Fixed address in PSA 1 of SE 2)

All interrupts and logouts are affected by PSBAR. Program-generated addresses are also affected where the 12 high-order address bits are all 0's.

The ORing of PSBAR is completely automatic. Note that the original address contained in the instruction is not changed. Actually, PSBAR is composed of both a logical and a physical PSBAR which are related to each other through the ATR discussed earlier.

Logical PSBAR

- An 11-position register in each CE.
- Loaded by LPSB instruction.
- Stored by SPSB instruction.
- Contains a four-position counter for SE selection.

This 11-position register is loaded by the LPSB instruction and retains this initial setting until it is reloaded by a new LPSB instruction or is changed by an external start.

Positions of the register are labeled to match their corresponding address positions (Figure 5-20). The 11 positions can be divided into two logical sections: positions 13–19, which can select a particular PSA within a storage element, and positions 9–12, which select a particular SE.

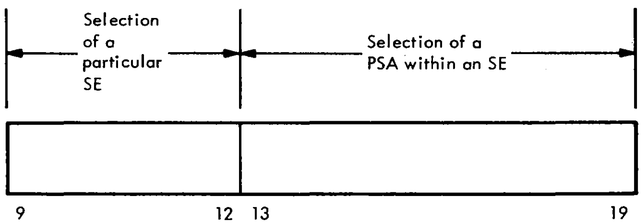


Figure 5-20. Logical PSBAR Format

As is explained later, positions 9–12 of logical PSBAR enter a 4-position binary counter that is used to automatically select new SEs under certain malfunction conditions. The contents of this logical register (bits 13–19) and the present value in the 4-position counter (bits 9–12) can be obtained by the program by the Store PSBA instruction (SPSB). Refer to "Store PSBA Instruction (SPSB)".

Physical PSBAR

- A four-position register in each CE.
- Set from logical PSBAR after translation by ATR.
- Stored by SPSB instruction.

Physical PSBAR specifies the physical, or actual, SE to be used in a preferential storage reference. It is a four-position register set to one of the identification characters (identifiers) found in the ATR. The particular ATR slot from which the identifier is taken is determined by decoding bits 9–12 of logical PSBAR. This decoding is shown in Figure 5-21. Since an address of all 0's would naturally fall in the first slot, all 0's in logical PSBAR decodes slot 1. The slot decoded is, therefore, always one more than the binary value in logical PSBAR (9–12) within the range of valid addresses.

Physical PSBAR is set during execution of the Load PSBA (LPSB) instruction. It is also set when, due to a malfunction, the PSBAR counter has stepped to the alternate PSA SE. When the alternate SE is located and found to be configured, the identifier from the new ATR slot is set into physical PSBAR. Bits 9–12 of logical PSBAR are also updated during this stepping, as discussed later under "PSBAR Counter".

Because the contents of physical PSBAR are always available in translated form, references to the PSA are made by using bits 9–12 directly from physical PSBAR rather than by using the contents of the ATR slot, as is done during a non-PSA storage access.

Figure 5-22 shows how the effective address for a PSA access is developed. Note that the address retains the original low-order bits but obtains the high-order bits from logical and physical PSBAR; bits 13–19 come from logical PSBAR and bits 9–12 come from physical PSBAR.

The value in physical PSBAR may be obtained by the program via the Store PSBA (SPSB) instruction (see "Store PSBA (SPSB)").

PSBAR Counter

- A four-position counter.
- Set from logical PSBAR (9–12).
- Automatically steps to new storage element (PSA) for certain PSA storage failures.

Positions 9–12 of the logical PSBAR are set into a four-position binary counter (Figure 5-23). By means of this counter, each CE can automatically reference an alternate PSBA whenever the inhibit logout stop (ILOS) bit is off in the CCR, and a failure occurs on an access to the SE containing the primary PSA. The alternate PSBA is obtained by incrementing the counter (adding successive 524,288-byte increments to the logical PSBA) until the next configured SE is reached. In Figure 5-23, the value of zero is shown in logical PSBAR (9–12). This decodes as ATR slot 1.

As the counter is stepped, each higher logical position of the ATR is tested for an identifier character of a configured SE. When the first configured SE is found in the ATR, physical PSBAR is updated with the new identifier character. PSA references are now made to this new SE where the EXC program has already set up proper PSWs, CAWs, CSWs, etc., to handle the situation.

If the counter reaches the highest SE in the system, incrementing continues past the non-existent SEs until wraparound effect is achieved, stepping from the highest to the lowest SE. The ATR is again tested from left to right until the alternate SE is found.

After stepping to an alternate SE, the PSBAR counter is inhibited from further stepping until a load PSBA instruction is issued by the CE. This instruction (or an external start) resets the counter's stepping abilities and allows normal incrementing as described previously.

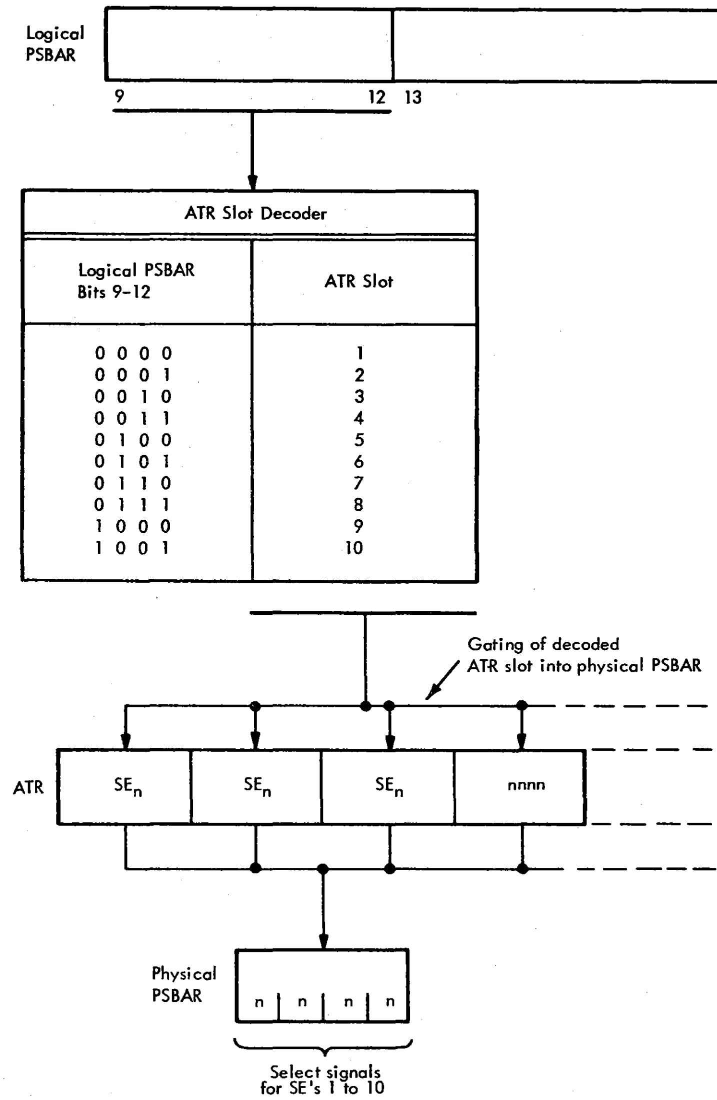


Figure 5-21. Setting of Physical PSBAR from Logical PSBAR

If, after locating an alternate SE through PSBAR stepping, errors are still obtained in accessing the PSA, the CE hardstops and issues an element check (ELC) signal. Until a Load PSBA instruction is issued, the CE retains its current logical and physical PSBAR and PSBAR counter values and all further incrementing is inhibited. A full analysis of all three can be obtained by a diagnostic logout.

If no configured alternate SE is found during PSBAR stepping, stepping stops when logical PSBAR contains 9 (1001 hex) the second time. Figure 5-21 shows that a 9 in logical PSBAR decodes ATR slot 10. The PSBAR counter would be set to 0000 at this time. When stepping stops with no configured alternate SE found, the CE hardstops and issues ELC.

Load PSBA Instruction (LPSB)

- SI format.
- Valid only in supervisor state and 9020 mode.
- Loads both the logical and physical PSBAR.

The load PSBA instruction is in SI format; the I2 field (positions 8–15) is ignored. Bits positions 8–19 of the word fetched by the LPSB instruction represent the 12 high-order bits of the PSBA.

The LPSB instruction can be executed only in supervisory state and 9020 mode, and the effective address of

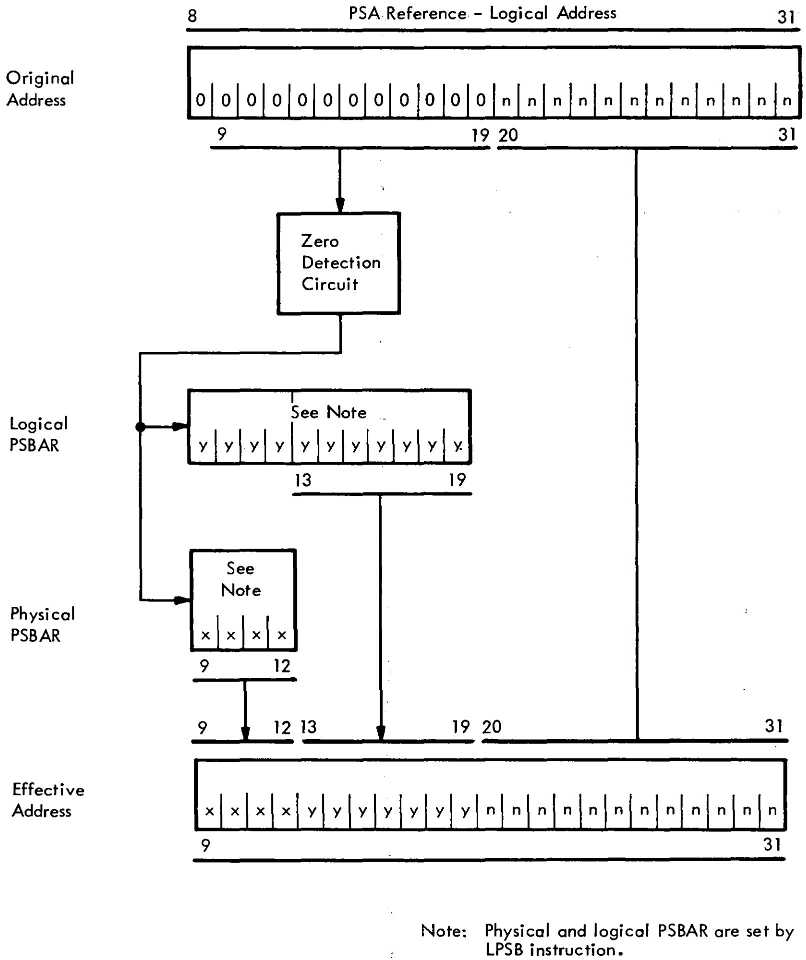


Figure 5-22. Effective PSA Address Generation

the word fetched by the instruction must specify word boundary addressing. A violation of any of these conditions causes a specification check and suppression of the operation.

A test is conducted to determine if bit positions 8–19 specify a location within an SE configured to communicate with the CE executing the instruction. A prerequisite to this test is the presence of the SE's identifier character in the ATR. This identifier must be in the ATR location corresponding to the logical address indicated by bits 8–19. If this ATR position does not contain a valid identifier, or if that SE is not configured, the LPSB instruction is terminated with a specification type program interrupt.

If the above test is successful, positions 8–19 are loaded into the logical PSBAR. The physical PSBAR is also set with the identifier character located in the ATR position indicated by 9–12 of the logical PSBAR (Figure 5-21).

The content of physical PSBAR is retained until it is replaced by another LPSB instruction, an IPL, a PSW restart, an external start, or a condition which causes PSBAR stepping.

Store PSBA Instruction (SPSB)

- SI format.

- Valid only in supervisory state and 9020 mode.

- Stores both the logical and physical PSBA.

The store PSBA instruction is in SI format; the I2 field (positions 8–15) is ignored. The instruction can only be executed in supervisory state and 9020 mode, and the effective address of the storage reference must specify word boundary addressing. A violation of any of these conditions causes a specification check and a suppression of the operation.

The current logical and physical PSBAs are both stored by the SPBA instruction. The logical PSBA is stored in positions 8–19; the physical PSBA is stored in positions 28–31; and positions 0–7 and 20–27 are set to 0's (Figure 5-24).

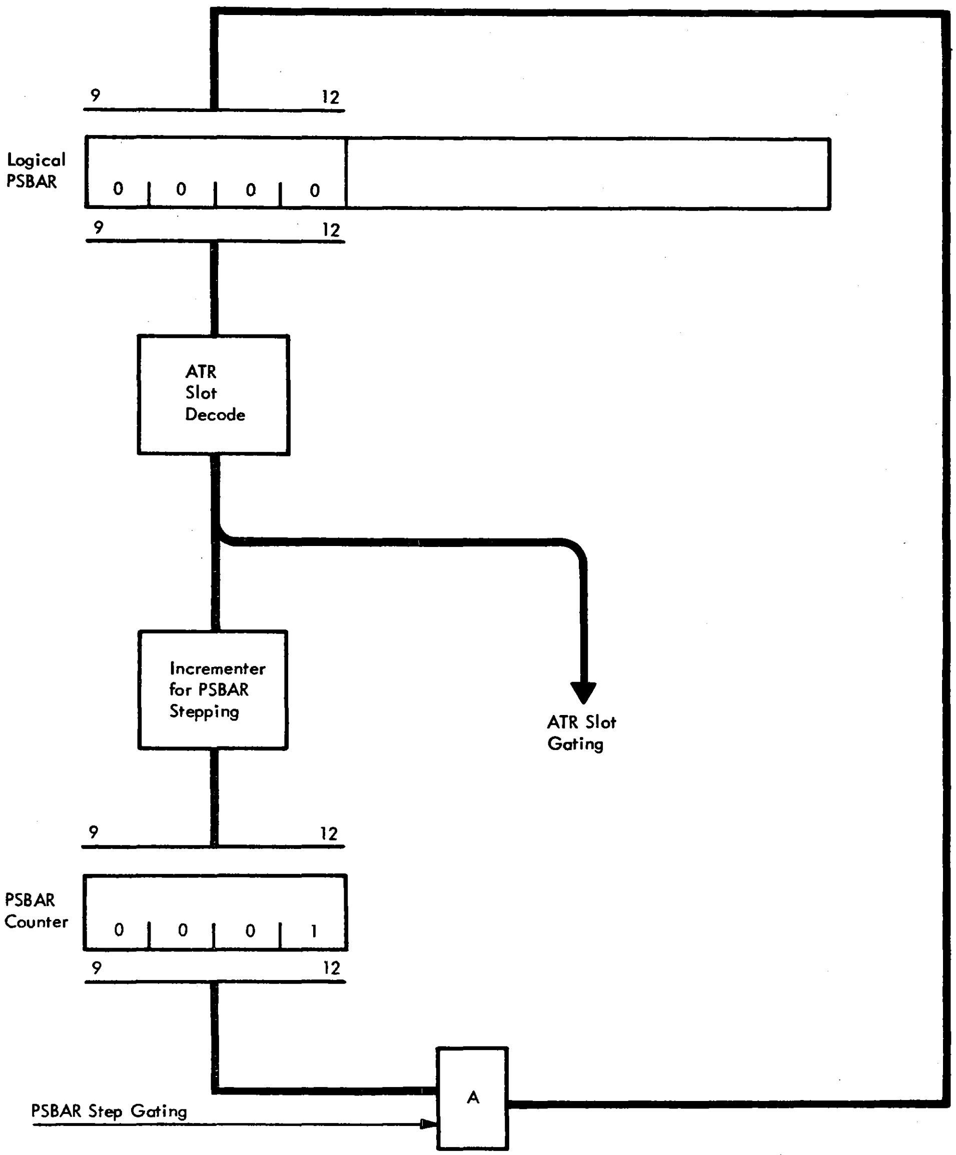


Figure 5-23. PSBAR Counter

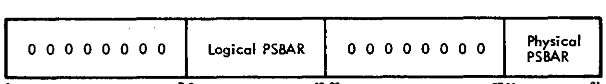


Figure 5-24. Storing of Logical and Physical PSBAR

Positions 9–12 of the logical PSBAR represent the current value of the PSBAR counter (including any stepping). The original value of 9–12 prior to stepping can be determined by examining the original LPSB instruction.

Operational Characteristics of PSBAR

Whenever the high-order 12 bits of a storage address are all zero, PSBAR is used to access storage. The low-order 12 bits which remain are sufficient to code addresses up to 4096. Thus, PSBAR establishes a block of 4096 bytes which may be anywhere in storage on 4096-byte boundaries. Since the normal contents of a PSA (PSWs, CAW, CSW, timer, and logout area) do not require 4096 bytes of storage, the operational programmer may use the remainder in any fashion. The program will always be able to locate information placed there since PSBAR will automatically be used when the high-order 12 bits of the address are zero. Only the relative location in the PSA is required.

Each operational CE in the system should have a unique PSA at all times. For maximum safety in the event of a storage malfunction, the PSA for each CE should be in a different SE. The automatic PSBAR stepping capability of the 9020 system imposes some restrictions on certain blocks of storage. Of course, a primary PSA area must be established in some 4096-byte block of storage. An alternate PSA area must also be established in the next configured SE. The alternate PSA must reside in the same relative 4096-byte block as does the primary PSA, as the PSBAR stepping capability steps in 524,288-byte (1 SE) increments. Thus, if the primary PSA is located in the highest 4096-byte block in its SE, the alternate PSA must occupy the highest 4096-byte block in its SE.

A further consideration in the multiprocessing environment is the necessity of placing a PSA in a location other than the lowest block of available storage. If this is not done, it may become impossible for one processor to access another processor's PSA, thus precluding this useful means of communication between CEs. The reason for this is that if one CE has its PSA in the lowest block of available storage and another CE attempts to access that PSA, the second CE will, instead, access its own PSA. This is because the low address causes the second CE's zero detect circuitry to force a PSBAR access, thus relocating the actual access to the location specified by PSBAR.

An additional consideration in establishing primary and secondary PSAs is the fact that each CE must have a unique PSA even after switching to alternate PSAs. For this reason, no primary or alternate PSA can occupy the same storage segment as any other primary or alternate PSA. To maintain this condition when an additional SE becomes available, or when an SE is lost to the system, may require some rearranging of primary and alternate PSA relationships.

PSA Example No. 1

Initially, a CE is configured to communicate with SE 1 and SE 3 [Figure 5-25(a)]. The primary PSA is in SE 1 and the alternate PSA is in SE 3. Any stepping of the PSBAR counter will pass over SE 2 and find SE 3 as the next configured (alternate) SE in the system.

At some point in the operation, SE 2 is added to (configured into) the system. Stepping of the PSBAR counter under these conditions finds SE 2 as the next configured SE. Two courses of action are possible: the alternate PSA can be relocated into SE 2, or the ATR can be set up to make SE 3 the higher (alternate) SE. In Figure 5-25(b), the CCR and ATR settings are such that any

No. 1 Computing Element

	State		SCON			SE										CE			IOCE		
CCR	S 0	S 1	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3	1	2	3
	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0

	SE									
ATR	1	2	3	4	5	6	7	8	9	10
	1	0	3	0	0	0	0	0	0	0

Alternate PSA

Primary PSA

(a) Initial Configuration

No. 1 Computing Element

	State		SCON			SE										CE			IOCE		
CCR	S 0	S 1	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3	1	2	3
	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0

	SE									
ATR	1	2	3	4	5	6	7	8	9	10
	1	3	2	0	0	0	0	0	0	0

Alternate PSA

Primary PSA

(b) Later Configuration

Figure 5-25. PSA Example No. 1

references to SE 2 are actually sent to SE 3. In this manner the secondary PSA areas need not be relocated in the next system.

The change in ATR must be performed quickly after reconfiguration because the system is endangered. The system elements are normally placed in a wait state during the time of change in configuration and address translation. If the elements were not stopped, data transfers could be split between two SEs, and PSA references could be directed to an SE where no PSA information exists.

PSA Example No. 2

Initially, a CE is configured to SEs 1, 2, and 3 [Figure 5-26(a)]. The primary PSA is in SE 2 and the alternate PSA is in SE 3. Any stepping of the PSBAR counter to an alternate PSA immediately finds SE 3 configured to the system.

At some point in the operation, SE 3 is removed from (reconfigured out of) the system. In this case, the alternate PSA that was in SE 3 had to be relocated into SE 1. By changing the ATR, references to logical SE 3 can be directed to physical SE 1. Any stepping of the PSBAR counter from SE 2 sets the physical PSBAR to SE 1 where the alternate PSA is now located. Any normal data references to logical SE 3 will also be directed to SE 1 [Figure 5-26(b)].

The PSA relocation must be performed as soon as possible (preferably before the unavailability of SE 3) because the system is without an alternate PSA during this time. If PSBAR were incremented during this interval, non-PSA information contained in SE 1 would be interpreted as control information. Note also in Figure 5-26(b) that the absence of a configured SE in ATR slot 1 causes the lowest 524,288-byte block of address to be interpreted as invalid. This might render the configuration less desirable than the original one, depending on the program.

After PSBAR steps automatically to the alternate PSA, the 'PSA alternate' latch is set, and further stepping is inhibited until a new alternate PSA can be set up in the appropriate SE. This latch is reset when a Load PSBA instruction is issued.

Because PSBAR can be loaded by the program, it is assumed that appropriate primary and alternate PSAs will have already been set up any time the PSBAR setting is changed. Further, the alternate PSA should be recognizable to the program as an alternate PSA, via some appropriate coding, so that action can be undertaken to deal with the cause of the PSBAR stepping.

No. 1 Computing Element

	State		SCON			SE										CE			IOCE		
CCR	S0	S1	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3	1	2	3
	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0

	SE									
ATR	1	2	3	4	5	6	7	8	9	10
	1	2	3	0	0	0	0	0	0	0

Alternate PSA
Primary PSA

(a) Initial Configuration

No. 1 Computing Element

	State		SCON			SE										CE			IOCE		
CCR	S0	S1	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3	1	2	3
	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0

	SE									
ATR	1	2	3	4	5	6	7	8	9	10
	0	2	1	0	0	0	0	0	0	0

Alternate PSA
Primary PSA

(b) Later Configuration

Figure 5-26. PSA Example No. 2

IOCE PSBAR

- PSBAR is a 12-bit register in IOCE.
- IOCE cannot step PSBAR.
- Two types of PSA accesses.

The PSBAR in the IOCE is a 12-bit register (bit 8 is included). In normal operation, PSBAR is set whenever updated PSBAR data is sent to the IOCE from the CE for I/O instructions, IPL, FLT load, and 'permit I/O' or 'MC interrupt'. PSBAR contents are gated from IOCE to SE during an IOCE PSA access. PSBAR always specifies the physical storage to be accessed; hence, it is not translated in the ATR. This is the same as CE operation. However, no provision is made for PSBAR stepping in the IOCE. The PSBAR obtains its setting from the CE and retains it until it is updated by new information on the CE-to-IOCE control bus.

Two types of PSA accesses are processed in the IOCE. The first includes all PSA operations, except IPL and FLT load and confines the accesses to the PSA in the specified SE. High-order address bits (9–19) are specified by PSBAR. Bits 20–31 are passed through the normal path from 'adder out bus' (AOB) latches to the storage address register (SAR). The second type of PSA access, found in IPL and FLT load, allows the IOCE to access any address within the SE specified by PSBAR. Bits 9–12 are specified by PSBAR; bits 13–31 are passed through the normal AOB to SAR path.

- Re-entrant coding.
- Special multiprocessing instructions.
- Special hardware for multiprocessing operations.

The 9020D central computer complex is a true multisystem organization in that it consists of two or more processing units which intercommunicate without manual intervention. It is capable of operating in a multiprogramming or a multiprocessing mode. In a multiprogramming type of operation, two or more programs are handled by running portions of each in an interleaved fashion. In a multiprocessing operation, however, more than one processor is available so that two or more programs may be running simultaneously or, conceivably, two processors could be simultaneously processing data using the same instruction coding from the same storage location. It is because of this latter possibility that much of the coding in the EXC program and the diagnostic monitors is "re-entrant". Re-entrant means that the coding may be accessed by two or more processors simultaneously without the actions of one processor interfering with the actions of the other. For example, in this type of coding, execution of the instructions must not alter the instructions in storage for this would interfere with execution by other processors.

This type of coding is not possible in all cases, however. Further, data being accessed by one processor must somehow be protected from the actions of other processors. For these reasons, in a multiprocessing environment certain facilities must be provided to enable the operation of the processors to proceed without interfering with each other and in such a manner that each can bear its share of the processing load.

The 9020 system is a dynamically reconfigurable multisystem capable of adjusting to variations in workload and of accommodating single element malfunctions without manual intervention. This capability depends largely on the EXC program, and on a number of features which make an integrated multiprocessing operation possible. These are:

1. Special multiprocessing instructions.
2. An elaborate system of intercommunication among the major elements.
3. An interruption-handling capability.
4. Special registers and hardware designed for operation in a multiprocessing environment.

Previous chapters have described how the reconfiguration capability is implemented and how storage may be assigned to different processors. Further, it has been shown that storage may be shared by more than one CE or IOCE. In this chapter, the special instructions which make multiprocessing possible are discussed, as is the manner in which the shared-storage and reconfiguration capability fit into the overall multisystem operation. The 9020 interrupt capability is discussed here because it makes possible intercommunication between programs, coordination of independent but concurrent system functions, and overall system monitoring of errors and abnormal conditions. This latter aspect of interruptions is enlarged upon in Chapters 7 and 8.

Two multiprocessing instructions, Write Direct (WRD) and Read Direct (RDD), are discussed first. These instructions and the associated hardware fall under the heading of "direct control", a facility which permits direct communication between processors.

DIRECT CONTROL

- CE direct control uses WRD and RDD instructions.
- IOCE processor direct control uses the WRD instruction.
- External signals are from: CE-CE, CE-IOCE, and IOCE-CE.

CE direct control provides Write Direct (WRD) and Read Direct (RDD) instructions for communication by CEs. IOCE processor direct control uses the WRD instruction to communicate from an IOCE to a CE.

Associated with direct control instructions are interface lines on which signals are made available. A signal from one CE may be connected to another CE or IOCE to cause an external interruption or other automatic operation. The direct control feature also provides static signals in the form of a communication byte that can be sent between two CEs.

CE direct control instructions may be validly executed only when the CE is in the supervisor state. IOCE processor direct control instructions can be executed in the problem state.

CE Write Direct Instruction (WRD)

- SI format.
- Eight coded commands.

The Write Direct instruction of the 9020 system can issue eight commands when executed by a CE:

1. To communicate between CEs.
2. To cause an external start of a CE.
3. To cause an automatic logout of a CE.
4. To cause an automatic logout of an IOCE.
5. To cause another CE to reset and go to the stopped state.
6. To stop an IOCE processor operation.
7. To start an IOCE processor after it has been stopped.
8. To cause an external interrupt of an IOCE processor.

Figure 6-1 summarizes the use of the I2 field of a CE WRD instruction for operations and element selection. Only one CE or IOCE may be selected by bits 12–15 of the I2 field. Honoring of these commands depends on the status of each receiving element. A CE accepts a logout, external start, or external stop if the proper CE communication bits are on in its CCR. Data communication is accepted if the proper CE field bits (20–23) are on. An IOCE honors a logout only if the corresponding SCON bit is on in its CCR.

Definition	Operation				Element Selection			
	8	9	10	11	12	13	14	15
Data Communication (CE-to-CE Data Transfer)	0	0	0	0				
CE External Start	0	0	0	1				
CE Logout	0	0	1	0				
IOCE Logout	0	0	1	1				
CE External Stop	0	1	0	0				
IOCE-Processor Start	0	1	0	1				
IOCE-Processor Stop	0	1	1	0				
IOCE-Processor Interrupt	0	1	1	1				
Invalid	1	x	x	x				
CE/IOCE 1					1	0	0	0
CE/IOCE 2					0	1	0	0
CE/IOCE 3					0	0	1	0
CE 4					0	0	0	1

Figure 6-1. I2 Field Definition for CE WRD Instruction

A wraparound feature, intended for maintenance of CEs, is also included in the WRD and RDD instructions. A CE can respond to all commands that it initiates, provided it is configured to listen to itself.

Data Communication Command

- CE-to-CE communication.
- Selected CE is interrupted.
- Gated by CE bit in CCR.

The byte at the location specified by the operand address is made available as a set of direct-out static signals which remain static until the next Write Direct instruction is executed. A Read Direct instruction at the receiving CE is used to read the data byte.

This type of communication can be used to direct the course of another CE. The byte of information, for example, might be a coded representation of a subroutine or operation to be performed by the element.

CE External Start Command

- Causes receiving CE to start.
- Only one CE may be selected per WRD.
- Gated by SCON bit.

The WRD external start operation can only be issued to one CE during each WRD instruction. Multiple bits in the I2 field (12–15) will cause a specification check.

The external start signal will be accepted by the CE only if it is SCONed to the sending CE. If properly SCONed, the receiving CE obtains a new PSW from location zero of its PSA and proceeds to execute the program indicated by the PSW address.

CE Logout Command

- Causes receiving CE to initiate a logout.
- Only one CE may be selected per WRD.
- Gated by SCON bit.

The WRD CE logout signal can be issued to only one CE during each WRD instruction. Multiple bits in the I2 field (12–15) will cause a specification check.

The logout signals are accepted by the CE only if it is SCONed to the sending CE. If properly SCONed, the receiving CE will commence logging out into the PSA indicated by its own preferential storage base address register (PSBAR).

IOCE Logout Command

- Causes receiving IOCE to initiate logout.
- Only one IOCE can be selected per WRD.
- Gated by communication bit.

The WRD IOCE logout signal can be issued only to one IOCE during each WRD instruction. Multiple bits in the I2 field cause a specification check.

The logout signal is accepted by the IOCE only if the communication bit for the requesting CE is set on in the IOCE's CCR. If the correct communication bit is set, the receiving IOCE will commence logging out into the PSA indicated by the sending CE.

Each of the preceding CE and IOCE logouts would probably be issued due to some type of element failure indication (i.e., element check). After the logout is completed, the controlling CE can analyze the data and determine the course of action necessary from that point.

CE External Stop Command

- Causes the selected CE to reset and go to the stopped state.

The CE External Stop command permits a CE to raise the 'external stop' line to a selected CE. At the end of the current instruction, the selected CE changes from the operating, wait, or check-stop state to the stopped state. The selected CE is reset and all pending interruptions are eliminated. Stopped state is indicated by the manual light on the SC and CE control panel.

The receiving CE must have the issuing CE's SCON bit on and it must be the only CE selected.

IOCE-Processor Stop Command

- Causes the selected IOCE processor to go to the stopped state.

The IOCE Processor Stop command permits a CE to raise the 'IOCE processor stop' line to a selected IOCE. At the end of the current IOCE instruction, the IOCE processor changes from the running or wait state to the stopped state. Interruptions remain pending but the timer is not updated in the stopped state.

For the Stop command to be effective, the IOCE processor must have its communication bit for the requesting CE set in the configuration control register (CCR) of the IOCE.

IOCE-Processor Start Command

- Causes the selected IOCE processor to leave the stopped state.

The IOCE Processor Start command permits a CE to raise the 'IOCE processor start' line to a selected IOCE. The IOCE processor immediately changes from the stopped state to either the running or the wait state, depending on the setting of PSW bit 14 in the IOCE processor. If bit 14 is off, an instruction is fetched from the location specified by the instruction address register (IAR).

For the Start command to be effective, the IOCE processor must have its communication bit for the requesting CE set in the CCR of the IOCE.

IOCE-Processor Interrupt Command

- Causes an external interruption request to be presented to a selected IOCE processor.

The IOCE Processor Interrupt command permits a CE to raise the 'IOCE processor interrupt' line to a selected IOCE. The interruption is taken if PSW bit 7 in the IOCE processor is a 1 and the processor is in the running or wait state; otherwise, the interrupt remains pending.

For this command to be effective, the IOCE processor must have its communication bit for the requesting CE set in the CCR of the IOCE.

Read Direct Instruction (RDD)

- SI format.
- Reads data sent by WRD instruction.
- Interrupts selected CE.

The RDD instruction is used to read the data transmitted by means of a WRD instruction during CE-to-CE communication. A direct-in data byte is placed in the location specified by the RDD operand address. Only one byte of data can be read in on each RDD instruction.

The RDD instruction accepts the data byte if the hold-in line is inactive, indicating that the byte is static. If the hold-in line is active for more than 4 usec, the RDD instruction terminates with a machine-check interrupt. Bit 29 of the PSW interrupt condition code is set to identify the interruption. No logout occurs.

As an indication that the data byte has been accepted, the RDD instruction causes an external interrupt at the selected CE by setting a corresponding bit in its external interrupt register.

IOCE Processor Write Direct Instruction (WRD)

- SI format.
- One command: CE external interrupt.
- Bits 8–11: 1000.

The IOCE WRD instruction permits the IOCE processor to request an external interrupt in the controlling CE by raising a processor interruption line to the CE. The IOCE requesting the interrupt is identified in a processor interruption register (PIR) in the CE.

This command is effective only if the IOCE has its communication bit for the controlling CE set in the CCR of the IOCE. Bit 7 of the PSW in the controlling CE must be on.

Direct Control Example

Figure 6-2 shows simplified representations of the CCRs of the CEs and IOCEs in a typical system. These are shown as they might be configured into three subsystems: the ATC subsystem in state three, a secondary subsystem in state two; and a maintenance subsystem in state zero.

In this example CE 1 is the only CE which can reconfigure the system; it is the only one in state three. CE 1 also executes the EXC program which is engaged both in the active ATC problem and in monitoring the secondary and maintenance subsystems.

Even though this example may not be a completely practical one, the settings of the various CCRs will point out important points of the direct control feature.

Data Communication

All three CEs can initiate a WRD or RDD operation provided they are in the supervisory state. In Figure 6-2, for example, CE 1 may initiate a WRD data communication operation to both CE 2 and CE 3. CE 2 has the CE 1 bit on in its CCR. CE 2 will, therefore, have its external interrupt register set and, if PSW mask bit 7 is on, will experience an external interrupt at the end of its current instruction. If the mask bit is off, the interrupt will be retained and delayed until bit 7 is set on by the monitor program. CE 2 may, in turn, issue an RDD instruction to CE 1. CE 1 acknowledges this RDD because the CE 2 bit is on in its CCR. CEs 1 and 2 can, therefore, effectively communicate with each other.

CE 1 issuing a data communication to CE 3 will be completely ignored by CE 3. CE 3 has been configured not to listen to CE 1 in this respect and will not have the external register set with any indication. In a similar manner, CE 1 will completely ignore any WRD or RDD data communication operations from CE 3. CEs 1 and 3, in this case, have no data communication abilities with each other.

Any such operations directed to an IOCE will be ineffective; data byte signals are not available at the inputs of the IOCEs.

CE External Start

CE 1 can initiate an external start to both CE 2 and CE 3, both of which are SCONed to listen to CE 1.

An external start to CE 2 is the more practical case. State two operations are assumed to be under tight monitor control. Therefore, it is quite likely that CE 1 could load SE 5 with the program for CE 2 to execute, load a proper PSW into location 00000 of SE 5, and issue an external start. At this point, CE 2 would load the PSW into its internal registers and begin executing the program indicated by the instruction address in PSW (40–63).

An external start could be issued by CE 2 and CE 1 if in supervisor state; but, because CE 1 is the controlling CE, it is not SCONed to accept an external start operation from a lower CE. By being able to ignore such operations as SCON and external start, for example, the EXC program is assured full control of the system at all times.

In this example, then, CE 1 can force an external start on CE 2 and CE 3 but not vice versa.

CE Logout

The CE logout conditions and restrictions are similar to those of the external start operation just discussed; CE 1 can cause a logout in CE 2 and CE 3, but not vice versa. Because the PSA of CE 2 is most likely to be in the first SE indicated in the CCR of CE 2, the logout will place the logged-out data into SE 5.

The logout signal to CE 3 will log the data into SE 8. Logout in this case depends on the setting of the test switch on CE 3. The logout will be ignored if the test switch is on in state zero.

No. 1 Computing Element ●

		SCON			SE										CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3	1	2	3
1	1	1	0	0	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0

No. 2 Computing Element ■

		SCON			SE										CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3	1	2	3
1	0	1	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	1	0

No. 3 Computing Element ⧄

		SCON			SE										CE			IOCE		
S	S	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3	1	2	3
0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

No. 1 I/O Control Element ●

		SCON			SE										CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3
1	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0

No. 2 I/O Control Element ■

		SCON			SE										CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3
1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

No. 3 I/O Control Element ⧄

		SCON			SE										CE		
S	S	1	2	3	1	2	3	4	5	6	7	8	9	10	1	2	3
0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

● State Three ATC Subsystem

■ State Two Subsystem

⧄ State Zero Maintenance Subsystem

Figure 6-2. Direct Control Example

IOCE Logout

In Figure 6-2, each CE can log out the IOCE to which it is configured. Each IOCE is configured to listen to only one CE. Any other CE attempting to issue an IOCE logout will have its operation effectively NOPed.

In each of the above cases, only one CE has been assumed to be in state three performing the active ATC operation. In large systems and during peak periods of air traffic, two or more CEs could be in state three directly concerned with ATC. Under these circumstances the same restrictions prevail. The EXC program, however, must maintain close control over the setting of the communication bits in the CCRs of the active CEs.

INTERRUPTS

- Five major categories.
- Priority-sensitive.
- Maskable by the PSW in CE or IOCE processor.

Automatic program interruption provides a quick and efficient means of alerting the system to a variety of conditions. These interrupts can be grouped in five categories: Machine check, Program, Supervisor call, External, Input/output.

Some interrupts can be controlled (masked); others cause an unconditional interrupt as soon as the particular condition occurs. Masking is accomplished by placing specific bits in a PSW (Figure 6-3). A 0 bit in the mask position, for example, causes the particular interrupt to be suppressed (masked off); a 1 bit in the mask position allows the interrupt to be recognized (masked on).

Note that there are two types of PSWs: one in each CE and one in each IOCE processor. Their purpose is the same, although the functions of the IOCE processor PSW are

System Mask	Key	AMWP	System Mask	Interruption Code
0–7	8–11	12–15	16–19	20–31

ILC	CC	Program Mask	Instruction Address
32–33	34–35	36–39	40–60

SYSTEM MASK

0	Multiplexer Channel 0
1	Selector Channel 1
2	Selector Channel 2
3	Selector Channel 3
4	Multiplexer Channel 4
5	Selector Channel 5
6	Selector Channel 6
7	External (Timer, Interrupt Switch, External Signals)
16	Selector Channel 7
17	Multiplexer Channel 8
18	Selector Channel 2
19	Selector Channel A

AMWP FIELD

13	Machine Check Mask

PROGRAM MASK

36	Fixed-Point Overflow
37	Decimal Overflow
38	Exponent Underflow
39	Significance

Figure 6-3. CE Program Status Word Mask Bits

slightly limited. Interrupts pertaining to the CE are discussed first.

Associated with each of the five types of interrupts are "old" and "new" PSWs. These PSWs are located in permanent storage assignments within the particular PSA as shown in Figure 6-4. The location of the PSA is determined by the base address in each CE. Therefore, different preferential areas can be assigned to each CE within the system. All addresses generated automatically by the CE are constructed using the current value in the PSBAR.

Hex Loc	Length	Purpose	Dec Loc
0	Doubleword	Initial Program Loading PSW	0
8	Doubleword	Initial Program Loading CCW1	8
10	Doubleword	Initial Program Loading CCW2	16
18	Doubleword	External Old PSW	24
20	Doubleword	Supervisor Call Old PSW	32
28	Doubleword	Program Old PSW	40
30	Doubleword	Machine Check Old PSW	48
38	Doubleword	Input/Output Old PSW	56
40	Doubleword	Channel Status Word	64
48	Word	Channel Address Word	72
4C	Word	Unused	76
50	Word	Timer	80
54	Word	Unused	84
58	Doubleword	External New PSW	88
60	Doubleword	Supervisor Call New PSW	96
68	Doubleword	Program New PSW	104
70	Doubleword	Machine Check New PSW	112
78	Doubleword	Input/Output New PSW	120
80		Diagnostic Logout Area	128

Figure 6-4. Permanent Preferential Storage Assignments

The old PSW preserves the essential machine status conditions at the time of the interrupt, and provides an interrupt code to indicate the cause of the interrupt. Also included in the old PSW is an instruction length code which indicates the length of the instruction executed just prior to the interrupt. A list of the various interrupts and their corresponding interrupt codes is shown in Figure 6-5.

The new PSW establishes the new machine modes, states, masking, and instruction addressing necessary to proceed properly into the particular interrupt routine.

During the execution of an instruction, several interrupt requests may occur simultaneously. These simultaneous requests are honored according to the following priority:

1. Machine check
2. Program or supervisor call
3. External
4. Input/Output

Program and supervisor call interruptions have the same priority because they are mutually exclusive; i.e., both cannot occur at the same time.

With the exception of the delay instruction, an interruption occurs when the preceding instruction is finished and the next instruction is not yet started. The manner in which the preceding instruction is finished may be influenced by the cause of the interruption. The instruction may have been completed, terminated, or suppressed.

Machine-Check Interrupt

- CE machine-check interrupts.
- IOCE machine-check interrupts.
- Maskable by PSW (13).

A machine-check interrupt can occur because of machine checks from within both the CE and configured IOCE, and assumes priority over the other four categories of interrupt. The machine-check interrupt is maskable by position 13 of the current PSW.

CE Machine-Check Interrupt

- CE malfunction.
- Read Direct timeout.
- Maskable by PSW (13).

Interrupt Source Identification	Interruption Code PSW Bits 20-31	Mask Bits	ILC	Instruction Execution
CE Malfunction	0000 00000000	13	x	Terminated
IOCE 1 Malfunction	0000 00000001	13	x	Completed
IOCE 2 Malfunction	0000 00000010	13	x	Completed
IOCE 3 Malfunction	0000 00000011	13	x	Completed
Read Direct Timeout	0000 00000100	13	x	Completed
(a) Machine Check interrupt (old PSW - 30 hex; new PSW - 70 hex; priority 1)				
Operation	0000 00000001	-	1,2,3	Suppressed
Privileged Operation	0000 00000010	-	1,2	Suppressed
Execute	0000 00000011	-	2	Suppressed
Protection	0000 00000100	-	0,2,3	Suppressed/Terminated
Addressing	0000 00000101	-	0,1,2,3	Suppressed/Terminated
Specification	0000 00000110	-	1,2,3	Suppressed
Data	0000 00000111	-	2,3	Terminated
Fixed-Point Overflow	0000 00001000	36	1,2	Completed
Fixed-Point Divide	0000 00001001	-	1,2	Suppressed/Completed
Decimal Overflow	0000 00001010	37	3	Completed
Decimal Divide	0000 00001011	-	3	Suppressed
Exponent Overflow	0000 00001100	-	1,2	Terminated
Exponent Underflow	0000 00001101	38	1,2	Completed
Significance	0000 00001110	39	1,2	Completed
Floating-Point Divide	0000 00001111	-	1,2	Suppressed
IOCE 3 PSA Lockout	0000 00010000	-	1,2,3	Terminated/Completed
IOCE 2 PSA Lockout	0000 00100000	-	1,2,3	Terminated/Completed
IOCE 1 PSA Lockout	0000 01000000	-	1,2,3	Terminated/Completed
Logout Stop	0000 10000000	-	1,2,3	Suppressed/Terminated
(b) Program Interrupt (old PSW - 28 hex; new PSW - 68 hex; priority 2)				
Instruction Bits	0000 rrrrrrrr	-	1	Completed
(c) Supervisor Call Interrupt (old PSW - 20 hex; new PSW - 60 hex; priority 2)				
DAR	xxxx xxxxxxx1	7	x	Completed
PIR (IOCE-Processor)	xxxx xxxxxx1x	7	x	Completed
CE 4 Write Direct	xxxx xxxx1xxx	7	x	Completed
CE 3 Write Direct	xxxx xxx1xxxx	7	x	Completed
Interrupt Switch	xxxx x1xxxxxx	7	x	Completed
Timer	xxxx 1xxxxxxx	7	x	Completed
CE 2 Write Direct	xxx1 xxxxxxxx	7	x	Completed
CE 2 Read Direct	xx1x xxxxxxxx	7	x	Completed
CE 1 Write Direct	x1xx xxxxxxxx	7	x	Completed
CE 1 Read Direct	1xxx xxxxxxxx	7	x	Completed
(d) External Interrupt (old PSW - 18 hex; new PSW - 58 hex; priority 3)				
Multiplexer Channel 0	0000 aaaaaaaa	0	x	Completed
Selector Channel 1	0001 aaaaaaaa	1	x	Completed
Selector Channel 2	0010 aaaaaaaa	2	x	Completed
Selector Channel 3	0011 aaaaaaaa	3	x	Completed
Multiplexer Channel 4	0100 aaaaaaaa	4	x	Completed
Selector Channel 5	0101 aaaaaaaa	5	x	Completed
Selector Channel 6	0110 aaaaaaaa	6	x	Completed
Selector Channel 7	0111 aaaaaaaa	16	x	Completed
Multiplexer Channel 8	1000 aaaaaaaa	17	x	Completed
Selector Channel 9	1001 aaaaaaaa	18	x	Completed
Selector Channel A	1010 aaaaaaaa	19	x	Completed
(e) Input/Output Interrupt (old PSW - 38 hex; new PSW - 78 hex; priority 4)				

Legend

a Device Address bits
r Bits of R1 and R2 field of Supervisor Call instruction
x Unpredictable

Figure 6-5. CE Interrupt Actions

A machine check in the CE can result from many internal sources such as serial or parallel adder half-sum, full-sum, and carry errors and parity errors at the various byte counters and registers. When this type of error occurs, the present instruction is terminated and an element check (ELC) pulse is unconditionally sent to all other CEs within the system.

As a result of the interrupt, the state of the CE is logged out into the PSA starting with location 80 hex and extending through as many words as the CE requires. The old PSW is stored in location 30 hex of the PSA with an interrupt code of zero. The new PSW is fetched from location 70 hex. Proper execution of these steps depends upon the nature of the machine check.

A RDD timeout condition causes a machine-check interruption. The instruction is not terminated, and no logout occurs when the machine-check interrupt results from this condition. The interrupt code is set to four (100) to identify the RDD timeout condition as the cause of the interrupt [Figure 6-5(a)]. RDD timeout is the result of the direct-in lines being busy for too long a time during an RDD instruction. This busy condition is normally imposed on the lines during the time data is being changed by another CE executing WRD. An excessive delay before busy drops, however, results in the timeout condition.

All machine checks are maskable by position 13 of the current PSW. If the machine check mask bit is 0, an attempt is made to complete the current instruction and proceed with the next sequential instruction.

IOCE Machine-Check Interrupt

- IOCE malfunction.
- Interrupt code identification.
- Maskable by PSW (13).

The IOCE machine-check interrupt requests to the CE are maskable by the CE's current PSW (13). When a machine check occurs, the IOCE issues an ELC to all CEs. At the same time, the IOCE initiates diagnostic procedures within itself and then issues a machine-check interrupt request to the configured CE. All instructions, with the exception of I/O instructions, are completed before the interrupt request is acknowledged. I/O instructions are terminated upon receipt of a machine-check request.

Program Interrupt

- Normal CE program interrupts.
- IOCE PSA lockout condition.
- Logout stop condition.
- Partially maskable by PSW (36–39).

Program interrupts occur primarily because of an improper specification or improper use of instructions or data. These interrupts include a logout stop condition from the CE, and an IOCE PSBAR lockout condition for each of the three IOCEs. Specific interrupt code bits in the old PSW define the cause of each program interrupt [Figure 6-5(b)]. Note that only four of the program interrupts are maskable by means of positions 36–39 of the current PSW.

Supervisor-Call Interrupt

- Not maskable.

The supervisor-call interrupt occurs as a result of executing the Supervisor Call (SVC) instruction. The SVC may be executed in problem state and, as the name implies, has the primary purpose of switching from problem state to supervisor state.

The contents of bit positions 8–15 of the SVC instruction become bits 24–31 of the interrupt code of the SVC old PSW. Through use of this instruction, a program written in problem state can convey a message or request to the control program which is written in supervisor state [Figure 6-5(c)].

External Interrupts

- Timer interrupt.
- Console interrupt.
- Direct control interrupt.
- DAR interrupt.
- PIR interrupt.
- Maskable by PSW (7).

External interrupts, for the most part, originate from signals or actions external to the particular CE. These sources would include interrupts caused by the operator's console INTERRUPT pushbutton, direct control operations, and abnormal condition signals set into the diagnose accessible register (DAR) by other major elements within the system. Interrupts which might not actually be considered external include the timer interrupts and certain conditions of the DAR. At any time in an IOCE processor operation, the IOCE can present an external interrupt to the controlling CE. The identification of the interrupting IOCE processor is saved in a processor interrupt register (PIR), and an external PIR interrupt is initiated.

External interrupts are under control of PSW (7). An external interrupt request may occur at any time, and several different requests may occur simultaneously. The requests are preserved until honored by the CE. When the external interrupt occurs, all pending requests are presented simultaneously and identified by unique code bits in the old PSW [Figure 6-5(d)].

Timer Interrupt

- Timer located in location 50 hex of PSBA.
- Maskable by PSW (7).

The timer occupies a 32-bit word at location 50 hex of the CE's PSA. Its setting may be changed at any time by storing a new value in location 50 hex. In this manner, the timer can serve as a real-time clock and as an interval timer.

The timer contents are reduced by 1 in positions 21 and 23 every 1/60 of a second (line frequency). The interruption is initiated as the count proceeds from a positive to a negative number, and is identified by position 24 of the interrupt code in the old PSW [Figure 6-5(d)].

The timer is not updated when the CE is in the stopped state, or when the CE is in state zero with the disable interval timer switch on.

Console Interrupt

- Operator intervention at CE.
- Can also be initiated from the SC.
- Maskable by PSW (7).

A console interrupt permits operator intervention with the system. These interrupts are maskable by position 7 of the current PSW and are identified by position 25 of the interrupt code in the old PSW [Figure 6-5(d)].

The console is further conditioned by the CE INTERLOCK switch and state bits. When in state two or three, the console INTERLOCK switch must also be used in conjunction with the INTERRUPT pushbutton. In states zero and one, however, the pushbutton is active without the need of the interlock switch. An interrupt can also be initiated from the SC provided the CE is not in state zero with the test switch on.

The IOCE also has a console INTERRUPT pushbutton which is maskable by its current PSW. The pushbutton is only usable in the IOCE when in state one and diagnostic mode, or when in state zero.

Direct-Control Interrupts

- Read direct and write direct.
- Under control of CE's CCR (20–23) and CCR (29–31).
- Maskable by PSW (7).

Each CE has the ability to acknowledge both RDD and WRD interrupt signals from other CEs within the system. Interrupt code bits 20–23 and 26–29 specifically indicate the RDD and WRD signals from CEs 1–4, respectively [Figure 6-5(d)]. A CE can also acknowledge a WRD interrupt signal from an IOCE processor. Bit 28, 29, or 30 in the PIR identifies the source of the interrupt as IOCE processor 1, 2, or 3.

Direct-control interrupts will not be accepted by the receiving CE if its CCR is not configured to listen to the sending CE or IOCE. If configured, the interrupt signal is accepted and retained until the interrupt occurs.

Abnormal Condition Signals

- Signals from major system elements.
- Set into DAR register.
- Individually maskable by the DAR Mask register.
- Collectively maskable by PSW (7).

The external interrupt capabilities of the CE are expanded by means of a 32-bit diagnose accessible register (DAR) to continually monitor abnormal condition signals from all CEs (including itself), SEs, IOCEs, PAMs, SCUs, and TCUs. This is discussed briefly here and more fully in Chapter 7.

Abnormal signals include: element checks (ELC), out-of-tolerance checks (OTC), and on-battery signal (OBS). Each system element has a corresponding position (or positions) in the DAR which continually monitors signals from the various elements [Figure 6-6(a)].

With the exception of ELCs from other CEs, each DAR position is maskable by a corresponding position in the receiving CE's DAR mask (DARM) register [Figure 6-6(b)].

Each IOCE is assigned two DAR bits to indicate:

(0, 0) Normal operation
(0, 1) On-battery signal (OBS)
(1, 0) Out-of-Tolerance check (OTC)
(1, 1) Element check (ELC)

IOCE 1		IOCE 2		IOCE 3		Storage ELC										Spare	Spare	PAM ELC			TCU ELC			SCU ELC			Other CE ELC/ CE Own OTC				CE Own OBS
a	b	a	b	a	b	1	2	3	4	5	6	7	8	9	10			1	2	3	1	2	3	1	2	3	1	2	3	4	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Note: Abnormal conditions from the IOCE's are encoded as follows:

a	b	Condition
0	0	Normal Condition
0	1	On Battery Signal (OBS)
1	0	Out of Tolerance Check (OTC)
1	1	Element Check (ELC)

(a) DAR Format

IOCE	Spare	IOCE	Spare	IOCE	Spare	Storage										Spare	Spare	PAM			TCU			SCU			Other CE/ Own OTC				CE Own OBS
1		2		3		1	2	3	4	5	6	7	8	9	10			1	2	3	1	2	3	1	2	3	1	2	3	4	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

(b) DAR Mask Register (DARM)

●Figure 6-6. Abnormal Condition Monitoring and Masking

The CE also has a bit to monitor its own OBS signal. Further, the CE's own OTC is indicated in the 'OTHER CE ELC/CE OWN OTC' field. For example, in CE 2, the CE 2 bit (bit 28) would indicate an OTC in CE 2 itself, while CE bits 1, 3, or 4 (bits 27, 29 or 30) would indicate an ELC in the corresponding CE. The SEs, PAMs, SCUs, and TCUs are each assigned one position to monitor ELC conditions, the specific meaning of which varies from one system element to another.

The acceptance of a bit into the DAR will, if properly masked by the DARM register, initiate an external interrupt. This interrupt is under further control of the current PSW (7) mask bit and places a bit (called the DAR bit) in position 31 of the interrupt code in the old PSW.

An element check from another CE has special significance in the overall system. In effect, this is a call for assistance from a malfunctioning CE to another CE within the system. The ELC condition is unconditionally set into the DAR but is only recognized if the receiving CE is SCONed to the sending CE. If not SCONed to the sending CE, the condition is remembered until SCONed or until the DAR is reset by subsequent diagnostic operations.

If the receiving CE is in state three, an external CE ELC is dealt with in the normal manner; i.e., is subject to gating by the SCON bit and masking by the appropriate DARM register position and PSW (7). If the receiving CE is in state two, one, or zero with the test switch off, however, the interrupt is dependent only on SCON gating; i.e., both DARM register and PSW (7) masking are ignored and the CE immediately assumes state three. At this point, the CE proceeds to assume program control of the system.

Input/Output Interrupts

- 11 channels on three IOCEs.
- Individually maskable by PSW.

I/O interrupts enable IOCEs to notify their controlling CE of special conditions concerning the attached I/O devices. A maximum of 11 channels can be attached to the 9020 system; each is maskable by specific bits in the controlling CE's current PSW [Figure 6-5(e)].

A request for an I/O interruption may occur at any time and more than one request may occur at the same time. The requests are preserved in the IOCE until accepted by the CE. Priority is established among requests so that only one interruption can be processed at a time.

IOCE Processor PSW and Interrupt Action

- Separate PSW in MACH storage.
- Limited interrupt handling.

As noted previously, the IOCE processor has its own PSW (Figure 6-7). This PSW is somewhat limited in comparison to the CE PSW. Since no I/O operations can be performed by the IOCE processor, the system mask consists of bit 7 only. Bit 7 permits masking of external interrupts. No machine-check masking is provided as machine checks are masked for the IOCE processor by the controlling CE. The

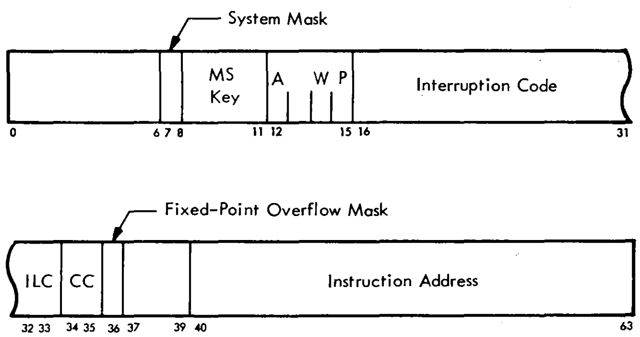


Figure 6-7. IOCE-Processor PSW

program mask consists of bit 36 only, the fixed point overflow mask bit. Because of the limited instruction set of the IOCE processor, bits 37–39 are not functional.

Figure 6-8 lists the interruptions active in an IOCE processor: program, supervisor call, external, and machine check. These PSWs are stored in MACH storage.

Machine-check masking comes from bit 13 of the PSW in the controlling CE. When a machine check originates in an IOCE processor, the Common Logic Unit (CLU) sets the appropriate bit in the check register, issues an element check, and performs a logout when permission to do so is received from the controlling CE. After the logout, the IOCE processor stores its machine check old PSW in MACH but does not load a new PSW. Instead, process mode turns off.

SHARED STORAGE

- Multiple CE or IOCE operation.

Many independent SEs exist within the 9020E system, and each may be configured to communicate with any one or all of the available CEs and IOCEs. Although the following discussion of shared storage is written from the viewpoint of the CE, storages are also shared by IOCEs. The examples of test and set and delay instructions apply to an IOCE as well as to a CE.

When two or more CEs are operating together to perform the ATC task, certain storage reference tables are created and used by the CEs to determine the status of their particular task. This shared storage contains common data, results, programs, and restart information, all of which are updated by the various operating CEs. With all of this interactivity, interlocks are essential to prevent other CEs from referring to the common data, tables, or instructions while one of the CEs is in the process of updating the information.

For example, if one CE attempts to update a storage location by executing an instruction that fetches data, updates it, and stores it back into the original location, it is possible for another CE, or an IOCE, to fetch or store data at that same location between the fetch and store cycles of the first CE. This would result in loss of the data stored by the second CE, or IOCE.

Several methods are available to synchronize these operations and place a "lock" on storage. One such method is through interrupts which can be programmed by direct-control instructions, Read Direct (RDD) and Write Direct (WRD). Coded data bytes can indicate the locking, unlocking, and testing of storage areas. In some cases, the immediate instructions (AND, OR, and Exclusive OR) can be effectively used to force the SE to give the executing CE two consecutive storage cycles before allowing any other unit to access that storage.

Another method of testing a storage area is the periodic program inspection of a particular storage location or bit position. The Test and Set instruction falls into this latter category.

Test and Set Instruction (TS)

- Executed by CEs or IOCEs.
- SI format.
- Tests storage availability.
- Sets "lock" on storage area.

The Test and Set (TS) instruction fetches the indicated byte from core storage and tests the leftmost bit (bit 0) of that byte for a 0/1 condition. As a result of this test, the condition code is set to 0 or 1. As the byte is returned to storage, all nine bits (including parity) are unconditionally set to 1's.

If the leftmost bit of the byte to be tested can be considered the lock, a 0 indicates an unlocked condition, and a 1 indicates a locked condition. Normally, a program would use the TS instruction only when it wished to operate with the storage area. Therefore, when the test is made and an unlocked (0 bit) condition is indicated, the area is immediately locked (reserved for the issuing CE) by setting the lock bit to a 1. The area is unlocked by storing a 0 in the lock bit by any one of a number of appropriate instructions.

For the TS instruction to be effective, the normal operation line must be inactive.

Test and Set Example

Assume that byte positions 5000–5199 are a common data or table area, and that byte position 5000 is considered the lock byte. Remember, however, that the size of the common area or the location of the lock byte is defined

Interruption Source Identification	Interruption Code PSW Bits 16-31	Mask Bits	ILC Set	Instruction Execution
PROGRAM (old PSW MACH 28 hex; new PSW MACH 68 hex; priority 2)				
Operation	0000 0000 00000001		1,2,3	Suppressed
Privileged Operation	0000 0000 00000010		1,2	Suppressed
Execute	0000 0000 00000011		2	Suppressed
Protection	0000 0000 00000100		0,2,3	Suppressed/ Terminated
Addressing	0000 0000 00000101		0,1,2,3	Suppressed/ Terminated
Specification	0000 0000 00000110		1,2,3	Suppressed
Data	0000 0000 00000111		2,3	Terminated
Fixed-pt. overflow	0000 0000 00001000	36	1,2	Completed
Fixed-pt. divide	0000 0000 00001001		1,2	Suppressed/ Completed
SE stopped	0000 0000 10000000		1,2,3	Suppressed/ Terminated
SUPERVISOR CALL (old PSW MACH 20 hex; new PSW MACH 60 hex; priority 2)				
Instruction bits	0000 0000 rrrrrrrr		1	Completed
EXTERNAL (old PSW MACH 18 hex; new PSW MACH 58 hex; priority 3)				
Unused	0000 0000 nnnnnnn1	7	x	Completed
Controlling CE	0000 0000 nnnnnn1n	7	x	Completed
Unused	0000 0000 nnnnn1nn	7	x	Completed
Unused	0000 0000 nnnn1nnn	7	x	Completed
Unused	0000 0000 nnn1nnnn	7	x	Completed
Unused	0000 0000 nn1nnnnn	7	x	Completed
Interrupt switch	0000 0000 n1nnnnnn	7	x	Completed
Timer	0000 0000 1nnnnnnn	7	x	Completed
MACHINE CHECK (old PSW MACH 30 hex; new PSW MACH 70 hex; priority 1)				
IOCE malfunction	0000 0000 00000000	13*	x	Terminated

Legend:

n Other external interruption conditions
x Unpredictable
r Bits of R_1 and R_2 field of Supervisor Call

*In CE PSW when operational mode; in IOCE-processor PSW when diagnostic mode.

Figure 6-8. IOCE-Processor Interrupt Actions

entirely by the program and is not restricted to a specific 2048- or 4096-byte blocks as is the case with storage protection or preferential storage base addresses.

Assume that CE 1 is the primary controlling CE in the ATC system, and that CE 2 is the secondary CE; i.e., CE 1 is assigning the work (data) and CE 2 is performing the calculations on this data.

Initially [Figure 6-9(a)], the common area is empty (logically, at least) and unloaded. A TS instruction to location 5000 [Figure 6-9(b)], tells CE 1 that the area is free and, at the same time, sets the lock on the area.

With the lock set [Figure 6-9(c)], CE 1 can proceed to fill the data area without program interference from other CEs. A TS instruction from CE 2 tells its program that the common area is temporarily unavailable. At this point, CE 2 can either proceed with other routines, or execute the Delay (DLY) instruction for a period of time.

Remember that the lock condition imposed on the storage area by CE 1 is only a logical lock and not a hardware lock except to the extent of setting the condition code to either a 0 or a 1. Other system elements may also be using this SE under the conditions of configuration and priority.

When the common area has been filled [Figure 6-9(d)], CE 1 issues any one of a variety of "store" type instructions which replaces byte location 5000 (or at least the leftmost bit of that position) with 0's.

The next time CE 2 tests the lock position [Figure 6-9(e)], a resulting condition code setting of 0 indicates an unlocked state. As a result [Figure 6-9(f)] CE 2 proceeds to

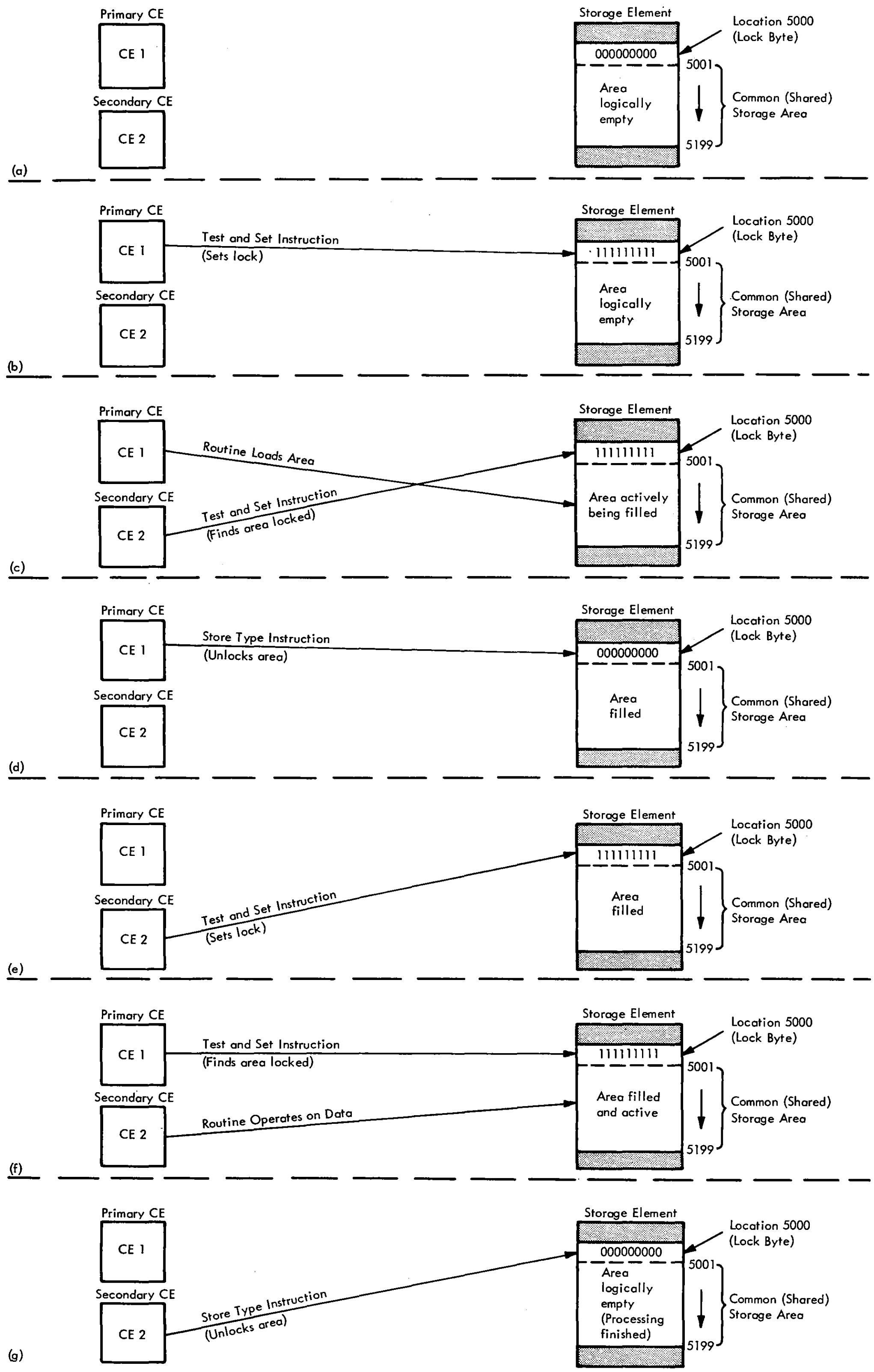


Figure 6-9. Test and Set Example

process the data in the shared area. Any test by CE 1 during this time finds the area locked.

At the end of the data processing [Figure 6-9(g)], CE 2 unlocks the area by restoring the lock byte to 0's. The cycle is now complete, and CE 1 can refill the area with new data.

Delay Instruction (DLY)

- Executed by CEs or IOCEs.
- RR format.
- R1-R2 field contains count.
- Terminated by interruptions or count = 0.

The eight bit R1-R2 field is treated as a single count field (N). Execution of the delay instruction causes a delay of approximately 256N usec. An initial count of 0 causes no delay; a maximum count of 256 provides a delay capability of over 65 ms. This delay is approximate and may be increased because of service requests from the interval timer.

The delay instruction is terminated by the count (N) being reduced to 0 or by the occurrence of an unmasked I/O, external, or machine-check interrupt condition.

The delay instruction is explained in this section because it is unique to the 9020 system and is one means of awaiting the availability of shared storage areas when using the TSS instruction.

RECONFIGURATION AND MULTISYSTEM OPERATION

- Initial configuration established by SCON.
- Storage allocation established by SATR.
- Backup established by PSA setup and element states.

The configuration control facility of the 9020 system may now be seen in the light of multisystem operation. The initial configuration of the 9020 system as established by the SCON instruction, together with the storage allocation as established by the SATR instruction, determines the nature of the total multisystem operation. This initial organization is performed by the CE which is, at the moment at least, the master CE. Under control of the EXC program, the master CE builds a multisystem organization sufficient for the workload and appropriate to the current tasks.

The configuration and storage allocation thus established determine which elements may communicate with each other, which groups of elements together constitute subsystems, which processors may share storage with other processors, and which elements shall monitor for errors and abnormal conditions. Inherent in this organization are provisions for backup in case of malfunctions. This backup is established by the structuring of alternate PSA areas in appropriate SEs and by the choice of element states in various subsystems so that elements engaged in tasks of lesser importance can be used to back up elements of primary importance.

As explained, the 9020 system has elaborate provision for controlling this multisystem organization. Special hardware, instructions, and communications paths, together with the interruption-handling facility, enable the EXC program to coordinate the operation of all of the subsystems and provide such services to the various programs as they may require. In Chapters 7 and 8, overall system monitoring for errors and abnormal conditions is discussed in detail. This monitoring is under control of the EXC program via the external interrupt facility and special hardware such as the DAR and abnormal condition signals which override the normal CCR gated communication paths within the system.

As a result of detecting a malfunction or an abnormal condition, the master CE may initiate procedures to isolate the condition and may reconfigure the system so that the primary task of the system may continue with a minimum of lost time. Should the malfunction or abnormal condition involve the master CE, another CE can automatically take its place. That is, the actual processing of EXC program instructions can be done by a backup CE so that, while an element is lost to the system, the control program can still function.

The EXC program can respond to requirements of the entire multiprocessing operation, when a reconfiguration is necessary, so that no primary function of the system is lost. This may involve terminating certain operations, eliminating certain lesser functions, establishing new PSAs, reallocating storage, relocation of programs, and building checkpoint records, all in addition to reconfiguration.

- 9020 system performs ATC and non-ATC tasks.
- ATC task is primary.
- EXC must monitor elements in both categories.
- Special hardware for monitoring non-ATC elements.

The 9020D system consists of multiple elements which may be configured into subsystems to accomplish various tasks. These tasks may be divided into two major categories: ATC and non-ATC. The non-ATC category includes "good" elements running diagnostics (or other programs) and elements which are not "good" due to malfunctions, maintenance, or engineering change activity.

The ATC task is performed by at least one subsystem and represents the primary function of the system. The Executive Control (EXC) program must monitor elements involved in non-ATC tasks insofar as they affect the overall capability of the system to accomplish its primary task. More explicitly, the system performing the ATC task must monitor certain classes of element malfunctions, which may be generated by other elements in state two, one, or zero, and which are performing other tasks since these other elements may be called on at any time to do the ATC task. The normal system of hardware and software by which the EXC program monitors the ATC task is not sufficient for monitoring non-ATC tasks because CCR gating in the individual subsystems may isolate them from the standpoint of data communication. For this reason hardware is supplied which overrides normal CCR gating to provide the needed system-wide monitoring capability for the EXC program.

This chapter describes system-level monitoring of errors and abnormal conditions together with the hardware provided for its implementation. Chapter 8 explains how the individual elements handle malfunctions within the framework of the larger system monitoring scheme.

PROGRAM AND HARDWARE COMMUNICATION

- Monitoring uses both program and hardware communications.
- Hardware communications used for malfunctions of specific interest to the EXC program.
- Utilizes 9020 external interruption facility.

Monitoring takes on two general forms: program communications and hardware communications. Program communication provides for certain element malfunctions (e.g., TCU logic errors) which are primarily of interest to the monitor program for the particular subsystem of which the element is a part. These malfunctions can then be brought to the attention of the EXC program in an orderly fashion if required.

Hardware communication facilities are provided for certain element malfunctions that are of specific interest to the EXC program directly. Included are those items which cannot be handled by the subsytem (e.g., CCR failure or power failure) since normal lines of communication may not exist. Also, these elements might be idle (i.e., not part of a subsystem) when these conditions occur. Certain malfunctions in SEs or CEs might place the subsystem in such a position that program communication is no longer possible.

The hardware communication lines utilize the external interruption facility of all CEs to notify the EXC program of a particular condition. Since the EXC program may be operating in any CE, each CE contains the needed hardware to monitor the entire system.

OVERALL OPERATION

Figure 7-1 shows the general method by which one element monitors the malfunctions of another. In the case presented, one CE is interrupted so that it can control the analysis of a second CE which is malfunctioning. Simplifying assumptions have been made (e.g., intermittent parity check) to present the philosophy. The two CEs are labeled "malfunctioning" and "attentive" since the attentive element need only be configured to listen to the malfunctioning CE. No indication is given of the masking which could be done.

The general course of action taken in this situation may be divided into four phases A, B, C, and D, as shown on Figure 7-1 and described below:

A. The malfunctioning CE detects an error. It stops its current processing and generates an element check to all CEs. It then proceeds to perform its own logout in three parts, as shown.

B. An "attentive" CE responds to the element check by accepting an external interruption. It will indicate to the malfunctioning CE (by altering a program in storage) that there is a listening element. The attentive CE will then perform the necessary "first line" analysis of the

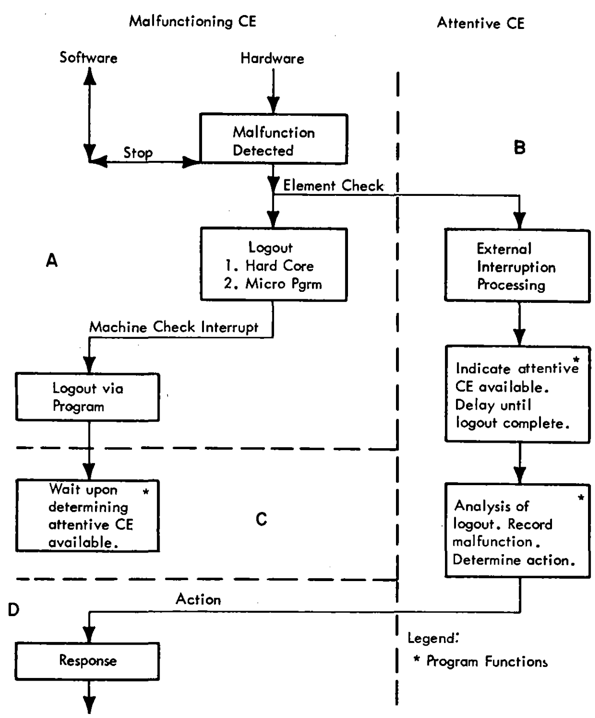


Figure 7-1. Monitoring of Element Malfunctions

situation to determine the immediate course of action necessary. This could also be extended to include a reasonably detailed analysis of logout data from the malfunctioning CE.

C. The malfunctioning CE now waits until action is taken by the attentive CE. If the malfunctioning CE had not been informed that another CE had responded to its element check, it could elect to start an analysis of its own logout data. The success of this action would depend upon the nature of the condition.

D. The malfunctioning CE will now respond to the course of action taken by the attentive CE.

MONITORING FACILITIES

The following system facilities are provided to enable system monitoring:

1. Interelement Signal Lines
2. Logout
3. External interrupt
4. Diagnose accessible register (DAR)
5. Diagnose accessible register mask (DARM)

Interelement Signal Lines

- Used to indicate exception (abnormal) conditions.
- Causes external interrupt in CEs not masked against interrupt.
- Signals originating in CEs force receiving CEs to state three if receiving CE is properly set up.

These lines, which exist between system elements and the CEs, are used to indicate that an abnormal condition (i.e., temperature out of tolerance check, power shutdown, CCR parity check, on-battery indication, checkstop, or logic check) has occurred in that element. These external signals will cause a single external interruption in each of the receiving CEs that is not masked against the condition. If the originating element is a CE, the signal will bring all receiving CEs not in the zero state with test switch on into state three, provided these CEs are configured to accept a SCON instruction from the originating CE.

This last point deserves special attention. It provides for the situation in which the CE in the ATC subsystem malfunctions and is unable to handle the malfunction itself. Since all CEs are interchangeable, the EXC program may operate in any one of them. By hardware-forcing all other available CEs into state three, provision is made for the continuing operation of the EXC program under these circumstances. Of course, at least one of the forced CEs must have the correct external interrupt new PSW to allow it to begin execution of the EXC program.

Upon receipt of an interelement signal, the receiving CE will take appropriate action (under control of the EXC program) to determine the operational status of the originating element and (1) attempts to alleviate the condition which generated the external signal, or (2) removes the element from the operational system.

External signals resulting from the abnormal conditions mentioned previously fall into three categories:

1. Element check (ELC): caused by an element failure (power or logic).
2. Out-of-tolerance Check (OTC): caused by element temperature becoming marginal.
3. On-battery signal (OBS): caused by an element switching from main-line power to battery-backup power.

Figure 7-2 summarizes the conditions which generate the external signals resulting in an external interruption.

Logout

- Logout performed by CEs and IOCEs.
- Critical controls and registers stored in an SE.

A logout in a CE or an IOCE causes the orderly storing of control conditions and critical registers into a preferential

Element	Generating Condition	External Signal	Originating Element Status after Signal
CE	CCR Parity	ELC	Operational
	Logic Check	ELC	Operational
	OTC	OTC	Operational
	OBS	OBS	Operational for 6.5 sec
	Power Check	ELC	Down
	Storage Check	ELC	Check Stop*
SE	Logout Stop	ELC	Stopped
	CCR Parity	ELC	Operational
	OTC	ELC	Operational
	OBS	ELC	Operational for 5.5 sec
	Power Check	ELC	Down
	Storage Check	ELC	Operational
	Address Check	ELC	Operational
	Data Check	ELC	Operational
IOCE	CCR Parity (spontaneous)	ELC	Operational
	CCR Parity (receiving SCON)	OBS/Pulse	Operational
	Common Logic Check	ELC	Check Stop**
	Storage Check	ELC	Check Stop**
	OTC	OTC	Operational
	OBS	OBS/level	Operational for 6.5 sec
	Power Check	ELC	Down
PAM, TCU, and SCU	CCR Parity	ELC	Operational
	Power Check	ELC	Down
	Check Stop (PAM)	ELC	Down

Legend:

OTC - Out of Tolerance Check (temperature)
OBS - On Battery Signal

* This is the status of the element if the generating condition occurs during logout. If it occurs during processing, the CE initiates its own logout.

** This is the status of the element if the generating condition occurs during logout. If it occurs during processing, the IOCE issues a machine check interruption request to its associated CE and waits for a response.

●Figure 7-2. Hardware-Generated External Interruption Status Table

storage area (PSA) in an SE. The address of the specific PSA is pointed to by the preferential storage base address register (PSBAR) in the CE. Upon successful completion of a CE logout, a machine check (MC) interruption is automatically taken. The processing of the interruption may include the saving of additional registers for later analysis, immediate analysis of the malfunction, or simply a wait condition, the exact action depending upon the assigned task of the CE.

Logout in the IOCE is not initiated until a request is made to the controlling CE for an MC interrupt (unless the malfunction took place in a selector channel). The IOCE receives the PSA address from the controlling CE, logs out, and indicates to the CE that the logout is complete. At that time, the CE takes the special MC interrupt and may analyze the IOCE malfunction. In the case of a selector channel error, the IOCE presents an I/O interrupt request to the controlling CE to request permission to logout the selector channel.

Logout of SEs is under program control of a CE, and the data is automatically placed in an SE specified by the CE performing the logout. Detailed malfunction information is available for TCUs, SCUs, and PAMs via the normal I/O sense command. Logout is discussed in detail in Chapter 8.

External Interrupts

- Allows CEs to monitor system conditions while processing.
- Normal and abnormal interruptions.

This facility allows the CEs to continually monitor system conditions of selected elements while simultaneously performing the normal processing functions.

The external-interruption scheme of the 9020D system is provided to allow programmed signaling between various CEs and hardware signaling between the system elements and the CEs. Whenever an external interruption is accepted by a CE, a unique bit is set in that CE. The external interruptions are completely maskable by bit 7 of the current PSW, except as signified in Figure 7-3. The interruptions are divided into two classes: normal and abnormal.

Normal Interruptions

- Program controlled.
- Not related to system check conditions.

Normal interruptions are program-controlled and not related to system check conditions. The source of an external interruption is available to the program from bits 20 to 31 of the external old PSW (Figure 7-4).

The CE Read and Write (Direct) or I/O Processor Write Direct indications are under control of the CCR described previously. The interrupt and timer bit positions in the PSW will be set regardless of the CCR. This type of interruption is described in detail in the 9020D/E System Principles of Operation manual. Normal interruptions do not require use of the diagnose accessable register (DAR), which is described later. Bit 31 of the PSW, which indicates a DAR-type interrupt, is not set for normal interruptions.

Abnormal Interruptions

- Hardware generated.
- Indicate failures or impending failures.
- Set bit in DAR.

Abnormal interruptions result from some external signal having set a bit in the DAR. The DAR is depicted in Figure 7-5. The signals which set bits in the DAR are the hardware-generated signals of current or impending failures. Each signal of this class causes an appropriate bit to be set

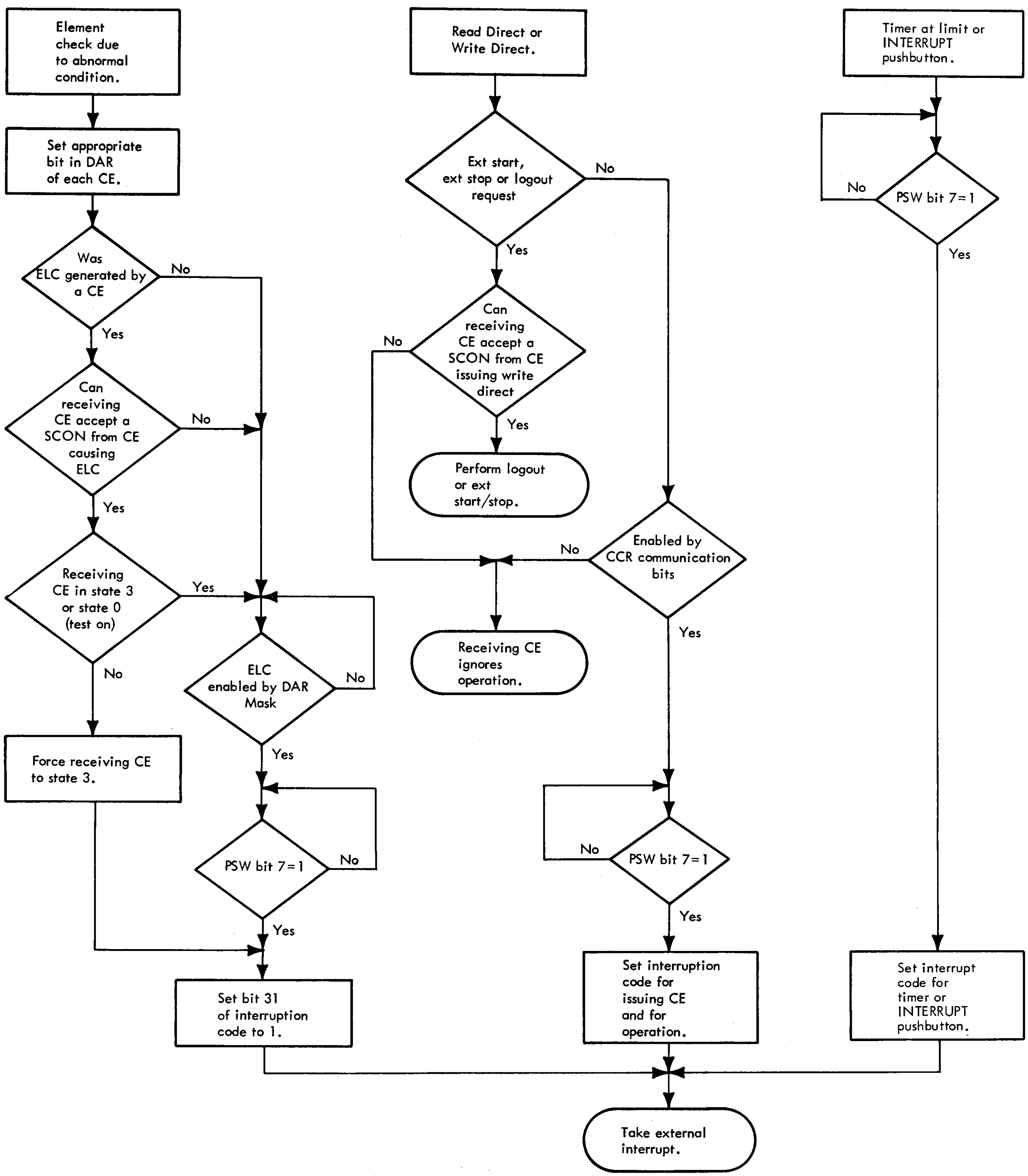


Figure 7-3. External Interrupt Handling

CE1		CE2		TIMER	INTP	CE3		CE4		PIR	DAR
RD DIR	WRT DIR	RD DIR	WRT DIR			RD DIR	WRT DIR	RD DIR	WRT DIR		
20	21	22	23	24	25	26	27	28	29	30	31

Figure 7-4. Old PSW, Interruption Source

in the DAR, which, in turn, causes an external interruption if the CE is not set to mask off external interruptions. The DAR bit (bit 31 in the old PSW) will be set at the time the interruption is taken to identify the interruption source.

The components of the external-interruption system of each CE, with usage and control, are defined in the following paragraphs.

Masking

- Bit 7 of current PSW normally masks all external interrupts.
- Abnormal interrupts masked by DARM.

Bit 7 of the current PSW is used to mask external interruptions, with one exception. If the CE is in state two, one, or zero (with test switch off), a CE ELC with the corresponding SCON bit on is sufficient to force an external interrupt and override mask bit 7. If this bit is a 1, normal interruptions can proceed as usual; abnormal interruptions may be subject to further masking by the DAR Mask (DARM). If mask bit 7 in the current PSW is a 0, all interruptions will be held pending until this bit is set to a 1 or the CE is reset. Each bit in DAR represents a specific reason for an external-interrupt request. If (while external interruptions are masked off) more than one of the external signals is received, more than one bit is set in DAR. When interruptions are again allowed, only one interruption will take place, but a reading of DAR will show all of the reasons for the interruption request. However, if a particular signal is received more than once while interruptions are masked off, all but the first is lost since a given DAR bit can be set only once.

PSW Interruption Code

- Bits 20–31 of PSW identify external-interruption source.
- PIR bit.
- DAR bit.

Bits 20 through 31 of the PSW contain the identification of the external interruption source. The appropriate PSW bit is set at the time the external interruption is taken. Figure 7-4 illustrates the source identification.

The eight bits associated with CE Read and Write Direct, specifying data communication are gated by the CCR. That is, if the CE is not configured to listen to the requesting CE or is in test, the request will be ignored, and the bit in the interruption code will not be set. If the CE is configured, the appropriate bit will be set in the PSW and an external interruption will be taken if not masked off by PSW bit 7.

The Interrupt and Timer bits are set any time the source signals arise and the interruption is taken if not masked off by bit 7.

The PIR bit (30) refers to the processor interrupt register which is a special three-position register used to identify external interrupts from an I/O processor. The bits are gated with the IOCE bits in CCR, and the interrupt is taken if not masked off by PSW bit 7.

The DAR bit refers to a special register that contains a group of interruption identification conditions too numerous to be included in the PSW. The DAR bit is set at the time the external interruption is taken.

Diagnose Accessible Register (DAR)

- Accessed only via a Diagnose instruction.
- Stores hardware-generated external-interruption requests.
- DAR is reset when it is read out.

The DAR is so named because it is not normally an addressable register; a Diagnose instruction is required for access. This register is used to store and identify hardware-generated external-interrution requests. At the time of an external interruption, this register will be read to supplement the PSW. The conditions that set this register are illustrated by Figure 7-2. The register layout is shown in Figure 7-5.

When any element generates one of the specified interruption requests, its identification bit is set in DAR.

IOCE 1		IOCE 2		IOCE 3		SE ELC										Spare	Spare	PAM ELC			TCU ELC			SCU ELC			Other CE ELC/ CE Own CBS				CE Own OBS
A	B	A	B	A	B	1	2	3	4	5	6	7	8	9	10			1	2	3	1	2	3	1	2	3	1	2	3	4	
0	1	2	3	4	5	6									15	16	17	18		20	21		23	24		26	27			30	31

● Figure 7-5. Diagnose Accessible Register (DAR)

This bit will cause an external interruption if the mask conditions are met. These conditions are:

1. Each position of the DAR has a corresponding mask position in the DAR mask (DARM, to be described later). If the DARM bit is 1 and bit 7 in the current PSW is set to 1, an external interruption will occur at the completion of the current instruction with the DAR bit in the old PSW set to 1. (The following section will describe the special masking technique for IOCE bits in the DAR.)
2. When a CE is in state two, one, or zero (with the Test switch off), CE ELCs cannot be masked off; that is, mask bits are ignored if the CE is configured to receive a SCON instruction from the originating CE.

The bits in the DAR will remain set until a read instruction (Diagnose) is issued to the register; then the entire register is reset.

The character of each signal (pulse or level) which sets DAR is specified in Chapter 8. If the signal which sets DAR is specified as a pulse, then reading of DAR will clear the affected bit and it is not set again unless, of course, the condition occurs again. If the signal which sets DAR is a level, then reading of DAR will clear the bit momentarily, but it will be immediately reset. This forced setting of DAR will continue until the condition causing the signal is cleared. An examination of these level signals, however, shows that there should be no ambiguity in interpretation, since a level will indicate either a non-determinable time for the condition (e.g., OTC or power off), or will indicate that the condition causing the signal has also forced the affected unit to cease operation and require assistance. This method of signaling, in fact, is valuable in determining whether an element can perform some degree of self-diagnosis or must be assisted. As an example, assume that a CE has detected some error and generates a check signal. This is sent to all other CEs as an ELC and will set the appropriate DAR bit. This signal is a pulse; when read by the receiving CE, the receiving DAR bit will be cleared. The CE which generated the ELC will proceed to log out to the PSA. Suppose however, that the CE is unable to perform this logout. This could occur for several reasons, but usually because of double errors. The CE would generate a second ELC and stop. This signal, however, is a level. A receiving CE, if it read its DAR twice in succession, would find the DAR bit still set. This static ELC would remain until the CE which generated it was restarted by some external means.

When DAR is read via Diagnose, the entire register is obtained without regard for any mask which may be used to control interruptions. No interruptions will set DAR during the read operation.

Diagnose Accessible Register Mask (DARM)

- Accessed by Diagnose instruction.
- One bit for each DAR bit except IOCE bits.
- One DARM bit masks both IOCE DAR bits.

The DARM is program-addressable (write) by a special Diagnose instruction. It permits program control over the conditions from the other elements that will be allowed to cause an external interruption in this particular CE. The CCR limits normal data flow between the various system elements while the DARM independently limits exception data flow between the system elements.

DARM contains a position for each position of DAR, except as noted in the next paragraph. If the DARM position is set to 1, a corresponding interruption request through DAR will, if not further masked by PSW bit 7, set the DAR bit in the PSW and request an external interruption. If the DARM is 0, corresponding positions of DAR will not cause the DAR bit to be set in the PSW; note previously mentioned exceptions on CE ELCs.

There are only two bits allotted for each IOCE. These bits are encoded (Figure 7-5) and cannot be considered distinct indications. DARM will mask both bits for each IOCE with a single mask bit. Specifically, the masking arrangement is as follows:

DAR Bits	DARM Mask Bit
0,1	0
2,3	2
4,5	4

DARM bits 1, 3, and 5 are not used.

SYSTEM MONITORING OF ABNORMAL CONDITIONS

The conditions which generated external interruptions were itemized previously. Here, all signals which represent abnormal conditions and the manner in which they are monitored by the system are discussed, whether or not an external interruption is generated. Figure 7-6 summarizes the handling procedure.

Power Supply Abnormal Conditions

- Power supply failure or power down condition results in ELC.

Condition / Element	Power Down or Power Check	OTC	OBS	CCR Parity Check	Check Stop	Logic Check
CE	EXT	EXT (to itself only)	EXT (to itself only)	EXT	EXT	EXT
SE	EXT	EXT	EXT	EXT	EXT	EXT plus specific error indication to using elements
IOCE	EXT	EXT	EXT	EXT (Pulse OBS when receiving SCON)	EXT	EXT (CLU errors) PGM (certain Sel Chan. & Storage errors)
PAM/TCU	EXT	PGM	N/A	EXT	N/A	PGM
SCU	EXT	EXT	N/A	EXT	N/A	PGM

Legend:

EXT - External interruption to all listening CEs.
PGM - Program interruption handled by the subsystem monitor in normal programming fashion.

●Figure 7-6. Summary of Procedure for Handling External Interruption Signals

A power supply output malfunction or a power-down condition in any major element will cause an ELC condition to be generated for that element at each CE.

Marginal Temperature Condition (Out-of-Tolerance Check)

- All major elements monitor internal temperature.
- Overtemperature condition results in OTC.
- Pushbuttons on each element permit simulation of OTC condition for test purposes.

All major elements are implemented with sensing devices for monitoring their internal temperature. A marginal temperature condition is reported to the system as an out-of-tolerance check (OTC). Pushbuttons are provided on each element to simulate the OTC condition for testing. The following OTC indications have been defined for each element of the system:

CE: An OTC condition in a CE causes that CE to take an external interruption. This condition causes a unique identification bit to be set in the DAR of the CE to allow the cause to be identified. It is expected that each CE can handle its own OTCs since they do not indicate an error condition but instead warn of a marginal condition in the element environment which could result in an error in the immediate future. If the CE cannot finish its expected actions before a power shutdown, the ELC which results from the power shutdown will alert the remaining CEs to the condition.

SE: An OTC condition in an SE causes that element to generate an ELC that is sent to all CEs. Those that are not masked for that condition take an external interruption. This condition sets a unique identification bit in DAR. The functional capability of the SE is not impaired by the generation of this ELC. An SE logout is necessary to further isolate the ELC originating conditions.

IOCE: An overtemperature condition in an IOCE causes that element to generate an OTC that is sent to all CEs. Those that are not masked for that condition take an external interruption. This condition sets a unique identification code in DAR. The functional capability of the IOCE is not impaired by the generation of this OTC.

TCU: An OTC condition in a TCU causes that element to generate an "attention" on its IOCE-TCU interface as part of the status byte either at the end of an operation or when an attempt is made to select the TCU. The 'attention' signal is used only for OTC indications by this unit. This interruption condition is handled in the same manner as any other I/O interruption condition. The generation of the OTC condition does not affect the operational capabilities of the TCU.

PAM: An OTC condition causes a PAM to generate "Attention" status from the Test and Monitor Adapter. This interruption condition is handled in the same manner as any other interruption condition. The generation of the OTC condition does not affect operational capabilities of the PAM. A sense command through the IOCE is necessary to detect that an OTC condition does not exist. The sense data will include, among other things, an OTC bit and CCR parity indication.

SCU: An OTC condition in an SCU causes the element to send a pulse ELC to all CEs and to set bit 3 of byte 4 in the sense register. Generation of the OTC condition does not affect operational capabilities of the SCU. The program may perform a Sense command to determine the cause of the ELC, but OTC is actually the only cause for a pulse ELC originating in an SCU.

On-Battery Signal (OBS)

- CE, IOCE, and SE generate OBS when switching to battery power.
- Pushbuttons on each element permit simulation of OBS condition for testing.

Three of the major elements of the 9020D system (CE, IOCE, and SE) have battery backup in case of power failure. A means is provided to signal when the batteries are being used. Switching from normal operation to batteries causes an OBS to be generated. A pushbutton is provided at each of these elements to simulate the OBS condition for testing. This OBS is treated in the following manner for the affected elements:

CE: Only the generating CE receives its own OBS signal. This signal causes an external interruption, which sets a unique identification bit in DAR. The operational status of the CE is not affected by the generation of the signal.

SE: The SE transmits its OBS signal under the common heading of ELC to all CEs. These CEs, if not masked for the condition, take an external interruption, which sets that SE's unique ELC bit in DAR in the CE. An SE logout is necessary to determine the cause of the ELC. The generation of the signal does not affect the operational capability of the SE.

IOCE: The IOCE transmits its OBS to the CEs as a level. The CEs, if not masked for the condition, take an external interruption. A unique OBS identification code is set in DAR in the CE. The operational status of the IOCE is not affected by the generation of this signal. To enable rapid identification, a CCR parity check when receiving a SCON is signaled as a pulse on the OBS line.

CCR Parity Check

- Every major element has a CCR.
- CCR parity check condition causes element to generate ELC.
- IOCE pulses OBS line if a CCR parity check occurs during a SCON.

Every major element has a CCR register. Parity is continually monitored on this register by the element; whenever incorrect parity is detected, an ELC is generated. However, if the CCR is in the process of being loaded, generation of ELC is suppressed since other means are used to inform the EXC program of the condition. This ELC will be transmitted to all CEs. Those that are not masked for that condition will take an external interruption. The ELC condition will cause an ELC identification bit or code to be set in DAR.

Should an element's CCR become set to allow no CE to issue a SCON to the element, this element would be lost to automatic system control. This condition can occur only through a malfunction or through manual action. Hardware is provided to detect this condition.

When this condition is detected, CCR SCON field gating is bypassed, and the element accepts a SCON from any CE, provided that the element is not in state zero. If an element is in state zero, and its SCON field is set to all 0's, it is presumed to be a desired condition and all SCONs are rejected.

A special indicator is used for CCR parity checks which occur in the IOCE during receipt of a SCON. This is a pulse on the OBS line. This unique indication provides for easy identification of the error by the program. The normal OBS indication is a level.

The generation of an ELC as a result of a CCR parity check in any element does not affect the operational capability of the generating element except insofar as CCR gated communications with other elements are concerned. Further analysis of the condition requires logout or sensing of the element.

Checkstop

- Major elements implemented with checkstop capability.
- Enables element to stop when error is detected.
- Results in level ELC.

All major elements are implemented with a checkstop that permits them to stop upon detection of an error condition. The checkstop condition always results in an ELC being issued to all listening CEs.

CE and IOCE: In the CE and IOCE, checkstop results when the element is unable to continue operation (e.g., when a logic error occurs during a logout). A level ELC is issued to all listening.

SE: In the SE, a checkstop occurs when an error is detected. A pulse ELC is issued as a result of the error, and the element waits 2.5 usec for a signal from the using element requesting it to stop for logout. If the 'logout stop' signal is received, the SE is effectively checkstopped and issues a level ELC to all CEs. An 'SE stopped' signal is also issued to all configured elements.

Logic Check

- Every element checks for internal errors.
- Logic check reporting varies from element to element.

Every system element has built-in internal checking procedures, described below. The CCR is not included since it was described previously.

CE: An internal logic check causes the CE to signal an ELC to all other CEs. The CE that has the logic check may proceed with a logout, depending upon whether its machine-check interruption is masked on or not.

SE: An internal logic check in an SE is only signaled when another element is using it. The signal appears as a pulse ELC to all CEs, as either an address check or data check to a CE user, or as a storage check to an IOCE user.

IOCE: An internal common logic check (or multiplexer channel check) causes the IOCE to checkstop and signal an ELC to all CEs, the reception of which was described previously. The IOCE then requests a special machine-check interruption which will allow it to log out from the configured controlling CE. The IOCE suspends I/O processor operations until the controlling CE reinitiates them.

A malfunction in the hardware of a selector channel causes that channel to stop. The IOCE requests an I/O interruption of its configured CE. When the interruption is permitted, the selector channel is logged out and the interruption performed.

TCU: The TCU attempts to signal the IOCE of any logic failures and expects remedial action through the IOCE using normal I/O checking hardware (and software). Malfunctions affecting only an individual tape drive or associated path do not affect the operation of the remainder of the TCU. Malfunctions originating from the common logic of the TCU affect the entire TCU system.

PAM: PAM attempts to signal the IOCE of any malfunction, and remedial action is expected through the IOCE interface in much the same fashion as the TCU. Some malfunctions in PAM Common will stop all PAM data service cycles; malfunctions originating in the PAM adapters will only affect the malfunctioning adapter.

SCU: The SCU attempts to signal the IOCE of any logic failures and expects remedial action through the IOCE, using normal I/O checking hardware (and software). Malfunctions affecting only an individual DSU do not affect the operation of the SCU. Malfunctions originating from the common logic of the SCU can affect the entire DASF.

- Individual elements contain error and abnormal condition detection circuitry.

- Elements vary in degree of sophistication.

- Internal and external errors.

- Six types of abnormal conditions.

Individual elements of the 9020 system contain circuitry for error checking, abnormal condition monitoring, and malfunction handling. Different element types vary in their degree of sophistication. For example, the CE is capable of accessing and executing complex programs whereas the SE is limited to a few basic operations. For this reason malfunction handling in the different elements ranges from complex analysis and system reconfiguration to simple error detection and reporting. The different element types may be thought of as falling into echelons based upon their degree of sophistication. The lower echelon elements detect errors and abnormal conditions and report them to higher echelon elements until ultimately the reported condition is acted upon at the subsystem or system level.

Each element has hardware facilities to detect errors occurring within its internal logic. In addition, where two types of elements work together, one is provided facilities for handling malfunctions occurring at the interface or arising out of their interrelated operation. Such malfunctions are termed external. For example an IOCE receiving data in bad parity from a CE, via the control bus, takes no action itself but reports the error to the CE. The malfunction may have occurred at the IOCE but the CE handles it as if it were a CE logic check. This distinction between internal and external errors is helpful in understanding how the malfunction-handling facilities of the individual elements fit together into a unified malfunction-handling capability.

Possible abnormal conditions fall into six categories in the 9020D system. These were described in Chapter 7 from the system standpoint. They are briefly described in the following paragraphs from the standpoint of the individual element. The detailed handling of these abnormal conditions by the individual elements is described later in this chapter. Abnormal conditions fall into six categories:

1. Abnormal power condition: power down and power check.
2. Abnormal temperature condition - out-of-tolerance check (OTC).
3. On-battery signal (OBS).
4. CCR parity check.
5. Checkstop
6. Logic check.

An abnormal power condition may indicate a malfunction in an element's power system (power check) or that power has been turned off for scheduled maintenance (power down). In either case the system must be alerted that the element is not in its normal operational condition and cannot be called upon to take part in the ATC task.

An overtemperature condition in an element may presage logic checks or a catastrophic power down. The OTC signal allows the system to prepare for the loss of the element by reassigning its task to a backup element.

On-battery signal (OBS) is an abnormal condition which is monitored by all elements which contain battery backup power sources so that the system can be alerted to the impending loss of the element and respond accordingly.

A CCR parity check can interfere with an element's ability to communicate with other elements with which it is working. This condition is monitored by all elements and the system is immediately alerted when it occurs.

A checkstop is implemented in each major element of the 9020 system, permitting the element to stop upon detection of a malfunction. The element may continue operation after alerting the system to the condition or it may be unable to continue, depending on the nature of the malfunction. In either case, the stopped condition is reported to the system via the element check (ELC) signal. The level ELC signal is used to indicate that the element cannot continue without external assistance, whether from other elements of the system or from operating personnel.

Logic checks, internal and external, constitute abnormal conditions which are reported to the system by the individual elements.

The handling of logic checks by the individual elements is usually more involved than the handling of other abnormal conditions. For this reason logic checks are given special emphasis later in this chapter in the discussion and flowcharts for the individual elements.

ERROR RECORDING

- Error information retained by individual elements.

- Error information available to EXC program via logout or sense command.

An element reporting a logic check must retain sufficient information for the system to determine the nature of the error so that it can react appropriately. All elements contain registers in which error information is retained temporarily. In the CE and IOCE these are the check registers. In the SE, error triggers are provided for the retention of error information. The TCU, SCU, and PAM retain error information in the status and sense registers.

This information regarding the nature of a logic check is made available to the EXC program for analysis via the logout facilities or, in the case of the TCU, SCU, and PAM, via the I/O sense command.

Logout

- CE, IOCE, and SE can be logged out.
- CE and IOCE can perform logout.
- IOCE must receive permission from controlling CE before performing logout.
- SE logged out by CEs via Diagnose instruction.

Logout was described briefly in Chapter 7. Here, it is described in detail from the standpoint of the individual elements. Later in the chapter, logout is treated as an integral part of the individual element malfunction-handling capability.

Logout is the process of automatically storing the contents of various registers of an element into a preassigned location in the PSA area of main storage. This is done in a manner which permits the actual parity of the data to be preserved whether it was correct or not.

The CE, IOCE, and SE can be logged out. The CE is capable of performing a logout of its own registers. The IOCE also has this facility but does not log out without first requesting permission from the CE with which it is working. This is necessary in order for the IOCE to obtain the CE's PSA address from the CE and to alert the CE that the logout is taking place. SEs are logged out under control of a CE. They have the facility to stop for logout upon request by a CE or IOCE and to send logout data to a CE as the CE requests it. The CE uses the Diagnose instruction to logout SEs.

Figure 8-1 shows the layout of the logout area in the PSA. The CE logs out 48 words (192 bytes) starting at location 80 (hex) and extending through the word at location 13C (hex). The last byte of the last word is at location 13F (hex).

The word at location 140 (hex) is used by the IOCE for temporary storage of the storage data register (SDR) during

Hex Address of Word	PSA Word No.			
000 07C	0 31	PSWs, CSW, CAW, etc.		
080 13C	32 79	CE Logout Area (48 words)		
140	80	Note 1		
144 1C4	81 113	Partial CLU Logout Area (34 words)		Complete CLU Logout Area (45 words)
1C8 1F0	114 124	Selector Channel Logout Area (11 words)		
1F4	125			
1F8 1FC	126 127	Unused Area (2 words)		

Notes:

1. This word is used by the IOCE for temporary storage of the SDR during logout. At completion of logout, this word should contain all zeros and should be in good parity.
2. SE logout data locations are not fixed but are specified by the Diagnose instruction which initiates the logout.

Figure 8-1. PSA Logout Area Locations

logout. At the end of the logout, this word should contain all zeros and should be in good parity.

The IOCE logs out 45 words (180 bytes) during a complete logout. The IOCE logout area begins at location 144 (hex) and extends through location 1F4 (hex). The last byte of the last word is at location 1F7 (hex).

The selector channel portion of the IOCE logout area comprises 11 words starting at location 1C8 (hex) and including the word at location 1F0 (hex), which is the next to the last word of the IOCE logout. The last word is part of the multiplexer channel logout.

A partial CLU logout includes all of the IOCE logout except the selector channel; i.e., CLU, common channel, and multiplexer channel. The partial logout starts at location 144 (hex), extends through the word at 1C4 (hex), and includes the singleword at location 1F4 (hex).

Note that the logout area for an SE is not fixed; instead it is specified by the Diagnose instruction which initiates the logout.

The logout format for the IOCE may be found in the IOCE Theory of Operation manual. The logout formats for the CE and SE may be found in the Maintenance Diagram manuals for these elements.

CE Logout

- CE logout may be initiated four different ways.
- Logout data placed in PSA starting at location 80 (hex).

- Logout data consists of 48 words.

A diagnostic logout may be initiated in a CE by four different means. Each method of initiating the logout causes a specific identifier bit to be set in the check register of the CE logging out, and causes a machine-check interruption request to be presented. Provided machine-check interruptions are not masked off, the logout is carried out and then a machine-check interruption is taken. If machine-check interruptions are masked off, both the logout and machine-check interruption requests remain pending.

When a CE logs out, the log information is placed in 48 contiguous words of the PSA, extending from byte location hex 80 through byte location hex 13F inclusive.

Logout Initiated by Another CE. Another CE may initiate the logout by executing Write Direct specifying the CE to be logged out. Provided the SCON bit for the CE initiating the logout is already set on in the CCR of the receiving CE, bit 26 is set in check register 2. If the machine-check interruptions are not masked off, the logout is carried out and then the machine-check interruption is taken.

Logout Initiated by an Address or Data Check. When an address check or data check is received from a configured SE on any storage reference other than to the alternate PSA, and provided masking conditions are satisfied, a CE logout occurs. Bit 11 or 12 is set in check register 2 to identify the cause of the logout.

Logout Initiated by a Storage Timeout Check. When a storage timeout check is encountered while attempting to access a configured SE, but 10 of check register 2 is set on, and a logout is carried out, subject to the machine-check masking conditions described previously.

Logout Initiated by an Internal Check. When an internal check (CE machine check) is detected in the CE, the appropriate check bit is set in check register 1 or 2. If machine checks are not masked, the logout is carried out, and a machine-check interruption is taken.

IOCE Logout

- IOCE performs two types of logouts: CLU and selector channel.
- Only one selector channel logged in any one logout.
- If no selector channel is in operation when CLU logout is initiated, selector channel area is set to all zeros.

The IOCE performs two types of diagnostic logouts: the common logic unit (CLU) and selector channel. The CLU logout information includes the CLU, common channel, multiplexer channel, and one selector channel, provided the selector channel is involved in the malfunction. When no selector channel is involved, all zeros are stored in the selector channel logout area (logwords 114–124). This is termed a "partial CLU logout". A CLU logout may be initiated by an IOCE or a CE. CLU logouts initiated by the IOCE request a machine-check interruption in the controlling CE. The logout occurs when the interruption is permitted. CLU logouts initiated by the CE executing Write Direct do not request machine-check interruptions.

The selector channel logout uses words 114–124 and applies only to the selector channel involved. Selector channel logouts are initiated by requesting an I/O interruption in the controlling CE. The logout occurs when the interruption is permitted. An exception to this occurs if the channel is setting up an I/O instruction and has not yet released the CE by sending response. In this case PSBAR is already available on the control bus and the logout can proceed immediately.

CLU Logout. A CLU logout may be initiated in an IOCE by three means:

1. A CLU check (IOCE machine check) is detected during a normal operation (i.e., I/O operation or IOCE processor operation) or during a selector channel logout.
2. A selector channel logout-request condition is detected while a Test Channel instruction is being processed.
3. An IOCE logout signal is received from a CE executing Write Direct with the IOCE to be logged out specified.

When a CLU logout is initiated by 1 or 2, the IOCE issues a pulsed ELC to all CEs in the system, requests a machine-check interruption in the controlling CE, and waits in check-stop condition until the machine-check interruption is allowed. When allowed, the IOCE logs out into the PSA, and ends the operation by issuing a response to the CE. In addition, when the CLU logout is initiated by a CLU check during an IOCE processor operation, the IOCE stores its old machine-check PSW in MACH 48 (dec) at the completion of a successful logout.

The CE handles an IOCE machine-check interruption request as follows. If an I/O instruction is in process, the CE terminates the operation, storing a condition code 3 in the PSW. If machine-check interruptions are not masked off, the IOCE is allowed to start the logout. If no I/O instruction is in process, and machine-check interruptions are unmasked, the IOCE is allowed to start the logout at completion of the current CE instruction. The CE waits during the logout. Upon its completion, a machine-check interruption is taken.

An IOCE logout may be initiated by a CE executing Write Direct provided the communications bit for the CE is already set in the IOCE's CCR. The IOCE sets bit 8 in check register 2 and proceeds while the CE waits for the IOCE to indicate that the logout is complete by sending 'response'. Upon receipt of 'response', the CE sets the condition code to zero and fetches its next instruction. Should a timeout occur, a condition code of three is set and instruction fetching is resumed as before.

When a CLU logout occurs, IOCE processor operation ceases and the IOCE goes into the wait loop at the completion of the logout.

Selector Channel Logout. When an IOCE detects a check other than a channel data check which is entirely associated with the selector channel hardware, a selector channel logout is initiated. The IOCE terminates the affected channel operation, logs it out, and resets it. Depending on the current activity in the channel when the error is detected, one of the following actions is taken:

1. If an I/O instruction other than Test Channel is in progress the IOCE logs out the selector channel and sets bit 45 (channel control check) or 46 (interface control check), as is appropriate in the CSW. A response is returned to the controlling CE with condition code 1. The instruction is terminated and the CSW is stored.
2. If the Test Channel instruction is in progress, a full CLU logout is taken.
3. If a data transfer is in progress, the IOCE requests an I/O interruption in the controlling CE. When permitted, the selector channel is logged out. Appropriate bits are set in the CSW as in 1 above, and a response is returned to the controlling CE.

If I/O interruptions are masked off, the affected channel waits in stopped state until the interruption is allowed, or until the IOCE receives a logout signal from the CE via Write Direct.

When a selector channel logout occurs, any concurrent IOCE processor operation is suspended during the logout, and then resumed upon completion of the channel logout. When a check is detected during a selector channel logout, full CLU logout is initiated.

SE Logout

- SEs must be placed in logout-stop status by CE or IOCE before being logged out.
- Only CEs can logout an SE.
- SEs logged via Diagnose instruction.
- Logout data placed in storage at location specified by Diagnose instruction.

In order to initiate a logout operation for an SE, the SE must first be placed in logout-stop status by a 'logout-stop' signal (LOS) from a CE or an IOCE. SE accepts a LOS signal from an issuing element provided its communications bit is set on in the SE's CCR and, in the case of an IOCE, if the response latch for that IOCE is set in the SE.

LOS from CE. Logout stop is automatically issued by a CE whenever it receives either an address check or data check, provided machine-check interruptions are not masked off, a CE logout is not in progress, and the inhibit logout stop (ILOS) bit is not already set on in the CCR of the CE.

An SE accepts a LOS signal when the communications bit for the issuing CE is set in the SE's CCR; otherwise it is ignored.

LOS from IOCE. Logout stop is automatically issued by an IOCE whenever it receives a storage check, provided the ILOS bit is not already set on in the CCR of the IOCE and an IOCE logout is not in progress. Bit 3 in check register 2 (SE LOS) in the IOCE is set on so that the fact that this particular IOCE stopped the SE can be determined from a subsequent logout. A pulse ELC is issued to all CEs, and the IOCE requests a machine-check interruption in the controlling CE.

The IOCE will also automatically issue a logout stop to an SE when the IOCE detects a parity error on data fetched, provided the ILOS bit is not already set on in the CCR of the IOCE and an IOCE logout is not in progress. Upon receipt of the logout-stop signal, the SE issues a level ELC to all CEs in the system. An SE may be issued an LOS signal by any configured CE or IOCE and thus be placed in a stopped condition, ready to be logged out. However, only a CE configured to communicate with the particular SE has the ability to effect the logout and restart the SE by issuing the logout-complete signal.

The transfer of logout information from the SE's check latches to a designated main storage location is initiated by a CE executing a Diagnose instruction which specifies the logout main storage kernel for a designated SE. The SE will always log out the complete format. The logout information is placed in main storage in six contiguous doublewords following the MCW specified by the Diagnose instruction which initiated the logout operation. Logout complete is automatically generated at the end of the diagnostic logout.

Split Logout

- Split logout may occur if PSA SE becomes unavailable during logout.

- PSBAR is stepped and logout is restarted in alternate SE.

- Split-logout bit is set in word 42 of CE logout data.

- Scan address sequencers show where logout split.

- Only CE can perform split logout; IOCE cannot.

Under certain circumstances during a logout (see "CE Error Handling" in this chapter), when the CE is unable to access the SE containing the PSA, a split logout will occur. That is, PSBAR is stepped to the alternate PSA SE and the logout is restarted. When this occurs, the split logout bit is set in check register 2 of the CE. This bit becomes bit 23 of logword 42 in the second logout.

Whenever the split-logout bit is found to be set in word 42 of the CE logout data, a portion of the logout data may be in the primary PSA. This may be determined by examining the contents of the scan address sequencers (bits 8–11 of word 43), which is logged in the alternate PSA. If the logged address sequencers reference a doubleword number less than 23, the doubleword number is one less than the logout number of the last doubleword of logout information contained in the primary PSA.

The alternate PSA always contains a complete set of current log data since the log data is reinitiated. However, the log data in those locations down to one greater than where the address sequencer points may not be identical in the alternate PSA logout. The doubleword of log data indicated by the address sequencers will be found in the ST register logwords in the alternate PSA.

Note that the ST register is normally stored out of parity at the beginning of logout and is corrected at the end of logout. On a split logout it is not possible to return to the primary SE and correct parity in the ST logword. It is expected that the program will allow for this out-of-parity condition when analyzing the logout, but maintenance personnel must be aware of the condition when examining the logout in core.

The IOCE cannot perform a split logout since it cannot step PSBAR. The effect can be obtained by programming, however, as discussed under "IOCE Handling of CLU Errors" later in this chapter.

Sense Command

- I/O control units have no logout facility.

- Sense command used in lieu of logout.

The TCU, SCU, and PAM have no logout facility. Errors are reported via the status byte during normal I/O interface operation. The sense command is used in lieu of logout. Upon receipt of a sense command, these units transfer a series of bytes of data to the channel. These data bytes represent the contents of the sense register which contains details of the error. This is analogous to an SE logout in which error information is transferred to the CE upon request.

MALFUNCTION HANDLING

All elements monitor for abnormal conditions, including internal and external logic checks. CEs handle their own abnormal conditions whenever possible. However, they issue a pulse ELC to other CEs to alert them that an abnormal condition is being handled. When a CE is unable to continue for any reason, it issues a level ELC to all other CEs.

An IOCE reports abnormal conditions to its controlling CE in considerable detail. It can perform a logout but only does so under control of a CE.

An SE reports logic checks to the current user and reports abnormal conditions to all CEs via ELC. Details of the abnormal condition can only be obtained via logout. The SE cannot, itself, perform a logout, but must be logged out by a CE.

TCUs, SCUs, and PAMs report logic errors via normal channel operation. With some exceptions, abnormal conditions are reported via ELC, and a sense command is required to obtain details. These exceptions are noted in the description of the individual element error-handling which follows.

CE Error-Handling

The CE continually monitors for errors occurring within its own logic and for errors resulting from its operation with an SE. For purposes of this discussion, those external errors which may result from operation with an IOCE or another CE (control bus check or read direct timeout) are included with errors in the CE's own logic. In addition to error monitoring, the CE monitors for a logout request, whether from another CE via Write Direct or from depression of the logout pushbutton. The manner is which the CE responds to these conditions is shown in flowchart form in Figure 8-2 and is described in the following paragraphs.

Logic Checks

- Recorded in check registers 1 and 2.

- Can be masked off by PSW bit 13.

Refer to Figure 8-2. When the CE detects an error in its internal logic or receives a check from an SE or DE with

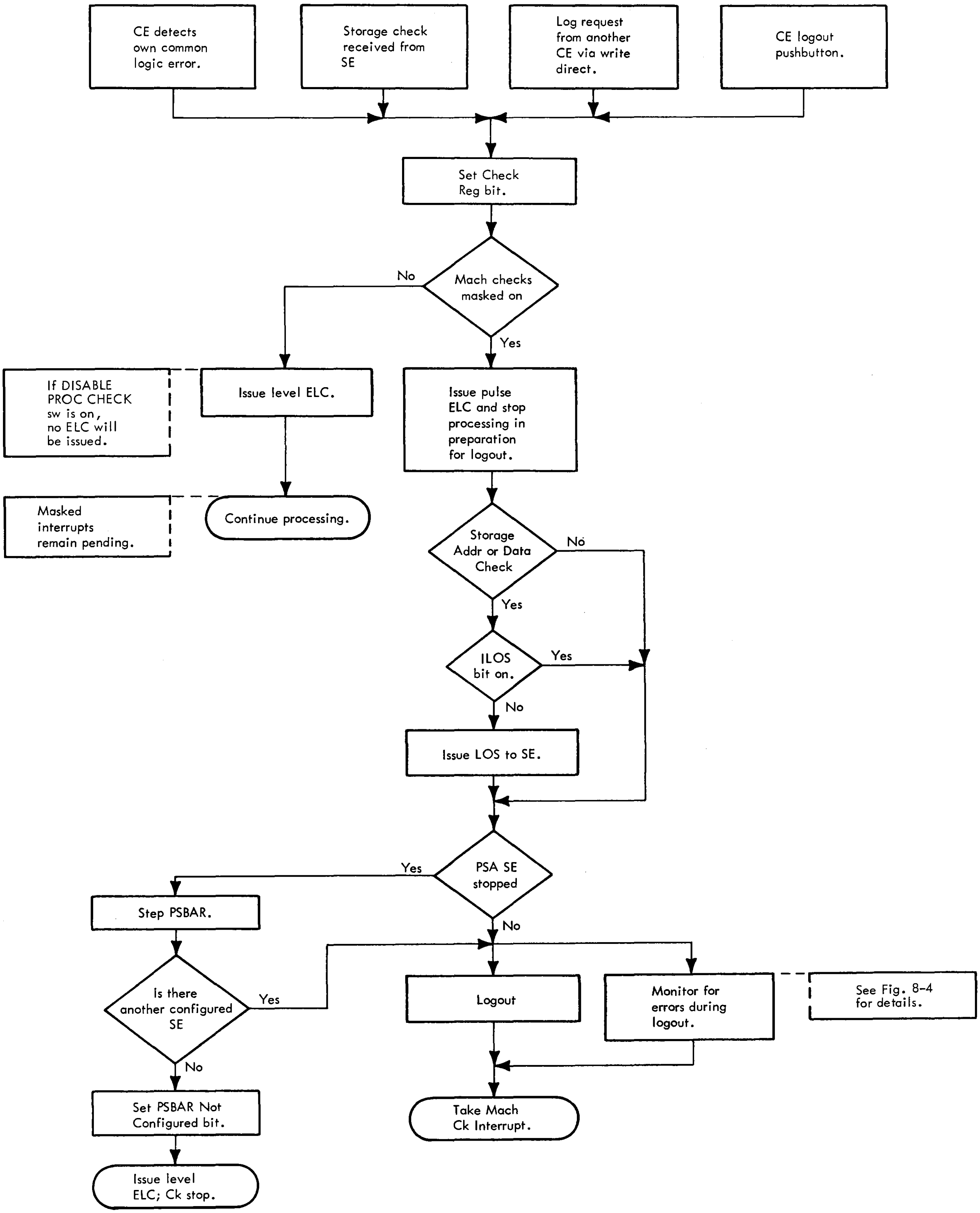


Figure 8-2. CE Error-Handling

which it is working, the appropriate bit is set in check register 1 or 2. A logout and a machine-check interrupt will then occur if machine-check interrupts are masked on in the current PSA (bit 13 on). If machine-check interrupts are masked off, a level element check (ELC) is issued to all other CEs, and the issuing CE attempts to continue processing until a change in the mask allows the pending interrupt to take place.

When the mask permits, a pulse ELC is issued to all other CEs, and the CE stops processing in preparation for logout. If the error was from storage (and the ILOS bit is not on in the CE's CCR), the CE sends the logout-stop (LOS) signal to the SE and sets the LOS bit in check register 2. The CE proceeds with its logout into the PSA followed by a machine-check interrupt. Normally, the machine-check interrupt handling routine would then recognize the LOS bit in the logout, if it had been set, and would use the Diagnose instruction to log out the SE.

It is possible for the SE containing the PSA to be logout-stopped. This is detected when the CE logout begins. PSBAR is then stepped to the alternate PSA. If no alternate is found, the PSBAR not-configured bit is set in check register 2, a level ELC is issued, and the CE checkstops.

CE Handling of SE Access Response Errors

- Program interruptions if SE stopped or not ready.
- Machine check interruption if SE not stopped and ready.

In addition to the error-handling discussed so far, the CE must be able to handle the condition in which an SE fails to respond to a storage request. In this case there is no data or address check; the SE simply fails to respond. Figure 8-3 shows how the CE handles SE access response errors. Upon making a storage request to a particular SE, the CE checks the 'SE stopped' and 'SE ready' lines from that SE. If the SE is stopped or not ready at this time, a program interrupt is indicated, since the program should not have attempted to access a stopped or not-ready SE. The appropriate interruption code is set into the program old PSW. A program interrupt should now occur and therefore the PSA SE must be accessed. A check is made to see if the original request was to the PSA area. If it was not, a request to the PSA SE is forced. If it was, then the PSA SE is known to be stopped or not ready. In 360 mode, the CE will checkstop since further operation is impossible. In normal operation, however, PSBAR is stepped and an access is made to the alternate PSA area. A check is first made of the 'alternate' latch. If it is already on, the original access was to the alternate PSA. In this case 'PSBAR Alternate Check' is set, a level ELC is issued to all other CEs, and the CE checkstops. Normally, the 'alternate' latch would be found to be off and would be set at this time. PSBAR is then stepped, ILOS permitting. If another configured SE is found, a select is forced to it. Should no other configured SE be found, 'PSBAR not configured' is set, a level ELC is issued to all other CEs, and the CE checkstops.

Note that PSBAR is stepped when a machine check occurs on an access to any location in the PSA SE, whether to the actual PSA or not, but, when a program check occurs, PSBAR is stepped only on an access to the PSA itself.

Returning to the beginning of the flowchart in Figure 8-3, note that when the SE is not stopped and is ready, a select is issued and a nominal 25-ms timedown is entered. This timedown actually varies between 16 and 32 ms. Normally the 'accept' pulse is received from the SE much sooner than this, so the time is not critical. However, should the SE fail to respond with 'accept', a timeout will occur, preventing an indefinite hang condition. Note that the SE-stopped and not-ready conditions are still monitored during the timedown.

In the event of an SE timeout, a pulse ELC is issued to all other CEs and a pseudo accept in generated within the CE to allow resetting of the storage request circuitry. The 'SE timeout' bit is set in check register 2, and preparation is made for a logout into the PSA area. If machine checks are masked off, the CE will attempt to continue processing. In this event the pulse ELC already issued alerts other CEs to the condition. When machine checks are masked on, however, the current instruction is terminated and the same procedure for locating the PSA area is followed as for the program interrupt conditions described previously. However, a logout is initiated at the end of this procedure rather than a program interrupt.

CE Error-Monitoring during Logout

- Most errors ignored during logout.
- Only errors that could cause incorrect or incomplete logout are checked:
  - Invalid address.
  - SE timeout.
  - SE stopped.
  - Log ROS check.
  - Log address check.

Note that the CE continues to monitor for errors during a logout. Error-handling during logout is different from normal error-handling. This is shown in Figure 8-4.

Most errors are ignored during logout. However, certain errors which would result in an incorrect or incomplete logout must be checked. Figure 8-4 shows that in the event of an 'invalid address' or 'SE timeout' a check of the

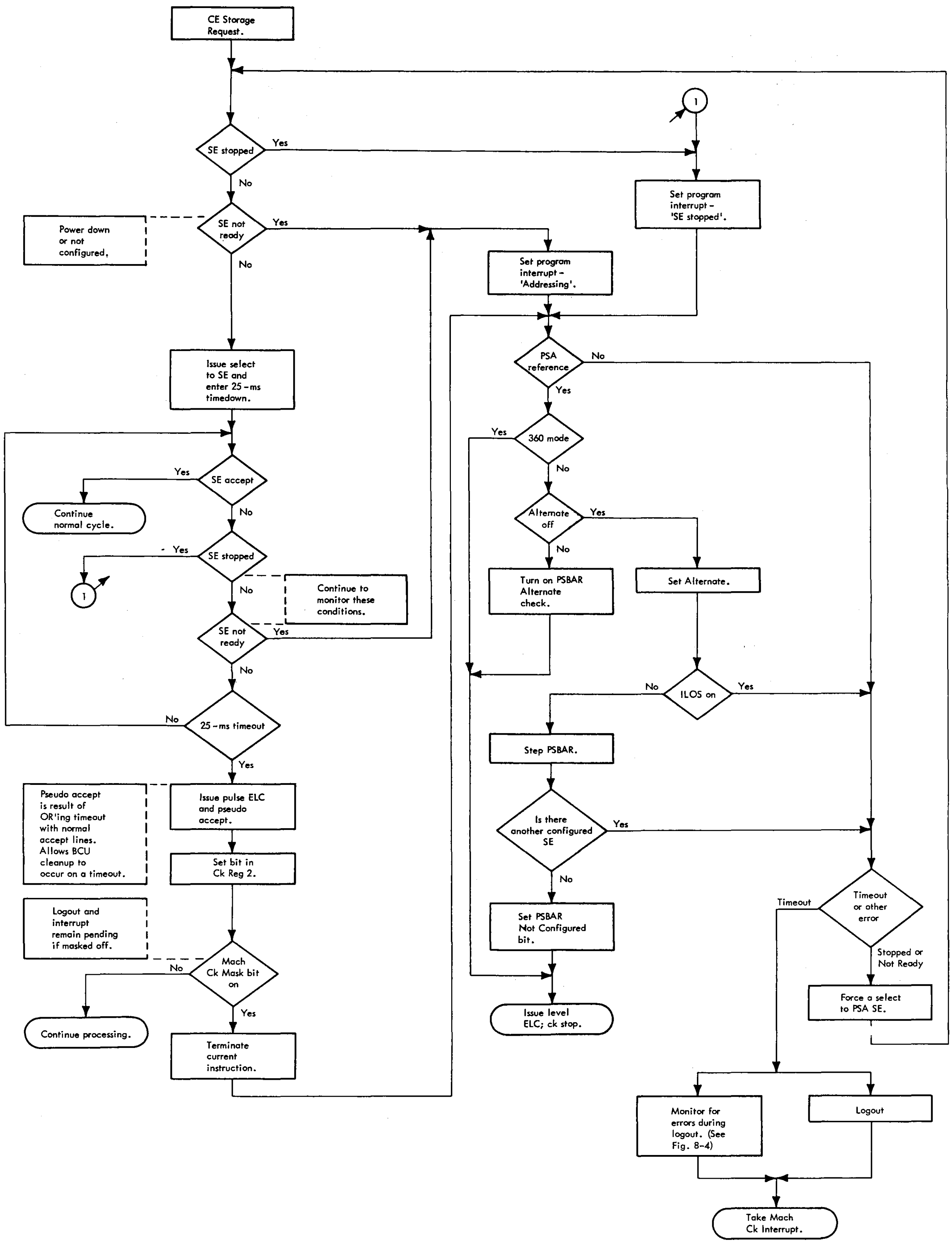


Figure 8-3. CE Handling of SE Access Response Errors

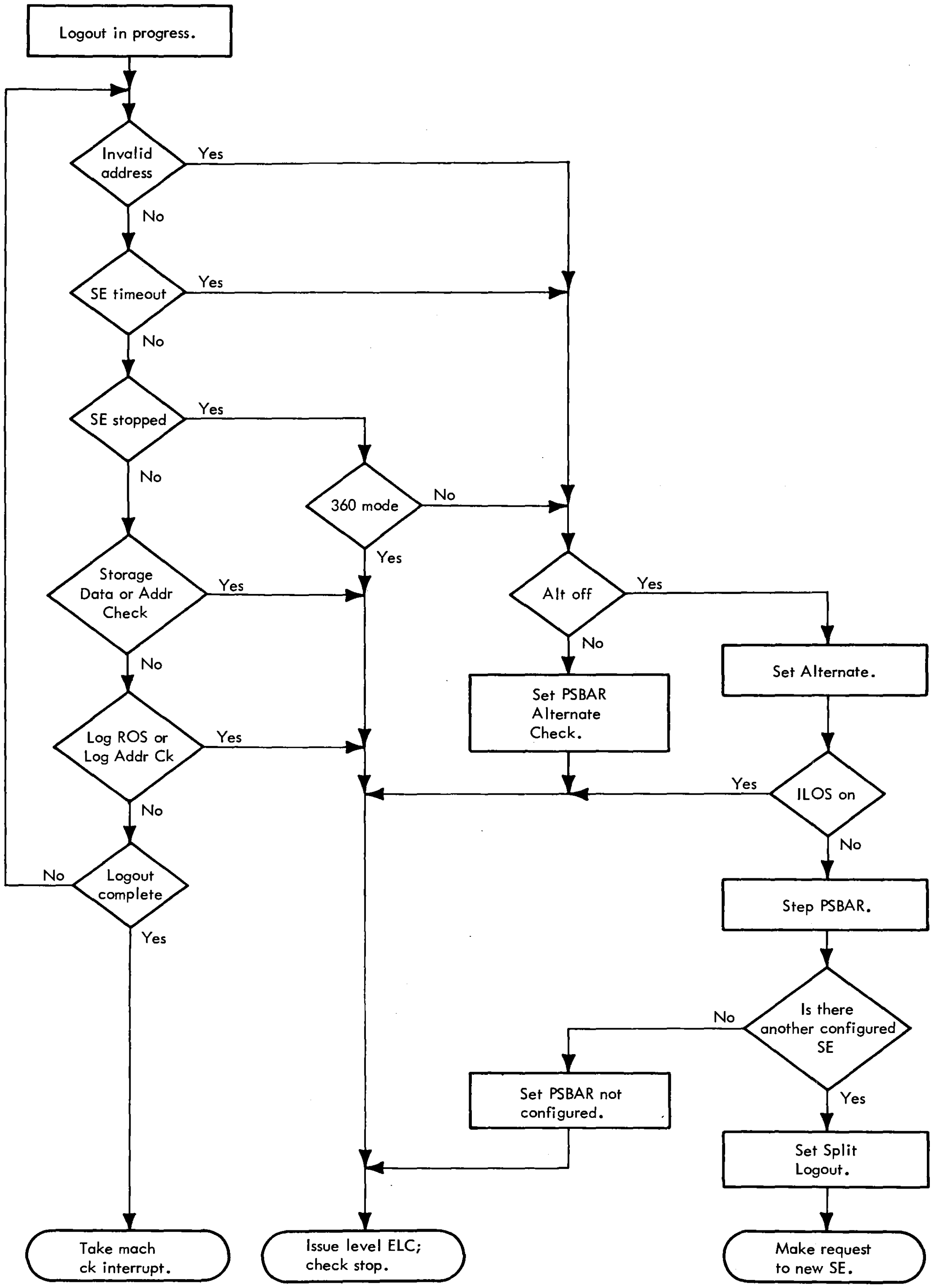


Figure 8-4. CE Error Monitoring During Logout

'alternate' latch is made to determine whether the logout is already being made into the alternate PSA SE. If so, 'PSBAR alternate check' will be set and the CE will issue a level ELC and checkstop. If not, PSBAR will be stepped, the ILOS bit permitting. If another configured SE is found, the split logout bit is set in check register 2 and a request is made to the new SE. Should no other configured SE be found, the PSBAR not-configured bit is set in check register 2, a level ELC is issued to all other CEs, and the CE checkstops.

The same procedure is followed upon detection of an SE-stopped condition unless operating in 360 mode. In 360 mode, the CE checkstops immediately upon detection of SE-stopped during logout.

During logout, the CE also monitors for 'log ROS check' and 'log address check', which would indicate that some ROS address outside the logout routine had been accessed or that log data was to be stored outside the PSA area. These checks will cause the appropriate bit to be set into check register 2. Storage data and storage address checks are also monitored during logout. The detection of any of these errors causes a level ELC to be issued and the CE to checkstop.

CE Handling of Internal Abnormal Conditions

- OTC or OBS causes external interruption of the CE in which it occurs.

- Internal and external logic checks result in ELC to all CEs:
  Pulse ELC if machine-checks masked on.
  Level ELC if machine checks masked on.

Figure 8-5 shows the way in which the CE handles abnormal conditions arising within the CE itself. The four consecutive decision blocks, together with the loop back to the entry, represent hardware monitoring of abnormal conditions. This diagram is for purposes of explanation only and does not imply looping or scanning by the hardware. An OTC or OBS arising in the CE sets the CE-own-OTC or CE-own-OBS bit, respectively, in DAR. No signal is sent to any other CE as it is expected that the CE will handle these conditions itself. If external interrupts are not masked off in the current PSW and the DAR Mask permits, the CE takes an external interrupt.

A logic check, internal or external, causes an ELC to be sent to all other CEs. If machine-check interrupts are masked on, a pulse ELC is sent and a logout and machine-check interrupt ensues. If machine-check interrupts are masked off, however, the CE attempts to continue normal operation. In this case, a level ELC is sent to all CEs to alert them to the fact that this CE cannot properly handle this condition.

Checkstop, power check, or power down also causes a level ELC to be sent to all other CEs.

IOCE Error-Handling

The IOCE continually monitors for errors occurring within its own common logic and channels, for errors related to its operation with SEs, and for abnormal conditions. The manner in which the IOCE handles these errors and abnormal conditions is described in the following text.

IOCE Handling of CLU Errors

- CLU monitors and logs out:
  1. Its own errors.
  2. Errors from SE with which it is working.
  3. Selector channel errors that occur during execution of a Test Channel instruction.

- CLU logout also caused by:
  1. Logout request from CE.
  2. Storage timeout and SE not stopped.
  3. CLU or storage check during selector channel logout.

- During logout most errors are ignored but IOCE monitors for errors that would affect validity of logout.

Figure 8-6 shows the IOCE handling of errors detected within the Common Logic Unit (CLU). Errors detected in CLU include errors occurring within CLU, storage errors reported by an SE with which the IOCE is working, and selector channel errors that occur during execution of the Test Channel instruction.

A logout request from a CE is handled in much the same way as a CLU error and is also shown in Figure 8-6. The CE log request bit is set in check register 2 and a CLU logout is initiated. The logic from that point is the same as for CLU errors and is described later.

Note, also, the entry point representing errors described in Figures 8-7 and 8-8. These errors are: (1) a storage timeout on a request to an SE which is not stopped and (2) a CLU or storage check occurring during a selector channel logout. These errors also result in a complete CLU logout.

When a CLU or storage check occurs, the appropriate bit is set in check register 1 or 2 to identify the error. The IOCE then checkstops in preparation for logout and issues a pulse ELC to all CEs. If the error was a storage check, it is desirable to log out the SE as well as CLU. If the ILOS bit is on, the SE is not stopped for logout. However, if ILOS is

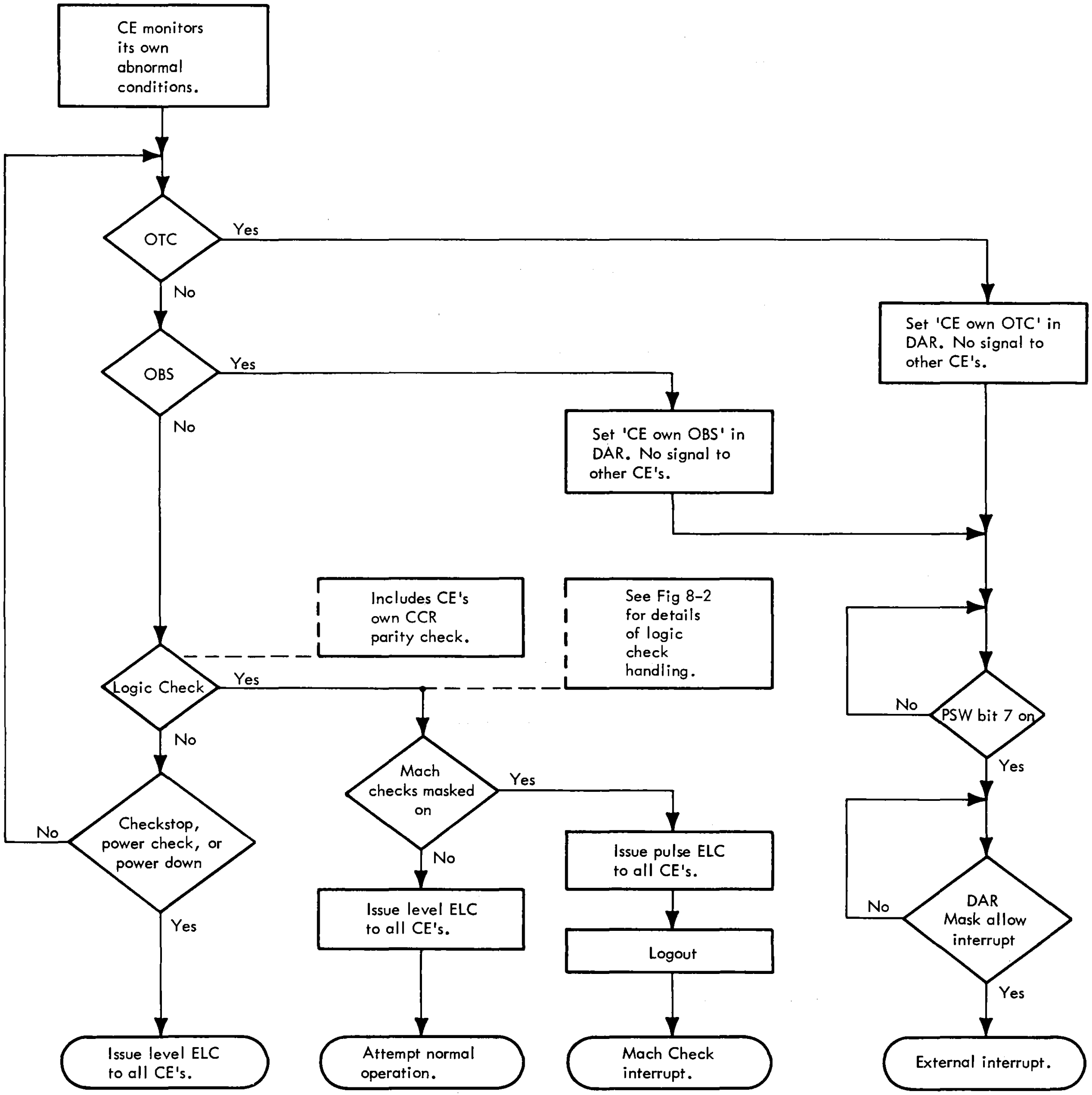


Figure 8-5. CE Handling of Internal Abnormal Conditions

not on, the SE is stopped to preserve its condition at the time of the error for subsequent logout by the controlling CE. It is also desirable to stop the SE for logout when an interface error has occurred, although the logout data is not always pertinent. On a fetch, a check is made for a full-sum check which would indicate an error in data coming into the IOCE; i.e., a fetch data check. If a fetch data check has occurred, the SE is stopped for logout, ILOS permitting.

Whether the SE is stopped or not, the IOCE issues the 'machine-check interrupt request' to the controlling CE and waits for 'permit interrupt' to be returned. This machine-check interrupt differs from the normal one in the CE in that the CE will not perform a logout and will honor the interrupt only at the end of the current instruction. Also, the interrupt will result in an interruption code, in the MC old PSW, of 1, 2, or 3 to identify the IOCE requesting the interrupt. This machine-check interruption is masked by PSW bit 13 in the CE.

When 'permit interrupt' is received from the CE, the IOCE begins the CLU logout. This logout will include a

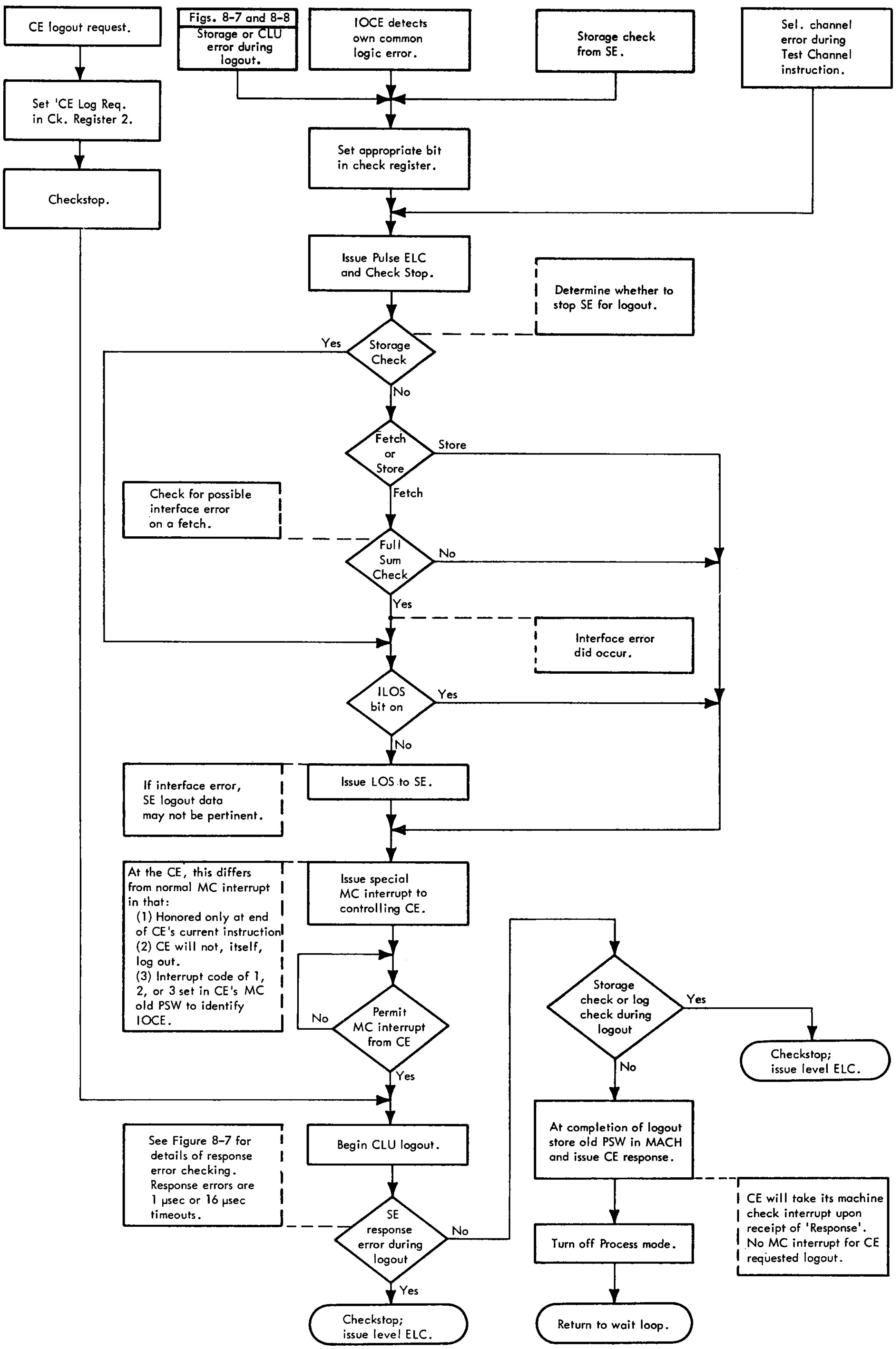


Figure 8-6. IOCE Handling of CLU Errors

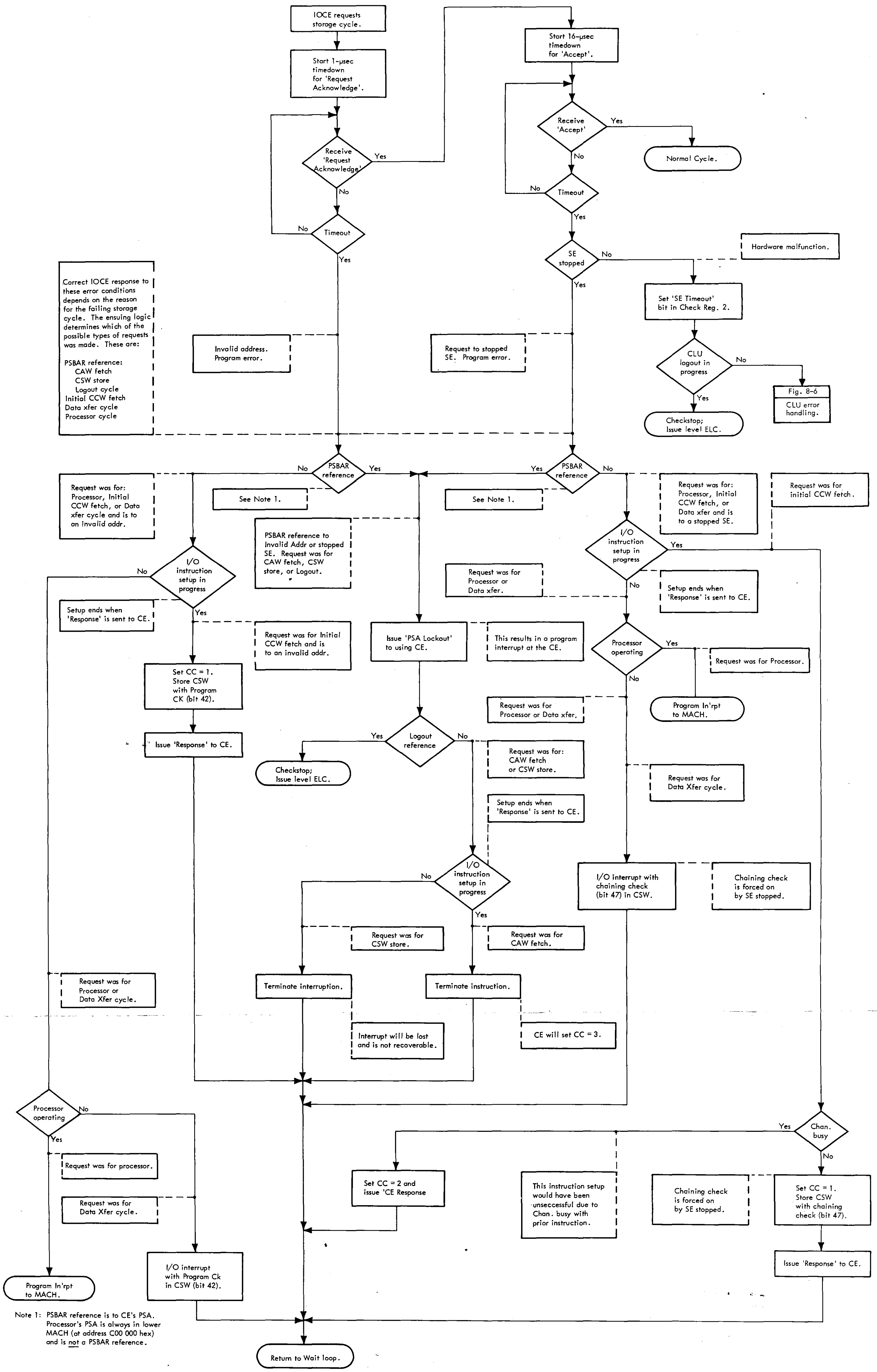


Figure 8-7. IOCE Handling of SE Access Response Errors

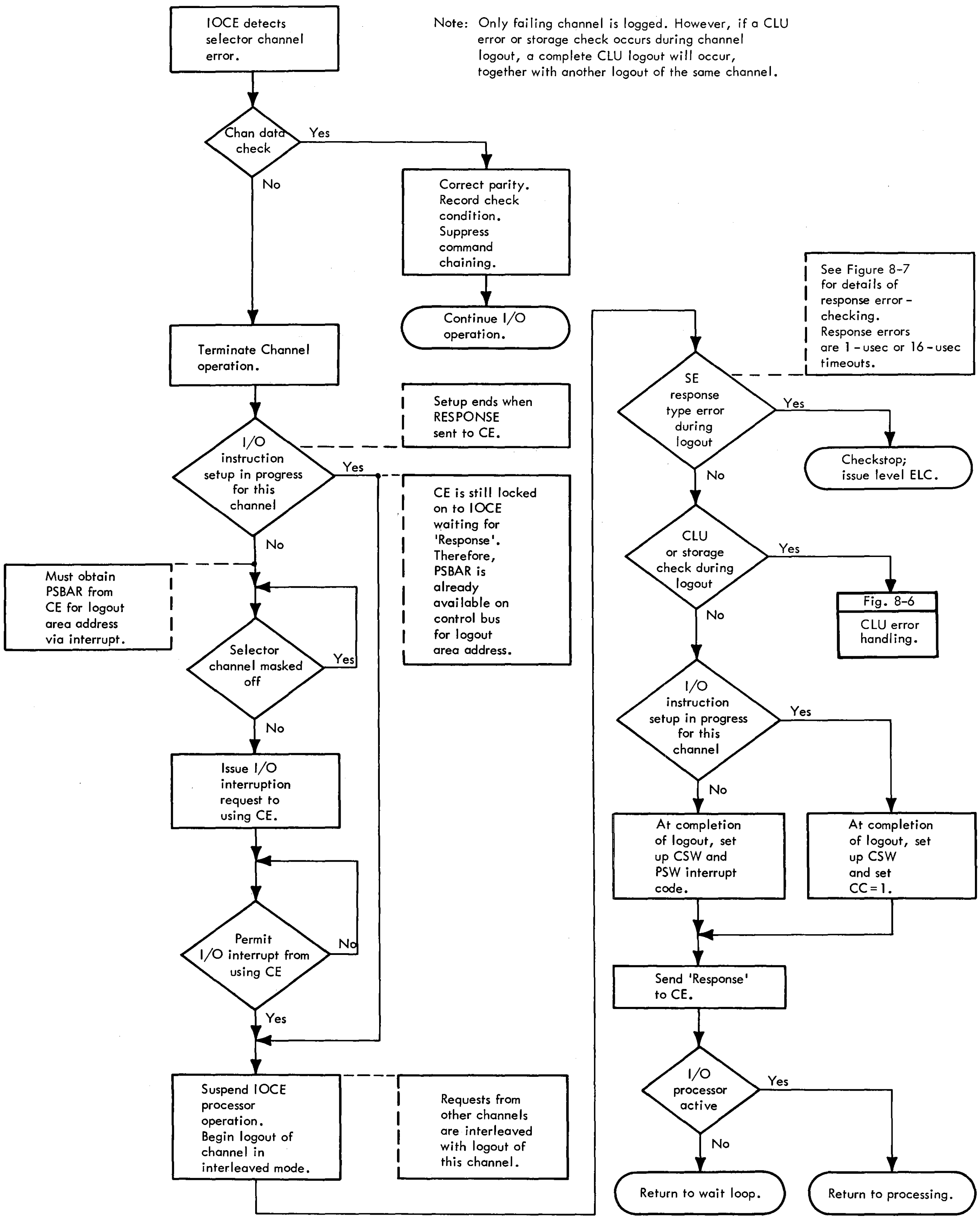


Figure 8-8. IOCE Handling of Selector Channel Errors

logout of common channel, the multiplexer channel, and a single selector channel if one is operating with CLU at the time the error is detected. If no selector channel is operating at that time, the selector channel logout area will contain zeros.

During logout, CLU errors are degated by the 'ignore error' trigger, but the IOCE monitors for errors which would affect the validity of the logout information. As a result, during logout the following errors cause the IOCE to checkstop and issue a level ELC to all CEs: Log ROS check, log address check, invalid ROS address, storage check, storage timeout, and PSA lockout.

At the completion of the logout, the IOCE stores the old machine-check PSW in MACH at location 48 (dec) to provide a return for the processor. This is done whether the processor was operating or not. 'Process mode' is then reset so that the processor will remain in the stopped state until started by a CE.

Returning to the top of Figure 8-6, note that a selector channel error which occurs during a Test Channel instruction also results in a CLU logout. This instruction requires only the use of common channel, so errors during its execution must result in a complete CLU logout to be meaningful.

Note that certain error condition indicated by bits set into check register 2 do not results in a logout. 'Control bus check' indicates that incorrect data has been received from a CE. The IOCE's only action when this occurs is to raise the line 'check response' to the CE. The CE then sets the control bus check bit in its own check register 2 and takes a machine-check interrupt.

The SE LOS and fetch data check bits also cause no IOCE action. However, they provide valuable information in the logout. Fetch data check is always accompanied by a full-sum check which does initiate a logout.

The log checks (log ROS and log ADDR) cause a checkstop and level ELC since they only occur during logout and no further action is possible with these checks present.

The PSA lockout bit is also an exception. It normally results in a program interrupt but, during logout, it causes the IOCE to checkstop and issue a level ELC. The logout cannot continue because the IOCE is unable to access the PSA SE.

One other exception to the normal error-handling scheme is the CCR parity check bit, explained later under "IOCE Handling of Abnormal Conditions".

IOCE Handling of SE Access Response Errors

- Invalid address if 'request acknowledge' not received within 1 usec.
- Hardware malfunction if 'accept' not received within 16 usec and SE not stopped.
- Program error if 'SE timeout' occurs for a stopped SE.

The IOCE must also be able to handle the condition in which an SE fails to respond to a request for a storage access. Handling of SE access response errors is shown in Figure 8-7.

When the IOCE requests a storage cycle, a 1-usec timedown is started. The SE normally responds with 'request acknowledge' before 1 usec to indicate that the IOCE's request has been received and that the access will be granted when the SE priority scheme permits. The IOCE then starts a 16-usec timedown to wait for 'accept' from the SE to indicate that the access has been granted.

If 'request acknowledge' is not received within 1 usec, timeout is interpreted as an invalid-address condition. That is, the request was made to an SE which was not physically present, was powered down, or was not configured. This is a program error.

If, during the 16-usec timedown, 'accept' is not received, the 'SE stopped' line is examined. If the SE is not stopped, the timeout is interpreted as a hardware malfunction. Since the SE did send 'request acknowledge' and is not stopped, only a malfunction can prevent 'accept' from being received. In this event, the SE timeout bit is set in check register 2 and preparation is made for logout as previously described. If the access request was made as a result of a CLU logout already in progress, no further action is possible, and the IOCE checkstops and issues a level ELC to all CEs.

The IOCE cannot do a split logout since it cannot step PSBAR. It is expected that the program for the controlling CE would handle this condition as a result of the level ELC from the IOCE. The program can do a Write Direct Logout to the IOCE and may supply a new PSBAR, using the Load PSBAR instruction. Forcing an IOCE logout to a new PSBAR setting has the effect of a split logout. There is no IOCE hardware involved in this effective split logout, however.

Still referring to Figure 8-7, note that the condition in which the SE is stopped when an SE timeout occurs is considered a program error. Correct IOCE response to this condition, as well as to the 1-usec timeout condition, depends on the nature of the storage access request being made. The remainder of the logic in Figure 8-7 determines what type of access was being made and generates the correct response.

This is clearer if it is realized that the IOCE can make a storage access request for one of only six reasons:

CAW fetch
CSW store

Logout access
Initial CCW fetch
Data transfer cycle
Processor access

The first three of these are PSBAR references; that is, accesses to the CE's PSA area. This should not be confused with accesses to the processor's PSA area, which is always in lower MACH and is not a PSBAR reference.

The first decision block after each of the program error conditions (invalid address and SE stopped) determines whether the request is a PSBAR reference. If so, the IOCE issues 'PSA lockout' to the using CE, resulting in a program interrupt at the CE.

As implied previously, a PSBAR reference can only be a CAW fetch, CSW store, or a logout access. If a logout is in progress, the IOCE checkstops and issues a level ELC. If not, the access is either a CAW fetch or a CSW store. Which of these is the case is determined by checking if an I/O instruction is presently being set up. The setup, or initialization, of an I/O instruction is normally completed by sending 'response' to the CE to release the CE for further processing. If an I/O instruction is being set up, the request must be a CAW fetch since the only other possibility is a CSW store which occurs after the setup is complete. The instruction is terminated and no response is sent to the CE, causing the CE to set the condition code to 3 (unavailable). After terminating the instruction, the IOCE returns to the wait loop.

If no instruction setup is in progress, the request was to store a CSW. The interruption is terminated. This interrupt is lost and is not recoverable. The 'PSA lockout' and subsequent CE program interrupt will alert the program to this condition. Upon termination of the interruption, the IOCE returns to the wait loop.

A storage access request which is not a PSBAR reference must be an initial CCW fetch, a data transfer cycle or a processor access. The correct IOCE responses to these conditions depend on whether the access was to an invalid address or to a stopped SE. The "no" exit from the left-hand decision block marked "PSBAR reference" represents the case of a request to an invalid address.

The next decision block determines whether an I/O instruction setup is in progress. If so, the request was for the initial CCW fetch. Since the CE is waiting for 'response', the IOCE sets the condition code to 1, stores a CSW with the program check bit on, and sends 'response'. The program check (bit 42) in the CSW alerts the program to the invalid address condition. The IOCE then returns to the wait loop.

If no I/O instruction is being set up, a check is made to see if the processor is operating. If it is, a program interrupt into MACH is taken to alert the processor program. If not, the access can only be a data transfer operation for an I/O operation already in progress. In this case, an I/O interruption is taken to the CE's PSA area. The program check bit is stored in the CSW, and the IOCE again returns to the wait loop.

The remaining case of a request to a stopped SE for a non-PSBAR reference is shown at the "no" exit from the right-hand decision block marked "PSBAR reference". The three possible types of access requests are handled here as they were for a request to an invalid address except that, where a CSW is stored the chaining check (bit 47) is set on. The chaining check is forced on by 'SE stopped'.

IOCE Handling of Selector Channel Errors

- Data checks recorded but operation is continued.
- For errors other than data checks operation is suppressed in preparation for logout.
- Contents of using CE's PSBAR must be obtained to effect logout.
- Error monitoring continues during logout.

Figure 8-8 shows the handling of selector channel errors by the IOCE. It should be recalled that errors occurring during execution of a Test Channel instruction are not handled here but, rather, are grouped with CLU error-handling as previously described.

When an error is detected within a selector channel, it is first determined whether the error was a data check. If it was, the operation is allowed to continue, but the check is recorded, parity is corrected in the data, and command chaining is suppressed. For errors other than data checks, the operation is terminated and the selector channel prepares to log out. The contents of the using CE's PSBAR must be available for the logout to proceed. If an I/O instruction setup is in progress, the CE is waiting for 'response', and PSBAR is available on the control bus. In this case the logout can proceed immediately. If no I/O instruction is being set up, the selector channel must issue an I/O interrupt to obtain PSBAR. If selector channel interrupts are not masked off, the interrupt is taken when 'permit I/O interrupt' is received from the CE. With PSBAR available, the selector channel proceeds with the logout.

Error-checking continues during the selector channel logout. An SE response error causes the IOCE to checkstop and issue a level ELC to all CEs. Any storage or CLU error will result in a complete CLU logout. In this case a second logout of the same selector channel would occur at the end of the CLU logout. The data in the selector channel logout area would then reflect the channel condition at the time the CLU or storage error occurred rather than at the time the channel error occurred.

At the completion of the selector channel logout, the IOCE action depends on whether an I/O instruction was being initiated when the malfunction occurred. If so, a CSW is stored, the condition code is set to 1, and 'response' is sent to release the CE from the instruction hold. If no I/O instruction was being set up, the CE is waiting for 'response' to clear the hold for the I/O interruption used to obtain PSBAR. The IOCE sets up a CSW and the interruption code in the I/O old PSW. Response is then sent to clear the interruption hold. The IOCE now returns to processing if it was in process mode, or to the wait loop if it was not in process mode.

IOCE Handling of Abnormal Conditions

- IOCE abnormal conditions (OTC and OBS) recorded in CE's DAR.
- CCR parity check during SCON results in 'pulse OBS' to all CEs. IOCE ignores SCON.
- CCR parity check when no SCON is being received results in a logic check (CCR parity-check bit set in check register 2).

Figure 8-9 illustrates the handling of abnormal conditions by the IOCE. The series of five decision blocks at the left, together with the loop back to the beginning, represent the hardware abnormal condition monitoring. This diagram is for purposes of explanation only and does not imply actual looping or scanning operation in the hardware.

It should be recalled that IOCEs report abnormal conditions to CEs via two signals: OTC and OBS. There are two corresponding bits for each IOCE in the DAR of each CE. Both bits on together indicate ELC.

Still referring to Figure 8-9, note that a temperature OTC condition causes a level OTC signal to be issued to all CEs. An OBS causes a level OBS to be issued to all CEs. In both of these cases normal operation continues.

A CCR parity check is handled as a logic check when it occurs spontaneously rather than during a reconfiguration. That is, the CCR parity check bit is set in check register 2, a pulse ELC is issued, and a request for logout is made. However, if incorrect data is sent by a CE during a reconfiguration, the IOCE issues a pulse OBS to all CEs and ignores the SCON. The IOCE then continues normal operation in the original configuration. The pulse OBS signal was chosen to differentiate this condition from other abnormal conditions.

A logic check causes a pulse ELC to be issued to all CEs. That is, both the OTC and OBS lines are pulsed. Logic-check handling has been previously described.

The remaining possible abnormal conditions are check-stop, power check, and power down. These conditions result in a level ELC (i.e., level OTC and OBS) being issued to all CEs.

SE Error-Handling

- All error conditions result in ELC to all CEs.
- Logic checks are further identified (i.e., data, address, storage) to the using CE or IOCE.
- An SE logout must be performed to identify errors other than logic checks.

Figure 8-10 shows the action that occurs in an SE when it detects an error. An error occurring in the SE's internal logic is recorded in the error latches within the SE. This information becomes the contents of logwords 5 or 11 upon an SE logout.

If the error is a data check, 'suppress log check' is examined. The 'suppress log check' signal is raised by the CE or IOCE to suppress indication of an expected data check. Therefore, the SE continues normal operation when 'suppress log check' is on. Otherwise a pulse ELC is issued to all CEs, and the applicable storage, data, or address check is issued to the using element (CE or IOCE).

Having alerted the system and the using element of the error, the SE enters a 2.5-usec timeout to await a possible 'logout stop' (LOS) signal. If LOS is not received within 2.5 usec, the SE resets the error and priority scanning is again started.

If the LOS signal is received before the 2.5-usec timeout occurs, the SE issues 'SE stopped' to all configured elements and a level ELC to all CEs. It then waits to be logged out. When 'logout complete' is received, the SE drops the level ELC and returns to normal operation. In the absence of 'logout complete', the SE will also respond to a reset or a reconfiguration.

Referring to the smaller flowchart on Figure 8-10, note that the SE responds to abnormal conditions other than logic checks. These are: power down or power check, temperature OTC, OBS, and CCR parity check. An abnormal power condition causes a level ELC to be issued to all CEs. The remaining conditions result in a pulse ELC check to all CEs. After issuing the pulse ELC, the SE returns to normal operation.

All abnormal conditions are reported to the CEs as ELC. Only a logic check is accompanied by more specific check information (data check, address check, or storage check); this is issued only to the using element. An SE logout must be performed to determine the specific cause of an ELC for other abnormal conditions.

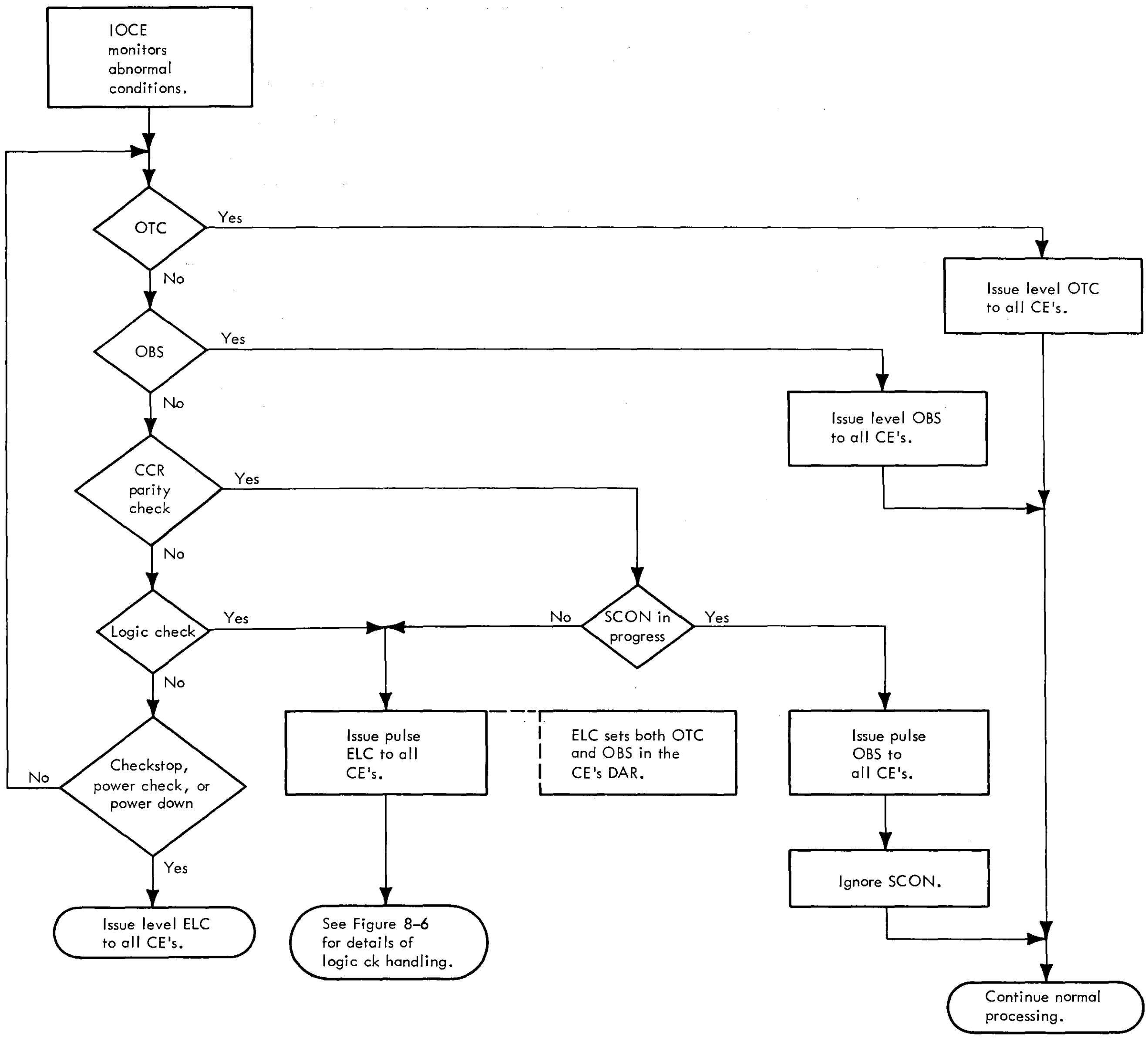


Figure 8-9. IOCE Handling of Abnormal Conditions

TCU Error-Handling

- Logic errors recorded in sense register.
- Unit check bit set in status register.
- Power check or CCR parity check results in ELC to all CEs.
- CCR parity check sets bit 5 in sense byte 3.
- OTC turns on thermal indicator and sets attention bit in status register; no ELC sent.

Figure 8-11 depicts the manner in which error conditions are handled by the TCU. The left entry represents errors detected by the internal logic. These errors result in an I/O interrupt with unit check in the status byte. No logout facility is provided, but details of the malfunction are retained in the sense register and are made available to the program through the Sense command. The right entry represents detection of an abnormal condition. Possible abnormal conditions are:

Power check or power down
CCR parity check
Temperature OTC

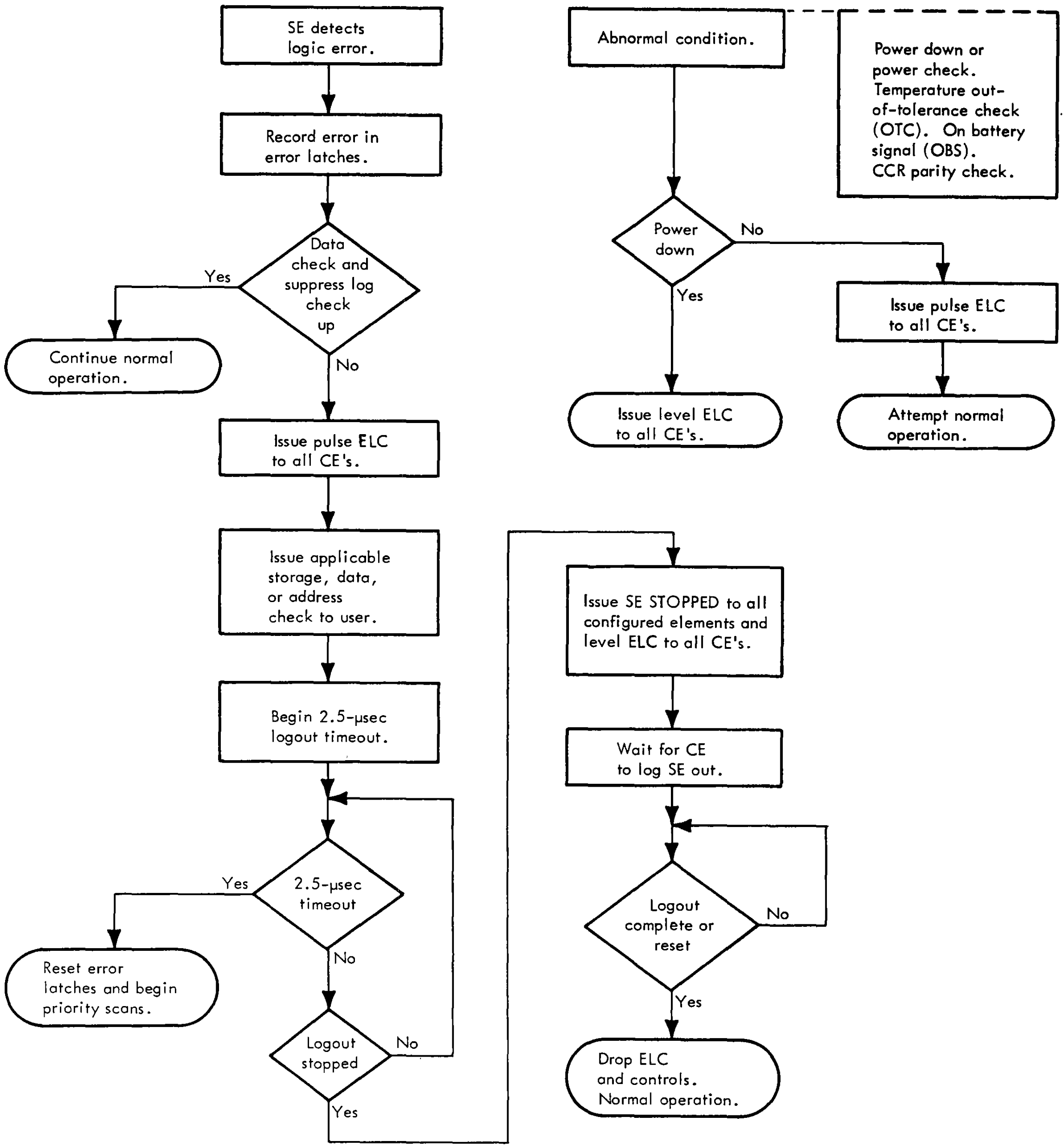


Figure 8-10. SE Error-Handling

Because the TCU does not have battery backup, there is no OBS. Abnormal power conditions and CCR parity checks result in ELC being sent to all CEs. OTC does not cause an ELC; rather, it causes the attention bit to be set in the status register.

When the TCU detects a check condition during the execution of a command (left entry to flowchart), the appropriate bit is set in the sense register to identify the type of check. The unit check bit is then set in the status register. The operation is permitted to continue to completion. At this time, ending status is presented to the channel. If the channel does not accept the status, it is retained (stacked) until the channel accepts it. When the status is accepted, the status byte containing the unit check is transferred to the IOCE, and the status register is reset. As a result of receiving the unit check in the status byte, it is expected that the program will request details of the malfunction by issuing a Sense command. In this event the initial selection sequence occurs, the Sense command is decoded, and the sense bytes are transferred to the IOCE. If the next command is a Test I/O or a No-Op, the sense information is retained and is still available to the program through a subsequent Sense command. If, however, a command representing a new tape operation is received, the

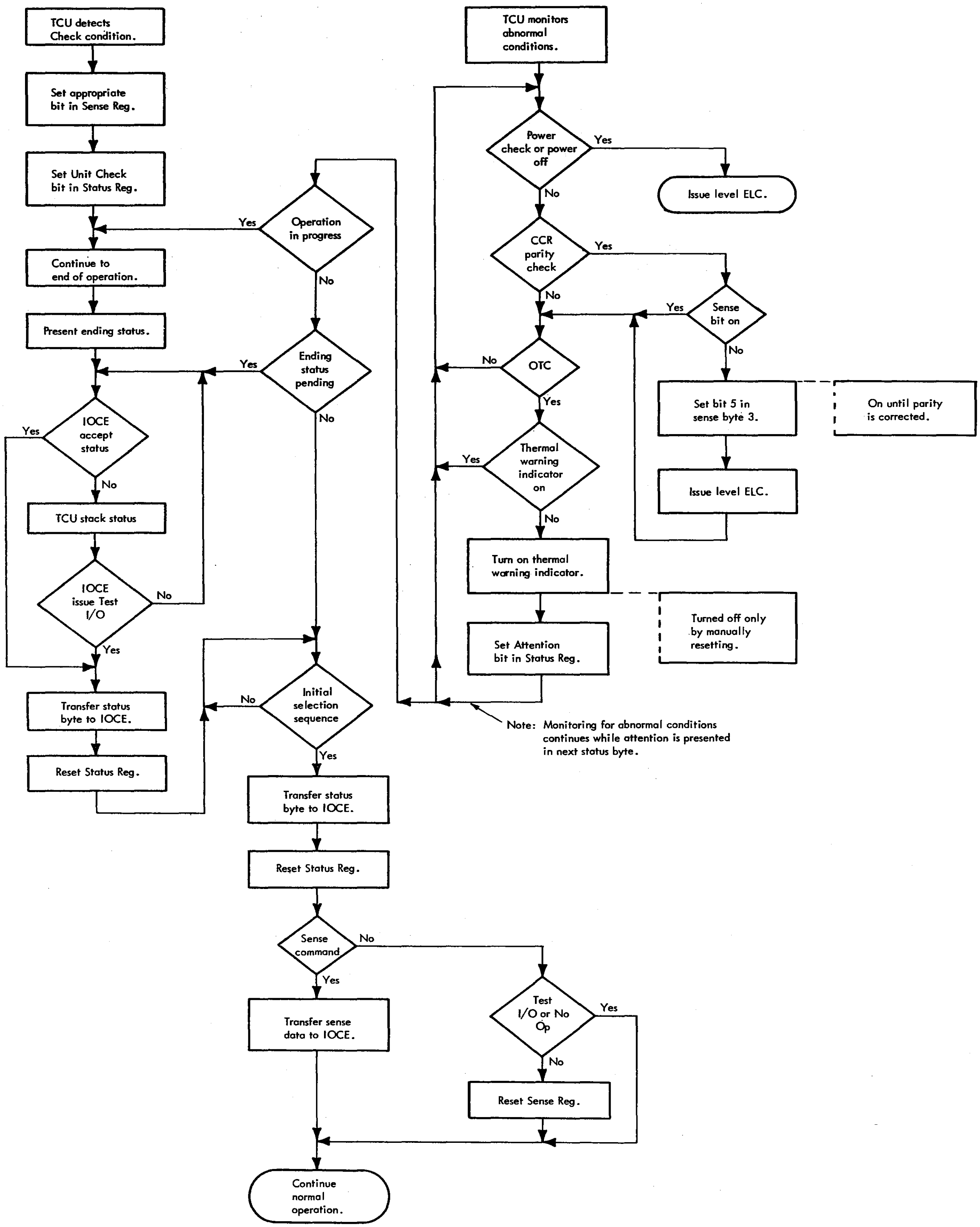


Figure 8-11. TCU Error-Handling

sense register is reset for use during that operation. In that event the detailed information regarding the malfunction is lost.

The TCU continually monitors for abnormal conditions, also. This is represented by the right entry to the flowchart. A power-check or power-down condition causes a level ELC to be issued to all CEs. A CCR parity check also causes a level ELC to be issued to all CEs but, in addition, a bit is set in the sense register (bit 5 of byte 3) so that the program may differentiate this condition from abnormal power conditions via the Sense command. The sense bit and the level ELC remain until parity is corrected in the CCR.

An overtemperature condition in the TCU gives rise to the OTC signal. A pushbutton is also provided to simulate the OTC. When OTC is detected, the TCU turns on a visual thermal warning indicator and sets the attention bit in the status register. This attention status is presented to the channel at the end of the current operation, if one is in progress, or during the initial selection sequence for the next operation. The TCU will not request service from the channel to present the attention bit only. The attention bit is unique to the OTC condition in the TCU and, therefore, requires no further definition to the program.

The attention status is presented only once for any one occurrence of OTC. The thermal warning indicator remains on, however, until it is manually reset. An attempt to manually reset this indicator before the overtemperature condition has been corrected will result in another attention interrupt.

PAM Error-Handling

- Test and Monitor Adapter (TAM) monitors for errors and abnormal conditions in PAM common logic.
- Errors detected by invididual adapters handled via standard I/O interface.

The Peripheral Adapter Module (PAM) is logically divided into the PAM Common section and the various adapters. One adapter, the Test and Monitor (TAM) adapter, works in conjunction with PAM Common to monitor for abnormal conditions and logic errors within the common logic. Errors detected in the individual adapter (whether occurring internally or at the device) are recorded at the adapter itself and reported via the standard I/O interface (through PAM Common) to the IOCE.

PAM Common Error-Handling

Figure 8-12 shows the PAM Common error-handling operation. A power-down or power-check condition results in a level ELC being issued to all CEs. A temperature OTC condition sets bit 6 of the third byte in the sense register of the TAM adapter. No ELC is issued as a result of OTC. However, the condition is reported to the channel via an attention interrupt. This will be discussed later.

A CCR parity error sets bit 5 of the second byte in the TAM sense register, and a level ELC is issued to all CEs. The ELC signal is necessary because the CCR parity error could cause a breakdown in normal (CCR-gated) communications.

The checkstop implementation in the PAM is slightly different from other elements. A 'check stop' latch is set by any error in the priority scanning circuitry. This latch causes priority scanning to cease. To prevent a transient error in the priority circuitry from stopping all PAM operation for an extended time, a command 'bypass check stop' is provided. With this command the program can restart priority scanning as soon as it becomes aware of the error. A solid error would, of course, result in the setting of the 'check stop' latch again.

When the check-stop condition is detected in PAM Common, bit 1 is set in the first byte of the TAM sense register and a level ELC is issued to all CEs. An attention interrupt follows.

Any logic error detected by PAM Common sets the appropriate bit in the TAM sense register. If the error is an out-of-parity address sent from the channel, no further action is taken and the address is ignored. All other errors cause the TAM adapter to request into the channel with attention in the status byte. When the status is accepted by the channel, it is expected that the program will issue a Sense command to obtain details of the malfunction. When the Sense command is received, the TAM sense bytes are sent to the channel. The PAM drops ELC if it is up and continues normal operation unless 'check stop' is set. In this latter case the PAM waits for a Bypass Check Stop command from the channel. 'Bypass check stop' clears the 'check stop' and ELC even though the check condition may still exist.

PAM Adapter Error-Handling

Figure 8-13 depicts the actions taken by PAM adapters when a check condition is detected by the adapter. Check conditions can result from other than logic errors in the adapter; i.e., they may also be caused by errors in data transmission from the channel or device, by conditions reported by the device through its control lines, or by failure of the channel to service an adapter in a particular period of time.

When the adapter detects a check condition, it sets the associated bit in its sense register. If initial selection is in progress, the I/O operation is not performed and the adapter presents status to the channel with 'unit check' in response to the command.

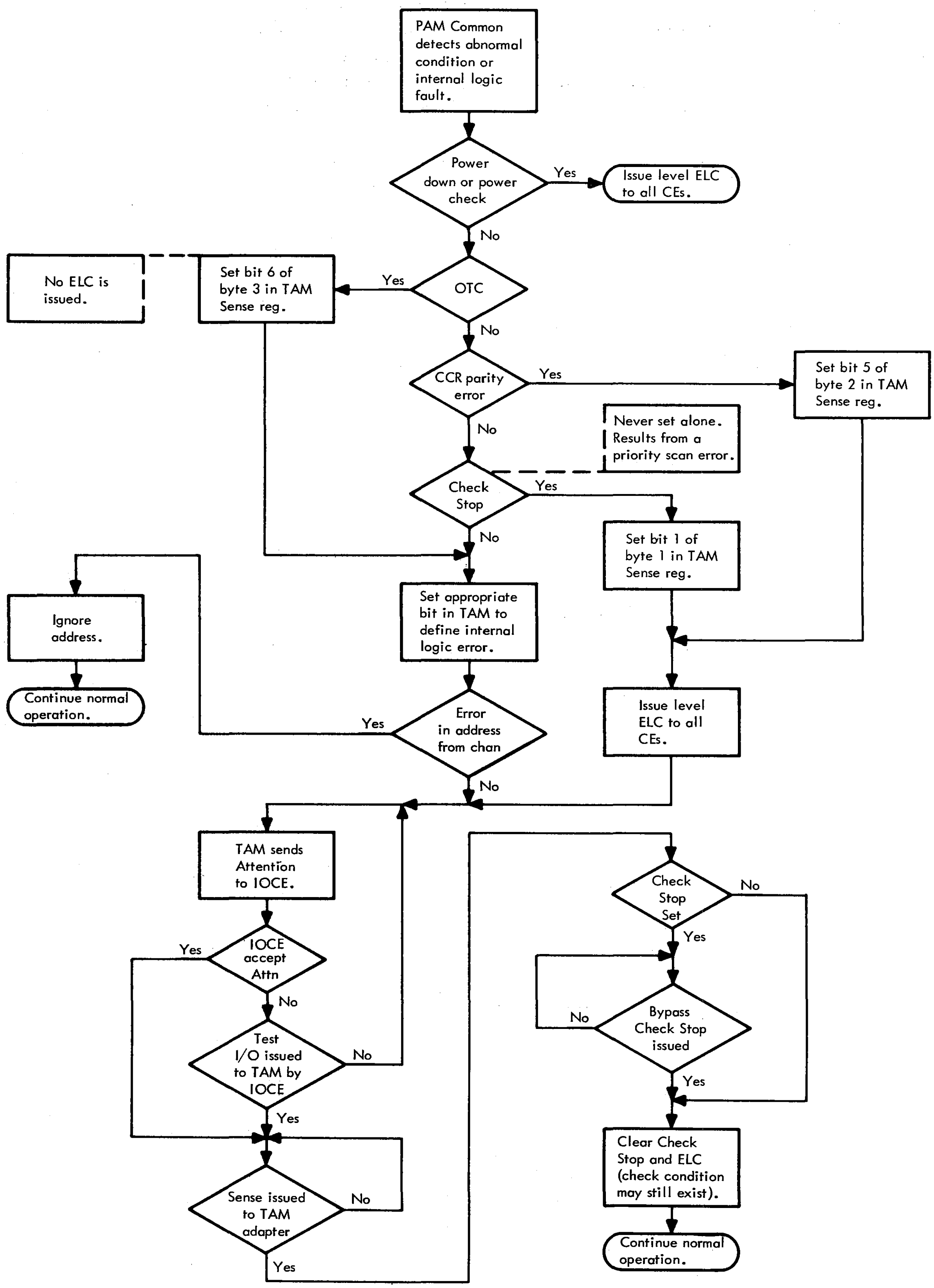
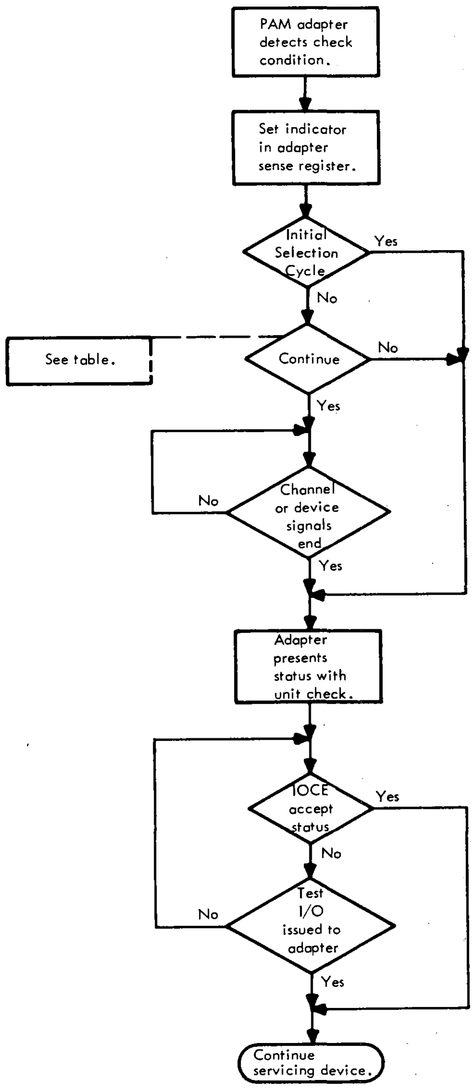


Figure 8-12. PAM Common Error-Handling

If a data transfer operation is in progress, the adapter will either terminate the operation immediately or the device signals the end of transmission.

The table in Figure 8-13 indicates which adapters will continue and which will terminate data transfer for each applicable check condition.

When the data transfer is terminated, the adapter presents ending status with 'unit check'. If the IOCE accepts status or clears status with a Test I/O command, the adapter is free to continue with the next command.



	GPI	GPO	INTI	INTO	TTYLL	RVDP	1052	CD	FDEP
Bus Out Check		T		C	C		C		C**
Data Check	C	T	C	C	C				C
Equipment Check			T				C		
Overrun			T	T	T			T	T
Echo Check					T				T
LRC			C		C				C
Device Inoperative		T							
Device Status 3, 5, 6		T							
Device Status 7		*							
Intervention Req'd							C		T
Timeout									T

T = Terminate C = Continue

Blank - Not applicable during data transfer operations.
* May be wired to terminate or continue.
** In Control mode, adapter terminates.

Figure 8-13. PAM Adapter Error-Handling

SCU Error Handling

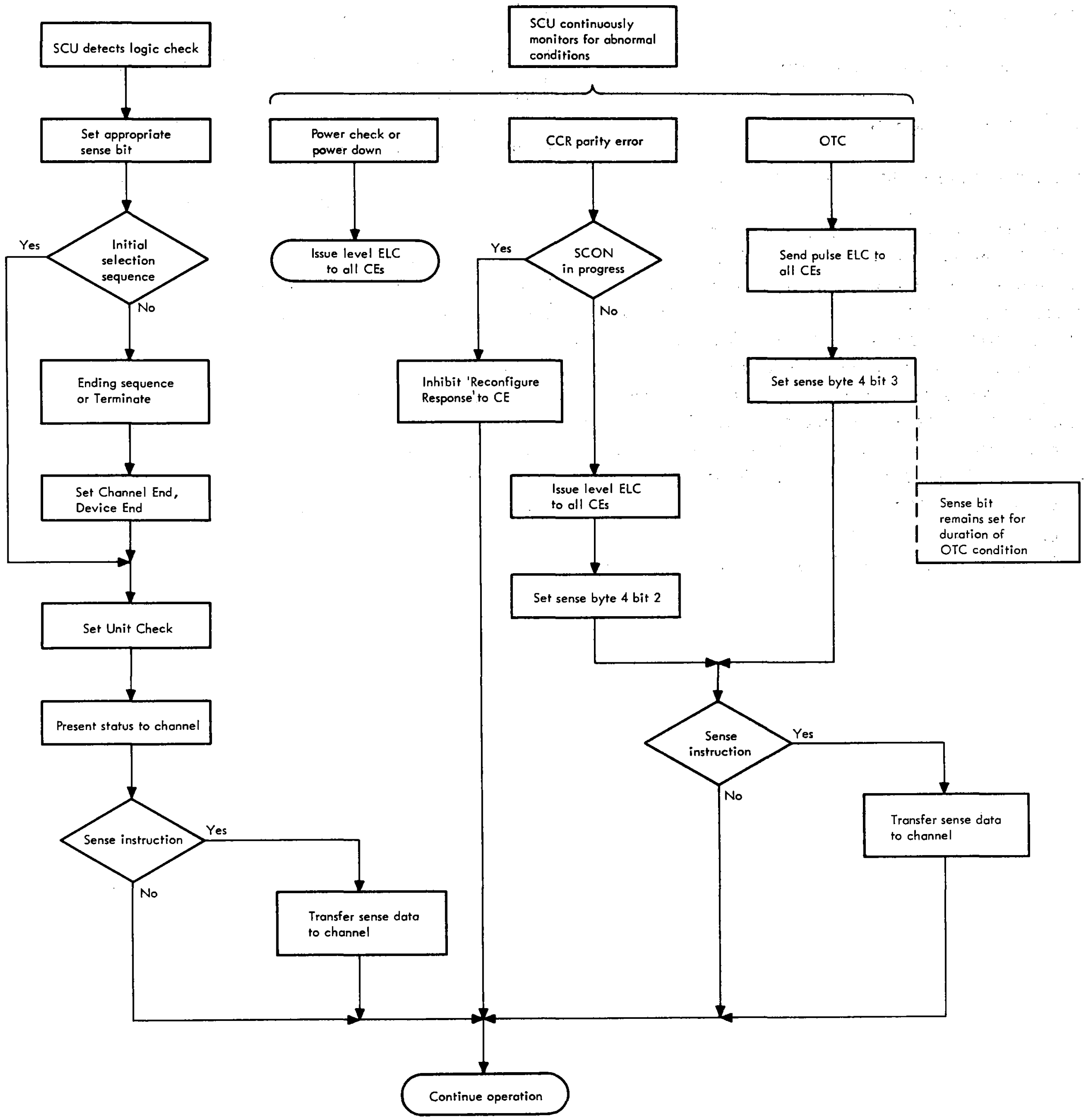
- Logic errors recorded in sense register.
- Unit Check bit set in status register.
- Abnormal conditions monitored continuously.

Figure 8-14 represents, in flowchart form, error handling in the SCU. The left entry represents detection of a logic error within the SCU or attached DSUs. The appropriate bit is set in the sense register to preserve details of the failure. During an initial selection sequence, Unit Check is set in the status register, and status is presented to the channel immediately. If an operation is in progress, an ending sequence or termination of the operation occurs first. Channel End/Device End is set, together with Unit Check. Upon receipt of Unit Check, the program will issue a Sense command to obtain details of the error.

The entries under the bracket on the right of Figure 8-14 show SCU monitoring for abnormal conditions. Power check or a power-down condition causes a level ELC to be sent to all CEs.

A CCR parity check is handled in two different ways, depending on whether it occurs spontaneously or as a result of receiving a SCON. A spontaneously occuring CCR parity check causes a level ELC to be sent to all CEs and bit 2 of sense byte 4 to be set. During a SCON, however, such a parity error is indicated to the CE doing the SCON by withholding 'reconfigure response'. After this time, the SCU will accept a SCON from any CE. This permits reconfiguration of the SCU by another CE if the failure was due to the CE's inability to perform a SCON correctly.

An out-of-tolerance check (OTC) occurs when the temperature rises to within approximately ten percent of the shutdown temperature. OTC causes a pulse ELC to be sent to all CEs and causes bit 3 of sense byte 4 to be set. While the program may perform a Sense command to determine the source of the ELC, it is not necessary that it do so because only OTC can generate a pulse ELC in the SCU.



● Figure 8-14. SCU Error-Handling

System initialization involves resets, initial program load (IPL), and PSW restarting. Resets establish (or re-establish), within the hardware of the elements in which they occur, hardware initial conditions. IPL is the process of reading a program from some external source into storage. Since there may be no operable program in storage at the time, this process is necessarily hardware and ROS-controlled. A reset precedes the IPL automatically so that the program, once loaded, may safely assume initial conditions. Once a program is loaded into storage and has been partially executed, it is possible to restart from initial conditions again via the PSW restart facility. PSW restart is also preceded by a reset. It causes a PSW to be loaded from location zero of the SE in ATR slot 1. The program must have previously placed the proper PSW in this location before PSW restart can be successfully used.

Since these initialization activities usually involve the coordinated operation of a number of elements, they are described at the system level in this manual. Strictly element-oriented actions (e.g., IOCE FLT load) are described in the manual for the particular element.

RESETS

- System reset.
- Subsystem reset.

Two major types of resets occur in the 9020D system: system reset and subsystem reset. These resets are initiated in one element and propagated to other elements until the entire system or a subsystem is reset. Other resets (such as power-on reset in an element or selective reset to an I/O channel) are not propagated in this way. These are described in the individual element manuals.

System Reset

- Resets all elments not in state zero and test.
- Resets all CCR bits except SCON bits which are set to all 1's.
- Resets all channels and I/O devices.

A system reset is initiated in two ways: during a system IPL and during a system PSW restart. Initiation of a system reset via PSW restart or IPL from a CE console is blocked if, at the System Console, the INTERLOCK key is on and that CE is selected by the CE SELECT switch.

A system reset causes all system components not in state zero (with the test switch on) to immediately terminate their current operation and to go into a reset state. In the reset state, the only communication a system element will accept is a configuration mask from any CE or a signal associated with an IPL operation. All control circuitry is reset in each system element upon receipt of a system reset. The configuration control register (CCR) in each element is set to all 0's with the exception of the SCON bits, which are set to all 1's (Figure 9-1).

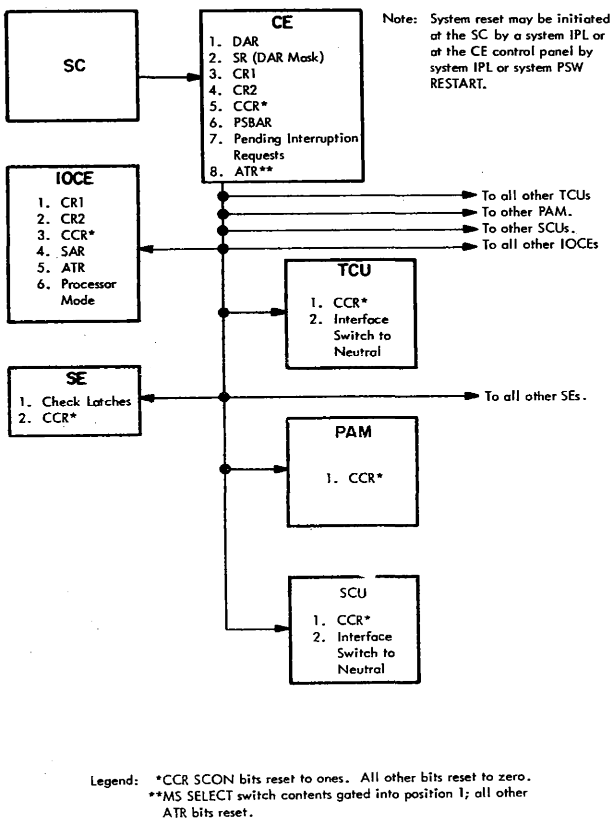
System reset to the IOCE causes an IOCE reset. This reset causes the channel to terminate operations on all subchannels. Status information and interruption conditions in the subchannels are reset, and all operational subchannels are placed in the available state. The channel sends the reset signal to all I/O devices attached to it.

It should be noted that an IOCE reset also occurs when an IOCE is in diagnose mode (no CE communications bit on) and state zero or one is reconfigured to a CE. Note also that turning power on in any element initiates a power-on reset which is a system reset in that element only. This system reset is not propagated to any other element.

Subsystem Reset

- Resets only elements configured to issuing CE.
- Does not affect CCR or ATR in any element.

A subsystem reset occurs when the system reset, subsystem IPL, or subsystem PSW restart facility is used at the CE console or when subsystem IPL is initiated from the SC. A 'subsystem reset' signal is only accepted by those system elements which are configured into the subsystem of the issuing CE. An IOCE reset is performed as in a system reset. Any configurable I/O control units must be configured to an IOCE controlled by the issuing CE to receive the reset. A non-configurable I/O control unit switched to an IOCE will accept the reset. The subsystem reset does not affect the contents of the CCR or ATR in any element. The system elements involved immediately terminate their current operations and reset their control circuitry. SEs are issued a 'logout complete' signal to release them from a possible logout stopped state (Figure 9-2).



●Figure 9-1. IBM 9020D System Reset

INITIAL PROGRAM LOAD (IPL)

- Performed by hardware.
- Two types of normal IPL: system, and subsystem.
- Reset precedes program loading.

The 9020D system uses two types of normal IPL: system IPL, and subsystem IPL. The two are alike in that the CE chosen to initiate the IPL raises the line 'IPL IOCE X' to the IOCE selected by the load unit switches.

The two types of IPL differ principally in the following way: In a system IPL, the CE generates, by hardware, a SCON and a SATR to force a configured system capable of the IPL; in a subsystem IPL, only the SATR is generated.

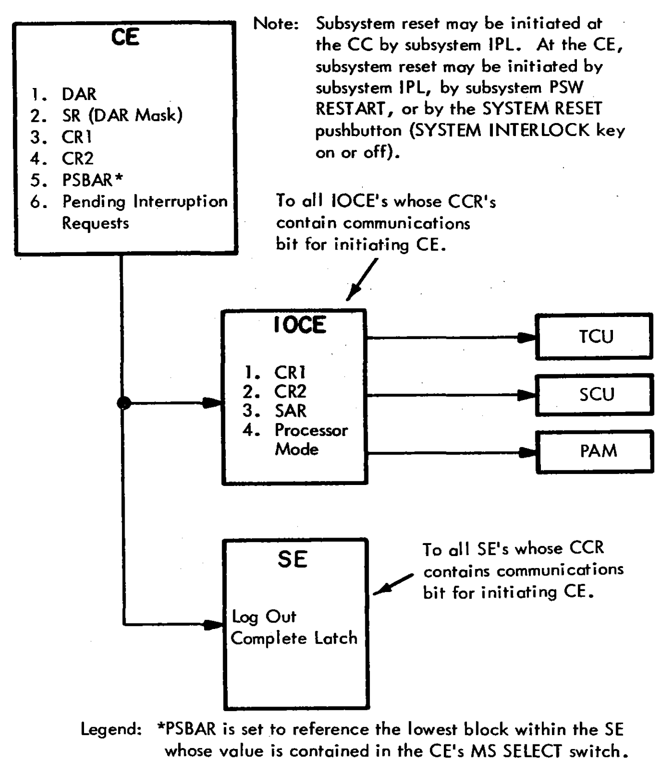
System IPL

- Initiated from CE or SC.
- Must have INTERLOCK key on.
- All elements not in state zero and test are forced to state three.

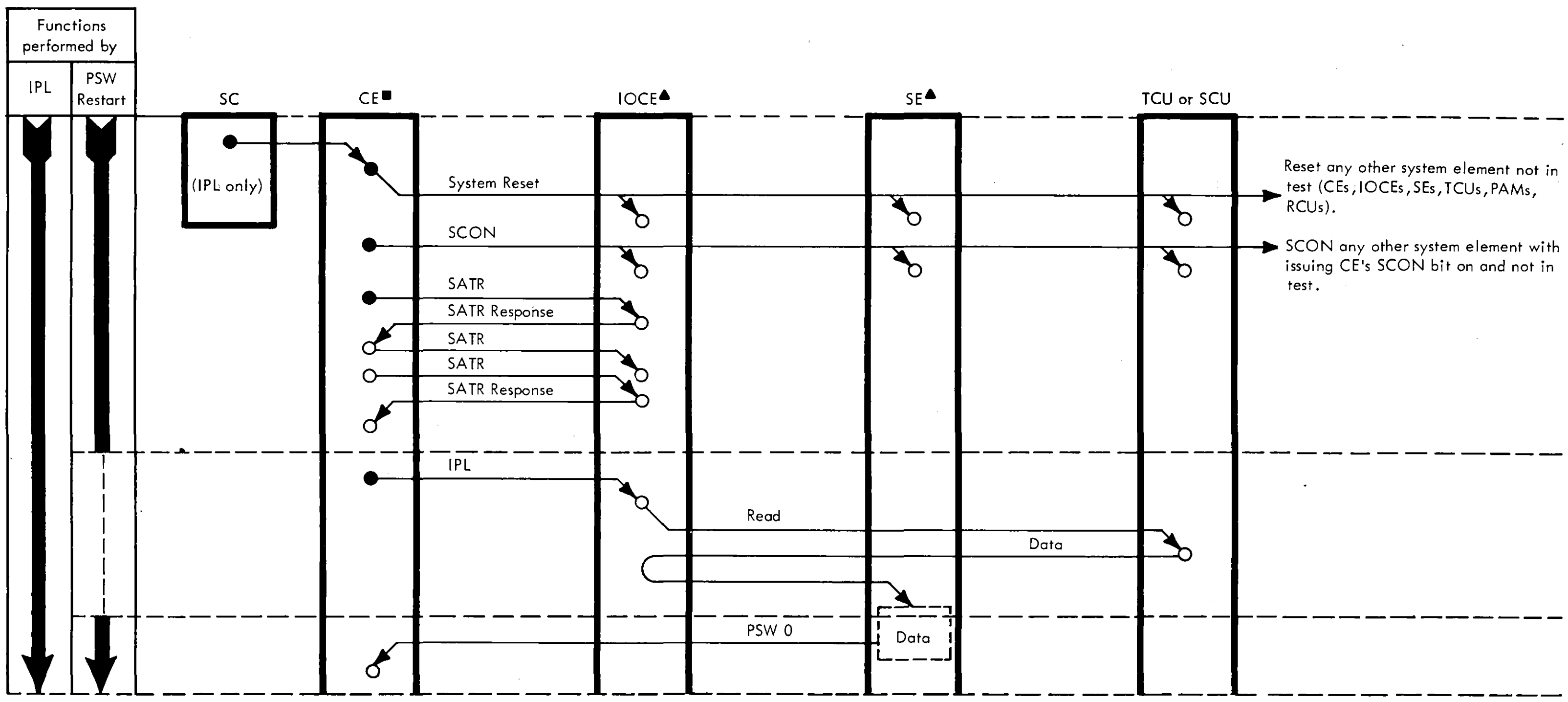
Figures 9-3 and 9-5 show in flowchart form the actions of the CE, IOCE, and SE during a system IPL. The upper portion of Figure 9-3 shows, in simplified form, the intercommunication between system elements during IPL and provides a summary of the more detailed portion of the flowchart. IPL can be initiated either from the System Console (SC) or a CE. The CE, SE, UNIT, and CHANNEL SELECT switches must be properly set up and the SYSTEM INTERLOCK switch on. The selected CE issues a system reset to all elements, turning on all SCON bits. It then takes the information from the SC or its own load unit select switches to configure a subsystem. The CE puts the selected SE number into its own ATR position 1 and physical PSBAR, issues a special IPL SCON (pseudo SCON) to each of the selected elements, issues a SATR to the selected IOCE (Figure 9-5), then raises 'IPL IOCE (X)' to the IOCE.

As shown in Figure 9-5, the IOCE reads 24 bytes into the PSA area in the selected SE starting at location zero as follows:

Location 0: IPL PSW 0 is read in. This is the first data which will be fetched by the CE. It includes the starting address of the program being read in by the IOCE.

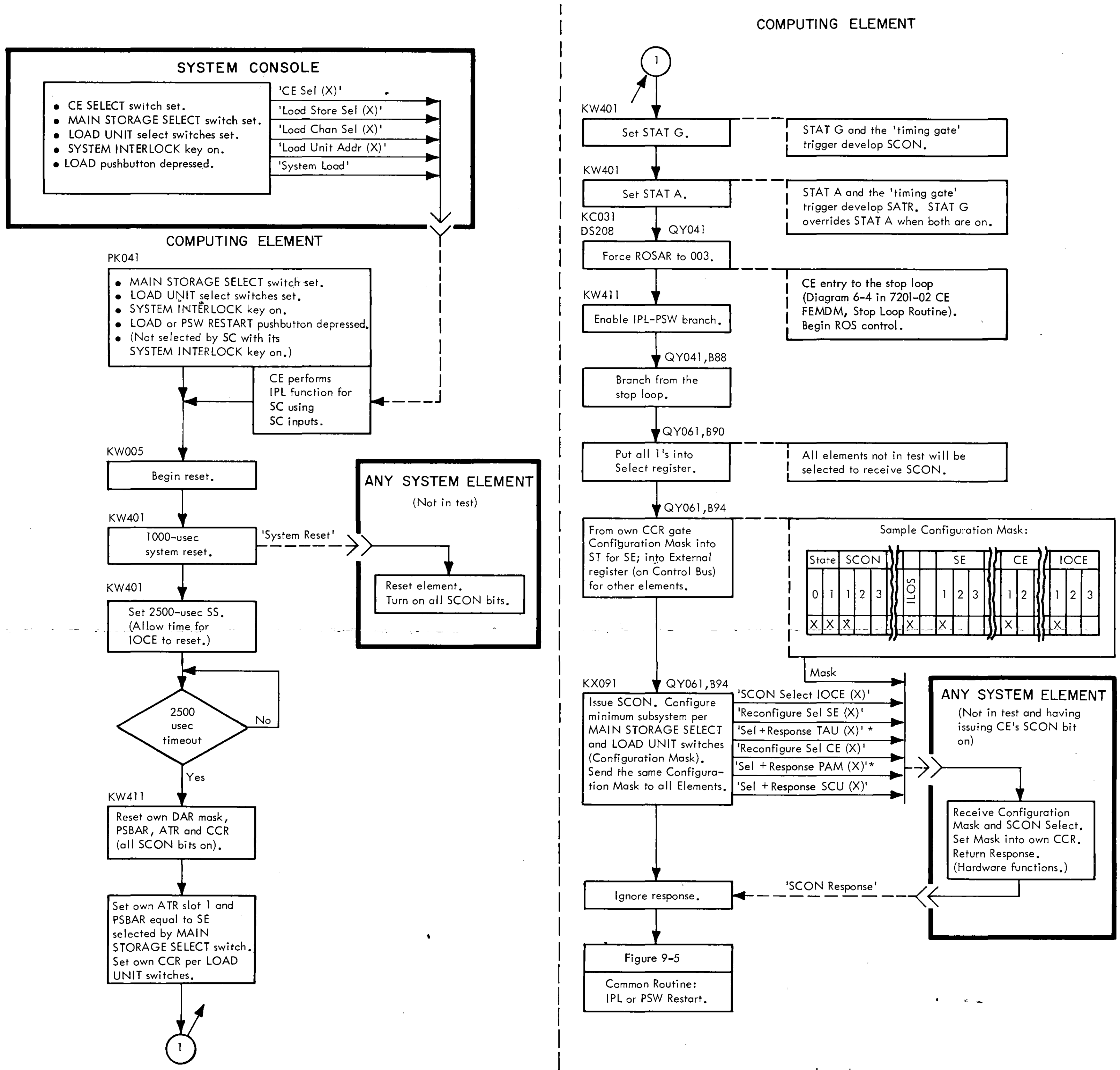


●Figure 9-2. IBM 9020D Subsystem Reset



Summary of System Operations: IPL or PSW Restart

Legend:
■ CE selected by SC if IPS is initiated at SC. CE at which IPL or PSW Restart is initiated.
▲ IOCE and TCU or SCU selected by SC or CE LOAD UNIT switches. SE selected by SC or CE MAIN STORAGE SELECT switch.
● Signal origin
○ Signal destination



Legend:
* True multiplex lines.

Figure 9-3. System Operation: IPL or PSW Restart

Location 8: CCW 1 is read in. This is the first CCW to be fetched by the IOCE. It specifies the number of bytes that the IOCE will read in and the location at which they will be placed. It may or may not specify chaining to CCW 2.

Location 10 (hex): IPL CCW 2 is read in. This CCW may be a transfer in channel (TIC) to another CCW or a data address and byte count with or without chaining specified.

Having read these three doublewords into the PSA, the IOCE fetches from location 8 and executes IPL CCW 1. Then a bootstrap-type operation may be performed in which IPL CCW 1 may first cause further CCWs to be read into storage from the input device and then chain to IPL CCW 2. CCW 2 would then specify a TIC to one of the CCWs just read in. The IOCE continues fetching and executing CCWs until one which specifies neither TIC nor chaining is fetched. It executes this CCW, then raises 'Response' to the CE. This releases the CE to fetch IPL PSW 0 and starts executing the program read in by the IOCE.

Figure 9-5 shows the detailed actions of the IOCE in any IPL operation including a normal IPL initiated by an IOCE in diagnose mode.

Subsystem IPL

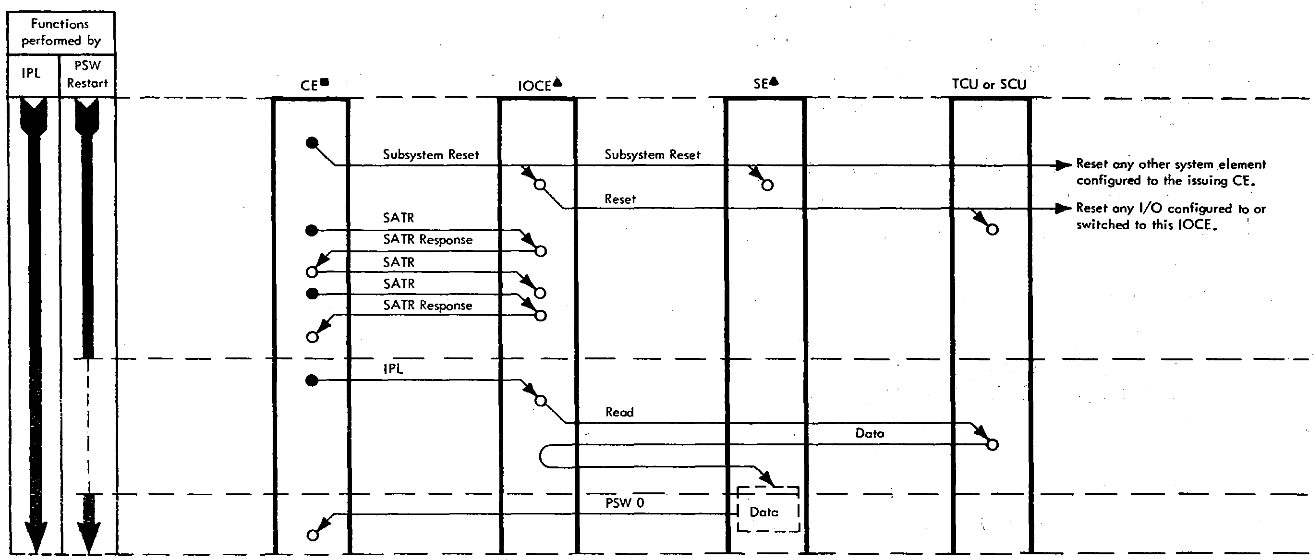
A subsystem IPL can be initiated from a CE, provided that the subsystem has been manually configured. The CE, SE, UNIT, and CHANNEL SELECT switches must be properly set up. The SYSTEM INTERLOCK key must be off. (Figures 9-4 and 9-5.) The CE issues a subsystem reset to the elements selected and issues a SATR and an IPL to the selected IOCE. All subsequent actions are the same as those described for a system IPL.

PSW RESTART

- Two types: system and subsystem.
- Initiated from CE.
- Preceded by reset.
- Loads a PSW from location zero of SE identified by the SE SELECT switch.

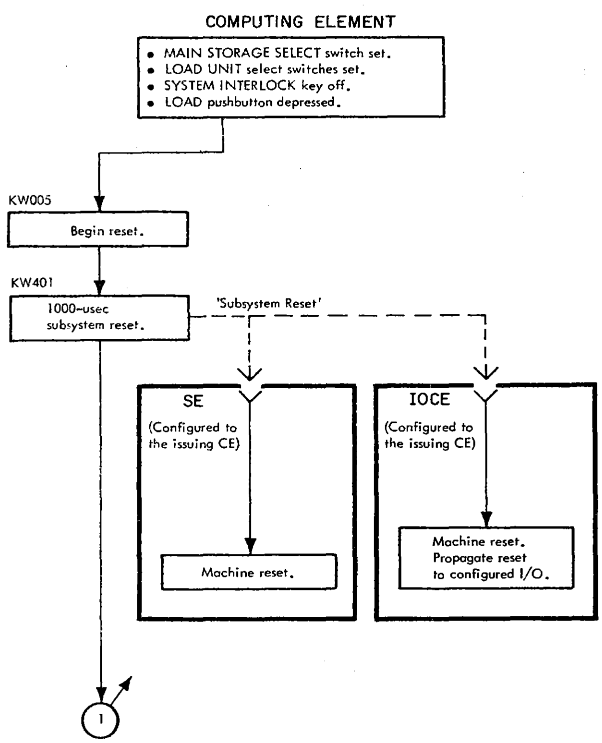
A PSW restart may be initiated at a CE. A system PSW restart occurs if the INTERLOCK key is turned on; a subsystem PSW restart occurs if the INTERLOCK key is turned off.

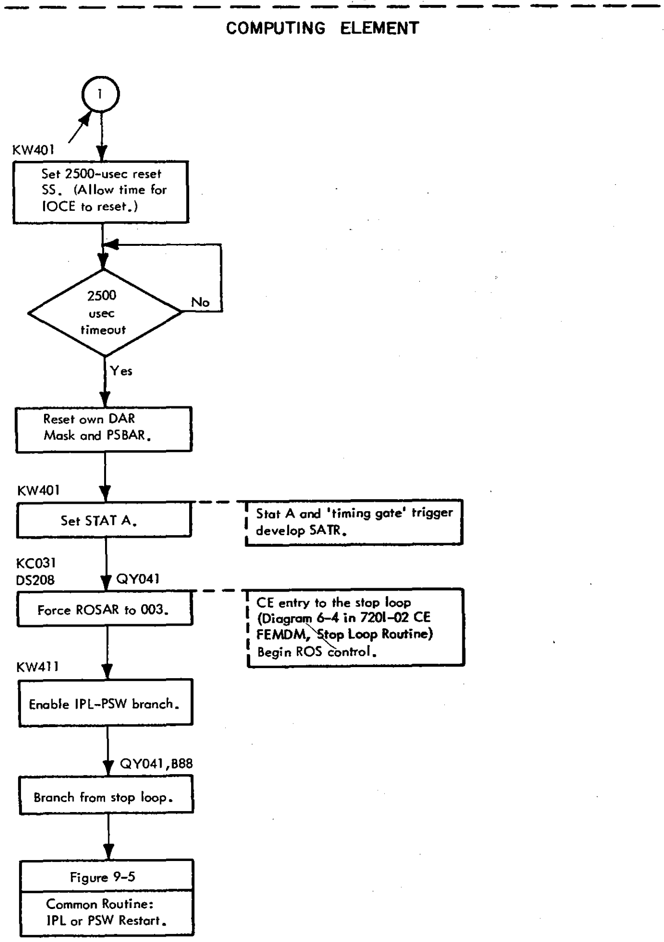
Figure 9-3 shows the system PSW restart action at the CE (as well as IPL which was described previously). The system PSW restart is the same as system IPL until the reset, SCON, and SATR routines are completed. At the completion of these routines, system PSW restart branches to the ROS routine to load a PSW from location zero of the SE identified by the SE SELECT switch. A subsystem PSW restart (Figure 9-4) performs neither SCON nor SATR. A subsystem reset occurs and the branch is taken to load a PSW.



Summary of Subsystem Operations: IPL or PSW Restart.

Legend:
■ CE at which IPL or PSW Restart is initiated.
▲ IOCE and TCU or SCU selected by CE LOAD UNIT switches and SE selected by CE MAIN STORAGE SELECT switch.
● Signal origin
○ Signal destination





• Figure 9-4. Subsystem Operation: IPL or PSW Restart

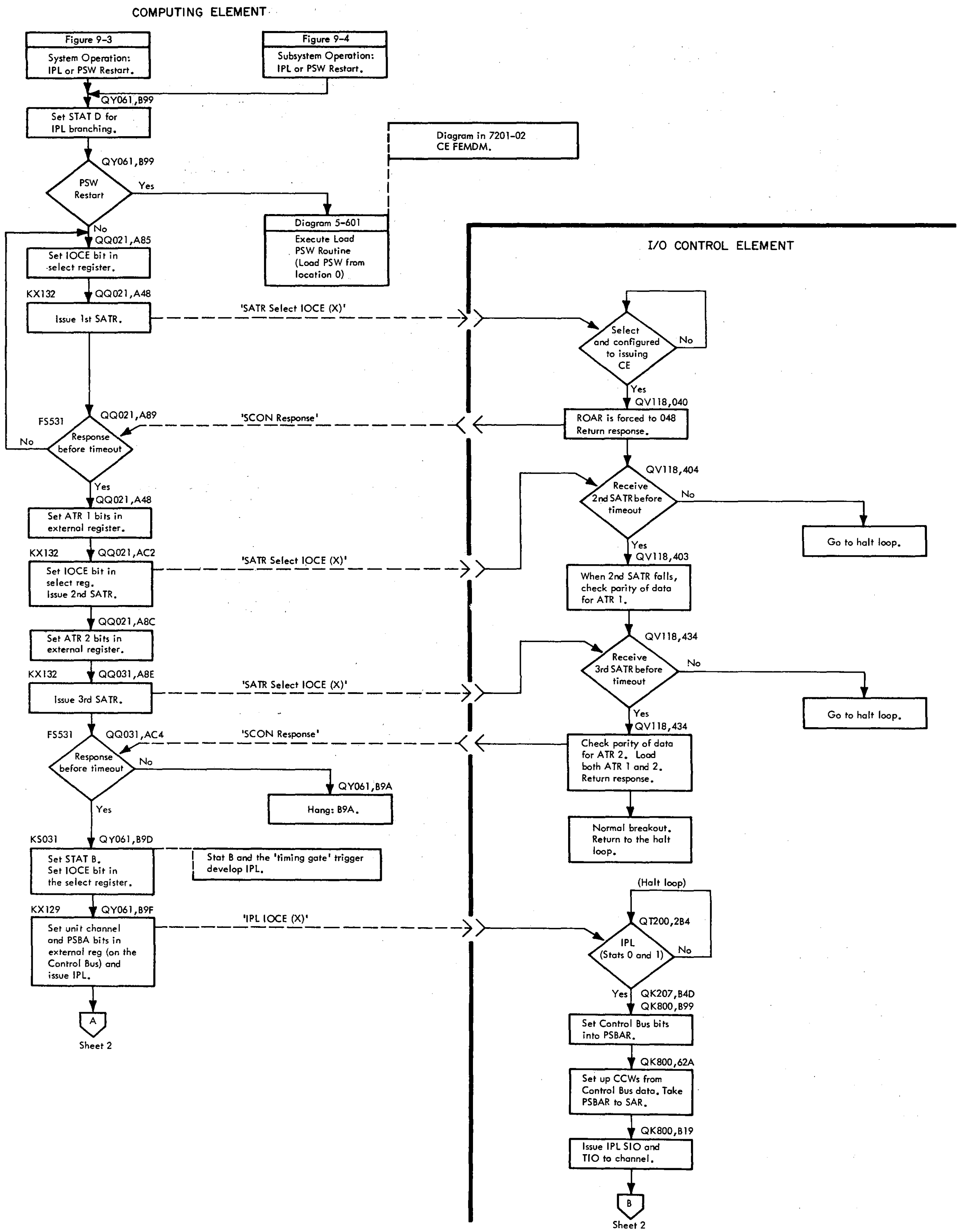
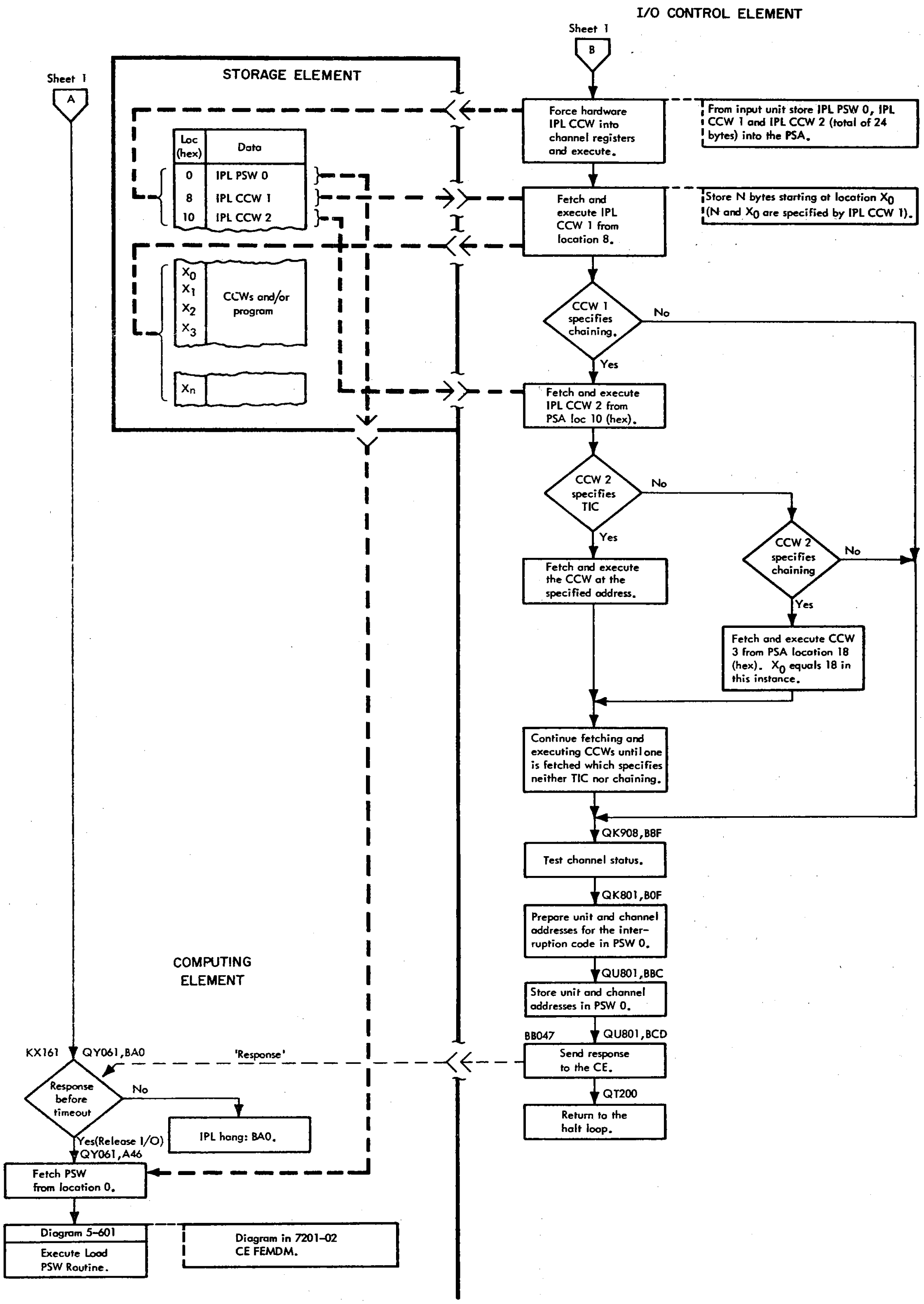


Figure 9-5. Common Routine: IPL or PSW Restart (Sheet 1 of 2)



Legend: Heavy dashed lines indicate data flow.

Figure 9-5. Common Routine: IPL or PSW Restart (Sheet 2 of 2)

The listings in the Type and Exceptions columns are defined as follows:

A	Addressing exception
C	Condition code is set
D	Data exception
DF	Decimal-overflow exception
DK	Decimal-divide exception
E	Exponent-overflow exception
EX	Execute exception
F	Floating-point feature
FK	Floating-point divide exception
IF	Fixed-point overflow exception
IK	Fixed-point divide exception
L	New condition code loaded
LS	Significance exception
M	Privileged-operation exception
P	Protection exception
S	Specification exception
T	Decimal feature
U	Exponent-underflow exception
Y	Direct control feature
Z	Protection feature

NOTE: Blank space indicates instruction not valid for unit indicated.

Name	Mnemonic	Format	Type	Exceptions	Code	360 Mode	CE	IOCE	IOCE-P
Add	AR	RR		C IF	1A	■	■	■	■
Add	A	RX		C A S IF	5A	■	■	■	■
Add Decimal	AP	SS	T	C P A D DF	FA	■	■		
Add Halfword	AH	RX		C A S IF	4A	■	■	■	■
Add Logical	ALR	RR		C	1E	■	■	■	■
Add Logical	AL	RX		C A S	5E	■	■	■	■
Add Normalized (Long)	ADR	RR	F	C S U E LS	2A	■	■		
Add Normalized (Long)	AD	RX	F	C A S U E LS	6A	■	■		
Add Normalized (Short)	AER	RR	F	C S U E LS	3A	■	■		
Add Normalized (Short)	AE	RX	F	C A S U E LS	7A	■	■		
Add Unnormalized (Long)	AWR	RR	F	C S E LS	2E	■	■		
Add Unnormalized (Long)	AW	RX	F	C A S E LS	6E	■	■		
Add Unnormalized (Short)	AUR	RR	F	C S E LS	3E	■	■		
Add Unnormalized (Short)	AU	RX	F	C A S E LS	7E	■	■		
AND	NR	RR		C	14	■	■	■	■
AND	N	RX		C A S	54	■	■	■	■
AND	NI	SI		C P A	94	■	■	■	■
AND	NC	SS		C P A	D4	■	■	■	■
Branch and Link	BALR	RR			05	■	■	■	■
Branch and Link	BAL	RX			45	■	■	■	■
Branch on Condition	BCR	RR			07	■	■	■	■
Branch on Condition	BC	RX			47	■	■	■	■

Name	Mnemonic	Format	Type	Exceptions	Code	360 Mode	CE	IOCE	IOCE-P
Branch on Count	BCTR	RR			06				
Branch on Count	BCT	RX			46				
Branch on Index High	BXH	RS			86				
Branch on Index Low or Equal	BXLE	RS			87				
Compare	CR	RR		C	19				
Compare	C	RX		C A S	59				
Compare Decimal	CP	SS	T	C A D	F9				
Compare Halfword	CH	RX		C A S	49				
Compare Logical	CLR	RR		C	15				
Compare Logical	CL	RX		C A S	55				
Compare Logical	CLI	SI		C A	95				
Compare Logical	CLC	SS		C A	D5				
Compare (Long)	CDR	RR	F	C S	29				
Compare (Long)	CD	RX	F	C A S	69				
Compare (Short)	CER	RR	F	C S	39				
Compare (Short)	CE	RX	F	C A S	79				
Convert and Sort Symbols	CSS	RR		P A S	02				
Convert to Binary	CVB	RX		A S D IK	4F				
Convert to Decimal	CVD	RX		P A S	4E				
Convert Weather Lines	CVWL	RR		P A S	03				
Delay	DLY	RR			0B				
Diagnose		SI		M A S	83				
Divide	DR	RR		S IK	1D				
Divide	D	RX		A S IK	5D				
Divide Decimal	DP	SS	T	P A S D DK	FD				
Divide (Long)	DDR	RR	F	S U E FK	2D				
Divide (Long)	DD	RX	F	A S U E FK	6D				
Divide (Short)	DER	RR	F	S U E FK	3D				
Divide (Short)	DE	RX	F	A S U E FK	7D				
Edit	ED	SS	T	C P A D	DE				
Edit and Mark	EDMK	SS	T	C P A D	DF				
Exclusive OR	XR	RR		C	17				
Exclusive OR	X	RX		C A S	57				
Exclusive OR	XI	SI		C P A	97				
Exclusive OR	XC	SS		C P A	D7				
Execute	EX	RX		A S EX	44				
Halt I/O	HIO	SI		C M	9E				
Halve (Long)	HDR	RR	F	S	24				
Halve (Short)	HER	RR	F	S	34				
Insert Adr Tsltr	IATR	RR			0E				
Insert Character	IC	RX		A	43				
Insert Storage Key	ISK	RR	Z	M A S	09				
Load	LR	RR			18				
Load	L	RX		A S	58				
Load Address	LA	RX			41				
Load and Test	LTR	RR		C	12				
Load and Test (Long)	LTDR	RR	F	C S	22				
Load and Test (Short)	LTER	RR	F	C S	32				
Load Chain	LC	RX		P A S	52				
Load Complement	LCR	RR		C IF	13				
Load Complement (Long)	LCDR	RR	F	C S	23				
Load Complement (Short)	LCER	RR	F	C S	33				

Name	Mnemonic	Format	Type	Exceptions	Code	360 Mode	CE	IOCE	IOCE-P
Load Data Address	LDA	RS			99				
Load Halfword	LH	RX		A S	48				
Load Identity	LI	RR			0C				
Load (Long)	LDR	RR	F	S	28				
Load (Long)	LD	RX	F	A S	68				
Load Multiple	LM	RS		A S	98				
Load Negative	LNR	RR		C	11				
Load Negative (Long)	LNDR	RR	F	C S	21				
Load Negative (Short)	LNER	RR	F	C S	31				
Load Positive	LPR	RR		C IF	10				
Load Positive (Long)	LPDR	RR	F	C S	20				
Load Positive (Short)	LPER	RR	F	C S	30				
Load PSBA	LPSB	SI		M P A S	A1				
Load PSW	LPSW	SI		L M A S	82				
Load (Short)	LER	RR	F	S	38				
Load (Short)	LE	RX	F	A S	78				
Move	MVI	SI		P A	92				
Move	MVC	SS		P A	D2				
Move Numerics	MVN	SS		P A	D1				
Move with Offset	MVO	SS		P A	F1				
Move Word	MVW	SS		P A S	D8				
Move Zones	MVZ	SS		P A	D3				
Multiply	MR	RR		S	1C				
Multiply	M	RX		A S	5C				
Multiply Decimal	MP	SS	T	P A S D	FC				
Multiply Halfword	MH	RX		A S	4C				
Multiply (Long)	MDR	RR	F	S U E	2C				
Multiply (Long)	MD	RX	F	A S U E	6C				
Multiply (Short)	MER	RR	F	S U E	3C				
Multiply (Short)	ME	RX	F	A S U E	7C				
OR	OR	RR		C	16				
OR	O	RX		C A S	56				
OR	OI	SI		C P A	96				
OR	OC	SS		C P A	D6				
Pack	PACK	SS		P A	F2				
Read Direct	RDD	SI	Y	M P A	85				
Repack Symbols	RPSB	RR		P A S	0F				
Set Adr Tsltr	SATR	RR		C M S	0D				
Set Configuration	SCON	RR		C M S	01				
Set PCI	SPCI	SI		C M	9B				
Set Program Mask	SPM	RR		L	04				
Set Storage Key	SSK	RR	Z	M A S	08				
Set System Mask	SSM	SI		M A	80				
Shift Left Double	SLDA	RS		C S IF	8F				
Shift Left Double Logical	SLDL	RS		S	8D				
Shift Left Single	SLA	RS		C IF	8B				
Shift Left Single Logical	SLL	RS			89				
Shift Right Double	SRDA	RS		C S	8E				
Shift Right Double Logical	SRDL	RS		S	8C				
Shift Right Single	SRA	RS		C	8A				
Shift Right Single Logical	SRL	RS			88				
Start I/O	SIO	SI		C M	9C				

Name	Mnemonic	Format	Type	Exceptions	Code	360 Mode	CE	IOCE	IOCE-P
Start I/O Processor	SIOP	SI		M S	9A				
Store	ST	RX		P A S	50				
Store Character	STC	RX		P A	42				
Store Halfword	STH	RX		P A S	40				
Store (Long)	STD	RX	F	P A S	60				
Store Multiple	STM	RS		P A S	90				
Store PSBA	SPSB	SI		M P A S	A0				
Store (Short)	STE	RX	F	P A S	70				
Subtract	SR	RR		C IF	1B				
Subtract	S	RX		C A S IF	5B				
Subtract Decimal	SP	SS	T	C P A D DF	FB				
Subtract Halfword	SH	RX		C A S IF	4B				
Subtract Logical	SLR	RR		C	1F				
Subtract Logical	SL	RX		C A S	5F				
Subtract Normalized (Long)	SDR	RR	F	C S U E LS	2B				
Subtract Normalized (Long)	SD	RX	F	C A S U E LS	6B				
Subtract Normalized (Short)	SER	RR	F	C S U E LS	3B				
Subtract Normalized (Short)	SE	RX	F	C A S U E LS	7B				
Subtract Unnormalized (Long)	SWR	RR	F	C S E LS	2F				
Subtract Unnormalized (Long)	SW	RX	F	C A S E LS	6F				
Subtract Unnormalized (Short)	SUR	RR	F	C S E LS	3F				
Subtract Unnormalized (Short)	SU	RX	F	C A S E LS	7F				
Supervisor Call	SVC	RR			0A				
Test and Set	TS	SI		C M P A S	93				
Test Channel	TCH	SI		C M	9F				
Test I/O	TIO	SI		C M	9D				
Test Under Mask	TM	SI		C A	91				
Translate	TR	SS		P A	DC				
Translate and Test	TRT	SS		C A	DD				
Unpack	UNPK	SS		P A	F3				
Write Direct	WRD	SI	Y	M A	84				
Zero and Add	ZAP	SS	T	C P A D DF	F8				

System/360 programs may be run on a simplex subsystem of the 9020D by using the 360 mode capability. Placing the subsystem in 360 mode inhibits certain 9020 actions which are not compatible with IBM System/360 architecture (as defined in IBM System/360 Principles of Operation). This appendix indicates the effects of 360 mode operation upon the 9020 hardware. For details regarding the effects on program operation, refer to Appendix G of the IBM 9020D/E Principles of Operation.

OPERATIONAL CHARACTERISTICS

The simplex subsystem must use IOCE 1 because the I/O channel addresses available on IOCE 1 correspond to IBM System/360 architecture. Other elements used in the subsystem include: any one CE, any SEs, the SC, I/O attached to the SC, and tapes and disks attached to IOCE 1.

The subsystem must be properly configured before being placed in 360 mode. It is placed in 360 mode by depressing the 360 MODE pushbutton on the CE control panel. The pushbutton is backlighted when 360 mode is active.

The subsystem may be taken out of 360 mode by again depressing the 360 MODE pushbutton. The following actions also reset 360 mode:

1. Power on reset in the CE.
2. External start to the CE.
3. State two or state three.

Note: System IPL and System PSW Restart reset 360 mode because they force state three.

HARDWARE DIFFERENCES

1. The subsystem operates as if ILOS [CCR(6) in CE and IOCE] were set to 1. That is:
   a. PSBAR stepping is inhibited.
   b. Logout Stop (LOS) cannot be sent to an SE.
2. PSBAR is set as follows:
   a. Logical PSBAR is reset to zeros.
   b. Physical PSBAR is set to the value in ATR 1 slot 1.
3. PSA Lockout and SE Stopped result in a checkstop condition; no interruption is caused.
4. Certain 9020 mode op codes become invalid. See Figure B-1 for a list of these op codes.
5. Bits 16–19 of the PSW are interpreted as part of the interruption code rather than as an extention of the system mask.

Operation Code	Name	Mnemonic
01	SET CONFIGURATION	SCON
02	CONVERT and SORT SYMBOLS	CSS
03	CONVERT WEATHER LINES	CVWL
0B	DELAY	DLY
0C	LOAD IDENTITY	LI
0D	SET ADDRESS TRANSLATOR	SATR
0E	INSERT ADDRESS TRANSLATOR	IATR
0F	REPACK SYMBOLS	RPSB
52	LOAD CHAIN	LC
9A	START I/O PROCESSOR	SIOP
9B	SET PCI	SPCI
A0	STORE PS BASE ADDRESS	SPSB
A1	LOAD PS BASE ADDRESS	LPSB
D8	MOVE WORD	MVW

Figure B-1. Op Codes Not Executable in 360 Mode

Note: This affects three status switching instructions: LPSW, SSM, and SVC.

6. Multiplex channel 0 and selector channels 1, 2, and 3 become the only operational channels. IOCE 2 channels become "not operational" and IOCE 3 channels become "invalid".
7. Storage protection operates differently. In 9020 mode, a protection key or a storage key equal to zero is equivalent to a key match; in 360 mode only, the protection key equal to zero is equivalent to a key match.
8. IOCE processor is hardware-stopped in IOCE 1 when it is part of a 360 mode subsystem.
9. System IPL and System PSW Restart cannot be used because it forces state three which resets 360 mode.

Note: The Direct Control feature of the 9020 has expanded capabilities not normally present in System/360 architecture. These additional capabilities are not disabled in 360 mode, however; Direct Control operates the same way in both 9020 and 360 modes.

ABO. Address bus out

ACTIVATE. A pushbutton which causes an operation to be initiated (such as the changing of a configuration control register SCON bits).

Adapter. The distinguishable hardware that provides the controls and signals to control a specific input/output device.

Address Keys. Keys that enable the addressing, by byte or word, of any addressable location in main or local storage. These keys also serve as a final loop address.

ALD. Automated Logic Diagram

AR. Address Register

Backup. An alternative or fall-back position, used mainly in conjunction with the power system.

Battery Power. A temporary backup power system for CEs, IOCEs, DEs and SEs, automatically available when main line power fails.

BSM. Basic Storage Module

BP. Buffer Processor adapter

Burst Mode. The mode of operation in which all channel facilities are monopolized during data transfer to or from a particular I/O device.

Bus. A set of common lines over which data and/or controls can be transmitted.

Busy. A device status (condition code 2); indicates that device is active.

Byte. A group of eight bits.

CAW. Channel Address Word

CB. Circuit Breaker

CC. Configuration Console/Condition Code

CCC. Central Computer Complex portion of NAS

CCR. Configuration Control Register

CCW. Channel Control Word

CD. Common Digitizer adapter

CE. Computing Element

CE Battery Frame. Part of the main wall section between two SEs or DEs. Provides battery packs and associated CE hardware (contained on the wall). Interframe cabling is routed through this frame.

CE CHECK CONTROL Switch. A switch used for maintenance purpose; it has three positions: STOP, DISABLE, and PROCESS. When a CE check occurs, the setting of this switch controls the subsequent activity. PROCESS is the normal position.

Channel. (Associated with an IOCE) the avenue through which data flows, to or from the system.

Channel Address Word. A word in preferential storage address 72 which contains the storage protection key and storage location of the channel command word.

Channel Command Word. A word in storage that specifies to the channel the I/O command to be executed.

Channel Status Word. A word in preferential storage address 64 which provides the status of an I/O device or the conditions under which the I/O operation has been terminated.

Character. A group of bits that varies in length between four and eight bits, depending on source and use.

Character Vector Generator. An adapter (Government Furnished Equipment), which interfaces the PVD and is contained in the DG.

C/I. Converter/Inverter

CLU. Common Logic Unit (a major portion of IOCE).

CM. Configuration Mask

Command. The first byte of the CCW; decoded by channel and I/O unit to specify I/O operation to be executed.

Common Logic Unit. The registers, latches, storage, and controls that make up the heart of each IOCE.

Computing Element. The processor of the 9020 system, which maintains system control and performs arithmetic and logic operations.

Configuration Console. A unit in the 9020E which provides a central monitoring and control position for the system. Reconfiguration and error reporting paths for the IBM DAUs, DGs and RKMs are provided by duplexed reconfiguration control units contained in the CC. The CC also interfaces the SMMC for error reporting.

Configuration Control. A hardware- and program-controlled system which defines system and subsystem communication paths and protects the operational system from malfunctioning system components assigned to a maintenance subsystem.

Configuration Control Register. A register in each system element and control unit, except the 2821 SC and 2701 DAU, which controls communication between system components.

Configuration Mask. The data used by the configuration control registers.

Console. An aggregation of indicators and controls.

Control Panel. Used interchangeably with console. (See Console.)

CSW. Channel Status Word

CTC. Channel-to-channel adapter

CVG. Character Vector Generator

DAR. Diagnose Accessible Register

DARM. Diagnose Accessible Register Mask

DASF. Direct Access Storage Facility.

Data Keys. These keys operate in conjunction with other keys and are used to provide data for subsequent storage or as a beginning address of a loop operation.

Data Interleave Mode. A byte mode of input/output operation, which is now referred to as Multiplex mode.

DAU. Data Adapter Unit (2701)

DBI. Data Bus In

DBO. Data Bus Out

DCP. Display Channel Processor portion of NAS

DE. Display Element

DESAR. Display Element Storage Address Register

DESDR. Display Element Storage Data Register

Destination. An addressed device or storage location.

Device. A system component, usually an input/output device; includes tape units.

DG. Display Generator

DGAR. Display Generator Address Register (in the display element)

DGDR. Display Generator Data Register (in the display element)

Diagnose. An instruction used primarily by maintenance programs to perform functions using parts of elements not possible with any other computer instruction.

Display Generator. A non-IBM unit used to drive displays.

Diagnose Accessible Register. A register in the CE used in conjunction with the External Old PSW to indicate source of some external interruptions; can be read only with the Diagnose instruction.

Diagnostic Monitor. A supervisor program which controls the operation of diagnostic programs.

Diagnostic Program. A program written to determine the malfunctioning parts of a system component.

Digit. A group of four bits; usually two digits to a byte.

Direct Access Storage Facility. A disk storage facility consisting of a 2314-A1 SCU and one or more 2312-A1/2318-A1 DSUs.

Disk Storage Unit. Either a 2312-A1 or 2318-A1 disk drive. The former contains one disk drive; the latter contains two. Both attach to a 2314-A1 SCU.

Display Element. An element that interfaces the CE for display update and DGs for display regeneration.

DRG. Data Receiving Group

DSU. Disk Storage Unit (2312-A1 or 2318-A1).

Duplex System. Configuration containing two CEs.

ELC. Element Check

Element. Major system component, which also contains battery backup: CEs, IOCEs, DEs, and SEs.

Element Check. An equipment malfunction detected by an element or unit and indicated to a CE; detectable through the external interrupt system.

Element Control Panel. Controls and indicators located on a panel at each element and unit frame.

ELEMENT MPO PULL. Element Master Power Off

Element Master Power Off Pull. A pull-type switch, which turns power off on each of the system elements and each PAM and TCU where it is located; operative in any state.

Element Numbering. Numbering scheme used to define physical location and order of expansion for main wall elements.

Element Reset. Reset of an element's or unit's registers and controls to an initial state.

EMERGENCY PULL. A pull switch located in the upper right-hand corner of the system console and configuration console; to be used in an emergency and to turn off power to all system components.

ENABLE. A pushbutton which allows an affiliated switch action to take place.

EOD. End of Display

EOM. End of Message

EPO. Emergency Power Off

External Cables. Protected covered cables used to interconnect normally separated elements, units, or devices. External cables are routed under the floor.

External Interrupt Register. External interruptions are stored either in the PSW, DAR, or in the PIR; all may be considered external interruption registers.

Fault Locating Tests. A fixed set of diagnostic or status tests used for isolation of equipment malfunctions in the CEs and IOCEs.

Fetch. The action whereby data is retrieved from storage.

FLT. Fault Locating Tests

Frame. The mechanical housing for the electronic, mechanical, and power equipment which constitutes each system element, unit, and device.

GPI. General Purpose Input adapter

GPO. General Purpose Output adapter

High-Order Bits. Most significant bits of word, byte, or group of bits.

IA. Instruction Address

IAR. Instruction Address Register

IC. Instruction Counter

IDES. Inhibit DE Stop bit. (Absence of this bit will cause DE to stop on any DE error.)

ILC. Instruction Length Code

ILOS. Inhibit Logout Stop

Indicator. A visual indicator on a panel or console; also referred to as lamp or neon.

Input/Output Control Element. The system component that provides the control for all system input/output operations and does processing under control of the CE.

Instruction. An instruction is fetched from storage by a CE or IOCE and is executed by that CE or IOCE to perform a useful function.

Interface. The matching of signal, data, and control lines between system components.

Interlock. A hardware control which requires another action to be performed to make certain manual controls effective.

Interruption. The stopping of processing in a CE or IOCE. (See 9020 System Principles of Operation Manual and 9020D and 9020E System.)

INTI. Interfacility Input adapter

INTO. Interfacility Output adapter

IOCE. Input/Output Control Element

IOCESAB. IOCE Storage Address Bus (in the SE).

IOCESBO. IOCE Storage Bus Out (in the SE).

IOCE Processor. An IOCE that is processing instructions under control of a CE.

IPL. Initial Program Load

ISK. Insert Storage Key

K. Contactor

Keys. Hardware toggle switches, or storage protect codes.

Lamp. Used interchangeably with indicator. (See Indicator.)

Lamp Test. A static test of indicators on a console, with exceptions noted for each panel.

LAR. Local Store Address Register

Latch. A hardware device capable of retaining a bit of information.

LOAD. A pushbutton located on some system elements and on the system console and the configuration console to start the initial program loading sequence.

LOAD UNIT. Rotary switches on some system elements and the system console; used to select an input/output device for the initial program loading process.

Local Storage. A group of internal registers within a CE or IOCE; used for instruction execution purposes.

Logic. The circuits provided in an element which make decisions concerning the data provided them.

Logic Check. The determination that the logic is not performing in a correct manner; usually associated with incorrect parity of data.

Logout. The storing of contents of registers and conditions of latches from an element into selected locations of main storage.

Logwords. Words contained in a logout (32 bits).

Low-Order Bits. Least significant bits of word, byte, or group of bits.

LRC. Longitudinal Redundancy Check

LS. Local Storage

LSAR. Local Storage Address Register (IOCE).

LSB. Least Significant Bit

LSFR. Local Storage Function Register

LSWR. Local Storage Working Register

LW. Logword

MACH. Maintenance and Channel Storage

Machine Cycle. The time required to perform one micro-instruction.

MAIN STORAGE SELECT. A rotary switch on the system console, configuration console, and CE; used to select a main (not a local) storage element for initial program loading, FLT loading, and store/display operations.

Main Wall Section. Joins CE and SE/DE elements into a contiguous wall. Contains interframe cabling and power components.

Main Wall Spacer Frame. Used between two SEs or DEs when not separated by a CE. Interframe cabling is routed through this frame.

Maintenance and Channel Storage. Storage in the IOCE used for Channel UCWs, IOCE processor, and maintenance operations.

Maintenance Controls. Controls located on all system components for use by engineers responsible for maintaining individual or subsystem components.

Marginal Condition. A marginal condition may be caused by an out-of-tolerance check or on-battery signal.

MC. Machine Checks or Marginal Check

MCW. Maintenance Control Word

Micro-instruction or Micro-order. The commands stored in read-only storage which control CE and IOCE actions.

Mode of Operation. Indicators which display in alphameric characters the operational system status on the system console.

Module. A circuit package; part of the SLT technology.

Monitor. The act of watching the display of information through indicators and the manipulation of operational controls.

MPLX. Multiplexer

MPDA. Modified Parallel Data Adapter

MPO. Master Power Off. (See Element Master Power Off.)

MSB. Most Significant Bit

MTU. Magnetic Tape Unit 2401-2/3

Multiplex Mode. The normal mode of operation for slow-speed devices; allows handling of single bytes or multiple bytes whenever necessary.

Multiplexer Channel. A channel in the IOCE which operates in the Multiplex mode.

NAS. National Airspace System

NBP. Normal Bit Period

OBS. On-Battery Signal

On-Battery Signal. An indication from an element that it has lost main line or standby power and is obtaining power from its battery system.

Operator Controls. Controls on the system console, configuration console, and CEs which an operator may use to affect a CE and the system operation.

Order. Used to specify functions peculiar to a device, such as rewinding tape or spacing of a printer.

OTC. Out-of-Tolerance Check

Out-of-Tolerance Check. An indication by temperature-sensing circuits that there has been an increase in internal temperature within approximately 10° of the thermal shut-down temperature.

PAM. Peripheral Adapter Module

Panel. An aggregation of indicators and controls; used interchangeably with console.

PCI. Program Controlled Interruption.

PDA. Parallel Data Adapter (in the 2701 DAU).

PDU. Power Distribution Unit

Peripheral Adapter Module. A unit in the 9020 System for interfacing with various input/output devices. PAM provides the control for automatic sequential polling and servicing for input/output devices.

PIR. Processor Interrupt Register

PN. Part number

Power Check. A power supply malfunction which results in an indicator display on the system component where the fault is located and on the system console under the appropriate component indication.

Power Controls. Controls that allow the various power functions to be performed.

Power Control Panel. A panel located on most system components which contains each component's power control switches and indicators.

Power Distribution Unit. Referred to as a power compartment; located within each system element and unit and some devices; contains the power supplies and power distribution equipment.

POWER ON/OFF. A toggle type switch which is used, except when interlocked, to turn power on or off on a system component.

POWER ON/OFF REMOTE Switch. A power on/off switch located in the power distribution unit. It can be used in place of the POWER ON/OFF switch.

Power Sequence Complete. When a system component has successfully sequenced all its voltages to the operational level, the POWER SEQUENCE COMPLETE indicator is turned on.

Power Wall Frame. Contains power circuitry for a related element. Interframe cabling is routed through this frame. This frame is part of main wall section.

Preferential Storage Base Address. Address in storage which contains the first byte of the preferential storage area.

Preferential Storage Address Register. A hardware register in the CE which contains the PSBA.

Primary Interface. The path established between a like-numbered PAM and IOCE and through which the maximum number of devices attached to the PAM may be addressed.

Processor Interrupt Register. A three-bit register in each CE to preserve external interrupts from IOCE processors.

Program Status Word. Contains information that is required for proper program execution.

PSA. Preferential Storage Area

PSBA. Preferential Storage Base Address

PSBAR. Preferential Storage Base Address Register

PSW. Program Status Word

PVD. Plan View Display

QUAD System. Configuration with four CEs.

RATE. A switch which allows a CE or IOCE to process instructions at normal processing speed or an instruction at a time.

R/Console. The enroute controller's console.

RCU. Reconfiguration Control Unit (portion of the CC).

Read Only Storage. A capacitor-type storage which is utilized in the CE and IOCE to hold the micro-instructions necessary to control the element's operations.

Refetch. When a piece of data is fetched and an error indication is noted by the checking circuits, another fetch, a refetch, can occur.

RKM. Radar Keyboard Multiplexer

RKM/R-Console. RKM-to-R-console configuration switch

ROAR. Read-Only Address Register

ROS. Read-Only Storage

ROS Address Stop. Causes the CE or IOCE to stop when the specified micro-instruction address is selected.

ROSDR. Read-Only Storage Data Register

ROS Repeat. A repeat of a selected micro-instruction.

Running State. The normal machine state for processing instructions, referred to as the processing state and/or the program or supervisor state.

RVDP. Radar Video Data Processor adapter

SAB. Storage Address Bus

SABR. Storage Address Buffer Register

SAP. Storage Address Protect

SAR. Storage Address Register

SBI. Storage Bus In

SBO. Storage Bus Out

SC. System Console

SCI. Storage Control Interface

Scan In. The filling of registers and triggers in an element with the selected contents of storage (via special paths).

SCON. Set Configuration Instruction and Set Configuration function

SCU. Storage Control Unit (2314-A1).

SDBI. Storage Data Bus In

SDBO. Storage Data Bus Out

SDC. Station Directing Code

SDR. Storage Data Register

SE. Storage Element

Secondary Interface. The alternate path for a PAM-IOCE interface through which an IOCE may address only part (half-secondary) or all (full-secondary) of the PAM's attached devices.

Selection Mask. The data used by the configuration control equipment to address the configuration control registers that are to be changed.

Selective Reset. A reset signal sent to a selected adapter from an IOCE as a result of an error detected on the I/O interface.

Selector Channel. A high-speed channel which operates only in the burst mode.

SENSE Switch. A switch (one of a set) located on the system console and configuration console; can be used as a single or combination bit input.

SESAR. Storage Element Storage Address Register.

SESDR. Storage Element Storage Data Register

Set Configuration. An instruction which assigns communication paths between elements and units.

SLT. Solid Logic Technology

SM. System Mask

SMMC. System Maintenance Monitor Console

SOBR. Storage Output Buffer Register

SOD. Start of Display

SOM. Start of Message

SP. Storage Protect

SPAR. Storage Protect Address Register

SPB. Storage Protect Buffer

SPCA. System Power Control Assembly

SPCR. Storage Protect Compare Register

SPDR. Storage Protect Data Register

SPIKR. Storage Protect In Key Register

SPOKR. Storage Protect Out Key Register

SR. Select Register

SSK. Set Storage Key

SSU. Storage Switching Unit

Standby Power. A standby power system for main line power supplied by the customer.

STAT. A status trigger that is hardware-testable.

START. In conjunction with the RATE switch, this pushbutton takes a CE or IOCE out of the stopped state.

State. Used to define the state of a CE (stopped or wait) or the state or status of the operational system.

State One. An interpretation of the state bits in the configuration control register; a state in which SCON may not be issued by a CE; some maintenance controls are operative.

State Three. An interpretation of the state bits in the configuration control register: A state in which SCON may be issued by a CE; no manual controls normally operative in this state.

State Two. An interpretation of the state bits in the configuration control register; a state in which SCON may not be issued by a CE; no manual controls normally operative in this state.

State Zero. An interpretation of the state bits in the configuration control register; a state in which the TEST switch is operative and, therefore, all manual controls may be used.

Status. The various states of all system components automatically displayed on the system console and configuration console.

Status Byte. A portion of the information supplied by a channel or I/O unit as a result of an I/O operation.

Stop. The placing of a CE or IOCE in the stopped state without destroying control or register data.

Stopped State. A machine condition where no instructions are executed, no interrupts are accepted, and the timer is not updated. Certain manual controls are operative only in this machine state.

Storage. Either main or local storage registers which are used for storing data or programs. Read-only-storage holds micro-instructions only.

Storage Control Unit. A 2314-A1 which is the control unit for one or more 2312-A1/2318-A1 Disk Storage Units (DSUs).

Storage Cycle. The time required to read a word from, and regenerate the word into, main or local storage; also, the time to read a word from ROS.

Storage Element. The main storage element of the 9020D/E System, which contains 131K words of addressable storage.

Storage Key. Four bits placed in the storage protect buffer which are specified by the program and which protect a block of 2048 bytes.

Storage Protection. The protection of selected parts of an SE, accomplished through programming and hardware means, to prevent destruction of important data.

Storage Protect Buffer. A 64-word storage used to hold the storage protect keys.

Storage Protect Key. Used interchangeably with storage key.

STORAGE SELECT. The two-position switch that allows the addressing of main or local storage.

STORAGE TEST. A switch on IOCEs which allows hardware testing of the element's internal storage.

Store. To replace the contents of an addressable storage location.

SU. Switch Unit

Switchable Indicators. Indicators on the CE and IOCE control panels which can be manually switched to one of several different positions in which different registers or functions are displayed.

System Components. Elements - CEs, IOCEs, DEs, and SEs; Units - PAMs, Tape Control Units, 2821 Control Unit, 2701 Data Adapter Unit, System Console, Configuration Console; Devices - Tape Units, 1052s, Printer, Card Reader Punch, and other I/O devices.

System Console. The main system monitor and control location.

System Control. The function of controlling system components through programming and manual operations, using configuration control, element checking, and the executive control program.

System Interlock. A key-operated switch which, when in the normally "off" position, prevents certain manual controls from being operative (which might jeopardize system operation).

System Reset. A signal which resets system components to their initial state.

Tag. An identifying number assigned to each element.

TAS. Test And Set

TCU. Tape Control Unit

Tape Control Unit. The system unit which controls the operation of up to eight tape units. Each tape control unit may be selected through one of two IOCEs only.

TB. Terminal Board

Thermal Condition. Over-temperature condition for a system element or unit.

TPS. Two-Processor Switch

Triplex System. Configuration containing three CEs.

TU. Tape Unit

UCW. Unit Control Word

Unit. System components which operate mainly as I/O device control units; PAMs, DAUs, Tape Control Units, 2821 (Printer, Card Reader/Punch) Control Unit. Also, the system console and configuration console are classified as units.

Unit Control Word. An aggregation of information about a device and control unit; maintained and used by the multiplexer channel in an IOCE; not available to the programmer.

VFL. Variable Field Length

Wait State. A machine state wherein instructions are not executed, unmasked interruptions are accepted, and the timer is updated.

XIC. Transmission Interface Converter

9020D. IBM System for the Central Computer Complex.

9020E. IBM System for the Display Channel Processor.

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