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IBM Field Engineering Maintenance Manual

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7201-02 Computing Element

SFN-0203-1

PREFACE

This manual contains maintenance information for the IBM 7201-02 Computing Element. The manual is divided into six chapters and three appendices:

Chapter 1. Maintenance Philosophy
Chapter 2. Manual Controls and Maintenance Facilities
Chapter 3. Preventive Maintenance
Chapter 4. Checks, Adjustment, and Removals
Chapter 5. Power
Chapter 6. Locations
Appendix A. Special Circuits
Appendix B. Reference Data
Appendix C. Voltmeter Calibration Chart

Within this manual are references to "figures", "diagrams", and ALDs: Figure references pertain to illustrations in this manual. Diagram references pertain to illustrations contained in the companion FE Maintenance Diagrams Manual. ALD references pertain to engineering maintenance procedures and illustrations contained in a separate ALD volume(s).

Prerequisite and companion manuals are:

Prerequisite Manuals

9020E System Introduction, Theory of Operation Manual, Form SFN-0103
9020D System Introduction, Theory of Operation Manual, Form SFN-0104

Companion Manuals

7201-02 Computing Element, Theory of Operation Manual, Form SFN-0201
7201-02 Computing Element, Maintenance Diagrams Manual, Form SFN-0202
7201-02 Computing Element, Installation Manual, Form SFN-0204
7201-02 Parts Catalog, Form SFN-0205
9020 D/E Power Controls and Distribution, Theory of Operation Manual, Form SFN-0105
IBM 9020D and 9020E System Maintenance Monitor Manual, Part No. 5444417

Other Manuals Referenced:

SLT Packaging FETOM, Form SY22-2800

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ILLUSTRATIONS

TABLES

ABBREVIATIONS

ABC	AB register byte counter
ac	alternating current
adr	address
ALD	automated logic diagram
amp	ampere
ASC	address store compare
ATC	air traffic control
ATN	alternate test number
ATR	address translation register
BCD	binary-coded decimal
BSM	basic storage module
C	capacitor
CAS	control automation system
CB	circuit breaker
CC	condition code
CCR	configuration control register
CCW	channel command word

C/I	converter/inverter
CLD	control automation system logic diagram
cm	centimeter
CW	Computing Element
DAR	diagnose accessible register
dc	direct current
DE	Display Element
DSBL	disable
EPO	emergency power off
F	fuse, also Fahrenheit
FAA	Federal Aviation Agency
FEMDM	Field Engineering Maintenance Diagrams Manual
FEMM	Field Engineering Maintenance Manual
FETOM	Field Engineering Theory of Operation Manual
FLT	fault locating test
GCT	gate control trigger
gnd	ground
GT	gate
hex	hexadecimal
HSS	high-speed storage
Hz	Hertz (cycles per second)
IC	instruction counter
IDES	inhibit DE stop
ILC	instruction length code
ILOS	inhibit logout stop
IND	indicator
INSN	instruction
INTF	interface
I/O	input/output
IOCE	Input/Output Control Element
IPL	initial program load
KBD	keyboard
LADS	logic automation documentation system
loc	location
LS	local storage
LSAR	local storage address register
LSWR	local storage working register
ma	milliampere
MC	margin control
MCW	maintenance control word
MDM	Multiprocessing Diagnostic Monitor
MPLE	multiple
MPLR	multiplier
MPO	master power off
ms	millisecond
mv	millivolt
ns	nanosecond
oc	overcurrent
OBS	on battery signal
OEAP	operational error analysis program
OP	operation
OTC	out of tolerance check
ov	overvoltage
P	parity
PAA	parallel adder A-side
PAB	parallel adder B-side
PAL	parallel adder latch
PDU	power distribution unit
PN	part number
PREV	previous
PROC	process
PROSAR A	previous read only storage address register A
PROSAR B	previous read only storage address register B
PS	power supply
PSA	preferential storage area
PSBAR	preferential storage base address register
PSW	program status word
RLR	roller
rms	root mean square
ROS	read-only storage register
ROSAR	read-only storage address register
ROSDR	read-only storage data register
RPT	repeat
SA	sense amplifier
SAA	serial adder A
SAB	serial adder B, also storage address bus
SAL	serial adder latch
SAP	storage address protect
SATR	set address translation register
SBA	serial adder bus A
SBB	serial adder bus B
SC	System Console
SCI	storage control interface
SCON	set configuration
SCOPEX	scoping index
SCR	silicon-controlled rectifier
SDBI	storage data bus in
SDBO	storage data bus out
SDM	subsystem diagnostic monitor
SE	storage element
SEVA	system evaluation
SIO	start input/output operation
SLT	solid logic technology
SMS	standard modular system
STAT	status trigger
sync	synchronizing
T	transformer
TB	terminal binder
TCU	tape control unit
TIC	transfer in channel
TU	tape unit
usec	microsecond
V	volt

This chapter consists of two sections: Section 1 describes the overall maintenance concepts used by the 9020D/E System; Section 2 describes the maintenance concepts for the 7201-02 CE.

The maintenance features of the 9020D/E System are divided into two general categories:

1. On-line Maintenance – Those features used for error detection and isolation when the 9020D/E System is performing air traffic control functions.
2. Off-line Maintenance – Those features used for diagnosis of the malfunctioning element after it has been removed (reconfigured) from the active 9020D/E System.

SECTION 1. SYSTEM MAINTENANCE CONCEPTS

This section describes the on-line and off-line maintenance facilities available to the 9020D/E System.

1.1 ON-LINE MAINTENANCE FACILITIES

The basic maintenance strategy for the 9020D/E System is shown in Figure 1-1. Malfunctions within the 9020D/E System are recognized by both built-in circuitry and on-line diagnostic routines. When a malfunction is detected, special circuitry within the Computing Element (CE), Input/Output Control Element (IOCE), Storage Element (SE), and Display Element (DE) records the element's status. This recording, or logout, places the status information in the system's primary preferential storage area where it is available for analysis by the operational program. Malfunctions of other system elements and units are also recognized by appropriate interrupts, and the status of these elements is recorded as status bits in sense bytes.

Each of these malfunctions causes an entrance into the Operational Error Analysis Program (OEAP) which is a subprogram of the operational system. The purpose of the error analysis program is to:

1. Analyze the logout to determine the element or interface causing the malfunction.
2. Count the malfunctions and record the malfunction rate.
3. Record the logout and other system environmental data and immediately furnish an edited hard-copy printout.
4. Retry/restart on malfunctions where practical.
5. Request a system reconfiguration when the malfunction is nonclearing so that the malfunctioning element can be excluded from the operational system.

From an analysis of the edited hard-copy printout of a logout, maintenance personnel can localize the trouble area within the indicated element and request the operational program to provide the minimum maintenance subsystem that is required to run the off-line diagnostic programs.

1.2 OFF-LINE MAINTENANCE FACILITIES

After a malfunctioning element has been removed from the active system, a maintenance subsystem is requested for testing that element. The request is made manually, via the 1052, with prior authorization from responsible FAA personnel.

When a maintenance subsystem is available, diagnostic maintenance programs are loaded into storage from tapes and are executed by the CE or IOCE. The maintenance programs fall into two major categories: Fault Locating Tests (FLTs) and Checkout and Evaluation Tests.

The Fault Locating Tests, which isolate malfunctions at the circuit level, are available only for the CE and IOCE. A complete set of FLTs is produced automatically from the same logic description as that used to manufacture the element. Thus, the FLTs should be performed before any other diagnostics to ensure that operation of the element conforms to its design.

The Checkout and Evaluation Tests are used to localize malfunctions to a functional area within the element. In general, these tests have the following characteristics:

1. Looping capabilities to aid in malfunction isolation.
2. Options to run on various sizes of maintenance subsystems.
3. Options to run all or portions of the program.

A malfunctioning element is repaired primarily by removal and replacement of pluggable assemblies or subassemblies. An element that malfunctions because of a logic card failure is repaired by replacing the logic card. The following methods may be used to isolate the malfunctioning card:

1. Group replacement.
2. One-for-one substitution.
3. Scoping.

After repair, the failing FLT or Checkout and Evaluation Test is repeated to verify that the error has been corrected. If it has, a request is made via the 1052 Keyboard to return the repaired element to a recallable state.

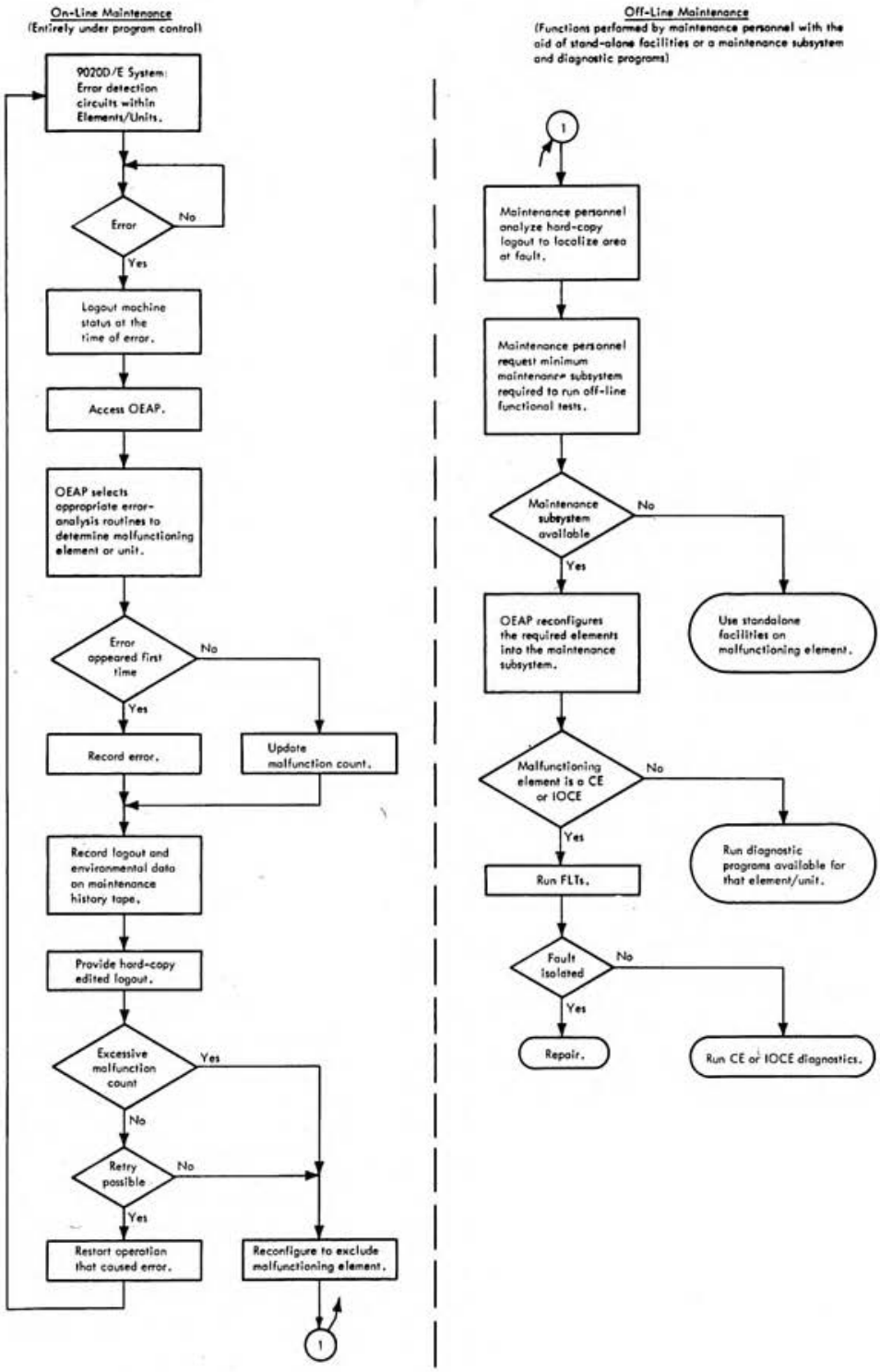


Figure 1-1. System Maintenance Strategy

Maintenance features for the IBM 7201-02 Computing Element fall into two general categories:

1. On-Line Maintenance – Those features used for error detection during normal operation, such as error-detecting logic and interruptions.
2. Off-Line Maintenance – Those features used to diagnose the cause of failures and for preventive maintenance. This category includes the CE control panel, logout, FLTs, ROS tests, Diagnose instruction, DE wrap bus, and a microprogram diagnostic.

1.3 ON-LINE MAINTENANCE

1.3.1 CE Check Handling

Check conditions are classified in two categories: (1) internal checks which are detected within the CE itself, and (2) external checks which are detected by the CE as a result of its operation with other elements. Any check condition sets an identifier bit on in check register 1 or 2, except out-of-tolerance (OTC) condition or on-battery supply (OBS). These two conditions set identifier bits on in DAR and cause an external interrupt request. Check register bits are indicated on an edited logout printout and are described in Chapter 2.

1.3.2 Interruption Action

The interruption system permits the CE to change its state as a result of conditions arising outside the system, in I/O units, or in the CE itself. The five classes of these conditions are input-output, program, supervisor call, external, and machine-check interruptions.

An interruption consists of storing the current PSW as an old PSW and fetching a new PSW. Processing resumes in the state indicated by the new PSW.

1.3.3 Logout

The logout feature of the CE records, in fixed storage locations, the state of the CE triggers. Recording is accomplished by storing binary bits that represent the states of the various triggers and registers in the CE. Logout is automatic following a CE machine check with machine checks enabled (PSW 13 on and CE Check switch in PROC), or it can be initiated manually by depressing the LOGOUT pushbutton. Logout is also initiated under program control by use of the Diagnose instruction (log on count option).

The occurrence of a machine check with machine checks enabled (PSW 13 on) forces the following sequence:

1. The CE clock is stopped (controlled clock).
2. The logout is executed.
3. The CE is reset, the controlled clock is started, and an interrupt sequence is initiated. This causes a fetch of the new machine check PSW and a store of the old PSW. Before the store, the old PSW is set with an interrupt code of all 0's, which denotes a CE internal machine check.

The logout information is then processed, edited, recorded on tape for history, and printed. From the printed copy, maintenance personnel can diagnose the cause of the machine check.

1.4 OFF-LINE MAINTENANCE

The surest means of trouble isolation is by running FLTs and Diagnostic programs on a maintenance subsystem which includes the malfunctioning CE. However, many malfunctions can be localized and fixed by interpreting the error indications on the CE panel or by analyzing the printed logout for the malfunctioning CE.

1.4.1 Edited Logout

Status information logged out into the PSA is processed and edited by the OEAP for a hard-copy printout on the 1403 High-Speed Printer. The 1403 is the primary printer; however, an option is provided to print on the 1052 Printer-Keyboard if the 1403 is not available. When the 1403 is available and used for logout, a message is printed on the 1052 to notify the operator that a logout has been initiated.

This printout of the edited logout provides maintenance personnel with a detailed description of the status of all triggers, latches, and registers that are displayed on the CE console, at the time a check is detected.

1.4.2 Maintenance Programs

There are two categories of maintenance programs for the CE:

1. Fault Locating Tests (FLTs) – These tests provide the best means of isolating solid CE failures and should be run first. The operating procedures for these tests are on LADS A6503.
2. Diagnostic Tests – There are many maintenance diagnostic programs for the CE, each having unique functions and uses. For a description of these programs, refer to IBM 9020D and 9020E System Maintenance Monitor Manual, Part No. 5444417.

1.4.3 Diagnose Instruction

The Diagnose instruction is provided as a maintenance tool and is used extensively by diagnostic programs (Refer to 7201-02 FETOM for a detailed description of the Diagnose instruction.)

From a maintenance viewpoint, troubleshooting of the CE can be reduced to one of the following situations:

1. CE Panel Observation. The trouble is apparent from examination of error indicators on the CE panel; e.g., a power malfunction. In such cases, the cause of the malfunction should be further isolated through suitable test equipment. After repair, the CE panel should be used to establish that the malfunction has been corrected. If the error still persists, further trouble isolation should be performed through analysis of the printed logout or by means of a maintenance subsystem.
2. Logout Analysis. Malfunctions can be isolated to a functional area within the CE by studying the latest logout information for that CE and by comparing the information with previous logouts. The malfunctions revealed by logout analysis may fall into one of two categories: (a) those that can be fixed without the use of a maintenance subsystem and (b) those that require a maintenance subsystem for further troubleshooting.
3. Analysis by Maintenance Subsystem. A maintenance subsystem is the ultimate means for malfunction isolation. It enables maintenance personnel to run FLTs and diagnostic programs on the malfunctioning CE. Program loading, control functions, and code conversations between maintenance personnel and the diagnostic tests are effected via the diagnostic monitor programs available to a maintenance subsystem.

The maintenance approach for the CE is shown in Diagram 1-1 of the 7201-02 FEMDM. This section describes, in general terms, a number of maintenance techniques used for fixing the CE. Whenever appropriate, this section refers to specific step-by-step procedures contained in this manual or to the related diagnostic documentation.

1.4.4 Scan Operations

Scan logic and controls provide a means of implementing FLTs and logout. Scan-in operation is a process of setting and resetting register and control triggers with a predetermined bit pattern from main storage to check for and locate a failing component. Logout (scan-out) operation is a process of recording the status of triggers and registers by developing a bit pattern from the CE console indicator logic and storing it in main storage. Refer to LADS pages A6521-A6641 for a description of storage locations for logout and scan-in.

1.4.5 DE Wrap Bus

The DE wrap bus is a maintenance feature that allows a CE to simulate display generator (DG) operations by executing a Diagnose instruction. It is a 16-bit bus from the DG interface of a DE and is gated alternately to K(0–15) and K(16–31) while being used.

1.4.6 Microprogram Diagnostic

The microprogram diagnostic is a special ROS routine provided for maintenance personnel to use in locating a failure of CE registers or data flow paths. It is started by doing a ROS transfer to address FAA, and, once started, it will loop on itself. If the CHECK CONTROL switch on the CE control panel is in the STOP position, the routine is stopped by CE error-checking logic detecting an error.

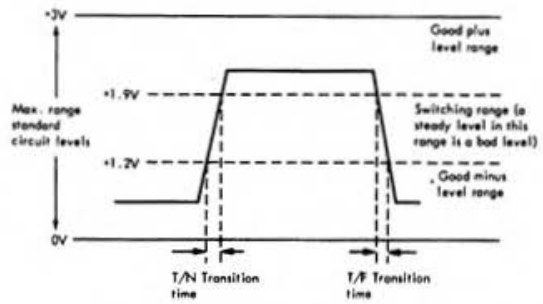
1.4.7 CE Control Panel Functions

The main functions provided by the CE control panel are the ability to store and display information in storage and in registers, to load initial program information, and to perform voltage bias testing.

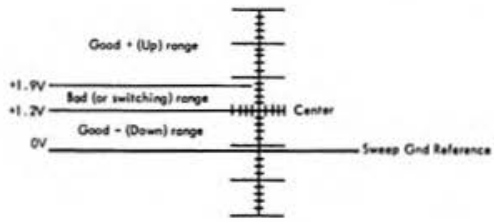
1.4.8 Circuit Levels

The CE uses the AOI (AND, OR, INVERT) family of high-speed circuits. The switching speeds of these circuits are approximately 5 to 15 ns. The maximum range of signal voltage levels in the system is 0 to +3V.

To compare one standard level pulse to another or to measure a pulse width, an understanding of switching points is required. The switching points for high-speed circuits are shown in Figure 1-2, A. For the positive-going slope of a pulse, the switching point is +1.2V above ground (0V); for the negative-going slope of a pulse, the switching



A. STANDARD LEVEL PULSE, SWITCHING POINTS



B. STANDARD SWITCHING LEVELS

Figure 1-2. CE Circuit Levels

point is +1.9V above ground (0V). This applies to both + pulses and - pulses. A useful method to follow when scoping is:

1. Set vertical calibration to 1V/div.
2. Ground the input to be used for scoping.
3. Set the vertical position (with free-running trace) until trace is 1.2 cm (volts) below center.
4. Now, while scoping, any steady level below the center line is a good "down" level, any steady level in the 1-cm division above the center line is bad or doubtful, and any steady level in the second 1-cm division above center is a good "up" level (Figure 1-2, B). Actually, not all of the 1-cm division above center is in the bad level range; only 0.7 of it.

1.4.9 Sync Signals and Locations

Main storage address compare sync is available whenever the CE is operating and an equal compare occurs between the storage address bus and MAIN STORAGE ADDRESS COMPARE switches (bits 9–28 of the ADDRESS switches). The ALD reference is MA301–321. ROS address compare sync is available whenever the CE is operating and an equal compare occurs between ROSAR and ROS ADDRESS COMPARE switches (bits 8–19 of the ADDRESS switches). The ALD reference is RX301–303. Both main storage and ROS address compare sync signals are available on coaxial connectors at the front of gate C.

The IBM 9020D System and the 9020E System have two principal control facilities: (1) the Computing Element Control Panel and (2) the System Console (9020D System) or the Configuration Console (9020E System).

The System Console (SC) is the central monitoring and control position in the 9020D System. It contains the switches and lights necessary to selectively operate and control each CE in the system. All critical console functions are duplicated on the CE Control Panel or elsewhere in the system.

The Configuration Console (CC) provides a similar function for the 9020E System and, in addition, provides status indications for the display subsystem. All critical CC functions are duplicated on the CE Control Panel or elsewhere in the system.

The CE Control Panel provides the facilities necessary to operate a computing subsystem and also contains the controls and indicators required to diagnose and repair machine malfunctions. This chapter describes the operation of all controls on the CE Control Panel only. However, if a control is also duplicated on the System or Configuration Console, the operation of that control (at the SC or CC) is also discussed. For a detailed description of all controls and indicators on the SC or CC, refer to the appropriate documentation for these units.

Those operator controls at the CE Control Panel which could be inadvertently used to disrupt the operation of the 9020D/E System are under control of a key-operated SYSTEM INTERLOCK switch. A separate SYSTEM INTERLOCK switch is provided at the CE Control Panel and at the SC or CC. When the interlock switch is operated at the CE Control Panel, the panel can perform a number of system functions. Thus, the CE Control Panel can also be used as backup for the SC or CC. However, if the interlock switch at the SC or CC and the interlock switch at the control panel of the selected CE are operated simultaneously, the SC or CC takes precedence.

A Computing Element with its power on can be in one of four states: three, two, one, and zero. These states are displayed at the CE Control Panel. In addition to the four STATE indicators, a TEST switch is provided which is functional only in the zero state. The states are defined by setting the state bits (S0, S1) of the Configuration Control Register (CCR) within the CE. The state bits and the SYSTEM INTERLOCK switch control the effect of all manual switches on the CE Control Panel.

2.1 CE CONTROL PANEL, DESCRIPTION OF CONTROLS AND INDICATORS

The Computing Element Control Panel contains the switches and indicators necessary to operate and control a subsystem. A subsystem is considered a combination of CEs, SEs, DEs (9020E system only), IOCEs, control units, and I/O devices. The main function of the control panel is to provide the ability to store and display information in main storage, local storage, some registers, part of the program status word (PSW); to allow the operator to reset the system; and to perform the initial program load (IPL) sequence. Table 2-1 lists the CE switches and their operational environment.

The control panel is divided into seven panels (A–G) as shown in Diagram 6-1 of the 7201-02 FEMDM. The following headings discuss the function of the controls and indicators located on each panel.

2.1.1 Panel A

1. DC voltmeter. Indicates the voltage levels of the marginable power supplies in the CE. The power supply to be indicated is determined by the MARGIN/METER SEL switch.
2. MARGIN/METER SEL switch. Enables selection of the power supply output voltage to be indicated on the meter. This switch has six positions:
   a. GATE A – Selects PS 16.
   b. GATE B – Selects PS 15.
   c. GATE C – Selects PS 8.
   d. GATE E – Selects PS 7.
   e. GATE K AND L – Selects PS 5 (Frame 02).
   f. ROS – Selects PS 11.
3. MARGIN indicators:
   a. ACTIVE: Indicates when any marginable power supply in the CE is varied from its nominal setting.
   b. LOCATE: Indicates when the power supply selected by the MARGIN/METER SEL switch is varied from its nominal voltage.
4. POWER STATUS:
   a. MAIN LINE ON indicator: Indicates that 208V ac is being supplied to the CE, and CB1 in the prime power box of the CE is closed. Refer to ALD YA082.

Table 2-1. Control Panel Switch Enabling

Switches	CE Program State	SYSTEM INTERLOCK Switch									
		OFF					ON				
		3	2	1	0	Ø	3	2	1	0	Ø
Address Compare	X			X	X	X	X	X	X	X	X
Address*		X	X	X	X	X	X	X	X	X	X
Backspace FLT	X X X				X	X				X	X
Check Control	X X X				X	X				X	X
Check Reset	X X X				X	X				X	X
Data*		X	X	X	X	X	X	X	X	X	X
Defeat Interleaving	X				X	X				X	X
Disable Interval Timer	X X				X	X				X	X
Display	X			X	X	X	X	X	X	X	X
Element MPO	X X X	X	X	X	X	X	X	X	X	X	X
Frequency Alteration	X X X					X					X
Indicate On Roller 1 Pos. 6	X X X	X	X	X	X	X	X	X	X	X	X
Inhibit CE Hard Stop	X X X				X	X				X	X
Interrupt	X X			X	X	X	X	X	X	X	X
Key (System Interlock)	X X X	X	X	X	X	X	X	X	X	X	X
Lamp Test/Allow Indicate†	X X X	X	X	X	X	X	X	X	X	X	X
Load	X X X			X	X	X	X	X	X	X	X
Load Unit*				X	X	X	X	X	X	X	X
Logout	X			X	X	X	X	X	X	X	X
Main Storage Select		X	X	X	X	X	X	X	X	X	X
Marginal Check and Voltage Controls	X X X	X	X	X	X	X	X	X	X	X	X
Power Off	X X X					X					X
PSW Restart	X X X			X	X	X	X	X	X	X	X
Pulse Mode	X X X					X					X
Rate	X			X	X	X	X	X	X	X	X
Register Select*	X					X					X
Register Set	X					X					X
Repeat Instruction	X			X	X	X			X	X	X
Repeat ROS Address	X X X			X	X	X			X	X	X
ROS Transfer	X			X	X	X			X	X	X
Scan Mode	X X X				X	X				X	X
Set IC	X			X	X	X	X	X	X	X	X
Start	X			X	X	X	X	X	X	X	X
Store	X			X	X	X	X	X	X	X	X
Stop	X X			X	X	X	X	X	X	X	X
Stop On ROS Address	X X X			X	X	X			X	X	X
Storage Select*				X	X	X	X	X	X	X	X
System Reset	X X X			X	X	X			X	X	X
Test Switch	X X X				X	X				X	X
360 Mode	X X X			X	X	X			X	X	X

Legend:
- X – Control is functional.
- * – Static; requires use of other control.
- Ø – State 0 and Test mode.
- † – Allow indicate in Scan mode, state 1 and 0 only.

b. OBS (on battery signal) indicator: Indicates that the CE is being powered with its battery backup power.
c. THERMAL indicator: Indicates the presence of an excessive heat condition within one of the CE's logic gates or power panels.
d. POWER CHECK indicator: Indicates an incomplete power-up condition, a thermal condition, or an overcurrent/undervoltage condition at one of the dc regulators.

2.1.2 Panel B

The six controls on this panel raise or lower the output voltage level of the six marginal regulators.

2.1.3 Panel C

ELEMENT MPO PULL switch. Pulling this switch knob opens the master power off (MPO) switch which shuts off all power in the CE except the 24V ac supply and the battery power supply.

2.1.4 Panel D

1. 360 MODE indicating pushbutton. A back-lighted pushbutton that places the CE (and IOCE 1 if configured) in System/360 mode when depressed. When in 360 mode (light on), depression of the pushbutton restores to 9020 mode.
2. STATE indicators. These four lamps indicate the operational capability of the CE, defined by CE CCR bits 0 and 1 as follows:
   a. THREE: Bits 0, 1 = 11. Most of the control panel controls are disabled.
   b. TWO: Bits 0, 1 = 10. Most of the control panel controls are disabled. A CE in state two cannot execute a SCON instruction (specification exception).
   c. ONE: Bits 0, 1 = 01. Control panel operation controls are enabled. A CE in state one cannot execute a SCON instruction (specification exception).
   d. ZERO: Bits 0, 1 = 00. All control panel controls are enabled if TEST switch is set to TEST position. TEST switch set to the normal position will disable power on/off; frequency alteration; pulse mode, manual setting of CE CCR, ATR, and PSBAR; and external control signals (SCON and SATR).
3. TEST switch. Switch is effective only in state zero.

2.1.5 Panel E

1. Roller indicators. These indicators are arranged in six groups of thirty-six each, to provide a display of CE status information. The data displayed in each set of lights is controlled by a selector rotary switch which can select up to six words. Roller 1 position 6 is used to display L- and M-registers under control of IND RLR 1 switch. The selector rotary switches also adjust a roller format to identify the information displayed. Refer to Table 2-2 for a description of individual roller indicator positions.
2. DATA 0–31 and DATA 32–63 switches. These 64 switches, in hexadecimal groups, permit data to be entered manually as follows:
   a. Main storage – switches 0–63.
   b. Local storage – switches 32–63.
   c. ATR – switches 0–3.
   d. CCR – switches 32–63.
   Correct parity is generated.

   Switches 53–63 supply a count in pulse mode count operation.
3. ADDRESS switches. These 24 switches provide a means of manually selecting any location in storage. The operation is as follows:
   a. Twenty-four switches, arranged in hexadecimal groups, permit manual storage addressing of main storage and local storage.
   b. Correct parity is generated.
   c. ADDRESS switches 9–28 are used in conjunction with the ADDRESS COMPARE switch to cause an address compare stop or address compare sync.
   d. ADDRESS switches 8–19 select the ROS address for a ROS address compare sync. A sync pulse is generated whenever there is a compare between the ROS address and the switch setting.
4. CHECK REG 1 SUMMARY indicator. An error condition in the CE is indicated as defined in check register 1 (roller 2, position 2).
5. CHECK REG 2 SUMMARY indicator. An error condition in the CE is indicated as defined in check register 2 (roller 6, position 5).

Table 2-2. Roller Indicators

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
1	1	0–3	CE SELECT ATR	KR 051	SATR or SCON from CE 1–4.
1	1	4	TC STEP	KD 601	Time clock step trigger.
1	1	18–26	G REGISTER (WRITE DIRECT)	RG 001	Contents of G register.
1	1	27–35	ATR-2	FA 091	Contents of ATR (32–29).
1	2	0–8	F REGISTER (READ DIRECT)	RF 001	Contents of F register.
1	2	9–35	D REGISTER	RD 001	Contents of D register.
1	3	0–35	S REGISTER	RS 001	Contents of S register.
1	4	0–11	READ ONLY STORAGE ADDRESS REGISTER	RX 021	Contents of ROSAR.
1	4	12–23	ROS PREVIOUS ADDRESS REGISTER A	RX 211	Contents of previous ROS address register A, (PROSARA).
1	4	24–35	ROS PREVIOUS ADDRESS REGISTER B	RX 211	Contents of previous ROS address register B, (PROSARB).
1	5	0–35	SELECT REGISTER	FS 001	Contents of select register.
1	6	0–35	L or M REGISTER	XL 031	Contents of L or M register (selected by IND RLR 1 switch).
2	1	0–35	ADDRESS TRANSLATION REGISTER 1	FA 111	Contents of ATR (0–31).
2	2	0	E REG PTY	RE 181	Parity error in E (0–15).
2	2	1–9	PADD FULL SUM	AP 075	Full-sum parity error.
2	2	18	MLPR DECODE PTY	DP 091	Parity error in multiplier (S register).
2	2	19–26	PADD HALF-SUM	AP 791	Half-sum parity error.
2	2	27	ERROR TGR	AP 801	Half-sum error.
2	2	31–33	ROS PTY	DS 431	ROS parity error.
2	2	34,35	SADD	AS 095	Half-sum or full-sum error in serial adder.
2	3	0–35	T REGISTER	RT 321	T register contents.
2	4	2–5	FAA CONTROLS	RY 015	Miscellaneous control lines.
2	4	6–9	AB, IC INGATES	RY 021	Ingating to A,B,IC.
2	4	10,11	LS-T, LS-S	RY 031	Gate local store to S, T.
2	4	12–16	ST, D, Q, G, PSW INGATES	RY 041	Ingating to D,K,Q,S,T,PSW,N,G.
2	4	17–20	F INGT AND EOP	RY 071	End ops and gate serial adder to F.
2	4	21–24	EMIT	RY 061	Emit and ingating to E,R.
2	4	25–30	MISC CONTROL PART 2	RY 101	Miscellaneous control lines.
2	4	31–35	MISC CONTROL PART 1	RY 081	Set IC and miscellaneous control lines.
2	5	0–35	X REGISTER	XX 031	Contents of X register.
2	6	0–35	K REGISTER	RK 001	Contents of K register.
3	1	0–5	STORAGE REQUEST	MC 061	Source of storage request.
3	1	6	PAGE 1 LTH	MC 991	Forced storage cycle for address of new page.
3	1	9–21	MANUAL CONTROLS	KW 031	CE control panel manual control functions.
3	1	22–35	FLT CONTROLS	KU 211	FLT control functions.
3	2	0–35	Q REGISTER	RQ 001	Contents of Q register.
3	3	0–35	A REGISTER	RA 001	Contents of A register.
3	4	0–6	EXTD and LS LAR CONTROL	RY 131	Local storage and special register controls.
3	4	7–10	STOR REQ SET MARK	DR 191	Memory request and mark setting.
3	4	11–20	NEXT ROS BASE ADDRESS	DS 401	ROSAR (0–9) for next ROS address.
3	4	21–25	Y BRANCH	DS 411	Conditional branch (ROSAR bit 10 for next ROS address).
3	4	26–32	X or Z BRANCH	DS 421	Conditional and functional branches (ROS bit 11 for next ROS address).
3	4	34	PREV ADR A	RX 201	Contents of PROSARA addresses previous ROS word.
3	4	35	FLT MODE	KU 471	Scan mode trigger.
3	5	0–2	PERMIT IOCE	KM 321	IOCE interrupt being processed.
3	5	3–5	IOCE MACH CHK	KM 331	IOCE machine check interrupt request.
3	5	6–8	SEL IOCE	KX 111	IOCE-CE operations in progress.
3	5	9	IOCE INTRPT REQ	KM 321	IOCE interrupt request.
2	5	10	IOCE MC REQ	KM 331	IOCE machine check interrupt being processed.
3	5	11	INTRPT GATE TGR	KX 181	Allow interrupt (ROS).

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
3	5	18–35	N REGISTER	XN 091	Contents of N register.
3	6	0–35	Y REGISTER	XX 351	Contents of Y register.
4	1	0–8	SYSTEM MASK	RW 011	I/O and external interrupts permitted.
4	1	9–13	KEY	RW 081	PSW storage protect key.
4	1	14	ASCII	RW 121	"USA Standard Code for Information Interchanges" mode of operation.
4	1	15	MC	RW 121	Machine check interrupts permitted.
4	1	16	WAIT	RW 121	Wait mode of operation.
4	1	17	PROB	RW 151	Problem mode of operation.
4	1	18	NO RETRY	KS 321	Instruction retry not advisable (programmer flag).
4	1	19	IC IN LSWR	KS 321	Contents of IC have been stored in LSWR.
4	1	20,21	COND CODE	RW 351	Current PSW condition code.
4	1	22–25	PSW PROGRAM MASK	RW 361	Current PSW program mask.
4	1	26	MACH CHK INTRPT	KM 121	Machine check interrupt is pending or being processed.
4	1	27	SUPV CALL INTRPT	KM 121	Supervisor call interrupt is pending (result of execution of "supervisor call" instruction).
4	1	30–33	PROGRAM INTRPT	KM 141	Program old PSW interrupt code, bits 28–31.
4	1	34,35	INTRPT PRI	KN 121	Priority assignments of current interrupt.
4	2	0–35	Q REGISTER	RQ 321	Contents of Q register.
4	3	0–35	B REGISTER	RB 321	Contents of B register.
4	4	0–4	A SIDE CTL SERIAL ADDER	AR 301	Ingating to serial adder, A side.
4	4	5–8	B SIDE CTL SERIAL ADDER	AR 801	Ingating to serial adder, B side.
4	4	9–11	PADDL CONTROL	AP 821	Ingating to parallel adder latches.
4	4	12	EW EXTD	AP 743	Block gating ST to serial adder B side.
4	4	13–15	GATE ONES PA	AP 811	Emit control for serial adder A side.
4	4	16	P 43–68	DS 411	Parity for ROS bits 43–68.
4	4	17	AB → F	AP 901	Gate contents of F to serial adder A side.
4	4	18–21	AB, IC, F → PB	RB 816	Ingating to parallel adder B side from A,B, and IC.
4	4	22	P 69–99	AP 901	Parity for ROS bits 69–99.
4	4	23–26	ST, DA → PA	RT 822	Ingating to parallel adder A side.
4	4	28–30	E, Q → PB	RQ 822	Ingating to parallel adder B side from E and Q.
4	4	32	RT DIG	KZ 321	Right digit trigger set (edit control).
4	4	33	S	KZ 321	Significant digit trigger set (edit control).
4	4	34	LEAVE	KZ 201	Character in edit control mask.
4	4	35	STEP ABC	KZ 501	Step ABC (edit control).
4	5	0–7	STATUS TRIGGERS	KS 021	Microprogram control triggers.
4	5	8	BLOCK	KD 501	Block I-fetch.
4	5	9–11	1 2 3	KD 111	I-fetch control triggers.
4	5	12	EXEC	KD 601	Execute instruction being performed.
4	5	14	PS CMPR	KD 501	Program store compare.
4	5	15	IN STOR FETCH	KD 701	I-fetch required.
4	5	16	BR INVLD ADDR	KD 701	Branch instruction execution developed invalid instruction address.
4	5	17	INVLD ADDR	KD 711	I-fetch invalid address.
4	5	18	IL NOT AVAIL	KM 85	Instruction length not available because of I-fetch storage protection check.
4	5	19–22	CE 1, CE 2	JA 211	Write direct (WD) and read direct (RD) external interrupt signals from CEs 1 and 2
4	5	23	TC AT LIMIT	JA 201	External interrupt signal resulting from the contents of the internal timer (time clock) being reduced to zero.
4	5	24	CONS SIG	JA 201	External interrupt signal resulting from the depression of INTERRUPT pushbutton.
4	5	25–28	CE 3, CE 4	JA 211	Write direct (WD) and read direct (RD) external interrupt signals from CEs 3 and 4.
4	5	29	PIR	JA 251	Interrupt request from an IOCE.
4	5	30	DAR	JA 251	External interrupt resulting from an ELC.

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
4	5	31–33	PIR	KM 381	Interrupt request from an IOCE.
4	5	35	TIME GATE TGR	KX 311	Timing gate trigger for external interrupt timing.
4	6	0–35	EXTERNAL REGISTER	FE 001	Contents of external register.
5	1	0–4	PHYSICAL RSBAR	MP 111	Contents of Physical PSBAR.
5	1	5–9	PSBAR COUNTER	MP 301	Contents of PSBAR Counter.
5	1	10–22	LOGICAL PSBAR	MP 201	Contents of Logical PSBAR.
5	1	23	ALT PSBA	MP 501	PSBAR has been stepped to alternate.
5	1	28–31	SYSTEM MASK	RW 161	System mask for channels 7-A (allow I/O interrupt).
5	1	32	SE STOP	KM 158	Storage request to an SE or a DE that is stopped.
5	1	33–35	PSA LOCKOUT	KM 158	PSA lockout signal from IOCE 1–3.
5	2	0	KEY SABTP (Process mode)	KU 001	MCW bit 0, reverse SAB tag, parity (SAB P1–5).
5	2	1	LCMPR (Process mode)	KU 001	MCW bit 1, start count on storage address compare (used with MCW bits 21–31).
5	2	2	REV SAFSP (Process mode)	KU 001	MCW bit 2, reverse serial adder full sum parity.
5	2	3	REV MRKP (Process mode)	KU 011	MCW bit 3, reverse mark parity.
5	2	0–3	CE TEST ADDR (Scan mode)	KU 011	MCW bits 0–3, address of ROS bit plane being tested (used for display only).
5	2	4	REV SARPA (Process mode)	KU 011	MCW bit 4, reverse storage address parity for byte 1 (SAC P 8–15).
5	2	4	LFTHF (Scan mode)	KU 011	Left half of word being scanned out contains the expected status of the trigger being tested.
5	2	5	REV SARPB (Process mode)	KU 011	MCW bit 5, reverse storage address parity for byte 2 (SAB P16–20).
5	2	5	UNCT (Scan mode)	KU 011	Unconditional terminate at end of current test.
5	2	6	LOG CNT (Process mode)	KU 021	MCW bit 6, start logout when FLT counter steps to zero.
5	2	6	CONDT (Scan mode)	KU 021	Conditional terminate, stop at end of current test if an error is encountered.
5	2	7	ERSLT (Scan mode)	KU 021	Expected result of the trigger being tested.
5	2	8	DSBL TMR	KU 021	MCW bit 20, disable internal timer (used for display only in scan mode and indicates a successful hardcore stop).
5	2	9–13	ADDR SEQUENCE	KU 101	Contents of address sequence register.
5	2	14–17	FLT COUNTER	KU 111	Contents of FLT counter.
5	2	18,19	FLT CHK	KU 271	FLT clock.
5	2	21–23	ROS TEST SEQ	KU 121	ROS test sequence, controls scan logic during a ROS test.
5	2	29	PASS	KU 391	An FLT or a ROS test has been completed and the expected result was obtained.
5	2	30	FAIL	KU 391	An FLT or a ROS test has been completed and the expected result was not obtained.
5	2	32	FLT STG ERR	KU 471	Any storage error detected while performing an FLT or a ROS test.
5	2	34	MMSC	KU 251	Maintenance mode stop clock.
5	2	35	BFR 1	KU 531	Buffer 1 (main storage 100–187) contains control information for FLT or ROS test being performed.
5	3	0–17	R REGISTER	RR 001	Contents of R register.
5	3	18–35	E REGISTER	RE 001	Contents of E register.
5	4	0	S 0–31 32–63	RT 815	Gate S (0–31) to parallel adder A (32–63).
5	4	1	T 32–63 32–63 T	RT 807	Gate T (32–63) to parallel adder A(32–63) true.
5	4	2	T 32–63 32–63 C	AP 731	Gate T (32–63) to parallel adder A (32–63) complement.
5	4	3	T32–63 31–62 TL 1	RT 811	Gate T (32–63) to parallel adder A (31–62) true.
5	4	4	T32–63 31–62 CL 1	RT 811	Gate T (32–63) to parallel adder A (31–62) complement.

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
5	4	5	T32–47 48–63	RT 813	Gate T (32–47) to parallel adder A (48–63).
5	4	6	T48–63 48–63	RT 815	Gate T (48–63) to parallel adder A (48–63).
5	4	7	K00–31 32–63	RT 817	Gate K (00–31) to parallel adder A (32–63).
5	4	8	D 8–31 8–31 T	RT 803	Gate D (8–31) to parallel adder A (8–31) true.
5	4	9	D8–31 8–31 C	RT 803	Gate D (8–31) to parallel adder A (8–31) complement.
5	4	10	D8–31 7–30 T	RT 805	Gate D (8–31) to parallel adder A (7–30) true.
5	4	11	D8–31 7–30 C	RT 805	Gate D (8–31) to parallel adder A (7–30) complement.
5	4	12	D8–31 40–63 T	RT 801	Gate D (8–31) to parallel adder A (40–63) true.
5	4	13	D8–31 40–63 C	AP 811	Gate D (8–31) to parallel adder A (40–63) complement.
5	4	14	FMTO	RT 843	Gate LM to XY per E 13–15 – used when executing repack symbols instruction to move history or current data from old refresh memory to new refresh memory.
5	4	15	FMTN	RT 843	Gate LM to XY per E13–15 – used when executing repack symbol instruction to move new data from a sort bin to new refresh memory.
5	4	16	FMTW	RT 843	Gate LM to XY per E14, 15 – used when executing convert weather lines instruction to assemble the correct doubleword format in XY.
5	4	17	IC 40–63	RB 811	Gate IC (8–31) to parallel adder B (40–63).
5	4	18	A 0–31 32–63	RB 805	Gate A(0–31) to parallel adder B (32–63).
5	4	19	A4–7 4–7	RB 805	Gate A(4–7) to parallel adder B(4–7).
5	4	20	A8–31 8–31	RB 757	Gate A(8–31) to parallel adder B (8–31).
5	4	21	B32–63 32–63	RB 813	Gate B (32–63) to parallel adder B(32–63).
5	4	22	B 64–67 64–67	RB 761	Gate B (64–67) to parallel adder B (64–67).
5	4	23	A6–31 4–29	RB 811	Gate A (6–31) to parallel adder B (4–29).
5	4	24	B32–67 30–65	AP 745	Gate B (32–67) to parallel adder B (30–65).
5	4	25	B64–67 28–31	RB 757	Gate B (64–67) to parallel adder B (28–31).
5	4	26	EXCS 6 28–63	AP 737	Generate excess 6 decimal correction factor to parallel adder B (28–63), used while executing convert to decimal instruction.
5	4	27	F 4–7 60–63	RB 807	Gate F (4–7) to parallel adder B (60–63).
5	4	28	HOT 1 60	RB 807	Generate a 1 bit to parallel adder B (60) which effectively adds +8.
5	4	29	E8–11 56–59	RQ 801	Gate E(8–11) to parallel adder B (56–59).
5	4	30	E 12–15 60–63	RQ 801	Gate E (12–15) to parallel adder B (60–63).
5	4	31	E 8–11 60–63	RQ 801	Gate E(8–11) to parallel adder B (60–63).
5	4	32	Q 4–15 52–63	RQ 815	Gate Q (4–15) to parallel adder B (52–63).
5	4	33	Q 20–31 52–63	RQ 815	Gate Q (20–31) to parallel adder B (52–63).
5	4	34	Q 36–47 52–63	RQ 815	Gate Q (36–47) to parallel adder B (52–63).
5	4	35	A52–63 52–63	RQ 815	Gate Q (52–63) to parallel adder B (52–63).
5	5	1,2	STATE	FC 001	Operational state of CE.
5	5	3–6	SCON	FC 001	Reconfiguration accepted from indicated CE.
5	5	7	ILOS	FC 061	CE will not issue logout stop signal to SE or DE..
5	5	10–20	SE SE/DE	FC 071	CE is able to communicate with indicated element.
5	5	23–26	CE	FC 191	CE is able to communicate with indicated element.
5	5	33–35	IOCE	FC 271	CE is able to communicate with indicated element.
5	6	0–35	DIAGNOSE ACCESSIBLE REGISTER MASK	FD 501	Indicated element is allowed to cause an external interruption in the CE.
6	1	0–35	PARALLEL ADDER LATCHES	AP 321	Contents of parallel adder latches (32–63).
6	2	0–8	MASKS	CT 011	Individual bytes of doubleword to be entered into main storage on a store operation.

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
6	2	10–14	LS ADDRESS REGISTER	LS 851	Contents of local storage address register.
6	2	15	LS WRITE	LS 812	CE is executing a micro-instruction to write into local storage.
6	2	16	INHIB STORE WRITE	RX 003	Inhibit storing into local storage.
6	2	17	TX TGR	DP 071	Multiply control trigger.
6	4	24–26	TCU ELC	FD 211	An external interrupt request from a TC 4 caused by an element check.
5	4	28	OTC	KT 291	An external interrupt request caused by an out-of-tolerance (heat) condition in the CE.
6	4	29	OBS	KT 291	An external interrupt request caused by an on-battery condition in the CE.
6	4	31–34	CE ELC	KT 291	An external interrupt request caused by an element check in a CE.
6	5	1–4	STOR UNIT CHECK ID	MC 961	Binary identification of SE or DE gating data to storage data bus out or causing time out pulse to be activated in the CE.
6	5	5	360 MODE	KM 201	CE is in 360 mode of operation.
6	5	6	TEST MODE	PX 331	CE is in state 0 and TEST switch is in TEST.
6	5	7	SE STOP 360	KM 201	Select pulse has been sent to a SE that is stopped while the CE is operating in 360 mode.
6	5	10	SAB PTY CHK	MA 951	Parity error is detected in SAB.
6	5	11	SDBI PTY CHK	MB 273	Parity error detected on SDBI.
6	5	12	STG TO	MC 753	SE or DE did not respond to a select signal within prescribed time.
6	5	13	STG ADDR CHK	MC 756	Storage address check signal received from an SE or a DE.
6	5	14	STG DATA CHK	MC 756	Storage data check signal received from an SE or a DE.
6	5	15	FETCH CHK	MC 941	Parity error detected on SDBO during a fetch cycle.
6	5	16	LOS SENT	MC 923	Logout stop signal sent to an SE or a DE.
6	5	19	IOCE CHK RESP	KX 311	Check response signal received from IOCE (error condition).
6	5	20	LS BUS CHK	BF 441	Parity error detected in local storage out bus.
6	5	21	CCR PTY CHK	FC 361	Parity error detected in CCR.
6	5	22	ATR PTY CHK	FA 141	Parity error detected in ATR.
6	5	23	PSBAR PTY CHK	MP 441	Parity error detected in PSBAR.
6	5	24	PSBAR NOT CONF	MP 531	CE does not have an SE available for its PSA.
6	5	25	PSA ALT	MP 531	'Go to Alt PSBAR' signal and 'Rem Alt' latch set.
6	5	26	SPLIT LOGOUT	MC 791	Invalid address or storage timeout detected during logout causes CE to step PSBAR to alternate and start new logout.
6	5	28	LOG ROS CHK	KU 231	ROS parity error detected during logout.
6	5	29	LOG ADDR CHK	MA 901	Address outside PSA detected on SAB during logout.
6	5	30	CE LOG REQ	KW 071	Logout request signal received from a CE.
6	5	31	RDD TO	KN 281	Data not available on direct control bus within prescribed time during read direct operation.
6	6	1–4	LOGOUT OR WRAP SELECTED STG ID	KU 041	Identify (binary) SE or DE selected during logout, wrap DE, or force DG request operation.
6	6	5–8	DG SELECTED	KU 061	Identify (binary) DG specified during wrap DE or force DG request operations.
6	6	10–15	CVG SELECTED	KU 071	Identify (numeric) CVG specified during wrap DE or force DG request operation.
6	6	16	REV NORM OP	KU 081	Reverse 'normal op'.
6	6	17	FORCE DG REQ	KU 081	Force DG request.
6	6	19	DIAG SE 1	KU 091	Blocks 'invalid address decoded' which is activated when SAB bit 8 = 1.

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
6	6	20	INV EXT PTY	KU 091	Invert P0–7 of external register.
6	6	21	RST CHKS	KU 091	Reset check register bits.
6	6	22	WRAP DE	KU 091	Wrap DE operation in progress.

2.1.6 Panel F

1. REPEAT switch. This switch causes the FLT or ROS test in storage to be repeated or allows searching for a particular test and repeating that test. The operation is as follows:
   a. REPEAT switch in REPEAT position and depression of START pushbutton will cause the FLT or ROS test in storage to be executed repeatedly.
   b. REPEAT switch in REPEAT position, test number in DATA switches (48–63), FLT tape rewound, and depression of STORE, then LOAD pushbuttons causes test number to be stored in T, FLT tape to be searched, and test to be loaded and executed repeatedly.
2. ROS/PROC/FLT switch. This switch provides two modes of testing. DISABLE INTERVAL TIMER switch must be in DISABLE position when running either test.
   a. FLT position: CE is conditioned for running FLTs.
   b. PROC (process) position: normal position for CE processing.
   c. ROS position: CE is conditioned for running ROS tests.
3. DEFEAT INTERLEAVING switch. This three-position lever switch performs the following functions:
   a. PROC position: Locations of consecutive doublewords are alternated between two basic storage modules (BSM) within an SE or a DE (interleave mode).
   b. No REV position: Locations of consecutive doublewords are within one BSM of an SE or a DE (defeat interleave mode).
   c. REV position: Locations of consecutive doublewords are within one BSM of an SE or a DE, and odd and even BSMs are interchanged.
4. INHIBIT CE HARD STOP switch. When this switch is set to INHIBIT CE HARD STOP position, conditions that cause the CE to enter hard-stop state are prevented from doing so.
5. DISABLE INTERVAL TIMER switch. When this switch is set to DISABLE INTERVAL TIMER position, the interval timer is not decremented.
6. STORAGE SELECT switch. This switch has three positions:
   a. MAIN: Main storage is selected for manually storing or displaying data.
   b. LOCAL: Local storage (LS) is selected for manually storing or displaying data.
   c. MAIN BYTE: Main storage is selected for manually storing or displaying data. The byte selected by ADDRESS switches 21–23 is the only byte affected by a manual store operation.
7. ADDRESS COMPARE switch. This switch has three positions:
   a. PROC: A sync pulse is available on a coaxial connector at the front of gate C whenever there is an equal compare between storage address bus and ADDRESS switches 9–28.
   b. STOP: The CE stops at the end of the instruction in progress whenever there is an equal compare between storage address bus and ADDRESS switches 9–28.
   c. LOOP: The CE branches to the address set in DATA switches 40–63 when there is an equal compare between storage address bus and ADDRESS switches 9–28.
8. CHECK CONTROL switch. This switch has three positions:
   a. PROC: The CE issues a pulsed element check upon detection of a failure. If the machine check mask bit, PSW bit 13, is on, logout of the CE occurs. If the machine check mask bit is off, processing continues, the check trigger is set, and the logout and machine check interruption is deferred until the PSW is loaded with bit 13 on.
   b. STOP: The CE is stopped upon detection of a failure. This stop occurs at the end of the cycle in which the check is detected and effectively freezes CE status. No logout occurs.
   c. DSBL: Upon detection of a failure, the appropriate check trigger is set but no stop, logout, or interruption occurs.
9. PULSE MODE. This switch provides a means of looping through a selected count of machine cycles starting at a selected address or when the interval timer is advanced. The starting address must be stored in bits 40 to 63 of location zero before beginning pulse mode. The operation is as follows:
   a. PROC: This is the normal position for CE processing.
   b. COUNT: The CE will proceed through a designated number of machine cycles, execute a system reset, and restart at the address in main storage location zero, bit positions 40–63. The cycle count is designated by the value set in DATA switches 53–63 and cannot be greater than 2047 (decimal).
   c. TIME: The CE will execute instructions until the interval timer advances (16 ms between advances), execute a system reset, and restart at the address in main storage location zero, bit positions 40–63.
10. REPEAT INSN switch. This switch provides a method of repeating a single instruction or a group of up to four halfword instructions. The operation is as follows:
    a. PROC: Normal instruction stepping is executed.

b. SINGLE: The instruction set in DATA switches, beginning with byte zero, is executed repeatedly.
c. MPLE: The group of instructions set in DATA switches 0–63 are executed repeatedly (looping through the four halfwords).

The contents of DATA switches 0–63 are loaded into Q (one time); branching instructions change the instruction counter but do not change Q.

11. ROS ADDRESS switch. This switch provides a means of stopping at a specific ROS address and of repeatedly reading and performing the functions of a specific ROS word. The operation is as follows:
    a. STOP: The CE stops when the ROS address specified by ADDRESS switches 8–19 is the same as the contents of ROSAR.
    b. PROC: This is the normal processing position.
    c. RPT: The CE continuously reads out and performs the functions of the ROS word specified by ADDRESS switches 8–19.
12. INDICATE RLR 1 POSITION 6 switch. This switch allows selection of either the L register or M register to be displayed on status roller 1, position 6.
13. FREQUENCY ALTERATION switch. This switch has two positions:
    a. DISABLE (normal position): Clock pulses are distributed from the oscillator to cause a 200-ns machine cycle.
    b. ENABLE: Clock pulses are distributed from the oscillator to cause a 195-ns machine cycle.
14. REGISTER SELECT switch. This switch directs the manual loading of PSBAR, CCR, or ATR upon depression of the REGISTER SET pushbutton.
15. RATE switch. The setting of the RATE switch indicates the manner in which instructions are to be performed. The four positions are:
    a. PROCESS: CE runs in normal processing mode.
    b. INSN STEP: CE fetches and executes a single instruction with each depression of START pushbutton.
    c. SINGLE CYCLE: CE executes a single machine cycle (one ROS cycle) with depression of START pushbutton, except that several cycles may be executed to prevent losing data from main storage.
    d. SINGLE CYCLE STORAGE INHIBIT: Same as SINGLE CYCLE except that all storage references are blocked.
16. START pushbutton. Depression of this pushbutton starts the operation defined by the RATE switch.
17. SYSTEM RESET pushbutton. Depression of this pushbutton initiates a subsystem reset which resets the CE and all IOCEs, SEs, and DEs configured to the issuing CE. It does not alter any CCRs.
18. LAMP TEST/ALLOW IND pushbutton. Depression of this pushbutton causes all indicators on the CE control panel to light with the exception of MARGIN, POWER STATUS, and roller indicators. When the CE hardstops during a logout, all the roller indicators are on. Depression of this pushbutton with this condition allows the roller indicators to display machine status.
19. CHECK RESET pushbutton. Depression of this pushbutton sets all CE check triggers to the non-error state.
20. PSW RESTART pushbutton. This pushbutton has two modes of operation:
    a. SYSTEM INTERLOCK switch off: Depression of PSW RESTART pushbutton causes the CE to issue a subsystem reset and load its PSW from the doubleword at main storage location 0.
    b. SYSTEM INTERLOCK switch on: Depression of PSW RESTART pushbutton causes the CE to issue a system reset, configure a subsystem according to the setting of MAIN STORAGE SELECT and LOAD UNIT switches, and load its PSW from the doubleword at main storage location 0.
21. REGISTER SET pushbutton. Depression of this pushbutton stores the data set in DATA switches into ATR, PSBAR, or CCR as selected by REGISTER SELECT switch setting.
22. ROS TRANSFER pushbutton. Depression of this pushbutton stores the address set in ADDRESS switches 8–19 into read-only storage address register (ROSAR).
23. SET IC pushbutton. Depression of this pushbutton stores the address set in ADDRESS switches 8–31 into IC and loads Q and R with instructions beginning with that address.
24. STORE pushbutton. This pushbutton has three modes of operation determined by the setting of STORAGE SELECT switch:
    a. MAIN: Depression of STORE pushbutton stores data set in DATA switches 0–63 into main storage location specified by the setting of ADDRESS switches 8–28.
    b. LOCAL: Depression of STORE pushbutton stores data set in DATA switches 32–63 into local storage location specified by the setting of ADDRESS switches 27–31.
    c. MAIN BYTE: Depression of STORE pushbutton stores one byte of data, selected by ADDRESS switches 29–31 from DATA switches 0–63, into main storage location specified by ADDRESS switches 8–31.
25. DISPLAY pushbutton. This pushbutton has three modes of operation determined by the setting of STORAGE SELECT switch:
    a. MAIN: Depression of DISPLAY pushbutton loads ST from main storage location specified by the setting of ADDRESS switches 8–28. This data is displayed in roller switch 1 position 3 and roller switch 2 position 3.

b. LOCAL: Depression of DISPLAY pushbutton loads T from local storage location specified by the setting of ADDRESS switches 27–31. This data is displayed in roller switch 2 position 3.
c. MAIN BYTE: This position has the same operation as MAIN position.

26. STOP pushbutton. Depression of this pushbutton causes the CE to enter the stopped state at the end of instruction execution.
27. BACKSPACE FLT pushbutton. Depression of this pushbutton causes the tape drive designated by LOAD UNIT switch setting to backspace tape one record.
28. LOG OUT pushbutton. Depression of this pushbutton causes the CE to perform a complete logout, identical with that which occurs when a check condition is detected, and take a machine check interrupt.

2.1.7 Panel G

1. POWER ON/OFF switch. This switch initiates power-on and power-off sequence for the CE.
2. SYSTEM INTERLOCK key switch. When this switch is operated to the ON position, all controls that are interlocked for states three and two are enabled (see Table 2-1); load and PSW restart operations are changed from subsystem to system functions.
3. POWER SEQUENCE COMPLETE indicator. This indicator is lit when all dc voltages are present in the CE.
4. MAIN STORAGE SELECT switch. Setting this switch specifies the PSA SE for a load or a PSW restart operation.
5. LOAD UNIT switches. Setting these three switches specifies the channel and I/O unit for a load operation.
6. INTERRUPT pushbutton. Depressing this pushbutton causes a request for an external interrupt.
7. SYSTEM indicator. This indicator is lit while the CE is not stopped and is not in wait state.
8. MANUAL indicator. This indicator is lit while the CE is stopped (executing the stop loop microprogram).
9. WAIT indicator. This indicator is lit while the CE is in wait state (PSW bit 14 set to 1).
10. TEST indicator. This indicator is lit while any of the following conditions exist (CE must be in a state that allows the condition to be effective):
    a. RATE switch is set to any position other than PROCESS.
    b. CHECK CONTROL switch is set to any position other than PROC.
    c. DISABLE INTERVAL TIMER switch is set to disable position.
    d. ADDRESS COMPARE switch is set to any position other than PROC.
    e. PULSE MODE switch is set to any position other than PROC.
    f. SCAN MODE (ROS/PROC/FLT) switch is set to any position other than PROC.
    g. REPEAT INSN switch is set to any position other than PROC.
    h. DEFEAT INTERLEAVING switch is set to any position other than PROC.
    i. ROS ADDRESS switch is set to any position other than PROC.
    j. Diagnose instruction is being executed.
    k. LAMP TEST pushbutton is depressed.
11. LOAD indicator. This indicator is lit while a load operation is being performed by the CE.
12. LOAD pushbutton. This pushbutton has two modes of operation:
    a. SYSTEM INTERLOCK switch off: Depression of LOAD pushbutton causes the CE to issue a subsystem reset, search for the PSA SE (beginning with ATR slot 1 and looking for the first configured SE), and read 24 bytes of data from the tape drive addressed with LOAD UNIT switch setting into main storage locations 0–23. The CE starts execution of the program by loading the current PSW from main storage location 0.
    b. SYSTEM INTERLOCK switch on: Depression of LOAD pushbutton causes the CE to issue a system reset, configure all elements of the system that are on-line into a subsystem, load ATR slot 1 with the value set in MAIN STORAGE SELECT switch, load physical PSBAR with the value in ATR slot 1, and read 24 bytes of data from the tape drive addressed with LOAD UNIT switch setting into main storage locations 0–23. The CE starts execution of the program by loading the current PSW from main storage location 0.

2.2 CE CONTROL PANEL OPERATING PROCEDURES

The following paragraphs describe operating procedures at the CE control panel which enable maintenance personnel to manually duplicate certain program operations and to exercise portions of the machine at a normal or reduced rate.

2.2.1 Turning On CE Power

1. MAIN LINE ON indicator must be lit, indicating that main line power is being supplied to the CE. If either THERMAL or POWER CHECK indicator is lit, the condition being indicated must be corrected before CE can be powered up.

2. Set POWER ON switch on CE power panel to POWER ON position.
3. Set POWER ON/OFF switch on CE control panel to ON position. CE will perform a power-up sequence and will light POWER SEQUENCE COMPLETE indicator when all voltages are present.

2.2.2 Turning Off CE Power

CE must be configured to state 0 and TEST switch set to TEST position for power-off switches to be effective.

1. If MANUAL light is not lit, depress STOP pushbutton.
2. Either one of two switches will start a power-down sequence. POWER ON/OFF switch on the CE control panel set to OFF position of POWER ON switch on CE power panel set to OFF position (down) will cause the CE to power down.

2.2.3 Stopping and Restarting the CE

The CE must be configured to state 1 or 0 to manually stop its operation. Depress STOP pushbutton. The CE will complete the instruction or I/O operation in progress and enter the stop microprogram loop. To restart the CE (from the point where it was stopped), depress START pushbutton.

2.2.4 Resetting CE Logic

SYSTEM RESET pushbutton provides a means of manually resetting CE logic and operates as follows:

1. CE must be in state 1 or 0.
2. If MANUAL indicator is not lit, depress STOP pushbutton.
3. Depress SYSTEM RESET pushbutton. The CE sets all control logic to inactive condition, resets all error-check logic, and returns to stopped state.

Initial program load, PSW restart, and power-on sequence operations include a reset of CE logic.

2.2.5 Resetting CE Error Check Logic

CHECK RESET pushbutton provides a means of manually setting all error-check logic in the CE to the non-error state and operates as follows:

1. CE must be in state 0.
2. Depress CHECK RESET pushbutton. The CE sets all error-check logic to non-error state. Processing may be continued by depressing START pushbutton; however, the results may be inaccurate.

2.2.6 Emergency Power Off

ELEMENT MPO PULL switch provides a means of powering down the CE when an emergency arises, such as fire or maintenance-personnel contact with high voltage. This switch is effective in all states and, when pulled, removes all power except battery power and 24V dc prime. Power down is immediate; the CE does not go on battery.

After the emergency situation is corrected, power may be restored to the CE as follows:

1. Set POWER ON/OFF switch to OFF position.
2. To obtain access to ELEMENT MPO PULL switch, open the right side cover of frame 02 and swing out gate E.
3. Reset ELEMENT MPO PULL switch by releasing latch on the switch and pressing against switch knob.
4. Set POWER ON/OFF switch to ON position to power up CE.

2.2.7 System IPL

1. Set SYSTEM INTERLOCK switch to ON position (insert key and turn key clockwise).
2. Set address of tape drive on which load tape is mounted into LOAD UNIT switches.
3. Set address of SE desired for PSA location into MAIN STORAGE SELECT switch.
4. Set all control switches to PROCESS position.
5. Depress LOAD pushbutton. The CE performs an initial program load operation as follows:
   a. All CE control logic is set to inactive condition.
   b. All CE error-check logic is set to non-error condition.
   c. Logical PSBAR is set to all 0's.
   d. ATR is set to all 0's.
   e. ATR slot 1 is set with the value set in MAIN STORAGE SELECT switch.
   f. Physical PSBAR is set with the value set in ATR slot 1.
   g. CCR bits 0–5 (state and SCON bits) are set to 1's; all other CCR bits are set to 0.
   h. DAR mask is set to all 0's.
   i. All elements in the system that are not off-line are configured into a subsystem as defined by LOAD UNIT switches and MAIN STORAGE SELECT switch.
   j. Twenty-four bytes of data are read from the load tape into main storage locations 0–23.
   k. Current PSW is loaded with data from main storage locations 0–7. Processing proceeds under control of current PSW.

2.2.8 Subsystem IPL

1. CE must be in state 1 or 0.
2. Set SYSTEM INTERLOCK switch to OFF position (key removed).

3. Set address of tape drive on which load tape is mounted into LOAD UNIT switches.
4. Set all control switches to PROCESS position.
5. Depress LOAD pushbutton. The CE performs an initial program load operation as follows:
   a. All CE control logic is set to inactive condition.
   b. All CE error-check logic is set to non-error condition.
   c. Logical PSBAR is set to all 0's.
   d. DAR mask is set to all 0's.
   e. ATR is searched, beginning with ATR slot 1, for a configured SE.
   f. Twenty-four bytes of data are read from the load tape into main storage locations 0–23.
   g. Current PSW is loaded with data from main storage locations 0–7. Processing proceeds under control of current PSW.

2.2.9 Manual Logout

1. CE must be in state 1 or 0 if SYSTEM INTERLOCK switch is set to OFF position.
2. CE must be in stopped state.
3. Depress LOG OUT pushbutton.

2.2.10 Display Current PSW

When the CE is in the wait or stopped state, all but two parts of the current PSW are displayed on roller 4, position 1. The two exceptions are: (1) the instruction address which is displayed in the D-register (roller 1, position 2) and (2) the instruction length code which is displayed in E-register positions 0 and 1 (roller 5, position 3).

2.2.11 System PSW Restart

1. Set SYSTEM INTERLOCK switch to ON position (insert key and turn key clockwise).
2. Set address of SE desired for PSA SE into MAIN STORAGE SELECT switch.
3. Set all control switches to PROCESS position.
4. Depress PSW RESTART pushbutton. The CE performs a PSW restart operation as follows:
   a. All CE control logic is set to inactive condition.
   b. All CE error-check logic is set to non-error condition.
   c. Logical PSBAR is set to all 0's.
   d. ATR is set to all 0's.
   e. ATR slot 1 is set with the value set in MAIN STORAGE SELECT switch.
   f. Physical PSBAR is set with the value set in ATR slot 1.
   g. CCR bits 0–5 (state and SCON bits) are set to 1's, and all other CCR bits are set to 0's.
   h. DAR mask is set to all 0's.
   i. All elements in the system that are not off-line are configured into a subsystem.
   j. Current PSW is loaded with data from main storage locations 0–7. Processing proceeds under control of current PSW.

2.2.12 Subsystem PSW Restart

1. CE must be in state 1 or 0.
2. Set SYSTEM INTERLOCK switch to OFF position (key removed).
3. Set all control switches to PROCESS position.
4. Depress PSW RESTART pushbutton. The CE performs a PSW restart operation as follows:
   a. All CE control logic is set to inactive condition.
   b. All CE error-check logic is set to non-error condition.
   c. Logical PSBAR is set to all 0's.
   d. ATR is searched, beginning with ATR slot 1 for a configured SE.
   e. Current PSW is loaded with data from main storage locations 0–7. Processing proceeds under control of current PSW.

2.2.13 Load Instruction Counter

The instruction counter (bits 40–63 of the current PSW) is always dynamically displayed by roller 6, position 3. To alter these bits without affecting the rest of the PSW:
1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.
2. Depress STOP pushbutton.
3. Set desired address into ADDRESS switches 8–31.
4. Depress SET IC pushbutton. (The contents of ADDRESS switches are loaded into the address field of the current PSW.)
5. Depress START pushbutton to resume processing.

2.2.14 Instruction Stepping

Instruction stepping enables the CE to process one instruction at a time, to service all interrupts, and to stop. Proceed as follows:
1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.
2. Depress STOP pushbutton.
3. Set RATE switch to INSN STEP.
4. Depress START pushbutton. The next instruction is processed, I/O operations are completed, and all pending interruptions are serviced. The program is run basically the same as during normal processing, except that the

CE returns to the stopped state when instruction execution is completed. The address of the next instruction to be processed is displayed in the instruction count portion of the PSW (D-register).
5. Repeat step 3 for each instruction step.

2.2.15 Display LS General Register

1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.
2. Depress STOP pushbutton.
3. Set STORAGE SELECT switch to LOCAL position.
4. Set ADDRESS switch 27 to center ("0") position.
5. Set ADDRESS switches 28–31 to binary address of general register to be displayed.
6. Depress DISPLAY pushbutton. The contents of the general register addressed are displayed in the T-register (roller 2, position 3). Any general register can be displayed by setting its address in ADDRESS switches 28–31 and depressing DISPLAY pushbutton.

2.2.16 Load LS General Register

1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.
2. Depress STOP pushbutton.
3. Set STORAGE SELECT switch to LOCAL position.
4. Set ADDRESS switch 27 to center ("0") position.
5. Set ADDRESS switches 28–31 to binary address of general register desired.
6. Set DATA switches 32–63 to generate the desired data.
7. Depress STORE pushbutton. The setting of DATA switches 32–63 is stored in the selected general register.

2.2.17 Display LS Floating-Point Register

1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.
2. Depress STOP pushbutton.
3. Set STORAGE SELECT switch to LOCAL position.
4. Set ADDRESS switch 27 to down ("1") position and ADDRESS switch 28 to center ("0") position.
5. Set ADDRESS switches 29–31 to binary address of floating-point register to be displayed.
6. Depress DISPLAY pushbutton. The contents of the floating-point register addressed are displayed in the T-register (roller 2, position 3). Any floating-point register may be displayed by setting its address in ADDRESS switches 29–31.

2.2.18 Load LS Floating-Point Register

1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.
2. Depress STOP pushbutton.
3. Set STORAGE SELECT switch to LOCAL position.
4. Set ADDRESS switch 27 to down ("1") position and ADDRESS switch 28 to center ("0") position.
5. Set ADDRESS switches 29–31 to binary address of first word in floating-point register to be loaded:

Floating-Point Register	Switches 29–31
0	000
2	010
4	100
6	110

6. Set first word of data to be loaded into DATA switches 32–63. (Place the exponent in byte 0.)
7. Depress STORE pushbutton. Desired data is stored into first word of selected register.
8. Set ADDRESS switches 29–31 to binary address of second word in floating-point register to be loaded:

Floating-Point Register	Switches 29–31
1	001
3	011
5	101
7	111

9. Set second word of data to be loaded into DATA switches 32–63.
10. Depress STORE pushbutton. Desired data is stored into second word of selected register.

2.2.19 Address-Compare Stop

This procedure compares the ADDRESS switch setting with the address sent to main storage. When the two are the same, the CE enters the stopped state.
1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.
2. Set ADDRESS switches 9–28 to the desired address.
3. Set ADDRESS COMPARE switch to STOP position.
4. To resume processing after an address compare stop, depress START pushbutton.

2.2.20 Display Doubleword from Main Storage (SE/DE)

To display any doubleword from main storage:
1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.

2. Depress STOP pushbutton.
3. Set ADDRESS switches 9–28 to desired doubleword address.
4. Set STORAGE SELECT switch to MAIN position.
5. Depress DISPLAY pushbutton. The contents of main storage doubleword location addressed are displayed in the ST and AB registers (position 3 of rollers 1–4).

Follow the above steps to display CAW or CCW:
1. CAW displayed in roller 1, position 3.
2. CCW displayed in position 3 of rollers 1 and 4.

2.2.21 Store Doubleword into Main Storage (SE/DE)

To store into any doubleword location in main storage:
1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.
2. Depress STOP pushbutton.
3. Set ADDRESS switches 9–28 to desired doubleword address.
4. Set STORAGE SELECT switch to MAIN position.
5. Set DATA switches 0–63 to generate desired data.
6. Depress STORE pushbutton.

Follow the above steps to store a new CAW or CCW:
1. CAW stored from DATA switches 0–31.
2. CCW stored from DATA switches 0–63.

2.2.22 Store Single Byte into Main Storage (SE/DE)

1. CE must be in state 1 or 0 or have SYSTEM INTERLOCK switch on.
2. Depress STOP pushbutton.
3. Set ADDRESS switches 9–31 to desired byte address.
4. Set STORAGE SELECT switch to MAIN BYTE position.
5. Set the byte of desired data into its correct position within the doubleword of DATA switches 0–63.
6. Depress STORE pushbutton.

2.2.23 Clear Main Storage Procedure

The following procedure may be used to clear (ripple) main storage of a subsystem as well as general-purpose and floating-point registers in local storage of a CE. CE must be in state 0.

1. Depress STOP pushbutton.
2. Place TEST switch in TEST position.
3. Place REGISTER SELECT rotary switch in ATR position.
4. Set DATA switches as follows:
   a. If the subsystem includes an SE, set DATA switches 0–3 to select SE.
   b. If the subsystem includes an SE and a DE, set DATA switches 0–19 to select SE, repeated five times, and set DATA switches 20–23 to select DE. This results in rippling the SE five times for each time the DE is rippled, but it does not cause error conditions. An optional procedure is to set DATA switches 0–3 to select SE and DATA switches 4–7 to select DE. This allows DE to ripple but causes SAR checks during ripple of second half of DE addresses.
   c. If the subsystem main storage consists of only one DE, set DATA switches 0–3 to select DE. SAR checks occur during ripple of second half of DE addresses.
5. Depress REGISTER SET pushbutton.
6. Place REGISTER SELECT rotary switch in PSBAR position.
7. Depress REGISTER SET pushbutton.
8. Place REGISTER SELECT rotary switch in PROCESS position.
9. If the subsystem includes an SE, proceed to step 10. If the subsystem does not include an SE, remove card at CE location 02A-C3F7 and jumper pin at location 02A-B3 B3 D12 to ground.
10. Set ADDRESS switches 8, 21, and 22 to down ("1") position and all other ADDRESS switches to center ("0") position. Address switches 21 and 22 cause writing into storage; if they are set to "0" position, storage may be rippled in a Read Only mode.
11. Set STORAGE SELECT rotary switch to MAIN position.
12. Set DATA switches 0–63 to "0" position.
13. Depress ROS TRANSFER pushbutton. Observe that D-register (roller 1, position 2) is stepping through all storage addresses. DATA switch setting is continuously being stored throughout the SE or DE.
14. Set STORAGE SELECT rotary switch to local; D-register stops stepping.
15. Set STORAGE SELECT rotary switch to MAIN position.
16. Depress SYSTEM RESET pushbutton.
17. If card was removed and jumper was installed as described in step 9, replace card and remove jumper.

2.2.24 Tape Drive Rewind Procedure

To cause a tape to rewind:
1. Set TEST switch to TEST.
2. Set SCAN MODE switch to FLT.

3. Set LOAD UNIT switches to address tape drive.
4. Depress FLT BACKSPACE and CHECK RESET push-buttons at the same time.

2.2.25 FLT Operating Procedure

Refer to LADS page A6503 for FLT operating procedure.

2.2.26 Requesting a Maintenance Subsystem

The operating ATC system can configure a maintenance subsystem. To obtain a maintenance subsystem, request operating personnel to initiate a reconfiguration procedure. Heading 4.5.1 contains a procedure for manual configuration of a subsystem.

The preventive maintenance schedule (Table 3-1) provides a checkout routine designed to keep the CE performance at original specifications. Several of these procedures permit anticipation of a failure for some of the critical circuits, providing ample warning for replacement planning. The accuracy of these predictions depends upon the frequency with which the checkout procedure is run. The frequency and thoroughness of each procedure should be increased if warranted by the conditions.

Table 3-1. Preventive Maintenance Schedule

Item	Procedure	Freq (wks)
Diagnostics	Heading 4.5	4
Marginal Checks*:	Heading 5.2	
ROS Tests and FLTs	Headings 4.3 and 4.4	4
Diagnostics	Heading 4.5	4
SEVA	Heading 4.5	13
Clock Timing and Distribution	Heading 4.6	26
ROS Checks:		
Optimization	Heading 4.9	26
Bit-plane pressure	Heading 4.13	26
Power:		
Visual checks and cleaning	Heading 5.1	26
Voltage checks	Heading 5.3	13
OV/OC checks	Heading 5.3.2	26
Thermal checks	Heading 5.4.1.3	26
Battery pack test	Heading 5.10	13
Miscellaneous:		
Lamp test	Heading 4.7	2
Blowers and filters	Check filters for accumulation of dust; vacuum or replace filters when necessary. Check for proper air flow through the blowers; it should be sufficient to hold a piece of punch-card stock against the air intake area of the blower assembly.	4
Visual inspection	Check for loose screws, bolts, nuts, and hardware; cable wear, evidence of overheating; and broken or loose connections. Check for loose or improperly adjusted cover hardware.	26
Manual controls	Verify operation of manual controls and switches. Clean switch contacts where necessary.	26
Cleaning	Vacuum and dust inside the CE. Check air flow paths.	52

*These checks consist of running tests under bias.

This chapter encompasses all procedures for trouble-shooting and checkout with the exception of power. All procedures relating to power are in 9020 D/E Power Controls and Distribution Manual.

SECTION 1. SERVICE CHECKS AND REPAIR PROCEDURES

4.1 MAIN STORAGE RIPPLE TESTS

4.1.1 Write All 1's

CE must be in state 0.

1. Depress STOP pushbutton.
2. Set TEST switch to TEST.
3. Set REGISTER SELECT switch to ATR.
4. Set DATA switches as follows:
   a. If the subsystem includes an SE, set DATA switches 0–3 to select SE.
   b. If the subsystem includes an SE and a DE, set DATA switches 0–19 to select SE, repeated five times, and DATA switches 20–23 to select DE. This results in rippling the SE five times for each time the DE is rippled, but does not cause error conditions. An optional procedure is to set DATA switches 0–3 to select SE and DATA switches 4–7 to select DE. This allows DE to ripple but causes SAR checks during ripple of second half of DE addresses.
   c. If the subsystem main storage consists of only one DE, set DATA switches 0–3 to select DE. SAR checks occur during ripple of second half of DE addresses.
5. Depress REGISTER SET pushbutton.
6. Set REGISTER SELECT switch to PSBAR.
7. Depress REGISTER SET pushbutton.
8. Set REGISTER SELECT switch to PROCESS.
9. If the subsystem includes an SE, proceed to step 10. If the subsystem does not include an SE, remove card at CE location 02A-C3F7 and jumper pin at location 02A-B3 B3 D12 to ground.
10. Set ADDRESS switches 8, 29, and 30 to down ("1") position and all other ADDRESS switches to center ("0") position. X"800006"
11. Set STORAGE SELECT switch to MAIN.
12. Set DATA switches 0–63 to 1.
13. Depress ROS TRANSFER pushbutton. Observe that D-register (roller 1, position 2) is stepping through all storage addresses.
14. Run at nominal voltage for 1/2 minute.
15. To stop test, set STORAGE SELECT switch to LOCAL.
16. Depress SYSTEM RESET pushbutton.
17. If card was removed and jumper installed in step 9, replace card and remove jumper.

4.1.2 Read All 1's

CE must be in state 0.

1. Perform steps 1–9 in heading 4.1.1.
2. Set ADDRESS switch 8 to 1. Set all other ADDRESS switches to 0. X"800000"
3. Set CHECK CONTROL switch to STOP.
4. Depress ROS TRANSFER pushbutton.
5. Run at nominal voltage for 1/2 minute.
6. To stop test, set STORAGE SELECT switch to LOCAL.
7. Depress SYSTEM RESET pushbutton.
8. If card was removed and jumper installed in step 9, replace card and remove jumper.

4.1.3 Write/Read All 0's

Perform procedures under headings 4.1.1 and 4.1.2 with DATA switches set to 0.

4.1.4 Write/Read Alternate Pattern

1. Repeat procedures under 4.1.1 and 4.1.2, with each byte of DATA switches set to 10101010 (AA in hex).
2. Repeat procedures under 4.1.1 and 4.1.2, with each byte of DATA switches set to 01010101 (55 in hex).

4.1.5 No Parity Bit Pattern

Repeat procedures under 4.1.1 and 4.1.2, with each byte of DATA switches set to 00000001 (01 in hex). This test will determine whether the parity bit for all storage addresses can be reset. In all previous tests, the parity bit is set.

4.2 LOCAL STORE RIPPLE TESTS

4.2.1 Write All 1's

1. Set ADDRESS switches 8, 29, and 30 to 1's.
2. Set DATA switches 32–63 to 1's.
3. Set STORAGE SELECT switch to LOCAL.
4. Set RATE switch to PROCESS.
5. Depress ROS TRANSFER.
6. Run at nominal voltage for 15 seconds.
7. To stop test, depress SYSTEM RESET.

4.2.2 Read All 1's

1. Set ADDRESS key 8 to 1. Set all other ADDRESS keys to 0.
2. Set CHECK CONTROL switch to STOP.
3. Depress ROS TRANSFER.
4. Run at nominal voltage for 15 seconds.
5. To stop test, depress SYSTEM RESET.

4.2.3 Write/Read All 0's

Repeat procedures under 4.2.1 and 4.2.2, with DATA switches 32–63 set to 0.

4.2.4 Write/Read Alternate Pattern

1. Repeat procedures under 4.2.1 and 4.2.2, with DATA switches 32–63 set to 10101010 in bytes 4, 5, 6, and 7.
2. Repeat procedures under 4.2.1 and 4.2.2, with DATA switches 32–63 set to 01010101 in bytes 4, 5, 6, and 7.

4.2.5 No Parity Bit Pattern

Repeat procedures under 4.1.5, making sure that the STORAGE SELECT switch is in LOCAL.

4.3 ROS TESTS

The ROS tests are explained in Chapter 4 of CE Theory of Operation. Operating procedures are found on LADS page A6503.

The ROS tests provide a thorough check of the ROS bit plane portion of the CE. These tests do not require the execution of a program; special hardware (hardcore) is used to run portions of the tests. This hardcore is tested first to ensure that hardware testing can proceed properly. To provide background information for troubleshooting, a discussion of ROS parity checking follows.

4.3.1 ROS Parity Checking

The ROS word is divided into four groups: bits 0–1, 2–42, 43–68, and 69–99. Bit 0–1 are ignored and are not parity-checked. The remaining three groups are parity-checked independently. Bit 20 is the parity bit for bits 2–42; bit 85, for bits 43–68; and bit 91, for bits 69–99.

If a parity error is detected, the reset to the part of the data register or indicator backup latches containing the failing group is blocked. The new data is not gated into this group. The group or groups not in error are reset and have their part of the next ROS word gated in. For example, if bit 87 fails, the reset to bits 69–99 is blocked. The other two groups, bits 6–42 and 43–68, receive their portion of the next ROS word.

The group in error may be determined by observing roller switch 2, position 2, the first three of the last five indicators (ROS PTY: 6–42, 48–68, and 69–99). The indicator(s) that is on indicates the failing group(s). The failing bit(s) may be identified by comparing the indicated bits of the failing group (roller switches 2, 3, and 4, position 4) with the bits listed in the ROS address list (QZ logic) for that ROS word.

The address of the failing ROS word may be found in the indicated Previous ROS Address Register (PROSAR). [Roller switch 3, position 4, the previous address indicator (PREV ADR A), provides the register indication. If the indicator is on, use PROSARA register; if off, use PROSARB register.] The alternate PROSAR contains the address of the word that accessed the failing word. ROSAR contains the address of the next word. A ROS parity error prevents these registers from advancing from this state. The registers are indicated by roller switch 1, position 4.

4.3.2 ROS All 0's, All 1's Word Tests

Stored in ROS are four words that may be used to check the ROS sense amplifiers, sense latches, data registers, and indicators. Two words contain all 0's except for the three parity bits. The other two words contain all 1's except bit 91 (parity 69–99). All four words have correct parity. To use these words, proceed as follows:

1. Depress SYSTEM RESET.
2. Set CHECK CONTROL switch to STOP.
3. Set REPEAT ROS ADDRESS switch.
4. Set roller switches 2, 3, and 4 to position 4.
5. Set address F02 (hex) in ADDRESS switches 8–19.
6. Depress ROS TRANSFER.
7. Observe indicators of rollers 2, 3, and 4; all indicators should be off except the three parity bits.
8. Depress SYSTEM RESET.
9. Repeat steps 5–8, using address F03.
10. Set address F00 (hex) in ADDRESS switches 8–19.
11. Depress ROS TRANSFER.
12. Observe indicators of rollers 2, 3, and 4; all indicators should be on except bit 91.
13. Depress SYSTEM RESET.
14. Repeat steps 10–13, using address F01.

Incorrect indications unique to one word may be due to bit plane, sense amplifier, or sense latch failures. Incorrect indications common to F00 and F01 or common to F02 and F03 may be due to sense latch, data register, or indicator failures.

4.3.3 ROS Word Tests

The ROS word tests check the ROS hardcore and each bit of each ROS word. Each ROS word bit is checked by comparing it with an expected value for it. The expected value used for the comparison is obtained from the manufacturing interface tape from which the ROS bit planes are manufactured. To perform the comparison, the ROS address is loaded into ROSAR by way of S. Each address is used repetitively until each bit in the ROS word is checked. If there is no comparison, the test stops with the failing bit and its address displayed on the system control panel.

The operating procedure for the ROS tests using the ROS test tape is found on LADS page A6503. If an error is encountered during steps 1–8, proceed in accordance with heading 4.3.4. If an error is encountered during steps 9–11, refer to heading 4.3.5 for additional information and proceed in accordance with 4.3.6.

4.3.4 ROS Hardcore Repair

This repair procedure consists of a series of observations and tests to locate a failure in the ROS hardcore. The correct operation of the hardcore is necessary for successful testing of the ROS word bits.

If any of the following failures occur, proceed as directed:

1. Failure to store 1's successfully in ST. This failure may be identified by inspecting the indicators (roller switches 1 and 2, position 3).
   a. Check that SCAN MODE switch is set to ROS; if it is not, set it, and restart the tests.
   b. Trace the failing bit(s), using logic, and repair.
2. Failure to complete IPL (first depression of LOAD). This failure may be identified by not finding the indications specified in the test procedure (LADS page A6503) or by the LOAD indicator (panel G) or TIMING GATE indicator (roller switch 4, position 5) remaining on.
   a. Check for the following:
      (1) LOAD UNIT switches are set to the correct channel and I/O unit address.
      (2) CE CHECK Control switch is set to DSBL.
      (3) I/O unit is ready and not in Test mode.
      (4) MAIN STORAGE SELECT switch is set to PSA SE.
   b. Depress SYSTEM RESET and BACKSPACE FLT. BACK SPACE indicator (roller 3, position 1) should not come on; GAP indicator (roller 3, position 1) should come on. If BACK SPACE flashes, the tape is not at load point. If it stays on, the IOCE has a malfunction (press reset on IOCE console) or the subsystem is not properly configured.
   c. Inspect storage location 0–38 (hex) for correct IPL data. Compare display data with data specified on LADS page A6511.
   d. If tape runs away, a failure of the test number compare operation is indicated. Either the test is not being performed at all or it is not successful. Depress BACK SPACE to stop runaway tape (will not change indications in the CE), and use the following procedure to isolate the trouble:
      (1) Clear main storage.
      (2) Store all ones in 100 and 200 of main storage. This will set up the buffers to scan in all bits to S and T.
      (3) Store FF FF FF FF 03 00 00 00 (hex) at main storage locations 108 and 208.
      (4) Jumper 02E-B3G7B10 to D08 ground (KU291 TIC LTH).
      (5) Set the following switches:
          CHECK CONTROL to DSBL.
          SCAN MODE to FLT with REPEAT on.
      (6) Set up ROS address 33F in ROS ADDRESS COMPARE switches and depress ROS TRANSFER.

(7) If the pass trigger comes on, the test number compare is functioning correctly. The trouble must be something which prevents the test from being performed e.g., a missing TIC pulse.

(8) If the fail trigger comes on, a missing bit from either S or T is indicated. Sync on ROS address 150 while observing 'Scan out S + T' for reference. Scope 'PAL=0' which should be active during 'Scan out S + T'. Scope back to the failing bit.

3. Storage check. This failure may be identified by the FLT STG ERR indicator (roller 5, position 2) being on. Use the ripple tests (heading 4.1) with CHECK CONTROL switch set to STOP to locate the failing address.
4. Failure to stop with the specified indications after each depression of LOAD. The indications are listed on LADS page A6503. (Tape must continue running.) This failure is caused by the inability to make test number comparison. The expected condition is all 1's in S and a 0 result from PAL. Use the following procedure to isolate the failure:
   a. Disable interval timer.
   b. Set CHECK Control switch to DSBL.
   c. Add the following jumpers to ground:
      (1) 02B-C2G4B10 ('Enable scan bypass' signal on ALD AP821).
      (2) 02E-B3F6D07 ('Scan Out ST' on KU491).
   d. Depress SYSTEM RESET.
   e. With the data switches all up, depress STORE. Verify that S and T contain all 0's. PAL (32–63) should contain all 1's (roller 6, position 1).
   f. Depress DATA switches 0–31 and depress STORE. Verify that S contains all 1's and that both T and PAL contain all 0's (except parity bits).

      Note: While in the stop loop, ROS address B8A (and 893 if IC (21, 22) = 11) will be gating IC and a constant through the adder. This may cause some indicators to glow dimly and may generate a pulse at the output of the zero-detection circuits. To prevent confusion in steps f and g, eliminate these indications by setting all ADDRESS switches to zero and depressing SET IC.

   g. Return DATA switches 0–31 to up position and depress DATA switches 32–63. Depress STORE and verify that S contains all 0's and T contains all 1's. PAL should again contain all 0's.
   h. During steps f and g, the output of the zero-detection circuits should indicate a zero result. This may be verified by checking 02E-B3C6D07 for a minus level (net AZ4 on logic KU311).
   i. If correct indications are not obtained, check zero-detection circuitry. Figure 4-1 shows a representative bit position in the circuitry used for test number and result comparisons in ROS word tests and FLTs. Note that a bit in S (roller 1) or its corresponding bit position in T (roller 2) will result in a zero output from PAL. PAL is set to 1 only if S and T both contain 0 in that position. Also note that indicators are numbered 0 to 35; e.g., S(31) and T(63) are roller bit 35.
   j. Remove ground jumpers and return switches to normal.
5. Hardcore error stop. See LADS page A6511.

4.3.5 ROS Hardware Tests

The ROS hardware tests provide for the isolation and repair of a failing ROS bit or bits if the failure is in the ROS hardware (up to and including the sense latches). To aid in understanding the adjustments and restrictions of ROS, the following background information is provided.

The ROS uses the capacitive coupling between a drive line and a differential sense line pair to generate a signal. The nominal signal level from a sense line pair is on the order of 1 mv. To amplify this low-level signal to SLT levels, a sense amplifier is used; a clipping network squares the signal and limits the amplitude.

The sense amplifier is essentially two differential amplifiers, a linear amplifier, and a clipping network. Each amplifier differentially senses the signal from comparable sense line pairs on each gate (C and D). The two differential amplifiers are then dot-ORed into the linear amplifier. (Since only one side of one gate is driven at a time, only one of the two differential amplifiers senses a signal.) The output of the linear amplifier is then fed through the clipping network to the sense latch. Figure 4-2, A, shows a typical 1 and 0 at the output of the sense amplifier (after clipping). Reference time T_0 may be found at location 02C-E3A2D06. Note that the output is always a bipolar signal; the difference between a 1 and a 0 is the sequence in which the positive and negative voltage swings occur. A 1 is first positive, then negative; a 0, negative, then positive. (The initial voltage swing is called the "signal"; the following kickback, the "recovery.")

When observing a string of 1's and 0's while in a particular loop (e.g., the stop loop), the 1's may be distinguished from the 0's by looking at the fall time of the positive voltage swing. A 1 has a sharp rise and fall; a 0 has a sharp rise and a slower fall. See Figure 4-2, A and B.

The drive line is driven by a transistor in a 1408 transistor array drive matrix, 88 transistors per bit plane. One side of the matrix (the base of the transistors) is driven by 22 'select bus base drive' (SBBD) signals, common to all bit planes. The other side of the matrix (the emitter of the transistors) is driven by 64 'select bus emitter drive' (SBED) signals, four per bit plane. The transistor in the matrix at the intersection of the active SBBD and SBED signals drives the selected drive line. To prevent more than one transistor from being gated on in each cycle, the SBBD precedes the SBED signal. See Figure 4-2, C and D.

4.3.6 ROS Hardware Repair

With the preceding background information in mind, the results of the ROS tests may be properly interpreted. The following discussion provides techniques for ROS hardware tests. The procedure on LADS page A6503, steps 9–11, is used to run the tests and to set up scoping loops when failures occur. Additional troubleshooting techniques and procedures, not based on the ROS tests, have been included in this discussion where they have been found to be of value to maintenance personnel.

A flowchart for ROS troubleshooting is given in the Diagnostic Techniques section of the 7201-02 FEMDM. ROS timing information is found on LADS page A8004. A chart of sense amplifier and sense latch locations is provided on logic page EF501. Refer to heading 4.9 for strobe timing and bias optimizing procedure.

4.3.6.1 Weak Sense Amplifier Output

A low or weak signal that appears with slow transitions and low amplitudes (Figure 4-2, E) may be caused by low torque on the pressure plates, dirt on the bit plane, or a poor drive signal.

Whenever a poor 1 or 0 is found, the first requirement is to substitute another sense amplifier card to be sure the card is not at fault. The card used, PN 5801524, has four amplifier channels on it.

On a few occasions, poor sense amplifier operation has been traced to a missing -18V bias voltage. This causes the sense amplifier to behave as if it were biased at -7V. The bits appear much wider than normal. Check for poor solder connections to voltage buses and for loose voltage connectors.

If the weak output is a result of low torque, the torque should be corrected, using the procedure under heading 4.13.3. Contamination on the bit plane may be sufficient to increase the distance between the drive line tabs and the sense lines causing reduced output. If this is the case, the bit plane must be cleaned. The procedure for this is under heading 4.13.2.

A slow or low array drive transistor output results in reduced sense amplifier output. Figure 4-2, G, shows this condition.

4.3.6.2 Distorted or Missing Sense Amplifier Output

A distorted or missing bit (Figure 4-2, F) may be caused by either an open or a short circuit. Either the sense line or the drive line could be open. If the drive line is open, the output of the driver transistor will appear as shown in Figure 4-2, H.

Possible shorted conditions are: a sense line shorted to ground, to an adjacent sense line, or to a drive line. A sense line to drive line short is the most probable. A detailed troubleshooting procedure for this condition follows.

The sense lines are isolated from the bit plane drive lines by a sheet of 1 mil Mylar*. If this sheet is punctured or has a piece of conductive material embedded in it, a short may occur. When this happens, failures can occur in all bit planes but will be limited to one bit position in either the upper or lower word (assuming only one puncture).

If a solid short exists, the input to the sense amplifier will be at approximately 6V. This can be scoped with the machine in SINGLE CYCLE after depressing START.

An alternative procedure, which allows a complete check for leakage between drive lines and sense lines or ground, is as follows:

1. Remove pressure bar from bottom of bit plane without removing pressure from pressure plates. This exposes the overlapped area of the bit plane tabs and the drive line tabs.
2. A red wire supplying +6V is connected to each edge of the drive line area of the bit plane. Isolate these +6V tabs from their mating bit plane tabs by slipping a small piece of insulating material between them. A piece of punch card stock can be used.

   CAUTION

   Be very careful not to damage the bit plane when inserting the insulator.

3. Check for infinite resistance between drive lines and ground. This is best done by connecting an ohmmeter across small bypass capacitor at top of plane. There are two capacitors, one for each half of the plane. Both must be checked. Connect + meter lead to + side of capacitor. The resistance should become infinite after 30 to 45 seconds when capacitor has fully charged.
4. If reading is infinite, proceed to next plane and repeat steps 1 through 3 above. Continue until all planes are checked or defective plane is located. If a short is indicated, proceed to step 5.

*Trademark of E. I. du Pont de Nemours & Co. (Inc.)

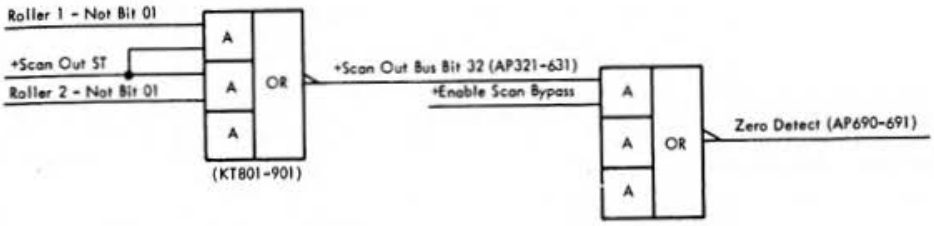
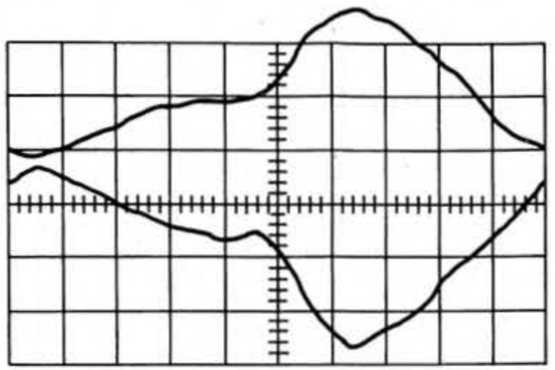


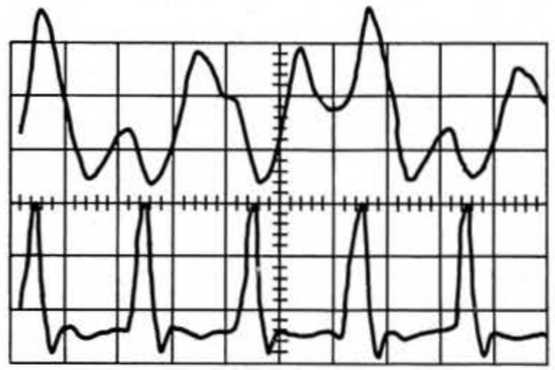
Figure 4-1. Test Number Comparison Circuit



20ns/div; .5v/div.

Top Trace = 1 Bit
Bottom Trace = 0 Bit

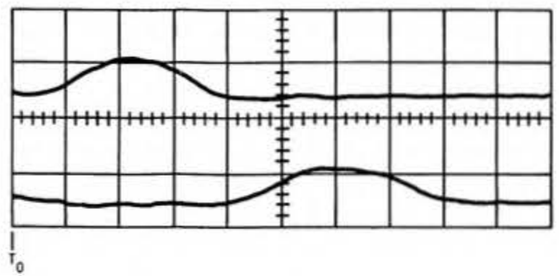
(A) Sense Amplifier Output, Typical 1 and 0



20ns/div; .5v/div.

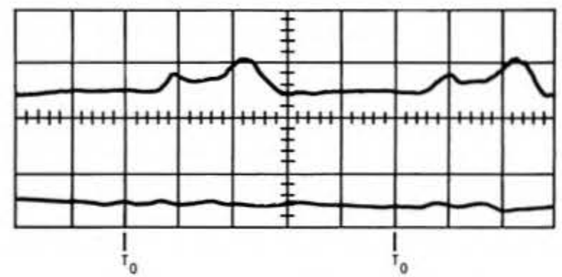
Top Trace = Bit Pattern (10010)
Bottom Trace = Strobe

(B) Sense Amplifier Output, Five Cycles



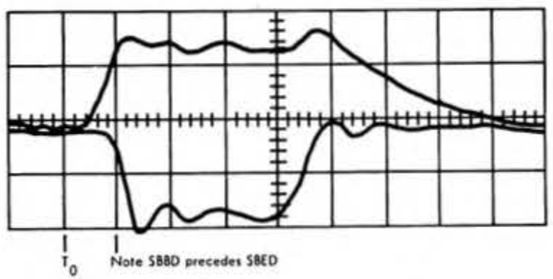
Upper waveshape: Weak 1
Lower waveshape: Weak 0
Scope settings:
V 1v/cm
H 20ns/cm

(E) Sense Amplifier Output, Weak 1 and 0



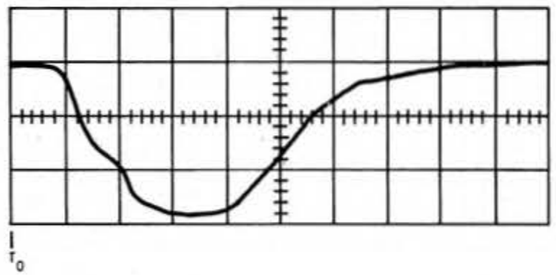
Upper waveshape: Distorted Bit
Lower waveshape: No Bit (Select Noise Present)
Scope settings:
V 1v/cm
H 40ns/cm

(F) Sense Amplifier Output, Distorted Bit



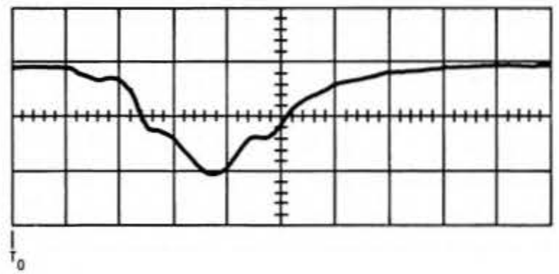
Upper waveshape: Typical SBBD
Lower waveshape: Typical SBED
Scope settings:
V 2v/cm
H 20ns/cm

(C) Signals to Array Drive Transistor



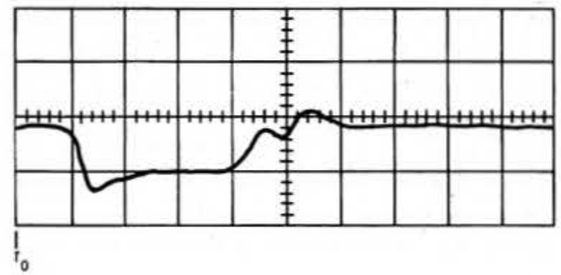
Scope settings:
V 2v/cm
H 20ns/cm

(D) Typical Array Drive Transistor Output



Scope settings:
V 2v/cm
H 20ns/cm

(G) Slow or Low Array Drive Transistor Output



Scope settings:
V 2v/cm
H 20ns/cm

(H) Array Drive Transistor with Open Drive Line

Figure 4-2. ROS Signals

5. Relax pressure on pressure plates one at a time. Meter should show a higher resistance when pressure is reduced near defect.

   Note: If the resistance does not change when the pressure plates are relaxed, examine the cabling from the 1/3 boards to the array. The short could also be in this area.

6. Remove defective plane using procedure under heading 4.13.1. Inspect area indicated by failing bit position and pressure plate that affected resistance reading. If a piece of foreign material is found, carefully remove it. If a hole is found, check for a burr or foreign substance on sense plate, which might have caused hole. A new bit plane must be ordered to replace any found not to have complete isolation from sense lines. Use steps 1 through 3 to verify condition of new bit plane when it is installed.
7. A temporary repair may be made while awaiting parts by using a piece of plastic wrap or transparent wrapper from a cigarette package as an insulator. This additional thickness of insulating material will reduce the output from that plane, however. Often a defective bit plane will work for a time after having been removed and reinstalled. This should not be considered a permanent repair.

If unable to isolate the cause of a distorted or missing bit using the preceding procedure, one of the less probable short or open conditions exists. The trouble may often be isolated by checking physically adjacent locations for signs of distortion. An example is shown in Figure 4-3. Assume that bit 87U is distorted. Bit 87L is normal but bit 86L shows distortion. A short probably exists between bits 87U and 86L.

A complete resistance check of the ROS array may be made which will isolate any of the possible short or open conditions. Proceed as follows:

1. Remove the following from the area of concern:
   a. Sense amplifier cards.
   b. Driver cards.
   c. Bus-to-board voltage jumpers.
   d. Select cables.
2. Make resistance readings between points indicated in the table of Figure 4-3.
3. Isolate the trouble and make the repair.

4.3.6.3 Extra or Missing Bits

Extra (picked) or missing (dropped) bits can result from electrical noise, late ROS branching, or multiple drive line selection. Most of these problems will be intermittent. To determine which is the most probable cause, refer to 4.3.6.5.

4.3.6.3.1 Electrical Noise. Noise problems are usually characterized by intermittent extra or missing bits and by failure of the ROS unit to operate error-free to the full -7V bias limit. Possible sources of electrical noise include: poor cable dress within the ROS unit; ground loops within the system; and defective switches, capacitors, and cooling fan motors. A troubleshooting procedure is given in 4.3.6.3.2.

Cable dress within the ROS unit is critical. Due to the high gain in the sense amplifiers, any noise picked up during strobe time is set into the latches as a bit. It is therefore imperative that all cables be carefully routed to minimize noise coupling and pickup. Figure 4-4 shows the cable dressing in a typical E1 board. Note how the shielded input cables are placed to act as a shield between the input and output pins of the sense amplifiers; also note that the individual leads are placed down between the pins. Figure 4-5 shows the cable routing between the E1, E2, and E3 boards. No significant departure from the routing shown should be made; the exposure to noise cannot be tolerated.

Noise can also result from ground loops within the system. To prevent ground loops, the ROS frame, including the spiders, is electrically isolated from the machine frame except for the single connection through ROS dc return line to the common ground in frame 01. (ROS frame is connected to ROS dc return line.) If extraneous signals to frame grounds are present, they must be removed (see heading 4.8).

Another source of noise may be open capacitors in the voltage crossovers on gate C, boards E1 and E2. The capacitors are needed only on the E1 and E2 boards.

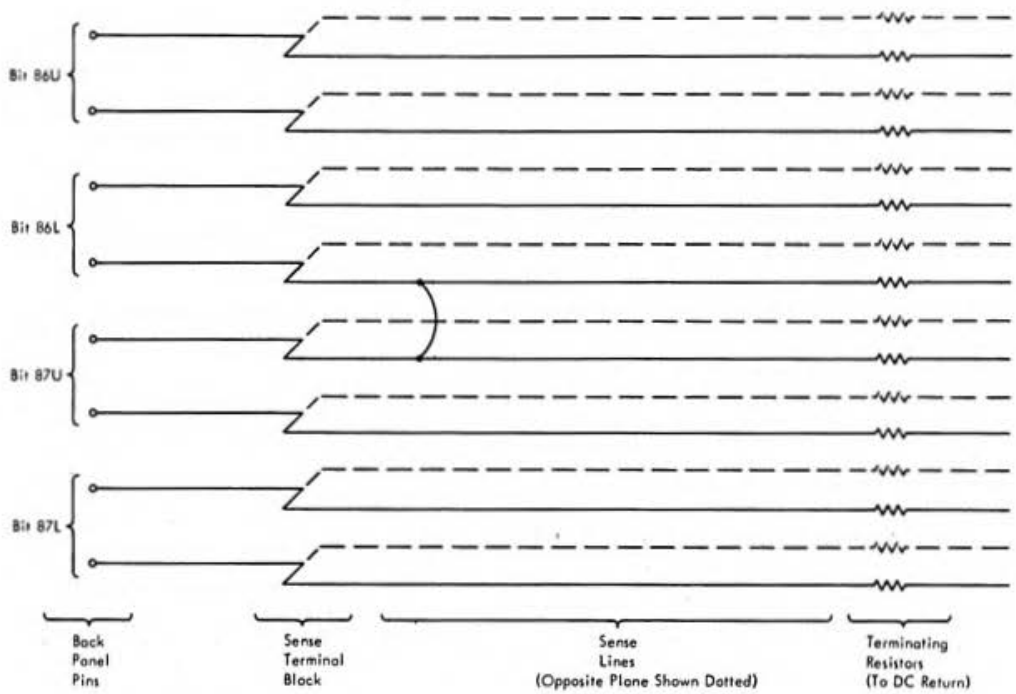
The susceptibility of the ROS unit to noise can be minimized by adjusting the strobe accurately. The following criteria should be met:

1. ROS strobe width, measured at the sense amplifier, should not exceed 30 ns at 50% amplitude. Strobe width as low as 20 ns is acceptable if the ROS bias limits can be reached. Since the strobes are generated by many drive signals, several sense amplifiers should be checked for minimum width.
2. ROS strobe timing should fall in the center of a no-bit (negative) pulse. A bit position in the center of the plane should be used for this measurement. Measured at 50% amplitude, the no-bit pulse should overlap the strobe pulse by 8 ns on rise and fall.

Note: Noise problems are intensified by low humidity. The recommended humidity for proper operation is 45 to 50%.

4.3.6.3.2 Troubleshooting Noise Problems. The following procedure should be used in troubleshooting noise problems:

1. Stop ROS clock by setting RATE switch to SINGLE CYCLE.
2. Depress START. The sense amplifiers are now gated.



Should an open or a short occur, check the indicated areas (a short from bit 86L to 87U is indicated here).

Resistance Readings *

Condition	From Sense Amp Input to	Resistance
Normal	DC return. Any other sense amp input. Any drive line.	16.5 ohms 33.0 ohms Open
Sense - sense line short	DC return. Input of sense amp to which it is shorted. Any other sense amp input. Any drive line.	8.25 ohms 0 ohm 24.75 ohms Open
Sense - DC return short	DC return. Any other sense amp input. Any drive line.	0 ohm 16.5 ohms Open
Sense - drive line short	DC return. Drive line to which it is shorted. Any drive line in same or opposite plane, except line to which it is shorted. Any drive line not in same or opposite plane.	16.5 ohms 0 ohm ** 200 ohms plus short resistance Open

* Remove sense amp and array drive cards and voltage jumpers in 1/3 boards.
** 0 ohm if dead short, may be a high impedance.

Figure 4-3. Sense Amplifier Input Resistances

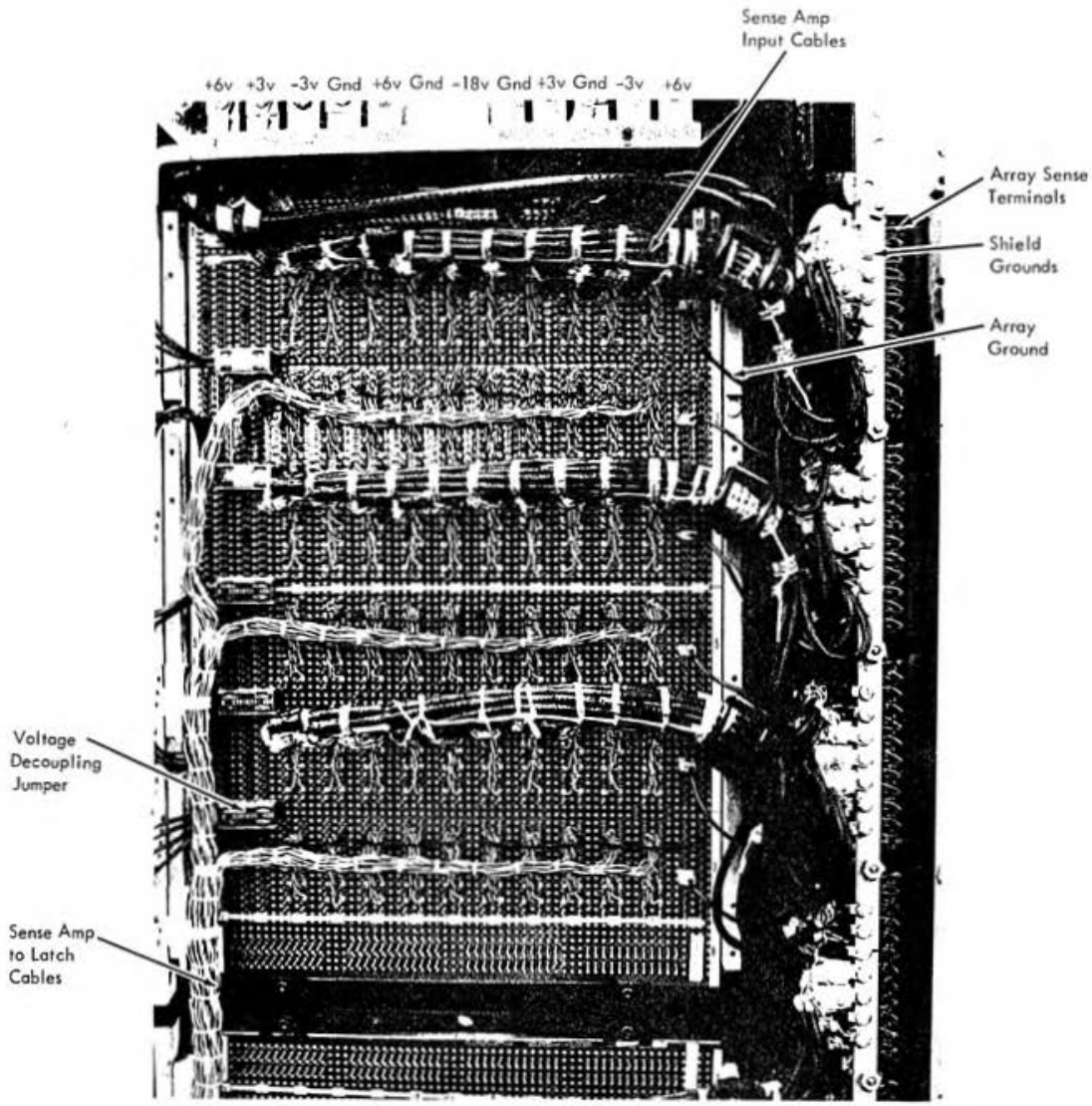


Figure 4-4. ROS E1 Board

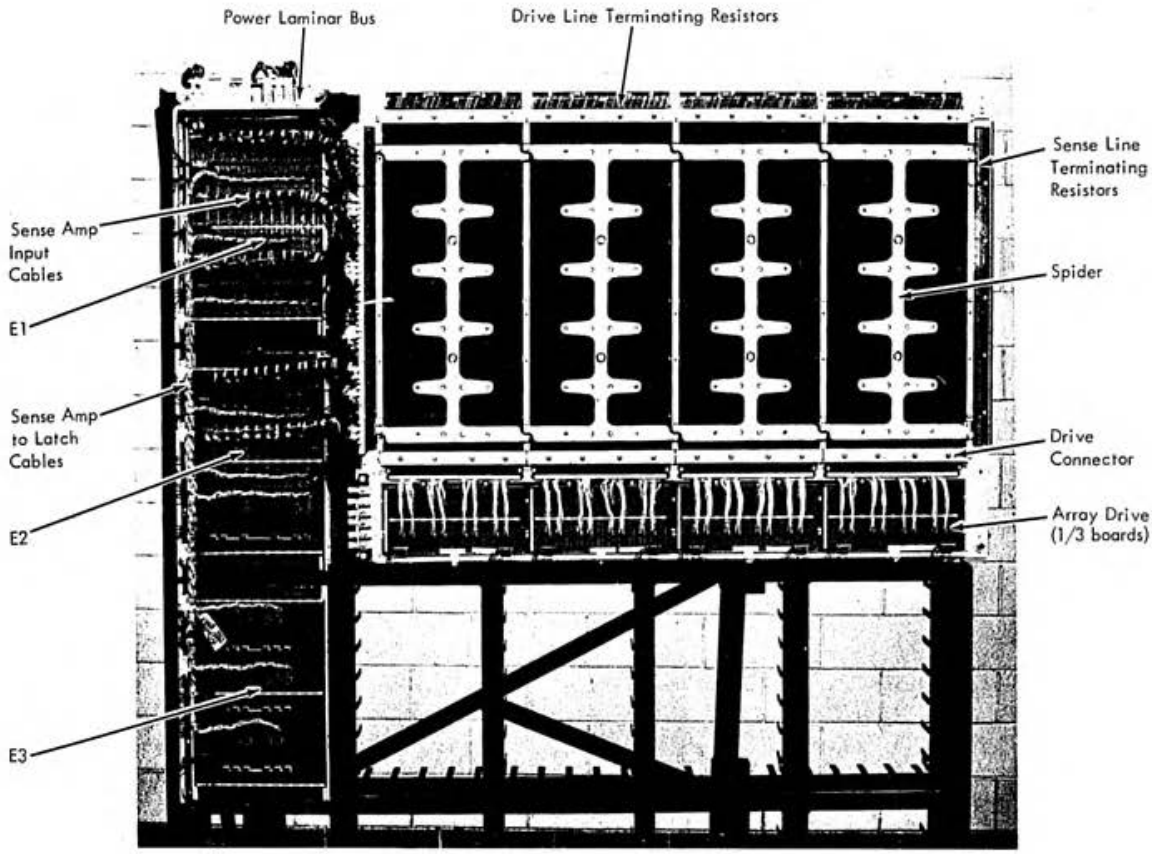


Figure 4-5. Overall ROS Layout

3. With bias at normal setting, observe failing sense amplifier outputs with an oscilloscope. Failing and non-failing bits can be compared.
4. Check for noise pulses of sufficient amplitude to sync the scope. Anything over 200 mv could indicate a shorted sense and drive line.
5. Slowly reduce the bias toward -7V. Noise resulting from incorrect cable dress usually shows up between -9V and -7V. It will appear as a 20-MHz signal having an amplitude of about 1/2V. The coaxial cables from the array to the sense amplifiers should be carefully dressed to correct this. Refer to the discussion in 4.3.6.3.1 for correct cable dress. When correctly dressed, the cables should be laced into position so that the trouble will not recur.

Noise from other sources must be found by systematically eliminating possible causes one at a time while observing the oscilloscope. Cooling fans can be disconnected one at a time, for example. Refer to the discussion in 4.3.6.3.1 for additional information.

4.3.6.3.3 Late ROS Branching. When the branch portion of the next ROS address is data-dependent, it is not available until late in the machine cycle. Due to a malfunction or a timing problem, the correct next ROS address may be decoded late. ROSAR will usually be set correctly but the ROS word will not be driven out of the array correctly. This condition is described as late ROS branching. It can produce ROS parity checks in patterns which are difficult to distinguish from those caused by electrical noise. The following method may be used to differentiate between the two.

After the machine has stopped with a ROS parity check indication, one additional word will have been read out of ROS. The address of this additional ROS word will be indicated in ROSAR. It may or may not be in good parity. Since the ROS clock was stopped when this word was read out, no parity check indications pertaining to it will be on.

The ROS word which caused the error will have its address in PROSARA or PROSARB, depending on the state of the PREV ADR A trigger. The section of this word which was out of parity will be saved in ROSDR. The remainder of ROSDR will contain bits from the word read out after the error.

Because electrical noise bursts are usually several milliseconds long, the second word will usually be out of parity as well as the first if noise is the cause. Look up the address of the last word read out (the address in ROSAR) in the ROS address list and determine whether it is in good parity. If it is in good parity, late ROS branching is the probable trouble; if not, noise should be suspected.

4.3.6.3.4 Multiple Drive Line Selection. Failures in which some bits are picked while others are dropped may result from more than one drive line being active at a time. When there is insufficient information to establish a pattern which might indicate an incorrect decode of plane, quarter plane, or drive, the following procedure may be used to find the second active drive line:

1. ROS repeat an address that fails.
2. Pull the voltage connectors from the driver boards one at a time (leaving the one for the plane being addressed) until the failure disappears. This will be the plane with the second conducting drive line. Reconnect all voltage connectors.
3. Set up the oscilloscope as follows:
   a. Form a small coil of insulated wire. Use one or two turns only. Connect this coil between the probe tip and the probe ground connection.
   b. Use a low-voltage setting on the oscilloscope.
4. Move the coil slowly across the bottom of the plane near the drive lines. As the conducting drive line is approached, a voltage will be induced in the coil. This will isolate the trouble to about three drive lines which can then be scoped normally.

4.3.6.4 ROS Parity Checks in Wait State

When ROS parity checks are experienced in wait state, the ROS clock is operating when it should not. To verify this:

1. Disable interval timer.
2. Replace system in wait state as follows:
   a. Depress SYSTEM RESET.
   b. Set DATA key bit 14 to a 1.
   c. Set all ADDRESS keys to 0.
   d. Depress STORE.
   e. Depress PSW RESTART.
3. Scope 02C-D3M6 (see logic RX003, net CD4 for pin location). There should be no clock pulses if machine is operating correctly.
4. Depress SYSTEM RESET; P0 clock pulses should be seen.

4.3.6.5 Intermittent ROS Failures

Intermittent ROS failures cannot always be resolved by card replacement. An effort should be made to gather information from logouts and indicator lights to establish the failing pattern. One of the following conditions may be found:

1. Failures in one bit in either the upper or lower word: A short may exist between a drive line and a sense line.

The shorted sense line can cause failures in all planes, but only the shorted bit line will fail. Refer to 4.3.6.2 for troubleshooting information.

2. Failures in multiple bits in one plane: This is probably due to low sense amplifier output, usually caused by plane contamination or low torque problems. The same bit positions in good addresses and failing addresses should be compared for amplitude at the output of the sense amplifiers. Varying ROS bias voltage will usually make low output problems more apparent. Refer to 4.3.6.1 for troubleshooting information.
3. Failures in one bit in one plane: Contamination or a bad plane is indicated. When the plane must be replaced, bias should be tried as a temporary repair until parts arrive. This failure pattern could also be an early indication of step 2, above.
4. Failures in multiple bits in multiple planes (extra bits): May be due to noise problems. Refer to 4.3.6.3.1 for additional information. Can be caused by gating both upper and lower word together, producing an effective ORing of the bits of the two words. This is usually a result of late ROS branching in which bit 11 of ROSAR is set too late to control gating of the upper and lower word strobe. Consult CLDs and ROS address listing to verify this. Refer to 4.3.6.3.3 for additional information on late ROS branching.
5. Failures in multiple bits in multiple planes (missing and extra bits): May indicate ROS power supply irregularities. Multiple driver selection also causes both extra and missing bits. An analysis of addresses which fail and addresses which work usually isolates this problem to incorrect decode of either plane, quarter plane, or drive. The one which does not fail is the erroneous decode. A more comprehensive procedure for troubleshooting this condition is given in 4.3.6.3.4.

4.4 FLTS

The operating procedure for the Fault Location Tests is on LADS page A6503. If an error stop is encountered, proceed in accordance with the following: heading 4.4.1 for hardcore errors, 4.4.3 for zero-cycle errors, and 4.4.4 for one-cycle errors.

4.4.1 FLT Hardcore Repair

This repair procedure consists of a series of observations and tests to locate a failure in the FLT hardcore. Correct operation of the hardcore is necessary for successful testing of the remainder of the CE hardware. Before proceeding with the FLT hardcore repairs, be sure that ROS is operating properly (heading 4.3). If any of the following failures occur, proceed as directed:

1. Failure to store 1's successfully in ST. This failure may be identified by inspecting the indicators (roller switches 1 and 2, position 3):
   a. Check that SCAN MODE switch is set to FLT position; if it is not, set it and restart the tests.
   b. Trace the failing bit(s), using logic, and repair.
2. Failure to complete IPL (first depression of LOAD). Refer to heading 4.3.4, failure 2, for further details.
3. Storage check. This failure may be identified by the FLT STG ERR indicator (roller 5, position 2) being on. Use the ripple tests (heading 4.1) with CHECK CONTROL switch set to STOP to locate the failing address.
4. Failure to stop with the specified indications after each depression of LOAD. Refer to heading 4.3.4, failure 4, for further details.
5. Hardcore error stops. See LADS page A6511.

4.4.2 FLT Zero-Cycle Tests

The zero cycle or "scan in-scan out" FLTs check each trigger by first resetting it, then setting it, and then resetting it again. The following areas are checked with these tests:

Reset to triggers.
Scan-in paths to triggers.
Zero and one clock advance.
Ability of triggers to retain their value in the absence of clock.
Scan-out matrix.

4.4.3 FLT Zero-Cycle Repair

When an error stop occurs, the following information about the failure is available in the console indicators:

1. Test number of the failing test (S9–15). This number refers to zero-cycle SCOPEX which gives the name of the trigger and its correct state, set or reset. Refer to logic page A6503 for an explanation of the notation used in SCOPEX.
2. Whether the trigger is actually set or reset. In some cases this is not possible; e.g., ROSAR and ST.
3. Whether failure was solid or intermittent.
4. Whether the stop was caused by an I/O or storage error.

To isolate the trouble:

1. Set TEST MODE switch to REPEAT.
2. Depress START.

3. Sync the scope on the 'ROS address compare' signal with the address of the last micro-instruction (see Figure 4-6 for scan-in word and ROS sync address) before the test cycle count set in the ADDRESS switches and scope the point called out in the zero-cycle listing.
4. For use as a timing reference during the scan-out operation, display the 'enable scan bypass' signal on the scope; refer to Figure 4-7.
5. SCOPEX indicates whether the trigger is set (S) or reset (R) and whether the point called out in the listing is a 0 or a 1 (0 is minus, 1 is plus).
6. Divide the failure three ways:
   a. The trigger is not being scanned to the proper value (step 7).
   b. The trigger is being set or reset correctly at scan-in time but does not retain this value until scan-out time (step 8).
   c. The trigger is at the correct value during scan-out so the error must occur during scan-out and result comparison (step 9).
7. If the trigger is not being scanned to the correct state, the cause could be bad scan-in or a faulty trigger. If so:
   a. Go to the ALDs at the page called out in SCOPEX and scope the inputs from scan (gate and bit). This is sometimes through normal data paths; e.g., R and E register triggers. If the gate and bit are present, replace the card(s) in the trigger. This applies also to a reset, except that it must be determined that none of the inputs are present to override the reset.
   b. If the gate or the data bit is missing, trace back while syncing on the micro-instruction that scans into the trigger in question (Figure 4-6). The word containing the bit may be found in scan-in and logout bit assignments shown on LADS pages A6611–A6641 and A6521–A6561.
8. If the failing trigger is initially set to the correct value and changes before it is scanned out, it could be caused by erroneous interaction between triggers. In all cases, where possible, random values have been placed in the other triggers.
   a. Go the ALDs at the page called out in SCOPEX and scope the inputs and resets to the trigger. The time period of interest is after scan-in and until after scan-out.
   b. This is best done by syncing on the ROS address that performs the scan-in. This may be determined from scan-in and logout bit assignments shown on LADS pages A6521–A6641.
9. If the trigger is set to the correct state at scan-out, do the following:
   a. Go to the logic page called out in SCOPEX and scope the output of the trigger.
   b. Go to the KT page fed by the indicator driver and scope the AND fed by bit and roller position or scan word. This scoping should be done with the roller containing the trigger in question turned to another position.
   c. If the bit is not present, trace back through the circuitry to the indicator driver and make the repair.
   d. If the gate is not present, trace back to the address sequencer. The address sequencer and left half bit are set from word 1 of the test data during scan-in with address sequencer equal to zero.
   e. If the gate is present, go forward to the correct KT8XX page and check the output on the right side of the page.

4.4.4 FLT One-Cycle Repair

When a one-cycle error occurs, the test number, shown in S(0–15), refers to the one-cycle listing of SCOPEX; see LADS page A6503. In addition, the nature of the test failure is indicated:

1. CE failure. Continual (FAIL indicator on) or intermittent (PASS and FAIL indicators on).
2. Storage failure. STOR CHK indicator on.
3. I/O failure. Channel (CCC indicator on) or I/O unit (UDC indicator on).

When a failure occurs, proceed as follows:

1. Locate test in SCOPEX and determine number of cards signified as G/F, G/FI, and those listed at end of test:
   a. If four or fewer cards are signified, replace them as described in step 2 below.
   b. If five or more cards are signified, scoping is required. The technique for scoping is described on LADS page A6503.
   c. If the timing information contains an * or a ► in the value column, refer to the logic because the feedback loop of the trigger or latch involves two or more cards.
2. If four or fewer cards are involved, replace them as follows:
   a. Determine part number of each card from ALD or card. Obtain one new card of each type.
   b. Change each card, one by one:
      (1) Do not turn off power.
      (2) After changing a card, set REPEAT switch and depress START. This operation resets the pass and fail triggers and repeats the failing test.
      (3) If the action taken in step (2) did not correct the trouble (PASS indicator on and FAIL indicator off), reset REPEAT switch and replace the original card.
      (4) Repeat steps (2) and (3) until all suspected cards have been changed or the trouble is

Scan-In Word	Register Scanner	ROS Address (Sync)	Comments
15	N	326, QY015	
14	X Y	325, QY015	
13	L M	9A9, QY015	After third time.
12	DAR and Misc	323, QY015	
11	DAR Mask	310, QY015	
10	External Register	707, QY015	
9	IOCE Machine Check Interrupt, Select Register	64D, QY015	
8	PIR, K-Register	1D1, QY015	
7	R and E	980, QY021 846, QY021 845, QY021 844, QY021	Storage Request Q(0-15) → R R → E Q(16-31) → R } Normal data paths are used.
6	PSW and IC	845, QY021	
5	D, Stats and Misc	844, QY021	
4	B and Misc	843, QY021	
3	A and Misc	842, QY021	
2	Q	842, QY021	Two cycles before ingate.
1	MCW	840, QY021	
0	S and T	150, QY021	

Figure 4-6. Sync Points for FLT Zero-Cycle Troubleshooting

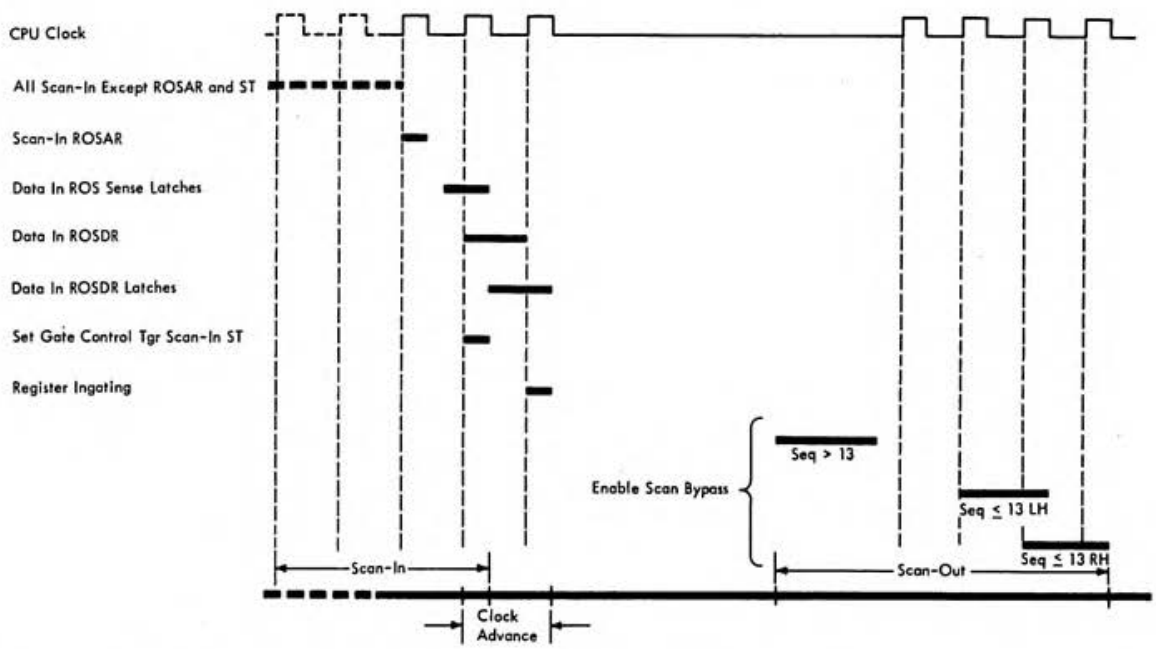


Figure 4-7. FLT Timing

corrected. If card replacement does not correct the trouble, proceed with step 3 below. If replacements made this test pass, restart FLTs from the beginning.

3. If five or more cards are involved or card replacement does not correct the trouble, isolate the trouble by using the scoping technique described on LADS page A6503. Note that the scan-out operation occurs either at 800 ns after the last clock cycle or after the clock has been started and three cycles have passed. The latter is true for all triggers that are scanned out by the address sequencer being equal to 13 or less. The triggers that are scanned out by the address sequencer being equal to 14 or more are ROSAR, ROSDR, GCTs, PAL, ST, LM, XY, K, N, and LSAR. These triggers will change state if the normal clock is allowed to start before they are sampled. Use the 'enable scan bypass' signal for reference; refer to Figure 4-7.

4.4.5 SCOPEX Timings

This discussion is to facilitate maintenance personnels' understanding of the SCOPEX timings shown on LADS page A6503. It consists of an explanation of times A, B, C, and D with reference to what is actually happening in the machine. Throughout this writeup, the term "Data" means either a 1 or a 0.

The 7201-02 works on the basic principle that data flows from trigger to latch to trigger, and that the triggers are set at clock time and latches at not-clock time. The FLTs generally test a data path from one trigger, through an associated latch, and into another trigger. From here, it is scanned out to "T" and checked. Only two clock pulses are required to perform this function. One pulse is needed to set it into the first trigger and address some ROS word to bring up appropriate gates to pass the data to the next trigger. The not-clock pulse passes the data from the first trigger to its latch. The second clock pulse sets the data into the trigger to be tested.

When synced on ROS address 150 and displaying three clock pulses, the first pulse seen on the scope is actually the one at address 150 and scan-in is just being completed. The micro-orders to scan into S & T are in CAS block 150, but these triggers are not actually set until the next clock pulse; i.e., the second clock pulse seen. This second clock pulse is the one of interest. It is at this time that the first trigger in the path will have data set into it (as in the case of S & T) unless it has been previously scanned into.

Now the first timing in SCOPEX can be discussed. It is the last shown on LADS page A6503, time D. When SCOPEX states a line should be up during D, it must be up shortly into the second clock pulse and remain up until almost the same time in the third clock pulse. It may have been up solid at the start of the second clock pulse if it was scanned into previously, but it must remain up at least during the second clock and not-clock pulses to transfer the data to the latch.

The second time is C. This is the time the data is passing through the latch. The data must be up at least by the second not-clock pulse and extend through the third clock pulse to allow it to gate into the next trigger.

The third time is A. This means that the line should come up sometime during the third clock pulse and remain up. It is from here that the data will be scanned out.

The fourth time is B. This is usually a gating line and may have a clock pulse associated with it, but it must be up during the third clock pulse. It is the gate which transfers the latch data into the trigger.

Note that when working with certain tests there will be only two clock pulses showing. When this is true, times A and B pertain to the third pulse shown, time C to the first not-clock pulse, and time D to the first clock pulse. The CE should follow the SCOPEX with the ALDs open, whenever possible, so he may more intelligently decide what is correct.

Figure 4-8, A, is a pictorial summary similar to that shown on LADS page A6503. It illustrates a typical FLT that will test the ability of the machine to transfer bit 63 of A, through the parallel adder, into position 63 of T. To do this, bit 63 of B will be set on during the scan-in operation. When scan-in has been completed, the CPU clock will be permitted to run for two cycles.

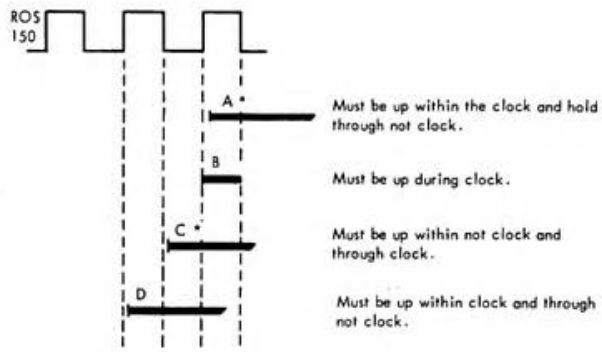
During the first clock cycle (Figure 4-8, B), the ROS word contains micro-orders necessary to gate bit 63 of B through the adder and into position 63 of T, where it will be decoded and executed. The second clock cycle is needed to accomplish ingating to T.

During the second clock cycle, the ROS sense latches are held reset, thereby preventing decode of the second ROS word. This prevents destroying the data set up in the previous cycle.

4.5 DIAGNOSTICS

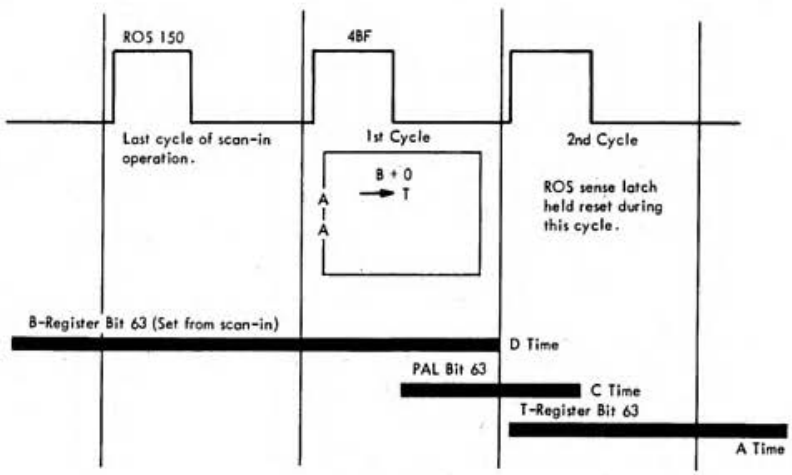
CE diagnostic programs are loaded into the system from the System Maintenance Tape. For the most thorough testing, the diagnostics should be run under high, low, and no bias (refer to Chapter 5, heading 5.2, for marginal checking procedure).

To run the CE diagnostics it is necessary to have configured a "maintenance subsystem" consisting of the following minimum number of elements: the CE to be tested, an IOCE, an SE, a TCU, and a tape drive. The subsystem may be configured by the operating ATC system or, if the elements are in state zero, it may be configured manually. Refer to heading 4.5.1 for manual configuration procedure.



Note: * Denotes triggers or latches where portions of the associated "latch back" circuitry will be found on more than one card.

a. Understanding of Scopex Timings



b. Typical Example

Figure 4-8. SCOPEX Timing

With a maintenance subsystem configured and the system maintenance tape mounted on one of the subsystem tape drives, a subsystem IPL of the diagnostic programs may be executed from the CE as follows:

1. Turn the TEST switch off.
2. Be certain that the SYSTEM INTERLOCK key is in the off position (counterclockwise).
3. Set the MAIN STORAGE SELECT switch to the number of the maintenance subsystem SE.
4. Set the LOAD UNIT switches to the address of the system maintenance tape drive.
5. Depress LOAD.

IPL loads Go/No-Go which runs and subsequently calls in the Basic Storage Test which, in turn, calls in Hardcore. Hardcore automatically loads the Subsystem Diagnostic Monitor (SDM). SDM goes into a wait state to permit entry of input messages in which the operator specifies diagnostic program sections to be run. SDM is intended to be the primary monitor for running CE sections but will not accommodate multiprocessing or multiprogramming. The Multiprocessing Diagnostic Monitor (MDM) will accommodate these. MDM can be loaded by SDM if it is specified by an operator's input message.

For further information regarding Go/No-Go, Basic Storage Test, Hardcore, SDM, and MDM D/E refer to the Maintenance Monitor Manual (PN 5444417). In addition, detailed operating requirements for diagnostic sections are given in each diagnostic section description.

4.5.1 Manual Configuration of Maintenance Subsystem

Manual configuration of a maintenance subsystem requires that the subsystem elements be in state zero. Further, consideration must be given to the IOCE to TCU channel connections so that the TCU chosen will be one which can actually communicate with the IOCE. Headings 4.5.1.1 through 4.5.1.4 provide procedures for manually configuring each of the elements in a minimum subsystem; namely, CE, IOCE, SE, and TCU.

4.5.1.1 Manual Configuration of CE

The following procedure outlines the actions that must be taken at the CE control panel during the manual configuration of a maintenance subsystem.

1. Set the CCR:
   a. Place TEST switch in TEST position.
   b. Place REGISTER SELECT rotary switch in CCR position.
   c. Depress RESET (Force CE into the Stop Loop).
   d. DATA switches (32–63): set switches on for this CE's SCON and communications bits and the maintenance subsystem SE and IOCE communications bits (the format is indicated beneath the switches).
   e. Set roller 5 to position 5 (CCR).
   f. Depress REGISTER SET pushbutton and observe that the bits in the data switches are set into the CCR.
2. Set ATRs 1 and 2:
   a. Place REGISTER SELECT rotary switch in the ATR position.
   b. DATA switches (0–3): set the identifier of the subsystem SE into the data switches.
   c. Set roller 2 to position 1 (ATR).
   d. Depress REGISTER SET pushbutton and observe that the subsystem SE identifier is transferred into ATR slot 1.
3. Set PSBAR:
   a. Place REGISTER SELECT rotary switch in the PSBAR position.
   b. DATA switches (41–51): set these data switches to zeros.
   c. Set roller 5 to position 1 (PSBAR).
   d. Depress REGISTER SET pushbutton and observe that logical PSBAR is set to zeros and physical PSBAR is set to the SE identifier from ATR slot 1.
4. Set TEST switch to normal position.

4.5.1.2 Manual Configuration of IOCE

The following procedure outlines the actions that must be taken at the IOCE control panel during the manual configuration of a maintenance subsystem for testing of a CE. The following steps permit the manual setting of the IOCE CCR:

1. Place TEST switch in TEST position.
2. Place REGISTER SELECT switch in CCR position.
3. DATA switches (0–31): set the controlling CE's SCON and communications bits and the subsystem SE communications bits into the data switches (the format is indicated beneath the data switches).
4. Set roller 3 to position 7 (CCR).
5. Depress REGISTER SET pushbutton and observe that the bits in the data switches are transferred to the CCR.
6. Set the TEST switch to normal position.

4.5.1.3 Manual Configuration of SE

The following procedure outlines the actions that must be taken at the SE during the manual configuration of a maintenance subsystem for testing the CE.

1. Set the CCR byte 1:
   a. Place TEST SWITCH in the TEST position.
   b. Depress RESET.
   c. Place INHIBIT CHECK STOP switch in OFF position.
   d. Set MARK SWITCH 4 to select first CCR byte (disregard Mark Parity).
   e. Set DATA SWITCHES to the desired bit pattern for the byte to be set. Use the format of the CCR indicators. The bit patterns should include the communications bits for the subsystem CE and IOCE (byte 1) and the CE's SCON bit (byte 2).
   f. Depress SET CONFIG and observe that the data bits are transferred to the CCR.
   g. Depress STOP.
2. Set the CCR byte 2:
   a. Repeat steps d–g using MARK SWITCH 7 in step d.

      Note: Do not depress RESET.

   b. Set TEST switch to normal position.

4.5.1.4 Manual Configuration of TCU

The following procedure outlines the actions that must be taken at the TCU during the manual configuration of a maintenance subsystem for testing the CE. The procedure permits the configuring of either interface to the subsystem IOCE and includes steps to perform a Release command from the unused interface if it has been reserved by a previous operation. To set the TCU CCR, perform the following steps at the TCU maintenance panel:

1. Plug the following jacks:
   OFF LINE
   TCU ADDRESS (plug a valid address observing odd parity)
   TU ADDRESS (plug a valid address observing odd parity)
2. Determine whether primary or secondary interface is to be configured (depends on IOCE to TCU channel cabling).

   Note: Primary = INTF B = Y OP
   Secondary = INTF A = X OP

3. If X or Y OP INTERFACE lamp is on for the channel to be configured (or if neither is on), perform configuration (steps 8–10); otherwise, it is necessary to perform a release on the opposite interface (steps 4–7).
4. Plug: INTF A if X OP INTERFACE lamp is on; INTF B if Y OP INTERFACE lamp is on.
5. Plug 0B hex (Release command) in COMMAND 1 and plug STOP for COMMAND 1.
6. Depress MACH RESET.
7. Depress START and observe that the interface is released (X OP INTERFACE or Y OP INTERFACE lamp goes off).
8. Plug the following jacks:
   INTF B (if primary interface is to be configured)
   INTF A (if secondary interface is to be configured)
   COMMAND 1 - 03 hex (Set Configuration command) + STOP.
   WR DATA 1 - Desired configuration:
   Bits 0–3 correspond to CE 1–4 SCON bits; bits 5–7 correspond to IOCE 1–3 communications bits (observe odd parity for CE group of bits and IOCE group of bits separately; bit 4 is the parity bit for the IOCE group).

   Note: Be certain ALL ONES is not plugged.

9. Depress START and observe that configuration is set into CCR.
10. Remove all pins in "red area" (including OFF LINE).

4.6 TIMING CHECKS

The timing procedure and checks for the CE delay lines and singleshots are found on LADS pages A8001, A8002. ROS timing procedure is on LADS page M8004.

4.7 LAMP TESTS

All lamps on the CE control panel, associated with a particular roller switch, light when the roller switch is between detents. All lamps on the CE control panel not associated with the roller switches or power light when LAMP TEST ALLOW IND pushbutton is depressed.

4.8 SIGNAL TO FRAME GROUND SHORTS; SERVICE CHECK

To make the CE less susceptible to transient voltage problems, there should be a single frame ground connection for each CE. That is, all dc returns in the CEs are brought to a common DC return bus which is located in the power wall. It is from this bus that a DC return to machine frame ground is made. The system should be checked for signal-to-frame ground shorts during installation. Additional frame grounds cause unexplained errors; for example, ROS parity checks or storage checks.

4.9 ROS OPTIMIZATION

The ROS timing and bias are optimized by a procedure called "shmooing". A ROS shmoo is a two-dimensional plot (bias vs time) of the failure points of ROS. The shmoo identifies the optimum operating point of both the bias voltage and the time of the leading edge of the strobe signal.

4.9.1 Adjustment Procedure

The adjustments and shmooing procedures are found on LADS pages A8004 and A8085. Figure 4-9 shows the waveshapes for a typical 1 and 0 bit. Basically, the shmooing procedures is as follows:

1. Adjust timing in accordance with the procedure in steps I through VII on LADS page A8004. Prepare a plot of the bias vs time failure points while running diagnostic program number D13CD.
2. Vary the strobe position about its initial time value in 5-ns increments while the ROS is being exercised. At each time setting, vary the ROS marginal panel control from -7V to -20V, recording both the upper and the lower V_M (-18 variable supply) values at which ROS errors occur. At each failure point, also record the failing ROS address and bit. This data should be plotted on a graph (shmoo). A typical shmoo is illustrated in Figure 4-10.
3. The optimum value of strobe timing and V_M is determined by placing a rectangle of area 6V by 15 ns within the area defined by the failure points of the shmoo. The rectangle should be vertically centered within the shmoo while maintaining the rectangle area error-free. It may be to the left or right of center, depending on the available delay taps. See Figures 4-11 and 4-12.
4. If the rectangle cannot be placed within an error-free area as defined above, the ROS must be debugged. This will require bit and sense plane cleaning. Heading 4.9.2 defines the prescribed debugging procedure.
5. When the machine has been debugged satisfactorily to allow successful completion of steps 2 and 3, the optimum strobe timing and ROS marginal panel control setting will be the center point of the rectangle. If this point does not lie on a value of strobe timing attainable with the -5-ns increments of the delay line, the operating point should be on an incremental value as close as possible to the indicated point. It may be to the left or right of center.
6. With ROS set at optimum strobe timing, ROS marginal panel control is to be varied ±20% of its optimum value (all other logic voltages are left at nominal); the ROS, being again exercised in all addresses, will run error-free during this ROS marginal panel control variation.
7. If step 6 is successfully completed, return ROS marginal panel control to its optimum value. The optimized values of strobe timing and ROS marginal panel control are the new nominal operational settings for the ROS. If step 6 cannot be successfully completed, the optimization procedure must be repeated.

4.9.2 Debugging Procedure

This procedure shall be followed if the conditions of steps 2 and 3 of heading 4.9.1 cannot be successfully met:

1. The shmoo shown in Figure 4-10 is a typical example of an area defined by failure points. Note that the recorded bits and addresses in error tend to be repetitive within the segments on either side of the peak of the shmoo. If only one or two bits are repeatedly causing failures throughout the shmoo, an attempt may be made to improve the shmoo by replacing or exchanging sense amplifier cards. If three or more bits appear to be causing failures, or if replacing the cards (for one or two bits) does not sufficiently improve the shmoo, scope the bits to verify which, if any, is weak (see Figure 4-13). Repeatedly failing planes should be cleaned first.
2. Remove the ROS planes indicated by the shmoo failure points and clean thoroughly according to 4.13.1, 4.13.2, and 4.13.3. When the cleaned planes have been replaced, re-evaluate the shmoo according to steps 2 and 3 of 4.9.1. If these steps are successful, continue with the remaining steps of the optimization procedure.
3. If the improvement obtained by the initial cleaning is not sufficient to meet the conditions of steps 2 and 3 of 4.9.1, repeat step 2 above.
4. If, after the second cleaning, steps 2 and 3 of 4.9.1 cannot be successfully completed, again verify seating of the amplifiers. If all cards prove to be properly seated, and optimization still is not possible, replace the amplifier card(s) in the position(s) of the predominant failing bit(s), and repeat the entire optimization procedure.

4.10 BASIC CLOCK TIMING

Refer to LADS pages A8001 and A8002 for CE clock timing procedure and to LADS page A8006 for storage control clock timing procedure.

4.11 1052 SINGLESHOT ADJUSTMENTS

Refer to ALD ZP090 for 1052 singleshot adjustments. Measure all time durations at the 1.5V level.

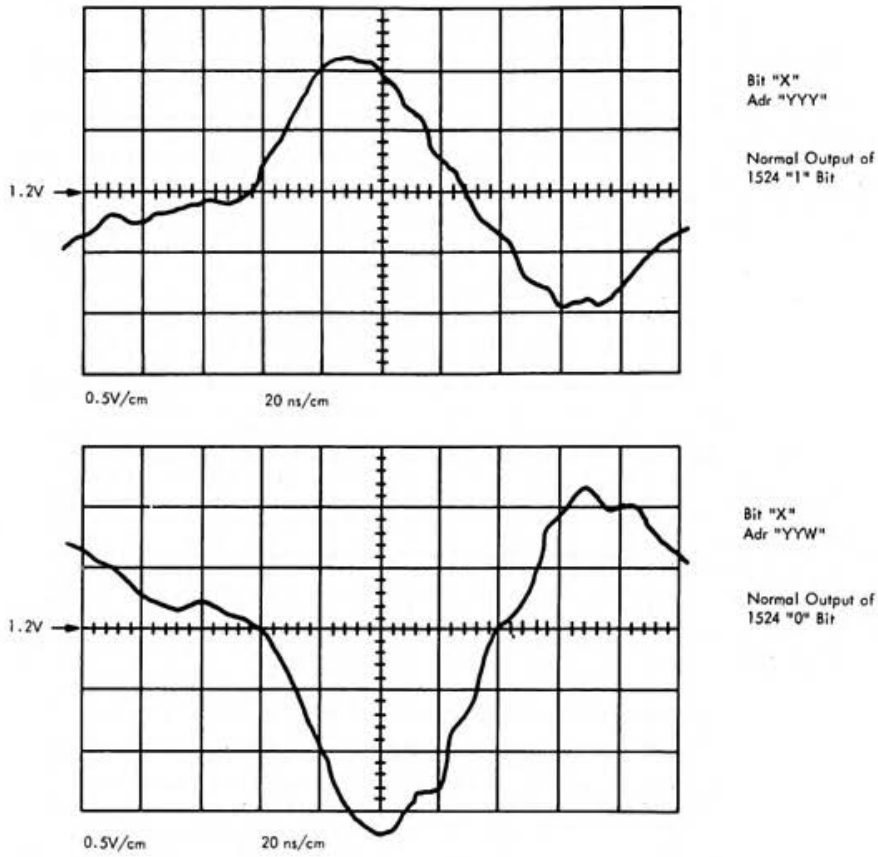


Figure 4-9. ROS Sense Amplifier 1 and 0 Bit Waveforms

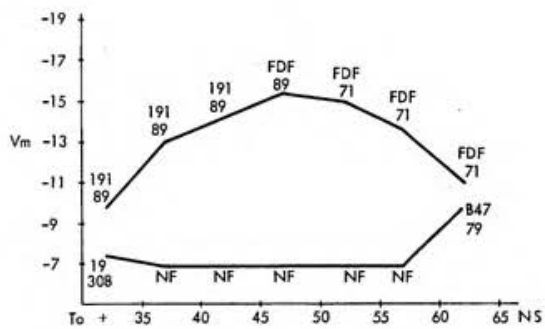


Figure 4-10. Typical Shmoo

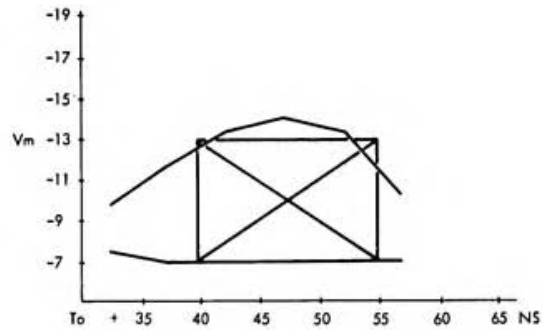


Figure 4-11. Unacceptable Shmoo

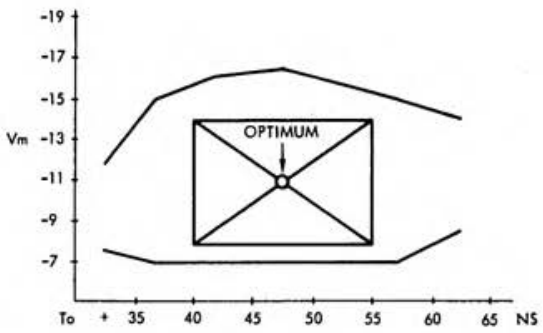


Figure 4-12. Acceptable Shmoo

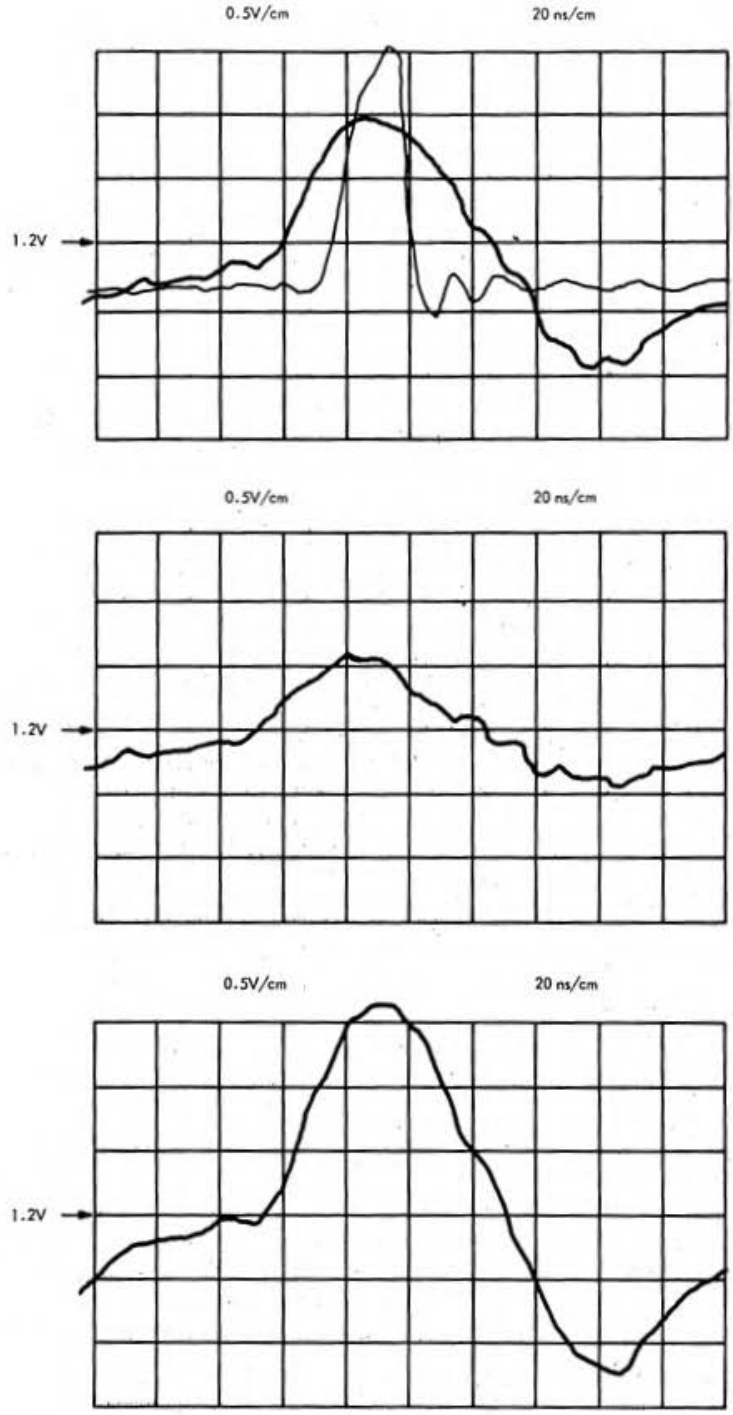


Figure 4-13. ROS Sense Amplifier, Average/Weak/Strong Waveshapes

Observe the following general hints on removal and replacement of assemblies:

1. Turn off power.
2. Use the right tool for the job.
3. Get help if the assembly is heavy.
4. Pay attention to the order of parts (spacers, washers, etc.) so that installation will be correct.
5. Tag wires as they are removed. Do not trust your memory.

4.12 BOARD REPAIR AND REPLACEMENT

The procedure for repairing and replacing boards is detailed in SLT Packaging FETOM.

4.13 ROS BIT PLANES

The following paragraphs discuss removal, cleaning, and installation of ROS bit planes.

4.13.1 Removal

The following procedure for removal of the ROS bit planes must be carefully followed:

1. Release pressure on the six pressure plates by loosening the 12 torque screws in the spider (Figure 4-14). Use standard bristol wrench or torque wrench (PN 461450). Do not remove torque screws; just relieve pressure. Do not loosen retaining screws.
2. Release pressure on upper and lower drive connectors by loosening pressure hex screws (four per connector). Do not remove pressure hex screws; just relieve pressure.
3. Remove the two retaining screws on both upper and lower drive connectors.
4. Remove the four corner hex screws on the spider.
5. Remove the two knurled nuts on the spider. They may be removed by hand.
6. Remove spider from two center studs. The six pressure plates are held to spider by the 12 retaining screws.
7. Remove rubber pressure pad from the two center studs.
8. Wearing lint-free gloves (PN 461421), carefully remove bit plane from alignment pins and center studs by holding at center of each horizontal edge. Plane must be held and gently lifted without being allowed to bow or touch anything.

CAUTION

The bit plane must not be creased, folded, scratched, allowed to come in contact with oil (including skin oils), or subjected to dust. The same is true of the sense lines.

4.13.2 Cleaning

The following procedure for cleaning the ROS bit planes must be carefully followed just prior to installation of these bit planes:

1. Wearing lint-free gloves (PN 461421), prepare a large flat surface, at least as large as bit plane, by washing it with lint-free cloth (PN 461622) thoroughly saturated with cleaner solution (PN 450608). Freon* should not be used.
2. Clean sense plane and upper and lower connector tabs by washing them with lint-free cloth thoroughly saturated with cleaner solution.
3. Place bit plane on prepared surface, Mylar* side up.
4. Fold new lint-free cloth into pad about 3 or 4 inches square and saturate it with cleaner solution.
5. Rub the bit plane with pad over entire surface, starting at one end and rubbing back and forth over entire length. If pad begins to dry, reapply cleaner solution.

CAUTION

Under no circumstances should the cleaner solution be applied directly to the bit plane or sense plane.

6. Immediately after drying, install bit plane.

4.13.3 Installation

The following procedure for the installation of clean ROS bit planes must be carefully followed:

1. Turn the 12 retaining screws on spider CCW until the six pressure plates are loose and flat against spider. Do not back screws out past this point.
2. Clean both bit and sense planes, as described in 4.13.2.

CAUTION

Under no circumstances should cleaning solution be applied directly to the bit plane or sense plane.

*Trademark of E. I. du Pont de Nemours & Co. (Inc.)

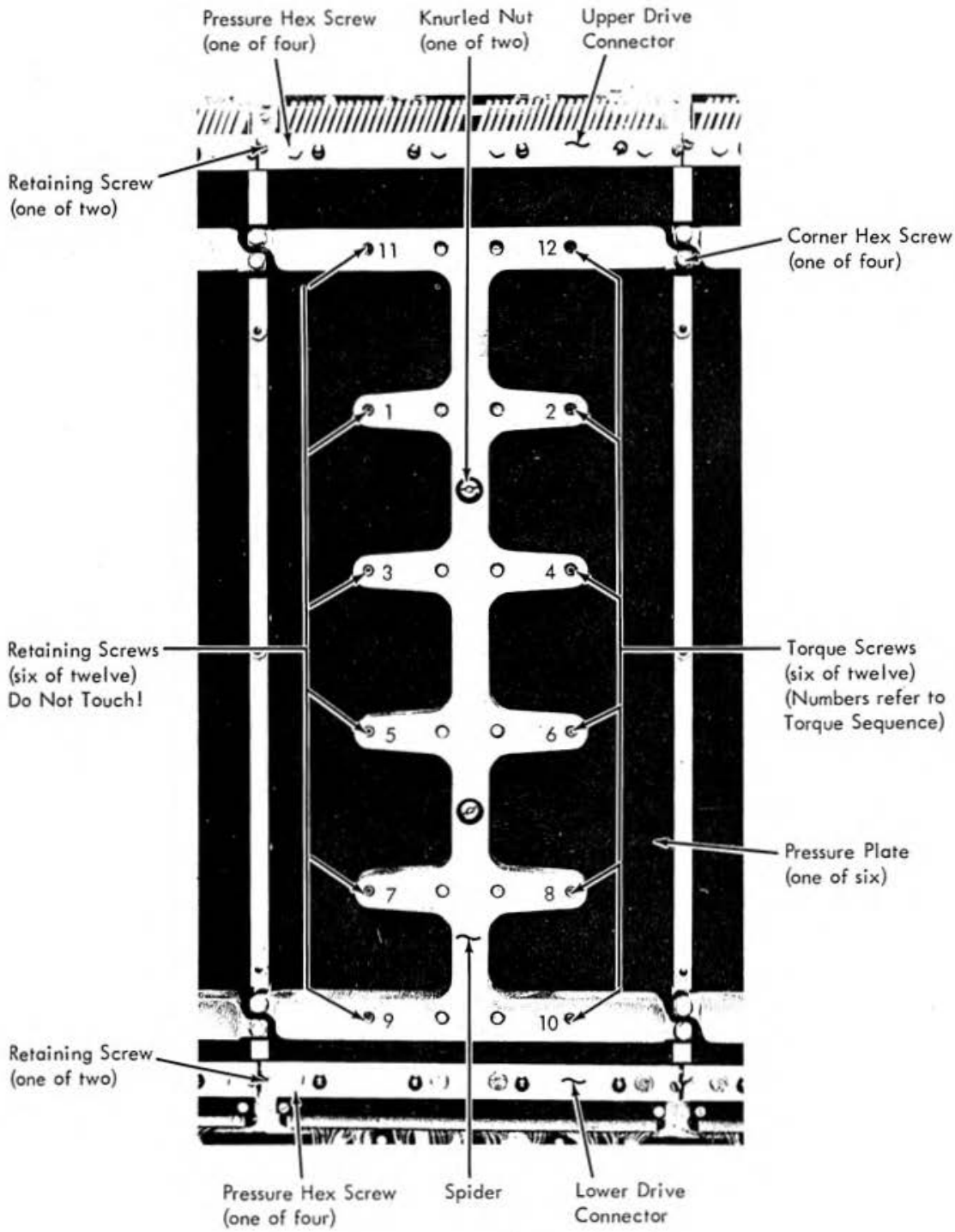


Figure 4-14. ROS Pressure Spider and Torque Sequence

3. Immediately place bit plane over the two center studs, Mylar side against sense plane, with alignment hole up and slot down. Gently press copper land around upper alignment hole flat against sense plane and then do same for lower slot. (Upper hole provides both horizontal and vertical alignment; lower slot provides only horizontal alignment.) Bit plane must be flat against sense plane. Check registration at top and bottom of bit plane. Drive line flag must completely cover sense line at both top and bottom of bit plane. (Use sense line for bit 0 upper and bit 90 upper for this check.) If the registration is not correct, push the bit plane up as far as possible. If the registration cannot be corrected, replace the bit plane and check registration again. If it is still incorrect, contact the plant through your area office.
4. Install both upper and lower drive connector pressure bars with the two retaining screws on each. Do not tighten pressure hex screws. Recheck that bit plane is flat against sense plane and that registration is correct.

   Note: Clean the rubber surface of the pressure bars before installation.

5. Install rubber pressure pad over the two center studs.
6. While holding rubber pressure pad in position, place spider and pressure plate assembly over the two center studs.
7. With slight upward pressure on spider, align it with corner hex screw holes. Install the four corner hex screws, but do not overtighten them; just be sure they are bottomed and snug.
8. Install the two knurled nuts, but tighten them no more than fingertight.

   CAUTION

   The two knurled nuts must be installed before torqueing and must not be more than fingertight or the spider may fracture as it is loaded.

9. Using torque wrench (PN 461450), tighten the 12 torque screws to 2-inch pounds in the sequence shown in Figure 4-14.
10. In the same sequence, tighten torque screws 1–8, 11, and 12 to 4-1/2 inch-pounds and tighten torque screws 9 and 10 to 3-1/2 inch-pounds.
11. In the same sequence, check that torque on torque screws 1–8, 11, and 12 is within 4 to 5 inch-pounds and that torque on 9 and 10 is within 3 to 4 inch-pounds. If any torque screw is not in required range, retorque in same sequence, and recheck.
12. Remove the two retaining screws on both upper and lower drive connector pressure bars.
13. Check horizontal alignment of bit plane drive line connector tabs with tabs on terminating resistor card at top of plane and tabs of drive card at bottom of plane. Both cards may be shifted horizontally for alignment with bit plane tabs by loosening the two hold-down screws in each.
14. Check vertical position of drive connector board. Drive tabs on board must be visible below bit plane. If tabs are completely covered by bit plane, drive board should be moved down as far as possible. If this adjustment cannot meet position requirements, board should be replaced. A temporary repair can be made by placing tape over diagonal land patterns on drive board.
15. Install both upper and lower drive connector pressure bars with the two retaining screws on each.
16. Tighten the four pressure hex screws on each pressure bar until they are bottomed and snug. Do not overtighten.

This section contains a collection of miscellaneous service aids which may point out a troubleshooting approach to a particular problem when FLTs and diagnostics have not isolated the trouble. To help maintenance personnel work more effectively, some common troubleshooting pitfalls are called out here, together with positive suggestions for avoiding them:

1. Make full use of console indicators. Much time can be lost by scoping points which are already indicated on the console. Lamp test should be used often to avoid being misled by burned out indicator lamps.
2. Determine early whether the trouble is broad or localized so that as much circuitry as possible can be eliminated.
3. Instead of proceeding block by block, choose scoping points so that the suspected circuitry is cut in half.
4. Keep the approach to a trouble as simple as possible by seeking the simplest operation that will fail. Do not key in long instruction loops by hand if such loops are available in the diagnostics.
5. When no progress is being made, recheck the most basic assumptions. For example, the original symptom may no longer be present or it may have been a result of an error in operating procedure. Some common operator errors are given here:
   a. RATE switch not in PROCESS position.
   b. Incorrect parity in general-purpose or floating-point registers.
   c. Wait bit on in current PSW.
   d. Program interrupt with no program new PSW stored. The IC contains 8 or A since the blank new PSW itself causes a program interrupt when no valid instructions are at location zero in storage.
   e. Program interrupt commonly caused by specification error in instruction or by incorrect protect key in current PSW while executing store-type instructions.
6. If trouble is difficult to isolate, consider the more remote possibilities. More than one trouble may be present or, less likely, more than one failing component may be responsible for a single symptom.
7. Several seemingly unrelated symptoms can result from a loose card or a loose flat cable connector.
8. An intermittent problem may be caused more frequently with voltage bias or frequency alteration.
9. If program looping is difficult because of a result from a failure, ground an appropriate pin to eliminate the result.
10. To loop a program, use ADDRESS COMPARE, LOOP (heading 2.1.6, item 7) instead of modifying the program.

4.14 STOP-LOOP FAILURES

Failures which occur during the stop loop may be isolated while operating at machine speed, using the following procedure:

1. Set ROS ADDRESS switch to STOP position.
2. Set ROS ADR COMPARE switches to address of first block of stop loop. (Refer to QY041.)
3. Depress SYSTEM RESET. PROSARA or PROSARB (depending on the PREV ADR A indicator) contains address stopped on. Address of next block to be executed is in ROSAR and must agree with next address shown in CLD.
4. If no error occurs, repeat steps 2 and 3 using sequential ROS addresses in stop loop until an error or wrong branch occurs.

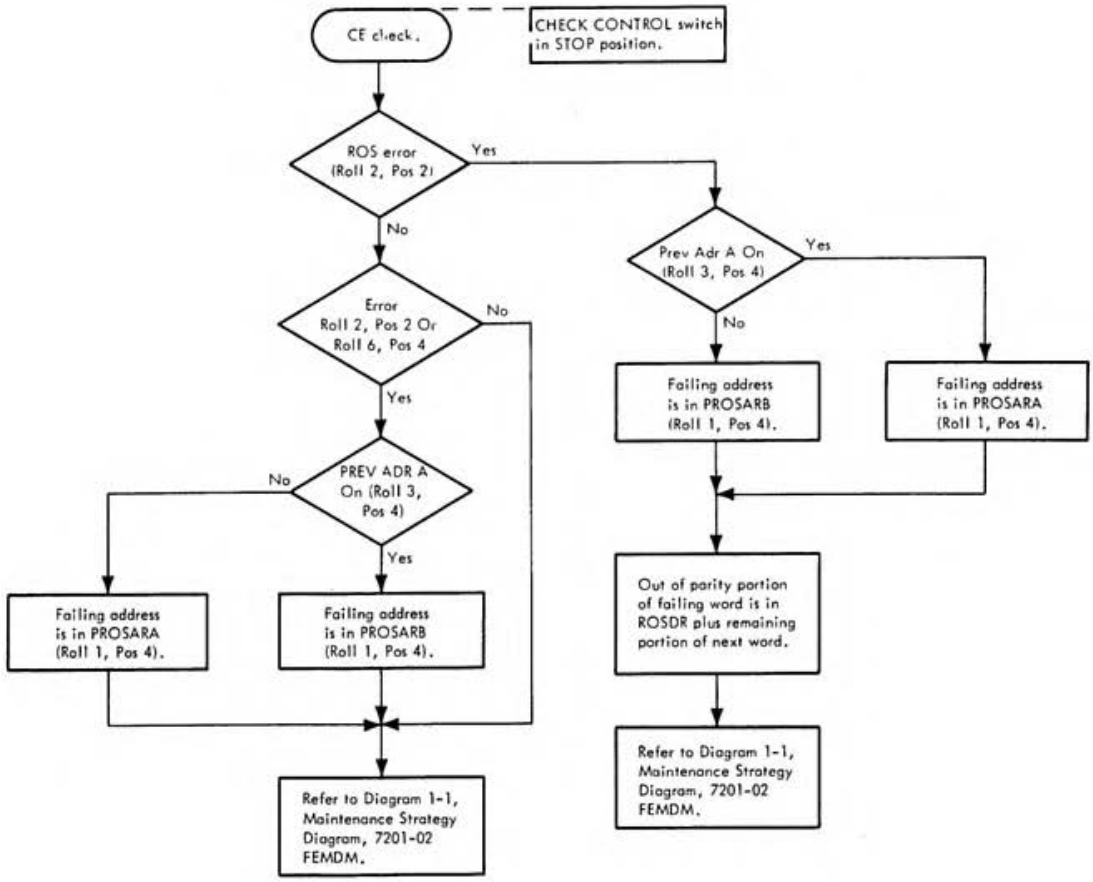
4.15 CE CHECKS; DETERMINING FAILING ROS CYCLE

When a CE check occurs while operating in Check Stop mode, the CE clock stops after execution of the ROS cycle in which the error trigger is set. The cycle in error is indicated differently for ROS parity checks and adder checks. For example, if the previous ROS address is in PROSARA (per the PREV ADR A trigger), the address of the failing ROS cycle in PROSARB for an adder check. Use Figure 4-15 to determine the ROS address corresponding to the cycle in which the failure occurred.

4.16 CE TROUBLESHOOTING FLOWCHARTS

Refer to the following flowcharts for troubleshooting specific areas of the CE:

Figure 4-16 E-Register Parity Checks
Figure 4-17 Multiplier Decode Parity Checks
Figure 4-18 Serial Adder Full-Sum Checks
Figure 4-19 Parallel Adder Half-Sum Checks



To Find	PREV ADR A Indicator	Look In
Next ROS Address	N/A	ROSAR
Current ROS Address	ON	PROSARA
	OFF	PROSARB
Previous ROS Address	ON	PROSARB
	OFF	PROSARA

Figure 4-15. CE Checks; Determination of Failing ROS Cycle

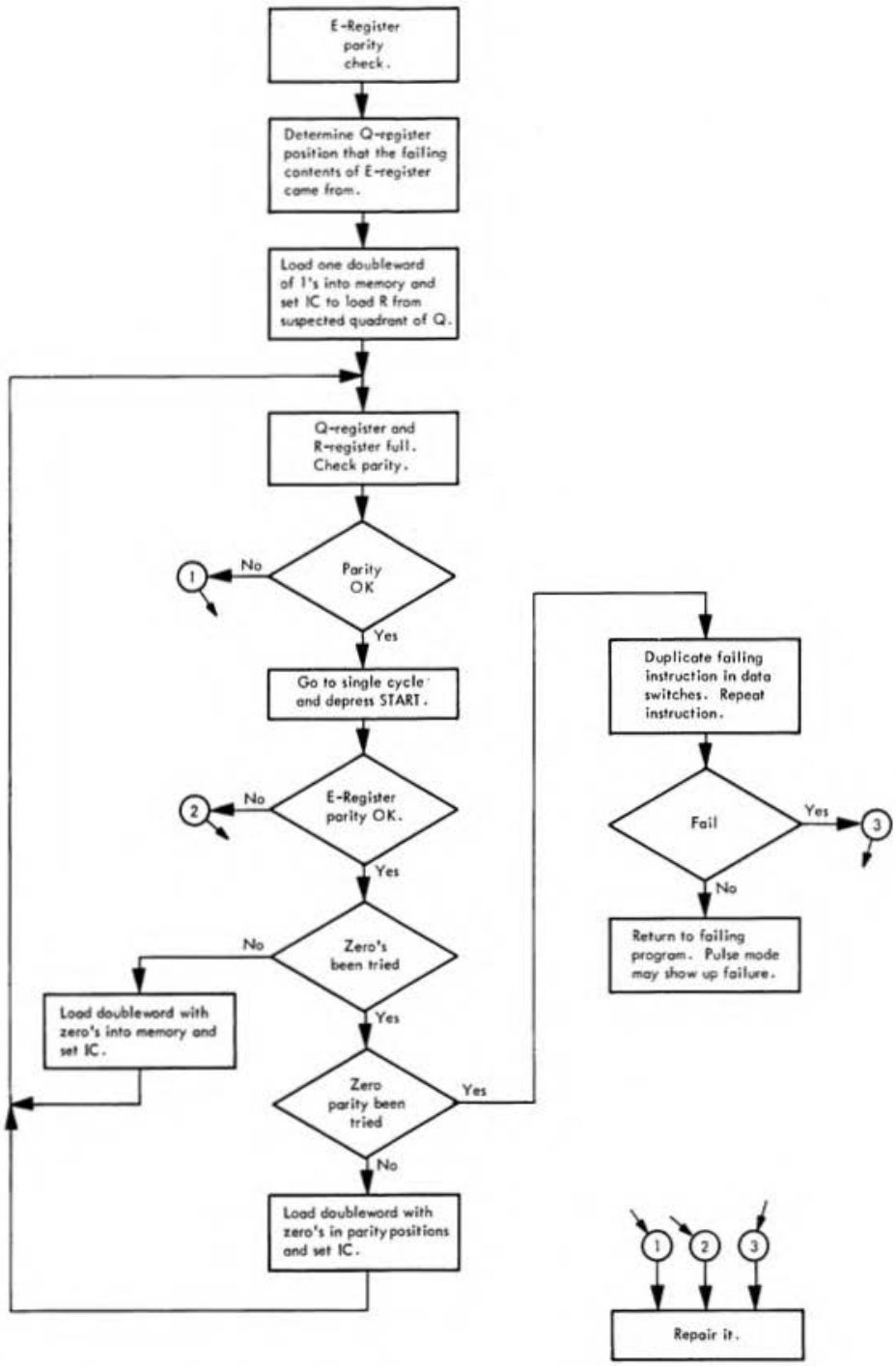


Figure 4-16. E-Register Parity Check Troubleshooting

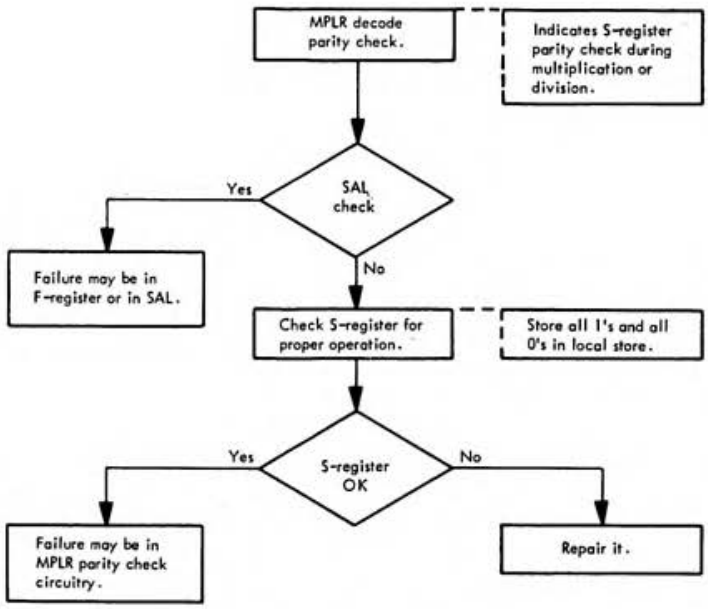


Figure 4-17. MPLR Decode Parity Check Troubleshooting

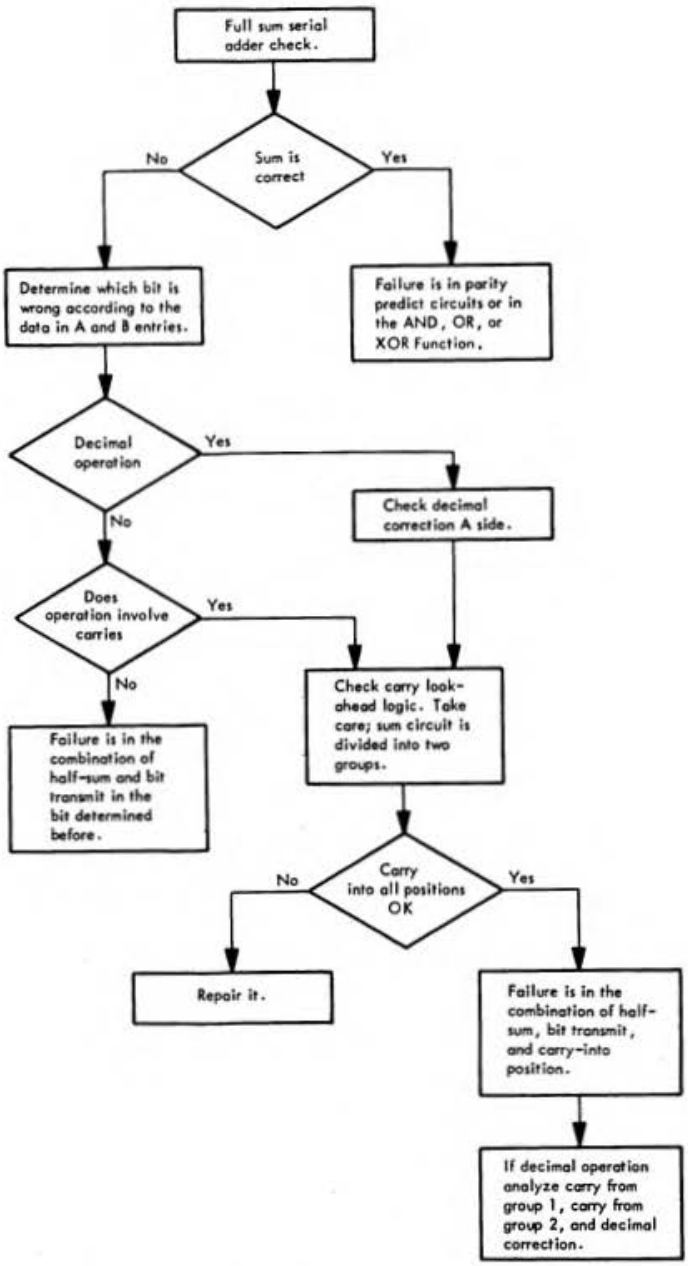
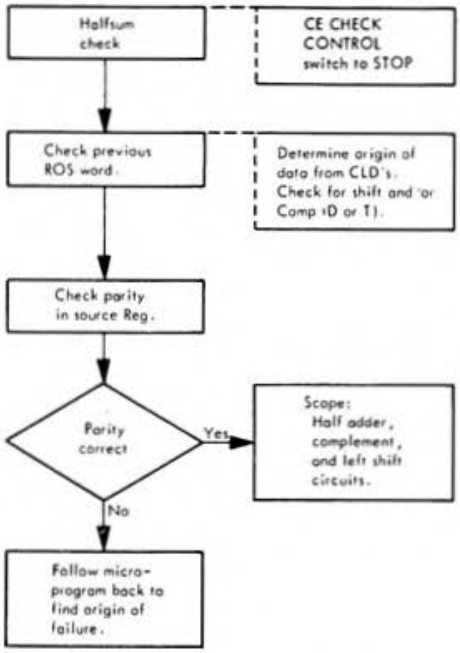


Figure 4-18. Serial Adder Full-Sum Check Troubleshooting



Possible Entries per Gate Control Triggers

Source	Adder Bits	ALD
S(00-31)	to PAA(32-63)	RT815
T(32-63)	to PAA(32-63)	RT807
T(32-63)	to PAA(31-62)	RT811
T(32-47)	to PAA(43-63)	RT813
T(48-63)	to PAA(48-63)	RT815
D(00-23)	to PAA(08-31)	RT803
D(00-23)	to PAA(07-30)	RT805
D(00-23)	to PAA(40-63)	RT801
ONES	to PAA(61-63)	RT813
IC	to PAB(40-63)	RB811
A(00-31)	to PAB(32-63)	RB805
A(04-07)	to PAB(04-07)	RB805
A(08-31)	to PAB(08-31)	RB813
B(32-63)	to PAB(32-63)	RB813
B(64-67)	to PAB(64-67)	RB813
A(06-31)	to PAB(04-29)	RB811
B(32-67)	to PAB(30-65)	RB811
B(64-67)	to PAB(28-31)	RB807
EXCS6	to PAB(28-63)	RB805
F(04-07)	to PAB(60-63)	RB807
HOT-1	to PAB 60	RB807
E(08-11)	to PAB(56-59)	RQ801
E(12-15)	to PAB(60-63)	RQ801
E(08-11)	to PAB(60-63)	RQ801
Q(04-15)	to PAB(52-63)	RQ811
Q(20-31)	to PAB(52-63)	RQ811
Q(36-47)	to PAB(52-63)	RQ811
Q(52-63)	to PAB(52-63)	RQ811

Figure 4-19. Parallel Adder Half-Sum Check Troubleshooting

4.17 REPETITION OF SELECTED ROS WORD

When the CE is not in the stop loop, the ROS TRANSFER pushbutton is not operative. It is often useful to repeat a ROS word when not in the stop loop; e.g., after having single-cycled up to a specific ROS address. This would normally be done when the results from the ROS word to be repeated are dependent upon the functions of previous ROS words. The following procedure may be used:

1. Set up address of desired ROS word in ROS ADDRESS COMPARE switches.
2. Place ROS ADDRESS switch in RPT position.
3. Place RATE switch in PROCESS.
4. Depress START. Desired ROS word is now being repeated.

4.18 CLEARING WAIT BIT

Three methods of clearing the wait bit in the current PSW are given here:

1. Store all zeroes in storage location zero and depress PSW RESTART.
2. With zeroes in S, repeat ROS address 9B4 (PSW bit 0 to 39).
3. The following method clears the wait bit without executing any instructions:
   a. Depress STOP.
   b. Place RATE switch in INSTRUCTION STEP.
   c. Ensure that bit 14 of word at storage location zero is a zero.
   d. Depress PSW RESTART.
   e. Depress SYSTEM RESET.
   f. Place RATE switch in PROCESS.

4.19 DETERMINING TRIGGER BEING TESTED BY FLT

1. To determine which buffer is being used, observe the BUFFER 1 indicator:
   On = buffer at 100
   Off = buffer at 200
2. Observe MASK and MCW (108 or 208):
   a. MASK indicates which bit in scanned out word is being tested.
   b. MSW (21–25) indicates which word will scan out to T. (The field is treated as a five-bit binary counter; e.g., 10011 = word 19.) Refer to LADS pages A6521–A6561 to determine which triggers will scan out.
   c. MCW(4), the LETHF trigger, determines which word of doubleword will scan out to T:
      On = bits 0–31
      Off = bits 32–63
   d. MCW(7), ERSLT trigger, determines whether scanned out trigger should be on or off.
3. The test may be restarted, after examining buffers, as follows:
   a. TEST MODE switch to FLT and REPEAT.
   b. Set up ROS address AD2 in ROS ADDRESS COMPARE switches.
   c. Depress ROS TRANSFER.

4.20 REPETITIVE CONSOLE PUSHBUTTON OPERATION

The operation of some console pushbuttons can be made repetitive by installing a jumper from 02C-B4L2D04 (logic page DS122) to ground and holding the pushbutton depressed. The following pushbuttons are affected: STORE, DISPLAY, SET IC, START, and ROS TRANSFER.

A 16-ms pulsed operation can be obtained from these pushbuttons by adding a jumper from 02A-C2D6D04 (logic page ID601) to 02E-E2F7D04 (logic page KW011) and holding the pushbutton depressed.

4.21 I/O SCOPING LOOP

The four-instruction loop shown in Figure 4-20 can be keyed into storage and is helpful in troubleshooting I/O problems. It provides a repetitive SIO.

If more than one operation is desired, specify chaining in the CCWs. If the problem is a control unit hang condition, it is helpful to store the address of the first instruction at location zero and use PSW RESTART or PULSE MODE. In the example shown, this address is hex 200.

4.22 SERVICE TECHNIQUES USING OSCILLOSCOPE

The Tektronix* 453 oscilloscope can be used in combination with the CE latch card (PN 5801358) as an input to SLT logic. This is done by using the +GATE outputs from the scope as inputs to the high impedance legs of the latch card. There are two +GATE outputs, one for each trace (A and B). These gates are active during their associated sweep and produce 0 to 12V signals. The –Sync output of the CE latch card can be dotted with any normal SLT logic circuit (except long line emitter followers), permitting the 453 gate outputs to control SLT logic.

Two typical examples of the use of this technique follow:

*Trademark of Tektronix, Incorporated.

Storage Location (Hex)	Assembly Language		Machine Language	Comments
	OP	Operands		
48	DC	X'00001000'	00001000	CAW
200	TIO	XXX	9D000XXX	TIO to device XXX
204	BC	7,200	47700200	Loop on TIO till available.
208	SIO	XXX	9C000XXX	SIO to device XXX
20C	B	200	47F00200	Unconditional branch
1000	CCW	----------	----------	CE may put any desired CCW's at this location.

Figure 4-20. I/O Scoping Loop

Example 1. To impulse an SLT line with a pulse of controlled frequency and duration. This can be used for simulating pushbuttons and resets, stepping counters, and triggering singleshots.

1. Wire output of +B gate to +high impedance input.
2. Ground reset line of CE latch card.
3. Wire –Sync output of latch card to SLT line to be activated. Use as short a wire as possible for this connection.
4. Allow scope to auto-trace.
5. Place scope in A Intensified By B mode.

The frequency of the pulse will be determined by the A-sweep speed. The duration will be determined by B-sweep speed.

Example 2. An output of a ROS field decode is found to be intermittently coming up when it logically should not. However, the same decode line occurs legitimately three other times while cycling the failing loop. The problem is to find which ROS address is producing the extra decode.

1. Allow original sync to continue to trigger A-sweep.
2. Place scope in A Intensified By B mode.
3. Position bright spot on scope so it overlaps only the extra decode.
4. Wire output of B gate to +high impedance input of CE latch card.
5. Wire decode line in question to another leg of AND circuit.
6. Wire –Sync output to some point that will freeze the machine. The machine will stop when the extra decode occurs, and the ROS address backup register will indicate the ROS word that developed the extra decode.

Another service technique is to use the Add Algebraic feature as an AND function for internal sync.

4.23 MICROPROGRAM DIAGNOSTIC

The microprogram diagnostic may be used to locate a failure of CE registers or data flow paths. To start the program, ROS transfer to address FAA (CE must be in state 0 or 1 and in manual mode to ROS transfer). The program will loop on itself, alternately using an all 0's and an all 1's pattern to transfer from one register to another. Set ADDRESS key 29 on to cause the program to load data from DATA keys (0–63) instead of using all 0's, all 1's patterns.

Set CHECK CONTROL switch to STOP position to stop on an error (active only in state 0). Failures show up as adder checks, local store bus checks, SDBI checks, E-register parity errors, ROS parity errors, or multiply decode parity errors. The following registers and functions are tested: S, T, A, B, Local Store, K, D, IC, F, G, Select, External, DAR Mask, M, N, Q, R, E, and multiple decode.

If parity errors occur in Q, R, N, or E registers due to residual bad parity in Q or LM, set ADDRESS key 30 on to cause the program to load good parity. The CE must have an SE configured to use this option. Refer to CLD AA001.

4.24 ANALYZING IMPRECISE INTERRUPTS

An imprecise interrupt can be defined as one which does not provide all the information pertinent to the interrupt. This is normal under certain conditions. However, when imprecise program interrupts occur, it is sometimes difficult to find the instruction which caused the interrupt. The following is an example. Given the following coding in which a store into a protected area is followed by an unconditional branch:

Location	Coding
100	ST1,200(2)
104	BCF,300

The program old PSW will contain:

System mask	N/A
Key	Greater than zero
AMWP	N/A
Interruption code	00 04
ILC	00
CC	N/A
Prog Mask	N/A
Instruction address	300

In this example, the instruction length code (ILC) is unknown, and the instruction address is not pointing to the instruction following the one which caused the interrupt. There is no way to trace the source of the problem from this information.

The following service technique may be used: float pin 02E-C3F4D04 (logic page KM831). This will cause a storage address protect (SAP) delay (ROS address 02E) every time a store is executed.

CAUTION

Do not leave this condition on the CE as it will cause jobs to run slower than normal.

4.25 ALD AND CLD INDEX

LADS page A6011 is an index reference for ALDs, and LADS page A6021 is an index reference for CLDs.

This Chapter is divided into two sections: Section 1 describes the maintenance procedures for the CE prime power; i.e., power supplies, regulators, converter/inverter. Section 2 describes the maintenance procedures for the CE battery backup power; i.e., battery charge circuits, line sense and switching circuits, bootstrap power supply, and battery pack.

Note: For a detailed theory discussion of CE power, refer to Chapter 2 of 9020 D/E Power Controls and Distribution Manual.

Before making changes, resistance measurements, or replacements, be sure all power is off and all capacitors are fully discharged; do not rely on bleeder resistors. Never work alone. If in doubt: Don't!

Figure 5-1 shows the ac power distribution for the CE. Note that normal power-off does not turn off the 28V ac, the 24V dc sequencing and EPO power, the 25V dc bias power, or the 115V ac to the convenience outlets. Set CB1 off (primary input) or turn off the primary wall power switch to remove these voltages.

5.1 VISUAL INSPECTION AND CLEANING

DANGER
Before the CE primary power system is inspected or cleaned, the CE should be powered down and CB1 tripped. Lethal potentials exist within the unit whenever power is on.

The CE power system is inspected for:
1. Loose or damaged wiring.
2. Burned or pitted contacts on relays and contactors.
3. Loose or maladjusted cams on the MC assemblies.
4. Dust accumulation. (Dust should be removed with a vacuum cleaner.)

5.2 MARGINAL CHECKING

The marginal checks are performed by running the FLTs and diagnostic programs with all 6V marginable power supplies in the CE varied by 5.5V and 6.5V and with ROS voltage varied to 80% of nominal. The procedure is as follows:
1. With the CE in state 0 and the TEST switch in TEST position, and configured to a subsystem, load applicable FLT/ROS or diagnostic program.
2. Select a gate (GT) or select ROS with the MARGIN/METER SEL rotary switch.
3. Vary the selected voltage with RAISE-LOWER potentiometer to limits stated above.
4. If FLT/ROS or diagnostic program does not reveal a malfunctions while operating under marginal voltages, return the power supply voltages to normal. Rotate FREQUENCY ALTERATION switch to ENABLE position and rerun the tests.

5.3 VOLTAGE CHECKS AND ADJUSTMENTS

With the CE in state 0 and the TEST switch in TEST position, measure the dc voltages at the locations specified in Table 5-1(a and b). Use 0.5% precision meter. (The voltage readings at the power supply regulators will be higher than at the gates.) If any voltage is out of tolerance, readjust as described in 5.3.1 through 5.3.3. (These adjustments are applicable to all power supplies except ROS. For adjustment on the ROS supply, refer to heading 4.9.)

After all voltages have been adjusted, the system control panel voltmeter may be calibrated. Measure all marginal power supply voltages with the system control panel voltmeter, and record in Figure C-1 of Appendix C. This information is for future reference in interpreting the system control panel voltmeter readings and should be kept with the CE.

5.3.1 Regulator Output Adjustment

Set the dc voltages by adjusting the potentiometer on the Amplifier Assembly card or on the associated panel control of the marginable regulators. All regulators with a single logic pin location listed in Table 5-1 are measured at that location. All regulators with more than one logic pin location listed in Table 5-1 are measured and adjusted accroding to the following formula:

$$S = \left(\frac{H-L}{2}\right) + N$$

where: N = listed nominal voltage
H = highest measured voltage
L = lowest measured voltage
S = voltage to be set at the logic pin with the highest measured voltage

The adjustment procedure for regulators with multiple pin locations may be implemented (in Table 5-1) as follows:
1. Measure voltage at each logic pin location.
2. Subtract lowest voltage reading (L) from highest (H).
3. Divide result of step 2 by 2.
4. Add result of step 3 to nominal voltage listed (N).
5. Measure voltage at logic pin with highest voltage reading (H).

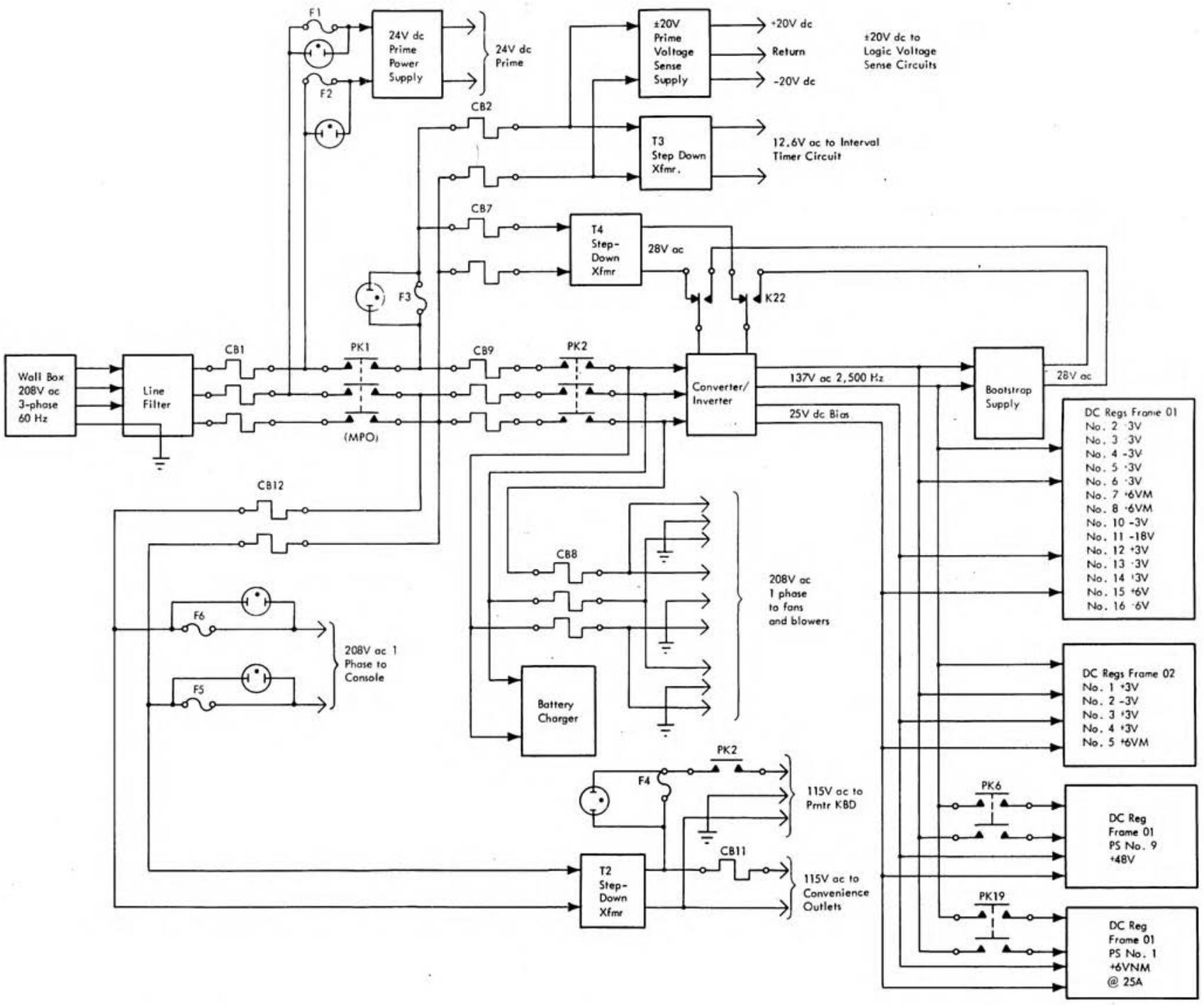


Figure 5-1. AC Power Distribution

Table 5-1(a). DC Distribution, PDU 1

Regulator	Nominal Output	Logic Page	Laminar Bus			Voltage Measurement Location
			Gate	Pin Voltage	Pin Return	
PS1	+ 6V 25 amp	YA061	C/D upper	12	11	02C-E2G7B11
			E upper	6	5	02E-A1G1E09
PS2	+ 3V 40 amp	YA062	B lower	8	7	02B-D3G2D03
PS3	+ 3V 40 amp	YA061	E lower	8	7	02E-D3G2D03
PS4	- 3V 40 amp	YA062	C/D upper	10	9	02C-E2G7B06
			C/D lower	10	9	02C-D3G2B06
PS5	+ 3V 40 amp	YA062	E upper	8	7	02E-B2G2D03
PS6	+ 3V 40 amp	YA062	C/D upper	4	3	02C-E2G7D03
			C/D lower	8	7	02C-D3G2D03
PS7*	+ 6V 40 amp	YA061	E upper	12	11	02E-D2G6B11
			E lower	12	11	02E-B4G6B11**
PS8*	+ 6V 40 amp	YA062	C/D lower	12	11	02C-D3G2B11**
PS91	+48V 2 amp	YA141	01C BB 9A	1	Capacitor C2A	01C BB 9A
PS10	- 3V 40 amp	YA072	A upper	10	9	02A-C1G2B06
			A lower	10	9	02A-D3G2B06
			B upper	10	9	02B-B1G2B06
			E upper	10	9	02E-B1G2B06
			E lower	10	9	02E-D3G2B06
PS11*	-18V 11 amp	YA071	C/D upper	6	5	Gate C/D upper - 6**
PS12	+ 3V 40 amp	YA072	A lower	12	11	02A-C4G6D03
PS13	+ 3V 40 amp	YA071	B upper	8	7	02B-B1G2D03
PS14	+ 3V 40 amp	YA072	A upper	12	11	02A-C1G2D03
PS15*	+ 6V 40 amp	YA071	B upper	12	11	02B-A1G2B11
			B lower	12	11	02B-B4G6B11**
PS16*	+ 6V 40 amp	YA072	A upper	8	7	02A-C1G2B11**
			A lower	8	7	02A-C4G6B11

Table 5-1(b). DC Distribution, PDU 2

Regulator	Nominal Output	Logic Page	Laminar Bus			Voltage Measurement Location
			Gate	Pin		
				Voltage	Return	
PS1	+3 40 amp	YA301	A lower	6	5	02A-B3G2D03
			B upper	6	5	02B-D1G2D03
			B lower	6	5	02B-D4G2D03
PS2	- 3 40 amp	YA301	B lower	10	9	02B-D4G2B06
			K	10	9	02K-C2G2B06
			L	10	9	02L-C2G2B06
PS3	+3 40 amp	YA301	L	8	7	02L-C2G2D03
PS4	+3 40 amp	YA301	K	12	11	02K-C2G2D03
PS5*	+6 40 amp	YA301	K upper	8	7	02K-C2G2B11
			L upper	12	11	02L-C2G2B11

* Marginable regulator.
** Use this point for voltage-limit measurement.
† PS9 may not be installed.

6. Adjust potentiometer on Amplifier Assembly card (of nonmarginable regulators) or on associated panel control (of marginable regulators) for voltage reading (step 5) equal to result of step 4 (S).
7. Perform adjustments 5.3.2 through 5.3.4 for all marginable regulators that require adjustment. It is advised that all steps be performed for one regulator before proceeding to the next regulator to avoid changing meter leads.

5.3.2 Regulator Overvoltage Trip Adjustment

Overvoltage sensing internal to each regulator is executed by the Overvoltage/Overcurrent card.

The marginal power supplies have an adjustable "ax" assembly to permit an accurate overvoltage trip point. Adjust as follows:

1. Loosen setscrew of clockwise limit collar on associated potentiometer (Figure 5-2, A).
2. Using voltmeter (0.5% or better), measure voltage at appropriate logic pin as listed in Figure 5-2, B.
3. Rotate panel control shaft until voltage listed in Figure 5-2, B, under "ax" is obtained.
4. Using a small screwdriver, very slowly decrease potentiometer setting of "ax" assembly on the regulator until power drops.
5. Turn panel control to a lower setting, and recycle power on.

5.3.3 Voltage Limit Stop Adjustment

Limit stops of voltage RAISE-LOWER potentiometers are set as follows:

1. Using voltmeter (0.5% or better), measure voltage at appropriate logic pin as listed in Figure 5-2, B.
2. Rotate panel control until voltage listed under "Limit Stop, Upper" is obtained.
3. Loosen setscrew of clockwise limit collar on associated potentiometer and rotate collar clockwise (as viewed form front of panel) until pin on collar rests on collar stop. Tighten setscrew.
4. Rotate panel control until voltage listed under "limit Stop, Lower" is obtained.
5. Loosen setscrew of counterclockwise limit collar and rotate collar counterclockwise until pin on collar rests on collar stop. Tighten setscrew.

5.3.4 MARGIN ACTIVE Indicator Switch Adjustment

Adjust the margin control locate collar, shown in Figure 5-2, A, as follows:

1. Using voltmeter (0.5% or better), measure voltage at appropriate logic pin as listed in Figure 5-2, B.
2. Loosen setscrew of margin control locate collar.
3. Rotate panel control potentiometer until a 46V reading or the nominal reading for ROS is obtained. (ROS nominal reading is determined by procedure in 4.9 and is recorded on chart of Figure C-1.)
4. Rotate margin control locate collar until MARGIN ACTIVE indicator goes out. (The follower falls into the notch on the collar and the switch opens.) Tighten setscrew on collar.

5.4 TROUBLESHOOTING

The troubleshooting procedures are described in three parts: Power Supply Protection Circuits, Converter/Inverter, and Regulators.

5.4.1 Power Supply Protection Circuits

The following paragraphs describe the power supply protection circuits used in the CE: circuit interlocks, voltage sensing circuits, overcurrent sensing circuits, and thermal sensing circuits.

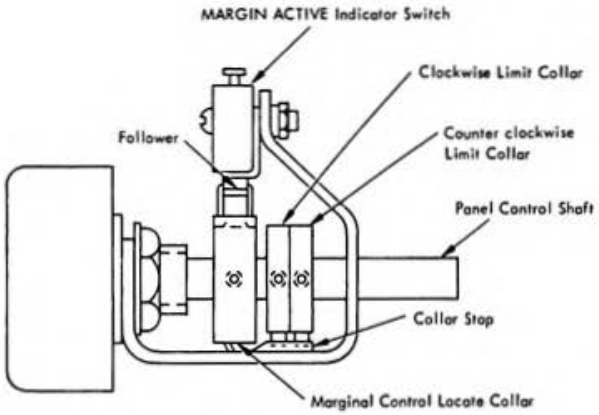
5.4.1.1 Voltage Sensing Circuits

The voltage sense relayd (ALD YA111) are energized when all dc voltage outputs from the regulators are present. If one or more of the dc regulators do not have an output, K10 (+ regulators) or K11 (– regulators) will not be picked and power will be dropped approximately 10 seconds after power on was initiated. Use the UNDER VOLTAGE CHECK switches on the CE power panel to locate the failing regulator. Each switch isolates the indicated regulator from the undervoltage sense circuit. Switch off all UNDER VOLTAGE CHECK switches and cycle power on. Switch in one regulator at a time until power drops, indicating the faulty unit. Reset the switch to off and recycle power on. Measure the output voltage of the regulator to ensure that the latter is not at fault. If it is at fault, refer to heading 5.4.3 for repair procedures.

Overvoltage sensing is internal to each regulator and is executed by the Overvoltage/Overcurrent card. Refer to heading 5.3.2.

5.4.1.2 Overcurrent Sensing Circuits

An overcurrent condition will cause a power-down sequence. An overloaded regulator will be indicated by the indicator lamp on its Overvoltage/Overcurrent card. Refer to heading 5.4.3.



(A)

Panel Control	Regulator	Logic Pin	Voltage Setting		
			"ax"	Limit Stop	
				Upper	Lower
+6M A GT	PS16	02A-C1G2B11	6.9V	6.5V - 6.7V	5.3V - 5.5V
+6M B GT	PS15	02B-B4G6B11	6.9V	6.5V - 6.7V	5.3V - 5.5V
+6M C GT	PS8	02C-D3G2B11	6.9V	6.5V - 6.7V	5.3V - 5.5V
+6M E GT	PS7	02E-B4G6B11	6.9V	6.5V - 6.7V	5.3V - 5.5V
ROS	PS11	*	22.0V	20.0V - 20.3V	6.8V - 7.0V

*Use pin 6 on gate C/D upper laminar bus.

(B)

Figure 5-2. Marginal Check Potentiometer Adjustment Limits

5.4.1.3 Thermal Sensing Circuits

The CE power panel has thermal trip indicators to signify the location of an overtemperature condition. When such a condition exists, check whether there is proper air flow through the area, fans are running, filters are clean and not obstructed, and the exhaust area is not blocked. If the air flow is proper, locate and replace the component that is overheating. Check for the cause of the overheating. Also check the accuracy of the sensing elements; one may have changed the point at which it opens. The warning thermals for logic gates are designed to open at 122°F and for PDU at 130°F. The catastrophic thermals for logic gates are designed to oepn at 134°F and for PDU at 140°F.

The thermal indicators may be reset by depressing THERMAL RESET on the CE power panel. If any indicator does not reset, check the indicator relay and diode from the reset line (ALD YA022).

5.4.2 Converter/Inverter

DANGER
The internal circuitry of the converter/inverter is not isolated from the power source; therefore, a lethal potential to ground is present whenever power is on. Exercise extreme caution. This potential exists on the SMS cards, heatsinks, and terminals to the regulators.

For the safety reasons stated above, maintenance is limited to the following:
1. Fuse and SMS card replacement.
2. SCR gate signal frequency adjustment.
3. Cleaning and checking for loose connections.
4. Air flow checks, including the fan.
5. Replacement of the entire converter/inverter.

Converter/inverter failures almost always show one of the following symptoms:
1. The fuses blow immediately when power is applied.
2. The input circuit breaker (C/I-CB2) trips almost immediately when power is applied.
3. The fuses blow when the load is applied (as C/I-K3 picks).
4. The fuses blow after operating briefly.

The first two symptoms imply an internal failure; the third, excessive regulator loading; and the fourth, a thermal condition. Upon the appearance of any of these symptoms, be sure the power is off and then replace the fuses.

CAUTION
Always replace both fuses at the same time with high-speed, 50-amp, form 101 fuses, PN 5261451.

With power still off, check the SCR gate signals and verify that the fan is running, the air input is not obstructed, and the exhaust area is not blocked.

The SCR gate signals are generated with the 28V ac bias power source and are observed with normal power off. Remove the cover over the SMS cards. Set the oscilloscope to add the inputs algebraically and invert input B. (Input B becomes the reference.) Observe the waveshapes shown in Figure 5-3 at the test points noted. The card in J9-2 drives SCR1, SCR5, and SCR6. The card in J9-3 drives SCR2, SCR3, and SCR4. If the frequency is not 2500 Hz (400 usec, leading edge to leading edge), adjust the potentiometer on the Magnetic Oscillator card in J9-1. Replace the cards if these tolerances are not met.

If the SCR gate signals are normal and the symptoms still exist, remove the entire regulator load (P2, P3, P4, and P5) and then cycle power on.

If the symptoms still exist, replace the entire converter/inverter (heading 5.5.1). If symptoms do not exist, replace the regulator connectors, one at a time, cycling power each time, until the symptoms reappear. See Figure 5-4 to determine which regulators are powered by the connectors.

Once the connector has been identified, disconnect the regulators supplied by it. Be sure all power is off. Reconnect the regulators, one at a time, cycling power each time, until the faulty regulator is isolated. Refer to heading 5.4.3 to isolate regulator malfunctions.

If trouble cannot be traced to a regulator malfunction, measure the 25V dc bias voltage [C/I-TB1-4 (positive) and -5 (negative)]. If the bias is off, check the 28V ac input, the Rectifier cards in J9-4 and J9-6, and the Contactor Driver card in J9-8. The GATES ON indicator should be on. If the bias is on, with the correct polarity, inspect the contactors for dirt or oxide; burnish the contacts, if necessary. [C/I-K2 picks when C1–C8 have charged to a total potential of approximately 150V dc. C/I-K1 and -K3 pick as C/I-K2 transfers. C1–C8 surge protection resistors (R12, R13, and R14) are shorted by C/I-K1 contacts. C/I-K3 contacts apply the load to the C/I.]

5.4.3 Regulators

DANGER
The input terminals of the regulators are not isolated from the power source; therefore, a lethal potential to ground is present whenever power is on. Exercise extreme caution.

The power supply regulators are floating supplies and must not be grounded to the frame. The regulators are isolated by two captive mounting screws in nylon standoffs on each regulator. If possible, limit maintenance to the following:
1. SMS card replacement.
2. Output voltage adjustment.

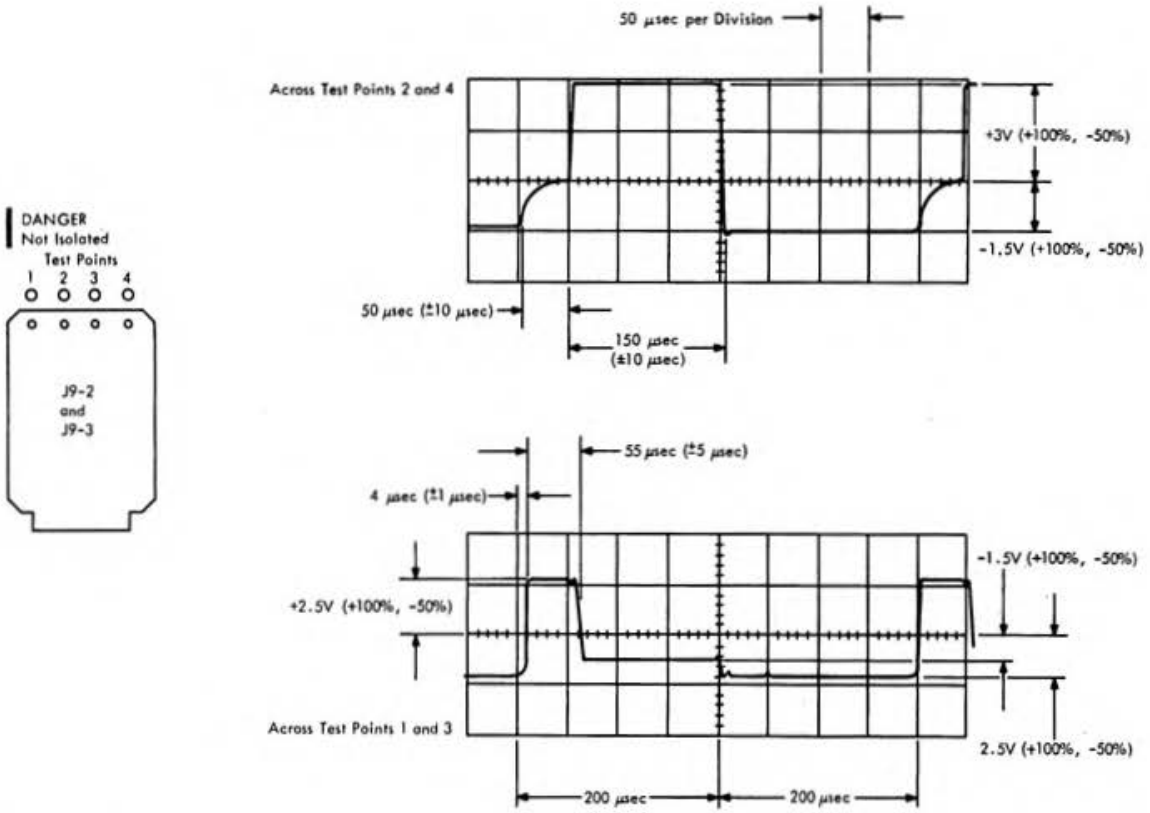
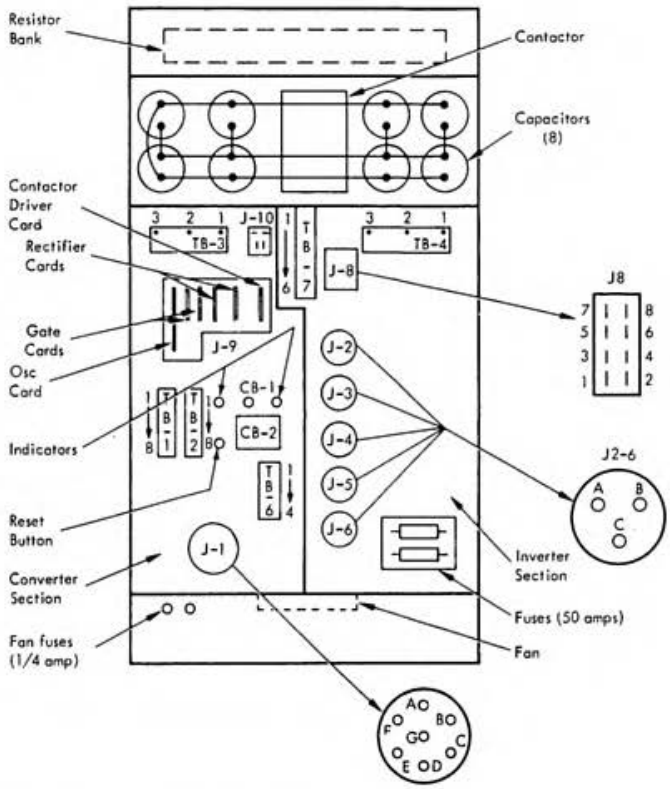


Figure 5-3. SCR Gate Signals (Converter/Inverter)



DANGER

Use extreme caution when working on the converter-inverter. High voltages are present throughout the converter-inverter tub assembly, including the heat sinks that are floating and the SMS cards.

Connector Loading PDU I

Connector	Power Supply Load
P2	PS1 PS3 PS5 PS7
P3	PS2 PS4 PS6 PS8
P4	PS9 PS11 PS13 PS15
P5	PS10 PS12 PS14 PS16

Connector Loading PDU II

Connector	Power Supply Load
P6	PS1 PS2 PS3 PS4 PS5

Figure 5-4. Converter/Inverter

3. Cleaning and checking for loose connections.
4. Air flow checks.
5. Resistance measurements.

Be sure that all power is off and all capacitors are fully discharged; do not rely on the bleeder resistors. Two types of regulators are used in the CE. One is the SCR-controlled output; the other is the magnetic-amplifier-controlled output. The 18V dc ROS regulator (PS11) is of the first type; the others are of the second type.

5.4.3.1 SCR Regulator

A regulator malfunction may be due to an undervoltage, overvoltage, or overcurrent condition. If an undervoltage condition exists within the regulator, proceed as follows:
1. Turn off power.
2. Replace Magnetic Amplifier card (socket A), cycle power, and check for normal output.
3. Replace Differential Amplifier card (socket B), cycle power, and check for normal output.
4. Turn off power and set CB1 off.
5. Remove the three SMS cards.
6. Remove all cables at output positive and negative terminals, including jumpers to TB1.
7. Make resistance measurements between points shown in Figure 5-5. Be sure capacitors are fully discharged by measuring voltages at these points first. Use R x 1 scale for resistance measurements.

   Note: Remember that a good diode has high resistance in one direction only, but a good SCR has high resistance in both directions.

If an overvoltage or overcurrent condition exists within the regulator, proceed as follows:
1. Turn off power.
2. Replace Overcurrent/Overvoltage card, cycle power, and check for normal output. If power remains up and is normal, check reed relay on old card to see if improper seating and poor contact made card fail. If power drops, proceed as described for undervoltage condition above.

Replace the regulator if the failing component(s) is not found.

5.4.3.2 Magnetic-Amplifier Regulator

A regulator malfunction may be due to an undervoltage, overvoltage, or overcurrent condition. If an undervoltage condition exists within the regulator, proceed as follows:
1. Turn off power.
2. Replace Amplifier Assembly card, cycle power, and check for normal output.
3. Turn off power and set CB1 off.
4. Remove both SMS cards.
5. Remove all cables at output positive and negative terminals, including jumpers to TB1.
6. Remove cables to TB1-6 and -7.
7. Make resistance measurements between points shown in Figure 5-6. Use page that corresponds to type of regulator under test. Be sure capacitors are fully discharged by measuring voltages at these points first. Use R x 1 scale for resistance measurements.

If an overvoltage or overcurrent condition exists within the regulator, proceed as follows:
1. Turn off power.
2. Replace Overcurrent/Overvoltage card, cycle power, and check for normal output. If power remains up and is normal, check reed relay on old card to see if improper seating and poor contact made card fail. If power drops, proceed as described for undervoltage condition above.

Replace the regulator if the failing component(s) is not found.

5.5 REPLACEMENT

5.5.1 Converter/Inverter Replacement

To replace the converter/inverter:
1. Turn off wall primary power switch. All power in CPU must be off.
2. As a precaution, set CB1 off.
3. Measure voltage across capacitors to be sure bleeder resistors have reduced voltage to a safe level, preferably 0V.
4. Remove P1 through P6.

DANGER
Inverter/converter power supply, PN 5703200, should not be installed or removed before partially disassembling the unit. The total weight of the supply is 153 pounds. Proper safety procedures require that the unit be disassembled to reduce the weight of each unit to be lifted to a safe amount.

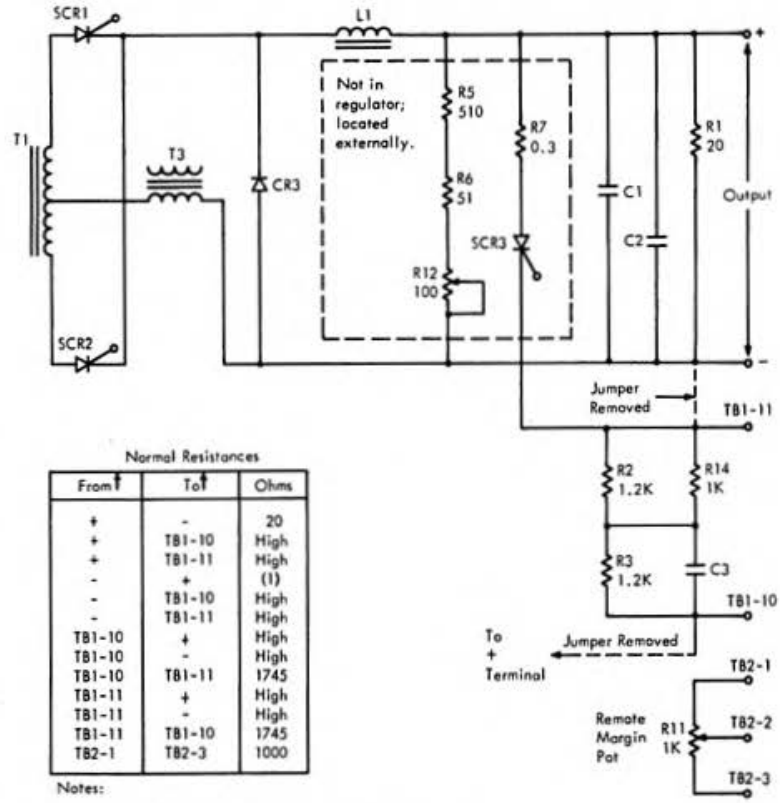
5. Remove Converter section (left box) and inverter section (right box) from assembly by disconnecting necessary wiring, removing metal stops (one at each bottom and one at each top), and sliding section out of inverter/converter assembly. Always remove inverter section (right side) before converter section. Always install converter unit before inverter unit.

6. Stand assembly on a dolly and roll it away from frame. Do not attempt to carry it.
7. Reverse this procedure to install converter/inverter assembly.

5.5.2 Regulator Replacement

To replace the regulator:

1. Turn off wall primary power switch.
2. As a precaution, trip CB1.
3. Remove terminal strip safety shields.
4. Bleed filter capacitors. Disconnect jumper wires connected to filter capacitors.
5. Disconnect and tag each external cable lead for reinstallation.
6. Remove captive mounting screws from nylon standoffs. Remove bottom screw first, then top. Note that these mounting screws are located at rear of regulators.
7. Lift out regulator.
8. Reverse this procedure to install regulator assembly.



Normal Resistances

From†	To†	Ohms
+	-	20
+	TB1-10	High
+	TB1-11	High
-	+	(1)
-	TB1-10	High
-	TB1-11	High
TB1-10	+	High
TB1-10	-	High
TB1-10	TB1-11	1745
TB1-11	+	High
TB1-11	-	High
TB1-11	TB1-10	1745
TB2-1	TB2-3	1000

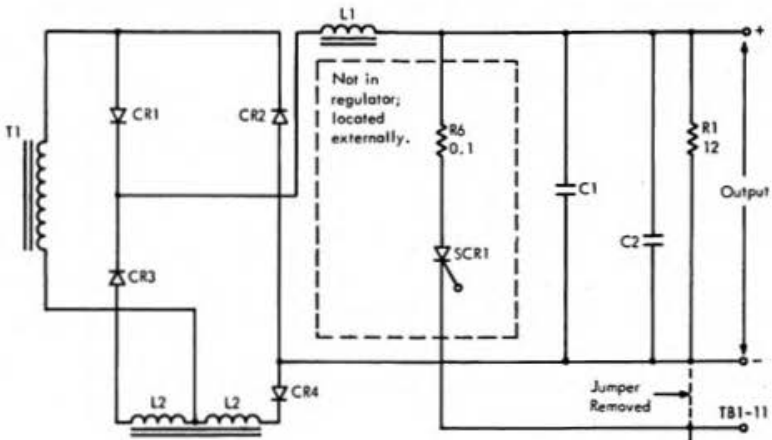
Notes:

(1) Typically 15-ohms through one diode and high if through two or more series diodes (since the meter voltage is not sufficient to break down the combination).

† From: + probe
To: - probe

18V at 11 amp regulator part number: 5709320

Figure 5-5. SCR Regulator Resistances



Normal Resistances

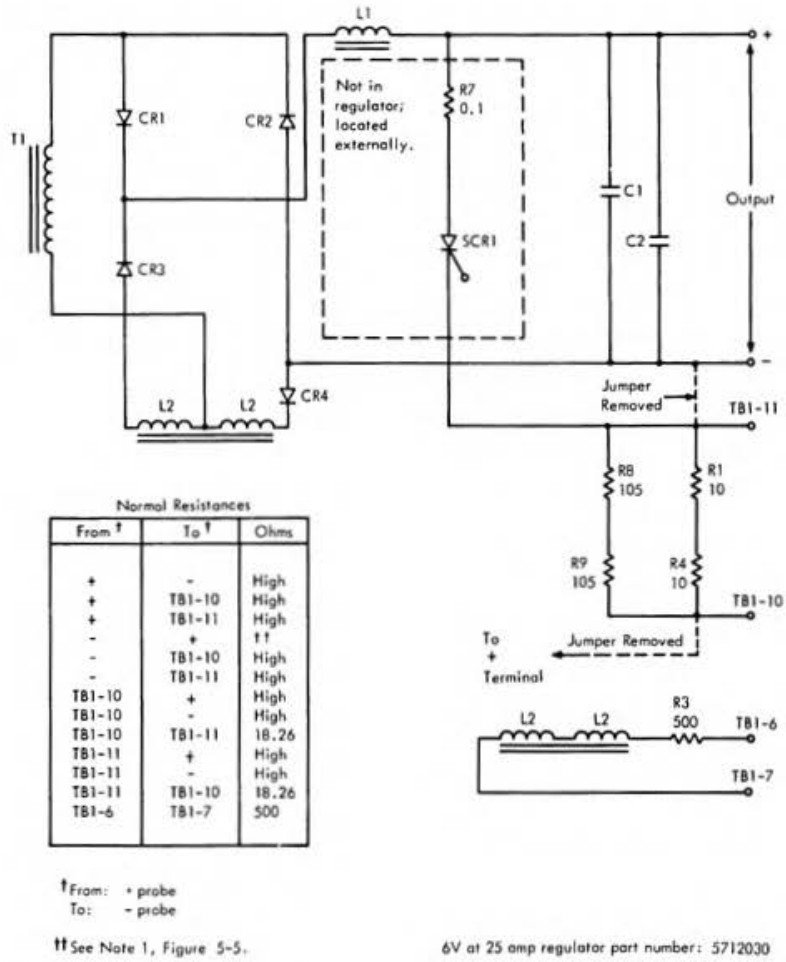
From†	To†	Ohms
+	-	12
+	TB1-10	High
+	TB1-11	High
-	+	††
-	TB1-10	High
-	TB1-11	High
TB1-10	+	High
TB1-10	-	High
TB1-10	TB1-11	High
TB1-11	+	High
TB1-11	-	High
TB1-11	TB1-10	High
TB1-6	TB1-7	620

†From: + probe
To: - probe

††See Note 1, Figure 5-5.

3V at 40 amp regulator part number: 5712020

Figure 5-6. Magnetic-Amplifier Regulator Resistances (Sheet 1 of 4)



Normal Resistances

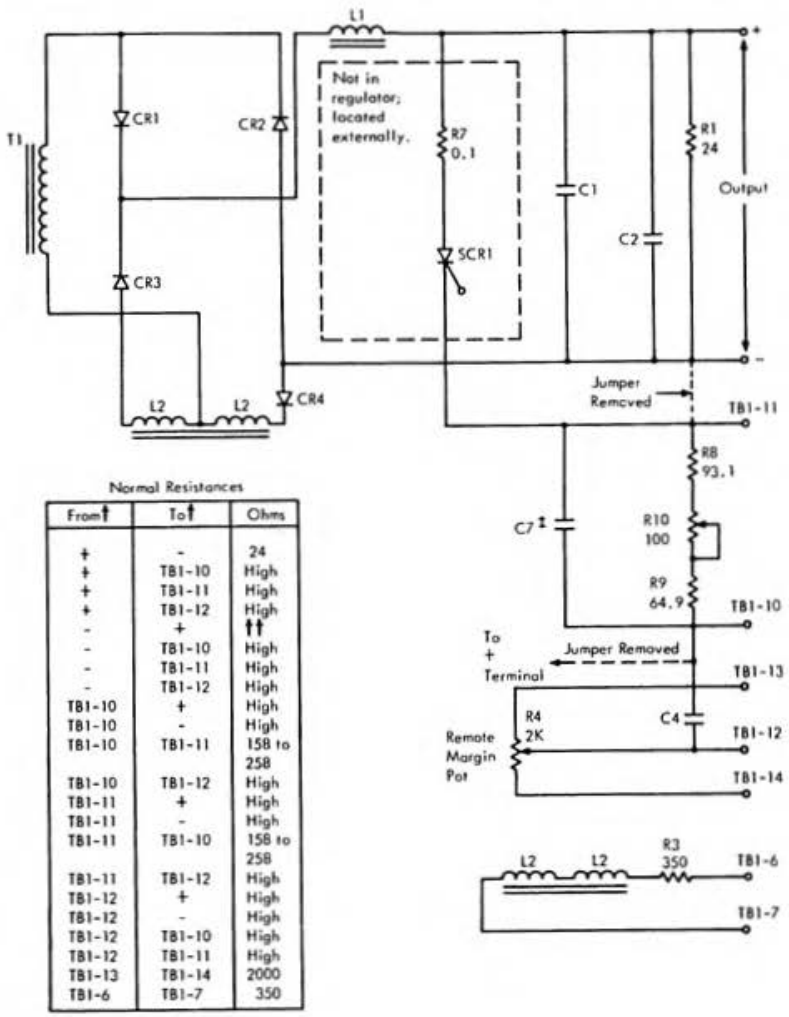
From †	To †	Ohms
+	-	High
+	TB1-10	High
+	TB1-11	High
-	+	††
-	TB1-10	High
-	TB1-11	High
TB1-10	+	High
TB1-10	-	High
TB1-10	TB1-11	18.26
TB1-11	+	High
TB1-11	-	High
TB1-11	TB1-10	18.26
TB1-6	TB1-7	500

†From: + probe
To: - probe

†† See Note 1, Figure 5-5.

6V at 25 amp regulator part number: 5712030

Figure 5-6. Magnetic-Amplifier Regulator Resistances (Sheet 2 of 4)



Normal Resistances

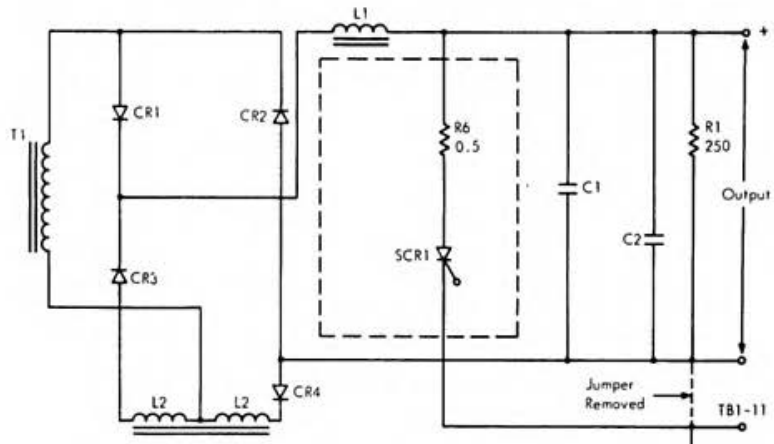
From†	To†	Ohms
+	-	24
+	TB1-10	High
+	TB1-11	High
+	TB1-12	High
-	+	††
-	TB1-10	High
-	TB1-11	High
-	TB1-12	High
TB1-10	+	High
TB1-10	-	High
TB1-10	TB1-11	158 to 258
TB1-10	TB1-12	High
TB1-11	+	High
TB1-11	-	High
TB1-11	TB1-10	158 to 258
TB1-11	TB1-12	High
TB1-12	+	High
TB1-12	-	High
TB1-12	TB1-10	High
TB1-12	TB1-11	High
TB1-13	TB1-14	2000
TB1-6	TB1-7	350

†From: + probe
To: - probe

††See Note 1, Figure 5-5.

6V at 40 amp regulator part number: 5712040

Figure 5-6. Magnetic-Amplifier Regulator Resistances (Sheet 3 of 4)



Normal Resistances

From †	To †	Ohms
+	-	250
+	TB1-10	High
+	TB1-11	High
-	+	††
-	TB1-10	High
-	TB1-11	High
TB1-10	+	High
TB1-10	-	High
TB1-10	TB1-11	1525.3
TB1-11	+	High
TB1-11	-	High
TB1-11	TB1-10	1525.3
TB1-6	TB1-7	680

†From: + probe
To: - probe

††See Note 1, Figure 5-5.

48V at 2 amp regulator part number: 5712081

Figure 5-6. Magnetic-Amplifier Regulator Resistances (Sheet 4 of 4)

DANGER
Use extreme care when working in the area of the battery packs. Lethal voltages are present. Before performing any of the tests or procedures on this page, read DANGER notice at the start of this section.

SECTION 2. CE BATTERY BACKUP POWER

DANGER
The full dc potential of the batteries is available across the red and black binding posts on the metal power-control box (inside the battery cabinet) when both battery switches are on and 24V dc is applied to the EPO contactor coil. This voltage ranges from 300V to 350V dc and can result in a dangerous electrical shock. Interrupting the 24V dc to the contactor coil, turning off both battery switches, or removal of the pull-type fuse holder removes the battery potential from the binding posts. However, if J1 is connected and the charger is active, full charger potential (450V–500V dc) is present at the binding posts even when the battery switches and contactor are inactive and the pull switch is out.

Internal to the battery packages beyond the protection of the OFF/ON switch, plastic shields PN 5447517, 5447518, and 5447519 (see heading 5.12.1) must be used for assembly, disassembly, or cell testing since nominal voltages in the range of 160V dc are always present. The caution to be observed when the cells of the battery package are exposed cannot be overemphasized. When using the insulated nut driver, avoid bridging adjacent terminals with the exposed metal end. When working on a battery pack, use the procedure described under heading 5.12.4, items 1, 2, and 3, to reduce the potential between any two adjacent trays to 25V. Safety glasses must be worn at all times.

Battery backup power is provided by a battery package which includes two packs of nickel-cadmium cells, a battery charger, and an EPO contactor assembly. The batteries are designed to maintain the CE on battery power for 6.5 seconds after a mainline power failure. The battery charger provides a 150-ma charge current to maintain the batteries in a full-charge condition. The EPO contactor assembly isolates the battery power from the rest of the SE in the event of an EPO condition.

The battery pack (PN 5713548) consists of 13 battery trays (PN 5713500) of 10 cells each. One battery pack has all 13 of these trays wired in series; the other battery pack (PN 5713549) has 12 of the trays wired in series. The unused tray may be used for spare cells if necessary. The bottom terminals of the OFF/ON switch connect to the ends of the series-wired battery. The top switch terminals connect to the external battery cable and are not at battery potential when the switch is in the OFF position. Refer to Figures 5-7 through 5-9.

5.6 BATTERY CHARGE REQUIREMENTS

For each period on-battery, a charge time equal to 300 times the on-battery time is required to recharge the batteries. The CE must not repeatedly be placed on-battery for more than a total time of 14 seconds without sufficient recharge time. Otherwise, battery damage may result.

If a battery pack, a tray, or cells in the battery pack are replaced, the CE must not be placed on-battery until sufficient time has passed for all cells to reach a full charge. The recommended time is 24 hours. Failure to allow all cells to reach an equal state of charge can lead to their destruction, with a resultant lower level of charge.

5.7 BATTERY CHARGING RATE

Refer to Figure 5-10 for a description of battery charge circuitry. The battery charging rate is adjusted as follows:

DANGER
High voltage is present on the cards in the charger. Battery charger circuits are not referenced to machine dc or frame ground.

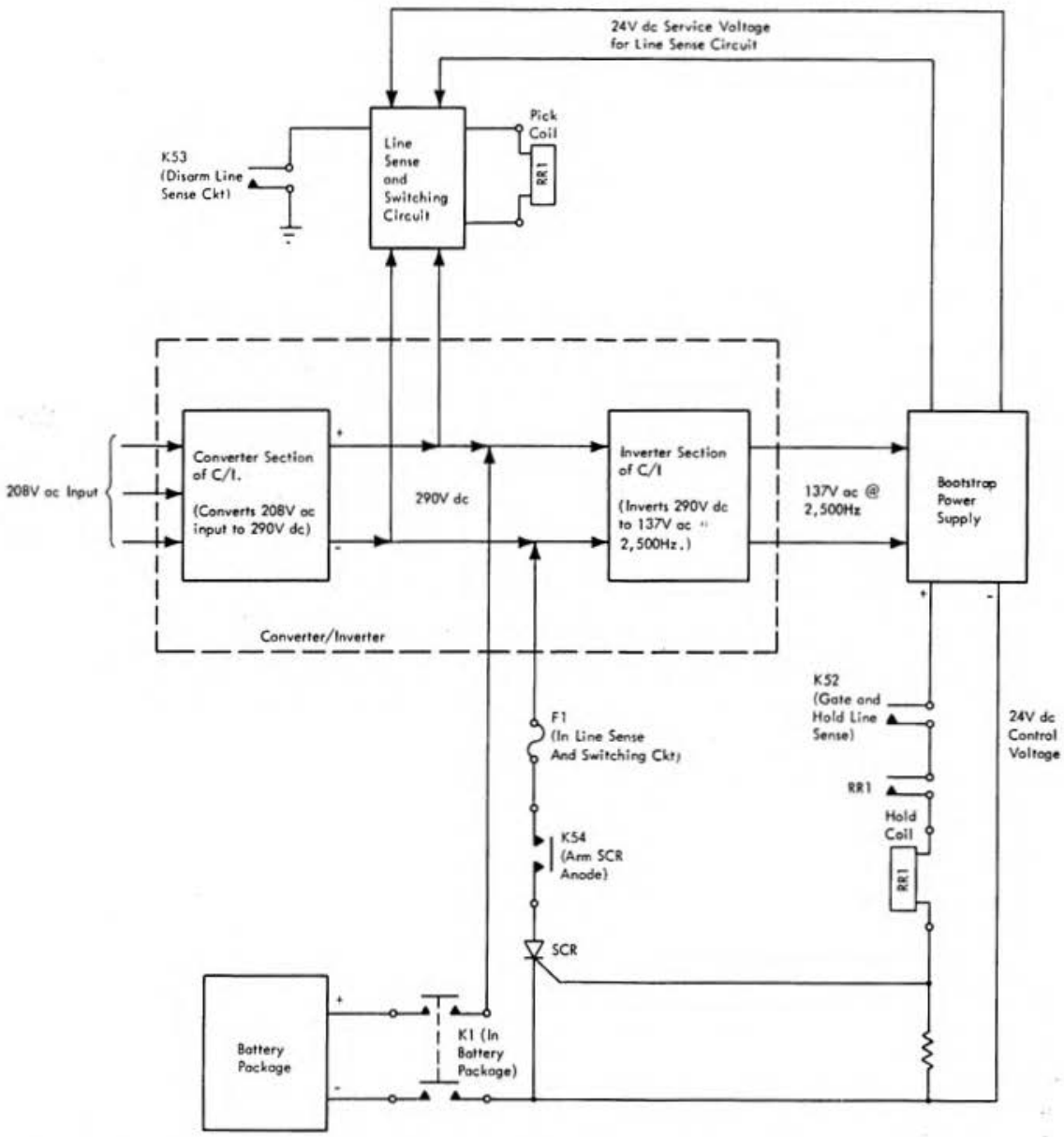


Figure 5-7. Battery Backup Block Diagram

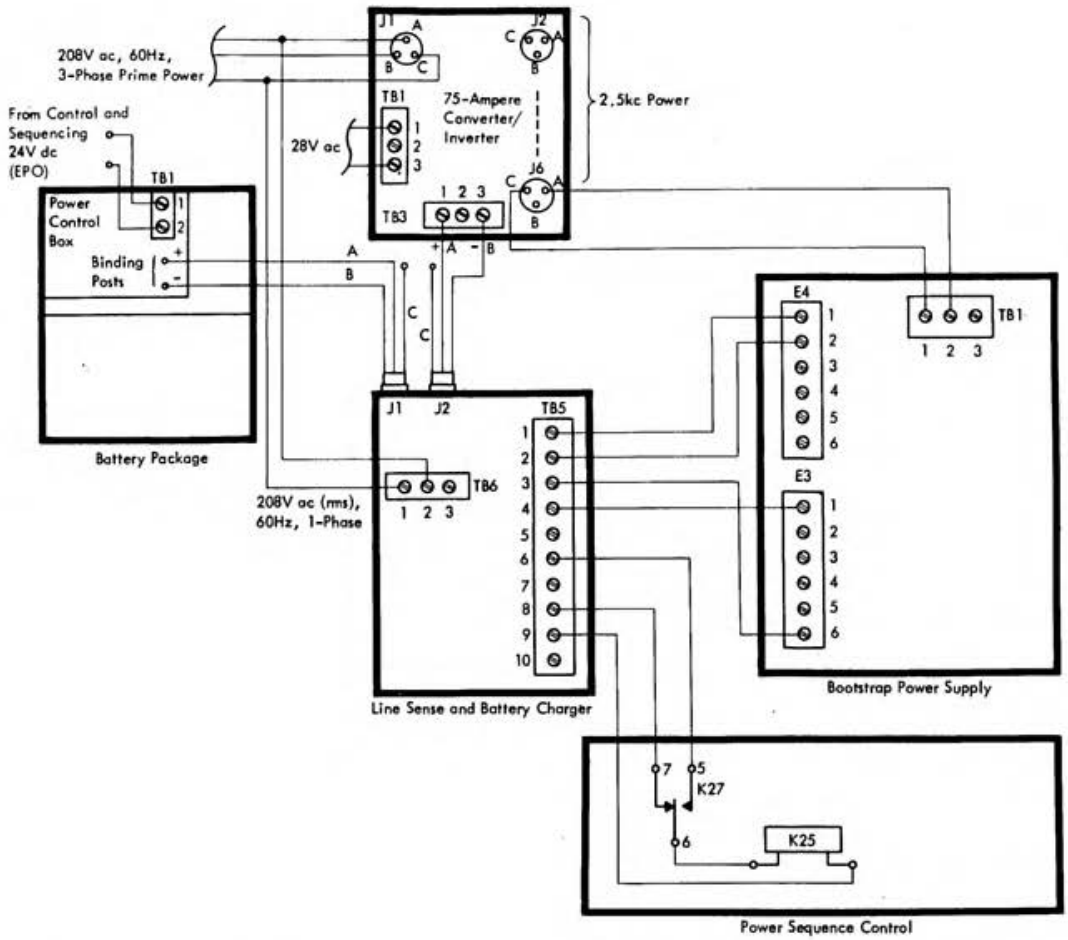


Figure 5-8. Battery Backup Interconnections

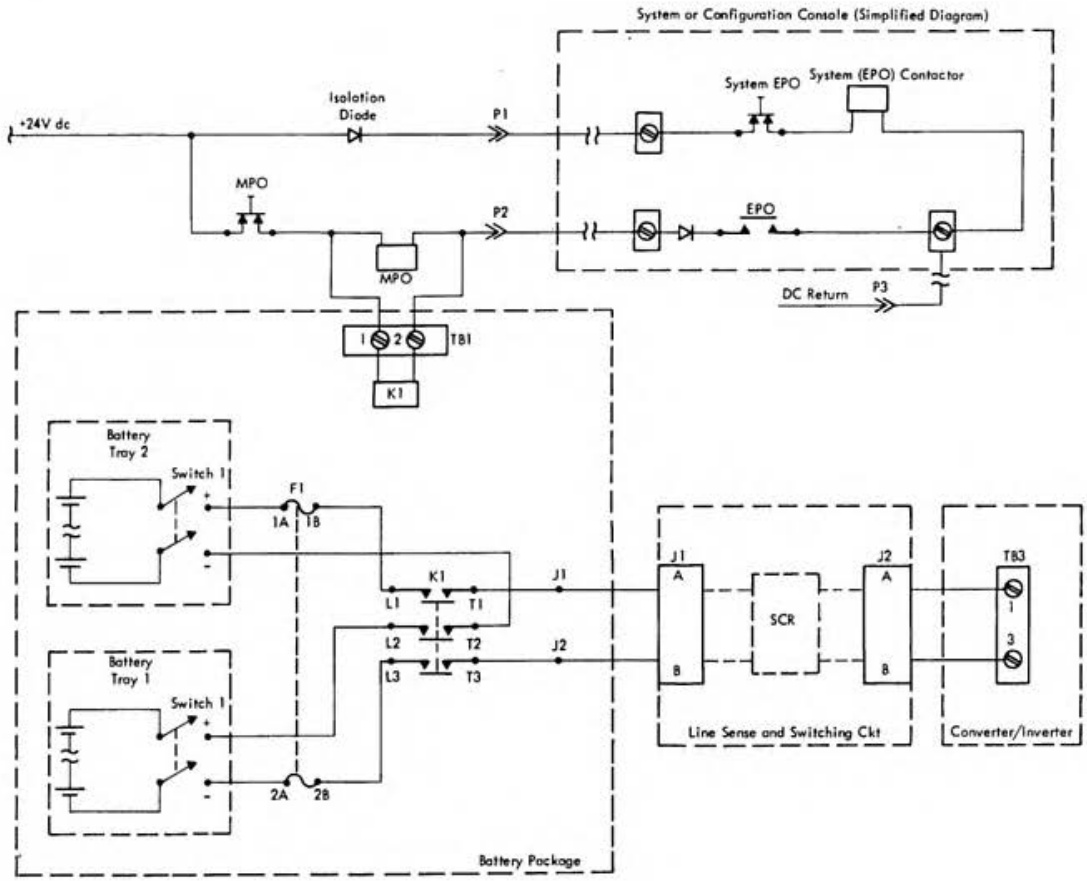
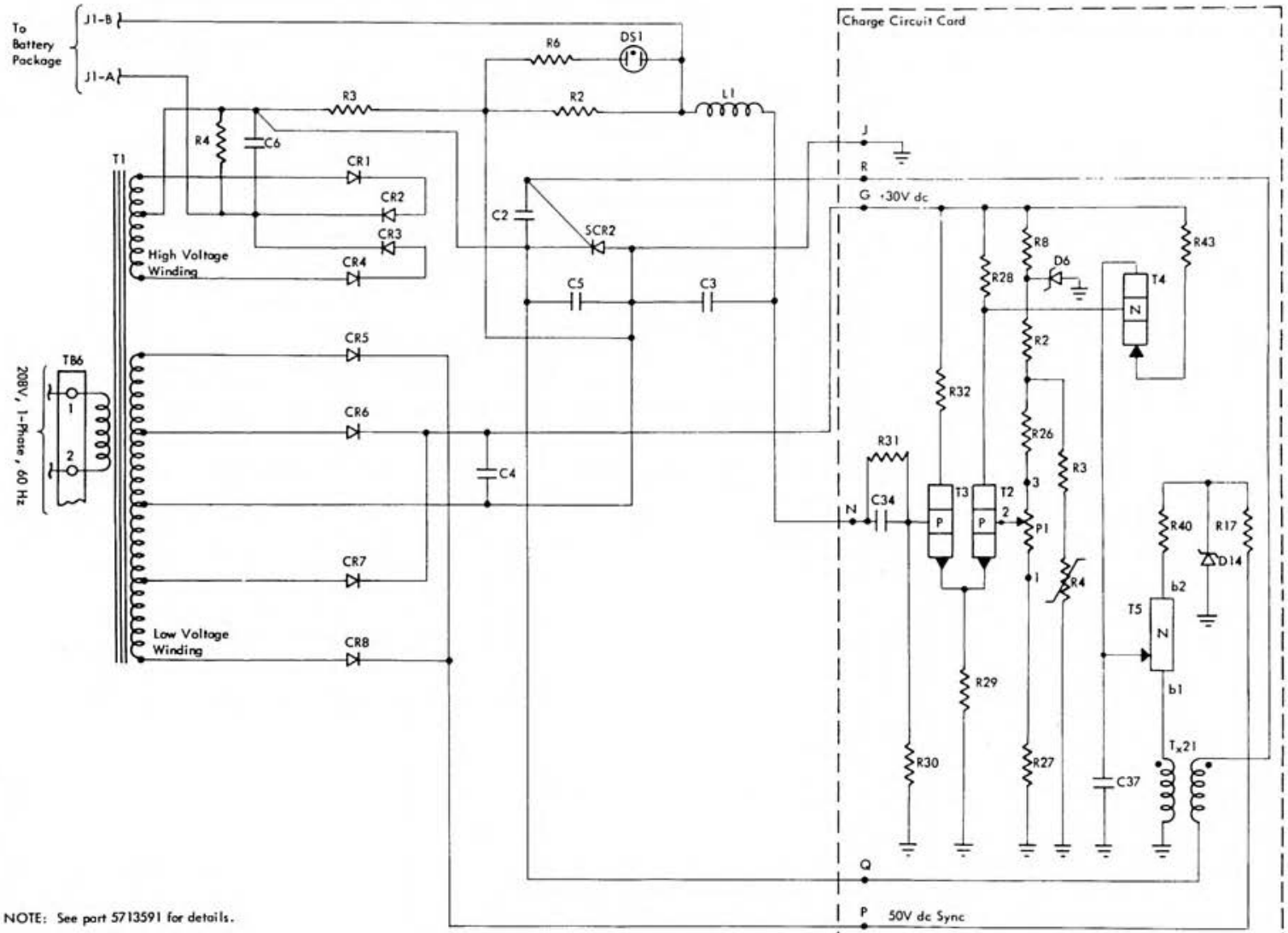


Figure 5-9. Battery Package Tie-In



NOTE: See part 5713591 for details.

Figure 5-10. Battery Charge Circuit

DANGER
Use extreme care when working in the area of the battery packs. Lethal voltages are present. Before performing any of the tests or procedures on this page, read DANGER notice at the start of this section.

1. Turn off unit power.
2. Remove battery package cover.
3. Turn both battery pack toggle switches to OFF.
4. Remove pull-type fuse holder.
5. Connect a dc voltmeter (at least ±1% accuracy) across 100-ohm, 25-watt resistor R2 (refer to logic page YA008).

DANGER
Resistor R2 may have reached a high temperature because of battery charger operation.

6. Insert fuse holder, and turn battery-pack toggle switches to ON.
7. Bring up unit power.
8. Adjust potentiometer on card PN 374863 (card socket B) for a reading of 16V on the voltmeter. This provides an average charging rate of 150 ma.
9. Turn off unit power.
10. Turn both battery-pack toggle switches to OFF.
11. Remove fuse holder.
12. Remove voltmeter leads.
13. Insert fuse holder.
14. Turn battery-pack toggle switches to ON.
15. Bring up unit power.

5.8 BATTERY CHARGE INDICATOR

Proper charger operation is indicated by the glow of the left electrode (as viewed through the Plexiglas* window) on the neon indicator located below the 50-amp fuse. Improper operation is indicated as follows:

1. If only the right electrode glows, current flow is in wrong direction. Check CR1 through CR4 of the charger.
2. If both electrodes glow, alternating current is indicated. Check CR1 through CR4.
3. If neither electrode glows, no charge is indicated. Change charger circuit card, check CR1 through CR4, and check for open SCR 2.
4. If indicator glows with extreme brightness, the charging rate is too high. SCR 2 is shorted.

Note: Nickel-cadmium cells lose some of their ability to deliver full load current on demand if they are not loaded periodically. To prevent this loss of load capability, the CE should be placed on battery within 30 days after the last battery load requirement.

*Trademark of Rohm and Haas Company

5.9 BATTERY PACK TEST SCHEDULE

1. Perform battery pack test at four-week intervals. See heading 5.10.
2. Perform individual tray test only when failure is observed. See heading 5.11.
3. Check appearance of terminals every three months. If deposits appear around terminals, it is permissible to vacuum these deposits, using a plastic or rubber brush attachment.

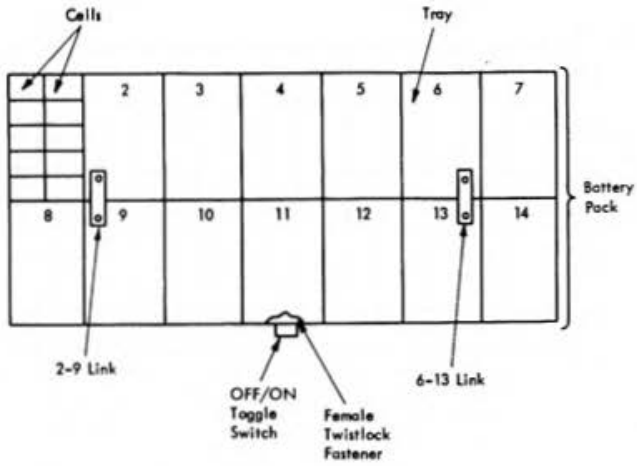
5.10 BATTERY PACK TEST

Figure 5-11 is provided for a component location reference.

1. Remove CE mainline power.
2. Remove cover from battery assembly to expose binding posts on metal power control box (inside battery cabinet).
3. Turn toggle switches on both battery packs to OFF.
4. Using a voltmeter capable of measuring 500V dc, connect positive lead to red terminal and negative lead to black terminal.
5. Turn toggle switches on ON.
6. The voltage indicated should be within the range of 289V to 350V dc.

Note: The 289V minimum assumes that the batteries have not been charged for any significant time. After batteries have been on charge at 150 ma for 24 hours, the minimum no-load voltage must be 320V dc. If the minimum voltage is below 320V, allow at least a 24-hour charge period and retest. Do not proceed until this requirement can be met. If, after a 24-hour charge period (see heading 5.8 for proper charge indication) the 320V dc minimum cannot be met, proceed to heading 5.11.

7. With meter remaining attached, turn on CE power.
8. Load and continuously execute any diagnostic routine.
9. Place TEST switch at normal position and, while executing routine, interrupt the 208V ac, 3-phase supply to the CE by flipping the main line CB off and leaving off.



Notes:
Numbers are for reference only.
Tray 11 contains no cells.

Figure 5-11. Battery Pack Component Locations

DANGER
Use extreme care when working in the area of the battery packs. Lethal voltages are present. Before performing any of the tests or procedures on this page, read DANGER notice at the start of this section.

10. Observe that power stays up for 6.5 ± 0.5 seconds, as shown by ON BAT indicator on power control panel.
11. Check that, after 6.5 ± 0.5 seconds power sequences down and ON BAT indicator turns off.

Note: To change the on-battery time, rotate knob on K23 (on-battery timer) clockwise to increase on-battery time. Refer to ALD YA004 for the location of K23.

12. Restore power to CE and wait for SEQ COMP indicator to light. Observe voltage levels stated in step 6.
13. Flip main line CB off and, quickly, on again.
14. Check that unit remains on-battery for the 6.5 ± 0.5-second timer duration, as indicated by ON BAT indicator. Then switch back to main line power.
15. Observe meter indication during the on-battery sequence. The output of the assembly must not fall to less than 250V dc before timeout ends. Allow on-battery sequence to proceed to full timeout. A lesser voltage is an indication of improper or insufficient charging or of weak battery cells. If the minimum load output voltage is less than 250V dc, allow sufficient charge time (see heading 5.6) and repeat this test. If, upon repeating the test, a voltage less than 250V dc is again observed, proceed to heading 5.12.
16. Turn off CE power and battery switches. Remove meter leads.
17. Turn on battery switches, and restore battery package cover.
18. Restore CE power.

5.11 BATTERY TRAY TEST

Note: This procedure should be performed only if a failure is observed in the procedure described under heading 5.10. Read DANGER notice at the start of this section before proceeding with test.

1. Turn off CE power.
2. Remove battery package cover.
3. Turn off battery pack switches, and remove the pull-type fuse holder.
4. Remove battery-pack ground strap.
5. Remove slide stop screw, if installed.
6. Pull out battery pack until slides lock.
7. Remove top cover from battery pack, using extreme caution to prevent shorting the battery terminals under the cover.

DANGER
Observe extreme caution. A live battery circuit voltage of about 160V dc exists beneath cover.

8. Place plastic safety covers on top of the battery pack so only one battery tray is exposed (see use of plastic covers under heading 5.12.1).
9. Remove the links connecting trays 2–9 and 6–13. This divides the pack so that the voltage between adjacent trays is 25V dc.
10. With a voltmeter, measure the tray potentials across the extreme terminals of each tray of 10 cells each. The potential should not be less than 11.5V dc. (The tray that is not connected in the one battery pack will not conform to this.) If the tray potential is sufficient, individual cell measurement in the tray is neither necessary nor desirable. If the tray potential is lower than 11.5V dc, either the bad tray or bad cell may be replaced as described under headings 5.13.3 and 5.12.4. Cell voltage should be at least 1.15V dc.

Note: To service the rear cells on a bottom pack, release the slide locks and slide the pack out an additional inch. Do not pull the assembly beyond the limitations of the slide.

11. Replace battery pack cover.
12. Unlock both slides, and return battery pack to operational position.
13. Install ground strap.
14. Install slide stop screw, if previously installed.
15. Plug in the pull-type fuse holder.
16. Turn on both battery switches.
17. Replace battery package cover.
18. Turn CE power on.

For cell removal procedure, see heading 5.12.4.

DANGER
Use extreme care when working in the area of the battery packs. Lethal voltages are present. Before performing any of the tests or procedures on this page, read DANGER notice at the start of this section.

5.12 MAJOR BATTERY PACK MAINTENANCE

DANGER
If the battery pack requires major maintenance, e.g., replacement of cells in several trays, the 13 trays of 10 cells each should be electrically disconnected from each other. This reduces the potential to 12.5V per tray; since there are no interconnections, this is the maximum voltage exposure. Follow the maintenance procedure described below when disconnecting any cell terminal.

5.12.1 Use of Special Tools

1. The insulated 5/16-inch nutdriver (PN 5447531) is for use on the cell terminals inside the battery packs. Care should be exercised to prevent bridging adjacent terminals with the exposed metal end.
2. The three plastic covers are used to cover all but one tray inside the battery pack. Each plastic cover is designed to cover a specific number of trays:

   The 8-1/16 x 14-inch cover (PN 5447517) covers six trays.
   The 5-25/64 x 14-inch cover (PN 5447519) covers four trays.
   The 5-25/64 x 14-inch "L" cover (PN 5447518) covers three trays.

   The following description refers to these covers by the number of trays covered.

   Note: The six-tray cover also has a slot which is used to remove links between trays 2 and 9 and between trays 6 and 13.

   a. Refer to Figure 5-11 for tray identification.
   b. The six-tray cover contains a notch in one edge to clear the twist-lock fastener. The three-tray cover contains two notches in one side and one notch in the opposite side to clear the twist-lock fastener.
   c. To gain access to trays 1, 2, 8, or 9, place the six-tray cover over trays 3, 4, 5, 10, 11, and 12 and the four-tray cover over trays 6, 7, 12, 13, and 14. The three-tray cover can be placed so that only one of the trays (1, 2, 8, or 9) is exposed.
   d. To gain access to trays 6, 7, 13, or 14, interchange the four-tray cover with the three-tray cover of step c.
   e. To gain access to trays 3, 4, 10, or 11, place the six-tray cover over trays 5, 6, 7, 12, 13, and 14 and the four-tray cover over trays 1, 2, 8, and 9. The three-tray cover can now be placed to expose only one tray (3, 4, 10, or 11).
   f. To gain access to trays 4, 5, 11, or 12, place the six-tray cover over trays 1, 2, 3, 8, 9, and 10 and the four-tray cover over trays 6, 7, 13, and 14. The three-tray cover can now be placed to expose only one tray (4, 5, 11, or 12).

5.12.2 Battery Pack Removal and Replacement

1. Remove two screws holding front cover, and remove front cover from battery package.
2. Turn toggle switches on both battery packs to OFF position.
3. Remove twist-lock fastener, and remove top cover from pack.
4. Disconnect ground straps.
5. Disconnect cable from toggle switch terminals, recording polarity for later reconnection.
6. Replace top cover.
7. Release both slide locks, and pull battery pack out until it is clear of slides.

DANGER
Battery pack weight exceeds 70 pounds. Normal safety practices must be adhered to.

8. Ensure that toggle switch is in OFF position in replacement pack.
9. Align slide assemblies and slide battery pack in until it locks.
10. Remove top cover.
11. Connect cable to toggle switch terminals. Observe polarity. Make sure toggle switches are in OFF position.
12. Replace top cover.
13. Replace pull-type fuse holder.
14. Turn both toggle switches to ON position.
15. Replace front cover by means of two screws.
16. Restore machine power.

DANGER
Use extreme care when working in the area of the battery packs. Lethal voltages are present. Before performing any of the tests or procedures on this page, read DANGER notice at the start of this section.

If any cells have been replaced, batteries should be charged for 24 hours before performing an on-battery test. Battery damage may result by going on-battery with cells that are not fully charged.

5.12.3 Tray Removal and Replacement

Note: An entire battery pack may be removed for tray or cell replacement.

1. Perform steps 1 through 4 under heading 5.12.2.
2. To remove a tray, position plastic covers so that connecting trays are exposed one at a time. Remove the links from connecting trays. Lift entire tray clear of battery pack. Observe polarity for replacement later.
3. Replace tray by sliding tray into position in battery pack. Observe polarity. Bolt connecting links to connecitng trays, using plastic covers to cover the other trays.

5.12.4 Cell Removal and Replacement

Note: If several trays in one battery pack are found to be bad (see heading 5.11), it may be more desirable to replace the entire pack (see heading 5.12.2). If site limitations require that the pack be serviced, follow the procedure for individual cell removal and replacement.

1. Upon isolating a battery failure to a pack, place six-tray cover over trays 1, 2, 3, 8, 9, and 10 so that the slot is over the 2-9 link (Figure 5-12). Place other covers to cover all other trays. Remove 2–9 link.
2. Reposition covers so that six-tray cover is over trays 5, 6, 7, 12, and 14 and the slot is over 6–13 link. Place other covers to cover all other trays. Remove 6–13 link.
3. There is now no potential higher than 25V between any two adjacent trays.
4. Place plastic covers so that only the defective tray is exposed. There is now only 12.5V exposed.
5. Measure individual cells of tray. They should not measure less than 1.15V dc with no load.
6. Remove any defective cell found from the previous test by unbolting connecting links from defective cell and sliding cell out of tray. Observe polarity.
7. Replace removed cell by sliding in a new cell from the spare tray or from a tray in stock and bolting the links back in place. Observe polarity.

Note: In the case of a rear cell on the bottom tray, it may be necessary to release the slide locks and slide the battery pack out an additional inch. Care should be exercised to prevent pulling the tray beyond the limitations of the slide assembly.

5.13 BATTERY BACKUP CUT-IN

DANGER
The secondary winding (end-to-end) of the charger transformer contains the highest voltage in the assembly. Unloaded, this can be as high as 897V ac rms. Other points in the circuitry are electrically "hot" with respect to chassis ground. Removal of both J2 and prime power ensures that the package is free from voltage.

Battery "cut-in" is brought about by a prime power failure. Confirmation of battery cut-in is obtained by measuring continuity across TB-5, connections 9 and 10. (Reed relay contacts close.)

Note: The sensing circuitry blocks battery backup cut-in during the following:

1. Power-on sequence.
2. CE in state 0 and TEST switch set to TEST position.
3. Power-off sequence caused by a thermal, an OV/OC, or a regulator undervoltage condition.
4. EPO/MPO power-off sequence.

5.14 LINE SENSE AND SWITCHING CIRCUIT

Refer to Figure 5-13 for a description of the line sense and switching circuit. This circuit is adjusted as follows:

1. Turn off unit power.
2. Turn both battery-pack toggle switches to OFF.
3. Remove pull-type fuse holder.
4. Remove sense card (PN 374862) from card socket A of battery charger box. Insert card extender in socket, and install card in extender.

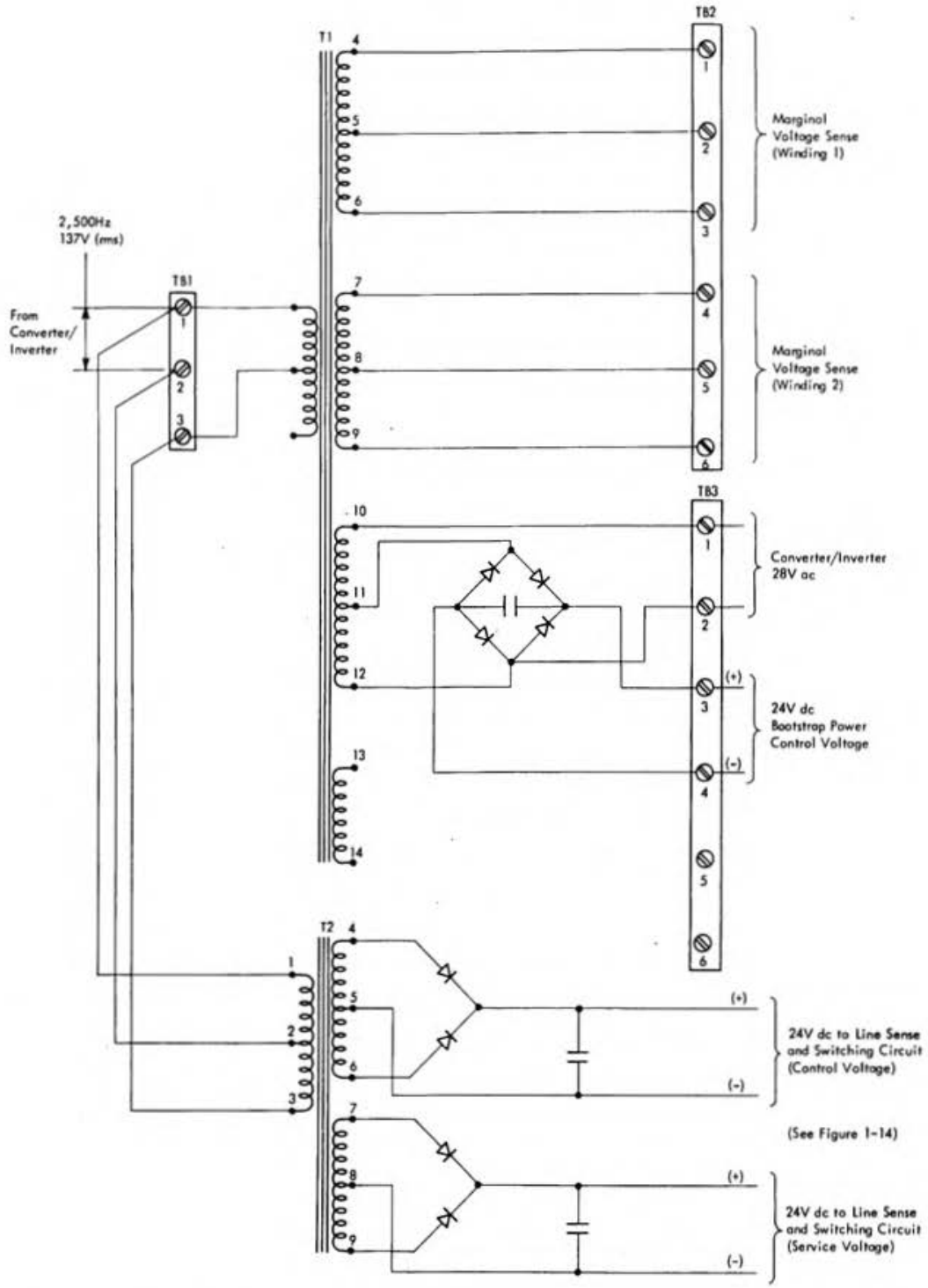


Figure 5-12. Bootstrap Power Supply

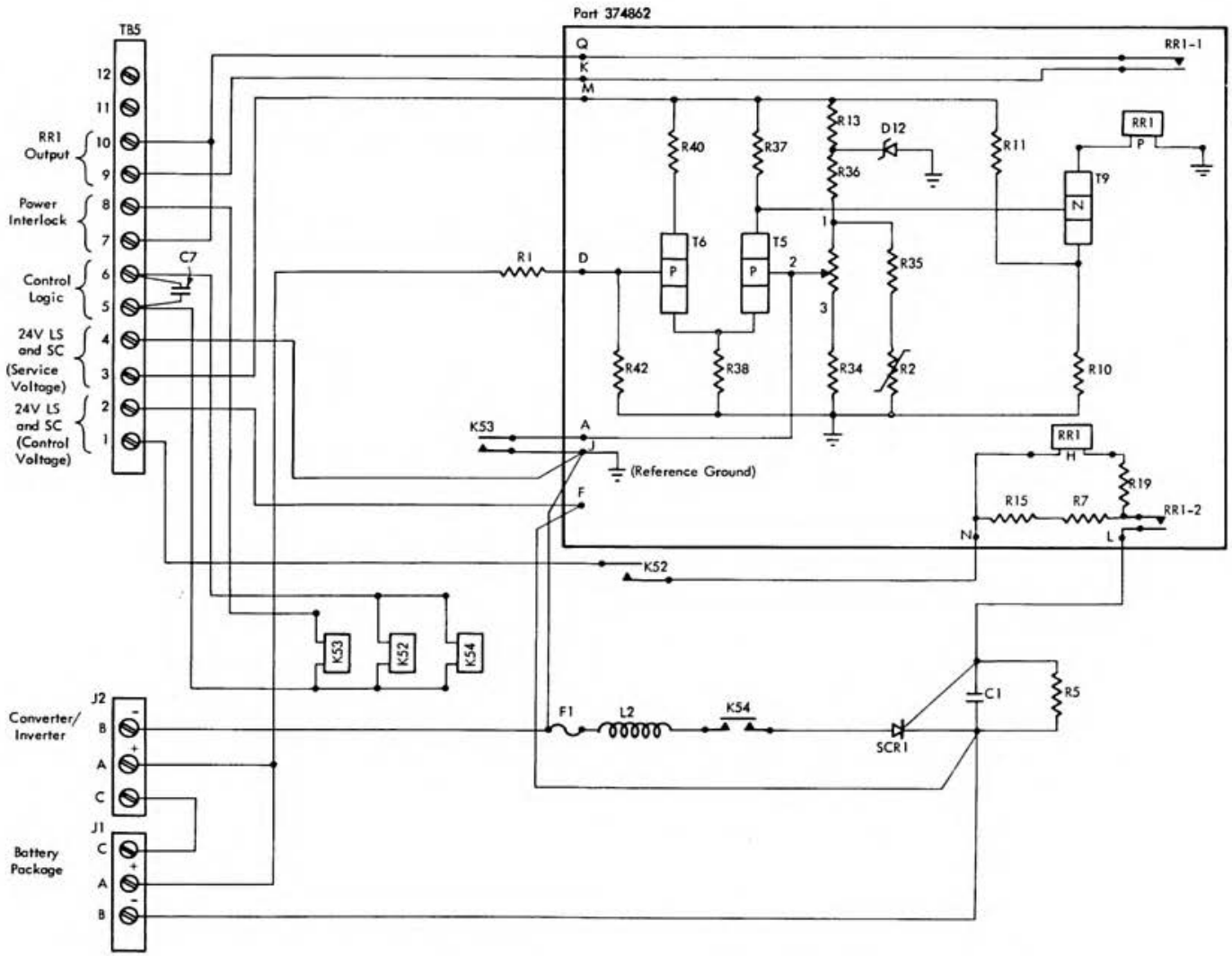


Figure 5-13. Line Sense and Switching Circuit

DANGER
Use extreme care when working in the area of the battery packs. Lethal voltages are present. Before performing any of the tests or procedures on this page, read DANGER notice at the start of this section.

DANGER
High voltage is present on the cards in the battery charger and sense circuit. Sense circuits are not referenced to machine dc or frame ground.

5. Connect a dc voltmeter (at least ±1% accuracy) across pins A and J of sense card (pin A to + terminal).
6. Insert pull-type fuse holder.
7. Turn battery-pack toggle switches to ON.
8. Bring up unit power.
9. Adjust potentiometer on sense card for a meter reading of 4.6V. This causes the sense circuit to switch in the battery package when prime power input drops to approximately 186V ac.
10. Turn off unit power.
11. Turn both battery-pack toggle switches to OFF.
12. Remove pull-type fuse holder.
13. Remove card extender, and replace sense card in socket.
14. Insert fuse holder.
15. Turn both toggle switches to ON.
16. Bring up unit power.

5.15 BOOTSTRAP POWER SUPPLY

The bootstrap power supply (Figure 5-12) receives its input as 2500 Hz, 137V rms power from the converter/inverter. This supply includes transformers and rectifying circuits which provide the necessary sense and control voltages needed for:

1. Voltage sensing circuitry.
2. 24V dc for prime/battery power sequencing and control.
3. 28V ac for converter/inverter bias.
4. On-battery sense and switching circuit and service voltages.

There is no adjustment to the bootstrap power supply.

DANGER
Most of the windings of the bootstrap power supply are at hazardous voltages with respect to chassis ground. The bootstrap supply is safe only when J1, J2, and prime power are removed.

5.15.1 DC Voltages

Table 5-2 lists dc voltage values of the bootstrap power supply. Refer to Figure 5-12 and ALD page YA008 for voltage-measurement terminals. Table 5-3 lists ac voltages of the bootstrap power supply.

Table 5-2. Bootstrap DC Voltage Measurements

Meter Across	Voltage Reading*	% Tolerance
TB-3 and TB-4	24V	+10, -5
E4-1 and E4-6 (ALD page A008) or TB5-1 and TB5-2 on assembly 5713610	24V	±10
E3-6 and E3-1 (ALD page A008) or TB5-3 and TB5-4	24V	±10

*Prime power input voltage to converter is 208V.

Table 5-3. Bootstrap AC Voltage Measurements

Terminals*	Voltage**
TB1-1	95
TB1-2	95
TB1-3	100
TB2-1	32
TB2-2	0
TB2-3	32
TB2-4	32
TB2-5	0
TB2-6	32
TB3-1	57
TB3-2	25

*Measure with oscilloscope referenced to machine (frame) ground.
**Voltages are peak to peak, ±10%.

This chapter contains figures and references to aid maintenance personnel in locating components within the CE.

Figure 6-1 identifies the frames and gates in the CE.

Figure 6-2 shows the board locations within gates A, B, C, E, K, and L and gives the locations of the functional elements within each gate.

Figure 6-3 shows the overall physical layout of the ROS unit, including parts of gate C and all of gate D.

Figure 6-4 shows the location and numbering of the laminar bus terminal boards.

Figure 6-5 shows battery charger terminal board locations and connector plug locations.

Figure 6-6 shows the battery package with the front cover removed.

Figure 6-7 shows the location of battery-pack components as viewed with pack extended and top cover removed.

Figure 6-8 shows the pin designations on a large board.

Figure 6-9 shows the card contact, board-pin relationship, and voltage pins for the cards.

Figure 6-10 shows the switch contact terminal locations for switches of the CE.

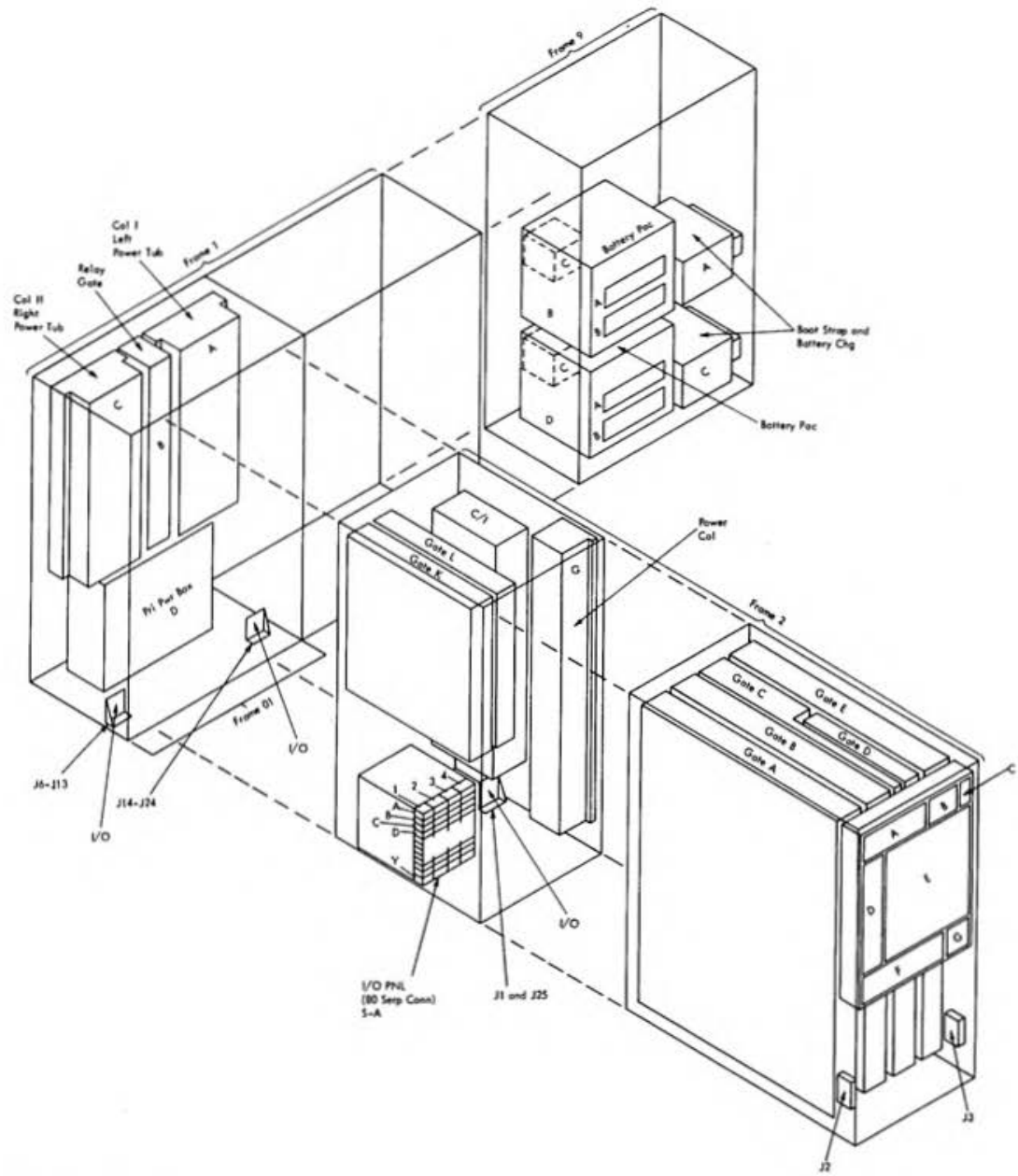


Figure 6-1. CE Layout

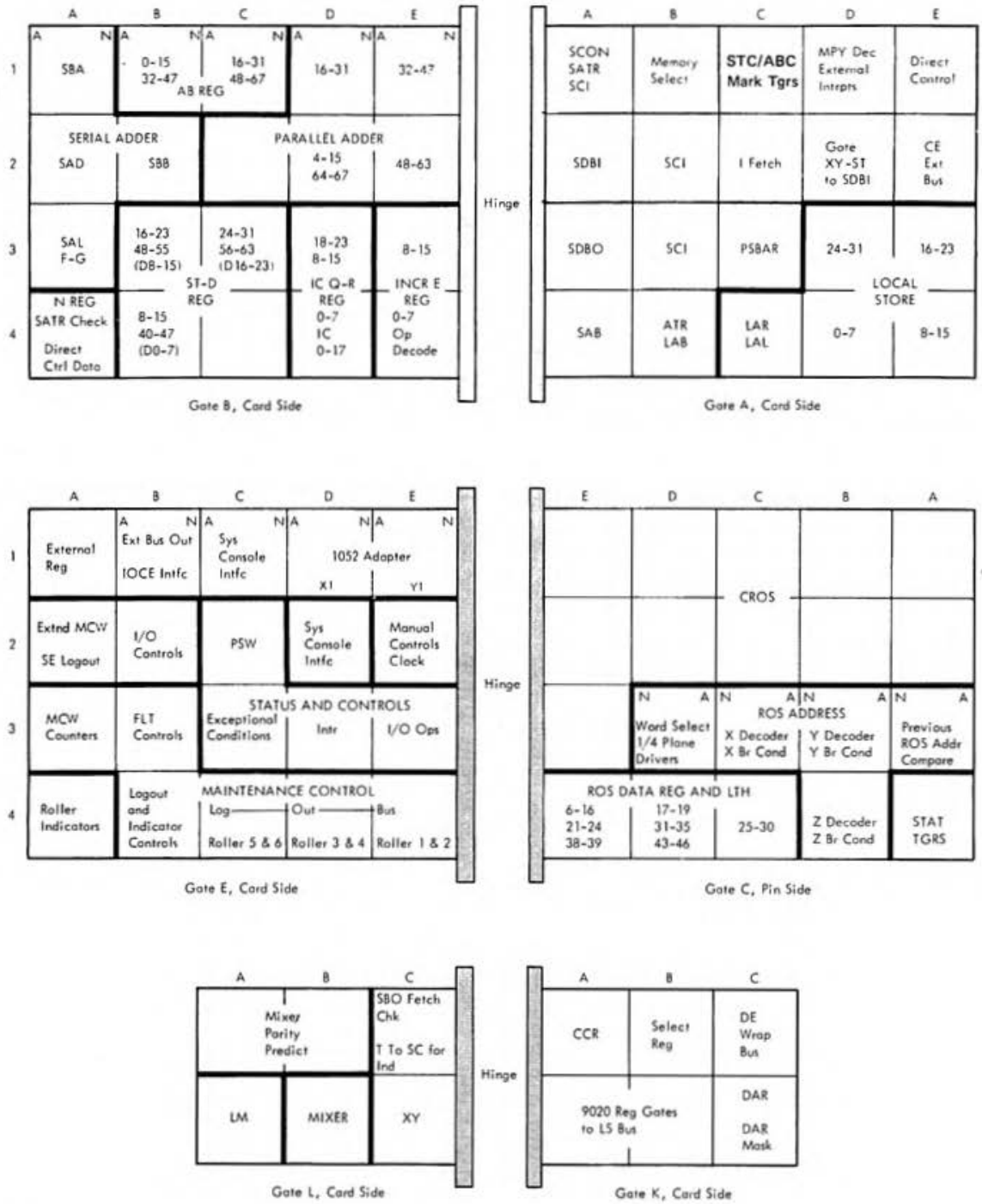
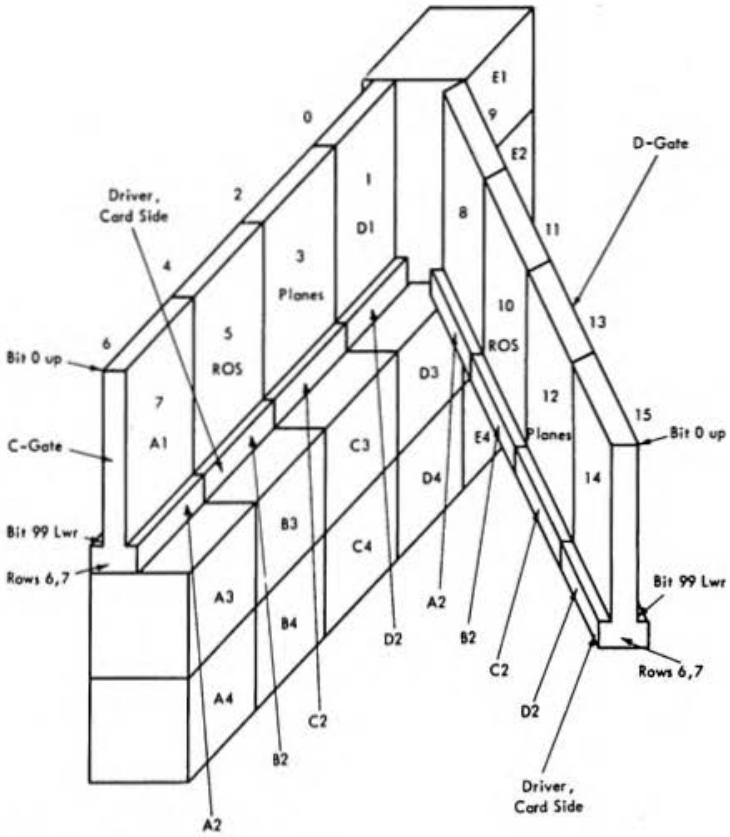


Figure 6-2. Large Board Assignments (Functional)



See ALD ED000-ED020 for detail of ROS layout.

Figure 6-3. ROS Physical Layout

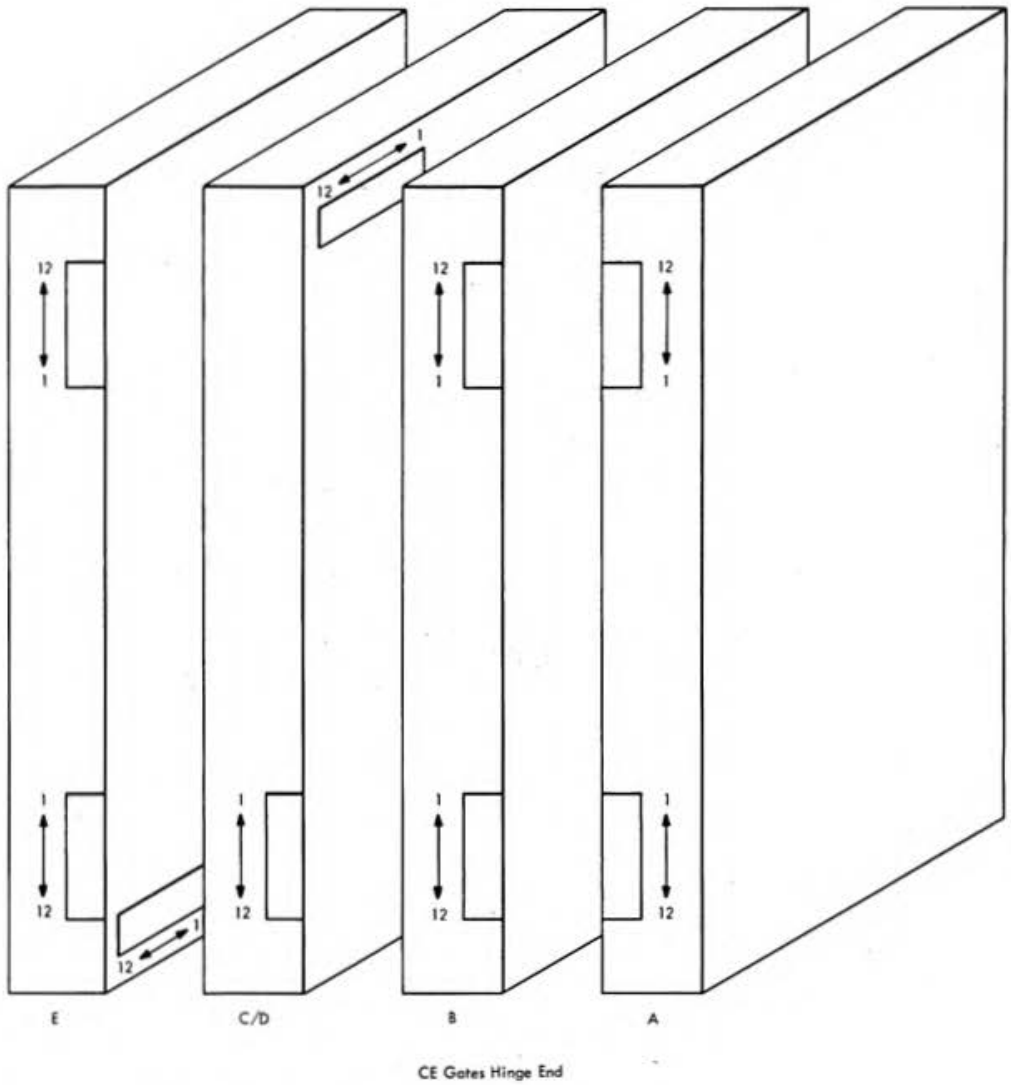


Figure 6-4. Laminar Bus Terminal Board Location

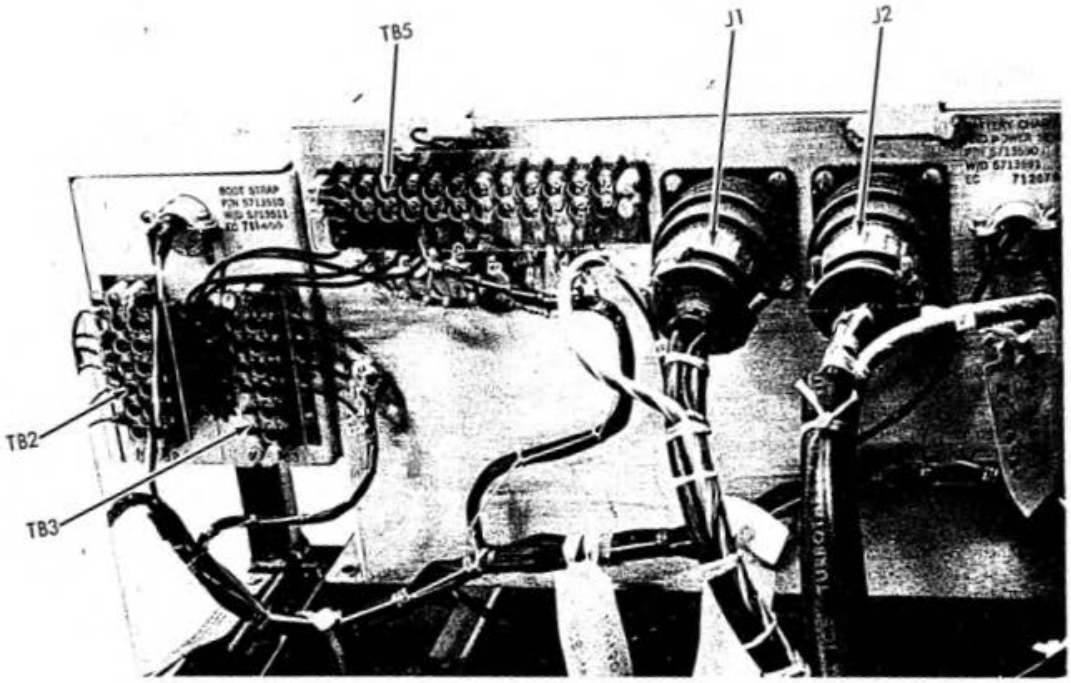


Figure 6-5. Battery Charger with Bootstrap

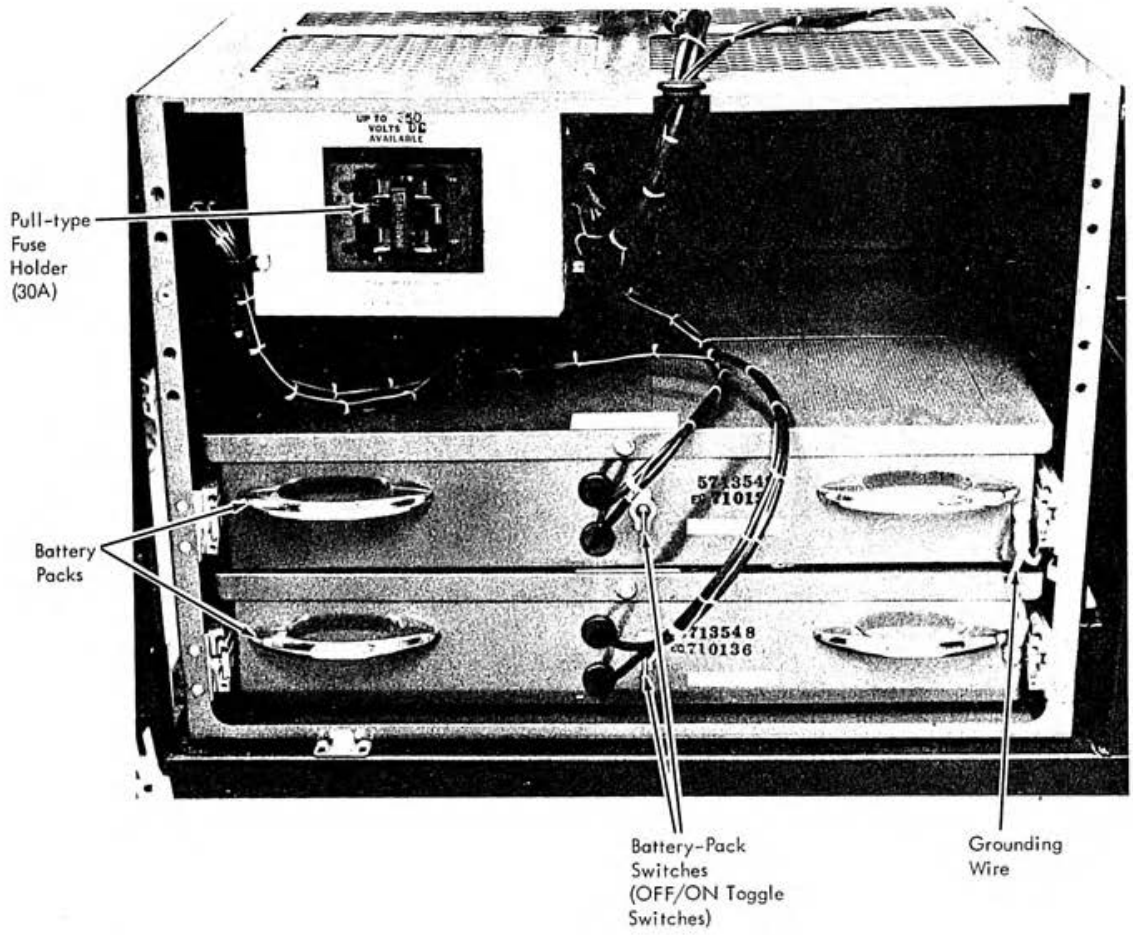


Figure 6-6. Battery Package with Cover Removed

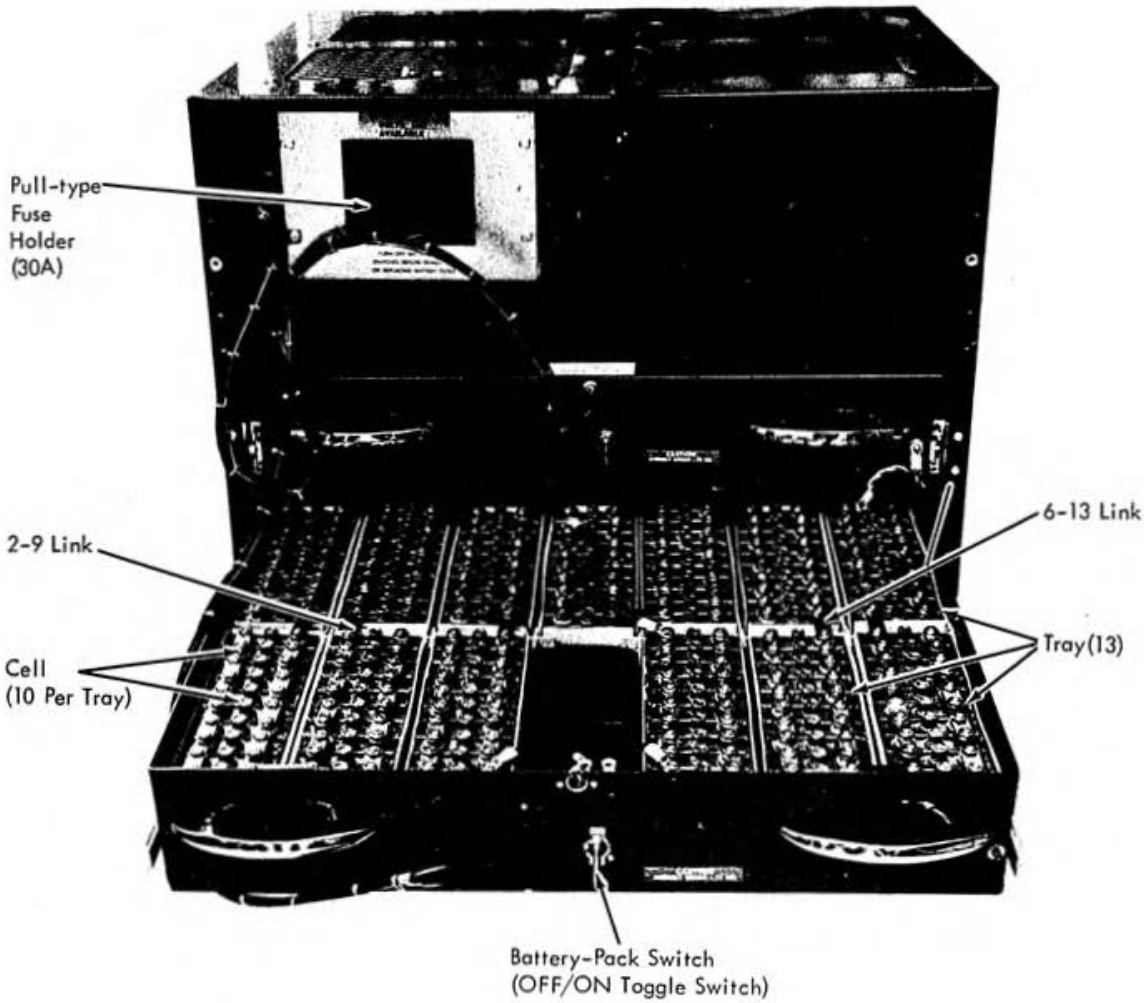


Figure 6-7. Battery Pack Components

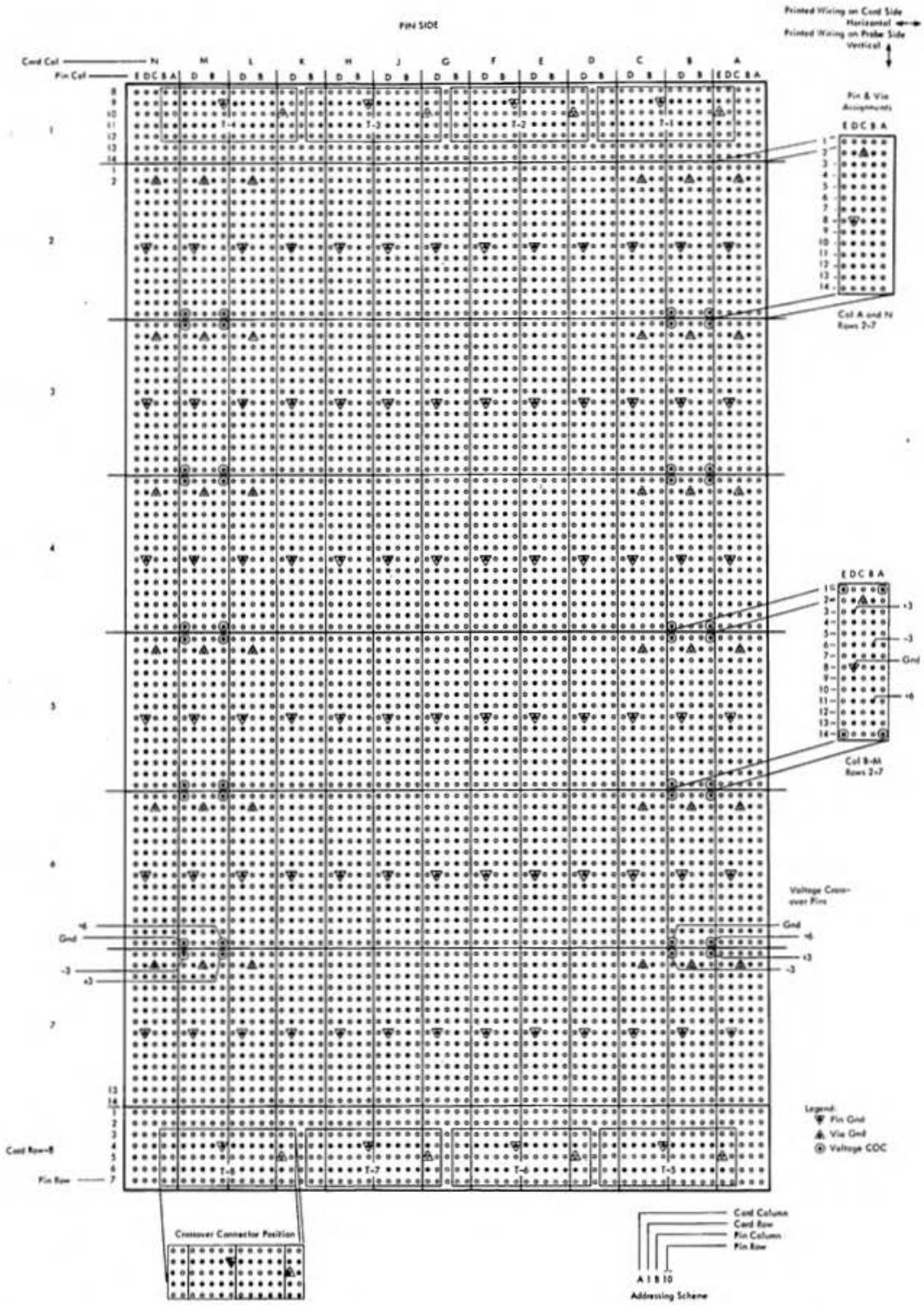


Figure 6-8. Large Board Pin Addresses

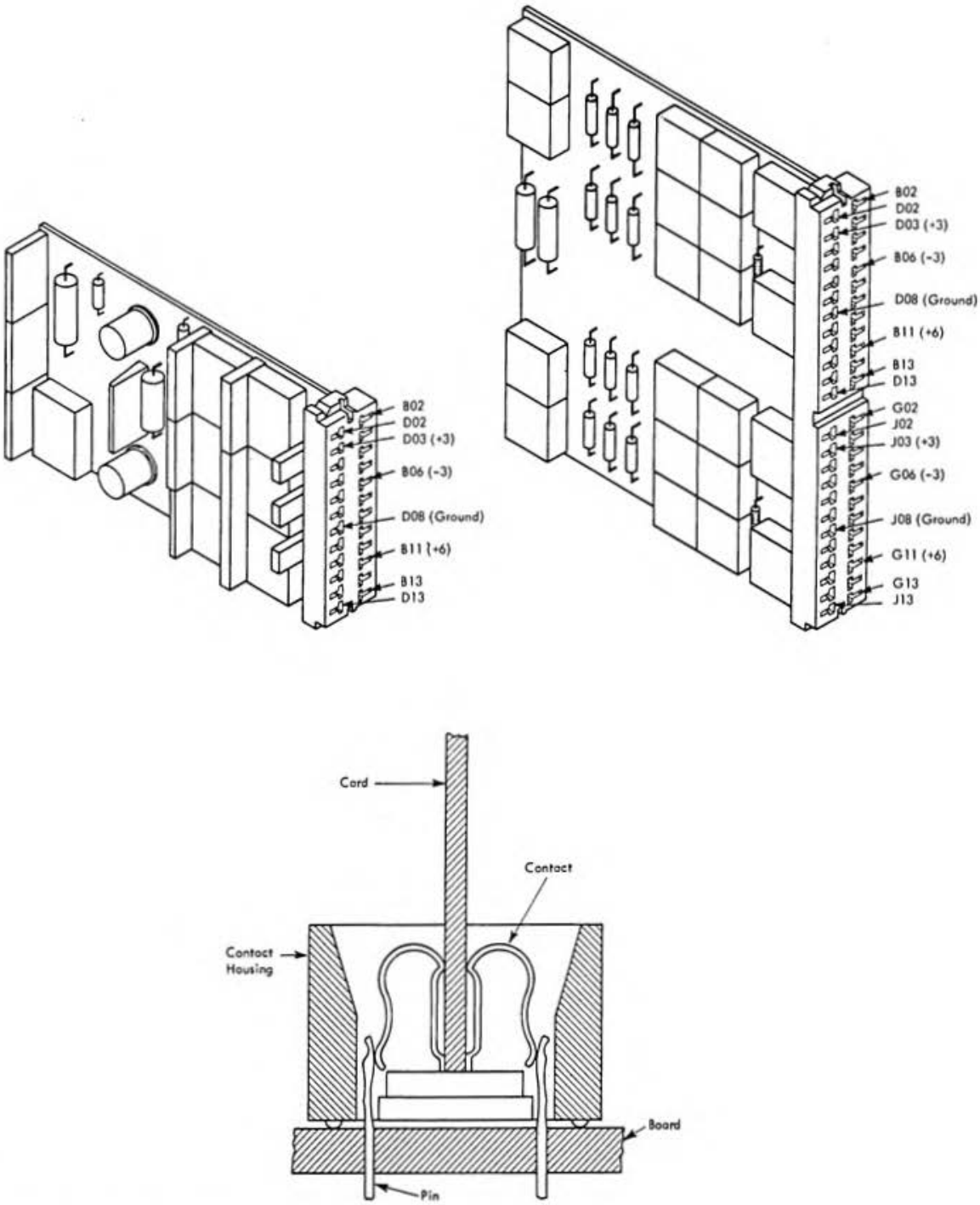
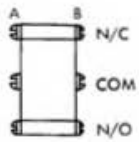
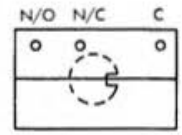


Figure 6-9. Card Contact, Board-Pin Relationship

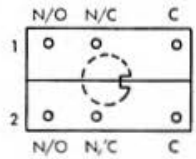
Pushbutton Switches
Power On/Off



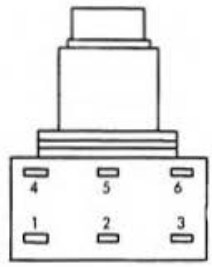
All Others



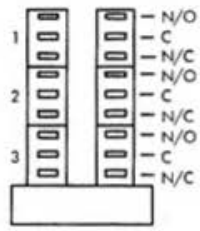
360 Mode



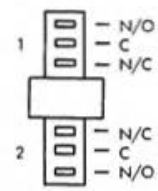
System Interlock Key



Toggle Switches
Data Switches
Address Switches



All Others



Scan Mode-Repeat
Inhibit CE Hardstop
Disable Interval Timer
Repeat ROS Address
Ind Roller 1 Pos 6
Test

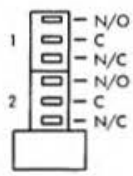
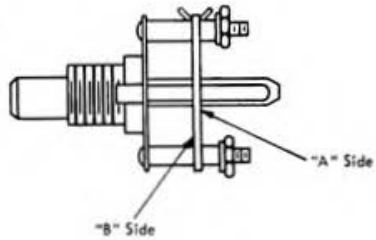
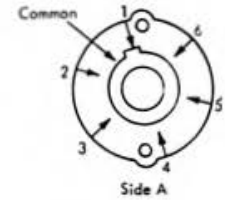


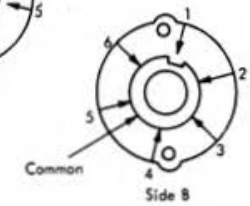
Figure 6-10. Switch Contacts (Sheet 1 of 2)

Rotary Switches

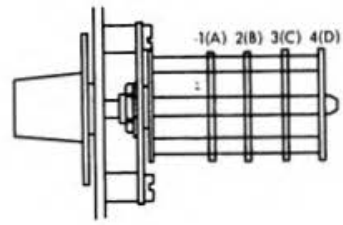
Indicator Roller Switches



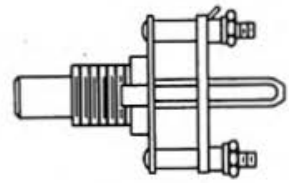


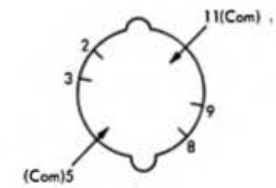


Main Storage Select and Load Unit Switches

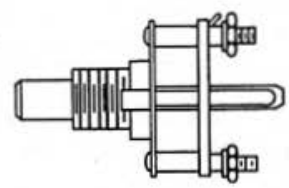


Register Select and Rate Switches





Frequency Alteration Switch



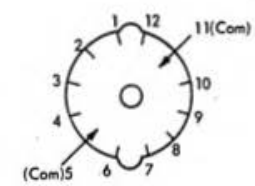


Figure 6-10. Switch Contacts (Sheet 2 of 2)

The only special circuits in the CE are in ROS for the differential (sense) amplifiers, sense latches, and array driver circuits. Because these circuits are internal to the SLT pluggable cards, circuit schematics are not required for maintenance. The ROS hardware repair is effected at the card level as described in heading 4.3.6 of this manual.

Tables B-1 through B-7 and Figures B-1 through B-3 are provided to aid in diagnosing and repairing the CE.

Table B-1. Conditions at End of I-Fetch

RR FORMAT

Instruction in E Reg (all instruction bits).
R1 Operand in A, B, and D Reg.
R2 Operand in S, T.

For Branch Instr. } STC = 4

R1 Operand in S, T Reg.
R2 Operand in A, B and D Reg.

RX FORMAT

Instruction in E Reg (first 16 bits of instruction).
R1 Operand in S, T.
Operand Address in D (C(B2) + C(X2) + D2).
Storage Req for Operand given on last I-Fetch Cycle.

RS, SI FORMAT

Instruction in E Reg (first 16 bits of instruction).
R1 Operand (if applicable) in S, T.
Operand Address in D(C(B) + D).
Storage Req for Operand given on last I-Fetch Cycle.

SS FORMAT

Instruction in E Reg.
Destination Operand in S, T.
Destination Address in D Reg.

Logical Operand Address	=	C(B1) + D1
Divide Operand Address	=	C(B1) + D1
Dec. & Not Div. Operand Address	=	C(B1) + D1 + L1

Storage Req for Source Operand given on last I-Fetch Cycle.
Source Address in IC = (IC in local store working reg)
Logical + Mult + Div Address = C(B2) + D2
Dec. $\overline{(\text{Mult} + \text{Div})}$ Address = C(B2) + D2 + L2
Program Store Compare (ASC) has been made.

Table B-2. Forced ROS Addresses

Function	Forced Address	CLD Page	Block
All Zeros Test	F02, F03	QY061	Q6, Q7
All Ones Test	F00, F01	QY061	Q8, Q9
External Interrupt	006	QU001	E1
Force Padder Full Sum (Scan)	6B7	QJ031	N2
Invalid Ins'n Address	002	QT041	J1
Paging Spec	007	QU001	A3
I/O Interrupt	00E	QU001	Q1
Machine Check Interrupt	00C	QU001	A1
Manual Control Stop	026	QY041	N2
Power On Reset	00B	QY041	A1
Program Interrupt	00A	QU001	L1
Program Store Compare	004	QY041	N3
Pulse Mode Reset	005	QY051	E1
Q Refill RX Format	030	QY041	N8
Q Refill RX Format	032	QT041	J6
Q Refill RX Format	022	QT041	L5
Q Refill RX Format	03A	QT041	J7
Q Refill RS-SI Format	034	QT041	N6
Q Refill RS-SI Format	024	QT041	Q7
Refill Shift Instruction	020	QJ001	C1
Repeat Instruction	028	QY051	G
ROSAR Test	9BB	QY021	G7
SAP Interrupt Delay	02E	QU001	A9
SCAN - Logout	019	QY001	C1
SCAN - PTSC (360)	6B0	QY011	N2
SCAN - MCW4	009	QY031	A1
SCAN - MASK	011	QY031	E1
End Op	010	QY041	G5
Storage Ripple	800	QY051	L1
SVC Interrupt	008	QU001	G1
System Reset	003	QY041	C3
Time Clock Step, Ext Start, Receive ATR, Ext Stop	014	QT041	A1
Wait Exception	02A	QY051	Q7
Wait	784	QY051	Q8
IPL-Wait For Release	BAO	QY061	J7
Diagnose - Keys to MCW Address +8	5B0	QY001	Q4
Ripples IC and PADDL	5C7	QY051	A9
Ripples IC and PADDL 40–63	500	QS101	A8
Ripples Serial Adder and F Reg	83A	QY041	Q3
Ripples D Reg	4C4	QY051	Q2
Ripples E Reg 8–15	839	QY041	A2
Ones to PADDL 32–63	7B2	QY461	N4
Ones to PADDL, D Reg	891	QY041	J9
Ones to D and T Regs	88F	QY041	A5
Ones to E Reg 8–15	00B	QY041	A1
Zeros to A, B, Regs and AB CTR	545	QS001	E4
Set CPU Marks	9BF	QY051	J5
Logout (All Indicators Should Light)	A15	QY001	N2
Read LS per E 12–15	200	QT001	C3
Read LS per E 11–15	7CE	QY051	N6
Write LS per E 11–15	7CF	QY051	L6
Blank Cycle, No gates should be up and all errors on roller 2 position 2 should be able to be reset by the CHK RESET pushbutton.	5B2	QY061	N3
Scan - SCNT (FAA)	AD2	QY011	Q2
No SATR RESPONSE (IPL)	B9A	QY001	G2
Micro Diagnostic	FAA	AA001	E2

Table B-3. ROS Sense Amp Outputs

The output of the ROS is read by the sense amplifiers located in boards E1 and E2. Each bit of the 200-bit word is located as shown below:										
Bit	0	10	20	30	40	50	60	70	80	90
0u	E1B2G10	E1G2G10	E1B4G10	E1G4G10	E1B6G10	E1G6G10	E2B2G10	E2G2G10	E2B4G10	E2G4G10
01	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
1u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
11	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12
2u	E1C2G10	E1H2G10	E1C4G10	E1H4G10	E1C6G10	E1H6G10	E2C2G10	E2H2G10	E2C4G10	E2H4G10
21	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
3u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
31	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12
4u	E1D2G10	E1J2G10	E1D4G10	E1J4G10	E1D6G10	E1J6G10	E2D2G10	E2J2G10	E2D4G10	E2J4G10
41	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
5u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
51	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12
6u	E1E2G10	E1K2G10	E1E4G10	E1K4G10	E1E6G10	E1K6G10	E2E2G10	E2K2G10	E2E4G10	E2K4G10
61	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
7u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
71	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12
8u	E1F2G10	E1L2G10	E1F4G10	E1L4G10	E1F6G10	E1L6G10	E2F2G10	E2L2G10	E2F4G10	E2L4G10
81	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
9u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
91	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12

Table B-4. ROS Sense Latch Outputs

The 100-bit ROS control word is contained in the Sense latches located in boards E2 and E3. Each bit is located as shown below:										
Bit	0	10	20	30	40	50	60	70	80	90
0	E3E2J13	E3H2J13	E3D4J13	E3H4J13	E3E6J13	E3J6J13	E2B6J10	E3H6J11	E2C6J12	E2H6J09
1	J10	J12	J10	J12	J10	J12	J12	J09	J09	J10
2	J11	J10	J11	J10	J11	J10	J09	J12	J10	J12
3	J12	J11	J12	J11	J12	J11	J11	J10	J11	J13
4	J09	J09	J09	J09	J09	J09	J13	J13	J13	J11
5	E3F2J10	E3J2J10	E3E4J10	E3J4J10	E3F6J10	E3K6J10	E3F4J12	E2L6J13	E2E6J13	E2K6J11
6	J09	J09	J09	J09	J09	J09	J09	J11	J10	J12
7	J13	J12	J13	J12	J13	J12	J13	J12	J09	J13
8	J12	J13	J12	J13	J12	J13	J11	J10	J12	J09
9	J11	J11	J11	J11	J11	J11	J10	J09	J13	J10

Table B-5. Diagnose Kernels

These Diagnose Kernels may be used in states 3, 2, 1, or 0:

Address	Function	CAS Page
FD0	Logout Storage	QQ171
FD1	Reset Checks	QQ171
FD2	Logout Local Storage	QQ181
FD3	Set DAR Mask	QQ181
FD4	Store DAR	QQ181
FD5	Define Storage	QQ181
FD6	Store PIR	QQ181
FD7	Logout Registers	QQ181

These Diagnose Kernels may be used in state 0 only:

Address	Function	CAS Page
5B0	Store Data Keys	QY001
6B0	Partial Scan-IN	QY011
AD1	Logout FAA	QQ041
AD2	Scan-In	QY011
AD3	Wrap DE	QQ171
010	NEOP Block Used when setting MCW on I_2 Field Bit	QT041
XXX	Branch to any ROS address	

Table B-6 (a). Diagnose Instruction I_2 Field Bit Description

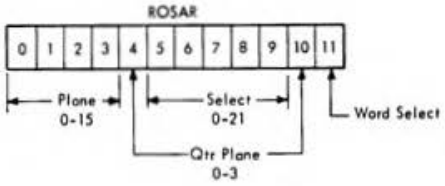
Bit	Use
8	Defeat interleaving.
9	Defeat interleaving and reverse.
10	Diagnose FLT.

Table B-6 (b). Diagnose Instruction MCW Bit Description

Bit	Use
0	Reverse SAB tag parity.
1	Start count on address compare.
2	Reverse serial adder full-sum parity.
3	Reverse mark parity.
4	Reverse SAB P_A.
5	Reverse SAB P_B.
6	Log on count (conditional terminate for FLT).
7	Expected response for FLT.
8–19	ROS address.
20	Disable interval timer.
21–31	Count (for DE wrap quadword count, bits 29–31 must be 0).
32–35	Select SE for logout or DE for DE wrap and DE force request.
36–39	Select DG for DE wrap or DE force request (if this field is all zero, all eight DGs will be selected).
40–45	Select CVG for DE wrap or DE force request.
46	Reverse 'Normal op'.
47	Force DG request.
48	Prevent SAB bit 8 from setting invalid address.
49	Reverse external register P 0–7.
50	Reset check register bits.

Table B-7. 1052 Latches/Triggers

Name	FETOM Figures FEMDM Diagrams	ALD
Address In	6–29, 6–32	PG 101
Attention Status	6–33	PG 131
Binary Trigger	Figure C-14	PG 701
Bus Out Check	6–33	PG 021
Busy Condition	6–30, 6–31	PG 121
Cam Control	Figure C-5	PG 641
Cancel		PG 421
Carrier Return	6–31	PG 631
Carrier In Motion		PG 641
CE Mode		PG 701
Channel End	6–31	PG 131
Command Chaining		PG 121
Command Reject	6–33	PG 141
Device End	6–31	PG 131
End of Line	6–31	PG 641
Enter		PG 421
Equipment Check	6–33	PG 021
Inhibit Carrier Return	6–31	PG 151
Initial Select	6–29	PG 101
Upper/Lower Case	6–31	PG 611
Operational In	6–29, 6–32	PG 101
Operational In Interlock	6–29	PG 101
Printer Busy	6–31	PG 641
Printer Cycle		PG 641
Read Command	6–29	PG 151
Ready	6–31, 6–33	PG 621
Request PB Interlock	6–33	PG 621
Sense Command	6–29	PG 151
Service In	6–30, 6–32	PG 111
Service Request	6–29, 6–32	PG 111
Shift Change	Figure C-8	PG 611
Status In	6–29	PG 111
Status Stacked	6–31	PG 121
Stop	6–31	PG 121
Store Device In	6–31	PG 621
Store Request	6–33	PG 621
Test I/O	6–29	PG 141
Unit Check	6–33	PG 131
Unit Exception	6–33	PG 131
Write Command	6–29	PG 151



Drive Location Chart

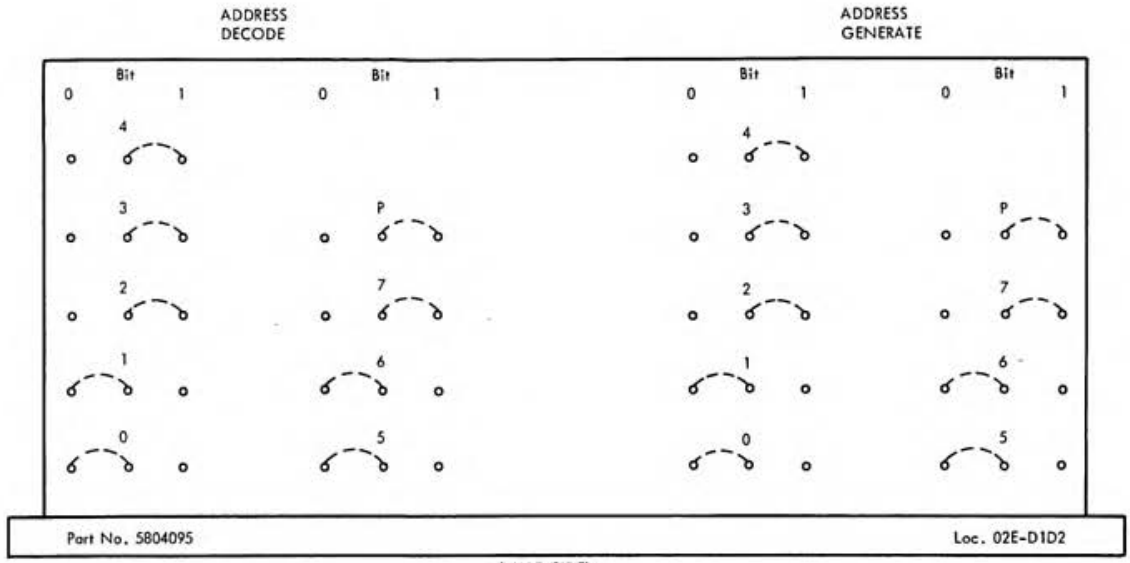
Qtr Plane	Select	Card Col	Qtr Plane	Select	Card Col
0	0-10	M6	2	0-10	F6
0	11-21	L6	2	11-21	E6
1	0-10	J6	3	0-10	C6
1	11-21	H6	3	11-21	B6

Select	Card Col	Pin Col	Pin
0, 11	D	J	4
1, 12	D	J	2
2, 13	D	J	5
3, 14	D	J	6
4, 15	D	J	7
5, 16	B	G	8
6, 17	B	G	7
7, 18	B	G	5
8, 19	B	G	2
9, 20	B	G	3
10, 21	B	G	4

If selected plane is on card side

If selected plane is on pin side

Figure B-1. ROSAR and ROS Driver Location Chart



Plug decode and generate sections for the same address.

ALD: PG 031
ZP 070-090

Jumper every bit for either 0 or 1.

Plug for odd parity.

Example: For address

	3			9				
	0	0	1	1	1	0	0	1	1	(hex)
	0	1	2	3	4	5	6	7	P	(bit number)

Jumper center to 1 (right) for bits 2, 3, 4, 7, and P.

Jumper center to 0 (left) for bits 0, 1, 5, and 6.

Figure B-2. Address Card Layout for 1052 Adapter

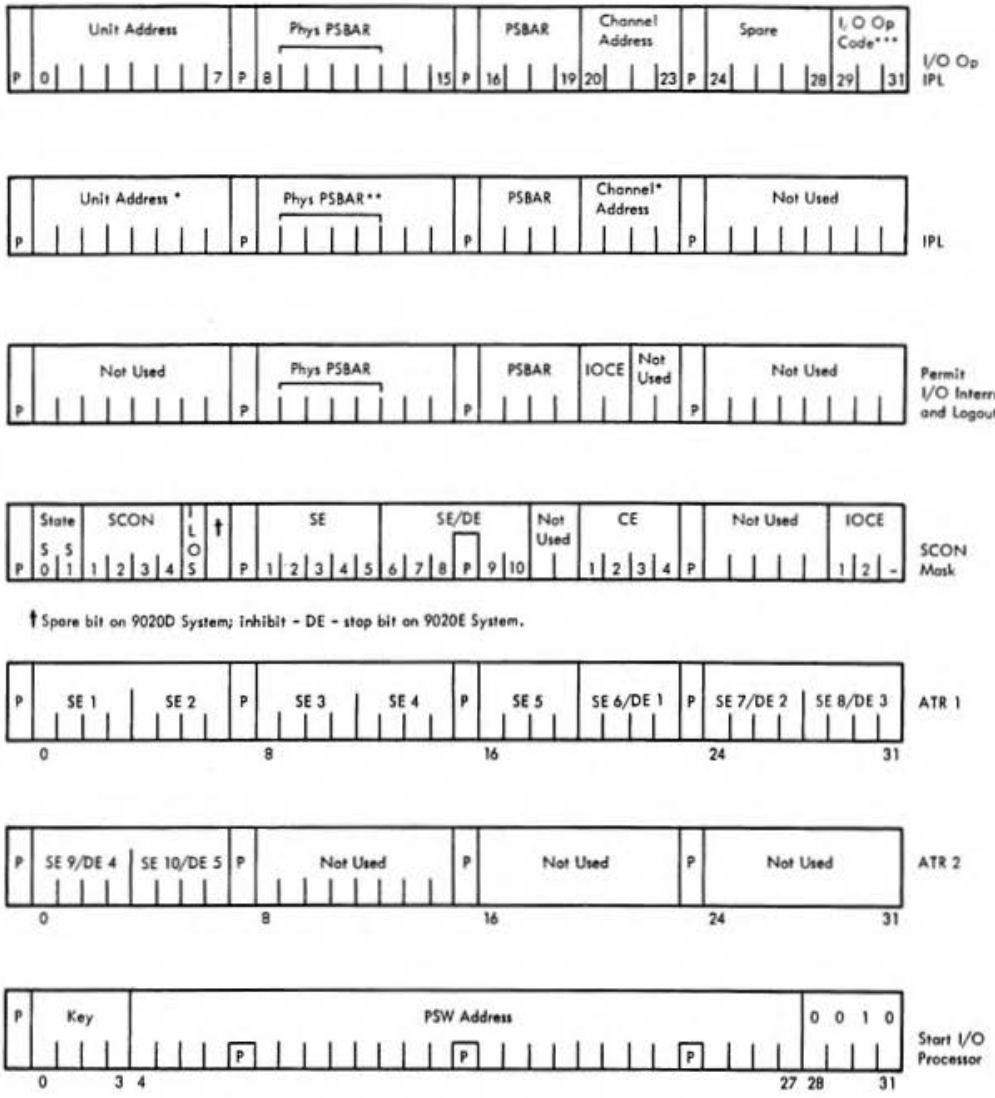


Figure B-3. External Register Formats

Figure C-1, below, is a removable chart that may be completed with applicable information and kept with the CE for future reference.

Marg/Meter Sel Switch Position	Margin Status	Actual + Voltage	Measurement Location	Indicated Voltage			
ROS LOCATE [PS11]	Nominal High Low	++ 20V 7V	Gate C/D Upper 6				
GATE A [PS16]	Nominal High Low	 6.5V 5.5V	02A C1G2 B11				
GATE B [PS15]	Nominal High Low	 6.5V 5.5V	02B B4G6 B11				
GATE C [PS8]	Nominal High Low	 6.5V 5.5V	02C D3G2 B11				
GATE E [PS7]	Nominal High Low	 6.5V 5.5V	02E B4G6 B11				
GATE K and L [PS5]	Nominal High Low	 6.5V 5.5V	02K C2G2 B11				
Date of calibration Calibrated by							

+Measure according to test procedure, heading 5.3.
++Set by optimization procedure, heading 4.9.

CE Serial Number _____

Figure C-1. System Control Panel Voltmeter Calibration Chart