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IBM Maintenance Information

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Volumes R01 through R06 accompany each Control Module and support all 3350s attached.

3350 Disk Storage

3350	BA0000 Seq. 1 of 2	2358629 Part No.	441300 31 Mar 76				

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PREFACE

MAINTENANCE INFORMATION MANUAL ORDERING PROCEDURE (IBM Internal)

Individual pages of the 3350 Maintenance Information Manual can be ordered from the San Jose plant by using the Wiring Diagram/Logic Page Request (Order No. 120-1679). In the columns headed "Logic Page" enter the page identifier information: sequence number, sheet number, part number, and EC number. Groups of pages can be ordered by including a description (section, volume, etc.) and the machine serial number.

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3350

BA0000 Seq. 2 of 2	2358629 Part No.

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SAFETY

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects.
3. After victim is breathing by himself or when help is available:
   a. Loosen clothing.
   b. Place victim on his side.
   c. Keep victim warm.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on back; lift neck and tilt head way back. (Quickly remove any noticeable food or objects from mouth.)

2. Pinch nose closed; make airtight seal around victim's mouth with your mouth; and forcefully breathe into victim until chest rises (expands).

3. Continue breathing for the victim 12 times per minute WITHOUT STOPPING.
4. If chest does not rise (expand), roll victim onto side and pound firmly between shoulder blades to remove blocking material. Also, try lifting jaw higher with your fingers. Resume rescue breathing.

OLT CONTENTS

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For additional information on OLTS and a bibliography, see the *System/370 Diagnostic Reference Summary* (Order No. SY25-0512) and the *OLT Users Guide* (Order No. D99-3350).

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RUNNING REFRESHER – OLTSEP

For additional information, see System/370 Diagnostic Reference Summary (Order No. SY25-0512).

Preparation

Mount OLTSEP disk or tape and IPL.

Starting OLTSEP

OLTSEP prints:

```
04 SEP188D ENTER DATE AND TIME IN THE FOLLOWING FORMAT 'MM/DD/YY,HH/MM/SS'
```

Reply:
`r 04,'MM/DD/YY'` or `r 04,'MM/DD/YY,HH/MM/SS'` or `PSW RESTART`

OLTSEP prints:

```
        SEP102I OLTS RUNNING
        SEP107I OPTIONS ARE NTL,NEL,EP,CP,NPP,PR,FE,NMI,SI
01      SEP105D ENTER DEV/TEST/OPT
```

If it is desired to run OLTs from card decks, the RDR device must be varied from its default of the IPL device to card. To do this, reply:

```
r 01,'VARY RDR=00C'
```

00C is the address of the card reader. Modify the address to conform to your system.

OLTSEP prints:

```
        SEP219I VARY COMPLETE
01      SEP105D ENTER DEV/TEST/OPT
```

If the RDR device is to remain the IPL device, do not reply with the VARY command.

Make a Run Request

Make a run request to select the test you want to run.
Reply:

```
r 01,'160/3350PSA//'
```

(See OLT descriptions, OLT 20 through 26.)

This reply begins testing on device 160, runs OLTS section PSA, and uses the default options. To select another sequence of testing, enter a reply of:

```
r 01,'160/3350PSA,2/NFE/'
```

This runs only routine 2 of the OLT section PSA, and causes all the default options to be selected except the option FE (first error communications), which will be altered to NFE.

See OS/VS-OLTEP Make a Run Request on OLT 6 for additional examples.

Options

OPTION	YES	NO	DEFAULT
TEST LOOP	TL (VALUE)	NTL	NTL
ERROR LOOP	EL		
	EL(I)		
	EL (VALUE)	NEL	NEL
ERROR PRINT	EP	NEP	EP
CONTROL PRINT	CP	NCP	CP
PARALLEL PRINT	PP (VALUE)	NPP	NPP
PRINT	PR	NPR	PR
FIRST ERROR COMM.	FE	NFE	FE
MANUAL INTERVENTION	*MI	NMI	NMI
SPURIOUS INTERRUPT	SI	NSI	SI
DATA ENTRY FIELD	EXT=(DATA)	---	---
REMOTE ENTRY	*RE	NRE	RE

RE and MI are mutually exclusive (only one can be on).

Halt OLTSEP

To halt OLTSEP at any time, press the Request key on the console.
OLTSEP prints:

```
        SEP107I OPTIONS ARE ---------
01      SEP105D ENTER DEV/TEST/OPT
```

Reply:
`r 01,'(newDEVice/(newTEST)/(newOPTions)'` New instructions to OLTSEP

or to continue:
`(EOB)`

or to continue or restart the section under test:

```
r 01,'///'
```

or to terminate the section under test:

```
r 01,'CANCEL'
```


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RUNNING REFRESHER – OS/VS-OLTEP

For additional information, see System/370 Diagnostic Reference Summary (Order No. SY25-0512).

Preparation

Units to be tested may be varied offline. This is accomplished through the console by using the Vary command.
Examples:

```
V 160,OFFLINE (Varies unit 160 offline.)
V(160,161,162),OFFLINE (Varies units 160,161, and 162 offline.)
```

(The System replies: `160,161,162 OFFLINE` when the vary is completed.)

SYSRES cannot be varied offline.

3350 OLTS PSA and PSB can be run online and they will not destroy data on any disk. However, to perform maintenance on the drive, you must vary the drive offline before starting OLTEP. If FRIEND (OLT T0200A) is used to write, the drive must be varied offline.

Starting OS/VS-OLTEP

1. S – causes a job to be started if a reader procedure is incorporated in the system.
   Examples:
   ```
   S OLTEP      (For an MVT or VS2 system.)
   S OLTEP.PX (For an MFT or VS1 system, where X is the partition number OLTEP is to run in. If in doubt, ask an
               operator which partition to use.)
   ```
   or
   Use JCL on cards to execute program IFDOLT.
2. Once OLTEP is running, it generates various messages.
   Examples:
   ```
   IFD1021 OLTS RUNNING          (To inform you that OLTEP is running.)
   00 IFD104D REPLY ANY CHARACTER TO REQUEST COMMUNICATION.
   ```
   (A reply of any character to the above request causes a communication interval.)

Make A Run Request

OLTEP waits for a reply after issuing the message.
`01 IFD005D ENTER-DEVICE/TEST/OPTION` (See OLT descriptions, OLT 20 through 28.)

Examples of DEVICE/TEST/OPTION replies: (The commands are given in this sequence.)

1. `r 01,'160/3350PSA/EP/'`
2. `r 01,'/3350PSA//'`
3. `r 01,'161///'`
4. `r 01,'160,163,165/3350PSA,PSB/PP/'`
5. `r 01,'160-163/3350PSA//'`
6. `r 01,'260/3350PSA,2/NEP,MI/NRE/'`

The commands carry forward until they are changed.

Examples	Devices (nine maximum)	Tests	Options
1.	160	3350PSA	EP,CP,PR,FE,SI
2.	160	3350PSA	EP,CP,PR,FE,SI
3.	161	3350PSA	EP,CP,PR,FE,SI
4.	160,163,165	3350PSA and PSB	PP,EP,CP,PR,FE,SI
5.	160,161,162,163	3350PSA	EL,EP,CP,PR,FE,SI
6.	260	3350PSA routine 2 only	PR,FE,MI,SI

Options

Use the OPTIONS list from OLTSEP, OLT 5.

Halt OS/VS-OLTEP

Reply to the outstanding request with any character to force communication.
OLTEP prints:

```
01 IFD005D ENTER--DEVICE/TEST/OPTION/
```

Reply:

```
r 01,'CANCEL' (This cancels OLTEP.)
```


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RUNNING REFRESHER – DOS-OLTEP

For additional information, see System/370 Diagnostic Reference Summary (Order No. SY25-0512).

Preparation

Units to be tested must not be assigned to either of the Foreground Programs. The Background Program must be available for CE use.

Starting DOS-OLTEP

Job Control Cards may be put in the reader or JCL commands may be entered from the system console. The example shown is for the console.

```
AR  START BG
BG  // JOB OLTEP
BG  //ASSGN SYS014, X'160'
BG  //EXEC IJZADOLT, REAL, SIZE=28K
BG  E0021 OLTS RUNNING
BG  E005D ENTER -- DEV/TEST/OPT/
```

This is printed after the first error, after operating the Interrupt switch, or at job completion.

Make a Run Request

Make a run request to select the test you want to run.
Reply:

`r 01,'160/3350PSA//'` (Test 160 with 3350PSA.)
`BG E158I ST3350A UNIT 0160` (Testing has begun.)

Option Field Entries

`/` (Run with default options on initial request only.)
`NTL,NEL,EP,CP,NAP/` (Run with default options.)
`AP/` (Run with default options but print on SYSLST.)

Halt DOS-OLTEP

To halt DOS-OLTEP at any time, operate the CP/Interrupt switch.
DOS-OLTEP prints:

```
BG 01E105D ENTER - DEV/TEST/OPT
```

Reply:

```
BG R 01,'Cancel'
```


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3350 OLT REQUIREMENTS

3350 OLT Tests

PSA – HA and R0 Format and Readability on 3350 HDA.
PSB – Data Readability (burst check) on 3350 HDA.
PSC – SD Directory and HA Recovery
WT – Write test on any selected track.
T0200A – OLT(S)EP Friend

These tests are described on OLT 20 through 26.

Program Requirements

3350 OLTs run under DOS OLTEP REL 32, VS1 OLTEP release 5, VS2 OLTEP release 3 (with ICR), or OLTSEP release 8.0 or higher.
3350 OLTs test 3330 Compatibility Mode volumes under operating systems that support the 3330.

OLTEP requires a system or private library containing:

- Standalone Online Test Support Processor (SOSP)
- Configuration Data Set (CDS), see 3350 CDS description.
- 3350 OLT Sections.

OLTSEP requires a load tape or disk load file containing:

- IPL Loader.
- OLTSEP Nucleus.
- OLTSEP Transient Modules.
- Standalone Online Test Support Processor (SOSP).
- Configuration Data Set (CDS), see 3350 CDS description.
- 3350 OLT Sections.

For additional information, see *OLT Users Guide (D99-3350) and System/370 Diagnostic Reference Summary* (SY25-0512).

Equipment Requirements

3350 OLTs may be run on any 3350 string. There are no special equipment requirements.

3350 Configuration Data Set (CDS)

Configuration data must be correctly supplied in the OLTEP or OLTSEP libraries. CDS for the 3350 should appear as follows (one card per drive):

CC 01	Blank
CC 02–04	CDS
CC 10–17	Device Address (Example – 0000 0160)
CC 18–19	Blank
CC 20–21	Feature Code (02 = 3830-2 or ISC storage control) (10 = 3830-3 staging adapter storage control) (Blank = other attachment)
CC 22–23	Device class (20)
CC 24–25	Device Type (Mode, see Note.) 3350 = 0B 3330-1 = 09 3330-11 = 0D
CC 26–29	Blank
CC 30–31	Flags (04 = 2-channel switch or string switch installed) (40 = device shared) (44 = both of the above)
CC 32–35	Blank
CC 36–37	CUCDS suffix (see 3830 CDS requirements)
CC 38	/

These cards for other devices on the system must be included in CDS.

SOSP

The Standalone Online Test Support Processor (SOSP) may be used to create a master load tape or disk load file for OLTSEP. SOSP does not support the 3350 as a resident device.

SOSP also has facilities for the following:

- Add, replace, or delete OLTs from the master file.
- Duplicate master files (DUP).
- Print the contents of a master file (LIST).
- Generate and modify the Configuration Data Set (CONFIG).

The SOSP Operators Guide (D99-SOSPB) has details for selecting the options.

Error Messages

To locate the error message referenced by the error printout, use the section number and REFNUM from the first printout line as an index to OLT pages starting on OLT 40. Messages with REFNUMs ending in 91 through 99 are common to all sections and are found at the start of the error message listing under Common Error Messages (see OLT 40, 50, and 60).

Note: *At least one CDS card must be included with Device Type 0B(3350) for correct 'Autoedit' function. If there are no drives in 3350 Mode, add a dummy CDS with Class 20, Device Type 0B.*

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TEST DESCRIPTIONS

USE OF OLTs

The Online Tests for the 3350 are designed to test the following:

- The readability and accuracy of the Home Address and Record Zero fields.
- The data integrity of data records.
- The ability of the 3350 to write and read different bit patterns on selected tracks.

SECTIONS

T3350PSA – HDA HA/R0 Scan (requires 8K)*
T3350PSB – HDA Burst Test (requires 8K)*
T3350PSC – SD Directory and HA Recovery (requires 16K)*
T3350WT – Write Test (requires 8K, attempts to get 8K more storage)*

*CPU storage

T3350PSA HDA HA/R0 SCAN

This section tests the readability and accuracy of HA and R0 fields on the HDA.

Running Considerations

1. This section requires that a completely operational file subsystem be used. Hardware errors invalidate results and the internal retry capability of the storage control must present hard errors to the OLT.

   OLT recalibrate/retry is performed once, then the error is printed and processing continues.

   Thirty hardware errors occurring on any one cylinder cause premature termination of the OLT (see OLT 210, REFNUM 0000A). Appropriate diagnostics should be run against the failing drive and/or corrective action completed before continuing to scan the HDA.

2. This OLT does not scan data on the CE cylinder. The CE cylinder is 1024, heads 0 through 29.

3. If the 3830 Model 2, ISC, or 3880 is placed in Forced Error Logging mode while running this section, errors normally transparent to the system program (retried at the storage control level) are displayed on the test printout. This is most effective for intermittent/soft errors.

   Do not use the Forced Error Logging mode if the string is shared.

Routine Descriptions

Routine 1: This routine is run by default. It scans the entire HDA except the CE cylinder. Home Addresses and Record Zeros are scanned for readability and data accuracy. Invalid HA and/or R0 fields are printed in expected-received form. HA and up to 16 bytes of R0 (8-byte Count field, 8-byte Data field) are displayed when an error is found. Alternate and defective tracks are verified to point to a valid mate. If none is found, an appropriate error message is printed.

Routine 2: This routine must be selected. It allows specific tracks to be tested.

User options:

1. Select track or tracks to be scanned.
2. R0 data length to be tested (8 or any).

Running Details

This OLT requires 4 to 6 minutes to run, or longer when run under VS-OLTEP.

1. In most cases, the default mode of operation (routine 1 only) successfully tests an HDA.

   Enter:
   ```
   /3350PSA//
   ```

2. If some specific area of the HDA is suspected, the test time can be shortened by selecting the track(s) to be tested (routine 2).

   Enter:
   ```
   /3350PSA,2//
   ```

   Message:
   ```
   ENTER TRACKS(S),'ALL'OR'END'
   AS'CCCHH–CCCHH'OR'CCCHH'
   ```

   Reply:
   ```
   'ALL',EOB
   ```
   or
   ```
   'END',EOB
   ```
   or
   ```
   'CCCHH–CCCHH',EOB
   ```
   or
   ```
   'CCCHH',EOB
   ```
   or
   ```
   EOB(DEFAULT='ALL'TRACKS)
   ```

   Valid limits for CCCHH are:
   3350 volume = '00000' through '22F1D'
   3330-1 volume = '00000' through '19412'
   3330-11 volume = '00000' through '32812'

3. If the R0 data is not 8 bytes long:

   Enter:
   ```
   /3350PSA,2//
   ```

   Message:
   ```
   ENTER TRACKS(S),'ALL'OR'END'
   AS'CCCHH–CCCHH'OR'CCCHH'
   ```

   If specific tracks are required:

   Reply:
   ```
   'CCCHH'or'CCCHH–CCCHH'
   ```
   (the identity of the suspect track(s))
   or
   ```
   EOB(DEFAULT='ALL'TRACKS)
   ```

   Message:
   ```
   ENTER R0 DATA LENGTH
   ```

   Reply:
   ```
   'ANY',EOB
   ```
   or
   ```
   '8',EOB
   ```

See OLT 200 for example.

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TEST DESCRIPTIONS

T3350PSB HDA BURST TEST

This section tests the readability of data records on the HDA.

Running Considerations

1. This section requires that the Home Addresses and Record 0s are valid and readable, therefore T3350PSA should be run before T3350PSB.
2. This section also requires that a completely operational file subsystem be used. Hardware errors invalidate results and the internal retry capability of the storage control must present hard errors to the OLT.

   OLT recalibrate/retry is performed once, then the error is printed and processing continues.

   Thirty hardware errors occurring on any one cylinder cause premature termination of the OLT (see OLT 250, REFNUM 0000A). Appropriate diagnostics should be run against the failing drive and/or corrective action completed before continuing to scan the HDA.
3. This OLT does not scan data on the CE cylinder. The CE cylinder is 1024, heads 0 through 29.
4. If the 3830 Model 2, ISC, or 3880 is placed in Forced Error Logging mode while running this section, errors normally transparent to the system program (retried at the storage control level) are displayed on the test printout. This is most effective for intermittent/soft errors.

   Do not use Forced Error Logging mode if the string is shared.

Routine Descriptions

Routine 1: This routine is run by default. It scans the entire HDA for readability (burst check), all records, and all tracks (except CE tracks). A statistical summary is printed at the end of the OLT. All data records are read with the SILI and SKIP bits on. No data is transferred or printed.

Routine 2: This routine must be selected. It allows specific tracks to be tested.

Routine 3: This routine must be selected. It allows a track to be selected for a burst check on that part of the track containing valid data, then forms a tight scope loop.

Running Details

This OLT requires 5 to 30 minutes to run. Running time depends on storage control and HDA usage and density (for special cases, see routine 2 and 3 description).

1. In most cases, the default mode of operation (routine 1 only) successfully tests an HDA.

   Enter:
   ```
   /3350PSB//
   ```
2. If a specific area of the HDA is suspected, the test time can be shortened by selecting the track(s) to be tested (routine 2).

   Enter:
   ```
   /3350PSB,2//
   ```
   Message:
   ```
   ENTER TRACK(s),'ALL'OR'END'
   AS'CCCHH-CCCHH'OR'CCCHH'
   ```
   Reply:
   ```
   'ALL',EOB
   ```
   or
   ```
   'END',EOB
   ```
   or
   ```
   'CCCHH-CCCHH',EOB
   ```
   or
   ```
   'CCCHH',EOB
   ```
   or
   ```
   EOB(DEFAULT='ALL'TRACKS)
   ```
   Valid limits for CCCHH are:

   3350 volume = '00000' through '22F1D'
   3330-1 volume = '00000' through '19412'
   3330-11 volume = '00000' through '32812'
3. If a hardware failure is causing a Data Check:

   Enter:
   ```
   /3350PSB,3//
   ```
   Message:
   ```
   ENTER TRACK FOR SCOPING
   ```
   Reply:
   CCCHH of the track to be looped.

   The OLT starts a tight loop of the track and continues until terminated by a normal console request or OLT(S)EP intervention.

   Command Chain may terminate when an abnormal condition occurs or the last data record has been read. Use OLT T0200A (FRIEND) or 3350 microdiagnostic routine B1 if a full track read of all gaps and fields is desired.

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T3350PSC SKIP DISPLACEMENT OLT

This OLT is designed to create a track-by-track directory (SDMAP) of nonzero SDs (Skip Displacements) and, if necessary, restore the SD information from the directory to one or more tracks, or analyze a track and generate the necessary skip displacement.

The directory of nonzero SDs must be created on each installed HDA and upon installation of a new 3350 or replacement HDA.

ROUTINE DESCRIPTIONS

Default Mode, Build SD Directory Routine M4

The Build SD Directory routine will:

- Build a directory of nonzero SDs on cylinder 561 using the Card Input option.
- Scan all HA/ROs on an HDA, storing a directory of nonzero SDs on cylinder 561.

The Build SD Directory routine will write only on cylinder 561. Customer data will not be destroyed during this step. On newer HDAs the SD Directory may have been written at the plant. (This can be determined by running T3350PSC in default mode.)

OPTIONAL ROUTINES

Any SD loss can be recovered after the SD Directory has been created by using the optional routines of this OLT. Routine M5 will analyze a track and assign a new skip displacement to allow a defect to be skipped thereby eliminating the need to assign an alternate track.

Caution: The Write HA with SD Bytes function is a Format Write. Any existing data on a track that undergoes HA/SD restoration (routines M1, M2, M3, or M5) will be lost.

Routine M1

Routine M1 will restore the SDs to the selected tracks from the directory, or from input provided by the user through CECOMS.

Routine M2

Routine M2 will scan all HA/ROs on an HDA and rewrite those which produce data checks, obtaining SD data from the SD Directory or from the user through CECOMS.

Routine M3

Routine M3 will rewrite all HA/ROs on an HDA, obtaining SD data from the SD Directory or from card input.

Routine M5

Routine M5 will analyze a selected track or range of adjacent tracks on a single surface. If an unusable surface area is found, Routine M5 will develop the necessary skip displacement data to allow use of the track using the skip defect function. This is preferable to alternate track assignment. Routine M5 can be used with both fixed and movable heads. This routine is available in OLT at version level 2.0 or later.

RUNNING CONSIDERATIONS

Invoke the OLT as follows:

1. Install OLT T3350PSC in OLT(S) EP OLTLIB.
2. Ensure that the 3830 Functional microcode disk (P/N 4168811 at EC 437465 with REA 13-57853 or later) is installed.
3. Select OLT xxx-yyy/3350PSC/NFE where xxx-yyy is the address range of 3350s having the SD Directory created.

The T3350PSC will only run against drives that are in native mode. This is necessary so that all tracks on a volume are available to be scanned. After T3350PSC has completed the Build SD Directory run, the CE may return the drive to compatibility mode. (For information on native/compatible plugging, see INST 4.)

Note: *After the reconstructions (routines M1, M2, M3, or M5) have been made in native mode, it will be necessary to reinitialize in compatibility mode to restore the format.*

RUNNING DETAILS

The OLT PSC routines M2 and Build SD Directory run in about 10 minutes under OLTSEP. Routine M3 runs in about 25 minutes. Expected run times for routine M5 are between 3 to 35 minutes per track, depending on system environment. The run is about twice as long under VS1 or DOS OLTEP and up to three times as long under VS2 OLTEP. This OLT is 16,000 bytes long for routines M1 through M4, and 44,000 bytes long for M5. The drive to be run must be offline and in native mode.

When to run OLT T3350PSC

BUILDING AN SD DIRECTORY

Run T3350PSC in default mode:

- On all installed HDA.
- At installation of any 3350 or replacement HDA.

RUNNING DETAILS (Continued)

RESTORING SD DATA

Run T3350PSC using optional routines:

- If AP1 or OLT T3350PSA detects unreadable home addresses.

  FSC = 4940, 4944, or 4949.

  Single Track Failure: use routine M1.

  Multiple Track Failure: use routine M2.

  Unknown extent of damage (HA Read Failure and/or unknown accuracy of SD data in HA fields): use routine M3.

GENERATING SD DATA

Run T3350PSC routine M5:

- If a track has been flagged defective and the user wishes to attempt to recover use of the track.
- If a track has recurring data checks and factory SD is known to be correct (restore routine M1, M2, or M3 has been run).

EQUIPMENT REQUIREMENTS

The following equipment is required:

Storage Control Unit or ISC and 3350 Disk Drive and Controller.

T3350PSC must be used with 3830 functional microdisk, P/N 4168811 at EC 437465 with REA 13-57853 or later.

See OLT Users Guide (Order No. D99-3350) for additional information.

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T3350WT WRITE TEST

This section tests the write and read capability of any selected HDA track. It also tests Index if 3330 Compatability Mode is used. T3350 WT writes a pattern on the CE track that is required for the scoping procedure used with microdiagnostic routine B1, Read test.

Running Considerations

Caution: The following steps must be followed to avoid loss of data.

1. Before running this test, OLT T3350PSA must be run and errors acted upon.
2. This OLT writes on any selected track. To test write and read capability, use only the CE track. The CE track is cylinder 1024 ('X400HH', where HH is head 0 through 29).
3. Always select a CE track first and test write/read. Resolve any errors detected on the CE track before selecting a non-CE track.
4. Always make sure that there is backup for data on a non-CE track or that it has been dumped.
5. If you are unsure about the status of data on the track to be tested, use the options to CHANGE the track selected or TERMINATE the test.
6. Once the data can be considered scratch data, reply GO to begin testing.

Routine Descriptions

Routine 1: This routine writes and reads records that are alternately all zeros and all ones.

Data = 0000.....and FFFF.....

Running time is 20 seconds.

Routine 2: This routine writes and reads records with only one bit set per byte. The bit is then shifted right within the byte.

Data = 80808.....through 010101.....

Running time is 90 seconds.

Routine 3: This routine writes and reads records with the worst case pattern. On each of two successive passes, the pattern is shifted right once to make sure bit shift errors are detected.

Data = DB6DB6D.....,6DB6DB6.....,B6DB6DB...

Running time is 35 seconds.

Routine 4: This is a dummy routine.

Routine 5: This routine only runs if selected.

Enter:

```
'/3350WT,5//'
```

It writes a single 2048 byte record on the track selected, then reads it 1024 times. This write/read routine is repeated ten times.

Data = worst case (DB6DB6D.....)

Running time is 3 minutes.

Routine 6: This routine only runs if selected.

Enter:

```
'/3350WT,6//'
```

A CE track must be selected. This routine writes a 256 byte R1 on the CE track selected and then terminates.

Data = AAAAAAAAFFFFFFFF.....

Running time is 5 seconds.

Running Details

This OLT runs for 2 minutes on each track selected for testing, or longer when run under VS-OLTEP. Each tested track is restored with a standard R0 before another track can be selected. This OLT must be allowed to terminate or be cancelled. Routines 1 through 3 run by default for a thorough write/read test.

Enter:

```
'/T3350WT//'
```

However, any routine or combination of routines can be selected to reduce the run time or to extend the test to include 10,000 reads (see Routine 5 description).

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T0200A FRIEND

The FRIEND OLT is a special diagnostic tool to support diagnosis of unique problems. Complete operation instructions are found in the Maintenance Diagnostic Program Users Guide For Friend (D99-0200).

Running Considerations

FRIEND truncates sense data to the rightmost non-zero byte.

FRIEND runs online under VS/OS/DOS OLTEP or OLTSEP. The Online Test Executive Program (OLTEP) or Online Test Standalone Execute Program (OLTSEP) schedules and controls the activity of FRIEND and provides communication with the operator. An I/O unit may be tested using FRIEND under OLTEP with minimum interference to the operation of other programs running in the system. This provides a method of testing I/O devices while customer programs are being processed by the system. Operation of FRIEND under OLTSEP eliminates the requirement for an operating system (OS) where an OS is not present.

FRIEND allows the user to construct man-readable S/360/370 channel programs.

FRIEND provides no data protection other than that of the OLT(S)EP.

Running Details

SELECTING FRIEND

Enter;

```
T0200A//
```

OLTSEP options (MI, TL, etc.) have no effect when running FRIEND.

If the controller being tested is shared and FRIEND is running standalone under OLTSEP, use Block Multiplex mode (Control Reg 0, bit 0).

After FRIEND is loaded and in control, the following messages are printed:

```
04 SEP1001    FRIEND running V/L=XX
04 SEP1001    Data area in bytes=XXXXX
04 SEP101D    Enter FRIEND command
```

COMMAND ENTRY

The program is now ready to receive user input in the form of CCW commands or interpreter commands. These may be entered singly or as a command string. String data must always end with a slash, for example:

```
SK/CYL=0/HD=0/SIDEQ/RCDNO.=3/TIC/
RDDATAINTO$A/NOP/GO/
```

This reads the volume label into a location known to FRIEND as $A. As each successive command or command string is entered, FRIEND processes each one and then prints 'ENTER CMND' when that command or string has been processed and it is ready to accept additional input. If more information is required, FRIEND asks for it. The FRIEND OLTSEP does not insert any CCW commands (such as SFM, TIC, or SET MODE).

TERMINATING FRIEND

Enter:

```
r04,END
```

FRIEND Examples

To verify a possible bad track, enter:

```
SK/CYL=XXX/HD=XXX/RDHAINTO$A
/RDR0INTO$B/KL=0/DL=8/GO/
```

To rewrite a bad track (standard R0), enter:

```
SFM/MASK=C0/SK/CYL=XX/HD=XX/
SRCHEQHA/TIC/WRR0/KEY=0/DATA=8X00/GO/
```

MASK=C4 must be entered to SK/WRITE on a CE track (cylinder 1024, heads 0 through 29).

Command Summary

Primary	Alternate	(hex)	Explanation
No Operation	NOP	03	No Operation
Seek	SK	07	Control Seek
Recalibrate	RECAL	13	Recalibrate
Restore	RESTR	17	Restore
Set File Mask	SFM	1F	Set File Mask
Seek Cyl	SKCYL	0B	Seek Cylinder
Seek Hd	SKHD	1B	Seek Head
Release (see Note)	REL	94	Release
Reserve (see Note)	RSV	B4	Reserve
Space Count	SPCNT	0F	Space Count (Space Record)
Set Sector	SS NO	23	Set Sector
Diagnostic Ld	DL	53	Diagnostic Load
Sense	SNS	04	Read 24 bytes, Sense information.

In the following Search commands, SEARCH, SRCH, SCH, or S can be used. MT indicates multitrack and is entered preceding a Read or Search command. Example: MT SEARCH ID or MT READ CNT.

Primary	Alternate	(hex)	MT	Explanation
Sch HA Eq	SRCHEQHA	39	B9	Search Home Address Equal
Sch ID Eq	SRCHEQID	31	B1	Search Identifier Equal
Sch ID Hi	SCHHIID	51	D1	Search Identifier High
Sch ID Eq Hi	SEQHIID	71	F1	Search Identifier Equal or High
Sch Key Eq	SEQK	29	A9	Search Key Equal
Sch Key Hi	SHIK	49	C9	Search Key High
Sch Key Eq Hi	SEQHIK	69	E9	Search Key Equal or High
Read HA	RDHA or RH	1A	9A	Read Home Address
Read Count	RDCNT or RC	12	92	Read Count
Read R0	RDR0 or RR0	16	96	Read Record Zero
Read Data	RDDT or RDD	06	86	Read Data Field
Read Key Data	RDKDT or RKD	0E	8E	Read Key Data
Read Count Key Data	RDCKD or RCKD	1E	9E	Read Count Key Data
Read IPL	RDIPL READ RD	02		Read IPL (Initial Program Load)
Read and Reset Buffered Log	RDBL, 3330 RDLG, 3330	A4		Read and Reset Buffered Log
Read Diagnostic Status	RDDS	44		Read Diagnostic Status

Primary	Alternate	(hex)	Explanation
Read Sector	RDS	22	Read Sector
Write HA	WHA WRHA		Write Home Address (requires Set File Mask and SHAEQ command preceding, or the defective track bit on in the flag byte)
Write R0	WRTR0 WRR0	15	Write Record Zero (requires Set File Mask)
Write Count Key Data	WRTCKD WRCKD WCKD	1D	Write Count Key Data
Write Special Count Key Data	WRSPCKD	01	Write Special Count Key Data (optional feature)
Write Key Data	WRTKD WRKD WKD	0D	Write Key Data
Write Data	WRTDT WRD WD	05	Write Data
Erase	RS	11	Erase (WRCKD without address marker)
Diagnostic Write	DWRT DW	73	Diagnostic Write

Note: *Channel Attachment and 2 Channel Switch or String Switch feature are required for the Release and Reserve commands.*

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CCW CHAIN EXAMPLES

1. Chain to fetch volume ID:

   SEEK (cyl=0,hd=0)
   SIDEQ (rcd no.=3)
   TIC (to SIDEQ)
   RDDATA (byte count=10)

2. Chain to burst check record n:

   SEEK (incremented)
   SFM ('18') inhibit seeks and head switching
   SIDEQ (rcd no.=n–1)
   TIC (to SIDEQ)
   MTRDCKD (byte count=8,DC)
   MTRDCKD (byte count=20000,SKIP,SILI)

3. Chain to bypass bad record n:

   SEEK (current track)
   SFM ('18') inhibit seeks and head switching
   SIDEQ (rcd no.=n–1)
   TIC (to SIDEQ)
   SPCNT (argument=000)
   MTRDCKD (byte count=8, DC)
   MTRDCKD (byte count=20000,SKIP,SILI)

4. Chain to scope loop track:

   SEEK (to CE selected track)
   SFM ('18') inhibit seeks and head switching
   SPCNT
   MTRDCKD (byte count=8,DC)
   MTRDCKD (byte count=20000,SKIP,SILI)
   TIC (to first MTRDCKD)

5. Chain to burst check cylinder:

   SEEK (incremented)
   SET SECTOR (0)
   MTRDCKD (byte count=20000,SKIP,SILI)
   TIC (to MTRDCKD)

   A failure in this chain causes the cylinder to be scanned in detail, a record at a time (see Chain 2 above).

6. Chain to read HA, SD, and RO:

   SFM (C0 or C4)
   SEEK
   RDHA
   SNS (BC = 24)
   RDRO (BC =4,SILI)

7. Chain to read VOL ID:

   RECAL
   SRCIDEQ (R3)
   TIC (to SRCIDEQ)
   READ DATA (BC = 10,SILI)

8. Chain to read RO:

   SFM (C0 or C4)
   SEEK
   RDRO (BC = 20000,SKIP,SILI)

9. Chain to read R1 through Rn (if not a CE track):

   SEEK
   SFM ('18') inhibit seeks and head switching
   SRCIDEQ (RO)
   TIC (to SRCIDEQ)
   MTRDCKD (BC = 20000, SKIP, SILI)
   TIC (to MTRDCKD)

10. Chain to read Rn (if CE track):

    SFM (C4)
    SEEK
    SRCIDEQ (Rn – 1)
    TIC (to SRCIDEQ)
    RDCKD (BC = 20000, SKIP, SILI)

11. Chain to Read HA/RO:

    SFM ('00')
    SEEK (cyl/hd incremented)
    RDHA
    RDRO (byte count=16, DC)
    RDRO (byte count=20000,SKIP+SILI)

12. Chain to write HA (if defective or alternate track is tested):

    SFM (C0 or C4)
    SEEK
    SRCHAEQ
    TIC (to SRCHAEQ)
    WRTHA (BC = 11 if type 0B,
      5 if type 09 or 0D)
    WRTRO (BC = 16)
    NOP

13. Chain to write RO:

    SFM (C0 or C4)
    SEEK
    SRCHAEQ
    WRTRO (BC=8,DC)
    NOP (BC=2048)
    NOP

14. Chain to write Rn:

    SFM (CO or C4)
    SEEK
    SRCIDEQ (n–1)
    TIC (to SRCIDEQ)
    WRTCKD (BC=8,DC)
    NOP (BC=1 to 8192)
    NOP

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PURPOSE OF THIS PAGE

This page is referenced by many of the Online Test pages. It contains instructions that are commonly used when OLT errors are found.

COMMON ACTION B

1. If a Fault Symptom Code (FSC) is not included in Sense Bytes 22 and 23, go to START 101 for Sense Byte analysis. If this step does not correct the problem, continue below.
2. The first error listed is probably the most valid error to investigate. Additional error data can be obtained by running all OLTs, and this additional information will reinforce or refute the original error.
3. Determine the failing CCW (marked by an *) and run microdiagnostics that verify the failing function. Select the appropriate microdiagnostic by checking the descriptions in the MICRO section of the MIM. The failing CCW may not reflect the test in process. An analysis of the chain printout will prevent misinterpretation of an invalid result. For example, the message HA READ=XXXXX is invalid if the Read HA command was not executed.
4. Was the OLT properly run? See Running section of OLT description (OLT 20 through 26).
5. Determine the failing CCW (marked by an *) and refer to the storage control maintenance documentation for the CCW description.

COMMON ACTION C

Use a DASDI utility program to correct tracks with unreadable or incorrect Home Addresses or R0s.

1. Control the DASDI program to flag the track as defective. If recovery or restart is desired without re-initializing the volume, go to Step 3.
2. Rerun the DASDI program on the HDA. All defective tracks are tested. If a track previously flagged is now usable, it is recovered and the Home Address and R0 are corrected.
3. Always run OLT T3350PSA on the volume after correcting format errors.

See OLT 30 for additional information on rewriting Home Address and R0.

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ALTERNATE TRACK ASSIGNMENT

DEFINITIONS

Alternate Track

An alternate track is used in place of a primary track. Alternate tracks are designated by the manufacturer and are logically addressed as follows:

3350	cylinders 555 – 559, heads 0 – 29
3330-1	cylinders 404 – 410, heads 0 – 18
3330-11	cylinders 808 – 814, heads 0 – 18

Unassigned alternate tracks contain their own logical track address in the CCHH bytes of the HA and R0 Count field. On a 3350 volume, bit 7 of the flag byte in the HA field is set to identify the track as an alternate. On a 3330 compatible volume, bit 7 of the flag byte may be set to 0 until the track is assigned to a defective primary track.

Defective Track

A defective track contains one or more surface defects that cause Read Data Checks. When the track is identified as defective, bit 6 of the flag byte in the HA field is set.

A defective alternate track will have both bits 6 and 7 of the flag byte set.

HOW TO REWRITE AN INCORRECT HA OR R0

To rewrite an unreadable or incorrect Home Address (HA) or Record 0 (R0), follow Step 1, 2, 3, or 4.

1. Run IBCDASDI, INTDK, or IEHDASDR to format the volume.
2. Run ICKDSF or ICLDSF to inspect the track.
3. Run IBCDASDI, ALTDK, or IEHDASDR to flag the track as defective. Then run the DASDI program again to analyze, and if possible, reclaim the track.
4. Run OLT T3350 PSC using routines M1, M2, or M3.

HOW THE UTILITIES ASSIGN AN ALTERNATE TRACK

Note: *The selected track(s) can be checked prior to flagging and assigning an alternate (conditional assignments).*

1. The R0 Count field on the alternate track is written with CCHH bytes equal to the address of the defective track.
2. The R0 Count field on the defective track is written with CCHH bytes equal to the address of the alternate track.
3. Bit 6 of the flag byte in the HA field on the defective track is set.

OS/VS UTILITIES

General utility programs are available with OS/VS operating systems to aid in alternate track assignment and HDA initialization. Because alternate track assignment is a customer responsibility, the following is for information only. For more detail, see *OS/VS Utilities* (Order No. GC35-0005).

IBCDASDI (standalone initializer)

A standalone utility used to initialize an HDA:

- Flags tracks defective and assigns alternate tracks. The track to be flagged is tested, and if found to be usable, is not flagged. Use the option BYPASS = YES to force flagging.
- Writes volume label on track 0, record 3.
- Writes an IPL record on track 0.
- Allows tracks flagged defective to be analyzed and reclaimed if they are usable.
- Formats a 3350 HDA or a 3330-1, or 3330-11 compatible volume.
- Writes R0 on each track.

See OLT 31 for additional information on using IBCDASDI to rewrite a home address and flag the track.

IEHDASDR (online initializer)

An online utility used to initialize an HDA:

- Performs the same functions as IBCDASDI.
- Can be used to dump or restore the contents or a portion of the contents of a 3350 HDA or 3330 compatible volume.

See OLT 34 for additional information on using IEHDASDR to rewrite a home address and flag the track.

IEHATLAS (assign alternate track)

A system utility used to assign and write an alternate track:

- Attempts to rewrite defective record(s) with data supplied by the user.
- Flags a track defective if it cannot be rewritten successfully.
- Locates and assigns an alternate track.
- Retrieves and transfers usable data records from the defective track to the alternate track.
- Replaces bad records with data supplied by the user.

Alternate tracks cannot be assigned for defects in Home Address or R0 Count fields. Tracks flagged defective cannot be reclaimed. Use IBCDASDI or IEHDASDR.

ICKDSF (Online)(ICLDSF (Standalone) Initializer

For more detail, see *Device Support Facility (DSF)* (Order No. GC 35-0033).

A system utility that can be used to:

- Check the track surfaces and assign alternate tracks to defective tracks.
- Reclaim tracks that were previously flagged defective if the results of surface checking shows there are no recording errors.
- Perform housekeeping and formatting with or without surface checking.
- Write a volume serial number in the volume label.
- Validate the home address and write record zero for each track.
- Erase data from a previously initialized volume if the volume serial number and owner identification are verified.
- Create a pack map that describes the format of a volume.
- Repair HA/R0s on all or selected tracks.

See OLT 40 for additional information on using ICKDSF/ ICLDSF for alternate track assignment.

DOS/VS UTILITIES

General utility programs are available with DOS/VS operating systems to aid in alternate track assignment and HDA initialization. Because alternate track assignment is a customer responsibility, the following is for information only. For more detail, see *DOS/VS System Utilities* (Order No. GC33-5381).

INTDK (initialize disk)

A system utility used to initialize an HDA:

- Reads and verifies HA and R0 fields.
- Writes volume label on track 0, record 3.
- Constructs and writes a volume table of contents (VTOC) on cylinder 0, track 0.
- Allows tracks flagged defective to be analyzed and reclaimed if they are usable.

Alternate tracks are not assigned for tracks flagged defective. It is assumed that any track that is flagged defective has previously had an alternate assigned. To assign an alternate track, use ALTDK or standalone IBCDASDI.

ALTDK (assign alternate track)

A system utility used to assign and write an alternate track:

- Flags defective track.
- Locates and assigns an alternate track (requires a valid VTOC on the volume).
- Retrieves and transfers usable data records from the defective track to the alternate track.
- Replaces bad record(s) with data supplied by the user.
- The condition of the defective track is not analyzed.

Alternate tracks cannot be assigned for defects in Home Address or R0 Count fields. Tracks flagged defective cannot be reclaimed. Use standalone IBCDASDI.

See OLT 37 for additional information on using ALTDK to rewrite a home address and flag the track.

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ALTERNATE TRACK ASSIGNMENT IBCDASDI

Caution: The use of this program will destroy any existing data on the selected track. The customer should do the flagging when that action is required. The information provided here is to enable the CE to advise and assist the customer when necessary.

Assigning an Alternate Track

IBCDASDI can be used to: (1) test a track and, if necessary, assign an alternate or (2) bypass testing and automatically assign an alternate.

Only 3350 (native) devices are tested before alternate tracks are assigned.

If testing is performed, an alternate track is assigned for any track found defective. If the defective track is an unassigned alternate, it is flagged to prevent its future use. The alternate track address is made known to the operator.

If a track is tested and not found to be defective, no alternate is assigned. The operator is notified by a message.

If testing is bypassed, an alternate track can be assigned for the specified track or its alternate, whether it is defective or not. If the specified track is an unassigned alternate, it is flagged to prevent its future use.

Executing IBCDASDI

IBCDASDI is loaded as a card deck or as card images on tape. Control statements for the requested program can follow the last card or card image of the program, or can be entered on a seperate input device. To execute IBCDASDI:

1. Place the object program deck in the reader or mount the tape reel that contains the object program.
2. Load the object program from the reader or tape drive by setting the load selector switches and pressing the console Load key. When the program is loaded, the wait state is entered and the console lights display the hexadecimal value 'FFFF'.
3. Define the control statement input device in one of the following ways:
   a. Press the Request key of the console typewriter and, in response to the message DEFINE INPUT DEVICE, enter INPUT = xxxx,cuu. The *xxxx* is the device type, *c* is the channel address, and *uu* is the unit address. The device type can be 1402, 2400, 2501, 2540, or 3505.
   b. If the console typewriter is not available or unsupported, enter at storage location '0110' (hexadecimal): 1*cuu* for a 1442 Card Read Punch; 2*cuu* for a 2400 9-track tape unit; or 0*cuu* for a 2540 Card Read Punch, 2501 card reader, 3410 tape, or 3420 tape. Press the console Interrupt key.
4. Control statements are printed on the message output device. At the end of the job, END OF JOB is printed on the message output device, and the program enters the wait state.

INPUT AND OUTPUT

I BCDASDI uses as input a control data set, which consists of utility control statements.

IBCDASDI produces as output an initialized direct access volume and a message data set.

CONTROL

IBCDASDI is controlled by utility control statements. Because IBCDASDI is an independent utility, operating system job control statements are not used.

Use IEHDASDR for online initialization of all supported DASD.

UTILITY CONTROL STATEMENTS

All utility control statements/operands must be preceded and followed by one or more blanks.

IBCDASDI utility control statements in the order in which they must appear are:

Statement	Use
JOB	Indicates the beginning of an IBCDASDI job.
MSG	Defines an output device for operator messages.
GETALT	Assigns an alternate track on a volume.
END	Indicates the end of an IBCDASDI job.
LASTCARD	Ends a series of staked IBCDASDI jobs.

JOB Statement

The JOB statement indicates the beginning of an IBCDASDI job. Examples on OLT 32.

The format of the JOB statement is:

1 [*label*] **JOB** [*user-information*]

MSG Statement

The MSG statement defines an output device for operator messages. It follows the JOB statement and precedes any function definition statements.

The format of the MSG statement is:

2 [*label*] **MSG** **TODEV** = *xxxx*
,TOADDR = *cuu*

GETALT Statement

The GETALT statement is used to assign an alternate track on a volume. Any number of alternate tracks can be assigned in a single job by including a GETALT statement for each track.

Note: *A GETALT statement that applies to a 3330, 3330-1, or 3340/3344 device causes an alternate track to be assigned automatically without testing.*

The format of the GETALT statement is:

3 [*label*] **GETALT** **TODEV** = *xxxx*
,TOADDR = *cuu*
,TRACK = *ccchhhh*
,VOLID = *serial*
[,BYPASS = {**YES**|**NO**}**]**

The GETALT function should not be used immediately after a Restore operation that did not complete successfully. Before using GETALT in such a case, reinitialize the volume, if possible.

END Statement

The END statement denotes the end of job. It appears after the last function definition statement.

The format of the END statement is:

4 [*label*] **END** [*user-information*]

END must be preceded and followed by at least one blank.

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ALTERNATE TRACK ASSIGNMENT IBCDASDI

Caution: IBCDASDI will destroy any existing data on the specified track and head.

Operands	Applicable Control Statement	Description of Operands/Parameters
BYPASS	GETALT G	**BYPASS=YES** Applicable to 3350. Causes an alternate track to be assigned without testing the track to be flagged. **Default:** BYPASS=NO Test the track to be flagged and assign an alternate only if the test results are in error (data check).
TOADDR	MSG C GETALT E	**TOADDR=***cuu* Specifies the channel number, *c*, and unit number, *uu*, of the message output device (MSG), or the direct access device.
TODEV	MSG B GETALT D	**TODEV=***xxxx* Specifies the type of device to receive messages. All supported tape drives and the following unit-record devices: 1403, 1443, 1052, 3210, 3215, 3211, and 3800. specifies the type of DASD device.
TRACK	GETALT H	**TRACK=***cccchhhh* Specifies the hexadecimal address if the track for which an alternate is requested, where *cccc* is the cylinder number and *hhhh* is the head number.
user-information	JOB A END	[*user-information*] Specifies user explanation of action.
VOLID	GETALT F	**VOLID=** *serial* **SCRATCH** Specifies the volume serial number of the volume to which an alternate track is to be assigned. If *serial* does not match the volume serial number found on this volume, the o operator is notified and the job is terminated. SCRATCH specifies that no volume serial number check is to be made.

IBCDASDI EXAMPLE

In this example, three alternate tracks are assigned to a disk volume, without reinitialization of the volume. The check for a defective track is bypassed when the three tracks are assigned.

```
        END
        4
            BYPASS=YES,TRACK=004B0007
STMT3   GETALT TODEV=3350,TOADDR=150,VOLID=P20000,
            BYPASS=YES,TRACK=00910004
STMT2   GETALT  TODEV=3350,TOADDR=150,VOLID=P20000,
            BYPASS=YES,TRACK=006F0001
                G          H
STMT1   GETALT  TODEV=3350,TOADDR=150,VOLID=P20000,
            3          D          E          F
            MSG  TODEV=1052,TOADDR=009
            2          B          C
ALTRK       JOB  ASIGN ALTERNATE TRACKS ON 3350
            1          A
```


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ALTERNATE TRACK ASSIGNMENT IEHDASDR

Caution: The use of this program will destroy any existing data on the selected track. The customer should do the flagging when that action is required. The information provided here is to enable the CE to advise and assist the customer when necessary.

ASSIGNING ALTERNATE TRACKS FOR SPECIFIED TRACKS

IEHDASDR can be used to assign an alternate track on a disk volume. An alternate track can be assigned for any track, only if it is defective. If the specified track is an alternate, a new alternate is assigned. If the specified track is an unassigned alternate, it is flagged to prevent its future use.

INPUT AND OUTPUT

IEHDASDR uses as input a control data set containing utility control statements, and optionally, IPL text.

The primary output or result of executing IEHDASDR is determined by the application.

A sequential message data set is created to list informational messages (for example, control statements used), dumped data (for a print operation), and any error messages.

IEHDASDR provides a return code to indicate the results of program execution. The return codes and their meanings are:

- 00, which indicates successful completion.
- 04, which indicates that an unusual condition was encountered; however, the overall result is successful. A warning message is issued.
- 08, which indicates that a specified operation did not complete successfully. An attempt is made to perform any additional operations.
- 16, which indicates that either an error occurred upon invoking IEHDASDR, or IEHDASDR was unable to open the input or message data set. The job step is terminated.

CONTROL

IEHDASDR is controlled by job control statements and utility control statements. The job control statements are used to execute or invoke IEHDASDR and define the data sets used and produced by IEHDASDR.

The utility control statements are used to control the functions of the program.

JOB CONTROL STATEMENTS

The job control statements necessary for using IEHDASDR are shown below. Examples on OLT 35.

The *anyname* DD statement can be entered:

```
//anyname DD UNIT=xxxx,VOLUME=SER=xxxxxx,
DISP=OLD
```

Statement	Use
1 JOB	Initiates the job.
2 EXEC	Specifies the program name (PGM = IEHDASDR) or, if the job control statements reside in a procedure library, the procedure name.
3 SYSPRINT DD	Defines a sequential message data set. The data set can be written to a system output device, a tape volume, or a direct access device.
4 anyname DD	Defines a direct access device type.
5 SYSIN DD	Defines the control data set. The control data set usually resides in the input stream; however, it can be defined as a blocked or unblocked sequential data set or as a member of a procedure library.

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ALTERNATE TRACK ASSIGNMENT IEHDASDR

UTILITY CONTROL STATEMENTS

The utility control statements used to control IEHDASDR are defined below.

GETALT Statement 6

The GETALT statement is used to assign an alternate track for a specified disk track if the volume was previously initialized.

For 3350 volumes, alternate tracks will be assigned only if an error is detected during surface analysis.

The format of the GETALT statement is:

[*label*] **GETALT** **TODD**=*ddname*
,**TRACK**=*ccccHHHH*

where:

(A) **TODD**=*ddname*

Specifies the ddname of a job control statement defining a disk device containing a volume on which an alternate track is to be assigned.

(B) **TRACK**=*ccccHHHH*

Specifies in hexadecimal the cylinder number, *cccc*, and head number, *HHHH*, of a track for which an alternate track is requested. **TRACK** cannot specify track 0 or the first track occupied by the VTOC.

IEHDASDR EXAMPLE

In this example, alternate tracks are to be assigned for three suspected defective tracks on a 3350 volume. The suspected defective tracks are tested and alternate tracks assigned only for those tracks found defective.

The control statements are discussed below:

- VOLUME 1 DD defines a device that is to contain the 3350 volume (222222).
- SYSIN DD defines the control data set, which follows in the input stream.
- The GETALT statements specify the ddname of the DD statements defining the device on which the 3350 volume is mounted . The GETALT statements specify the relative track addresses of the tracks for which alternates are to be assigned.

```
/*
        GETALT  TODD=VOLUME1,TRACK=01010002
        GETALT  TODD=VOLUME1,TRACK=00A00007
        GETALT  TODD=VOLUME1,TRACK=00050011
          6              A             B
//SYSIN       DD      *
  5
// VOLUME=(PRIVATE,,SER=(222222))
//VOLUME1     DD      UNIT=(3350,,DEFER),DISP=KEEP,
 4
//SYSPRINT    DD      SYSOUT=A
 3
//          EXEC PGM=IEHDASDR
             2
//DASDR3  JOB
            1
```


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ASSIGN ALTERNATE TRACK DISK (ALTDK)

Caution: The use of this program will destroy any existing data on the selected track. The customer should do the flagging when that action is required. The information provided here is to enable the CE to advise and assist the customer when necessary.

DESCRIPTION

ALTDK is used to assign an alternate track on a disk device, and to copy data from a defective track to an alternate track. If an alternate track is found to be defective, a new alternate track must be assigned to the primary track.

ASSIGNING AN ALTERNATE TRACK

Specifications in the utility modifier statement identify the defective track. The format-4 record of the VTOC (volume table of contents) on the disk pack identifies the alternate track.

The records from the defective track are transfered to the alternate track, beginning with the data area of RO (track descriptor record), and continuing with the count, key, and data areas of R1 through Rn.

The VTOC format-4 record is modified to contain the address of the next available alternate track. The condition of the defective track may then be analyzed, depending upon the specifications in the utility modifier statement.

When an IBM 3350 is used, an alternate track is assigned unconditionaly. The condition of the track is not analyzed.

Effects of Defective Areas

Defective areas on the defective track may effect the transfer of records to the alternate track. They may also cause the program to terminate. The possible location of defective areas and their effect on program processing are shown in Figure 1.

Figure 1: Defective Area Effect

Defective area	Effect
Address marker of a record. Gap preceding the count area of a record. Count area of a record.	The record is bypassed and is not transferred to the alternate track.
Key area of a record. Data area of a record.	The record is transferred to the alternate track exactly as it is read.
Gap following the count area of a record.	The count area is transferred to the alternate track. The key and data areas are filled with A's on the alternate track.
Gap following the key area of a record.	The count and key areas of the record are transferred to the alternate track. The data area is filled with A's on the alternate track.
Gap between the data area of a record and the address marker of the next record.	The records are transferred to the alternate track exactly as they are read.
HA of the track. R0.	IBM 3350: The appropriate Skip Displacement (SD) value. which depends on error location and device type, is used to bypass the defective area and assign an alternate track. If an error persists after use of SD value, the program is terminated (the track cannot be flagged defective).

Record Printing Option

By means of the output option parameter Ox, you can specify in the utility modifier statement whether you want to print all records transferred to the alternate track, or only those that were read in error from the defective track. The records are printed on the device assigned to SYSLST.

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ASSIGN ALTERNATE TRACK DISK (ALTDK)

UTILITY MODIFIER STATEMENT

Contains information required to run the program.

The format entries are:

```
// UAT R=(cccchhh),Ox,Ix,Cn,Ux
```

The parameters are not positional. The first parameter, R=(cccchhh), must be supplied. The other parameters have the following default values:

```
// U R=(cccchhh),OY,IF,UN
```

1	// U	Utility modifier statement entry.
	AT	Indicates the Assign Alternate Track Disk program. Can be omitted.
2	R=	Indicates the track location parameter.
	(cccchhh)	Indicates the track to which an alternate track will be assigned, or a track whose condition flag is to be changed from defective to non-defective. cccc = cylinder number (decimal) 0 - 554 hhh = head number (decimal) 0 - 29
4	Ox	Identifies the output option parameter.
	x=N	Indicates that only the records found to be in error must be printed.
3	Ix	Identifies the input option parameter.
	x=F	Indicates that an alternate track is to be assigned without surface analysis.

ALTDK EXAMPLE

In the following example, 3350 address 191 will have an alternate track assigned for cylinder 27, head 3.

```
/&
                LAST CARD
// UAT  R=(0027003),IF,ON
   1        2        3 4
// EXEC  ALTDK
                PROGRAM TO BE EXECUTED
// ASSIGN  SYS000,X'191'          ASSIGNMENT CARD   SYS000=SYMBOLIC OUTPUT DEVICE
                                                     X'191'=DASD ADDRESS
// JOB  ALTRK
                'JOB' STATEMENT
```


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ALTERNATE TRACK ASSIGNMENT ICKDSF/ICLDSF

For more detail, see *Device Support Facility* (Order No. GC 35-0033).

Caution: The use of this program will destroy any existing data on the selected track. The customer should do the flagging when that action is required. The information provided here is to enable the CE to advise and assist the customer when necessary.

ICKDSF/ICLDSF

ICKDSF/ICLDSF can be used to:

- Check the track surfaces and assign alternate tracks to defective tracks. See example 1, OLT 44.
- Reclaim tracks that were previously flagged defective if the results of surface checking shows there are no recording errors. See example 2, OLT 44.
- Validate the home address and write record zero for each track. See example 3, OLT 44.
- Assign alternate track(s) without checking the track surfaces. See example 4, OLT 44.

Size Estimates

Both the system-supported (ICKDSF) and the stand-alone (ICLDSF) versions of the Device Support Facility require a minimum of 256K bytes of main storage for execution.

ICKDSF (OPERATING SYSTEM)

OS/VS JCL statements are used to invoke the Device Support Facility processor when running a job or job step. The Device Support Facility processor is identified by PGM = ICKDSF in the EXEC statement.

```
//JOBNAME     JOB    YOUR INSTALLATION'S
//                   JOB-ACCOUNTING DATA
//JOBCAT      DD     DSNAME=YOUR.CATALOG,
//                   DISP=SHR
//STEP 1      EXEC   PGM=ICKDSF
//STEPCAT     DD     DSNAME=ANOTHER.CATALOG,
//                   DISP=SHR
//SYSPRINT    DD     SYSOUT=A
//SYSIN       DD     *
  Device Support Facility commands (see examples on
  OLT 44).
/*
```

Job Control Language (JCL) Commands

The following steps are an explanation of the JCL commands:

1. //JOBNAME is required. The JOB statement describes the job to the OS/VS system. User identification, accounting, and authorization information may be required within the JOB statement parameters.
2. //JOBCAT is optional. The JOBCAT DD statement identifies a user catalog that can be used by each of the job steps. If the job uses only the master catalog, do not specify the JOBCAT DD statement because the master catalog is always open and available to all the jobs on the system.
3. //STEP1, an EXEC statement, is required. The EXEC statement invokes the Device Support Facility processor to process the device Support Facility commands.
4. //STEPCAT is optional. The STEPCAT DD statement identifies a user catalog that can be used when processing the job step. If user catalogs are identified with JOBCAT and STEPCAT DD statements, only the catalog identified with the STEPCAT DD statement and master catalog are used with the job step. If the job step uses only the master catalog, do not specify the STEPCAT DD statement because the master catalog is always open and available to all the jobs on the system.
5. //SYSPRINT is required. The SYSPRINT DD statement identifies the output data set that receives messages and output information from the Device Support Facility.

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ALTERNATE TRACK ASSIGNMENT ICKDSF/ICLDSF

ICLDSF (STAND-ALONE)

The stand-alone version of the Device Support Facility is equivalent to the system-supported version. Execution does not involve an operating system; there is no job control language (JCL). In place of the JCL, there are special techniques that will cause the program to execute, and that identifies the input and output streams. The IPL tape is a reproduction of the card deck (over 3000 cards).

The stand-alone version is invoked simply by loading the program into main storage (IPL the tape or card deck). When the program is fully loaded, it enters the wait state, displaying the following pattern in the program status word (PSW):

FF060000 00FFFFFF

The console, the command input stream, and the listing output stream (and optionally, the date and time-of-day) must now be identified.

OPERATOR CONSOLE DEVICE

The console is identified to the program simply by pressing the Request key.

COMMAND INPUT STREAM DEVICE (SYSIN)

The command input stream contains the command(s) that are executed by device support facility. The device types supported are:

- 2540
- 2520
- 3505
- 1052
- 1442
- 3210
- 2501
- 3215

Note that the Operator console may itself be specified as the command input device by entering the word CONSOLE in place of the above.

LISTING OUTPUT DEVICE (SYSPRINT)

The listing output device prints messages that occur during execution. The device types supported are:

- 1403
- 3800
- 3211
- 1052
- 3203-1, 2 or 4
- 3210
- 1443
- 3215

Note that the Operator's console may itself be specified as the Listing Output device by entering the word CONSOLE in place of the above.

DATE AND TIME-OF-DAY

Any string of eight or fewer characters may be entered, and will appear in the title line of the listing output pages. The ENTER key may be pressed without specifying a date or time-of-day, in which case the title line will contain blanks.

Device Support Facility Commands

See examples on OLT 44.

Intervention Required State

Should a device, such as the printer or card reader, require intervention (that is, to make it ready), message ICK012 will be issued and the PSW will display the following:

FF060000 00111111

Perform the necessary intervention actions, and the program will proceed.

Program Termination

The Device Support Facility program terminates upon encountering the end of the command input stream. The end of the command input stream is indicated by the characters EOF. Should the console be used as the command input device, these characters are entered in response to the request for the next command.

Upon normal program termination, the PSW is set to place the central processor into the wait state, and displays the following pattern:

00020000 00EEEEzz

The following zz values, in the rightmost byte of the PSW, indicate the highest condition-code encountered during execution:

- X'00' – Decimal 0
- X'04' – Decimal 4
- X'08' – Decimal 8
- X'0C' – Decimal 12
- X'10' – Decimal 16

When the program terminates, it may be started again by pressing the Request key. When started again, the requests for specification of the input and output devices, as well as the date and time-of-day, may be satisfied simply by pressing the Enter key, in which case the previously entered values for these parameters will be re-used.

ADDITIONAL CONDITIONS

To indicate the cause of certain types of terminating errors, the cause is set in the address field of the PSW and the central processor is then placed in a wait state. The PSW displays the pattern:

00020000 00EEEExx

The values of xx indicate:

- X'13' – SVC interrupt occurred
- X'14' – Program interrupt occurred
- X'15' – Main Storage depleted
- X'16' – I/O error detected
- X'17' – Data set not open
- X'18' – Write-to-operator issued, but no console exists
- X'19' – No end-of-data routine specified

Should the program terminate due to any of the above errors, it may be started again by pressing the Request key. When started again, the requests for specification of the input and output devices, as well as the date and time-of-day, may be satisfied simply by pressing the Enter key, in which case the previously entered values for these parameters will be re-used.

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ALTERNATE TRACK ASSIGNMENT ICKDSF/ICLDSF

Caution: The use of this program will destroy any existing data on the selected track. The customer should do the flagging when that action is required. The information provided here is to enable the CE to advise and assist the customer when necessary.

INSPECT AND INIT COMMAND PARAMETERS

After a volume has been initialized, it may be necessary to inspect the volume for defective tracks. Defective tracks can be detected and assigned alternate tracks, and tracks that have their defective-track flag on can be reclaimed.

The abbreviation for the Inspect command is INSP. The syntax of the Inspect command is:

Command	Required Parameters	Optional Parameters
INSPECT and INIT	UNIT ADDRESS (cuu) | DDNAME (dname) TRACKS(cylinder:track[,...]) | ALLTRACKS VERIFY(serial) NOVERIFY DEVICETYPE (devtype)	CHECK(n) | NOCHECK RECLAIM | NORECLAIM PRESERVE | NOPRESERVE* MAP | NOMAP ASSIGN | NOASSIGN* VALIDATE**

*INSPECT only
**INIT only

EXAMPLES OF DEVICE SUPPORT FACILITY COMMANDS

See Notes 1 through 3.

Example 1: Check the track surfaces and assign alternate tracks to defective tracks.

```
bbINSPECT bUNITADDRESS (CUU)b
NOVERIFYbDEVICETYPE (3350) b
ALLTRACKS bCHECK (n)
```

Example 2: Reclaim tracks that were previously flagged defective if after checking they are found to be good.

```
bbINSPECT bUNITADDRESS (CUU)b
NOVERIFYbDEVICETYPE (3550) b
ALLTRACKSbCHECK (n) b
RECLAIM
```

Example 3: Validate the Home Address and write record zero (R0).

```
bbINITbUNITADDRESS (CUU)b
NOVERIFYbDEVICETYPE (3550) b
ALLTRACKSbVALIDATE
```

Example 4: Assign alternate tracks unconditionally without checking track surfaces.

```
bbINSPECT bUNITADDRESS (CUU)b
NOVERIFYbDEVICETYPE (3550) b
TRACKS (Cyl: Track,
Cyl: Track, . . . . . , Cyl: Track) b
NOCHECK
```

UNITADDRESS: This is replaced by DDNAME if volume is online to the operating system.

CUU: This is the device address (for example: 250).

DEVICETYPE: Enter 3350 if volume is in native mode. Enter 3330 or 3330-11 if volume is in compatibility mode.

ALLTRACKS: Enter ALLTRACKS to check all tracks on a volume. Enter CYL: TRACK,. . . . . CYL: TRACK,. . . . . CYL: TRACK, (in Hex) to select specific tracks.

CHECK-NOCHECK: CHECK will check the specified tracks for recording errors and assign an alternative only if the track is found to be defective. For *n* substitute a decimal number from 1 to 225 for the number of times a track is to be checked. (This number is forced to a maximum of 10 if ALL TRACKS are specified).

NOCHECK will not check tracks for recording errors. Alternates will be assigned to the specified track(s).

VALIDATE: This specifies reading and validating the Home Address and Record Zero.

DEVICE SUPPORT FACILITY MESSAGES

ICK003D REPLY 'U' TO PURGE VOLUME cuu CONTENTS, ELSE 'T'

Operator Response: Respond U to proceed with command processing; respond T to terminate the command.

ICK004D READY OFFLINE DEVICE cuu AND REPLY 'U', ELSE 'T'

Operator Response: Ensure that the device is in the ready state, and respond U to continue processing the command or respond T to terminate the command.

ICK005E DEFINE INPUT DEVICE: 'INPUT=xxxx, cuu'

Explanation: This messages appears only in a stand-alone environment. The operator must specify the location of the command input stream or CONSOLE.

ICK006E DEFINE OUTPUT DEVICE: 'OUTPUT=xxxx, cuu'

Explanation: This message appears only in a stand-alone environment. The operator must specify the location of the device support facility output stream or CONSOLE.

ICK011E I/O ERROR – error type cuu, command, csw, sense

Explanation: This message appears only in a stand-alone environment. An I/O error of the type indicated occurred on the device at address cuu. The command in error is indicated as are the contents of the channel status word (CSW) and the results of a sense operation against the device.

ICK012E INTERVENTION REQUIRED, cuu

Operator Response: Ensure that the device is in a ready state.

Notes:

1. *The Device Support Facility commands must be entered within the margins of 2 and 72. If the length of the command exceeds space 72, a continuation mark (+ sign in 73) must be entered, and the command continued to the next line.*

   Values or variables can be specified with some keyword parameters. The value or variable is entered within parentheses following the keyword parameter. A typical keyword with a value is VOLID (serial).

2. *Delimiters – When a Device Support Facility command is issued, the command name must be separated from the first parameter by one or more blanks. Separate parameters from each other by one or more blanks or a comma. Do not use a semicolon as a delimiter; any characters that follow a semicolon are ignored.*

3. *Line Continuations – To continue a command to the next line, specify a plus or a minus sign as the last character of the current line. When a plus sign (+) is used, leading delimiters are removed from the continued line.*

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Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350X	CECOM 038	INT REQ, R TO RETRY, T TO TERM	After replying, the Start I/O is retried or the OLT is terminated.	1. Determine the cause of Intervention Required Status, then reply. 2. Ensure that the drive is ready.
T3350X	CECOM 039	CC = X, R TO RETRY, T TO TERM	This message is sent to the console to warn of catastrophic failure (condition code = 2 or 3). Usually when the storage control is busy or not operational, further testing is invalid. Determine if the controller is "hung" before continuing. If so, a Halt I/O failed to clear the condition. After replying, the Start I/O is retried or the OLT is terminated.	1. Determine if the subsystem is "hung" before continuing. See if the storage control is in the normal idle loop. If normal, enter desired reply; if not, go to START 100. 2. Ensure that all cables and connectors are secure. 3. Ensure that the drive is ready. 4. Ensure that the interface is online.
T3350X	CECOM 041	DEV NOT 3350	CDS type code for the device under test is not '0B' (3350), '09' (3330-1), or '0D' (3330-11).	Correct the CDS type code for the device to be tested or equate (by entering 'EQU') the device address to some existing CDS with the desired type code.

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Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350X	XX090	FPM MODE	File Protect mode was established. This section needs write space so it is not allowed to run.	1. Reply YES (Y) to the OLT message CAN VOL DATA ON XXX BE DESTROYED. 2. Then select the CE track (cylinder 1024, heads 0 through 29) to prevent destruction of valuable data.
Note:	*Nine (9) standard error numbers (REFNUM) have been reserved for errors encountered by the Start I/O used by OLT sections. These error numbers are XX091 through XX099, where XX is the routine number.*			
T3350X	XX091	ENVIRONMENTAL ERROR	An error occurred on a test CCW chain that established Error Logging mode or storage control was in Force Logging mode.	If a log overflow occurred, ignore the following actions. 1. If the storage control is in Normal mode and this message appears intermittently, set the storage control to CE Normal mode. 2. If the storage control is in CE Normal mode and the error looks solid, analyze errors as shown in Common Action B (OLT 28).
T3350X	XX092	CHANNEL CHECK	This error message is printed by the STARTIO subroutine when channel checks are found in the CSW status. The test is terminated when channel checks are found.	Channel checks are probably not due to subsystem failure. Run CPU channel tests.
T3350X	XX093	WAIT TIMED OUT	This error message is printed by the STARTIO subroutine when the test has timed-out while waiting for ending status. The test is terminated when it times-out.	Ending status was not received from the CCW chain printed with this message. The subsystem may have become Busy or not operational, which invalidates further testing. Look for messages to this effect following REFNUM 93. If the control unit is "hung", the storage control must be reset before continuing the test.
T3350X	XX094	ERR ON SENSE	This error message is printed by the STARTIO subroutine. When the sense data is not posted, another STARTIO is tried.	1. If this failure persists 32 times (see REFNUM XX095), continue running tests to determine if Sense I/O failure is intermittent or solid. 2. Run storage control tests. 3. Run CPU channel test for Sense I/O.
T3350X	XX095	32 RETRIES	This message is printed before terminating a section if either CU Busy or Invalid Sense was received on STARTIO and retried 32 times. See example on OLT 60.	1. Continue running tests to determine if Sense I/O failure is confined to this OLT. 2. Run storage control tests. 3. Run CPU channel test for Sense I/O.

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<table>
<tr><th>Sect ID</th><th>REFNUM</th><th>Error Messages and Console Communications</th><th>Diagnostic Information</th><th>CE Action</th></tr>
<tr><td>Example:</td><td></td><td>
<pre>
*T3350PSA-24 RTN 001   DEV/LN 02E1   ECA 0   REFNUM 00003
  HDA HA/R0 SCAN
 CCW01 1F 01796A 40 00 0001   CAW 00017918
 CCW02 07 01796C 40 00 0006
*CCW03 1A 017981 40 00 0005
 CCW04 16 017986 80 00 0010
 CCW05 16 017938 30 00 2328
 XPTD CC 0   RCVD CC 0
 XPTD CSW1 00 017940 0C00 0000
*RCVD CSW1 00 017930 0E40 0005
*RCVD SNS   08 00 82 00 40 00 21 44 01 00 00 00 00 00 00 00 00
            00 00 00 00 00 49 44
 I/O ERRS READING HA/R0
</pre>
</td><td>This is an example of the error message output whenever a status error occurs. This message includes:

Symbol — Meaning
* — Error message
T3350PSA — OLT section identification
V/L 24 — OLT version and level
RTN001 — Routine number in OLT
DEV/LN — Device address against which OLT was run
REFNUM — Index into error dictionary (OLT section)
* on CCW03 — Failing CCW
* on RCVD CSW — Failing status
* on RCVD SNS — Failing sense data</td><td>1. Locate the REFNUM in the OLTs section (starting on OLT 200) and follow the Diagnostic Information and CE Action.
2. Go to Common Action B (OLT 29).</td></tr>
<tr><td>T3350X</td><td>XX099</td><td>ABTERM, RET CODE - XX RCVD FROM YYYYYYYY

<table>
<tr><th>Module (YYYYYYYYY)</th><th>Return Code (XX)</th><th>Termination Reason</th><th>Termination Code</th></tr>
<tr><td>ALLOCATE</td><td>04</td><td>Module not available</td><td>D</td></tr>
<tr><td></td><td>08</td><td>Device not in device entry list</td><td></td></tr>
<tr><td></td><td>10</td><td>Space not available</td><td>D</td></tr>
<tr><td>CECOM</td><td>04</td><td>Module not available</td><td>C,D</td></tr>
<tr><td></td><td>08</td><td>Error executing module</td><td>C,D</td></tr>
<tr><td>CONVERT</td><td>04</td><td>Module is not available</td><td>D</td></tr>
<tr><td></td><td>08</td><td>Error from EH conversion</td><td>O,D</td></tr>
<tr><td>DPRINT</td><td>04</td><td>Module not available</td><td>D</td></tr>
<tr><td></td><td>08</td><td>Error while printing line of data</td><td>H</td></tr>
<tr><td></td><td>0C</td><td>Incomplete parameter list</td><td>O</td></tr>
<tr><td>EXIO</td><td>04</td><td>Module not available</td><td>D</td></tr>
<tr><td></td><td>08</td><td>Device not available</td><td>C,D,T</td></tr>
<tr><td></td><td></td><td>Device not primary or data protected</td><td>O,D</td></tr>
<tr><td></td><td></td><td>Device busy</td><td>T</td></tr>
<tr><td></td><td>0C</td><td>File protect violate. Respond with YES to CAN VOL DATA BE DESTROYED</td><td>U</td></tr>
<tr><td>GRAB</td><td>04</td><td>Device not in device entry list</td><td>U</td></tr>
<tr><td></td><td>08</td><td>Entry list contains only one device</td><td>U</td></tr>
<tr><td></td><td>0C</td><td>Device descriptors not available</td><td>C</td></tr>
<tr><td>PLINK</td><td>04</td><td>Module not available</td><td>D</td></tr>
<tr><td>WAITIO</td><td>04</td><td>Module not available</td><td>D</td></tr>
<tr><td></td><td>08</td><td>Timed out</td><td>T</td></tr>
<tr><td></td><td>0C</td><td>Error - Device not valid</td><td>O,C</td></tr>
</table>
</td><td>The OLT(S)EP module name YYYYYYYY returned to the OLT in use with an error (return code = 'XX', should be = '00').

Meaning of Termination Code
Termination Code — Termination may be due to:
O — The OLT
D — The OLT(S)EP driver
T — Device under test, including channel and/or storage control
C — Configuration Data Set not correct
H — Hardware in use, including console printer
U — User error</td><td>1. Usually due to a failure in OLT(S)EP (unless EXIO or WAITIO is involved). Restart OLTEP or re-IPL OLTSEP.
2. Check the Configuration Data Set (CDS) to make sure that it is correct for the system. Use SOSP LIST function or DISPLAY to obtain configuration data.
3. Module not available (return code '04') from any request for a module means that:
a. OLT and OLT(S)EP are not at compatible levels. This is not an error, but probably a down-level OLT(S)EP.
b. Module has been removed from OLT Library.
c. Device may be shared. This is not an error.</td></tr>
</table>

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HDA HA/R0 SCAN

Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350PSA	CECOM 033	ENTER TRACK(S) FOR HA/R0 CHECK, 'ALL' OR 'END' AS CCCHH OR CCCHH-CCCHH (IN HEX)	Valid track entries are as follows: 3350 = '00000' (cylinder 0, head 0) through '22F1D' (cylinder 559, head 29) 3330-1= '00000' through '19412' (cylinder 404, head 18) 3330-11= '00000' through '32812' (cylinder 808, head 18)	Example: Enter one track ('00501', CYLINDER 5, HEAD 1) or some portion of the HDA ('00501' – '01008', CYLINDER 5, HEAD 1 through CYLINDER 16, HEAD 8) to be scanned. At the conclusion of scanning the last track selected, a statistical summary is printed and routine 2 is re-entered to allow selection of some other tracks or End. Default (EOB) is to check the entire logical volume.
T3350PSA	CECOM 034	ENTER R0 DATA LENGTH AS '8', or 'ANY'		Enter R0 data length to be scanned; eight bytes if a standard OS/VS HDA is mounted, and any number of bytes if no data length test is required. The test defaults (EOB) to an 8-byte data length scan.

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HDA HA/R0 SCAN

Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350PSA	00001	VOL ID ON XXXX IS YYYYYYYYYY	This message is printed if the HDA under test is labeled, where XXXX is the drive address. If no label record (cyl 0, hd 0, R3) exists or it cannot be read, YYYYYYYYYY reads -NONE-. This message is preceded by error REFNUM 00002 if some hardware error other than No Record Found terminates the operation. The HDA scan continues.	This is a normal message unless preceded by error REFNUM 00002.
T3350PSA	00002	I/O ERR READING VOL ID	This message warns of some hardware failure other than No Record Found while trying to read track 0, data Record 3. The HDA scan continues.	1. If the error is a Data Check and the drive has already been tested error free using microdiagnostics, the problem is with the volume label. The operator must use the appropriate utility to restore the label. See OLT 30 for utility descriptions. 2. If the error is not a Data Check, use the printed status and sense data, then go to Common Action B (OLT 29).
T3350PSA	00003	I/O ERR READING HA/R0 CCW01 1F 01781E 40 00 0001 CAW 000177D0 CCW02 07 017820 40 00 0006 CCW03 1A 017835 40 00 0005 *CCW04 16 01783A 80 00 0010 CCW05 16 0177F0 30 00 2328 XPTD CC 0 RCVD CC 0 XPTD CSW1 00 0177F8 0C00 0000 *RCVD CSW1 00 0177F0 0E40 0008 *RCVD SNS 08 00 00 00 40 22 19 41 00 22 00 19 00 00 00 00 00 00 00 00 00 00 49 41 CCC HHRR KL DL |..SNS 0-6...| FM |.....SNS 8-23.....| 0022001900 00 0008 08000000402219 41 00220019000000000000000000004941	This message warns of some error while trying to read HA and/or R0. The HDA scan continues. *This message may be followed by REFNUM 00007, which identifies an incorrect HA and/or R0 Read.*	1. If the error is followed by REFNUM 00007 or 00009, see action for that REFNUM. 2. If the error is not followed by REFNUM 00007 or 00009, use the status and sense data printed with REFNUM 00003, then go to Common Action B (OLT 29).
T3350PSA	00007	-HA AND/OR R0 COMPARE ERROR FOUND ....CYL#=0057 HD#=0F (HEX).... HOME ADDR- R0 COUNT-------- R0 DATA------- EXPD=040057000F 0057000F00000008 XXXXXXXXXXXXXXX RCVD=000017000F 0194000100000008 000000000000000	This message warns of HAs and/or R0s that are not as expected. XX---XX in EXPD field(s) indicates data insignificant. XX---XX in any RCVD field indicates significant data was not read into appropriate buffer (incomplete operation).	1. If the error was preceded by REFNUM 00003 and the error was not a Data Check or No Record Found, go to Common Action B (OLT 29). 2. HA miscompare may be due to volume format and drive mode jumpering which do not agree. Compare EXPD and RCVD HA to identify this condition, example: EXPD=0000000014 and RCVD =0000010000 shows EXPD native MODE jumper and RCVD compat FORMAT. If drive mode (jumper) is correct go to 3. 3. Verify that all microdiagnostics run error free on this drive. If there are no microdiagnostic errors, run OLT T3350WT on the CE track with the failing head selected. 4. If T3350WT runs error free, the problem is with the HA or R0 on this track. Restore the track with the appropriate utility. See OLT 30 for utility descriptions. **Caution: Restoring the HA and R0 destroys the remaining data on the track.**
T3350PSA	00008	DEF TRK FOUND WITH INCORRECT -ALT-MATE ASSIGNED HOME ADDR- R0 COUNT------- R0 DATA-------- DEF= 0201090001 010E0001 MATE= 01010E0001 010E0001 ....CYL= 0109 HD= 01 (HEX).... 3350 HDA HA/R0 SCAN HOME ADDR- R0 COUNT-------- R0 DATA-------- EPXD=0001090001 0109000100000008 XXXXXXXXXXXXXXXX RCVD=0201090001 010E0001FA000008 01090001FAFFFFFF	This message warns of defective or alternate flagged tracks that point to mate tracks that are not correctly flagged, or if flagged, R0 does not point back to the ALT/DEF track (invalid assignment). Alternate tracks with incorrect mates do not have to be corrected.	If the track is defective, the operator must use the appropriate utility to restore the track. See OLT 30 for utility descriptions.

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T3350PSA ERROR MESSAGES

HDA HA/R0 SCAN

Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350PSA	00009	DATA CHECK ON HA OR R0	This message is printed immediately to warn of a Data Check on the record indicated (see the failing CCW in REFNUM 00003, marked with an *, to determine the failing command). The sense data is reproduced in its entirety to allow absolute identification of the data error. See SENSE 100 for a Sense Byte breakdown. The most significant byte is Sense Byte 7, identified by FM in the message. Sense Byte 7 Description: **Format / Msg / Field / Meaning** 4 / 0 / HA / ECC Data Check 4 / 1 / Count / ECC Data Check 4 / 2 / Key / ECC Data Check 4 / 3 / Data / ECC Data Check 4 / 4 / HA / No Sync Byte Found 4 / 5 / Count / No Sync Byte Found 4 / 6 / Key / No Sync Byte Found 4 / 7 / Data / No Sync Byte Found 5 / 3 / Data / Data Check *Format 4 Uncorrectable Data Checks are caused by a failure while reading data and should be considered as HDA failures or hardware failures in the tested drive. Format 5 Correctable Data Checks are handled by system recovery procedures.*	The CE action to be taken when a Data Check is discovered depends upon the analysis of the 3350 HDA HA/R0 Scan Error Statistics Table (REFNUM 0000B) and this detailed error message. Consistent Data Checks may indicate a defective head or drive read problems. Run OLT T3350WT and select the suspected heads on the CE cylinder (X400HH). Run read/write microdiagnostics to verify that the drive and HDA are OK. If the drive has already been checked, the error is related to the HDA. The HDA may be corrected by the operator by using the appropriate utility. See OLT 30 for utility descriptions. Go to Common Action C (OLT 29).
T3350PSA	0000A	I/O ERRS READING HA/R0 ....CYL#=XXXX HD#=XX(HEX).... (EXCESSIVE HDWR ERRS ON CURRENT CYL, TEST TERMINATED)	This message is printed immediately to warn that some error other than a Data Check occurred in the chain displayed. Data integrity information for the record indicated is lost. If this was the 30th error on this cylinder, the message including TEST TERMINATED is added to the message, a statistical summary is printed, and the OLT terminates.	Use the printed status and sense data in REFNUM 00003, then proceed to Common Action B (OLT 29).

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HDA HA/R0 SCAN

Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350PSA	0000B	3350 HDA HA/R0 SCAN ERROR STATISTICS TABLE *** VOL ID ON 0160 IS .... -NONE-*** HD# -------ERR TYPE# (SENSE BYTE 07)-------- (HEX) 40 41 (42----49, 50------52) 53 XX TOTAL 00 000 000 ---------- 000 000 0000 01 000 000 ---------- 000 001 0001 SUMMARY INFORMATION FOR HEADS 2-28 WILL BE INCLUDED HERE 1D 000 000 ---------- 000 001 0001 TOTALS 00000000 ---------- 0000 0002 0002	This message follows abnormal termination or cancellation of the OLT. It also follows testing of the selected portions of the HDA, but the error statistics may not represent the condition of the entire HDA. ERR TYPES 40 through 53 are derived from the sense data provided on Data Checks. ERR TYPE XX includes all non-Data Check errors (hardware failures). Totals by head number (HD #) and by ERR TYPE number are shown, as well as an overall total. *The maximum value for any individual ERR TYPE #/HD# error counter is 255. If any additional errors occur, the error counter is locked at 255 until the error message is printed. A count of 255 may represent more than 255 errors.* If the drive (volume) being scanned has fixed heads, the actual cylinders that failed determine whether the failing heads are movable or fixed. See the detailed message corresponding to this error and see REFNUMs 00003, 00007, or 0000A for identification of logical cylinder and head numbers. Then convert the logical cylinder and head numbers to physical fixed head numbers by using the following charts: **3350 Logical Cylinder** / **Heads** / **Physical Fixed Heads** 1 — 0 – 29 — 0 – 29 2 — 0 – 29 — 30 – 59 **3330-1, 3330-11 Logical Cylinders (Primary Address)** / **Heads** / **Physical Fixed Heads** 1 — 0 – 18 — 0 – 18 2 — 0 – 18 — 19 – 37 3 — 0 – 18 — 38 – 56	This output should be analyzed to determine if data errors or hardware failures follow any pattern. Many errors on one head, for instance, may indicate a defective head. Refer to the detailed error messages (REFNUM 00009) for more specific information on tracks/records in error. Follow the CE Action under REFNUM 00009.
T3350PSA	0000C	DEFECTIVE/ALTERNATE TRACK SUMMARY CYL HD /CYL HD (HEX) 002B 05 /022B 00 002F 01 /022B 01 003C 01 /022B 02 0044 03 /022B 03 0059 01 /022B 04 005C 19 /-NO MATE 007E 00 /022B 05	This message follows the ERROR STATISTICS TABLE above. Defective and alternate tracks are summarized with NO MATE appearing beside those tracks flagged but not pointing to a valid or readable mate. Detailed information for these faulty ALT/DEF tracks is printed immediately and is found preceding this message (see REFNUM 00008). All tracks in the alternate area are flagged and point to themselves until assigned to a defective track. These are not summarized here.	No action is necessary unless DEFECTIVE tracks with the NO MATE message appear. Then, the operator must use the appropriate utility to restore the HDA. See OLT 30 for utility descriptions.

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T3350 PSB ERROR MESSAGES

HDA BURST CHECK

Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350PSB	CECOM 033	ENTER TRACKS(S) FOR DATA CHECK 'ALL' or 'END' as CCCHH OR CCCHH-CCCHH (IN HEX)	Entering this track select mode of testing (routine 2) causes the OLT to go into a record-at-a-time test mode where selection of routine 1 (default) allows the faster cylinder-at-a-time mode. Do not use this routine 2 mode to check all tracks. Valid track entries are as follows: 3350 = '00000' (cylinder 0, head 0) through '22F1D' (cylinder 559, head 29) 3330-1= '00000' through '19412' (cylinder 404, head 18) 3330-11= '00000' through '32812' (cylinder 808, head 18)	Enter one track or some portion of the HDA to be checked. At the conclusion of the burst check of the last track selected, a statistical summary is printed and routine 2 is re-entered to allow selection of some other track(s) or End. Default (EOB) is to check all tracks.
T3350PSB	CECOM 035	ENTER TRACK TO LOOP AS CCCHH IN HEX		Enter one track address (in hex) to be burst checked in a tight loop. Default (EOB) is to cylinder 0, head 0.

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HDA BURST CHECK

Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350PSB	00001	VOL ID ON XXXX IS YYYYYYYYYY	This message is printed if the HDA under test is labeled and XXXX is the drive address. If no label record (cyl 0,hd 0,R3) exists or it cannot be read, YYYYYYYYYY is -NONE-. This message is preceded by error REFNUM 00002 if some hardware error other than No Record Found terminates the operation. The HDA scan continues.	This is a normal message unless preceded by error REFNUM 00002.
T3350PSB	00002	-I/O ERR READING VOLID	This message warns of some hardware failure other than No Record Found while trying to read track 0, data Record 3. The HDA scan continues.	1. If the error is a Data Check and the drive has already been tested error free using microdiagnostics, the problem is with the volume label. The operator must use the appropriate utility to restore the label. See OLT 30 for utility descriptions. 2. If the error is not a Data Check, use the printed status and sense data, then go to Common Action B (OLT 29).
T3350PSB	00004	SEARCH FAILED ON REC# XX ...CYL#=XXXX,HD#=XX(HEX)	This message indicates the search for record number XX failed after a prior read of record number XX was completed successfully. The test continues on next record.	1. If this failure first occurred on REC #00, then the R0 on this track is missing. Run OLT T3350PSA on this track. For any other REC #, see Steps 2 and 3. 2. If the storage control is not in Normal mode, this is printed as a result of reading/searching any Count field with an intermittent uncorrectable error. In other than Normal mode, testing moves to the next track and leaves the remainder of this track untested. 3. If the storage control is in Normal mode, the problem is an intermittent read error. Follow the CE Action for REFNUM 00009.
T3350PSB	00006	UNCORRECTABLE DATA CHECK IN HA FIELD SKIP BURST CHECK ON THIS TRACK ....CYL#=XXXX, HD#=XX (HEX)	This message indicates the HA or CNT field on this track contains an uncorrectable Data Check, preventing burst check on subsequent records on this track. This message is followed by REFNUM 00009. Test continues on next track.	1. If the message reads HA FIELD, run T3350PSA on this track. 2. If the message reads CNT FIELD, do one of the following: a. Backup this track and then test it using OLT T3350WT. Use IEHATLAS to save the track. b. Have the customer perform the appropriate data recovery action for this track, record, data set, or volume.

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HDA BURST CHECK

Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350PSB	00009	DATA CHECK ON REC# 01 (HEX) CCC HHRR KL DL |..SNS 0-6...| FM |.....SNS 8-23.....! 0002000301 1811C4 08000000400203 43 00020003010200000000000000004943	This message is printed immediately to warn of a Data Check on the record indicated. The sense data is reproduced in its entirety to allow absolute identification of the data error. See SENSE 100 for a Sense Byte breakdown. The most significant byte is Sense Byte 7, identified by FM in the message at the left. Sense Byte 7 Description: **Format / Msg / Field / Meaning** 4 / 0 / HA / ECC Data Check 4 / 1 / Count / ECC Data Check 4 / 2 / Key / ECC Data Check 4 / 3 / Data / ECC Data Check 4 / 4 / HA / No Sync Byte Found 4 / 5 / Count / No Sync Byte Found 4 / 6 / Key / No Sync Byte Found 4 / 7 / Data / No Sync Byte Found 5 / 3 / Data / Data Check *Format 4 Uncorrectable Data Checks are caused by a failure while reading data and should be considered as HDA failures or hardware failures in the tested drive. Format 5 Correctable Data Checks are handled by system recovery procedures.*	The CE action to be taken when a Data Check is discovered depends upon the analysis of the 3350 HDA Burst Test Error Statistics Table (REFNUM 0000B) and this detailed error message. Consistent Data Checks may indicate a defective head or drive read problem. Run T3350WT (using a CE track) or run read/write microdiagnostics to verify that this drive and HDA are OK. If the drive has already been checked, the error may be related to the HDA. The HDA can be tested using T3350WT (see OLT 26 for description) or Device Support Facility (DSF) see OLT 30 for description. Write/read failures on a single track indicate that it should be flagged as defective. The HDA must be corrected by the operator using the appropriate utility. See OLT 30 for utility descriptions.
T3350PSB	0000A	I/O ERRS READING REC# XX (HEX) ....CYL#=XXXX HD#=XX (HEX).... (EXCESSIVE HDWR ERRS ON CURRENT CYL, TEST TERMINATED)	This message is printed immediately to warn that some error other than a Data Check occurred in the chain displayed. Data integrity information for the record indicated is lost. If this was the 30th error on this cylinder, the message including TEST TERMINATED is added to the message, a statistical summary is printed, and the OLT terminates.	Use the printed status and sense data, then go to Common Action B (OLT 29).
T3350PSB	0000B	3350 HDA BURST TEST *** VOL ID ON 0160 IS .... -NONE- *** HD# -------ERR TYPE# (SENSE BYTE 07)-------- (HEX 40 41 42----49, 50------52) 53 XX TOTAL 00 000 000 ---------- 000 000 0000 01 000 000 ---------- 000 001 0001 SUMMARY INFORMATION FOR HEADS 2-29 (HEX) WILL BE INCLUDED HERE 1D 000 000 ---------- 000 001 0001 TOTALS 00000000 ---------- 0000 0002 0002	This message is printed following testing on the portion of the HDA selected, following abnormal termination, or following cancellation of the OLT. ERR TYPES 40 through 53 are derived from the sense data provided on Data Checks. ERR TYPE XX is a catchall type to include all non-Data Check errors (hardware failures). Totals by head number (HD#) and by ERR TYPE number are shown as well as an overall total. *The maximum value for any individual ERR TYPE #/HD# error counter is 255. If any additional errors occur, the error counter is locked at 255 until the error message is printed. A count of 255 may represent more than 255 errors.* For fixed heads, see the Diagnostic Information under T3350 PSA, Refnum 0000B.	This output should be analyzed to determine if data errors or hardware failures follow any pattern. Many errors on one head for instance, may indicate a defective head. Refer to the detailed error messages (REFNUM 00009) for more specific information on tracks/records in error. Follow the CE Action under REFNUM 00009.
T3350PSB	0000D	RECORD XX COUNT FIELD NOT 8 BYTES ....CYL#=XXXX HD#=XX(HEX)	This message warns of some record, XX, which does not have an 8-byte Count field.	The operator must use the appropriate utility to restore the track. See OLT 30 for utility descriptions.

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SKIP DISPLACEMENT DIRECTORY

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350 PSC	CECOM 520	DEVICE IS NOT PLUGGED NATIVE 3350, FIX PLUG AND RERUN ROUTINE.	The drive under test is not plugged in native mode. The OLT terminates.	Plug native and rerun the OLT, see Figure 1 on HDA 711 for plugging. After running routines M2 or M3 reinitialization will be required to restore compatibility format. After running routine M1 the track(s) selected by M1 must be reinitialized
T3350 PSC	CECOM 521	SD DIRECTORY MICRO CHANGE IS NOT INSTALLED.	The functional microcode in the control unit will not allow seeks to cylinder 561. OLT terminates.	Re-IMPL control unit with functional microcode disk P/N 4168811 at EC 437465 with REA 13-57853 or later.
T3350 PSC	CECOM 522	ROUTINE TERMINATED	The OLT has abnormally terminated.	Correct errors indicated by other CECOMs and rerun the OLT.
T3350 PSC	CECOM 523	VOL ID ON xxxx IS yyyyyyyyyy	The volume ID on device XXXX is YYYYYYYYYY. If the volume has no ID, ... - none - will appear in the second field.	Normal message
T3350 PSC	CECOM 524	DIRECTORY RECORD ALREADY EXIST, DO YOU WISH TO OVERLAY? REPLY 'Y' TO CONTINUE, 'T' TO TERMINATE	At least a partial directory was found on cylinder 561.	Normally a 'T' reply should be entered. A reply of 'Y' will direct the OLT to discard this old directory and continue building a new one in its place. A reply of 'T' will direct the OLT to retain the existing directory.
T3350 PSC	CECOM 525	RHA FAILED ON CCCCHHHH, CANNOT DETERMINE SD. REPLY 'R' TO RETRY, 'T' TO TERMINATE, 'I' TO IGNORE.	A Read Home Address (RHA) sense CCW chain failed to execute properly on track ccchhhh.	'R' will retry the chain; 'T' will terminate the OLT; 'I' will cause the OLT to assume a zero SD for the track in question and continue scanning. Use Sense Data to determine the type of error. If Data Check reply 'I', if other error reply 'T' and go to Common Action B (OLT 29).
T3350 PSC	CECOM 526	DIRECTORY BUILD ROUTINE IS COMPLETE.	This message is output to indicate that routine Build SD Directory has come to normal completion and that an SD directory now exists on cylinder 561 of the tested volume.	Normal message
T3350 PSC	CECOM 527	UNRECOVERABLE ERRORS HAVE OCCURRED DURING THE DIRECTORY BUILD.	The OLT has terminated for some reason (perhaps a 'T' response was given to a CECOM with a terminate option) and is unable to successfully do cleanup operations on the existing SD directory due to I/O errors. The OLT will terminate.	Check the hardcopy output for failing CCW and sense. Correct the problem and rerun the routine. Do not attempt to restore the HDA from this erroneous directory. Go to Common Action B, OLT 29.
T3350 PSC	CECOM 528	DIRECTORY BUILD IS INCOMPLETE	The OLT has terminated for some reason (perhaps a 'T' response was given to a CECOM with a terminate option) and the OLT has marked the SD directory as incomplete. This message will occur if there is not enough room on cylinder 561 for the entire directory to be written. This condition should never occur. Cylinder 561 should accommodate all anticipated SD information. The directory is still usable, however some non-zero SD data may not be recorded in it.	Use microdiagnostic routine B1 to ensure that all available tracks on cylinder 561 are useable (not flagged defective) then rerun OLT. If this message persists the directory should be used only for recovery of selected track(s) (routine M1) to limit rewriting HAs with inaccurate SD data.
T3350 PSC	CECOM 529	FPM MODE -- RTN TERMINATED	The volume is in file protect mode (FPM) and could not be allocated to this routine. The OLT terminates.	Vary the volume offline. Restart OLT and reply Yes to "Can data be destroyed" message. If running in default mode (Build SD directory), writing will occur only on CE cylinder 561.

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SKIP DISPLACEMENT DIRECTORY

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350 PSC	CECOM 530	ERROR TRYING TO READ THE VOLID. REPLY 'C' TO CONTINUE, 'T' TO TERMINATE.	The OLT could not read the volume ID.	Go to common action B, OLT 29. 'C' will continue with the routine selected, 'T' will terminate the OLT.
T3350 PSC	CECOM 532	NO DIRECTORY RECORDS HAVE BEEN WRITTEN.	This message is output to inform the user that routine Build SD Directory has not written any directory on cylinder 561. Preceding CECOM messages should indicate conditions which brought this about. The OLT terminates.	Respond to preceding CECOM messages.
T3350 PSC	CECOM 534	CARD SEQ NUMBER xxx CONTAINS NONSEQUENTIAL CCH.	A cch (cylinder/head) entry on the SDMAP card* (number = xxx) in question was not higher than the last cch entry recognized by the OLT. The OLT terminates.	Correct the card* in question and rerun the OLT.
T3350 PSC	CECOM 540	CARD SEQ NUMBER xxx CONTAINS NONHEX DATA.	The OLT terminates.	Correct the SDMAP card* (number = xxx) in question and rerun the OLT.
T3350 PSC	CECOM 541	CARD SEQ NUMBER xxx DOES NOT HAVE SDMAP IN COLS 1-5.	An SD data card did not have SDMAP in card* (number = xxx) cols 1-5. OLT terminates.	Correct the card in question and rerun the OLT.
T3350 PSC	CECOM 542	CARD SEQ NUMBER xxx IS OUT OF SEQ.	An SDMAP card* (number = xxx) was out of sequence or a sequence number was skipped. The OLT terminates.	Resequence the deck, inserting blank SDMAP cards* to complete the sequence. Check to be sure no SDMAP cards are missing. Rerun the OLT.
T3350 PSC	CECOM 544	NO CARD WITH SEQ NUMBER 001 FOUND.	The first SDMAP card* in the deck must contain a sequence number of 001. This check is necessary to insure that the OLT can identify the HDA to which the SD data deck belongs. The OLT terminates.	Correct the SDMAP deck* and rerun the OLT.
T3350 PSC	CECOM 545	EOF OCCURRED WITHOUT FINDING 'FE' IN INPUT.	While reading SDMAP cards*, an EOF occurred before the end of data marker 'FE'* was encountered. The OLT terminates.	Check the deck for missing cards*, rerun the OLT.
T3350 PSC	CECOM 546	PERM ERROR OCCURRED WHILE READING CARDS.	An uncorrectable I/O error occurred while reading the SDMAP card* deck. The OLT terminates.	Check for invalidly punched cards. Correct the error and rerun the OLT.
T3350 PSC	CECOM 547	xxxxxxxxxxxxxxxx = HDA SERIAL #. PROCEED Y/N.	The OLT has SD data ready for HDA with serial number xxxxxxxxxxx.	Check to be sure the HDA with this serial number is mounted at the device address specified at device/test/option time. If the correct HDA is under test, respond 'Y'. If not, respond 'N' to terminate the OLT; mount the correct HDA, or specify the proper device address, and rerun the OLT.

*SDMAP CARD DECK CONTAINS THE SKIP DISPLACEMENT information. See OLT users guide (Order number D99-3350) for detailed information.

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T3350 PSC ERROR MESSAGES

SKIP DISPLACEMENT DIRECTORY

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350 PSC	CECOM 554	HA/R0 HAS BEEN ALTERED AS REQUESTED.	This message is informational and will follow successful. completion of CECOM 564.	Normal
T3350 PSC	CECOM 555	cchh ENTRY IS INVALID; HA HAS NOT BEEN ALTERED	The cchh entry in response to CECOM 564 was invalid for the type of HDA under test. This message is always followed by CECOM 564.	Check ccchh entry to be sure it is not too large. Check for illegal characters.
T3350 PSC	CECOM 558	CANNOT READ SD DIRECTORY.	A record in the SD directory cannot be read because of a permanent I/O error or because the record is invalid. If encountered while running routines M1 or M2, this message is followed by message CECOM 570. If encountered while running routine M3, the OLT terminates.	Go to Common Action B, OLT 29 and determine cause of error. If no error is found the record is invalid and the SD information must be entered manually using routine M1.
T3350 PSC	CECOM 559	ALL TRACKS BEYOND END OF THE DIRECTORY WILL HAVE SD=0	This message is output with CECOM 568 to indicate that only a partial SD directory has been found and if directed to continue, the OLT will use SD=0 for all tracks beyond the end of the directory.	Informational message
T3350 PSC	CECOM 560	WARNING - ALL DATA ON THE TRACKS WRITTEN WILL BE DESTROYED.	This message is output each time the OLT is run.	If the tracks having HAs rewritten contain valuable data, respond 'T' to the CECOM 562 that follows. If the data can be destroyed, reply 'GO',
T3350 PSC	CECOM 561	DRIVE MUST HAVE BEEN RUNNING FOR TWO MINUTES BEFORE CONTINUING.	This message is output as an alert that if the drive has recently been turned off, it must be allowed to warm up.	Do not respond 'GO' to the CECOM 562 that follows until the specified warm-up time or 5 five minutes has been exceeded.
T3350 PSC	CECOM 562	DUMP ALL VALUABLE DATA BEFORE CONTINUING. ENTER 'T' TO TERMINATE OR 'GO' TO CONTINUE.	This message is output as a reminder to backup all valuable data on any track that will have the HA & R0 rewritten.	If valuable data resides on those tracks that will be rewritten, respond 'T'. If the data can be destroyed, respond 'GO'.
T3350 PSC	CECOM 563	SD DIRECTORY DOES NOT EXIST ON THE HDA. ENTER 'T' TO TERMINATE, 'GO' TO CONTINUE.	This message is output if the OLT cannot find an SD directory on cylinder 561 of the HDA under test.	If SD data is to be input from the console, respond 'GO'.
T3350 PSC	CECOM 564	ENTER TRACK TO WRITE HA AS CCCHH (DEC) OR XCCCHH (HEX).		Enter the track number that is to have HA & R0 rewritten by routine M1.

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SKIP DISPLACEMENT DIRECTORY

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350 PSC	CECOM 565	EOB RESPONSES WILL SET SD DATA TO ZERO. ENTER SDN IN HEX AS 'XXXX' CR EOB FOR CYI TRK - CCCHH.	This message is output to elicit SD data from the console for track ccchh. The *n* indicates the SD field for which data is requested.	If the SD field is to be zero, respond with End of Block. If SD field is to be nonzero, enter the value.
T3350 PSC	CECOM 566	I/O ERROR READING HA/RO - CCCHH. ENTER 'R' TO RETRY OR 'T' TO TERMINATE.	An I/O error other than a data check occurred while reading HA/R0 (or writing if 'WRITING' is specified) on track ccchh.	Check hardcopy output for failing CCW and sense information. Respond 'T' to terminate or 'R' to retry the chain. If error persists go to common action B, OLT 29.
T3350 PSC	CECOM 567	NO SD DIRECTORY ON HDA - CARD RESTORE? ENTER 'Y', YES OR 'T', TERMINATE.	A full restore was requested. The OLT was unable to locate an SD directory on cylinder 561. The option is to input SD data from a card deck.	If a card deck is to be used, respond 'Y'. Respond 'T' to terminate the OLT. See OLT users guide (order number D99-3350) for details on ordering a card deck containing SD data.
T3350 PSC	CECOM 568	HDA CONTAINS A PARTIAL SD DIRECTORY. CONTINUE WITH PARTIAL DIRECTORY. ENTER 'Y', YES OR 'N', NO.	This message is output when routine M1, M2 or M3 is requested and the OLT can only find a partial SD directory on cylinder 561.	Reply 'N' to terminate the OLT. If routine M1 or M2 has been selected, reply 'Y' will cause tracks beyond the end of the directory, which are rewritten, to output CECOM 565 to elicit SD data from the console. If routine M3 has been selected, reply 'Y' will cause all tracks beyond the end of the directory, which are rewritten, to use SD=0.
T3350 PSC	CECOM 569	PERMANENT ERROR READING THE SD DIRECTORY.	This message is output to indicate that part, or all of the SD directory on cylinder 561 is unreadable. This message is always followed by message CECOM 558.	Information only
T3350 PSC	CECOM 570	ENTER 'T' - TERMINATE, 'S' - SKIP RECORD, OR 'N' - CONTINUE WITH NO DIRECTORY.	This message always follows message CECOM 558.	'T' - terminate the OLT; 'S' skip the directory record in error (all SD data that would have come from the skipped record will be set to zero); 'N' - from this point on, bad tracks will cause message CECOM 565 to be output, requesting SD data from the console.
T3350 PSC	CECOM 001	ERROR ENCOUNTERED	This error print is output with CECOMs that give the user an option to retry a failing chain.	The user should examine the SENSE and CCW to determine the problem. Go to common action B, OLT 29. Retry the chain after the problem is corrected.

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WRITE TEST

Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350WT	**CECOM 064**	ENTER TRACK TO TEST AS CCCHH (DEC) OR XCCCHH (HEX) DUMP VALUABLE DATA BEFORE CONTINUING, ENTER 'T' TO TERM OR SELECT CE TRACK (CYL 1024, ENTER 'X400HH')		Enter the track address to be tested or terminate the test. If a head is to be tested, use a CE track. Enter 'X40001' to run the write/read test on the CE cylinder 1024, head 1. Enter 'X4000A' to run the write/read test on the CE cylinder 1024, head 10. If tests have been run successfully on the CE track and the data on the track to be tested is considered scratch, then a non-CE track can be tested. The track address can be entered in either decimal or hex. Enter 05201 or 'X03401' to test cylinder 52, head 1. Enter 00311 or 'X0030B' to test cylinder 3, head 11. **Note:** *One track on the CE cylinder is error free and suitable for running OLT T3350 WT. A label on the rear of the HDA will identify the error free track. If no label is present track 1 is error free. Use parameters 'X4000HH' where HH is the track number in hex.*
T3350WT	**CECOM 065**	**WARNING** TESTING ON TRACK XXX XX (CCC HH IN DEC) ALL DATA ON THIS TRACK WILL BE DESTROYED		Verify and double check that the track to be tested is the one that you desire.
T3350WT	**CECOM 066**	REPLY 'GO' TO PROCEED, 'C' TO CHANGE OR 'T' TO TERM		If you do not want to destroy data on the track described in CECOM 065, reply 'C' to return to the track select mode (CECOM 064). If you do not want to continue T3350WT, reply 'T' to terminate the OLT. If it is OK to destroy the data on the track described in CECOM 065, reply 'GO' to start the write/read test.
T3350WT	**CECOM 067**	DEFECTIVE TRACK XXX XX (CCC HH IN DEC) TO BE UNFLAGGED OR ALTERNATE TRACK XXX XX (CCC HH IN DEC) TO BE UNFLAGGED	A defective or alternate track has been selected for the write/read test. Before testing can continue, the Home Address must be rewritten with bits 6 and 7 of the flag byte set to 00.	If this track is not to be tested, reply "C" or "T" to the CECOM 066 message that follows. If this track is to be tested, reply "GO". The track is re-flagged at the conclusion of testing.
T3350WT	**CECOM 068**	*WARNING*DEFECTIVE TRACK XXX XX(CCC HH IN DEC) NOT RE-FLAGGED OR *WARNING*ALTERNATE TRACK XXX XX(CCC HH IN DEC) NOT RE-FLAGGED	A defective or alternate flagged track was tested. At the conclusion of testing, the Write HA/R0 chain failed to re-flag this track.	Analyze the failure information presented with REFNUM 054 and: 1. Run T3350PSA, routine 2, and select this track (in hex) to determine the extent of the damage. 2. Run T3350PSA to scan the HDA for damage or erroneous HA or R0 fields. Restore HA and R0 on the track tested if necessary. 3. Go to Common Action C (OLT 29).
T3350WT	**CECOM 069**	CORE NOT AVAILABLE TO WRITE RECORDS>4K or >2K	The OLT attempts to get a Morecore Region of 4096 to 8192 bytes. If the message reads > 4K, only records 4096 bytes or shorter will be written. If the message reads > 2K only records 2048 bytes or shorter will be written. The test continues.	If the maximum test capability is desired, increase the region for OLTEP job. See the OLTEP system library manual for the region requirements for a 16K OLT.
T3350WT	**CECOM 070**	VOL ID ON XXXX IS YYYYYYYYYY	If the VOL ID (YYYYYYYYYY) is blank, this volume is unlabeled.	Verify that the correct drive and volume were selected before continuing. If either is incorrect, reply "T" to CECOM 064.
T3350WT	**CECOM 072**	*NO ERROR ON INDEX TEST	No Invalid Track Format (Sense Byte 1, bit 1) was presented while writing records longer than the 3330 track capacity.	1. This drive is configured as a 3330 compatible volume (CDS type 09 or 0D). Verify that the drive being tested is wired for 3330 Compatibility Mode. 2. Run microdiagnostic routine BB to test the Track Used (TR) Counter.

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WRITE TEST

Sect ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
T3350WT	00050	ERROR ON READ HA CHAIN or WRITE HA CHAIN or SENSE I/O CHAIN	The OLT terminates on any of these three errors. An error on the Read HA command ('1A') can be caused by a bad Home Address or a drive failure. An error on the Write HA command ('19') can be caused by a storage control or drive failure. An error on the Sense I/O command ('04') can be caused by a channel, storage control, or drive failure.	Rerun the test and select a CE track. 1. If the test runs successfully, the original track is probably damaged. Restore the HA and R0 fields by using the procedure under Common Action C (OLT 29). 2. If the test fails on the CE tracks, go to Common Action B (OLT 29).
T3350WT	00051	ERROR ON READ ID CHAIN	An error occurred while attempting to Search and Read Record 3 on track 0. The test continues to test write/read on the selected track.	1. If the test runs successfully on the selected track, there is damage on the label record (track 0). Restore the label. 2. If the test fails on the selected track, follow the CE Action under the REFNUMs produced by the test.
T3350WT	00052	ERROR ON WRITE R0 CHAIN or WRITE CKD CHAIN	These errors cause the current routine to terminate. See the first line of the error message for the routine number (RTN XX).	Rerun the test and select a CE track. 1. If the test runs successfully, the non CE track that previously failed is is probably damaged. Flag the track defective (See OLT 30). 2. If the test fails on the CE tracks, go to Common Action B (OLT 29). 3. Run OLT T3350PSA for final verification that the problem has been resolved.
T3350WT	00053	ERROR ON READ R0 CHAIN or READ CKD CHAIN		
T3350WT	00054	ERROR ON WRITE R0 CHAIN or WRITE HA CHAIN	WRITE R0 CHAIN indicates an error terminated the chain to re-write a standard R0 on the track being tested. WRITE HA CHAIN indicates an error terminated the chain to re-write an alternate or defective HA and R0 following testing. If the Write HA chain failed, this defective or alternate track may not be flagged.	
T3350WT	00055	ERROR ON INDEX TEST, SNS BYTE 1 BIT 1 NOT ON	Some error other than Invalid Track Format occurred while writing records that were longer than the 3330 track capacity.	Go to Common Action B (OLT 29).

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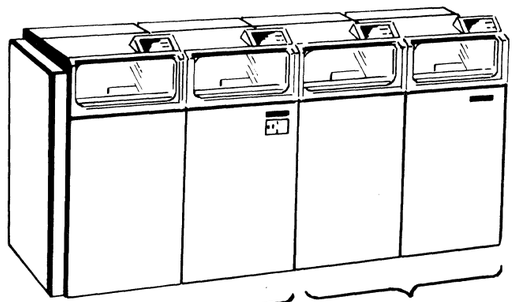
INTRODUCTION

The IBM 3350 Disk Storage is a direct access storage device. The IBM 3350 contains the following physical units:

- Control module A2 (A2F with fixed heads)
- Satellite module B2 (B2F with fixed heads)

For C2 (C2F) Module information, see FSI 970 through 986.



CONTROL MODULE A2 (A2F)

The control module contains:

- Controller
- Drives A and B

Controller

The controller performs the following:

- Receives control information, data, and commands from storage control.
- Controls the operation of drives A and B and any satellite modules with the control information, data, and commands.
- Receives control information, data, and status information from drives A and B and from any satellite module(s).
- Sends the control information, data, and status information to storage control.
- Sends controller status information to storage control.

See OPER 4 for details.

Drive A (or B)

Drive A (or B) performs the following:

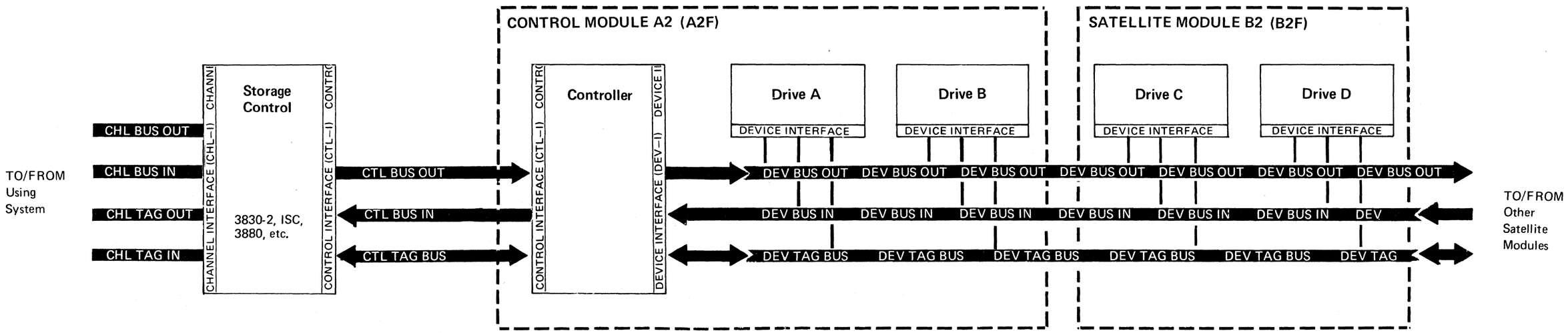
- Receives control information and data from the controller.
- Controls the operation of the Head/Disk Assembly (HDA) with the control information and data.
- Receives control information, data, and status information from the HDA.
- Sends the control information, data, and status information to the controller.
- Sends drive status information to the controller.

See OPER 15 for details.

SATELLITE MODULE B2 (B2F)

The satellite module B2, contains two drives. Each drive performs the same functions as drive A (or B) in a control module.

Three satellite modules can be connected to a control module.



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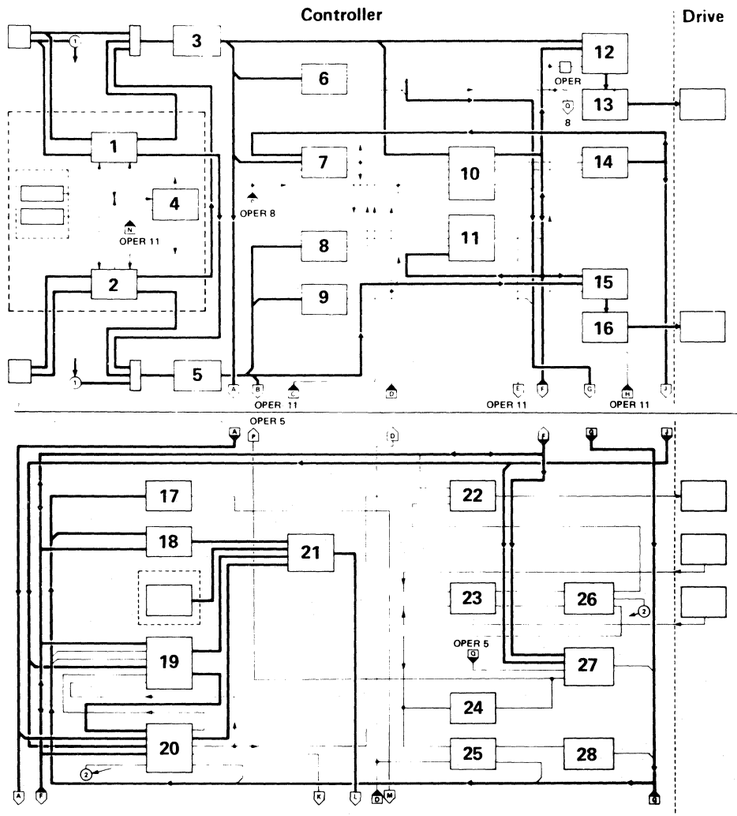
FUNCTIONAL UNITS

CONTROLLER

The following pages describe the functional units in the controller. The diagram on this page gives an overall view of the controller functional logic diagram. As indicated on the overall view, the diagram is contained on three pages: Oper 5, 8, and 11. Each of these pages is followed by pages explaining each functional unit as follows:

- **The input, or inputs, to the functional unit and their source.**
- **The function of the functional unit.**
- **The output, or outputs, from the functional unit and their destination.**

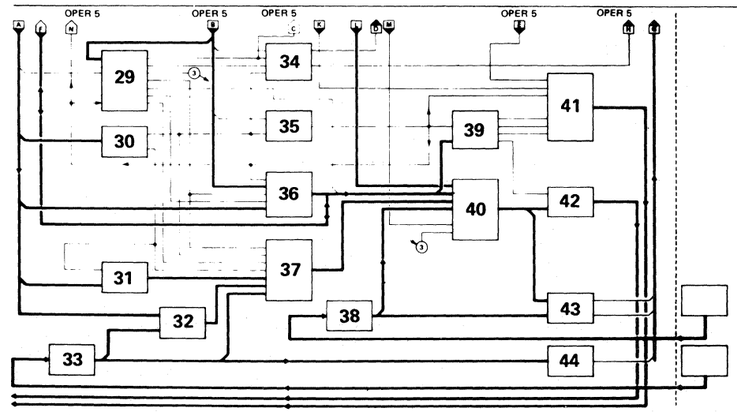


OPER 5

1. String Switch Select A (Cards A2D2 and A2H2)
2. String Switch Select B (Cards A2E2 and A2J2)
3. Ctl Bus Out NPL to MST Convertor (Card A2G2)
4. String Switch A and B Common Circuitry (Card A2M2)
5. Ctl Tag Bus Out NPL to MST Convertor (Card A2G2)
6. Bus Out Parity Check (Card A2G2)
7. Gap Counter and Control (Card A2P2)
8. Read Op and Write Op Tags Decoder (Card A2L2)
9. Tag Bus Parity Check (Card A2G2)
10. Macros-Operation Control (Card A2Q2)
11. Op End Generator (Card A2P2)
12. Bits Out Gate (Card A2F2)
13. Bits Out to Dev Bus Out Convertor (Card A2F2)
14. ECC Control (Card A2P2)
15. Dev Tag Bus Generator (Card A2L2)
16. Dev Tag Bus MST to NPL Convertor (Card A2L2)

OPER 8

17. Controller Error Indicator (Card A2K2)
18. Check Bit Register (Card A2K2)
19. Error Correction (Card A2R2)
20. SERDES (Card A2S2)
21. Assm Register (Card A2K2)
22. Write Data Gate (Card A2T2)
23. Read Data Gate (Card A2T2)
24. Bit Ring (Card A2S2)
25. Reorient Counter (Card A2R2)
26. Variable Frequency Oscillator –VFO–(Card A2T2)
27. Track Used Counter (Card A2N2)
28. Status Monitor Check (Card A2L2)



OPER 11

29. Tag Bus Bits Decoder (Card A2G2)
30. Controller Address Compare (Card A2G2)
31. Poll Addr Bit Decoder (Card A2G2)
32. Unsuppr Attn Bits Generator (Card A2G2)
33. Attn/Sel Bus NPL to MST Convertor (Card A2G2)
34. Read/Write Control (Card A2L2)
35. Select Control (Card A2G2)
36. Operation Control (Card A2L2)
37. Poll/Select Reg and Control (Card A2G2)
38. Dev Bus In NPL to MST Convertor (Card A2F2)
39. Tags In Generator (Card A2K2)
40. Ctl Bus In Reg and Control (Card A2E2)
41. Tags In MST to NPL Convertor (Card A2K2)
42. Ctl Bus In MST to NPL Convertor (Card A2F2)
43. Dev Bus In and Ctl Bus In Parity Check (Card A2F2)
44. Attn/Sel Bus (1-of-8) Check (Card A2G2)

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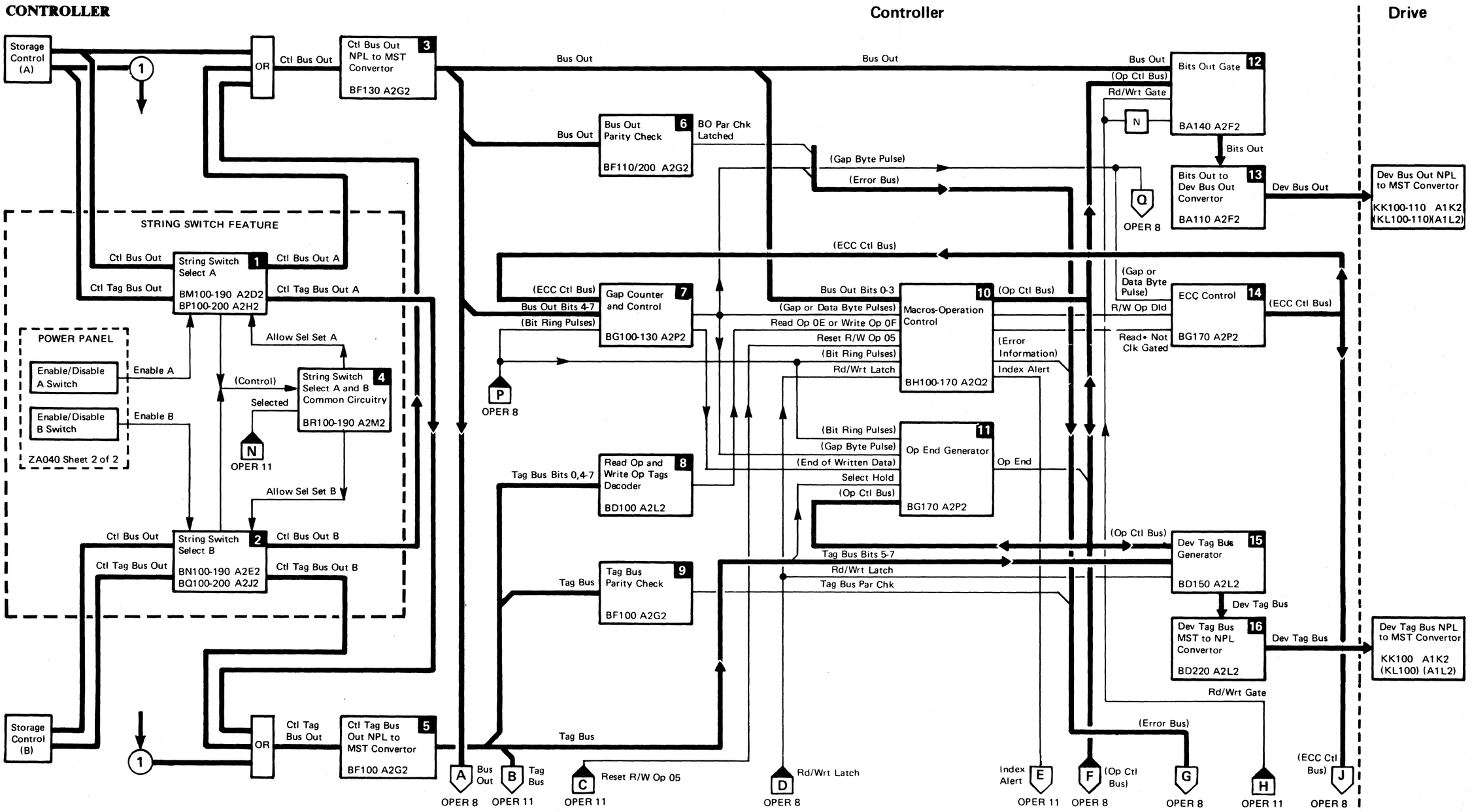

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FUNCTIONAL UNITS

CONTROLLER (Continued)

1 String Switch Select A (Cards A2D2 and A2H2)

The String Select Switch A functions as follows:

- Receives

  Ctl Bus Out and Ctl Tag Bus Out from storage control A.

  Enable A from the Enable/Disable A Switch on the power panel.

  Allow Sel Set A from the String Switch Select A and B Common Circuitry (card A2M2).
- Sends Ctl Bus Out A to the Ctl Bus Out NPL to MST Convertor (card A2G2).
- Sends Ctl Tag Bus Out A to the Ctl Tag Bus Out NPL to MST Convertor (card A2G2).
- Sends control signals to the String Switch Select A and B Common Circuitry (card A2M2)

2 String Switch Select B (Cards A2E2 and A2J2)

The String Switch Select B functions as follows:

- Receives

  Ctl Bus Out and Ctl Tag Bus Out from storage control B.

  Enable B from the Enable/Disable B Switch on the power panel.

  Allow Sel Set B from the String Switch A and B Common Circuitry (card A2M2).
- Sends Ctl Bus Out B to the Ctl Bus Out NPL to MST Convertor (card A2G2).
- Sends Ctl Tag Bus Out B to the Ctl Tag Bus Out NPL to MST Convertor (card A2G2).
- Sends control signals to the String Switch Select A and B Common Circuitry (card A2M2)

3 Ctl Bus Out NPL to MST Convertor (Card A2G2)

The Ctl Bus Out NPL to MST Convertor functions as follows:

- Receives Ctl Bus Out from one of the following:

  Storage Control

  String Switch Select A (cards A2D2 and A2H2)

  String Switch Select B (cards A2E2 and A2J2)
- Converts Ctl Bus Out NPL voltage levels to Ctl Bus Out MST voltage levels.
- Sends Bus Out to the following:

  Bits Out Gate (card A2F2)

  Macros-Operation Control (card A2Q2)

  Bus Out Parity Check (card A2G2)

  Gap Counter Control (card A2P2)

  SERDES (card A2S2)

  Tag Bus Bits Decoder (card A2G2)

  Controller Address Compare (card A2G2)

  Operation Control (card A2L2)

  Poll Addr Bit Decoder (card A2G2)

  Unsuppr Attn Bits Generator (card A2G2)

4 String Switch A and B Common Circuitry (Card A2M2)

The String Switch A and B Common Circuitry functions as follows:

- Receives control signals from the following:

  String Switch Select A (cards A2D2 and A2H2)

  String Switch Select B (cards A2E2 and A2J2)
- Receives the signal, Selected, from the Select Control (card A2G2).
- Generates Allow Sel Set A or Allow Sel Set B.
- Sends Allow Sel Set A to the String Switch Select A (cards A2D2 and A2H2).
- Sends Allow Sel Set B to the String Switch Select B (cards A2E2 and A2J2).

5 Ctl Tag Bus Out NPL to MST Convertor (Card A2G2).

The Ctl Tag Bus Out NPL to MST Convertor functions as follows:

- Receives Ctl Tag Bus Out from one of the following:

  Storage Control

  String Switch Select A (cards A2D2 and A2H2)

  String Switch Select B (cards A2E2 and A2J2)
- Converts Ctl Tag Bus Out NPL voltage levels to Ctl Tag Bus Out MST voltage levels.
- Sends Tag Bus MST voltage levels to the following:

  Read Op and Write Op Tags Decoder (card A2L2)

  Tag Bus Parity Check (card A2G2)

  Dev Tag Bus Generator (card A2L2)

  Tag Bus Bits Decoder (card A2G2)

  Read/Write Control (card A2L2)

  Select Control (card A2G2)

  Operation Control (card A2L2)

6 Bus Out Parity Check (Card A2G2)

The Bus Out Parity Check functions as follows:

- Receives Bus Out from the Ctl Bus Out NPL to MST Convertor (card A2G2).
- Checks the parity of Bus Out.
- Generates BO Par Chk Latched when a Bus Out parity error occurs.
- Sends BO Par Chk Latched via the Error Bus to the following:

  Check Bit Register (card A2K2)

  Controller Error Indicator (card A2K2)

7 Gap Counter and Control (Card A2P2)

The Gap Counter and Control functions as follows:

- Receives

  ECC control signals via the ECC Ctl Bus from the ECC Control (card A2P2).

  Bus Out Bits 4 through 7 from the Ctl Bus Out NPL to MST Convertor (card A2G2).

  Bit ring pulses from the Bit Ring (card A2S2).

During a read operation, the Gap Counter:

- Counts the bit ring pulses. Each bit ring pulse represents one gap byte or one data byte.
- Generates a gap byte pulse or a data byte pulse.
- Sends a gap byte pulse or a data byte pulse to the following:

  Macros-Operation Control (card A2Q2)

  Op End Generator (card A2P2)

  Check Bit Register (card A2K2) via the Error Bus.

  ECC Control (card A2P2)

  Track Used Counter (card A2N2)

During a Write operation, the Gap Counter:

- Generates a signal to indicate the end of written data.
- Sends this signal to the Op End Generator (card A2P2).

8 Read Op and Write Op Tags Decoder (Card A2L2)

The Read Op and Write Op Tags Decoder functions as follows:

- Receives Tag Bus Bits 0, 4 through 7 from the Ctl Tag Bus Out NPL to MST Convertor (card A2G2).
- Decodes Tag Bus Bits 0, 4 through 7 into one of the following:

  Read Op 0E

  Write Op 0F
- Sends Read Op 0E or Write Op 0F to Macros-Operation Control (card A2Q2).

9 Tag Bus Parity Check (Card A2G2)

The Tag Bus Parity Check functions as follows:

- Receives Tag Bus from the Ctl Tag Bus Out NPL to MST Convertor (card A2G2).
- Checks the parity of Tag Bus.
- Generates Tag Bus Par Chk when a Tag Bus parity error occurs.
- Sends Tag Bus Par Chk to the Check Bit Register (card A2K2).

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FUNCTIONAL UNITS

10 CONTROLLER (Continued)

Macros-Operation Control (Card A2Q2)

The Macros-Operation Control functions as follows:

- Receives

  Bus Out Bits 0 through 3 from the Ctl Bus Out NPL to MST Convertor (card A2G2).

  Gap byte pulses or data byte pulses from the Gap Counter (card A2P2).

  Read Op 0E or Write Op 0F from the Read Op and Write Op Tags Decoder (card A2L2).

  Reset R/W Op 05 from the Tag Bus Bits Decoder (card A2G2).

  Bit ring pulses from the Bit Ring (card A2S2).

  Rd/Wrt Latch from the Read/Write Control (card A2L2).

- Generates operation control signals and sends these signals via the Op Ctl Bus to the following:

  Bits Out Gate (card A2F2)

  Dev Tag Bus Generator (card A2L2)

  Op End Generator (card A2F2)

  Track Used Counter (card A2N2)

  Write Data Gate (card A2T2)

  Check Bit Register (card A2K2)

  SERDES (card A2S2)

  Tags In Generator (card A2K2)

- Generates R/W Op Dld, and, Read*Not Clk Gated and sends them to the ECC Control (card A2P2).
- Generates error information and sends it via the Error Bus to the Check Bit Register (card A2K2).
- Generates the tag Index Alert and sends it to the Tags In MST to NPL Convertor (card A2K2).

11 Op End Generator (Card A2P2)

The Op End Generator functions as follows:

- Receives

  Bit ring pulses from the Bit Ring (card A2S2).

  A gap byte pulse from the Gap Counter (card A2P2) indicating the end of a gap.

  The "end of written data" signal from the Gap Counter (card A2P2).

  Select Hold via Tag Bus from the Ctl Tag Bus Out MST to NPL Convertor (card A2G2).

  Operation control signals via the Op Ctl Bus from the Macros-Operation Control (card A2Q2).

- Generates Op End at the fall of Select Hold.
- Sends Op End via the Op Ctl Bus to the Tags In Generator (card A2K2).

12 Bits Out Gate (Card A2F2)

The Bits Out Gate functions as follows:

- Receives

  Bus Out from the Ctl Bus Out NPL to MST Convertor (card A2G2).

  Operation control signals via the Op Ctl Bus from the Macros-Operation Control (card A2Q2).

  Rd/Wrt Gate from the Read/Write Control (card A2L2).

- Sends Bus Out or the operation control signals via Bits Out to the Bits Out to Dev Bus Out Convertor (card A2F2).
- Rd/Wrt Gate gates the control signals to the Bits Out to Dev Bus Out Convertor (card A2F2).
- (Not) Rd/Wrt Gate gates Bus Out to the Bits Out to Dev Bus Out Convertor (card A2F2).

13 Bits Out to Dev Bus Out Convertor (Card A2F2)

The Bits Out to Dev Bus Out Convertor functions as follows:

- Receives Bits Out from the Bits Out Gate (card A2F2).
- Converts Bits Out MST voltage levels into Dev Bus Out NPL voltage levels.
- Sends Dev Bus Out to the Dev Bus Out NPL to MST Convertor in a drive.

14 ECC Control (Card A2P2)

The ECC Control functions as follows:

- Receives

  Gap byte pulse or data byte pulse from the Gap Counter and Control (card A2P2)

  R/W Op Dld from the Macros-Operation Control (card A2Q2)

  Read * Not Clk Gated from Macros-Operation Control (card A2Q2)

- Generates ECC Control signals.
- Sends the ECC Control signals via the ECC Ctl Bus to the following:

  Gap Counter and Control (card A2P2)

  Track Used Counter (card A2N2)

  Error Correction (card A2R4)

  SERDES (card A2S2)

15 Dev Tag Bus Generator (Card A2L2)

The Dev Tag Bus Generator functions as follows:

- Receives

  Operation control signals via the Op Ctl Bus from the Macros-Operation Control (card A2Q2).

  Tag Bus Bits 5 through 7 from the Ctl Bus Out NPL to MST Convertor (card A2G2).

  Rd/Wrt Latch from the Read/Write Control (card A2L2).

- Generates Dev Tag Bus.
- Rd/Wrt Latch gates Dev Tag Bus to the Dev Tag Bus MST to NPL Convertor (card A2L2).

16 Dev Tag Bus MST to NPL Convertor (Card A2L2)

The Dev Tag Bus MST to NPL Convertor functions as follows:

- Receives the Dev Tag Bus from the Dev Tag Bus Generator (card A2L2).
- Converts Dev Tag Bus MST voltage levels into Dev Tag Bus NPL voltage levels.
- Sends Dev Tag Bus NPL voltage levels to the Dev Tag Bus NPL to MST Convertor in a drive.

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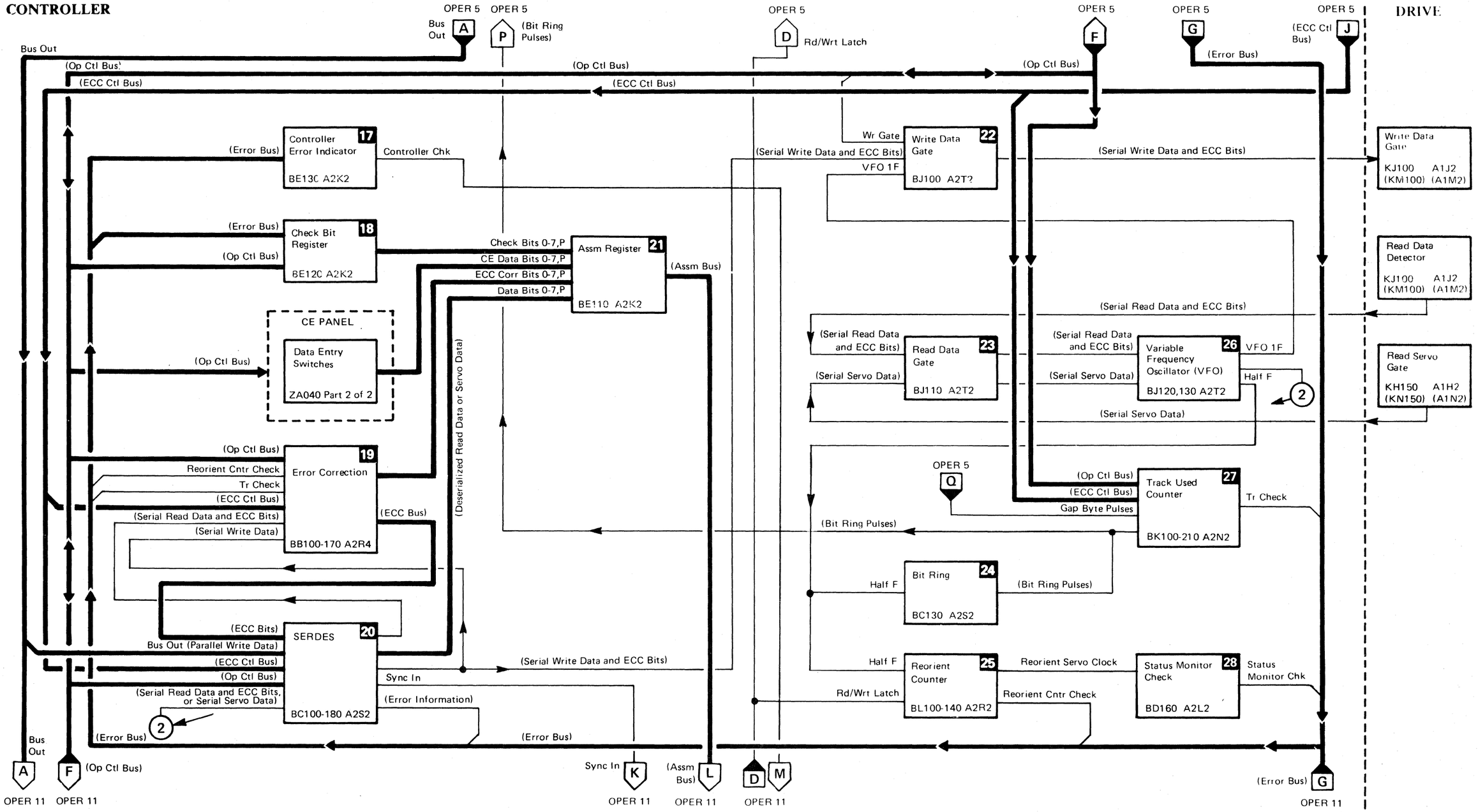
CONTROLLER



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17 CONTROLLER (Continued)

Controller Error Indicator (Card A2K2)

The Controller Error Indicator functions as follows:

- Receives error information via the Error Bus from the following:

  SERDES (card A2S2)

  Reorient Counter (card A2R2)

  Status Monitor Check (card A2L2)

  Dev Bus In and Ctl Bus In Parity Check (card A2F2)

  Track Used Counter (card A2N2)

  Attn/Sel Bus (1-of-8) Check (card A2G2)

  Bus Out Parity Check (card A2G2)

- Generates Controller Chk from any one of the above.
- Sends Controller Chk to the Ctl Bus In Register (card A2F2).

18 Check Bit Register (Card A2K2)

The Check Bit Register functions as follows:

- Receives error information via the Error Bus from the following:

  SERDES (card A2S2).

  Status Monitor Check (card A2L2).

  Dev Bus In and Ctl Bus In Parity Check (card A2F2).

  Attn/Sel Bits (1-of-8) Check (card A2F2).

  Tag Bus Out Parity Check (card A2G2).

  Macros-Operation Control (card A2Q2).

  Bus Out Parity Check (card A2G2).

  Gap Counter (card A2P2).

- Also receives operation control signals via the Op Ctl Bus from the following:

  Macros-Operation Control (card A2Q2).

- Generates Check Bits 0 through 7,P.
- Sends Check Bits 0 through 7, P (error information) to the Assm Register (card A2K2).

19 Error Correction (Card A2R4)

During a Read operation the Error Correction functions as follows:

- Receives serial read data and ECC bits from the SERDES (card A2S2).
- Compares the serial read data to the ECC bits.
- Generates ECC Corr Bits 0 through 7,P, when an error exists in the received serial read data.
- Sends the ECC Corr Bits 0 through 7,P, to the Assm Register (card A2K2).

During a Write operation the Error Correction functions as follows:

- Receives serial write data from the SERDES (card A2S2).
- Produces ECC bits from the serial write data.
- Sends the ECC bits to the SERDES (card A2S2).

The Error Correction also receives:

Operation control signals via the Op Ctl Bus from the Operations Control (card A2L2).

Reorient Cntr Check via the Error Bus from the Reorient Counter (card A2R2).

Tr Check via the Error Bus from the Track Used Counter (card A2N2).

ECC control signals via the ECC Ctl Bus from the ECC Control (card A2P2).

The Error Correction sends Reorient Cntr Check and Tr Check via the ECC Corr bits to the Assm Register (card A2K2).

20 SERDES (Card A2S2)

During a Read operation the SERDES functions as follows:

- Receives serial read data and ECC bits, or serial servo data, from the Variable Frequency Oscillator (card A2T2).
- Sends the serial read data and ECC bits to the Error Correction (card A2R4).
- Deserializes the serial read data, or the serial servo data, from the Variable Frequency Oscillator (card A2T2).
- Sends the deserialized read data, or the deserialized servo data, via the Data Bits 0 through 7, P to the Assm Register (card A2K2).

During a Write operation the SERDES functions as follows:

- Receives and serializes parallel write data via Bus Out from the Ctl Bus Out NPL to MST Convertor (card A2G2).
- Sends the serialized write data to the Error Correction (card A2R4).
- Receives ECC bits from the Error Correction (card A2R4).
- Sends the serialized write data and the ECC bits to the Write Data Gate (card A2T2).

The SERDES also receives the following:

ECC control signals via the ECC Ctl Bus from the ECC Control (card A2P2) and sends these signals to the Error Correction (card A2R4).

Operation control signals via the Op Ctl Bus from the Macros-Operation Control (card A2Q2).

The SERDES generates the tag, Sync In, and sends it to the Tags In MST to NPL Convertor (card A2K2).

The SERDES also generates error information and sends it via the Error Bus to the following:

Check Bit Register (card A2K2).

Controller Error Indicator (card A2K2).

21 Assm Register (Card A2K2)

The Assm Register functions as follows:

- Receives

  Check Bits 0 through 7, P from the Check Bit Register (card A2K2).

  CE Data Bits 0 through 7, P from the Data Entry Switches on the CE Panel.

  ECC Corr Bits 0 through 7, P from the Error Correction (card A2R4).

  Data Bits 0 through 7, P (deserialized read data or servo data) from the SERDES (card A2S2).

- Sends the Check Bits, CE Data Bits, ECC Corr Bits, or Data Bits via the Assm Bus to the Ctl Bus In Register (card A2F2).

22 Write Data Gate (Card A2T2)

The Write Data Gate functions as follows:

- Receives

  Wr Gate via the Op Ctl Bus from the Macros-Operation Control (card A2Q2).

  Serial write data and ECC bits from the SERDES (card A2S2).

  VFO 1F from the Variable Frequency Osciallator (card A2T2).

- VFO 1F and Wr Gate gate the serial write data and ECC bits to the Write Data Gate in a drive.

23 Read Data Gate (Card A2T2)

The Read Data Gate functions as follows:

- Receives

  Serial read data and ECC bits from the Read Data Detector in a drive.

  Serial servo data from the Read Servo Gate in a drive.

- Sends the serial read data and ECC bits, or the serial servo data, to the Variable Frequency Oscillator (card A2T2).

24 Bit Ring (Card A2S2)

The Bit Ring functions as follows:

- Receives the signal, Half F, from the Variable Frequency Oscillator (card A2T2).
- Counts the Half F pulses and generates a bit ring pulse for each eighth pulse (each byte) counted.
- Sends bit ring pulses to the following:

  Track Used Counter (card A2N2)

  Gap Counter and Control (card A2P2)

  Macros-Operation Control (card A2Q2)

  Op End Generator (card A2P2)

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FUNCTIONAL UNITS

CONTROLLER (Continued)

25 Reorient Counter (Card A2R2)

The Reorient Counter functions as follows:

- Receives

  Half F pulses from the Variable Frequency Oscillator (card A2T2).

  Rd/Wrt Latch from the Read/Write Control (card A2L2).

- Counts the Half F pulses.
- Generates Reorient Cntr Check when a certain number of Half F pulses are counted.
- Sends Reorient Cntr Check via the Error Bus to the following:

  Error Correction (card A2R4)

  Controller Error Indicator (card A2K2)

The Reorient Counter also generates Reorient Servo Clock and sends it to the Status Monitor Check (card A2L2).

26 Variable Frequency Oscillator—VFO—(Card A2T2)

During a Read operation the Variable Frequency Oscillator (VFO) functions as follows:

- Receives one of the following from the Read Data Gate (card A2T2):

  Serial read data and ECC bits

  Serial servo data

- Adjusts its frequency to the frequency of the serial read data and ECC bits or the serial servo data.
- Stabilizes the frequency of the serial read data and ECC bits or the serial servo data.
- Sends the serial read data and ECC bits or the serial servo data to the SERDES (card A2S2).

During a Write operation the Variable Frequency Oscillator (VFO) frequency VFO 1F is used by the Write Data Gate (card A2T2).

The Variable Frequency Oscillator (VFO) frequency Half F is used by the following:

Bit Ring (card A2S2)

Reorient Counter (card A2R2)

27 Track Used Counter (Card A2N2)

The Track Used Counter functions as follows:

- Receives

  Operation control signals via the Op Ctl Bus from the Macros-Operation Control (card A2Q2).

  ECC control signals via the ECC Ctl Bus from the ECC Control (card A2P2).

  Gap byte pulses from the Gap Counter (card A2P2).

  Bit ring pulses from the Bit Ring (card A2S2).

- Counts the bit ring pulses (bytes) during a Write operation.
- Generates Tr Check when more bytes are counted than should be written.
- Sends Tr Check via the Error Bus to the following:

  Error Correction (card A2R4)

  Controller Error Indicator (card A2K2)

28 Status Monitor Check (Card A2L2)

The Status Monitor check functions as follows:

- Receives Reorient Servo Clock from the Reorient Counter (card A2R2).
- Generates the signal, Status Monitor Chk.
- Sends Status Monitor Chk via the Error Bus to the following:

  Check Bit Register (card A2K2).

  Controller Error Indicator (card A2K2).

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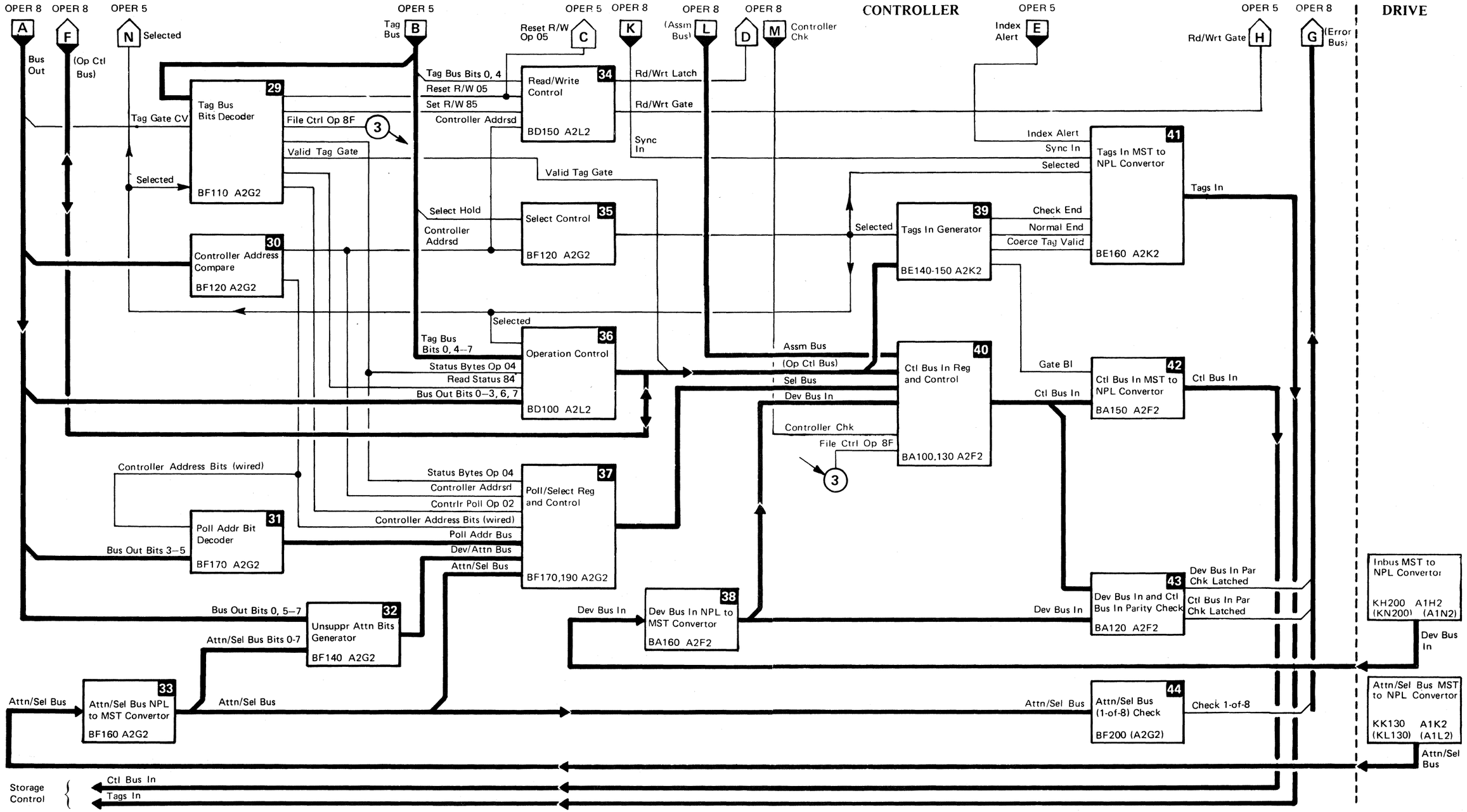

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FUNCTIONAL UNITS

CONTROLLER (Continued)

29 Tag Bus Bits Decoder (Card A2G2)

The Tag Bus Bits Decoder functions as follows:

- Receives

  Tag Bus from the Ctl Tag Bus Out NPL to MST Convertor (card A2G2).

  The signal, Tag Gate CV, via Bus Out from the Ctl Bus Out NPL to MST Convertor (card A2G2).

  The signal, Selected, from the Select Control (card A2G2).

- Decodes Tag Bus into one of the following tags:

Tag	Signal Name	Gated, by Selected, to:
05	Reset R/W Op 05	Read/Write Control (card A2L2) Macros-Operation Control (card A2Q2)
85	Set R/W Op 85	Read/Write Control (card A2L2)
8F	File Ctrl Op 8F	Ctl Bus In Register (card A2F2)
04	Status Bytes Op 04	Operation Control (card A2L2) Poll/Select Reg Control (card A2G2)
84	Read Status 84	Operation Control (card A2L2)
02	Contrlr Poll Op 02	Poll/Select Reg Control (card A2G2)

- Generates the signal Valid Tag Gate from the signal Tag Gate CV.
- Sends Valid Tag Gate via the Op Ctl Bus to the Tags In Generator (card A2K2).

30 Controller Address Compare (Card A2G2)

The Controller Address Compare functions as follows:

- Receives Bus Out from the Ctl Bus Out NPL to MST Convertor (card A2G2).
- Compares Bus Out Bits 0 through 2 with controller address bits wired on card A2G2.
- Generates Controller Addrsd when Bus Out Bits 0 through 2 and the controller address wired on card A2G2 are equal.
- Sends Controller Addrsd to the following:

  Read/Write Control (card A2L2)

  Select Control (card A2G2)

  Poll/Select Reg Control (Card A2G2)

31 Poll Addr Bit Decoder (Card A2G2)

The Poll Addr Bit Decoder functions as follows:

- Receives

  Controller address bits wired on card A2G2.

  Bus Out Bits 3 through 5 from the Ctl Bus Out NPL to MST Convertor (card A2G2).

- Decodes the controller address bits wired on card A2G2 and the Bus Out Bits 3 through 5 into 1-of-8 Poll Addr bits.
- Sends the decoded Poll Addr bit via the Poll Addr Bus to the Poll/Select Reg (card A2G2).

32 Unsuppr Attn Bits Generator (Card A2G2)

The Unsuppr Attn Bits Generator functions as follows:

- Receives

  Bus Out Bits 0, 5 through 7 from the Ctl Bus Out NPL to MST Convertor (card A2G2).

  Attn/Sel Bus Bits 0 through 7 from the Attn/Sel Bus NPL to MST Convertor (card A2G2)

- Selects the Attn/Sel Bus bits to be sent via the Dev/Attn Bus to the Poll/Select Reg (card A2G2)

33 Attn/Sel Bus NPL to MST Convertor (Card A2G2)

The Attn/Sel Bus NPL to MST Convertor functions as follows:

- Receives the Attn/Sel Bus from the Attn/Sel Bus MST to NPL Convertor in a drive.
- Converts Attn/Sel Bus NPL voltage levels to Attn/Sel Bus MST voltage levels.
- Sends Attn/Sel Bus to the following:

  Unsuppr Attn Bits Generator (card A2G2)

  Poll/Select Reg (card A2G2)

  Attn/Sel Bus (1-of-8) Check (card A2G2)

34 Read/Write Control (Card A2L2)

The Read/Write Control functions as follows:

- Receives

  Tag Bus Bits 0, 4 from the Ctl Tag Bus Out NPL to MST Convertor (card A2G2).

  Reset R/W Op 05 (tag 05) and Set R/W Op 85 (tag 85) from the Tag Bus Bits Decoder (card A2G2).

  Controller Addrsd from the Controller Address Compare (card A2G2).

- Generates the signal Rd/Wrt Latch and the signal Rd/Wrt Gate.
- Sends Rd/Wrt Latch to the following:

  Reorient Counter (card A2R2)

  Dev Tag Bus Generator (card A2L2)

  Macros-Operation Control (card A2Q2)

- Sends Rd/Wrt Gate to the Bits Out Gate (card A2F2).

35 Select Control (Card A2G2)

The Select Control functions as follows:

- Receives

  Select Hold via the Tag Bus from the Ctl Tag Bus Out NPL to MST Convertor (card A2G2).

  Controller Addrsd from the Controller Address Compare (card A2G2)

- Generates the signal, Selected.
- Sends Selected to the following:

  Tags In Generator (card A2K2)

  Tags In MST to NPL Convertor (card A2K2)

  Operation Control (card A2L2)

  Tag Bus Bits Decoder (card A2G2)

  String Select Switch A and B Common Circuitry (card A2M2)

36 Operation Control (Card A2L2)

The Operation Control functions as follows:

- Receives

  Selected from the Select Control (card A2L2).

  Tag Bits 0, 4 through 7 from the Ctl Tag Bus Out NPL to MST Convertor (card A2G2).

  Status Bytes 04 and Read Status 84 from the Tag Bus Bits Decoder (card A2G2).

  Bus Out Bits 0 through 3,6,7 from the Ctl Bus Out NPL to MST Convertor (card A2G2).

- Generates operation control signals.
- Sends operation control signals via the Op Ctl Bus to the following:

  Ctl Bus In Reg (card A2F2)

  Tags In Generator (card A2K2)

  Error Correction (card A2R4)

  Check Bit Register (card A2K2)

  CE Panel

37 Poll/Select Reg and Control (Card A2G2)

The Poll Select Reg and Control functions as follows:

- Receives

  Status Bytes 04 and Contrlr Poll Op 02 from the Tag Bus Bits Decoder (card A2G2).

  Controller Addrsd from the Controller Address Compare (card A2G2)

  Controller address bits wired on card A2G2.

  Poll Addr bit via the Poll Addr Bus from the Poll Addr Bit Decoder (card A2G2).

  Dev/Attn Bus from the Unsuppr Attn Bits Generator (card A2G2).

  Attn/Sel Bus from the Attn/Sel Bus NPL to MST Convertor (card A2G2).

- Status Bytes 04 and Contrlr Poll Op 02 gate one of the following through the Poll/Select Reg to the Ctl Bus In Reg (card A2E2):

  Controller address bits wired.

  Poll Addr bit

  Dev/Attn Bus

  Attn/Sel Bus

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FUNCTIONAL UNITS

CONTROLLER (Continued)

38 Dev Bus In NPL to MST Convertor (Card A2F2)

The Dev Bus In NPL to MST Convertor functions as follows:

- Receives Dev Bus In from the NPL Inbus MST to NPL Convertor in a drive.
- Converts Dev Bus In voltage levels to Dev Bus In MST voltage levels.
- Sends the Dev Bus In MST voltage levels to the Ctl Bus In Reg (card A2F2) and to the Dev Bus In Parity Check (card A2F2).

39 Tags In Generator (Card A2K2)

The Tags In Generator functions as follows:

- Receives Selected from the Select Control (card A2G2).
- Generates Gate BI from Selected
- Sends Gate BI to the Ctl Bus In MST to NPL Convertor (card A2F2).
- Also receives operation control signals via the Op Ctl Bus from the following:

  Operation Control (card A2L2)

  Tag Bus Bits Decoder (card A2G2)

  Op End Generator (card A2P2)

  Macros-Operation Control (card A2Q2)
- Generates the tags: Check End, Normal End, and Coerce Tag Valid.
- Sends the generated tags to the Tags In MST to NPL Convertor (card A2K2).

40 Ctl Bus In Reg and Control (Card A2E2)

The Ctl Bus In Reg and Control functions as follows:

- Receives

  Assm Bus from the Assm Register (card A2K2).

  Operation control signals via the Op Ctl Bus from the Operation Control (card A2L2).

  Sel Bus from the Poll Select Reg (card A2G2).

  Dev Bus In from the Dev Bus In NPL to MST Convertor (card A2F2).

  Controller Chk from the Controller Error Indicator (card A2K2).

  File Ctrl Op 8F from the Tag Bus Bits Decoder (card A2G2)
- Places Controller Chk on Dev Bus In.
- Sends Assm Bus, Sel Bus, or Dev Bus In via Ctl Bus In to the Ctl Bus In MST to NPL Convertor (card A2F2).

41 Tags In MST to NPL Convertor (Card A2K2)

The Tags In MST to NPL Convertor functions as follows:

- Receives the following Tags In MST voltage levels:

  Index Alert from the Macros-Operation Control (card A2Q2).

  Sync In from the SERDES (card A2S2)

  Selected from the Select Control (card A2G2)

  Check End, Normal End, or Coerce Tag Valid from the Tags In Generator (card A2K2).
- Converts Tags In MST voltage levels to Tags In NPL voltage levels.
- Sends Tags In NPL voltage levels via Tags In to storage control.

42 Ctl Bus In MST to NPL Convertor (Card A2F2)

The Ctl Bus In MST to NPL Convertor functions as follows:

- Receives

  Gate BI from the Tags In Generator (card A2K2).

  Ctl Bus In from the Ctl Bus In Reg (card A2F2).
- Converts Ctl Bus In MST voltage levels to Ctl Bus In NPL voltage levels.
- Gate BI gates the Ctl Bus In NPL voltage levels to storage control.

43 Dev Bus In and Ctl Bus In Parity Check (Card A2F2)

The Dev Bus In and the Ctl Bus In Parity Check functions as follows:

- Receives

  Dev Bus In from the Dev Bus In MST to NPL Convertor (card A2F2).

  Ctl Bus In from the Ctl Bus In Reg and Control (card A2F2).
- Checks

  Dev Bus In parity at the input to the Ctl Bus In Register (card A2F2).

  Ctl Bus In parity at the output of the Ctl Bus In Register (card A2F2).
- Sends Dev Bus In Par Chk Latched, or Ctl Bus In Par Chk Latched via the Error Bus to the following:

  Check Bit Register (card A2K2)

  Controller Error Indicator (card A2K2)

44 Attn/Sel Bus (1-of-8) Check (Card A2G2)

The Attn/Sel Bus (1-of-8) Check functions as follows:

- Receives the Attn/Sel Bus from the Attn/Sel Bus NPL to MST Convertor (card A2G2).
- Checks that only one Attn/Sel bit on the bus is active.
- Sends an error indication (Check 1-of-8) via the Error Bus to the following when more than one, or none, of the Attn/Sel bits are active:

  Controller Error Indicator (card A2K2)

  Check Bit Register (card A2K2)

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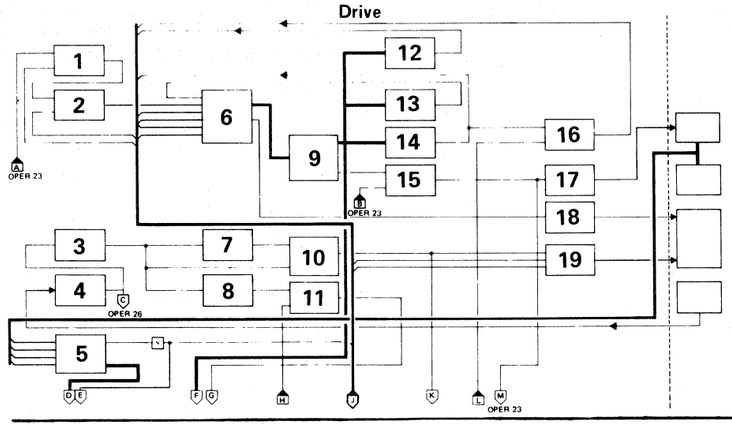
DRIVE

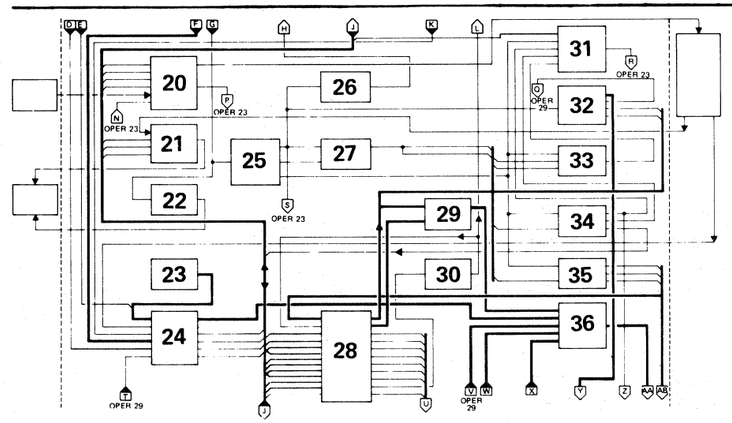
The following pages describe the functional units in the drive. The diagram on this page gives an overall view of the drive functional logic diagram. As indicated on the overall view, the diagram is contained on five pages: OPER 17, 20, 23, 26, and 29. Each of these pages is followed by pages explaining each functional unit as follows:

- The input, or inputs, to the functional unit and their source.
- The function of the functional unit.
- The output, or outputs, from the functional unit and their destination.



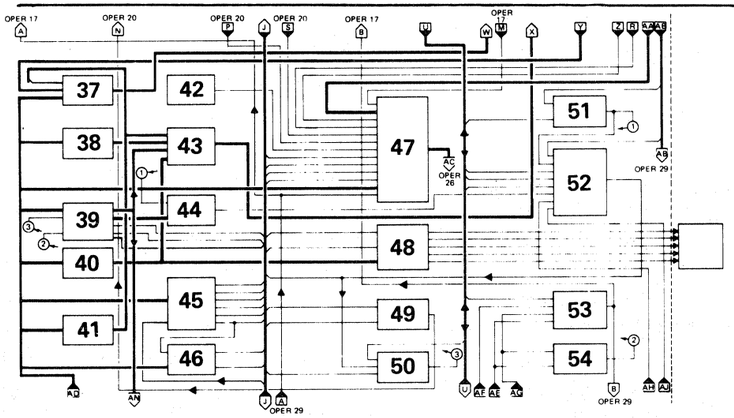
OPER 17

1. Inhibit HDA Sequence Generator (Card A1F2)
2. Stop Sequence Status Generator (Card A1F2)
3. Servo Clock Detector (Card A1C2)
4. Raw Servo Signal Amplifier (Card A1C2)
5. Drive Switches +24 V to MST Convertor (Card A1F2)
6. Bit Latches 1,2,4 (Card A1F2)
7. Access Control Timer Gate Generator (Card A1C2)
8. Incrementer (Card A1D4)
9. State Generator (Card A1F2)
10. Motor-at-Correct-Speed Detector (Card A1D4)
11. Voltage-Controlled Oscillator (Card A1C2)
12. Sequence Rezero Generator (Card A1F2)
13; 15 Second Delay Timer (Card A1F2)
14. Carriage Go Home Generator (Card A1E2)
15. Ready Lamp Driver (Card A1F2)
16. Go Home Complete Generator (Card A1E2)
17. Ready Lamp Driver (Card A1F2)
18. Drive Motor Run Relay Control (Card A1F2)
19. HDA Sequence Complete Relay Control (Card A1F2)



OPER 20

20. Write Data Gate (Card A1J2)
21. Read Data Detector (Card A1J2)
22. Read Servo Gate (Card A1H2)
23. Format Mode Jumpers (Card A1F2)
24. HDA Status Bits Generator (Card A1F2)
25. Servo Byte Counter (Card A1D4)
26. Decrementer (Card A1D4)
27. Index Shift Register (Card A1D4)
28. Access Control (Card A1E2)
29. Access Check Status Gate (Card A1E2)
30. Access Timeout Generator (Card A1C4)
31. Index Check (Card A1D4)
32. Sector Counter (Card A1J4)
33. Index Mark Generator (Card A1D4)
34. Valid Index Generator (Card A1D4)
35. Guardband Pattern Generator (Card A1D4)
36. MST Inbus Generator (Card A1H2)



OPER 23

37. Target Register (Card A1J4)
38. Cylinder Address Register (Card A1G2)
39. Difference Counter and Control (Card A1G2)
40. Head Address Register (Card A1G2)
41. Sense Operations Decode (Card A1G2)
42. Head Short Detector (Card A1G2)
43. HAR or CAR or Difference Counter Output Gate (Card A1G2)
44. Digital-to-Analog Convertor (Card A1D2)
45. Read Write Control (Card A1H2)
46. Write Gate Control (Card A1H2)
47. Inbus Generator (Card A1H2)
48. Movable/Fixed Heads Decoder (Card A1G2)
49. Select Write Current Generator (Card A1G2)
50. Allow Difference Counter Generator (Card A1E2)
51. Position Enable Generator (Card A1C4)
52. End of Acceleration Detector (Card A1C4)
53. Track Following Timer (Card A1C4)
54. Track Crossing Detector (Card A1D2)

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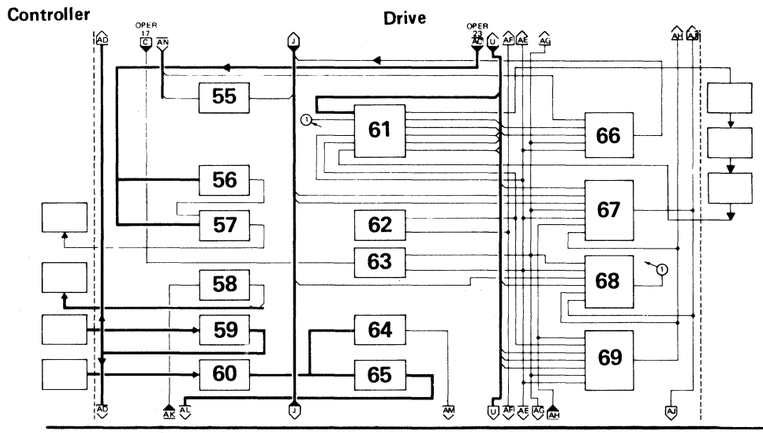
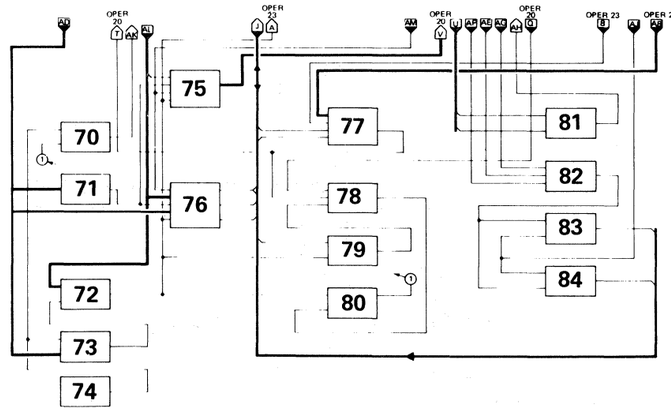
FUNCTIONAL UNITS

DRIVE



OPER 26

55. Even Track Detector (Card A1E2)
56. Inbus Parity Check (Card A1H2)
57. Inbus MST to NPL Convertor (Card A1H2)
58. Attn/Sel Bit MST to NPL Convertor (Card A1K2)
59. Dev Bus Out NPL to MST Convertor (Card A1K2)
60. Dev Tag Bus NPL to MST Convertor (Card A1K2)
61. Access Control Amplifier (Card A1C4)
62. +/−Error Demodulator and Amplifier (Card A1C2)
63. Dev Tag Bus Parity (Card A1K2)
64. Tag Decoder (Card A1K2)
65. Allow Rezero Generator (Card A1D2)
66. Allow Rezero Generator (Card A1D2)
67. Velocity Detector (Card A1D2)
68. Gated Position Derivative Generator (Card A1D2)
69. Access Current Magnitude Detector (Card A1D2)



OPER 29

70. Attention/Select Bit Generator (Card A1K2)
71. Dev Bus Out Parity (Card A1K2)
72. Drive Selected Generator (Card A1K2)
73. Drive Address Compare (Card A1K2)
74. Drive Logical Address Jumpers (Card A1K2)
75. Interface Status Bits Generator (Card A1K2)
76. Drive Operation Control (Card A1K2)
77. Access Complete Generator (Card A1E2)
78. Attention Generator (Card A1E2)
79. Access Busy Generator (Card A1E2)
80. Normal Attention Generator (Card A1K2)
81. Velocity Enable Generator (Card A1C4)
82. On Track Detector (Card A1C4)
83. Velocity Intensity Detector (Card A1C4)
84. End of Deceleration Detector (Card A1C4)

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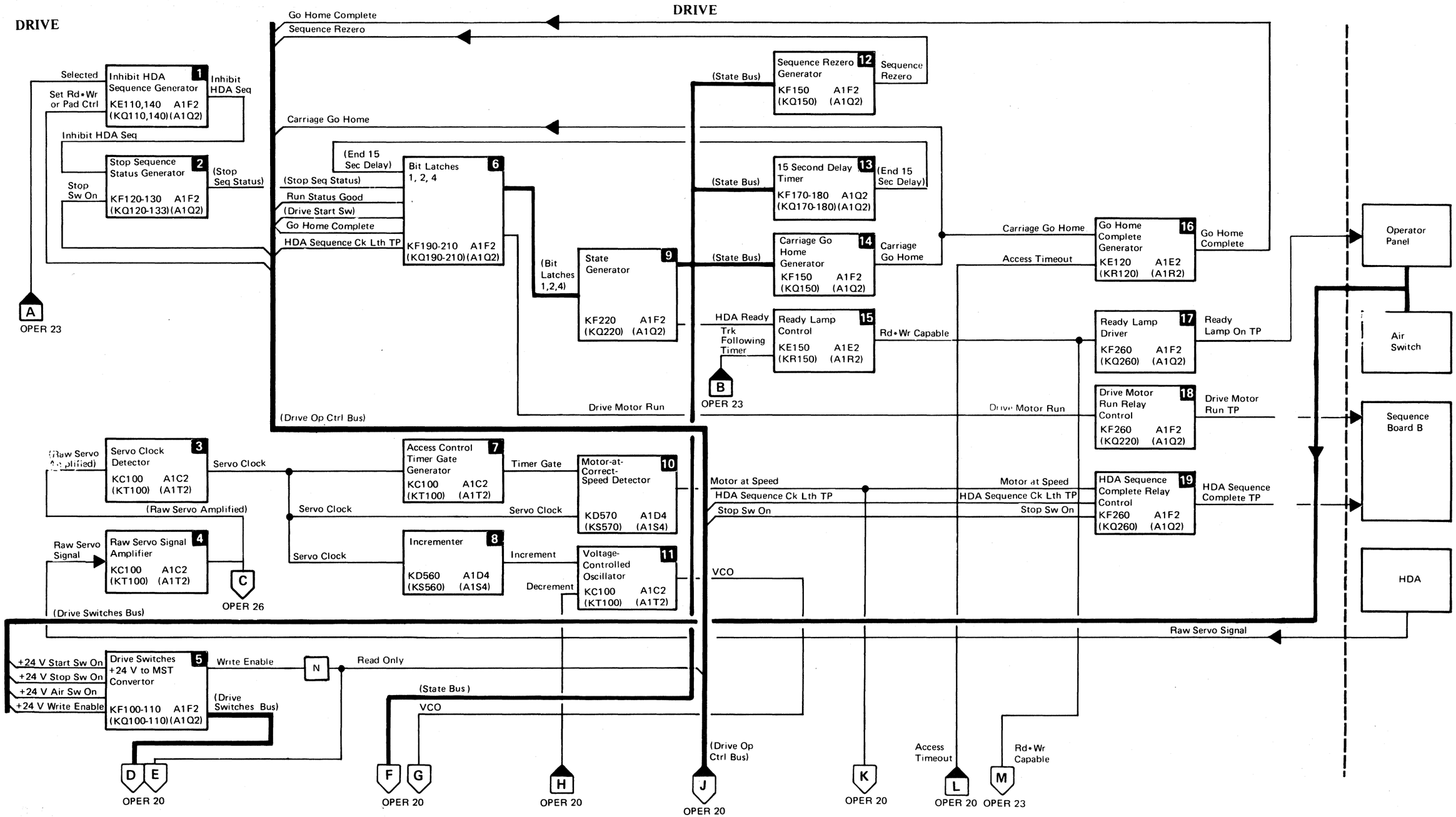
DRIVE



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FUNCTIONAL UNITS

DRIVE

1 Inhibit HDA Sequence Generator (Card A1F2)

The Inhibit HDA Sequence Generator functions as follows:

- Receives

  Selected from the Drive Selected Generator (card A1K2).

  Set Rd*Wr or Pad Ctrl via the Drive Op Ctrl Bus from the Read*Write Control (card A1H2).
- Generates the Inhibit HDA Seq signal.
- Sends Inhibit HDA Seq to the Stop Sequence Status Generator (card A1F2).

2 Stop Sequence Status Generator (Card A1F2)

The Stop Sequence Status Generator functions as follows:

- Receives

  Inhibit HDA Seq from the Inhibit Sequence Generator (card A1F2).

  Stop Sw On via the Drive Op Ctrl Bus from the HDA Status Bits Generator (card A1F2).
- Generates the Stop Seq Status signal.
- Sends Stop Seq Status to the Bit Latches 1, 2, 4 (card A1F2).

3 Servo Clock Detector (Card A1C2)

The Servo Clock Detector functions as follows:

- Receives Raw Servo Amplified from the Raw Servo Signal Amplifier (card A1C2).
- Detects the Servo Clock from Raw Servo Amplified.
- Sends Servo Clock to the following:

  Access Control Timer Gate Generator (card A1C2)

  Motor-at-Correct-Speed Detector (card A1D4)

  Incrementer (card A1D4)

4 Raw Servo Signal Amplifier (Card A1C2)

The Raw Servo Signal Amplifier functions as follows:

- Receives Raw Servo Signal from the HDA.
- Amplifies Raw Servo Signal and generates Raw Servo Amplified.
- Sends Raw Servo Amplified to the following:

  Servo Clock Detector (card A1C2)

  +/− Error Demodulator and Amplifier (card A1C2)

5 Drive Switches +24 V to MST Convertor (Card A1F2)

The Drive Switches +24 V to MST Convertor functions as follows:

- Receives drive switch signals via the Drive Switches Bus from the operator panel and the air switch.
- Converts drive switch +24 V voltage levels to MST voltage levels.
- Sends drive switch MST voltage levels via Read Only and the Drive Switches Bus to the HDA Status Bits Generator (card A1F2).
- Also sends Read Only via the Drive Op Ctrl Bus to the Inbus Generator (card A1H2).

6 Bit Latches 1, 2, 4 (Card A1F2)

The Bit Latches 1, 2, 4 block functions as follows:

- Receives

  End 15 Sec Delay from the 15 Second Delay Timer (card A1F2)

  Stop Seq Status from the Stop Sequence Status Generator (card A1F2)
- Also receives the following via the Drive Op Ctrl Bus:

  Run Status Good from the HDA Status Bits Generator (card A1F2).

  Drive Start Sw from the HDA Status Bits Generator (card A1F2).

  Go Home Complete from the Go Home Complete Generator (card A1E2).

  HDA Sequence Ck Lth TP from the HDA Status Bits Generator (card A1E2).
- Generates Bit Latches 1, 2, 4 and sends them to the State Generator (card A1F2).
- Generates Drive Motor Run and sends it to the Drive Motor Run Relay Control (card A1F2).

7 Access Control Timer Gate Generator (Card A1C2)

The Access Control Timer Gate Generator functions as follows:

- Receives Servo Clock from the Servo Clock Detector (card A1C2).
- Generates Timer Gate.
- Sends Timer Gate to the Motor-at-Correct-Speed Detector (card A1D4).

8 Incrementer (Card A1D4)

The Incrementer functions as follows:

- Receives Servo Clock from the Servo Clock Detector (card A1C2).
- Generates Increment.
- Sends Increment to the Voltage Controlled Oscillator (card A1C2).

9 State Generator (Card A1F2)

The State Generator functions as follows:

- Receives Bit Latches 1, 2, 4 from the Bit Latches 1, 2, 4 (card A1F2).
- Generates the State Bus and sends it to the following:

  Sequence Rezero Generator (card A1F2)

  15 Second Delay Timer (card A1F2)

  Carriage Go Home Generator (card A1F2)

  HDA Status Bits Generator (card A1F2)
- Generates HDA Ready and sends it to the Ready Lamp Control (card A1E2).

10 Motor-at-Correct-Speed Detector (Card A1D4)

The Motor-at-Correct-Speed Detector functions as follows:

- Receives

  Time Gate from the Access Control Timer Gate Generator (card A1C2)

  Servo Clock from the Servo Clock Detector (card A1C2)
- Generates Motor at Speed.
- Sends Motor at Speed to the following:

  HDA Sequence Complete Relay Control (card A1F2)

  HDA Status Bits Generator (card A1F2)

11 Voltage-Controlled Oscillator (Card A1C2)

The Voltage-Controlled Oscillator functions as follows:

- Receives

  Increment from the Incrementer (card A1D4)

  Decrement from the Decrementer (card A1D4)
- Generates the VCO signal.
- Sends VCO to the following:

  Servo Byte Counter (card A1D4)

  Read Servo Gate (card A1H2)

12 Sequence Rezero Generator (Card A1F2)

The Sequence Rezero Generator functions as follows:

- Receives the State Bus from the State Generator (card A1F2).
- Generates Sequence Rezero.
- Sends Sequence Rezero via the Drive Op Ctrl Bus to the Access Control (card A1E2).

13 15 Second Delay Timer (Card A1F2)

The 15 Second Delay Timer functions as follows:

- Receives the State Bus from the State Generator (card A1F2).
- Generates End 15 Sec Delay.
- Sends End 15 Sec Delay to the Bit Latches 1, 2, 4 (card A1F2).

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14 Carriage Go Home Generator (Card A1F2)

The Carriage Go Home Generator functions as follows:

- Receives the State Bus from the State Generator (card A1F2).
- Generates Carriage Go Home.
- Sends Carriage Go Home to the following:

  Go Home Complete Generator (card A1E2)

  Access Control (card A1E2) via the Drive Op Ctrl Bus.

15 Ready Lamp Control (Card A1E2)

The Ready Lamp Control functions as follows:

- Receives

  HDA Ready from the State Generator (card A1F2).

  Trk Following Timer from the Track Following Timer (card A1C4)

- Generates Rd*Wr Capable.
- Sends Rd*Wr Capable to the following:

  Ready Lamp Driver (card A1F2)

  Inbus Generator (card A1H2)

16 Go Home Complete Generator (Card A1E2)

The Go Home Complete Generator functions as follows:

- Receives

  Carriage Go Home from the Carriage Go Home Generator (card A1F2).

  Access Timeout from the Access Timeout Generator (card A1C4).

- Generates Go Home Complete.
- Sends Go Home Complete via the Drive Op Ctrl Bus to the Bit Latches 1, 2, 4 (card A1F2).

17 Ready Lamp Driver (Card A1F2)

The Ready Lamp Driver functions as follows:

- Receives Rd*Wr Capable from the Ready Lamp Control (card A1E2).
- Generates and amplifies Ready Lamp On TP.
- Sends Ready Lamp On TP to the Ready Lamp on the Operator Panel.

18 Drive Motor Run Relay Control (Card A1F2)

The Drive Motor Run Relay Control functions as follows:

- Receives Drive Motor Run from the Bit Latches 1, 2, 4 (card A1F2).
- Generates and amplifies Drive Motor Run TP.
- Sends Drive Motor Run TP to the Drive Motor Run Relay on the Sequence Board B.

19 HDA Sequence Complete Relay Control (Card A1F2)

The HDA Sequence Complete Relay Control functions as follows:

- Receives

  Motor at Speed from the Motor-at-Correct-Speed Detector (card A1D4).

  HDA Sequence Chk Lth TP via the Drive Op Ctrl Bus from the HDA Status Bits Generator (card A1F2).

  Stop Sw On via the Drive Op Ctrl Bus from the HDA Status Bits Generator (card A1F2).

- Generates and amplifies HDA Sequence Complete TP.
- Sends HDA Sequence Complete TP to the HDA Sequence Complete Relay on the Sequence Board B

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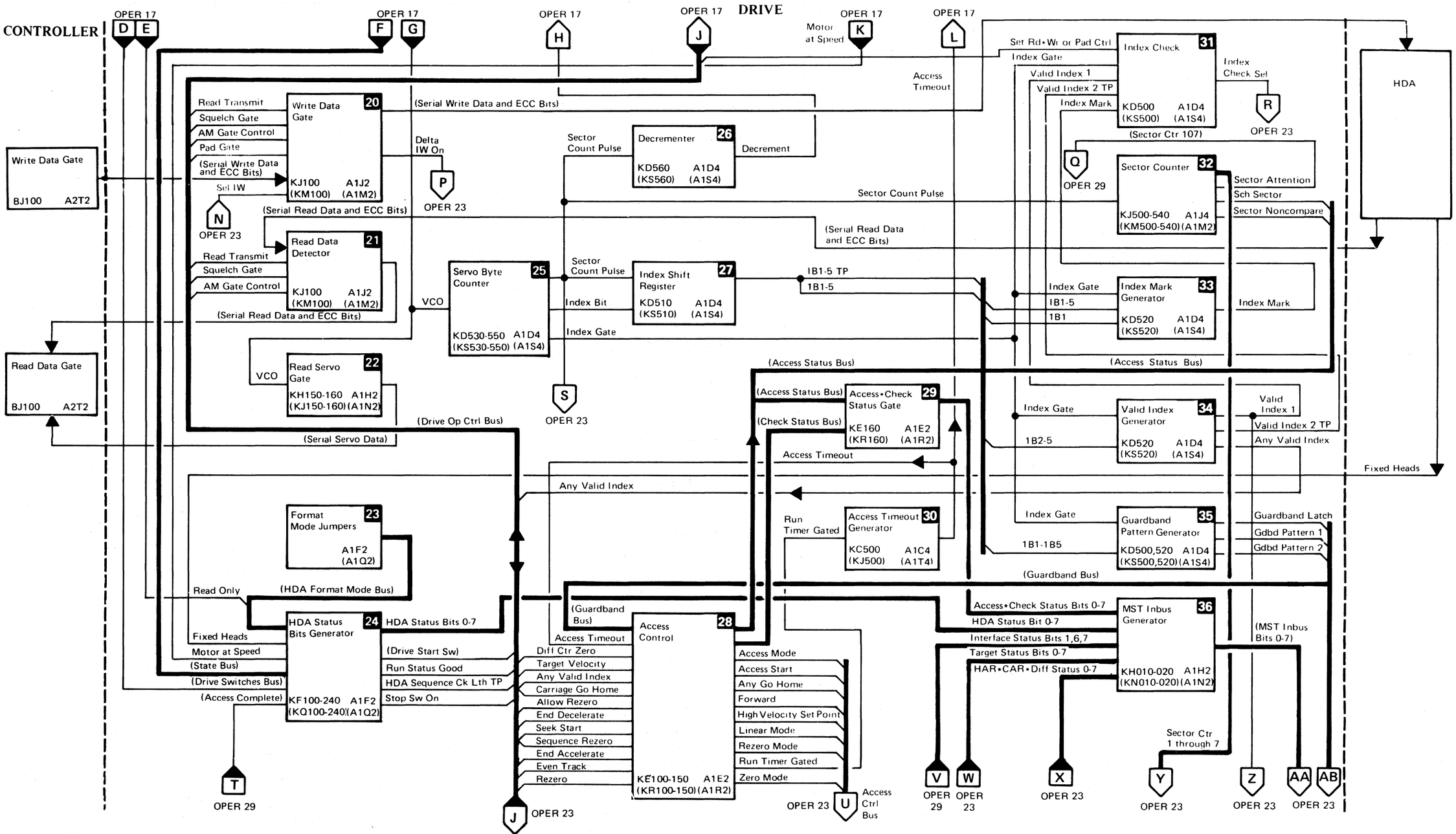

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FUNCTIONAL UNITS

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20 Write Data Gate (Card A1J2)

The Write Data Gate functions as follows:

- Receives the following via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2):

  Read Transmit

  Squelch Gate

  AM Gate Control

  Pad Gate

- Also receives:

  Serial Write Data and ECC Bits from the Write Data Gate (card A2T2) in the controller.

  Sel IW from the Select Write Current Generator (card A1G2).

- Gates Serial Write Data and ECC Bits to the HDA.
- Generates Delta IW On and sends it to the Inbus Generator (card A1H2).

21 Read Data Detector (Card A1J2)

The Read Data Detector functions as follows:

- Receives

  Serial Read Data and ECC Bits from the HDA.

  Read Transmit via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).

  Squelch Gate via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).

  AM Gate Control via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).

- Detects the Serial Read Data and ECC Bits from the HDA.
- Sends Serial Read Data and ECC Bits to the Read Data Gate (card A2T2) in the controller.

22 Read Servo Gate (Card A1H2)

The Read Servo Gate functions as follows:

- Receives the VCO signal from the Voltage-Controlled Oscillator (card A1C2).
- Sends VCO as Serial Servo Data to the Read Data Gate (card A2T2) in the controller.

23 Format Mode Jumpers (Card A1F2)

The Format Mode Jumpers block functions as follows:

- Generates one of the following:

  Native Fmt Mode

  3330–1 Fmt Mode

  3330–11 Fmt Mode

- Sends Native Fmt Mode, 3330–1 Fmt Mode, or 3330–11 Fmt Mode via the Format Mode Bus to the HDA Status Bits Generator (card A1F2).

24 HDA Status Bits Generator (Card A1F2)

The HDA Status Bits Generator functions as follows:

- Receives

  HDA Format Mode Bus from the Format Mode Jumpers (card A1F2).

  Fixed Heads from the HDA.

  Motor at Speed from the Motor-at-Correct-Speed Detector (card A1D4).

  State Bus from the State Generator (card A1F2)

  Drive Switches Bus from the Drive Switches +24 V to MST Convertor (card A1F2).

  Access Complete from the Access Complete Generator (card A1E2)

- Generates HDA Status Bits 0 through 7 and sends them to the MST Inbus Generator (card A1H2).
- Generates Drive Start Sw and sends it via the Drive Op Ctrl Bus to the Bit Latches 1, 2, 4 (card A1F2).
- Generates Run Status Good and sends it via the Drive Op Ctrl Bus to the Bit Latches 1, 2, 4 (card A1F2).
- Generates HDA Sequence Ck Lth TP and sends it via the Drive Op Ctrl Bus to the following:

  HDA Sequence Complete Relay Control (card A1F2)

  Bit Latches 1, 2, 4 (card A1F2)

- Generates Stop Sw On and sends it via the Drive Op Ctrl Bus to the following:

  HDA Sequence Complete Relay Control (card A1F2)

  Stop Sequence Status Generator (card A1F2)

25 Servo Byte Counter (Card A1D4)

The Servo Byte Counter functions as follows:

- Receives the VCO signal from the Voltage-Controlled Oscillator (card A1C2).
- Generates Sector Count Pulse each time a certain number of VCO pulses are counted.
- Sends Sector Count Pulse to the following:

  Decrementer (card A1D4)

  Sector Counter (card A1J4)

  Index Shift Register (card A1D4)

  Inbus Generator (card A1H2)

- Generates Index Bit and sends it to the Index Shift Register (card A1D4).
- Generates Index Gate and sends it to the following:

  Index Check (card A1D4)
  Index Mark Generator (card A1D4)

  Valid Index Generator (card A1D4)

  Guardband Pattern Generator (card A1D4)

26 Decrementer (Card A1D4)

The Decrementer functions as follows:

- Receives Sector Count Pulse from the Servo Byte Counter (card A1D4).
- Generates Decrement.
- Sends Decrement to the Voltage-Controlled Oscillator (card A1C2).

27 Index Shift Register (Card A1D4)

The Index Shift Register functions as follows:

- Receives

  Sector Count Pulse from the Servo Byte Counter (card A1D4).

  Index Bit from the Servo Byte Counter (card A1D4).

- Generates IB1 through 5 TP and also 1B1 through 5.
- Sends IB1 through 5 TP and also 1B1 through 5 via the Index Shift Bus to the following:

  Index Mark Generator (card A1D4)

  Valid Index Generator (card A1D4)

  Guardband Pattern Generator (card A1D4)

28 Access Control (Card A1E2)

The Access Control functions as follows:

- Receives

  The Guardband Bus from the Guardband Pattern Generator (Card A1C4).

  The Access Timeout signal from the Access Timeout Generator (card A1C4).

- Also receives the following control signals via the Drive Op Ctrl Bus:

  Diff Ctr Zero from the Difference Counter and Control (card A1G2).

  Target Velocity from the Velocity Intensity Generator (card A1C4).

  Any Valid Index from the Valid Index Generator (card A1D4).

  Carriage Go Home from the Carriage Go Home Generator (card A1F2).

  Allow Rezero from the Allow Rezero Generator (card A1D2).

  End Decelerate from the End of Deceleration Detector (card A1C4).

  Seek Start from the Drive Operation Control (card A1K2).

  Sequence Rezero from the State Generator (card A1F2).

  End Accelerate from the End of Acceleration Detector (card A1C4).

  Even Track from the Even Track Detector (card A1E2).

  Rezero from the Drive Operation Control (card A1K2).

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FUNCTIONAL UNITS

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- Generates Access Mode and sends it via the Access Ctrl Bus to the following:
  - End of Acceleration Detector (card A1C4)
  - Allow Difference Counter Generator (card A1E2)
  - Access Control Amplifier (card A1C4)
  - Velocity Detector (card A1D2)
- Generates Access Start and sends it via the Access Ctrl Bus to the Allow Rezero Generator (card A1D2).
- Generates Any Go Home and sends it via the Access Ctrl Bus to the following:
  - Access Control Amplifier (card A1C4)
  - Velocity Enable Generator (card A1C4)
- Generates the Forward signal and sends it via the Access Ctrl Bus to the following:
  - Access Control Amplifier (card A1C4)
  - Allow Rezero Generator (card A1D2)
- Generates High Velocity Set Point and sends it via the Access Ctrl Bus to the End of Acceleration Detector (card A1C4).
- Generates Linear Mode and sends it via the Access Ctrl Bus to the following:
  - Access Control Amplifier (card A1C4)
  - Track Following Timer (card A1C4)
- Generates Rezero Mode and sends it via the Access Ctrl Bus to the Access Control Amplifier (card A1C4).
- Generates Run Timer Gated and sends it to the Access Timeout Generator (card A1C4).
- Generates Zero Mode and sends it via the Access Ctrl Bus to the following:
  - Access Control Amplifier (card A1C4)
  - Velocity Enable Generator (card A1C4)

29 Access Check Status Gate (Card A1E2)

The Access*Check Status Gate functions as follows:

- Receives Access Status Bus from the following:
  - Access Control (card A1E2)
  - Sector Counter (card A1J4)
- Receives Check Status Bus from the Access Control (card A1E2)
- Gates the Access*Check Status Bits 0–7 to the MST Inbus Generator (card A1H2).

30 Access Timeout Generator (Card A1C4)

The Access Timeout Generator functions as follows:

- Receives Run Timer Gated from the Access Control (card A1E2).
- Generates Access Timeout.
- Sends Access Timeout to the following:
  - Access Control (card A1E2)
  - Go Home Complete Generator (card A1F2)

31 Index Check (Card A1D4)

The Index Check functions as follows:

- Receives
  - Set Rd*Wr or Pad Ctrl via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).
  - Index Gate from the Servo Byte Counter (card A1D4).
  - Valid Index 1 from the Valid Index Generator (card A1D4).
  - Valid Index 2 TP from the Valid Index Generator (card A1D4).
  - Index Mark from the Index Mark Generator (card A1D4).
- Generates Index Check Sel.
- Sends Index Check Sel to the Inbus Generator (card A1H2).

32 Sector Counter (Card A1J4)

The Sector Counter functions as follows:

- Receives Sector Count Pulse from the Servo Byte Counter (card A1D4).
- Counts sector count pulses and generates Sector Ctr 1 through 7.
- Sends Sector Ctr 1 through 7 to the Target Register (card A1J4).

The Sector Counter also:

- Generates Sector Attention and sends it to the Attention Generator (card A1E4).
- Generates Sch Sector and sends it via the Access Status Bus to the Access*Check Status Gate (card A1E2).
- Generates Sector Noncompare and sends it via the Access Status Bus to the Access*Check Status Gate (card A1E2).

33 Index Mark Generator (Card A1D4)

The Index Mark Generator functions as follows:

- Receives
  - Index Gate from the Servo Byte Counter (card A1D4).
  - IB1 through 5 from the Index Shift Register (card A1D4).
  - 1B1 from the Index Shift Register (card A1D4).
- Generates Index Mark when the Index Shift Register (card A1D4) is full.
- Sends Index Mark to the Index Check (card A1D4).

34 Valid Index Generator (Card A1D4)

The Valid Index Generator functions as follows:

- Receives
  - Index Gate from the Servo Byte Counter (card A1D4).
  - 1B2 through 5 from the Index Shift Register (card A1D4).
- Generates Valid Index 1 and sends it to the Index Check (card A1D4).
- Generates Valid Index 2 TP and sends it to the Index Check (card A1D4).
- Generates Any Index Valid and sends it via the Drive Op Ctrl Bus to the following:
  - Allow Difference Counter Generator (card A1E2)
  - Access Complete Generator (card A1E2)

35 Guardband Pattern Generator (Card A1D4)

The Guardband Pattern Generator functions as follows:

- Receives
  - Index Gate from the Servo Byte Counter (card A1D4).
  - 1B1 through 5 from the Index Shift Register (card A1D4).
- Generates
  - Guardband Latch
  - Guardband Pattern 1
  - Guardband Pattern 2
- Sends the generated signals via the Guardband Bus to the following:
  - Access Control (card A1E2)
  - Position Enable Generator (card A1C4)
  - End of Acceleration Detector (card A1C4)
  - Access Complete Generator (card A1E2)

36 MST Inbus Generator (Card A1H2)

The MST Inbus Generator functions as follows:

- Receives
  - Access*Check Status Bits 0 through 7 from the Access*Check Status Gate (card A1E2).
  - HDA Status Bits 0 through 7 from the HDA Status Bits Generator (card A1F2).
  - Interface Status Bits 1, 6, 7 from the Interface Status Bits Generator (card A1K2).
  - Target Status Bits 0 through 7 from the Target Register (card A1J4).
  - HAR*CAR*Diff Status 0 through 7 from the HAR or CAR or Difference Counter Output Gate (card A1G2).
- Sends the HDA Status Bits, the Access*Check Status Bits, the Interface Status Bits, the Target Status Bits, or the HAR*CAR*Diff Status via the MST Inbus Bits 0 through 7 to the Inbus Generator (card A1H2).

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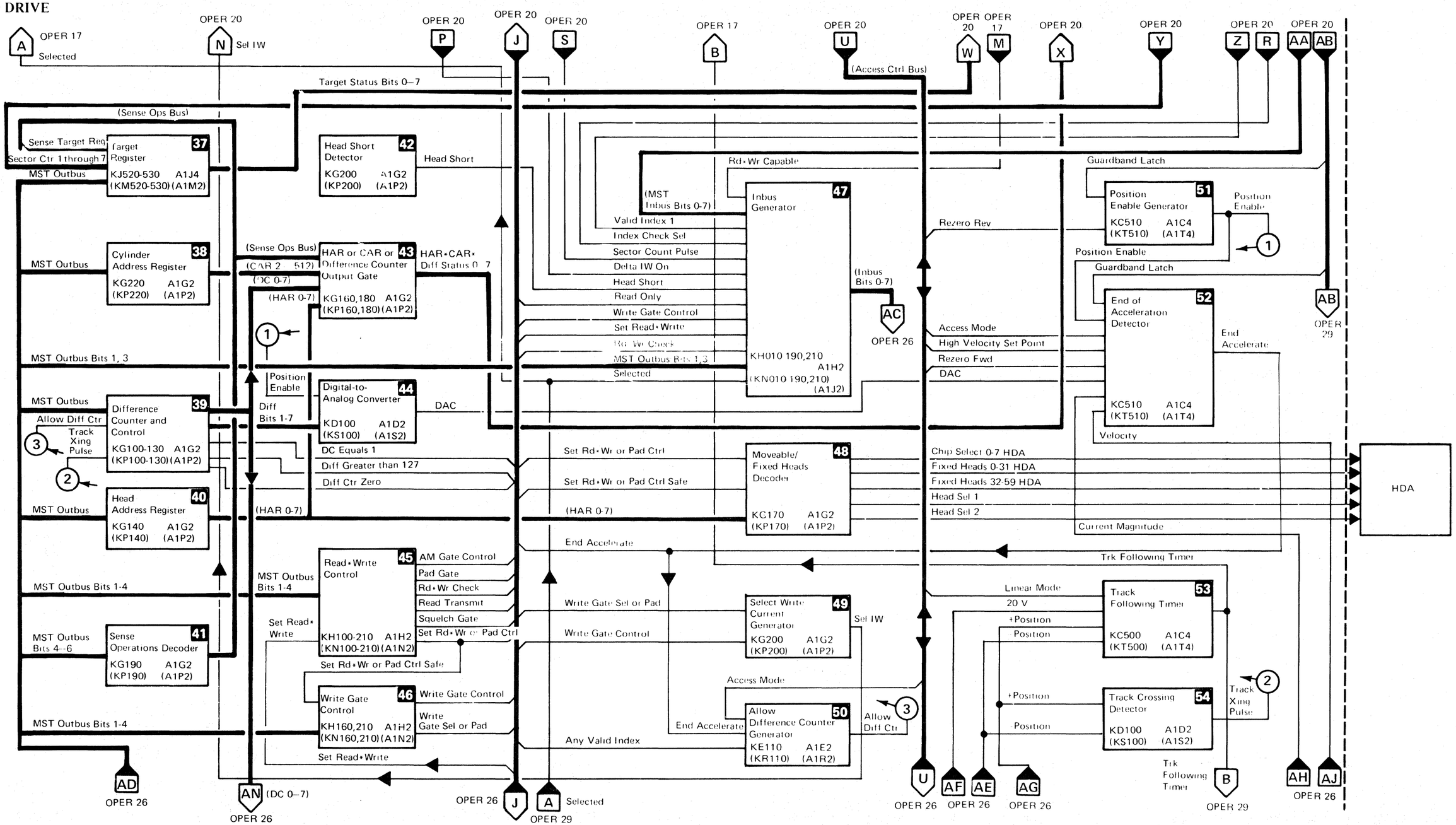
DRIVE



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FUNCTIONAL UNITS

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37 Target Register (Card A1J4)

The Target Register functions as follows:

- Receives

  Sense Target Reg via the Sense Ops Bus from the Sense Operations Decoder (card A1G2).

  Sector Ctr 1 through 7 from the Sector Counter (card A1J4).

  MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).

- Generates Target Status Bits 0 through 7.
- Sends the Target Status Bits 0 through 7 to the MST Inbus Generator (card A1H2).

38 Cylinder Address Register (Card A1G2)

The Cylinder Address Register functions as follows:

- Receives the MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).
- Generates CAR 2 through 512.
- Sends CAR 2 through 512 to the HAR or CAR or Difference Counter Output Gate (card A1G2).

39 Difference Counter and Control (Card A1G2)

The Difference Counter and Control functions as follows:

- Receives

  MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).

  Allow Diff Ctr from the Allow Difference Counter Generator (card A1E2).

  Track Xing Pulse from the Track Crossing Detector (card A1D2).

- Generates DC 0 through 7 and sends them to the HAR or CAR or Difference Counter Output Gate (card A1G2).
- Also sends DC 7 via DC 0 through 7 to the following:

  Even Track Detector (card A1E2)

  Allow Rezero Generator (card A1D2)

- Generates Diff Bits 1 through 7 and sends them to the Digital-to-Analog Convertor (card A1D2).
- Generates DC equals 1 and sends it via the Drive Op Ctrl Bus to the following:

  Velocity Detector (card A1D2)

  Gated Positive Derivative Generator (card A1D2)

- Generates Diff Greater than 127 and sends it via the Drive Op Ctrl Bus to the Velocity Detector (card A1D2).
- Generates Diff Ctr Zero and sends it via the Drive Op Ctrl Bus to the Access Control (card A1E2).

40 Head Address Register (Card A1G2)

The Head Address Register (HAR) functions as follows:

- Receives the MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).
- Generates HAR 0 through 7.
- Sends HAR 0 through 7 to the following:

  HAR or CAR or Difference Counter Output Gate (card A1G2).

  Movable/Fixed Heads Decoder (card A1G2).

41 Sense Operations Decoder (Card A1G2)

The Sense Operations Decoder functions as follows:

- Receives MST Outbus Bits 4 through 6 from the Dev Bus Out NPL to MST Convertor (card A1K2).
- Decodes MST Outbus Bits 4 through 6 into Sense Ops Bus.
- Sends Sense Ops Bus to the following:

  HAR or CAR or Difference Counter Output Gate (card A1G2)

  Target Register (card A1J4)

42 Head Short Detector (Card A1G2)

The Head Short Detector functions as follows:

- Generates the signal Head Short when more than one head is detected On during a Write operation.
- Sends Head Short to the Inbus Generator (card A1H2).

43 HAR or CAR or Difference Counter Output Gate (Card A1G2)

The HAR or CAR or Difference Counter Output Gate functions as follows:

- Receives

  Sense Ops Bus from the Sense Operations Decoder (card A1G2).

  CAR 2 through 512 from the Cylinder Address Register (CAR) (card A1G2).

  DC 0 through 7 from the Difference Counter and Control (card A1G2).

  HAR 0 through 7 from the Head Address Register (HAR) (card A1G2).

- Gates CAR 2 through 512, DC 0 through 7, or HAR 0 through 7 to the MST Inbus Generator (card A1H2).

44 Digital-to-Analog Convertor (Card A1D2)

The Digital-to-Analog Convertor functions as follows:

- Receives

  Position Enable from the Position Enable Generator (card A1C4).

  Diff Bits 1 through 7 from the Difference Counter and Control (card A1G2).

- Converts the Diff Bits 1 through 7 digital inputs into the DAC analog output.
- Sends DAC to the End of Acceleration Detector (card A1C4).

45 Read*Write Control (Card A1H2)

The Read*Write Control functions as follows:

- Receives

  MST Outbus Bits 1 through 4 from the Dev Bus Out NPL to MST Convertor (card A1K2).

  Set Read*Write via the Drive Op Ctrl Bus from the Drive Operation Control (card A1K2).

- Generates AM Gate Control and sends it via the Drive Op Ctrl Bus to the Read Data Detector (card A1J2).
- Generates Pad Gate and sends it via the Drive Op Ctrl Bus to the Write Data Gate (card A1J2).
- Generates Rd*Wr Check and sends it via the Drive Op Ctrl Bus to the Inbus Generator (card A1H2).
- Generates Read Transmit and sends it via the Drive Op Ctrl Bus to the following:

  Read Data Detector (card A1J2)

  Write Data Gate (card A1J2)

- Generates Squelch Gate and sends it via the Drive Op Ctrl Bus to the following:

  Read Data Detector (card A1J2)

  Write Data Gate (card A1J2)

- Generates Set Rd*Wr or Pad Ctrl and sends it via the Drive Op Ctrl Bus to the following:

  Movable/Fixed Heads Decoder (card A1G2)

  Index Check (card A1D4)

  Inhibit HDA Sequence Generator (card A1F2)

- Generates Set Rd*Wr or Pad Ctrl Safe and sends it to the Write Gate Control (card A1H2) and via the Drive Op Ctrl Bus to the Movable/Fixed Heads Decoder (card A1G2).

46 Write Gate Control (Card A1H2)

The Write Gate Control functions as follows:

- Receives

  Set Rd*Wr or Pad Ctrl Safe from the Read/Write Control (card A1H2).

  MST Outbus Bits 1 through 4 from the Dev Bus Out NPL to the MST Convertor (card A1K2).

- Generates Write Gate Control and sends it via the Drive Op Ctrl Bus to the following:

  Select Write Current Generator (card A1G2)

  Inbus Generator (card A1H2)

- Generates Write Gate Sel or Pad and sends it via the Drive Op Ctrl Bus to the Select Write Current Generator (card A1G2).

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FUNCTIONAL UNITS

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47 Inbus Generator (Card A1H2)

The Inbus Generator functions as follows:

- Receives

  Rd*Wr Capable from the Ready Lamp Control (card A1E2).

  MST Inbus Bits 0 through 7 from the MST Inbus Generator (card A1H2).

  Valid Index 1 from the Valid Index Generator (card A1D4).

  Index Check Sel from the Index Check (card A1D4).

  Sector Count Pulse from the Servo Byte Counter (card A1D4).

  Delta IW On from the Write Data Gate (card A1J2).

  Head Short from the Head Short Detector (card A1G2).

  Read Only via the Drive Op Ctrl Bus from the Drive Switches +24 V to MST Convertor (card A1F2).

  Write Gate Control via the Drive Op Ctrl Bus from the Write Gate Control (card A1H2).

  Set Read*Write via the Drive Op Ctrl Bus from the Drive Operations Control (card A1K2).

  Rd*Wr Check via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).

  MST Outbus Bits 1, 3 via the MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).

  The signal, Selected, from the Drive Selected Generator (card A1K2).

- Generates Inbus Bits 0 through 7.
- Sends Inbus Bits 0 through 7 to the following:

  Inbus Parity Check (card A1H2)

  Inbus MST to NPL Convertor (card A1H2)

48 Movable/Fixed Heads Decoder (Card A1G2)

The Movable/Fixed Heads Decoder functions as follows:

- Receives

  Set Rd*Wr or Pad Ctrl via the Drive Op Ctrl Bus from the Read*Write Control (card A1H2).

  Set Rd*Wr or Pad Ctrl via the Drive Op Ctrl Bus from the Read*Write Control (card A1H2).

  HAR 0 through 7 from the Head Address Register (HAR) (card A1G2).

- Generates the following and sends them to the HDA:

  Chip Select 0 through 7 HDA

  Fixed Heads 0 through 31 HDA

  Fixed Heads 32 through 59 HDA

  Head Sel 1

  Head Sel 2

49 Select Write Current Generator (Card A1G2)

The Select Write Current Generator functions as follows:

- Receives the following via the Drive Op Ctrl Bus from the Write Gate Control (card A1H2)

  Write Gate Sel or Pad

  Write Gate Control

- Generates Sel IW.
- Sends Sel IW to the Write Data Gate (card A1J2).

50 Allow Difference Counter Generator (Card A1E2)

The Allow Difference Counter Generator functions as follows:

- Receives

  Access Mode via the Access Ctrl Bus from the Access Control (card A1E2).

  End Accelerate from the End of Acceleration Detector (card A1C4).

  Any Valid Index via the Drive Op Ctrl Bus from the Valid Index Generator (card A1D4).

- Generates the Allow Diff Ctr signal.
- Sends Allow Diff Ctr to the Difference Counter and Control (card A1G2).

51 Position Enable Generator (Card A1C4)

The Position Enable Generator functions as follows:

- Receives

  Guardband Latch via the Guardband Bus from the Guardband Pattern Generator (card A1D4).

  Rezero Rev via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

- Generates Position Enable.
- Sends Position Enable to the following:

  End of Acceleration Detector (card A1C4)

  Digital-to-Analog Convertor (DAC) (card A1D2)

52 End of Acceleration Detector (Card A1C4)

The End of Acceleration Detector functions as follows:

- Receives

  Guardband Latch via the Guardband Bus from the Guardband Pattern Generator (card A1D4).

  Position Enable from the Position Enable Generator (card A1C4).

  Access Mode via the Access Ctrl Bus from the Access Control (card A1E2).

  High Velocity Set Point via the Access Ctrl Bus from the Access Control (card A1E2).

  Rezero Fwd via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

  DAC from the Digital-to-Analog Convertor (card A1D2).

  Current Magnitude from the Access Current Magnitude Detector (card A1D2).

  The Velocity signal from the Velocity Detector (card A1D2).

- Detects the end of acceleration of the carriage and generates End Accelerate.
- Sends End Accelerate to the Allow Difference Counter Generator (card A1E2) and also via the Drive Op Ctrl Bus to the Access Control (card A1C2).

53 Track Following Timer (Card A1C4)

The Track Following Timer functions as follows:

- Receives

  Linear Mode via the Access Ctrl Bus from the Access Control (card A1E2).

  20 V from the Reference Voltage Generator (card A1C2).

  + Position and also – Position from the +/– Error Demodulator and Amplifier (card A1C2).

- Generates the Track Following Timer signal.
- Sends Track Following Timer to the following:

  Ready Lamp Control (card A1E2)

  Access Complete Generator (card A1E2).

54 Track Crossing Detector (Card A1D2)

The Track Crossing Detector functions as follows:

- Receives + Position and also – Position from the +/– Error Demodulator and Amplifier (card A1C2).
- Generates Track Xing Pulse.
- Sends Track Xing Pulse to the Difference Counter and Control (card A1G2).

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DRIVE

CONTROLLER

OPER 23 AD MST Outbus

OPER 17 C

OPER 23 AN (DC 0–7)

OPER 23 J Drive Op Ctrl Bus

OPER 23 AC U

OPER 23 AF AE

OPER 23 AG

OPER 23 AH AJ

Allow Rezero

(Inbus Bits 0–7)

DC 7

55 Even Track Detector
KE150 A1E2
(KR150) (A1R2)
Even Track

(Access Ctrl Bus)
Gated Position
Derived
–Position
V Ref

61 Access Control Amplifier
KC500 A1C4
(KT500) (A1T4)
Power Amp Drive
Move Forward
Move Reverse
Rezero Fwd
Rezero Rev
Current Sense
Current Sense

(1)

DC 7
Access Start
Forward
+Position
–Position

66 Allow Rezero Generator
KD100 A1D2
KS(100) (A1S2)
Allow Rezero

Power Amp
(Same physical amp as shown below)

HDA

Power Amp
(Same physical amp as shown above)

(Inbus Bits 0-7)

56 Inbus Parity Check
KH190 A1H2
(KN190) (A1J2)
(Inbus Parity)

DC Equals 1
Diff Greater than 127

Access Mode
DC Equals 1
Diff Greater than 127
+Position
–Position
Velocity Enable

67 Velocity Detector
KD100 A1D2
(KS100) (A1S2)
Velocity
Current Magnitude

Dev Bus In NPL to MST Convertor
BR160 A2F2

(Inbus Bits 0-7)

57 Inbus MST to NPL Convertor
KH200 A1H2
(KJ200) (A1N2)
Dev Bus In

62 Reference Voltage Generator
KC100 A1C2
(KT100) (A1T2)
V Ref
20 V

63 +/– Error Demodulator and Amplifier
KC100 A1C2
(KT100) (A1T2)
+Position
–Position

(Raw Servo Amplified)

DC Equals 1

+Position
–Position
DC Equals 1
Move Forward

68 Gated Position Derivative Generator
KD100 A1D2
(KS100) (A1S2)
Gated Position Derived

(1)

Velocity
Current Magnitude

Attn/Sel Bus NPL to MST Convertor
BF160 A2G2

Attn/Sel Bit

58 Attn/Sel Bit MST to NPL Converter
KK120 A1K2
(KL120) (A1L2)
Attn/Sel Bit

Attn/Sel Bus

Bits Out to Dev Bus Out Convertor
BA110 A2F2

Dev Bus Out

59 Dev Bus Out NPL to MST Convertor
KK100-110 A1K2
(KL100-110) (A1L2)
MST Outbus

MST Outbus

Tag Bus

64 Dev Tag Bus Parity
KK120 A1K2
(KL120) (A1L2)
Tag Bus Parity Error

Velocity Enable
V Ref
Move Forward
Move Reverse
Current Sense
+Position
–Position

69 Access Current Magnitude Detector
KD100 A1D2
(KS100) (A1S2)
Current Magnitude

Dev Tag Bus MST to NPL Convertor
BD220 A2L2

Dev Tag Bus

60 Dev Tag Bus NPL to MST Convertor
KK100 A1K2
(KL100) (A1L2)
Tag Bus

Tag Bits 0 - 2

65 Tag Decoder
KK120 A1K2
(KL120) (A1L2)
(Tag Decodes)

Access Ctrl Bus

Velocity

OPER 29 AD MST Outbus

OPER 29 AK AL

OPER 29 Drive Op Ctrl Bus J

OPER 29 AM

OPER 29 AP AF AE AG AH

OPER 29 AJ

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DRIVE

55 Even Track Detector (Card A1E2)

The Even Track Detector functions as follows:

- Receives DC 7 via DC 0 through 7 from the Difference Counter and Control (card A1G2).
- Generates Even Track.
- Sends Even Track via the Drive Op Ctrl Bus to the Access Control (card A1E2).

56 Inbus Parity Check (Card A1H2)

The Inbus Parity Check functions as follows:

- Receives Inbus Bits 0 through 7 from the Inbus Generator (card A1H2).
- Generates the Inbus Parity signal when an even number of Inbus bits are active.
- Sends Inbus Parity to the Inbus MST to NPL Convertor (card A1H2).

57 Inbus MST to NPL Convertor (Card A1H2)

The Inbus MST to NPL Convertor functions as follows:

- Receives

  Inbus Parity from the Inbus Parity Check (card A1H2).

  Inbus Bits 0 through 7 from the Inbus Generator (card A1H2).
- Converts the Inbus MST voltage levels to Dev Bus In NPL voltage levels.
- Sends Dev Bus In to the Dev Bus In NPL to MST Convertor (card A2F2) in the controller.

58 Attn/Sel Bit MST to NPL Convertor (Card A1K2)

The Attn/Sel Bit MST to NPL Convertor functions as follows:

- Receives the Attn/Sel Bit from the Attention/Select Bit Generator (card A1K2).
- Converts the Attn/Sel Bit MST voltage level to an NPL voltage level.
- Sends the Attn/Sel Bit NPL voltage level via the Attn/Sel Bus to the Attn/Sel Bus NPL to MST Convertor (card A2G2) in the controller.

59 Dev Bus Out NPL to MST Convertor (Card A1K2)

The Dev Bus Out NPL to MST Convertor functions as follows:

- Receives Dev Bus Out from the Bits Out to Dev Bus Out Convertor (card A2F2) in the controller.
- Converts Dev Bus Out NPL voltage levels to MST Outbus MST voltage levels.
- Sends MST Outbus to the following:

  Write Gate Control (card A1H2)

  Sense Operations Decode (card A1G2)

  Read*Write Control (card A1H2)

  Head Address Register (card A1G2)

  Difference Counter and Control (card A1G2)

  Inbus Generator (card A1H2)

  Cylinder Address Register (card A1G2)

  Target Register (card A1J4)

  Dev Bus Out Parity (card A1K2)

  Drive Operation Control (card A1K2)

  Drive Address Compare (card A1K2)

60 Dev Tag Bus NPL to MST Convertor (Card A1K2)

The Dev Tag Bus NPL to MST Convertor functions as follows:

- Receives Dev Tag Bus from the Dev Tag Bus MST to NPL Convertor (card A2L2) in the controller.
- Converts Dev Tag Bus NPL voltage levels to Tag Bus MST voltage levels.
- Sends Tag Bus to the following:

  Dev Tag Bus Parity (card A1K2)

  Tag Decode (card A1K2)

61 Access Control Amplifier (Card A1C4)

The Access Control Amplifier functions as follows:

- Receives

  Access Ctrl Bus from the Access Control (card A1E2).

  Gated Position Derived from the Gated Position Derivative Generator (card A1D2).

  −Position from the +/− Error Demodulator and Amplifier (card A1C2).

  V Ref from the Reference Voltage Generator (card A1C2).

  Current Sense from the HDA via the Power Amp and sends Current Sense via the Access Ctrl Bus to the Access Current Magnitude Detector (card A1D2).
- Generates Power Amp Drive and sends it to the HDA via the Power Amp.
- Generates the signals Move Forward and Move Reverse and sends them via the Access Ctrl Bus to the Access Current Magnitude Detector (card A1D2).
- Generates Rezero Fwd and sends it via the Access Ctrl Bus to the End of Acceleration Detector (card A1C4).
- Generates Rezero Rev and sends it via the Access Ctrl Bus to the Position Enable Generator (card A1C4).

62 Reference Voltage Generator (Card A1C2)

The Reference Voltage Generator functions as follows:

- Generates the reference voltages V Ref and 20 V.
- Sends V Ref to the following:

  Access Control Amplifier (card A1C4)

  Access Current Magnitude Detector (card A1D2).
- Sends 20 V to the following:

  Track Following Timer (card A1C4)

  On Track Detector (card A1C4)

63 +/− Error Demodulator and Amplifier (Card A1C2)

The +/− Error Demodulator and Amplifier functions as follows:

- Receives the Raw Servo Amplified signal from the Raw Servo Signal Amplifier (card A1C2).
- Demodulates the Raw Signal Amplified signal and obtains the signal + Position and the signal −Position.
- Amplifies + Position and − Position and sends them to the following:

  Track Following Timer (card A1C4)

  Track Crossing Detector (card A1D2)

  Allow Rezero Generator (card A1D2)

  Velocity Detector (card A1D2)

  Gated Position Derivative Generator (card A1D2)

  Access Current Magnitude Detector (card A1D2)

  On Track Detector (card A1C4)
- Sends −Position to the Access Control Amplifier (card A1C4).

64 Dev Tag Bus Parity (Card A1K2)

The Dev Tag Bus Parity functions as follows:

- Receives Tag Bus from the Dev Tag Bus NPL to MST Convertor (card A1K2).
- Checks the parity of the Tag Bus.
- Generates Tag Bus Parity Error when Tag Bus parity is odd.
- Sends Tag Bus Parity Error to the following:

  Interface Status Bits Generator (card A1K2)

  Drive Operations Control (card A1K2)

65 Tag Decoder (Card A1K2)

The Tag Decoder functions as follows:

- Receives Tag Bits 0 through 2 via the Tag Bus from the Dev Tag Bus NPL to MST Convertor (card A1K2).
- Decodes Tag Bus into the Tag Decodes.
- Sends the Tag Decodes to the following:

  Interface Status Bits Generator (card A1K2)

  Drive Operations Control (card A1K2)

  Drive Selected Generator (card A1K2)

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FUNCTIONAL UNITS

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66 Allow Rezero Generator (Card A1D2)

The Allow Rezero Generator functions as follows:

- Receives

  DC 7 via DC 0 through 7 from the Difference Counter and Control (card A1G2).

  Access Start via the Access Ctrl Bus from the Access Control (card A1E2).

  Forward via the Access Ctrl Bus from the Access Control (card A1E2).

  + Position and also − Position from the +/− Error Demodulator and Amplifier (card A1C2).

- Generates Allow Rezero.
- Sends Allow Rezero via the Drive Op Ctrl Bus to the Access Control (card A1E2).

67 Velocity Detector (Card A1D2)

The Velocity Detector functions as follows:

- Receives

  Access Mode via the Access Ctrl Bus from the Access Control (card A1E2).

  DC Equals 1 and also Diff Greater than 127 via the Drive Op Ctrl Bus from the Difference Counter and Control (card A1G2).

  + Position and also − Position from the +/− Error Demodulator and Control (card A1C2).

  Velocity Enable from the Velocity Enable Generator (card A1C4).

  Current Magnitude from the Access Current Magnitude Detector (card A1D2).

- Generates the Velocity signal.
- Sends Velocity to the following:

  End of Acceleration Detector (card A1C4)

  Gated Position Derivative Generator (card A1D2)

  Velocity Intensity Detector (card A1C4)

  End of Deceleration Detector (card A1C4)

68 Gated Position Derivative Generator (Card A1D2)

The Gated Position Derivative Generator functions as follows:

- Receives

  + Position and also − Position from the +/− Error Demodulator and Amplifier (card A1C2).

  DC equals 1 via the Drive Op Ctrl Bus from the Difference Counter and Control (card A1G2).

  Move Forward via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

  Current Magnitude from the Access Current Magnitude Detector (card A1D2).

  The Velocity signal from the Velocity Detector (card A1D2).

- Generates Gated Position Derived.
- Sends Gated Position Derived to the Access Control Amplifier (card A1C4).

69 Access Current Magnitude Detector (Card A1D2)

The Access Current Magnitude Detector functions as follows:

- Receives

  Velocity Enable from the Velocity Enable Generator (card A1C4).

  V Ref from the Reference Voltage Generator (card A1C2).

  Move Forward and also Move Reverse via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

  Current Sense via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

  + Position and also − Position from the +/− Error Demodulator and Amplifier (card A1C2).

- Generates Current Magnitude
- Sends Current Magnitude to the following:

  Gated Position Derivative Generator (card A1D4)

  Velocity Detector (card A1D2)

  End of Acceleration Detector (card A1C4)

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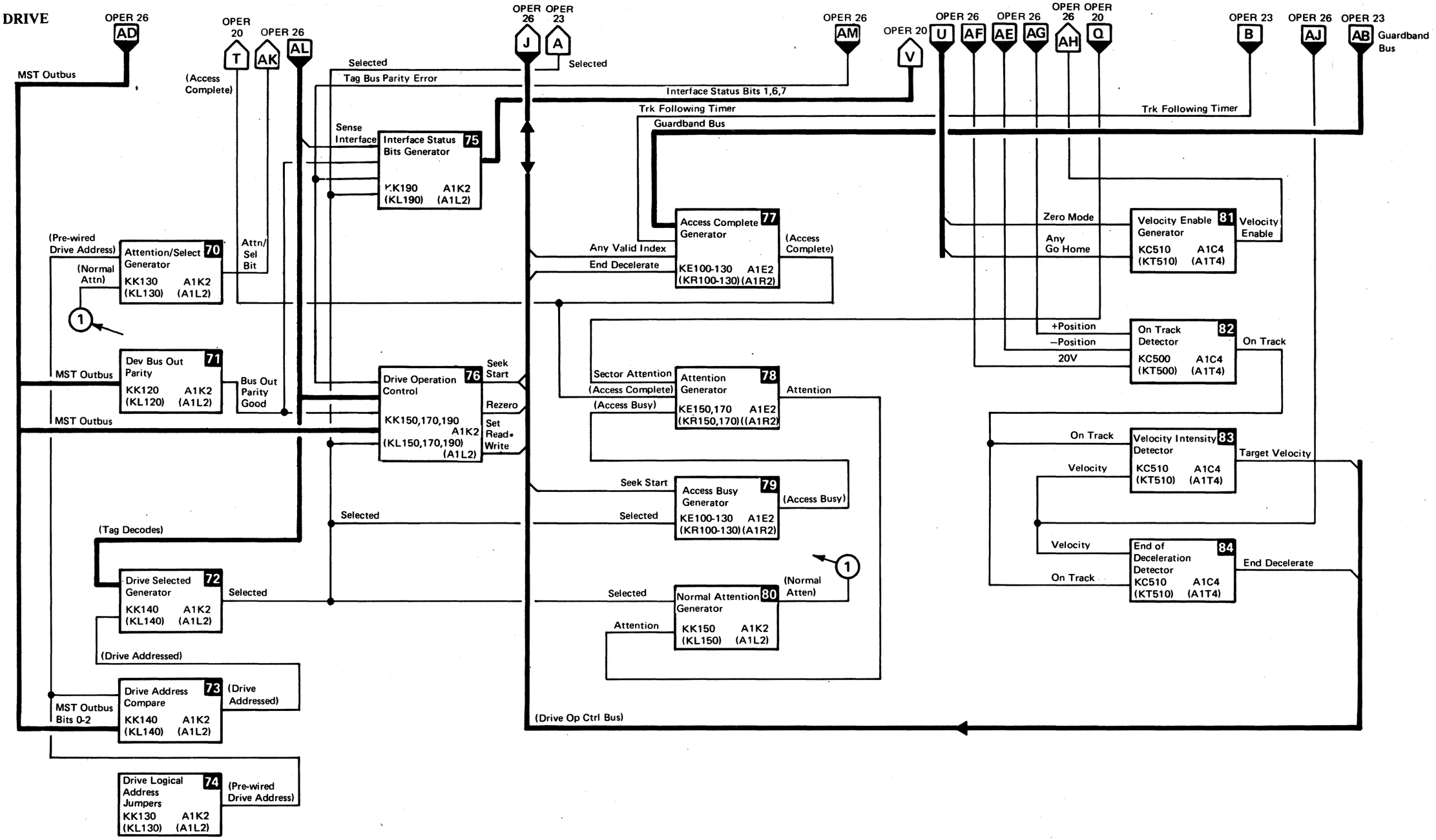
DRIVE



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FUNCTIONAL UNITS

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70 Attention/Select Bit Generator (Card A1K2)

The Attention/Select Bit Generator functions as follows:

- Receives

  Pre-wired Drive Address from the Drive Logical Address Jumpers (card A1K2)

  Normal Attn from the Normal Attention Generator (card A1K2).

- Generates Attn/Sel Bit.
- Sends Attn/Sel Bit to the Attn/Sel Bit MST to NPL Convertor (card A1K2).

71 Dev Bus Out Parity (Card A1K2)

The Dev Bus Out Parity functions as follows:

- Receives MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).
- Checks the parity of the MST Outbus.
- Generates Bus Out Parity Good when parity is odd.
- Sends Bus Out Parity Good to the following:

  Drive Operations Control (card A1K2)

  Interface Status Bits Generator (card A1K2)

72 Drive Selected Generator (Card A1K2)

The Drive Selected Generator functions as follows:

- Receives

  Tag Decodes from the Tag Decoder (card A1K2)

  Drive Addressed from the Drive Address Compare (card A1K2).

- Generates Selected.
- Sends Selected to the following:

  Normal Attention Generator (card A1K2)

  Access Busy Generator (card A1E2)

  Drive Operation Control (card A1K2)

  Interface Status Bits Generator (card A1K2)

  Inbus Generator (card A1H2)

  Inhibit HDA Sequence Generator (card A1F2)

73 Drive Address Compare (Card A1K2)

The Drive Address Compare functions as follows:

- Receives

  Prewired Drive Address from the Drive Logical Address Jumpers (card A1K2)

  MST Outbus Bits 0 through 2.

- Generates Drive Addressed when the address contained in the MST Outbus bits 0 through 2 equals the prewired drive address.
- Sends Drive Addressed to the Drive Selected Generator (card A1K2).

74 Drive Logical Address Jumpers (Card A1K2)

The Drive Logical Address Jumpers block functions as follows:

- Generates Prewired Drive Address.
- Sends Prewired Drive Address to the following:

  Drive Address Compare (card A1K2)

  Attention/Select Generator (card A1K2)

75 Interface Status Bits Generator (Card A1K2)

The Interface Status Bits Generator functions as follows:

- Receives

  Sense Interface via the Tag Decodes Bus from the Tag Decoder (card A1K2).

  Bus Out Parity Good from the Dev Bus Out Parity (card A1K2).

  Tag Bus Parity Error from the Dev Tag Bus Parity (card A1K2).

  Selected from the Drive Selected Generator (card A1K2).

- Generates Interface Status Bits 1, 6, 7.
- Sends Interface Status Bits 1, 6, 7 to the MST Inbus Generator (card A1H2).

76 Drive Operation Control (Card A1K2)

The Drive Operation Control functions as follows:

- Receives

  Tag Bus Parity Error from the Dev Tag Bus Parity (card A1K2).

  Tag Decodes from the Tag Decoder (card A1K2).

  Bus Out Parity Good from the Dev Bus Out Parity (card A1K2).

  MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).

  Selected from the Drive Selected Generated (card A1K2).

- Generates Seek Start and sends it via the Drive Op Ctrl Bus to the following:

  Access Busy Generator (card A1E2)

  Access Control (card A1E2)

- Generates Rezero and sends it via the Drive Op Ctrl Bus to the Access Control (card A1E2).
- Generates Set Read*Write and sends it via the Drive Op Ctrl Bus to the following:

  Read*Write Control (card A1H2)

  Inbus Generator (card A1H2)

77 Access Complete Generator (Card A1E2)

The Access Complete Generator functions as follows:

- Receives

  Guardband Bus from the Guardband Pattern Generator (card A1D4).

  Trk Following Timer from the Track Following Timer (card A1C4).

  Any Valid Index via the Drive Op Ctrl Bus from the Valid Index Generator (card A1D4).

  End Decelerate via the Drive Op Ctrl Bus from the End of Deceleration Detector (card A1C4).

- Generates Access Complete.
- Sends Access Complete to the following:

  Attention Generator (card A1E2)

  HDA Status Bits Generator (card A1F2)

78 Attention Generator (Card A1E2)

The Attention Generator functions as follows:

- Receives

  Sector Attention from the Sector Counter (card A1J4).

  Access Complete from the Access Complete Generator (card A1E2).

  Access Busy from the Access Busy Generator (card A1E2).

- Generates the Attention signal.
- Sends Attention to the Normal Attention Generator (card A1K2).

79 Access Busy Generator (Card A1E2)

The Access Busy Generator functions as follows:

- Receives

  Seek Start via the Drive Op Ctrl Bus from the Drive Operation Control (card A1K2).

  The signal, Selected, from the Drive Selected Generator (card A1K2).

- Generates Access Busy.
- Sends Access Busy to the Attention Generator (card A1E2).

80 Normal Attention Generator (Card A1K2)

The Normal Attention Generator functions as follows:

- Receives

  Selected from the Drive Selected Generator (card A1K2).

  Attention from the Attention Generator (card A1E2).

- Generates Normal Attn.
- Sends Normal Attn to the Attention/Select Bit Generator (card A1K2).

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FUNCTIONAL UNITS

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81 Velocity Enable Generator (Card A1C4)

The Velocity Enable Generator functions as follows:

- Receives Zero Mode and also Any Go Home via the Access Ctrl Bus from the Access Control (card A1E2).
- Generates Velocity Enable.
- Sends Velocity Enable to the following:

  Access Current Magnitude Detector (card A1D2)

  Velocity Detector (card A1D2)

82 On Track Detector (Card A1C4)

The On Track Detector functions as follows:

- Receives

  + Position and also − Position from the +/− Error Demodulator and Amplifier (card A1C2).

  20 V from the Reference Voltage Generator (card A1C2).

- Detects that the carriage is on track and then generates the On Track signal.
- Sends On Track to the following:

  Velocity Intensity Generator (card A1C4)

  End of Deceleration Detector (card A1C4)

83 Velocity Intensity Detector (Card A1C4)

The Velocity Intensity Detector functions as follows:

- Receives

  On Track from the On Track Detector (card A1C4).

  The Velocity signal from the Velocity Detector (card A1D2).

- Detects the velocity of the carriage and generates the Target Velocity signal.
- Sends the Target Velocity signal via the Drive Op Ctrl Bus to the Access Control (card A1E2).

84 End of Deceleration Detector (Card A1C4)

The End of Deceleration Detector functions as follows:

- Receives

  The Velocity signal from the Velocity Detector (card A1D2).

  On Track from the On Track Detector (card A1C4).

- Detects the end of deceleration of the carriage and then generates End Decelerate.
- Sends End Decelerate to the Access Control (card A1E2).

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HEAD/DISK ASSEMBLY

OPERATING MODES

The 3350 operates in one of three modes:

3350 Native Mode
3330-1 Mode
3330-11 Mode

3350 Native Mode

When the 3350 is operating in 3350 Native Mode, the logical cylinder and logical head addresses are directly related to the physical cylinders (or Access positions) and physical head addresses.

Examples:

Logical cylinder 0 is located at Access position 0; logical cylinder 75 is located at Access position 75.

Logical head address 0 is located at physical head 0; logical head address 23 is located at physical head 23.

3330-1 and 3330-11 Modes

These two modes have different logical cylinder and head addressing schemes. See OPER 40 for 3330-1 Mode and OPER 50 for 3330-11 Mode.

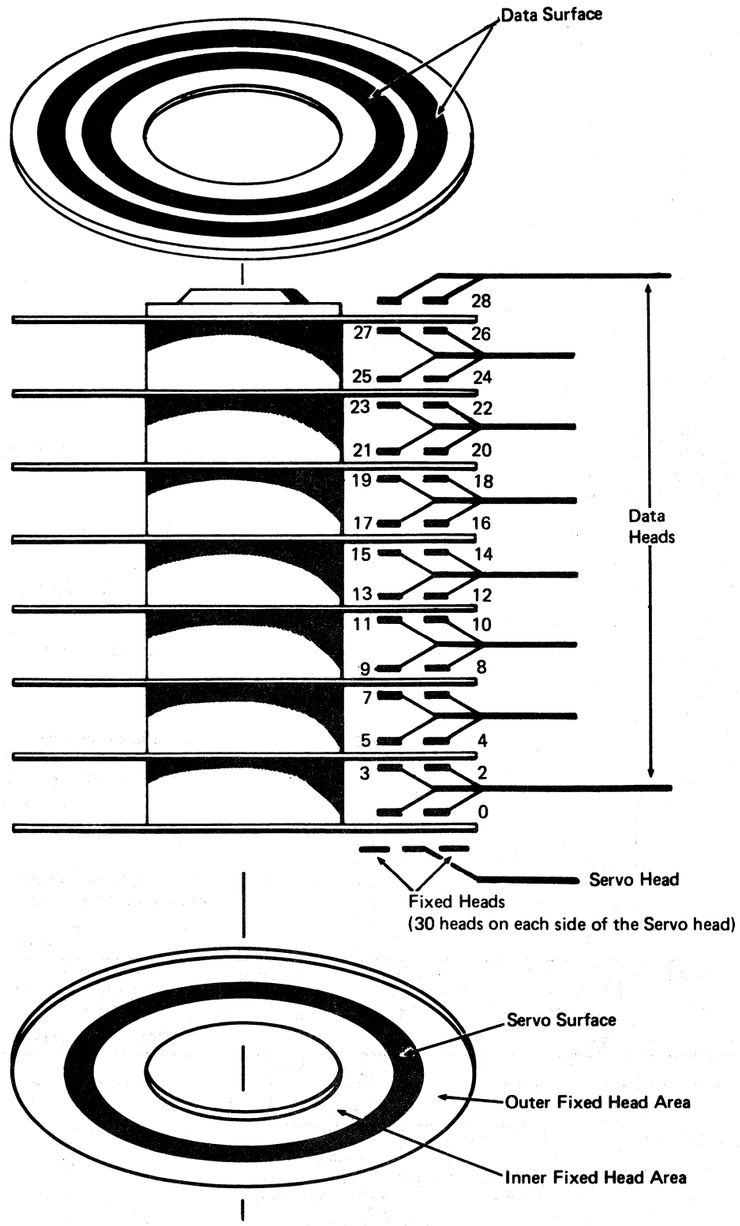
DESCRIPTION

The Head/Disk Assembly (HDA) contains 16 recording surfaces (8 disks). Of these 16 surfaces, the upper 15 are data surfaces; the underside of the bottom disk is the servo surface.

The HDA also contains a movable carriage that attaches outside the HDA to a voice coil motor. The carriage holds 30 movable Read/Write heads and one servo head.

The 30 movable Read/Write heads are located above the 15 data surfaces, two heads for each surface. The servo head is located on the servo surface.

If the 3350 is a Model A2F or B2F, there are 60 additional Read/Write heads on the servo surface. These heads are not attached to the carriage, but are fixed in place outside of the moving range of the servo head, 30 heads on either side of the servo head.



DATA SURFACE

Each data surface contains two data bands. The data bands are divided into tracks numbered from 0 to 560, counting from the outside track to the inside track.

Each data band has its own movable Read/Write head. Each head can read or write information on any of the tracks.

The tracks are assigned as follows:

Tracks 0 to 554	= Customer data tracks
Tracks 555 to 559	= Alternate tracks
Track 560	= CE track

Home addresses are prerecorded on all data tracks for track identification, seek verification, and skip displacement information.

SERVO SURFACE

The servo surface has one servo head and one band of servo data tracks. The servo tracks are prerecorded for seeking, track following, data clocking, Index point signal generation, and rotational position signal generation. If the 3350 is a fixed head model (A2F, C2F, or B2F), the servo surface is also used for reading or writing data by the fixed heads. The fixed-head tracks occupy the areas on both sides of the servo band.

HEAD POSITIONING

The data heads and the servo head are fixed in position on the carriage. The servo head does all of the track seeking and track following; when the servo head is on track, every data head is on track.

Note: *More details of Servo (Access) operation are described beginning on OPER 116.*

HDA SUMMARY

Data Surfaces	15	
Servo Surfaces	1	
R/W Heads	30	(2 per data surface)
Servo Heads	1	
Physical Cylinders	561	
Data 555		
Alternate 5		
CE 1		
Tracks per cylinder (logical and physical)	30	(1 per head)

With fixed heads (Models A2F, C2F, and B2F):

Fixed heads	60
Logical cylinders under the fixed heads	2

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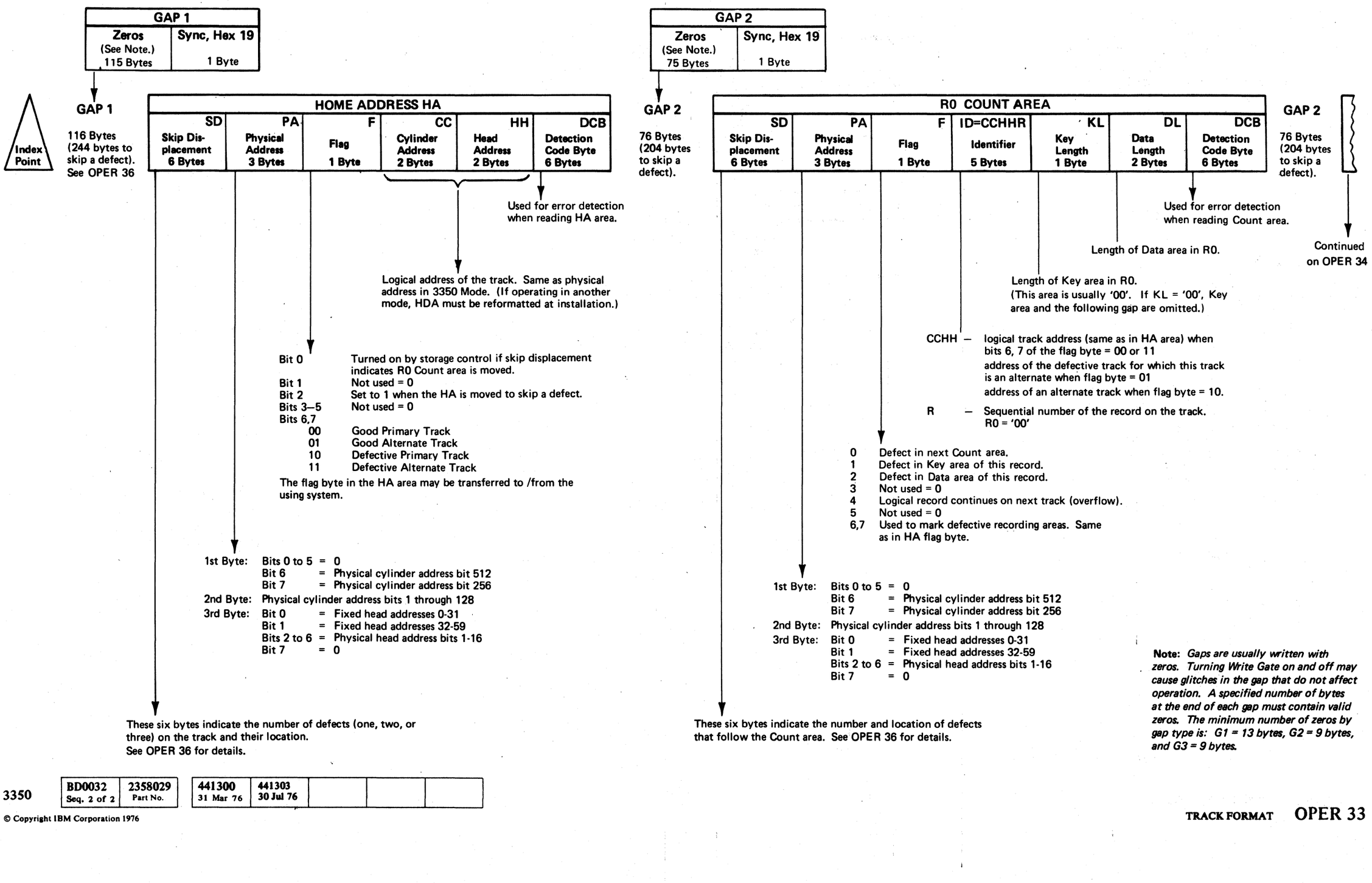

Note: *Gaps are usually written with zeros. Turning Write Gate on and off may cause glitches in the gap that do not affect operation. A specified number of bytes at the end of each gap must contain valid zeros. The minimum number of zeros by gap type is: G1 = 13 bytes, G2 = 9 bytes, and G3 = 9 bytes.*

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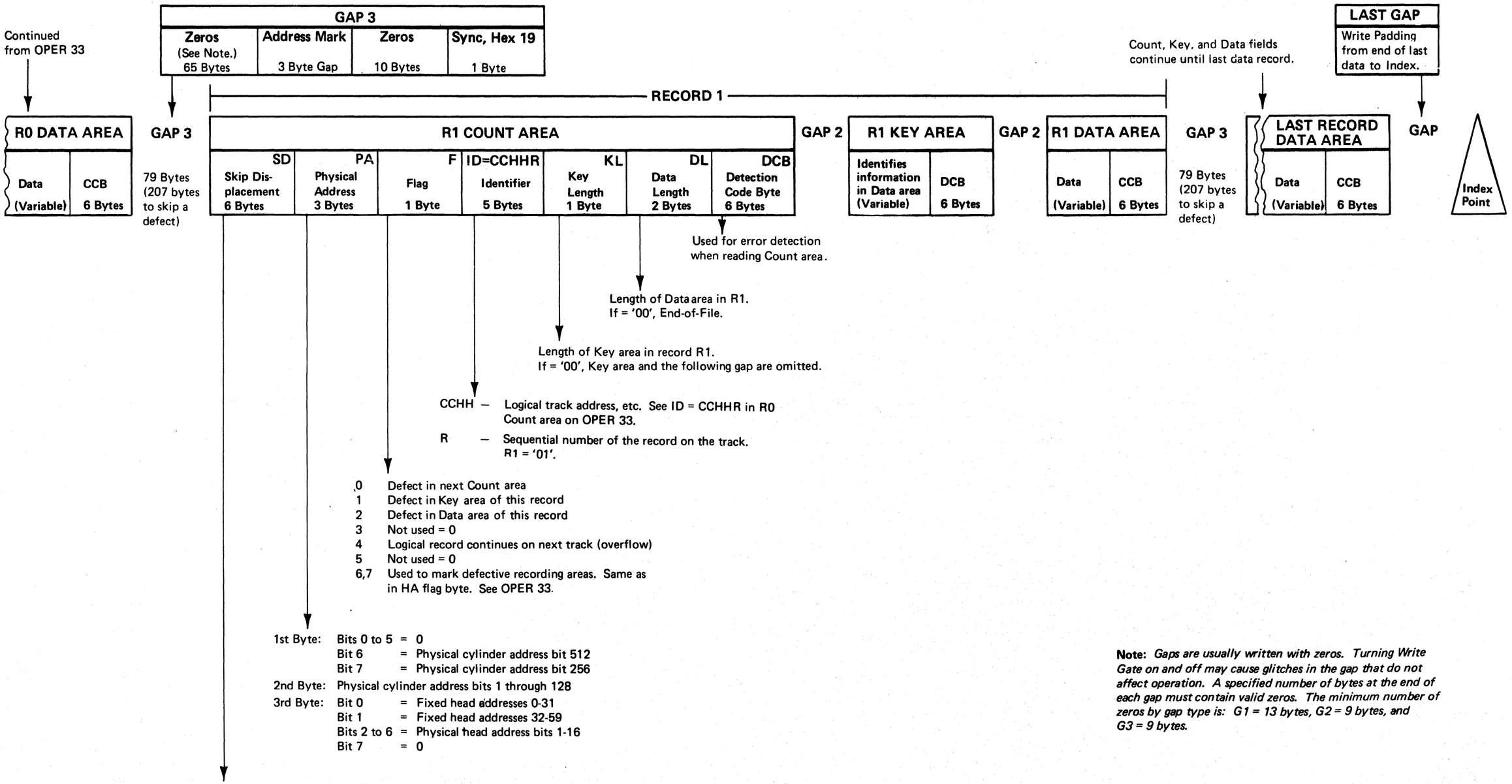
TRACK FORMAT (Continued)



Note: *Gaps are usually written with zeros. Turning Write Gate on and off may cause glitches in the gap that do not affect operation. A specified number of bytes at the end of each gap must contain valid zeros. The minimum number of zeros by gap type is: G1 = 13 bytes, G2 = 9 bytes, and G3 = 9 bytes.*

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SURFACE DEFECT SKIPPING

FORMAT

Before a Head/Disk Assembly (HDA) is shipped from the plant, thorough surface analysis and initialization is performed. During initialization, the Home Address (HA) and Record 0 (R0) areas are written on each HDA track. Both areas include surface defect information. Up to three surface defects are allowed per track. Two bytes are reserved for each possible defect. Hexidecimal 80,00 indicates that there is no defect or that the defect has been passed. The high-order bit is supplied by the storage control during a Write HA operation. If a surface defect is found, its displacement is written in the six bytes of the Skip Displacement (SD) field of the HA and R0 Count areas as follows:

HA Area, SD Field

NO DEFECT
Bytes 1, 3, and 5 = '80'

ONE DEFECT
Bytes 1 and 3 = '80'

Bytes 5 and 6 = distance in bytes from Index to the center of the defect.

TWO DEFECTS
Byte 1 = '80'

Bytes 3 and 4 = distance in bytes from the center of the first defect to the center of the second defect.

Bytes 5 and 6 = distance in bytes from Index to the center of the first defect.

THREE DEFECTS
Bytes 1 and 2 = distance in bytes from the center of the second defect to the center of the third defect. *(See OPER 37.)*

Bytes 3 and 4 = distance in bytes from the center of the first defect to the center of the second defect.

Bytes 5 and 6 = distance in bytes from Index to the center of the first defect.

R0 Count Area, SD Field

NO DEFECT
Bytes 1, 3, and 5 = '80'

ONE DEFECT
Bytes 1 and 3 = '80'

Bytes 5 and 6 = distance in bytes from the end of the Count area to the center of the defect.

TWO DEFECTS
Byte 1 = '80'

Bytes 3 and 4 = distance in bytes from the center of the first defect to the center of the second defect.

Bytes 5 and 6 = distance in bytes from the end of the Count area to the center of the first defect.

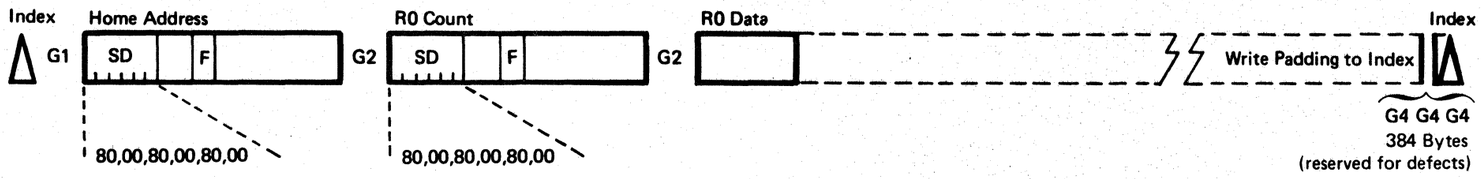
THREE DEFECTS
Bytes 1 and 2 = distance in bytes from the center of the second defect to the center of the third defect. *(See OPER 37.)*

Bytes 3 and 4 = distance in bytes from the center of the first defect to the center of the second defect.

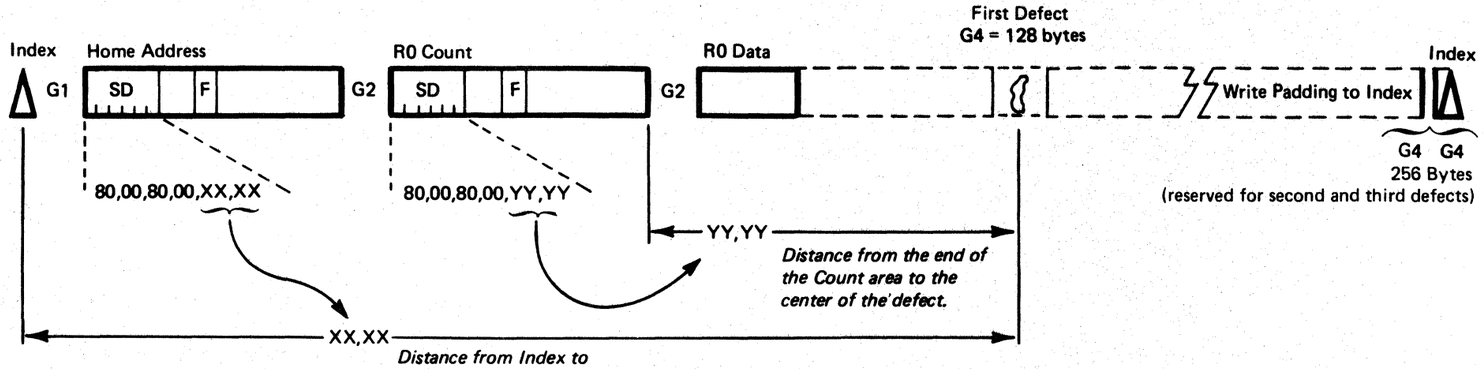
Bytes 5 and 6 = distance in bytes from the end of the Count area to the center of the first defect.

Continued on OPER 37.

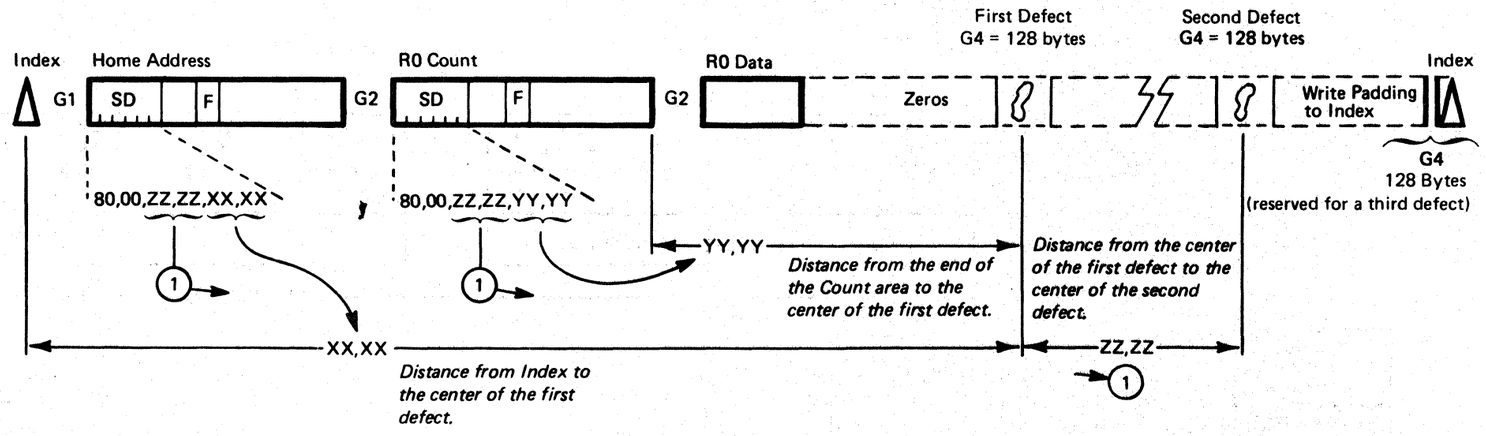
NO DEFECT



ONE DEFECT



TWO DEFECTS



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SURFACE DEFECT SKIPPING

When writing a track containing defects, a special gap of 128 bytes (G4) is written over each defective area.

When the customer formats the HDA and a defect is detected, it can be skipped by:

- Moving the field and extending the preceding gap if the defect falls near or within the gap.
- Splitting the field into two parts and positioning them on each side of the G4 gap previously written over the defective area.

If a defect is too large or there are more than three defects on a single track, the track is flagged and an alternate track is assigned.

HOW TO DETERMINE SKIP DISPLACEMENT

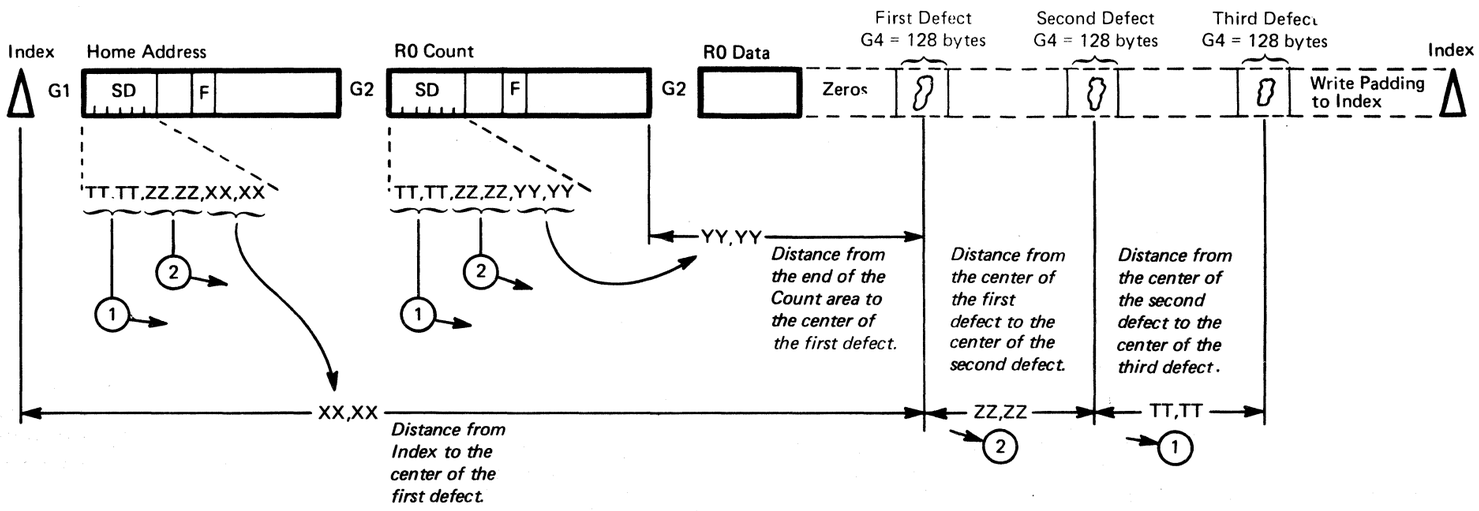
During normal operation, the Skip Displacement field of the Home Address is transparent to the user at the channel level. However, the SD field of the HA can be determined by executing the following CCW chain via the channel:

- Read Home Address
- Sense I/O

If there is no outstanding Device End or Unit check following the execution of this chain, the contents of the SD field of the HA appear in Sense Bytes 18 through 23.

If the track is error free, the SD field 00, 00, 00, 00, 00, 00, (not 80,00....., XX, XX). is contained in Sense Bytes 18 through 23. If the track has one defect, Sense Bytes 18 through 23 contain 00, 00, 00, 00, XX, XX (not 80,00....., XX, XX). The high-order bit (80) is removed by the storage control. The values in Sense Bytes 18 through 23 should be used when rewriting the Home Address.

THREE DEFECTS



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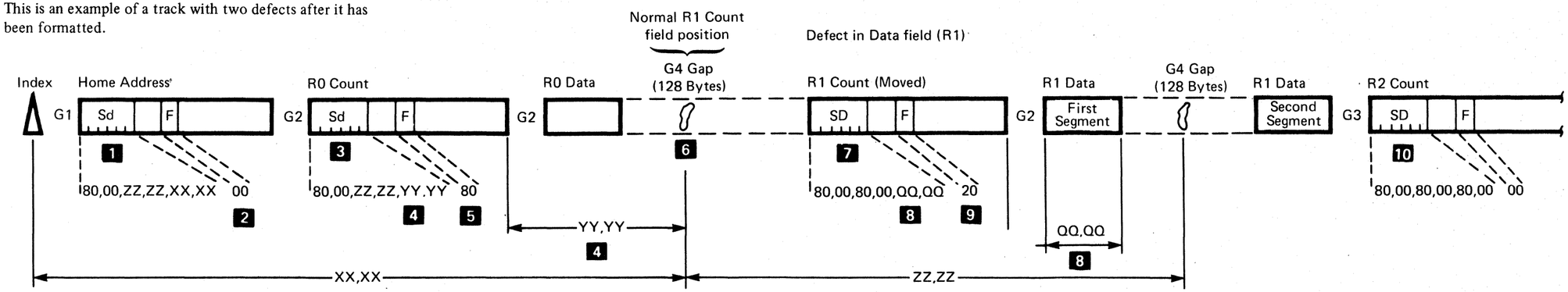
SURFACE DEFECT SKIPPING

This is an example of a track with two defects after it has been formatted.



1 SD bytes indicate that this track has two defects. See OPER 36 for a description.

2 Flag byte indicates that the primary track is good and that the defect does not involve the HA or R0 Count fields.

3 SD bytes indicate that this track has two defects, same as above.

4 Bit 0 of YY, YY is set to 1, and with the flag byte, indicates that the Count field is moved, not split.

5 Flag byte indicates that a defect is in the next Count field.

6 Normal Count field would be here but it has been moved due to the defect.

7 Since the first defect has been passed, its information is no longer required in the SD field. Skip data, relative to the next defect (ZZ, ZZ), is moved to bytes QQ, QQ. Bytes ZZ,ZZ are made inoperative by setting the high-order bit to one. The other bits may or may not be set to zero as shown.

8 Bytes QQ,QQ indicate the length of the Data segment prior to the G4 gap. The difference between QQ,QQ and the data length of the record equals the length of the Data segment following the defect. Bit 0 of QQ,QQ is set to 0, and with the flag byte, indicates that the Data field is split.

9 Flag byte (as shown) indicates that the next defect is in the R1 Data field.

10 Since the second, and last defect, has been passed, the defect information is no longer required. Bytes QQ, QQ are made inoperative by setting the high-order bit to one. The other bits may or may not be set to zero as shown.

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3330-1 MODE – LOGICAL CYLINDERS AND HEADS

When operating in 3330-1 Mode, the HDA is divided into two logical cylinder parts:

- Upper Logical Cylinders
- Lower Logical Cylinders

UPPER LOGICAL CYLINDERS

The upper logical cylinders **1** occupy the top five disk surfaces of the HDA. The upper logical cylinders are numbered: 1,4,7,10,13 (and every third number up to 409). See the Logical Cylinder Reference Chart.

Physical heads 20 to 29 are used for the upper logical cylinders. These physical heads are assigned logical head numbers as in the following example:

Physical head 20 **3** is logical head 0 when the head is at an even Access position, and physical head 20 **3** is logical head 10 when it is at an odd Access position.

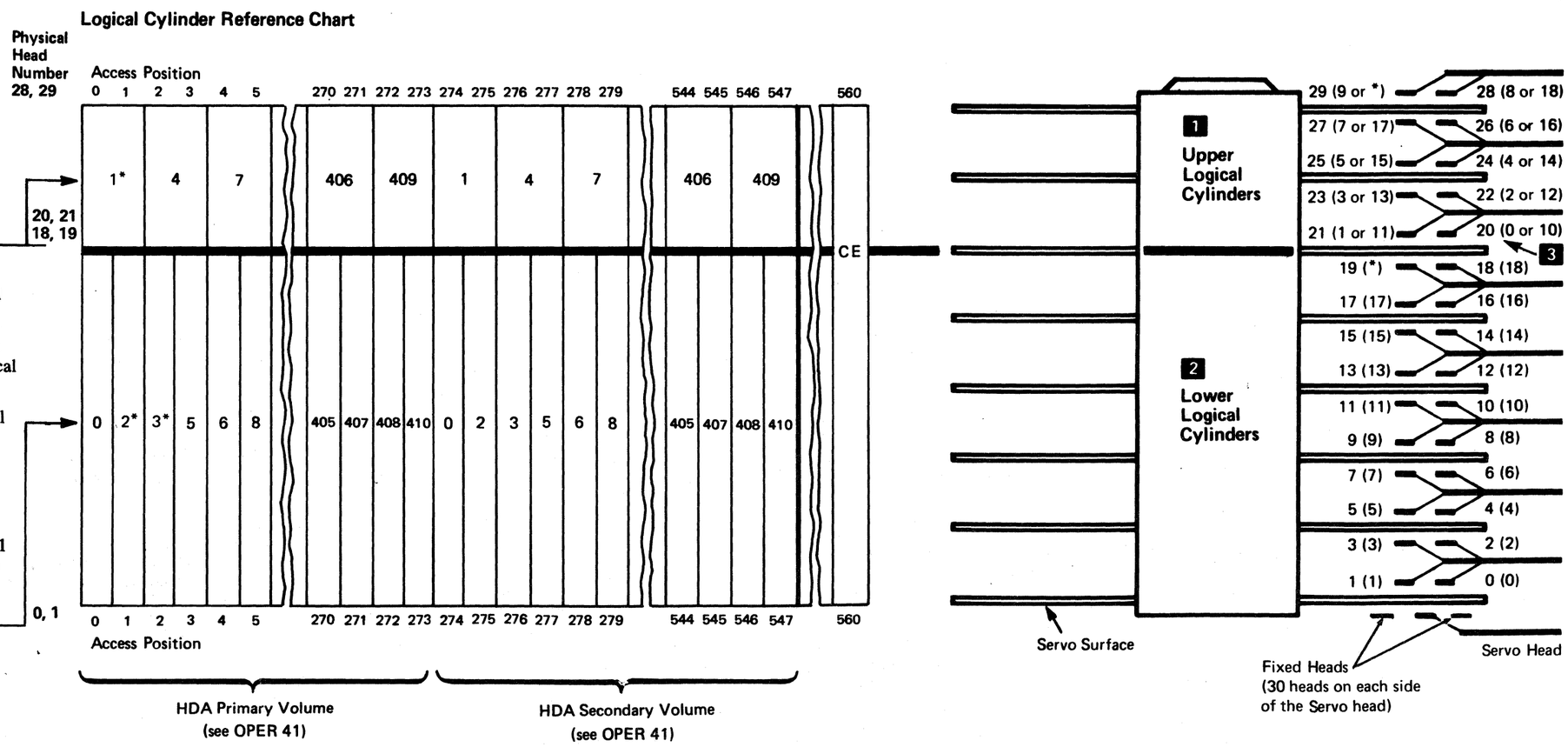
The Physical/Logical Head Chart **4** shows the physical to logical cross-reference at the even or odd Access positions.

LOWER LOGICAL CYLINDERS

The lower logical cylinders **2** occupy ten of the lower 11 disk surfaces. (The bottom surface is the Servo surface.) The lower logical cylinders are numbered: 0,2,3,5,6,8,9 (and all other numbers not used by the upper logical cylinders). See the Logical Cylinder Reference Chart.

Physical heads 0 to 18 are used for the lower logical cylinders (19 is not used). The physical head numbers are the same as the logical head numbers for these lower logical cylinders.

Logical Cylinder Reference Chart



If fixed heads are installed, data for logical cylinders 1, 2, and 3 is written and read by the fixed heads.

4

Physical/Logical Head Chart

Physical Head	Logical Head Number	
	Even Position	Odd Position
20	0	10
21	1	11
22	2	12
23	3	13
24	4	14
25	5	15
26	6	16
27	7	17
28	8	18
29	9	*(not used)

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3330-1 MODE — LOGICAL VOLUMES

When operating in 3330-1 Mode, the HDA is divided into two separate logical volumes representing two logical device addresses:

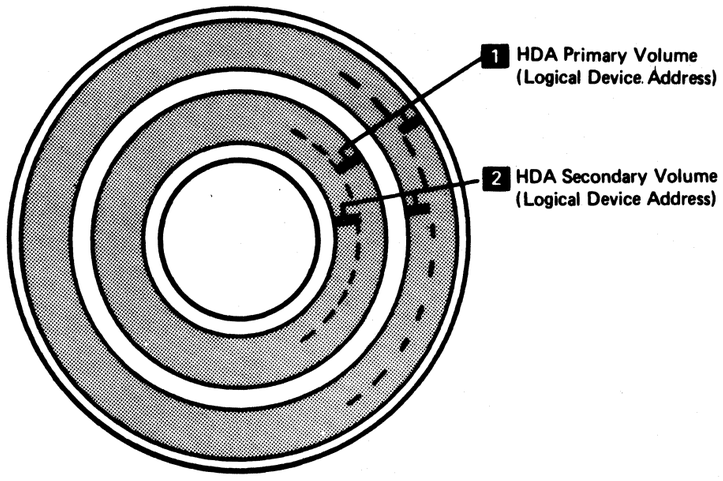
- HDA Primary Volume
- HDA Secondary Volume

HDA PRIMARY VOLUME

The HDA Primary Volume 1 represents one logical addressable device. The HDA Primary Volume consists of the first half of all data bands of the HDA (both the outer data bands and the inner data bands).

HDA SECONDARY VOLUME

The HDA Secondary Volume 2 represents one logical addressable device. The HDA Secondary Volume consists of the second half of all data bands of the HDA (both the outer data bands and the inner data bands).



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3330-1 MODE – TRACK USED COUNTER

TR INDEX

The Index-to-Index track capacity on a 3350 is approximately 19,000 bytes. The track capacity on a 3330 is approximately 13,000 bytes.

To make a 3350 track appear to be a 3330 track, the Track Used Counter (TR Counter) counts only the number of bytes of the 3350 track that would be **used** on a 3330 track. When the TR Counter reaches track capacity of a 3330, the TR Index signal is activated and sent to the Index detection circuits (see ALD page BK210). TR Index at the Index detection circuits indicates that the logical end of the track has been reached. (See Figure 1.)

TR COUNT FIELD

In 3330-1 Mode, each Count area except the R0 Count area contains a TR Count field. The TR Count field is located in the first three bytes after the ECC bytes of the Count area **1** (see Figure 2).

During Write operations, when the Read/Write head is at the end of each Count area, the accumulated count of the TR Counter is written in the TR Count field (see Figure 2).

1. The TR Counter is Off (not counting) from Index time until Gap Counter 63 time in the G2 gap before the R0 Count area (see Figure 2).
2. The TR Counter is On and begins counting from Gap Counter 63 time until Gap Counter 37 time after the R0 Count area. It counts 74 bytes during that time.
3. The TR Counter is Off from Gap Counter 37 time until Gap Counter 63 time.
4. At Gap Counter 63 time, the TR Counter turns On again and counts 64 bytes during the R0 Data area until Gap Counter 37 time. (The number of data bytes in the R0 Data area is 8 for this example.)
5. The TR Counter is Off again from Gap Counter 37 time until Gap Counter 63 time.
6. At Gap Counter 63 time of the G3 gap, the TR Counter turns On again and counts 34 bytes during the R1 Count area. The TR Counter turns Off at the beginning of the ECC bytes (at Gap Counter reset time).
7. After the ECC bytes are written on the track, the accumulated TR count of 'AC' is written in the TR Counter field **1**. (Count = 74 + 64 + 34 = 172 decimal, or 'AC' in hexidecimal).

During Read and Search operations, the value from the TR Count field is read and used to load the TR Counter for use in Write operations that may follow.

Figure 1.

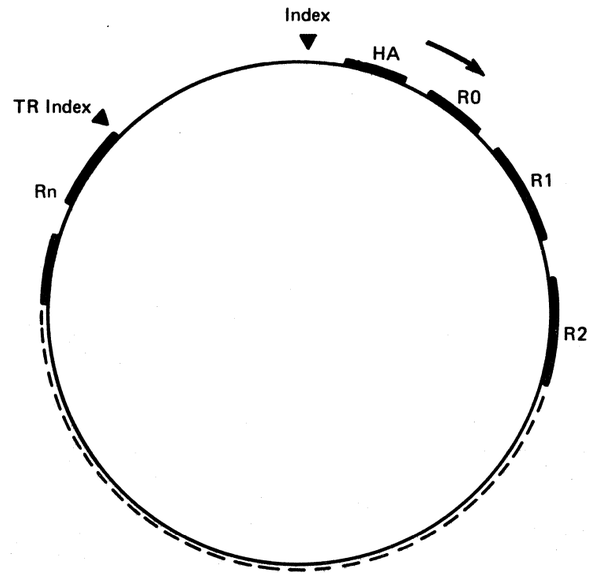
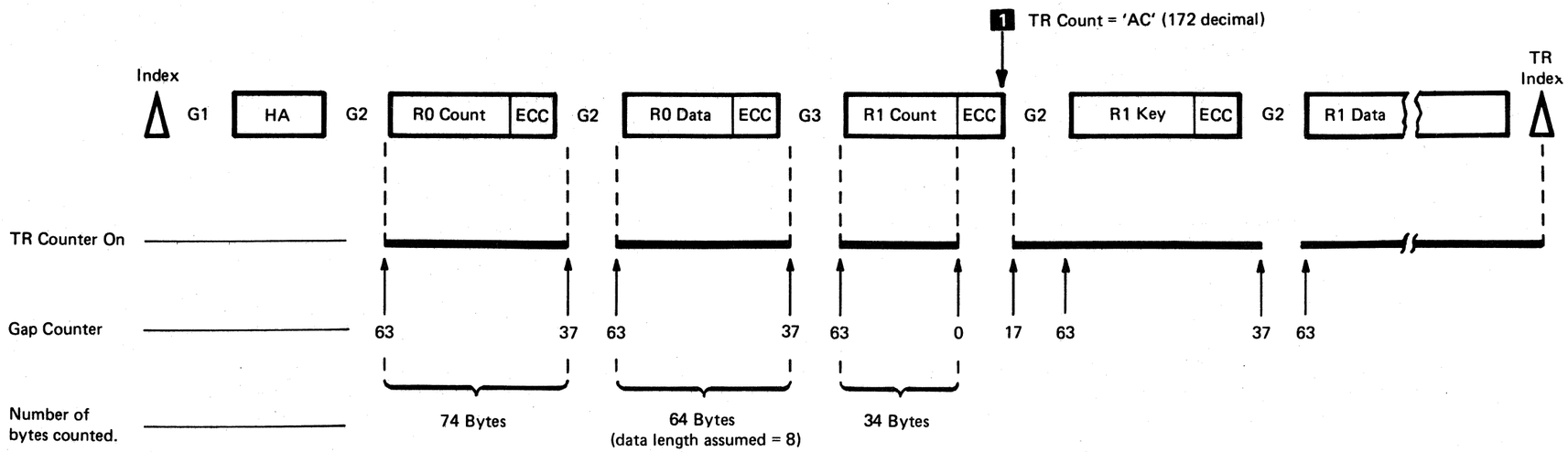


Figure 2.



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3330-11 MODE – LOGICAL CYLINDERS AND HEADS

When operating in 3330-11 Mode, the HDA is divided into two logical parts:

- Upper Logical Cylinders ,
- Lower Logical Cylinders

UPPER LOGICAL CYLINDERS

The upper logical cylinders 1 occupy the top five disk surfaces of the HDA. The upper logical cylinders are numbered 1,4,7,10,13 (and every third number up to number 814). See Logical Cylinder Reference Chart.

Physical heads 20 to 29 are used for the upper logical cylinders. These physical heads are assigned logical head numbers as in the following example:

Physical head 20 3 is logical head 0 when the head is at an even Access position and physical head 20 3 is logical head 10 when it is at an odd Access position.

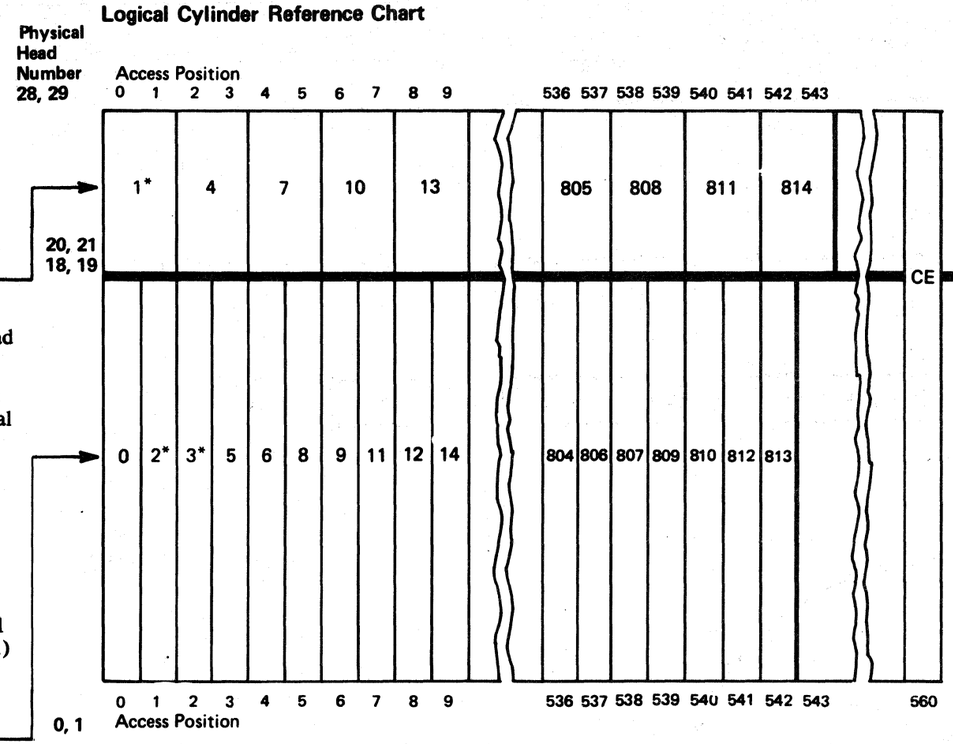
The Physical/Logical Head Chart 4 shows the physical to logical cross-reference at the even or odd Access positions.

LOWER LOGICAL CYLINDERS

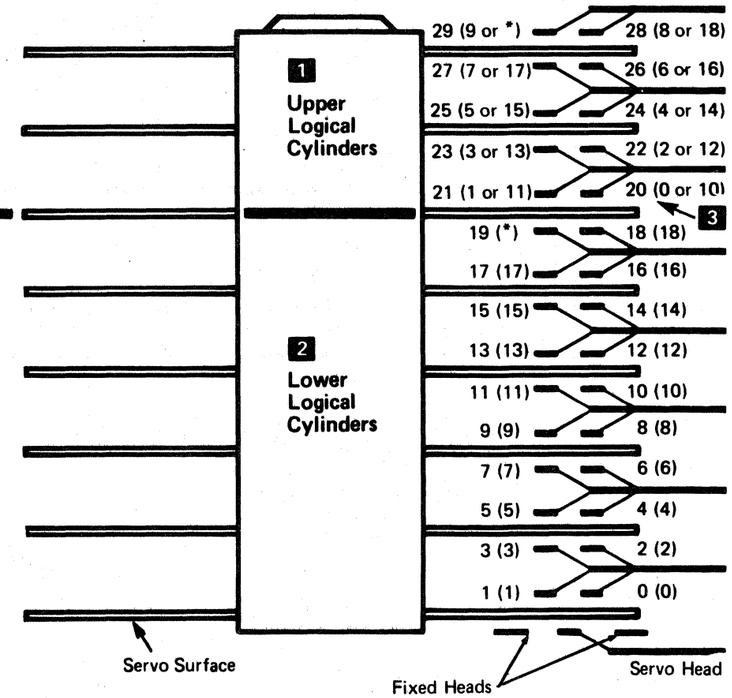
The lower logical cylinders 2 occupy ten of the lower 11 disk surfaces. (The bottom surface is the Servo surface.) The lower logical cylinders are numbered 0,2,3,5,6,8,9 (and all other numbers that are not used for the upper logical cylinders). See the Logical Cylinder Reference Chart.

Physical heads 0 to 18 are used for the lower logical cylinders (19 is not used). The physical head numbers are the same as the logical head numbers for these lower logical cylinders.

Logical Cylinder Reference Chart



*If fixed heads are installed, data for logical cylinders 1, 2, and 3 is written and read by the fixed heads.



4

Physical/Logical Head Chart

Physical Head	Logical Head Number	
	Even Position	Odd Position
20	0	10
21	1	11
22	2	12
23	3	13
24	4	14
25	5	15
26	6	16
27	7	17
28	8	18
29	9	*(not used)

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3330-11 MODE — TRACK USED COUNTER

TR INDEX

The Index-to-Index track capacity on a 3350 is approximately 19,000 bytes. The track capacity on a 3330 is approximately 13,000 bytes.

To make a 3350 track appear to be a 3330 track, the Track Used Counter (TR Counter) counts only the number of bytes of the 3350 track that would be used on a 3330 track. When the TR Counter reaches track capacity of a 3330, the TR Index signal is activated and sent to the Index detection circuits (see ALD page BK210). TR Index at the Index detection circuits indicates that the logical end of the track has been reached. (See Figure 1.)

TR COUNT FIELD

In 3330 Mode, each Count area except the R0 Count area contains a TR Count field. The TR Count field is located in the first three bytes after the ECC bytes of the Count area 1 (see Figure 2).

During Write operations, when the Read/Write head is at the end of each Count area, the accumulated count of the TR Counter is written in the TR Count field (see Figure 2).

1. The TR Counter is Off (not counting) from Index time until Gap Counter 63 time in the G2 gap before the R0 Count area (see Figure 2).
2. The TR Counter is On and begins counting from Gap Counter 63 time until Gap Counter 37 time after the R0 Count area. It counts 74 bytes during that time.
3. The TR Counter is Off from Gap Counter 37 time until Gap Counter 63 time.
4. At Gap Counter 63 time, the TR Counter turns On again and counts 64 bytes during the R0 Data area until Gap Counter 37 time. (The number of data bytes in the R0 Data area is 8 for this example.)
5. The TR Counter is Off again from Gap Counter 37 time until Gap Counter 63 time.
6. At Gap Counter 63 time of the G3 gap, the TR Counter turns On again and counts 34 bytes during the R1 Count area. The TR Counter turns Off at the beginning of the ECC bytes (at Gap Counter reset time).
7. After the ECC bytes are written on the track, the accumulated TR count of 'AC' is written in the TR Counter field. 1 (Count = 74 + 64 + 34 = 172 decimal, or 'AC' in hexidecimal).

During Read and Search operations, the value from the TR Count field is read and used to load the TR counter for use in Write operations that may follow.

Figure 1.

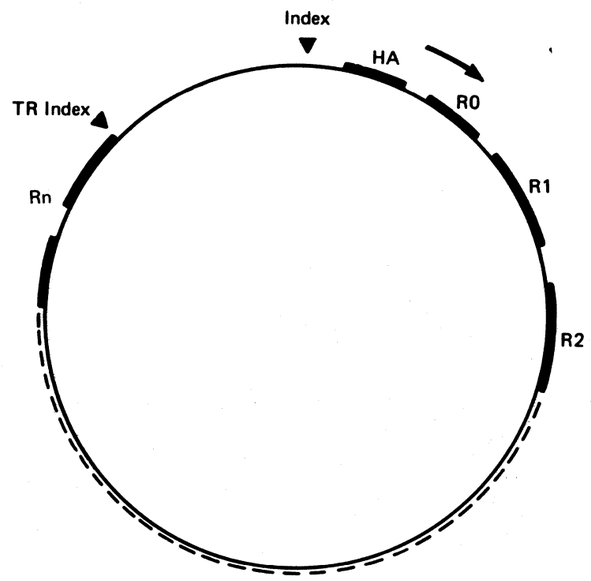
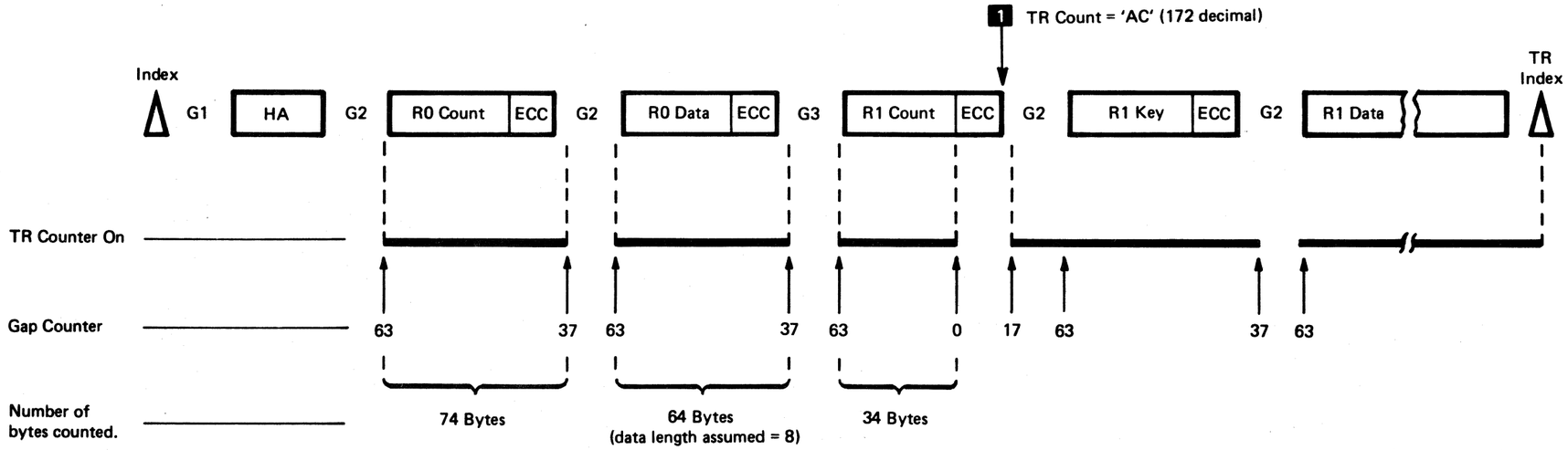


Figure 2.



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CONTROL COMMANDS – DESCRIPTION

Control commands are used to start operations not involving data recorded (or to be recorded) on the HDA. These operations include positioning the access mechanism and selecting the head. For most control functions, the entire operation is specified by the command code. If the command code does not specify the entire control function, the data address field of the CCW designates a main storage location containing the additional information.

Command	Hex Code	Function	Data Transferred Across Channel	Error Conditions			
				Error	Command Executed	Sense Bit Set	Presented During Ending Status
* No Operation	03	No action. Channel End and Device End are presented during initial status.	None				
**Seek	07	1. Moves the access to cylinder specified by the seek address. 2. Selects the head specified by the seek address.	Seek Address (six bytes)	Less than six address bytes transferred.	No	Command Reject	Unit Check Channel End Device End
**Seek Cylinder	0B			Invalid address			
Space Count	0F	When chained from a Read, Search, Write, or Space Count command, this command locates the start of the next Count field (including R0), spaces over the Count field, and ends with Channel End and Device End in the gap before the Key field. When not chained, Space Count searches for Index, clocks over Gap 1, Home Address, Gap 2, and spaces over R0 count. Operation ends in gap following R0 count with Channel End and Device End.	Key Length (one byte) and Data Length (two bytes) which are used during the next command. (See Note.) **Note:** *Key length and Data length values that exceed the actual length of the associated field cause reading in the gap to occur. Data read from the gap area and beyond is unpredictable.*	Index point occurs before an address marker is read. Space Count command chained from an Erase or a format Write command. Write, Erase, Read IPL, Set File Mask, Device Reserve, or Device Release command issued in the same chain following a Space Count command. Index point detected before the end of space count command.	Yes	No Record Found Command Reject Invalid Track Format	Unit Check Channel End Device End
Recalibrate	13	Moves the access to cylinder 0 and selects head 0.	None				
Restore	17	No action. Zero initial status is followed by final status of Channel End and Device End.					
**Seek Head	1B	Selects the head specified by the seek address.	Seek Address (six bytes). Only the 4 low-order bits of the sixth byte are used for the seek address.	Less than six address bytes transferred Invalid address	No	Command Reject	Unit Check Channel End Device End
* Set File Mask	1F	Sets the file mask to indicate permitted Write and Seek commands.	One byte of file mask data.	More than one Set File Mask command issued in a chain of CCWs.	Second Set File Mask Number	Second Set File Mask Command Reject.	
Set Sector	23	Used on disconnected command chaining channels to eliminate the need for the channel to maintain connection with the control unit while waiting for the selected record to reach the head.	One byte specifies angular track position (0–127).	Angular position specified is greater than 127 and less than 255.	No	Command Reject	Unit Check Channel End Device End
* Diagnostic Load	53†	Transfers the specified block of diagnostic microcode from the diskette reader to a storage control buffer.	One byte of control information (Diagnostic Microprogram ID Number).	Invalid sector address.	No	Command Reject	Unit Check Channel End Device End
* Diagnostic Write	73†	3830-2/ISC: Transfers an inline test from main storage to control storage and executes the test. 3880: Transfers 8 bytes of data from main storage to the storage director and initiates execution of the diagnostic test previously loaded by a Diagnostic Load command. All: A 16-byte error code message is stored in the storage control buffer area. A subsequent Diagnostic Sense command transfers the error code message to main storage.	3830-2/ISC: A maximum of 512 bytes 3880: A maximum of 8 bytes	3830-2/ISC: Less than 512 bytes 3880: Less than 8 bytes	No	Command Reject	Unit Check Channel End Device End

*Storage control commands only.

**See OPER 139 for Seek operation description.

†**Note:** *This command is intended for maintenance purposes only. Any use other than that provided by IBM diagnostic programs may yield unpredictable results.*

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SENSE COMMANDS – DESCRIPTION

These commands transfer Sense or usage/error log information from the 3350 string to the using system.

Command	Hex Code	Function	Data Transferred Across Channel	Error	Comments
* Sense I/O	04	Determines the type of error or unusual condition that caused the last Unit Check.	24 bytes of sense information.	Command Reject** Bus Out Parity Overrun	Sense data is reset after transfer.
* Device Reserve	B4	Same as Sense I/O. Also dedicates the addressed device to the storage control issuing the command.	24 bytes of sense information.	Command Reject which sets Unit Check only.	Used only when string switch feature is installed. The command is executed regardless of any abnormal device conditions, such as offline.
* Device Release	94	Same as Sense I/O. Also terminates the dedication of a dedicated device.	24 bytes of sense information.	Command Reject which sets Unit Check only.	Used only when string switch feature is installed. The command is executed regardless of any abnormal device conditions, such as offline.
* Diagnostic Sense	44†	Transfers to the channel any error indications found during a Diagnostic Write command. Transfers from storage control to the channel any diagnostic test data accumulated during a Diagnostic Load command.	16 bytes of Error Code message. 3830-2/ISC: 512 bytes of diagnostic test data. 3880: 16 bytes of diagnostic test data.	Command Reject** Bus Out Parity Overrun	If the command is not preceded by a Diagnostic Write or a Diagnostic Load command, 16 bytes of data from the Error Code message area are transferred.
* Read and Reset Buffered Log	A4	Supplies usage or error statistics on the addressed drive.	24 bytes of usage or overrun error information.	Command Reject** Bus Out Parity Overrun	Usage or overrun error information is reset after transfer.
* Sense I/O Type	E4	Transfers seven bytes to the channel to identify the selected storage control type and the Device type.	Byte 0 = 'FF' Byte 1 = 'xx' } Storage Byte 2 = 'xx' } Control Type Byte 3 = 'xx' Storage control model Byte 4 = '33' } Device Byte 5 = '50' } type Byte 6 = '00' Device model	Unit Check and Intervention Required if the device is not powered on.	
Unconditional Reserve	14	Removes the string switch reservation from one storage control and establishes a reservation for the other storage control.	24 bytes of sense information.	Command Reject which sets Unit Check only.	Used only when string switch feature is installed. The command is executed regardless of any abnormal device conditions, such as offline. **Note:** *Indiscriminate use of this command can impact data integrity by removing a reservation during a data transfer operation.*

* *Storage control commands only.*
** *Sets Unit Check, Channel End, and Device End.*

† **Note:** *This command is intended for maintenance purposes only. Any use other than that provided by IBM diagnostic programs may yield unpredictable results.*

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READ COMMANDS – DESCRIPTION

Read commands transfer information from the subsystem to main storage of the using system. On all Read commands, the device checks (by means of correction code bytes) the validity of each area of a record as the record is read from a track. A parity bit is added to each byte as it is sent to the channel. All Read commands can operate on overflow records and, except for Read IPL and Read Sector, can operate in multitrack mode.

MULTITRACK MODE

Setting bit 0 of a Read command enables the drive to automatically select the next sequentially numbered head. Head switching does not occur when:

- The incremented head address crosses a file protected boundary.
- The incremented head address exceeds the limits of the cylinder.

Command	Hex Code		Function	Data to be Read	Error Type**			Comments
	Single Track Mode	Multi-Track Mode			Data Overrun	Data Check		
						Correctable	Uncorrectable	
*Read Initial Program Load	02	—	Seeks to cylinder 0 and head 0, searches for Index, and reads R1 data from the drive to main storage.	First data area after R0.	Yes	Data Field. Use ECC.	System repeats operation.	A Read IPL command cannot be preceded by a Set File Mask command in the same chain.
*Read Data	06	86	Transfers Data area of a record from drive to main storage.	First data area after address marker or the data area of the record that was chained from the Count or Key area of the same record.	Yes	Use ECC.	System repeats operation.	
*Read Key and Data	0E	8E	Transfers Key and Data areas of a record from drive to main storage.	First Key and Data area after address marker or the Key and Data area that was chained from the Count area of the same record.	Yes	Data Field. Use ECC.	System repeats operation.	If the K_L equals 0, the command is executed as a Read Data command.
*Read Count	12	92	Transfers next Count area (8 bytes) from the drive to main storage	Next record Count area or first Count area after R0.	Yes		System repeats operation.	
*Read Record Zero (R0)	16	96	Transfers the Count, Key, and Data areas of R0 from the drive to main storage.	Record 0	Yes	Data Field. Use ECC.	System repeats operation.	When chained from a Search HA or Read HA command, the Read R0 command is executed immediately and does not initiate a search for index point.
*Read Home Address	1A	9A	Transfers 5 bytes (FCCHH) of the home address to channel.	Byte 0 = Flag Byte 1 = Cylinder address Byte 2 = Cylinder address Byte 3 = 0 Byte 4 = Head address	Yes		System repeats operation.	
*Read Count, Key, and Data	1E	9E	Transfers Count, Key, and Data areas of a record from drive to main storage.	Next record or first record after R0.	Yes	Data Field. Use ECC.	System repeats operation.	
*Read Sector	22	—	Transfers to the channel one byte of angular position information which is used by a subsequent Set Sector command. The byte transferred contains the angular position required to access the last record processed on the drive.					Causes loss of orientation.
*Read Multiple Count, Key, and Data	5E	—	Transfers the remaining records on a track to the channel.		Yes	Data Field. Use ECC.	System does not repeat operation.	

** See OPER 230 for Read operation description.*
*** Sets Unit Check, Channel End, and Device End.*

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WRITE COMMAND – DESCRIPTION

Write commands transfer data from main storage to the subsystem for recording on the HDA. While writing data, the device appends the appropriate correction code bytes to each Count, Key and Data area as they are written. There are two types of Write commands: (1) Format Write commands, used to establish records, and (2) Nonformat Write commands (Write Data and Write Key and Data), used to update previously written records.

Command	Type	Hex Code	Function	Data Written	Error **	Comments
* Write Special Count, Key and Data	Format	01	Same as Write Count, Key, and Data command except a 1 is written in bit 4 of the flag byte to indicate an overflow record segment.	Same as Write Count, Key, and Data		Same as Write Count, Key, and Data. Not used for last segment of an overflow record.
* Write Data	Non-format	05	Changes the Data area of a record.	Data from the system. Write the number of bytes specified by the D_L D_L bytes of the Count area of the same record.	Command Reject Bus Out Parity Overrun	If file mask is violated, set Command Reject. Must be chained from a successful Search Equal Key or Search Equal ID command. Also, CCW count must equal D_L D_L.
* Write Key and Data	Non-format	0D	Changes the Key and Data areas of a record.	Data from the system. Write the number of bytes specified by the K_L and D_L D_L bytes of the Count area of the same record.		If file mask is violated, set Command Reject. Must be chained from a successful Search Equal ID command. If K_L=0, operation is the same as Write Data. Also, CCW count must equal K_L and D_L D_L.
Erase	Format	11	Operates exactly like a Write Count, Key, and Data command except data from the channel is not written on the track.	Bytes of 0s to end of track.		The storage control skips writing an Address Marker, Sync Byte, or ECC.
* Write Record (R0)	Format	15	Writes Count, Key, and Data of R0.	Flag byte from HA area. CCHHR$K_L D_L D_L$ from system written in Count area. Key and Data from system.		Same as Write Count, Key, and Data except must be chained from a Write HA or a successful Search HA Equal command.
* Write Home Address (HA)	Format	19	Writes the 11-byte (SDFCCHH) Home Address area on the selected drive and track. (SD equals 6 bytes.)	11-byte (SDFCCHH) home address field transferred from the system.		Must be chained from a successful Search HA command with a CCW count of four or more. If the CCW count is less than five, Command Reject is set.
* Write Count, Key, and Data	Format	1D	Writes 1 complete record on the selected drive and track.	Count, Key, and Data areas of next record on the track. Data for the areas comes from the system. The Count area flag byte, ECC, and gap data comes from storage control.	Command Reject Bus Out Parity Overrun. Invalid track format.	If file mask is violated, set Command Reject. Must be chained from Write R0; Write Count, Key, and Data; Erase; or a successful Search Equal ID or Search Equal Key command. After last Count, Key, and Data command on a track, Write Padding to Index.

See OPER 225 for Write operation description.

**Sets Units Check, Channel End, and Device End.*

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SEARCH COMMANDS – DESCRIPTION

Search commands transfer a specific number of bytes from main storage to storage control. Storage control compares these bytes with data read from a track record. When the condition specified in the Search command is satisfied, the Status Modifier bit is set. The status bytes hold the condition of the Status Modifier bit until that bit is reset. Significant bit definitions of the Search Commands are:

- Channel Status Byte bit 1, Status Modifier, is set when search is successful.
- If a Search command is unsuccessful, it must be reissued to continue the search.
- Multitrack bit is not on. Search until successful or Index is passed twice.
- Multitrack bit is on. Head switches to the next track at Index.

MULTITRACK MODE

Setting bit 0 of a Search command enables the drive to automatically select the next sequentially numbered head. Head switching does not occur when:

- The incremented head address crosses a file-protected boundary.
- The incremented head address exceeds the limits of the cylinder.

Command	Hex Code		Function	Data Compared	Error **	Comments
	Single Track	Multi-track				
* Search Key Equal	29	A9	Locates a Key area selected by the system.	The Key area bytes from the selected drive and track, with data from the system.	Command Reject Bus Out Parity Overrun End of Cylinder No Record Found Data Check.	The Key area compared is the Key area of the next record (excluding R0), unless chained from a Read Count or Search ID command. If chained from a Count operation, the Key area searched is in the same record.
* Search ID Equal	31	B1	Locates a Count area selected by the system.	Five bytes (CCHHR) of the next Count area from the selected drive and track, with CCHHR from the system.		
* Search Home Address Equal	39	B9	Locates a Home Address area selected by the system.	Four bytes (CCHH) of Home Address area from the selected drive and track, with CCHH from the system.		
* Search Key High	49	C9	Locates a Key area selected by the system.	The Key area bytes from the selected drive and track, with Key area bytes from the system.		Locates any Key area that is higher than the Key area from the system.
* Search ID High	51	D1	Locates a Count area selected by the system.	Five bytes (CCHHR) of the next Count area from the selected drive and track, with CCHHR from the system.		Locates a Count area with an ID higher than the ID from the system.
* Search Key Equal or High	69	E9	Locates a Key area selected by the system.	The Key area bytes from the selected drive and track, with Key area bytes from the system.		Locates any Key area that is equal to or higher than the Key area from the system.
* Search ID Equal or High	71	F1	Locates a Count area selected by the system.	Five bytes (CCHHR) of the next Count area from the selected drive and track, with CCHHR from the system.		Locates a Count area with an ID that is equal to or higher than the ID from the system.

*See OPER 200 for search operation description.
**Sets Unit Check, Channel End, and Device End.

Note: *If a Search operation is started on the track at a point past the key, count, or record being searched for, the information will never be found because head switch occurs at Index. See the Reference Manual for 3350 (Order No. GA26-1638) for the correct start procedure.*

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CONTROL INTERFACE

This page identifies and defines each part of the control interface. (The basic timing sequence of the interface is given on OPER 95. The Tag and Bus information for each Tag decode is summarized in chart form on OPER 98 through 101 and fully described on OPER 102 through 106.)

- The control interface is the common connection between storage control and all attached controllers.
- The controllers are attached in parallel to one set of signal lines, allowing simultaneous addressing or polling by the storage control.
- A controller is connected to the interface until all information is transferred and the storage control signals it to disconnect.
- Only one controller is logically connected to the storage control at a time.
- Signals from different controllers are ORed together to be transmitted to the storage control on common lines.

CONTROL TAG BUS OUT

Tag Bus Out Bits

Tag Bus Out bits 0, 4 through 7, and P send an instruction (control information) to the controller when Tag Gate is active. The instruction identifies the operation to be performed.

All Tag Bus data must be valid at least 100 ns before Tag Gate becomes active, and must remain valid at least 150 ns after Tag Gate becomes inactive.

Tag Gate

Tag Gate indicates the presence of an instruction on Tag Bus. Tag Gate remains active until acknowledged by the controller with Tag Valid.

An operation must be decoded in the controller within 100 ns after Tag Gate becomes active.

Select Hold

Select Hold becomes active during any Select Tag. Select Hold remains active to maintain selection of a drive until the end signal of the last operation to be performed on the drive is received and acknowledged.

Sync Out

Sync Out checks the data count during controller data transfers and orientation clocking.

Sync Out is not dc-interlocked with any inbound line, but it must have a minimum pulse width of 60 ns.

Recycle

Recycle forces the Gap counter (in Modulo-16 mode) to continue counting data bytes by causing the Gap counter to count to 15, step to 0, and count to 15 and continue in this manner until all bytes of data have been transferred. Recycle becomes inactive during transmission of the last 16 bytes of data to end the data transfer sequence at count 15.

Response

Response acknowledges either a Normal End or Check End condition. Response is not dc-interlocked with any line, but it must have a minimum pulse width of 60 ns.

CONTROL BUS OUT

Control Bus Out transfers control or address information to the controller as a tag modifier when Tag Gate is active. Bus Out must be valid at least 100 ns before Tag Gate becomes active, and must remain valid at least 150 ns after Tag Gate becomes inactive.

Control Bus Out transfers data to the controller for the drive when Sync Out is active. All Bus Out data must be valid at least 100 ns before Sync Out becomes active, and must remain valid for at least 100 ns after Sync Out becomes inactive.

CONTROL TAG BUS IN

Sync In

Sync In validates and times Bus In during data transfers from the controller to storage control. Sync In becomes active after Bus In is valid.

Bus In remains valid until after Sync In becomes inactive. During data transfers from the storage control to controller, Sync In provides timing for the data being transferred.

Select Active

Select Active becomes active as a result of the selection sequence. It remains active to indicate proper selection as long as Select Hold is active and selection of the drive is correctly maintained by the controller.

Tag Valid

Tag Valid indicates that the controller or drive has validated and accepted a tag instruction sent from the storage control. When required, Tag Valid indicates to storage control that Bus In information is valid.

Normal End

Normal End indicates that the normal ending of an operation occurred with the expected results. Normal End is active with or before Tag Valid for Immediate operations. For Read, Write, Set Read/Write, and ECC Control operations (Extended operations), Tag Gate becomes inactive and the operation is complete before Normal End becomes active.

Normal End becomes active at the successful completion of the operation. Information on Bus In is valid at the start of Normal End.

When Normal End is generated with Tag Gate, it remains active until Tag Gate becomes inactive; otherwise it remains active until Response becomes active.

Check End

Check End indicates that an abnormal ending condition exists. The abnormal condition is presented on Bus In with proper parity during the time Check End is active.

For Read or Write operations, Check End is active and Bus In maintains proper parity until the storage control acknowledges the receipt of the status information by activating the Response line.

Check End is not activated on an Immediate operation.

Alert Lines

Selected Alert lines indicate that certain special events have occurred in the selected drive or controller. They are active only if Select Active is present.

Unselected Alert indicates that the execution of an appropriate polling sequence is required.

SELECTED ALERT LINE 1 (Error Alert): Indicates an unusual condition (Equipment Check) in the selected controller or drive.

SELECTED ALERT LINE 2 (Index Alert): Indicates the detection of Index or an ECC correctable pattern.

UNSELECTED ALERT LINE 1 (CE Alert Execute): Indicates that a CE Panel Execute switch was operated.

If more than one controller is on the interface, the storage control must poll to determine which controller activated the Alert.

CONTROL BUS IN

Control Bus In transmits data from the drive to storage control when Sync In is active. Certain commands cause status, error, or information originating in the drive to be transmitted on Bus In while Tag Valid is active.

If an abnormal condition occurs during a Read, Write, or ECC Control operation (Extended operations), Check End is activated and the error information relating to the abnormal condition is presented on Bus In.

During read data transfers, Bus In is active at least 125 ns before Sync In and remains active for at least 125 ns after Sync In is inactive.

During information transfers, Bus In is active with or before Tag Valid and is valid until the tag ends.

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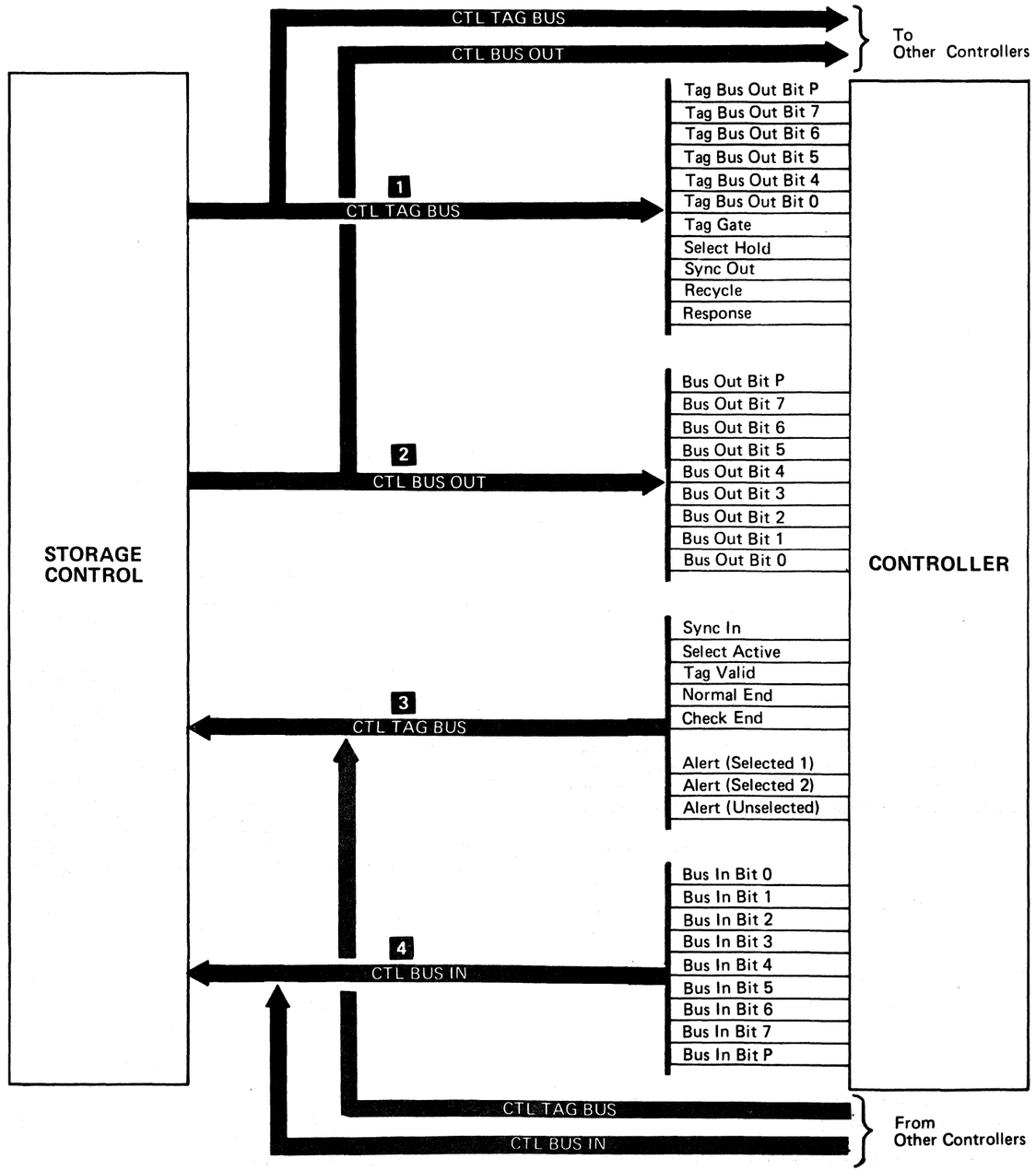

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DEVICE INTERFACE

This page defines the device interface. (The Tag and Bus information for each Device Tag decode is summarized in chart form on OPER 100 and 101. The Tag decodes are fully described on OPER 104 through 106).

- The device interface is the common connection between all drives and the controller.
- The interface can accommodate up to eight drives.
- All signals from the controller are received by all drives.
- Like signals from different drives are ORed together on a common line to the controller.
- Read/Write data and PLO reference pulses are carried on two balanced, bi-directional cables.

DEVICE BUS OUT

Device Bus Out transfers operational information from the controller to the drive. The meaning of the information is determined by the Tag Bus.

Parity is checked at the drive for all functions except Read/Write.

DEVICE TAG BUS

Device Tag Bus Bits 0, 1, 2, and Parity

The following Device Tag Bus lines are coded to define the data presented on Bus Out:

Code	Tag
000	Select
001	Sense Interface
010	Diagnostic Set
011	Set HAR
100	Set Difference (count)
101	Set Target
110	Set Cylinder (address)
111	Control

Tag Gate

The Tag Gate signal is sent to the drives to gate the Tag Bus and Bus Out. It is raised after the data appears on the bus and an appropriate delay has elapsed (see OPER 95).

Select Hold

Select Hold is used to maintain selection. It must be raised before or during Tag Gate and stay up as long as communication is necessary with the selected drive.

READ/WRITE DATA

The Read/Write data cable carries Read or Write data from the controller to the selected drive when writing, and from the selected drive to the controller when reading.

PLO PULSES

PLO reference pulses, necessary for write data clocking, are transmitted from the selected drive to the controller via the PLO cable when Select Hold is up.

DEVICE BUS IN

Device Bus In carries status and sense information from the selected drive to the controller. As soon as a drive is selected, machine status is placed on Device Bus In. Status stays on the bus until one of the following occurs:

- Select Hold falls.
- A Sense or Read/Write function control tag is raised.
- A Diagnostic Set or Sense Interface tag is raised.

ATTENTION/SELECT RESPONSE BUS

This bus transmits the unique 1-bit physical drive address to the controller when the drive has an Attention signal to present or when that drive is selected.

Attention is generated by:

- HDA Attention.
- Seek Complete.
- Pad Complete.
- Sector Compare.
- Search Sector.

If a drive is in CE Mode, attention appears on Bus Bit S (service drive position).

The Select Response signal represents the physical address of the drive that has been selected. Only one bit should appear on the bus when a drive is selected:

Bus Bit	Unique Physical Drive Address
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
S	Service Drive

TAG VALID

Tag Valid is sent from the selected drive to indicate that Device Bus Out and Tag Bus were received with correct parity. Device Tag Valid forces Tag Valid and Normal End in the controller.

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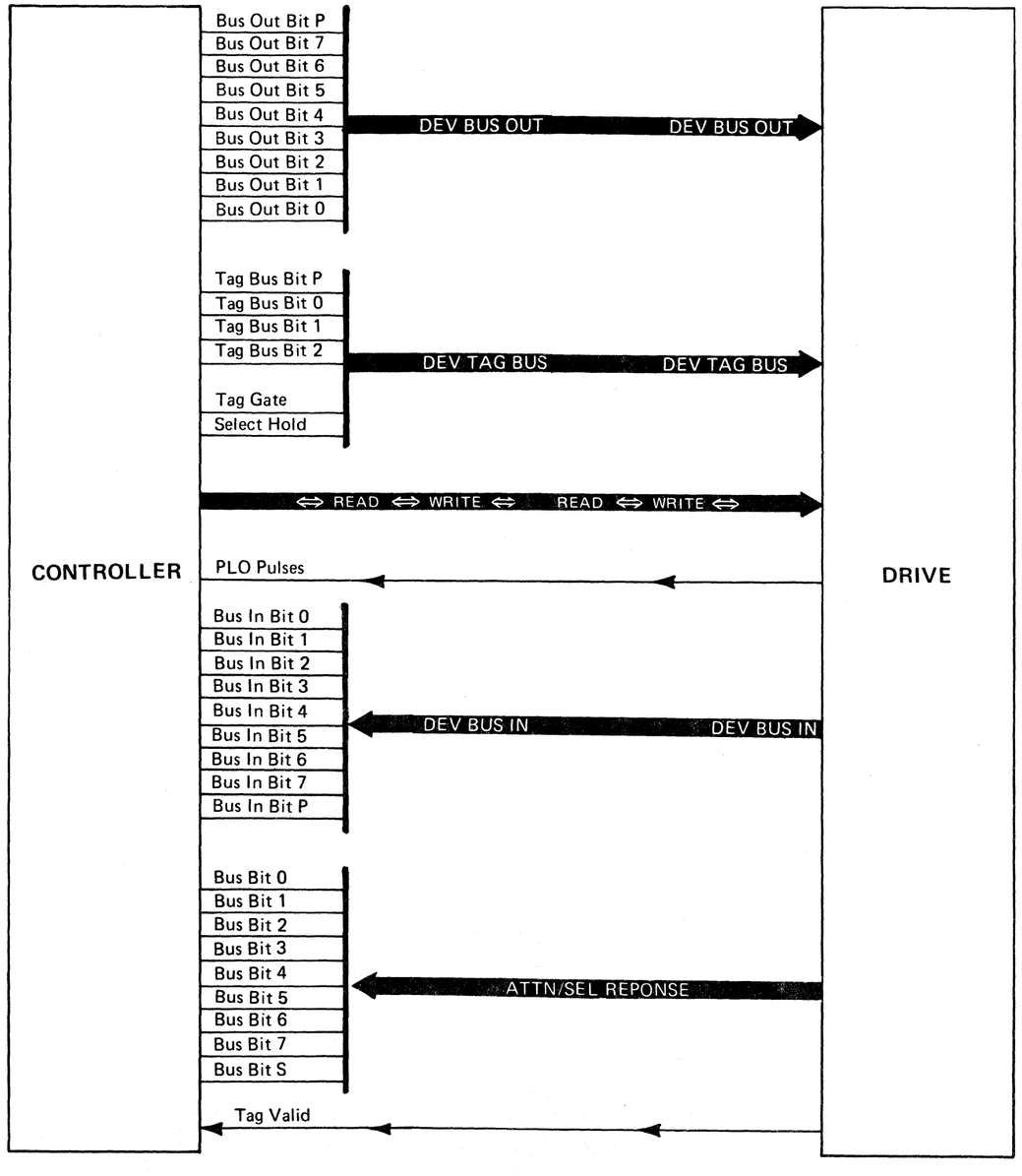

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CONTROL/DEVICE INTERFACE TIMING

There are three types of interface operation:

- Immediate Operation
- Extended Operation
- Select Operation

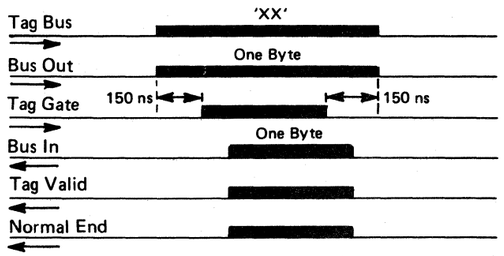
IMMEDIATE OPERATION

An Immediate operation transfers a single control instruction to the controller over the Control Interface and a single byte of information to or from the controller.

The appropriate tag is placed on the Ctl Tag Bus. At the same time, a single byte of data, either an instruction modifier or a byte of information, may be placed on the Ctl Bus Out. Tag Gate is raised after allowing for the 150 ns de-skewing.

The controller responds with Tag Valid, forcing Normal End. Data sent by the controller is placed on Ctl Bus In along with Normal End. The storage control must provide for any de-skewing for the interface. When Normal End is returned, data on Bus In is the expected response from the controller. Tag Gate drops when Tag Valid and Normal End are recognized by the storage control. The controller resets Tag Valid and Normal End when Tag Gate becomes inactive. The storage control cannot activate Tag Gate again until Tag Valid becomes inactive.

Check End is not presented on Immediate operations.



EXTENDED OPERATION

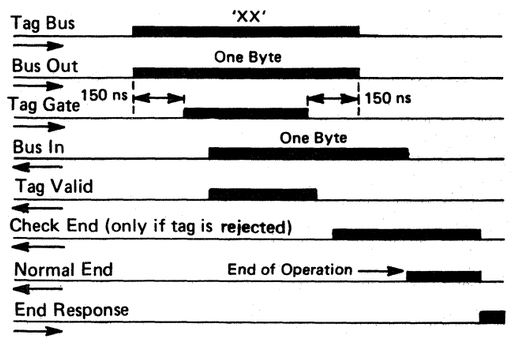
An Extended operation starts a sequence of events in the controller that requires extended time or many transfers across the Control Interface and Device Interface. The Extended operations are Read, Write, Set Read/Write, and ECC Control. The appropriate tag is placed on the Ctl Tag Bus. Simultaneously, a single byte of data or modifier information is placed on Ctl Bus Out. Tag Gate starts after the 150 ns de-skewing interval.

The controller responds with Tag Valid, indicating acceptance of the tag, causing the storage control to reset Tag Gate.

If the operation cannot be performed because of an abnormal condition, such as Command Overrun, Check End is indicated after Tag Gate becomes inactive. Ctl Bus In indicates the check condition.

If the operation can be performed, Normal End is activated at the completion of the operation.

Normal End or Check End remains active until Response is returned to the controller to acknowledge either end condition.



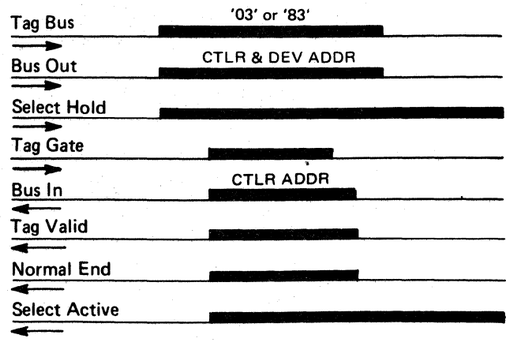
SELECT OPERATION

A Select Operation connects the storage control to a specified controller or drive.

The appropriate select tag is placed on the Ctl Tag Bus. Modifiers and address information are placed on the Ctl Bus Out. Assuming that the tag and bus information is correct, Select Hold and Tag Gate become active.

When selection has been completed, the controller responds with Tag Valid, Select Active and Normal End. When these tags are acknowledged by the storage control, Tag Gate becomes inactive. While Tag Valid is present, Ctl Bus In returns the address of the selected controller. The address contains coding that allows the storage control to check for double selection.

Select Hold maintains selection and must remain active until all operations are complete on the selected controller or drive. Select Active remains active until Select Hold falls. If a selection error occurs within the controller or drive, no response is generated.



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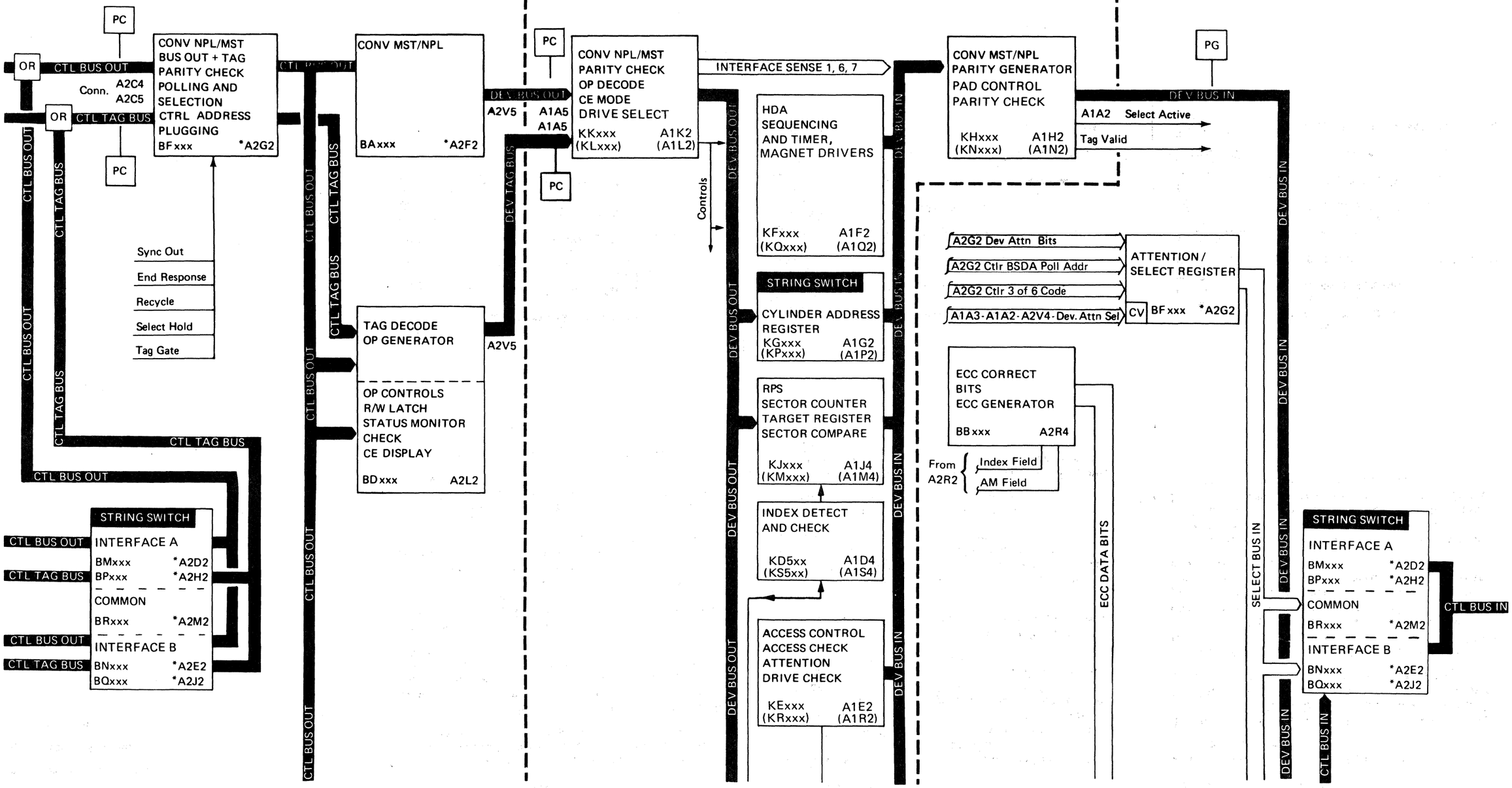
CONTROLLER OUT — DRIVE — CONTROLLER IN

See Legend on OPER 97.



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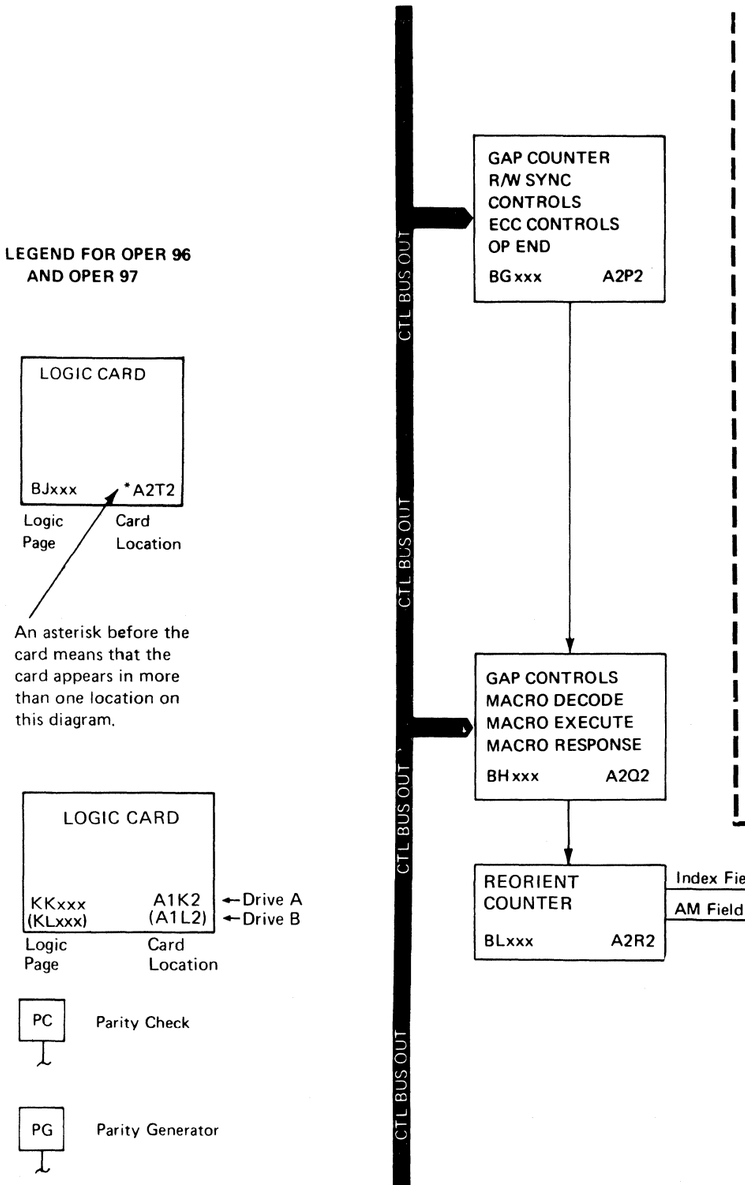

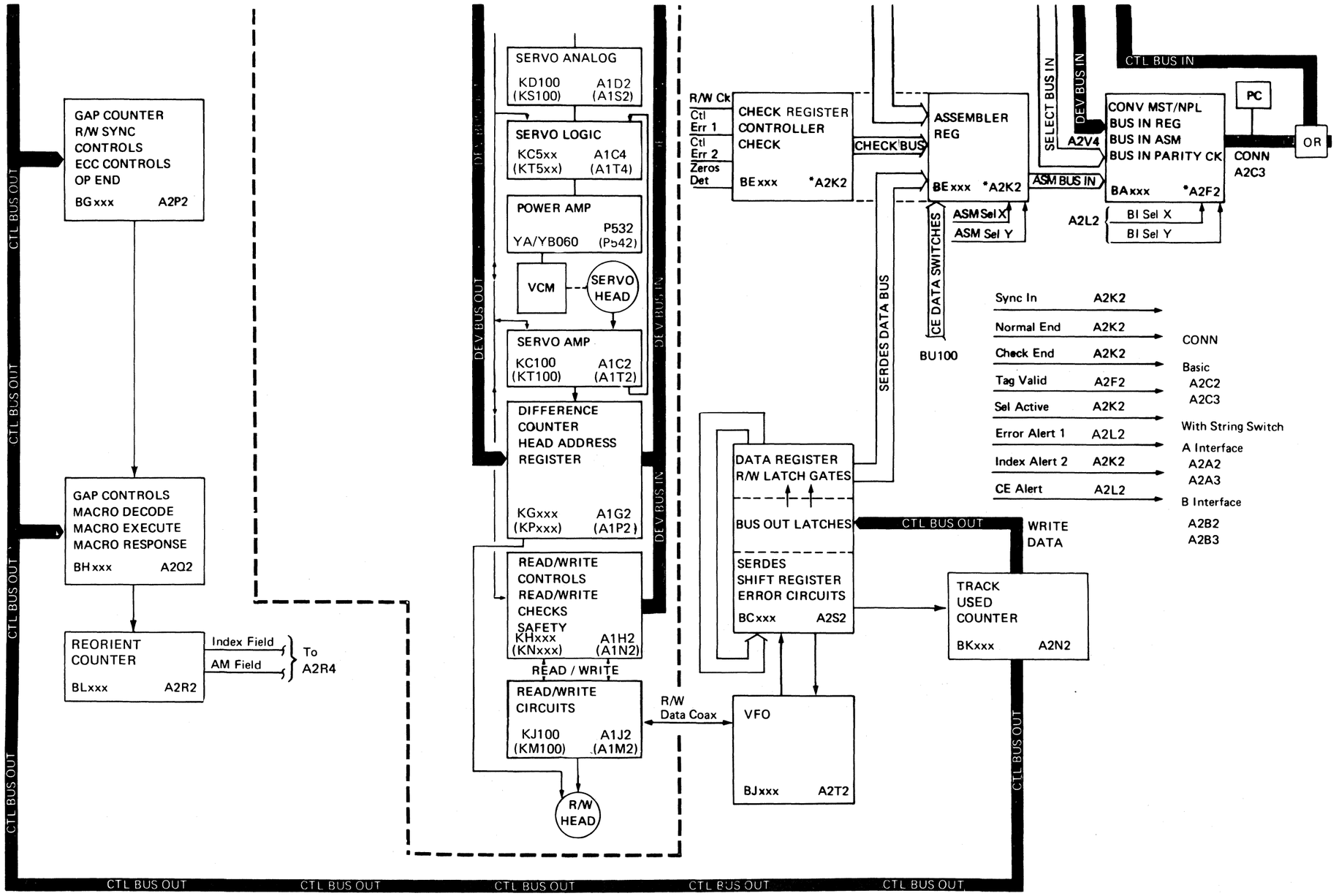

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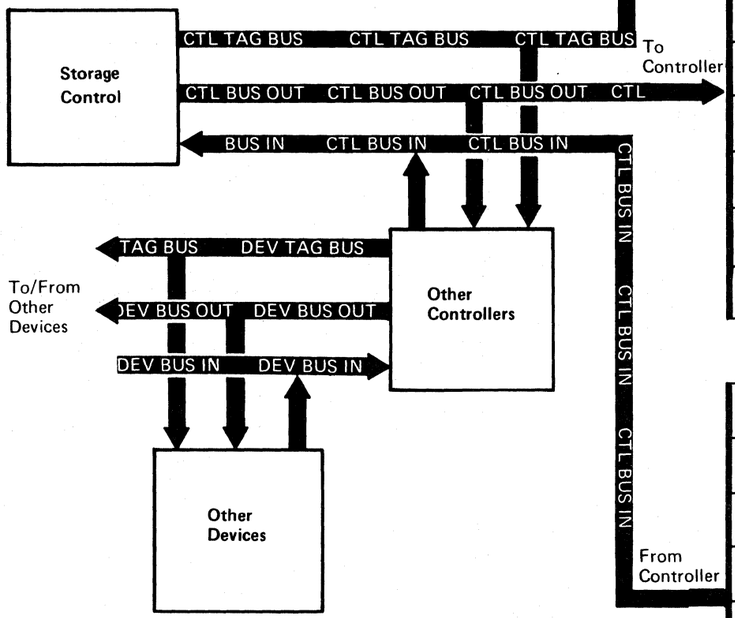
CONTROL AND DEVICE INTERFACE TAG SUMMARY

Tag Bus Decode	0	1	2	3	4	5	6	7	Operations performed by:
01–0F	0	–	–	–	X	X	X	X	Controller Only
82–86	1	–	–	–	0	X	X	X	Controller and drive
89–8F	1	–	–	–	1	X	X	X	Drive only



Tag

	Set Unsuppressible Register	Poll Controller	Select Controller	Sense Status
	01	02	03	04
0	Control 1=set, 0=reset		CA 4	All Zeros
1			CA 2	
2			CA 1	
3		Unsup-pressible		
4	Reserved	CE Poll		
5	DA 4			
6	DA 2			
7	DA 1			

CONTROL INTERFACE (CTL–I)

0												
1						ECC High						
2							High Byte Track Used					
3								Physical Address				
4									Low Byte Track Used			
5										Reorient Counter		
6											Controller Error 2	
7												Controller Error 1

Sense Status Tag '04' is modified by Ctl Bus Out. Information placed on Ctl Bus In is determined by the active bit on Ctl Bus Out.

CA = Controller Address
DA = Device Address

CONTROL INTERFACE (CTL–I)

0	Not Used	CA 0	CA 4	Command Overrun	ECC Low-Order Bits	ECC High-Order Bits	TR 8192	DA 0	TR 64		VFO Error Bit 2	Controller Tag Bus Parity
1		CA 1	CA 2	Data Overrun			TR 4096	DA 1	TR 32		VFO Error Bit 1	Controller Bus Out Parity
2		CA 2	CA 1	Lost Orientation			TR 2048	DA 2	TR 16		SERDES Data Check	Drive Select Error
3		CA 3		Trk Overrun or ECC Data Check			TR 1024	DA 3	TR 8		Gap Counter Check	Device Bus In Parity
4		CA 4		Status Overrun			TR 512	DA 4	TR 4		Write Data Check	Controller Bus In Parity
5		CA 5	$\overline{\text{CA 4}}$				TR 256	DA 5	TR 2	Index Field	Monitor Check	I Write Fail
6		CA 6	$\overline{\text{CA 2}}$	G1 Unoriented			TR 128	DA 6	TR 1	AM Field	ECC Check	TR Counter Check
7		CA 7	$\overline{\text{CA 1}}$				0	DA 7	0		ECC Zeros Detected	Reorient Counter Check

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To Controller CTL TAG BUS

Tag

To Controller CTL BUS OUT

From Controller CTL BUS IN

CONTROL INTERFACE (CTL–I)

	05	06	07	08	09	0A		0B	0C	0D	0E	0F
	Reset Read/Write	Switch Control 1 (SWFE Feature)	Switch Control 2 (SWFE Feature)	ECC Control	Transmit Control	Read Control (Information gated on Bus In controlled by bit active on Bus Out)		SYNC (RAS TP)	Display CE High	Display CE Low	Read OP	Write OP
0	0	See OPER 102	See OPER 102		Controller Reset	Device Type		Not Used	Lamp 0	Lamp 0	Modifier Bits	Modifier Bits
1	0						Data Entry Switches		1	1		
2	0				Set Diagnostic				2	2		
3	0				Reset Diagnostic				3	3		
4	0			Count 8					4	4	Count 8	Count 8
5	0			4	Diagnostic 4				5	5	4	4
6	0			2	2				6	6	2	2
7	0			1	1				7	7	1	1

Type of Read Op defined by bits 0–3:
- 0 0 0 1 Clock G3
- 0 0 1 0 Clock G2
- 0 0 1 1 Read G4
- 0 1 0 0 Read G1
- 0 1 0 1 Read G3
- 0 1 1 0 Read G2
- 0 1 1 1 Read G3 AM Search
- 1 1 1 0 Special Read G2

Type of Write OP defined by bits 0–3:
- 0 0 1 0 Write G2
- 0 0 1 1 Format Recovery
- 0 1 0 0 Format G4
- 0 1 0 1 Format G3
- 0 1 1 0 Format G2
- 0 1 1 1 Format/Erase
- 1 0 1 1 Write G4
- 1 1 0 0 Special Format G1
- 1 1 1 0 Special Write G2

Diagnostic Bit Decodes
- 000 = Invert Dev Bus In and Ctl Bus In P bit
- 001 = Invert Tag Bus P bit
- 010 = Invert Bus Out P bit
- 011 = Suppress Write Gate
- 100 = Forced Monitor Check

	0A		0B	0C	0D	0E	Tag Valid	Normal End	Check End	Tag Valid	Normal End	Check End
0	Not Used		See OPER 102	See OPER 102				0	Command Overrun		0	Command Overrun
1		CE Switch Decode 0						0	Sync Out Timing Error		0	Sync Out Timing Error
2		1					Lost Orientation	0		Lost Orientation	0	
3		2						0	ECC Data Check		0	Track Overrun
4	Both bits 4 and 5 = 3350	3					Status Overrun	0	No AM* Found	Status Overrun	0	
5		4						0	No Sync Found		0	
6		5					Read G1 Unoriented	0	Data Found		0	
7	ECC Zeros Detected	6	Undefined	Undefined	Undefined			0			0	
		7										

*Redundant ECC Data Check (See OPER 103)

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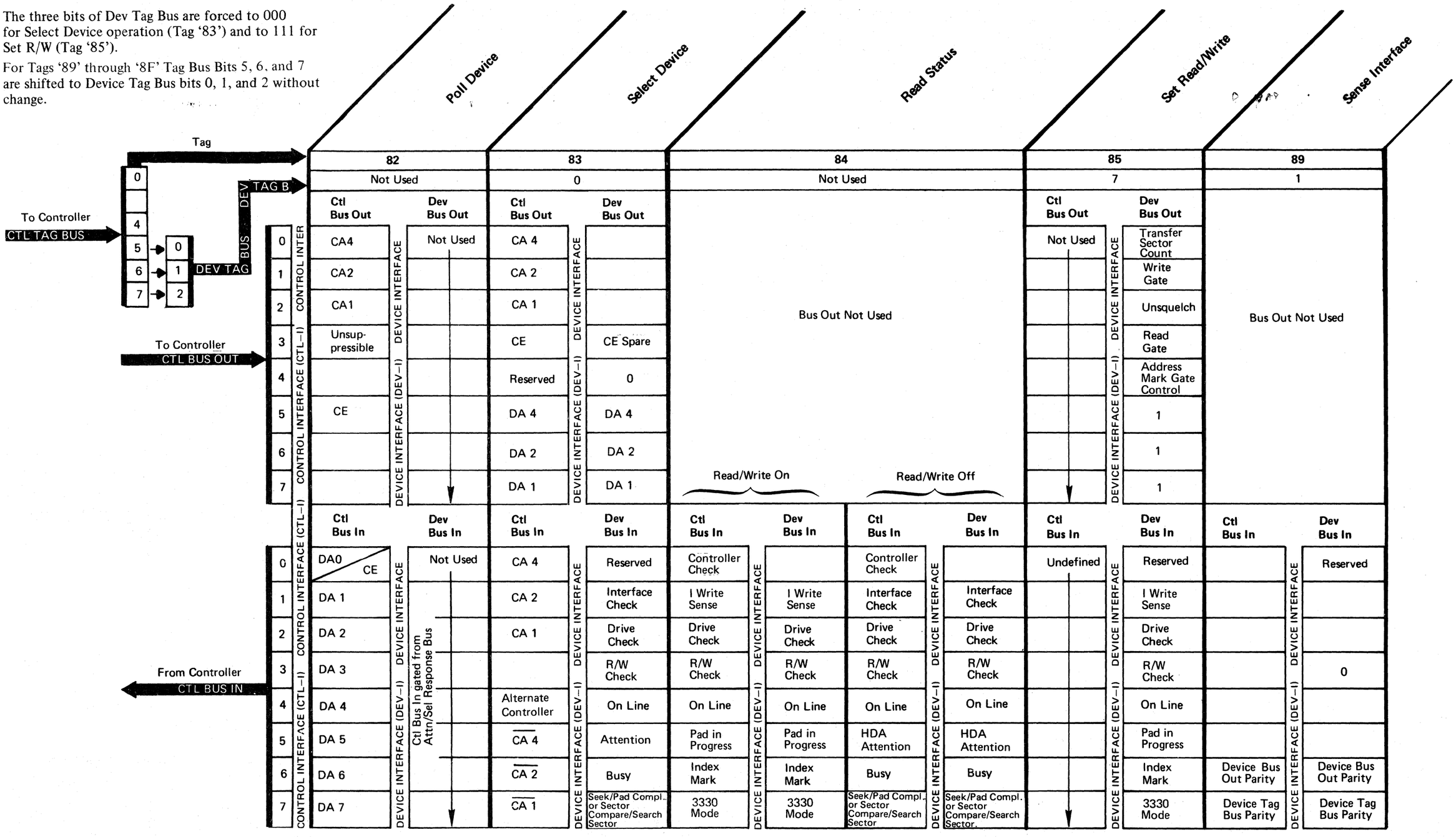
CONTROL AND DEVICE INTERFACE TAG SUMMARY

The three bits of Dev Tag Bus are forced to 000 for Select Device operation (Tag '83') and to 111 for Set R/W (Tag '85').

For Tags '89' through '8F' Tag Bus Bits 5, 6, and 7 are shifted to Device Tag Bus bits 0, 1, and 2 without change.



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CONTROL AND DEVICE INTERFACE TAG SUMMARY

For Drive Only operations '8A' through '8F', Ctl Bus Out is routed through the controller to the device without change. Dev Bus Out and Dev Bus In only are shown.

Control Tag '8F' is modified by Dev Bus Out. Information placed on Dev Bus In is determined by bits active on Dev Bus Out.

Ctl Tag → Diagnostic Set / Set HAR / Set Difference / Set Target / Set Cylinder (SWFE) / Control

Device Tag — From Controller — DEV BUS OUT

DEVICE INTERFACE (DEV–I)	8A	8B	8C	8D	8E	8F
	2	3	4	5	6	7
0	Servo Reset	Fixed Heads 32–59	Difference Counter 128	Not Used	Cylinder Address Register256	Direction 1 = In / 0 / 1 / 0 / 0 / Transfer Sector Count
1	Go Home	Fixed Heads 0–31	64	Target Register 64	128	Difference Counter 512 / 0 / 0 / 1 / 0 / 0 / Write Gate
2	Force Delta 1 W Chk	Head Address Register 16	32	32	64	Difference Counter 256 / 0 / 0 / 0 / 1 / 0 / Unsquelch/ Cue Pad
3		8	16	16	32	Cylinder Address 512 / 0 / 0 / 0 / 0 / 1 / Read Gate
4	Force Pad Gate	4	8	8	16	0 / 1 / 0 / 1 / 0 / 1 / 0 / Write Check Reset / 1 / Difference Hi / 1 / 0 / SCAR (SWFE) / 0 / Difference Counter / 1 / 0 / SHAR / 1 / Starget / 1 / 0 / Status 0 / 0 / Status 1 (Drive Check Status) / 0 / Status 2 (HDA Sequence Control) / 0 / Status 3 (Load Switch Status) / 0 / Status 4 (Access Status) / 0 / Sense Read/Write / 1 / Address Mark Gate
5		2	4	4	8	See OPER 105 / 0 / Seek Start / 0 / Attention Reset / 1 / Check Reset / 1 / Rezero / 0 / Drive Sync / 0 / Read/Write Check / 1 / Set Difference H / 1 / Sense CAR (SWFE) / 0 / Sense Difference Counter / 0 / Sense SHAR / 1 / Sense Starget / 1 / Sense Status 0 / 0 / Sense Status 1 / 0 / Sense Status 2 / 0 / Sense Status 3 / 0 / Sense Status 4 / 0 / Sense Read/Write / 0 / Diagnostic Set Read/Write / 1
6	Force Multi-Hd Chk/Rd Unsafe	1	2	2	4	0 / 0 / 0 / 0 / 1 / 0 / 1 / 1 / 1 / 0 / 0 / 1 / 1 / 1

CONTROL AND DEVICE INTERFACE TAG DESCRIPTION

SET UNSUPPRESSIBLE REGISTER — '01'

Tag '01' sets the unsuppressible register in the controller to mask certain drive addresses and block them from activating Bus In during polling. This allows some interrupt priority decisions to be made at the controller level. This tag is of the immediate class.

Bus Out bits 5, 6, and 7 contain the drive address. The appropriate latch is set when bit 0 is active and it is reset when bit 0 is inactive.

The unsuppressible register is reset during power on.

POLL CONTROLLER — '02'

Tag '02' allows all controllers to be polled for service requests. Bus Out defines the type of service request the poll is addressing. If Bus Out bits 3 and 4 are zero, a drive interrupt from any drive causes the controller to respond with the controller bit significant address on Bus In.

If Bus Out bit 3 is active, the controller responds to only those drive interrupts that have their drive addresses set in the unsuppressible register. For example, if a drive with address 3 has an interrupt, but bit 3 of the unsuppressible register is inactive, then the controller does not respond on Bus In.

If Bus Out bit 4 is active, the controller responds on Bus In with its bit significant address only if it has a CE maintenance panel request.

Tag Valid and Normal End are initiated by all controllers. This tag is of the immediate class.

SELECT CONTROLLER — '03'

Tag '03' is used when CE Panel communication is desired.

Bus Out bits 0 through 2 contain the controller address. If the address on Bus Out matches that assigned to the controller, Bus In responds with the controller address in bits 0 through 2, and its inverse in bits 5 through 7. Tag Valid, Select Active, and Normal End are activated. Bus In is checked to ensure that only one controller is selected.

If the address on Bus Out is not recognized or if either Bus Out or Tag Bus have incorrect parity, no inbound lines are activated. Parity on Bus In is guaranteed if Normal End is present.

If a device control command is issued when only the controller has been selected, no Tag Valid or end responses are present. This tag is of the immediate class.

SENSE STATUS — '04'

The Sense Status tag (Error Bytes tag) reads the drive physical address, error correction pattern, Track Used counter, Reorient counter, and controller detected errors. Bus Out defines the byte present on Bus In as follows:

0000 0000 Orientation Status Byte

All zeros on Bus Out activate Tag Valid to check the status bytes at the beginning of a Read/Write operation.

1000 0000 Gate ECC Low Byte

Bit 0 gates the ECC low-order correction byte into Bus In.

0100 0000 Gate ECC High Byte

Bit 1 gates the ECC high-order correction byte onto Bus In.

0010 0000 Gate High Byte Track Used

Bit 2 gates the high-order byte of the Track Used counter (TR counter) onto Bus In.

0001 0000 Gate Physical Address

Bit 3 gates the bit significant physical address of the drive onto Bus In.

0000 1000 Gate Low Byte Track Used

Bit 4 gates the low-order byte of the Track Used counter (TR counter) onto Bus In.

0000 0100 Gate Reorient Counter

Bit 5 gates the Reorient counter information onto Bus In.

0000 0010 Gate Controller Error 2

Bit 6 gates Error Byte 2 onto Bus In. Except for ECC Zeros Detected (Bus In bit 7), Error Byte 2 contains errors or conditions that were reported as a Controller Check in the status byte. These errors or conditions are shown on OPER 98.

0000 0001 Gate Controller Error 1

Bit 7 gates Error Byte 1 onto Bus In. Error Byte 1 contains errors or conditions reported as a Controller Check in the status byte. These errors or conditions are shown on OPER 98.

RESET READ/WRITE — '05'

Tag '05' resets the Read/Write state established by Set Read/Write. Bus In is not defined and parity cannot be guaranteed. This tag is of the immediate class.

SWITCH CONTROL 1 — '06' (STRING SWITCH ONLY)

Tag '06' sets and resets the Assignment, Device End, and Pack Change registers in the drive; it also reads the switch status.

Bus Out (See Note 1)

1100 0aaa	Assign Drive to interface
0100 0aaa	Unassign Drive from interface
1010 0aaa	Set Device End latch
0010 0aaa	Reset Device End latch
1001 0aaa	Set Pack Change latch for opposite interface.
0001 0aaa	Reset Pack Change latch for this interface.
1000 1aaa	Set the switch to neutral if locked to the opposite interface. (See Note 2)
0000 1aaa	Reset the Assignment latch in the opposite interface. (See Note 2)

Note 1: *aaa = binary drive address*
Note 2: *Bus In values below do not apply.*

Bus In

1001 0xxx	Device End Interrupt is active for this interface.
0101 0xxx	Pack Change Interrupt is active for this interface.
0011 0xxx	Addressed drive is assigned to this interface.
0001 0xxx	Connection is made through a switchable controller.
0001 1xxx	Addressed drive is assigned to the opposite interface.

If the string switch feature is not installed, no Bus In bits are active. Parity is never generated.

SWITCH CONTROL 2 — '07' (STRING SWITCH ONLY)

Long Connection is required when extended operations are to be performed (see OPER 93). Tag '07' with Bus Out modifiers sets and resets Long Connection.

The Reset Disable Interlock command activates the disabled portion of the Enable/Disable manual switch.

Bus Out

11x0 xxxx	Set Long Connection
01x0 xxxx	Unlock Switch operation (Reset Long Connection latch)
00x1 xxxx	Reset Disable Interlock

ECC CONTROL — '08'

Tag '08' is used when a Data Check has been detected to determine correctability of the data. This is done while Set Read/Write is still active. This tag is of the extended class.

TRANSMIT CONTROL — '09'

Tag '09' initiates an operation as defined by the contents of Bus Out. This tag is of the immediate class.

Bus Out bits, when active, perform the following functions:

Bit 0 — Controller Reset

Bit 0 resets all the control and the check indicator latches.

Bit 1

Not Used

Bit 2 — Set Diagnostic

Bit 2 sets the diagnostic modes as defined by the Diagnostic Decode.

Bit 3 — Reset Diagnostic

Bit 3 resets any diagnostic mode that is left set in the controller. These modes are also reset by Power On Reset and Controller Reset.

Bit 4

Reserved

Bits 5 through 7 — Diagnostic Decodes

Refer to Control and Device Interface Summary Chart (OPER 99) for decodes.

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CONTROL AND DEVICE INTERFACE TAG DESCRIPTION

READ CONTROL — '0A'

Tag '0A' reads control bytes from the controller. The contents of Bus Out define the byte presented on Bus In. Bus Out must have only one bit active. This tag is of the immediate class.

Bus Out

10xx xxxx Gate Device Type.
Gates the device type bits to Bus In if the selected device is online. Bus In bits 4 and 5 define the 3350.

01xx xxxx Gate CE Switches.
Gate contents of CE data switches onto Bus In.

SYNC — '0B'

Tag '0B' provides a scope sync. Activates Test point A2L2J11 (logic page BD100) during a Tag Gate operation.

DISPLAY CE HI — '0C'

Tag '0C' sets the eight high-order positions of the controller CE Panel lights. Bus In is not defined and parity cannot be guaranteed. This tag is of the immediate class.

DISPLAY CE LO — '0D'

Tag '0D' sets the eight low-order positions of the controller CE Panel lights. Bus In is not defined and parity cannot be guaranteed. This tag is of the immediate class.

READ OP — '0E'

Tag '0E' issues Read or Clock Data commands to the controller. Tag '0E' is an extended operation (see OPER 95).

When Tag '0E' is issued, the variable frequency oscillator (VFO) must be locked in and Set Read/Write must be active in the drive. Except for the gap codes involving HA and AM Search, all read codes can only be issued after field orientation has been previously established. The controller responds with Check End indicating Command Overrun if this is violated.

Ctl Bus Out

Ctl Bus Out defines the type of Read or Clock Data command and a count. Bits 4 through 7 contain the modulo-16 count of the number of bytes of the next data field to be transferred by the controller. Bits 0 through 3 contain the type of Read and the prefield gap preceding it. The Read and Clock Data commands are as follows:

0001 xxxx CLOCK G3
0010 xxxx CLOCK G2

Clock G3 and Clock G2 commands allow Key and Data areas to be clocked without locking to data and searching for the sync byte. The controller executes these codes by keeping the VFO locked to servo and simulating a Write G3 or G2 operation with the Write Gate off. Sync In occurs then as if the field were being written. The data on Bus In is valid and therefore parity is not generated.

0011 xxxx READ G4

Read G4 is used for defect skipping. It is used to extend a gap by 128 bytes following the Special Read G2 code.

0100 xxxx READ G1

Read G1 allows orientation on Home Address. This code is executed in two ways. If the gap counter is counting from Index and has not reached byte 63, the execution proceeds immediately. If the counter is past byte 63 or if the counter is not running, the execution is delayed until Index occurs. This code never overruns the command. If no sync byte is located before the normal position of HA on the track, a second attempt to read a sync byte is made 128 bytes later. No Sync Found and Check End occur if the second attempt fails.

0101 xxxx READ G3
0110 xxxx READ G2

Both codes (Read G3 and Read G2) involve locking VFO to data sequence at the proper point in the gap, searching for sync bytes, and if successful, transferring the data read and processing the ECC bytes. The difference between Read G2 and Read G3 is that the Read G3 sets the gap counter to process a G3 prefield gap whereas the Read G2 implies a G2 prefield gap. Also, the Transfer Sector Counter line is only activated during execution of the Read G3 code.

0111 xxxx READ G3 AM SEARCH

Read G3 AM Search initiates an address mark search sequence. Once an Address Mark is found, the execution is the same as a Read G3 code. Field orientation is established when Address Mark (AM) is found. Transfer Sector Count line to the drive is activated when an AM is found.

1110 xxxx SPECIAL READ G2

Special Read G2 is the same as Read G2 except that it denotes there is an inter-record gap following and that there is no ECC at the end of the field.

Ctl Bus In

Ctl Bus In is valid for each Sync In as denoted for data transfer after each gap definition. In addition, Bus In is valid for Tag Valid, Normal End, and Check End.

TAG VALID

Information is gated onto Bus In for Command Overrun control.

Bit 0: Not Used

Bit 1: Not Used

Bit 2 Lost Orientation: Indicates that orientation is not established when the Read or Write operation is issued.

Bit 3: Not Used

Bit 4 Status Overrun: Indicates that Tag Gate is active too late for the operation to continue successfully. It usually means that the channel has not responded to Status In on a chained Read or Write operation.

Bit 5: Not Used

Bit 6 G1 Unoriented: Indicates that a Read G1 operation has been issued when the controller is not oriented, that is, not in a G1 gap area.

Bit 7: Not Used

NORMAL END

Normal End is raised after the last ECC byte or last byte of a skipped record has been transferred and no error condition has been detected. Bus In is all zeros with correct parity.

CHECK END

Check End is raised if an unusual condition occurs. Bus In is never zero when Check End is active. The conditions causing Check End are as follows:

Bit 0 Command Overrun: Bus In bit 0 is set if the Read operation is not received at the controller before the gap counter reaches byte count 71. The Read G1 and Read G3 AM Search codes are exceptions since they do not have an overrun point. The Check End lines rise after Tag Gate falls at the controller. Since the gap counter stops running when Command Overrun occurs, record orientation is lost. Bit 0 is reset by Response.

Bit 1 Sync Out Timing Error: Bus In bit 1 is set if there is a late or extra response to a Sync Out. Data transfer stops when this condition is detected. Bit 1 is reset by Response.

Bit 3 ECC Data Check: Bus In bit 3 is set if (after processing the ECC bytes) the ECC hardware indicates a data check. This bit is not reset until the next Read or Write operation.

Bit 4 No AM Found/ECC Data Check: Bus In bit 4 is set as an end condition of the Read G3 AM Search code if an AM is not found. It is also set as a redundant ECC Data Check with bit 3. Bit 4 is reset by Response.

Bit 5 No Sync Found: Bus In bit 5 is set if the controller does not find a sync byte. This does not apply to Clock G3 and Clock G2 codes. Bit 5 is reset by Response.

Bit 6 Data Found: Bus In bit 6 is set if at least a single bit was found from the start of a sync byte search. This bit is only gated to Bus In if bit 5 (No Sync Found) is on. Bit 6 is reset by Response.

ERROR ALERT CONDITIONS

Error Alert Condition is activated whenever an error condition is detected that is not covered by Check End. The Error Alert (Selected Alert 1) line may become active at any time and may accompany Tag Valid, Normal End, or Check End. Except for drive selection errors, any condition that sets Error Alert is latched for examination under the Status and Error bytes.

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WRITE OP — '0F'

Tag '0F' issues Write commands to the controller. This tag is an extended operation (see OPER 95).

When this tag is issued, The VFO is locked in as a result of the Set Read/Write tag. If the VFO is not locked in, Error Alert reports a VFO error.

Except for the Format G1 code, all other write codes may only be issued after a field orientation on the active portion of the track has been previously established. If this requirement is not satisfied, the controller responds with Check End, and Command Overrun is noted on Bus In. The Format Write operations cause Write Gate to be set at a predetermined point on the track. From this point Write Gate remains active until Index is detected. If subsequent format operations are not activated, zeros are padded throughout the rest of the track. Write Gate is also dropped with Reset Read/Write or the fall of Select Hold. When a format command has been executed, all subsequent Write commands are executed as format commands. When required, the controller writes the following: the address marker, sync byte, data transferred from storage control, ECC bytes, and gaps. Data transfer is initiated with a Sync In when the controller starts to write the sync byte. The ECC bytes are written immediately following the end of data transfer. ECC hardware sequence is handled by the controller. The normal updating Write command causes Write Gate to be set at a predetermined point in the gap and to be reset at the end of the field after the ECC bytes have been written.

Bus Out

Bits 0 through 3 contain the type of Write command (modifiers) to be performed and the prefield gap associated with it. Bits 4 through 7 contain the modulo-16 residual count of the number of bytes of the next field to be transferred to the controller. This count is loaded into the controller data transfer counter. Following is a summary of the Write modifiers.

0010 xxxx WRITE G2

Bit 2 writes a G2 prefield gap. Write Gate is turned off at the end of the data field.

0011 xxxx FORMAT REORIENT

The Format Reorient tag reorients the R/W head on the track when a count field is reached that contains a defect skip within its control. The count field must be rewritten once this is determined. The command is issued in the gap following the count field. Sync In is presented and padding is continued to Index.

Sync In continues to the reorientation point. The count used to reorient ahead of the R0 count field is 19,785 bytes and 19,782 bytes when ahead of other fields. This places the orientation just after the last byte before the ECC bytes of the data field and prior to the desired count field. Normal End is presented in the normal manner.

0100 xxxx FORMAT G1

This code causes the controller to search for Index. G1 is formatted and Home Address is written according to the data transfer. The Transfer Counter line to the drive is activated at byte 63 in the gap.

0101 xxxx FORMAT G3

The Format G3 tag writes a G3 prefield gap and writes the Address Mark. The Transfer Counter line to the drive is activated at byte 63 in the gap.

0110 xxxx FORMAT G2

This code is the same as the Write G2 code. It is used to write a G2 prefield gap. Write Gate is turned off at the end of the data field.

0111 xxxx FORMAT ERASE

This code causes zeros to be written to Index and turns off the Write Gate. Clocking continues until Recycle drops and the modulo-16 count has decremented to zero or Index is detected. Track overrun is presented during this command when Index is detected.

1011 xxxx WRITE G4

This code is used to extend a gap before the gap definition is presented (to skip a defect).

1100 xxxx SPECIAL FORMAT G1

This code causes a search for Index and Active Track. When found, 128 bytes of zeros are written. After this, the controller continues writing the Format G1.

1110 xxxx SPECIAL WRITE G2

This code allows a following gap without ECC bytes at the end of the data field. Write Gate is turned off after the last byte of data.

Bus In

Bus In is valid when Tag Valid, Normal End, or Check End is active.

TAG VALID

Bits 0 and 1: Not Used

Bit 2 Lost Orientation: Indicates that orientation is not established at the time the Read or Write operation is issued.

Bit 3: Not Used

Bit 4 Status Overrun: Indicates that Tag Gate is active too late for the operation to continue successfully. It usually means that the channel has not responded to Status In on a chained Read or Write operation.

Bit 5: Not Used

Bit 6: Not Used

Bit 7: Not Used

NORMAL END

Normal End is raised if the Check End condition does not exist after the last byte of the ECC field is written. Bus In is set to zero.

CHECK END

Bus In is never zero when Check End is raised. Check End is raised if one of the following unusual conditions occur:

Bit 0 Command Overrun: Bus In bit 0 is set if the command is not received at the controller before the gap counter reaches byte count 63 (for operations requiring maintained operation).

Bit 1 Sync Out Timing Error: Bus In bit 1 is set if Sync Out arrives too late to service a byte of data. If Write Gate is active, it is turned off.

Bit 3 Track Overrun: Bus In bit 3 is set if the index point is detected while a field is being written. The field includes the prerecord gap through the end of the ECC bytes. Write Gate is dropped and Check End is raised when Index is detected, except when Format G1 is being processed.

ERROR ALERT

Error Alert is raised whenever an error condition is detected that is not covered by Check End. The alert line may rise at any time.

POLL DEVICE — '82'

Tag '82' allows the drives of the addressed controller to be polled for service requests and can only be issued when no drive is selected on the control interface. Bus Out bits 0 through 2 contain the address of the desired controller. The controller responds with Tag Valid and Normal End if there is no Bus Out or Tag Bus parity error. If Bus Out bit 3 and 5 are zero, the presence of a drive interrupt from any drive causes the bit significant address of that drive to be activated on Bus In.

If Bus Out bit 3 is active, the drive address for which an interrupt exists is only seen on Bus In if the corresponding address in the controller unsuppressible register is set. For example, if a drive with address 7 has an interrupt, Bus In bit 7 is only activated if bit 7 of the unsuppressible register is set.

Bit 5 on Bus Out polls requests from only the drive in the service mode. Bus In bit 0 indicates a request is present. Bus Out bit 3 (unsuppressible) is not defined when polling the service drive and should not be used.

Parity on Bus In is not guaranteed for Poll Device. This tag is of the immediate class.

SELECT DEVICE — '83'

Tag '83' is used to select both a controller and a drive. Bus Out contains the address of the controller and the logical drive address. The controller generates the selection sequence to the drive. Bus Out to the controller is gated on Bus Out to the drive for the logical drive address contained in bits 5 through 7. The controller responds to this tag with Tag Valid, Select Active, and Normal End if the address on Bus Out matches that assigned to the controller and if Tag Valid is received from the device. Tag Valid is returned from the device to the controller if a drive is selected and there are no device Tag Bus or Bus Out parity checks. Bus In contains the controller address (bits 0–2) and its inverse (bits 5–7) if selection is successful. Bit 4 is active if the alternate controller is selected. When Bus Out bit 4 = 1, drive selection is blocked. Bus Out bit 3 = 1 causes drive in CE Mode to be selected while ignoring bits 5 through 7. If the address on Bus Out is not recognized, or if either Bus Out or Tag Bus have incorrect parity, no inbound lines are activated. This tag is of the immediate class.

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CONTROL AND DEVICE INTERFACE TAG DESCRIPTION

READ STATUS — '84'

Tag '84' causes the controller to transmit the drive status onto Bus In bits 1 through 7. The tag does not affect the drive. The Controller Check bit is transmitted on Bus In bit 0. The drive status has some differences when Set Read/Write is active. Refer to Control and Device Interface Tag Summary chart on OPER 100 for a summary of the status bits with Set Read/Write active and inactive. This tag is of the immediate class.

Correct parity on Bus In is not guaranteed because of the asynchronous state of the information presented.

SET READ/WRITE — '85'

Tag '85' sets the Read/Write control in the controller and synchronizes the VFO with Servo Pulses from the activated drive. The Read/Write control to the device is established as follows:

1. Device Tag Bus bits 0, 1, and 2 are forced to all 1s.
2. Device Bus Out bits 5, 6, and 7 are forced to all 1s.
3. Device Bus Out bits 0 through 4 are conditioned so the various Read and Write controls may be transmitted to the device.
4. Device Tag Gate is forced on.
5. The Device Bus Out parity checker is blocked after Set Read/Write is decoded in the device.
6. Upon detection of Index, the Read/Write controls are blocked for approximately 63 microseconds. This allows the microprogram to set the head address register to a new value during multitrack Read or Search operations.

It is expected that after this tag is issued, Read operation (Tag '0E') or Write operation (Tag '0F') will be issued.

The Read/Write controls are reset by:

1. Reset Read/Write operation (Tag '05').
2. Controller Reset (Tag '09', Bus '80').
3. Dropping Select Hold.

Tag '85' is of the extended class and Normal End usually signals that the Read/Write logic is ready. Check End is not possible.

Bus In is not defined and parity cannot be guaranteed.

SENSE INTERFACE — '89'

Tag '89' determines the cause of a Device Interface check. Bus In bits 6 and 7 indicate:

Bit 6 — Device Bus Out Parity Check.
Bit 7 — Device Tag Bus Parity Check.

This tag forces Tag Valid even though the Device Interface checks are present. The Device Bus Out and Device Tag Bus Parity Check latches are reset when Tag Gate drops.

This tag is of the immediate class. Bus Out is not used.

DIAGNOSTIC SET — '8A'

Tag '8A' is used in conjunction with Device Bus Out to set the selected drive into predefined hardware states to aid troubleshooting.

Device Bus Out

10xx 0x00 SERVO RESET

Servo Reset forces the Servo into Zero mode and inhibits access movement or track following control while the tag is active.

01xx 0x00 GO HOME

Go Home causes the access mechanism to go to the home position, fully retracted into the Head/Disk Assembly (HDA).

001x 0x00 FORCE DELTA I W CHECK

Force Delta I W Check forces a Delta I W Check when an inner (odd-numbered) head is selected.

00xx 0x10 FORCE PAD GATE D CHECK

Force Pad Gate causes the device padding function to operate under diagnostic control.

00xx 0x10 FORCE MULTIHEAD CHECK

The Force Multihead Check command sets the Odd Head latch in the drive. A subsequent Set Read/Write command forces Multihead Check if HAR bit 6 is off.

00xx 0x01 DECREMENT DIFFERENCE COUNTER

Decrement Difference Counter causes the difference count to be decreased by one each time Diagnostic Set Tag is applied with Device Bus Out bit 7 active.

SET HAR — '8B'

Tag '8B' is used to transfer the Head Address.

Bits 0 and 1 — Fixed Heads

Bit 0 is on when any one of the 30 fixed heads from 32 to 59 is addressed. Bit 1 is on when any one of the fixed heads from 0 to 31 is addressed.

Bits 2–6 — Head Address

SET DIFFERENCE — '8C'

Tag '8C' loads the Difference Counter of the selected drive. The Difference Counter is loaded with the difference between the current cylinder address and the desired cylinder address as calculated by the controlling system. The 256 bit and the 512 bit of the Difference Counter are loaded with Control Tag '8F' Bus 'xE'. The difference value, including the 256 and 512 bits, must be set at least 8 microseconds before a Seek Start is issued.

SET TARGET — '8D'

Tag '8D' transfers a sector number to the Target Register of the selected drive for rotational position sensing. The drive immediately begins to perform a Search Sector operation to compare the Target Register with the Sector Counter to find a match.

SET CYLINDER — '8E'

Tag '8E' loads the Cylinder Address Register (CAR). CAR is not functionally connected to the access mechanism; it serves only as a storage register to contain current position information of the access mechanism to be used with the string switch feature of the controller. CAR is reset by a Rezero operation to indicate that the heads are positioned over track 0.

CONTROL — '8F'

Tag '8F' transfers control information to the selected drive. Under this tag, the Device Bus Out is divided into two groups of four bits each. Device Bus Out bits 4 through 7 are coded to perform 14 different functions. Bits 0 through 2 are interpreted to further control certain of these functions. Refer to Control and Device Interface Tag Summary chart on OPER 101. The functions are:

No-op	Sense Cylinder
Seek Start	Sense Difference Counter
Attention Reset	Sense Head Register
Check Reset	Sense Target Register
Rezero	Sense Status
Drive Sync Tag	Sense Read/Write
Read/Write Check Reset	Diagnostic Set Read/Write
Set Difference Hi	

xxxx 0000 No-op

The drive sees this tag as a No-op, but status as under tag 84 is returned to storage control. Some storage control types use this tag/bus combination to obtain status.

xxxx 1000 Seek Start

Seek Start causes the drive to move the Read/Write heads as specified by the information contained in the Difference Counter and Head Address Register. The Difference Counter and the Head Address Register must previously have been set. If the difference count is zero, no physical accessing occurs, and the completion of the zero track Seek is signaled immediately. Completion of the action initiated by Seek Start is signaled by Attention. At the termination of a Seek, the Seek Complete status bit in the machine status is on. An Access failure is indicated by the Drive Check bit being active with Attention.

xxxx 0100 Attention Reset

Bit 5 resets the attention signals in the selected drive. To prevent masking of attention signals, Attention Reset should be performed to reset attentions already present prior to the initiation of an operation resulting in an attention. Attention Reset also cancels pending Seek Rezero or Search Sector Attentions.

xxxx 1100 Check Reset

This code resets check conditions in the selected drive including Read/Write checks.

xxxx 0010 Rezero

Bit 6 causes the drive to place the heads over track 0 with HAR and Difference Counter reset to zero, which is the same condition as that after a head/disk assembly has completed a load sequence. Rezero is a low-speed operation used to recover to a known track position after a seek error has occurred. Check Reset must be issued prior to a Rezero operation if an Access check is present in the drive. The response of the drive to the controller after completion of this control function is similar to Seek Start.

xxxx 1010 Drive Sync Tag

Drive Sync Tag causes A1C2G02 to shift to a minus level (MST-1). The microdiagnostics use this to provide oscilloscope sync pulses.

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CONTROL AND DEVICE INTERFACE DESCRIPTION

xxxx 0110 Read/Write Check Reset

Read/Write Check Reset causes these common Read/Write Checks to be reset:

- Multihead Check
- Capable/Enable Check
- Write Overrun
- Index Check
- Interlock Check
- Control Check
- Transition Check
- Write Current Check

yyyy 1110 Set Difference Hi

Set Difference Hi is used to load yyyy (yyyy=Bus Out bits 0–3):

Bit 0 – Direction (1=in)
Bit 1 – Difference count 512
Bit 2 – Difference count 256 (Bits 2 and 3 are extensions of the difference counter. See Tag '8C'.)
Bit 3 – CAR bit 512. (This is an extension of cylinder address register. See Tag '8E'.)

xxxx 0001 Sense Cylinder

Sense Cylinder causes the contents of the cylinder address register to be presented on the Device Bus In.

xxxx 1001 Sense Difference Counter

Sense Difference Counter causes the contents of the difference counter to be presented on the Device Bus In.

xxxx 0101 Sense Head Register

Sense Head Register causes the contents of the head register to be presented on Device Bus In.

xxxx 1101 Sense Target Register

Sense Target Register causes the contents of the target register to be presented on the Device Bus In.

xxxx 0011 Sense Status

Sense Status causes one of five drive status bytes to be placed on Device Bus In as determined by bits 0 through 3 of Device Bus Out. For a summary of each of the status bytes, refer to the Control and Device Interface Summary Chart on OPER 101.

xxxx 1011 Sense Read/Write

Sense Read/Write presents Read/Write check conditions on the Device Bus In. Refer to OPER 101 for Bus In bit significance.

xxxx x111 Diagnostic Set Read/Write

Diagnostic Set Read/Write causes bits 0 through 4 of the Device Bus Out to control Read/Write functions in the device. While the Set Read/Write Control function is present, parity checking of Device Bus Out by the drive is disabled and Read/Write status of the drive is presented on Device Bus In. Refer to the Control and Device Interface Summary Chart on OPER 101 for the drive status on Device Bus In.

During a normal Set Read/Write, (see Set Read/Write Tag '85' on OPER 105), the controller hardware controls the action of the bits on Device Bus Out. During a Diagnostic Set Read/Write (Tag '8F', Bus xxxx x111) the diagnostic microprogram must control the bits on Device Bus Out.

The control functions under Device Bus Out are as follows:

Bit 0 Transfer Sector Count: The contents of the sector counter are transferred to the target register for later readout.

Bit 1 Write Gate: When active, (along with bit 4) Address Mark Control causes writing to be performed on the head/disk assembly. Read/Write Checks prevent writing.

Bit 2 Unsquelch/Cue Pad: During Read operations, bit 2 causes squelch to be removed from the read amplifier to allow read data operations. During Write operations, bit 2 conditions the file to pad to Index independently of the controller.

Bit 3 Read Gate: Causes the read amplifier, read detector, and data line drivers to be set to Read mode. Read/Write checks prevent Read operations.

Bit 4 Address Mark Control: In Read mode, the read detector is set to detect Address Marks. In Write mode, it must be used with Write Gate to allow writing on the head/disk assembly.

Bits 5 through 7: Must be ones.

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INTERFACE SEQUENCING

A timing chart of a typical control and device interface operation is shown on OPER 108 and 109. A Seek operation (OPER 108) followed by Polling and a Seek Complete Attention (OPER 109) shows the sequence of events that take place on the Bus In, Bus Out, and Tag Bus.

The charts on OPER 98 through 101 show the data on each bus for both interfaces, and for each tag and modifier issued. Note that some tags do not use the device interface. See OPER 102 through 106 for tag descriptions and OPER 95 for tag considerations.

BUS OUT

The Control Interface Bus Out is sent to the Device Interface Bus Out at all times except during Read/Write mode.

TAG BUS

The Device Tag Bus uses a register to transmit tags to the device as follows (see diagram):

1. Selection Tag '83' causes the register to reset. Since the register is not clocked and neither the G1 nor G2 input is active, the register is reset to zero. Tag '83' also activates Tag Gate.
2. Tags with bits 0 and 4 on are device tags (Tags '89' through '8F'). These tags activate the G1 gate to the register. The active Control Interface Tag Bus bits 5,6, and 7 are set into the register and become Device Tag Bus bits 0,1, and 2. Selected Tag Gate activates Device Tag Gate.
3. Read/Write mode activates the G2 inputs and sets all output Device Tag bits on. Read/Write mode also forces Device Tag Gate.
4. Controller Tags ('00' through '85', except '83') do not affect the register settings. Device Tag Gate is not activated.

SEEK OPERATION

The timing chart of a Seek operation on OPER 108 shows a typical sequence of interface operations and controller and device interaction for a storage-control-initiated operation.

The timing chart is based on a 3830-2 using a microprogram disk that has string switch code and 3340s with or without the string feature.

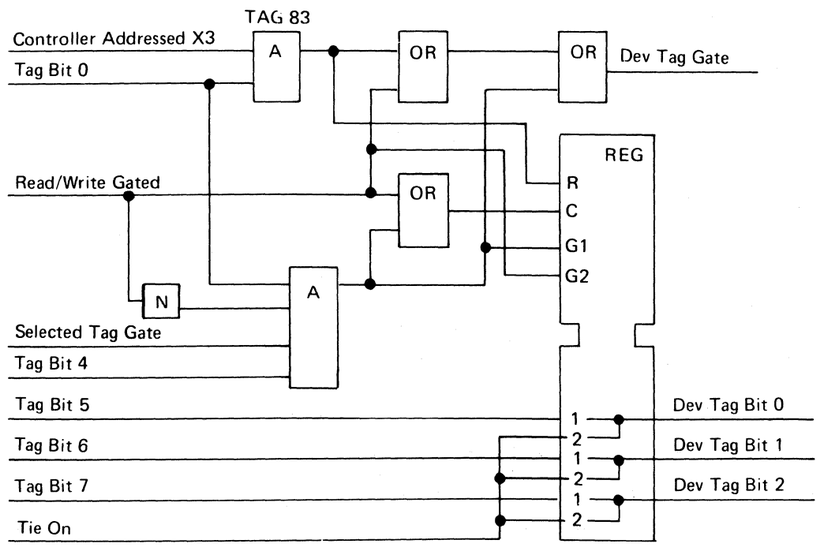
A Start I/O with a Seek command is issued by the CPU. The storage control selects the addressed device and makes certain checks of the device such as status, features, and device type. The direction and length of the Seek are computed and sent to the device along with the Read address. These values are verified by a read-back check. Cylinder address values are also transmitted and are verified if the string switch feature is installed. If no errors are encountered, the access is started. As soon as the device becomes Busy, it is de-selected and finishes the operation independently. The storage control returns to Polling mode to await either an Attention from the device or a channel command.

SEEK COMPLETE ATTENTION

The timing chart on OPER 109 illustrates Polling with a device-initiated sequence of interface operations.

The timing chart is based on a 3830-2 using a microprogram disk that has string switch code and 3340s with or without the string switch feature.

The storage control, when idle, polls all of the attached controllers for outstanding Attentions. If an event such as a Seek Complete has occurred, the device places its Bit Significant Device Address (BSDA) on the Attention/Select Bus to the controller (BSDA equals bit 0 for device 0, bit 1 for device 1, etc.). When the controller is polled, it places the BSDA on the Control Interface Bus In. The storage control then selects the first device and interrogates it (Read Status Tag '84') to determine the type of Attention. The Attention is stacked (not reset) as indicated on the timing chart or reset depending upon the storage control/channel requirements.



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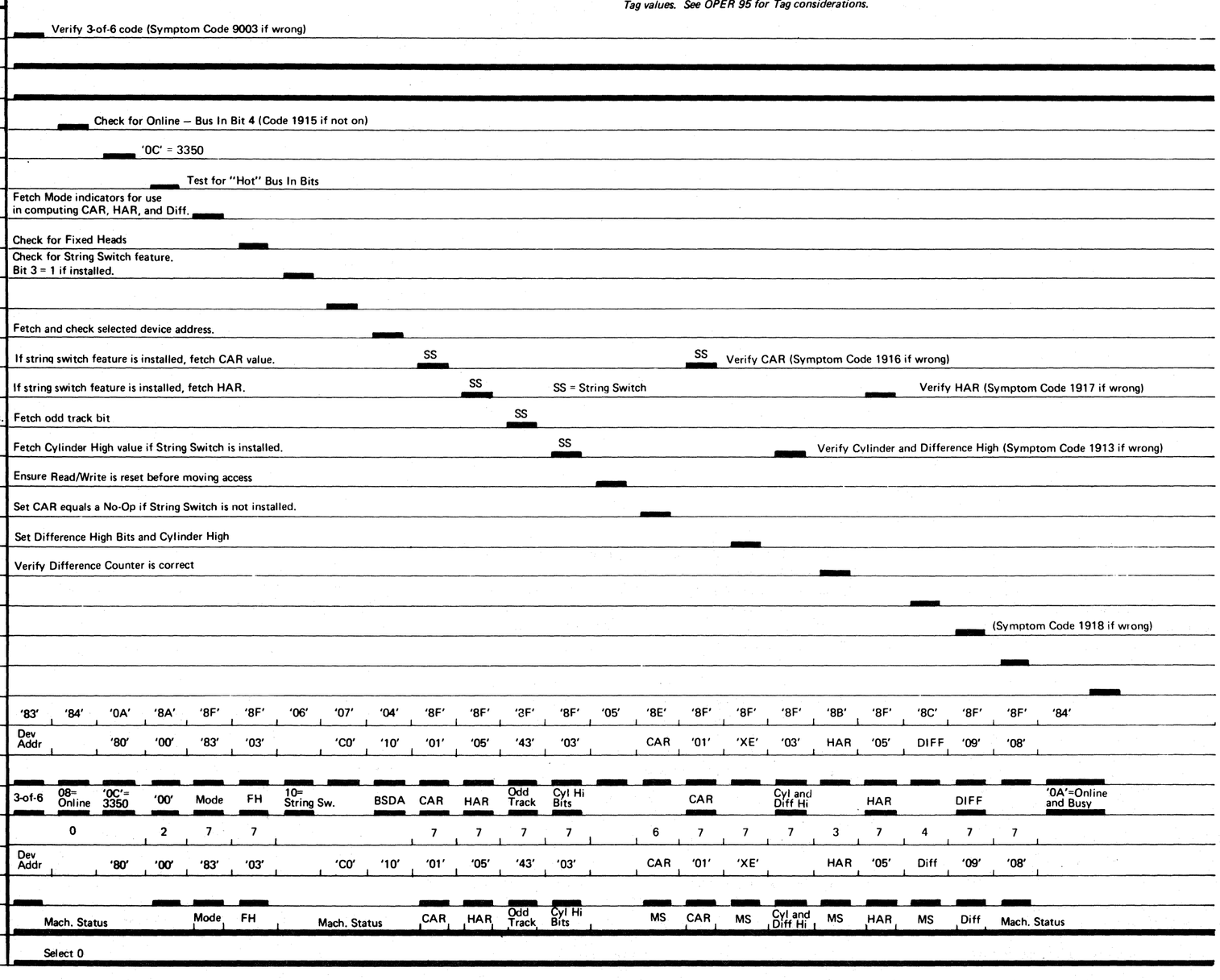
Seek Operation

Line Name	Control Interface*			Device Interface*		
	Tag Bus	Bus Out	Bus In	Tag Bus	Bus Out	Bus In
Select Tag	'83'	Addr.	3 of 6	0	Addr.	Mach Status
Select Hold	–	–	–	–	–	–
Selected	–	–	–	–	–	–
Read Status	'84'	–	Mach Status	–	–	Mach Status
Gate Device Type	'0A'	'80'	'0C'	–	–	Mach Status
Diagnostic Set	'8A'	'00'	'00'	'2'	'00'	'00'
Sense Status 1	'8F'	'83'	HDA Size	'7'	'83'	HDA Size
Sense Status 0	'8F'	'03'	Fixed Head	'7'	'03'	Fixed Head
String Switch	'06'	–	'00' or '10'	–	–	Mach Status
Set Long Connection	'07'	'C0'	–	–	–	Mach Status
Gate Physical Address	'04'	'10'	BSDA	–	–	Mach Status
Sense Cylinder Address Register	'8F'	'01'	Cyl Addr.	7	'01'	Cyl. Addr.
Sense Head Address Register	'8F'	'05'	Hd Addr.	7	'05'	Hd Addr.
Sense Status 2	'8F'	'43'	Odd Track etc.	'7'	'43'	Odd Track etc.
Sense Status 0	'8F'	'03'	Cyl Hi Bits	'7'	'03'	Cyl Hi Bits
Reset Read/Write	'05'	–	–	–	–	Mach Status
Set Cylinder Address Register	'8E'	Cyl. Addr.	–	'6'	Cyl. Addr.	Mach Status
Set Difference High	'8F'	'XE'	Diff High	'7'	'XE'	Diff High
Set Head Address Register	'8B'	Hd Addr.	–	3	Hd Addr.	Mach Status
Set Difference Counter	'8C'	–	–	4	–	Mach Status
Sense Diff	'8F'	'09'	Diff	7	'09'	Diff
Seek Start	'8F'	'08'	–	7	'08'	Mach Status
Busy	–	–	–	–	–	–

* *See OPER 98 – 106 for a complete description of Bus and Tag values. See OPER 95 for Tag considerations.*



Control Interface Tag Bus
Control Interface Bus Out
Control Interface Tag Gate
Control Interface Bus In
Device Interface Tag Bus
Device Interface Bus Out
Device Interface Tag Gate
Device Interface Bus In
Device Interface Attention/Select Bus

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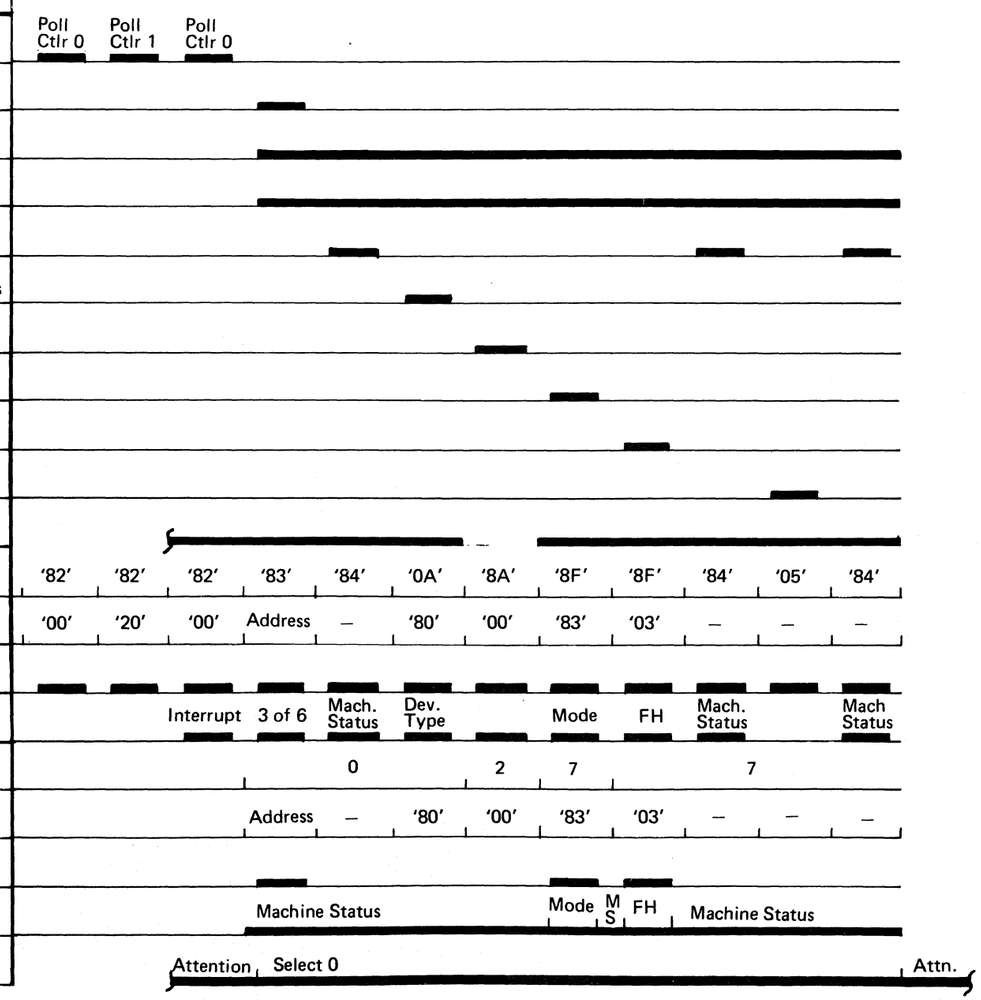
Seek Complete Attention

	Control Interface*			Device Interface*		
	Tag Bus	Bus Out	Bus In	Tag Bus	Bus Out	Bus In
Poll	'82'	Ctrl Addr	Intrpt Addr	–	–	–
Select Tag	'83'	Addr	3 of 6	0	Addr	Mach. Status
Select Hold	–	–	–	–	–	–
Selected	–	–	–	–	–	–
Read Status	'84'	–	Mach. Status	–	–	Mach. Status
Gate Device Type	'0A'	'80'	'0C'	–	–	Mach. Status
Diagnostic Set	'8A'	'00'	'00'	2	'00'	'00'
Sense Status 1	'8F'	'83'	Mode	7	'83'	Mode
Sense Status 0	'8F'	'03'	FHF	7	'03'	FHF
Reset Read/Write	'05'	–	–	–	–	–
Seek Complete	–	–	–	–	–	–



** See OPER 98 through 106 for a complete description of Bus and Tag values. See OPER 95 for Tag considerations.*

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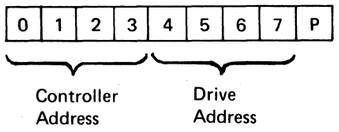
SELECT OPERATION

This page describes the diagram on OPER 111.

UNIT SELECTION

The unit address consists of an 8-bit byte plus parity. Bits 0 through 3 contain the address of a controller. Bits 4 through 7 contain the address of a drive.



To select a drive:

1. Storage control places Tag '83' on Ctl Tag Bus 1. Tag '83' indicates that an address is on Ctl Bus Out 1.
2. Each controller decodes Tag '83' 4.
3. Storage control places a unit address (a controller address and a drive address) on Ctl Bus Out 1. (Ctl Bus Out bit 3 is zero.)
4. Storage control activates Tag Gate and then Select Hold 3.
5. Each controller compares its prewired 3-bit address and Bus Out bits 0 through 2 7.
6. Comparison is successful in the controller when Controller Addressed becomes active. This sets the Select Ctlr latch 5 and causes Select Active 8 to be sent from the selected controller to storage control.
7. The selected controller places its prewired 3-bit address on Selection Bus bits 0 through 2 and the inverted prewired 3-bit address on Selection Bus bits 5 through 7, (3-of-6 code) 11. Selection Bus bits 0 through 2 and 5 through 7 are placed on Ctl Bus In by the Bus In Assm 13.
8. The selected controller generates Dev Tag Bus Tag (000) from Ctl Tag Bus Tag '83' 2.
9. Each drive attached to the selected controller generates Select Gate 6 from Tag bits 0 through 2 (000).
10. Each drive compares its prewired 3-bit address and MST Outbus Bits 5 through 7 9.
11. Comparison will be successful in one drive where Drive Addressed becomes active. This sets the Select Drive latch and activates Selected A (B) 10.
12. Selected activates NPL Attn Sel Resp drive x A (B) which activates the drive address bit on the Attention/Select Response Bus 12. (Bit 0 = drive 0, bit 1 = drive 1, etc.) Selected also gates Tag Gate Valid to the controller.
13. A Sense Physical Address tag (Ctl Tag Bus '04' and Ctl Bus Out '10') gates the Attention/Select Response Bus through the Bus In Assm onto Ctl Bus In 13.
14. The controller sends Tag Valid 14 and Normal End 15 to storage control.

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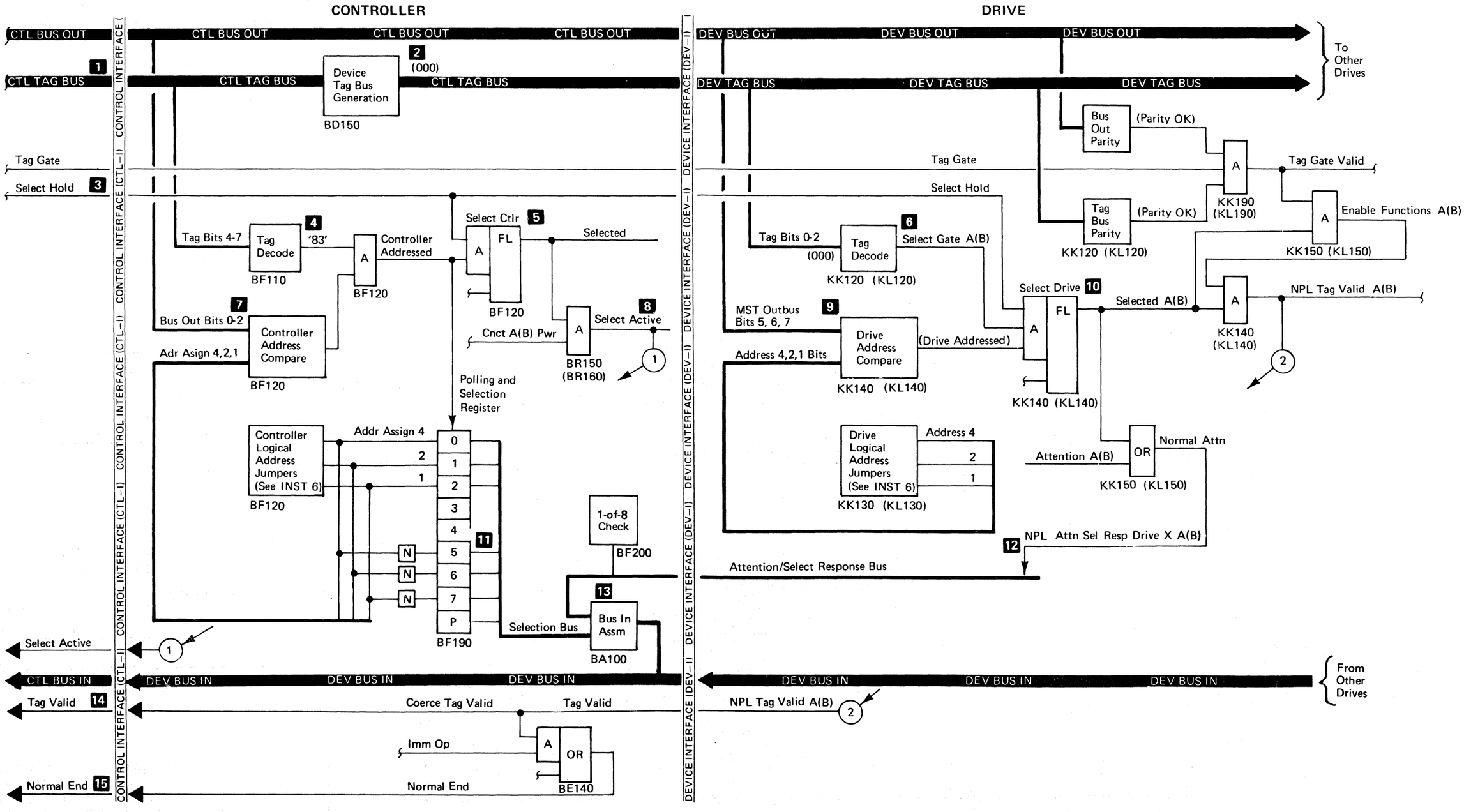
SELECT OPERATION



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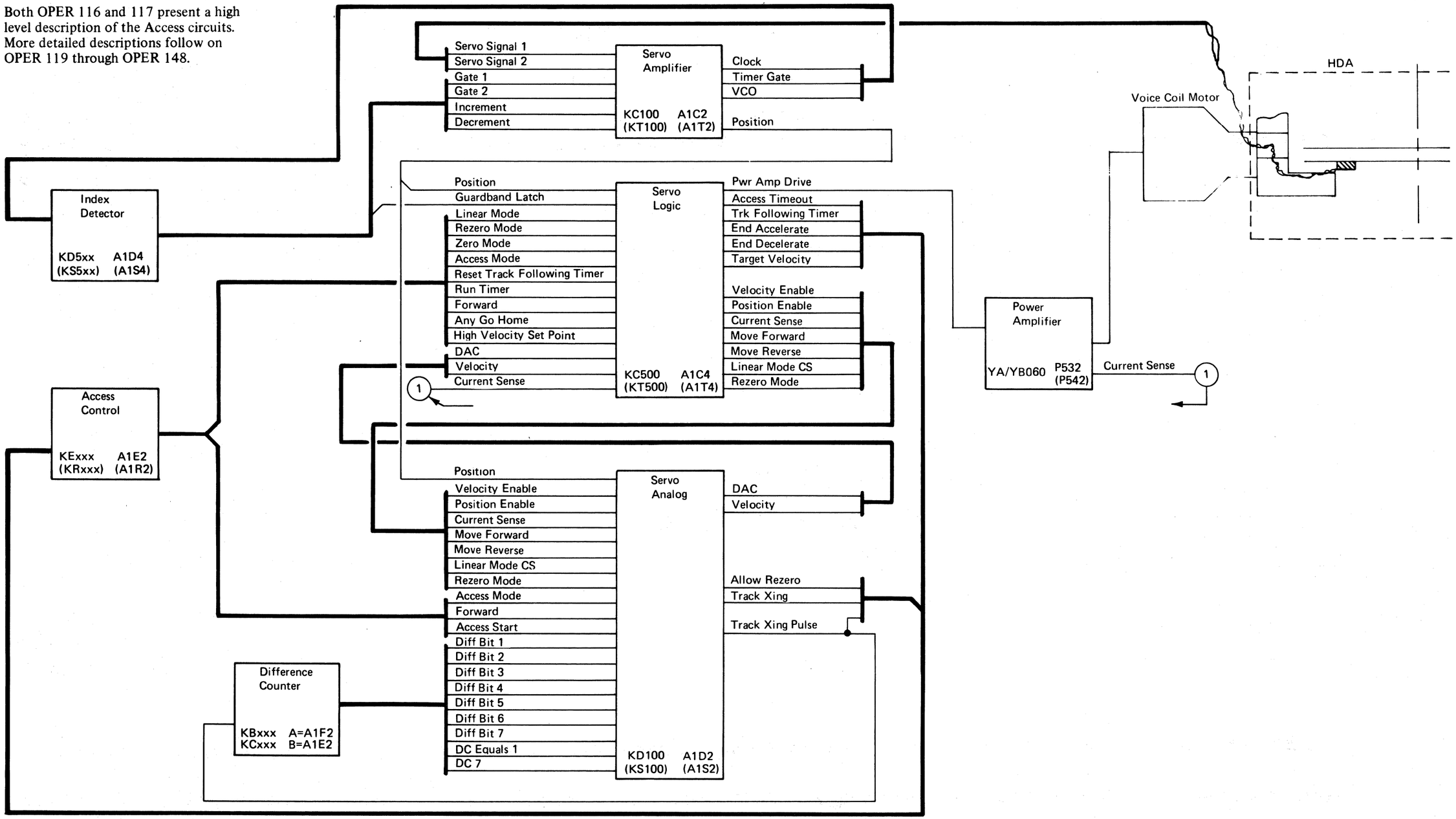
Both OPER 116 and 117 present a high level description of the Access circuits. More detailed descriptions follow on OPER 119 through OPER 148.



3350	BD0111 Seq. 2 of 2	2358048 Part No.	441300 31 Mar 76	441303 30 Jul 76			

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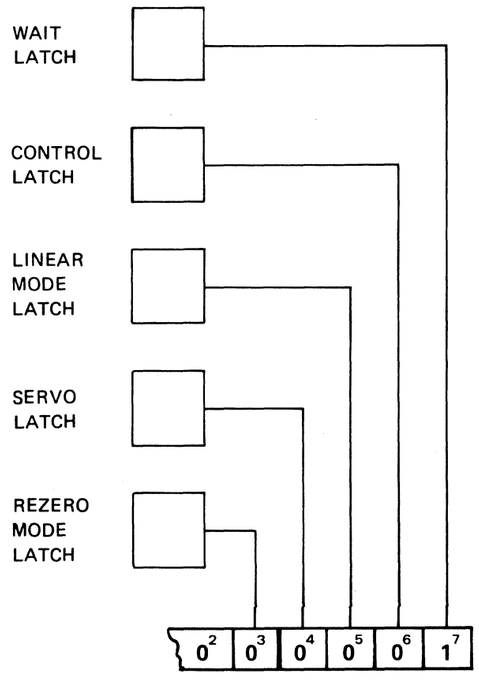
ACCESS OPERATION — BLOCK DIAGRAM DESCRIPTION

ACCESS CONTROL

Access control provides control signals for the servo logic to start operations and give direction and speed for access movement. Five latches monitor the correct state of the access operation.



0^2	0^3	0^4	0^5	0^6	1^7				
						=	State 01	Wait State	Reset
0	0	0	0	0		=	State 00	Start Rezero	Rezero Operation
1	0	0	0	0		=	State 10	Move Out	
1	0	0	1	0		=	State 12	Turnaround	
1	0	1	1	0		=	State 16	Move In	
0	0	1	1	0		=	State 06	Rezero Linear Mode	
0	1	1	1	0		=	State 0E	On Track	
0	1	0	1	0		=	State 0A	Accelerate	Seek Operation
0	1	0	0	0		=	State 08	Decelerate	
0	1	1	0	0		=	State 0C	Seek Linear Mode	
0	1	1	1	0		=	State 0E	On Track	

INDEX DETECTOR

The Index detector identifies Index patterns for Index sensing and identifies the sectors for Rotational Position Sensing (RPS).

DIFFERENCE COUNTER

During Seek operations, the difference counter counts track crossings as the heads move from the start track to the target track.

SERVO AMPLIFIER

The servo amplifier maintains an even signal from the servo head to develop the Position signal. It provides input and timing for the Voltage Controlled Oscillator (VCO), the sector counter, and the Index register.

SERVO LOGIC

The Servo Logic circuits drive the power amplifier, monitor access operations, and act as an interface between access control and servo analog.

SERVO ANALOG

The Servo Analog converts the Position signal, the difference counter, and the track crossing inputs into the Velocity output signal. Velocity represents the carriage speed.

POWER AMPLIFIER

The power amplifier amplifies forward-or reverse-drive current to move the voice coil.

VOICE COIL MOTOR

The voice coil motor is connected to the carriage within the head/disk assembly (HDA). When the voice coil motor moves, the carriage and the heads also move.

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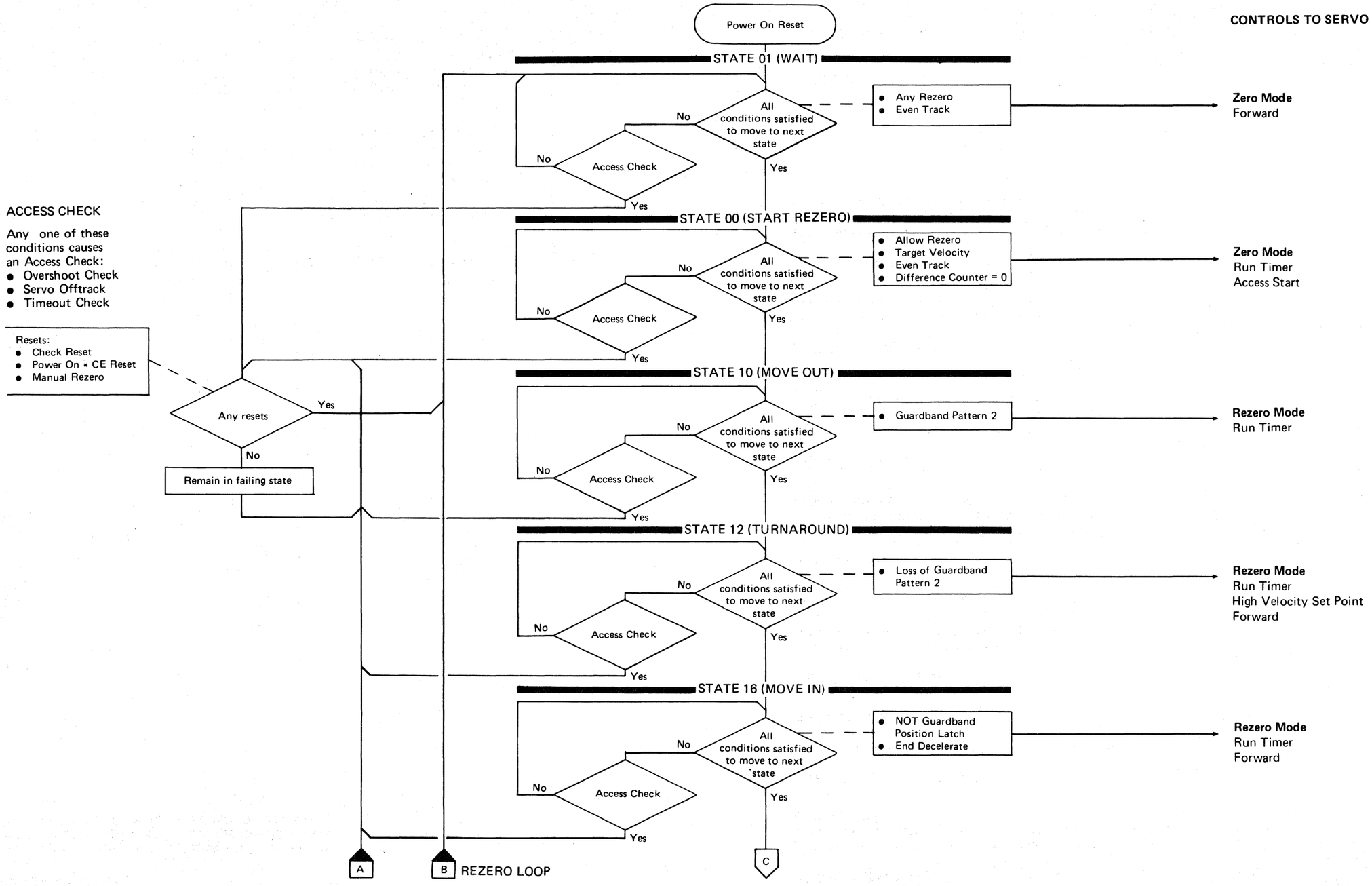

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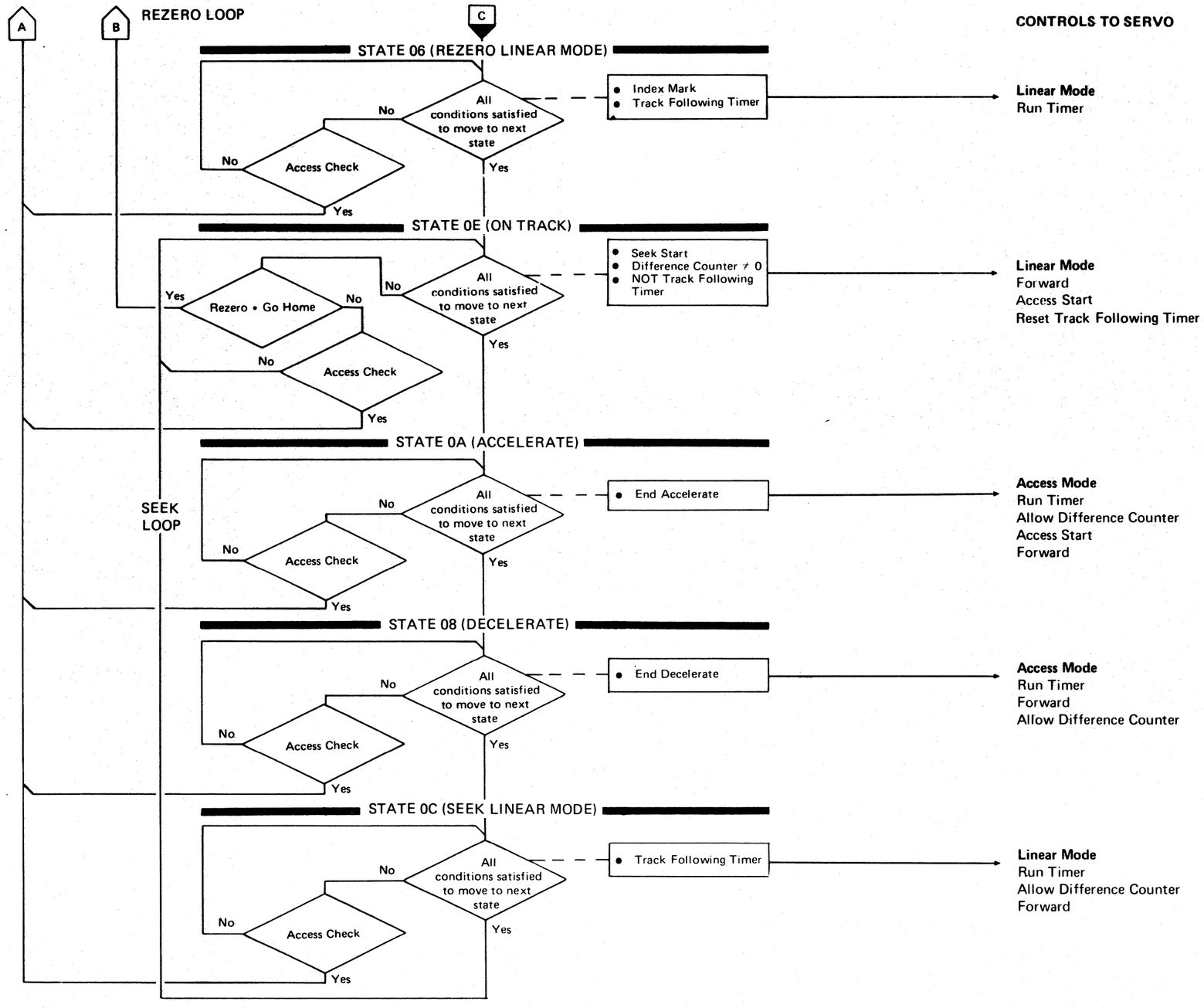

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TRACK FOLLOWING

All data heads in the Head/Disk Assembly (HDA) are tied **directly through the carriage to the servo head. When the servo head is on a particular track, every head is on the same track.**

At the completion of a Seek or Rezero operation, the servo head locks on the correct track and continues to follow that track until a new Seek or Rezero operation is initiated.

TRACK FOLLOWING LOOP

1. The servo head 1 reads the servo signal.
2. The servo amplifier 2 develops the composite servo signal.

   Steps 1 and 2 are described in more detail on OPER 124 and OPER 125.
3. The demodulator 3 produces a voltage level (Position signal) proportional to the servo head position over the center of the servo track.
4. The compensator 4 uses the Position signal to generate the Position Error signal. This error signal is proportional to the distance that the servo head is off the track center.
5. During track following time, access control provides Linear Mode, which gates Position Error through the select amplifier 5 to generate Power Amp Drive to the power amplifier.
6. The power amplifier 6 provides the current to the voice coil motor to move the servo head back on track.

ACCESS CHECK

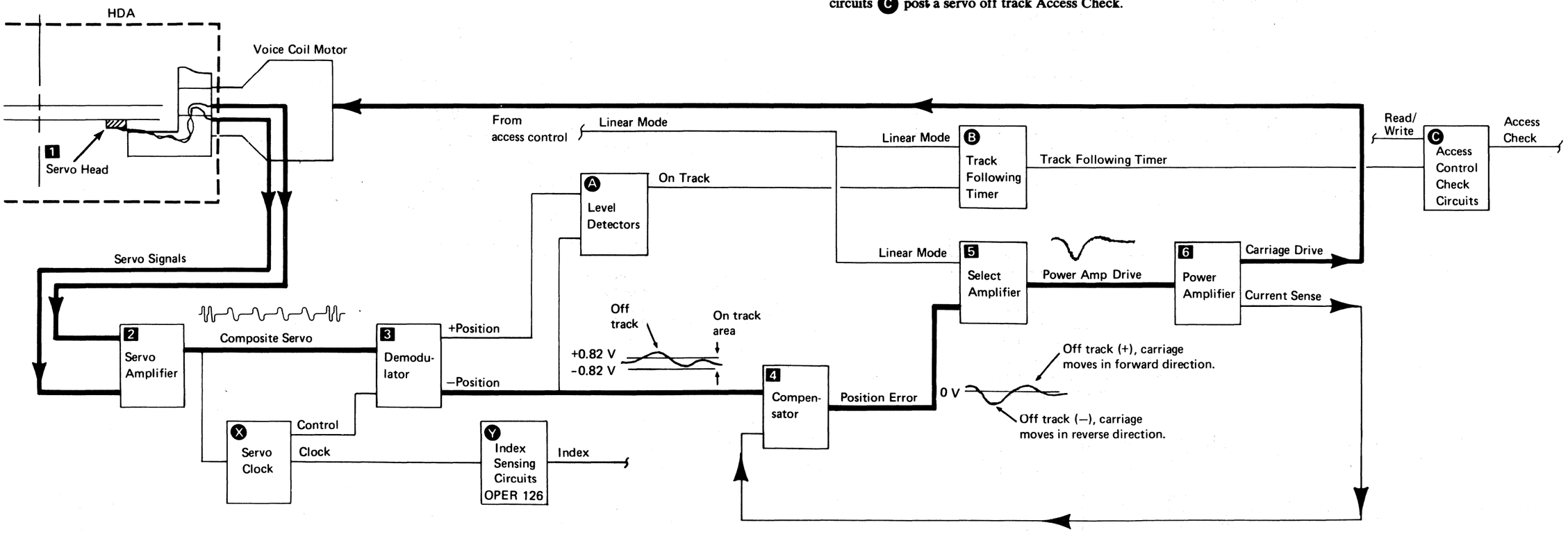
1. The Position signal is checked by voltage level detectors A to determine when the servo head is within the proper on track area.
2. During Linear Mode, the track following timer B sends a signal to access control if the heads remain on track.
3. If the Track Following Timer signal is lost during a Read or Write operation, the access control check circuits C post a servo off track Access Check.

SERVO CLOCK

The servo clock X develops clock pulses to synchronize Read/Write operations to the disk and access control lines.

INDEX SENSING

Using the clock bits from the servo clock, the Index Sensing circuitry Y determines when the servo head passes over an Index Mark. (See OPER 126 for a more detailed description of Index detection.)



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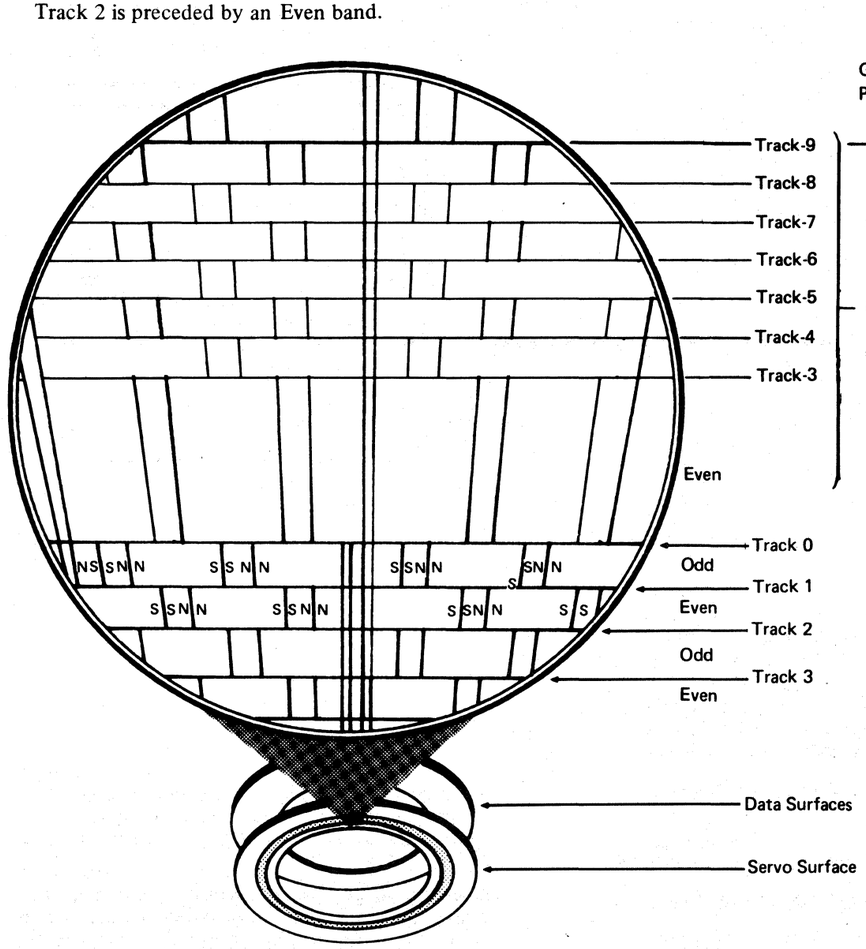
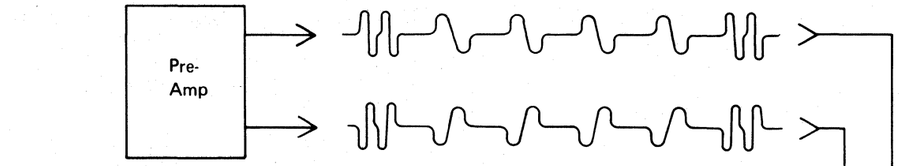
TRACK FOLLOWING

In order for the servo head to be able to track follow, the servo surface of the HDA has the following format:

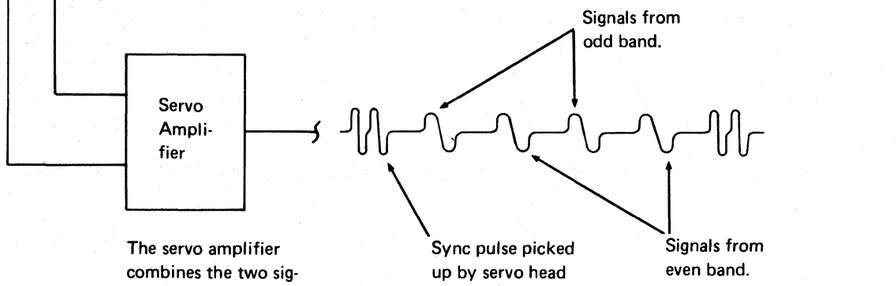
- 561 tracks between special prerecorded bands.
- Bands are either Odd or Even and arranged alternately; one even, one odd.
- Bands are recorded like bar magnets, end-to-end, with north and south poles.
- Odd-numbered tracks are preceded by odd bands; even-numbered tracks by even bands, so that:

  Track 1 is preceded by an Odd band.
  Track 2 is preceded by an Even band.





As the disk rotates, the servo head senses the magnetic changes. The resultant differential signal passes through the preamplifier in the HDA on the way to the servo amplifier.



The servo amplifier combines the two signals into a composite servo signal. This is the basic pattern used by the servo circuits for track following. (Continued on OPER 125.)

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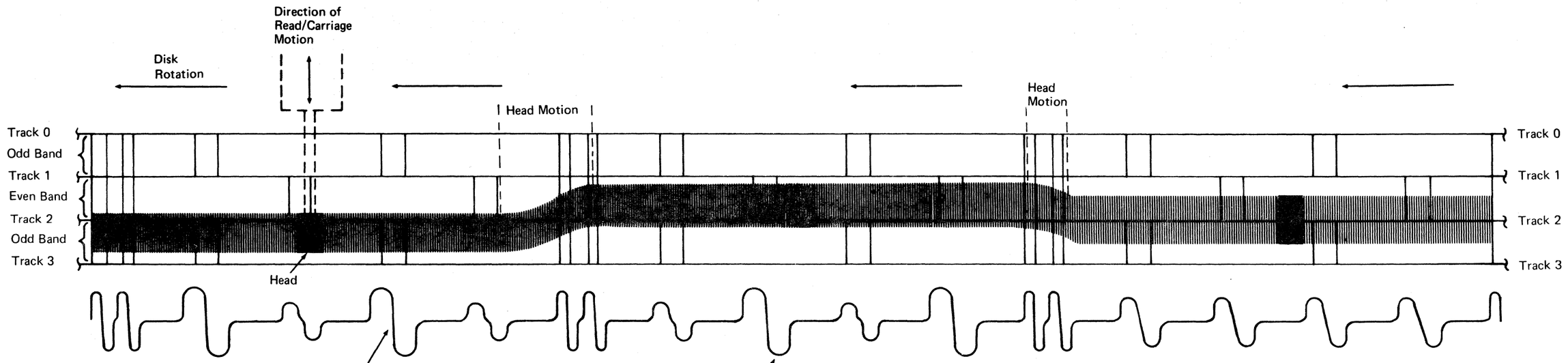
TRACK FOLLOWING

When the servo head is exactly between an "odd" and an "even" band, it is *On Track*. In this example, the head is attempting to follow track 2. As the disk rotates under the head, the carriage tries to keep the head on the track center.



If the servo head drifts off the track center toward the spindle (toward track 3), the composite servo signal becomes unbalanced.

The level of this part of the signal is higher because more current is induced from the odd servo band than from the even band.

If the head drifts off track in the other direction (toward the outer edge of the disk), the signal becomes unbalanced again,

and this part of the signal becomes higher than the other one.

When the servo system recognizes an off-track condition, it moves the carriage in the proper direction to balance the composite servo signal to keep the head on track.

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INDEX DETECTION

It is necessary for Read or Write operations to begin at the correct location on a track. A reference point is needed to indicate the start of the track. The reference point is Index.

The sync characters of the composite servo signal are used for encoding the Index. The method of encoding a single Index bit is to omit the first half of the sync character.

The Index detection circuits recogonize an Index bit by this absence of the first half of the sync character and decode it as a 1 bit.

Figure 1 shows a normal composite servo signal. Figure 2 shows a composite signal with Index coded sync characters.

An Index signal is finally indicated when the correct sequence of ones is decoded. The correct sequence for a valid Index is 1-1-0-1-0.

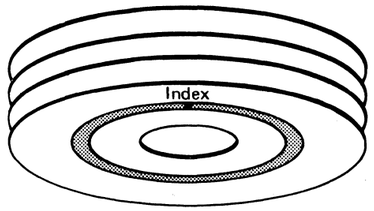

Figure 1. Normal Composite Servo Signal.

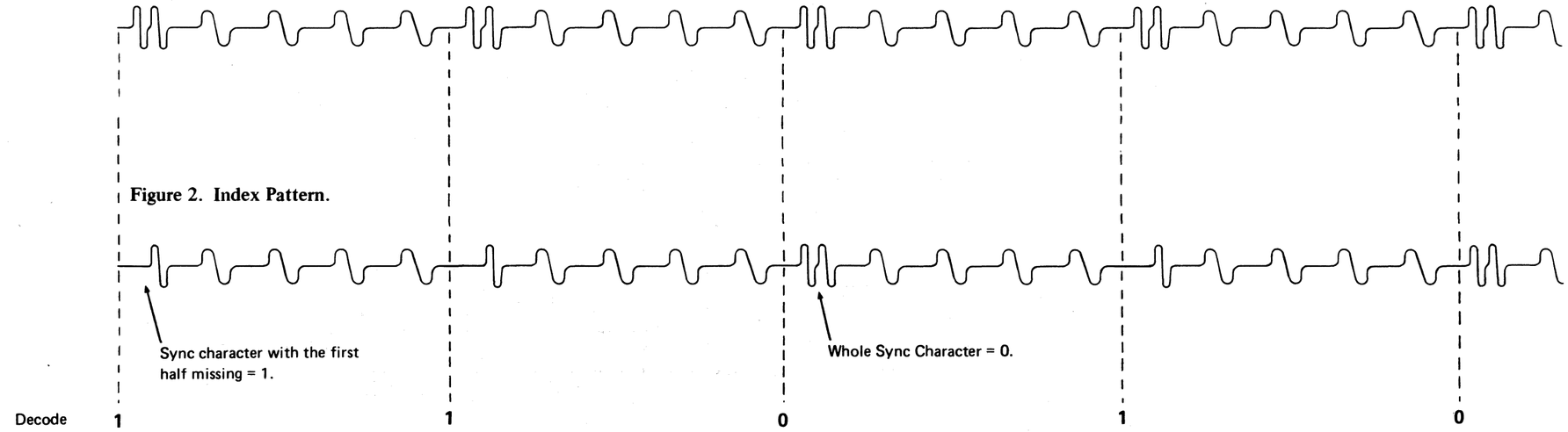

Figure 2. Index Pattern.

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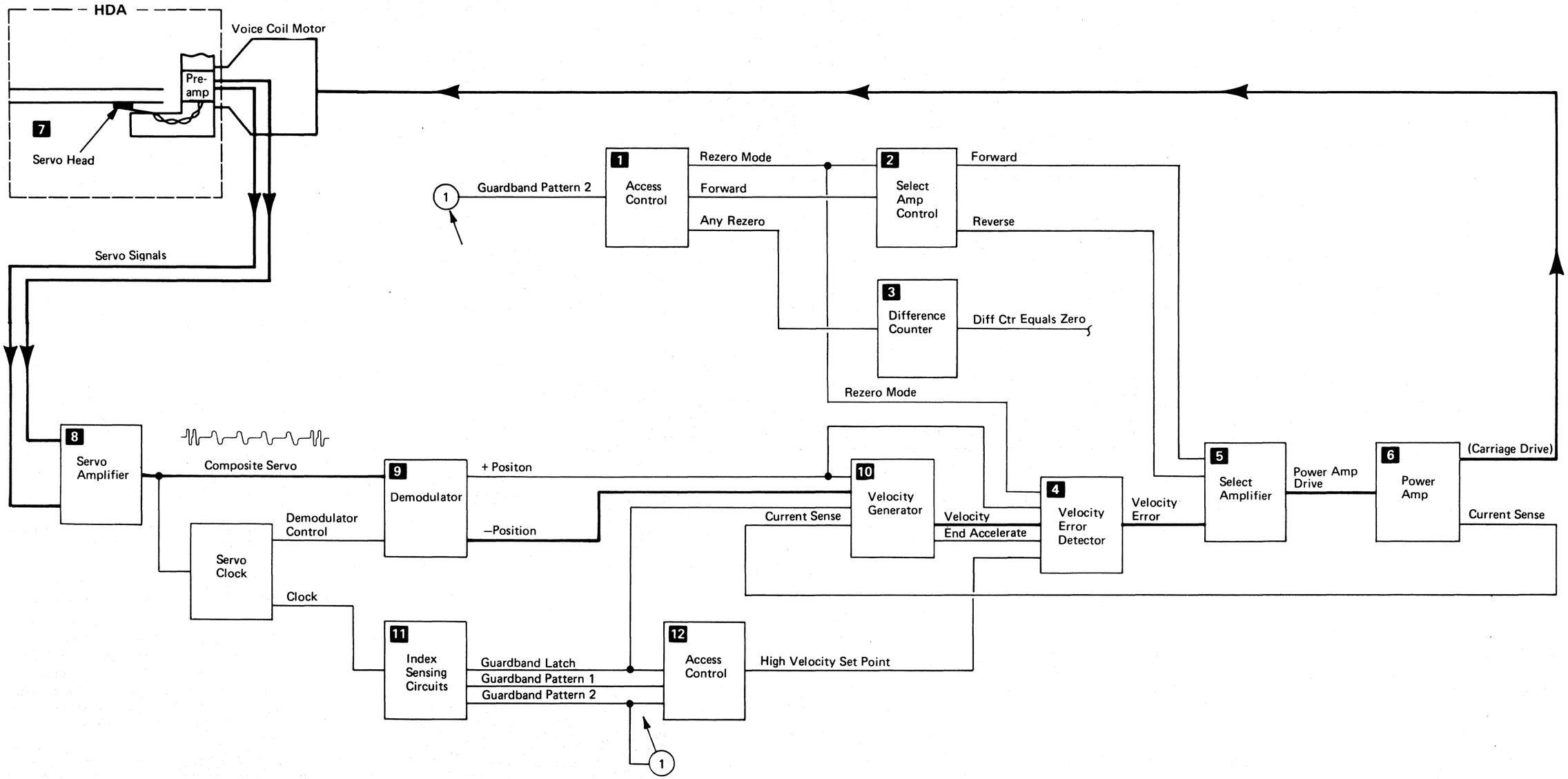
REZERO – FUNCTIONAL BLOCK DIAGRAM

See OPER 130 for a description of this diagram.



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REZERO — BLOCK DIAGRAM DESCRIPTION

The Rezero operation is neccessary to establish (or re-establish) a reference point for access control. Rezero causes the carriage to:

1. Move out from the center of the disk, past track 0.
2. Turn around.
3. Move slowly in the direction of the spindle.
4. Stop and track follow on track 0.

Use the timing diagram on this page with the block diagram on OPER 129.

A Rezero operation begins as a result of one of the following conditions: an HDA Rezero during HDA sequencing, a Recalibrate command under program control, or by a manual Rezero (pushing the Rezero pushbutton on the Operator Panel). For any of these conditions, access control **1** sends Rezero Mode to the select amp control **2** and Any Rezero to the Difference counter **3**.

The Forward signal from access control to the select amp control **2** indicates the direction the carriage moves at the start of the operation:

- Forward = toward the spindle.
- Reverse = toward the outside edge of the disk.

With Rezero Mode and not Forward as input signals, the select amp control sends Reverse to the select amplifier **5**.

Any Rezero from access control resets the Difference counter **3**. Because the Difference counter is reset and Rezero Mode is active to the velocity error detector **4**, the maximum velocity of a Rezero operation is 15 inches per second.

With the Velocity Error and Reverse as input signals, the select amplifier **5** provides Power Amp Drive for the power amplifier **6** to start the carriage moving outward from the center of the disk toward track 0.

The servo head **7** reads the servo signal and sends it through the pre-amp and servo amplifier **8** to the demodulator **9**.

The output of the demodulator (the Position signal) reflects track crossings used by the velocity generator **10** to calculate the velocity of carriage movement.

When the servo head is in the guardband pattern area, the Index sensing circuits **11** decode Guardband Pattern 1 and send the Guardband Latch signal to the velocity generator **10**. (See OPER 131 for a detailed description of guardband pattern detection.)

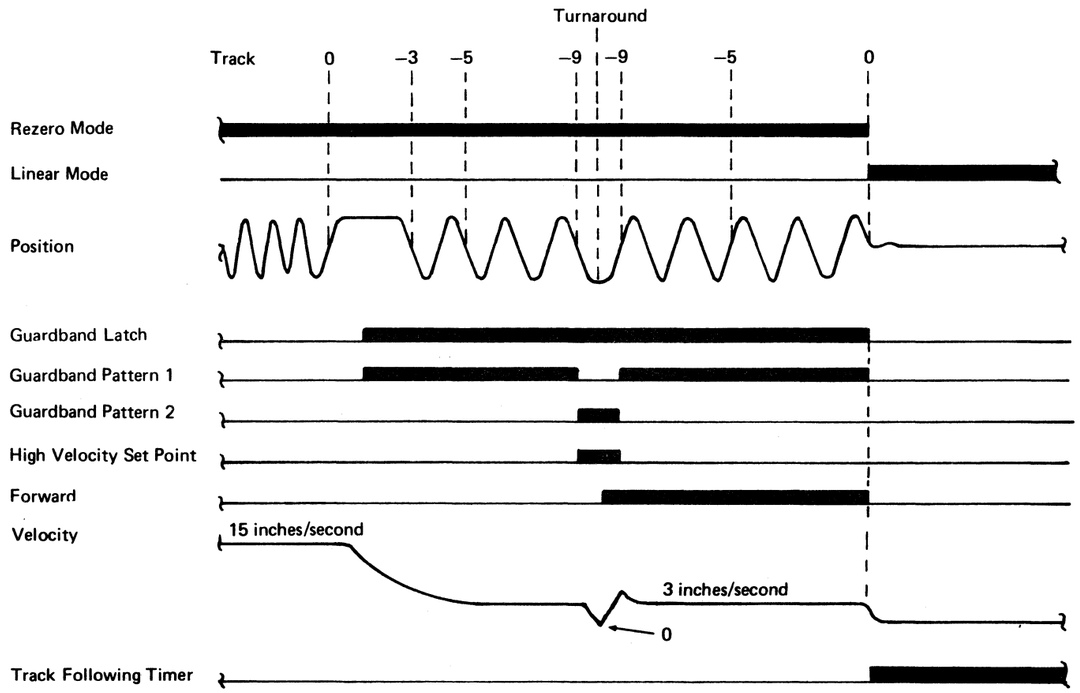
When the velocity generator receives the Guardband Latch signal, it sends End Accelerate to the velocity error detector **4**.

End Accelerate controls the carriage speed by gating + Position to the velocity error detector. Carriage velocity decreases to 3 inches per second because of the decrease in voltage (from Position) into the velocity error detector.

The carriage continues at 3 inches per second until it reaches Guardband Pattern 2 near track −9. At Guardband Pattern 2 time, access control **12** sends High Velocity Set Point to the velocity error detector to stop the carriage.

Guardband Pattern 2 also feeds access control **1** and activates the Forward signal for Turn around.

The carriage moves forward toward track 0 at 3 inches per second. When the carriage nears track 0, the Guardband Latch becomes inactive. Rezero Mode and Forward becomes inactive at access control **1**, and the carriage slows down to a stop and begins track following on track 0 in Linear Mode.



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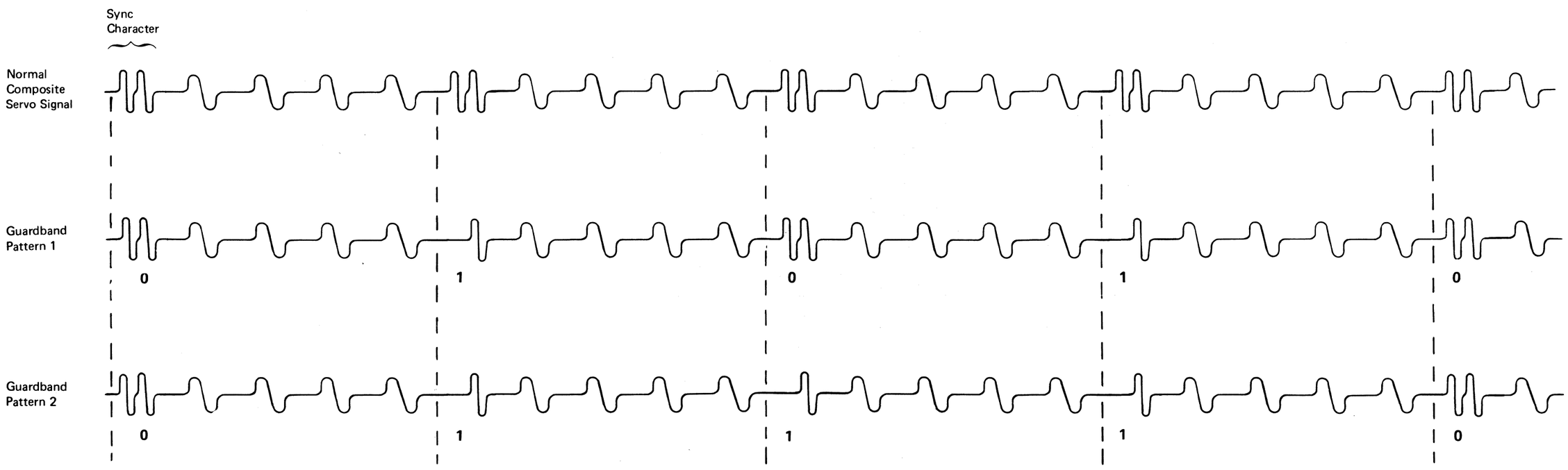
GUARDBAND PATTERN DETECTION

The Guardband pattern is detected by the Index detection circuits in the same way that Index is detected. The Index detection circuits look at each sync character of the composite servo signal for Index bits. As mentioned on OPER 126, the Index detection circuits recognize an Index bit by the absence of the first half of a sync character. This absence is decoded as a 1 bit. The correct sequence of 1 and 0 bits is decoded as follows:

For Guardband Pattern 1 — 0-1-0-1-0

For Guardband Pattern 2 — 0-1-1-1-0

The Index detection circuit decoders are shown on ALD page KR030.



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SEEK OPERATION DESCRIPTION

The three most important steps of a Seek operation (OPER 108) are Select (Tag '83'), Set HAR (Tag '8B'), and Set Difference (Tag '8C').

SELECT

The controller and the drive must both be selected (Tag '83').

A 6-byte Seek address must be transferred from the channel to the storage control.

Tag Gate and Tag Bus must be latched to the drive.

SET HAR

Ctl Tag '8B' sets the Head Address Register (HAR). Tag bits 6 and 7 are routed through the controller to the device and shifted to Dev Tag Bus bits 1 and 2 (OPER 140 **1**).

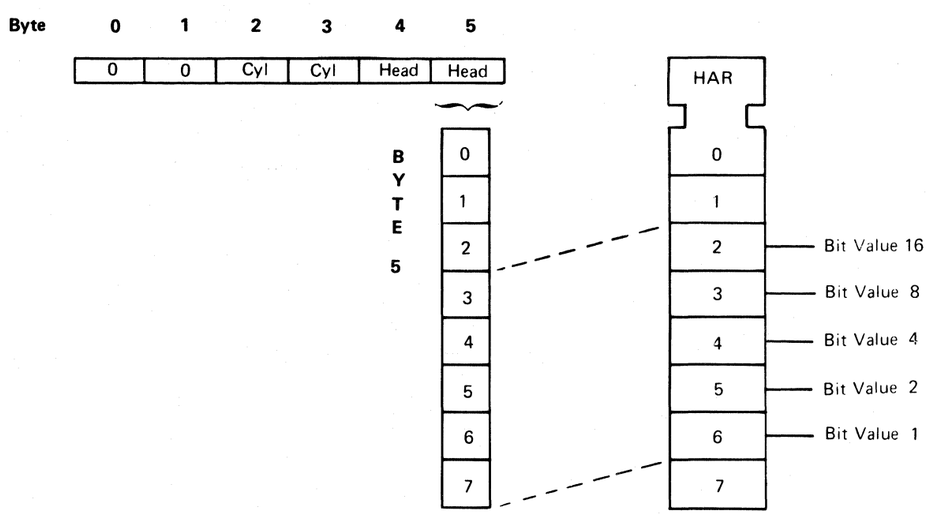
Bytes 2 and 3 of the Seek address specify the logical cylinder address and bits 3 through 7 of Byte 5 specify the logical head address. (See Figure 1.) The head address is placed on Bus Out and is routed through the controller and shifted to Dev Bus Out to set the Head Address Register (OPER 140 **3**).

SET DIFFERENCE

Ctl Tag '8C' sets the Difference Counter (OPER 140 **2**). The Difference Counter is loaded with the difference between the current cylinder address and the desired cylinder address as calculated by the storage control.

The storage control sends a Seek Start (OPER 140 **4**) to the drive access control to start carriage movement (see OPER 141 and 142 for Access operation during the Seek).

Figure 1. Seek Address



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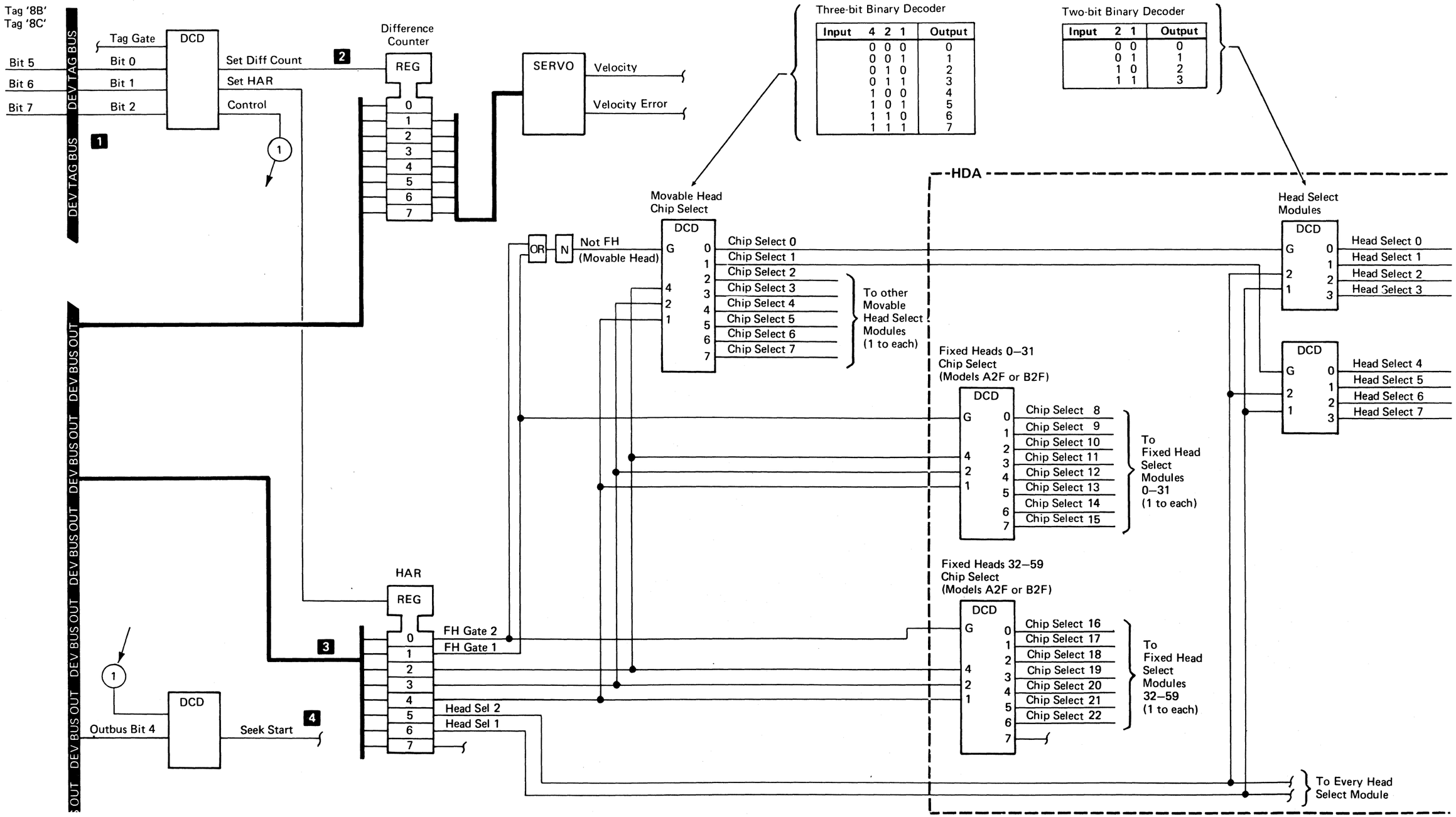
SEEK OPERATION



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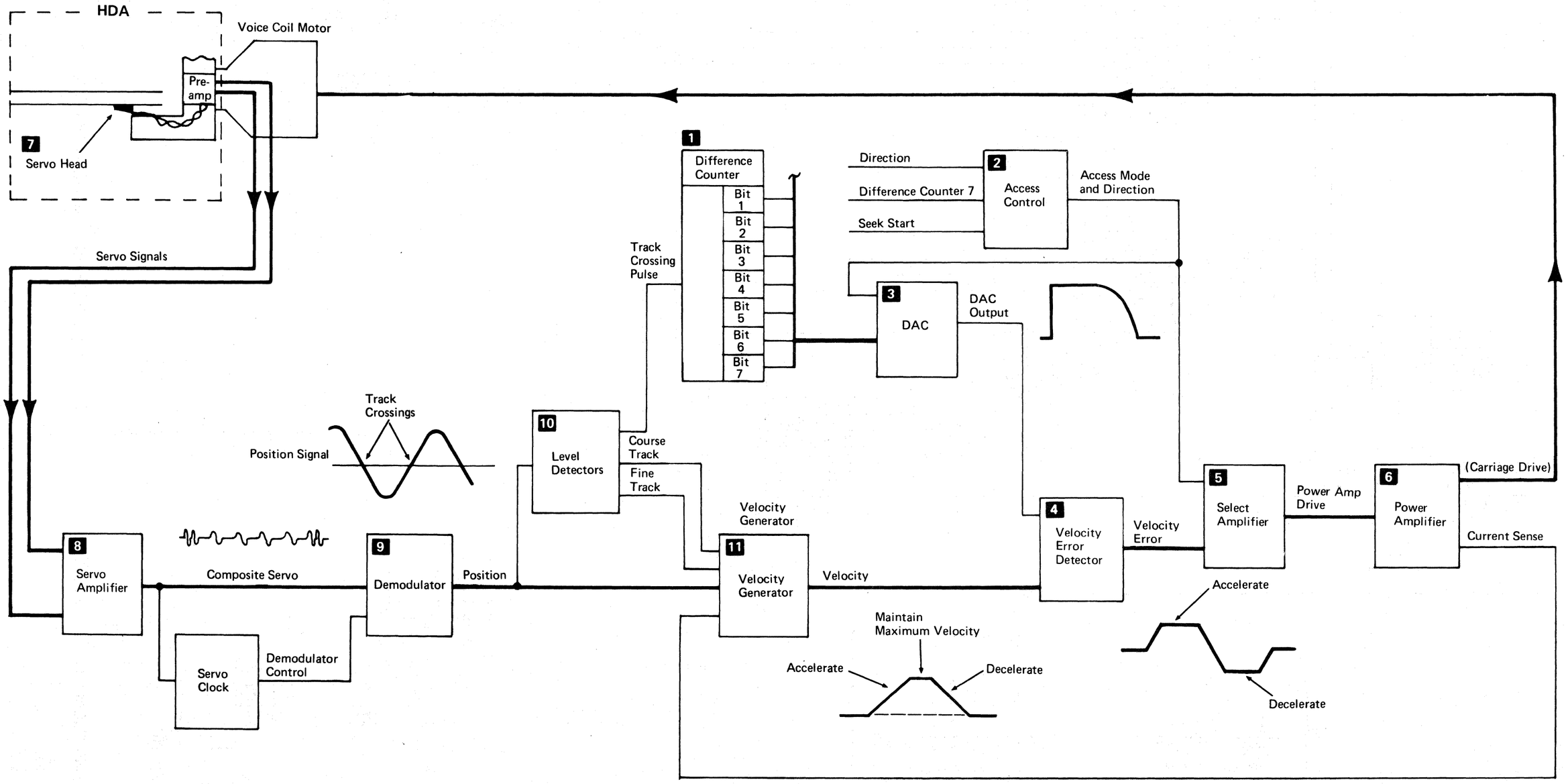
See OPER 142 for a description of this diagram.



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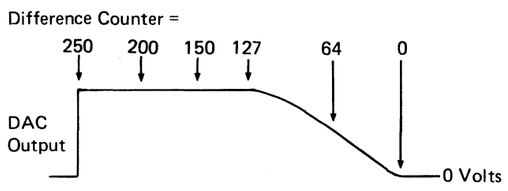
SEEK – DESCRIPTION OF BLOCK DIAGRAM

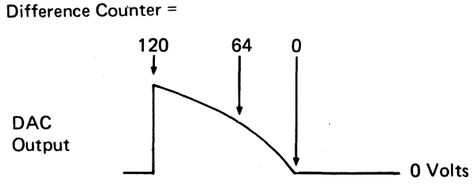
A Seek command causes the carriage to move from one physical track to another by first loading the difference between the current carriage address and the new carriage address into the difference counter. It then places the new head address and direction of the Seek (forward or reverse) in the Head Address Register (HAR). The carriage is moved the correct number of tracks to the new location and track follows on the new track.

The operation begins after the difference counter **1** is loaded and access control **2** sends Access Mode and the direction of the Seek to the servo circuits. This allows the Digital-to-Analog Converter (DAC) **3** to set the speed of the carriage.

If the difference counter has a value of 127 or above, the DAC output voltage is at its maximum point. During the Seek, as the difference counter decreases, the DAC output remains at maximum until the count reaches 127. At that time, the DAC output voltage begins to decrease proportionately to the value in the difference counter. As a result, if the difference counter is 250 at the start of a Seek, the DAC Output signal curve is as shown below:



If the Seek starts with a difference count of less than 127 (for example, 120), the curve is more like the following:



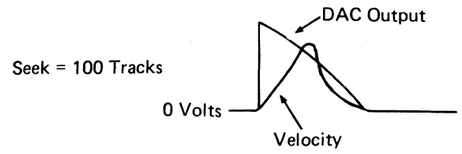
The output of the velocity error detector **4**, Velocity Error, is the sum of DAC Output and Velocity. Velocity Error feeds the select amplifier **5**, which feeds a voltage signal to the power amplifier **6** to drive the carriage toward the target track.

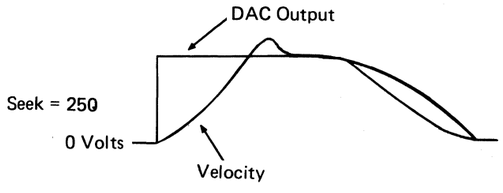
As the servo head **7** moves across the tracks, the servo signal is fed through the servo amplifier **8** to the demodulator **9** where the resulting output Position signal reflects the frequency of the track crossings.

The level detectors **10** use the Position signal to develop the Coarse Track and Fine Track signals, and from them, the Track Crossing Pulse. (See Figure 1 for the relationship of these signals to each other.)

The velocity generator **11** also uses the Position signal to determine the speed of the carriage and sends the Velocity signal to the velocity error detector.

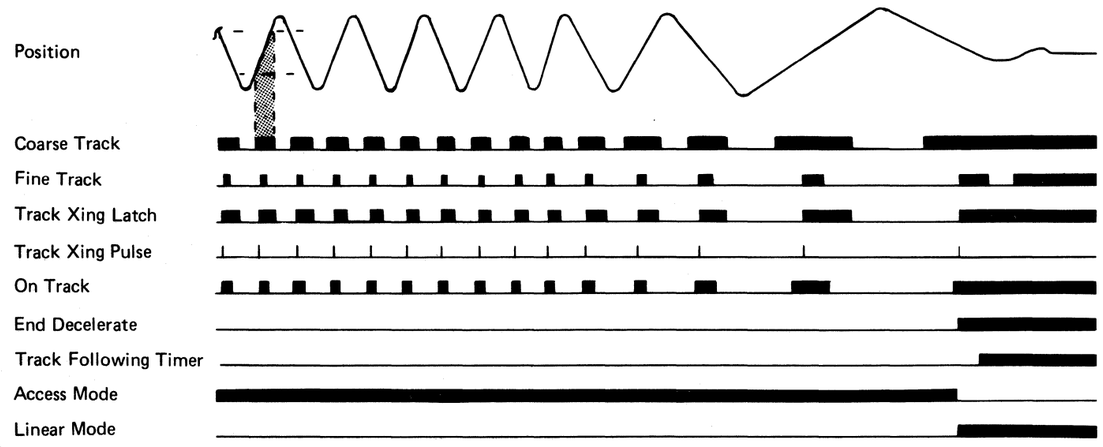
The velocity error detector takes DAC output and the Velocity signal, adds them algebraically, and produces Velocity Error. DAC output represents an ideal carriage velocity; Velocity is the actual velocity of the carriage. The figures below show the Velocity signal superimposed on the DAC output signal to show their relationship for two seeks of different length.





When the Velocity signal becomes greater than the DAC output, reverse current is applied to the Voice Coil Motor (VCM) to slow down the carriage. As the difference counter decreases, the carriage continues to slow down until the target track is reached. At that point, the carriage stops, access control goes to Linear Mode, and the servo system begins track following on the new track.

Figure 1.



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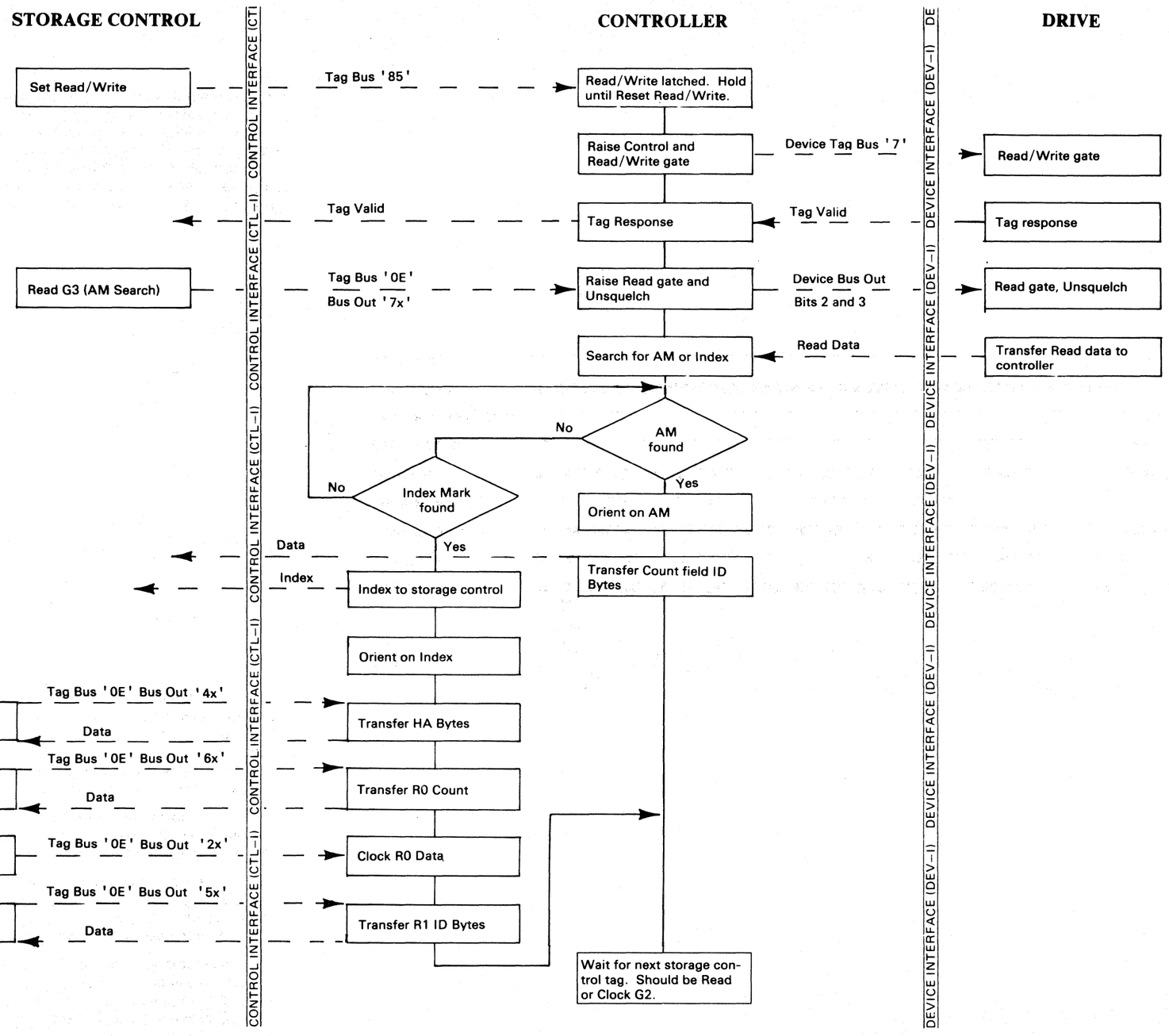
SEARCH ID EQUAL

Storage control compares data from the system with data read from the HDA (the ID bytes for Search HA or Search ID; Key field bytes for Search Key).

Only one record is operated on for each Search command.

When the search is unsuccessful, the channel must reissue the Channel Command Word (CCW). This is done by the use of a Transfer In Channel (TIC) back to the Search command.

When the search is successful, the Status Modifier bit in the Channel Status Word (CSW) is set on. This causes the channel to skip the next CCW (TIC) in the chain.



When Index is sensed during an AM search, this sequence of operations is performed to maintain orientation and read the R1 Count field. If the second active Index is sensed before the search is successful, No Record Found is set.
(See OPER 208.)

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ROTATIONAL POSITION SENSING

Rotational Position Sensing (RPS) reduces the channel time consumed by disk rotation during Search operations. The channel time consumed is reduced by the drive releasing the channel to perform other operations until just before the record is reached. The drive reconnects to the channel when the Target Register and the Sector Counter are equal (compare equal).

The Sector Counter counts from 0 (at Index) to 127. The Sector Counter runs continuously while the drive is track following. Sector Count pulses are derived from the servo clock. The Sector Clock Counter (see OPER 204) accepts 39 sector count pulses before advancing the Sector Counter one count. After the Sector Counter reaches 127, the Valid Index 1 pulse resets the Sector Counter for the next revolution.

The Target Register performs two functions:

1. It is loaded at the beginning of all Read, Write, and Search CCWs by a Set Sector command. The sector number is fetched from main storage.
2. It holds the starting sector location of the record to be read or written. It temporarily stores the beginning sector count transferred from the Sector Counter.

After the Target Register is loaded during a Search operation, its value can be moved over the channel to main storage by a Read Sector command. The storage location of the sector number is determined by the individual customer program.

An example of an RPS application (Figure 1), is Read Verification (read-back check). The sequence of channel commands or functions is:

1. Seek
2. Search ID
3. TIC*-8
4. Write Data
5. Read Sector
6. Set Sector
7. Disconnect (Function)
8. Search ID
9. TIC*-8
10. Read Data

Seek

Moves the carriage to the desired track and selects the head.

Search ID

Finds the record to be written and transfers the sector number from the Sector Counter to the Target Register at **2** .

TIC*-8

Loops until the desired ID is located.

Write Data

Transfers data from main storage to the disk record at **3** .

Read Sector

Moves the sector number from the Target Register at **4** to main storage.

Set Sector

- Moves the sector number from main storage to the Target Register at **5** . The Target Register has the correct sector number but comparison is required three sectors earlier to ensure channel reconnection.
- The number three is subtracted from the sector number in the storage control before it is loaded into the Target Register.

Disconnect

The Disconnect function releases the channel at **6** to perform other operations.

Search ID

Search ID is a short search from **1** to **2** in which the time demand on the channel was reduced.

TIC*-8

Loops until ID is located.

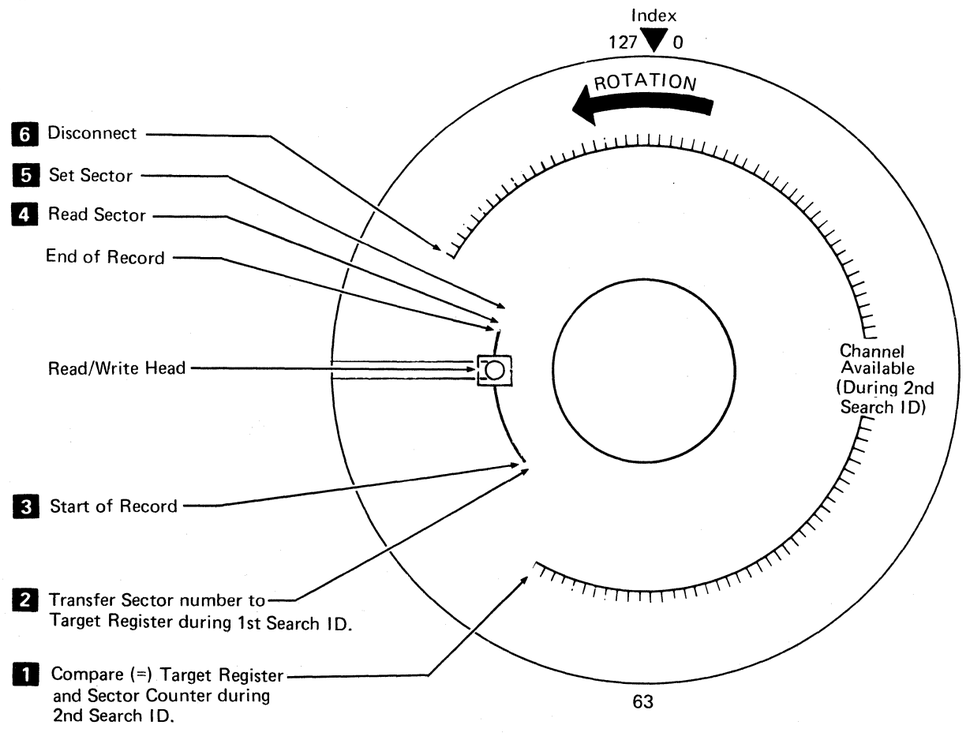
Read Data

The data written earlier at **3** is now read into main storage for comparison with the original data.

If all records were of fixed length, the sector number could be calculated for each record to be written. With RPS, the search before writing could release the channel and reconnect when the Target Register and Sector Counter are compared.

OPER 204 and 205 contain more details on Rotational Position Sensing.

Figure 1. Read Verification with RPS



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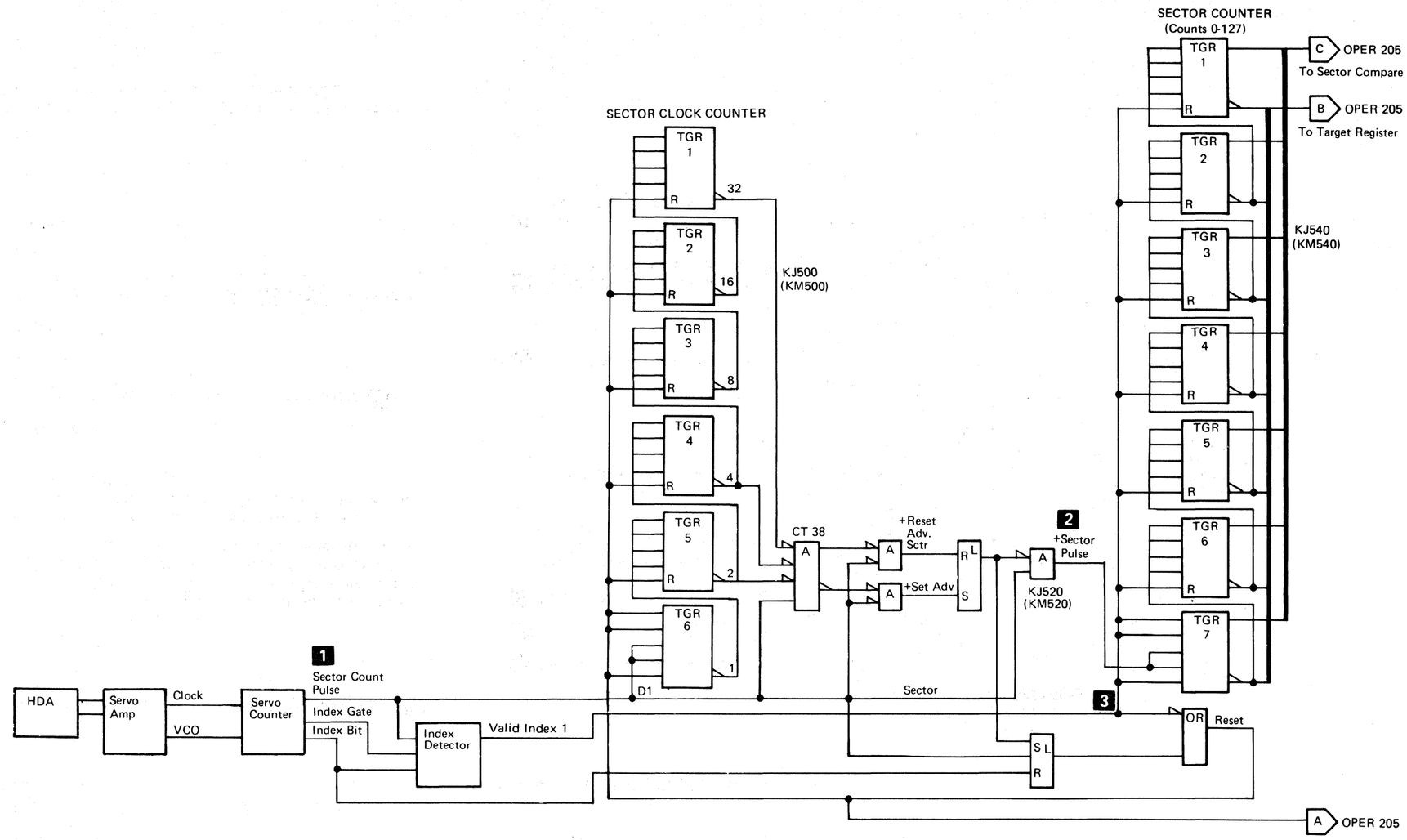
RPS – SEARCH SECTOR OPERATION

Functional characteristics of the Search Sector operation are:

- One sector count pulse for each servo byte **1** .
- 4992 sector count pulses for a full track.
- 128 sectors for each track (0 to 127).
- 39 sector count pulses for each sector (38 clock counter pulses plus next sector count pulse) **2** .
- Sector duration is 124 to 136 microseconds.
- Sector Counter resets at Valid Index 1 while the drive is track following **3** .

OPERATION

- The value in the Target Register is set with a Set Target Command which also starts a Search Sector Operation (OPER 205 **5** and **8**).
- When the sector count is equal to the value in the Target Register, a Sector Compare occurs for 124 to 136 microseconds. Attention is also active for that sector time.
- A Sector Compare occurs each revolution until Attention is reset (OPER 205 **9**).
- Device Bus In bit 7 is active during the Search Sector operation.
- Device Bus In bit 6 (Busy) is active during the Search Sector operation except during the sector in which the compare is equal (OPER 205 **7**).
- Sector Compare check occurs if a Sector Compare does not take place in two revolutions. Drive Check is set (OPER 205 **6** and **10**).
- The controller issues Transfer Sector Count to the drive before all G1 and G3 Read and Write tags at count 67 time and on Search commands when an Address Mark is found.
- A Sense Target command then sends the value of the sector count to Device Bus In (OPER 205 **4**).



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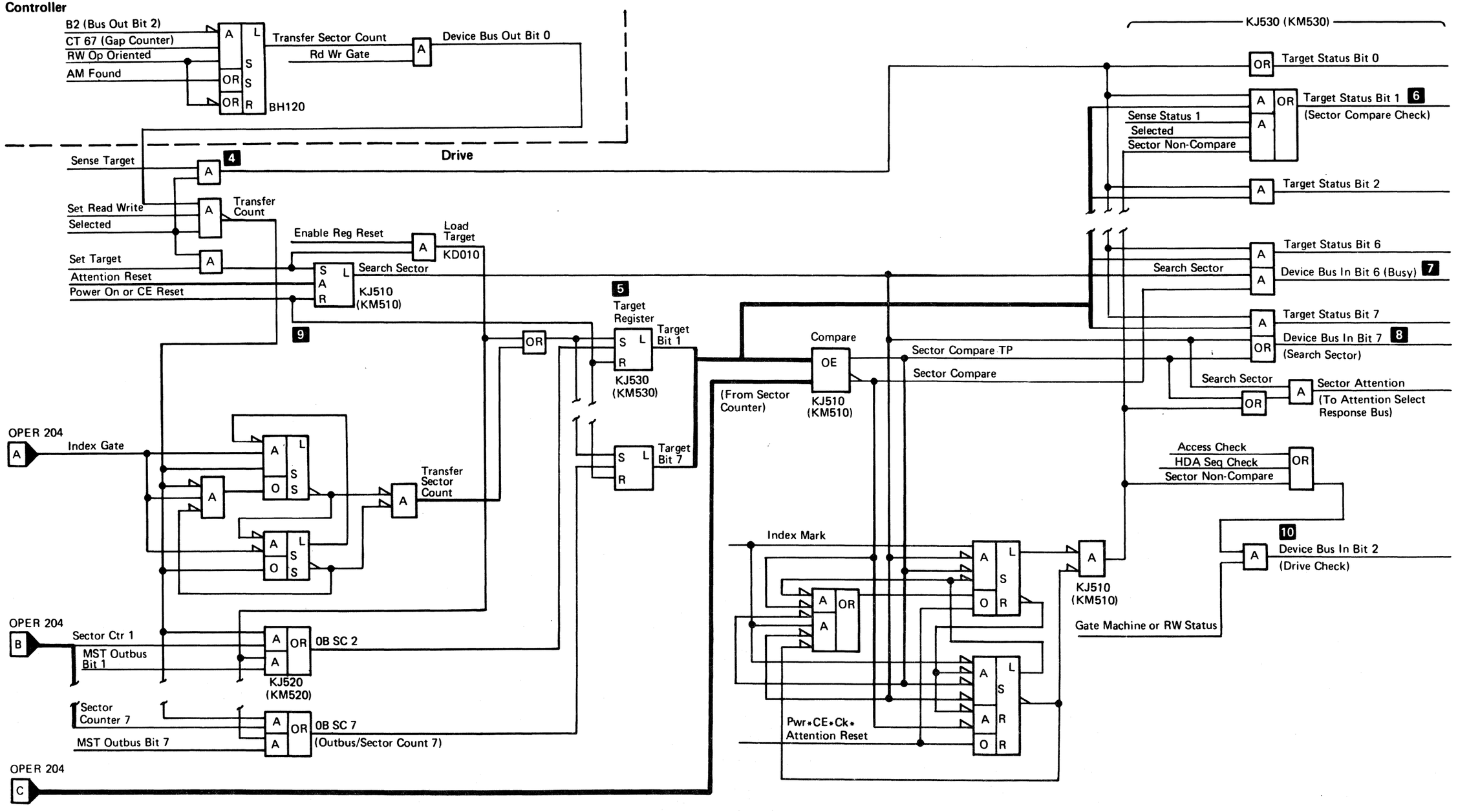
RPS – SEARCH SECTOR OPERATION



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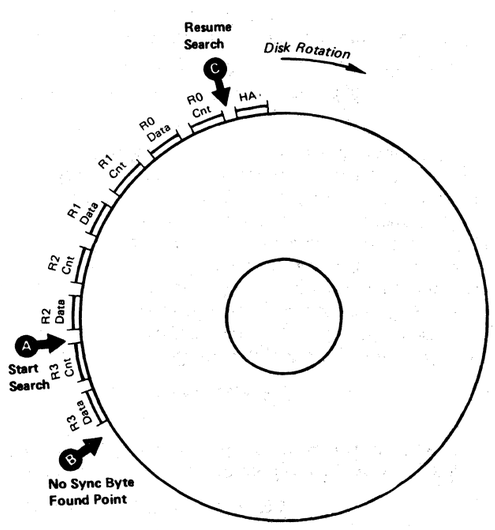
NO RECORD FOUND

A No Record Found condition exists when Index has been passed twice in the same non-multitrack search and TIC loop. When the No Record Found condition is detected, the storage control posts a unit check with No Record Found indicated in Sense Byte 1 bit 4.

To illustrate the No Record Found operation, assume the track is formatted as shown below and the following command chain has been issued:

Seek
Search ID Equal Record 5
TIC-8 (Transfer In Channel To The Previous CCW)
Read Count, Key, Data

When a non-multitrack search and TIC are successive commands in a command chain, the loop continues until either the search is successful or until Index has been passed twice.



If the Search is started at (A), the operation becomes oriented on the Address Mark in the gap prior to the record 3 Count area. The record 3 Count area (record 3) is read and compared against the search argument (record 5) and a non-compare results. The TIC-8 causes the Search command to be reissued.

There are no fields after record 3; therefore, no sync byte is found at (B). Because no sync byte is found, the storage control suspends the search at (B) until Index is encountered.

After Index is passed, the storage control reads and clocks the Home Address area and saves certain information. This operation is transparent to the command chain.

The Search command, which was suspended at (B), is resumed at (C) beginning with Record 0 Count area. As before, a non-compare results and a TIC-8 occurs.

The Search command is reissued for record 1, record 2, and record 3 with non-compare results. Then, the Search command is issued for the last time. As before, the search is suspended at (B), because no sync byte is found.

When the Index is encountered again, the storage control signals a unit check, which breaks the command chain to terminate the operation.

Sense information is formatted with Byte 1 bit 4 set to 1 to indicate No Record Found.

The Index counter is reset whenever a Read Data, Read Home Address, or any Write Sense or Control command is issued subsequent to a successful search. This allows each separate search loop to search past Index twice before posting No Record Found.

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This page describes the diagram on OPER 211.

SET READ/WRITE – Tag '85'

Set Read/Write – Tag '85' is an extended operation. (See OPER 95 for an explanation of an extended operation.) Tag '85' conditions the controller and the drive for data transfer operations (Read or Write operations) in the following way. Set Read/Write:

- Sets the Read/Write latch 1
- Activates G2 (gate 2) on the Device Tag Reg 2 causing tag bits 0, 1, and 2 to be sent to the device (drive).
- Activates Device Tag Gate 3 .
- Activates Rd/Wr Gate 4 which activates G2 (gate 2) of the Bus Out Selector 6 . This deconditions the normal bus out bits (from storage control) and allows the Device Bus Out to carry read/write control information to the drive (from controller hardware). Bus Out bits 5, 6, and 7 are held active by the Rd Wrt Gate. The other Bus Out bits are manipulated by controller hardware 5 to control the data transfer. The device checks the condition of Bus Out ('07') after the Set Read/Write Op is issued, prior to the data transfer.
- Places the device in Control mode 7 .
- Activates Set Rd*Wr 8 in the device. This is a result of Control mode and Bus Out bits 5, 6, and 7 being active. The Set Rd*Wr line:
  1. Blocks normal device Bus Out Parity Error detection.
  2. Gates machine read/write status to Device Bus In 9 . (See OPER 100 for Device Bus In under Tag '85'.)
  3. Activates Set Rd*Wr Safe if no R/W Check conditions exist 10 .
  4. Provides a path for the Read/Write control lines to the Read Detector card of the selected drive 12 and 13 .
  5. Causes a Read/Write head to be selected in accordance with the value in HAR 15 . (HAR was set during the Seek, Tag '8B', that preceded this tag. See OPER 139 and 140.)
  6. Allows monitoring the Read/Write control lines for proper sequence 11 .
  7. Establishes a data path between the controller and the selected drive 14 .
- Enables the following functions of the data transfer control hardware 5 :
  1. Index processing.
  2. Gap counter control.
  3. Function Pulse generation.
  4. Synchronization of VFO with the controller and Servo pulses on the servo track of the HDA.
  5. Orientation (must be established between microprogram and disk rotational position for most operations).
- Signals the microprogram (with Normal End) that the controller and the device are conditioned to receive a data transfer tag. A data transfer tag is either '0E' for a Read operation or '0F' for a Write operation.

RESET READ/WRITE – Tag '05'

Reset Read/Write – Tag '05' is an immediate operation (see OPER 95 for an explanation of an immediate operation). Tag '05' resets the controller and device hardware that was set by Tag '85' after Read or Write Tags (Tags '0E' and '0F') have been completed.

To have a complete data transfer operation, the sequence of tags should be:

1. Set Read/Write – Tag '85'
2. Data Transfer
   Tag '0E' for Read
   Tag '0F' for Write
3. Reset Read/Write – Tag '05'

Reset Read/Write – Tag '05':

- Resets the Read/Write Latch 1 .
- Deactivates Device Tag Gate 3 , which removes the device from control mode, disabling the device Read/Write hardware.
- Restores data transfer control hardware functions 5 to non-data transfer condition:
  1. Allows bit ring 0 time pulse to reset the gap counter and control the function pulse.
  2. Disables Index processing.
  3. Disables VFO synchronization.
  4. Disables Orientation.
- Returns control of Device Bus Out to the storage control 6 .
- Resets conditions set up during a Read (Tag '0E') or Write (Tag '0F') operation.
- Signals the microprogram with Normal End.

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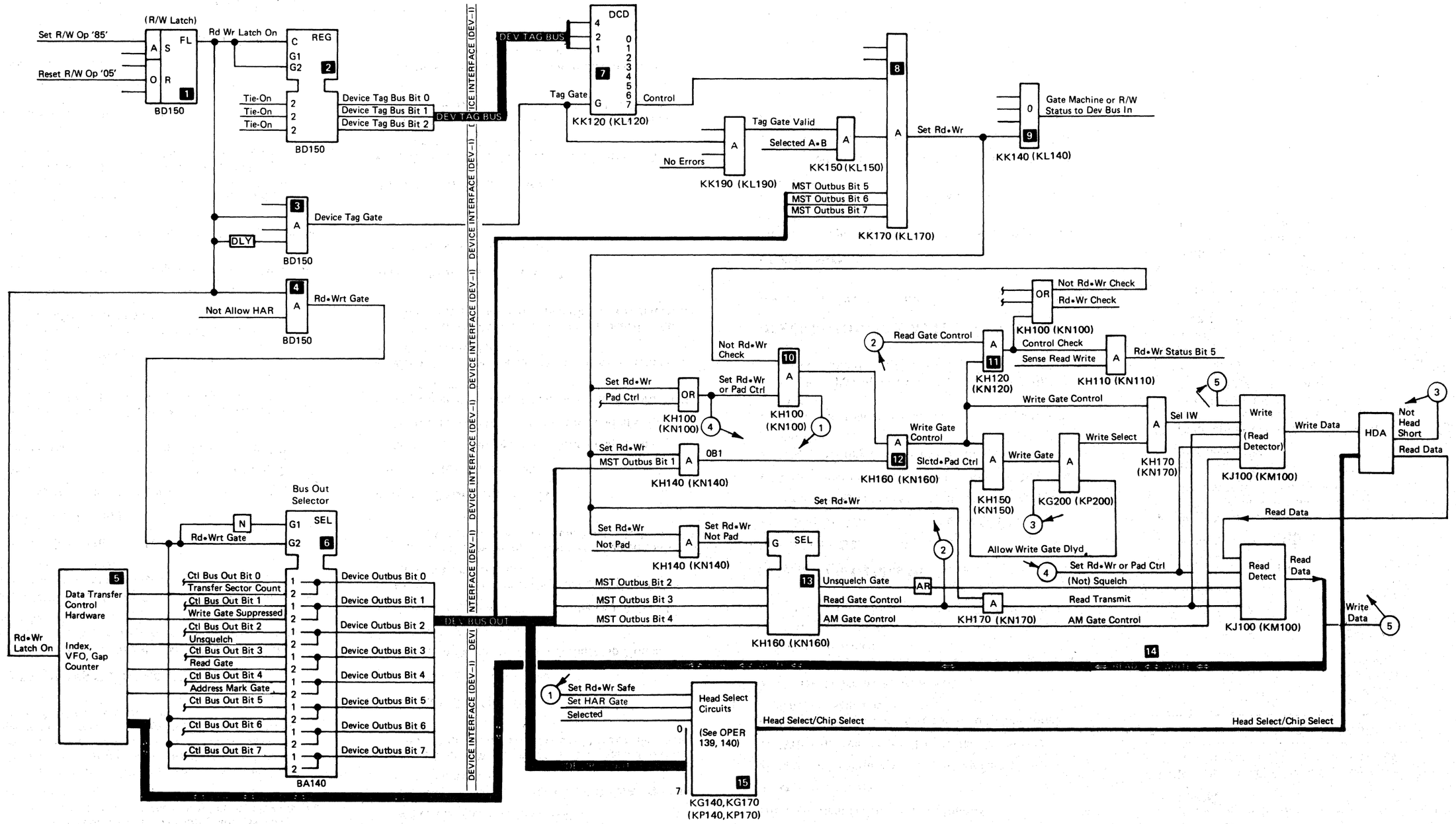
SET AND RESET READ/WRITE–TAGS '85' AND '05' **OPER 210**

SET AND RESET,READ/WRITE—TAGS '85' AND '05'



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WRITE-TAG '0F'

When the Write command is sent by the CPU to storage control, storage control (the microprogram) issues the appropriate chain of tags to the controller to carry out the Write command.

Note: *So that the R/W head can start from a known reference point on the track, the first tag operation in the chain is the one that establishes orientation: Format G1, Special Format G1, Read G1, or Read G3 AM Search.*

TYPES OF WRITE OPERATIONS

See OPER 99 and OPER 104 – Tag '0F', Bus Out bits 0 to 3 for the type of Write operation on Bus Out.

See OPER 33 and OPER 34 – for track format and gap-to-data-area relationships.

Write G2 (Bus Out = '2x')

Write G2 functions as follows:

- Sets up the Write operation during Gap 2 time.
- Writes the sync byte ('19') at the end of Gap 2.
- Writes the Key area, Data area, or Record 0 (R0) Count area.
- Turns off Write Gate at the end of the written area (after the ECC bytes have been written).

Format Reorient (Bus Out = '3x')

Format Reorient is initiated when a Count area indicates a skipped defect within its control.

Format Reorient functions as follows:

- Begins its operation in the gap immediately following the Count area.
- Reorients to the last byte before the ECC bytes of the preceding Data area.
- Turns off the Write Gate at Index time. (Write Gate is under the control of the Format latch at this time. The Format latch was set by the Format G3 operation that preceded the Format Reorient operation.)

Format G1 (Bus Out = '4x')

Format G1 functions as follows:

- **Orients** on Index.
- Sets up the Write operation during Gap 1 time.
- Writes the sync byte ('19') at the end of Gap 1.
- Writes the Home Address (HA).
- Keeps Write Gate on at the end of the HA area until Index is detected.

  (If no other Write operations are chained to this one, Write padding occurs until Index is detected).

Format G3 (Bus Out = '5x')

Format G3 functions as follows:

- Sets up the Write operation during Gap 3 time.
- Writes the Count area.
- Writes the sync byte ('19') at the end of Gap 3.
- Keeps Write Gate on at the end of the Count area until Index is detected.

  (If no other Write operations are chained to this one, Write padding occurs until Index is detected.)

Format G2 (Bus Out = '6x')

Format G2 functions as follows:

- Sets up the Write operation during Gap 2 time.
- Writes the sync byte ('19') at the end of Gap 2.
- Writes the Key area, Data area, or the Record 0 (R0) Count area.
- Keeps Write Gate on at the end of the written area until Index is detected.

  (If no other Write operations are chained to this one, Write padding occurs until Index is detected.)

Format/Erase (Bus Out = '7x')

Format/Erase functions as follows:

- Writes zeros to Index

Write G4 (Bus Out = 'Bx')

Write G4 is used to skip a track defect during a Write operation in one of two ways:

- Extends a normal gap (G1, G2, or G3) by adding a Gap 4 **before** the normal gap. (Gap 4 = 128 bytes, see OPER 33)
- Extends a defect gap when more than one defect occurs without intervening data.

Special Format G1 (Bus Out = 'Cx')

Special Format G1 functions as follows:

- **Orients** on Index
- Sets up the Write operation during Gap 1 time.
- Writes the sync byte ('19') at the end of Gap 1.
- Writes 128 bytes of zeros, followed by the normal Gap 1 to skip a defect.
- Writes the Home Address (HA)
- Keeps Write Gate on at the end of the HA area until Index is detected.

  (If no other Write operations are chained to this one, Write padding occurs until Index is detected.)

Special Write G2 (Bus Out = 'Ex')

Special Write G2:

- Sets up the Write operation during Gap 2 time.
- Writes the sync byte ('19') at the end of Gap 2.
- Writes the first segment of a Key area or Data area.
- Inhibits writing ECC bytes following the first segment.
- Causes the following Gap 2 to be increased to 128 bytes.
- Will be followed by a Write G2 to write the final segment and the ECC bytes.

DESCRIPTION OF A WRITE OPERATION

See the diagram on OPER 226.

Prerequisites

The microprogram prerequisites for a Write operation are as follows:

- The Controller and the drive must both be selected (Tag '83').
- Set Read/Write (Tag '85') must be latched.
- Tag Gate and Tag Bus must be latched to the drive.
- VFO must be locked in.
- Orientation must be established.

Sequence of Operation

1. Write command '0F' is placed on the CTL Tag Bus **1**.

CTL Bus Out contains a modifier that specifies the type of Write command and the pre-field gap **2**.

Bus Out bit	0	1	2	3	Operation
	0	0	1	0	Write G2
	0	0	1	1	Format Reorient
	0	1	0	0	Format G1
	0	1	0	1	Format G3
	0	1	1	0	Format G2
	0	1	1	1	Format/Erase
	1	0	1	1	Write G4
	1	1	0	0	Special Format G1
	1	1	1	0	Special Write G2

2. Write Gate is set **8**.
3. Write Mode is set **3**.
4. Write Mode enables generation of Sync In **4**, which indicates that the controller is ready to accept the first byte of data on Bus Out (Sync Byte '19').
5. Sync Out and the first byte of write data are transferred **5**.
6. Data on Bus Out is sent to the Data Register **6** and serialized by the Data Serializer **7** for recording on the disk surface. The controller is now in the data transfer mode.
7. The controller continues to transfer data until End Data is detected. The path between the ECC Shift register and the SERDES Shift register **9** is enabled. Six bytes of ECC are transferred from the ECC Shift register, through the SERDES Shift register, and recorded at the end of the data field.
8. After End Data is detected, the controller resets the Write Op latch and activates Normal End to the user if there are no check conditions. The user answers with End Response.

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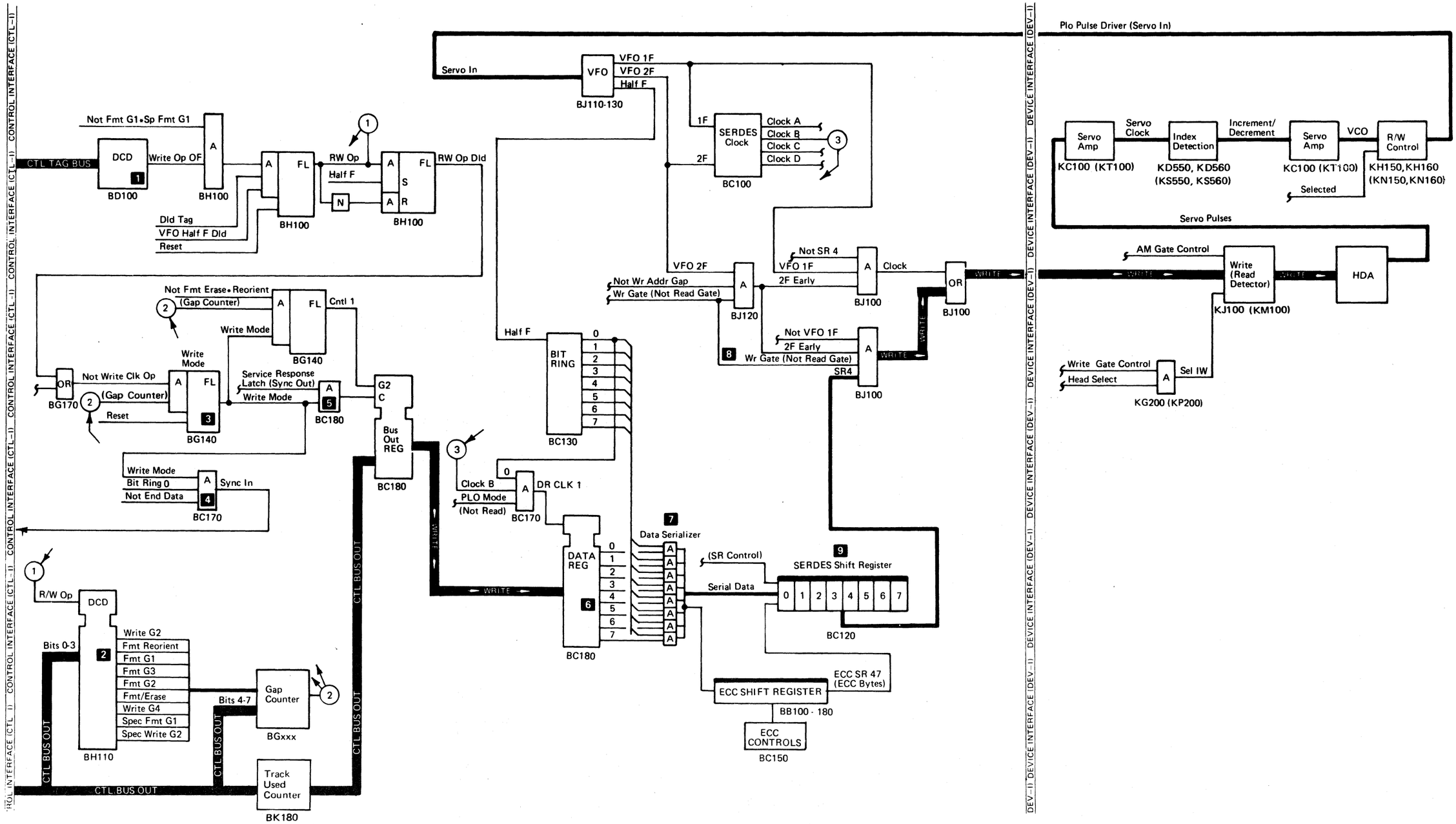

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WRITE PADDING

Write padding is the writing of bytes of zeros on the remaining portion of a track. The padding bytes are written until the next Index Mark. Write padding occurs immediately after writing during a Format Write command. When successive Write commands are issued and any one of them is a Format Write command (FMT G1, FMT G2, or FMT G3), padding starts immediately following the last command even if the last Write command is not a Format Write command. The following command sequence is an example:

FMT G3 (Create a Count field)
WR G2 (Create a Key field)
WR G2 (Create a Data field)

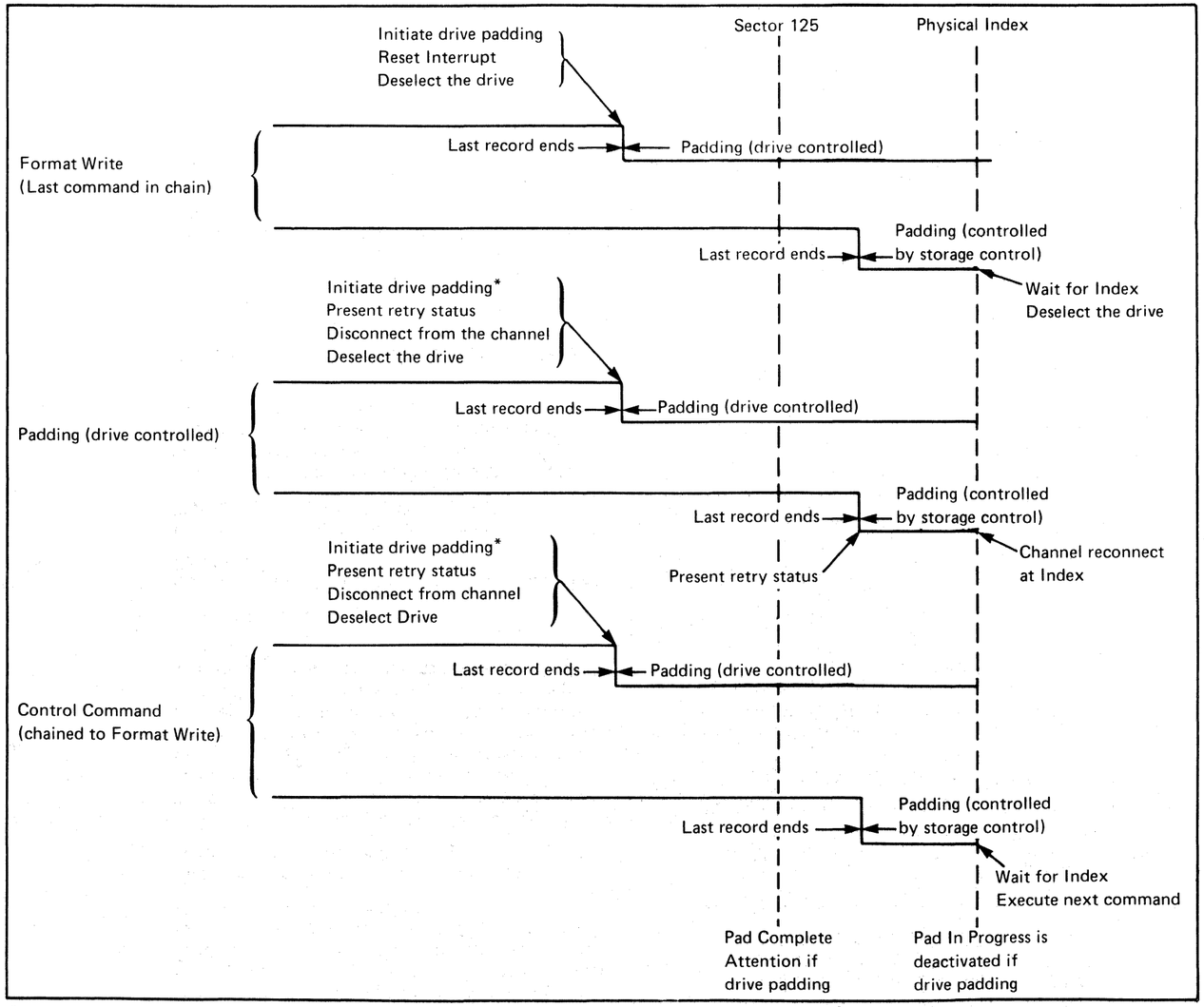
Padding that was specified by the FMT G3 operation starts following the last WR G2 operation.

In 3330-1 Mode, write padding is initiated and controlled by storage control.

In 3330-11 Mode or in 3350 Native Mode, write padding is initiated by storage control and controlled by the storage control or by the drive. The drive controls write padding that begins prior to disk sector 125. The storage control controls padding that begins in or after disk sector 125 by maintaining Write mode in the controller until Index time. Figure 1 represents the operation of write padding with various command chaining/non-chaining applications.

If a new chain is started on a drive that is padding, the storage control accepts the SIO command but waits to execute the command (except TIO and Sense commands) until padding is complete.

Figure 1. Write Padding



*Index orientation is not ensured upon reconnection.

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When a Read command is sent by the CPU to storage control, storage control (the microprogram) issues the appropriate tags to the controller to carry out the Read operation. For example, the appropriate chain of tags for a Read Data command ('06') might be:

1. Read G3,Tag '0E', Bus '5x'
2. Clock G2,Tag '0E', Bus '2x'
3. Read G2,Tag '0E', Bus '6x'

Note that the tag chain must always begin with either a Read G1 or a Read G3 AM Search for track orientation, so the read head can start reading from a known reference point.

TYPES OF READ OPERATIONS

These operations are defined by bits 0 through 3 of Bus Out during Tag '0E'. See OPER 99 and OPER 103.

See also: Track Format on OPER 33 and 34 for gap-to-read area relationships.

Clock G3 (Bus Out = '1x')

Clock G3 functions as follows:

- Sets up the Read operation during Gap 3.
- Clocks over the Count area that follows the gap, while maintaining track orientation.

Clock G2 (Bus Out = '2x')

Clock G2 functions as follows:

- Sets up the Read operation during Gap 2.
- Clocks over the Key or Data area that follows the gap, while maintaining track orientation.

Read G4 (Bus Out = '3x')

Read G4 functions as follows:

- Clocks over the 128-byte gap for a skipped defect.
- Is followed by a Read G2 to read the next area on the track.

Read G1 (Bus Out = '4x')

Read G1 functions as follows:

- **Orients** on Index
- Sets up the Read operation during Gap 1.
- Reads the Home Address area.

Read G3 (Bus Out = '5x')

Read G3 functions as follows:

- Sets up the Read operation during Gap 3.
- Reads the Count area (except R0 Count area).

Read G2 (Bus Out = '6x')

Read G2 functions as follows:

- Sets up the Read operation during Gap 2.
- Reads the Key area, Data area, or the R0 Count area.

Read G3 AM Search (Bus Out = '7x')

Read G3 AM Search functions as follows:

- Sets up the Read operation.
- **Orients** on the Address Mark (AM) in Gap 3. (**Note:** If Index is detected before the Address Mark, No AM Found is posted and the microprogram orients on Index and issues a Read G1.)
- Reads the Count area that follows the Gap (except R0 Count area).

Special Read G2 (Bus Out = 'Ex')

Special Read G2 functions as follows:

- Sets up the Read operation
- Reads the first part of the Key or Data area that has been split for defect skipping.
- Saves the ECC Shift Register contents at the end of the data transfer.
- Sets up conditions to process a 128-byte gap for a following Read G2 operation.

DESCRIPTION OF A READ OPERATION (Read G1)

See the diagram on OPER 231 and the timing chart on OPER 232.

Sequence of Operation

1. Read Op Tag '0E' is placed on Ctl Tag Bus. Ctl Bus Out contains a modifier in bits 0 through 3 that specifies the Read G1 operation (0100) 1. Ctl Bus Out bits 4 through 7 contain the modulo count (units digit of the hex byte count) and are latched for future use by the gap counter 5. For a Read G1, the modulo count is always 9.
2. Tag Valid is returned to the storage control if there are no control interface errors 8.
3. At Index time, orientation is established 2 and the gap counter is reset. The gap counter starts counting and at count-64 time, Read Gate is raised to the drive 6. At count-76 time, Unsquelch is raised to the drive 6. Device Bus Out bits 2 and 3 are used to transfer these controls to the selected drive 7. These controls are necessary to amplify and transfer read data from the selected drive to the controller 3.
4. Count 102 resets the gap counter.
5. Count 1 time locks VFO to data and activates VFO Fast Sync 9.
6. Count 8 resets VFO Fast Sync and gates Standardized Data to SERDES 10.
7. When a sync byte is detected in SERDES, Data Good causes Read Mode to become active 4. The gap counter is set to the 15s complement of the modulo count. For a Read G1, the complemented modulo count is 1.

   Bit ring 7 transfers the sync byte from SERDES to the data register 11.

   During the next complete bit ring cycle the first data byte is assembled in SERDES. At bit ring 1 time of that cycle, Sync In is sent to the storage control and the sync byte is placed on Ctl Bus In 13.
8. At the next bit ring 4 time, the gap counter is stepped to 2.
9. Bit ring 7 transfers the first data byte to the data register. Bit ring 1 of the next bit ring cycle activates Sync In to the storage control with the data byte on Ctl Bus In. Bit ring 4 increments the gap counter to 3. The next data byte is being assembled in SERDES and is ready to be transferred to the data register at bit ring 7 time.
10. **Data transfer continues until the gap counter reaches 15. Read Mode is reset and prevents any further data transfer 4.**

    Count 15 also activates Transfer ECC Control to allow the next byte (first ECC byte) to be gated to the ECC Shift Register 12.
11. The six ECC bytes are transferred to the ECC Shift Register. If ECC Zeros Compare is active after the six ECC bytes are transferred, ECC Data Check is blocked.
12. Op End is activated and Normal End is sent to the storage control provided no errors have occurred 14.
13. End Response is returned from the storage control and Reset End condition is activated in the controller.

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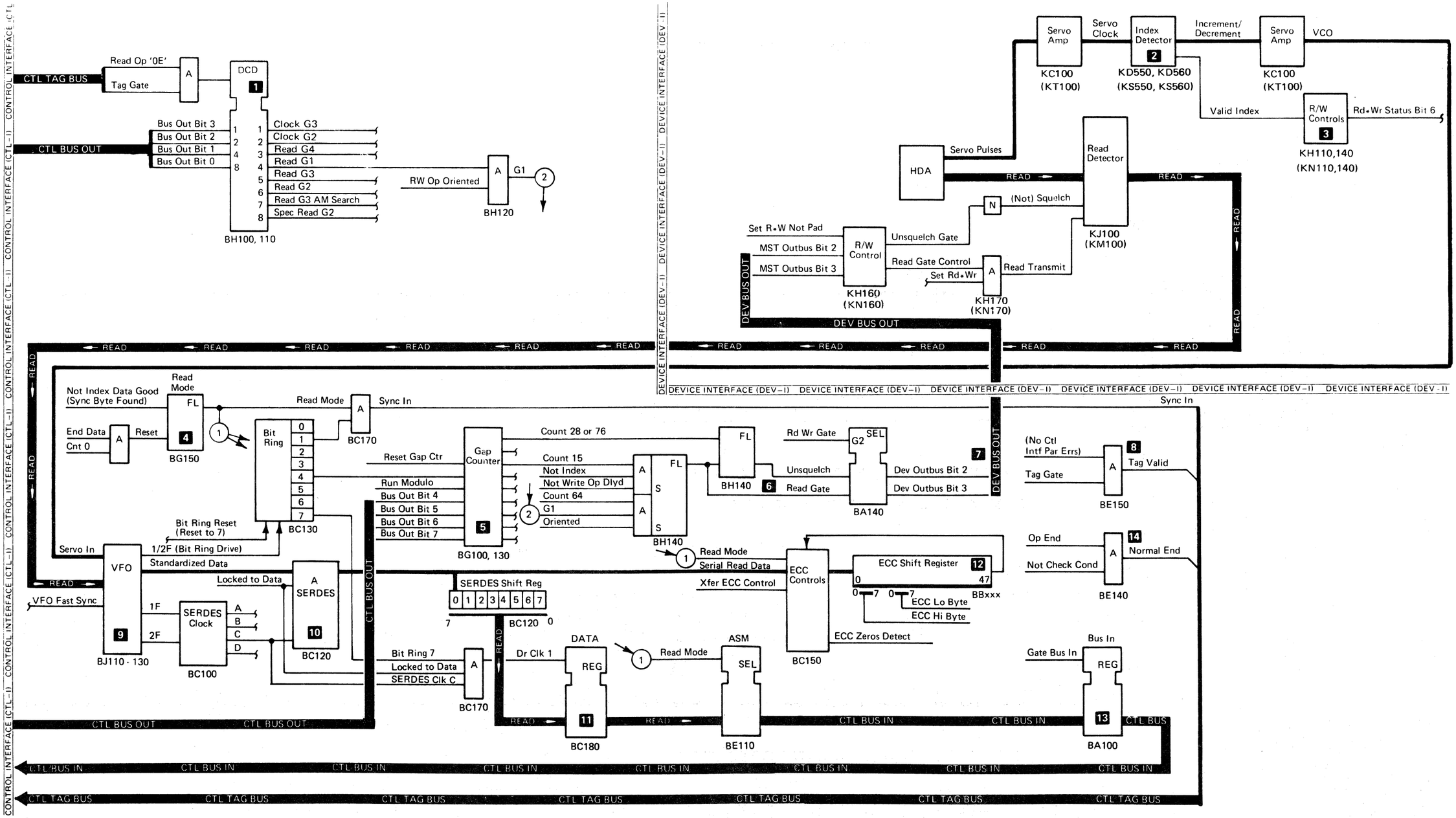
READ—TAG '0E'



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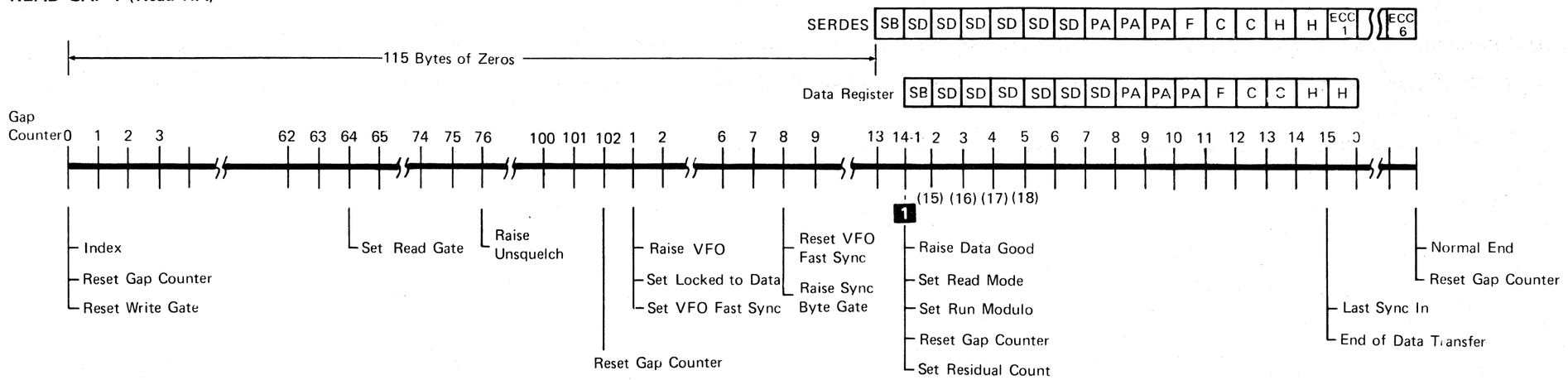
READ G1/G2 TIMING REFERENCE

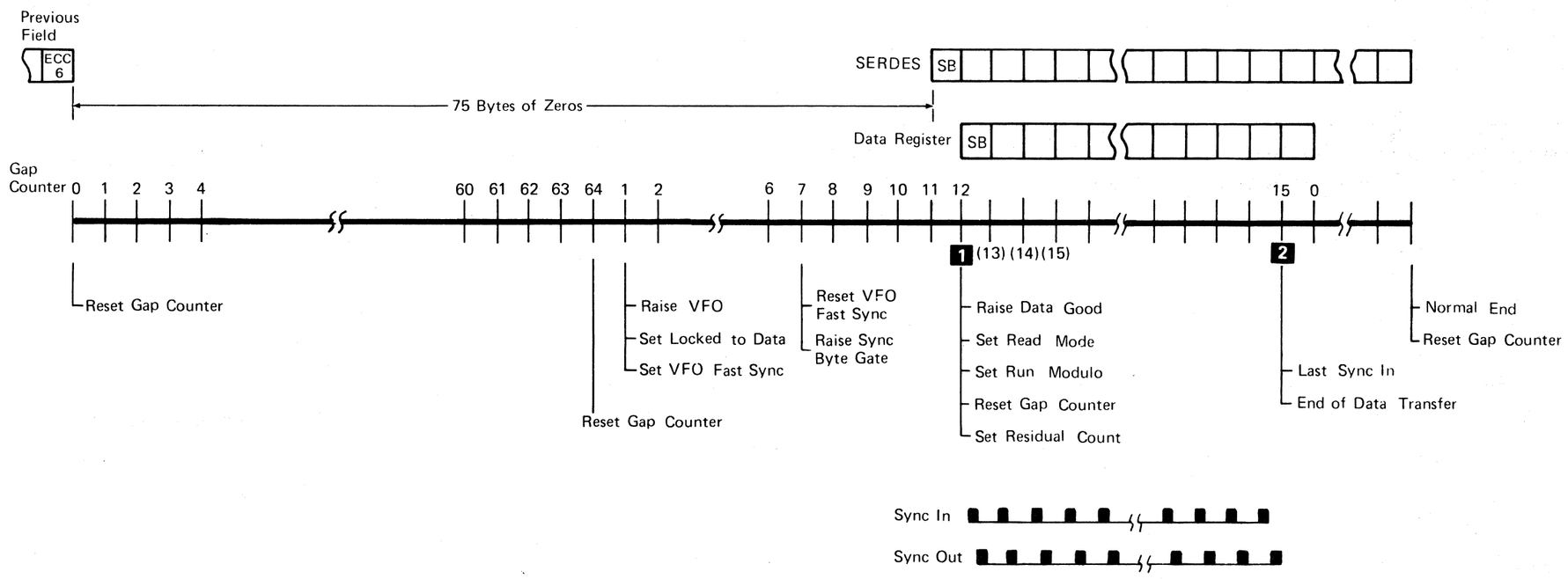
READ GAP 1 (Read HA)



Legend

SB = Sync Byte
SD = Skip Displacement
PA = Physical Address
F = Flag
C = Cylinder
H = Head
ECC = Error Correction Code

READ GAP 2 (Read Key, Data, R0 Count)



1

The sync byte (SB) is recognized during the period from count 8 to count 21. When the sync byte is detected in SERDES, the gap counter is reset to the complement of the Modulo-16 count (Bus Out bits 4 to 7 of Tag '0E'). The sync byte detection activates Data Good.

If the count reaches 21 while performing a Read G1, a skipped defect is assumed and at count 128 the Gap Counter is reset to zero and a new attempt is made to detect the sync byte.

If the count reaches 21 while performing a Read G2 to Read G3, a Check End results and No Sync Byte Found is sent to storage control.

2

When the number of bytes to be transferred is greater than 15:

1. *The complement of the Modulo-16 counter is set into the Gap Counter. (The value in the Modulo-16 counter is the remainder, if any, obtained by dividing the byte count by 15.)*
2. *The Recycle Tag line prevents End Data from being activated until the Gap Counter has counted to 15 for X number of times. (X = the number of bytes transferred, divided by 15.)*

See OPER 94 for a description of the Recycle Tag line.

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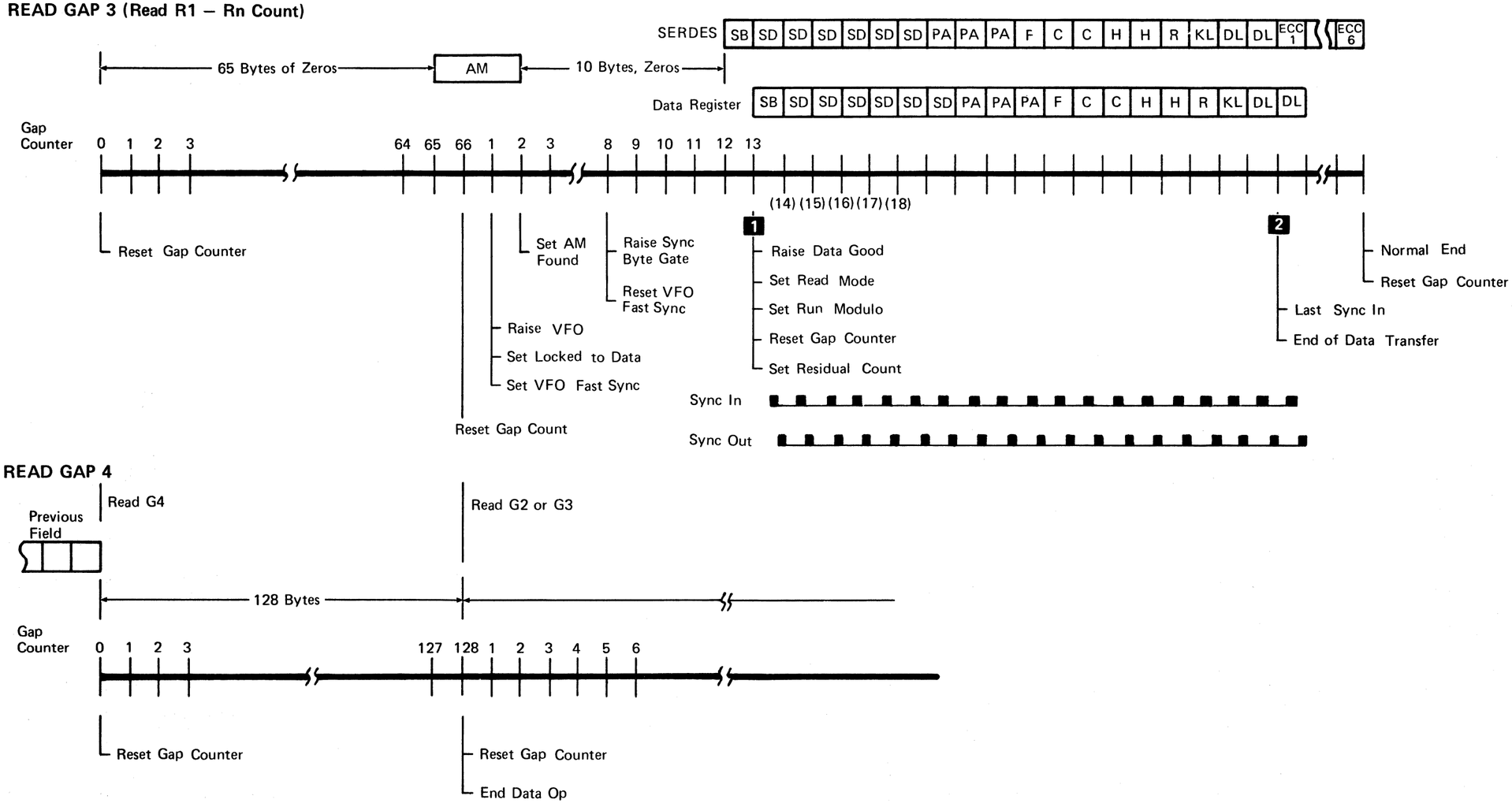
READ G3/G4 TIMING REFERENCE

READ GAP 3 (Read R1 – Rn Count)



READ GAP 4

See 1 *on OPER 232*

See 2 *on OPER 232.*

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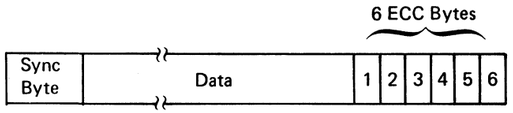
ECC (ERROR CORRECTION CODE)

See OPER 236 for timing diagram .

Each area on the disk (Home Address, Count, Key, or Data) includes six bytes of hardware-generated Error Correction Code (ECC) information. The ECC bytes are the last six bytes of each area.



The ECC bytes are used for both error detection and error correction and are referred to as either Detection Code bytes, or Correction Code bytes.

The six ECC bytes added to the Home Address area, Count area, or Key area, provide error detection capability. They are called Detection Code Bytes (DCBs).

The six ECC bytes added to Data areas provide error correction as well as error detection capabilities and are called Correction Code Bytes (CCBs).

The DCB and CCB detect any error burst of a 10-bit span or less. The CCB can be used to correct errors of a 4-bit span or less.

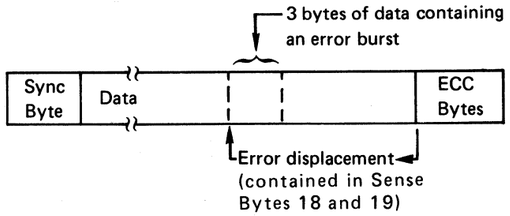
As the data plus the six ECC bytes are shifted through the ECC Shift Register, the data is divided by the generator polynomial. If there are no data errors, the contents of the ECC Shift Register is zero after shifting the six ECC bytes, giving ECC Zeros Compare. The detection of zeros inhibits the setting of the ECC Data Check latch at End Data Op time (approximately 7.84 microseconds after Transfer ECC latch is set).

Op End is enabled with the setting of End Data Op and activates Normal End to the user. The user responds with End Response, resetting End Data, End Data Op, and Normal End. If the remainder in the ECC Shift Register is not zero, the ECC Data Check latch is set by End Data Op time and Check End is raised under Op End. The storage control issues an ECC Correct Op (Tag '08') starting error correction procedures. A constant of 19,544 is set into a counter and the ECC Shift Register shifts. The storage control counter is decremented as a result of Sync In pulses until zeros are detected in Shift Register positions 3 through 47 (SR3 to SR47) or the counter is decremented to zero.

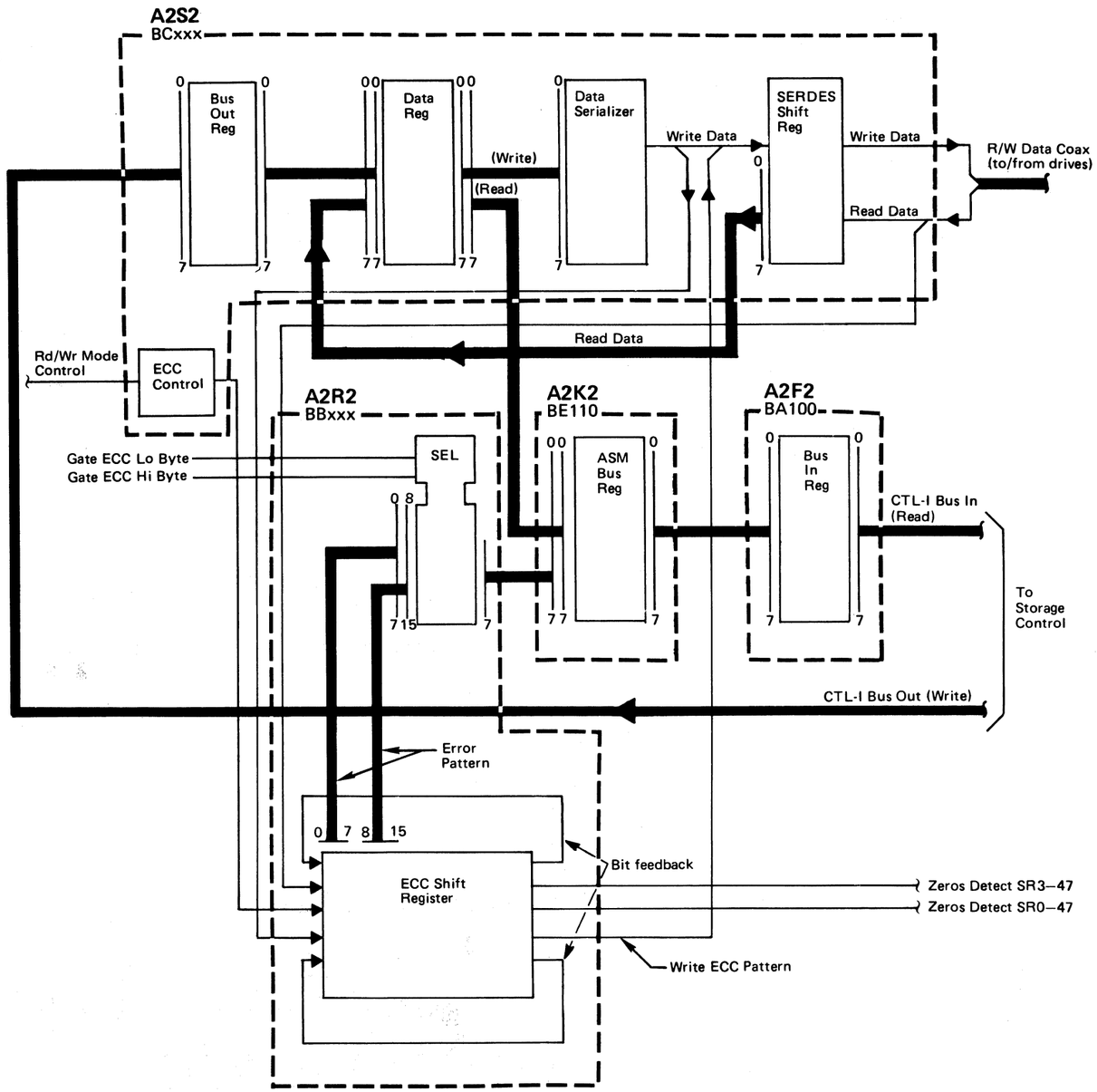
After zeros are detected in SR3 to SR47, the Shift Register continues shifting bits until the next byte boundary is reached. The error correction pattern is now contained in the ECC Shift Register positions 0 to 15.

The pattern is gated to storage control by control Tag '04' (read correction bytes) and Bus Out bit 8 (gate ECC low byte, ECC Shift Register position 0 to 7) and Bus Out bit 1 (gate ECC Hi byte, ECC Shift Register position 8 to 15).

The error pattern is placed in Sense Bytes 20, 21, and 22 (Sense Byte 22 contains all logical zeros). The storage control calculates the displacement of the error from the last byte of data. The error displacement is placed in Sense Bytes 18 and 19.



Error correction is accomplished by aligning the error pattern from Sense Bytes 20, 21, and 22 with the erroneous data from storage and exclusive ORing the pattern with the erroneous data.



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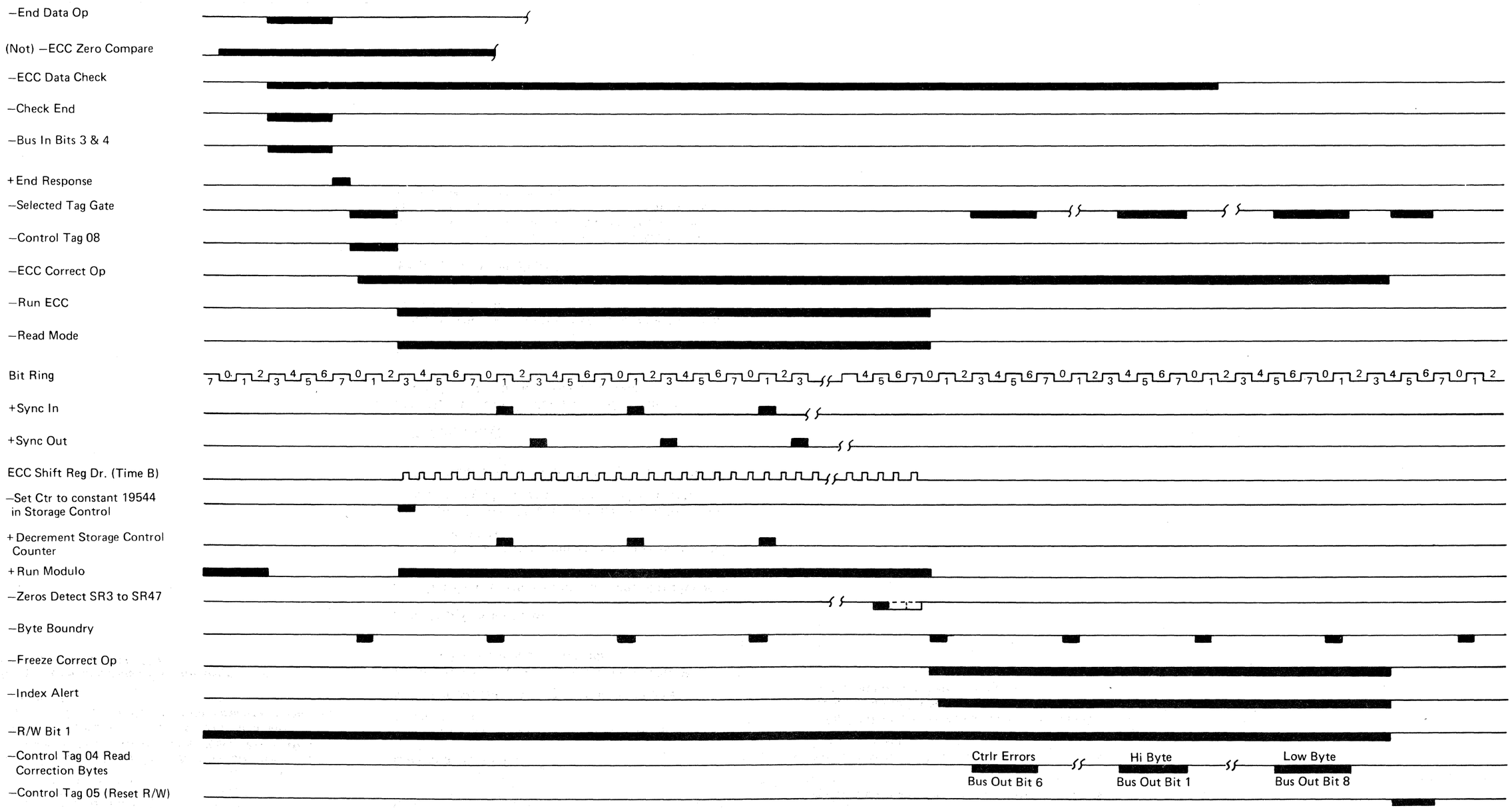
ECC (ERROR CORRECTION CODE)



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All abnormal or unexpected conditions in the controller are considered error conditions. Controller error conditions are classified as one of two conditions:

- Check End conditions
- Error Alert conditions

Note: *All errors (controller errors, or otherwise) are identified in Status Bytes, Sense Bytes, Error Message bytes, or Console Display Bytes. This summary is provided only to describe the error detecting circuits in the controller.*

Always begin maintenance or troubleshooting procedures on START 100.

CHECK END

Check End errors occur at the end of Read or Write operations when abnormal conditions occur (not Normal End).

Command Overrun

Command Overrun indicates that one of two possible conditions exist:

- A nonoriented Write tag exists at Index time.
- An oriented type tag is attempting a Read or Write operation in a nonoriented mode.

Sync Out Timing Error

Sync Out Timing Error indicates that one of the following conditions occurred:

- Sync Out pulses were more than 2 pulses behind the Sync In pulses.
- A Sync Out signal that was not a response to a prior Sync In signal was detected on the Control Interface.
- Data transfer ended without enough Sync Out pulses.

ECC Data Check

ECC Data Check indicates that the ECC circuits detected a Data Check in the data stream.

Track Overrun

Track Overrun indicates that a Write operation was still active at Index time.

No Address Mark Found

No Address Mark Found indicates that a Read G3 AM Search tag failed to identify an Address Mark. (This may mean that an Index Mark occurred prior to an Address Mark under an AM Search tag.)

No Sync Byte Found

No Sync Byte Found indicates that one of three conditions occurred:

- No Sync Byte was detected in the Home Address area.
- No Sync Byte was detected in either the Gap 2 or Gap 3 area being searched.
- A false Address Mark was detected. (A void or erased area was found that was similar to an Address Mark, but no Sync Byte was found.)

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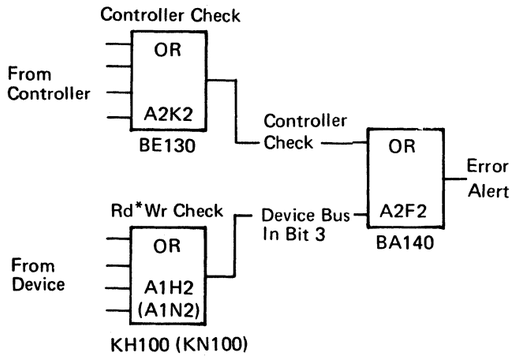
CONTROLLER ERROR CONDITIONS – SUMMARY

ERROR ALERT

Error Alert errors are either *controller* errors or indications that conditions exist that could endanger data integrity during Read or Write operations.

Error Alert errors from the *controller* are indicated by a Control Check.

Error Alert errors from the *drive* are indicated by a Read * Write Check.



VFO Detected Errors (Controller Check)

The VFO Detected Error bits (bits 0 and 1) together indicate whether an error occurred and the type of error:

VFO Error Bit 0	VFO Error Bit 1	Error
0	0	No error
0	1	Missing Servo input
1	0	VFO phase error during a Write operation.
1	1	Missing data input

SERDES Check (Control Check)

SERDES Check indicates that the SERDES Shift Register parity did not match its predicted parity.

Gap Counter Check (Controller Check)

Gap Counter Check indicates that incorrect parity was detected in the Gap Counter.

Write Data Check (Controller Check)

Write Data Check indicates that parity did not match parity of the data byte received from storage control.

Monitor Check (Controller Check)

Monitor Check indicates that there is a high probability the controller will stop functioning because of one or more of the following conditions:

- The Bit Ring is stopped.
- The Gap Counter is stopped.
- Sync In was missing for six consecutive byte times.
- Raw Read data was missing during an AM Search.

ECC Check (Controller Check)

ECC Check indicates that an ECC control failure or an ECC parity error has occurred.

Control Tag Bus Parity Check (Controller Check)

Control Tag Bus Parity Check indicates that a parity error was detected on the Control Interface Tag Bus while Tag Gate was active.

Control Bus Out Parity Check (Controller Check)

Control Bus Out Parity Check indicates that a parity error was detected on Control Interface Bus Out while Tag Gate was active.

Drive Selection Check (Controller Check)

Drive Selection Check indicates that more than one drive or no drive was selected.

Device Bus In Parity Check (Controller Check)

Device Bus In Parity Check indicates that a parity error was detected on Device Bus In.

Control Bus In Parity Check (Controller Check)

Control Bus In Parity Check indicates that a parity error was detected on Control Interface Bus in.

I Write Fail (Controller Check)

I Write Fail indicates that I Write Sense was not detected in the drive within approximately nine microseconds after the rise of Write Gate.

TR Index Check (Controller Check)

In 3330 mode, the TR Index Check indicates that an error occurred in the Track Used Counter circuitry.

Reorient Counter Check (Controller Check)

Reorient Counter Check indicates that an error occurred in the Reorient Counter circuitry.

Multiple Chip Select Check (Rd * Wr Check)

Multiple Chip Select Check indicates that more than one Chip (for 4 R/W heads) was selected in the HDA of the selected drive.

Capable/Enable Check (Rd * Wr Check)

Capable/Enable Check indicates that one of the following conditions occurred:

- Writing was attempted with the Read/Write switch set to Read Only.
- Reading or Writing was attempted with the drive not Ready or with the servo not Track Following.

Write Overrun (Rd * Wr Check)

Write Overrun indicates that writing was attempted through an Index Mark. (Writing into or out of Index is valid.)

Index Check (Rd * Wr Check)

Index Check indicates that an invalid Index pattern was detected while Set Read/Write was present.

Delta I Write Check (Rd * Wr Check)

Delta I Write Check indicates that one of the following conditions occurred:

- Writing was attempted on an even numbered movable head or on a fixed head, and Delta Write current was not detected.
- Writing was attempted on an odd numbered movable head and Delta Write current was detected.

Head Short Check (Rd * Wr Check)

Head Short Check indicates that more than one head was selected (detected as being on) at the same time, in the selected drive.

Control Check (Rd * Wr Check)

Control Check indicates that the Write Gate signal was present with the Unsquelch or Read Gate signals.

Pad Gate Error (Rd * Wr Check)

Pad Gate Error indicates that Write padding was attempted through an Index Mark.

Write Transition Check (Rd * Wr Check)

Write Transition Check indicates that one of the following conditions occurred:

- Write transitions were not detected within four microseconds (nominal) after Write Gate was turned on.
- Write transitions were present when Write Gate was turned off.
- Write transitions were detected while reading.

Write Current Check (Rd * Wr Check)

Write Current Check indicates that one of the following conditions occurred:

- No Write current was detected during a Write operation.
- Write current was detected while reading.

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FIXED HEADS – MODEL A2F, B2F, AND C2F

There are six 3350 models available:

A2: Control module without fixed heads.
B2: Satellite module without fixed heads.
C2: Alternate control module without fixed heads.
A2F: Control module with fixed heads.
B2F: Satellite module with fixed heads.
C2F: Alternate control module with fixed heads.

Models A2F, B2F, and C2F each have 60 additional Read/Write heads in the HDA. The heads are fixed in position, one to a data track, on the servo surface. (See the HDA description on OPER 32.)

The HDA capacity is the same for all models.

In 3350 Mode, cylinders 1 and 2 are located on the fixed head tracks *instead of* on the movable head tracks. Cylinder 1 is under the first 30 fixed heads; cylinder 2 is under the second 30 fixed heads.

In 3330 Mode, cylinders 1, 2, and 3 are located on the fixed head tracks *instead of* on the movable head tracks. Cylinder 1 is located under fixed heads 0 through 18; cylinder 2 is located under fixed heads 19 through 37; cylinder 3 is located under fixed heads 38 through 56. (Fixed heads 57, 58, and 59 are not used.)

Reference pages:

Physical location on the HDA, OPER 32.
Head Select logic, OPER 140.

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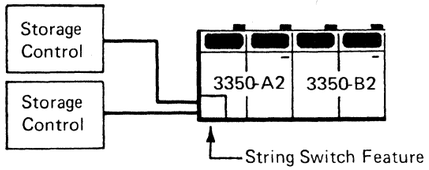
STRING SWITCH FEATURE

The string switch feature allows an IBM 3350 Disk Storage to be physically connected to two storage controls. Only one storage control is logically connected to the 3350 at any time.

For information on the C2 Module string switch feature, see OPER 270 and FSI 980.



OPERATION

1. Storage control A(B) **1** places a controller address on Ctl Bus Out and a Tag '03' or a Tag '83' on Ctl Tag Bus.
2. Controller A(B) Address Compare **2** generates Adr Compare Eq A(B) when Ctl Bus Out bits 0, 1, 2 equal the controller address bits Wired Adr 1, 2, 4.
3. Adr Compare Eq A(B) allows Tag Bus Decoder A(B) **3** to generate Decoded Tags and Selecting A(B) from the Ctl Tag Bus bits 0, 4 through 7.
4. Interface A(B) Out-In Control Select (Tie Breaker) **4** generates Allow Sel Set A(B) from Enable A(B). See Enable/Disable switch A(B) on this page.
5. Allow Sel Set A(B) allows Interface A(B) Out-In Control **5** to generate Cnt Pwr 1, Cnt Pwr 2, and In Code 1, 2.
6. Cnt Pwr 1 gates Ctl Bus Out bits 0 through 7, P through the Bus Out A(B) Gate **6** to the following:

   Polling and Selection **9** in the controller.

   Drive Address Compare **10** in the drive.
7. Cnt Pwr 2 gates Ctl Tag Bus bits 0, 4 through 7, P through the Tag Out A(B) Gate **7** to Polling and Selection **9** in the controller.
8. In Code 1, 2 gates Bus In Asm Bits 0 through 7, P through the Bus In A(B) Register **8** onto Ctl Bus In.

ENABLE/DISABLE SWITCH A(B)

The Enable/Disable switches A and B allow one or both storage controls to be connected to/disconnected from the 3350 Disk Storage.

The Enable/Disable switches A and B are located on the 3350-A2 Power Panel.

ALTERNATE PATH RECOVERY

This function uses an Unconditional Reserve (UR) command to break device allocation to the primary path, that has become inoperative, and establishes an alternate path within the system.

Unconditional Reserve

If a storage control attached to a string of 3350 drives with string switch feature stops operating while an interface is selected or an assignment register position is set, no operation to the string or effected drive is possible from another storage control.

To elimnate this condition the select latch and assignment register positions can be reset through the use of the Unconditional Reserve (UR) command. Once the select latch and/or assignment register positions for the desired drive(s) have been reset, the string is reserved for the storage control through which the UR Command was issued and normal operation may continue on the functional interface.

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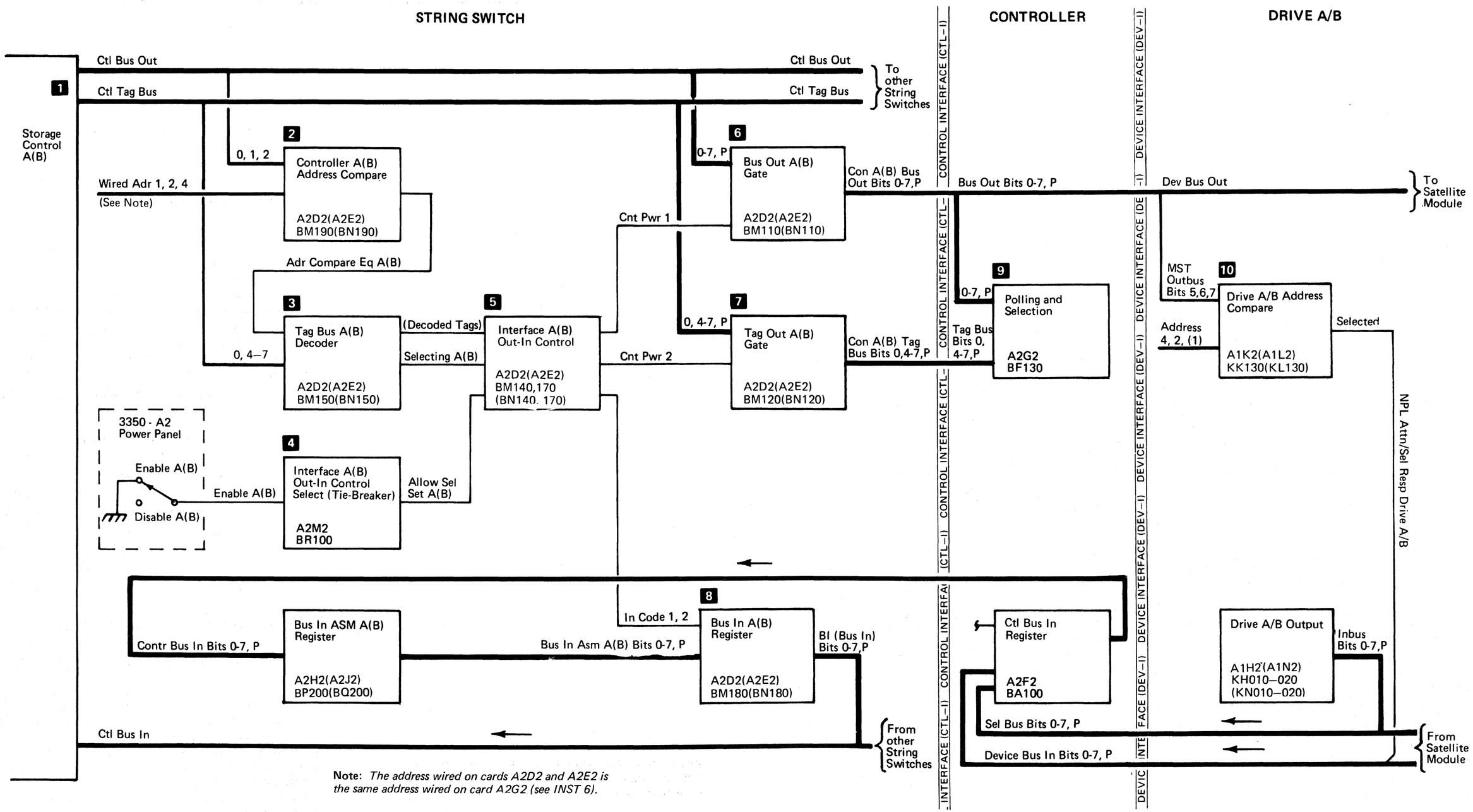
STRING SWITCH FEATURE



Note: *The address wired on cards A2D2 and A2E2 is the same address wired on card A2G2 (see INST 6).*

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ALTERNATE CONTROLLER FEATURE (C2 Module)

The Alternate Controller feature adds a second control module (C2) to the 3350 string. The C2 Module contains two drives and a controller board. The string configuration consists of 4, 6, or 8 drives that can be accessed by either the A2 of C2 controller over a common device interface. All drives, but only one controller, can be online running customer programs. The offline controller has the capability of running microdiagnostics inline while customer programs are running.

PRIMARY/ALTERNATE SWITCH

The Primary/Alternate switch is located on the Controller Select Panel of the C2 Module and determines which controller is online.

With the Primary/Alternate switch set to Primary:

- The A2 controller is online.
- The C2 controller is offline.

With the Primary/Alternate switch set to Alternate:

- The A2 controller is offline.
- The C2 controller is online.

To change the status of the controllers:

1. Power off the 3350 string.
2. Change the Primary/Alternate switch setting.
3. Power on the 3350 string.

CONTROLLER ADDRESSING

Both controllers (A2 and C2) have the same address plugged during installation. The high-order address bit is off and the two low-order bits are plugged as required to give addresses 0, 1, 2, or 3. The online controller address is the same as the address plugged on installation. The Primary/Alternate switch forces on the high-order address bit in the offline controller. This gives the online controller addresses 0, 1, 2, or 3 and the offline controller addresses 4, 5, 6, or 7. The functional microcode accepts only addresses 0, 1, 2, and 3 while the diagnostic microcode accepts addresses 0 through 7.

STRING SWITCH FEATURE OPERATION

With each controller having a unique address, the use of a common device interface causes no problems during string switch operation. String switch microdiagnostics cannot be run from the offline controller while customer programs are running on the online controller.

POWER CONTROL

The offline controller can be powered off for maintenance while the online controller is being used by the customer. See service notes on FSI 970 for the power off procedure.

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Power Sequencing (without C2) . PWR 6
Power Sequencing (with C2) . . PWR 306

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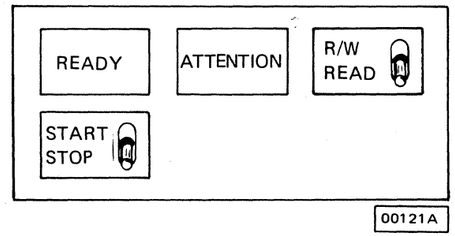
3350 OPERATOR PANEL



READY Indicator

Lights when the HDA has sequenced to Ready with no errors.

START/STOP Switch

In the Start position, the drive motor starts turning and the heads are moved to track 0 (see HDA 500 to HDA 502).

In the Stop position, the Ready lamp is turned off, the carriage is moved to Home position, and the voltage is then dropped to the drive motor. The drive stop sequence is inhibited if it is selected and Set Read/Write is active, or if the drive is selected and busy (see HDA 504 to HDA 506).

R/W or READ Switch

In the R/W position, the drive is write enabled.

In the Read position, the drive is write inhibited.

If the drive is selected, it cannot switch from Read to Write mode or from Write to Read mode. The drive remains in this condition until it is deselected.

ATTENTION Pushbutton

Pressing the pushbutton causes a Rezero operation:

1. Read/Write heads are moved to track 0.
2. Seek Complete Attention is signaled to the controller when the Rezero operation is complete.

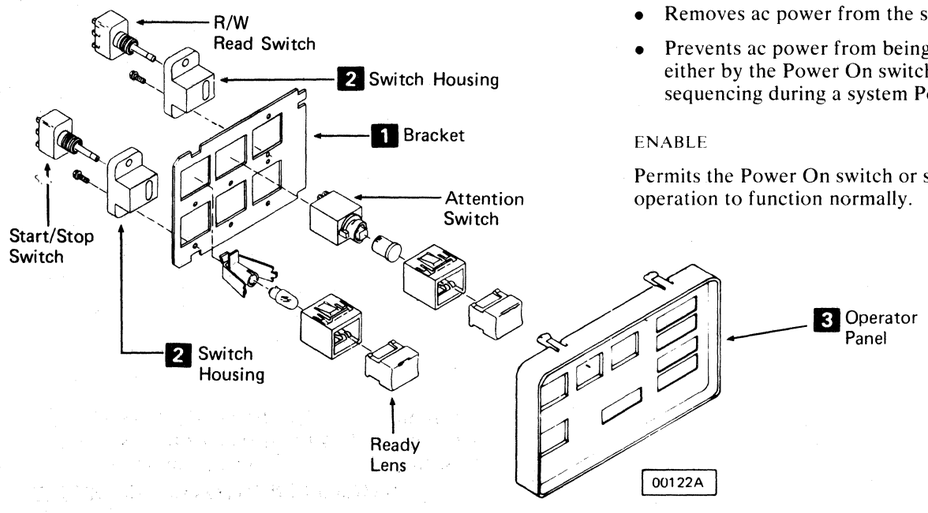
OPERATOR PANEL SWITCH REMOVAL and REPLACEMENT

Removal

1. Remove all lens covers.
2. Pull the Operator Panel **3** up and out of the front cover.
3. Lift the bracket **1** up and out from the front cover.
4. Remove the switch housing **2**.
5. Note the position of the wires and remove them from the rear of the switch.
6. Loosen the lock nut on the switch. Unscrew and remove the switch from the housing.

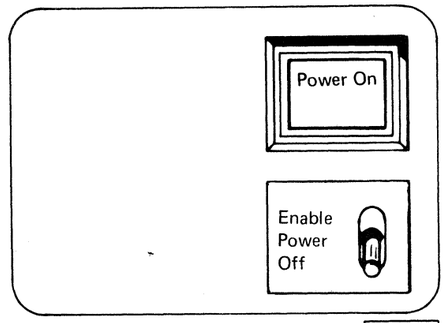
Replacement

Replace in the reverse order of removal.



8xx POWER PANEL

A2 Module (Standard)



Power On Switch

Pressing the Power On switch allows ac power to be applied to the string if the Power Off/Enable switch is in the Enable position. The switch is bypassed by the subsystem sequencing controls during a system Power-On operation if the CE Panel Power Mode switch is in the Remote position.

Power Off/Enable Switch

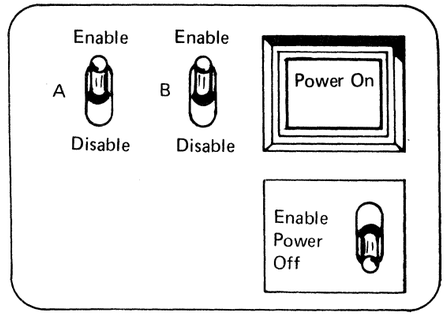
OFF

- Removes ac power from the string.
- Prevents ac power from being applied to the string either by the Power On switch or by subsystem sequencing during a system Power On operation.

ENABLE

Permits the Power On switch or system Power On operation to function normally.

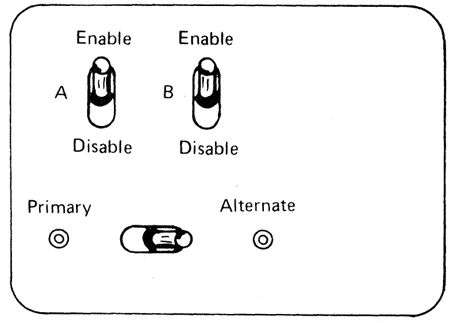
A2 Module (String Switch)



Enable/Disable Switches

The Enable/Disable switches (A or B) can be used to dedicate the 3350-A2 and associated drives to a single interface. Interlocking is provided. Machines without the string switch feature do not have these switches.

C2 Module (String Switch)



Primary/Alternate Switch (String Switch)

The Primary/Alternate switch determines which controller is operating.

With switch set to Primary:
A2 controller is online, C2 controller is offline.

With switch set to Alternate:
A2 controller is offline, C2 controller is online.

To change the status of controllers:

1. Power off the 3350 string.
2. Change the Primary/Alternate switch setting.
3. Power on the 3350 string.

Changing the Primary/Alternate switch setting with the power on does not change the status of the controllers.

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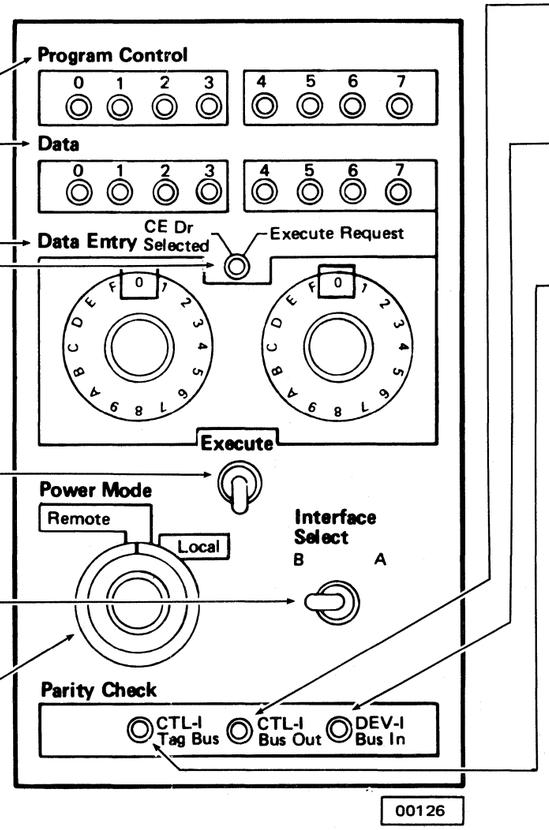
CE CONTROLS

CE PANEL CONTROLS

The CE Panel (under the lower rear covers of the A2 and C2 Modules):

- Communicates with the storage control to initiate and control microdiagnostics from the 3350-A2 or C2 Module. (See MICRO 10 and 11.)
- Removes the 3350 string from system power sequencing.
- Resets various drive circuits.



Program Control and Data Displays

Program Control and Data display receive information from the storage control to the 3350-A2 or C2 Module. For a description of Program Control displays and their corresponding Data displays, see MICRO 10 and 11.

Data Entry Switches

The Data Entry switches are used in conjunction with the Execute switch to send information to the storage control. Examples are:

- Microdiagnostic routine and test numbers.
- Test parameters.
- Running options.

CE Dr Selected/Execute Request Lamp

This lamp turns on when the Execute switch is operated. It resets when the operation requested by the Data Entry switches is complete and the Program Control display is set. The lamp also turns on while a drive in CE Mode is being selected and the Select Hold line is active.

Execute Switch

Operating the Execute switch:

- Turns on the Execute Request lamp and activates the CE Alert Execute line to the storage control.
- Causes the control program to read the Data Entry switches.
- Resets the Party Check Indicator latches.

Interface Select Switch

The Interface Select switch selects control interface A or B for CE Panel operation (string switch feature).

Power Mode Switch

A C2 Module has no Power Mode switch.

The two positions of the Power Mode switch are:

- The Remote position, which places the power sequencing under system control.
- The Local position, which removes the 3350 string from the normal system power sequence. The 3350 string can then be powered off without affecting the system operation. The system power-on sequence cannot power on the 3350 string while the switch is in the Local position.

PARITY CHECK

CTL-I Bus Out Lamp

The CTL-I Bus Out lamp is turned on by a Control Bus Out Parity error. It is reset by the Execute switch or by a power-on/off sequence.

DEV-I Bus In Lamp

The DEV-I Bus In lamp is turned on by a Device Bus In Parity error. It is reset by the Execute switch or by a power-on/off sequence.

CTL-I Tag Bus Lamp

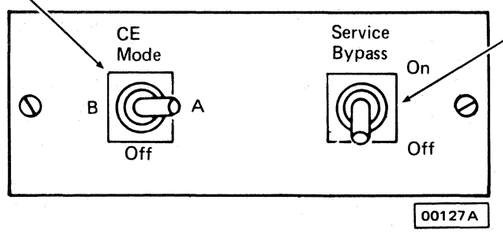
The CTL-I Tag Bus lamp is turned on by a Control Interface Tag Bus Parity error. It is reset by the Execute switch or by a power-on/off sequence.

CE POWER AND MODE CONTROLS

The CE Power and Mode controls are in the A2, B2, and C2 Modules.

CE Mode Switch

The CE Mode switch places either Drive A or B in CE Mode so it can be selected when a Select Tag accompanied by the Service Select bit on Bus Out is present. Neither drive is in CE Mode when the CE Mode switch is in the Off (center) position.



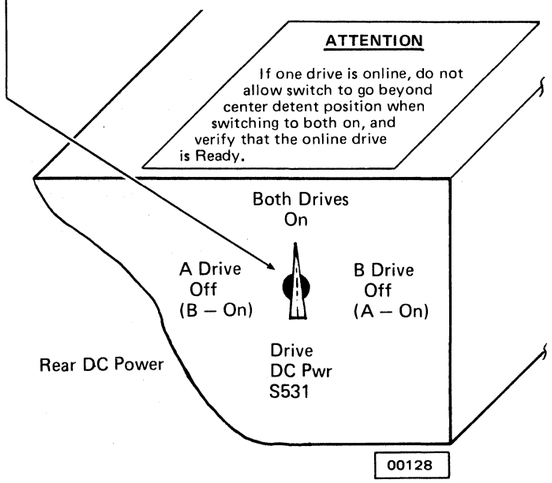
AC Power Switch (Service Bypass Switch)

The Service Bypass switch removes the module from the string power-on sequence. It also removes dc power from both drives in either A2, B2, or C2 Modules, as well as ac power from certain power supplies and other components.

Note: *On the A2 and C2 Modules, the Service Bypass switch does not remove the ac and dc power from the controller logic power supplies.*

Drive DC Power Switch

The Drive DC Power switch removes dc power from either Drive A or B for servicing.



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Note 1: *If the A2G2 card is replaced or swapped, the address jumpers must be checked. See INST 6.*

Note 2: *When there is more than one controller on the interface (but without the C2 Module installed), the following conditions exist:*

- *The controller Execute Request lamp is on continuously with the higher address after having operated the Execute Request switch.*
- *No apparent Execute Request lamp is on the controller with the lower address when the Execute Request switch is operated.*

Replace cards in the controller with the lower address:

Basic – A2G2
Interface A – A2D2 } *SWFE*
Interface B – A2E2 }

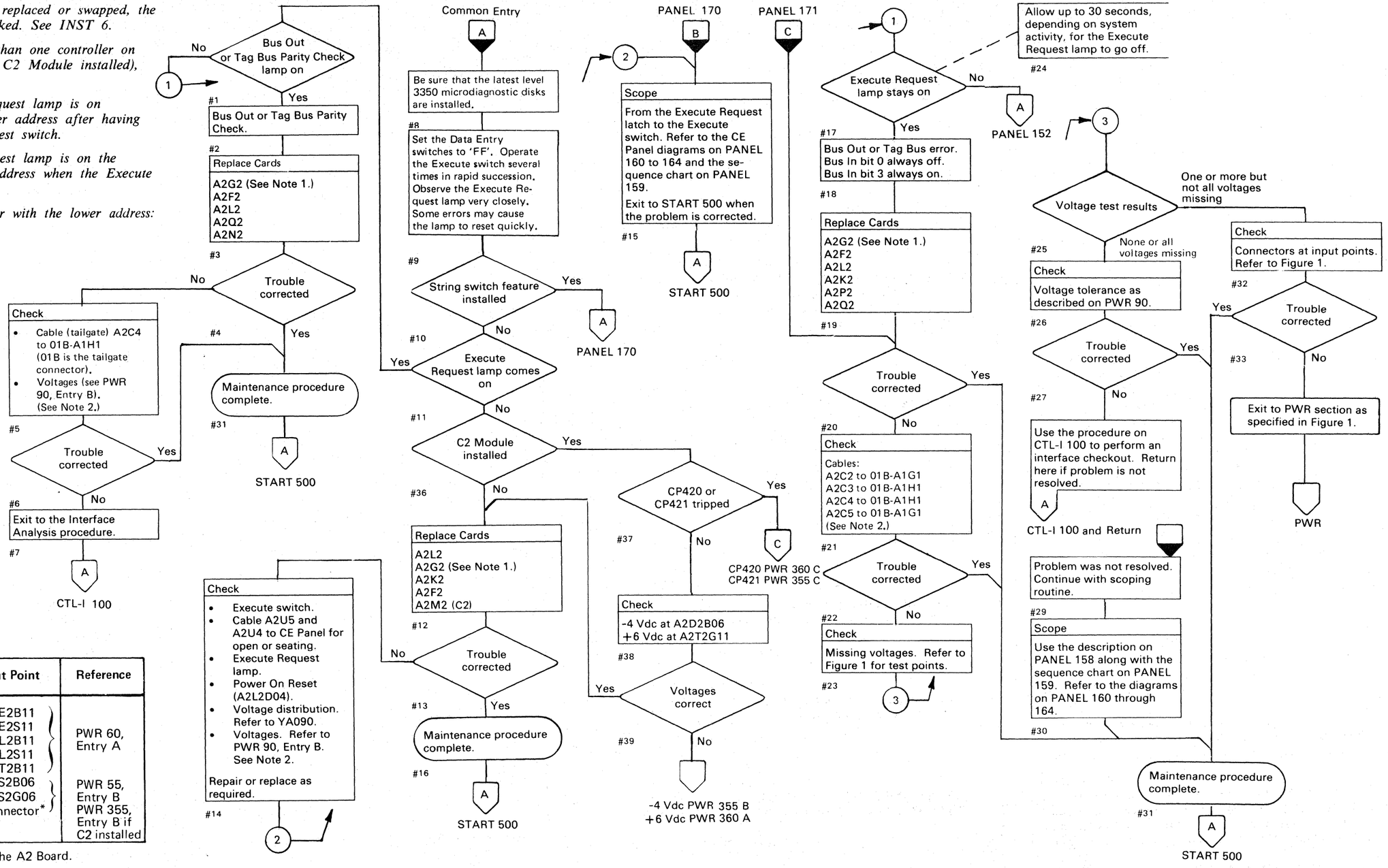

Figure 1. Voltage Locations

Voltage	Test Point	Input Point	Reference
+6	A2F2B11	A2E2B11	PWR 60, Entry A
+6	A2D2S11	A2E2S11	
+6	A2K2B11	A2L2B11	
+6	A2M2S11	A2L2S11	
+6	A2T2G11	A2T2B11	
–4	A2T2B06	A2S2B06	PWR 55, Entry B PWR 355, Entry B if C2 installed
–4	A2T2G06	A2S2G06	
–4	A2D2B06	Connector*	

* Planar connector at the top of the A2 Board.

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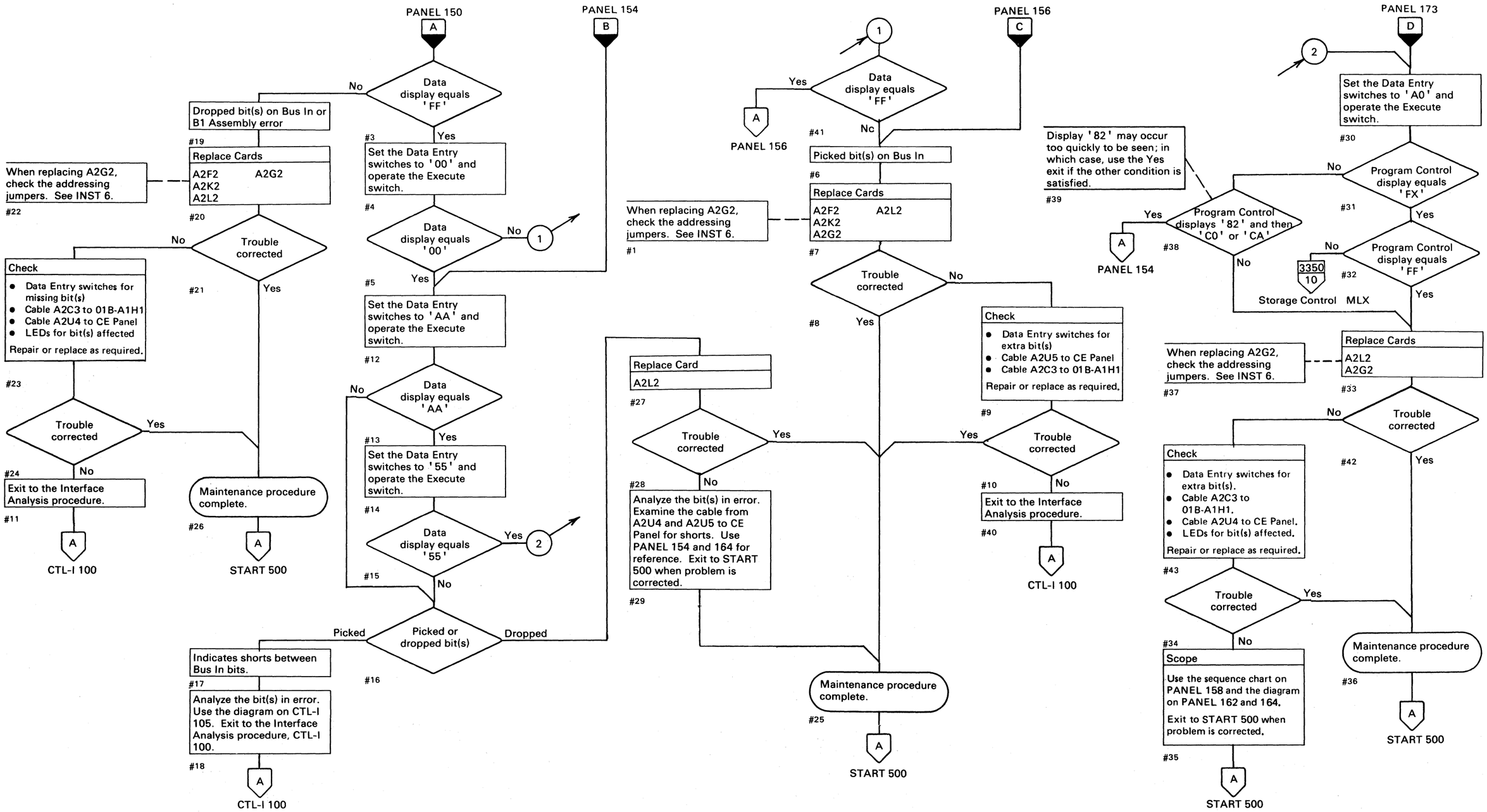

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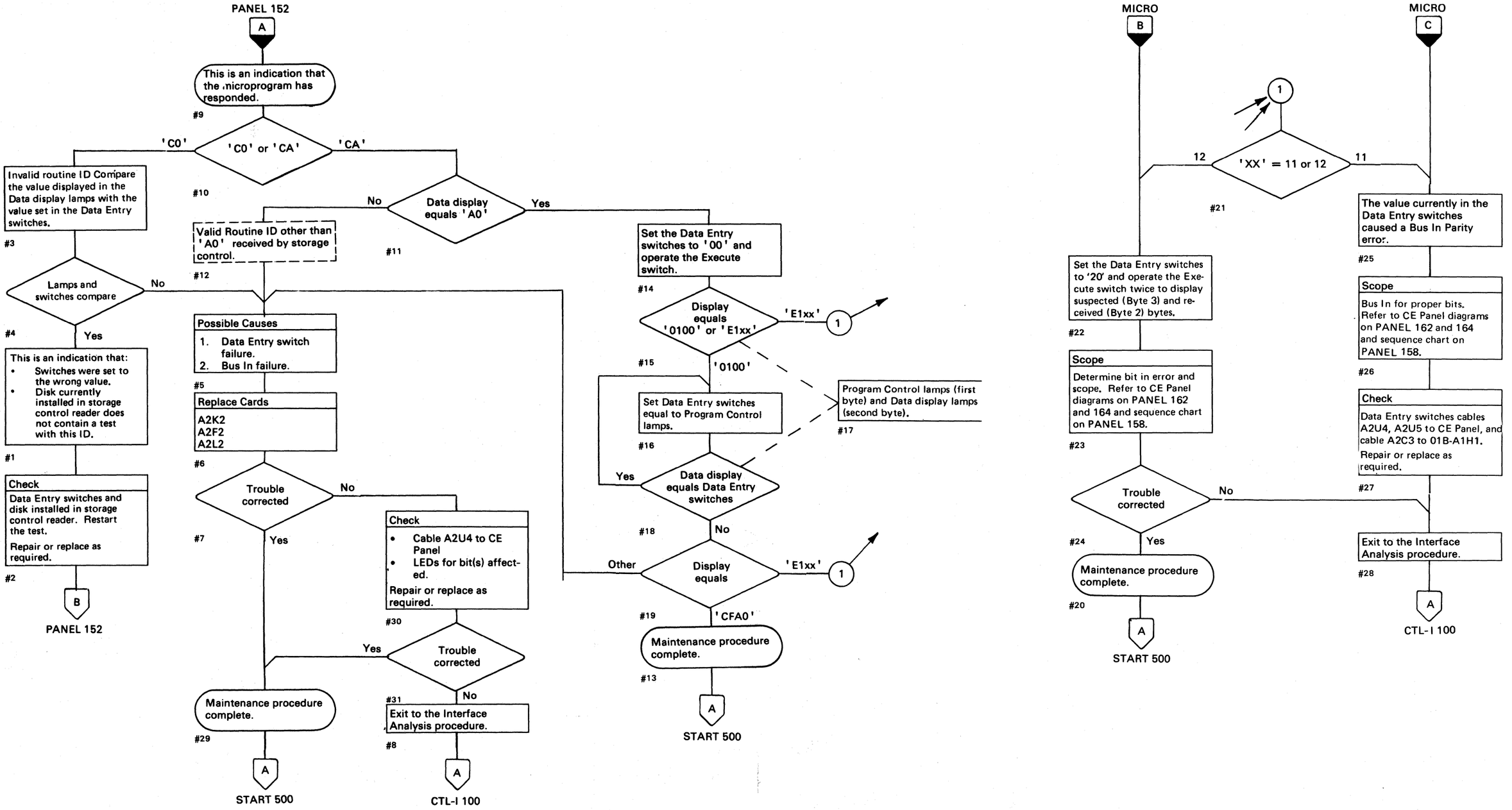

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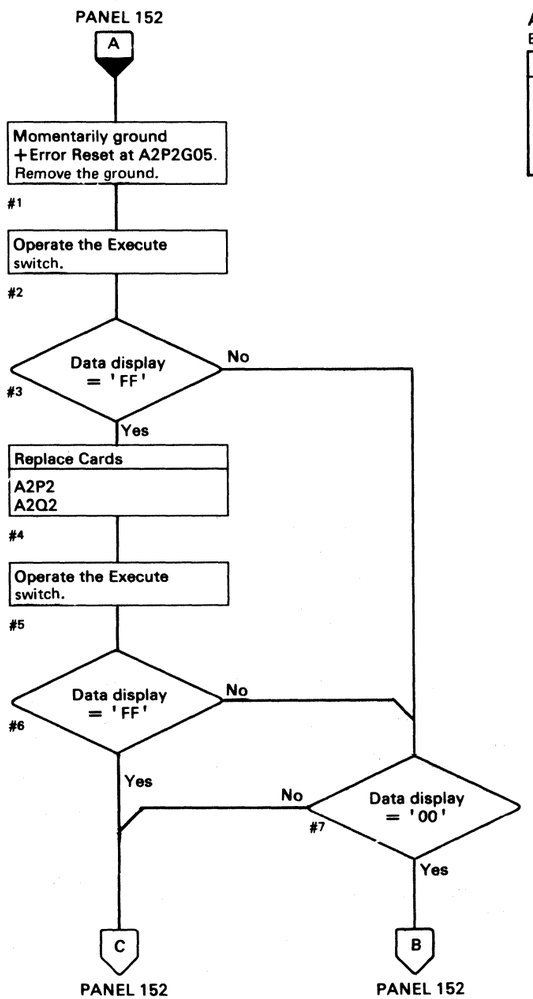
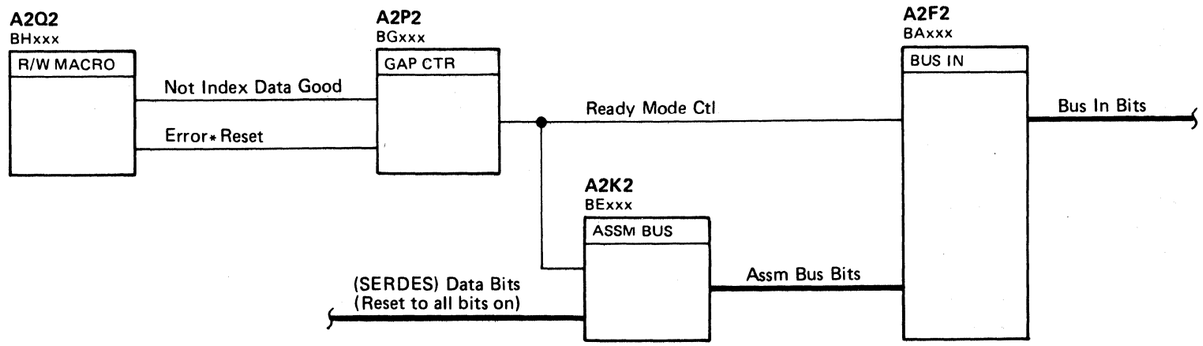
CE PANEL CHECKOUT

Read Mode Ctl causes the (SERDES) Data Bits, which are reset to all bits on, to be gated to the Bus In. When this happens, hex FF is on Bus In for all operations. The Not Index Data Good line can cause the Read Mode Ctl latch to set erroneously. The latch may be reset by grounding the Error*Reset line (ALD BG150).





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CE PANEL DATA TRANSFER

POLL CONTROLLER

See PANEL 160 through 164 for CE Panel operation diagrams and Figure 1 for inactive lines that affect CE Panel operations.

The Execute switch sets the CE Alert Latch (Y) if the controller is not selected (Select Hold (C) and Selected (K) inactive). The CE Alert Latch activates CE Alert Execute NPL (Z). The storage control responds to CE Alert Execute NPL with a Controller Poll operation (Tag '02', Bus '08'). The controller responds on Bus In with its bit significant address. (Bit 0 for Controller 0 or bit 1 for Controller 1). If the C2 Module is installed, bit 4 indicates the offline controller.

SELECT CONTROLLER

The storage control then selects the controller using an address based on the response from the Controller Poll operation. To select Controller 0, Bus Out equals '00' and to select Controller 1, Bus Out equals '20'. To select the offline controller if the C2 Module is installed, Bus Out should equal 1xx00000 (xx = Controller address).

The controller responds to selection by placing a 3-of-6 code (prewired 3-bit address on bits 0 through 2 and the inverted prewired address on bits 5 through 7) on Bus In to the storage control. The value of Bus In equals '07' for Controller 0 and '26' for Controller 1. See OPER 110 for description of the Select operation. If the C2 Module is installed, bit 0 is on for the offline controller and bit 4 is on for the alternate controller.

SET LONG CONNECTION

If the offline controller needs servicing, the online controller is selected first to Set Long Connection.

The storage control then sends Tag '07', Bus 'C0' to the controller to Set Long Connection if there is a String Switch feature or C2 Module installed. Tag '07' is a no-op to a machine without String Switch.

CE DATA TO STORAGE CONTROL

The storage control brings up Tag '0A' Bus '40' to the controller. Tag '0A' Bus '40' is decoded in the controller to activate Gate CE Data. Gate CE Data resets the CE Alert Latch (Y) and activates Assm Sel X (1) and Assm Sel Y (2). The bit value of the Data Entry switches is set into the Assembly register. Selected (K) brings up Gate BI. Gate BI places the CE data bits on the Bus In to the storage control.

SENSE DEVICE TYPE

Tag '0A', Bus '80' is then issued by the storage control to determine the proper device type so that the correct responses can be issued.

DATA DISPLAY

The storage control brings up Tag '0C', then Tag '0D'. Tag '0C' gates the Bus Out (CE Hi byte) to the Program Control lights on the CE Panel. Tag '0D' gates the Bus Out (CE Lo byte) to the Data Display lights on the CE Panel.

RESET

General Reset, Tag '09', Bus '80' resets errors that may be set.

UNLOCK SWITCH

If the String Switch feature is installed the Unlock Switch command (Tag '07' Bus '04) will reset the Select latch or the Partial Select latch for the active interface resulting in a reset to the Set Long Connection latch. Tag '07' is a no-op to a machine without String Switch.

Figure 1. Inactive lines affecting CE Panel operation. See PANEL 159 and 160.

Chart Line No.	Line Name	ALD	Test Point	
1	–Invert Tag Bus Bit P	BD170	A2L2 J07	(5)
2	+Power On Reset	BD180	A2L2 D04/B08	(X)
3	–Read Status 84	BF110	A2G2 D09	(N)
4	–BO Par Chk Latched	BF110	A2G2 J10	(R)
5	–Read Mode Ctl	BG150	A2P2 D03	(11)
6	–Not Index Data Good	BG150	A2P2 M07	(10)

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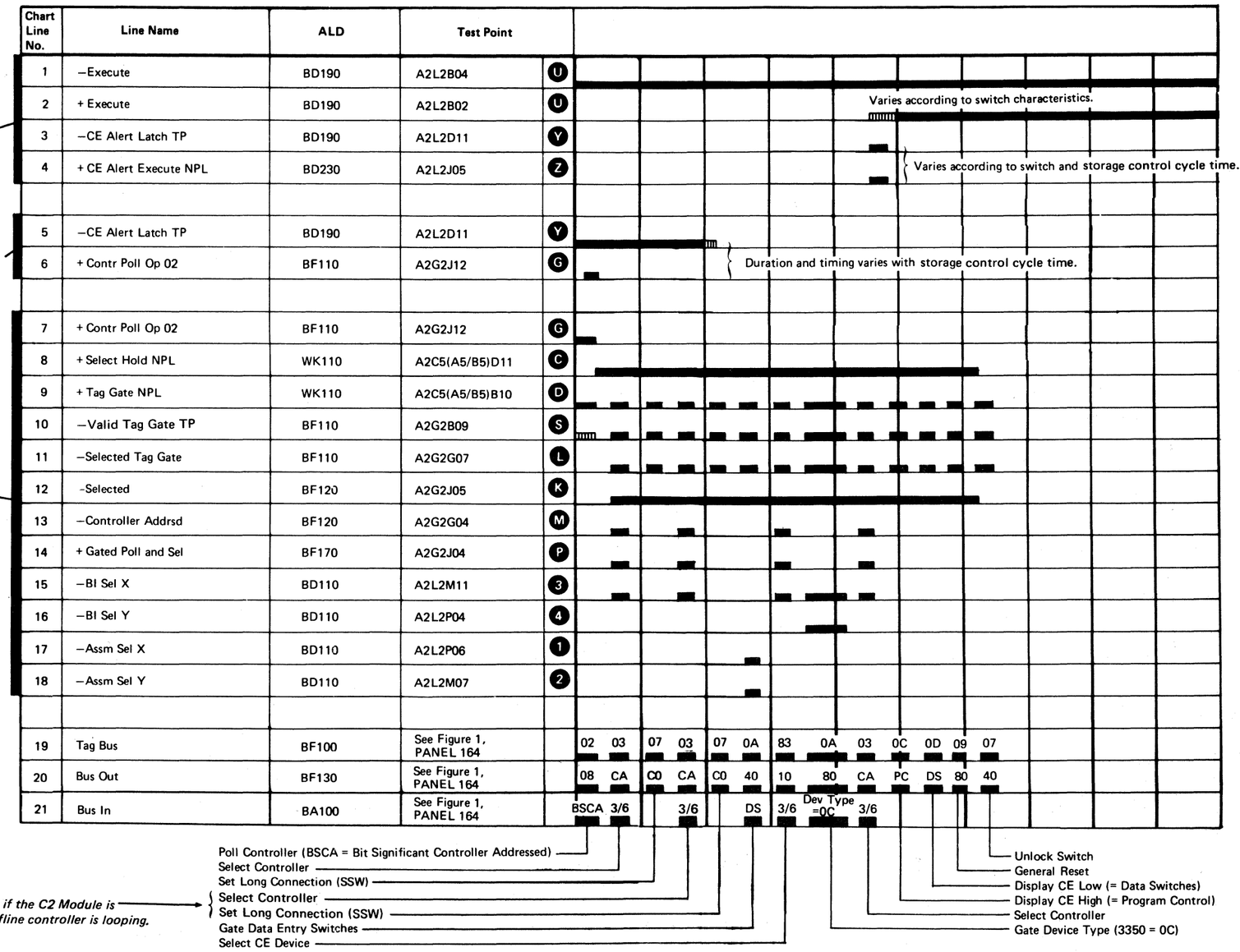
CE PANEL DATA TRANSFER

Sweep 0.2 ms/div
Trigger Int-Ch 1
Slope
Ch 1 A2L2B04
−Execute
volts/div 0.2
probe X10
Ch 2 A2L2B02
+Execute
volts/div 0.2
probe X10

Sweep 50 µs/div
Trigger Int-Ch 1
Slope (−)
Ch 1 A2L2D11
−CE Alert Latch TP
volts/div 0.1
probe X10

Sweep 20 µs/div
Trigger Int-Ch 1
Slope (+)
Ch 1 A2G2J12
+Contr Poll Op 02
Ch 2 See Sequence Chart.

Chart Line No.	Line Name	ALD	Test Point	
1	−Execute	BD190	A2L2B04	U
2	+ Execute	BD190	A2L2B02	U
3	−CE Alert Latch TP	BD190	A2L2D11	Y
4	+ CE Alert Execute NPL	BD230	A2L2J05	Z
5	−CE Alert Latch TP	BD190	A2L2D11	Y
6	+ Contr Poll Op 02	BF110	A2G2J12	G
7	+ Contr Poll Op 02	BF110	A2G2J12	G
8	+ Select Hold NPL	WK110	A2C5(A5/B5)D11	C
9	+ Tag Gate NPL	WK110	A2C5(A5/B5)B10	D
10	−Valid Tag Gate TP	BF110	A2G2B09	S
11	−Selected Tag Gate	BF110	A2G2G07	L
12	-Selected	BF120	A2G2J05	K
13	−Controller Addrsd	BF120	A2G2G04	M
14	+ Gated Poll and Sel	BF170	A2G2J04	P
15	−BI Sel X	BD110	A2L2M11	3
16	−BI Sel Y	BD110	A2L2P04	4
17	−Assm Sel X	BD110	A2L2P06	1
18	−Assm Sel Y	BD110	A2L2M07	2
19	Tag Bus	BF100	See Figure 1, PANEL 164	
20	Bus Out	BF130	See Figure 1, PANEL 164	
21	Bus In	BA100	See Figure 1, PANEL 164	



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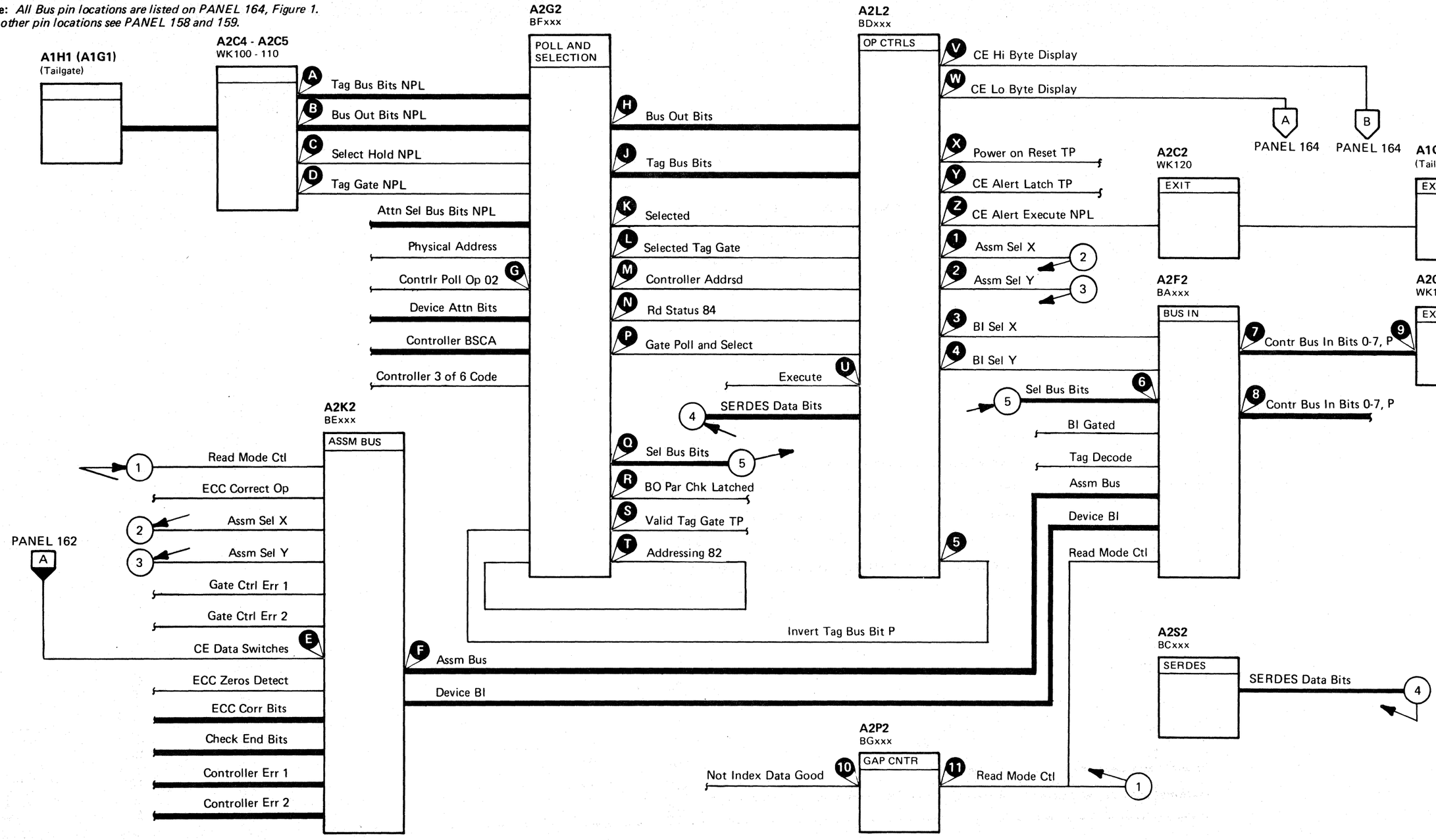
Note: *All Bus pin locations are listed on PANEL 164, Figure 1. For other pin locations see PANEL 158 and 159.*



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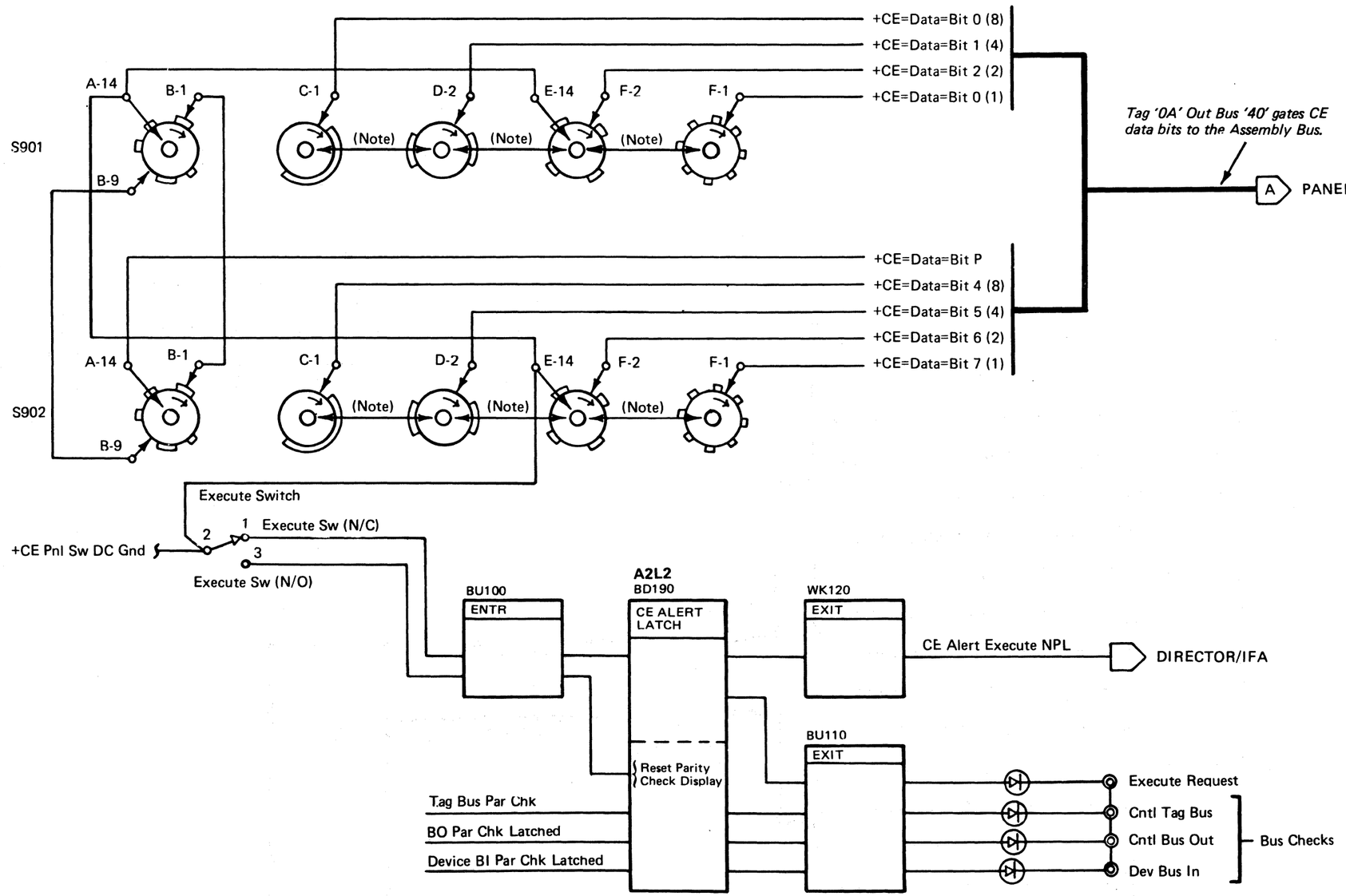
CE PANEL DATA ENTRY

See PANEL 158 for CE Panel operation description and sequence chart.

Note: *Lines indicated are internal to switch.*

DATA ENTRY SWITCHES



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CE PANEL DATA DISPLAY

See PANEL 158 for CE Panel operation description and sequence chart.

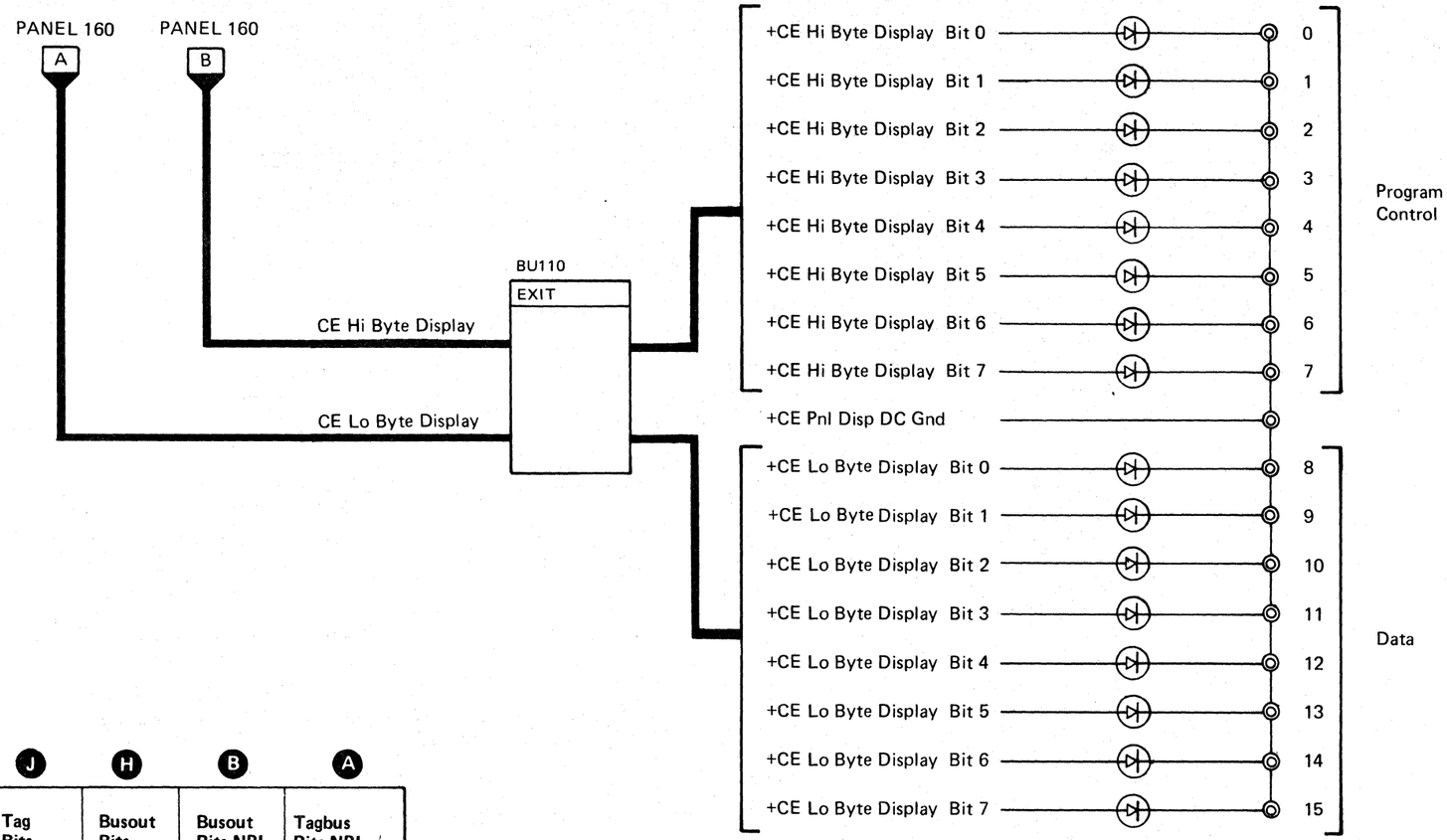

Figure 1. Pin Location Chart Keyed To PANEL 160 Diagram.

	E	F	8	7	6	V	W	J	H	B	A
	CE Data Switches	Assm Bus	Contr Bus In	Contr Bus In	Sel Bus	CE Hi Byte Display	CE Lo Byte Display	Tag Bits	Busout Bits	Busout Bits NPL	Tagbus Bits NPL
Card Loc	A2K2 (BE100)	A2K2 (BE110)	A2F2 (BA100)	A2F2 (BA150)	A2F2 (BA190)	A2L2 (BD200)	A2L2 (BD210)	A2G2 (BF100)	A2G2 (BF130)	A2C4 (WK100)	A2C5 (WK110)
Bit 0	G10	M07	P05	D06	B02	U11	U04	J03	P02	D05	B04
Bit 1	J10	M09	M10	B03	D04	B05	U05	–	J13	B05	–
Bit 2	U10	S11	M08	D10 plus	B04	U02	M12	–	M02	D06	–
Bit 3	S12	S13	S07	D09 NPL	B05	P12	U06	–	P05	B08/B09	–
Bit 4	G13	M02	P06	J02 at	D11	S13	S09	J02	P04	D09/D10	B05
Bit 5	J13	M04	U03	J07 inter-	B12	U12	U09	B02	P06	B10	D05
Bit 6	P10	M11	P09	J11 face	J06	U13	S10	D07	P11	D11	B08/B09
Bit 7	P11	M13	U06	J03	G08	S12	U10	B07	M10	B12	D06
Bit P	J11	G07	U04	J12	G04	–	–	D10	–	B02	D09/D10

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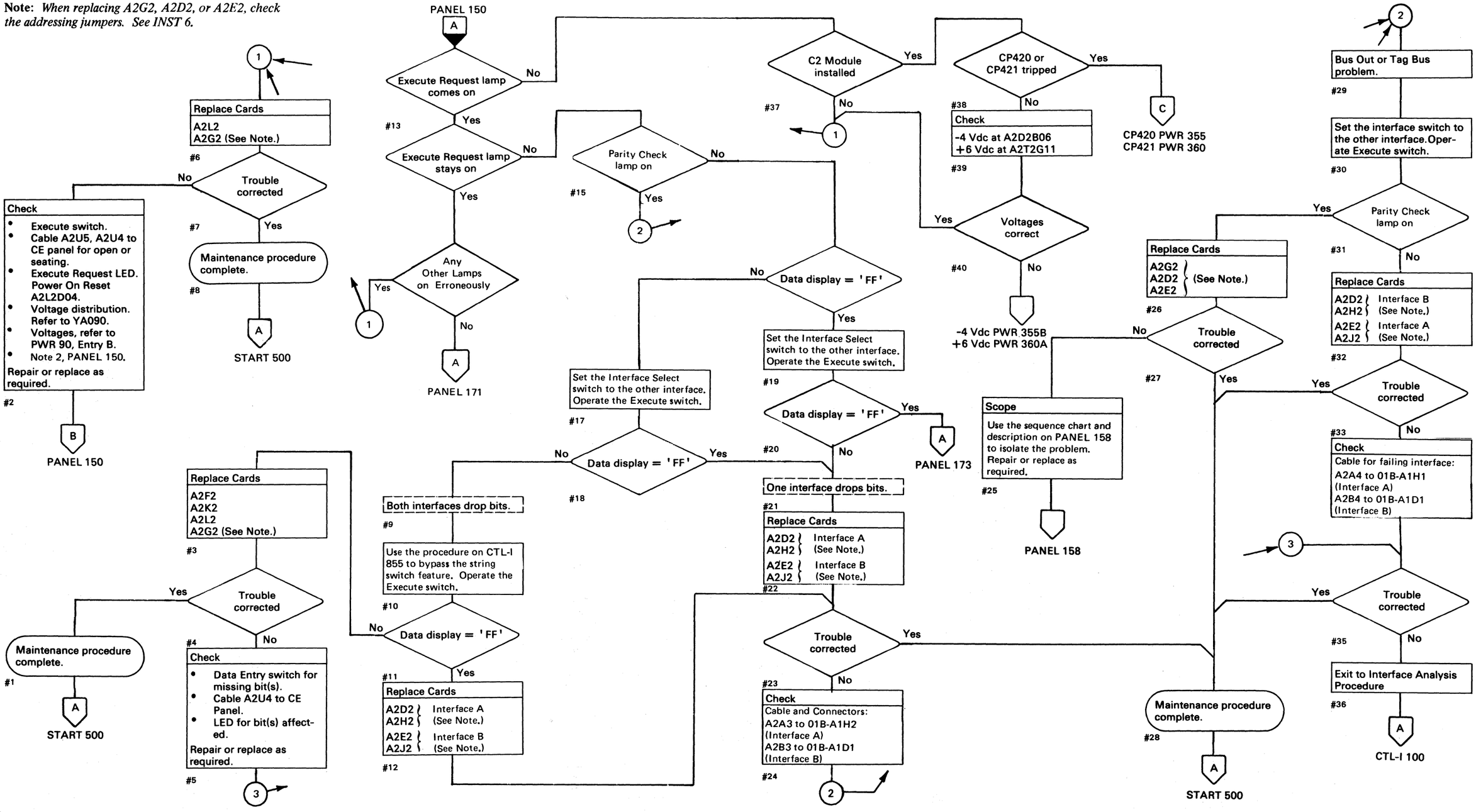
CE PANEL CHECKOUT (String Switch Feature)

Note: *When replacing A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.*



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PANEL 170

A

Use this MAP only when the Execute Request lamp stays on.

Execute Request lamp stays on when trying to run any microdiagnostic.

Check
1. All drives are powered on.
2. CE Mode switch on required drive is on.
3. Proper 3350 microdiagnostic disks are inserted.
4. Interface Select switch is set to the proper interface (MICRO 10).
5. Required interface is enabled by using the Enable/Disable switches on the Power Panel (PANEL 10).

Visual checkout OK?

Yes

First time through this block?

No → 1

Yes

The 3350 string can be taken offline?

No → If the string becomes available and the trouble is not corrected, return here and take the Yes path.

Yes → Take the 3350 string offline. → 2

Possible Causes

On Interface A:
A2D2 (See Note.)
A2H2

On Interface B:
A2E2 (See Note.)
A2J2

Common Cards
A2M2
A2G2 (See Note.)
A2F2
A2L2
A2P2

Trouble corrected?

No → 1

Yes → Maintenance procedure complete. → A → START 500

No → Use the procedure on PANEL 150 to analyze any of the visual checks found to be in error. Return to Entry A on this page when problem is corrected. → A → PANEL 150

Note: *When replacing A2D2, A2E2, or A2G2, check the addressing jumpers. See INST 6.*

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3350 C2 Module installed?

No → The 3350 string must be taken offline before proceeding. → 2

Yes → Fault Symptom Code 1915?

Yes → A → DEV-I 410

No → Return to the page recorded on FSI 970. If entry to FSI 970 was from an FSI page, perform the steps listed in the Additional Action column on that page. → Common Exit

2

Microdiagnostic

Reset the storage controls on both interfaces to avoid error indications when running microdiagnostic routines.

If the storage control does not appear to be in its idle state, it may be necessary to stop the attached CPU(s) before resetting.

Execute Request lamp still on?

Yes → Microdiagnostics

Run the same microdiagnostic routines on the other interface using the following procedure:
1. Reset the storage controls on both interfaces to avoid error indications when running microdiagnostic routines on the other interface.
2. With the Execute Request lamp still on, set the Enable/Disable switch on the interface to be tested to the Disable position.
3. Set the Enable/Disable switch on the other interface to the Disable position.
4. Turn the Interface Select switch to the interface to be tested.
5. Operate the Execute switch if the Execute Request lamp has gone out.
6. Enable the interface to be tested and run microdiagnostic routines starting with routine A1.

→ 1

No → Use the procedure on PANEL 150 to check the Execute Request lamp circuit. Return to Entry A on this page when the problem is corrected. → A → PANEL 150

CTL-I 850

B

Lamp remains on?

No → Trouble is unique to one interface. → B → CTL-I 850

Yes → Same trouble indication on both interfaces.

Replace Card
A2M2

Trouble corrected?

Yes → Maintenance procedure complete. → A → START 500

No → Analysis

Use the procedure on CTL-I 100 to perform interface checkout. Check both interfaces A and B. Return if trouble is not corrected.

A → CTL-I 100 and Return

Continue analysis.

Where Dot ORing is used in the string switch, a grounded card I/O pin gives an error indication on both interfaces. For reference, see CTL-I 852.

→ 3

Figure 1. String Switch Cards

Location	Type	Interface
A2M2	X760	Both
A2D2	X758	A
A2E2	X758	B
A2H2	X759	A
A2J2	X759	B

3

Isolate the failure to either the basic controller or the string switch. Bypass the string switch by connecting either interface directly to the basic controller.

CTL-I 855 and Return

Try to run the same microdiagnostic routines on the connected interface. Be sure all string switch cards are removed.

Lamp remains on?

Yes → A → PANEL 172

No → Trouble is isolated to string switch cards.

With the string switch bypassed, replug cards one at a time, attempt to run the microdiagnostics after each, and observe the Execute Request lamp. Do this for each card listed in Figure 1.

Plugging any card causes lamp to stay on?

No → Re-install the original string switch cards. Return here if trouble persists.

CTL-I 855 and Return

Rerun the original interface and scope beginning at PANEL 158.

PANEL 158–164

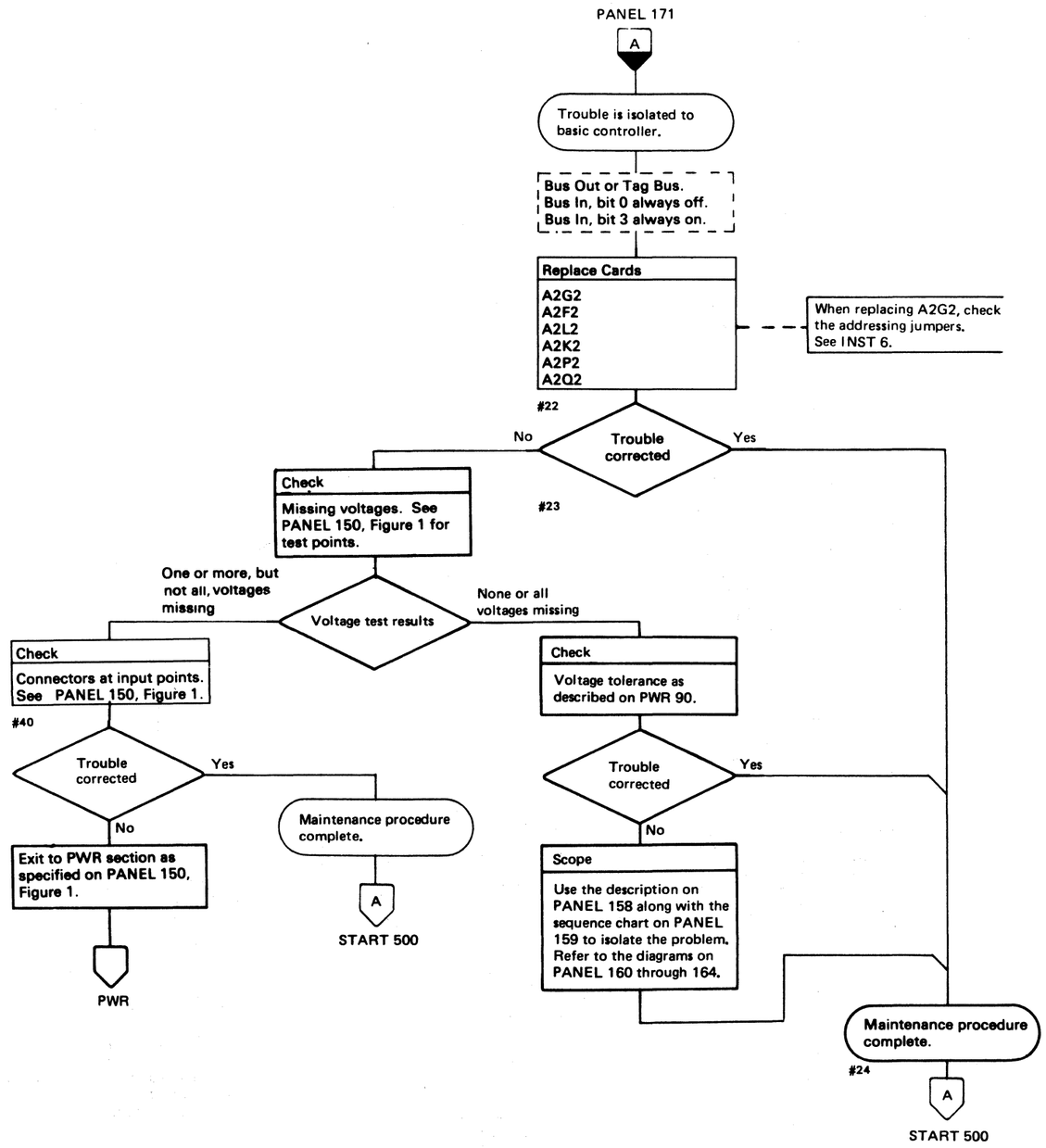
Yes → Re-install the string switch cards using good cards. Return here if trouble persists.

CTL-I 855 and Return

Rerun the original microdiagnostic over the first interface.

A → PANEL 150

CE PANEL CHECKOUT (String Switch Feature)



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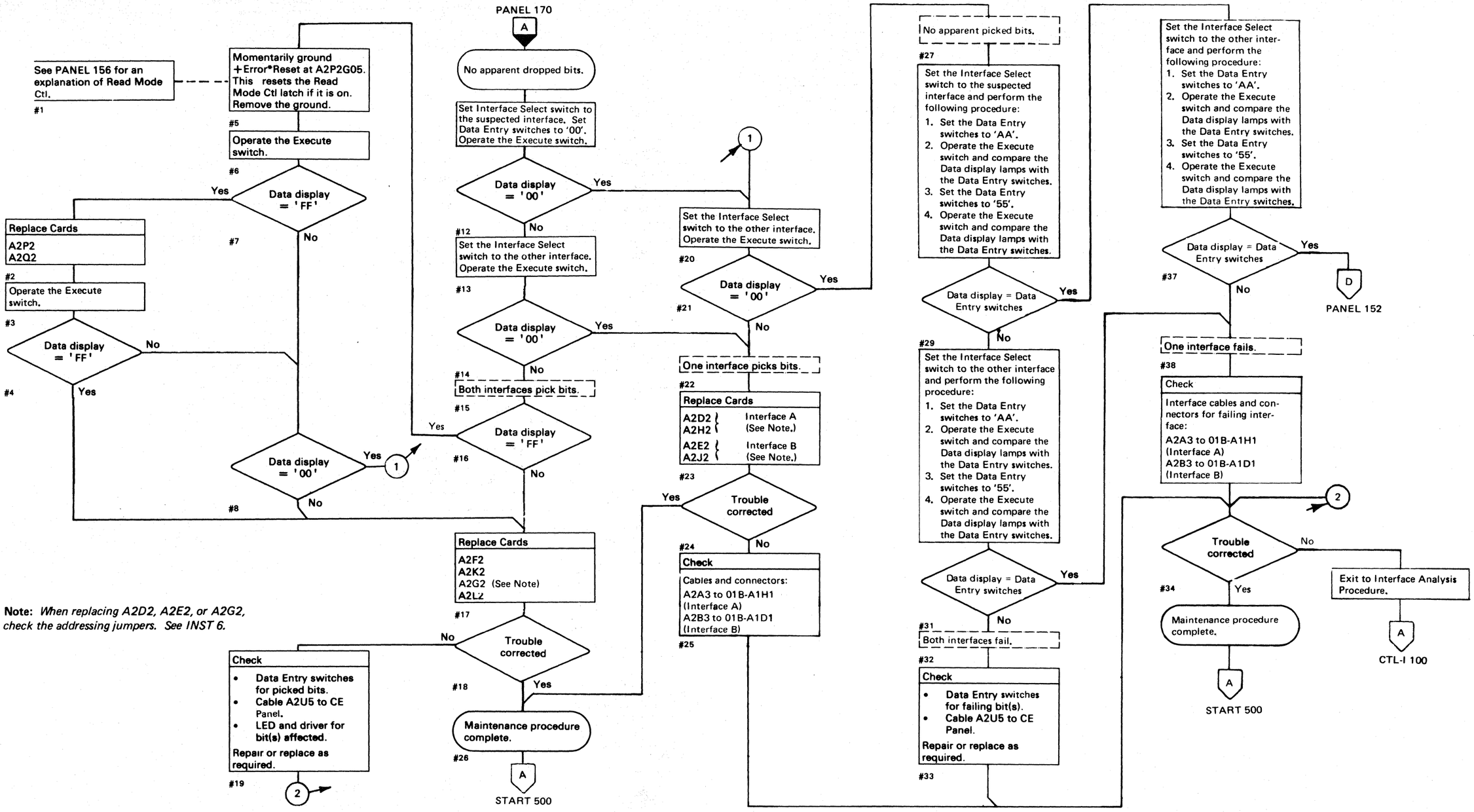

Note: *When replacing A2D2, A2E2, or A2G2, check the addressing jumpers. See INST 6.*

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3350 with String Switch . . . CTL-I 113 – 116

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Overview . . . . . CTL-I 852
Bypass Procedure . . . . . CTL-I 855

TROUBLE NOT FOUND . . . CTL-I 990

CABLE CHECKING HINTS . . CTL-I 993

REFERENCES TO OTHER SECTIONS
Controller Functional Units . . OPER 4 – 13
Control Interface Description . . . . . OPER 90, 91
Tag Summary . . . . . OPER 98 – 101
Controller Error Conditions . . OPER 240, 241
String Switch Feature . . . . OPER 261, 262
String Switch Checkout . . . START 120

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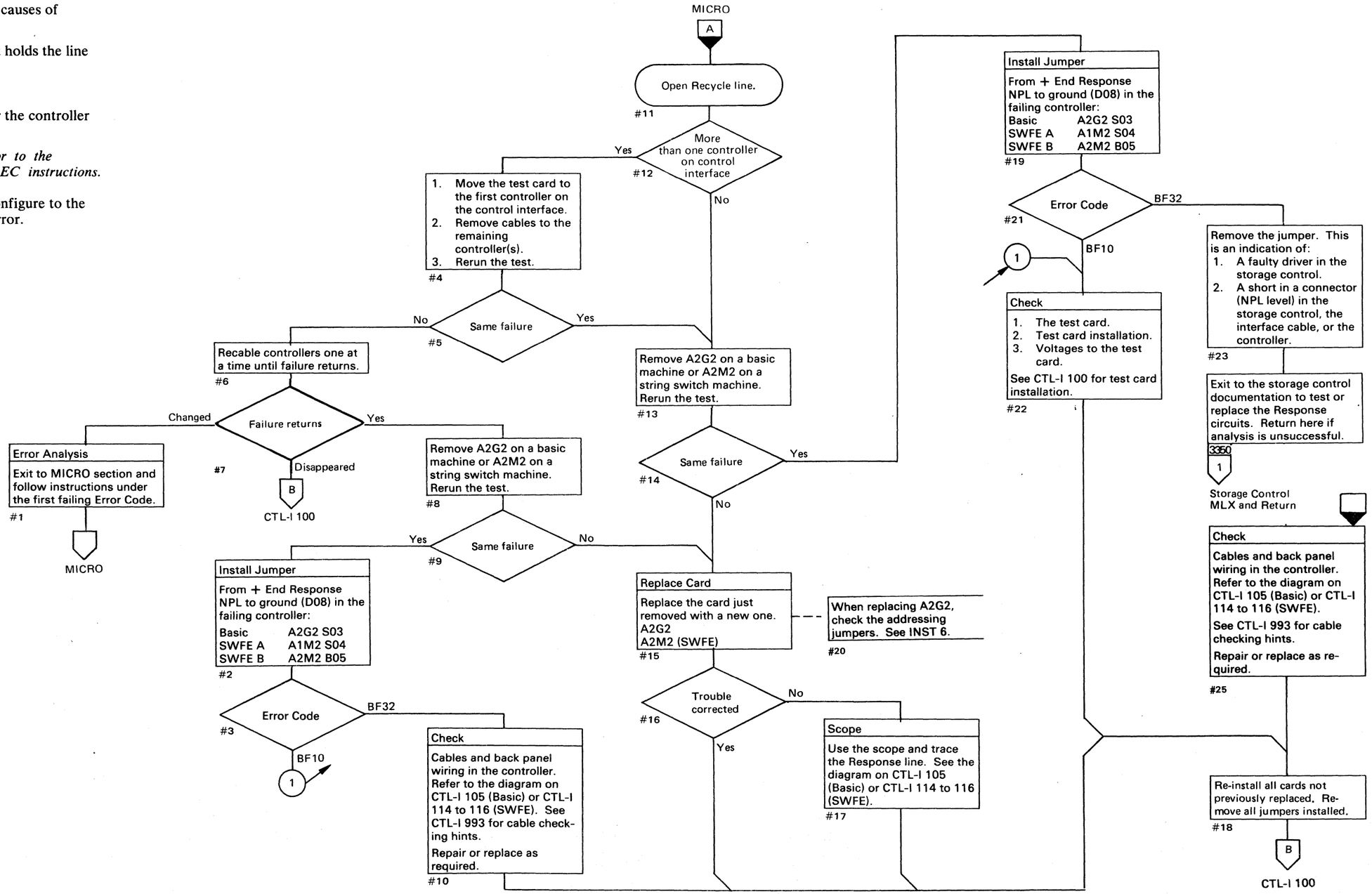
FAULTY END RESPONSE LINE

The End Response line is open. Possible causes of trouble are:

- A faulty receiver in the controller that holds the line at ground.
- A faulty driver in the storage control.
- Short to ground or signal line in either the controller or the storage control.

Note: *If an EC was installed just prior to the failure, recheck the EC work and the EC instructions.*

For strings with multiple controllers, reconfigure to the smallest configuration that sustains the error.



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INACTIVE INBOUND LINE

One or more, but not all, of the inbound signal lines are inactive at a time when they should be active. Possible causes of trouble are:

- An open circuit in the specified inbound line(s) in the interface cable.
- A short between the specified inbound signal line and a shield in the interface cable or a signal line shorted to ground.
- A faulty receiver in the storage control.
- A faulty driver in the (A) controller holding the line at an inactive level.
- Opens or shorts to ground in other cables or on the back panel.

Note: *If an EC was installed just prior to the failure, check the EC instructions and verify the changes made.*

For strings with multiple controllers, reconfigure to the smallest configuration that sustains the error.

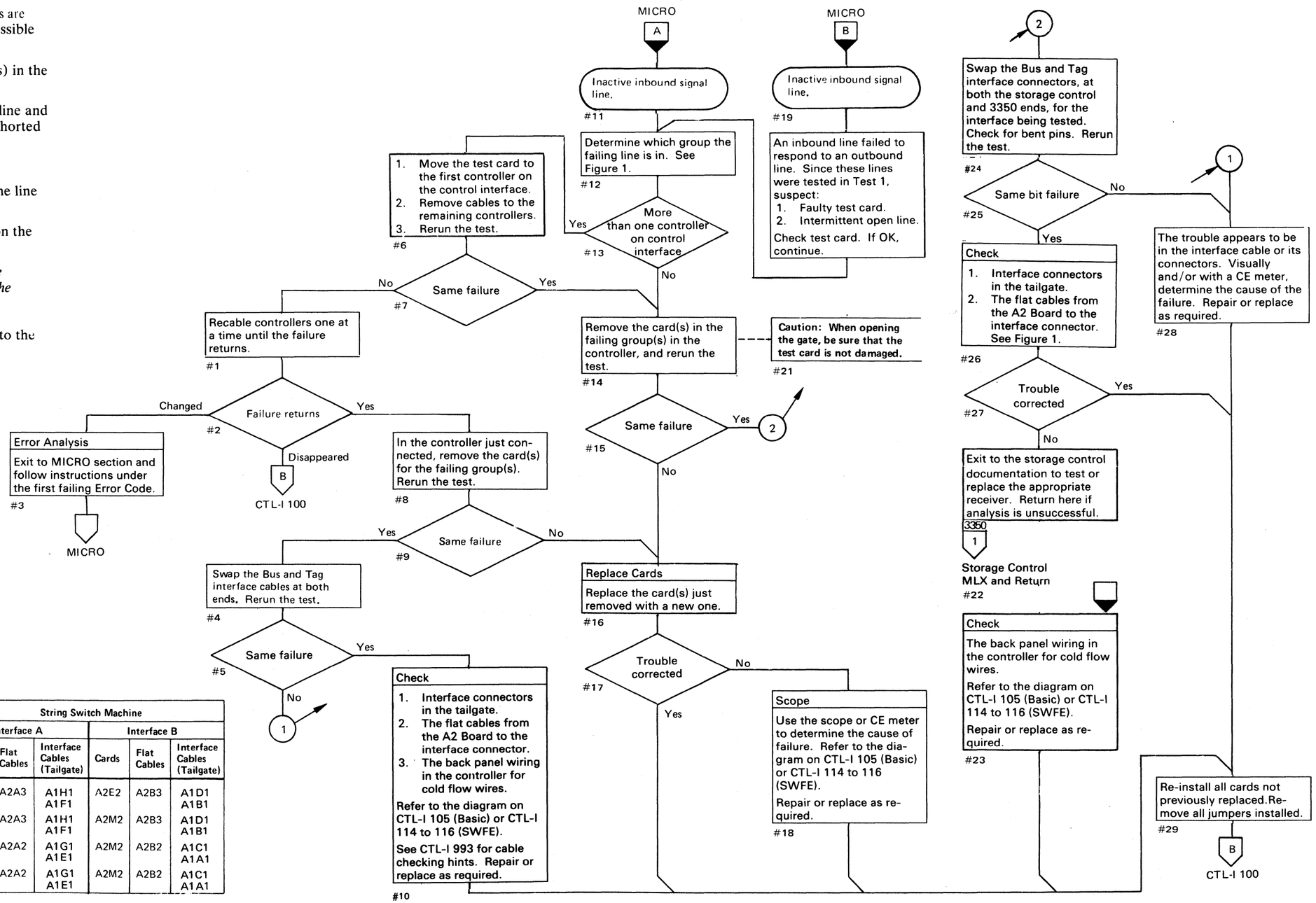

Figure 1. Inbound Signal Lines

Group	Line Name	Basic Machine			String Switch Machine					
					Interface A			Interface B		
		Cards	Flat Cables	Interface Cables (Tailgate)	Cards	Flat Cables	Interface Cables (Tailgate)	Cards	Flat Cables	Interface Cables (Tailgate)
Group 1	Bus In Bits	A2F2	A2C3	A1H1 A1F1	A2D2	A2A3	A1H1 A1F1	A2E2	A2B3	A1D1 A1B1
Group 2	Sync In	A2F2 A2K2	A2C3	A1H1 A1F1	A2M2	A2A3	A1H1 A1F1	A2M2	A2B3	A1D1 A1B1
Group 3	Error Alert CE Alert	A2F2 A2L2	A2C2	A1G1 A1E1	A2M2	A2A2	A1G1 A1E1	A2M2	A2B2	A1C1 A1A1
Group 4	All Others	A2F2 A2K2	A2C2	A1G1 A1E1	A2M2	A2A2	A1G1 A1E1	A2M2	A2B2	A1C1 A1A1

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FAULTY OUTBOUND LINE

One or more outbound signal lines are active at a time when they should be inactive. Possible causes of the trouble are:

- A faulty driver in the storage control.
- A faulty receiver in the controller holding the line at an active level.
- A short to a voltage or signal line in either the controller or storage control.

Note: *If an EC was installed just prior to the failure, check the EC instructions and verify the changes made.*

For strings with multiple controllers, reconfigure to the smallest configuration that sustains the error.

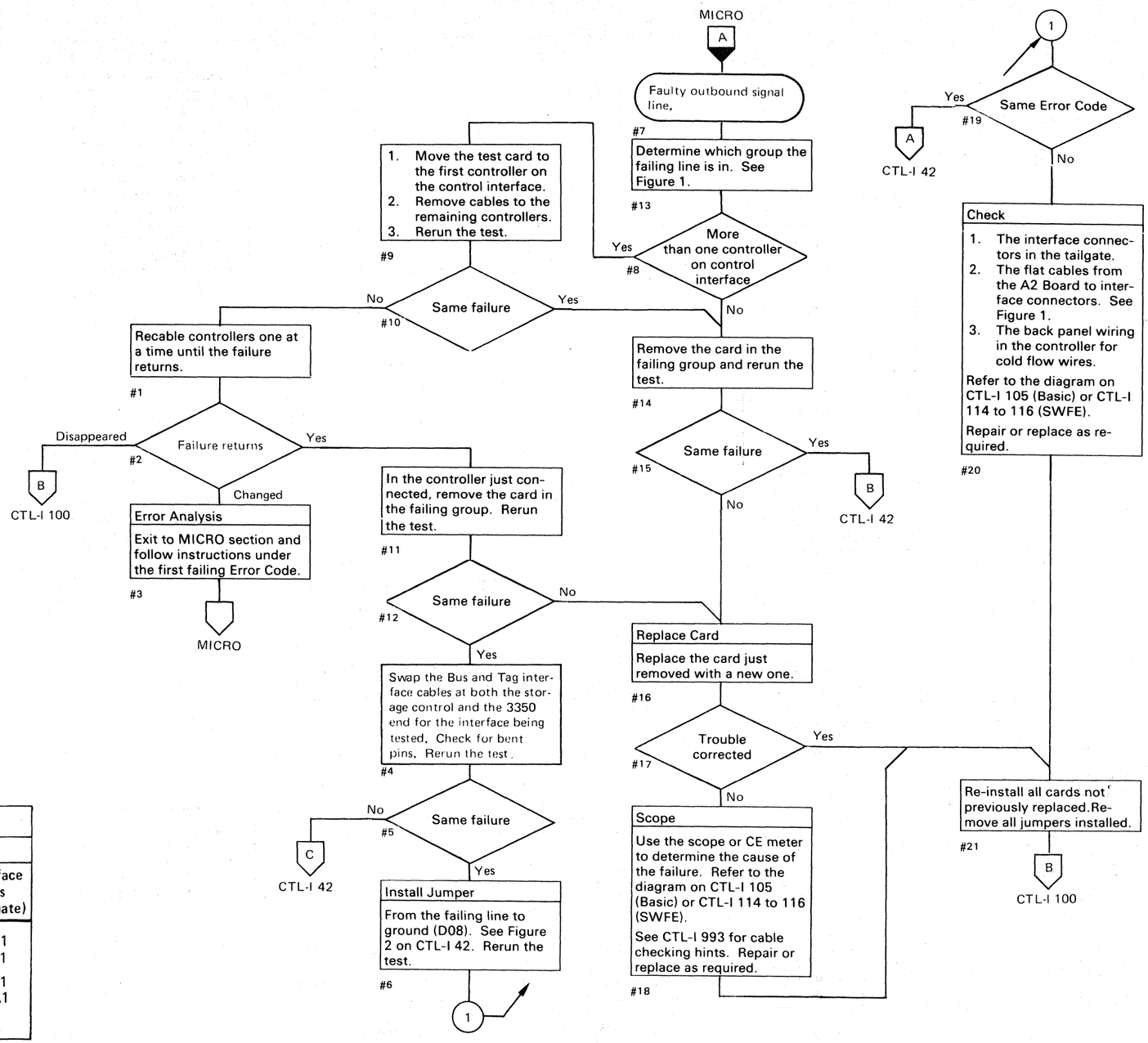

Figure 1. Outbound Signal Lines

Group	Line Name	Basic Machine			String Switch Machine					
					Interface A			Interface B		
		Cards	Flat Cables	Interface Cables (Tailgate)	Cards	Flat Cables	Interface Cables (Tailgate)	Cards	Flat Cables	Interface Cables (Tailgate)
Group 1	Bus Out Bits 0–7, P	A2G2	A2C4	A1H1 A1F1	A2D2	A2A4	A1H1 A1F1	A2E2	A2B4	A1D1 A1B1
Group 2	Tag Bus Bits 0, 4–7, P Select Hold Tag Gate	A2G2	A2C5	A1G1 A1E1	A2D2	A2A5	A1G1 A1E1	A2E2	A2B5	A1C1 A1A1

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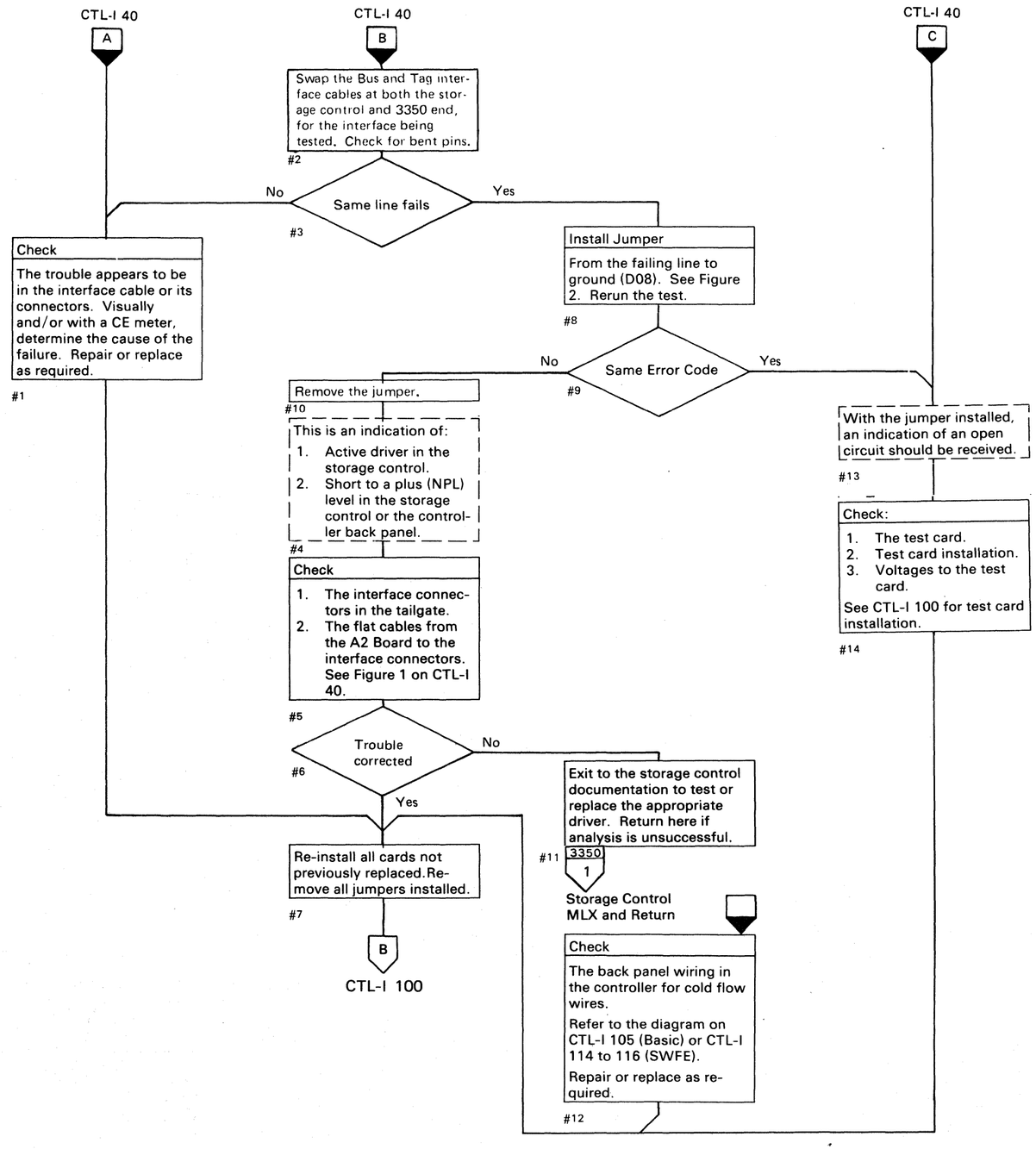
FAULTY OUTBOUND LINE

Figure 2. Jumper Chart

Outbound Lines		Basic Machine	String Switch Machine	
			Interface A	Interface B
		A2 Board	A2 Board	A2 Board
Bus Out Bit	0	G2G12(BF130)	D2G11(BM100)	E2G11(BN100)
	1	G2G13(BF130)	D2J11(BM100)	E2J11(BN100)
	2	G2P03(BF130)	D2J05(BM100)	E2J05(BN100)
	3	G2M03(BF130)	D2J04(BM100)	E2J04(BN100)
	4	G2M04(BF130)	D2J03(BM100)	E2J03(BN100)
	5	G2M07(BF130)	D2D07(BM100)	E2D07(BN100)
	6	G2M09(BF130)	D2G03(BM100)	E2G03(BN100)
	7	G2P10(BF130)	D2G04(BM100)	E2G04(BN100)
	P	G2P09(BF130)	D2G05(BM100)	E2G05(BN100
Sync Out		G2B13(BF100)	M2S03(BR130)	M2D03(BR130)
Tag Bus Bit	0	G2D13(BF100)	D2B07(BM100)	E2B07(BN100)
	4	G2G02(BF100)	D2G12(BM100)	E2G12(BN100)
	5	G2B03(BF100)	D2D09(BM100)	E2D09(BN100)
	6	G2B05(BF100)	D2D10(BM100)	E2D10(BN100)
	7	G2D04(BF100)	D2B09(BM100)	E2B09(BN100)
	P	G2B04(BF100)	D2D11(BM100)	E2D11(BN100)
Tag Gate		G2J11(BF130)	D2D06(BM100)	E2D06(BN100)
Response		G2S03(BF160)	M2S04(BR130)	M2B05(BR130)
Select Hold		G2B12(BF100)	D2J12(BM100)	E2J12(BN100)
Recycle		G2U12(BF160)	M2U02(BR130)	M2B02(BR130)



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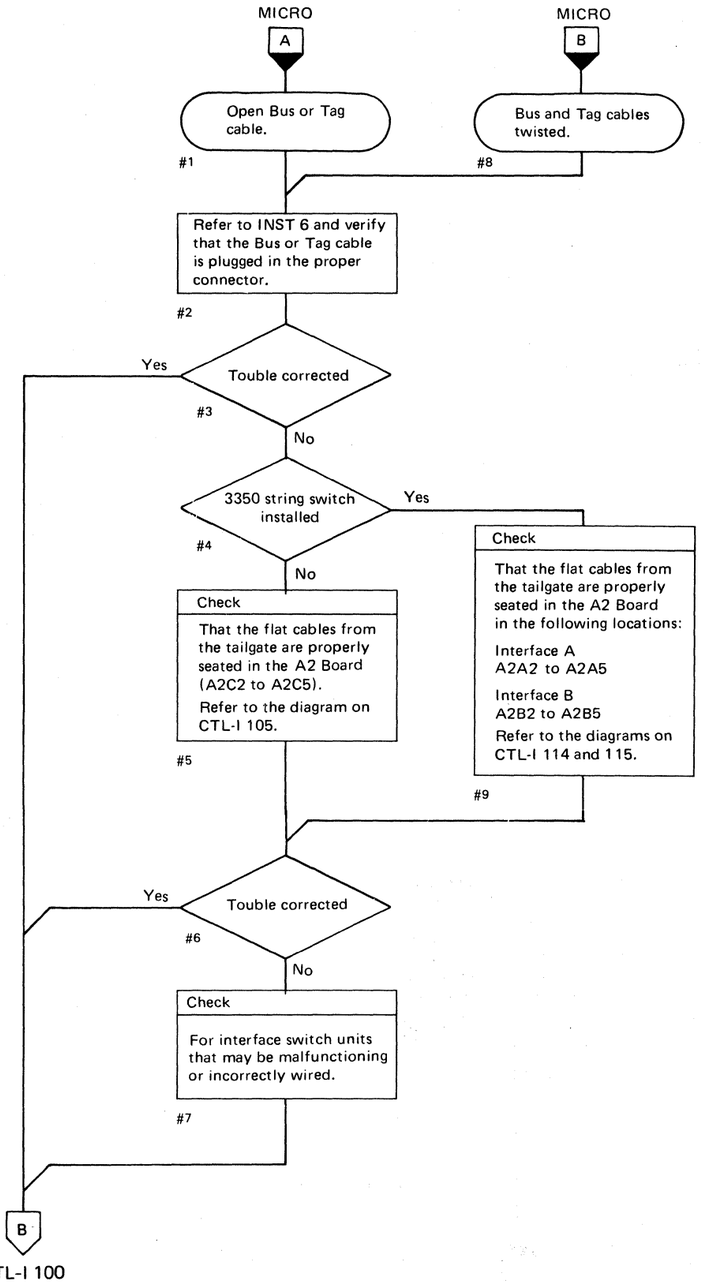
OPEN BUS OR TAG CABLE

Diagnostic tests indicate that all of the Bus cable lines or all of the Tag cable lines are open. Connecting the cable usually corrects the problem.

Bus and Tag Cables Twisted

Diagnostic tests indicate that the Bus and Tag cables are crossed. Swapping connectors at either end usually corrects the problem.

See CTL-I 993 for cable checking hints.



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OPEN OUTBOUND LINE

During this portion of the test a bit is placed on one of the Outbound lines. Proper operation activates a corresponding Inbound line. If the Outbound line is open, the test card activates all of the Inbound lines.

The program recognizes this condition. The bit indicated in the display is the open line. Possible causes of the trouble are:

- A line or connector pin open, shorted to ground, or shorted to the shield.
- A faulty driver in the storage control.
- A faulty receiver in the controller.
- A short to ground or a –level NPL in either the storage control or the controller.

Note: *If an EC was installed just prior to the failure, check the EC instructions and verify the changes made.*

For strings with multiple controllers, reconfigure to the smallest configuration that sustains the error.

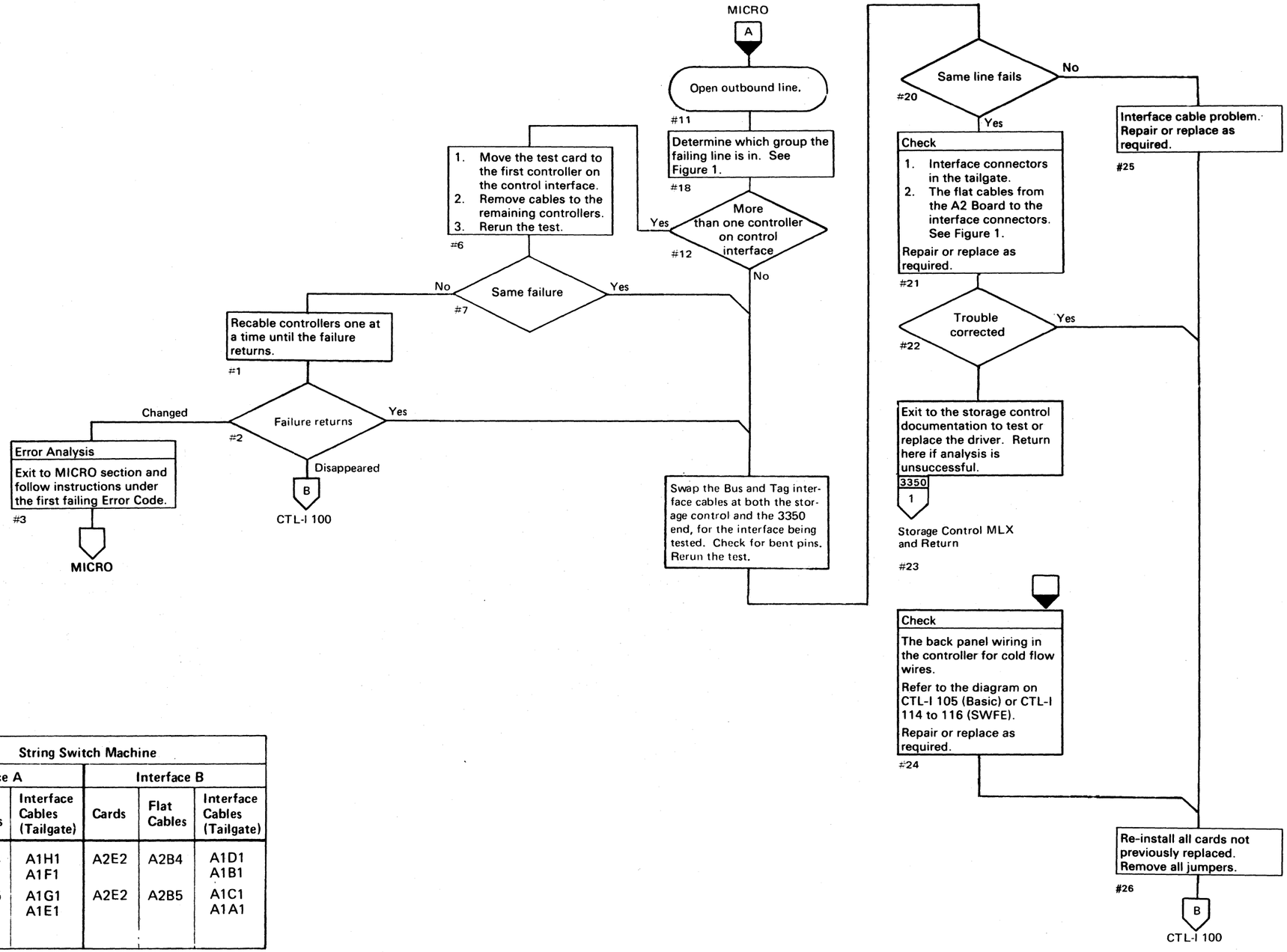

Figure 1. Outbound Signal Lines

Group	Line Name	Basic Machine			String Switch Machine					
					Interface A			Interface B		
		Cards	Flat Cables	Interface Cables (Tailgate)	Cards	Flat Cables	Interface Cables (Tailgate)	Cards	Flat Cables	Interface Cables (Tailgate)
Group 1	Bus Out Bits 0–7, P	A2G2	A2C4	A1H1 A1F1	A2D2	A2A4	A1H1 A1F1	A2E2	A2B4	A1D1 A1B1
Group 2	Tag Bus Bits 0, 4–7, P Select Hold Tag Gate	A2G2	A2C5	A1G1 A1E1	A2D2	A2A5	A1G1 A1E1	A2E2	A2B5	A1C1 A1A1

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FAULTY INBOUND LINE

An inbound bit line is active when its corresponding outbound bit line is not active. A further test is made to ensure that a short condition does not exist. During this portion of the test, a bit is placed on an outbound line. Proper operation causes the corresponding bit on Bus In to be activated. If an additional bit is received, two possibilities exist:

1. The bit line is shorted to a voltage source.
2. The bit line is shorted to an active bit line.

The outbound bit corresponding to the additional bit is placed on the outbound lines. If both bits are received again, it is assumed to be a short to a voltage source. If only one bit is received, it is assumed to be shorted to an active signal line. Possible causes of failure are:

- A faulty driver in the controller.
- A faulty receiver in the storage control.
- A short to a voltage in either the controller or storage control.

Note: *If an EC was installed just prior to the failure, check the EC instructions and verify the changes made.*

For strings with multiple controllers, reconfigure to the smallest configuration that sustains the error.

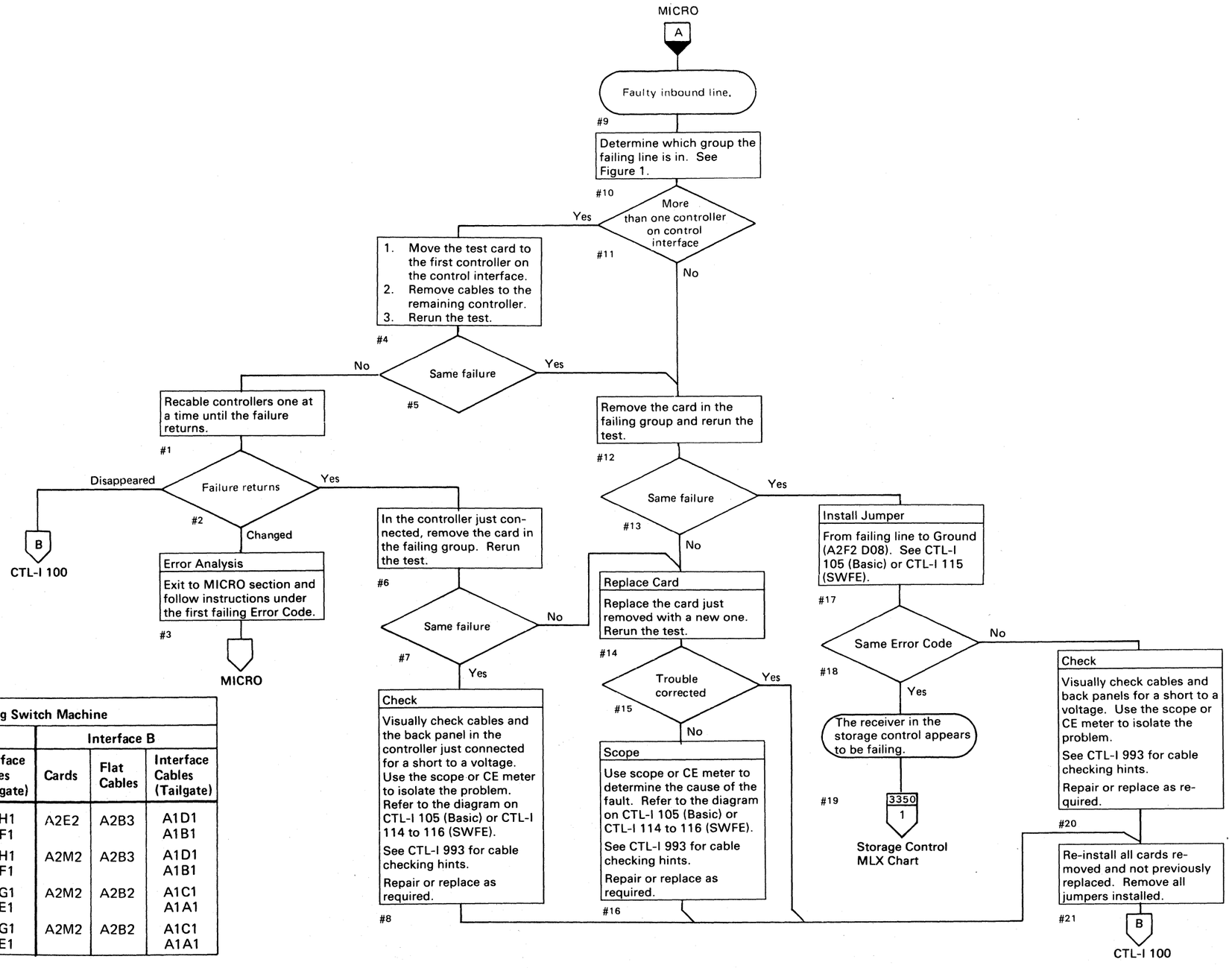

Figure 1. Inbound Signal Lines

Group	Line Name	Basic Machine			String Switch Machine					
					Interface A			Interface B		
		Cards	Flat Cables	Interface Cables (Tailgate)	Cards	Flat Cables	Interface Cables (Tailgate)	Cards	Flat Cables	Interface Cables (Tailgate)
Group 1	Bus In Bits	A2F2	A2C3	A1H1 A1F1	A2D2	A2A3	A1H1 A1F1	A2E2	A2B3	A1D1 A1B1
Group 2	Sync In	A2F2 A2K2	A2C3	A1H1 A1F1	A2M2	A2A3	A1H1 A1F1	A2M2	A2B3	A1D1 A1B1
Group 3	Error Alert CE Alert	A2F2 A2L2	A2C2	A1G1 A1E1	A2M2	A2A2	A1G1 A1E1	A2M2	A2B2	A1C1 A1A1
Group 4	All Others	A2F2 A2K2	A2C2	A1G1 A1E1	A2M2	A2A2	A1G1 A1E1	A2M2	A2B2	A1C1 A1A1

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SHORTED INTERFACE LINES

This portion of the test determines the interaction between two interface lines. A bit is placed on one of the outbound lines and two or more inbound lines are detected. When the outbound lines for the spurious signals are activated, the line for the original line is also activated. For example:

Test 1A

Bus Out = Bit 0
Bus In = Bit 0 and Bit 1.

This is an error because Bit 1 is not expected.

Test 1B

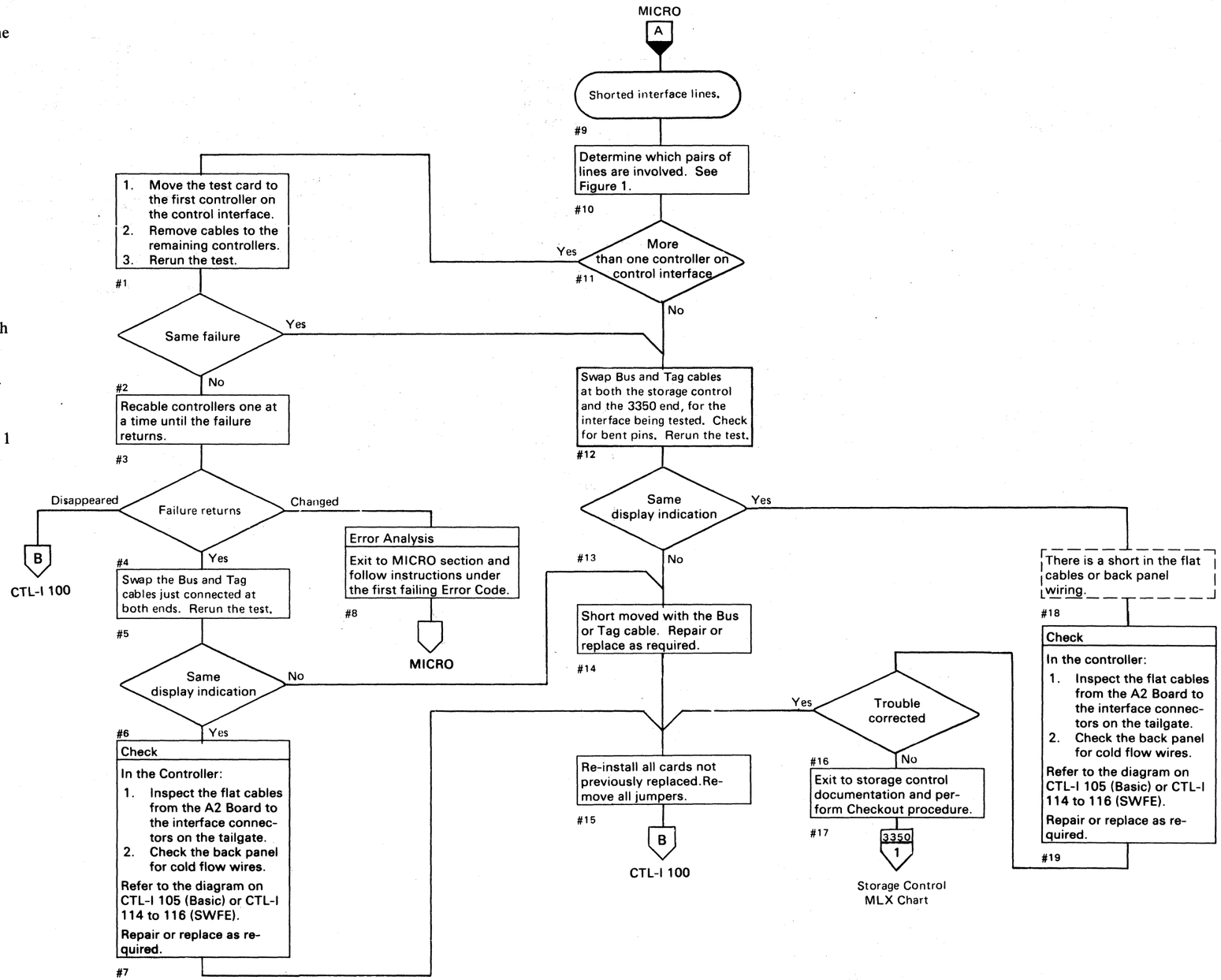
Bus Out = Bit 1
Bus In = Bit 0 and Bit 1.

This also is an error because Bit 0 is not expected. These errors indicate that there is a short since each line activates the other.

This program cannot determine whether the outbound or inbound lines are shorted, but can point to a pair of possibilities. In the example above, the Bus In display was identical in both cases. However, Bus In Bits 0 and 1 may not be the shorted pair. (See Figure 1 for corresponding lines and CTL-I 82 for Bus In, Bus Out shorted examples.)

Figure 1. Interface Lines

Displayed Line	Corresponding Line
Bus In Bit 0	Bus Out Bit 0
Bus In Bit 1	Bus Out Bit 1
Bus In Bit 2	Bus Out Bit 2
Bus In Bit 3	Bus Out Bit 3
Bus In Bit 4	Bus Out Bit 4
Bus In Bit 5	Bus Out Bit 5
Bus In Bit 6	Bus Out Bit 6
Bus In Bit 7	Bus Out Bit 7
Error Alert	Tag Bus Bit 6
Select Active	Select Hold
Sync In	Tag Bus Bit 0
CE Alert	Tag Bus Bit P
Normal End	Tag Bus Bit 4
Check End	Tag Bus Bit 5
Tag Valid	Tag Gate
Index Alert	Tag Bus Bit 7



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SHORTED INTERFACE LINES

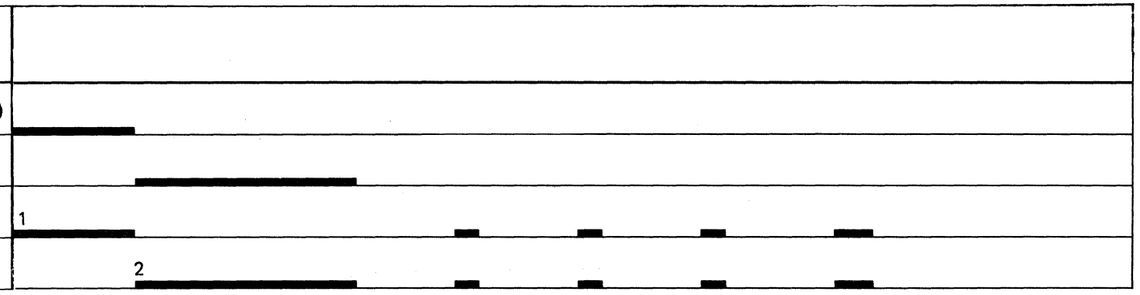
Scope Setup

Loop Routine BF Test 1.
Sweep 0.5 μs/div
Trigger
Slope (+)
Test points (A)
Ch1/Ch2 Volts/div 0.2
Probe ×10

Legend: Inactive, Active level, Tolerance

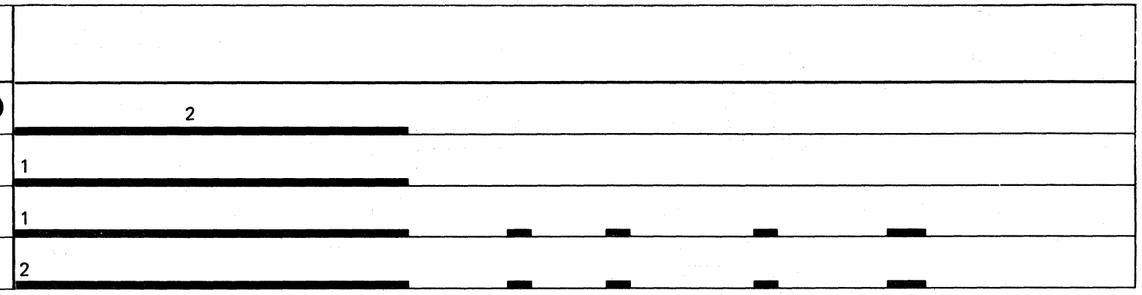
Example 1. Bus Operation Normal

Chart Line No.	Line Name	ALD	Test Point	
1	Bus Out Bit 1 NPL	BF130 BM100 (BN100)	A2G2 G13 A2D2(A2E2) J11	(A)
2	Bus Out Bit 0 NPL	BF130 BM100 (BN100)	A2G2 G12 A2D2(A2E2) G11	
3	Bus In Bit 1 NPL	BA150 BM160 (BN160)	A2F2 B03 A2D2(A2E2) U07	
4	Bus In Bit 0 NPL	BA150 BM160 (BN160)	A2F2 D06 A2D2(A2E2) U06	



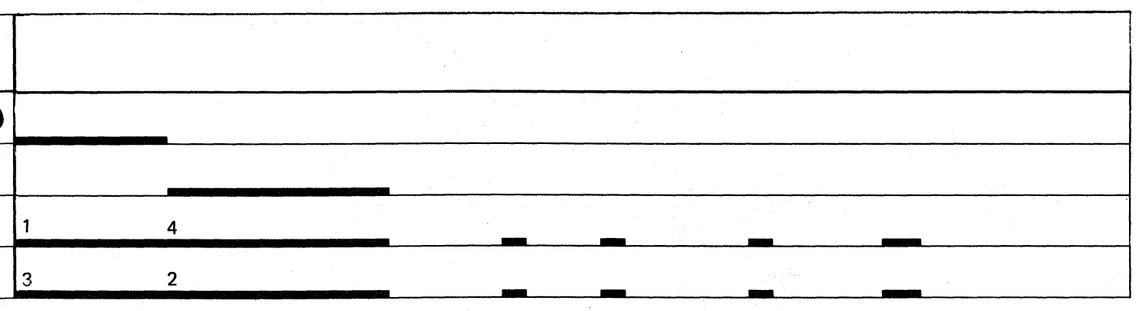
Example 2. Bus Out Bits 0 and 1 Shorted

Chart Line No.	Line Name	ALD	Test Point	
1	Bit Out Bit 1 NPL	BF130 BM100 (BN100)	A2G2 G13 A2D2(A2E2) J11	(A)
2	Bus Out Bit 0 NPL	BF130 BM100 (BN100)	A2G2 G12 A2D2(A2E2) G11	
3	Bus In Bit 1 NPL	BA150 BM160 (BN160)	A2F2 B03 A2D2(A2E2) U07	
4	Bus In Bit 0 NPL	BA150 BM160 (BN160)	A2F2 D06 A2D2(A2E2) U06	



Example 3. Bus In Bits 0 and 1 Shorted

Chart Line No.	Line Name	ALD	Test Point	
1	Bus Out Bit 1 NPL	BF130 BM100 (BN100)	A2G2 G13 A2D2(A2E2) J11	(A)
2	Bus Out Bit 0 NPL	BF130 BM100 (BN100)	A2G2 G12 A2D2(A2E2) G11	
3	Bus In Bit 1 NPL	BA150 BM160 (BN160)	A2F2 B03 A2D2(A2E2) U07	
4	Bus In Bit 0 NPL	BA150 BM160 (BN160)	A2F2 D06 A2D2(A2E2) U06	



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FAULTY RESPONSE OR SYNC OUT

After the Sync In and Normal End lines are checked and found to be functioning normally, they are used to check the Sync Out and Response lines. The sequence is as follows:

1. Set the Storage Control to Data Response mode.
2. Raise Tag Bit 0, which causes Sync In.
3. Sync In activates Sync Out.
4. Sync Out sets a latch on the test card.
5. The latch forces Normal End to become active.
6. Normal End is used to raise Response.
7. Response resets the latch and drops Normal End.

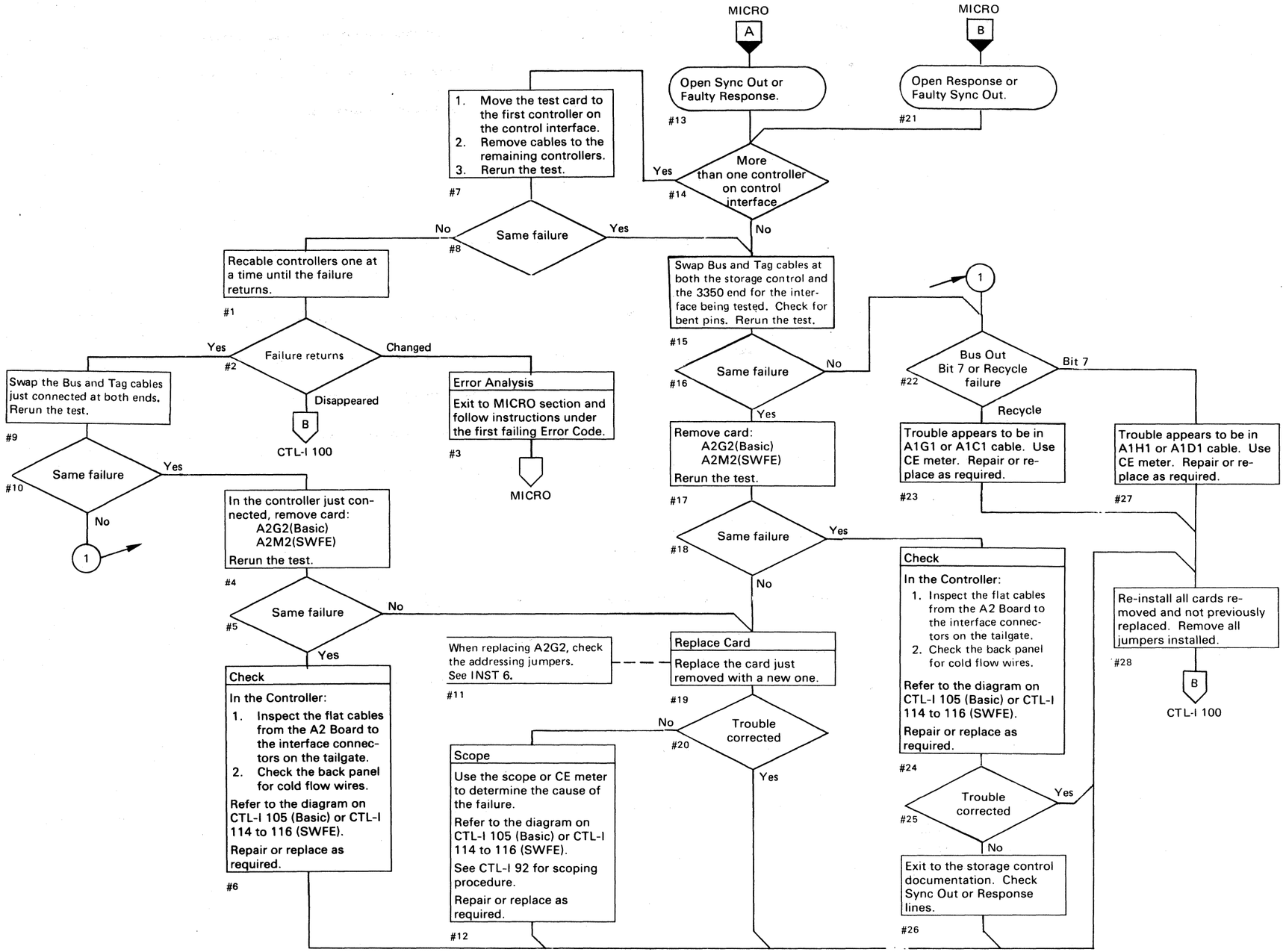
A Sync Out failure (open) is indicated by a missing Normal End. A Response failure (open) is indicated by an active Normal End after raising Response. Possible causes of failure are:

- Open interface cables or a short to ground.
- Faulty receiver in the controller.
- Open, short to ground, or short to plus voltage on the back panel or flat cable in either the controller or storage control.
- Faulty driver in the storage control.

Note: *If an EC was installed just prior to the failure, check the EC instructions and verify the changes made.*

For strings with multiple controllers, reconfigure to the smallest configuration that sustains the error.

See CTL-I 92 for typical timing relationships.



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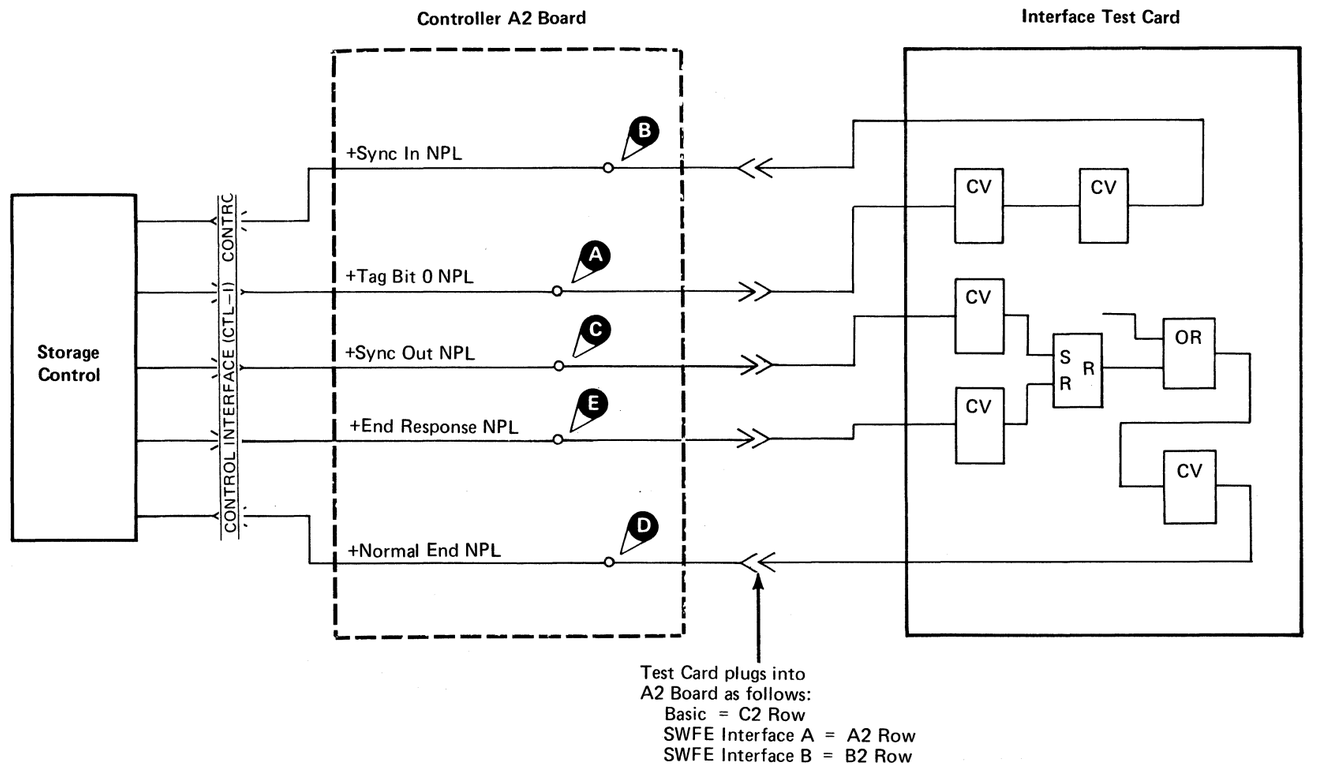
OPEN SYNC OUT

Scope Setup

Sweep 0.2 μs/div
Trigger Slope (+)
Test Point (A)
Ch1/Ch2 Volts/div 0.2
Probe ×10

See OPER 90 for additional theory.



Note: *Sequence chart shows typical relationships. Timings vary slightly depending on the interface length and configuration.*

Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point		
1	+Tag Bit 0 NPL	BF100 BM100 (BN100)	A2G2 D13 A2D2(A2E2) B07	A	
2	+Sync In NPL	BE160 BR190	A2K2 D04 A2M2 J06(J07)	B	1
3	+Sync Out NPL	BF100 BR130	A2G2 B13 A2M2 S03(D03)	C	2
4	+Normal End NPL	BE160 BR170 (BR180)	A2K2 D11 A2M2 U13(P07)	D	3 5
5	+End Response NPL	BF160 BR130	A2G2 S03 A1M2 S04(B05	E	4

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PHILOSOPHY OF INTERFACE ANALYSIS

The recommended approach to interface problems is to replace the designated replaceable unit in the controller and determine if the problem is corrected. (The replacements are normally made prior to coming to this page.) When successful, this method causes a minimum impact on system operation.

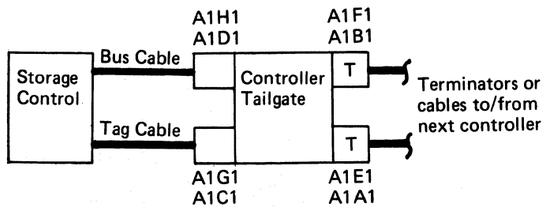
If further action is required, go to the Interface Checkout procedure for the storage control/drive interface. If the problem is not resolved, return here.

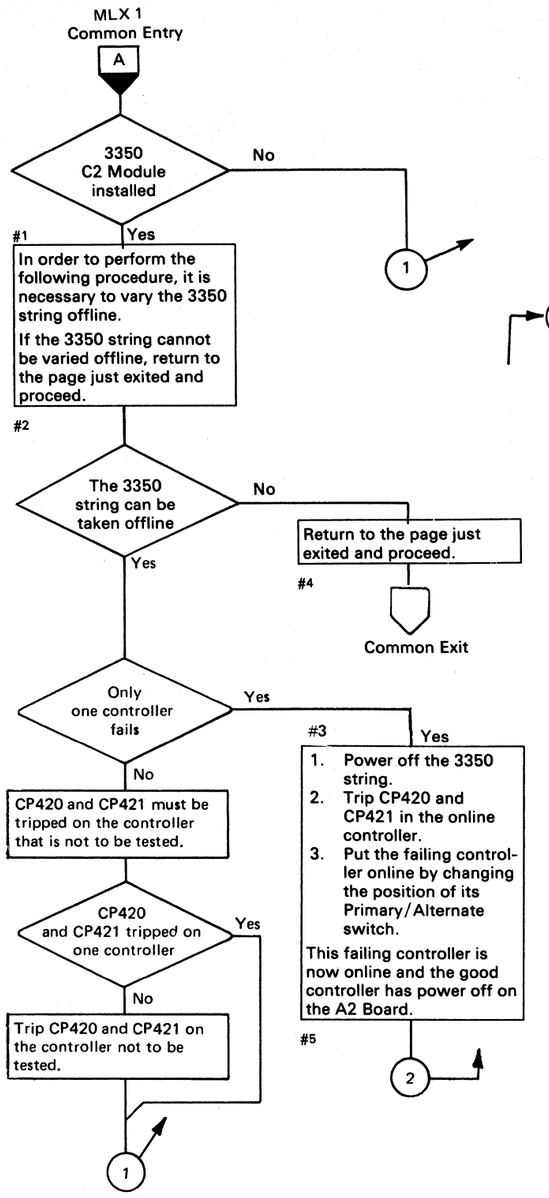
Service Hints

1. If more than one controller is attached to the interface, install the terminators in the first controller and check that it functions correctly; then proceed to the next controller and continue until all units function correctly.
2. Note that the lines listed below require a back panel connection to distribute the signal to the next controller. If a connector is loose at the A2 Board in any controller, all controllers may appear to fail. Check that the following connectors in all controllers are securely seated:

	Basic Machine	Interface A	Interface B
Bus Out bit 3	A2C4	A2A4	A2B4
Bus Out bit 4	A2C4	A2A4	A2B4
Tag Bus bit 6	A2C5	A2A5	A2B5
Tag Bus bit P	A2C5	A2A5	A2B5
Bus In bit 3	A2C3	A2A3	A2B3
Bus In bit 4	A2C3	A2A3	A2B3
Error Alert	A2C2	A2A2	A2B2
Index Alert	A2C2	A2A2	A2B2

3. For new installations, location changes, or whenever cables are removed, the interface cables may be transposed. Verify the cabling at the tailgate.





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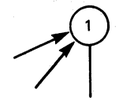


INTERFACE ANALYSIS PROCEDURE

Operating Instructions

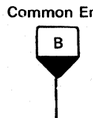
1. Request the operator to vary offline the storage control and all its drives.
2. On the controller to be tested, operate the Power Off switch to remove ac power from the subsystem.
3. Install the Interface Test Card (arrow up ▲) on the pin side of the A2 Board (see Figure 1, CTL-I 102):

	Basic 3350	With String Switch	
		Interface A	Interface B
Card Location	A2C2	A2A2	A2B2

4. Plug the Interface Test Card voltage cable connector on A2K2. See Figure 1, CTL-I 102.
5. Operate the controller Power On switch.
6. Assure that the diskette containing the 3350 microdiagnostics is in the Storage Control reader (see MICRO 8).
7. If attached to a 3880 Storage Control refer to the 3880 maintenance documentation for running BF (Control Interface bringup program)
   3350 MLX exit 3.

3880 Storage Control MLX Chart

   If attached to a 3830 or ISC perform the following steps at the Storage Control CE Panel:
   a. Set the Operation Mode switch to CE Normal.
   b. Set Enter/Display Mode switch to Program Data Enter/Display.
   c. Operate the Stop/SI switch.
   d. Operate the Reset switch.
   e. Operate the IMPL switch.



   f. When 'CABF' is displayed in the Address Check Program Display lamps, routine BF (CTL Interface Bringup Program) is ready for execution.
   g. Set the Data Entry switches to '00' and operate the Execute switch. 'CFBF' in the Address Check Program Display lamps indicates successful completion of routine BF. 'EOxx' indicates an error condition, where xx is the error number (EOxx = BFxx). Display and record the message bytes, then locate BFxx in the 3350 MICRO section for the meaning and the analysis of the error. See CTL-I 100 for additional operating instructions for 3830 and ISC's.
8. Terminate control interface testing by performing the following steps:
   a. Operate the controller Power Off switch to remove power from the controller being tested.
   b. Remove the Interface Test Card and its cable.
   c. Operate the controller Power On switch to restore power to the subsystem.
   d. Insert the functional microprogram disk in the reader. (3830 or ISC only.)
   e. Operate the following switches at the Storage Control CE Panel (3830 or ISC only):
      Stop/SI
      Reset
      IMPL
   f. If attached to a 3880 Storage Control, refer to the 3880 maintenance documentation for restoring the Storage Control from the MD (Maintenance Device) after running BF.

3880 Storage Control MLX Chart

9. If necessary, return to the section exited from. Otherwise, exit to START 500, Entry A.

INTERFACE ANALYSIS

To Display Message Bytes

1. Set the Data Entry switches to '20'.
2. Operate the storage control Execute switch. The messages appear in the Address Check Program Display lamps. Refer to MICRO 700 for a description of the messages.

Note: *Two message bytes are displayed at the same time.*

To Reset and Restart Program

1. Operate the Stop/SI switch
2. Operate the Reset switch
3. Operate the Start switch.
4. Return to step 7 on CTL-I 100 under Operating Instructions

To Loop A Test

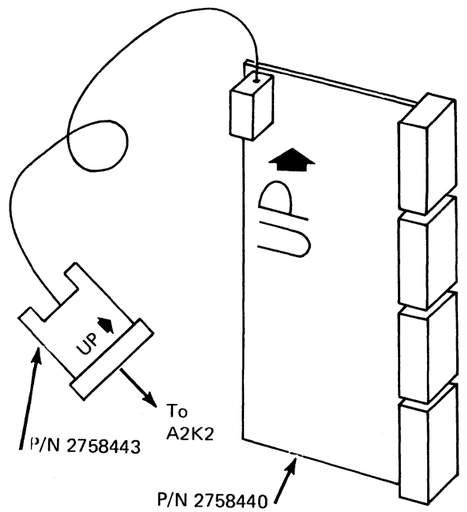
1. Operate the Stop/SI switch.
2. Operate the Reset switch.
3. Operate the Start switch.
4. After 'CABF' is displayed in the Address Check Program Display lamps, enter 10,YY,ZZ,00.

   Where YY = Test Number

   ZZ = 00 for stop on error
   01 to loop and display error number
   02 to loop and display line message
   03 for scope loop

   00 = start execution

Figure 1. Interface Test Card



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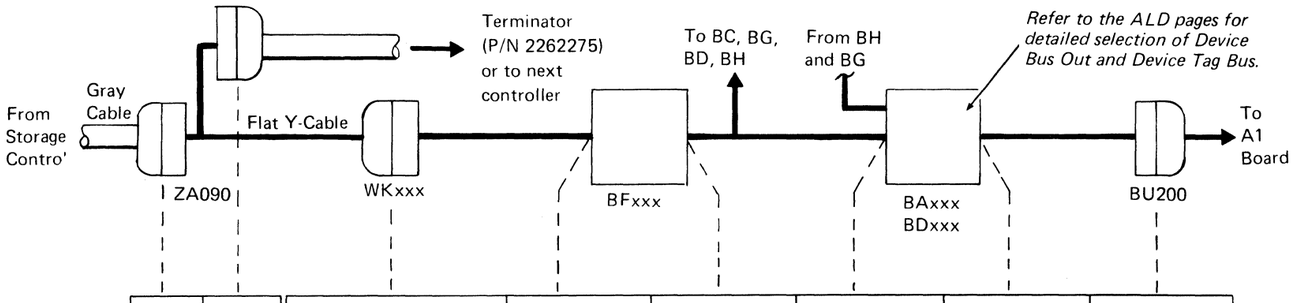
INTERFACE CONNECTOR DIAGRAM

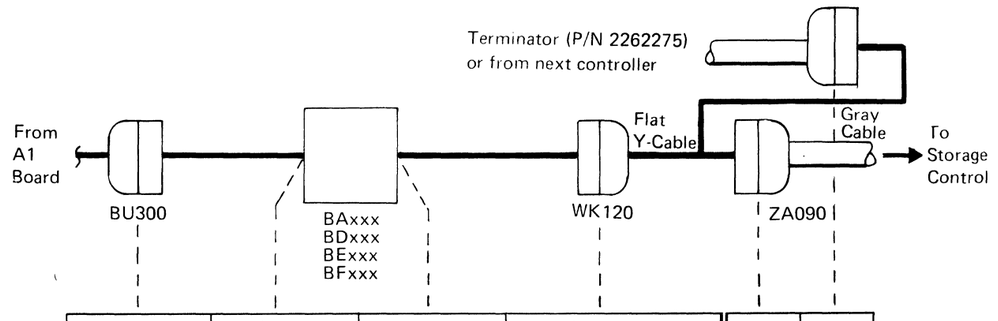
BUS OUT/TAG OUT



		A1*	A1*	A2	A2	A2	A2	A2	A2
Bus Out Bit	0	H1D04	F1B04	C4D05(WK100)	G2G12(BF130)	G2P02(BF130)	F2M02(BA140)	F2P10(BA110)	V5B02(BU200)
	1	H1B05	F1D05	C4B05(WK100)	G2G13(BF130)	G2J13(BF130)	F2M03(BA140)	F2P12(BA110)	V5B04(BU200)
	2	H1D06	F1B06	C4D06(WK100)	G2P03(BF130)	G2M02(BF130)	F2S05(BA140)	F2U02(BA110)	V5B05(BU200)
	3	H1B08	F1D08	C4B08/B09(WK100) 1	G2M03(BF130)	G2P05(BF130)	F2U10(BA140)	F2S03(BA110)	V5B06(BU200)
	4	H1D09	F1B09	C4D09/D10(WK100) 1	G2M04(BF130)	G2P04(BF130)	F2U11(BA140)	F2S12(BA110)	V5B08(BU200)
	5	H1B10	F1D10	C4B10(WK100)	G2M07(BF130)	G2P06(BF130)	F2S13(BA140)	F2U12(BA110)	V5B09(BU200)
	6	H1D11	F1B11	C4D11(WK100)	G2M09(BF130)	G2P11(BF130)	F2S09(BA130)	F2U05(BA110)	V5B10(BU200)
	7	H1B12	F1D12	C4B12(WK100)	G2P10(BF130)	G2M10(BF130)	F2U13(BA140)	F2U09(BA110)	V5B12(BU200)
Bus Out Bit	P	H1B03	F1D03	C4B02(WK100)	G2P09(BF130)	–	–	F2M07(BA110)	V5B13(BU200)
Sync Out		H1D13	F1B13	C4D13(WK110)	G2B13(BF100)	G2D12(BF100)	–	–	–
Tag Bus Bit	0	G1B03	E1D03	C5B02(WK110)	G2D13(BF100)	G2J03(BF100)	L2G04(BD100)	–	–
	4	G1B05	E1D05	C5B05(WK110)	G2G02(BF100)	G2J02(BF100)	L2G08(BD100)	–	–
	5	G1D04	E1B04	C5D05(WK110)	G2B03(BF100)	G2B02(BF100)	L2G13(BD100)	L2J10(BD220)	V5D02(BU200)
	6	G1B08	E1D08	C5B08/B09(WK110) 1	G2B05(BF100)	G2D07(BF100)	L2G11(BD100)	L2P03(BD220)	V5D03(BU200)
	7	G1D06	E1B06	C5D06(WK110)	G2D04(BF100)	G2B07(BF100)	L2G12(BD100)	L2J12(BD220)	V5D05(BU200)
Tag Bus Bit	P	G1D09	E1B09	C5D09/D10(WK110) 1	G2B04(BF100)	G2D10(BF100)	L2G09(BD100)	L2J04(BD220)	V5D06(BU200)
Tag Gate		G1B10	E1D10	C5B10(WK110)	G2J11(BF130)	–	–	L2J02(BD230)	V5D07(BU200)
Response		G1B12	E1D12	C5B12(WK100)	G2S03(BF160)	–	–	–	–
Select Hold		G1D11	E1B11	C5D11(WK110)	G2B12(BF100)	–	–	L2M03(BD230)	V5D09(BU200)
Recycle		G1D13	E1B13	C5D13(WK110)	G2U12(BF160)	G2S10(BF160)	–	–	–

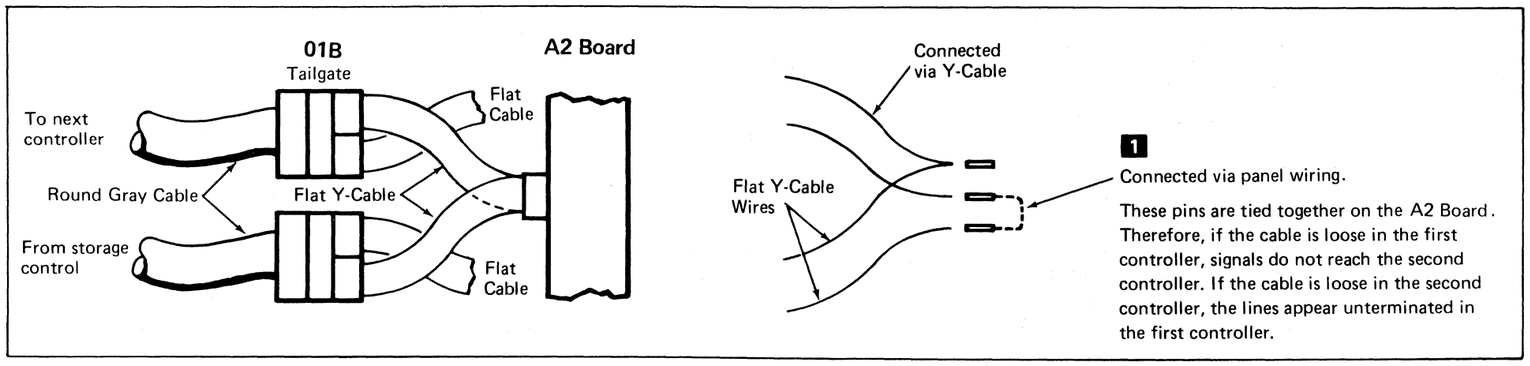
*Tailgate

BUS IN/TAG IN



A2	A2	A2	A2 (See Note)	A1*	A1*		
V4B02(BU300)	F2B10(BA160)	F2D06(BA150)	C3D05(WK120)	H1J04	F1G04	Bus In Bit	0
V4B04(BU300)	F2B07(BA160)	F2B03(BA150)	C3B05(WK120)	H1G05	F1J05		1
V4B05(BU300)	F2G03(BA160)	F2D10(BA150)	C3D06(WK120)	H1J06	F1G06		2
V4B06(BU300)	F2B09(BA160)	F2D09(BA150)	C3B08/B09(WK120) 1	H1G08	F1J08		3
V4B08(BU300)	F2G12(BA160)	F2J02(BA150)	C3D09/D10(WK120) 1	H1J09	F1G09		4
V4B09(BU300	F2J04(BA160)	F2J07(BA150)	C3B10(WK120)	H1G10	F1J10		5
V4B10(BU300)	F2G05(BA160)	F2J11(BA150)	C3D11(WK120)	H1J11	F1G11		6
V4B12(BU300)	F2G13(BA160)	F2J03(BA150)	C3B12(WK120)	H1G12	F1J12		7
V4B13(BU300)	F2J13(BA160)	F2J12(BA150)	C3B02(WK120)	H1G03	F1J03	Bus In Bit	P
–	–	K2D04(BE160)	C3D13(WK120)	H1J13	F1G13	Sync In	
–	–	K2J03(BE160)	C2B02(WK120)	G1G03	E1J03	Select Active	
–	–	K2D11(BE160)	C2B05(WK120)	G1G05	E1J05	Normal End	
–	–	K2D05(BE160)	C2D06(WK120)	G1J06	E1G06	Check End	
V5D13(BU300)	G2S07(BF160)	K2G05(BE160)	C2D05(WK120)	G1J04	E1G04	Tag Valid	
–	–	L2B09(BD230)	C2B08/B09(WK120) 1	G1G08	E1J08	Error Alert	
–	–	K2B05(BE160)	C2D09/D10(WK120) 1	G1J09	E1G09	Index Alert	
–	–	L2J05(BD230)	C2B12(WK120)	G1G12	E1J12	CE Alert	

*Tailgate



1 Connected via panel wiring.

These pins are tied together on the A2 Board. Therefore, if the cable is loose in the first controller, signals do not reach the second controller. If the cable is loose in the second controller, the lines appear unterminated in the first controller.

All interface lines and pins are NPL levels. All logic lines and pins are MST levels. See CTL-I section divider tab for signal levels.

Note: *Pin numbers do not appear on WK120. See ALD pages indicated in the column to the left or the chart on ZA090 for pin identification.*

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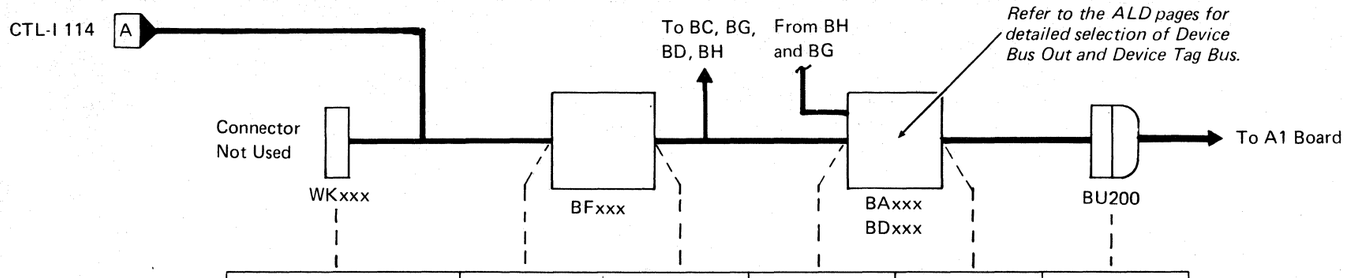
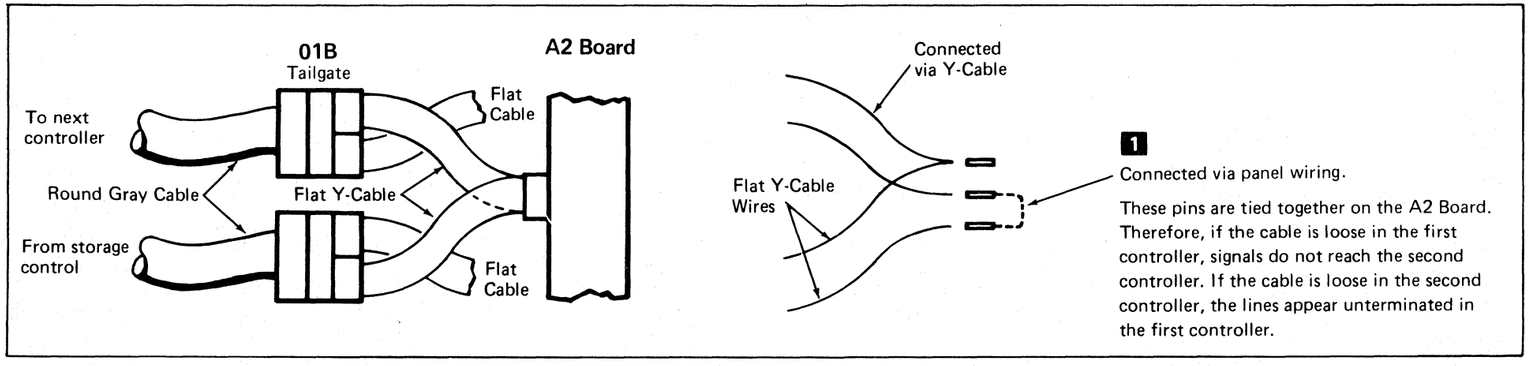
INTERFACE CONNECTOR DIAGRAM (With String Switch)

BUS OUT/TAG OUT

All interface lines and pins are NPL levels. All logic lines and pins are MST levels. See CTL-I section divider tab for signal levels.



		A2	A2	A2	A2	A2	A2		
Bus Out Bit	0	C4D05(WK100)	G2G12(BF130)	G2P02(BF130)	F2M02(BA140)	F2P10(BA110)	V5B02(BU200)	Bus Out Bit	0
	1	C4B05(WK100)	G2G13(BF130)	G2J13(BF130)	F2M03(BA140	F2P12(BA110)	B5B04(BU200)		1
	2	C4D06(WK100)	G2P03(BF130)	G2M02(BF130)	F2S05(BA140)	F2U02(BA110)	V5B05(BU200)		2
	3	C4B08/B09(WK100) 1	G2M03(BF130)	G2P05(BF130)	F2U10(BA140)	F2U10(BA1[illegible]0)	V5B06(BU200)		3
	4	C4D09/D10(WK100) 1	G2M04(BF130)	G2P04(BF130)	F2U11(BA140)	F2S12(BA110)	V5B08(BU200)		4
	5	C4B10(WK100)	G2M07(BF130)	G2P06(BF130)	F2S13(BA140)	F2U12(BA110)	V5B09(BU200)		5
	6	C4D11(WK100)	G2M09(BF130)	G2P11(BF130)	F2S09(BA130)	F2U05(BA110)	V5B10(BU200)		6
	7	C4B12(WK100)	G2P10(BF130)	G2M10(BF130)	F2U13(BA140)	F2U09(BA110)	V5B12(BU200)		7
Bus Out Bit	P	C4B02(WK100)	G2P09(BF130)	–	–	F2M07(BA110)	V5B13(BU200)	Bus Out Bit	P
Sync Out		C4D13(WK110)	G2B13(BF100)	G2D12(BF100)	–	–	–	Sync Out	
Tag Bus Bit	0	C5B02(WK110)	G2D13(BF100)	G2J03(BF100)	L2G04(BD100)	–	–	Tag Bus Bit	0
	4	C5B05(WK110)	G2G02(BF100)	G2J02(BF100)	L2G08(BD100)	–	–		4
	5	C5D05(WK110)	G2B03(BF100)	G2B02(BF100)	L2G13(BD100)	L2J10(BD220)	V5D02(BU200)		5
	6	C5B08/B09(WK110) 1	G2B05(BF100)	G2D07(BF100)	L2G11(BD100)	L2P03(BD220)	V5D03(BU200)		6
	7	C5D06(WK110)	G2D04(BF100)	G2B07(BF100)	L2G12(BD100)	L2J12(BD220)	V5D05(BU200)		7
Tag Bus Bit	P	C5D09/D10(WK110) 1	G2B04(BF100)	G2D10(BF100)	L2G09(BD100)	L2J04(BD220)	V5D06(BU200)	Tag Bus Bit	P
Tag Gate		C5B10(WK110)	G2J11(BF130)	–	–	L2J02(BD230)	V5D07(BU200)	Tag Gate	
Response		C5B12(WK100)	G2S03(BF160)	–	–	–	–	Response	
Select Hold		C5D11(WK110)	G2S12(BF100)	–	–	L2M03(BD230)	V5D09(BU200)	Select Hold	
Recycle		C5D13(WK110)	G2U12(BF160)	G2S10(BF160)	–	–	–	Recycle	



1 Connected via panel wiring.

These pins are tied together on the A2 Board. Therefore, if the cable is loose in the first controller, signals do not reach the second controller. If the cable is loose in the second controller, the lines appear unterminated in the first controller.

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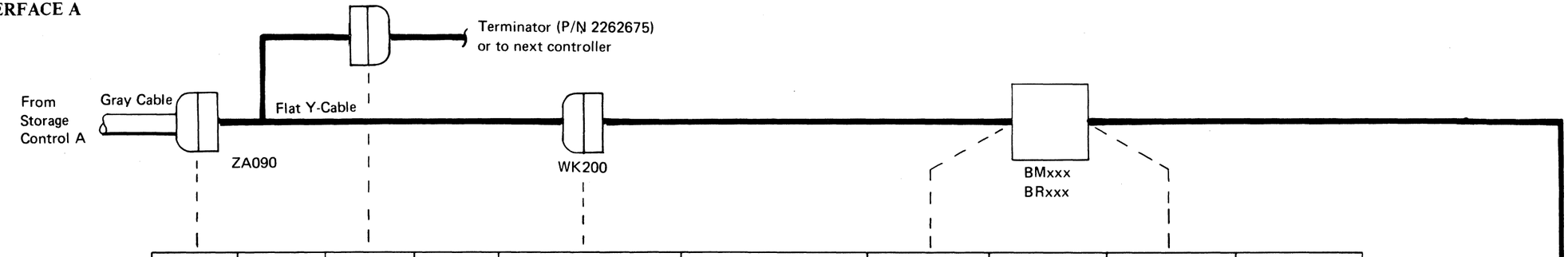
INTERFACE CONNECTOR DIAGRAM (With String Switch)

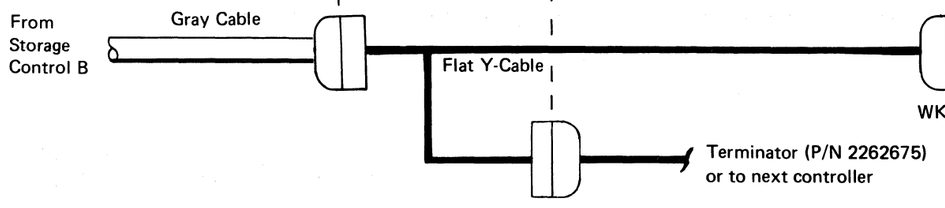
BUS OUT/TAG OUT INTERFACE A

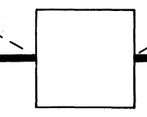


	Interface A A1	Interface B A1	Interface A A1	Interface B A1	Interface A A2	Interface B A2	Interface A A2	Interface B A2	Interface A A2	Interface B A2	
Bus Out Bit 0	H1D04	D1D04	F1B04	B1B04	A4D05(WK200)	B4D05(WK210)	D2G11(BM100)	E2G11(BN100)	D2J09(BM110)	E2J09(BN110)	Bus Out Bit 0
1	H1B05	D1B05	F1D05	B1D05	A4B05(WK200)	B4B05(WK210)	D2J11(BM100)	E2J11(BN100)	D2G08(BM110)	E2G08(BN110)	1
2	H1D06	D1D06	F1B06	B1B06	A4D06(WK200)	B4D06(WK210)	D2J05(BM100)	E2J05(BN100)	D2B12(BM110)	E2B12(BN110)	2
3	H1B08	D1B08	F1D08	B1D08	A4B08/B09(WK200) 1	B4B08/B09(WK210) 1	D2J04(BM100)	E2J04(BN100)	D2B13(BM110)	E2B13(BN110)	3
4	H1D09	D1D09	F1B09	B1B09	A4D09/D10(WK200) 1	B4D09/D10(WK210) 1	D2J03(BM100)	E2J03(BN100)	D2D13(BM110)	E2D13(BN110)	4
5	H1B10	D1B10	F1D10	B1D10	A4B10(WK200)	B4B10(WK210)	D2D07(BM100)	E2D07(BN100)	D2D12(BM110)	E2D12(BN110)	5
6	H1D11	D1D11	F1B11	B1B11	A4D11(WK200)	B4D11(WK210)	D2G03(BM100)	E2G03(BN100)	D2D03(BM110)	E2D03(BN110)	6
7	H1B12	D1B12	F1D12	B1D12	A4B12(WK200)	B4B12(WK210)	D2G04(BM100)	E2G04(BN100)	D2B03(BM110)	E2B03(BN110)	7
Bus Out Bit P	H1B03	D1B03	F1D03	B1D03	A4B02(WK200)	B4B02(WK210)	D2G05(BM100)	E2G05(BN100)	D2D02(BM110)	E2D02(BN110)	Bus Out Bit P
Sync Out	H1D13	D1D13	F1B13	B1B13	A4D13(WK200)	B4D13(WK210)	M2S03(BR130)	M2D03(BR130)	M2G03(BR140)★	M2G03(BR140)★	Sync Out
Tag Bus Bit 0	G1B03	C1B03	E1D03	A1D03	A5B02(WK200)	B5B02(WK210)	D2B07(BM100)	E2B07(BN100)	D2M03(BM120)	E2M03(BN120)	Tag Bus Bit 0
4	G1B05	C1B05	E1D05	A1D05	A5B05(WK200)	B5B05(WK210)	D2G12(BM100)	E2G12(BN100)	D2P03(BM120)	E2P03(BN120)	4
5	G1D04	C1D04	E1B04	A1B04	A5D05(WK200)	B5D05(WK210)	D2D09(BM100)	E2D09(BN100)	D2M04(BM120)	E2M04(BN120)	5
6	G1B08	C1B08	E1D08	A1D08	A5B08/B09(WK200) 1	B5B08/B09(WK210) 1	D2D10(BM100)	E2D10(BN100)	D2B02(BM120)	E2B02(BN120)	6
7	G1D06	C1D06	E1B06	A1B06	A5D06(WK200)	B5D06(WK210)	D2B09(BM100)	E2B09(BN100)	D2B05(BM120)	E2B05(BN120)	7
Tag Bus Bit P	G1D09	C1D09	E1B09	A1B09	A5D09/D10(WK200) 1	B5D09/D10(WK210) 1	D2D11(BM100)	E2D11(BN100)	D2D05(BM120)	E2D05(BN120)	Tag Bus Bit P
Tag Gate	G1B10	C1B10	E1D10	A1D10	A5B10(WK200)	B5B10(WK210)	D2D06(BM100)	E2D06(BN100)	D2G07(BM120)	E2G07(BN120)	Tag Gate
Response	G1B12	C1B12	E1D12	A1D12	A5B12(WK200)	B5B12(WK210)	M2S04(BR130)	M2B05(BR130)	M2M04(BR190)	M2D06(BR190)	Response
Select Hold	G1D11	C1D11	E1B11	A1D11	A5D11(WK200)	B5D11(WK210)	D2J12(BM100)	E2J12(BN100)	D2G09(BM120)	E2G09(BN120)	Select Hold
Recycle	G1D13	C1D13	E1B13	A1D13	A5D13(WK200)	B5D13(WK210)	M2U02(BR130)	M2B02(BR130)	M2J11(BR190)	M2D11(BR190)	Recycle

A CTL-I 113

BUS OUT/TAG OUT INTERFACE B





★ *Sync Out bypasses this converter.*

Note: *All interface lines and pins are NPL levels. All logic lines and pins are MST levels. See CTL-I section divider tab for signal levels.*

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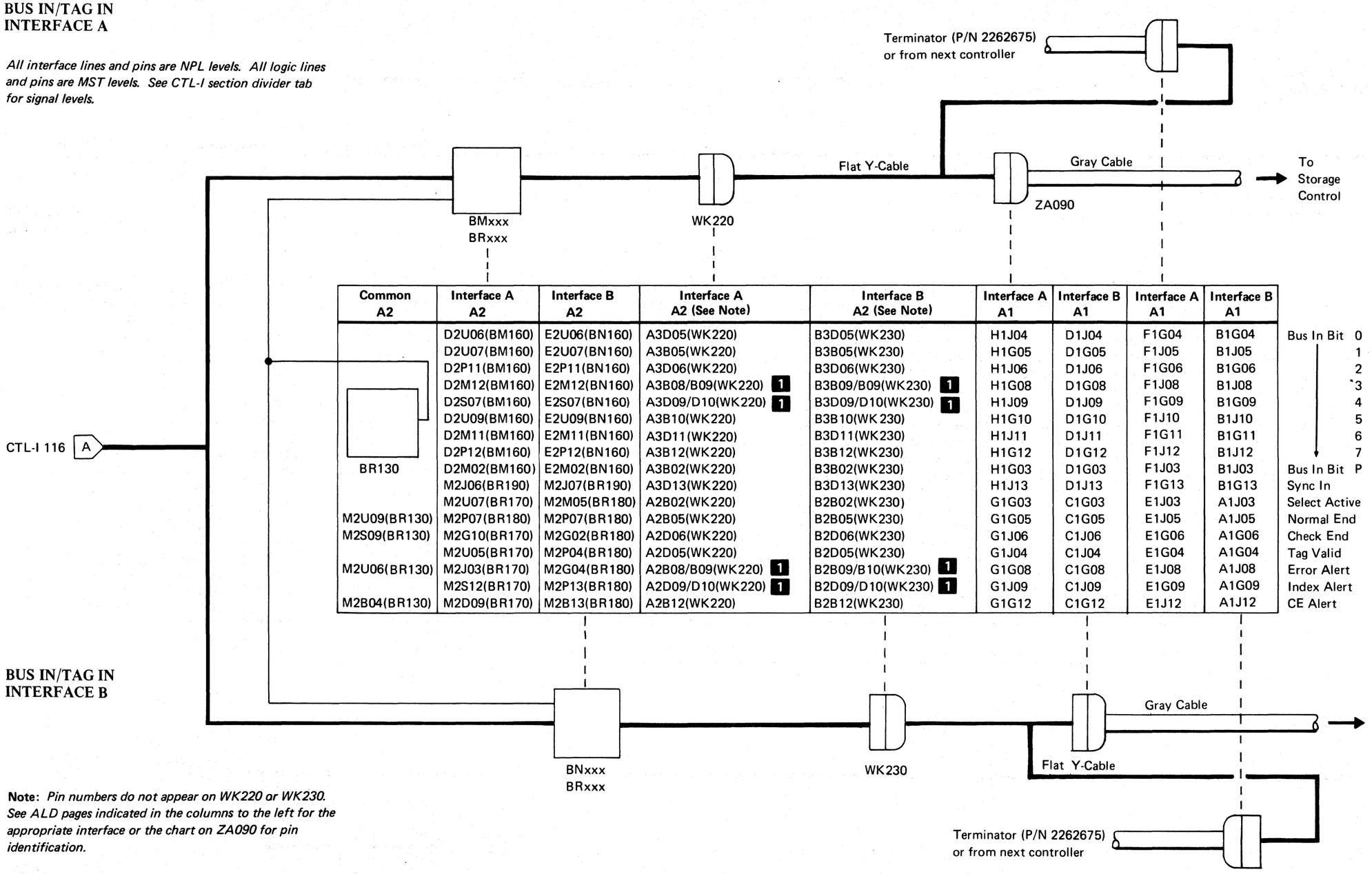
INTERFACE CONNECTOR DIAGRAM (With String Switch)

BUS IN/TAG IN INTERFACE A

All interface lines and pins are NPL levels. All logic lines and pins are MST levels. See CTL-I section divider tab for signal levels.



Common A2	Interface A A2	Interface B A2	Interface A A2 (See Note)	Interface B A2 (See Note)	Interface A A1	Interface B A1	Interface A A1	Interface B A1	
	D2U06(BM160)	E2U06(BN160)	A3D05(WK220)	B3D05(WK230)	H1J04	D1J04	F1G04	B1G04	Bus In Bit 0
	D2U07(BM160)	E2U07(BN160)	A3B05(WK220)	B3B05(WK230)	H1G05	D1G05	F1J05	B1J05	1
	D2P11(BM160)	E2P11(BN160)	A3D06(WK220)	B3D06(WK230)	H1J06	D1J06	F1G06	B1G06	2
	D2M12(BM160)	E2M12(BN160)	A3B08/B09(WK220) 1	B3B09/B09(WK230) 1	H1G08	D1G08	F1J08	B1J08	3
	D2S07(BM160)	E2S07(BN160)	A3D09/D10(WK220) 1	B3D09/D10(WK230) 1	H1J09	D1J09	F1G09	B1G09	4
	D2U09(BM160)	E2U09(BN160)	A3B10(WK220)	B3B10(WK230)	H1G10	D1G10	F1J10	B1J10	5
	D2M11(BM160)	E2M11(BN160)	A3D11(WK220)	B3D11(WK230)	H1J11	D1J11	F1G11	B1G11	6
	D2P12(BM160)	E2P12(BN160)	A3B12(WK220)	B3B12(WK230)	H1G12	D1G12	F1J12	B1J12	7
	D2M02(BM160)	E2M02(BN160)	A3B02(WK220)	B3B02(WK230)	H1G03	D1G03	F1J03	B1J03	Bus In Bit P
	M2J06(BR190)	M2J07(BR190)	A3D13(WK220)	B3D13(WK230)	H1J13	D1J13	F1G13	B1G13	Sync In
	M2U07(BR170)	M2M05(BR180)	A2B02(WK220)	B2B02(WK230)	G1G03	C1G03	E1J03	A1J03	Select Active
M2U09(BR130)	M2P07(BR180)	M2P07(BR180)	A2B05(WK220)	B2B05(WK230)	G1G05	C1G05	E1J05	A1J05	Normal End
M2S09(BR130)	M2G10(BR170)	M2G02(BR180)	A2D06(WK220)	B2D06(WK230)	G1J06	C1J06	E1G06	A1G06	Check End
	M2U05(BR170)	M2P04(BR180)	A2D05(WK220)	B2D05(WK230)	G1J04	C1J04	E1G04	A1G04	Tag Valid
M2U06(BR130)	M2J03(BR170)	M2G04(BR180)	A2B08/B09(WK220) 1	B2B09/B10(WK230) 1	G1G08	C1G08	E1J08	A1J08	Error Alert
	M2S12(BR170)	M2P13(BR180)	A2D09/D10(WK220) 1	B2D09/D10(WK230) 1	G1J09	C1J09	E1G09	A1G09	Index Alert
M2B04(BR130)	M2D09(BR170)	M2B13(BR180)	A2B12(WK220)	B2B12(WK230)	G1G12	C1G12	E1J12	A1J12	CE Alert

Note: *Pin numbers do not appear on WK220 or WK230. See ALD pages indicated in the columns to the left for the appropriate interface or the chart on ZA090 for pin identification.*

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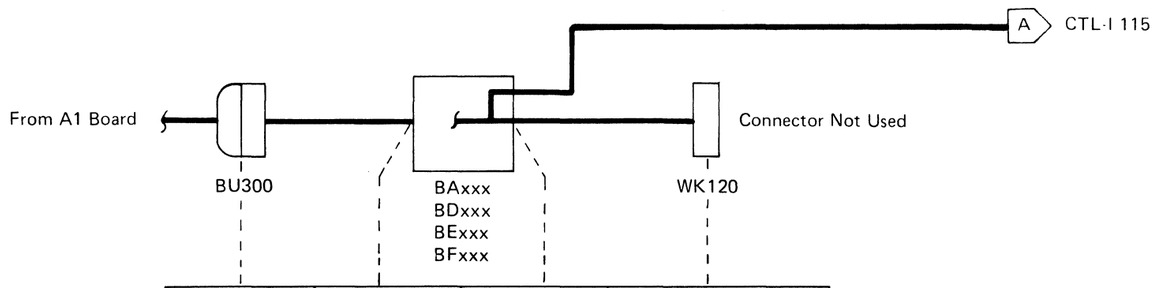
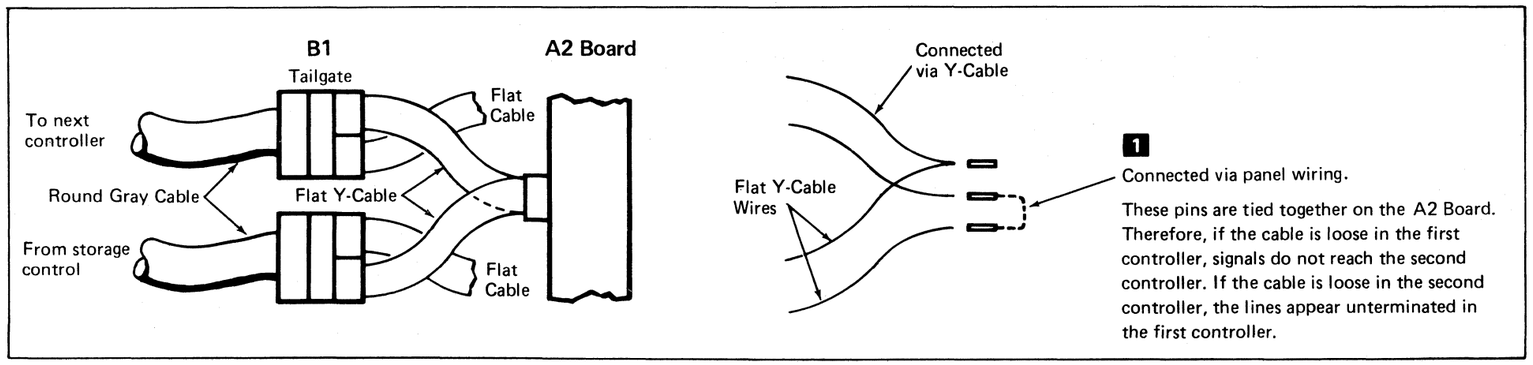
INTERFACE CONNECTOR DIAGRAM (With String Switch)

BUS IN/TAG IN

All interface lines and pins are NPL levels. All logic lines and pins are MST levels. See CTL-I section divider tab for signal levels.



	A2	A2	A2	A2	
Bus In Bit 0	V4B02(BU300)	F2B10(BA160)	F2D06(BA150)	C3D05(WK120)	Bus In Bit 0
1	V4B04(BU300)	F2B07(BA160)	F2B03(BA150)	C3B05(WK120)	1
2	V4B05(BU300)	F2G03(BA160)	F2D10(BA150)	C3D06(WK120)	2
3	V4B06(BU300)	F2B09(BA160)	F2D09(BA150)	C3B08/B09(WK120) 1	3
4	V4B08(BU300)	F2G12(BA160)	F2J02(BA150)	C3D09/D10(WK120) 1	4
5	V4B09(BU300	F2J04(BA160)	F2J07(BA150)	C3B10(WK120)	5
6	V4B10(BU300)	F2G05(BA160)	F2J11(BA150)	C3D11(WK120)	6
7	V4B12(BU300)	F2G13(BA160)	F2J03(BA150)	C3B12(WK120)	7
Bus In Bit P	V4B13(BU300)	F2J13(BA160)	F2J12(BA150)	C3B02(WK120)	Bus In Bit P
Sync In	–	–	K2D04(BE160)	C3D13(WK120)	Sync In
Select Active	–	–	K2J03(BE160)	C2B02(WK120)	Select Active
Normal End	–	–	K2D11(BE160)	C2B05(WK120)	Normal End
Check End	–	–	K2D05(BE160)	C2D08(WK120)	Check End
Tag Valid	V5D13(BU300)	G2S07(BF160)	K2G05(BE160)	C2D05(WK120)	Tag Valid
Error Alert	–	–	L2B09(BD230)	C2B08/B09(WK120) 1	Error Alert
Index Alert	–	–	K2B05(BE160)	C2D09/D10(WK120) 1	Index Alert
CE Alert	–	–	L2J05(BD230)	C2B12(WK120)	CE Alert



1

Connected via panel wiring.

These pins are tied together on the A2 Board. Therefore, if the cable is loose in the first controller, signals do not reach the second controller. If the cable is loose in the second controller, the lines appear unterminated in the first controller.

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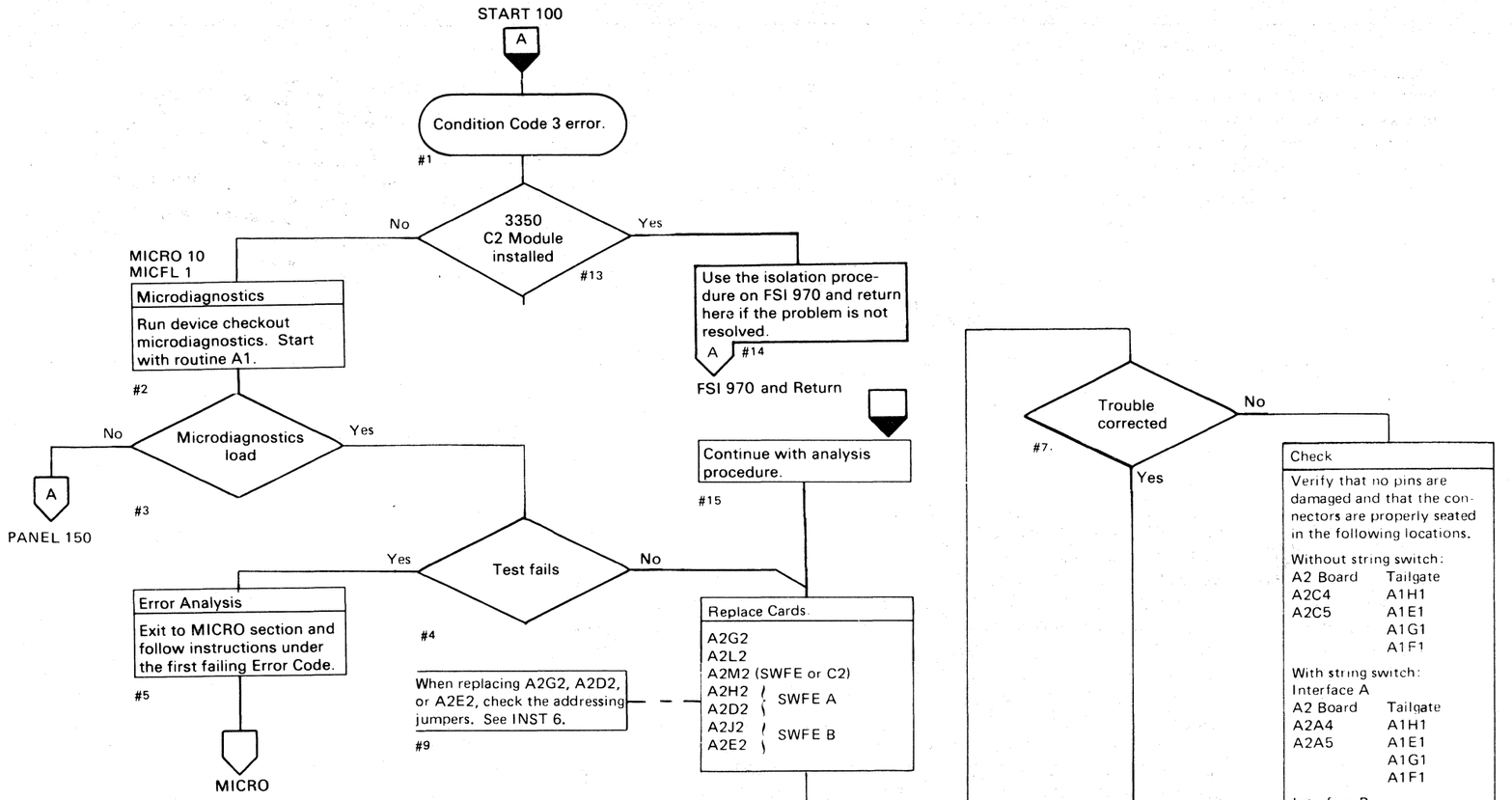
CONDITION CODE 3 ERRORS



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CONDITION CODE 3 ERRORS

Circuit Description

Condition Code 3 errors are caused by:

Active Outbus bit (A)

Erroneous Tag Bus bit (B)

Inactive Tag Bus or Select Hold (C)

Condition Code 3 errors normally prevent controller selection and the microdiagnostics fail to load properly.

Controller selection requires the following:

Select Hold
Valid Tag Gate
Tag '03'
Online (If C2 Module is installed.)

Valid Tag Gate becomes active if there is no Bus Out Parity or Tag Bus Parity check.

See OPER 90 for additional theory.

Analysis Procedure

Three microdiagnostic tests in routine A1 may be looped to help determine the cause of the failure:

- Test 2 exercises the select circuits (C) by issuing Tag '03' (Select Controller) and Tag '09' (Reset Controller).
  See CTL-I 252 for more detail.
- Test 3 exercises the outbus bits (A) and forces Tag Bus Parity and Bus Out Parity check.
  See CTL-I 304 for more detail.
- Test 4 exercises the Tag Bus bits (B) and issues all tags and checks for Tag Valid.

1. Loop the appropriate test:

   Load routine A1
   Enter 10,xx,00
   XX = Selected test number

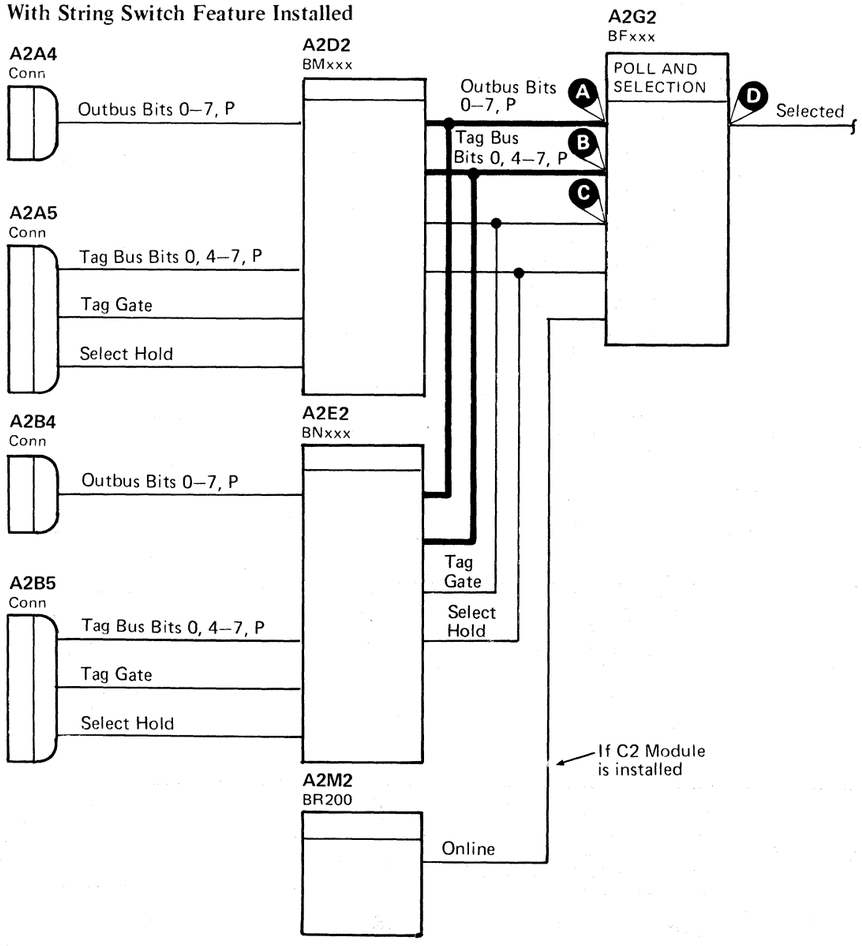
2. Scope setup:

   Sweep 20 μs/div.
   Trigger
   Slope (+)
   A2G2B12
   (+Select Hold NPL)
   Ch 1 A2G2J05
   (−Selected)

Additional Service Hints

1. Check the −4 V and +6 V for a stable and proper level. See PWR 90, Entry B for procedure.
   Note: *Adjusting the −4 V or +6 V regulators out-of-spec can cause an intermittent failure to become less intermittent.*
2. Check the backpanel wiring for tight wire wraps. See Figure 1 for wire net locations.
3. Check connectors for shorts or broken land patterns. See Figure 1 for connector pin locations.

With String Switch Feature Installed



Without String Switch Feature Installed

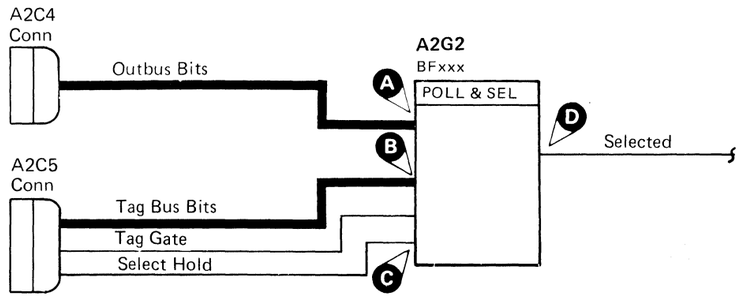


Figure 1. Pin Locations

Line Name	Conn A2C4, A2A4, and A2B4 Pins	Card A2G2 Pins (A)	SWFE Card A2D2, A2E2
+NPL Outbus Bit 0	D05	G12	G11
+NPL Outbus Bit 1	B05	G13	J11
+NPL Outbus Bit 2	D06	P02	J05
+NPL Outbus Bit 3	B08/B09	M03	J04
+NPL Outbus Bit 4	D09/D10	M04	J03
+NPL Outbus Bit 5	B10	M07	D07
+NPL Outbus Bit 6	D11	M09	G03
+NPL Outbus Bit 7	B12	P10	G04
+NPL Outbus Bit P	B02	P09	G05
	Conn A2C5, A2A5, and A2B5 Pins	**Card A2G2 Pins (B)**	**SWFE Card A2D2, A2E2**
+NPL Tag Bus Bit 0	B02	D13	B07
+NPL Tag Bus Bit 4	B05	G02	G12
+NPL Tag Bus Bit 5	D05	B03	D09
+NPL Tag Bus Bit 6	B08/B09	B05	D10
+NPL Tag Bus Bit 7	D06	D04	B09
+NPL Tag Bus Bit P	D09/D10	B04	D11
	Conn A2C5, A2A5, and A2B5 Pins	**Card A2G2 Pins (C)**	**SWFE Card A2D2, A2E2**
+Select Hold NPL	D11	B12	J12
+Tag Gate	B10	J11	D06
		Card A2G2 Pins (D)	**SWFE Card A2D2, A2E2**
−Selected		J05	M08

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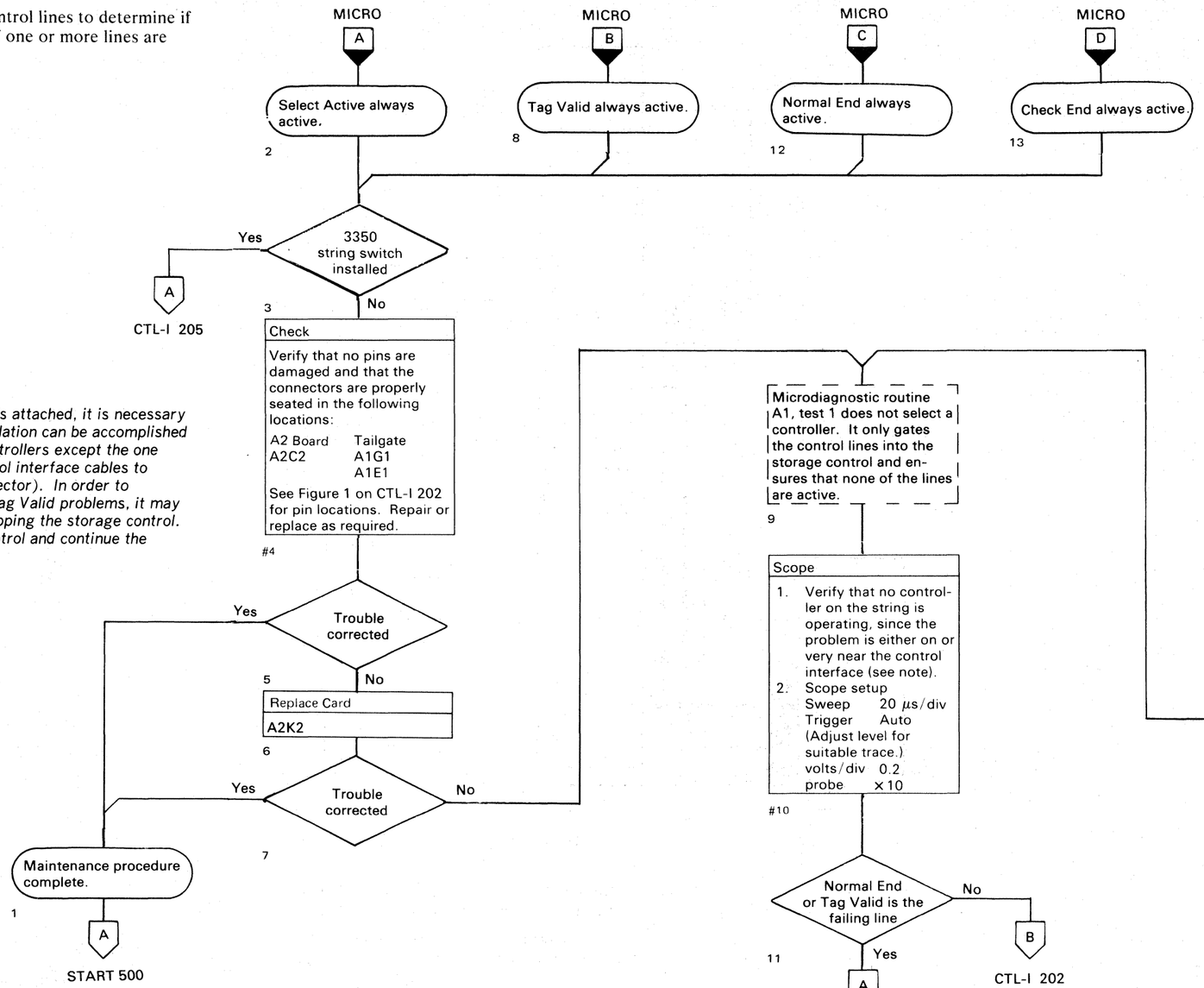
ALWAYS ACTIVE LINES

The microdiagnostics test the control lines to determine if they are off prior to selection. If one or more lines are on, an error is indicated.

Note: *If more than one controller is attached, it is necessary to isolate to a single controller. Isolation can be accomplished by either removing power to all controllers except the one being tested, or removing the control interface cables to succeeding controllers (A1E1 connector). In order to properly analyze Normal End and Tag Valid problems, it may be necessary to stop polling by stopping the storage control. When feasible, stop the storage control and continue the analysis.*



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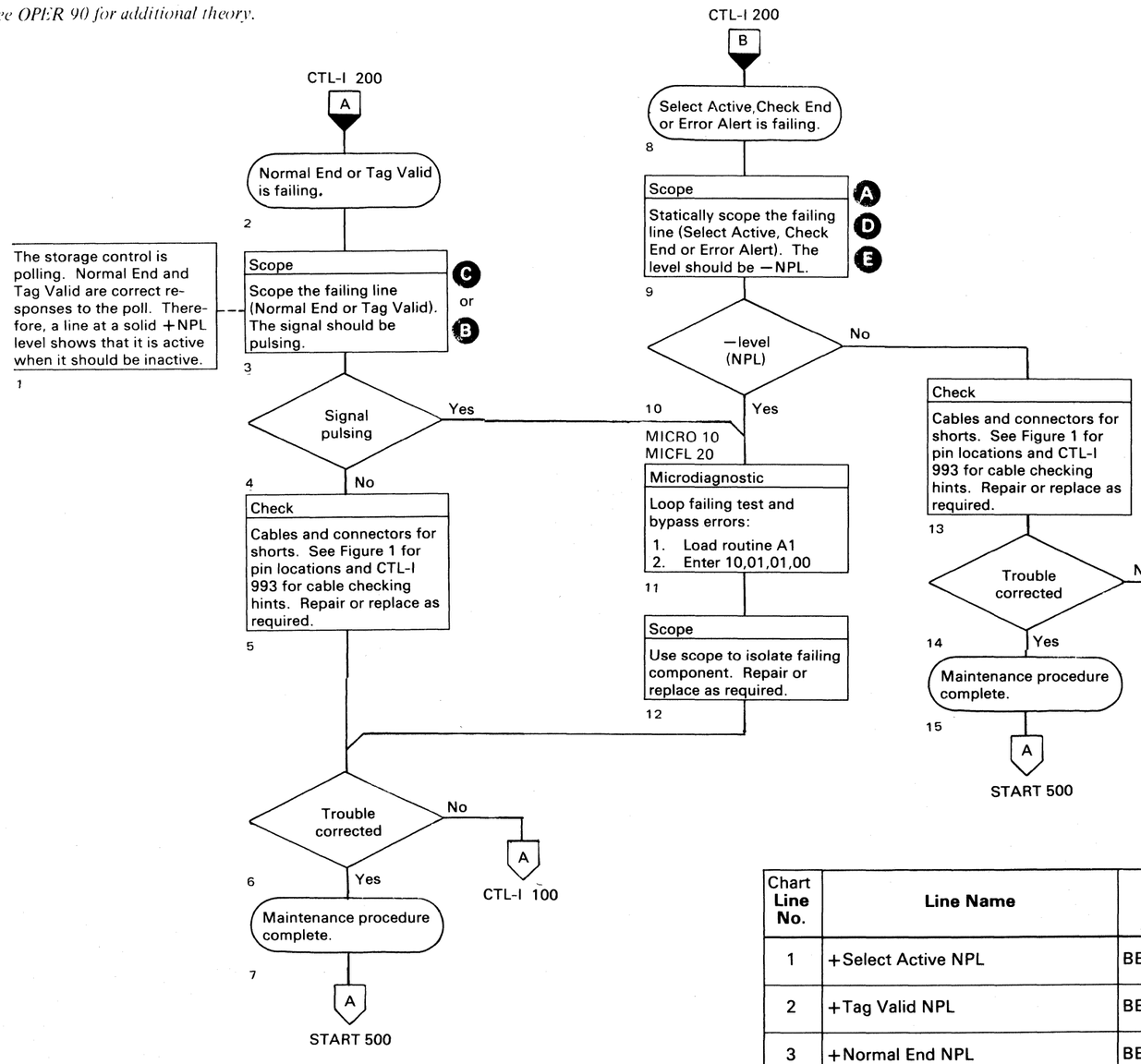
ALWAYS ACTIVE LINES

See OPER 90 for additional theory.



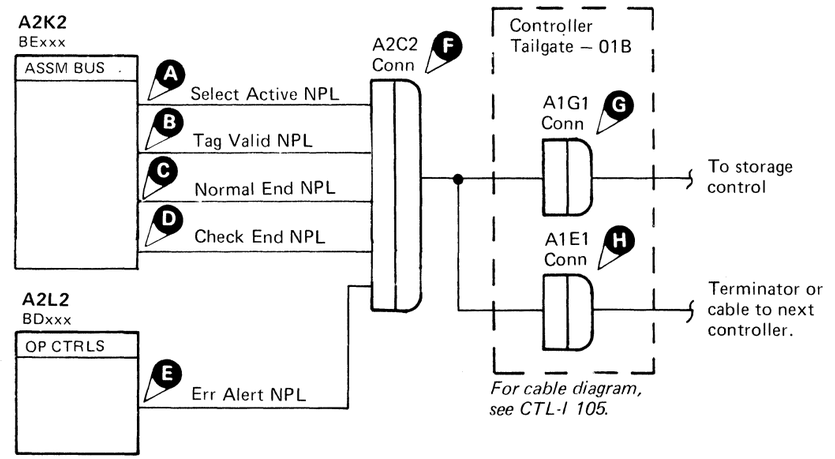


Figure 1. Connector Pin Locations

Line Name	Conn A2C2 Pins (F)	Conn A1G1 Pins (G)	Conn A1E1 Pins (H)
+Select Active NPL	B02	G03	G03
+Tag Valid NPL	D05	J04	J04
+Normal End NPL	B05	G05	G05
+Check End NPL	D05	J06	J06
+Err Alert NPL	B09	G08	G08

Legend: Inactive; Active level; Tolerance

Chart Line No.	Line Name	ALD	Test Point		
1	+Select Active NPL	BE160	A2K2 J03	A	
2	+Tag Valid NPL	BE160	A2K2 G05	B	
3	+Normal End NPL	BE160	A2K2 D11	C	
4	+Check End NPL	BE160	A2K2 D05	D	Inactive
5	+Err Alert NPL	BD230	A2L2 B09	E	Inactive

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ALWAYS ACTIVE LINES (With String Switch)

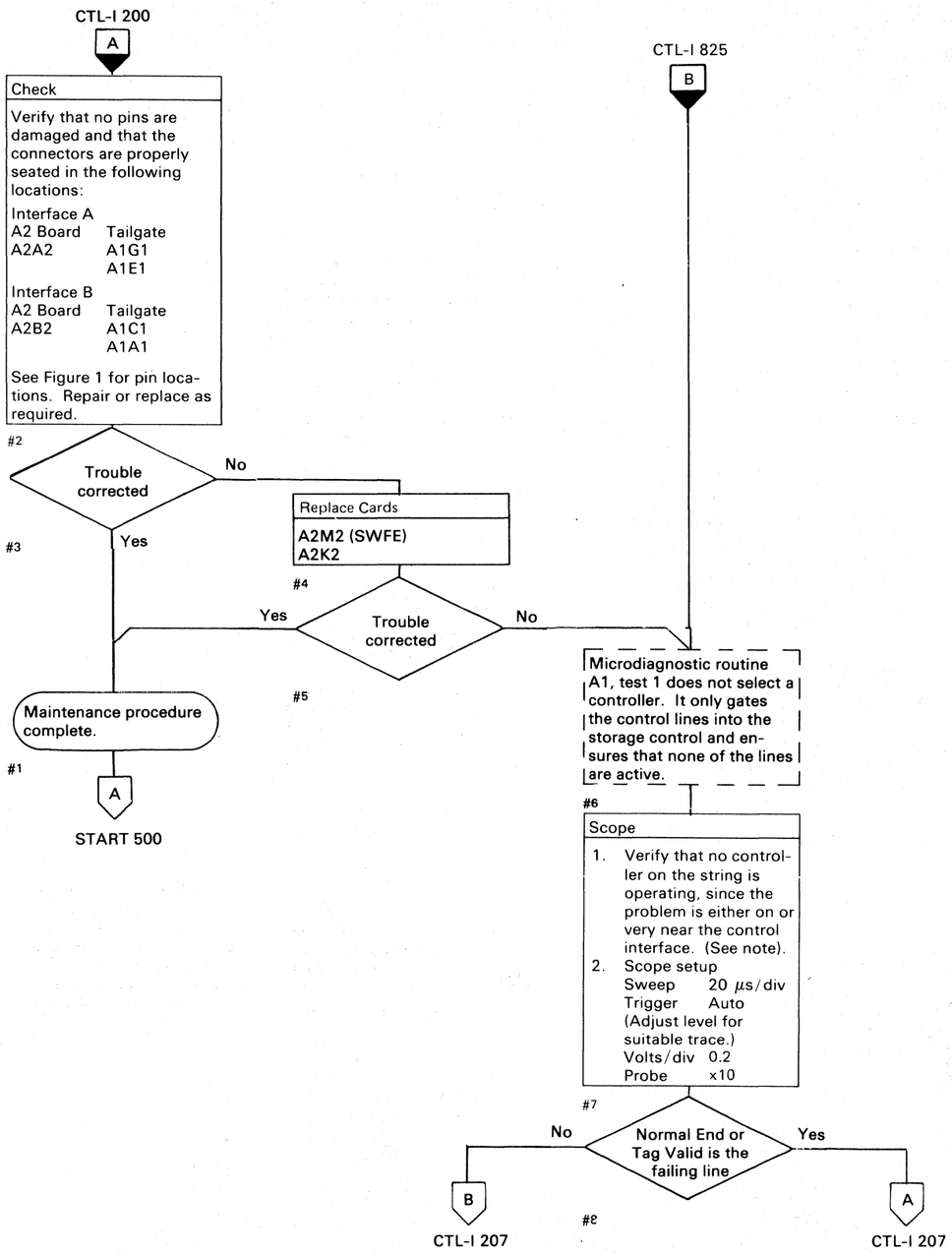

Figure 1. Pin Locations

Line Name	Conn A2A2 Pins (E)	Conn A1G1 Pins (G)	Conn A1E1 Pins (H)
+Select Active A NPL	B02	G03	G03
+Tag Valid A NPL	D05	J04	J04
+Normal End A NPL	B05	G05	G05
+Check End A NPL	D06	J06	J06
+Error Alert A NPL	B08/B09	G08	G08
	Conn A2B2 Pins (F)	**Conn A1C1 Pins (J)**	**Conn A1A1 Pins (K)**
+Select Active B NPL	B02	G03	G03
+Tag Valid B NPL	D05	J04	J04
+Normal End B NPL	B05	G05	C05
+Check End B NPL	D06	J06	J06
+Error Alert B NPL	B08/B09	G08	G08

Note: *If more than one controller is attached, it is necessary to isolate to a single controller. Isolation can be accomplished by either removing power to all controllers except the one being tested, or removing the control interface cables to succeeding controllers (A1E1 and A1A1 connectors). In order to properly analyze Normal End and Tag Valid problems, it may be necessary to stop polling by stopping the storage control. When feasible, stop the storage control and continue the analysis.*

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ALWAYS ACTIVE LINES (With String Switch)

See OPER 90 and OPER 260 for theory.

The storage control is polling. Normal End and Tag Valid are correct responses to the poll. Therefore, a line at a solid +NPL level is an indication of a line being active when it should be inactive.
1

CTL-I 205 A

Normal End or Tag Valid is failing.
2

Scope
Scope the failing line (Normal End or Tag Valid). The signal should be pulsing.
C or D
3

Signal pulsing
Yes
No
4

Check
Cables and connectors for shorts. See Figure 1 on CTL-I 205 for pin locations and CTL-I 993 for cable checking hints. Repair or replace as required.
5

Trouble corrected
No
A CTL-I 100
Yes
6

Maintenance procedure complete.
12
A START 500

CTL-I 205 B

Select Active, Check End or Error Alert is failing.
7

Scope
Statically scope the failing line (Select Active, Check End or Error Alert). The level should be −NPL.
C or D
8

−level (NPL)
No
Yes
9

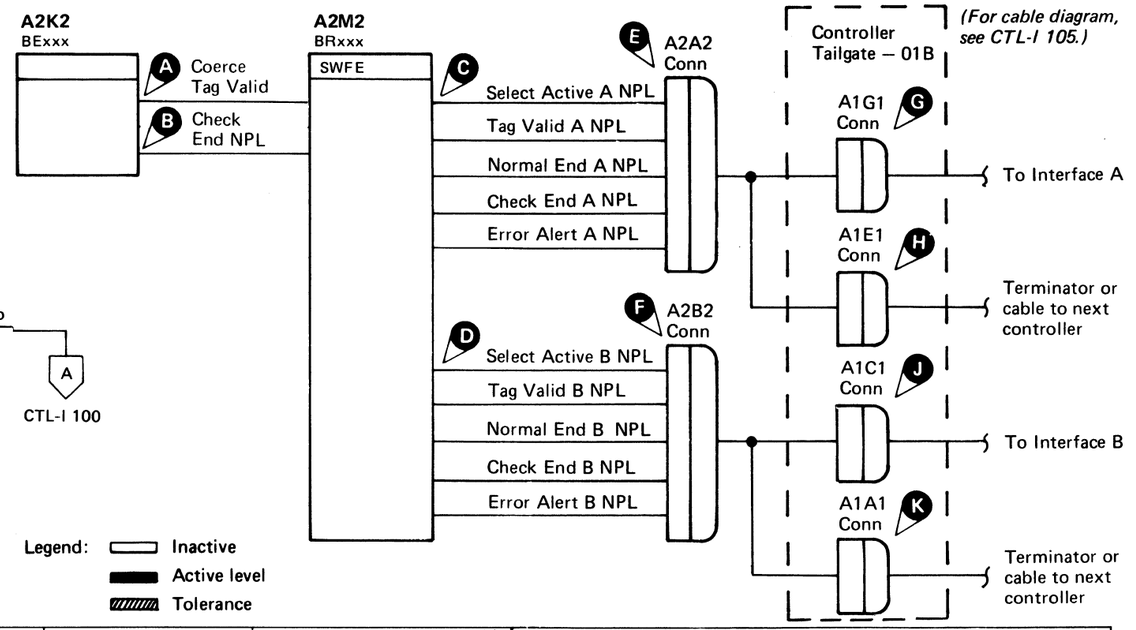
MICRO 10
MICFL 20
Microdiagnostic
Loop failing test and bypass errors:
1. Load routine A1
2. Enter 10,01,01,00
10

Scope
Use scope to isolate failing component. Repair or replace as required.
11

Check
Cables and connectors for shorts. See Figure 1 on CTL-I 205 for pin locations and CTL-I 993 for cable checking hints. Repair or replace as required.
13

Trouble corrected
No
A CTL-I 100
Yes
14

Maintenance procedure complete.
15
A START 500



(For cable diagram, see CTL-I 105.)

Chart Line No.	Line Name	ALD	Test Point		
1	+Select Active A NPL	BR170	A2M2 U07	C	
2	+Tag Valid A NPL	BR170	A2M2 U05		
3	+Normal End A NPL	BR170	A2M2 U13		
4	+Check End A NPL	BR170	A2M2 G10		Inactive
5	+Error Alert A NPL	BR170	A2M2 J03		Inactive
6	+Select Active B NPL	BR180	A2M2 M05	D	
7	+Tag Valid B NPL	BR180	A2M2 P04		
8	+Normal End B NPL	BR180	A2M2 P07		
9	+Check End B NPL	BR180	A2M2 G02		Inactive
10	+Error Alert B NPL	BR180	A2M2 G04		Inactive
11	+Check End NPL	BR130	A2M2 S09	B	Inactive
12	−Coerce Tag Valid	BR150	A2M2 S05	A	

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MULTIPLE CONTROLLER CHECKOUT PROCEDURE

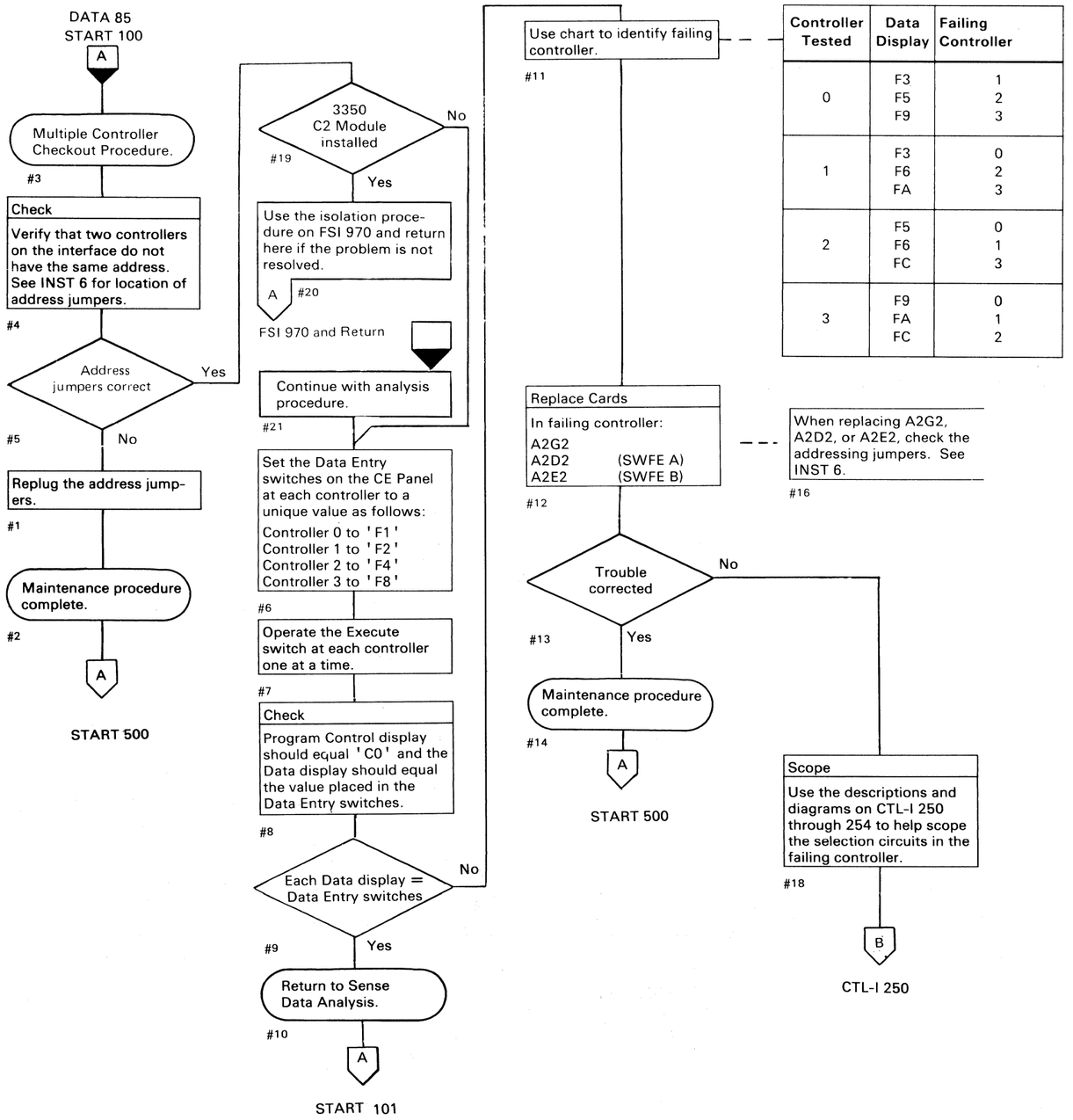
When two controllers with the same address respond to selection on the same storage control, their responses are identical. It is impossible for the storage control to determine if more than one controller responded. Only on subsequent operations, where different responses are possible, is the condition detected.

Examples of errors that might be expected with multiple controllers selected are:

Storage control detected Bus In Parity errors.

Head Switch Timer Expired check.

This procedure establishes controller conditions that enable the failing unit to be isolated.



Controller Tested	Data Display	Failing Controller
0	F3 F5 F9	1 2 3
1	F3 F6 FA	0 2 3
2	F5 F6 FC	0 1 3
3	F9 FA FC	0 1 2

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CONTROLLER SELECTION FAILURE

Microdiagnostic routine A1 selects the controller Tag '03' (Select Controller). The controller responds with 3 bits active on Control Bus In:

Bits 0,1,2 contain the controller address
Bits 5,6,7 contain the complement.

Routine A1 then checks the validity of this 3-of-6 code.

Controller Address	Message Byte 3 Bits 0123 4567	Hex Value
0	000--111	07
1	001--110	26
2	010--101	45
3	011--100	64
The controller address is determined by jumpers on the A2G2 card. See INST 6 for jumper locations.		

If the C2 Module is installed, the controller responds with 4 bits active on the Control Bus In:

Bit 0 indicates the status of the controller being addressed.
- Bit 0 = 1 Offline controller addressed.
- Bit 0 = 0 Online controller addressed.

Bit 4 indicates the A2 or C2 controller addressed.
- Bit 4 = 1 C2 controller addressed.
- Bit 4 = 0 A2 controller addressed.

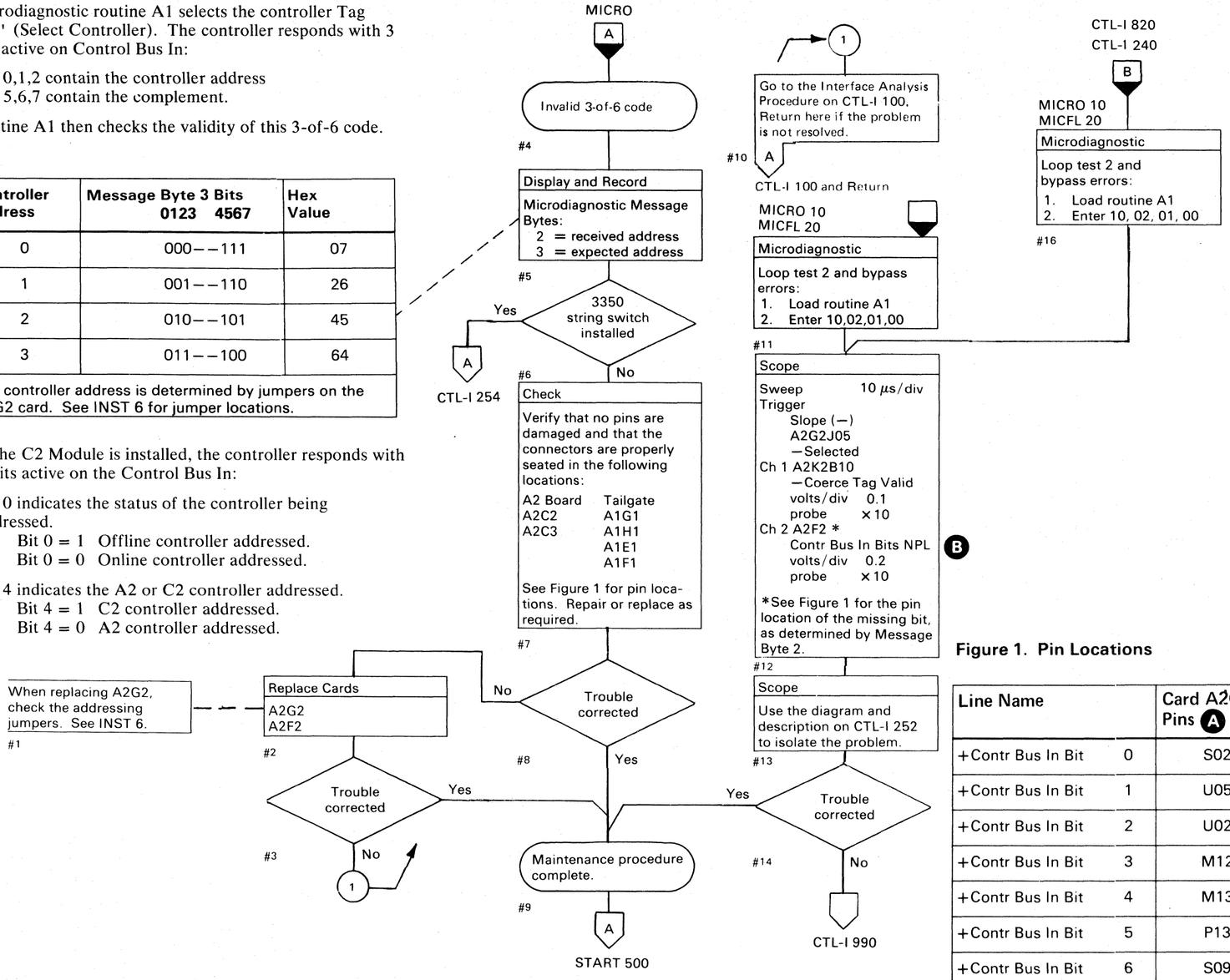

Figure 1. Pin Locations

Line Name		Card A2G2 Pins A	Card A2F2 Pins G	Card A2F2 Pins B	Conn A2C3 Pins C	Conn A1H1 Pins D	Conn A1F1 Pins E
+Contr Bus In Bit	0	S02	P05	D06	D05	J04	J04
+Contr Bus In Bit	1	U05	M10	B03	B05	G05	G05
+Contr Bus In Bit	2	U02	M08	D10	D06	J06	J06
+Contr Bus In Bit	3	M12	S07	D09	B09	G08	G08
+Contr Bus In Bit	4	M13	P06	J02	D10	J09	J09
+Contr Bus In Bit	5	P13	U03	J07	B10	G10	G10
+Contr Bus In Bit	6	S09	P09	J11	D11	J11	J11
+Contr Bus In Bit	7	U13	U06	J03	B12	G12	G12
+Contr Bus In Bit	P	G08		J12	B02	G03	G03

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CONTROLLER SELECTION FAILURE

Circuit Description

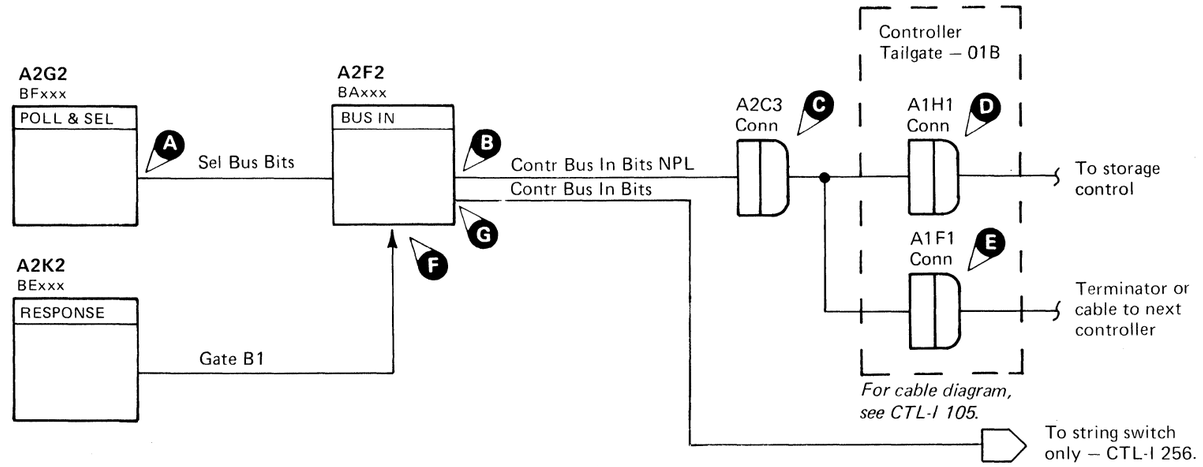
The 3-of-6 code is generated by Sel Bus Bits (A).

Sel Bus Bits (A) becomes Contr Bus In Bits (G). Contr Bus In Bits activate Contr Bus In Bits NPL (B). Gate B1 (F) gates the Contr Bus In Bits NPL (B) to the storage control.

Analysis Procedure

Find the bit that is in error and scope it back (see Figure 1 on CTL-I 250).

See OPER 90 for additional theory.



Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

Legend: Inactive
Active level
Tolerance

Chart Line No.	Line Name	ALD	Test Point		A Controller is Selected with OP Code 03. / The Controller responds with 3 bits active on Control Bus In.
1	–Selected	BF120	A2G2 J05		
2	–Coerce Tag Valid	BE150	A2K2 B10		
3	+Contr Bus In Bits NPL	BA150	A2F2 (See Figure 1 on CTL-I 250 for pin locations)	B	
4	–Gate BI	BA150	A2F2 G11	F	

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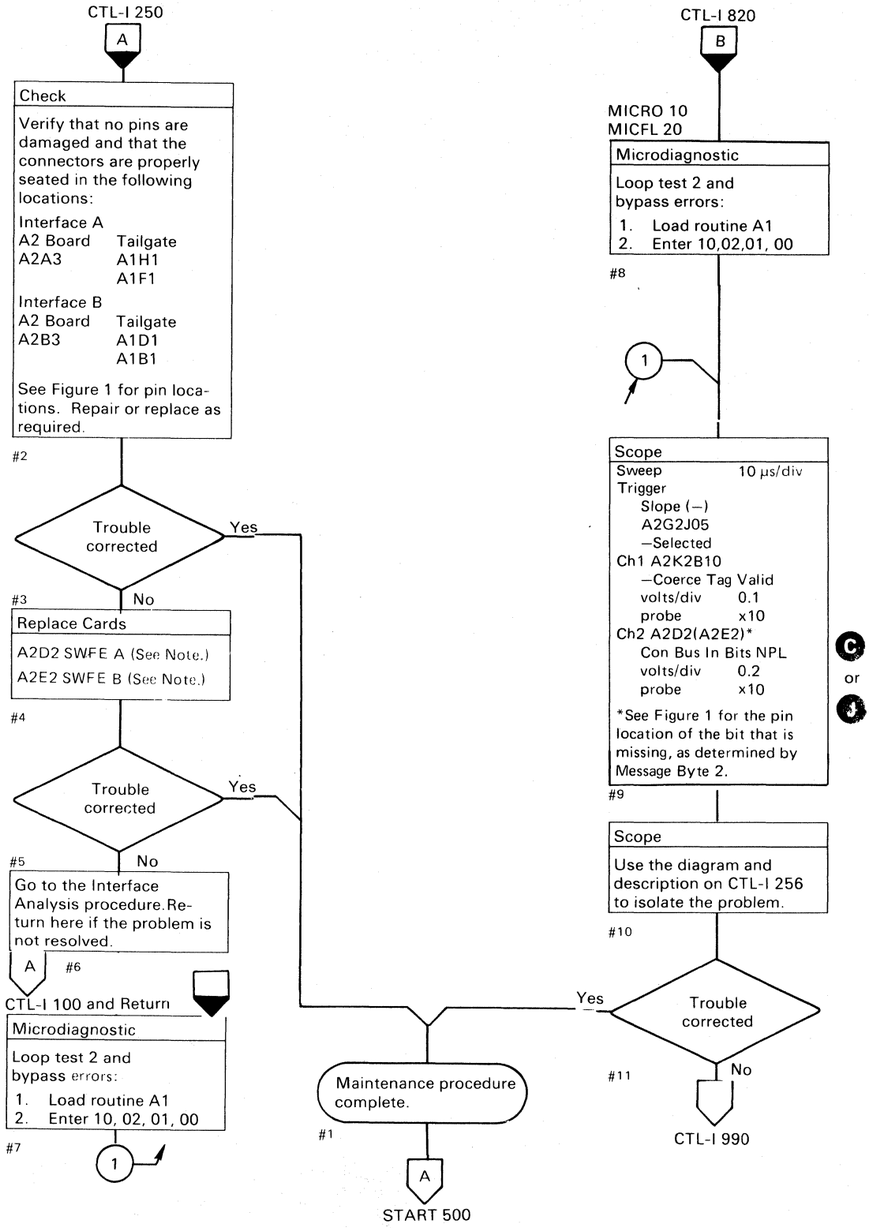
CONTROLLER SELECTION FAILURE (With String Switch)



Note: *When replacing A2D2 or A2E2, check the addressing jumpers. See INST 6.*

3350	BJ0252 Seq. 2 of 2	2358526 Part No.	441300 31 Mar 76	441303 30 Jul 76			

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Figure 1. Pin Locations

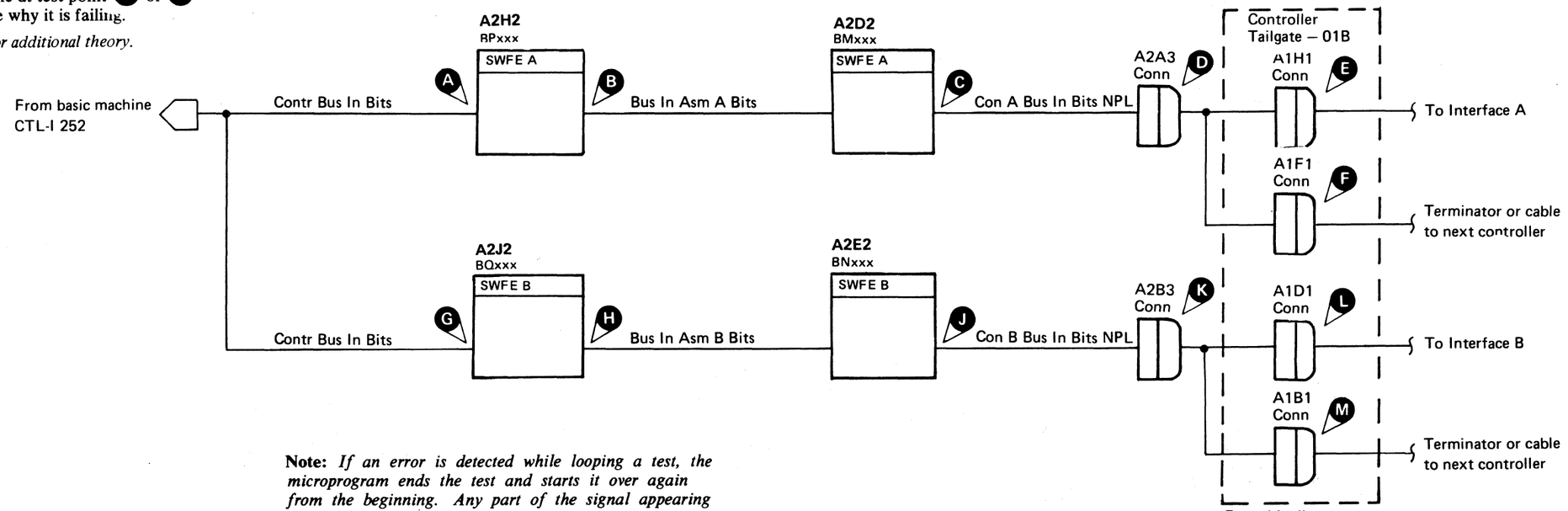
Line Name	Card A2D2 Pins C	Conn A2A3 Pins D	Conn A1H1 Pins E	Conn A1F1 Pins F	Card A2H2 Pins A	Card A2H2 Pins B
+Con A Bus In Bit 0	U06	D05	J04	J04	G02	G03
+Con A Bus In Bit 1	U07	B05	G05	G05	G05	J04
+Con A Bus In Bit 2	P11	D06	J06	J06	D11	B11
+Con A Bus In Bit 3	M12	B08/B09	G08	G08	D13	B13
+Con A Bus In Bit 4	S07	D09/D10	J09	J09	D06	B07
+Con A Bus In BIt 5	U09	B10	G10	G10	D10	B10
+Con A Bus In Bit 6	M11	D11	J11	J11	D02	B03
+Con A Bus In Bit 7	P12	B12	G12	G12	B05	B04
+Con A Bus In Bit P	M02	B02	G03	G03	G12	D12
	Card A2E2 Pins J	**Conn A2B3 Pins K**	**Conn A1D1 Pins L**	**Conn A1B1 Pins M**	**Card A2J2 Pins G**	**Card A2J2 Pins H**
+Con B Bus In Bit 0	U06	D05	J04	J04	G02	G03
+Con B Bus In Bit 1	U07	B05	G05	G05	G05	J04
+Con B Bus In Bit 2	P11	D06	J06	J06	D11	B11
+Con B Bus In Bit 3	M12	B08/B09	G08	G08	D13	B13
+Con B Bus In Bit 4	S07	D09/D10	J09	J09	D06	B07
+Con B Bus In Bit 5	U09	B10	G10	G10	D10	B10
+Con B Bus In Bit 6	M11	D11	J11	J11	D02	B03
+Con B Bus In Bit 7	P12	B12	G12	G12	B05	B04
+Con B Bus In Bit P	M02	B02	G03	G03	G12	D12

CONTROLLER SELECTION FAILURE (With String Switch)

Analysis Procedure

Start scoping the failing bit line at test point C or J and trace it back to determine why it is failing.

See OPER 90 and OPER 260 for additional theory.



For cable diagram, see CTL-I 105.

Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

Legend: Inactive / Active level / Tolerance

Chart Line No.	Line Name	ALD	Test Point		A Controller is Selected with OP Code 03. / The Controller responds with 3 bits active on CTL Bus In.
1	–Selected	BF120	A2G2 J05		
2	–Coerce Tag Valid	BE150	A2K2 B10		
3	+Con A Bus in Bits NPL	BM160	A2D2*	C	
4	+Con B Bus In Bits NPL	BN160	A2E2*	J	

**See Figure 1 on CTL-I 254 for pin locations.*

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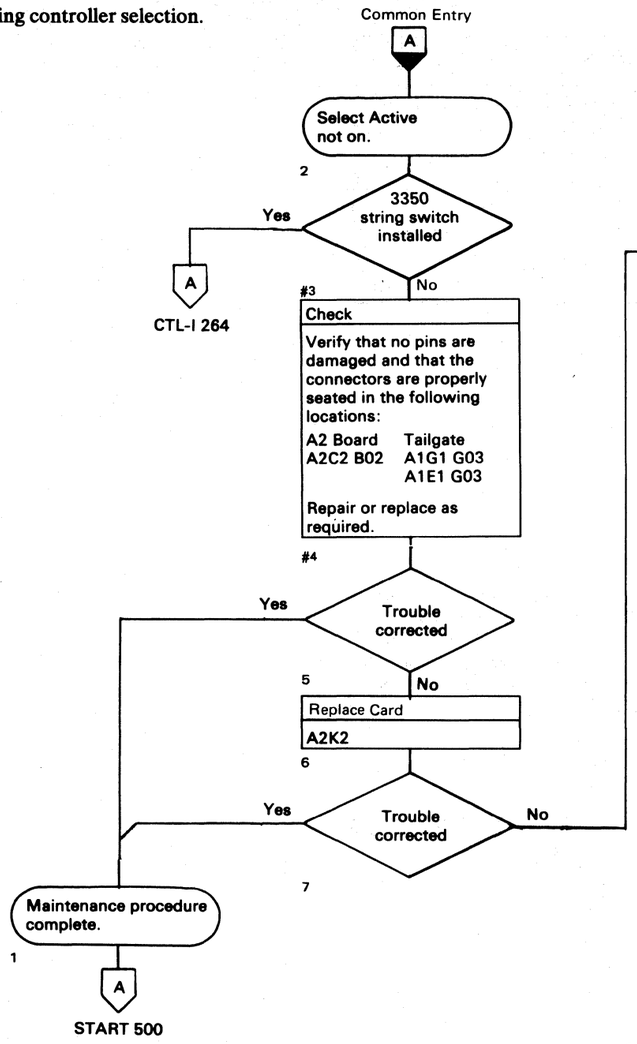
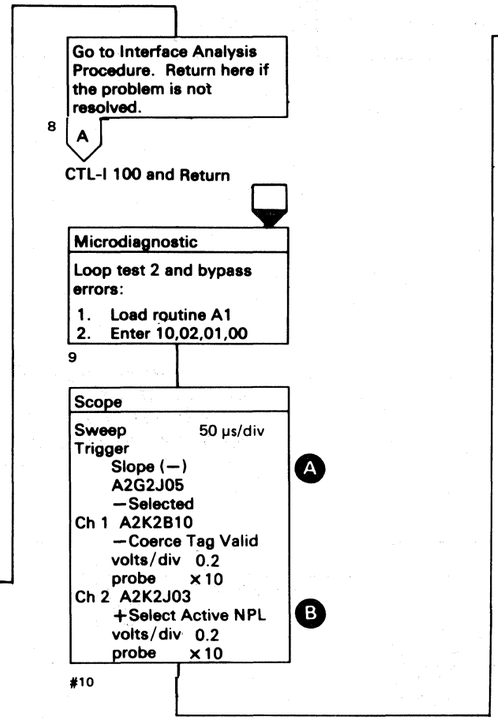
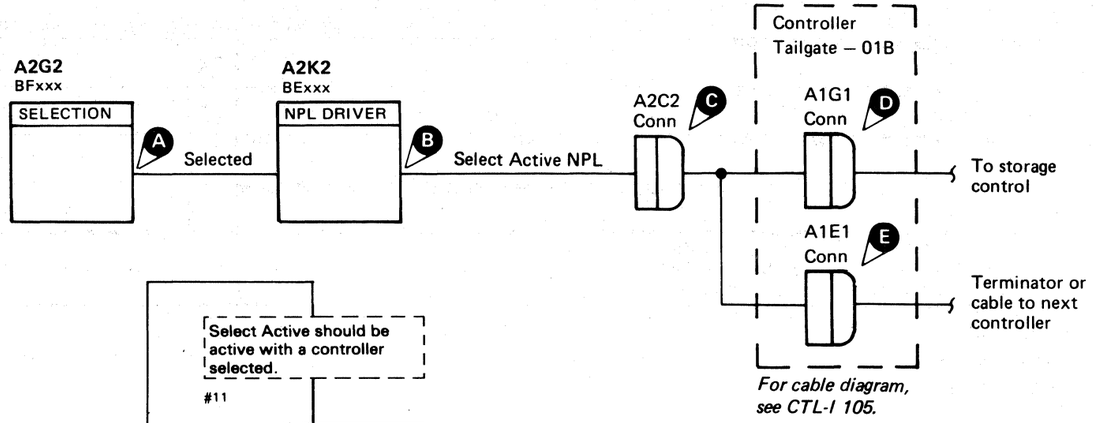
SELECT ACTIVE NOT ON

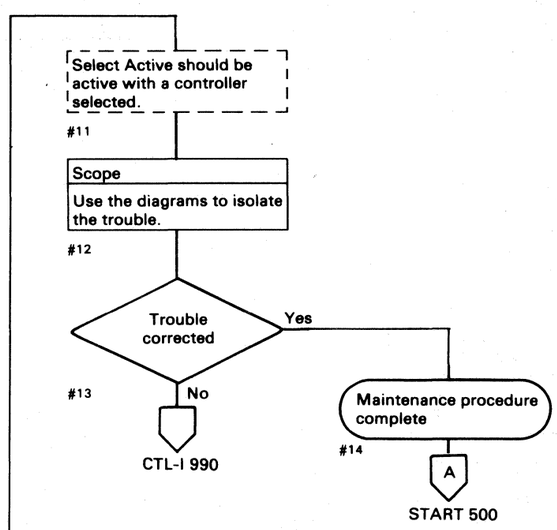
Select Active was off following controller selection.

See OPER 90 for theory.









Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point		Controller Selection
1	—Selected	BF120	A2G2 J05	A	
2	—Coerce Tag Valid	BE150	A2K2 B10		
3	+Select Active NPL	BE160	A2K2 J03	B	

Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

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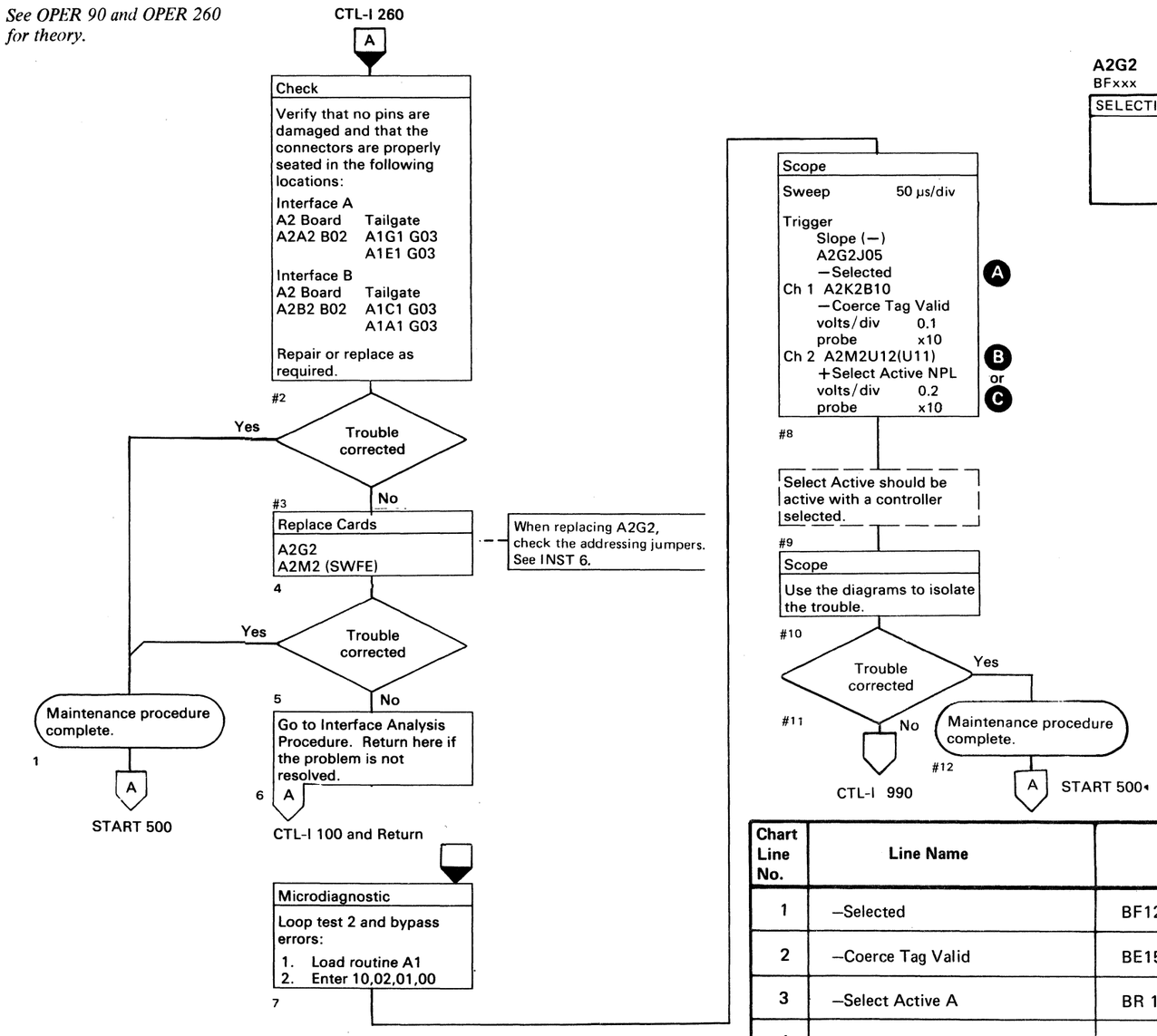
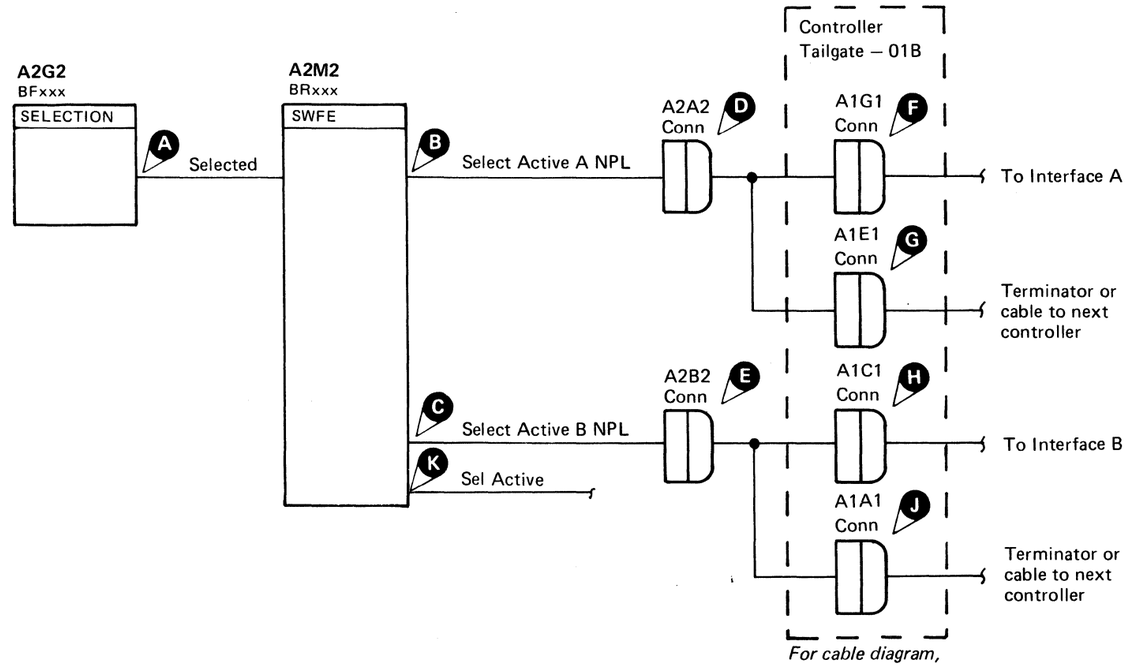
SELECT ACTIVE NOT ON (With String Switch)

See OPER 90 and OPER 260 for theory.





Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected and before the test is restarted is not valid.*

Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	—Selected	BF120	A2G2 J05	A
2	—Coerce Tag Valid	BE150	A2K2 B10	
3	—Select Active A	BR 150	A2M2 U12	K
4	+Select Active A NPL	BR170	A2M2 U07	B
5	—Select Active B	BR160	A2M2 U11	K
6	+Select Active B NPL	BR180	A2M2 M05	C

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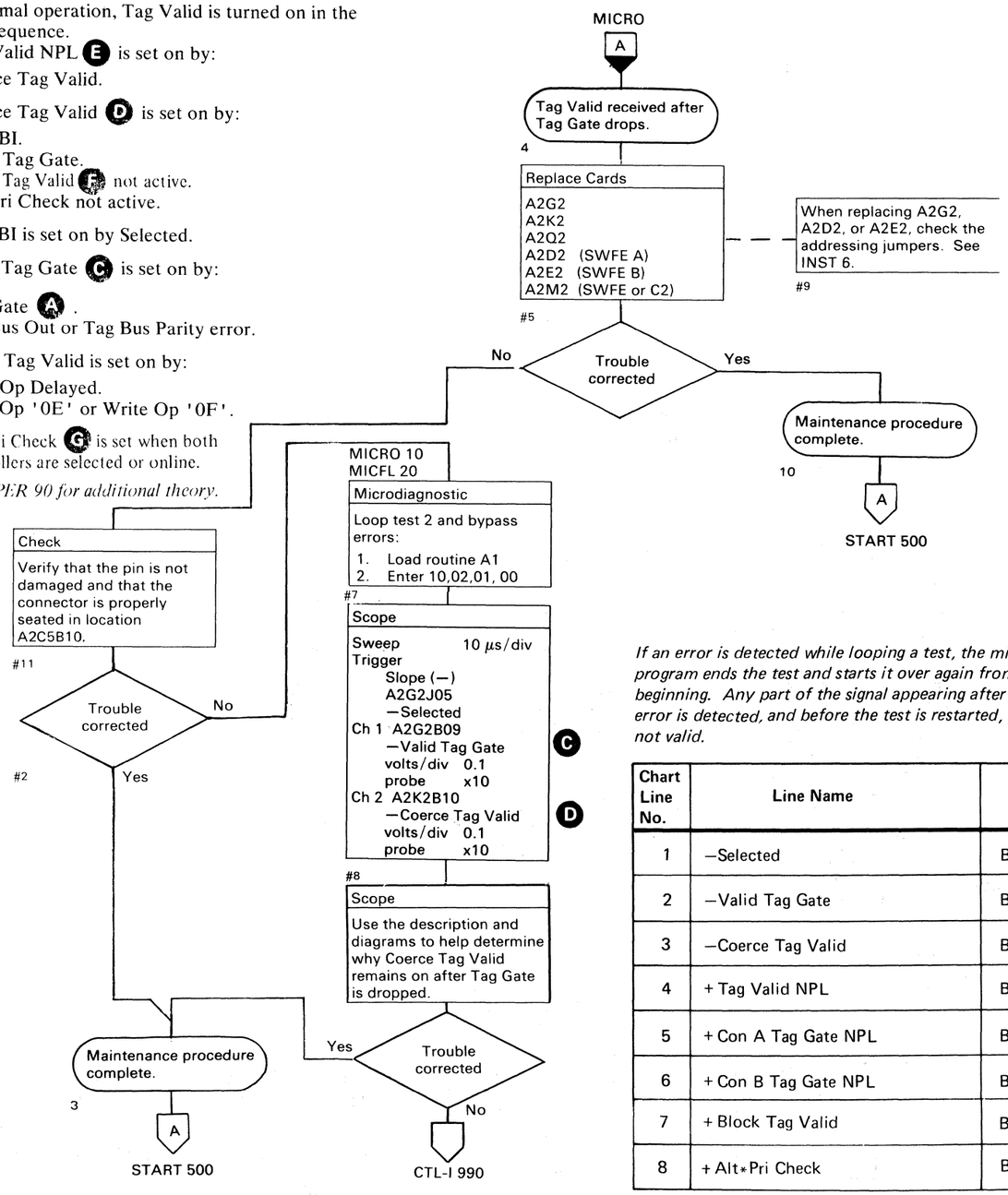
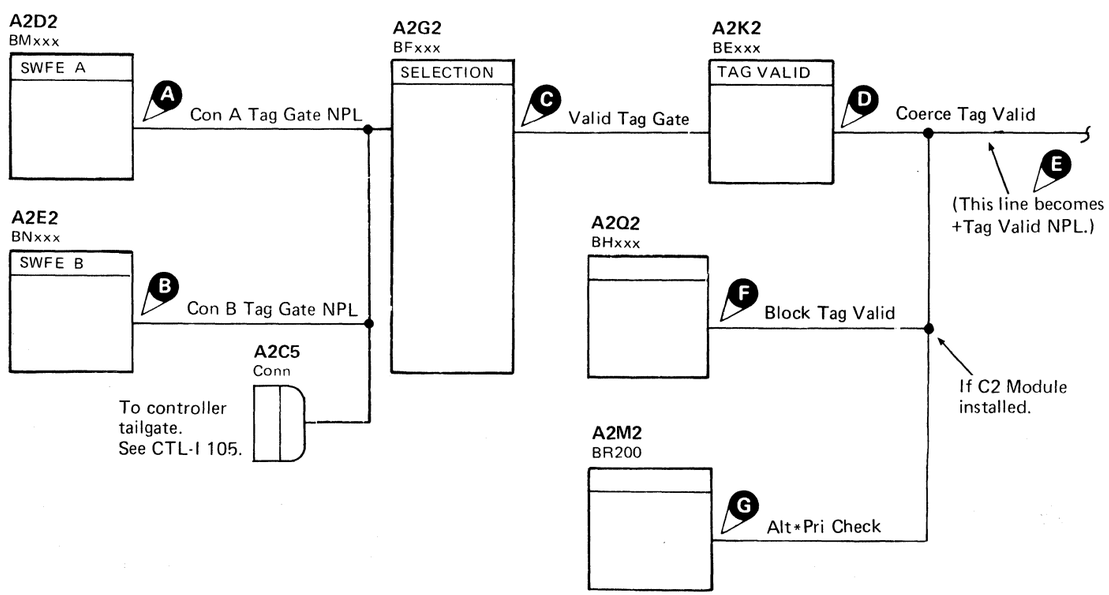
TAG VALID FAILURE

During normal operation, Tag Valid is turned on in the following sequence.

1. Tag Valid NPL (E) is set on by:
   Coerce Tag Valid.
2. Coerce Tag Valid (D) is set on by:
   Gate BI.
   Valid Tag Gate.
   Block Tag Valid (F) not active.
   Alt*Pri Check not active.
3. Gate BI is set on by Selected.
4. Valid Tag Gate (C) is set on by:
   Tag Gate (A).
   Not Bus Out or Tag Bus Parity error.
5. Block Tag Valid is set on by:
   R/W Op Delayed.
   Read Op '0E' or Write Op '0F'.
6. Alt*Pri Check (G) is set when both controllers are selected or online.

See OPER 90 for additional theory.





For circuit description of A2M2 card, see FSI 968.

If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.

Legend: Inactive / Active level / Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tag '03' Select / Tag '09' Transmit Control
1	—Selected	BF120	A2G2 J05		
2	—Valid Tag Gate	BF110	A2G2 B09	C	
3	—Coerce Tag Valid	BE150	A2K2 B10	D	
4	+ Tag Valid NPL	BE160	A2K2 G05	E	
5	+ Con A Tag Gate NPL	BM120	A2D2 G07	A	
6	+ Con B Tag Gate NPL	BN120	A2E2 G07	B	
7	+ Block Tag Valid	BH100	A2Q2 B09	F	
8	+ Alt*Pri Check	BR200	A2M2 S08	G	

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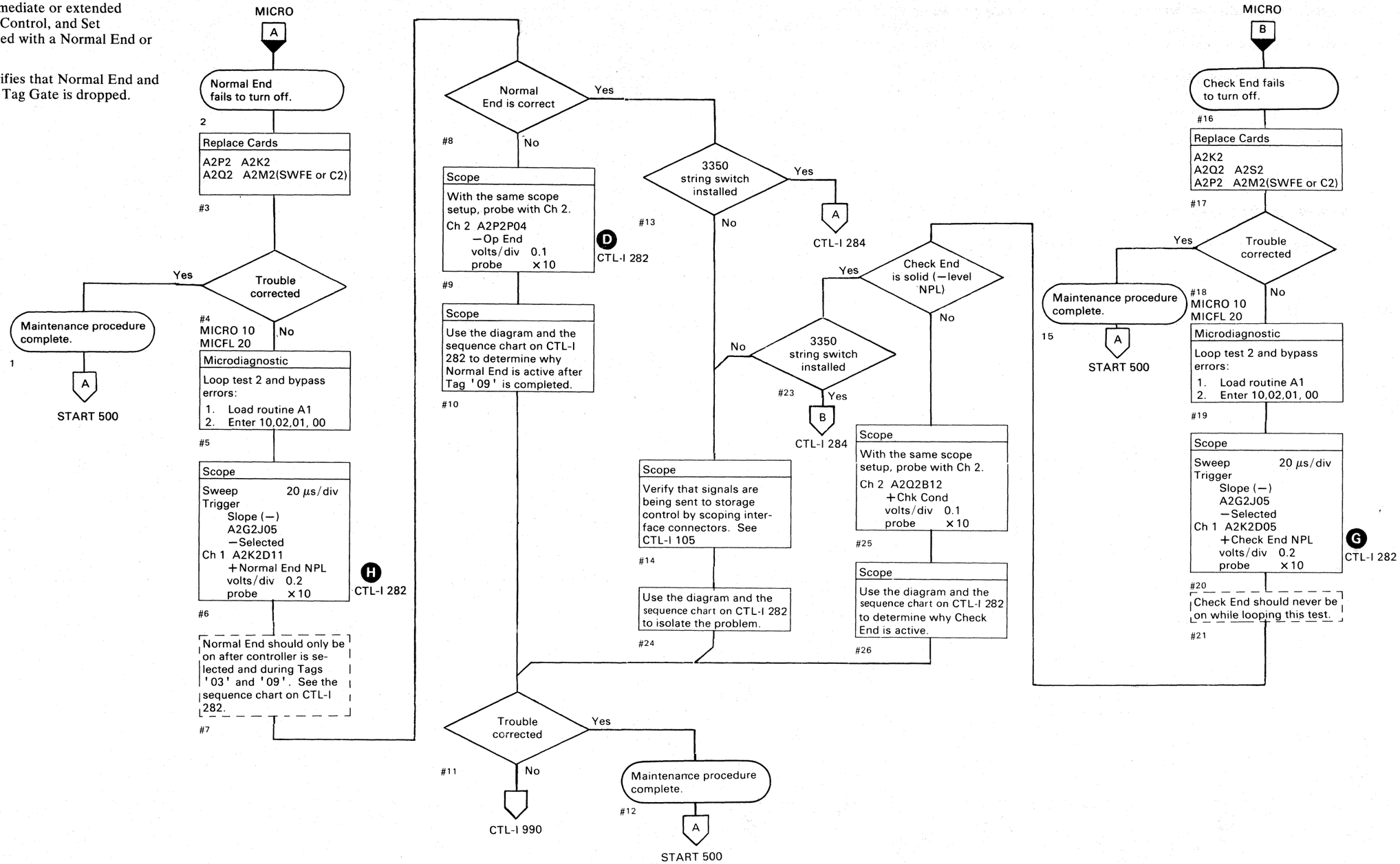
NORMAL END/CHECK END FAILURE

Each operation, whether an immediate or extended operations (Read, Write, ECC Control, and Set Read/Write), must be terminated with a Normal End or a Check End.

Microdiagnostic routine A1 verifies that Normal End and Check End are turned off after Tag Gate is dropped.



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NORMAL END/CHECK END FAILURE

Normal End

During normal operation:

Normal End is set by Coerce Tag Valid (K) and Imm Op (J) during this microdiagnostic test.

If Op End (D) is active, an error occurs.

Op End is set by End Data Op (F).

End Data Op is set by PLO End Op (C).

Check End

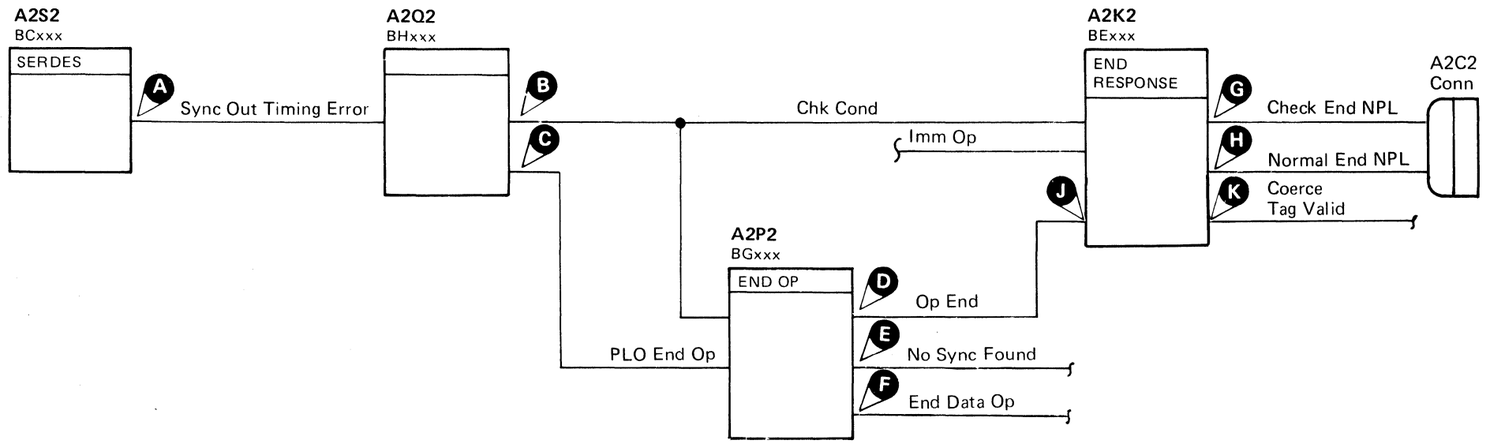
Check End should not be active during this test.

During normal operation:

Check End is set by Chk Cond (B).

Chk Cond is set by Sync Out Timing Error (A) or No Sync Found (E).

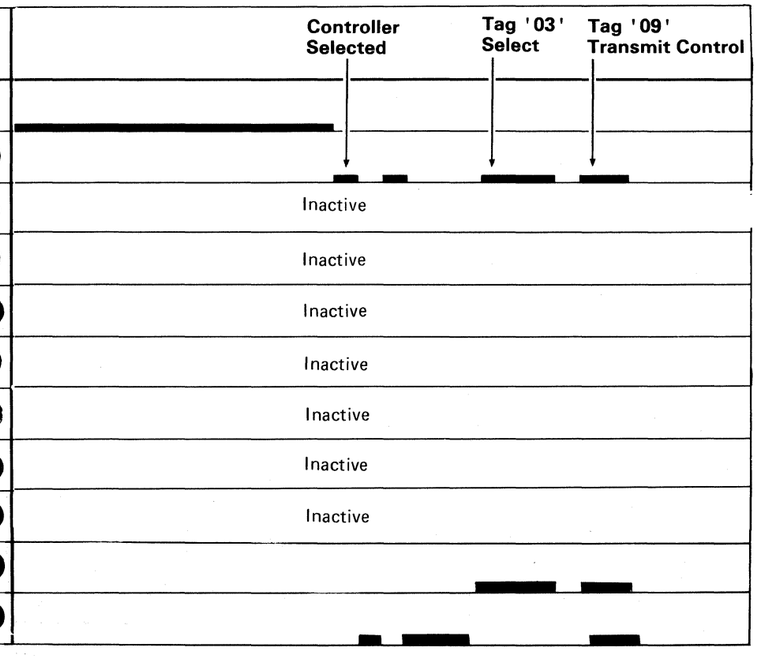
See OPER 90 for additional theory.



Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected and before the test is restarted is not valid.*

Legend: Inactive; Active level; Tolerance

Chart Line No.	Line Name	ALD	Test Point		
1	−Selected	BF120	A2G2 J05		
2	+Normal End NPL	BE160	A2K2 D11	H	
3	−Op End	BG170	A2P2 P04	D	
4	−End Data Op	BG170	A2P2 D10	F	
5	+PLO End Op	BH160	A2Q2 S12	C	
6	+Check End NPL	BE160	A2K2 D05	G	
7	+Chk Cond	BH150	A2Q2 B12	B	
8	−No Sync Found	BG140	A2P2 S04	E	
9	−Sync Out Timing Error	BC170	A2S2 U10	A	
10	−Imm Op	BE140	A2K2 B07	J	
11	−Coerce Tag Valid	BE140	A2K2 B10	K	



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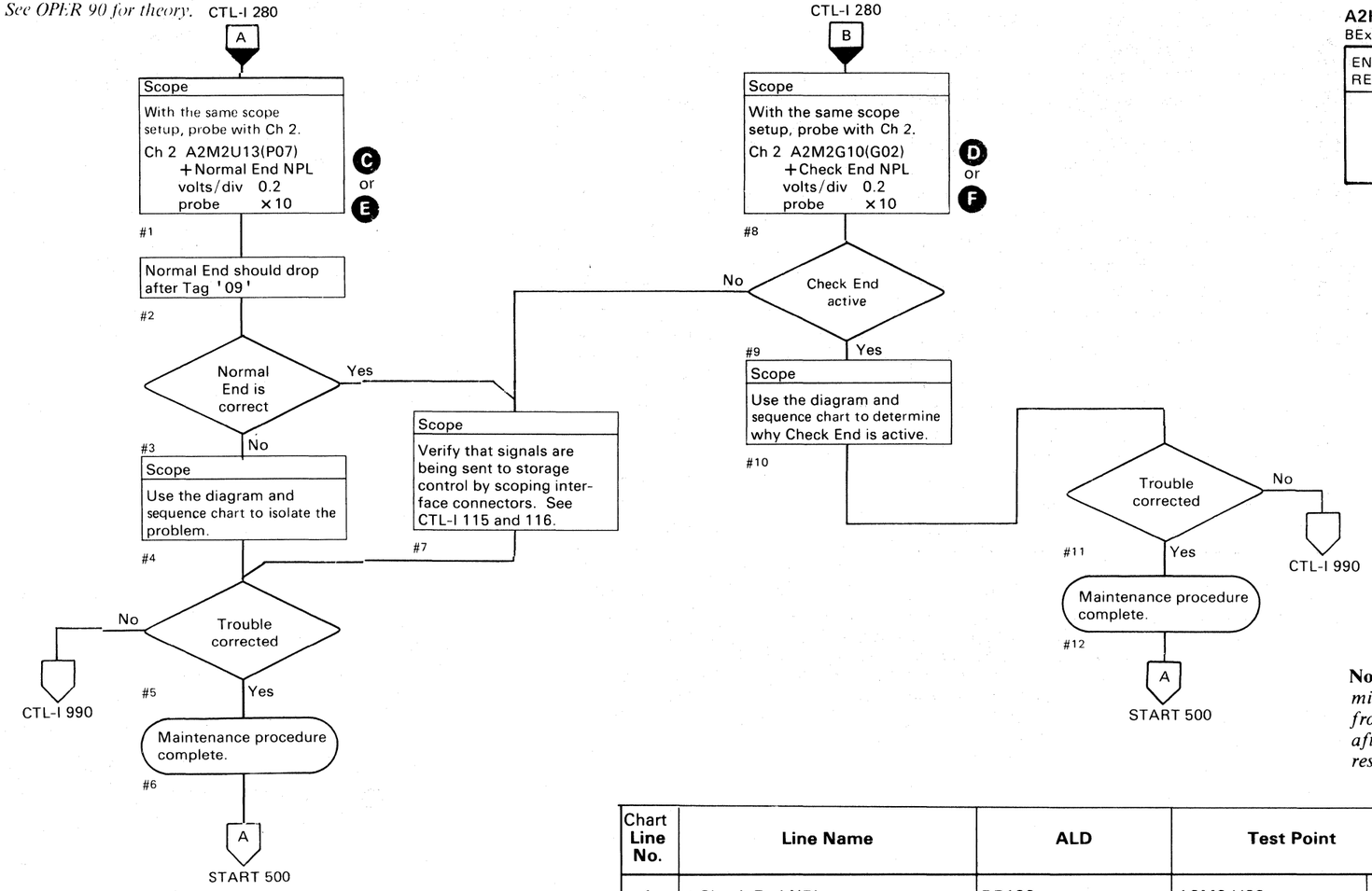
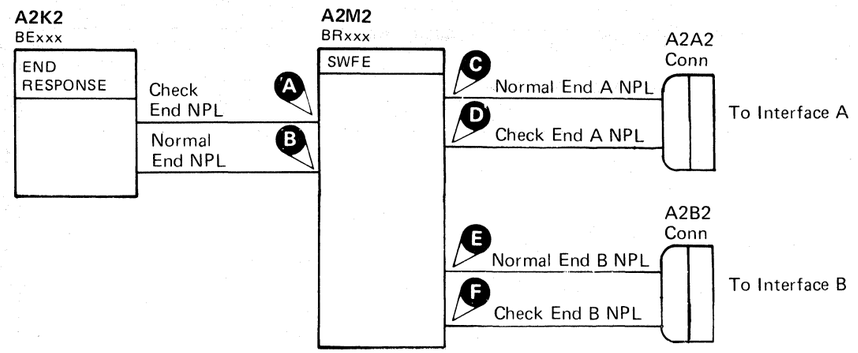
NORMAL END/CHECK END FAILURE (With String Switch)

See OPER 90 for theory.

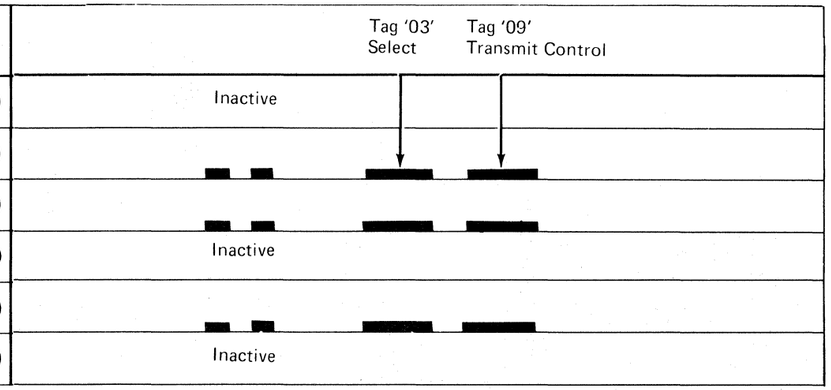




Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted is not valid.*

Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+Check End NPL	BR130	A2M2 U09	A
2	+Normal End NPL	BR130	A2M2 S09	B
3	+Normal End A NPL	BR170	A2M2 U13	C
4	+Check End A NPL	BR170	A2M2 G10	D
5	+Normal End B NPL	BR180	A2M2 P07	E
6	+Check End B NPL	BR180	A2M2 G02	F



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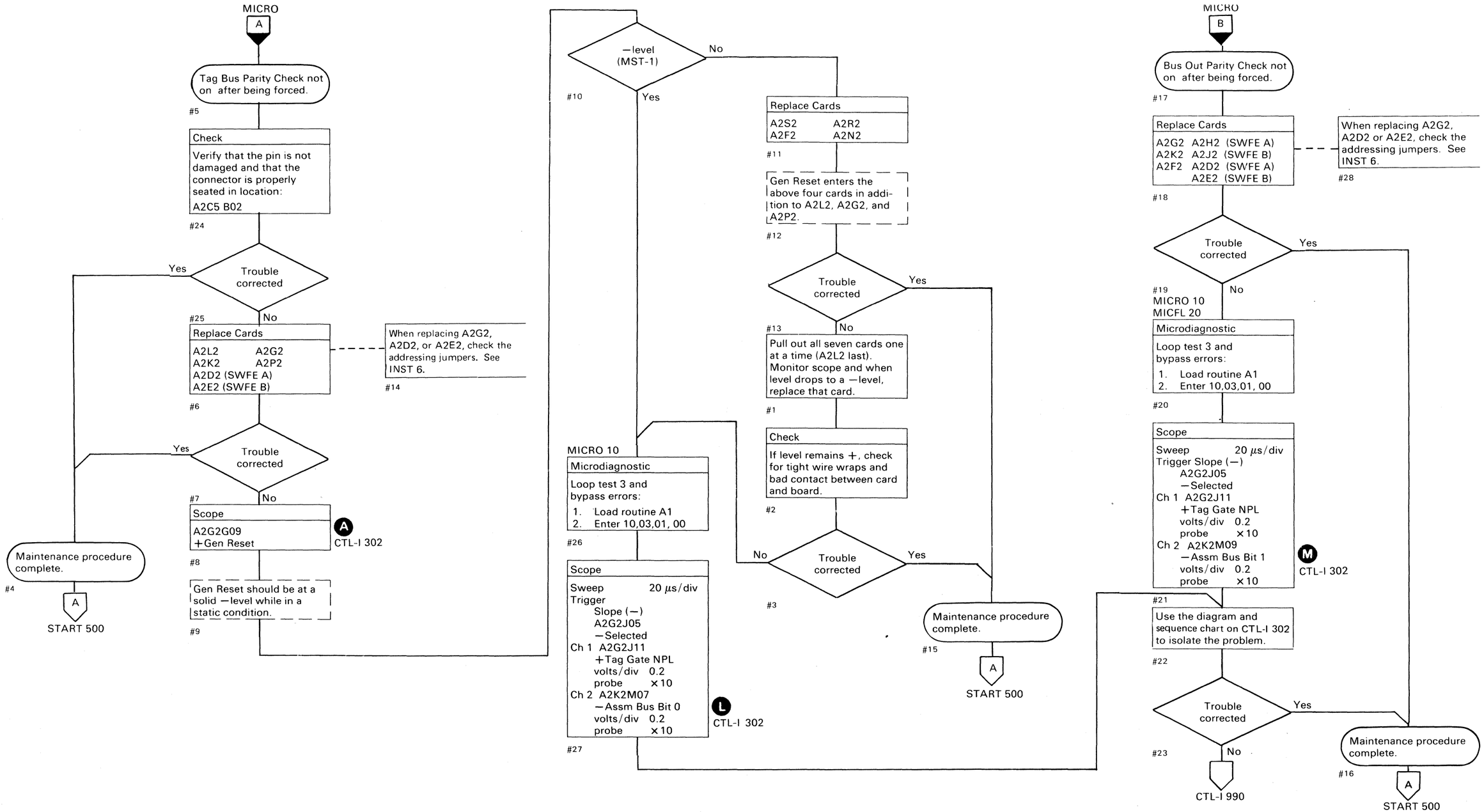
TAG BUS/BUS OUT PARITY CHECK



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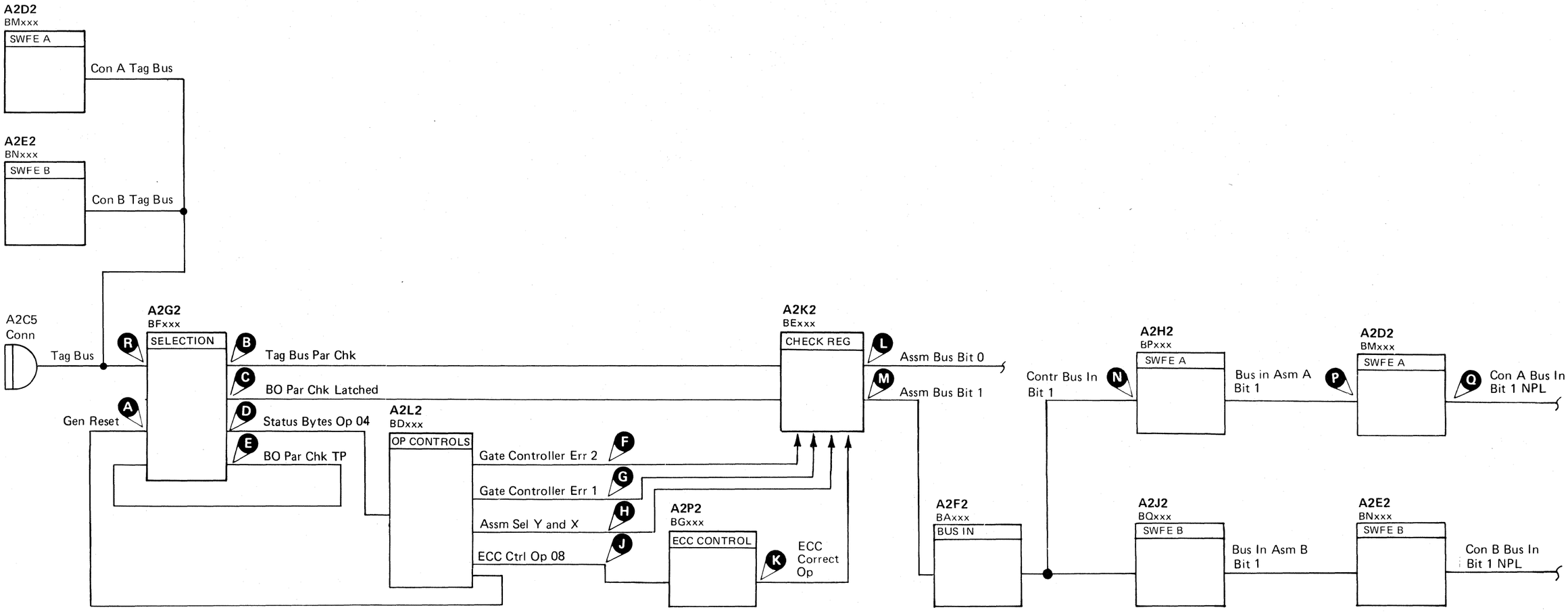
TAG BUS/BUS OUT PARITY CHECK

See OPER 90 for theory.



TAG BUS/BUS OUT PARITY CHECK

Tag Bus Parity Check

See the diagram on CTL-I 302 for referenced test points.

Microdiagnostic routine A1, test 3 issues an invalid Tag '94' which causes a Tag Bus Parity Check (B).

The microdiagnostic then issues a Tag '04', expecting an Assm Bus Bit 0 (L).

Status Byte Op 04 (D) and Bus Out Bit 6 activate Gate Controller Err 1.

Gate Controller Err 1 (G) gates Tag Bus Parity Check through the Check Register as Check Bit 0. Check Bit 0 becomes Assm Bus Bit 0 (L) if Assm Sel Y and X (H) are not active.

If Tag Bus Bit 0 (R) is not active during Tag '94' time, a Tag Bus Parity Error does not occur.

If any of the following gates are active during Tag '04' time, Tag Bus Parity Chk (B) is not gated through the Check Register and an error occurs:

- Gate Controller Err 2
- Assm Sel Y
- Assm Sel X
- ECC Correct Op
- ECC Ctrl Op 08

Bus Out Parity Check

See the diagram on CTL-I 302 for referenced test points.

Microdiagnostic routine A1, test 3 forces a BO Parity Check (E) by changing Bus Out from '00' to '01' while Tag Gate is active.

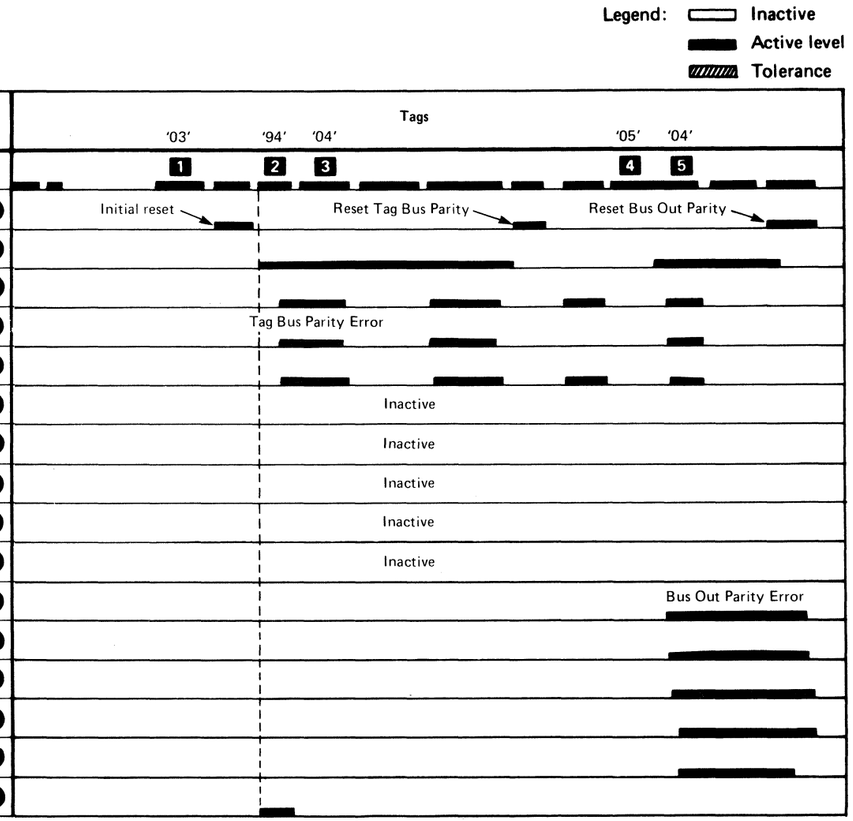
Tag Gate and Bus Out Parity Check sets BO Par Chk Latched (C).

The microdiagnostic then issues a Tag '04' to sense Assm Bus Bit 1 (M).

If the string switch feature is installed and Assm Bus Bit 1 is correct, trace bit 1 through the SWFE cards (N), (P) and (Q).

Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

Chart Line No.	Line Name	ALD	Test Point	
1	+Tag Gate NPL	BF130	A2G2 J11	
2	+Gen Reset	BF110	A2G2 G09	A
3	–Tag Bus Par Chk	BF110	A2G2 G10	B
4	–Gate Controller Err 1	BD100	A2L2 J09	G
5	–Assm Bus Bit 0	BE110	A2K2 M07	L
6	–Status Byte Op 04	BF110	A2G2 G03	D
7	–Gate Controller Err 2	BD100	A2L2 P13	F
8	–Assm Sel Y	BD110	A2L2 M07	H
9	–Assm Sel X	BD110	A2L2 P06	H
10	–ECC Correct Op	BG170	A2P2 B04	K
11	–ECC Ctrl Op 08	BD100	A2L2 J13	J
12	–Assm Bus Bit 1	BE110	A2K2 M09	M
13	–Contr Bus In Bit 1	BP200 (BQ200)	A2H2 (A2J2) G05	N
14	–Bus In Assm Bit 1	BM180 (BN180)	A2D2 (A2E2) U13	P
15	+Con Bus In Bit 1 NPL	BM160 (BN160)	A2D2 (A2E2) U07	Q
16	–B0 Par Chk Latched	BF110	A2G2 J10	C
17	+Tag Bus Bit 0 NPL	BF100	A2G2 D13	R



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CONTROLLER CHECK MISSING

The following is the normal operation for generating a Controller Check.

Controller Chk is gated by BI Sel Y and sent to storage control as Contr Bus In Bit 0 NPL (F).

Tag Bus Par Chk (C) sets Controller Chk (D).

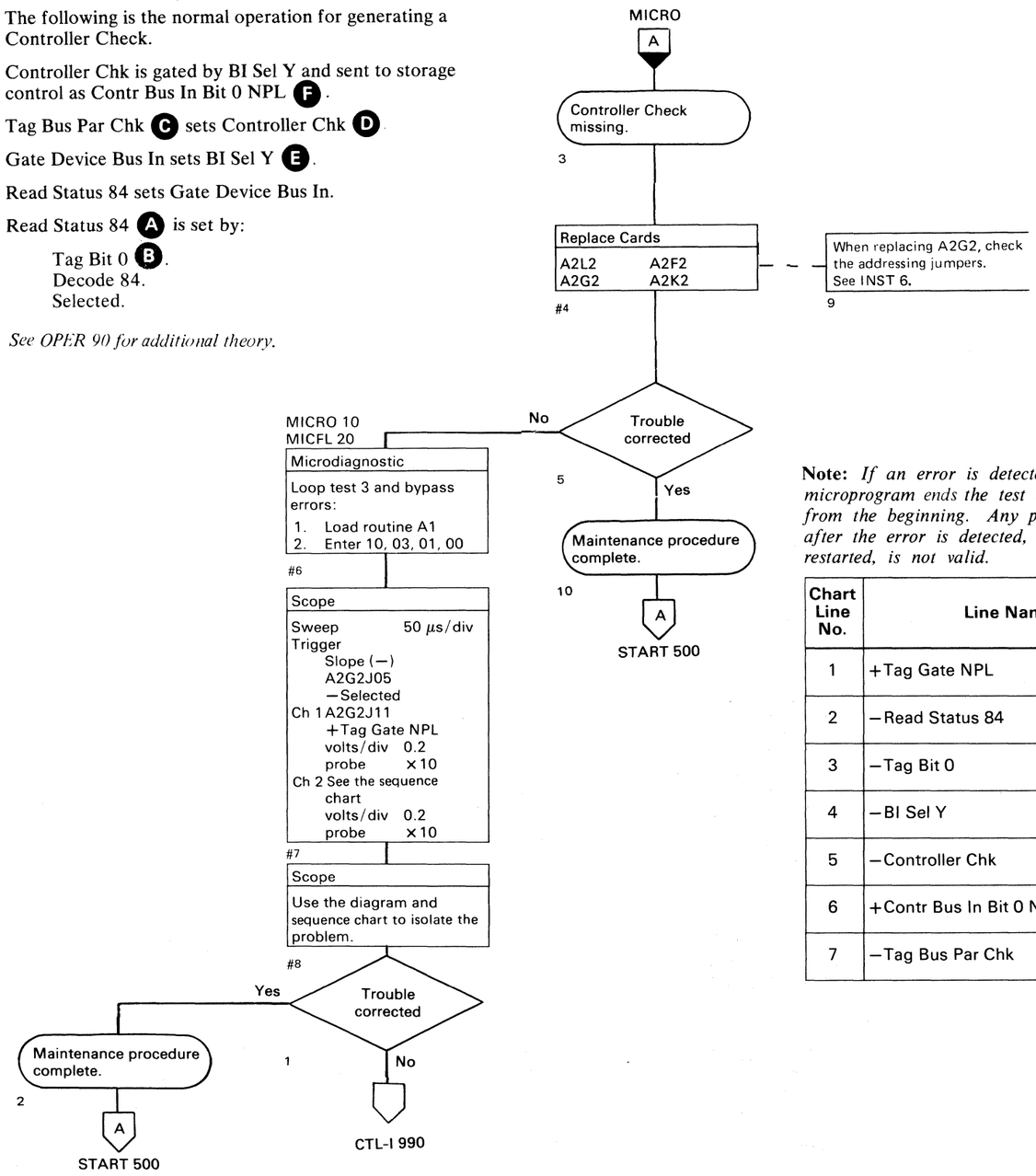
Gate Device Bus In sets BI Sel Y (E).

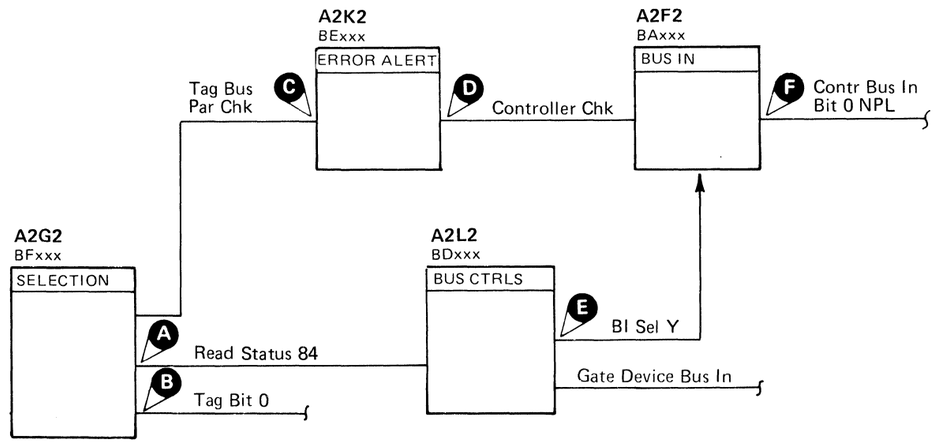
Read Status 84 sets Gate Device Bus In.

Read Status 84 (A) is set by:

- Tag Bit 0 (B).
- Decode 84.
- Selected.

See OPER 90 for additional theory.

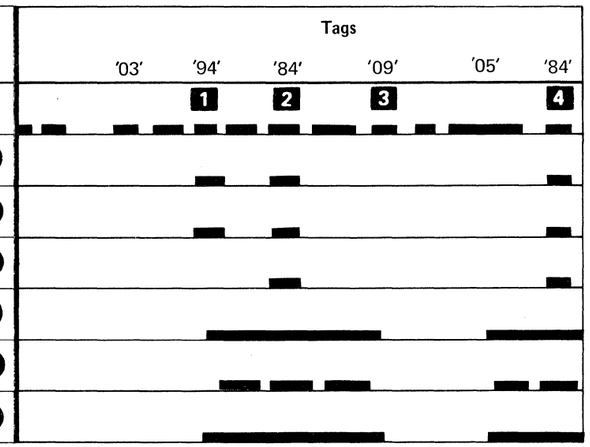




Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

Legend: Inactive / Active level / Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+Tag Gate NPL	BF130	A2G2 J11	
2	−Read Status 84	BF110	A2G2 D09	A
3	−Tag Bit 0	BF100	A2G2 J03	B
4	−BI Sel Y	BD110	A2L2 P04	E
5	−Controller Chk	BE130	A2K2 M12	D
6	+Contr Bus In Bit 0 NPL	BA150	A2F2 D06	F
7	−Tag Bus Par Chk	BE120	A2K2 U02	C



1 Tag '94' = Invalid tag
2 Tag '84' = If Controller Check is not on, A135 Error Code occurs.
3 Tag '09' = Reset Controller Check.
4 Tag '84' = If Controller Check is not on, A138 Error Code occurs

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ERROR ALERT FAILURE

The following is the normal operation for generating an Error Alert.

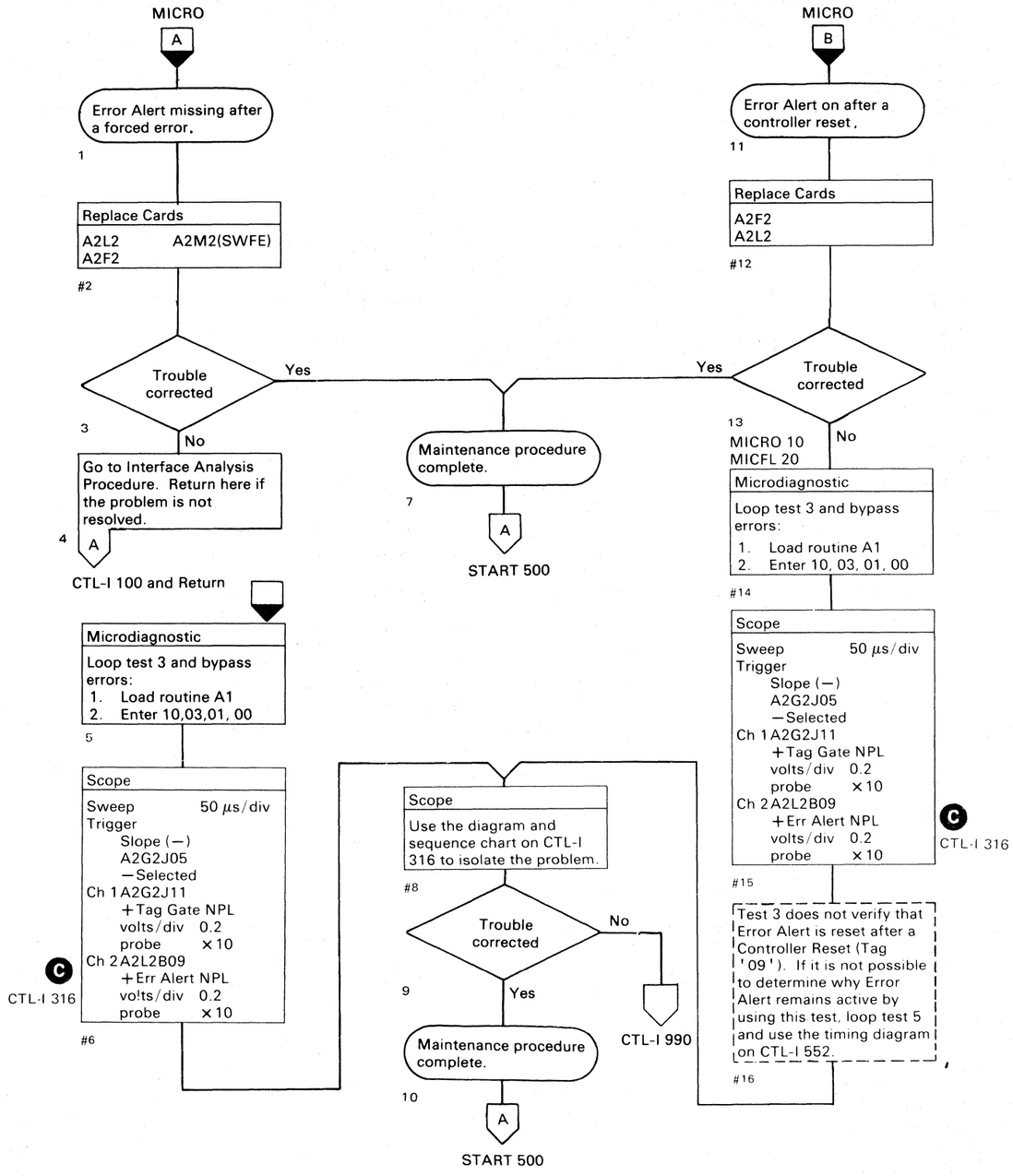
See the diagram on CTL-I 316 for referenced test points.

Controller Chk (A) sets Err Alert Cond (B).

Err Alert Cond sets Suppr Error Alert (D).

Suppr Error Alert sets Err Alert NPL (C).

See OPER 241 for errors that cause Error Alert.



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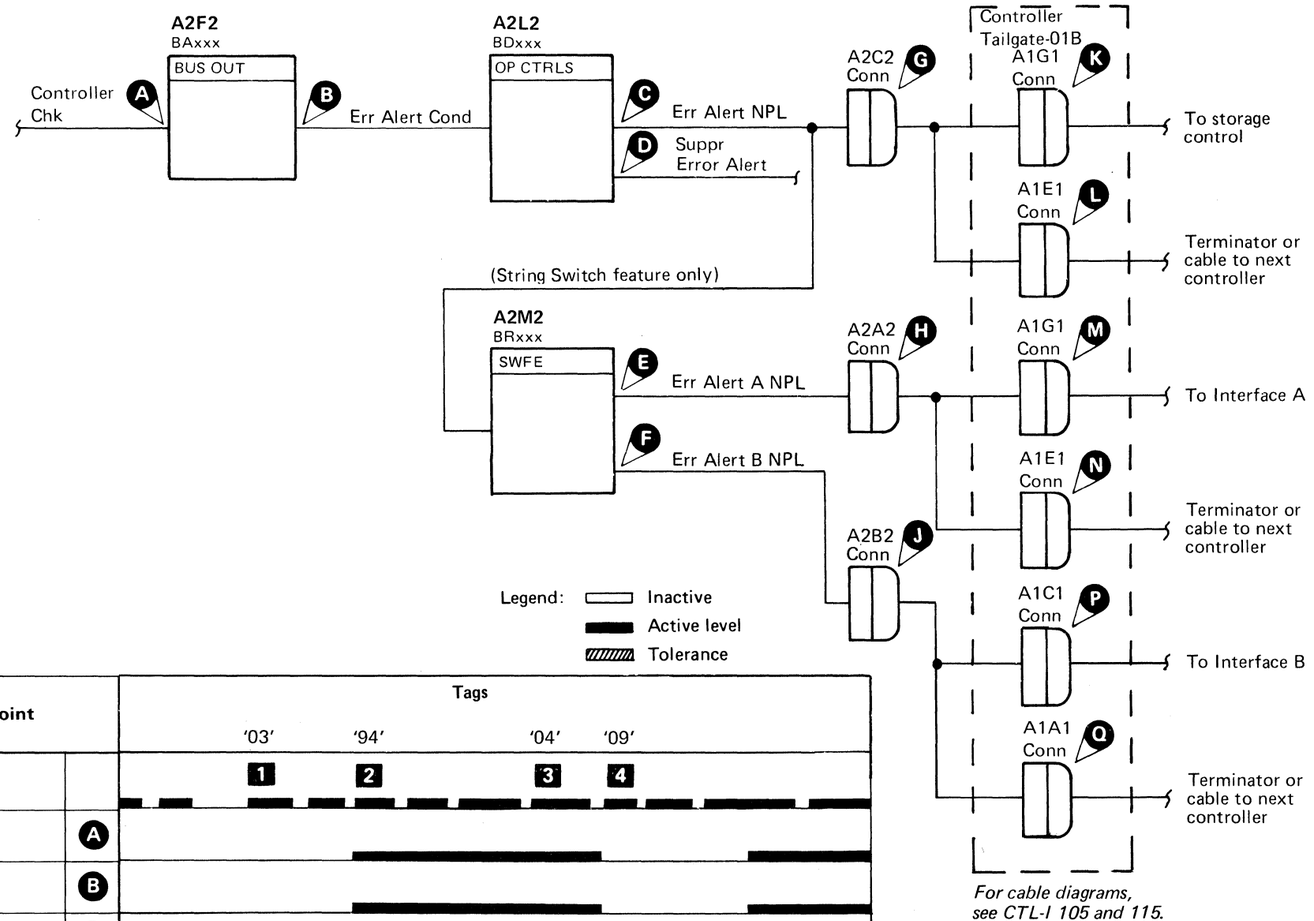
ERROR ALERT FAILURE

See OPER 90 for theory.

Figure 1. Connector Pin Locations.

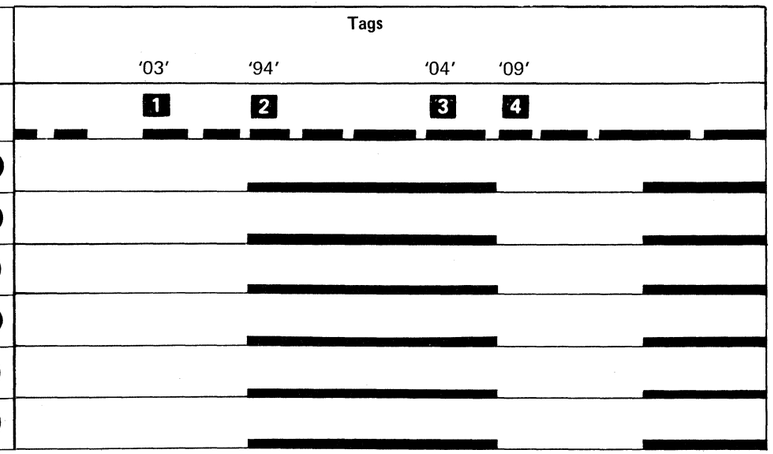
Line Name	Conn A2C2 Pin G	Conn A1G1 Pin K	Conn A1E1 Pin L
+Err Alert NPL	B08/B09	G08	G08
	Conn A2A2 Pin H	**Conn A1G1 Pin M**	**Conn A1E1 Pin N**
+Err Alert A NPL	B08/B09	G08	G08
	Conn A2B2 Pin J	**Conn A1C1 Pin P**	**Conn A1A1 Pin Q**
+Err Alert B NPL	B08/B09	G08	G08



For cable diagrams, see CTL-I 105 and 115.

Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

Chart Line No.	Line Name	ALD	Test Point	
1	+Tag Gate NPL	BF130	A2G2 J11	
2	−Controller Chk	BA140	A2F2 P02	A
3	−Err Alert Cond.	BA140	A2F2 J10	B
4	−Suppr Error Alert	BD170	A2L2 D12	D
5	+Err Alert NPL	BD230	A2L2 B09	C
6	+Err Alert A NPL	BR170	A2M2 J03	E
7	+Err Alert B NPL	BR180	A2M2 G04	F



1 Tag '03' = Select controller
2 Tag '94' = Invalid tag
3 Tag '04' = Sense Error Alert. If it is not on, A134 Error Code occurs.
4 Tag '09' = Reset Controller Check

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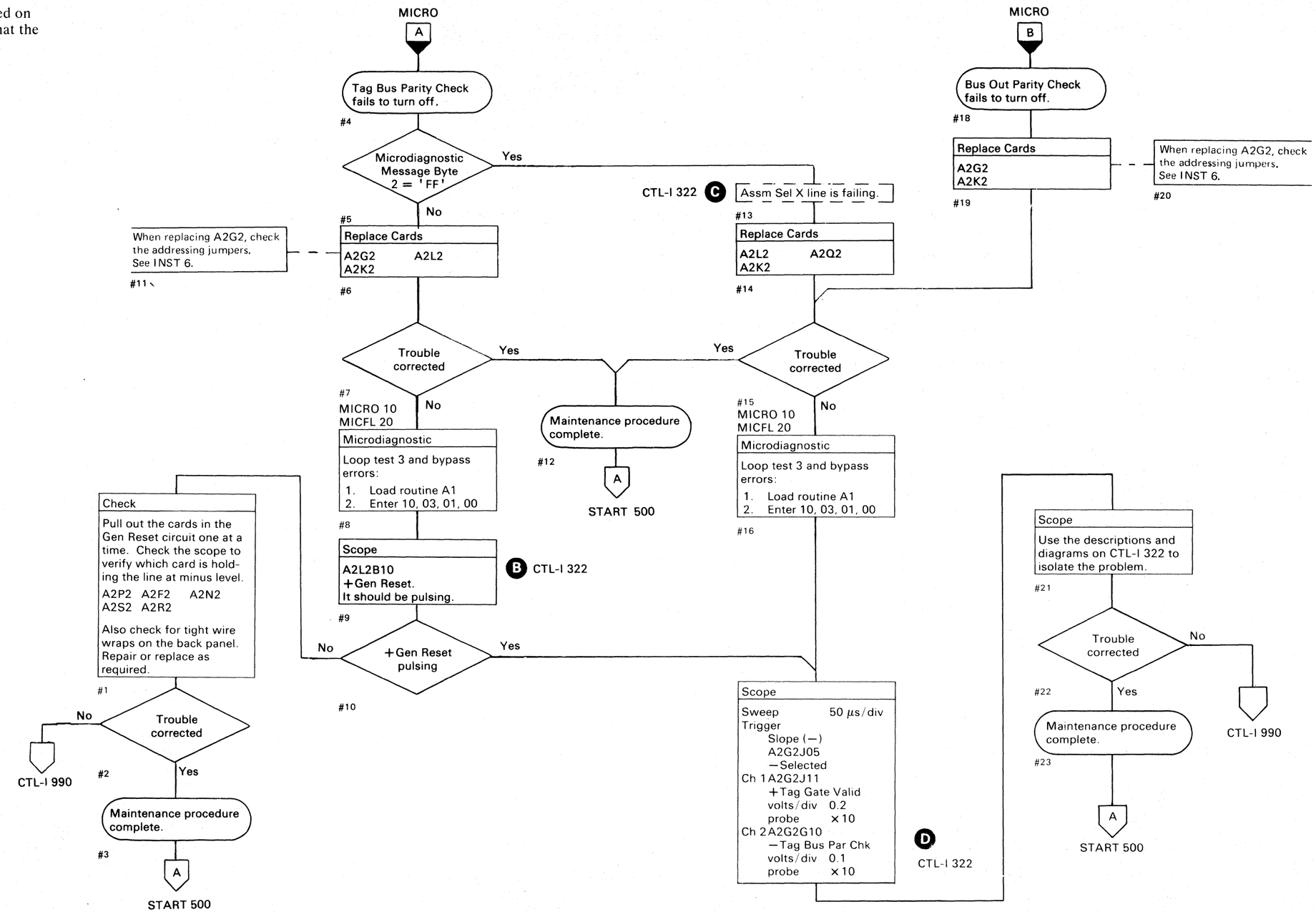
PARITY CHECK FAILURE

Tag Bus and Bus Out Parity Check latches are forced on and then reset. The microdiagnostic then verifies that the error condition was reset.



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PARITY CHECK FAILURE

Tag Bus Parity Check

Assm Bus Bit 0 (F) is set by Tag Bus Par Chk (D).

Gen Reset (B) turns off Tag Bus Parity Chk.

All Assm Bus Bits ('FF') are gated to the interface if Assm Sel X (C) is active.

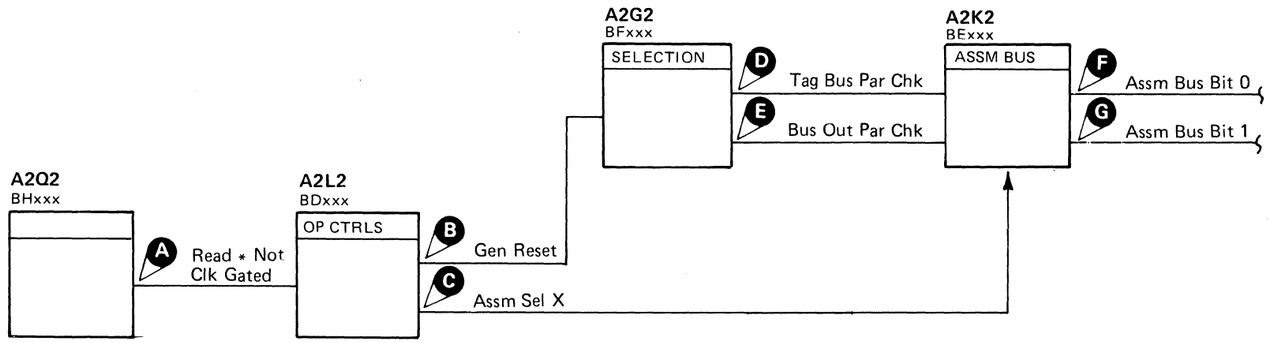
Assm Sel X is activated by Read*Not Clk Gated (A).

Bus Out Parity Check

Assm Bus Bit 1 (G) is set by Bus Out Par Chk (E).

Gen Reset (B) turns off Bus Out Parity Chk.

See OPER 90 for additional theory.



Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

Legend: Inactive / Active level / Tolerance

Chart Line No.	Line Name	ALD	Test Point		'03'	'94'	'09'	'04'	'05'	'84'	'09'
1	+Tag Gate NPL	BF130	A2G2 J11		1	2	3	4	5		6
2	−Tag Bus Par Chk	BF110	A2G2 G10	D							
3	−Bus Out Par Chk	BF110	A2G2 J10	E							
4	−Assm Sel X	BD110	A2L2 P06	C	Inactive						
5	+Gen Reset	BD100	A2L2 B10	B							
6	−Read*Not Clk Gated	BH120	A2Q2 D06	A	Inactive						
7	−Assm Bus Bit 0	BE110	A2K2 M07	F							
8	−Assm Bus Bit 1	BE110	A2K2 M09	G							

1. Tag '03' = Select controller
2. Tag '94' = Force Tag Bus Parity Check
3. Tag '09' = Reset Tag Bus Parity Check. If it fails to reset, A131 Error Code occurs.
4. Tag '04' = Verify that Tag Bus Pairty was reset.
5. Tag '05' = Force Bus Out Parity Check by changing Bus Out from '00' to '01' with Tag Gate active.
6. Tag '09' = Reset Bus Out Parity Check. If it fails to reset, A133 Error Code occurs.

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NORMAL END FAILURE

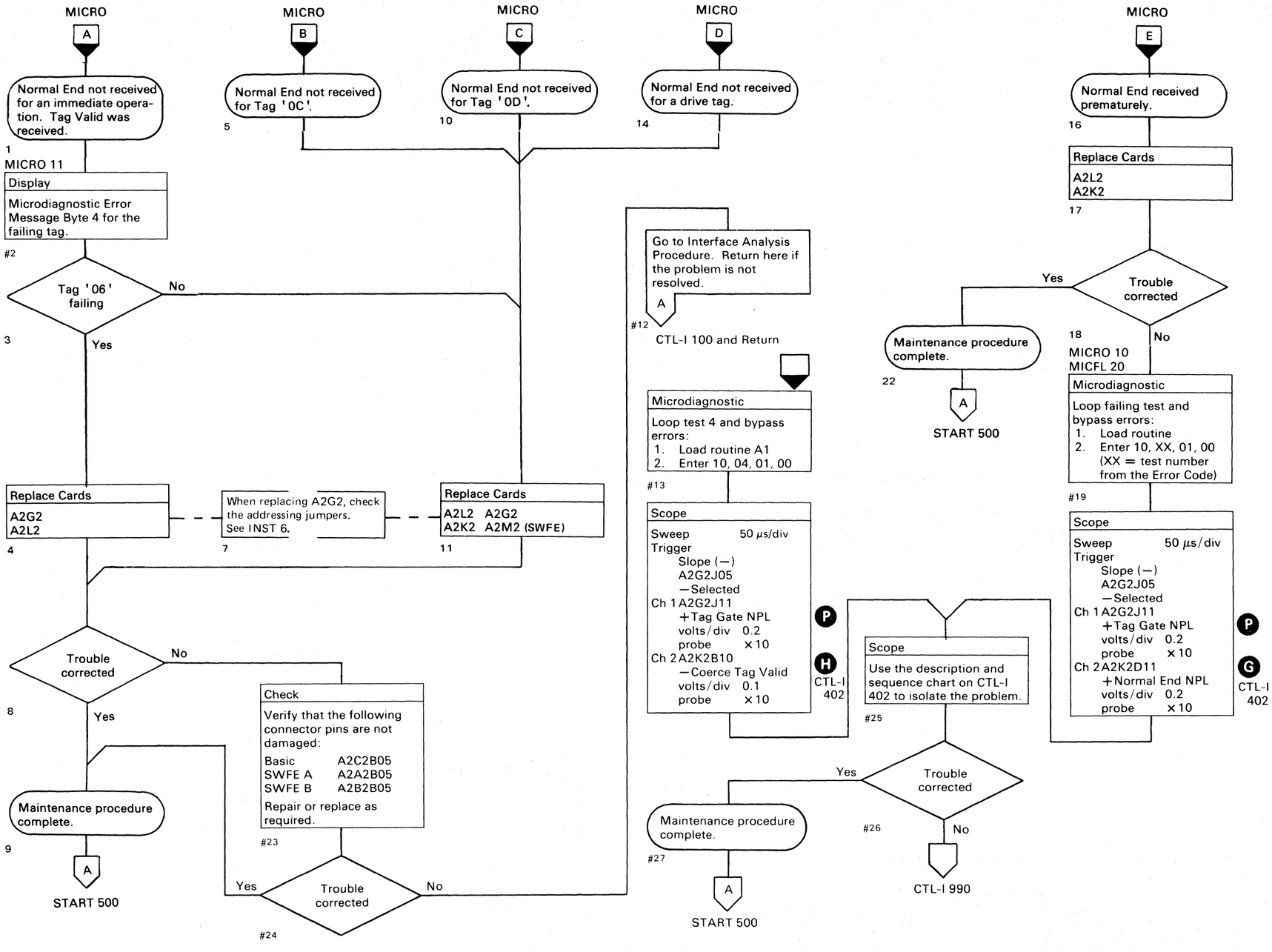
Each operation, whether an immediate or extended operation, must be terminated with a Normal End or a Check End.

For immediate operations, Normal End occurs simultaneously with Tag Valid.

For extended operations (Read, Write, ECC Control and Set Read/Write), Normal End and Tag Valid are returned at different times.

Microdiagnostic routine A1, test 4 issues all controller tags and checks for Tag Valid. If Tag Valid is returned, the microdiagnostic then checks for Normal End. If Normal End is not returned, an A141 Error Code occurs. The tag sequence is as follows:

'0B', '01', '02', '04', '05', '06', '07', '09', '0A', '0C', '0D'.



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NORMAL END FAILURE

Normal End Missing (A141 Error Code)

Normal End NPL (G) is set by:

Coerce Tag Valid (H)
Imm Op (C)

Imm Op blocks Normal End if any of the following lines are active before the extended Ops ('08', '0E' or '0F') are issued:

Read Op 0E (F)
Set RW Op 85 (A)
ECC Ctrl Op 08 (D)
Write Op 0F (E)

Tag Bit 4 (B) should not be active when tags '01', '02', '04', '05', '06', '07' are issued. If Tag Bit 4 is active with the above tags, the controller decodes:

Tag	'01' as '09'	Tag	'0E' as '0D'
	'02' as '0A'		'06' as '0E'
	'04' as '0C'		'07' as '0F'

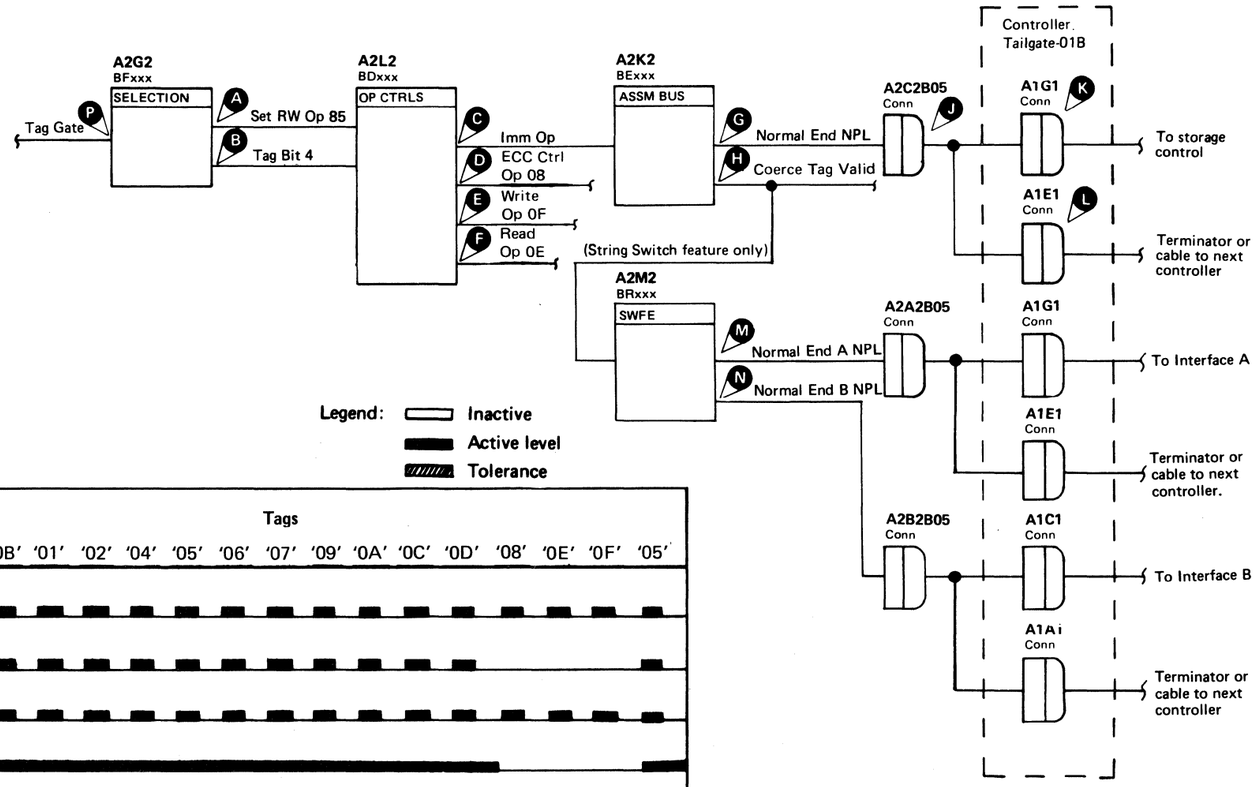
Normal End Premature (A14C Error Code)

Imm Op (C) is at a +level (MST-1) while the following lines are active:

ECC Ctrl Op 08 (D)
Read Op 0E (F) (E)
Write Op 0F

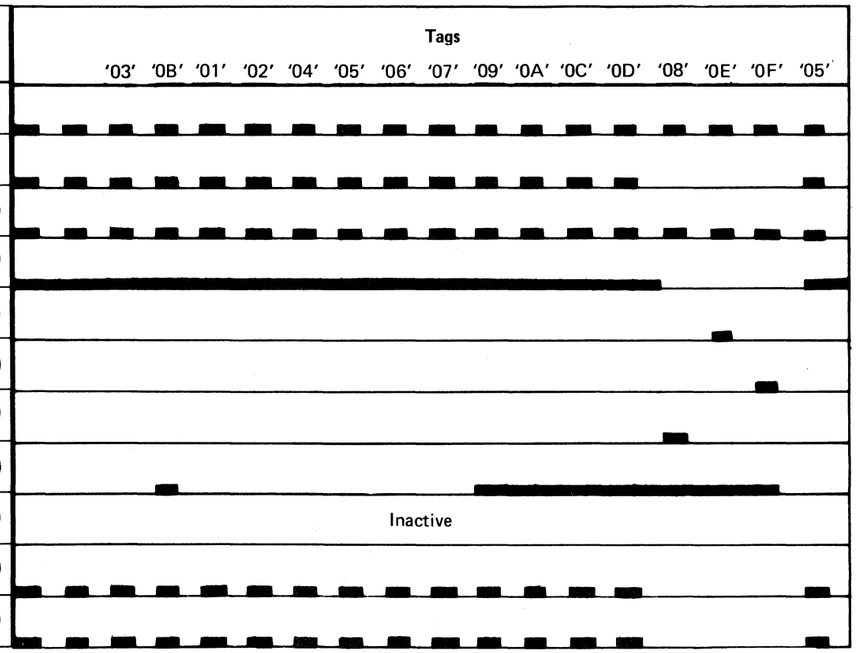
Microdiagnostic Message Byte 4 identifies the tag that caused the Normal End.

See OPER 90 for additional theory.



For cable diagrams, see CTL-I 105 and 115.

Chart Line No.	Line Name	ALD	Test Point	
1	+Tag Gate NPL	BF130	A2G2 J11	P
2	+Normal End NPL	BE160	A2K2 D11	G
3	−Coerce Tag Valid	BE150	A2K2 B10	H
4	−Imm Op	BD100	A2L2 P02	C
5	−Read Op 0E	BD100	A2L2 M02	F
6	−Write Op 0F	BD100	A2L2 M04	E
7	−ECC Ctrl Op 08	BD100	A2L2 J13	D
8	−Tag Bit 4	BF100	A2G2 J02	B
9	−Set RW Op 85	BF110	A2G2 D03	A
10	+Normal End A NPL	BR170	A2M2 U13	M
11	+Normal End B NPL	BR180	A2M2 P07	N



Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

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CONTROL TAG BUS/BUS OUT PARITY CHECK

See the diagram on CTL-I 412 for referenced test points.

Tag Bus Parity Check

While Tag Gate is active, bits on the Control Tag Bus are monitored. If an even number of bits is detected, the following occurs:

Tag Bus Par Chk (E) latch is set.
Tag Valid is blocked.
Normal End is inhibited.
Tag Bus Parity Check Display latch is set.
Error Alert and Controller Chk (F) are activated.

Bus Out Parity Check

While Tag Gate is active, bits on the Control Bus Out are monitored. If an even number of bits is detected, the following occurs:

BO Par Chk Latched (D) is set.
Tag Valid is blocked.
Normal End is inhibited.
Bus Out Parity Check Display latch is set.
Error Alert and Controller Chk (F) are activated.

Parity Check Lamps

Microdiagnostic routine A1, test 3, checks the Tag Bus and Bus Out Parity Check lamps. They should be on after running this test and remain on until reset by the Execute switch or Power On Reset.

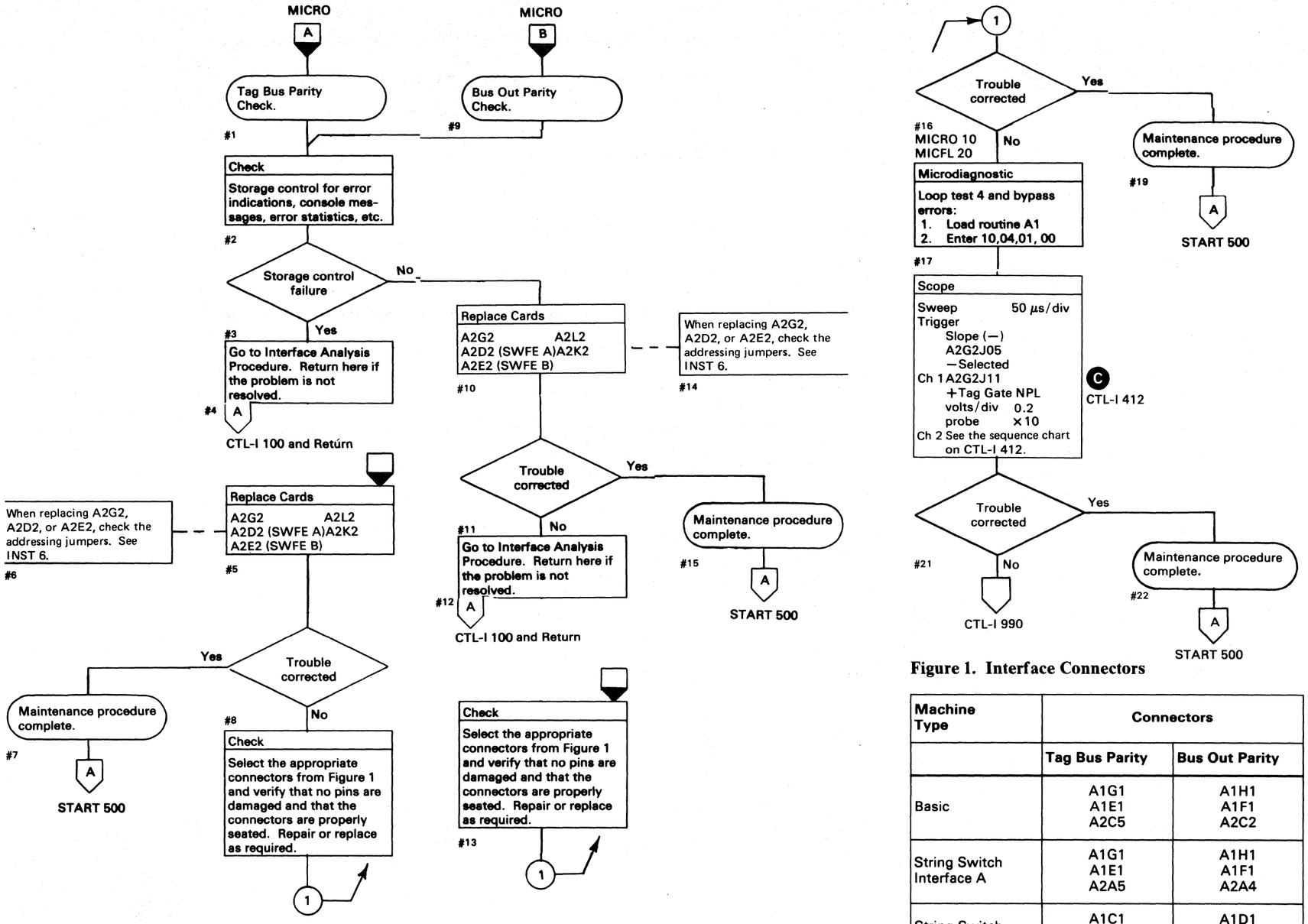

Figure 1. Interface Connectors

Machine Type	Connectors	
	Tag Bus Parity	Bus Out Parity
Basic	A1G1 A1E1 A2C5	A1H1 A1F1 A2C2
String Switch Interface A	A1G1 A1E1 A2A5	A1H1 A1F1 A2A4
String Switch Interface B	A1C1 A1A1 A2B5	A1D1 A1B1 A2B4

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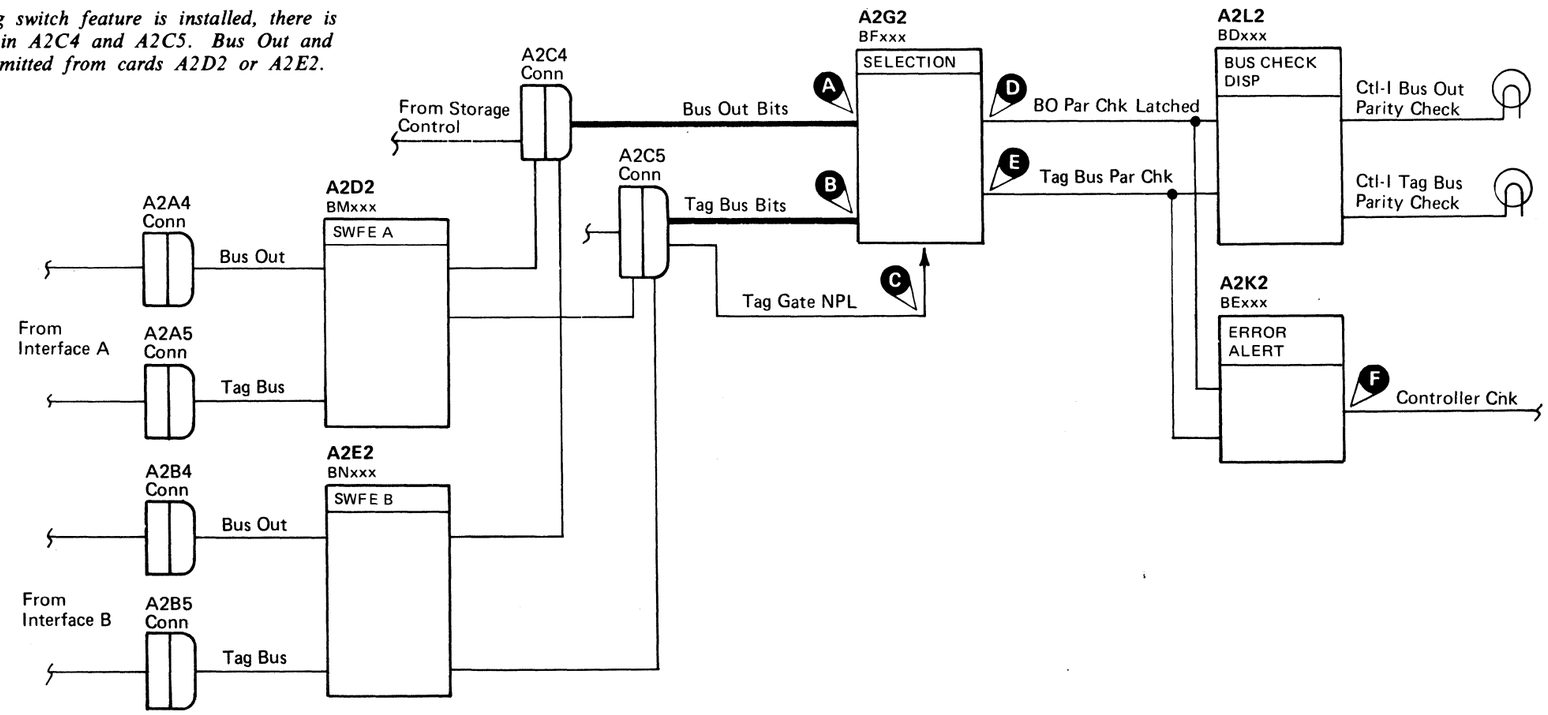
CONTROL TAG BUS/BUS OUT PARITY CHECK

See OPER 90 for theory.

Note: *If the string switch feature is installed, there is no cable installed in A2C4 and A2C5. Bus Out and Tag Bus are transmitted from cards A2D2 or A2E2.*



Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

Legend: Inactive
Active level
Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags '03' '0B' '01' '02' '04' '05' '06' '07' '09' '0A' '0C' '0D' '08' '0E' '0F' '05'
1	+Tag Gate NPL	BF130	A2G2 J11	C	
2	–BO Par Chk Latched	BF110	A2G2 J10	D	Inactive
3	–Tag Bus Par Chk	BF110	A2G2 G10	E	Inactive

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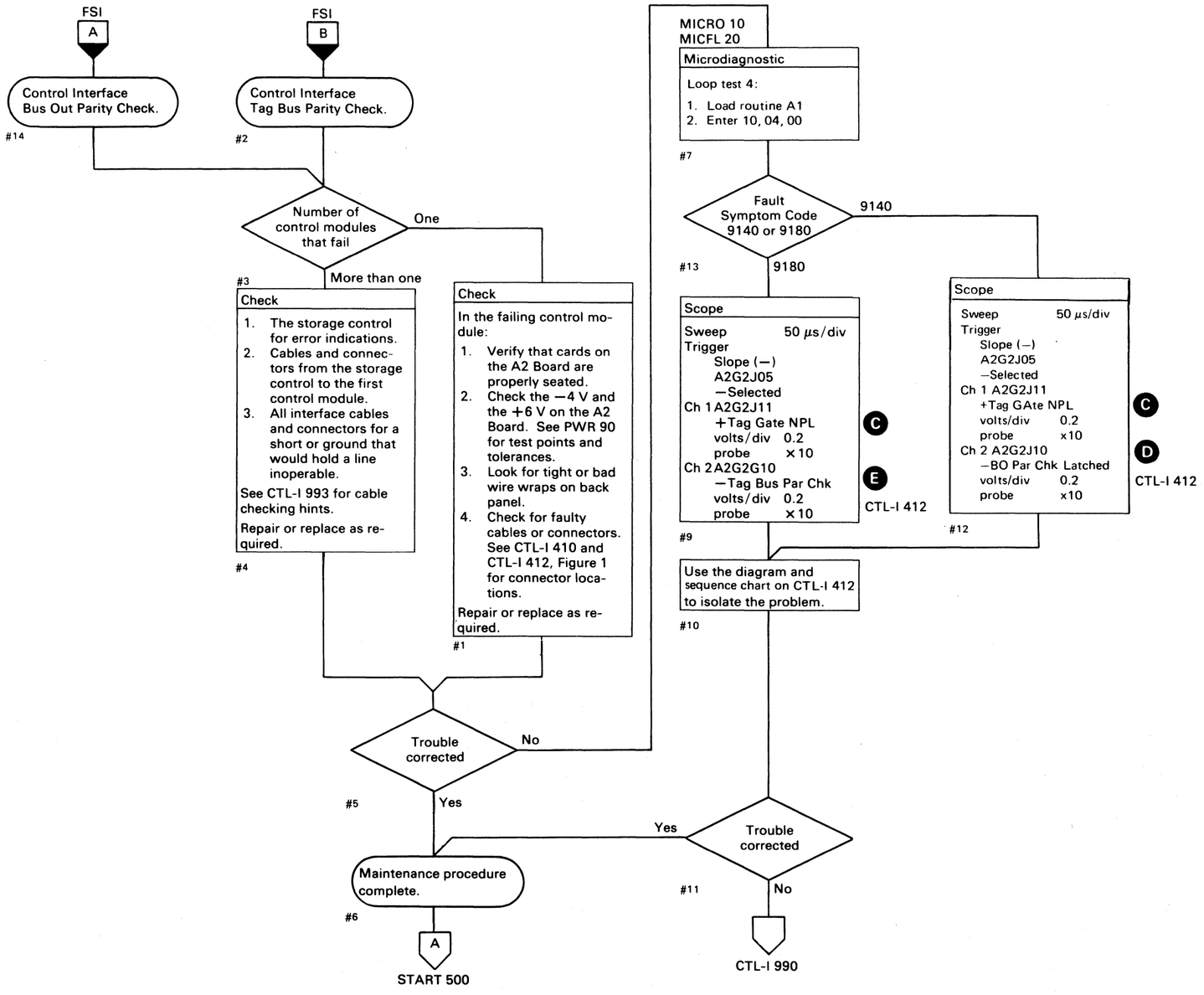
CONTROL TAG BUS/BUS OUT PARITY CHECK



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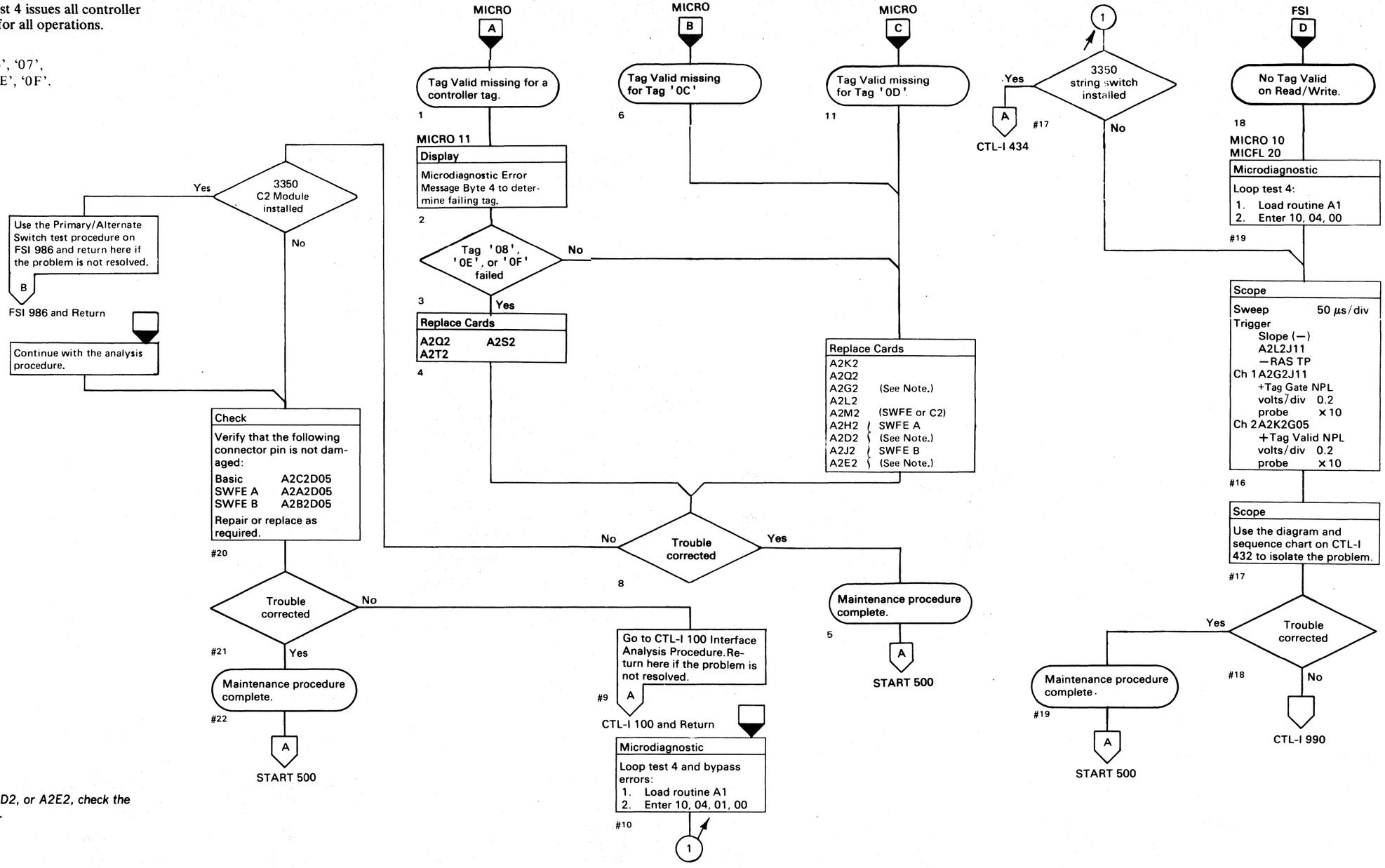
MISSING TAG VALID

Microdiagnostic routine A1, test 4 issues all controller tags and checks for Tag Valid for all operations. The tag sequence is as follows:

'0B', '01', '02', '04', '05', '06', '07', '09', '0A', '0C', '0D', '08', '0E', '0F'.



Note: *When replacing A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.*

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MISSING TAG VALID

Tag Valid Missing On Tags '08', '0E', and '0F'

This error is usually caused by RW Op Dld (K) going to −level (MST-1) and activating Block Tag Valid to a +level (MST-1).
RW Op Dld is −level if Half F (F) is at either a solid +level or −level.
Half F is pulsing if VFO 1F (G) is pulsing and Special VFO Reset (B) is −level (MST-1).
VFO 1F is pulsing if VCO Inject TP (H) is pulsing.
Selected Tag Gate (E) must be at a −level (MST-1).

Tag Valid Missing On Immediate Tags.

Each time a tag is issued, it sets Tag Valid NPL.
If Tag Valid NPL is correct, the problem is in the cables and connectors to storage control.
Tag Valid NPL (L) is set by Coerce Tag Valid (Q).
Coerce Tag Valid is set by Valid Tag Gate (D) and not Block Tag Valid (J) or Alt*Pri Check (R).
Tag Valid missing is caused by:

- Allow Drive Tag Valid (C)
- Valid Tag Gate (D)
- Write Op 0F (A), causing +Block Tag Valid (J).
- + Alt*Pri Check (R)

Alt * Pri Check is set when both controllers are selected or online.

See OPER 90 for additional theory.

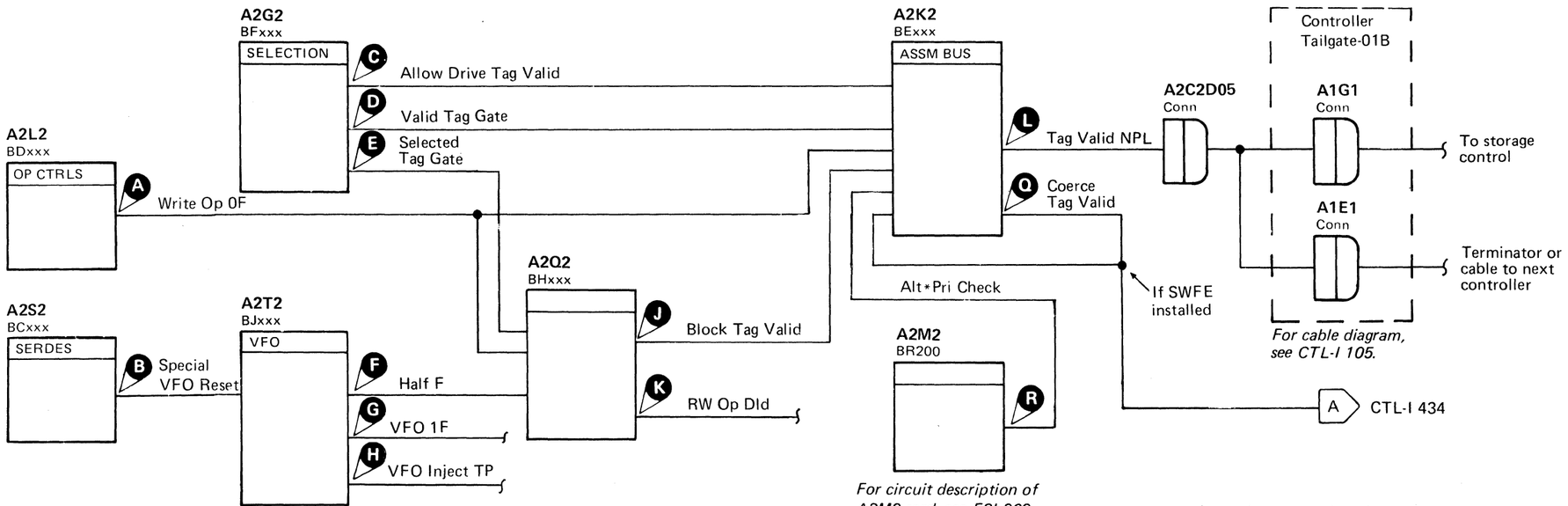

Chart Line No.	Line Name	ALD	Test Point		Tags
1	−Write Op 0F	BD100	A2L2 M04	A	Inactive
2	+Tag Gate NPL	BF130	A2G2 J11		'0B' '01' '02' '04' '05' '06' '07' '09' '0A' '0C' '0D' '08' '0E' '0F' '05'
3	−Selected Tag Gate	BF110	A2G2 G07	E	
4	+Tag Valid NPL	BE160	A2K2 G05	L	
5	−Allow Drive Tag Valid	BF110	A2G2 G11	C	Inactive
6	−Valid Tag Gate	BF110	A2G2 B09	D	
7	+Half F	BJ130	A2T2 G13	F	
8	+VFO 1F	BJ130	A2T2 B07	G	High Frequency Pulses
9	VCO Inject TP	BJ130	A2T2 G08	H	
10	+Special VFO Reset	BC130	A2S2 J07	B	Inactive
11	−RW Op Dld	BH100	A2Q2 B10	K	

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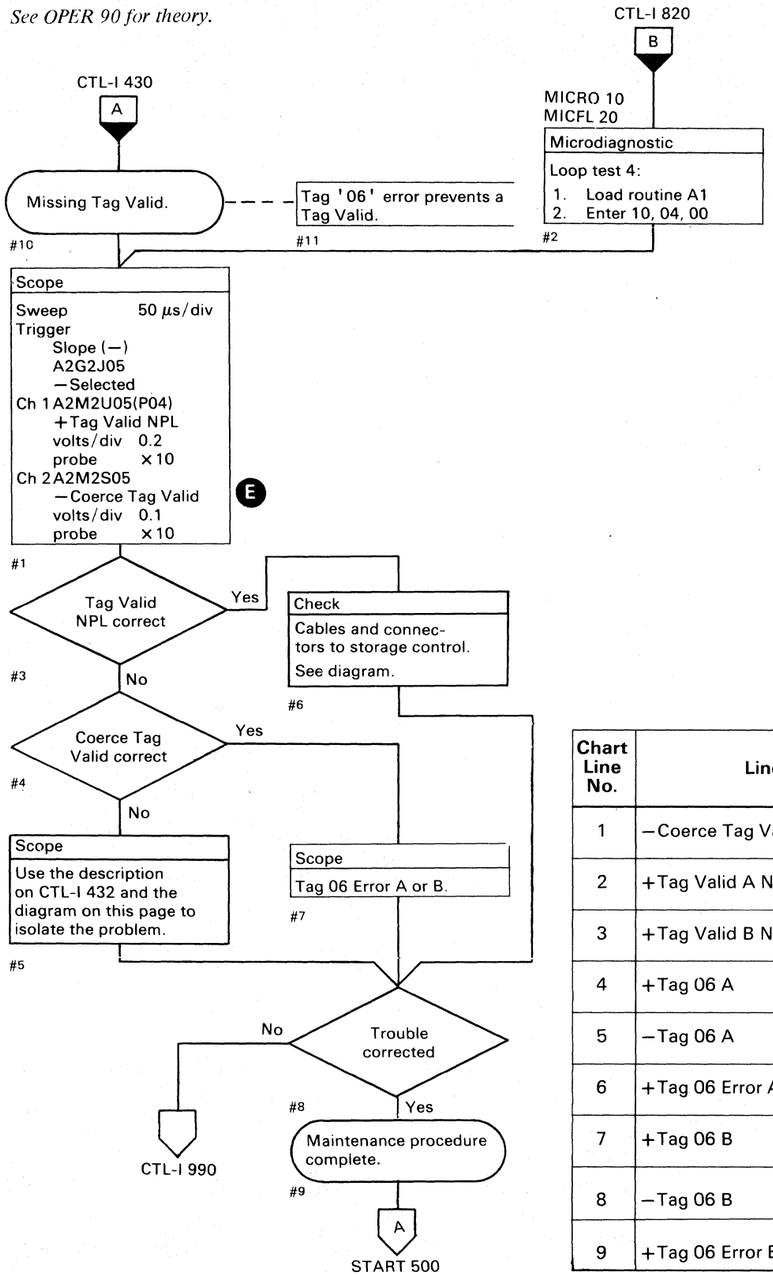
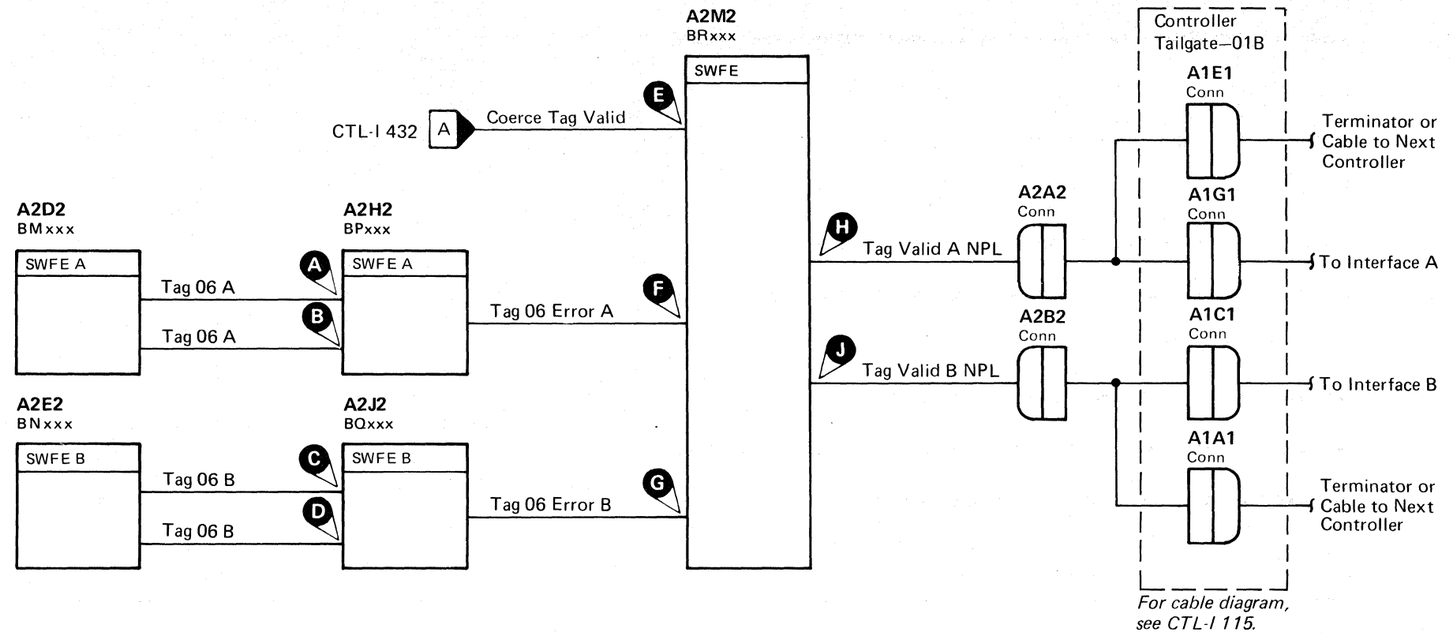
MISSING TAG VALID (With String Switch)

See OPER 90 for theory.





Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags '03' '0B' '01' '02' '04' '05' '06' '07' '09' '0A' '0C' '0D' '08' '0E' '0F' '05'
1	—Coerce Tag Valid	BR150	A2M2 S05	E	
2	+Tag Valid A NPL	BR170	A2M2 U05	H	
3	+Tag Valid B NPL	BR180	A2M2 P04	J	
4	+Tag 06 A	BP190	A2H2 G04	A	
5	—Tag 06 A	BP190	A2H2 M03	B	
6	+Tag 06 Error A	BR150	A2M2 J05	F	Inactive
7	+Tag 06 B	BQ190	A2J2 G04	C	
8	—Tag 06 B	BQ190	A2J2 M03	D	
9	+Tag 06 Error B	BR160	A2M2 J10	G	Inactive

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BUS IN PARITY CHECK

Bus In Parity Failed to Set

Microdiagnostic routine A1 issues Tag '09', Bus '20' to Invert Bus In Par (B).
Tag '04', Bus '02' is issued to set Contr Bus In Par Chk Latch (E).
Contr Bus In Par Chk Latch is then gated through registers as:

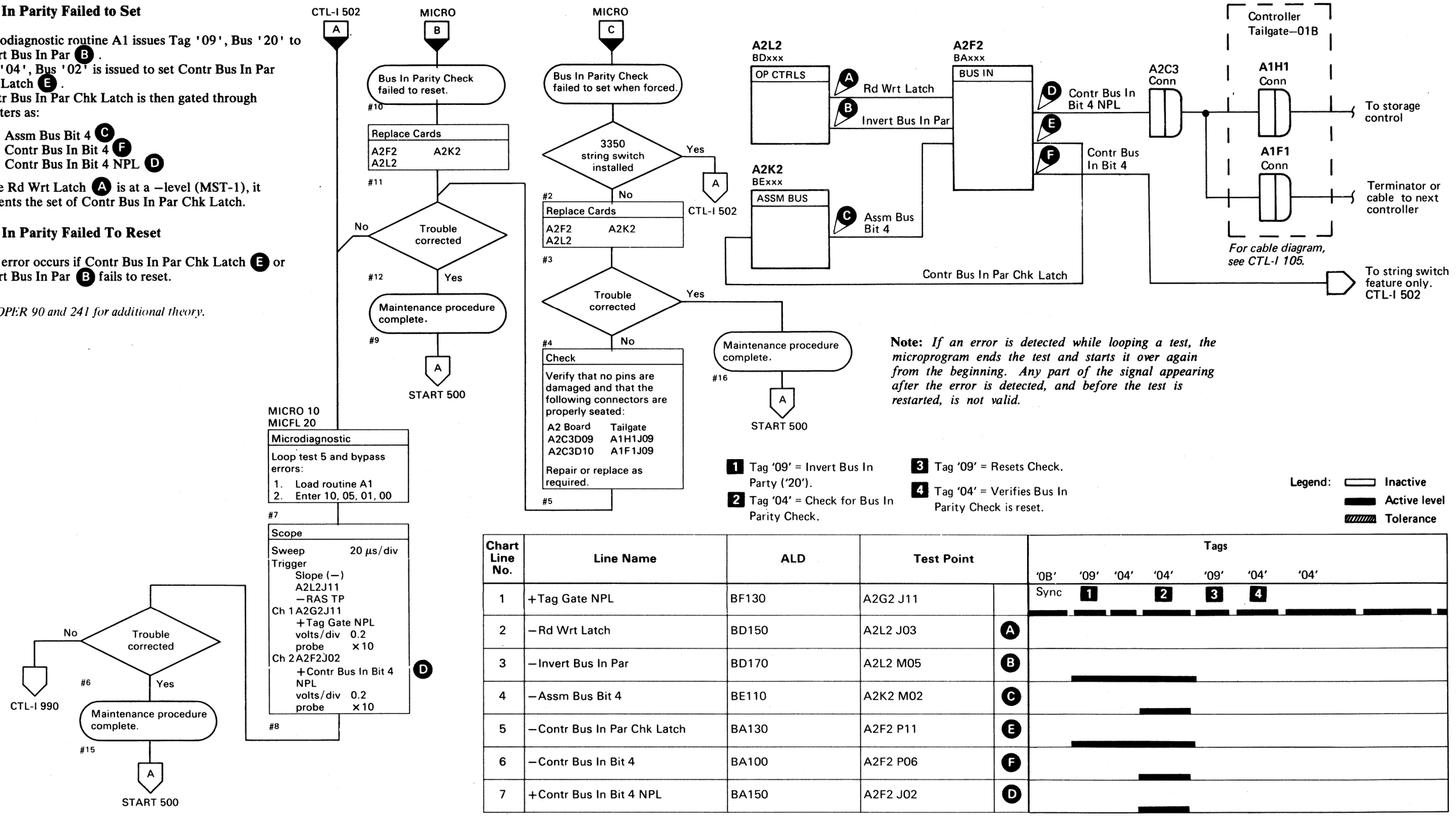
- Assm Bus Bit 4 (C)
- Contr Bus In Bit 4 (F)
- Contr Bus In Bit 4 NPL (D)

If the Rd Wrt Latch (A) is at a −level (MST-1), it prevents the set of Contr Bus In Par Chk Latch.

Bus In Parity Failed To Reset

This error occurs if Contr Bus In Par Chk Latch (E) or Invert Bus In Par (B) fails to reset.

See OPER 90 and 241 for additional theory.



Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

1. Tag '09' = Invert Bus In Party ('20').
2. Tag '04' = Check for Bus In Parity Check.
3. Tag '09' = Resets Check.
4. Tag '04' = Verifies Bus In Parity Check is reset.

Legend: Inactive; Active level; Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags: '0B'	'09'	'04'	'04'	'09'	'04'	'04'
1	+Tag Gate NPL	BF130	A2G2 J11		Sync	1		2	3	4	
2	−Rd Wrt Latch	BD150	A2L2 J03	A							
3	−Invert Bus In Par	BD170	A2L2 M05	B							
4	−Assm Bus Bit 4	BE110	A2K2 M02	C							
5	−Contr Bus In Par Chk Latch	BA130	A2F2 P11	E							
6	−Contr Bus In Bit 4	BA100	A2F2 P06	F							
7	+Contr Bus In Bit 4 NPL	BA150	A2F2 J02	D							

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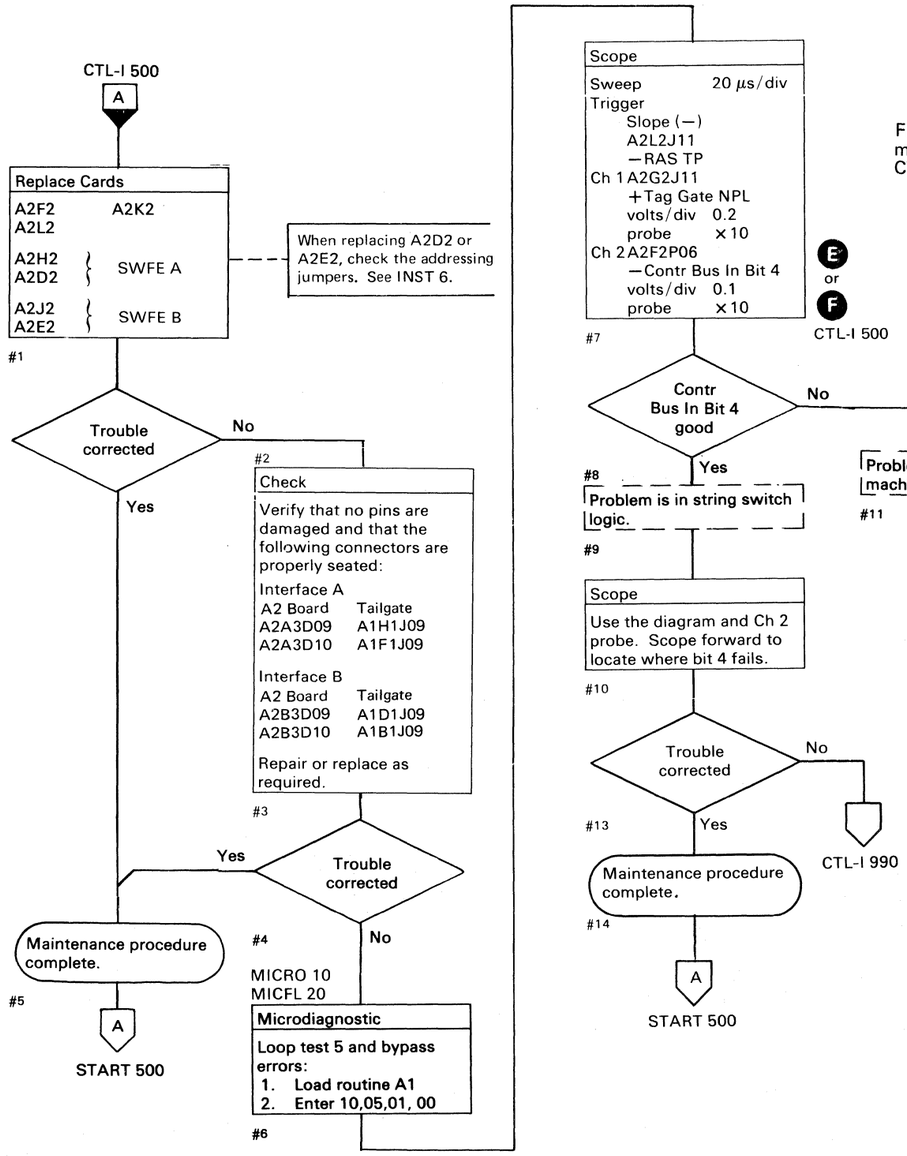
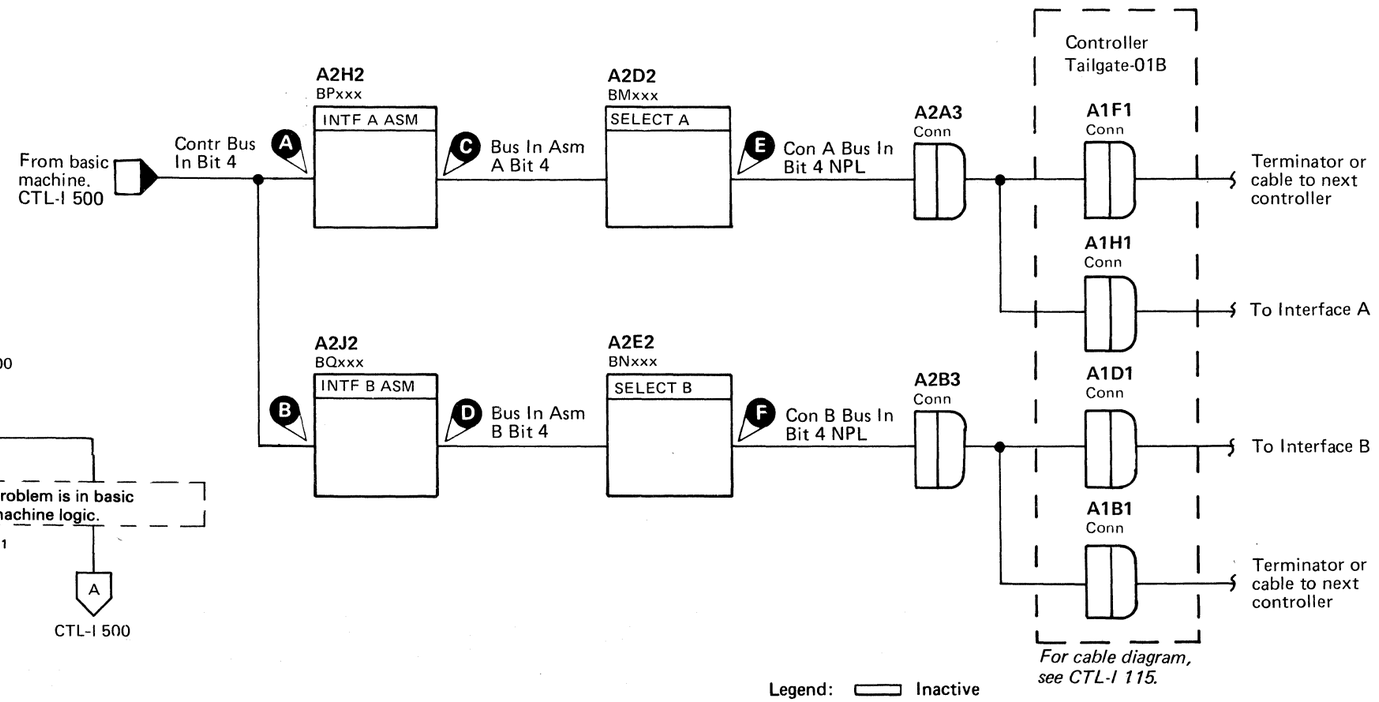
BUS IN PARITY CHECK (With String Switch)

See OPER 241 for theory.





Legend: Inactive
Active level
Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags '0B' '09' '04' '04' '09' '04'
1	+Tag Gate NPL	BF130	A2G2J11		Sync 1 2 3 4
2	−Contr Bus In Bit 4	BP200	A2H2 D06	A	
3	−Bus In Asm A Bit 4	BP200	A2H2 B07	C	
4	+Con A Bus In Bit 4 NPL	BM160	A2D2 S07	E	
5	−Contr Bus In Bit 4	BQ200	A2J2 D06	B	
6	−Bus In Asm B Bit 4	BQ200	A2J2 B07	D	
7	+Con B Bus In Bit 4 NPL	BN160	A2E2 S07	F	

1 Tag '09' = Invert Bus In Parity ('20').
2 Tag '04' = Check for Bus In Parity Check.
3 Tag '09' = Resets Check.
4 Tag '04' = Verifies Bus In Parity Check is reset.

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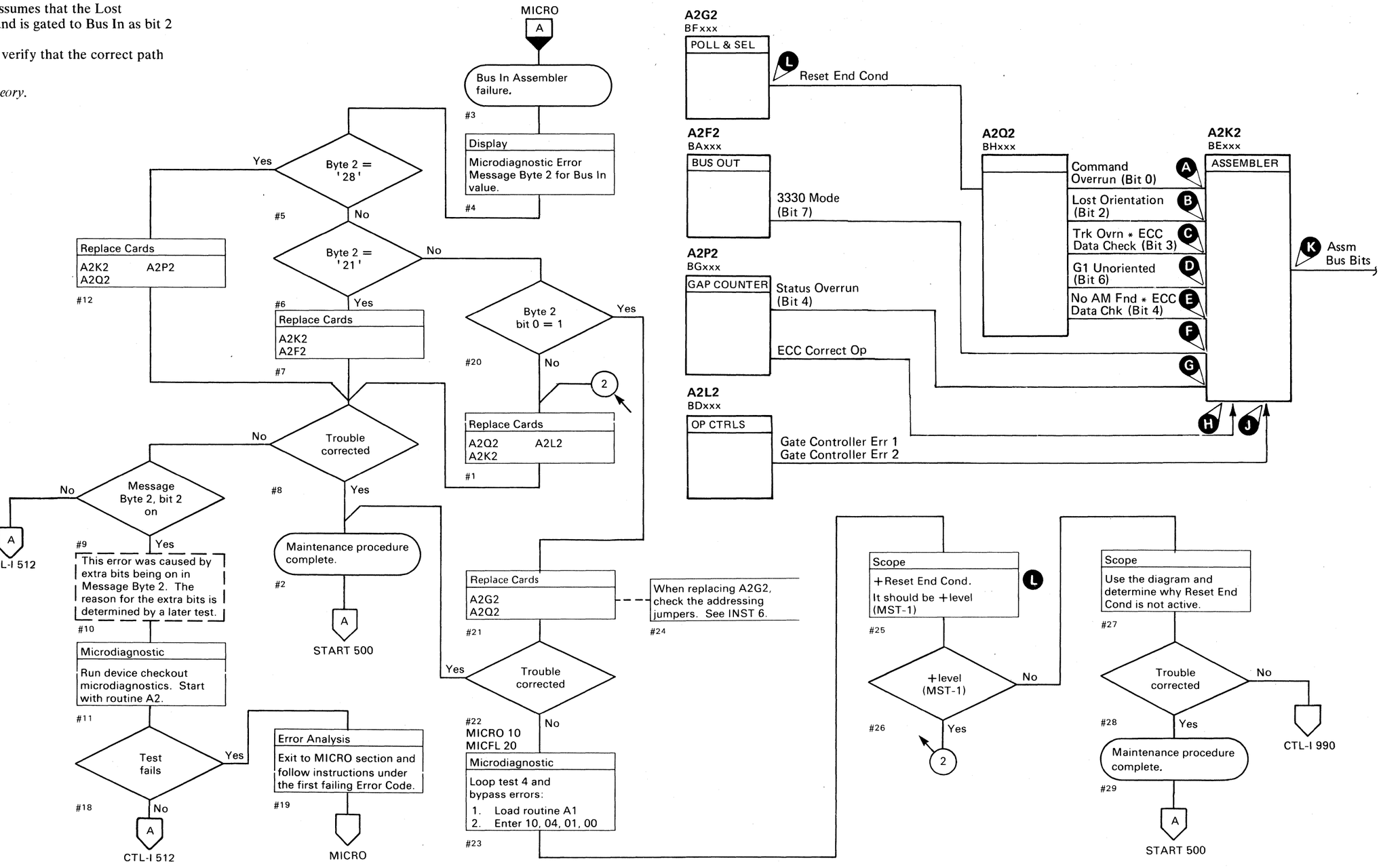
BUS IN ASSEMBLER FAILURE

The Bus In Assembler test assumes that the Lost Orientation latch (B) is on and is gated to Bus In as bit 2 (K). All other bits are off.
The purpose of the test is to verify that the correct path to Bus In exists.

See OPER 90 for additional theory.



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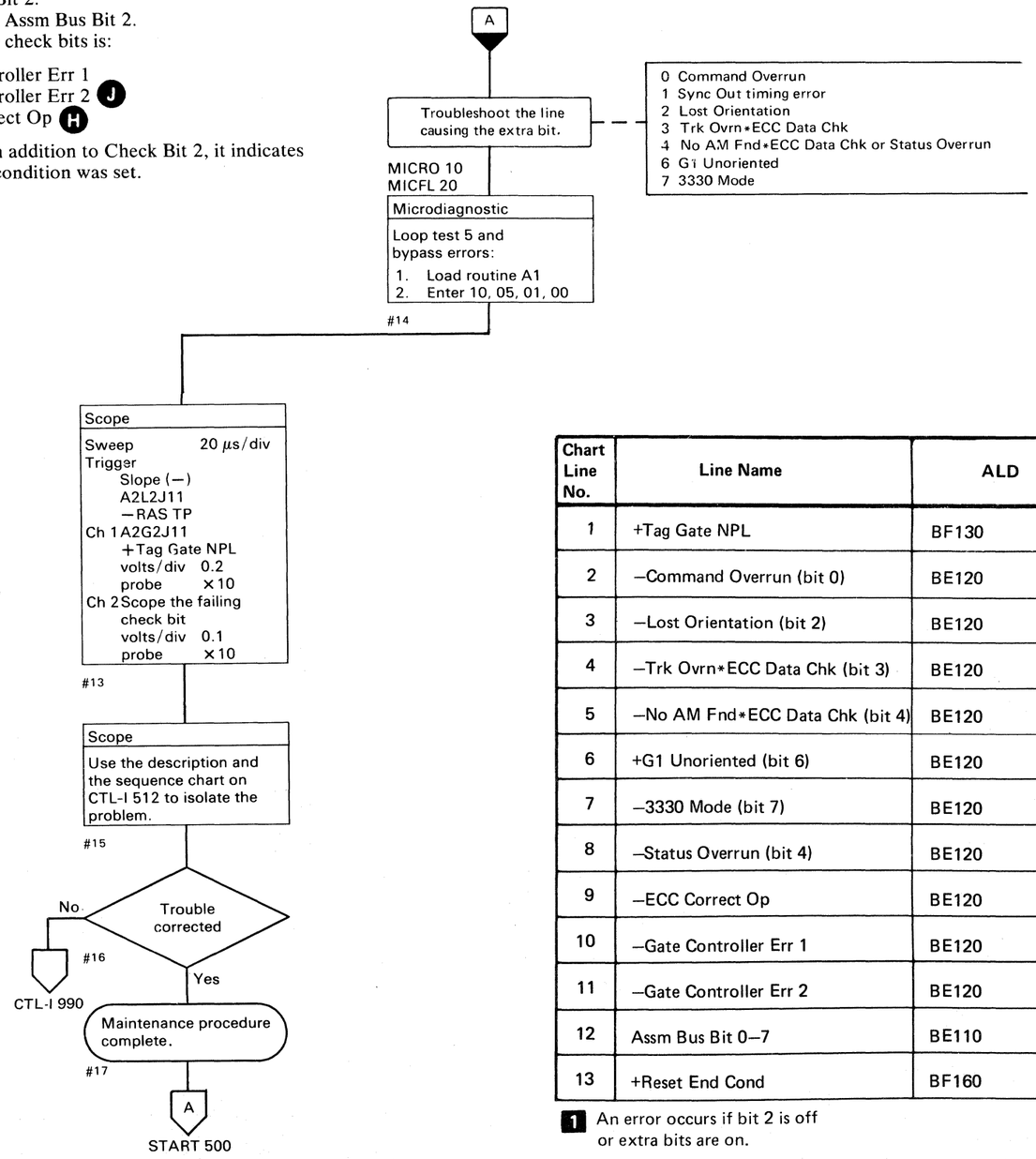
BUS IN ASSEMBLER FAILURE

The Lost Orientation Latch (B) is set, and with proper gating it sets Check Bit 2.
Check Bit 2 turns on Assm Bus Bit 2.
Proper gating for the check bits is:

Not Gate Controller Err 1
Not Gate Controller Err 2 (J)
Not ECC Correct Op (H)

If other bits are on in addition to Check Bit 2, it indicates an erroneous check condition was set.



Legend: Inactive / Active level / Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags '0B' '04' '04'
1	+Tag Gate NPL	BF130	A2G2 J11		Sync 1
2	−Command Overrun (bit 0)	BE120	A2K2 S03	A	Inactive
3	−Lost Orientation (bit 2)	BE120	A2K2 U05	B	
4	−Trk Ovrn*ECC Data Chk (bit 3)	BE120	A2K2 U09	C	Inactive
5	−No AM Fnd*ECC Data Chk (bit 4)	BE120	A2K2 G03	E	Inactive
6	+G1 Unoriented (bit 6)	BE120	A2K2 B03	D	(Sweep changed to 50 μsec/div)
7	−3330 Mode (bit 7)	BE120	A2K2 G04	F	Inactive
8	−Status Overrun (bit 4)	BE120	A2K2 J06	G	Inactive
9	−ECC Correct Op	BE120	A2K2 U07	H	Inactive
10	−Gate Controller Err 1	BE120	A2K2 M05	J	
11	−Gate Controller Err 2	BE120	A2K2 M03	J	
12	Assm Bus Bit 0−7	BE110		K	Inactive
13	+Reset End Cond	BF160	A2G2 G05	L	Inactive

1 An error occurs if bit 2 is off or extra bits are on.

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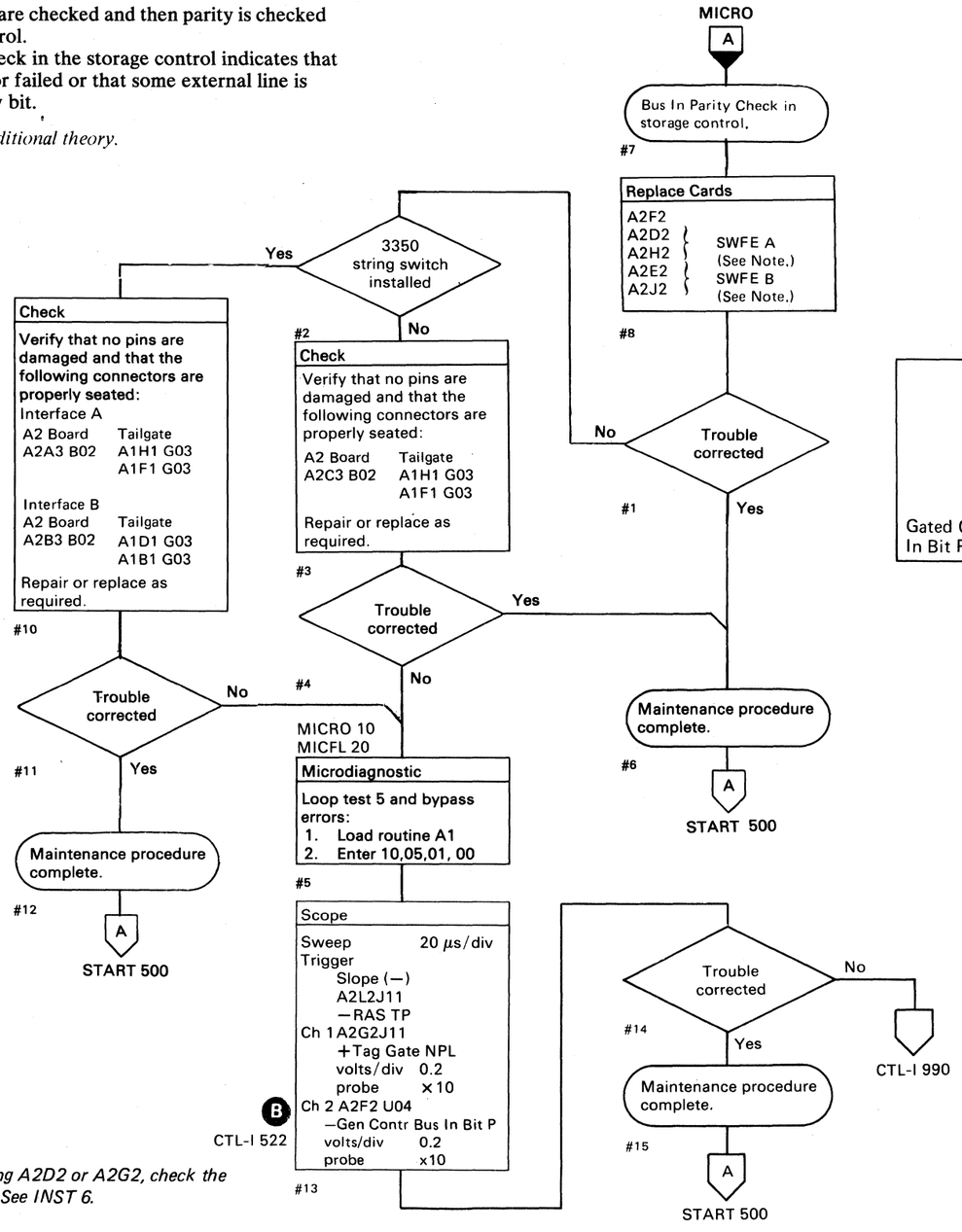
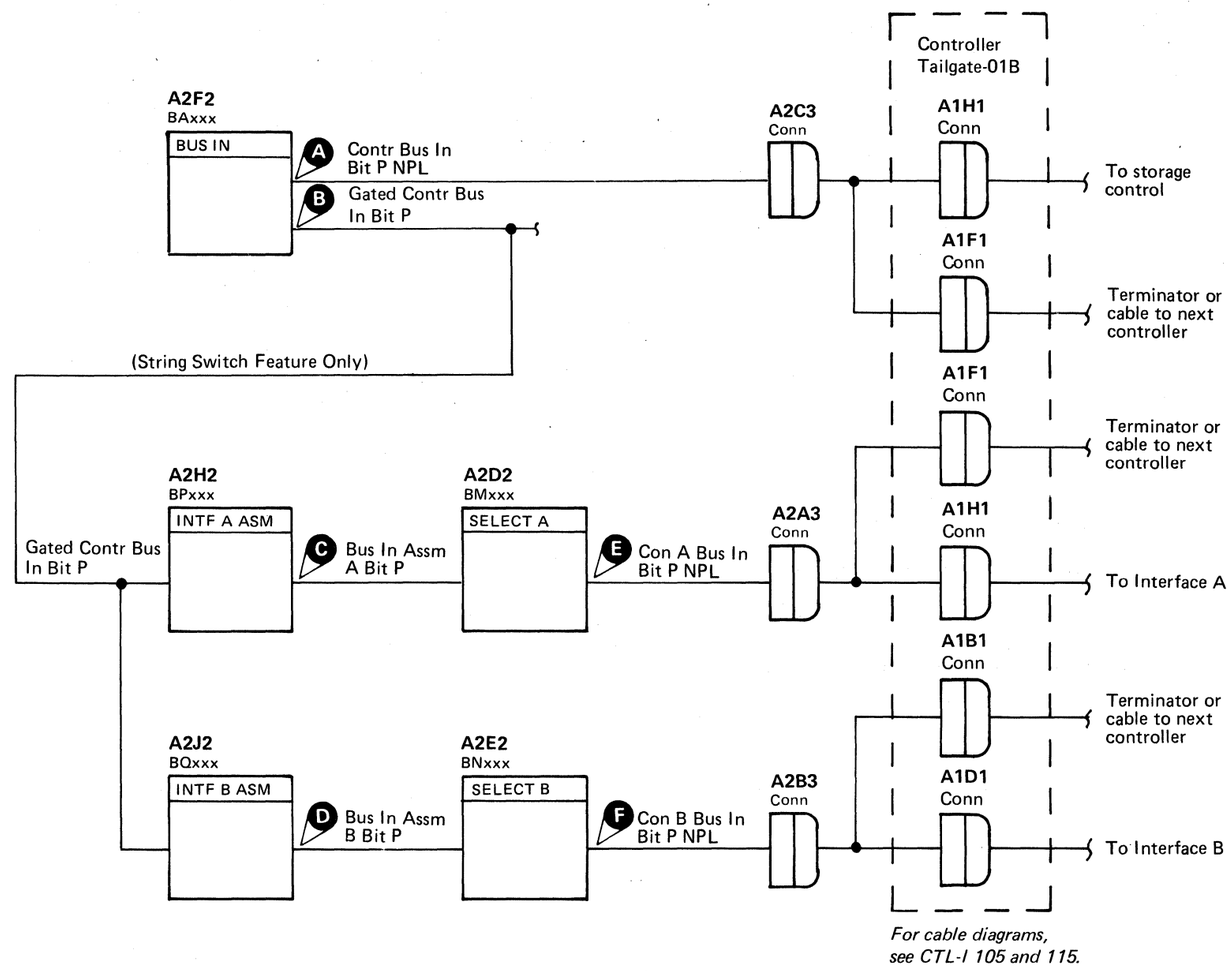
BUS IN PARITY CHECK

The bits on Bus In are checked and then parity is checked in the storage control.
A Bus In Parity check in the storage control indicates that the parity generator failed or that some external line is affecting the parity bit.

See OPER 90 for additional theory.



Note: *When replacing A2D2 or A2G2, check the addressing jumpers. See INST 6.*



For cable diagrams, see CTL-I 105 and 115.

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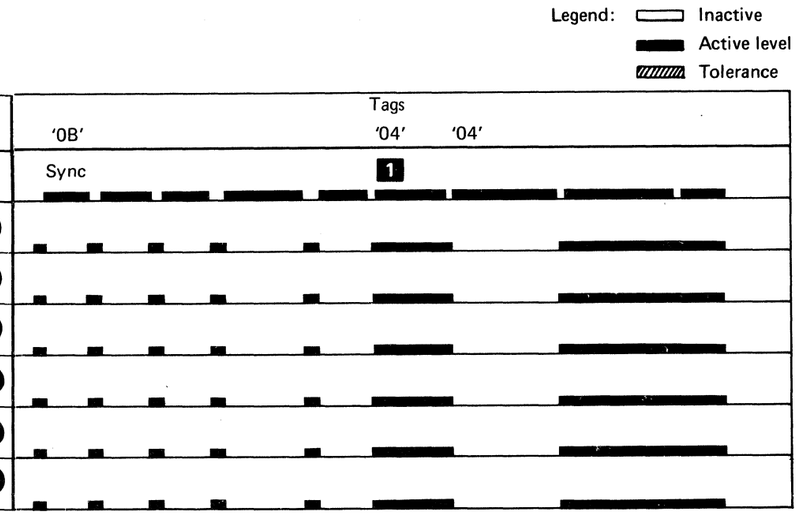
BUS IN PARITY CHECK

Note: *If an error is detected while looping a test, the microprogram terminates the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

Chart Line No.	Line Name	ALD	Test Point	
1	+Tag Gate NPL	BF130	A2G2 J11	
2	–Gated Contr Bus In Bit P	BA120	A2F2 U04	B
3	+Contr Bus In Bit P NPL	BA150	A2F2 J12	A
4	–Bus In Asm A Bit P	BP200	A2H2 D12	C
5	+Con A Bus In Bit P NPL	BM160	A2D2 M02	E
6	–Bus In Asm B Bit P	BQ200	A2J2 D12	D
7	+Con B Bus In Bit P NPL	BN160	A2E2 M02	F



1 Tag '04' = Parity is Checked.

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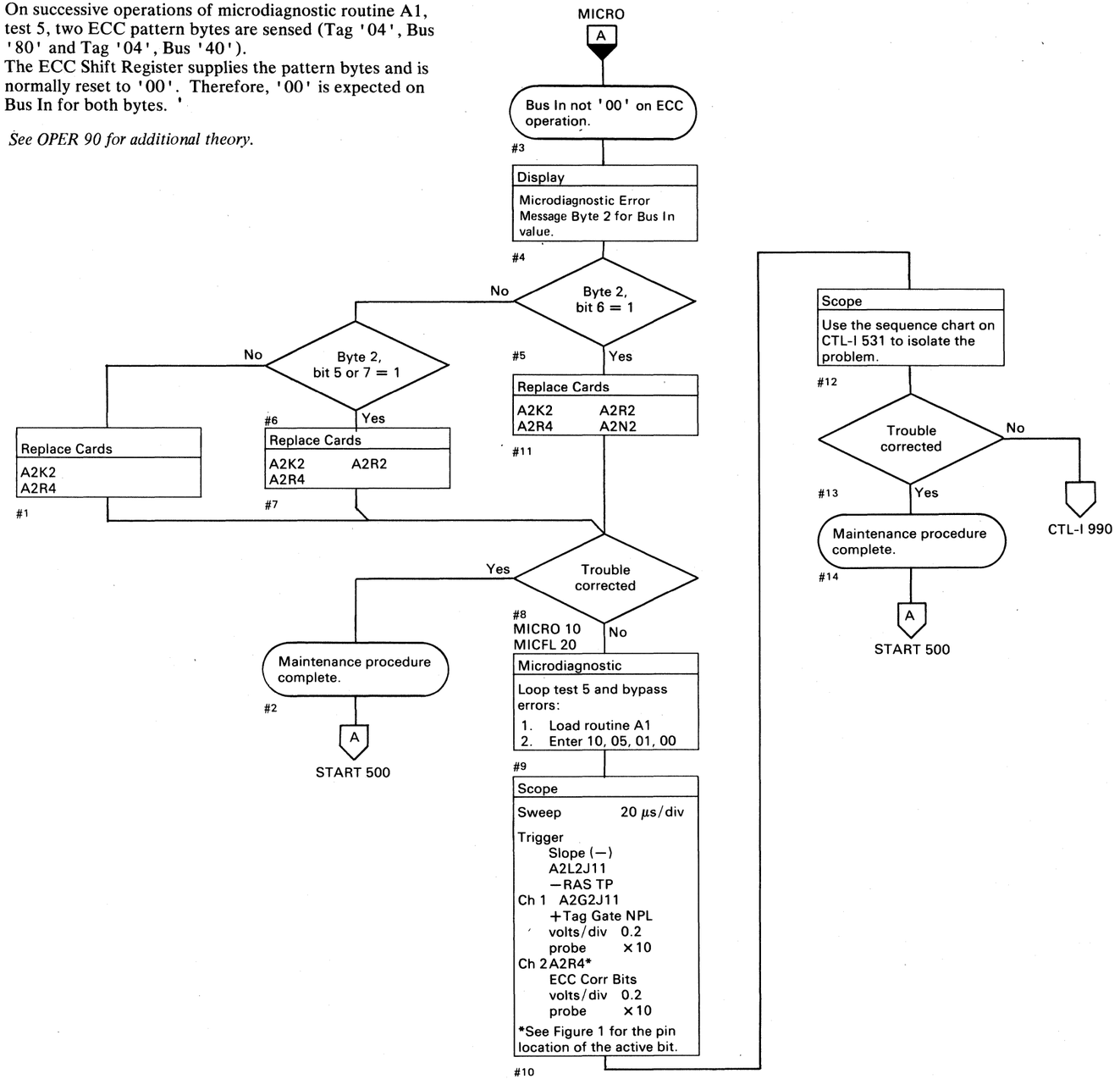
BUS IN ASSEMBLER FAILURE

On successive operations of microdiagnostic routine A1, test 5, two ECC pattern bytes are sensed (Tag '04', Bus '80' and Tag '04', Bus '40').
The ECC Shift Register supplies the pattern bytes and is normally reset to '00'. Therefore, '00' is expected on Bus In for both bytes.

See OPER 90 for additional theory.



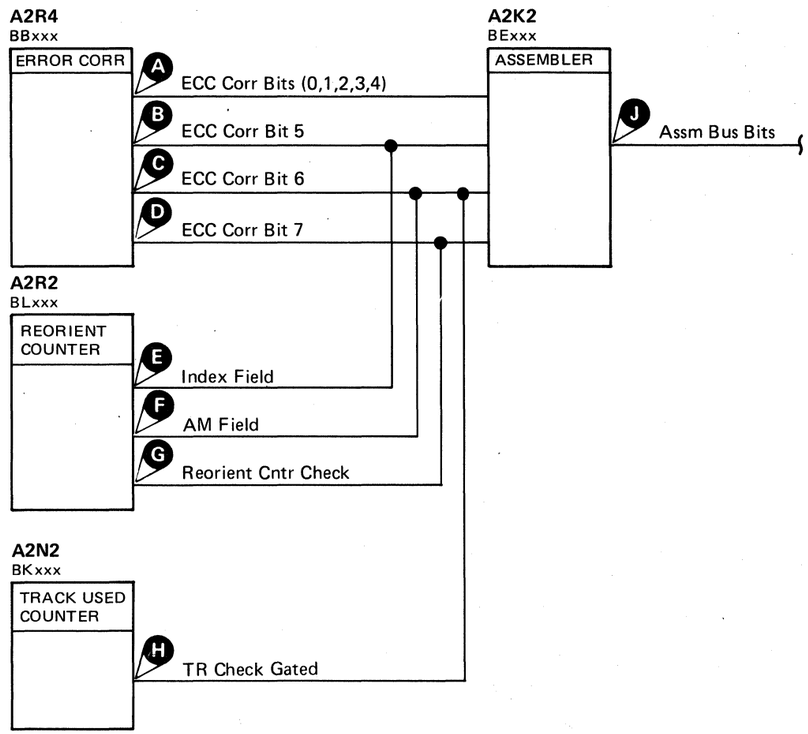


Figure 1. Pin Locations

Line Name	Card A2R4 Pins
+ECC Corr Bit 0	J04
+ECC Corr Bit 1	J13
+ECC Corr Bit 2	G09
+ECC Corr Bit 3	J06
+ECC Corr Bit 4	J05
+ECC Corr Bit 5	J03
+ECC Corr Bit 6	G03
+ECC Corr Bit 7	G13

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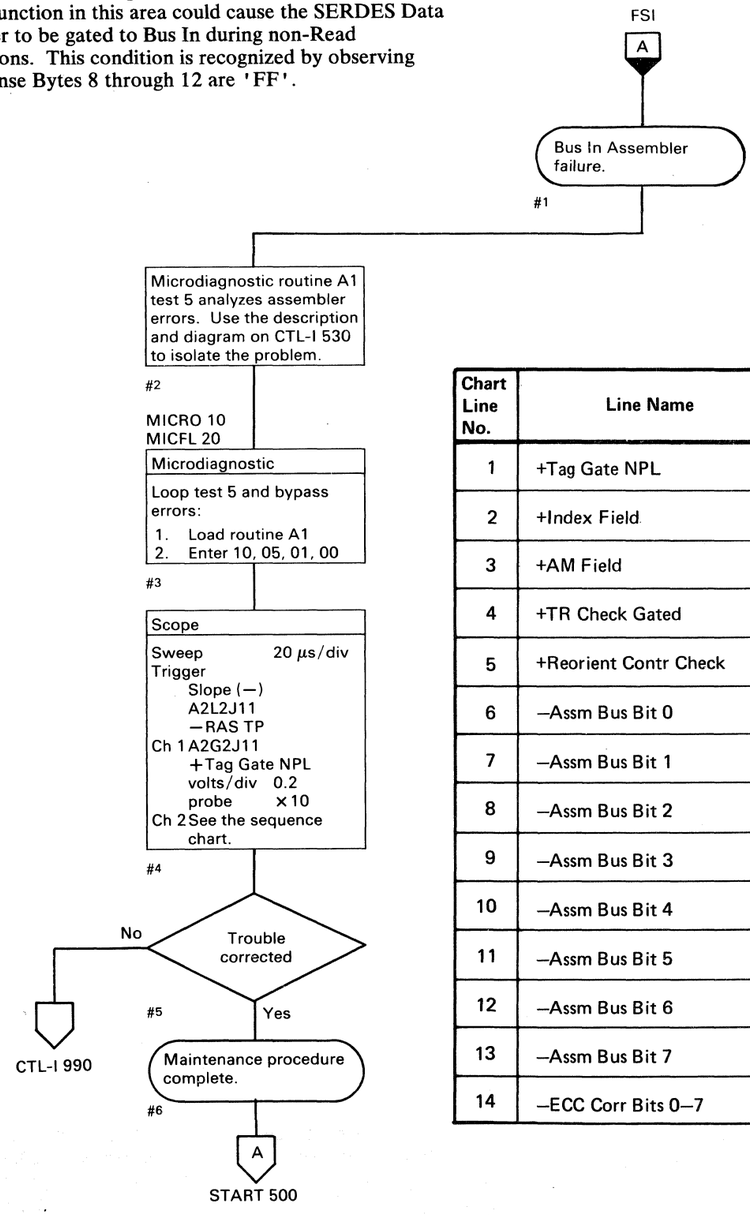
BUS IN ASSEMBLER FAILURE

To ensure data integrity on Read operations, redundant controls are on the registers that assemble the Bus In bits. A malfunction in this area could cause the SERDES Data Register to be gated to Bus In during non-Read operations. This condition is recognized by observing that Sense Bytes 8 through 12 are 'FF'.



Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags '04' '04'
1	+Tag Gate NPL	BF130	A2G2 J11		0B Sync 1 2
2	+Index Field	BL130	A2R2 J04	E	Inactive
3	+AM Field	BL130	A2R2 G02	F	Inactive
4	+TR Check Gated	BK140	A2N2 B04	H	Inactive
5	+Reorient Contr Check	BL120	A2R2 G04	G	Inactive
6	—Assm Bus Bit 0	BE110	A2K2 M07	J	
7	—Assm Bus Bit 1	BE110	A2K2 M09		
8	—Assm Bus Bit 2	BE110	A2K2 S11		
9	—Assm Bus Bit 3	BE110	A2K2 S13		
10	—Assm Bus Bit 4	BE110	A2K2 M02		
11	—Assm Bus Bit 5	BE110	A2K2 M04		
12	—Assm Bus Bit 6	BE110	A2K2 M11		
13	—Assm Bus Bit 7	BE110	A2K2 M13		
14	—ECC Corr Bits 0—7	BB160-170	See Figure 1 on CTL-I 530		Inactive

1 Check for '00' on Bus In.
If Bus In is not '00', Error Code A155 occurs.

2 Check for '00' on Bus In.
If Bus In is not '00', Error Code A156 occurs.

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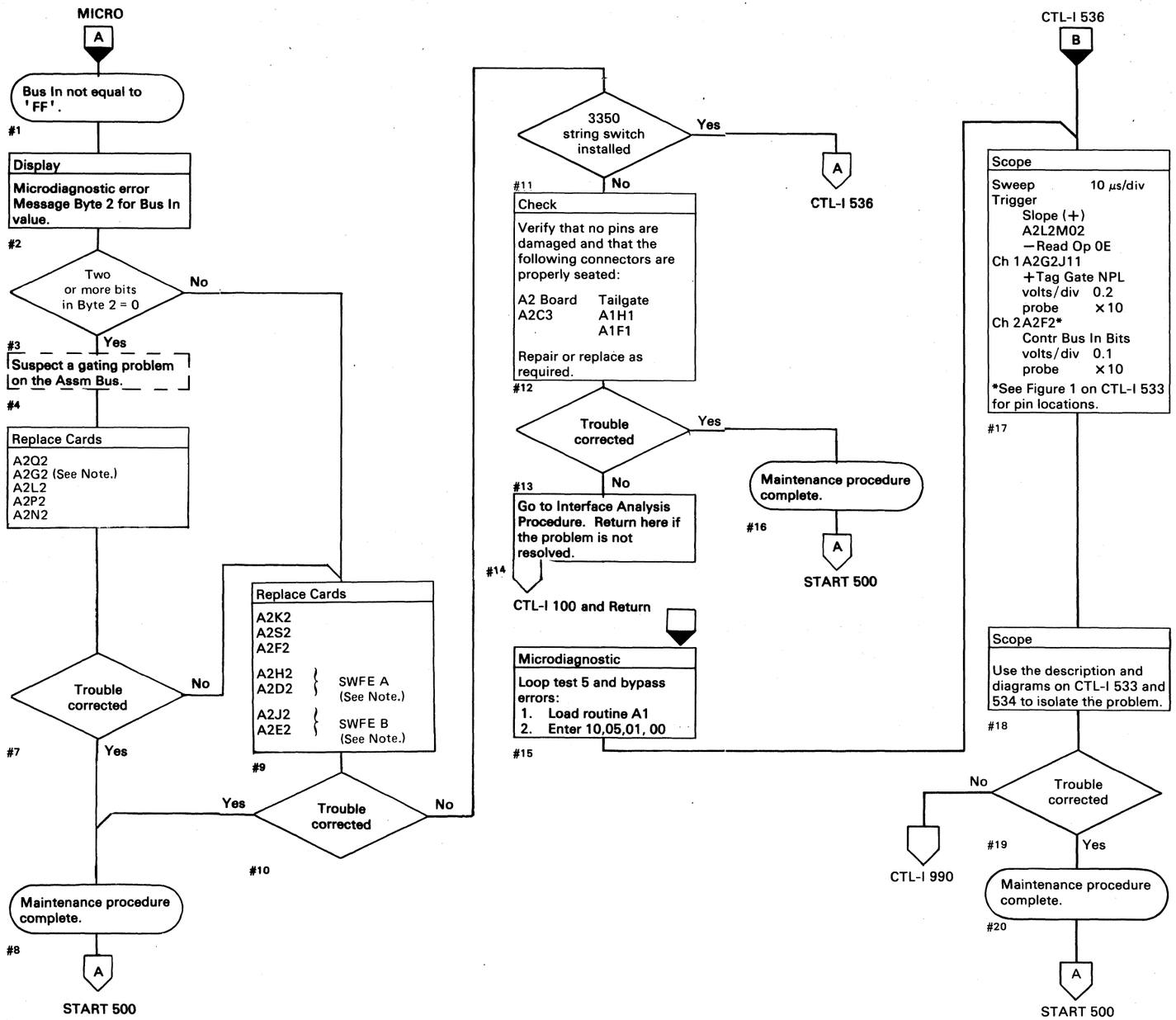
BUS IN ASSEMBLER FAILURE

Microdiagnostic routine A1 resets the Data Register to all ones ('FF').
Read Tag '0E' is then issued.
Approximately 2 microseconds after Tag Gate drops, Bus In is checked to verify that the Data Register contains 'FF'.



Note: *When replacing A2D2, A2E2, or A2G2, check the addressing jumpers. See INST 6.*

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BUS IN ASSEMBLER FAILURE

See the sequence diagram on CTL-I 534.
See OPER 90 for theory.

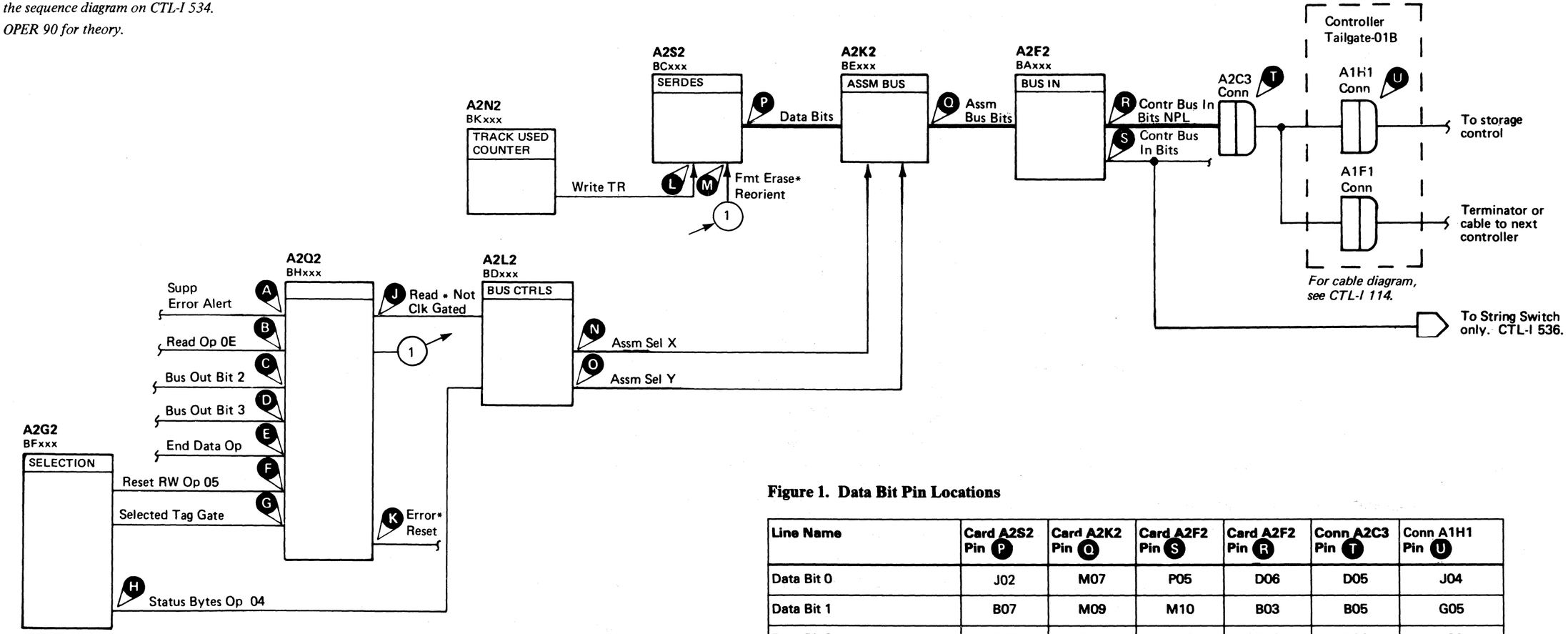

Figure 1. Data Bit Pin Locations

Line Name	Card A2S2 Pin (P)	Card A2K2 Pin (Q)	Card A2F2 Pin (S)	Card A2F2 Pin (R)	Conn A2C3 Pin (T)	Conn A1H1 Pin (U)
Data Bit 0	J02	M07	P05	D06	D05	J04
Data Bit 1	B07	M09	M10	B03	B05	G05
Data Bit 2	D06	S11	M08	D10	D06	J06
Data Bit 3	G02	S13	S07	D09	B08/B09	G08
Data Bit 4	B10	M02	P06	J02	D09/D10	J09
Data Bit 5	D09	M04	U03	J07	B10	G10
Data Bit 6	D10	M11	P09	J11	D11	J11
Data Bit 7	J03	M13	U06	J03	B12	G12

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BUS IN ASSEMBLER FAILURE

See the diagram on CTL-I 533 for referenced test points.

Normal Operation

During normal operation of the Bus In Assembler while running microdiagnostic routine A1, the following occurs:

The Data Bits (P) are all active ('FF') and Fmt Erase*Reorient (M) and Write TR (L) are inactive. The Data Bits are gated through the Assembler Bus when Assm Sel X (N) is active and Assm Sel Y (O) is inactive. The Assm Bus Bits (Q) feed through the Bus In card to form Contr Bus In Bits NPL (R).

The gate, Assm Sel X (N), is activated by:

Read*Not Clk Gated (J)

Read*Not Clk Gated is activated by:

RW Op
Not Dld Tag

Dld Tag is held inactive by:

Not Selected Tag Gate (G)

RW Op is activated by:

Read Op 0E (B)
Not End Data Op (E)
Not Error* Reset (K)
Not Reset Rd Op

Error*Reset is held inactive by:

Not Suppr Error Alert (A)
Not Reset RW Op 05 (F)

Reset Rd Op is held inactive by:

Rd G1
Not Bus Out Bit 2 (C)
Not Bus Out Bit 3 (D)

Assm Sel Y (O) is not active because Status Bytes Op 04 (H) is inactive.

Analysis Procedure

If one data bit is missing, scope that line to find where it is missing. See Figure 1 on CTL-I 533 for pin locations.
If more than one bit is missing, suspect a problem in the gating circuits:

Fmt Erase*Reorient
Assm Sel X
Assm Sel Y
Write TR

Note: *If an error is detected while looping a test, the microprogram ends the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected, and before the test is restarted, is not valid.*

1 Check Bus In for 'FF'. If Bus In is not 'FF', A157 Error Code occurs.

Legend: Inactive; Active level; Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags '0E' '05' '04'
1	+Tag Gate NPL	BF130	A2G2 J11		1
2	+Fmt Erase*Reorient	BC180	A2S2 B05		Inactive
3	–Write TR	BC180	A2S2 P13	L	Inactive
4	–Assm Sel Y	BE130	A2K2 J09	O	Inactive
5	–Assm Sel X	BE130	A2K2 G08	N	
6	–Read*Not Clk Gated	BD110	A2L2 P05	J	
7	–Selected Tag Gate	BH100	A2Q2 G05	G	
8	–Rd Op 0E	BH100	A2Q2 M03	B	
9	–End Data Op	BH150	A2Q2 G08	E	Inactive
10	+Error*Reset	BH100	A2Q2 S04	K	
11	–Suppr Error Alert	BH130	A2Q2 G03	A	Inactive
12	+Reset RW Op 05	BH130	A2Q2 D12	F	
13	–Bus Out Bit 2	BH100	A2Q2 B04	C	
14	–Bus Out Bit 3	BH100	A2Q2 B02	D	Inactive
15	–Status Bytes Op 4	BD110	A2L2 P11	H	

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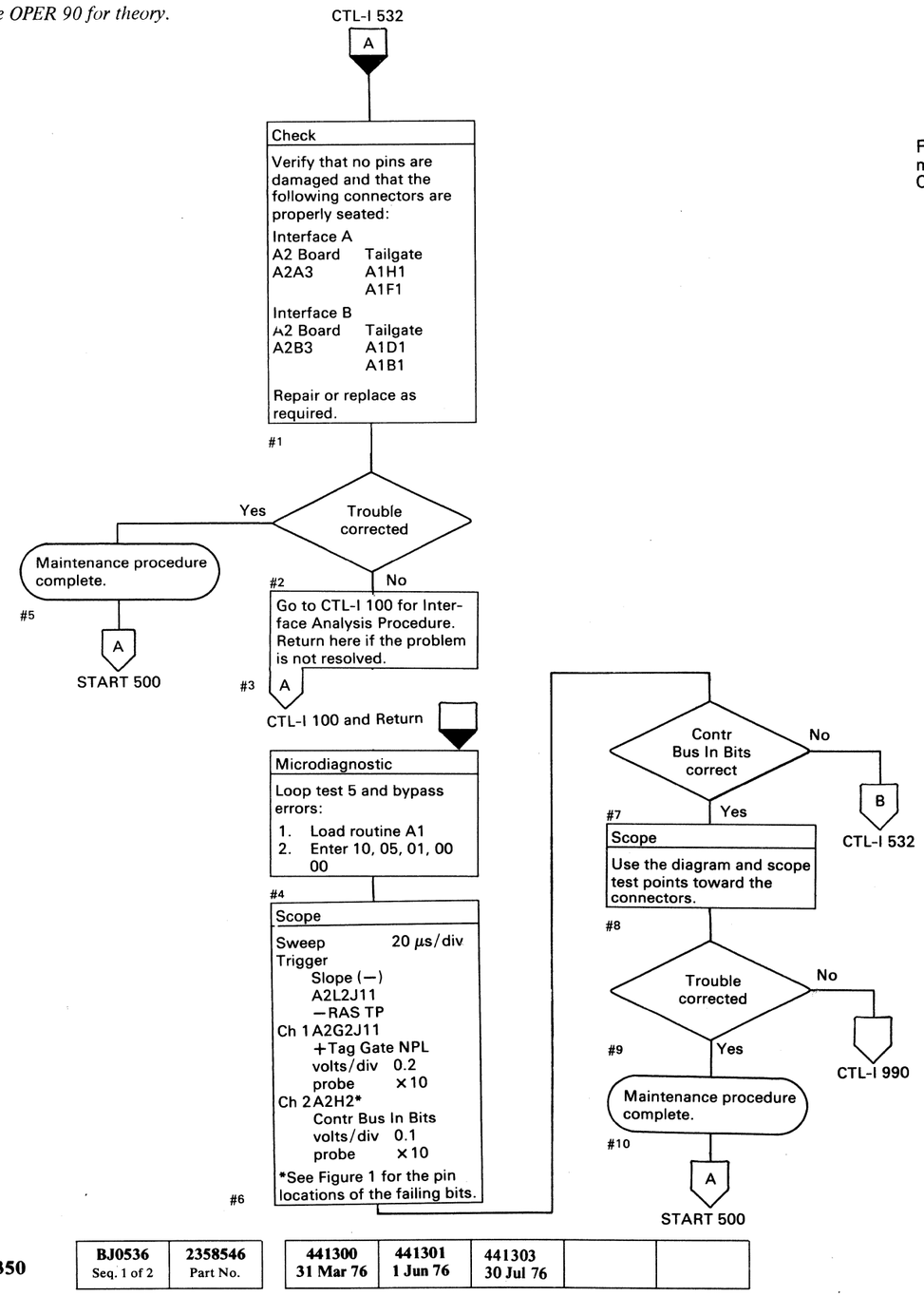
BUS IN ASSEMBLER FAILURE (With String Switch)

See OPER 90 for theory.



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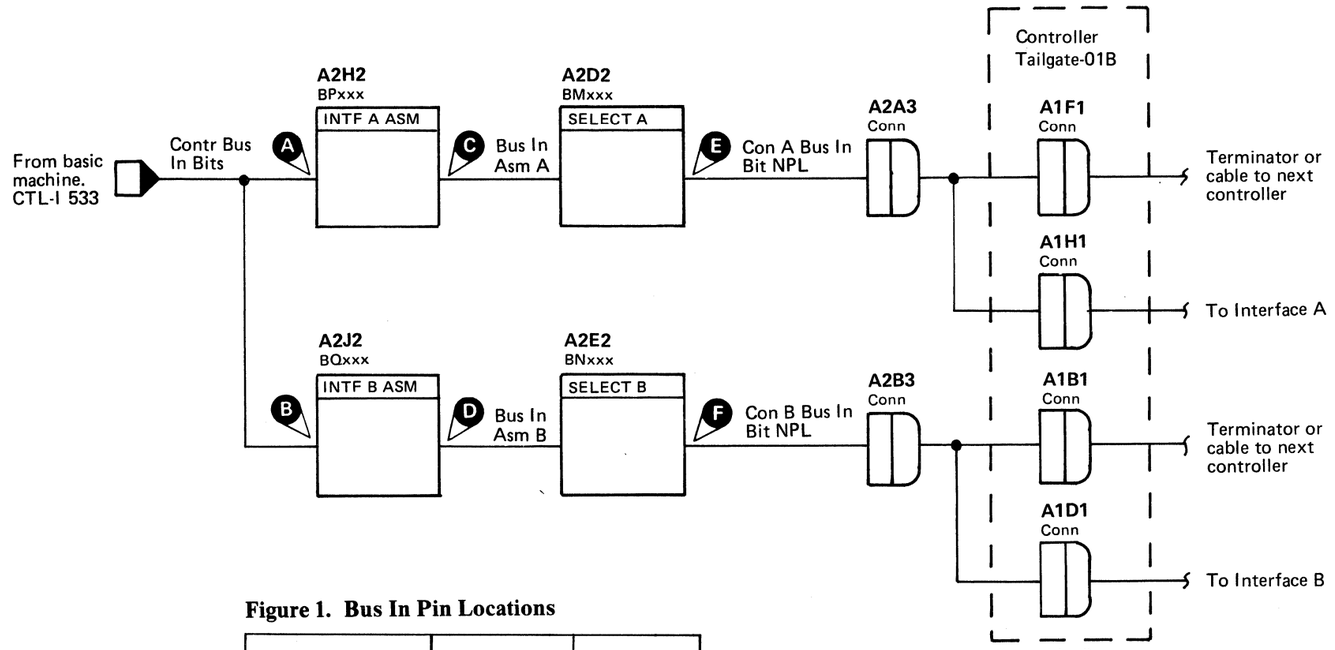


Figure 1. Bus In Pin Locations

Line Name	Card A2H2 Pin A	Card A2J2 Pin B
Contr Bus In Bit 0	G02	G02
Contr Bus In Bit 1	G05	G05
Contr Bus In Bit 2	D11	D11
Contr Bus In Bit 3	D13	D13
Contr Bus In Bit 4	D06	D06
Contr Bus In Bit 5	D10	D10
Contr Bus In Bit 6	D02	D02
Contr Bus In Bit 7	B05	B05

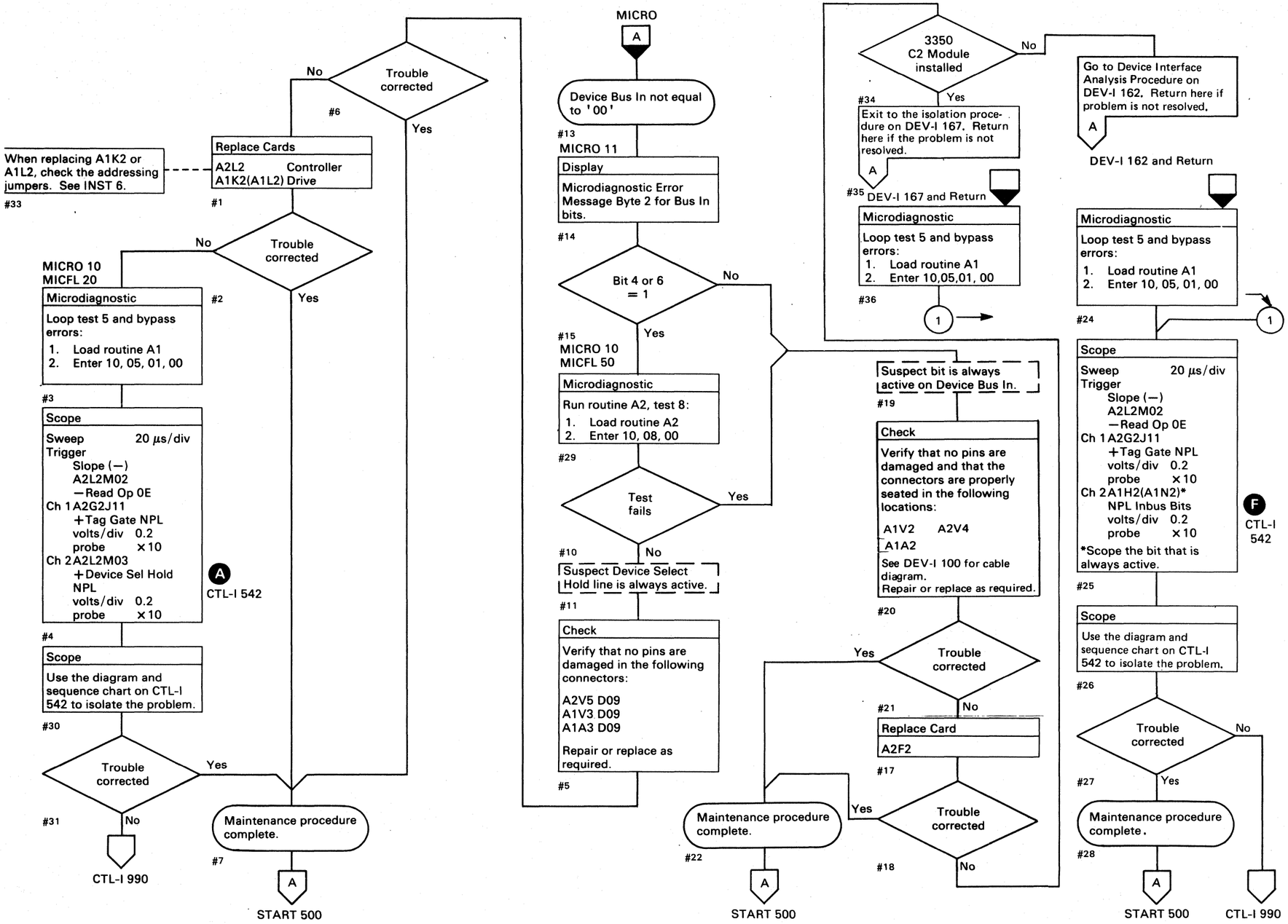
DEVICE BUS IN FAILURE

See the diagram on CTL-I 542 for referenced test points.

The microdiagnostic issues Tag '84' which gates the Device Bus In bits (C) to the storage control. All bits should be 0.

If bit 4 or 6 is on, Device Select Hold (A) may be active. This causes the erroneous selection of a drive.

If a drive is selected when Tag '84' is issued, bit 4 (On Line) or bit 6 (Busy) is active.



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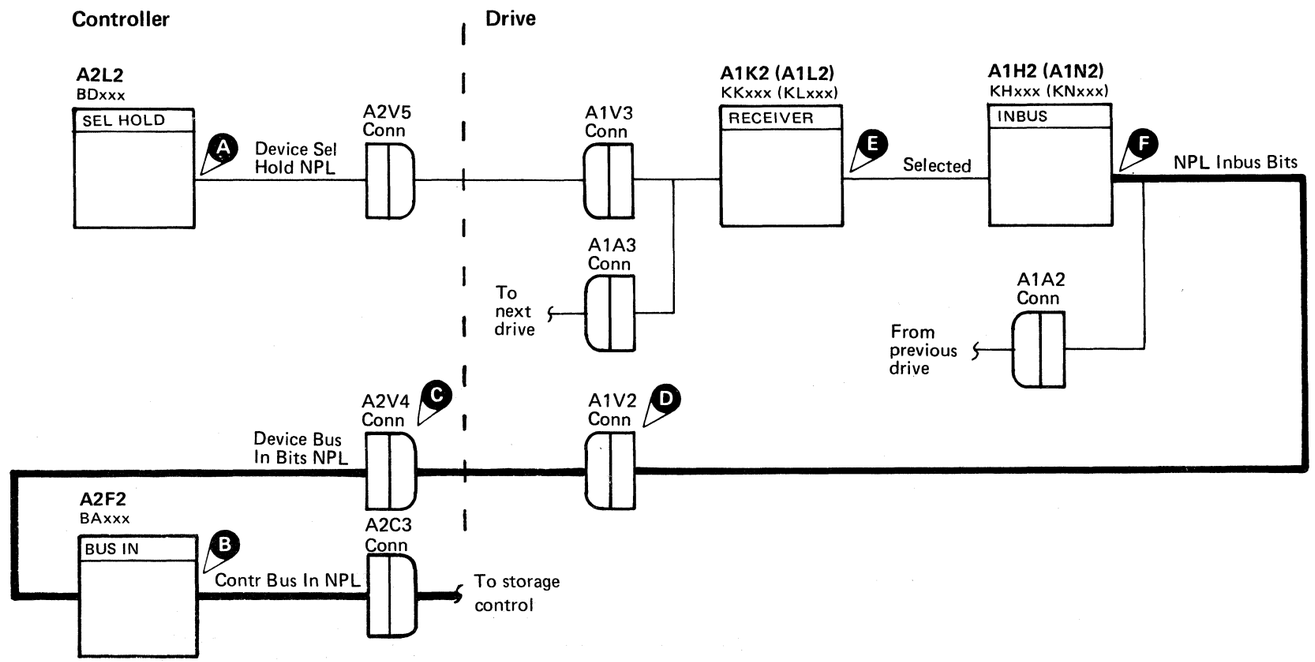
DEVICE BUS IN FAILURE

See OPER 20 for theory.

Figure 1. Connector Pin Locations

Line Name	Conn A2V5 Pin	Conn A1V3 Pin	Conn A2V4 Pins (C)	Conn A1V2 Pins (D)
+Device Sel Hold NPL	D09	D09	—	—
+Device Bus In Bit 0 NPL			B02	B02
+Device Bus In Bit 1 NPL			B04	B04
+Device Bus In Bit 2 NPL			B05	B05
+Device Bus In Bit 3 NPL			B06	B06
+Device Bus In Bit 4 NPL			B08	B08
+Device Bus In Bit 5 NPL			B09	B09
+Device Bus In Bit 6 NPL			B10	B10
+Device Bus In Bit 7 NPL			B12	B12
+Device Bus In Bit P NPL			B13	B13



Legend: Inactive
Active level
Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags '0E' '84'
1	+Tag Gate NPL	BF130	A2G2 J11		Sync 1
2	+Device Sel Hold NPL	BD230	A2L2 M03	A	Inactive
3	+Selected	KK100 (KL100)	A1K2 (A1L2) G12	E	Inactive
4	+NPL Inbus Bits 0–7	KH200 (KN200)	A1H2 (A1N2)	F	Inactive
5	+Device Bus In Bits 0–7 NPL	BA160	A2F2	B	Inactive

1 Tag '84' checks for Device Bus In Bits = '00'.

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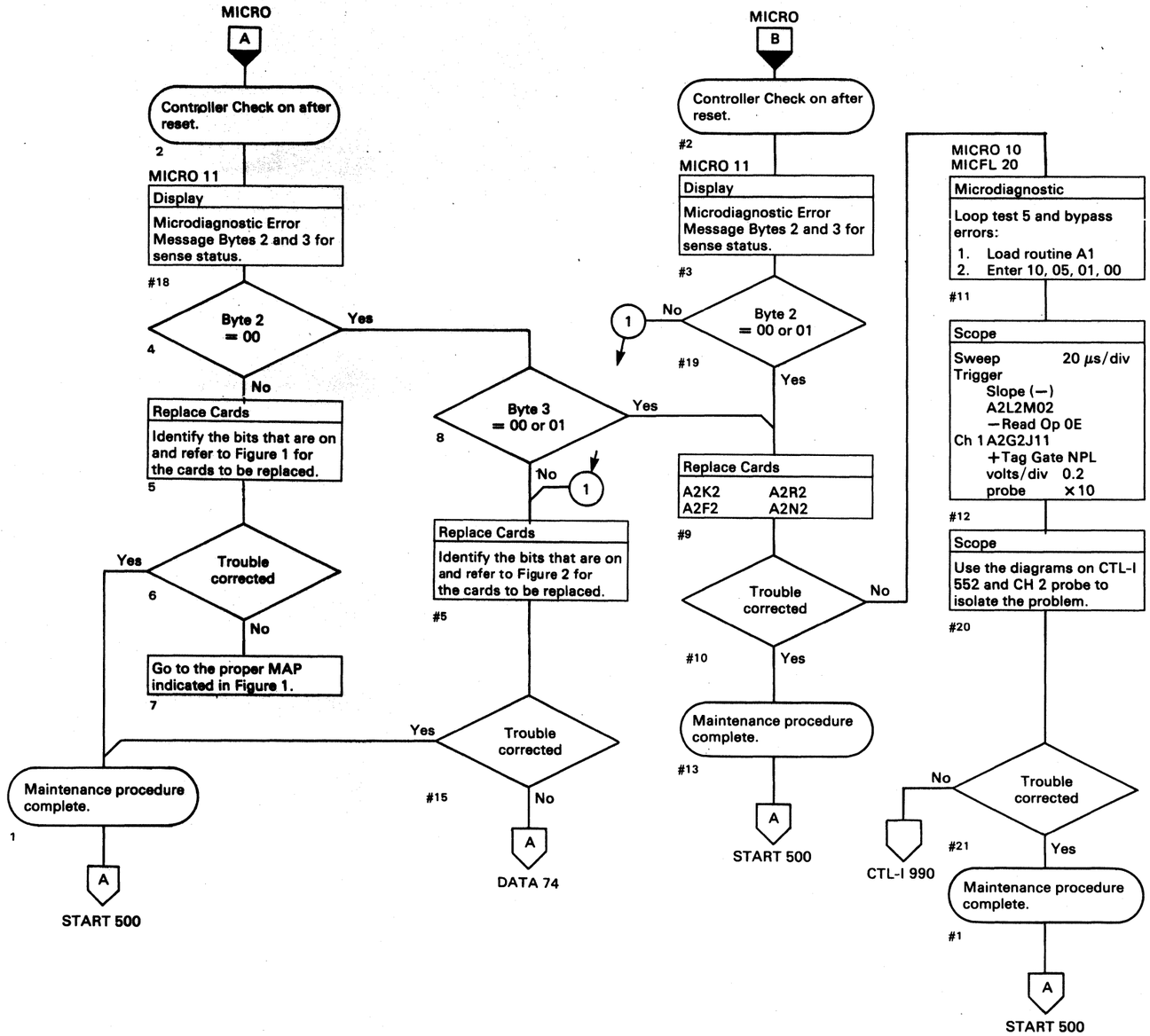

Figure 1. Sense Status – Controller Error 1

Byte 2 Bits	Error Latch	Possible Causes	MAP	
			Section	Entry
0	Tag Bus Parity Check	A2K2, A2G2*	CTL-I 410	A
1	Bus Out Parity Check	A2K2, A2G2*	CTL-I 410	B
2	Drive Select Error	A2G2*, A2K2	DEV-I 112	A
3	Device Bus In Parity	A2F2, A2K2	DEV-I 160	A
4	CTL-I Bus In Parity	A2K2, A2F2	CTL-I 500	B
5	I Write Fail	A2P2, A2K2	DATA 260	A
6	Index Check	A2R2,A2N2,A2K2	DATA 260	A
7	Reorient Check	A2R2, A2K2	DATA 260	A

*When replacing A2G2, check the addressing jumpers. See INST 6.

Figure 2. Sense Status – Controller Error 2

Byte 3 Bits	Error Latch	Possible Causes	MAP	
			Section	Entry
0 1	00 = Missing Servo Input 01 = Phase Error 11 = Missing Data Input	A2S2, A2K2, A2R2 A2T2, A2Q2	DATA 260	A
2	SERDES Data Check	A2S2, A2K2		
3	Gap Counter Check	A2S2, A2P2, A2K2		
4	Write Data Check	A2S2, A2K2		
5	Monitor Check	A2L2, A2Q2, A2G2*, A2K2		
6	ECC Check	A2S2, A2P2, A2K2		

*When replacing A2G2, check the addressing jumpers. See INST 6.

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CONTROLLER CHECK AFTER RESET

The microdiagnostic issues Tag '94' to activate Tag Bus Par Chk (A). Tag Bus Par Chk then activates Controller Chk (N). Tag Bus Par Chk is reset and the microdiagnostic verifies that Controller Chk is also reset. If Controller Chk or one of the error latches (A) through (N) is still active at Tag '09' reset or Tag '84', an error occurs.

See OPER 90 for additional theory.

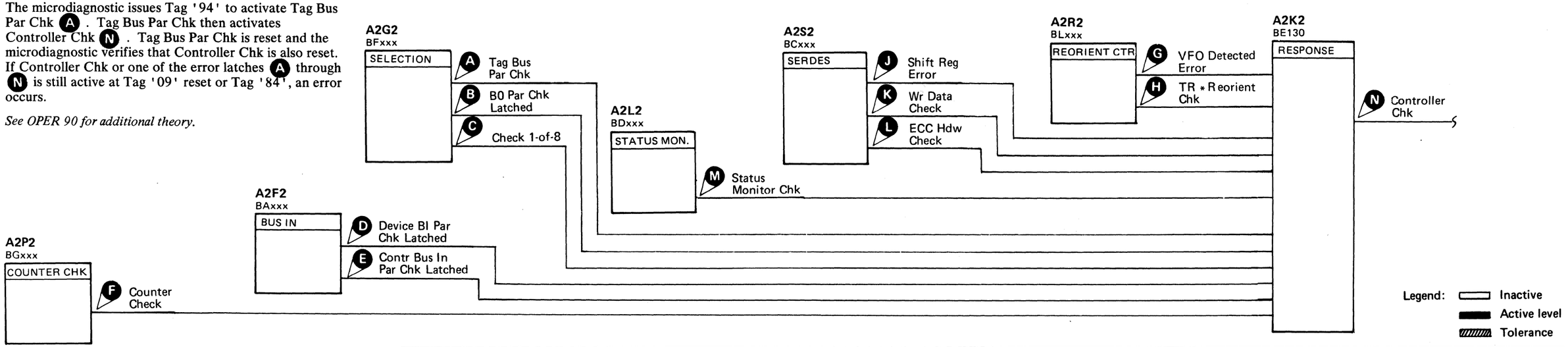


Chart Line No.	Line Name	ALD	Test Point		Tags '0E' '94' '09' '84'
1	+Tag Gate NPL	BF130	A2G2 J11		Sync 1 2 3
2	−Controller Chk	BE130	A2K2 M12	N	
3	−Tag Bus Par Chk	BF110	A2G2 G10	A	
4	−VFO Detected Error	BL140	A2R2 G05	G	
5	−TR * Reorient Chk	BL120	A2R2 J10	H	
6	−Shift Reg Error	BC110	A2S2 P02	J	
7	−Wr Data Check	BC130	A2S2 P06	K	
8	−ECC Hdw Check	BC160	A2S2 S07	L	
9	−Status Monitor Chk	BD160	A2L2 D09	M	Inactive
10	−BO Par Chk Latched	BF110	A2G2 J10	B	
11	+Check 1-of-8	BF200	A2G2 S13	C	
12	−Device BI Par Chk Latched	BA140	A2F2 M05	D	
13	−Contr Bus In Par Chk Latched	BA130	A2F2 P11	E	
14	−Counter Check	BG160	A2P2 J09	F	

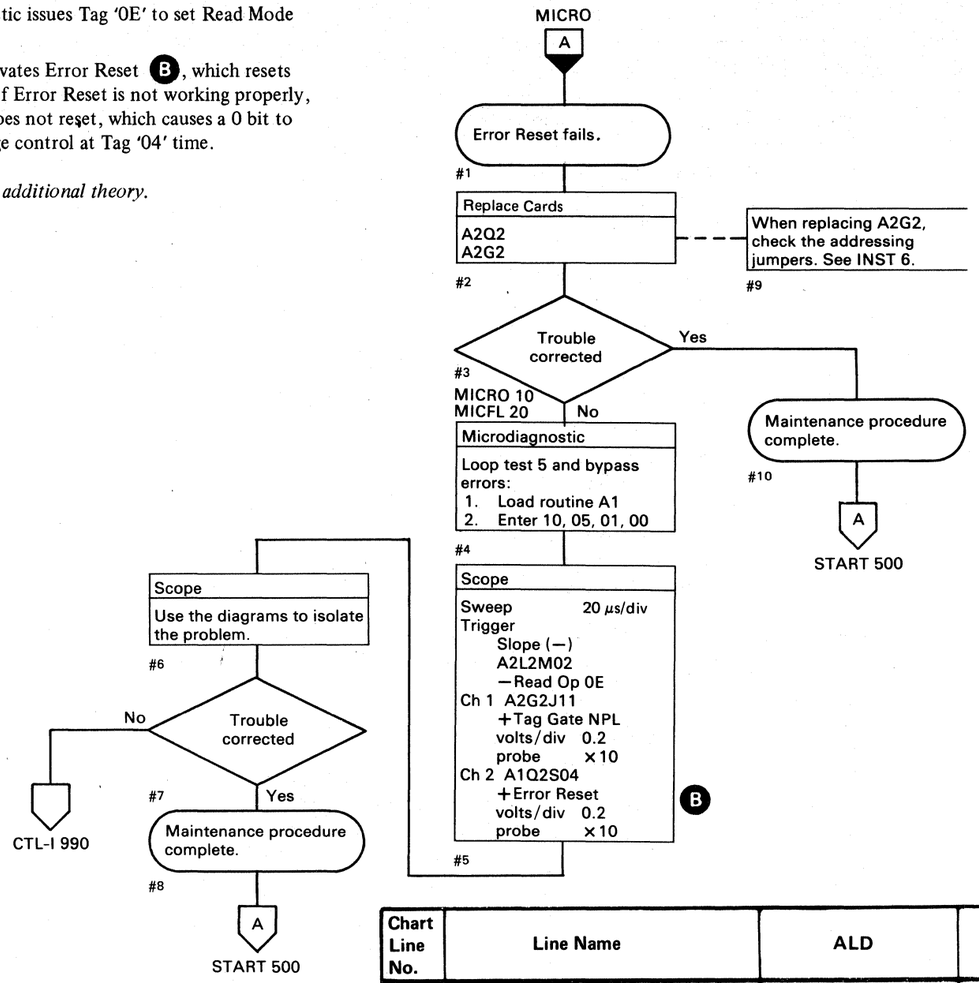
1 Tag '94' = Invalid tag, sets Controller Chk.
2 Tag '09' = Reset Controller Chk.
3 Tag '84' = Verifies that Controller Chk is reset.

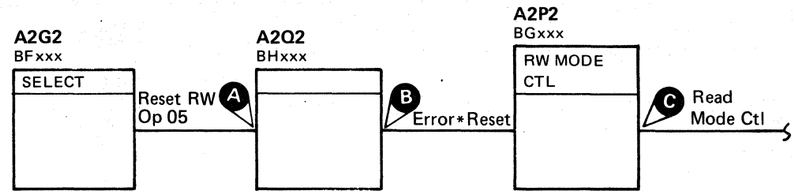
ERROR RESET FAILURE

The microdiagnostic issues Tag '0E' to set Read Mode Ctl (C).

Tag '05' then activates Error Reset (B), which resets Read Mode Ctl. If Error Reset is not working properly, Read Mode Ctl does not reset, which causes a 0 bit to be gated to storage control at Tag '04' time.

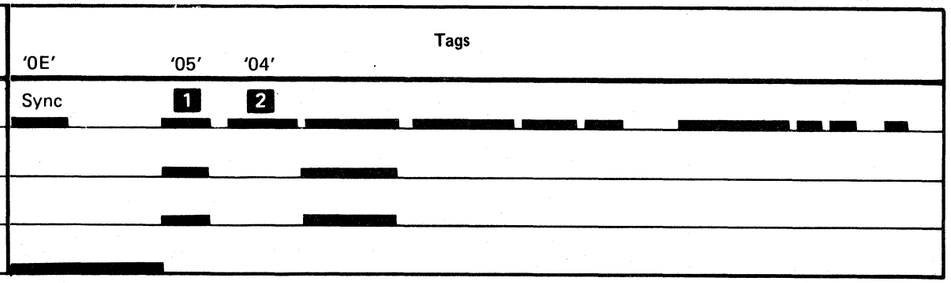
See OPER 90 for additional theory.





Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+Tag Gate NPL	BF130	A2G2 J11	
2	+Error*Reset	BH130	A2Q2 S04	B
3	+Reset RW Op 05	BH130	A2Q2 D12	A
4	—Read Mode Ctl	BG150	A2P2 D03	C



1 Tag 05 = Reset R/W

2 Tag 04 = If reset fails, Error Code A15C occurs.

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DEVICE TYPE FAILURE

At times, the storage control must determine the type of device that is attempting to communicate with it. This is accomplished with a Gate Device Type Command (Tag '0A', Bus '80').

If the addressed device can be selected, the controller responds with bits 4 and 5 on Bus In.

The device does not have to be ready.

Gated Attn Sel gates bits 4 and 5 through the Select Bus and is generated by:

Decode Tag 0A
Bus Out Bit 0
Selected
Any Attn Sel

} See ALD BF100.

Sel Bus Bit 4 activates Contr Bus In Bit 4 (B) and Bit 5 (C).

If the addressed device cannot be selected, only the parity bit appears on Bus In.

See OPER 90 for additional theory.

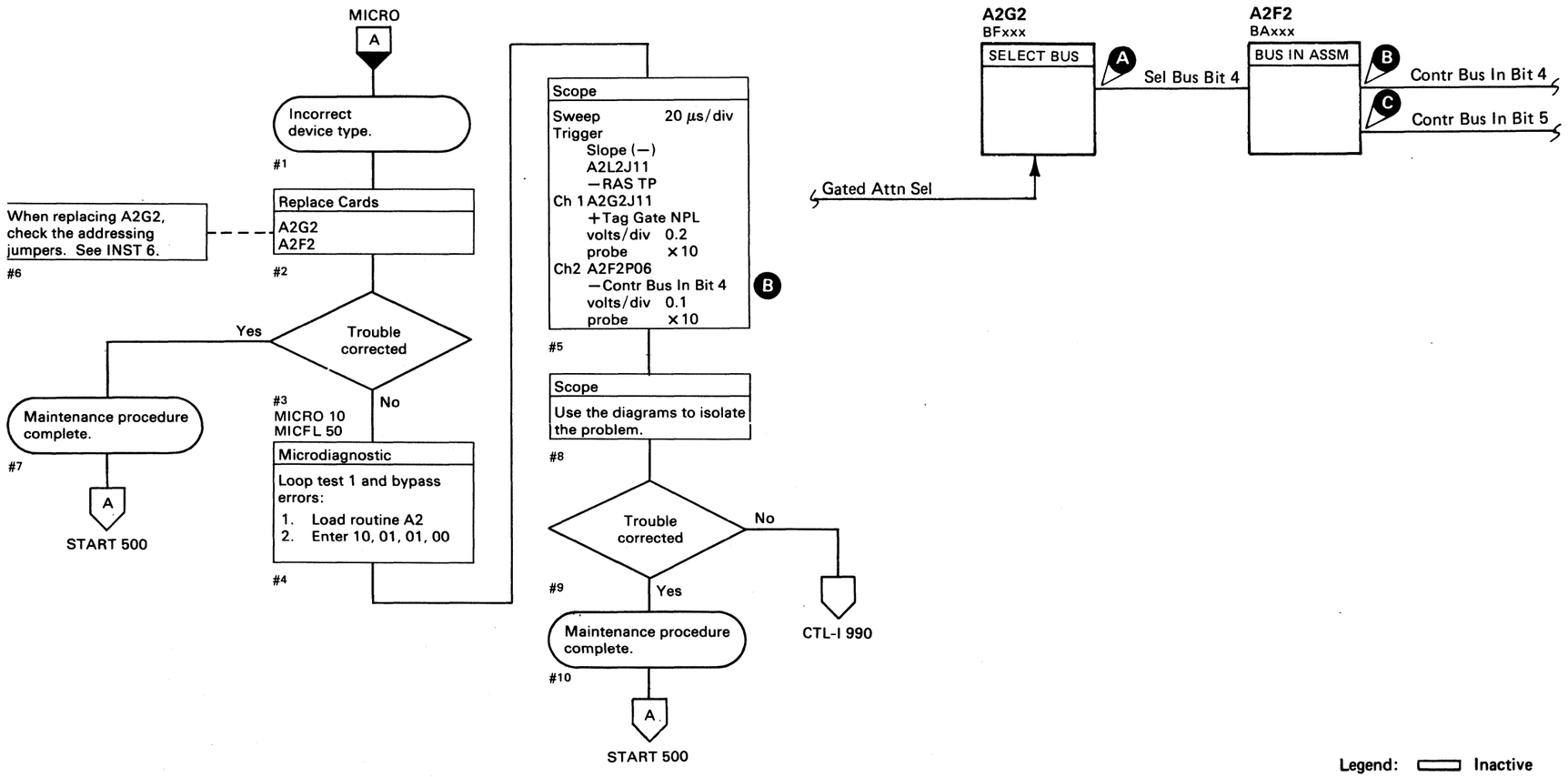

Chart Line No.	Line Name	ALD	Test Point		Tags '0B' '0A'
1	+ Tag Gate NPL	BF130	A2G2 J11		Sync 1
2	—Sel Bus Bit 4	BF190	A2G2 M13	A	
3	—Contr Bus In Bit 4	BA100	A2F2 P06	B	
4	—Contr Bus In Bit 5	BA100	A2F2 U03	C	

Legend: Inactive; Active level; Tolerance

1 Tag '0A' = Device type bit 4 and 5 must be active.

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TAG VALID FAILURE

See the diagram on CTL-I 611 for referenced test points.

Tag Valid Missing - Error Code A258

The microdiagnostic verifies that Tag Valid is received for Tag '82'. Addressing 82 (H) and Valid Tag Gate (G) activates Coerce Tag Valid (L).

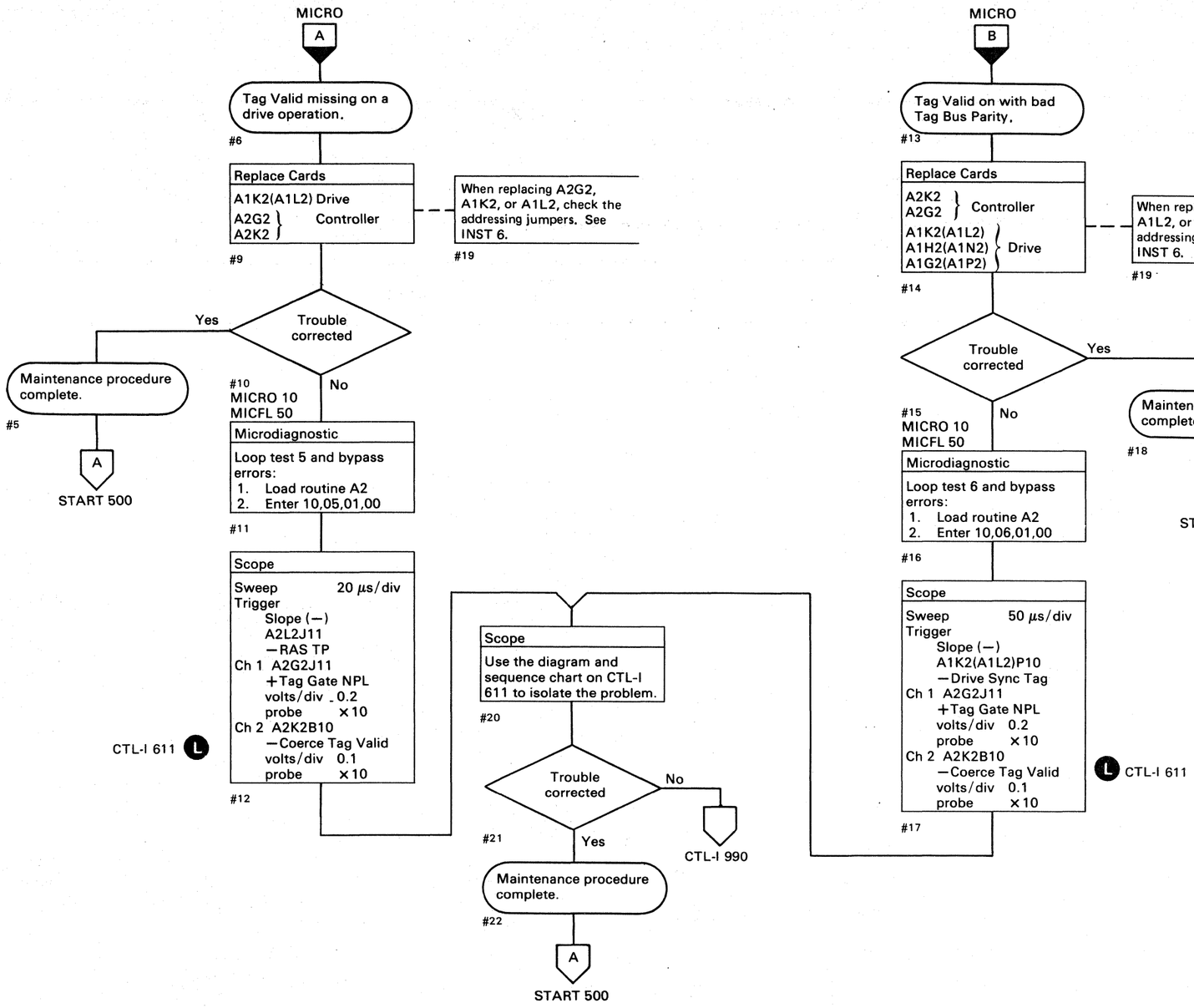
Tag Valid With Tag Bus Parity - Error Code A260

The microdiagnostic verifies that Coerce Tag Valid (L) is not received for certain drive tags when Tag Bus Parity is bad. Tag '09', Bus '21' inverts the tag bus parity bit to cause a Tag Bus Parity Error (A) in the drive. The Tag Bus Parity error prevents File Tag Valid NPL (D) and Coerce Tag Valid.

The following conditions occur for all drive Tags 8A through 8F during this microdiagnostic test:

Coerce Tag Valid is inactive (L).
Dlyd Tag Response is inactive (K).
Allow Drive Tag Valid is active (J).
Tag Response is inactive (F).
Tag Bus Parity Error is active (A).
NPL Tag Gate is active.

See OPER 95 for a description of the sequence of tag operations and Tag Valid.



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TAG VALID FAILURE

Circuit Description

Tag Valid is activated by Coerce Tag Valid (L).

Coerce Tag Valid is activated by the following conditions:

- –Allow Drive Tag Valid (J)
- +Addressing 82 (H)
- –Valid Tag Gate (G)
- –Dlyd Tag Response (K)

Allow Drive Tag Valid is activated by Tag Bit 0 and Not Tag 84.

Valid Tag Gate is activated by:

Not Bus Out Parity Chk
Not Tag Bus Parity Chk
Tag Gate

Dlyd Tag Response is activated by Tag Response (F), which is activated by File Tag Valid NPL (D).

File Tag Valid in the drive is generated by Enable Functions (C).

See OPER 90 for additional theory.

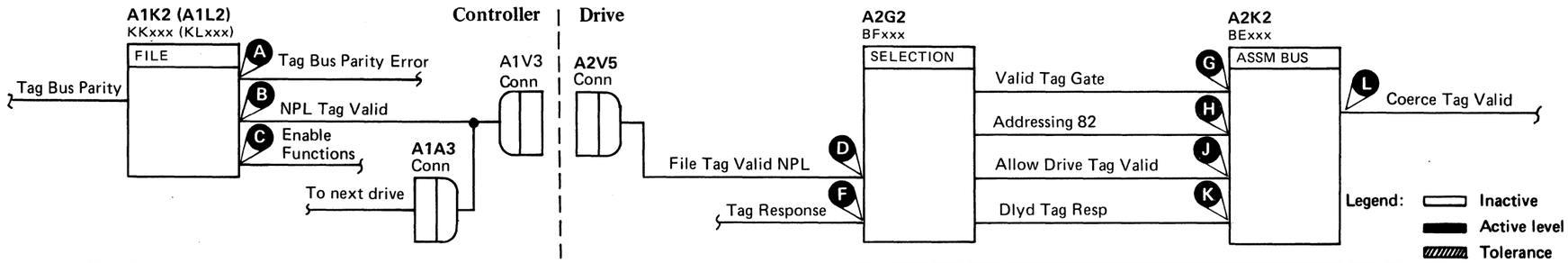


Chart Line No.	Line Name	ALD	Test Point		
Routine A2, Test 6					
1	+NPL Tag Gate	BF130	A2G2 J11		
2	–Coerce Tag Valid	BE150	A2K2 B10	L	
3	–Valid Tag Gate	BE150	A2K2 B09	G	
4	–Dlyd Tag Response	BE150	A2K2 D10	K	
5	–Allow Drive Tag Valid	BE150	A2K2 B13	J	
6	+Addressing 82	BE150	A2K2 D13	H	
7	+Tag Response	BE150	A2K2 B02	F	
8	+File Tag Valid NPL	BF160	A2G2 S07	D	
9	+Enable Functions	KK140 (KL140)	A1K2 G10	C	
10	–Tag Gate Valid Dlyd	KK150 (KL150)	A1K2 J03		
11	+NPL Tag Gate	KK100 (KL100)	A1K2 P09		
12	–Tag Bus Parity Error	KK190 (KL190)	A1K2 P05	A	

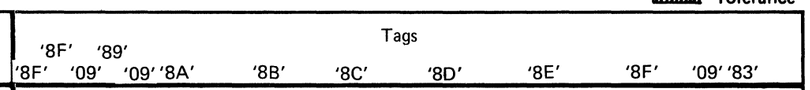
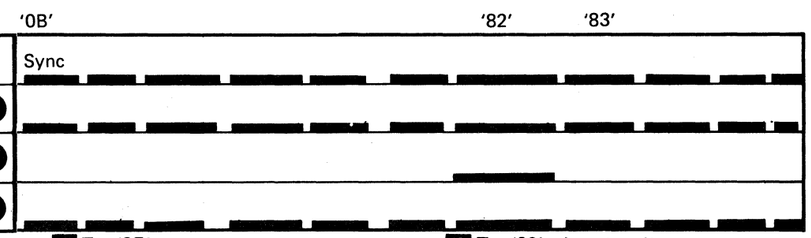


Chart Line No.	Line Name	ALD	Test Point		
Routine A2, Test 5					
1	+NPL Tag Gate	BF130	A2G2 J11		
2	–Coerce Tag Valid	BE150	A2K2 B10	L	
3	+Addressing 82	BE150	A2K2 D13	H	
4	–Valid Tag Gate	BE150	A2K2 B09	G	



1 Tag '8F' = sync.
2 Tag '8F' = reset.
3 Tag '89' = sense device interface.
4 Tag '09' = invert parity.
5 Tag '09' = reset diagnostic.
6 Tag '83' = sense device interface.

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ALLOW HAR/SET READ/WRITE FAILURE

Allow HAR is generated during index range when in Read mode to allow the Head Address Register to be advanced during Multitrack and Record Overflow operations. Allow HAR interrupts the Set Read/Write values (Dev Tag '07', Bus Out = xxxx x111) and allows the Set HAR bus and tag values to be sent to the drive.

Allow HAR functions:

Prevent the RW latch from holding Tag Gate active.

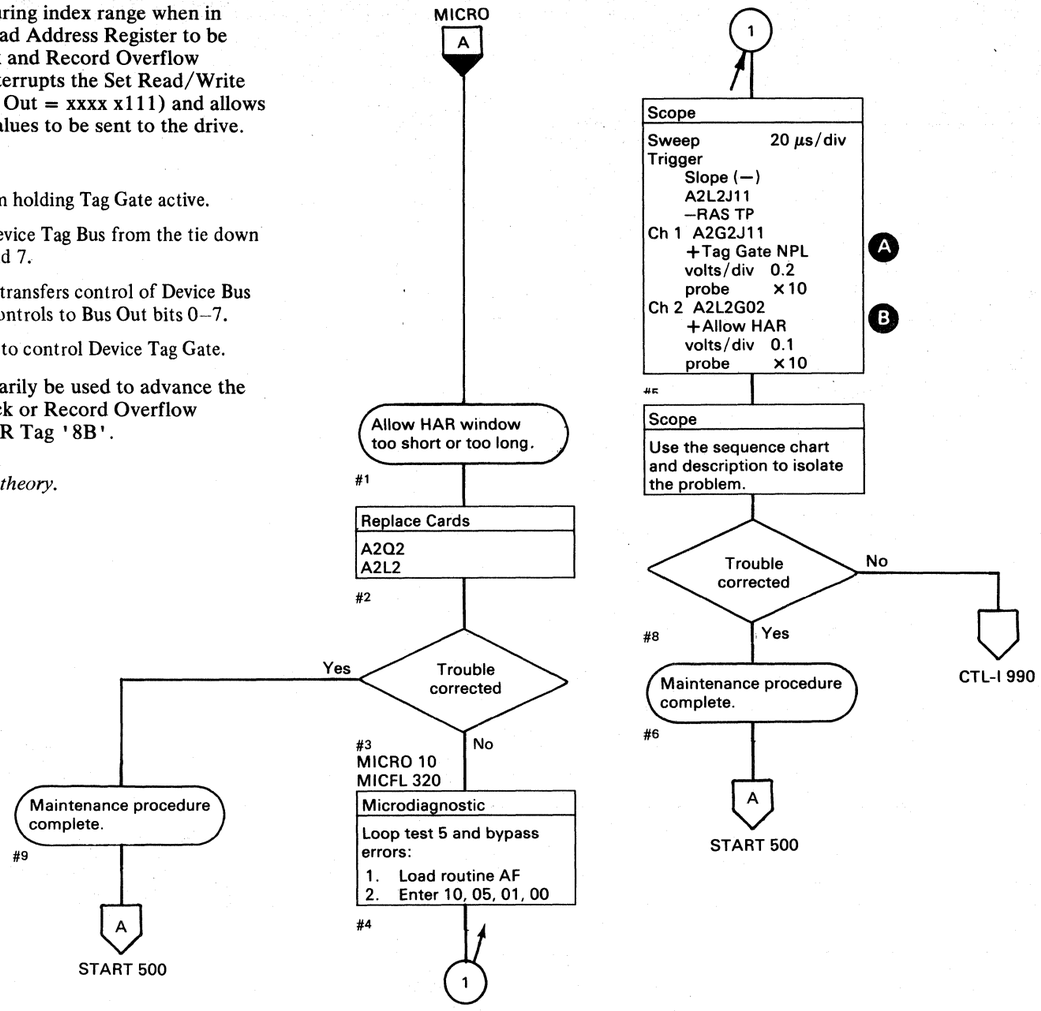
Transfer control of the Device Tag Bus from the tie down to the Tag bus bit 5, 6, and 7.

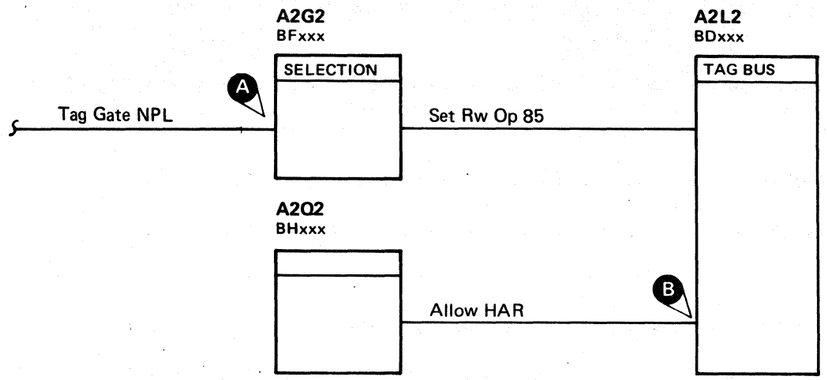
Drop Rd Wrt Gate which transfers control of Device Bus Out from the read write controls to Bus Out bits 0–7.

Permit Selected Tag Gate to control Device Tag Gate.

These controls would ordinarily be used to advance the head address on a Multitrack or Record Overflow operation by use of Set HAR Tag '8B'.

See OPER 210 for additional theory.





Legend: Inactive / Active level / Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags '0B'	'8B'	'8B'	'05'	'8F'
1	+Tag Gate NPL	BF130	A2G2 J11	A	Sync	1	2	3	4
2	+Allow HAR	BD150	A2L2 G02	B					

1 Tag '8B' = Set HAR to '01'.
2 Tag '8B' = Set HAR to '02'.
3 Tag '05' = Reset read/write.
4 Tag '8F' = Sense HAR.

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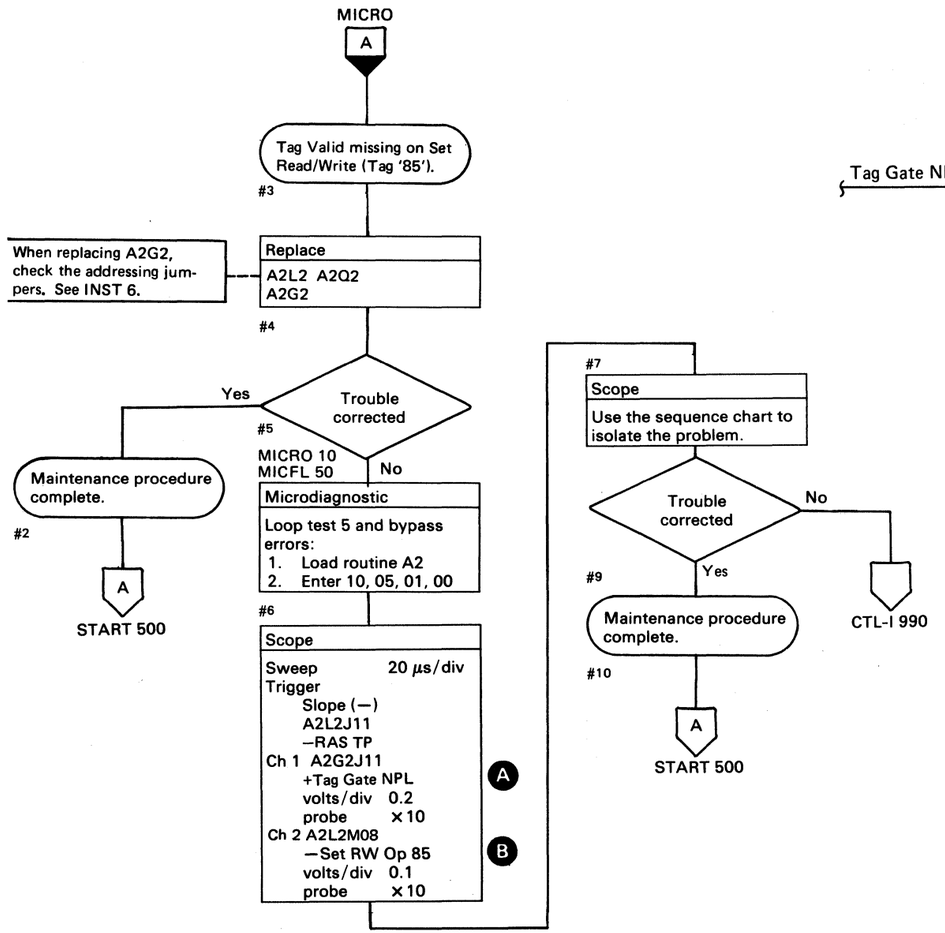
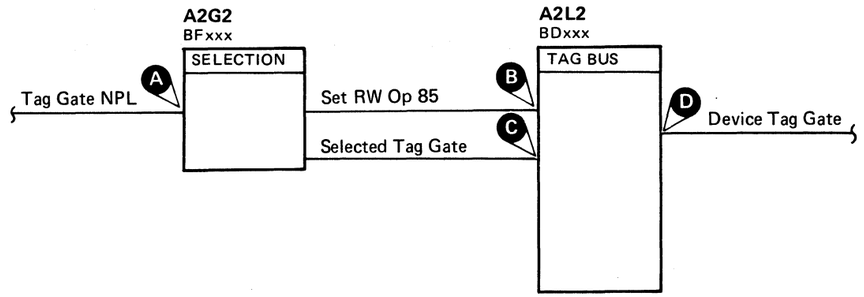
TAG VALID MISSING

Set RW Op 85 (B) and Selected Tag Gate (C) allow the set of Device Tag Gate (D). Tag Gate and no errors activates Tag Gate Valid. Tag Gate Valid activates Enable Functions and allows File Tag Valid to be returned to the controller.

The microdiagnostic issues Tag '85' and then tests for Interface Checks during Tag '84'. The microdiagnostic again issues Tag '85' and checks for Tag Valid active.

See OPER 90 for additional theory.





Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point		Tags
1	+Tag Gate NPL	BF130	A2G2 J11	A	Sync 1 2 3 4
2	+File Tag Valid NPL	BU300	A2V5 D13		
3	—Set RW Op 85	BD150	A2L2 M08	B	

Tags: '0B' '85' '84' '85' '05'

1 Tag '85' = Set RW.
2 Tag '84' = Test for Interface Check.
3 Tag '85' = Set RW.
4 Tag '05' = Reset RW.

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UNSUPPRESSIBLE ATTENTION REGISTER

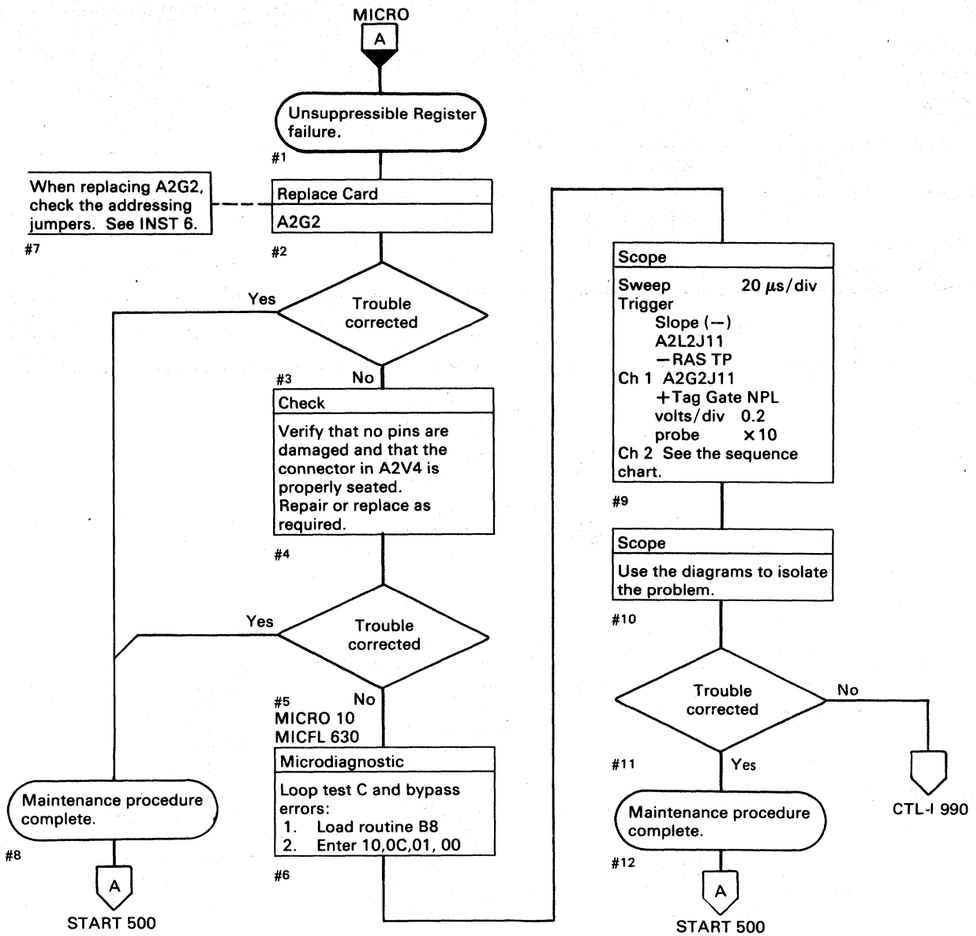
The Unsuppressible Attention bits are used by the storage control to selectively poll for Device Attentions.

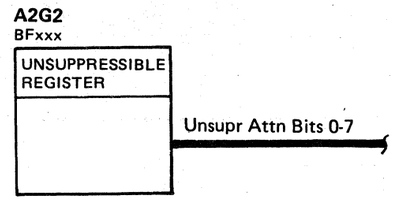
The Unsuppressible Attention bits are set and reset individually by Tag '01'.

These bits are only effective when a Tag '82' (Poll Device) is issued with Bus Out bit 3 on. Then, Attention bits that have their respective Unsuppressible Attention bits active, are transmitted to the controller.

For example:
If device 5 has an Attention bit active and an Unsuppressible Attention bit 5 not active, there is no response to a Poll Unsuppressible operation. However, if Unsuppressible Attention bit 5 is active, an Attention Bit 5 is returned to the controller in response to the Poll Unsuppressible Operation.

See OPER 104 for additional theory.





Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point	Tags '0B'
1	+Tag Gate NPL	BF130	A2G2 J11	Sync
2	—Sel Bus Bits	BF190		

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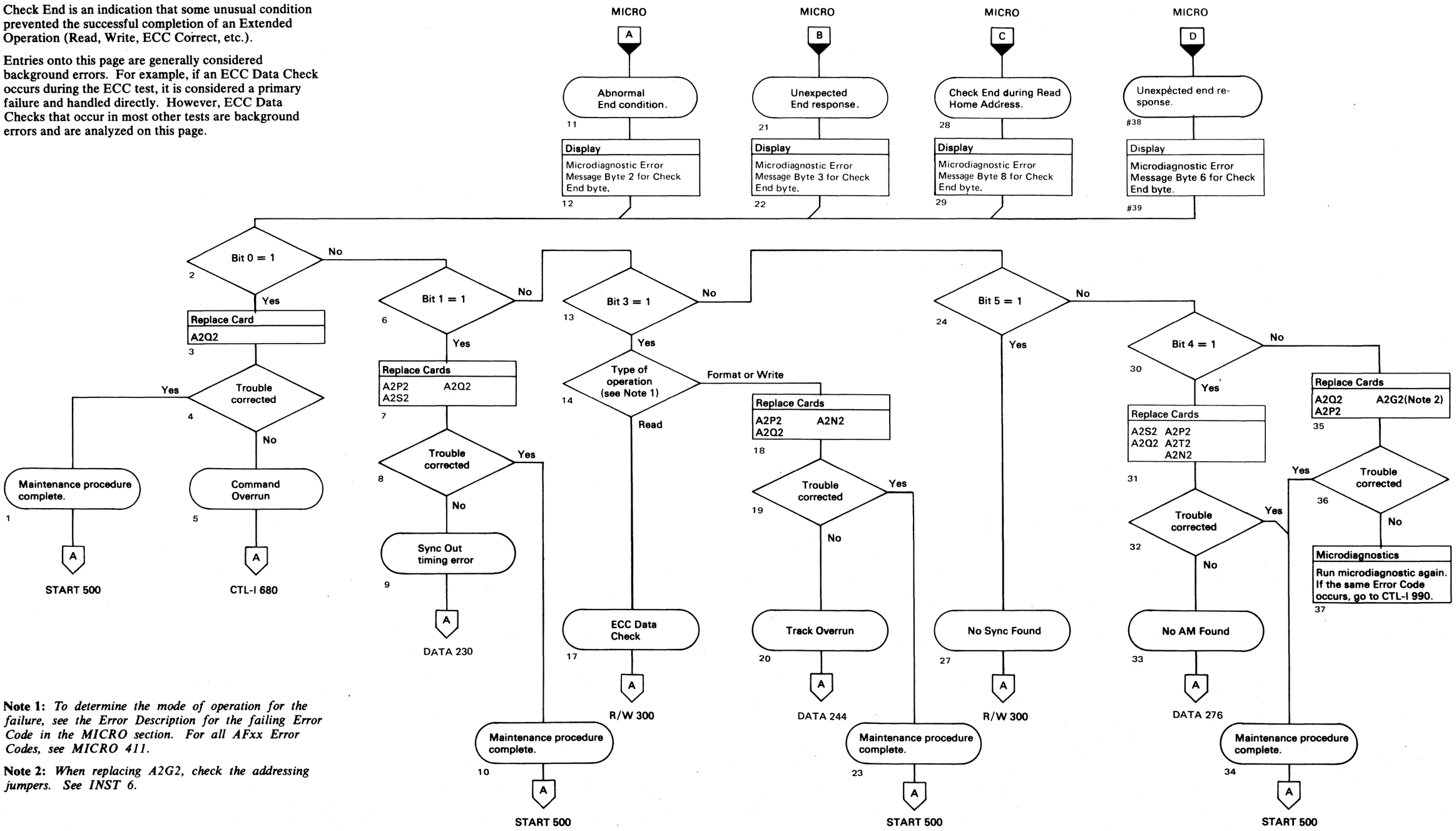
CHECK END DECISIONS

Check End is an indication that some unusual condition prevented the successful completion of an Extended Operation (Read, Write, ECC Correct, etc.).

Entries onto this page are generally considered background errors. For example, if an ECC Data Check occurs during the ECC test, it is considered a primary failure and handled directly. However, ECC Data Checks that occur in most other tests are background errors and are analyzed on this page.



Note 1: *To determine the mode of operation for the failure, see the Error Description for the failing Error Code in the MICRO section. For all AFxx Error Codes, see MICRO 411.*

Note 2: *When replacing A2G2, check the addressing jumpers. See INST 6.*

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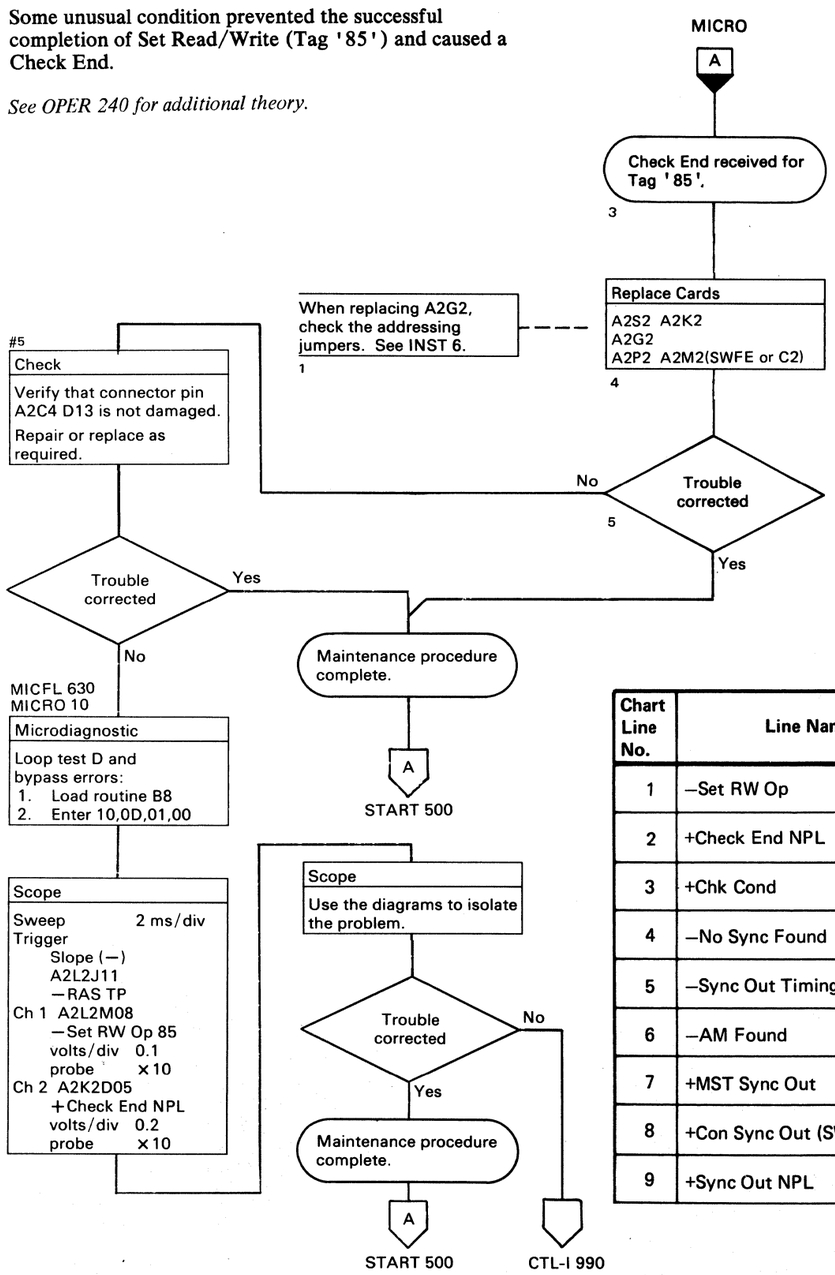
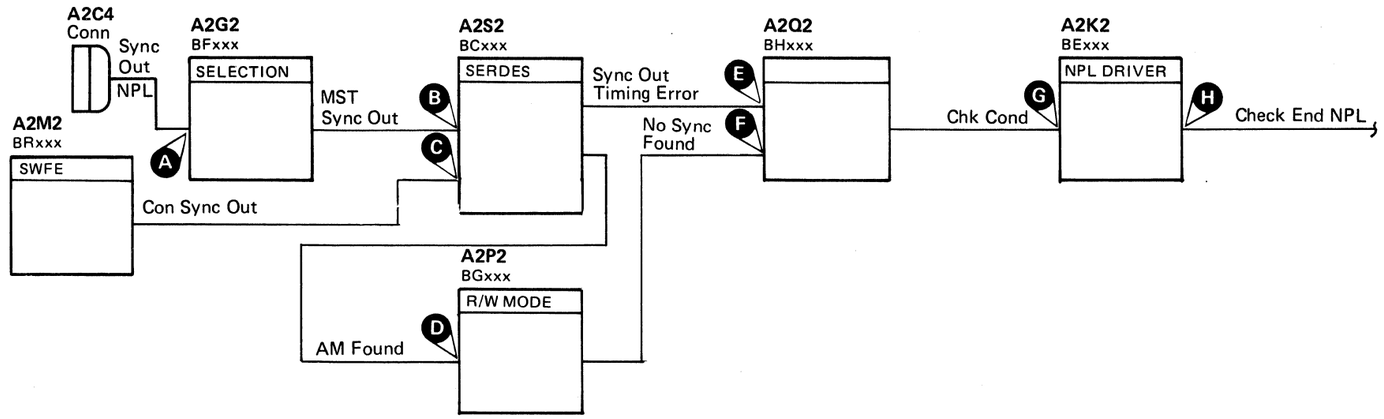
CHECK END ON SET READ/WRITE

Some unusual condition prevented the successful completion of Set Read/Write (Tag '85') and caused a Check End.

See OPER 240 for additional theory.





Legend: Inactive, Active level, Tolerance

Chart Line No.	Line Name	ALD	Test Point		
1	−Set RW Op	BD150	A2L2 M08		
2	+Check End NPL	BE160	A2K2 D05	H	Inactive
3	+Chk Cond	BE140	A2K2 D02	G	Inactive
4	−No Sync Found	BH150	A2Q2 M02	F	Inactive
5	−Sync Out Timing Error	BH150	A2Q2 P04	E	Inactive
6	−AM Found	BG140	A2P2 P09	D	Inactive
7	+MST Sync Out	BC170	A2S2 S12	B	Inactive
8	+Con Sync Out (SWFE)	BC170	A2S2 S12	C	Inactive
9	+Sync Out NPL	BF100	A2G2 B13	A	Inactive

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NORMAL END MISSING ON SET R/W

Each operation, whether an immediate or extended operation, must be terminated with a Normal End or a Check End.

For immediate operations, Normal End occurs simultaneously with Tag Valid.

For extended operations (Read, Write, ECC Control and Set Read/Write), Normal End and Tag Valid are returned at different times.

If Normal End or Check End is not received at the proper time, an error is posted.

For additional information on tag sequencing, see OPER 95.

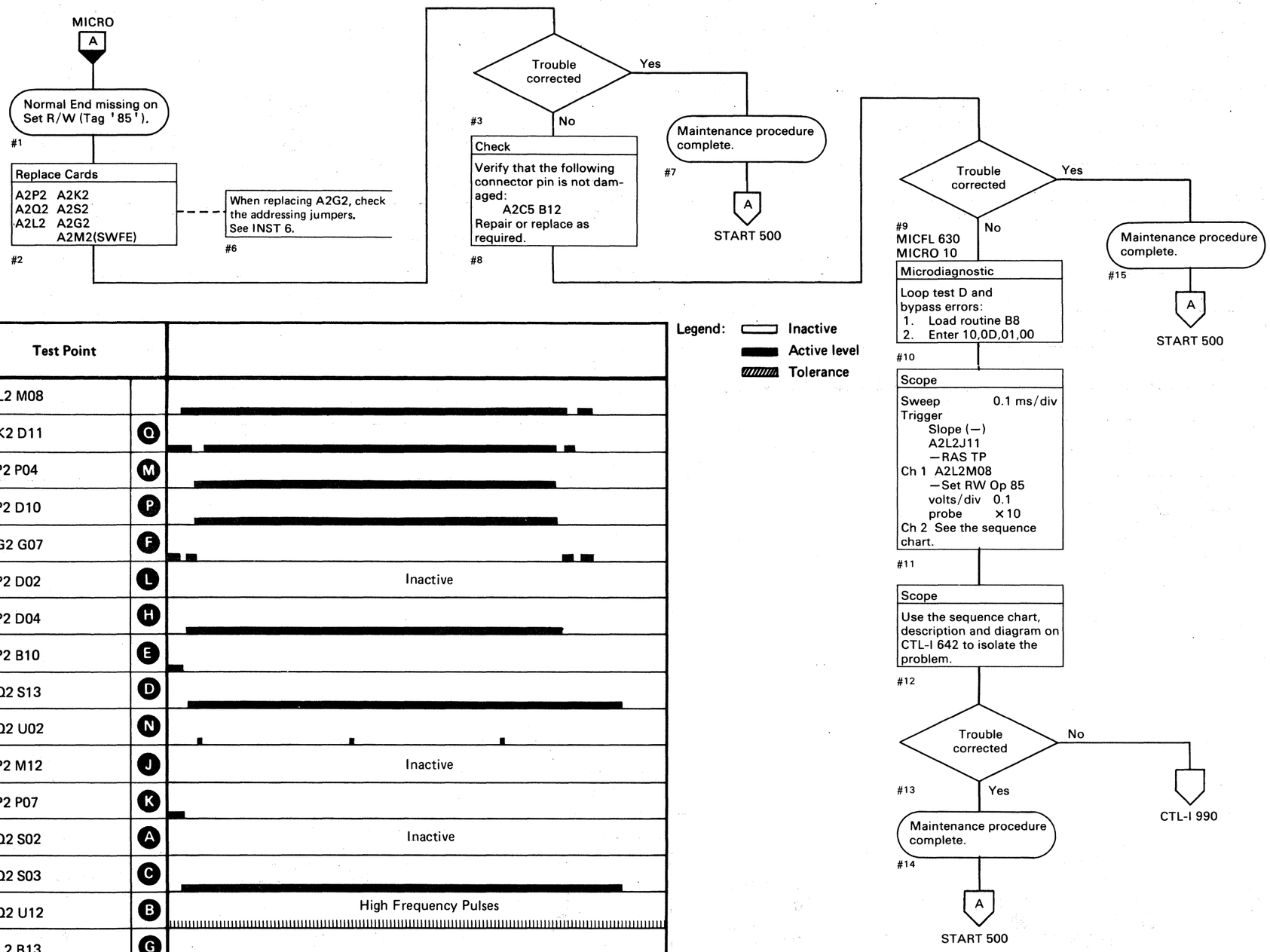

Chart Line No.	Line Name	ALD	Test Point		
1	—Set RW Op 85	BD150	A2L2 M08		
2	+Normal End NPL	BE160	A2K2 D11	Q	
3	—Op End	BG170	A2P2 P04	M	
4	—End Data Op	BG170	A2P2 D10	P	
5	—Selected Tag Gate	BF110	A2G2 G07	F	
6	—Read*Not Clk Gated	BG170	A2P2 D02	L	Inactive
7	+PLO End Op	BG170	A2P2 D04	H	
8	+Reset End Cond	BG170	A2P2 B10	E	
9	—VFO Good	BH160	A2Q2 S13	D	
10	—CT 15	BH150	A2Q2 U02	N	
11	+Add 128	BG140	A2P2 M12	J	Inactive
12	+Reset Gap Ctr	BG140	A2P2 P07	K	
13	—AM Area	BH160	A2Q2 S02	A	Inactive
14	—Rd Wrt Latch	BH130	A2Q2 S03	C	
15	—Bit Ring 1 Pwr	BH130	A2Q2 U12	B	High Frequency Pulses
16	+Reset RW Op 05	BD150	A2L2 B13	G	

Legend: Inactive; Active level; Tolerance

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NORMAL END MISSING ON SET R/W

Normal End is set by:

Op End active (M) and not Chk Cond.

Op End is set by:

End Data Op (P) active while Selected Tag Gate (F) and Read * Not Clk Gated (L) are inactive.

End Data Op is set by:

PLO End Op (H) active and not Reset End Cond (E).

PLO End Op is set by VFO Good (D) and not Reset End Cond (E).

VFO Good is set by:

Rd Wrt Bit 1 and CT 15 (N).

CT 15 is set by:

Add 128 (J) and Reset Gap Ctr (K) both inactive.

AM Area (A) active causes Reset Gap Ctr to be active.

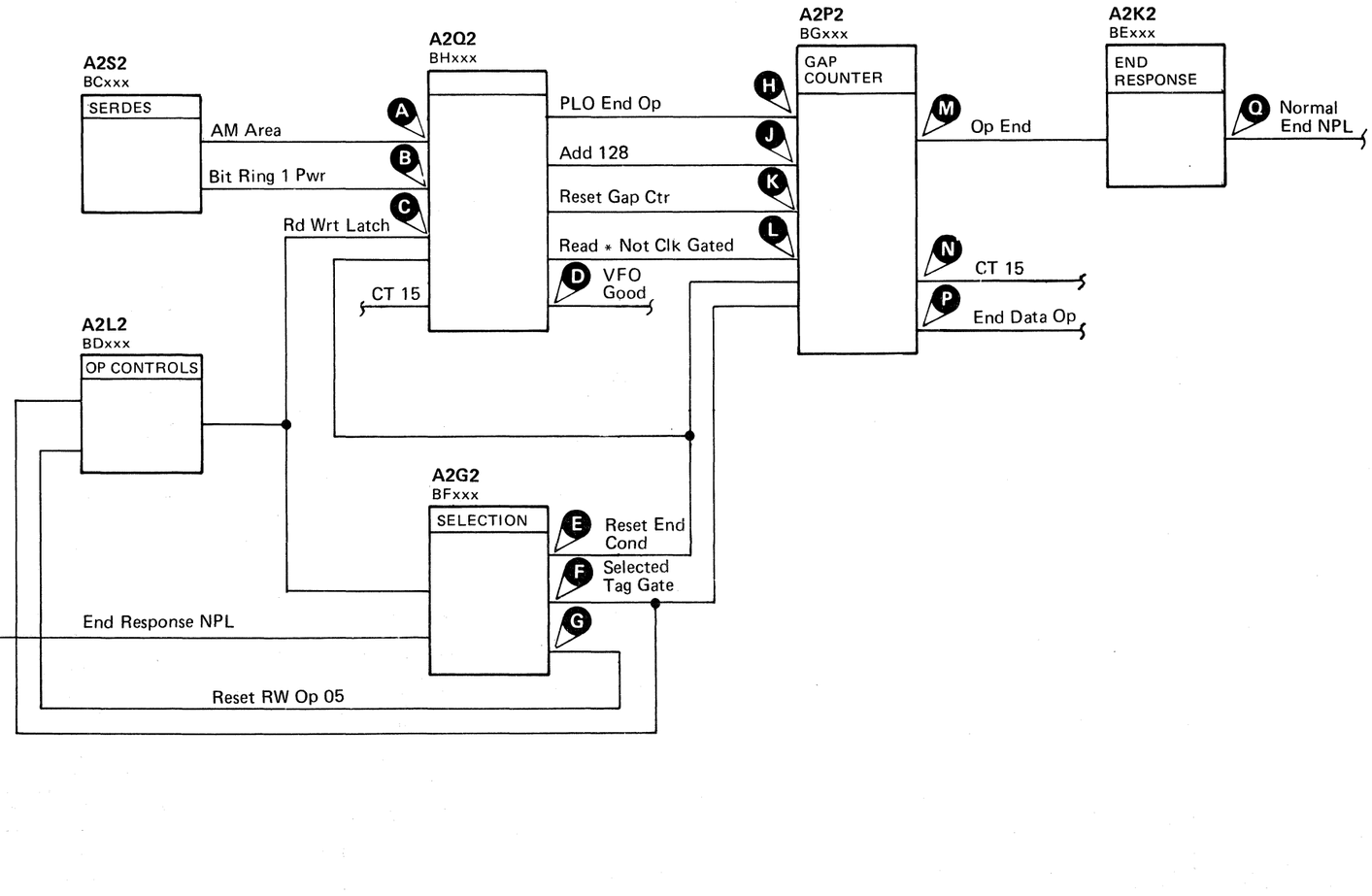
Rd Wrt Bit 1 is set by:

Rd Wrt Latch (C) and Bit Ring 1 Pwr (B).

Rd Wrt Latch is set by:

Reset RW Op 05 (G) is inactive.

See OPER 95 for additional theory.



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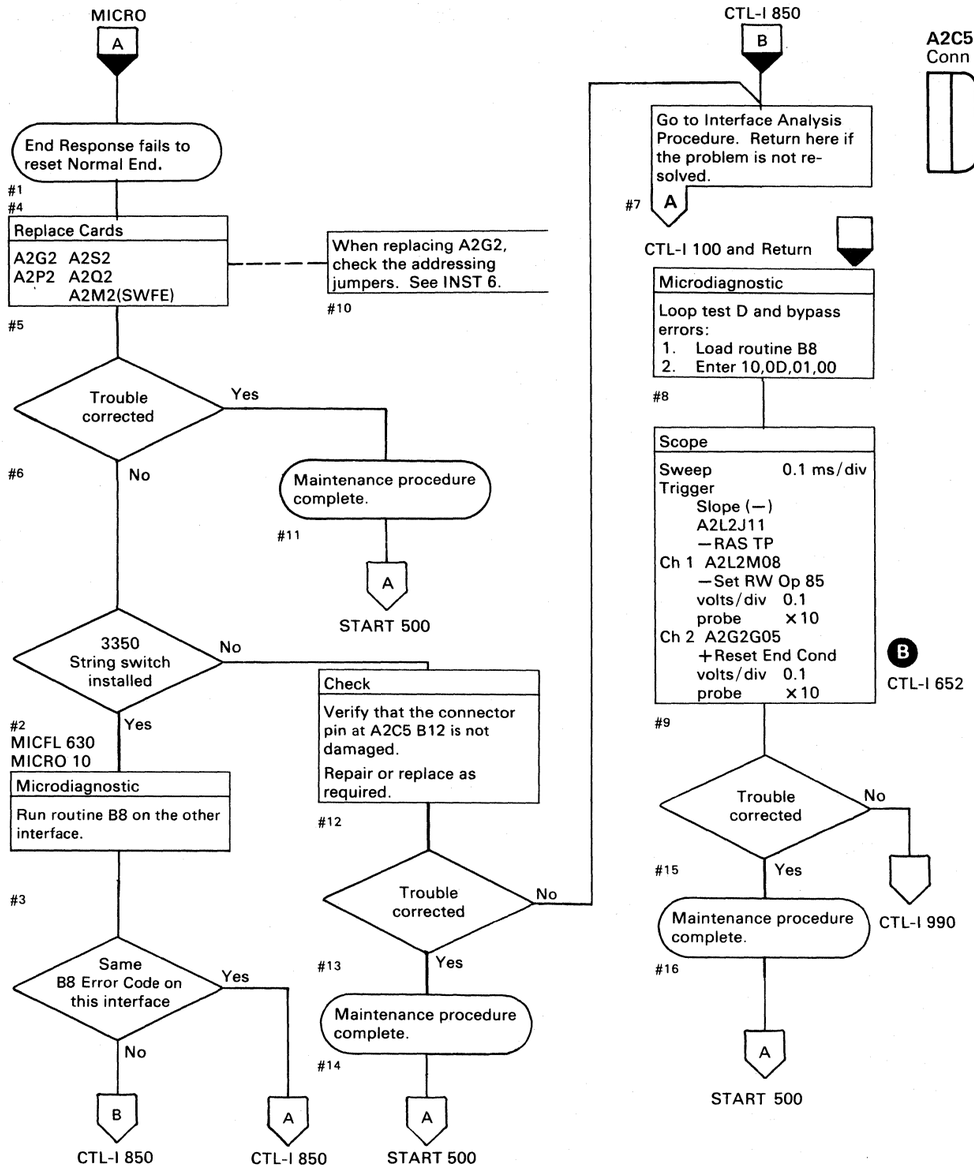
END RESPONSE FAILURE

The End Response signal is sent from storage control to the controller after Normal End or Check End is received.

Failure to receive End Response is recognized when one or more of the end latches fail to reset.

See OPER 95 for the sequence of the end conditions.



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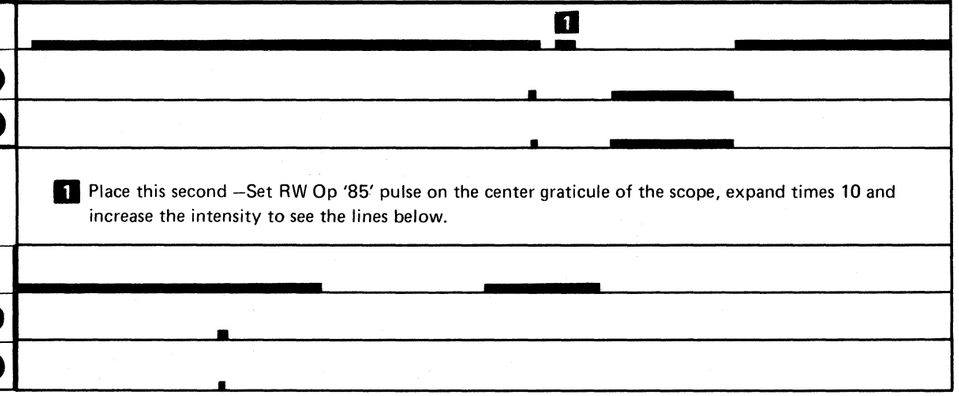
END RESPONSE FAILURE

See the diagram on CTL-I 650 for referenced test points.

Legend: Inactive
Active level
Tolerance

Chart Line No.	Line Name	ALD	Test Point		
1	–Set RW Op 85	BD100	A2L2 M08		
2	+Reset End Cond	BF160	A2G2 G05	B	
3	+End Response NPL	BF160	A2G2 S03	A	
4	–Set RW Op 85	BD100	A2L2 M08		
5	+Reset End Cond	BF160	A2G2 G05	B	
6	+End Response NPL	BF160	A2G2 S03	A	



1 Place this second –Set RW Op '85' pulse on the center graticule of the scope, expand times 10 and increase the intensity to see the lines below.

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NORMAL OR CHECK END MISSING

Each operation, whether an Immediate or Extended operation, must be terminated with a Normal End or a Check End.

Immediate Operations

For Immediate operations, Normal End occurs simultaneously with Tag Valid.

Extended Operations

For Extended operations (Read, Write, ECC Control and Set Read/Write), Normal End and Tag Valid are returned at different times.

If Normal End or Check End is not received at the proper time, an error is posted.

End Data (G) and Not Rst Run ECC TP (F) causes an Op End (E). Op End activates Normal End NPL (K) or Check End NPL (J).

The Recycle Tag (A) in conjunction with the counter in Modulo-16 Mode, determines when End Data (G) becomes active.

See DATA 100 for a description of a Recycle Line Failure.

Run Modulo is active for Extended operations. If Modulo does not run, Op End (E) never becomes active.

Modulo is activated by Cntl 1 on a Write operation.

Cntl 1 is activated by Sync In (L). Sync In is activated by Gated Write Mode. Gated Write Mode is activated by Not End Data (G) and Write Mode (H). Write Mode is activated by Not Extend G1 (C) and Fmt G1 (D).

For additional information on tag sequencing, see OPER 95.

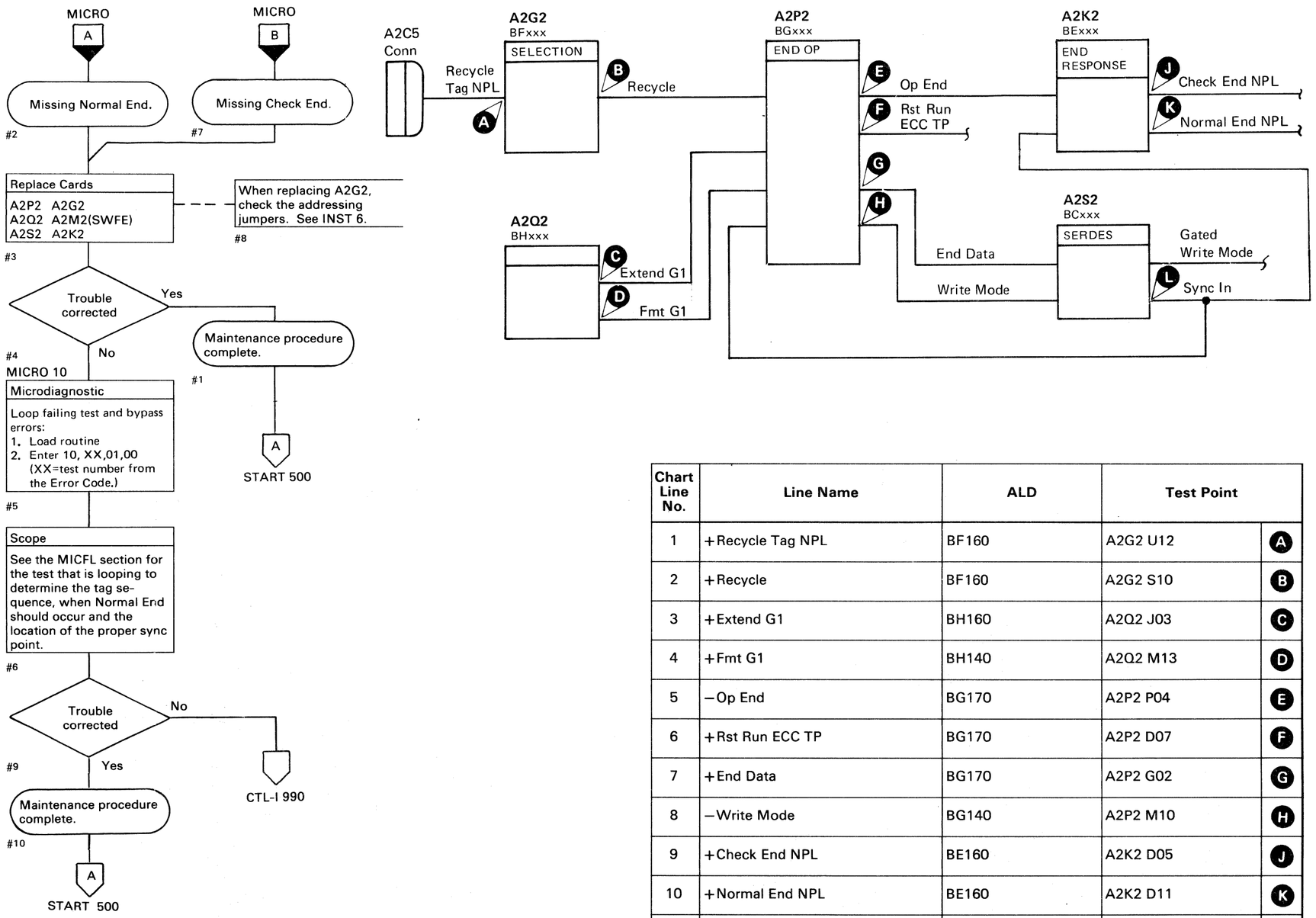

Chart Line No.	Line Name	ALD	Test Point	
1	+Recycle Tag NPL	BF160	A2G2 U12	A
2	+Recycle	BF160	A2G2 S10	B
3	+Extend G1	BH160	A2Q2 J03	C
4	+Fmt G1	BH140	A2Q2 M13	D
5	−Op End	BG170	A2P2 P04	E
6	+Rst Run ECC TP	BG170	A2P2 D07	F
7	+End Data	BG170	A2P2 G02	G
8	−Write Mode	BG140	A2P2 M10	H
9	+Check End NPL	BE160	A2K2 D05	J
10	+Normal End NPL	BE160	A2K2 D11	K
11	−Sync In	BC170	A2S2 S10	L

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COMMAND OVERRUN

Command Overrun (C) is generated when one of the following occurs:

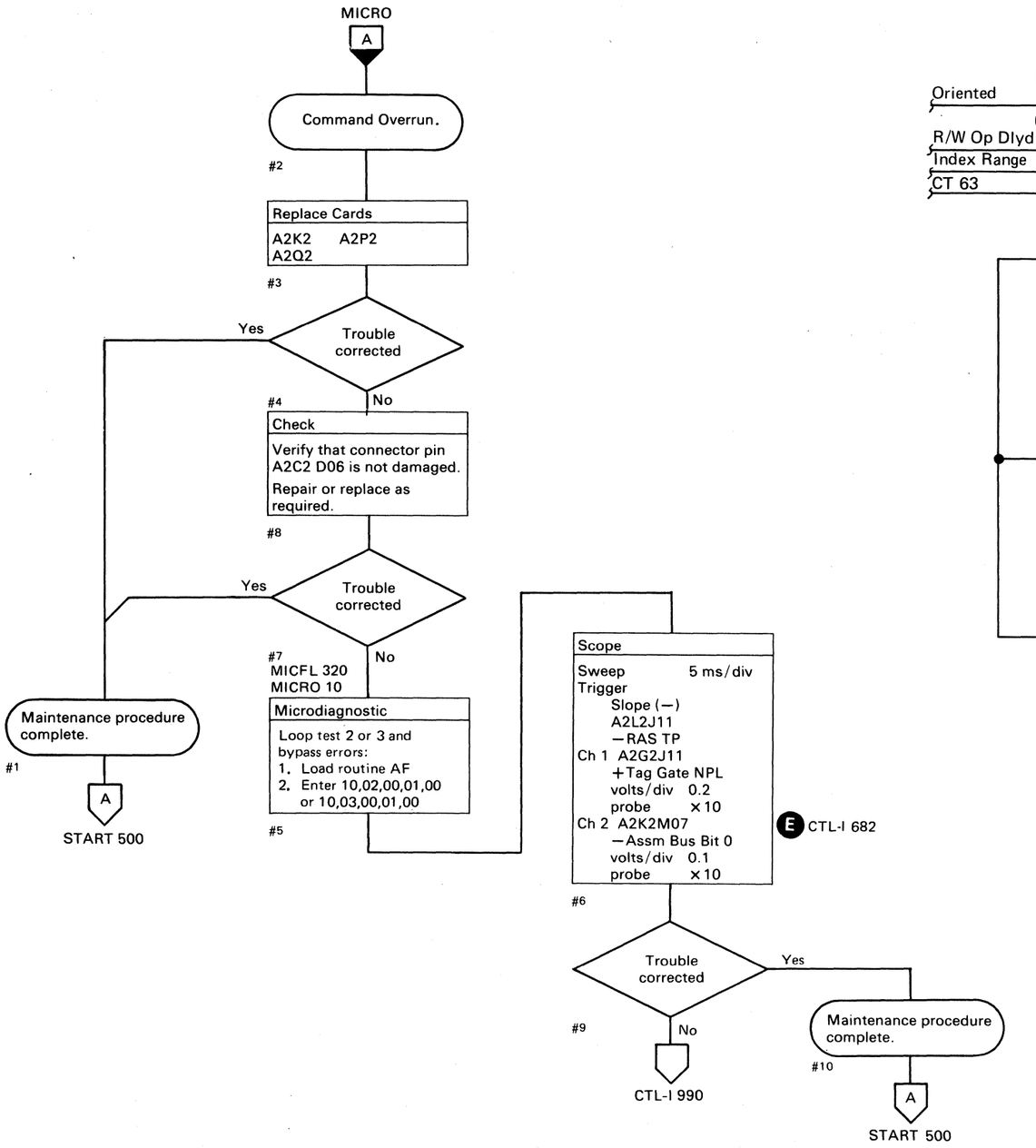
- Oriented (A) becomes active. This indicates that orientation has occurred during a non-oriented Read or Write command. Orientation normally occurs only during a Read Format G1 command or during a Search Address Mark command.
- R/W Op Dlyd (B) becomes active within 63 bytes after Index Range activates.

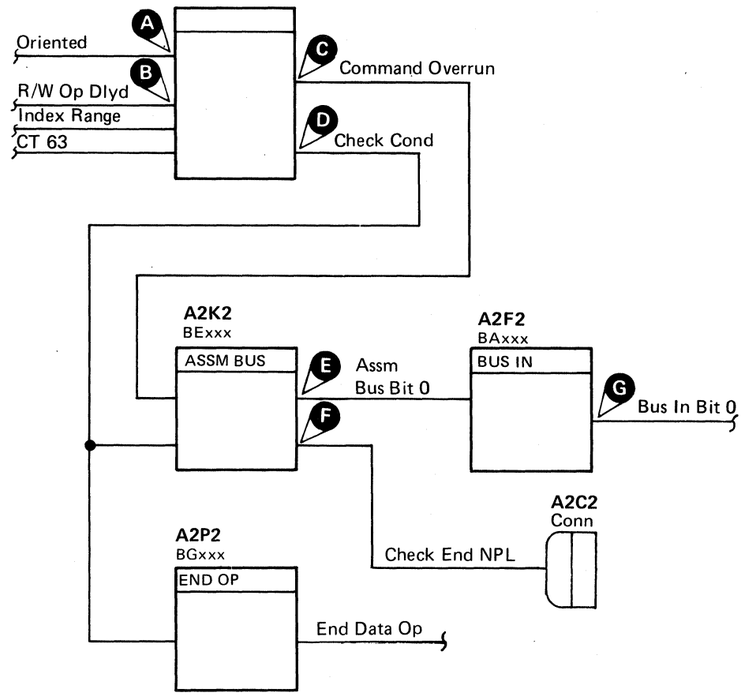
Command Overrun sets Assm Bus Bit 0 (E) and Chk Cond (D).

Assm Bus Bit 0 sets Bus In Bit 0 (G).

Chk Cond sets Check End NPL (F).

See OPER 240 for additional theory.





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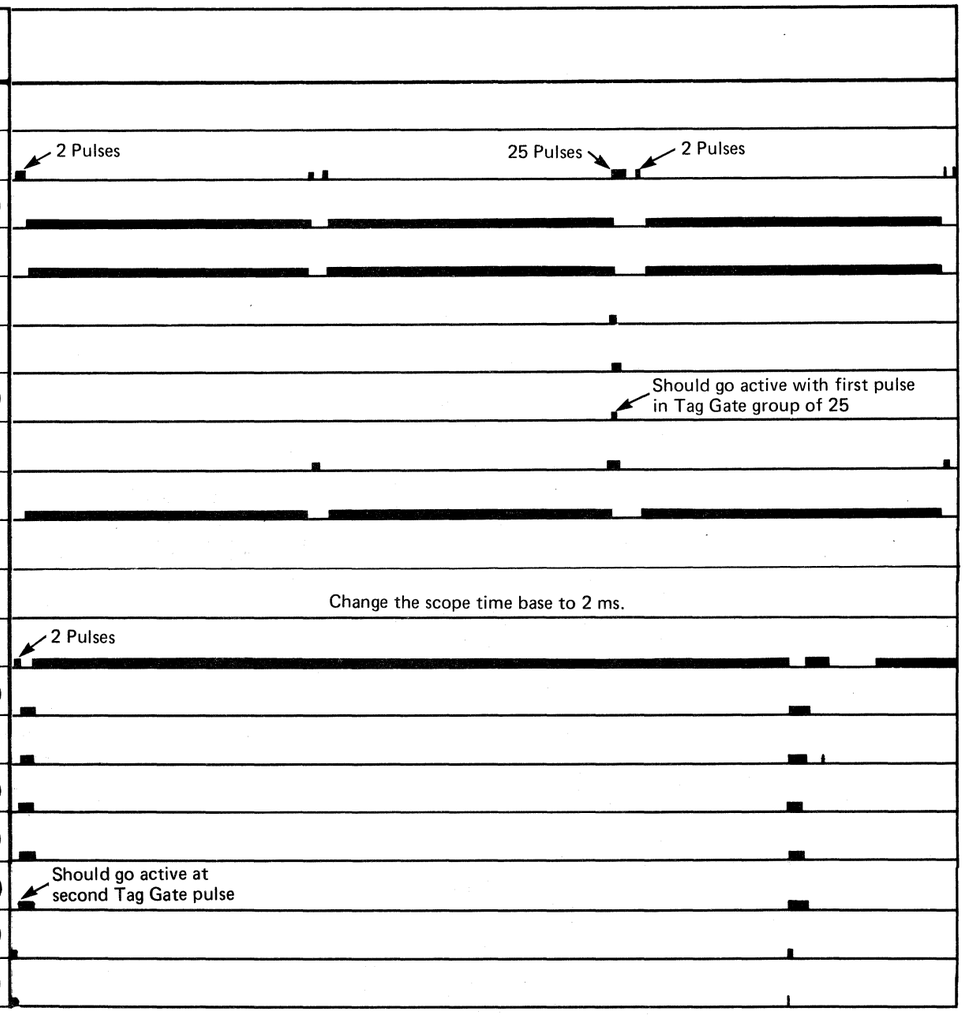
COMMAND OVERRUN

See the diagram on CTL-I 680 for referenced test points.

Legend: Inactive
Active level
Tolerance

Chart Line No.	Line Name	ALD	Test Point	
	Routine AF, Test 2			
1	+Tag Gate NPL	BF130	A2G2 J11	
2	–Assm Bus Bit 0	BE110	A2K2 M07	E
3	–Bus In Bit 0	BA100	A2F2 P05	G
4	+Chk End NPL	BE160	A2K2 D05	F
5	+Chk Cond	BE140	A2K2 D02	D
6	–Command Overrun	BH130	A2Q2 M05	C
7	–Oriented	BH130	A2Q2 J06	A
8	+RW Op Dlyd	BH100	A2Q2 B10	B
	Routine AF, Test 3			
9	+Tag Gate NPL	BF130	A2G2 J11	
10	–Assm Bus Bit 0	BE110	A2K2 M07	E
11	–Bus In Bit 0	BA100	A2F2 P05	G
12	+Chk End NPL	BE160	A2K2 D05	F
13	+Chk Cond	BE140	A2K2 D02	D
14	–Command Overrun	BH130	A2Q2 M05	C
15	–Oriented	BH130	A2Q2 J06	A
16	+RW Op Dlyd	BH100	A2Q2 B10	B



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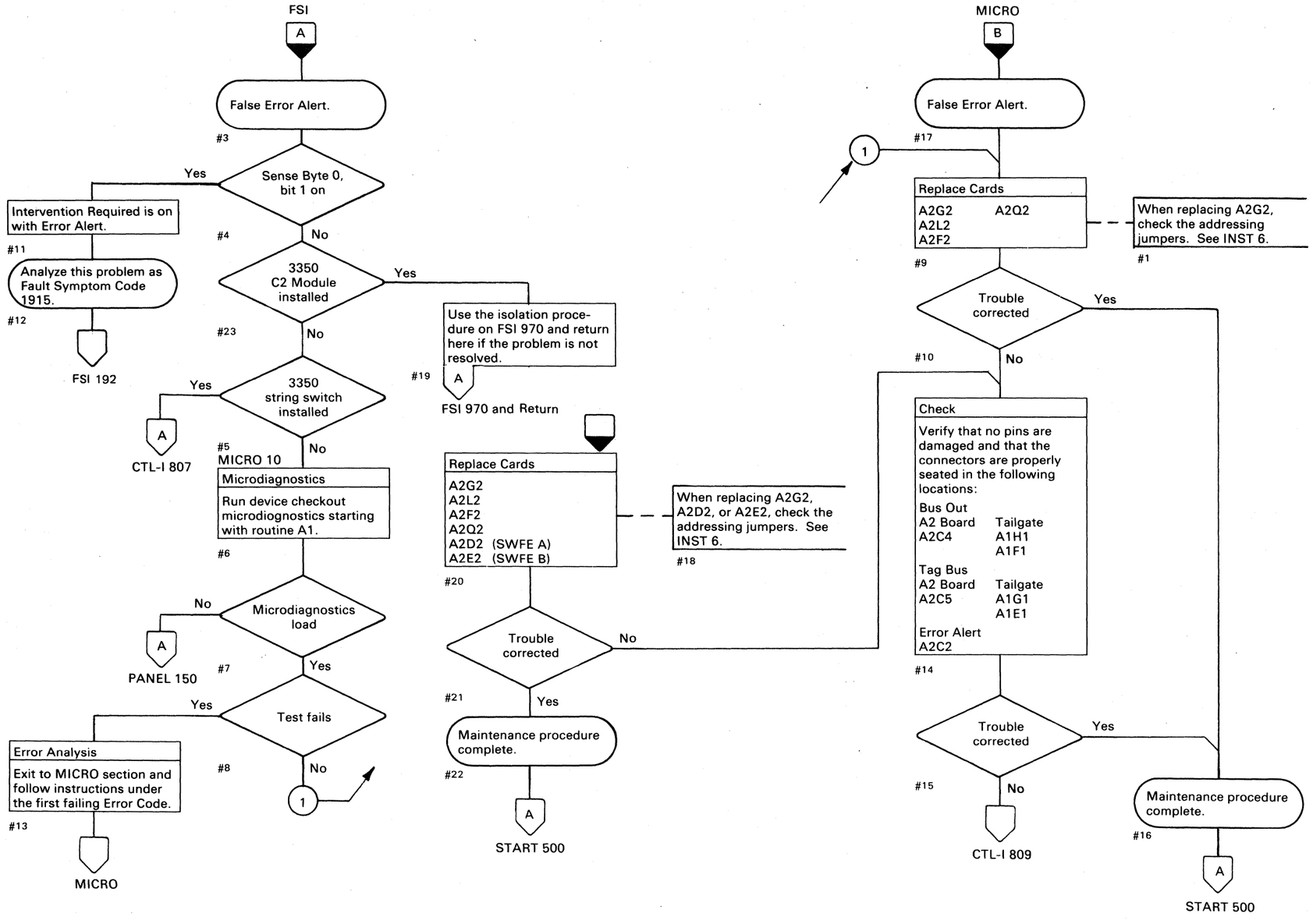
CONTROLLER CHECK – False Error Alert

A false Error Alert is an indication of an Error Alert condition that is not further defined by Controller Error 1 or 2 sense information, or by bit 3 of machine status (Read/Write Check) from the device.

An undefined Error Alert is also used to indicate that Diagnostic Suppress Write Gate is active when not in Diagnostic Mode.



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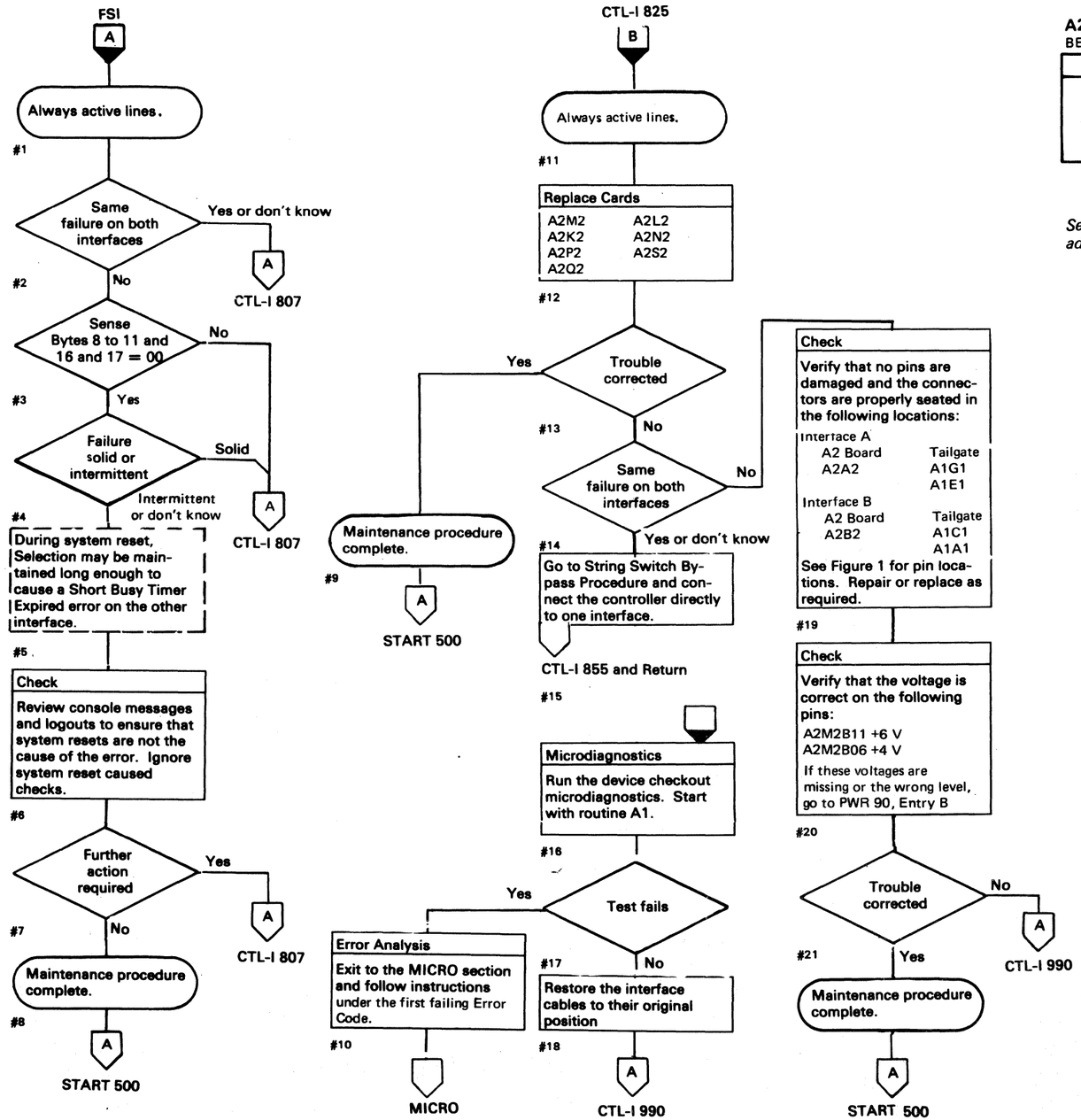
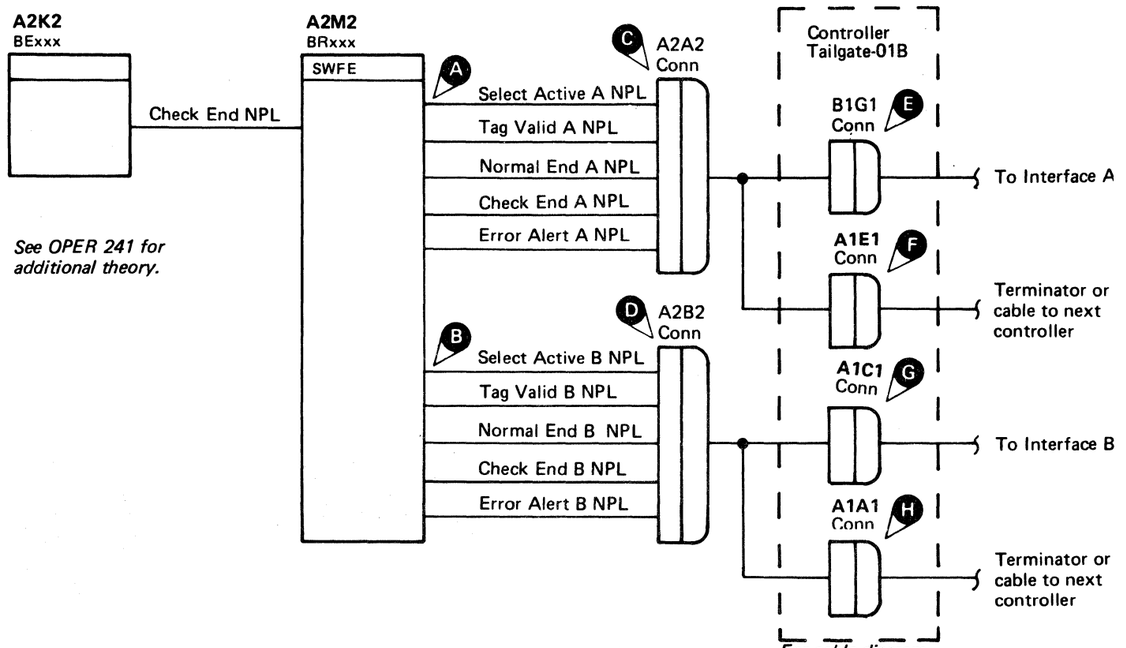
ALWAYS ACTIVE LINES (With String Switch)





See OPER 241 for additional theory.

Figure 1. Pin Locations

Line Name	Conn A2A2 Pins (C)	Conn A1G1 Pins (E)	Conn A1E1 Pins (F)
+Select Active A NPL	B02	G03	G03
+Tag Valid A NPL	D05	J04	J04
+Normal End A NPL	B05	G05	G05
+Check End A NPL	D06	J06	J06
+Error Alert A NPL	B08/B09	G08	G08
	Conn A2B2 Pins (D)	**Conn A1C1 Pins (G)**	**Conn A1A1 Pins (H)**
+Select Active B NPL	B02	G03	G03
+Tag Valid B NPL	D05	J04	J04
+Normal End B NPL	B05	G05	G05
+Check End B NPL	D06	J06	J06
+Error Alert B NPL	B08/B09	G08	G08

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STRING SWITCH CHECKOUT PROCEDURE

FSI
CTL-I 805
CTL-I 806
DEV-I 410

String switch checkout.

#1

Prepare the 3350 subsystem to run microdiagnostics:

1. Place the microdiagnostic disk in the failing storage control.
2. At the 3350 CE Panel, select a drive and have the operator vary it offline. Turn the CE Mode switch to the On position.
3. Move the Interface Select switch to the interface from which the microdiagnostics are going to run.
4. At the 3350 Power Panel, enable both Interfaces A and B.

#1

MICRO 10

Microdiagnostics
Run device checkout microdiagnostics. Start with routine A1.

#3

Microdiagnostics load — Yes

#4 No

A

PANEL 150

#5 Tests fail — Yes

No

Error Analysis
Exit to the MICRO section and follow instructions under the first failing Error Code.

#10

MICRO

Both interfaces fail — No

#6 Yes or don't know

1. Move the microdiagnostic disk to the other storage control.
2. Move the Interface Select switch to the interface from which the microdiagnostics are now going to run.

#7

Microdiagnostics
Run device checkout microdiagnostics. Start with routine A1.

#8

Microdiagnostics load — Yes

#9 No

A

PANEL 150

1

1

#12 Tests fail — Yes

No

At the 3350 Power Panel:
Disable and then Enable both interfaces.

#13

Microdiagnostics
Run string switch microdiagnostic routines B6 and BC. See MICRO 70 and MICRO 82 for detailed operating instructions.

#15 Tests fail — Yes

No

Error Analysis
Exit to the MICRO section and follow instructions under the first failing Error Code.

#11

MICRO

#15 Fault Symptom Code 1910 — Yes

#17 No

#15 Fault Symptom Code 1915 — Yes

No

Return to the FSI section and replace the cards listed and perform the additional action under the failing Fault Symptom Code.

#16

FSI

#18

Replace Cards
A2D2 (SWFE A)
A2E2 (SWFE B)
A2G2 A2F2
A2L2 A2Q2

When replacing A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

#21

#19

Replace Cards
A2M2 (SWFE)
A2D2 } SWFE A
A2H2 }
A2E2 } SWFE B
A2J2 }

When replacing A2D2 or A2E2, check the addressing jumpers. See INST 6.

#22

Trouble corrected — No

CTL-I 809 #23

Yes

Trouble corrected — Yes

#22 No

C

DEV-I 410

Yes

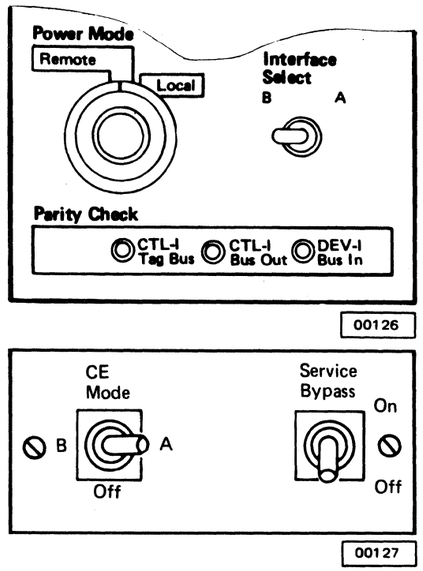
Maintenance procedure complete.

#24

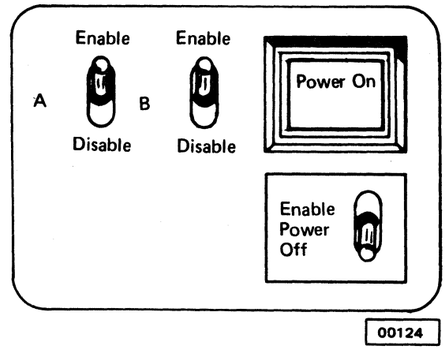
A

START 500

3350 CE Panel



3350 Power Panel



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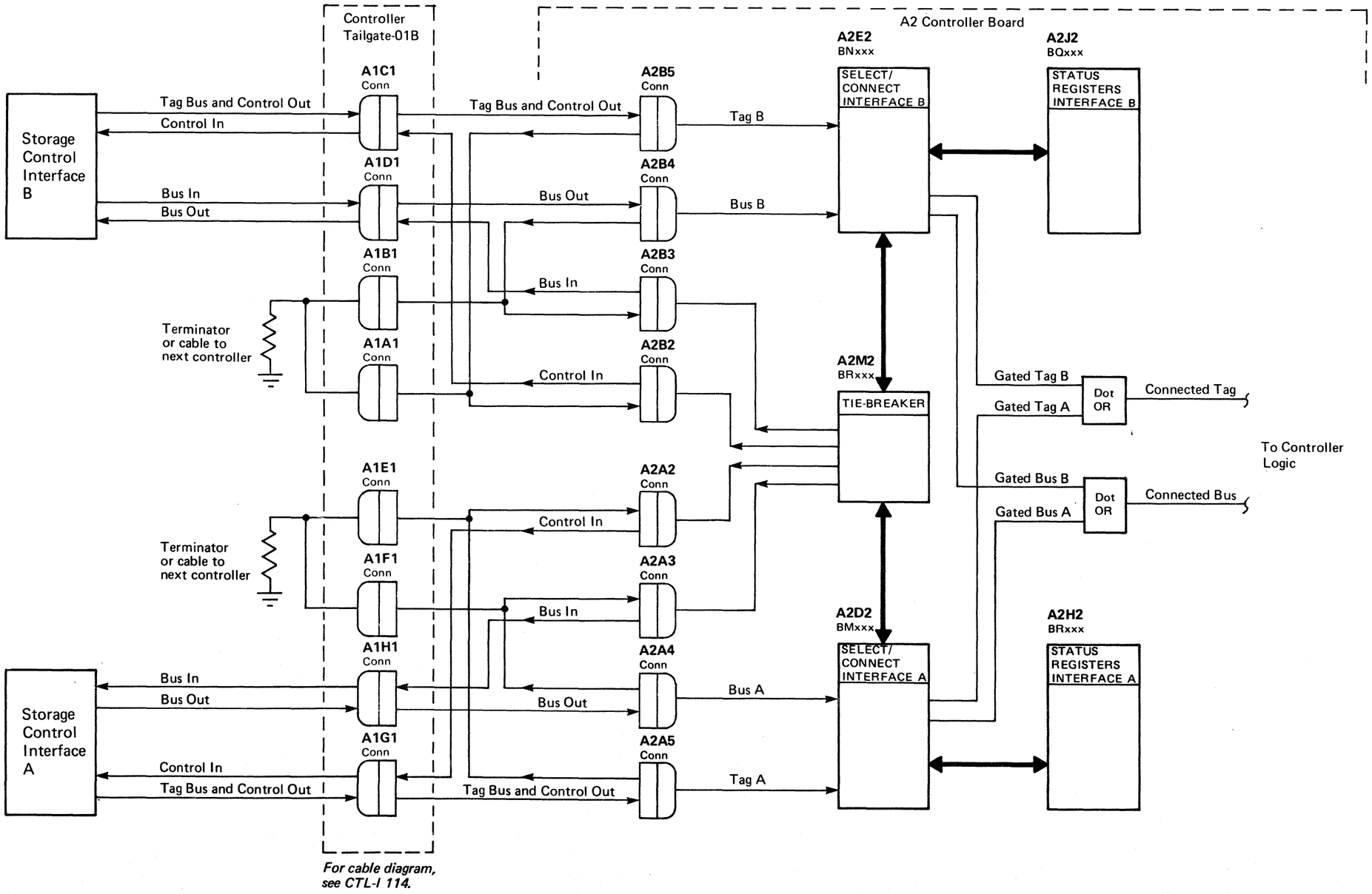
STRING SWITCH OVERVIEW

See OPER 261 for theory.



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ERROR ALERT

Circuit Description

Error Alert is caused by one of two conditions:

1. Controller Chk (A)
2. Read/Write Check from the device (bit 3) (G)

Controller Check can be caused by intermittent bits from storage control on Bus Out (D) or Tag Bus (E).

Read/Write Check (Device Bus In Bit 3 NPL) causes an Error Alert when Rd Wrt Latch and Dld Tag Response (H) are both active. See A2F2 Logic Diagram (inset).

Analysis Procedure

To determine which condition is causing the Error Alert:

Controller Check – Loop microdiagnostic routine A1, test 4. See CTL-I 410 and 412 for scoping procedure and diagrams.

Read/Write Check – Loop microdiagnostic routine B8, test D. See CTL-I 640 and 642 for scoping procedure and diagrams.

If string switch is installed, Bus Out (D) and Tag Bus (E) come from A2D2 for Interface A and A2E2 for Interface B.

See CTL-I 808 for string switch overview.

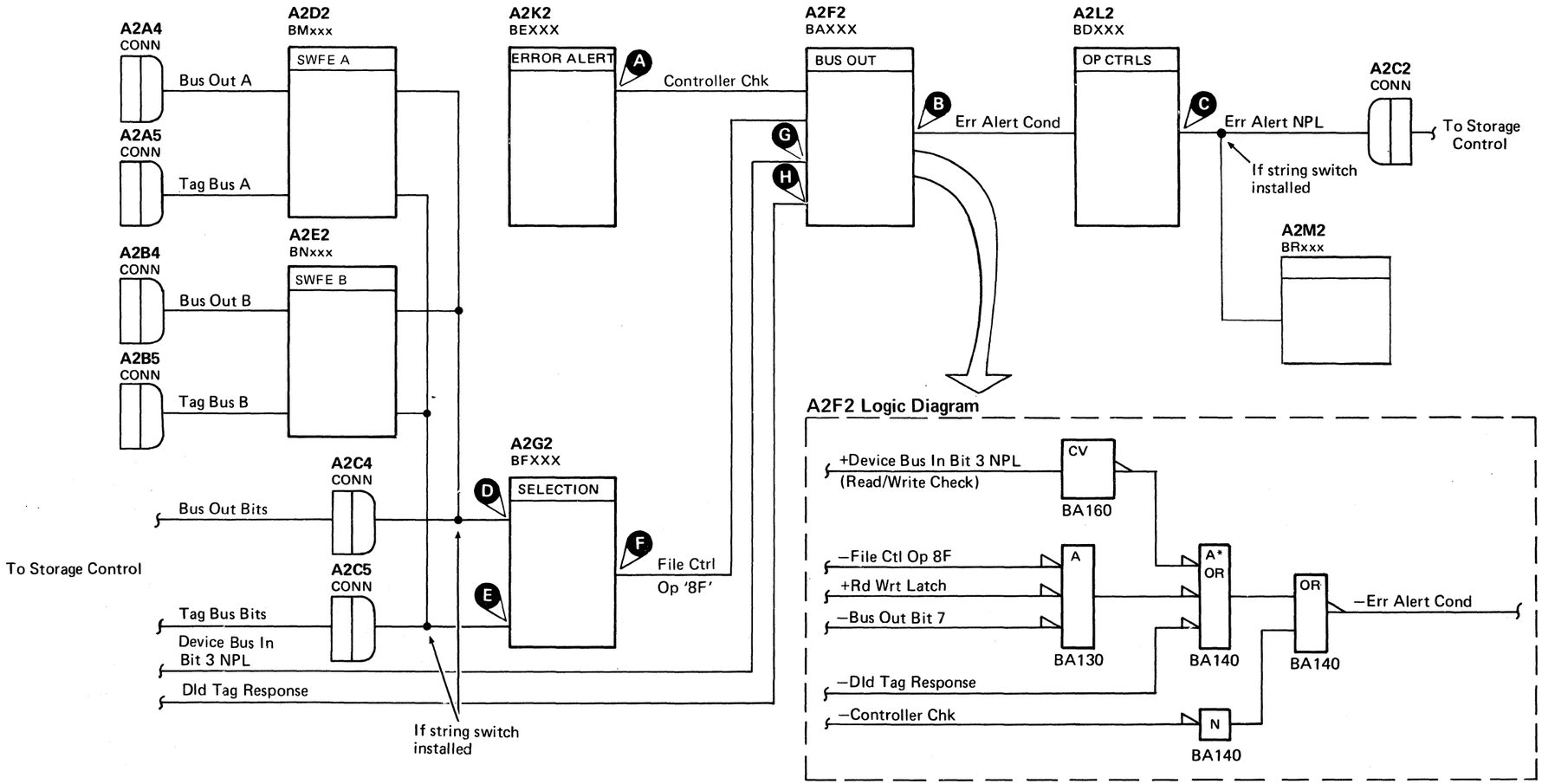
Additional Service Hints

1. Check the −4 V and +6 V for a stable and proper level. See PWR 90, Entry B for procedure.

   Note: *Adjusting the −4 V or +6 V regulators out-of-spec can cause an intermittent failure to become less intermittent.*

2. Verify that cards and connectors are properly seated.
3. Check to see if an Engineering Change has been recently installed.

See OPER 241 for additional theory.



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NORMAL END MISSING

Circuit Description

See the diagram on CTL-I 812 for referenced test points.

Each Read (Tag '0E'), Write (Tag '0F'), ECC Correct (Tag '08') and Set Read/Write (Tag '85') operation must terminate with a Normal End or Check End response.

Fault Symptom Code 9002 indicates Normal End was not received for:

Set RW Op '85' (F)
Read Op '0E' (G)
Write Op '0F' (J)

SET R/W OP '85'

Normal End (M) turns on when Op End (L) is active and no check conditions are detected.

As shown in the logic diagram for A2P2:

- Op End normally turns on when End Data Op is received.
- Selected Tag Gate and Read* Not Clk Gated are inactive (+MST-1) before End Data Op is received.
- When a Set RW Op '85' is complete, End Data Op is activated by PLO End Op and Bit Ring 6 Pwr.

As shown in the logic diagram for A2Q2:

- When Set RW (Tag '85')is first issued, Reset End Cond is active (+MST-1) because Rd Wrt Latch is inactive (+MST-1).
- VFO Good is also inactive (+MST-1), therefore PLO End Op is inactive (−MST-1).
- Tag 85 now activates Rd Wrt Latch.
- Rd Wrt Latch activates VFO Good (−MST-1) and causes Reset End Cond to go to −MST-1.
- An inactive Reset End Cond keeps Resp Rd * Wr Latch inactive.
- VFO Good and Resp Rd * Wr Latch, both at −MST-1, activates PLO End Op.

When the storage control receives Normal End, it sends back End Response (A). End Response activates Reset End Cond (E).

- Reset End Cond activates Resp Rd * Wr Latch. This causes PLO End Op to return to −MST-1.

READ OR WRITE OP

When a Read Op '0E' or a Write Op '0F' is complete, End Data Op (Q) is activated by End Data, Rst Run ECC TP, and ECC Set.

Analysis Procedure

Determine which of the following lines is causing Op End to fail:

−End Data Op (Q)
−Selected Tag Gate (D)
−Read*Not Clk Gated (H)

If End Data Op is the problem, determine whether the Set RW Op '85', the Read or Write Op path is the cause. Looping the microdiagnostic may help to determine the failing path.

Set RW Op '85' – Loop routine B8, test D. See CTL-I 640 for scoping procedure.

Write Op '0F' – Loop routine AD, test 1. See CTL-I 660 for scoping procedure.

Read Op '0E' – Loop routine AF, test 1. See CTL-I 660 for scoping procedure.

Additional Service Hints

1. Check the −4 V and +6 V for a stable and proper level. See PWR 90, Entry B for procedure.

   Note: *Adjusting the −4 V or +6 V regulators out-of-spec can cause an intermittent failure to become less intermittent.*

2. Verify that cards and connectors are properly seated.
3. Check to see if an Engineering Change has been recently installed.

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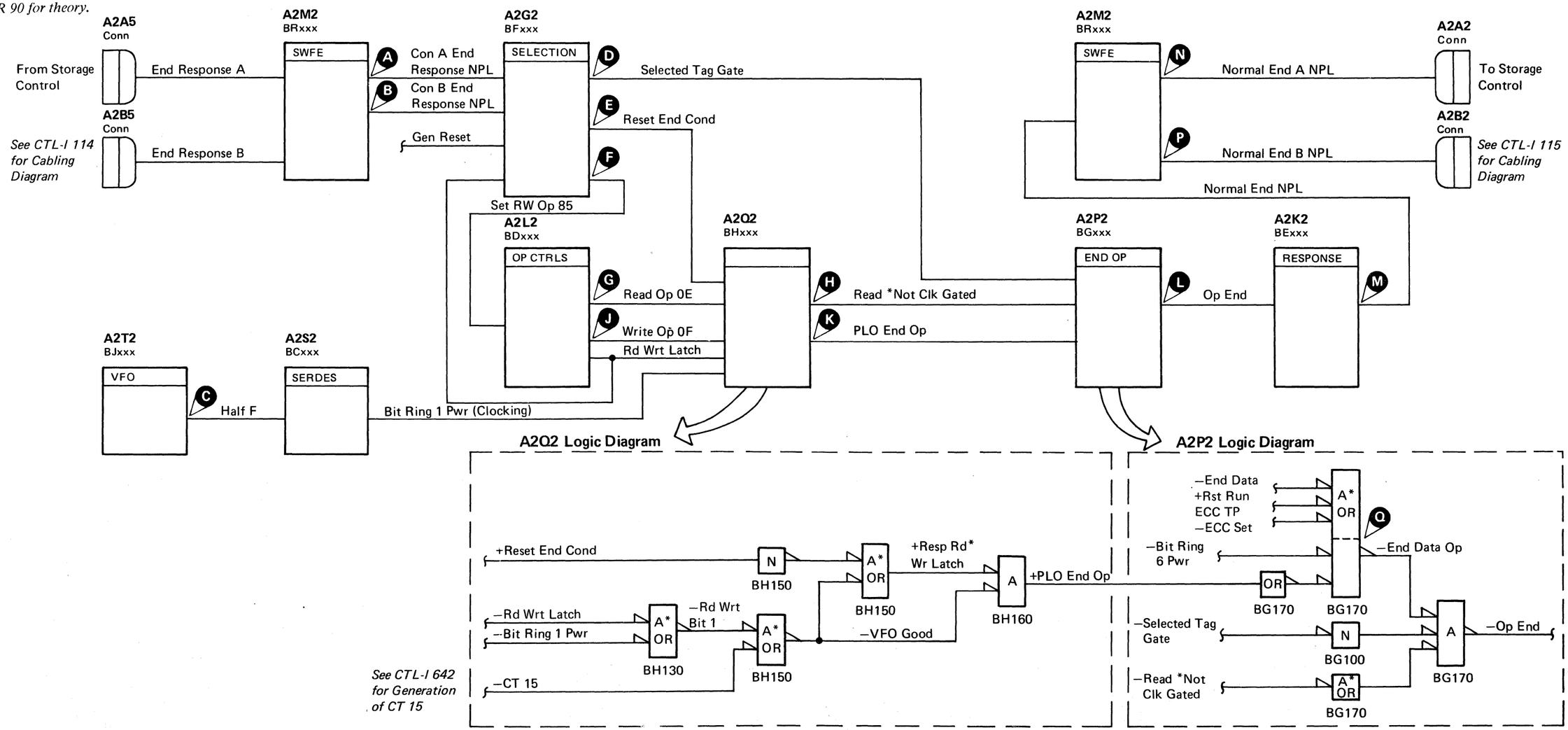
NORMAL END MISSING

See OPER 90 for theory.



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MULTIPLE CONTROLLERS SELECTED (Fault Symptom Code 9006)

Circuit Description

When a controller is selected by Tag '03' or '83', it responds with the controller address on Bus In.

Sense Byte 13 contains the address of the controller desired.

Sense Byte 14 contains the address and compliment returned by the selected controller.

Analysis Procedure

1. Check Sense Byte 13 for the correct value:

Controller Selected	Value in Sense Byte 13
0	07
1	26
2	45
3	64

2. Check Sense Byte 14 for returned address.

   If one bit has been dropped, scope the Contr Bus In bit by looping microdiagnostic routine A1, test 2.

   See CTL-I 250, Entry B (basic 3350) or CTL-I 254, Entry B (string switch installed) for scoping procedure.

   If value is 00, suspect the following lines:

   Gate BI (F)
   BI Sel X (D)
   BI Sel Y (E)
   Tag Bits (A)
   Status Bytes Op 04 (B)
   Tag Valid NPL (G)

   If value is '80', suspect Contrlr Poll Op 02 (C).

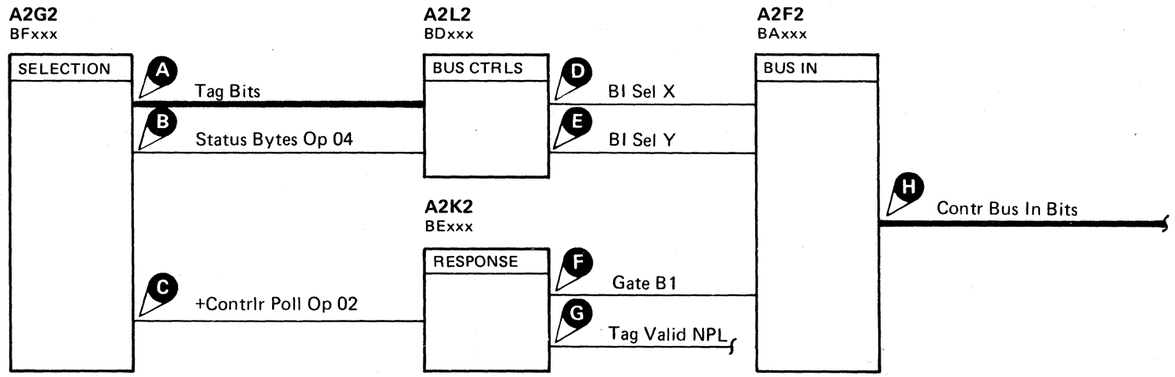
Additional Service Hints

1. Check the −4 V and +6 V for a stable and proper level. See PWR 90, Entry B for procedure.

   Note: *Adjusting the −4 V or +6 V regulators out-of-spec can cause an intermittent failure to become less intermittent.*

2. Verify that cards and connectors are properly seated.
3. Check to see if an Engineering Change has been recently installed.

See OPER 110 for additional theory.



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ALWAYS ACTIVE LINES (Fault Symptom Code 9007)

Circuit Description

Prior to selection, the control lines are tested for their zero state. If any one or more is not zero, an error is indicated.

End Data Op (C) activates Op End (D).

Op End turns on Normal End (one of the control lines).

Freeze Correct Op (A) or TR Index (B) activates Index Alert (E) and Err Alert NPL (G).

Analysis Procedure

Two microdiagnostic tests may be looped to help determine the cause of failure.

Loop routine A1, test 1. See CTL-I 202 (basic 3350) or CTL-806 (string switch installed) for scoping procedure and sequence diagram.

This test exercises the control lines (F) and Err Alert NPL (G).

Also loop routine A1, test 2.

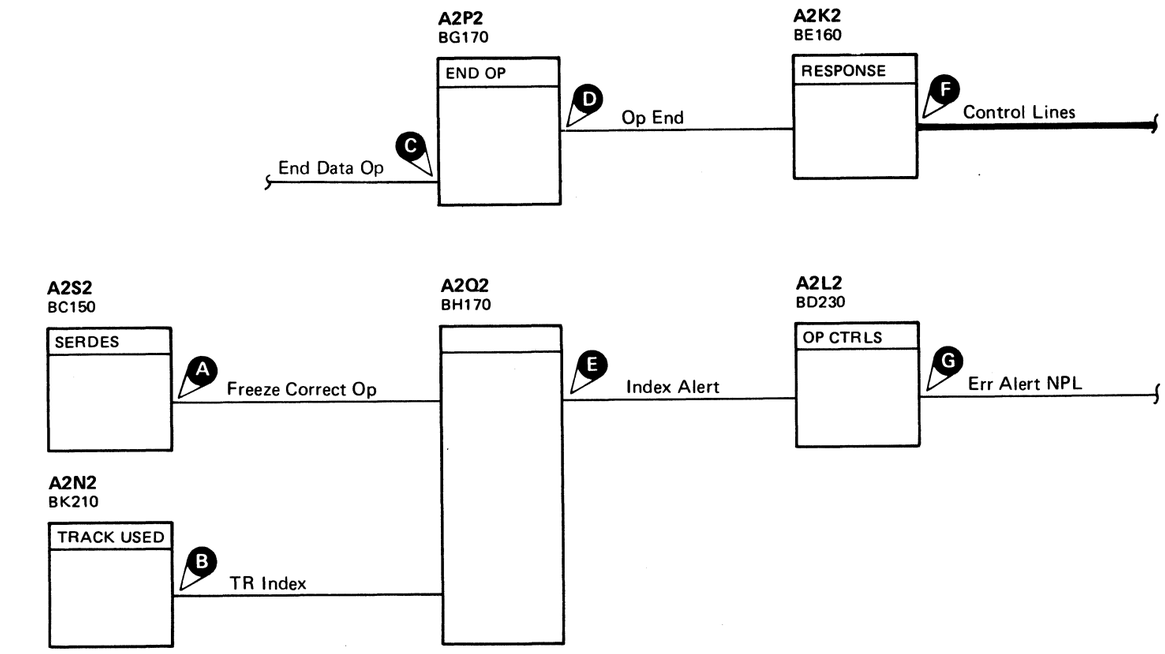
Additional Service Hints

1. Check the −4 V and +6 V for a stable and proper level. See PWR 90, Entry B for procedure.

   Note: *Adjusting the −4 V or +6 V regulators out-of-spec can cause an intermittent failure to become less intermittent.*

2. Verify that cards and connectors are properly seated.
3. Check to see if an Engineering Change has been recently installed.

See OPER 241 for additional theory.



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CONTROLLER BUS IN PARITY CHECK (Fault Symptom Codes 9108 and 9188)

Circuit Description

On operations where the Data Bits (B) or the Cntrl Bus In Bits (E) must maintain good parity, the input to the Bus In drivers is checked for proper parity. If parity is bad, the Contr Bus In Par Chk Latch (F) is set.

Analysis Procedure

Data Bits – Loop microdiagnostic routine A1, test 5. Refer to CTL-I 534 (basic 3350) or CTL-I 536 (string switch installed) for scoping procedure and sequence diagrams.

This routine checks for all data bits on.

Also loop microdiagnostic routine AD, test 7 for a check of all data bits off.

Note: *Write Mode (A) must be operating correctly for Data Bits to be good.*

Sel Bus Bits – Loop microdiagnostic routine A2, test 4. This routine checks for Sel Bus Bits off.

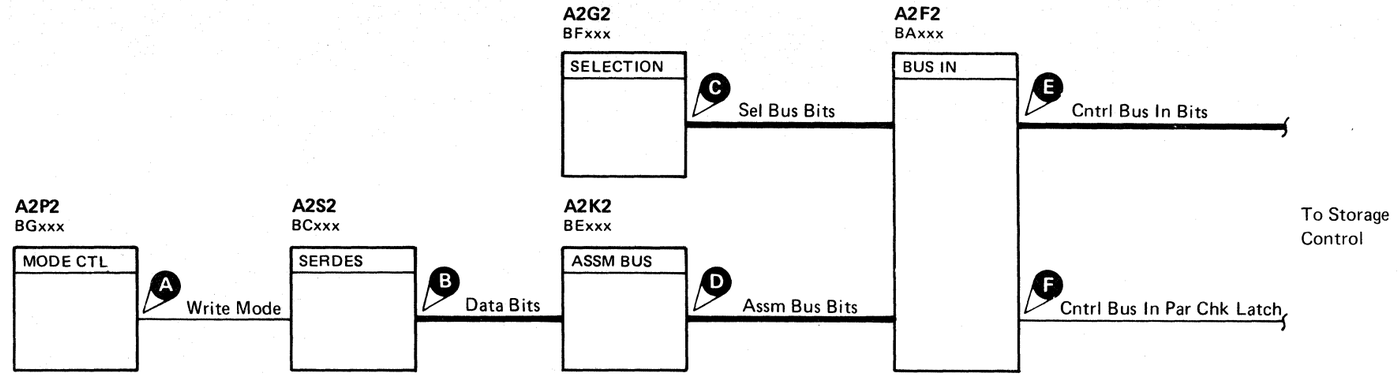
Additional Service Hints

1. Check the −4 V and +6 V for a stable and proper level. See PWR 90, Entry B for procedure.

   Note: *Adjusting the −4 V or +6 V regulators out-of-spec can cause an intermittent failure to become less intermittent.*

2. Verify that cards and connectors are properly seated.
3. Check to see if an Engineering Change has been recently installed.

See OPER 241 for additional theory.



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STORAGE CONTROL DETECTED FAILURE

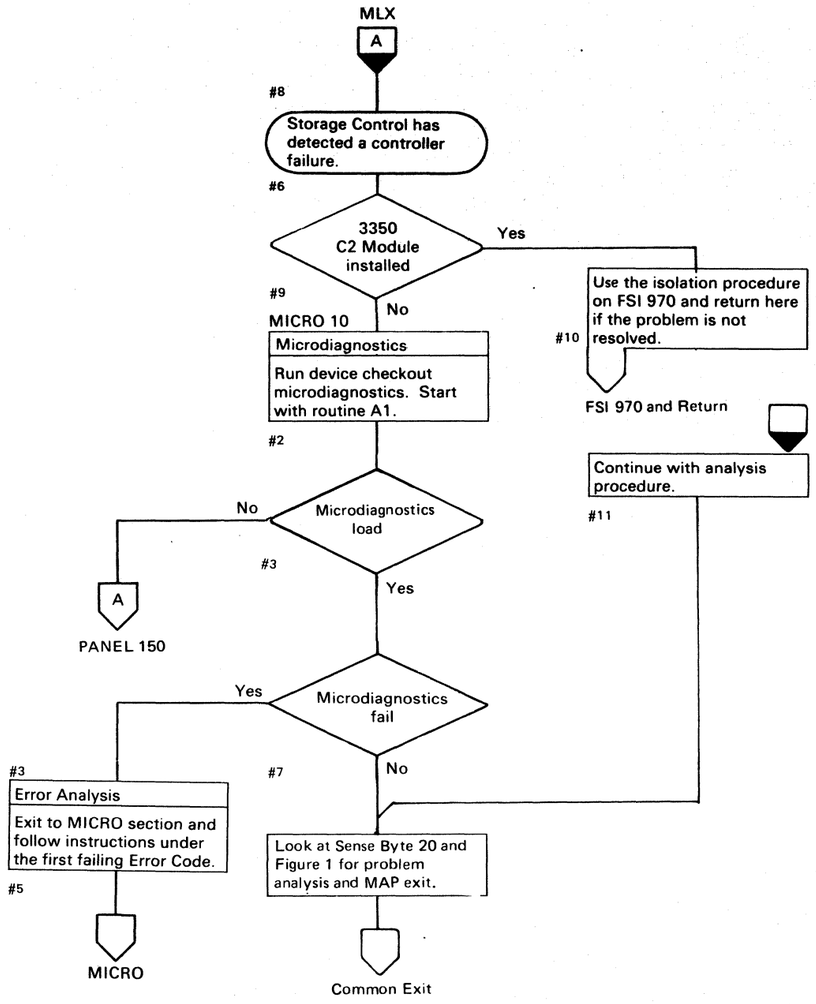

Figure 1. Controller Errors

Sense Byte 20	Possible Causes	Error Description	Logic Lines related to error.	MAP Exit	Additional Action
Bit 3 = 1	A2P2 A2Q2 A2G2* A2S2 A2K2 A2C5 (Conn) A2D2* } SWFE A A2A5 (Conn) } SWFE A A2E2* } SWFE B A2B5 (Conn) } SWFE B	Unexpected end during data response.	Recycle Tag NPL Reset End Cond PLO End Op	DATA 100 CTL-I 282	Some latch is failing to reset. See ALD BF160.
Bit 2 = 1	A2F2 A2C3 (Conn) A2H2 A2D2* } SWFE A A2A3 (Conn) } SWFE A A2J2 A2E2* } SWFE B A2B3 (Conn) } SWFE B	Buffer Bus In Parity check. Storage control detected a Bus In Parity check from the controller.	Contr Bus In Bit P	CTL-I 520	
Bit 1 = 1	A2K2 A2G2* A2C2 (Conn) A2C5 (Conn) A2D2* } SWFE A A2M2 } SWFE A A2A2 (Conn) } SWFE A A2A5 (Conn) } SWFE A A2E2* } SWFE B A2M2 } SWFE B A2B2 (Conn) } SWFE B A2B5 (Conn) } SWFE B	Select Active without Select Hold.	Select Active NPL	CTL-I 260	
Bit 6 = 1	A2P2 A2G2* A2C5 (Conn) A2D2* } SWFE A A2A5 (Conn) } SWFE A A2E2* } SWFE B A2B5 (Conn) } SWFE B	Control Interface Transfer check.	Recycle	CTL-I 660	Loop microdiagnostic routine AD, test 1.

When replacing A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

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FALSE CONTROLLER ERROR (Fault Symptom Code 9200)

A Controller Check has been detected, but is not further defined. Sense Bytes 17 and 20 normally define the Error Latch that caused the Controller Check.

Circuit Description

SENSE BYTE 20 IS NOT '00'.

This error is due to incorrect gating through the Check Reg or Assm Reg (G). Each Error Latch is gated through the Check Reg by:

- Gate Controller Err 1 (See ALD BE120)
- Gate Controller Err 2 (See ALD BE120)

Incorrect gating occurs if ECC Ctrl Op 08 (E) or ECC Correct Op (F) is active.

The check bit is gated through the Assm Reg by:

- Assm Sel Y inactive (D).
- Assm Sel X inactive.

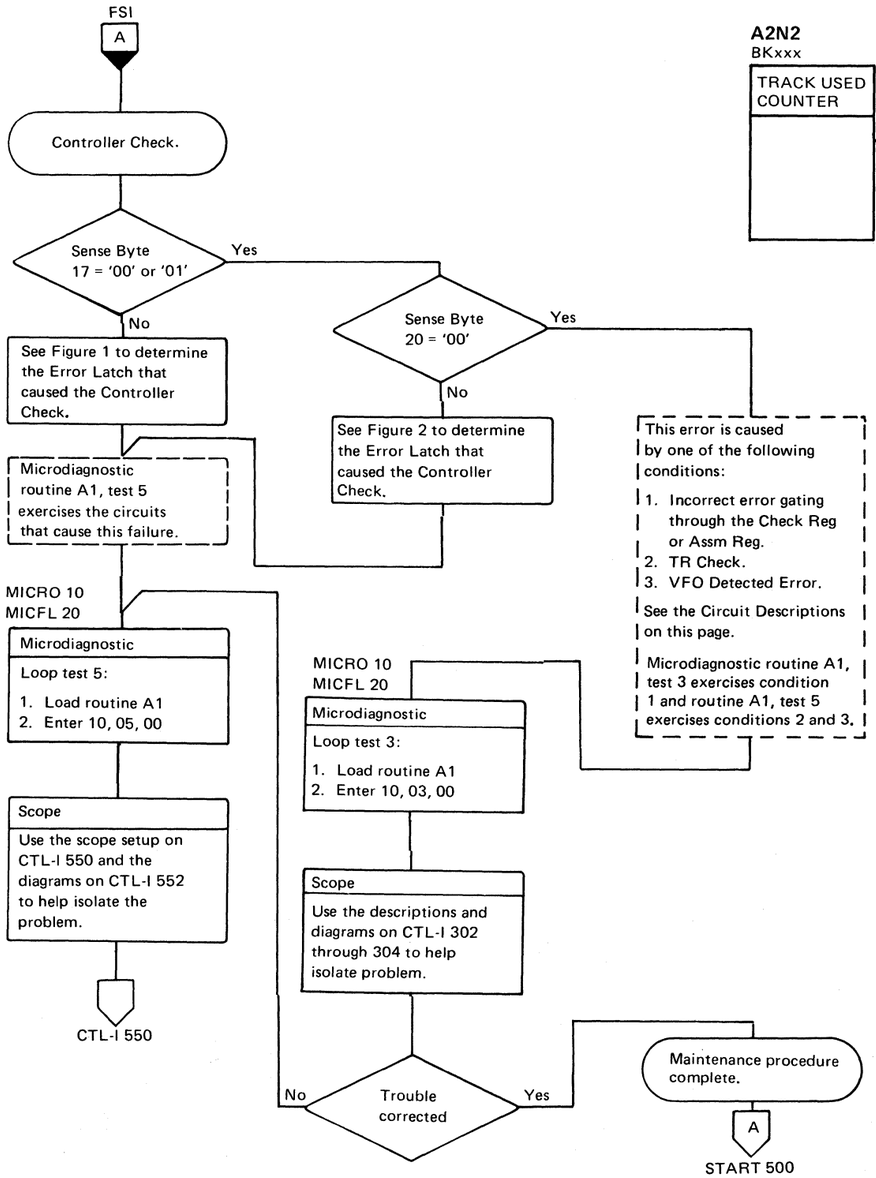
SENSE BYTE 17 IS '00' and SENSE BYTE 20 IS '00'.

This error is caused by TR Check or VFO Detected Error.

TR Check (A) activates TR*Reorient Ck (B) and causes a Controller Check (G).

VFO Detected Error (C) causes a Controller Check (G).

See OPER 241 for additional theory.



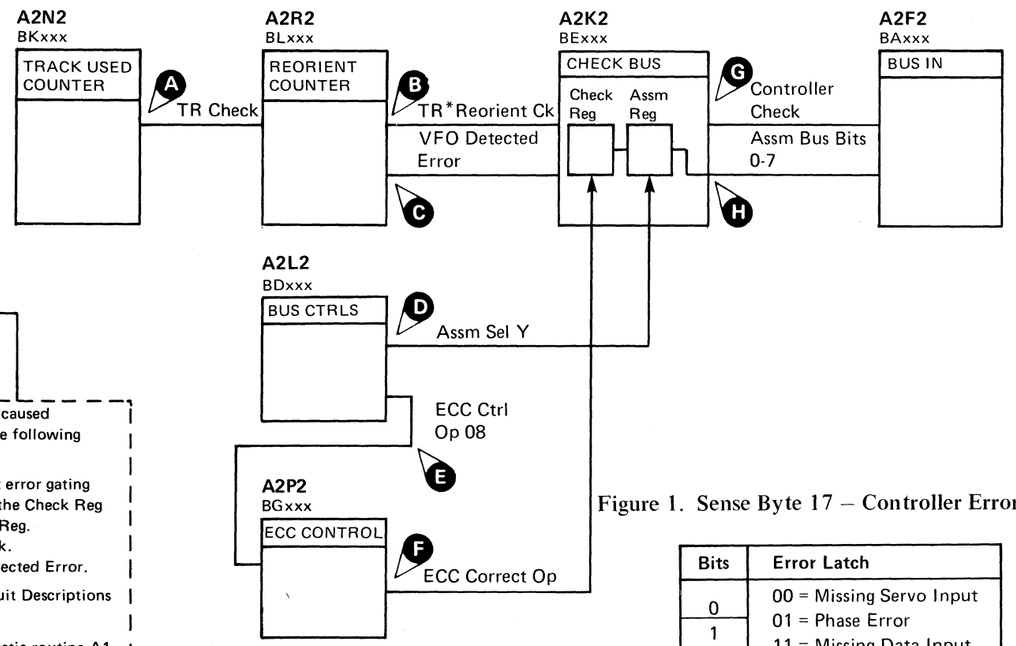


Figure 1. Sense Byte 17 – Controller Error 2

Bits	Error Latch
0	00 = Missing Servo Input 01 = Phase Error 11 = Missing Data Input
1	
2	SERDES Data Check
3	Gap Counter Check
4	Write Data Check
5	Monitor Check
6	ECC Check

Figure 2. Sense Byte 20 – Controller Error 1

Bits	Error Latch
0	Tag Bus Parity Check
1	Bus Out Parity Check
2	Drive Select Error
3	Device Bus In Parity
4	CTL-I Bus In Parity
5	I Write Fail
6	Index Check
7	Reorient Check

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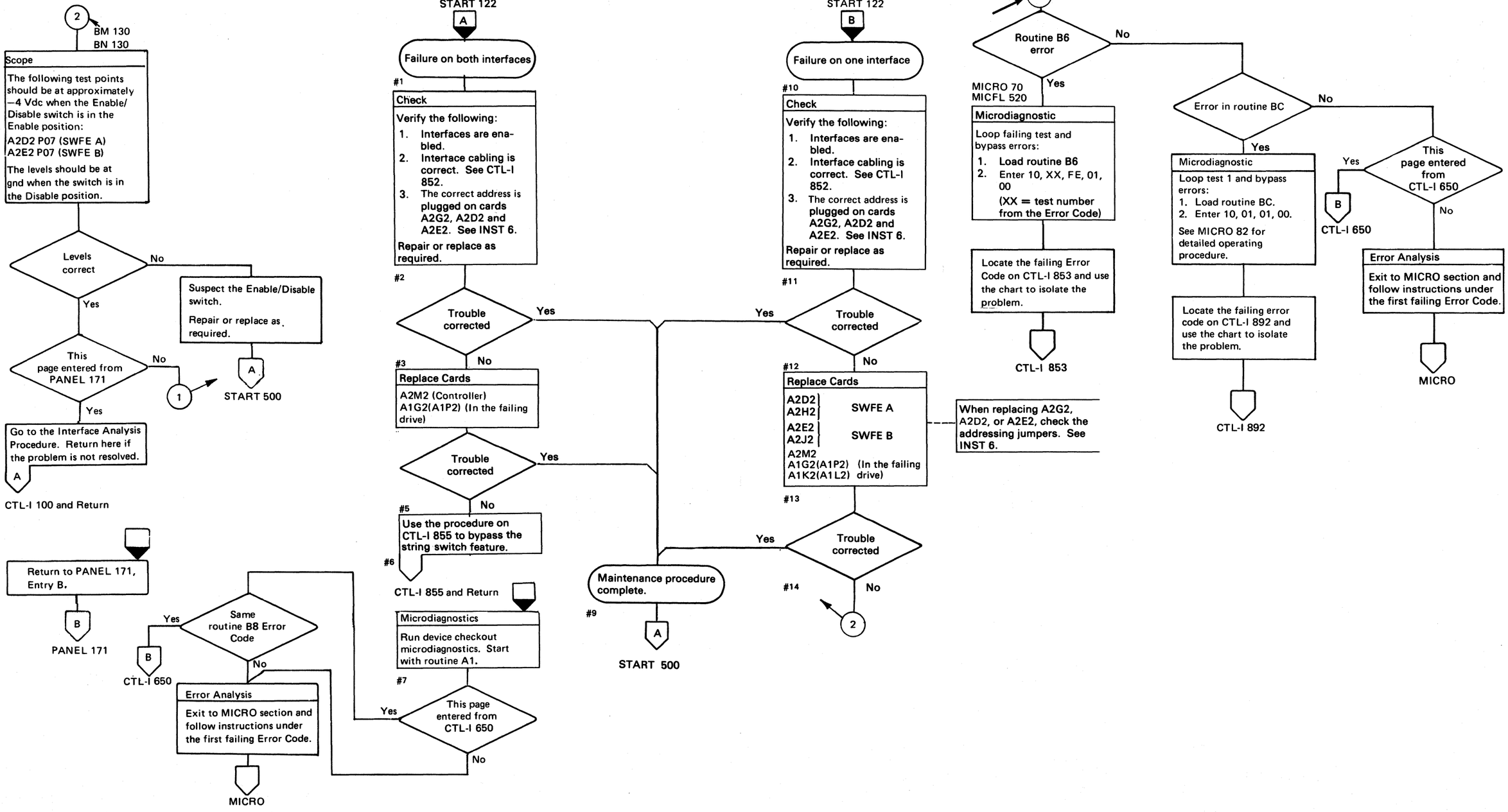
STRING SWITCH INTERFACE ANALYSIS

See CTL-I 852 for string switch overview.



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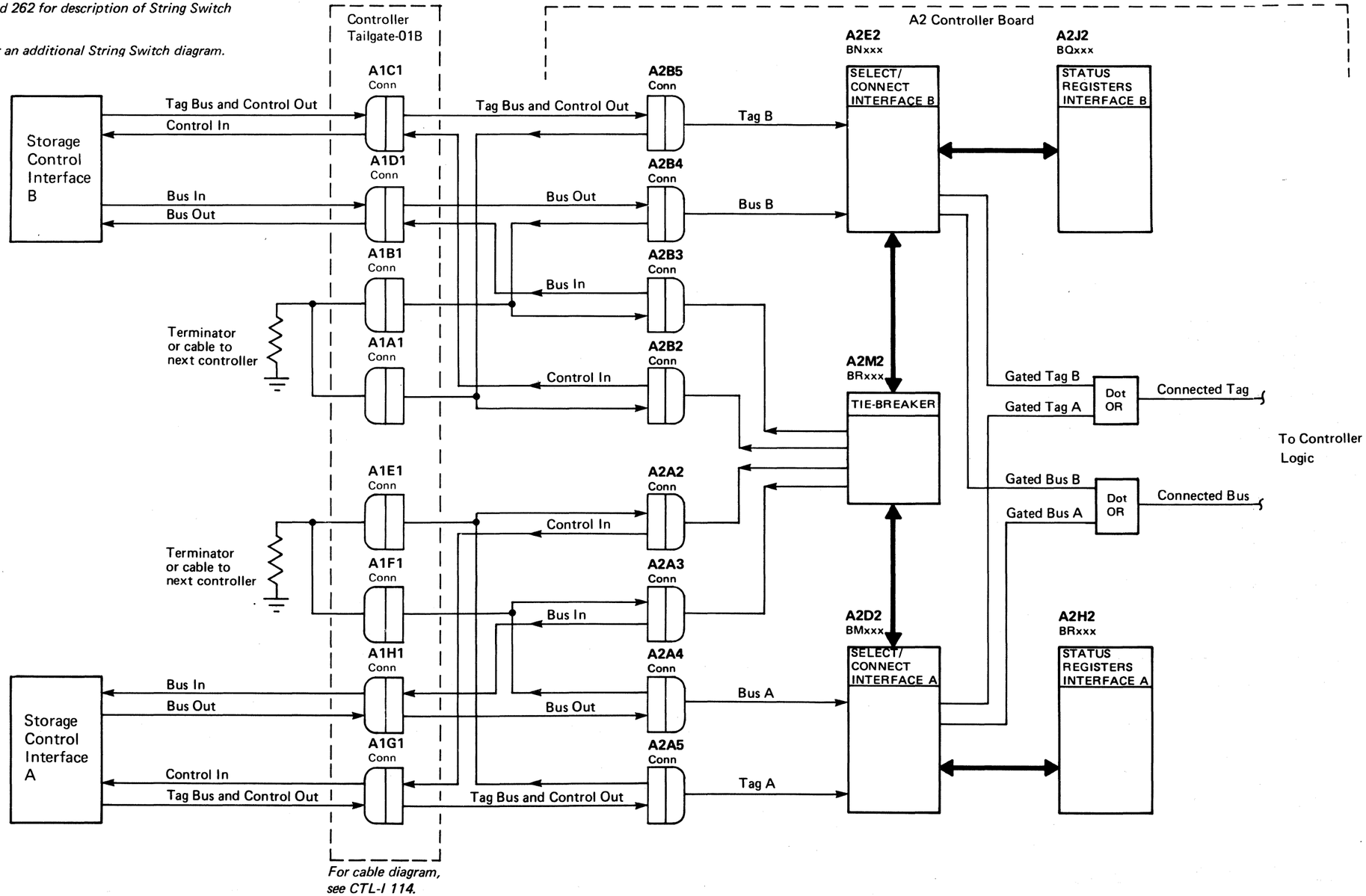
STRING SWITCH OVERVIEW

See OPER 261 and 262 for description of String Switch operation.

See CTL-I 890 for an additional String Switch diagram.



For cable diagram, see CTL-I 114.

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STRING SWITCH FAILURE ANALYSIS

Error Code	Error Description	Suspected Logic Lines	Possible Causes				Comments	MICFL Reference
			Interface A		Interface B			
			ALD	Card	ALD	Card		
B615 B616 B617	Failed to receive Index Alert with a short connection.	–Set Long Con Ltch –Sel Ltch –Selecting	BM140 BR120 BR120	A2D2 J13 A2M2 D12 A2M2 P10	BN140 BR120 BR120	A2E2 J13 A2M2 B10 A2M2 P06	Set Long Con Ltch sets long connection. If long connection is set, Index Alert is not returned. –Sel Ltch, +Selecting, and Short Con Latch TP activate –Wait. –Wait and –Normal End Switch activate –Wait. Alert.	
B619 B61A B61B	Index Alert fails to turn off.	–Set Long Con Ltch –Sel Ltch –Selecting	BM140 BR120 BR120	A2D2 J13 A2M2 D12 A2M2 P10	BN140 BR120 BR120	A2E2 J13 A2M2 B10 A2M2 P06	Set Long Con Ltch sets long connection. If long connection is set, Index Alert is not returned. –Sel Ltch, +Selecting, and Short Con Latch TP activate – Wait. –Wait and –Normal End Switch activate –Index Alert.	
B61D B61E B61F	Unable to select the Service Drive.	–Sel Ltch –Allow Sel Set	BR110 BR100	A2M2 B10 A2M2 J13	BR110 BR100	A2M2 D12 A2M2 G11	–Sel Ltch activates –Allow Sel Set. –Allow Sel Set is necessary to set the Select Latch.	
B621 B622 B623	Failed to receive Tag Valid or Normal End for Tag '07'.	+Tag '07'	BM150	A2D2 J10	BN150	A2E2 J10	Tag '07' inactive causes a Check 1-of-6 which prevents Tag Valid.	MICFL 520
B625 B626 B627	Failed to detect Select Active during partial select.	–Allow Par Sel Set –Set Long Con Ltch	BR100 BM140	A2M2 P09 A2D2 J13	BR100 BN140	A2M2 P05 A2E2 J13	–Allow Par Sel Set must be active to set the Partial Select Latch. The Partial Select Latch and Coerce Tag Valid activate Sel Active. Allow Par Sel Set is activated only if Long Connection is set on the opposite interface. Long Connection cannot set if –Set Long Con Ltch is inactive.	
B629 B62A B62B	Short Busy indicator remains active when Long Connection is set.	–Short Con Ltch TP	BR120	A2M2 M09	BR120	A2M2 M09	The set of the Long Con Ltch resets the Short Con Ltch. Short Connection activates Wait, which causes an Index Alert.	
B62D B62E B62F	Failed to detect a Partial Select with Long Connection set.	+Non Selecting Valid Tag –Tag '01' –Busy	BM150 BM150 BR150	A2D2 J10 A2D2 J06 A2M2 P12	BN150 BN150 BR160	A2E2 J10 A2E2 J06 A2M2 M03	Non Selecting Valid Tag and Partial Select Latch activate Gate BI. Gate BI gates the Bus In Bits. If Non Selecting Valid Tag is always active, the bits are not gated to Bus In. Tag '01' active causes a Check 1-of-6, preventing a Normal End or Tag Valid. –Busy becomes BI bit 3, which should be active and indicates Partial Select.	
B6E1 B6E2 B6E3	The Enable/Disable switch disabled the interface with the Disable Interlock Latch still set.	–Enable Latch	BM170	A2D2 M09	BN170	A2E2 M09	The Enable Latch should remain set with the Enable/Disable switch set to Disable.	
B6E5 B6E6 B6E7	The Enable Latch cannot be reset.	–Enable Latch	BM170	A2D2 M09 A2H2	BN170	A2E2 M09 A2J2	The Dislock Latch resets with Tag '07' Bus '10' and Sel Active if the Enable/Disable switch is set to Disable.	
B6E9 B6EA	The Enable Latch cannot be set again by turning the Enable/Disable switch to Enable.	–Enable Latch	BM170	A2D2 M09	BN170	A2E2 M09	The Enable Latch should become active with the Enable/Disable switch set to Enable.	
B6ED B6EE B6EF	Registers fail to reset with the interface disabled.	–Enable Latch	BM170	A2D2 M09 A2H2	BN170	A2E2 M09 A2J2	The Enable Pwr Lines are inactive with the Enable Latch inactive. All registers are reset by the inactive Enable Pwr Lines.	

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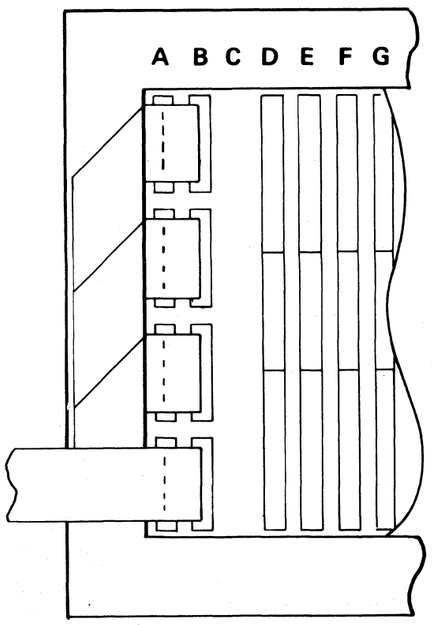
STRING SWITCH BYPASS PROCEDURE

STRING SWITCH INSTALLED

- Flat cables from interface B are plugged to sockets A2B2, A2B3, A2B4, A2B5.
- Flat cables from interface A are plugged to sockets A2A2, A2A3, A2A4, A2A5.
- Discrete-wire cable from CE Panel and Power Panel is plugged into socket A2V3.
- Feature cards are installed at:

A2D2	A2J2
A2E2	A2M2
A2H2	

Controller A2 Board



PROCEDURE 1. CONNECT INTERFACE B DIRECTLY TO CONTROLLER.

1. Turn both interface switches to Disable.
2. Remove power.
3. Move interface B flat cables from sockets in column B to sockets in column C.

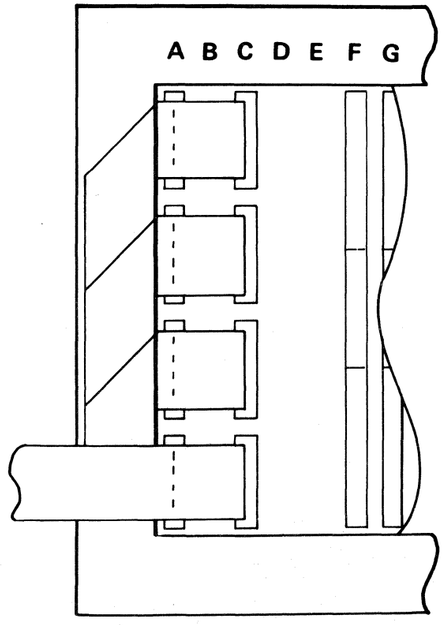
   Interface A flat cables remain in column A.

   Discrete-wire cable remains in A2V3.
4. Remove cards:

A2D2	A2J2	
A2E2	A2M2	(If C2 Module is installed, do not remove A2M2.)
A2H2		

5. Plug A2G2 address compare jumper to active (see INST 6).
6. If C2 Module is installed, perform Steps 1 through 5 on both controllers.

Controller A2 Board



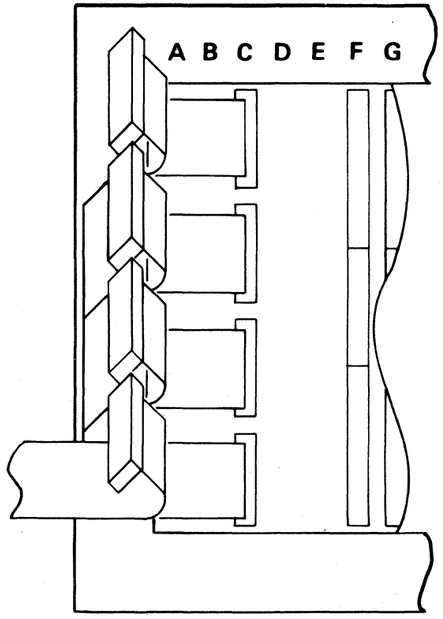
PROCEDURE 2. CONNECT INTERFACE A DIRECTLY TO CONTROLLER.

1. Turn both interface switches to Disable.
2. Remove power.
3. Remove interface B flat cables from sockets in column B and fold back out of the way.
4. Move interface A flat cables from sockets in column A to sockets in column C. Discrete-wire cable remains in A2V3.
5. Remove cards:

A2D2	A2J2	
A2E2	A2M2	(If C2 Module is installed, do not remove A2M2.)
A2H2		

6. Plug A2G2 address compare jumper to active (see INST 6).
7. If C2 Module is installed, perform Steps 1 through 6 on both controllers.

Controller A2 Board



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MISSING INTERRUPT (With String Switch)

Device Interrupts originate from each drive or from string switch status cards A2H2 (Interface A) or A2J2 (Interface B). The interrupts coming from each drive are identified by reading Drive Status (Tag '84'):

- Attention
- Seek Complete
- Sector Compare

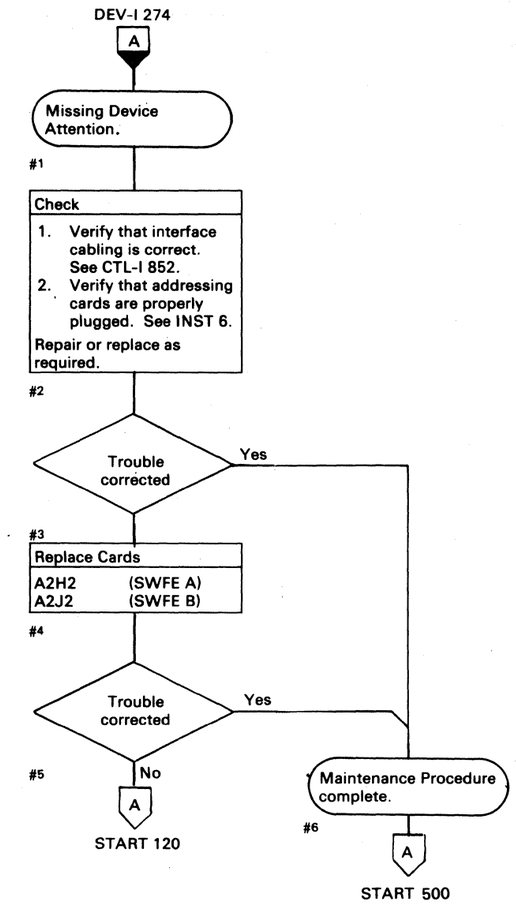
The resulting Device Attentions bypass the controller and are sent to the proper control interface by the string switch.

The interrupts originating from the string switch status cards are identified by reading Switch Status (Tag '06'):

- Device End (Primed interrupt for Busy)
- Pack Change

All interrupts pass through string switch and are removed from one interface for all devices assigned to the other interface.

See OPER 261 and 262 for a detailed description of the string switch feature. .



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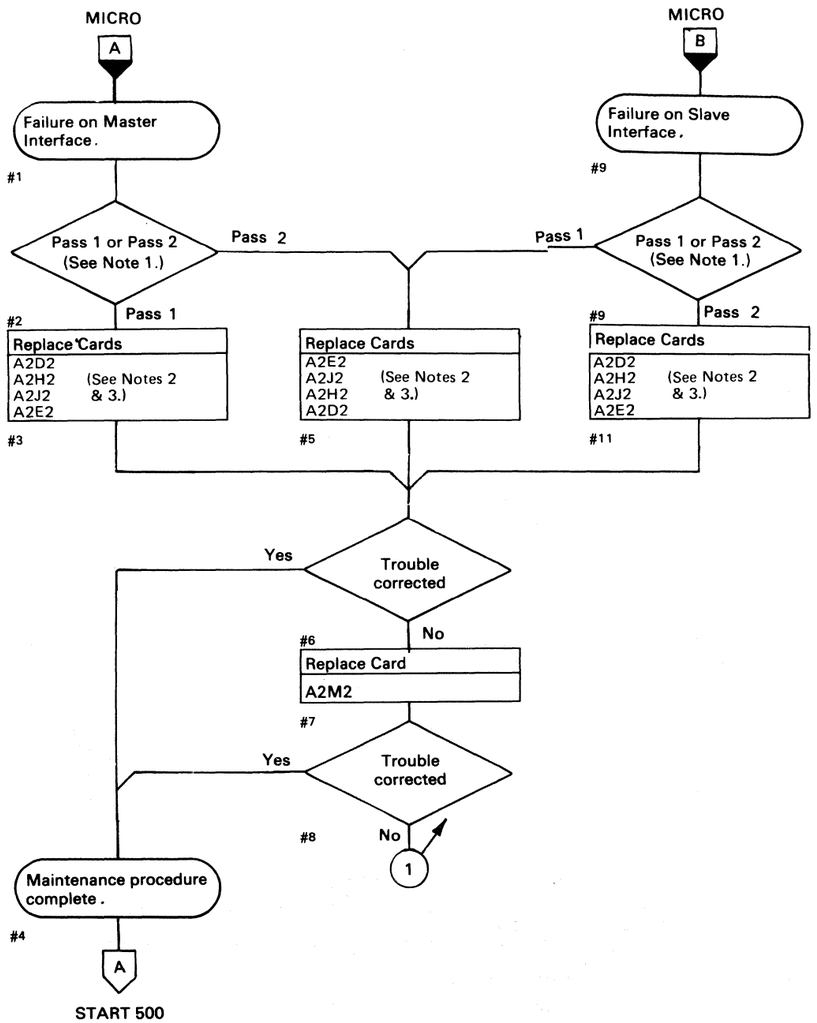
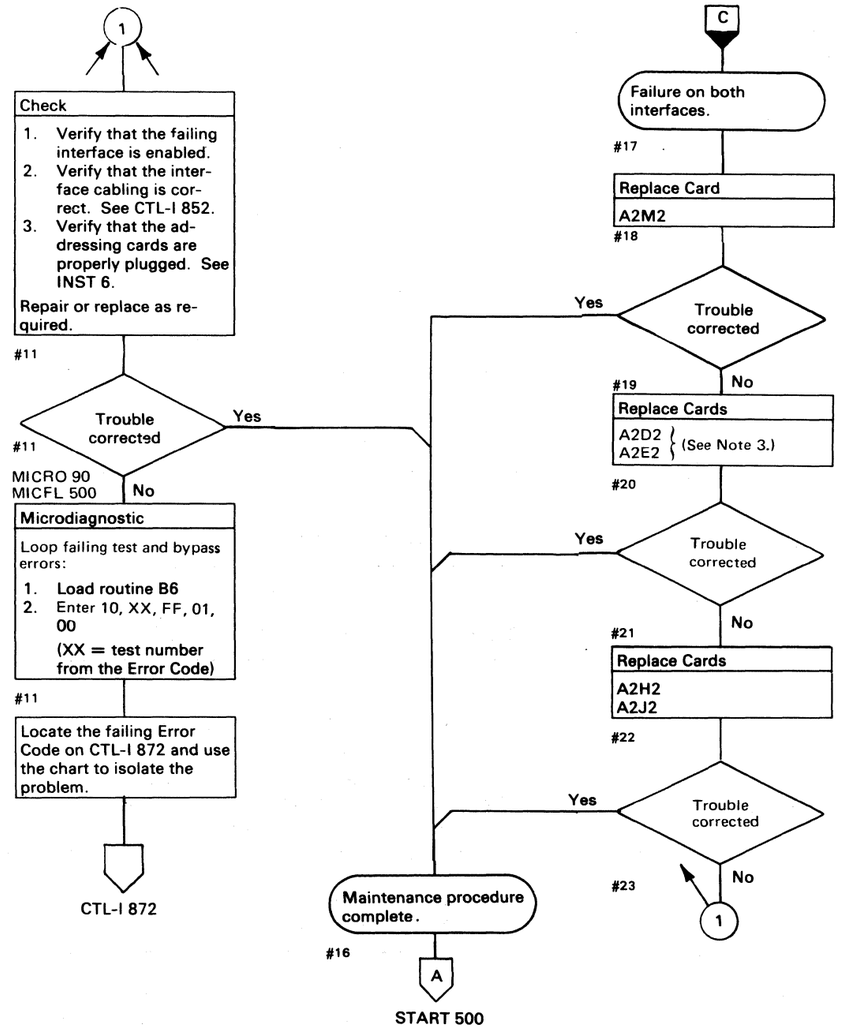
INTERFACE FAILURE (With String Switch)





Note 1: *See routine B6 operating procedures on MICFL 520.*
Pass 1:
Master = Interface A
Slave = Interface B
Pass 2:
Master = Interface B
Slave = Interface A

Note 2: *For isolation purposes, Interface A cards may be swapped with Interface B cards.*
Swap A2D2 with A2E2, and
A2H2 with A2J2 (see CTL-I 852).

Note 3: *When replacing A2D2 or A2E2, check the addressing jumpers. See INST 6.*

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STRING SWITCH FAILURE ANALYSIS

Error Code	Error Description	Suspected Logic Lines	Possible Causes				Comments	MICFL Reference
			Interface A		Interface B			
			ALD	Card	ALD	Card		
B609	Tag '06' Bus '00' is issued. Bus In Bit 3 should be on.	–Set Active	BM150	A2D2 M07	BN150	A2E2 M07	Tag '06' is not being activated with –Sel Active.	MICFL 520
B631 B632 B633	Tag '06' Bus '8x' is issued. But In Bit 0 should be off.	–Bus Out Bit 0 –Bus Out Bit 2	BP100 BP110	A2H2 D07 A2H2 M04	BQ 100 BQ110	A2J2 D07 A2J2 M04	Dev End 0 can be activated by –Bus Out Bit 0. Dev End is activated by –Bus Out Bit 2.	
B635 B636 B637	Tag '06', Bus '8x' is issued. Bus In Bit 1 should be off.	–Set PC Latch	BP110	A2H2 M02	BQ110	A2J2 M02	–Set PC Latch sets the Pack Change Latches.	
B639 B63A B63B	Tag '06', Bus '8x' is issued. Bus In Bit 2 should be off.	–Dev Asgn Bit (For drive in CE Mode.) –Bus Out Bit 1 –Dev UR Asgd Bit (For drive in CE Mode.)	BP140 BP110 BP210	A2H2 A2H2 P04 A2H2	BQ140 BQ110 BQ210	A2J2 A2J2 P04 A2J2	Check the Dev Asgn Bit for the drive in CE Mode. Bus Out Bit 1 and Tag '06' activate – Asgnment.	
B63D B63E B63F	Failed to detect Tag Valid or Normal End with Tag '06'.	–Bus Out Bit 5 –Bus Out Bit 6 –But Out Bit 7	BP100	A2H2 J12 A2H2 G13 A2H2 J13	BQ100	A2J2 J12 A2J2 G13 A2J2 J13	Bits 5, 6, and 7 can cause a Dev Addr Miscompare. Dev Addr Miscompare activates +Tag '06' Error, preventing a Tag Valid or Normal End.	
B641 B642 B643	Tag '06' is issued. Bus In Bit 3 should be on.	–Bus In Asm Bit 3	BP200	A2H2 B13	BQ200	A2J2 B13	Bus In Asm Bit 3 is always active on a Tag '06'.	
B645 B646 B647	Tag '06', Bus '00' activates the Assignment Register.	+Tag 06 Error +Error A or B	BP190 BR110	A2H2 G07 A2M2 M07	BQ190 BR110	A2J2 G07 A2M2 M08	Tag '06' Error or Error A/B prevents Tag Valid.	
B64D B64E B64F	Tag '06', Bus '40' resets the Assignment Register.	+Tag 06 Error +Error A or B	BP190 BR110	A2H2 G07 A2M2 M07	BQ190 BR110	A2J2 G07 A2M2 M08	Tag '06' Error or Error A/B prevents Tag Valid.	
B65D B65E B65F	Failed to receive Tag Valid from a Tag '06' with partial selection.	+Nonselecting Valid Tag	BR150	A2M2 M10	BR160	A2M2 M13	+Nonselecting Tag Valid activates Tag Valid.	
B675 B676 B677	See Error Code B645.							
B679 B67A B67B	The Primed Interrupt Register fails to turn on.	–Bus Out Bit 2	BP110	A2H2 M04	BQ110	A2J2 M04	Tag '06' and Bus Out Bit 2 activate Dev End. Dev End gates the Primed Interrupt Registers.	
B683	Primed Interrupt indication during a Poll.		BM140	A2D2 S02	BN140	A2E2 S02	Tag '02' and any Attention can indicate an interrupt.	

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STRING SWITCH FAILURE ANALYSIS

Error Code	Error Description	Suspected Logic Lines	Possible Causes				Comments	MICFL Reference
			Interface A		Interface B			
			ALD	Card	ALD	Card		
B685 B686 B687	Failed to receive an expected interrupt.	–Allow Poll –Tag '82'	BR110 BM150	A2M2 D10 A2D2 G02	BR110 BN150	A2M2 D13 A2E2 G02	Allow Poll senses the Dev Attn Bus. –Tag '82' and not Bus Out Bit 3 or 5 activates –SY. –SY gates the Dev Attn Bus to Contr Bus In.	
B689 B68A B68B	Failed to receive an expected interrupt on a Tag '01' with the Unsuppressible Register set.	–Tag '01'	BP150	A2H2 J10	BQ150	A2J2 J10	–Tag '01' gates the Unsuppressible Registers.	
B68D B68E B68F	Received an interrupt on a Tag '01' with the Unsuppressible Register reset.	–Unsup Attn Bits	BP150	A2H2	BQ150	A2J2	Unsuppressible Register does not reset.	
B6A1 B6A2 B6A3	Pack Change Register failed to set.	–Tag '06' –Bus Out Bit 3 –Bus Out Bit 5 –Bus Out Bit 6 –Bus Out Bit 7 –Set PC Latch	BP110	A2H2 M10 A2H2 S10 A2H2 P09 A2H2 P06 A2H2 P07 A2H2 M02	BQ110	A2J2 M10 A2J2 S10 A2J2 P09 A2J2 P06 A2J2 P07 A2J2 M02	Bus Out Bit 5, 6, and 7 and Tag '06' activate the other Device Address Decoder. Bus Out Bit 3 and Tag '06' activate Set PC Latch –Set PC Latch and –Other Dev Addr Bit set Pack Change Latch.	MICFL 520
B6A5 B6A6 B6A7	Failed to receive a Pack Change Interrupt.	–Pack Chg Bits	BP130	A2H2	BQ130	A2J2	A Pack Change Interrupt sets a Dev Attn Bus Bit that is gated to the Bus In Asm.	
B6BD B6BE B6BF	Primed Interrupt and Assignment Registers are set erroneously.	–Asgnment	BP140	A2H2	BQ140	A2J2	Asgnment gates the Assignment Registers.	
B6C1 B6C2 B6C3	Primed Interrupt is received from one or more register positions that are not set.	–Dev End Bits	BP120	A2H2	BQ120	A2J2	Dev End Bits activate Dev Attn Bits.	

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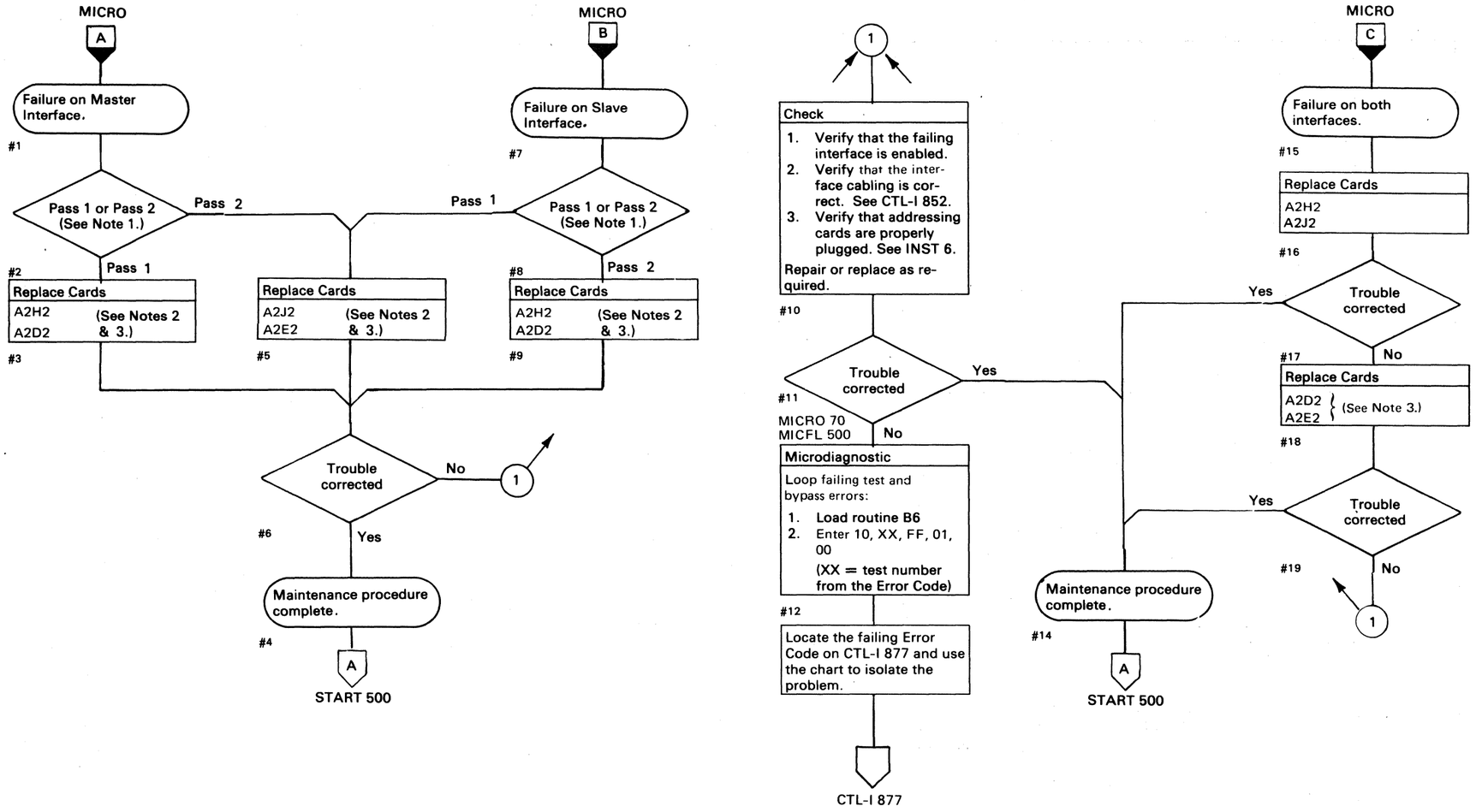
INTERFACE FAILURE (With String Switch)



Note 1: *See routine B6 operating procedures on MICFL 520.*
Pass 1:
Master = Interface A
Slave = Interface B
Pass 2:
Master = Interface B
Slave = Interface A

Note 2: *For isolation purposes, Interface A cards may be swapped with Interface B cards.*
Swap A2D2 with A2E2, and
A2H2 with A2J2 (see CTL-I 852)

Note 3: *When replacing A2D2 or A2E2, check the addressing jumpers. See INST 6.*

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STRING SWITCH FAILURE ANALYSIS

Error Code	Error Description	Suspected Logic Lines	Possible Causes				Comments	MICFL Reference
			Interface A		Interface B			
			ALD	Card	ALD	Card		
B649 **B64A** **B64B**	One or more positions of the Assignment Register failed to come on.	–Dev Asgn Bits –Enable Latch –Bus Out Bit 1 –Dev UR Asgn Bits	BP140 BP100 BP110 BP210	A2H2 A2H2 D09 A2H2 P04 A2H2	BQ140 BQ100 BQ110 BQ210	A2J2 A2J2 D09 A2J2 P04 A2J2	Check the Dev Asgn Bit Latch for proper operation. –Enable Latch becomes –Enable Pwr. –Enable Pwr allows the Dev Asgn Bit to become active. –Bus Out Bit 1 and Tag '06' activate –Asgnment. –Asgnment gates the decoder for the Dev Asgn Bits.	
B651 **B652** **B653**	One or more positions of the Assignment Register failed to reset.	–Dev Asgn Bits –Dev UR Asgn Bits	BP140 BP210	A2H2 A2H2	BQ140 BQ210	A2J2 A2J2	Check the Polarity Holds to verify that they are resetting.	MICFL 520
B655 **B656** **B657**	Bus In Bit 4 is active with the Assignment Register reset.	+Adrsd Dev A Asgd B +Adrsd Dev B Asgd A	BP180	A2H2 U13	BQ180	A2J2 U13	+Adrsd Dev Asgd active causes Bit 4 to become active.	
B661 **B662** **B663**	Bus In Bit 4 is not active with Device Assignment.	+Adrsd Dev A Asgd B +Adrsd Dev B Asgd A –Dev Asgd Bits	BP180 BP140	A2H2 U13 A2H2	BQ180 BQ140	A2J2 U13 A2J2	+Adrsd Dev Asgd active causes Bit 4 to become active.	
B67D **B67E** **B67F**	One or more positions of the Primed Interrupt Register failed to reset.	–Dev End Bits	BP120	A2H2	BQ120	A2J2	Check the Dev End Polarity Holds to be sure they reset.	
B6C9 **B6CA** **B6CB**	Received an Assignment To indication from registers that should be inactive.	–Dev Asgn Bits	BP140	A2H2	BQ140	A2J2	Check the Dev Asgn Polarity Holds to be sure they reset.	
B6CD **B6CE** **B6CF**	See Error Code B655.							

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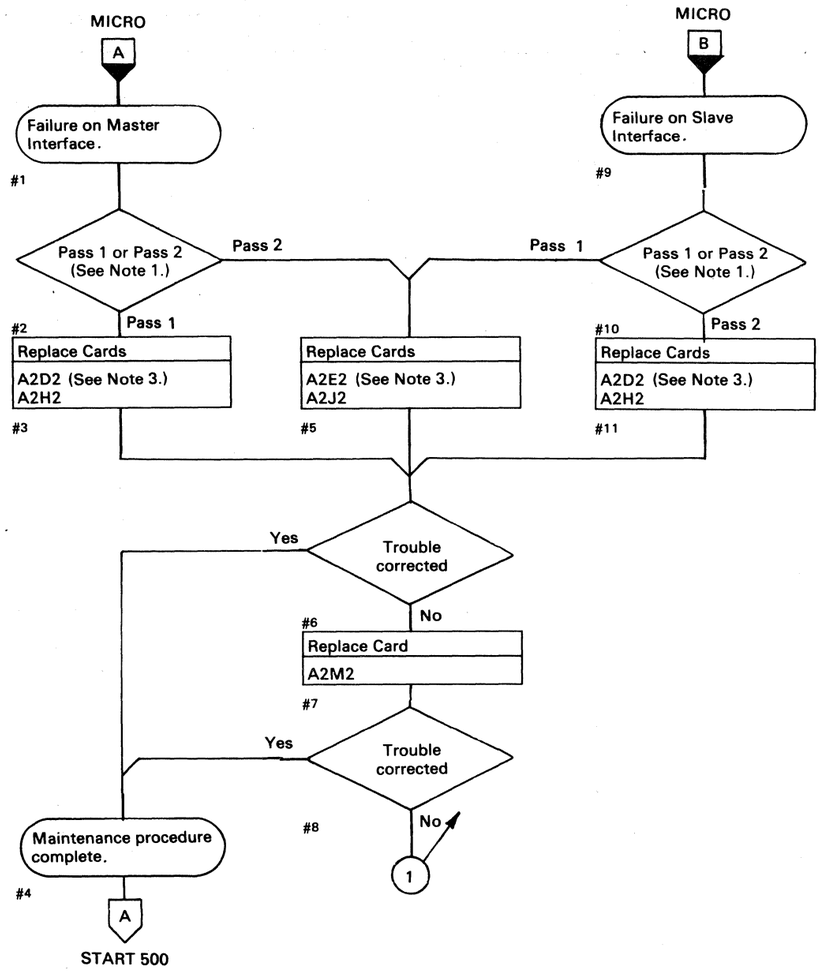
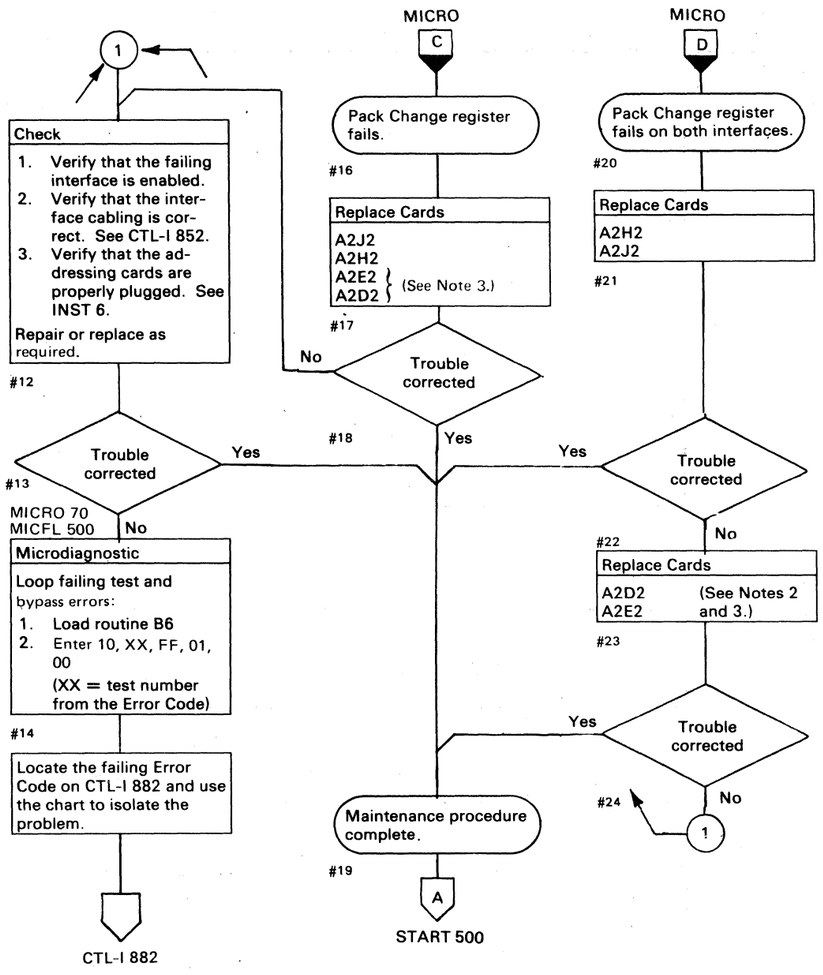
INTERFACE FAILURE (With String Switch)





Note 1: *See routine B6 operating procedures on MICFL 520.*
Pass 1:
Master = Interface A
Slave = Interface B
Pass 2:
Master = Interface B
Slave = Interface A

Note 2: *For isolation purposes, Interface A cards may be swapped with Interface B cards.*
Swap A2D2 with A2E2 and
A2H2 with A2J2 (see CTL-I 852)

Note 3: *When replacing A2D2 or A2E2, check the addressing jumpers. See INST 6.*

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STRING SWITCH FAILURE ANALYSIS

Error Code	Error Description	Suspected Logic Lines	Possible Causes				Comments	MICFL Reference
			Interface A		Interface B			
			ALD	Card	ALD	Card		
B659 B65A B65B	Failed to receive a Partial Selection indication when trying to select a drive that is already assigned.	–Adrsd Dev A Asgd B –Adrsd Dev B Asgd A –Gate Adrsd Dev A Asgd 01 –Gate Adrsd Dev B Asgd 01 –Connect A –Connect B	BP180 BP180 BR140	A2H2 U13 A2H2 S12 A2M2 G09	BQ180 BQ180 BR140	A2J2 U13 A2J2 S12 A2M2 G05	–Gate Adrsd Dev A/B Asgd 01 activates +Adrsd Dev Asgd if a Dev Asgn Bit is active. +Adrsd Dev Asgd and –Connect allow Partial Selection to become active.	MICFL 520
B681 B682	An interrupt is received from a drive assigned to the other interface while Polling devices.	Dev Attn Bus Bits	BP160	A2H2	BQ160	A2J2	Check the Dev Attn Bus Latches to the sure they are resetting.	
B6A9 B6AA B6AB	Pack Change Register fails to reset.	–Pack Chg Bits	BP130	A2H2	BQ130	A2J2	Check the Pack Chg Bit Latches to be sure they are resetting.	
B6AD B6AE B6AF	Received an unexpected Pack Change Interrupt during a Poll.							
B6C5 B6C6 B6C7	Received a Pack Change Interrupt from a register that should be off.							

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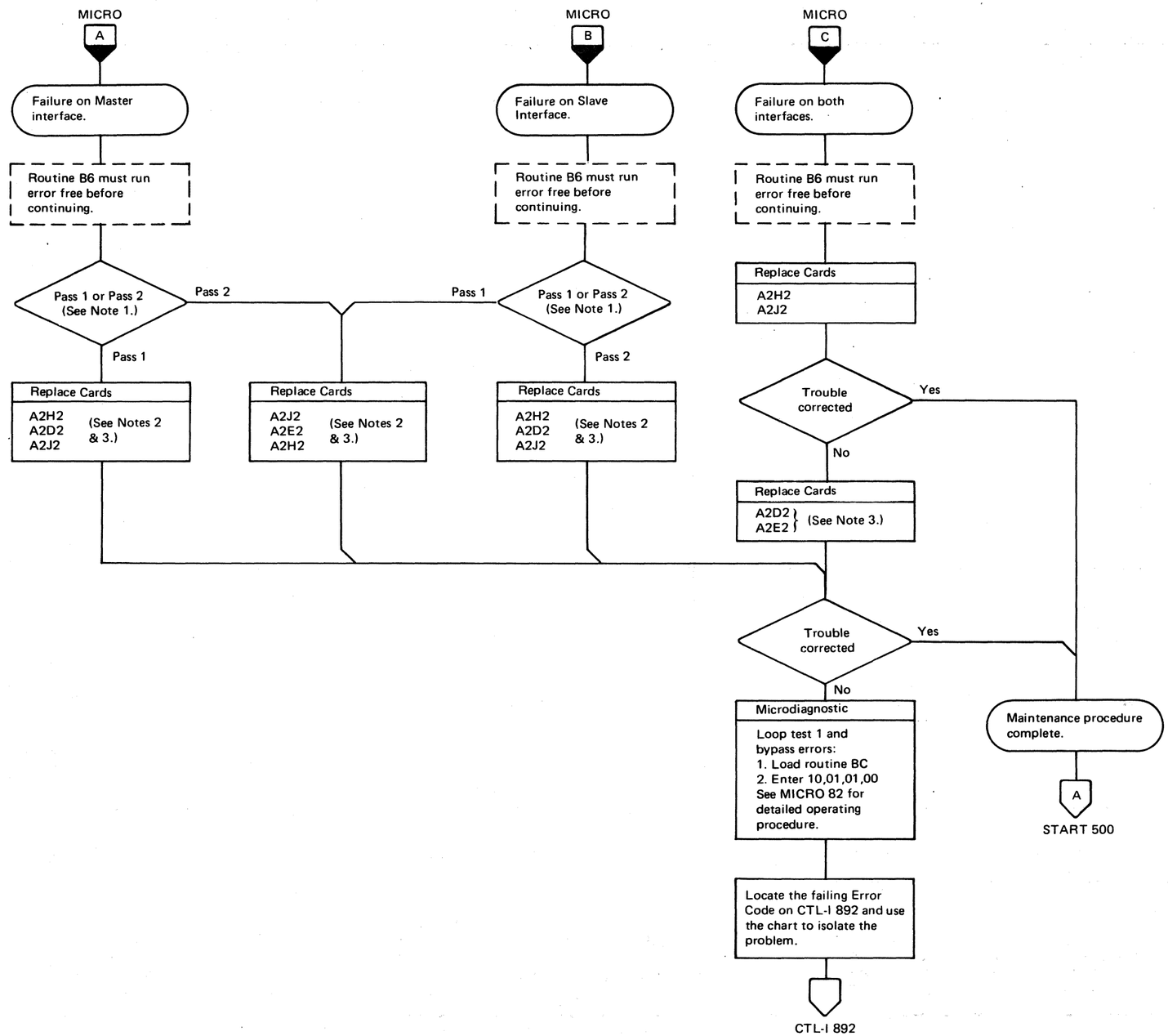
INTERFACE FAILURE (With String Switch)



Note 1: *See routine BC operating procedures on MICRO 82.*

Pass 1:
Master = Interface A
Slave = Interface B
Pass 2:
Master = Interface B
Slave = Interface A

Note 2: *For isolation purposes, Interface A cards may be swapped with Interface B cards.*
Swap A2D2 with A2E2, and
A2H2 with A2J2 (see CTL-I 852).

Note 3: *When replacing A2D2 or A2E2, check the addressing jumpers. See INST 6.*

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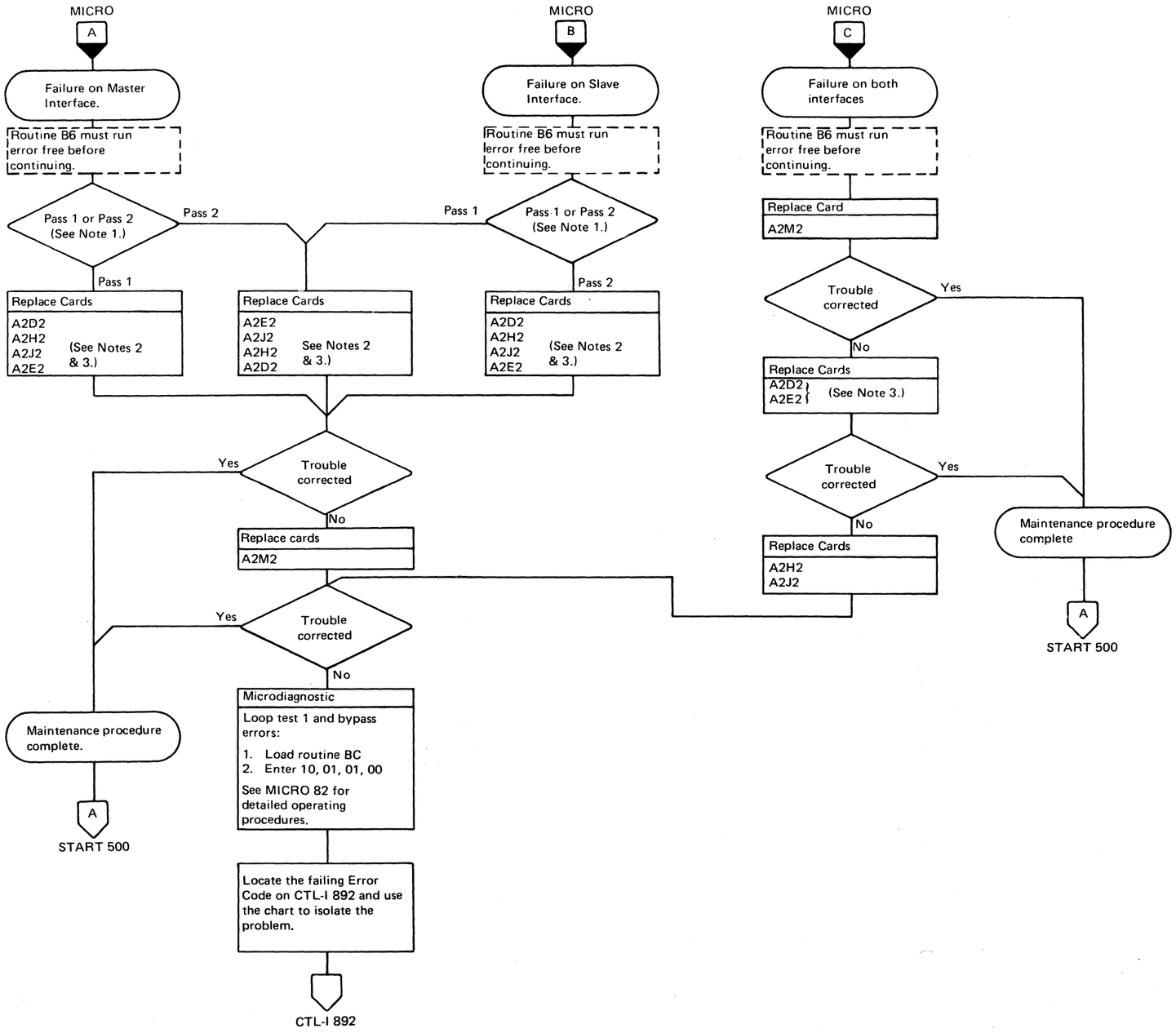
INTERFACE FAILURE (With String Switch)



Note 1: *See routine BC operating procedures on MICRO 82.*

Pass 1:
Master = Interface A
Slave = Interface B
Pass 2:
Master = Interface B
Slave = Interface A

Note 2: *For isolation purposes, Interface A cards may be swapped with Interface B cards.*
Swap A2D2 with A2E2, and
A2H2 with A2J2 (see CTL-I 852).

Note 3: *When replacing A2D2 or A2E2, check the addressing jumpers. See INST 6.*

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INTERFACE FAILURE (With String Switch)

ALTERNATE PATH RECOVERY

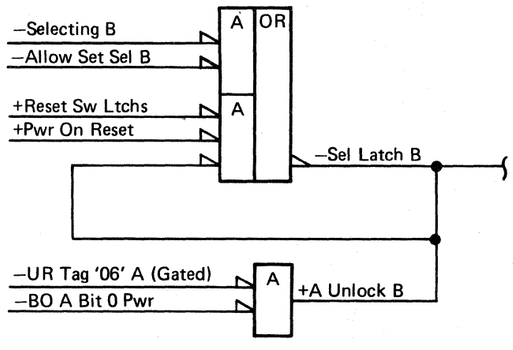
This function uses an Unconditional Reserve (UR) command to break device allocation to the primary path, that has become inoperative, and establishes an alternate path within the system.

Unconditional Reserve

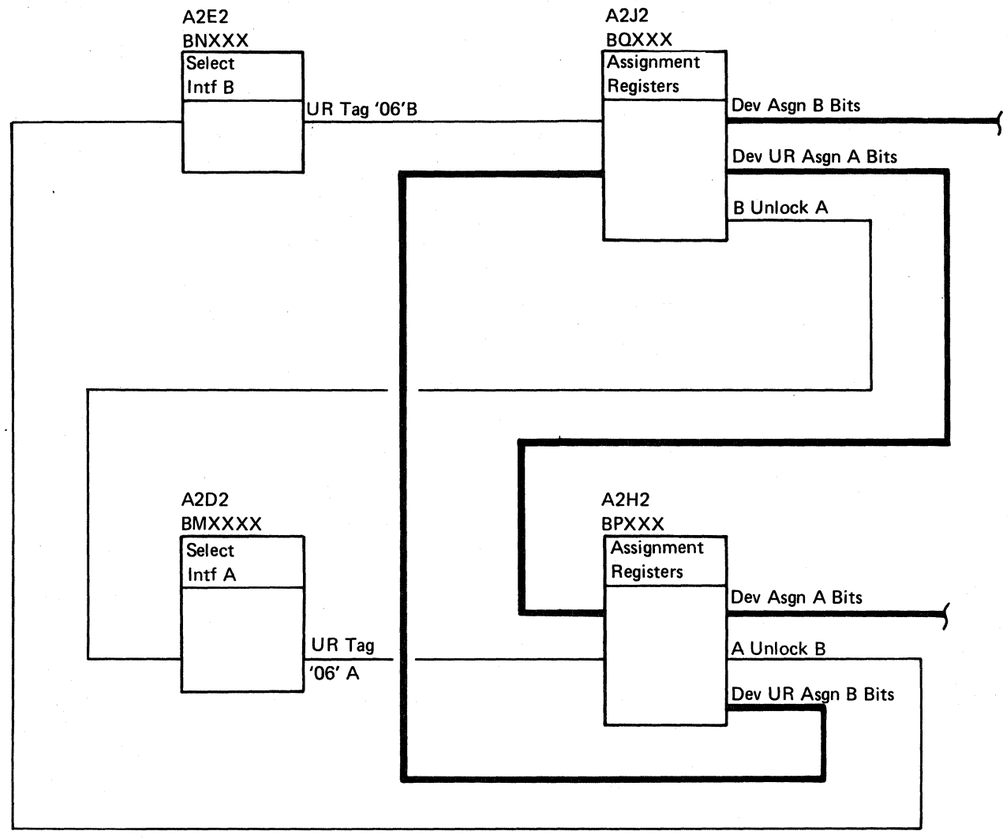
When a 3350 string with string switch feature is attached to a storage control that stops operating while an interface is selected or an Assignment Register position is set, no operation is possible from another storage control to the affected string or drive. To eliminate this condition, the Select latch and Assignment Register positions can be reset by the UR (Unconditional Reserve) command using a circuit similar to Figure 1. For example, the Select latch for Interface B is latched On and prevents Interface A from operating. Interface A may activate A Unlock B using Tag '06' Bus '88'. This forces –Sel Ltch B to a plus level breaking the latch back. Similarly, the Assignment Register positions may be reset using the Dev UR Asgn A (or B) bits to break the Assignment Register latch back on the opposite interface. Once the interface Select latch and/or the Assignment Register positions have been reset, the string is reserved for the storage control through which the UR command was issued and normal operation may continue on the functional interface.

See CTL-I 852 for String Switch Overview diagram.

Figure 1. Select Latch



Device Assignment/Select Latch



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UNCONDITIONAL RESERVE FAILURE ANALYSIS

Error Code	Error Description	Suspected Logic Lines	Possible Causes				Comments	MICFL Reference
			Interface A		Interface B			
			ALD	Card	ALD	Card		
BC11 BC12 BC13	Tag '06' Bus '08'; reset to the Assignment Register bit on the opposite interface failed.	Device UR Asgn Bits	BP210	A2H2	BQ210	A2J2	The operation attempts to reset the Assignment Register latch in the opposite interface by forcing the latch back to a plus level.	MICFL 770
BC15 BC16 BC17	Tag '06' Bus '88' failed to reset the Select latch on the opposite interface.	A Unlock B B Unlock A	BP210	A2H2 A2D2	BQ210	A2J2 A2E2	The operation attempts to reset the Tag Select latch on the opposite interface by forcing the latch back to a plus level.	
BC19 BC1A BC1B	Full selection failed in an attempt to force the string switch to neutral.	A Unlock B B Unlock A	BP210	A2H2 A2D2	BQ210	A2J2 A2E2	Select latch failed.	
BC1D BC1E BC1F	No Normal End on select tag.	–Selecting	BM150	A2D2	BN150	A2E2	This error is primarily intended to prevent a hang condition and is not an expected error for this test.	
BC20	Failed to detect a Partial Select with long connection set.	+ Non Selecting Tag Valid –Tag '01' –Busy	BM150 BM150 BR150	A2D2 J10 A2D2 J06 A2M2 P10	BN150 BN150 BR160	A2E2 J10 A2E2 J06 A2M2 M03	Non Selecting Tag Valid and Partial Select Latch active gate B1. Gate B1 gates the Bus In bits. If Non Selecting Tag Valid is always active, the bits are not gated to Bus In. Tag '01' active causes a Check 1 of 6, preventing a Normal End or Tag Valid. –Busy becomes BI bit 3, which should be active, indicating Partial Select.	

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TROUBLE NOT FOUND

This page contains aids for problem resolution where insufficient error information is available to follow the maintenance analysis procedure. It may also be used as an aid in analyzing intermittent errors.

VOLTAGE CHECKS

Check for unstable voltage (−4 Vdc, +6 Vdc) on drive or controller board. Voltages can be monitored while looping a failing microdiagnostic or while machine is running online. See PWR 90 (controller) or PWR 290 (drive) for procedure and tolerances.

VISUAL CHECKS

Connectors

Check for bent or damaged pins, foreign objects between pins, and proper seating.

Back Panel Wiring

Check for a tight wire wrap cutting into a pin on the back panel. Check for a cracked land pattern on a board or card.

EC INSTALLATION

If an enginerring change has been recently installed, check the EC installation instructions and determine where the change was made. Inspect the back panel for tight wire wraps.

REFERENCES

Microdiagnostic Routine A1 Summary

Test 1

- Checks for always active lines between controller and storage control.

  See OPER 11 and 13 41 .

Test 2

- Verifies that the controller can be selected (Tag '03').

  See OPER 11 and 12 30 35 .

- Resets controller circuits (Tag '09') and verifies that the following lines are active:

  Tag Valid, Normal End, Check End } See OPER 11 and 13 39 .

  Select Active — See OPER 11 and 13 35 .

  Sync In — See OPER 8 and 9 20 .

Test 3

- Verifies the set and reset of the following latches:

  Tag Bus Parity Check, Bus Out Parity Check } See OPER 5 and 6 9 6 .

  Controller Check, Error Alert } See OPER 241 17 .

Test 4

- Verifies that Tag Valid and Normal End are returned for all controller tags.

  See OPER 11 and 13 39 .

Test 5

- Checks the set and reset of controller Bus In Parity Check.

  See OPER 11 and 13 42 .

- Checks the Bus In Registers for proper operation.

  See OPER 8,9,11, and 13 18 21 40 .

- Checks for always active bits on Device Bus In

  See OPER 11 and 13 38 .

- Checks for proper operation of the reset lines.

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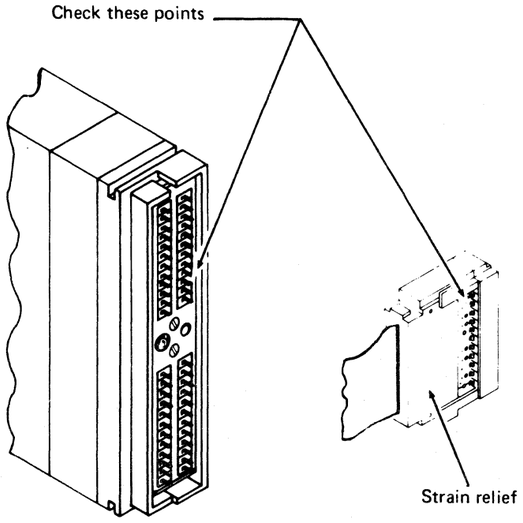
CABLE CHECKING HINTS

The following items should be considered when checking cables.

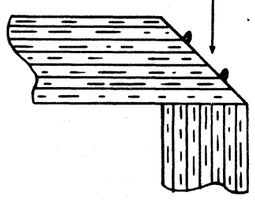
Note: *Interface cables must always be connected light (gray) to dark (black). Light to light or dark to dark is wrong (see INST 10).*

POSSIBLE CAUSES

- Inspect contacts; they may be bent, broken, or pushed in.



- Inspect for broken wires at crimps and around strain reliefs.
- Inspect SLT paddle cards for cold solder connections, solder splashes, or open land patterns.
- Inspect flat cables at bends for wires breaking through insulation caused by straightening bent cables.



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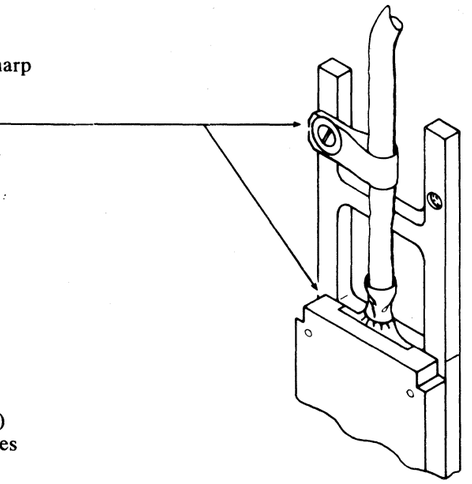
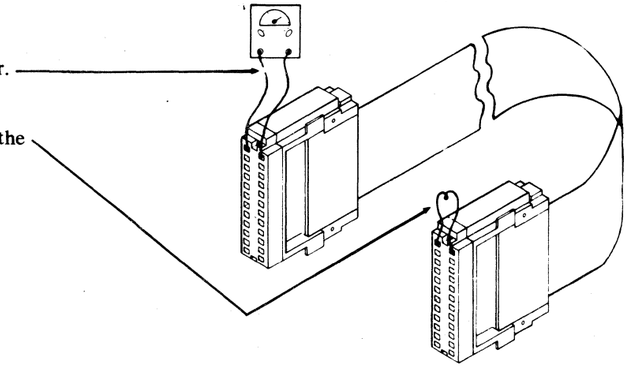
- Inspect wire for evidence of arcing or burning, especially paddle cards that carry high current.
- Inspect cables and wires for chafing at rough or sharp pivot points.
- Inspect for interference of strain relief hardware.
- Check that connectors are properly seated and/or mated.
- Where specific lines are suspected or indicated by analysis procedures, use a CE meter to check for:

  Open
  Short to ground
  Short to adjacent signal line



POSSIBLE ACTION

1. Swap both ends of identical cables (check P/Ns) for isolation (for example, control interface cables or device interface cables).
2. Use card extenders to swap wires within a cable for isolation or a temporary fix.

Continuity Checks for Long Cables

1. Connect a CE meter to two pins in the connector.
2. Verify that you have an open circuit.
3. Short the corresponding pins in the other end of the cable.
4. Verify that you now have a short circuit.