IBM Maintenance Library

Logic Blocks
Automated Logic Diagrams
SLT, SLD, ASLT, MST

SY22-2798-2

Preface

This manual describes typical component circuits and logical functions, standard logic blocks, Automated Logic Diagrams (ALD's), and Field Engineering ALD's for the following technologies:

Solid Logic Technology (SLT)
Solid Logic Dense (SLD)
Advanced Solid Logic Technology (ASLT)
Monolithic System Technology (MST)

Major aims of this manual are to explain how to interpret analog and digital logic blocks, and to explain how to read an FEALD.

Related Maintenance Library and Field Engineering Theory of Operation manuals are:

Solid Logic Technology–Packaging, Tools, Wiring Change Procedure, TO, SY22-2800

Advanced Solid Logic Technology (ASLT); Monolithic System Technology x (MST x)–Packaging, Tools, Wiring Change Procedure, Field Engineering Theory of Operation, SY22-6620

Monolithic System Technology–Packaging, Tools, Wiring Change Procedure, TO, SY22-6739

Sixth Edition (October 1971)
This is a major revision of, and obsoletes SY22-2798-1. Information has been added on analog logic blocks and integrated circuits. Minor changes have been made to the sections on ALD's and FEALD's. Changes or additions to the text and illustrations are indicated by a vertical line to the left of the change.

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Illustrations

Chapter 3. Automated Logic Diagrams (ALD's)

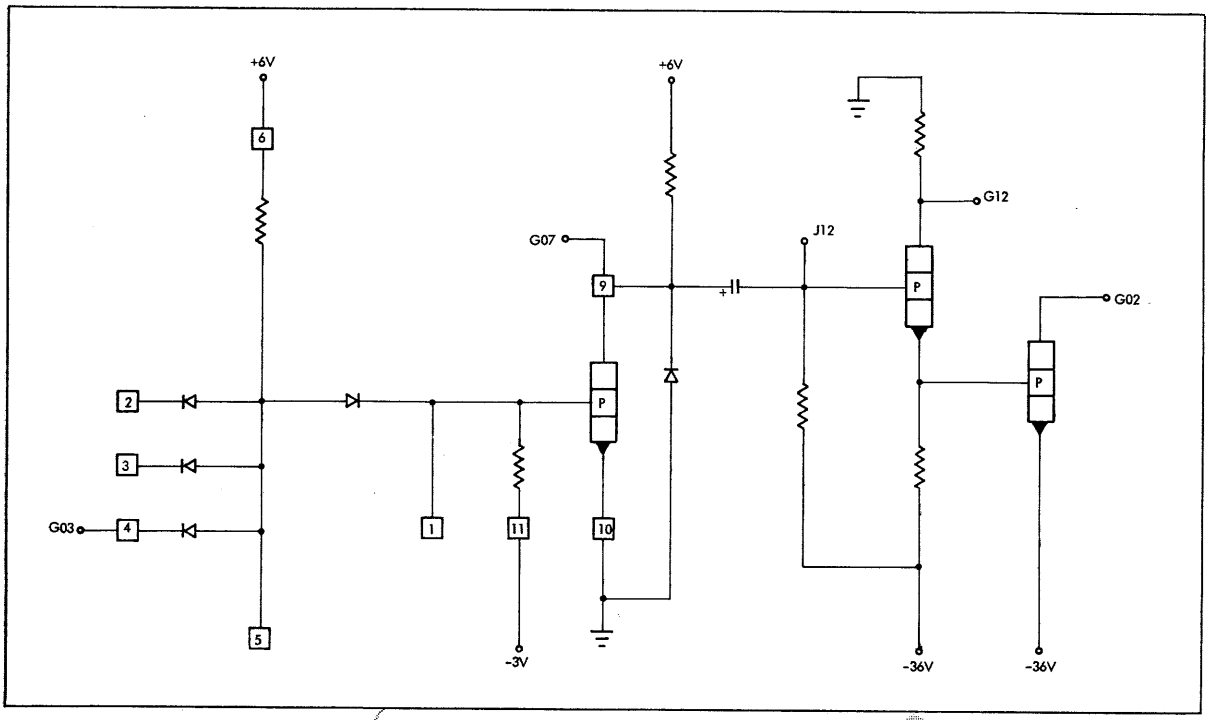
Chapter 4. Card Layout

Chapter 5. Field Engineering ALD's

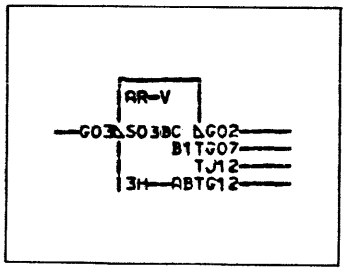
Abbreviations

A	AND
A	AND circuit
A-2, A-3	threshold
AI	AND inverter
AIT	AND-inverter-terminate
ALD	automated logic diagram
AMH	amplitude hold
ANO	analog-OR
AOI	AND-OR-inverter
AOPI	AND-OR-power-inverter
AOPX	AND-OR-power-extender
AOX	AND-OR-extender
API	AND-power-inverter
AR	amplifier
ASLT	Advanced Solid Logic Technology
C	capacitor
CABL	cable
CD	controlled data
CD	core driver
chan	channel
clk	clock
comp	comparator
CR	diode
CS	current switch
CT	contact
ctrl	control
CV	converter
D	driver
DA	design automation
DCD	decoder
DCI	direct-coupled inverter
DET	detector
DF	differential amplifier
DIF	differentiator
DL	delay line
DLD	delay line driver
DLY	delay
EC	engineering change
ENGALD	engineering ALD
ENTR	entry from machine type
EV	even count
EXIT	exit to machine type
FEALD	Field Engineering ALD
FET	field-effect transistor
FF	flip-flop
FFL	flip-flop latch
FG	function generator
FL	flip-flop latch or flip latch
FLTR	filter
GND	ground
H	hold coil
HD	magnetic head driver
HP	high power
HPD	high-power driver
HS	high speed
I	inverter
ID	indicator driver
IDL	indicator driver lamp
II	isolating inverter
IND	indicator
INT	integrator
I/O	input/output
JMPR	jumper
L	inductor
LD	(transmission) line driver
LIM	limiter
LMT	logic master tape
LS	low speed
LSA	line sensing amplifier
LTN	line terminating network
mach	machine
MD	magnet driver
MFI	machine features index
mHz	megahertz
MIX	mixer
mpx	multiplex
MS	medium speed
MST	Monolithic System Technology
mV	millivolt
N	inverter
NC	normally closed
NL	no load
NO	normally open
ns	nanosecond
OD	odd count
OE	exclusive OR
OI	OR inverter
OIT	OR-inverter-terminate
OR	OR circuit
OSC	oscillator
P	pick coil
PB	pushbutton
pF	picofarad
PH	polarity hold
PMT	physical master tape
PT	relay point
PWR	power

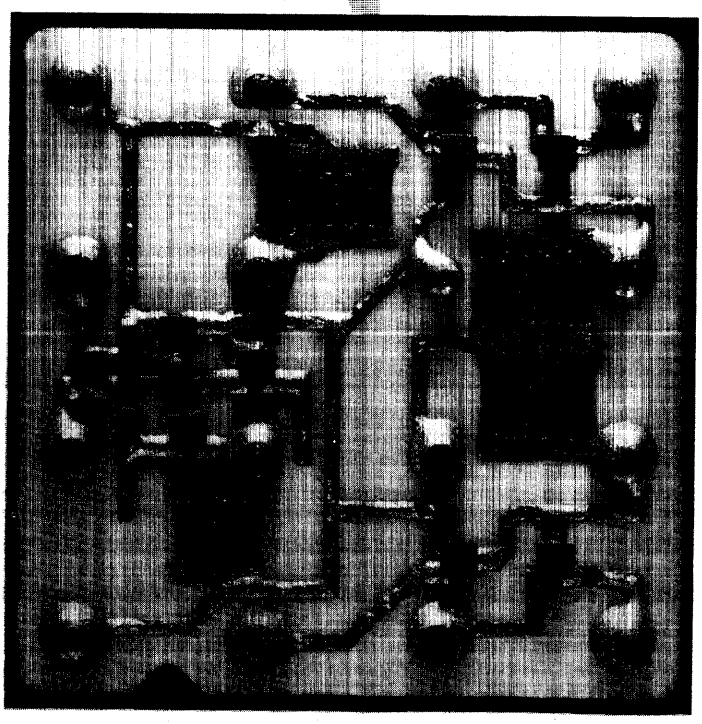
Q	transistor
R	resistor
RC	resistor-capacitor
rcvr	receiver
rd	read
RECT	rectifier
reg	register
rly	relay
RW	read/write
RY	relay
sel	select
SEL	selector
ser	serial
SERV	service voltage
SLD	Solid Logic Dense
SLT	Solid Logic Technology
SPD	sample pulse driver
SPEC	special
SRV	service
SS	singleshot
ST	Schmitt trigger
SW	switch
T	terminate, transformer
TD	time delay
tgr	trigger
THRM	thermal switch
TLD	transmission line driver
TLD	transmission line receiver
TLT	transmission line terminator
TTL	transistor-transistor logic
Tx	transistor
uF	microfarad
uH	microhenry
V	voltage amplifier, volts
var	variable
WL	wired logic
XOI	exclusive-OR-inverter
XOR	exclusive OR
XORL	exclusive OR latch
XOVR	crossover
xtl	crystal
Z	impedance



Schematic Equivalent of S03BC Module



ALD Logic Block
Equivalent of Schematic



Module S03BC

- The current technologies are: SLT, SLD, ASLT, and MST.
- Each technology has its own basic logic circuits.
- Logical functions are represented by standard logic blocks on Automated Logic Diagrams (ALD's).
- An ALD is a simplified schematic diagram of an electronic machine or system.
- Representative logic circuits are: AND circuit, OR circuit, inverter, flip-flop, polarity hold, singleshot, and oscillator.

The principal objective of this manual is to explain the several forms of Automated Logic Diagrams (ALD's) for machines of the System/360 and System/370 eras. The order of treatment is:

1. Component circuits – basic electronic circuits, their relation to logical functions in computers, and the circuit technologies used to implement them.
2. Logic blocks – standard digital and analog logical functions appearing in all forms of ALD's.
3. Automated Logic Diagrams – types of information, other than logical functions, appearing in each type of ALD.

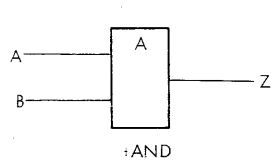
This chapter presents the building blocks of current systems: the transistor or circuit chip, module, card, board, gate, and frame. This chapter deals with component circuits. Because three basic circuits – diode AND, diode OR, and the inverter – perform many logical functions in systems, these circuits are used to illustrate computer logic. Other representative circuits, such as the flip-flop and singleshot, are explained with respect to logical function, circuit operation, input and output, and technology. The latter part of Chapter 1 is devoted to current technologies, and their impact on component circuits in relation to operating speeds, input and output voltages, transition times, and terminology. Chapter 2 defines and explains ALD logic blocks, without regard to technology or type of ALD. Succeeding chapters describe the several types of ALD's, with emphasis on reading an FEALD.

BASIC COMPONENT CIRCUITS

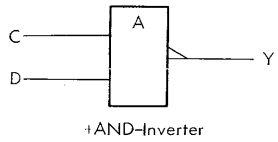
Computer functions are represented by logic blocks on an ALD, or FEALD. For example, an AND function is represented by a rectangular block containing an A. This block, in turn, is a symbol for a more complicated schematic circuit (see Frontispiece). The following sections describe representative component circuits, from simple to complex, and their relation to logical functions and logic blocks.

AND Circuit

The output of an AND circuit (Figure 1-1) is at its indicated polarity only when all of its inputs are at their indicated polarities. Polarity is indicated by a wedge (◺), or absence of one, at the input or output of a logic block. Figure 1-1 is an ALD representation of an AND block and a truth table for an AND function. Figure 1-2 is a corresponding circuit schematic and timing chart for an AND block.



Z	AB	
A	B	Z
1	1	1
1	0	0
0	1	0
0	0	0



Y	CD	
C	D	Y
1	1	0
1	0	1
0	1	1
0	0	1

Figure 1-1. AND Functions

The meaning of the AND block in Figure 1-1 is: if input A and input B are both at their more positive potential, then output Z will be at its more positive potential. Positive, as used here, does not necessarily mean a positive voltage, but merely the more positive of two states that an input or output to a logic block can have. A truth table can be constructed to represent logical functions. By definition, a 1 equals the more positive potential, and a 0 equals the less positive potential. The truth table for the AND block shows that if inputs A and B are in the 1 state, output Z is also in the 1 state. If either input is in the 0 state, the output is in the 0 state.

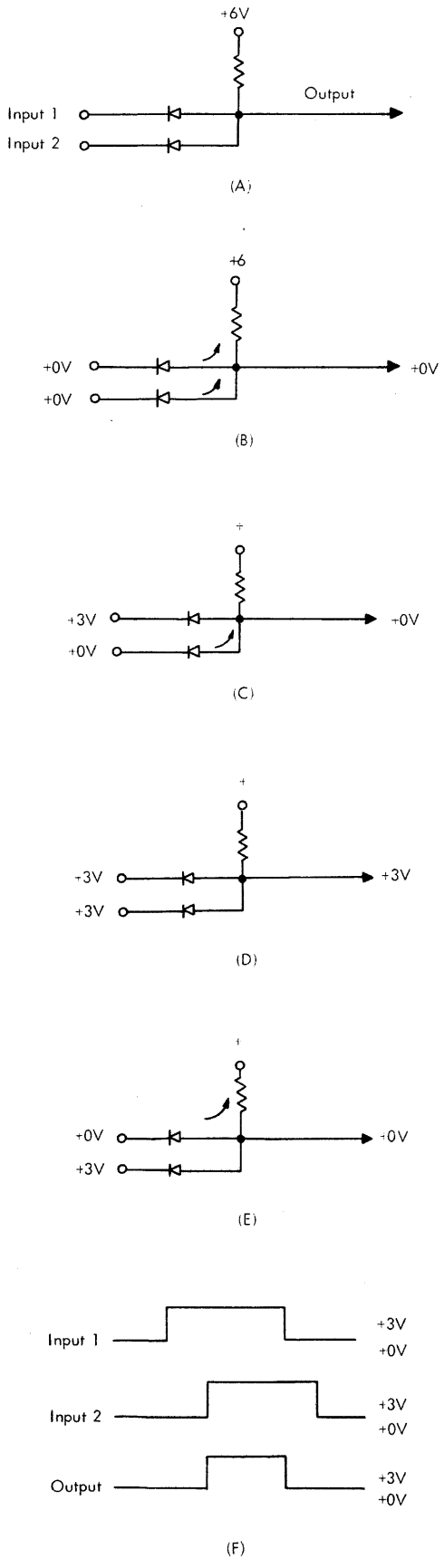


Figure 1-2. AND Circuit

The second AND block in Figure 1-1 is a positive-AND-inverter, in which inputs C and D must both be at their more positive potential (1 state) for output Y to be at its more negative potential (0 state). A wedge at the input or output of a logic block indicates a more negative potential.

Figure 1-2 is a diode AND circuit in its simplest form of only two inputs. This is a positive AND circuit, which requires both inputs to be positive before the output can be positive. In example B, both inputs are negative (0 volt), causing both diodes to conduct under forward bias. The resultant current flow through the resistor causes a voltage drop across the resistor and maintains a negative (0 volt) output. Because of the forward resistance of the diodes, the output voltage is approximately the same as the input voltage; generally, the voltage drop across a discrete, conducting diode is 0.6 volt.

If input 1 (the upper input) changes instantaneously to a positive polarity (+3 volts, example C), diode 1 cuts off because the cathode is more positive than the anode. Diode 2, with a negative voltage on its cathode, continues to conduct and the output voltage remains unchanged (negative). As input 2 also changes to positive (+3 volts, example D), diode 2 cuts off. When the output voltage reaches slightly more than +3 volts, both diodes go back into conduction and the output remains at +3 volts. Should input 1 fall to +0 volt (example E), diode 1 conducts harder and diode 2 cuts off. The output follows the input to +0 volt. If input 2 falls to +0 volt, diode 2 goes back into conduction to maintain the +0 volt output as in example B.

In summary, the output voltage of a positive AND circuit approximates the more negative input voltage, regardless of the number of inputs. The timing chart in example F shows that the output is up only if and when both inputs are up.

OR Circuit

The output of an OR circuit is at its indicated polarity when one or more of its inputs are at their indicated polarities. Figure 1-3 is an ALD representation of an OR

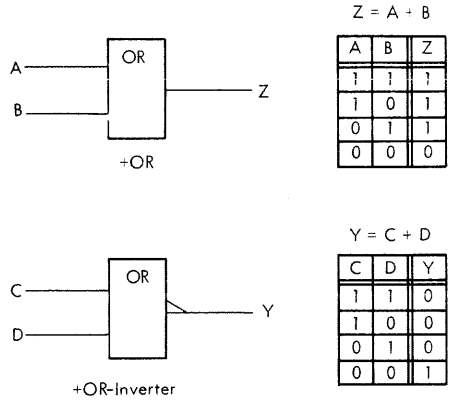


Figure 1-3. OR Functions

block and its corresponding truth table. The logical meaning of this OR block is: if input A or input B, or both, are at their more positive potential, then output Z will be at its more positive potential. The truth table gives an equivalent: if either or both inputs are in the 1 state, then the output will be in a 1 state.

The second OR block is a positive-OR-inverter, in which output Y is in its more negative state if either or both inputs are at their more positive potential.

The positive OR circuit (+OR) in Figure 1-4 has a positive output when either or both inputs are positive. If both inputs are at their more negative level (0 volt), both diodes conduct (example B) and the voltage drop across the resistor maintains the output at approximately 0 volt.

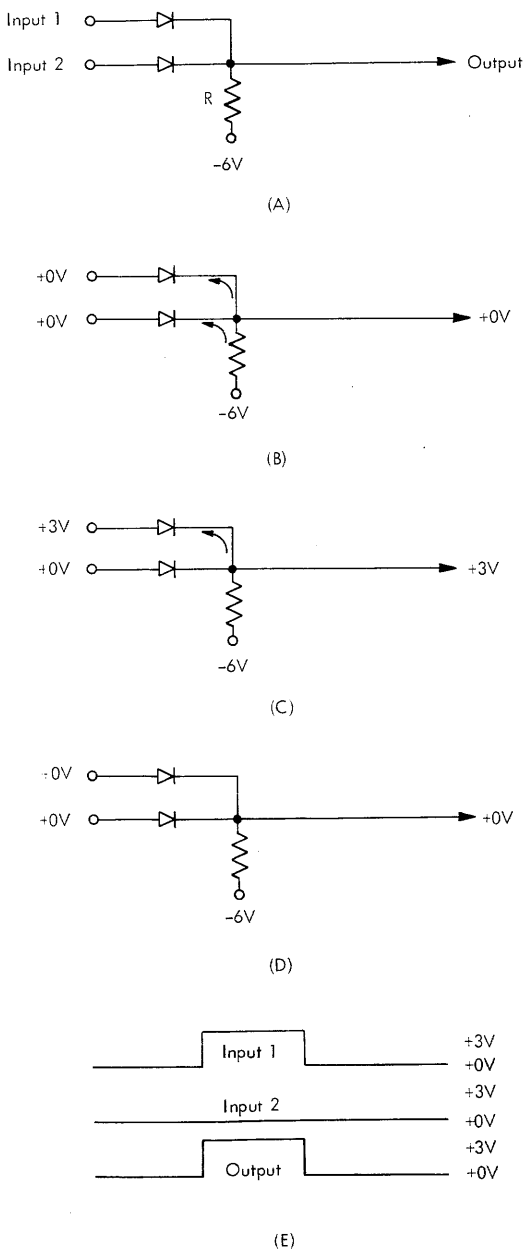


Figure 1-4. OR Circuit

If either input rises to its more positive level (example C, input 1 at +3 volts), that diode conducts more, cutting off the other diode. The output follows the more positive input voltage, +3 volts. Normally, only one input to an OR circuit is up at any given time. When the input that was up falls, its input diode cuts off (example D). This input diode conducts again when the output voltage reaches a point slightly more positive than the more negative input level.

In summary, the output voltage of a positive OR circuit approximates the more positive input voltage. The timing chart in example E shows that the output from an OR circuit rises when an input rises.

Inverter Circuit

The output of an inverter is of opposite potential to the input (Figure 1-5). Again, the wedge at the output of a block means that the output must be at its least positive potential when the function of the block is satisfied. In SLT circuits, where a transistor provides inversion, the inverter circuit uses an NPN transistor having a grounded emitter (Figure 1-6, example B).

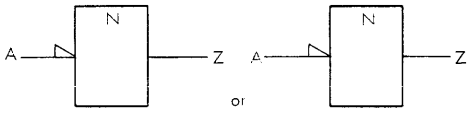


Figure 1-5. Inverter Function

Bias is the term given to the voltage that controls a transistor; bias voltage is the dc voltage difference in potential between the base and emitter. Transistor conduction, the current that flows through the collector or emitter circuit, is controlled by bias.

Consider the emitter voltage held at a constant ground level, as in example B. Conduction can be controlled by varying the base voltage above and below the emitter voltage. Conduction follows two rules:

1. An NPN transistor conducts if its base is more positive than its emitter.
2. A PNP transistor conducts if its base is more negative than its emitter.

Forward bias causes conduction; reverse bias cuts off conduction. An input voltage more than 0.3V can start a transistor into conduction; with 0.8V at its base, the transistor conducts at saturation. In the conducting state, the transistor presents a relatively small resistance to current flow. A cut-off, or nonconducting, transistor presents a large resistance to current flow through the transistor. Because current (electrons) flows from negative to positive, and from emitter to collector in an NPN transistor, the collector must be returned to a more positive voltage than its emitter. Likewise, the collector of a PNP transistor must be returned to a voltage more negative than its emitter. A conducting transistor with a grounded emitter cuts off with +0.3V at its base.

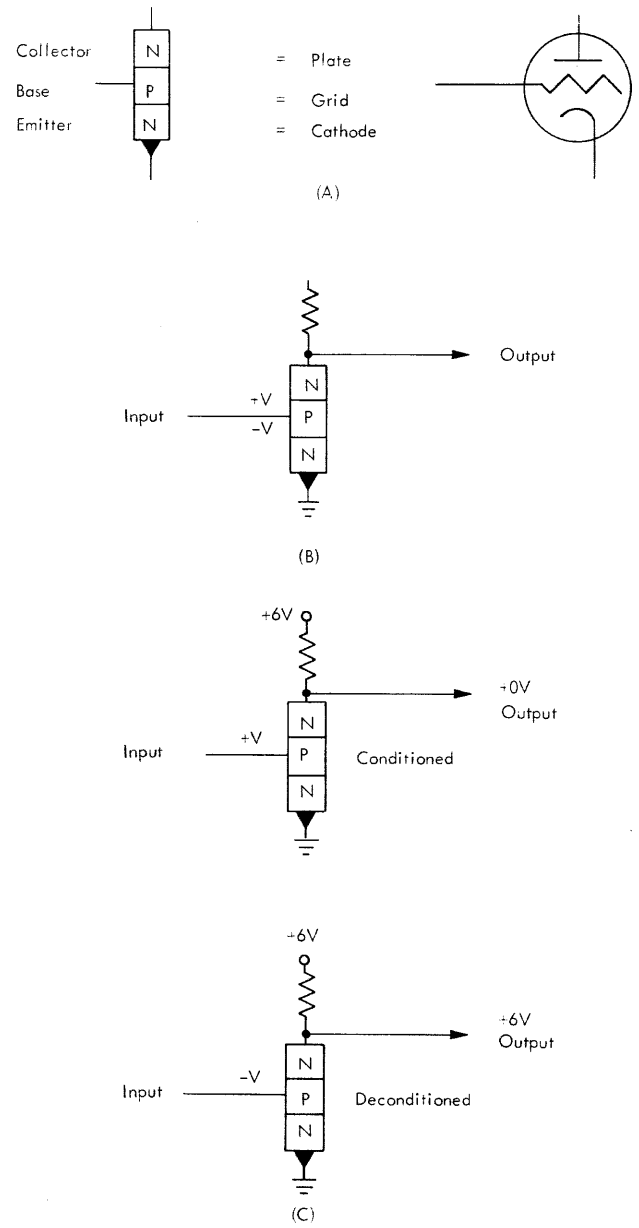


Figure 1-6. Inverter Circuit

Figure 1-6, example C, illustrates a grounded NPN inverter. A positive input voltage greater than 0.3V causes the output voltage to follow the voltage at the emitter (approximately 0.3V). A negative input voltage at the base causes the transistor to cut off and the output follows the voltage at the collector, +6 volts. Thus the function of the inverter is fullfilled: positive input produces a negative output; negative input produces a positive output.

Positive AND Equals Negative OR

A positive AND circuit may be used logically as a negative OR circuit. The truth table and timing chart in Figure 1-7 represent the positive AND circuit as previously defined.

From the rules defining an OR circuit, it can be seen that the same truth table and timing chart also apply to the negative OR circuit. For instance, if both inputs to the negative OR circuit are positive, the inputs are not satisfied, the function of the block is not satisfied, and the output is positive.

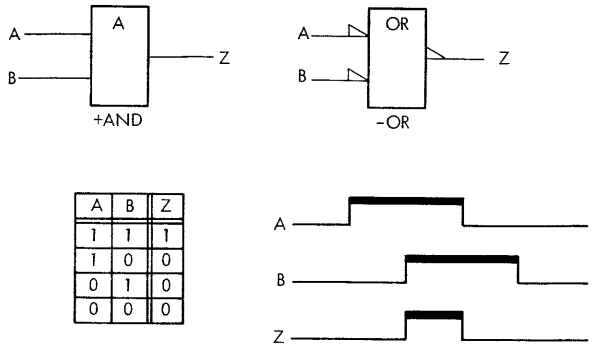


Figure 1-7. Positive AND Equals Negative OR

Figure 1-8 shows a positive-AND-inverter and its inverse function, a negative-OR-inverter. Inspection shows that the truth table applies to both blocks. Changing all inputs and outputs from plus to minus, and from minus to plus, permits conversion from positive AND (+AND) to negative OR (-OR) and vice versa.

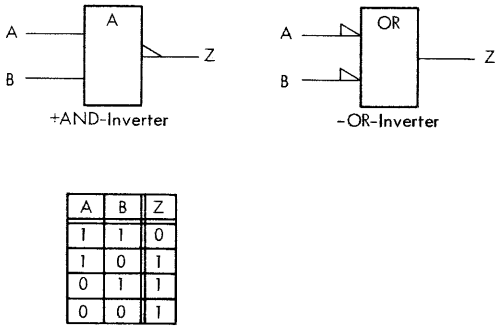


Figure 1-8. Positive AND Inverter Equals Negative OR Inverter

Extender and DOT Functions

AND circuits and OR circuits can be connected to produce a single output (Figure 1-9). In diode logic an extender (E) connects one logic block to another. The extender, in effect, is a method of adding diodes to the input of a circuit. The symbol E is seen in ALD's when the connection is between two cards. In transistor logic, the outputs of logic blocks are connected by a DOT block. Generally the AND DOT is a positive AND; the OR DOT is a negative OR.

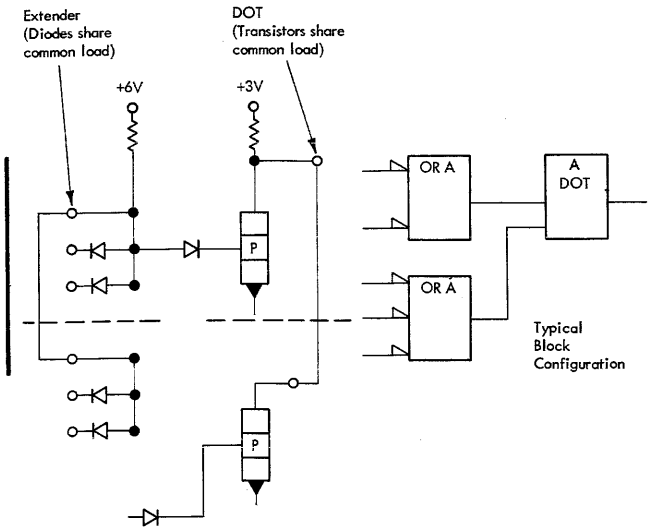


Figure 1-9. Extender and DOT Functions

Flip-Flop (FF) Circuit

A flip-flop has two stable states: a set (1) state and a reset (0) state. The flip-flop block (Figure 1-10) is put in the set state by a pulse on the set input, which produces output polarities as indicated on the block; in this case, the 1 output is positive and the 0 output is negative. The 1 and 0 outputs are always of opposite polarity. A signal of the indicated polarity at the reset input causes the outputs to assume polarities opposite to those indicated.

A signal of the indicated polarity at the complement input changes the state of the flip-flop. Simultaneous inputs of the indicated polarity at the set and reset inputs also change the state of the flip-flop (complement it).

The flip-flop schematic shows that the circuit is composed of several modules: two cross-coupled AI modules, an R-Pac, and an RC-Pac, all mounted on one card. The negative-going transition of an ac set pulse at an ac input feeds through a 175 pF capacitor to turn the ON transistor off. Current flows from the AND resistor of the ON transistor and the 30k bias resistor to the collector of the ac set driver. The OFF transistor turns on. Each side of a flip-flop has two dc set/reset inputs available, which can be driven from any low-speed logic block.

Polarity Hold Latch (PH)

The polarity hold latch has a single bi-stable output that can be changed by sequencing the control and data inputs (Figure 1-11). When the control input is at its indicated polarity, the output "follows" the data line; in the example block, the output is positive when the data input is positive. As soon as the control line goes to the opposite polarity, the output remains at whatever polarity it had at the moment the control line changed.

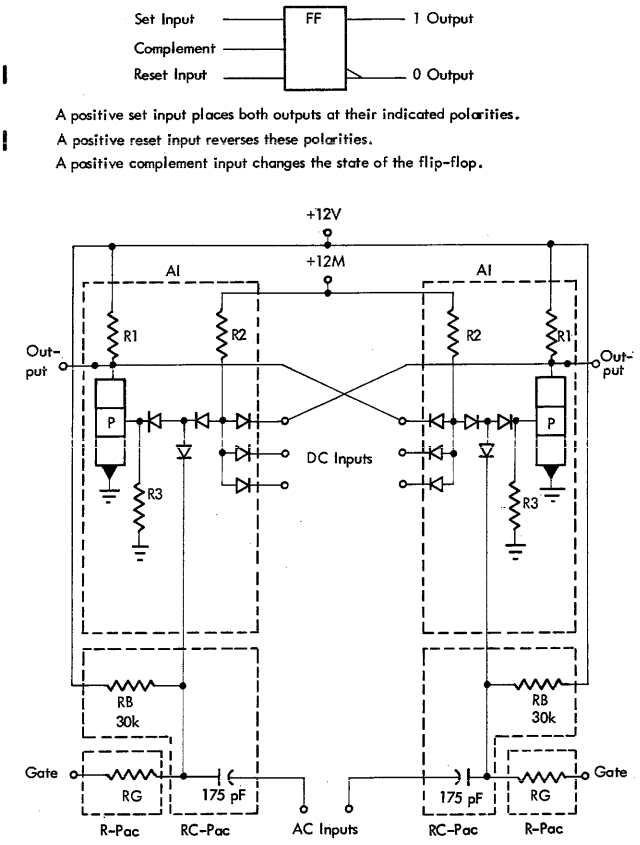


Figure 1-10. Flip-Flop (FF) Circuit

The polarity hold block may have a reset input. When the reset input is at its indicated polarity, the output is at a polarity opposite to that indicated.

Schematic Operation

Sequence 1: Control input is normally down.

1. Data Line Up – Rise of control input sets the output to the 1 state.
2. Data Line Down – Rise of control input sets the output to the 0 state.

As long as the data line remains constant, changes in the control input do not change the output.

Sequence 2: Control input is normally up.

1. Data Line Up – Fall of the control input holds the output in the 1 state.
2. Data Line Down – Fall of control input holds the output in the 0 state.

As long as the control input is up, the output changes with the data line. When the control input falls, further changes to the data line do not affect the output, and the output remains at whatever polarity it had at the moment the control line dropped.

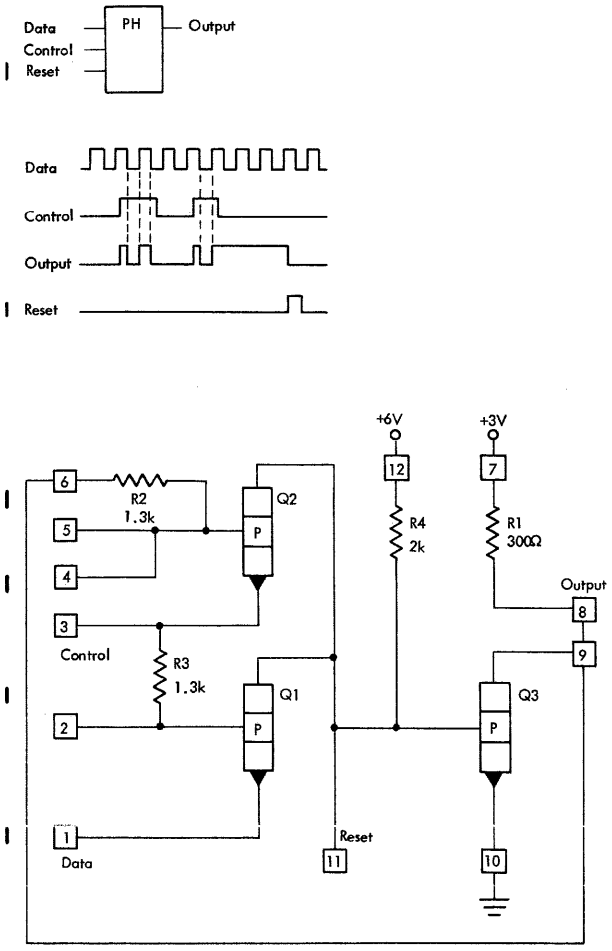
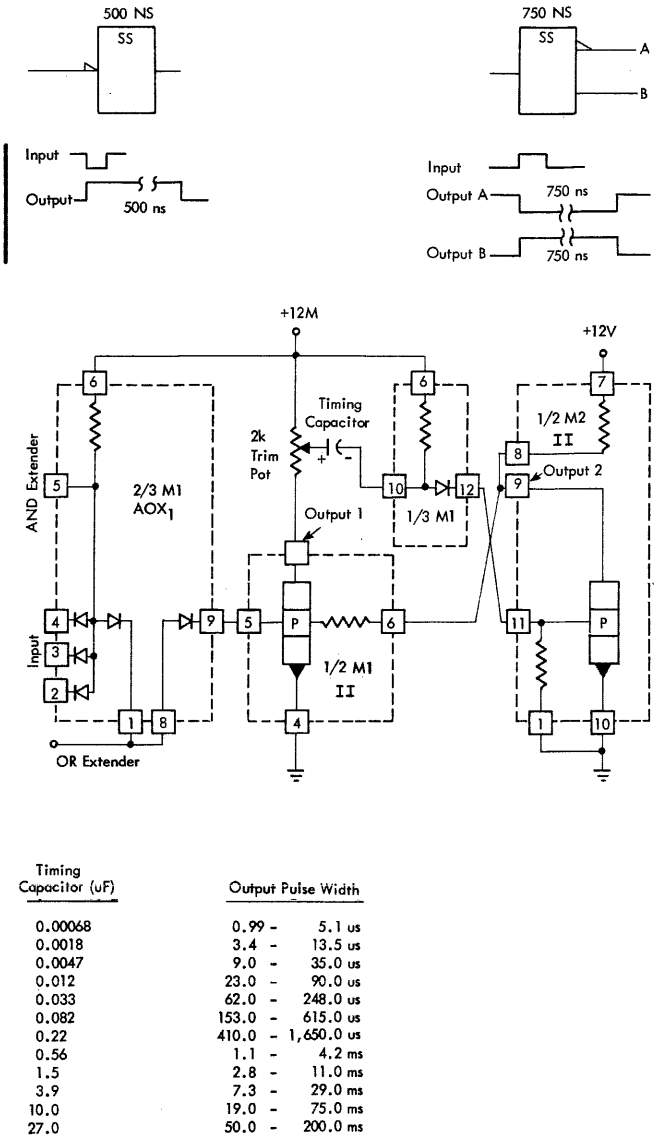


Figure 1-11. Polarity Hold (PH) Latch



Timing Capacitor (uF)	Output Pulse Width
0.00068	0.99 - 5.1 us
0.0018	3.4 - 13.5 us
0.0047	9.0 - 35.0 us
0.012	23.0 - 90.0 us
0.033	62.0 - 248.0 us
0.082	153.0 - 615.0 us
0.22	410.0 - 1,650.0 us
0.56	1.1 - 4.2 ms
1.5	2.8 - 11.0 ms
3.9	7.3 - 29.0 ms
10.0	19.0 - 75.0 ms
27.0	50.0 - 200.0 ms

Figure 1-12. Singleshot (SS) Circuit

Singleshot (SS) Circuit

The output of a singleshot (Figure 1-12) changes temporarily to its indicated polarity when the input receives a signal of the indicated polarity. The output remains in this quasi-stable state for a time that is characteristic of the particular block. The title area of the block shows the time duration. If a singleshot has more than one output not of the same time duration, the time durations are labeled or otherwise noted.

The variable singleshot shown in the schematic consists of one AOX_1 module, one isolating inverter (II) module, one trimming potentiometer, and one capacitor. A positive-going pulse starts the singleshot. It has two complementary outputs; output 2 is in phase with the input. Width of the output pulse is controlled by the 2k trimming potentiometer and timing capacitor. The capacitor fixes the range of output pulse widths as shown in the table. The 2k potentiometer provides continuous adjustment in each range.

Between the end of the output pulse and the start of the next input pulse, a minimum recovery time must exist to allow the capacitor to charge; recovery time is equal to or greater than the desired output pulse width. Premature triggering results in an incorrect pulse width.

Oscillator

An oscillator produces a uniform, repetitive, continuous output, or produces an output only when the input signal is at its indicated polarity (Figure 1-13). The schematic illustrates a 4.0 mHz free-running oscillator and pulse generator. The circuit consists of a basic switching circuit having an output dependent upon the quartz crystal. This crystal vibrates at 4.0 mHz and develops a sinusoidal voltage that is amplified and clipped to produce a square-wave output. An inductively tuned tank circuit provides regenerative feedback to sustain the crystal oscillations.

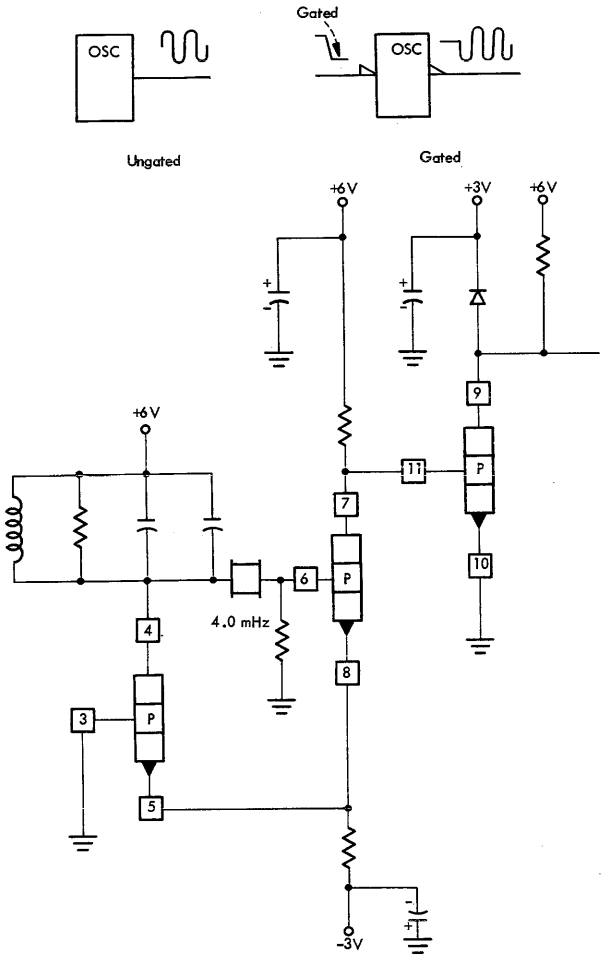


Figure 1-13. Oscillator Circuit (Typical)

SOLID LOGIC TECHNOLOGY (SLT)

Solid Logic Technology is one of several technologies used in System/360 era machines and systems. As in other technologies, the physical building blocks of SLT are the transistor chip, module, card, board, and gate.

1. The basic semiconductors of which circuits are composed are the dual diode and single transistor chip, which are each about 0.025 inch square.
2. Chips are mounted on a substrate with screened resistors and connected by printed wiring. The substrate and its components are encapsulated to form a 0.500 inch square module.
3. Modules plus molded resistors, capacitors, and other components are mounted on pluggable cards, which contain printed wiring to connect components. Cards can contain 6, 12, 24, 36, or more modules.
4. Cards plug into 8½ x 12½ inch boards, with printed wiring interconnections, and in turn are connected by cables to form gates, and then frames.

SLT Circuits

The basic SLT circuit is the AND-OR-inverter (AOI). SLT operating circuit speeds and voltages are:

5-10 ns	+0.9V to +3.0V	High Speed
30 ns	+0.0V to +3.0V	Medium Speed
700 ns	+0.0V to +12.0V	Low Speed

Each logical function, such as an FF, may use a different circuit for each of the three circuit speeds.

SLT Circuit Transitions

Transition (Figure 1-14, example A) is the time required for a transistor output to switch from one logic state to another. Voltage levels at which transitions are measured in SLT and SLD are:

Circuit Family	*Transition Measuring Points*
5-10 ns	+1.2V and 1.9V
30 ns	+0.3V and 1.8V
700 ns	+0.29V and 2.0V

Switching times include turn-on transition, turn-off transition, turn-on delay, and turn-off delay. Transition times are turn-on transition and turn-off transition. These values are generally the same for each of the circuit families. The major difference is that the transition points and voltage levels vary for each family.

Turn-on Transition (Figure 1-14, example B) is the time required for the circuit to switch from an off state to an on state. Turn-on transition is measured on the output waveform from a specified value in the nonconducting state to a specified value in the conducting state.

Turn-off Transition (Figure 1-14, example C) is the time required for the circuit to switch from an on state to an off state. Turn-off transition is measured on the output waveform from a specified value in the conducting state to a specified value in the nonconducting state.

Turn-on Delay (Figure 1-14, example D) or *turn-off delay* (example E) is the time required for the circuit to change its output state after a change in the input state has occurred. Switching time is measured from a point where the input waveform has reached a specified value to a point where the output waveform has reached a specified value.

SOLID LOGIC DENSE (SLD)

The Solid Logic Dense technology increases packaging density and circuit performance with respect to SLT. The gain mainly results from mounting transistors and diodes on top of the substrate and mounting resistors on the bottom of the substrate. SLD circuit-switching speeds are 30, 100, and 700 nanoseconds. Voltage levels and transition times are the same as in SLT circuits.

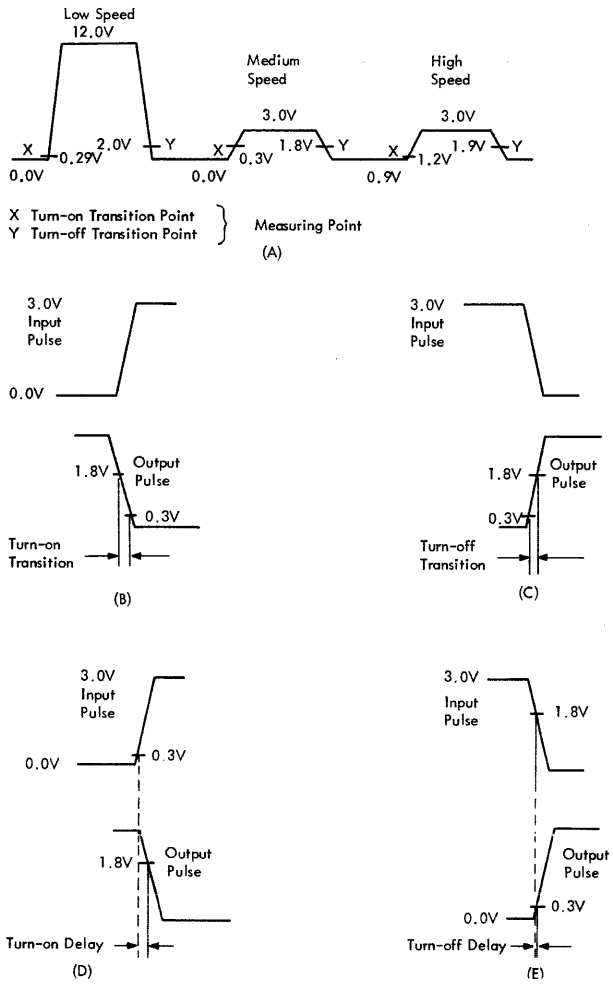


Figure 1-14. SLT Transitions

ADVANCED SOLID LOGIC TECHNOLOGY (ASLT)

ASLT, an offshoot of SLT, stacks two ceramic substrates in a module, thereby increasing circuit performance by 2½ to 3 times that of SLT. ASLT circuits have switching speeds of 2-10 nanoseconds. Input and output voltage levels for ASLT are shown in Figures 1-15 and 1-16. ASLT transitions and delays are given in Figures 1-17 and 1-18.

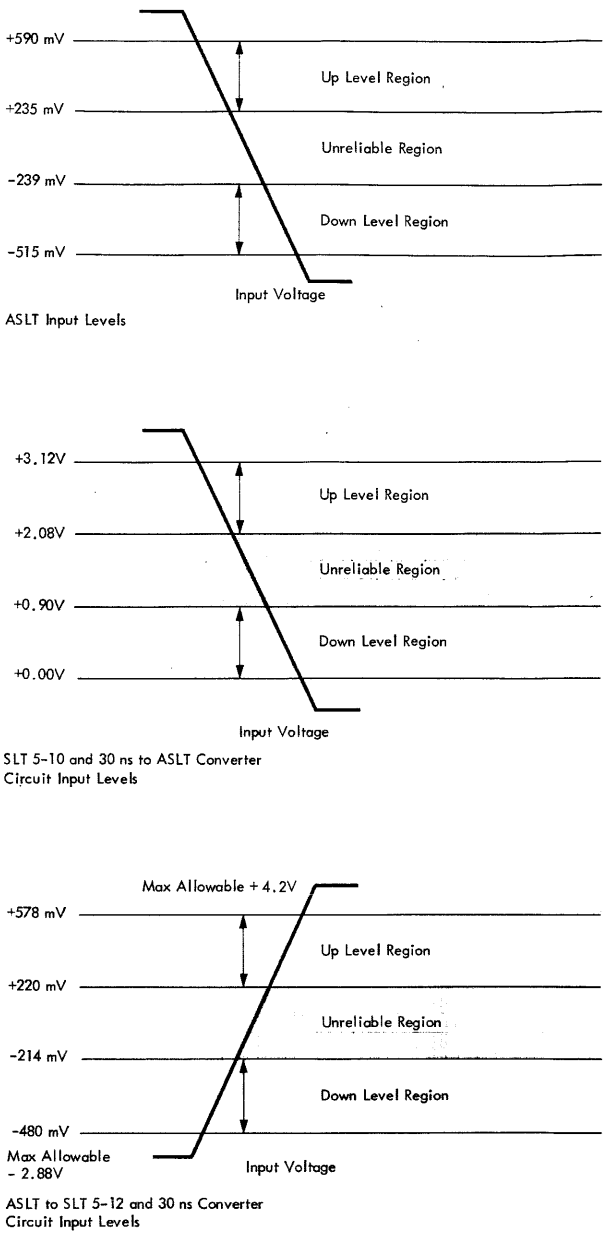
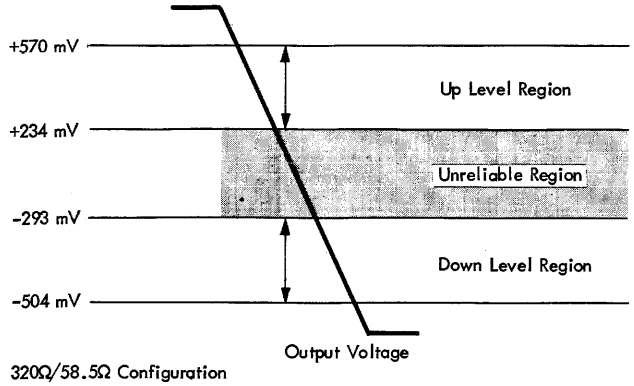
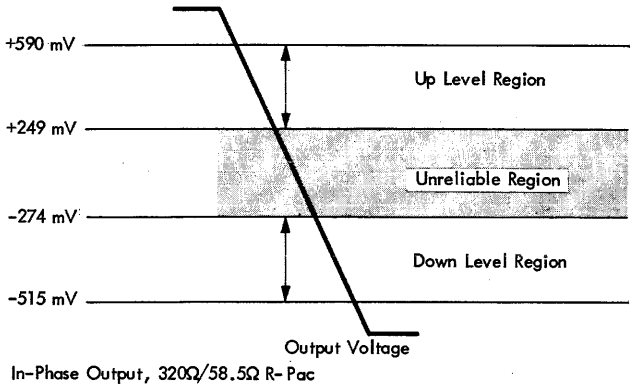


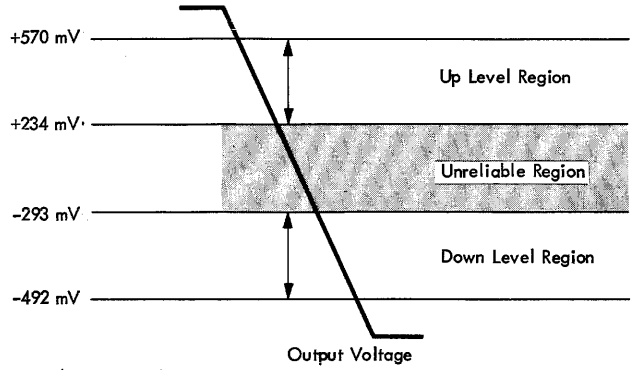
Figure 1-15. ASLT Input Voltages



320Ω/58.5Ω Configuration

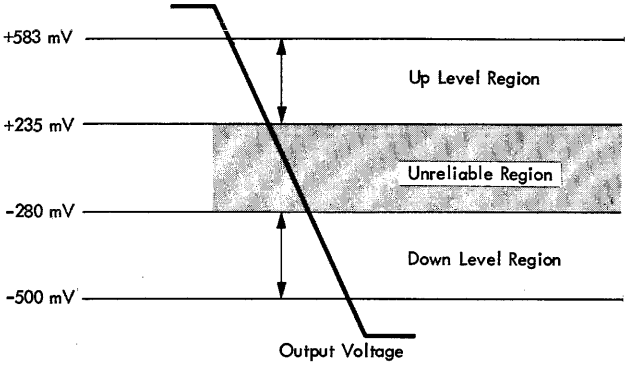


In-Phase Output, 320Ω/58.5Ω R-Pac

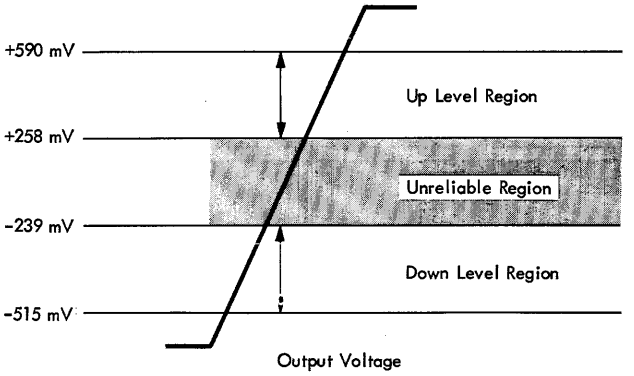


281Ω/49.5 Ω Configuration

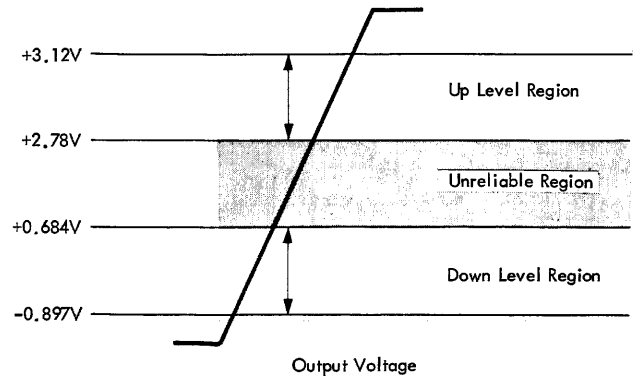
SLT 5-10 and 30 ns to ASLT
Converter Circuit Output Levels



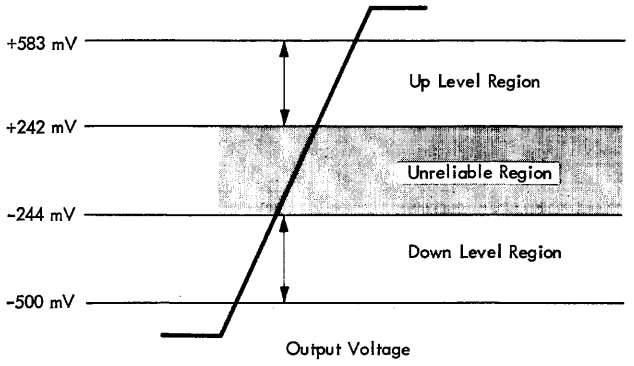
In-Phase Output, 281Ω/49.5Ω R-Pac



Out-of-Phase Output, 320Ω/58.5Ω R-Pac



ASLT to SLT 5-12 and 30 ns
Converter Circuit Output Levels



Out-of-Phase Output, 281Ω/49.5Ω R-Pac

Figure 1-16. ASLT Output Voltages

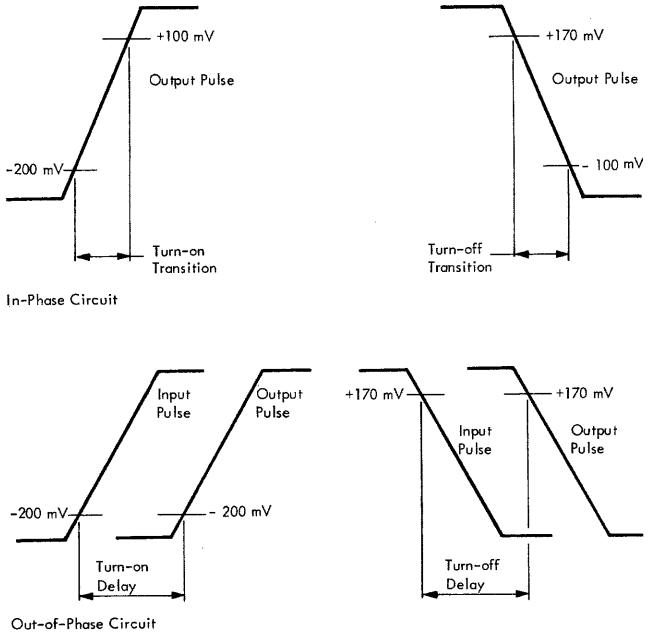


Figure 1-17. ASLT In-Phase Transitions and Delays

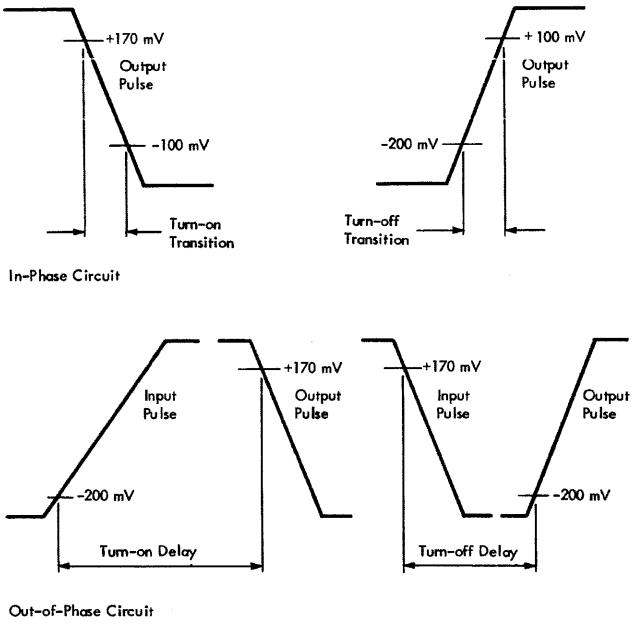


Figure 1-18. ASLT Out-of-Phase Transitions and Delays

ASLT Basic Circuits

A basic circuit in ASLT is the emitter-follower-coupled switch, which is used in several configurations: an in-phase circuit, an out-of-phase circuit, and an in-phase and out-of-phase circuit. Current-switching logic permits increased operating speeds. Transistors are not usually operated in saturation and small voltage swings are used. A phase-compensating network in the emitter current source makes these circuits stable.

MONOLITHIC SYSTEM TECHNOLOGY (MST)

The smallest circuit building block in MST is the integrated circuit chip, which contains about five circuits and is roughly equivalent to an SLT card. An encapsulated, 0.500-inch square module contains from one to four circuit chips and screened connections mounted on one side of the substrate. Resistors are packaged on the same card, external to the MST module. A maximum of 60 modules may be placed on the MST card, along with separate resistors and capacitors. The card has laminated signal and voltage planes, similar to an SLT board.

MST circuits have switching speeds of 2-5 ns, 30 ns, and 100 ns and voltage levels of +1.25V and 0.0V to -3V. Input and output voltages for MST circuits are shown in Figure 1-19.

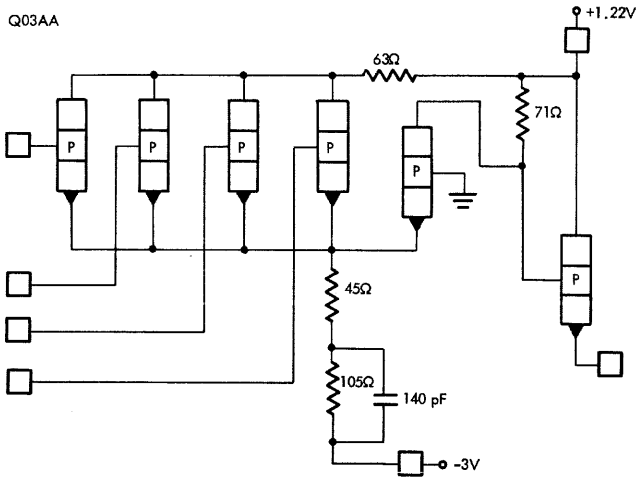


Figure 1-19. MST Input and Output Voltages

MST Basic Circuits

MST uses basic current-switch emitter-follower circuits: the high-power circuit, and the low-power circuit. Low-power circuits drive loads within the module; high-power circuits drive loads external to the module.

Terminating resistors are contained in an R-Pac or RC-Pac. Because each leg of an AND/OR block must not float, unused legs are terminated by external resistors.

FET Circuits

FET circuits are integrated circuits in which the major active element is a field effect transistor (FET), a three-terminal, semiconductor device identical in function (current control) to earlier junction transistors. In Figure 1-20, the three terminals (source, gate, drain) compare to the emitter, base, and collector of a junction transistor. The gate on the FET controls current flow. In some FET devices, the source and drain are interchangable. The earliest FET device is a static FET, which operates by the gate setting up an electronic field transverse to the direction of current flow, which controls the output current.

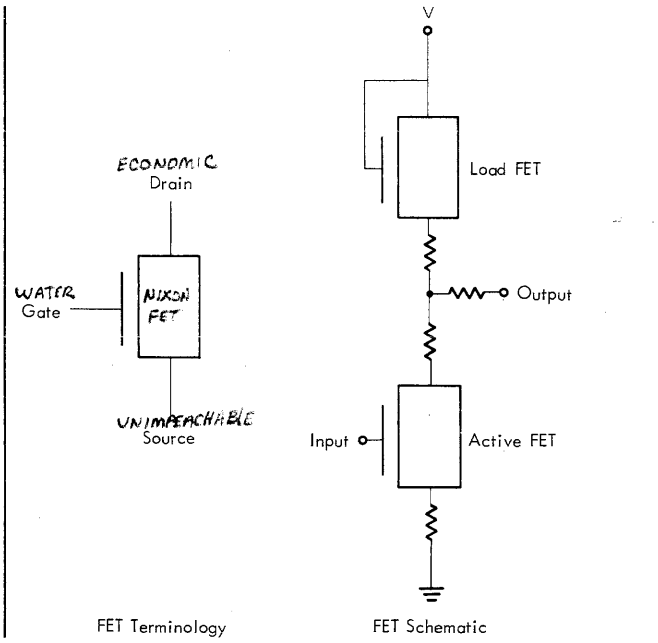


Figure 1-20. Field Effect Transistor

FET circuits are characterized by low power dissipation and relatively long risetimes. The basic FET logic block is a static OR-inverter circuit.

TTL Circuits

TTL (transistor-transistor logic) circuits have the following characteristics: medium speed, high volume, low cost. A TTL circuit chip contains densely packed integrated circuits, encapsulated in a dual-in-line module having 14, 16, or 24 pins. In contrast to an MST module, a TTL module is rectangular and has pins aligned in two rows. Figure 1-21 shows the general voltage and delay values of TTL circuits.

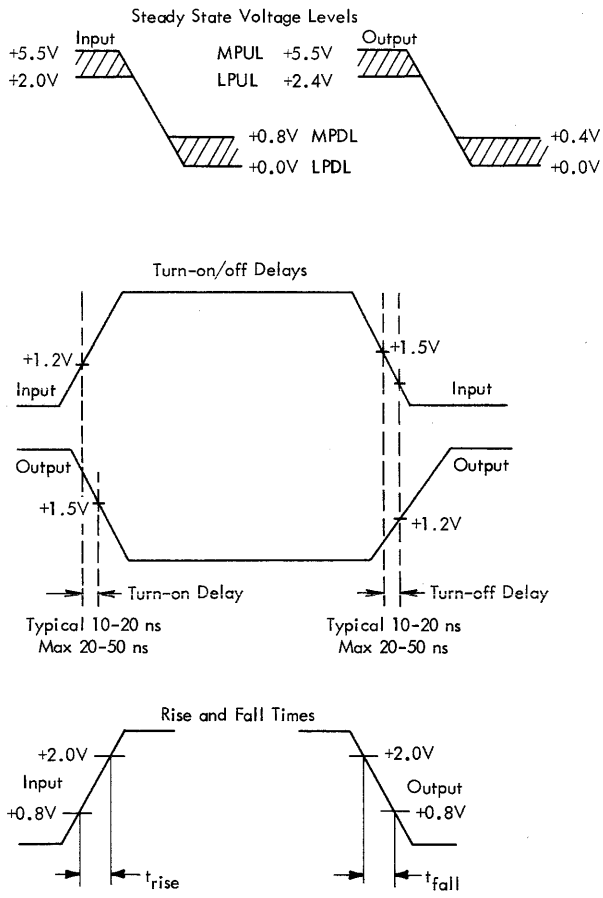


Figure 1-21. TTL Voltage Levels and Delays

- Logic blocks appear on all forms of Automated Logic Diagrams.
- Standard logic blocks include unit logic (AND/OR/FF etc.) and component blocks (relay, capacitor, etc.).
- Circuits may be represented by multiple block configurations.
- Higher level blocks include macro-logic and functional logic blocks, such as the selector, register, and decoder on FEALD's.
- Nonlogic blocks include: entry/exit block, service-voltage block, and cable block.

This chapter describes logic blocks appearing in all forms of ALD's–the engineering ALD, the Field Engineering ALD, and the card ALD. These descriptions are independent of technology and concern logical function, not circuit schematic operation. The order of treatment is from unit logic, as seen on all forms of ALD's, through the multiple block configurations, macro-logic, and butted blocks, to that logic appearing only on an FEALD.

UNIT LOGIC

AND

The output of the AND block is at its indicated polarity only when all of its inputs are at their indicated polarities. The letters in the block are the symbol of the function. In this case, A is the symbol for the AND function (Figure 2-1).

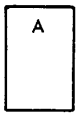


Figure 2-1. AND Block

Positive AND (Negative OR)

The output of the positive AND block is in its more positive condition only when all the inputs are in their more positive condition (Figure 2-2).

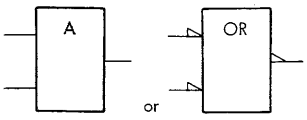


Figure 2-2. Positive AND Block

Positive-AND-Inverter

The output of the positive-AND-inverter is in its more negative condition only when all of the inputs are in their more positive condition (Figure 2-3).

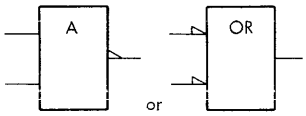


Figure 2-3. Positive-AND-Inverter Block

OR

The output of the OR block is at its indicated polarity only when one or more of its inputs are at their indicated polarity (Figure 2-4).

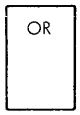


Figure 2-4. OR Block

Positive OR (Negative AND)

The output of the positive OR block is in its more positive condition only when one or more of the inputs are in their more positive condition (Figure 2-5).

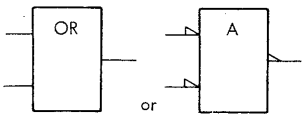


Figure 2-5. Positive OR Block

Positive-OR-Inverter

The output of the positive-OR-inverter is in its more negative condition when one or more of the inputs are in their more positive condition (Figure 2-6).

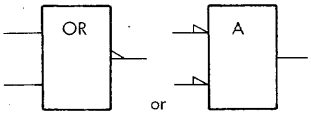


Figure 2-6. Positive-OR-Inverter Block

Exclusive OR

The output of an exclusive OR block is at its indicated polarity when *only one* of its inputs is at the indicated polarity (Figure 2-7).

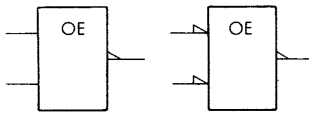


Figure 2-7. Exclusive OR Block

The following examples describe types of inverter, amplifier, threshold, odd, and even functions.

Inverter

The output of the inverter is of opposite potential to the input (Figure 2-8).

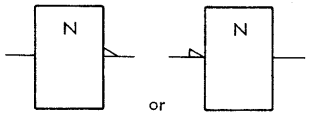
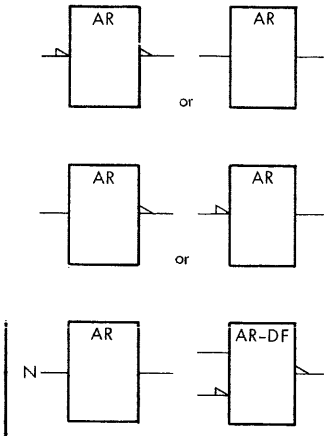


Figure 2-8. Inverter Block

Amplifier

The amplifier (AR) provides adequate driving energy and an appropriate impedance match to other blocks. The amplifier output is at its indicated polarity only when the input is at its indicated polarity (Figure 2-9).



The lower two blocks are AR variations. In the first, the N indicates a negative pulse or shift that is amplified. In the AR-DF differential amplifier, both inputs must be present; the hyphen indicates a non-standard input or output voltage. See Figure 2-63 for a definition of differential amplifer.

Figure 2-9. Amplifier Block

Threshold

The output of the threshold is at its indicated polarity only when the number of inputs (at their indicated polarity) reaches or exceeds the number specified in the function symbol.

The A-(n) symbol (shown in Figure 2-10) has at least two inputs. The number specified in the function symbol is not 1, or equal to the number of inputs.

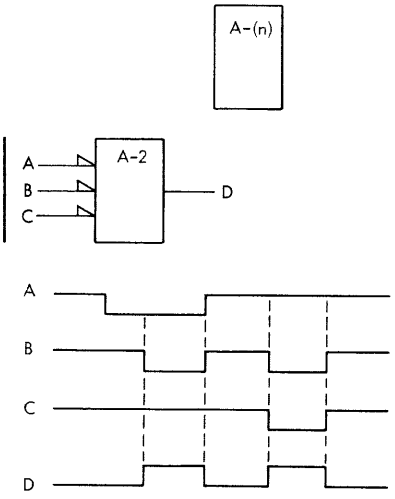


Figure 2-10. Threshold Block

Odd Count

The output of odd count (OD) is at its indicated polarity only when an odd number (such as 1, 3, 5, and 7) of inputs are at their indicated polarity (Figure 2-11).

Note: An OD block may be shown as an even count (EV) by changing the polarity indication. The AND and OR circuits have a similar relationship.

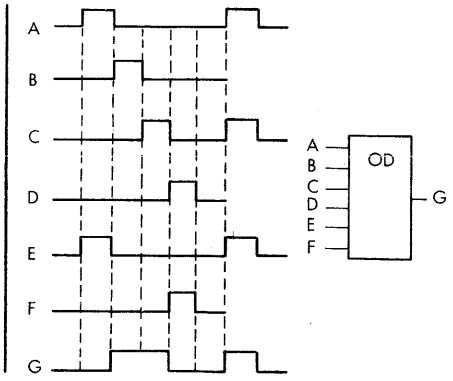


Figure 2-11. Odd Count Block

Even Count

The output of even count (EV) is at its indicated polarity only when an even number (such as 0, 2, 4, and 6) of inputs are at their indicated polarity (Figure 2-12).

As noted earlier, an EV may be shown as an OD by changing the polarity indication. This change may be compared to the AND and OR circuit.

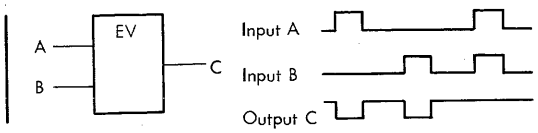


Figure 2-12. Even Count Block

Flip-Flop

The flip-flop has two stable states. One of these is the 1 state or set state; the other is the 0 state or reset state. The flip-flop block normally has two outputs, a 1 output and a 0 output. In the ALD's, a line from the upper part of the block represents the 1 output and a line from the lower part of the block represents the 0 output.

The flip-flop is in the 1 state when the 1 output (the upper output on the ALD) is at its indicated polarity. Regardless of the input of a flip-flop, its 1 output and 0 output in the stable state are always opposite in polarity.

A signal of indicated polarity sent to the line opposite the 1 output causes the outputs of the block to assume their indicated polarities.

A signal of indicated polarity sent to the line opposite the 0 output causes the outputs to assume polarities opposite to those indicated.

A signal of indicated polarity sent to a line centered between the two lines already mentioned, or sent to both the set and reset inputs simultaneously, changes the state of the flip-flop (complements the flip-flop).

The polarities shown at the inputs and outputs of a flip-flop for a particular circuit are unchanging parts of the symbol (Figure 2-13).

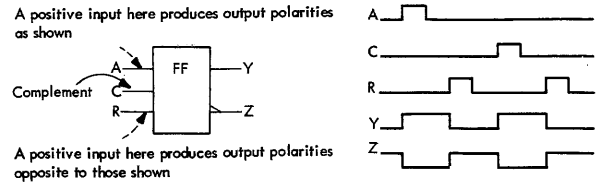


Figure 2-13. Flip-Flop Block

Master-Slave Flip-Flop

The "master-slave" flip-flop uses the trailing-edge symbol (⌐), see "Storage Blocks (FEALD)" for definition, and sets on the trailing edge of the setting pulse. When this pulse goes to a polarity opposite to that indicated, the flip-flop is set.

Flip-Flop Latch or Flip Latch

The definition of the flip-flop latch or the flip latch is the same as that given for a flip-flop, except that simultaneous signals of the indicated polarity at the 1 input and the 0 input are not a normal operation. If, however, simultaneous set and reset occur, the design of the circuit determines the polarity of both outputs (Figure 2-14).

The complement input is not used with the flip-latch block.

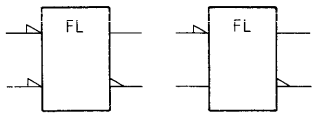


Figure 2-14. Flip Latch Block

Polarity Hold

The output of this block is at the indicated polarity when the data line is at its indicated polarity and the control line is at its indicated polarity. When the control input goes to the polarity opposite to that indicated, the output remains at whatever polarity it possessed at that moment. The PH block may have a reset input. If so, when the reset input is at its indicated polarity, the output is opposite to that of its indicated polarity.

The data line is the input line toward the top of the block. The control line is centered on the input side of the block. The reset line is toward the bottom of the block (Figure 2-15).

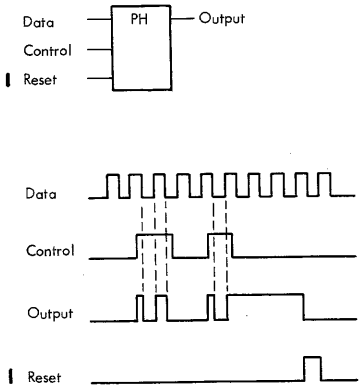


Figure 2-15. Polarity Hold Block

Singleshot

The output of the singleshot (Figure 2-16) changes temporarily to the indicated polarity when it receives an input signal of the indicated polarity. The output remains in this quasi-stable state for a time characteristic of the particular

block. The singleshot always has the time duration shown in the title area of the block. If a singleshot has more than one output not of the same duration, the block is labeled or a reference note on the page relates pin numbers to time durations.

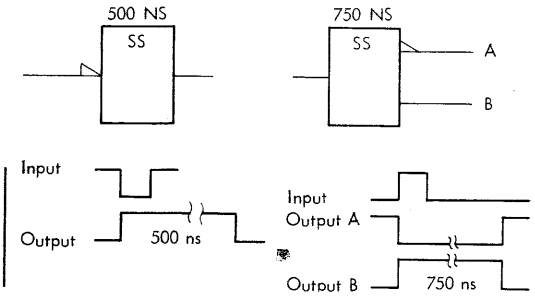


Figure 2-16. Singleshot Block

Schmitt Trigger

The output of the Schmitt trigger goes to its indicated polarity when the input crosses the threshold in the direction of the indicated polarity. The output remains at this indicated polarity until the input signal crosses the threshold in the opposite direction (Figure 2-17). The nominal threshold voltage is indicated in the block title area.

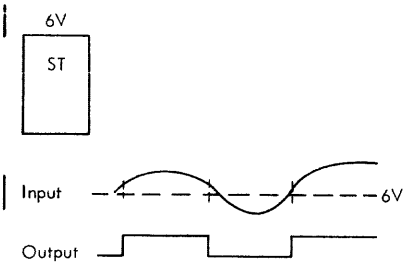


Figure 2-17. Schmitt Trigger Block

Oscillator

The oscillator produces a uniform, repetitive output either continuously or during the application of an input signal of the indicated polarity.

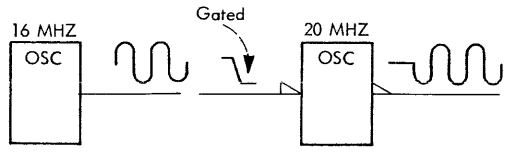


Figure 2-18. Oscillator Block

Special Blocks

Two conditions must exist for a block to be designated as special:

1. The function is not covered by any single block symbol.
2. The function cannot be expressed in terms of an interconnected set of individual block symbols.

The function of a special block is described by the wording on the ALD, either at the block or in a comment area referenced by a note in the title area of the block (Figure 2-19).

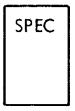


Figure 2-19. Special Block

Converter

The converter block provides the necessary conversion or translation between two types of logic: voltage mode to current mode, voltage to voltage, etc. An indication of input and output voltage levels, or line types, is shown in the title area of the block (Figure 2-20).

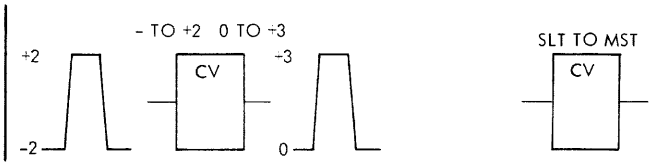


Figure 2-20. Converter Block

Time Delay

The time delay block delays a signal without intentional distortion of the signal. The time delay symbol must always be accompanied by the time delay (Figure 2-21).

Time delays having a delay time for the leading edge of the output that is different from the time delay for the trailing edge are identified by the placement of an L for leading and a T for trailing immediately prior to the separate delay times in the block area. The input polarity at the block must be that associated with the "leading" edge of the output.

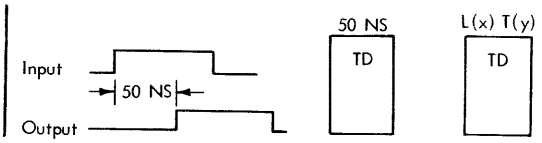


Figure 2-21. Time Delay Block

Limiter

The limiter block sets one or both extremes of a waveform to a predetermined level without intentional distortion of the remaining waveform (Figure 2-22).

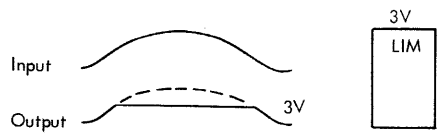


Figure 2-22. Limiter Block

Current Switch

Sometimes it is difficult to describe the logic operations of ANDing and ORing because of the use of series control of current flow; for example, handling the drive currents in a magnetic core array. At times the purpose of a circuit is to allow a flow of current (either in or out) under logic voltage control. When this condition exists, the circuit cannot cause the current to flow solely through electrical action at its own logic input. Because of the series flow of this current through other controlling circuits, the circuit may be given the function label CS (current switch).

The control input of the CS is placed toward the top of the block. Sending a signal of indicated polarity to this input allows (not necessarily causes) electron flow through the block in the direction indicated by the polarity symbol at the output side of the block (on the current line). A negative polarity symbol indicates electron flow away from the output side. A line opposite the output line is assumed to be the same current line, separated by the circuitry of the CS. The polarity indication for this line is the same as that of the corresponding output line (Figure 2-23).

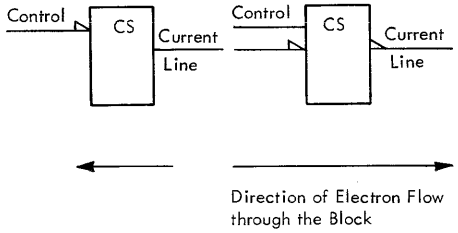


Figure 2-23. Current Switch Block

Figure 2-24 shows the use of the current switch in the control of a series flow of current through more than one circuit. A negative signal at ① causes current to flow in the array, provided the control signal is negative at ②.

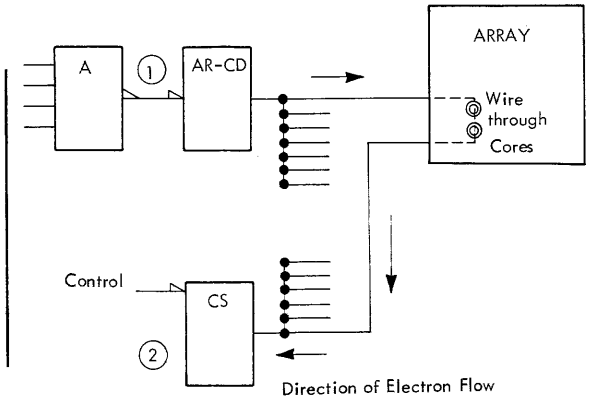


Figure 2-24. Current Switch Circuit

COMPONENT AND AUXILIARY BLOCKS

Many types of components may be mounted on a logic card. The following examples are typical (Figures 2-25, 2-26, and 2-27).

Component Blocks

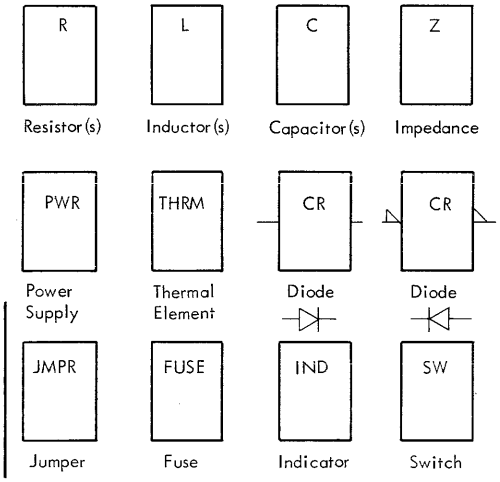


Figure 2-25. Component Blocks

Switch Blocks

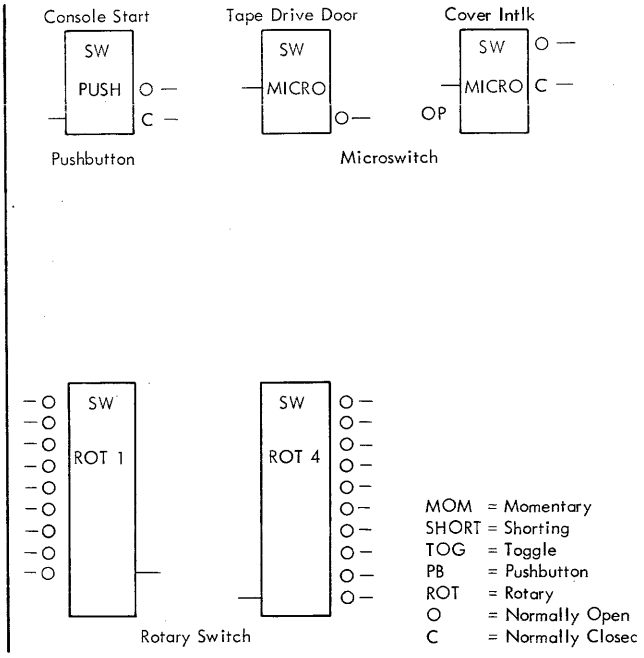
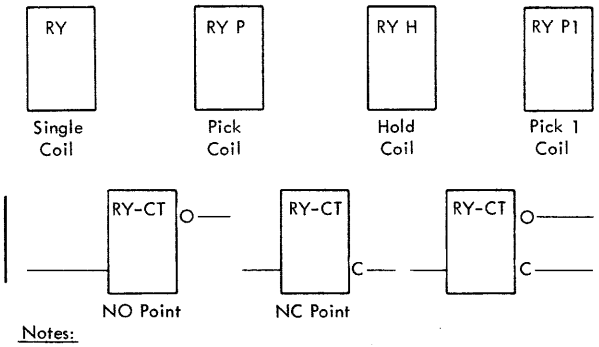


Figure 2-26. Switch Blocks

Relay Coil and Contact Blocks



Notes:

1. One set of contact points will be shown in each block.
2. This symbology refers to relays mounted on cards.

Figure 2-27. Relay Coil and Contact Blocks

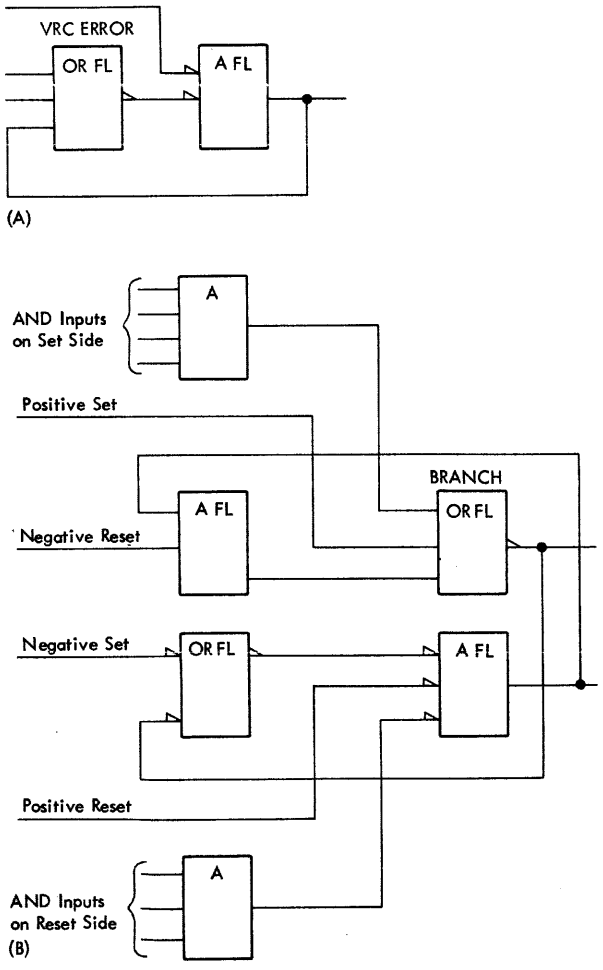


Figure 2-28. Bi-stable Circuits

MULTIPLE BLOCK CONFIGURATIONS

Bi-stable Circuits

The flip-flop, flip latch, or polarity hold circuits (Figure 2-28) may be designed with AND-OR blocks instead of a single circuit. When these bi-stable circuits are shown in multiple block form, one of the blocks is an OR block placed toward the top (or left) in the block arrangement containing the cross-coupled parts. The title of the arrangement is placed above this OR block (Figure 2-29).

When AND-OR blocks are arranged to perform the function of a flip latch, flip-flop, or polarity hold, the symbol FL, FF, or PH is added to the AND-OR function symbol in the top of every block making up the cross-coupled arrangement. An exception to this arrangement occurs when the AND-OR block is part of a DOT AND or DOT OR. (See "DOT OR and DOT AND.")

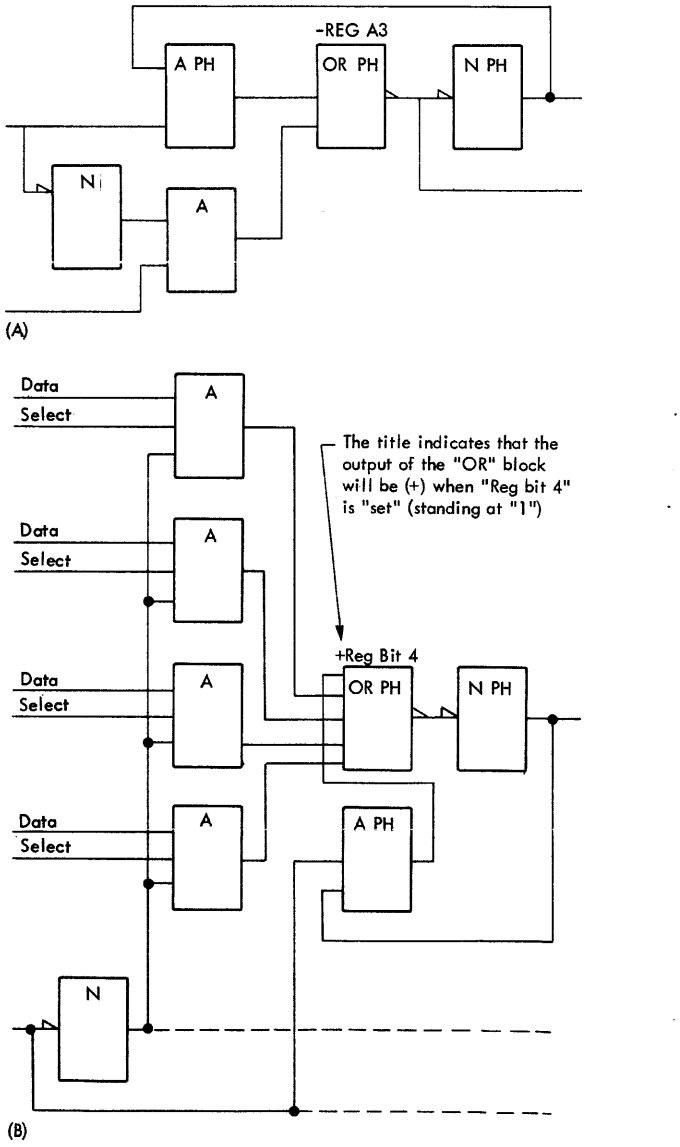


Figure 2-29. Multiblock Circuits

DOT OR and DOT AND

Basic blocks whose outputs are connected externally to perform an AND or OR operation (DOT AND and DOT OR) are identified by an additional A or OR placed in the block to the right of the primary block function symbol. In ALD's a block labeled OR DOT or A DOT is used to form the junction of the lines being connected (Figure 2-30).

When the output of a block enters both a DOT OR and a DOT AND, the letters WL (wired logic) are placed to the right of the primary block function symbol.

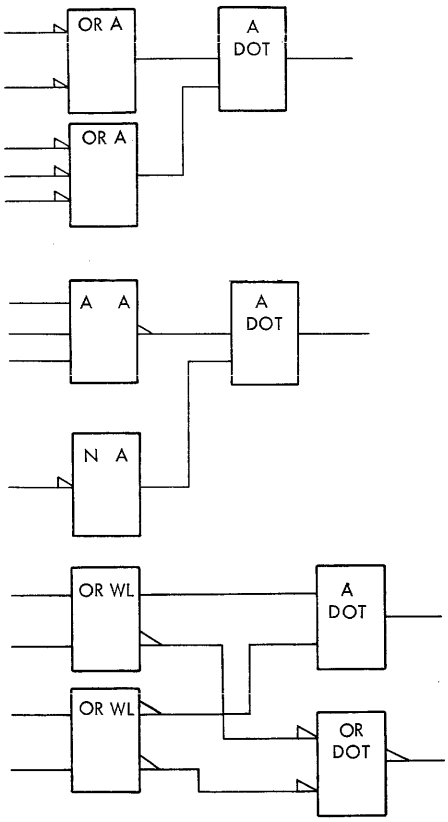


Figure 2-30. DOT-OR and DOT-AND Blocks

NONLOGIC BLOCKS

Entry and Exit Blocks

Entry and exit blocks (Figure 2-31) can be used to show crossreferencing from one machine to another or a line crossing a machine type. The information may be associated with the line name or it may be shown in a pseudo block. These pseudo blocks are identified by an asterisk (*) in the sixth position of line 1. The machine type from which the line is coming or to which the line is going is on line 2.The machine type where the logic block is located is on line 3. The page of the other end of the line is shown on line 4. Line 5 is the serial number of the block on the other end of the line. The print location and serial number of the logic block are shown on line 6.

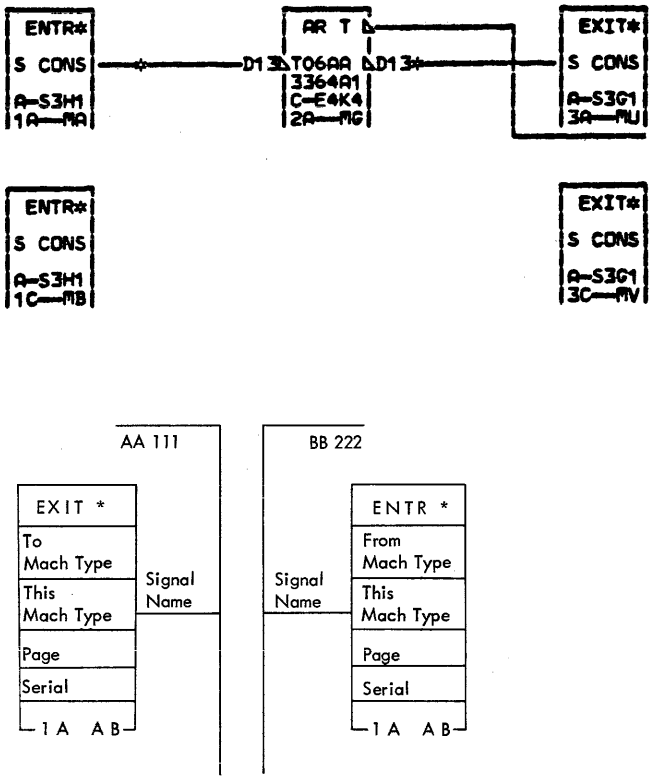


Figure 2-31. Entry and Exit Blocks

Service-Voltage Logic Blocks

The four-character mnemonic code (SERV) identifies one type of pseudo block. An asterisk (*) in the first character of line 1 indicates that the inputs are in particular positions; the asterisk (*) in the last character of line 1 indicates that the block is special. Line 3 identifies the voltage. Line 5 locates the card socket. The logic block pin numbers identify which pins are wired for the particular voltage.

A SERV logic block (Figure 2-32) indicates that a voltage is wired into a connector area by printed wiring.

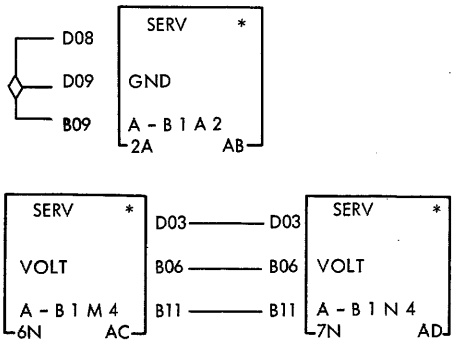


Figure 2-32. Service-Voltage Logic Blocks

Note: No voltages are present in either of the two outside columns (A and N) of card sockets on the board.

Normally, the sockets in columns A and N of the board are used for cable connectors. When these sockets are used for cards, service voltages are brought to these sockets by printed wiring. This arrangement is shown with the SERV special block (Figure 2-32). When a half cable connector plugs into column A or N on the printed board, additional ground wires are shown on the ALD's in the lower half of the socket. A board is not normally wired in this way. Normally, on a given board all blocks that are used for service voltages appear on the same ALD page(s).

Cable Logic Blocks

Two logic blocks (Figure 2-33) are used to define each cable: one logic block shows the "from" location; the other logic block shows the "to" location. Line 1 contains CABL* for regular cables (both intergate and intragate) and XOVR* for crossover cables.

Basic data in the block provides cable block identification: location of the end points, cable assembly part number, location suffix (half cable can be plugged into top or bottom section, or left or right section of the connector socket), intergate sequence numbers, and orientation of intergate cable.

The code used in Figure 2-33 is:

NNNN	Last four numbers of the cable assembly drawing appear only in the "from" block. The first three numbers (580) are understood as relating to the part number.
P	Socket portion used; that is, T for top, B for bottom, and F (or blank) for full; this appears as a location suffix.
QQQQ	Installation sequence number (required in both blocks of the intergate cable).
GGBBSS	Gate, board, and socket for the respective end of the cable.
Z	L or R indicates left or right for the direction this cable takes in leaving the board specified in the "from" block. (Assume a position facing the card side of the board.)

Cable blocks have "from" and "to" orientations similar to the orientations of the particular cable assembly reference drawings.

Line 2 may contain an additive card code, but it is not required.

Installation Sequence

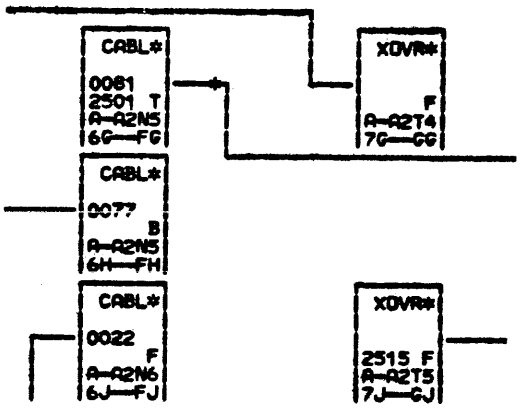
Intergate cables are divided into groups; each group contains all the cables connecting a particular pair of logic or I/O gates. The group number is the first number of the code QQQQ. It defines the cabling sequence required for gate pairs. The number may be 1 through 9. Other numbers of the code QQQQ are the installation order of the cables in the group, with the lower numbers being installed first, advancing in order to the higher numbers.

Via Points

The point at which the intergate cable leaves the gate is designated as a via and the point at which it enters the "to" gate is designated as a via.

Via coordinates identify channel intersections as well as identify segments of the vertical channel. Within the channel intersection and within the vertical segments, channel coordinates are specified. At these coordinates, the cable is folded and the lengths are specified.

The via points are shown in order from one end of the cable to the other. The format of routing vias is in the form FFG-VVCC---: FF designates frame, G- designates gate, VV designates via coordinate, CC designates channel coordinate, and --- (three dashes) fill out the 11 characters. An example is 01A-C2D5---.



Cable Block Formats

	X	O	V	R	*
N	N	N	N		P
G	G	B	B	S	S

Crossover Cable

	X	O	V	R	*
					P
G	G	B	B	S	S

From

	C	A	B	L	*
N	N	N	N		P
G	G	B	B	S	S

Intragate Cable

To

	C	A	B	L	*
					P
G	G	B	B	S	S

	C	A	B	L	*
Q	Q	Q	Q		
N	N	N	N		P
G	G	B	B	S	S

Intergate Cable *

	C	A	B	L	*
Q	Q	Q	Q		
				Z	P
G	G	B	B	S	S

*Denotes via listing at the bottom of the ALD page.

Figure 2-33. Cable Logic Blocks

Cable Routing

The routing of the cable is given by via and channel coordinates (Figure 2-34). These coordinates are identified by the asterisk (*) on the line between the "to" and "from" block. The asterisk (*) references the connector field at the bottom of the (cable) ALD page.

The general form of the via designation is:

01	A-	C2	D5	---
		Via	Channel	Not
Frame	Gate	Coordinate	Coordinate	Used

The general form of a logic connector is:

01	A-	D3	B2	D09
Frame	Gate	Board	Socket	Pin

Example 1 in Figure 2-34 shows a six-pack cable on gate A in frame 01 between board A1 socket N3 and board C2 socket A3. In this example, the connector listing is:

01A-A1N3	(Appears in CABL* Block)
01A-A1N3	Identification
01A-B1H2 ---	Cable Vias
01A-B2B2 ---	
01A-C2B2 ---	
01A-C2H2 ---	
01A-C2A3	(Appears in Second CABL* Block)

Example 2 in Figure 2-34 shows a split six-pack cable on gate B in frame 01 between board B1, top half of the socket A4, and board A2, bottom half of socket A6. In this example, the connector listing is:

01B-B1A4T	(In CABL* Block)
01B-B1K1 ---	Cable Vias
01B-B2C1 ---	
01B-A2C3 ---	
01B-A1T3 ---	
01B-A2A6B	(In CABL* Block)

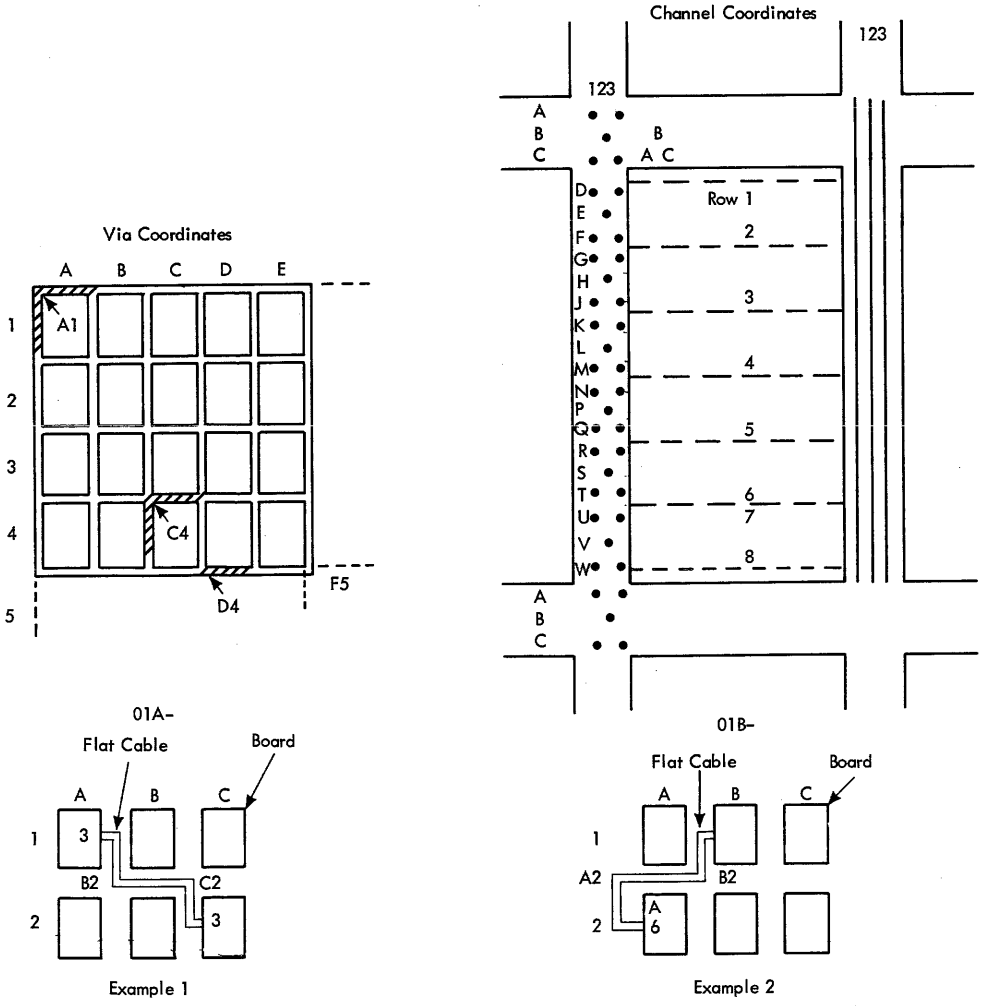


Figure 2-34. Cable Routing

SUFFIXES TO THE BLOCK FUNCTION SYMBOL

The suffix is information added to the block function to clarify the logic usage. Some of the suffixes are:

LT	Transmission line terminator
LD	Transmission line driver
ID	Indicator driver
CD	Core driver
HD	Magnetic head driver
MD	Magnet driver
V	Voltage amplifier
DF	Differential amplifier
FF, FL, PH	Used for emphasis of storage type blocks when these blocks are in multiple block form.
OR, A, WL	Used in the identification of blocks whose outputs are connected in the DOT OR or DOT AND arrangement; these suffixes take precedence over all others. When DOT AND or DOT OR takes precedence over a suffix, the suffix is placed in the title area of the block.
P, H, CT	Used with the RY (relay) blocks to indicate coil and contacts.

Some possible uses of the suffix are shown in Figure 2-35.

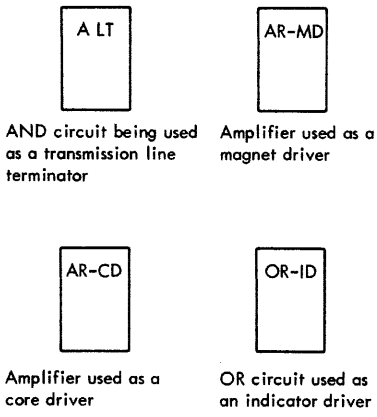


Figure 2-35. Block Suffix Examples

MACRO-LOGIC BLOCKS

Engineering ALD's can contain macro-logic blocks, which are equivalent to butted logic blocks on FEALD's. Macro logic is composed of unit logic (AND/OR/FF) in various combinations to depict multiple logical functions in one macro-logic block. Figure 2-36 shows several examples of macro logic, from simple to complex, and their logical FEALD counterparts. Macro logic has the following characteristics:

1. Input lines are grouped by logical function.
2. Symbols for macro logic are the same as for unit logic.
3. Symbols are generally inside macro-logic blocks, but may be adjacent to a block. Examples 3 and 4 of Figure 2-36 show input functions OR-AND-OD-OE external to the block.
4. For SLT/SLD, inputs to any one function of a macro block have the same polarity and voltage characteristics.
5. All components of a macro block are on the same replaceable unit (an SLT/SLD card, or MST module).
6. Groups of inputs may be separated by an asterisk (*). Some of the combinations of inputs and outputs and their macro block symbols are shown in Figure 2-37.

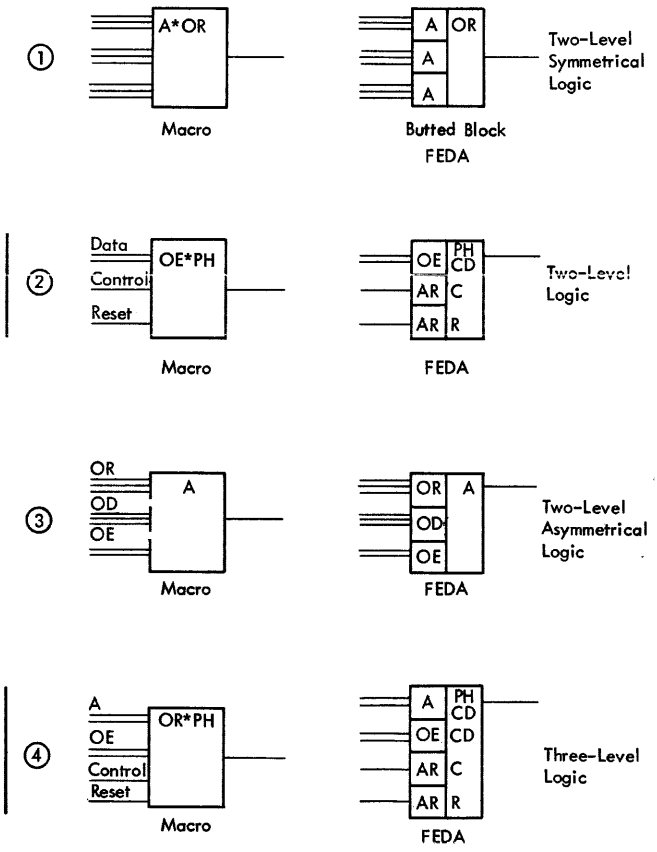


Figure 2-36. Macro-Logic Block Examples

Two-Level Symmetrical Logic:

Input Level	Output Level	Macro Block Symbol
OE OD OR	A	OE*A OD*A OR*A
A OE	OR	A*OR OE*OR
A	OD	A*OD
A OR	OE	A*OE OR*OE
A OE OR	PH	A*PH OE*PH OR*PH
A OE OR	FF or FL	A*FF A*FL OE*FF OE*FL OR*FF OR*FL
A OE OR	SS	A*SS OE*SS OR*SS

Three-Level Logic:

Input Level	Second Level	Output Level	Macro Block Symbol
*	OR OE	A	OR*A OE*A
*	A OE	OR	A*OR OE*OR
*	OR A OE	PH	OR*PH A*PH OE*PH
*	A OR OE	FF or FL	A*FF A*FL OR*FF OR*FL OE*FF OE*FL
*	A OR OE	SS	A*SS OR*SS OE*SS

*Any of the following basic functions: A, OR, AR, or OE.

Two-level non-symmetrical logic:

Input Level	Output Level	Macro Block Symbol
* * * * OD OD	A OR OD OE PH SS	A OR OD OE PH SS

*Any of the following basic functions: A, OR, AR, OE, or OD.

Figure 2-37. Macro-Logic Block Functions

FEALD LOGIC TYPES

An FEALD can contain the various types of logic described earlier in this chapter: unit logic, butted logic, and component blocks. In addition, an FEALD can contain functional logic blocks, such as the selector, register, decoder, and multiregister. These, and other, functional logic blocks permit a greater amount of logic to be shown on an FEALD page than is shown on an engineering ALD page.

On an FEALD, the storage blocks (FF, FL, PH) have their inputs identified by letters appearing inside the block. The following text discusses items unique to logic blocks appearing on an FEALD.

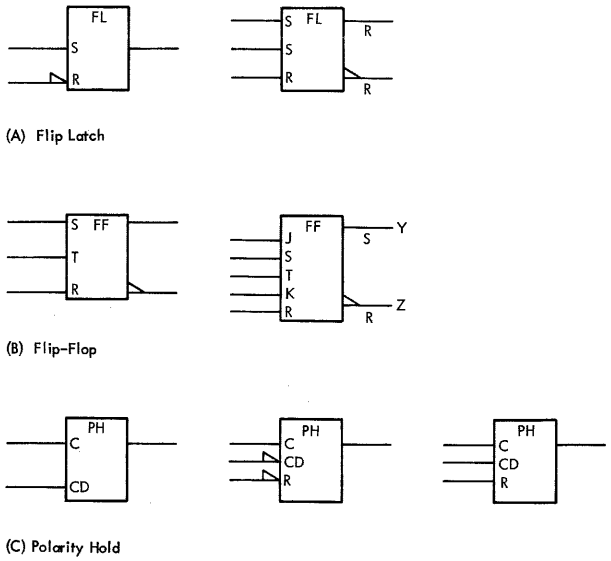


Figure 2-38. Inputs to Storage Blocks

Storage Blocks (FEALD)

Inputs to storage blocks are identified by letters inside the block, adjacent to each input.

S	Set
R	Reset
J	Set (Complement)
K	Reset (Complement)
T	Complement
C	Control
CD	Controlled Data
⌝	Trailing Edge Symbol

Figure 2-38 shows several combinations of inputs as they appear in FF, FL, and PH blocks. These inputs are defined as follows:

S Set: When set is active, all outputs are at their indicated polarity.

R Reset: When reset is active, all outputs are at a polarity opposite to that indicated.

J Set: Acts like a set input, except that simultaneous application of J and K inputs will complement the outputs.

K Reset: Acts like reset, except in combination with a J input.

T Complement: The T input complements each output.

C Control: When active, the control input permits the output to change with changes to the data input line. When inactive, the control line holds the output at whatever polarity it possessed at the moment the control line went inactive.

CD Controlled Data: When the associated control input is at its indicated polarity, a CD input at its indicated polarity sets the storage element. Likewise, a CD input at an opposite polarity resets the storage element, when a control input is active. When a storage element has multiple CD inputs, any active CD input can set the element.

⌝: The trailing-edge symbol indicates that the output of a storage device assumes its indicated polarity on the trailing edge of some input, the trailing edge being a transition of the input to a polarity opposite to that shown. The trailing-edge symbol, prefixed by a line label of the dependent input, is located inside the logic block adjacent to the output.

Flip Latch (FL)

The flip latch has only inputs S and R (example A, Figure 2-38). When the set input is active, all outputs are at their indicated polarity. When the reset input is active, all outputs are at a polarity opposite to that indicated. Generally, the outputs are unknown if the set and reset inputs are applied simultaneously. However, if the outputs can be determined for simultaneous set-reset, an S or R below an output indicates its condition, either set or reset.

Multiple set (or reset) inputs are considered to be ORed.

Flip-Flop (FF)

A flip-flop can have five types (S, R, J, K, and T) of inputs or multiples of them, in different combinations (example B, Figure 2-38). Inputs J and K act like inputs S and R, respectively, in the flip latch, except that simultaneous application of a J set and K reset will complement the output. The T input complements each output. In the FF

example, a simultaneous S-R (set-reset) input causes output Y to follow the set (+) and output Z to follow the reset (+). If any other inputs are active during simultaneous S-R input, the outputs are undefined.

Master-Slave Flip-Flop: This flip-flop is one of the storage devices that uses the trailing-edge symbol. Figure 2-39 shows that the output goes active (FF in 1 state) on the trailing edge of the dependent pulse, or line.

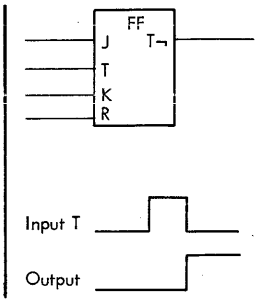


Figure 2-39. Master-Slave Flip-Flop

Polarity Hold (PH)

A polarity hold block (example C, Figure 2-38) must have a control (C) input and a controlled data (CD) input. This block may have a set (S) and a reset (R) input.

Butted Logic

Butted logic on an FEALD replaces macro logic on an engineering ALD. Restrictions are the same; there shall be no card I/O pins between the butted blocks and all blocks shall be on the same card. In addition to AND-OR logic, blocks such as the FF, FL, PH, OE, OD, and EV can be butted.

Functional Logic Blocks

One purpose of the FEALD generation program is to combine unit logic, as seen on the engineering ALD, into functional logic blocks, in order to place more logic on a given FEALD page. Any unit logic can be combined into functional logic blocks, where card I/O pins are available in the unit logic. Functional logic blocks include the following: selector (SEL), register (REG), decoder (DCD), matrix (MTX), multiregister (MREG), and delay (DLY).

Selector

A selector (SEL) (Figure 2-40) is a switching device, composed of unit logic, and contains an upper common section (with gating lines) and a lower data section, separated by a narrow neck. In the common section, a gating line can be a gate-in or a gate-out. The digits 1, 2, and 3 correspond to those dependent lines in the data section that require a gate.

In the example, output line X is active when:

1. Line R (G3) is active, and
2. Lines A and P or lines B and Q are active.

The diamond (◇) is considered to be an OR function. Output lines Y and Z are activated in a similar manner:

Y = C, P, and R, or
Y = D, Q, and R.
Z = E, P, and R, or
Z = F, Q, and R.

Register

A register (REG) (Figure 2-41) is a storage device composed of AND-OR logic or other storage blocks (FF, FL, and PH). Like a selector, the register has a common section and a data section. Inputs can be S, R, T, C, and CD. Gates can be gate-in and gate-out. Registers in Figure 2-41 are composed of unit logic:

Example A shows four FL blocks with a common reset.

Example B shows four PH blocks with a common control line.

Example C shows four FF blocks with a common reset.

Example D shows a register with gate. The G1 gate-in line is needed to set bits into the register (upper set of inputs); ORed with each of these inputs (by a diamond) is an ungated input. The G2 gate-out line is necessary to produce an output.

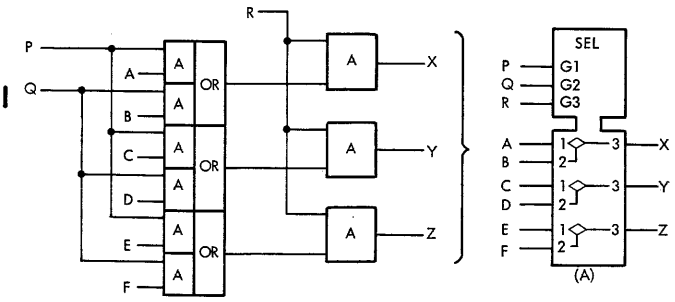


Figure 2-40. Functional Logic Block–Selector

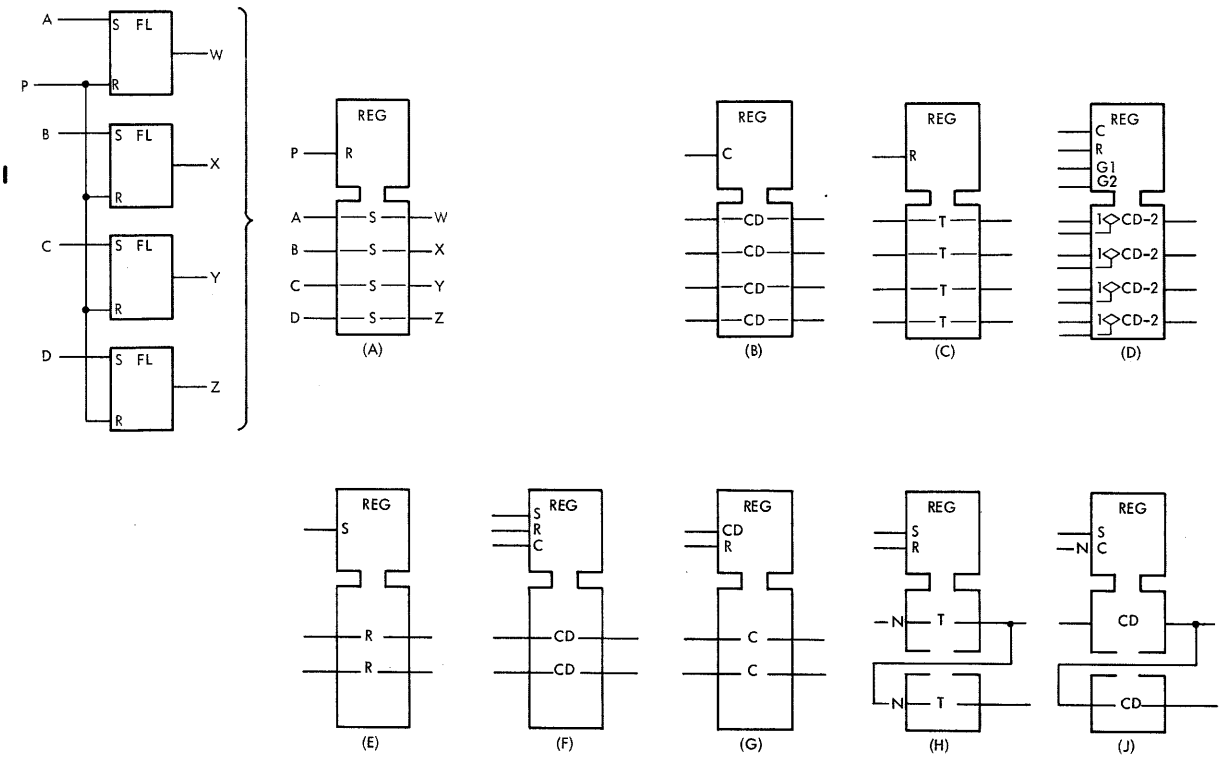


Figure 2-41. Functional Logic Block–Register

Example E shows a set line common to two positions.

Example F shows two data positions capable of being set or reset by a single S or R input.

Example G shows a data line common to more than one control input; whatever data is available at CD is stored into a position when the appropriate C input is active.

Example H shows a multiposition register in which the state of a position depends on the data stored in the previous position. In the example, each position can be set or reset by the common S or R line. Whenever a negative shift appears at the input to the first position, the position complements; the second position, likewise, complements only if the first position changes from plus to minus.

Example J is similar to H except that CD lines appear in the data section. At any time, the data available to the first position is stored in that position (and reflected at its output) when the control line shifts negatively. All remaining positions of the register store the data available at the immediately previous position. *Note:* The N external to the block indicates that a negative pulse or shift activates the control line (nonstandard).

Decoder

A decoder (DCD) (Figure 2-42) translates a group of related inputs into a specific output. Most decoders do not have a

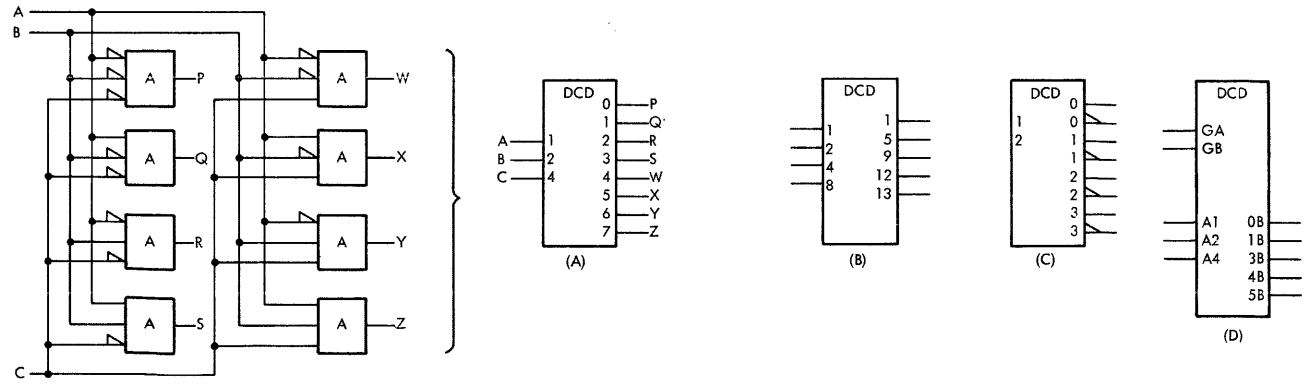


Figure 2-42. Functional Logic Block–Decoder

common section. Inputs are numbered in binary progression: 1, 2, 4, 8, 16, and so on. The output equals the sum of the active inputs. Only one output can be active at any given time, depending on the sum of the inputs. In example A, output 0 is active if no input is active; output 7 is active if all inputs are active.

Not all output sums need be used. In example B, input 2 is not required and, if active, makes all outputs inactive.

Example C shows that multiple output lines can be associated with a given output (sum).

Example D shows a decoder with gating. Note that letters are used to prevent ambiguity among gated lines.

Matrix (MTX)

A matrix block is analogous to a core array in that (AND-circuit) elements can be addressed by "intersecting" input lines (Figure 2-43). Each AND block in the figure is addressed by a specific X input and Y input. For an output to be active, at least one line in each input group must be active. If more than one input is active in a given group, a double address occurs, which may or may not be an error, depending upon the application.

The lower matrix block has three input groups. Here, output 10 is active if inputs X-1, Y-3, and Z-6 are active.

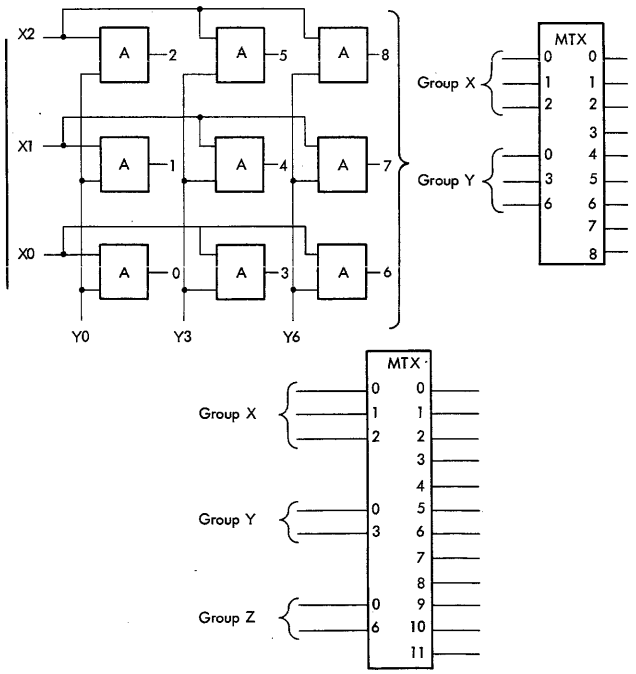


Figure 2-43. Functional Logic Block–Matrix

Line Bundling

Line bundling is a method for depicting the many outputs commonly associated with decoder and matrix blocks. Bundled lines represent many consecutively labeled lines of the same polarity that are not connected to card I/O pins. Rather than show many outputs, a range of outputs can be indicated as in Figure 2-44. The 16 outputs of the decoder block are indicated as a 00 to 15 range. The matrix block in the figure has 192 outputs, ranging from 000 to 191. In this case, the maximum input to the matrix (128 + 48 + 15) matches the 192-output capacity of the matrix block, but this need not be true. The capacity of a block is always indicated at its output, irrespective of the number of inputs.

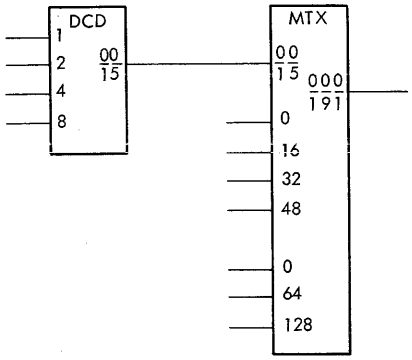


Figure 2-44. Line Bundling

Multiregister (MREG)

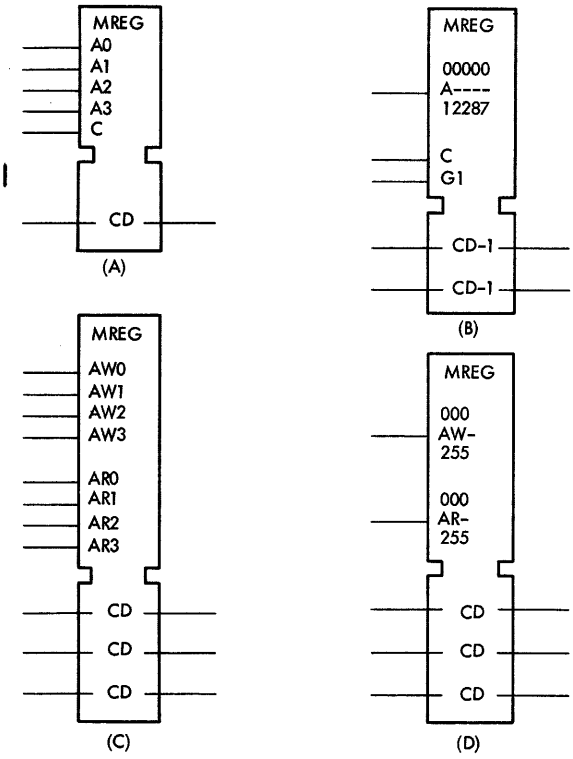
The multiregister block represents two or more registers having a common data line. Example A in Figure 2-45 represents four registers where data available on the CD line can be set into any or all of the four registers controlled by lines A0 through A3, and control line C.

Example B combines bundling with a multiregister to depict a 12k by 2-position storage device. An active control line permits data to enter the multiregister on the CD line; an active gate-out line permits data in the register to be available as output. However, to select a particular register in the MREG, an address line from 00000 to 12287 must also be active. The data written into the register is that data available on the CD line when the address and control lines are active. Data read out is not dependent upon the control line.

A multiregister can contain two sets of addresses, AWn for write and ARn for read, as in example C. Example D shows a multiregister with bundled read/write addresses.

Delay (DLY)

In a delay block on an FEALD (Figure 2-46), delay is measured in terms of the delay caused by a given number of logic blocks. In the example, after input X is active, output Y becomes active after a delay equivalent to four blocks. A delay block can account for the removal of logically unnecessary amplifier or inverter blocks during the generation of an FEALD. The FEALD program may remove a single nonlogical block without inserting a delay block in its place. The lower example shows another form of delay block.



Example	Input Lines Needed	Output Lines Needed
A	A(0,1,2,3) C CD	A(0,1,2,3) CD (data)
B	A(0-12287) C CD-1	A(0-12287) G1 (gate) CD-1 (data)
C	AW(0,1,2,3) CD	AR(0,1,2,3) CD (data)
D	AW(0-255) CD	AR(0-255) CD (data)

Figure 2-45. Functional Logic Block–Multiregister

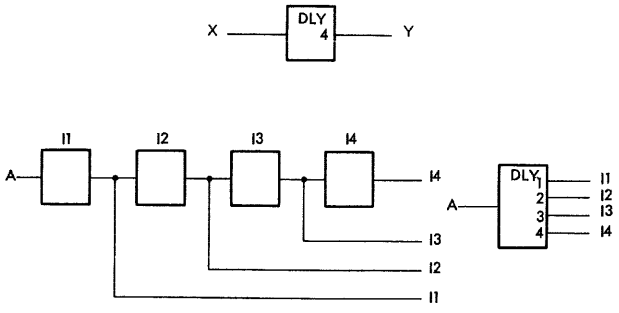
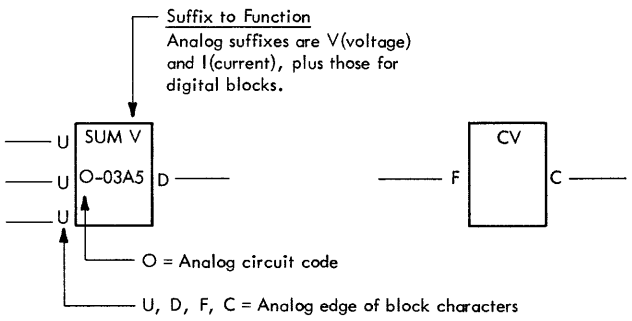


Figure 2-46. Functional Logic Block–Delay

ANALOG LOGIC BLOCKS

Digital logic conveys information by a device assuming a limited number of discrete states, usually two. Analog logic conveys information through signals that vary in amplitude, frequency, phase, or compound frequency throughout a continuous operating range or time period. A logic diagram can contain analog circuits intermixed with digital circuits.

An analog logic block is distinguished from a digital block by having the circuit number code of O, by having different edge-of-block characters (U, D, F, C in Figure 2-47), and by having logical functions unique to analog circuits. The block suffixes V, for voltage, and I, for current, can clarify the function of an analog block. In addition, explanatory titles and notes often clarify analog functions.



Note: An ALD line entering a page at an analog block has the following format: a C, F, U, or D; line title; and line type (voltage or current information).

Figure 2-47. Analog Logic Block

Edge of Block Character

Analog logic blocks are identified by the four edge-of-block characters: U, D, F, and C.

U (Up): A voltage mode or current mode signal that performs its function as the voltage changes toward positive (voltage mode) or as the magnitude of the current increases (current mode).

D (Down): A signal that performs its function as the voltage changes toward negative (voltage mode) or as the magnitude of the current decreases (current mode).

Note: For a steady state analog signal, the U or D refers to the relative polarity of the signal compared to the no-signal state. If the edge-of-block character is insignificant, the U is used. Signal inversion is indicated by the use of U-D or D-U as in Figure 2-48.

F (Frequency): A radio-frequency or audio-frequency signal that conveys information by the combined effect of many individual oscillations. The F character is limited to

the logical functions AND, OR, CV, FLTR, MIX, DET, and AR. An F signal, if combined with the amplitude of another signal, is converted to a U or D signal. Where two F signals are combined and result in a frequency-mode output, a special (SPEC) block with an appropriate title describes the resulting function.

C: Indicates the presence of short pulses produced through a sampling technique that is applied at intervals to an analog signal (Figure 2-49).

Figures 2-50 through 2-64 illustrate and define the analog logic blocks: integrator, differentiator, analog OR, sum, amplitude hold, filter, function generator, mixer, detector, rectifier, comparator, analog-digital-AND, analog-digital-OR, and differential amplifier.

Digital-Analog Blocks

Other logic blocks that may operate with analog signals include the linear or nonlinear amplifier, signal mode converter, limiter, Schmitt trigger, series current switch, and special block (Figure 2-64). The function of a special block is described in the block title area or in the comments area of a logic diagram. When used with analog signals, the signal mode converter has a single input with its mode converted or translated, such as from frequency variation to amplitude variation.

Figure 2-48. Analog Inversion

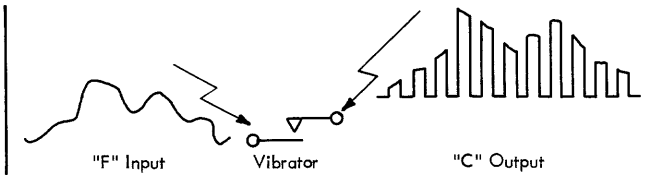
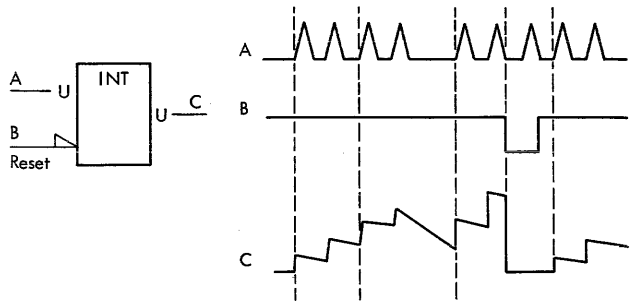
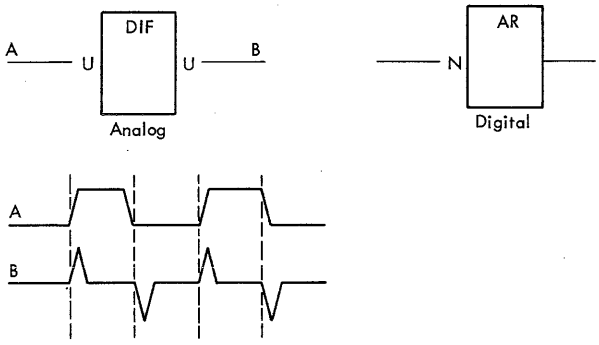


Figure 2-49. C Type Output



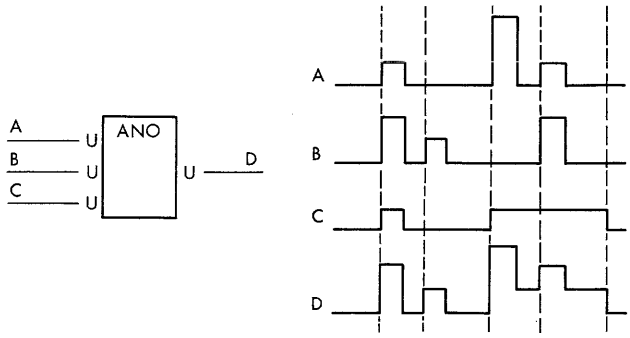
The amplitude of the output of an integrator is a time integral of the input signal amplitude. A signal of the indicated polarity at the (binary) reset input causes the output amplitude to assume a no-signal level.

Figure 2-50. Integrator



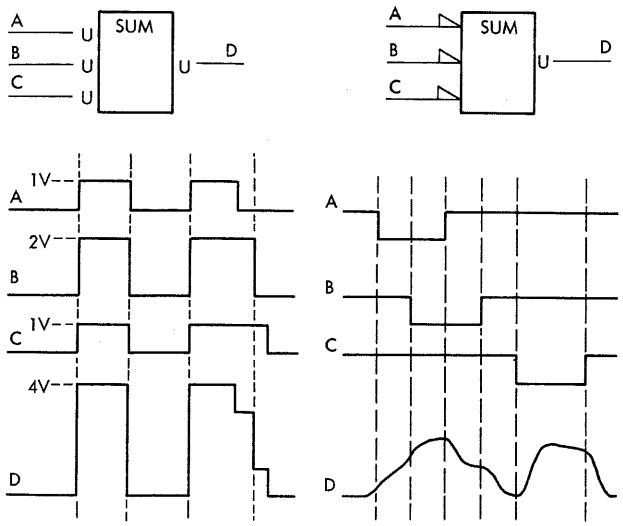
The output amplitude of a differentiator is a function of the time-rate of change of the input. In digital logic, the result of differentiation is shown by a P or N at the input of a block.

Figure 2-51. Differentiator



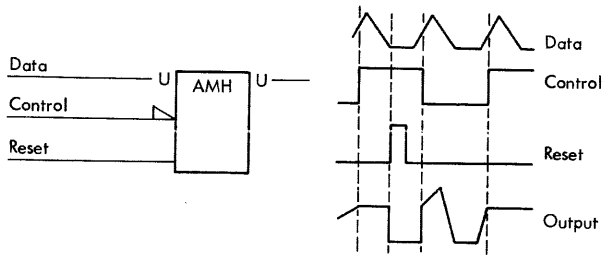
The output amplitude of an analog OR block is a value corresponding to the greatest input amplitude, in the direction shown by the U or D character. Output mode may be indicated by an I or V.

Figure 2-52. Analog OR



The output amplitude of an analog sum block is a value corresponding to the algebraic sum of the weighted values of the inputs. The analog output has an appropriate U or D character.

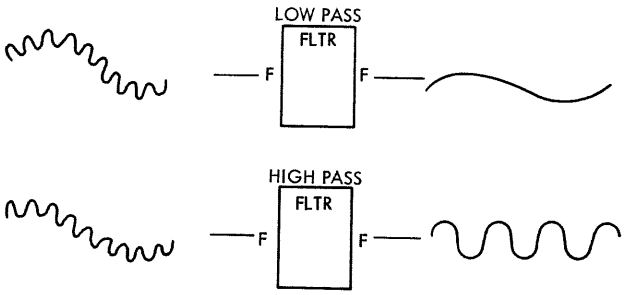
Figure 2-53. Sum



When the control input is at its indicated polarity, the output of an amplitude hold block is at an amplitude corresponding to that of the data input line. When, subsequently, the control input goes to an opposite polarity, the output holds at whatever amplitude it possessed at that moment.

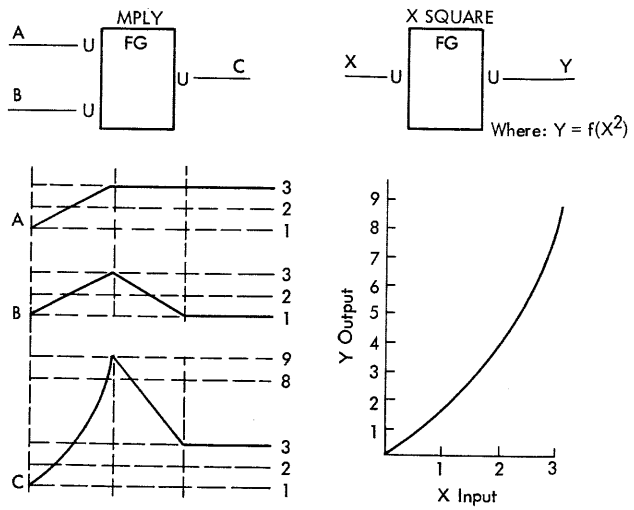
Control and reset are binary signals. If an amplitude hold block has a reset input, then the indicated polarity causes the output to go to a no-signal level.

Figure 2-54. Amplitude Hold



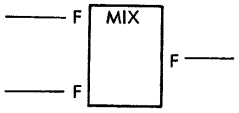
Except for amplitude variations resulting from the frequency response characteristics of the filter, the output of a filter corresponds to the input. Where bandpass action, wide or narrow, is accompanied by amplification, an AR symbol and block title, such as low pass or high pass is shown.

Figure 2-55. Filter



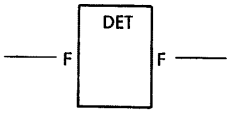
The output amplitude of a function generator is a value that is a mathematical function of the input values. The block title describes the function. Inputs and outputs are U- or D-type analog signals.

Figure 2-56. Function Generator



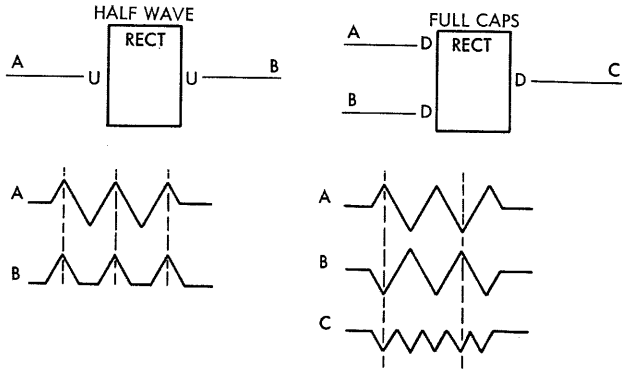
The output of a mixer is an F-type signal that contains the sum and difference frequencies of two inputs. The block title defines the output frequency if filtering occurs in the circuit.

Figure 2-57. Mixer



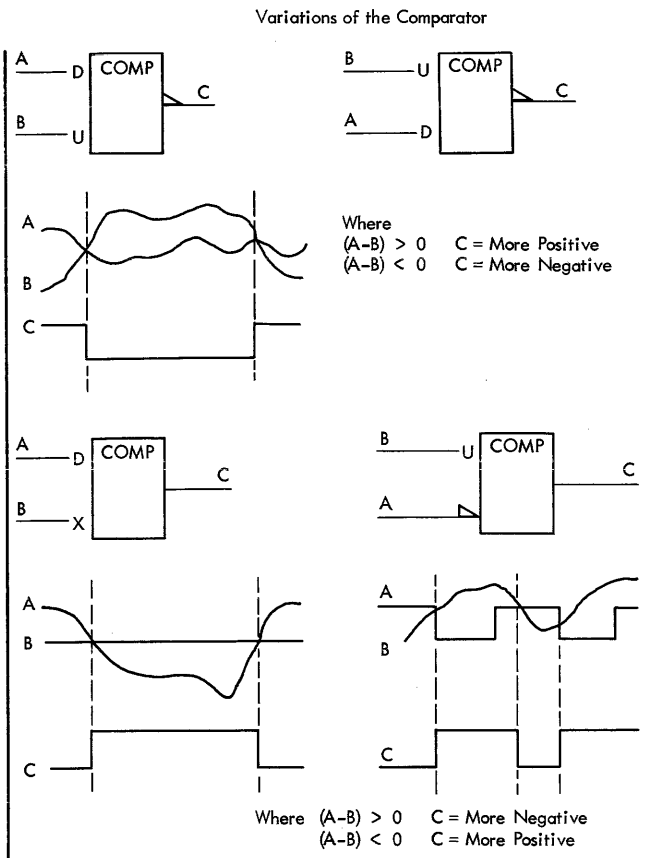
The detector is a circuit that acts upon F-type signals to recover a carried signal of lower frequency, such as an audio signal.

Figure 2-58. Detector



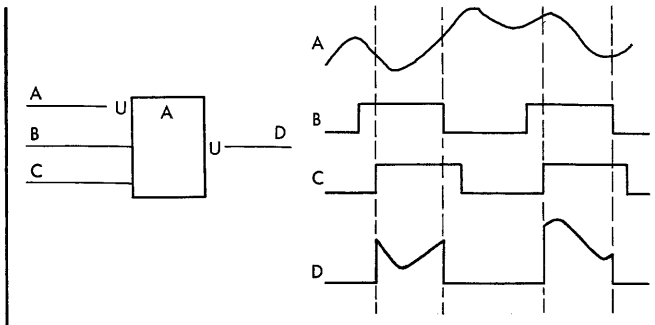
The output amplitude of a rectifier corresponds, at any point in time, to that input whose amplitude exceeds a reference level in the direction indicated.

Figure 2-59. Rectifier



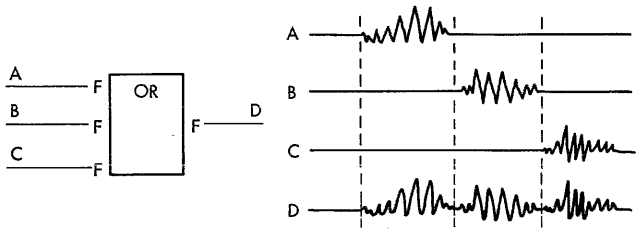
The output of a comparator is at its indicated polarity when either input reaches or exceeds (in the direction shown by the U or D) the voltage existing on the other input. A comparator has a digital output.

Figure 2-60. Comparator



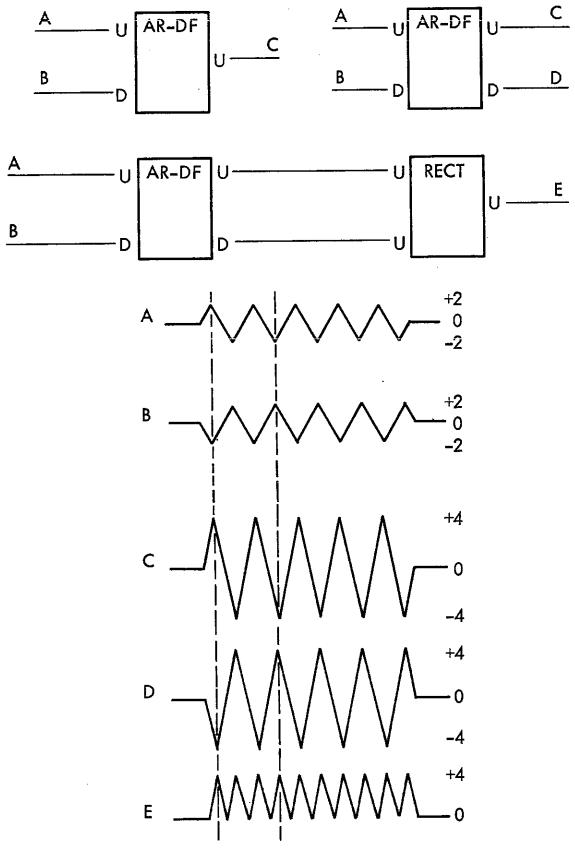
The analog output of this AND block corresponds to the analog input when all digital inputs are at their indicated polarities. At other times, the output is at a no-signal level.

Figure 2-61. Digital-Analog-AND



When used with analog inputs, the output of a digital-OR block corresponds to the particular analog input that is active at the time. The output is not meaningful if more than one input is active simultaneously.

Figure 2-62. Digital-Analog-OR



The output of a differential amplifier is a signal that corresponds to the signed difference in voltage between two input signals. The output shifts toward the indicated polarity when either input exceeds (in the direction shown by its polarity indicator) the voltage at the other input.

Figure 2-63. Differential Amplifier

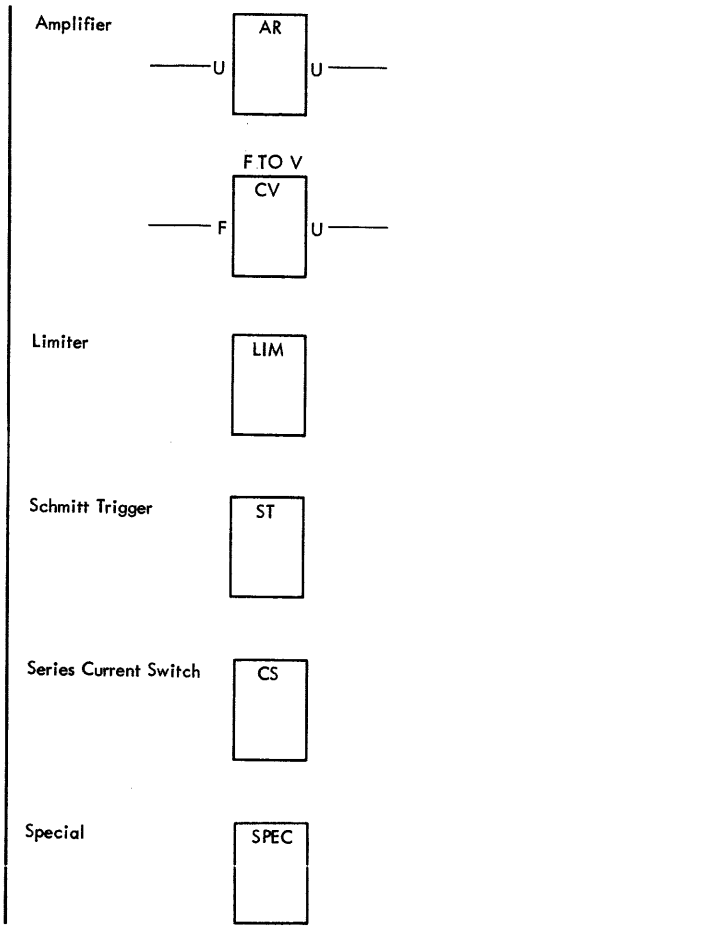


Figure 2-64. Other Analog Blocks

- ALD's are computer-generated logic diagrams of IBM products.
- ALD's use the same logic symbols and page formats for all technologies.
- ALD's include the engineering ALD, the card ALD, and the field engineering ALD (FEALD).
- This chapter describes the content and format of the engineering ALD.

Computer-automated design helps engineers check designs and connect individual circuit sections involving hundreds of thousands of electrical connections, components, cables, and other items. The computer maintains an interim magnetic tape record of circuits as they are developed and produces the final tape used in an automatic system to make new circuit patterns.

The design automation program is used to:

1. Assist the engineer to simulate logical designs and verify circuit loading before the designs are committed to manufacturing.
2. Compute cable length requirements for different interconnections.
3. Assist the engineer in assigning the logical elements to boards and cards, and in locating printed wiring on boards.
4. Document on magnetic tape the logical design of computers, determining the layout of printed boards and cards.
5. Print the ALD's.
6. Provide a monitoring service to help engineering and manufacturing groups coordinate their activites.

The SLT design automation program accepts various forms of information from design engineers and processes it into machine logic. Design automation gives the engineer the option of using the computer to package a logic design or to check manual packaging. In addition, it allows him to treat a portion of a system as a unit for simulation, packaging, or design modification.

Simulation and circuit load checking programs verify logic designs recorded on a logic master tape. Packaging programs, which pertain to card selection, card-to-board assignments, pin locations, and card placement, assist in mapping logic circuits into the circuit cards. The computer also aids integration of cable design and installation data with cable manufacturing data.

After the computer determines the connections and designs the board wiring, it records the printed connections on a master tape. This tape is later used to produce other tapes containing circuit board design data.

The basic document produced by design automation is the Automated Logic Diagram (ALD), a computer-drawn schematic representation of machine functions. The ALD is an 11 x 17 inch sheet. See Figures 3-3 and 3-4 for an overall view of engineering ALD's.

On an ALD, circuits are represented by rectangular blocks, which symbolize logical functions. They are connected by printed lines, which symbolize electrical connections. Inputs enter the circuits on the left; outputs leave at the right. Most of the page is used for the representation of logic; page identification and supplemental information appear at the bottom of the sheet.

Engineering ALD's

PAGE NUMBER

The page number is located in three places on the sheet. The page number in Figure 3-3 is KH142. In this illustration, the page number is in the upper right corner, as well as in both the lower right and the lower left corners.

Logic pages are numbered according to a coded prefix consisting of two alphabetic symbols, representing the major and the minor characters. The general coding scheme is shown in Figure 2-1.

For example, the coding for the A-register is RA. "R" is the major character; it means register. "A" is the minor character, designating the particular register. Another example is KR101, which means control (K), check triggers (R), page 101.

Figure 2-1 is CPU-oriented. Slight variations appear both in the CPU pages and in the I/O pages.

MACHINE VERSION

A version page (Figure 3-2) shows wiring and cards that are not on the basic machine. This wiring must be added to that used in the basic machine. This is in direct contrast to the additive card code, in which the wiring is part of the basic machine, and only cards are added to make the feature operative. An example of a version page is a page that adds the cards and wiring for the floating-point feature.

A version page is made up of all basic page blocks which are unchanged in the version design plus additional blocks (version blocks) needed to change the basic page into a version page.

The machine version number appears below the page number; for a basic (standard) machine, this number is 000. A version page assigned by design automation has a number other than 000.

The version page number is placed on the top line of those blocks that are added by the version. An example of machine version "041" is shown by the shaded blocks in Figure 3-2.

Adders	
Addressing Adder	AA-AB
IC Incrementer	AC-AD
Exponent Adder	AE-AF
Main Adder	AM-AQ
Serial Adder	AS
VFL and Decimal Adder	AV-AW
Busing (Excluding Storage Bus)	BA-BZ
Consoles	PA-PE, PJ-PZ
1052 Console Adapter	PF, PG, PH
Controls	
Advance or Seq Controls	KA
Branch and IC Controls	KB
Clock Controls	KC
I-Execute, I-Fetch, and Execute	KD
Chan Controls	KE
Fixed Sequence Controls	KF
General Register Controls	KG
FLT Controls	KH
ROS Controls	KK
Local Storage Controls	KL
Priority and Interrupt Controls	KM
I/O Instruction Controls	KN
VFL Controls	KP
VFL Controls	KQ
Check Triggers	KR
Status Triggers	KS
VFL Controls and Decimal Controls	KY
Any Miscellaneous Controls such as FP Fixed Point, Storage Protect, Real Time Clock, Status Controls	KT-KU KW-KZ
Counters	
Instruction Counters	CA-CB
Local Storage Address Counter	CC-CD
Miscellaneous Counters	CE-CZ
Hardware-Oriented Pages	ZA-ZZ
CROS	ED-EF
Decoders	
Op Decoders	DN
FLP and Generator Decoder	DP
Addressing and Pre-Fetch	DA
Trap Decoder	DB
Register Decoder	DG
ROS Decoder	DR-DS
I/O Channels	
Multiplexer Channel	FA-FZ
Selector Channel 1	GA-GZ
Selector Channel 2	HA-HZ
Direct Data	JA-JZ
Local Storage	LS-LT
Main Storage Registers and Controls in CPU (Includes SDR Registers, Storage Buses, SAR, SBI, OR, M and N Registers	MA-MC
Power Supplies	YA-YZ
Registers	
A-Register	RA
B-Register	RB
D-Register	RD
E-Register	RE
F-Register	RF
G-Register	RG
H-Register	RH
J-Register	RJ
K-Register	RK
L-Register	RL
M-Register	RM
N-Register	RN
P-Register	RP
Q-Register	RQ
R-Register	RR
S-Register	RS
T-Register	RT
U-Register	RU
V-Register	RV
W-Register	RW
X-Register	RX
VFL and Decoder Register	RY
Direct Data Register	RZ
ROS Flowcharts	QA-QZ
Special Features	XA-XZ
TROS	EA-EC

Figure 3-1. ALD Page Number Prefixes

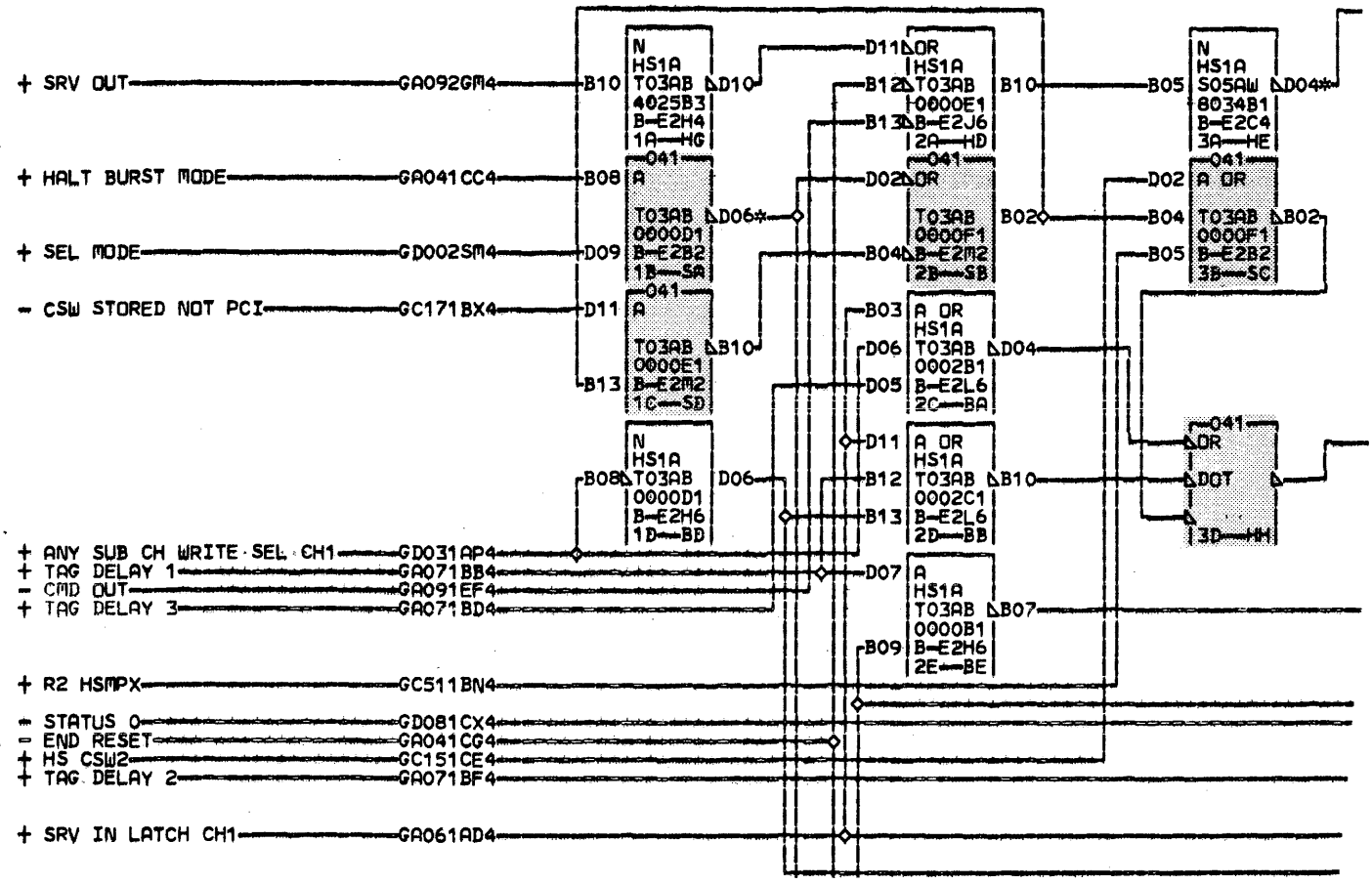


Figure 3-2. Example of Version Blocks

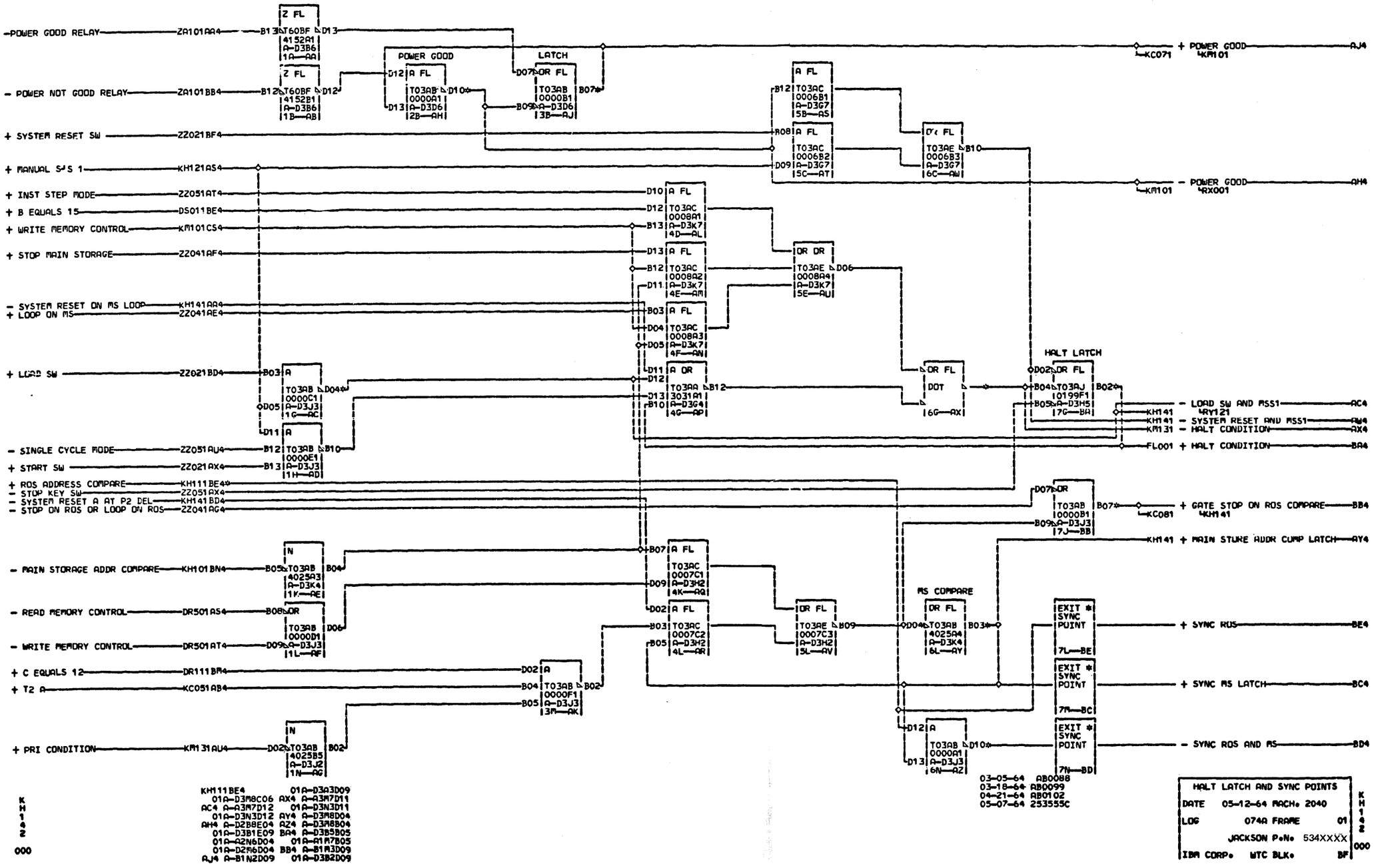


Figure 3-3. Automated Logic Diagram (ALD)

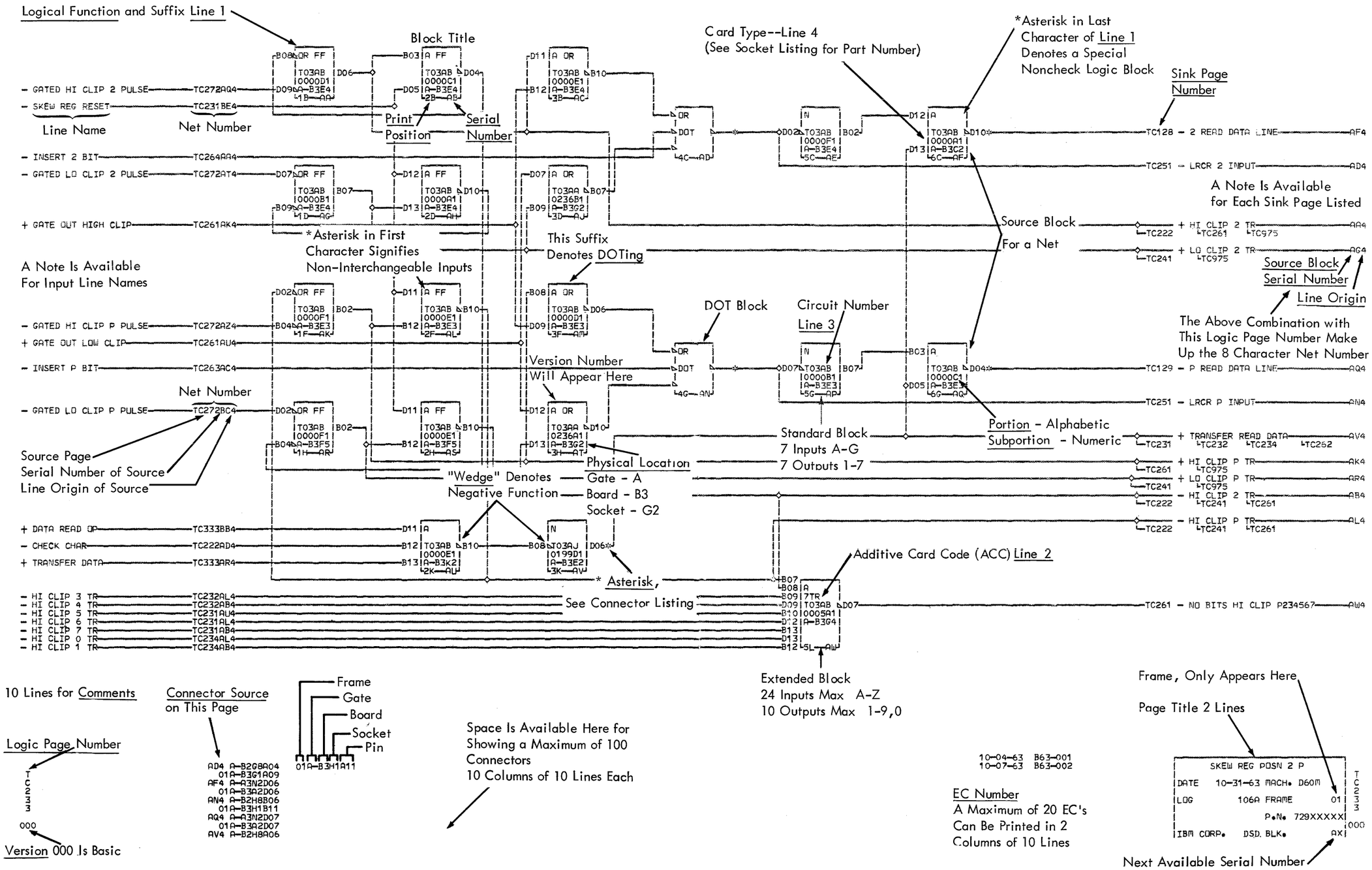


Figure 3-4. Annotated ALD Page

TITLE BLOCK

The title block is printed in the lower right corner of the page. As Figure 3-5 shows, information can be found at three places in the block:

1. At the top
   a. The page (sheet) title ("LS Address Register J Bits 0 thru 3" in Figure 3-5).
2. On the left side
   a. Date of processing by design automation (05-12-64).
   b. Log number (or computer run), "074A," assigned by design automation.
   c. The corporate division, WTC (World Trade Corporation).
3. On the right side
   a. Machine type, "2040." This may be a pseudo number or it may be the machine number followed by a suffix. The suffix differentiates between models or features of the machine number.
   b. Frame, "01"; within the machine, may be 01 to 63.
   c. Part number of the page, "534XXXX."
   d. Block DF is, in terms of design automation, the next block serial number available for use on that page.

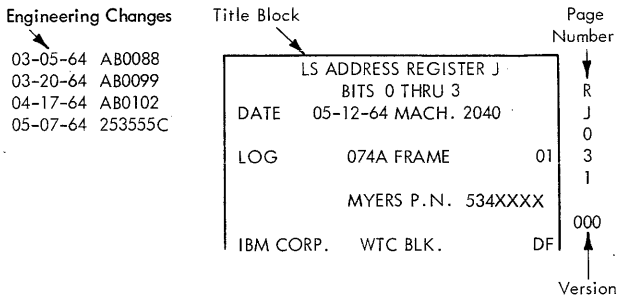


Figure 3-5. Example of Title Block Area

LOGIC BLOCK

Logic blocks shown in Figure 3-6 are positioned on the page in a matrix 7 columns wide and 13 rows high. The columns are numbered 1 through 7. Rows are lettered A through N, excluding I.

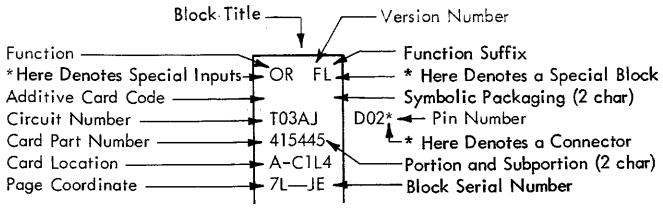


Figure 3-6. ALD Logic Block

A logic block is 6 increments wide by 7 increments high; it may be lengthened downward to a maximum of 24 increments. The block may have 1 to 7 input and/or output lines on the basic block; 1 to 24 input and/or 1 to 10 output lines on the extended block.

Information Inside the Block

Line 1

The logical function being performed by the circuit represented appears on line 1 such as A, OR, N, or FF. An asterisk (*) preceding the logic function symbol means to design automation that the input line positions are placed in a certain arrangement; that is, the pin numbers and position of the input lines are fixed by the physical makeup of the components used.

The suffix, preceded by a space and following the function, is additional information describing the function. The suffix indicates DOT functions such as A OR, OR A, N OR, or OR WL; to indicate the blocks in a multiblock configuration of bi-stable circuits such as A FF, OR FF, A PH, OR PH, or N PH; and to indicate additional information in special component blocks such as RY CT, RY P, or A LT.

An asterisk (*) following the suffix and/or in position 6 indicates a special block that does not follow the rules of design automation. Some of the special blocks are exit and entry, service-voltage logic, switch, and jack blocks, as well as discrete components such as capacitors or resistors.

Line 2

The additive card code (special machine feature) appears on line 2 in the first four characters; for example, 7TR (seven-track tape feature). Additive card codes identify those logic blocks which pertain to a special class of machine features in which the feature can be installed by plugging in the feature cards.

The last two characters of line 2 contain the symbolic package designation. The use of these two characters allows design automation to generate the ALD's, to position the card on the board, and to generate the wiring (printed or discrete) on the board. Blocks with the same characters in the symbolic package field are placed on the same board by the card partitioning program used by design automation.

Note: Blocks with different symbolic packages may be placed on the same board.

Line 3

The circuit number (Figure 3-7) appears on line 3, except when design automation generates a pseudo block for a DOT function. In this case, DOT appears on line 3. A DOT block is a tie-point for the output of two or more circuits which provide input for one circuit.

The circuit number is the coded name given to a particular circuit. The number is defined in Figure 3-7. It is used to understand the logic and to identify particular components on the logic card.

Line 4

The first four positions of line 4 are the card code. These four digits refer to the part number of the card as indicated in the plug/socket listing. (See "Connector and Resistor Listing" and "Socket Listing.")

The last two characters on line 4 represent the portion and subportion. A portion represents an independent section of a card. A section may be represented by one or more logic blocks; each block has a subportion number. The portion character has the form A, B, . . . Z (excluding I, O, and R). ALD blocks which are interconnected on a card are in the same portion. Every block in a portion has a unique subportion number. These subportion numbers are assigned in the sequence 1, 2 . . .9, A, B, . . . Z (excluding I, O, and R).

Exception: When a circuit with an unloaded collector and an associated load resistor packaged on the same card are used together, the block designating the load resistor has the same portion as the unloaded circuit, and the subportion character is R.

Line 5

The card location is placed on line 5:

1. Character 1 is the gate (A through Z), followed by a dash.
2. Characters 3 and 4 are the board location, one alphabetic and one numeric.
3. Characters 5 and 6 are the card location, one alphabetic and one numeric.

Bottom Line

The print location in positions 1 and 2 of the bottom line (generally line 6) is made up of the grid coordinates of the block and the ALD page; for example, 1B, 3F. The serial number of the logic block appears in positions 5 and 6, and is expressed in alphabetic characters. Serial numbers begin with AA and proceed in a sequential order (AA, AB, AC, . . . ZZ). Serial numbers AA through RZ refer to the basic system group, and numbers SA through ZZ refer to the special engineering group.

An engineering change (EC) may add logic blocks; in this case, the sequence of double alphabetic characters is continued. An EC may move a block to another print location, but the serial number for that block remains the same. If an EC eliminates a block, that serial number does not appear again on that page. The block serial number is an integral part of the net number. (See the "Glossary.")

Circuit Number Code -- General Forms: XNNZZ or XAYZZ

X	Circuit Classification
A or NN	Circuit Type
Y	Circuit Origin
ZZ	Circuit Number

X--Circuit Classifications

A	MST-2
B	TTL
C	TTL
O	Analog
P	MST General
Q	ASLT
R	SLD 100 ns
S	SRETL General
T	SLT/SLD 30 ns
U	SLT/SLD 5-12 ns
V	SLT/SLD 700 ns
W	Monolithic
X	MST-1
Y	MST-4

A or NN--Circuit Types

A	NN	Circuit Type
A	07	Sense Amplifier
B	55	Indicator Driver
C	61	Component
D	45	Delay Circuit
E	11	Noninverting Logic Driver less than 50 mA
F	20	Trigger, Flip-Flop, Polarity Hold, Schmitt Trigger
H	22	Oscillator
K	16	Magnetic Head and Core Driver
L	03	Logic Circuit and Extender
M	65	Functional Logic Circuit
N	10	Inverting Logic Driver less than 50 mA
P	15	Power Driver more than 50 mA
Q	25	Clip, Clamp, Limiter, Regulator
R	63	Relay
S	21	Singleshot
T	06	Transmission Line Driver, Receiver
U	32	Parity Check, Exclusive OR
V	29	Reference Power Supply
W	40	Special Circuits
X	05	Voltage Translator, Converter
Z	60	Switch Integrator, Filter

Y--Circuit Origins

A	Poughkeepsie	N	Sweden
B	Burlington	P	Austin
C	Poughkeepsie	R	Rochester
D	Holland	S	San Jose
E	Endicott	T	Boca Raton
F	France	U	United Kingdom
G	Germany	V	Boulder
H	Poughkeepsie	W	Italy
J	Japan	X	Lexington
K	Kingston	Y	Fishkill
L	Poughkeepsie	Z	Raleigh

Figure 3-7. Circuit Number Codes

Information Outside the Block

Title

When logic blocks have been assigned a title, the title appears over the block.

Pin Numbers

Pin numbers are in line with the input or output line. They are the actual numbers of the base pins on the card.

Asterisk (*) on an Input or Output Line

An asterisk (*) on an input or output line denotes a connection that leaves the board. The routing is at the bottom of the ALD page, keyed with the serial number of the block and the output line number; for example, AQ4.

Information on the Side of the Block

Wedges

The wedge (◺) is a small triangle at the point where a signal line joins a logic block. The wedge indicates that the active state of this line (the state which satisfies the function of the block to produce an output line of the state indicated) is at the least positive potential with respect to the most positive potential shown by the signal line without a wedge.

A wedge is placed in the edge of the block in line with an input or output line. When the block or circuit is performing its function, the wedge indicates the most negative (least positive) dc voltage for that line.

Note: Signal lines can be at one of two voltages, an up level or a down level. Because circuits operate at different speeds and at different pulse levels (0.0V to +12.0V; +0.9V to 3.0V), the line level designated by the wedge must be described as the most negative (least positive); the absence of the wedge is the most positive (least negative) level of the line.

E in the Side

An E is placed in the side of the block whose inputs are being extended. An example is a circuit that is used to add inputs to another AND or OR circuit; the connection from this second circuit to the first is made at other than a normal input or output of the first circuit. A connection of this type is shown without polarity and is labeled E, extender, (Figure 3-8).

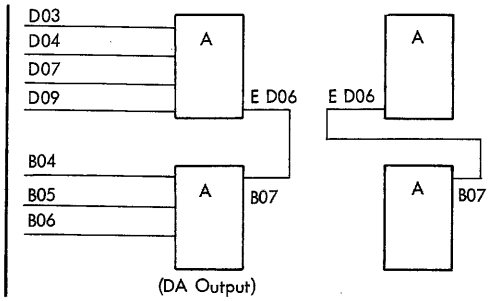


Figure 3-8. Block Expanded, E in the Side

K in the Side

Nonlogic outputs of different blocks are not tied together by DOT blocks. Instead, a K is put in the edge of the block in line with each (except one) of the connected outputs. The one exception is the output used to determine the net number.

Output (or input) lines on the same block may be tied together. In this case, the net number is the position without the K in the edge of the block (Figure 3-9).

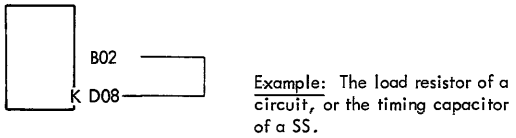


Figure 3-9. Nonlogic Outputs, K in the Side

Nonlogic outputs on different blocks may be tied together when:

1. All the outputs tied together appear on the same page. The net number then includes the line origin of one of the outputs from one block. The commoned outputs are differentiated from the source by a K in the edge of the block position.
2. All the outputs tied together are not on the same page. In this case, the outputs tied together on one page show an output to the right side of that page. The outputs in the same net on other pages return to the left of their respective pages and are referenced to the first page in

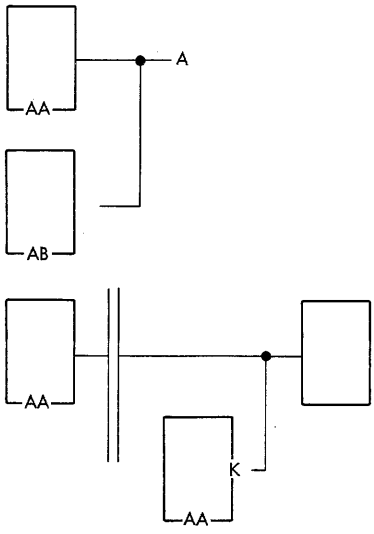


Figure 3-10. Nonlogic Outputs Tied, Example

the normal manner. The net number includes the line origin of one of the commoned outputs on the first page. In the edge of all the other blocks having outputs in the same net, a K appears in line with each commoned output (Figure 3-10).

P or N in the Side

When a capacitive input to a block is designated, a P or N in the side of the block indicates the polarity of the shift necessary to satisfy the function of the block (Figure 3-11).

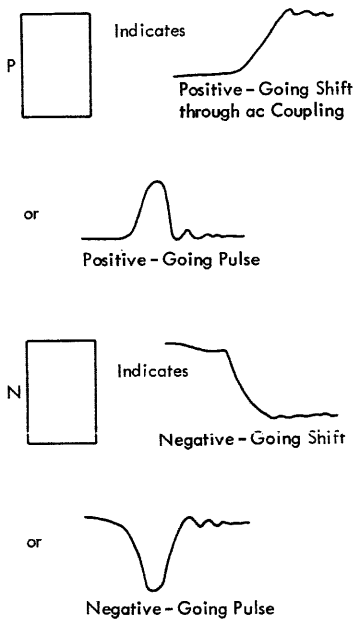


Figure 3-11. Pulsed Blocks, P or N in the Side

X in the Side

Nonlogic connections to a logic block have an "x" in the side at the place where the polarity indicator (wedge) is normally placed. This nonlogic input or output can be a bias line. In Figure 3-12, D06x is a nonlogic connection to the two-way OR block. The nonlogic line is generally a feedthrough line or voltage line.

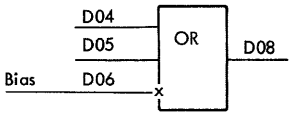


Figure 3-12. Nonlogic Connections, X in the Side

Figure 3-13 shows the use of the "x" in the edge of the block. An "x" appears on lines D05 and J13, showing that these lines are the same. (It is really one ground line that is common to several blocks, and this line completes the ground circuit in these blocks.) At location 1L, lines D13 and G13 are similar to lines D05 and J13, except that a K is at G13 because a net may have only one source. (Other input lines to a net are designed with the K.)

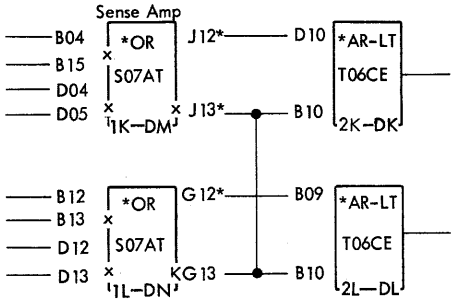


Figure 3-13. X in the Side, Example

LINE NAMES

Input Line

Each input line (Figure 3-4) entering an ALD page has a net number and a line name.

The net number is composed of the source page, the serial number of the source block, and the line origin of the source block. For example, KH141AT4 means that this line came from page KH141, from the block whose serial number is AT on that page, and from the fourth line position on the block. When an input line comes from more than one unit, such as one of many types of I/O devices, or from more than one storage unit, a pseudo-net number is put on the ALD net number position. These pseudo-net numbers are generally in sequence on a page starting at 000.

A net is a set of signal points (a source and sinks) which are electrically interconnected. Generally, the source point refers to the output pin of the driving block, and the sink points refer to the input pins at the driven blocks. The net identification indicates which points (pins) belong to a given network (Figure 3-14).

The line name is generally a description of the line function and is signed plus (+) or minus (–), depending on the active condition of the line at that point. If most of the lines in the machine are plus (+), the sign may not appear unless it is minus (–). An analog line can have a C, F, U, or D identifier instead of a + (plus) or – (minus) sign.

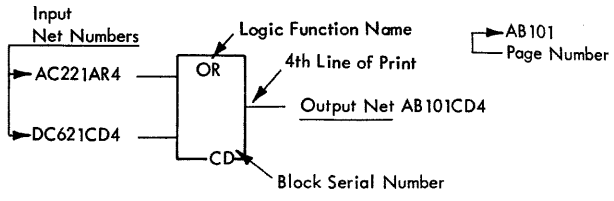


Figure 3-14. Net Identification

Output Line

On each output line (Figure 3-4) leaving the ALD page, the sink page number (where the line is going), the line name (with the sign of the active state of the line), and the line origin are printed.

The line origin is composed of the serial number of the last logic block before the line name and the number of the printing line of that block.

When the output line branches to several pages, the sink pages are listed below the line name.

In Figure 3-4, the top output line is "TC128-2 Read Data Line AF4." The sink page number is TC128 (the page where the line is going); the active state of the line is minus (-) and a description of the line would be "2 Read Data Line"; the source point is the logic block whose serial number is AF, and the line leaves the block at position 4.

ENGINEERING CHANGES

To the left of the title block, 20 engineering change levels, with dates, may be listed in two columns of 10 lines. For example, Figure 3-3 shows EC 25355C on 05-07-64.

COMMENTS

Comments are at the bottom left of the page. As many as ten lines of comments may be listed.

CONNECTOR AND RESISTOR LISTING

Connectors and resistors (Figures 3-4 and 3-15) are listed at the bottom center of the page. Space is provided to list 100 connectors or resistors. The general form of an SLT logic connector is:

01	A-	D3	B2	D09
Frame	Gate	Board	Socket	Pin

The general form of an ASLT or MST logic connector is:

(First Line)

BL4	B-	A1	E6	D02
Connector Source	Gate	Board	Socket	Pin

(Succeeding Lines)

2	01	A-	A3	M5	D07
Level/Type Indicator	Frame	Gate	Board	Socket	Pin

The level/type indicator shows "blank, 1, 2, etc." to indicate further branching on the connection chain.

The level/type indicator characters are in pairs and show the two ends of a cable. When the format is as shown in Figure 3-16, "AC4-A-A1M4D07" precedes the first "1" level connector.

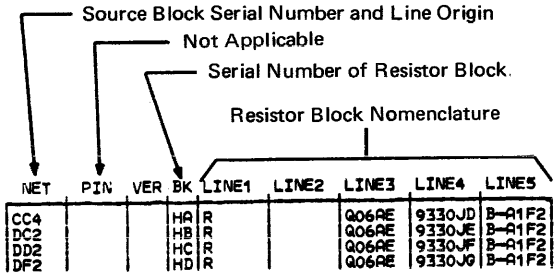


Figure 3-15. ALD Resistor Chart

Example of Connector Listings:

AC4-A-A1M4D07
1 01A-A3M5D07
2 01A-A3H8B06
2 01A-A4H1B11
3 01A-A3C1B11
3 01A-A2C8B06

Pictorial Representation:

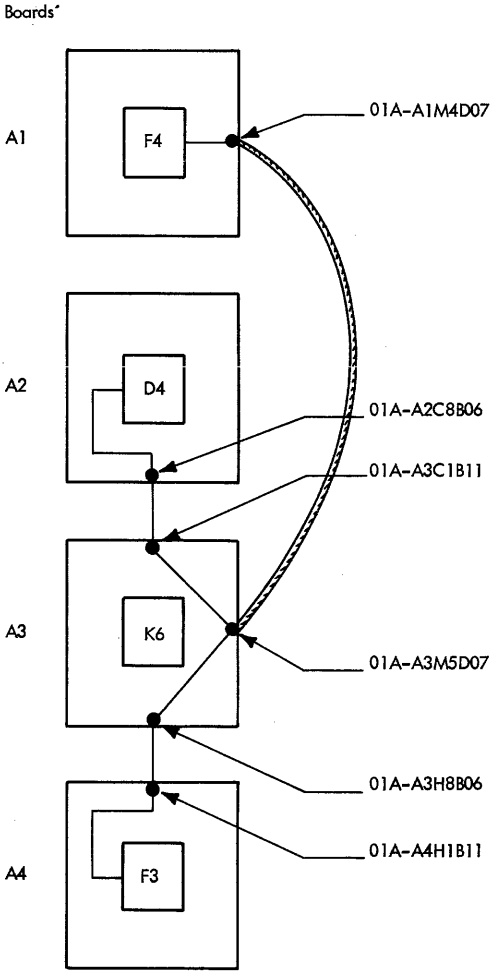
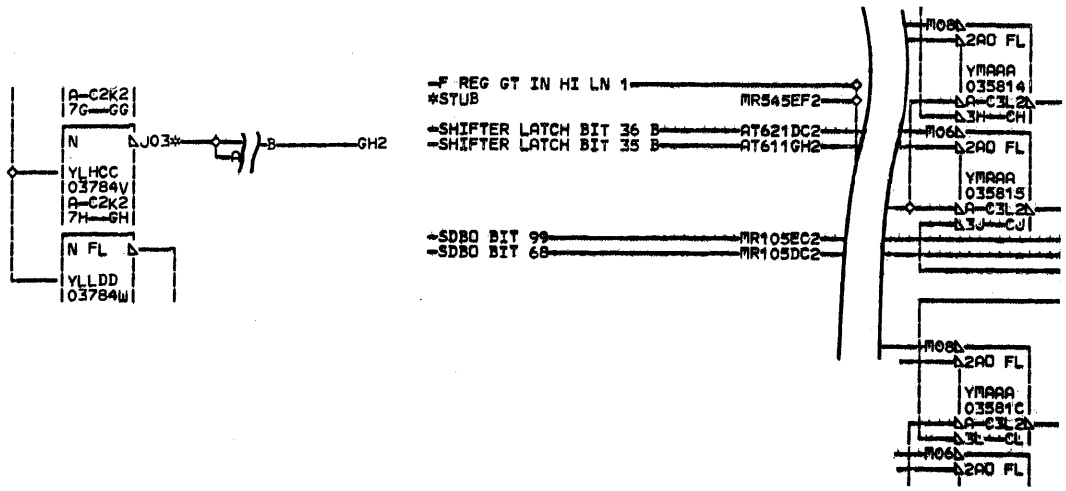


Figure 3-16. Connector Listing, Example



		NET	PIN	VER	BK	LINE1	LINE2	LINE3	LINE4	LINE5
DC2**	GB2**									
1 04A-C2L6E02	1 04A-C2M6A04	AL6			AP	R		YCAAA	037816	A-C2K2
1 04A-D3R1C11	1 04A-D3R1B13	BG2			AQ	R		YCAAA	037817	A-C2K2
DD2**	GC2**	BK4			AR	R		YCAAA	037818	A-C2K2
1 13X115G-G03	1 13X115G-G05	CB4			AS	R		YCAAA	037819	A-C2K2
2 13X215G-G03	2 13X215G-G05	DC2**	U08		AU	R		YCAAB	03781A	A-C2K2
1 04A-C2S1A13	1 04A-C2S1A11	DD2**	B03		AV	R		YCAAB	03781B	A-C2K2
2 02A-C3U6D04	2 02A-C3V2S04	DG2**	D06		AW	R		YCAAB	03781C	A-C2K2
DG2**	GG2**	DH2**	D05		AX	R		YCAAB	03781D	A-C2K2
1 04A-C2M6A02	1 04A-C2M6B04	DK4			AY	R		YCAAA	03781E	A-C2K2
1 04A-D3R1B11	1 04A-D3Q1C11	EK4			AZ	R		YCAAA	03781F	A-C2K2
DH2**	GH2**	FB2			BQ	R		YCAAA	03781G	A-C2K2
1 13X115G-G07	1 04A-C2T1A11	FG2			BR	R		YCAAA	03781H	A-C2K2
2 13X215G-G07	2 02A-C3V2M14	GB2**	D13		BS	R		YCAAB	03781J	A-C2K2
1 04A-C2T1A13	2 13X215G-G09	GC2**	B04		BT	R		YCAAB	03781K	A-C2K2
2 02A-C3V2U04	1 13X115G-G09	GG2**	J09		BV	R		YCAAB	03781L	A-C2K2

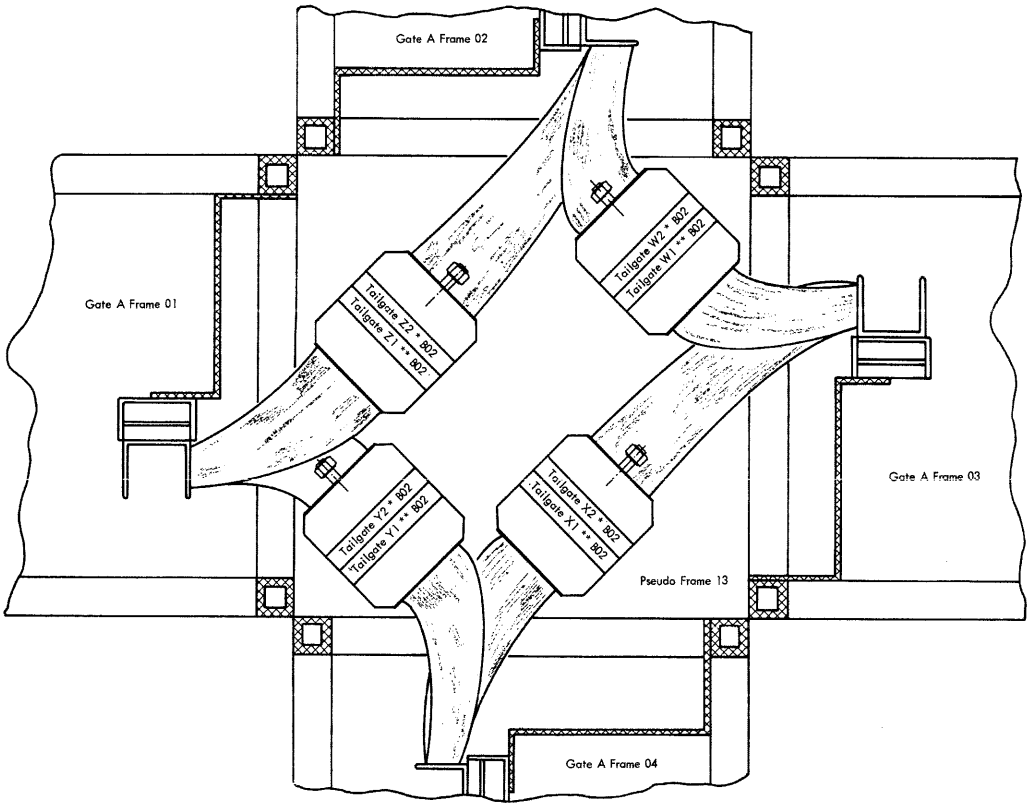


Figure 3-17. Tailgate Connector Listing, Example

Figure 3-16 shows an example of a connector listing. In the illustration, connectors 01A-A3H8B06 and 01A-A4H1B11 are on a branch from connector 01A-A3M5D07 and are considered as connector 2. The 01A-A3C1B11 and 01A-A2C8B06 connectors form another branch from connector 01A-A3M5D07 and are called level 3 on the connector listing. The connections are made by signal wire connectors.

"A, B, C, etc." indicate that the connection is one wire of a six-pack connector. The connector source "GH2" in Figure 3-17 may be followed by an asterisk (*) which means that the connector is either a connector or a terminating resistor. When the connector source "GH2**" is followed by two asterisks (**), the connection is to both a terminating resistor and a connector cable. A "9" indicates that the connection is a plug-on terminating resistor.

Another example of a connector listing (Figure 3-17) shows a net involving a tailgate. In the illustration, the "1" level indicator indicates the connector that is on the "to" side of the tailgate serpentine connector, and the "2" level indicator indicates the connector that is on the "from" side of the tailgate serpentine connector.

The general form of the resistor listing is:

CC4 Source Block	HA Serial Number of Resistor Block	R Function	Q06AE Circuit Number	9330JD Card Part Number and Portion Number	B-A1F2 Card Location

Resistor block nomenclature is:

Line	*Description*
1	Function is "R".
2	Characters 1 through 4 are blank; characters 5 and 6 are component portion and subportion.
3	Circuit number (or identification).
4	Characters 1 through 4 contain the component type which refers to the listing, the part numbers on the component assembly drawing; characters 5 and 6 are card portion.
5	Location of the A01 pin of component character 1 is A through 9 (or up and down dimension of the card) and characters 2 and 3 are 01 through 54 (the shroud or socket side of the card); character 4 is always a minus (–) and character 5 is the orientation of the component (see Figure 4-4).

The actual and implied cables are designated in Figure 3-18. For example, there is an implied cable from the source block BD4, to the 03A-B4U2G13 end of cable 1 whose other end is 03A-C4M6C02.

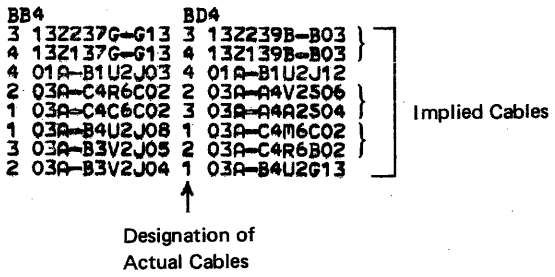


Figure 3-18. Implied Cables, Example

VOLTAGE LEVELS AND DELAYS

Complete information about voltage levels and delays for logic blocks is in the card ALD documentation for each system. In addition, voltages and logic block voltage codes are tabulated in ALD and FEALD chapters 3 and 5. Typical block delays for each technology are in Chapter 1.

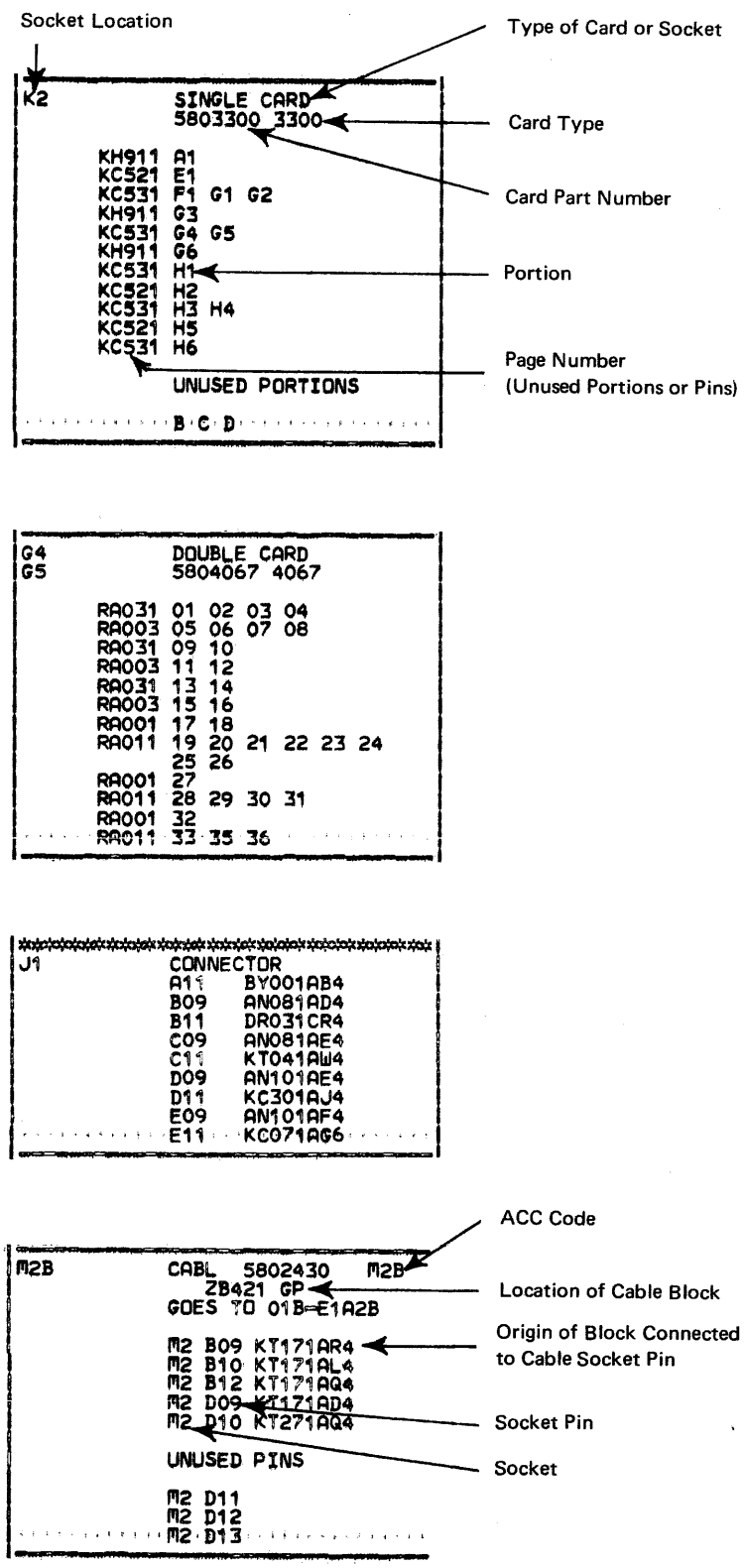
SOCKET LISTING

The socket listing (Figure 3-19) is a physical layout of an SLT board showing the cards and cables used and their ALD page locations.

Each card and socket listing shows the ALD page for each portion or pin used. The unused portions or pins are also listed.

Each board has a summary listing which shows the cards and cables in part number order. Each part number has the ACC code, card type (as in the ALD block), sockets occupied, and total cards for the board. The unused sockets on the board are also listed.

Generally, the socket listing is at the beginning of the ALD's in Volume 0.



PAGE 02

PLUG LIST

PART NO	ACC	TYPE	SOCKETS	TOTAL
5800000		0000	B4 B6 C6 G3 G6 G7 H6	07
5800006		0006	C7 E6 F5 G4	04
5800007		0007	F4 J6 J7 L4 M4	05
5800008		0008	E7 F6	02
5800015		0015	D5 F7 G5 H5 H7 K5 K7 M5	08
5800199		0199	D4 F3	02
5800236		0236	D6 L5 L7	03
5800243		0243	C4 L2	02
5800310		0310	E4	01
5800529		0529	J4	01
5802200		CABL	A2 A3 N3 N7	04
5802201		CABL	A5T	01
5802202		CABL	A6B	01
5802204		CABL	A5B	01
5802207		CABL	N5B	01
5802216		XOVR	N4 T1 T3 T4	04
5802928		CABL	T5 T6 T7 T8	04
5803016		3016	J2 K2	02
5803024		3024	E5	01
5803028		3028	B7 L3	02
5803031		3031	D3 M7	02
5803036		3036	J5 L6 M6	03
5803043		3043	E3	01
5803063		3063	B5	01
5803064		3064	C5	01
5803067		3067	B2 C2 D2 E2 G2 H4	06
5803131		3131	B3 C3	02
5803357		3357	H3 J3 K3	03
5803578		3578	F2 H2	02
5804018		4018	K6	01
5804025		4025	D7 K4	02
5804651		4651	M2	01
UNUSED			A4 A7 N2 N6 T2	05

Summary of socket listing for one board (generally on page 2)

SOCKET LISTING
DATE 02-23-67 MACH. 2040HSC Z C 5 5 1
LOG 246 BOARD 01A-B3
PREV. ENGR. - -
PRES. ENGR. 02-22-67 282029
P.N. 537XXXX SDD 026
IBM CORP. SDD BLK.

Socket listing page identification

Figure 3-19. Socket Listing

- A card ALD sheet shows ALD logic blocks appearing on a given SLT/SLD/ASLT/MST card.
- The assembly drawing shows the physical placement of the components on the card.
- The schematic shows a circuit diagram of the electronic components on the card.

The card layout is defined as the card ALD sheet, the assembly drawing sheet, and the schematic sheet. These sheets (Figure 4-1) are a three-way representation of the actual logic card.

At least one page is provided for each type of sheet but only one page is provided for the assembly drawing. The circuit complexity, the circuit speed, functional versus logic card packaging, and the size of the card are some of the factors determining whether a card will have more than one page of card ALD sheets and/or schematic sheets.

SLT AND SLD CARD LAYOUT

Card ALD Sheet

The card ALD sheet (Figure 4-1, part 1) is similar to a standard ALD logic sheet. The part number appears at three corners of the sheet. The part number consists of four digits and a suffix. Generally, a 580 precedes the four digits; because of exceptions, however, the prefix must be verified by checking the complete part number in the title block. The suffix consists of the number of the card ALD sheet. The engineering change (EC) level appears to the left of the title block.

Logic Block

The logic block is similar to the ALD logic block, except that specific machine information is omitted. Line 1 gives the function of the block; an asterisk (*) is placed before the function name if the input line position is significant. Line 3 designates the circuit number. Line 4 describes the portion and subportion of the block. Line 6 indicates the block position and the serial number of the block for the card ALD. Sometimes the engineering specification of the circuit is placed above the block; for example, the OR block at location 2B of Figure 4-1, part 1, is labeled 890972. The pin numbers of the card, if they exist for the block, are placed on the input and output lines of the logic block.

As in standard ALD logic blocks, wedges (◺) denote the line levels required to satisfy the function of the block.

Card Characterization

The lower left corner (Figure 4-1, part 1) contains information concerning the card size, the voltage pins, and the card characterization code. Five card sizes are in general use: 1-6, 1-12, 2-6, 2-24, and 2-36, where the first digit (1 or 2) designates the number of the socket into which the card fits, and the next digit or digits (6, 12, 24, or 36) designate the number of standard module positions on the card.

The voltage pin information indicates where and what actual voltages are present on the card.

The card characterization code indicates the general voltage and the logical use of the card. This code has a voltage code and a use code, which consists of the number portion of the circuit number. See Figure 3-7 for interpretation of the use code.

The voltage codes are:

T	Requires a +3V, −3V, or +6V power supply or any combination.
V	Requires *only* a +12V power supply.
U	Requires a +3V, −3V, or +6V power supply or any combination and is specifically associated with the 5ns family.
S	Requires either a combination of the voltages listed for U or may be used in category.
L	Are the SMS circuits associated with the SMALL family.
O	Are associated with analog circuits.
X,Y	For MST circuits

For example, T03 (Figure 4-1, part 1) means the card uses a combination of +3V, −3V, or +6V (T) and has logic circuits (03).

Input Lines

Input lines are identified by the pin number of the card and by a net number. An example of pin number on a card is D05.

The net number may be a number assigned by design automation, such as 001 or 002. However, it may be a net number of the type used when there are multiple card ALD sheets; the number 41681AB4, for example, means the line originates from the block on part number 5804168, page 1, with serial number AB, fourth line.

Output Lines

Output lines are identified by the source block and line origin and by a net number. The source block and line origin (for example, AA5) are the same as that shown on the ALD page.

The net number is either the card pin number or a combination of the card pin number and the page number to which the line goes. An example of the card pin number is J10. If the line goes to page 41682, the combination is 41682J10.

Assembly Drawing

The assembly drawing sheet (Figure 4-1, part 2) contains two parts. On the left portion of the page, a graphic representation of the components on the card and on the right side of the page, a chart listing the part numbers.

This sheet has the part number in the upper right and lower left corners, a title block in the lower right corner, the EC record in the upper right portion of the sheet, and a chart of the voltages and their respective pins near the part number chart.

The part number chart (Figure 4-1, part 2) consists of a listing of the component parts used on the card. Each component is listed with part number, description or value, quantity used on the card, and a code that is used on the schematic sheet and the assembly drawing sheet. The module code is A for an RC module and Z for an SLT module.

The graphic representation shows the numbers for each component (modular and discrete) from top to bottom and from right to left.

Schematic Sheet

The schematic sheet (Figure 4-1, part 3) shows the schematic of the circuits, along with the card part number, a regular title block, and an EC block. The schematic has the actual components (such as resistors, transistors, diodes, and capacitors) of the ALD logic block (by circuit numbers). The components are keyed to the assembly drawing by a location code.

Each ALD logic block in the ALD's references an SLT card by part number. Each particular ALD logic block has card pin numbers and a circuit number. The same ALD block is on the card ALD sheet of the card layout and also on the schematic sheet with the same card pin numbers and circuit number.

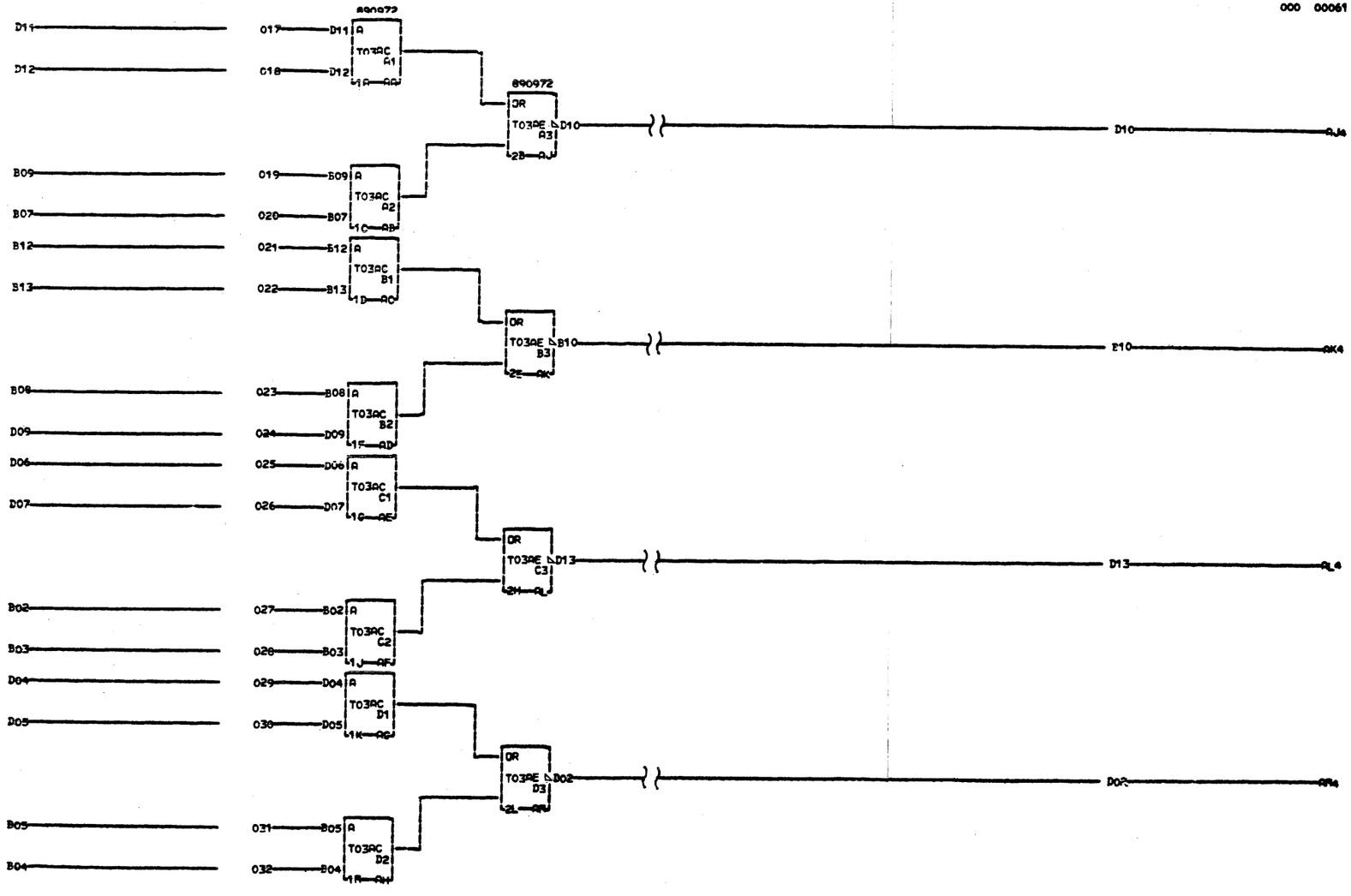
The circuit number on the schematic sheet identifies its components. The identification of each component is its physical location on the card as shown on the assembly drawing sheet, Figure 4-1, part 2.

The complexity of the card may require more than one sheet of schematics. Sometimes each sheet (Figure 4-1) is complete as far as the individual circuits are concerned; that is, there are no electrical connections between circuits on the card. However, if the circuits are electrically connected, the schematic is interconnected on more than one sheet.

Particular Example

A particular logic line can be examined by using Figure 4-1. The logic line labeled D11 is the top line of part 1. This line has a net number, assigned by design automation, of 017. This line enters the card on card pin D11. This line in its more positive condition activates one leg of AND circuit T03AC. Part 3 shows that the logic line entering the card at D11 is connected to pin 3 of a module. Numbers with squares around them (□) refer to pins of a module. Pin 3 of the module is connected to the cathode of the diode labeled 5Z1. The diode 5Z1 is one of two legs of circuit T03AC. Circuits are usually labeled with their circuits numbers on the schematic sheet.

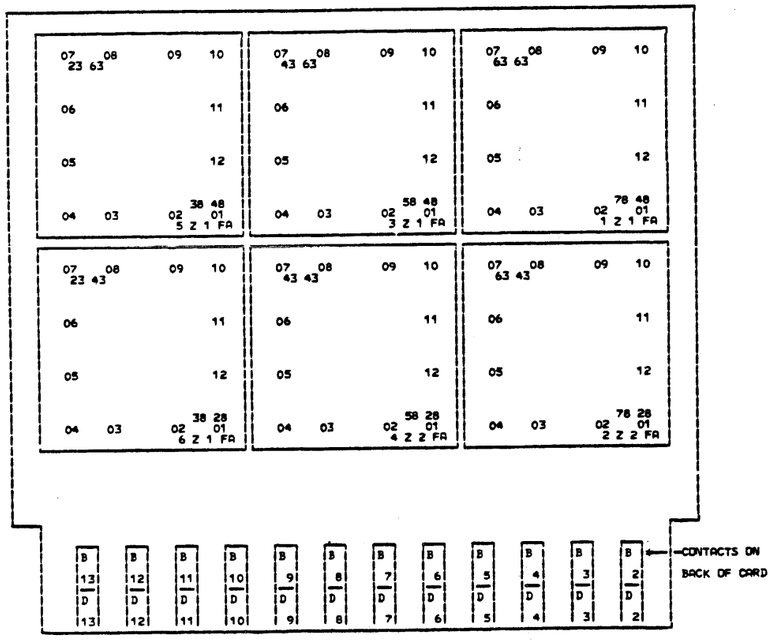
The part number chart on part 2 shows that Z1 is part number 361000. The 5 of the 5Z1 designation of the diode locates the module as the fifth component on the card when counting top to bottom and right to left. In the chart, module 5Z1 is in the upper left portion of the card.




```
CARD SIZED 1-6 PAC          T03
VOLTAGE PINS
0 +6V0B11      +3V0D03
0 -3V0B06      GND0D08
0 STANDARD RESTRICTED
6
1
000
```

```
4-2INPUT-2WAY AND OR INVERT                    0
DATE   02-24-64 MACH. ASSEMBLY                 0
LOG          0491 FRAME                        6
                  P.N. 580XXXX                 1
IBM CORP.   ED BLK.          AN                000
```

Figure 4-1. Regular Card Layout (Part 1 of 3)



STANDARDS CODE	2-7045			580XXXX
CIRCUIT APPROVAL		- -	STATUS	RESTRICTED
LOCATION				
RAW CARD NUMBER	5812019		HOLE PATTERN	811192
FRONT ARTWORK	DATE	CHANGE NO.	DATE	CHANGE NO
5812018 3	10-25-62	DEV 10762	2-19-63	DEV 1265
BACK ARTWORK	1-4-63	DEV 11871	4-18-63	DEV 1421
5812020 3	1-21-63	D-DEV 1PP	3-19-64	160021

PIN	VOLT.
D 8	GRD
D 3	+ 3
B11	+ 6
B 6	- 3

CODE	PART NO	VALUE	QTY
Z 1	361000	SLT MODULE	4
Z 2	361001	SLT MODULE	2

NOTES.

AA-ALL CIRCUITS MUST CONFORM TO ENG.SPEC. SHOWN ON SHEET 1.

AB-ASSEMBLE TO ENGINEERING SPECIFCATION 890913

AG-CARD CONFORMS TO ENGINEERING SPECIFICATION 890918.

FA-TECH LAB EVALUATION INCOMPLETE. PART SUBJECT TO WITHDRAWAL.
ADDITIONAL USAGE TO BE AVOIDED

X RESTRICTED USAGE. TECHNICAL LABORATORY APPROVAL INCOMPLETE. PART SUBJECT TO MODIFICATION AND/OR WITHDRAWAL. USE IN SLT APPLICATION ONLY

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	4 2-INPUT 2-WAY AND OR INVERT				
DESIGN	02-03-64	VE	TYPE		
DETAIL	02-20-64	JMR	SCALE	NONE	
CHECK	03-02-64	MZ	DRGW	7090	03-17-64
APPRD	- -		SHEET	OF	

580XXXX

Figure 4-1. Regular Card Layout (Part 2 of 3)

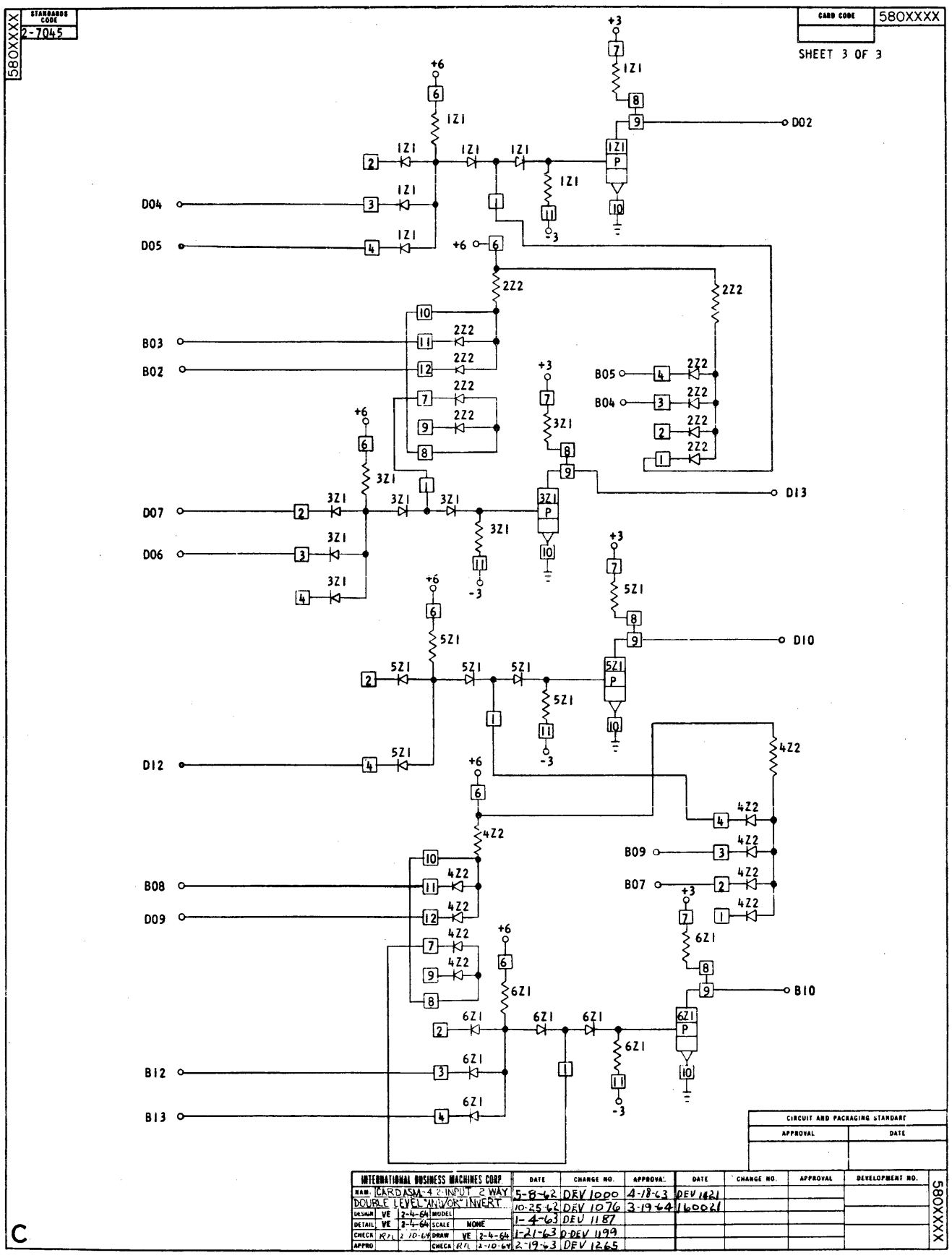


Figure 4-1. Regular Card Layout (Part 3 of 3)

ASLT CARD LAYOUT

ASLT card layout is similar to SLT card layout. The difference is in the information on lines 2, 4, and 5 of the logic block (Figure 4-2). Also part 2, the assembly drawing (Figure 4-4), has different component locations and coding.

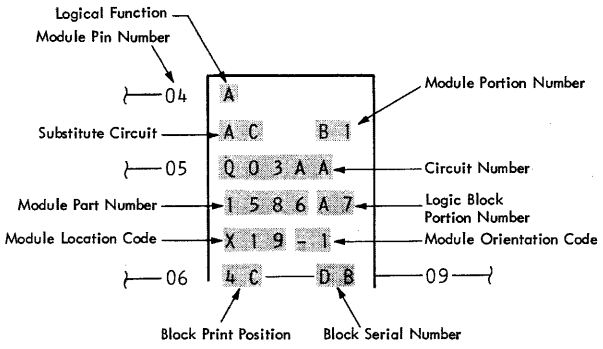


Figure 4-2. ASLT/MST Card ALD Logic Block

Logic Block

Line 2 describes the substitute circuit and module portion number. The two-output Q03AC circuit in a module can be used for a one-output circuit (Q03AA or Q03AB) by not wiring it to the unused pin. When a Q03AC is thus used, the last two letters of the Q03AC circuit number appear in the first two characters on line 2, and the one-output circuit number appears on line 3. Module circuits are assigned portion numbers for special test purposes. The module portion number appears in the last two characters on line 2.

The first four characters on line 4 are the last four digits of the module part number. The last two characters describe the portion number of the logic block.

Line 5 describes the module location coding (first three characters) and the module orientation coding (last character). A numeric character denotes ASLT orientation; an alphabetic character denotes MST orientation. The module location and orientation coding system is shown in Figure 4-4. Note that the module locating pin is in the lower right corner of the module.

MST CARD LAYOUT

MST card layout is similar to ASLT card layout. The main difference is in component orientation.

Component Orientation

The orientation characters in the card SLD block identify the direction of pin A02 from A01, regardless of whether the component has a physical pin A02. The code is:

Code	*Direction to Pin A02*
A	←
B	↑
C	→
D	↓

For example:

Line 5 of ALD Block	*A01 Hole*	*A02 Hole*
X15-A	X15	X16
X15-B	X15	Y15
X15-C	X15	X14
X15-D	X15	W15

Edge Connectors—Only MST Card ALD Pages

The format of the edge connectors on the card ALD page is shown in Figure 4-3.

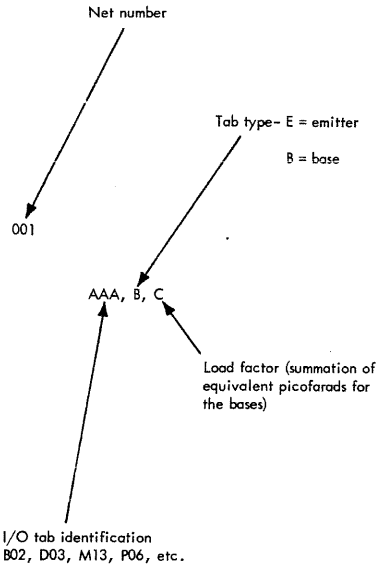


Figure 4-3. Edge Connectors—MST Card ALD Page

MST Card Coordinates (FEALD)

Figure 4-5 represents an MST card and shows the coordinates for locating module pins for scoping. The need to locate a module pin arises when a storage device on an FEALD (MST) is buried (not connected to a card I/O pin) and must be scoped. In Figure 4-5, the designation 09B represents a module pin; B09 would be a card I/O pin on an FEALD.

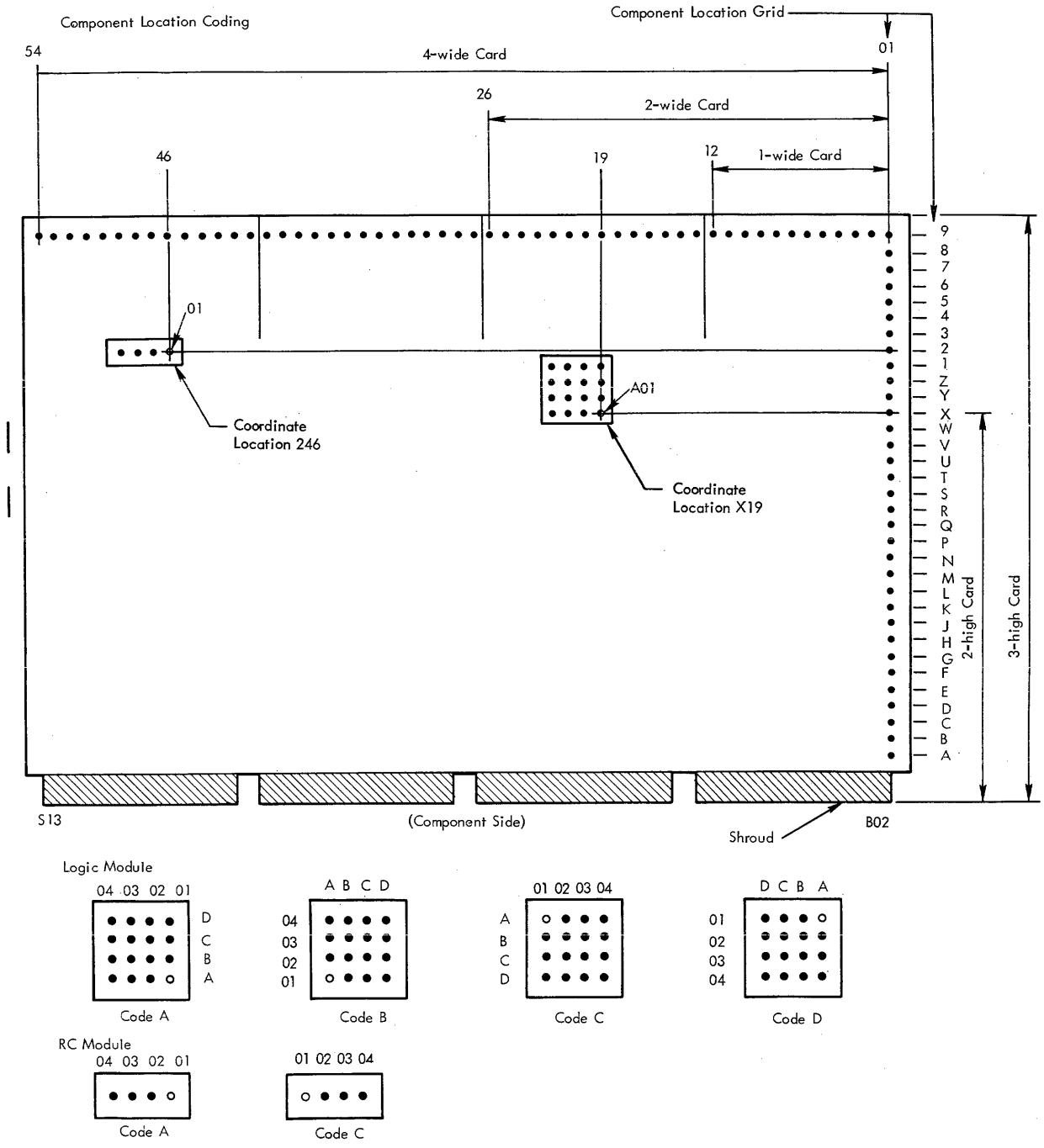


Figure 4-4. ASLT/MST Component Location and Orientation Coding

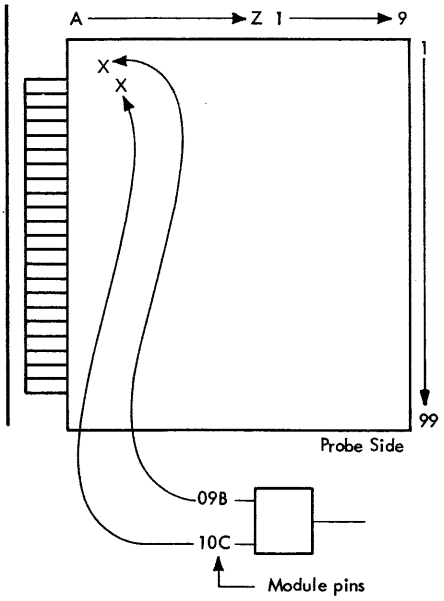


Figure 4-5. Card Coordinates (MST)

Card Coordinates (TTL Modules)

Figure 4-6 shows card coordinates for locating TTL module pins on an MST card. The first digit defines a region on the card; the next three digits define the column and row.

Note: Depending upon card size and other factors, region 1 may end on a digit other than 9. Before scoping TTL module pins in region 2, check the card layout to determine the exact layout of the card being scoped.

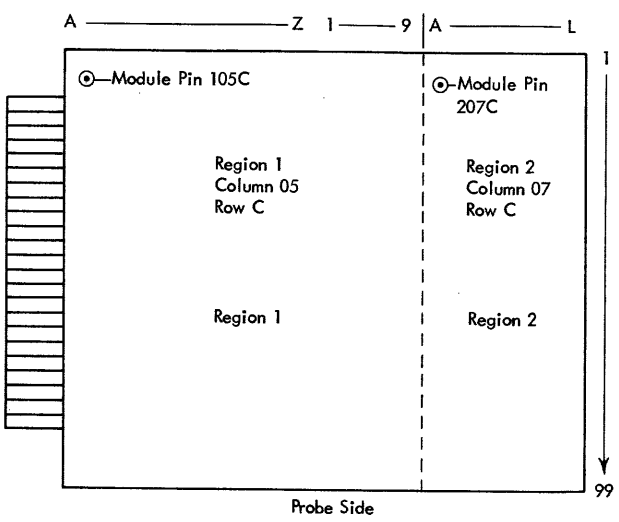


Figure 4-6. Card Coordinates (TTL)

- Field Engineering ALD's (FEALD) are a simplified form of engineering ALD.
- FEALD's are of two types: line-drawn and direct-addressing.
- An FEALD for an SLT machine is always a line-drawn page.
- An FEALD for an MST machine may be line-drawn or direct-addressing.
- A direct-addressing FEALD generally represents more than one engineering ALD page.
- An FEALD (MST) can contain functional logic blocks such as the selector, register, and decoder.

While a machine is in its design stages, engineers generate engineering ALD's. After a design is complete, a design automation program provides Field Engineering with the prime maintenance document–the FEALD. Figure 5-1 shows that there are three forms of FEALD's produced by two FEALD programs. An FEALD for SLT machines is a simplified, 1 for 1 representation of an engineering ALD. For MST machines, the use of functional logic blocks permits more logic to be shown on a page, thereby allowing multiple engineering ALD pages to be represented by one FEALD page–this is the direct-addressing FEALD. In MST, line-drawn FEALD's and direct-addressing FEALD's may be intermixed on a given system. In either case, the FEALD represents the machine logic on a field-replaceable unit, normally a card.

The following text describes the FEALD for SLT machines. Later in this chapter, the FEALD for MST machines will be covered. To differentiate the two types of FEALD's, the FEALD for MST machines is abbreviated FEALD (MST).

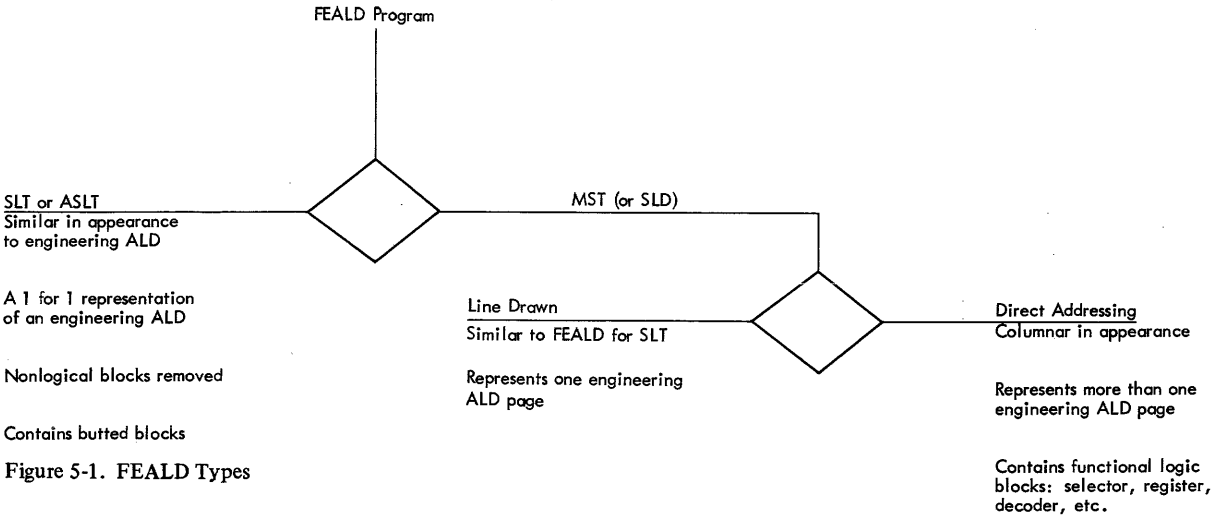


Figure 5-1. FEALD Types

PAGE NUMBER

The page number is in three places on the sheet. The page number in Figure 5-5 is KH331. In this illustration, the page number is in the upper right corner, as well as in both the lower right and the lower left corners.

Logic pages are numbered according to a coded prefix consisting of two alphabetic symbols, representing the major and the minor characters. The general coding scheme is shown in Figure 5-2.

For example, the coding for the A-register is RA. "R" is the major character; it means register. "A" is the minor character, designating the particular register. The minor characters and their designations vary from system to system.

Figure 5-2 is CPU-oriented. Slight variations appear both in the CPU pages and in the I/O pages.

Adders	
Addressing Adder	AA-AB
IC Incrementer	AC-AD
Exponent Adder	AE-AF
Main Adder	AM-AQ
Serial Adder	AS
VFL and Decimal Adder	AV-AW
Busing (Excluding Storage Bus)	BA-BZ
Consoles	PA-PE, PJ-PZ
1052 Console Adapter	PF, PG, PH
Controls	
Advance or Seq Controls	KA
Branch and IC Controls	KB
Clock Controls	KC
I-Execute, I-Fetch, and Execute	KD
Chan Controls	KE
Fixed Sequence Controls	KF
General Register Controls	KG
FLT Controls	KH
ROS Controls	KK
Local Storage Controls	KL
Priority and Interrupt Controls	KM
I/O Instruction Controls	KN
VFL Controls	KP
VFL Controls	KQ
Check Triggers	KR
Status Triggers	KS
VFL Controls and Decimal Controls	KY
Any Miscellaneous Controls such as FP Fixed Point, Storage Protect, Real Time Clock, Status Controls	KT-KU KW-KZ
Counters	
Instruction Counters	CA-CB
Local Storage Address Counter	CC-CD
Miscellaneous Counters	CE-CZ
Hardware-Oriented Pages	ZA-ZZ
CROS	ED-EF
Decoders	
Op Decoders	DN
FLP and Generator Decoder	DP
Addressing and Pre-Fetch	DA
Trap Decoder	DB
Register Decoder	DG
ROS Decoder	DR-DS
I/O Channels	
Multiplexer Channel	FA-FZ
Selector Channel 1	GA-GZ
Selector Channel 2	HA-HZ
Direct Data	JA-JZ
Local Storage	LS-LT
Main Storage Registers and Controls in CPU (Includes SDR Registers, Storage Buses, SAR, SBI, OR, M and N Registers	MA-MC
Power Supplies	YA-YZ
Registers	
A-Register	RA
B-Register	RB
D-Register	RD
E-Register	RE
F-Register	RF
G-Register	RG
H-Register	RH
J-Register	RJ
K-Register	RK
L-Register	RL
M-Register	RM
N-Register	RN
P-Register	RP
Q-Register	RQ
R-Register	RR
S-Register	RS
T-Register	RT
U-Register	RU
V-Register	RV
W-Register	RW
X-Register	RX
VFL and Decoder Register	RY
Direct Data Register	RZ
ROS Flowcharts	QA-QZ
Special Features	XA-XZ
TROS	EA-EC

Figure 5-2. ALD Page Number Prefixes

MACHINE VERSION

A version page shows wiring and cards that are not on the basic machine. This wiring must be added to that used in the basic machine. This is in direct contrast to the additive card code (ACC), in which the wiring is part of the basic machine, and only cards are added to make the feature operative. An example of a version page would be those pages that add the cards and wiring for the floating-point feature.

A version page is made up of all basic page blocks which are unchanged in the version design plus additional blocks (version blocks) needed to change the basic page into a version page.

The machine version number appears below the page number; for a basic (standard) machine, this number is 000 (Figure 5-3). A version page assigned by design automation has a number other than 000.

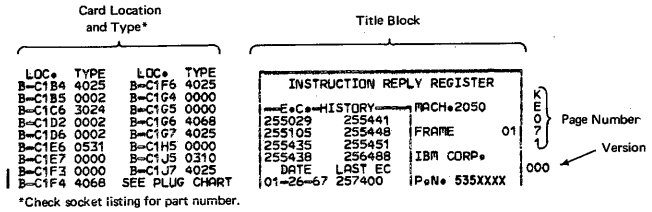


Figure 5-3. Title Block, Page Number, and Version

TITLE BLOCK

The title block is printed in the lower right corner of the page. As Figure 5-3 shows, information can be found at three places in the block:

1. At the top
   a. The page title ("Instruction Reply Register" in Figure 2-21).
2. On the left side
   a. The engineering change (EC) history in two columns with the latest EC number and date.
3. On the right side
   a. Machine type, "2050." This may be a pseudo number or it may be the machine number followed by a suffix. The suffix differentiates between models or features of the machine number.
   b. Frame, "01"; within the machine, may be 01 to 63.
   c. The corporate division, WTC (World Trade Corporation).
   d. Part number of the page (sheet), "535XXXX."

LOGIC BLOCK

Logic blocks shown in Figure 5-5 are positioned on the page in a matrix 7 columns wide and 13 rows high. The columns are numbered 1 through 7. Rows are lettered A through N, excluding I.

A logic block (Figure 5-4) is 6 increments wide by 5 increments high; it may be lengthened downward to a maximum of 24 increments. The block may have 1 to 5 inputs and/or output lines on the basic block; 1 to 24 input and/or 1 to 10 output lines on the extended block.

Information Inside the Block

Top Line (Line 1)

Line 1 (the top of the block) consists of the multiblock configuration, such as FF, in positions 1 and 2 and the serial number of the block in positions 5 and 6. The serial number of the block is a part of the net number and part of the identification of the asterisk function of an output line.

Line 2

The logical function being performed by the circuit represented appears on line 2; for example, A, OR, N, or FF. An asterisk (*) preceding the logical function symbol means to design automation that the input line positions are placed in a certain arrangement; that is, the pin numbers and position of the input lines are fixed by the physical makeup of the components used.

The suffix, preceded by a space and following the function, is additional information describing the function. The suffix indicates additional information that would be helpful in understanding the circuit such as A V or AR ID; and to indicate additional information in component blocks such as RY CT, RY P, or A LT.

An asterisk (*) in position 6 indicates an unchecked block. This can occur when:

1. The engineer who submitted the page specified that checking is not to be performed. This is normally done to process special blocks such as exit, entry, service, switch, and component.
2. The program does not have sufficient data to perform the checking operation. Errors in drawings or circuit rules are indicated with six asterisks in line 2, the function placed on line 3, and the block lengthened one line (see block serial number BD in Figure 5-6).

Line 3

The additive card code (special machine feature) appears here; for example, 7TR (seven-track feature). Additive card codes identify those logic blocks which pertain to a special class of machine features in which the feature can be installed by plugging in the feature cards. Also, when the block is an input to a DOT block, the DOT function, such as +A or ◺ O, is indicated in position 6. If the output "DOTing" cannot be specified within the two positions available, the characters WL (wired logic) appear here.

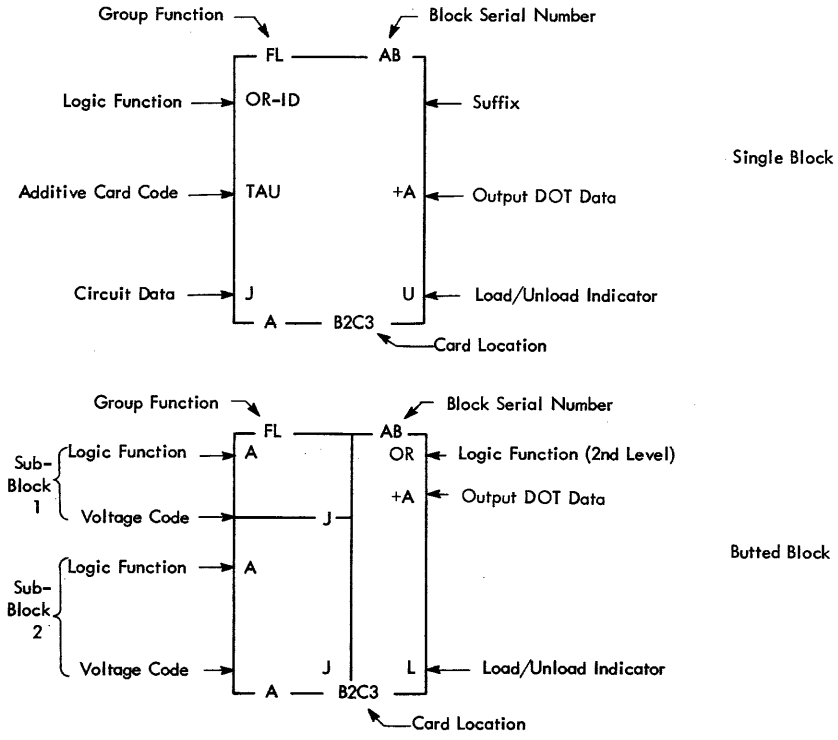
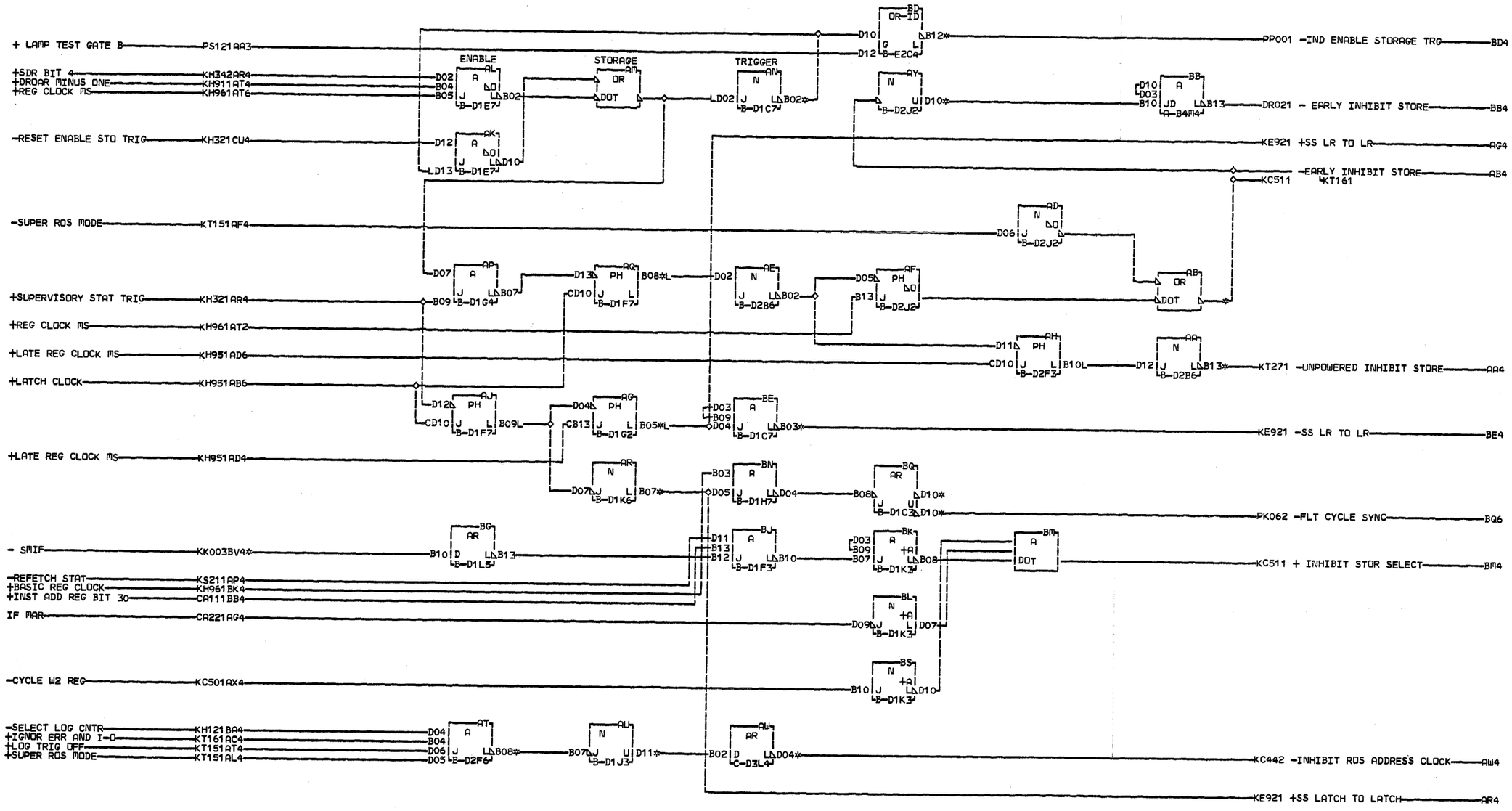


Figure 5-4. FEALD Block



K H 3 3 1 000

KK003BV4 RESISTOR B-D1L5B09 AG4 AA4 B-D2M8E04 01B-E2C8E04 AN4 01B-E2N3D13 01A-A2A3D13 AB4 B-D1H8D04 01B-D2H1D09 AQ2
01B-D2N2D04 01B-E2A2D04 01B-D1J8A06 01B-D2J1A11 01B-D1M8A06 01B-D2M1A11 01B-D2N2B06 01B-E2A2B06 01B-D1A5B05
01B-D2A4B05 AW4 C-D3J1B09 AR4 B-D1J8C06 AY4 B-D2N2B02 AT4 B-D2A4B11 01B-D1A5B11 AU4 B-D1N2D10 01C-D3N2D10 RESISTOR C-D3L4B12
A-B4M4B09 BD4 B-E2B4B07 01B-E2N2B10 BE4 B-D1A6D04 01A-A3N3B10 01A-A3N4D04 01A-B4A4D04 RESISTOR
B-D1C3B02 BQ6 B-D1N7B12 01C-A3C4B12 01C-A3F4D02 01C-A3C8B04 01C-A4C1B09 01B-B1N5D04 01B-B1G8E06 01B-B2G1E11 BQ4 RESISTOR

LOC.	TYPE	LOC.	TYPE
A-B4M4	4019	B-D1J3	3024
B-D1C3	4061	B-D1K3	4025
B-D1C7	4025	B-D1K6	0000
B-D1E7	0000	B-D1L5	4019
B-D1F3	0000	B-D2B6	4025
B-D1F7	4007	B-D2F3	4007
B-D1G2	4007	B-D2F6	0531
B-D1G4	0000	B-D2J2	4025
B-D1H7	0000	SEE PLUG CHART	

INHIBIT ROS STORAGE FUNCTIONS
E.C. HISTORY
255029 255448
255105 255458
255435
255441
DATE LAST EC
12-06-66 123457
MACH. 2050AMD
FRAME 01
IBM CORP.
P.N. 535XXXX

000C

Figure 5-5. Field Engineering Automated Logic Diagram (FEALD)

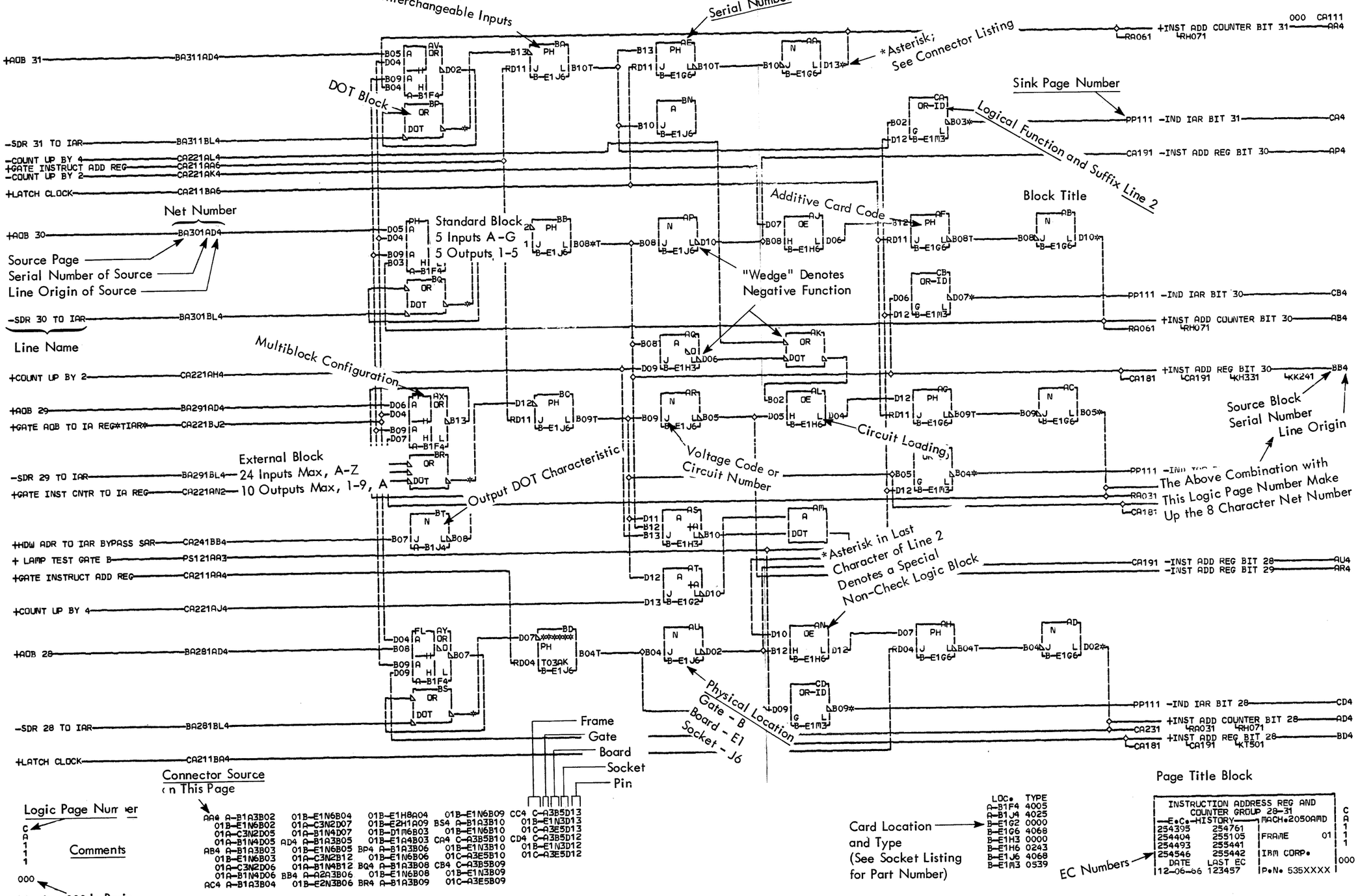


Figure 5-6. Annotated FEALD Page

Line 4 (Always the Next-to-the-Bottom Line of the Block)

Circuit data appears on this line. The voltage code (Figure 5-7) appears here for a standard circuit. Blocks with two or more input requirements have all the codes on this line (requirements from top to bottom, corresponding to the voltage codes from left to right on the line).

The voltage code does not appear in a block without pins; that is, the voltage cannot be measured with a meter or an oscilloscope.

Code	Minimum Up Level (Volts)	Minimum Down Level (Volts)
B	2.5 to 2.1	1.9 to 1.5
C	2.5 to 2.1	1.4 to 1.0
D	1.9 to 1.6	1.4 to 1.0
E	2.0 to 1.6	0.9 to 0.6
F	4.0 to 3.5	0.5 to 0.3
G	2.5 to 2.1	0.5 to 0.3
H	2.0 to 1.6	0.5 to 0.3
J	1.5 to 1.1	0.5 to 0.3
L	0.7 to 0.5	0.4 to 0.2
T	0.3	-0.3
Z	-1.0	-1.5

Figure 5-7. Voltage Code

The circuit number (Figure 5-8) appears here if the block is a special circuit or if the voltage requirements are not included in the defined voltage codes.

Component blocks have the necessary discrete information placed on this line.

DOT appears here when the block is a DOT block.

The load/unload indicator is placed in position 6 of this line, an L for a loaded circuit and a U for an unloaded circuit. The unloaded circuit has an asterisk (*) on the output line to denote that the load can be found in the connector listing at the bottom of the ALD page, or in the next block.

Bottom Line (Line 5)

The card location is placed on line 5 (bottom of the block):

1. Character 2 is the gate (A through Z), followed by a dash.
2. Characters 3 and 4 are the board location, one alphabetic and one numeric.
3. Characters 5 and 6 are the card location, one alphabetic and one numeric.

Information Outside the Block

Title

When logic blocks have been assigned a title, the title appears over the block.

Pin Numbers

Pin numbers are in line with the input or output line. They are the actual numbers of the base pins on the card.

Circuit Number Code -- General Forms: XNNZZ or XAYZZ

X	Circuit Classification
A or NN	Circuit Type
Y	Circuit Origin
ZZ	Circuit Number

X--Circuit Classifications

A	MST-2
B	TTL
C	TTL
O	Analog
P	MST General
Q	ASLT
R	SLD 100 ns
S	SRETL General
T	SLT/SLD 30 ns
U	SLT/SLD 5-12 ns
V	SLT/SLD 700 ns
W	Monolithic
X	MST-1
Y	MST-4

A or NN--Circuit Types

A	NN	Circuit Type
A	07	Sense Amplifier
B	55	Indicator Driver
C	61	Component
D	45	Delay Circuit
E	11	Noninverting Logic Driver less than 50 mA
F	20	Trigger, Flip-Flop, Polarity Hold, Schmitt Trigger
H	22	Oscillator
K	16	Magnetic Head and Core Driver
L	03	Logic Circuit and Extender
M	65	Functional Logic Circuit
N	10	Inverting Logic Driver less than 50 mA
P	15	Power Driver more than 50 mA
Q	25	Clip, Clamp, Limiter, Regulator
R	63	Relay
S	21	Singleshot
T	06	Transmission Line Driver, Receiver
U	32	Parity Check, Exclusive OR
V	29	Reference Power Supply
W	40	Special Circuits
X	05	Voltage Translator, Converter
Z	60	Switch Integrator, Filter

Y--Circuit Origins

A	Poughkeepsie	N	Sweden
B	Burlington	P	Austin
C	Poughkeepsie	R	Rochester
D	Holland	S	San Jose
E	Endicott	T	Boca Raton
F	France	U	United Kingdom
G	Germany	V	Boulder
H	Poughkeepsie	W	Italy
J	Japan	X	Lexington
K	Kingston	Y	Fishkill
L	Poughkeepsie	Z	Raleigh

Figure 5-8. Circuit Number Codes

Asterisk (*) on an Input or Output Line

An asterisk (*) on an input or output line denotes a connection that leaves the board; a resistor; a reference to the tabled blocks at the bottom of the page; or the end of the output line which is terminated in one of the tabled blocks at the bottom of the page. The asterisk (*) in each case refers to the bottom of the page. The information at the bottom of the page is identified (keyed) with the serial number of the block and the line number; for example, AQ4.

Information on the Side of the Block

Wedges

The wedge (◺) is a small triangle at the point where a signal line joins a logic block. The wedge indicates that the active state of this line (the state which satisfies the function of the block to produce an output line of the state indicated) is at the least positive potential with respect to the most positive potential shown by the signal line without a wedge.

A wedge is placed in the edge of the block in line with an input or output line. When the block or circuit is performing its function, the wedge indicates the most negative (least positive) dc voltage for that line.

Note: Signal lines can be at one of two voltages, an up level or a down level. Because circuits operate at different speeds and at different pulse levels (0.0V to +12.0V; +0.9V to 3.0V), the line level designated by the wedge must be described as the most negative (least positive); the absence of the wedge is the most positive (least negative) level of the line.

K in the Side

Nonlogic outputs of different blocks are not tied together by DOT blocks. Instead, a K is put in the edge of the block in line with each of the connected outputs (except one). The one exception is the output used to determine the net number.

Output (or input) lines on the same block may be tied together. In this case, the net number is the position without the K in the edge of the block (Figure 5-9).

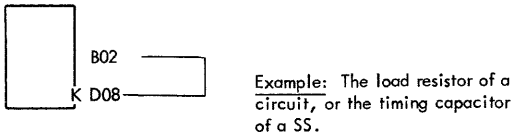


Figure 5-9. Nonlogic Outputs, K in the Side

Nonlogic outputs on different blocks may be tied together when:

1. All the outputs tied together appear on the same page. The net number then includes the line origin of one of the outputs from one block. The commoned outputs are differentiated from the source by a K in the edge of the block position.
2. All the outputs tied together are not on the same page. In this case, the outputs tied together on this page show an output to the right side of the page. The outputs in the same net on other pages return to the left of their respective pages and are referenced to the first page in the normal manner. The net number includes the line origin of one of the commoned outputs on the first page. In the edge of all other blocks having outputs in the same net, a K appears in line with each commoned output (Figure 5-10).

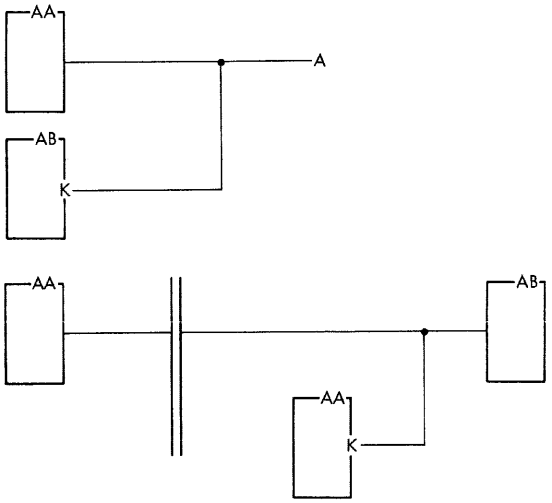


Figure 5-10. Nonlogic Outputs Tied, Example

P or N in the Side

When a capacitive input to a block is designated, a P or N in the side of the block indicates the polarity of the shift necessary to satisfy the function of the block (Figure 5-11).

X in the Side

Nonlogic connections to a logic block have an "x" in the side at the place where the polarity indicator (wedge) is normally placed. This nonlogic input or output can be a bias line. In Figure 5-12, D06x is a nonlogic connection to the two-way OR block. The nonlogic line is generally a feedthrough line or voltage line.

T at Output Pin

A "T" at the output of a block means that this pin is a test point and is capable of being scoped.

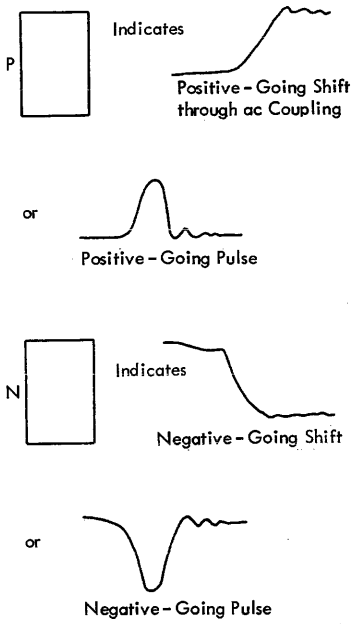


Figure 5-11. Pulsed Blocks, P or N in the Side

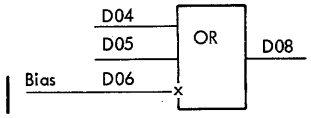


Figure 5-12. Nonlogic Connections, X in the Side

LINE NAMES

Input Line

Each input line (Figure 5-6) entering an ALD page has a net number and a line name.

The net number is composed of the source page, the serial number of the source block, and the line origin of the source block. For example, BA301AD4 means that this line came from page BA301, from the block whose serial number is AD on that page, and from the fourth line position on that block. When an input line comes from more than one unit, such as one of many types of I/O devices, or from more than one storage unit, a pseudo-net number is put on the ALD net number position. These pseudo-net numbers are generally in sequence, starting at 000.

A net is a set of signal points (a source and sinks) which are electrically interconnected. Generally, the source point refers to the output pin of the driving block, and the sink points refer to the input pins at the driven blocks. The net identification indicates which points (pins) belong to a given network (Figure 5-13).

The line name is generally a description of the line function and is signed plus (+) or minus (–), depending on the active condition of the line at that point. If most of the lines in the machine are plus (+), the sign may not appear unless it is minus (–).

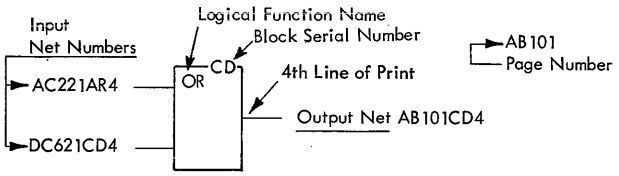


Figure 5-13. Identification of Nets

Output Line

On each output line (Figure 5-6) leaving the ALD page, the sink page number (where the line is going), the line name (with the sign of the active state of the line), and the line origin are printed.

The line origin is composed of the serial number of the last logic block before the line name and the number of the printing line of that block.

When the output line branches to several pages, the sink pages are listed below the line name.

In Figure 5-5, the top output line is "PP001–Ind Enable Storage Trg–BD4." The sink page number is "PP001" (the page where the line is going); the active state of the line is minus (–), and a description of the line would be "Ind Enable Storage Trg"; the source point is the logic block whose serial number is BD, and the line leaves the block at position 4.

COMBINATIONAL BLOCKS

Multiple blocks (Figure 5-14) are combined into "butted" or combinational blocks under the following conditions:

1. The blocks are all on the same card.
2. The interconnections between the blocks do not connect to any other block and no pins exist between the blocks.

The format of the block is similar to the standard block. The top and bottom lines, and line 3, are the same as the standard ALD block.

Two to seven blocks that are multiple inputs may be butted top to bottom as the left half of the butted block. Each of these blocks contains a function and a voltage code if there are physical pins (card pins).

The output block, the right half of the butted block, contains a function (line 2); output DOT data (line 3), if the output is DOTed; and a load/unload indicator (next-to-bottom line), if the output has a physical pin (card pin).

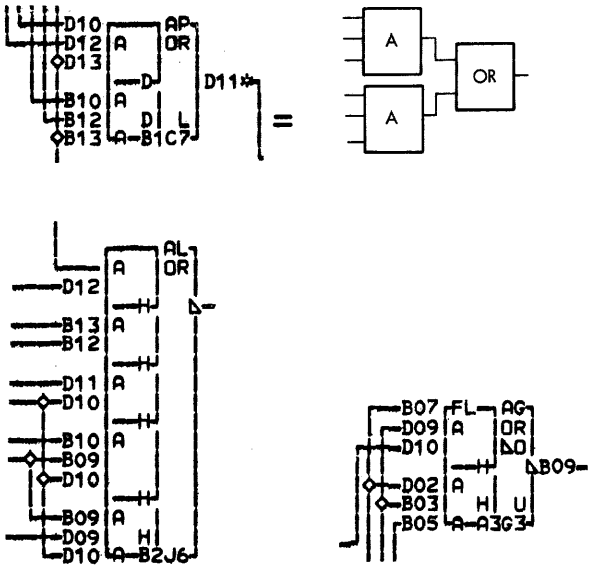


Figure 5-14. Butted Blocks

COMMENTS

Comments are at the bottom left of the page (Figure 5-15). As many as ten lines of comments may be listed.

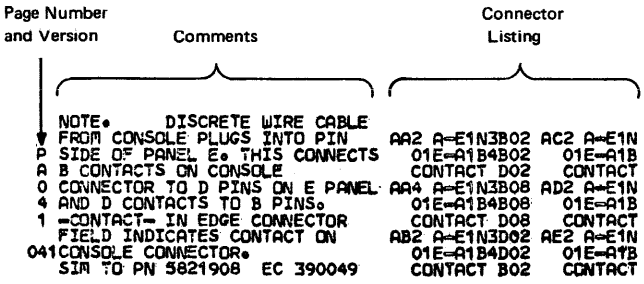


Figure 5-15. Comments Area

CONNECTOR AND RESISTOR LISTING

Connectors and resistors (Figure 5-3) are listed at the bottom center of the page. Space is provided to list 100 connectors or resistors. The general form of a logic connector or resistor is:

01	A-	D3	B2	D09
Frame	Gate	Board	Socket	Pin

SOCKET LISTING

The socket listing (Figure 3-19) is a physical layout of an SLT board showing the cards and cables used and their ALD page locations.

Each card and socket listing shows the ALD page for each portion or pin used. The unused portions or pins are also listed.

Each board has a summary listing which shows the cards and cables in part number order. Each part number has the ACC code, card type (as in the ALD block), sockets occupied, and total cards for the board. The unused sockets on the board are also listed.

Generally, the socket listing is at the beginning of the ALD's in Volume 0.

FEALD for MST

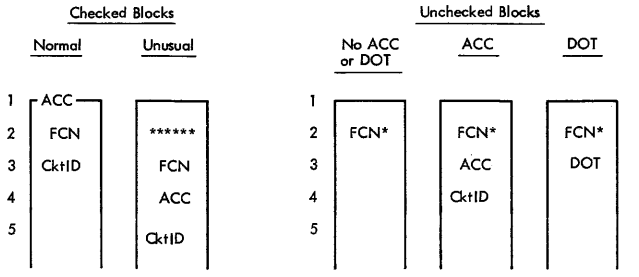
This section describes the Field Engineering Automated Logic Diagram for MST machines. Logic blocks, including the functional logic block, are defined in Chapter 2, "Standard Logic Blocks." The following text covers the content and layout of an FEALD (MST) page, and the system of direct addressing used on an FEALD (MST).

At the beginning of this chapter, it was mentioned that the FEALD program for MST machines can produce two types of FEALD's: a line-drawn FEALD and a direct-addressing FEALD. In appearance, the line-drawn FEALD is about the same as an FEALD for an SLT machine. Both have lines forming a direct connection between logic blocks. The title and comments area on a page are the same. However, the placement of information within a logic block differs in MST and SLT. For MST machines, line-drawn and direct-addressing FEALD's *may be intermixed.* Figure 5-28 is a direct-addressing FEALD (MST). Note three things about this page:

1. A system of direct addressing replaces the traditional line-connections between logic blocks. Direct addressing will be explained later.
2. This FEALD (MST) page is equivalent to three engineering ALD pages: ML051, ML061, and ML071. All this logic is on one card at EB4F2.
3. The page contains functional logic blocks: selector(SEL), register(REG), and decoder(DCD). Functional logic puts more logic in a given space than does unit logic (AND/OR/FF).

FEALD (MST) BLOCK

The placement of information on an FEALD (MST) logic block depends upon the type of block. Figure 5-16 summarizes the location of information in the several variations in an MST logic block. Information that has a fixed location is not in the figure. For example, the block serial is always at the top right of the block; card location is always at the bottom of a block. The following text specifies what is on each line of an FEALD (MST) logic block.



ACC Additive card code
FCN Logical function
CktID Circuit identifier or equivalent (resistance, capacitance, inductance, delay, etc.)
DOT Block is dot ANDed or dot ORed

Note: Block serial and card location are at fixed locations on a block.

Figure 5-16. FEALD (MST) Block–Variable Information

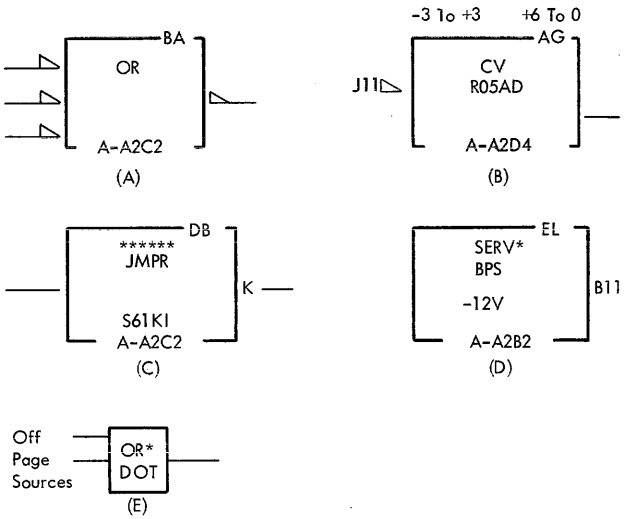


Figure 5-17. FEALD (MST) Block

Information Inside the Block

Line 1

Line 1 contains the additive card code (ACC) and block serial number. The additive card code appears on line 3 in unchecked blocks. The ACC may contain as many as four characters.

The block serial is a two-character alphabetic code at the right edge of line 1 (BA in example A, Figure 5-17). Because an FEALD can combine several engineering ALD pages, and as a result block serials can be duplicated, the block serial does not locate the position of a block on a page. Rather, the block serial locates information listed at the bottom of a page on an FEALD without direct addressing.

Lines 2 and 3

Line 2 contains the block function (OR in example A, Figure 5-17) or six asterisks. If asterisks occupy line 2, the block function moves to line 3. A row of asterisks indicates an unusual use of a circuit. A single asterisk after the block function indicates that the block is unchecked (example E, Figure 5-17) by the design automation program. A DOT block with an asterisk after the function indicates that all input lines come from off the page, or that a wedge conflict exists.

Line 3, which is generally blank, can contain:

1. The block function, if asterisks occupy line 2 (JMPR in example C, Figure 5-17). Asterisks in line 2 indicate an unusual condition or use of a circuit.
2. The · circuit number, which is printed for special reasons–a row of asterisks in line 2, or a circuit having no standard voltage code (CV in example B, Figure 5-17).
3. The additive card code on unchecked blocks (BPS in example D, Figure 5-17).

Line 4

Line 4 is generally blank but may contain a circuit number (S61KI in example C, Figure 2-36). In a service (SERV) block, line 4 contains voltage information (−12V in example D, Figure 5-17). Line 4 can contain the value of a capacitor or resistor block. As an alternative, the circuit number may appear in line 2. Groups of resistors may be represented by a single block (R) as long as they are on the same card. Block BD in Figure 5-28 is an example.

As an alternative, the next-to-last line of a block can contain the circuit number or value of resistance, capacitance, or inductance (Figure 5-18).

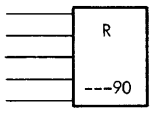


Figure 5-18. Resistor Block

Card Location

The bottom line of a block contains the card location (Figure 5-19), in the form A-ANAN, which represents gate, board, and card.

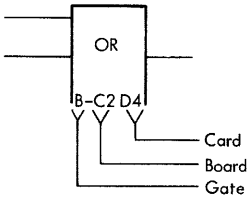


Figure 5-19. Card Location

Titles

A title may appear over a block (Figure 5-20) or over the output lines of a functional logic block, such as a register.

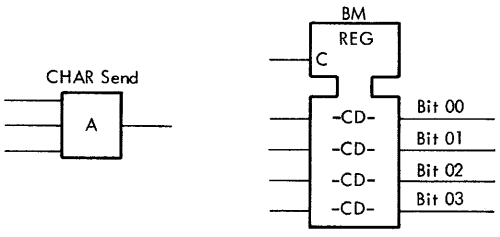


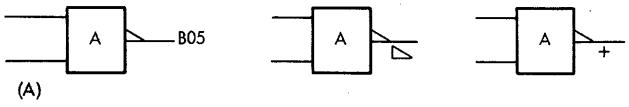
Figure 5-20. Block Titles

Wedge and Plus Sign

Generally, a wedge on an FEALD (MST) means the same as on engineering ALD's or other FEALD's—a wedge at an input or output represents the least positive potential of a line with respect to the most positive potential.

On an FEALD (MST), a wedge under an output line (Figure 5-21) indicates that the output can be forced to its least positive potential by some external source. Similarly, a plus sign under an output line means that the output can be forced to its most positive potential by an external source.

In example B, Figure 5-21, outputs K and M are forced to their least positive potential when the AND circuit is active, regardless of any inputs to the register. Outputs J and L are not affected by the AND circuit.



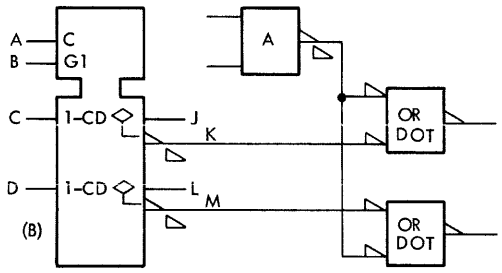


Figure 5-21. Wedges and Plus Sign

Output Loading

When an externally loaded circuit cannot be isolated from the driving circuit without affecting the output of the driver, a loading character (L or U) indicates this external load. The loading character (Figure 5-22) is under the polarity indicator (wedge) of the active output.

If the output is loaded, an L or no character may appear. If the output is unloaded, the character U always appears. When a branch occurs within a block, the loading character (U) is associated only with the output immediately above the character.

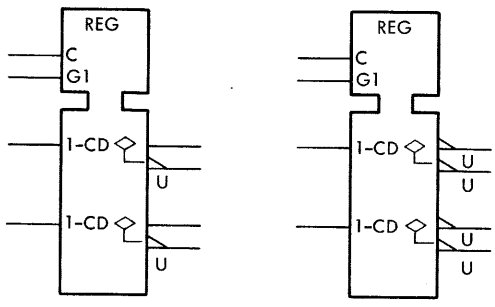


Figure 5-22. Output Loading

Card I/O Pins, Module Pins, and Voltage Codes

Associated with an input or output of a logic block is a 3-character pin field that identifies a card I/O pin (Figure 5-23). An *input* can be prefixed by an additional alphabetic character (T in example A) that specifies the minimum up level and minimum down level of a circuit. Figure 5-24 shows the voltage codes and ranges available on an FEALD (MST).

Note that the letter T at the output of a logic block identifies a test point (Example B in Figure 5-23).

Card coordinates were described in Chapter 4 (Figure 4-5). These coordinates, along with an FE template, locate module pins for scoping. Module pins are identified as in example C of Figure 5-23. Note that .09B is a module pin, whereas B09 represents a card I/O pin, at the input or output of a logic block on an FEALD (MST).

Card coordinates for TTL circuits (Figure 4-6) are slightly different in that the first digit defines a region on the card, and the next three digits define the column and row.

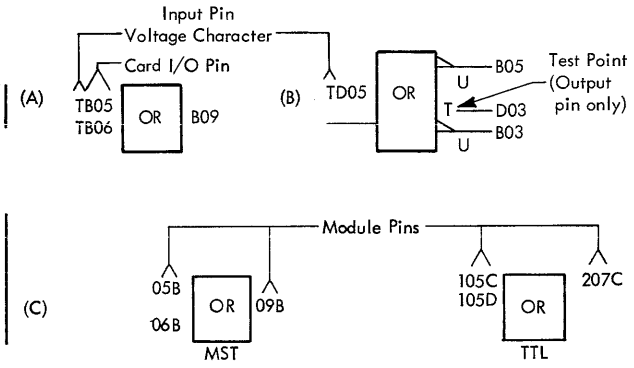


Figure 5-23. Card I/O Pins and Module Pins

Code	Minimum Up Level (Volts)	Minimum Down Level (Volts)
B	2.5 to 2.1	1.9 to 1.5
C	2.5 to 2.1	1.4 to 1.0
D	1.9 to 1.6	1.4 to 1.0
E	2.0 to 1.6	0.9 to 0.6
F	4.0 to 3.5	0.5 to 0.3
G	2.5 to 2.1	0.5 to 0.3
H	2.0 to 1.6	0.5 to 0.3
J	1.5 to 1.1	0.5 to 0.3
L	0.7 to 0.5	0.4 to 0.2
T	0.3	-0.3
Z	-1.0	-1.5

Figure 5-24. Voltage Codes–FEALD (MST)

Edge of Block Character

An edge of block character, alongside or in the edge of an FEALD (MST) block (Figure 5-25), serves the following functions:

Example A	E	An extender. In combination with a K output, shows that additional blocks act as inputs to the first block.
Example A	K	At the output of a block, a K can connect to another K output or to an E output; these K "outputs" are actually inputs to the first block (with the output E) and extend its function.
Example B	K	At times, the number of inputs to a logic block exceeds design automation program capabilities. In this case, the excess inputs are shown as outputs but identified with the letter K.
Example C	X	A nonlogic input or output. The driving circuit to this input is usually a fixed voltage or bias. An X line does not influence the state of a circuit.
Example D	P	A positive-going shift or pulse activates the block.
Example E	N	A negative-going shift or pulse activates the block.
Example B	T	A test point. Do not confuse this with T as an input voltage character. See output pin D03 in example B, Figure 5-23.

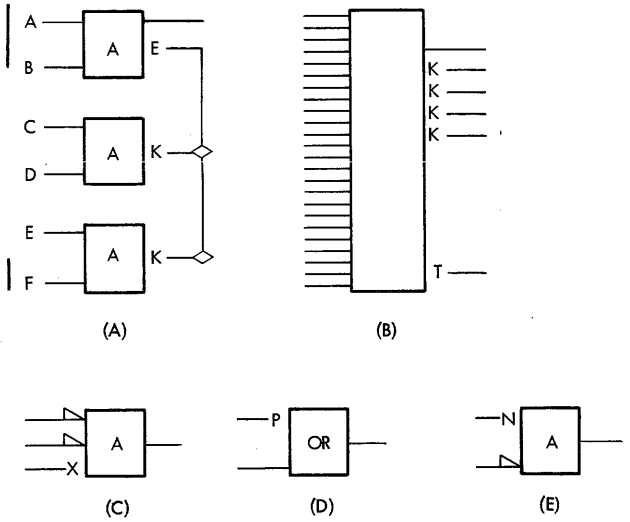


Figure 5-25. Edge of Block Character

FEALD (MST) PAGE

Figure 5-26 shows, from right to left, the six types of information at the bottom of an FEALD (MST) page:

1. Page numbers and page version
2. Title block
3. Engineering ALD pages, version, and EC level
4. Card location and type
5. Connector and resistor listing
6. Comments

Page Number

A range of page numbers represented by the FEALD (MST) is shown in the upper right, lower left, and lower right corners. In the example, the range is ML051 to ML071. A line-drawn FEALD (MST) has a single page number, that of the engineering ALD it represents.

Occasionally, two FEALD (MST) pages are required to present the logic for a machine function. On the two-page, direct-addressing FEALD, both pages have the same group page number, part number, and edge connector list, but each page is designated Page 1 of 2 or Page 2 of 2. Logically, these two form one FEALD page. Page 1 contains the left edge lines; page 2 contains the right edge lines. Everything else is consistent with a one-page FEALD.

Below the page numbers is the version of the FEALD. This version takes the alphameric form ANN (A01, for example) if the corresponding ALD pages contain more than one version and all are on the FEALD (MST).

Title Block

The title block identifies the page part number and logical function, the machine name and frame, the IBM division that released the machine, the EC history, and the last EC and its date.

ALD Pages and Version

To the left of the title block are listed the engineering ALD pages comprising the FEALD (MST), along with the version and EC number for each page. Version 000 is the basic design. A version represents cards and wiring not on the basic design.

The version of the FEALD page is at the lower right corner, under the FEALD page range. If the engineering ALD pages have different versions, the version of the FEALD page takes the form ANN (A01, for example).

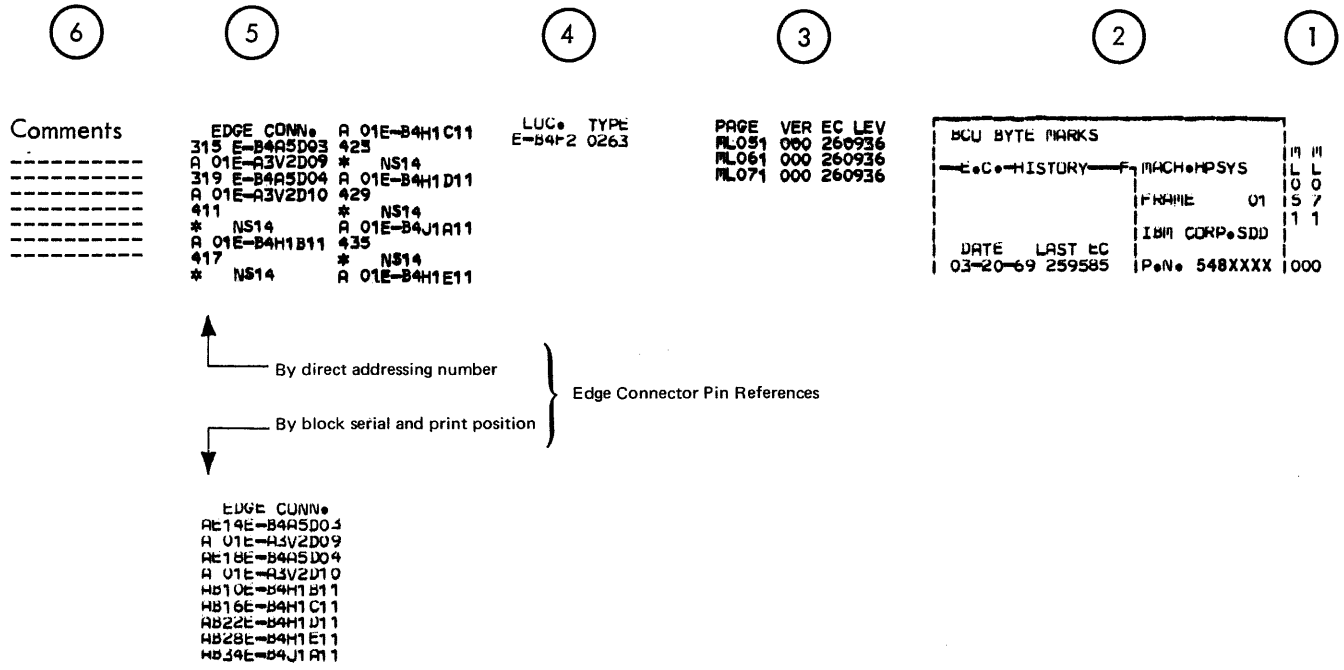


Figure 5-26. FEALD (MST) Page Data

Card Location and Type

To the left of the engineering ALD page list are the card types and locations for those cards represented by this FEALD (MST). Consult the socket listing for the part number of a card.

Connector Listing

There are two methods of referencing from an FEALD (MST) logic pin to an edge connector listed at the bottom of the FEALD page. On a direct-addressing FEALD, a direct-addressing number is the reference; on a line-drawn FEALD (MST), the block serial and vertical print position are used as reference.

In the direct-addressing FEALD (MST) of Figure 5-28, the output from a block is designated: G02*315. The asterisk identifies this pin (G02) as one connected to an edge connector. The 315 is a direct-addressing number. Example 5 of Figure 5-26 shows the edge connector listing on this FEALD, which indicates that pin G02 connects to a connector at gate E, board B4, card A5, pin D03. (See the first line in the list, direct-addressing number 315.)

The lower part of example 5 is a connector listing arranged by block serial and print position, as it would be for a line-drawn FEALD (MST). A pin, at block serial AE print position 14, connects to a connector at E-B4A5D03.

Resistor Listing

If an output pin or input net has an asterisk (*), resistors may be listed at the bottom of an FEALD (MST) page, in which case the word "resistor" appears below the block serial. If an FEALD represents more than one engineering ALD page (and therefore uses direct addressing), resistors are not listed; instead, an R block contains those resistors on the card.

Comments

Comments appear at the extreme left bottom of an FEALD (MST) page.

DIRECT ADDRESSING

Direct addressing is a method of connecting logic blocks that eliminates the traditional line-connections between blocks. Figure 5-28 is a typical FEALD (MST), annotated to demonstrate right-to-left tracing of logic.

The logic block area consists of columns of information:

1. A column of input line names and nets
2. Five (or less) columns of logic blocks and connections
3. A column of output line names and nets

On an FEALD (MST), logic blocks and line names are "connected" by a direct-addressing key, which is a three-digit number common to two or more blocks or points on a page. The main significance of this number is that it defines the location of the *output* of a block. Of the three digits, the first specifies one of five columns, the last two specify one of 92 vertical print positions. In Figure 5-28, the key 311 means that this line exits from a block in column 3, eleven lines from the top of the page. Note that the column of input line names at the left edge of the page might be considered column 0, with 0's suppressed in printing.

At the right edge of a page, line names and nets are grouped according to the engineering ALD page number, (ML051, ML061, ML071) and within the page by net serial and ALD page destination. Because net serials (EB6 in the example) may be duplicated on an FEALD (MST) page, it is important to enter from the right at the correct ALD page (ML061 in the example). The net serial no longer references a logic block on an FEALD (MST) as it did in SLT/SLD, but merely crossreferences nets between pages.

At the left edge of an FEALD, input lines are arranged sequentially from top to bottom by the engineering ALD page, and within a page by net serial.

Figure 5-29 shows logic being traced from left to right. Because the output of a block can go to several other blocks on a page, a logic-column key (Figure 5-27) points to those columns where a given output line goes, and shows the number of connections to each column.

A diamond (◇) symbol means that the output of a block goes to an off-page line name and net (example B, Figure 5-27).

Example C in Figure 5-27 illustrates a logic-column key for a two-page FEALD (MST), which consists of eight columns of logic, divided 4-4, on two pages.

Because there are no restrictions on the placement of blocks on a page, any output from any column can go to any other column. For example, in Figure 5-29 line 460 in column 4 loops back twice within column 4 and also goes to an off-page line name. If required by logic, this same line could loop to any of the other three columns.

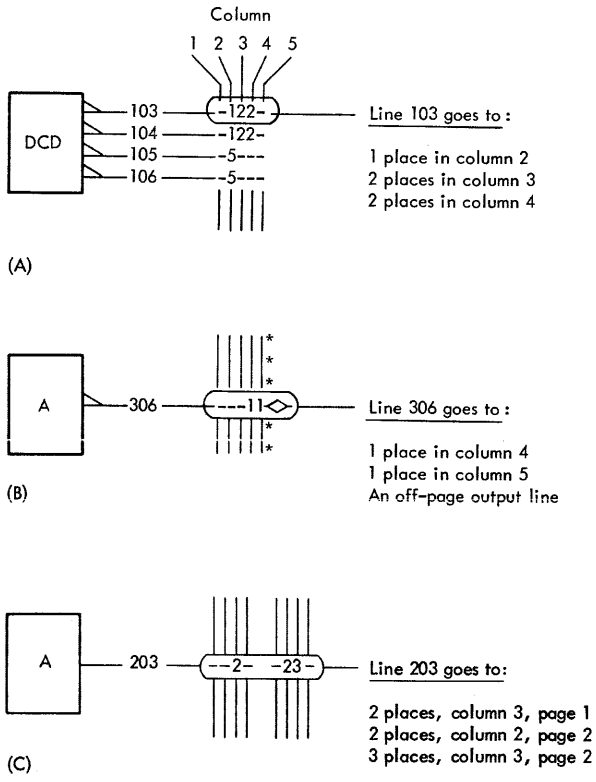


Figure 5-27. Logic-Column Key

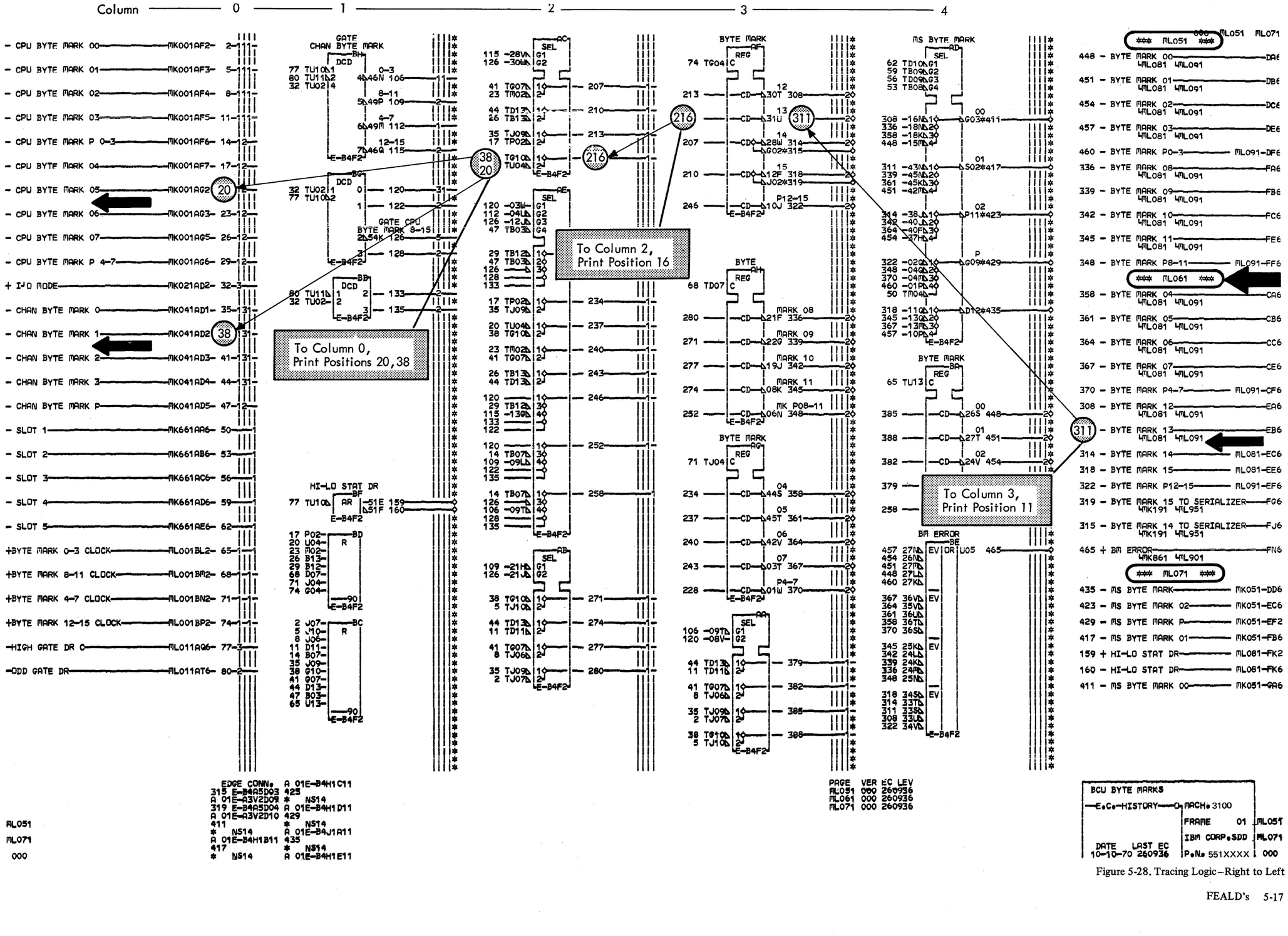


Figure 5-28. Tracing Logic–Right to Left

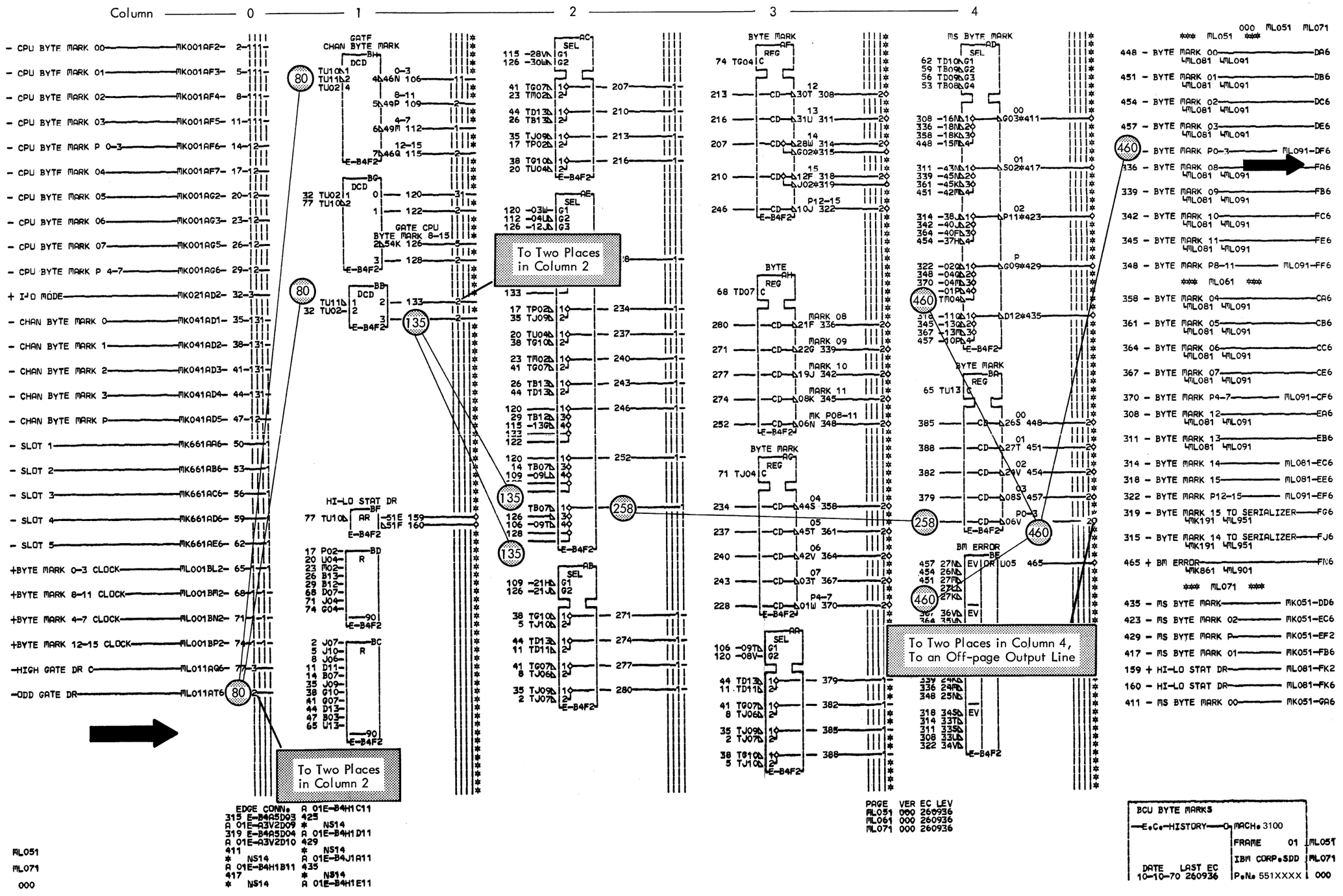


Figure 5-29. Tracing Logic–Left to Right

Basic refers to the standard design of the machine; it includes optional features (MFI's) if drawn as part of the standard logic page. "Basic" is in contrast to "Version."

Circuit Number consists of five alphameric characters which uniquely define a particular basic circuit.

Design Automation refers to the programs that prepare and print the ALD's. They consist of four major stages of processing: logic master tape, simulation, packaging and checking, and physical master tape. The outputs consist of documents to aid engineering in the development of computers, release documents (ALD's), and tapes for manufacturing.

DOT Block is an ALD block used on ALD logic pages to show DOT AND and DOT OR functions, which are physically accomplished by tying two signals together at a pin. Thus, one logical net on the ALD is combined with other logical nets by the DOT block to produce one combined physical net.

Note: One DOT block does not connect to another DOT block.

Grouping refers to the associating of certain circuit configurations prior to partitioning. Circuits represented on the ALD's by more than one block but always on the same card are said to be in the same group.

Logic Master Tape (LMT) is the machine language record in logic page order. Each time a portion of this machine record is altered, logic pages containing the changes are produced for the engineer.

Net is a complex of nodes, normally pins or connectors on the ALD, all common electrically.

Net Number consists of the source block page number, block serial number, and output line position of the source block. It consists of eight alphameric characters of the form AANNNAAB (A is alphabetic, N is numeric, and B is either alphabetic or numeric).

Node is one circuit end point of a net (such as a pin on a card or a connector on a board).

Packaging and Checking refers to a series of programs that aid the engineer in the physical packaging of the logic and check data that is manually inserted on the pages.

Partitioning refers to that part of the design automation program that separates logic into cards and assigns the cards to boards.

Physical Master Tape (PMT) is a machine language record of the physical aspects of the design. It is arranged in physical sequence. Its purpose is to retain in a convenient form the physical data from LMT, as well as the physical data from the PMT (wiring data primarily), to retain the physical design at a fixed level while the logical design is undergoing change, and to extract information from the tapes at the request of the engineer or other users.

Pins are the male parts of the connection between card and board or between cable connector and board.

Portion refers to those circuits on a card that are connected by printed wiring.

Signal Name is the title (may be blank) that gives meaning to a logical net; each net has only one signal name.

Simulation refers to programs that allow the engineer to exercise the logic dynamically before the machine is packaged.

Sink is the end or ends of a net to which signals flow.

Source is the beginning of a net from which signals flow.

Symbolic Package is two characters to be used by design automation in the partitioning and placement programs. Blocks with the same characters in the symbolic package field are placed on the same board by the card partitioning program.

Note: Blocks with different symbolic packages may be placed on the same board.

Version is a term used by design automation and indicates the particular manner in which logic records are kept for certain features; a feature is a version of its records and is kept as an add-delete (by block) to the basic records.

Note: "Version" gives automatic or implied updating of the feature by the basic page, because an added basic block is, in effect, in the version.

Version Page is the ALD page made up of all blocks on the basic page which appear unchanged in the version design, plus additional version blocks needed to change the basic page into the version page.

Via Hole is a plated-through hole which may or may not contain a pin; it is used to make contact between conducting layers of the board. It is not a node.

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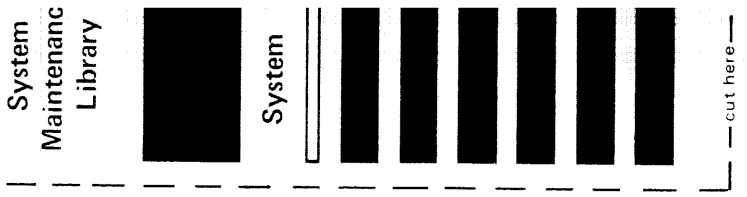

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