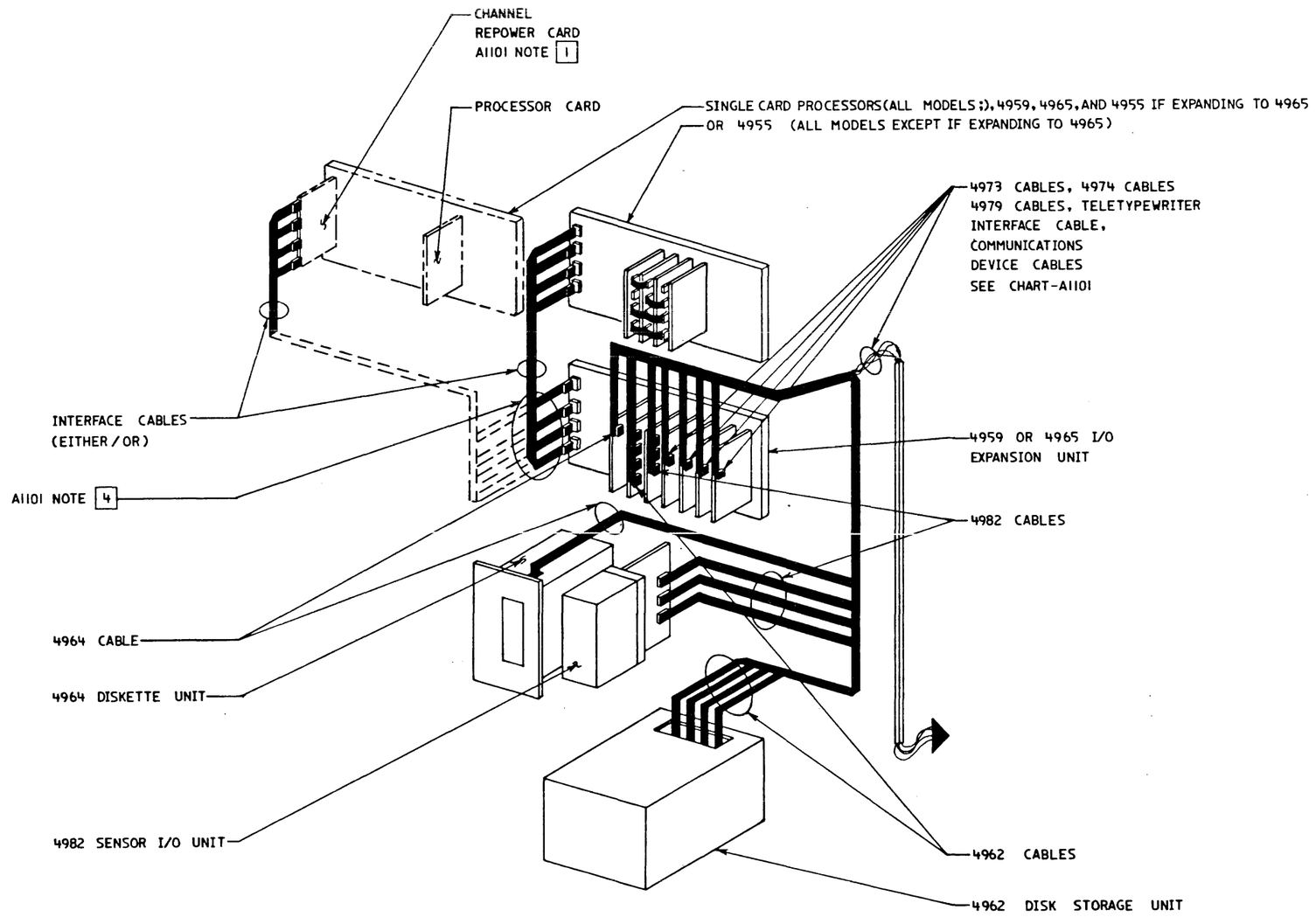


TYPICAL RACK CABLING

	EC HISTORY		DRAWING TITLE
HIST	30 JUL 81	994400	I/O CABLE CHART
RED	24 NOV 81	466795	MACH SERIES/1
	16 MAR 82	997238	PART NO 8326721
D	17 JUN 82	329851	CLASSIFICATION
			IBM CORP

A1100

A1100

A1101

CABLE IDENTIFICATION CHART

CABLE P/N	D C	DESCRIPTION	FEAT. D/C	DESCRIPTION
0984023	5700	30 (9,1) FT - 4973 EXTENDED CABLE	5630	4973 PRINTER ATTACHMENT
0984024	↑	40 (12,2)	↑	↑
0984025	↕	50 (15,2)	↕	↕
0984026	↕	60 (18,3)	↕	↕
0984027	↕	70 (21,3)	↕	↕
0984028	↕	80 (24,4)	↕	↕
0984029	↕	90 (27,4)	↕	↕
0984030	↕	100 (30,5)	↕	↕
0984031	↕	110 (33,5)	↕	↕
0984032	↕	120 (36,6)	↕	↕
0984033	↕	130 (39,6)	↕	↕
0984034	↕	140 (42,7)	↕	↕
0984035	5700	150 (45,7) FT - 4973 EXTENDED CABLE	5630	4973 PRINTER ATTACHMENT
1632206	2060	BSC V35/H.S. DDN CABLE	2075	BSC SINGLE LINE CONTROL (H.S.)
1632207	5721	20 (6,1) - 4974 BASIC ATT. CABLE	5620	4974 PRINTER ATTACHMENT
1632208	2057	EIA DATA SET CABLE	1310	MULTI-FUNCTION ATTACHMENT
			1610	ASYNCHRONOUS COMMUNICATIONS SINGLE LINE CONTROL
			2074	BSC SINGLE LINE CONTROL
			2090	SDLC SINGLE LINE CONTROL
			2092	ASYNCHRONOUS COMMUNICATIONS-4 LINE ADAPTER
			2094	BSC-4 LINE ADAPTER [2]
			2096	PROGRAMMABLE COMMUNICATIONS-4 LINE ADAPTER
1632209	2055	TTY 20 (6,1) FT CABLE	7850	TTY ATTACHMENT
1632210	2058	BSC/HIGH SPEED CABLE	2075	BSC SINGLE LINE CONTROL (H.S.)
1632211	2056	ASYNCHRONOUS, LOCAL COMMUNICATIONS, CABLE	1310	MULTI-FUNCTION ATTACHMENT
			1610	ASYNCHRONOUS COMMUNICATIONS SINGLE LINE CONTROL
			2092	ASYNCHRONOUS COMMUNICATIONS - 4 LINE ADAPTER [2]
			2096	PROGRAMMABLE COMMUNICATIONS - 4 LINE ADAPTER
1632919	2944	JAPANESE EIA DATA SET CABLE	2057	EIA DATA SET CABLE
1632924	2064	TTY TO EIA DIR. CONN (MALE)	7850	TTY ATTACHMENT
1633096	----	COMMUNICATIONS CROSS-OVER CABLE	2091	ASYNCHRONOUS COMMUNICATIONS - 8 LINE CONTROL
			2093	BSC - 8 LINE CONTROL
			2095	PROGRAMMABLE COMMUNICATIONS - 8 LINE CONTROL [2]
1634981	5701	20 (6,1) - 4973 BASIC ATT. CABLE	5630	4973 - PRINTER ATTACHMENT
1727744	2724	U.K. MODEM ADAPTER CABLE	2057	EIA DATA SET CABLE
4411751	2065	TTY TO EIA DIR. CONN (FEMALE)	7850	TTY ATTACHMENT
4412661	5741	20 (6,1) FT - 4979 BASIC CABLE	3585	4979 VIDEO ATTACHMENT
4412662	5740	30 (9,1) FT - 4979 EXTENDED CABLE	3585	4979 VIDEO ATTACHMENT
4412663	↑	40 (12,2) FT	↑	↑
4412664	↕	50 (15,2) FT	↕	↕
4412665	↕	60 (18,3) FT	↕	↕
4412666	↕	70 (21,3) FT	↕	↕
4412667	↕	80 (24,4) FT	↕	↕
4412668	↕	90 (27,4) FT	↕	↕
4412669	↕	100 (30,5) FT	↕	↕
4412670	↕	110 (33,5) FT	↕	↕
4412671	↕	120 (36,6) FT	↕	↕
4412672	↕	130 (39,6) FT	↕	↕
4412673	↕	140 (42,7) FT	↕	↕
4412674	5740	150 (45,7) FT - 4979 EXTENDED CABLE	3585	4979 VIDEO ATTACHMENT
4412703	5720	30 (9,1) FT - 4974 EXTENDED CABLE	5620	4974 PRINTER ATTACHMENT
4412704	↑	40 (12,2) FT	↑	↑
4412705	↕	50 (15,2) FT	↕	↕
4412706	↕	60 (18,3) FT	↕	↕
4412707	↕	70 (21,3) FT	↕	↕
4412708	↕	80 (24,4) FT	↕	↕
4412709	↕	90 (27,4) FT	↕	↕
4412710	↕	100 (30,5) FT	↕	↕
4412711	↕	110 (33,5) FT	↕	↕
4412712	↕	120 (36,6) FT	↕	↕
4412713	↕	130 (39,6) FT	↕	↕
4412714	↕	140 (42,7) FT	↕	↕
4412715	5720	150 (45,7) FT - 4974 EXTENDED CABLE	5620	4974 PRINTER ATTACHMENT
6844552	5770		1310	MULTI-FUNCTION ATTACHMENT
8326751	5760	10 (3,05) FT 5250 IDS ATTACHMENT CABLE	1210	IDS ATTACHMENT FEATURE
8327455	2061	20 (6,1) FT PC 20 MA I-LOOP CABLE	2096	PROGRAMMABLE COMMUNICATIONS - 4 LINE ADAPTER
6031258	2071	20 (6,1) FT TELEPHONE COMM CBL/VCA	7881	TELEPHONE COMMUNICATION FEATURE
6839455	2066	50 (15,2) FT 3101 CABLE CURRENT LOOP	7850	TTY ATTACHMENT
↕	↕	↕	2096	FPMLC 4 LINE ADAPTER
			4704	TTY ADAPTER (4987)
6839455	2066	50 (15,2) FT 3101 CABLE CURRENT LOOP	4734	TTY ADAPTER (4987)
6845570	2070	20 (6,1) FT TELEPHONE COMM CBL / DAA	7881	TELEPHONE COMMUNICATIONS FTR
1632206	2060	V.35 H.S. DDN CABLE	2075	BSC SINGLE LINE CONTROL (HS)
			2080	SYNC COMM CTRLR (HS)
6844126	2067	32.8 (10.0) FT X .21 CABLE	2080	SYNC COMM CTRLR (HS)
4498426		TWINAX	1400	LOCAL COMM CONTROLLER
2577672		COAX (INDOOR)	1400	LOCAL COMM CONTROLLER
1833108		COAX (OUTDOOR)	1400	LOCAL COMM CONTROLLER

WRAP-BACK TOOLS

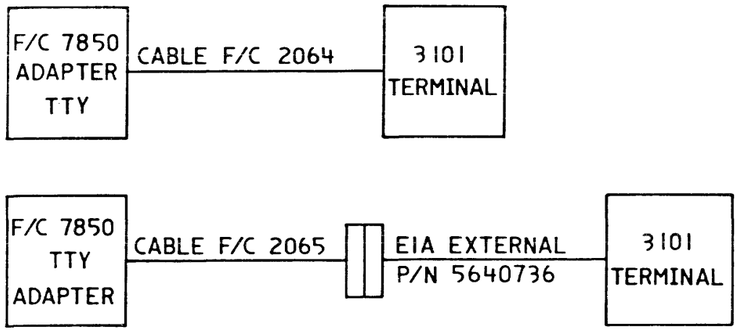
TOOL P/N	REQ'D FOR D/C
1633810	2058
1633811	2056
1633812	2060
1633834	2055
	2064
	2065
2704136	2057
6846868 NOTE [5]	
2722052	2944
4413770 NOTE [3]	2057
6825399	2061
6844547	5770
4468531	7880
6844226	2080

NOTES:
1. CHANNEL REPOWER CARD (D/C 1565): USAGE - OPTIONAL ON 4955 A-E: REQUIRED ON ALL OTHER PROCESSORS, 4959, 4965 AND 4955 IF GOING TO 4965
2. "ASYNCHRONOUS COMMUNICATIONS" ALSO KNOWN AS "START/STOP"
3. THIS TOOL PRESENT ONLY WITH FEATURE CODES 2092 & 2094. THIS P/N 4413770 (QTY 16) SHOULD BE JUMPERED FROM PINS 4 THRU 5,6 THRU 20 ON SPECIFIED CABLE FOR INITIAL INSTALLATION CHECK-OUT
4. "A" SLOT OF 4959 MAY CONTAIN D/C 7900 ATTACHMENT CARD
5. THIS TOOL REQUIRED FOR FEATURE CODE 1310 MULTI-FUNCTION ATTACHMENT WHEN USED WITH CABLE D/C 2057

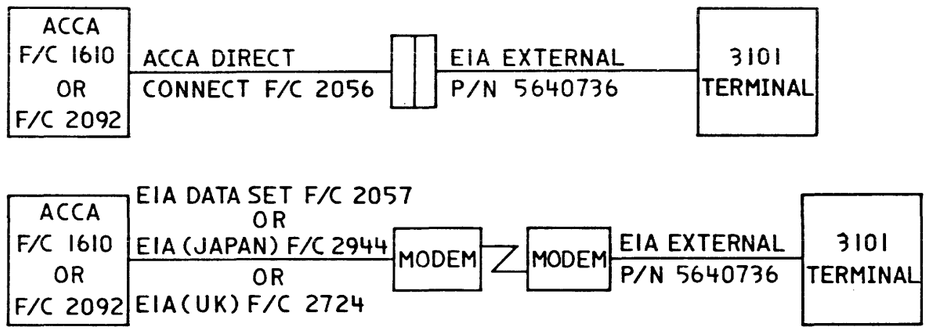
EC HISTORY		DRAWING TITLE	
17DEC81	466795	I/O CABLE CHART	
16 MAR 82	997238	MACH SERIES/1	
17 JUN 82	329851	PART NO 4745798	
		CLASSIFICATION	IBM CORP

D

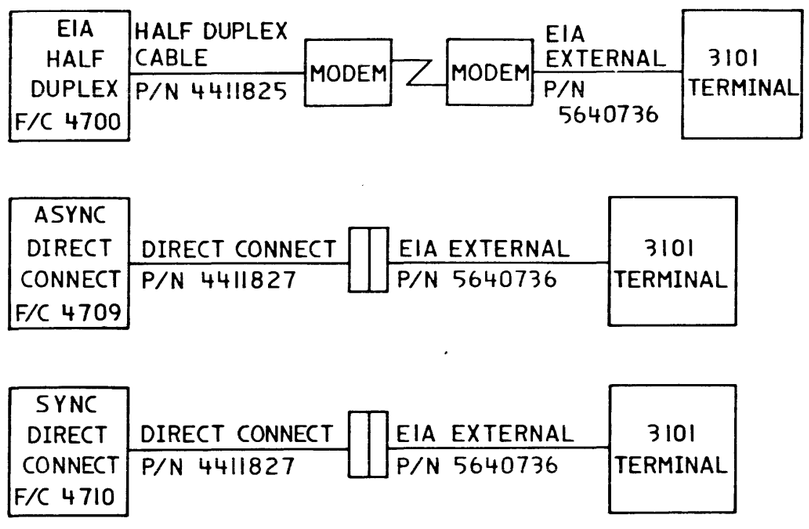
TELETYPEWRITER F/C 7850



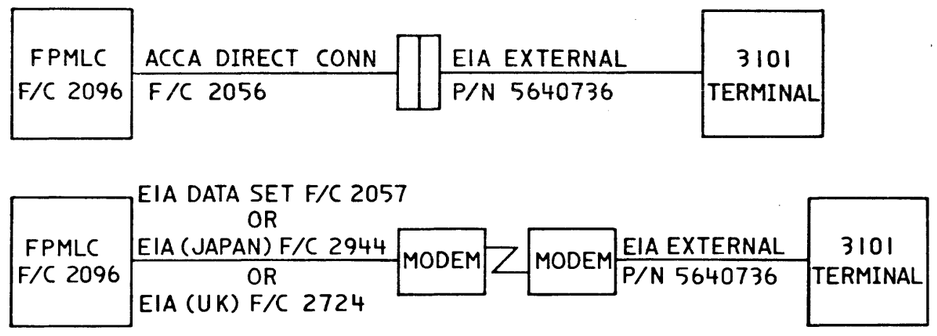
ASYNCHRONOUS COMMUNICATIONS F/C 1610, AND ASYNCHRONOUS COMMUNICATIONS (MULTI-LINE) F/C 2091/2092



PROGRAMMABLE COMMUNICATIONS SUBSYSTEM TYPE 4987



FEATURE PROGRAMMABLE MULTI-LINE COMMUNICATIONS F/C 2095/2096



NOTE:

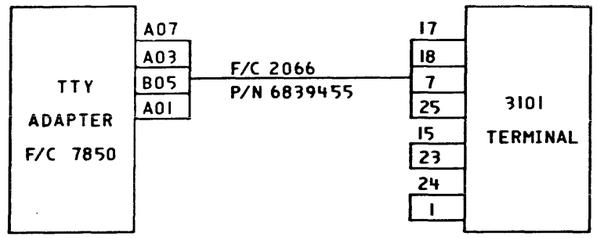
ALSO SEE GENERAL INFORMATION ON A1202

EC HISTORY		DRAWING TITLE
19SEP79	375342A	3101 TO SERIES I INTERFACES
24 NOV 81	466795	MACH RS232C
16 JUN82	329851	PART NO 6840609
		CLASSIFICATION

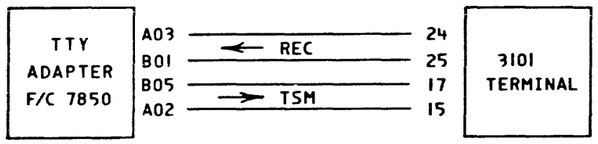
C

IBM CORP

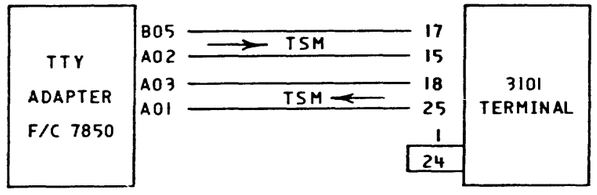
TELETYPEWRITER F/C 7850



CONNECTION WITH 3101 SUPPLYING
ALL CURRENT



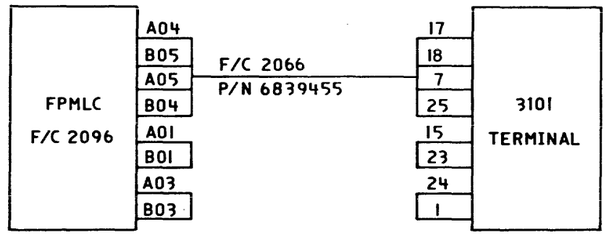
CONNECTIONS WITH TTY ADAPTER
F/C 7850 SUPPLYING ALL CURRENT.
CABLE NOT SUPPLIED



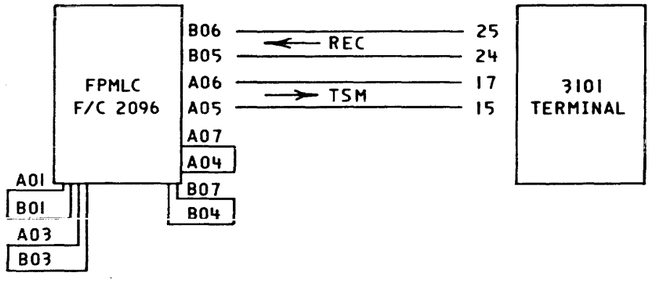
CONNECTIONS WITH EACH END
SUPPLYING ITS TSM LOOP CURRENT.
CABLE NOT SUPPLIED

NOTE:
ALSO SEE GENERAL INFORMATION ON A1202

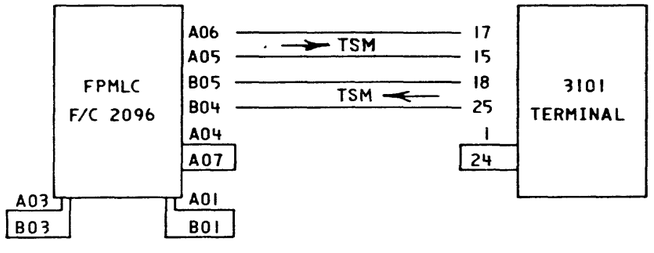
FEATURE PROGRAMMABLE MULTI-LINE COMMUNICATIONS



CONNECTION WITH 3101 SUPPLYING
ALL CURRENT

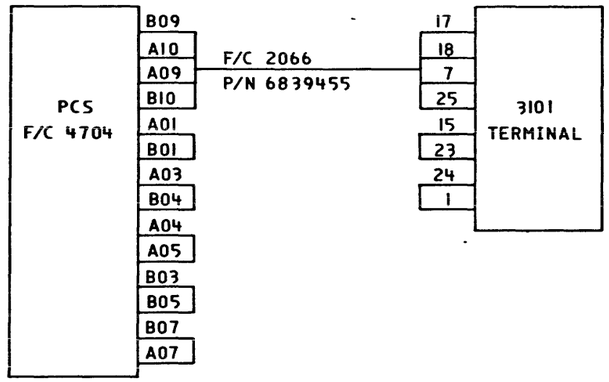


CONNECTION WITH FPMLC ADAPTER
F/C 2096 SUPPLYING ALL CURRENT.
CABLE NOT SUPPLIED



CONNECTIONS WITH EACH END
SUPPLYING ITS TSM LOOP CURRENT.
CABLE NOT SUPPLIED

PROGRAMMABLE COMMUNICATIONS SUB-SYSTEM 4987



CONNECTIONS WITH 3101 SUPPLYING
ALL CURRENT.
PCS DOES NOT HAVE A CURRENT
SUPPLYING CONFIGURATION

EC HISTORY		DRAWING TITLE
19SEP79	375342A	3101 TO SERIES 1 CURRENT LOOP INTERFACE
24NOV81	466795	MACH SERIES 1
17 JUN 82	329851	PART NO 6840610
C		CLASSIFICATION

IBM CORP

A1201

GENERAL INFORMATION
SERIES 1 TO 3101 TERMINAL INTERCONNECT

1. IF CARRIER DETECT IS UP TO THE 3101 ALL THE TIME (S/1 ATTACHMENT JUMPERED FOR PERMANENT RTS), THEN THE 3101 HAS TO HAVE 'PRTS' SWITCH ON TO BE ABLE TO SEND DATA. (EIA OPERATION.)

2. WHEN THE 3101 'CRTS' SWITCH ON, RTS IS BROUGHT UP WHEN FIRST KEY IS DEPRESSED AND KEEPS IT UP UNTIL EOT/ETX (DEPENDS ON THE 3 SWITCH SETTING) IS SENT (EIA OP).

3. WITH CURRENT LOOP OPERATION, THE ONLY SWITCH ON THE 3101 WHICH AFFECTS THE OPERATION OF THE XMIT/REC DATA IS THE 'FDX' SWITCH. WHEN THIS IS ON, IT REQUIRES THE S/1 ATTACHMENT TO ECHO THE DATA.

4. IF OPERATING THE 3101 IN 'FDX' MODE (ECHOPLEX) WITH FPMLC ATTACH., RTS SHOULD BE JUMPERED ACTIVE ON THE FOUR LINE CARD SO AS TO PROVIDE CARRIER DETECT TO THE 3101. THIS ALLOWS THE ECHOED DATA TO BE RECEIVED BY THE 3101 (EIA OPERATION).

5. IF OPERATING THE 3101 IN 'FDX' MODE (ECHOPLEX) WITH THE PCS DIRECT CONNECT, THE SERIES/1 PROGRAM OR PCS FUNCTION STRING HAS TO ENSURE THAT CARRIER DETECT IS ACTIVE TO THE 3101 (EIA OPERATION).

6. THE TTY ATTACHMENT ALWAYS ECHOES THE DATA AND XMITS 2 STOP BITS.

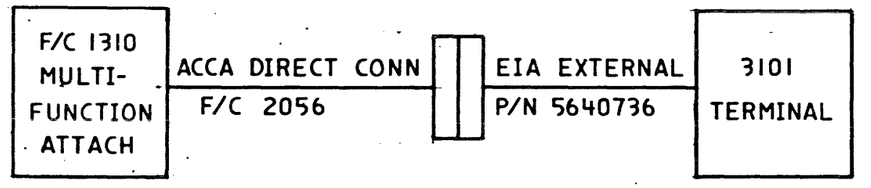
7. WHEN USING THE TTY ATTACHMENT IN CURRENT LOOP MODE, THE TTY CARD SHOULD BE JUMPERED FOR ISOLATED CURRENT LOOP TO ALLOW THE 3101 TO SUPPLY THE CURRENT.

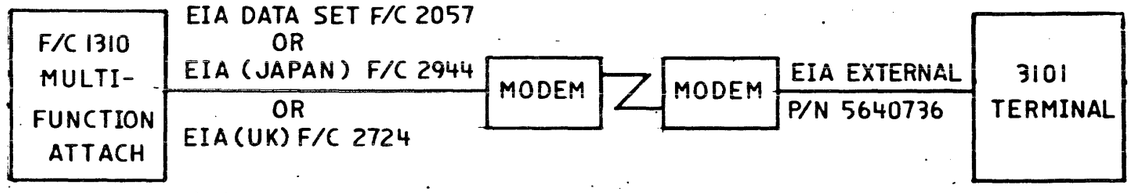
8. SINGLE LINE AND MULTILINE ACCA CANNOT ECHO THE DATA SO SHOULD OPERATE WITH THE 3101 'HDX' SWITCH ON AND 'PRTS' SWITCH ON, AND THE SERIES 1 ADAPTER JUMPERED FOR RTS ALWAYS ON.

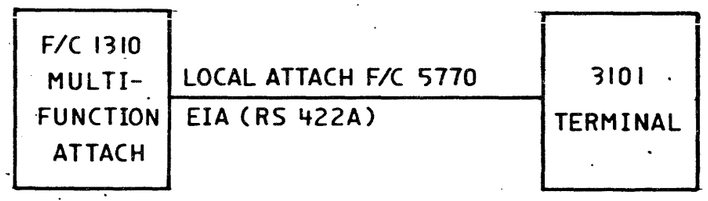
9. WHEN USING THE SINGLE LINE AND MULTILINE ACCA, THE SERIES 1 DATA HAS TO BE THE MIRROR IMAGE OF THE ASC II CHARACTERS USED BY THE 3101 (I.E., AN ASC II ETX=03, IN SERIES/1 IT IS = C0 WITH EVEN OR NO PARITY; OR C1 ODD PARITY).

10. ACCA SINGLE STOP BIT RPQ D02236 SAME AS F/C 1610 EXCEPT FOR STOP BIT SWITCH SETTING ON THE 3101

MULTI-FUNCTION ATTACHMENT F/C 1310







EC HISTORY		DRAWING TITLE	
19SEP79	375342A	3101 TO SERIES 1 INTERFACES	
24NOV81	466795	MACH RS 232C	
17 JUN 82	329851	PART NO 6840611	
		CLASSIFICATION	IBM CORP

B

A1202

4955 MOD F00 PROCESSOR BOARD

STANDARD CHANNEL	ADDR EXP CARD Q	OUT STG N P	OUT STG M	IN STG L	ROS CARD K	ADDR CARD J	DATA CARD H	DIR	I/O CARD(S) B C D E F G FLT PNT CARD G	ROW A *	CABLE BOARD TO BOARD
- ADDR BUS BIT--00---	----	---	---	---	-----	-G02-	-----	<-->	--B02--	-A2B02-	-A2B02
- ADDR BUS BIT--01---	----	---	---	---	-----	-G03-	-----	<-->	--B03--	-A2B03-	-A2B03
- ADDR BUS BIT--02--	----	---	---	---	-----	-G04-	-----	<-->	--B04--	-A2B04-	-A2B04
- ADDR BUS BIT--03---	----	---	---	---	-----	-G05-	-----	<-->	--B05--	-A2B05-	-A2B05
- ADDR BUS BIT--04---	----	---	---	---	-----	-G07-	-----	<-->	--B07--	-A2B07-	-A2B07
- ADDR BUS BIT--05---	----	---	---	---	-----	-G08-	-----	<-->	--B08--	-A2B08-	-A2B08
- ADDR BUS BIT--06---	----	---	---	---	-----	-G09-	-----	<-->	--B09--	-A2B09-	-A2B09
- ADDR BUS BIT--07---	----	---	---	---	-----	-G10-	-----	<-->	--B10--	-A2B10-	-A2B10
- ADDR BUS BIT--08---	----	---	---	---	-----	-J02-	-----	<-->	--B12--	-A2B12-	-A2B12
- ADDR BUS BIT--09---	----	---	---	---	-----	-J04-	-----	<-->	--D02--	-A2D02-	-A2D02
- ADDR BUS BIT--10---	----	---	---	---	-----	-J05-	-----	<-->	--D04--	-A2D04-	-A2D04
- ADDR BUS BIT--11---	----	---	---	---	-----	-J06-	-----	<-->	--D05--	-A2D05-	-A2D05
- ADDR BUS BIT--12---	----	---	---	---	-----	-J07-	-----	<-->	--D06--	-A2D06-	-A2D06
- ADDR BUS BIT--13---	----	---	---	---	-----	-J09-	-----	<-->	--D07--	-A2D07-	-A2D07
- ADDR BUS BIT--14---	----	---	---	---	-----	-J10-	-----	<-->	--D09--	-A2D09-	-A2D09
- ADDR BUS BIT--15---	----	---	---	---	-----	-J11-	-----	<-->	--D10--	-A2D10-	-A2D10
- ADDR BUS BIT--16---	----	---	---	---	-----	-B12-	-----	<-->	--D11--	-A2D11-	-A2D11
- ADDR GATE----------	----	---	---	---	-----	-D07-	-----	--->	--M08--	-A4B08-	-A4B08
- ADDR GATE RETURN---	----	---	---	---	-----	-G13-	-----	<---	--M09--	-A4B09-	-A4B09
- BURST RETURN-------	----	---	---	---	-----	-D04-	-----	<---	--P04--	-A4D04-	-A4D04
- COND CODE IN BIT-00	----	---	---	---	-----	-B06-	-----	<---	--D12--	-A2D12-	-A2D12
- COND CODE IN BIT-01	----	---	---	---	-----	-B11-	-----	<---	--D13--	-A2D13-	-A2D13
- COND CODE IN BIT-02	----	---	---	---	-----	-B13-	-----	<---	--B13--	-A2B13-	-A2B13
- CYCLE BYTE IND-----	----	---	---	---	-----	-U10-	-----	<-->	--P10--	-A4D10-	-A4D10
- CYCLE INPUT IND----	----	---	---	---	-----	-M13-	-----	<-->	--P09--	-A4D09-	-A4D09
- CYCLE STEAL REQ IN-	----	---	---	---	-----	-U13-	-----	<---	--M02--	-A4B02-	-A4B02
- DATA BUS BIT------00	----	---	---	---	-----	-----	-G02-	<-->	--G02--	-A3B02-	-A3B02
- DATA BUS BIT------01	----	---	---	---	-----	-----	-G03-	<-->	--G03--	-A3B03-	-A3B03
- DATA BUS BIT------02	----	---	---	---	-----	-----	-G04-	<-->	--G04--	-A3B04-	-A3B04
- DATA BUS BIT------03	----	---	---	---	-----	-----	-G05-	<-->	--G05--	-A3B05-	-A3B05
- DATA BUS BIT------04	----	---	---	---	-----	-----	-G07-	<-->	--G07--	-A3B07-	-A3B07
- DATA BUS BIT------05	----	---	---	---	-----	-----	-G08-	<-->	--G08--	-A3B08-	-A3B08
- DATA BUS BIT------06	----	---	---	---	-----	-----	-G09-	<-->	--G09--	-A3B09-	-A3B09
- DATA BUS BIT------07	----	---	---	---	-----	-----	-G10-	<-->	--G10--	-A3B10-	-A3B10
- DATA BUS BIT------P0	----	---	---	---	-----	-----	-G12-	<-->	--G12--	-A3B12-	-A3B12
- DATA BUS BIT------08	----	---	---	---	-----	-----	-J02-	<-->	--J02--	-A3D02-	-A3D02
- DATA BUS BIT------09	----	---	---	---	-----	-----	-J04-	<-->	--J04--	-A3D04-	-A3D04
- DATA BUS BIT------10	----	---	---	---	-----	-----	-J05-	<-->	--J05--	-A3D05-	-A3D05
- DATA BUS BIT------11	----	---	---	---	-----	-----	-J06-	<-->	--J06--	-A3D06-	-A3D06
- DATA BUS BIT------12	----	---	---	---	-----	-----	-J07-	<-->	--J07--	-A3D07-	-A3D07
- DATA BUS BIT------13	----	---	---	---	-----	-----	-J09-	<-->	--J09--	-A3D09-	-A3D09
- DATA BUS BIT------14	----	---	---	---	-----	-----	-J10-	<-->	--J10--	-A3D10-	-A3D10
- DATA BUS BIT------15	----	---	---	---	-----	-----	-J11-	<-->	--J11--	-A3D11-	-A3D11
- DATA BUS BIT------P1	----	---	---	---	-----	-----	-J12-	<-->	--J12--	-A3D12-	-A3D12
- DATA STROBE--------	----	---	---	---	-----	-B10-	-----	--->	--M10--	-A4B10-	-A4B10
- HALT OR MCHK-------	----	---	---	---	-----	-D09-	-----	--->	--M07--	-A4B07-	-A4B07
- INITIATE IPL-------	----	---	---	---	-S04-	-----	-----	--->	--P07--	-A4D07-	-A4D07
- IPL----------------	----	---	---	---	-S02-	-----	-----	<---	--S04--	-A5B04-	-A5B04
- POLL IDENT BIT---00	----	---	---	---	-----	-S11-	-----	--->	--P11--	-A4D11-	-A4D11
- POLL IDENT BIT---01	----	---	---	---	-----	-J12-	-----	--->	--S02--	-A5B02-	-A5B02
- POLL IDENT BIT---02	----	---	---	---	-----	-J12-	-----	--->	--S03--	-A5B03-	-A5B03
- POLL IDENT BIT---03	----	---	---	---	-----	-U05-	-----	--->	--P12--	-A4D12-	-A4D12
- POLL IDENT BIT---04	----	---	---	---	-----	-S12-	-----	--->	--P13--	-A4D13-	-A4D13
- POLL RETURN--------	----	---	---	---	-----	-G12-	-----	<---	--M04--	-A4B04-	-A4B04
- POWER ON RESET-***-	-M04	M04	M04	M04	-U02-	-----	-----	--->	--S05--	-- * --	-A5B05
- REQ IN BUS BIT---00	----	---	---	---	-----	-S02-	-----	<---	--S07--	-A5B07-	-A5B07
- REQ IN BUS BIT---01	----	---	---	---	-----	-S03-	-----	<---	--S08--	-A5B08-	-A5B08
- REQ IN BUS BIT---02	----	---	---	---	-----	-S04-	-----	<---	--S09--	-A5B09-	-A5B09
- REQ IN BUS BIT---03	----	---	---	---	-----	-S05-	-----	<---	--S10--	-A5B10-	-A5B10
# REQ IN BUS BIT---04	----	---	---	---	-----	-----	-----	<---	#-S12--	#A5B12-	-A5B12
# REQ IN BUS BIT---05	----	---	---	---	-----	-----	-----	<---	#-S13--	#A5B13-	-A5B13
# REQ IN BUS BIT---06	----	---	---	---	-----	-----	-----	<---	#-U02--	#A5D02-	-A5D02
# REQ IN BUS BIT---07	----	---	---	---	-----	-----	-----	<---	#-U04--	#A5D04-	-A5D04
# REQ IN BUS BIT---08	----	---	---	---	-----	-----	-----	<---	#-U05--	#A5D05-	-A5D05
# REQ IN BUS BIT---09	----	---	---	---	-----	-----	-----	<---	#-U06--	#A5D06-	-A5D06
# REQ IN BUS BIT---10	----	---	---	---	-----	-----	-----	<---	#-U07--	#A5D07-	-A5D07
# REQ IN BUS BIT---11	----	---	---	---	-----	-----	-----	<---	#-U09--	#A5D09-	-A5D09
# REQ IN BUS BIT---12	----	---	---	---	-----	-----	-----	<---	#-U10--	#A5D10-	-A5D10
# REQ IN BUS BIT---13	----	---	---	---	-----	-----	-----	<---	#-U11--	#A5D11-	-A5D11
# REQ IN BUS BIT---14	----	---	---	---	-----	-----	-----	<---	#-U12--	#A5D12-	-A5D12
# REQ IN BUS BIT---15	----	---	---	---	-----	-----	-----	<---	#-U13--	#A5D13-	-A5D13
- SERVICE GATE-------	----	---	---	---	-----	-B09-	-----	--->	--P05--	-A4D05-	-A4D05
- SERVICE GATE RETURN	----	---	---	---	-P06-	-M06-	-----	<---	--P06--	-A4D06-	-A4D06
- STATUS BUS BIT---00	----	---	---	---	-B03-	-----	-----	--->	--J13--	-A3D13-	-A3D13
- STATUS BUS BIT---01	----	---	---	---	-B12-	-----	-----	--->	--G13--	-A3B13-	-A3B13
- STATUS BUS BIT---02	----	---	---	---	-----	-S10-	-----	--->	--M03--	-A4B03-	-A4B03
- STATUS BUS BIT---03	----	---	---	---	-U05-	-B08-	-----	--->	--P02--	-A4D02-	-A4D02
- SYSTEM RESET-------	----	---	---	---	-----	-----	-----	--->	--M05--	-A4B05-	-A4B05

VOLTAGE PIN ASSIGNMENTS (YA445)
+5V---D03--J03--P03--U03 ALL
+12V--S11 STORAGE ONLY
GND---D08--J08--P08--U08 ALL
-5V---G06--I/O AND STORAGE (NOT ROW A)

+8.5V-G11--I/O ONLY (NOT ROW A)

-12V--B06-I/O ONLY (NOT ROW A)
+12V--B11-I/O AND STORAGE (NOT ROW A)

\# LINES NOT USED BY PROCESSOR

* SEE INSTALLATION INSTRUCTIONS FOR RESTRICTIONS ON I/O ATTACHMENTS IN ROW A. IF A CARD IS INSTALLED IN ROW A, JUMPER A2S05 TO B2S05.

** SEE 4955 THEORY DIAGRAMS MANUAL FOR DATA FLOW AND POLL INFORMATION.

*** POWER ON RESET REFER TO YA445 FROM Q2M04 TO T2M04.

POLL NET ON BOARD

	A 2	B 2	C 2	D 2	E 2	F 2	G 2
POLL M11 PROPAGATE	*	*	*	*	*	*	*
POLL M12	*	*	*	*	*	*	*
POLL PRIME M13	*	*	*	*	*	*	*

* J2D11 POLL FROM PROCESSOR

4955 MOD F00 PROCESSOR BOARD

E.C. HISTORY MACH.

15JAN81 869422
23FEB81 987889 4955

IBM CORP. GSD

DATE LAST E.C. P.N. 6031138
20NOV81 466795

A52203 0 0 0

4955 MOD F00 PROCESSOR BOARD

LINE NAME	ADDR EXP CARD Q	OUTER STG N M P 128K	INNER STG L 128K	ROS CARD K	ADDR CARD J	DATA CARD H	I/O CARDS D E F G FLOAT POINT CARD G	I/O CARDS B C
AC FAILURE	**	REFER TO YA445 IF BBU INSTALLED						
AC FAILURE RETURN	**	REFER TO YA445 IF BBU INSTALLED						
- ADDR CARD GND T P					-B02-			
- ANY WRITE CYCLE EXT				-G02-	-G11-			
- BLK DEST PULSE & STG CY				-U04-		-U07-		
- BYTE 0 PTY GEN/+STG PO				-S11-		-S11-		
- BYTE 1 PTY GEN/+STG P1				-U10-		-U10-		
- CLK CS SDR					-B03-	-B06-		
- CLK Z REG T P						-B11-		
- COLUMN 1					-D12-	-B13-		
- COLUMN 7					-D13-	-D13-		
- CPU DATA STROBE				-M06-		-M13-		
- CTR 8-15 EQ 0					-U11-	-U11-		
- DATA CD CON MET BIT 5				-G04-		-S12-		
- DATA CD CON MET BIT 6A				-J04-		-S13-		
- DATA CD CON MET BIT 6B				-G03-		-G13-		
- DATA CARD GND T.P.						-U04-		
+ END OF CYCLE	-U02-			-J11-				
- FLOATING PT. INSTALLED				-U06-			G2S11-	
+ GATE SDR 8-15 TO STG0-7				-S07-		-S07-		
+ GATE STG DATA TO SDR 1				-S09-		-S09-		
+ GATE STG DATA TO SDR 2				-S10-		-S10-		
- GATE TRANSLATOR SAR	-S02-				-U04-			
- GATED TIME A				-B04-		-S04-	-M06*-	
- GATED TIME C				-J02-		-G06-	-S06*-	
+ INNER STG CYCLE	-B13-			-J09-				
- MACHINE CHK SET CON DOT				-P11-	-P12-			
9.09 MHZ OSC				-D13-				
+ OP REG BIT 07				-P10-		-S02-		
+ OP REG BIT 14				-M05-		-M06-		
+ OP REG BIT 15				-P13-		-U06-		
+ OSC TO CLOCK				-B13-				
+ OSC TO CLOCK				-D12-				
- PCK MCK COND				-S06-	-S13-	-S03-		
- PWR THERMAL WARN IND -*				-S03-	-U02-			
+ PRI INT REQ				-J13-	-J13-			
+ PROC CYCLE EXT NOT INHI				-J12-	-D02-			
+ PROC INSTR FETCH REQ				-B06-	-D06-			
- PROGRAM CHK SET CON DOT				-M11-	-M12-			
- PROTECT CHK COND DOT	-U10-			-B11-	-D05-			
- PROTECT KEY BIT 01	-J11-				-U07-			
- PROTECT KEY BIT 02	-J10-				-U09-			
- PROTECT KEY BIT 04	-D05-				-B05-			
+ ROS DATA BIT 26				-P04-		-U02-		
+ REFRESH ADDRESS BIT 05	-S05-	-M13-	-M13-					
+ REFRESH ADDRESS BIT 06	-M09-	-U02-	-U02-					
+ REFRESH CYCLE	-G06-			-M02-				
+ REFRESH REQUEST	-D10-			-M03-				
- REFRESH RESET	-U11-			-M04-				
- SAR BIT 00	-D04-	-S12-	-S12-	-P12-	-M02-			
- SAR BIT 01	-G02-	-U11-	-U11-	-M12-	-M03-			
- SAR BIT 02	-J06-	-S09-	-S09-		-M04-			
- SAR BIT 03	-J05-	-S05-	-S05-		-M05-			
- SAR BIT 04	-G07-	-M09-	-M09-		-M07-			
+ SAR BIT 05	-B05-	-B05-	-B05-		-M08-			
+ SAR BIT 06	-B08-	-B08-	-B08-		-M09-			
+ SAR BIT 07	-B10-	-B10-	-B10-		-M10-			
+ SAR BIT 08		-B12-	-B12-		-P02-			
+ SAR BIT 09		-D02-	-D02-		-P04-			
+ SAR BIT 10		-D13-	-D13-		-P05-			
+ SAR BIT 11		-G05-	-G05-		-P06-			
+ SAR BIT 12		-J07-	-J07-		-P07-			
+ SAR BIT 13		-M10-	-M10-		-P09-			
+ SAR BIT 14		-P07-	-P07-		-P10-			
+ SAR BIT 15				-M10-	-P11-			
- S/D DCB 24-27 BIT 01					-S06-	-S05-		
+ S/D DCB 24-27 BIT 02					-S07-	-S06-		
- S/D DCB 24-27 BIT 04					-S08-	-S08-		
+ SDR BIT 00				-P09-		-P13-		
+ SDR BIT 01				-J05-		-J13-		
+ SDR BIT 02				-J07-		-U05-		
+ SDR BIT 03				-J06-		-G11-		
+ SDR BIT 04				-M09-		-M11-		

* INSTALL FLOATING POINT IN ROW G ONLY

VOLTAGE PIN ASSIGNMENTS (YA445)

+5V---D03--J03--P03--U03 ALL
+12V--S11 STORAGE ONLY
GND---D08--J08--P08--U08 ALL
-5V---G06 I/O AND STORAGE

+8.5V-G11 I/O ONLY

-12V--B06 I/O ONLY
+12V--B11 I/O AND STORAGE

* PWR THERMAL WARN IND (YA445)
FROM K2S03 TO T2M05

** AC FAILURE---------R2M10 TO T2M10
AC FAILURE RETURN--R2M11 TO T2M11
REFER TO YA445
REFER TO YX100 IF BBU INSTALLED.

SEE 4955 THEORY DIAGRAMS MANUAL FOR DATA FLOW

4955 MOD F00 PROCESSOR BOARD

E.C. HISTORY		MACH.	
15JAN81	869422		A
23FEB81	987889	4955	5 2 1 3
DATE	LAST E.C.	IBM CORP. GSD P.N. 6031139	0 0 0
20NOV81	466795		

4955 MOD F00 PROCESSOR BOARD

LINE NAME	ADDR EXP CARD Q	OUTER STG N P M	INNER STG L	ROS CARD K	ADDR CARD J	DATA CARD H	I/O CARDS D E F G FLT PT CARD G	I/O CARDS B C
+ SDR BIT 00 TO STG	-U12-	-U12-	-U12-	-----	-----	-B02-	------	------
+ SDR BIT 01 TO STG	-U13-	-U13-	-U13-	-----	-----	-B03-	------	------
+ SDR BIT 02 TO STG	-S07-	-S07-	-S07-	-----	-----	-B04-	------	------
+ SDR BIT 03 TO STG	-U06-	-U06-	-U06-	-----	-----	-B05-	------	------
+ SDR BIT 04 TO STG	-P12-	-P12-	-P12-	-----	-----	-B07-	------	------
+ SDR BIT 05 TO STG	-P13-	-P13-	-P13-	-----	-----	-B08-	------	------
+ SDR BIT 06 TO STG	-P09-	-P09-	-P09-	-----	-----	-B09-	------	------
+ SDR BIT 07 TO STG	-M08-	-M08-	-M08-	-----	-----	-B10-	------	------
+ SDR BIT 08 TO STG	-D06-	-D06-	-D06-	-----	-----	-D02-	------	------
+ SDR BIT 09 TO STG	-M03-	-M03-	-M03-	-----	-----	-D04-	------	------
+ SDR BIT 10 TO STG	-G10-	-G10-	-G10-	-----	-----	-D05-	------	------
+ SDR BIT 11 TO STG	-J09-	-J09-	-J09-	-----	-----	-D06-	------	------
+ SDR BIT 12 TO STG	-G04-	-G04-	-G04-	-----	-----	-D07-	------	------
+ SDR BIT 13 TO STG	-J04-	-J04-	-J04-	-----	-----	-D09-	------	------
+ SDR BIT 14 TO STG	-D11-	-D11-	-D11-	-----	-----	-D10-	------	------
+ SDR BIT 15 TO STG	-D12-	-D12-	-D12-	-----	-----	-D11-	------	------
- SEG REG CYCLE	-B06-	-----	-----	-J10-	-----	-----	------	------
+ SET BYTE LTH HO	-----	-----	-----	-U13-	-----	-U13-	------	------
- STG DATA IN P0/-BYT OPE	-----	-P02-	-P02-	-D02-	-----	-B12-	------	------
- STG DATA IN P1/-BYT 1PE	-----	-D07-	-D07-	-B02-	-----	-D12-	------	------
+ STG DATA OUT BIT 00	-S10-	-S10-	-S10-	-----	-----	-M02-	------	------
+ STG DATA OUT BIT 01	-U09-	-U09-	-U09-	-----	-----	-M03-	------	------
+ STG DATA OUT BIT 02	-S04-	-S04-	-S04-	-----	-----	-M04-	------	------
+ STG DATA OUT BIT 03	-S03-	-S03-	-S03-	-----	-----	-M05-	------	------
+ STG DATA OUT BIT 04	-M12-	-M12-	-M12-	-----	-----	-M07-	------	------
+ STG DATA OUT BIT 05	-P11-	-P11-	-P11-	-----	-----	-M08-	------	------
+ STG DATA OUT BIT 06	-M07-	-M07-	-M07-	-----	-----	-M09-	------	------
+ STG DATA OUT BIT 07	-P06-	-P06-	-P06-	-----	-----	-M10-	------	------
- STG DATA OUT BIT P0	-----	-G12-	-G12-	-U11-	-----	-M12-	------	------
+ STG DATA OUT BIT 08	-B04-	-B04-	-B04-	-----	-----	-P02-	------	------
+ STG DATA OUT BIT 09	-J12-	-J12-	-J12-	-----	-----	-P04-	------	------
+ STG DATA OUT BIT 10	-G09-	-G09-	-G09-	-----	-----	-P05-	------	------
+ STG DATA OUT BIT 11	-G08-	-G08-	-G08-	-----	-----	-P06-	------	------
+ STG DATA OUT BIT 12	-J02-	-J02-	-J02-	-----	-----	-P07-	------	------
+ STG DATA OUT BIT 13	-G03-	-G03-	-G03-	-----	-----	-P09-	------	------
+ STG DATA OUT BIT 14	-D09-	-D09-	-D09-	-----	-----	-P10-	------	------
+ STG DATA OUT BIT 15	-B09-	-B09-	-B09-	-----	-----	-P11-	------	------
- STG DATA OUT BIT P1	-----	-B03-	-B03-	-S12-	-----	-P12-	------	------
+ STG REQ TO TRANSLATOR	-B11-	-----	-----	-G08-	-----	-----	------	------
+ STG WRITE BYTE 00	-----	-M06-	-M06-	-S13-	-----	-----	------	------
+ STG WRITE BYTE 01	-----	-G13-	-G13-	-U09-	-----	-----	------	------
+ STG WRITE OP 00	-P05-	-----	-----	-S08-	-----	-----	------	------
+ STG WRITE OP 01	-P10-	-----	-----	-U07-	-----	-----	------	------
- STP CLK DOT T P	-----	-----	-----	-B09-	-----	-----	------	------
- SUPVSR STOR CYC STL CYC	-U07-	-----	-----	-----	-B04-	-----	------	------
+ TIME A	-S06-	-B02-	-B02-	-D11-	-B07-	-----	------	------
+ TIME B	-S08-	-G02-	-G02-	-B08-	-----	-----	------	------
+ TIME C	-S11-	-M02-	-M02-	-B10-	-D10-	-----	------	------
+ TIME D	-G11-	-S02-	-S02-	-D10-	-----	-----	------	------
- TRANSLATOR ENABLED	-----	-----	-----	-M08-	-M11-	-----	------	------
- TRANSLATOR INSTALLED	-----	-----	-----	-U12-	-P13-	-----	------	------
- TRANSLATOR INSTALLED	-----	-----	-----	-U08-	-P08-	-----	------	------
- TRANSLATOR ISA	-B07-	-----	-----	-D09-	-----	-----	------	------
- TRANSLATOR REFRESH CYC	-J07-	-G07-	-G07-	-----	-----	-----	------	------
+ TRIG DEC CTR	-----	-----	-----	-----	-U12-	-U12-	------	------
+ WRITE EN OR DATA STROBE	-----	-----	-----	-G05-	-G06-	-----	------	------
+ 64K CARD SELECT	-----	-----	-M05-	-M13-	-----	-----	------	------
+ 128K CARD SELECT	-M10-	-----	-S06-	-----	-----	-----	------	------
+ 192K CARD SELECT	-M05-	M2M05	-----	-----	-----	-----	------	------
+ 256K CARD SELECT	-M06-	M2S06	-----	-----	-----	-----	------	------
- 256K INSTALLED	-S09-	M2M11	-----	-----	-----	-----	------	------
+ 320K CARD SELECT	-M11-	N2M05	-----	-----	-----	-----	------	------
+ 384K CARD SELECT	-M13-	N2S06	-----	-----	-----	-----	------	------
- 384K INSTALLED	-S12-	N2M11	-----	-----	-----	-----	------	------
+ 448K CARD SELECT	-U04-	P2M05	-----	-----	-----	-----	------	------
+ 512K CARD SELECT	-U05-	P2S06	-----	-----	-----	-----	------	------
- 512K INSTALLED	-S13-	P2M11	-----	-----	-----	-----	------	------

VOLTAGE PIN ASSIGNMENTS

+5V---D03--J03--P03--U03 ALL
+12V--S11---------- STORAGE ONLY
-5V---G06---------- I/O AND STORAGE
+8.5V-G11---------- I/O ONLY
GND---D08--J08--P08--U08 ALL

-12V---B06 I/O ONLY
+12V---B11 I/O AND STORAGE

SEE 4955 THEORY DIAGRAMS MANUAL FOR DATA FLOW

4955 MOD F00 PROCESSOR BOARD

E.C. HISTORY MACH.
15JAN81 869422 4955

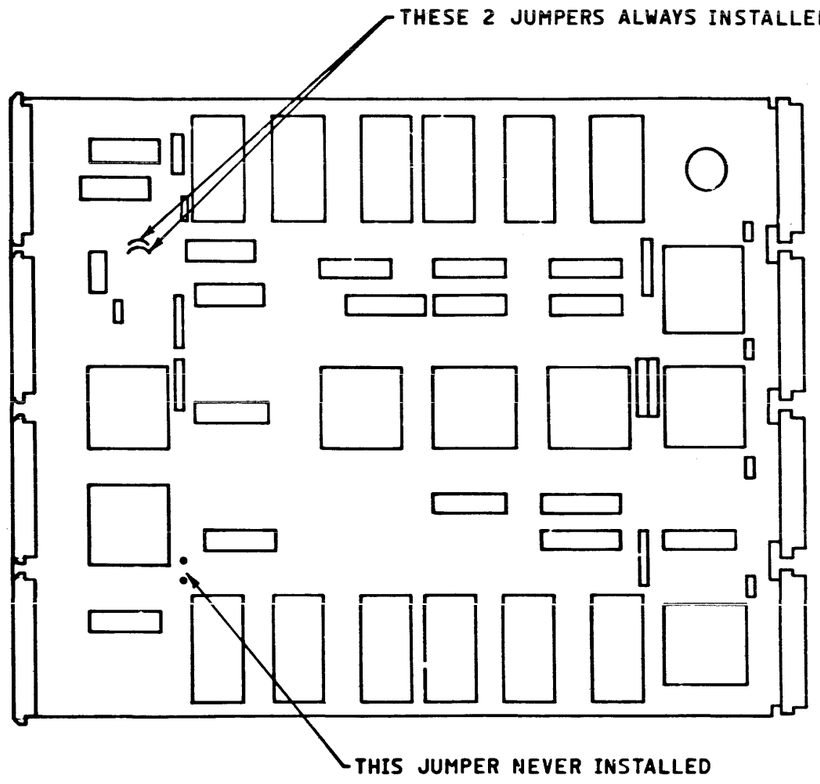
IBM CORP. GSD

DATE 23FEB81 LAST E.C. 987889 P.N. 6031140

4955MM3 0 0 0

A5300

PROCESSOR CPU ROS CARD

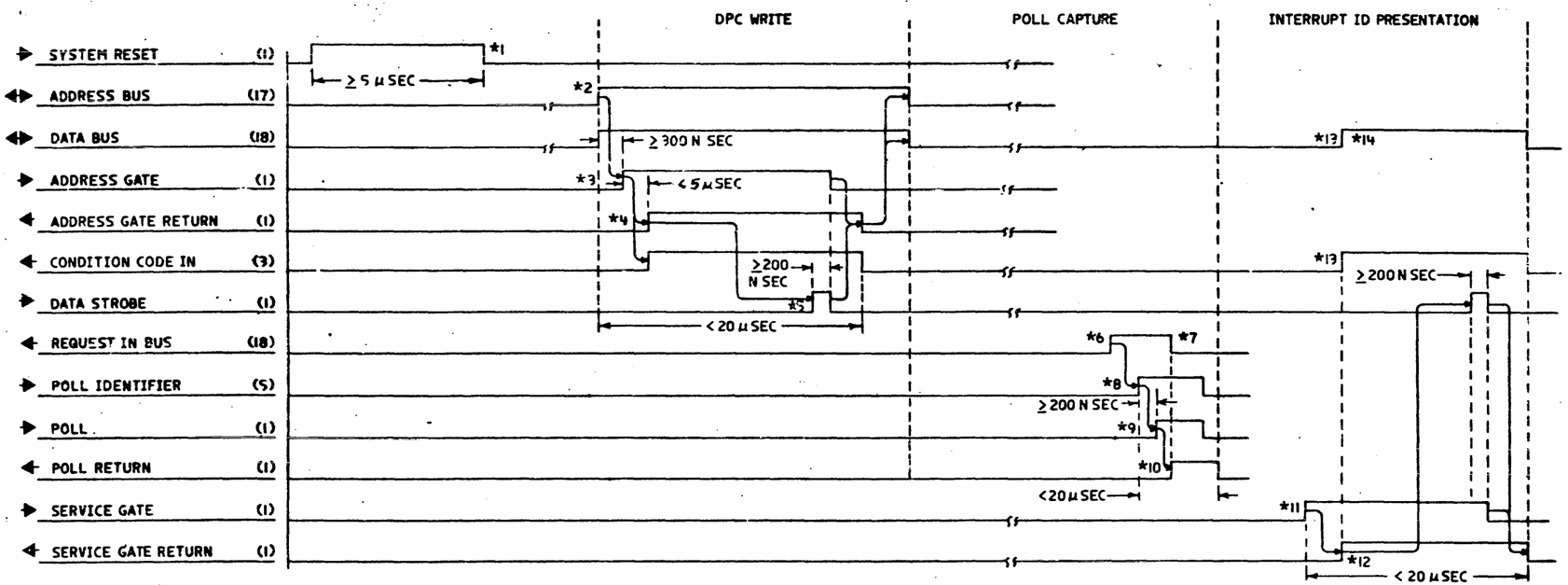


A5300

EC HISTORY		DRAWING TITLE
27SEP76	578468	4955 ROS CARD
30SEP77	754882	MACH 4955
		PART NO 1635201
C		CLASSIFICATION

IBM CORP

A5300



ALL OUTBOUND TAG AND BUS RELATIONSHIPS ARE AS SEEN AT THE OUTPUT OF THE CHANNEL. ALL INBOUND TAG AND BUS RELATIONSHIPS ARE AS SEEN AT THE OUTPUT OF THE DEVICE. ALL TIMES INDICATED ARE AS SEEN AT THE CHANNEL OUTPUT.

THESE SEQUENCES ARE SHOWN IN THIS ORDER FOR TIMING CHART SIMPLICITY. THEY DO NOT IMPLY A FIXED ORDER OF EVENTS REQUIRED BY THE CHANNEL

NOTES:

* 1 SYSTEM RESET MUST DISABLE SELECTION, BLOCK POLL PROPAGATION AND CLEAR ANY STATUS, STATES, REQUESTS, REGISTERS AND INTERFACE CONTROL LOGIC
* 2 BIT 16 ON, ADDRESS BUS CONTAINS THE COMMAND CODE (0-7) AND THE DEVICE ADDRESS (8-15)
* 3 ADDRESS BUS BIT 16 ON, EXAMINE 8-15 FOR DEVISE ADDRESS, LOGICAL COMPARE CONSTITUTES INITIAL SELECTION
* 4 INITIAL SELECTION-ADDRESS GATE SIGNALS A DEVICE THAT IT CAN RESPOND TO INITIAL SELECTION AND BEGIN EXECUTION OF THE COMMAND SPECIFIED BY BITS 0-7 OF THE ADDRESS BUS
  ADDRESS GATE RETURN-SIGNALS THE RECEPTION OF ADDRESS GATE-EXAMINE ADDRESS BUS BITS 0-7 FOR COMMAND ACCEPTANCE AND ACTIVATION OF CONDITION CODE IN BUS
* 5 DATA STROBE IS RAISED FOR A DURATION OF 200 NSEC AND FALLS BEFORE THE FALL OF ADDRESS GATE SET DATA BUS INTO HOLDING REG, IF INITIAL SELECTION AND OUTBOUND TRANSFER IS OCCURING (BIT 1 OF ADDRESS BUS ON)
* 6 REQUEST IN BUS BIT 16 OFF EQUALS INTERRUPT REQUEST ONE OF BITS 0-15 ON IS DETERMINED BY AN INTERRUPTING CONDITION IN THE DEVICE AND EQUALS THE LEVEL OF A PREVIOUS PREPARE COMMAND WITH "1" BIT ON
* 7 REQUEST IN BUS MUST STAY ACTIVE UNTIL IT IS SERVICED (POLL CAPTURE OCCURS RECEIVES A HALT I/O, DEVICE RESET, SYSTEM RESET, OR POWER ON RESET
* 8 POLL IDENTIFIER BUS (5 BITS) IS RAISED AT LEAST 200 NSEC BEFORE POLL BIT 0 OFF IS FOR INTERRUPT IDENTIFICATION
* 9 IF THE DEVICE DOES NOT CAPTURE THE POLL IT MUST PROPAGATE POLL TO THE NEXT DEVICE
* 10 POLL RETURN IS RAISED IF THE POLL IDENTIFIER MATCHES THE LOGICAL REQUEST BEING MADE ON THE REQUEST IN BUS, POLL RETURN RESETS THE REQUEST IN BUS
* 11 SERVICE GATE AFTER POLL CAPTURE INDICATES BEGIN TRANSFER TO THE DEVICE
* 12 SERVICE GATE RETURN SIGNALS THE DEVICES RECOGNITION OF SERVICE GATE
* 13 MUST BE ACTIVE BY THE RISE OF SERVICE GATE RETURN
* 14 DATA BUS BITS 0-7 ARE THE INTERRUPT STATUS BYTE (ISB), BITS 0-15 ARE THE DEVICE ADDRESS

NOTE: ALL BUS BITS MUST BE SUITABLE PRIOR TO ACTIVATING OF ANY TAG LINE
TAG LINE MUST BE DEACTIVATED PRIOR TO ANY BUS LINES GOING INACTIVE

SCOPE LOOP- DPC WRITE
(PREPARE DEVICE TO LEVEL 0, I-BIT ON)

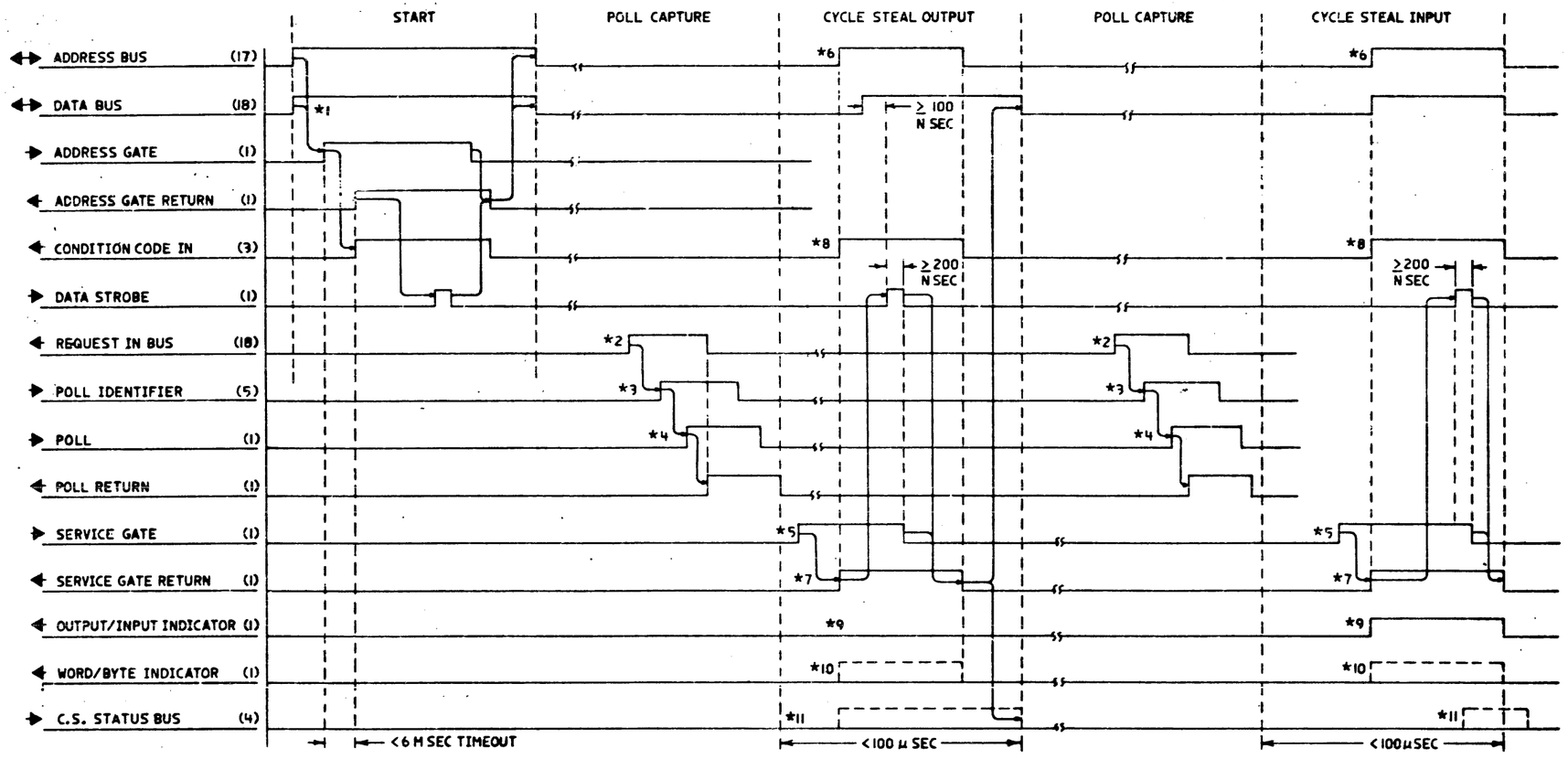
ADDRESS (HEX)	DATA (HEX)	
0000	680C	I/O COMMAND
0002	0024	ADDRESS OF IDCB
0004	6802	*UNCONDITIONAL BRANCH
0006	0000	* TO ADDRESS 0000
0024	60XX	IDCB PREPARE 'XX'- PUT DESIRED DEVICE
		ADDRESS HERE
0026	0001	PREPARE DATA, LEVEL 0, I BIT ENABLED

A5310

EC HISTORY		DRAWING TITLE
1 OCT 76	578468	DPC WRITE
1 AUG 77	578757	MACh
		PART NO 1635490
		CLASSIFICATION

D

IBM CORP



ALL OUTBOUND TAG AND BUS RELATIONSHIPS ARE AS SEEN AT THE OUTPUT OF THE CHANNEL. ALL INBOUND TAG AND BUS RELATIONSHIPS ARE AS SEEN AT THE OUTPUT OF THE I/O DEVICE. ALL TIMES INDICATED ARE AS SEEN AT THE CHANNEL OUTPUT

THESE SEQUENCES ARE SHOWN IN THIS ORDER FOR TIMING CHART SIMPLICITY. THEY DO NOT IMPLY A FIXED ORDER OF EVENTS REQUIRED BY THE CHANNEL

NOTE:

1 FOR NOTES SEE PAGE A5321

EC HISTORY		DRAWING TITLE
1 OCT 76	578468	CYCLE STEAL
.1 AUG 77	578757	MACH
		PART NO 1635491
		CLASSIFICATION

D

IBM CORP

NOTES:

* 1 DATA BUS CONTAINS THE DEVICE CONTROL BLOCK (DCB) ADDRESS DURING A START COMMAND

* 2 REQUEST IN BUS BIT 16 ON EQUALS CYCLE STEAL REQUEST

* 3 POLL IDENTIFIER BITS 0 ON, 3 ON AND 4 ON EQUAL POLL FOR CYCLE STEAL

* 4 POLL IS CAPTURED BY THE FIRST DEVICE TO SEE IT WITH A REQUEST IN RAISED, OTHERWISE POLL IS PROPAGATED TO THE NEXT DEVICE IN LINE

* 5 SERVICE GATE AFTER POLL CAPTURE INDICATES BEGIN DATA TRANSFER TO THE DEVICE

* 6 ADDRESS BUS BIT 16 OFF AT PROCESSOR PRIOR TO SERVICE GATE ACTIVE INDICATES CYCLE STEAL TO OR FROM STORAGE TO THE I/O DEVICE ADDRESS BUS BITS 0-15 CONTAIN THE STORAGE ADDRESS FOR CYCLE STEAL

* 7 SERVICE GATE RETURN SIGNALS A SERVICE GATE CAPTURE BY THE DEVICE AND ACTIVATION OF ADDRESS BUG (ON A CYCLE STEAL SEQUENCE), DATA BUS, CONDITION CODE IN BUS AND OTHERS TAGS AS REQUIRED BY THE PARTICULAR CYCLE STEAL OR INTERRUPT SERVICE SEQUENCE

* 8 CONDITION CODE IN BITS 0-3 RAISED DURING CYCLE STEAL DATA TRANSFERS ARE LOGICALLY EQUAL TO THE CYCLE STEAL ADDRESS KEY DURING CYCLE STEAL TRANSFERS FOR FETCHING THE DCB AND REPORTING RESIDUAL STATUS, A VALUE OF LOGICAL ZERO IS USED FOR THE ADDRESS KEY. DURING DATA TRANSFER, ADDRESS TRANSFER KEY EQUALS CONTROL WORD BITS 5-7 WHICH WERE SET IN THE DCB

* 9 CYCLE INPUT INDICATOR OFF INDICATES AN OUTPUT FROM STORAGE, CYCLE INPUT INDICATOR ON INDICATES AN INPUT TO STORAGE

* 10 CYCLE BYTE INDICATOR ON INDICATES A BYTE TRANSFER, CYCLE BYTE INDICATOR OFF INDICATES A WORD TRANSFER

* 11 STATUS BUS - ANY BIT 0-3 SIGNALS THE DEVICE THAT A CHANNEL ERROR HAS BEEN DETECTED IF ACTIVATED DURING CYCLE STEAL SERVICING THE DEVICE WILL RETAIN THIS INFORMATION FOR PRESENTATION IN THE ISB AT INTERRUPTION TIME THE DEVICE WILL TERMINATE ANY OTHER CYCLE STEAL OPERATIONS AND PRESENT AN END INTERRUPT

NOTE: ALL BUS BITS MUST BE STABLE PRIOR TO ACTIVATING OF ANY TAG LINE. TAG LINE MUST BE DEACTIVATED PRIOR TO ANY BUS LINES GOING INACTIVE

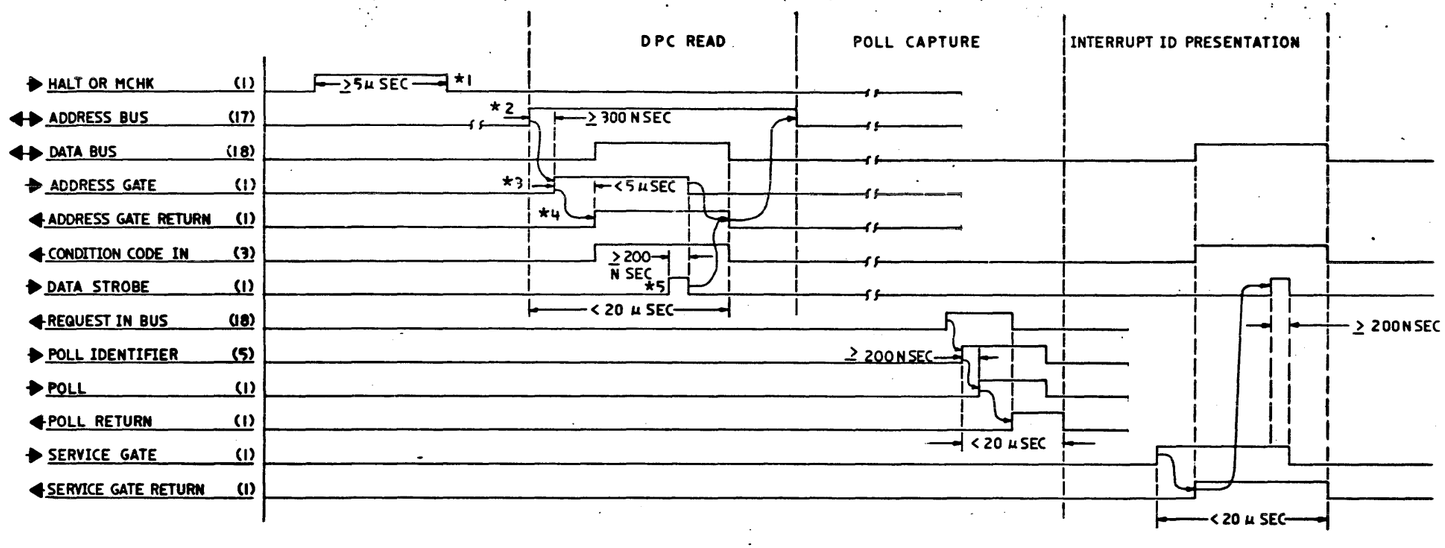
SCOPE LOOP - READ CYCLE STEAL STATUS (CYCLE STEAL DEVICES ONLY)		
ADDRESS (HEX)	DATA (HEX)	
0000	680C	I/O COMMAND
0002	0024	ADDRESS OF IDCB
0004	6802	*UNCONDITIONAL BRANCH
0006	0304	*TO ADDRESS 0304
0024	60XX	*IDCB - PREPARE 'XX' = DESIRED DEVICE ADDRESS
0026	0001	PREPARE DATA, LEVEL 0, I BIT ENABLED
0030		
↕	0300	PUT DDB POINTER (0300) IN PROPER ADDRESS.
022F		ADDRESS (HEX) CALCULATION = 0030 + 2
		(DEVICE ADDRESS). IT IS ONLY NECESSARY
		TO STORE INTO THE ONE CALCULATED
		ADDRESS
0300	0304	START INSTRUCTION POINTER
0302	0000	
0304	680C	I/O COMMAND
0306	030A	ADDRESS OF IDCB
0308	6100	LEVEL EXIT
030A	7FXX	IDCB 'XX' = DEVICE ADDRESS
030C	030E	DCB ADDRESS
030E	2000	DCB - START CYCLE STEAL
0310		
↓	0000	
0318		
031A	000X	BYTE COUNT - 'X' SEE DEVICE TDM FOR BYTE COUNT
031C	031E	DATA ADDRESS
031E	—	*CYCLE STEAL STATUS IS PUT HERE AT END
—	—	*OF CYCLE STEAL STATUS COMMAND

EC HISTORY		DRAWING TITLE
1 AUG 77	578757	A5320 NOTES
		MACH
		PART NO 4414342
		CLASSIFICATION

D

IBM CORP

A5321



ALL OUTBOUND TAG AND BUS RELATIONSHIPS ARE AS SEEN AT THE OUTPUT OF THE CHANNEL. ALL INBOUND TAG AND BUS RELATIONSHIPS ARE AS SEEN AT THE OUTPUT OF THE DEVICE. ALL TIMES INDICATED ARE AS SEEN AT THE CHANNEL OUTPUT.

THESE SEQUENCES ARE SHOWN IN THIS ORDER FOR TIMING CHART SIMIPLICITY. THEY DO NOT IMPLY A FIXED ORDER OF EVENTS REQUIRED BY THE CHANNEL.

NOTES

*1 HALT OR MCHK SIGNALS THE DEVICE TO DESELECT, BLOCK POLL PROPOGATION AND TO CLEAR ANY STATUS REQUESTS OR REGISTERS EXCEPT FOR PREPARE FIELD, OUTPUT SENSOR POINTS AND TIMER VALUES.

*2 BIT 16 ON, ADDRESS BUS CONTAINS THE COMMAND CODE (0—7) AND THE DEVICE ADDRESS (8—15)

*3 ADDRESS BUS BIT 16 ON, EXAMINE 8—15 FOR DEVICE ADDRESS, EQUAL COMPARE CONSTITUTES INITIAL SELECTION — EXAMINE ADDRESS BUS BITS 0—7 FOR COMMAND ACCEPTANCE. ACTIVATE IMMEDIATE STATUS ON CONDITION CODE IN AND DATA ON DATA BUS.

*4 INITTAL SELECTION AND ADDRESS GATE — DEVICE SETS ADDRESS GATE RETURN

*5 ON INBOUND DPC TRANSFERS, SHOULD THE CHANNEL DETECT A PARITY ERROR, DATA STROBE WILL NOT BE ACTIVATED AND ADDRESS GATE WILL BE DROPPED

NOTE: ALL BUS BITS MUST BE STABLE PRIOR TO ACTIVATING ANY TAG LINES
TAG LINE MUST BE DEACTIVATED PRIOR TO ANY BUS LINE GOING INACTIVE

SCOPE LOOP—DPC READ (READ DEVICE ID)		
ADDRESS (HEX)	DATA (HEX)	
0000	680C	I/O COMMAND
0002	0024	ADDRESS OF IDCB
0004	6802	*UNCONDITIONAL BRANCH
0006	0000	*TO ADDRESS 0000
0024	20XX	IDCB—READ DEVICE ID 'XX' = DESIRED DEVICE
		ADDRESS DEVICE ID IS STORED IN ADDRESS
0026	0000	0026 WHEN READ DEVICE ID ENDS.

A5330

EC HISTORY		DRAWING TITLE
1 OCT 76	578468	DPC READ
1 AUG 77	578757	MACH
		PART NO 1635489
		CLASSIFICATION

D

IBM CORP

A5330

SERIES 1 PROGRAMMER CONSOLE OR C E CONSOLE

LINE NAME	PROC CARD	CABLE & PIN	PROC. PIN	CONS. PIN	THRU TO BAS CON
AUTO IPL MODE	-ROS-	-C3D07-	-W07-	-D07-	-C5D07-
BUZZER	-ROS-	-C3B11-	-W31-	-B11-	
CHECK INDICATOR	-ROS-	-C3D13-	-W13-	-D13-	
CHECK RESTART INDICATOR	-ROS-	-C3B07-	-W27-	-B07-	
COLUMN 00	-ROS-	-C3D03-	-W03-	-D03-	-C5D03-
COLUMN 01	-DATA-	-C1D10-	-X10-	-D10-	
COLUMN 02	-ADDR-	-C2B13-	-W33-	-B13-	
COLUMN 03	-ADDR-	-C2D10-	-W10-	-D10-	
COLUMN 04	-ADDR-	-C2D11-	-W11-	-D11-	
COLUMN 05	-ADDR-	-C2D12-	-W12-	-D12-	
COLUMN 06	-ADDR-	-C2D13-	-W13-	-D13-	
COLUMN 07	-DATA-	-C1D11-	-X11-	-D11-	
COLUMN 08	-ROS-	-C3B08-	-W28-	-B08-	
COLUMN 09	-ROS-	-C3B12-	-W32-	-B12-	
COLUMN 10	-ROS-	-C3B13-	-W33-	-B13-	
COLUMN 11	-ROS-	-C3D02-	-W02-	-D02-	
DATA DISPLAY BIT 00 IND	-DATA-	-C1B02-	-X22-	-B02-	
DATA DISPLAY BIT 01 IND	-DATA-	-C1B03-	-X23-	-B03-	
DATA DISPLAY BIT 02 IND	-DATA-	-C1B04-	-X24-	-B04-	
DATA DISPLAY BIT 03 IND	-DATA-	-C1B05-	-X25-	-B05-	
DATA DISPLAY BIT 04 IND	-DATA-	-C1D06-	-X06-	-D06-	
DATA DISPLAY BIT 05 IND	-DATA-	-C1B07-	-X27-	-B07-	
DATA DISPLAY BIT 06 IND	-DATA-	-C1B08-	-X28-	-B08-	
DATA DISPLAY BIT 07 IND	-DATA-	-C1B09-	-X29-	-B09-	
DATA DISPLAY BIT 08 IND	-DATA-	-C1B10-	-X30-	-B10-	
DATA DISPLAY BIT 09 IND	-DATA-	-C1D07-	-X07-	-D07-	
DATA DISPLAY BIT 10 IND	-DATA-	-C1B12-	-X32-	-B12-	
DATA DISPLAY BIT 11 IND	-DATA-	-C1B13-	-X33-	-B13-	
DATA DISPLAY BIT 12 IND	-DATA-	-C1D02-	-X02-	-D02-	
DATA DISPLAY BIT 13 IND	-DATA-	-C1D09-	-X09-	-D09-	
DATA DISPLAY BIT 14 IND	-DATA-	-C1D04-	-X04-	-D04-	
DATA DISPLAY BIT 15 IND	-DATA-	-C1D05-	-X05-	-D05-	
DIAGNOSTIC MODE	-ROS-	-C3D09-	-W09-	-D09-	-C5B02-
GROUND	-DATA-	-C1D08-	-X08	-D08-	
GROUND	-ROS-	-C3D08-	-W08	-D08-	-C5D08-
INSTRUCTION STEP IND	-ROS-	-C3D11-	-W11-	-D11-	
LEVEL 00 IND	-ADDR-	-C2B09-	-W29-	-B09-	
LEVEL 01 IND	-ADDR-	-C2B10-	-W30-	-B10-	
LEVEL 02 IND	-ADDR-	-C2B11-	-W31-	-B11-	
LEVEL 03 IND	-ADDR-	-C2B12-	-W32-	-B12-	
LOAD IND	-ROS-	-C3D06-	-W06-	-D06-	-C5D06-
PRIMARY	-ROS-	-C3B09-	-W29-	-B09-	
ROW A	-ROS-	-C3B10-	-W30-	-B10-	
ROW B	-ROS-	-C3B03-	-W23-	-B03-	
ROW C	-ROS-	-C3B04-	-W24-	-B04-	
ROW D	-ROS-	-C3B05-	-W25-	-B05-	-C5B05-
RUN IND	-ROS-	-C3D04-	-W04-	-D04-	-C5D04-
STOP INDICATOR	-ROS-	-C3D10-	-W10-	-D10-	
STOP ON ADDRESS IND	-ROS-	-C3D12-	-W12-	-D12-	
STOP ON ERROR IND	-ROS-	-C3B06-	-W26-	-B06-	
WAIT IND	-ROS-	-C3D05-	-W05-	-D05-	-C5D05-
SPARE	-DATA-	-C1D12-	-X12-	-D12-	
SPARE	-DATA-	-C1D13-	-X13-	-D13-	
SPARE	-ROS-	-C3B02-	-W22-	-B02-	

CABLE CONNECTIONS

PROGRAMMER OR C.E MAINTENANCE CONS.

4952/4953 CABLE CONNECTIONS

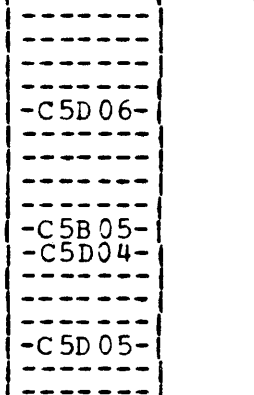
CONSOLE	PROCESS
C1	X
C2	YL
C3	W

C5 JUMPER C6

4955 CABLE CONNECTIONS

CONSOLE	PROCESS
C1	DATA X
C2	ADDR WL
C3	ROS W

C5 JUMPER C6



TYPICAL TOP CARD CONNECTOR

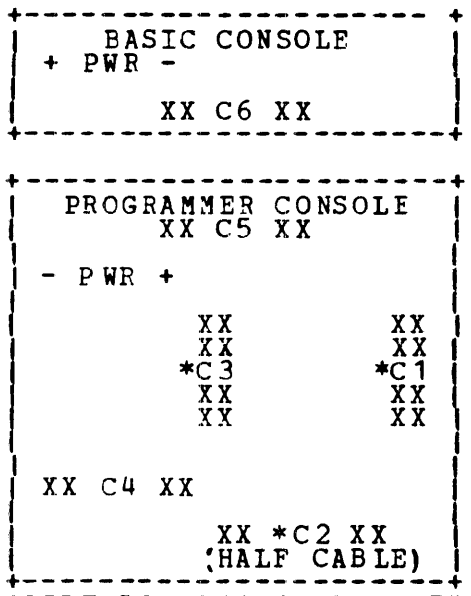
BASIC CONSOLE INSTALLED ONLY

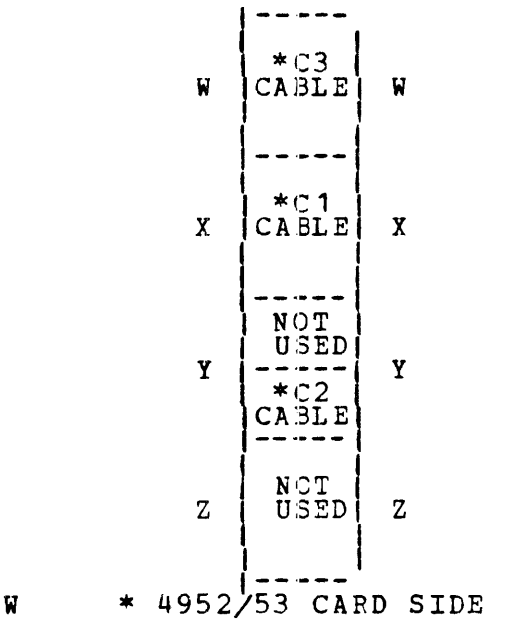
AUTO IPL MODE	-ROS-	-C3D07-	-WC7-	-----|	-C6D07-
COLUMN 00 --- (LOAD SW)	-ROS-	-C3D03-	-W03-	-----|	-C6D03-
DIAGNOSTIC MODE	-ROS-	-C3D09-	-W09-	-----|	-C6B02-
GROUND	-ROS-	-C3D08-	-W08-	-----|	-C6D08-
LOAD IND	-ROS-	-C3D06-	-WC6-	-----|	-C6D06-
PRIMARY	-ROS-	-C3B09-	-W29-	-----|	-C6B09-
ROW D (LOAD SW)	-ROS-	-C3B05-	-W25-	-----|	-C6B05-
RUN IND	-ROS-	-C3D04-	-W04-	-----|	-C6D04-
WAIT IND	-ROS-	-C3D05-	-W05-	-----|	-C6D05-

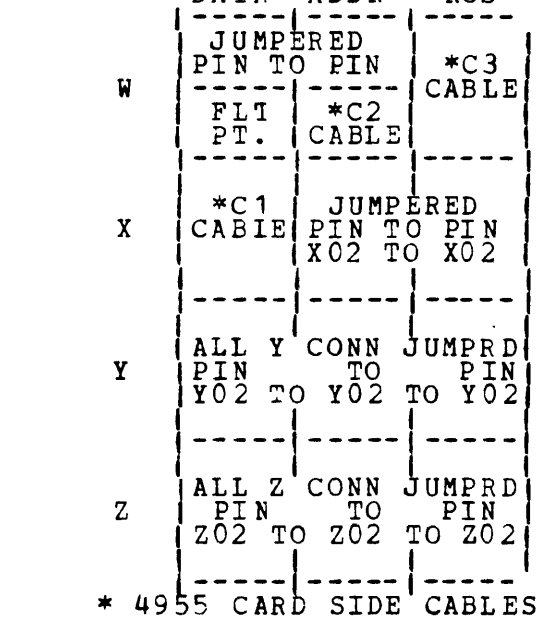
C3 CABLE CONNECTION

BASIC CONSOLE	PROC CARD
4952	C6 W
4953	C6 W
4955	C6 ROS W

* C3 CABLE FROM C6 TO PROCESSOR







CABLE LOCATIONS REAR VIEW

* 4952/53 CARD SIDE

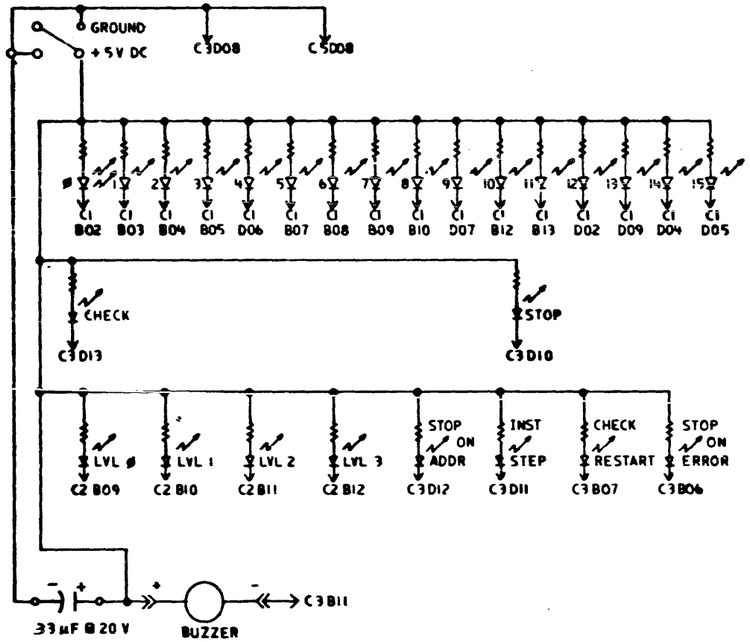
* 4955 CARD SIDE CABLES

* CONSOLE CABLES C1, C2 AND C3 ARE LABELED X, Y AND W ON THE PROCESSOR END.

SEE SERIES 1 THEORY DIAGRAMS MANUAL FOR DATA FLOW

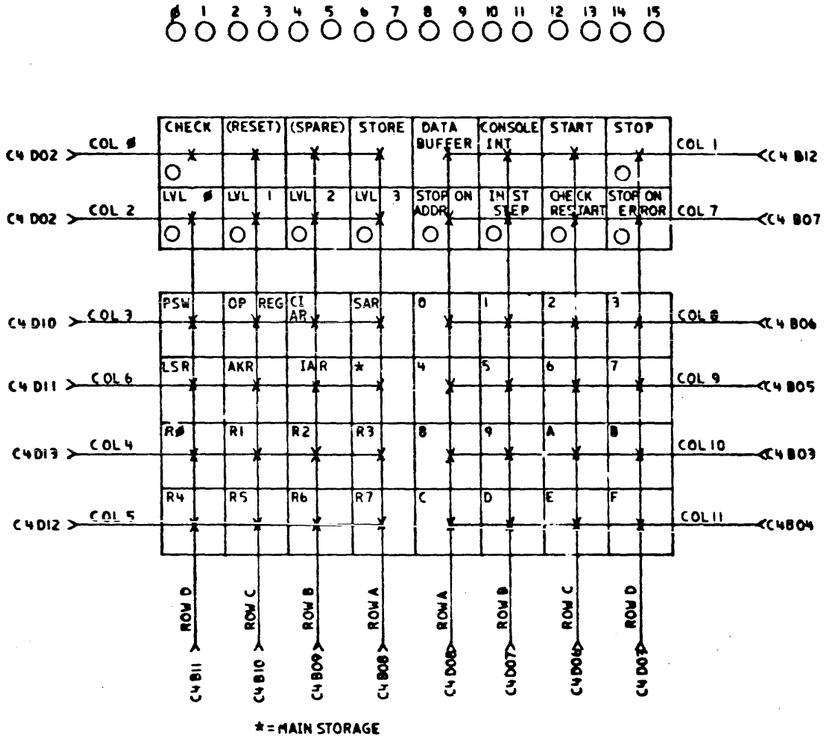
SERIES 1 PROGRAMMER OR CE CONSOLE

E.C. HISTORY		MACH.	P
06-21-76	578446		A
10-01-76	578468	SERIES 1	1
12-02-76	578469		0
03-15-77	578714		0
07-12-77	578984		
01-15-79	375147	IBM CCRP. GSD	
DATE	LAST E.C.		0 0 0
04-20-79	375401	P.N. 1635004	



NOTE:

1 ALL LED RESISTORS ARE 200 Ω (R-PAC)



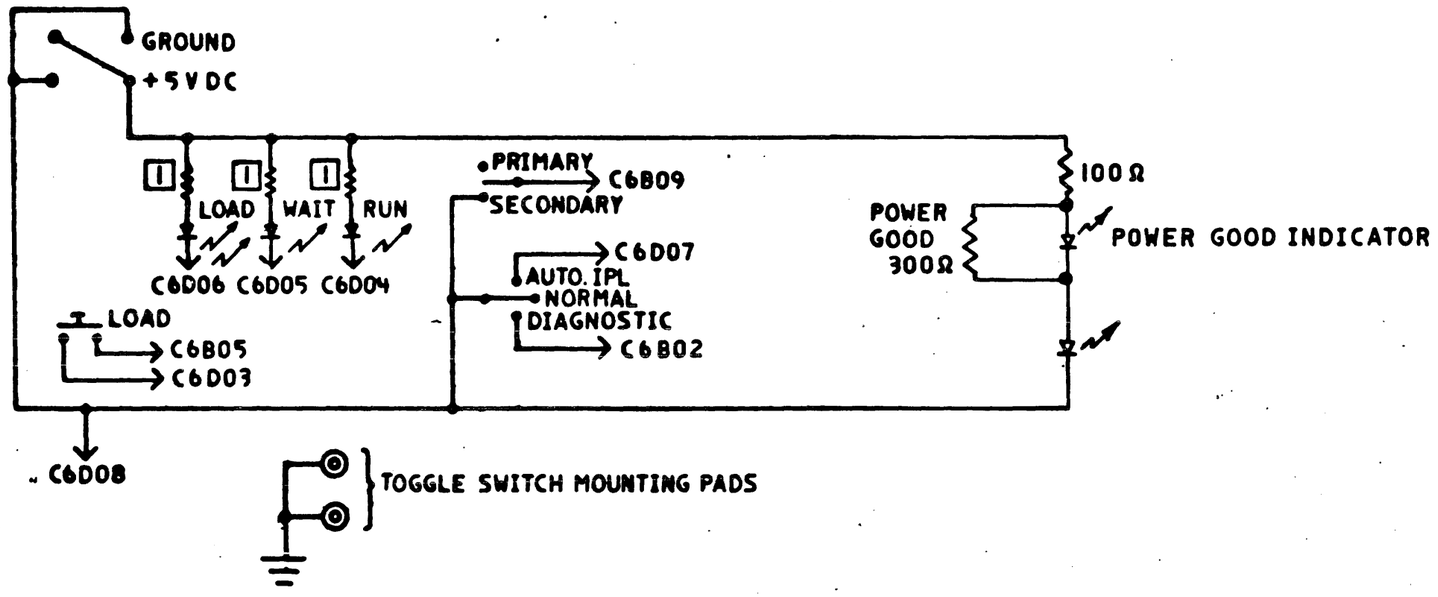
*= MAIN STORAGE

EC HISTORY		DRAWING TITLE
2 MAY 77	578751	FULL FUNCTION CONSOLE WIRING DIAGRAM
30 SEP 77	754882	MACH
		PART NO 4414120
C		CLASSIFICATION

IBM CORP

PA105

PA105



PA110

NOTE

[1] RESISTORS ARE 200Ω (R-PAC)

EC HISTORY		DRAWING TITLE
29 APR 77	578751	BASIC CONSOLE WIRING DIAGRAM
		MACH
		PART NO 4414121
		CLASSIFICATION

B

IBM CORP

PA110

1310 MULTI-FUNCTION ATTACHMENT CARD

STANDARD CHANNEL

```
ADDRESS BUS BIT--00------B02
ADDRESS BUS BIT--01------B03
ADDRESS BUS BIT--02------B04
ADDRESS BUS BIT--03------B05
ADDRESS BUS BIT--04------B07
ADDRESS BUS BIT--05------B08
ADDRESS BUS BIT--06------B09
ADDRESS BUS BIT--07------B10
ADDRESS BUS BIT--08------B12
ADDRESS BUS BIT--09------D02
ADDRESS BUS BIT--10------D04
ADDRESS BUS BIT--11------D05
ADDRESS BUS BIT--12------D06
ADDRESS BUS BIT--13------D07
ADDRESS BUS BIT--14------D09
ADDRESS BUS BIT--15------D10
ADDRESS BUS BIT--16------D11
ADDRESS GATE------------M08
ADDRESS GATE RETURN-----M09
# BURST RETURN-----------(P04)
CONDITION CODE IN BIT-00-D12
CONDITION CODE IN BIT-01-D13
CONDITION CODE IN BIT-02-B13
CS BYTE INDICATOR-------P10
INPUT INDICATOR---------P09
CYCLE STEAL REQUEST IN---M02
DATA BUS BIT-----00------G02
DATA BUS BIT-----01------G03
DATA BUS BIT-----02------G04
DATA BUS BIT-----03------G05
DATA BUS BIT-----04------G07
DATA BUS BIT-----05------G08
DATA BUS BIT-----06------G09
DATA BUS BIT-----07------G10
DATA BUS BIT-----P0------G12
DATA BUS BIT-----08------J02
DATA BUS BIT-----09------J04
DATA BUS BIT-----10------J05
DATA BUS BIT-----11------J06
DATA BUS BIT-----12------J07
DATA BUS BIT-----13------J09
DATA BUS BIT-----14------J10
DATA BUS BIT-----15------J11
DATA BUS BIT-----P1------J12
DATA STROBE-------------M10
HALT OR MCHK------------M07
INITIATE IPL------------P07
IPL---------------------S04
POLL--------------------M12
POLL IDENTIFIER BIT--00--P11
POLL IDENTIFIER BIT--01--S02
POLL IDENTIFIER BIT--02--S03
POLL IDENTIFIER BIT--03--P12
POLL IDENTIFIER BIT--04--P13
POLL PRIME--------------M13
POLL PROPAGATE----------M11
POLL RETURN-------------M04
POWER ON RESET (POR)-----S05
REQUEST IN BUS BIT--00---S07
REQUEST IN BUS BIT--01---S08
REQUEST IN BUS BIT--02---S09
REQUEST IN BUS BIT--03---S10
REQUEST IN BUS BIT--04---S12
REQUEST IN BUS BIT--05---S13
REQUEST IN BUS BIT--06---U02
REQUEST IN BUS BIT--07---U04
REQUEST IN BUS BIT--08---U05
REQUEST IN BUS BIT--09---U06
REQUEST IN BUS BIT--10---U07
REQUEST IN BUS BIT--11---U09
REQUEST IN BUS BIT--12---U10
REQUEST IN BUS BIT--13---U11
REQUEST IN BUS BIT--14---U12
REQUEST IN BUS BIT--15---U13
SERVICE GATE------------P05
SERVICE GATE RETURN-----P06
CS STATUS BUS BIT---00---J13
CS STATUS BUS BIT---01---G13
CS STATUS BUS BIT---02---M03
CS STATUS BUS BIT---03---P02
SYSTEM RESET------------M05
```

\# = LINE NOT USED BY THIS ATTACHMENT
CS = CYCLE STEAL

VOLTAGE PIN ASSIGNMENT

```
+5-----D03--J03--P03--U03
-5-----G06
+8.5---G11
+12.5--B11
-12.5--B06
GND----D08--J08--P08--U08
```

TOP CARD CONNECTORS

INDICATOR PANEL CONNECTOR

```
J2A05-- -FUNCTION/DISPLAY SW 01
J2A06-- -FUNCTION/DISPLAY SW 02
J2B06-- -FUNCTION/DISPLAY SW 04
J2A07-- -FUNCTION/DISPLAY SW 08
J2B07-- -FUNCTION/DISPLAY SW 16
J2B01--  GROUND
J2B12-- -LAMP DRIVER  00
J2A12-- -LAMP DRIVER  01
J2B11-- -LAMP DRIVER  02
J2A11-- -LAMP DRIVER  03
J2B10-- -LAMP DRIVER  04
J2A10-- -LAMP DRIVER  05
J2B09-- -LAMP DRIVER  06
J2A09-- -LAMP DRIVER  07
J2A04-- -LINE SELECT SW  01
J2B04-- -LINE SELECT SW  02
J2A05-- -LINE SELECT SW  04
J2A03-- +5 VOLTS
J2A01, A02, A08--NOT USED
J2B02, B03, B08--NOT USED
```

DATASET INTERFACE CABLE

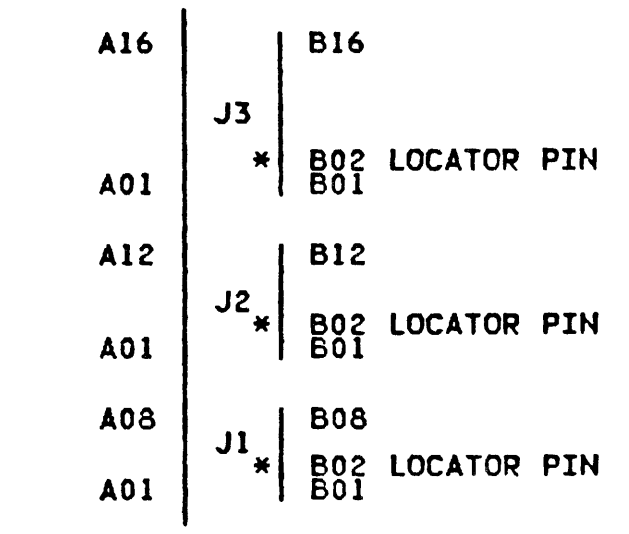
		MODEM PIN
J1B03--	+CLEAR TO SEND	05
J1B01--	+DATA SET READY	06
J1A02--	-DATA SIGNAL RATE SELECT	23
J1A01--	+DATA TERMINAL READY	20
J1B06--	+RECEIVE CLOCK	17
J1B04--	-RECEIVE DATA	03
J1A03--	+REQUEST TO SEND	04
J1B07--	+RING INDICATOR	22
J1A08--	SIGNAL GROUND	07
J1A06--	+TRANSMIT CLOCK	15
J1A04--	+TRANSMIT DATA	02

J1A05, A07, B02, B05, B08-NOT USED

DATASET CABLE

```
J3A01 +XMIT DATA OUT (4) BASE ADDR+3
J3A04 -XMIT DATA OUT (4) BASE ADDR+3
J3A05 +XMIT DATA OUT (3) BASE ADDR+2
J3A08 -XMIT DATA OUT (3) BASE ADDR+2
J3A09 +XMIT DATA OUT (2) BASE ADDR+1
J3A12 -XMIT DATA OUT (2) BASE ADDR+1
J3A13 +XMIT DATA OUT (1) BASE ADDR
J3A16 -XMIT DATA OUT (1) BASE ADDR
J3B01 +RCV DATA IN (4) BASE ADDR+3
J3B04 -RCV DATA IN (4) BASE ADDR+3
J3B05 +RCV DATA IN (3) BASE ADDR+2
J3B08 -RCV DATA IN (3) BASE ADDR+2
J3B09 +RCV DATA IN (2) BASE ADDR+1
J3B12 -RCV DATA IN (2) BASE ADDR+1
J3B13 +RCV DATA IN (1) BASE ADDR
J3B16 -RCV DATA IN (1) BASE ADDR
J3A02, A03, A06, A07, A10,
   A11, A14, A15--NOT USED
J3B02, B03, B06, B07, B10,
   B11, B14, B15--NOT USED
```

TOP CARD CONNECTORS



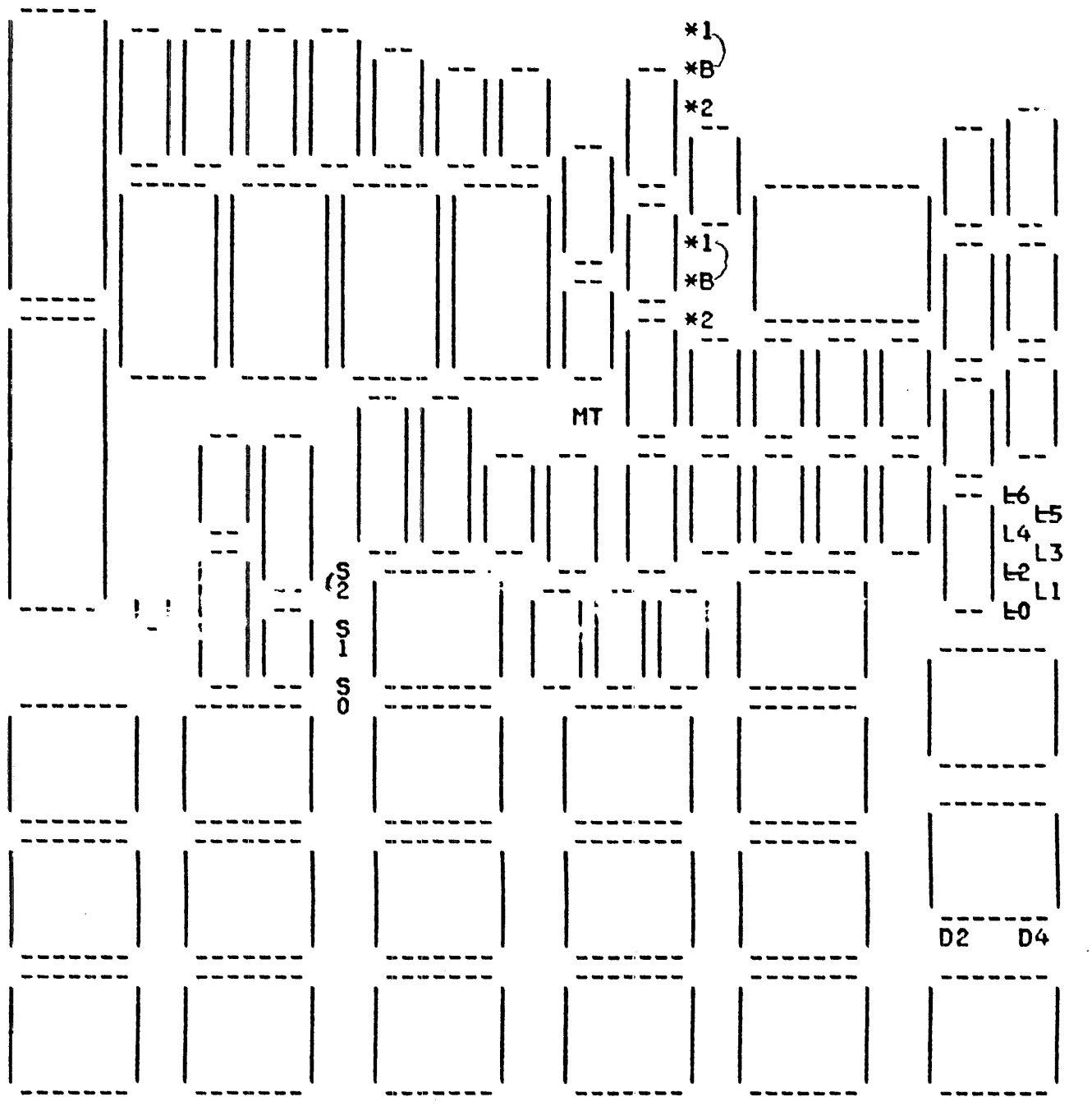
MULTI-FUNCTION ATTACHMENT
FEATURE # 1310

E.C. HISTORY
DATE | E. C. | MACH.
SERIES/1

IBM CORP. GSD
DATE | LAST E.C. | P.N. 8257771

SC425 000

MULTI-FUNCTION CARD JUMPER LOCATIONS



MFA IDENTIFICATION WORD (0011 00DD 0011 0110)

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	0	1	1	0	0	X	X	0	0	1	1	0	1	1	0
	SEE NOTE 1															

SERIES/1 DEVICE ADDRESS

BIT	8	9	10	11	12	13	14	15
	0	1	0	1	1	0	0	
	L0	L1	L2	L3	L4	L5	L6	0

(JUMPER ON = LOGICAL 0, BIT 15 ALWAYS 0)

NOTE 1: THE RELATIONSHIP BETWEEN THE TWO DEVICE COUNT (DOMAIN) JUMPERS AND THE ID WORD IS SHOWN IN THE FOLLOWING TABLE:

DEVICE COUNT	JUMPERS D2	JUMPERS D4	ID BITS 6	ID BITS 7
1	ON	ON	0	1
2	ON	OFF	0	1
3	OFF	ON	1	0
4	OFF	OFF	1	0

B = BIAS JUMPERS. THE TWO BIAS JUMPERS MUST ALWAYS BE PRESENT. THE JUMPERS CAUSE THE RS-422-A INTERFACES TO BE IN THE MARK (B1) OR SPACE (B2) CONDITION WHEN NO CABLE IS ATTACHED.

MT = MULTIPOINT TRIBUTARY JUMPER. WHEN THIS JUMPER IS OFF, JUMPERS S0, S1 AND S2 TAKE ON THE FOLLOWING MEANING:

- S2 ON: IPL DISABLED
- S1 ON: ANSWERTONE PROVIDED
- S0 ON: SWITCHED LINE IN USE

WHEN THE MT JUMPER IS ON (LOGICAL 1), THE SECONDARY STATION ADDRESS IS CX, WHERE X IS DETERMINED BY JUMPERS S0, S1, AND S2:

SEC. STA. ADDRESS	JUMPERS S2	S1	S0
C0	OFF	OFF	OFF
C1	OFF	OFF	ON
C2	OFF	ON	OFF
C3	OFF	ON	ON
C4	ON	OFF	OFF
C5	ON	OFF	ON
C6	ON	ON	OFF
C7	ON	ON	ON

(JUMPER ON = LOGICAL 1)

NOTE:
INSTALL THE MT JUMPER ONLY IF REMOTE IPL IS REQUIRED.
THE MT, S0, S1, AND S2 JUMPERS ARE NOT USED AFTER THE MULTI-FUNCTION ATTACHMENT IS INITIALIZED.

1310 MULTI-FUNCTION ATTACHMENT

EC HISTORY		MACHINES
15JAN81	987656	
28MAY81	988013	
24SEP81	323285	SERIES 1

IBM CORP. ISD

DATE	LAST E.C.	P.N.
22MAR82	467043	8257772

S C4 28 000

FEATURE PROGRAMMABLE MULTI LINE COMMUNICATIONS CONTROLLER
FEATURE CODE 2095

STANDARD CHANNEL

```
  ADDRESS BUS BIT--00------B02
  ADDRESS BUS BIT--01------B03
  ADDRESS BUS BIT--02------B04
  ADDRESS BUS BIT--03------B05
  ADDRESS BUS BIT--04------B07
  ADDRESS BUS BIT--05------B08
  ADDRESS BUS BIT--06------B09
  ADDRESS BUS BIT--07------B10
  ADDRESS BUS BIT--08------B12
  ADDRESS BUS BIT--09------D02
  ADDRESS BUS BIT--10------D04
  ADDRESS BUS BIT--11------D05
  ADDRESS BUS BIT--12------D06
  ADDRESS BUS BIT--13------D07
  ADDRESS BUS BIT--14------D09
  ADDRESS BUS BIT--15------D10
  ADDRESS BUS BIT--16------D11
  ADDRESS GATE------------M08
  ADDRESS GATE RETURN------M09
# BURST RETURN------------(P04)
  CONDITION CODE IN BIT-00-D12
  CONDITION CODE IN BIT-01-D13
  CONDITION CODE IN BIT-02-B13
  CYCLE BYTE INDICATOR-----P10
  CYCLE INPUT INDICATOR----P09
  CYCLE STEAL REQUEST IN---M02
  DATA BUS BIT-----00------G02
  DATA BUS BIT-----01------G03
  DATA BUS BIT-----02------G04
  DATA BUS BIT-----03------G05
  DATA BUS BIT-----04------G07
  DATA BUS BIT-----05------G08
  DATA BUS BIT-----06------G09
  DATA BUS BIT-----07------G10
  DATA BUS BIT-----P0------G12
  DATA BUS BIT-----08------J02
  DATA BUS BIT-----09------J04
  DATA BUS BIT-----10------J05
  DATA BUS BIT-----11------J06
  DATA BUS BIT-----12------J07
  DATA BUS BIT-----13------J09
  DATA BUS BIT-----14------J10
  DATA BUS BIT-----15------J11
  DATA BUS BIT-----P1------J12
  DATA STROBE-------------M10
  HALT OR MCHK------------(M07)
# INITIATE IPL------------(P07)
# IPL----------------------S04
  POLL---------------------M12
  POLL IDENTIFIER BIT--00--P11
  POLL IDENTIFIER BIT--01--S02
  POLL IDENTIFIER BIT--02--S03
  POLL IDENTIFIER BIT--03--P12
  POLL IDENTIFIER BIT--04--P13
  POLL PRIME---------------M13
  POLL PROPAGATE-----------M11
  POLL RETURN--------------M04
  POWER ON RESET-----------S05
  REQUEST IN BUS BIT--00---S07
  REQUEST IN BUS BIT--01---S08
  REQUEST IN BUS BIT--02---S09
  REQUEST IN BUS BIT--03---S10
  REQUEST IN BUS BIT--04---S12
  REQUEST IN BUS BIT--05---S13
  REQUEST IN BUS BIT--06---U02
  REQUEST IN BUS BIT--07---U04
  REQUEST IN BUS BIT--08---U05
  REQUEST IN BUS BIT--09---U06
  REQUEST IN BUS BIT--10---U07
  REQUEST IN BUS BIT--11---U09
  REQUEST IN BUS BIT--12---U10
  REQUEST IN BUS BIT--13---U11
  REQUEST IN BUS BIT--14---U12
  REQUEST IN BUS BIT--15---U13
  SERVICE GATE-------------P05
  SERVICE GATE RETURN------P06
  STATUS BUS BIT------00---J13
  STATUS BUS BIT------01---G13
  STATUS BUS BIT------02---M03
  STATUS BUS BIT------03---P02
  SYSTEM RESET-------------M05
```

CONTROLLER TOP CARD CONNECTOR(S)

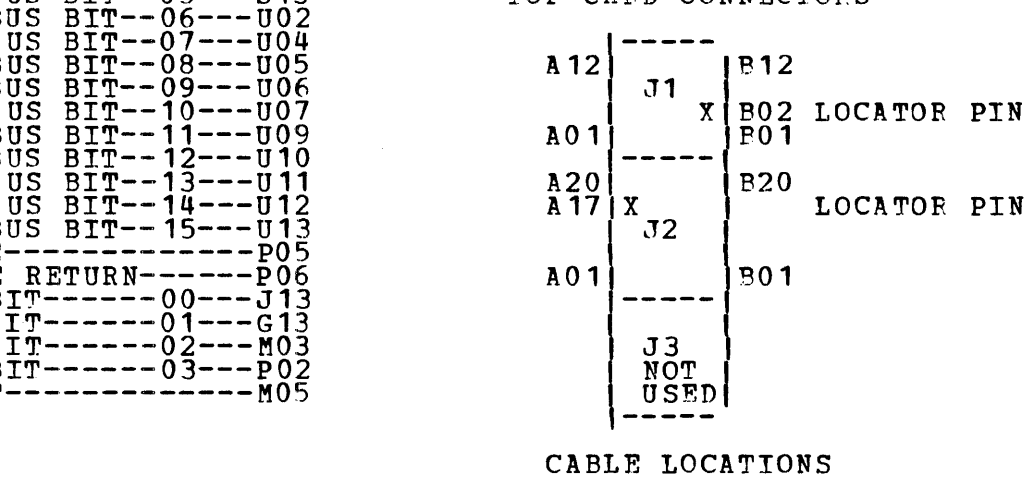
INDICATOR PANEL CONNECTOR

```
  J1B05-- -FUNCTION/DISPLAY SW   01
  J1A06-- -FUNCTION/DISPLAY SW   02
  J1B06-- -FUNCTION/DISPLAY SW   04
  J1A07-- -FUNCTION/DISPLAY SW   08
  J1B07-- -FUNCTION/DISPLAY SW   16
  J1B01--  GROUND
  J1B12-- -LAMP DRIVER   00
  J1A12-- -LAMP DRIVER   01
  J1B11-- -LAMP DRIVER   02
  J1A11-- -LAMP DRIVER   03
  J1B10-- -LAMP DRIVER   04
  J1A10-- -LAMP DRIVER   05
  J1B09-- -LAMP DRIVER   06
  J1A09-- -LAMP DRIVER   07
  J1A04-- -LINE SELECT SW   01
  J1B04-- -LINE SELECT SW   02
  J1A05-- -LINE SELECT SW   04
  J1A03-- +5V
```

ADAPTER CONNECTOR CABLE

```
  J2B18-- -ADDRESS BUS OUT BIT   00
  J2B19-- -ADDRESS BUS OUT BIT   01
  J2A18-- -ADDRESS BUS OUT BIT   02
  J2A19-- -ADDRESS BUS OUT BIT   03
  J2B12-- -ADDRESS BUS OUT BIT   04
  J2B13-- -ADDRESS BUS OUT BIT   05
  J2B14-- -ADDRESS BUS OUT BIT   06
  J2B15-- -ADDRESS BUS OUT BIT   07
  J2B16-- -CONTROL STROBE POWERED
  J2A08-- -DATA BUS IN BIT   00
  J2A09-- -DATA BUS IN BIT   01
  J2A10-- -DATA BUS IN BIT   02
  J2A11-- -DATA BUS IN BIT   03
  J2A15-- -DATA BUS IN BIT   04
  J2A14-- -DATA BUS IN BIT   05
  J2A12-- -DATA BUS IN BIT   06
  J2A13-- -DATA BUS IN BIT   07
  J2B03-- -DATA BUS OUT BIT   00
  J2B04-- -DATA BUS OUT BIT   01
  J2B05-- -DATA BUS OUT BIT   02
  J2B06-- -DATA BUS OUT BIT   03
  J2B07-- -DATA BUS OUT BIT   04
  J2B08-- -DATA BUS OUT BIT   05
  J2B09-- -DATA BUS OUT BIT   06
  J2B10-- -DATA BUS OUT BIT   07
  J2B11-- -HEX F
  J2A04-- +LINE LATCH   00
  J2A05-- +LINE LATCH   01
  J2A06-- +LINE LATCH   02
  J2A07-- +LINE LATCH   03
  J2A01-- +LINE LATCH   04
  J2A02-- +LINE LATCH   05
  J2A03-- +LINE LATCH   06
  J2B01-- +LINE LATCH   07
  J2B17-- -SENSE STROBE
  J2A16--  153.6 KHZ
  J2B20-- -1.63 USEC. CLK
  J2A20-- -6.66 MSEC CLK
# J2B02--  NOT USED
```

TOP CARD CONNECTORS



CABLE LOCATIONS

VOLTAGE PIN ASSIGNMENTS
+5V---D03--J03--P03--U03
GND---D08--J08--P08--U08
-5V---G06
+8.5V-G11

LINES ARE NOT USED BY THIS ATTACHMENT.

SEE THE PROCESSOR THEORY DIAGRAMS MANUAL FOR DATA FLOW.

F P M L COMMUNICATIONS CONTROLLER

E.C. HISTORY

MACH. SERIES/1

SC450

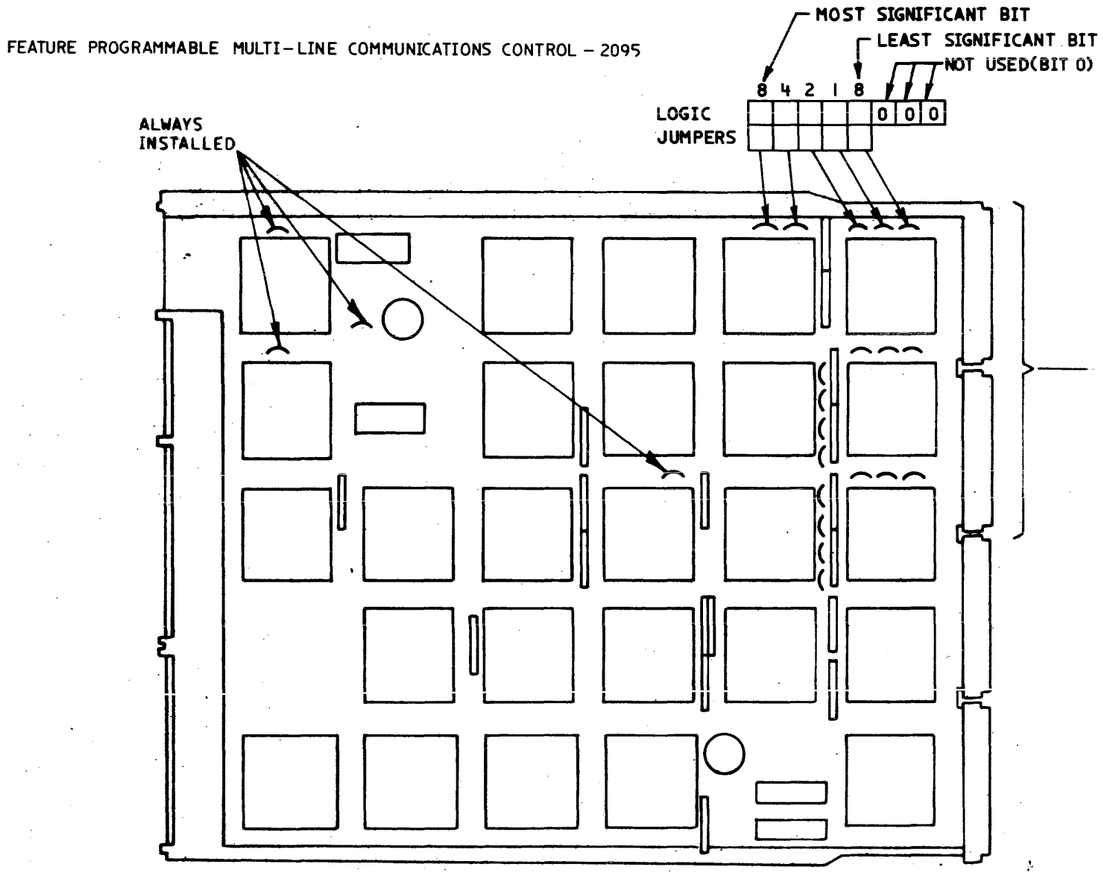
IBM CORP. GSD

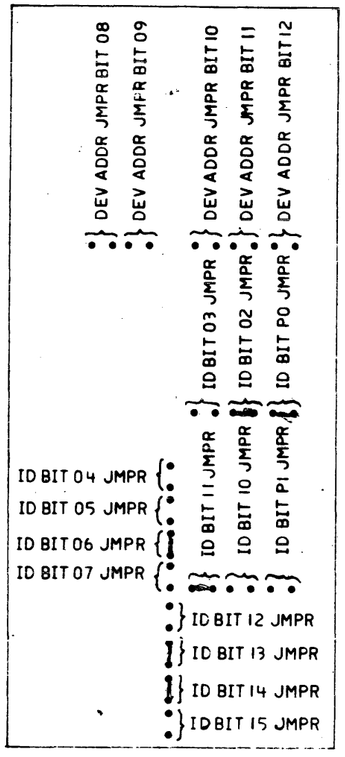
DATE 23-02-79 LAST E.C. 375094

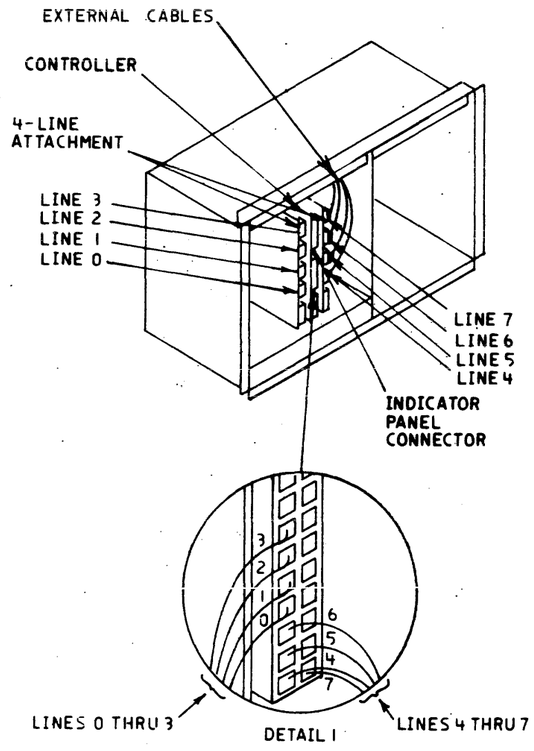
P.N. 6839764

0 0 0

FEATURE PROGRAMMABLE MULTI-LINE COMMUNICATIONS CONTROL - 2095







NOTE:
TO INSURE PROPER INSTALLATION OF THE CABLE BETWEEN THE CONTROLLED CARD AND THE 4-LINE ATTACHMENT CARDS SEE DETAIL 1

NOTES:

THE FEATURE PROGRAMMABLE MULTI-LINE COMMUNICATIONS CONTROL ID WORD IS JUMPERED OR WIRE WRAPPED AS FOLLOWS:

BIT 2 - ON
BITS 3,4,5 - OFF
BITS 6&7 - DETERMINED BY THE NUMBER OF LINES ATTACHED. FOR TWO LINES JUMPER ON BIT 7; FOR FOUR LINES JUMPER ON BIT 6; FOR SIX LINES JUMPER ON BOTH 6&7; FOR EIGHT LINES NO JUMPERS ON 6 OR 7
BIT PO - JUMPERED AS REQUIRED TO MAKE BIT 2 THRU 7 ODD PARITY - 2 LINES = PO ON, 4 LINES = PO ON, 6 LINES = PO OFF, 8 LINES = PO OFF
BITS 10,12,PI-OFF
BITS 11,13,14-ON
DEVICE ADDRESS JUMPERS ON = LOGICAL 1
TYPICAL DEV ADDR: 48 = HEX 01001000

SC455

EC HISTORY		DRAWING TITLE
14MAR79	375094	FEAT. PROGRAMMABLE MULTI-LINE COMM'S. CONT.
16 AUG 79	375589	MACH SERIES/1
10 MAR 82	326765	PART NO 6839765
C		CLASSIFICATION

IBM CORP

SC455

FEATURE PROGRAMMABLE FOUR (4) COMMUNICATIONS LINE ADAPTER CARD
FEATURE 2096

STANDARD CHANNEL

POLL----------M12
POLL PRIME ----------M13
POLL PROPAGATE----------M11

NOTE-
FOR POLL PROPAGATION ONLY.
NOT USED BY ADAPTER CARD.

TOP CARD CONNECTORS

DATASET INTERFACE CABLE — MODEM
FEATURE CODE 2057 PIN
(WHEN LINE IS JUMPERED FOR EIA RS232C / CCITT V.24)

	JXB03-- +CLEAR TO SEND	05
	JXB01-- +DATA SET READY	06
	JXA02-- -DATA SIGNAL RATE SELECT	23
	JXA01-- +DATA TERMINAL READY	20
	JXA07-- +DATA CARRIER DETECT	08
#	JXB08-- -MODEM TEST	
	JXB06-- +RECEIVE CLOCK	17
	JXB04-- -RECEIVE DATA	03
	JXA03-- +REQUEST TO SEND	04
#	JXA05-- RESERVED	
#	JXB05-- RESERVED	
	JXB07-- +RING INDICATOR	22
	JXA08-- SIGNAL GROUND	07
	JXA06-- +TRANSMIT CLOCK	15
	JXA04-- -TRANSMIT DATA	02

CURRENT LOOP INTERFACE CABLE
FEATURE CODE 2061
(WHEN LINE JUMPERED FOR CURRENT LOOP)

	JXA05--	-XMIT DATA RTN	+XMIT WHITE
	JXA06--	-XMIT BIAS RTN	-XMIT RED
	JXB05--	-RCV DATA RTN	+RCV BLACK
	JXB06--	-RCV BIAS RTN	-RCV YELLOW
	JXA01--	+DATA TERMINAL READY	JUMPER 1
	JXB01--	+DATA SET READY	JUMPER 1
#	JXA02--	+RATE SELECT	NOT USED
	JXA03--	+REQUEST TO SEND	JUMPER 2
	JXB03--	+CLEAR TO SEND	JUMPER 2
	JXA04--	+XMIT DATA	JUMPER 3
	JXA07--	+XMIT BIAS	JUMPER 3
	JXB04--	+RCV DATA	JUMPER 4
	JXB07--	+RCV BIAS	JUMPER 4
#	JXA08--	GROUND	NOT USED
#	JXB08--	-MODEM TEST	NOT USED

** JX=ANY MODEM CABLE, J1 TO J4

TOP CARD CONNECTORS

A08	J1 LINE 3/7	B08	
	X	B02	LOCATOR PIN
A01		B01	
A08	J2 LINE 2/6	B08	
	X	B02	LOCATOR PIN
A01		B01	
A08	J3 LINE 1/5	B08	
	X	B02	LOCATOR PIN
A01		B01	
A08	J4 LINE 0/4	B08	
	X	B02	LOCATOR PIN
A01		B01	
A20		B20	
A17	X J5		LOCATOR PIN
A01		B01	

CABLE LOCATIONS

CONTROLLER CONNECTOR CABLE

#	J5B18--	-ADDRESS BUS OUT BIT 00
#	J5B19--	-ADDRESS BUS OUT BIT 01
#	J5A18--	-ADDRESS BUS OUT BIT 02
#	J5A19--	-ADDRESS BUS OUT BIT 03
	J5B12--	ADDRESS BUS OUT BIT 04
	J5B13--	-ADDRESS BUS OUT BIT 05
	J5B14--	-ADDRESS BUS OUT BIT 06
	J5B15--	-ADDRESS BUS OUT BIT 07
	J5B16--	-CONTROL STROBE POWERED
	J5A08--	-DATA BUS IN BIT 00
	J5A09--	-DATA BUS IN BIT 01
	J5A10--	-DATA BUS IN BIT 02
	J5A11--	-DATA BUS IN BIT 03
	A5A15--	-DATA BUS IN BIT 04
	J5A14--	-DATA BUS IN BIT 05
	J5A12--	-DATA BUS IN BIT 06
	J5A13--	-DATA BUS IN BIT 07
	J5B03--	-DATA BUS OUT BIT 00
	J5B04--	-DATA BUS OUT BIT 01
	J5B05--	-DATA BUS OUT BIT 02
	J5B06--	-DATA BUS OUT BIT 03
	J5B07--	-DATA BUS OUT BIT 04
	J5B08--	-DATA BUS OUT BIT 05
	J5B09--	-DATA BUS OUT BIT 06
	J5B10--	-DATA BUS OUT BIT 07
	J5B11--	-HEX F
	J5A04--	+LINE LATCH 00/04
	J5A05--	+LINE LATCH 01/05
	J5A06--	+LINE LATCH 02/06
	J5A07--	+LINE LATCH 03/07
	J5B17--	-SENSE STROBE
#	J5A16--	-153.6 KHZ
#	J5B20--	-1.63 USEC. CLOCK
	J5A20--	-6.66 MSEC CLOCK
#	J5B02--	NOT USED

VOLTAGE PIN ASSIGNMENTS
+5V---D03--J03--P03--U03
GND---D08--J08--P08--U08
-12V--B06
+12V--B11

LINES ARE NOT USED BY THIS ADAPTER.

SEE THE PROCESSOR THEORY DIAGRAMS MANUAL FOR DATA FLOW.

F P 4 LINE COMMUNICATIONS ADAPTER

E.C. HISTORY — MACH. SERIES/1

E. C. 375094

IBM CORP. GSD

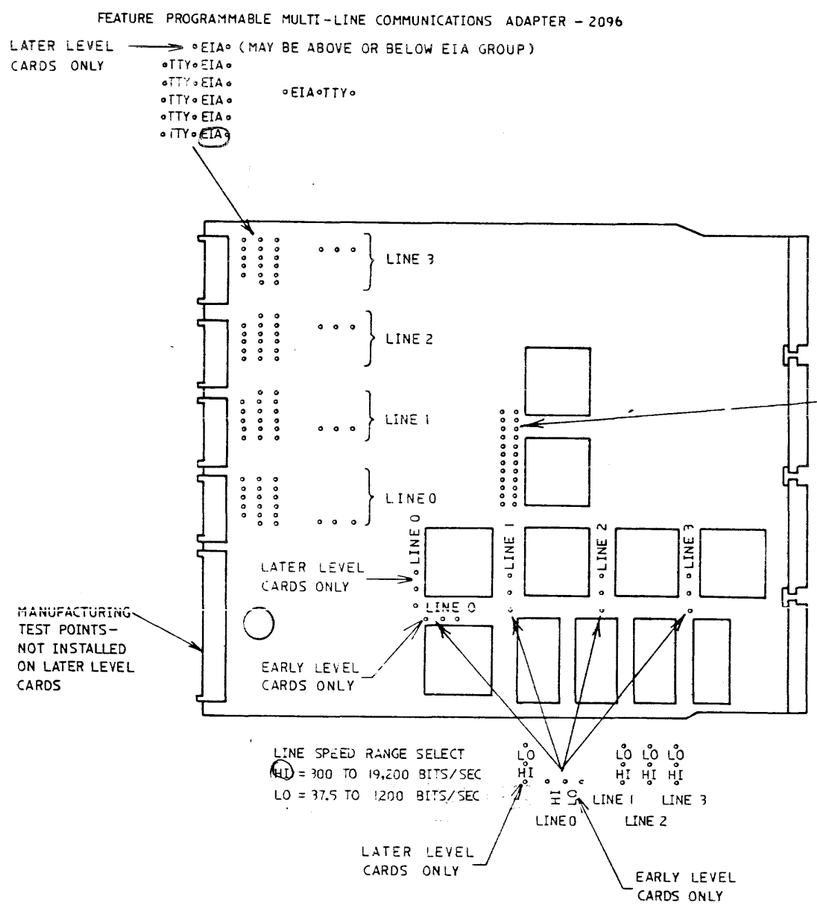
DATE 16-07-79 — LAST E.C. 375589 — P.N. 6839766

SC4600 000

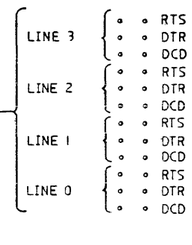
254-1264 BILL

SC465

FEATURE PROGRAMMABLE MULTI-LINE COMMUNICATIONS ADAPTER - 2096



EIA / TTY JUMPERS
MUST BE INSTALLED AS A GROUP OF 6 (TTY) OR 7 (EIA) JUMPERS.
EIA = RS232C/CCITT V.24
TTY = CURRENT LOOP INTERFACE



MODEM CONTROL JUMPERS
INSTALLED AS REQUIRED BY USER CONFIGURATION. IF JUMPER IS INSTALLED, IT UNCONDITIONALLY ACTIVATES SIGNAL.
RTS = REQUEST TO SEND (TO MODEM)
DTR = DATA TERMINAL READY (TO MODEM)
DCD = DATA CARRIER DETECT (TO ADAPTER)

NOTE: FOR DIRECT CONNECT APPLICATIONS OR CURRENT LOOP APPLICATIONS INSTALL DCD, DTR AND RTS JUMPERS FOR EACH LINE IN USE

SC465

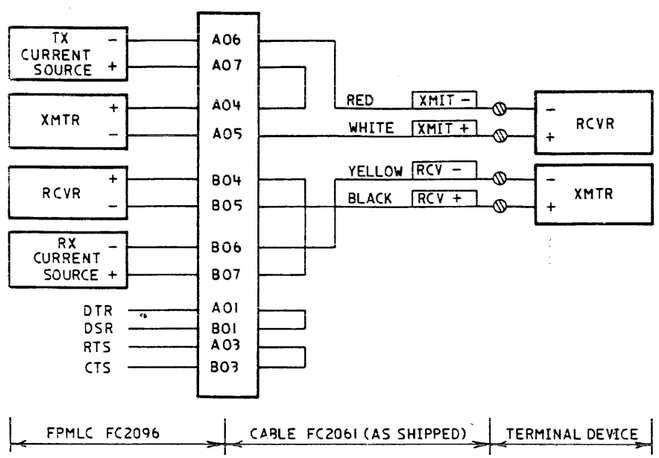
EC HISTORY		DRAWING TITLE	
14 MAR 79	375094	FEATURE PROGRAMMABLE MULTI-LINE COMM'S.	
15 AUG 79	375589	MACH SERIES 1	
14 SEP 79	375743	PART NO 6839767	
15 MAY 81	987965	CLASSIFICATION	IBM CORP
C			

SC465

SC470

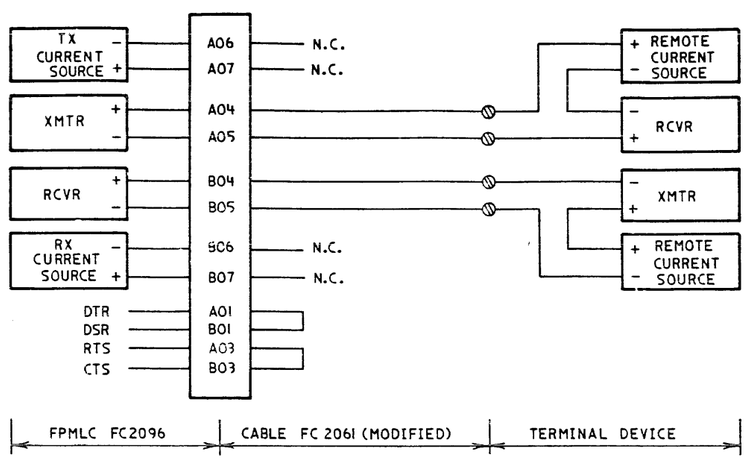
CONFIGURATION # 1

4-WIRE, FC 2096 SUPPLIES 20MA FOR BOTH LOOPS



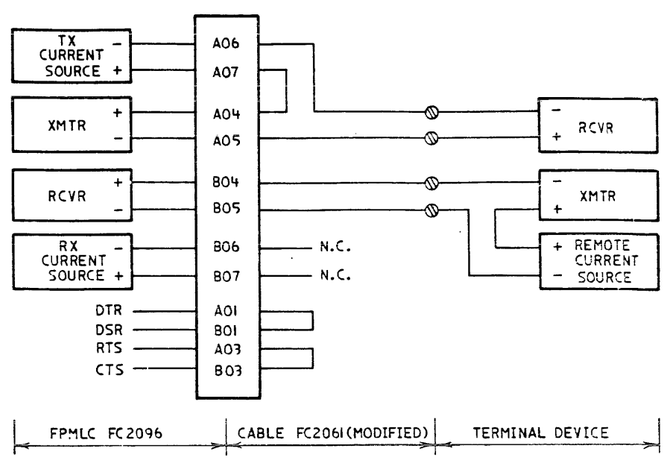
CONFIGURATION # 2

4-WIRE, REMOTE CURRENT SOURCES SUPPLY 20MA/60MA FOR BOTH LOOPS



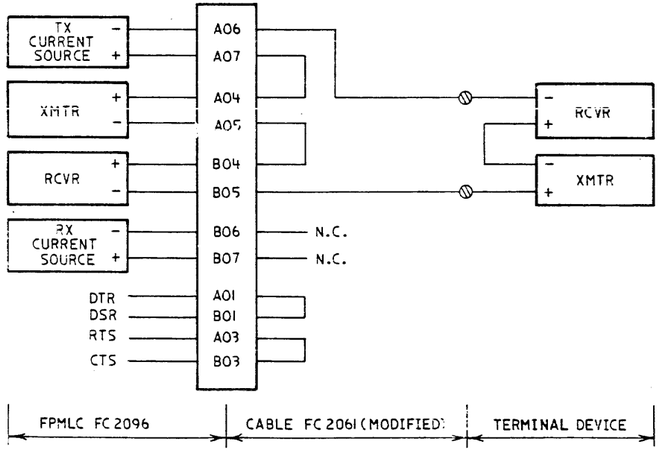
CONFIGURATION # 3

4-WIRE, EACH DEVICE POWERS ITS TRANSMIT LOOP



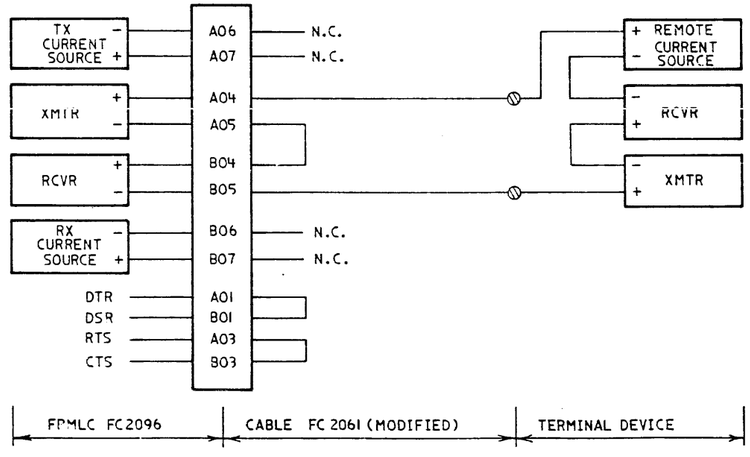
CONFIGURATION # 4

2-WIRE, FC 2096 SUPPLIES 20MA FOR LOOP



CONFIGURATION # 5

2-WIRE, REMOTE CURRENT SOURCE SUPPLIES 20MA/60MA FOR LOOP



NOTES:

1. CONFIGURATION # 1 REPRESENTS CABLE ASSEMBLY FC 2061 AS SHIPPED. OTHER CONFIGURATIONS ARE ACCOMPLISHED BY REARRANGING FOUR WIRES AND TWO JUMPERS AT THE CABLE ASSEMBLY BERG CONNECTOR
2. CONFIGURATION # 3 IS RECOMMENDED FOR LONGER CABLE RUNS AND/OR HIGHER DATA RATES
3. ECHO PLEX IS PROVIDED BY FC 2096 AS A PROGRAMABLE OPTION

SC470

EC HISTORY		DRAWING TITLE
23AUG79	375589	FPMLC CURRENT LOOP CONFIGURATION
	987965	MACH
		PART NO 6841485
		CLASSIFICATION

D

IBM CORP

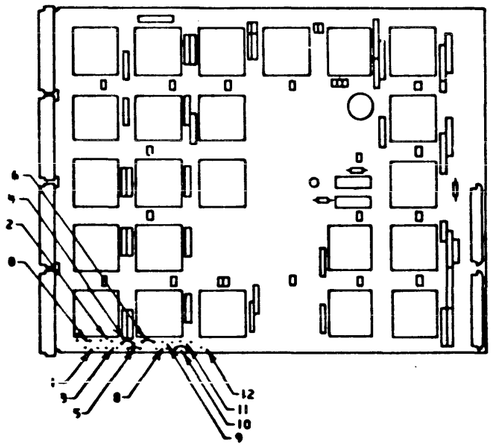


CHART A

DEVICES COUNT	1 DEVICE CONNECTOR	2 DEVICE CONNECTOR	3 DEVICE CONNECTOR	4 DEVICE CONNECTOR
JUMPER 11	X		X	
JUMPER 12	X	X		

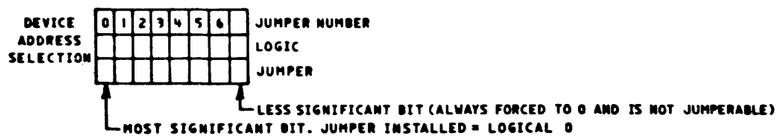
× MEANS JUMPER INSTALLED DEVICE I.D. WILL BE SET AUTOMATICALLY DEPENDING ON THE NUMBER OF FILES CONNECTED:
UP TO 2 FILES - DEVICE I.D. = 3106
3 OR 4 FILES - DEVICE I.D. = 3206

CHART B

IPL SELECTION	JUMPER 8	JUMPER 9	JUMPER 10
IPL NOT SUPPORTED			
FILE 0 PRIMARY			X
FILE 1 PRIMARY	X		X
FILE 0 SECONDARY	X	X	
FILE 1 SECONDARY		X	
FILE 0 PRIMARY AND FILE 1 SECONDARY		X	X
FILE 1 PRIMARY AND FILE 0 SECONDARY	X	X	X

× MEANS JUMPER INSTALLED

JUMPER P/N 4410751, QTY MAX 12



NOTES:

1. THE BASE ADDRESS IS ALWAYS DIVISIBLE BY 2. IF MORE THAN 2 FILES ARE CONNECTED THE BASE ADDRESS MUST BE DIVISIBLE BY 4
2.
3. CARD JUMPERS AS SHOWN
   BASE ADDRESS = F0 = 1111 0000
   IPL = FILE 0 PRIMARY
   DEVICE ID = 3206 = 0011 0010 0000 0110
   CONFIGURATION ENTRIES FOR OPTIONS AS SHOWN
   -F07A 0000 0000 0000 0000 0000 0000 3206
   -F17A 0000 0000 0000 0000 0000 0000 3206
   -F27A 0000 0000 0000 0000 0000 0000 3206
   -F37A 0000 0000 0000 0000 0000 0000 3206

EC HISTORY		DRAWING TITLE
31 AUG 78	374947	CARD JUMPERS
2 FEB 79	375351	MACH 4963 ATTACHMENT
		PART NO 6837770
		CLASSIFICATION

C

IBM CORP

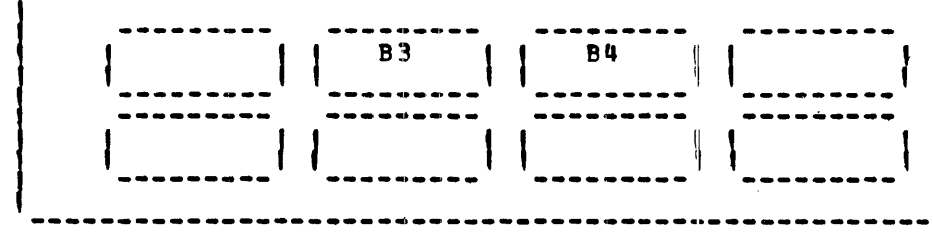
SF502

4963 DEDICATED CABLES (TO FILE 0 & FILE 1)

DUC BOARD (A2) PIN ASSIGNMENTS		FILE 0 BOARD (A1) PIN ASSIGNMENTS
B3B03--	-CNTRL SAMPLE FILE 0	-- A5B03
B3B04--	-DU INTRPT FILE 0	-- A5B04
B3B05--	-SECTOR 0	-- A5B05
B3B08--	+NRZ DATA 0	-- A5B08
B3B09--	-MISSING SECTOR 0	-- A5B09
B3B10--	-WRITE DATA 0	-- A5B10
B3B12--	+INTRFC DEGATE FILE 0	-- A5B12
B3D03--	+WRITE GATE RTN 0	-- A5D03
B3D04--	-DATA SELECT 0	-- A5D04
B3D05--	-FAST SYNC 0	-- A5D05
B3D06--	-RESET ERROR FILE 0	-- A5D06
B3D07--	-INDEX 0	-- A5D07
B3D09--	-READ 0	-- A5D09
B3D10--	+READ CLOCK 0	-- A5D10
B3D11--	-WRITE 0	-- A5D11
B3D12--	+WRITE CLOCK 0	-- A5D12
B3B02--	-CABLE CONTINUITY OUT	-- A5B02
B3D13--	-CABLE CONTINUITY IN	-- A5D13
B3B07--	GND	-- A5B07
B3B13--	GND	-- A5B13
B3D02--	GND	-- A5D02
B3D08--	GND	-- A5D08

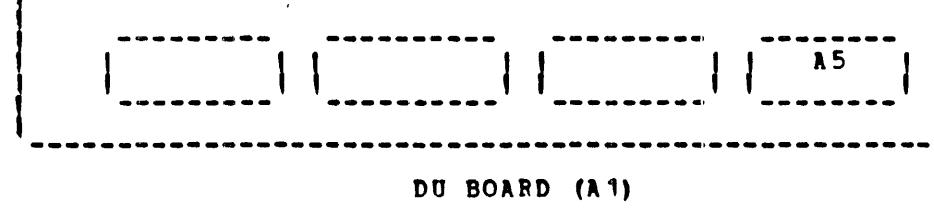
DUC BOARD (A2) PIN ASSIGNMENTS		FILE 1 BOARD (A1) PIN ASSIGNMENTS
B4B03--	-CNTRL SAMPLE FILE 1	-- A5B03
B4B04--	-DU INTRPT FILE 1	-- A5B04
B4B05--	-SECTOR 1	-- A5B05
B4B08--	+NRZ DATA 1	-- A5B08
B4B09--	-MISSING SECTOR 1	-- A5B09
B4B10--	-WRITE DATA 1	-- A5B10
B4B12--	+INTRFC DEGATE FILE 1	-- A5B12
B4D03--	+WRITE GATE RTN 1	-- A5D03
B4D04--	-DATA SELECT 1	-- A5D04
B4D05--	-FAST SYNC 1	-- A5D05
B4D06--	-RESET ERROR FILE 1	-- A5D06
B4D07--	-INDEX 1	-- A5D07
B4D09--	-READ 1	-- A5D09
B4D10--	+READ CLOCK 1	-- A5D10
B4D11--	-WRITE 1	-- A5D11
B4D12--	+WRITE CLOCK 1	-- A5D12
B4B02--	-CABLE CONTINUITY OUT	-- A5B02
B4D13--	-CABLE CONTINUITY IN	-- A5D13
B4B07--	GND	-- A5B07
B4B13--	GND	-- A5B13
B4D02--	GND	-- A5D02
B4D08--	GND	-- A5D08

B3 CONNECTS THRU CABLE TO A5 DU BOARD FILE 0
B4 CONNECTS THRU CABLE TO A5 DU BOARD FILE 1
(IF EXISTING)



DUC BOARD (A2)

A5B02 TIED TO A5D13 ON BOARD



DU BOARD (A1)

SEE 4963 THEORY DIAGRAMS MANUAL FOR DATA FLOW

4963 DEDICATED CABLES

E.C. HISTORY 08-17-78 374947

MACH. 4963

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DATE 02-01-79 LAST E.C. 375351 P.N. 6837771

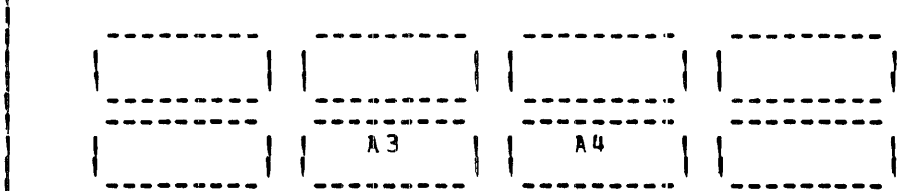
SF5033 000

4963 DEDICATED CABLES (TO FILE 2 & FILE 3)

DUC BOARD (A2) PIN ASSIGNMENTS		FILE 2 BOARD (A1) PIN ASSIGNMENTS
A4B03--	-CNTRL SAMPLE FILE 2	-- A5B03
A4B04--	-DU INTRPT FILE 2	-- A5B04
A4B05--	-SECTOR 2	-- A5B05
A4B08--	+NRZ DATA 2	-- A5B08
A4B09--	-MISSING SECTOR 2	-- A5B09
A4B10--	-WRITE DATA 2	-- A5B10
A4B12--	+INTRFC DEGATE FILE 2	-- A5B12
A4D03--	+WRITE GATE RTN 2	-- A5D03
A4D04--	-DATA SELECT 2	-- A5D04
A4D05--	-FAST SYNC 2	-- A5D05
A4D06--	-RESET ERROR FILE 2	-- A5D06
A4D07--	-INDEX 2	-- A5D07
A4D09--	-READ 2	-- A5D09
A4D10--	+READ CLOCK 2	-- A5D10
A4D11--	-WRITE 2	-- A5D11
A4D12--	+WRITE CLOCK 2	-- A5D12
A4B02--	-CABLE CONTINUITY IN	-- A5B02
A4D13--	-CABLE CONTINUITY OUT	-- A5D13
A4B07--	GND	-- A5B07
A4B13--	GND	-- A5B13
A4D02--	GND	-- A5D02
A4D08--	GND	-- A5D08

DUC BOARD (A2) PIN ASSIGNMENTS		FILE 3 BOARD (A1) PIN ASSIGNMENTS
A3B03--	-CNTRL SAMPLE FILE 3	-- A5B03
A3B04--	-DU INTRPT FILE 3	-- A5B04
A3B05--	-SECTOR 3	-- A5B05
A3B08--	+NRZ DATA 3	-- A5B08
A3B09--	-MISSING SECTOR 3	-- A5B09
A3B10--	-WRITE DATA 3	-- A5B10
A3B12--	+INTRFC DEGATE FILE 3	-- A5B12
A3D03--	+WRITE GATE RTN 3	-- A5D03
A3D04--	-DATA SELECT 3	-- A5D04
A3D05--	-FAST SYNC 3	-- A5D05
A3D06--	-RESET ERROR FILE 3	-- A5D06
A3D07--	-INDEX 3	-- A5D07
A3D09--	-READ 3	-- A5D09
A3D10--	+READ CLOCK 3	-- A5D10
A3D11--	-WRITE 3	-- A5D11
A3D12--	+WRITE CLOCK 3	-- A5D12
A3B02--	-CABLE CONTINUITY IN	-- A5B02
A3D13--	-CABLE CONTINUITY OUT	-- A5D13
A3B07--	GND	-- A5B07
A3B13--	GND	-- A5B13
A3D02--	GND	-- A5D02
A3D08--	GND	-- A5D08

A4 CONNECTS THRU CABLE TO A5 DU BOARD FILE 2 (IF EXISTING)
A3 CONNECTS THRU CABLE TO A5 DU BOARD FILE 3 (IF EXISTING)



DUC BOARD (A2)

A5B02 TIED TO A5D13 ON BOARD

DU BOARD (A1)

SFE 4963 THEORY DIAGRAMS MANUAL FOR DATA FLOW

4963 DEDICATED CABLES

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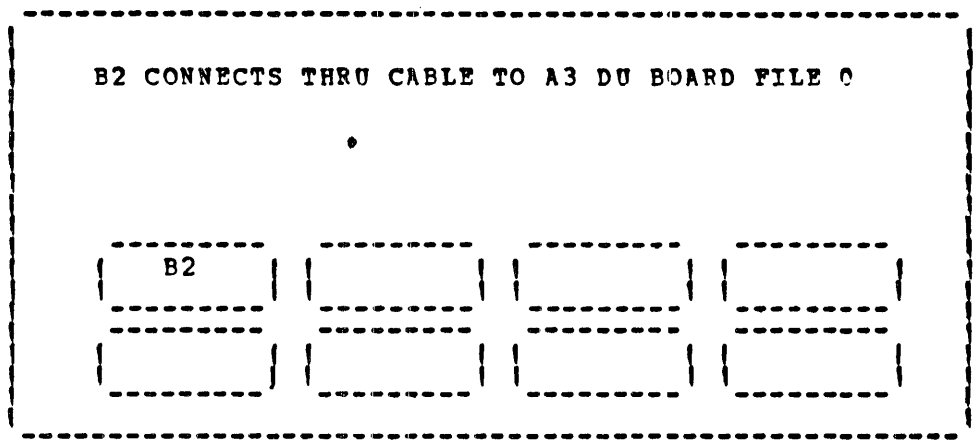
DATE 02-01-79 LAST E.C. 375351

P.N. 6837772

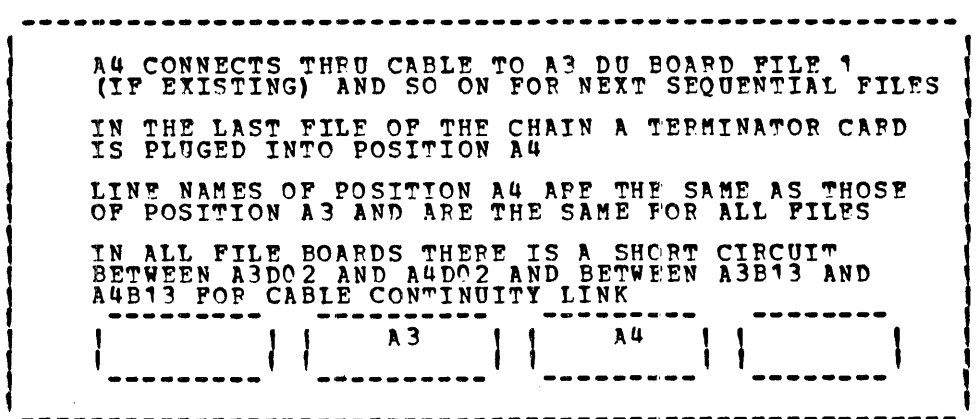
SF5040 000

4963 CHAIN CABLE

DUC BOARD (A2) PIN ASSIGNMENTS		FILE 0 BOARD (A1) PIN ASSIGNMENTS
B2B02--	-DU TAG BUS BIT 0	-- A3B02
B2B03--	-DU TAG BUS BIT 1	-- A3B03
B2B04--	-DU TAG BUS BIT 2	-- A3B04
B2B05--	-DU TAG BUS BIT P	-- A3B05
B2B06--	NOT USED	-- A3B06
B2B07--	+5 VOLTS FOR TERM CD	-- A3B07
B2B08--	+5 VOLTS FOR TERM CD	-- A3B08
B2B09--	+5 VOLTS FOR TERM CD	-- A3B09
B2B10--	NOT USED	-- A3B10
B2B11--	NOT USED	-- A3B11
B2B12--	-CONTROL SAMPLE RCVD	-- A3B12
B2B13--	-CABLE CONTINUITY IN	-- A3B13
B2D02--	-CABLE CONTINUITY OUT	-- A3D02
B2D03--	NOT USED	-- A3D03
B2D04--	-MC DATA BUS BIT 0	-- A3D04
B2D05--	-MC DATA BUS BIT 1	-- A3D05
B2D06--	-MC DATA BUS BIT 2	-- A3D06
B2D07--	-MC DATA BUS BIT 3	-- A3D07
B2D08--	GND	-- A3D08
B2D09--	-MC DATA BUS BIT 4	-- A3D09
B2D10--	-MC DATA BUS BIT 5	-- A3D10
B2D11--	-MC DATA BUS BIT 6	-- A3D11
B2D12--	-MC DATA BUS BIT 7	-- A3D12
B2D13--	-MC DATA BUS BIT P	-- A3D13



DUC BOARD (A2)



DU BOARD A1 (FILE 0)

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4963 CHAIN CABLE

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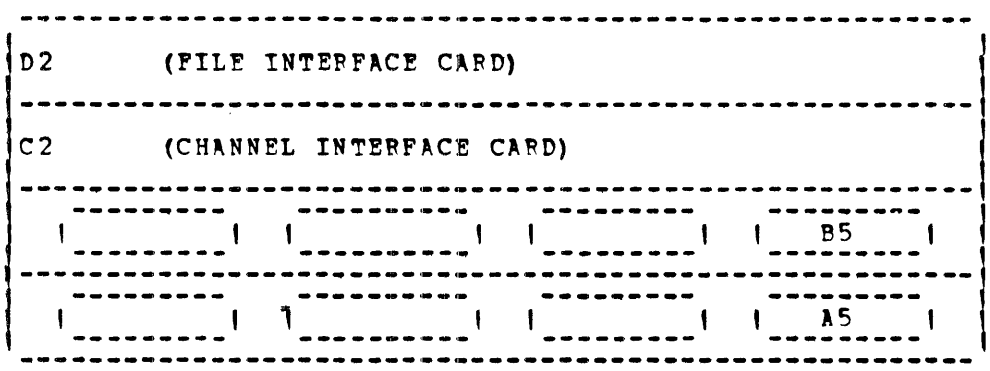
DATE 02-01-79 LAST E.C. 375351

P.N. 6837773

000

4963 DUC BOARD (A2) CABLE POSITIONS A5, B5 TO CARD A2C2

DUC BOARD (A2) CABLE POSITIONS A5, B5 PIN ASSIGNMENTS	DUC CARD A2C2 PIN ASSIGNMENTS
B5B02-- -FILE DATA BUS BIT 00	-- C2M08-
B5B03-- -FILE DATA BUS BIT 01	-- C2M09-
B5B04-- -FILE DATA BUS BIT 02	-- C2M10-
B5B05-- -FILE DATA BUS BIT 03	-- C2M11-
B5B06-- -FILE DATA BUS BIT 04	-- C2M12-
B5B08-- -FILE DATA BUS BIT 05	-- C2M13-
B5B09-- -FILE DATA BUS BIT 06	-- C2S02-
B5B10-- -FILE DATA BUS BIT 07	-- C2S03-
B5B11-- -FILE DATA BUS BIT P0	-- C2S12-
B5D03-- -FILE DATA BUS BIT 08	-- C2S04-
B5D04-- -FILE DATA BUS BIT 09	-- C2S05-
B5D05-- -FILE DATA BUS BIT 10	-- C2S06-
B5D06-- -FILE DATA BUS BIT 11	-- C2S07-
B5D07-- -FILE DATA BUS BIT 12	-- C2S08-
B5D09-- -FILE DATA BUS BIT 13	-- C2S09-
B5D10-- -FILE DATA BUS BIT 14	-- C2S10-
B5D11-- -FILE DATA BUS BIT 15	-- C2S11-
B5D12-- -FILE DATA BUS BIT P1	-- C2S13-
A5B11-- -INTRFC PARITY CHECK	-- C2P11-
A5D03-- -FILE TAG 0	-- C2U04-
A5D04-- -FILE TAG 1	-- C2U05-
A5D05-- -FILE TAG 2	-- C2U06-
A5D06-- -FILE TAG 3	-- C2U07-
A5D12-- -FILE TAG P	-- C2U13-
A5B05-- -AKN REQ OUT	-- C2J06-
A5B08-- -STROBE IN	-- C2J10-
A5B09-- -REQUEST IN	-- C2J11-
A5D13-- -PARAKEET POR	-- C2M02-
A5B03-- -SYSTEM RESET	-- C2M03-
A5B04-- -REQUEST OUT	-- C2J13-
A5B06-- -STROBE OUT	-- C2J12-
A5B10-- -AKN REQ IN POWERED	-- C2J05-
A5B12-- -SYSTEM PWR ON RST	-- C2M06,C2D13-
A5D07-- -FILE TAG 4	-- C2U09-
A5D09-- -FILE TAG 5	-- C2U10-
A5D10-- -FILE TAG 6	-- C2U11-
A5D11-- -FILE TAG 7	-- C2U12-
B5D02-- GND	
B5D08-- GND	
B5B07-- GND	
B5B13-- GND	
A5D02-- GND	
B5D13-- -IPL (NOT USED)	-- C2D12-
A5B02-- BURST MODE (NOT USED)	-- C2U02-



DUC (A2) BOARD (CARD SIDE VIEW)

SEE 4963 THEORY DIAGRAMS MANUAL FOR DATA FLOW

4963 DUC BOARD PINS

E.C. HISTORY 08-17-78 374947

MACH. 4963

S F 5 0 6

IBM CORP. GSD

DATE 02-01-79 LAST E.C. 375351

P.N. 6837774

0 0 0

4963 DUC BOARD (A2) CABLE POSITIONS B2,B3,B4,A3,A4 TO CARD C2

DUC BOARD (A2) CABLE POSITIONS B2,B3,B4,A3,A4 PIN ASSIGNMENTS		DUC CARD A2C2 PIN ASSIGNMENTS
B2B02--	-DU TAG BUS BIT 0	-- C2B10-
B2B03--	-DU TAG BUS BIT 1	-- C2B09-
B2B04--	-DU TAG BUS BIT 2	-- C2B12-
B2B05--	-DU TAG BUS BIT P	-- C2B13-
B2B12--	-CNTRL SAMPLE RCVD	-- C2P04-
B2D04--	-MC DATA BUS BIT 0	-- C2J07-
B2D05--	-MC DATA BUS BIT 1	-- C2G07-
B2D06--	-MC DATA BUS BIT 2	-- C2G08-
B2D07--	-MC DATA BUS BIT 3	-- C2G09-
B2D09--	-MC DATA BUS BIT 4	-- C2G10-
B2D10--	-MC DATA BUS BIT 5	-- C2J09-
B2D11--	-MC DATA BUS BIT 6	-- C2G12-
B2D12--	-MC DATA BUS BIT 7	-- C2G13-
B2D13--	-MC DATA BUS BIT P	-- C2G05-
B3B03--	-CNTRL SAMPLE FILE 0	-- C2J02-
B3B04--	-DU INTRPT FILE 0	-- C2P02-
B3B12--	+INTRFC DEGATE FILE 0	-- C2G03-
B3D06--	-RESET ERROR FILE 0	-- C2P12-
B4B03--	-CNTRL SAMPLE FILE 1	-- C2G02-
B4B04--	-DU INTRPT FILE 1	-- C2D11-
B4B12--	+INTRFC DEGATE FILE 1	-- C2B07-
B4D06--	-RESET ERROR FILE 1	-- C2P13-
A4B03--	-CNTRL SAMPLE FILE 2	-- C2J04-
A4B04--	-DU INTRPT FILE 2	-- C2P05-
A4B12--	+INTRFC DEGATE FILE 2	-- C2P07-
A4D06--	-RESET ERROR FILE 2	-- C2M05-
A3B03--	-CNTRL SAMPLE FILE 3	-- C2G04-
A3B04--	-DU INTRPT FILE 3	-- C2P06-
A3B12--	+INTRFC DEGATE FILE 3	-- C2P09-
A3D06--	-RESET ERROR FILE 3	-- C2M04-
D4B07--	+PLA CLOCK	-- C2B08-

GROUND FOR CARD ON BOARD
C2B08

CABLE CONTINUITY LINK DUC BOARD (A2) PIN ASSIGNMENTS		DUC BOARD (A2) PIN ASSIGNMENTS
B2D02--	GND	
B2B13--	CHAIN CABLE CONT.	-- B3B02-
B3B02--	DEDIC. CABLE FILE 0 CONT.	
B3D13--	DEDIC. CABLE FILE 0 CONT.	-- B4B02,A2D02-
B4B02--	DEDIC. CABLE FILE 1 CONT.	
B4D13--	DEDIC. CABLE FILE 1 CONT.	-- A4D13,A2D03-
A4D13--	DEDIC. CABLE FILE 2 CONT.	
A4B02--	DEDIC. CABLE FILE 2 CONT.	-- A3D13,A2D04-
A3D13--	DEDIC. CABLE FILE 3 CONT.	
A3B02--	DEDIC. CABLE FILE 3 CONT.	-- C2M07,A2B02,A2B03, A2B04-

DUC BOARD (A2) CABLE CONTINUITY JUMPERS

DEPENDING ON THE NUMBER OF FILES CONNECTED A JUMPER MUST BE INSTALLED ON THE DUC BOARD (A2) PER THE FOLLOWING TABLE

	A2B02-A2D02	A2B03-A2D03	A2B04-A2D04
1 FILE CONNECTED	YES	NO	NO
2 FILES CONNECTED	NO	YES	NO
3 FILES CONNECTED	NO	NO	YES
4 FILES CONNECTED	NO	NO	NO

D2 (FILE INTERFACE CARD)

C2 (CHANNEL INTERFACE CARD)

B2	B3	B4	
A2	A3	A4	

DUC BOARD A1 (CARD SIDE VIEW)

SEE 4963 THEORY DIAGRAMS MANUAL FOR DATA FLOW

4963 DUC BOARD PINS

E.C. HISTORY 08-17-78 374947

MACH. 4963

IBM CORP. GSD

DATE 02-01-79 LAST E.C. 375351

P.N. 6837775

SY5C7

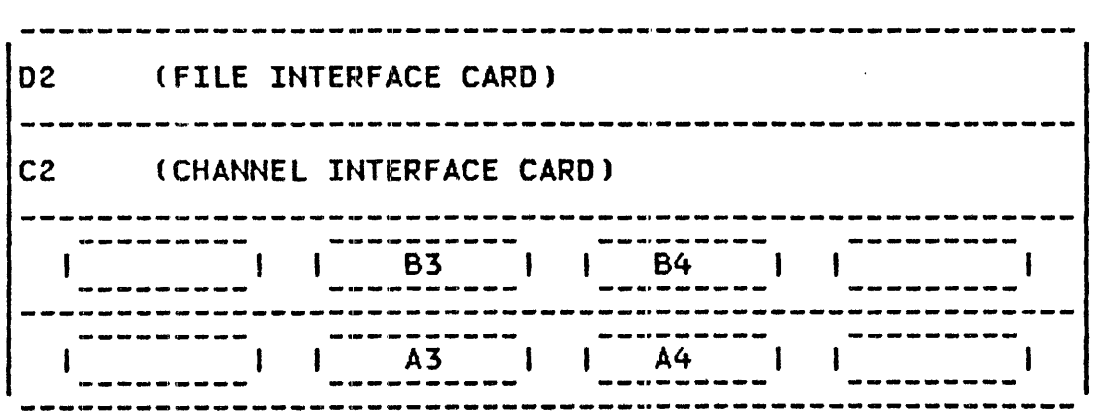
0 0 0

4963 DUC BOARD (A2) CABLE POSITIONS B3,B4,A3,A4,TO CARD D2

DUC BOARD (A2) CABLE POSITIONS B3,B4,A3,A4 PIN ASSIGNMENTS	DUC CARD A2D2 PIN ASSIGNMENTS
B3B05-- -SECTOR 0	-- D2J07-
B3B08-- +NRZ DATA 0	-- D2P05-
B3B09-- -MISSING SECTOR 0	-- D2D12-
B3B10-- -WRITE DATA 0	-- D2P02-
B3D03-- +WRITE GATE RTN 0	-- D2J02-
B3D04-- -DATA SELECT 0	-- D2D07-
B3D05-- -FAST SYNC 0	-- D2D05-
B3D07-- -INDEX 0	-- D2J05-
B3D09-- -READ 0	-- D2D02-
B3D10-- +READ CLOCK 0	-- D2J12-
B3D11-- -WRITE 0	-- D2D10-
B3D12-- +WRITE CLOCK 0	-- D2J10-
B4B05-- -SECTOR 1	-- D2J09-
B4B08-- +NRZ DATA 1	-- D2P06-
B4B09-- -MISSING SECTOR 1	-- D2D13-
B4B10-- -WRITE DATA 1	-- D2S02-
B4D03-- +WRITE GATE RTN 1	-- D2J04-
B4D04-- -DATA SELECT 1	-- D2D09-
B4D05-- -FAST SYNC 1	-- D2D06-
B4D07-- -INDEX 1	-- D2J06-
B4D09-- -READ 1	-- D2D04-
B4D10-- +READ CLOCK 1	-- D2J13-
B4D11-- -WRITE 1	-- D2D11-
B4D12-- +WRITE CLOCK 1	-- D2J11-
A4B05-- -SECTOR 2	-- D2G07-
A4B08-- +NRZ DATA 2	-- D2M04-
A4B09-- -MISSING SECTOR 2	-- D2B12-
A4B10-- -WRITE DATA 2	-- D2M02-
A4D03-- +WRITE GATE RTN 2	-- D2G02-
A4D04-- -DATA SELECT 2	-- D2B07-
A4D05-- -FAST SYNC 2	-- D2B04-
A4D07-- -INDEX 2	-- D2G04-
A4D09-- -READ 2	-- D2B02-
A4D10-- +READ CLOCK 2	-- D2G12-
A4D11-- -WRITE 2	-- D2B09-
A4D12-- +WRITE CLOCK 2	-- D2G09-
A3B05-- -SECTOR 3	-- D2G08-
A3B08-- +NRZ DATA 3	-- D2M05-
A3B09-- -MISSING SECTOR 3	-- D2B13-
A3D10-- -WRITE DATA 3	-- D2M03-
A3D03-- +WRITE GATE RTN 3	-- D2G03-
A3D04-- -DATA SELECT 3	-- D2B08-
A3D05-- -FAST SYNC 3	-- D2B05-
A3D07-- -INDEX 3	-- D2G05-
A3D09-- -READ 3	-- D2S12-
A3D10-- +READ CLOCK 3	-- D2G13-
A3D11-- -WRITE 3	-- D2B10-
A3D12-- +WRITE CLOCK 3	-- D2G10-
A5D13-- -PARAKEET POR	-- D2S03,S13

CARD PINS TIED TOGETHER ON BOARD FOR TEST POINTS	
D2S09-- +CLOCK 2 TP	-- D2S11---
D2S05-- +T6 CLOCK TP	-- D2S05,S06,S07-
D2M08-- +WRITE SELECT TP	-- D2S08---
D2S10-- +BIT RING 8 TP	-- D2U10---

PINS ON CARD TIED TO GROUND AT BOARD
D2M11,M12,P04,P10,P11,P12,U04,U05



DUC BOARD A2 (CARD SIDE VIEW)

SEE 4963 THEORY DIAGRAMS MANUAL FOR DATA FLOW

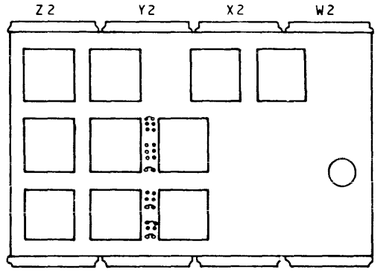
4963 DUC BOARD PINS

E.C.	HISTORY	MACH.
17AUG78	374947	
01FEB79	375351	4963

IBM CORP. GSD

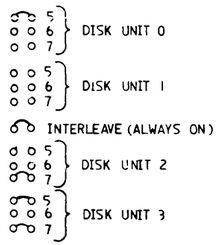
DATE	LAST E.C.	P.N.
10AUG81	323396	6837776

SF5508 0 0 0



A2C2 CARD IN DISK UNIT CONTROL BOARD

JUMPER NUMBERING



IN THE ABOVE EXAMPLE

DISK UNIT 0 IS A MODEL 64A
DISK UNIT 1 IS A MODEL 59B
DISK UNIT 2 IS A MODEL 23B
DISK UNIT 3 IS A MODEL 29B

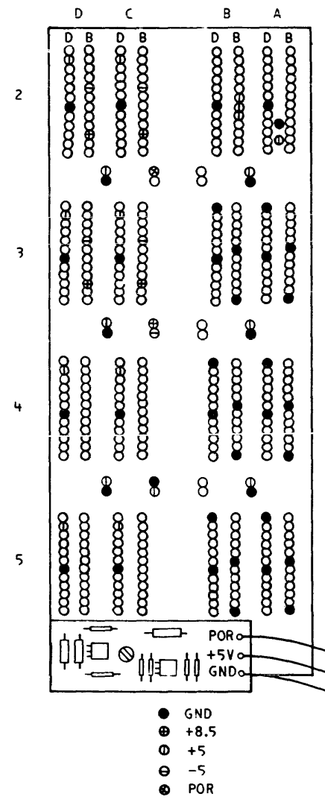
EXAMPLE OF PINS JUMPERED FOR DISK NOT INSTALLED

MODEL DESIGNATION

JUMPER NUMBER	5	6	7
DISK UNIT NOT INSTALLED		X	X
MODELS 23A OR 23B			X
MODELS 29A OR 29B	X		X
MODELS 58A OR 58B			
MODELS 64A OR 64B	X		

AN 'X' IN THE TABLE SIGNIFIES THAT A JUMPER IS INSTALLED. JUMPER P/N 1675209

DISK UNIT CONTROL BOARD
PIN PATTERN (PIN SIDE VIEW)



- GND
- +8.5
- +5
- −5
- POR

CARDS
- CHANNEL CARD
  PLUGS IN C2
- FILE CARD
  PLUGS IN D2

OF FILES ATTACHED
- 1 FILE JUMPER
  A2B02 TO A2D02
- 2 FILES JUMPER
  A2B03 TO A2D03
- 3 FILES JUMPER
  A2B04 TO A2D04
- 4 FILES NO JUMPERS

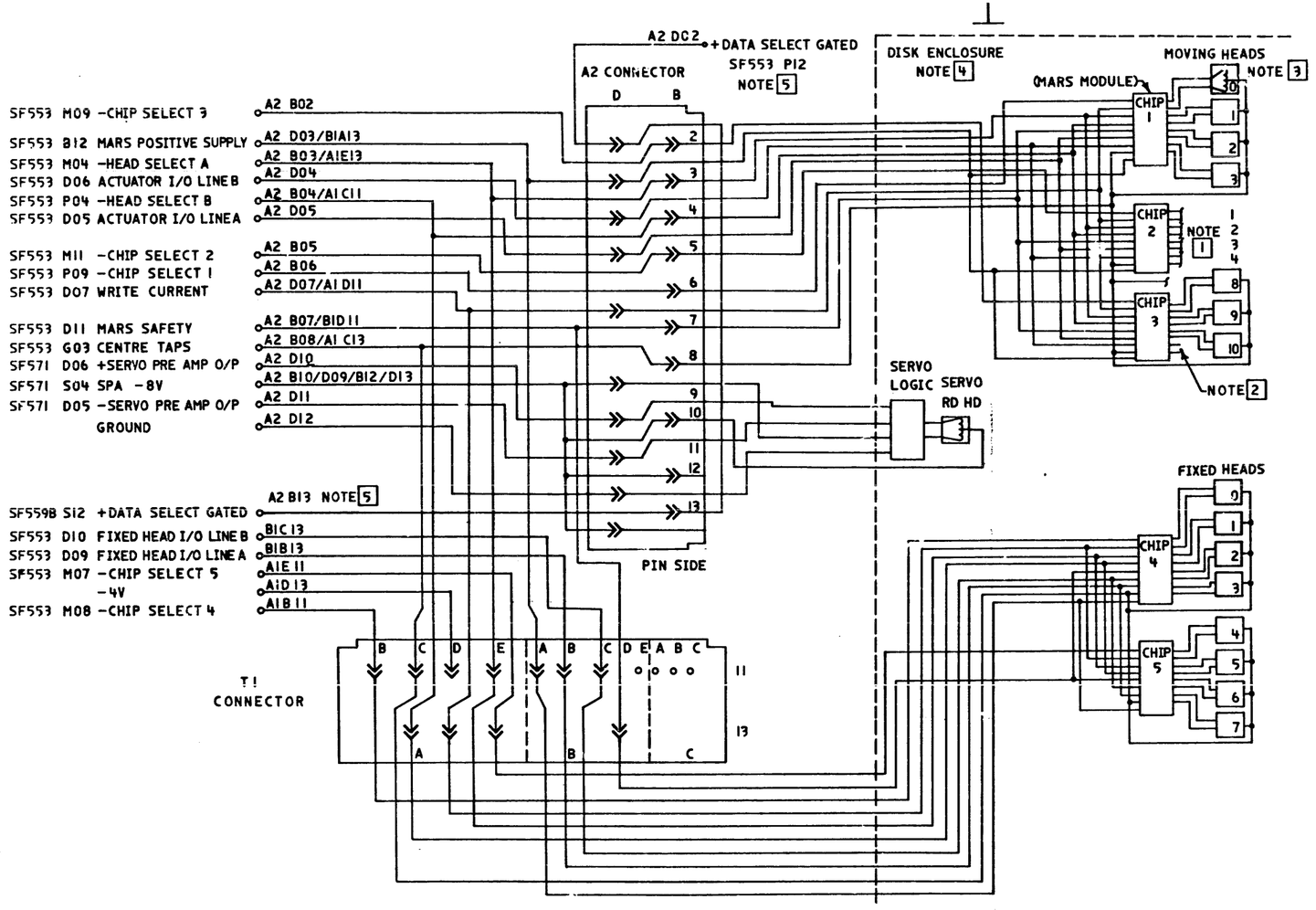
- ATTACHMENT CABLES
  W2 PLUGS TO B5
  X2 PLUGS TO A5
- CHAIN CABLE
  A3 OF FILE 0 TO B2
- DEDICATED CABLES
  A5 OF FILE 0 TO B3
  A5 OF FILE 1 TO B4
  A5 OF FILE 2 TO A4
  A5 OF FILE 3 TO A3
- DECOUPLING CAP
  PLUG IN A2

EC HISTORY		DRAWING TITLE
20 FEB 79	375351	DUC JUMPERING
11 MAR 80	375662	MACH 4963
10 AUG 81	323396	PART NO 6839630
		CLASSIFICATION
C		IBM CORP

SF509

SF509

SF509



NOTES:

1. CHIP 2 IS WIRED IN A SIMILAR MANNER TO CHIP 1
2. HEAD 11 IS NOT FITTED. IF AN UNSAFE CONDITION IS DETECTED LOGIC CIRCUITS FORCE SELECTION OF HEAD 11 TO AVOID OVERWRITING DATA TRACKS
3. HEAD 0 NOT FITTED IF FIXED HEADS ARE INCLUDED IN DE.
4. COMPONENTS WITHIN THE DE ARE SEALED AND CANNOT BE SERVICED IN THE FIELD
5. DATA SELECT GATED IS LOOPED THROUGH THE A2 CONNECTOR TO TEST IF CONNECTOR IS CORRECTLY INSTALLED.

HEAD SELECTION DECODE (DOWN LEVEL = 1)

SYSTEM HEAD SELECT CODE	HEAD SELECTED	OUTPUT LINES SELECTED						
		CHIP SELECTS					HEAD SELECTS	
		1	2	3	4	5	A	B
00000	0	1	0	0	0	0	0	0
00001	1	1	0	0	0	0	1	0
00010	2	1	0	0	0	0	0	1
00011	3	1	0	0	0	0	1	1
00100	4	0	1	0	0	0	0	0
00101	5	0	1	0	0	0	1	0
00110	6	0	1	0	0	0	0	1
00111	7	0	1	0	0	0	1	1
01000	8	0	0	1	0	0	0	0
01001	9	0	0	1	0	0	1	0
01010	10 NOTE 3	0	0	1	0	0	0	1
01011	11 NOTE 2	0	0	1	0	0	1	1
01100	INVALID CODES	0	0	0	0	0	0	0
01101		0	0	0	0	0	1	0
01110		0	0	0	0	0	0	1
01111		0	0	0	0	0	1	1
10000	FH0	0	0	0	1	0	0	0
10001	FH1	0	0	0	1	0	1	0
10010	FH2	0	0	0	1	0	0	1
10011	FH3	0	0	0	1	0	1	1
10100	FH4	0	0	0	0	1	0	0
10101	FH5	0	0	0	0	1	1	0
10110	FH6	0	0	0	0	1	0	1
10111	FH7	0	0	0	0	1	1	1
11000	INVALID CODES	0	0	0	0	0	0	0
11001		0	0	0	0	0	1	0
11010		0	0	0	0	0	0	1
11011		0	0	0	0	0	1	1
11100		0	0	0	0	0	0	0
11101		0	0	0	0	0	1	0
11110		0	0	0	0	0	0	1
11111		0	0	0	0	0	1	1

SF527

EC HISTORY		DRAWING TITLE
20FEB79	375351	HEAD SELECTION DU CABLE
11MAR80	375662	MACH 4963
		PART NO 6839719
		CLASSIFICATION

D

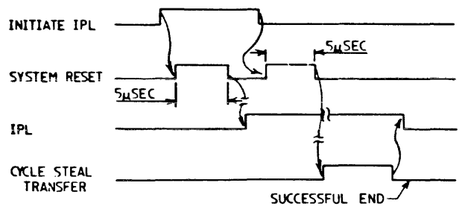
IBM CORP

SF527

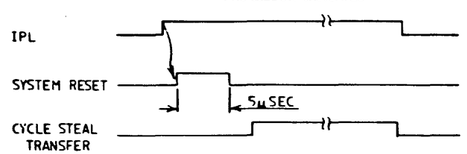
SF530

THE FOLLOWING SEQUENCE CHARTS ARE FOR REFERENCE ONLY AND TIMINGS ARE APPROXIMATE

INITIAL PROGRAM LOAD



PROCESSOR INITIATED



ADDRESS BUS (17)
BIT 16 OFF INDICATES CYCLE STEAL TO OR FROM STORAGE TO THE I/O DEVICE

DATA BUS
DATA BUS CONTAINS THE DEVICE CONTROL BLOCK (DCB) ADDRESS DURING A START COMMAND

ADDRESS GATE

ADDRESS GATE RETURN

CONDITION CODE IN
SIGNALS THE KEY DURING CYCLE ST TRANSFER

DATA STROBE
USED BY DEVICE TO REGISTER THE DATA ON OUTBOUND TRANSFER

CYCLE STEAL REQUEST
USED BY I/O DEVICE TO REQUEST AN INTERVAL OR ACCESS TO STORAGE RESOURCES

POLL IDENTIFIER
IDENTIFY NATURE OF POLL

POLL
IS CAPTURED BY FIRST DEVICE TO SEE IT WITH REQUEST IN RAISED

POLL RETURN
SENT BY I/O DEVICE TO SIGNAL A POLL CAPTURE HAS BEEN TAKEN

SERVICE GATE
INDICATES BEGIN TRANSFER TO THE DEVICE

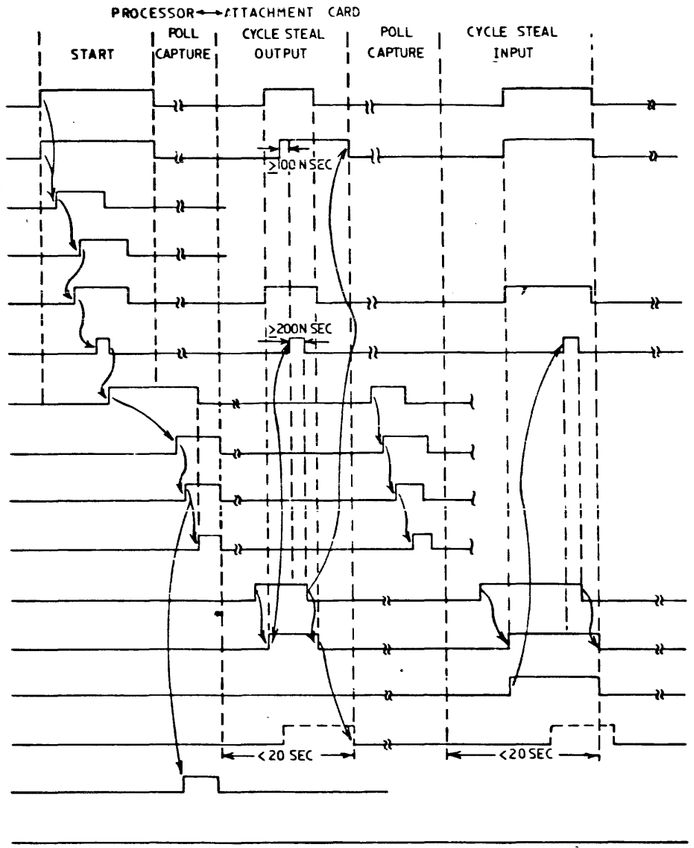
SERVICE GATE RETURN
SIGNALS RECOGNITION OF SERVICE GATE

OUTPUT/INPUT INDICATOR
OFF OUTPUT FROM STORAGE
ON INPUT TO STORAGE

C.S. STATUS BUS
SIGNALS THE DEVICE OF ANY ERRORS THE CHANNEL HAS DETECTED

POLL PROPAGATE
IF REQUEST IS NOT ON

REQUEST IN BUS
ONE OF 16 LINES ON FOR INTERRUPT REQUEST



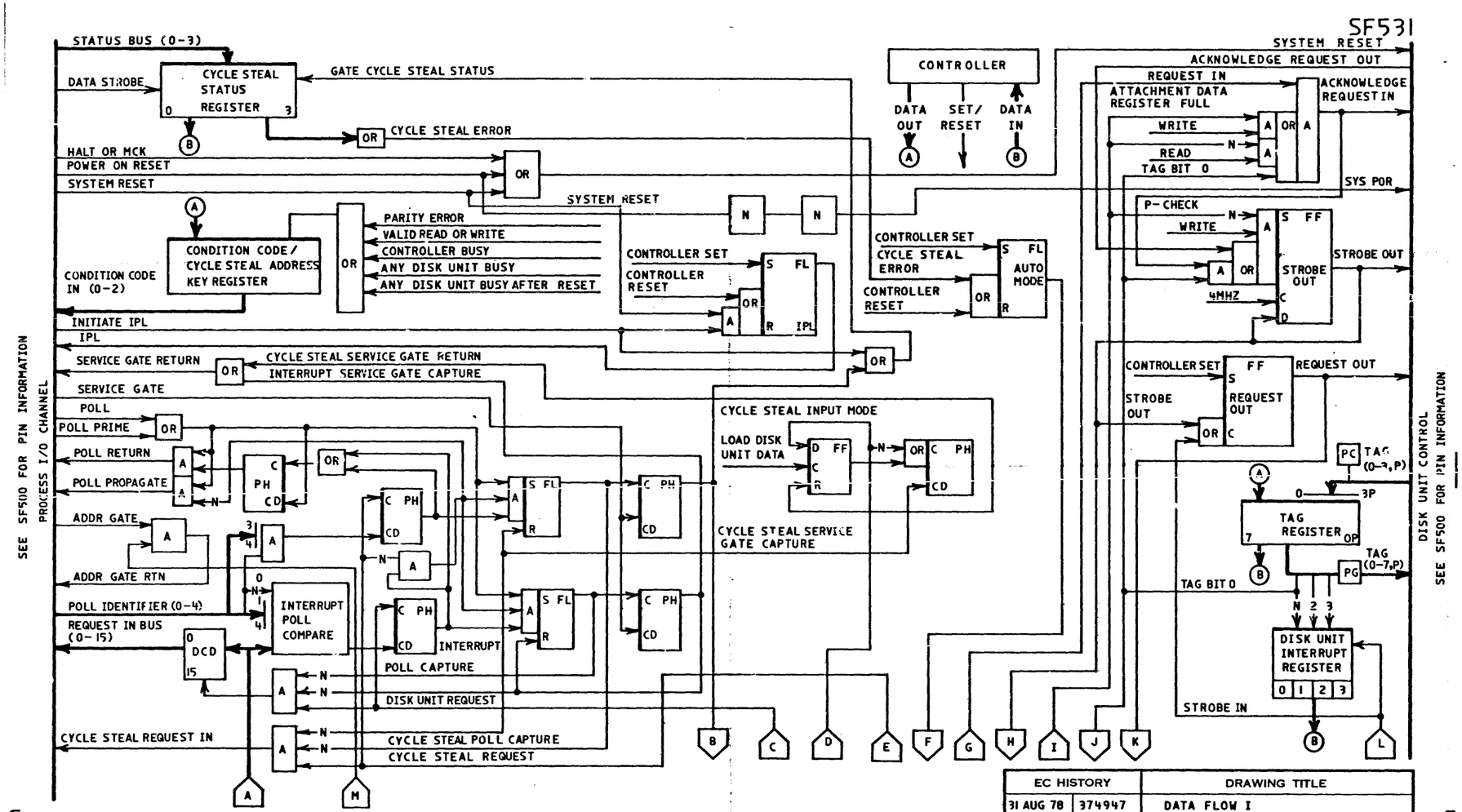
EC HISTORY		DRAWING TITLE
20FEB79	375351	DPC AND CYCLE STEAL SEQ
		MACH 4963
		PART NO 6839631
C		CLASSIFICATION

IBM CORP

SF530

SF530

SF531

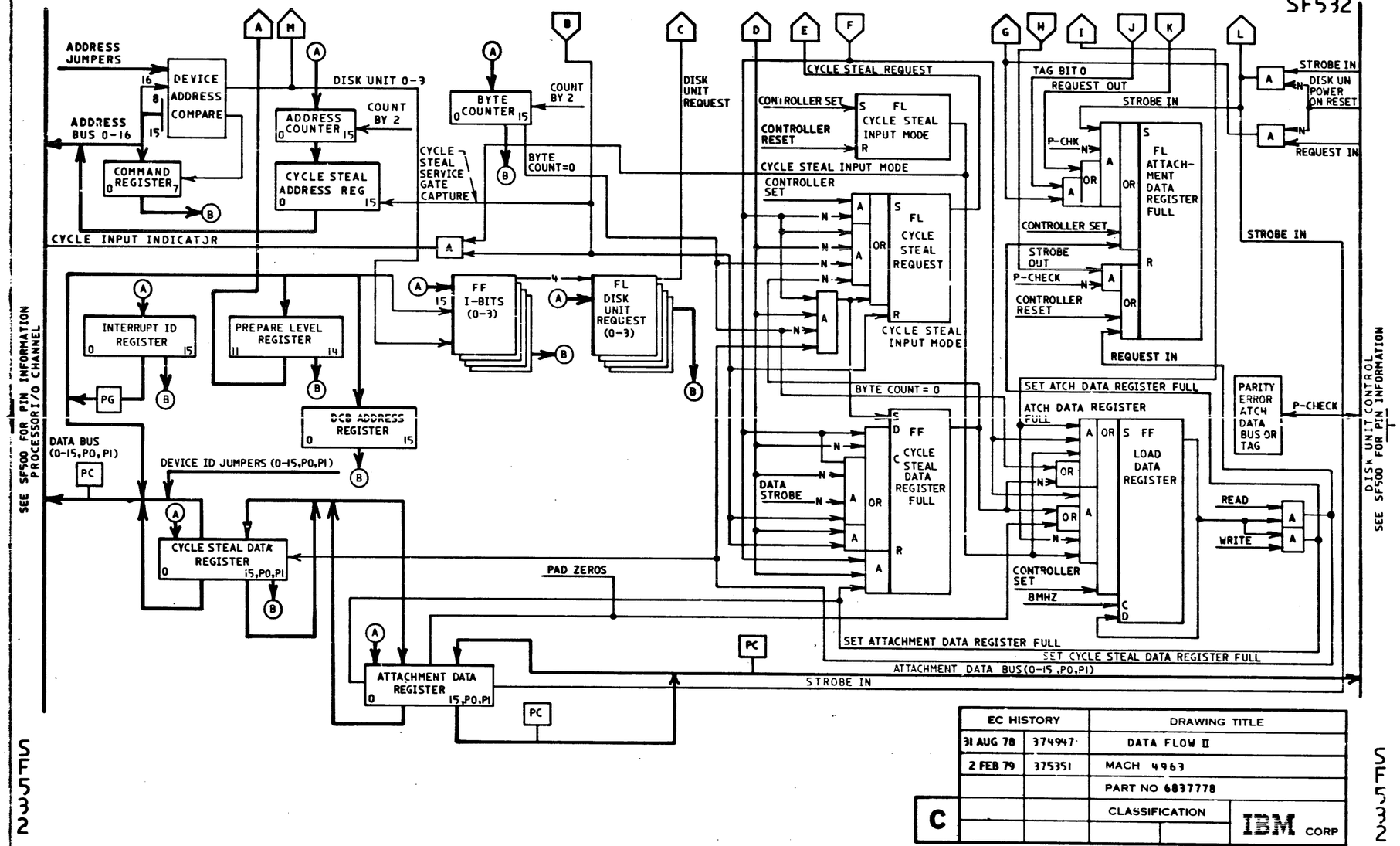


EC HISTORY		DRAWING TITLE
31 AUG 78	374947	DATA FLOW I
2 FEB 79	375351	MACH 4963
11 MAR 80	375662	PART NO 6837777
C		CLASSIFICATION

IBM COPP

SF531

SF532

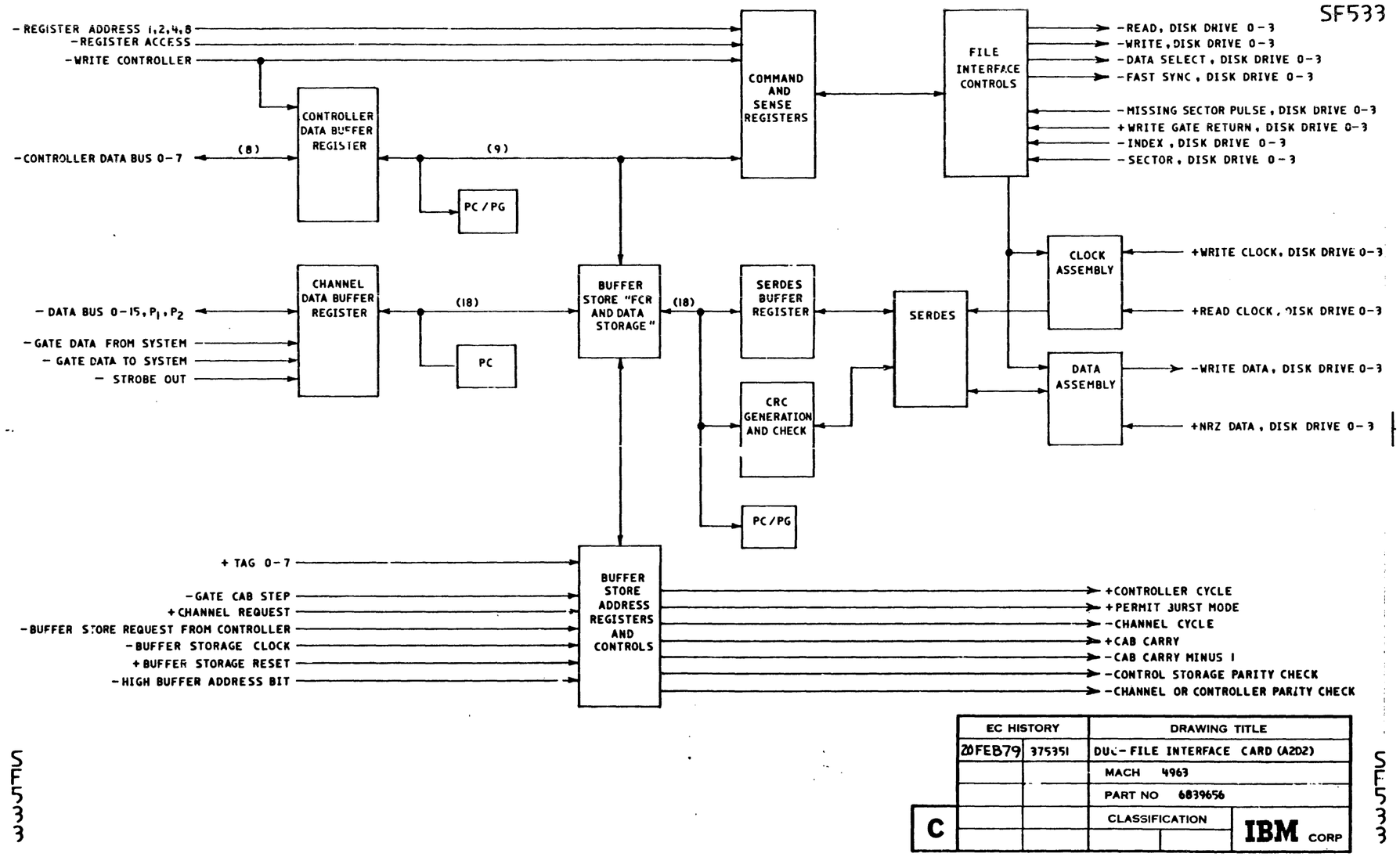


EC HISTORY		DRAWING TITLE
31 AUG 78	374947	DATA FLOW II
2 FEB 79	375351	MACH 4963
		PART NO 6837778
		CLASSIFICATION

C

IBM CORP

SF533



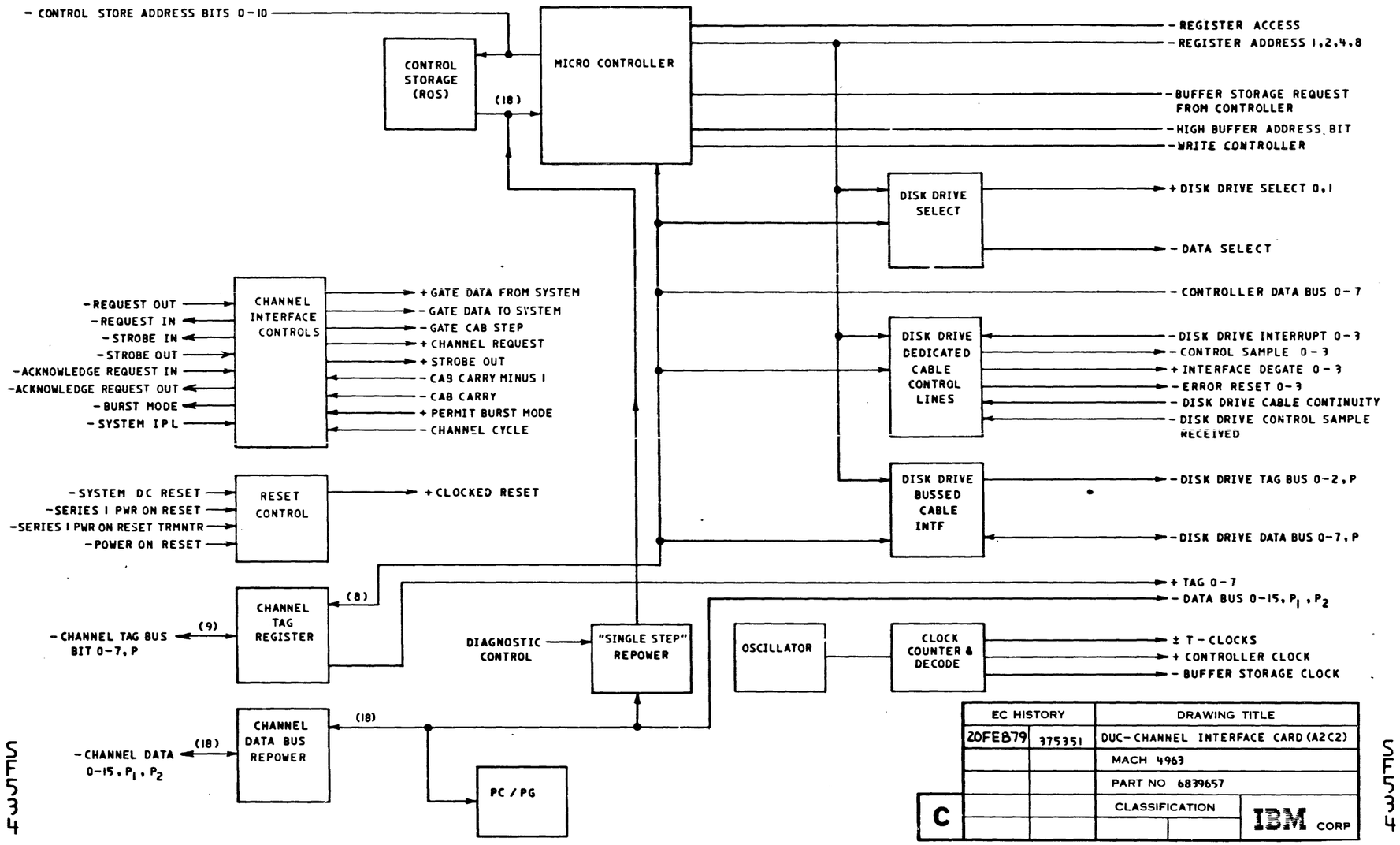
EC HISTORY		DRAWING TITLE
20FEB79	375351	DUC-FILE INTERFACE CARD (A2D2)
		MACH 4963
		PART NO 6839656
C		CLASSIFICATION

IBM CORP

SF533

SF533

SF534



EC HISTORY		DRAWING TITLE
20FEB79	375351	DUC-CHANNEL INTERFACE CARD (A2C2)
		MACH 4963
		PART NO 6839657
		CLASSIFICATION

C

IBM CORP

SF534

SF534

SF535

LINE NAME	PIN
+ TAG 0	A2-D2 X24
1	X25
2	X26
3	X28
4	X29
5	X30
6	X32
7	X33
- CONTROLLER DATA BUS BIT 0	Y23
1	Y24
2	Y25
3	Y26
4	Y28
5	Y29
6	Y30
7	Y32
- DATA BUS BIT 0	Z05
1	Z06
2	Z07
3	Z09
4	Z10
5	Z11
6	Z12
7	Z13
8	Z22
9	Z23
10	Z24
11	Z25
12	Z26
13	Z28
14	Z29
15	Z30
P1 (0-7)	Z02
P2 (8-15)	Z03
+ DISK DRIVE SELECT BIT 0	W06
1	W07
- DATA SELECT	W09
- REGISTER ADDRESS 1	X05
2	X06
4	X22
8	X23
- REGISTER ACCESS	X11
- WRITE CONTROLLER	Y22

LINE NAME	PIN
+ GATE DATA FROM SYSTEM	A2-D2 Y05
- GATE DATA TO SYSTEM	Y07
+ STROBE OUT	Y09
- GATE CAB STEP	W29
+ CHANNEL REQUEST	X03
- BUFFER STORE REQUEST FROM CONTROLLER	X13
- BUFFER STORAGE CLOCK	Y33
+ BUFFER STORAGE RESET	Y06
+ PERMIT BURST MODE	W13
- CHANNEL CYCLE	W10
+ CAB CARRY	X09
- CAB CARRY MINUS 1	X10
+ CONTROLLER CYCLE	W11
+ T0	W12
+ T0	Y13
+ T1	X02
+ T2	W33
+ T4	W32
- T5	W28
+ T7	Y11
+ T9	W30
+ OSCILLATOR INPUT	W03
+ OSCILLATOR OUTPUT	W23
- CONTROLLER WRAP	W05
- CONTROLLER WRAP	W22
+ EXTERNAL RESET	W26
- CONTROL STORAGE PARITY CHECK	W02
- HIGH BUFFER ADDRESS BIT	X12
- CHANNEL OR CONTROLLER PARITY CHECK	Y03
+ DIAGNOSTIC DATA	Z32
+ DIAGNOSTIC LATCH 1	Y12
2	Z33
3	Y02
+ SCAN DATA	X07
- LEFTMOST BYTE	Y10

EC HISTORY		DRAWING TITLE
20FEB79	375351	CAP - CHANNEL FILE INTF TOP CARD
		MACH 4963 CONNECTORS
		PART NO 6839658
		CLASSIFICATION

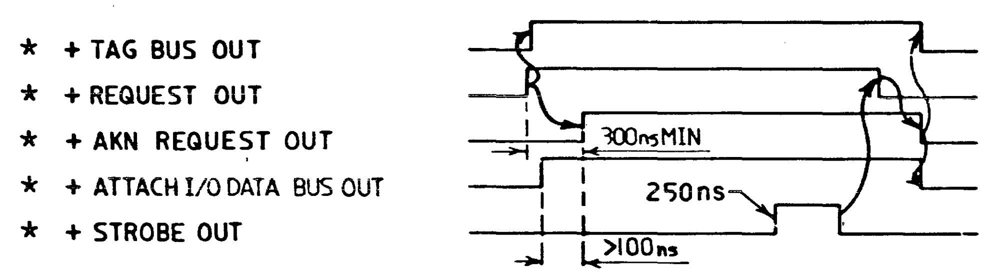
C

IBM CORP

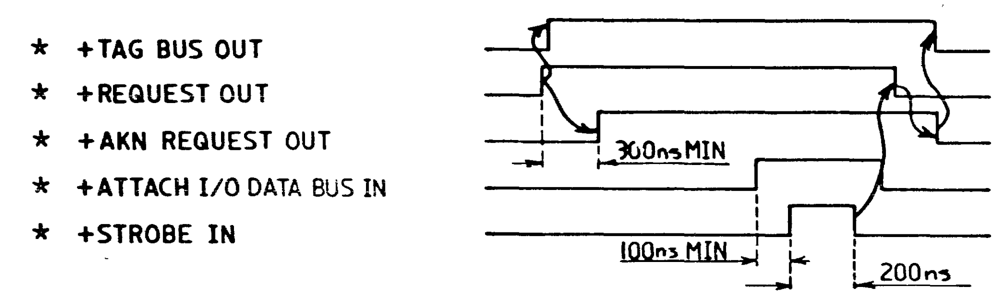
SF535

SF535

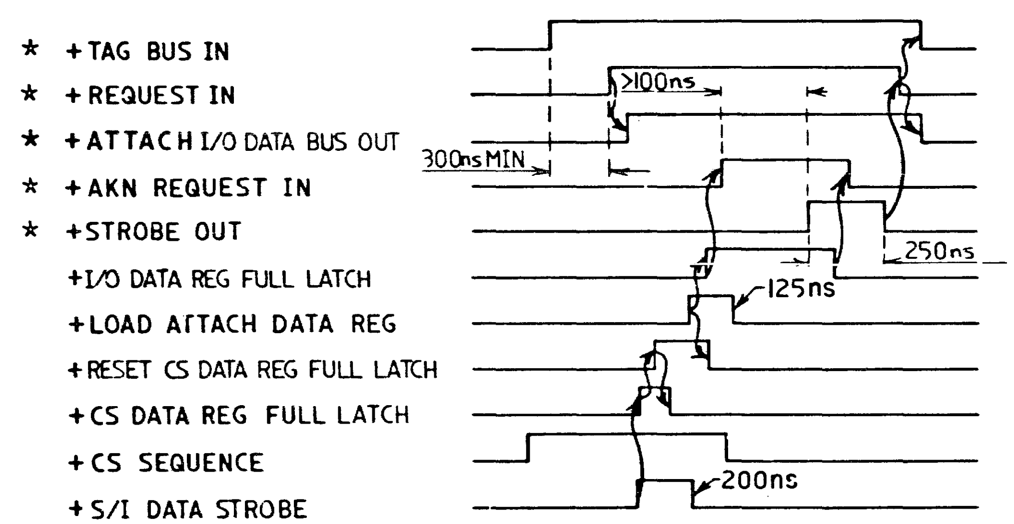
COMMAND MODE - WRITE



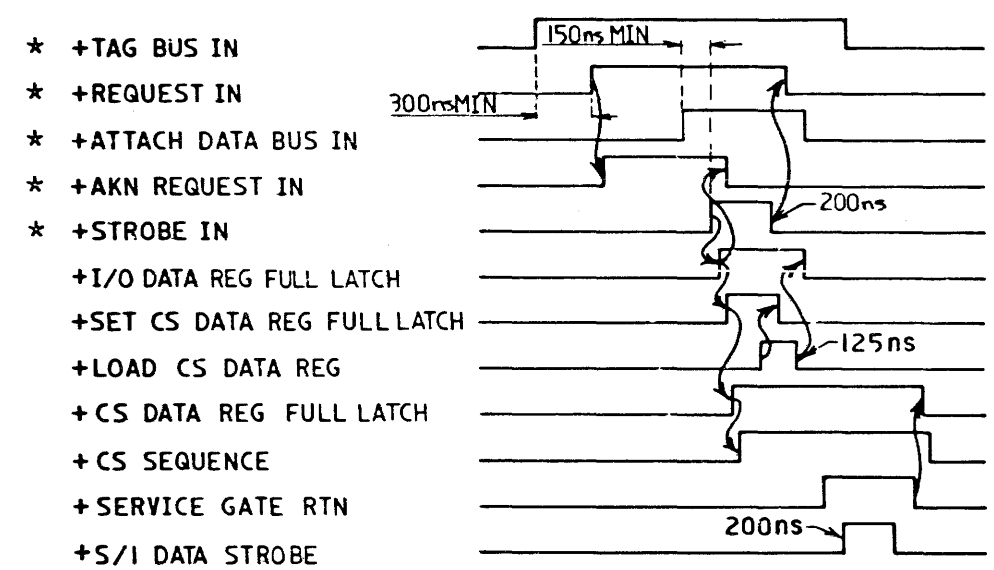
COMMAND MODE READ



HIGH SPEED DATA MODE-WRITE



HIGH SPEED DATA MODE - READ



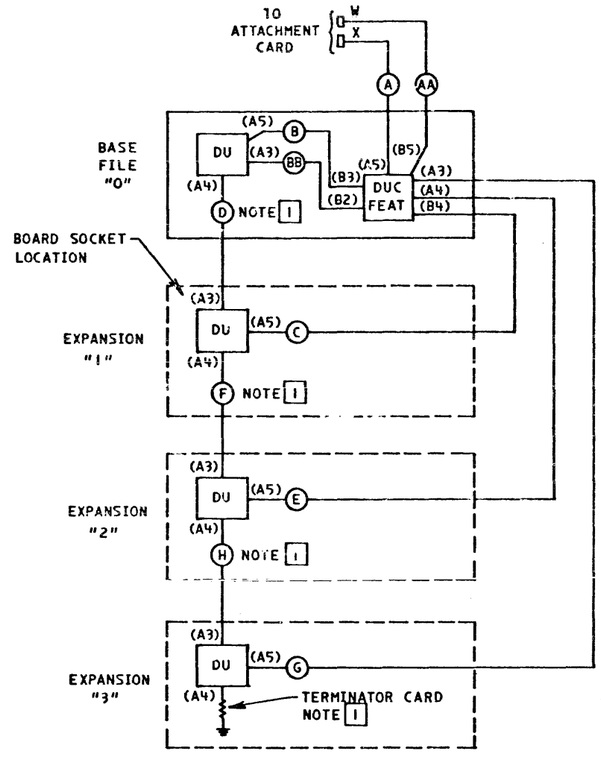
* ATTACHMENT INTERFACE LINE

EC HISTORY		DRAWING TITLE	
20FEB79	375351	ATTACHMENT TO CAP TIMINGS	
		MACH 4963	
		PART NO 6839654	
		CLASSIFICATION	IBM CORP

C

SF536

SF536



NO.	FLAT CABLE P/N	CABLE TYPE (REF)	USED ON
A	4411709 SEQ 001	5802425	4411397
AA	4411709 SEQ 002	5802425	4411397
B	4411710 SEQ 001	5802425	4411397
BB	4411710 SEQ 002	5802225	4411397
C	4411711	5802425	4411399
D	4411714	5802225	4411399
E	4411712	5802425	4411400
F	4411715	5802225	4411400
G	4411713	5802425	4411401
H	4411716	5802225	4411401

5802425 – 20 SIG (4 GND – D8, D2, B7, B13)
5802225 – 20 SIG (1 GND – D8)

NOTE :
[1] TERMINATOR CARD PN 5861353 PLUGS INTO POSITION A4 OF DU BOARD (A1) OF LAST FILE

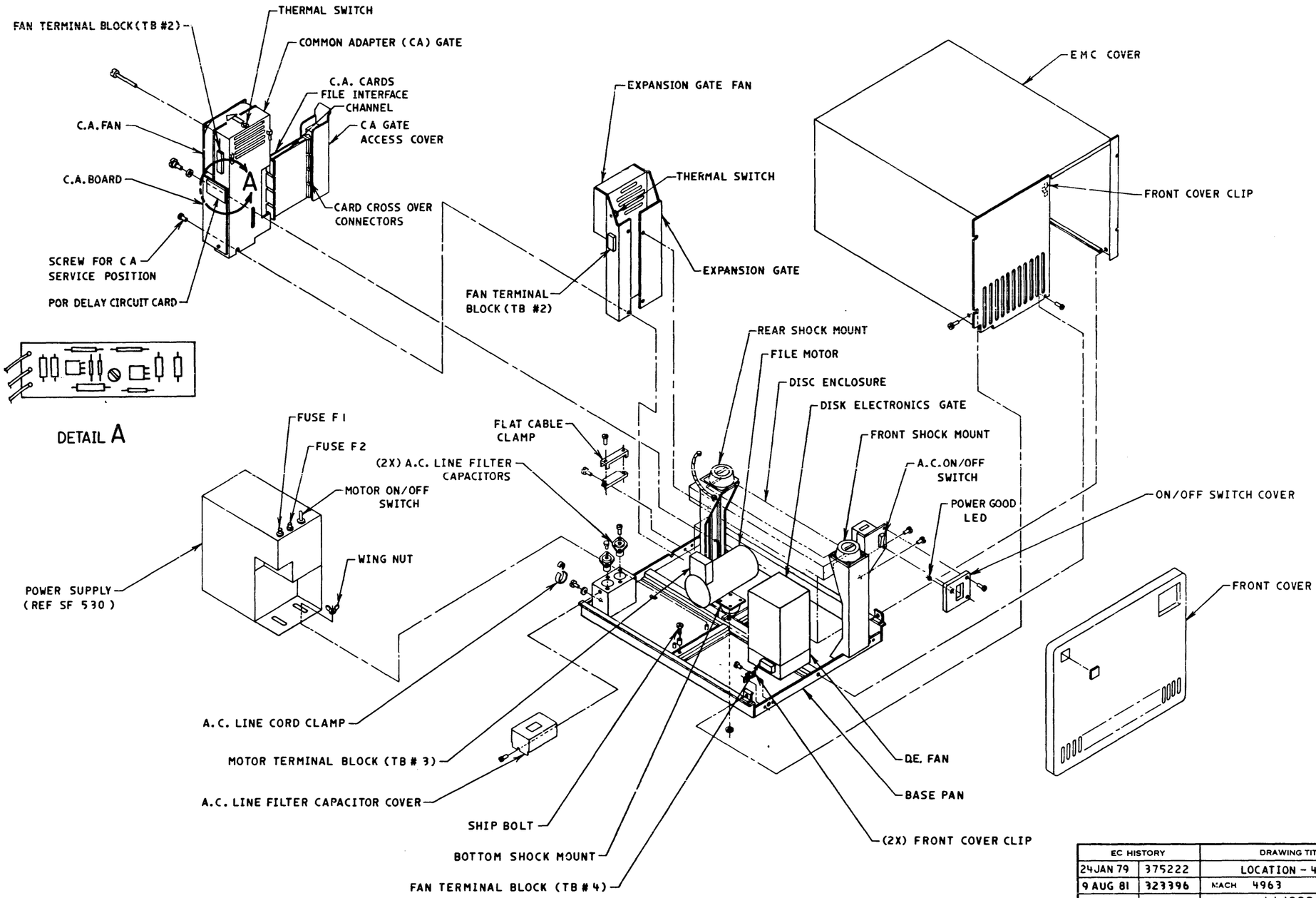
SF537

EC HISTORY		DRAWING TITLE
20FEB79	375351	CABLING OF DU'S
		MACH 4963
		PART NO 5839655
		CLASSIFICATION

C

IBM CORP

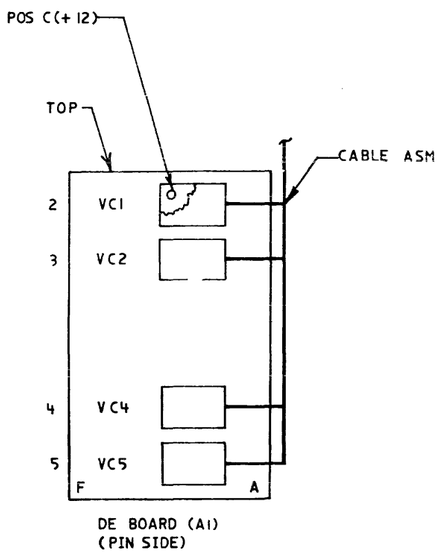
SF537



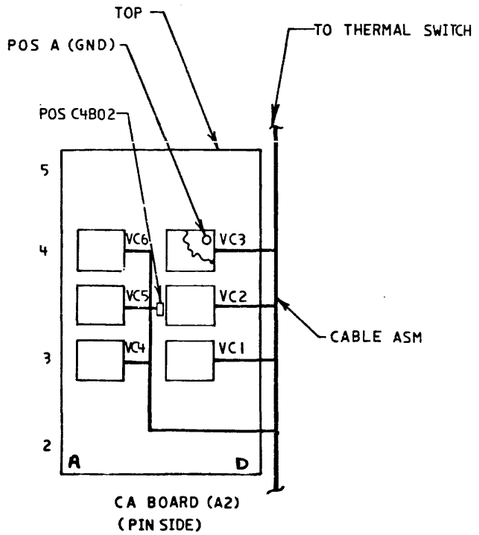
EC HISTORY		DRAWING TITLE
24JAN 79	375222	LOCATION - 4963
9 AUG 81	323396	MACH 4963
		PART NO 4412888
D		CLASSIFICATION

IBM CORP

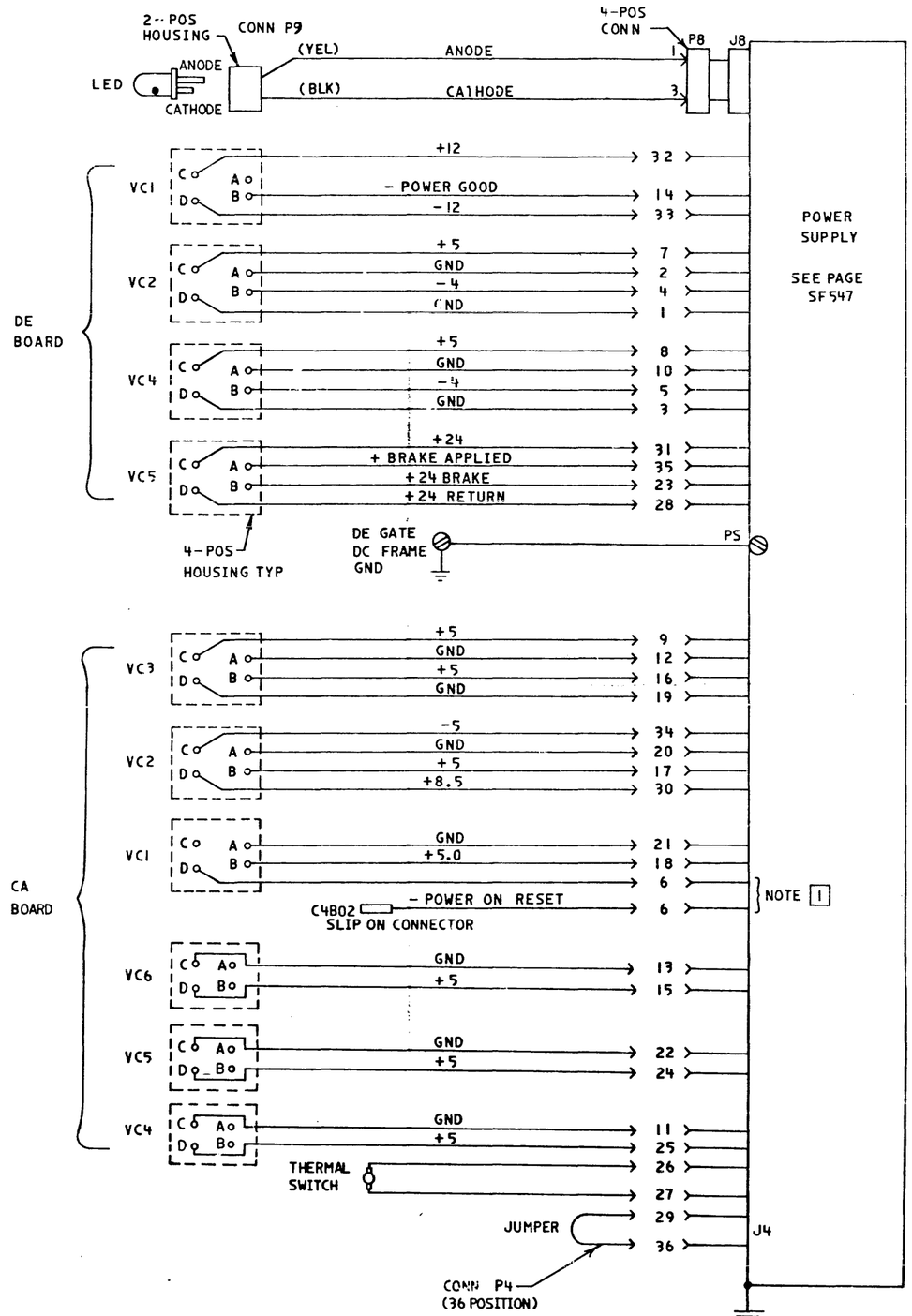
SE544



DE BOARD (A1)
(PIN SIDE)



CA BOARD (A2)
(PIN SIDE)



NOTE:

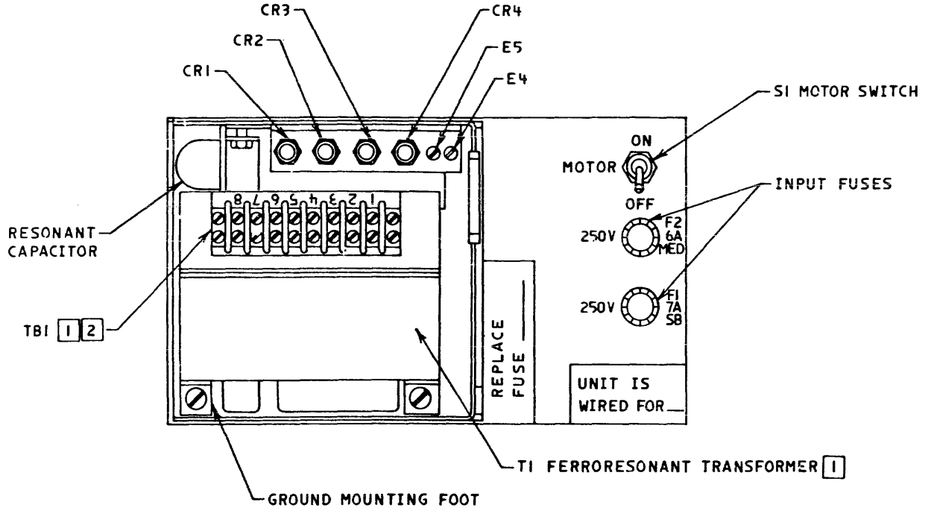
1. DEPENDING ON 4963 EC LEVEL, POWER ON RESET (6) CAN BE WIRED TO VC1-D OR SLIP ON CONNECTOR THAT PLUGS TO C4802 ON BOARD

SF545

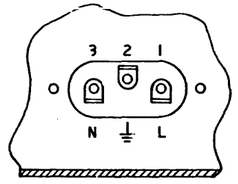
EC HISTORY		DRAWING TITLE
31 AUG 78	374947	SCHEMATIC - BDS DC
2 FEB 79	375351	MACH 4963
11 MAR 80	375662	PART NO 6837362
D		CLASSIFICATION

IBM CORP

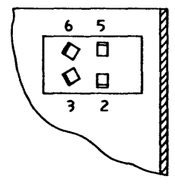
SF545



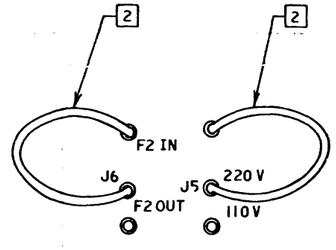
TOP VIEW



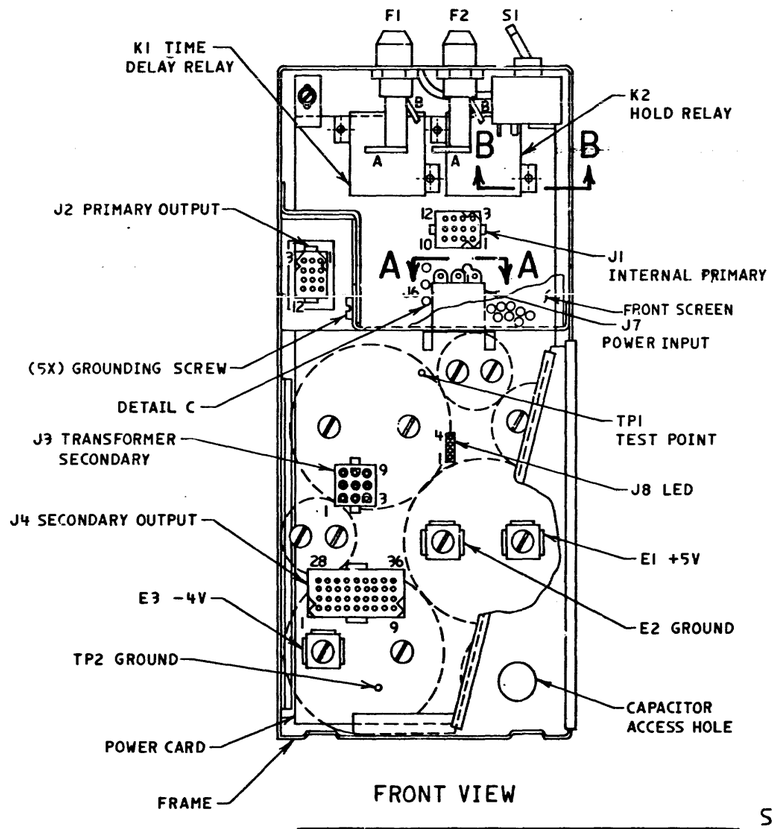
PARTIAL VIEW A-A
WIRING SIDE OF J7 CONN



PARTIAL VIEW B-B
WIRING SIDE OF S1 MOTOR SWITCH



DETAIL C
J5 AND J6 JUMPERS



FRONT VIEW

NOTES:
1. T1 AND TB1 ARE SHOWN WITH SHIELD REMOVED
2. SEE TABLE I, PAGE SF547, FOR WIRING INSTRUCTIONS

EC HISTORY		DRAWING TITLE
31 AUG 78	374947	POWER SUPPLY VIEWS
2 FEB 79	375351	MACH 4963
11 MAR 80	375662	PART NO 4411341
		CLASSIFICATION

D — IBM CORP

SF546

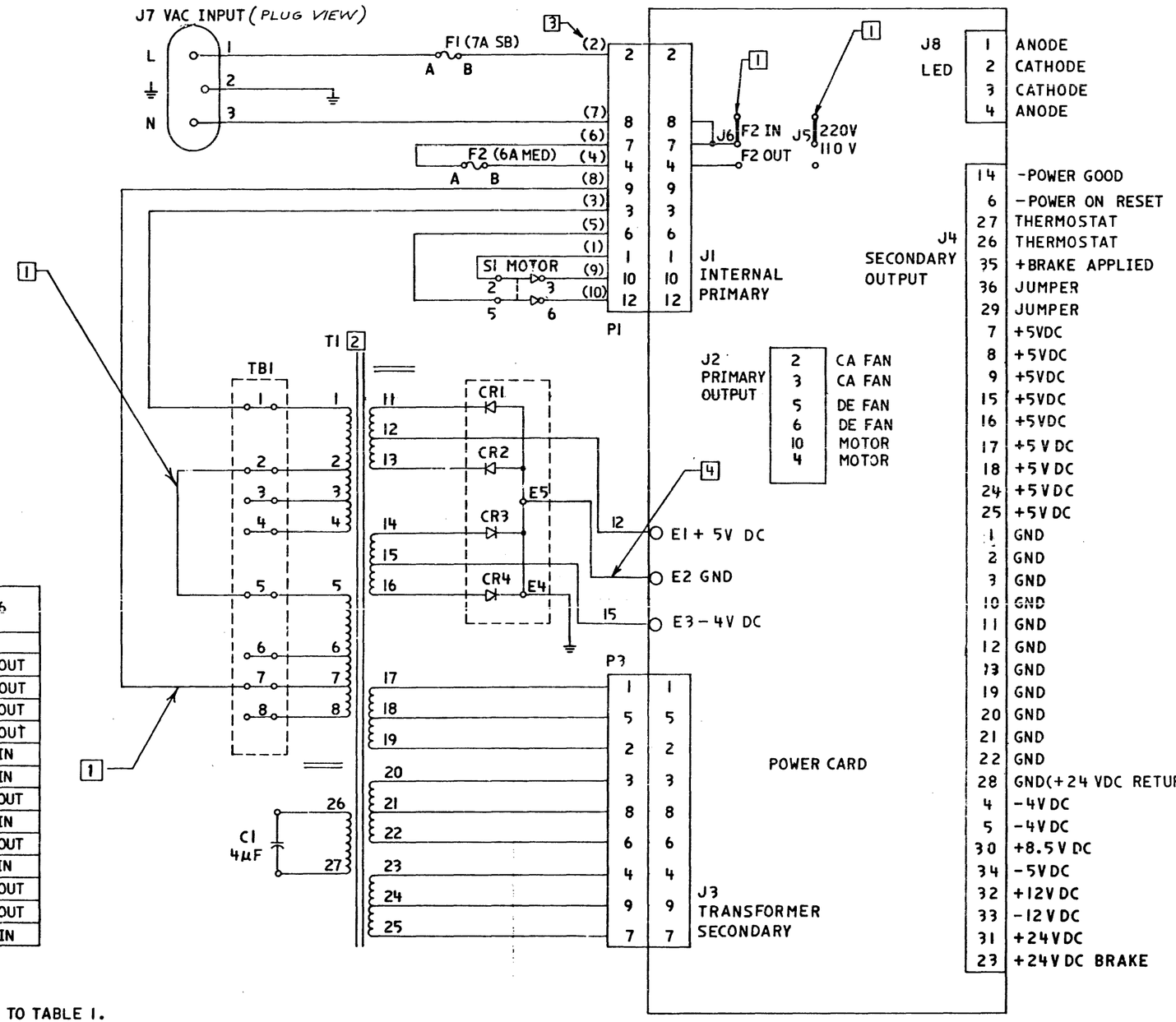


TABLE I
ALTERNATE VOLTAGES

VOLTS	FREQ [2]	TB1		J5	J6
AC	Hz	INPUT	JUMPER		
100	50,60	1-2	1-5,2-6	110V	F2 OUT
110	50,60	1-3	1-5,3-7	110V	F2 OUT
115	60	1-4	1-5,4-8	110V	F2 OUT
120	60	1-4	1-5,4-8	110V	F2 OUT
200	50,60	1-6	2-5	220V	F2 IN
208	60	1-7	2-5	220V	F2 IN
220	50	1-7	3-5	220V	F2 OUT
220	60	1-7	3-5	220V	F2 IN
230	50	1-8	3-5	220V	F2 OUT
230	60	1-8	4-5	220V	F2 IN
235	50	1-8	4-5	220V	F2 OUT
240	50	1-8	4-5	220V	F2 OUT
240	60	1-8	4-5	220 V	F2 IN

[1] WIRING SHOWN IS FOR 208V AC.
FOR ALTERNATE VOLTAGES, REFER TO TABLE I.

[2] T1 (60Hz): P/N 4411333 REF OR P/N 6825363 REF
T1 (50Hz): P/N 4411334 REF OR P/N 6825364 REF

[3] INTERNAL PRIMARY CABLE ASM WIRE NUMBERS

[4] LARGE WIRE WITHOUT A WIRE NUMBER

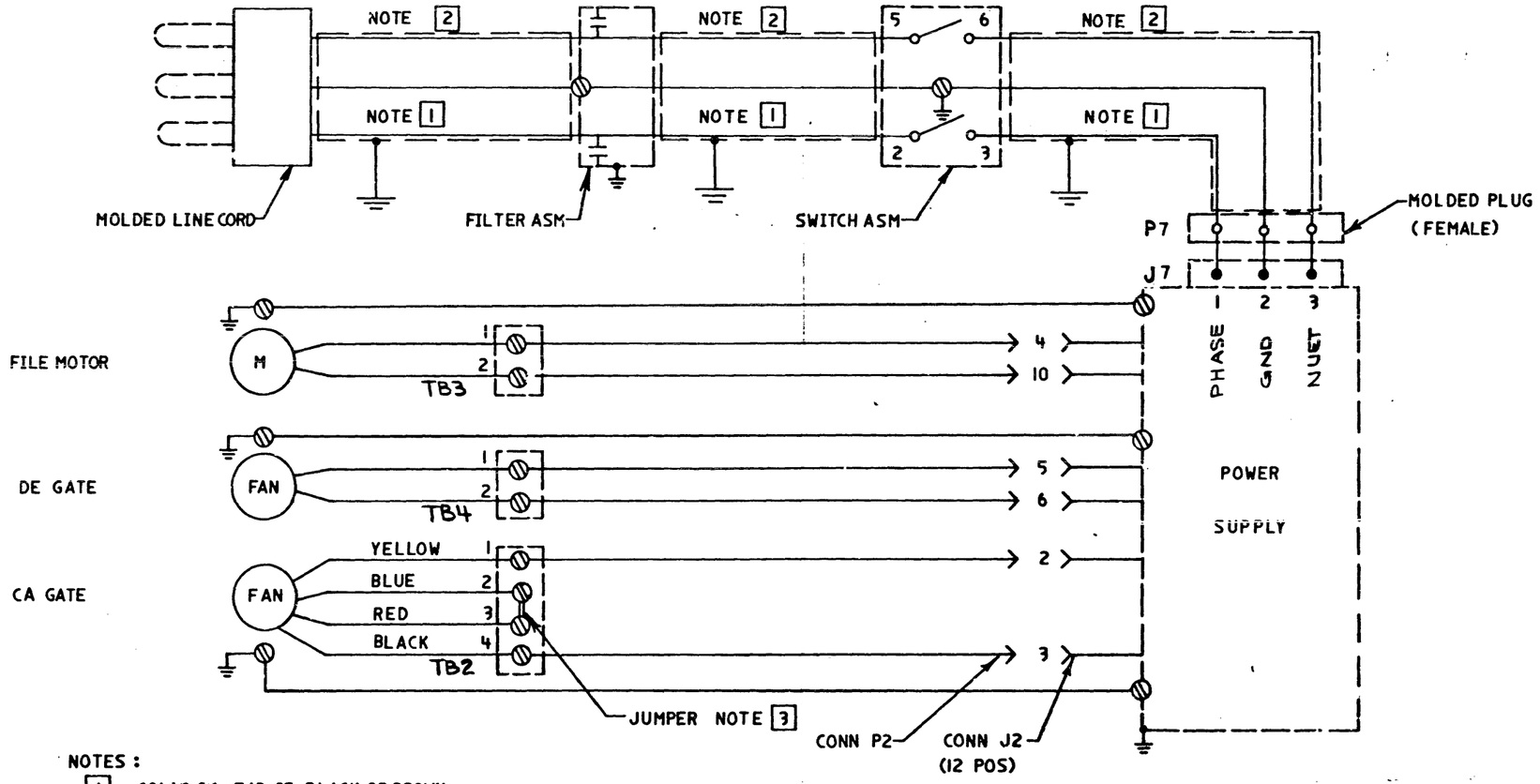
EC HISTORY		DRAWING TITLE
SEE EC	HISTORY	PWR SPLY INTERNAL WIRING
2 FEB 79	375351	MACH 4963
11 MAR 80	375662	PART NO 4411329
		CLASSIFICATION

D

IBM CORP

SF547

SF548



NOTES :

1. COLOR OF LEAD IS BLACK OR BROWN
2. COLOR OF LEAD IS WHITE OR LIGHT BLUE
3. JUMPER SHOWN FOR 220V CONNECTION. FOR 110V INSTALL JUMPERS BETWEEN POS 1 TO 2 AND 3 TO 4

EC HISTORY		DRAWING TITLE
31AUG78	374947	SCHEMATIC – PWR AC
2 FEB 79	375351	MACH 4963
		PART NO 6837363
C		CLASSIFICATION

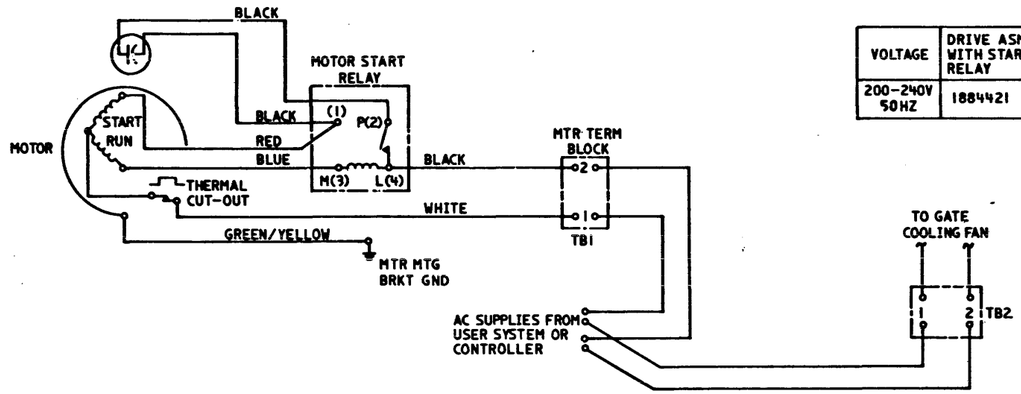
IBM CORP

SF548

SF548

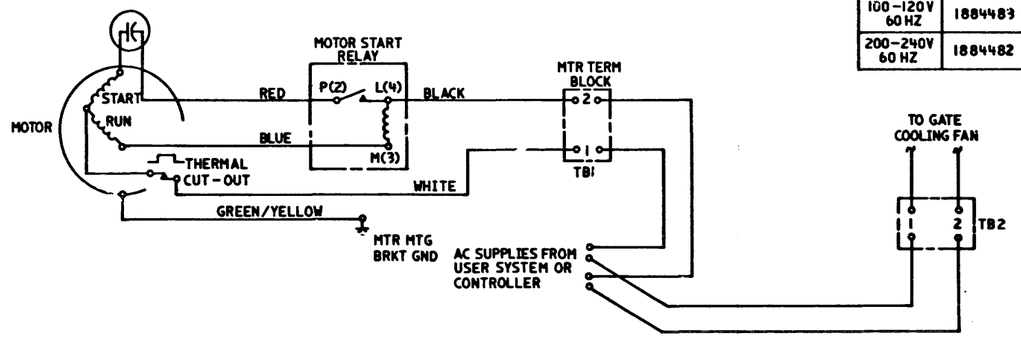
SF549

200-240V 50HZ



VOLTAGE	DRIVE ASM WITH START RELAY	START RELAY	GATE COOLING FAN ASM
200-240V 50HZ	1884421	5616573	5145639

100-120V 60HZ
200-240V 60HZ

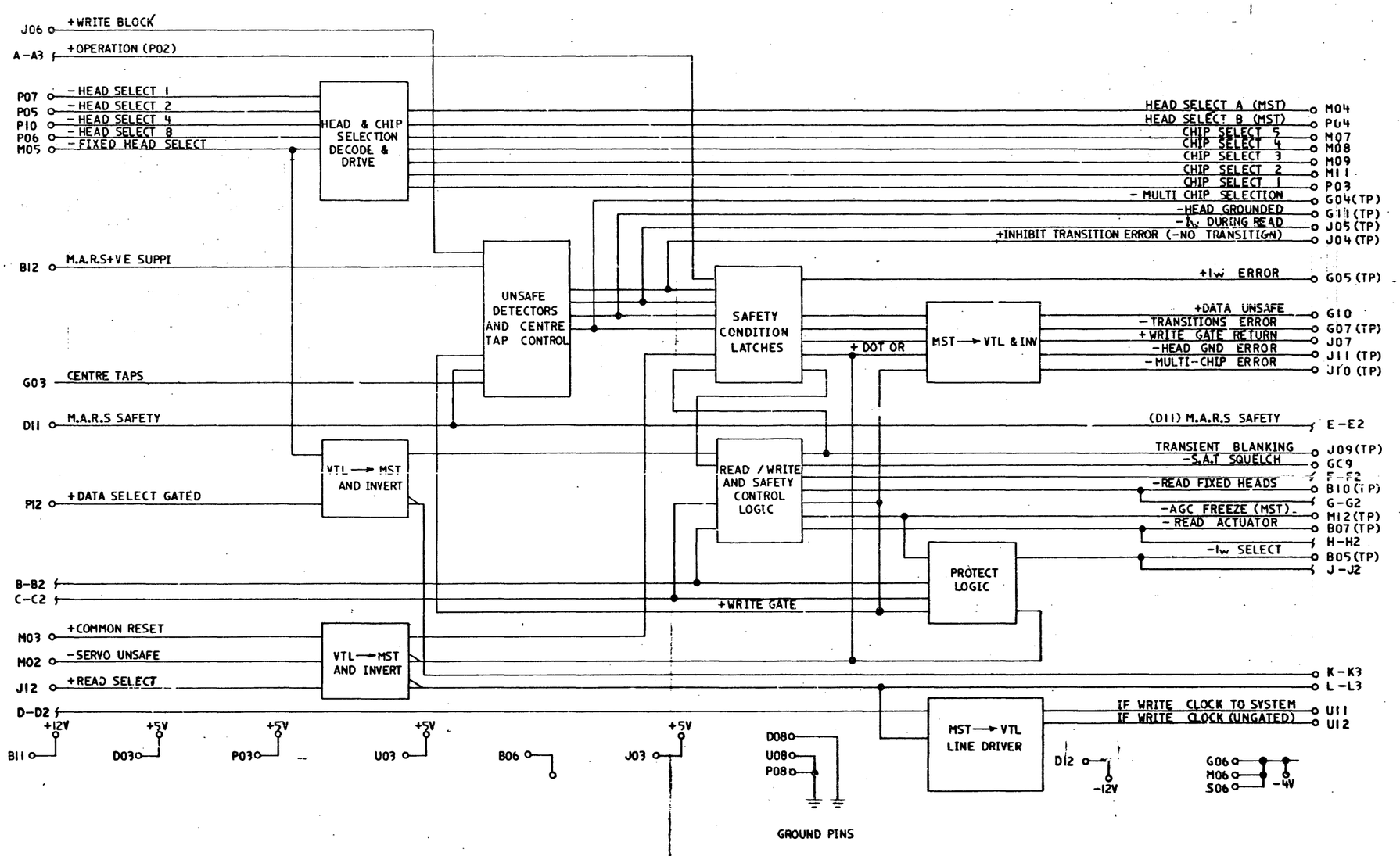


VOLTAGE	DRIVE ASM WITH START RELAY	START RELAY	GATE COOLING FAN ASM
100-120V 60HZ	1884483	2175165	5145615
200-240V 60HZ	1884482	2410082	5145639

SF549

EC HISTORY		DRAWING TITLE
28FEB79	375351	AC POWER TO DU
		MACH 4963
		PART NO 6839629
		CLASSIFICATION
C		IBM CORP

SF549



EC HISTORY		DRAWING TITLE
20FEB79	375351	A1B2 DATA CHANNEL CARD
		MACH 4963
		PART NO 6839601
		CLASSIFICATION

D

IBM CORP

SF550

SF551

U02 -WRITE DATA

VTL → MST (PART)

4 BIT SHIFT REG

J13 (TP) SHIFT REG SHIFT PULSE

G12 *WRITE DC

M10 2F WRITE CLOCK

PRE-COMP TIMING

PRE-COMP ENCODER

A.C. TRIG (PART)

∫ D-D1

∫ D-D3

G13 *WRITE SELECT

VTL → MST AND INVERT

∫ M-M3

∫ B-B1

∫ B-B3

AGC CONTROL VOLTAGE J02 (TP)

F-F1 ∫

G-G1 ∫ (B10)-READ FXD HEADS

E-E1 ∫ (D10 M.A.R.S. SAFETY

D10 FXD HEAD I/O LINES

D09 FXD HEAD I/O LINES

D07 WRITE CURRENT

M.A.R.S. INTERFACE (LOW GAIN)

DIFFERENTIAL ANALOGUE SIGNAL (HIGH LEVEL) D13 (TP)

DIFFERENTIAL ANALOGUE SIGNAL (HIGH LEVEL) B13 (TP)

VGA

AGC CONTROL AND SQUELCH DIFFERENTIAL AMPLIFIER

ΔV DETECTOR

∫ N-N3

H-H1 (B07)-READ ACTUATOR

J-J1 (B05)-I∞ SELECT

WRITE CURR DEFINING RES

D04 (TP)

M.A.R.S. INTERFACE AND IW SOURCE

DIFFERENTIAL BUFFERS A.G.C FREEZE DRIVER INTERNAL SUPPLIES & VTL → MST

DIFFERENTIAL ANALOGUE SIGNAL TO DATA SERVO B02

DIFFERENTIAL ANALOGUE SIGNAL TO DATA SERVO B03

-V INTERNAL (-1.32V) B08 (TP)

∫ C-C1

∫ C-C3

AGC REF VOLTAGE G02 (TP)

D05 ACTUATOR I/O LINES

D06 ACTUATOR I/O LINES

B04 -ACG FREEZE (VTL)

+V INTERNAL (5.8V) B09 (TP)

EC HISTORY		DRAWING TITLE
20FEB79	375351	A1 B2 DATA CHANNEL CARD
		MACH 4963
		PART NO 6839602
		CLASSIFICATION

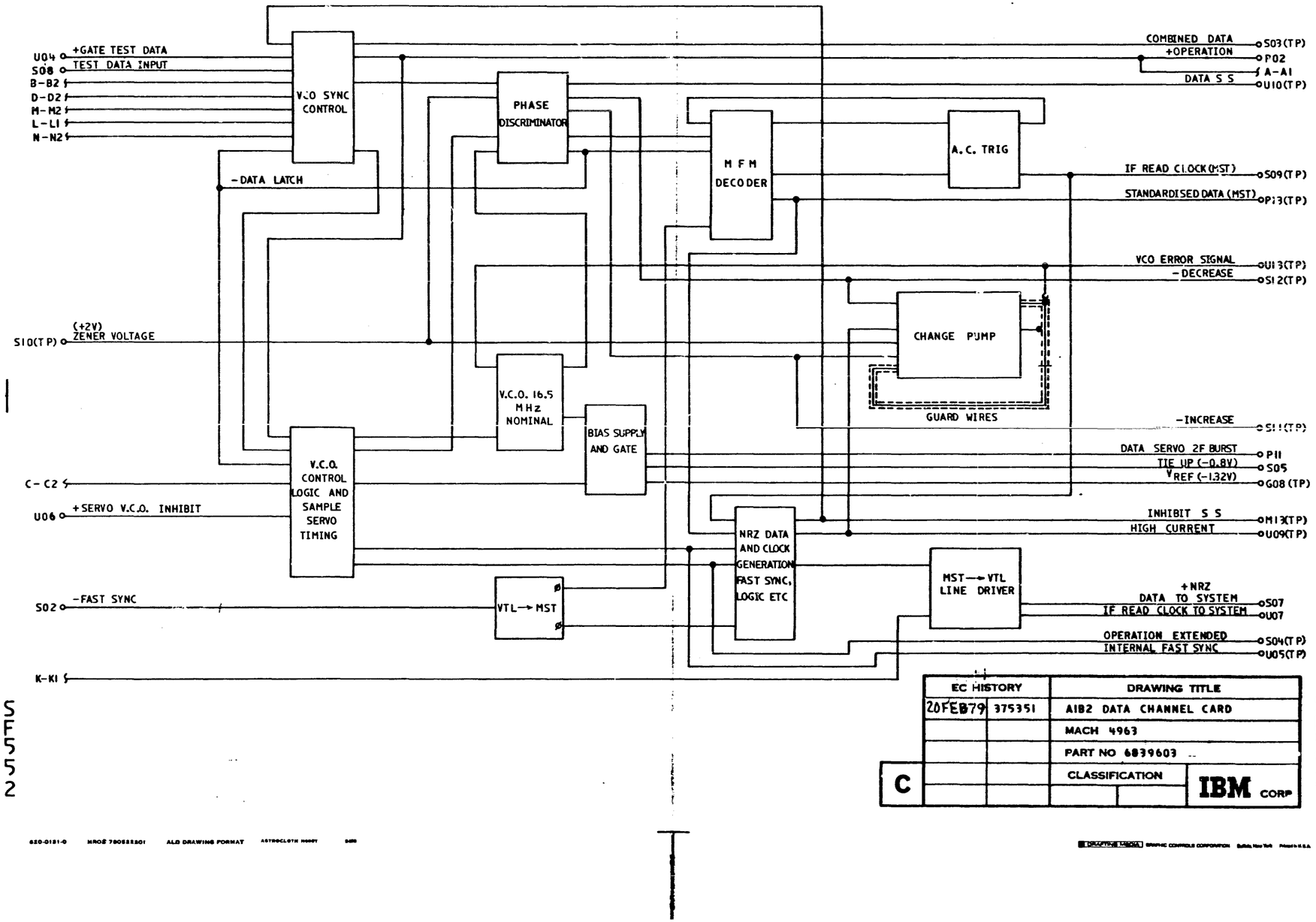
D

IBM CORP

SF551

SF551

SF552



EC HISTORY		DRAWING TITLE
20FEB79	375351	AIB2 DATA CHANNEL CARD
		MACH 4963
		PART NO 6839603
		CLASSIFICATION

C

IBM CORP

SF552

SF552

620-0131-0 MROS 780SS2501 ALD DRAWING FORMAT ASTROCLOTH MYLAR 0499

DRAFTING SYSTEMS GRAPHIC CONTROLS CORPORATION Buffalo, New York Printed in U.S.A.

A1B2 – DATA CHANNEL – INPUT

PIN		LINE NAME	SOURCE	PAGE
SF550	J06	+ WRITE BLOCK	C2G11	SF554
	P07	– HEAD SEL 1	C2P12	SF556
	P05	– HEAD SEL 2	C2P10	SF556
	P10	– HEAD SEL 4	C2J06	SF556
	P06	– HEAD SEL 8	C2G02	SF556
	M05	– FIXED HEAD SEL	C2D09 (D1D13) (D2J04)	SF556
	B12	M.A.R.S.	A2D03 (B1A13)	SF527
	G03	CENTER TAPS	A2B08 (A1C13)	SF527
	D11	MARS SAFETY	A2B07 (B1D11)	SF527
	P12	+ DATA SEL GATED	A2D02	SF527
	M03	+ COMMON RESET	C2U09	SF554
	M02	– SERVO UNSAFE	C2S11	SF554
	J12	+ READ SELECT	C2J12	SF554
SF551	U02	– WRITE DATA	A5B10	SF503
	G12	+ WRITE D.C.	D1D11	
	M10	2F WRITE CLOCK	E2G12	SF568
	G13	+ WRITE SELECT	C2U12 – E1C13	SF554
	D10	FXD HDS I/O LINES	B1B13 – E1B13	SF527
	D09	FXD HDS I/O LINES	B1C13 – E1B11	SF527
	D07	WRITE CURRENT	A2D07 – A1D11	SF527
	D05	ACTUATOR I/O LINES	A2D05 – D1B13	SF527
	D06	ACTUATOR I/O LINES	A2D04 – D1B11	SF527
	B04	– AGC FREEZE	C2G02 – D2G08	SF556
SF552	U04	+ GATE TEST DATA		TP
	S08	TEST DATA INPUT		TP
	U06	+ SERVO VCO INHIBIT	E2G03	SF568
	S02	– FAST SYNC	A5D05	SF503

A1B2 – DATA CHANNEL – OUTPUT

PIN		LINE NAME	SYNC	PAGE
SF550	M04	HEAD SEL A(MST)	A2B03 A1E13	SF527
	P04	HEAD SEL B(MST)	A2B04 A1C11	SF527
	M07	CHIP SELECT 5	A1E11	SF527
	M08	CHIP SELECT 4	A1B11	SF527
	M09	CHIP SELECT 3	A2B02	SF527
	M11	CHIP SELECT 2	A2B05	SF527
	P09	CHIP SELECT 1	A2B06	SF527
	G09	– S.A.T. SQUELCH	F1B13	SF527
	U11	IF WRITE CLOCK	A5D12	SF503
	U12	IF WRITE CLOCK	D2J05	SF564
SF551	B02	DIFF ANALOG SIG	E2B03	SF567
	B03	DIFF ANALOG SIG	E2D02	SF567
SF552	P02	+ OPERATION		TP
	P11	DATA SERVO 2F	E2G08	SF568
	S05	TIE UP		TP
	S07	+ NRZ DATA	A5B08	TP
	U07	IF READ CLOCK	A5D10	TP
SF550	G10	+ DATA UNSAFE	C2M11	SF554
	J07	+ WRITE GATE RTN		TP
	J05	+ IN DURING READ		TP
SF552	S09	IF READ CLOCK		TP
	P13	STANDARDIZED DATA		TP
	S03	COMBINED DATA		TP
	U10	DATA SS		TP

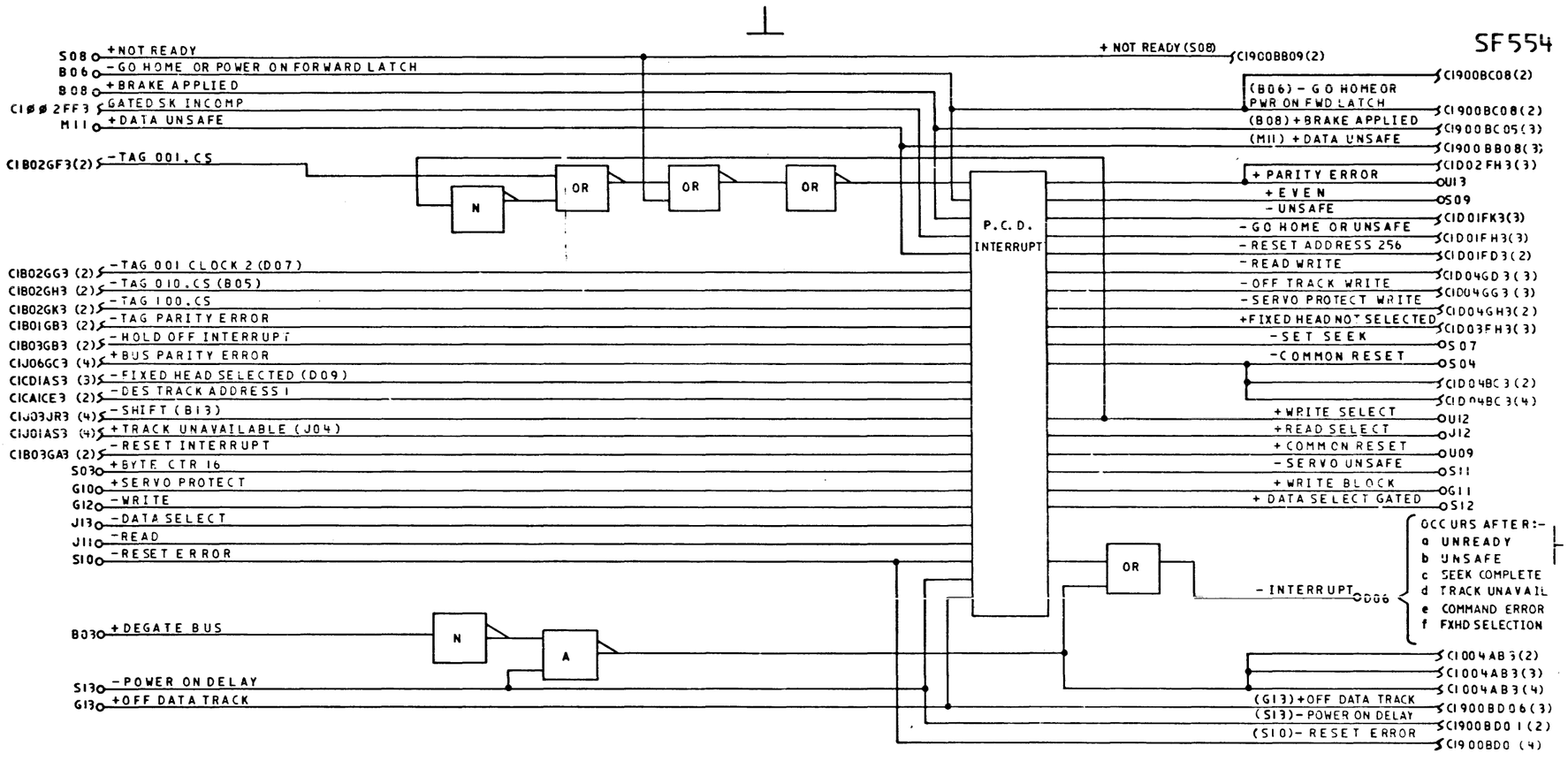
EC HISTORY		DRAWING TITLE
20FEB79	375351	A1B2 DATA CHANNEL
11 MAR 80	375662	MACH 4963
		PART NO 6839604
		CLASSIFICATION

C

IBM CORP

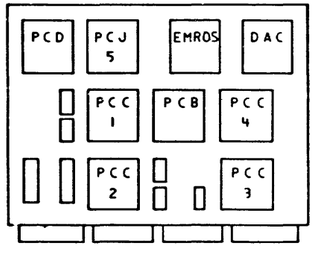
SF553

SF553



POWER SUPPLIES

+5V	PINS	D03, J03, P03, U03
GND	PINS	D08, J08, P08, U08
+12V	PIN	B11
-12V	PIN	D12



MODULE PLACEMENT

* NOTE: SEE LOGIC PAGE SF585A FOR TAG DECODE INFORMATION

EC HISTORY		DRAWING TITLE
20FEB79	375351	AIC2 LOGIC 1.
		MACH 4963
		PART NO 6839605
		CLASSIFICATION

C

IBM CORP

SF554

SF555

C1900BB09(1) +NOT READY (S08)
U10 CTR 5 IN SYNC
U07 + HOME
C1D04GH3(1) - SERVO PROTECT WRITE
U04 +ROS DA ERROR
U11 MISSING PES
U05 ILLEGAL MOVE
C1J02HW3(4) - FORCE DISTANCE 127
C19005C08(1) -GO HOME OR POWER ON FORWARD LATCH (B06)
C1D01FD3(1) - RESET ADDRESS 256
C1J02FG3(4) - OUT

S06 - COUNT UP 2 TRACKS
U06 - ABS TRACK ADDRESS 1
S05 - COUNT DOWN 2 TRACKS

E10C90 +CLOCK IN

+5V

G09 - CONTROL SAMPLE

P07 - TAG BIT 0
M07 - TAG BIT 1
M09 - TAG BIT 2
M08 - TAG PARITY
C1900BD01(1) - POWER ON DELAY (S13)
C1D04BC3(1) - COMMON RESET (S04)
C1CBIAS3(3) - HEAD REG 1 (P12)
C1CBIBC3(3) - HEAD REG 2 (P10)
C1CC1AS3(3) - HEAD REG 4 (J06)
C1CC1BC3(3) - HEAD REG 8 (G02)
C1CD1AS3(3) - FXHD SELECTED (D09)
C1004BH1(3) - BUS BIT 1 (P02)
C1002FF30 - STROBE LATCH
C1002FJ30 - LATCH INPUT

C1004AB3(1)

PCB TAGS

PCC (A) ADDRESS 1

OR

OR

OR

JUMPER

- COUNT DOWN TO STAGE 8 C1CA2FP3(3)
- COUNT UP TO STAGE 8 C1CA2FN3(3)
- ABS TRACK ADDRESS 4 C1CA2FR3(3)
- CARRY 2 C1CA3IC3(3)
-DES TRACK ADDRESS 1 C1CA1CE3(1) C1CA1CE3(4)
+ REL TRACK ADDRESS 1 C1CA4CQ3(4) E70B60
-DES TRACK ADDRESS 256 C1CA1AS3(4)
-DES TRACK ADDRESS 2 C1CA1CF3(4)
+PARITY OF BUS IN BITS 6,7 C1CA1AI3(4)
+ REL TRACK ADDRESS 2 F10B60 C1CA4CU3(4)

- BUS BIT 6 P05
- BUS BIT 7 M06
- TAG 000 C1B01DB30

C1B02GH3(1) C1B02GH3(3) C1B02GH3(4)
-TAG 010.CS B05
+OSC E30C90
-TAG 011 C1B01FE3(3) C1B01FE3(4)
- TAG PARITY ERROR C1B01GL3(1)
- TAG 001 CS NO FIXED HEAD G06
-TAG 100 C1B01FG3(3)
-TAG 101 C1B01DG3(3)
-TAG 110 C1B01DH3(3)
+ENABLE BUS C1B02GA3(3) C1B02GA3(4)
-TAG 001.CS C1B02GF3(1) C1B02GF3(3)
+CLOCK D60B60
-TAG 111 C1B01DJ3(3)
-SET OUTPUT REG C1B02GB3(3)
- TAG 100.CS C1B02GK3(1)
-RESET INTERRUPT C1B030A3(1)
-TAG 001.CLOCK 1 C1B02GE3(4)
-SAMPLE BUS PARITY C1B02GJ3(4)
+HEAD 1 SELECTED M12
-HOLD OFF INTERRUPT C1B03GB3(1)
-TAG 001.CLOCK 2 D07 C1B02GG3(1)

- CONTROL SAMPLE RECEIVED P09

SF555

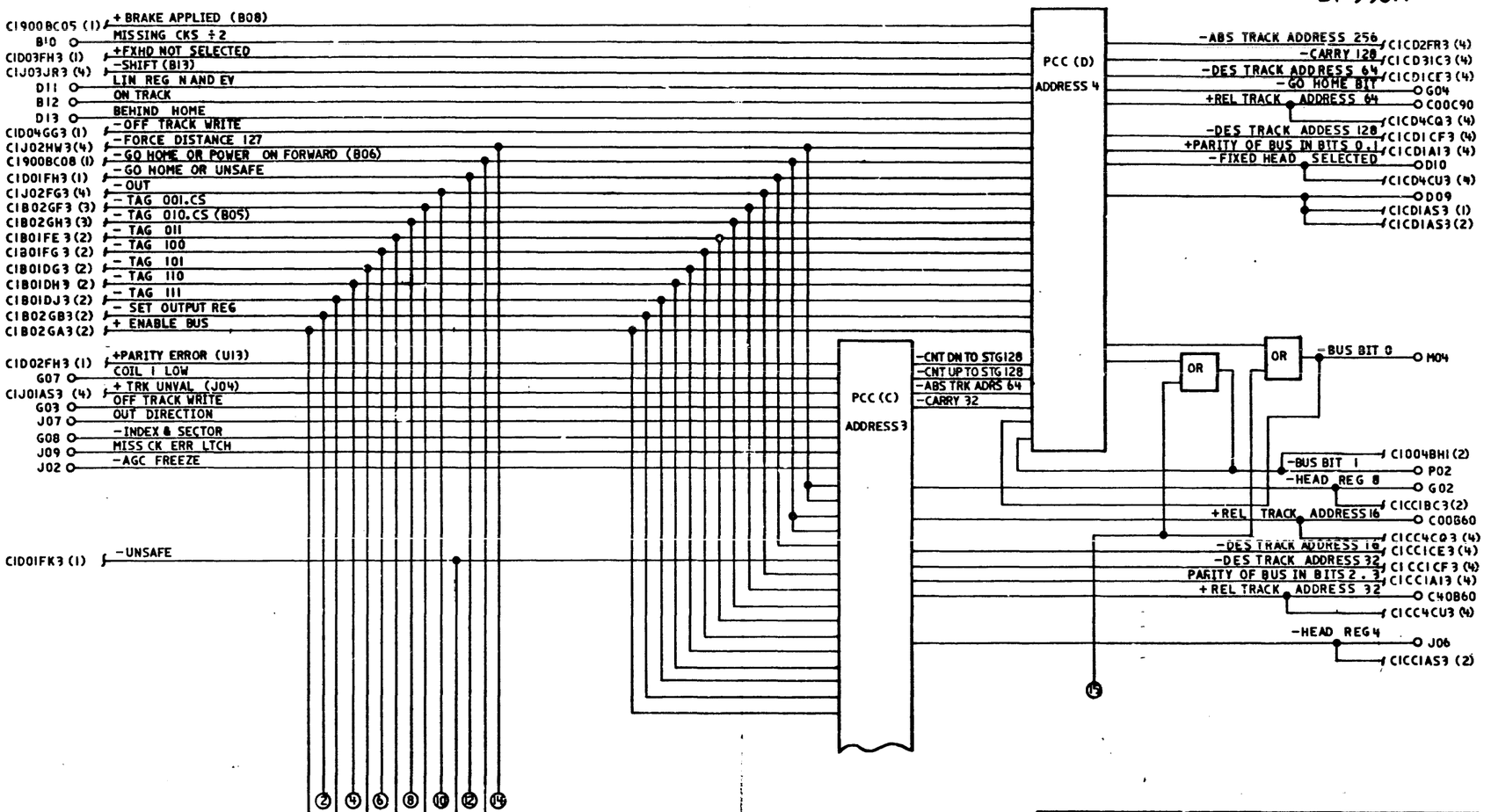
EC HISTORY		DRAWING TITLE
20FEB79	375351	AIC2 LOGIC 1 CARD
		MACH 4963
		PART NO 6839606
		CLASSIFICATION

D

IBM CORP

SF555

SF556A



SF556A

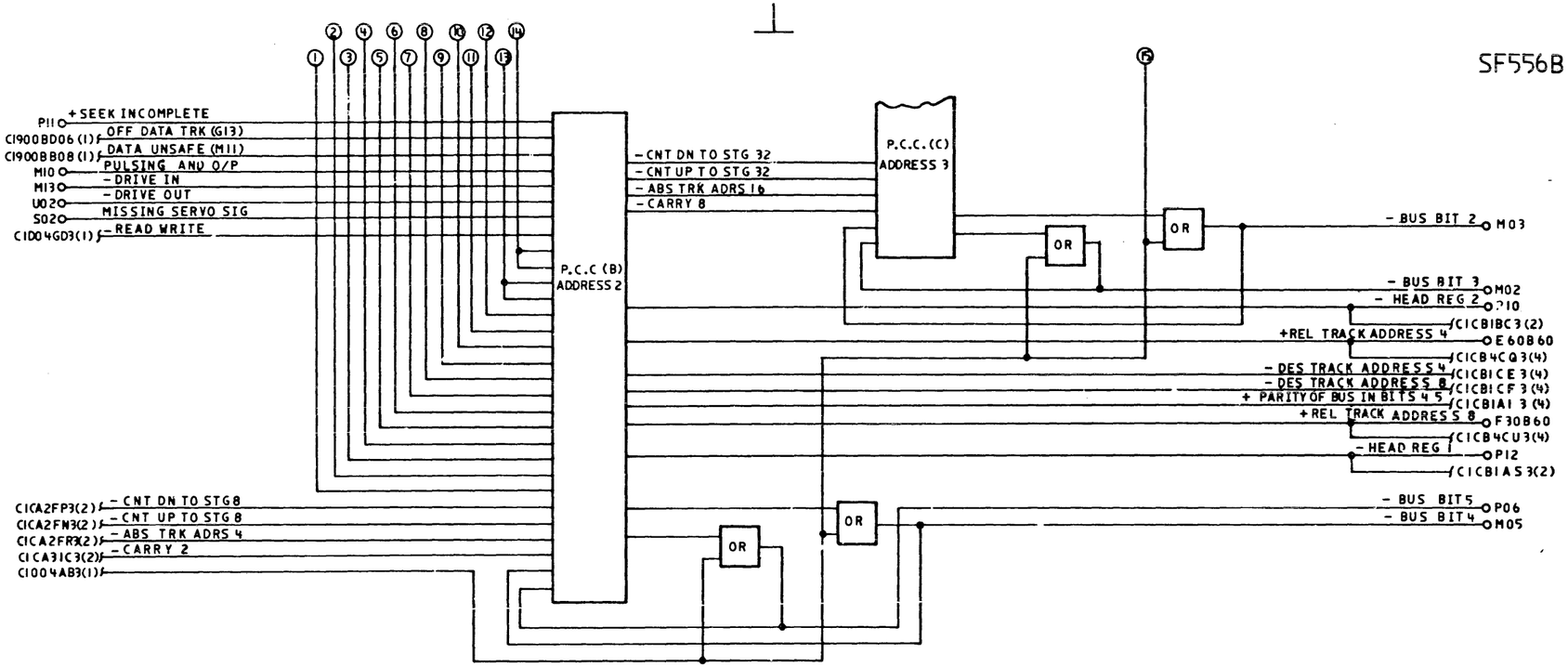
EC HISTORY		DRAWING TITLE
20FEB79	375351	AIC2 LOGIC 1
		MACH 4963
		PART NO 6839607
		CLASSIFICATION

C

IBM CORP

SF556A

SF556B



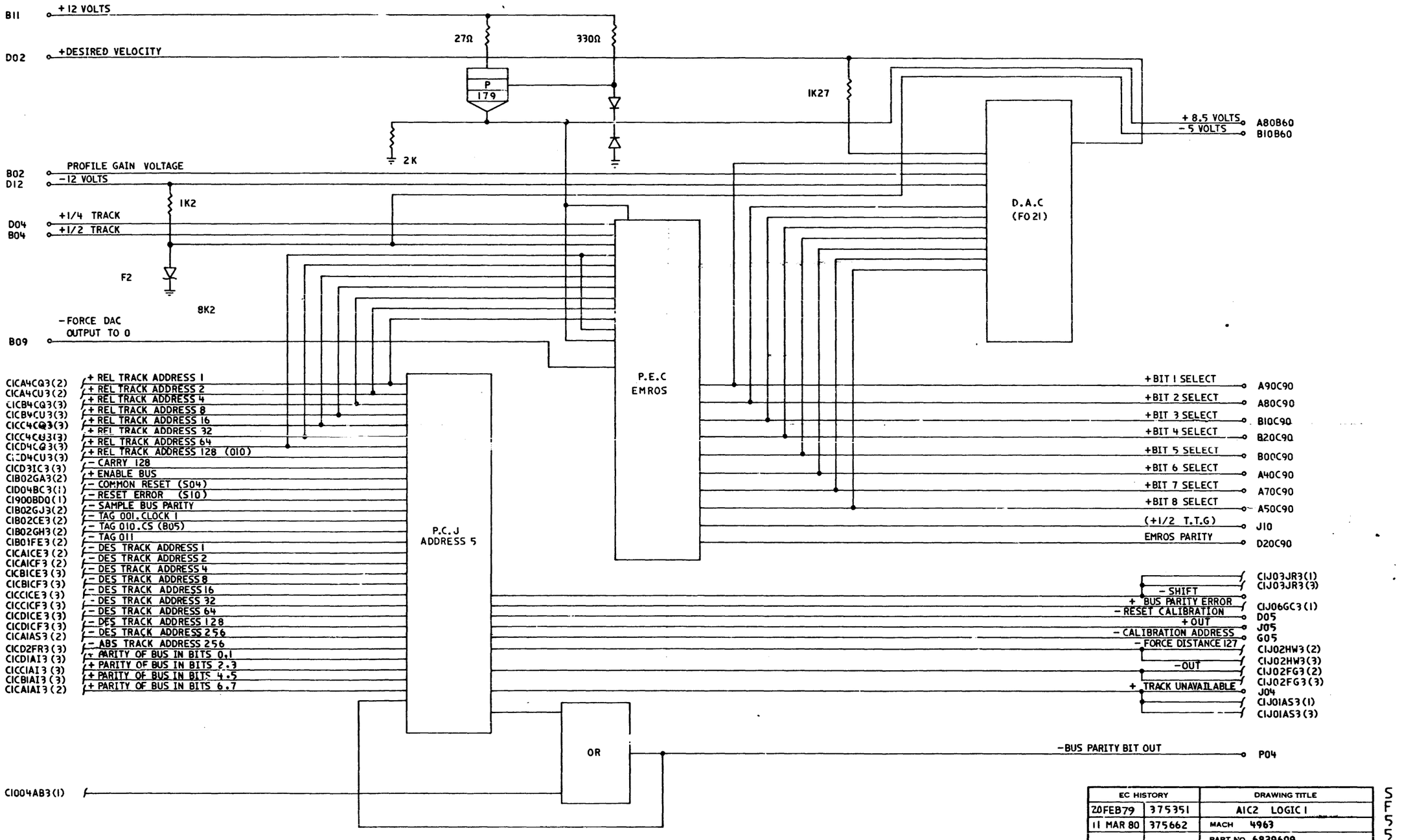
EC HISTORY		DRAWING TITLE
20FEB79	375351	A1C2 LOGIC 1
		MACH 4963
		PART NO 6839608
C		CLASSIFICATION

IBM CORP

SF556B

SF556B

SF 557



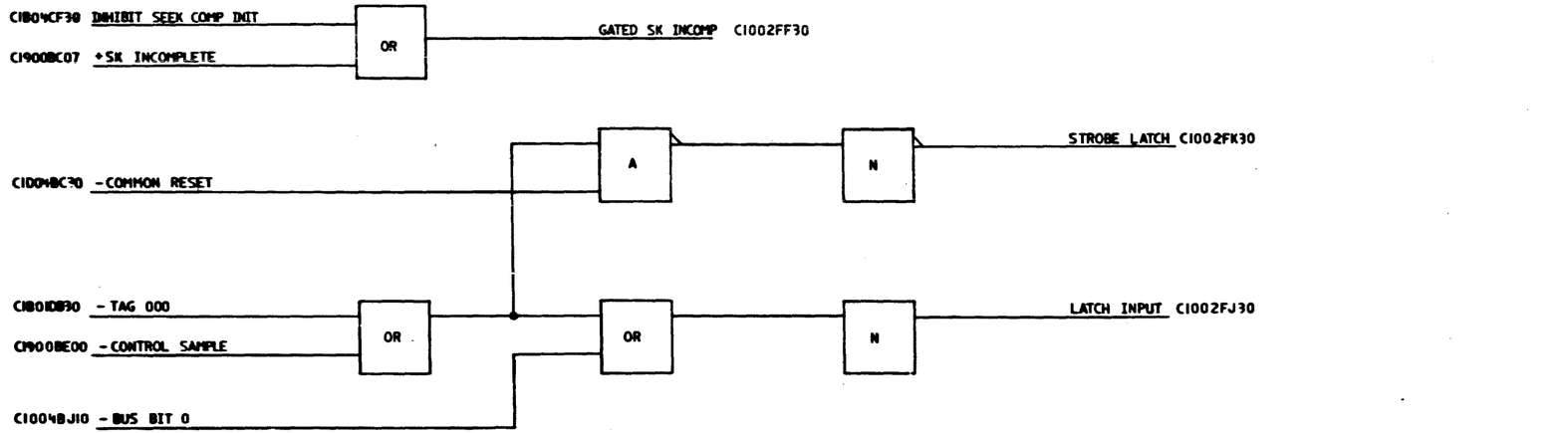
EC HISTORY		DRAWING TITLE
20FEB79	375351	AIC2 LOGIC 1
11 MAR 80	375662	MACH 4963
		PART NO 6839609
		CLASSIFICATION

D

IBM CORP

SF557

SF558



SF558

EC HISTORY		DRAWING TITLE
20FEB79	375351	AIC2 LOGIC 1
		MACH 4963
		PART NO 6839610
		CLASSIFICATION

C

IBM CORP

SF558

AIC2 - LOGIC 1 - INPUT

PIN	LINE NAME	SOURCE	PAGE
SF554 S08	+NOT READY	D2M07	SF562
B06	-GO HOME	D2U10	SF562
B08	+BRAKE APPLIED	F2M02 (D2P07)	SF570 (SF563)
M11	+DATA UNSAFE	B2G10	SF550
S03	+BYTE CTR 16	D2S08	SF565
G10	+SERVO PROTECT	D2U06	SF563
G12	-WRITE	A5D11	SF503
J13	-DATA SELECT	A5D04	SF503
J11	-READ	A5D09	SF503
S10	-RESET ERROR	A5D06 (D2P13)	SF503 (SF563)
B03	+DEGATE BUS	A5D12	SF503
S13	-POWER ON DELAY	F2P02 (D2U09)	SF570 (SF563)
G13	+OFF DATA TRACK	E2J13 (E1A11)	SF568 (SF510)
SF555 U10	CRT 5 IN SYNC	D2G07	SF562
U07	+HOME	D2P10	SF562
U04	+ROS ERROR	D2D09	SF565
U11	MISSING PES	F2J04	SF570
U05	ILLEGAL MOVE	D2P04	SF563
S06	-COUNT UP 2 TRACKS	D2D05	SF560
U06	-ABS TRK ADDRESS 1	D2B05	SF560
S05	-COUNT DN 2 TRACKS	D2D07	SF560
G09	-CONTROL SAMPLE	A5B03	SF503
P07	-TAG BIT 0	A4B02 (A3B02)	SF505
M07	-TAG BIT 1	A4B03 (A3B03)	SF505
M09	-TAG BIT 2	A4B04 (A3B04)	SF505
M08	-TAG PARITY	A4B05 (A3B05)	SF505

AIC2 - LOGIC 1 - INPUT

PIN	LINE NAME	SOURCE	PAGE
SF556 D11	LINE REG N + EV	D2B03	SF560
B12	ON TRACK	F2G12 (E2G13)	SF570 (SF568)
D13	BEHIND HOME	D2U11	SF565
G07	COIL LOW	F2G03	SF570
G03	OFF TRACK WRITE	E2D09	SF567
J07	OUT DIRECTION	F2S13 (D2D06)	SF570 (SF562)
G08	-INDEX AND SECTOR	D2P05	SF563
J09	MISS CK ERR LCH	D2M03	SF563
J02	-AGC FREEZE	D2G09 (B2B04)	SF565 (SF551)
P11	+SEEK INCOMPLETE	F2S07 (D2J13)	SF570 (SF563)
M10	PULSING AND O/P	D2M04	SF563
M13	-DRIVE IN	F2P11 (D2S07)	SF570 (SF565)
U02	-DRIVE OUT	F2S13 (D2U07)	SF570 (SF565)
S02	MISSING SERVO SIG	D2M02	SF563
SF557 D02	+DESIRED VELOCITY	D2B02	SF561
B02	PROFILE GAIN VOLTAGE	D2B08	SF562
D04	+1/4 TRACK	D2B10	SF560
B04	+1/2 TRACK	D2D10	SF560

EC HISTORY		DRAWING TITLE
20FEB79	375351	AIC2 LOGIC 1
		MACH 4963
		PART NO 6839611
		CLASSIFICATION

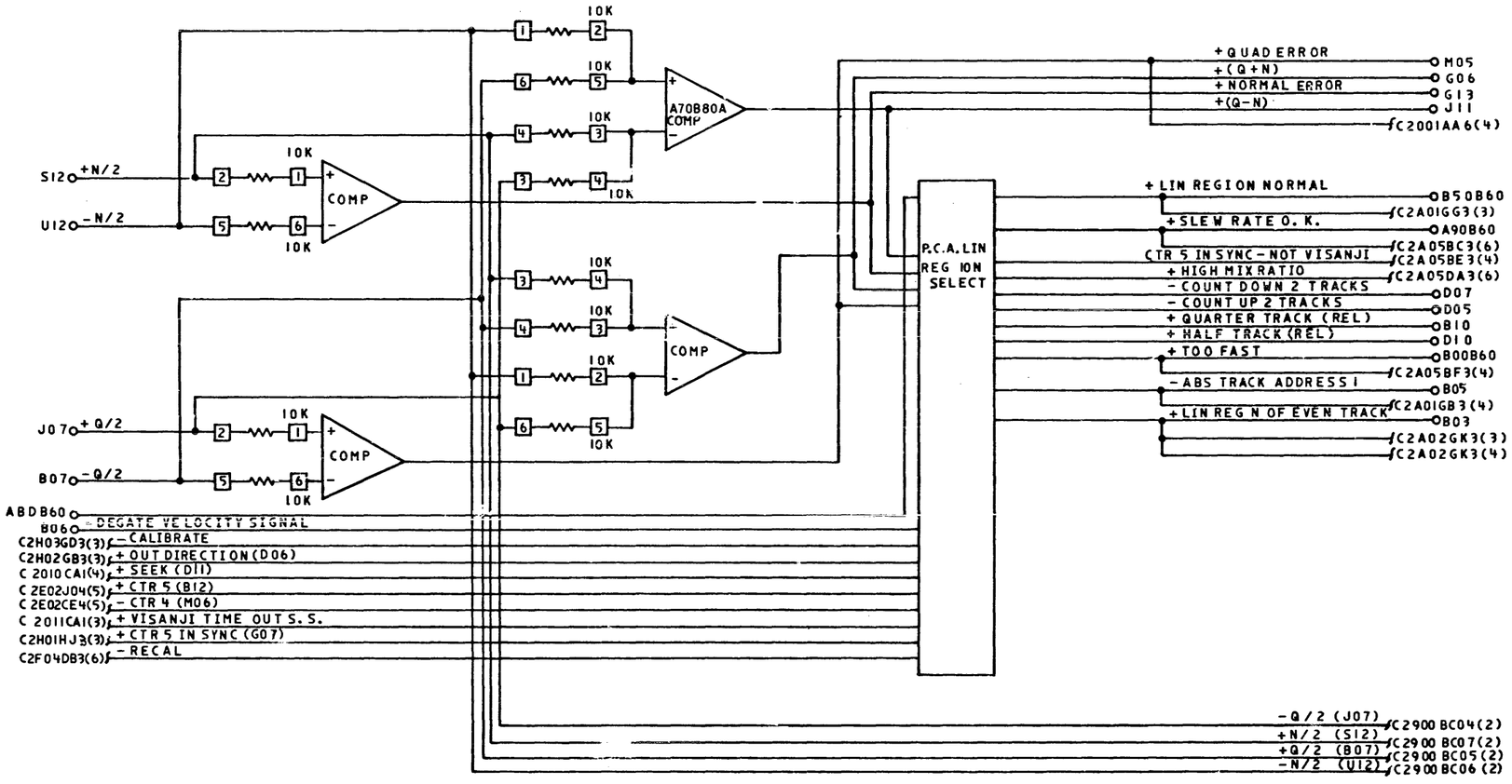
C

IBM CORP

SF559A

SF559A

SF560



POWER SUPPLIES

+5V D03, J03, P03, U03
GND D08, J08, P08, U08
-12V D12
+12V B11
+24V J02

EC HISTORY		DRAWING TITLE
20FEB79	375351	AID2 LOGIC 2
11 MAR 80	375662	MACH 4963
		PART NO 6839613
C		CLASSIFICATION

IBM CORP

SF560

SF560

SF561

B02 +DESIRED VELOCITY
D02 -HYBRID VELOCITY
B09 COIL CURRENT SIGNAL
C2Q03BD3(6) -HIGH MIX RATIO
100K
100K
N
136
1nF
1K
237
2.2nF
200K
PCA LIN REGULATOR SELECT
10K
1K
AMP
8K
6.2nF
11K
20K1%
+5V
200K
10nF
3K
3K
3K
10 F
COMP
PROG LINK
+HOLE IN PROFILE
J12
+HOLE IN PROFILE
A40B60
+BYTE COUNTER BIT 32
C2M02GG3(6)
HANDOVER VELOCITY
S03
30K
10nF
200K
10nF
2K
COMP
+(VEL>PROFILE)
B04
C2001AAB(3)
(S03)HANDOVER VELOCITY
C2005FD1(3)
C2900BC04(1) -Q/2
C2900BC05(1) +Q/2
2.49nF
2.49nF
11K
11K
H05
J06
COMP
J05
C2900BC06(1) -N/2
C2900BC07(1) +N/2
2.49nF
11K
11K
COMP
D03

SF561

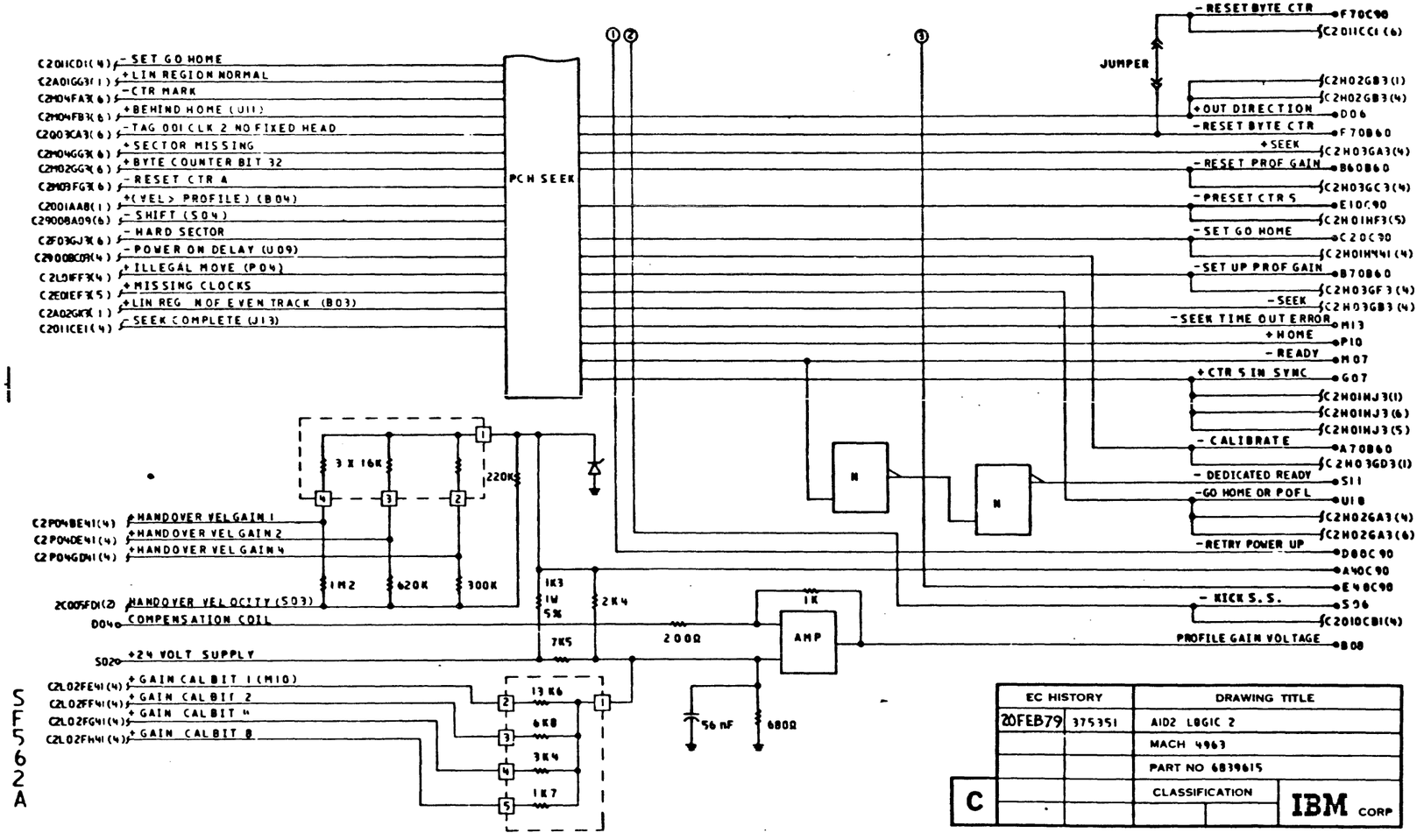
EC HISTORY		DRAWING TITLE
20FEB79	375351	AID2 LOGIC 2
		MACH 4963
		PART NO 6839614
		CLASSIFICATION

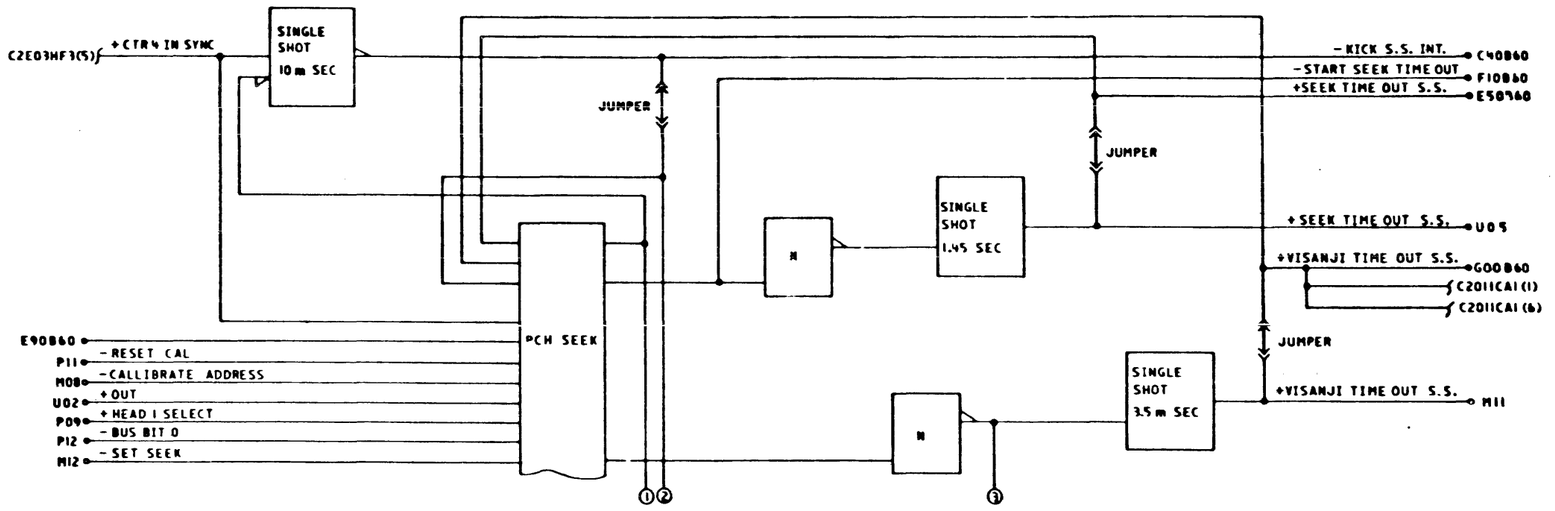
C

IBM CORP

SF561

SF562A


C2011CD1(4)
-SET GO HOME
C2A01GG3(1)
+LIN REGION NORMAL
C2M04FA3(6)
-CTR MARK
C2M04FB3(6)
+BEHIND HOME (U11)
C2Q03CA3(6)
-TAG 001 CLK 2 NO FIXED HEAD
C2M04GG3(6)
+SECTOR MISSING
C2M02GG3(6)
+BYTE COUNTER BIT 32
C2M03FG3(6)
-RESET CTR A
C2001AA8(1)
+(VEL> PROFILE) (B04)
C29008A09(6)
-SHIFT (S04)
C2F03GJ3(6)
-HARD SECTOR
C29008C09(4)
-POWER ON DELAY (U09)
C2L01FF3(4)
+ILLEGAL MOVE (P04)
C2E01EF3(5)
+MISSING CLOCKS
C2A02GK3(1)
+LIN REG NOF EVEN TRACK (B03)
C2011CE1(4)
-SEEK COMPLETE (J13)
PCH SEEK
JUMPER
-RESET BYTE CTR
F70C90
C2011CC1(6)
C2H02GB3(1)
C2H02GB3(4)
+OUT DIRECTION
D06
-RESET BYTE CTR
F70B60
+SEEK
C2H03GA3(4)
-RESET PROF GAIN
B60B60
C2H03GC3(4)
-PRESET CTR 5
E10C90
C2H01HF3(5)
-SET GO HOME
C20C90
C2H01HN41(4)
-SET UP PROF GAIN
B70B60
C2H03GF3(4)
-SEEK
C2H03GB3(4)
-SEEK TIME OUT ERROR
M13
+HOME
P10
-READY
M07
+CTR 5 IN SYNC
G07
C2H01HJ3(1)
C2H01HJ3(6)
C2H01HJ3(5)
-CALIBRATE
A70B60
C2H03GD3(1)
-DEDICATED READY
S11
-GO HOME OR POFL
U18
C2H02GA3(4)
C2H02GA3(6)
-RETRY POWER UP
D80C90
A40C90
E40C90
-KICK S.S.
S06
C2010CB1(4)
PROFILE GAIN VOLTAGE
B08
3 X 16K
220K
C2P04BE41(4)
+HANDOVER VEL GAIN 1
C2P04DE41(4)
+HANDOVER VEL GAIN 2
C2P04GD41(4)
+HANDOVER VEL GAIN 4
1M2
620K
300K
2C005FD1(2)
HANDOVER VELOCITY (S03)
D04
COMPENSATION COIL
S02
+24 VOLT SUPPLY
1K3
1W
5%
2K4
7K5
200Ω
1K
AMP
56 nF
680Ω
N
N
C2L02FE41(4)
+GAIN CAL BIT 1 (M10)
C2L02FF41(4)
+GAIN CAL BIT 2
C2L02FG41(4)
+GAIN CAL BIT 4
C2L02FH41(4)
+GAIN CAL BIT 8
13K6
6K8
3K4
1K7
SF562A
EC HISTORY
20FEB79
375351
DRAWING TITLE
AID2 LOGIC 2
MACH 4963
PART NO 6839615
CLASSIFICATION
C
IBM CORP
SF562A



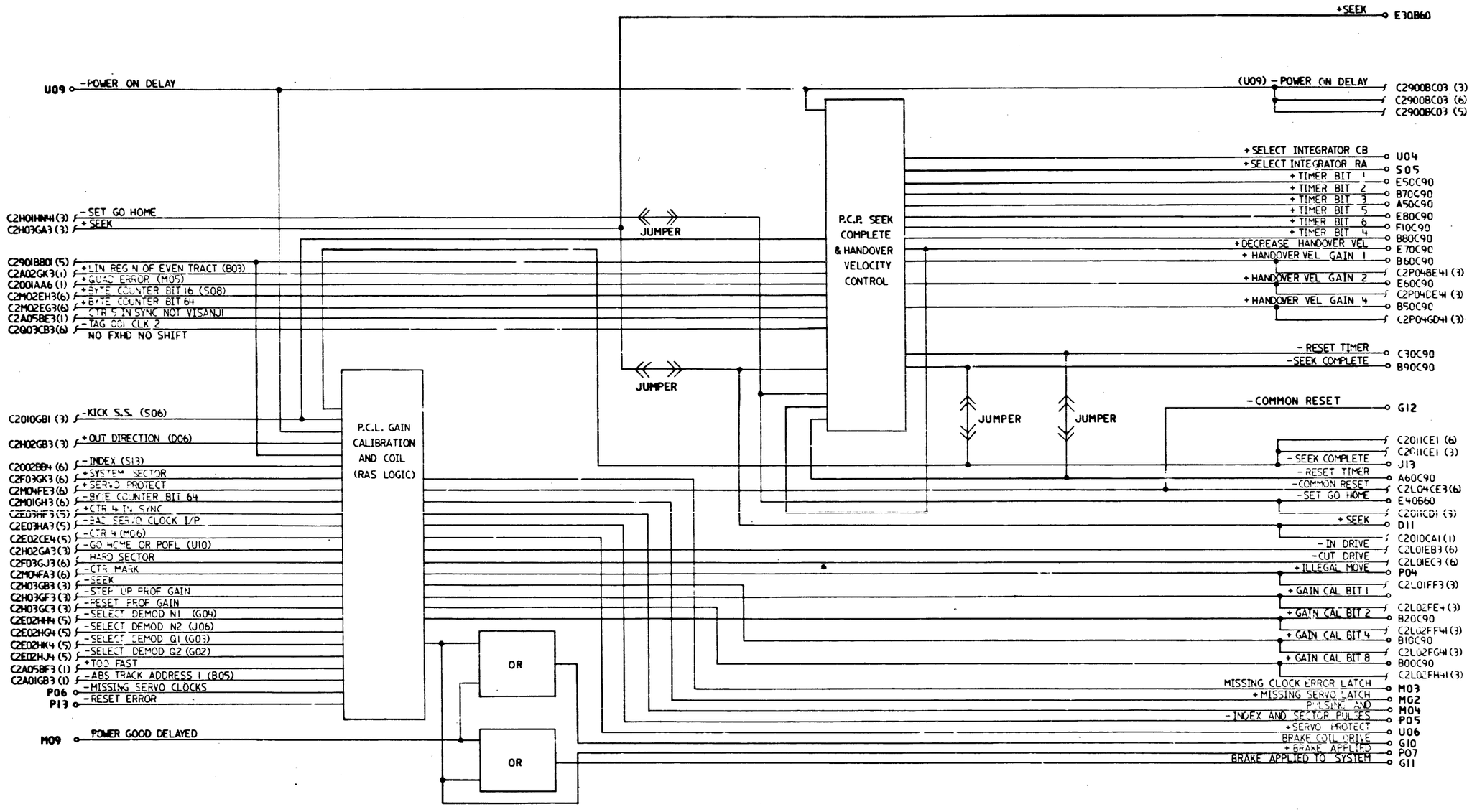
EC HISTORY		DRAWING TITLE
20FEB79	375351	AID2 LOGIC 2
		MACH 4963
		PART NO 6839616
		CLASSIFICATION

C

IBM CORP

SF562B

SF562B



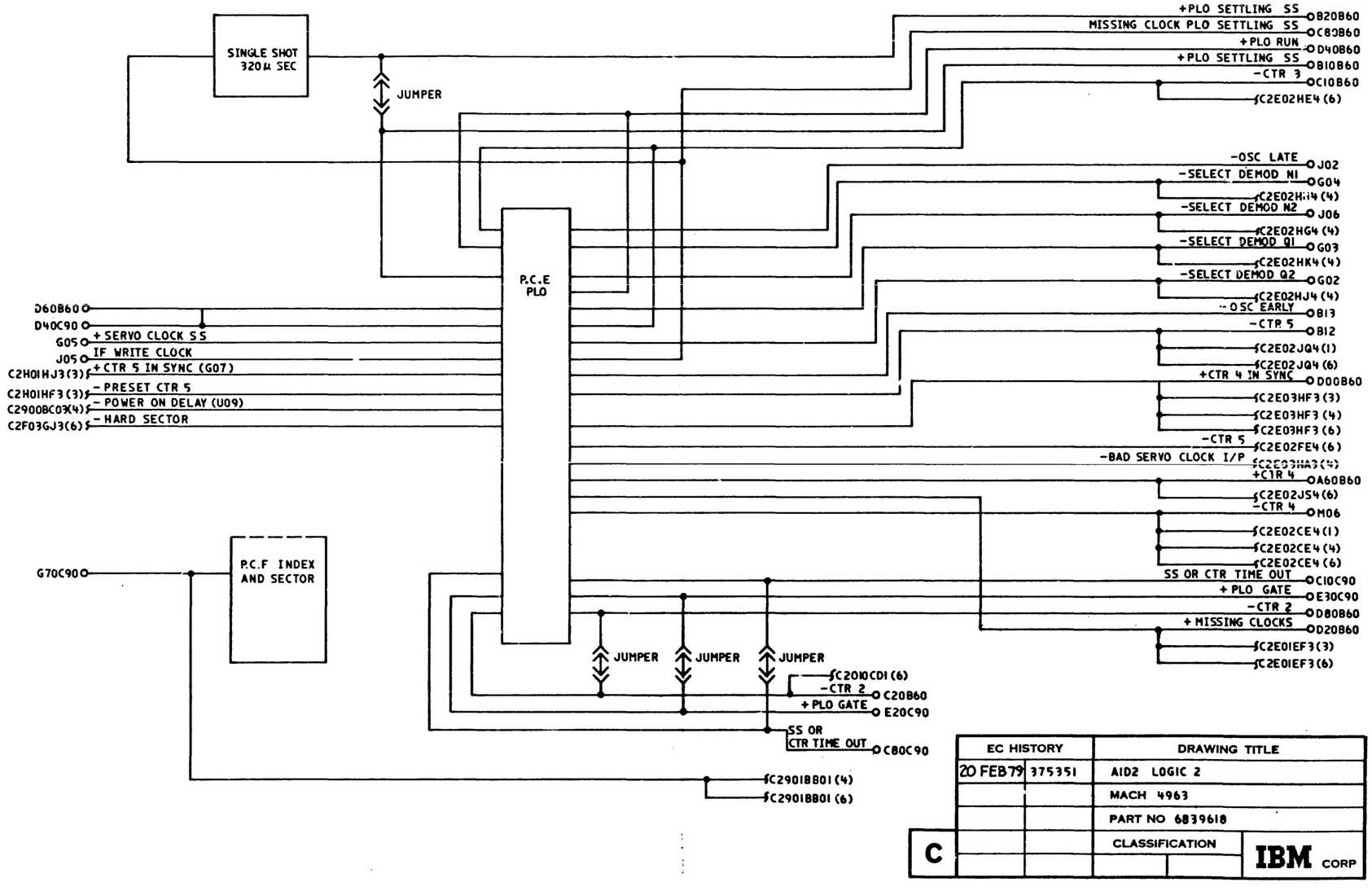
SF563

EC HISTORY		DRAWING TITLE
20FEB79	375351	AID2 LOGIC 2
		MACH 4963
		PART NO 6839617
D		CLASSIFICATION

IBM CORP

SF563

SF564



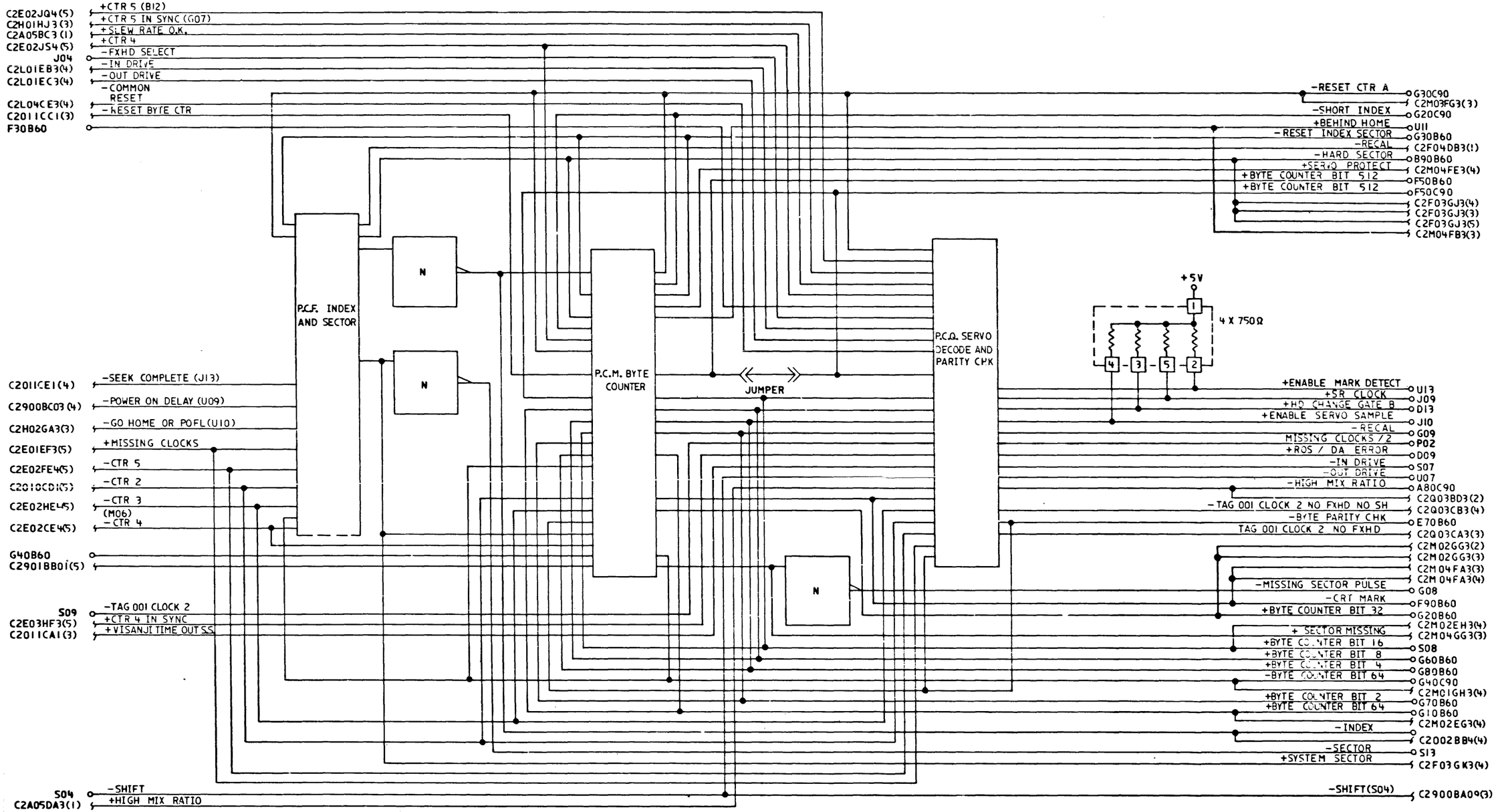
SF564

EC HISTORY		DRAWING TITLE
20 FEB 79	375351	AID2 LOGIC 2
		MACH 4963
		PART NO 6839618
		CLASSIFICATION

C

IBM CORP

SF564



SF565

EC HISTORY		DRAWING TITLE
20FEB79	375351	A1D2 LOGIC 2
		MACH 4963
		PART NO 6839619
		CLASSIFICATION

D

IBM CORP

SF565

SF566A

AID2 – LOGIC 2 – INPUT

	PIN	LINE NAME	SOURCE	PAGE
SF560	S12	+N/2	-F2D13	SF570
	U12	-N/2	-F2M08	SF570
	J07	+Q/2	-F2S02	SF570
	B07	-Q/2	-F2D11	SF570
	B06	-DEGATE VELOCITY SIG	-	TP
SF561	B02	+DESIRED VELOCITY	-C2D02	SF557
	D02	-HYBRID VELOCITY	-	TP
	B09	COIL CURRENT	-F2S10	SF570
	S03	HANDOVER VELOCITY	-	TP
SF562	P11	-RESET CALIBRATION	-C2D05	SF557
	M08	-CALIBRATE ADDRESS	-C2G05	SF557
	U02	+OUT	-C2J05	SF557
	P09	+HD SEC I	-C2M12	SF555
	P12	-BUS BIT 0	-C2G04	SF556
	M12	-SET SEEK	-C2S07	SF554
	D04	COMPENSATION COIL	-E4A14	
	S02	+24 VOLTS	-F2G02 (B5E14)(E5A14)	SF570
SF563	U09	-POWER ON DELAY	-F2P02 (C2S13)	SF570 (SF554)
	P06	-MISSING SERVO CLOCKS	-F2G13	SF570
	P13	-RESET ERROR	-A5D06 (C2S10)	SF503 (SF554)
	M09	POWER GOOD DELAYED	-F2P09	SF570
SF564	G05	+SERVO CLOCK S.S.	-F2B04	SF570
	J05	IF WRITE CLOCK	-B2U12	SF550
SF565	J04	-FIXED HEAD SELECT	-C2D09 (B2M05)(D1D13)	SF556 (SF550)
	S09	-TAG CLOCK 2	-C2D07	SF555
	S04	-SHIFT	-C2B13	SF557

AID2 – LOGIC 2 – OUTPUT

	PIN	LINE NAME	SYNC	PAGE
SF560	M05	+QUAD ERROR		TP
	G06	+(Q+N)		TP
	G13	+NORMAL ERROR	-F2B12	SF570
	J11	+(Q-N)		TP
	D07	-COUNT DN 2 TKS	-C2S05	SF555
	D05	-COUNT UP 2 TKS	-C2S06	SF555
	B10	+QUARTER TK	-C2D04	SF557
	D10	+HALF TRACK	-C2B04	SF557
	B05	-ABS TK ADDRESS !	-C2U06	SF555
	B03	+LIN REG N EVEN TK	-C2D11	SF556
SF561	J12	+HOLE IN PROFILE		TP
	B04	+(VEL> PROFILE)		TP
SF562	V05	+SEEK TIME OUT S.S.		
	M11	TIME OUT S.S.		
	D06	+OUT DIRECTION	-C2J07 (F2513)	SF556 (SF570)
	M13	-SEEK TIME OUT ERROR		TP
	P10	+HOME	-C2U07	SF555
	M07	-READY	-C2S08	SF555
	G07	+CTR 5 IN SYNC	-C2U10	SF555
	S11	-DEDICATED READY		TP
	U10	-GO HOME OR PRO	-C2B06	SF554
	S06	-KICK S.S.		TP
	B08	PROFILE GAIN VOLTAGE	-C2B02	SF557

SF566A

EC HISTORY		DRAWING TITLE
20FEB79	375351	AID2 LOGIC 2
11MAR80	375662	MACH 4963
		PART NO 6839620
C		CLASSIFICATION

IBM CORP

SF566A

AID2 – LOGIC 2 – OUTPUT

PIN	LINE NAME	SYNC	PAGE
SF563 U04	+SEL INTEG CB	F2P07	SF570
S05	+SEL INTEG RA	F2P05	SF570
G12	– COMMON RESET		TP
J13	– SEEK COMPLETE	C2P11 (F2S07)	SF556 (SF570)
D11	+SEEK	F2S08	SF570
P04	+ILLEGAL MOVE	C2U05	SF555
M10	+GAIN CAL BIT 1		TP
M03	– MISSING CLK ERROR LATCH	C2J09	SF556
M02	+MISS SERVO LATCH	C2S02	SF556
M04	PULSING AND	C2M10	SF556
P05	– INDEX AND SECTOR	C2G08	SF556
U06	+SERVO PROTECT	C2G10	SF554
G10	+BRAKE COIL DRIVE	B3A14	SF
P07	+BRAKE APPLIED	F2M02 (C2B08)	SF570 (SF554)
G11	+BRAKE APPLIED TO SYS	B5A14	SF545
SF564 J02	– OSC LATE	E2J07	TP
G04	– SEL DEMOD N1	F2D09	SF570
J06	– SEL DEMOD N2	F2B10	SF570
G03	– SEL DEMOD Q1	F2B08	SF570
G02	– SEL DEMOD Q2	F2B09	SF570
B13	– OSC EARLY	E2G07	SF568
B12	+ CTR 5		TP
M06	– CTR 4		TP

AID2 – LOGIC 2 – OUTPUT

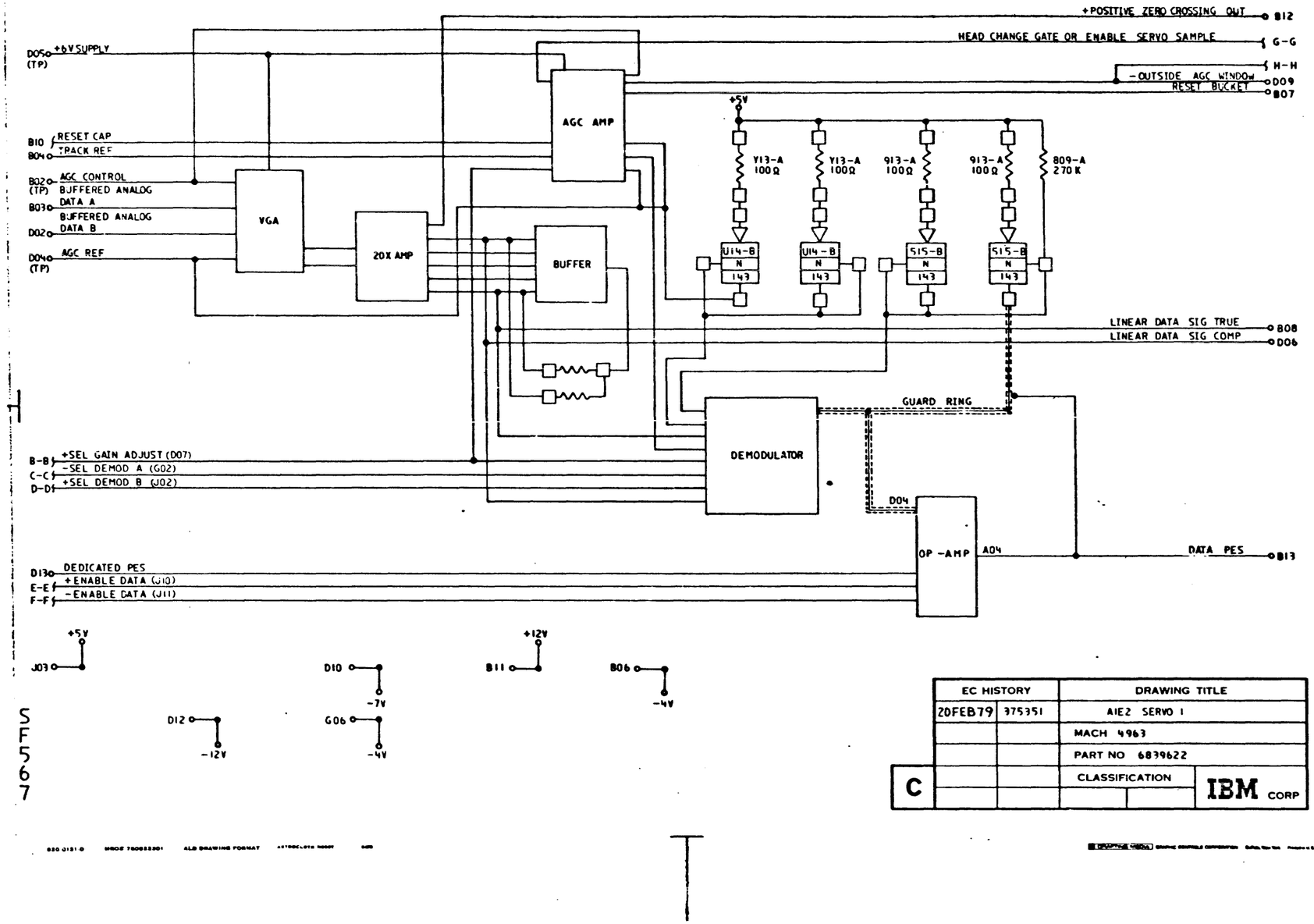
PIN	LINE NAME	SYNC	PAGE
SF565 U11	+BEHIND HOME	C2D13	SF556
U13	DETECT	E2G04	SF568
J09	SR CLOCK	E2G10	SF568
D13	+HD CHANGE GATE	E2D11	SF568
J10	+ENABLE SERVO SPL	E2J04	SF568
G09	–RECAL	C2J02 (B2P04)	SF567 (SF551)
P02	MISSING CLOCKS/2	C2B10	SF556
D09	+ROS/DA ERROR	C2U04	SF555
S07	– IN DRIVE	F2P11 (C2M13)	SF570 (SF556)
U07	– OUT DRIVE	F2M13 (C2U02)	SF570 (SF556)
G08	– MISSING SECTOR PULSE	A5B09	SF503
S08	+BYTE COUNTER BIT 16	C2U03	SF559A
S13	– INDEX	A5D07 (F1A11)	SF503
S10	– SECTOR	A5B05	SF503

SF566B

EC HISTORY		DRAWING TITLE
20FEB79	375351	AID2 LOGIC 2
11 MAR 80	375662	MACH 4963
		PART NO 6839621
C		CLASSIFICATION
		IBM CORP

SF566B

SF567



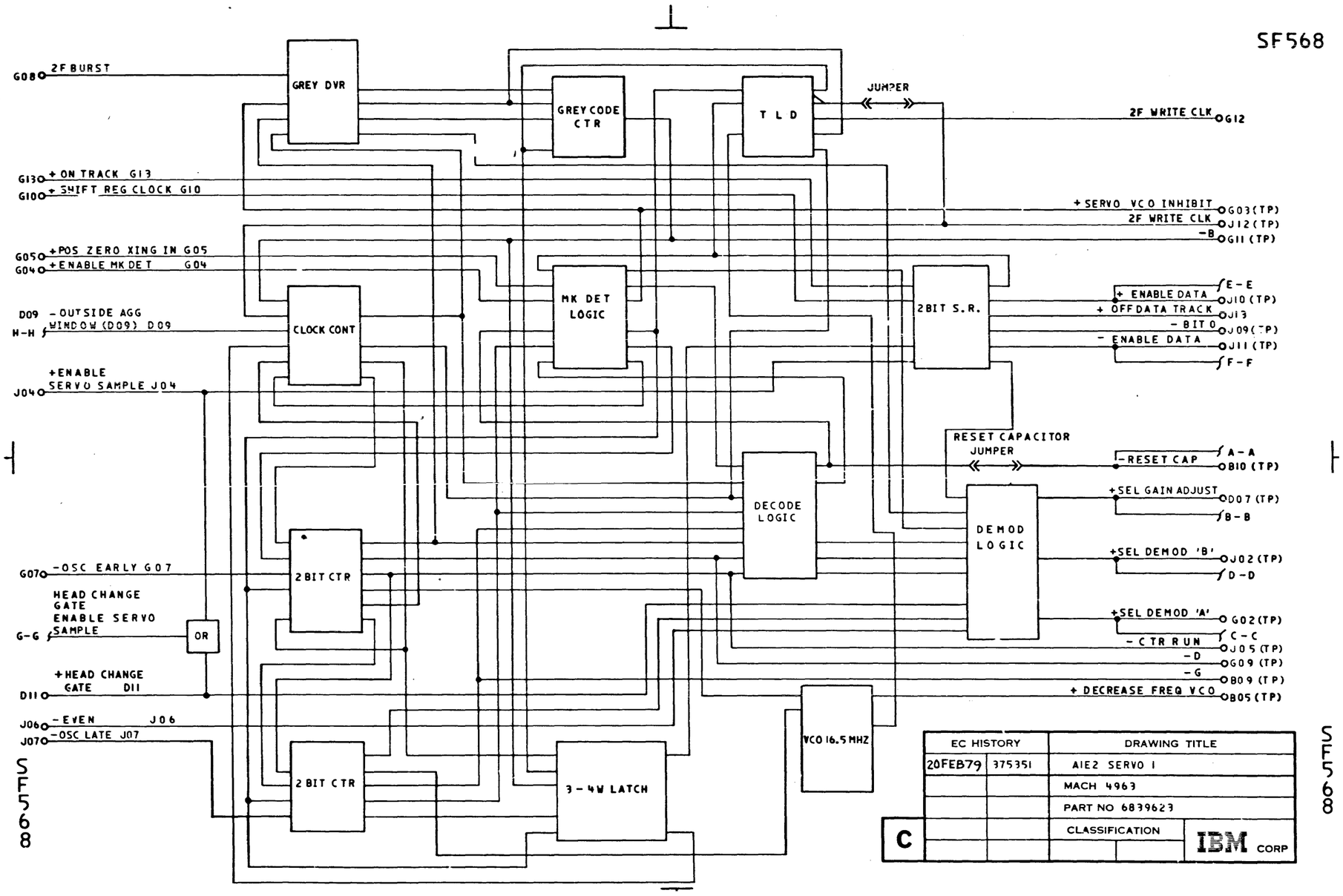
SF567

EC HISTORY		DRAWING TITLE
20FEB79	375351	AIE2 SERVO 1
		MACH 4963
		PART NO 6839622
C		CLASSIFICATION

IBM CORP

SF567

SF568



EC HISTORY		DRAWING TITLE
20FEB79	375351	AIE2 SERVO I
		MACH 4963
		PART NO 6839623
		CLASSIFICATION

C

IBM CORP

AIE2 - SERVO 1 - INPUT

PIN	LINE NAME	SOURCE	PAGE
SF567 B10	RESET CAP		
B04	TRACK REF	F2B07	SF570
B03	BUFFERED DATA A	B2B02	SF551
D02	BUFFERED DATA B	B2B03	SF551
D07	+SEL GAIN ADJUST		TP
G02	+SEL DEMODE A		TP
J02	+SEL DEMODE B		TP
D13	DEDICATED PES	F2D02	SF570
J10	+ENABLE DATA		TP
J11	-ENABLE DATA		TP
SF568 G08	2F BURST	B2P11	SF552
G13	+ON TRACK	C2B12 (F2G12)	SF556 (SF570)
G10	+SHIFT REG CLOCK	D2J09	SF556
G05	+POS ZERO XING	E2B12	SF567
G04	+ENABLE MARK DETECT	D2U13	SF565
D09	-OUT AGC WINDOW	C2G03	SF556
J04	+ENABLE SERVO SPL	D2J10	SF565
G07	-OSC EARLY	D2B13	SF564
D11	+HEAD CHANGE GATE	D2D13	SF565
J06	-EVEN	F2B03 (C2S09)	SF570 (SF554)
J07	-OSC LATE	D2J02	SF564

AIE2 - SERVO 1 - OUTPUT

PIN	LINE NAME	SYNC	PAGE
SF567 B12	+POS ZERO XING	E2G05	SF568
D09	-OUT AGC WINDOW	C2G03	SF556
B07	RESET BUCKET		TP
B08	LINEAR DATA TRUE		TP
D06	LINEAR DATA COMP		TP
B13	DATA PES	F2P06	SF570
SF568 G12	2F WRITE CLOCK	B2M10	SF551
G03	+SERVO INHIBIT	B2U06	SF552
J13	+OFF DATA TRACK	C2G13	SF554

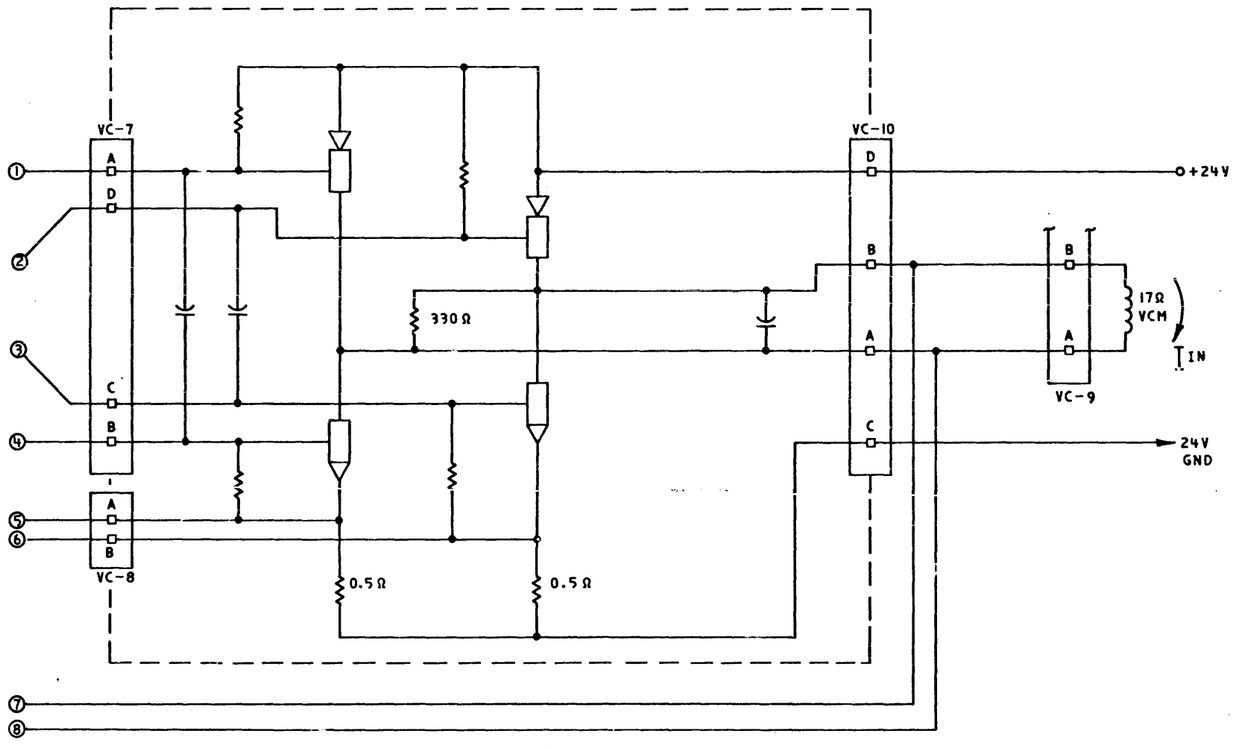
SF569

EC HISTORY		DRAWING TITLE
20FEB79	375351	AIE2 SERVO 1
		MACH 4963
		PART NO 5839624
C		CLASSIFICATION

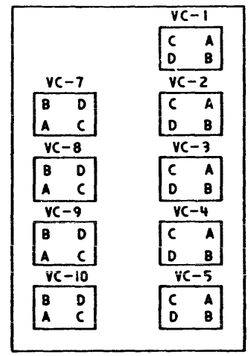
IBM CORP

SF569

SF570A



ACTIVATOR DRIVER CARD



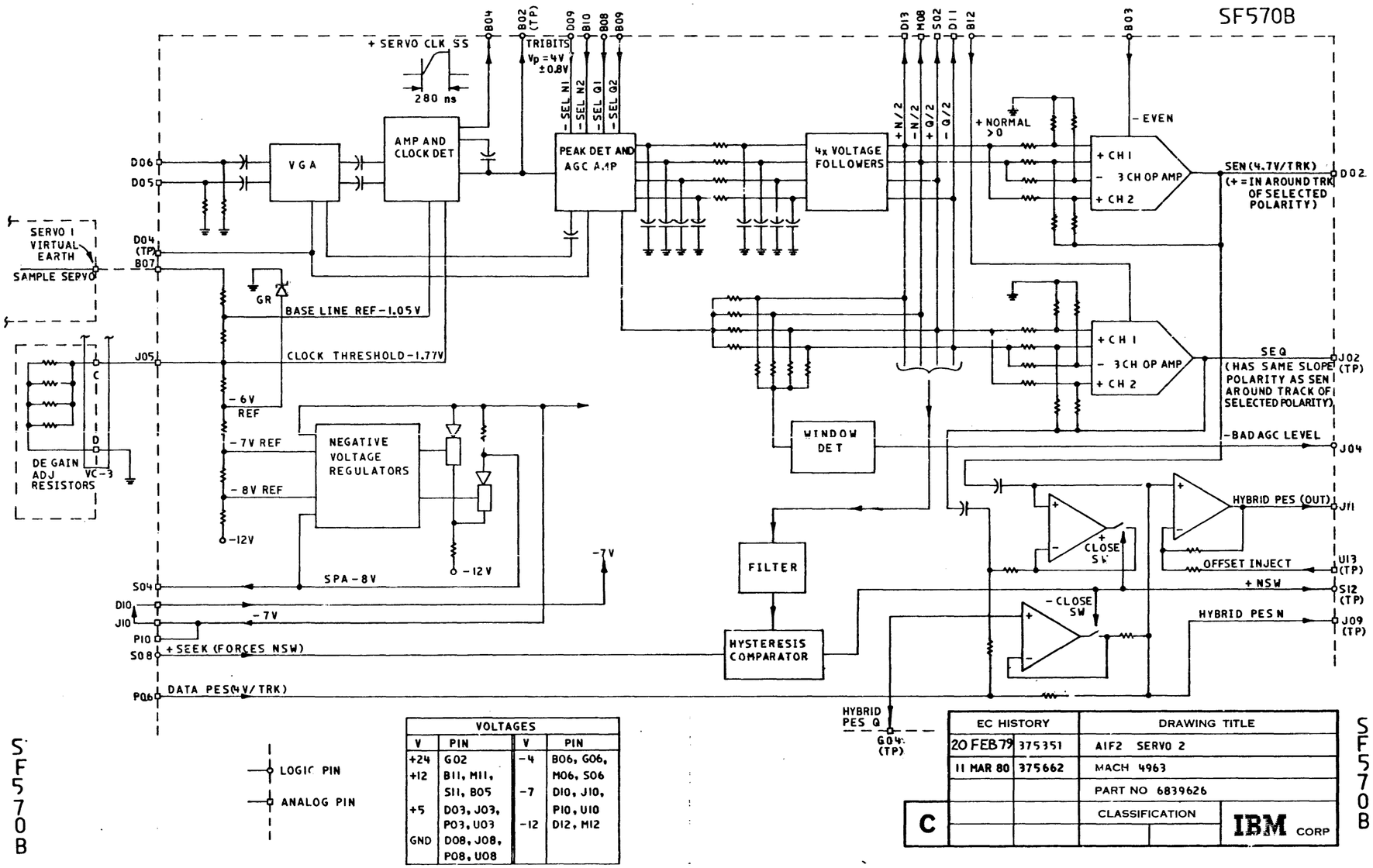
BOARD SHOWING
VOLTAGE CROSSOVERS

EC HISTORY		DRAWING TITLE	
20 FEB79	375351	ACTIVATOR DRIVER CARD	
11 MAR 80	375662	MACH 4963	
		PART NO 6839625	
C		CLASSIFICATION	IBM CORP

SF570A

SF570A

SF570B



VOLTAGES			
V	PIN	V	PIN
+24	G02	-4	B06, G06, M06, S06
+12	B11, M11, S11, B05	-7	D10, J10, P10, U10
+5	D03, J03, P03, U03	-12	D12, M12
GND	D08, J08, P08, U08		

LOGIC PIN

ANALOG PIN

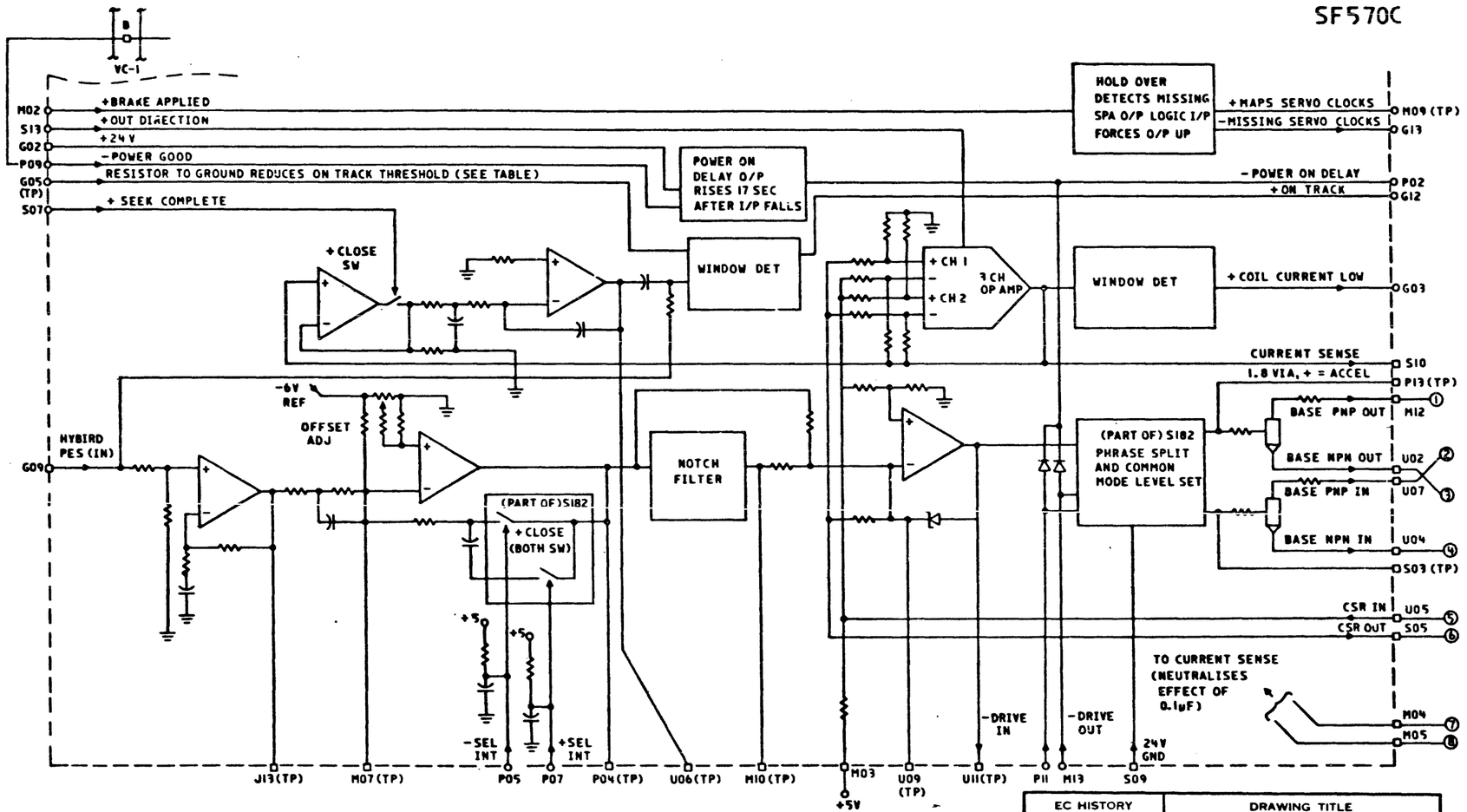
EC HISTORY		DRAWING TITLE
20 FEB 79	375351	AIF2 SERVO 2
11 MAR 80	375662	MACH 4963
		PART NO 6839626
		CLASSIFICATION

C

IBM CORP

SF570B

SF570C



ON TRK THRESHOLD	
G05 R	% TRK DC
∞	12 %
25.5 K	10%
10.2 K	8%
5.1 K	6%

EC HISTORY		DRAWING TITLE
20FEB79	375351	A1F2 SERVO 2
		MACH 4963
		PART NO 6639627
		CLASSIFICATION

C

IBM CORP

SF570C

SF570C

AIF2 – SERVO 2 – INPUT

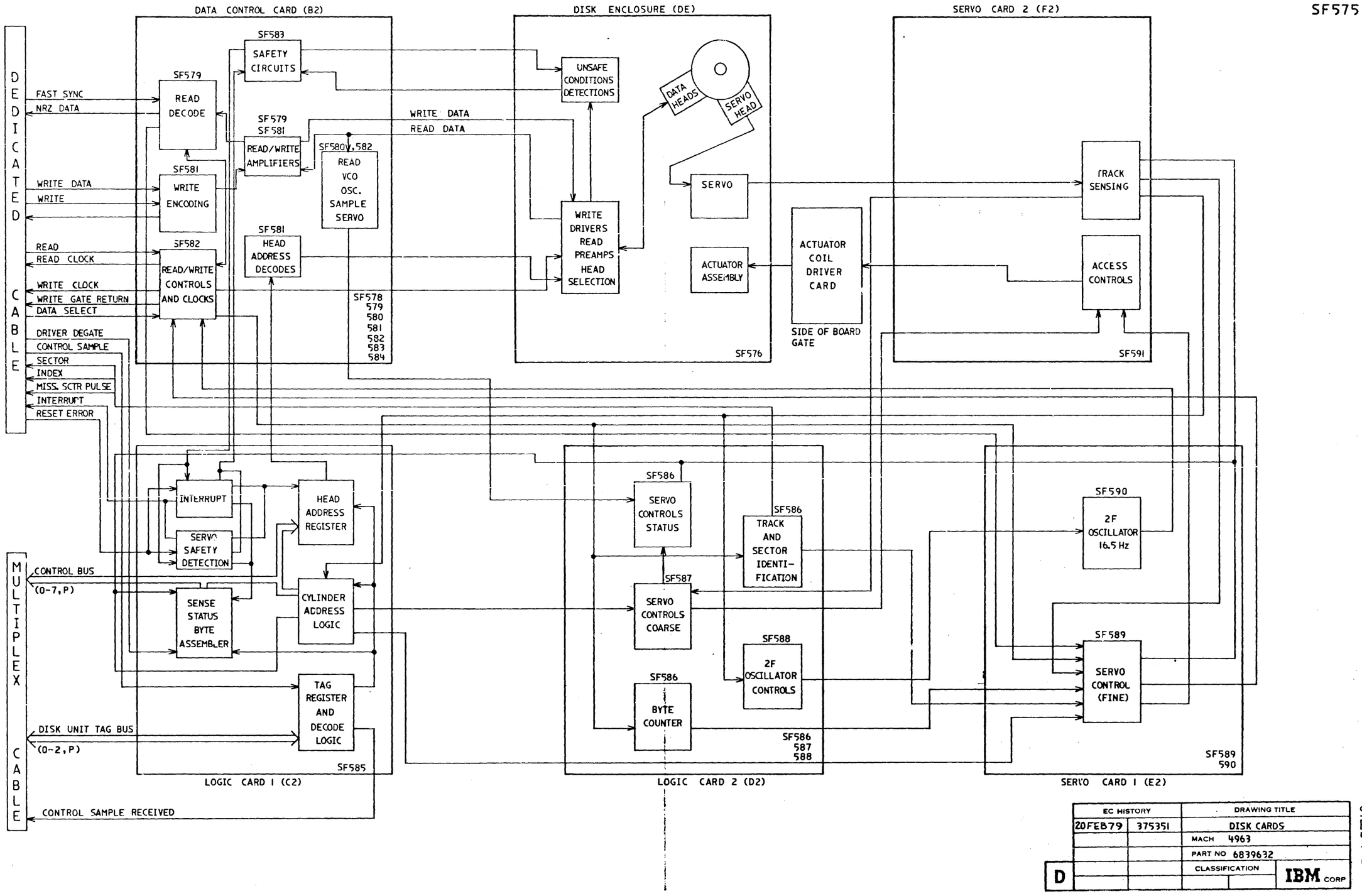
PIN	LINE NAME	SOURCE	PAGE
SF570 B03	– EVEN	E2J06 (C2509)	SF568 (SF554)
B12	+ NORMAL	D2G13	SF560
B09	– SEL Q2	D2G02	SF564
B08	– SEL Q1	D2G03	SF564
B10	– SEL N2	D2J06	SF564
D09	– SEL N1	D2G04	SF564
D06	SERVO OUTPUT	A2D10	SF527
D05	SERVO OUTPUT	A2D11	SF527
B07	SAMPLE SERVO	E2B04	SF567
J05	DE GAIN	B3E14 (D1C13)	SF510
D10	–7 VOLTS	F2U10 (F2J10)(F2D10)(E2D10)	SF570 (SF545)
S08	+SEEK	D2D11	SF563
P06	DATA PES	E2B13	SF567
M02	+ BRAKE APPLIED	D2P07 (C2B08)	SF563 (SF554)
S13	+ OUT DIRECTION	D2D06 (C2J07)	SF562 (SF556)
G02	+12 VOLTS	E5A14 (D2S02) (B5E14)	SF545 (SF562)
P09	– POWER GOOD	D2M09	SF563
S07	+ SEEK COMPLETE	C2P11 (D2J13)	SF556 (SF563)
G09	HYBRID PES	F2J11 (D1E13)	SF570
P05	– SEL INT	D2S05	SF563
P07	+SEL INT	D2U04	SF563
P11	– DRIVE IN	D2S07 (C2M13)	SF565 (SF556)
M13	– DRIVE OUT	D2U07 (C2U02)	SF565 (SF556)
S09	+24 VOLT GND	B6E01 (E6A01)	SF545
G10	–POWER GOOD	VC–1–B	SF545

AIF2 – SERVO 2 – OUTPUT

PIN	LINE NAME	SYNC	PAGE
SF570 D02	SENSE	E2D13	SF567
J04	– BAD AGC	C2U11	SF555
J11	HYBRID PES	F2G09 (D1E13)	SF570 (SF510)
G13	– MISS SERVO CLKS	D2P06	SF562
P02	– POWER ON DELAY	D2U09 (C2S13)	SF563 (SF565)
G03	+COIL CURRENT LOW	C2G07	SF556
S10	CURRENT SENSOR	D2B09	SF561
B04	+SERVO CLK S.S.	D2G05	SF564
D13	+N/2	D2S12	SF560
M08	–N/2	D2U12	SF560
S02	+Q/2	D2J07	SF560
D11	–Q/2	D2B07	SF560
S04	SPA	A2D09 (A2D13) A2B10 (A2B12)	SF527
G12	+ON TRACK	C2B12, E2G13, T2D06	
U04	BASE NPN IN	ACT DR CARD	

EC HISTORY		DRAWING TITLE
20FEB79	375351	AIF2 SERVO 2
11 MAR 80	375662	MACH 4963
		PART NO 6839628
C		CLASSIFICATION
		IBM CORP

SF571



SF575

EC HISTORY		DRAWING TITLE
20FEB79	375351	DISK CARDS
		MACH 4963
		PART NO 6839632
		CLASSIFICATION

D

IBM CORP

SF575

DISK ENCLOSURE CONTROLS

THE FOLLOWING CIRCUITS ARE CONTAINED IN THE DE: READ/WRITE SELECTION CIRCUITS FOR WRITE DRIVERS AND READ PRE-AMPLIFIERS, HEAD SELECTION LOGIC, AND DETECTION FOR UNSAFE LOGIC.

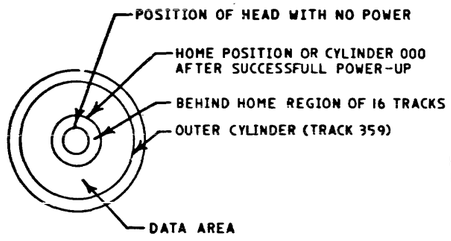
READ/WRITE SELECTION

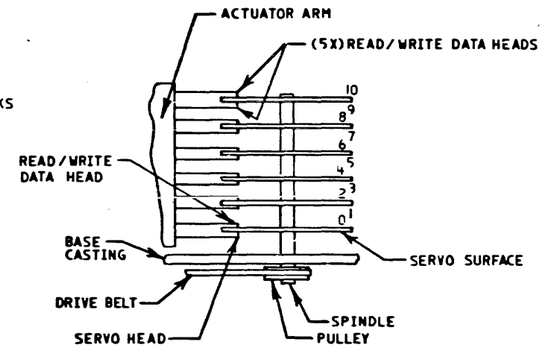
READ AND WRITE MODE SELECTION IS CONTROLLED BY THE 'CENTER TAP' LINE; THIS LINE IS CONNECTED TO THE WRITE DRIVERS AND THE READ PRE-AMPLIFIERS.

IN THE WRITE MODE, THE 'CENTER TAP' LINE IS RAISED TO A POSITIVE-VOLTAGE LEVEL, AND, WHEN 'WRITE GATE' AND 'NOT WRITE BLOCK' ARE APPLIED, WRITE CURRENT IS FED THROUGH THE HEAD.

IN THE READ MODE, THE 'CENTER TAP' LINE IS GROUNDED; THIS SELECTS THE READ CIRCUITS IN THE DE.

PART OF THE CENTER TAP CIRCUIT ACTS AS A CURRENT LIMITER THAT LIMITS THE CENTER-TAP CURRENT TO A SAFE LEVEL.





HEAD SELECTION LOGIC

HEADS ARE SELECTED BY A 5-BIT SELECTION CODE PROVIDED BY THE SYSTEM. THIS CODE, HELD IN A REGISTER IN THE DSD, IS CONVERTED INTO CONTROL SIGNALS THAT SELECT CORRESPONDING COMBINATIONS OF MOVING AND FIXED HEADS.

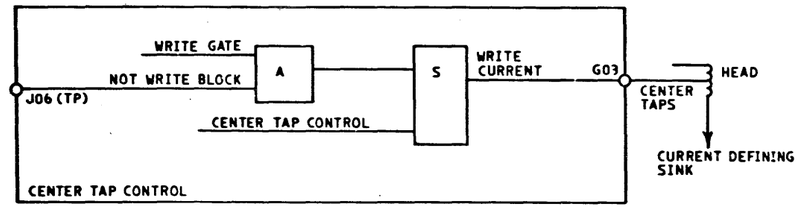
THE MAXIMUM NUMBER OF HEADS FOR WHICH SELECTION IS PROVIDED IN DES WITH FIXED HEADS, IS TEN MOVING HEADS WITH EIGHT FIXED HEADS.

IN DES WITH MOVING HEADS ONLY, THE MAXIMUM FOR WHICH SELECTION IS PROVIDED IS 11 MOVING HEADS.

HEAD SELECTION DECODE

THE SYSTEM CODES FOR SELECTION OF THE APPROPRIATE HEADS ARE GIVEN IN THE TABLE.

WRITE MODE



HEAD SELECT CODE (FROM SYSTEM)	HEAD SELECTED	OUTPUT LINES SELECTED		
		CHIP SELECTS 1 2 3 4 5	HEAD SELECTS A	B
MOVING HEADS:				
00000	0	1 0 0 0 0	0	0
00001	1	1 0 0 0 0	1	0
00010	2	1 0 0 0 0	0	1
00011	3	1 0 0 0 0	1	1
00100	4	0 1 0 0 0	0	0
00101	5	0 1 0 0 0	1	0
00110	6	0 1 0 0 0	0	1
00111	7	0 1 0 0 0	1	1
01000	8	0 0 1 0 0	0	0
01001	9	0 0 1 0 0	1	0
01010	10	0 0 1 0 0	0	1
01011	11*	0 0 1 0 0	1	1
FIXED HEADS:				
10000	0	0 0 0 1 0	0	0
10001	1	0 0 0 1 0	1	0
10010	2	0 0 0 1 0	0	1
10011	3	0 0 0 1 0	1	1
10100	4	0 0 0 0 1	0	0
10101	5	0 0 0 0 1	1	0
10110	6	0 0 0 0 1	0	1
10111	7	0 0 0 0 1	1	1

*NO PHYSICAL HEAD 11 EXISTS BUT A HEAD POSITION 11 IS A SPARE INPUT ON THE DSD ACTUATOR. THE CODE FOR HEAD 11 IS FORCED WHEN AN 'UNSAFE' CONDITION IS DETECTED.

EC HISTORY		DRAWING TITLE
20FEB79	375351	DISK ENCLOSURE
		MACH 4963
		PART NO 6839633
		CLASSIFICATION

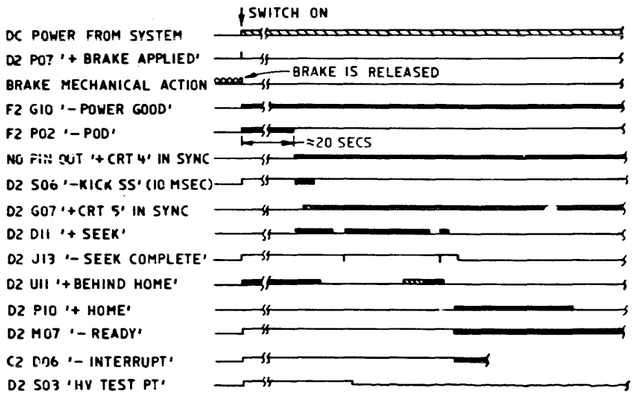
C

IBM CORP

SF576

SF577

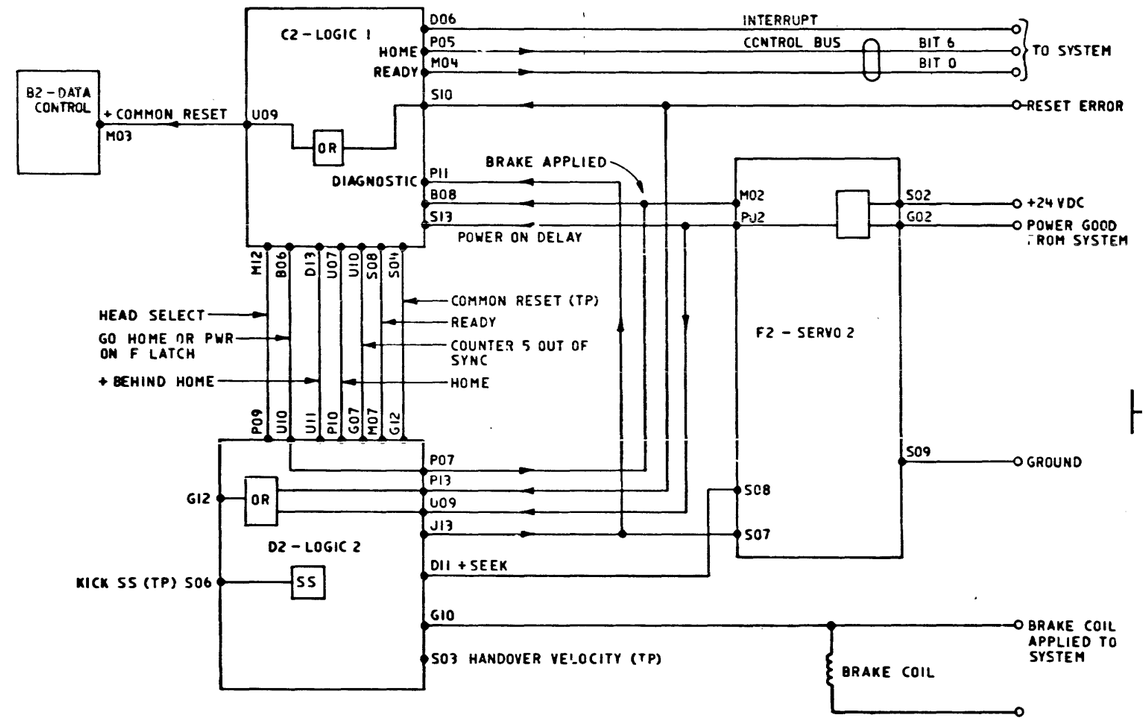
POWER ON LOGIC SEQUENCE TIMING



NOTE: THIS CHART INDICATES THE CORRECT SEQUENCE OF EVENTS. ACTUAL TIMES AND WAVE FORMS WILL VARY FROM SYSTEM TO SYSTEM.

POWER ON LOGIC SEQUENCE

1. AC AND DC POWER ARE APPLIED TO THE DSD.
2. 'BRAKE APPLIED' REMAINS ESSENTIALLY NEGATIVE TO PROVIDE RETURN PATH FOR BRAKE CURRENT WHICH RETRACTS THE BRAKE AND ALLOWS THE SPINDLE TO ACCELERATE.
3. '–PWR GOOD' IS RAISED BY THE USING SYSTEM WHEN DC VOLTAGES ARE WITHIN TOLERANCE.
4. '–POD' BECOMES ACTIVE FOR APPROXIMATELY 20 SECONDS TO ALLOW THE DISK SPEED TO STABILIZE AT 3125 RPM.
5. 'CTR 4' COMES INTO SYNCHRONIZATION AFTER '–POD TIMES OUT' AND FIRES THE 'KICK SS'. IF 'CTR 4' FAILS TO COME INTO SYNC BEFORE '–POD' AND 'PLO HOLDOVER SS' TIMES OUT, THEN BRAKE APPLIED WILL BE RAISED, THE BRAKE WILL ACTIVATE AND 'BRAKE APPLIED' TO SYSTEM WILL BE RAISED. AC AND DC POWER WILL THEN BE SWITCHED OFF WITHIN 5 SECONDS.
6. '–KICK SS' APPLIES MAXIMUM ACCELERATION TO THE ACTUATOR ARM FOR 10 MILLISCEONDS TO MOVE THE ACTUATOR ARM INTO THE DATA AREA.
7. DURING THE INITIAL ACCESS MOVEMENT 'CTR 5' COMES INTO SYNCHRONIZATION.
8. '+ SEEK' IS RAISED WITH THE 'KICK SS' CYCLE AND IS LOWERED WHEN THE ACTUATOR COMES TO REST.
9. '– SEEK COMPLETE' INITIATES A 'RECALIBRATE' CYCLE.
10. AT THE COMPLETION OF THE RECALIBRATE CYCLE 'HOME' AND 'READY' BECOME ACTIVE AND AN INTERRUPT IS RAISED.
11. DURING THIS RECALIBRATE CYCLE, 'HANDOVER VELOCITY (HV)' IS CALIBRATED. THIS IS AN ANALOG VOLTAGE THAT SHOULD SET TO A SIMILAR LEVEL EACH TIME THE DSD IS POWERED UP. THIS LEVEL WILL HOWEVER VARY FROM DSD TO DSD.



EC HISTORY		DRAWING TITLE
20FEB79	375351	POWER ON SEQ
		MACH 4963
		PART NO 6839634
		CLASSIFICATION

C

IBM CORP

SF577

SF577

DATA CONTROL (B2 CARD)

INTRODUCTION

THE DATA CONTROL OPERATIONS OF THE DU ARE CONTROLLED BY LOGIC CONTAINED ON ONE CARD. THIS LOGIC CONTROLS THE WRITING OF DATA ONTO THE DISKS AND THE READING OF THAT DATA WHEN READ COMMANDS ARE ISSUED BY THE SYSTEM.

THE DATA CONTROL CARD INTERFACES WITH THE SYSTEM DIRECTLY, FOR THE TRANSFER OF DATA AND TO EFFECT SOME CONTROL SIGNALS. THE REMAINING CONTROL SIGNALS ARE HANDLED ON OTHER CARDS. THE DATA CONTROL CARD ALSO PRODUCES SIGNALS USED IN THE SERVO CONTROL CIRCUITS.

THE DATA CONTROL INCLUDES THE FOLLOWING ANALOG AND DIGITAL CIRCUITS:

- MODE CONTROL LOGIC
- READ DATA (PAGE SF579)
- READ DATA SEPARATION (PAGE SF584)
- DATA CONTROL SAMPLE SERVO CONTROL (PAGE SF580)
- WRITE DATA (PAGE SF581)
- WRITE SAFETY DETECTION (PAGE SF583)
- DISK ENCLOSURE CONTROLS (PAGE SF576)
- VOLTAGE CONTROLLED OSCILLATOR CONTROL (PAGE SF582)

MODE CONTROL LOGIC

THREE SIGNALS, ONE GENERATED IN THE DU AND THE OTHER TWO PROVIDED BY THE SYSTEM, CONTROL THE MODE OF OPERATION:
- '+ DATA SELECT GATED' (GENERATED ON LOGIC 1, C2 CARD)
- '+ WRITE SELECT'
- '+ READ SELECT'

+ DATA SELECT GATED

THIS SIGNAL GATES THE FOLLOWING SIGNALS TO THE SYSTEM WHEN IT IS APPLIED TO THE LINE DRIVER CIRCUITS:

- '1F WRITE CLOCK' (CARD PIN B2U11)
- '1F READ CLOCK' (CARD PIN B2U07)
- 'NRZ DATA (CARD PIN B2S07)

A FURTHER DRIVER (IN THE WRITE LINE DRIVER), USED ONLY AS AN MST TO VTL LEVEL CONVERTER, PROVIDES UNGATED '1F WRITE CLOCK' SIGNALS TO OTHER CARDS IN THE DSD (DATA STORE).

+READ SELECT

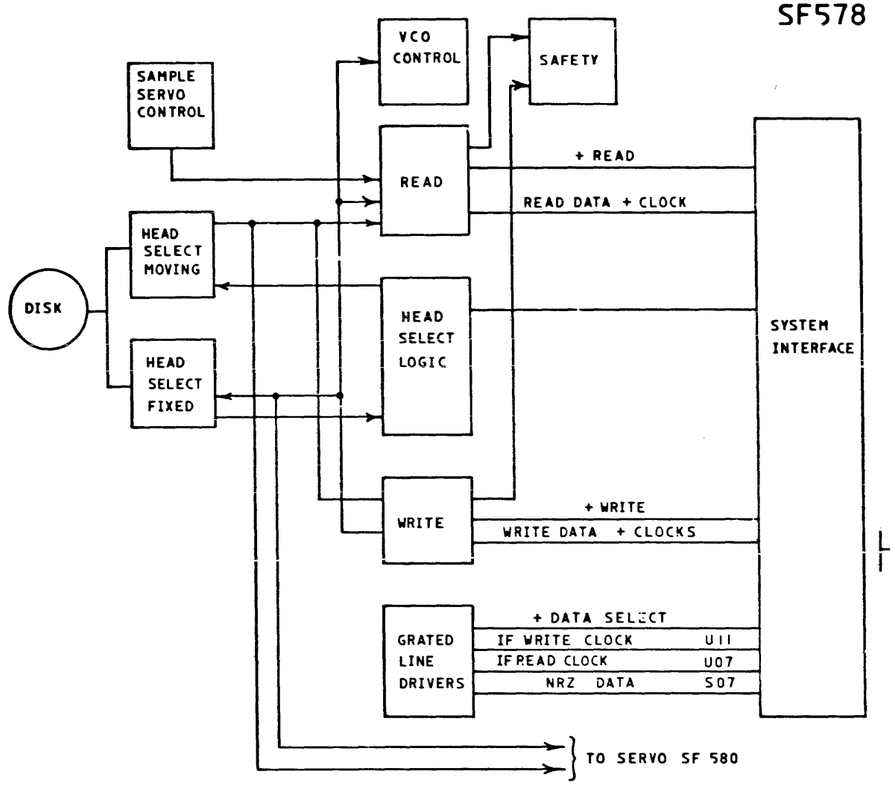
OPERATIONS EFFECTED WHEN '+ READ SELECT' IS ACTIVATED ARE DESCRIBED IN "READ DATA", ON PAGE SF582

+ WRITE SELECT

OPERATIONS EFFECTED WHEN '+ WRITE SELECT' IS ACTIVATED ARE DESCRIBED IN "WRITE DATA", ON PAGE SF581.

SF578

SF578



EC HISTORY		DRAWING TITLE
20FEB79	375351	A1B2 DATA CONTROL
		MACH 4963
		PART NO 6839635
C		CLASSIFICATION

IBM CORP

SF578

DATA CONTROL (B2 CARD) (CONTINUED)

READ DATA

CIRCUIT DESCRIPTION

DATA READ FROM THE DISKS CAUSE EACH SELECTED HEAD TO GIVE ANALOG OUTPUT SIGNALS OF LESS THAN 1 MILLIVOLT. THESE SIGNALS ARE AMPLIFIED AND DIFFERENTIATED SO THAT CORRESPONDING DIGITAL DATA CAN BE PRODUCED TO BE USED BY THE SYSTEM.

THE DATA SIGNALS FROM THE MOVING AND FIXED HEADS ARE AMPLIFIED AND ROUTED THROUGH A LOW-PASS FILTER TO A VARIABLE-GAIN AMPLIFIER (VGA) AND TO THE SERVO CONTROL CIRCUIT. TWO AC-COUPLED INPUTS ARE APPLIED TO THE VGA; BOTH PRODUCE DIFFERENTIAL AC CURRENTS IN THE VGA. ONE OF THESE INPUTS IS SET WITH RESPECT TO A REFERENCE VOLTAGE AND THE OTHER HAS A GAIN CONTROL VOLTAGE APPLIED TO IT. THE SIGNAL CURRENTS PRODUCED ARE IN A RATIO THAT DEPENDS ON THE DIFFERENTIAL VOLTAGE BETWEEN THE TWO INPUTS. THESE SIGNAL CURRENTS ARE CONVERTED IN THE VGA TO SIGNAL VOLTAGES.

TO ENSURE THAT THE OUTPUT DC POTENTIAL DOES NOT VARY WITH GAIN, COMPENSATING GATES, CONTROLLED BY THE SAME REFERENCE AND GAIN CONTROL VOLTAGE AS THE INPUT CIRCUIT, ARE CONNECTED INTO THE OUTPUT CIRCUIT.

THE SIGNAL VOLTAGES AT THE OUTPUT OF THE VGA ARE APPLIED TO A LINEAR GAIN AMPLIFIER THAT HAS A GAIN OF APPROXIMATELY TEN. THE OUTPUT OF THE LINEAR GAIN AMPLIFIER IS APPLIED TO A DATA DETECTOR, AND TO AN AMPLITUDE DETECTOR AND HOLD CIRCUIT THAT PRODUCES THE GAIN CONTROL VOLTAGE.

NOTE: DURING WRITE OPERATIONS (SEE "WRITE DATA"), VGA FORMS A 'SQUELCH' CIRCUIT THAT ELIMINATES LARGE TRANSIENTS IN THE INPUT OF THE DATA CHANNEL, PARTICULARLY DURING TURN-ON AND TURN-OFF TIMES.

THE DATA DETECTOR CIRCUIT EXTRACTS FROM THE ANALOG SIGNAL TIMING INFORMATION CONTAINED IN THE SIGNAL PEAKS. THIS TIMING INFORMATION IS PROCESSED IN THE VOLTAGE-CONTROLLED OSCILLATOR (VCO) SYNC CONTROL, PHASE DISCRIMINATOR AND MFM DECODES CIRCUITS, DESCRIBED LATER.

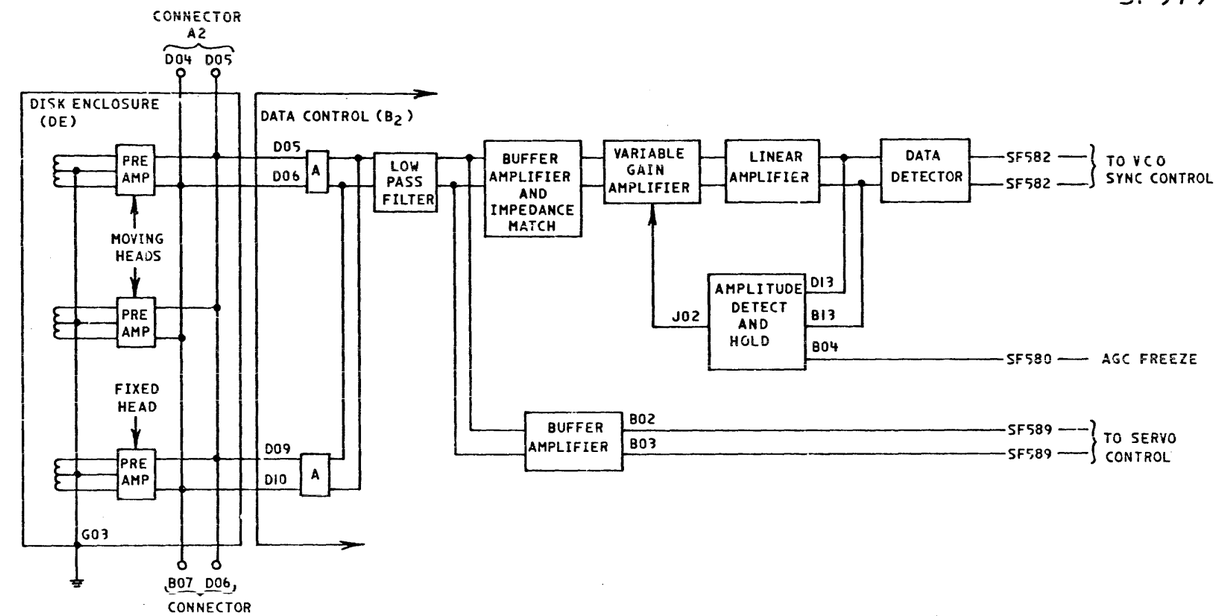
AMPLITUDE DETECTOR AND HOLD CIRCUIT

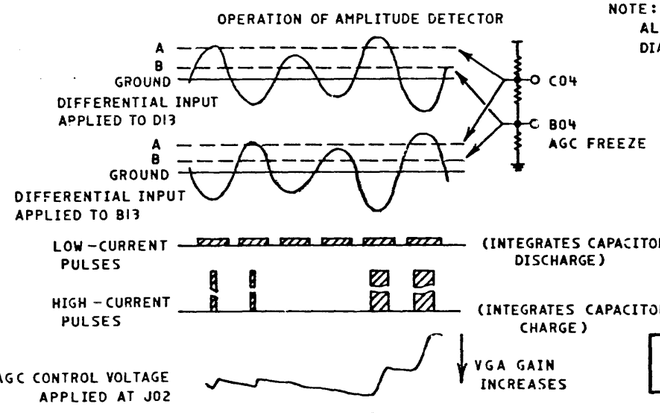
TWO REFERENCE LEVELS (A AND B) ARE SET IN THE AMPLITUDE DETECTOR AND HOLD CIRCUIT AS FOLLOWS.

WHEN SIGNALS APPLIED AT EITHER OF THE DIFFERENTIAL INPUTS TO THE VGA ARE OF GREATER AMPLITUDE THAN THE FIRST OF THE REFERENCE LEVELS (A) AN INTEGRATOR CAPACITOR IN THE AMPLITUDE DETECTOR AND HOLD CIRCUIT IS CHARGED POSITIVELY. LOW-CURRENT SIGNAL PULSES DISCHARGE THE CAPACITOR. WHEN THE CIRCUIT IS BALANCED, HIGH CURRENT PULSES OCCUR ONLY AT THE PEAKS OF INPUT WAVEFORMS.

THE SECOND REFERENCE LEVEL (B) IS A REFERENCE POTENTIAL THAT DETERMINES THE DISCHARGE CHARACTERISTICS OF THE INTEGRATOR CAPACITOR.

DURING THE TIMES THAT SAMPLE SERVO INFORMATION IS READ, THE TWO REFERENCE LEVELS ARE RAISED ABOVE THE NORMAL DATA-READ LEVELS, AND THE CHARGING AND DISCHARGING OF THE INTEGRATOR CAPACITOR ARE INHIBITED. THIS PREVENTS TRANSIENT DISTRUBANCES IN THE READ CHANNEL.





NOTE:
ALL THE PINS SHOWN ON THIS DIAGRAM ARE ON BOARD -A1

EC HISTORY		DRAWING TITLE
20FEB79	375351	A1B2 READ DATA
		MACH 4963
		PART NO 6839636
		CLASSIFICATION
C		IBM CORP

SF579

DATA CONTROL (CONTINUED)

DATA CONTROL SAMPLE SERVO CONTROL

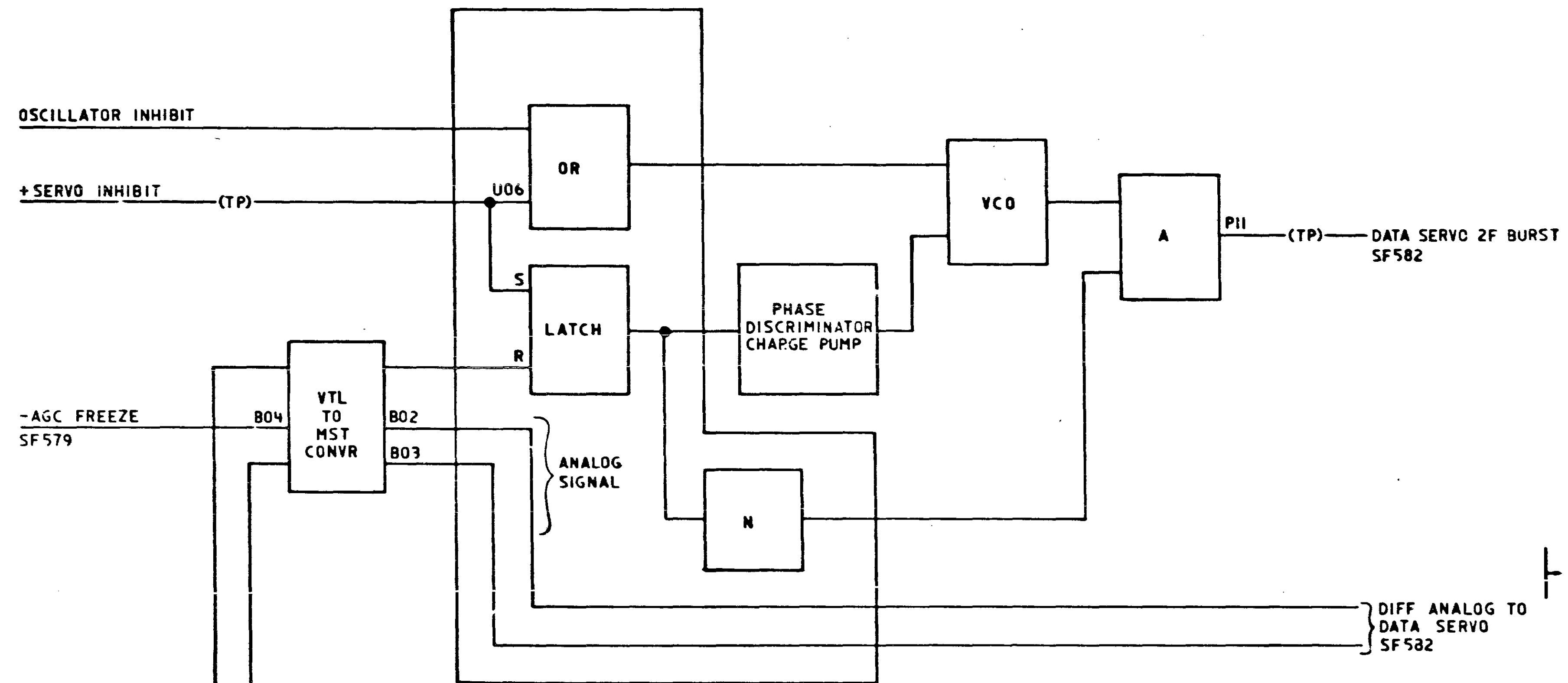
WHEN DATA IS BEING READ, THE VOLTAGE CONTROLLED OSCILLATOR (VCO) IS SYNCHRONIZED, IN FREQUENCY AND PHASE, WITH THE RECORDED DATA.

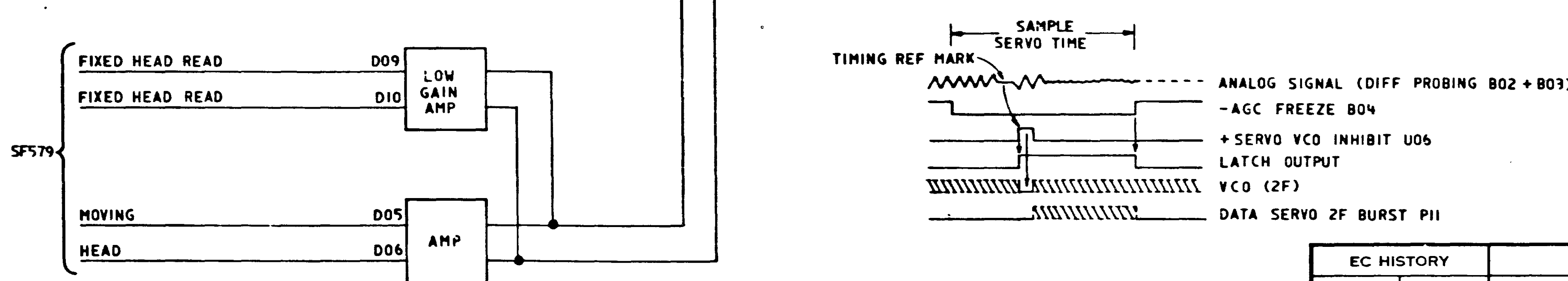
HOWEVER, DURING THE SERVO SAMPLE TIME THE VCO IS SYNCHRONIZED WITH DATA READ FROM THE SERVO SURFACE, AS DESCRIBED BELOW.

THE DURATION OF THE SAMPLE SERVO TIME (22 BYTES) IS SET BY THE '–AGC FREEZE' SIGNAL. JUST AFTER THE START OF THIS SIGNAL, THE MARK DETECTION CIRCUIT (ON THE SERVO CARD) DETECTS A TIMING REFERENCE MARK IN THE ANALOG SIGNAL, AND FROM IT PRODUCES THE '+ SERVO VCO INHIBIT' SIGNAL. THE '+ SERVO VCO INHIBIT' SIGNAL SETS THE LATCH THE OUTPUT OF WHICH GOES POSITIVE. THIS GATES OFF DATA INPUTS TO THE PHASE DISCRIMINATOR AND THUS PREVENTS '–INCREASE LINE' OR '–DECREASE LINE' INPUTS TO THE CHARGE PUMP; THE CHARGE PUMP OUTPUT IS THEN HELD AT THE VALUE REACHED JUST BEFORE THE '+ SERVO VCO INHIBIT' WAS APPLIED. THE VCO THEN 'FREE RUNS'.

THE OUTPUT OF THE VCO DURING SAMPLE SERVO TIME IS GATED OFF THE DATA CONTROL CARD AS 'DATA SERVO 2F BURST'.

AT THE END OF THE SAMPLE SERVO TIME THE LATCH IS RESET AND DATA CONTROL OF THE VCO IS RE-ESTABLISHED.





EC HISTORY		DRAWING TITLE
20FEB79	375351	A1B2 DATA CHANNEL SERVO
		MACH 4963
		PART NO 6839637
		CLASSIFICATION

C

IBM CORP

SF580

SF580

WRITE DATA

NOTE: 'PRE-COMPENSATION', MENTIONED IN THE FOLLOWING TEXT, IS A DISTORTION OF MFM (MODIFIED FREQUENCY MODULATION) ENCODED DATA TO COMPENSATE FOR TIMING ERRORS.

DATA TO BE WRITTEN ON THE DISK IS SERIAL 'NRZ' DATA APPLIED TO THE '–WRITE DATA' INPUT U02. THE '–WRITE DATA' SIGNAL IS CONVERTED TO MST LEVELS AND APPLIED TO THE 4-BIT SHIFT REGISTER AS DESCRIBED BELOW.

'WRITE SELECT' IS APPLIED TO THE PRE-COMPENSATION TIMING VIA THE VTL TO MST CONVERTER AND INVERTER. '2F WRITE CLOCK' IS DIVIDED BY 2 IN THE 2 AC TRIGGER AND APPLIED TO THE PRE-COMPENSATION TIMING CIRCUIT AS '1F'. WHEN 'WRITE SELECT' IS ACTIVE, '1F' IS GATED INTO THE PRE-COMPENSATION CIRCUIT WHICH THEN PRODUCES '2F EARLY', '2F ON TIME', AND '2F LATE' OUTPUTS. THE OUTPUTS ARE CLOCK PULSES OF DIFFERENT PHASES WITH RESPECT TO EACH OTHER. '2F EARLY' AND '2F LATE' ARE DISPLACED RESPECTIVELY + AND –9 NANOSECONDS FROM '2F ON TIME'.

THE 1F SIGNAL IS ALSO APPLIED TO THE MFM ENCODER IN WHICH IT IS ANDED WITH THE '2F EARLY' OUTPUT OF THE PRE-COMPENSATION TIMING CIRCUIT. THIS PRODUCES NARROW PULSES AT BIT-CELL RATE. THE NARROW PULSES CLOCK 'WRITE DATA' INTO THE 4-BIT SHIFT REGISTER.

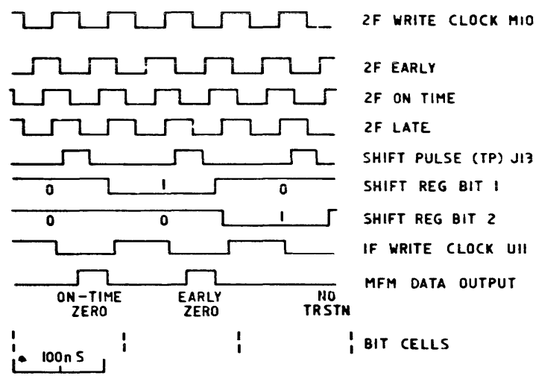
THE SHIFT REGISTER CHANGES THE SERIAL INPUT DATA INTO A 4-BIT PARALLEL SIGNAL THAT IS APPLIED TO THE MFM ENCODER. THE MFM ENCODER PRODUCES MFM-CODED DATA (A TRAIN OF PULSES EACH OF APPROXIMATELY 30 NANOSECONDS DURATION) THAT IS CONVERTED TO 'BI-PHASE' SIGNALS BY AN AC TRIGGER. THE BI-PHASE SIGNAL IS APPLIED TO THE HEADS VIA THE WRITE LINE DRIVERS.

THE PRE-COMPENSATION CIRCUIT USES THE '2F EARLY' TO ADD PRE-COMPENSATION TO THE ENCODED DATA.

THE MFM ENCODER OUTPUT IS ALSO APPLIED TO THE DATA SEPARATOR CIRCUIT WHICH READS BACK THE WRITTEN DATA DURING A WRITE OPERATION.

THE '+ WRITE DC' CONTROL LINE IS USED ONLY DURING MANUFACTURING TESTS.

WRITE ENCODING TIMING EXAMPLE

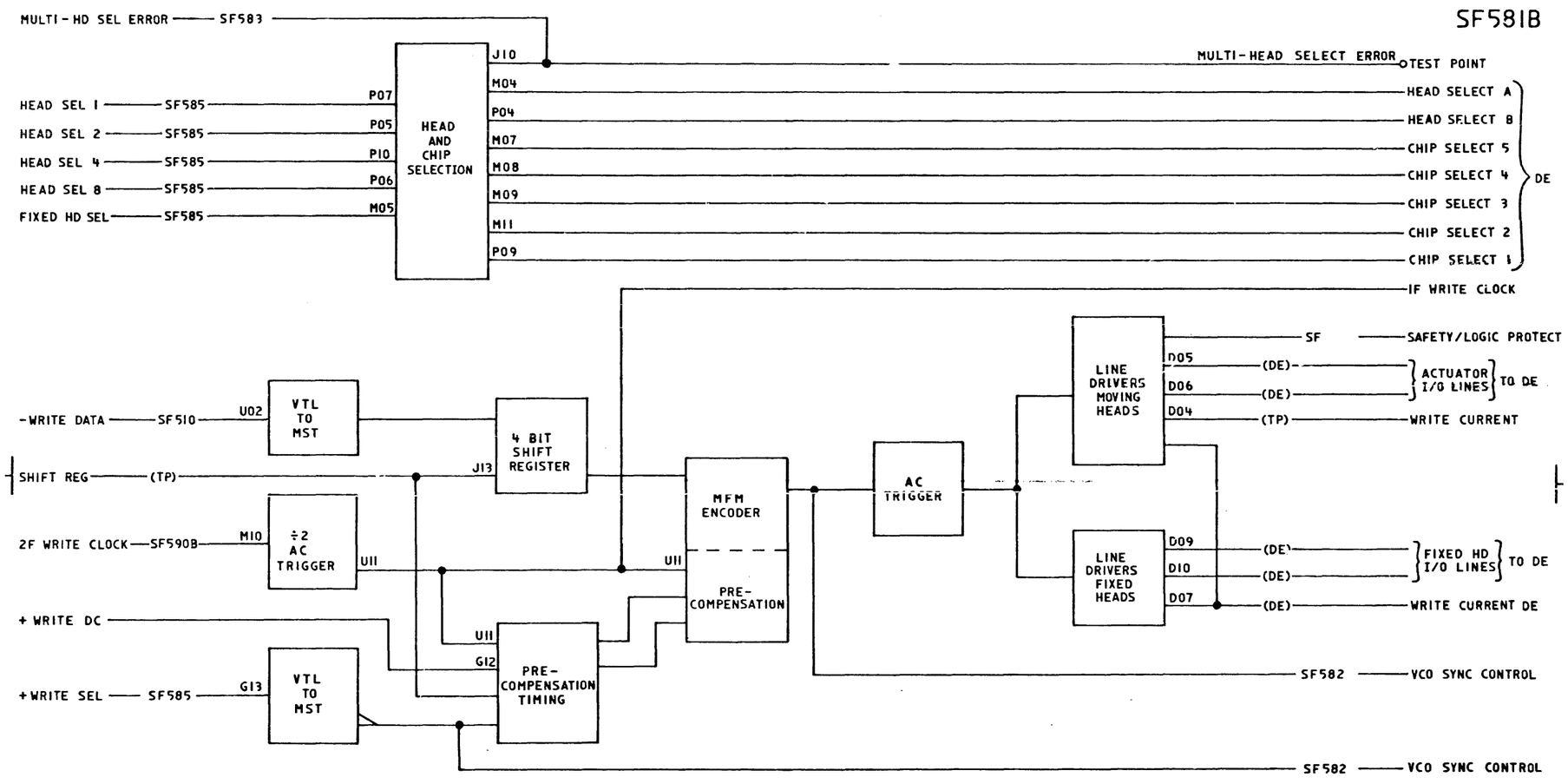


EC HISTORY		DRAWING TITLE	
20FEB79	375351	A1B2 WRITE DATA	
		MACH 4963	
		PART NO 6839638	
C		CLASSIFICATION	IBM CORP

SF581A

SF581A

SF581B



EC HISTORY		DRAWING TITLE
20FEB79	375351	AIB2 WRITE DATA
11 MAR 80	375662	MACH 4963
		PART NO 6839639
		CLASSIFICATION

C

IBM CORP

SF581B

SF581B

SF582

VOLTAGE CONTROLLED OSCILLATOR (VCO) CONTROL

THE VCO AND ASSOCIATED CONTROL CIRCUIT FORM A PHASE-LOCKED LOOP THAT TRACKS THE FREQUENCY AND AVERAGE PHASE OF THE READ INPUT DATA SIGNAL, AND CORRECTS FOR ANY DRIFT IN THESE SIGNAL COMPONENTS.

CIRCUIT OPERATION

THE 2F READ CLOCK APPLIED TO THE 'DATA LATCH' IS COMPARED WITH THE 'DATA SS (SINGLE SHOT)' FOR COINCIDENCE. IF THE 'DATA SS' PULSE IS COMPLETED BEFORE THE END OF THE CORRESPONDING 'DATA LATCH' PULSE, AN '–INCREASE LINE' IS ACTIVATED. IF THE 'DATA SS' PULSE IS COMPLETED AFTER THE END OF THE CORRESPONDING 'DATA LATCH' PULSE, A '–DECREASE LINE' IS ACTIVATED. THE COMBINED OUTPUT (AN ANALOG CONTROL VOLTAGE) IS APPLIED TO THE VCO TO RESTORE THE CORRECT COINCIDENCE OF THE 'DATA LATCH' PULSES WITH THE 'DATA SS' PULSE.

RELATIVELY LARGE DISCONTINUITIES OF THE DATA SIGNAL CAN CAUSE LOSS OF SYNCHRONIZATION OF THE 'DATA LATCH' AND 'DATA SS' SIGNALS. THEREFORE, WHEN THE SOURCE OF THE DATA SIGNAL CHANGES, FOR EXAMPLE WHEN CHANGING FROM WRITING TO READING, THE VCO CONTROL CIRCUIT IS SWITCHED MOMENTARILY TO THE 'FAST SYNCHRONIZATION' STATE.

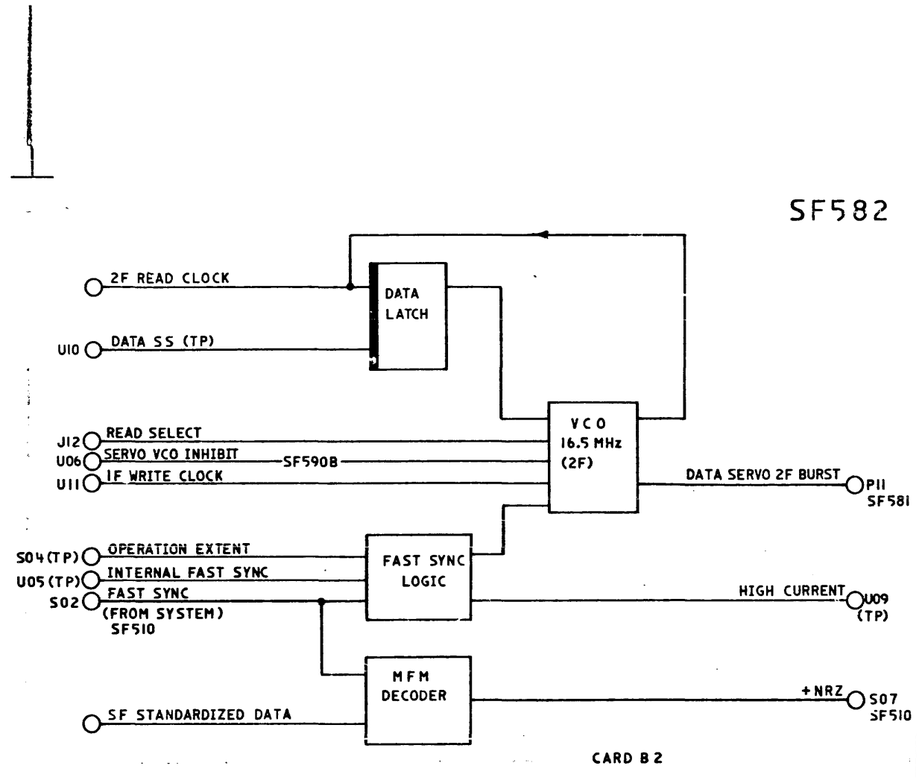
DURING FAST SYNCHRONIZATION THE VCO OPERATES SIMILARLY TO THE MANNER DESCRIBED FORMERLY, EXCEPT THAT THE SIGNALS INVOLVED ARE MUCH GREATER.

THE 'FAST SYNC' SIGNAL APPLIED TO THE FAST SYNC LOGIC CAN BE IN ONE OF TWO PAHSES DEPENDING ON THE MODE (READ OR WIRTE) IN WHICH THE DSD IS OPERATING. THE FAST SYNC LOGIC SELECTS THE APPROPRIATE FAST SYNC INPUT, THAT IS, 'FAST SYNC' FROM USING SYSTEM OR 'INTERNAL FAST SYNC'.

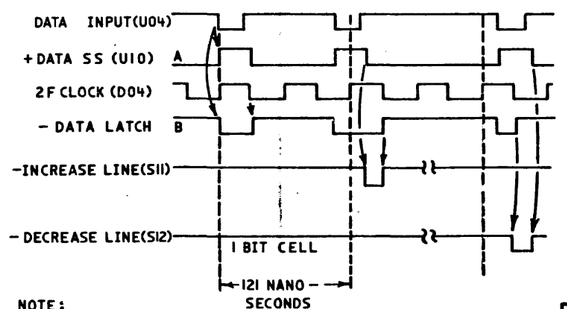
THE 'INHIBIT SS' PULSE SETS A VCO CONTROL LATCH, THE OUTPUT OF WH'CH CUTS OFF THE DATA APPLIED TO THE PHASE DISCRIMINATOR AND DATA DECODER PART OF THE VCO. THE VCO IS STOPPED DURING THIS TIME BY A 2F CLOCK PULSE.

THE CIRCUIT IS RESET BY THE END OF THE 'INHIBIT SS' PULSE AND THE DATA PULSES, THE VCO IS THEN RESTARTED SO THAT THE DATA PULSES AND THE VCO OUTPUT ARE SYNCHRONIZED.

WHEN THE DSD IS NOT UNDER THE CONTROL OF THE USING SYSTEM, THE VCO IS SYNCHRONIZED WITH THE WRITE CLOCK.



VCO CONTROL DIAGRAM



NOTE:
THIS IS A SIMPLIFIED TIMING DIAGRAM. OSCILLATOR LATE AND EARLY PULSES DO NOT OCCUR ON CONSECUTIVE SERVO CLOCK PULSES.

EC HISTORY		DRAWING TITLE
20 FEB 79	375351	AIB2 VCO CONTROL
11 MAR 80	375662	MACH 4963
		PART NO 6839640
		CLASSIFICATION

C

IBM CORP

SF582

SF582

620-0131-1 MROZ 780522201 ALD DRAWING FORMAT ASTROCLOTH N680T 3730 ABCDE

DRAFTING MEDIA GRAPHIC CONTROLS CORPORATION Printed in U.S.A.

WRITE SAFETY DETECTION

GENERAL

WRITE SAFETY DETECTION CIRCUITS ON THE DATA CHANNEL CARD CHECK OPERATIONS OF THE DSD THAT COULD AFFECT DATA WRITTEN ON THE DISKS OR DATA BEING WRITTEN.

THESE CIRCUITS CHECK FOR THE FOLLOWING UNSAFE CONDITIONS:

- NO TRANSITIONS – THAT IS, FAILURE OF WRITE DRIVERS TO SWITCH CURRENT IN A HEAD IN WRITE MODE.
- HEAD GROUNDED – THIS CAUSES EXCESSIVE CURRENT IN THE CENTER TAP LINE.
- MULTI CHIP SELECTION – THIS CAUSES EXCESSIVE CURRENT IN THE POSITIVE POWER SUPPLY TO THE DE CIRCUITS.
- SERVO UNSAFE – LOGICAL OR ANALOG UNSAFE CONDITIONS EXTERNAL TO THE DATA CHANNEL.
- WRITE CURRENT WHEN NOT WRITING.

EACH OF THE FIRST FOUR UNSAFE CONDITIONS LISTED ABOVE CAUSES A LATCH TO BE SET IN THE SAFETY CONDITION LATCHES.

THE LATCH OUTPUTS ARE ORED AND THE OUTPUT OF THE OR IS DOT ORED WITH '+ SERVO UNSAFE' TO PRODUCE THE LINE '+ DATA UNSAFE'.

NO TRANSITIONS

NORMALLY, WHEN THE CURRENT IN A HEAD IS REVERSED DURING A WRITE OPERATION, VOLTAGE SPIKES ARE PRODUCED IN THE HEAD WINDING. IF THESE SPIKES ARE MISSING, (THAT IS, NO TRANSITIONS OCCUR) EITHER THE HEAD, OR THE WRITE DRIVER HAS FAILED.

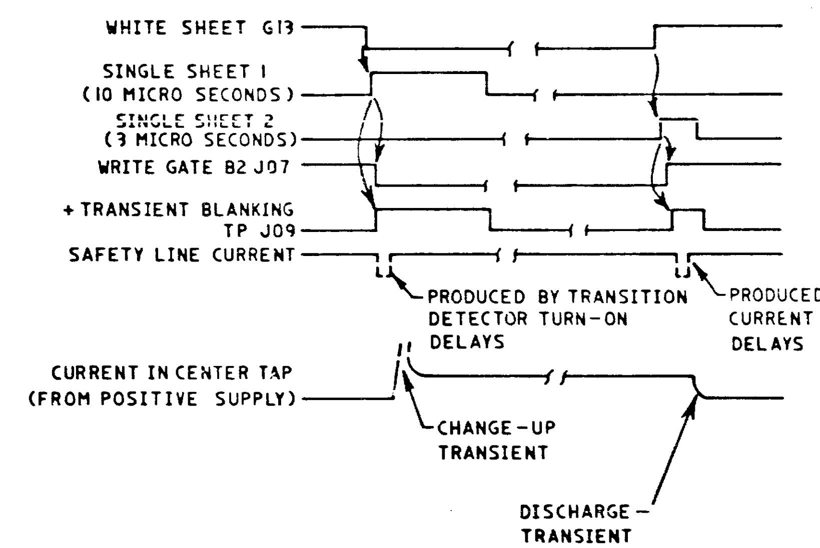
THE VOLTAGE DUE TO THIS FAILURE ANDED WITH '–WRITE GATE' PRODUCES THE '– NO TRANSITIONS DURING WRITING' SIGNAL. THIS SIGNAL SETS THE APPROPRIATE SAFETY CONDITION LATCH.

HEAD GROUNDED

A HEAD-TO-GROUND SHORT CIRCUIT CAN CAUSE CURRENT IN THE CENTER-TAP LINE TO EXCEED THE THRESHOLD SET IN THE ASSOCIATED CURRENT THRESHOLD SENSE CIRCUIT; THEN A 'HEAD GROUNDED' ERROR SIGNAL IS PRODUCED.

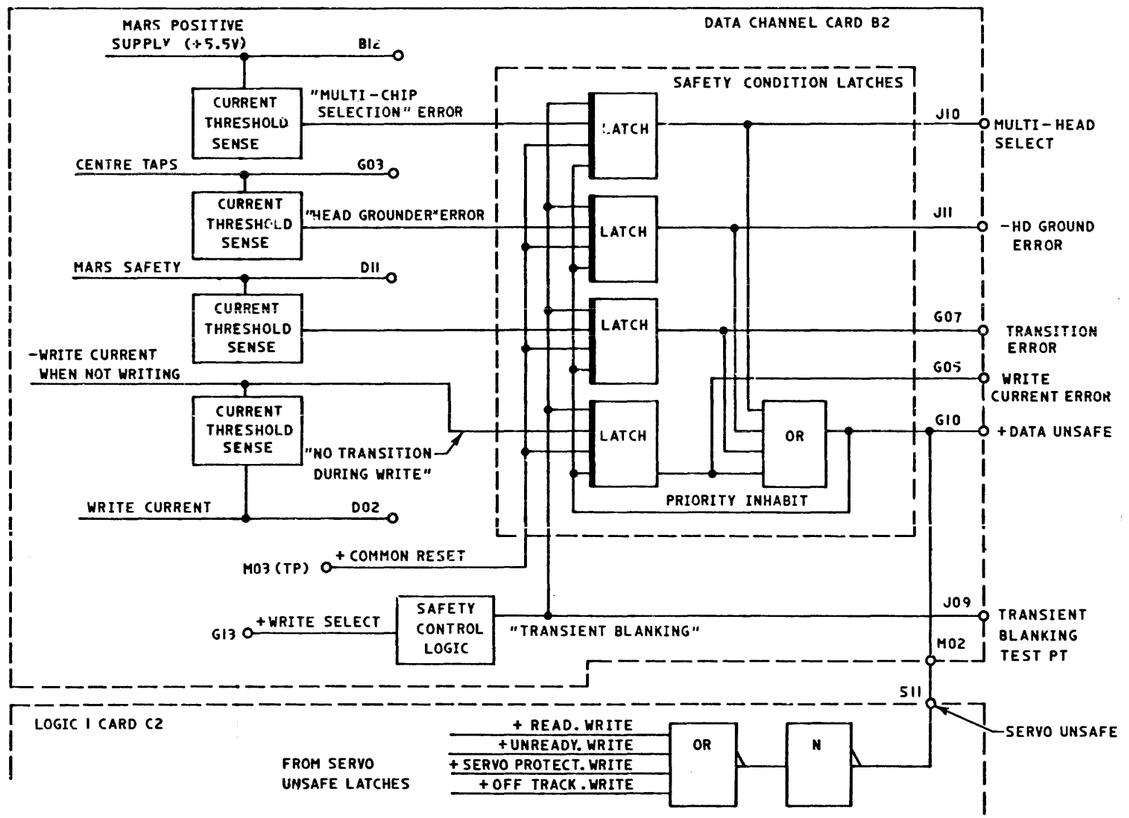
MULTI-CHIP SELECTION

IF CURRENT IN THE POSITIVE SUPPLY TO THE DE EXCEEDS THE THRESHOLD SET IN THE ASSOCIATED CURRENT THRESHOLD SENSE CIRCUIT, A 'MULTI-CHIP SELECTION' ERROR SIGNAL IS PRODUCED.



EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	A2B2 WRITE SAFETY	
		MACH 4963	
		PART NO 6839641	
C		CLASSIFICATION	IBM CORP

SF583B



EC HISTORY		DRAWING TITLE
20 FEB 79	375351	A1B2 WRITE SAFETY
11 MAR 80	375662	MACH 4963
		PART NO 6839642
		CLASSIFICATION

C

IBM CORP

SF583B

SF583B

SF 584

READ DATA SEPARATION

DATA FROM THE DATA DETECTOR CONSISTS OF A TRAIN OF PULSES THAT CONTAIN TIMING INFORMATION RELATED TO PEAKS IN THE ORIGINAL ANALOG SIGNAL. THE DATA SEPARATION LOGIC IDENTIFIES THE TIMING INFORMATION AS '1' OR '0' PULSES, ELIMINATES THE '0' PULSES, AND RE-TIMES THE '1' PULSES WITH THE INTERNAL CLOCK.

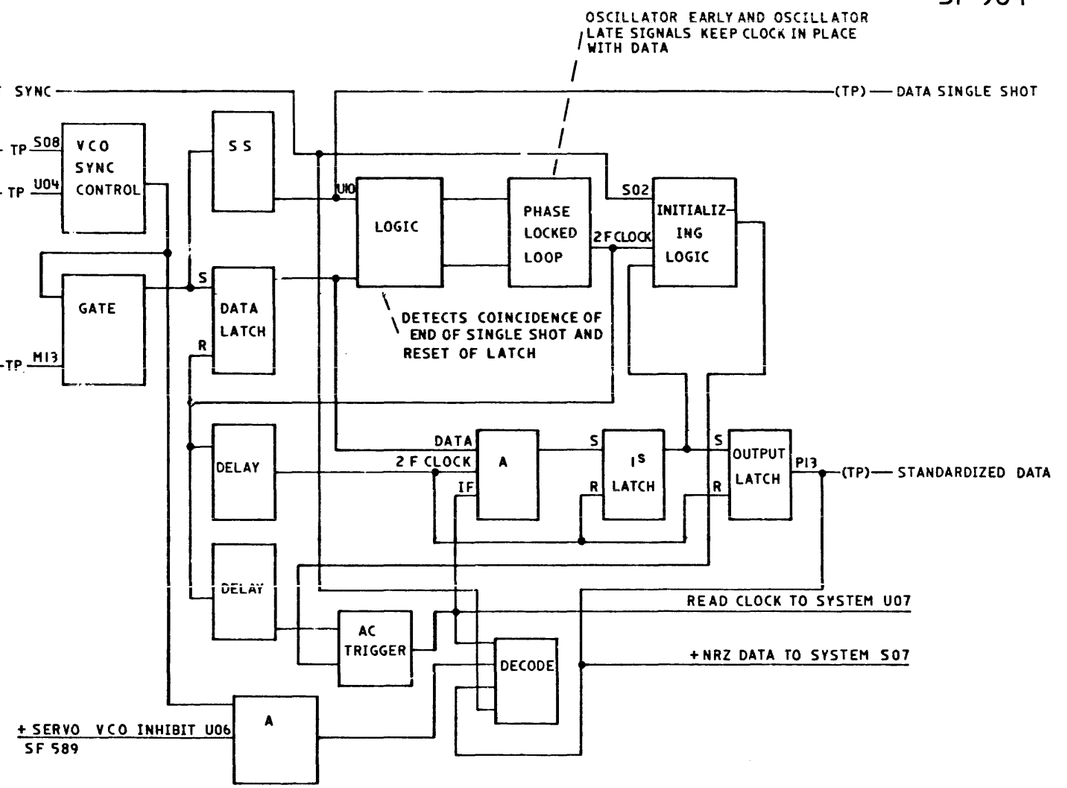
(DEFINITION OF '1S' AND '0S': A '1' BIT IS TRANSMITTED DURING THE SECOND HALF OF A 1F CLOCK CYCLE. A '0' BIT IS TRANSMITTED DURING THE FIRST HALF OF A 1F CLOCK CYCLE, EXCEPT WHEN A '0' IMMEDIATELY FOLLOWS A '1' BIT. IN THIS CASE, NO '1' BIT IS TRANSMITTED DURING THE 1F CLOCK CYCLE.)

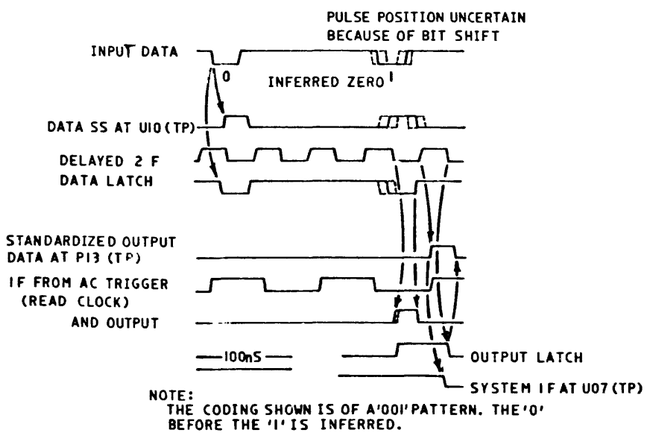
NOTE: IN THE FOLLOWING DESCRIPTION IT ASSUMED THAT THE PHASE LOCKED LOOP IS 'LOCKED' TO THE AVERAGE PHASE AND FREQUENCY OF THE INPUT DATA SIGNAL.

THE INPUT DATA IS ROUTED THROUGH THE VCO SYNC CONTROL, WHICH, IN THE READ MODE, INVERTS THE DATA SIGNAL AND APPLIES IT THROUGH THE GATE (IN THIS MODE THE 'INHIBIT' SIGNAL ON THE GATE IS INEFFECTIVE) TO THE DATA LATCH AND THE SINGLE SHOT CIRCUIT. THE SINGLE SHOT CIRCUIT FORMS PART OF THE DISCRIMINATOR THAT CONTROLS THE PHASE OF THE PHASE-LOCKED LOOP.

IF THE DATA LATCH IS SET, THE DATA IS APPLIED TO AN AND GATE (THAT FORMS PART OF A MFM DECODER CIRCUIT) WITH A DELAYED '2F CLOCK' SIGNAL, AND A '1F' SIGNAL FROM THE AC TRIGGER. WHEN THESE THREE INPUTS ARE SATISFIED, THE OUTPUT OF THE AND CIRCUIT SETS THE '1'S' LATCH; THIS LATCH PROVIDES AN OUTPUT WHEN A '1' IS DETECTED. THE OUTPUT OF THE '1'S' LATCH IS APPLIED TO THE OUTPUT LATCH WHICH, IN TURN, GIVES AN OUTPUT SIGNAL IN THE FORM OF 30-NANOSECOND PULSES.

THE INITIALIZING LOGIC FORCES THE PHASE OF THE AC TRIGGER SO THAT THE 1F THAT THE TRIGGER PRODUCES CORRESPONDS TO THE TIMING OF BIT CELLS DURING FAST SYNCHRONIZATION.





EC HISTORY		DRAWING TITLE
20 FEB 79	375351	AIB2 READ DATA
11 MAR 80	375662	MACH 4963
		PART NO 6839643
		CLASSIFICATION
C		IBM CORP

SF584

SF584

LOGIC 1 CARD (C2)

INTERRUPT SENSE CYCLE

SENSE COMMAND CYCLE AFTER A POWER-UP

NOTE: THE NUMBERS QUOTED IN THE CIRCLES REFER TO THEIR CORRESPONDING NUMBERS SHOWN IN THE TIMING DIAGRAM.

THE FOLLOWING USER SYSTEM-TO-DSD SENSE STATUS SEQUENCE OCCURS AFTER AN INTERRUPT (1) :

1. TAG CODE 100 (TAG 4) (2) IS SET BY THE SYSTEM.
2. AFTER A DELAY OF 100 NANOSECONDS, 'CONTROL SAMPLE' (3) IS SET.
3. THE DSD READS THE TAG CODE (4) AND SETS THE SENSE DATA ON THE CONTROL BUS (5) ; 'CONTROL SAMPLE RECEIVED' (6) IS ALSO SET.
4. CONTROL BUS READ INFORMATION (7) IS READ BY THE SYSTEM, THEN 'CONTROL SAMPLE' IS RESET.
5. THE DSD RECEIVES 'CONTROL SAMPLE' AND RESETS 'INTERRUPT', 'CONTROL SAMPLE RECEIVED', AND (SLIGHTLY DELAYED) THE CONTROL BUS.
6. DSD INTERNAL TIMING GATES OFF THE 'HOLD OFF INTERRUPT' WHICH RESETS 'INTERRUPT'.

TAG / BUS	SEEK CONTROL	DES'D ADDRESS	WRAP BACK	SENSE	DIAG SENSE 1	DIAG SENSE 2	DIAG SENSE 3
TAG	001	010	011	100	101	110	111
0	RECAL	128		FIXED HD NOT SEL	ON TRACK	BEHIND HOME	NOT SHIFT
1	FIX HD SEL	64		BRAKE APPLIED	LIN REG N & EV	MISSING CKS ÷ 2	NOT OFF TRK WRITE
2	HEAD SEL 8	32		TRACK UNAVAIL	MISG IND & SECT	NOT MISG CK ERR LTH	INSIDE AGC WINDOW
3	HEAD SEL 4	16		COMMAND ERROR	OUT DIRECTION	COIL 1 LOW	-AGC FREEZE
4	HEAD SEL 2	8		UNSAFE	NOT DRIVE OUT	MISS SERVO SIG	DEMODS PULSING
5	HEAD SEL 1	4		SEEK INCPLT	NOT DRIVE IN	OFF DATA TRACK	NOT READ WRITE
6		2		HOME	TAG ERROR	NOT MISSING PES	NOT SERVO PROT WR
7	CYLINDER SEL	1		NOT READY	VEL PROFILE ERR	CTR 5 IN SYNC	ILLEGAL MOVE

TIMING DIAGRAM

SEQUENCE AFTER DSD INTERRUPT

NOTE: THE TIMINGS SHOWN ARE AT THE DSD PIN LOCATIONS

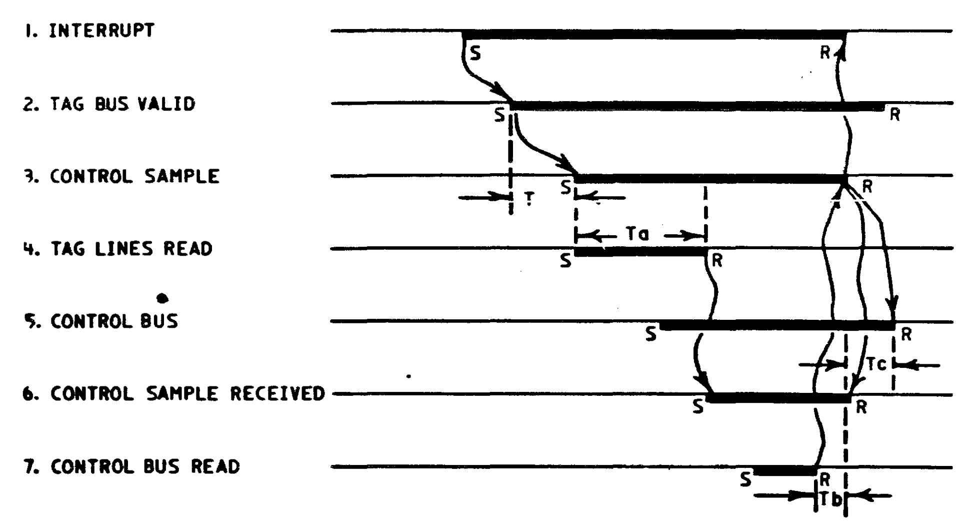
T = 100 nS MINIMUM

Ta = 1 μS MINIMUM

~~Tb = 500 nS MINIMUM~~

Tc = 0 nS MINIMUM

30 nS MAXIMUM



DSD INTERRUPT TO USING MACHINE

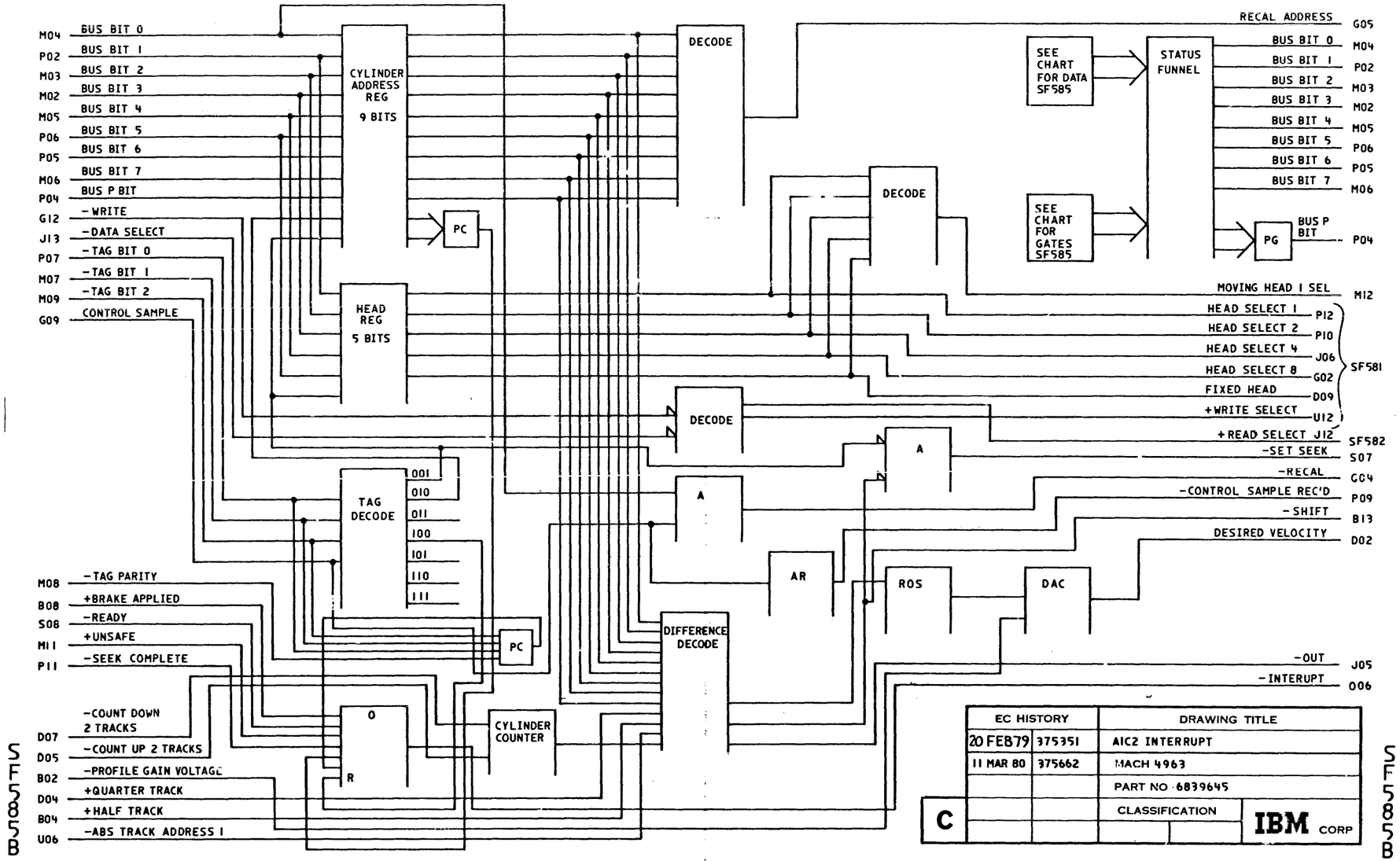
TAG DECODE TAG 100 (TAG 4)

SENSE CYCLE TAG 100 (TAG 4)

CONTROL BUS

EC HISTORY		DRAWING TITLE
20 FEB 79	375351	A1C2 INTERRUPT
		MACH 4963
		PART NO 6839644
		CLASSIFICATION
C		IBM CORP

SF585B



EC HISTORY		DRAWING TITLE
20 FEB 79	375351	AIC2 INTERRUPT
11 MAR 80	375662	MACH 4963
		PART NO 6839645
		CLASSIFICATION

C

IBM CORP

SF585B

SF585B

620-0131-1 MROF 780822201 ALD DRAWING FORMAT ASTROCLOTH N680Y 2720 ABCDE

DRAFTING MEDIA GRAPHIC CONTROLS CORPORATION Buffalo, New York Printed in U.S.A.

LOGIC 2

WRITE CLOCK IS DIVIDED BY 16 BY COUNTERS. COUNTER 4 OUTPUT IS THE SAME FREQUENCY AS THE SERVO CLOCK SS. COUNTER 5 IS USED TO DISTINGUISH BETWEEN NORMAL AND QUADRATURE CELLS CORRESPONDING TO ALTERNATE SERVO CLOCK PULSES.

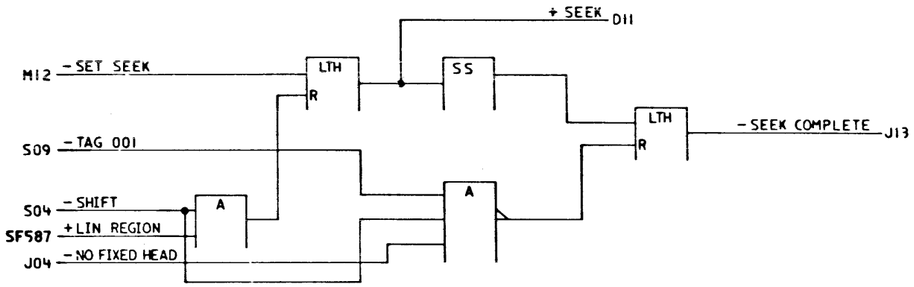
COUNTER 4 AND 5 OUTPUTS ARE DECODED INTO 4 OUTPUTS CORRESPONDING TO THE N1, N2 AND Q1, Q2. ANY OUT OF SYNC CONDITION WILL BE SIGNALLED TO THE OSCILLATOR BY THE 'OSCILLATOR EARLY' OR 'LATE' LINES TO FORCE A FREQUENCY SHIFT TO BRING THE WRITE CLOCK BACK INTO SYNCHRONISM.

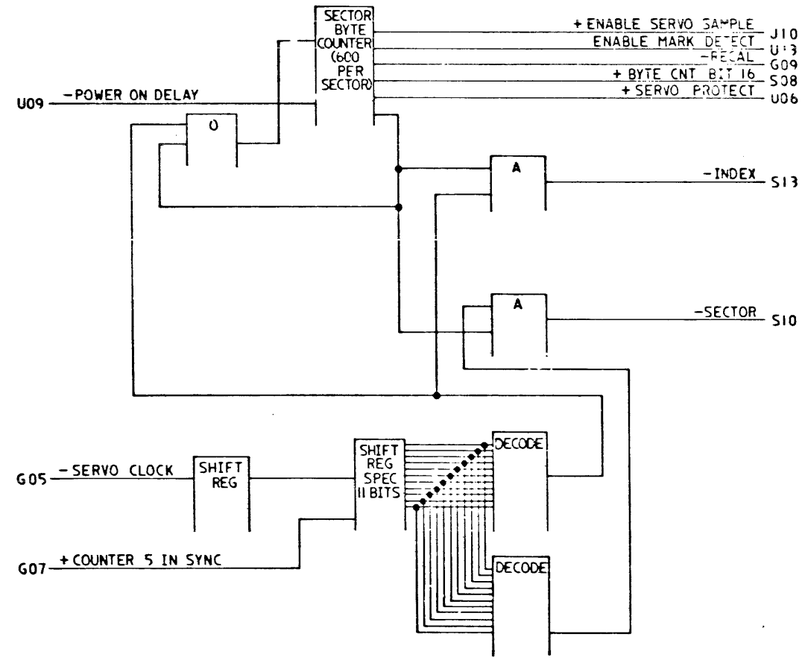
THE SYNC DETECTOR PROVIDES PROTECTION FOR ANY GROSS TIMING ERRORS.

MISSING CLOCK PULSES ARE FED TO A 1 BIT SHIFT REG AND DECODE TO LOOK FOR INDEX AND SECTOR PULSES.

HANDOVER VELOCITY CALIBRATION IS USED AFTER POWER UP TO PROVIDE AN OFFSET VOLTAGE TO THE "DESIRED VELOCITY" VOLTAGE. THE REQUIRED OFFSET IS GENERATED BY PRESETTING THE COUNTER AT THE START OF HVC TO 7 AND CHECKING VELOCITY OVER 2 TRACKS. IF VELOCITY IS 1.9ms PER TRACK THE COUNTER IS DECREMENTED BY 1 AND THE CYCLE REPEATED UNTIL THE TIME IS 1.9 ms TRACK OR UNTIL THE COUNTER HAS REACHED 0 WHEN ALLOW HVC IS RESET.

PROFILE GAIN VOLTAGE IS RECALIBRATED IN A SIMILAR METHOD EXCEPT THAT THE COUNTER IS RESET TO ZERO AND INCREMENTS UP UNTIL + VEL. PROF DROPS OR THE COUNTER IS FULL. "COUNTER FULL" PREVENTS THE COUNTER RESETTING TO ZERO IF ITS MAXIMUM COUNT IS EXCEEDED. RECALIBRATION ONLY TAKES PLACE ON COMMAND FROM THE SYSTEM.



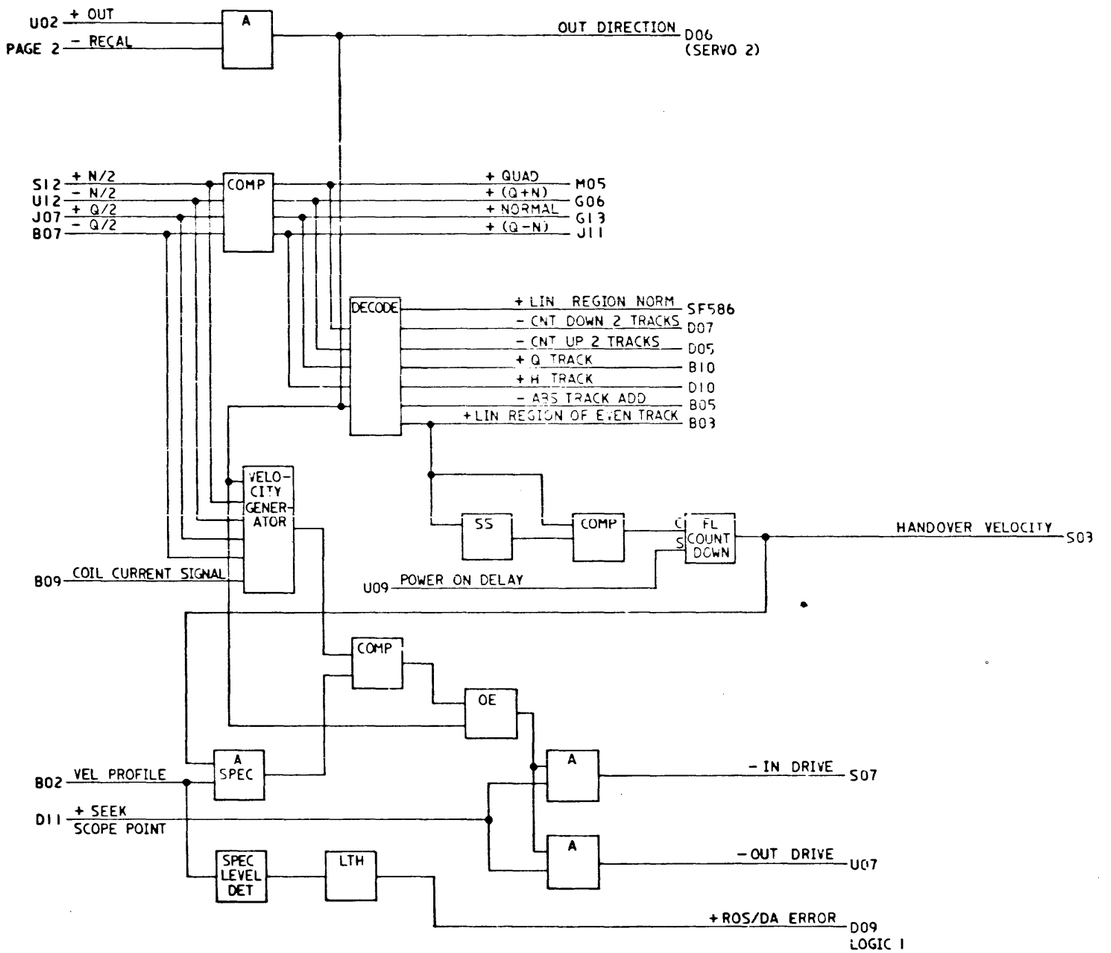


SF586

EC HISTORY		DRAWING TITLE
20FEB79	375351	AID2 SECTOR AND INDEX
		MACH 4963
		PART NO 6839646
		CLASSIFICATION

D

IBM CORP



SF587

EC HISTORY		DRAWING TITLE
20FEB79	375351	A1D2 HANDOVER VELOCITY
		MACH 4903
		PART NO 6839647
		CLASSIFICATION

D

IBM CORP

SF 588

PHASE LOCKED OSCILLATOR (PLO) LOOP

THE PLO IS SYNCHRONIZED IN PHASE AND FREQUENCY BY THE SERVO SIGNAL CLOCK PULSES AS FOLLOWS:

THE VOLTAGE CONTROLLED OSCILLATOR (VCO) RUNS AT APPROXIMATELY 16.5 MHz. THE OUTPUT 2F IS DIVIDED BY 2 TO GIVE '1F WRITE CLOCK'.

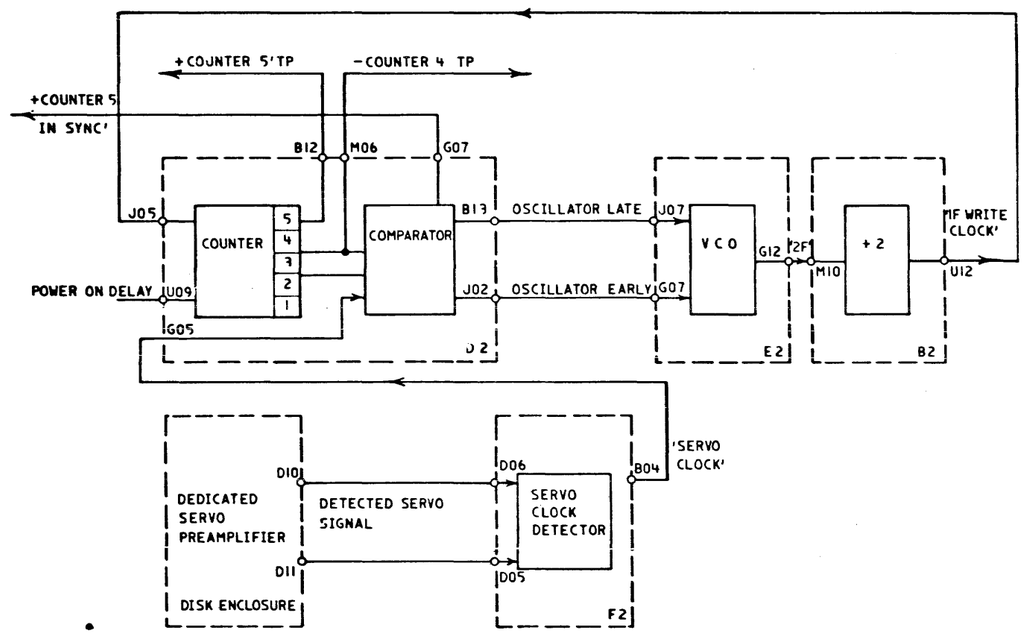
'1F WRITE CLOCK' DRIVES A 5 BIT COUNTER; 'COUNTER 4' OUTPUT IS 1/16TH OF THE PLO FREQUENCY. THE 'SERVO CLOCK' PULSES TRIGGER A SINGLE SHOT (+ SERVO CLOCK SS - 280 nS).

FOR THE PLO TO BE IN SYNCHRONIZATION THE TRAILING EDGE OF THE SERVO CLOCK SS MUST COINCIDE WITH THE MID-POINT OF THE NEGATIVE LEVEL OF THE 'COUNTER 4' SIGNAL .

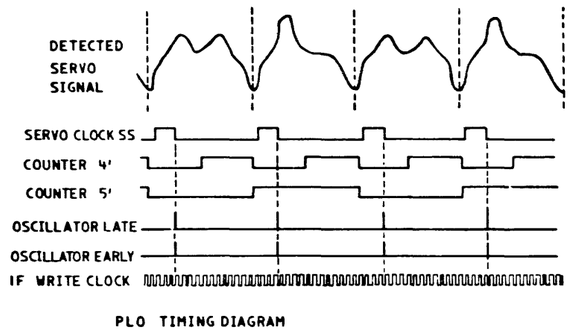
A COMPARATIVE CIRCUIT ON THE LOGIC 2 (D2) CARD LOOKS FOR THIS COINCIDENCE AND PROVIDES AN OUTPUT OF OSCILLATOR EARLY OR LATE TO THE VCO TO CORRECT ANY MISALIGNMENT.

DURING NORMAL SYNCHRONOUS OPERATION, NARROW OSCILLATOR LATE AND OSCILLATOR EARLY SIGNALS ARE PRODUCED CONTINUOUSLY AS SHOWN IN THE TIMING DIAGRAM.

THE PLO IS USED BY THE USING SYSTEM TO SERIALIZE WRITE DATA.



PLO DIAGRAM



PLO TIMING DIAGRAM

EC HISTORY		DRAWING TITLE
20FEB79	375351	AID2 PLO
		MACH 4963
		PART NO 6839648
		CLASSIFICATION

C

IBM CORP

SF588

SF588

SF589A

SERVO CONTROL E2 SERVO 1

SERVO MARKER FIELD

THE SERVO MARKER FIELD CONTAINS A PATTERN SEQUENCE OF POSITIVE ZERO CROSSINGS (9) (POSITIVE-GOING PULSES THAT PASS THROUGH 0 (ZERO) VOLTS) THAT SYNCHRONIZE THE DEMODULATOR WAVEFORMS 'SELECT DEMOD A', AND 'SELECT DEMOD B'.

SERVO GAIN FIELD

THE SERVO GAIN FIELD IS JUST OVER TWO BYTES OF EACH 22-BYTE SERVO SAMPLE FIELD. IN THE SERVO GAIN FIELD, A FIXED-AMPLITUDE SIGNAL CALLED 'DATA SURFACE LINEAR' (1) CONTROLS THE AUTOMATIC GAIN CONTROL (AGC) LOOP SO THAT THE LOOP COMPENSATES FOR CHANGES DUE TO:

- HEAD-TO-DISK SURFACE VARIATIONS.
- SURFACE CHANGES.
- TRACK LOCATION VARIATIONS THAT OCCUR BECAUSE OF DIFFERENCES IN LINEAR SPEED BETWEEN INNER TRACKS AND OUTER TRACKS, AND, THUS, COUPLING BETWEEN HEAD AND DISK SURFACE.

THE AGC LOOP COMPRISES THE VARIABLE GAIN AMPLIFIER (VGA) AND THE AGC AMPLIFIER.

THE 'SELECT GAIN ADJUST' SIGNAL (2) IS ACTIVE THROUGHOUT THE SERVO GAIN FIELD. THIS CAUSES THE DEMODULATOR TO GIVE AN OUTPUT THAT IS ASYNCHRONOUSLY RECTIFIED AND THEN APPLIED TO THE AGC LOOP. THE AGC LOOP INVERTS THE DEMODULATOR OUTPUT AND SUBTRACTS IT FROM THE 'TRACK REFERENCE SIGNAL' (3). THE DIFFERENCE VOLTAGE CHARGES THE GAIN STORE CAPACITOR C2.

THE RESULTING GAIN VOLTAGE ACROSS THE GAIN STORE CAPACITOR C2 IS FILTERED AND BUFFERED IN THE AGC AMPLIFIER. THE AMPLIFIER THEN PRODUCES A SIGNAL TO THE NEW LEVEL REQUIRED FOR THE PARTICULAR SECTOR IF EITHER 'ENABLE SERVO SAMPLE' (4) IS ACTIVE, OR IF 'ENABLE SERVO SAMPLE' (4) AND 'HEAD CHANGE GATE' (5) ARE ACTIVE 'ENABLE SERVO SAMPLE' (4), WHICH IS ACTIVE FOR THE WHOLE OF THE SAMPLE SERVO FIELD, REDUCES THE GAIN OF THE AGC AMPLIFIER (TO WITHIN THE LIMITS (6) SHOWN ON THE TIMING DIAGRAM) IN OPERATIONS OUTSIDE THE SAMPLE SERVO FIELD. THE 'HEAD CHANCE GATE' (5) COMPENSATES FOR HEAD RESPONSE DURING A HEAD-CHANGE OPERATION.

IF THE AGC VOLTAGE IS EITHER TOO SMALL, OR ABSENT COMPLETELY, AN AGC DETECTOR CAUSES THE AMPLIFIER TO GIVE AN 'OUTSIDE AGC WINDOW' OUTPUT SIGNAL (6), WHICH IS INDICATED A 'TAG 111' (THAT IS, TAG 7) DIAGNOSTIC DATA.

THE GAIN STORE CAPACITOR C2 IS RESET AFTER THE END OF THE SERVO GAIN FIELD, WHEN THE '-RESET CAPACITOR' SIGNAL (7) IS ACTIVATED.

SERVO ERROR FIELD

THE SERVO ERROR FIELD IS 4.5 BYTES OF THE 22-BYTE SERVO SAMPLE FIELD. DURING THE SERVO ERROR FIELD, THE SERVO ERROR CIRCUIT MEASURES THE AMOUNT AND DIRECTION (EITHER IN OR OUT) THAT THE HEAD IS OFF TRACK, AND PRODUCES A 'DATA POSITION ERROR' SIGNAL THAT CORRESPONDS TO THE ERROR. THIS SIGNAL RETURNS THE HEAD ON TRACK TO READ OR WRITE DATA IN THE PARTICULAR SECTOR.

BEFORE THE SERVO ERROR FIELD OF A PARTICULAR SECTOR IS ENTERED, THE ERROR CAPACITOR C1 IS RESET BY 'RESET CAPACITOR' APPLIED TO IT THROUGH THE CIRCUIT. THEREFORE, NO VOLTAGE IS ACROSS C1. THUS THE 'DATA POSITION ERROR' SIGNAL FOR THE PREVIOUS SECTOR IS REMOVED.

IF A HEAD IS OFF-TRACK WHEN THE SERVO ERROR FIELD IS ENTERED, THE RESULTING ERROR SIGNAL CAUSES THE DEMODULATOR TO PRODUCE AN 'ERROR SAMPLE' SIGNAL. THE 'ERROR SAMPLE' IS SYNCHRONOUSLY RECTIFIED BY 'SELECT DEMOD A' AND 'SELECT DEMOD B' SYNCHRONIZED TO THE LINEAR SIGNAL ZERO CROSSINGS. THE RECTIFIED SAMPLE SIGNAL IS APPLIED TO THE ERROR CAPACITOR C1, CHARGING C1, OVER THE PERIOD OF THE SERVO ERROR FIELD, TO A LEVEL THAT CORRESPONDS TO THE AMOUNT OF ERROR. THE '+SELECT DEMOD A' AND '+SELECT DEMOD B' PULSES ARE SWITCHED ALTERNATELY ON AND OFF WITH RESPECT TO EACH OTHER, AT TIMES DETERMINED BY THE DECODING AND GATING OUTPUT OF COUNTER 2. THE POLARITIES OF THESE DEMODULATOR SIGNALS DEPEND ON WHETHER THE TRACK IS ODD OR EVEN NUMBERED.

THE ERROR VOLTAGE ON C1 IS APPLIED TO THE OPERATIONAL AMPLIFIER, SWITCHED AS A VOLTAGE FOLLOWER BY THE '+ENABLE DATA' AND '-ENABLE DATA' INPUTS, AND THE OPERATIONAL AMPLIFIER PROVIDES THE 'DATA POSITION ERROR SIGNAL AT ITS OUTPUT.

THE 'DATA POSITION ERROR' SIGNAL IS APPLIED TO THE HEAD ACTUATOR COIL VIA A COMPENSATOR CIRCUIT (NOT SHOWN). THIS MOVES THE HEAD TO THE ON-TRACK POSITION SO THAT THE DATA FIELD THAT FOLLOWS THE SERVO ERROR FIELD, WITHIN THE SAME SECTOR, CAN BE READ OR WRITTEN.

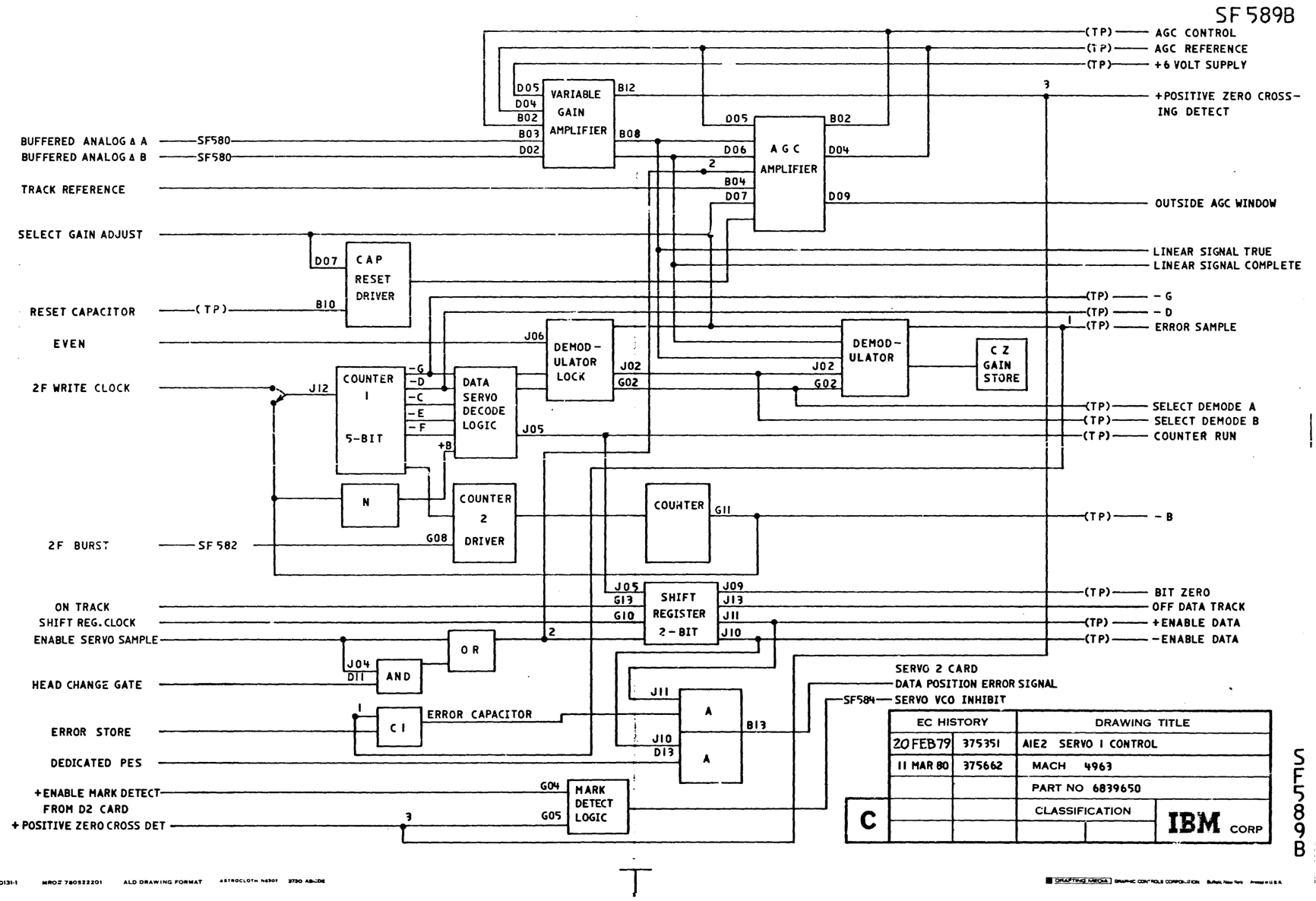
TIMING REFERENCE

TIMING IN THE SAMPLE SERVO FIELD, BETWEEN THE BEGINNING OF THE ID MARKER FIELD AND THE END OF THE SERVO ERROR FIELD, IS BASED ON A REFERENCE FREQUENCY PROVIDED BY THE DEDICATED SERVO HEAD. PHASE CORRECTION OF THIS FREQUENCY IS PROVIDED BY THE MARK DETECT LOGIC CIRCUIT.

EC HISTORY		DRAWING TITLE
20 FEB 79	375351	AIE2 SERVO 1 CONTROL
		MACH 4963
		PART NO 6839649
		CLASSIFICATION
C		IBM CORP

SF589A

SF 589B



EC HISTORY		DRAWING TITLE
20 FEB 79	375351	AIE2 SERVO 1 CONTROL
11 MAR 80	375662	MACH 4963
		PART NO 6839650
		CLASSIFICATION

C

IBM CORP

SF589B

SF589B

620-0131-1 MROZ 780522201 ALD DRAWING FORMAT ASTROCLOTH N6307 3730 ABLIDE

DRAFTING MEDIA GRAPHIC CONTROLS CORPORATION Buffalo, New York Printed in U.S.A.

SERVO 1 (E2)

SAMPLE SERVO MARKER FIELD

MARKER FIELD

THE ALTERNATING PEAKS IN THE 'OFF TRACK' SIGNAL MEASURE OFF-TRACK ERROR. THE PEAKS ARE SYNCHRONOUSLY RECTIFIED IN RELATION TO A SQUARE WAVE SIGNAL (G02, J02) SYNCHRONIZED TO THE LINEAR SIGNAL ZERO CROSSINGS. THIS PRODUCES A SIGNAL, PROPORTIONAL TO THE OFF TRACK ERROR, THAT IS USED TO POSITION THE HEADS CORRECTLY OVER THE PARTICULAR TRACK.

THE OUTPUT OF THE MARK DETECTOR RELEASES THE VOLTAGE CONTROLLED OSCILLATOR (VCO) FROM THE CONTROL OF THE DEDICATED SERVO SURFACE, TO WHICH IT WAS PHASE-LOCKED. THE VCO FREE RUNS AT THE RELEASE FREQUENCY FOR THE 10 MICROSECOND PERIOD OF THE SERVO GAIN AND ERROR FIELDS. DURING THAT PERIOD, THE VCO OUTPUT GENERATES THE CONTROL AND GATING SIGNALS.

NOTE: ANY SMALL VELOCITY ERROR DURING THIS PERIOD CAN BE IGNORED.

THE SIGNALS '+ SELECT GAIN ADJUST', '– RESET CAPACITOR', '+ SELECT DEMOD A' AND '+ SELECT DEMOD B' ARE DERIVED BY DECODING THE OUTPUTS OF COUNTER 1 AND COUNTER 2 (FIVE-BIT COUNTERS). THESE COUNTERS ARE CONTROLLED BY THE 'CONTROL RUN' LINE THAT IS ACTIVATED AT A POINT ON THE SAMPLE SERVO SIGNAL (MARKER).

THE COUNTER:

- CONTROLS A LOGIC SWITCH IN THE CLOCK CONTROL. THE SWITCH CONNECTS EITHER '2F WRITE CLOCK', OR THE OUTPUT OF COUNTER 2 INTO THE CLOCK INPUT OF COUNTER 1.
- INHIBITS THE ANALOG CONTROL SIGNALS (WHEN THE COUNTER IS DEACTIVATED).

WHEN 'COUNTER RUN' IS DEACTIVATED, COUNTER 1 RUNS FROM THE START OF 'ENABLE MARK DETECT', AND RESETS AT EVERY CHANGE OF '+ POSITIVE ZERO CROSSING'. IF THE COUNTER 1 REACHES A COUNT OF '–F', THE NEXT ZERO CROSSING SETS '+ SERVO VCO INHIBIT', AND RESETS THE COUNTER 1.

IF THE NEXT ZERO CROSSING OCCURS WHEN '–F' IS NOT ACTIVE, THE SERVO MARKER IS RECOGNIZED, '+ SERVO VCO INHIBIT' IS RESET, AND 'COUNTER RUN' IS ACTIVATED.

'SERVO VCO INHIBIT' RELEASES CONTROL OF THE VCO. FROM THE DEDICATED SERVO SURFACE, THE VCO THEN PRODUCES THE '2F BURST'. 'COUNTER RUN' SWITCHES THE COUNTER 1 'CLOCK' TO THE OUTPUT OF COUNTER 2. COUNTER 1, WHICH DIVIDES BY SIX, IS DRIVEN BY '2F BURST', VIA A SINGLE BIT COUNT IN COUNTER 2, AND ADVANCES ON BOTH POLARITIES OF THE INPUT SIGNAL.

WHEN 'COUNTER RUN' IS ACTIVE, IT ALSO INHIBITS THE RESET OF COUNTER 1, AND ALLOWS ANALOG CONTROL DECODE TO OPERATE. THIS PRODUCES GAIN, DEMODULATOR AND RESET CAPACITOR SIGNALS.

THE 'SELECT GAIN ADJUST' LINE IS CONTROLLED BY 'DEFAULT GATE' OR 'HEAD CHANGE GATE'. A TWO-BIT SHIFT REGISTER CONTROLS THE 'ENABLE DATA' LINES.

'COUNTER RUN' APPLIED TO THE SHIFT REGISTER INDICATES THAT A SAMPLE HAS BEEN FOUND THAT IS CLOCKED BY '+ SHIFT REGISTER CLOCK'. A SIGNAL DERIVED FROM THE DEDICATED SERVO SURFACE. THE GATING CAUSES 'ENABLE DATA' TO BE ACTIVATED ON THE SECOND SAMPLE FOUND AND DEACTIVATED ON THE THIRD SAMPLE FOUND.

EC HISTORY		DRAWING TITLE
20 FEB 79	375351	AIE2 SERVO 1 CONTROL
		MACH 4963
		PART NO 6839651
		CLASSIFICATION

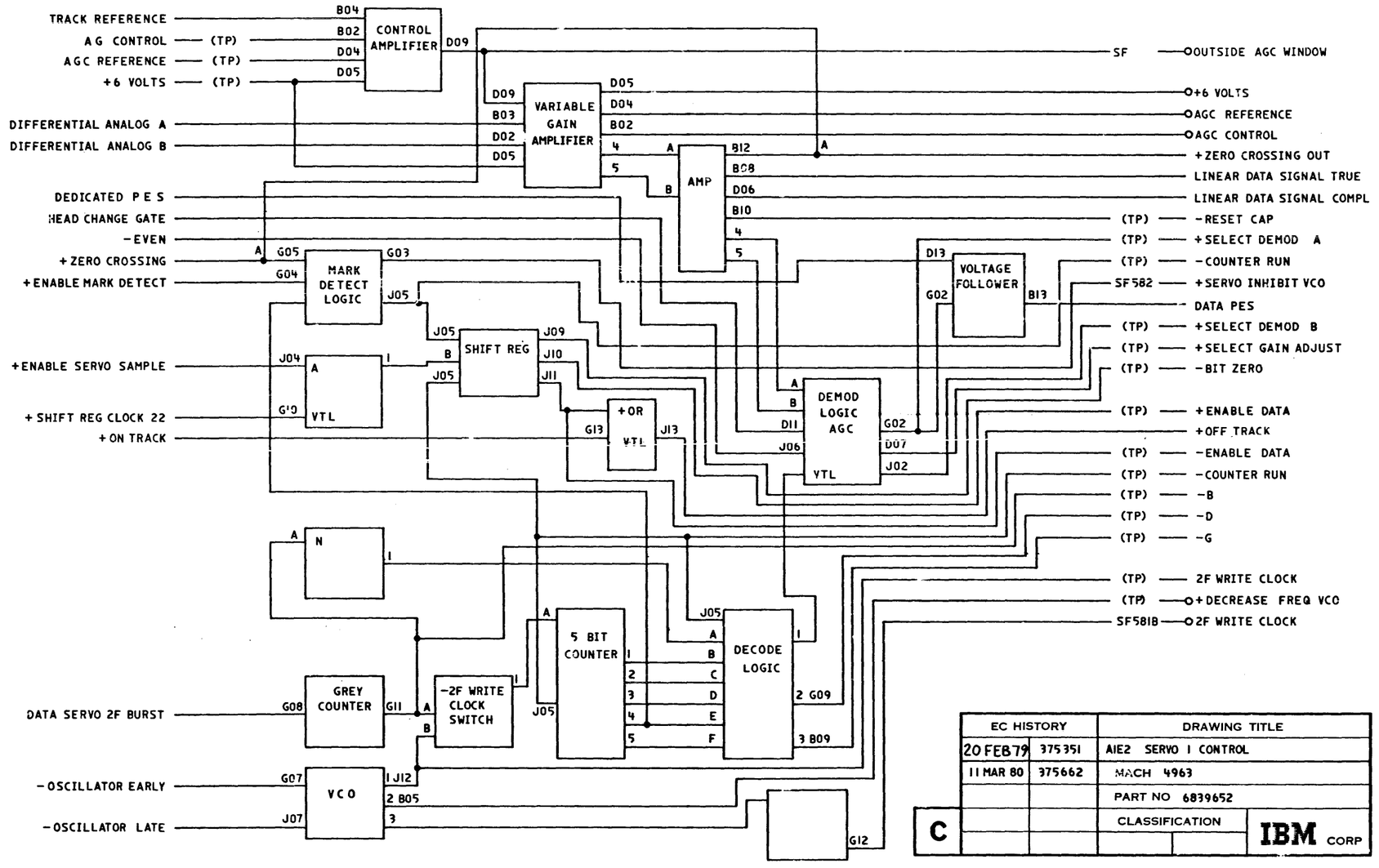
.C

IBM CORP

SF590A

SF590A

SF5908



EC HISTORY		DRAWING TITLE
20 FEB 79	375351	AIE2 SERVO I CONTROL
11 MAR 80	375662	MACH 4963
		PART NO 6839652
		CLASSIFICATION

C

IBM CORP

SF5908

SF5908

SF591

SERVO 2 LOCATION F2

THIS CARD CONSISTS OF FIXED AND VARIABLE GAIN AMPLIFIERS TO AMPLIFY THE DIFFERENTIAL OUTPUT FROM THE DEDICATED SERVO READ HEADS TO A CONSTANT OUTPUT LEVEL. INCLUDED IS CIRCUITRY TO DETECT SERVO CLOCK PULSES WHICH FIRE A 280 msec SINGLE SHOT.

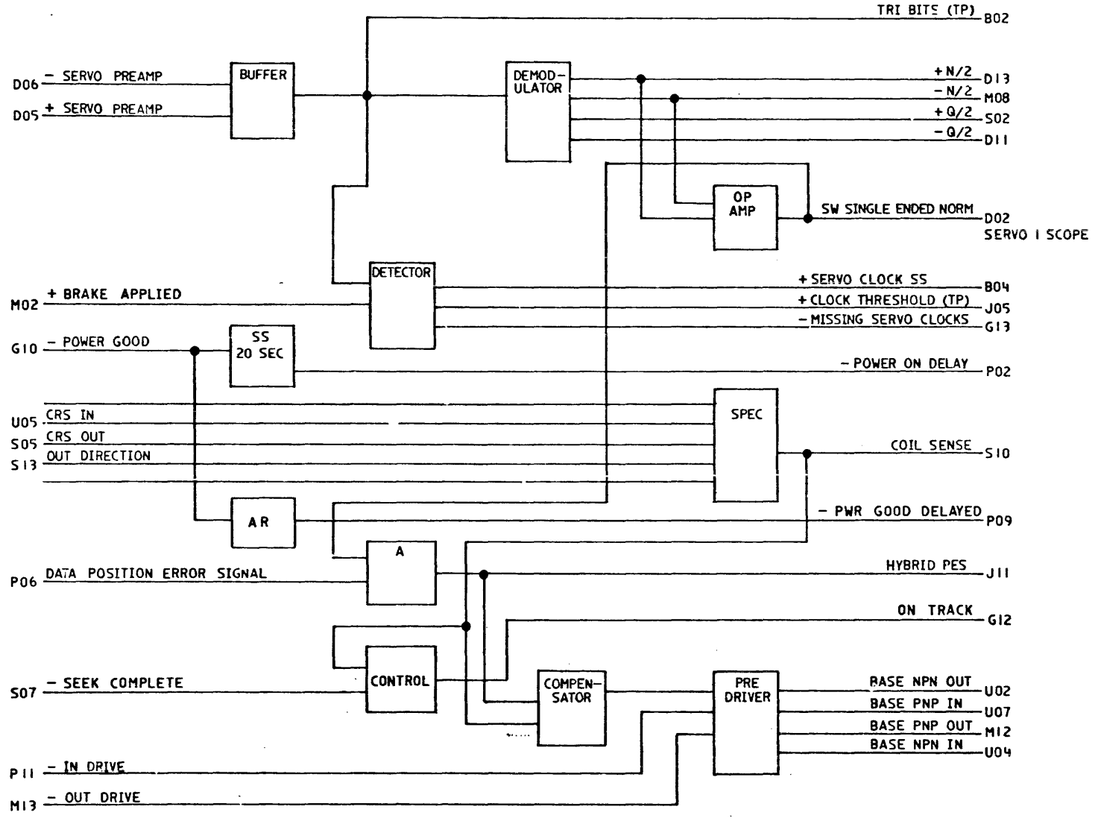
PEAKS ON THE AMPLIFIED OUTPUT ARE DETECTED AND SELECTED BY THE SEL N1, N2, Q1 AND Q2 LINES INTO THEIR RESPECTIVE ±N/2 AND ±Q/2 OUTPUTS, CORRESPONDING TO THE NORMAL AND QUADRATURE FIELDS RECORDED ON THE SERVO SURFACE.

THE N SIGNALS AND THE Q SIGNALS ARE FED TO BUFFERS. THE INPUT IS HOWEVER INVERTED TO ONE BUFFER. SERVO SIGNALS ON THE DEDICATED SURFACES ARE INVERTED IN PHASE ON ALTERNATE TRACKS WHICH ALLOW SELECTION OF THE CORRECT POLARITY OF THE OUTPUT SIGNAL. "DATA PES" FROM SERVO 1 IS COMBINED TO FORM A "HYBRID PES O/P".

THE "DELAY" IN "POWER GOOD DELAYED" IS OF THE ORDER OF μsecs AND ENTIRELY DUE TO CIRCUIT DELAYS IN THE FILTERS.

THE VOLTAGES DEVELOPED ACROSS CURRENT SENSE RESISTORS (CSR) ON THE D.E. DRIVE BOARD TO DETECT LOW VOICE COIL MOTOR CURRENT. "+OUT DIRECTION" CONTROLS THE INPUT POLARITY TO ENSURE CORRECT OUTPUT FOR BOTH DIRECTIONS OF ACCESS ARM TRAVEL. VCM START AND FINISH ARE DIRECT CONNECTION TO THE VOICE COIL WINDINGS AND PROVIDE COMPENSATION TO THE AMPLIFIER. "VOICE COIL CURRENT SIGNAL" IS A VOLTAGE LEVEL WHICH IS PROPORTIONAL TO THE VOICE COIL CURRENT. THE VOICE COIL CURRENT SIGNAL IS AMPLIFIED WHEN "SEEK COMPLETE" IS ACTIVE AND ENSURES THAT THERE IS MINIMAL VOICE COIL CURRENT. "+ ON TRACK" DROPS IF SUFFICIENT VOICE COIL CURRENT IS DETECTED TO MOVE THE ACCESS ARM OFF TRACK.

"HYBRID PES." "±SEL INT" PROVIDES CONTROL OF A CAPACITOR WHICH HOLDS THE "HYBRID PES" LEVEL CONSTANT DURING ACCESSING TO REDUCE TRANSIENTS AT ACCESS COMPLETION. THE SIGNAL DRIVES THE VOICE COIL MOTOR TRANSISTOR MATRIX. "-IN DRIVE" AND "-OUT DRIVE" OVERRIDE THE INPUT SIGNAL AND FORCE THE ACCESS DRIVE INTO FULL IN OR OUT MOTION.



EC HISTORY		DRAWING TITLE
20FEB79	375351	AIF2 SERVO 2 CARD
		MACH 4963
		PART NO 6839653
C		CLASSIFICATION

IBM CORP

SF591

SF591

820-0131-0 MROJ 780822501 ALD DRAWING FORMAT ASTROCLOTH N660T 8-79

GRAPHIC CONTROLS CORPORATION Buffalo, New York Printed in U.S.A.

NOTE: SCOPE PICTURES GO WITH MAP 7A74

SF599

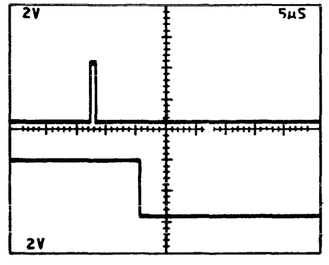


FIGURE 1

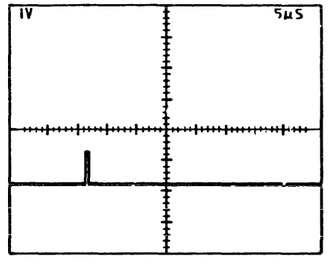


FIGURE 2

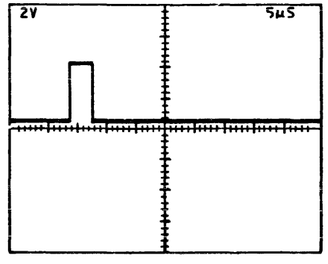


FIGURE 3

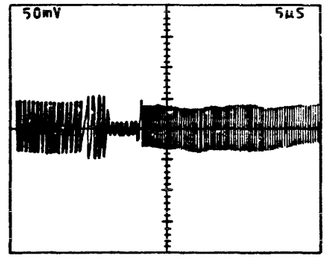


FIGURE 4

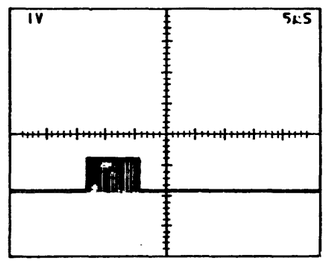


FIGURE 5

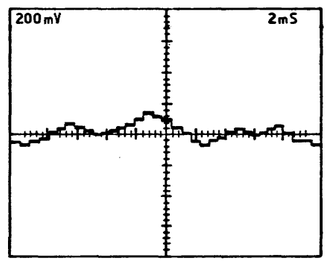


FIGURE 6

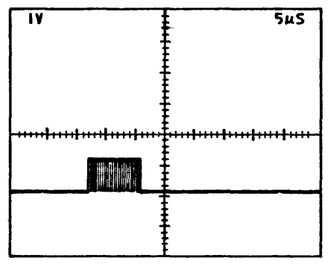


FIGURE 7

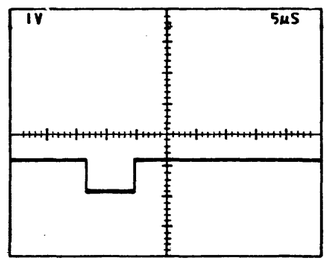


FIGURE 8

SF599

EC HISTORY		DRAWING TITLE	
9APR80	375662	MAP 7A74 SCOPE PICTURES	
		MACH 4963	
		PART NO 6846296	
C		CLASSIFICATION	IBM CORP

SF599

AIC2 – LOGIC I – OUTPUT

	PIN	LINE NAME	SYNC	PAGE
SF554	U13	+ PARITY ERROR	–	TP
	S09	+ EVEN	– F2B03 (E2J06)	SF570 (SF568)
	S07	– SET SEEK	– D2M12	SF562
	S04	– COMMON RESET	–	TP
	U12	+ WRITE SELECT	–B2G13(E1C13)	SF551
	J12	+ READ SELECT	–B2J12 (F1C11)	SF550
	U09	+ COMMON RESET	–B2M03	SF550
	S11	– SERVO UNSAFE	–B2M02	SF550
	G11	+ WRITE BLOCK	–B2J06	SF550
	S12	+ DATA SFL GATED	–A2B13	SF527
	D06	– INTERRUPT	–A5B04	SF503
SF555	P05	–BUS BIT 6	–A4D11(A3D11)	SF (SF505)
	M06	–BUS BIT 7	–A4D12(A3D12)	SF (SF505)
	B05	– TAG 010 CS	–	TP
	G06	– TAG NO FIXED HEAD	–	TP
	M12	+ HEAD I SELECTED	– D2P09	SF562
	D07	– TAG CLOCK 2	– D2509	SF565
	P09	– CONT SAMPLE REC'D	– A3B12	SF505

AIC2 LOGIC I – OUTPUT

	PIN	LINE NAME	SYNC	PAGE
SF556	G04	– GO HOME BIT	– D2 P12	SF562
	D10	+ REL TRK ADDRESS	–	TP
	D09	– FIXED HEAD SEL	– D2J04(B2M05)	SF565(SF550)
	M04	– BUS BIT 0	–A4D04(A3D04)	SF505
	P02	– BUS BIT 1	–A4D05 (A3D05)	SF505
	G02	– HEAD REG 8	–B2F06	SF550
	J06	– HEAD REG 4	–B2P10	SF550
	M03	–BUS BIT 2	– A4D06(A3D06)	SF505
	M02	–BUS BIT 3	– A4D07 (A3D07)	SF505
	P10	– HEAD REG 2	–B2P05	SF550
	P12	– HEAD REG 1	–B2P07	SF550
	P06	–BUS BIT 5	–A4D10(AD10)	SF505
	M05	–BUS BIT 4	–A4D09(A3D09)	SF505
SF557	J10	+ 1/2 TTG		
	B13	– SHIFT	–D2504	SF565
	D05	– RESET CAL	–D2P11	SF562
	J05	+OUT	–D2U02	SF562
	G05	– CAL ADDRESS	–D2M08	SF562
	J04	+TRACK UNAVAILABLE	–	TP(SF557)
	P04	– BUS PARITY BIT OUT	–A4D13 (A3D13)	SF505

SF559B

EC HISTORY		DRAWING TITLE
20FEB79	375351	AIC2 LOGIC I
11 MAR 80	375662	MACH 4963
		PART NO 6839612
		CLASSIFICATION

C

IBM CORP

SF559B

4966 DISKETTE MAGAZINE ATTACHMENT CARD

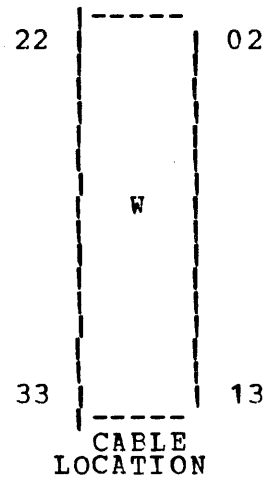
STANDARD CHANNEL

```
  ADDRESS BUS BIT--00------B02
  ADDRESS BUS BIT--01------B03
  ADDRESS BUS BIT--02------B04
  ADDRESS BUS BIT--03------B05
  ADDRESS BUS BIT--04------B07
  ADDRESS BUS BIT--05------B08
  ADDRESS BUS BIT--06------B09
  ADDRESS BUS BIT--07------B10
  ADDRESS BUS BIT--08------B12
  ADDRESS BUS BIT--09------D02
  ADDRESS BUS BIT--10------D04
  ADDRESS BUS BIT--11------D05
  ADDRESS BUS BIT--12------D06
  ADDRESS BUS BIT--13------D07
  ADDRESS BUS BIT--14------D09
  ADDRESS BUS BIT--15------D10
  ADDRESS BUS BIT--16------D11
  ADDRESS GATE-------------M08
  ADDRESS GATE RETURN------M09
# BURST RETURN------------(P04)
  CONDITION CODE IN BIT-00-D12
  CONDITION CODE IN BIT-01-D13
  CONDITION CODE IN BIT-02-B13
  CYCLE BYTE INDICATOR-----P10
  CYCLE INPUT INDICATOR----P09
  CYCLE STEAL REQUEST IN---M02
  DATA BUS BIT-----00------G02
  DATA BUS BIT-----01------G03
  DATA BUS BIT-----02------G04
  DATA BUS BIT-----03------G05
  DATA BUS BIT-----04------G07
  DATA BUS BIT-----05------G08
  DATA BUS BIT-----06------G09
  DATA BUS BIT-----07------G10
  DATA BUS BIT-----P0------G12
  DATA BUS BIT-----08------J02
  DATA BUS BIT-----09------J04
  DATA BUS BIT-----10------J05
  DATA BUS BIT-----11------J06
  DATA BUS BIT-----12------J07
  DATA BUS BIT-----13------J09
  DATA BUS BIT-----14------J10
  DATA BUS BIT-----15------J11
  DATA BUS BIT-----P1------J12
  DATA STROBE--------------M10
  HALT OR MCHK-------------M07
  INITIATE IPL-------------P07
  IPL----------------------S04
  POLL---------------------M12
  POLL IDENTIFIER BIT--00--P11
  POLL IDENTIFIER BIT--01--S02
  POLL IDENTIFIER BIT--02--S03
  POLL IDENTIFIER BIT--03--P12
  POLL IDENTIFIER BIT--04--P13
  POLL PRIME---------------M13
  POLL PROPAGATE-----------M11
  POLL RETURN--------------M04
  POWER ON RESET-----------S05
  REQUEST IN BUS BIT--00---S07
  REQUEST IN BUS BIT--01---S08
  REQUEST IN BUS BIT--02---S09
  REQUEST IN BUS BIT--03---S10
  REQUEST IN BUS BIT--04---S12
  REQUEST IN BUS BIT--05---S13
  REQUEST IN BUS BIT--06---U02
  REQUEST IN BUS BIT--07---U04
  REQUEST IN BUS BIT--08---U05
  REQUEST IN BUS BIT--09---U06
  REQUEST IN BUS BIT--10---U07
  REQUEST IN BUS BIT--11---U09
  REQUEST IN BUS BIT--12---U10
  REQUEST IN BUS BIT--13---U11
  REQUEST IN BUS BIT--14---U12
  REQUEST IN BUS BIT--15---U13
  SERVICE GATE-------------P05
  SERVICE GATE RETURN------P06
  STATUS BUS BIT-------00---J13
  STATUS BUS BIT-------01---G13
  STATUS BUS BIT-------02---M03
  STATUS BUS BIT-------03---P02
  SYSTEM RESET-------------M05
```

4966 TOP CARD CONNECTOR

```
                  DRIVE          - AUTOLOADER
W 02-- +ACCESS 0                 | +COMMAND 0
W 03-- +ACCESS 1                 | +COMMAND 1
W 04-- +ACCESS 2                 | +COMMAND 2
W 05-- +ACCESS 3                 | +COMMAND 3
W 06--          +ENABLE AUTOLOADER
W 07--          +4F CLOCK PHASE 1 OUT
W 08--                GROUND
W 09--          +STANDARD CLOCK OUT
W 10--          +STANDERD DATA OUT
W 11--          +STATUS A
W 12-- +SWITCH FILTER            | +COMMAND 4
W 13--                +INDEX
W 22--          - NOT AVAILABLE -
W 23-- +WRITE DATA               | CLOCK(500KHZ)
W 24--          +ERASE GATE
W 25--          +WRITE GATE
W 26-- +INNER TRACKS             | +COMMAND 5
W 27-- +SELECT HEAD              | +COMMAND P
W 28-- +DISKETTE 2 SENCE         | +STATUS B
W 29-- +ERASE CUR. SENCE         | +STATUS C
W 30--          +VFO DATA SYNC IN
W 31--          +MFM MODE IN
W 32--          +COVER OPEN
W 33-- -WRAP                     | +STATUS D
```

TOP CARD CONNECTOR



CABLE LOCATION

VOLTAGE PIN ASSIGNMENTS
+5V---D03--J03--P03--U03
GND---D08--J08--P08--U08
+8.5V-G11

\# LINES ARE NOT USED BY THIS ATTACHMENT.

SEE 4966 THEORY DIAGRAMS MANUAL FOR DATA FLOW

4966 DISKETTE MAGAZINE

E.C. HISTORY MACH. 4966

IBM CORP. GSD

DATE 09-05-78 LAST E.C. 755551B P.N. 6838044

SF6000

0 0 0

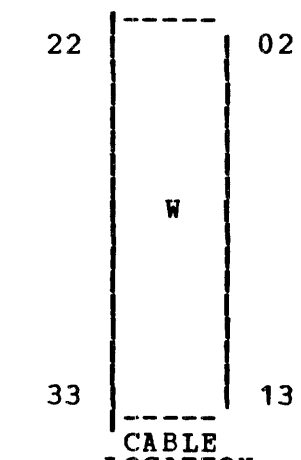
4966 DISKETTE MAGAZINE ATTACHMENT CABLE

4966 DISKETTE MAGAZINE
ATTACHMENT CABLE
PIN ASSIGNMENTS

4966 DISKETTE MAGAZINE
DISKETTE CABLE
PIN ASSIGNMENTS

	DRIVE	-	AUTOLOADER	
W 02--	+ACCESS 0		+COMMAND 0	--D 02
W 03--	+ACCESS 1		+COMMAND 1	--D 03
W 04--	+ACCESS 2		+COMMAND 2	--D 04
W 05--	+ACCESS 3		+COMMAND 3	--D 05
W 06--	+ENABLE AUTOLOADER			--D 06
W 07--	+4F CLOCK PHASE 1 OUT			--D 07
W 08--	GROUND			--D 08
W 09--	+STANDARD CLOCK OUT			--D 09
W 10--	+STANDERD DATA OUT			--D 10
W 11--	+STATUS A			--D 11
W 12--	+SWITCH FILTER		+COMMAND 4	--D 12
W 13--	+INDEX			--D 13
W 22--	- NOT AVAILABLE -			--B 02
W 23--	+WRITE DATA		CLOCK(500KHZ)	--B 03
W 24--	+ERASE GATE			--B 04
W 25--	+WRITE GATE			--B 05
W 26--	+INNER TRACKS		+COMMAND 5	--B 06
W 27--	+SELECT HEAD		+COMMAND P	--B 07
W 28--	+DISKETTE 2 SENCE		+STATUS B	--B 08
W 29--	+ERASE CUR. SENCE		+STATUS C	--B 09
W 30--	+VFO DATA SYNC IN			--B 10
W 31--	+MFM MODE IN			--B 11
W 32--	+COVER OPEN			--B 12
W 33--	-WRAP		+STATUS D	--B 13

PROCESSOR ATTACHMENT
TOP CARD CONNECTOR



SEE 4966 THEORY DIAGRAMS
MANUAL FOR DATA FLOW

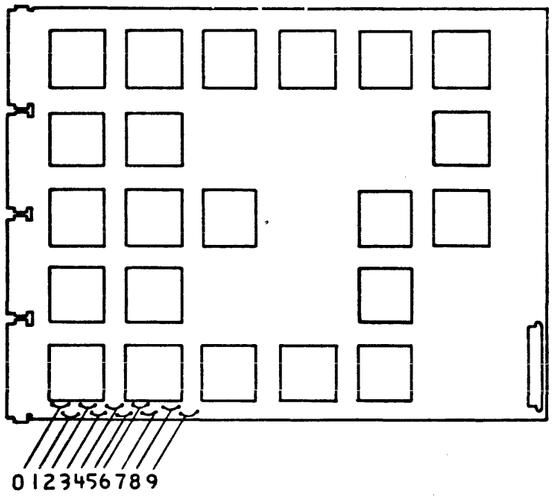
4966 DISKETTE MAGAZINE
ATTACHMENT CARD

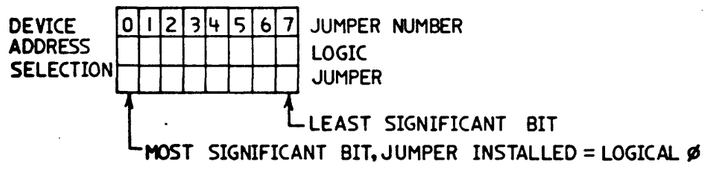
E.C. HISTORY MACH. 4966

IBM CORP. GSD

DATE 09-05-78 LAST E.C. 755551B P.N. 6838045

SF6100 000





NOTES:

1 JUMPER 8 INSTALLED MEANS CARD IS ALTERNATE IPL SOURCE.
JUMPER 9 INSTALLED MEANS CARD IS PRIMARY IPL SOURCE.
NEITHER JUMPER INSTALLED MEANS IPL IS DISABLED.

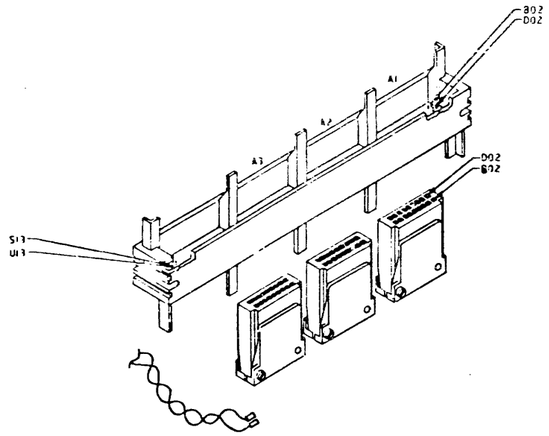
2 ATTACHMENT CARD DEVICE ID = 0126 = 0000 0001 0010 0110

EC HISTORY		DRAWING TITLE
31AUG 78	7555518	CARD JUMPERS
		MACH
		PART NO 6838046
		CLASSIFICATION

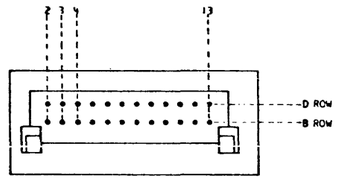
C

IBM CORP

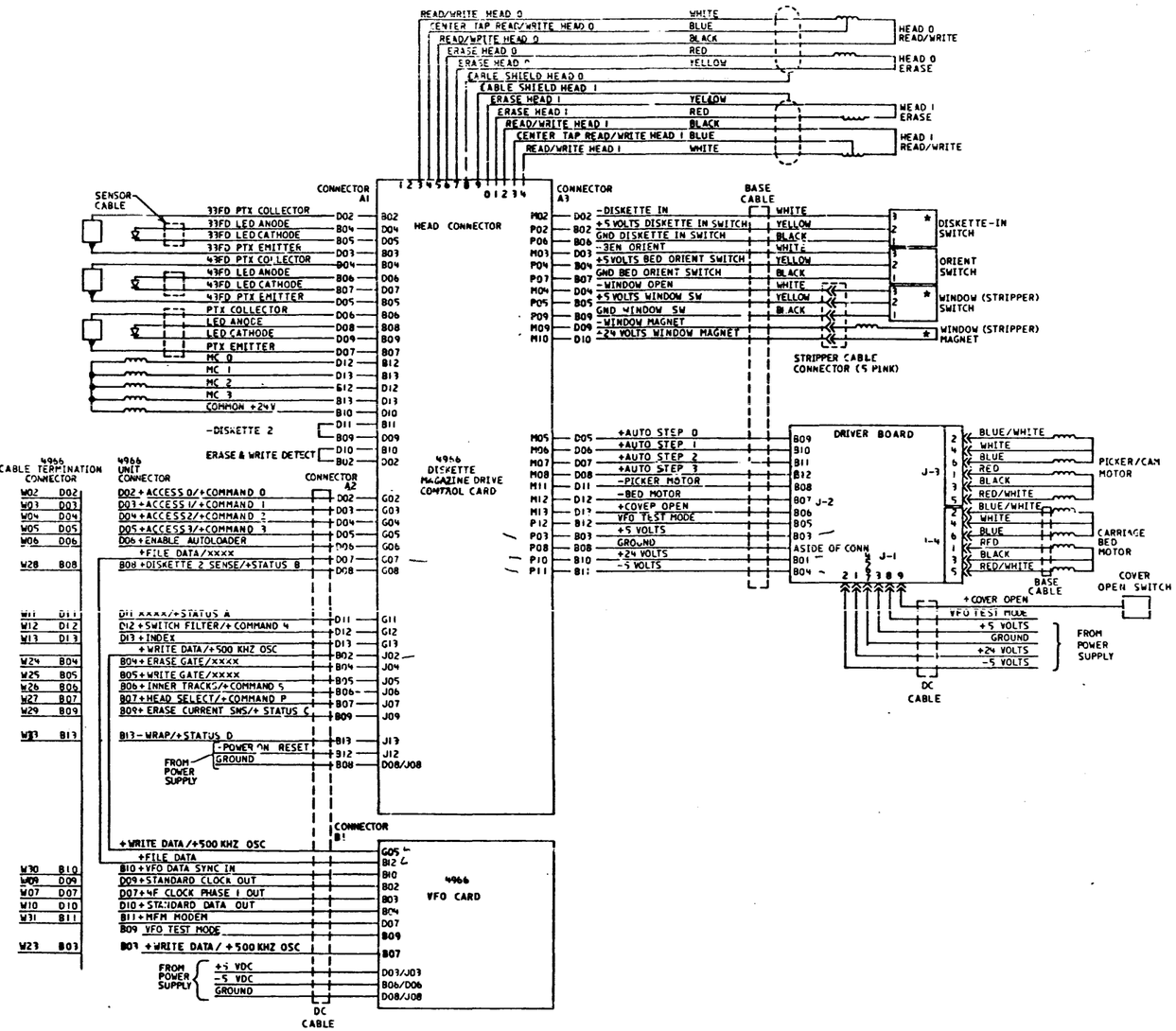
SF620



4966 DISKETTE MAGAZINE DRIVE CONTROL CARD SOCKET



4966 DISKETTE MAGAZINE UNIT CABLE TERMINATION SOCKET



* - NOT USED ON MACHINES WITHOUT A STRIPPER ASM.
(SEE MIM PARA. 2.3 FOR LOCATION OF STRIPPER ASM.)

SF630

EC HISTORY		DRAWING TITLE
31 AUG 78	755551B	DISKETTE MAGAZINE U/C LINES
29 JAN 79	375255	MACH
6 OCT 7[illegible]	375397	PART NO 6838047
26 JUN 80	877049	CLASSIFICATION

D

IBM CORP

SF630

SF640

TPA-1	33 FD LED ANODE	**
TPA-2	43 FD LED ANODE	
TPA-3	+24 VOLTS	
TPA-4	HEAD MOTOR MC-2 (YELLOW)	
TPA-5	HEAD MOTOR MC-3 (BLUE)	
TPA-6	+WRITE DATA/+500 kHz OSC	
TPA-7	+ERASE GATE	
TPA-8	+WRITE GATE	
TPA-9	+INNER TRACKS/+COMMAND 5	
TPA-10	+HEAD SELECT/ +COMMAND P	
TPA-11	+ERASE CURRENT SENSE/+STATUS C	
TPA-12	+STATUS D	
TPA-13	GROUND	
TPA-14	-5 VOLTS	
TPA-15	+5 VOLTS	

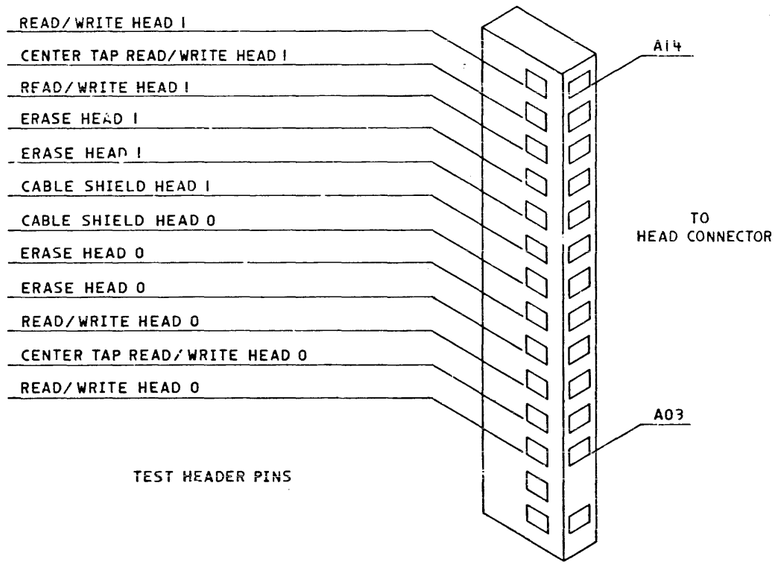
TPB-1	33 FD PTX EMITTER	**
TPB-2	43 FD PTX EMITTER	
TPB-3	PICKER PTX COLLECTOR	
TPB-4	PICKER LED ANODE	
TPB-5	HEAD MOTOR MC-0 (ORANGE)	
TPB-6	HEAD MOTOR MC-1 (RED)	
TPB-7	+ACCESS 0/+COMMAND 0	
TPB-8	+ACCESS 1/+COMMAND 1	
TPB-9	+ACCESS 2/+COMMAND 2	
TPB-10	+ACCESS 3/+COMMAND 3	
TPB-11	+ENABLE AUTOLOADER	
TPB-12	+FILE DATA/XXXX	
TPB-13	+DISKETTE 2/+STATUS B	
TPB-14	+STATUS A	
TPB-15	+SWITCH FILTER/+COMMAND 4	
TPB-16	+INDEX	
TPB-17	-BED ORIENT SWITCH	
TPB-18	+AUTO STEP 0	
TPB-19	+AUTO STEP 1	
TPB-20	+AUTO STEP 2	
TPB-21	+AUTO STEP 3	
TPB-22	-PICKER MOTOR	
TPB-23	-BED MOTOR	
TPB-24	+COVER OPEN	

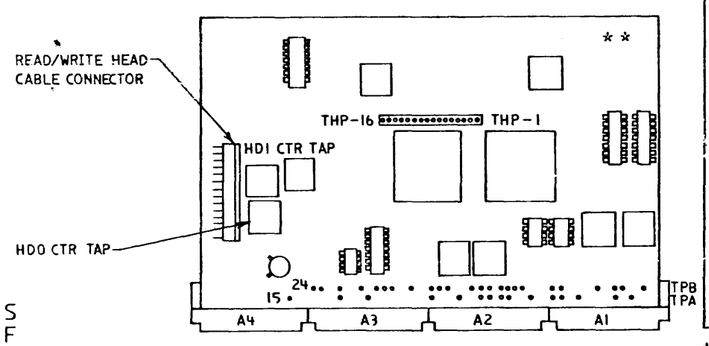
TPA-1	33 FD LED ANODE	*
TPA-2	43 FD LED ANODE	
TPA-3	HEAD MOTOR MC-2 (YELLOW)	
TPA-4	HEAD MOTOR MC-3 (BLUE)	
TPA-5	+WRITE DATA/+500 kHz OSC	
TPA-6	+ERASE GATE	
TPA-7	+WRITE GATE	
TPA-8	+INNER TRACKS/+COMMAND 5	
TPA-9	+HEAD SELECT/+COMMAND P	
TPA-10	+ERASE CURRENT SENSE/+STATUS C	
TPA-11	+5 VOLTS // 0	
TPA-12	GROUND	
TPA-13	+24 VOLTS	
TPA-14	-5 VOLTS	

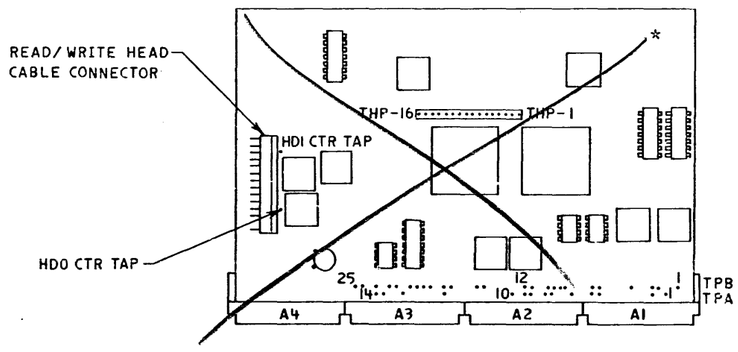
THP-1	GROUND	***
THP-2	HEAD REFERENCE (CE MODE)	
THP-3	SINGLE STEP PICKER	
THP-4	SINGLE STEP BED	
THP-5	PICKER EXTENDED	
THP-6	-AGC OUT	
THP-7	+AGC OUT	
THP-8	GROUND	
THP-9	CONTROL VOLTAGE	
THP-10		
THP-11		
THP-12	+14.3 VOLTS	
THP-13		
THP-14	-VGA IN PREAMP TP-1	
THP-15	+VGA IN PREAMP TP-2	
THP-16	GROUND	

TPB-1	33 FD PTX EMITTER	*
TPB-2	43 FD PTX EMITTER	
TPB-3	PICKER PTX COLLECTOR	
TPB-4	PICKER LED ANODE	
TPB-5	HEAD MOTOR MC-0 (ORANGE)	
TPB-6	HEAD MOTOR MC-1 (RED)	
TPB-7	+ACCESS 0/+ COMMAND 0	
TPB-8	+ACCESS 1/+ COMMAND 1	
TPB-9	+ACCESS 2/+COMMAND 2	
TPB-10	+ACCESS 3/+COMMAND 3	
TPB-11	+ENABLE AUTOLOADER	
TPB-12	+FILE DATA/XXXX	
TPB-13	+SWITCH FILTER/+COMMAND 5	
TPB-14	+INDEX	
TPB-15	-DISKETTE IN	
TPB-16	-BED ORIENT SWITCH	
TPB-17	WINDOW OPEN	
TPB-18	+AUTO STEP 0	
TPB-19	+AUTO STEP 1	
TPB-20	+AUTO STEP 2	
TPB-21	+AUTO STEP 3	
TPB-22	-WINDOW MAGNET	
TPB-23	-PICKER MOTOR	
TPB-24	-BED MOTOR	
TPB-25	+COVER OPEN	

* -USE FOR MACHINES WITH A STRIPPER ASM
** -USE FOR MACHINES WITHOUT A STRIPPER ASM
***-USE ON ALL MACHINES
(SEE MIM PARA. 2.3 FOR LOCATION OF STRIPPER ASM)







EC HISTORY		DRAWING TITLE
	7555518	DISKETTE MAGAZINE CTRL CD
6 OCT 79	375397	MACH SERIES/1
		PART NO 6838048
		CLASSIFICATION
D		IBM CORP

SF640

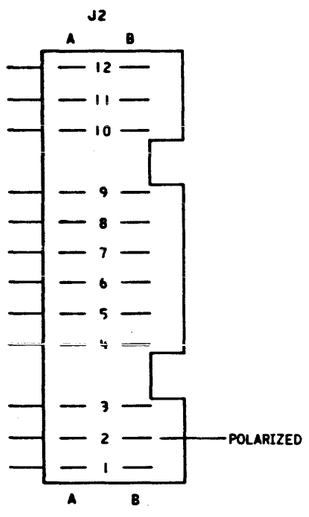
SF640

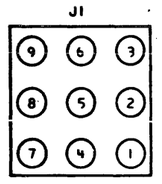
J1

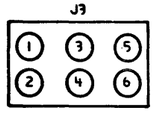
PIN	LINE NAME
1	+24V
2	-5V
3	+5V
4	GROUND
5	GROUND
6	GROUND
7	GROUND
8	VFO (TEST MODE)
9	+COVER OPEN

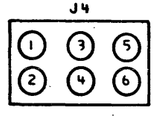
J2

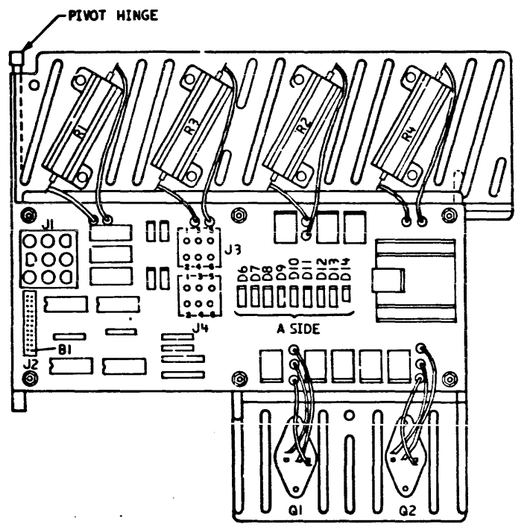
PIN	LINE NAME
A1	GROUND
A2	
A3	GROUND
A4	GROUND
A5	
A6	GROUND
A7	GROUND
A8	GROUND
A9	GROUND
A10	GROUND
A11	GROUND
A12	GROUND
B1	+24V
B2	
B3	+5V
B4	-5V
B5	VFO (TEST MODE)
B6	+COVER OPEN
B7	-BED MOTOR
B8	-PICKER MOTOR
B9	+AUTO STEP-0
B10	+AUTO STEP-1
B11	+AUTO STEP-2
B12	+AUTO STEP-3











EC HISTORY		DRAWING TITLE
31AUG78	755551B	DISKETTE MAG DRIVER BD
29JAN79	375255	MACH
		PART NO 6838049
		CLASSIFICATION

C

IBM CORP

SF650

SF650

SF660

4966 POWER SUPPLY

PC BOARD

INPUT POWER

GREEN/YELLOW

LINE FILTERS

R20 1MΩ LF1

R21 1MΩ LF2

ON/OFF SW1

BOX AC GROUND

F4 FUSE SLO-BLOW 3A 125V 1.5A 250V

TB1 60 HZ

1 COMMON
2 100 V AC
3 115 V AC
4 200 V AC
5 208 V AC
6 230 V AC
7

C4 FILTER CAP

T1 60 HZ TRANSFORMER

60 HZ

D6
D7

E1
E2

C1

F1 10A

J2

1 +5V
2 +5V RETURN
3 -5V RETURN
6 -5V
5 +24V
4 +24V RETURN

F2 1.0A

F3 6.25A

D1
D2
D3
D4

C2
C3

J1

E4 GROUND

1.8K
13K
7.5K
3.83K
2K
750Ω
6.8μF
5.6K
6.34K
D5 DN
1/4 MI
138

E3 -POR

200 Ω

E5 +POWER ON

TB1 50 HZ

TFMR 2462155

1 COMMON
2 100 VAC
3 110/112.5 VAC
4 123.5 VAC
5 200 VAC
6 220 VAC
7 235 VAC

T1 50 HZ

50 HZ

D6
D7

E1
E2

A J1

C4

8
20 CHASSIS GND

TRANSFORMER 50 HZ

J3

M 4966 DRIVE MOTOR

M 4966 FAN MOTOR

4966 GROUND

J2

4 +5V
5 +5V RETURN
6 -5V
9 -5V RETURN
8 +24 V
7 +24 V RETURN
2 GND
3 -POR
1 +POWER ON

NOTES:

1 FOR ALL 4966 MACHINES AT SERIAL NUMBER 60022 AND ABOVE USE THE J2 CONNECTOR DIAGRAM SHOWN ON THE RIGHT

EC HISTORY		DRAWING TITLE
31 AUG 78	755551B	4966 POWER SUPPLY
29 JAN 79	375255	MACH SERIES/1
		PART NO 6838051
		CLASSIFICATION

D

IBM CORP

SF660

SF660

4963 DISK ATTACHMENT CARD

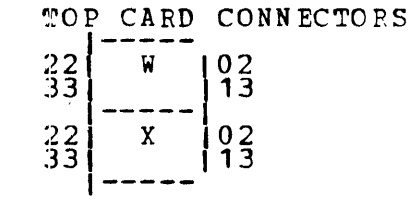
STANDARD CHANNEL

```
  ADDRESS BUS BIT--00------B02
  ADDRESS BUS BIT--01------B03
  ADDRESS BUS BIT--02------B04
  ADDRESS BUS BIT--03------B05
  ADDRESS BUS BIT--04------B07
  ADDRESS BUS BIT--05------B08
  ADDRESS BUS BIT--06------B09
  ADDRESS BUS BIT--07------B10
  ADDRESS BUS BIT--08------B12
  ADDRESS BUS BIT--09------D02
  ADDRESS BUS BIT--10------D04
  ADDRESS BUS BIT--11------D05
  ADDRESS BUS BIT--12------D06
  ADDRESS BUS BIT--13------D07
  ADDRESS BUS BIT--14------D09
  ADDRESS BUS BIT--15------D10
  ADDRESS BUS BIT--16------D11
  ADDRESS GATE-------------M08
  ADDRESS GATE RETURN------M09
# BURST RETURN------------(P04)
  CONDITION CODE IN BIT-00-D12
  CONDITION CODE IN BIT-01-D13
  CONDITION CODE IN BIT-02-B13
# CYCLE BYTE INDICATOR----(P10)
  CYCLE INPUT INDICATOR----P09
  CYCLE STEAL REQUEST IN---M02
  DATA BUS BIT------00-----G02
  DATA BUS BIT------01-----G03
  DATA BUS BIT------02-----G04
  DATA BUS BIT------03-----G05
  DATA BUS BIT------04-----G07
  DATA BUS BIT------05-----G08
  DATA BUS BIT------06-----G09
  DATA BUS BIT------07-----G10
  DATA BUS BIT------P0-----G12
  DATA BUS BIT------08-----J02
  DATA BUS BIT------09-----J04
  DATA BUS BIT------10-----J05
  DATA BUS BIT------11-----J06
  DATA BUS BIT------12-----J07
  DATA BUS BIT------13-----J09
  DATA BUS BIT------14-----J10
  DATA BUS BIT------15-----J11
  DATA BUS BIT------P1-----J12
  DATA STROBE-------------M10
  HALT OR MCK-------------M07
  INITIATE IPL------------P07
  IPL---------------------S04
  POLL--------------------M12
  POLL IDENTIFIER BIT--00--P11
  POLL IDENTIFIER BIT--01--S02
  POLL IDENTIFIER BIT--02--S03
  POLL IDENTIFIER BIT--03--P12
  POLL IDENTIFIER BIT--04--P13
  POLL PRIME--------------M13
  POLL PROPAGATE----------M11
  POLL RETURN-------------M04
  POWER ON RESET----------S05
  REQUEST IN BUS BIT--00---S07
  REQUEST IN BUS BIT--01---S08
  REQUEST IN BUS BIT--02---S09
  REQUEST IN BUS BIT--03---S10
  REQUEST IN BUS BIT--04---S12
  REQUEST IN BUS BIT--05---S13
  REQUEST IN BUS BIT--06---U02
  REQUEST IN BUS BIT--07---U04
  REQUEST IN BUS BIT--08---U05
  REQUEST IN BUS BIT--09---U06
  REQUEST IN BUS BIT--10---U07
  REQUEST IN BUS BIT--11---U09
  REQUEST IN BUS BIT--12---U10
  REQUEST IN BUS BIT--13---U11
  REQUEST IN BUS BIT--14---U12
  REQUEST IN BUS BIT--15---U13
  SERVICE GATE------------P05
  SERVICE GATE RETURN------P06
  STATUS BUS BIT------00---J13
  STATUS BUS BIT------01---G13
  STATUS BUS BIT------02---M03
  STATUS BUS BIT------03---P02
  SYSTEM RESET------------M05
```

4963 TOP CARD CONNECTORS

```
  W22-- -FILE DATA BUS BIT 00
  W23-- -FILE DATA BUS BIT 01
  W24-- -FILE DATA BUS BIT 02
  W25-- -FILE DATA BUS BIT 03
  W26-- -FILE DATA BUS BIT 04
  W28-- -FILE DATA BUS BIT 05
  W29-- -FILE DATA BUS BIT 06
  W30-- -FILE DATA BUS BIT 07
  W31-- -FILE DATA BUS BIT P0
  W03-- -FILE DATA BUS BIT 08
  W04-- -FILE DATA BUS BIT 09
  W05-- -FILE DATA BUS BIT 10
  W06-- -FILE DATA BUS BIT 11
  W07-- -FILE DATA BUS BIT 12
  W09-- -FILE DATA BUS BIT 13
  W10-- -FILE DATA BUS BIT 14
  W11-- -FILE DATA BUS BIT 15
  W12-- -FILE DATA BUS BIT P1
  X31-- -INTRFC PAR CHECK
  X03-- -FILE TAG 0
  X04-- -FILE TAG 1
  X05-- -FILE TAG 2
  X06-- -FILE TAG 3
  X12-- -FILE TAG P
  X25-- -AKN REQ OUT
  X28-- -STROBE IN
  X29-- -REQUEST IN
  X13-- -PARAKEET POR
  X23-- -SYSTEM RESET
  X24-- -REQUEST OUT
  X26-- -STROBE OUT
  X30-- -AKN REQ IN PWRD
  X32-- -SYSTEM PWR ON RST
  X07-- -FILE TAG 4
  X09-- -FILE TAG 5
  X10-- -FILE TAG 6
  X11-- -FILE TAG 7
  W02--  GND
  W08--  GND
  W27--  GND
  W33--  GND
  X02--  GND
  X08--  GND
  X27--  GND
  X33--  GND
  W32--  NOT USED
# W13-- -IPL
# X22-- -BURST MODE
```

TOP CARD CONNECTORS



CABLE LOCATIONS

VOLTAGE PIN ASSIGNMENTS
+5V---D03--J03--P03--U03
GND---D08--J08--P08--U08
-5V---G06
+8.5V---G11

LINES ARE NOT USED BY THIS ATTACHMENT.

SEE 4963 THEORY DIAGRAMS MANUAL FOR DATA FLOW

4963 ATTACHMENT CARD

E.C. HISTORY 08-17-78 374947

MACH. SERIES 1

IBM CORP. GSD

DATE 01-15-79 LAST E.C. 375147

P.N. 6837768

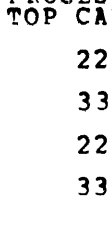
SF5000

0 0 0

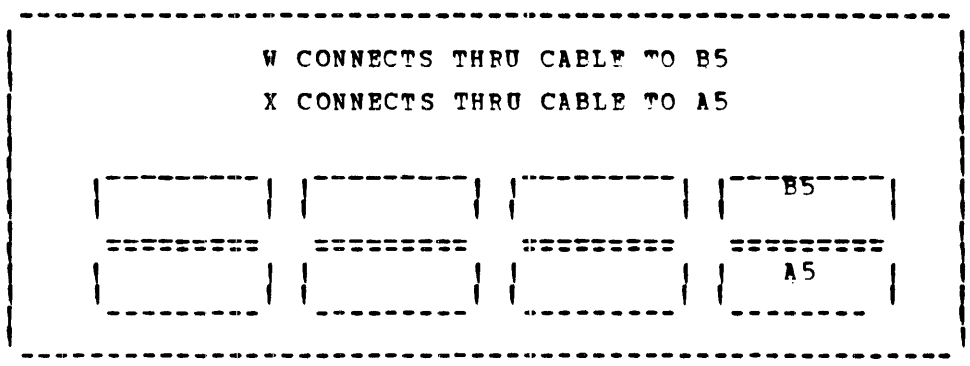
4963 DISK ATTACHMENT CABLE

ATTACHMENT CABLES PIN ASSIGNMENTS		DUC BOARD (A2) PIN ASSIGNMENTS
W22--	-FILE DATA BUS BIT 00	-- B5B02
W23--	-FILE DATA BUS BIT 01	-- B5B03
W24--	-FILE DATA BUS BIT 02	-- B5B04
W25--	-FILE DATA BUS BIT 03	-- B5B05
W26--	-FILE DATA BUS BIT 04	-- B5B06
W28--	-FILE DATA BUS BIT 05	-- B5B08
W29--	-FILE DATA BUS BIT 06	-- B5B09
W30--	-FILE DATA BUS BIT 07	-- B5B10
W31--	-FILE DATA BUS BIT P0	-- B5B11
W03--	-FILE DATA BUS BIT 08	-- B5D03
W04--	-FILE DATA BUS BIT 09	-- B5D04
W05--	-FILE DATA BUS BIT 10	-- B5D05
W06--	-FILE DATA BUS BIT 11	-- B5D06
W07--	-FILE DATA BUS BIT 12	-- B5D07
W09--	-FILE DATA BUS BIT 13	-- B5D09
W10--	-FILE DATA BUS BIT 14	-- B5D10
W11--	-FILE DATA BUS BIT 15	-- B5D11
W12--	-FILE DATA BUS BIT P1	-- B5D12
X31--	-INTRFC PARITY CHECK	-- A5B11
X03--	-FILE TAG 0	-- A5D03
X04--	-FILE TAG 1	-- A5D04
X05--	-FILE TAG 2	-- A5D05
X06--	-FILE TAG 3	-- A5D06
X12--	-FILE TAG P	-- A5D12
X25--	-AKN REQ OUT	-- A5B05
X28--	-STROBE IN	-- A5B08
X29--	-REQUEST IN	-- A5B09
X13--	-PARAKEET POR	-- A5D13
X23--	-SYSTEM RESET	-- A5B03
X24--	-REQUEST OUT	-- A5B04
X26--	-STROBE OUT	-- A5B06
X30--	-AKN REQ IN PWRD	-- A5B10
X32--	-SYSTEM PWR ON RST	-- A5B12
X07--	-FILE TAG 4	-- A5D07
X09--	-FILE TAG 5	-- A5D09
X10--	-FILE TAG 6	-- A5D10
X11--	-FILE TAG 7	-- A5D11
W02--	GND	-- B5D02
W08--	GND	-- B5D08
W27--	GND	-- B5B07
W33--	GND	-- B5B13
X02--	GND	-- A5D02
X08--	GND	-- A5D08
X27--	GND	-- A5B07
X33--	GND	-- A5B13
W32--	NOT USED	-- B5B12
# W13--	-IPL	-- B5D13
# X22--	-BURST MODE	-- A5B02

PROCESSOR ATTACHMENT
TOP CARD CONNECTORS



CABLE LOCATIONS



DUC BOARD (A2) (CARD SIDE VIEW)

LINES ARE NOT USED

SEE 4963 THEORY DIAGRAMS MANUAL FOR DATA FLOW

4963 ATTACHMENT CABLE

E.C. HISTORY 08-17-78 374947

MACH. 4963

SF5001

IBM COPP. GSD

DATE 02-01-79 LAST E.C. 375351

P.N. 6837769

0 0 0

TIMER FEATURE ATTACHMENT CARD

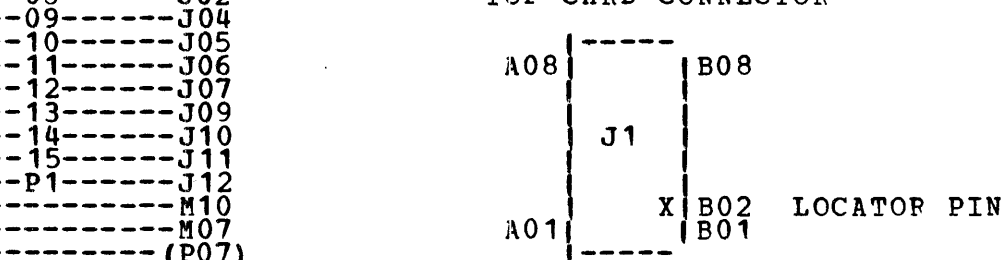
STANDARD CHANNEL

```
  ADDRESS BUS BIT--00------B02
  ADDRESS BUS BIT--01------B03
  ADDRESS BUS BIT--02------B04
  ADDRESS BUS BIT--03------B05
  ADDRESS BUS BIT--04------B07
  ADDRESS BUS BIT--05------B08
  ADDRESS BUS BIT--06------B09
  ADDRESS BUS BIT--07------B10
  ADDRESS BUS BIT--08------B12
  ADDRESS BUS BIT--09------D02
  ADDRESS BUS BIT--10------D04
  ADDRESS BUS BIT--11------D05
  ADDRESS BUS BIT--12------D06
  ADDRESS BUS BIT--13------D07
  ADDRESS BUS BIT--14------D09
  ADDRESS BUS BIT--15------D10
  ADDRESS BUS BIT--16------D11
  ADDRESS GATE------------M08
  ADDRESS GATE RETURN-----M09
# BURST RETURN-----------(P04)
  CONDITION CODE IN BIT-00-D12
  CONDITION CODE IN BIT-01-D13
  CONDITION CODE IN BIT-02-B13
# CYCLE BYTE INDICATOR----(P10)
# CYCLE INPUT INDICATOR---(P09)
# CYCLE STEAL REQUEST IN--(M02)
  DATA BUS BIT-----00------G02
  DATA BUS BIT-----01------G03
  DATA BUS BIT-----02------G04
  DATA BUS BIT-----03------G05
  DATA BUS BIT-----04------G07
  DATA BUS BIT-----05------G08
  DATA BUS BIT-----06------G09
  DATA BUS BIT-----07------G10
  DATA BUS BIT-----P0------G12
  DATA BUS BIT-----08------J02
  DATA BUS BIT-----09------J04
  DATA BUS BIT-----10------J05
  DATA BUS BIT-----11------J06
  DATA BUS BIT-----12------J07
  DATA BUS BIT-----13------J09
  DATA BUS BIT-----14------J10
  DATA BUS BIT-----15------J11
  DATA BUS BIT-----P1------J12
  DATA STROBE-------------M10
  HALT OR MCHK------------M07
# INITIATE IPL-----------(P07)
# IPL--------------------(S04)
  POLL---------------------M12
  POLL IDENTIFIER BIT--00--P11
  POLL IDENTIFIER BIT--01--S02
  POLL IDENTIFIER BIT--02--S03
  POLL IDENTIFIER BIT--03--P12
  POLL IDENTIFIER BIT--04--P13
  POLL PRIME---------------M13
  POLL PROPAGATE-----------M11
  POLL RETURN--------------M04
  POWER ON RESET-----------S05
  REQUEST IN BUS BIT--00---S07
  REQUEST IN BUS BIT--01---S08
  REQUEST IN BUS BIT--02---S09
  REQUEST IN BUS BIT--03---S10
  REQUEST IN BUS BIT--04---S12
  REQUEST IN BUS BIT--05---S13
  REQUEST IN BUS BIT--06---U02
  REQUEST IN BUS BIT--07---U04
  REQUEST IN BUS BIT--08---U05
  REQUEST IN BUS BIT--09---U06
  REQUEST IN BUS BIT--10---U07
  REQUEST IN BUS BIT--11---U09
  REQUEST IN BUS BIT--12---U10
  REQUEST IN BUS BIT--13---U11
  REQUEST IN BUS BIT--14---U12
  REQUEST IN BUS BIT--15---U13
  SERVICE GATE-------------P05
  SERVICE GATE RETURN------P06
  STATUS BUS BIT-------00---J13
  STATUS BUS BIT-------01---G13
  STATUS BUS BIT-------02---M03
  STATUS BUS BIT-------03---P02
  SYSTEM RESET-------------M05
```

TIMER TOP CARD CONNECTOR(S)

```
J1A08-- FRAME GROUND STRAP
J1A06-- NOT USED
J1A07-- NOT USED
J1B01-- NOT USED
J1B02-- NOT USED
J1B03-- NOT USED
J1A01-- TIMER 00 CUSTOMER CLK
J1A05-- TIMER 00 CUSTOMER SIGNAL GND
J1A02-- TIMER 00 EXT GATE
J1A04-- TIMER 00 EXT GATE ENB
J1A03-- TIMER 00 RUN STATE
J1B08-- TIMER 01 CUSTOMER CLK
J1B04-- TIMER 01 CUSTOMER SIGNAL GND
J1B07-- TIMER 01 EXT GATE
J1B05-- TIMER 01 EXT GATE ENB
J1B06-- TIMER 01 RUN STATE
```

TOP CARD CONNECTOR



CABLE LOCATION

CUSTOMER ACCESS PANEL (C.A.P.)
PIN ASSIGNMENTS

CARD END	PANEL END
J1A01	A
J1A02	C
J1A03	B
J1A04	D
J1A05	*
J1B04	*
J1B05	T
J1B06	V
J1B07	S
J1B08	U

* TWISTED PAIR GROUND SHIELDS
TO FRAME GROUND ON C.A.P.

TIMER 00 GROUND -- A05
TIMER 01 GROUND -- B04

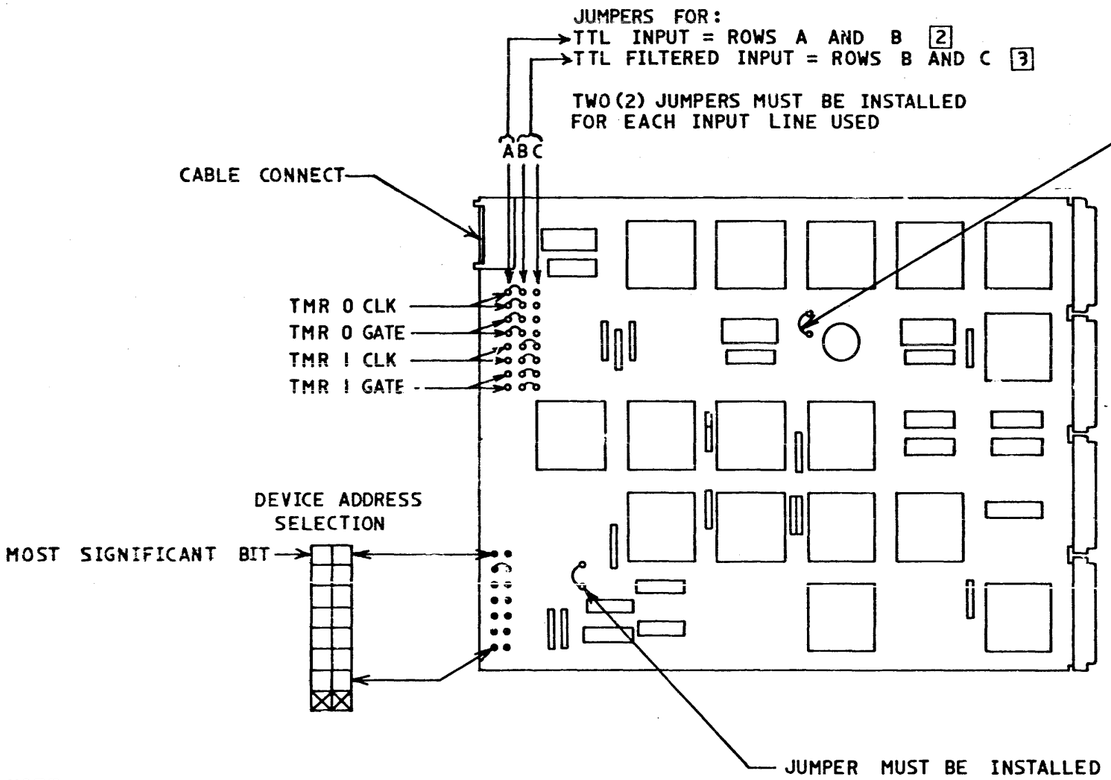
VOLTAGE PIN ASSIGNMENTS
+5V---D03--J03--P03--U03
GND---D08--J08--P08--U08

\# LINES ARE NOT USED BY THIS ATTACHMENT.

SEE PROC THEORY DIAGRAMS
MANUAL FOR DATA FLOW

TIMER ATTACHMENT CARD

E.C.	HISTORY	MACH.	ST100
06-21-76	578446		
10-01-76	578468	TIMER	
12-02-76	578469		
		IBM CORP. GSD	
DATE	LAST E.C.		000
06-10-77	578625	P.N. 1635187	



NOTES:

[2] 0 TO +5.5 VOLTS MAX @ ≤ MHZ RATE

[3] ±24 VOLTS MAX @ ≤ 50 KHZ RATE (WORSE CASE)

NOTE:

[1] JUMPER INSTALLED = LOGICAL 1
NO JUMPER = LOGICAL 0

STANDARD CARD JUMPERING (AS SHOWN)
ADDRESS = 40 HEX = 01000000
INPUT = TTL(TIMER 0) TTL FILTERED(TIMER 1)

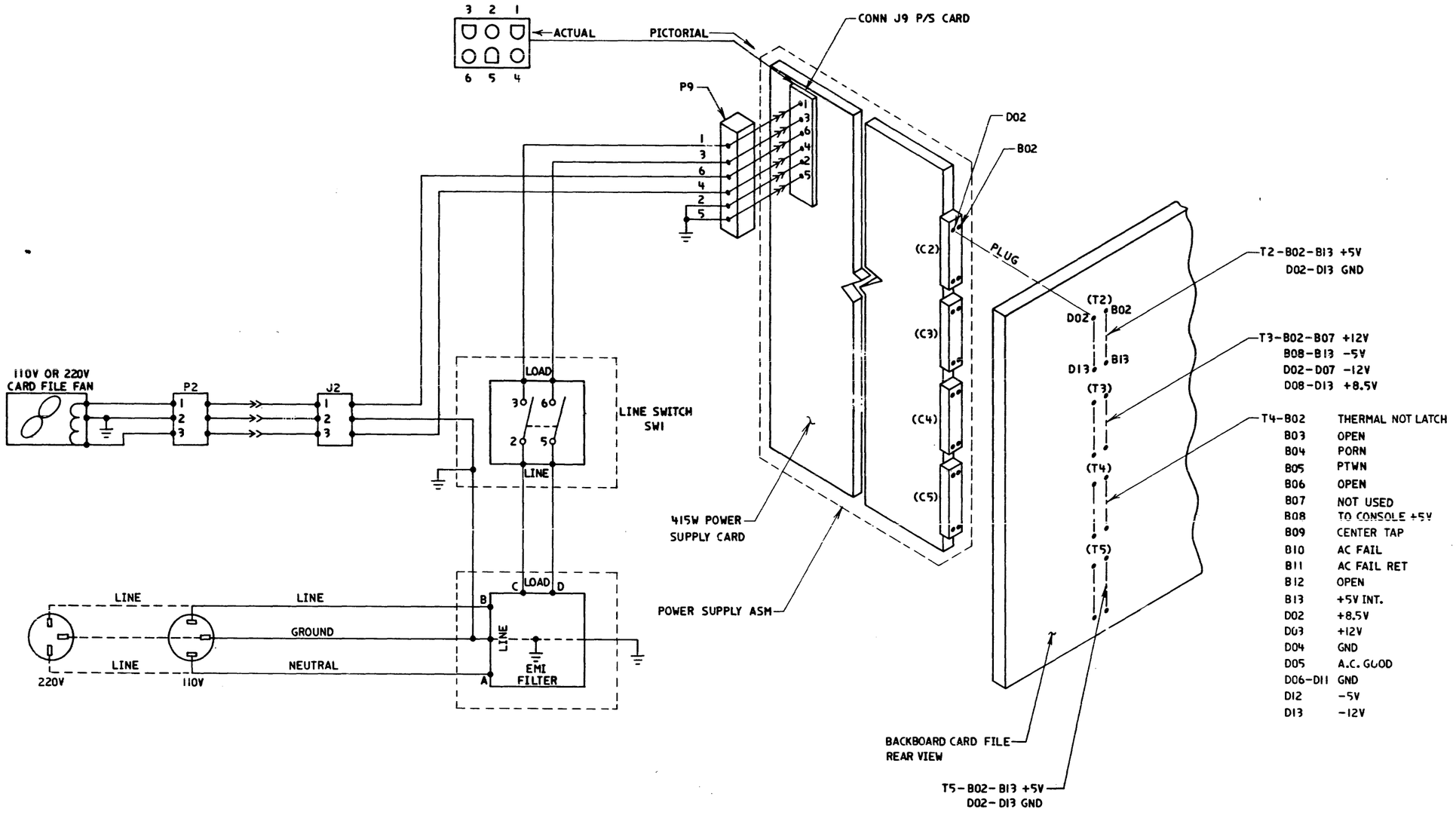
DIAGNOSTIC CONFIGURATION ENTRY FOR CARD AS SHOWN
TMR0 = 4050, 4000,0000,0000,0000,0000,0000,0028
TMR1 = 4150, 0000,0000,0000,0000,0000,0000,0028

WRAP CONNECTOR P/N 1633835

EC HISTORY		DRAWING TITLE
31 MAR 77	578714	TIMER
16 AUG 78	755404	MACH SERIES/1
14 SEP 79	375743	PART NO 1635151
C		CLASSIFICATION

IBM CORP

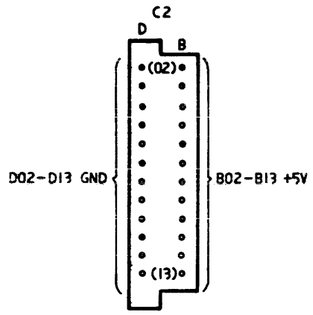
YA450

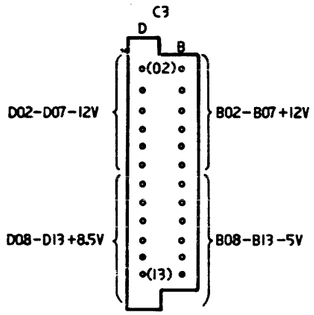


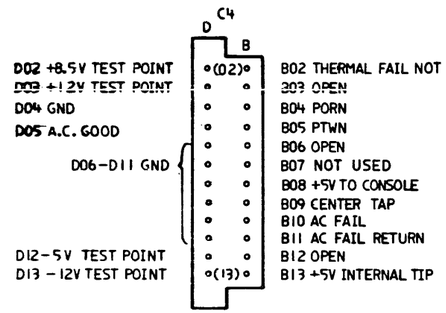
EC HISTORY		DRAWING TITLE
13AUG80	869341C	FULL FILE AC/DC DISTRIBUTION
28JUL81	994400	MACH
		PART NO 6844420
D		CLASSIFICATION

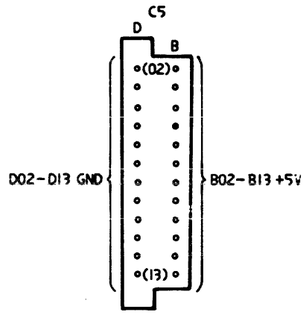
IBM CORP

YA450

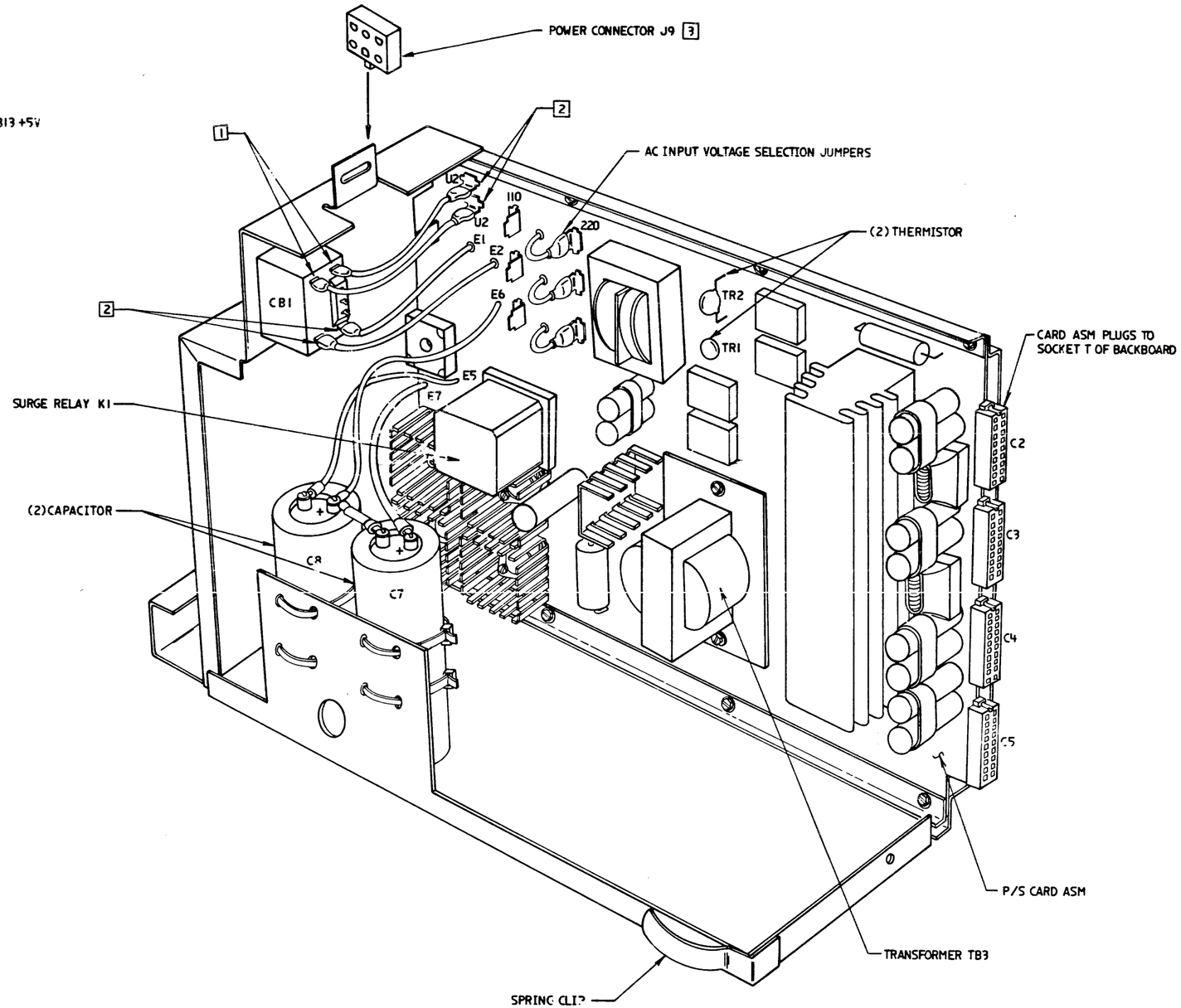








YA455



NOTES:

1. THESE LEADS ARE SOLDERED ONTO THE CIRCUIT BREAKER
2. SLIP-ON TERMINALS
3. POWER CONNECTOR J9 IS ON THE FRONT OF THE POWER SUPPLY CHASSIS

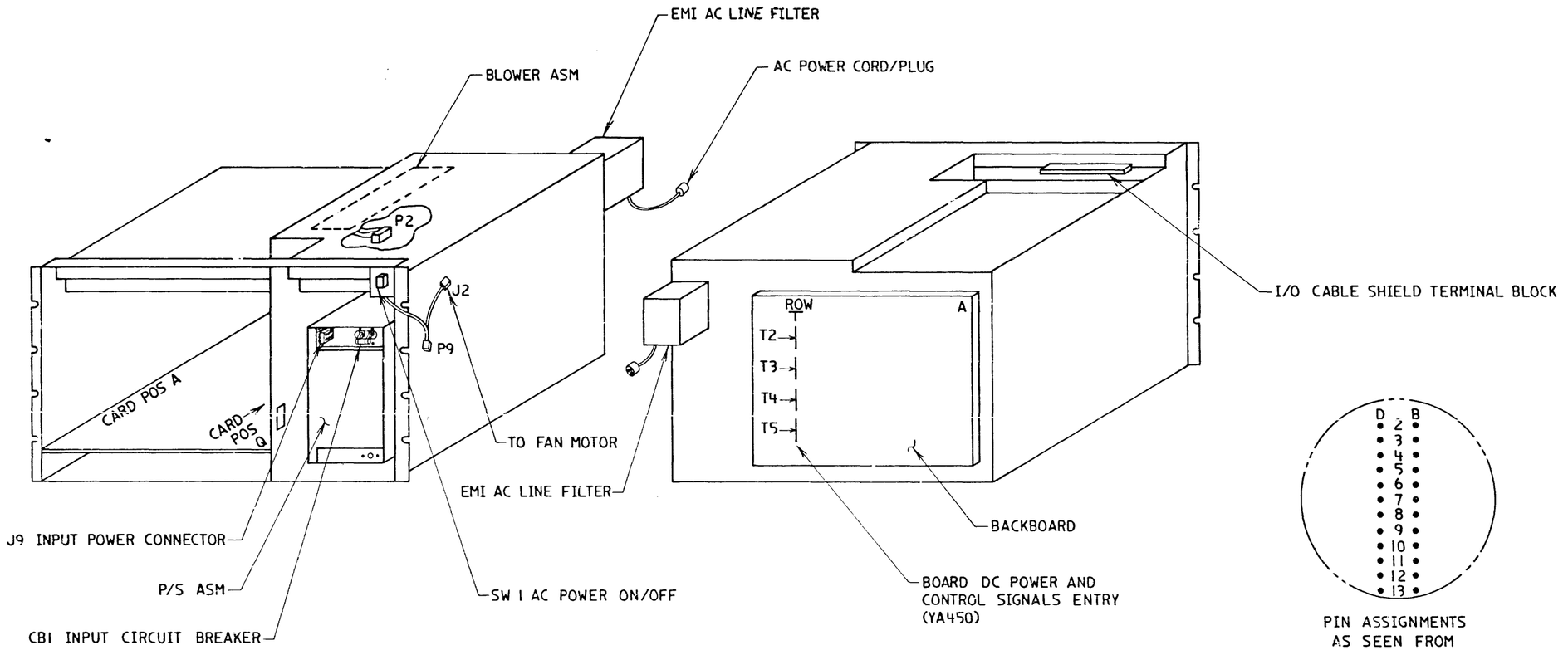
EC HISTORY		DRAWING TITLE
13 AUG 80	869341C	POWER SUPPLY 415 WATT-PLUGGABLE
21 JAN 81	987893	MACH
28 JUL 81	994400	PART NO 6844421
		CLASSIFICATION

D

IBM CORP

YA455

YA460



PIN ASSIGNMENTS
AS SEEN FROM
BACKBOARD SIDE

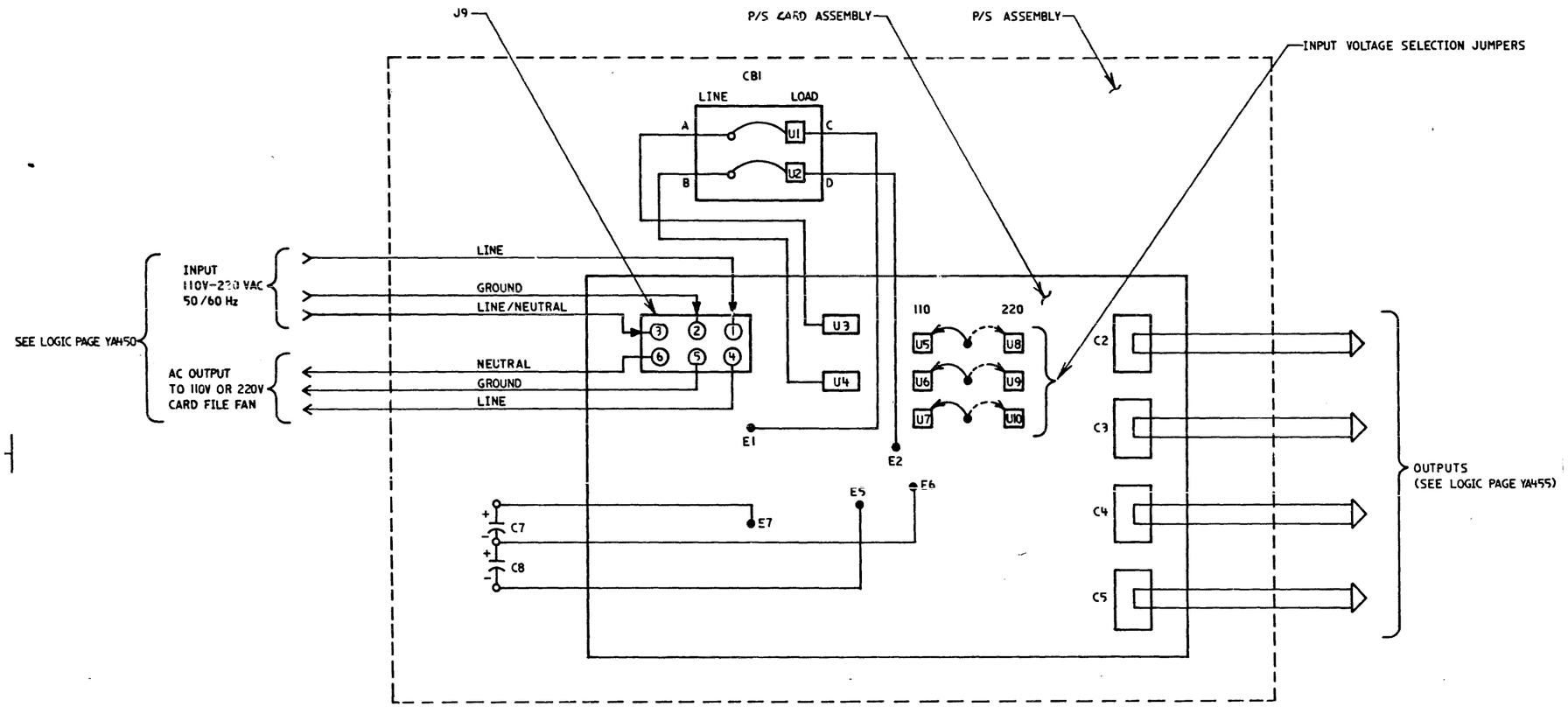
EC HISTORY		DRAWING TITLE
13 AUG 80	869341C	CARD FILE COMPONENT LOC
		MACH 415 W
		PART NO 6844422
		CLASSIFICATION

D

IBM CORP

YA460

YA465



NOTE: U2 CONNECTIONS ARE FOR SLIP-ON TERMINALS

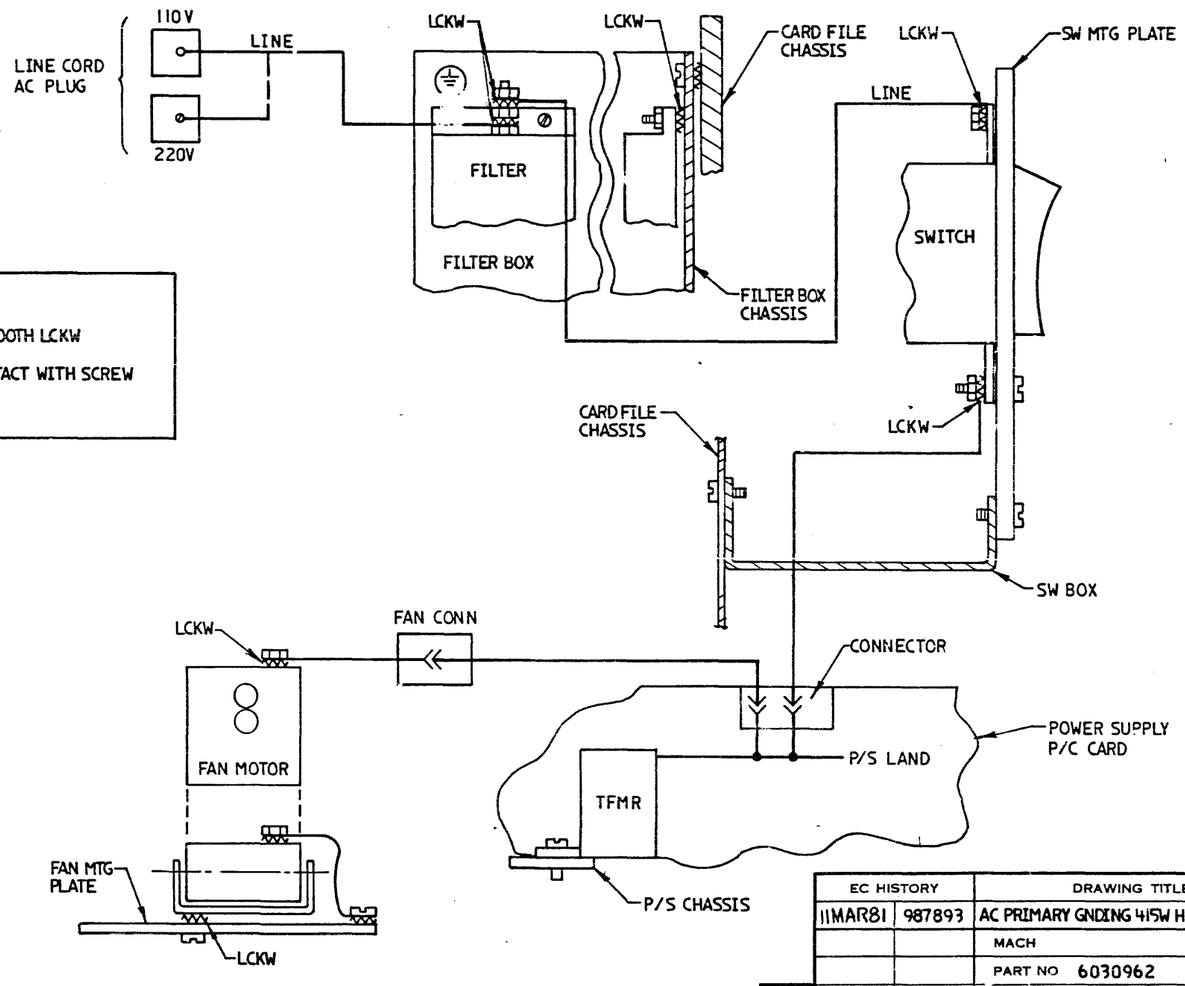
COMPONENTS	
SYM	DESCRIPTION
C7,C8	CAPACITOR, 2900 μF 200VDC
CB1	CIRCUIT BREAKER, 10A, 240VAC

EC HISTORY		DRAWING TITLE
	869741C	POWER SUPPLY SCHEMATIC
		MACH 415 W
		PART NO 6844423
C		CLASSIFICATION

IBM CORP

YA465

YA465



YA470

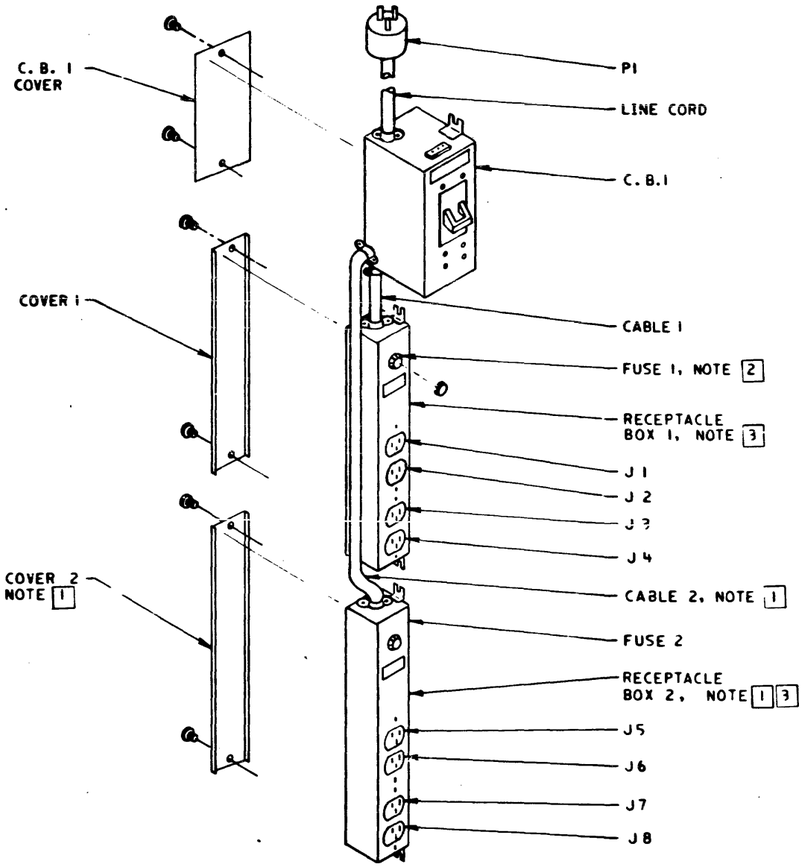
EC HISTORY		DRAWING TITLE
11MAR81	987893	AC PRIMARY GNDING 415W HI FREQ. P/S
		MACH
		PART NO 6030962
		CLASSIFICATION

C

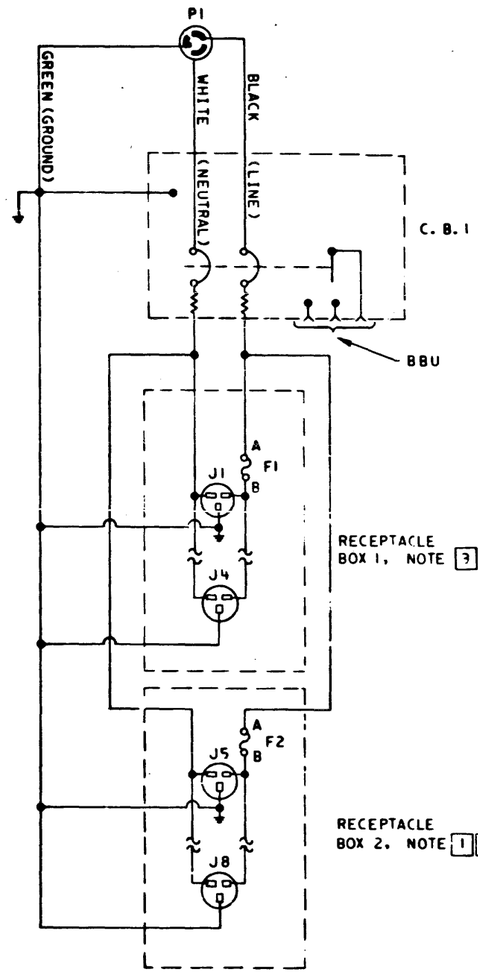
IBM CORP

YA470

YA470



1.8 METER ENCLOSURE



NOTES:

1. NOT INCLUDED IN THE 1.0 METER ENCLOSURE
2. FOR CANADA ONLY
3. MAY BE EITHER 110 OR 220 VOLT RECEPTACLES
4. JAPAN INSTALLATIONS ONLY; A COMPENSATION NETWORK ASSEMBLY IS USED. REFER TO INSTALLATION INSTRUCTIONS, PART NUMBER 1633743, PARAGRAPH 4.1

YD100

EC HISTORY		DRAWING TITLE
	578625	AC PWR DIST LOCATION & WD
28 JUN 79	375342A	MACH
		PART NO 4412901
		CLASSIFICATION

D

IBM CORP

YD100