IBM

Series/1

SY34-0092-0

# IBM Series/1
# 4969 Magnetic Tape Subsystem
# Theory Diagrams

**First Edition (December 1979)**

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# Preface

This book describes how the 4969 Magnetic Tape Subsystem works. The information is designed to be used in the classroom as a teaching aid, and in the field as a recall document. It is intended for 4969 maintenance personnel who have received Series/1 CE training and are familiar with the Series/1 diagnostic programs. The sequence charts and diagrams in this book are intended for instructional purposes only and are not to be used in place of the machine logic diagrams (MLDs) when diagnosing problems.

## How This Book is Organized

The material is presented in four chapters.

Chapter 1 introduces the reader to the general characteristics and features of the various 4969 subsystems available. It also describes the magnetic recording modes, basic data flow, and required maintenance.

Chapter 2 describes the functional units of the 4969.

Chapter 3 explains the circuit functions of the attachment feature, controller feature, and the tape unit.

Chapter 4 describes how the processor transfers data to and from the tape units.

## Related Publications

Series/1 processor information can be found in the following publications:

*IBM Series/1 4952 Processor and Processor Features Description*, GA34-0084

*IBM Series/1 4952 Processor and Processor Features Theory Diagrams*, SY34-0089

*IBM Series/1 4953 Processor and Processor Features Description*, GA34-0022

*IBM Series/1 4953 Processor and Processor Features Theory Diagrams*, SY34-0042

*IBM Series/1 4955 Processor and Processor Features Description*, GA34-0021

*IBM Series/1 4955 Processor and Processor Features Theory Diagrams*, SY34-0041

Additional 4969 information can be found in the following publications:

*IBM Series/1 4969 Magnetic Tape Subsystem Description*, GA34-0087

*IBM Series/1 4969 Magnetic Tape Subsystem Model 4 Maintenance Information*, SY34-0093

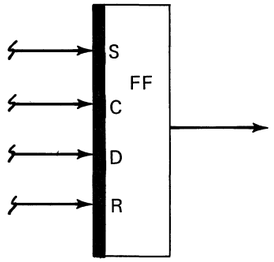
*IBM Series/1 4969 Magnetic Tape Subsystem Model 4 Parts Catalog*, S134-0037

*IBM Series/1 4969 Magnetic Tape Subsystem Model 7 Maintenance Information*, SY34-0097

*IBM Series/1 4969 Magnetic Tape Subsystem Model 7 Parts Catalog*, S134-0038

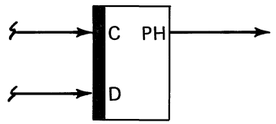
Other Series/1 information can be found in publications listed in *IBM Series/1 Graphic Bibliography*, GA34-0055.

# Legend



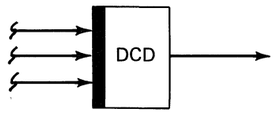

Flip Flop

The flip flop (FF) is a storage element that may have set (S), reset (R), control (C), or controlled data (D) inputs.



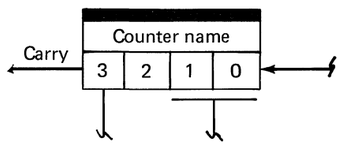

Polarity Hold

The polarity hold (PH) is a storage element that may have control (C), controlled data (D), or reset (R) inputs.




Decode

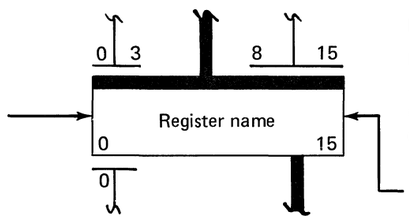
The decode (DCD) block may have multiple inputs of individual lines, a bus input, or a combination of both.




Counter

+1 for up

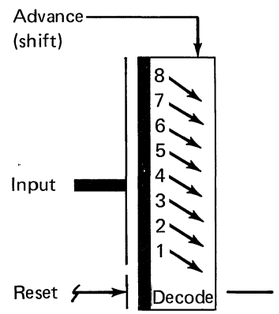
−1 for down




Register

Input side is denoted by a heavy border. A partial transfer of contents is shown by numbered input and/or output lines.

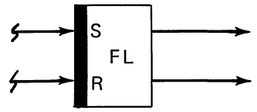
Carry or increment




Shift registers

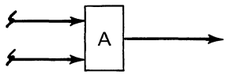
The shift registers are commonly used to serialize and deserialize data. Input side is denoted by the heavy border. A partial transfer of contents is shown by numbered input/output lines.

Output

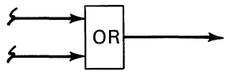



Flip latch

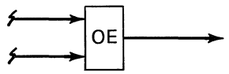
Input side is denoted by the heavy border. Circuit multiples shown by numeral in lower right corner.



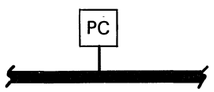

AND




OR

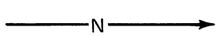



Exclusive OR

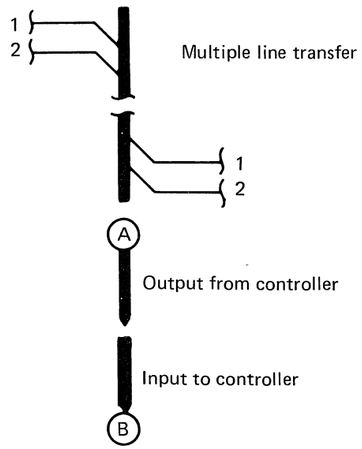


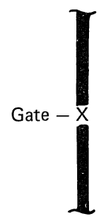

Bus on which parity is checked


Bus on which parity is generated




Negator (invertor)




Gated bus

Gate must be active for data to flow on bus.

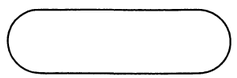


On-page connector

Indicates connection between two parts of the same page. Arrow leaving symbol points to correspondingly numbered symbol.

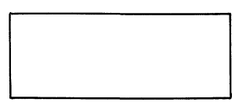

Off-page connector

Indicates connection between diagrams located on separate pages. Location of correspondingly lettered symbol shown adjacent to the connector.



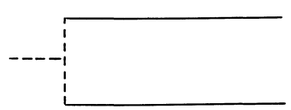
Terminal block

Indicates beginning or end of event within a flowchart



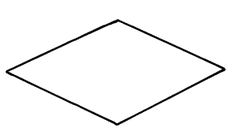
Process block

Indicates a major function or event within a flowchart.



Annotation

Gives descriptive comment or explanatory note.



Decision block

Indicates a point in a flowchart where a branch to alternate paths is possible.

# Contents

# Chapter 1. Introduction

## Tape Subsystem Description

The IBM 4969 Magnetic Tape Subsystem enables the IBM Series/1 to handle applications that require magnetic tape processing and additional offline storage. The tape subsystem consists of one to four 4969 Magnetic Tape Units, a 4969 Tape Subsystem Attachment Feature, and a controller feature. The tape units function in the system as both input and output devices. They transport the magnetic tape and read and write the information, as directed by the processor. The different tape units are similar in general appearance and operational use; the principal differences are the speed at which the units transport tape, and the rate and mode of recording information on tape. The tape unit is available in six models, providing a selection of recording modes—NRZI*, PE**, or a combination of both called dual density. The six tape unit models are:

| 4969 Model | Recording mode | Tape Speed | |
|---|---|---|---|
| | | meters/sec | inches/sec |
| 4N | NRZI | 1.1 | 45 |
| 4P | PE | | |
| 4D | Dual density | | |
| 7N | NRZI | 1.9 | 75 |
| 7P | PE | | |
| 7D | Dual density | | |

The Model 4 tape units use tension arms for mechanical tape buffering; the Model 7 units use vacuum columns.

* Non-return-to-zero change-on-ones recording. (Recording in which the ones are represented by a change in the state of magnetization and the zeros are represented by the absence of a change.)

** Phase encoding. (Recording in which ones are represented by a change in polarity from negative to positive and the zeros are represented by a change in polarity from positive to negative.)

## Configurations

The first tape unit attached to the Series/1 processor contains a controller feature and acts as an interface between the other tape units and the attachment feature card, which occupies an I/O slot in the processor or I/O expansion unit. The controller feature and attachment feature allow the maximum configuration of four tape units to be connected in serial fashion to the processor. Multiple attachments can be installed in one Series/1 where there is a requirement for more than four tape units. The controller can operate in NRZI, PE, or dual-density recording mode. All tape units connected to the controller must operate at the same speed. If the controller has the dual-density feature, connected tape units may be NRZI, PE, or dual-density.

### Attachment Feature

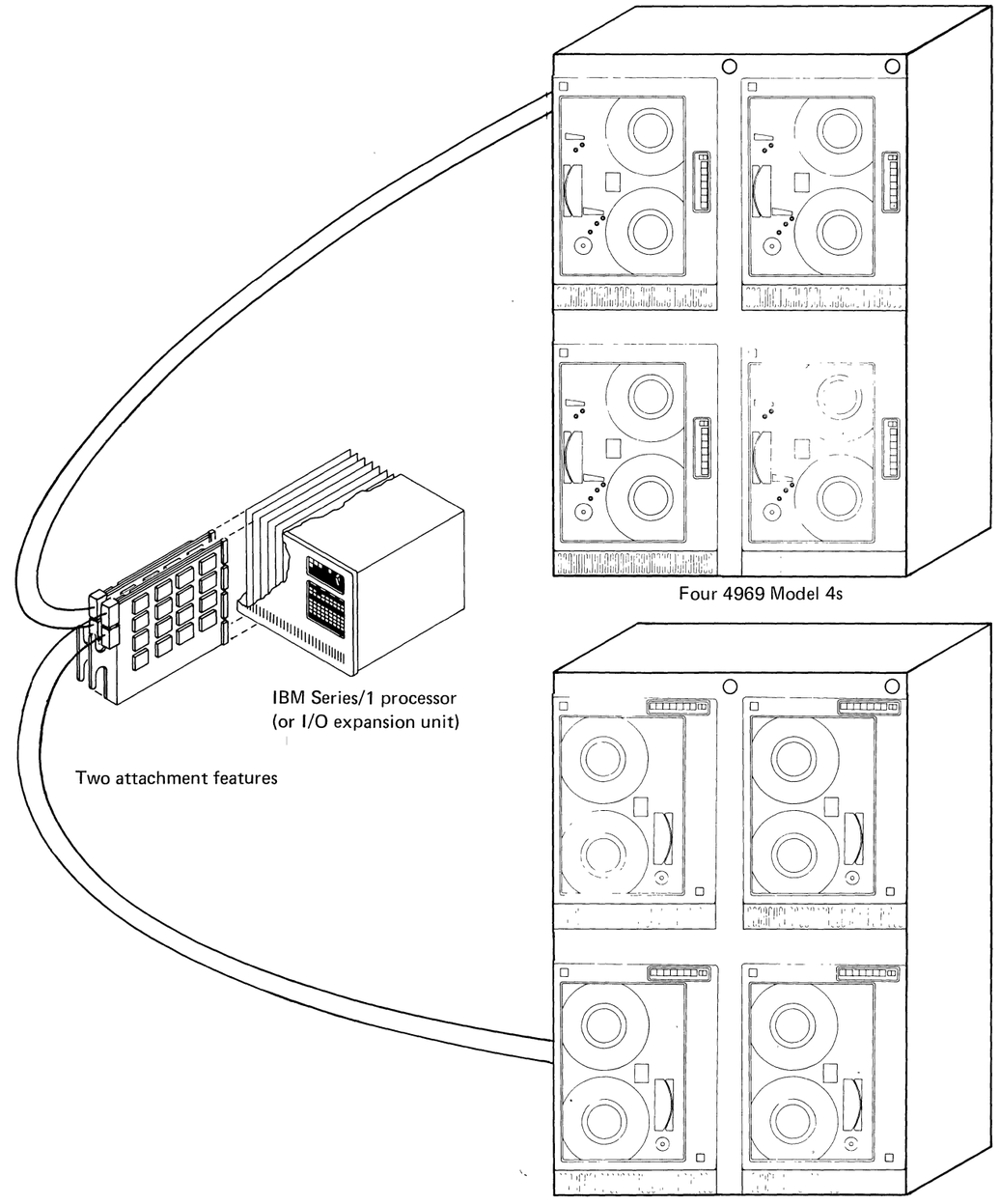
The attachment feature:

- Physically connects and logically adapts the tape unit to the processor
- Interrupts and controls execution of tape unit operations
- Transfers data from the processor to the tape unit in cycle-steal mode
- Furnishes status information and reports condition codes to the processor after executing Operate I/O instructions
- Supports the connection of NRZI/PE modes of nine-track tapes at data densities to 1600 characters per inch and speeds to 1.9 meters (75 inches) per second
- Retries failing read operations
- Permits overlapping other operations with a rewind operation

### Controller Feature

The controller feature:

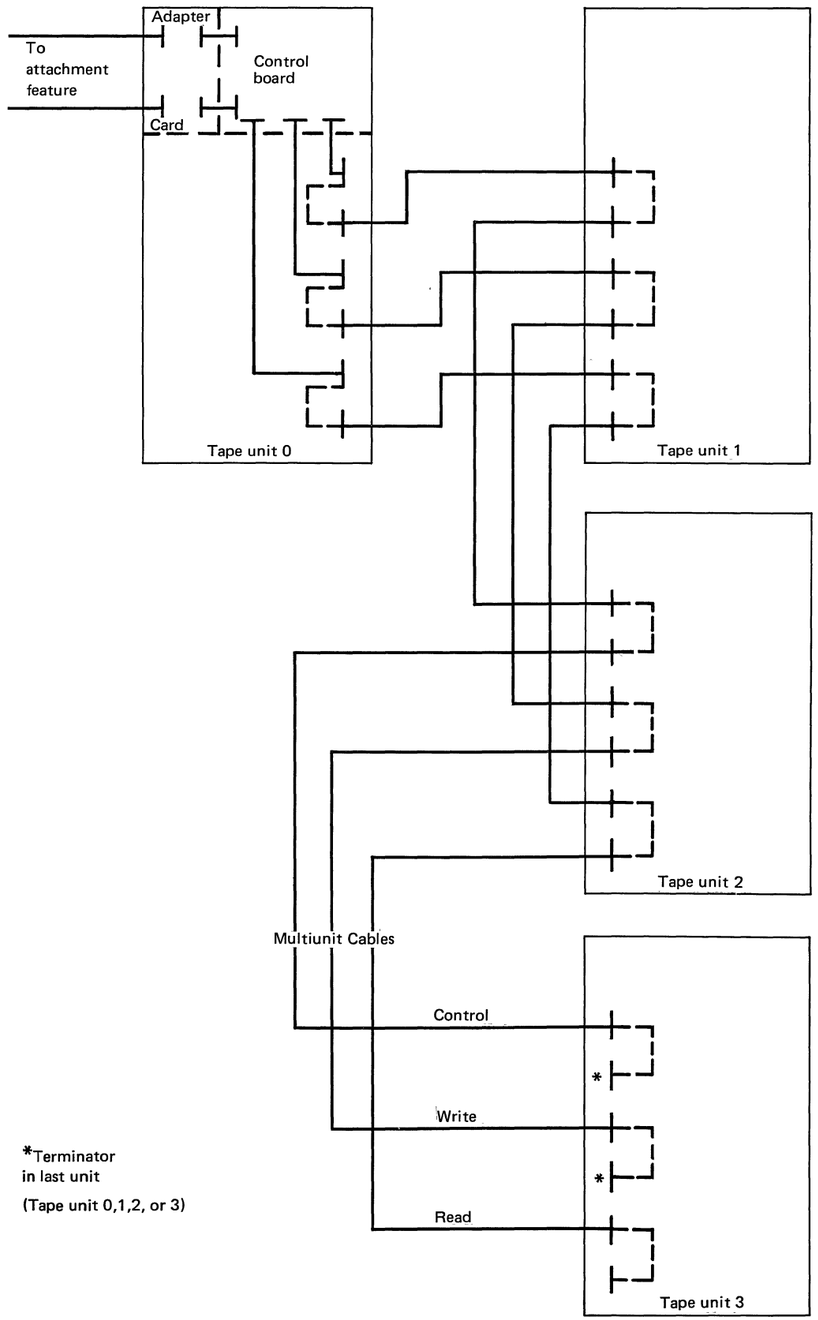
- Physically connects and logically adapts a maximum of four tape units to the attachment feature
- Supports the connection of tape units that use NRZI/PE modes
- Operates at either 1.1 meters (45 inches) per second or 1.9 meters (75 inches) per second tape unit speed




Two IBM Series/1 4969 Magnetic Tape Subsystems

**Cabling**

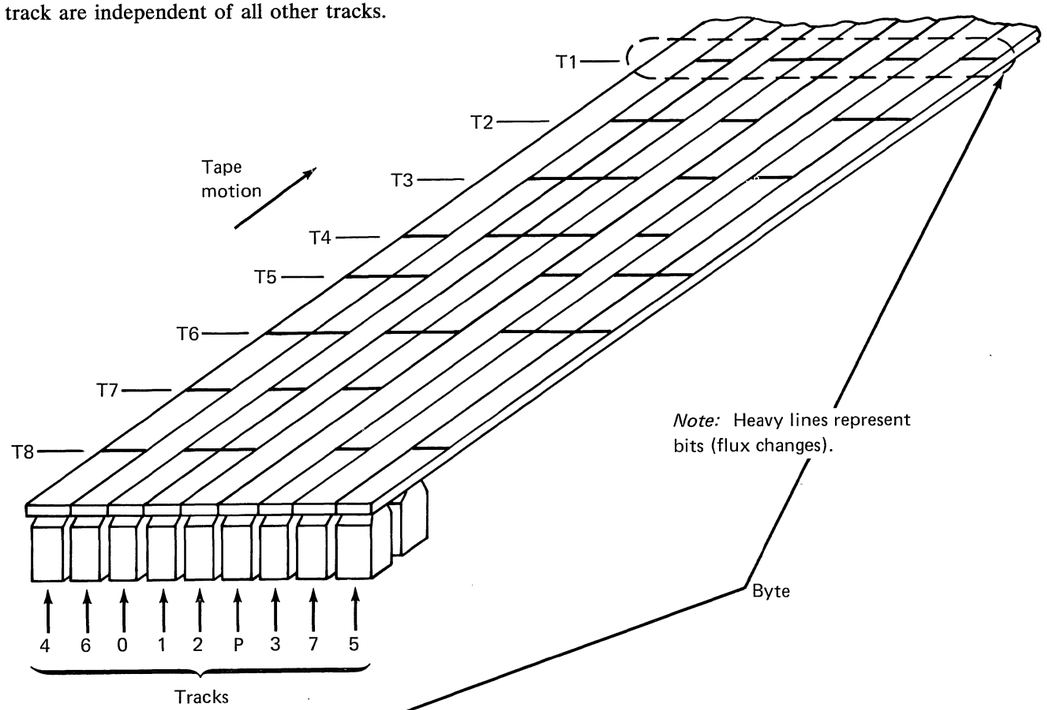
The primary tape unit (unit 0) is connected to the attachment feature by two cables. Each expansion unit (units 1–3) is connected into the subsystem by three multiunit cables that contain control, read data, and write data lines. The last unit in the subsystem contains terminator cards. If the subsystem does not include expansion units, the terminator cards must be installed in the primary unit. The top pin of select lines in control cable is used to select the tape unit (as shown in the following diagram).



## Magnetic Tape

### Tracks

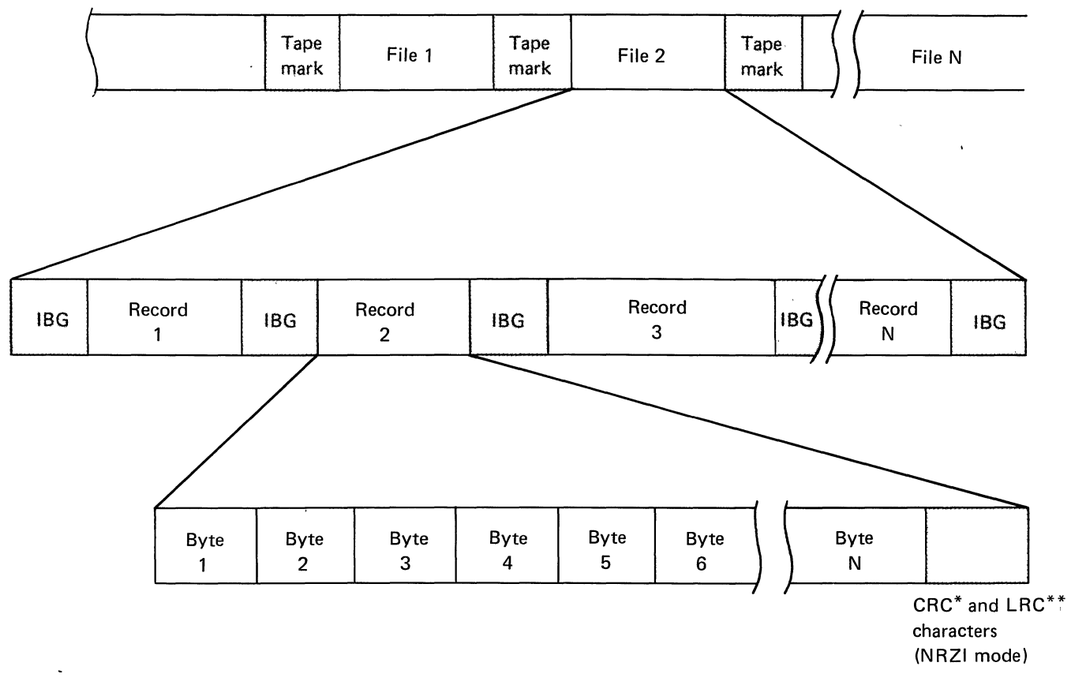
Bits of information are written on magnetic tape in parallel rows called tracks. One read coil and one write coil are provided for each track. Although the coils for all tracks are located in the same physical unit (the read/write head, which also contains an erase coil common to all tracks), the coils for each track are independent of all other tracks.




**Magnetic tape tracks**

### Format

Data is written on magnetic tape in groups of bytes called tape records. The number of bytes in each tape record depends on the number of bytes to be written. Tape records are separated by an area of erased tape called interblock gaps (IBG) which are created between two write type operations because tape cannot start or stop instantaneously. A period of time (in milliseconds) is required to accelerate tape to full speed and to stop tape after the record is written. Start-stop times, which are adjustable in the tape unit, have a direct bearing on the length of the gap. The nominal gap between records is 0.6 inch. Related tape records can be assembled on tape as a data file. Because one tape may contain several data files, tape marks are written between files to identify the boundaries.

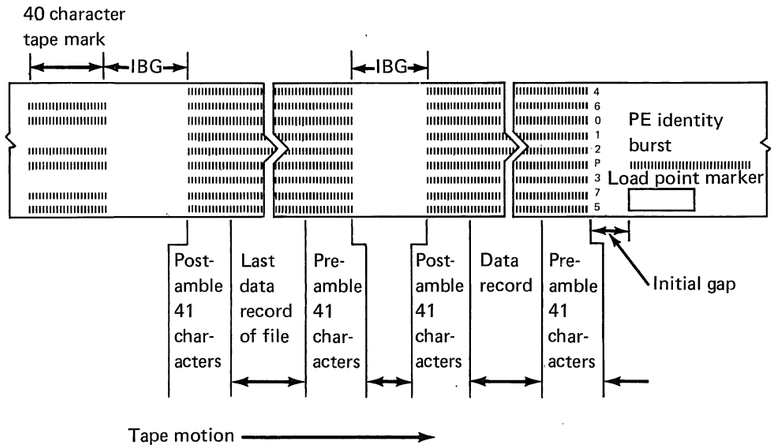



*Cyclic redundancy check character
**Longitudinal redundancy check character

**PE Recording**

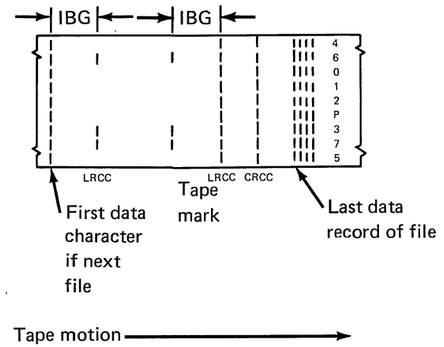
In the PE mode of recording, both 1's and 0's are represented by a change of direction of magnetization. A "1" is represented by a change in polarity from negative to positive; a "0" is represented by a change in polarity from positive to negative. In the PE mode, a special burst of syncronization bytes is written on each end of all data records. These bytes are generated by the controller and enable the controller to synchronize its read detection circuits when reading the data record.

Preceding the data record a preamble is written consisting of 41 characters, of which the first 40 characters contain 0-bits in all tracks, followed by a single character containing 1-bits in all tracks. Following each data record a postamble is written consisting of which the first character shall contain 1-bits in all tracks, followed by 40 characters containing 0-bits in all tracks. The tape mark in PE mode consists of 40 0-bits in tracks P, 0, 2, 5, 6, and 7. Tracks 1, 3, and 4 are erased.




**NRZI**

In the NRZI mode of recording, a 1 is represented by a change of magnetization, and a 0 is represented by no change of magnetization. At the end of each data record, the controller inserts a cyclic redundancy check (CRC) character, a longitudinal redundancy check (LRC) character, and an interblock gap (IBG). The tape mark in NRZI mode consists of 1-bits in tracks 3, 6, and 7 and is followed by its own LRC character.




**Erasing**

Tape is erased by magnetizing it continuously in one direction. When the polarity of the tape does not change for a period of time, no bits are recorded on the tape; it is erased. When bits are recorded on tape, the old bits are erased immediately prior to recording the new bits.

## Basic Subsystem Data Flow

During a write operation, data is transferred from the processor I/O channel to the tape unit; during a read operation, data is transferred from the tape unit to the channel. Data transfer is a parallel operation that sends one full word (16 bits plus two parity bits) at a time. During a write operation:

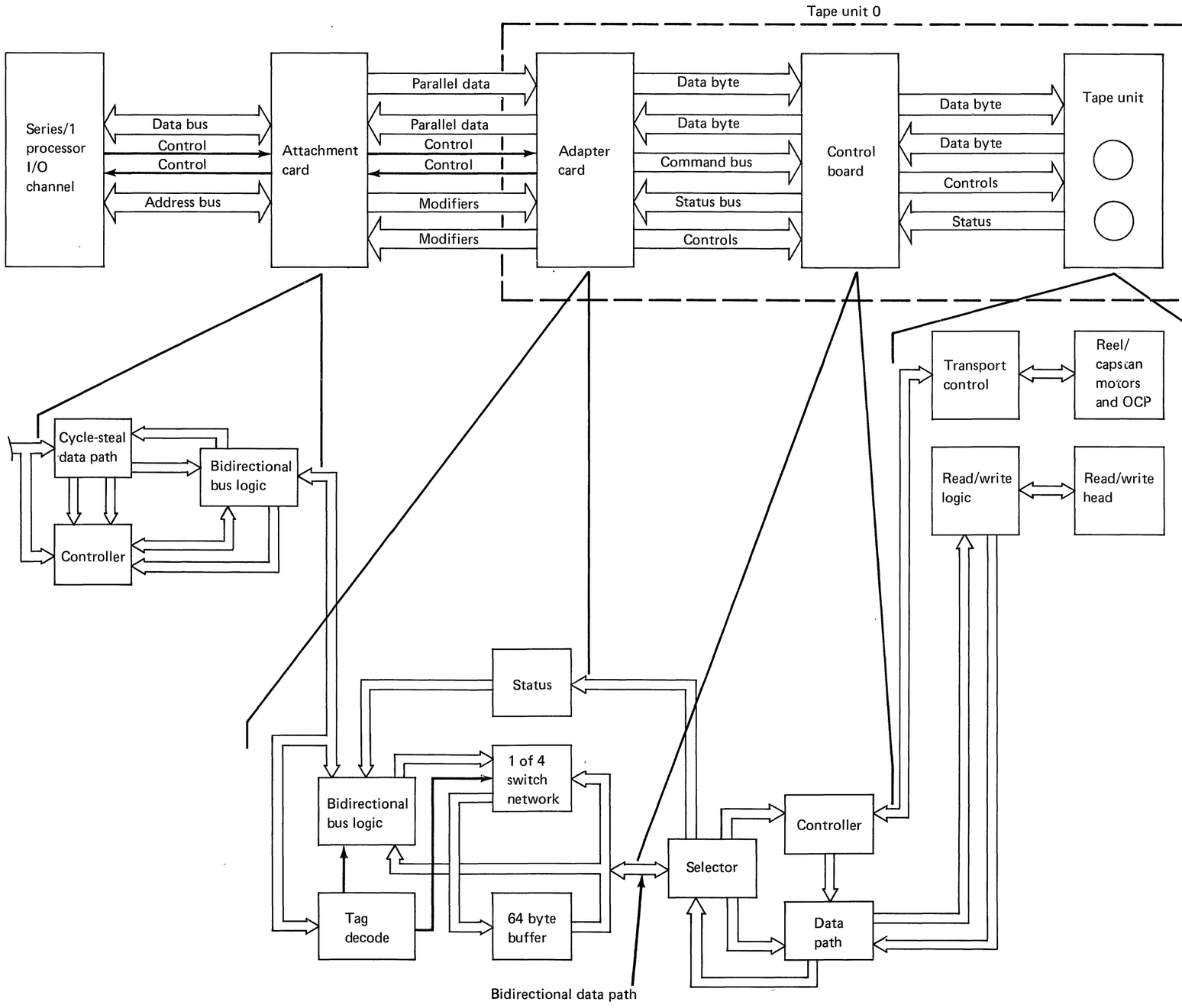
1. The attachment transfers a full word to the adapter card.
2. The adapter card divides the word into two bytes and transfers the data a byte at a time to the control board.
3. The control board formats the data for transfer to the tape unit and provides tape motion control.
4. The selected tape unit accelerates the tape up to speed and writes each byte of data including parity on the tape.

During a read operation:

1. The selected tape unit accelerates the tape up to speed.
2. The control board checks the parity of each byte of data as it is read from tape.
3. The control board transfers each byte of data to the adapter card.
4. The adapter card assembles the bytes of data into 16-bit words to transfer to the attachment card
5. The attachment card transfers the data word into the Series/1 main storage by "cycle stealing" storage cycles.

## Maintenance

Regular and proper preventive maintenance ensures a maximum level of both mechanical and data reliability. It is very important that the maintenance tasks be performed at the recommended intervals. The preventive maintenance routines may be found in the 4969 maintenance information manual.



# Chapter 2. Functional Units

## Operator Control Panel

### Power Switch/Indicator

This switch controls input power to the tape unit and controller feature. Within the power switch is an indicator that turns on when power is applied. The rocker is red and white. The indicator is located behind the white portion of the rocker.

### File Protect Indicator

This indicator is on when the file tape reel does not contain a write-enable ring. The absence of the write-enable ring prevents writing on the tape. When the write-enable ring is installed on the file reel, the indicator is turned off and writing is allowed.

### Load Switch/Indicator

Pressing the Load switch/indicator (after the tape is threaded) moves the tape to the load point, turns on the Load indicator, and puts the tape unit online. After the 4969 is online, the Load switch is functionally disabled. The Load switch is enabled again if tape tension is lost (model 4) or if vacuum in the vacuum chamber is lost (model 7).

### On Line Switch/Indicator

Pressing the On Line switch/indicator turns on the indicator and puts the 4969 online. (The unit automatically goes online when initially loaded.)

*Note:* The On Line switch/indicator controls the state of the 4969 as online or offline.

- When Online:
  - The 4969 accepts system commands only and disables all operator controls except Reset.
  - The 4969 can be taken offline by a system command, by breaking an interlock, or by pressing Reset.
- When Offline:
  - The 4969 is controlled manually from the operator control panel.
  - The 4969 can be put back online (if tape tension is present and interlocks are closed) by pressing On Line.

### Reset Switch

Pressing the Reset switch:

- Places the 4969 offline.
- Stops all tape motion unless an unload operation is already in progress.
- Clears all read, write, and control functions previously initiated.

### Forward Switch/Indicator

Pressing the Forward switch/indicator (disabled when the 4969 is online) turns on the indicator and moves the tape forward at read/write speed until the tape reaches the end-of-tape marker. (Tape motion can be stopped by pressing the Reset switch.)

### Reverse Switch/Indicator

This is a combination switch and indicator. The reverse switch is enabled when the unit is offline. Pressing the switch turns on the indicator and the tape accelerates in the reverse direction. Tape motion is stopped by pressing the Reset switch.

### Rewind Switch

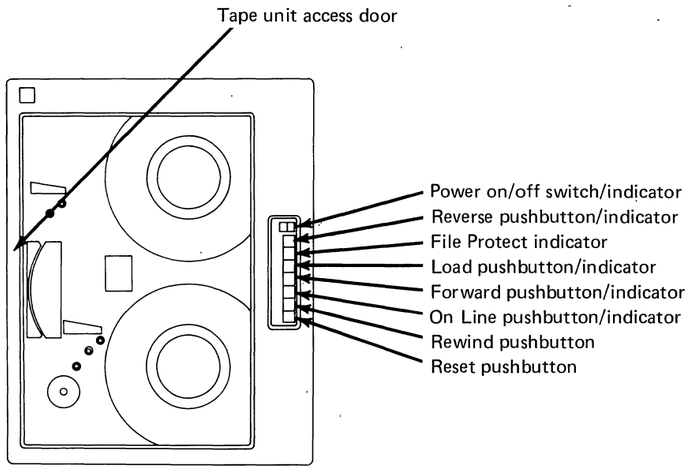
Pressing the Rewind switch causes the tape to rewind at high speed. (Rewinding can be halted by pressing the Reset switch.) Pressing the Rewind switch when the tape is at load point initiates an unload operation (the tape is drawn from the tape path).

*Notes*:

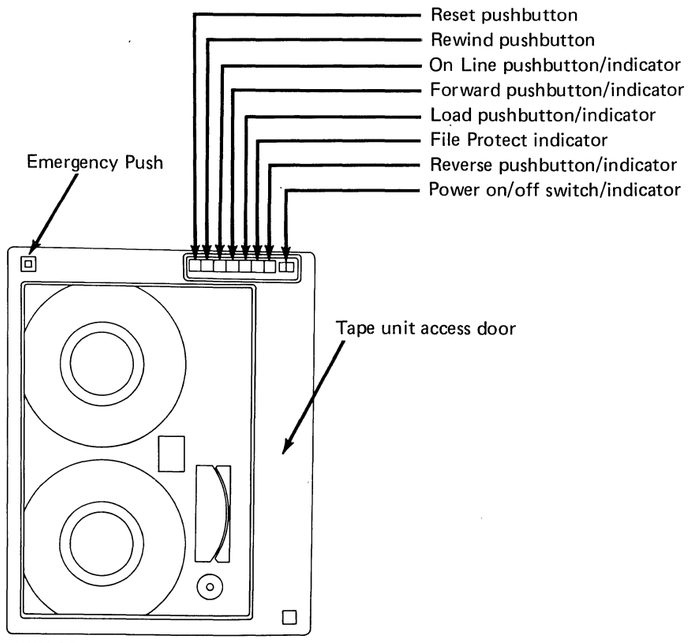
1. The Rewind switch is disabled when the unit is online.
2. On a model 7, the Rewind switch *is not* disabled when the front cover is open. Rewinding can be accomplished by pressing and holding the Rewind switch.

### Emergency Push Switch (Model 7 only)

Pressing the Emergency Push switch turns off all power to the unit. This switch should only be used for emergencies. To reset this switch, open the front cover and pull the button back out.




4969 Model 4




4969 Model 7

## CE Panel

There is a CE panel in each 4969 tape unit. The CE panel provides offline maintenance capability of each unit by the CE. The tape unit must be in the *On Line* mode to be able to perform any operations. Tapes written by the CE panel can only be read by its own CE panel.

### Transport Control Status

Light-emitting diodes display status information. Ready, rewinding, end of tape, file protect, beginning of tape, NRZI, and online are displayed.

- Ready (RDY)–This indicator is turned on when the tape unit is loaded and mechanically ready.
- Rewinding (RWD)–This indicator is turned on for a rewind operation. After the tape has returned to load point this indicator is turned off.
- End-of-tape (EOT)–This indicator is turned on when the end-of-tape reflective marker is under its photosensor. Forward tape motion generated by the CE panel will stop when the end-of-tape marker is sensed.
- Beginning-of-tape (BOT)–This indicator is turned on when the beginning-of-tape reflective marker is under its photosensor. Reverse tape motion generated by the CE panel will stop when the beginning-of-tape marker is sensed.
- NRZI–This indicator is turned on when the tape unit is NRZI only regardless of NRZI/PE data mode switch position. A dual mode tape unit will turn on this indicator when the data mode switch is in the NRZI position.
- File protect (FILE PROT)–This indicator is turned on when the file reel does not have a write-enable ring installed.
- On Line–This indicator is turned on anytime the online indicator is turned on at the operator control panel.

### Data Check

Tapes written by using the CE panel can be read with error checking. A missing bit or extra bit will turn on the error indicator. The dead track indicator is turned on when there is no data present for a single track. The tracks are sampled, for several bit times, one at a time for a read or read after write operation.

### Data Mode

The CE panel supports NRZI, PE, and dual-density tape units. A switch selects the recording mode to match the tape unit. A recording mode may also be selected by a switch that will write an all -1's pattern or alternate 1's and 0's.

### Run Mode

A run mode switch is provided to allow the tape unit to write or read continuously (CONT), or to write or read a record of predetermined length (PGM). A delay is established between records to ensure a correct IBG is written.

### Start/Stop

This switch initiates all commands from the CE panel to the tape unit. The command begins when the switch is moved from Stop to Start. Tape motion is stopped when this switch is moved to the Stop position except for a rewind and read operation (read operation will stop when an IBG is reached).

### Command Input

#### *Write*

The Write command writes the selected data mode and pattern in either continuous or fixed-length records.

#### *Read Forward (RD FWD)*

The Read Forward command reads tape in the forward direction and motion is stopped by placing the Start/Stop switch in the Stop position and the reaching of an IBG.

#### *Read Reverse (RD REV)*

The Read Reverse command reads tape in the reverse direction and motion is stopped by placing the Start/Stop switch in the Stop position and the reaching of an IBG.

#### *Servo Forward (SV FWD)*

The Servo Forward command, along with the program mode, sets up the required tape motion to check and adjust the forward start-stop ramp. In continuous mode, this command moves tape in the forward direction for adjustment of forward speed.

#### *Servo Reverse (SV REV)*

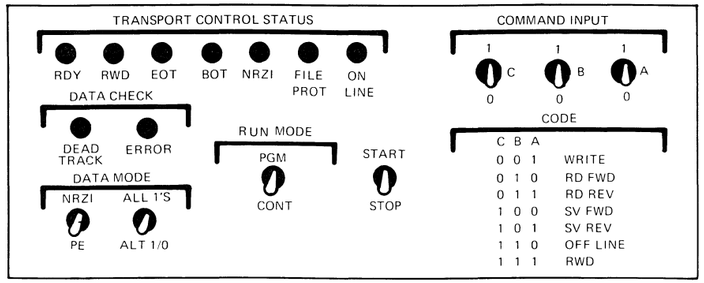
The Servo Reverse command, along with the program mode, establishes the required tape motion for checking and adjustment of the reverse start-stop ramp. With continuous mode set, tape motion in reverse direction is established for reverse speed adjustment.

#### *Off Line*

The Off Line command removes the tape unit from online mode and all status indicators are turned off.

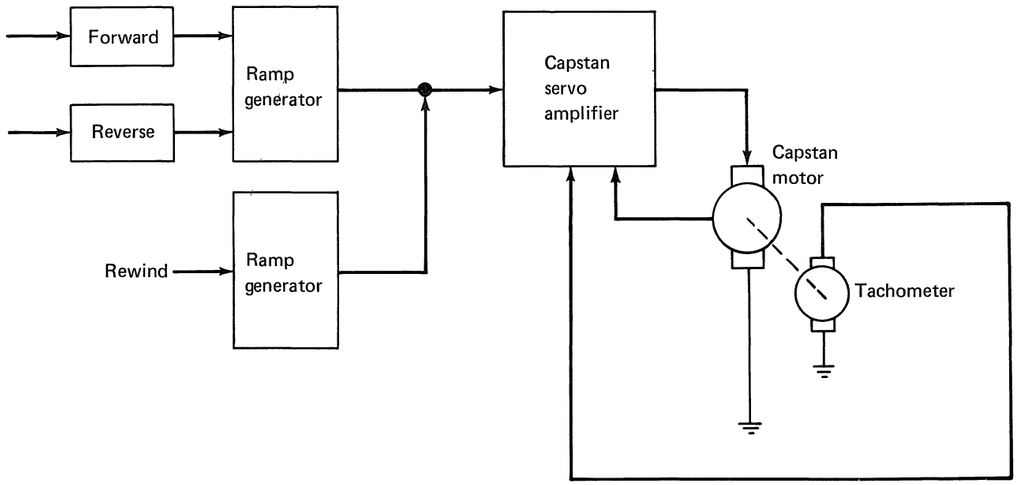
#### *Rewind (RWD)*

The Rewind command rewinds the tape to load point. The stop switch will not stop this operation.



## Capstan Drive and Servo System

All tape motion is initiated by the capstan, which is driven by a dc motor. When the motor is running, a tachometer provides a dc voltage to the capstan servo amplifier system to control the capstan speed and is adjustable for either 1.1 or 1.9 meter per second (45 or 75 inches per second). The capstan servo offset is adjusted to keep the capstan from turning until receiving a motion operation. There are two ramp generators used in the capstan servo system. One controls the nominal forward and reverse speeds; the other controls the rewind speed. Either a forward or reverse command to the ramp generator establishes tape motion in the appropriate direction. The distances traveled during acceleration or deceleration are such that an interblock gap (IBG) is generated. Symmetry of the start times, stop times, and distances traveled are achieved by adjusting the forward and reverse inputs to the ramp generator.




**Capstan drive and servo system**

## Tension Arm Unit (Model 4)

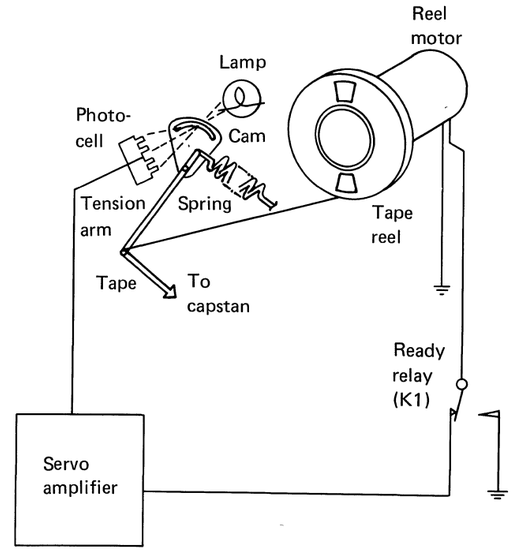
Two identical servo systems control the file and fixed reels.

### Tension Arm Position

A light-sensing circuit provides arm-position information to the servo amplifier that drives the reel motor. The tension arm position adjustment is made to center the tension arm in its operating range. As tape is delivered to the arm or taken from it, the arm moves up or down, and the position of the mask between the light source and the light-sensing element changes. When the mask is at the neutral position, the drive current to the reel motors is removed. The arm sense photocell board is adjusted to place the photocell in the center of its operating range.

### Reel Drive and Servo System

The reel servo amplifier gain is adjustable to establish the amplifier range for both the file and fixed reel servo amplifiers. During the rewind mode, the reel-motor servo-amplifier gain maintains tension on the tape. During the unload cycle, an offset signal is fed to each servo amplifier to bias each servo swing arm close to its respective stop. This ensures gentle handling of tape as it unloads from the reels. Spring tension on the tension arms is balanced by torque in the reel motors. If the power fails or servo operation is interrupted, the springs pull the arms out and into contact with limit switches that turn off all reel servo and capstan functions.



## Vacuum Column Unit (Model 7)

With tape threaded on the tape unit, a portion of the tape crosses the end of the vacuum column. A vacuum source at the opposite end of the vacuum column attempts to draw air in from the end of the column. Since air is drawn from the column and no more air can enter from the end, a vacuum is created in the column. The vacuum causes the tape at the end of the column to be positioned in the column.

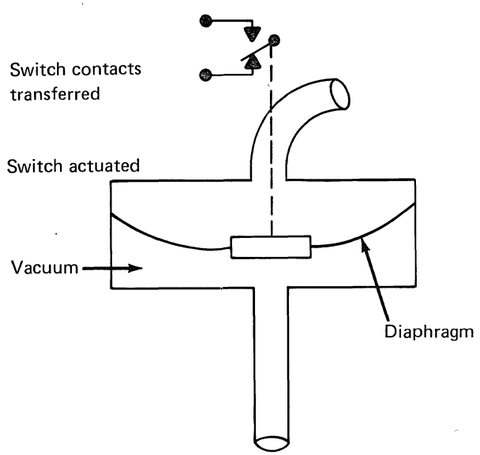
### Vacuum Blower

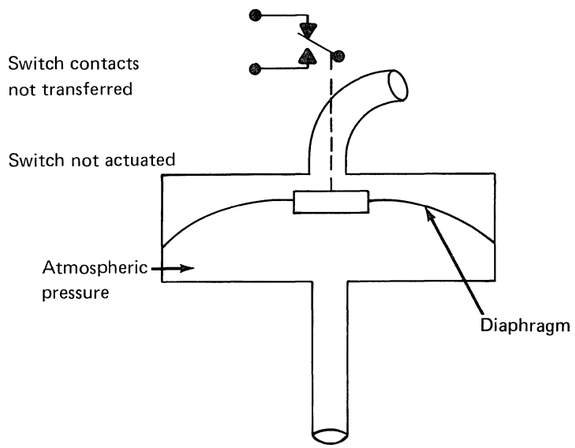
The vacuum blower consists of a centrifugal blower which is belt-driven by a motor. Air is drawn into the center of the blower from the vacuum column and exhausted from the blower.

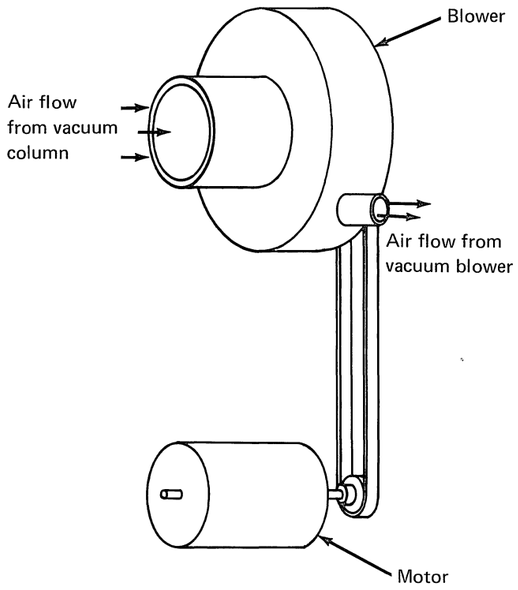
### Vacuum Switch

The vacuum switches are connected to the end port holes by hollow tubes. If vacuum is present at the end port holes the diaphragm of the switch is pulled toward the tube opening and the switch contacts are transferred. If atmospheric pressure is present at the end port hole, the diaphragm is in its normal position and the switch contacts not transferred. If the tape is not between the two ports, there is no pressure difference across the switch and the switch opens, breaking the tape interlock, stopping tape movement, and removes vacuum from the vacuum columns.

Vacuum sensing holes in each of the vacuum columns senses the position of the loops of tape.

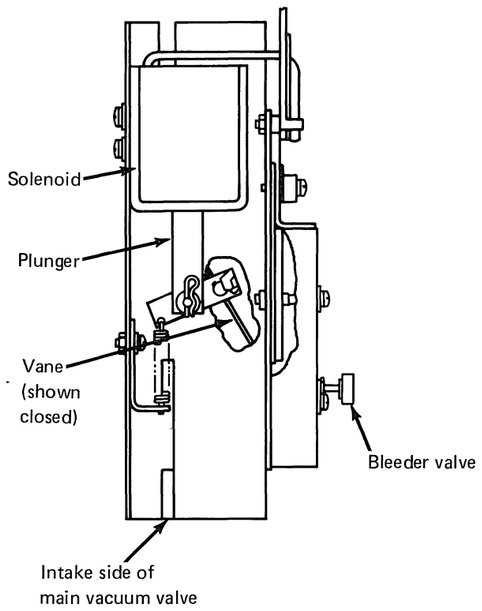


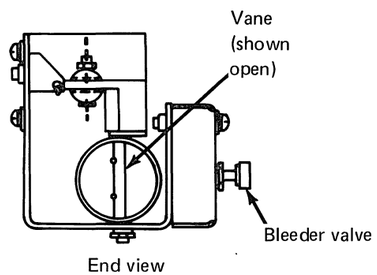




### Main Vacuum Valve

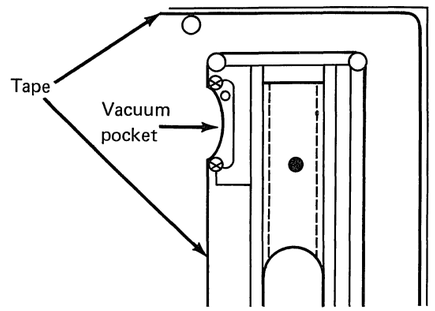
The main vacuum valve controls vacuum to the vacuum columns and vacuum pocket. Vacuum is not applied to the columns when the valve is closed. The amount of vacuum is adjustable by the air bleed located on the main vacuum valve.




### Vacuum Pocket

The vacuum pocket is used to produce light tape tension for a small length of tape so the capstan can start with less load in the forward direction.

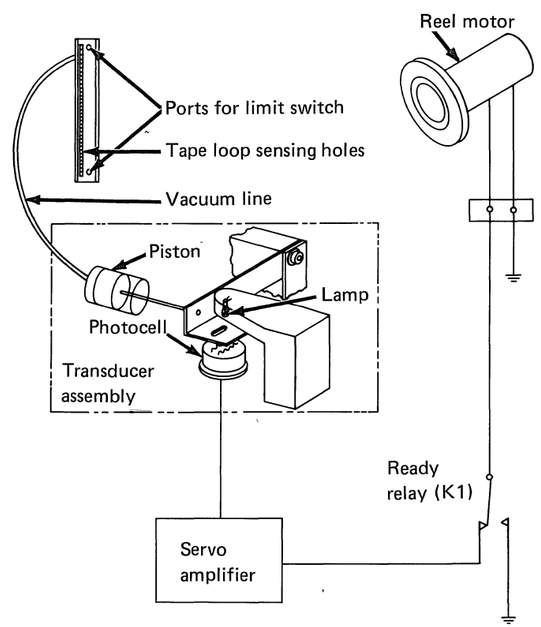



### Reel Drive and Servo System

Two identical servo systems control the file and fixed reels.

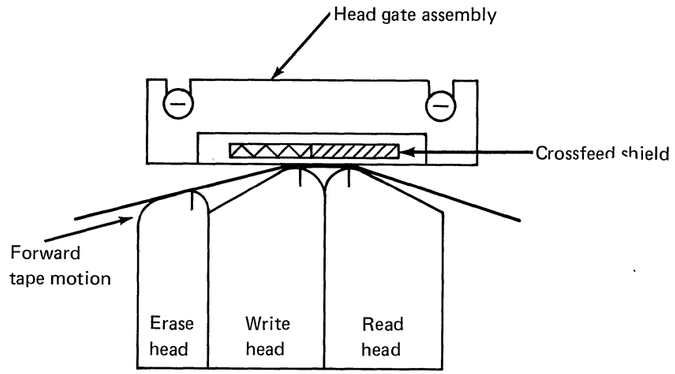
Tape loop sensing holes cause a vacuum-operated, light-sensing circuit, to provide tape loop information to the servo amplifier that drives the reel motors. In rewind mode, the amplifier gain is changed electronically to maintain tension on the tape.

The servo amplifier gain is adjusted for full excursion of tape within the vacuum columns. The transducer alignment is performed with the tape loops located in the center of each column to get proper transducer output levels.



## Read/Write Head Assembly

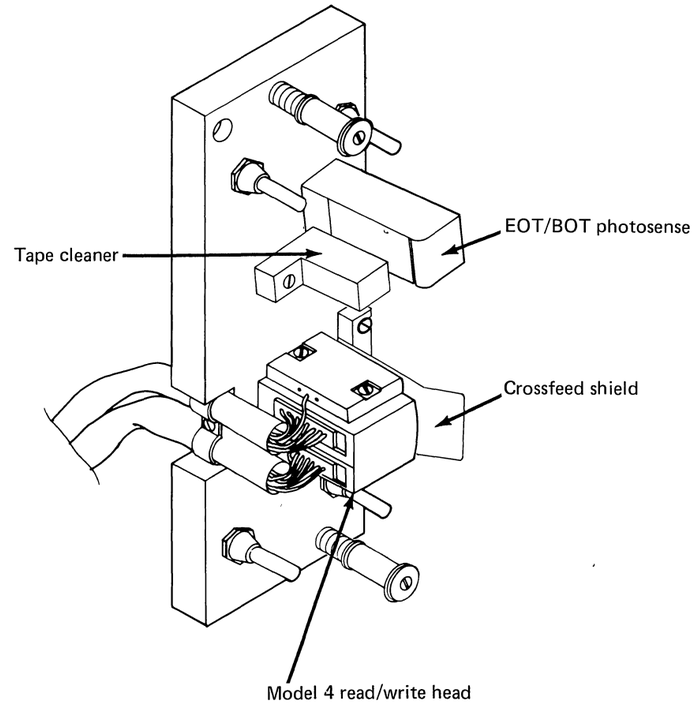
A dual-gap read-after-write head is used with a full-width erase head located on the oxide side of the tape. Head azimuth is adjusted by shimming one of two fixed head guides. This adjustment ensures that the tape path is properly aligned to the read head. Also the write stack deskew adjustment (NRZI and Dual units only) is made to electrically deskew the write head to match the read head so that each byte of data is written in a straight line.




**Read/write head assembly**

### Crossfeed Shield

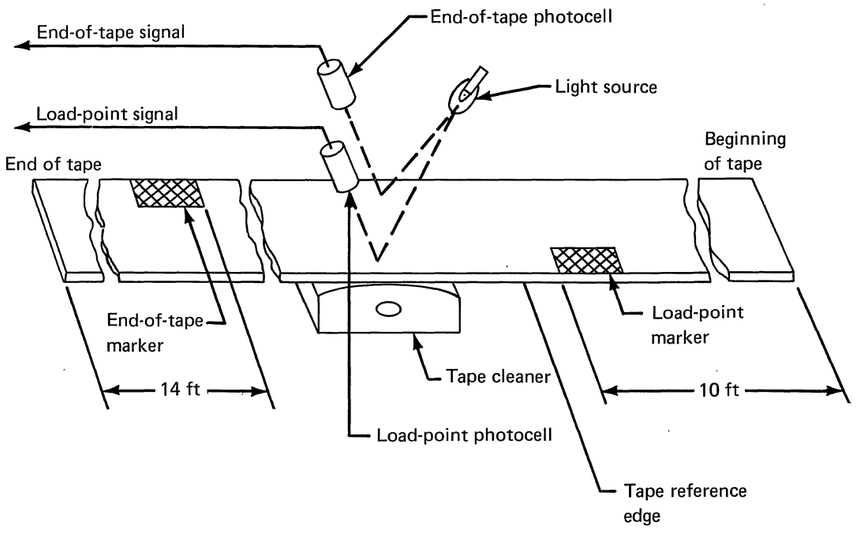
During a write operation, magnetic lines of force (flux) from the write gap pass through the oxide coating on the tape. Some of these flux lines extend beyond the tape and reach the read head, inducing noise in the read head windings. The cross feed shield prevents the extended flux lines (feed through) from reaching the read head.




Model 4 read/write head

### EOT/BOT Photosense

The EOT/BOT senses when either end of the tape reached. The ends of tape are sensed by a light source that reflects from markers on the tape to a pair of photocells. These photosensors are adjusted with tape present and no reflective markers present.



## Power Supply

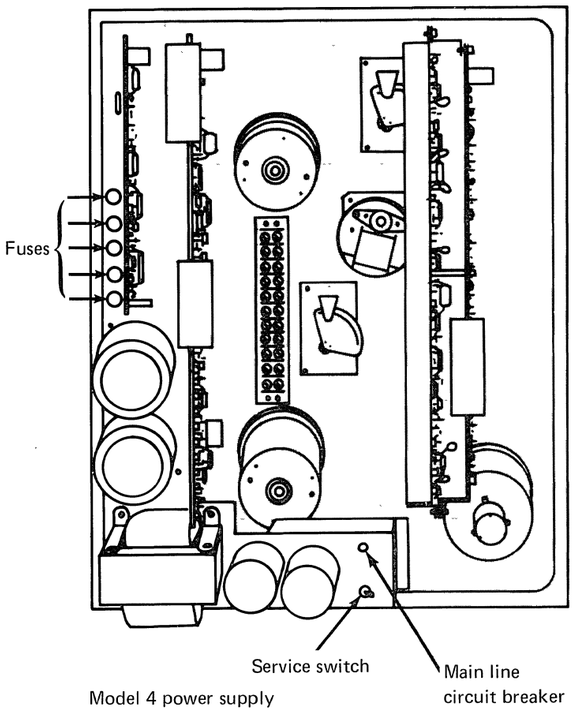
The power supply consists of transformer, rectifier, filter, and regulators that supply power to the capstan, reel motors, data electronics, and control electronics. The ac power to the tape unit is controlled by a switch on the power supply chassis and a switch on the operator control panel. The switch on the power supply chassis must be switched on before the operator control panel switch can be used to control power.

### Model 4

The model 4 power supply provide all of the ac and dc power used within the tape unit; it uses single-phase ac power source to provide ac voltages to the motors, cooling fan, controller feature (if installed), and the following voltages:

- +13 volts, −13 volts, +19 volts, −19 volts, +5 volts, and +12 volts for the transport electronics
- +5 volts, −12 volts, and +12 volts for data electronics

Also contained within the power supply is the ready relay (K1) which provides transport ready and servo motor controls.



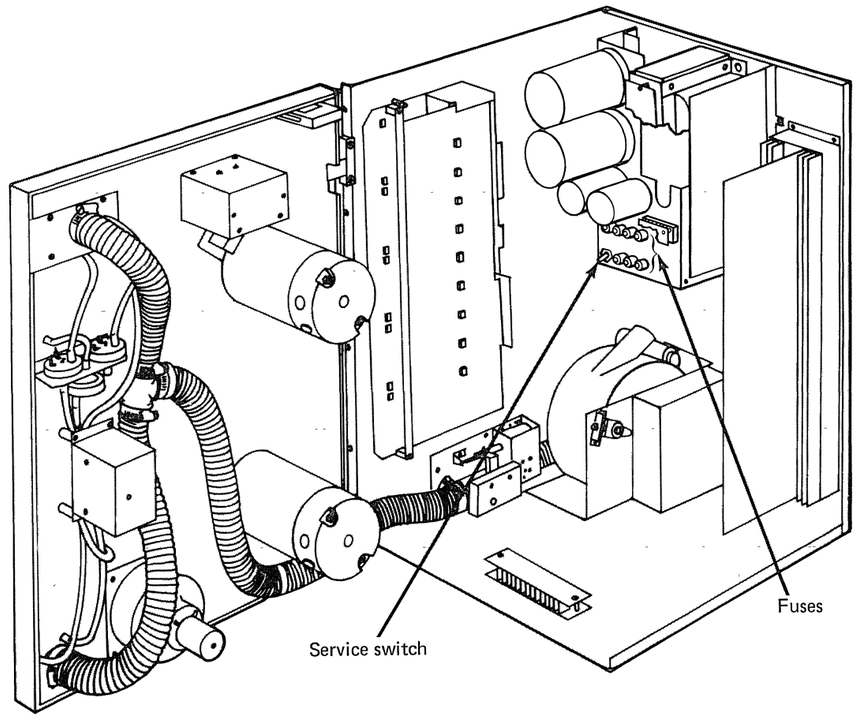

Model 4 power supply

### Model 7

The model 7 power supply provides all of the ac and dc power used within the tape unit; it uses single-phase ac power source to provide ac voltages to the motors, cooling fan, controller feature (if installed), and the following voltages:

- −44 volts, +44 volts, +24 volts, −24 volts, +5 volts, and +12 volts for the servo electronics
- −24volts, +24 volts, +5 volts, −12 volts, −5 volts, and +12 volts for the transport control logic
- +5 volts, −12 volts, and +12 volts for data electronics

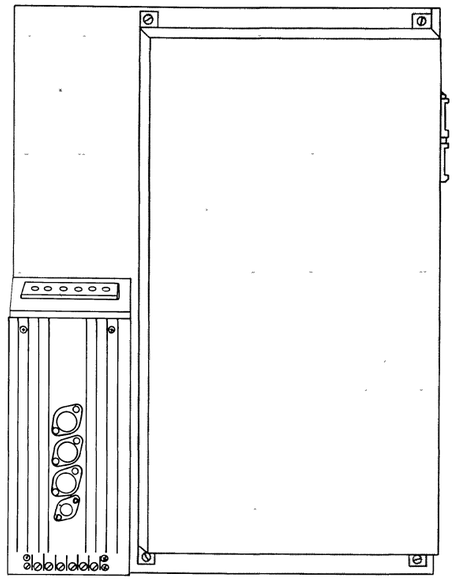
Also contained within the power supply is the ready relay (K1) which provides transport ready and servo motor controls.




Model 7 power supply

### Controller Feature

For tape units that contain the controller feature a power supply is located on the rear of the tape unit and supplies +5 volts for the adapter card and the control board.



Rear view showing controller feature power supply

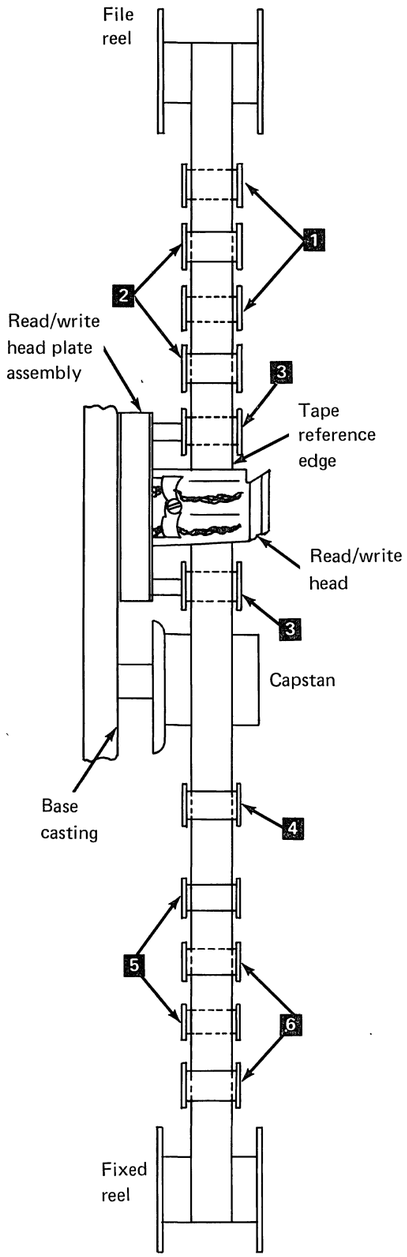
## Tape Tracking

Correct tape tracking is the mechanical alignment of the tape path elements so that tape passes from reel to reel without damage, in parallel path to the transport and perpendicular to the read/write head.

### Model 4

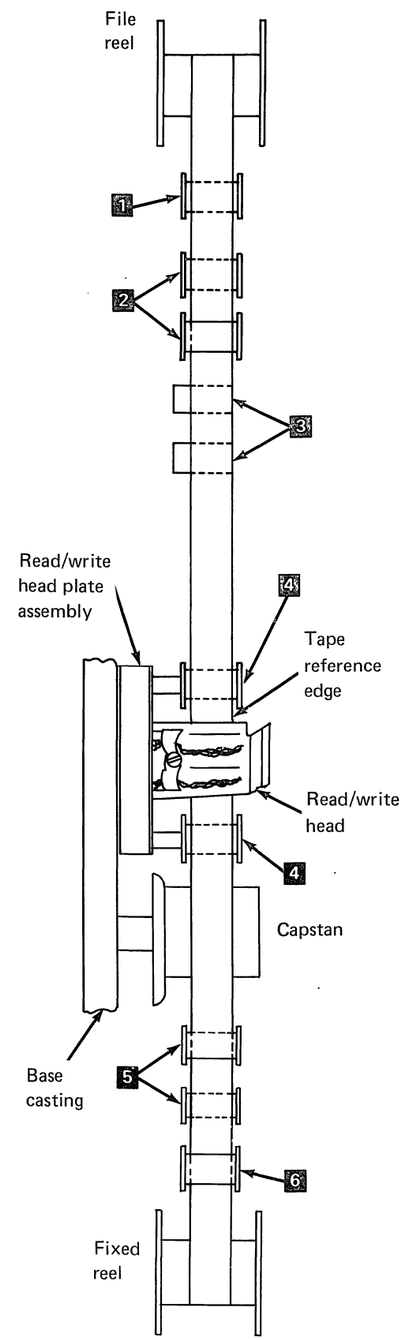
Forward tracking is controlled by guides between the file reel and capstan, which include the capstan, upper tension arm roller guides 2, and deck mounting guides 1.

Reverse tracking is controlled by guides between the fixed reel and capstan, which include the capstan, lower tension arm roller guides 5, deck mounting guides 6, and reverse tracking roller 4. The head guides 3 are used for adjusting the head azimuth.

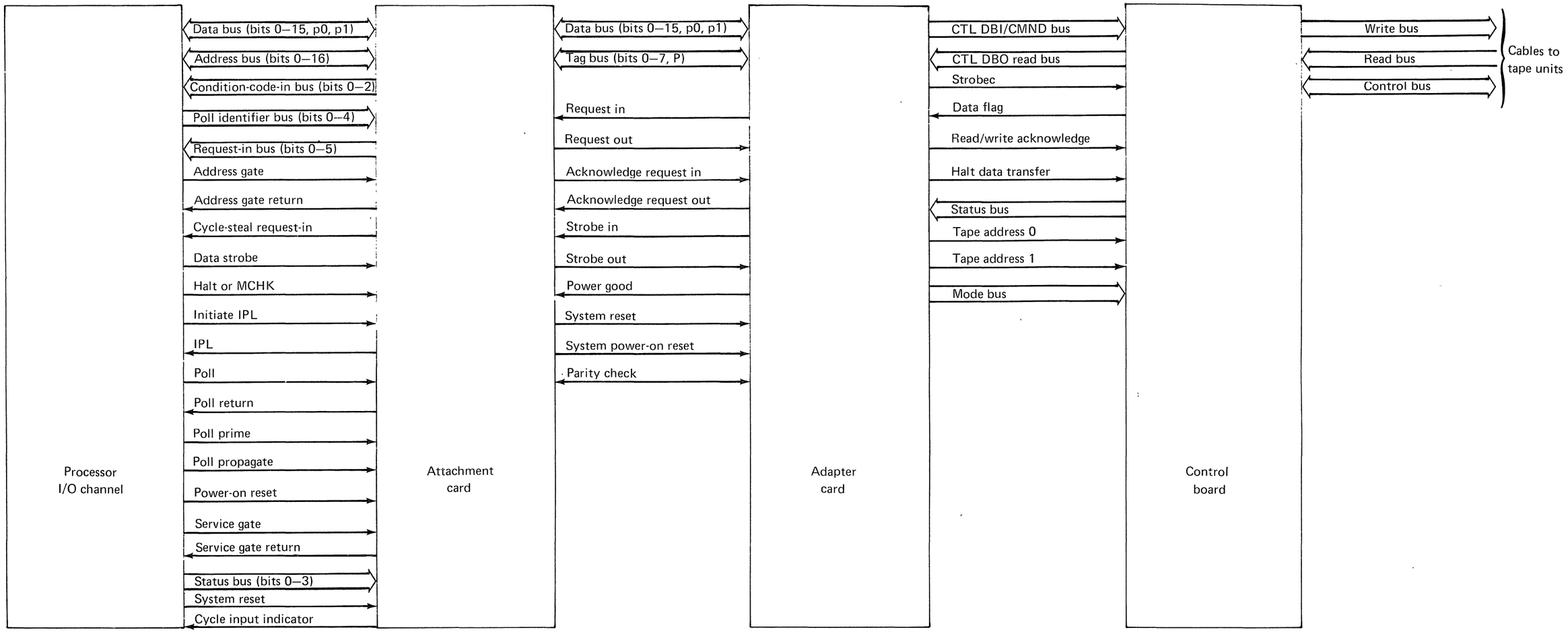



### Model 7

Tape tracking on the model 7 is adjusted with reference to the vacuum column. Forward tracking is controlled by guiding elements between the file reel and capstan and include the capstan and deck mounting guides (file-reel vacuum column) 2. Reverse tracking is controlled by guiding elements between the fixed reel and capstan and include the capstan and deck mounting guides (fixed-reel column) 5. The tape guides at 1 and 6 are used for loading only and do not affect tape tracking. Located at 3 are the vacuum pocket rails which also do not affect tracking. The head guides 4 are used for adjusting the head azimuth.



# Chapter 3. Circuit Functions


Data bus (bits 0–15, p0, p1)
Address bus (bits 0–16)
Condition-code-in bus (bits 0–2)
Poll identifier bus (bits 0–4)
Request-in bus (bits 0–5)
Address gate
Address gate return
Cycle-steal request-in
Data strobe
Halt or MCHK
Initiate IPL
IPL
Poll
Poll return
Poll prime
Poll propagate
Power-on reset
Service gate
Service gate return
Status bus (bits 0–3)
System reset
Cycle input indicator
Processor I/O channel
Data bus (bits 0–15, p0, p1)
Tag bus (bits 0–7, P)
Request in
Request out
Acknowledge request in
Acknowledge request out
Strobe in
Strobe out
Power good
System reset
System power-on reset
Parity check
Attachment card
CTL DBI/CMND bus
CTL DBO read bus
Strobec
Data flag
Read/write acknowledge
Halt data transfer
Status bus
Tape address 0
Tape address 1
Mode bus
Adapter card
Write bus
Read bus
Control bus
Cables to tape units
Control board

## Line Descriptions

The diagram on the previous page shows the signal lines that connect the processor I/O channel, attachment card, adapter card, control board, and the tape unit. The following paragraphs describe these lines; the diagram is repeated on succeeding pages for ease of reference.

### Processor I/O Channel to Attachment Card

#### Data Bus (Bits 0–15, P0, and P1)

The data bus is an 18-bit bidirectional bus that is capable of carrying two eight-bit bytes of data (bits 0–15) and two parity bits (P0 and P1); it transfers data and control information between the processor and the attachment. Parity bit P0 is used to maintain odd parity for bits 0–7; parity bit P1 is used to maintain odd parity for bits 8–15.

During command sequences, data-bus bits 0–15 contain the same information as bits 16–31 of the IDCB.

During interrupt service sequences, the data bus transfers the interrupt identification (ID) word to the processor. Data bus bits 0–15, sent by the attachment to the processor, are equal to bits 0–15 of the interrupt ID word.

When leaving the processor, bits 0–15 are the same as the contents of the word at the main storage location that is addressed by the attachment. The attachment specifies that output is taking place by not activating 'cycle input indicator.' When entering the processor, bits 0–15 are the same as the contents of the cycle steal data register in the attachment. The attachment specifies that an input word transfer is taking place by activating 'cycle input indicator'.

Odd parity is maintained on the data bus during all I/O sequences.

#### Address Bus (Bits 0–16)

The address bus is used for direct program control (DPC) selection of the 4969 and for storage address presentation by the cycle-stealing tape unit. The address bus is 17 bits wide; it is received by all attachments installed on the processor I/O channel. All I/O devices that are capable of cycle-stealing activate bits 0–15. The processor activates bits 0–16.

During DPC sequences, address-bus bits 0–15 are equal to bits 0–15 of the first word of the immediate device control block (IDCB). If bit 16 is active, it indicates that a DPC sequence is taking place. During a cycle-steal data transfer, the attachment places the main storage address on the address bus, using bits 0–15.

During a main storage access, address bits 0–15 represent a main storage address. Bit 16 is not used, which indicates to the processor that a main storage access is taking place.

#### Condition Code In Bus (Bits 0–2)

The condition-code-in bus is a three-bit bus used by the attachment to send I/O instruction condition codes, interrupt condition codes, or cycle-steal address key information to the processor I/O channel. Condition-code-in information is sent to the channel with the appropriate inbound tag (either 'address gate return' or 'service gate return') during command, interrupt, and cycle-steal sequences.

Information on the condition-code-in bus is valid from the time that either 'address gate return' or 'service gate return' becomes active until the time that either 'address gate' or 'service gate' becomes inactive.

#### Poll Identifier Bus (Bits 0–4)

The poll-identifier bus is a five-bit bus that is used to identify the type of poll occurring on the processor I/O channel. The channel places a value on the poll-identifier bus prior to activating the 'poll' tag; the value remains valid until the channel receives 'poll return'.

The meanings of the poll-identifier bus bits are:

| Bits 0 1 2 3 4 | |
|---|---|
| 0 0 0 0 0 | Poll for interrupt level 0 |
| 0 0 0 0 1 | Poll for interrupt level 1 |
| 0 0 0 1 0 | Poll for interrupt level 2 |
| 0 0 0 1 1 | Poll for interrupt level 3 |
| 1 0 0 0 0 | Quiescent value |
| 1 X X 1 1 | Poll for cycle-steal |

#### Request-In Bus (Bits 0–3)

The request-in bus is a four-bit bus used by the attachment to either present an interrupt request or to access main storage.

When the attachment detects an interrupt condition, it turns on one of the request-in bus bits. The level field of the Prepare command determines which bit is activated.

The attachment can turn on an interrupt request bit only when the I-bit (bit 31 of the IDCB for a Prepare command) equals 1. The interrupt request remains active until the attachment captures a poll, receives 'halt or MCHK,' receives a device or system reset, or receives 'power-on reset.'

#### Address Gate

When 'address gate' (an outbound tag) is active, it indicates that the attachment can now respond to initial selection and can begin executing the command specified by bits 0–7 on the address bus.

#### Address Gate Return

The attachment activates 'address gate return' to indicate that it has received 'address gate,' that immediate status is on the conditioncode-in bus, and that data is on the data bus if bit 1 of the address bus equals 0.

If 'address gate return' does not become active after 'address gate' becomes active, I/O instruction condition code 0 (device not attached) is generated, the sequence is terminated, 'address gate' becomes inactive, and the address bus is reset.

#### Cycle-Steal Request-In

The attachment activates 'cycle-steal request-in' if a tape unit must use cycle-steal mode to access main storage. The line remains active until the attachment feature receives a poll, 'halt or MCHK,' 'system reset,' or 'power on reset.'

#### Data Strobe

'Data strobe' is an outbound tag to the attachment. It is activated during command, interrupt, or cycle-steal service sequences.

#### Halt or MCHK

'Halt or MCHK' is an outbound tag that indicates that either a Halt command has been encountered in the program or that a machine-check class interrupt has occurred. This tag resets any error or busy conditions that exist in the tape subsystem.

#### Initiate IPL

'Initiate IPL' is an outbound tag from the processor I/O channel to the IPL source on the system. 'Initiate IPL' is a signal to the IPL source that the processor requires an IPL. It is held active until the IPL source responds with 'IPL.' Bits 0 and 1 of the status bus are used to select the primary or alternate IPL source, respectively; the bit is turned on concurrently with 'initiate IPL.'

#### IPL

'IPL' is an inbound signal activated by the IPL source attachment either to respond to 'initiate IPL' or to indicate to the processor that another processor is initiating the IPL. The IPL information is loaded into storage using cycle-steal sequences.

The attachment activates 'IPL' and begins transferring information to the processor after the processor performs a system reset. 'IPL' remains active until the IPL is complete.

#### Poll

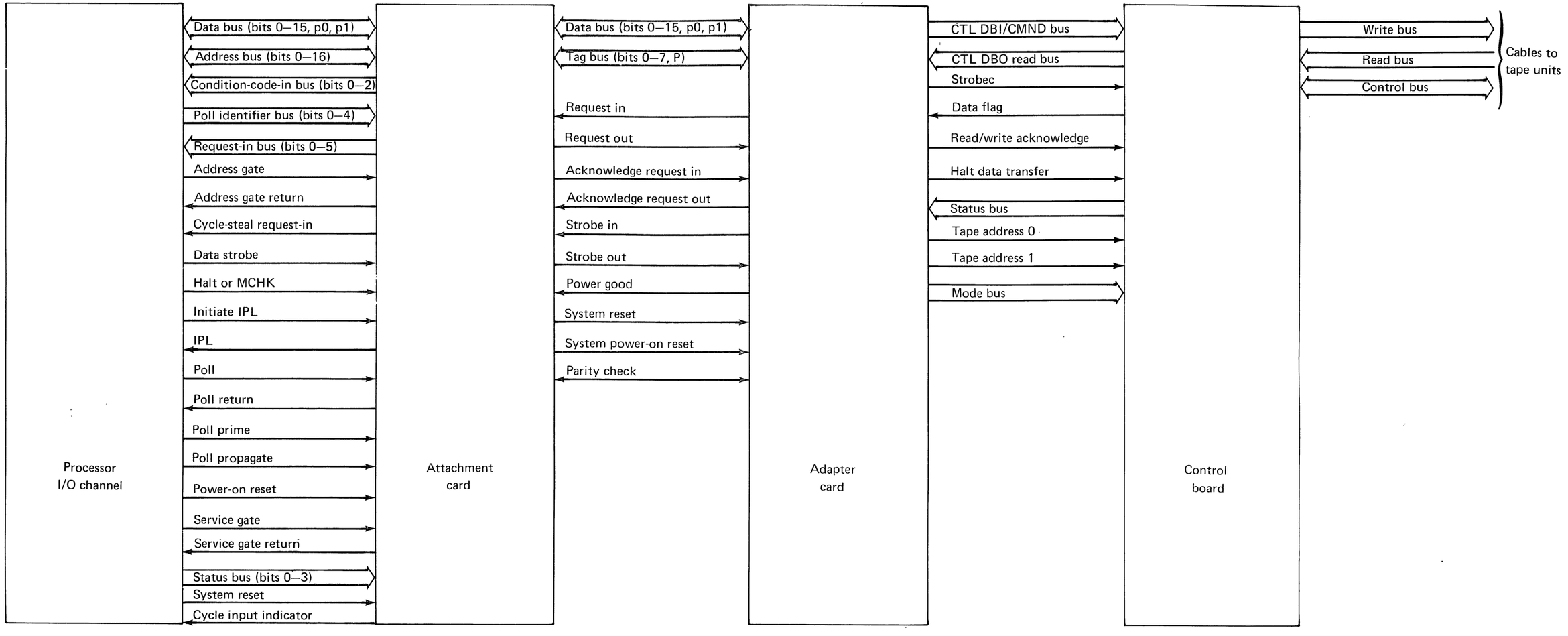
'Poll' is generated by the processor I/O channel and is sent serially to all attachments on the channel. The purpose of this tag is to resolve any contentions that exist between two or more attachments, on the same level, that have interrupt requests or cycle-steal requests pending.

#### Poll Return

'Poll return' is used to signal the channel control logic that an I/O device has accepted a polling sequence. 'Poll return' must remain active until 'poll' goes inactive.

#### Poll Prime

'Poll Prime' is a line that is connected to the same back-panel pin as 'poll' but connects to a different back-panel pin on the *next* I/O attachment card position.


Data bus (bits 0–15, p0, p1)
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Status bus (bits 0–3)
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Tag bus (bits 0–7, P)
Request in
Request out
Acknowledge request in
Acknowledge request out
Strobe in
Strobe out
Power good
System reset
System power-on reset
Parity check
Attachment card
CTL DBI/CMND bus
CTL DBO read bus
Strobec
Data flag
Read/write acknowledge
Halt data transfer
Status bus
Tape address 0
Tape address 1
Mode bus
Adapter card
Write bus
Read bus
Control bus
Cables to tape units
Control board

### Poll Propagate

If an interrupt or a cycle-steal request is not pending, the attachment relays 'poll' to the next device on the I/O channel by activating 'poll propagate'.

When 'poll' and 'poll prime' are received by the attachment, the attachment recognizes that a poll is occurring. The attachment compares the poll ID bits from the processor I/O channel with the ID bits in the prepare level register. An equal compare of the poll ID bits logically ANDed with 'poll' and 'poll prime' is called a poll capture. Once the poll is captured, the attachment responds with 'poll return.' If the poll capture does not occur, the 'poll' is propagated to the next device on the channel and the attachment takes no further action until the next poll occurs.

Because of the serial nature of 'polling', the physical position of the attachment on the channel determines the priority for servicing contending cycle-steal and interrupt requests that occur at the same interrupt level. The attachments that are located in positions closest to the processor are the first attachments in the polling chain and, therefore, have the highest priority.

However, if the attachment receives a power on reset, a system reset, or a 'halt or MCHK,' 'poll propagate' is deactivated regardless of the state of the 'poll' tag.

### Power-On Reset

'Power-on Reset' is a control line sent by the power supply in the processor to all system components; it holds them in a system reset state. 'Power on reset' is activated during power-on or power-off sequences.

### Service Gate

The outbound 'service gate' indicates to the attachment that a cycle-steal or interrupt service sequence can begin, if the attachment captured the last poll.

### Service Gate Return

'Service gate return' is sent by the attachment to the I/O processor channel to indicate that it has recognized 'service gate' and that the inbound information required by either the cycle-steal sequence or the interrupt service sequence has been placed on the condition-code-in bus.

### Status Bus (Bits 0–3)

The status bus is a four-bit outbound bus used by the processor I/O channel to indicate to the attachment that an error condition has been detected. The bits have the following meaning:

| Bit | Meaning |
|---|---|
| 0 | Storage data check |
| 1 | Invalid storage address |
| 2 | Protect check |
| 3 | Interface data check |

The attachment retries the specified operation one time for these error conditions when the suppress exception (SE) bit of the DCB control word equals 1. If the operation fails a second time, a hard error condition is posted (condition code 2 or 6) and the appropriate bit in the interrupt ID word is set to 1.

The attachment retains this information in the interrupt status byte for presentation to the processor I/O channel by using the interrupt ID word at interrupt presentation time. Bits 0–3 of the status bus are equal to bits 4–7 of the interrupt ID word.

### System Reset

'System reset' is sent by the channel to all I/O devices. It resets any error or busy conditions that exist in the tape subsystem.

### Cycle Input Indicator

'Cycle input indicator' defines the direction of data transfer over the data bus. 'Cycle input indicator' is activated by either the attachment or by the processor when a data transfer *to* main storage occurs. When a data transfer *from* main storage occurs, it is not activated.

This line is valid from the activation of 'service gate return' until the deactivation of 'service gate'; it must not change state during this period.

## Attachment Card to Adapter Card

### Data Bus (Bits 0–15, P0, and P1)

Two bytes of data (plus a parity bit for each byte) are transferred in parallel either to or from the attachment using the data bus. The bidirectional data bus lines are gated to the tape adapter during write operations and are gated to the attachment during read operations.

### Tag Bus (Bits 0–7 and P)

The tag bus lines define the type of operation that is occurring between the attachment and the tape adapter. Five lines (bits P, 0, 1, 2, 3) are bidirectional; four lines (bits 4, 5, 6, 7) are outbound lines. During an inbound sequence, only bits P, 0, 1, 2, and 3 are used. The parity bit is used to maintain odd parity for these bits. During an outbound sequence, bits P, 0, 1, 2, 3, 4, 5, 6, and 7 are used. The parity bit, in this instance, is used to maintain odd parity for all bits.

### Request In

'Request in' is an inbound control line activated by the adapter. It indicates to the attachment that the tape unit either has data to transfer or requires an interrupt request. This line gates the tag bus bits P, 0, 1, 2, and 3 to the attachment.

### Request Out

'Request out' is activated by the attachment when it has data to transfer to the adapter card. The nine outbound tag bus lines are gated by 'request out.' If 'request out' and 'request in' become active simultaneously, 'request out' takes precedence over 'request in.' Under these conditions, 'request in' is deactivated and inhibited by the adapter card; however, 'request out' is not activated if 'request in' has been accepted by the attachment. The attachment indicates that it has accepted 'request in' by activating 'acknowledge request in.'

### Acknowledge Request In

The attachment activates 'acknowledge request in' in response to 'request in' from the adapter card. When 'acknowledge request in' becomes active, it indicates that the attachment is ready to begin the type of operation defined by the tag bus lines.

### Acknowledge Request Out

The adapter card activates 'acknowledge request out' in response to 'request out' from the attachment, indicating that the adapter is ready to begin the type of operation defined by the 'tag bus' lines. If a parity check occurs on the tag register bus, 'parity check' is activated instead of 'acknowledge request out.'

### Write Data End

The attachment activates 'write data end' to terminate a write record operation.

### Record Length Counter

The tape unit controls activate 'record length counter' to reduce the value in the record length counter for each byte of data transferred to or from the tape unit. On read operations, the counter value is compared to the byte count to calculate the overflow byte count.

### Strobe In

'Strobe in' is an inbound line used to gate data from the adapter into the attachment data register. Data is gated into the register at the leading edge of 'strobe in' and latched into the register at the trailing edge.

### Strobe Out

'Strobe out' is an outbound line from the attachment to the adapter card. It is used by the adapter card to latch the data into the data register.

### Power Good

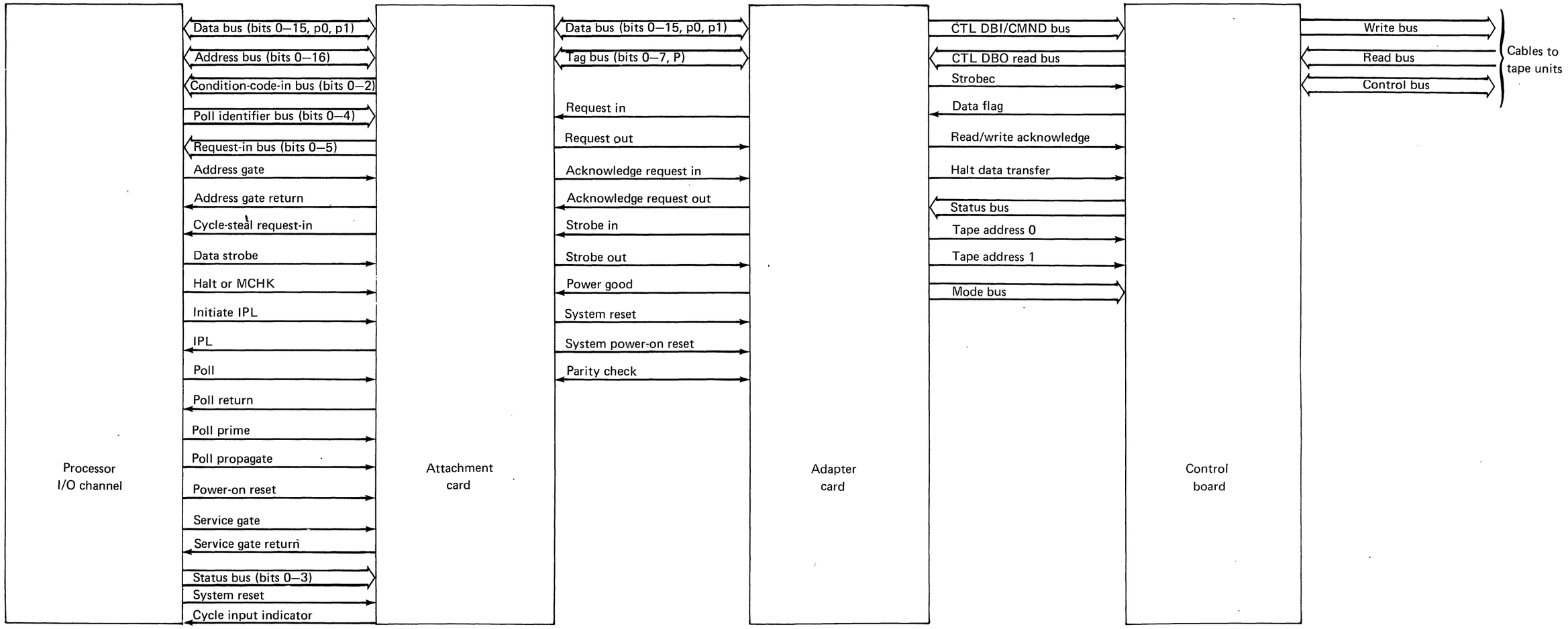
'Power good' is activated by the tape unit controls to inhibit 'strobe in' and 'request in' lines going to the attachment when a "power good" condition does not exist in tape unit 0.

### System Reset

'System reset' is an outbound line from the attachment used to reset the tape unit controls to a nonbusy, error-free, cleared state. The line is activated when 'halt or MCHK,' 'power-on reset,' or 'system reset' from the processor I/O channel becomes active.

### System Power-On Reset

During a system power-on reset, the attachment sends 'system power-on reset' to the adapter to initialize the tape unit controls to a known cleared state. It performs the same functions as 'system reset.'


Data bus (bits 0–15, p0, p1)
Address bus (bits 0–16)
Condition-code-in bus (bits 0–2)
Poll identifier bus (bits 0–4)
Request-in bus (bits 0–5)
Address gate
Address gate return
Cycle-steal request-in
Data strobe
Halt or MCHK
Initiate IPL
IPL
Poll
Poll return
Poll prime
Poll propagate
Power-on reset
Service gate
Service gate return
Status bus (bits 0–3)
System reset
Cycle input indicator
Processor I/O channel
Data bus (bits 0–15, p0, p1)
Tag bus (bits 0–7, P)
Request in
Request out
Acknowledge request in
Acknowledge request out
Strobe in
Strobe out
Power good
System reset
System power-on reset
Parity check
Attachment card
CTL DBI/CMND bus
CTL DBO read bus
Strobec
Data flag
Read/write acknowledge
Halt data transfer
Status bus
Tape address 0
Tape address 1
Mode bus
Adapter card
Write bus
Read bus
Control bus
Cables to tape units
Control board

**Parity Check**

'Parity check' is a bidirectional line that is activated when an out-of-parity condition is detected on either the data bus or the tag bus. The direction in which 'parity check' is sent is determined by the origin of the previous request. If the previous request was a 'request in,' the attachment activates the line; if the previous request was a 'request out,' the adapter activates the line.

Data parity is checked during the 'strobe in' or 'strobe out' pulses. The tape unit controls must reset 'parity check' before deactivating 'acknowledge request out' or before activating the next 'request in.'

## Adapter Card to Control Board

**CTL DBI/CMND Bus (Bits 0–7 and P)**

The CTL DBI/CMND bus is a nine-bit bus used to transfer a byte of data from the adapter card to the control board. Command information is also sent on this bus when 'strobec' is active.

**CTL DBO Read Bus (Bit 0–7 and P)**

The CTL DBO Read bus is a nine-bit bus used to transfer the nine-bit tape character from the control board to the adapter card.

**Strobec**

'Strobec' is activated by the adapter card to indicate to the control board that the CTL DBI/CMND bus contains command information.

**Data Flag**

'Data flag' is activated by the control board for both read and write operations. It is activated on a write operation to indicate that a byte of data is needed by the control board; it is activated on a read operation to indicate that data is available on the CTL DBO Read bus.

**Read/Write Acknowledge**

'Read/Write acknowledge' is activated by the adapter card in response to 'data flag' from the control board.

**Halt Data Transfer**

'Halt data transfer' is activated by the adpater card on write operations to terminate the data transfer requests ('data flag').

**Status Bus**

The status bus is used to indicate the following status:

- End of tape
- Command reject
- NRZI or PE
- Timing error
- Parity error
- Tape mark
- Ready
- Rewinding
- File protect
- Load point
- Identity burst detected
- Corrected error

**Tape Address 0 and 1**

These lines are decoded by the control board to select one of the four tape units.

| Tape address 0 | Tape address 1 | Tape unit selected |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

**Mode Bus**

These lines are activated by the adapter card to select read threshold low, PE (high density), and test read mode.

## Control Board to Tape Unit

**Write Bus (Bits 0–7, P, and Strobe)**

The write bus is used to transfer data to the selected tape unit along with the write data strobe (WDS) pulse. There is one write data line for each data bit in a tape character.

**Read Bus (Bits 0–7, P, and Strobe)**

The read bus is used to transfer data to the control board along with the read data strobe (RDS) pulse. There is one read data line for each data bit in a tape character.

**Control Bus**

The control bus is used to transfer control information from the control board to the tape unit. The following controls are sent:

- Forward
- Reverse
- Rewind
- Offline
- Tape unit select (0–3)
- Write enable
- Read threshold low
- Write amplifier reset
- PE (high density)

It is also used to transfer status information from the tape unit to the control board. The following status is reported

- Ready
- Online
- Rewinding
- File protect
- Load point
- End-of-tape
- Tape unit type (PE or NRZI)
- Density selected (PE or NRZI)

### Attachment Card

The attachment card physically connects and logically adapts the processor I/O channel to the tape units.

It consists of the following components:

- A digital controller
- Two 16-bit (plus two parity bits) I/O data registers that provide a cycle-steal data bypass (with minimum controller intervention) between the processor I/O channel and the tape unit controls, using auto mode
- Interrupt status and control circuits for the processor I/O channel and the tape unit controls

The attachment's digital controller performs the following functions:

- Interprets the immediate device control block (IDCB) of the Operate I/O instruction
- Executes the IDCB command
- Fetches, in cycle-steal mode, the device control block (DCB) specified by the IDCB
- Controls the starting and stopping of the automatic cycle-steal data transfers in auto mode
- Monitors and checks the accuracy of all data transfers
- Reports status information and condition codes, and handles interrupt requests going to the processor
- Performs error-recovery procedures
- Executes and monitors built-in diagnostic programs
- Accommodates variable-length initial program load (IPL) records (up to 64K bytes)
- Allows the attachment circuits to be tested without disconnecting the cables between the attachment and the tape unit controls
- Optimizes data transfers when instructions are issued to more than one tape unit

Information is transferred from the processor I/O channel to the tape unit controls in either command mode or auto mode. Command mode includes all attachment-initiated transfers that are begun by activating 'request out.' In this mode, the data passes through the controller that is in the attachment. In the data mode, data is transferred using the high-speed cycle-steal data bus. The data mode is the normal mode of operation for data transfers. In this mode, the controller acts as a supervisor and intervenes only during the beginning of the data transfers, during interrupt request servicing, and during error handling.

#### Command Mode

When the controller is operating in command mode, it requests data transfers by activating the 'request out' line going to the tape unit controls. The controller loads the data to be transferred to the tape unit controls directly into the attachment data register. If data is to be transferred from the tape unit controls to the attachment, the data must be loaded into the cycle-steal data register (after being loaded into the attachment data register) before it can be transferred to the controller. When data is being transferred between the processor I/O channel and attachment controller, the data passes only through the cycle-steal data register.

#### Data Mode

When the controller is operating in data mode, it sets or verifies the condition of the status latches that apply to the high-speed cycle-steal data bus. The tape unit controls initiate data transfers by activating 'request in'; then, the data is transferred between the processor I/O channel and the tape unit.

#### Data Transfer Sequence

A typical data transfer consists of executing a Prepare command, followed by executing a Start command. Executing the Start command includes fetching a DCB, loading the attachment registers, and cycle stealing the data.

The following paragraphs further describe this sequence; the diagrams of the attachment feature card are for instructional purposes only. The keys in the text refer to keys in the diagrams.

#### Executing the Prepare Command

The first word of the IDCB is placed in the command register 16 and the device address compare register 10. If the device address compares with the attachment's address jumpers, the controller 1 analyzes and executes the command that is in the command register 16.

If the command initiates a DPC type of operation, the immediate data field (second word of the IDCB) is used for data. If the command initiates a cycle-steal type operation, the immediate data field is the address of the DCB.

When a Prepare command is issued to the attachment, the prepare level register 18 is loaded with IDCB immediate data field bits 11 through 14. The tape unit's address is also set into the I-bit flip-flops 19 which set a tape unit request trigger 20 that corresponds to the tape unit address. This operation designates the tape units that are permitted to interrupt and on which level the units can interrupt the processing operations.

#### Fetching the DCB

When a Start command is issued to the attachment, the DCB address register 23 is loaded with the IDCB's immediate data field. This is the address in processor storage of the first word of the DCB. The controller 1 reads the DCB address register 23 and sets the address counter 11, the byte counter 12 and the condition code/cycle-steal address key register 2. The controller then sets the cycle-steal input mode latch 13; the cycle-steal request latch 21 begins to cycle-steal eight DCB words to the controller storage 1 using the cycle-steal data register 26.

#### Loading the Registers

When the DCB fetch is complete, the controller 1 loads the address counter 11, the cycle-steal address register 17, the byte counter 12, and the condition code/cycle-steal address key register 2. The cycle-steal input mode latch 13 is set during an input operation and reset during an output operation. The controller 1 then gives control of the cycle-steal data handling to the attachment's data-bypass circuits. This operation is initiated by setting the auto mode latch 34.

#### Cycle Stealing the Data

Cycle-stealing is placed under control of the following automatic cycle-steal control triggers and latches:

- Load data registers trigger 25
- Cycle-steal data register full trigger 24
- Attachment data register full trigger 22
- Cycle-steal request latch 21

The automatic circuits control the address counter 11, the byte counter 12, and the data register 28.

During an output operation, the cycle-steal data register 26 is gated to the attachment data register 28 using the cycle-steal data bus 27. The ANDing of 'write' and the load data register trigger 26 signals provides the gate. The attachment data register full trigger 22 sets the load data register trigger 25.

At the completion of an automatic cycle-steal data transfer operation (byte count equals 0), the controller 1 resumes control by resetting the auto mode latch 3. At this time, it also reports the condition code, handles interrupt requests, and if chaining is necessary, fetches additional DCBs.

The signal-line sequencing between the attachment and the tape unit controls is controlled by the controller 1. The input and output lines to the tag register 8 define the type of data transfer operation in progress to the tape unit controls. The request out trigger 7, the 'request in' line 15, the 'acknowledge request out' line 6, and the 'acknowledge request in' line 4 define the direction of data transfer between the attachment and the tape unit controls. The 'strobe in' 14 and 'strobe out' 5 signal lines strobe the data being transferred into the attachment or the tape unit controls, respectively. The attachment 'data bus' 29 is a bidirectional bus that functions as a data path between the attachment and the tape unit controls. The interrupt register 9 is a four-bit register (one bit for each unit) that allows interrut requests to be posted during automatic cycle-steal operation.

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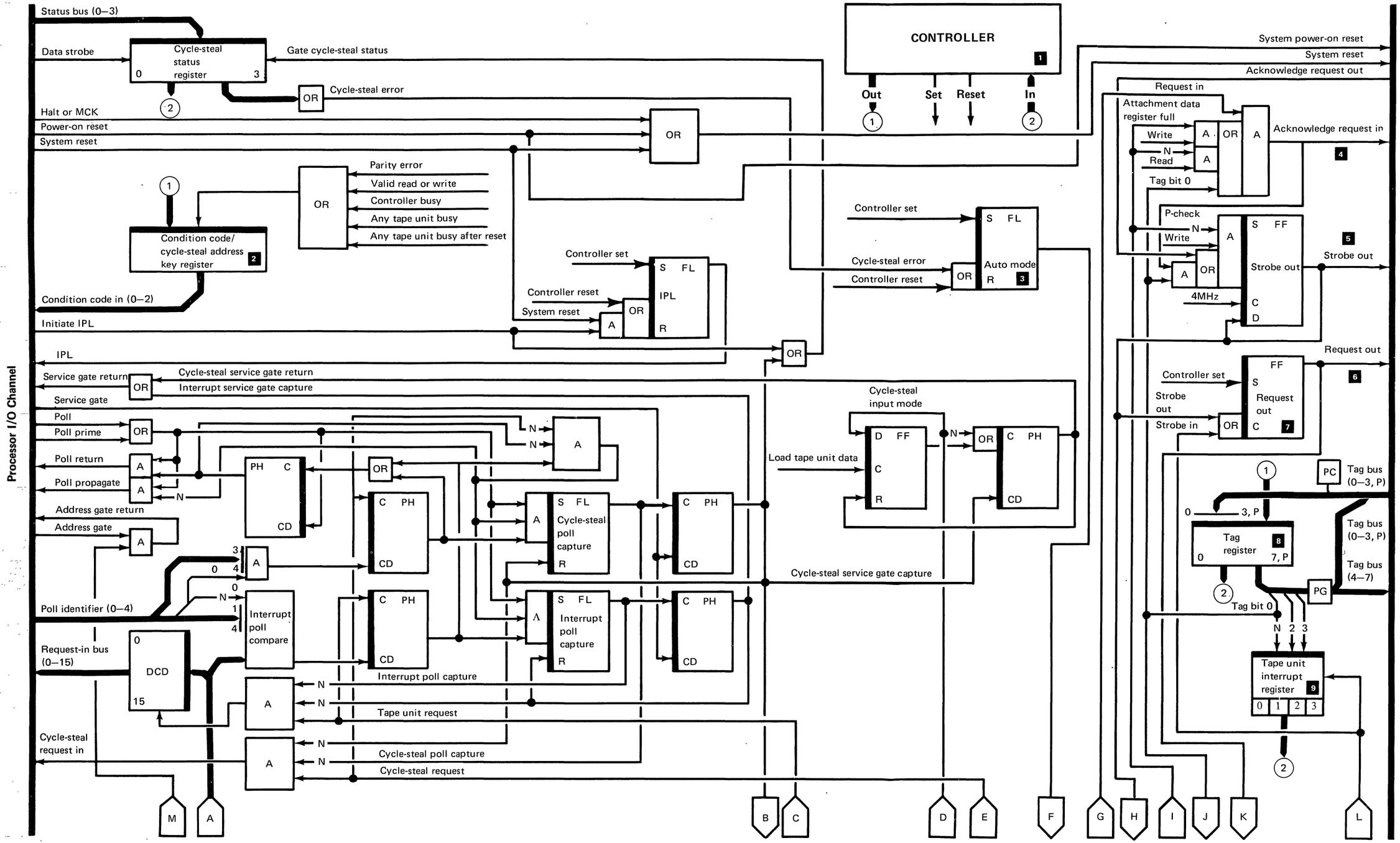
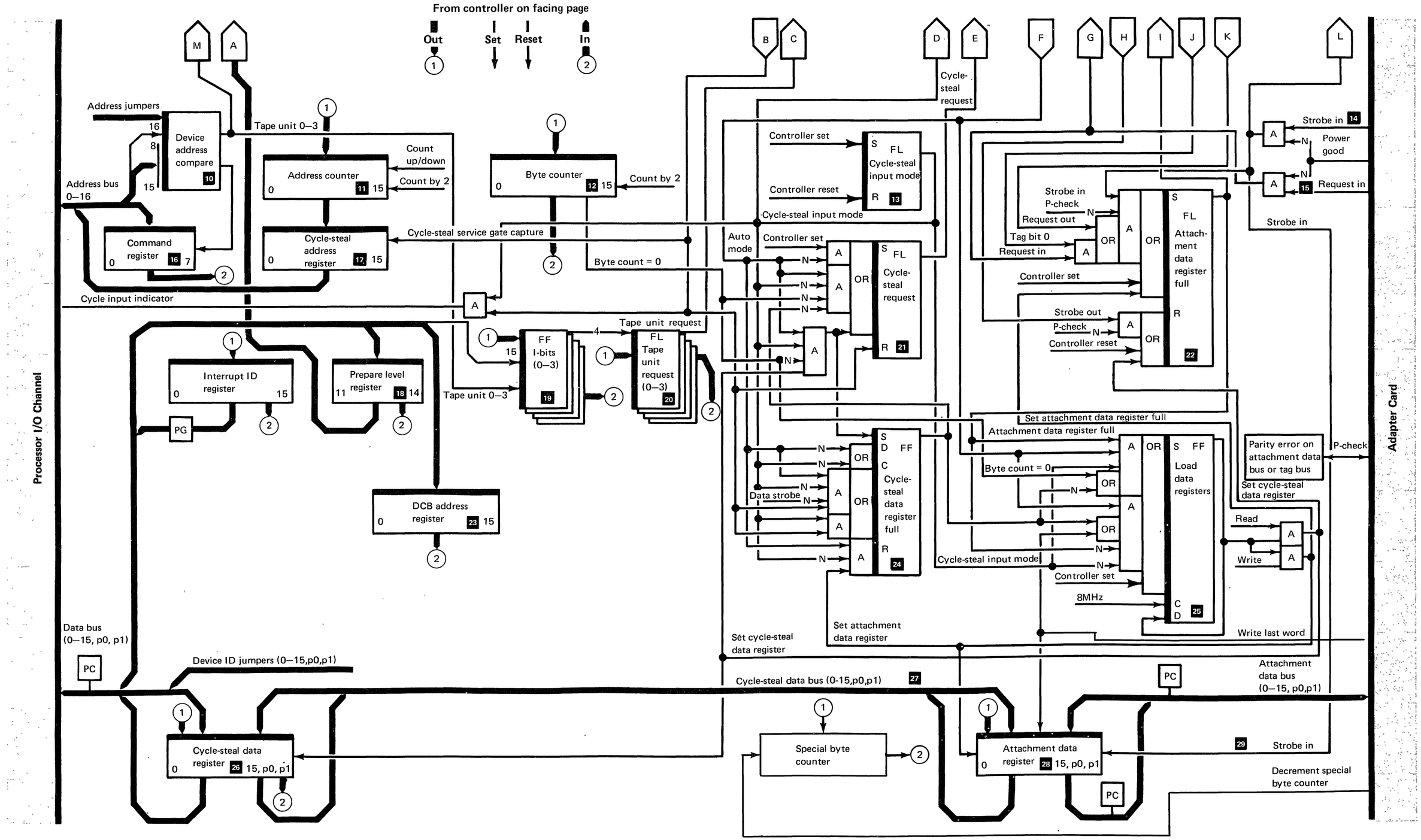

Processor I/O Channel
Tape Adapter Card
CONTROLLER
1
Out
Set
Reset
In
Status bus (0–3)
Data strobe
Cycle-steal status register
0
3
Gate cycle-steal status
Cycle-steal error
OR
Halt or MCK
Power-on reset
System reset
Parity error
Valid read or write
Controller busy
Any tape unit busy
Any tape unit busy after reset
Condition code/ cycle-steal address key register
2
Condition code in (0–2)
Initiate IPL
IPL
Controller set
Controller reset
System reset
S FL
IPL
R
A
Cycle-steal error
Auto mode
3
Service gate return
Cycle-steal service gate return
Interrupt service gate capture
Service gate
Poll
Poll prime
Poll return
Poll propagate
Address gate return
Address gate
PH C
CD
C PH
S FL
Cycle-steal poll capture
Cycle-steal input mode
D FF
Load tape unit data
Cycle-steal service gate capture
Poll identifier (0–4)
Interrupt poll compare
Interrupt poll capture
Request-in bus (0–15)
DCD
Tape unit request
Cycle-steal request in
Cycle-steal poll capture
Cycle-steal request
System power-on reset
System reset
Acknowledge request out
Request in
Attachment data register full
Write
Read
Tag bit 0
Acknowledge request in
4
P-check
Strobe out
5
4MHz
FF
Request out
6
Strobe in
7
PC
Tag bus (0–3, P)
Tag register
8
7, P
Tag bus (4–7)
PG
Tag bit 0
Tape unit interrupt register
9
M
A
B
C
D
E
F
G
H
I
J
K
L


From controller on facing page
Out
Set
Reset
In
Processor I/O Channel
Adapter Card
Address jumpers
Device address compare 10
Address bus 0–16
Tape unit 0–3
Address counter 11
Count up/down
Count by 2
Byte counter 12
Command register 16
Cycle-steal address register 17
Cycle-steal service gate capture
Byte count = 0
Cycle input indicator
Interrupt ID register
Prepare level register 18
PG
DCB address register 23
FF I-bits (0–3) 19
FL Tape unit request (0–3) 20
Tape unit request
Cycle-steal request
Controller set
Controller reset
FL Cycle-steal input mode 13
Cycle-steal input mode
Auto mode
FL Cycle-steal request 21
Strobe in 14
Power good
Request in 15
Strobe in P-check
Request out
Tag bit 0
Request in
FL Attachment data register full 22
Strobe out
P-check
Controller reset
Set attachment data register full
Attachment data register full
Byte count = 0
FF Load data registers
Parity error on attachment data bus or tag bus
P-check
Set cycle-steal data register
Read
Write
Data strobe
FF Cycle-steal data register full 24
Cycle-steal input mode
8MHz
FF 25
Set attachment data register
Set cycle-steal data register
Write last word
Data bus (0–15, p0, p1)
Device ID jumpers (0–15,p0,p1)
Cycle-steal data bus (0-15,p0,p1) 27
Attachment data bus (0–15, p0,p1)
PC
Cycle-steal data register 26 15, p0, p1
Special byte counter
Attachment data register 28 15, p0, p1
29 Strobe in
Decrement special byte counter

### Adapter Card

The first word that is transferred from the attachment card defines the operation to be performed. The tag bus is loaded into decode register 1 and the data bus is loaded into the data register 11. The output of the data register is gated to the 1-of-4 switch 7, which divides the data into bytes. The output of the 1-of-4 switch is gated to the 64 byte buffer 8. The output of the buffer is placed on the bus 9 with 'strobec' 4, that is generated by the decode of register 1, which defines the operation to be performed by the control board.

During an output operation each word of data is placed into the adpater by activating 'request in' 6. Each byte of data is transferred to the control board by the activation of 'data flag' 3 by the control board. With the last word that is transferred from the attachment the 'write last word' line 5 is activated. With the last byte of data that is transferred from the buffer 8 the 'halt data TRF' line 2 is activated to end the operation. During an input operation the control board activates 'data flag' 3 to load the buffer 8. The AND gate at 12 loads data register 11 one byte at a time; the AND gate at 10 gates the accumulated 18 bits from the data register to the data bus for transfer to the attachment card. 'Dec SPCL byte ctr' 13 is pulsed for each byte of data that is transferred in either direction. In order for the attachment card to give an ending sequence to the Series/1 processor, it checks the status of 'data busy' and 'controller busy.'

Attachment card

Tape unit address bit 0

Tag unit address bit 1

Tag bit 2

Tag bit 1

A FF

0

1

Tag 0

1

Adapter operation decode

0–3 Parity adapter tag bus bits

4–7 Adapter tag bus bits

Set attachment interrupt

Read/Write

Status WD1

Status WD2

Set diag status

Set controller interface wrap

CMD tag

Reset

FL

Controller wrap diagnostic mode

Data busy

NRZI mode

High density

Data busy end

Last byte out FIFO

FF

OR

Data busy

Halt data transfer

CRC tag in

Data flag

Tag diagnostic bus

Read/write

Diagnostic data flow register full and synthetic data flag

Tag diagnostic mode

Strobec

Write last word

Last byte into FIFO

Request in

Request out

Ack request in

Strobe out

Request in

Ack request out

Strobe in

Interface control

FIFO full

CTL DBO read

Read/write acknowledge

Test read mode

Read thres-hold low

Load data flow register byte 1

Load data flow register byte 0

Load status to data flow register

Gate data to bus

Mode latches

High density

Select - A

Select - B

CTRL interface diagnostic wrap latch

Strobec ungated

Read/write

FIFO shift in

Data flag

Write/read

Odd funnel pointer

Write/read

Parity checker

Buffer parity error

CTL DBI/CMND

Data bus

Tag diag bus

1 or 4 Switch

Buffer 64 x 12 bits (FIFO register)

CMD tag out

CRC tag out

FIFO input ready

Output Ready

Status WD1

Status WD2

Status word generation

Read clock activity sensor

Data busy

End of tape

File mark

Identity

Parity errors

Reserve

Controller busy

Reject CMD

NRZI/PE

Timing error

Ready

Rewinding

File protect

Corrected error

Load point

DFR empty

Write/read

Data flag

Shift in

Last byte tag out

Read/write

DFR empty

Write Ack

FIFO

FIFO Shift out

Set diagnostic status

Decode + drive

7 Diag bits

9 status bits

Switch Latch

9 diagnostic bits

7 status bits

Data register

CTL DBI/CMND (9 bits)

Decrement special byte counter

18 Status bytes

Parity generator

Data flow register (18 bits)

Data bus bits 10–15

Control board

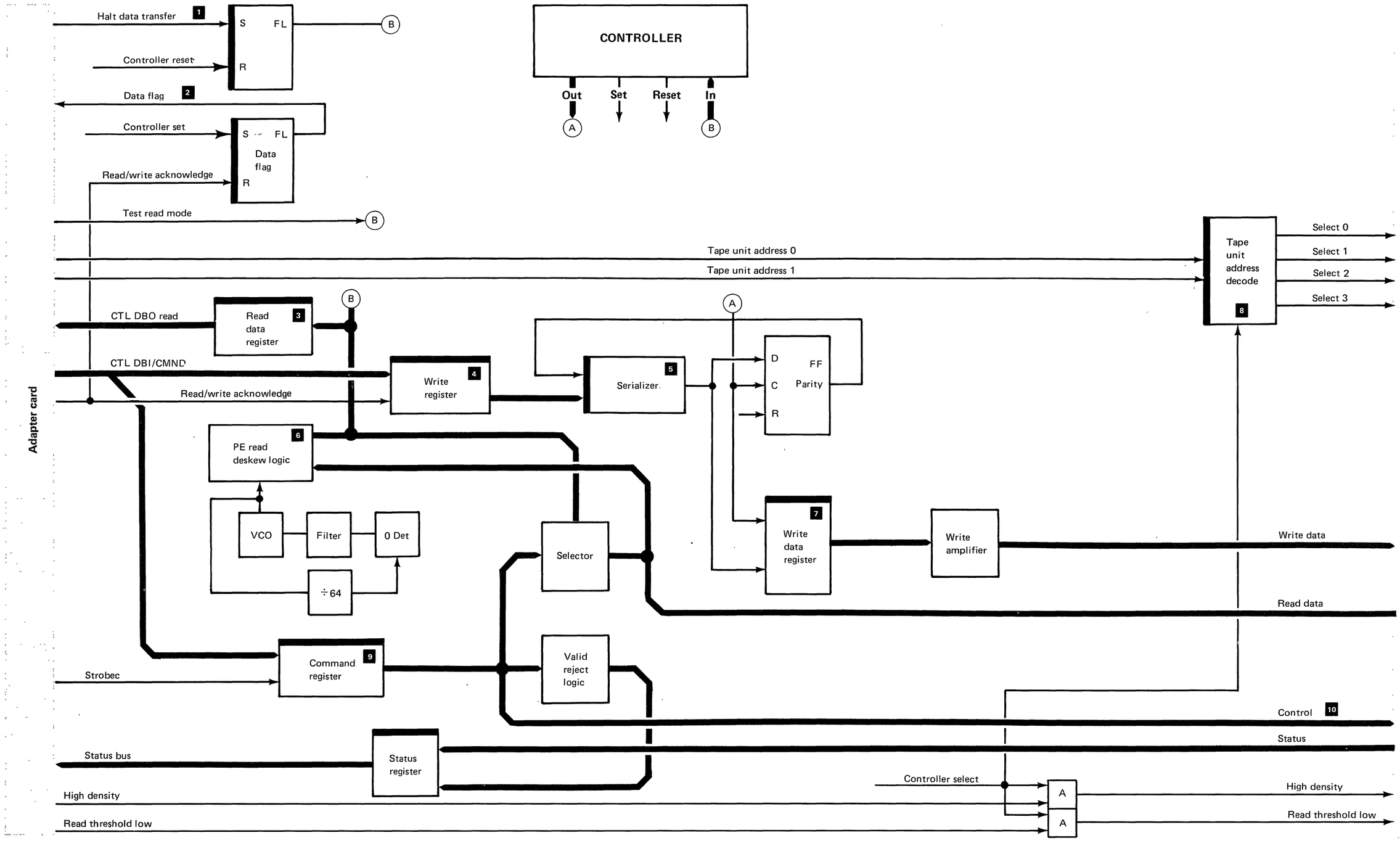
## Control Board

The command register 9 is loaded by 'strobec' and one of the following CTL DBI/CMND bus bits.

| Bit | Operation |
|---|---|
| 0 | Offline |
| 1 | Rewind |
| 2 | Backspace |
| 3 | Forward space |
| 4 | Erase |
| 5 | Write tape mark |
| 6 | Read |
| 7 | Write |

When performing an output operation, such as a write, the operation is decoded 9 and the forward control line 10 becomes active to cause the selected tape unit 8 to accelerate. The control board activates 'data flag' 2 to request data from the adapter card. Data is placed into the write register 4 by 'read/write acknowledge' from the adapter card. The data is passed through the serializer 5 to generate parity for this data and placed into the write data register 7. After a specified amount of time has elapsed, which depends on the speed of the tape unit, the write data is gated to the tape unit. The activation of 'halt data transfer' 1 with the last byte of data causes the control board to end the operation by deactivating 'data flag' and the forward control line.

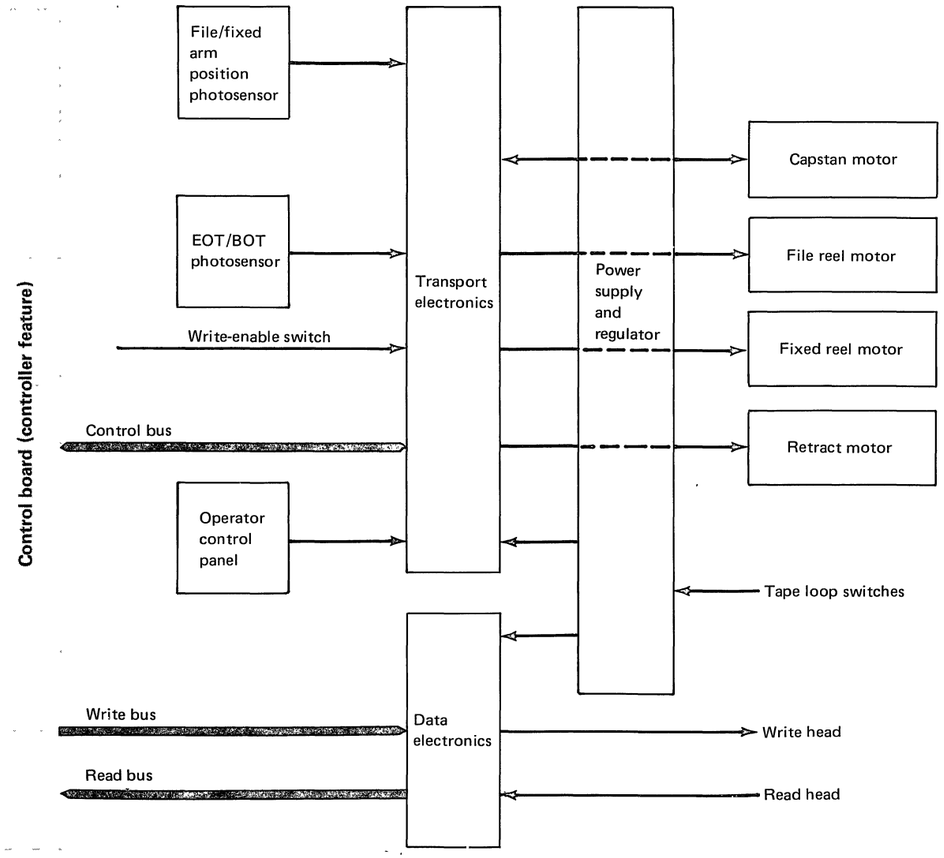
When performing an input operation, such as a read, the operation is decoded 9 and the forward control line 10 becomes active to cause the selected tape unit 8 to accelerate. If the tape is recorded in PE mode, the character is passed through the PE read deskew logic 6 and loaded into read data register 3. If the tape character read is NRZI it is placed directly into the read data register. The tape character is then placed on the CTL DBO read bus and the control board activates 'data flag' 2.


Adapter card
Halt data transfer
1
S
FL
R
B
Controller reset
Data flag
2
Controller set
S
FL
Data flag
R
Read/write acknowledge
Test read mode
B
CONTROLLER
Out
Set
Reset
In
A
B
Tape unit address 0
Tape unit address 1
Tape unit address decode
8
Select 0
Select 1
Select 2
Select 3
CTL DBO read
Read data register
3
B
CTL DBI/CMND
Read/write acknowledge
Write register
4
A
Serializer
5
D
C
R
FF
Parity
PE read deskew logic
6
VCO
Filter
0 Det
÷64
Selector
7
Write data register
Write amplifier
Write data
Read data
Command register
9
Strobec
Valid reject logic
Control
10
Status
Status bus
Status register
Controller select
A
A
High density
Read threshold low
High density
Read threshold low
Tape unit

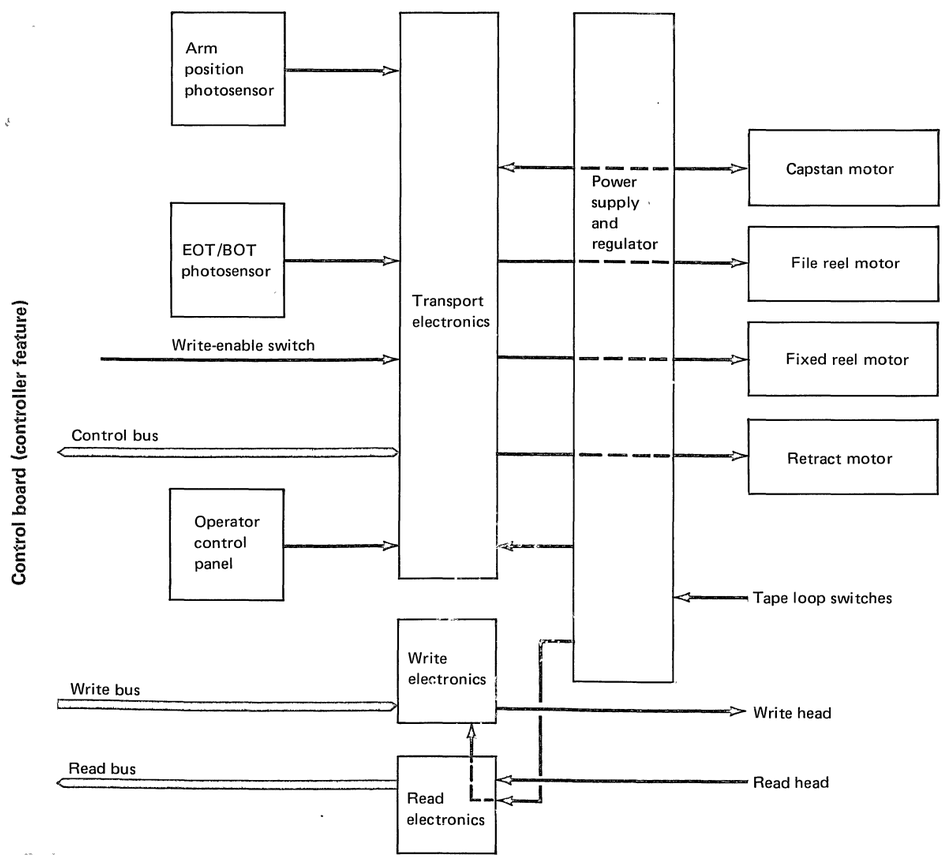
## Tape Unit

There are electronics boards in each tape unit. The electronics boards:

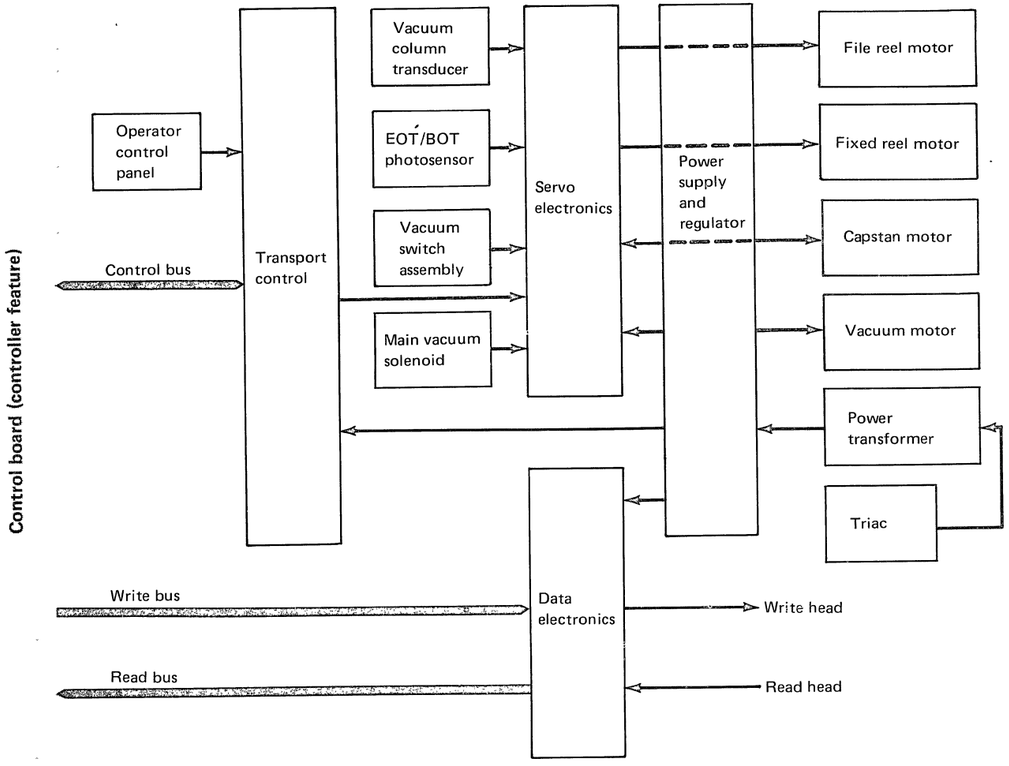
- Receive control information from the control board
- Send status information to the control board
- Send and receive data
- Control the tape position and motion



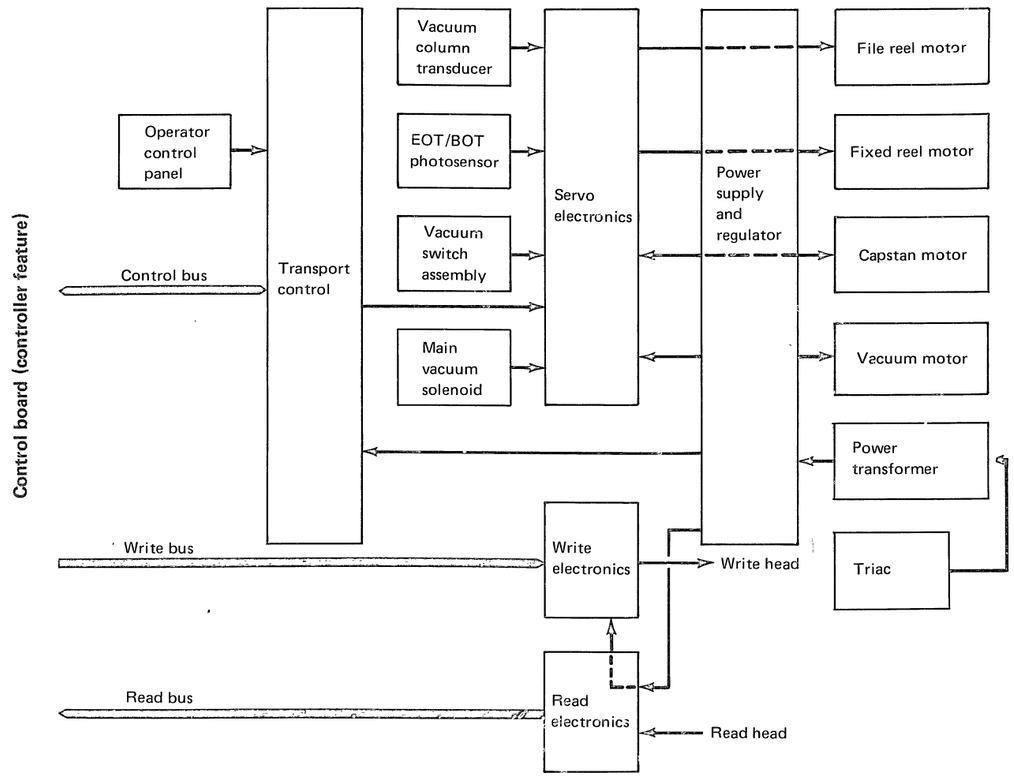

Tape unit circuit functions, models 4N, 4P




Tape unit circuit functions, model 4D




**Tape unit circuit functions, Models 7N, 7P**




**Tape unit circuit functions model 7D**

**Load Sequence (Model 4)**

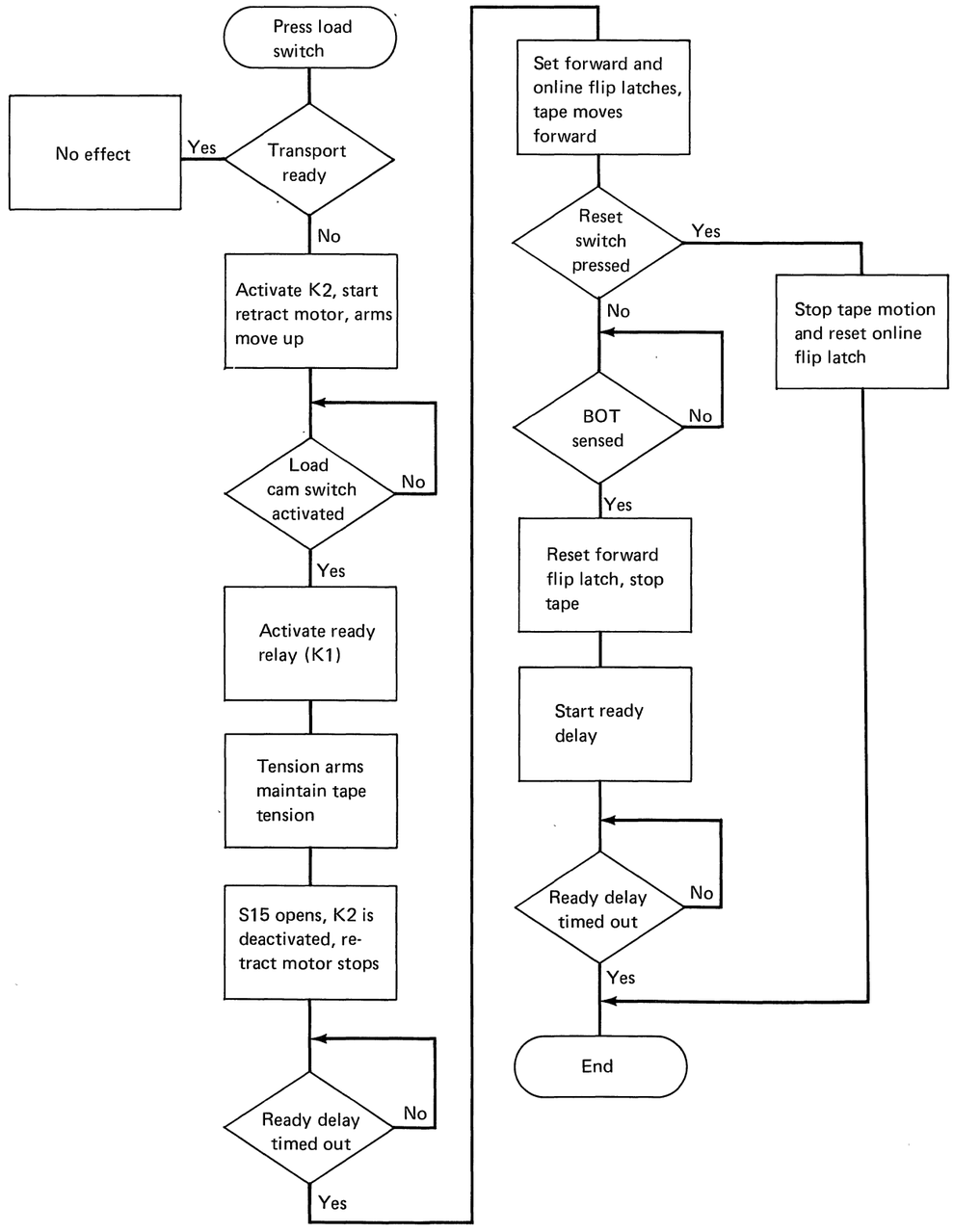
When power is applied to the tape unit, it activates the arm retract motor and returns the tension arms to the load position. With the arms in the load position, the ready relay (K1) is de-energized, and all three servo motors are shorted to ground. Interlock switches S11 and S13 are also open preventing latching of the ready relay. When the load switch is pressed, with tape properly threaded, the load sequence begins.

The retract motor is energized by activating the retract motor relay K2 through the normally open contacts of S16. The load cam begins to turn closing S15 normally open contacts which holds K2 energized when the load switch is released. The retract motor motion releases the tension arms from their retract position, and the series string of interlock switches (S10, S11, S12, S13) are in their normally closed positions. As the retract motor continues to turn, the load cam detent is sensed by the load cam switch S14, and a momentary ground is transmitted to ready-relay This energizes the ready relay and provides power to the servo motors, which then maintain tension on the tension arms. The retract motor continues to turn 180° removing mechanical linkage from the tension arms now under servo control. The motor stops when S15 opens, deenergizing K2, which removes ac power to the motor. The series string of interlock switches provide an unbroken circuit to ground for the ready relay holding the ready relay energized. If any one of the switches S10 through S13 is opened, the ready relay is de-energized. When the ready relay is energized, it sends a ground signal to the ready delay circuitry which, after timing out, gives an internal ready signal. (This signal does not reach the tape control board.) If the tape is not already at load point, a set forward and online operation is generated that sets the forward and online flip-flops. The tape moves forward until it reaches the load point marker. (Ready status to the tape control board is still inhibited.)

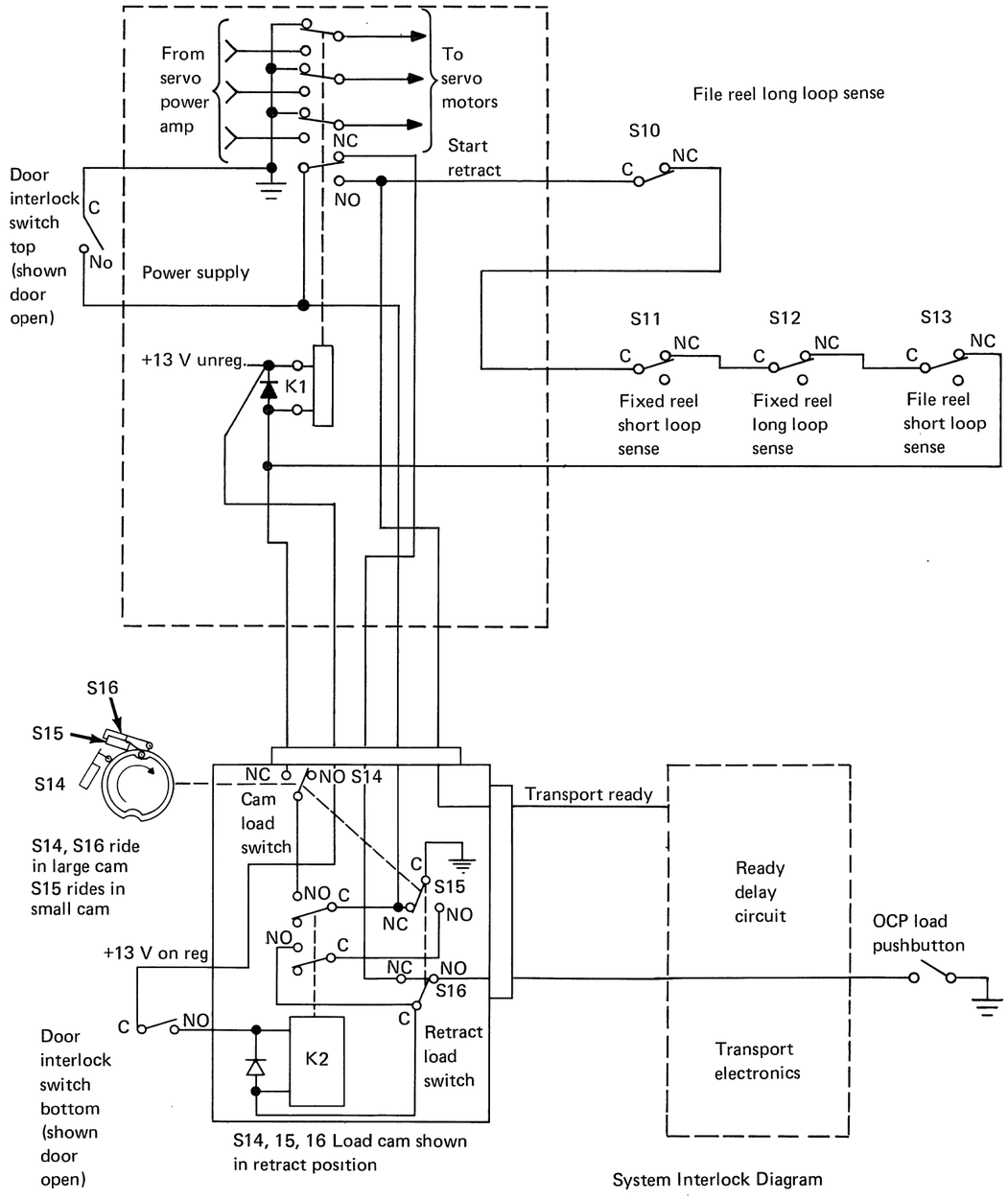
If the tape is already at load point (or when it reaches load point):

1. Tape motion stops (or is not initiated if at load point).
2. The Load and On Line indicators are turned on.

*Note:* If the tape unit door is open, two door interlock switches inhibit all retract arm and motor motion.




**Model 4 load sequence**

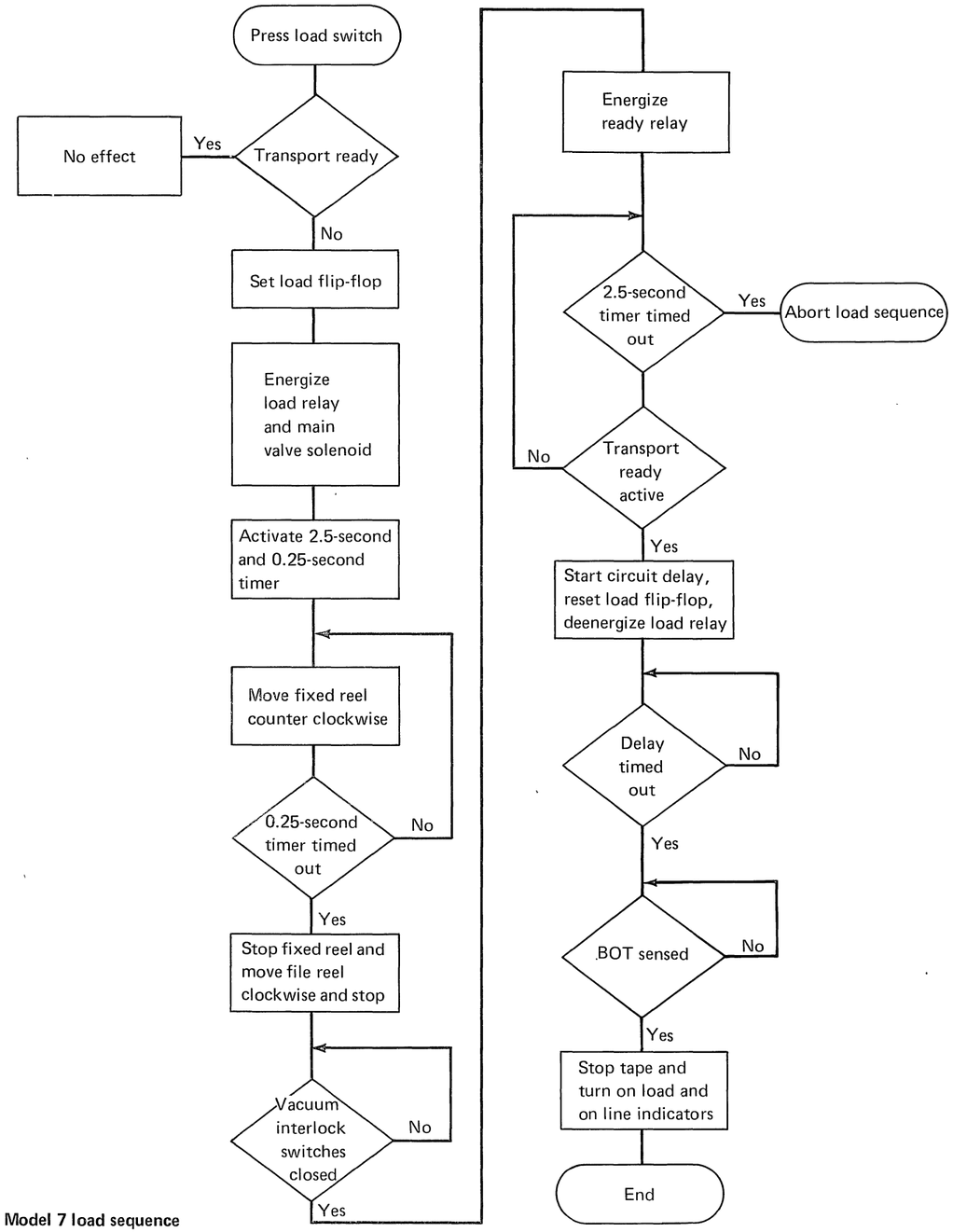

From servo power amp
To servo motors
NC
Start retract
NO
Door interlock switch top (shown door open)
C
No
Power supply
+13 V unreg.
K1
File reel long loop sense
S10
C
NC
S11
S12
S13
Fixed reel short loop sense
Fixed reel long loop sense
File reel short loop sense
S16
S15
S14
S14, S16 ride in large cam
S15 rides in small cam
NC
NO S14
Cam load switch
Transport ready
Ready delay circuit
OCP load pushbutton
+13 V on reg
S15
S16
Retract load switch
Door interlock switch bottom (shown door open)
K2
Transport electronics
S14, 15, 16 Load cam shown in retract position
System Interlock Diagram

**Load Sequence (Model 7)**

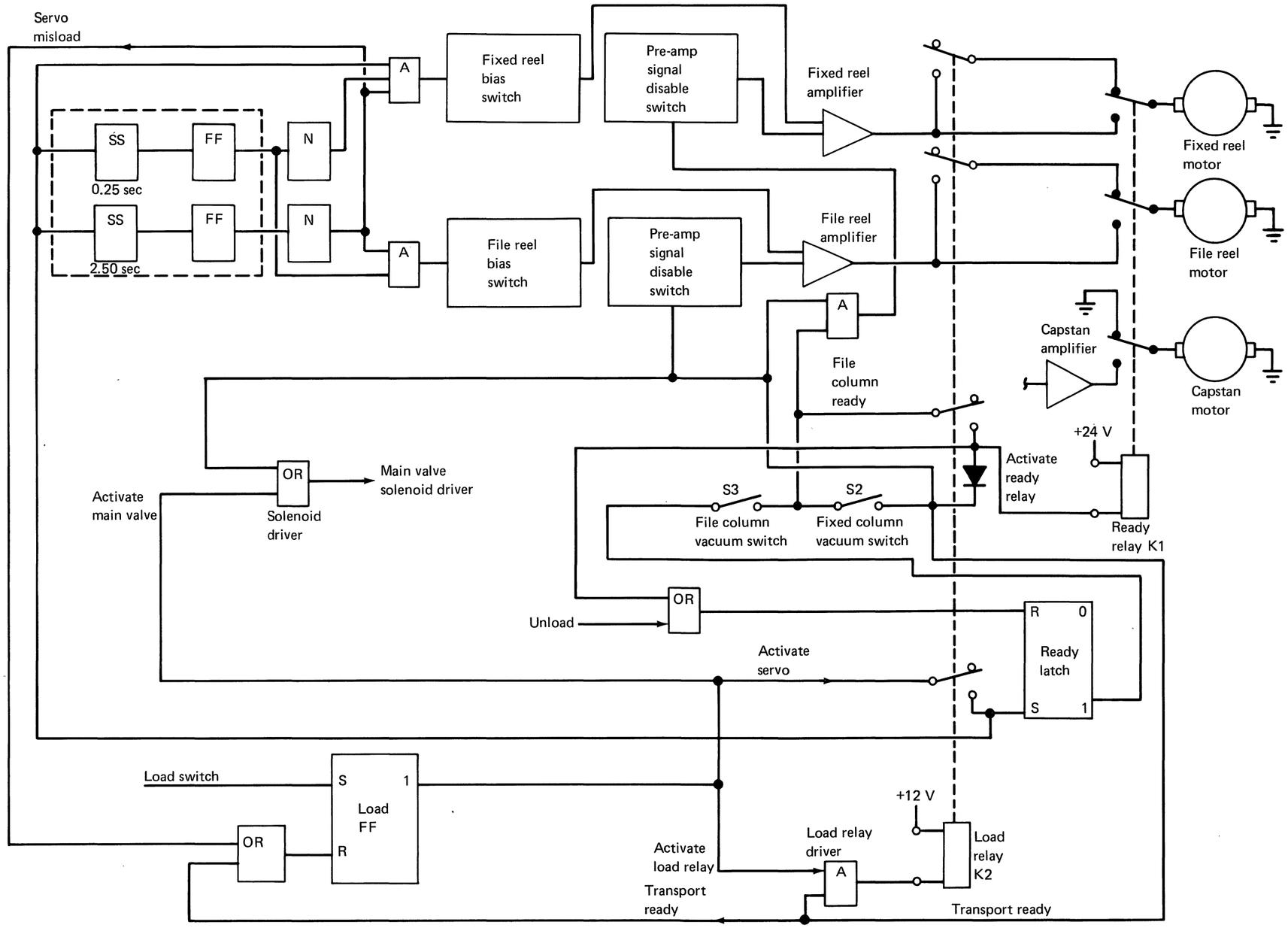
Pressing the Load switch, with tape properly threaded, begins the load sequence. Voltage detection circuits sense for proper regulated voltages and +24 volts are present before the load sequence can continue. The load flip-flop is set which will energize the load relay (K2 on servo electronics board) and the main valve solenoid. The main valve solenoid energized applies vacuum to the vacuum columns. Also activated is a 2.5-second timer and a 0.25-second timer through a set of K2 contacts by 'activate servo'. The 0.25-second timer causes the fixed reel to move counter clockwise to allow the vacuum to form a tape loop in the fixed reel vacuum column. The 0.25-second timer timing out will stop the fixed reel and move the file reel clockwise for approximately 0.5 second to allow the vacuum to form a tape loop in the file reel vacuum column.

The vacuum switches transferred (enough tape in the vacuum columns) energizes the ready relay (K1 in power supply). If the 2.5-second timer times out before transport ready becomes active, the load sequence is aborted and the load circuitry is reset. When transport ready is active, it will start a circuit delay, reset the load flip-flop, and de-energize the load relay. After the delay the tape moves forward until it reaches the load point marker; with the load point marker (BOT) sensed:

1. Stop tape motion
2. Turn on Load and On Line indicators



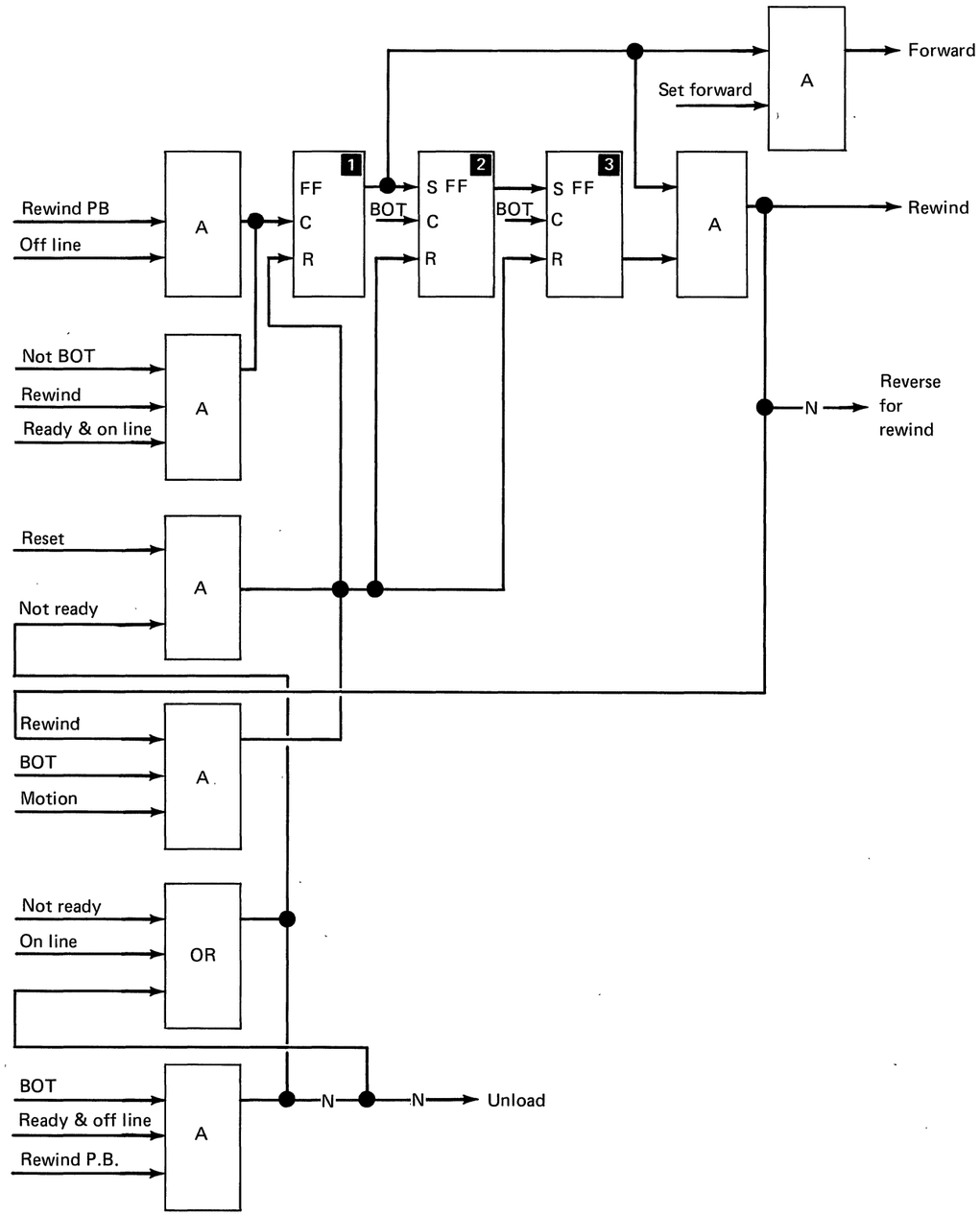

**Model 7 load sequence**


Servo misload
A
Fixed reel bias switch
Pre-amp signal disable switch
Fixed reel amplifier
SS
FF
N
0.25 sec
SS
FF
N
2.50 sec
A
File reel bias switch
Pre-amp signal disable switch
File reel amplifier
Fixed reel motor
File reel motor
A
Capstan amplifier
Capstan motor
File column ready
+24 V
Activate ready relay
OR
Main valve solenoid driver
Activate main valve
Solenoid driver
S3
S2
File column vacuum switch
Fixed column vacuum switch
Ready relay K1
OR
Unload
R 0
Ready latch
S 1
Activate servo
Load switch
S 1
Load FF
R
OR
+12 V
Load relay driver
A
Load relay K2
Activate load relay
Transport ready
Transport ready

**Rewind/Unload**

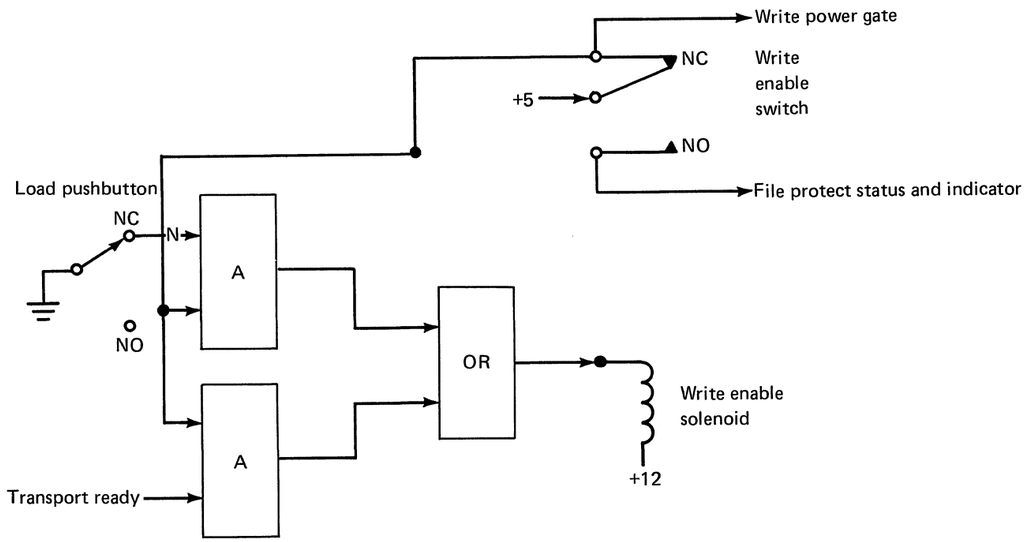
The rewind sequence is initiated by either a programmed rewind command or by pressing the Rewind switch when the tape unit is in the offline mode. Decoding the flip-flops at 1 and 3 gives a rewind signal to the capstan rewind ramp generator. When the capstan servo receives the rewind signal, the tape drive accelerates to rewind speed and moves tape until either the load point marker is reached or the Reset switch is pressed. Unless the Reset Switch is pressed, the leading edge of the load point marker pulses the clock input of the flip-flop at 2, and the trailing edge pulses the clock input of the flip-flop at 3. With the flip-flop at 3 set, the rewind signal is no longer active, which generates the set forward signal and stops rewinding. When the flip-flop at 1 is set and 'set forward' is active, the tape moves forward until the load point marker is sensed, which resets the forward latch and the three flip-flops.

The unload sequence is initiated when the load point marker is sensed, the tape unit is offline, and the Rewind switch is pressed.



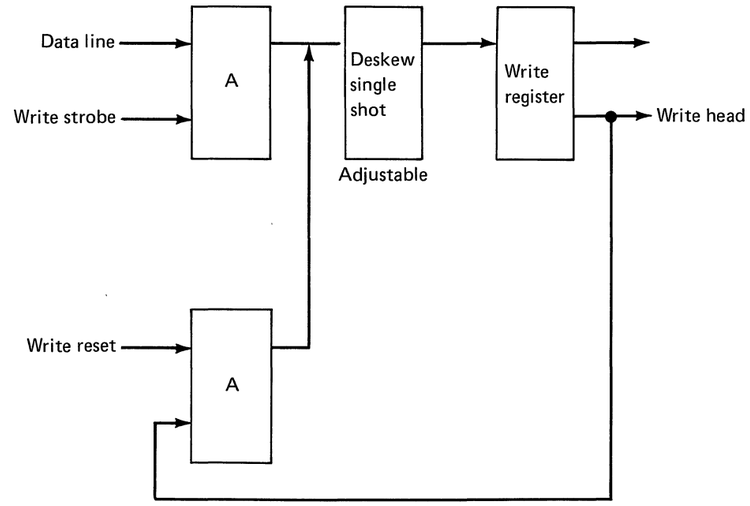
### File Protect Sensor

To write on a reel of tape, a write-enable ring must be installed on the back of the reel. The mechanism that senses the write-enable ring is designed so that it holds the sensing pin retracted to keep it from scraping the ring. When the Load Switch is pressed, the mechanism is released so it can sense whether there is a write-enable ring in place and to verify that the solenoid was not accidently energized. When the load cycle is complete, the tape unit 'ready' signal holds the solenoid energized. The absence of a write-enable ring on the file reel will, through the file protect circuitry, prevent writing on the tape. Also a status bit is set and the file protect indicator located on the operator control panel will be turned on.

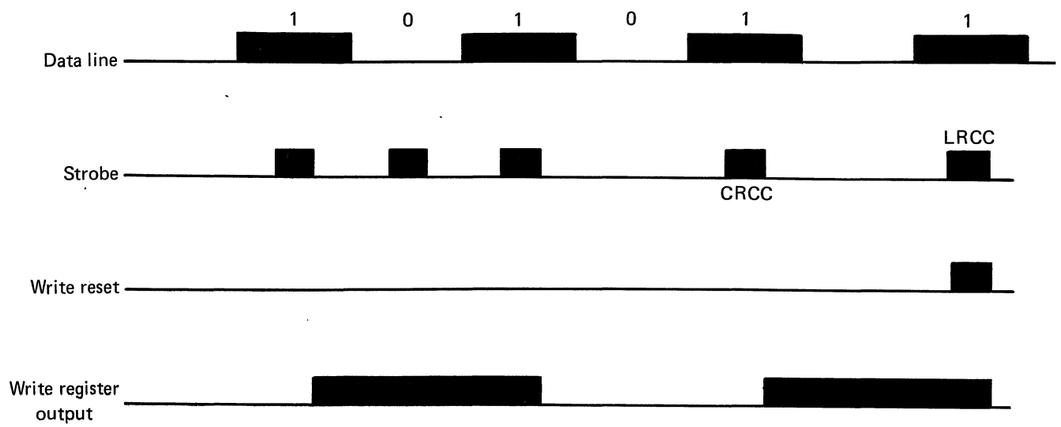



### Write Data (NRZI)

A pulse on 'write strobe' clocks information from the data lines into the write circuitry. The write deskew single-shot is adjustable to correct for the static skew characteristics of the write head to ensure that data is written perpendicular to the edge of the tape. This is done to ensure maximum reliability and interchangeability of tapes.



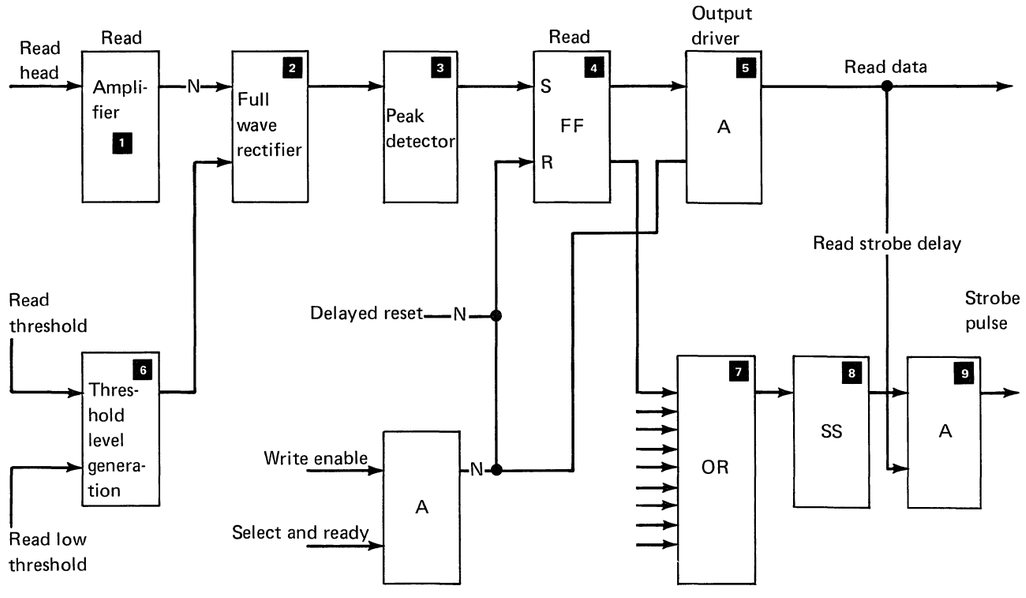

1 of 9 track write circuits



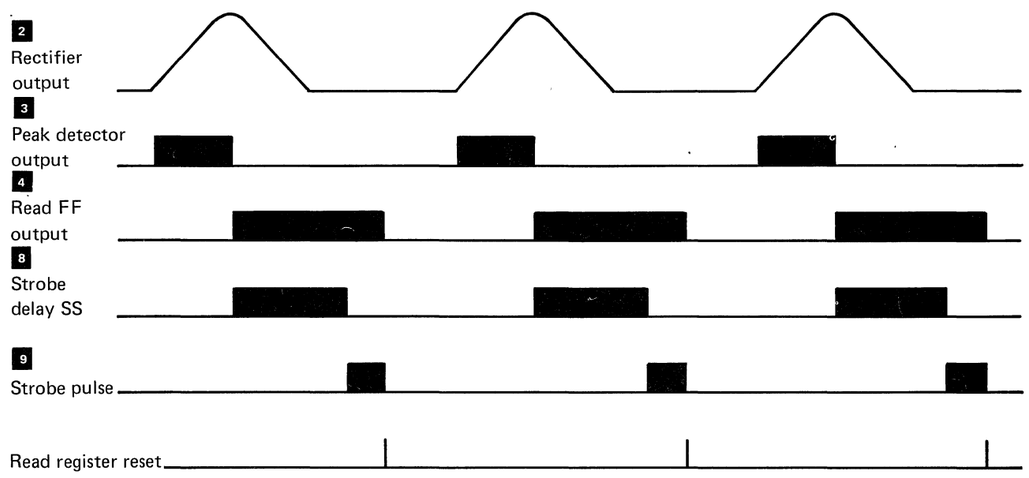
**Read Data (NRZI)**

The read head generates a low-level analog signal. The read amplifier 1 picks up this signal and amplifies it to a suitable level and then sends it to the full-wave rectifiers. A threshold level dc bias 6 is fed into the input of the full-wave rectifier 2 with the result that positive peaks above the threshold level are at the output of the circuit. This signal is then sent to the peak detector 3, which in turn, generates a digital pulse whose trailing edge corresponds to the peak of the analog signal and is used to load the read flip-flop 4. The contents of the read flip-flop 4 are sent to the output drivers 5.

A strobe pulse is generated and sent to the control board that indicates read data is available on the data lines. This strobe pulse is generated by taking the nine read flip-flops and feeding them into a nine-way OR-gate at 7 whose output goes to a single-shot. The first bit sensed by the OR-gate is used to trigger the single-shot at 8. The trailing edge of the single-shot pulse generates the strobe pulse signal 9.

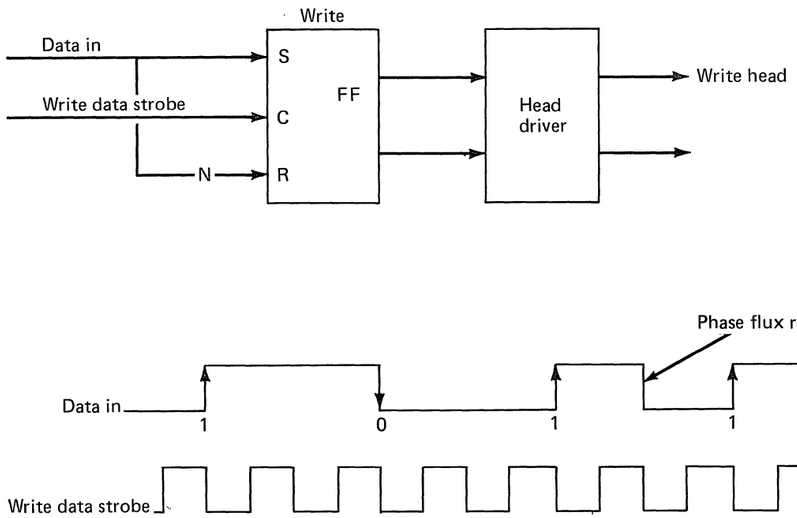



1 of 9 Read circuits



### Write Data (PE)

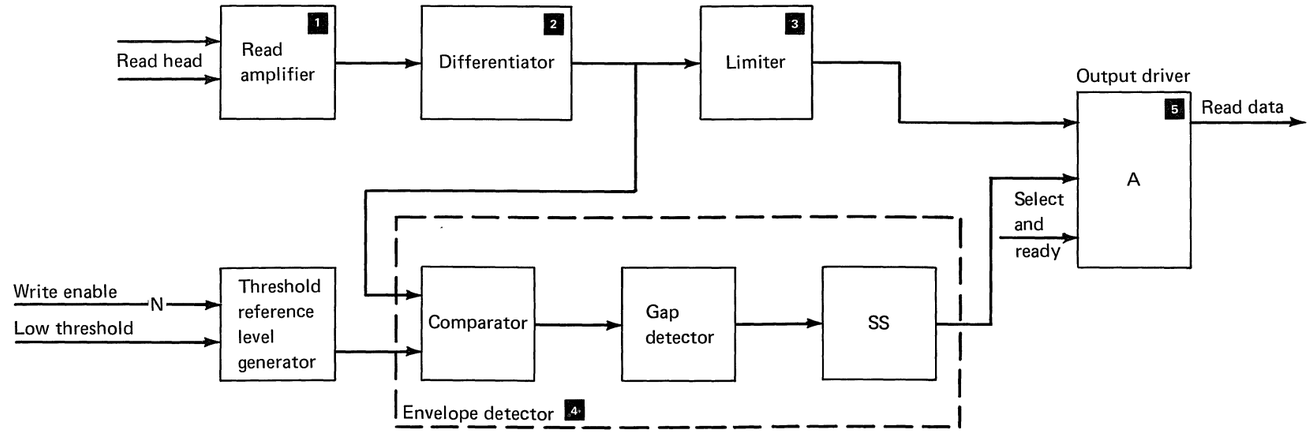
The phase encoded write data is transferred to the write flip-flops at the trailing edge of the write data strobe. The contents of the write flip-flops are converted into write currents by the head drives. When the write data lines are low, the head currents are changed (unless already in the proper state) by the write data strobe pulse, and magnetizes the tape in the opposite direction of the IBG polarity. The write data strobe is generated by the control board and its frequency is twice the character transfer rate to write phase flux reversals on tape.




### Read Data (PE)

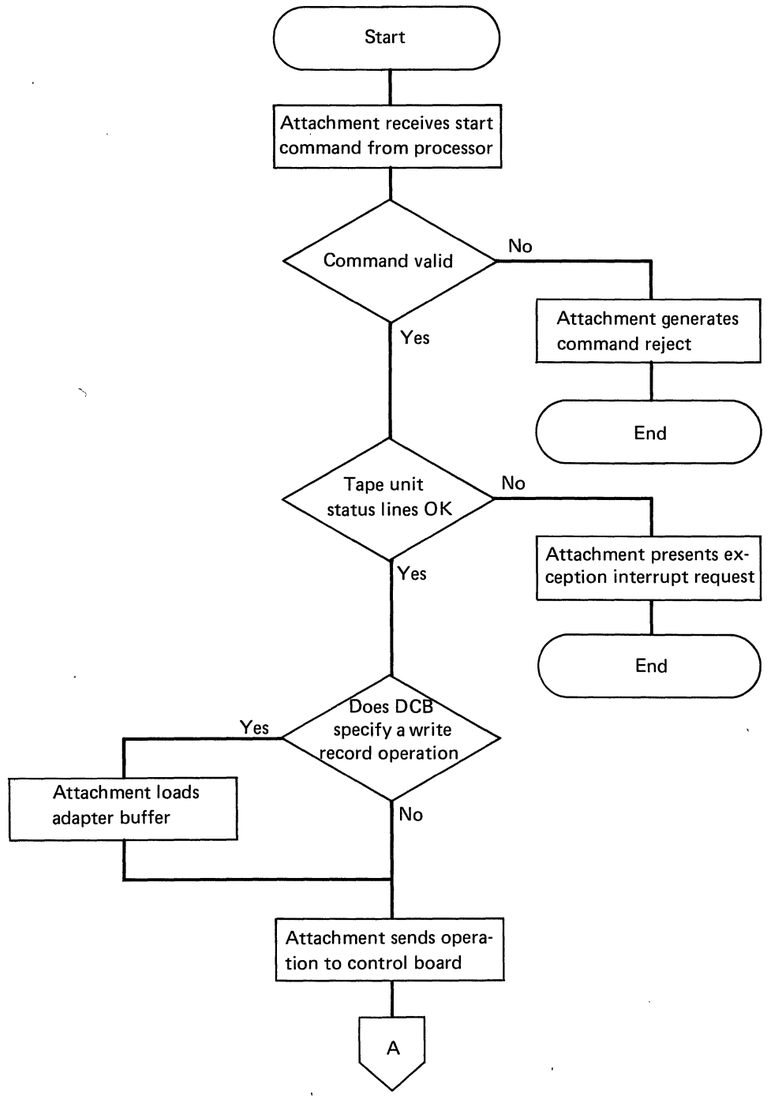
The read head generates an analog signal that is then amplified 1 to a suitable level. The signal is then passed through the differentiator 2 to equalize the amplitude and to convert the peaks to zero crossover points. Next, zero crossover detection is accomplished by amplification and limiting 3 of the signal. The digitized data is then sent to its output driver 5.

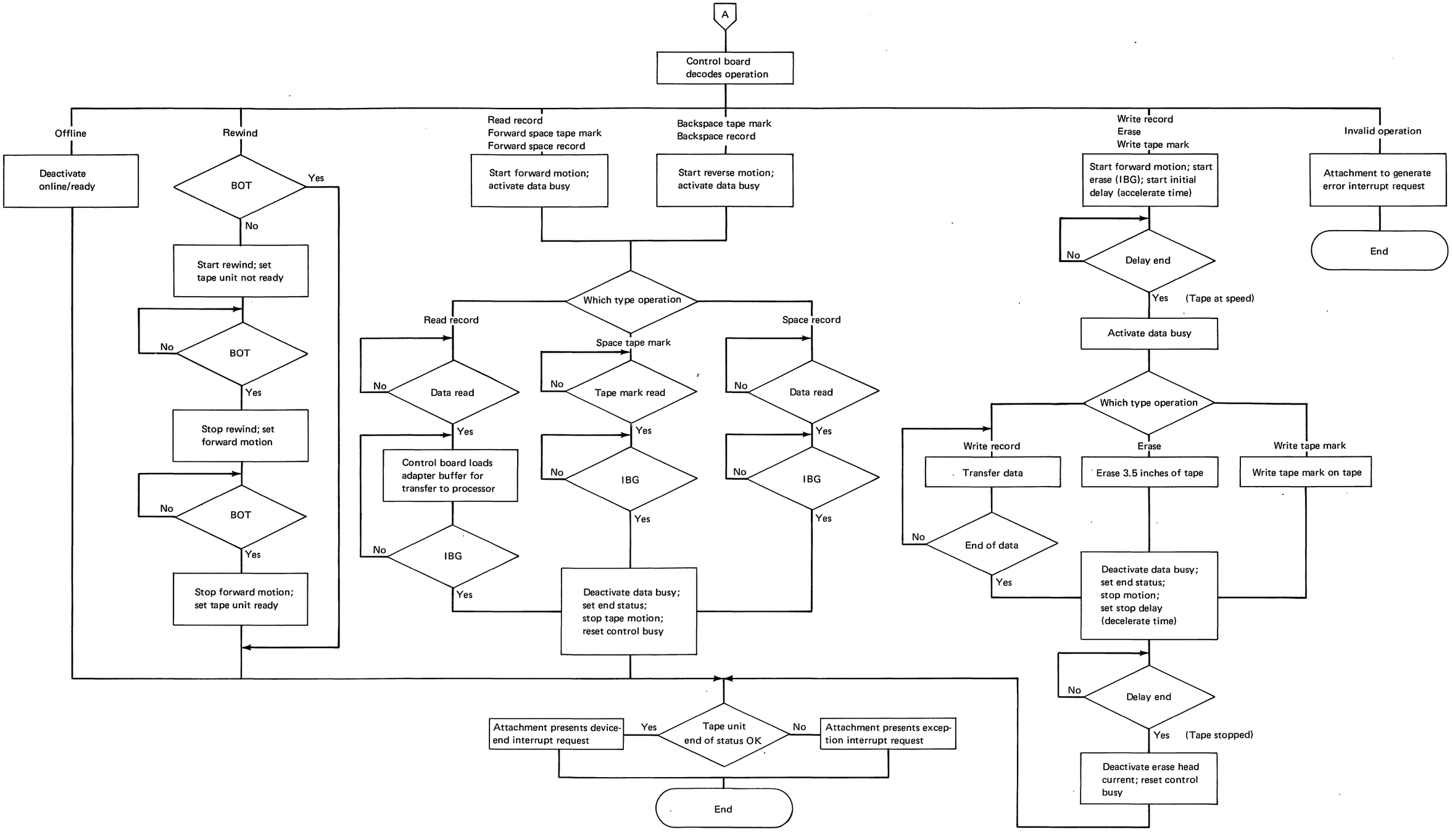
Envelope detection 4 is done in parallel with the limiting process. The purpose for this is to disable data flow to the control board as soon as data is no longer present and to maintain the data channels disabled while in the IBG.



### Tape Operation Flow Chart

The following flow chart shows the 4969 subsystem operation for normal tape operations. It shows the sequence of events from the time the attachment receives a Start command from the processor until the subsystem terminates the operation.




A
Control board decodes operation
Offline
Deactivate online/ready
Rewind
BOT
Yes
No
Start rewind; set tape unit not ready
No
BOT
Yes
Stop rewind; set forward motion
No
BOT
Yes
Stop forward motion; set tape unit ready
Read record
Forward space tape mark
Forward space record
Start forward motion; activate data busy
Backspace tape mark
Backspace record
Start reverse motion; activate data busy
Which type operation
Read record
No
Data read
Yes
Control board loads adapter buffer for transfer to processor
No
IBG
Yes
Space tape mark
No
Tape mark read
Yes
No
IBG
Yes
Space record
No
Data read
Yes
No
IBG
Yes
Deactivate data busy; set end status; stop tape motion; reset control busy
Write record
Erase
Write tape mark
Start forward motion; start erase (IBG); start initial delay (accelerate time)
No
Delay end
Yes (Tape at speed)
Activate data busy
Which type operation
Write record
Transfer data
No
End of data
Yes
Erase
Erase 3.5 inches of tape
Write tape mark
Write tape mark on tape
Deactivate data busy; set end status; stop motion; set stop delay (decelerate time)
No
Delay end
Yes (Tape stopped)
Deactivate erase head current; reset control busy
Invalid operation
Attachment to generate error interrupt request
End
Attachment presents device-end interrupt request
Yes
Tape unit end of status OK
No
Attachment presents exception interrupt request
End

# Chapter 4. Operations

This chapter describes how the processor transfers data to and from the 4969 tape subsystem. It includes descriptions of the Operate I/O instruction and its associated commands, status words, and condition codes. The processor initiates all 4969 tape subsystem operations by issuing an Operate I/O instruction, and then uses the processor I/O channel to transfer data to and from the 4969.

The Operate I/O instruction is a privileged instruction. Its effective address (the combination of the R2 and address fields) points to an immediate device control block (IDCB) in processor storage. The IDCB contains a command, a device address, and an immediate data field. The command defines the type of I/O operation. The device address identifies the device on which the operation is to be performed. Tape units within the subsystem are designated as physical units 0, 1, 2, and 3. The device address for the primary unit (physical unit 0) can be any even address from 2 through 254 within the following parameters:

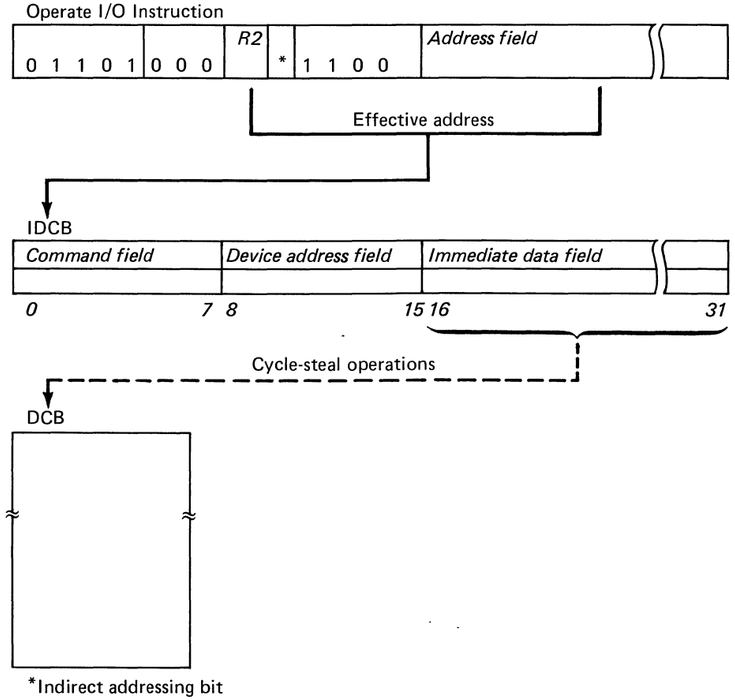
- If one or two units are installed (a primary unit or a primary unit and an optional unit), the device address of the primary unit must be divisible by 2.
- If three or four units are installed (a primary unit with either two or three optional units), the device address of the primary unit must be divisible by 4.

Optional unit device addresses are sequentially numbered in ascending order immediately following the primary unit's device address.

*Examples:*

Primary unit device address = 6
Optional unit device address = 7
or
Primary unit device address = C
Optional unit device address = D
Optional unit device address = E
Optional unit device address = F

The use of information in the immediate data field depends on the mode of operation. For direct program control (DPC) operations, the immediate data field contains a data word; for cycle-steal operations, this field points to a device control block (DCB) that contains additional information needed to perform the operation. The IDCB must be on a fullword boundary. Refer to an appropriate processor description manual listed in the preface under "Prerequisite Publications" for a more detailed description.

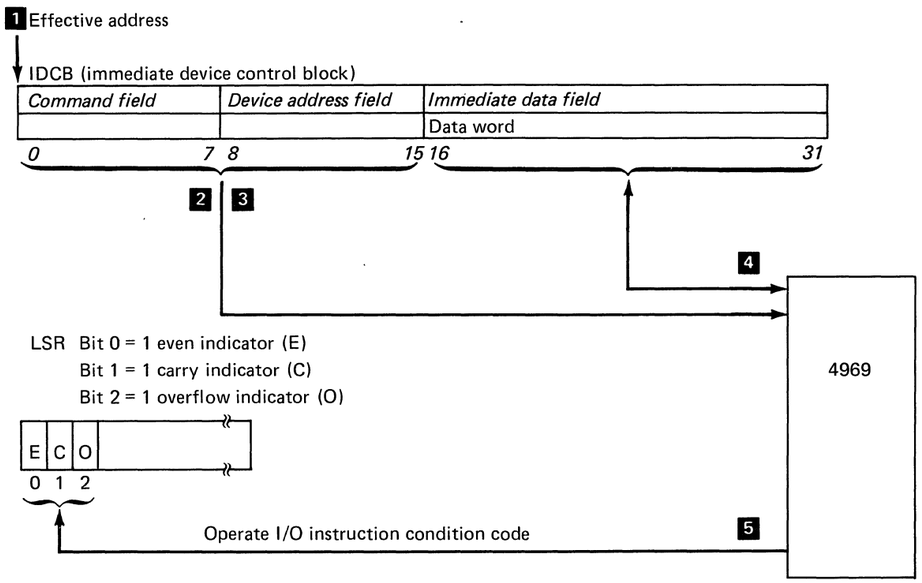


## Direct Program Control

A direct program control operation causes an immediate transfer of data or control information to or from the 4969.

An Operate I/O instruction must be executed for each data transfer. Each execution causes the following events (refer to Figure 2-2):

1. The Operate I/O instruction's effective address points the program to an IDCB in processor storage 1.
2. The I/O channel uses the IDCB's device address field 3 to select the 4969, and the command field 2 to determine the operation to perform.
3. The processor transfers the contents of the immediate data field to the 4969, or transfers information from the 4969 to the immediate data field, depending on the command being executed 4.
4. The 4969 sends a condition code to the level status register (LSR) in the processor 5. Condition codes are explained under "Condition Codes" later in this chapter.




### Read ID

IDCB (immediate device control block)

| Command field | Device address field |
|---|---|
| 0 0 1 0 0 0 0 0 | X X X X X X X X |
| 0 7 | 8 15 |
| 20 | 00–FF |

| Immediate data field |
|---|
| Returned ID word |
| 16 31 |

This command transfers the identification (ID) word for the 4969 to the immediate data field of the IDCB. After command execution, the immediate data field contains:

Read ID for 4969

| Immediate data field |
|---|
| 0 0 1 1 0 0 X X 1 0 0 0 0 1 1 0 |
| 16 22 23 31 |

- 01 indicates one or two tape units attached
- 10 indicates three or four tape units attached

In the following example, assume that one tape unit is attached and a Read ID command is issued to device address hex 48. The result of executing the Read ID command is hex 3186 in the immediate data field.

IDCB (immediate device control block)

| Command field | Device address field |
|---|---|
| 0 0 1 0 0 0 0 0 | 0 1 0 0 0 1 1 0 |
| 0 7 | 8 15 |
| 20 | 48 |

| Immediate data field |
|---|
| 0 0 1 1 0 0 0 1 1 0 0 0 0 0 1 1 0 |
| 16 23 31 |

This indicates that either one or two tape units are attached because bit 23 equals 1. To determine if a second tape unit is attached, a second Read ID command is issued to the device address plus 1, or, in this case, to device address hex 49. Because the second tape unit in this example is not attached, a condition code of 0 is posted.

In the next example, assume that four tape units are attached and a Read ID command is issued to device address hex 48. The result of executing the Read ID command is hex 3286 in the immediate data field.

IDCB (immediate device control block)

| Command field | Device address field |
|---|---|
| 0 0 1 0 0 0 0 0 | 0 1 0 0 1 0 0 0 |
| 0 7 | 8 15 |
| 20 | 48 |

| Immediate data field |
|---|
| 0 0 1 1 0 0 1 0 1 0 0 0 0 1 1 0 |
| 16 22 31 |

This indicates that there are either three or four tape units attached because bit 22 equals 1. To determine if the fourth tape unit is attached, a second Read ID command is issued to the device address plus 3, or, in this case, to device address hex 4B. Because the fourth tape unit in this example is attached, a condition code of 7 is posted.

### Prepare

IDCB (immediate device control block)

| Command field | Device address field |
|---|---|
| 0 1 1 0 0 0 0 0 | X X X X X X X X |
| 0 7 | 8 15 |
| 60 | 00–FF |

| Immediate data field | | |
|---|---|---|
| Zeros | Level | I |
| 16 26 27 | 30 31 | |

0 = interrupts disabled
1 = enable interrupts

*Note:* Refer to "Prerequisite Publications" in the Preface of this manual. Processor description manuals contain information about interrupt levels.

This command loads the interrupt level and I-bit into the 4969. The I-bit (IDCB bit 31) defines whether the 4969 tape unit can present I/O interrupt requests. If the I-bit equals 1, requests are presented on the level defined by the level field (bits 27–30); if the I-bit equals 0, the tape unit cannot present interrupt requests. All tape units attached to a given tape attachment will be assigned the same interrupt level, but a separate interrupt I-bit is provided for each tape unit.

### Device Reset

IDCB (immediate device control block)

| Command field | Device address field |
|---|---|
| 0 1 1 0 1 1 1 1 | X X X X X X X X |
| 0 7 | 8 15 |
| 6F | 00–FF |

| Immediate data field |
|---|
| Zeros |
| 16 31 |

This command resets any pending interrupt request or busy condition for the addressed 4969 tape unit. The prepare level and the residual address are not affected. The IDCB's immediate data field is not used.

An external reset signal is sent to the controller if the tape controller is using the addressed tape unit or if the controller is inactive. This reset signal places the controller in a quiescent state.

### Attachment General Diagnostic

IDCB (immediate device control block)

| Command field | Device address field |
|---|---|
| 0 1 0 0 0 0 0 1 | X X X X X X X X |
| 0 7 | 8 15 |
| 41 | 00–FF |

| Immediate data field |
|---|
| Zeros |
| 16 31 |

This command causes the attachment to test its data registers and control latches. Any detected failure causes an interrupt request and sets the equipment check bit (8) equal to 1 in cycle-steal status word 4.

### Attachment Storage Diagnostic

IDCB (immediate device control block)

| Command field | Device address field |
|---|---|
| 0 1 0 0 1 1 0 0 | X X X X X X X X |
| 0 7 | 8 15 |
| 4C | 00–FF |

| Immediate data field |
|---|
| Zeros |
| 16 31 |

This command causes the attachment to test its storage. Any detected failure causes an interrupt request and sets the equipmet check bit (8) equal to 1 in cycle-steal status word 4.

### Halt I/O

IDCB (immediate device control block)

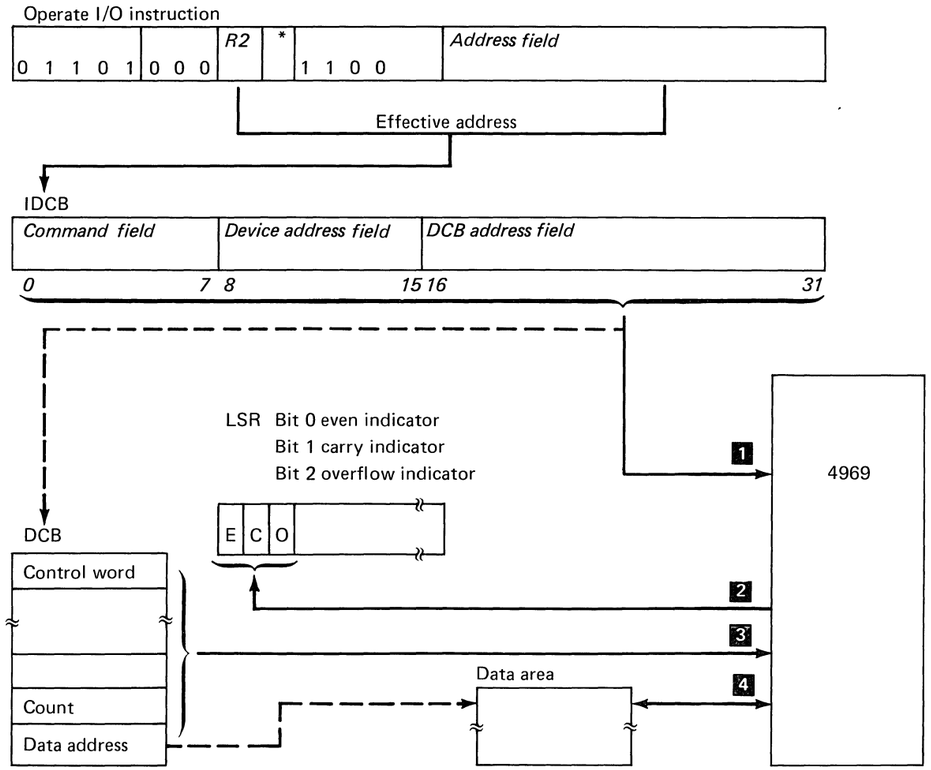
| Command field | Device address field |
|---|---|
| 1 1 1 1 0 0 0 0 | Not used |
| 0 7 | 8 15 |
| F0 | |

| Immediate data field |
|---|
| Not used |
| 16 31 |

This is a channel-directed command that halts all I/O activity on the I/O channel and resets all devices. Any pending interrupt request or busy condition is reset. The prepare level and the residual address are not affected. The IDCB's immediate data field is not used.

## Cycle Steal

Cycle-steal mode permits overlapping an I/O operation with processor operations and other I/O operations (see Figure 2-3). The processor transfers the IDCB under direct program control from processor storage to the 4969 1, and after the 4969 accepts the IDCB, it sends a condition code back to the processor 2. Then the processor is free to continue with other operations while the 4969 uses the information in the IDCB to execute the command. The IDCB's immediate data field contains the address of a DCB. This eight-word DCB contains parameters that define and control the I/O operation. The 4969 cycle steals the DCB words it needs to perform the operation 3. Each data transfer reduces a preset byte count in DCB word 6. When the data transfer ends (byte count equals 0), an interrupt request is sent to the processor 2. The processor then accepts the interrupt condition code and an interrupt ID word from the 4969.



## Start

IDCB (immediate device control block)

| *Command field* | *Device address field* |
|---|---|
| 0 1 1 1 0 0 0 0 | X X X X X X X X |
| *0* *7* | *8* *15* |
| 70 | 00—FF |

| *Immediate data field* |
|---|
| DCB address |
| *16* *31* |

The Start command initiates 4969 I/O operations that transfer data to or from processor storage in cycle-steal mode. An interrupt request is sent to the processor when the I/O operation ends. The control information and parameters required for a particular 4969 operation must be stored in the DCB associated with that operation.

The eight words in the DCB and their bit configurations are explained in the following text and illustrations.

DCB (device control block)

| *Word* | | |
|---|---|---|
| *0* | | *Addr key* |
| | X 0 X 0 X | X X X |
| *1* | Tape unit control | |
| *2* | Unused | |
| *3* | Repeat count | |
| *4* | Residual status block address | |
| *5* | DCB chain address | |
| *6* | Byte count | |
| *7* | Data address | |

DCB control word (word 0)

| | | *Addr key* | |
|---|---|---|---|
| X 0 X 0 X | | X X X | |
| *Bits* *0* *1* *2* *3* *4* *5* *7* | | *8* | *15* |

- Protect key
- Suppress exception
- Not used
- Input flag
- Not used
- Chaining flag

### DCB Word 0—Control Word

***Bit 0—Chaining Flag***

When this bit equals 1, the 4969 performs a chaining operation. Chaining means the 4969 completes the current operation, but does not present an interrupt request to the processor. Instead, the 4969 fetches the next DCB in the chain and performs the next operation. DCB word 5 indicates where the next DCB word is located. Chaining continues until a DCB is fetched that has its chaining bit equal to 0, indicating the last operation in the chain. If an error occurs, chaining to succeeding DCBs is automatically suspended, and an interrupt request is sent to the processor. Normally, an interrupt request is not presented until the 4969 has completed the last operation in the chain.

***Bit 1***

This bit is not used and must be 0.

***Bit 2—Input Flag***

This bit indicates to the 4969 which direction the data is to be transferred. When this bit equals 1, the 4969 transfers data into processor storage; when this bit equals 0, the data transfer is from processor storage to the 4969.

***Bit 3***

This bit is not used and must be 0.

***Bit 4—Suppress Exception***

The user program can be designed to recover from certain errors that occur when the suppress exception bit equals 1. (See "Error recovery" later in this chapter.)

When this bit equals 1:

- It suppresses the reporting of some exception conditions that otherwise would cause an exception interrupt request.
- It allows certain 4969 operations to be retried (see individual operations in this chapter).
- The 4969 status is stored at the address specified by the residual status block address in DCB word 4.

The residual status block is available at the end of an operation that uses the suppress exception bit.

The format and a description of the residual status block follow:

Residual status block

| *Word* | |
|---|---|
| *0* | Residual byte count |
| *1* | Residual status block flags |
| *2* | Overflow byte count |
| *3* | Residual address |
| *4* | Error status word |
| *5* | Last DCB address |

*Word 0—Residual Byte Count.* This word contains the byte count that was specified in DCB word 6, less the number of bytes transferred.

*Word 1—Residual Status Block Flags.* The bit meanings for this word are as follows:

| Bit | Meaning |
|---|---|
| 0 | Equals 1 if bit 0 of DCB word 0 equals 0 |
| 1 | Equals 1 if a retry operation was performed |
| 2–11 | Not used |
| 12 | Equals 1 if a corrected error was detected during a read or space operation |
| 13 | Equals 1 if a controller parity error occurred |
| 14 | Equals 1 if the record read from tape was shorter or longer than the byte count specified in DCB word 6 |
| 15 | Equals 1 to indicate no error |

*Word 2—Overflow Byte Count.* Specifies the number of bytes of a tape record that were not transferred to processor storage because the record was longer than the DCB byte count specified in DCB word 6 for that read operation.

*Word 3—Residual Address.* This word contains the address of the data for the last cycle-steal data transfer.

*Word 4—Error Status Word.* The bit meanings for this word are as follows:

| Bit | Meaning |
|---|---|
| 0 | Equals 1 to indicate an equipment error<br>The adapter card failed to transfer a character before the next transfer was required. |
| 1 | Equals 1 for any tape error (PE or NRZI) |
| 2 | Equals 1 for a PE read operation that has detected a single track error and the error has been corrected |
| 3 | Equals 1 if the parity bit of the CRC character equals 1 |
| 4 | Equals 1 to indicate:<br>• A backspace operation is initiated when tape is at load point.<br>• A write record, write tape mark, or erase operation is initiated when there is no write-enable ring installed.<br>• An operation other than a write is initiated during IBG time of a previous write operation. |
| 5 | Equals 1 to indicate an equipment error<br>A parity error other than a buffer parity error detected in the adapter card. |
| 6 | Equals 1 to indicate an equipment error<br>Adapter buffer parity error. |
| 7 | Equals 1 to indicate a tape parity error that has been detectected by the control board |
| 8 | Equals 1 to indicate an equipment error<br>Attachment detected hardware error. |
| 9 | Equals 1 to indicate an equipment error<br>Attachment detected an internal parity error. |
| 10 | Equals 1 to indicate an equipment error<br>Attachment detected that a transfer operation took to long or failed to complete. |
| 11 | Equals 1 to indicate an equipment error<br>An error occurred during a Start Cycle Steal Status command. |
| 12–15 | These bits contain the number of read retry operations performed after a tape parity error (Bits 1 and 7 equal to 1) |

*Word 5—Last DCB Address.* This word contains the starting address of the last DCB used by the selected tape unit.

***Bits 5–7—Cycle Steal Address Key***

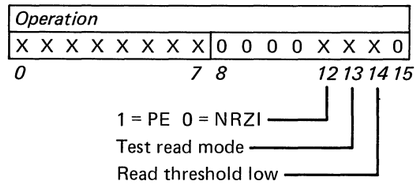
This is a three-bit key that the 4969 presents to the processor during data transfers to verify that the program has authorization to access processor storage. An invalid address key causes an exception interrupt request (condition code 2).

***Bits 8–15***

These bits are not used and must be 0.

**DCB Word 1—Tape Unit Control**

As the following chart shows, bits 0–7 define the operation to be performed. The subsequent paragraphs describe each operation.




| Bits 0–7 (in hex) | Operation |
|---|---|
| 30 | Rewind offline |
| 70 | Offline |
| B0 | Rewind |
| DE | Backspace tape mark |
| DF | Backspace record |
| EE | Forward space tape mark |
| EF | Forward space record |
| F7 | Erase |
| FB | Write tape mark |
| FD | Read record |
| FE | Write record |

***Rewind Offline***

The rewind offline operation causes the selected tape unit to rewind the tape and switch to an offline state. A device-end interrupt request (interrupt condition code 3) is presented as soon as the offline operation is accepted by the tape unit.

Programming considerations:

- A device-end interrupt request does not indicate that the tape has reached load point, but only that the rewind operation has been initiated and that the offline operation has been accepted.
- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address. Operations requested of a tape unit that is offline cause an exception interrupt request (interrupt condition code 2).

***Offline***

The offline operation causes the selected tape unit to switch to an offline state. A device-end interrupt request (interrupt condition code 3) is presented as soon as the offline operation is accepted by the tape unit.

Programming considerations:

To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address. Operations requested of a tape unit that is offline cause an exception interrupt request (interrupt condition code 2).

***Rewind***

The rewind operation causes the selected tape unit to rewind the tape to load point. A device-end interrupt request (interrupt condition code 3) is presented when the tape is at load point and the tape unit is ready. Other tape operations can be requested of other tape units while the rewinding is being done. If the rewind operation is completed before the other operation, the device-end interrupt request for the rewind is delayed until after the other operation is complete.

Programming considerations:

- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address.
- If the selected tape unit is not ready or becomes not ready, an exception interrupt request (interrupt condition code 2) is presented with interrupt status byte bit 0 equal to 1 (device dependent status available).

***Backspace Tape Mark***

The backspace tape mark operation causes the selected tape unit to backspace until a tape mark is detected. A device-end interrupt request (interrupt condition code 3) is presented at the completion of the operation.

Programming considerations:

- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address.

- To space over more than one tape mark, enter the number of tape marks to be spaced over into DCB word 3 (repeat count). A count of 0 or 1 causes one space operation.
- Bit 12 of DCB word 1 must equal 1 for PE and 0 for NRZI. If the NRZI/PE mode bit is not correctly set or if the selected tape unit is not ready, becomes not ready, or is at load point, an exception interrupt request (interrupt condition code 2) is presented with interrupt status byte bit 0 equal to 1 (device dependent status available).

***Backspace Record***

This operation causes the selected tape unit to backspace one record. A device-end interrupt request (interrupt condition code 3) is presented at the completion of the operation.

Programming considerations:

- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address.
- To space over more than one record, enter the number of records to be spaced over into DCB word 3 (repeat count). A count of 0 or 1 causes one space operation.
- Bit 12 of DCB word 1 must equal 1 for PE and 0 for NRZI. If the NRZI/PE mode bit is not correctly set or if the selected tape unit is not ready, becomes not ready, or is at load point, an exception interrupt request (interrupt condition code 2) is presented with interrupt status byte bit 0 equal to 1 (device dependent status available).

***Forward Space Tape Mark***

The forward space tape mark operation causes the selected tape unit to space forward until a tape mark is detected. A device-end interrupt request (interrupt condition code 3) is presented at the completion of the operation.

Programming considerations:

- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address.
- To space over more than one tape mark, enter the number of tape marks to be spaced over into DCB word 3 (repeat count). A count of 0 or 1 causes one space operation.
- Bit 12 of DCB word 1 must equal 1 for PE or 0 for NRZI. If the NRZI/PE mode bit is not correctly set or if the selected tape unit is not ready or becomes not ready, an exception interrupt request (interrupt condition code 2) is presented with interrupt status byte bit 0 equal to 1 (device dependent status available).

***Forward Space Record***

The forward space record operation causes the selected tape unit to space the tape forward one record. A device-end interrupt request (interrupt condition code 3) is presented at the completion of the operation.

Programming considerations:

- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address.
- To space over more than one record, enter the number of records to be spaced over in word 3 (repeat count). A count of 0 or 1 causes one space operation.
- Bit 12 of DCB word 1 must equal 1 for PE or 0 for NRZI. If the NRZI/PE mode bit is not correctly set or if the selected tape unit is not ready, becomes not ready, or detects a tape mark, an exception interrupt request (interrupt condition code 2) is presented with interrupt status byte bit 0 equal to 1 (device dependent status available).

***Erase***

The erase operation causes the selected tape unit to erase approximately 92 mm (3.7 in) of tape. A device-end interrupt request (interrupt condition code 3) is presented at the completion of the operation.

Programming considerations:

- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address.
- DCB word 3 (bits 8–15) defines the number of erase operations to be performed. A count of 0 or 1 causes one erase operation.
- If an erase operation is attempted on a tape unit that is file protected, is not ready, becomes not ready, or has detected an end-of-tape marker, an exception interrupt request (interrupt condition code 2) is presented with interrupt status byte bit 0 equal to 1 (device dependent status available).

***Write Tape Mark***

The write tape mark operation causes the tape unit to write a tape mark on the tape. A device-end interrupt request (interrupt condition code 3) is presented at the completion of the operation.

Programming considerations:

- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address.
- Bit 12 of DCB word 1 must equal 1 for PE or 0 for NRZI. If the NRZI/PE mode bit is not correctly set or if the selected tape unit is not ready, becomes not ready, is file protected, has detected an end-of-tape marker, or a tape mark is not detected after a write tape mark operation (Start Cycle Steal Status word 3 bit 5 equal 0), an exception interrupt request (interrupt condition code 2) is presented with interrupt status byte bit 0 equal to 1 (device dependent status available).

***Read Record***

The read record operation causes the selected tape unit to read one record. The amount of data to be transferred is specified by DCB word 6 and the starting processor storage address is specified by DCB word 7. The byte count in DCB word 6 may be even or odd, but the starting address in DCB word 7 must be even. If the record read is shorter or longer than the byte count specified in DCB word 6 and the suppress exception bit (bit 4) in DCB word 0 is off, an exception interrupt request (interrupt condition code 2) occurs with bits 0 and 2 equal to 1 in the interrupt status byte (device dependent status available and incorrect record length).

Programming considerations:

- When bit 14 (read threshold low) of DCB word 1 equals 1, the tape unit changes the read threshold to enable the recovery of low-amplitude data.
- When bit 13 (test read) of DCB word 1 equals 1, additional data can be added to the read data. The type of data depends on whether the read operation was done in NRZI or PE mode. For NRZI, the CRC and LRC bytes are added; for PE, the postamble (41 bytes consisting of one byte of all ones followed by 40 bytes of all zeros) is added to the record read. The byte count in DCB word 6 must include the additional test read mode bytes to prevent an incorrect record length interrupt request. Read operations in PE mode with test read mode bit equal to 1 will cause an exception interrupt with interrupt information byte bit 0 equal to 1 and status word 4 bit 6 (buffer parity error) equal to 1.

  When the test read mode bit equals 1 and data with incorrect parity is read from the tape, the attachment corrects the parity before sending it to processor storage.
- If the attachment detects a parity error and the suppress exception bit equals 0, an exception interrupt request occurs with bit 0 of the interrupt status byte equal to 1. If the suppress exception bit equals 1, the attachment backspaces over the failing record, complements the read threshold low bit, and reads the record again. This sequence is repeated 16 times or until the record is successfully read. If the retry is successful, a device-end interrupt request is presented with bit 0 of the interrupt information byte equal to 1 and the number of retry operations reported in the residual status word 4. If the retry is unsuccessful an exception interrupt request occurs with bit 0 of the interrupt status byte equal to 1.
- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address. The number of retry operations and corrected errors for all read operations within a chain are presented with the device-end interrupt request at the end of the chain if the suppress exception bit equals 1 (DCB word 0, bit 4).
- Bit 12 of DCB word 1 must equal 1 for PE or 0 for NRZI. If the NRZI/PE mode bit is not correctly set or if the selected tape unit is not ready or becomes not ready, or detects a tape mark, an exception interrupt request (interrupt condition code 2) is presented with interrupt status byte bit 0 equal to 1 (device dependent status available).

***Write Record***

The write record operation causes a record to be written on the selected tape unit. The starting processor storage address of the record to be written is specified by DCB word 7 and must be an even address. The length of the record is specified by DCB word 6 and must be even.

Programming considerations:

- To use DCB chaining, bit 0 of DCB word 0 must equal 1 and DCB word 5 must contain the chain address.
- A byte count of 0 results in a no-op with an interrupt condition code of 3.
- If a write operation is attempted on a tape unit that is file protected, is not ready, or becomes not ready, an exception interrupt request (interrupt condition code 2) is presented with interrupt status byte bit 0 equal to 1 (device dependent status available).
- Bit 12 of DCB word 1 must equal 1 for PE or 0 for NRZI. If the NRZI/PE mode bit is not correctly set or if the end-of-tape marker is detected, the operation ends with an exception interrupt request (interrupt condition code 2) presented with interrupt status byte bit 0 equal to 1 (device dependent status available).

**DCB Word 2**

This word is not used and not checked.

**DCB Word 3—Repeat Count**

The repeat count (bits 8–15) is used on space record (forward and reverse) and space tape mark (forward and reverse) operations. It specifies the number of records or file marks to space over, expressed as an eight-bit unsigned integer, and can range from 0 through 255. The repeat count can also be used for repeat erase operations. Bits 0–7 are not used and must be zeros.

**DCB Word 4—Residual Status Block Address**

The address contained in this word points to the beginning of a processor storage area where the residual status block is stored. The residual status block is stored only when the suppress exception bit equals 1.

**DCB Word 5—Chaining Address**

The chaining address is the location of the next DCB to be executed if the chaining flag bit (bit 0 of DCB word 0) equals 1. If the chaining address is odd, an exception interrupt request is posted and the DCB specification check bit (3) is set to 1 in the ISB.

**DCB Word 6—Byte Count**

This word contains a 16-bit unsigned integer representing the number of data bytes to be transferred for the current DCB. If the byte count equals 0, no data is transferred. For a read operation, the byte count can be any number from 1 through 65,535; for a write operation, it must be an even number from 2 through 65,534.

**DCB Word 7—Data Address**

This word contains the starting processor storage address for the data associated with the operation to be performed and must be an even address.

## Start Cycle Steal Diagnostic

IDCB (immediate device control block)

| *Command field* | | | | | | | *Device address field* | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | X | X | X | X | X | X | X |
| *0* | | | | | | *7* | *8* | | | | | | | *15* |
| 7D | | | | | | | 00–FF* | | | | | | | |

| *Immediate data field* |
|---|
| DCB address |
| *16* *31* |

*Device address field must be the address of tape unit 0.

The Start Cycle Steal Diagnostic command is used to diagnose the attachment feature card and controller feature in tape unit 0. Results from the execution of this command are unpredictable.

DCB (device control block)

| *Word* | *Control word* | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *0* | 0 | 0 | X | 0 | 0 | *Addr key* | X | X | X | X | X | X | X | X | | |
| | *0* | | | | *4* | *5* | | *7* | *8* | | | | | | | *15* |
| *1* | Not used (zeros) | | | | | | | | | | | | | | | |
| *2* | Not used (zeros) | | | | | | | | | | | | | | | |
| *3* | Not used (zeros) | | | | | | | | | | | | | | | |
| *4* | Not used (zeros) | | | | | | | | | | | | | | | |
| *5* | Not used (zeros) | | | | | | | | | | | | | | | |
| *6* | Byte count | | | | | | | | | | | | | | | |
| *7* | Data address | | | | | | | | | | | | | | | |

Bits 2 and 8–15 of the control word define the test to be performed. The following paragraphs describe each test.

Control word

| | | | | | *Addr key* | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | X | 0 | 0 | X | X | X | X | X | X | X | X | X | X |
| *0* | | | | *4* | *5* | | *7* | *8* | | | | | | *15* |
| | | | | | **Bits 8–15** | | | | | | | | | |

| **Bit 2** | **(in hex)** | **Test** |
|---|---|---|
| 1 | 02 | Diagnostic wrap A |
| 1 | 03 | Diagnostic wrap B |
| 1 | 04 | Diagnostic wrap C |
| 1 | 05 | Diagnostic wrap D |
| 1 | 06 | Diagnostic wrap E |
| 1 | 10 | Read diagnostic patch |
| 0 | 11 | Write diagnostic patch |
| 1 | 12 | Read only storage diagnostic |
| 1 | 13 | Diagnostic read |
| 0 | 14 | Diagnostic write |

**Diagnostic Wraps A–E**

These tests are used to verify the correct operation of portions of the controller feature in tape unit 0. Correct operation is reported by a device-end interrupt request; an error causes an exception interrupt request.

**Read Diagnostic Patch**

This test is used to read the patch area of the attachment's storage.

**Write Diagnostic Patch**

This test is used to write into the patch area of the attachment's storage.

**Read Only Storage Diagnostic**

This test causes the attachment to generate a check-sum word and then cycle steal two words into processor storage. the first word is the calculated checksum word and the second word is the reference checksum word.

**Diagnostic Read**

This test exercises the attachment's cycle-steal data bus in the read direction.

**Diagnostic Write**

This test exercises the attachment's cycle-steal data bus in the write direction. During execution of this test, the attachment's controls are electrically isolated from the controller feature. A parity error causes an exception interrupt request with the equipment error bit (9) equal to 1 in cycle-steal status word 4.

## Start Status

IDCB (immediate device control block)

| *Command field* | | | | | | | *Device address field* | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X |
| *0* | | | | | | *7* | *8* | | | | | | | *15* |
| 7E | | | | | | | 00–FF | | | | | | | |

| *Immediate data field* |
|---|
| DCB address |
| *16* *31* |

DCB (device control block)

| *Word* | *Control word* | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *0* | 0 | 0 | 1 | 0 | 0 | *Addr key* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | *0* | | | | *4* | *5* | | *7* | *8* | | | | | | | *15* |
| *1* | Not used (zeros) | | | | | | | | | | | | | | | |
| *2* | Not used (zeros) | | | | | | | | | | | | | | | |
| *3* | Not used (zeros) | | | | | | | | | | | | | | | |
| *4* | Not used (zeros) | | | | | | | | | | | | | | | |
| *5* | Not used (zeros) | | | | | | | | | | | | | | | |
| *6* | Byte count ( hex 2 ) | | | | | | | | | | | | | | | |
| *7* | Data address | | | | | | | | | | | | | | | |

The Start Status command initiates a cycle-steal operation to obtain the currently selected tape unit's status word.

**Status Word**

The bit meanings for this word are as follows:

***Bit 0—Ready.*** This bit equals 1 if all of the following conditions exist in the tape unit and controller:

- All interlocks are closed.
- The initial load sequence is complete after applying power.
- The tape unit is online.
- The tape unit is not rewinding.

***Bit 1—NRZI.*** This bit equals 1 for a NRZI tape unit or 0 for a PE tape unit. For dual mode tape units this bit equals 1.

***Bit 2—File Protect.*** This bit equals 1 when a reel of tape that does not have a write-enable ring is mounted on a tape unit.

***Bit 3—Load Point.*** This bit equals 1 when:

- The beginning-of-tape marker is sensed.
- All interlocks are closed.
- The initial load or rewind sequence is complete.

***Bits 4 and 5.*** Not used.

***Bit 6—Tape Controller Busy.*** This bit equals 1 from the time the tape controller has accepted a command until the operation is completed and tape motion has ceased. Offline, rewind, and rewind offline operations do not cause the tape controller to become "busy."

***Bits 7–11.*** Not used.

***Bit 12—Tape Controller Power On.*** This bit equals 1 when power is applied to the tape unit that contains the controller.

***Bits 13–15.*** Not used.

## Start Cycle Steal Status

IDCB (immediate device control block)

| *Command field* | *Device address field* |
|---|---|
| 0 1 1 1 1 1 1 1 | X X X X X X X X |
| *0* 7 | *8* 15 |
| 7F | 00–FF |

| *Immediate data field* |
|---|
| DCB address |
| *16* *31* |

The Start Cycle Steal Status command initiates a cycle-steal operation to obtain residual parameters from the device that performed the previous cycle-steal operation. These parameters are transferred from the attachment to processor storage by using DCB words 0, 6, and 7. The byte count in word 6 must be hex 0010.

DCB (device control block)

| *Word* | |
|---|---|
| *0* | *Control word* |
| | 0 0 1 0 0 \| *Addr key* \| 0 0 0 0 0 0 0 0 |
| | *0* 4 5 7 8 15 |
| *1* | Not used (zeros) |
| *2* | Not used (zeros) |
| *3* | Not used (zeros) |
| *4* | Not used (zeros) |
| *5* | Not used (zeros) |
| *6* | Byte count ( hex 10 ) |
| *7* | Data address of status word 0 (must be even) |

**Cycle Steal Status Words**

| *Word* | |
|---|---|
| *0* | Residual address |
| *1* | Residual byte count |
| *2* | Overflow byte count |
| *3* | Residual status word 1 |
| *4* | Residual status word 2 |
| *5* | Current status word |
| *6* | Residual repeat count |
| *7* | Last DCB address |

***Word 0—Residual Address***

This word contains the processor storage address of the last cycle-steal transfer attempted for a Start command. The residual address might be a data address, a DCB address, or a residual-status-block address.

***Word 1—Residual Byte Count***

This word contains the byte count as it was specified in DCB word 6 of the last cycle-steal operation, less the number of bytes successfully transferred.

***Word 2—Overflow Byte Count***

This word specifies the number of bytes of a tape record that were not transferred to processor storage on a tape read operation because the record was longer than the DCB byte count specified for that read operation.

***Word 3—Residual Status Word 1***

This word contains ending status information about the last command executed by the selected tape unit.

***Bit 0—Ready.*** This bit equals 1 if all of the following tape unit and controller conditions exist:

- All interlocks are closed.
- The initial load or rewind sequence is complete.
- The tape unit is online.
- The tape unit is not rewinding.

***Bit 1—NRZI.*** This bit equals 1 for NRZI or 0 for PE. For dual mode tape units this bit equals 1.

***Bit 2—File Protect.*** This bit equals 1 when a reel of tape that does not have a write-enable ring is mounted on a tape unit.

***Bit 3—Load Point.*** This bit equals 1 when:

- The beginning-of-tape marker is sensed.
- All interlocks are closed.
- The initial load or rewind sequence is complete.

***Bit 4—End of Tape.*** This bit equals 1 when the tape unit has sensed the end-of-tape marker.

***Bit 5—Tape Mark.*** This bit equals 1 when a tape mark has been detected during the last data transfer.

***Bit 6—Tape Controller Busy.*** This bit equals 1 from the time the tape controller has accepted a command until the operation has ended and tape motion has ceased.

***Bit 7—Idents.*** This bit equals 1 when the selected tape unit senses the PE identity burst in the beginning-of-tape marker area of the tape and is only valid when processing the first record on tape.

***Bit 8—Command Sent.*** This bit equals 1 if a Start command has been sent to the tape unit.

***Bit 9.*** Not used.

***Bit 10—Any Error.*** This bit equals 1 when residual status word 2 contains error indications.

***Bit 11.*** Not used.

***Bit 12—Tape Controller Power On.*** This bit equals 1 when the tape unit that contains the controller has power on.

***Bit 13.*** Not used.

***Bit 14—Threshold Level.*** This bit equals 1 when the last read operation was completed at the low read threshold level.

***Bit 15.*** Not used.

***Word 4—Residual Status Word 2***

This word contains ending status information about the last command executed by the selected tape unit. The bit meanings for this word are as follows:

| Bit | Meaning |
|---|---|
| 0 | Equals 1 to indicate an equipment error<br>The adapter card failed to transfer a character before the next transfer was required. |
| 1 | Equals 1 for any tape error (PE or NRZI) |
| 2 | Equals 1 for a PE read operation that has detected a single track error and the error has been corrected |
| 3 | Equals 1 if the parity bit of the CRC character equals 1 |
| 4 | Equals 1 to indicate:<br>• A backspace operation is initiated when tape is at load point.<br>• A write record, write tape mark, or erase operation is initiated when there is no write-enable ring installed.<br>• An operation other than a write is initiated during IBG time of a previous write operation. |
| 5 | Equals 1 to indicate an equipment error<br>A parity error other than a buffer parity error detected in the adapter card. |
| 6 | Equals 1 to indicate an equipment error<br>Adapter buffer parity error. |
| 7 | Equals 1 to indicate a tape parity error that has been detected by the control board |
| 8 | Equals 1 to indicate an equipment error<br>Attachment detected hardware error. |
| 9 | Equals 1 to indicate an equipment error<br>Attachment detected an internal parity error |
| 10 | Equals 1 to indicate an equipment error<br>Attachment detected that a transfer operation took to long or failed to complete. |
| 11 | Equals 1 to indicate an equipment error<br>An error occurred during a Start Cycle Steal Status command. |
| 12–15 | These bits contain the number of read retry operations performed after a tape parity error. (Bits 1 and 7 equal to 1) |

***Word 5—Current Status***

This word contains the status of the selected tape unit at the time the Start Cycle Steal status block was presented.

*Bit 0—Ready.* This bit equals 1 if the following conditions exist in the tape unit and controller:

- All interlocks are closed.
- The initial load sequence is complete after applying power.
- The tape unit is online.
- Tape unit is not rewinding.

*Bit 1—NRZI.* This bit equals 1 for NRZI or 0 for PE. For dual mode tape units this bit equals 1.

*Bit 2—File Protect.* This bit equals 1 when a reel of tape that does not have a write-enable ring is mounted on a tape unit.

*Bit 3—Load Point.* This bit equals 1 when:

- The beginning-of-tape marker is sensed.
- All interlocks are closed.
- The initial load or rewind sequence is complete.

*Bit 4.* Not used.

*Bit 5.* Not used.

*Bit 6—Tape Controller Busy.* This bit equals 1 from the time the tape controller has accepted a command until the operation is completed and tape motion has ceased. Rewind and offline operations do not cause the tape controller to become "busy."

*Bits 7–11.* Not used.

*Bit 12—Tape Controller Power On.* This bit equals 1 when power is applied to the tape unit that contains the controller.

*Bits 13–15.* Not used.

***Word 6—Residual Repeat Count***

This word contains the count as it was specified in DCB word 3, less the number of successful repeat operations.

***Word 7—Last DCB Address***

This word contains the starting address of the last DCB used by the attachment for the selected tape unit.

# Condition Codes and Status Information

## Condition Codes

Each time the attachment receives an Operate I/O instruction, it immediately sends the processor a condition code pertaining to the execution of the I/O command. This three-bit code, representing a decimal number from 0 through 7, is stored in the even, carry, and overflow positions of the level status register (LSR) located in the processor.

Refer to the appropriate processor description manual, listed in the preface under "Prerequisite Publications," for additional information about level status registers.

### Operate I/O Instruction

Condition codes reported after execution of an Operate I/O instruction are:

- CC0—Device not attached
  This condition code is reported when the addressed tape unit is not attached.
- CC1—Busy
  This condition code is reported when the tape unit is unable to execute a command because it is in a busy state. The tape unit enters the busy state upon acceptance of a command that requires an interrupt request for termination. It exits the busy state when the processor accepts the interrupt request.
- CC2—Busy after reset
  This condition code is reported when the tape unit is in the process of being reset.
- CC3—Command reject
  This condition code is reported when:
  – A command is issued that is outside the tape unit command set.
  – The tape unit is in an improper state to execute the command.
  – The IDCB contains an incorrect parameter.
- CC4
  This condition code is not reported.
- CC5—Interface data check
  This condition code is reported when a parity error is detected on the processor I/O channel data bus during a data transfer.
- CC6—Controller busy
  This condition code is reported when the attachment feature to which two or more tape units are attached is busy. A subsequent controller-end interrupt request is presented to the processor. This condition should not occur if the Start commands are issued over 0.5 msec apart.
- CC7—Satisfactory
  This condition code is reported when the attachment feature accepts a command.

### Interrupt Condition Codes

The following condition codes are presented with a priority interrupt request.

- CC0—Controller end
  This condition code is reported by the attachment when a previous Operate I/O condition code 6 (controller busy) was reported and the attachment is free to accept I/O commands.
- CC1
  This condition code is not reported.
- CC2—Exception
  This condition code is reported when an error or exception condition is associated with the interrupt request. The condition is described in the interrupt status byte or in device-dependent status words. The status words can be obtained by executing a Start Cycle Steal Status command.
- CC3—Device end
  This condition code is reported when an operation has terminated under normal conditions.
- CC4—Attention
  This condition code is reported when a tape unit becomes ready. The change from not-ready to ready at the end of a rewind operation doesn't cause an attention interrupt request.
- CC5
  This condition code is not reported.
- CC6—Attention and exception
  This condition code is reported when attention and exception conditions are both present.
- CC7—Attention and device end
  This condition code is reported when attention and device-end conditions are both present.

**Interrupt Identification Word**

The attachment, when presenting a priority interrupt request along with an interrupt condition code, also transfers an interrupt ID word to the processor.

Interrupt ID word

| *IIB (ISB)* | *Device address* |
|---|---|
| X X X X X X X X | X X X X X X X X |
| *0* *7* | *8* *15* |

The attachment provides the interrupt information byte (IIB) with attention or device-end interrupt requests. The IIB for attention and controller-end interrupt requests contains all zeros.

For device-end and attention/device-end interrupt requests, all IIB bits equal 0 except 0. When bit 0 (permissive device end) equals 1, it indicates that information about errors is available in the residual status block. In the case of chained DCBs, this bit indicates that at least one of the residual status blocks stored contains information about errors. When chaining DCBs, this bit equals 1 only if at least one DCB in the chain uses the suppress exception bit option.

**Interrupt Status Byte**

For exception and attention/exception interrupt requests, the eight-bit IIB takes on a different format called an interrupt status byte (ISB). The ISB stores accumulated status information, as described in the following paragraphs.

***Bit 0—Device Dependent Status Available.*** This bit equals 1 when further attachment status information is available in the cycle-steal status block.

***Bit 1—Delayed Command Reject.*** This bit equals 1 to indicate there is an incorrect parameter in the IDCB or that a DPC command was received that is outside of the attachment's command set. Diagnostic operations requested of other than tape unit 0 or of a tape unit that is busy are also rejected.

***Bit 2—Incorrect Record Length.*** This bit equals 1 when the attachment encounters a mismatch between the byte count specified in DCB word 6 and the length of the record read from tape.

***Bit 3—DCB Specification Check.*** This bit equals 1 to indicate that an invalid parameter was found in the DCB, preventing proper execution of the command.

*Examples:*

- An odd-byte chaining address
- An odd address for a start-cycle-steal-status word
- An invalid modifier in control word 1
- An incorrect count

Condition code 2 is reported when the interrupt request is accepted. The residual address points to the right-most byte of the DCB word in which the DCB specification check was found.

***Bit 4—Storage Data Check.*** This bit equals 1 for cycle-steal output operations if the data at the accessed storage location contains a parity error.

***Bit 5—Invalid Storage Address.*** This bit equals 1 as the result of a cycle-steal operation in which the processor storage address used to access data exceeds the storage capacity of the processor.

***Bit 6—Protect Check.*** This bit equals 1 when the attachment attempts to access a processor storage location without using the correct key.

***Bit 7—Interface Data Check.*** This bit equals 1 when a parity error is detected on the data bus during a cycle-steal data transfer.

## How to Check the CRC Character

To check the CRC character, perform the following steps:

1. Read the NRZI record from tape with the test read mode bit (DCB word 1, bit 13) equal to 1. The byte count (DCB word 6) should equal the byte count for this record plus 2 for test read mode (CRC and LRC characters are added).
2. Place the CRC character into bits 8–15 of processor register R5. (Processor register assignments do not have to be those used for this example.)
3. Issue a Start Cycle Steal Status command to obtain the CRC parity bit (start cycle steal status word 4, bit 3).
4. Place this bit into bit 7 of processor register R5.
5. Clear processor register R4.
6. Place the byte of data just read into bits 8–15 of processor register R3 and clear the high order byte of register R3.
7. Determine the parity for this data and set bit 7 of processor register R3 accordingly, to represent the correct parity.
8. Exclusive OR the data in processor register R3 with processor register R4.
9. Shift processor register R4 one position to the right (bit 7 to 8, bit 8 to 9, including so forth, and bit 15 to 7).
10. If bit 7 equals 1, invert bits 10, 11, 12, and 13.
11. Repeat steps 6–10 for each byte of data.
12. Invert all bits except 10 and 12.

The character generated should compare with the CRC character that was read with the record.

A subroutine like the following example could be used:

```
CRCCHK   STM   R6,REGSAVE          SAVE REGISTERS
         TWI   X'0008',RDRDCB+WD1 TEST FOR NRZI MODE
         BON   CRCRTN             BRANCH IF NO
         TWI   X'0004',RDRDCB+WD1 TEST FOR TRD BIT ON
         BOFF  CRCRTN             BRANCH IF NO
*
*  READ CYCLE STEAL STATUS
*
         *
         *
         *     USER ROUTINE TO READ CYCLE STEAL STATUS
         *
         *
*
*  GENERATE CRC CHAR. FOR COMPARE TO ACTUAL CRC CHAR. READ
*
*
*  GET BYTE COUNT AND READ BUFFER ADDR. AND CLEAR THE CRCC REG.
*
         MVW   WRCNT,RO           NO. OF BYTES TO CHECK
         MVBI  0,R4               CLEAR CRCC REGISTER
         MVA   RDBUF,R2           READ BUFFER ADDRESS
*
*  DETERMINE PARITY BIT FOR DATA BYTE
*
CRCLPO   MVBI  0,R6               CLEAR REG. 6
         MVBI  8,R7               LOOP COUNT
         MVB   (R2),R3            GET DATA BYTE
         SLL   8,R3               MOVE TO HIGH ORDER BYTE
         JN    CRCLP2             JUMP IF BIT 0 IS ON
CRCLP1   SLL   1,R3               SHIFT DATA BYTE
         JNN   CRCLP3             JUMP IF BIT 0 IS OFF
CRCLP2   ABI   1,R6               INC. BIT COUNT
CRCLP3   JCT   CRCLP1,R7          LOOP UNTIL DONE
         MVB   (R2)+,R3           GET DATA BYTE AGAIN
         NWI   X'00FF',R3         CLEAR HIGH ORDER BYTE
```

```
*
*  ADD PARITY BIT IF APPLICABLE
*
         MVW   R6,R7              GET PARITY BIT COUNT
         JNEV  NOPRTY             JUMP IF ODD NO. OF BITS
         OWI   X'0100',R3         ADD PARITY BIT
*
*  EXCLUSIVE OR DATA BYTE TO CRC REGISTER
*
NOPRTY   XW    R3,R4              EXCLUSIVE OR TO CRCC REG.
*
*  SHIFT CRC CHAR. RIGHT.  LAST BIT GOES BACK AS PARITY BIT.
*
         SRLD  1,R4               SHIFT THE CRC CHARACTER
         TWI   X'8000',R5         TEST IF BIT 15 OF R4 WAS ON
         JOFF  CRCLP4             JUMP IF NO
         OWI   X'0100',R4         OR IN THE PARITY BIT
*  INVERT BITS 10,11,12, & 13 BECAUSE PARITY BIT BECAME 1
*
         XWI   X'003C',R4         INVERT BITS 10,11,12, & 13
CRCLP4   ABI   -1,R0              DEC. BYTE COUNT REG
         BNZ   CRCLPO             LOOP UNTIL DONE
*
*  INVERT ALL BITS EXCEPT 10 AND 12
*
         XWI   X'01D7',R4         INVERT ALL BUT 10 & 12
         NWI   X'01FF',R4         CLEAR HIGH ORDER BITS
         JZ    CRCRTN             NO COMPARE IF CRCC=0
*
*  GET CRC CHARACTER READ FROM TAPE AND ADD PARITY IF APPLICABLE
*
         MVB   (R2),R5            GET CRC CHAR. FROM READ BUFFER
         NWI   X'00FF',R5         CLEAR HIGH ORDER BYTE
         TWI   X'1000',STATUS     CHECK PARITY BIT IN CSS WORD 4
         JOFF  CRCCOM             JUMP IF OFF
         OWI   X'0100',R5         OR IN PARITY BIT
*
*  COMPARE ACTUAL CRC CHAR. WITH GENERATED CRC CHAR.
*
CRCCOM   CW    R4,R5              COMPARE 2 CRC CHAR.
         JE    CRCRTN             JUMP IF EQUAL
               *
               *     USER ERROR ROUTINE
               *
CRCRTN   LMB   REGSAVE            RETURN TO CALLER
```

## Error Recovery

The user program should be designed to recover from certain errors that occur.

The following chart lists those errors, the priority in which they should be tested for, and the bits to be tested. It also identifies the appropriate action to perform when an error is detected.

| Bit(s) tested | | | | | |
|---|---|---|---|---|---|
| Cycle-steal status word | Bit | Bit condition tested for | Priority | Recommended first action* | Error |
| 3 | 12 | 0 | 1 | 4 | Tape controller power off |
| 3 | 0 | 0 | 2 | 5 | Tape controller not ready |
| 4<br>3 | 6<br>8 | 1<br>0 | 3 | 2 | Equipment error and Start command not sent |
| 4<br>3 | 5<br>8 | 1<br>0 | 4 | 2 | |
| 4<br>3 | 11<br>8 | 1<br>0 | 5 | 2 | |
| 4 | 4 | 1 | 6 | 2 | Tape controller command reject |
| 4<br>3 | 6<br>8 | 1<br>1 | 7 | 1 | Equipment error and Start command sent |
| 4<br>3 | 5<br>8 | 1<br>1 | 8 | 1 | |
| 4<br>3 | 11<br>8 | 1<br>1 | 9 | 1 | |
| 4<br>3 | 8<br>8 | 1<br>0 | 10 | 2 | Equipment error and Start command not sent |
| 4<br>3 | 9<br>8 | 1<br>0 | 11 | 2 | |
| 4<br>3 | 10<br>8 | 1<br>0 | 12 | 2 | |
| 4<br>3 | 8<br>8 | 1<br>1 | 13 | 1 | Equipment error and Start command sent |
| 4<br>3 | 9<br>8 | 1<br>1 | 14 | 1 | |
| 4<br>3 | 10<br>8 | 1<br>1 | 15 | 1 | |
| 4 | 1 | 1 | 16 | 1 | Tape error |
| 4 | 0 | 1 | 17 | 3 | Equipment error |
| 4 | 7 | 1 | 18 | 3 | Tape parity error |
| 4 | 2 | 1 | 19 | 3 (write record only) | Corrected error |

*Described in chart on following page

Error conditions should be tested in order of priority (priority 1 is the highest). Begin the recovery sequence with the recommended action associated with the highest priority error detected. Then perform the remaining actions in sequence. For example, if cycle steal status word 4 bits 4 and 1 equal 1 (priorities 6 and 16) error recovery should begin with action 2.

| Action | Description |
|---|---|
| 1 | Position the tape at its starting point. A procedure must be used to return to the same starting point to ensure the correct IBG has been reached. This can be done by using checkpoints, file labels, and record labels. |
| 2 | Retry the operation that failed. If still unsuccessful, issue an operator message and exit the error recovery procedures. |
| 3 | Backspace the tape to the beginning of the record and then go to action 2. |
| 4 | Ensure that the tape unit with the tape controller (unit 0) has power on. (A message to the operator might be required.) If the power is on, go to action 2; otherwise, exit the error recovery procedures. |
| 5 | Ensure that the selected tape unit is made ready. Wait for an attention interrupt request and then go to action 1. (A message to the operator can also be used here.) |

## Initial Program Load (IPL)

Upon receiving an IPL command, the 4969 performs a rewind operation if the tape is not already positioned at load point. When the tape is at load point, a read record operation is requested of the tape unit. One record (maximum of 65,535 bytes) is read and transferred to processor storage starting at data address 0. A successful IPL terminates with a device-end interrupt request on priority level 0. On dual-density tape units, the IPL read record operation is done only in PE mode.

Cut Along Line

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