IBM SYSTEM/3

Field Engineering

Theory of Operation

5475 Keyboard Attachment

SY31-0247-0

Field Engineering

Theory of Operation

5475 Keyboard Attachment

Preface

This manual explains the logical functions and major circuit objectives for the 5475 Keyboard Attachment.

Other manuals needed to understand and service the 5475 Keyboard Attachment are:

1. The *IBM 5475 Keyboard Attachment Field Engineering Diagrams Manual,* Form SY31-0248.
2. The *The IBM Elastic Diaphragm Encoded Keyboards and 5475, Field Engineering Theory Maintenance Manual,* SY27-0073.
3. The *IBM 5410 Central Processing Unit, Field Engineering Theory of Operation Manual,* Form SY31-0207.
4. The *IBM 5410 Central Processing Unit, Field Engineering Maintenance Diagrams Manual,* Form SY31-0202.
5. The *IBM 5410 Central Processing Unit, Field Engineering Maintenance Manual,* Form SY31-0244.
6. The *IBM 5496 Data Recorder, Field Engineering Theory of Operations Manual,* Form SY31-0220.
7. For data recording and data verifying program information, refer to the *Data Recording and Data Verifying Program Operator's Guide,* Form C21-7538.
8. For machine characteristics, refer to the *IBM System/3 Installation Manual–Physical Planning,* Form A21-9084.

First Edition

Some illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

Changes are continually made to the specifications herein; any such change will be reported in subsequent revisions or FE Supplements.

A form for reader's comments is provided at the back of this publication. If the form has been removed, comments may be addressed to IBM Corporation, Product Publications, Department 245, Rochester, Minnesota 55901.

Contents

The IBM 5475 Data Entry Keyboard Attachment provides a means for the attached IBM 5475 Data Entry Keyboard to use the facilities of the IBM 5410 Central Processing Unit. The attachment handles data and status, and also controls the keyboard functions of the data entry keyboard. The attachment logic is located between the 5410 data channel and the 5475 keyboard (Figure 1-1). The attachment logic is MST-1 and is located on gate A, board B2 of the CPU main frame.

With the data recording and data verifying program in CPU storage, the keyboard attachment and data entry keyboard can be used to simulate the functions of the IBM 5496 Data Recorder. To transcribe data into punched cards (or to verify punched cards) online, the operator uses the keys, switches, and indicators on the 5475 keyboard in the same manner as he would on the 5496 keyboard. The IBM 5424 Multi-Function Card Unit (MFCU) does the punching and reading for verifying.

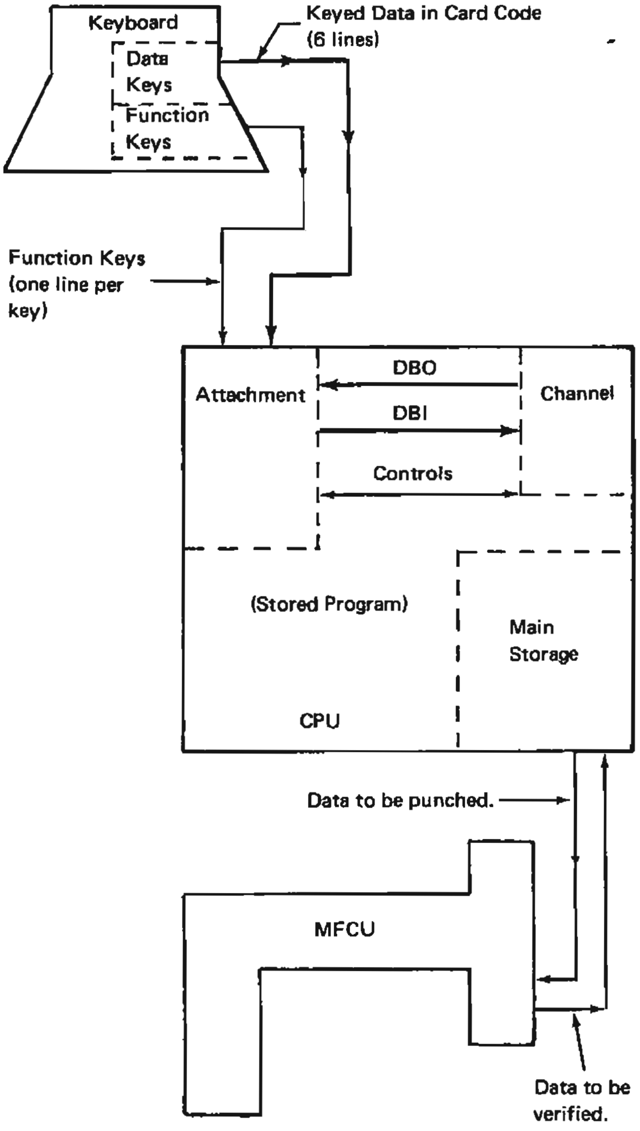


Figure 1-1. Keyboard Data Flow

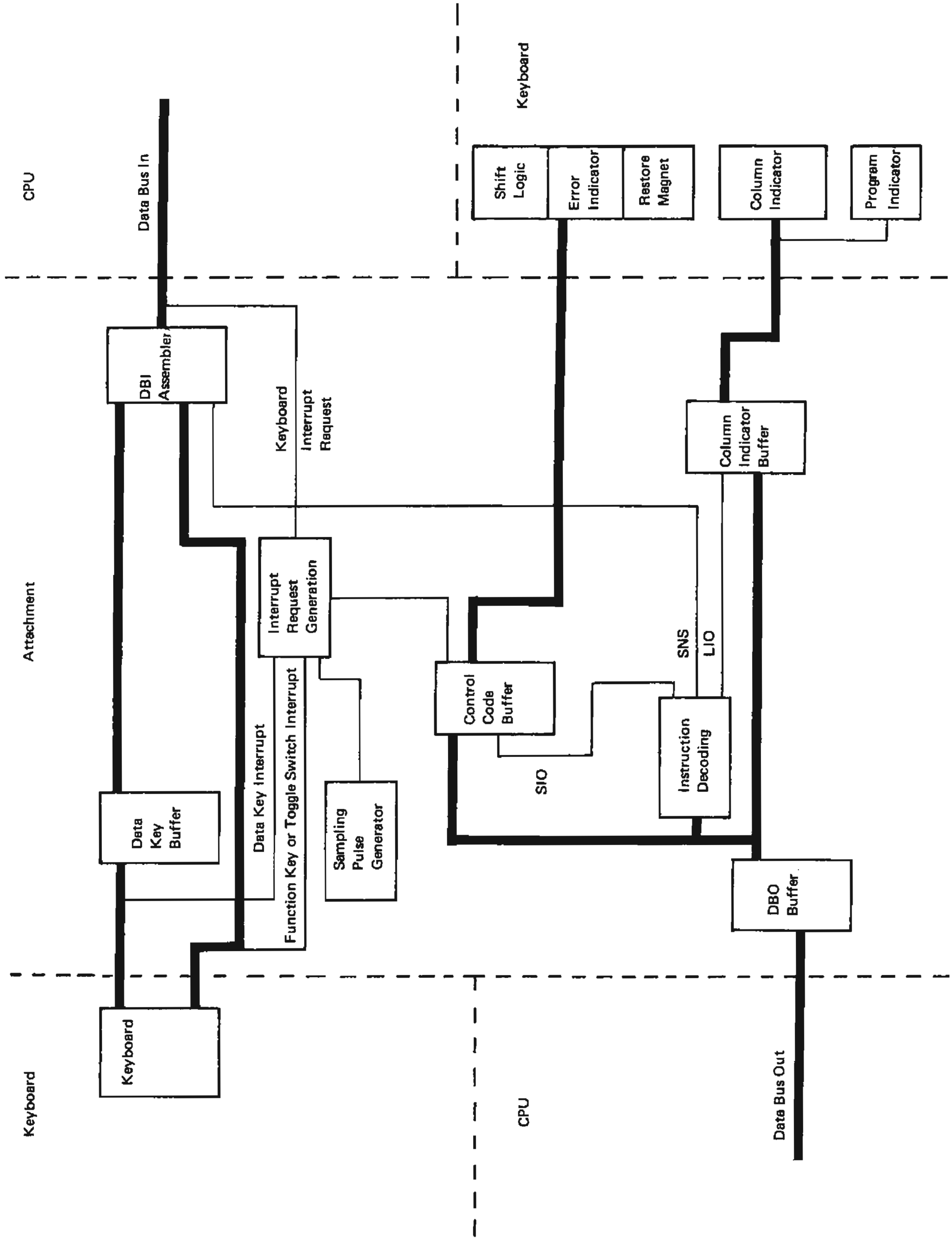


Figure 1-2. Channel Operation

IBM 5475 DATA ENTRY KEYBOARD ATTACHMENT OPERATION

The attachment operates on an interrupt principle, on interrupt level number one (which is number four in interrupt priority). The attachment communicates with the CPU during interrupts (Figure 1-2). Upon receiving a sense I/O (SNS) instruction, information is sent to the CPU main storage.

This SNS instruction is sent to the attachment on data bus out lines and control lines. The attachment decodes the instruction. Then transfers keyboard data and function information to CPU main storage.

The switches, function keys, or data keys are disabled until start I/O (SIO) instruction (with the appropriate bits active in the control code) restores them. Once the keyboard is restored, interrupts are enabled and information can be keyed. After the SIO instruction, a load I/O (LIO) instruction is issued to turn on the column indicator and appropriate program indicator.

Interrupt Request

Activating a toggle switch, a function key, or a data key, generates a 1 bit in the data bus in assembler (DBI). This bit active, requests an interrupt when 'interrupt poll' is active in the CPU at clock 5-7 time. The 'DBI bit 1' line is raised each time 'interrupt poll' is activated until the CPU grants the interrupt. Upon recognizing the interrupt, the CPU issues sense instructions to the attachment. The sense instructions decode the contents of the DBI assembler. The output of the DBI assembler is taken to the CPU on the data bus in lines.

With this information, the stored program in the CPU determines the cause of the interrupt, branches to that routine in the main program, and performs the required operation. When the operation is complete, the CPU can issue another SIO instruction to the attachment.

Instruction Format

Each instruction has an operation code and a Q code, followed by either a control code (SIO), or a storage address (LIO, SNS). Thus the length of the instruction varies between 3 and 4 bytes depending upon the type of instruction and the type of addressing.

The first half byte of the op code (bits 0-3) determines the format of the instruction performed (one address or command), and the method of storage addressing used (indexed or direct). The second half byte of the op code determines the actual operation performed (SIO, LIO, SNS).

Use of the control code or the storage address byte(s) depends upon the operation being performed. Refer to Chapter 3 for a description of the individual instructions.

The test I/O (TIO) and advance program level (APL) instructions are not used with the keyboard attachment. Therefore, any attempt to issue one of these instructions to the keyboard attachment results in a processor check stop and an INV-Q indication.

5475 Data Entry Keyboard

The keyboard has 34 data keys, 12 function keys, 4 indicators, and 6 switches as shown in Figure 1-3.

Data Keys

There are 34 dual shift keys plus the shift independent space bar designated as data keys. These keys are used to generate the 63 characters shown in Figure 1-3 (some characters are present in both shifts) plus blank. The data keys are mechanically interlocked and latched in such a way that two keys can't be pressed at once, yet rolling of the keys is allowed. The attachment generates a program interrupt request each time a data key is pressed. The character keyed is stored as a SNS byte. Restoring of the data keys is controlled by the CPU program through the SIO instruction.

Function Keys

The 12 shaded keys shown in Figure 1-3 are function keys. A description of the keys is in the table following Figure 1-3. They are keystem contact type keys and are not interlocked from each other or from the other keys on the keyboard.

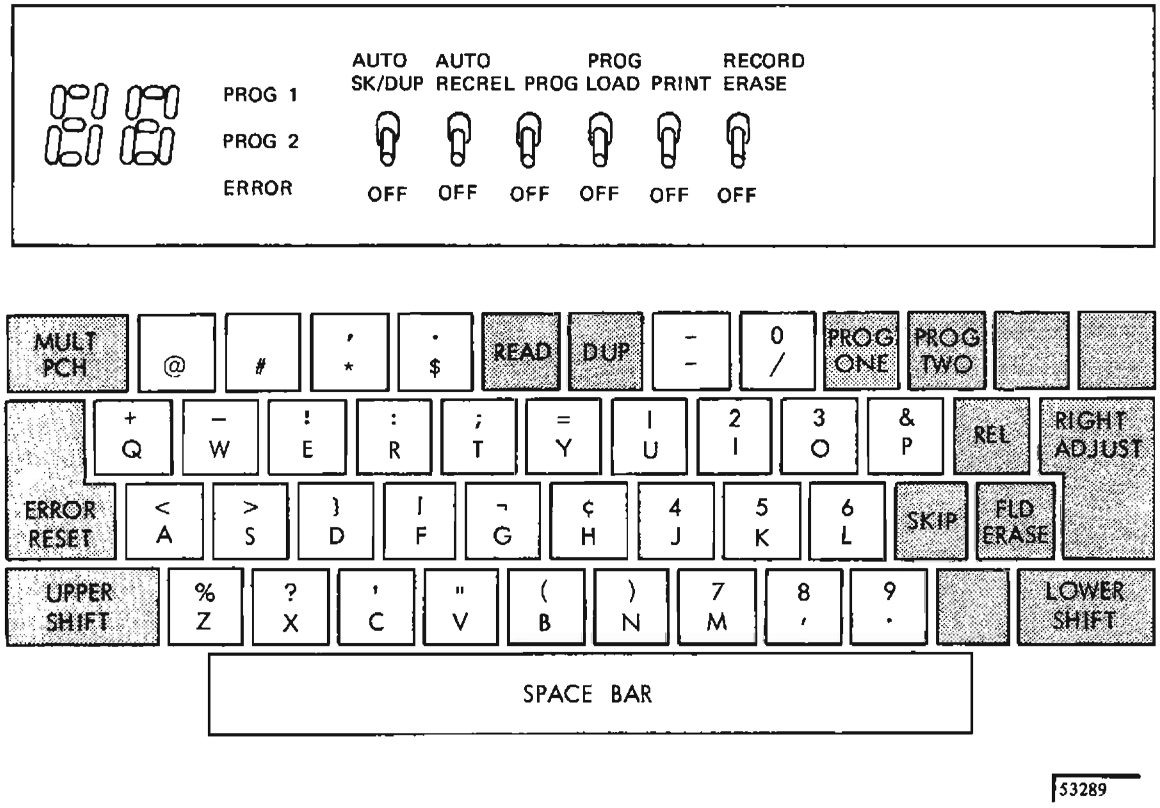


Figure 1-3. Data Entry Keyboard

Function Key Name	Conditions and Functions	Interrupt Request	Available as SNS Information	Function using data recording and data verifying program
Upper shift key	Conditions logic for upper shift characters.	no	no	Places keyboard in upper shift.
Lower shift key	Conditions logic for lower shift characters.	no	no	Places keyboard in lower shift.
Multipunch key	Allows more than one data character to enter the data latches. Conditions logic for upper shift.	yes (On release of the key, if a data key was pressed).	yes	Allows more than one character to be punched in the same column.
Program 1 key	Program switch on	yes	yes	Selects program 1 area in storage as the program card.
	Program switch off	no		
Program 2 key	Program switch on	yes	yes	Selects program 2 area in storage as the program card.
	Program switch off	no		
Release key		yes	yes	Signals the end of manual entries for a card.
Field Erase key		yes	yes	Blanks out the last manually entered field. If the lower shift key is pressed at the same time the field erase is pressed, a word erase function is performed which causes manually entered characters to be blanked out until either a space or the beginning of a field is met.
Error Reset key		yes	yes	Resets error conditions detected by the program.
Read key		yes	yes	Causes a card to be fed from the MFCU primary hopper and read into a data area. Then pressing the dup key duplicates the card.
Skip key	Program switch on	yes (One interrupt per key depression).	yes	Skip the remainder of a field.
	Program switch off	yes (10 interrupts per second as long as the key is pressed).		Columns are skipped at the rate of 10 per second, as long as the key is pressed.

Function Key Name	Conditions and Functions	Interrupt Request	Available as SNS Information	Function using data recording and data verifying program
Dup key	Program switch on	yes (One interrupt per key depression).	yes	Duplicate the remainder of a field.
	Program switch off	yes (10 interrupts per second as long as the key is pressed).		Duplicate columns at the rate of 10 per second, as long as the key is pressed.
Right Adjust key		yes	yes	Causes all characters entered in a field to be moved to the right end of that field and the remaining left end positions filled with blanks.

Indicators

The 4 keyboard indicators are shown in Figure 1-3. A description of each indicator is given in the following table:

Indicator Name	Instruction Turning on the Indicator	Function using data recording and data verifying program
Column Indicator	LIO	Indicates the card column that the next data character keyed enters.
Error Indicator	SIO	Indicates any errors detected by the program, such as a non-compare, while verifying.
Program 1 Indicator	LIO	Indicates program card data loaded in the program 1 area is in control.
Program 2 Indicator	LIO	Indicates program card data loaded in the program 2 area is in control.

Switches

The 6 switches on the keyboard are shown in Figure 1-3. A description of each is given in the following table:

Switch Name	Interrupt request on transfer of switch	Available as SNS Information	Function using data recording and data verifying program
Program Switch	yes	yes	In the off position, no program is selected. In the on position, program 1 is selected. Program 2 is selected by pressing the program 2 key with the program switch on.
Program Load Switch	yes, if the program switch is on.	yes	Causes a card to feed from the primary feed of the MFCU and loads the data from the card into the program area selected.
Record Erase Switch	yes	yes	Blanks out all information entered into the record being keyed.
Auto Record Release Switch	yes	yes	This switch on automatically causes the card to be punched as soon as the last manual entry has been completed.
Auto Skip/ Dup Switch	yes	yes	This switch on allows auto dup and auto skip functions that are coded in the program card to be performed.
Print Switch	no	yes	Allows data to be printed as it is punched in the card.

DATA KEY BUFFER

The data key buffer is an 8 position register used to store the data character that is keyed (Figure 2-1). The keyed data character is translated and stored as a card code character.

Circuit Objectives

Refer to FEMD 4-10.

Data is set into the data key buffer when the kyb bit lines and 'set data latches' line are active. They are reset by 'reset data latches.'

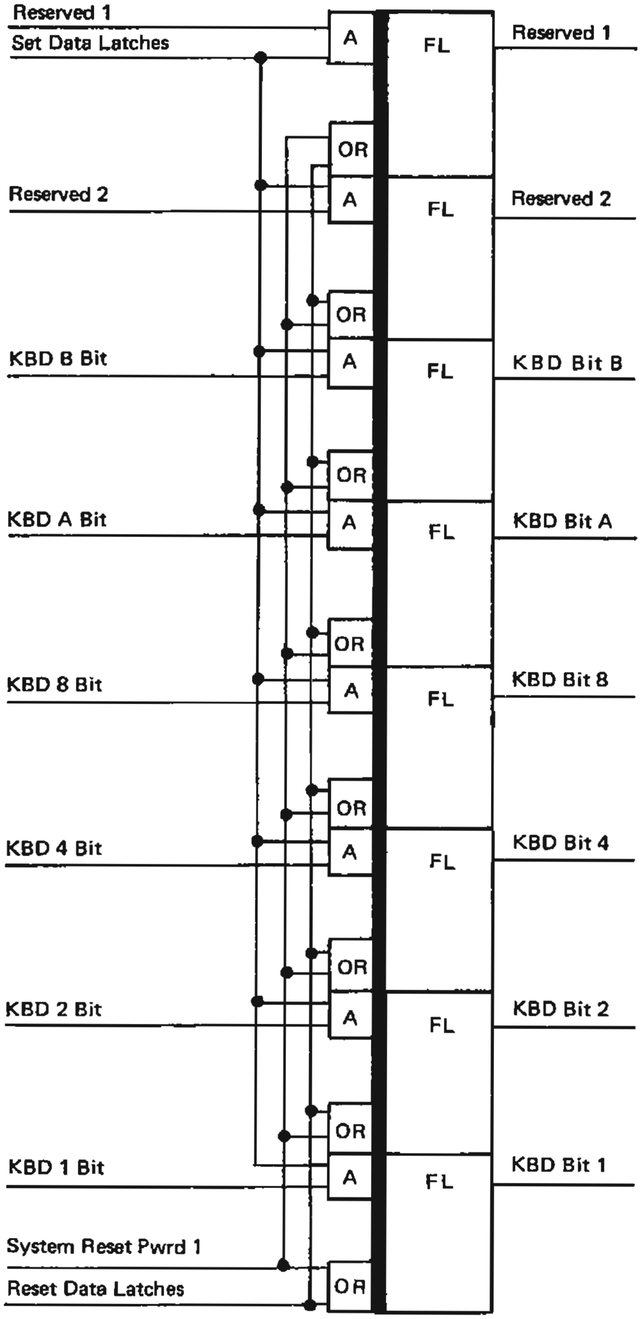


Figure 2-1. Data Key Buffer

DATA BUS OUT BUFFER (DBO)

All data information from the CPU enters the attachment through the DBO buffer which has 9 latches. When the correct device address is decoded, the DBO buffer places the data information into the appropriate register in the attachment (Figure 2-2).

Circuit Objectives

Refer to FEMD 4-15.

The DBO buffer is loaded by activating the 'load DBO buffer' line and chan DBO lines.

COLUMN INDICATOR BUFFER (CIB)

LIO instruction loads the CIB with 2 bytes of data. The presence of data in the CIB lights the units and tens position of the column indicator and the program 1 and program 2 indicators. The data addressed by a LIO instruction is used to light the segments of the column indicator and the program indicators (Figure 2-3).

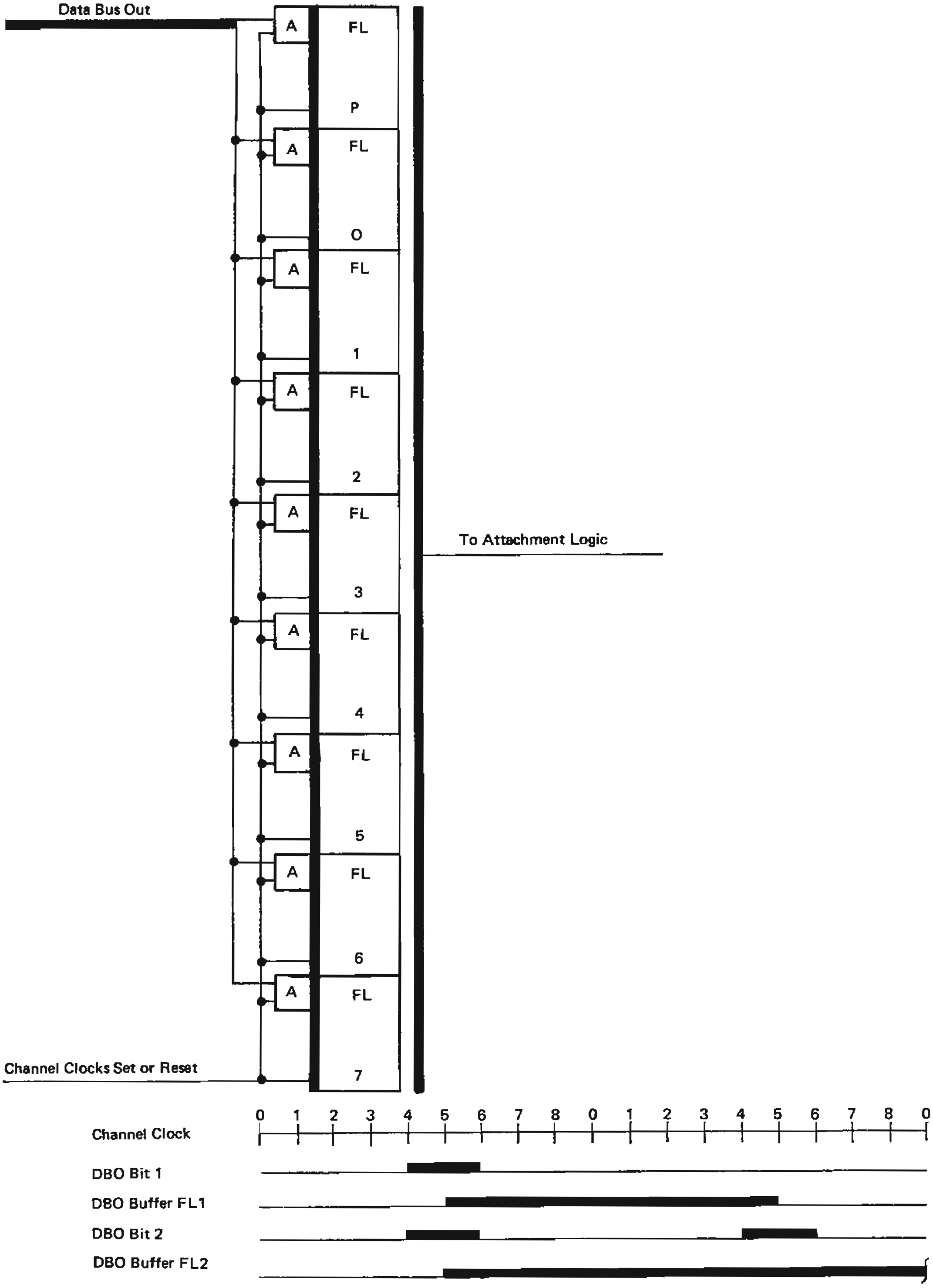
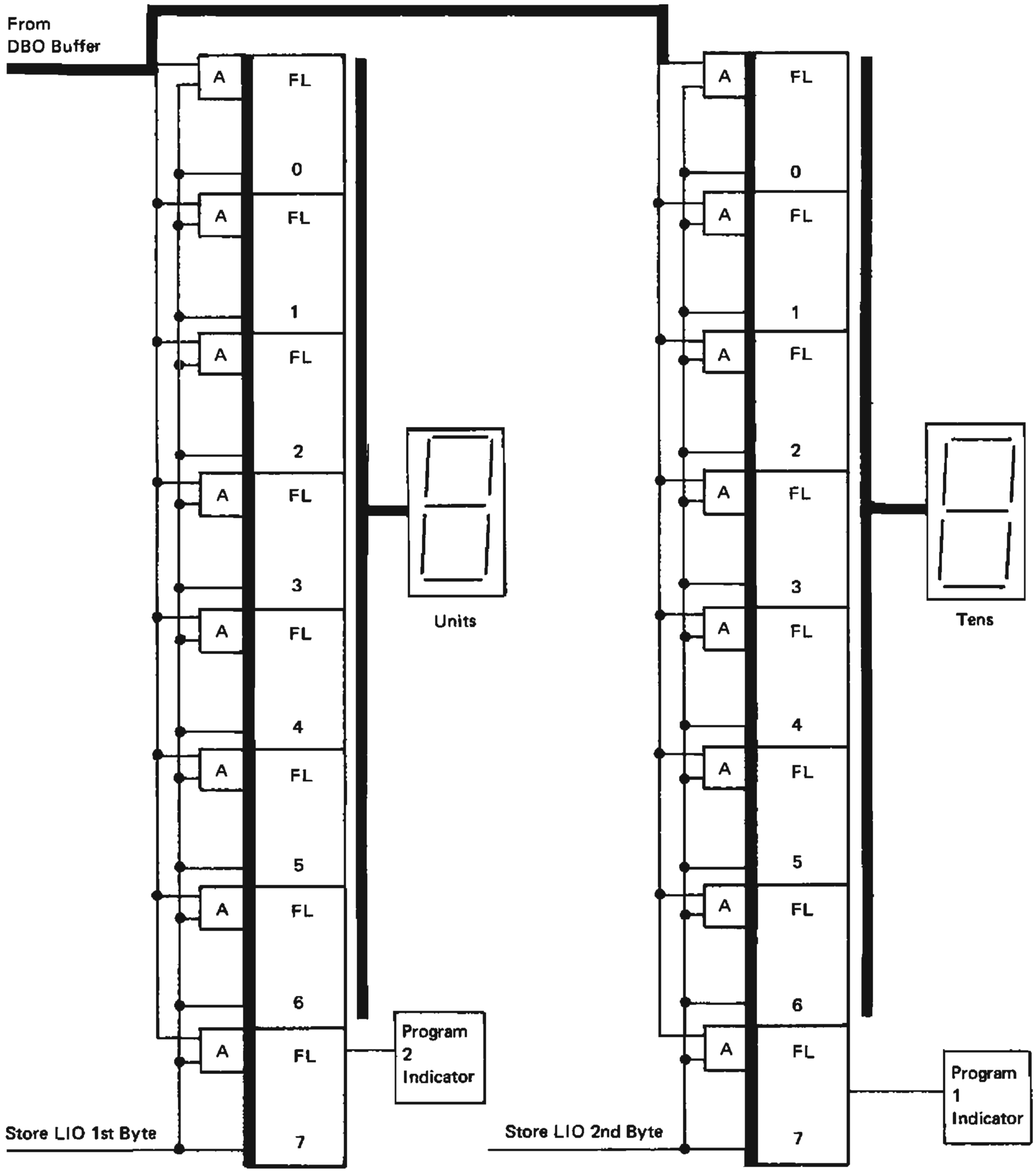


Figure 2-2. Data Bus Out Buffer



Note: Store LIO 1st byte and store LIO 2nd byte occur at CPU clock 6 time.

Figure 2-3. Column Indicator Buffer

Circuit Objectives

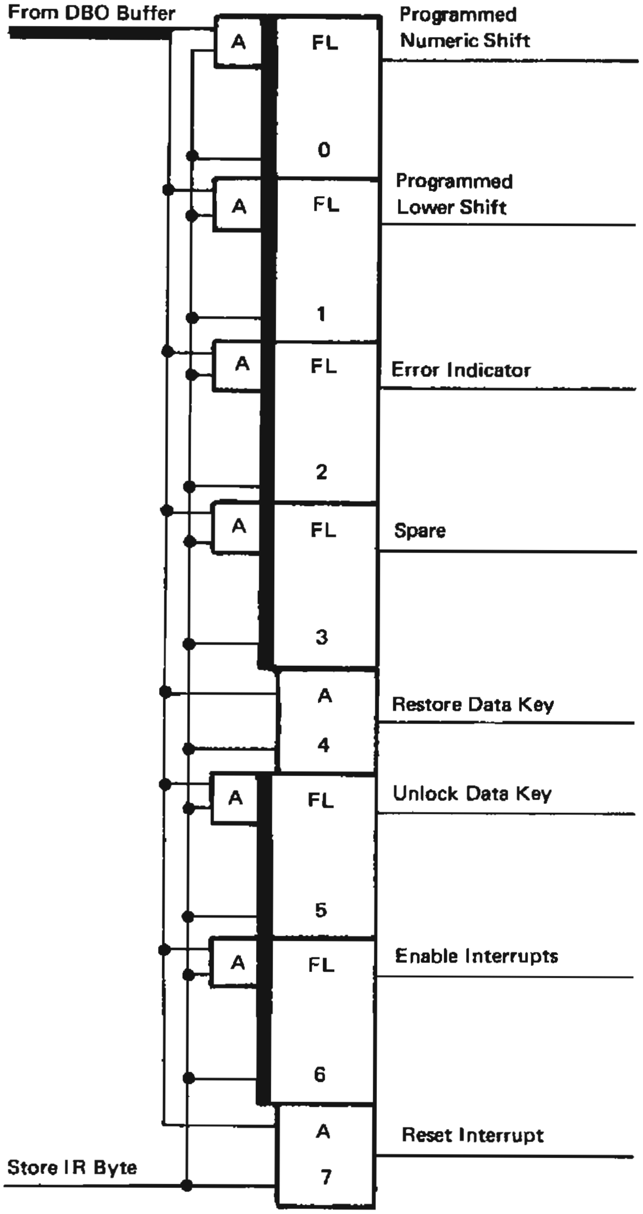
Refer to FEMD 4-20.

The CIB has 16 flip latches (Figure 2-3); 14 are used for the column indicator, and 2 for the program indicators.

The first byte addressed by a LIO instruction is loaded into the units position of the CIB when the 'store LIO 1st byte' line is active. The second byte addressed by a LIO instruction (first byte address minus 1) is loaded into the tens position of the CIB when the 'store LIO 2nd byte' line is active. Any latches without data present at their inputs are reset at this time if they were set on by a previous LIO instruction.

CONTROL CODE BUFFER

An SIO instruction accepted by the attachment loads the control code data into the control code buffer which consists of 6 latches. This data is used to control various keyboard functions as indicated in Figure 2-4.



Note: Store IR byte is active during CPU clock 6 time.

Figure 2-4. Control Code Buffer

Circuit Objectives

Refer to FEMD 5-15.

Control code data is loaded into the control code buffer when the 'store IR byte' line is active. All latches with data present at their inputs are turned on at this time. Any latch set by a previous SIO with no data present at its input is reset at this time.

DATA BUS IN ASSEMBLER (DBI)

The DBI assembler decodes and stores data generated by the data keys, function keys, and toggle switches. This data is gated out of the DBI assembler during a SNS instruction to the CPU. The CPU checks this data to determine which key or switch was operated.

Circuit Objectives

Refer to FEMD 4-25.

Data is stored in 8 flip latches in the DBI assembler. Keyboard switches and keys activate the input to the DBI latches. At clock 1 time of an EB1 and EB2 cycle during an SNS instruction, a sense line ANDs with the line activated by the keyboard setting the sense latches. The output of the latches is sent to the CPU on data bus in. The output of the DBI assembler latches are exclusive ORed determining if a parity bit was generated. At clock 5 time 'reset DBI buffer' is activated to reset the DBI assembler latches.

SAMPLING PULSE GENERATOR

The sampling pulse generator converts the channel oscillator pulses into keyboard A and keyboard B time pulses. These pulses test sample the lines from the keyboard that cause interrupts (function keys, data keys, and toggle switches). When the keys or switches are operated, if there is no contact bounce from keyboard A time to keyboard B time, the attachment logic generates an interrupt request. This eliminates the possibility of extraneous noise generating interrupt requests (Figure 2-5).

Circuit Objectives

Refer to FEMD 4-35.

The 160 ns channel pulse is converted into a 6.4 us. pulse by 6 binary flip flop triggers in the attachment. The 6.4 us. pulse is converted into 'kbd A time' and 'kbd B time' by 9 more binary flip flop triggers. The pulses are 5.12 us. in duration. The keyboard B pulse becomes active 1.65 ms after the keyboard A pulse becomes active (Figure 2-6).

PARITY CHECK

The parity check circuit has 8 exclusive OR circuits that check for odd parity in the DBO buffer.

Circuit Objectives

Refer to FEMD 5-15, and FEMD 4-30.

The parity is checked at 'CPU clock 5' time when the data bus out bits are being loaded into the DBO buffer.

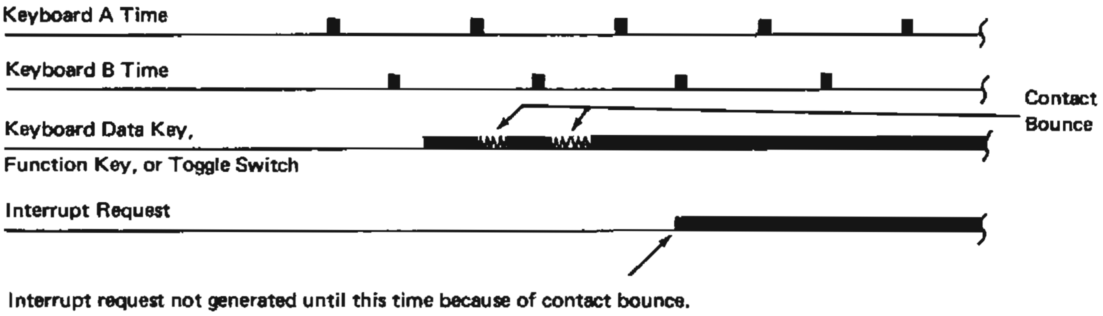

Keyboard A Time
Keyboard B Time
Keyboard Data Key,
Function Key, or Toggle Switch
Contact Bounce
Interrupt Request
Interrupt request not generated until this time because of contact bounce.

Figure 2-5. Keyboard Contact Sampling

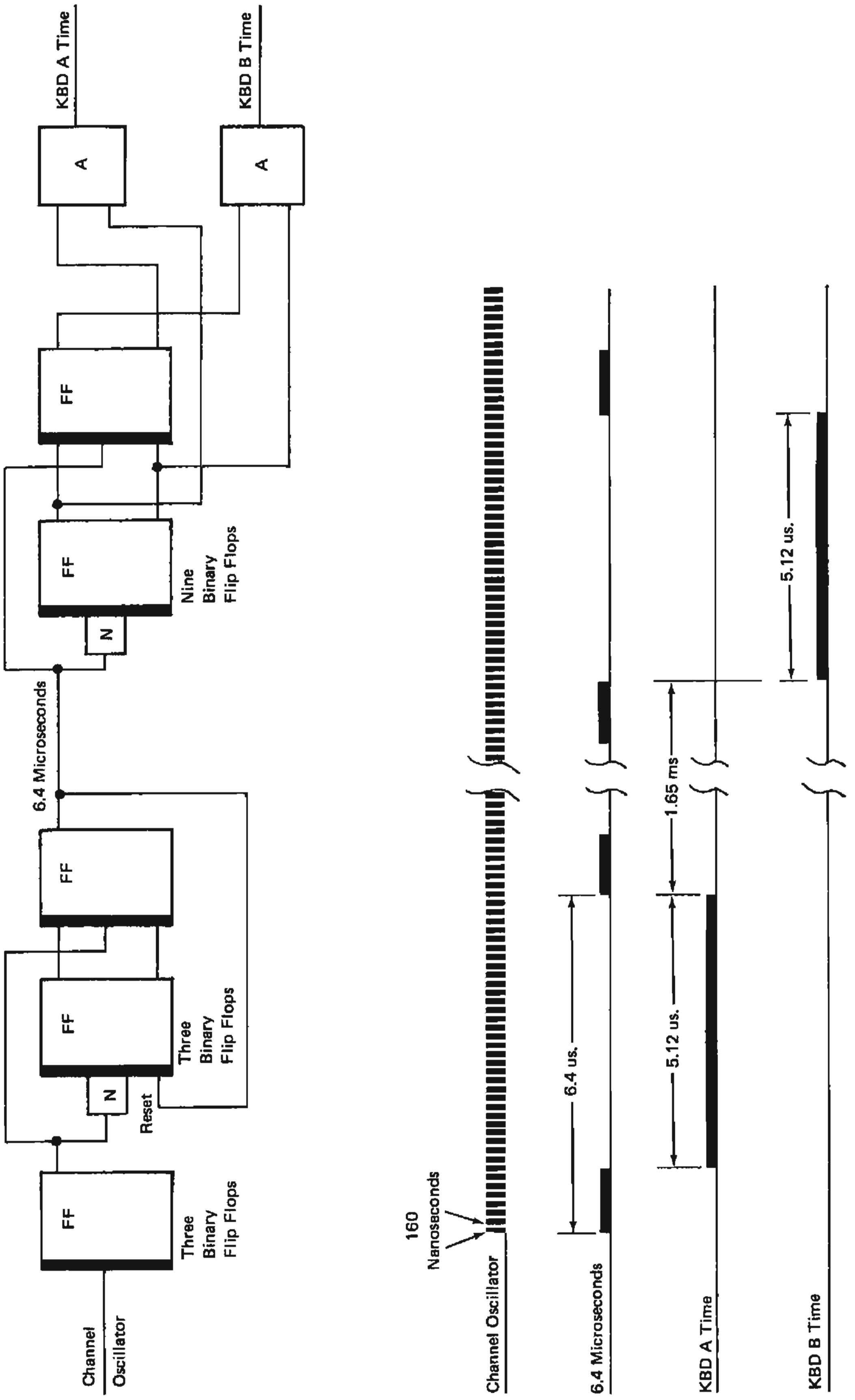


Figure 2-6. Sampling Pulse Generator

Chapter 3. Theory of Operation

This chapter describes the electrical operation of the IBM 5475 Data Entry Keyboard Attachment. References are made to the FEMD's and all logic names used in the circuit descriptions appear as they do in the FEMD's.

SIO INSTRUCTION

SIO instruction is used to:

1. Control programmed numeric and lower shift modes.
2. Turn on the error indicator.
3. Restore the keyboard.
4. Unlock the keyboard.
5. Enable the keyboard for interrupt requests.
6. Reset interrupts.

The SIO instruction is made up of three bytes (Figure 3-1). The first byte is the op code (hex F3). The second byte contains the device address (bit 3 on for the keyboard) and the M and N fields (must be zero for the keyboard). The third byte contains the control code which provides control information for the keys and indicators.

The 'SIO instr' tag line informs all attachments that this instruction will perform a SIO. The first keyboard attachment cycle is an I-Q cycle. During this cycle the device address is decoded and the M and N fields are checked for all zeros. The condition of the attachment (I/O condition B, I/O condition A) is also determined during this cycle and returned to the CPU.

During the I-R cycle, the control code is loaded into the attachment control code buffer. The bits of the control code perform various functions as shown in Figure 3-1.

The keyboard is disabled until the CPU issues a SIO with control code bits 4, 5, and 6 active. This restores and unlocks the data keys allowing the keyboard to generate an interrupt.

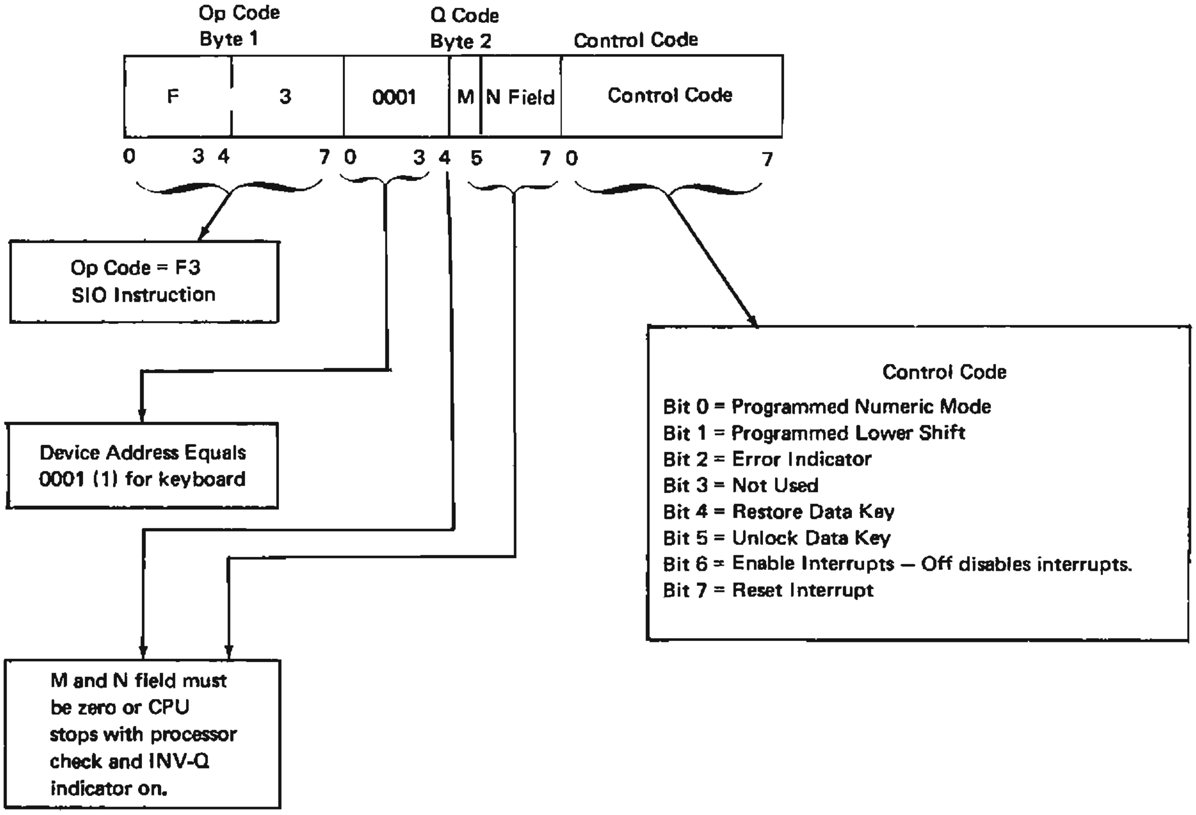
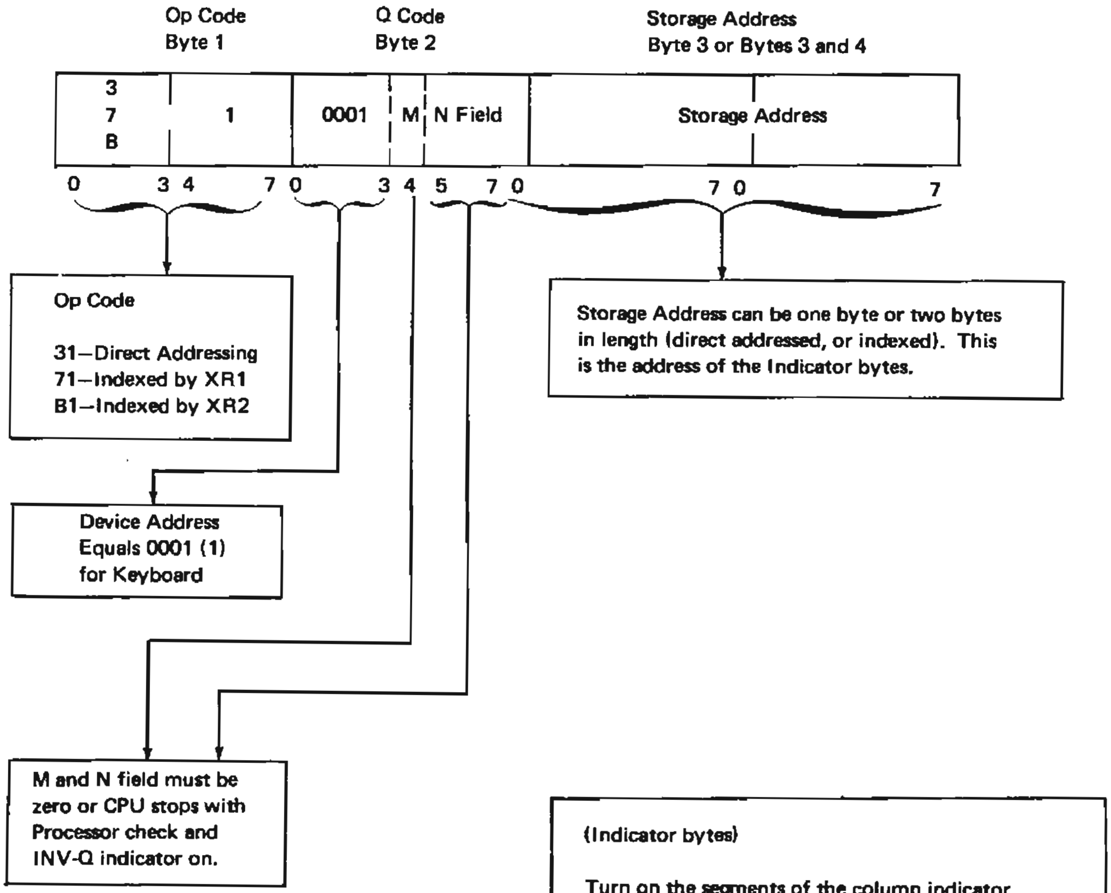


Figure 3-1. SIO Instruction Format


Op Code
Byte 1
Q Code
Byte 2
Storage Address
Byte 3 or Bytes 3 and 4
3
7
B
1
0001
M
N Field
Storage Address
0 3 4 7 0 3 4 5 7 0 7 0 7
Op Code
31—Direct Addressing
71—Indexed by XR1
B1—Indexed by XR2
Storage Address can be one byte or two bytes in length (direct addressed, or indexed). This is the address of the Indicator bytes.
Device Address Equals 0001 (1) for Keyboard
M and N field must be zero or CPU stops with Processor check and INV-Q indicator on.

(Indicator bytes)

Turn on the segments of the column indicator and the program 1 and 2 indicators (Figure 1-7).

Byte 1 Units Indicator

Bit 0 = Segment 1
Bit 1 = Segment 2
Bit 2 = Segment 3
Bit 3 = Segment 4
Bit 4 = Segment 5
Bit 5 = Segment 6
Bit 6 = Segment 7
Bit 7 = Program 2 Indicator

EB 1 cycle
High CPU Address

Byte 2 Tens Indicator

Bit 0 = Segment 1
Bit 1 = Segment 2
Bit 2 = Segment 3
Bit 3 = Segment 4
Bit 4 = Segment 5
Bit 5 = Segment 6
Bit 6 = Segment 7
Bit 7 = Program 1 Indicator

EB 2 cycle
Low CPU Address

Figure 3-2. LIO Instruction Format

Parity and Error Conditions

Odd parity must be maintained in the SIO instruction. If a parity error is detected by the attachment circuitry, a processor check stop occurs and the console lights indicate a DBO parity in the CPU.

FEMD 5-10 contains the circuit description.

LIO INSTRUCTION

The LIO instruction is used to control the state of segments of the column indicator program 1 indicator and program 2 indicator. The instruction is composed of 3 bytes if the op code indicates indexing, or 4 bytes if the op code indicates direct addressing (Figure 3-2). The first byte is the op code. The second byte contains the device address (hex 1 for the keyboard) and the M and N fields (must be zero). If the M and N fields are not zero, a CPU processor check occurs and INV-Q indicator comes on. The third byte (or third and fourth bytes) contain the storage address of the indicator bytes.

During the I-Q cycle, the Q code of the LIO instruction is loaded into the DBO buffer in the attachment. The Q code is decoded for the keyboard address (hex 1) and parity (correct parity is odd). If the attachment decodes its address and the parity is correct, the CPU proceeds with the next phase of the instruction.

The E-B1 cycle loads the units position of the column indicator. During the E-B2 cycle, the tens position of the column indicator is loaded. An LIO instruction is issued to the attachment whenever the column or program indicators need to be changed.

Storage Address

The storage address portion of the instruction contains the CPU storage address of the two column indicator/program indicator bytes. The first byte from storage provides the input to light the units position of the column indicator. Bit 7 of the first byte lights the program 2 indicator. The second byte provides the inputs for the tens position of the column indicator and bit 7 lights the program 1 indicator (Figure 3-3).

Internal CPU cycles (I-H1, I-L1 for direct addressing and I-X1 for indexing) transfer the desired storage address to the B address register. Then, EB cycles transfer data to the keyboard indicators.

Refer to FEMD 5-040.

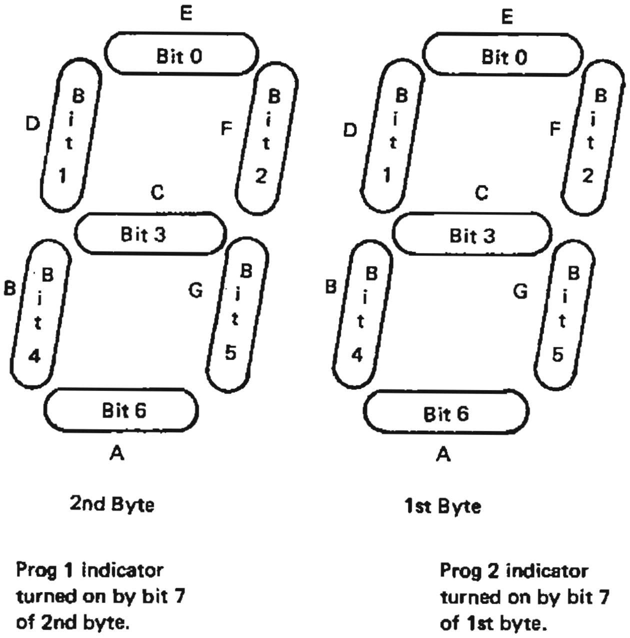


Figure 3-3. Column Indicator Segments and Program Indicators

SNS INSTRUCTION

The SNS instruction is composed of 3 bytes if the op code indicates indexing, or 4 bytes if the op code indicates direct addressing (Figure 3-4). The first byte is the op code. The second byte contains the device address (hex 1 for the keyboard and the M and N fields (M field must be zero). The N field determines what two sense bytes are stored. The third byte (or third and fourth bytes) contains the storage address where the sense bytes are stored.

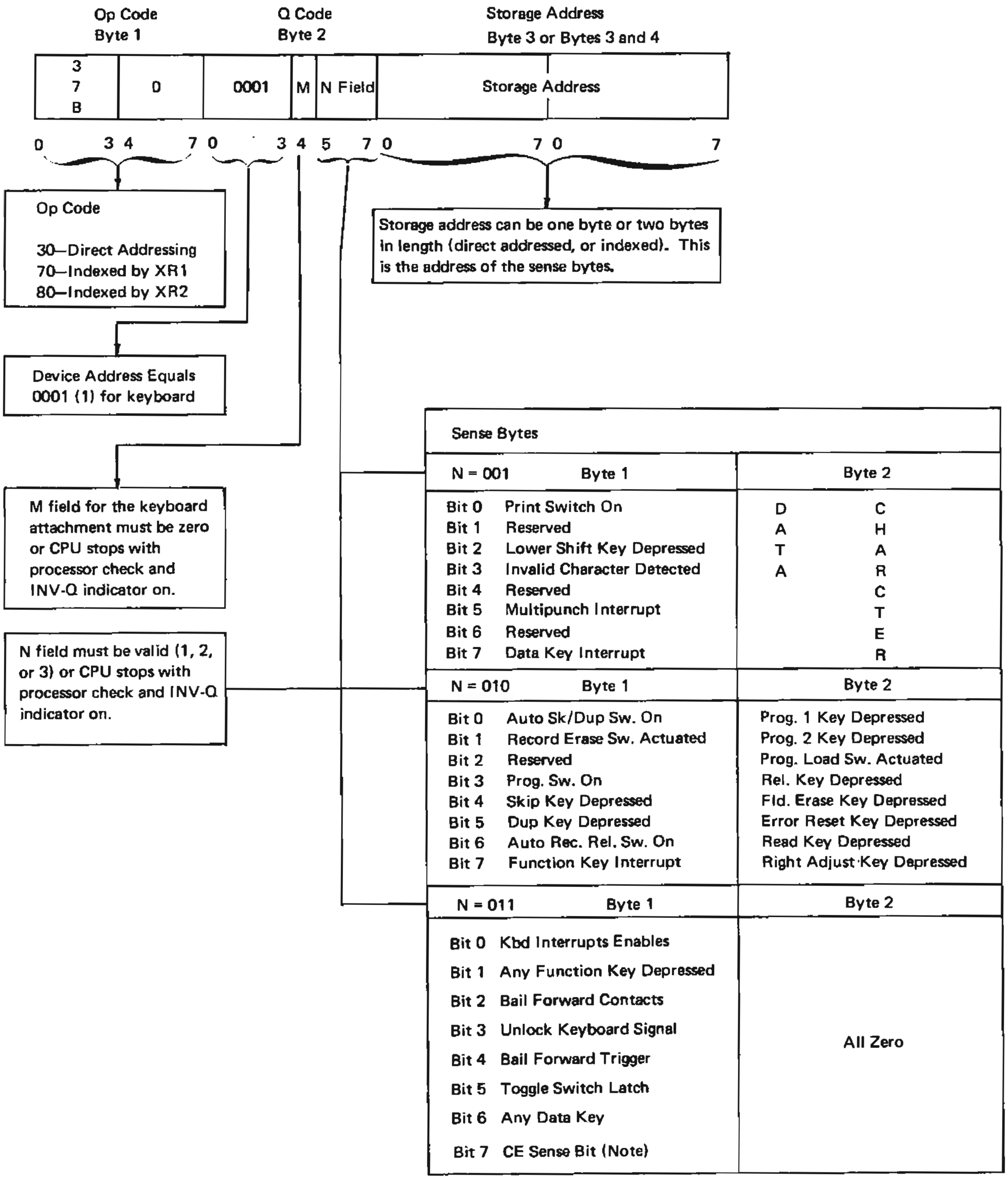
During the I-Q cycle of the SNS instruction, the Q byte is loaded into the DBO buffer in the attachment. The Q byte is decoded for the device address of the keyboard (hex 1) and the DBO buffer is parity checked. The N field is decoded to determine which sense bytes are transferred.

Internal CPU cycles (I-H1, I-L1 for direct addressing, and I-X1 for indexing) transfer the desired storage address to the B address register. Then, EB cycles transfer sense data to CPU storage.

The E-B cycles of the SNS instruction send the sense information as specified by the N field to the CPU. Refer to Figures 3-4 for the N field configurations.

An SNS instruction is issued to the attachment when an interrupt request is generated. The CPU checks the sense bytes to determine the cause of the interrupt. If the interrupt was caused by a data key, the CPU uses the data sense byte and the main program in the CPU completes the operation. Figure 3-5 is an example of how an SNS instruction is used.

Refer to FEMD 5-025.


Op Code
Byte 1
Q Code
Byte 2
Storage Address
Byte 3 or Bytes 3 and 4
3
7
B
0
0001
M
N Field
Storage Address
0 3 4 7 0 3 4 5 7 0 7 0 7
Op Code
30—Direct Addressing
70—Indexed by XR1
80—Indexed by XR2
Device Address Equals
0001 (1) for keyboard
M field for the keyboard attachment must be zero or CPU stops with processor check and INV-Q indicator on.
N field must be valid (1, 2, or 3) or CPU stops with processor check and INV-Q indicator on.
Storage address can be one byte or two bytes in length (direct addressed, or indexed). This is the address of the sense bytes.

Sense Bytes

N = 001	Byte 1	Byte 2
Bit 0	Print Switch On	D C
Bit 1	Reserved	A H
Bit 2	Lower Shift Key Depressed	T A
Bit 3	Invalid Character Detected	A R
Bit 4	Reserved	C
Bit 5	Multipunch Interrupt	T
Bit 6	Reserved	E
Bit 7	Data Key Interrupt	R
N = 010	**Byte 1**	**Byte 2**
Bit 0	Auto Sk/Dup Sw. On	Prog. 1 Key Depressed
Bit 1	Record Erase Sw. Actuated	Prog. 2 Key Depressed
Bit 2	Reserved	Prog. Load Sw. Actuated
Bit 3	Prog. Sw. On	Rel. Key Depressed
Bit 4	Skip Key Depressed	Fld. Erase Key Depressed
Bit 5	Dup Key Depressed	Error Reset Key Depressed
Bit 6	Auto Rec. Rel. Sw. On	Read Key Depressed
Bit 7	Function Key Interrupt	Right Adjust Key Depressed
N = 011	**Byte 1**	**Byte 2**
Bit 0	Kbd Interrupts Enables	All Zero
Bit 1	Any Function Key Depressed	
Bit 2	Bail Forward Contacts	
Bit 3	Unlock Keyboard Signal	
Bit 4	Bail Forward Trigger	
Bit 5	Toggle Switch Latch	
Bit 6	Any Data Key	
Bit 7	CE Sense Bit (Note)	

Note: The presence of the "CE Sense Bit" indicates that any signal which is jumpered to pin A-B2M2P03 is at the MST down level. If this pin is left floating, the bit will be on

Figure 3-4. SNS Instruction Format

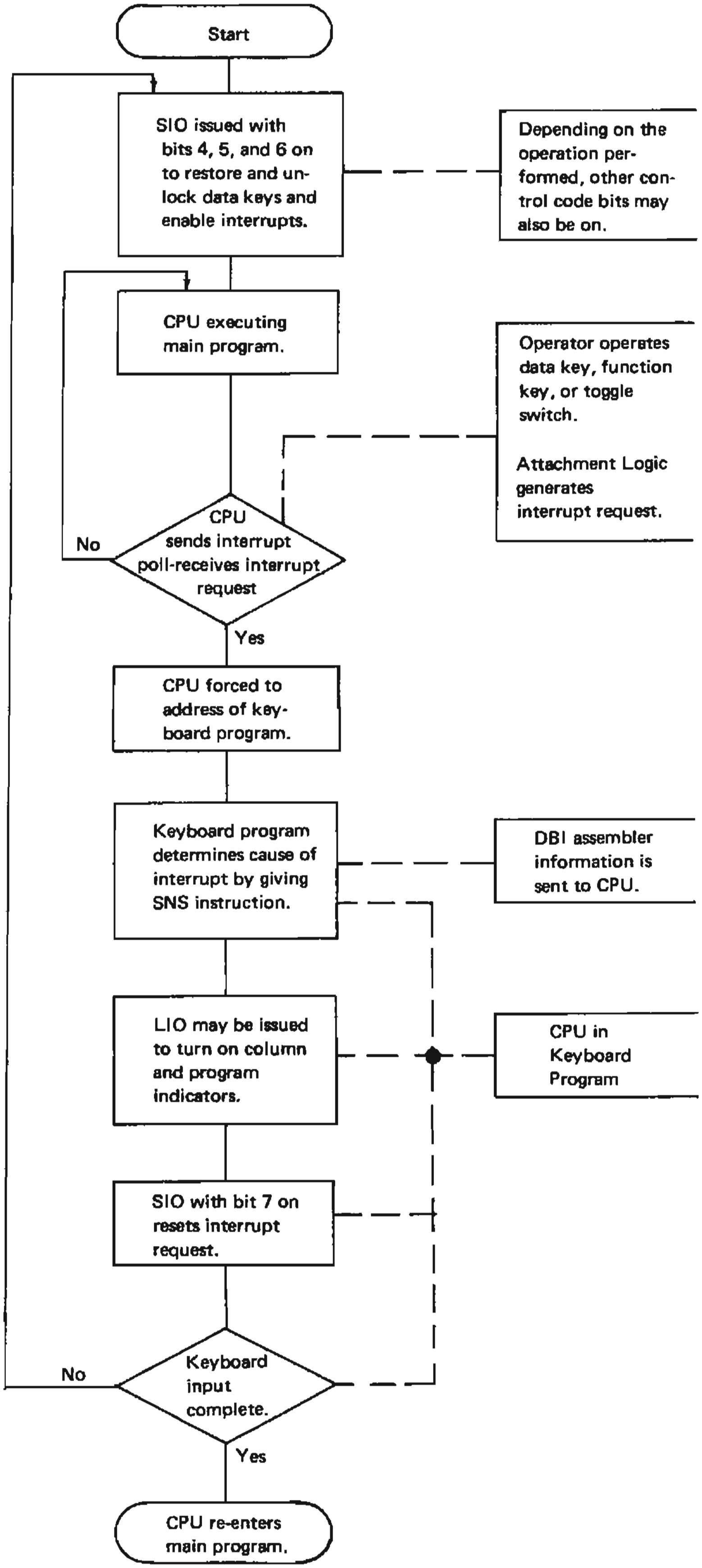

Start
SIO issued with bits 4, 5, and 6 on to restore and unlock data keys and enable interrupts.
Depending on the operation performed, other control code bits may also be on.
CPU executing main program.
Operator operates data key, function key, or toggle switch.
Attachment Logic generates interrupt request.
No
CPU sends interrupt poll-receives interrupt request
Yes
CPU forced to address of keyboard program.
Keyboard program determines cause of interrupt by giving SNS instruction.
DBI assembler information is sent to CPU.
LIO may be issued to turn on column and program indicators.
CPU in Keyboard Program
SIO with bit 7 on resets interrupt request.
No
Keyboard input complete.
Yes
CPU re-enters main program.

Figure 3-5. Keyboard Operation

DATA KEY OPERATION

Before a data key operation can occur, the attachment must receive an SIO instruction that enables interrupts, restores and unlocks data keys. Information keyed in by the data keys is stored in the data key buffer. Output of the data key buffer is sent to the DBI assembler. When interrupt level one has priority, the CPU grants an interrupt to the keyboard attachment. A SNS instruction issued to the attachment determines the cause of the interrupt. During the SNS instruction, the information stored in the data key buffer is sent to the CPU. The CPU issues a SIO instruction to the attachment, and then the keyboard is ready for operation.

Keyboard Shift

The shift of the keyboard determines the character generated when the data key is pressed. The shift is determined by four keyboard functions:

1. If the program switch is off, the keyboard is in lower shift.
2. If the program switch is on: a. the keyboard is in upper shift unless the program designates lower shift for the next entry. The stored program conditions the encoding logic for the lower shift entries through the SIO instruction. b. the program may also designate numeric mode for the next entry. In this case, the keyboard remains in upper shift. However, if a character other than 0 through 9 or blank is keyed, an invalid character SNS bit is generated. The stored program conditions the encoding logic for numeric mode entries through the SIO instruction. If the SIO control code designates both programmed numeric mode, the numeric mode overrides.
3. Any of the above shift conditions can be manually overridden by holding the shift keys or the multi-punch key down for the duration required.

Data Key Restoring

Once a data key is pressed, all other data keys are mechanically locked. Restoring the data keys is controlled by the program through the SIO instruction. One bit in the SIO control code causes the pressed key to be restored, but leaves all the data keys locked. Another SIO control code bit unlocks the keys. If a SIO control code has both bits on, a complete restore cycle is taken.

Caution
All data keys will be locked if an SIO instruction initiates a complete restore cycle and another SIO instruction (without the unlock keys control code bit) is issued before the pressed key is restored (about 15 to 20 ms).

To allow a burst rate of 1500 key strokes per minute, the SIO instruction, which restores the keyboard, must be issued within 10 ms after the start of the interrupt request, generated by the pressed data key.

Refer to FEMD 5-60.

FUNCTION KEY AND TOGGLE SWITCH OPERATION

Before a function key or toggle switch operation, a SIO instruction must be received by the attachment to enable the keys, switches, and interrupts.

Information generated by activating a function key or toggle switch conditions the input to the DBI assembler. When interrupt level one has priority, the CPU grants an interrupt to the keyboard attachment. A SNS instruction issued to the attachment determines the cause of the interrupt. During a SNS instruction, the information in the DBI assembler is taken to the CPU. The CPU then issues a SIO instruction to the attachment to make the keyboard operational again.

When an interrupting function key or toggle switch is activated, the data keys are mechanically locked and no other function key can generate an interrupt until the first key is released. However, if more than one function key is pressed when a SNS instruction is executed, the corresponding bits will be present. If the SNS instruction is not executed until after the operator has released the key, the corresponding bit will be missing.

Refer to FEMD 5-70 and 5-85.

MULTIPUNCH OPERATION

During a multipunch operation, an SIO instruction sent to the attachment enables interrupt. When the multipunch key is active (held):

1. All data characters keyed are punched in the same column.
2. The keyboard is in upper shift.
3. The data keys are restored without generating interrupt requests.
4. If a data key was activated, an interrupt request is generated when the multipunch key is de-activated.

The multipunch operation is the same as the data key operation except the interrupt is taken after the multipunch key is de-activated. If no data is keyed in when the multipunch key is active, an interrupt is not taken.

Refer to FEMD 5-95.

Chapter 4. Features

There are no special features.

Chapter 5. Power Supplies and Controls

The IBM 5475 Data Entry Keyboard Attachment receives all of its logic voltages from the 5410 CPU. These voltages are:

1. -4 vdc.
2. +6 vdc to convert from SLD logic to MST logic.
3. Ground.

Chapter 6. Console and Maintenance Features

This chapter is not applicable.

Appendix A. Unit Characteristics

For machine characteristics, refer to the *IBM System/3 Installation Manual–Physical Planning,* Form A21-9084.

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SY31-0247-0

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