IBM Field Engineering

Maintenance Diagrams

5424 Multi-Function Card Unit Attachment

SY31-0254-1

Preface

The diagrams in this manual are organized by operation. Thus, the details of machine operations are presented in operational flowcharts, most of which are *two-level*. The general flow path of the two-level charts (heavy line) shows the major objectives of an operation or instruction. Detailed flow paths of major objectives are located to the right of the general flow path.

Positive-logic diagrams support the operational flowcharts. They show logical circuit operation without regard to signal levels. Most of the logic diagrams in this manual are not block-for-block representations of Automated Logic Diagrams. Rather, only blocks necessary for a logical understanding of the operation are shown.

A knowledge of MFCU operations and CPU operations is necessary to understand MFCU attachment operations.

Other manuals needed to understand and service the 5424 MFCU attachment are:

1. The *IBM 5424 MFCU Attachment, Field Engineering Theory of Operations Manual*, SY31-0253.
2. The *IBM 5424 MFCU, Field Engineering Theory of Operations Manual*, SY31-0213.
3. The *IBM 5424 MFCU, Field Engineering Maintenance Manual*, SY31-0230.
4. The *IBM 5410 Central Processing Unit, Field Engineering Theory of Operations Manual*, SY31-0207.
5. The *IBM 5410 Central Processing Unit, Field Engineering Maintenance Diagrams Manual*, SY31-0202.
6. The *IBM 5410 Central Processing Unit, Field Engineering Maintenance Manual*, SY31-0244.

Second Edition (Feburary 1971)

This is a major revision of, and obsoletes, SY31-0254-0.

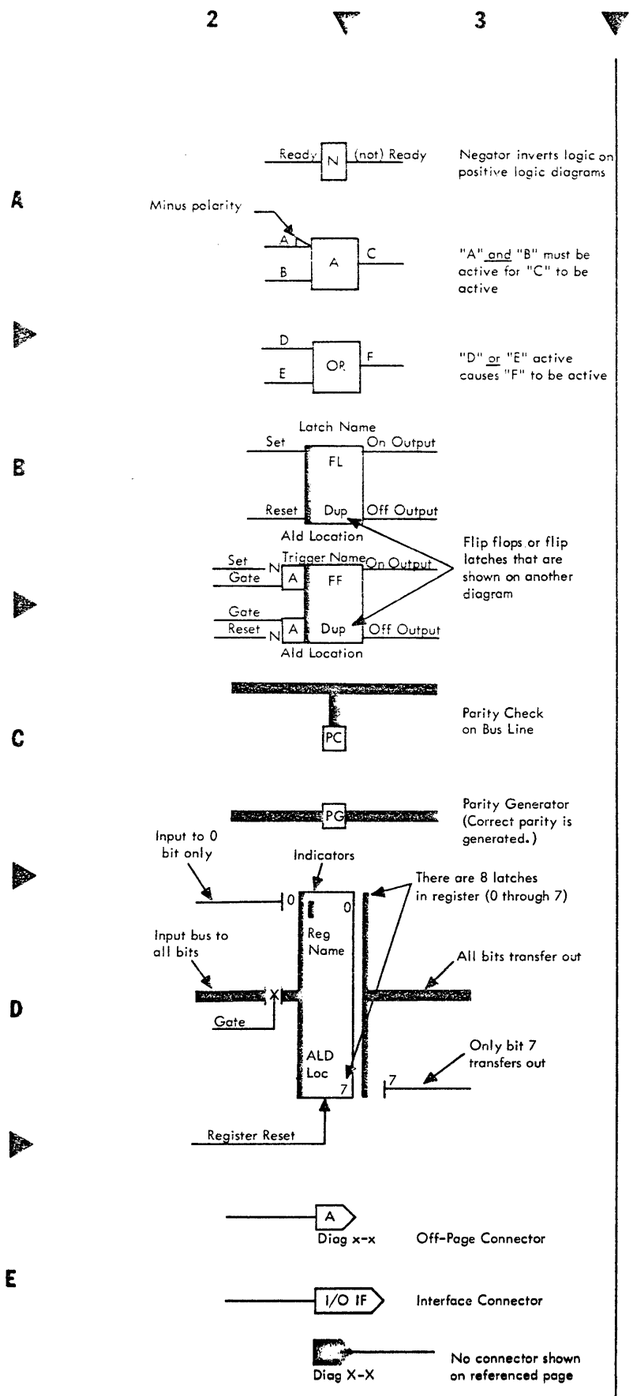
Changes are continually made to the specifications herein; any such change will be reported in subsequent revisions or Technical Newsletters.

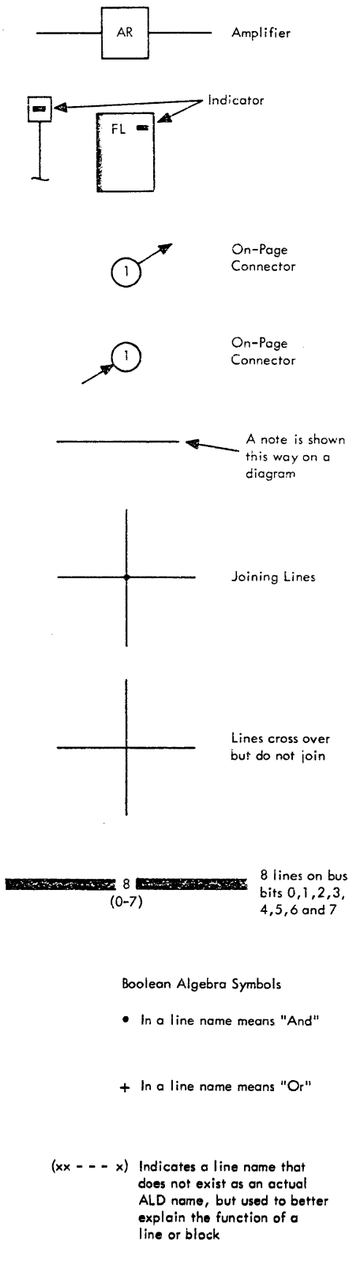
A form for reader's comments is provided at the back of this publication. If the form has been removed, comments may be addressed to IBM Corporation, Product Publications, Department 245, Rochester, Minnesota 55901.

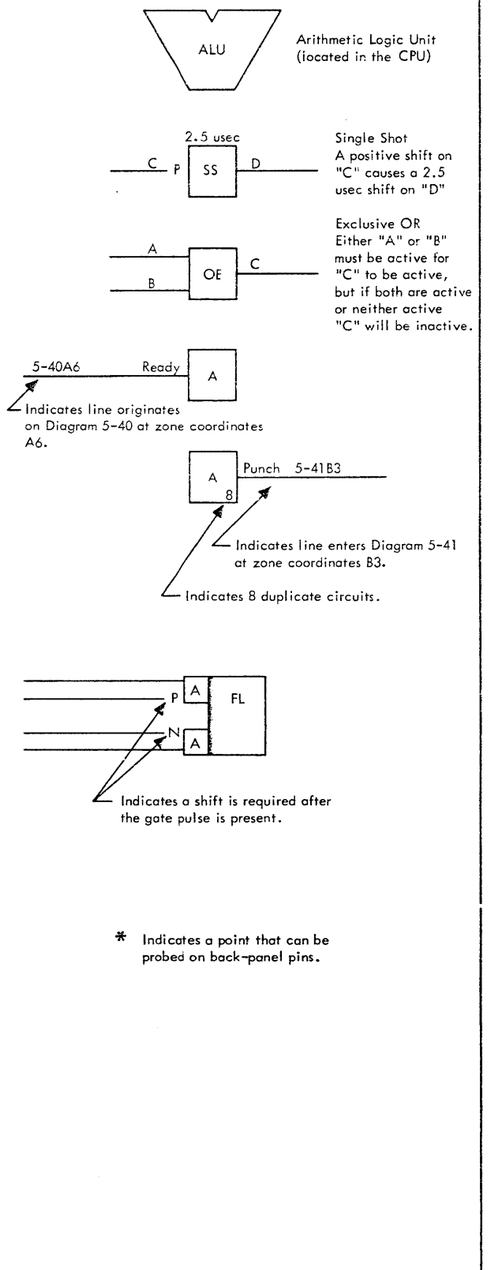
Abbreviations

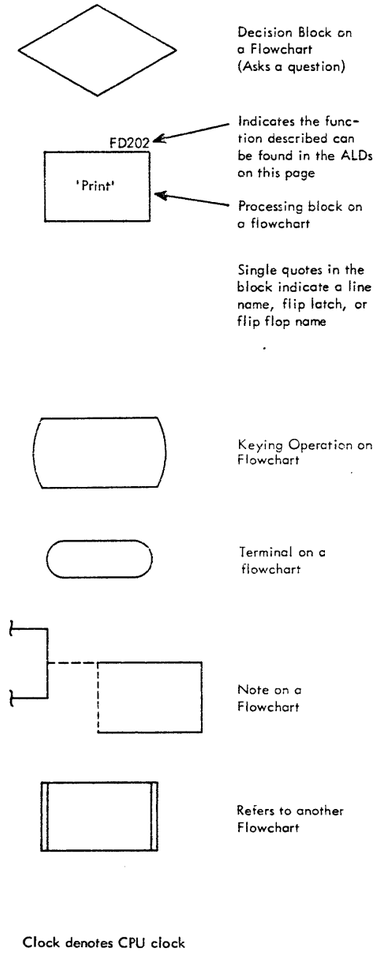
ALD	Automated Logic Diagram
ALU	Arithmetic and Logical Unit
APL	Advance Program Level
CPU	Central Processing Unit
CS	Cycle Steal
CSR	Cycle Steal Request
DA	Device Address
DBI	Data Bus In
DBO	Data Bus Out
EBCDIC	Extended Binary Coded Decimal Interchange Code
FEMD	Field Engineering Maintenance Diagrams
I-O	Input-Output (I/O)
IPL	Initial Program Load
LIO	Load Input-Output
LSR	Local Store Register
MAP	Maintenance Analysis Procedure
MFCU	Multi-Function Card Unit
MPCAR	MFCU Punch Data Address Register
MPTAR	MFCU Print Data Address Register
MRDAR	MFCU Read Data Address Register
MST	Monolithic System Technology
NPRO	Non-Process Run Out
PC	Parity Check
PG	Parity Generate
POR	Power on Reset
SAR	Storage Address Register
SIO	Start Input-Output
SIOC	Serial I/O Channel
SLD	Solid Logic Dense
SNS	Sense Input-Output
SS	Single Shot
TIO	Test Input-Output and Branch
XR	Index Register

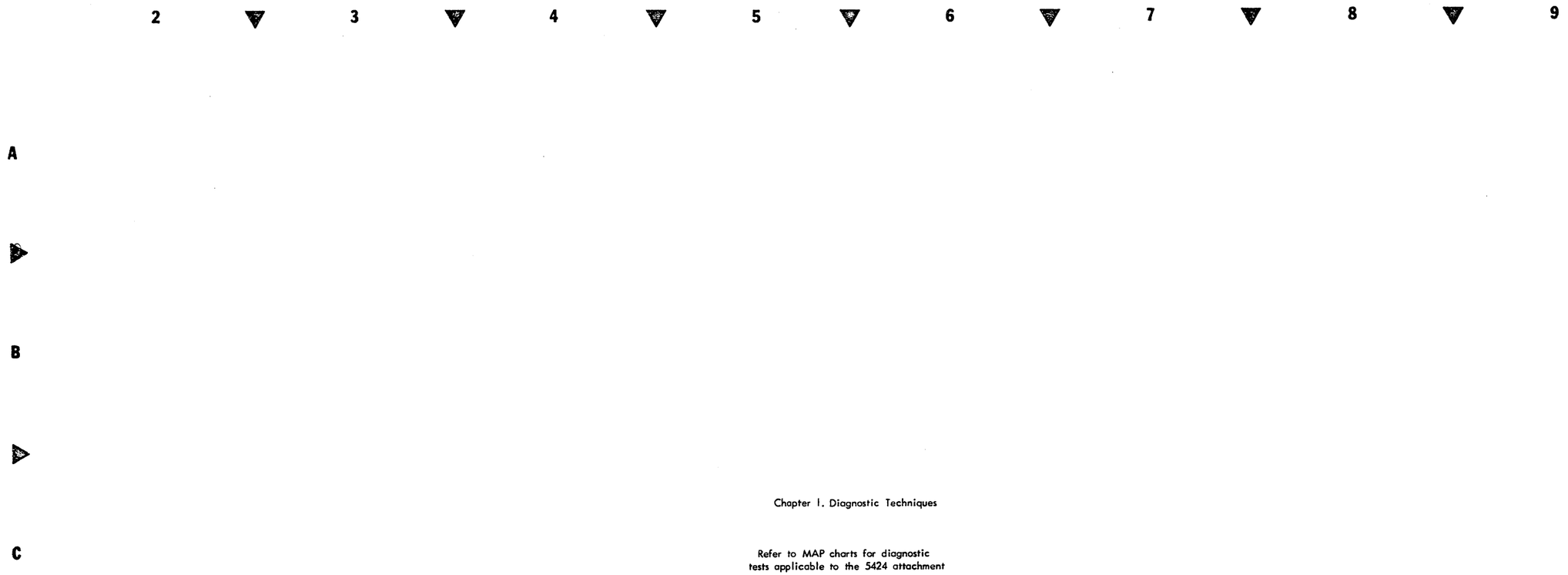
Contents


2
3
4
5
6
7
8
9
A
B
C
D
E
Ready
N
(not) Ready
Negator inverts logic on positive logic diagrams
Minus polarity
A
B
C
"A" and "B" must be active for "C" to be active
D
E
OR
F
"D" or "E" active causes "F" to be active
Latch Name
Set
On Output
FL
Reset
Dup
Off Output
Ald Location
Flip flops or flip latches that are shown on another diagram
Trigger Name
Gate
FF
PC
Parity Check on Bus Line
PG
Parity Generator (Correct parity is generated.)
Input to 0 bit only
Indicators
There are 8 latches in register (0 through 7)
Input bus to all bits
Reg Name
All bits transfer out
Gate
ALD Loc
Only bit 7 transfers out
Register Reset
Diag x-x
Off-Page Connector
I/O IF
Interface Connector
Diag X-X
No connector shown on referenced page


AR
Amplifier
Indicator
FL
On-Page Connector
A note is shown this way on a diagram
Joining Lines
Lines cross over but do not join
8
(0-7)
8 lines on bus bits 0,1,2,3, 4,5,6 and 7
Boolean Algebra Symbols
• In a line name means "And"
+ In a line name means "Or"
(xx - - - x) Indicates a line name that does not exist as an actual ALD name, but used to better explain the function of a line or block


ALU
Arithmetic Logic Unit (located in the CPU)
2.5 usec
C
P
SS
D
Single Shot
A positive shift on "C" causes a 2.5 usec shift on "D"
A
B
OE
C
Exclusive OR
Either "A" or "B" must be active for "C" to be active, but if both are active or neither active "C" will be inactive.
5-40A6
Ready
A
Indicates line originates on Diagram 5-40 at zone coordinates A6.
Punch 5-41B3
8
Indicates line enters Diagram 5-41 at zone coordinates B3.
Indicates 8 duplicate circuits.
P
N
FL
Indicates a shift is required after the gate pulse is present.
* Indicates a point that can be probed on back-panel pins.


Decision Block on a Flowchart (Asks a question)
FD202
'Print'
Indicates the function described can be found in the ALDs on this page
Processing block on a flowchart
Single quotes in the block indicate a line name, flip latch, or flip flop name
Keying Operation on Flowchart
Terminal on a flowchart
Note on a Flowchart
Refers to another Flowchart
Clock denotes CPU clock



Refer to MAP charts for diagnostic tests applicable to the 5424 attachment

Diagram 1-105. Diagnostic Techniques

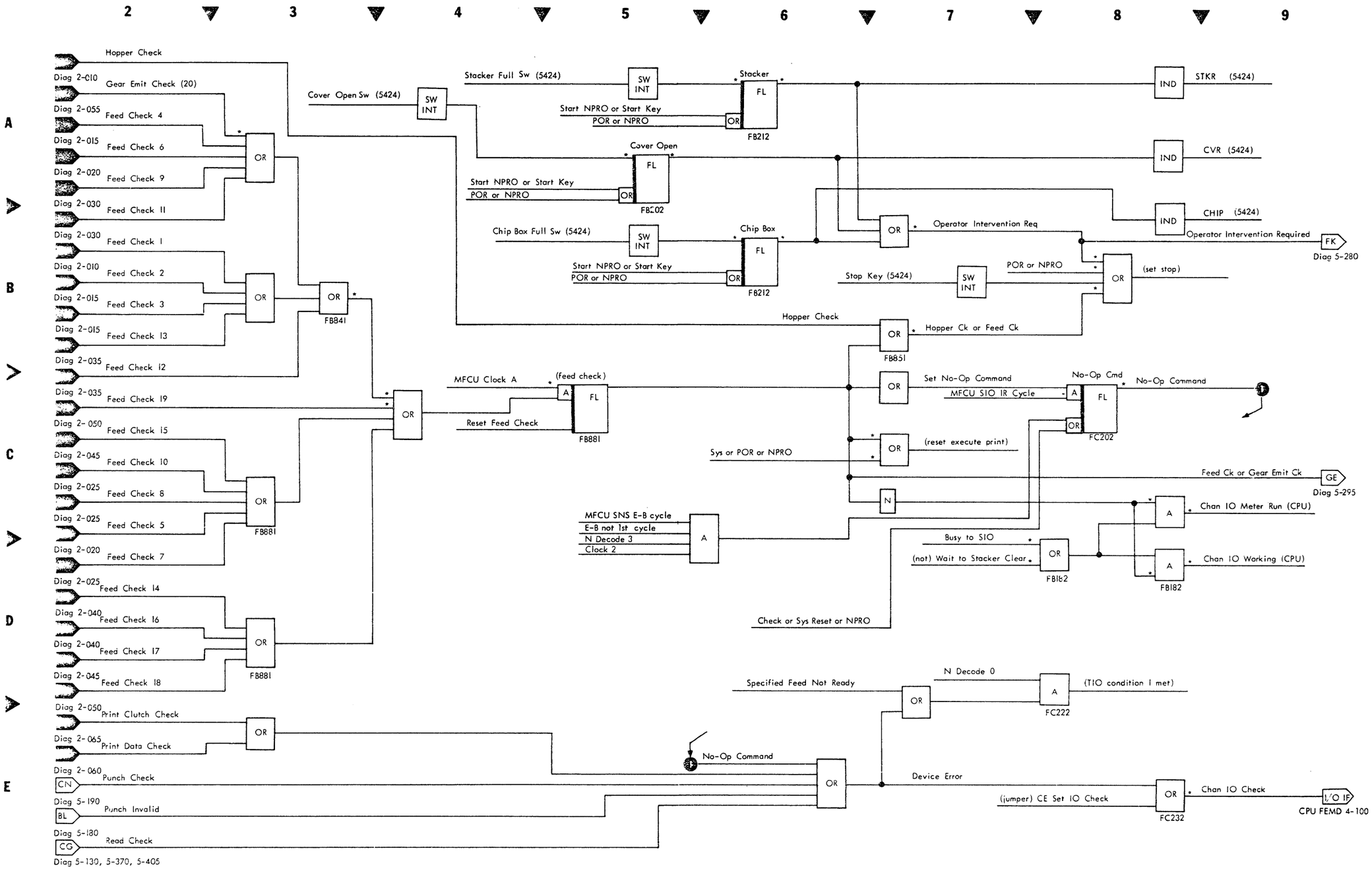
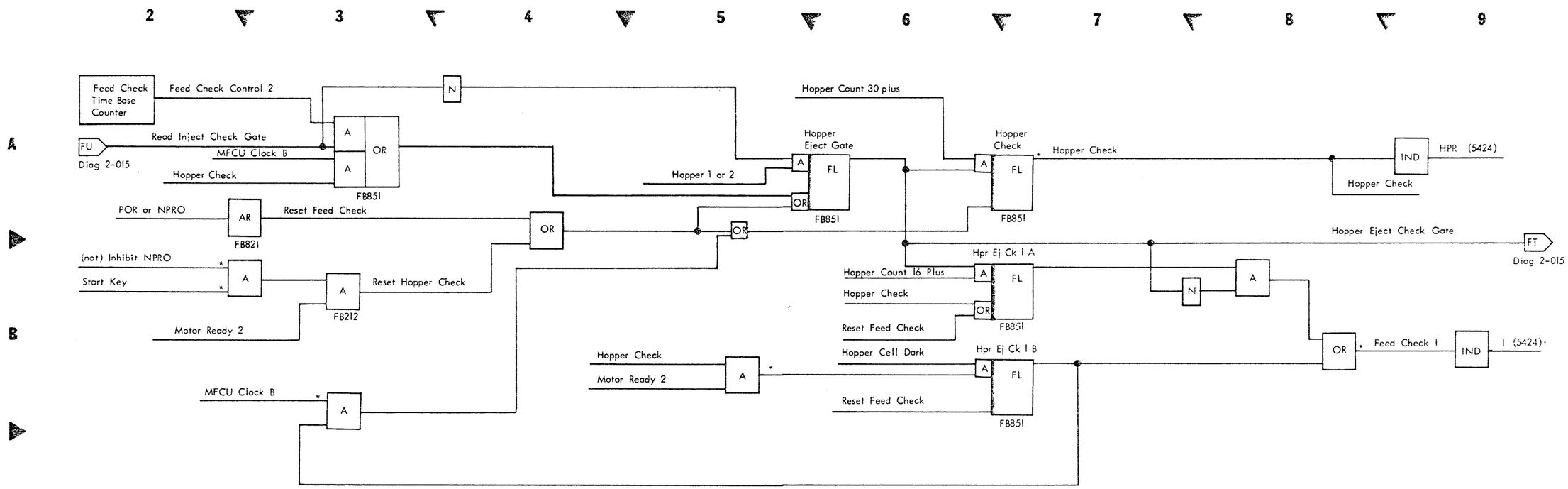
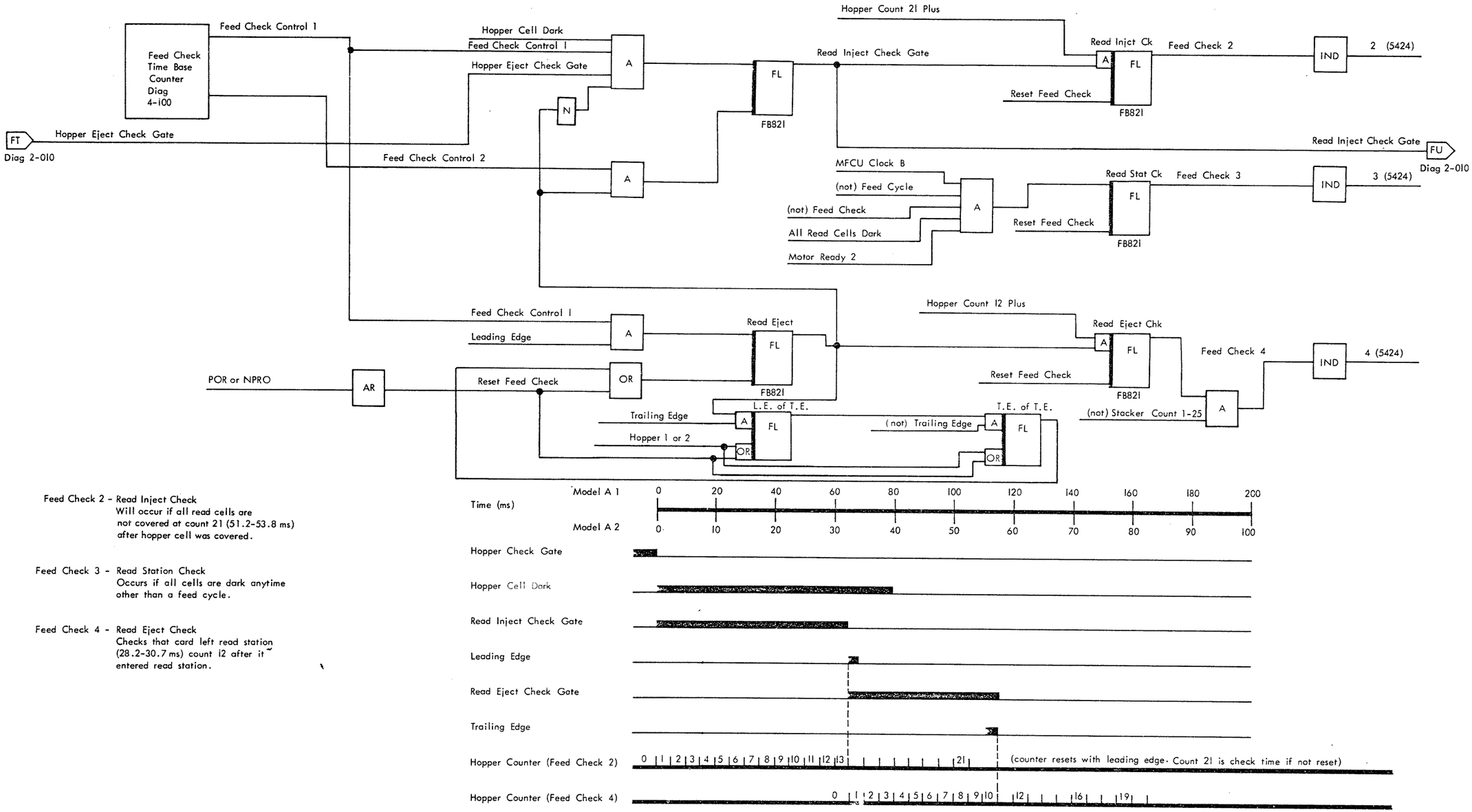


Diagram 2-005. MFCU Errors


2
3
4
5
6
7
8
9
A
B
C
D
E
Feed Check Time Base Counter
Feed Check Control 2
N
Hopper Count 30 plus
Read Inject Check Gate
FU
Diag 2-015
MFCU Clock B
Hopper Check
A
A
OR
FB851
Hopper Eject Gate
Hopper Check
Hopper 1 or 2
A
OR
FL
FB851
A
FL
FB851
Hopper Check
IND
HPR (5424)
Hopper Check
POR or NPRO
AR
FB821
Reset Feed Check
OR
OR
Hopper Eject Check Gate
FT
Diag 2-015
(not) Inhibit NPRO
Start Key
A
A
FB212
Reset Hopper Check
Motor Ready 2
Hpr Ej Ck 1 A
Hopper Count 16 Plus
Hopper Check
A
OR
FL
FB851
Reset Feed Check
N
A
OR
Feed Check 1
IND
1 (5424)
Hopper Check
Motor Ready 2
A
Hopper Cell Dark
Reset Feed Check
Hpr Ej Ck 1 B
A
FL
FB851
MFCU Clock B
A
1. Hopper Check - Hopper cell not covered by hopper count 30
2. Feed Check 1 - Hopper Eject Check
a. Hopper cell was not covered by count 16 (35.8-38.4 ms)
b. Card covered hopper cell after count 30
Time (ms)
Model A 1
0 20 40 60 80 100 120 140 160 180 200
Model A 2
0 10 20 30 40 50 60 70 80 90 100
Hopper 1 or 2
Hopper Cell Dark
Hopper Eject Check Gate
Read Inject Check Gate
Hopper Counter
0 1 2 3 4 5 6 7 8 9 16 30
(counter reset with hopper cell dark and starts counting again)
See feed checks 2 and 4



Feed Check 2 - Read Inject Check
Will occur if all read cells are not covered at count 21 (51.2-53.8 ms) after hopper cell was covered.

Feed Check 3 - Read Station Check
Occurs if all cells are dark anytime other than a feed cycle.

Feed Check 4 - Read Eject Check
Checks that card left read station (28.2-30.7 ms) count 12 after it entered read station.

Read Eject Check Gate must be reset prior to count 12.
Counter continues to run until count 19. Count 19 turns on 'End Feed Cycle' which then resets 'Card on Way to Wait'.
Counter resets with reset of 'Card on Way to Wait'.

Diagram 2-015. Feed Checks 2, 3, and 4

2 3 4 5 6 7 8 9

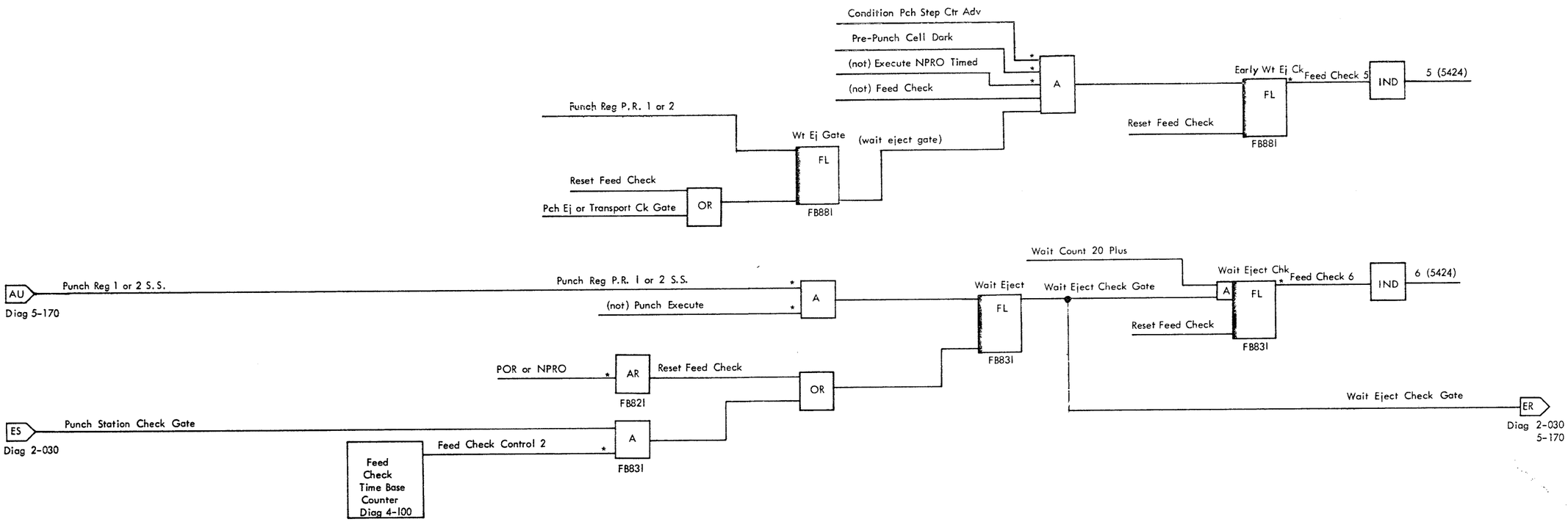
A

B

C

D

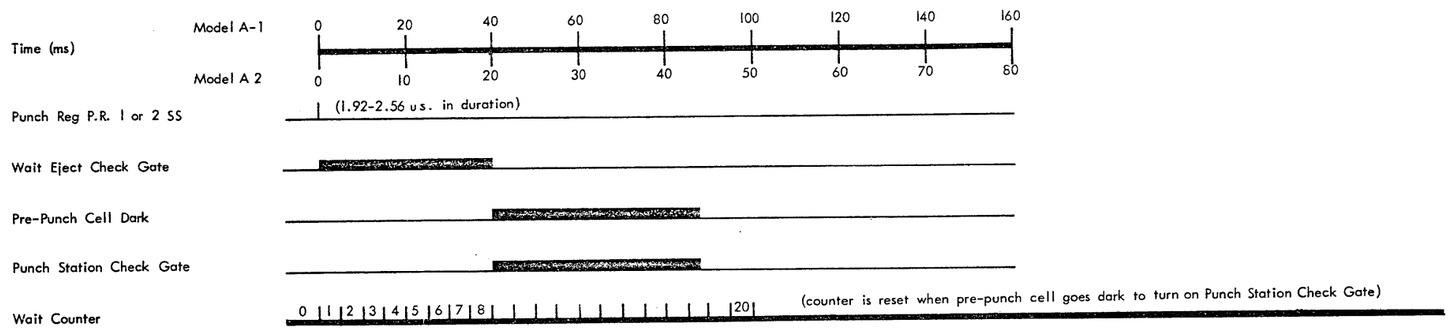
E

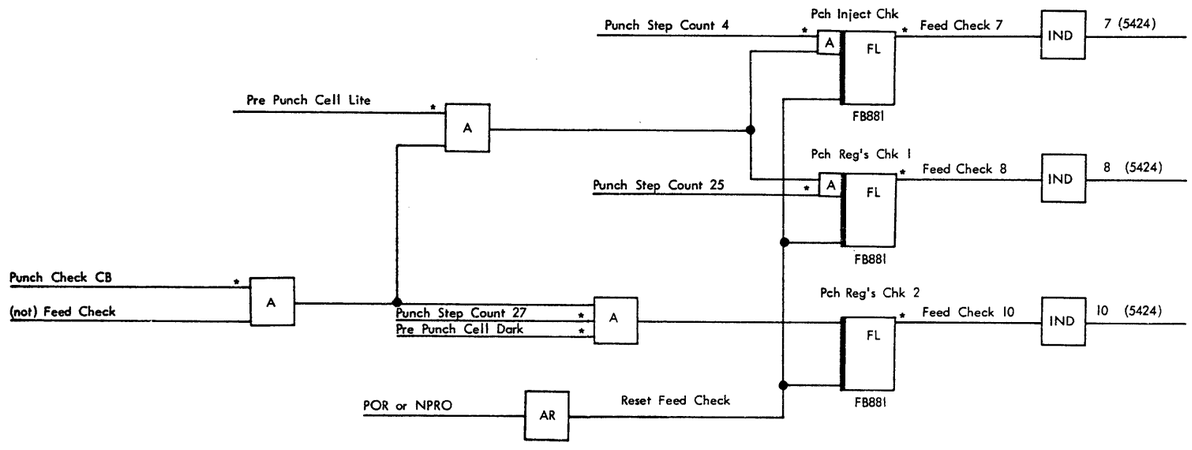


Feed Check 5 - Early Wait Eject Check
Checks that the card does not cover pre-punch cell unless the punch reg pressure roll has been energized.

Feed Check 6 - Wait Eject Check
Occurs if the pre-punch cell is not covered (48.6-51.2 ms-count 20) after the pick of pressure roll 1 or 2.

Note: No punch operation





Feed Check 7 - Punch Inject Check
Occurs if pre-punch cell is not covered by the card before punch step count 4. The card should be registered at the punch station by punch step count 4 (40 ms after reg pressure roll pick).
Note: Punch operation only

Feed Check 8 - Punch Registration Check 1
Checks that pre-punch cell is covered at stepper count 25 (≈292 ms-column 21)
Note: Punch operation only

Feed Check 10 - Punch Registration Check 2
Checks that pre-punch cell is exposed at stepper count 27 (≈316 ms-column 23)
Note: Punch operation only

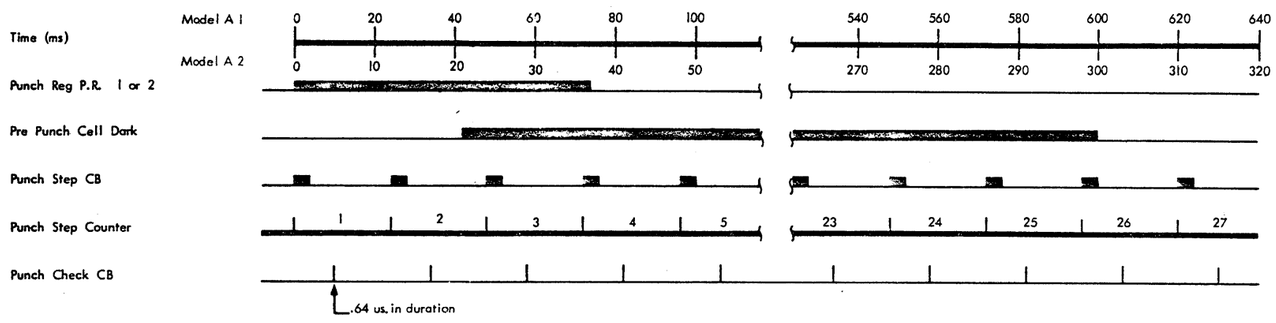
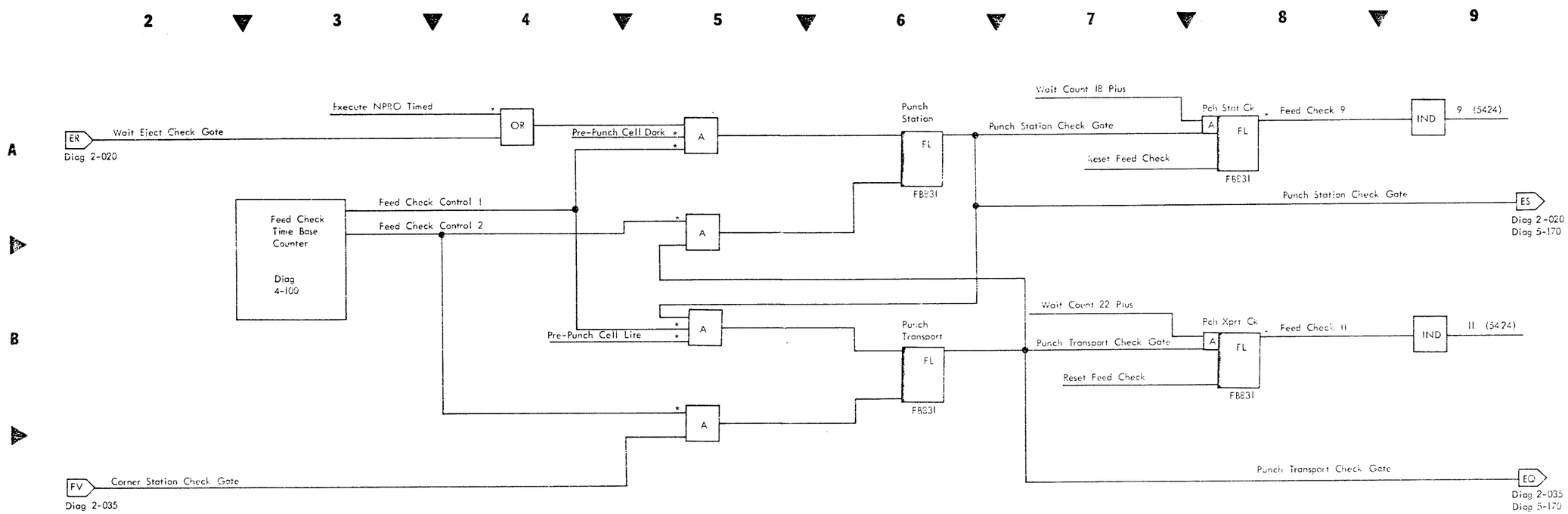
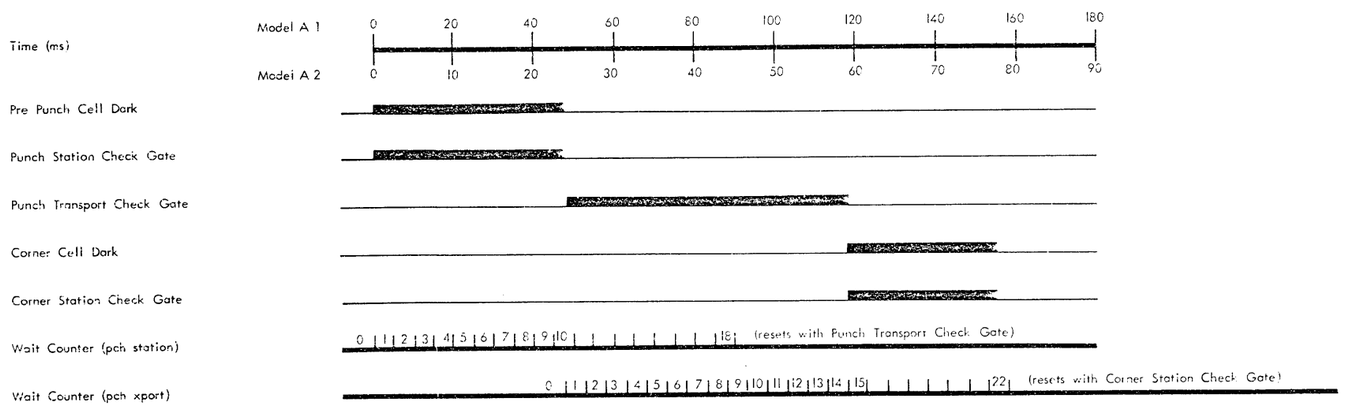


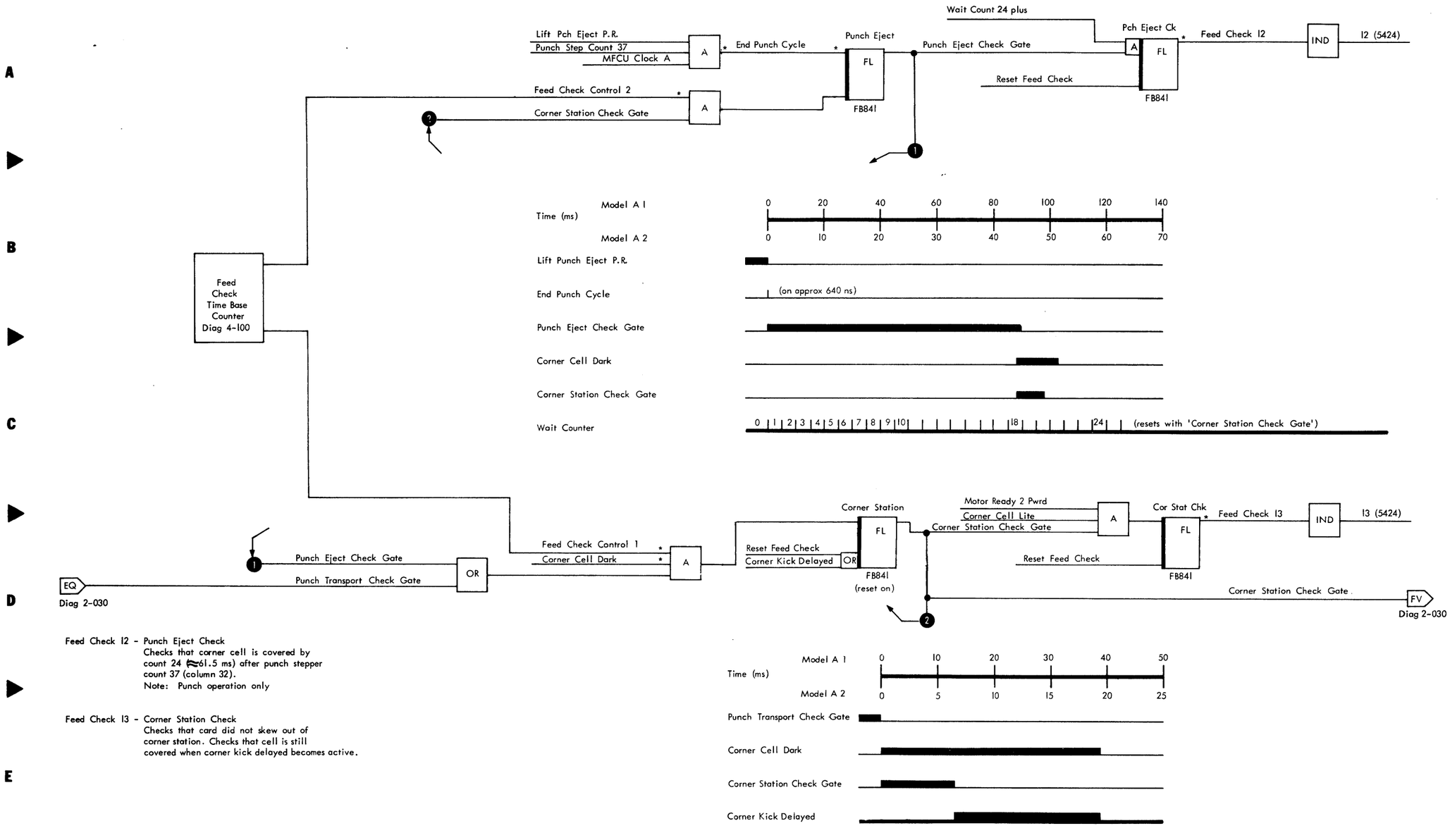
Diagram 2-025. Feed Checks 7, 8, and 10



Feed Check 9 – Punch Station Check
Checks that Pre-Punch Cell is exposed by count 18 (43.5–46.1 ms) after being covered.
Note: No punch operation

Feed Check 11 – Punch Transport Check
Checks that Corner Cell is covered by count 22 (53.8–56.3 ms) after Pre-Punch Cell is exposed.
Note: No punch operation

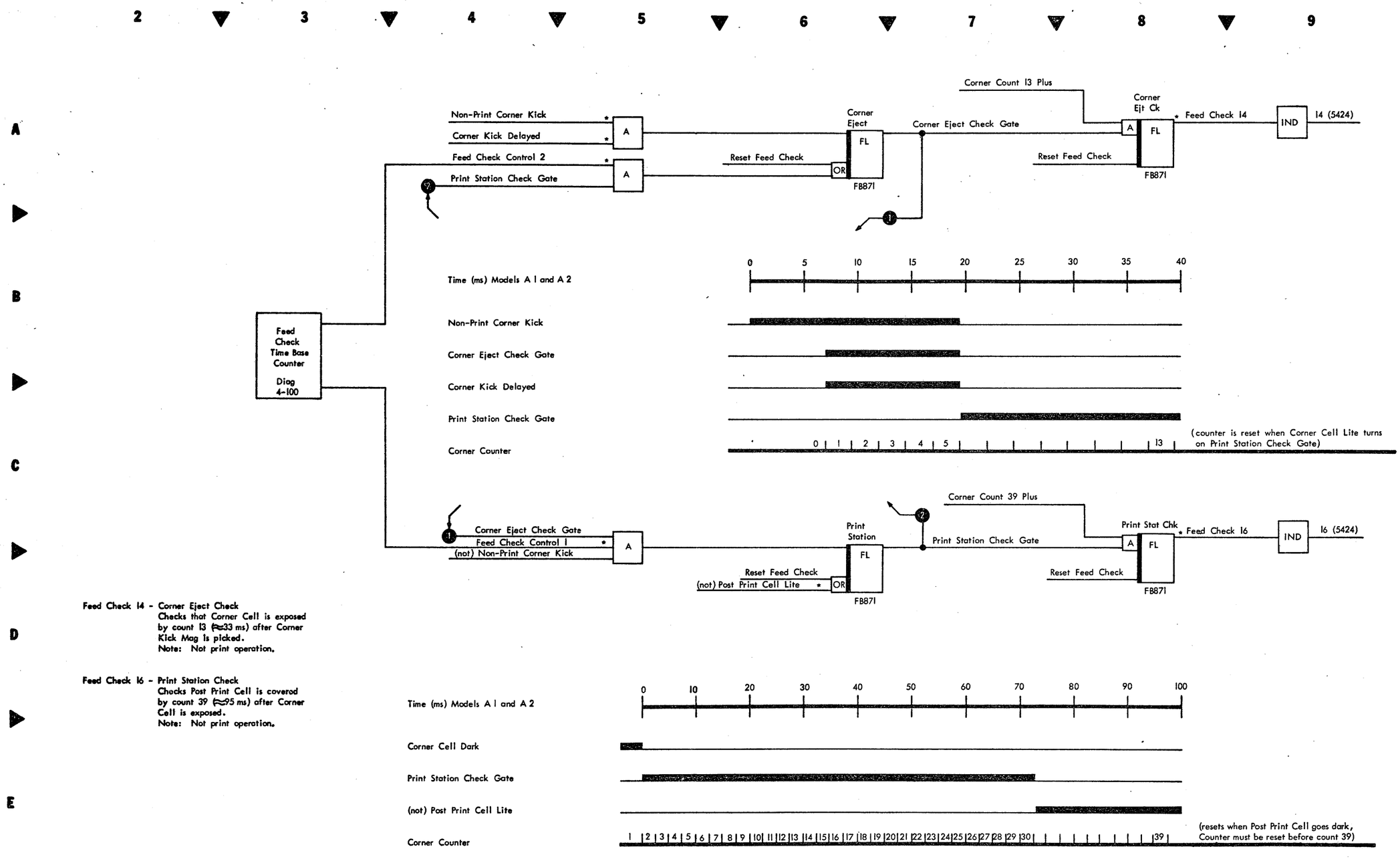




Feed Check 12 - Punch Eject Check
Checks that corner cell is covered by count 24 (≈61.5 ms) after punch stepper count 37 (column 32).
Note: Punch operation only

Feed Check 13 - Corner Station Check
Checks that card did not skew out of corner station. Checks that cell is still covered when corner kick delayed becomes active.

Diagram 2-035. Feed Checks 12 and 13



Feed Check 14 - Corner Eject Check
Checks that Corner Cell is exposed by count 13 (≈33 ms) after Corner Kick Mag is picked.
Note: Not print operation.

Feed Check 16 - Print Station Check
Checks Post Print Cell is covered by count 39 (≈95 ms) after Corner Cell is exposed.
Note: Not print operation.

2 3 4 5 6 7 8 9

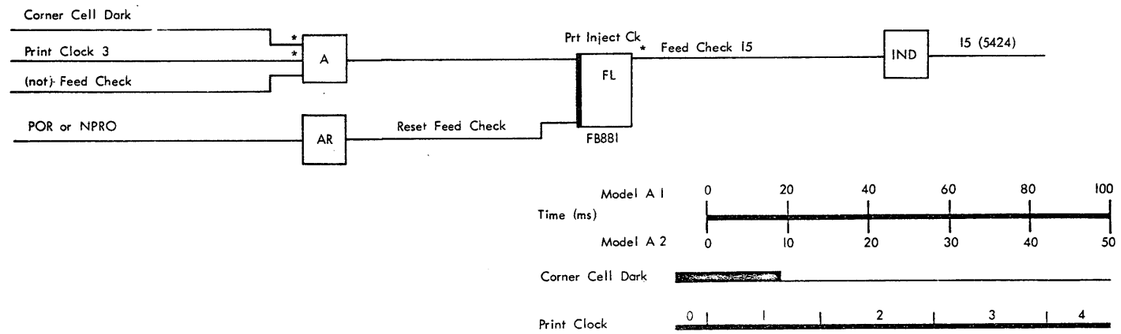
A

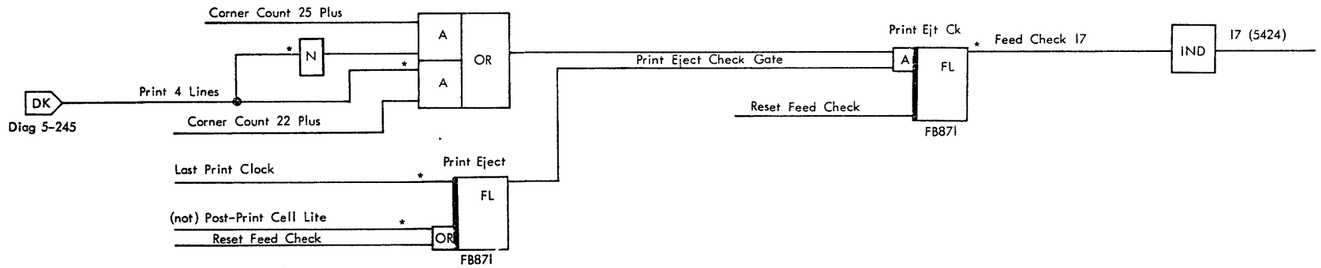
B

C

D

E





Feed Check 15 - Print Inject Gate
Checks that corner cell is exposed by print clock count 3
Note: Print operation only

Feed Check 17 - Print Eject Check
Checks that card covers post-print cell by count 25 (≈72 ms) after print clock 22 for 3 lines of print or by count 22 (≈56 ms) after print clock 28 for 4 lines of print
This feed check indicates that card is early or late in covering post cell. If print stepper clutch fails to latch, the card is sent to the stacker before check resulting in feed check 17. Usually a clutch check is also indicated
Note: Print operation only

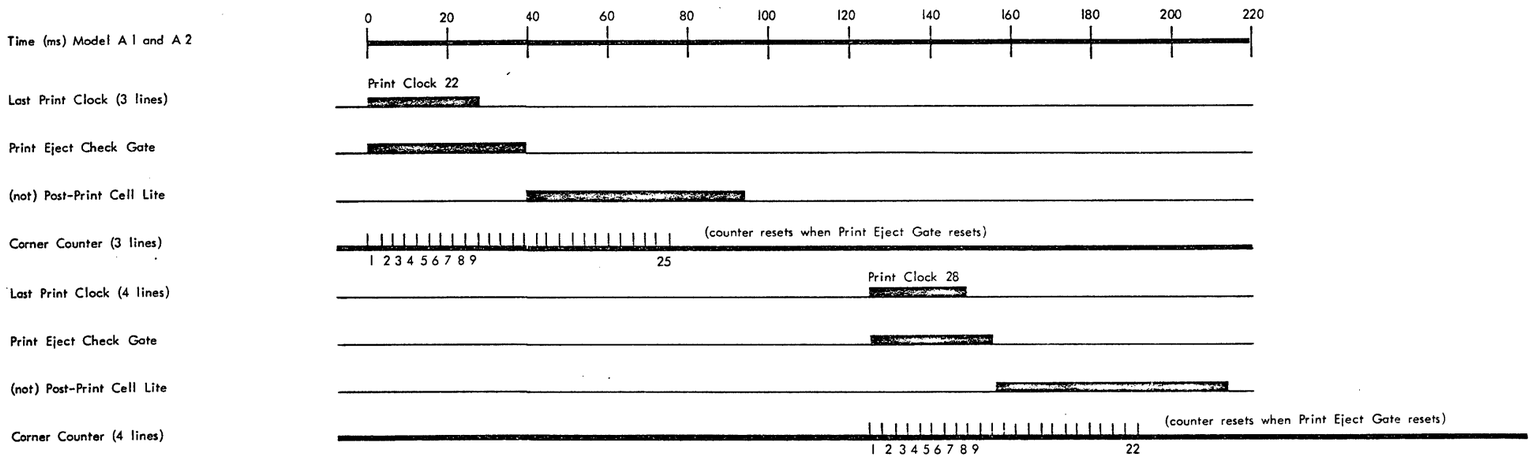
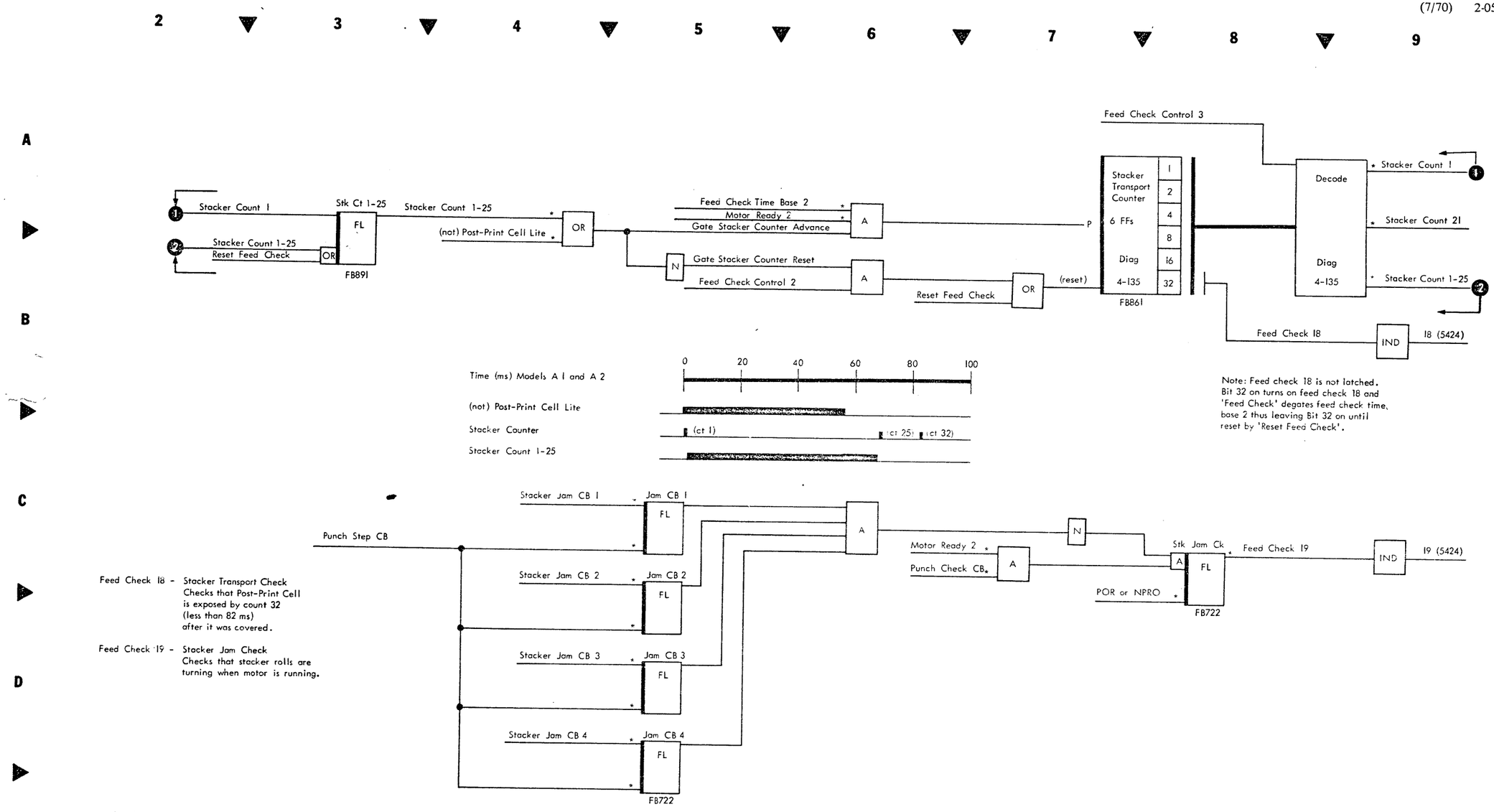


Diagram 2-045. Feed Checks 15 and 17


2
3
4
5
6
7
8
9
A
B
C
D
E
Stacker Count 1
Stacker Count 1-25
Reset Feed Check
Stk Ct 1-25
FL
OR
FB891
Stacker Count 1-25
(not) Post-Print Cell Lite
OR
Feed Check Time Base 2
Motor Ready 2
Gate Stacker Counter Advance
A
P
Gate Stacker Counter Reset
N
Feed Check Control 2
A
Reset Feed Check
OR
(reset)
Feed Check Control 3
Stacker Transport Counter
6 FFs
Diag
4-135
1
2
4
8
16
32
FB861
Decode
Diag
4-135
Stacker Count 1
Stacker Count 21
Stacker Count 1-25
Feed Check 18
IND
18 (5424)
Note: Feed check 18 is not latched. Bit 32 on turns on feed check 18 and 'Feed Check' degates feed check time, base 2 thus leaving Bit 32 on until reset by 'Reset Feed Check'.
Time (ms) Models A 1 and A 2
0 20 40 60 80 100
(not) Post-Print Cell Lite
Stacker Counter
(ct 1)
(ct 25)
(ct 32)
Stacker Count 1-25
Stacker Jam CB 1
Jam CB 1
FL
Punch Step CB
Stacker Jam CB 2
Jam CB 2
FL
Stacker Jam CB 3
Jam CB 3
FL
Stacker Jam CB 4
Jam CB 4
FL
FB722
A
Motor Ready 2
Punch Check CB
A
N
Stk Jam Ck
A
FL
FB722
POR or NPRO
Feed Check 19
IND
19 (5424)
Feed Check 18 - Stacker Transport Check
Checks that Post-Print Cell is exposed by count 32 (less than 82 ms) after it was covered.
Feed Check 19 - Stacker Jam Check
Checks that stacker rolls are turning when motor is running.
Model A 1
Time (ms)
0 2 4 6 8 10 12 14
Stacker Jam CB
Punch Step CB
Punch Check CB
Punch Step CB Duration Will Vary With CB Air Gap Adjustment
.64 us. in Duration
Model A 2
Time (ms)
0 1 2 3 4 5 6 7
Stacker Jam CB
Punch Step CB
Punch Check CB
Punch Step CB Duration Will Vary With CB Air Gap Adjustment
.64 us. in Duration

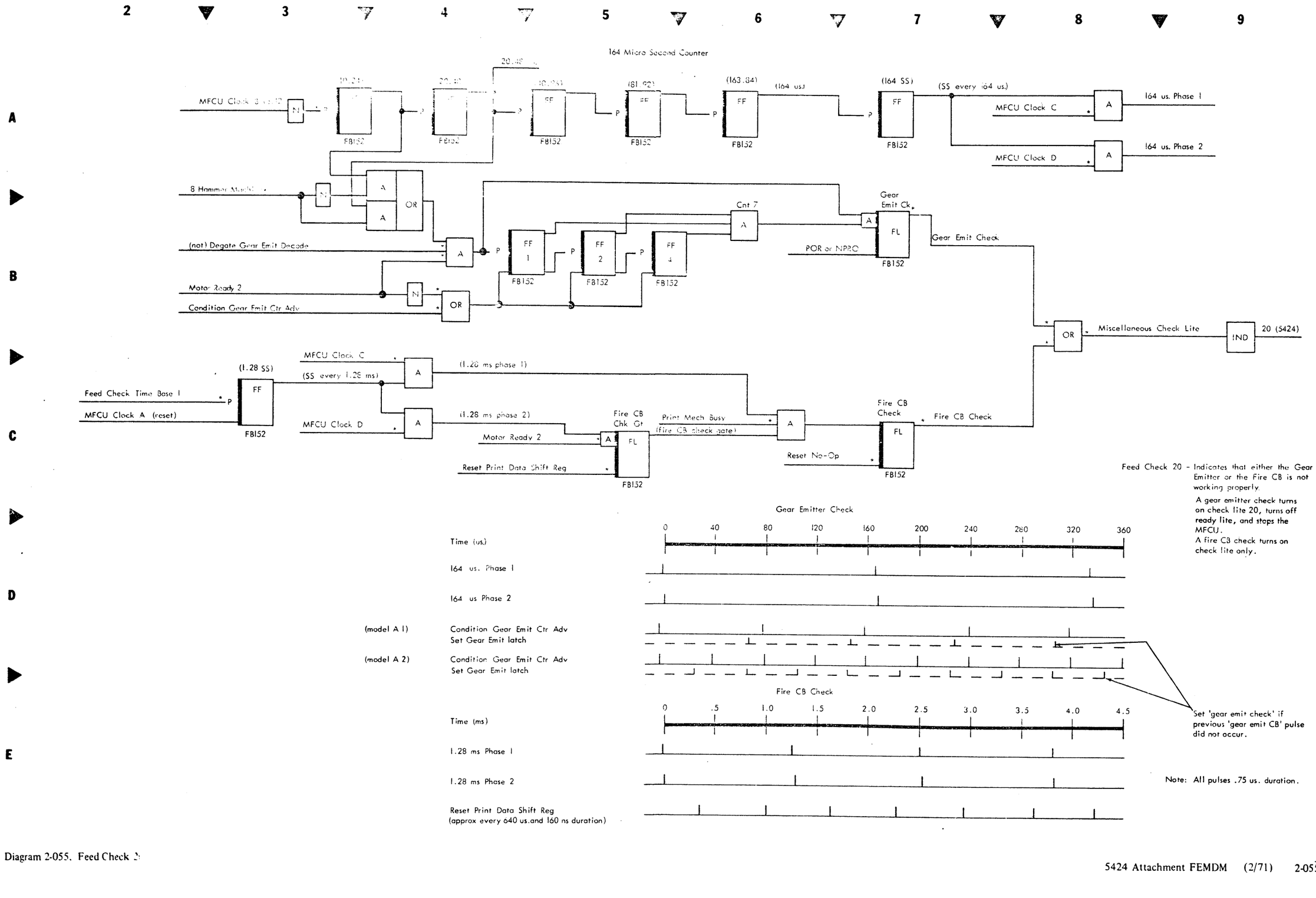
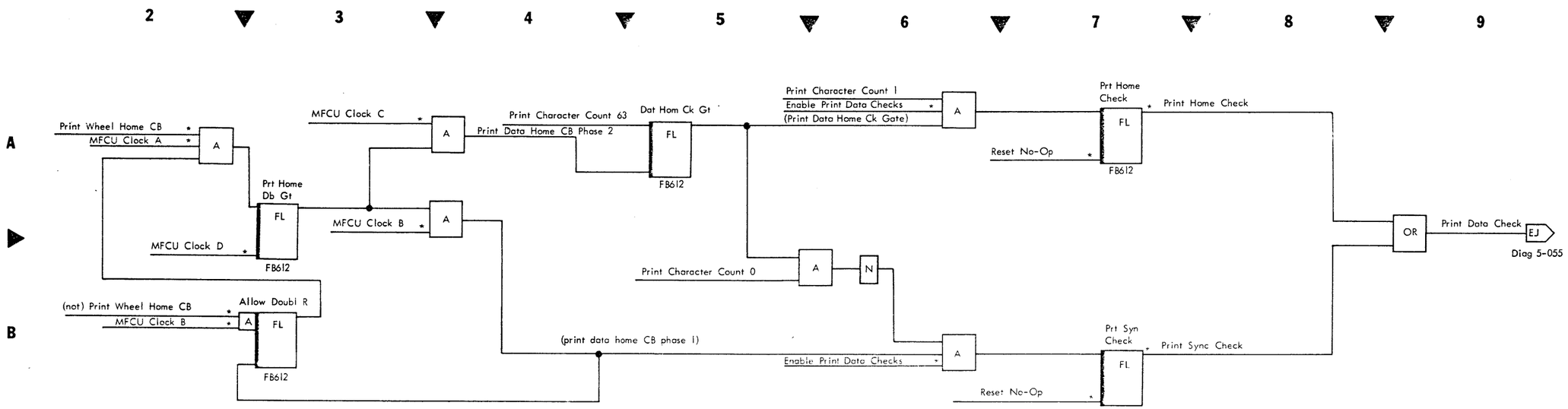


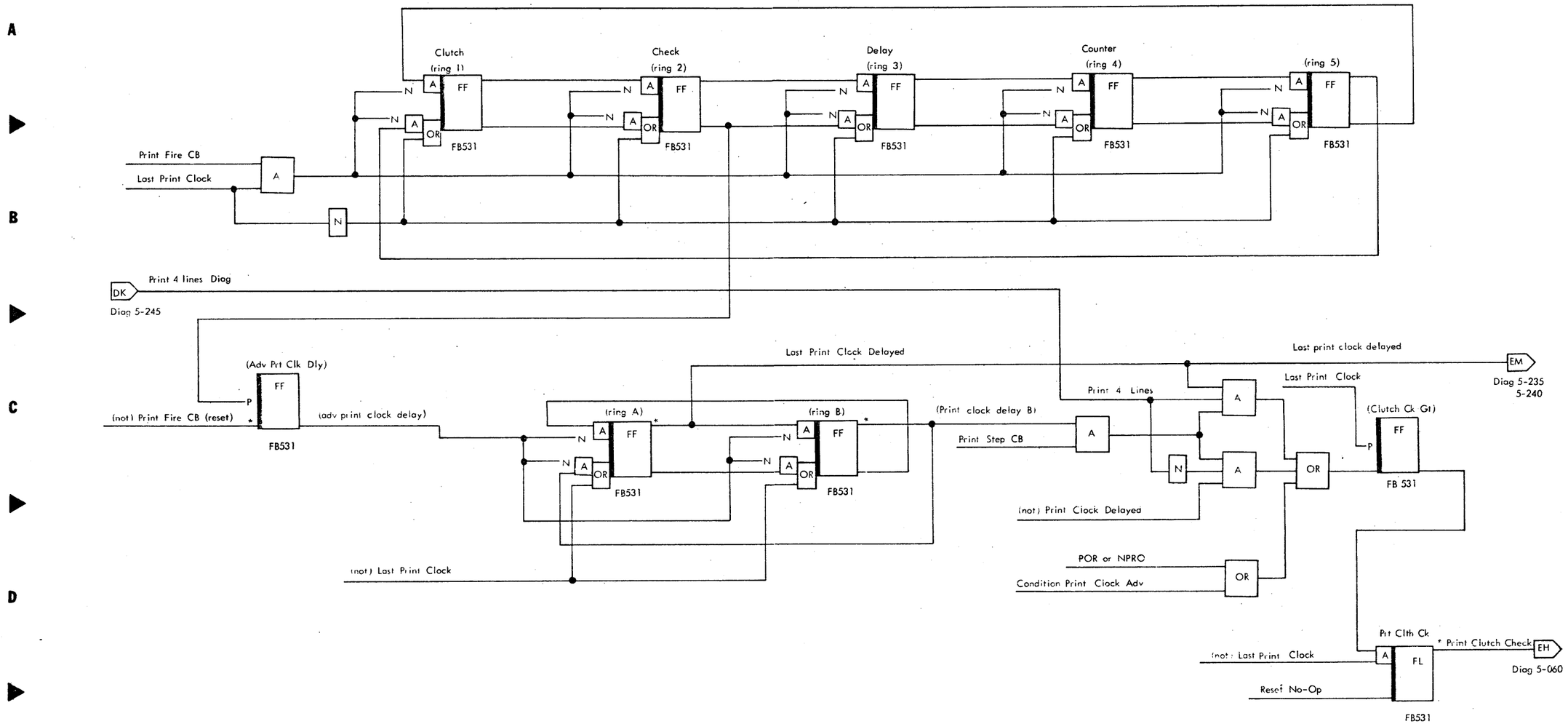
Diagram 2-055. Feed Check 2



Print Home Check - Checks that Home CB occurs after Print Character Count 63 and prior to Character Count 1

Print Sync Check - Checks that Home CB occurs during Print Character Count 0

Note 1: Leading edge of 'Print Wheel Home CB' must occur from 1 to 500 us. after the leading edge of the 'Fire CB'. Timings of 'Print Home Double Gate', 'Allow Prt Home Dblr Gate' and 'Home CB' will shift with 'Print Wheel Home CB'.


2
3
4
5
6
7
8
9
A
B
C
D
E
Clutch (ring 1)
Check (ring 2)
Delay (ring 3)
Counter (ring 4)
(ring 5)
FF
A
N
OR
FB531
Print Fire CB
Last Print Clock
Print 4 lines Diag
DK
Diag 5-245
(Adv Prt Clk Dly)
P
(not) Print Fire CB (reset)
(adv print clock delay)
(ring A)
(ring B)
(not) Last Print Clock
Last Print Clock Delayed
(Print clock delay B)
Print Step CB
Print 4 Lines
Last print clock delayed
EM
Diag 5-235
5-240
Last Print Clock
(Clutch Ck Gt)
FB 531
(not) Print Clock Delayed
POR or NPRO
Condition Print Clock Adv
Prt Clth Ck
(not) Last Print Clock
Reset No-Op
* Print Clutch Check
EH
Diag 5-060
FL

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

A
B
C
D
E

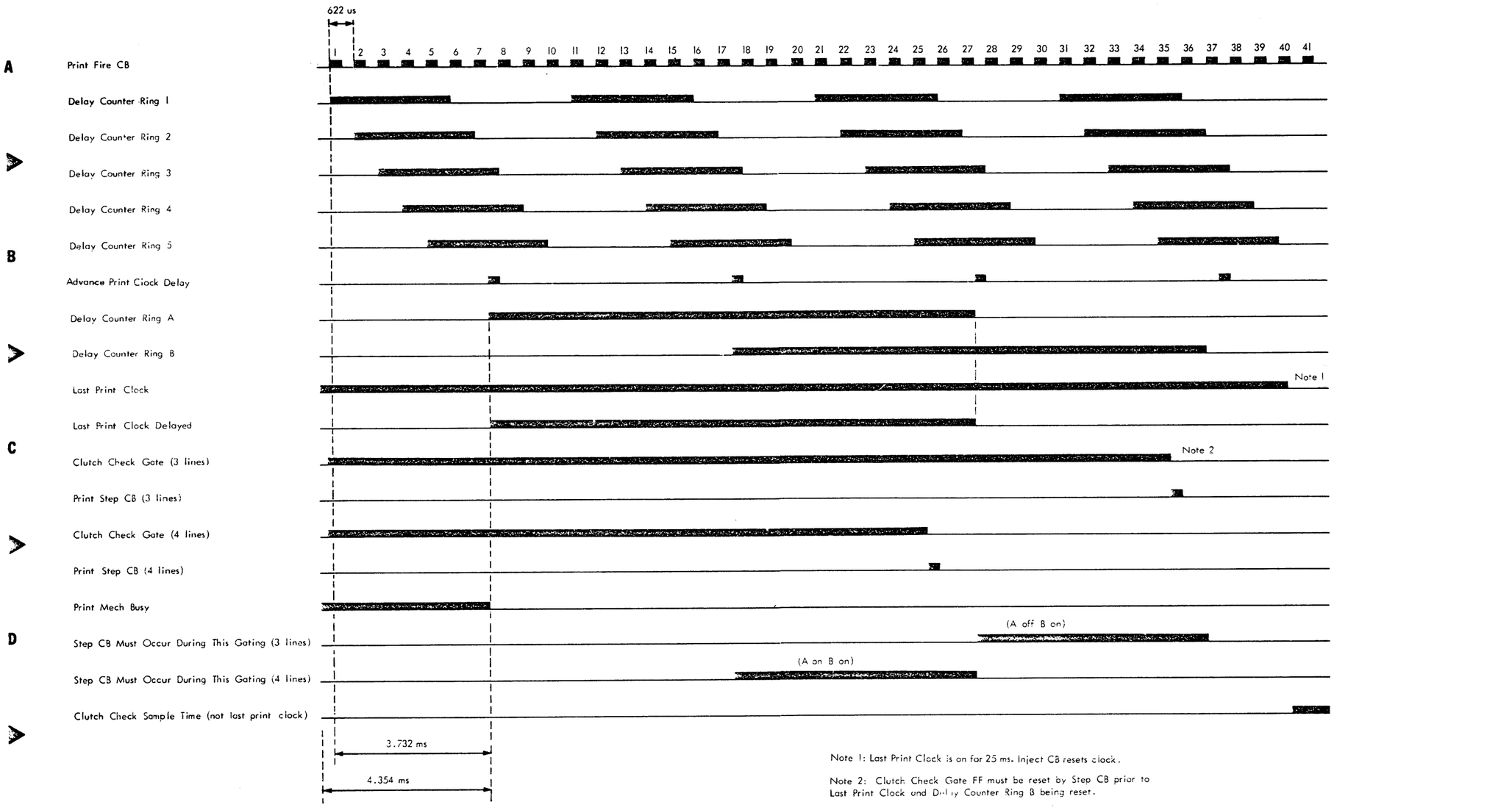


Diagram 2-070. Print Clutch Check (Part 2 of 2)

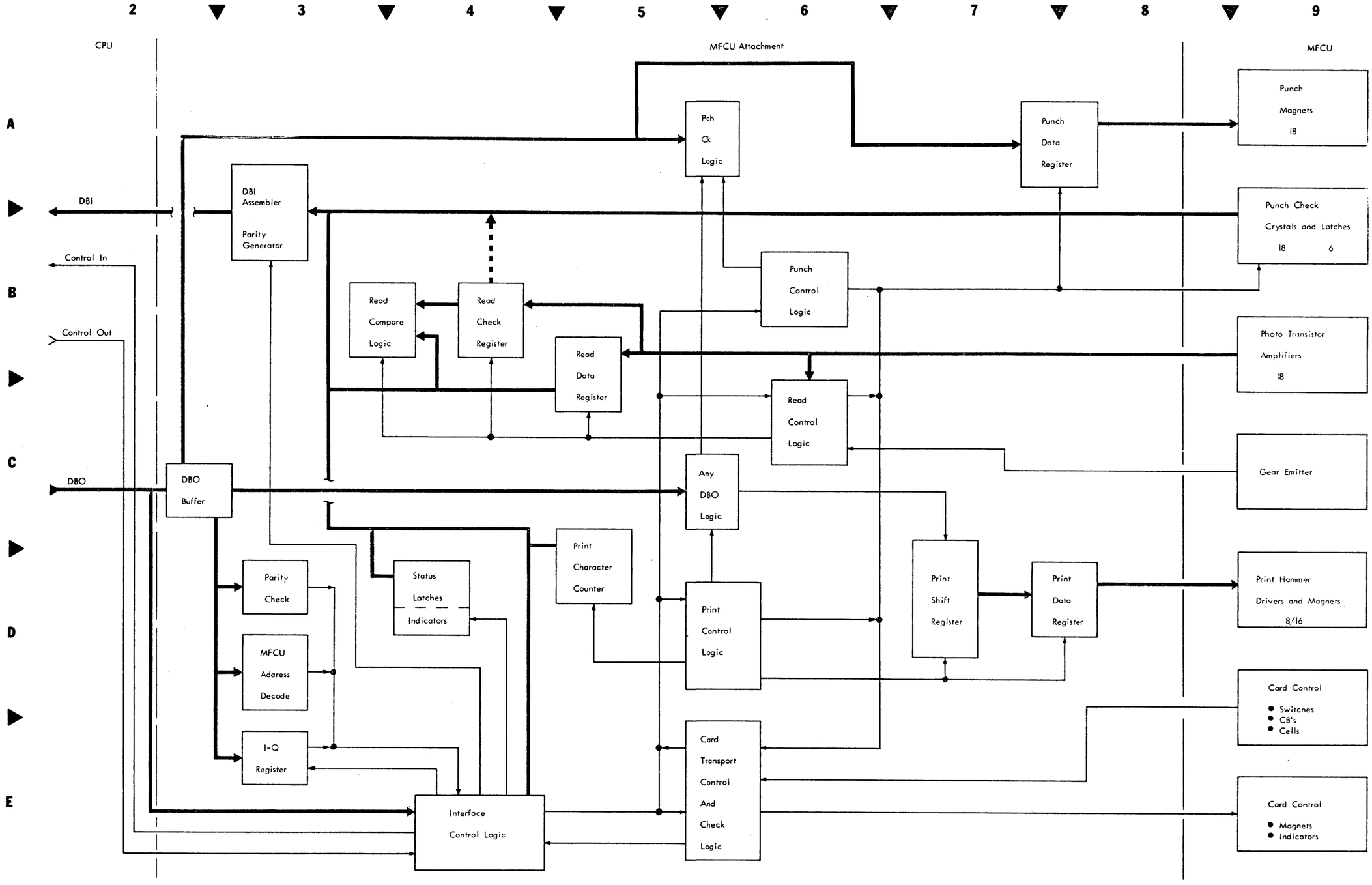


Diagram 3-005. MFCU Attachment Data Flow

2 3 4 5 6 7 8 9

A

B

C

D

E

Data Bus Out

Data Bus In

In

Controls

Out

5424

PTX

Gear

Emitter

Switches

Emitters

Cells

Controls

Read

Controls

Card

Transport

Controls

LSR

Select

Status

Register

Data Bus In

Register

Read

Data

Register

Read

Check

Register

Read

Compare

5424

Card Control

Magnets and Indicators

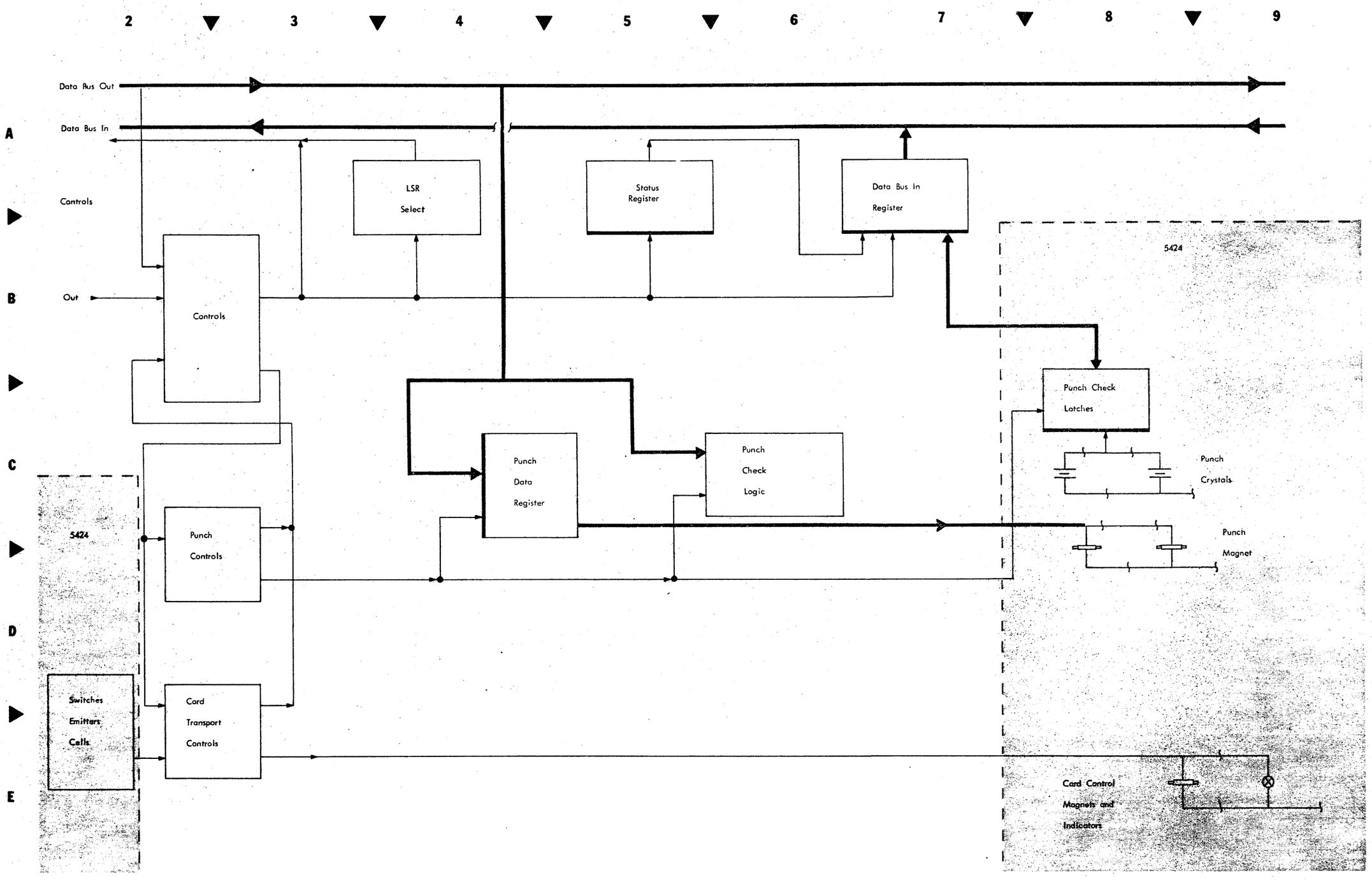
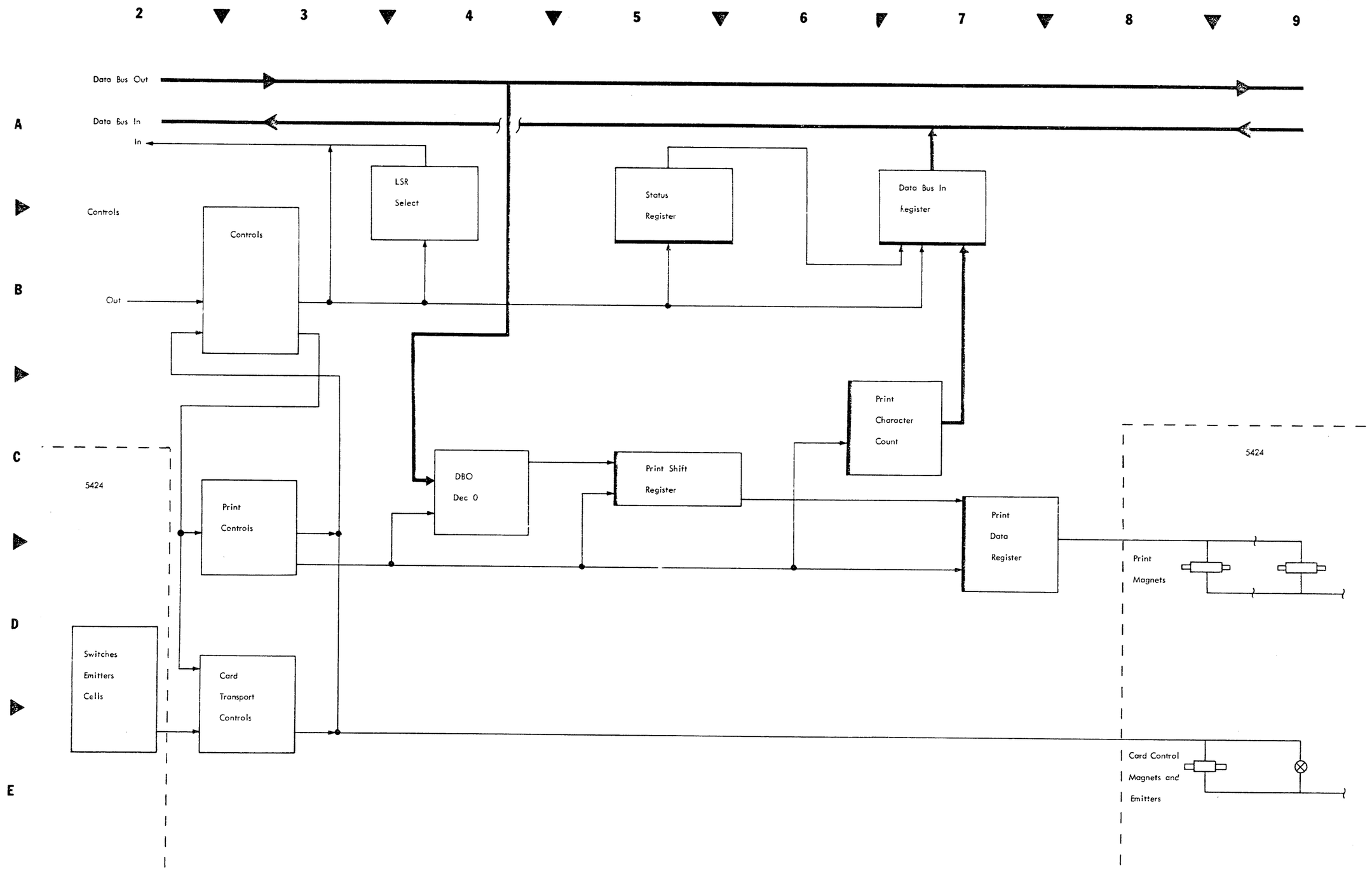


Diagram 3-015. Punch Data Flow

Diagram 3-020. Print Data Flow



2 3 4 5 6 7 8 9

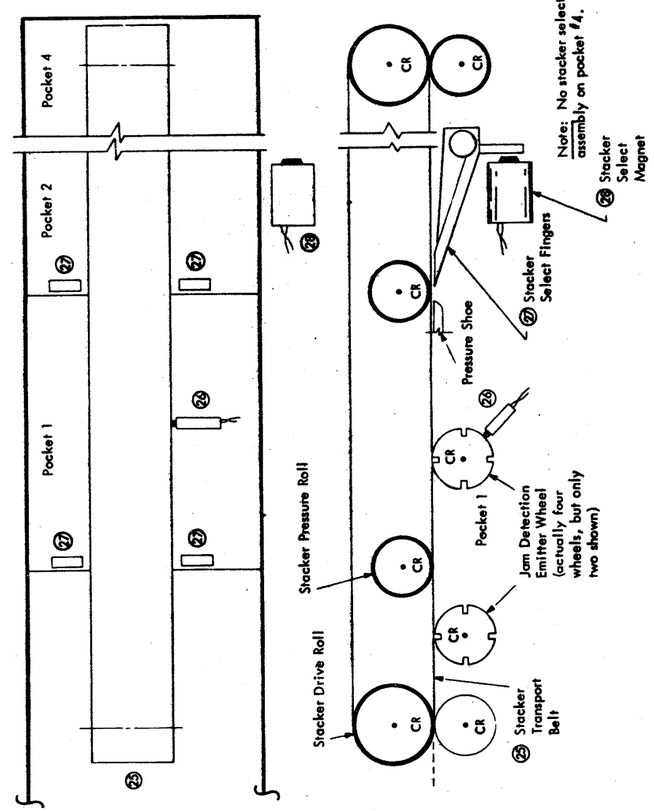
A

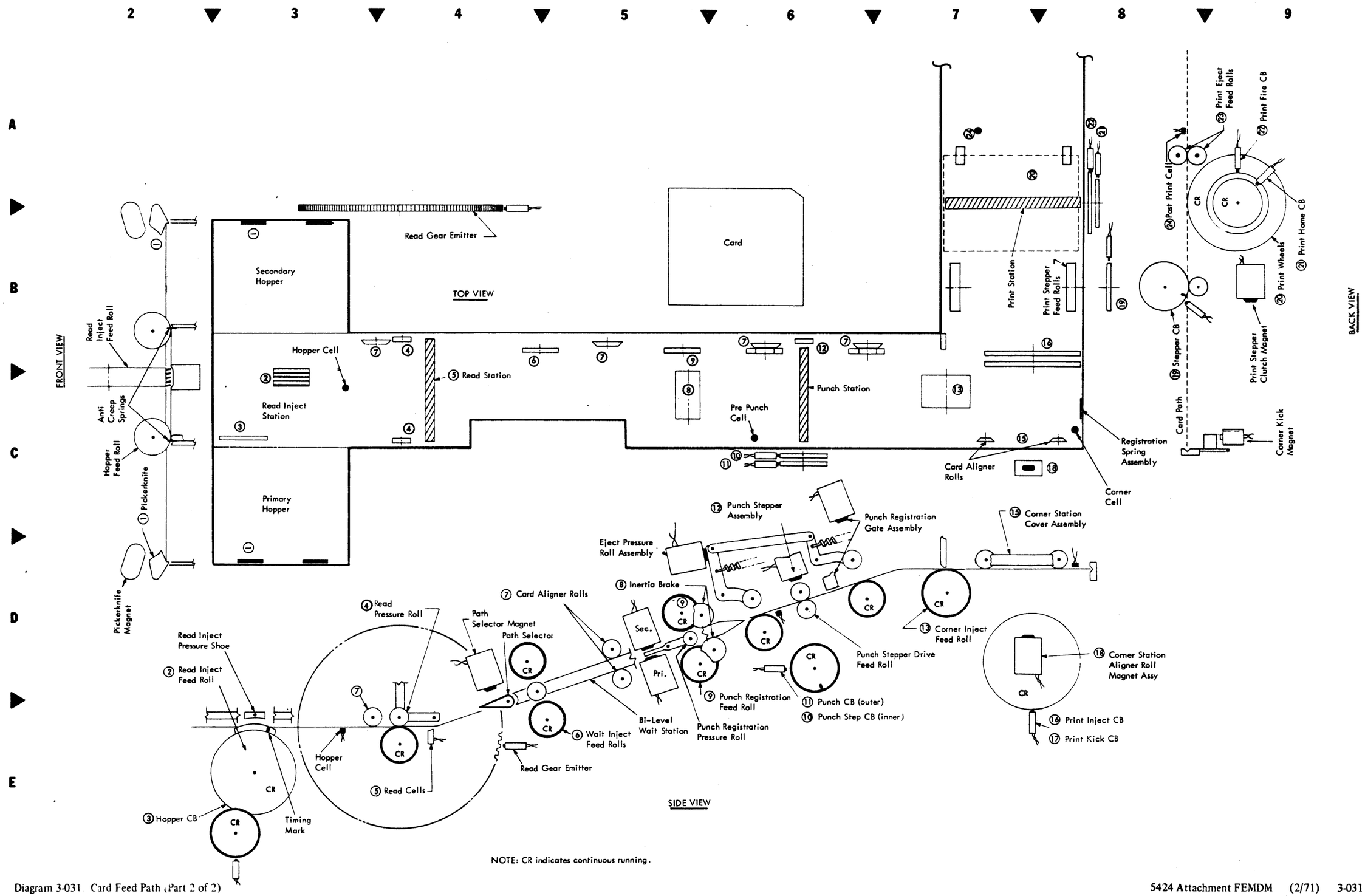
B

C

D

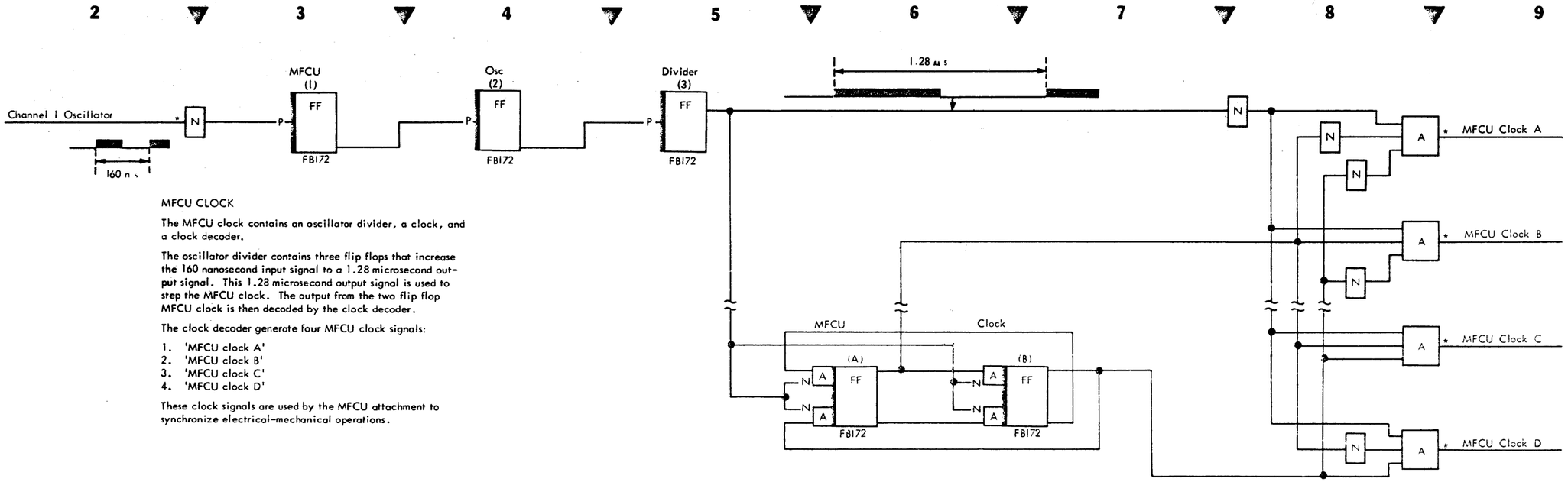
E





NOTE: CR indicates continuous running.

Diagram 3-031 Card Feed Path (Part 2 of 2)



MFCU CLOCK

The MFCU clock contains an oscillator divider, a clock, and a clock decoder.

The oscillator divider contains three flip flops that increase the 160 nanosecond input signal to a 1.28 microsecond output signal. This 1.28 microsecond output signal is used to step the MFCU clock. The output from the two flip flop MFCU clock is then decoded by the clock decoder.

The clock decoder generate four MFCU clock signals:

1. 'MFCU clock A'
2. 'MFCU clock B'
3. 'MFCU clock C'
4. 'MFCU clock D'

These clock signals are used by the MFCU attachment to synchronize electrical-mechanical operations.

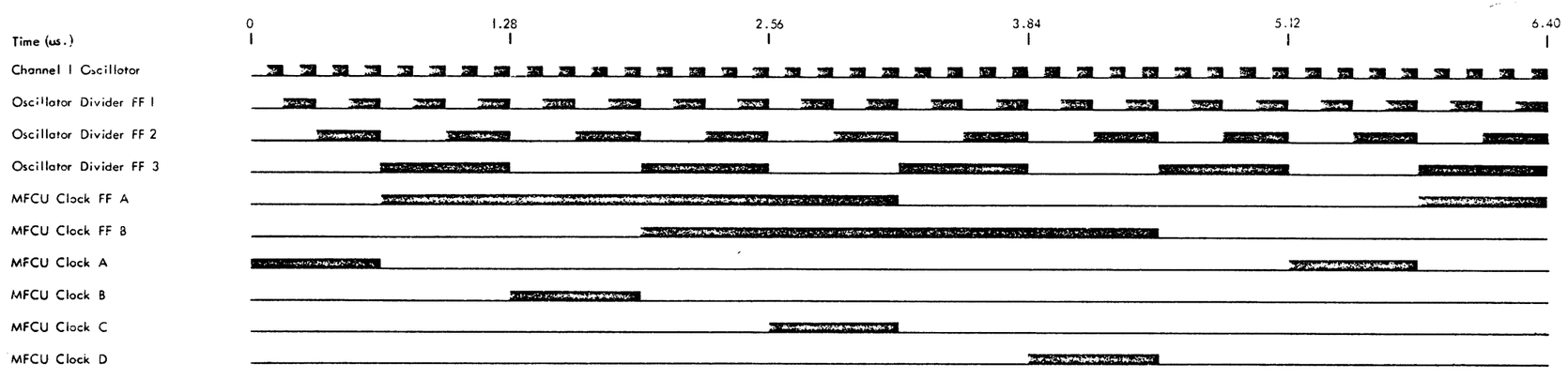
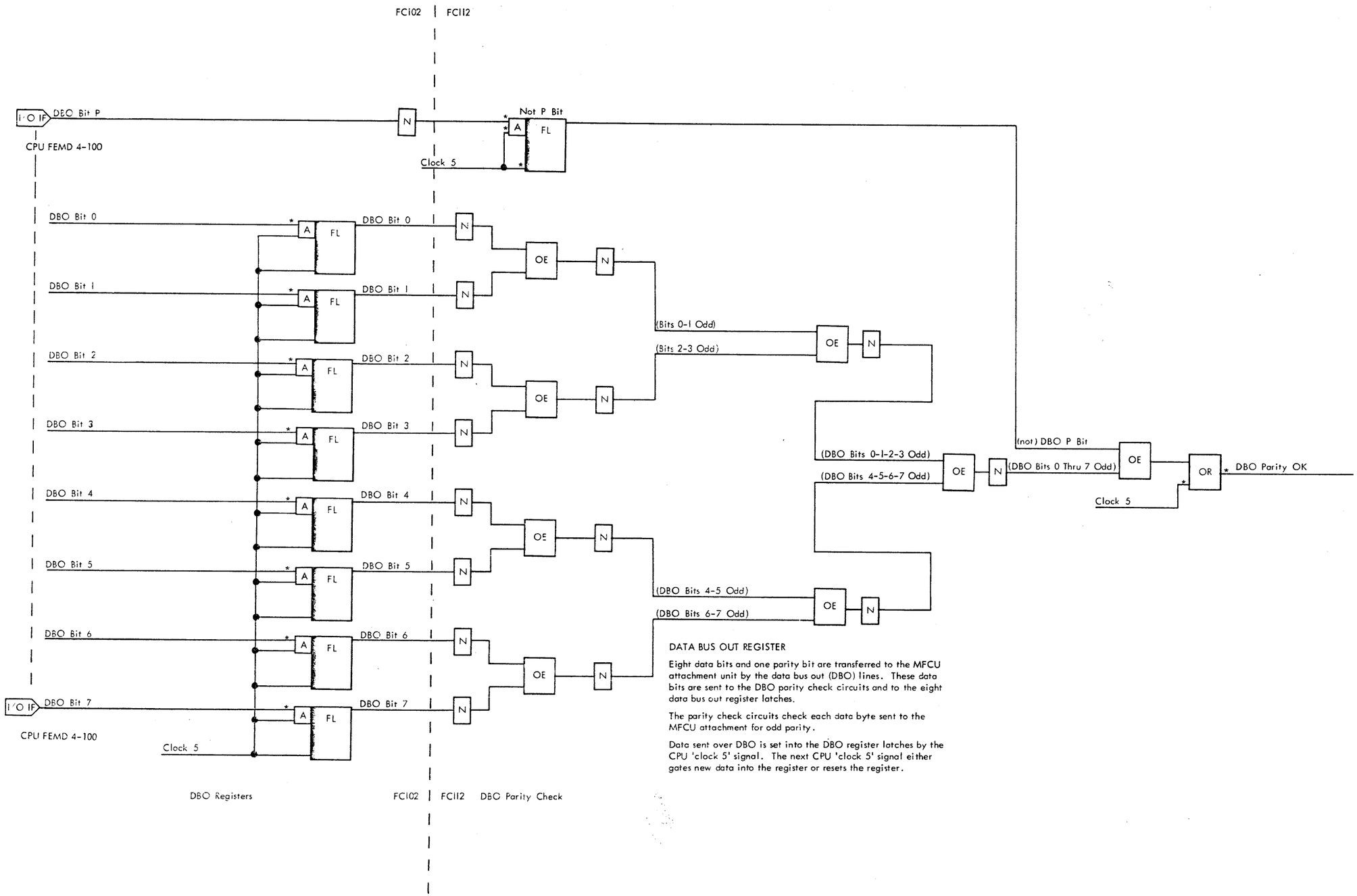


Diagram 4-005. MFCU Clock



DATA BUS OUT REGISTER

Eight data bits and one parity bit are transferred to the MFCU attachment unit by the data bus out (DBO) lines. These data bits are sent to the DBO parity check circuits and to the eight data bus out register latches.

The parity check circuits check each data byte sent to the MFCU attachment for odd parity.

Data sent over DBO is set into the DBO register latches by the CPU 'clock 5' signal. The next CPU 'clock 5' signal either gates new data into the register or resets the register.

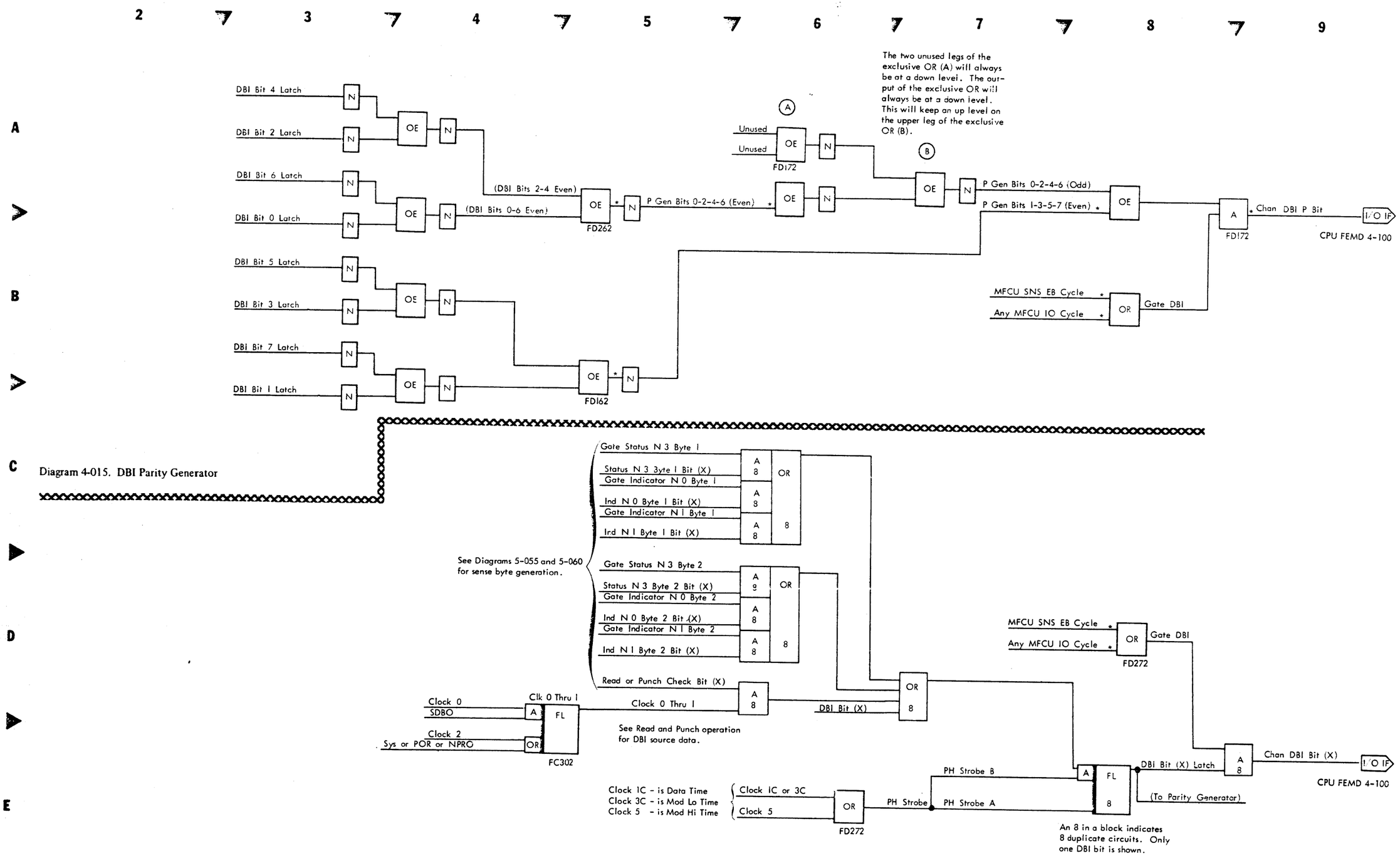
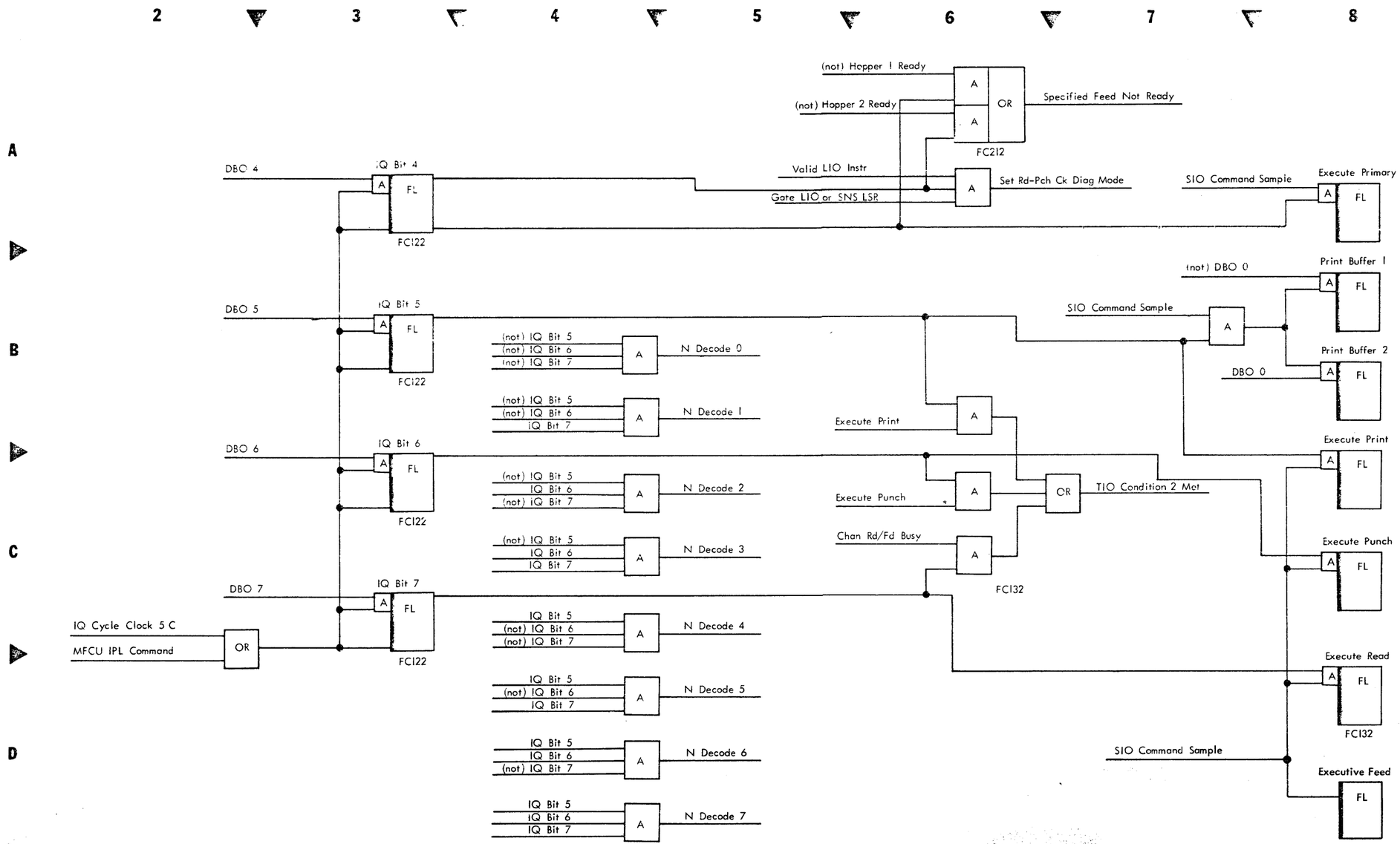


Diagram 4-015. DBI Parity Generator

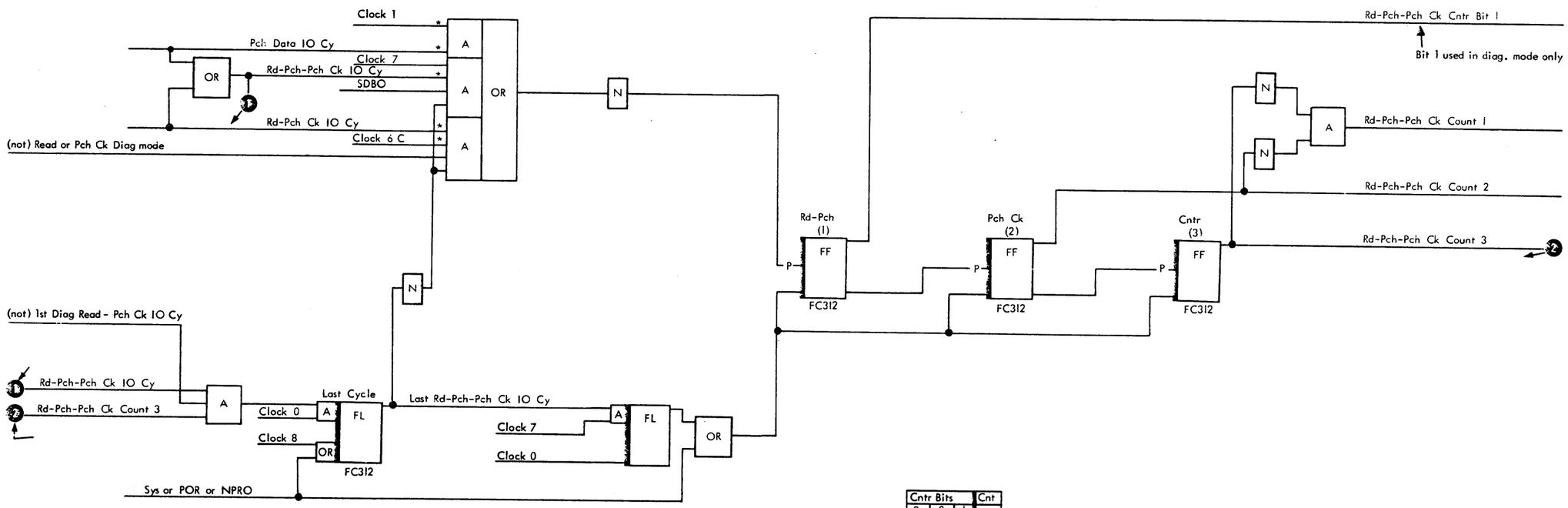
Diagram 4-020. DBI Assembler



I-Q REGISTER

The I-Q register is a four bit register that is loaded during the I-Q cycle of an MFCU instruction. During the MFCU instruction I-Q cycle, bits 4, 5, 6, and 7 are gated to the I-Q register by a CPU 'I-Q clock 5C' signal.

The function to be performed by the MFCU is defined by decoding the output of the I-Q register. The functions performed depend upon the programmed I/O instruction.



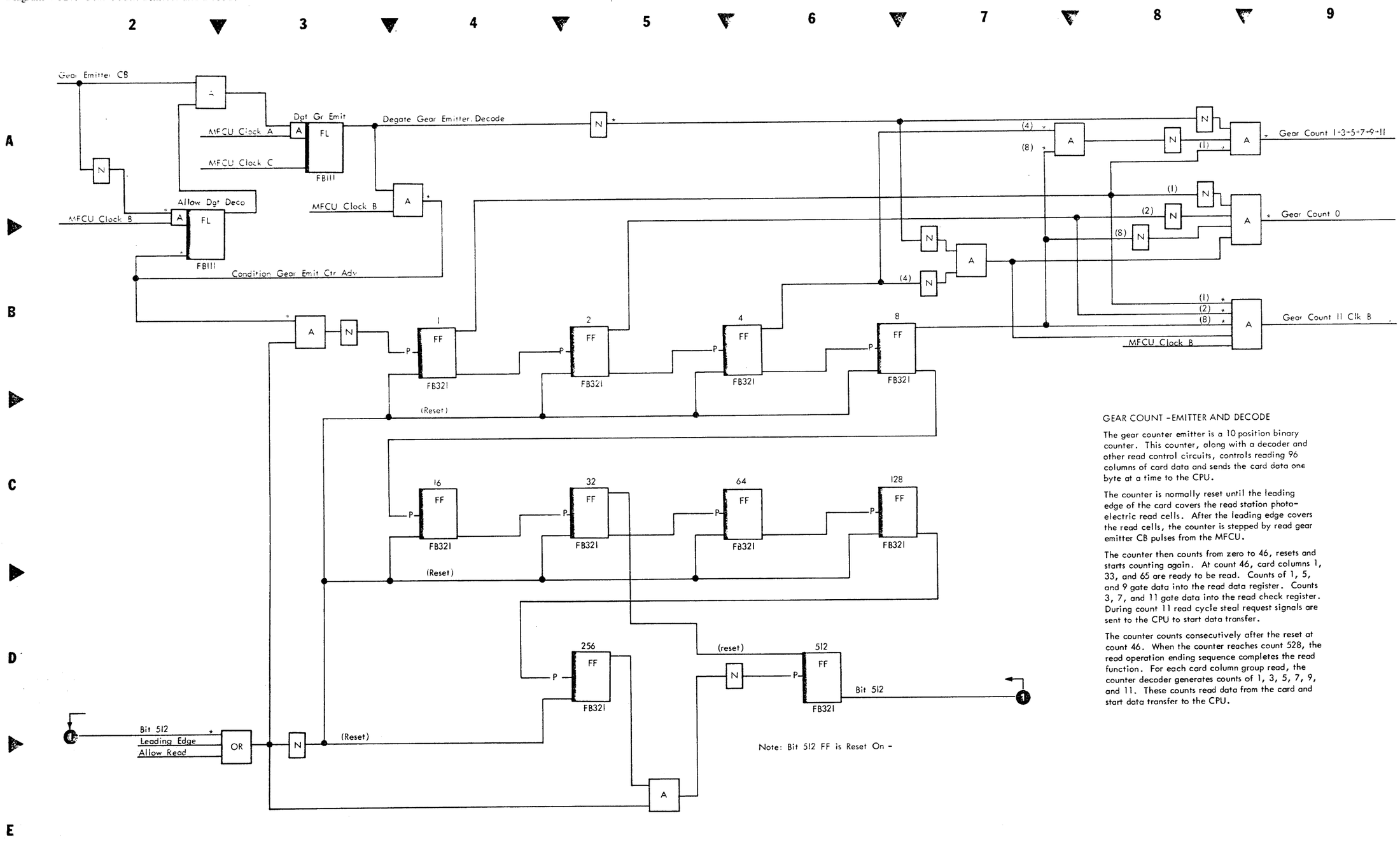
Read-Punch-Punch Ck Counter

- Keeps track of read, punch, or punch check cycle steals
- Advanced at clock 6C and clock 7 on read operation and punch check operation
- Advanced at clock 1 and clock 7 on punch operation
- Two advances necessary to change count
- Diag. read or punch = one advance per cycle steal

Cntr Bits 3	2	1	Cnt
0	0	0	
0	0	1	1
0	1	0	
0	1	1	2
1	0	0	
1	0	1	3

Bit 1 used in diag. mode only

Diagram 4-025. Read-Punch-Punch Check Counter



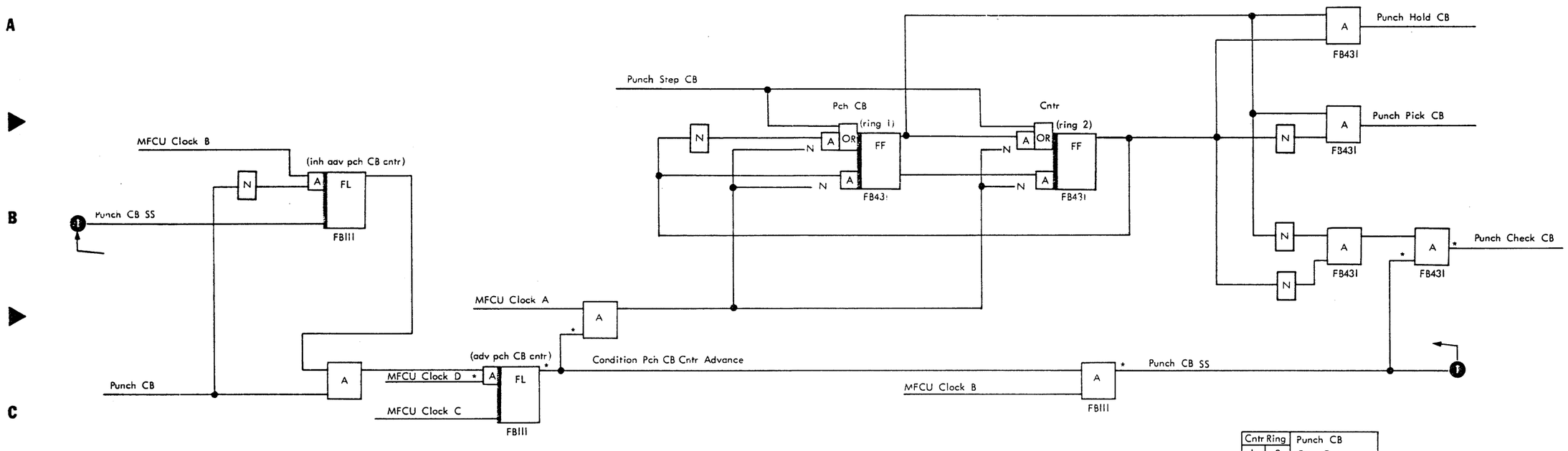
GEAR COUNT - EMITTER AND DECODE

The gear counter emitter is a 10 position binary counter. This counter, along with a decoder and other read control circuits, controls reading 96 columns of card data and sends the card data one byte at a time to the CPU.

The counter is normally reset until the leading edge of the card covers the read station photo-electric read cells. After the leading edge covers the read cells, the counter is stepped by read gear emitter CB pulses from the MFCU.

The counter then counts from zero to 46, resets and starts counting again. At count 46, card columns 1, 33, and 65 are ready to be read. Counts of 1, 5, and 9 gate data into the read data register. Counts 3, 7, and 11 gate data into the read check register. During count 11 read cycle steal request signals are sent to the CPU to start data transfer.

The counter counts consecutively after the reset at count 46. When the counter reaches count 528, the read operation ending sequence completes the read function. For each card column group read, the counter decoder generates counts of 1, 3, 5, 7, 9, and 11. These counts read data from the card and start data transfer to the CPU.



Cntr Ring 1	Cntr Ring 2	Punch CB Cntr Output
1	1	Punch Hold CB
0	1	Not Used
0	0	Punch Check CB
1	0	Punch Pick CB

PUNCH CB COUNTER AND DECODE

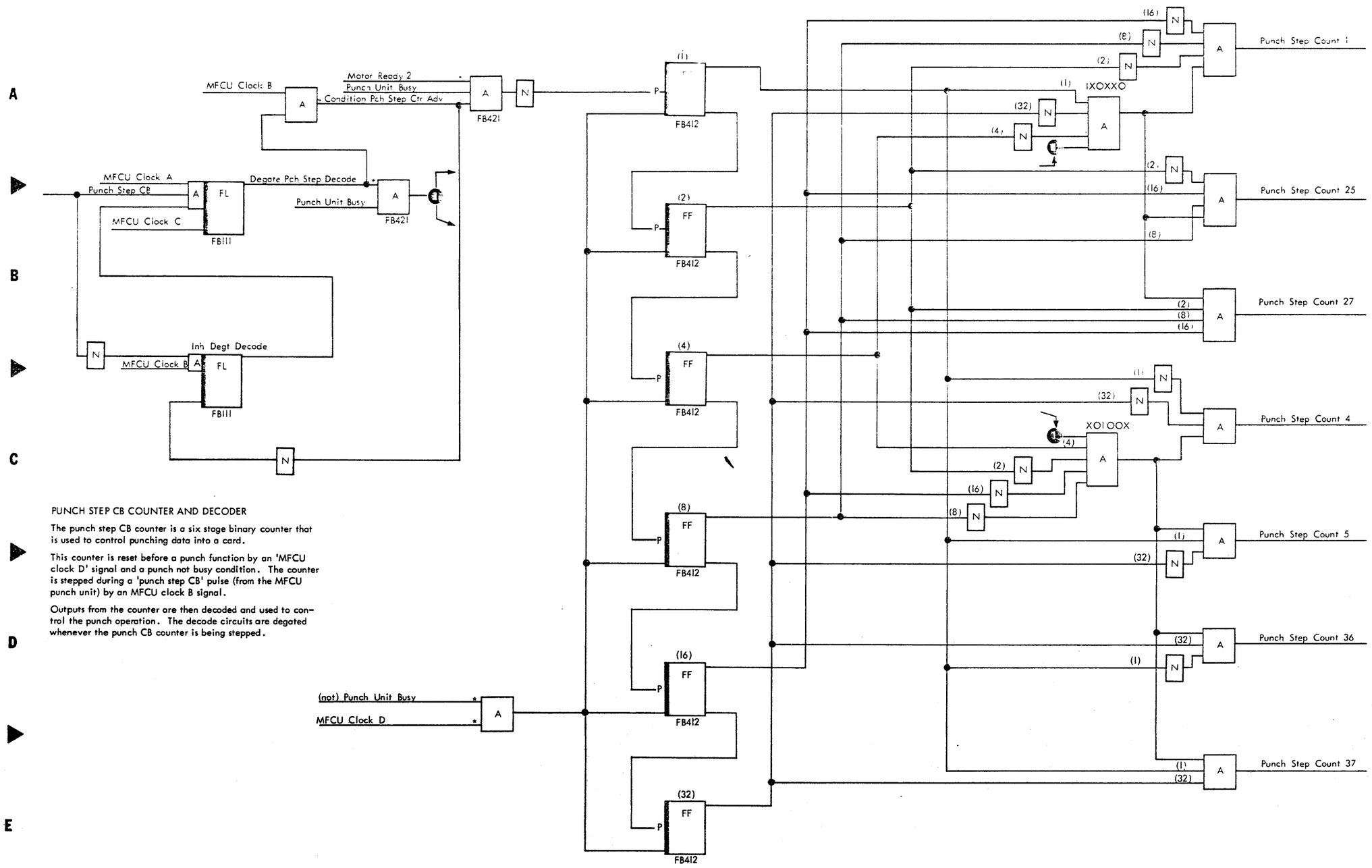
This two stage binary punch CB counter and decode activates the punch pick, the punch hold, the punch de-energize, and the punch check circuits.

Each 'punch step CB' pulse from the MFCU resets the counter. The counter is stepped by the 'condition punch CB control advance' signal during MFCU clock A time four times per card column group (three tiers) punched.

The outputs from the decoder determine when the punch magnets are to be energized and de-energized. Also, the counter gates the punch magnet hold current.

Checking of a column group that was punched occurs at the beginning of the next card column group to be punched.

Diagram 4-030. Punch CB Counter



PUNCH STEP CB COUNTER AND DECODER

The punch step CB counter is a six stage binary counter that is used to control punching data into a card.

This counter is reset before a punch function by an 'MFCU clock D' signal and a punch not busy condition. The counter is stepped during a 'punch step CB' pulse (from the MFCU punch unit) by an MFCU clock B signal.

Outputs from the counter are then decoded and used to control the punch operation. The decode circuits are degated whenever the punch CB counter is being stepped.

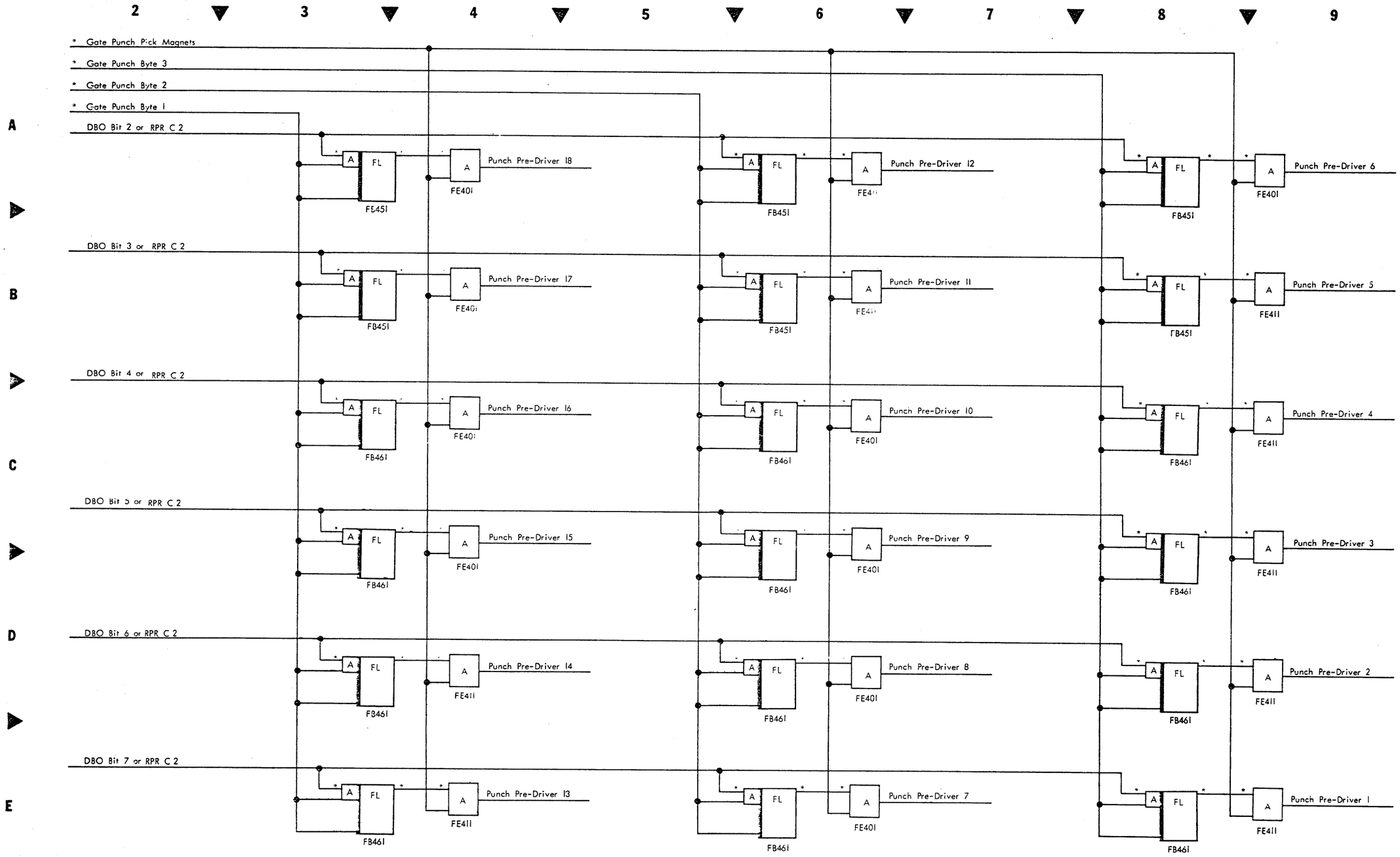


Diagram 4-040. Punch Data Register

2 3 4 5 6 7 8 9

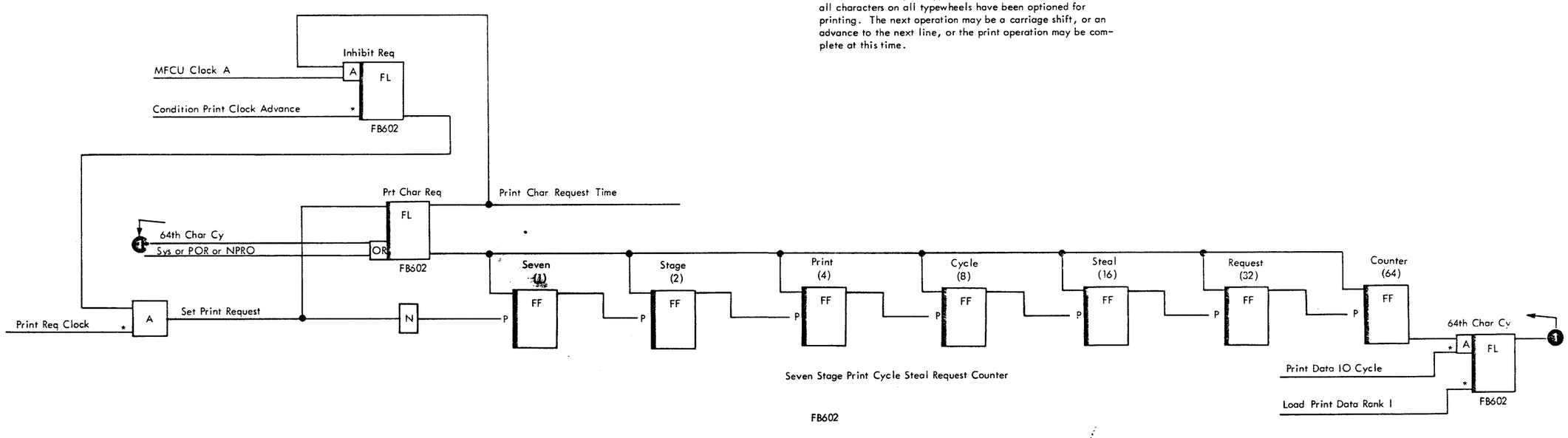
A

B

C

D

E



Seven Stage Print Cycle Steal Request Counter

FB602

PRINT CYCLE STEAL REQUEST COUNTER

The print cycle steal request counter is a seven position binary counter. This counter is stepped after each 'print fire CB' pulse by the 'set print CS request' signal.

The counter counts to 64; thereby, indicating one complete revolution of the print typewheels. After the count of 64, all characters on all typewheels have been optioned for printing. The next operation may be a carriage shift, or an advance to the next line, or the print operation may be complete at this time.

A

B

C

D

E

PRINT I/O CYCLE COUNTER

The print I/O cycle counter is a five position counter that indicates the 'last print data I/O cycle' for each group of comparisons made by the CPU.

This counter is stepped after each comparison is made by the CPU. After the print character count value for each typewheel has been compared with the character codes in the print area of core storage (16 comparisons for model A2 machines; 8 for model A1), the 'last print data I/O cycle' signal is used to modify the LSR address so that 16 more comparisons can be made for the next print character count. The counter is reset and counting begins for the next group of comparisons.

After a complete revolution of the typewheels, the LSR address is modified accordingly to select the correct core storage address for printing after a carriage shift or to begin printing the next line. Remember that the LSR address is modified after each cycle steal request.

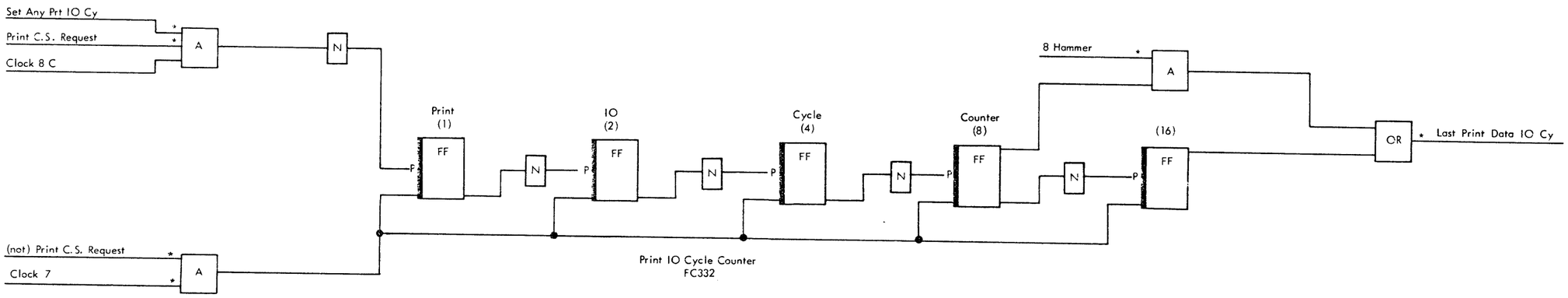
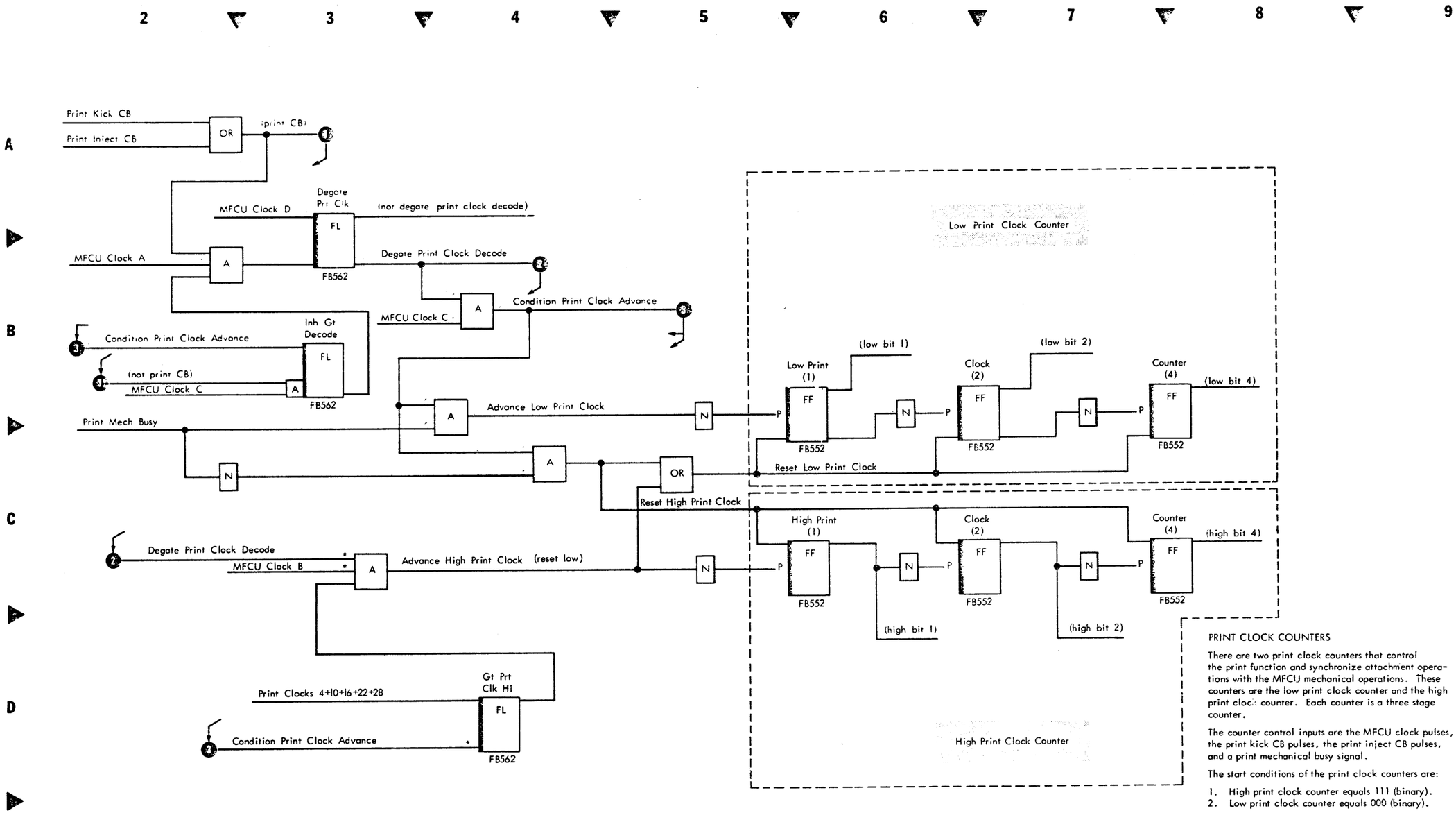


Diagram 4-050. Print I/O Cycle Counter



PRINT CLOCK COUNTERS

There are two print clock counters that control the print function and synchronize attachment operations with the MFCU mechanical operations. These counters are the low print clock counter and the high print clock counter. Each counter is a three stage counter.

The counter control inputs are the MFCU clock pulses, the print kick CB pulses, the print inject CB pulses, and a print mechanical busy signal.

The start conditions of the print clock counters are:

1. High print clock counter equals 111 (binary).
2. Low print clock counter equals 000 (binary).

After the print mechanical busy line is activated, the low print clock counter is stepped by each print kick CB pulse or a print inject CB pulse. The high print clock counter is stepped as a result of activating 'print clocks 4, or 10, or 16, or 22, or 28' line. The low print clock counter is reset each time the high print clock is advanced.

Low Print Clock Bit 1	Bit 2	Bit 4	High Print Clock Bit 1	Bit 2	Bit 4	
0	0	0	1	1	1	Count 0
1	0	0	1	1	1	Count 1
0	1	0	1	1	1	Count 2
1	1	0	1	1	1	Count 3
0	0	1	1	1	1	Count 4
1	0	0	0	0	0	Count 5
0	1	0	0	0	0	Count 6
1	1	0	0	0	0	Count 7
0	0	1	0	0	0	Count 8
1	0	1	0	0	0	Count 9
0	1	1	0	0	0	Count 10
1	0	0	1	0	0	Count 11
0	1	0	1	0	0	Count 12
1	1	0	1	0	0	Count 13
0	0	1	1	0	0	Count 14
1	0	1	1	0	0	Count 15
0	1	1	1	0	0	Count 16
1	0	0	0	1	0	Count 17
0	1	0	0	1	0	Count 18
1	1	0	0	1	0	Count 19
0	0	1	0	1	0	Count 20
1	0	1	0	1	0	Count 21
0	1	1	0	1	0	Count 22
1	0	0	1	1	0	Count 23
0	1	0	1	1	0	Count 24
1	1	0	1	1	0	Count 25
0	0	1	1	1	0	Count 26
1	0	1	1	1	0	Count 27
0	1	1	1	1	0	Count 28

PRINT CLOCK DECODE

The outputs of the print clocks are decoded and used by the print control circuits to control the print operation.

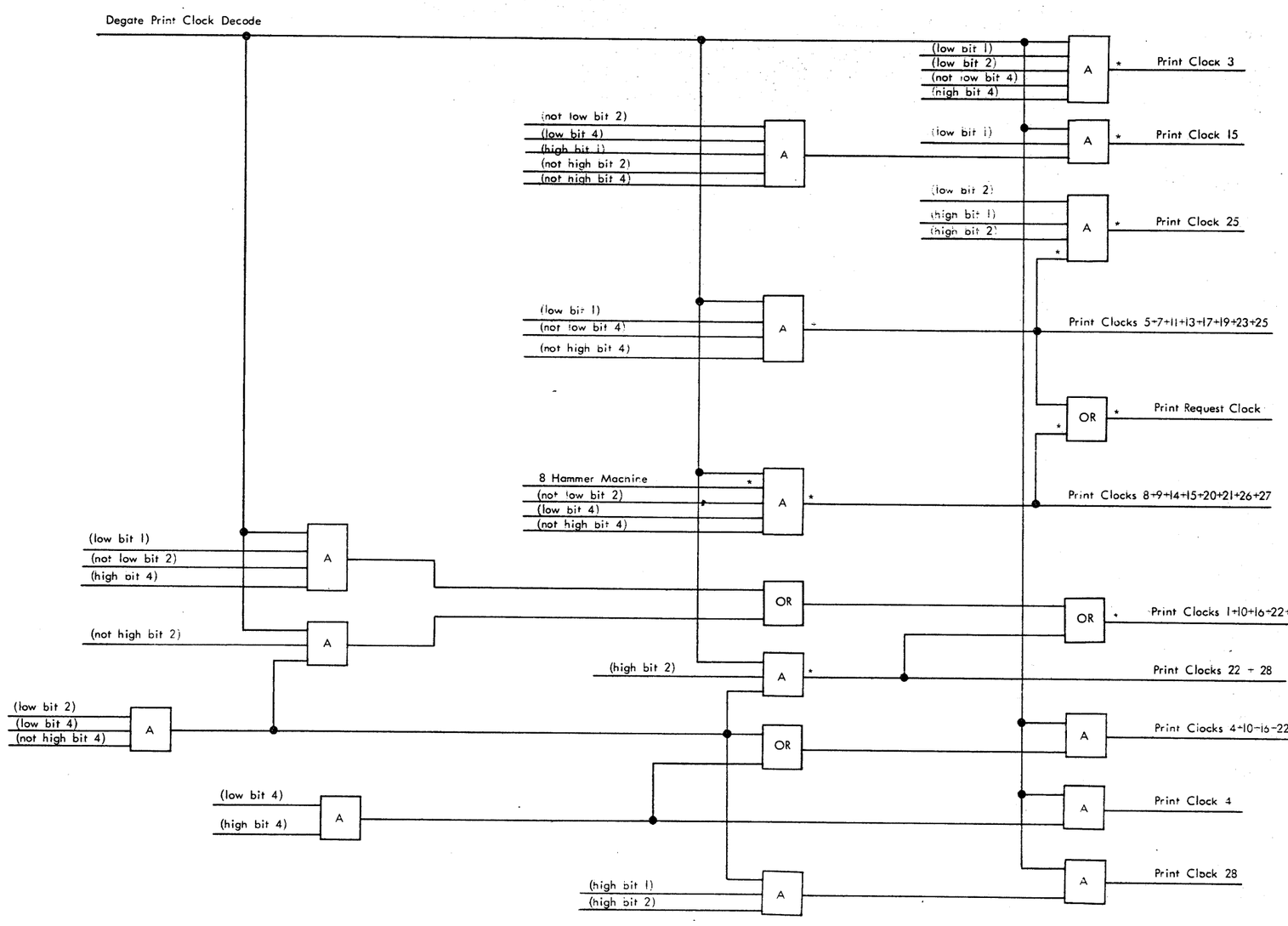


Diagram 4-060. Print Clock Decode

2 3 4 5 6 7 8 9

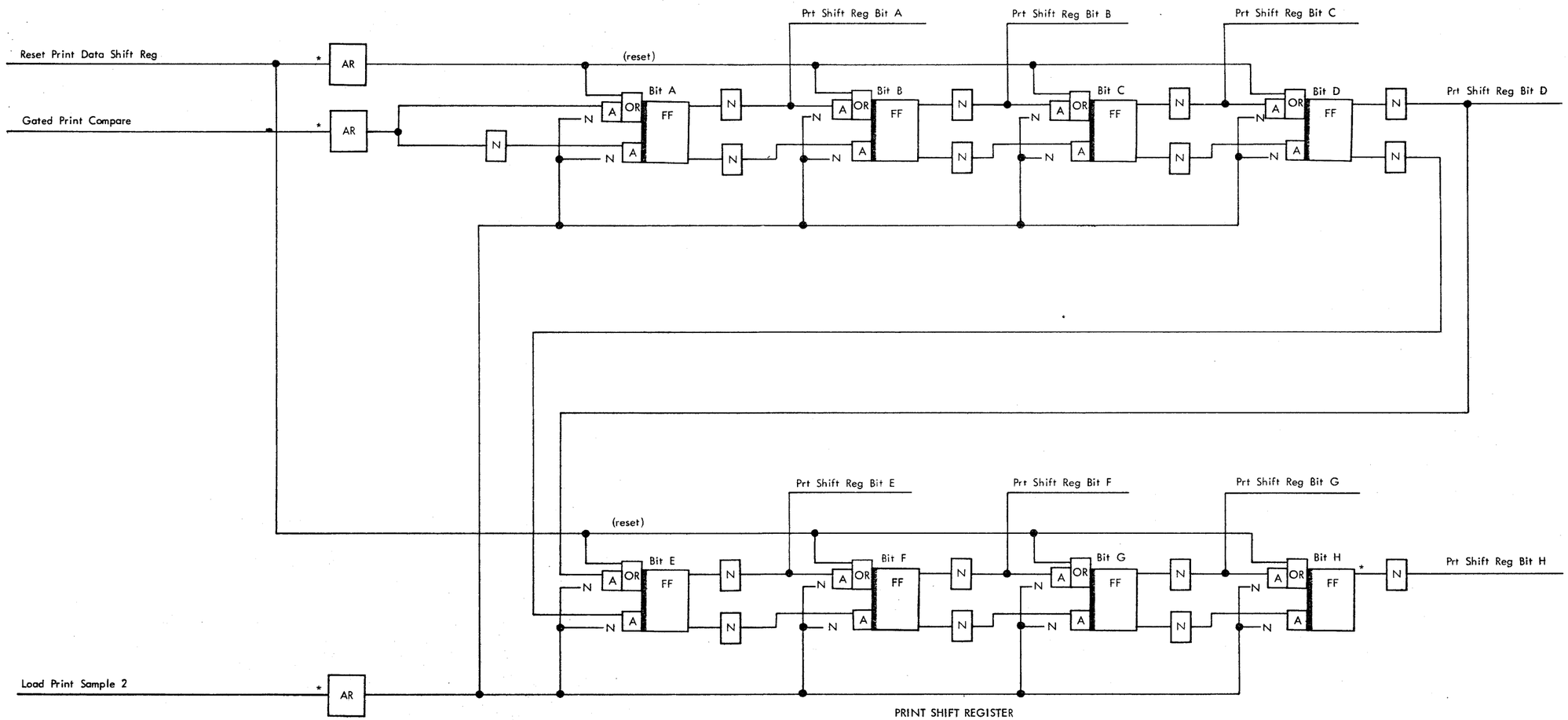
A

B

C

D

E



FD 302

PRINT SHIFT REGISTER

The print shift register has 16 bit positions (model A2 machines). On model A1 machines the print shift register has 8 bit positions. The character count that represents a specific character on the 16 (or eight) typewheels is compared with each corresponding character code stored in core storage. Sixteen (or eight) comparisons are made for each character count value. (Note that the same character is ready to be printed by each typewheel for each count value.) As the comparisons are made, the compare result is sent to the attachment over DBO. The 'gated print compare' (or no compare) is gated into the print shift register. Each 'load print sample 2' and 'load print sample 1' signals shifts the data in the shift register one bit position (See 4-070 and 4-072). After 16 (or eight) comparisons are completed, the data is gated into the print data register buffer. From the buffer the data is set directly in the print data register. The set always overrides the reset. The print data register output positions are then gated by the 'print time switch' signal to energize the print magnet hammers. After printing of the first character group, the print data register and the shift register are reset. The logic circuits are ready to receive comparison signals from the next character count sent to the CPU from the print character counter.

2 3 4 5 6 7 8 9

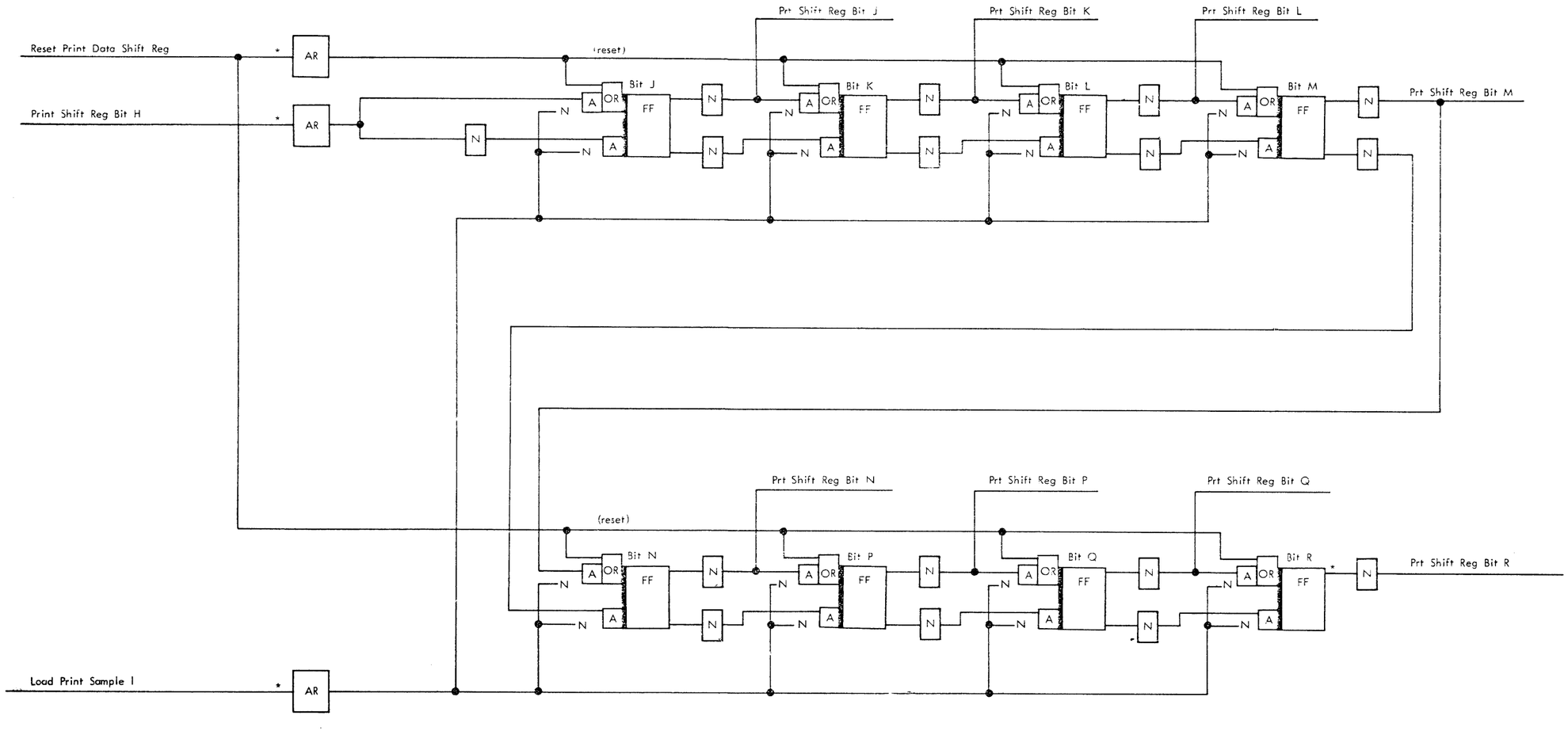
A

B

C

D

E



FD 352

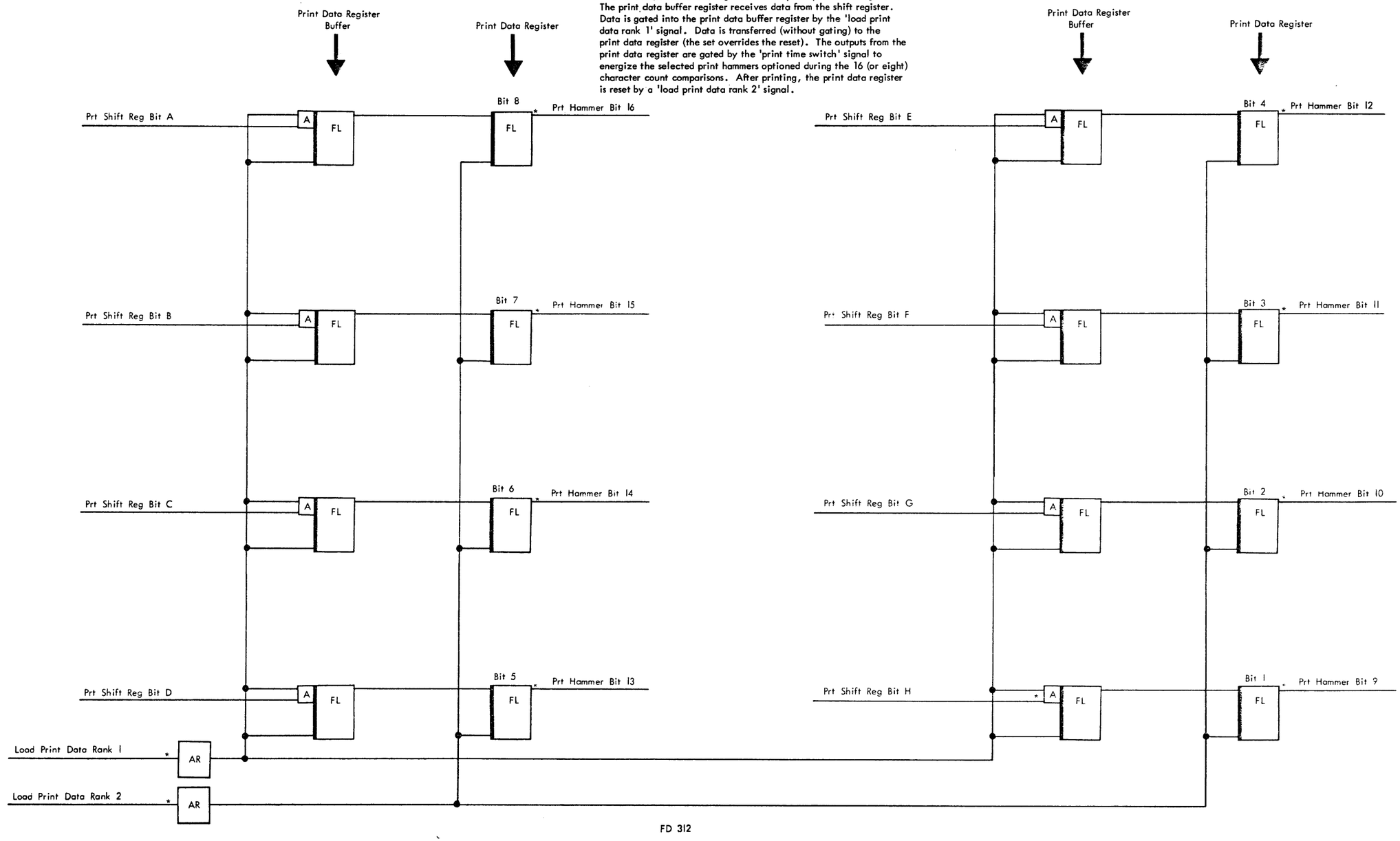
Diagram 4-067. Print Data Shift Register (Part 2 of 2)

2 3 4 5 6 7 8 9

A B C D E

PRINT DATA REGISTERS

Two 16-bit (or two 8-bit) registers make up the print data registers. The print data buffer register receives data from the shift register. Data is gated into the print data buffer register by the 'load print data rank 1' signal. Data is transferred (without gating) to the print data register (the set overrides the reset). The outputs from the print data register are gated by the 'print time switch' signal to energize the selected print hammers optioned during the 16 (or eight) character count comparisons. After printing, the print data register is reset by a 'load print data rank 2' signal.



FD 312

2 3 4 5 6 7 8 9

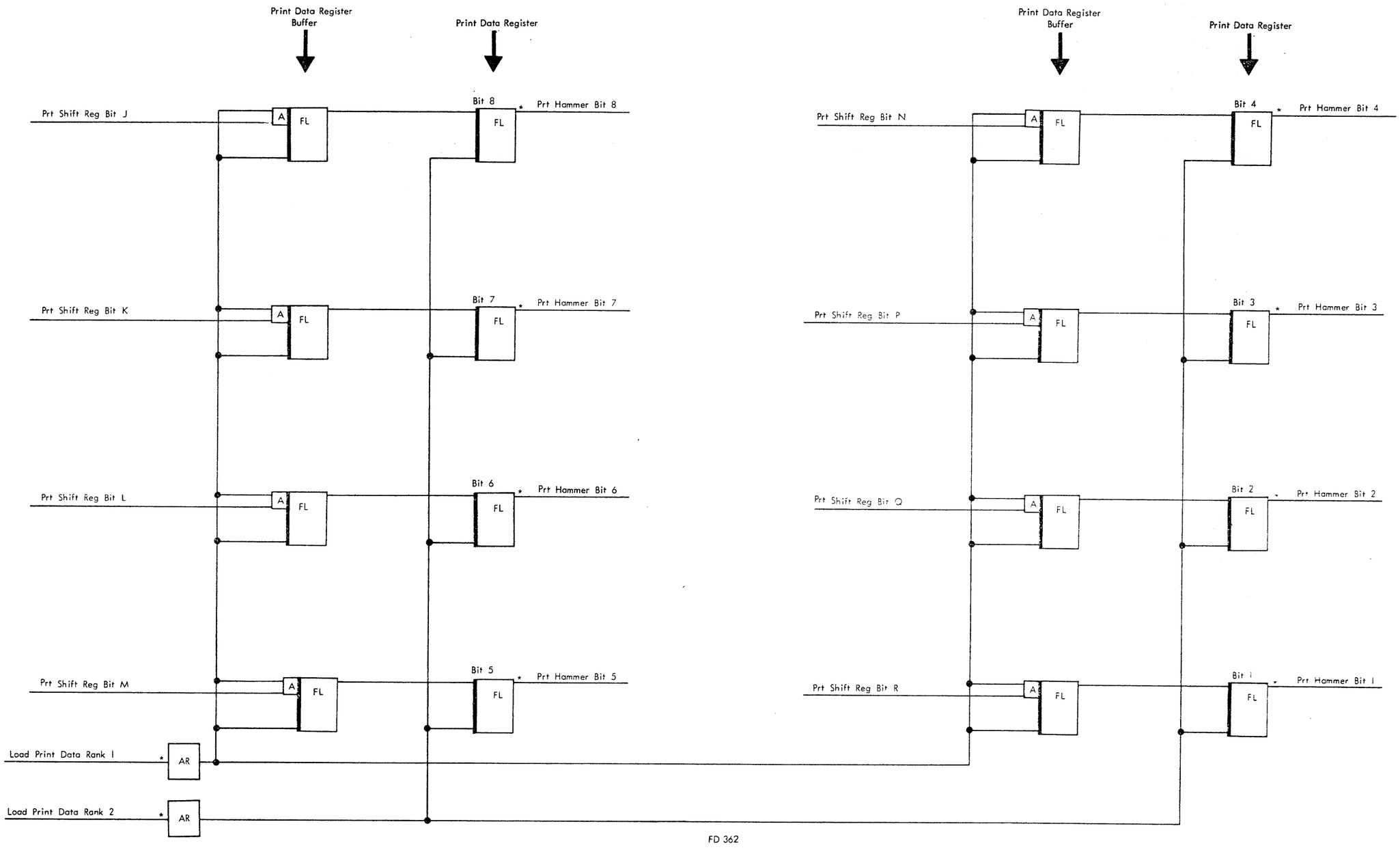
A

B

C

D

E



FD 362

Diagram 4-072. Print Data Register (Part 2 of 2)

2 3 4 5 6 7 8 9

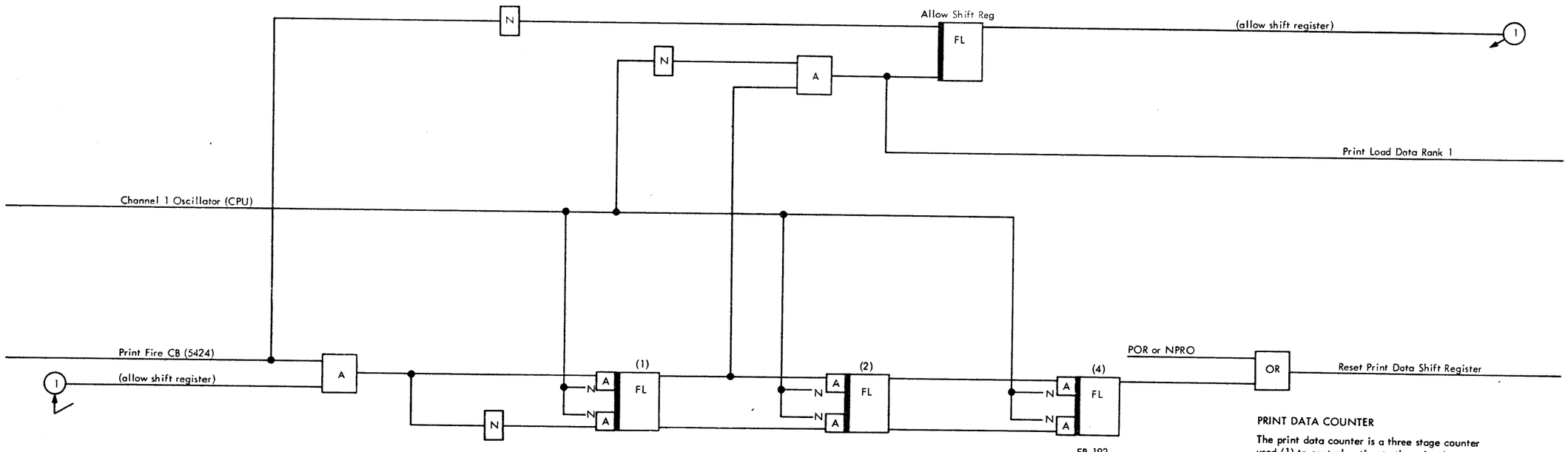
A

B

C

D

E

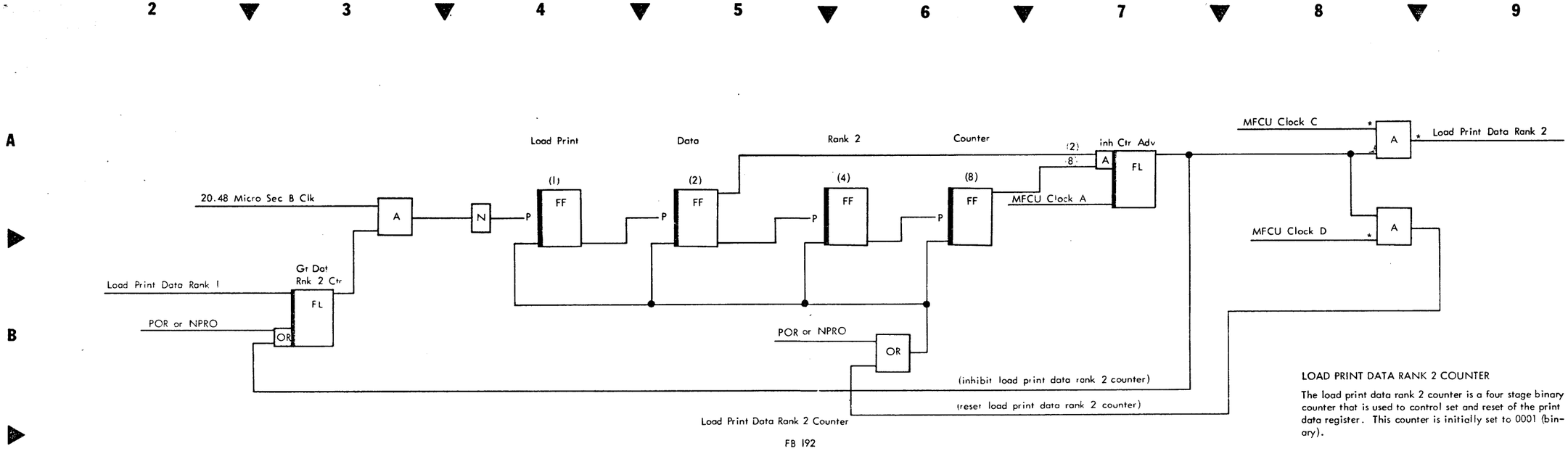


Print Data Counter
FB192

PRINT DATA COUNTER

The print data counter is a three stage counter used (1) to control gating to the print data register buffer, (2) to reset the print shift register and (3) to enable the load print data rank 2 counter.

Diagram 4-074. Print Data Counter

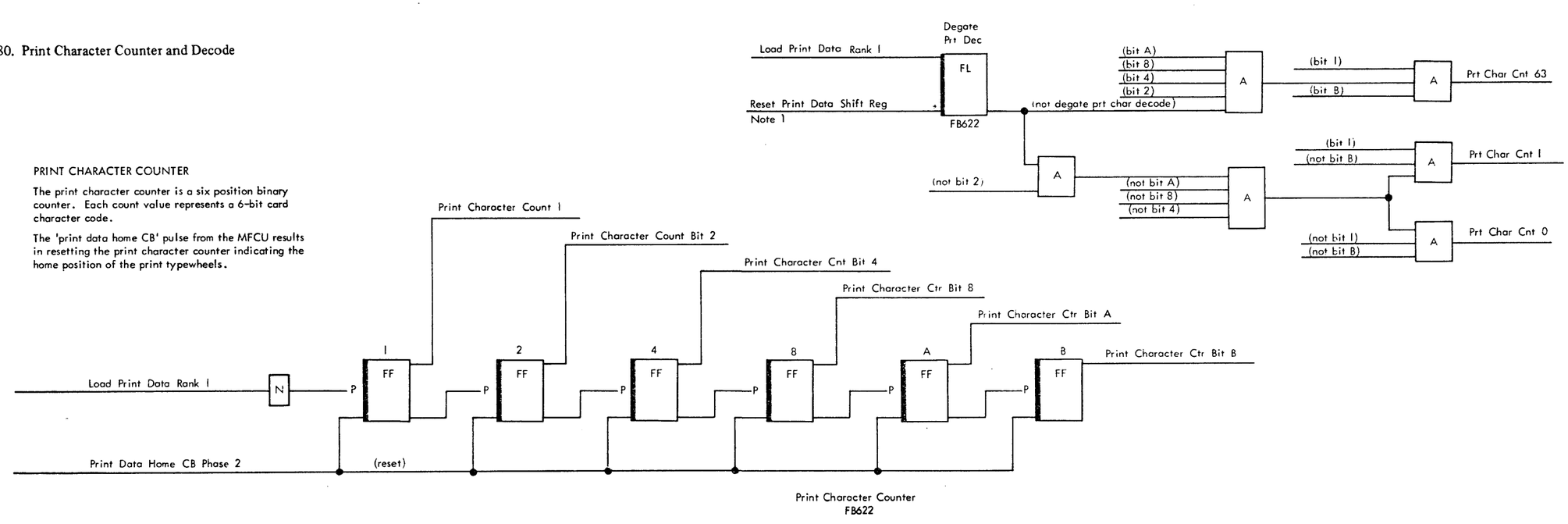


LOAD PRINT DATA RANK 2 COUNTER

The load print data rank 2 counter is a four stage binary counter that is used to control set and reset of the print data register. This counter is initially set to 0001 (binary).

C

Diagram 4-080. Print Character Counter and Decode



PRINT CHARACTER COUNTER

The print character counter is a six position binary counter. Each count value represents a 6-bit card character code.

The 'print data home CB' pulse from the MFCU results in resetting the print character counter indicating the home position of the print typewheels.

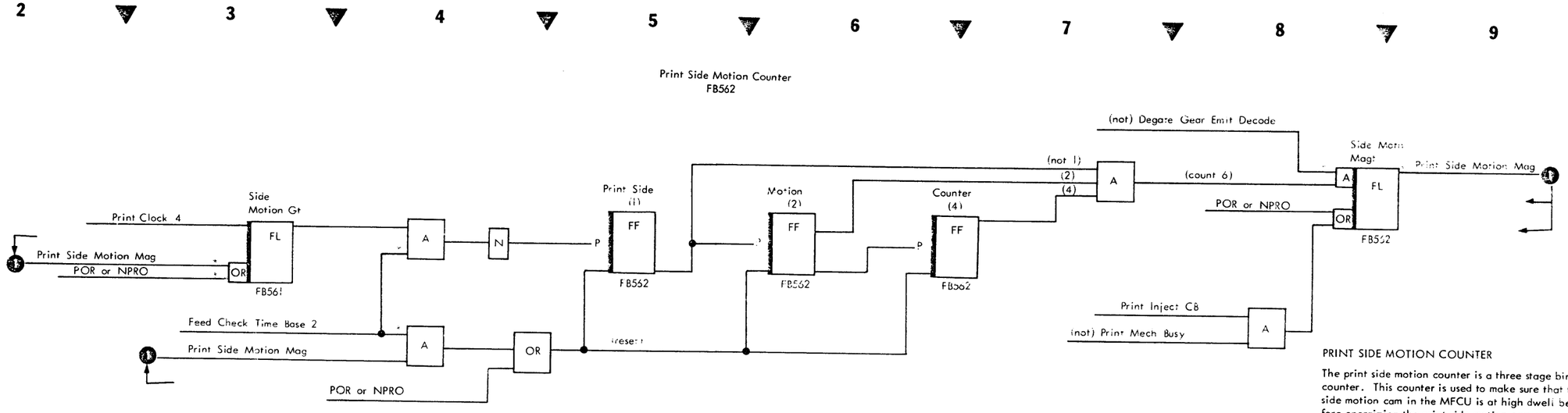


Diagram 4-085. Print Side Motion Counter and Decode

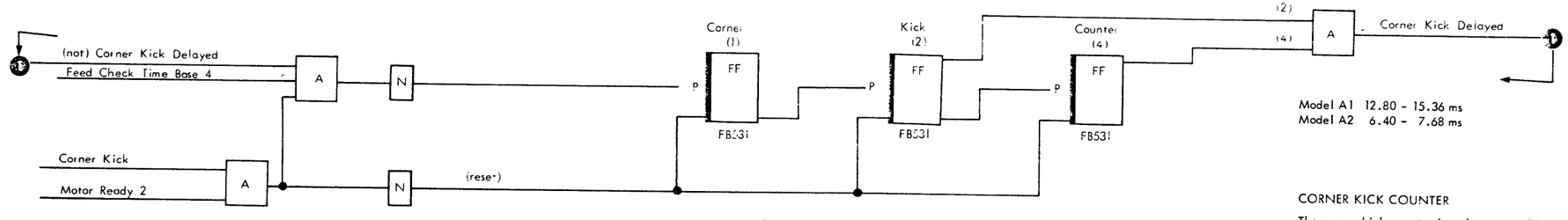


Diagram 4-090. Corner Kick Counter

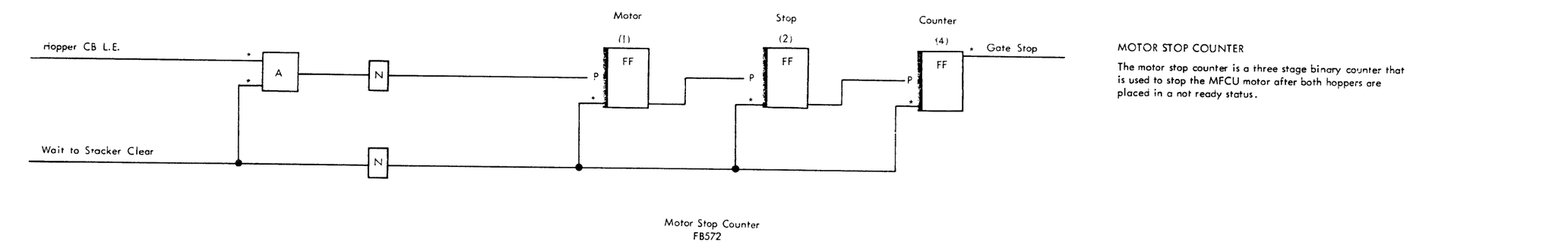
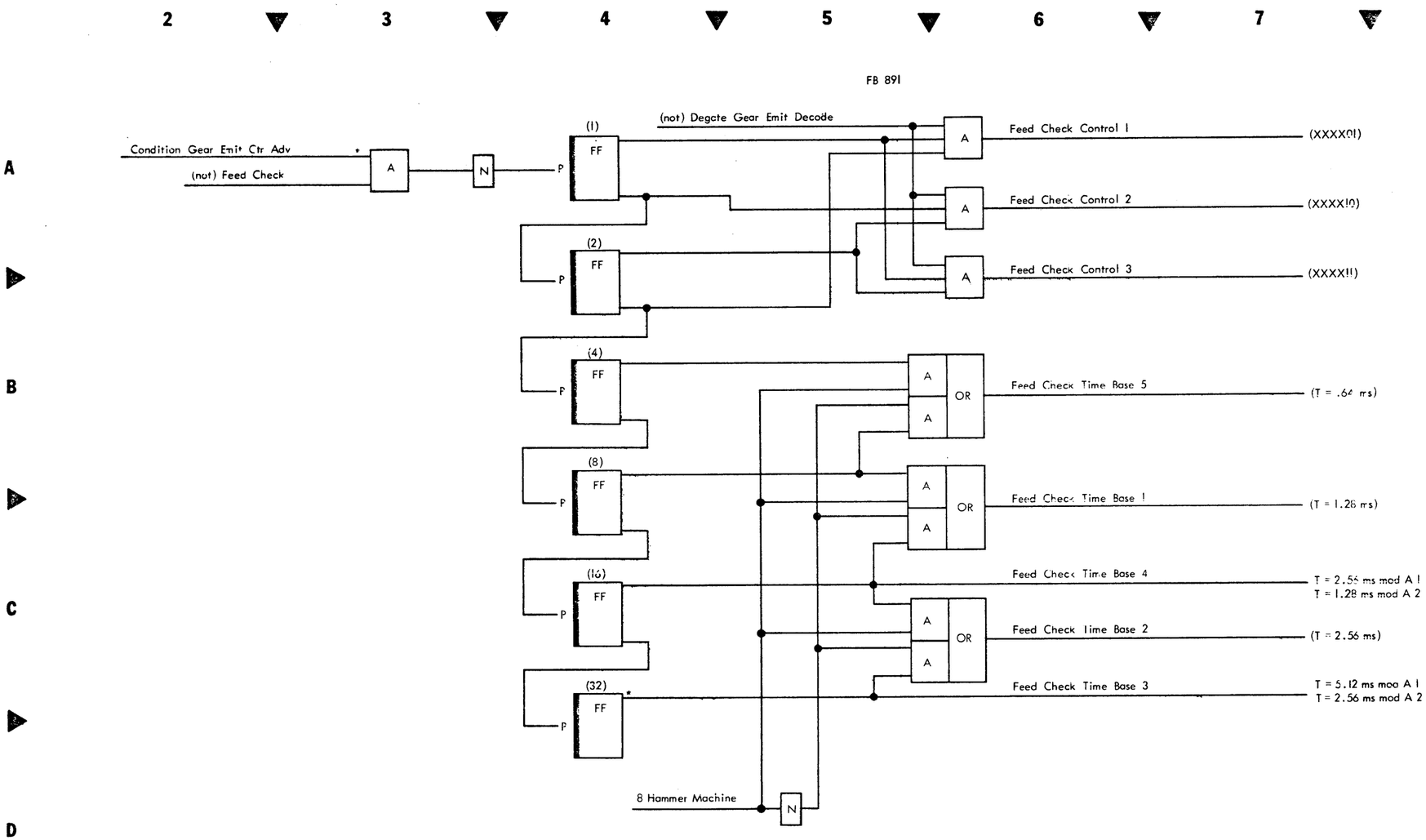


Diagram 4-095. Motor Stop Counter



FEED CHECK TIME BASE COUNTER

The feed check time base counter is a six stage binary counter that counts from zero to 63, resets and begins counting from zero. This counter is stepped every 80 microseconds for model A1 machines (40 microseconds for model A2 machines) by the 'condition gear emitter counter advance' signal.

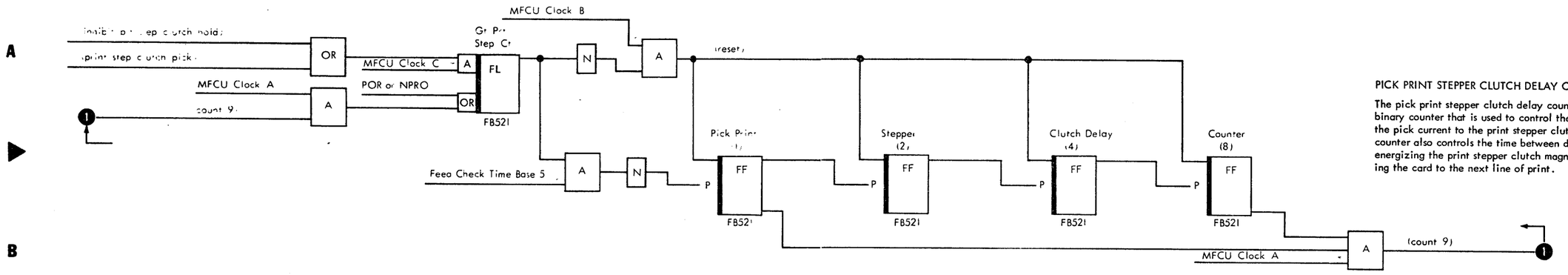
Counter positions 1 and 2 feed decode circuits to generate three feed check control levels:

1. Feed check control 1.
2. Feed check control 2.
3. Feed check control 3.

These control signals are used along with the feed check time base signals to indicate card progression through the transport. The feed check control levels are used to control and gate various feed check circuits.

The decode circuits are degated whenever the counter is being stepped. Counter positions 4, 8, 16, and 32 feed the feed check time base decode circuits to generate five feed check time base signals. These time base signals are used to drive the various feed check counters (hopper, wait, corner, and stacker) for feed checking.

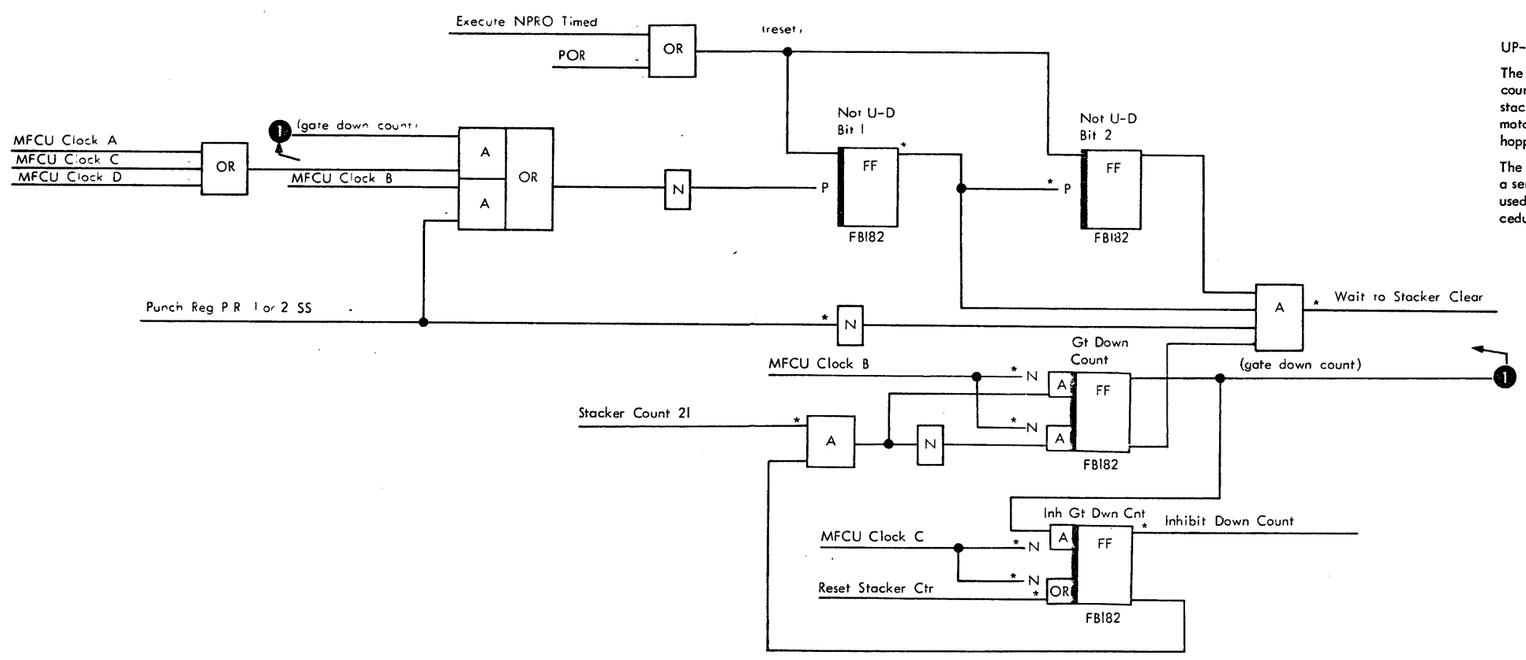
Feed Check Time Base	FF set for 8 hammer Machines	FF set for 16 hammer Machines	Time in Milliseconds	
			Model 1	Model 2
Feed Check Time Base 1	8	16	1.28	1.28
Feed Check Time Base 2	16	32	2.56	2.56
Feed Check Time Base 3	32	32	5.12	2.56
Feed Check Time Base 4	16	16	2.56	1.28
Feed Check Time Base 5	4	8	.64	.64



PICK PRINT STEPPER CLUTCH DELAY COUNTER

The pick print stepper clutch delay counter is a four stage binary counter that is used to control the time duration of the pick current to the print stepper clutch magnets. This counter also controls the time between de-energizing and energizing the print stepper clutch magnets while advancing the card to the next line of print.

Diagram 4-105. Pick Print Stepper Clutch Delay Counter

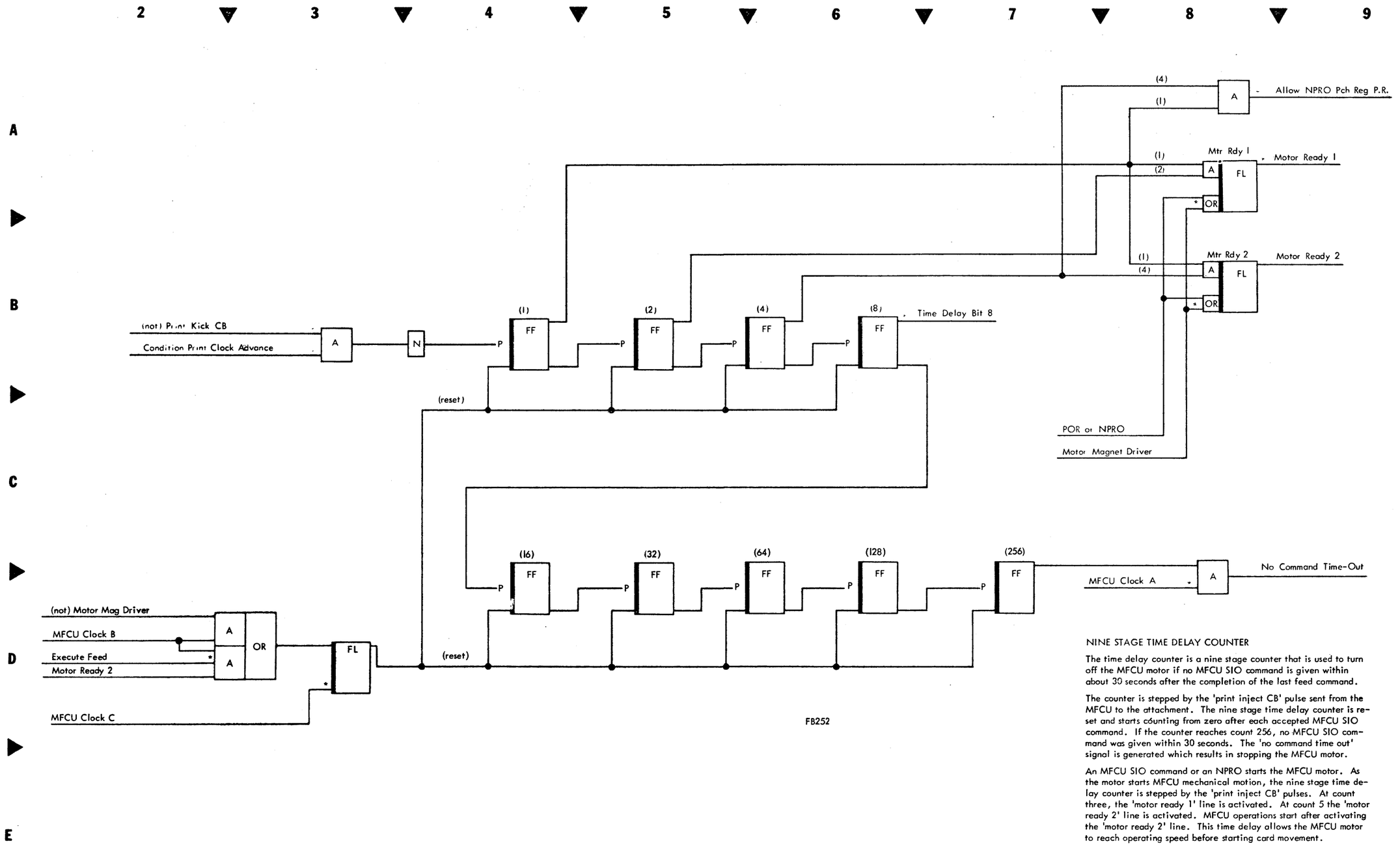


UP-DOWN COUNTER

The up-down counter is a two stage binary counter that is used to generate the 'wait to stacker clear' signal. This signal allows the motor stop counter to be stepped by each hopper CB pulse (See 4-095).

The up-down counter value can be stored by a sense command. The counter value is then used by the program to determine restart procedures after an MFCU error.

Diagram 4-110. Up-Down Counter



NINE STAGE TIME DELAY COUNTER

The time delay counter is a nine stage counter that is used to turn off the MFCU motor if no MFCU SIO command is given within about 30 seconds after the completion of the last feed command.

The counter is stepped by the 'print inject CB' pulse sent from the MFCU to the attachment. The nine stage time delay counter is reset and starts counting from zero after each accepted MFCU SIO command. If the counter reaches count 256, no MFCU SIO command was given within 30 seconds. The 'no command time out' signal is generated which results in stopping the MFCU motor.

An MFCU SIO command or an NPRO starts the MFCU motor. As the motor starts MFCU mechanical motion, the nine stage time delay counter is stepped by the 'print inject CB' pulses. At count three, the 'motor ready 1' line is activated. At count 5 the 'motor ready 2' line is activated. MFCU operations start after activating the 'motor ready 2' line. This time delay allows the MFCU motor to reach operating speed before starting card movement.

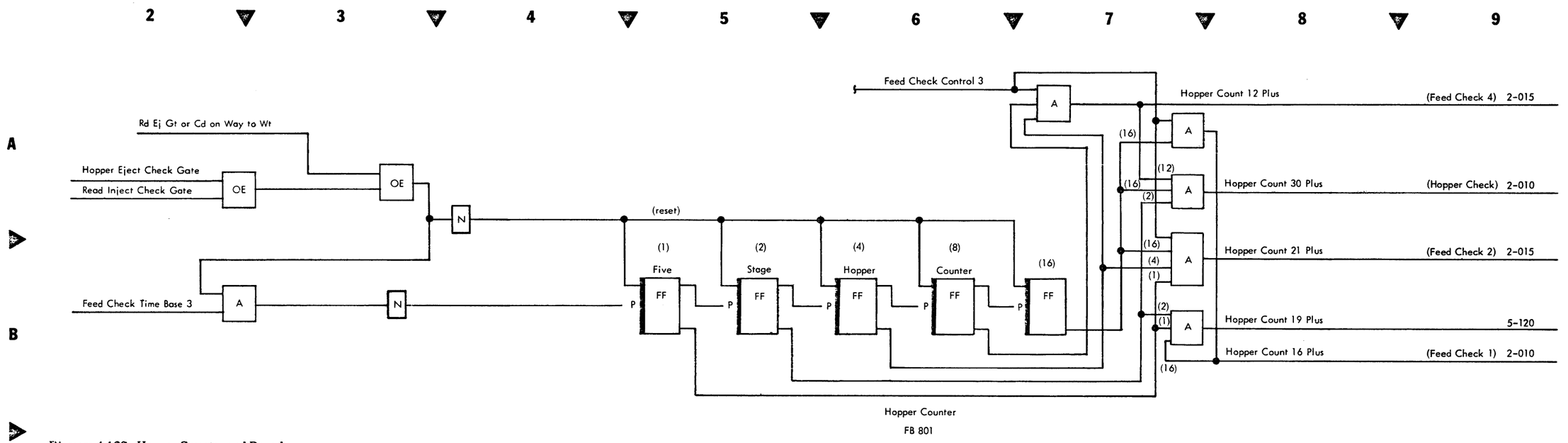


Diagram 4-120. Hopper Counter and Decode

Diagram 4-125. Wait Counter and Decode

2 3 4 5 6 7 8 9

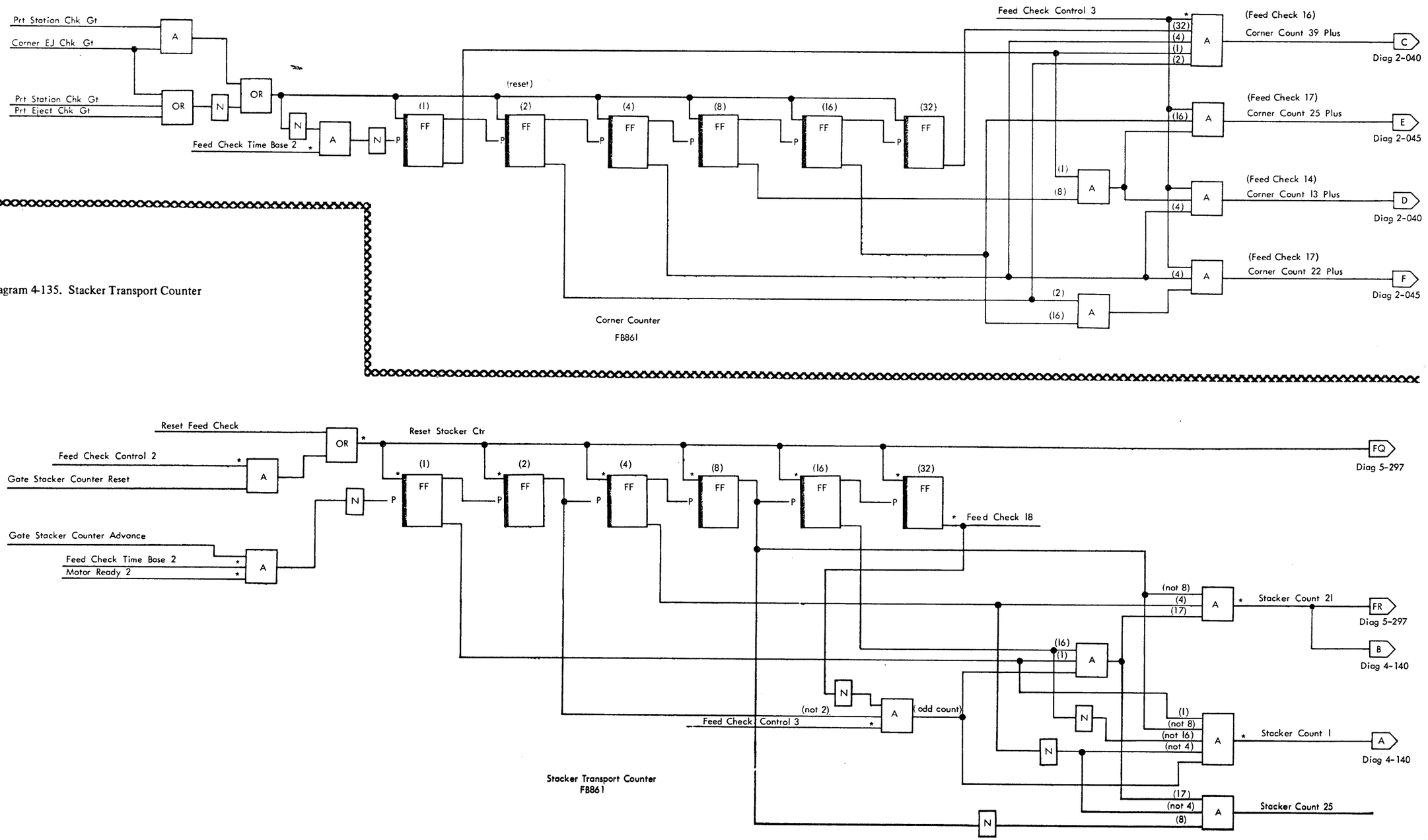
A

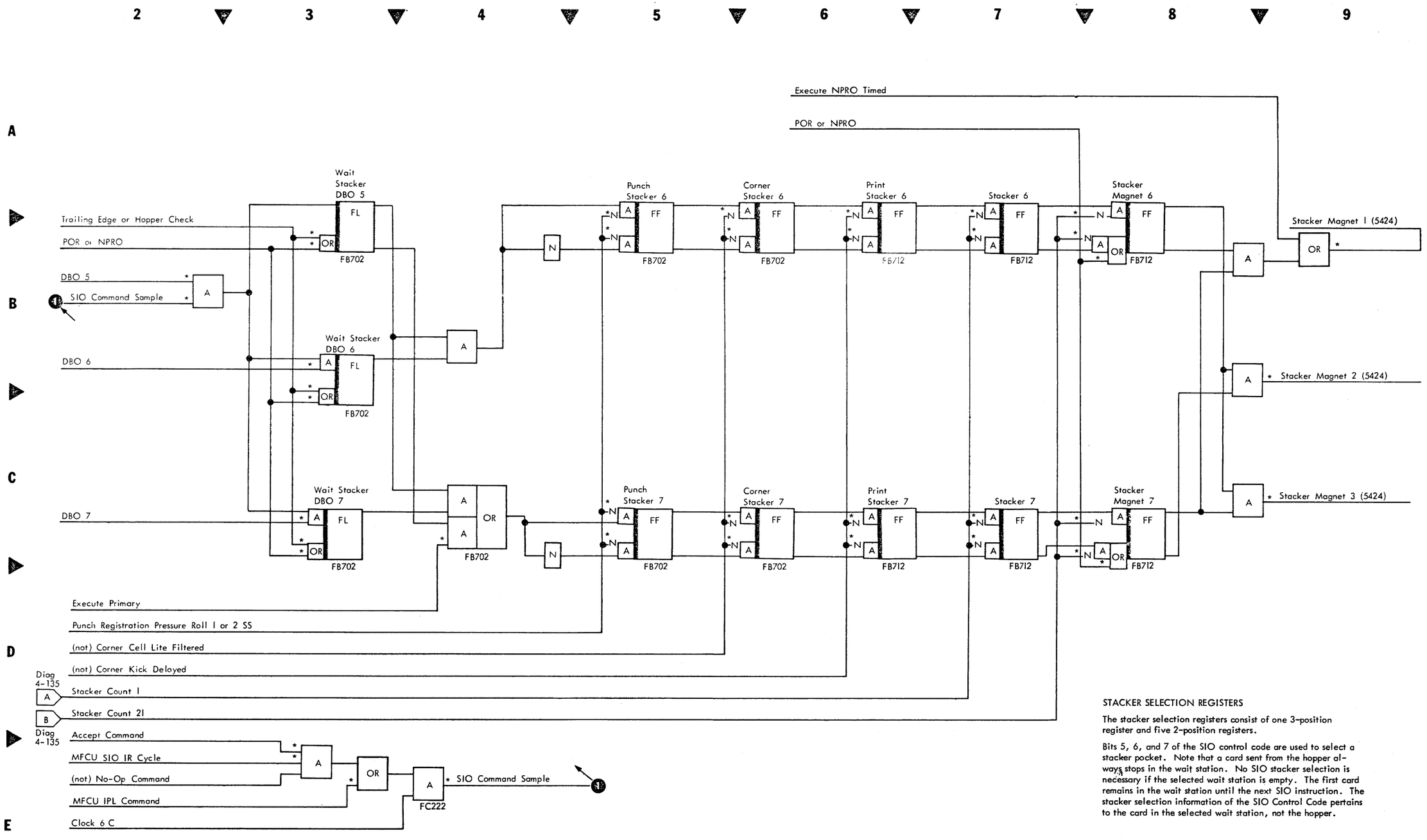
B

C

D

E





STACKER SELECTION REGISTERS

The stacker selection registers consist of one 3-position register and five 2-position registers.

Bits 5, 6, and 7 of the SIO control code are used to select a stacker pocket. Note that a card sent from the hopper always stops in the wait station. No SIO stacker selection is necessary if the selected wait station is empty. The first card remains in the wait station until the next SIO instruction. The stacker selection information of the SIO Control Code pertains to the card in the selected wait station, not the hopper.

DBO			Wait Stacker			Primary Feed	Secondary Feed	Punch Stacker		Corner Stacker		Print Stacker		Stacker		Stacker Magnet		Stacker Pocket Selected
5	6	7	5	6	7	Selected	Selected	6	7	6	7	6	7	6	7	6	7	
0	0	0	0	0	0	X		0	1	0	1	0	1	0	1	0	1	1
0	0	0	0	0	0		X	0	0	0	0	0	0	0	0	0	0	4
0	0	1	0	0	0	X		0	1	0	1	0	1	0	1	0	1	1
0	0	1	0	0	0		X	0	0	0	0	0	0	0	0	0	0	4
0	1	0	0	0	0	X		0	1	0	1	0	1	0	1	0	1	1
0	1	0	0	0	0		X	0	0	0	0	0	0	0	0	0	0	4
0	1	1	0	0	0	X		0	1	0	1	0	1	0	1	0	1	1
0	1	1	0	0	0		X	0	0	0	0	0	0	0	0	0	0	4
1	0	0	1	0	0	X	X	0	0	0	0	0	0	0	0	0	0	4
1	0	1	1	0	1	X	X	0	1	0	1	0	1	0	1	0	1	1
1	1	0	1	1	0	X	X	1	0	1	0	1	0	1	0	1	0	2
1	1	1	1	1	1	X	X	1	1	1	1	1	1	1	1	1	1	3

Note: An NPRO operation selects stacker pocket 1.

2 3 4 5 6 7 8 9

A

B

C

D

E

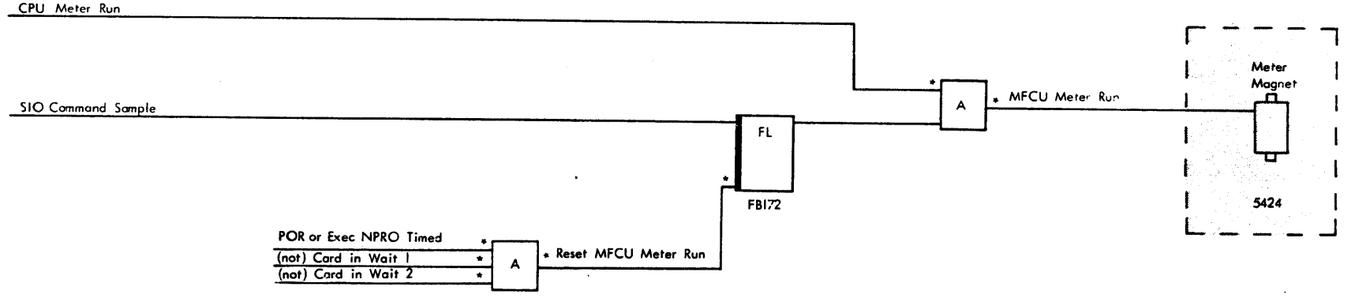
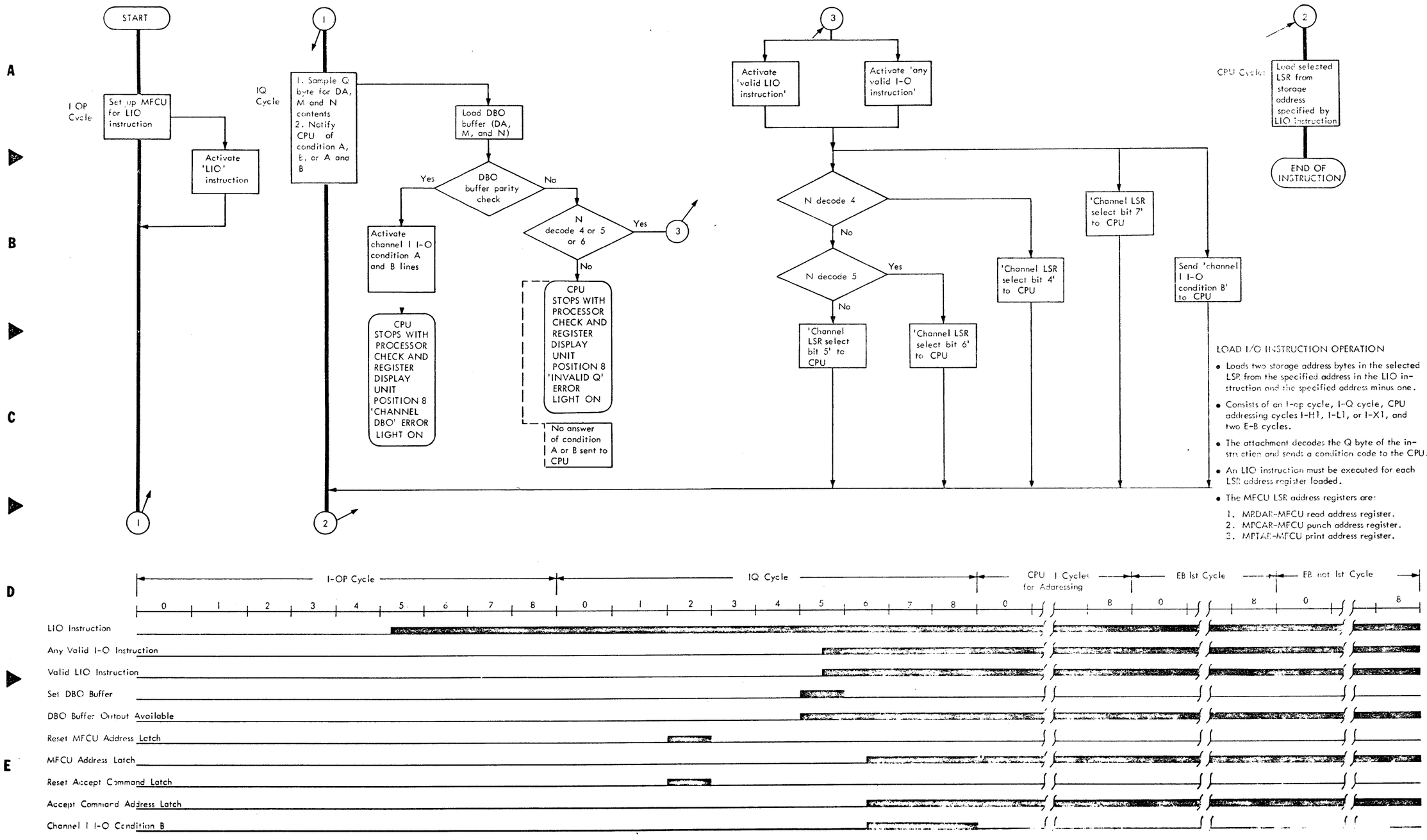


Diagram 4-150. MFCU Meter Control


2
3
4
5
6
7
8
9
A
B
C
D
E
START
I OP Cycle
Set up MFCU for LIO instruction
Activate 'LIO' instruction
IQ Cycle
1. Sample Q byte for DA, M and N contents
2. Notify CPU of condition A, B, or A and B
Load DBO buffer (DA, M, and N)
DBO buffer parity check
Yes
No
Activate channel I I-O condition A and B lines
CPU STOPS WITH PROCESSOR CHECK AND REGISTER DISPLAY UNIT POSITION 8 'CHANNEL DBO' ERROR LIGHT ON
N decode 4 or 5 or 6
Yes
No
CPU STOPS WITH PROCESSOR CHECK AND REGISTER DISPLAY UNIT POSITION 8 'INVALID Q' ERROR LIGHT ON
No answer of condition A or B sent to CPU
Activate 'valid LIO instruction'
Activate 'any valid I-O instruction'
N decode 4
N decode 5
'Channel LSR select bit 5' to CPU
'Channel LSR select bit 6' to CPU
'Channel LSR select bit 4' to CPU
'Channel LSR select bit 7' to CPU
Send 'channel I I-O condition B' to CPU
CPU Cycle
Load selected LSR from storage address specified by LIO instruction
END OF INSTRUCTION
LOAD I/O INSTRUCTION OPERATION
• Loads two storage address bytes in the selected LSR from the specified address in the LIO instruction and the specified address minus one.
• Consists of an I-op cycle, I-Q cycle, CPU addressing cycles I-H1, I-L1, or I-X1, and two E-B cycles.
• The attachment decodes the Q byte of the instruction and sends a condition code to the CPU.
• An LIO instruction must be executed for each LSR address register loaded.
• The MFCU LSR address registers are:
1. MRDAR-MFCU read address register.
2. MPCAR-MFCU punch address register.
3. MPTAR-MFCU print address register.
I-OP Cycle
IQ Cycle
CPU 1 Cycles for Addressing
EB 1st Cycle
EB not 1st Cycle
0 1 2 3 4 5 6 7 8 0 1 2 3 4 5 6 7 8 0 8 0 8 0 8
LIO Instruction
Any Valid I-O Instruction
Valid LIO Instruction
Set DBO Buffer
DBO Buffer Output Available
Reset MFCU Address Latch
MFCU Address Latch
Reset Accept Command Latch
Accept Command Address Latch
Channel I I-O Condition B

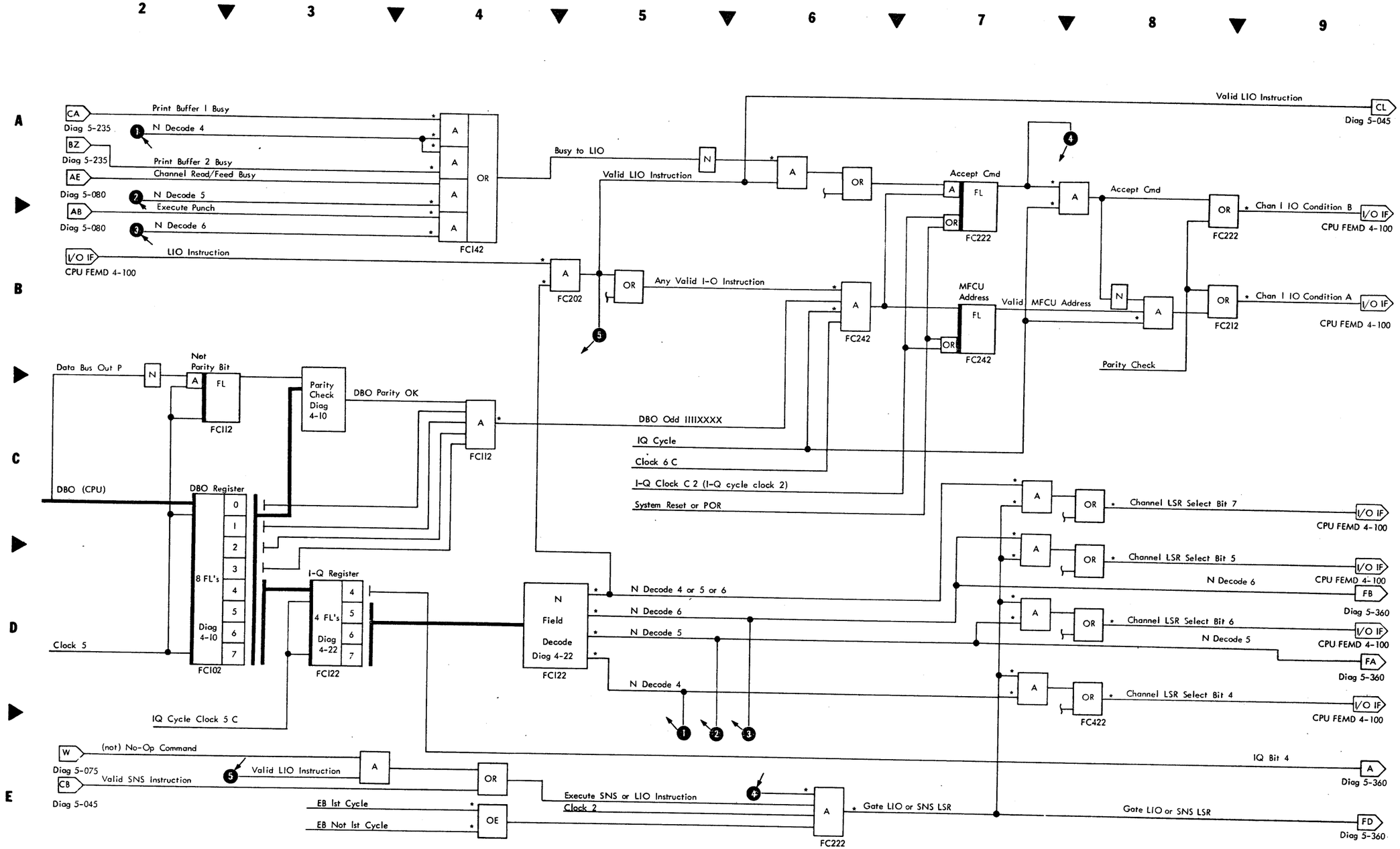
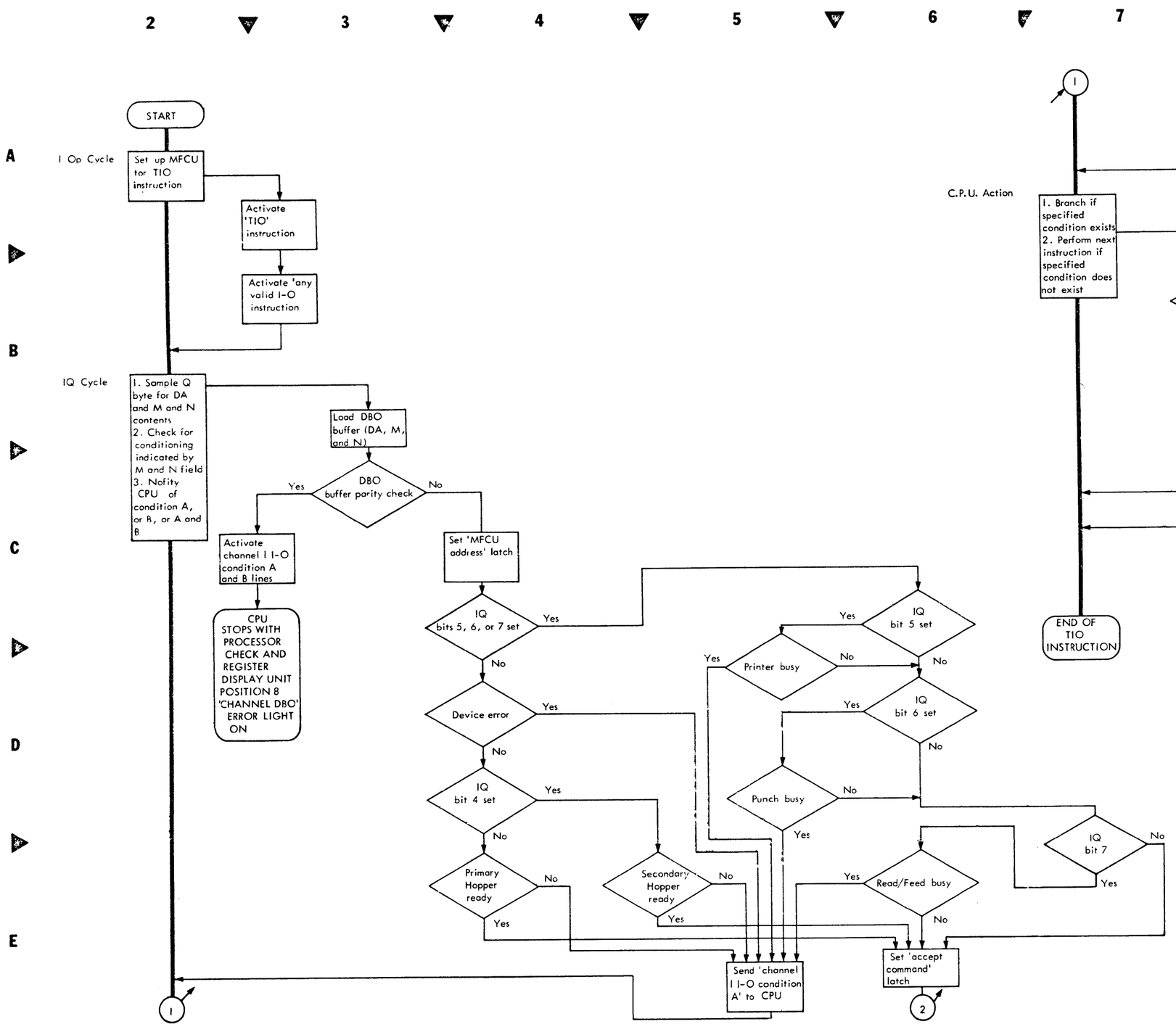


Diagram 5-010. LIO Instruction (Part 2 of 2)



TEST I/O AND BRANCH INSTRUCTION OPERATION

- Test for conditions specified by N code.
- Branch to address specified in branch address if condition is met.

Q Code DA	F	M	N	I-R Byte	
5424 MFCU		0			Device Address MFCU
		1			Primary
			000		Secondary
			001		Feed not ready or error
			010		Read feed busy (condition 1)
			011		Punch data busy (condition 2)
			100		Condition 1 or 2
			101		Print data busy (condition 4)
			110		Condition 1 or 4
			111		Condition 2 or 4
				xxxx xxxx	Condition 1, 2, or 4
					Branch to address if condition met
					Op codes D1 and E1 are indexed

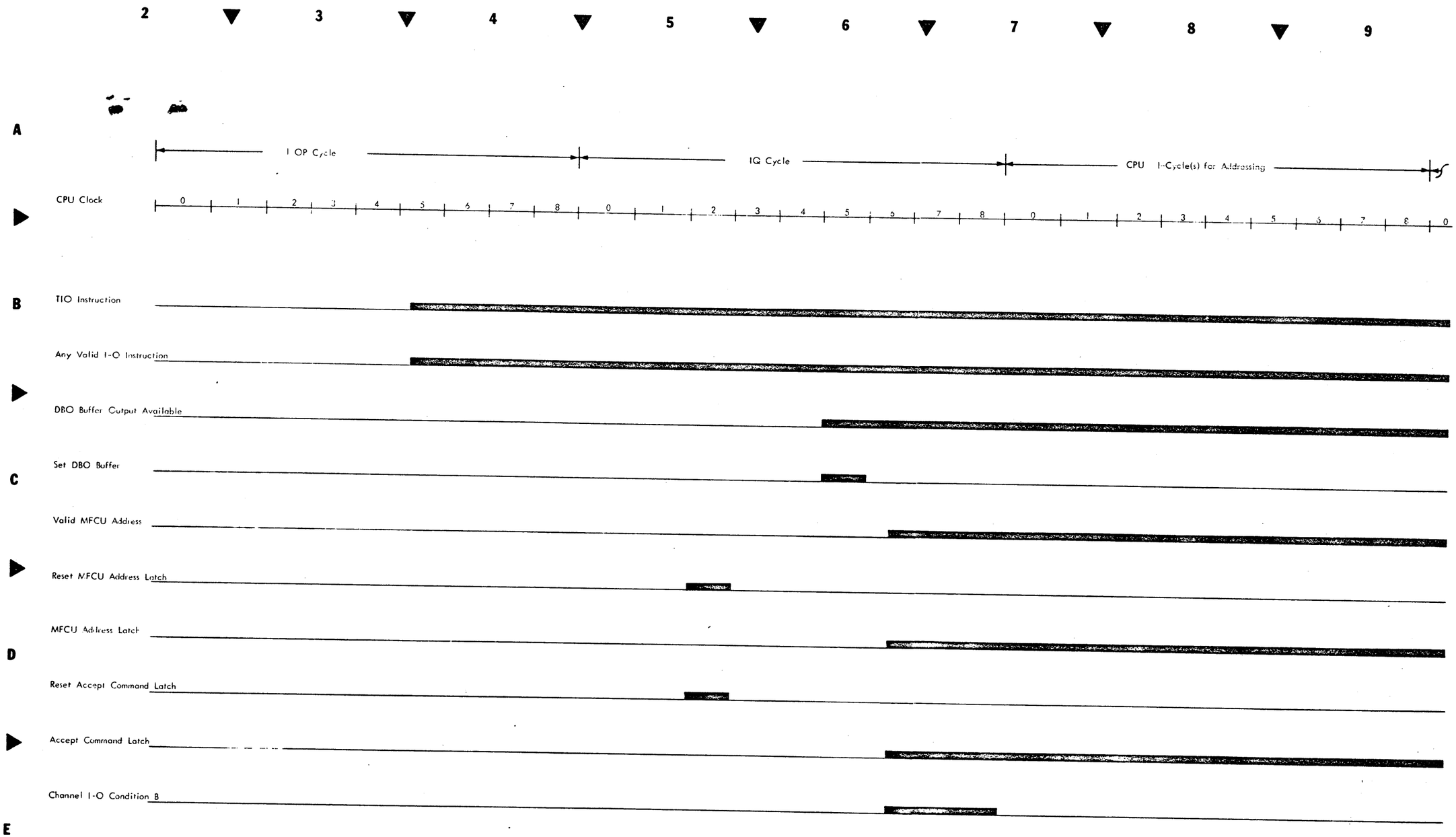
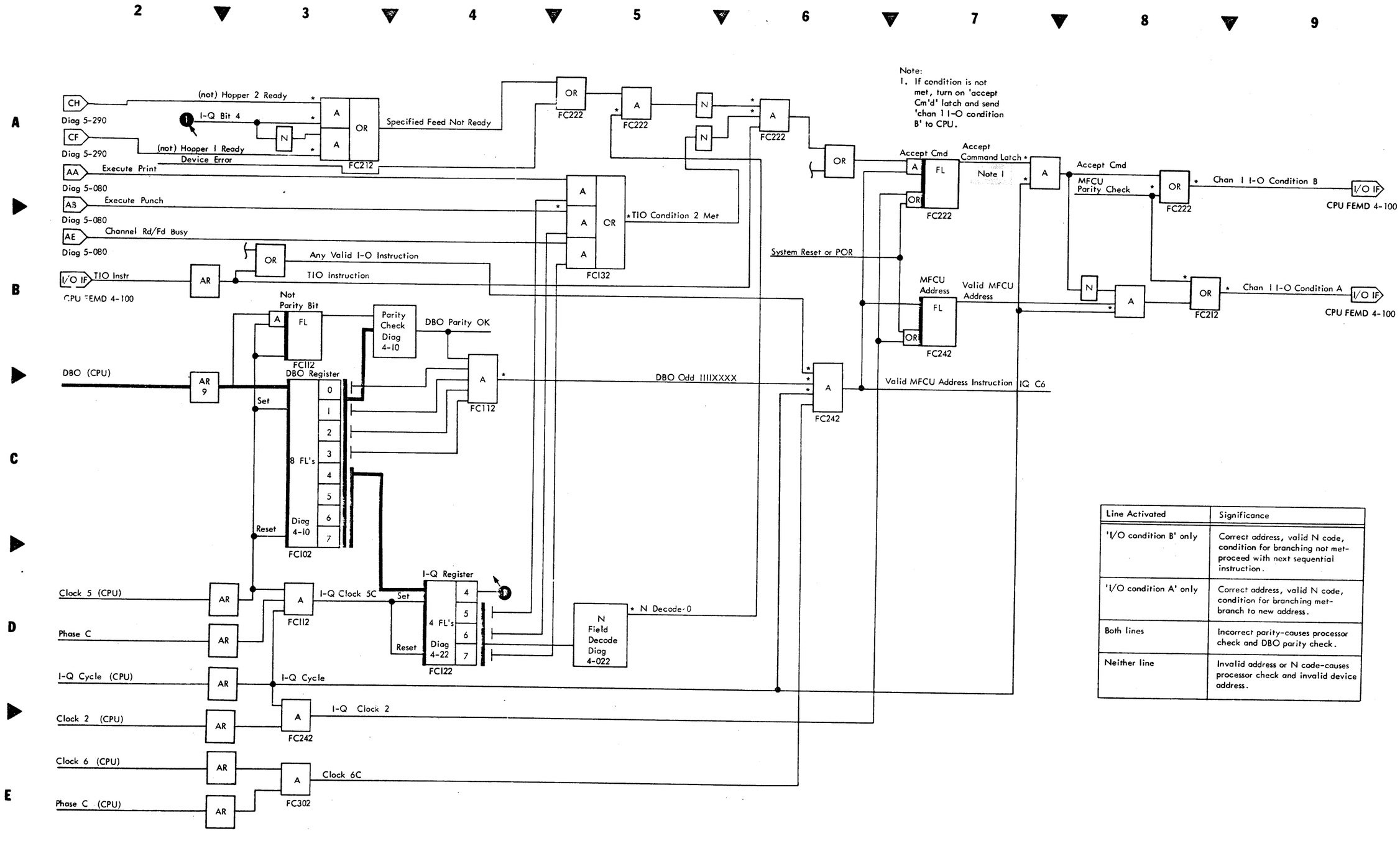


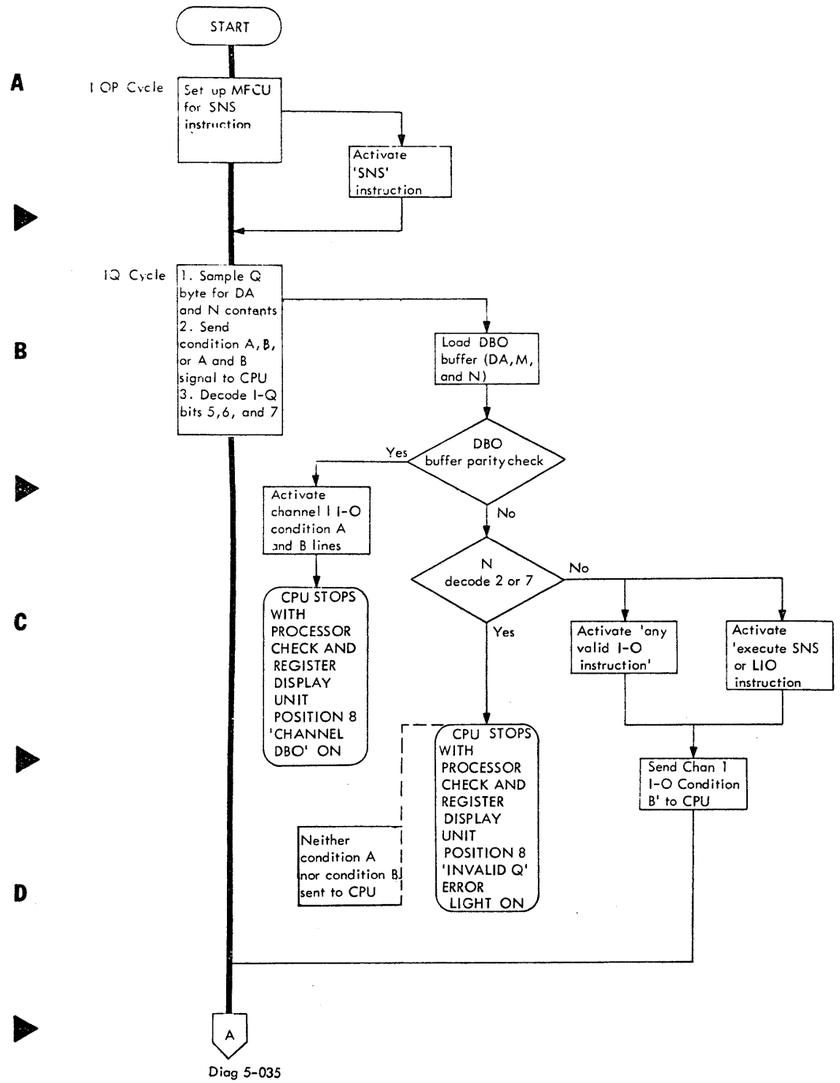
Diagram 5-020. Test I/O and Branch Timing Chart (Part 2 of 3)



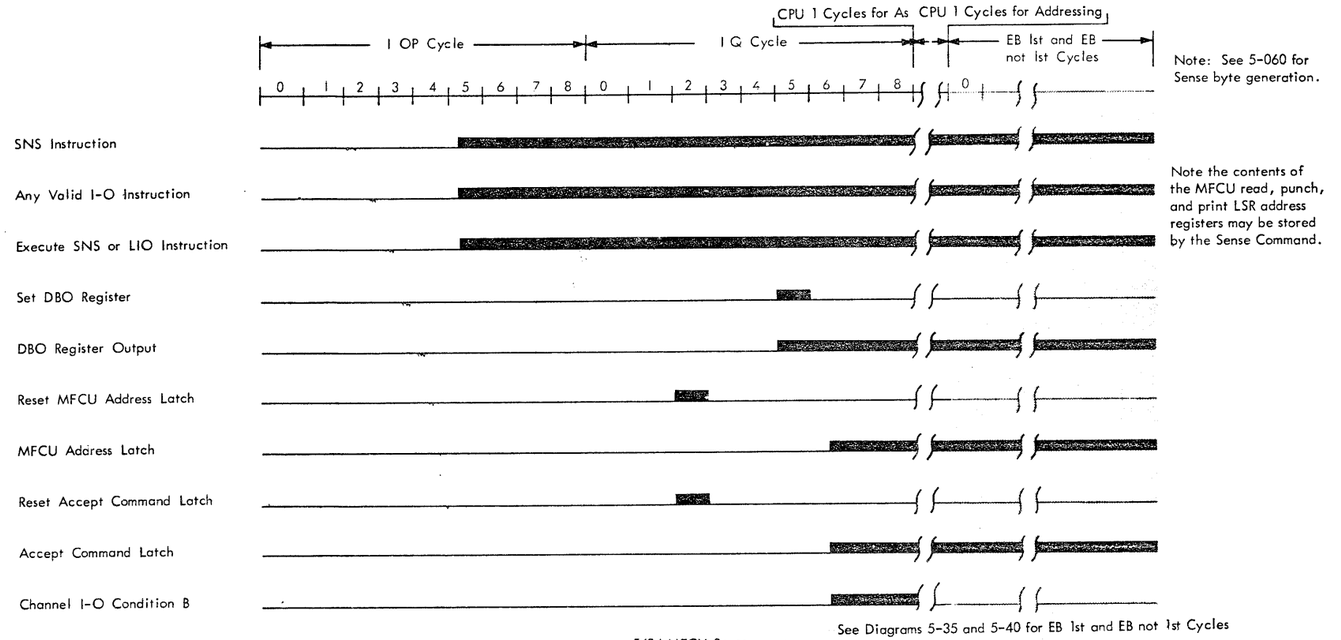
Line Activated	Significance
'I/O condition B' only	Correct address, valid N code, condition for branching not met-proceed with next sequential instruction.
'I/O condition A' only	Correct address, valid N code, condition for branching met-branch to new address.
Both lines	Incorrect parity-causes processor check and DBO parity check.
Neither line	Invalid address or N code-causes processor check and invalid device address.

Diagram 5-025. Test I/O and Branch Circuit Diagram (Part 3 of 3)

Diagram 5-030. Sense Instruction, I-Op and I-Q Cycles (Part 1 of 7)



Diag 5-035



Note: See 5-060 for Sense byte generation.

Note the contents of the MFCU read, punch, and print LSR address registers may be stored by the Sense Command.

See Diagrams 5-35 and 5-40 for EB 1st and EB not 1st Cycles

SENSE I/O INSTRUCTION OPERATION

The SNS instruction assembles two sense bytes and stores these two bytes in core storage. The program examines these sense bytes to determine MFCU and attachment status.

- Move two sense bytes from attachment to core storage.
- Instruction is always executed whether or not the device is busy or needs attention.
- Consists of an I-op cycle, an I-Q cycle, CPU addressing cycles, and two E-B cycles.
- I-Q cycle decodes the Q byte and sends a condition code of B back to the CPU.
- Two E-B cycles are taken to assemble the sense bytes and to send the sense data to the CPU.

5424 MFCU Sense

Op Code 0 7	Q Code DA 8 11	M 12	N 13 15	Operand 1 16 23		
3 0					Direct Addressing	Byte 1 = Operand Address
7 0					Indexed by XR1	Byte 2 = Operand Address - 1
B 0					Indexed by XR2	
	1111				Device Address for MFCU	
		0			Not used	
			000		Low Core Address Byte 2 (EB2)	High Core Address Byte 1 (EB1)
					0 Punch CB	0 Hopper 1 or 2 magnet
					1 Punch strobe	1 Hopper cell covered
					2 Punch magnet one	2 Gear count 1,3,5,7,9,11
					3 IND1 Byte 2 Bit 3	3 Read cell one exposed
					4 Print time	4 Read cell 18 exposed
					5 Print fire CB	5 Allow read
					6 Print magnet 1(A1) 9(A2)	6 Hopper CB
					7 Reserved	7 IND1 Byte 1 Bit 7
			001		0 Corner kick magnet	0 Punch registration roll 1 or 2
					1 Print stepper clutch magnet	1 Prepunch cell covered
					2 Post-print cell covered	2 Punch gate magnet
					3 Print inject CB	3 Punch eject roll magnet
					4 Print kick CB	4 Punch stepper roll magnet
					5 Print stepped CB	5 Corner cell covered
					6 Print allow, punch execute	6 Punch stepper CB
					7 IND2 Byte 2 Bit 7	7 IND2 Byte 1 Bit 7
			011		0 Print buffer 1 busy	0 Read check
					1 Print buffer 2 busy	1 Punch check
					2 Card in wait 1	2 Punch invalid
					3 Card in wait 2	3 Print data check
					4 Reserved	4 Print clutch check
					5 Hopper cycle not complete	5 Hopper check
					6 Card in transport counter Bit 2	6 Feed check
					7 Card in transport counter Bit 1	7 No Op
			010		Invalid	
			100		MFCU Print Address Register	Stores Register
			101		MFCU Read Address Register	Contents at
			110		MFCU Punch Address Register	Operand Address 1 and
			111		Invalid	Operand Address 1 minus one.
				xxxxxxxx	Operand address (Sense bytes destination)	

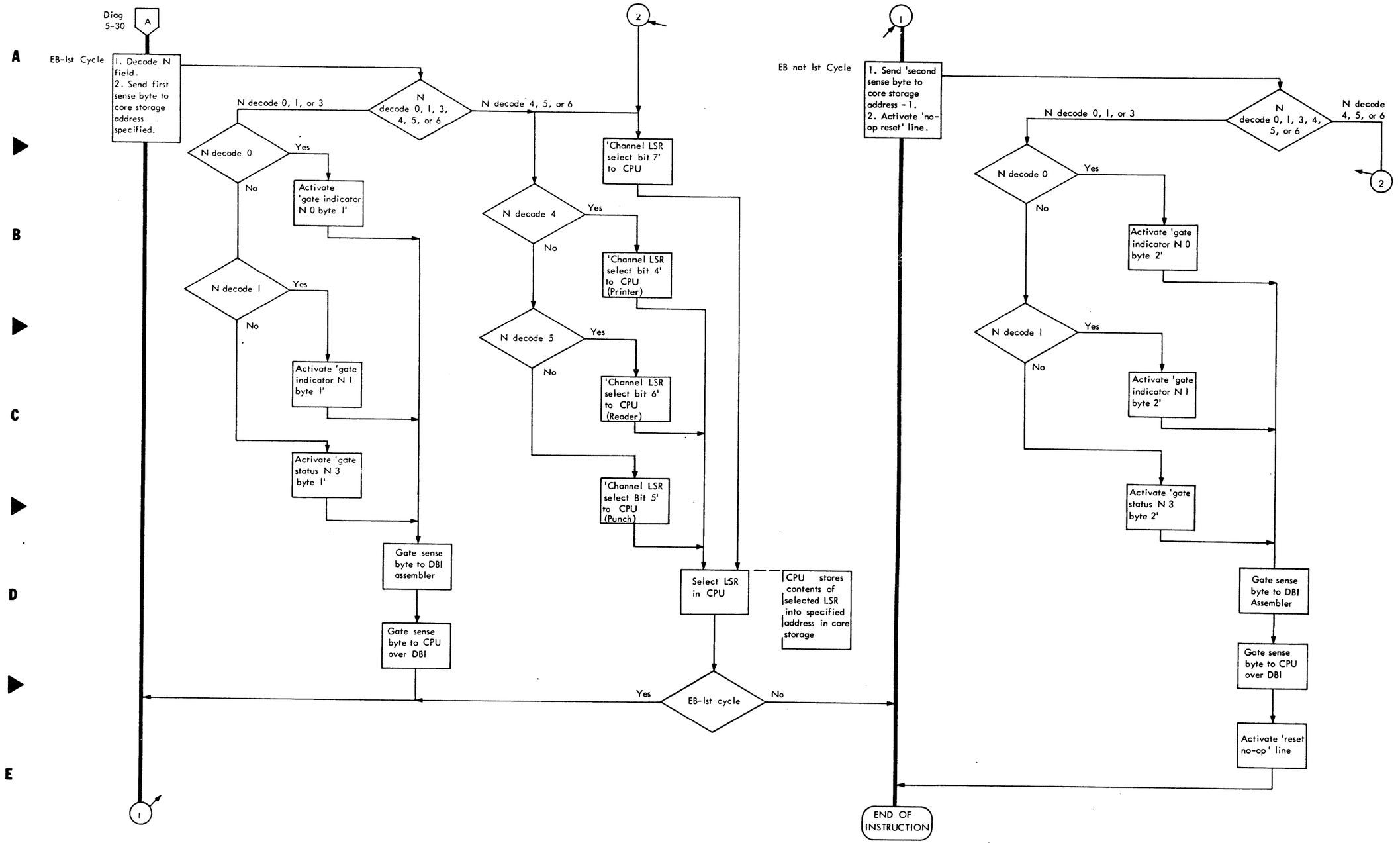
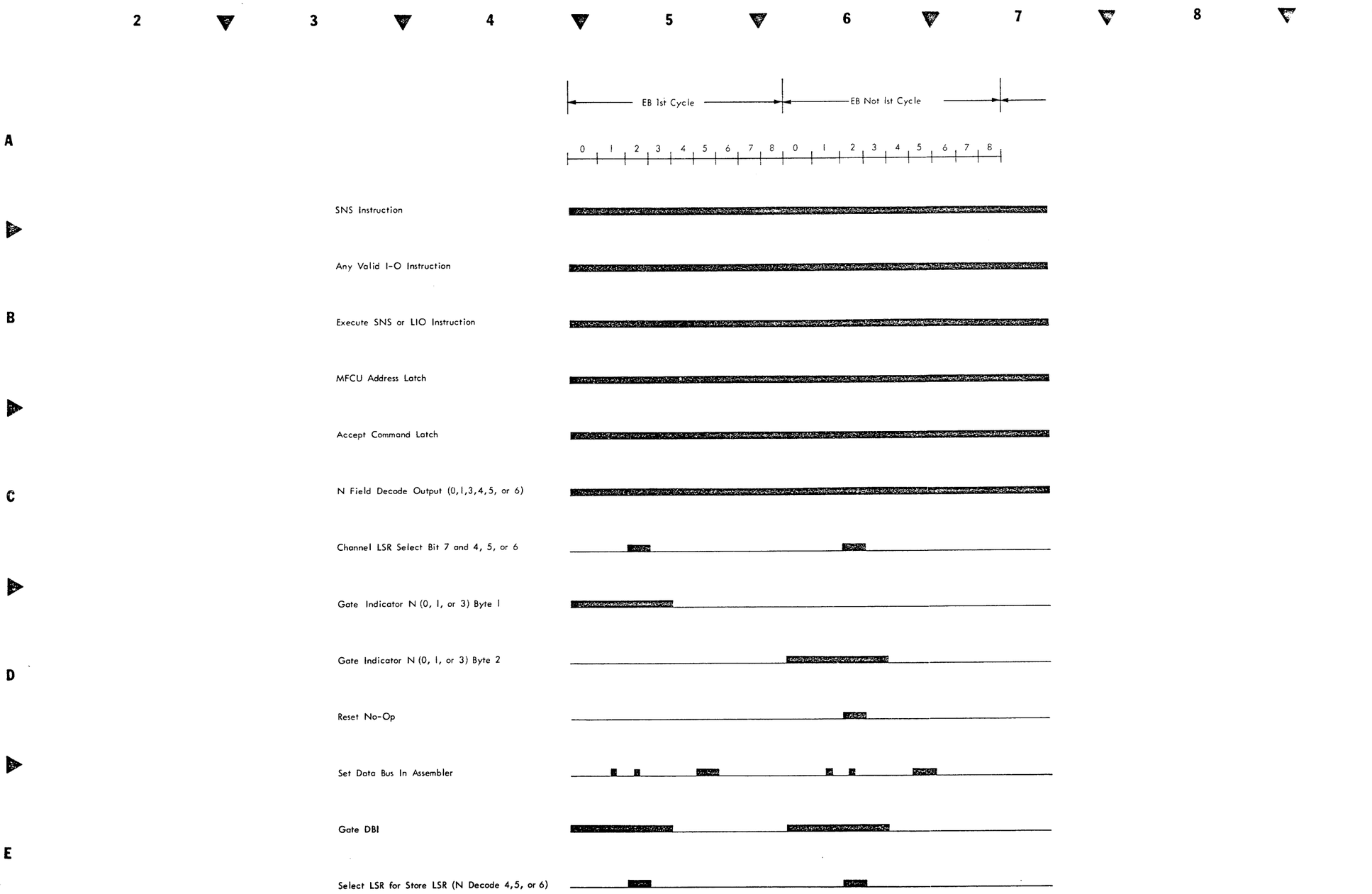


Diagram 5-035. Sense Instruction, E-B Cycles (Part 2 of 7)


2
3
4
5
6
7
8
9
EB 1st Cycle
EB Not 1st Cycle
0 1 2 3 4 5 6 7 8 0 1 2 3 4 5 6 7 8
A
SNS Instruction
Any Valid I-O Instruction
B
Execute SNS or LIO Instruction
MFCU Address Latch
Accept Command Latch
C
N Field Decode Output (0,1,3,4,5, or 6)
Channel LSR Select Bit 7 and 4, 5, or 6
Gate Indicator N (0, 1, or 3) Byte 1
D
Gate Indicator N (0, 1, or 3) Byte 2
Reset No-Op
Set Data Bus In Assembler
Gate DBI
E
Select LSR for Store LSR (N Decode 4,5, or 6)

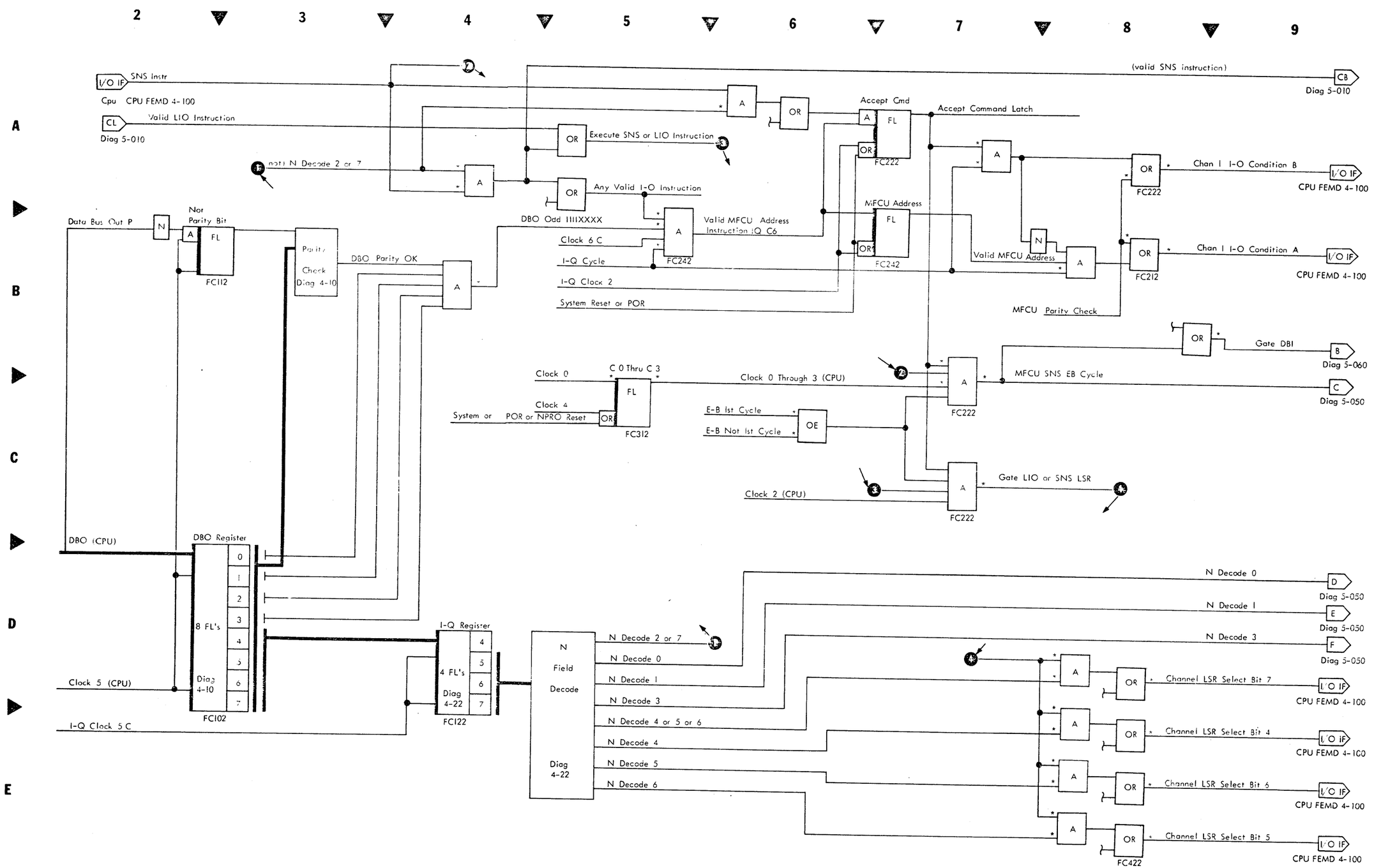
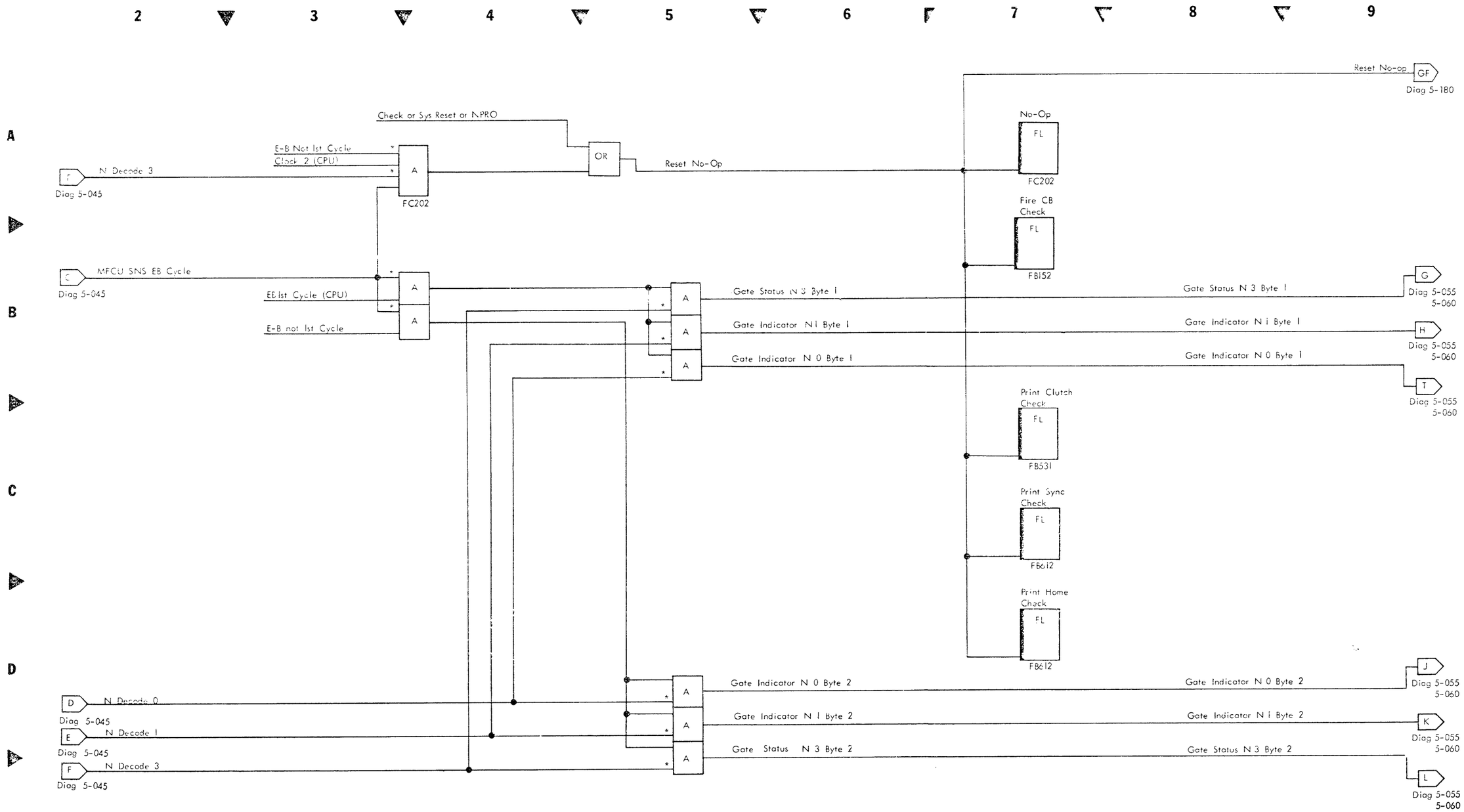
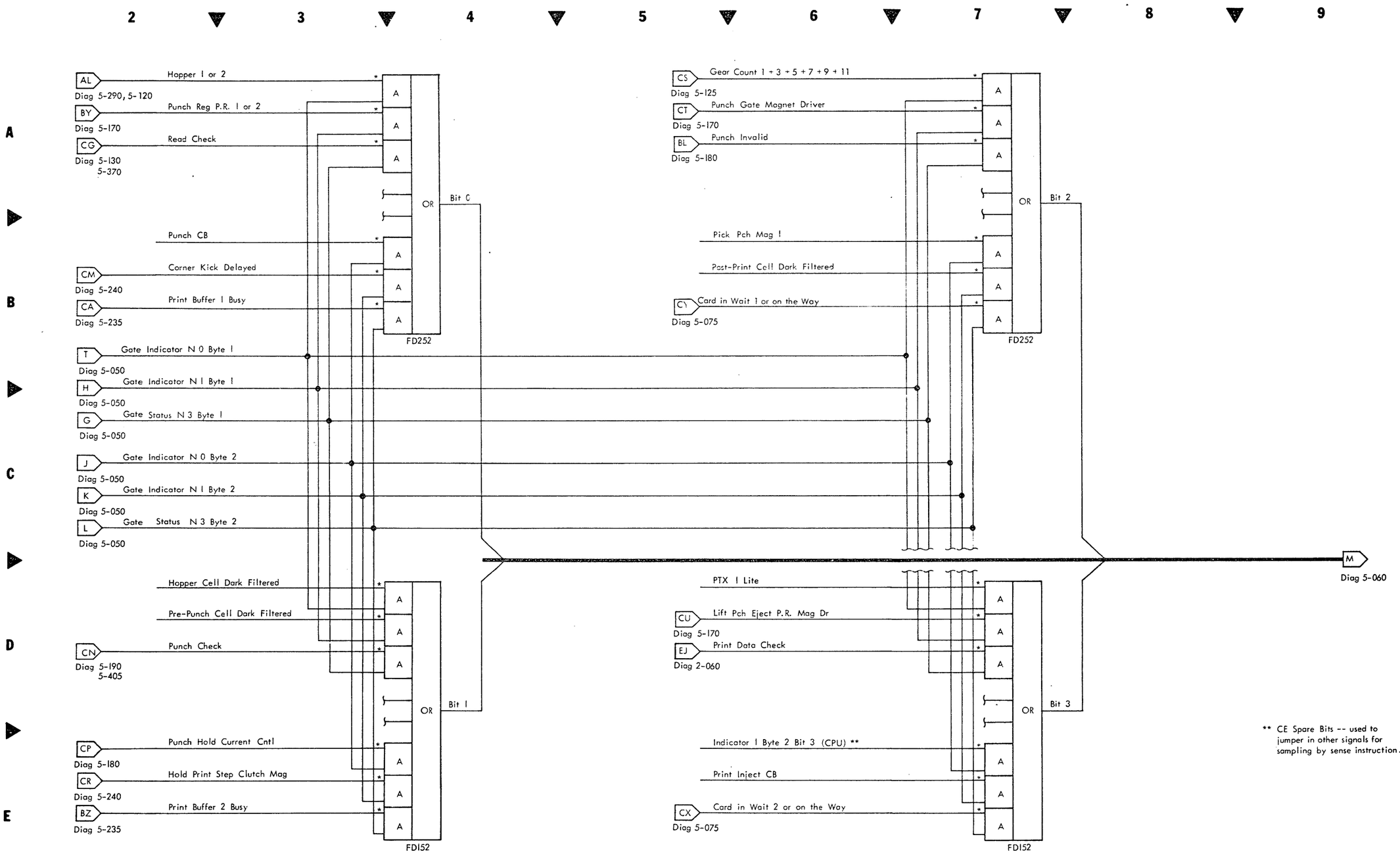
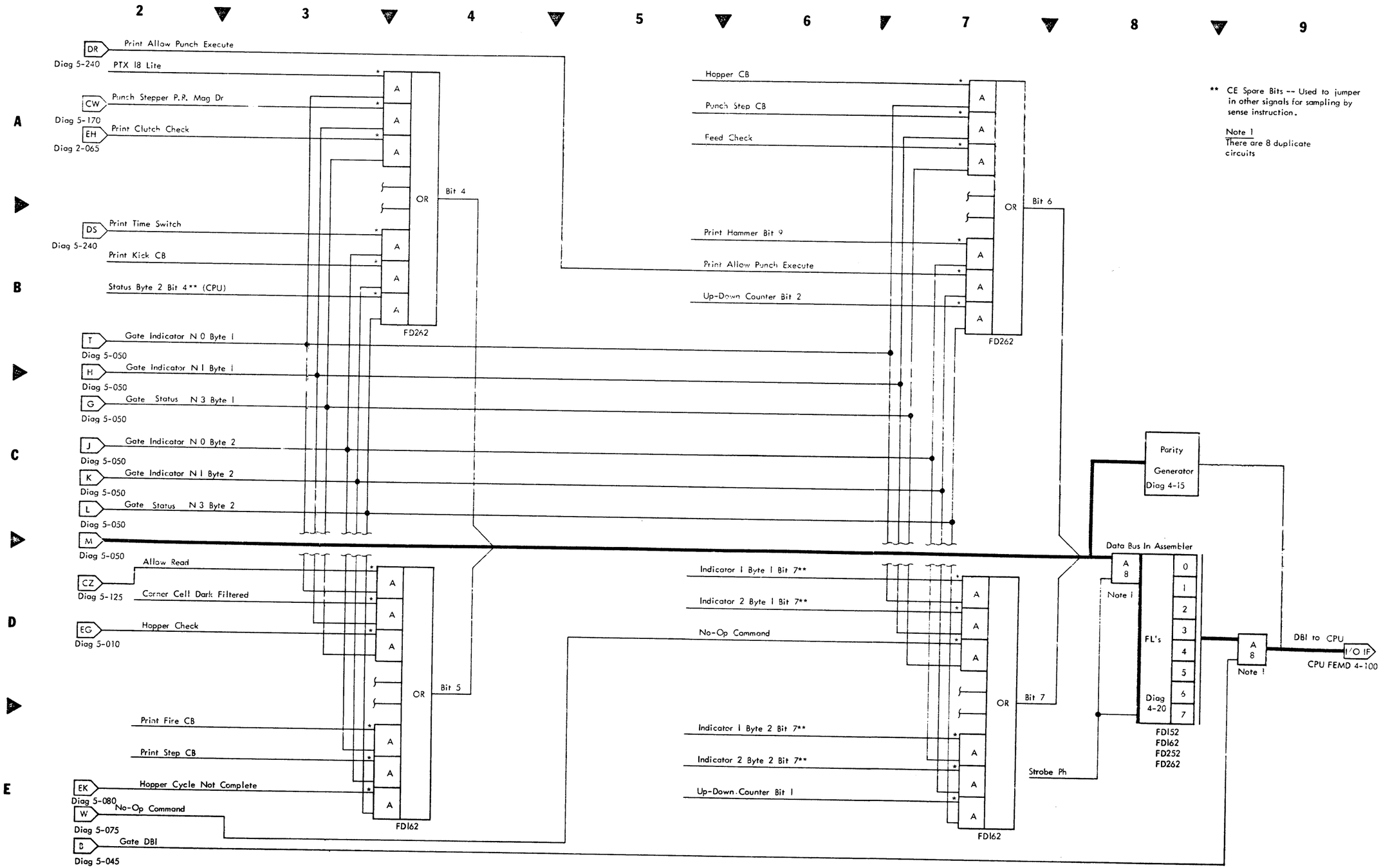


Diagram 5-045. Sense Instruction (Part 4 of 7)


2
3
4
5
6
7
8
9
A
B
C
D
E
Check or Sys Reset or NPRO
E-B Not 1st Cycle
Clock 2 (CPU)
N Decode 3
Diag 5-045
A
FC202
OR
Reset No-Op
Reset No-op
GF
Diag 5-180
No-Op
FL
FC202
Fire CB Check
FL
FB152
MFCU SNS EB Cycle
Diag 5-045
EB 1st Cycle (CPU)
E-B not 1st Cycle
A
A
A
A
A
Gate Status N 3 Byte 1
Gate Indicator N 1 Byte 1
Gate Indicator N 0 Byte 1
Gate Status N 3 Byte 1
Gate Indicator N 1 Byte 1
Gate Indicator N 0 Byte 1
G
Diag 5-055 5-060
H
Diag 5-055 5-060
T
Diag 5-055 5-060
Print Clutch Check
FL
FB531
Print Sync Check
FL
FB612
Print Home Check
FL
FB612
D
N Decode 0
Diag 5-045
E
N Decode 1
Diag 5-045
F
N Decode 3
Diag 5-045
A
A
A
Gate Indicator N 0 Byte 2
Gate Indicator N 1 Byte 2
Gate Status N 3 Byte 2
Gate Indicator N 0 Byte 2
Gate Indicator N 1 Byte 2
Gate Status N 3 Byte 2
J
Diag 5-055 5-060
K
Diag 5-055 5-060
L
Diag 5-055 5-060


2
3
4
5
6
7
8
9
A
B
C
D
E
AL
Hopper 1 or 2
Diag 5-290, 5-120
BY
Punch Reg P.R. 1 or 2
Diag 5-170
CG
Read Check
Diag 5-130
5-370
Punch CB
CM
Corner Kick Delayed
Diag 5-240
CA
Print Buffer 1 Busy
Diag 5-235
T
Gate Indicator N 0 Byte 1
Diag 5-050
H
Gate Indicator N 1 Byte 1
Diag 5-050
G
Gate Status N 3 Byte 1
Diag 5-050
J
Gate Indicator N 0 Byte 2
Diag 5-050
K
Gate Indicator N 1 Byte 2
Diag 5-050
L
Gate Status N 3 Byte 2
Diag 5-050
A
OR
Bit C
FD252
Hopper Cell Dark Filtered
Pre-Punch Cell Dark Filtered
CN
Punch Check
Diag 5-190
5-405
CP
Punch Hold Current Cntl
Diag 5-180
CR
Hold Print Step Clutch Mag
Diag 5-240
BZ
Print Buffer 2 Busy
Diag 5-235
Bit 1
FD152
CS
Gear Count 1 + 3 + 5 + 7 + 9 + 11
Diag 5-125
CT
Punch Gate Magnet Driver
Diag 5-170
BL
Punch Invalid
Diag 5-180
Pick Pch Mag 1
Post-Print Cell Dark Filtered
C\
Card in Wait 1 or on the Way
Diag 5-075
Bit 2
PTX 1 Lite
CU
Lift Pch Eject P.R. Mag Dr
Diag 5-170
EJ
Print Data Check
Diag 2-060
Indicator 1 Byte 2 Bit 3 (CPU) **
Print Inject CB
CX
Card in Wait 2 or on the Way
Diag 5-075
Bit 3
M
Diag 5-060
** CE Spare Bits -- used to jumper in other signals for sampling by sense instruction.



** CE Spare Bits -- Used to jumper in other signals for sampling by sense instruction.

Note 1
There are 8 duplicate circuits

Diagram 5-060. Sense Byte Generation (Part 7 of 7)

Diagram 5-065. Start I/O Flowchart (Part 1 of 4)

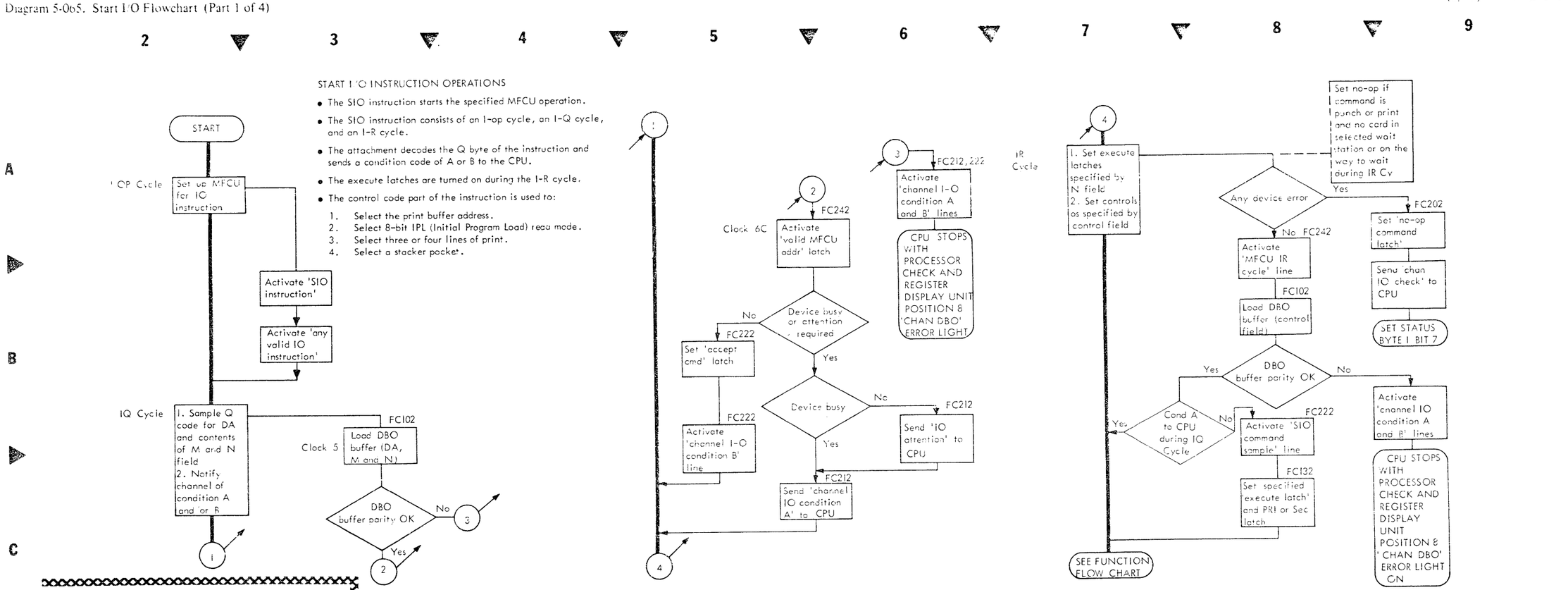
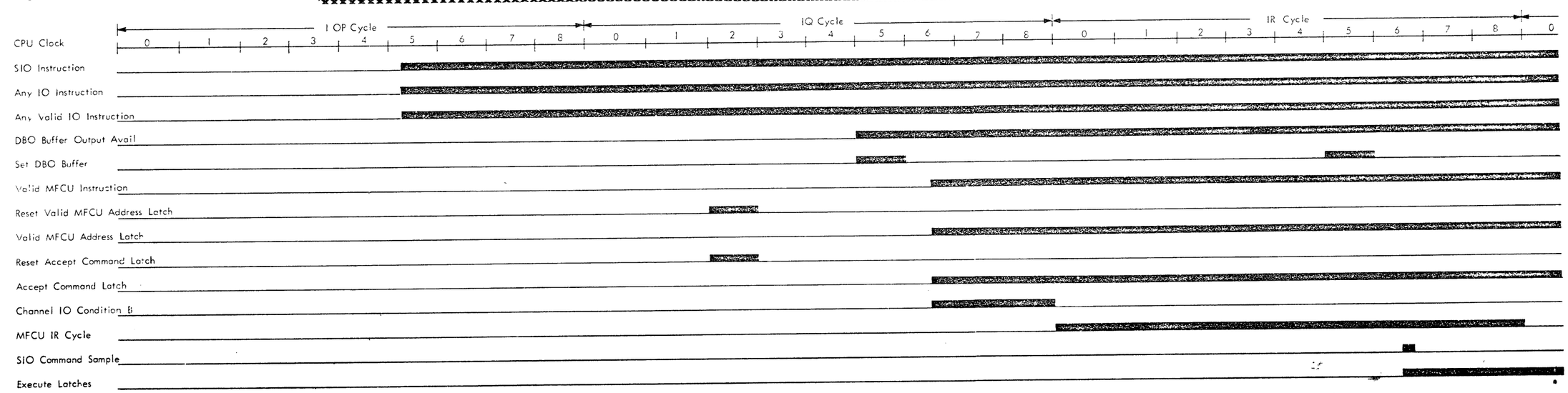
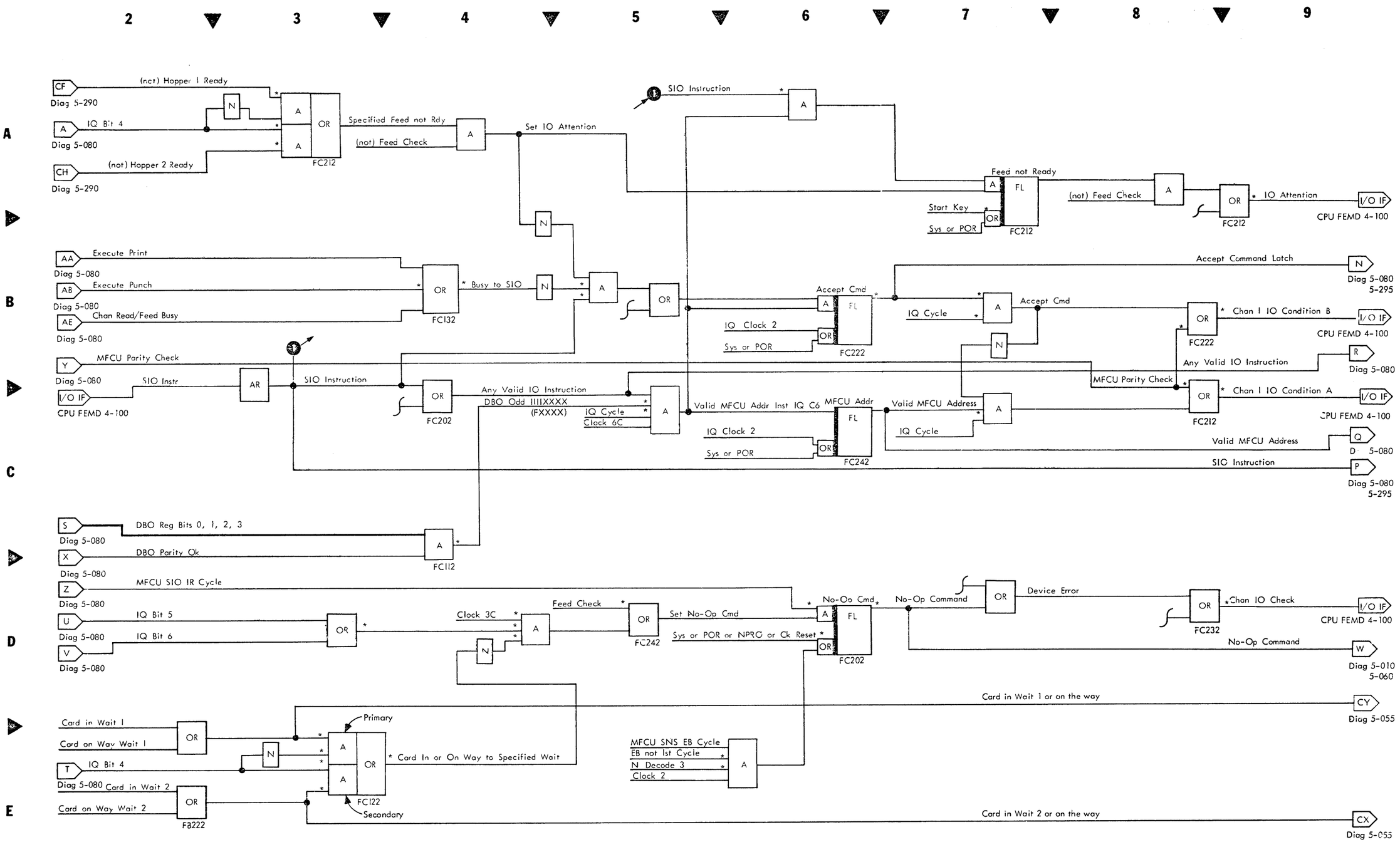
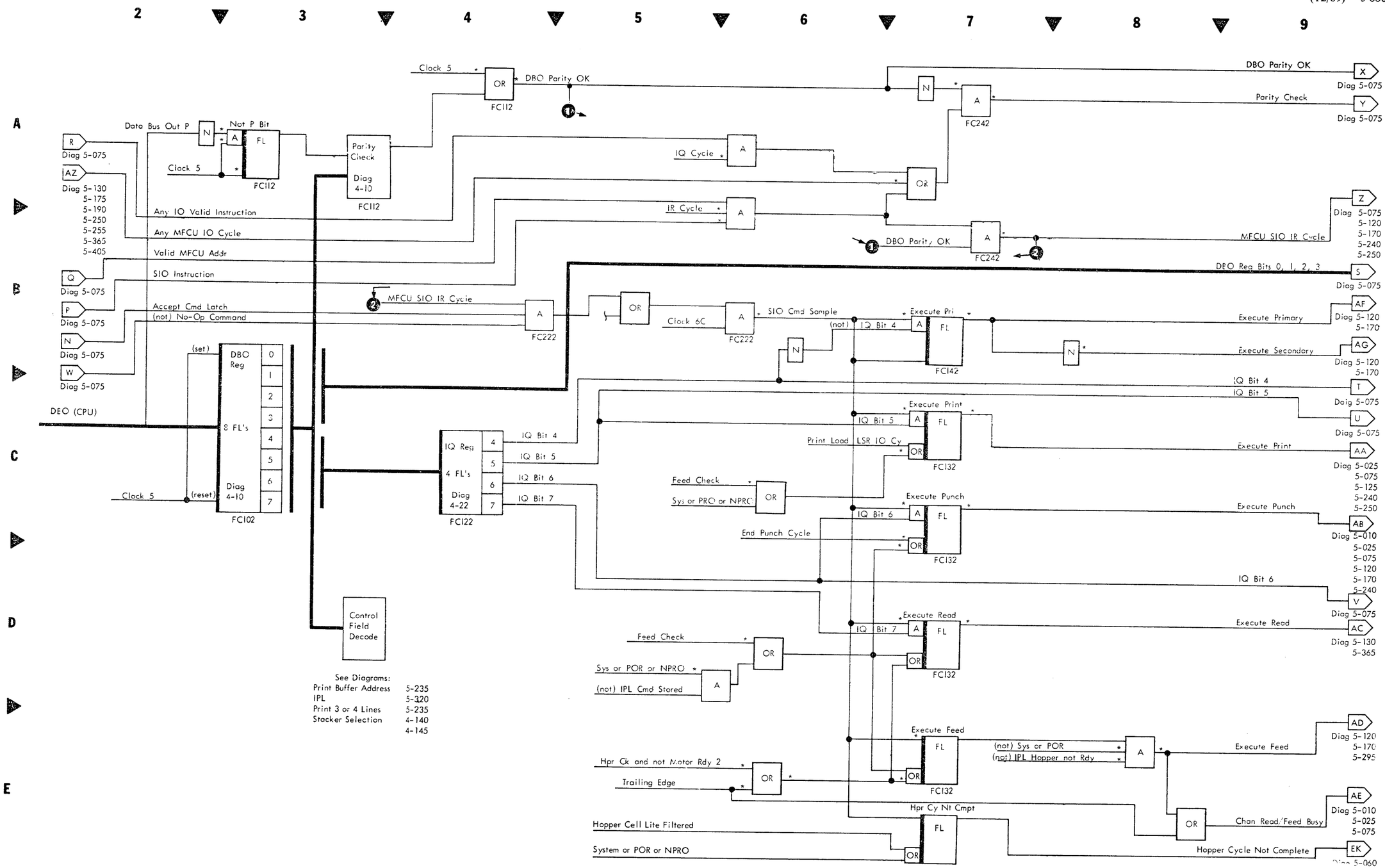


Diagram 5-070. Start I/O Timing Chart (Part 2 of 4)

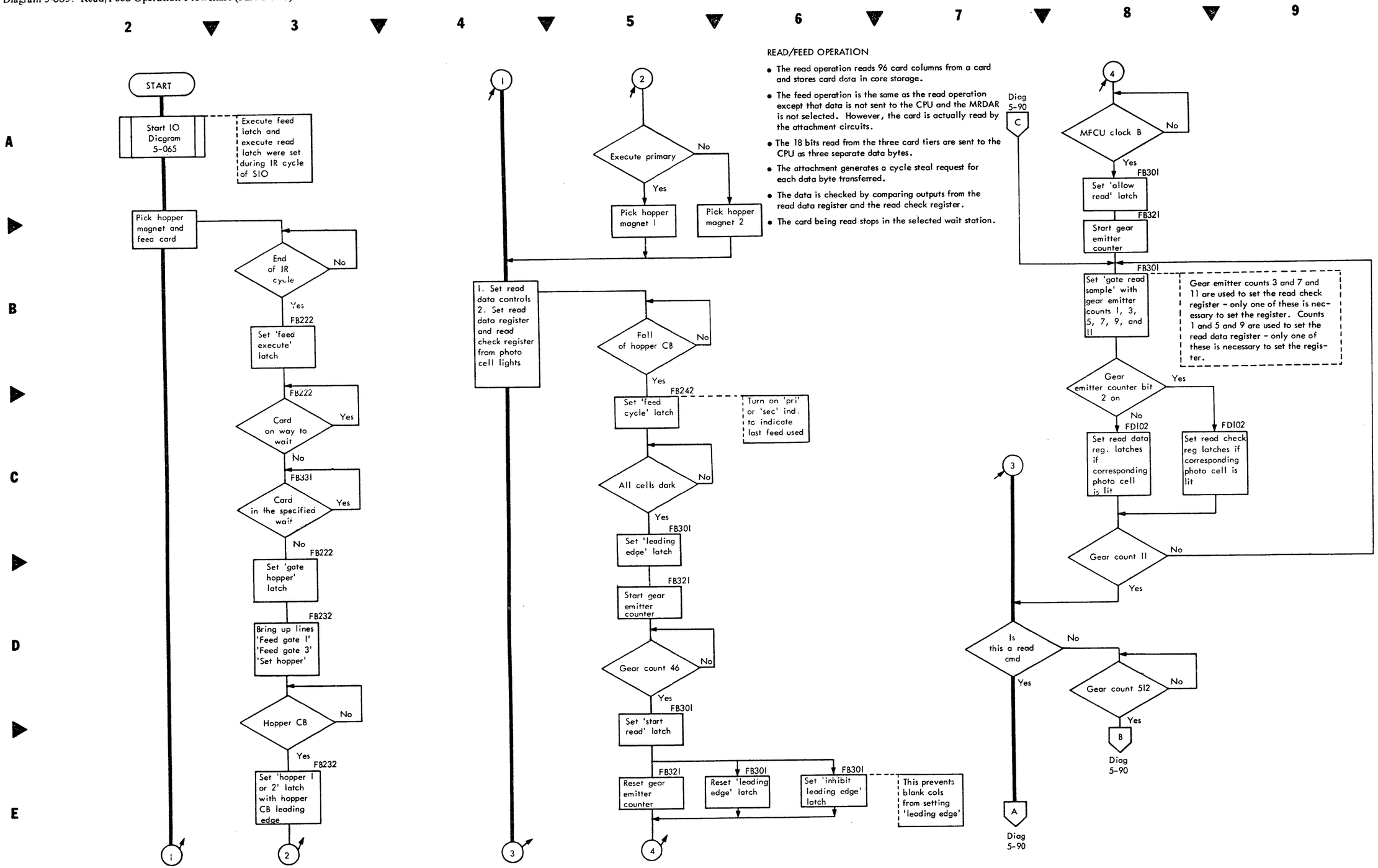



2
3
4
5
6
7
8
9
A
B
C
D
E
CF
Diag 5-290
(not) Hopper 1 Ready
A
Diag 5-080
IQ Bit 4
CH
Diag 5-290
(not) Hopper 2 Ready
N
A
A
OR
FC212
Specified Feed not Rdy
(not) Feed Check
A
Set IO Attention
N
SIO Instruction
A
Feed not Ready
A
FL
OR
FC212
Start Key
Sys or POR
(not) Feed Check
A
OR
FC212
IO Attention
I/O IF
CPU FEMD 4-100
AA
Diag 5-080
Execute Print
AB
Diag 5-080
Execute Punch
AE
Diag 5-080
Chan Read/Feed Busy
OR
FC132
Busy to SIO
N
A
OR
Accept Cmd
A
FL
OR
FC222
IQ Clock 2
Sys or POR
IQ Cycle
A
Accept Cmd
Accept Command Latch
N
Diag 5-080
5-295
OR
FC222
Chan I IO Condition B
I/O IF
CPU FEMD 4-100
N
Y
Diag 5-080
MFCU Parity Check
I/O IF
CPU FEMD 4-100
SIO Instr
AR
SIO Instruction
OR
FC202
Any Valid IO Instruction
DBO Odd IIIIXXXX
(FXXXX)
IQ Cycle
Clock 6C
A
Valid MFCU Addr Inst IQ C6
MFCU Addr
FL
OR
FC242
IQ Clock 2
Sys or POR
Valid MFCU Address
IQ Cycle
A
Any Valid IO Instruction
R
Diag 5-080
MFCU Parity Check
OR
FC212
Chan I IO Condition A
I/O IF
CPU FEMD 4-100
Valid MFCU Address
Q
Diag 5-080
SIO Instruction
P
Diag 5-080
5-295
S
Diag 5-080
DBO Reg Bits 0, 1, 2, 3
X
Diag 5-080
DBO Parity Ok
A
FC112
Z
Diag 5-080
MFCU SIO IR Cycle
U
Diag 5-080
IQ Bit 5
V
Diag 5-080
IQ Bit 6
OR
Clock 3C
A
Feed Check
OR
FC242
Set No-Op Cmd
Sys or POR or NPRO or Ck Reset
N
No-Op Cmd
A
FL
OR
FC202
No-Op Command
OR
Device Error
OR
FC232
Chan IO Check
I/O IF
CPU FEMD 4-100
No-Op Command
W
Diag 5-010
5-060
Card in Wait 1 or on the way
CY
Diag 5-055
Card in Wait 1
Card on Way Wait 1
OR
T
Diag 5-080
IQ Bit 4
Card in Wait 2
Card on Way Wait 2
OR
F8222
N
Primary
A
A
OR
FC122
Secondary
* Card In or On Way to Specified Wait
MFCU SNS EB Cycle
EB not 1st Cycle
N Decode 3
Clock 2
A
Card in Wait 2 or on the way
CX
Diag 5-055



See Diagrams:

Print Buffer Address	5-235
IPL	5-320
Print 3 or 4 Lines	5-235
Stacker Selection	4-140
	4-145


2
3
4
5
6
7
8
9
A
B
C
D
E
START
Start IO Diagram 5-065
Execute feed latch and execute read latch were set during IR cycle of SIO
Pick hopper magnet and feed card
End of IR cycle
No
Yes
FB222
Set 'feed execute' latch
FB222
Card on way to wait
Yes
No
FB331
Card in the specified wait
Yes
No
FB222
Set 'gate hopper' latch
FB232
Bring up lines 'Feed gate 1' 'Feed gate 3' 'Set hopper'
Hopper CB
No
Yes
FB232
Set 'hopper 1 or 2' latch with hopper CB leading edge
1
2
1
2
Execute primary
No
Yes
Pick hopper magnet 1
Pick hopper magnet 2
1. Set read data controls 2. Set read data register and read check register from photo cell lights
Fall of hopper CB
No
Yes
FB242
Set 'feed cycle' latch
Turn on 'pri' or 'sec' ind. tc indicate last feed used
All cells dark
No
Yes
FB301
Set 'leading edge' latch
FB321
Start gear emitter counter
Gear count 46
No
Yes
FB301
Set 'start read' latch
FB321
Reset gear emitter counter
FB301
Reset 'leading edge' latch
FB301
Set 'inhibit leading edge' latch
This prevents blank cols from setting 'leading edge'
3
4
3
4
READ/FEED OPERATION
• The read operation reads 96 card columns from a card and stores card data in core storage.
• The feed operation is the same as the read operation except that data is not sent to the CPU and the MRDAR is not selected. However, the card is actually read by the attachment circuits.
• The 18 bits read from the three card tiers are sent to the CPU as three separate data bytes.
• The attachment generates a cycle steal request for each data byte transferred.
• The data is checked by comparing outputs from the read data register and the read check register.
• The card being read stops in the selected wait station.
Diag 5-90
C
4
MFCU clock B
No
Yes
FB301
Set 'allow read' latch
FB321
Start gear emitter counter
FB301
Set 'gate read sample' with gear emitter counts 1, 3, 5, 7, 9, and 11
Gear emitter counts 3 and 7 and 11 are used to set the read check register - only one of these is necessary to set the register. Counts 1 and 5 and 9 are used to set the read data register - only one of these is necessary to set the register.
Gear emitter counter bit 2 on
Yes
No
FD102
Set read data reg. latches if corresponding photo cell is lit
FD102
Set read check reg latches if corresponding photo cell is lit
Gear count 11
No
Yes
3
Is this a read cmd
No
Yes
Gear count 512
No
Yes
B
Diag 5-90
A
Diag 5-90

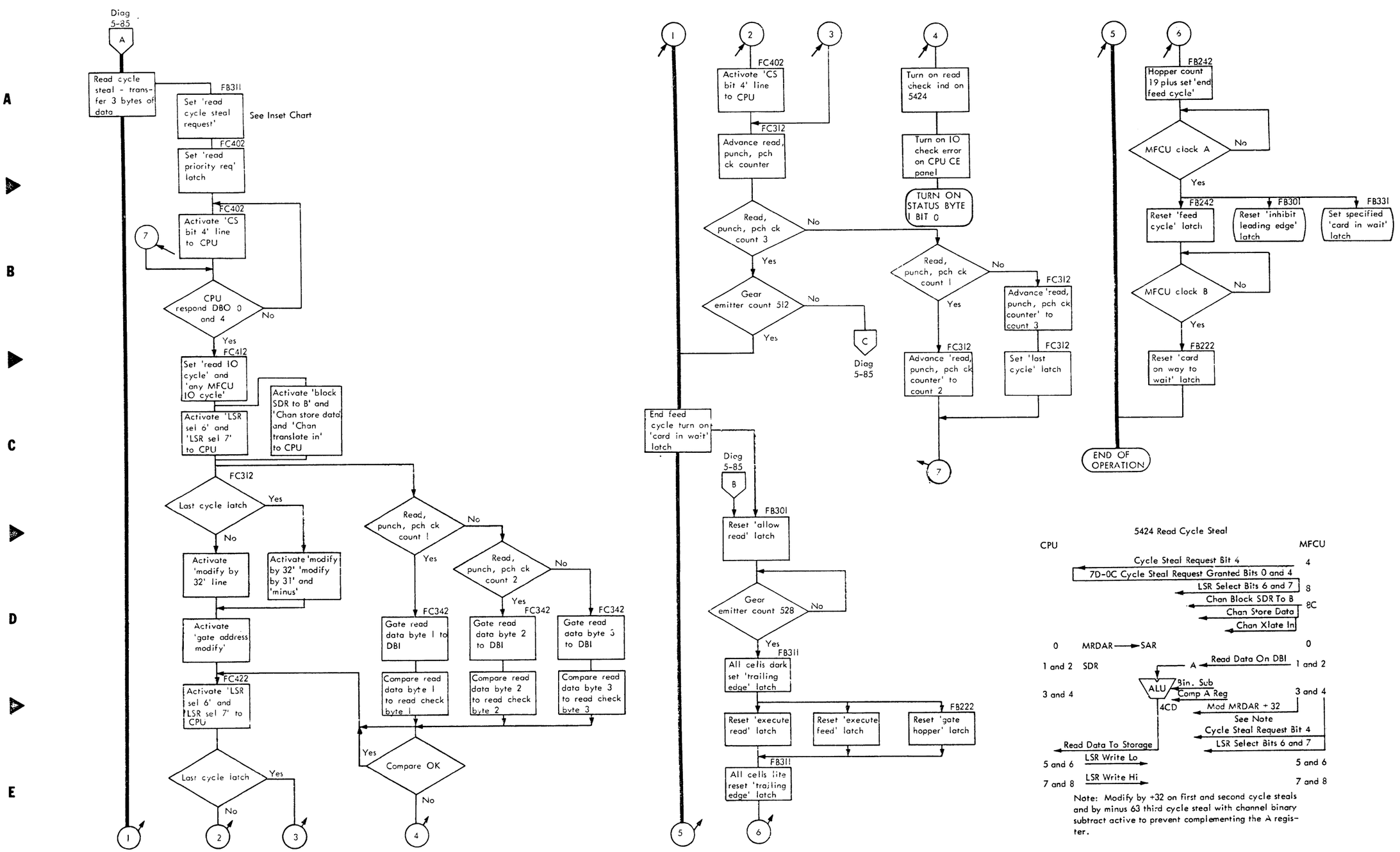


Diagram 5-090. Read/Feed Operation Flowchart (Part 2 of 8)

2 3 4 5 6 7 8 9

A

Time (ms) Model A 1

Time (ms) Model A 2

Hopper CB

Execute Read

Execute Feed

Feed Execute

Hopper 1 or 2 FF

Feed Cycle

Read Busy

Read Inject Feed Roll (Mech Action)

B

Leading Edge

Start Read

Allow Read

Wait Inject Feed Roll (Mech Action)

Card In Watt Latch

Read Data Controls Timing Chart

C

Leading Edge

Gear Emitter (Count)

Gear Counter Reset

D

Start Read

Allow Read

Gear Counts 1,3,5,7,9,11

Reset Read Data and Read Check Reg's

Set Read Data Reg's

Set Read Check Reg's

Cycle Steal Request

Trailing Edge

E

See Diagram 5-105 Start Read and Gear Emitter Counter for Expansion

See Diagram 5-110 Read C.S. Request for Expansion. See Diagrams 5-350 and 5-355 for Diagnostic Read C.S. Request.

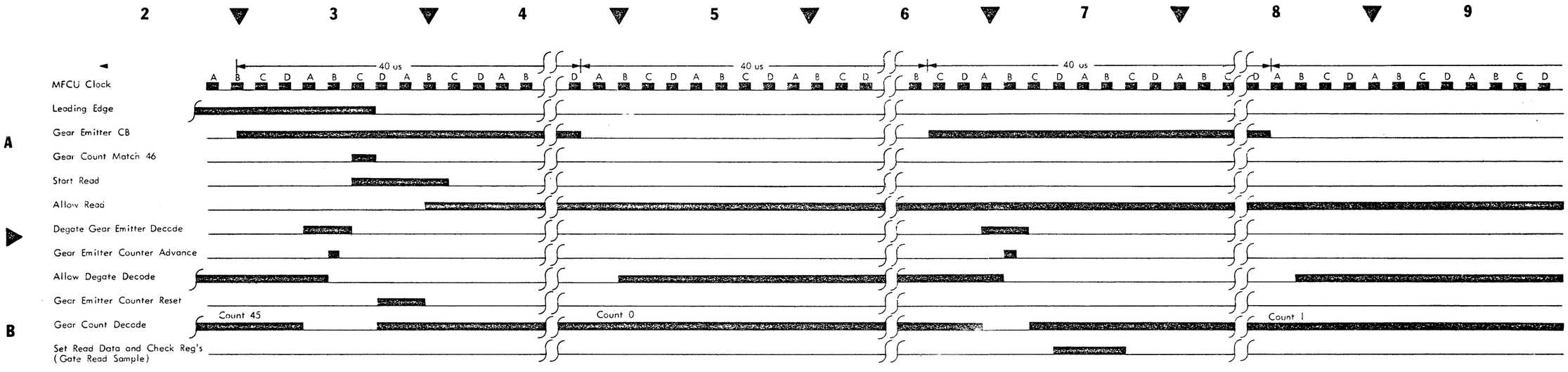


Diagram 5-105. Start Read and Read Gear Emitter Counter Timing Chart (Part 4 of 8)

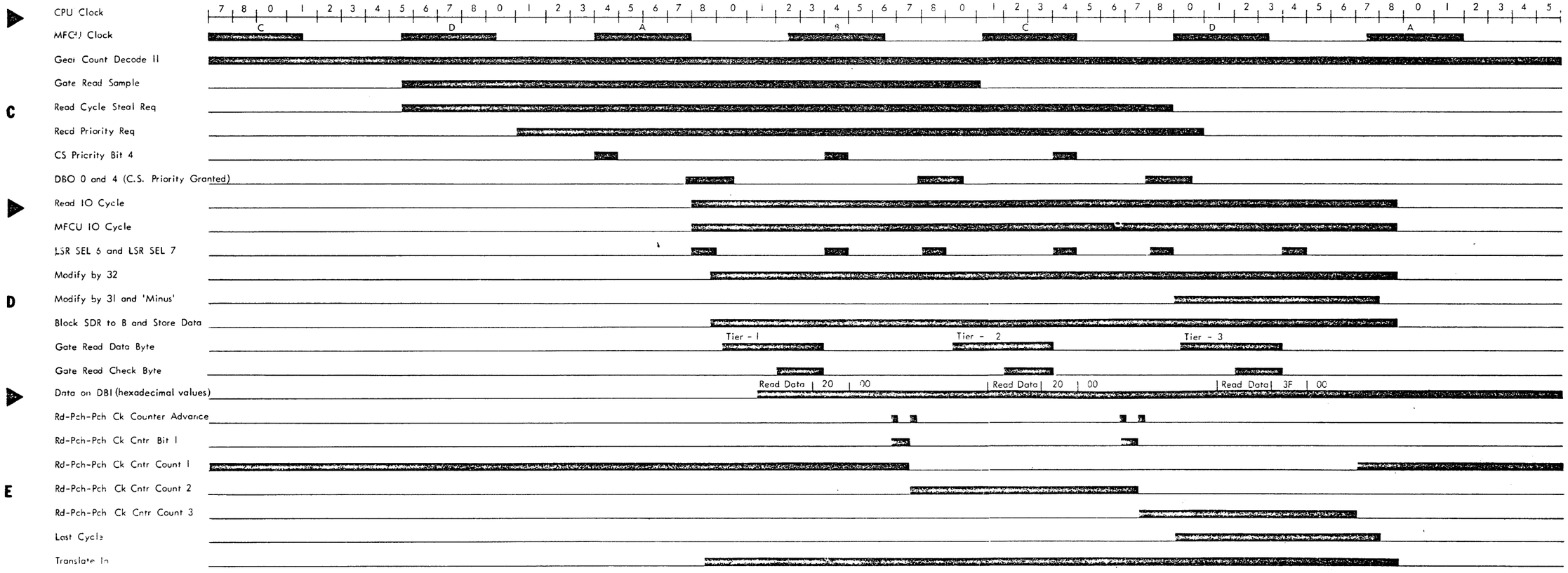
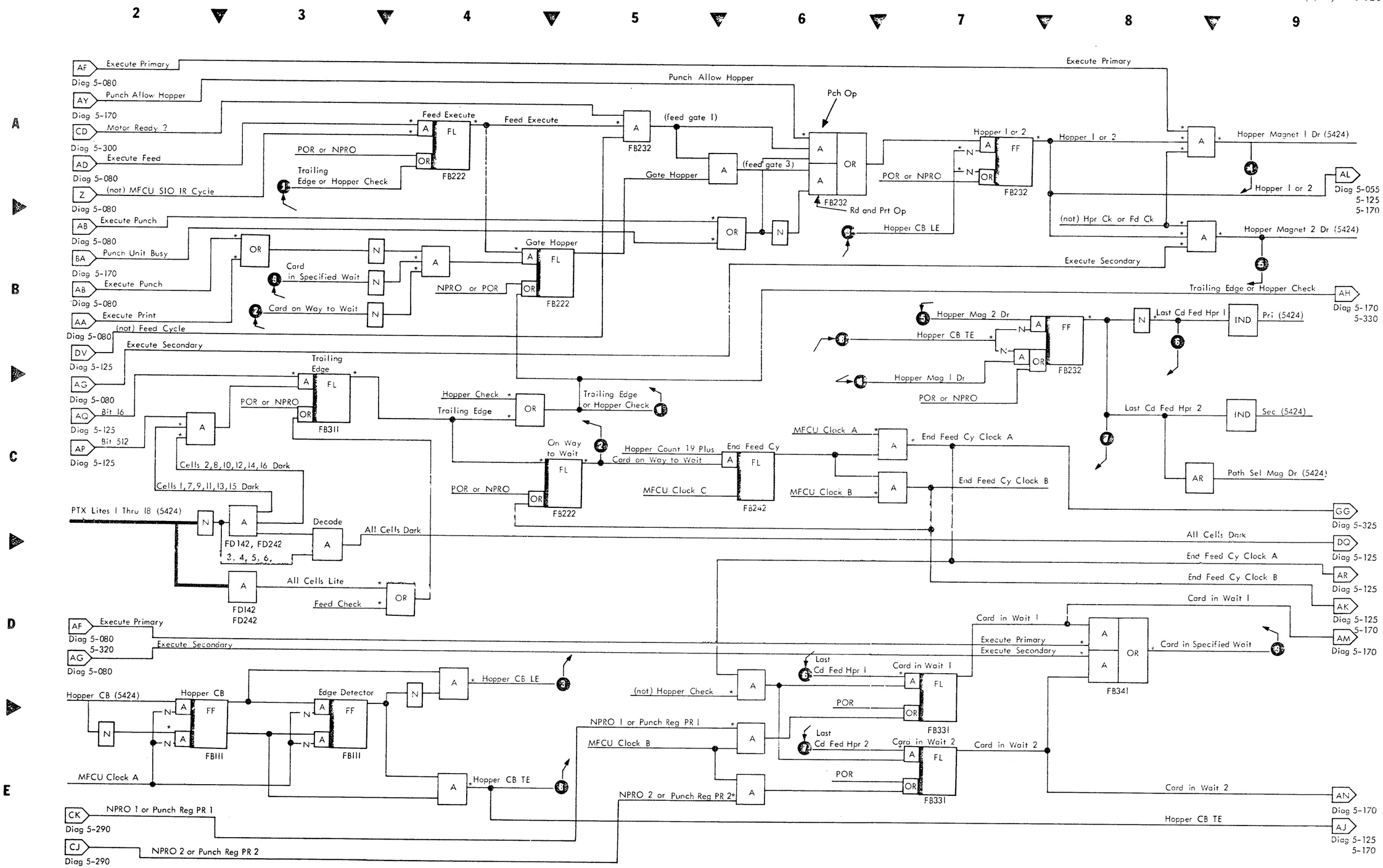


Diagram 5-110. Read Cycle Steal Request Timing Chart (Part 5 of 8)


2
3
4
5
6
7
8
9
A
B
C
D
E
AF Execute Primary
Diag 5-080
AY Punch Allow Hopper
Diag 5-170
CD Motor Ready ?
Diag 5-300
AD Execute Feed
Diag 5-080
Z (not) MFCU SIO IR Cycle
Diag 5-080
AB Execute Punch
Diag 5-080
BA Punch Unit Busy
Diag 5-170
AB Execute Punch
Diag 5-080
AA Execute Print
Diag 5-080
DV (not) Feed Cycle
Diag 5-125
AG Execute Secondary
Diag 5-080
AQ Bit 16
Diag 5-125
AP Bit 512
Diag 5-125
Feed Execute
FL
FB222
POR or NPRO
Trailing Edge or Hopper Check
Feed Execute
A
FB232
(feed gate 1)
Punch Allow Hopper
Pch Op
Gate Hopper
(feed gate 3)
OR
N
FB232
Rd and Prt Op
Hopper CB LE
Execute Primary
Hopper 1 or 2
FF
FB232
Hopper Magnet 1 Dr (5424)
Hopper 1 or 2
AL
Diag 5-055
5-125
5-170
(not) Hpr Ck or Fd Ck
Hopper Magnet 2 Dr (5424)
Execute Secondary
Trailing Edge or Hopper Check
AH
Diag 5-170
5-330
Gate Hopper
NPRO or POR
Card in Specified Wait
Card on Way to Wait
Trailing Edge
FB311
Hopper Check
Trailing Edge
Trailing Edge or Hopper Check
On Way to Wait
FB222
POR or NPRO
Hopper Count 19 Plus Card on Way to Wait
End Feed Cy
FB242
MFCU Clock C
MFCU Clock A
End Feed Cy Clock A
MFCU Clock B
End Feed Cy Clock B
Hopper Mag 2 Dr
Hopper CB TE
Hopper Mag 1 Dr
POR or NPRO
FB232
Last Cd Fed Hpr 1
IND
Pri (5424)
Last Cd Fed Hpr 2
IND
Sec (5424)
AR
Path Sel Mag Dr (5424)
Cells 2,8,10,12,14,16 Dark
Cells 1,7,9,11,13,15 Dark
PTX Lites 1 Thru 18 (5424)
Decode
FD142, FD242
3, 4, 5, 6,
All Cells Dark
All Cells Lite
Feed Check
FD142
FD242
GG
Diag 5-325
All Cells Dark
DQ
Diag 5-125
End Feed Cy Clock A
AR
Diag 5-125
End Feed Cy Clock B
AK
Diag 5-125
5-170
Card in Wait 1
AM
Diag 5-170
AF Execute Primary
Diag 5-080
5-320
AG Execute Secondary
Diag 5-080
Hopper CB (5424)
Hopper CB
FF
FB111
Edge Detector
FF
FB111
Hopper CB LE
Hopper CB TE
MFCU Clock A
(not) Hopper Check
NPRO 1 or Punch Reg PR 1
MFCU Clock B
NPRO 2 or Punch Reg PR 2
Last Cd Fed Hpr 1
Card in Wait 1
FL
FB331
POR
Last Cd Fed Hpr 2
Card in Wait 2
FL
FB331
POR
Card in Wait 1
Execute Primary
Execute Secondary
Card in Specified Wait
FB341
Card in Wait 2
AN
Diag 5-170
Hopper CB TE
AJ
Diag 5-125
5-170
CK NPRO 1 or Punch Reg PR 1
Diag 5-290
CJ NPRO 2 or Punch Reg PR 2
Diag 5-290

Notes:

1. There are 18 Read Data Register FL's and 18 Read Check Register FL's.
2. See Diagrams 5-315, 5-320, and 5-325 for IPL operations. Diagram 5-320 shows C and D bit gating.

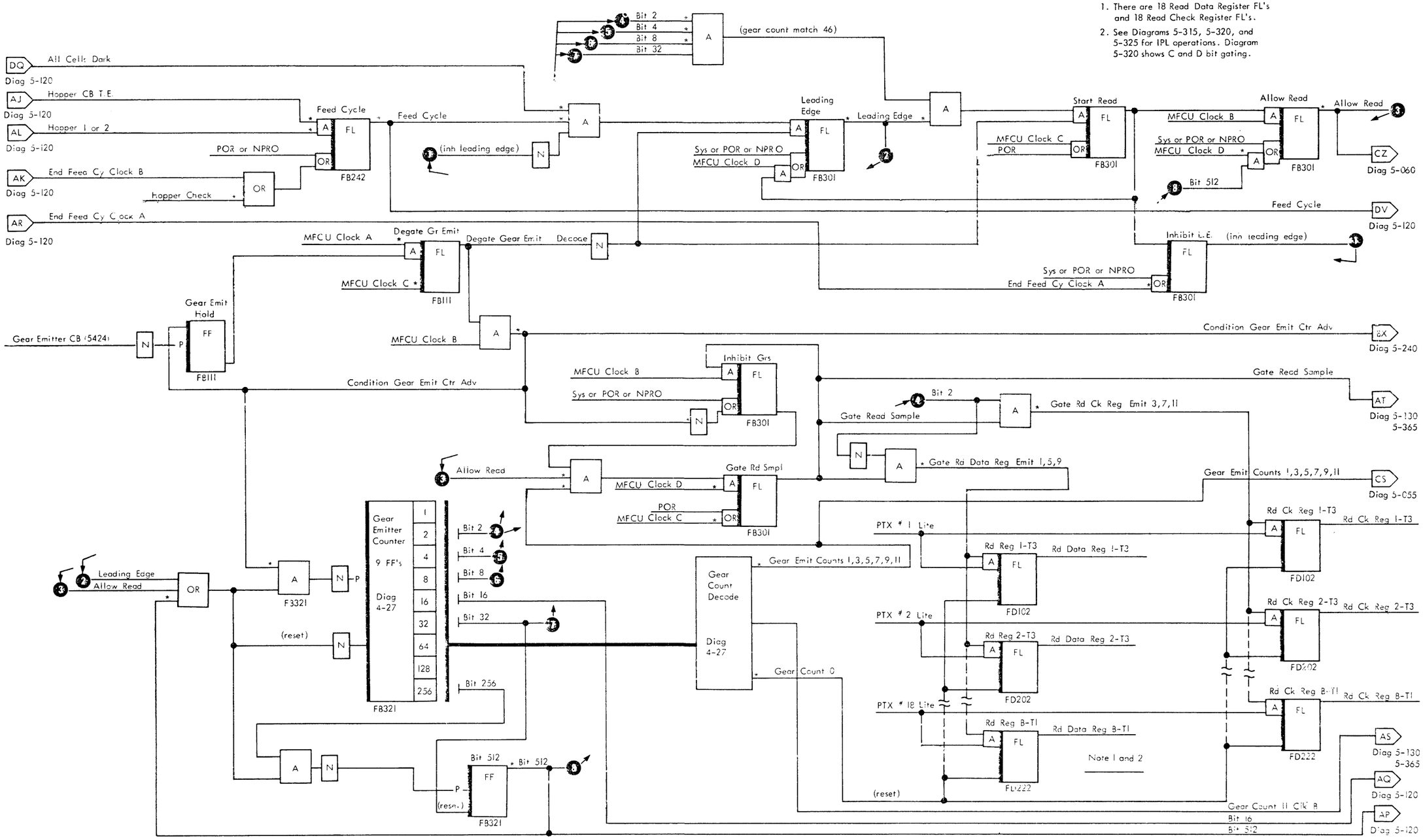
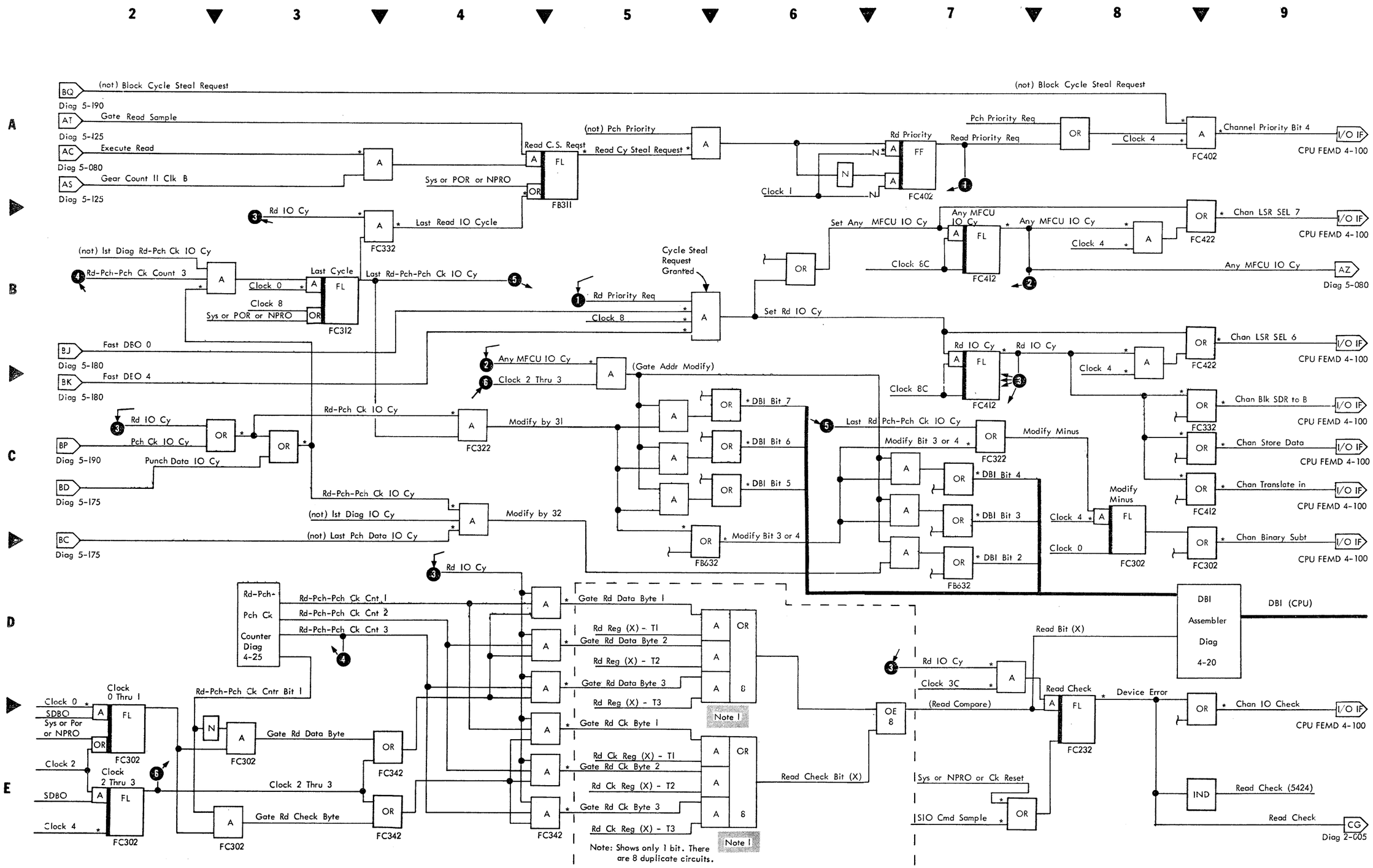
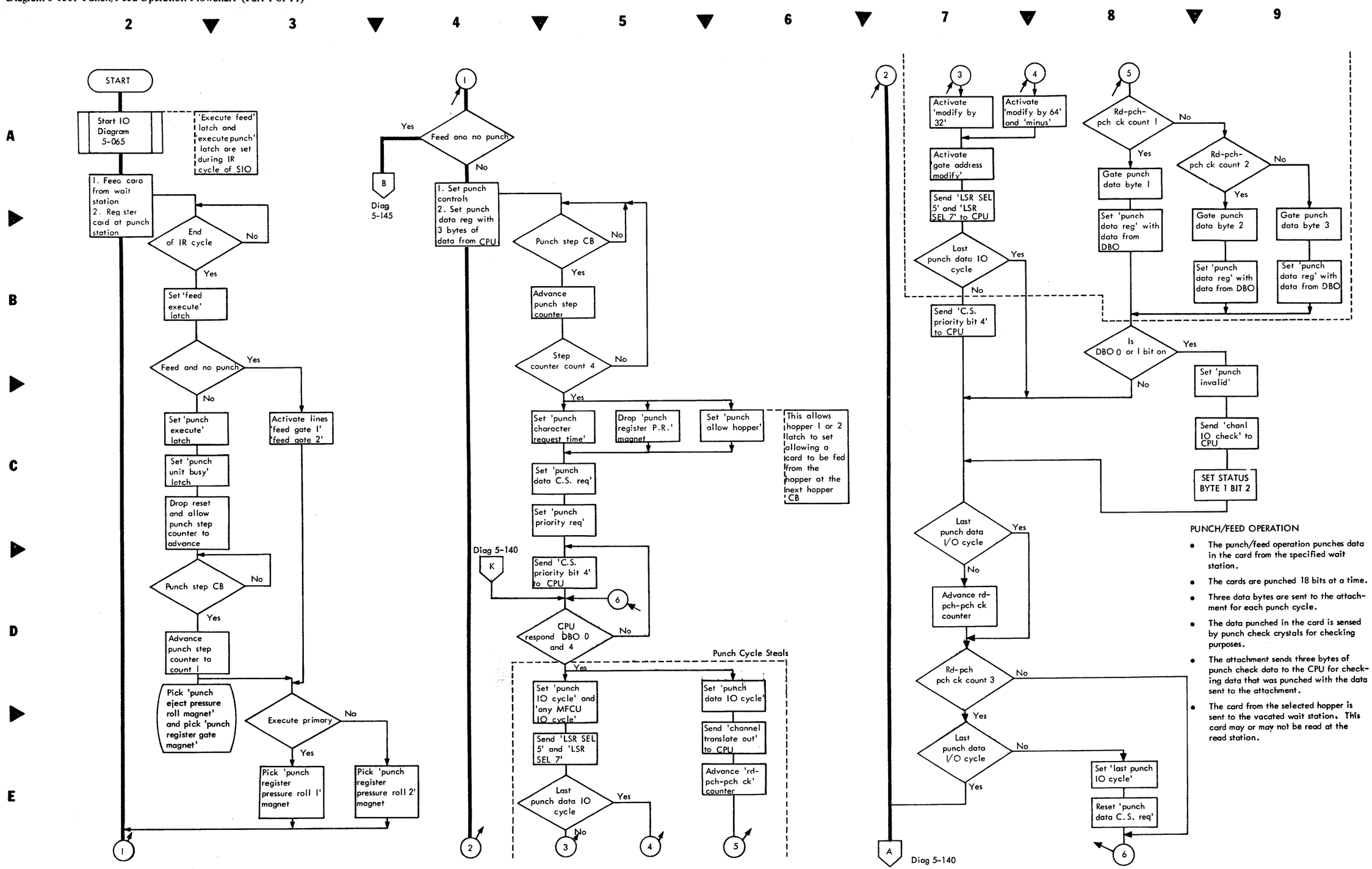


Diagram 5-125. Read/Feed Data Controls (Part 7 of 8)


2 3 4 5 6 7 8 9
A
B
C
D
E
BQ (not) Block Cycle Steal Request
Diag 5-190
AT Gate Read Sample
Diag 5-125
AC Execute Read
Diag 5-080
AS Gear Count 11 Clk B
Diag 5-125
Read C.S. Reqst
Read Cy Steal Request *
(not) Pch Priority
Sys or POR or NPRO
FB311
Rd IO Cy
Last Read IO Cycle
FC332
(not) 1st Diag Rd-Pch Ck IO Cy
Rd-Pch-Pch Ck Count 3
Clock 0
Clock 8
Sys or POR or NPRO
Last Cycle
Last Rd-Pch-Pch Ck IO Cy
FC312
Cycle Steal Request Granted
Rd Priority Req
Clock 8
Set Rd IO Cy
BJ Fast DEO 0
Diag 5-180
BK Fast DEO 4
Diag 5-180
Any MFCU IO Cy
Clock 2 Thru 3
(Gate Addr Modify)
Rd-Pch Ck IO Cy
Modify by 31
FC322
BP
Diag 5-190
Rd IO Cy
Pch Ck IO Cy
Punch Data IO Cy
BD
Diag 5-175
Rd-Pch-Pch Ck IO Cy
(not) 1st Diag IO Cy
(not) Last Pch Data IO Cy
Modify by 32
BC
Diag 5-175
DBI Bit 7
DBI Bit 6
DBI Bit 5
Modify Bit 3 or 4
FB632
Last Rd Pch-Pch Ck IO Cy
Modify Bit 3 or 4
Modify Minus
DBI Bit 4
DBI Bit 3
DBI Bit 2
FB632
Rd Priority
Read Priority Req
Pch Priority Req
Clock 1
FC402
Clock 4
Channel Priority Bit 4
I/O IF
CPU FEMD 4-100
FC402
Set Any MFCU IO Cy
Any MFCU IO Cy
Clock 6C
FC412
Chan LSR SEL 7
FC422
Any MFCU IO Cy
AZ
Diag 5-080
Clock 8C
Chan LSR SEL 6
Chan Blk SDR to B
FC332
Chan Store Data
Chan Translate in
FC412
Chan Binary Subt
FC302
Modify Minus
Clock 0
Rd-Pch-Pch Ck Cnt 1
Rd-Pch-Pch Ck Cnt 2
Rd-Pch-Pch Ck Cnt 3
Rd-Pch- Pch Ck Counter Diag 4-25
Rd-Pch-Pch Ck Cntr Bit 1
Clock 0 Thru 1
SDBO
Sys or Por or NPRO
FC302
Clock 2
Clock 2 Thru 3
SDBO
Clock 4
FC302
Gate Rd Data Byte
Gate Rd Check Byte
FC342
Gate Rd Data Byte 1
Rd Reg (X) - T1
Gate Rd Data Byte 2
Rd Reg (X) - T2
Gate Rd Data Byte 3
Rd Reg (X) - T3
Gate Rd Ck Byte 1
Rd Ck Reg (X) - T1
Gate Rd Ck Byte 2
Rd Ck Reg (X) - T2
Gate Rd Ck Byte 3
Rd Ck Reg (X) - T3
Note 1
Note: Shows only 1 bit. There are 8 duplicate circuits.
Read Check Bit (X)
OE 8
Read Bit (X)
DBI Assembler Diag 4-20
DBI (CPU)
Clock 3C
(Read Compare)
Read Check
Device Error
FC232
Chan IO Check
Sys or NPRO or Ck Reset
SIO Cmd Sample
IND
Read Check (5424)
Read Check
CG
Diag 2-005



PUNCH/FEED OPERATION

- The punch/feed operation punches data in the card from the specified wait station.
- The cards are punched 18 bits at a time.
- Three data bytes are sent to the attachment for each punch cycle.
- The data punched in the card is sensed by punch check crystals for checking purposes.
- The attachment sends three bytes of punch check data to the CPU for checking data that was punched with the data sent to the attachment.
- The card from the selected hopper is sent to the vacated wait station. This card may or may not be read at the read station.

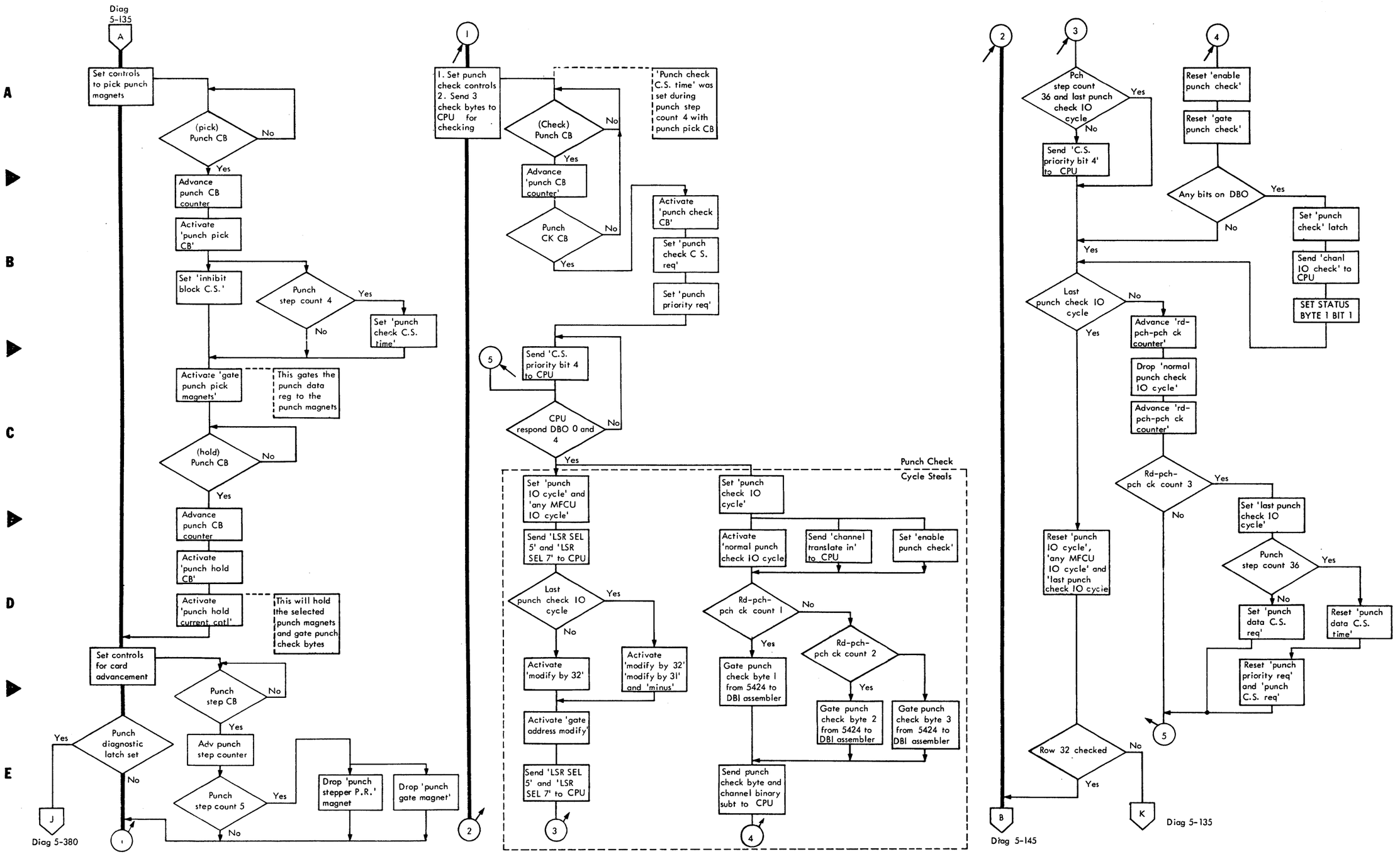
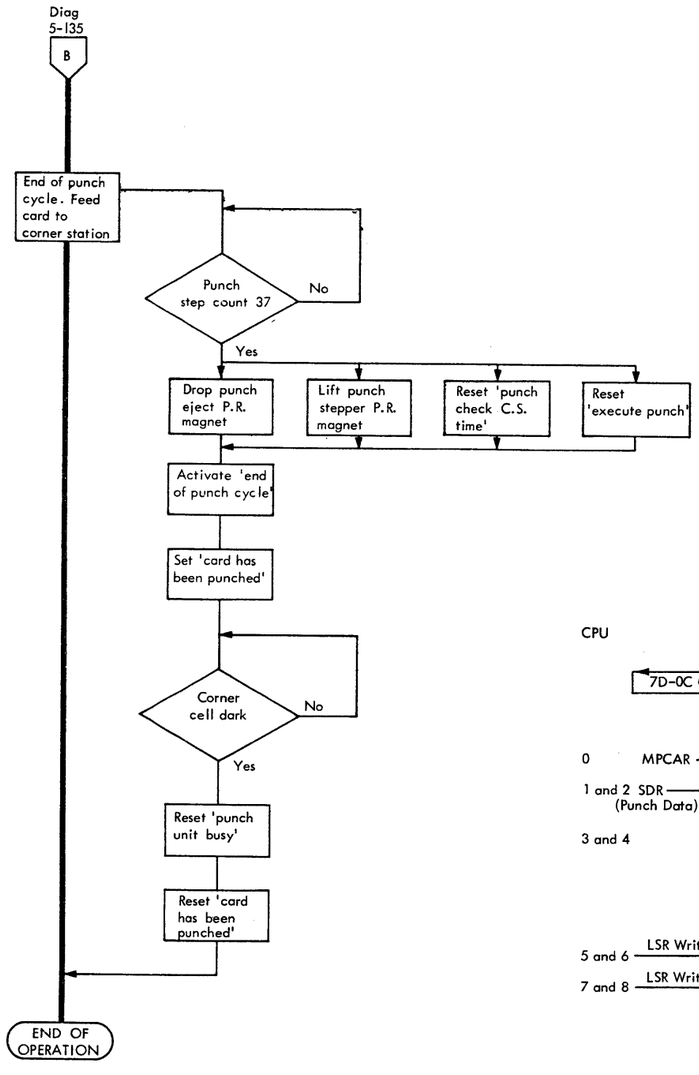
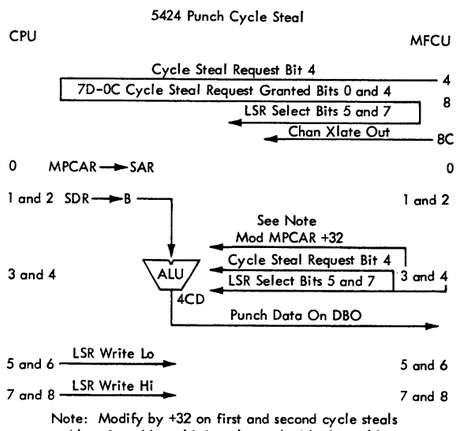
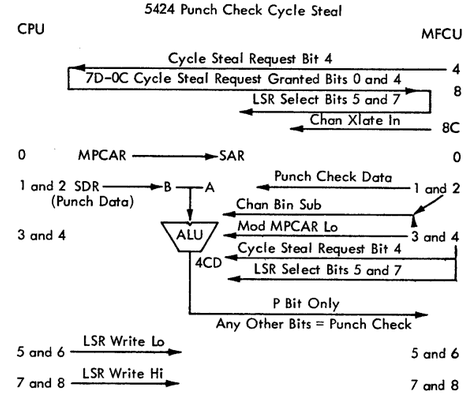


Diagram 5-140. Punch/Feed Operation Flowchart (Part 2 of 11)





Note: Modify by +32 on first and second cycle steals and by minus 64 on third cycle steal with channel binary subtract active to prevent complementing the A register.



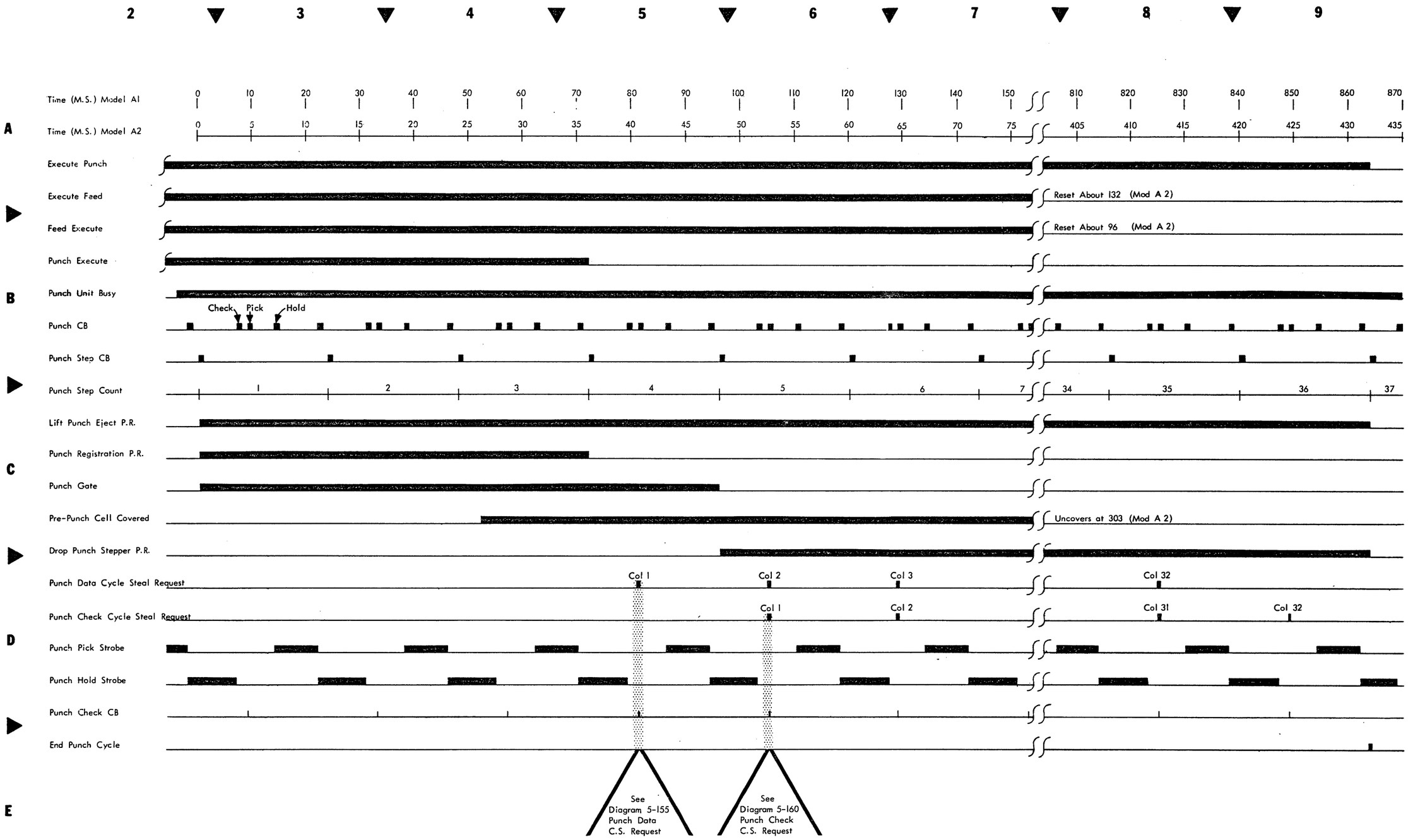
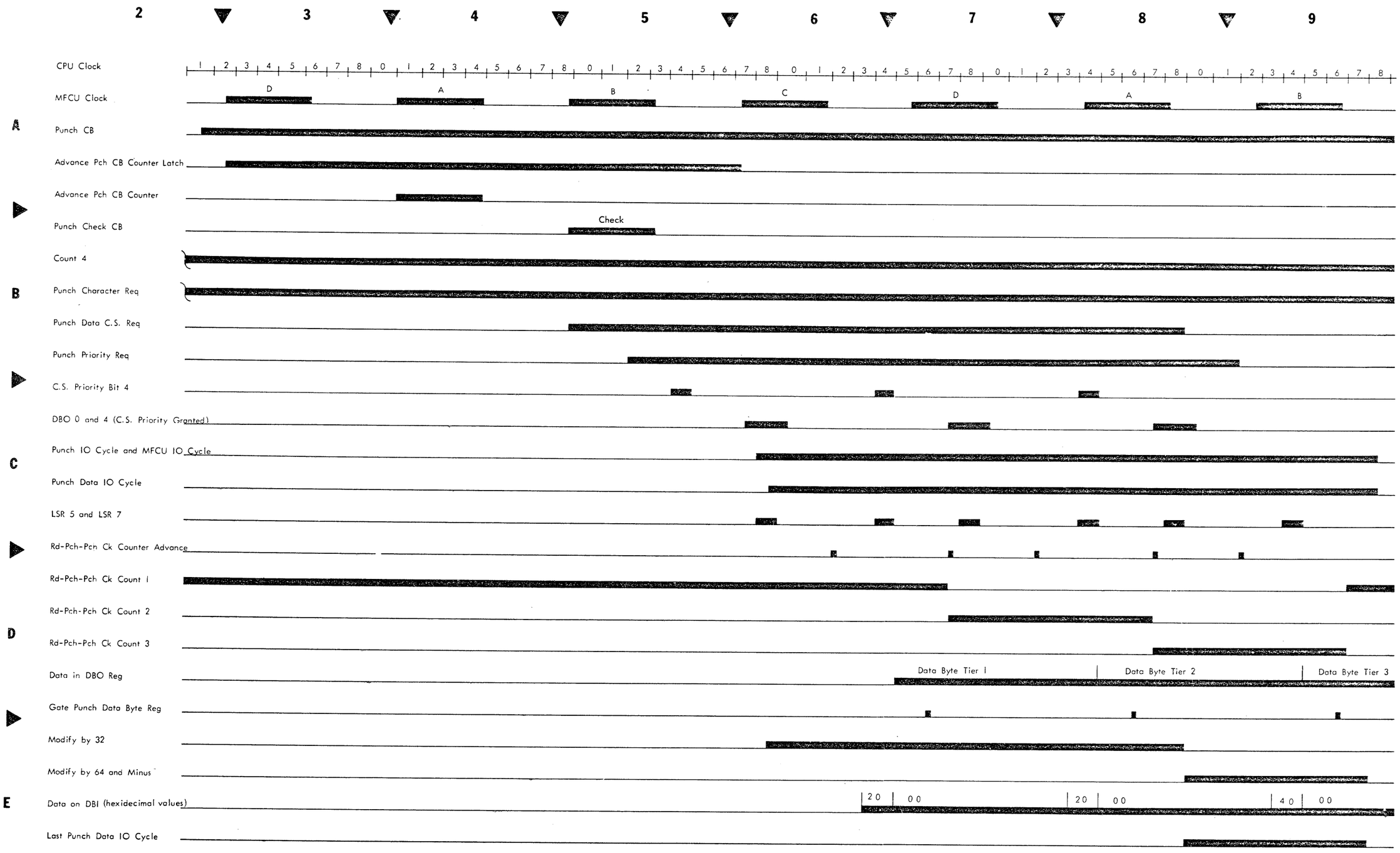


Diagram 5-150. Punch/Feed Timing Chart (Part 4 of 11)


2
3
4
5
6
7
8
9
CPU Clock
MFCU Clock
D
A
B
C
D
A
B
A
Punch CB
Advance Pch CB Counter Latch
Advance Pch CB Counter
Punch Check CB
Check
Count 4
B
Punch Character Req
Punch Data C.S. Req
Punch Priority Req
C.S. Priority Bit 4
DBO 0 and 4 (C.S. Priority Granted)
C
Punch IO Cycle and MFCU IO Cycle
Punch Data IO Cycle
LSR 5 and LSR 7
Rd-Pch-Pch Ck Counter Advance
Rd-Pch-Pch Ck Count 1
Rd-Pch-Pch Ck Count 2
D
Rd-Pch-Pch Ck Count 3
Data in DBO Reg
Data Byte Tier 1
Data Byte Tier 2
Data Byte Tier 3
Gate Punch Data Byte Reg
Modify by 32
Modify by 64 and Minus
E
Data on DBI (hexidecimal values)
20
00
20
00
40
00
Last Punch Data IO Cycle

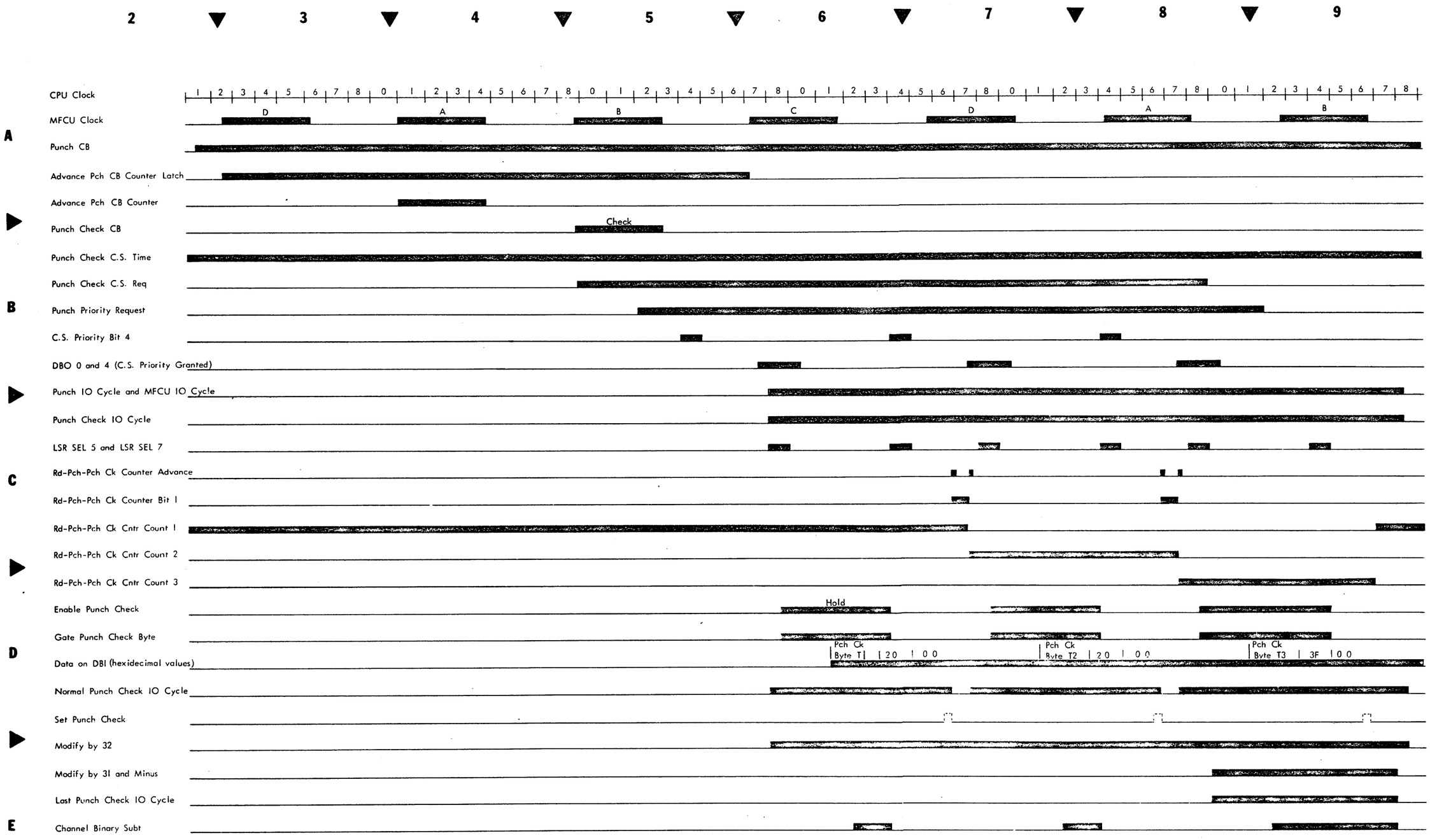
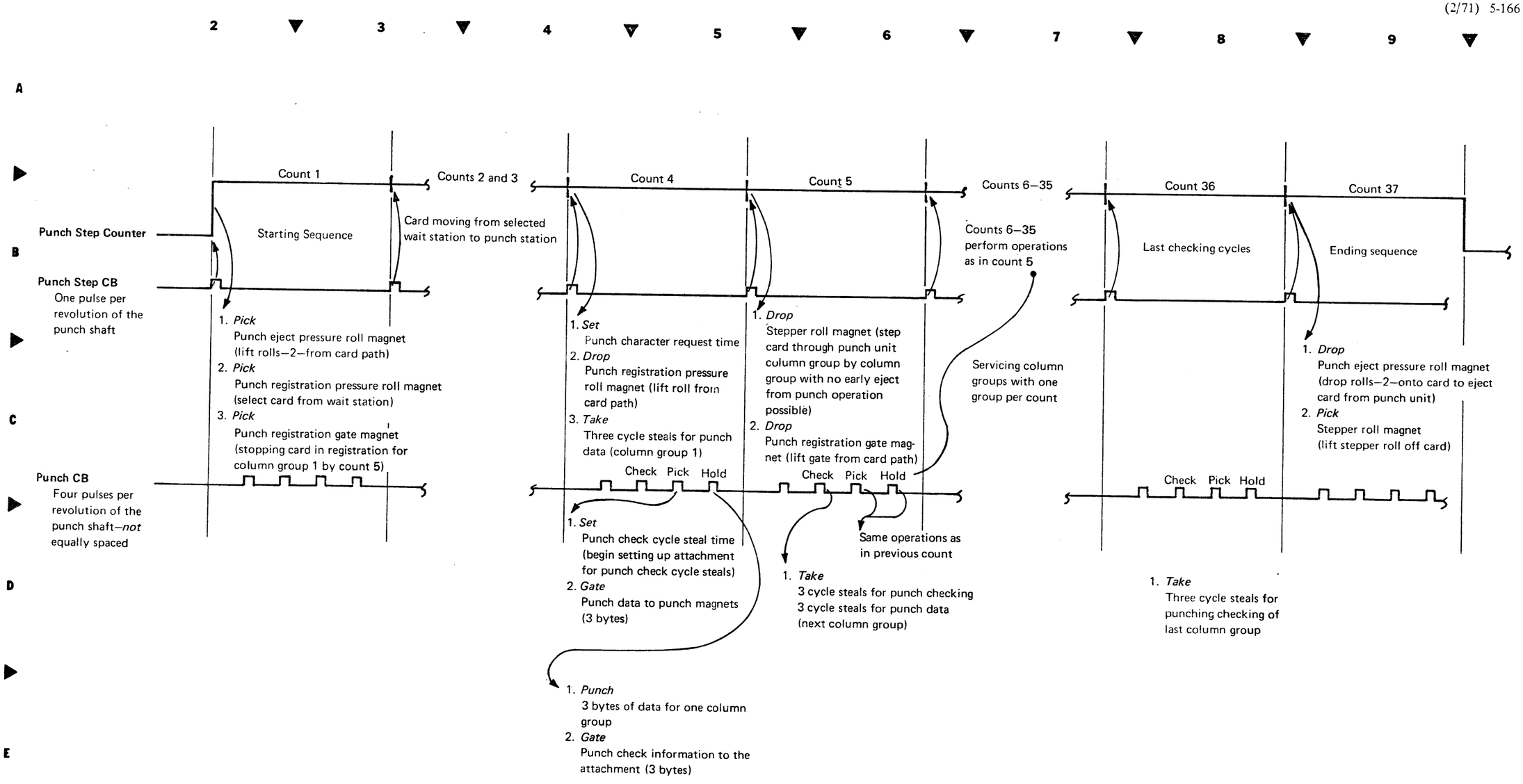
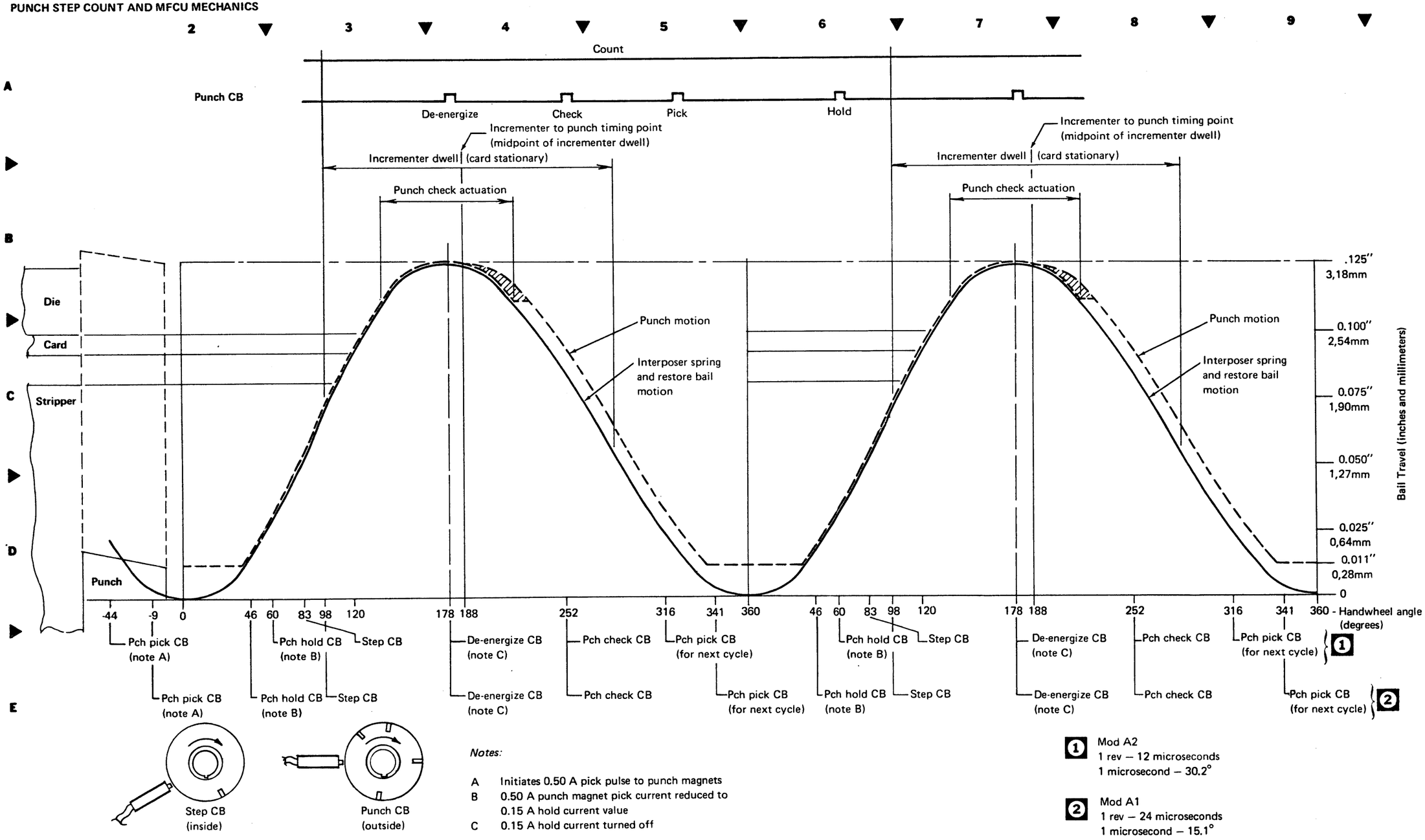


Diagram 5-160. Punch Check Cycle Steal Request (Part 6 of 11)


2
3
4
5
6
7
8
9
A
B
C
D
E
Punch Step Counter
Punch Step CB
One pulse per revolution of the punch shaft
Punch CB
Four pulses per revolution of the punch shaft—not equally spaced
Count 1
Starting Sequence
Counts 2 and 3
Card moving from selected wait station to punch station
1. Pick
Punch eject pressure roll magnet (lift rolls—2—from card path)
2. Pick
Punch registration pressure roll magnet (select card from wait station)
3. Pick
Punch registration gate magnet (stopping card in registration for column group 1 by count 5)
Count 4
Count 5
Counts 6—35
1. Set
Punch character request time
2. Drop
Punch registration pressure roll magnet (lift roll from card path)
3. Take
Three cycle steals for punch data (column group 1)
1. Drop
Stepper roll magnet (step card through punch unit column group by column group with no early eject from punch operation possible)
2. Drop
Punch registration gate magnet (lift gate from card path)
Check Pick Hold
Counts 6—35 perform operations as in count 5
Servicing column groups with one group per count
Same operations as in previous count
1. Set
Punch check cycle steal time (begin setting up attachment for punch check cycle steals)
2. Gate
Punch data to punch magnets (3 bytes)
1. Take
3 cycle steals for punch checking
3 cycle steals for punch data (next column group)
1. Punch
3 bytes of data for one column group
2. Gate
Punch check information to the attachment (3 bytes)
Count 36
Count 37
Last checking cycles
Ending sequence
1. Drop
Punch eject pressure roll magnet (drop rolls—2—onto card to eject card from punch unit)
2. Pick
Stepper roll magnet (lift stepper roll off card)
Check Pick Hold
1. Take
Three cycle steals for punching checking of last column group

TIMING RELATIONSHIP BETWEEN ATTACHMENT PUNCH STEP COUNT AND MFCU MECHANICS



Notes:

A Initiates 0.50 A pick pulse to punch magnets

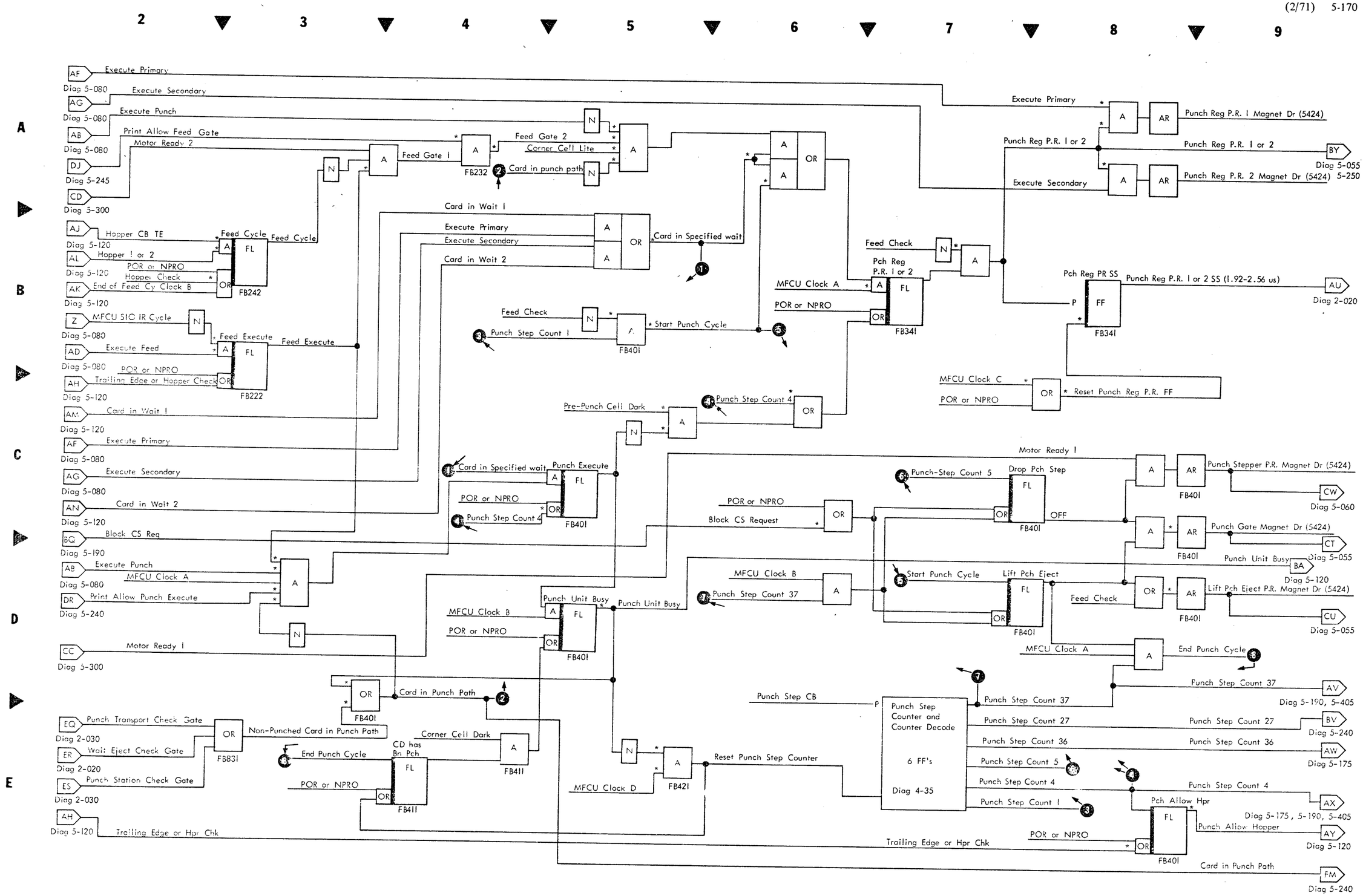
B 0.50 A punch magnet pick current reduced to 0.15 A hold current value

C 0.15 A hold current turned off

1 Mod A2
1 rev – 12 microseconds
1 microsecond – 30.2°

2 Mod A1
1 rev – 24 microseconds
1 microsecond – 15.1°

Diagram 5-168. Timing Relationship Between Attachment Punch Step Count and MFCU Mechanics


2
3
4
5
6
7
8
9
A
B
C
D
E
AF Execute Primary Diag 5-080
AG Execute Secondary Diag 5-080
AB Execute Punch Diag 5-080
DJ Print Allow Feed Gate Diag 5-245
CD Motor Ready 2 Diag 5-300
AJ Hopper CB TE Diag 5-120
AL Hopper 1 or 2 Diag 5-120
AK POR or NPRO Hopper Check End of Feed Cy Clock B Diag 5-120
FB242
Feed Cycle
Z MFCU SIO IR Cycle Diag 5-080
AD Execute Feed Diag 5-080
AH POR or NPRO Trailing Edge or Hopper Check Diag 5-120
FB222
Feed Execute
AM Card in Wait 1 Diag 5-120
AF Execute Primary Diag 5-080
AG Execute Secondary Diag 5-080
AN Card in Wait 2 Diag 5-120
BQ Block CS Req Diag 5-190
AB Execute Punch Diag 5-080
DR Print Allow Punch Execute Diag 5-240
MFCU Clock A
CC Motor Ready 1 Diag 5-300
Feed Gate 1
Feed Gate 2
Corner Cell Lite
Card in punch path
FB232
Card in Wait 1
Execute Primary
Execute Secondary
Card in Wait 2
Card in Specified wait
Feed Check
Punch Step Count 1
Start Punch Cycle
FB401
Pre-Punch Cell Dark
Punch Step Count 4
Punch Execute
POR or NPRO
Punch Unit Busy
MFCU Clock B
Card in Punch Path
EQ Punch Transport Check Gate Diag 2-030
ER Wait Eject Check Gate Diag 2-020
ES Punch Station Check Gate Diag 2-030
FB831
Non-Punched Card in Punch Path
End Punch Cycle
CD has Bn Pch
Corner Cell Dark
FB411
MFCU Clock D
FB421
Reset Punch Step Counter
Punch Step CB
Punch Step Counter and Counter Decode
6 FF's
Diag 4-35
Punch Step Count 37
Punch Step Count 27
Punch Step Count 36
Punch Step Count 5
Punch Step Count 4
Punch Step Count 1
Trailing Edge or Hpr Chk
Execute Primary
Punch Reg P.R. 1 Magnet Dr (5424)
Punch Reg P.R. 1 or 2
BY Diag 5-055
Execute Secondary
Punch Reg P.R. 2 Magnet Dr (5424) 5-250
MFCU Clock C
Reset Punch Reg P.R. FF
Pch Reg PR SS
Punch Reg P.R. 1 or 2 SS (1.92-2.56 us)
AU Diag 2-020
FB341
Motor Ready 1
Punch-Step Count 5
Drop Pch Step
OFF
Punch Stepper P.R. Magnet Dr (5424)
CW Diag 5-060
Punch Gate Magnet Dr (5424)
CT Diag 5-055
Punch Unit Busy
BA Diag 5-120
Lift Pch Eject
Lift Pch Eject P.R. Magnet Dr (5424)
CU Diag 5-055
End Punch Cycle
AV Diag 5-190, 5-405
BV Diag 5-240
AW Diag 5-175
AX Diag 5-175, 5-190, 5-405
Pch Allow Hpr
Punch Allow Hopper
AY Diag 5-120
FM Diag 5-240

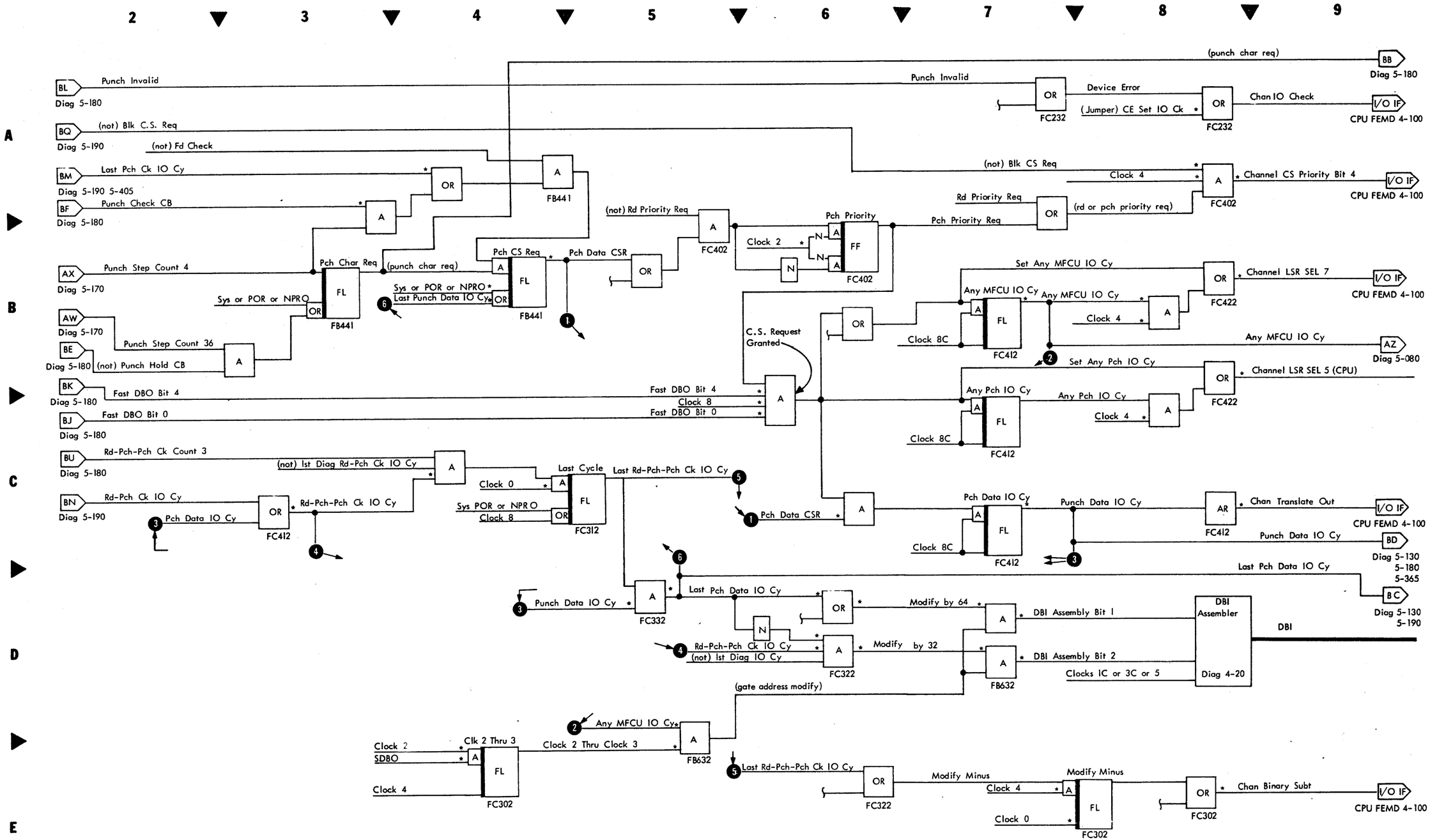
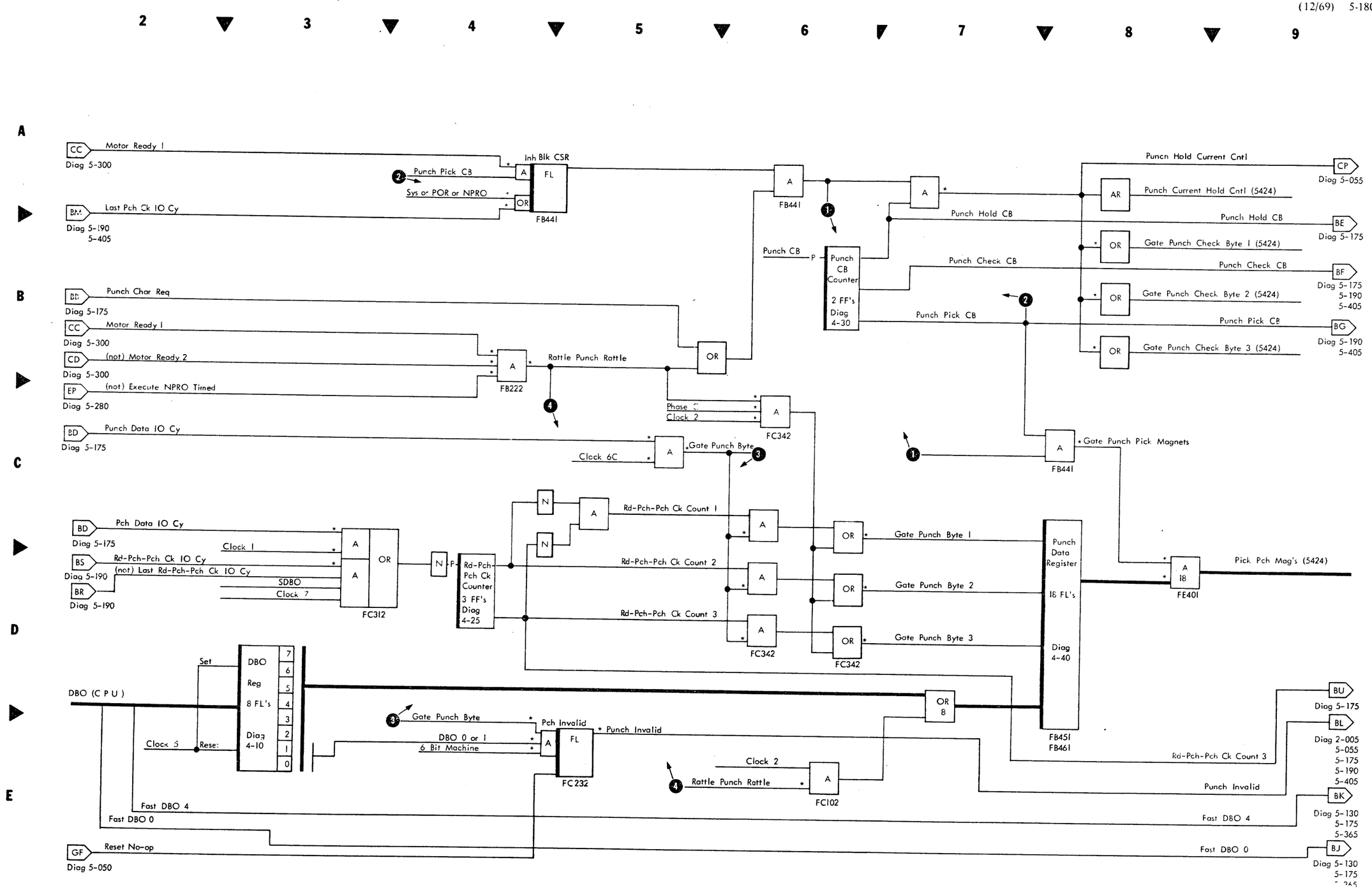


Diagram 5-175. Punch Data Cycle Steal Channel Controls (Part 8 of 11)


2
3
4
5
6
7
8
9
A
B
C
D
E
CC
Motor Ready 1
Diag 5-300
BM
Last Pch Ck IO Cy
Diag 5-190
5-405
Inh Blk CSR
Punch Pick CB
Sys or POR or NPRO
A
OR
FL
FB441
BB
Punch Char Req
Diag 5-175
CD
(not) Motor Ready 2
Diag 5-300
EP
(not) Execute NPRO Timed
Diag 5-280
A
FB222
Rattle Punch Rattle
OR
Phase C Clock 2
A
FC342
BD
Punch Data IO Cy
Diag 5-175
Clock 6C
A
Gate Punch Byte
Punch CB
P
Punch CB Counter
2 FF's
Diag 4-30
Punch Hold CB
Punch Check CB
Punch Pick CB
A
FB441
Punch Hold Current Cntl
CP
Diag 5-055
AR
Punch Current Hold Cntl (5424)
Punch Hold CB
BE
Diag 5-175
OR
Gate Punch Check Byte 1 (5424)
Punch Check CB
BF
Diag 5-175
5-190
5-405
OR
Gate Punch Check Byte 2 (5424)
Punch Pick CB
BG
Diag 5-190
5-405
OR
Gate Punch Check Byte 3 (5424)
A
FB441
Gate Punch Pick Magnets
BD
Pch Data IO Cy
Diag 5-175
BS
Rd-Pch-Pch Ck IO Cy
(not) Last Rd-Pch-Pch Ck IO Cy
Diag 5-190
BR
Diag 5-190
Clock 1
SDBO
Clock 7
A
A
OR
FC312
N
P
Rd-Pch-Pch Ck Counter
3 FF's
Diag 4-25
N
N
A
Rd-Pch-Pch Ck Count 1
Rd-Pch-Pch Ck Count 2
Rd-Pch-Pch Ck Count 3
A
A
A
FC342
OR
OR
OR
FC342
Gate Punch Byte 1
Gate Punch Byte 2
Gate Punch Byte 3
Punch Data Register
16 FL's
Diag 4-40
FB451
FB461
A
18
FE401
Pick Pch Mag's (5424)
DBO (C P U)
Set
DBO Reg
8 FL's
Diag 4-10
7
6
5
4
3
2
1
0
Clock 5
Rese:
Gate Punch Byte
Pch Invalid
DBO 0 or 1
6 Bit Machine
A
FL
FC232
Punch Invalid
OR
8
Clock 2
Rattle Punch Rattle
A
FC102
Fast DBO 4
Fast DBO 0
GF
Reset No-op
Diag 5-050
BU
Diag 5-175
BL
Diag 2-005
5-055
5-175
5-190
5-405
Rd-Pch-Pch Ck Count 3
Punch Invalid
BK
Diag 5-130
5-175
5-365
Fast DBO 4
Fast DBO 0
BJ
Diag 5-130
5-175

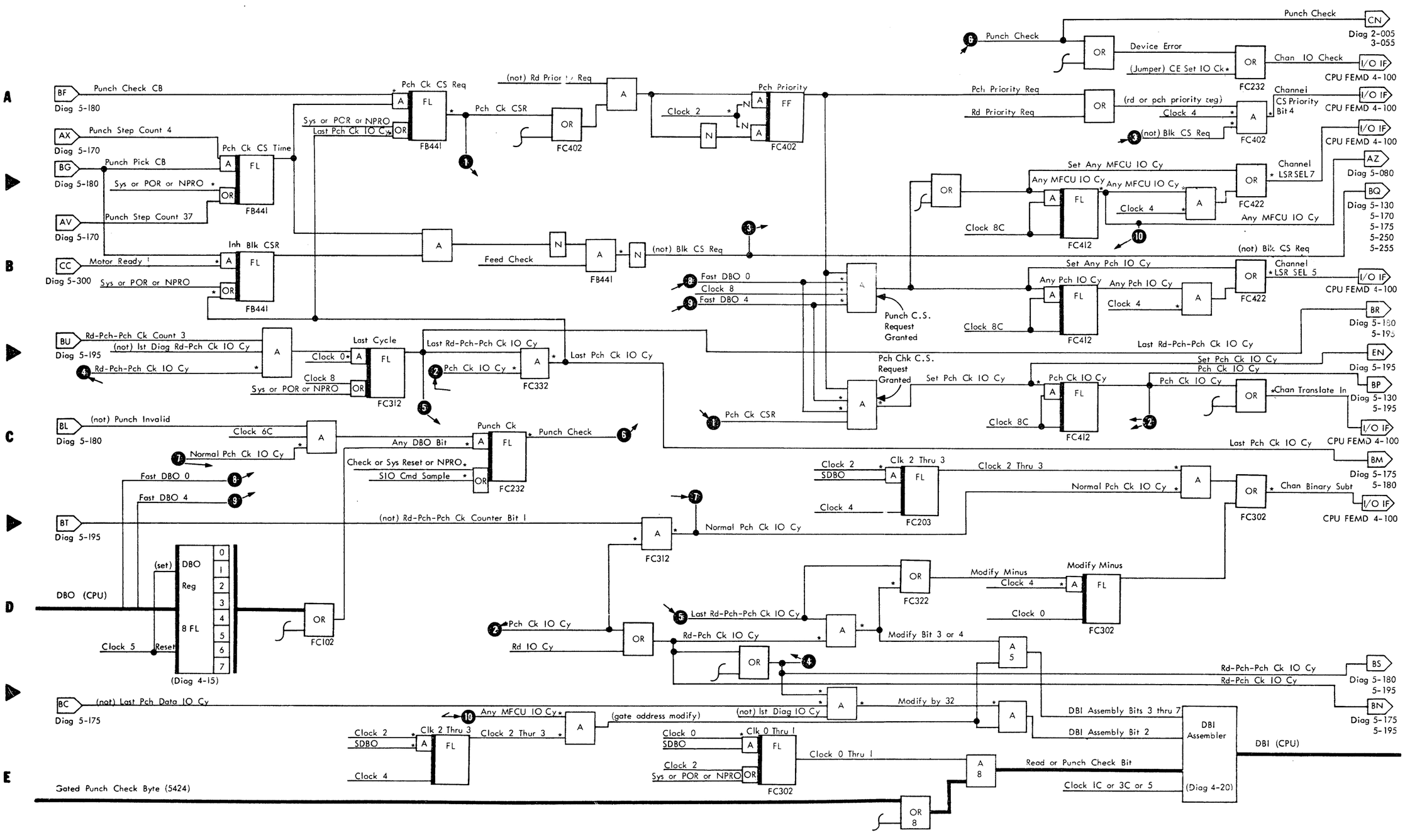
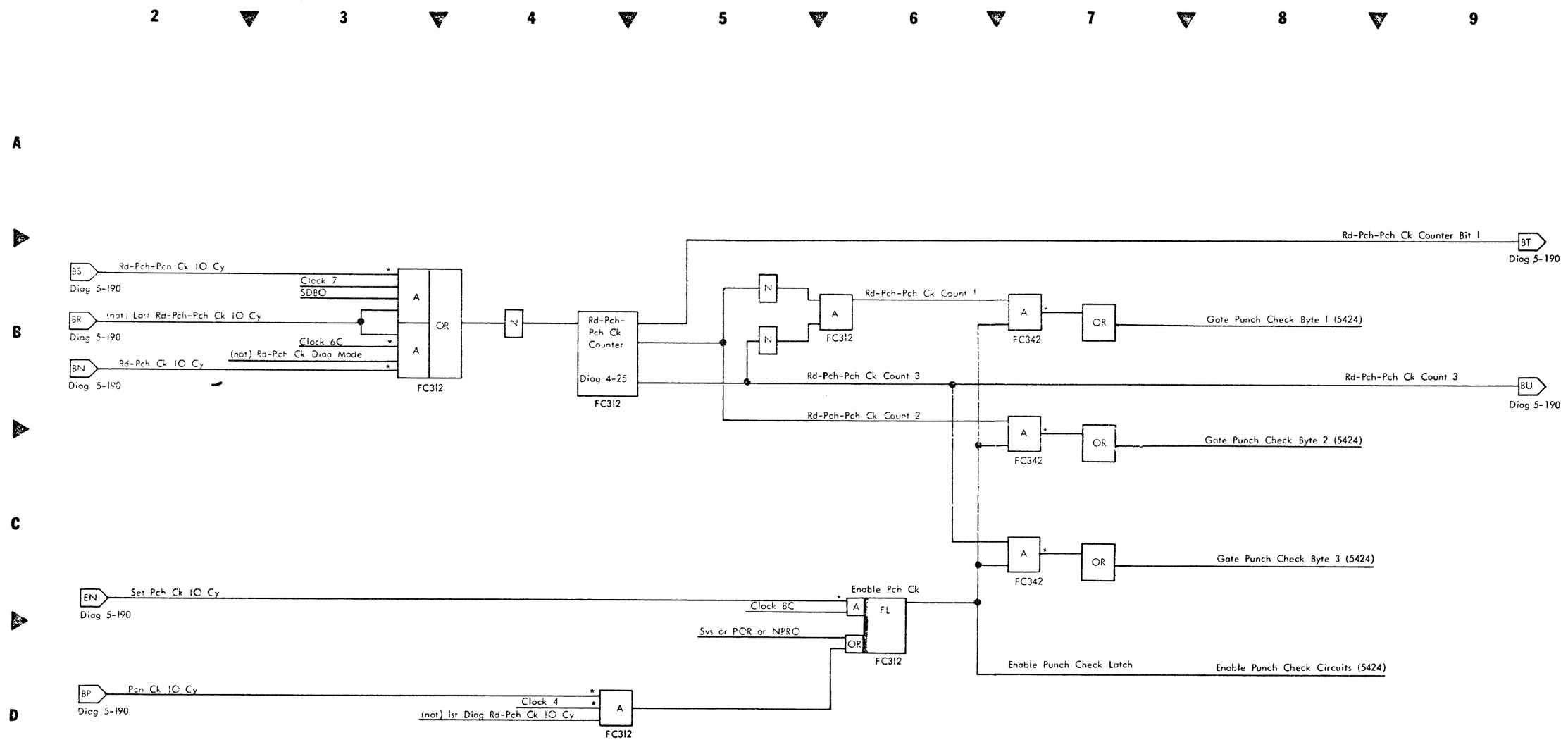
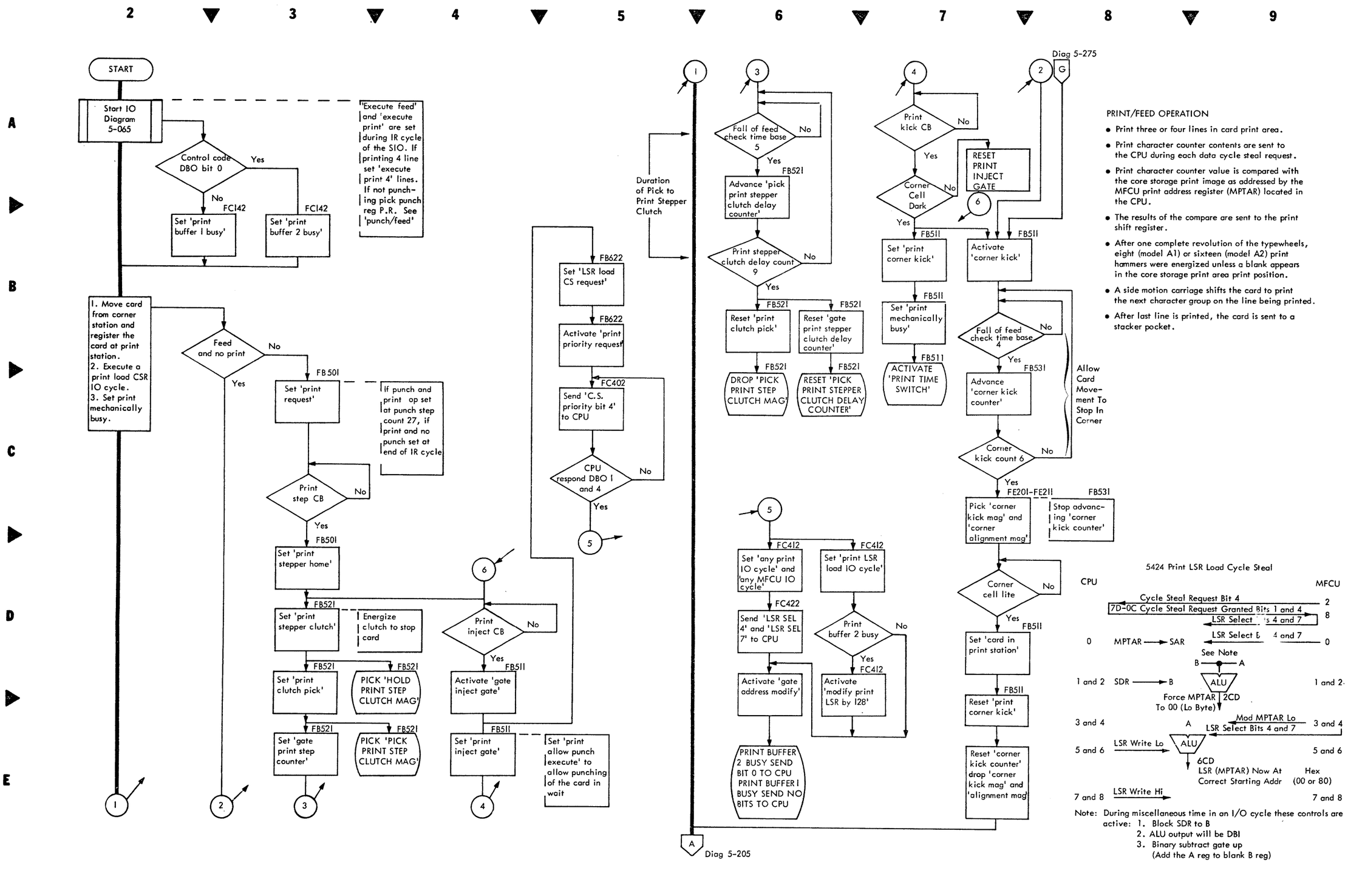


Diagram 5-190. Punch Check Cycle Steal Channel Controls (Part 10 of 11)


2
3
4
5
6
7
8
9
A
B
C
D
E
BS
Rd-Pch-Pch Ck 10 Cy
Diag 5-190
Clock 7
SDBO
BR
(not) Last Rd-Pch-Pch Ck 10 Cy
Diag 5-190
Clock 6C
(not) Rd-Pch Ck Diag Mode
BN
Rd-Pch Ck 10 Cy
Diag 5-190
A
A
OR
FC312
N
Rd-Pch-Pch Ck Counter
Diag 4-25
FC312
Rd-Pch-Pch Ck Counter Bit 1
BT
Diag 5-190
N
N
A
FC312
Rd-Pch-Pch Ck Count 1
A
FC342
OR
Gate Punch Check Byte 1 (5424)
Rd-Pch-Pch Ck Count 3
Rd-Pch-Pch Ck Count 3
BU
Diag 5-190
Rd-Pch-Pch Ck Count 2
A
FC342
OR
Gate Punch Check Byte 2 (5424)
A
FC342
OR
Gate Punch Check Byte 3 (5424)
EN
Set Pch Ck 10 Cy
Diag 5-190
Enable Pch Ck
Clock 8C
Sys or PCR or NPRO
A
OR
FL
FC312
Enable Punch Check Latch
Enable Punch Check Circuits (5424)
BP
Pch Ck 10 Cy
Diag 5-190
Clock 4
(not) 1st Diag Rd-Pch Ck 10 Cy
A
FC312



PRINT/FEED OPERATION

- Print three or four lines in card print area.
- Print character counter contents are sent to the CPU during each data cycle steal request.
- Print character counter value is compared with the core storage print image as addressed by the MFCU print address register (MPTAR) located in the CPU.
- The results of the compare are sent to the print shift register.
- After one complete revolution of the typewheels, eight (model A1) or sixteen (model A2) print hammers were energized unless a blank appears in the core storage print area print position.
- A side motion carriage shifts the card to print the next character group on the line being printed.
- After last line is printed, the card is sent to a stacker pocket.

5424 Print LSR Load Cycle Steal

Note: During miscellaneous time in an I/O cycle these controls are active:
1. Block SDR to B
2. ALU output will be DBI
3. Binary subtract gate up (Add the A reg to blank B reg)

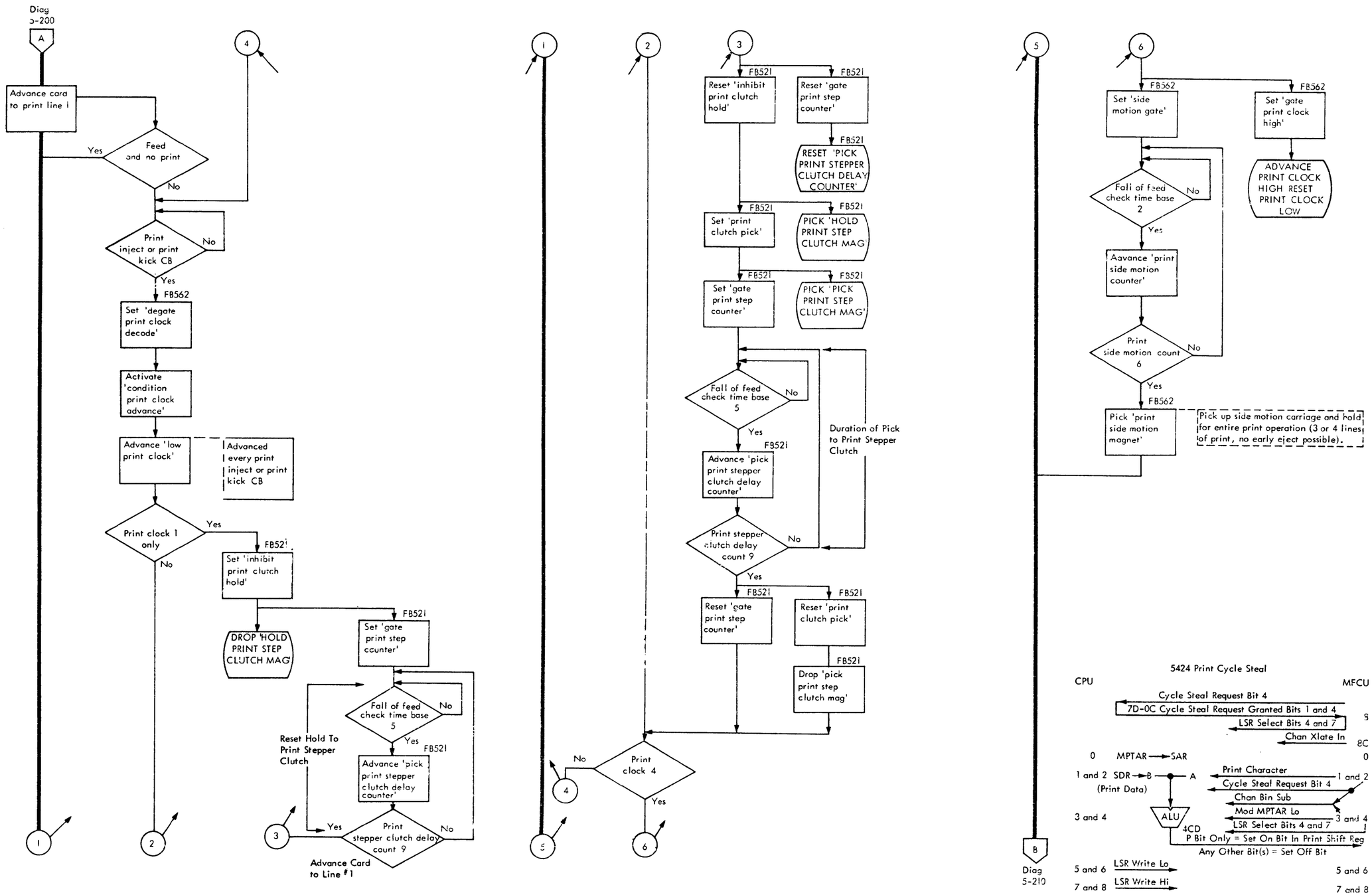
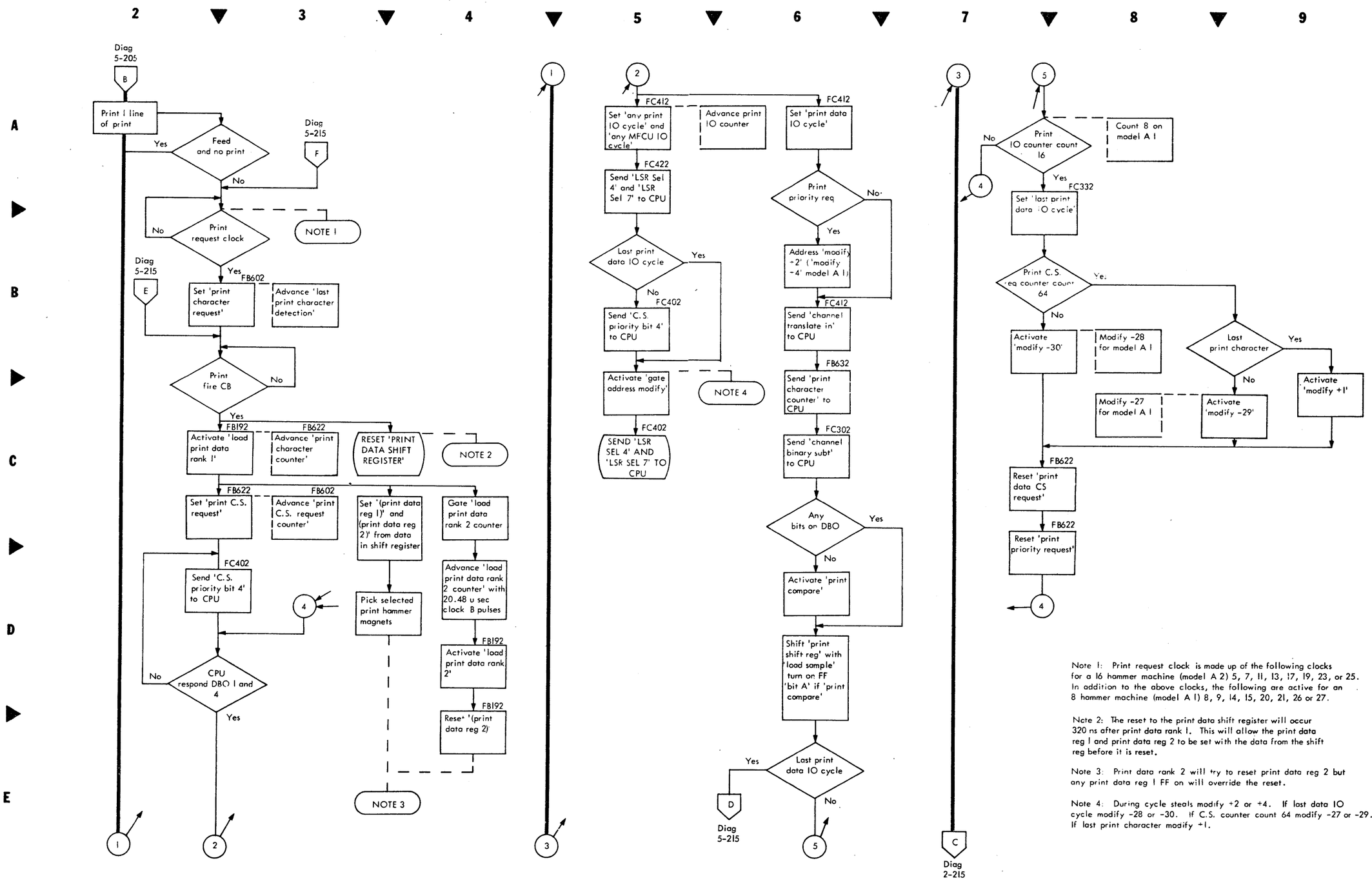


Diagram 5-205. Print/Feed Operation Flowchart (Part 2 of 14)



Note 1: Print request clock is made up of the following clocks for a 16 hammer machine (model A 2) 5, 7, 11, 13, 17, 19, 23, or 25. In addition to the above clocks, the following are active for an 8 hammer machine (model A 1) 8, 9, 14, 15, 20, 21, 26 or 27.

Note 2: The reset to the print data shift register will occur 320 ns after print data rank 1. This will allow the print data reg 1 and print data reg 2 to be set with the data from the shift reg before it is reset.

Note 3: Print data rank 2 will try to reset print data reg 2 but any print data reg 1 FF on will override the reset.

Note 4: During cycle steals modify +2 or +4. If last data IO cycle modify -28 or -30. If C.S. counter count 64 modify -27 or -29. If last print character modify +1.

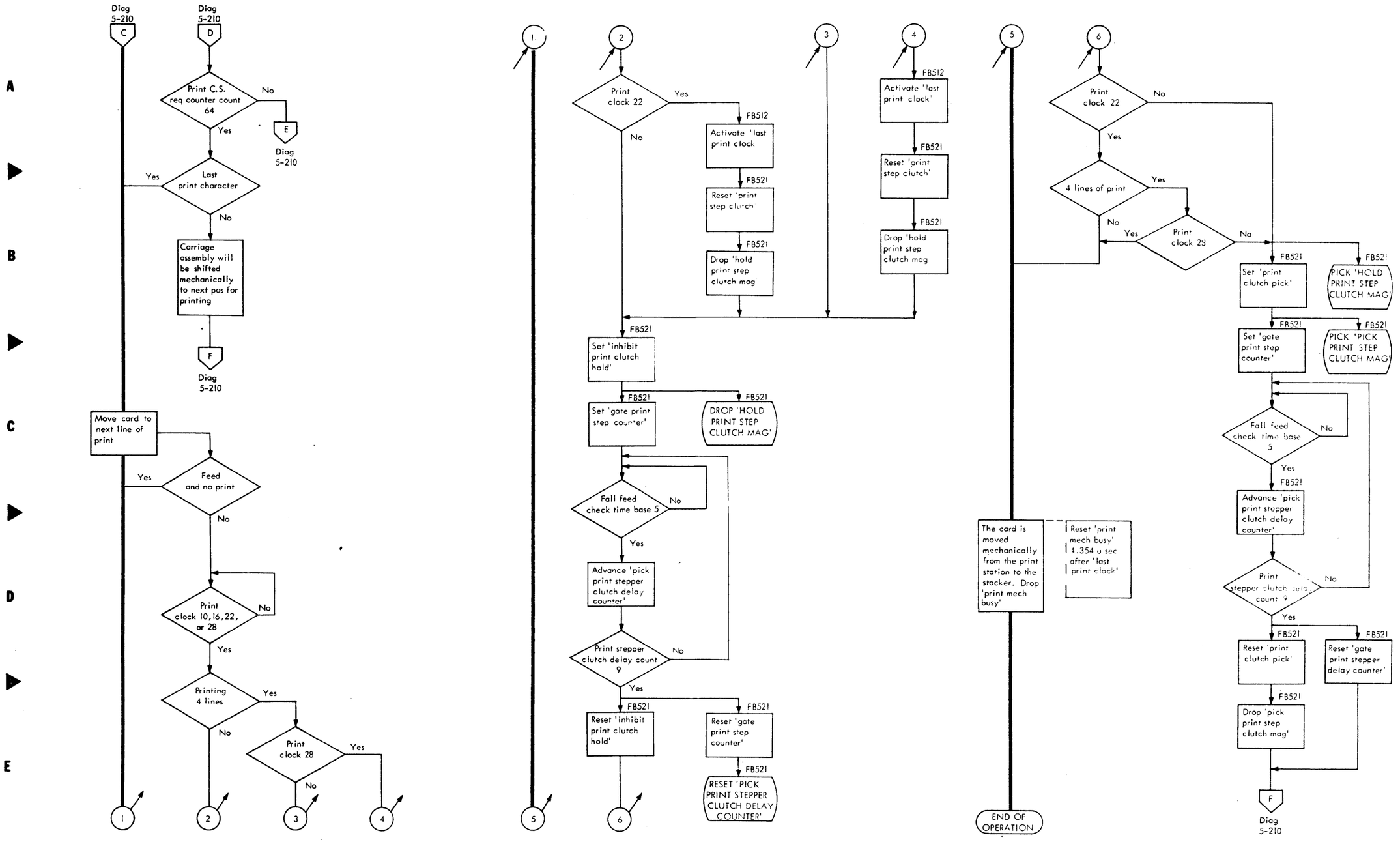
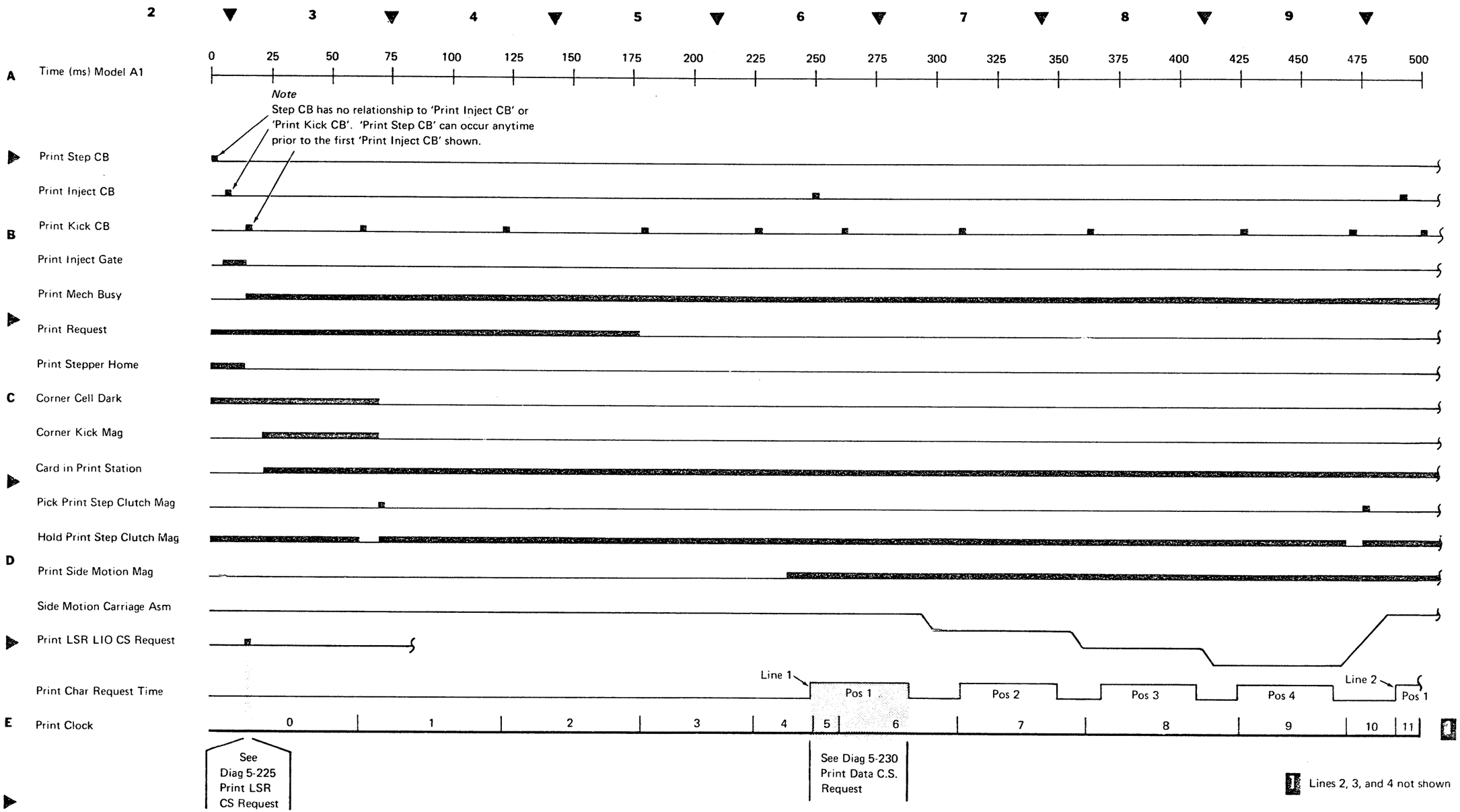
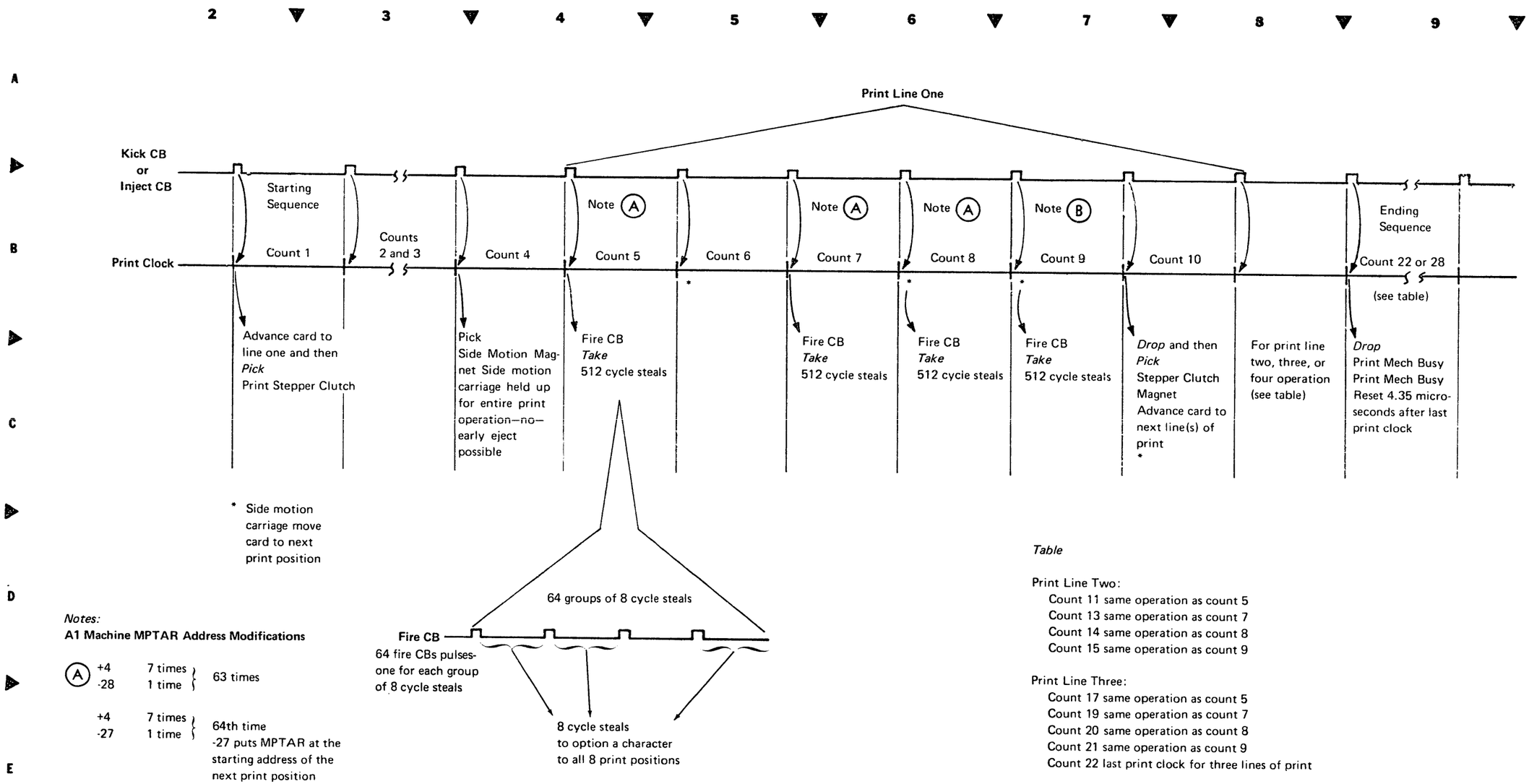


Diagram 5-215. Print/Feed Operation Flowchart (Part 4 of 14)


2
3
4
5
6
7
8
9
A
Time (ms) Model A1
0 25 50 75 100 125 150 175 200 225 250 275 300 325 350 375 400 425 450 475 500
Note
Step CB has no relationship to 'Print Inject CB' or 'Print Kick CB'. 'Print Step CB' can occur anytime prior to the first 'Print Inject CB' shown.
Print Step CB
Print Inject CB
B
Print Kick CB
Print Inject Gate
Print Mech Busy
Print Request
Print Stepper Home
C
Corner Cell Dark
Corner Kick Mag
Card in Print Station
Pick Print Step Clutch Mag
Hold Print Step Clutch Mag
D
Print Side Motion Mag
Side Motion Carriage Asm
Print LSR LIO CS Request
Print Char Request Time
Line 1
Pos 1
Pos 2
Pos 3
Pos 4
Line 2
Pos 1
E
Print Clock
0 1 2 3 4 5 6 7 8 9 10 11
See Diag 5-225 Print LSR CS Request
See Diag 5-230 Print Data C.S. Request
Lines 2, 3, and 4 not shown

PRINT OPERATION A-1 MODEL MACHINE



* Side motion carriage move card to next print position

Notes:

A1 Machine MPTAR Address Modifications

(A)	+4	7 times	63 times
	-28	1 time	
	+4	7 times	64th time -27 puts MPTAR at the starting address of the next print position
	-27	1 time	
(B)	+4	7 times	63 times
	-28	1 time	
	+4	7 times	64th time +1 puts MPTAR at the start address of the next line of print
	+1	1 time	

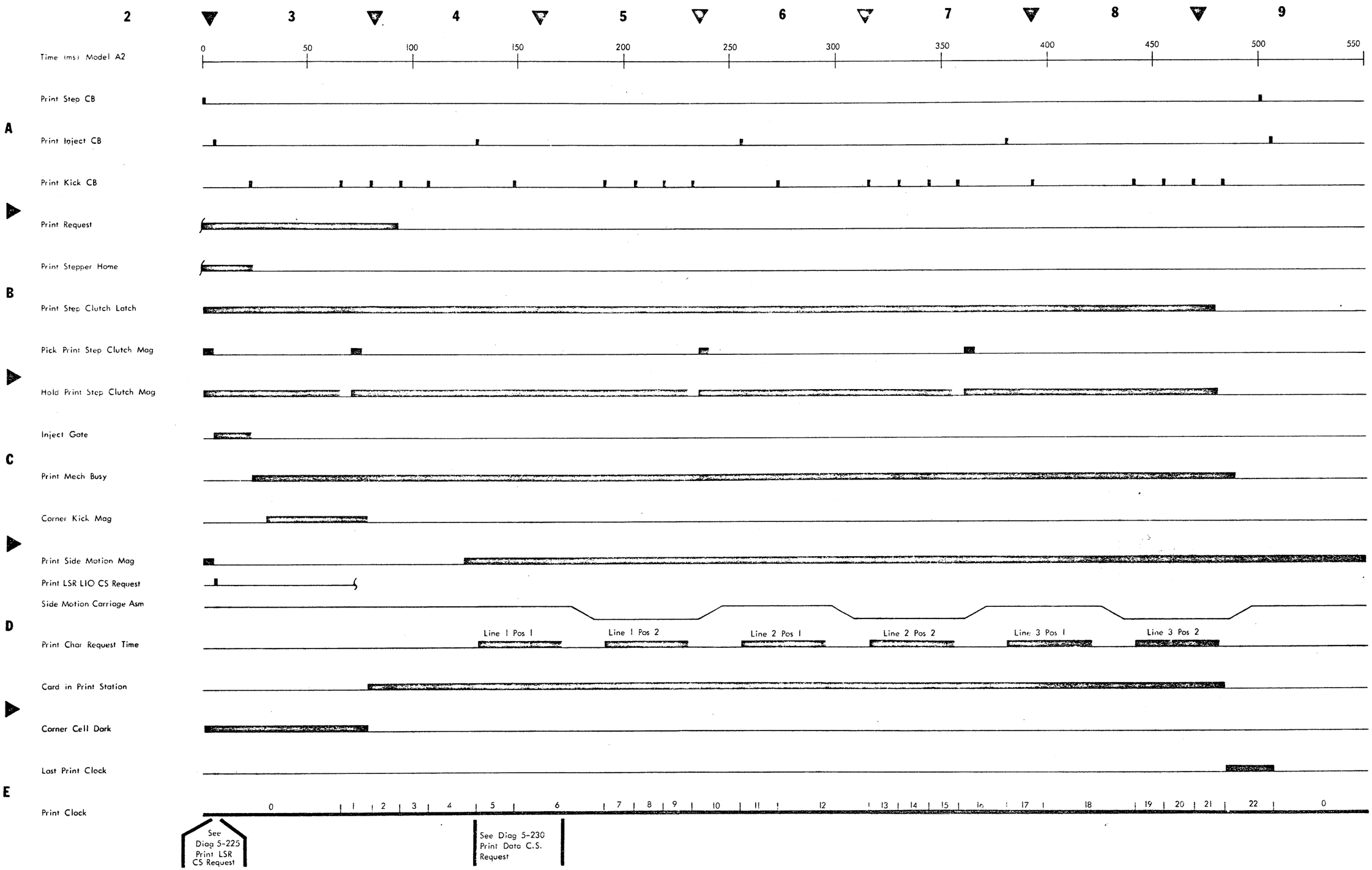
Table

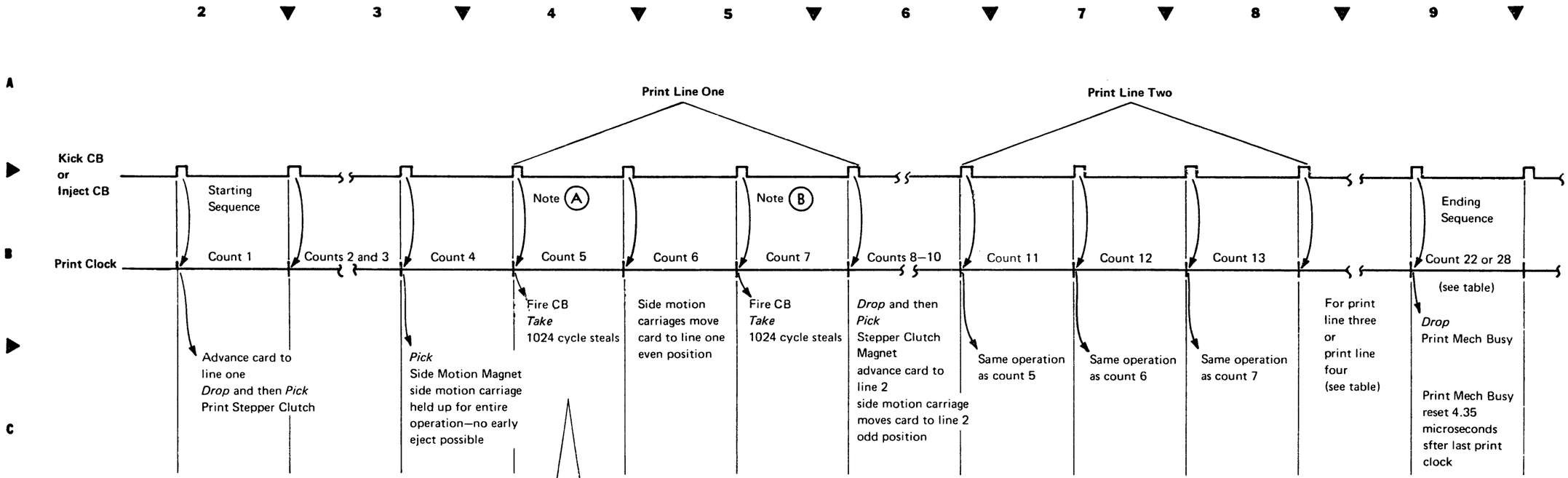
Print Line Two:
- Count 11 same operation as count 5
- Count 13 same operation as count 7
- Count 14 same operation as count 8
- Count 15 same operation as count 9

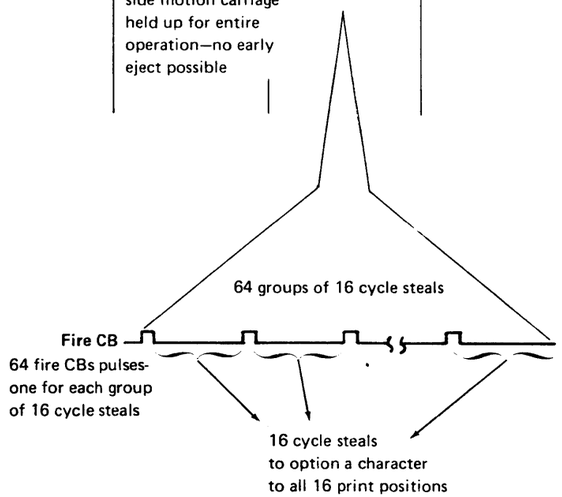
Print Line Three:
- Count 17 same operation as count 5
- Count 19 same operation as count 7
- Count 20 same operation as count 8
- Count 21 same operation as count 9
- Count 22 last print clock for three lines of print

Print Line Four:
- Count 23 same operation as count 5
- Count 25 same operation as count 7
- Count 26 same operation as count 8
- Count 27 same operation as count 9
- Count 28 last print clock for four lines of print

Diagram 5-219. Print Operation A-1 Model Machine


2
3
4
5
6
7
8
9
Time (ms) Model A2
0
50
100
150
200
250
300
350
400
450
500
550
A
Print Step CB
Print Inject CB
Print Kick CB
Print Request
Print Stepper Home
B
Print Step Clutch Latch
Pick Print Step Clutch Mag
Hold Print Step Clutch Mag
Inject Gate
C
Print Mech Busy
Corner Kick Mag
Print Side Motion Mag
Print LSR LIO CS Request
Side Motion Carriage Asm
D
Print Char Request Time
Line 1 Pos 1
Line 1 Pos 2
Line 2 Pos 1
Line 2 Pos 2
Line 3 Pos 1
Line 3 Pos 2
Card in Print Station
Corner Cell Dark
Last Print Clock
E
Print Clock
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 0
See Diag 5-225 Print LSR CS Request
See Diag 5-230 Print Data C.S. Request





Notes:

A2 Macine MPTAR Address Modification

(A) Odd Position (1, 3, 5, . . . 29, 31)

+2	15 times	63 times
-30	1 time	
+2	15 times	64th time
-29	1 time	-29 puts MPTAR at the starting address of next even position

(B) Even Position (2, 4, 6, . . . 30, 32)

+2	15 times	63 times
-30	1 time	
+2	15 times	64th time
+1	1 time	+1 puts MPTAR at the starting address of next odd position

Table

Print Line Three:
- Count 17 same operation as count 5
- Count 18 same operation as count 6
- Count 19 same operation as count 7
- Count 22 starts ending sequence (last print clock for three lines of print)

Print Line Four:
- Count 23 same operation as count 5
- Count 24 same operation as count 6
- Count 25 same operation as count 7
- Count 28 starts ending sequence (last print clock for four lines of print)

Diagram 5-224. Print Operation A-2 Model Machine

2 3 4 5 6 7 8 9

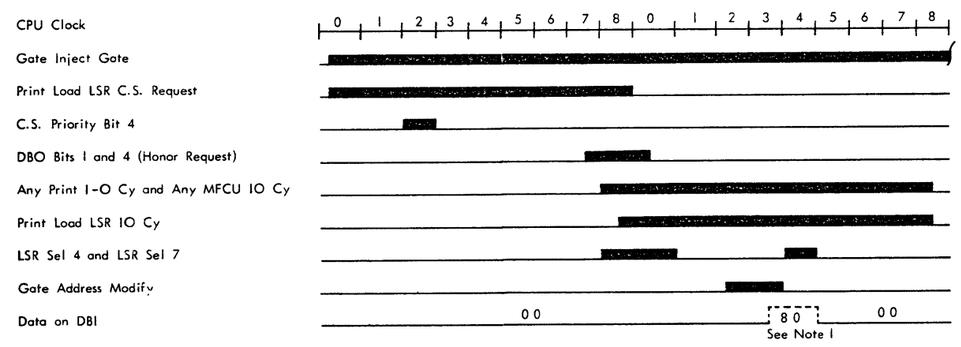
A

B

C

D

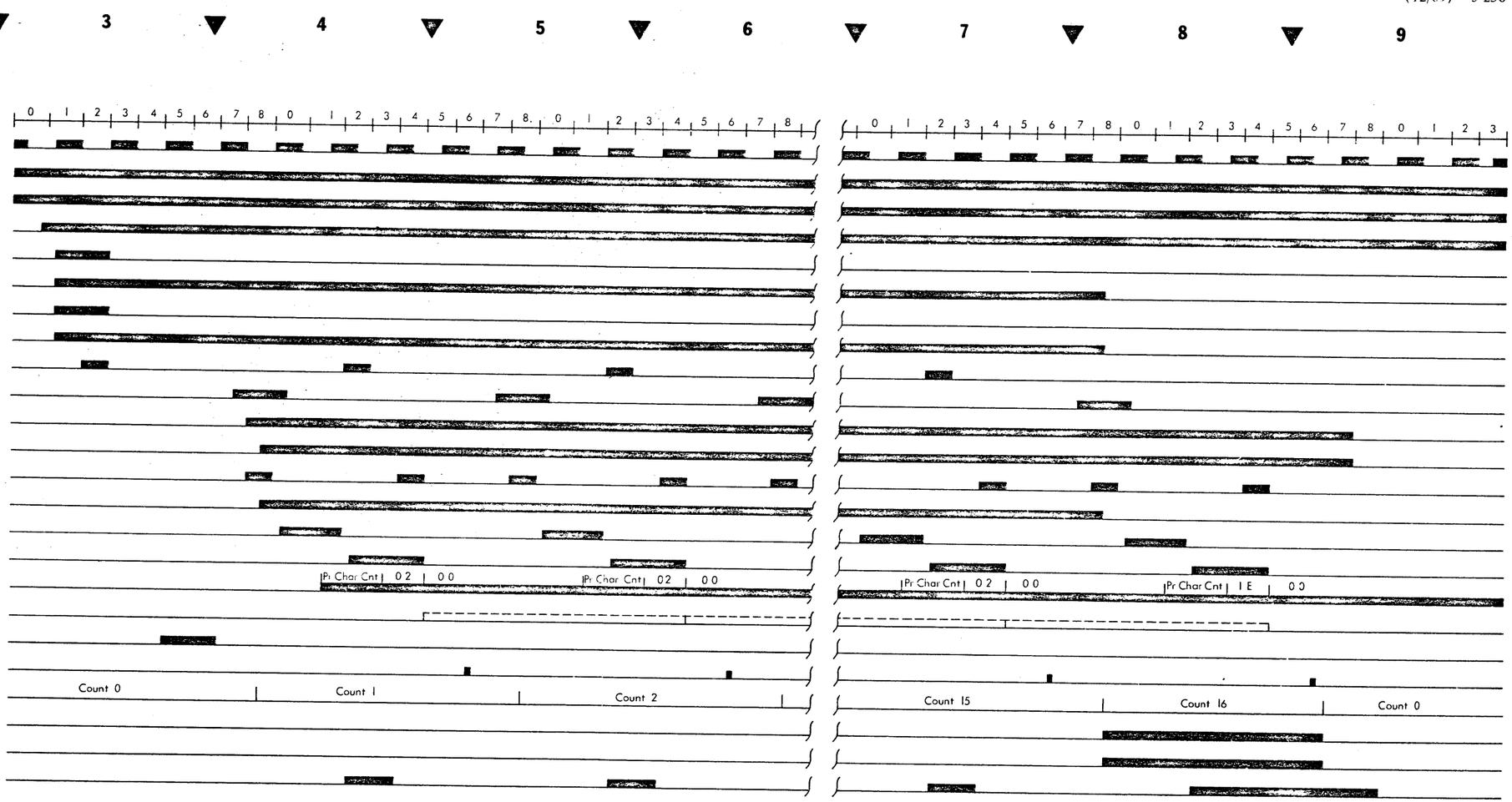
E



Note 1: If Print Buffer 2 Busy Address Modify by 128 (80). If Print Buffer 1 Busy Modify by 0 (0 0)

Diagram 5-225. Print/Feed Print Load LSR Cycle Steal Request (Part 6 of 14)

Diagram 5-230. Print Data Cycle Steal Request Timing Chart (Part 7 of 14)



Note 1: Print Request Clock is Activated for the following Clocks (model A2); 5,7,11,13,17,19,23, and 25. In Addition to the Above Clocks, the following are active for a Model A 1; 8,9,14,15,20,21,26, and 27.

Note 2: Gate Print Compare is Active Only if DBO has no bits

Note 3: Print Shift Register will be set Only if DBO has no bits

2 3 4 5 6 7 8 9

A

B

C

D

E

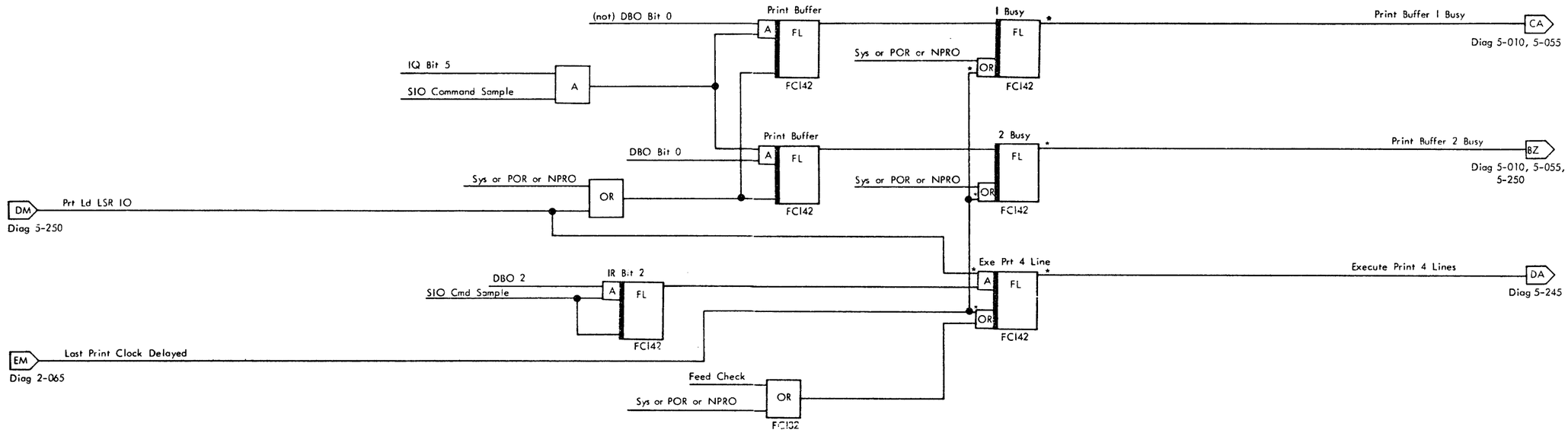
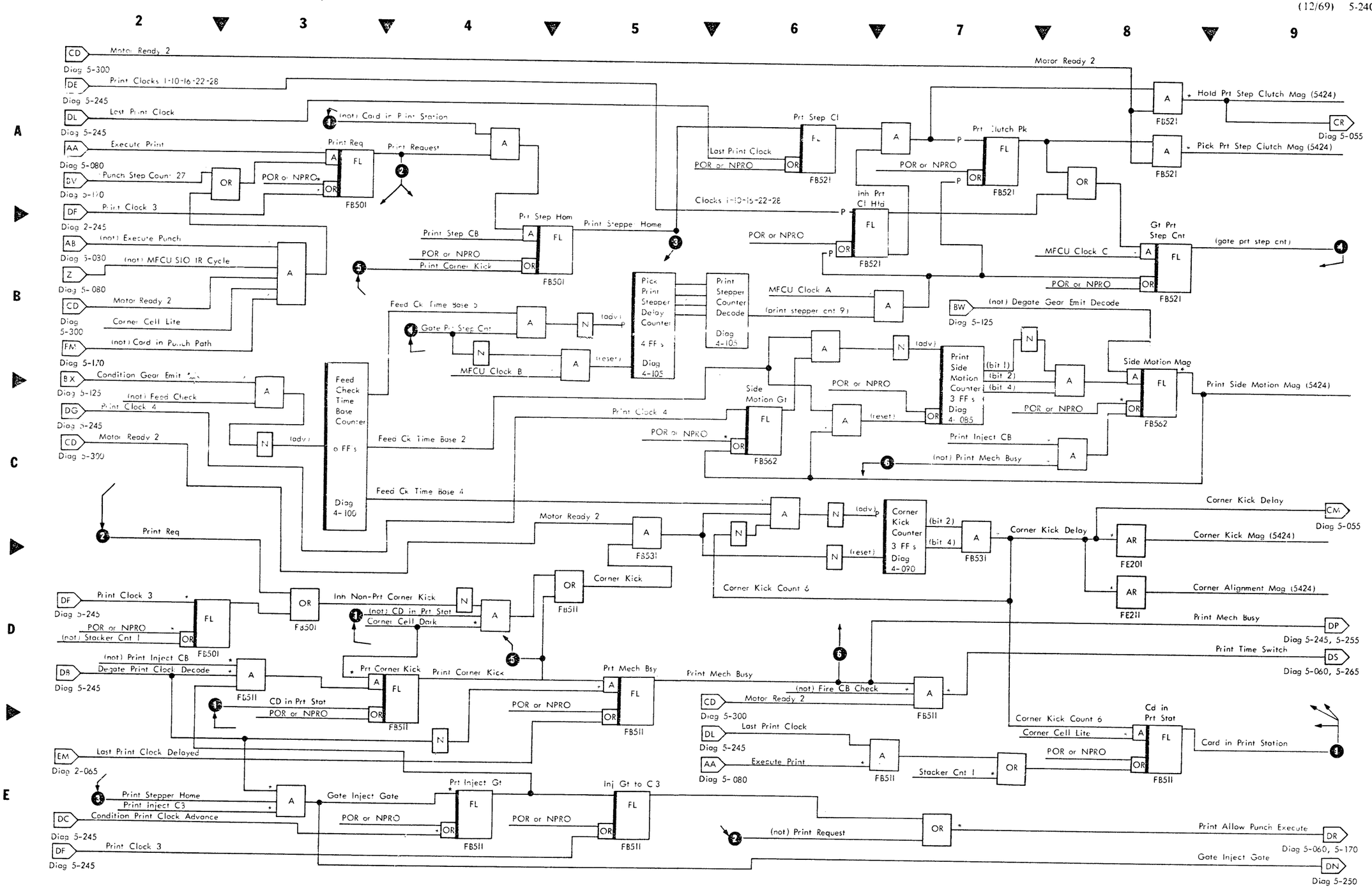


Diagram 5-235. Print/Feed Print Buffer 1 or 2 Busy and Print 4 Lines (Part 8 of 14)

Diagram 5-240. Print/Feed Operation Feed Controls (Part 9 of 14)



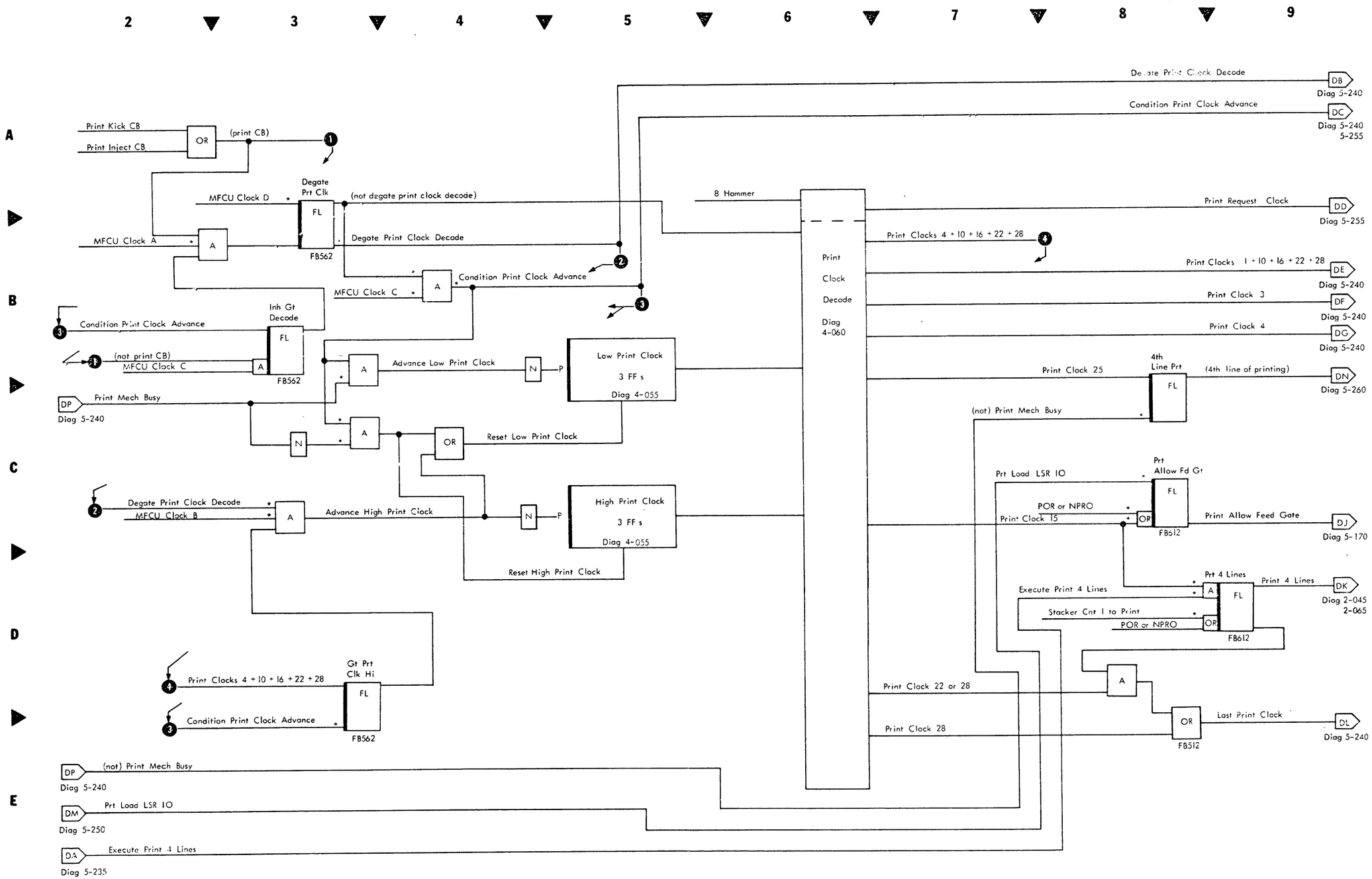
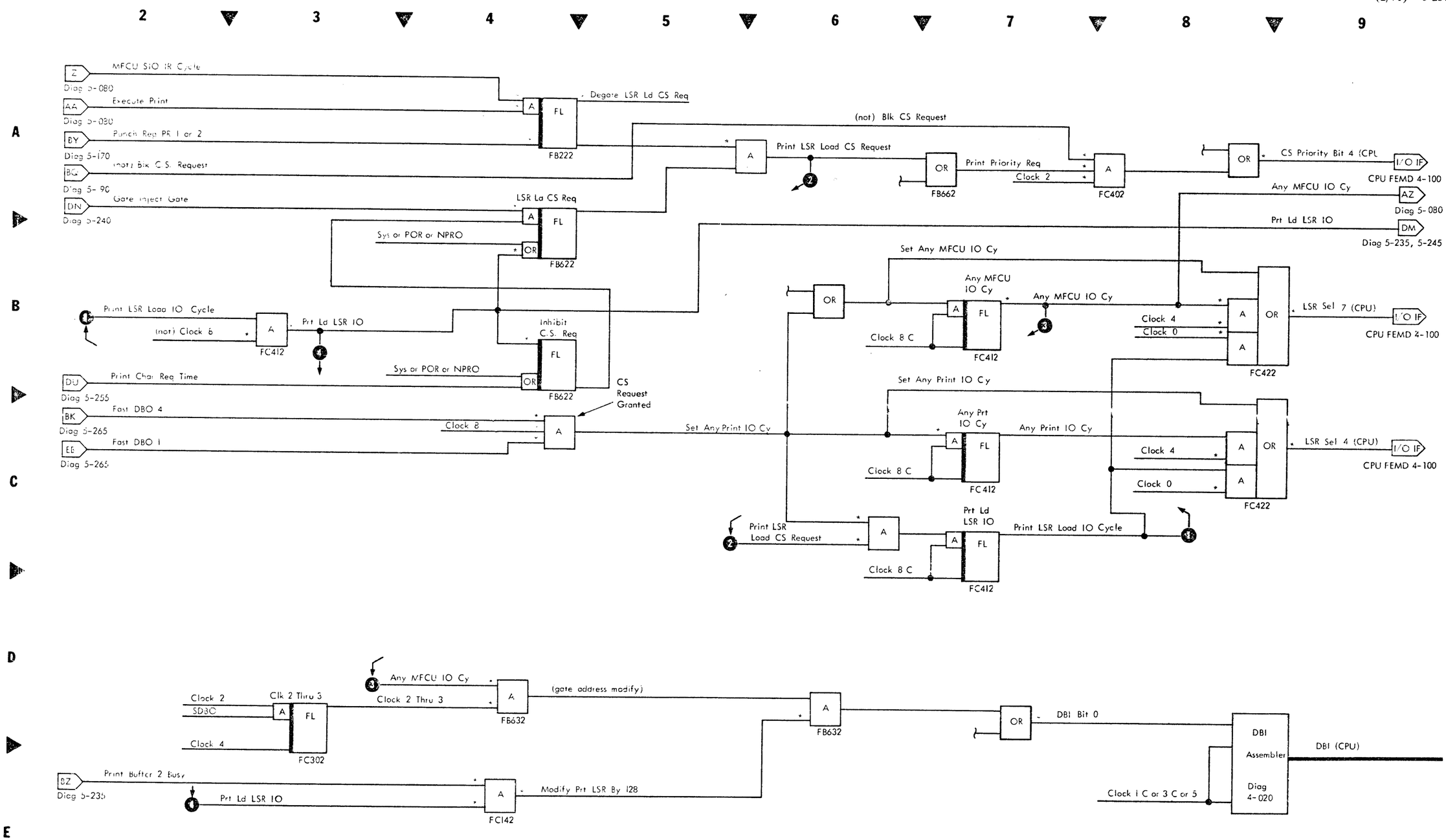


Diagram 5-245. Print/Feed Print Clock and Controls (Part 10 of 14)


2
3
4
5
6
7
8
9
A
B
C
D
E
Z
MFCU SIO IR Cycle
Diag 5-080
AA
Execute Print
Diag 5-080
BY
Punch Req PR 1 or 2
Diag 5-170
BG
(not) Blk C.S. Request
Diag 5-90
DN
Gate Inject Gate
Diag 5-240
A
FL
FB222
Degate LSR Ld CS Req
LSR Ld CS Req
FB622
Sys or POR or NPRO
OR
(not) Blk CS Request
Print LSR Load CS Request
FB662
Print Priority Req
Clock 2
FC402
CS Priority Bit 4 (CPU)
I/O IF
CPU FEMD 4-100
Any MFCU IO Cy
AZ
Diag 5-080
Prt Ld LSR IO
DM
Diag 5-235, 5-245
Print LSR Load IO Cycle
(not) Clock 8
FC412
Prt Ld LSR IO
Inhibit C.S. Req
DU
Print Char Req Time
Diag 5-255
BK
Fast DBO 4
Diag 5-265
EE
Fast DBO 1
Diag 5-265
Clock 8
CS Request Granted
Set Any Print IO Cy
Set Any MFCU IO Cy
Any MFCU IO Cy
Clock 8 C
Clock 4
Clock 0
FC422
LSR Sel 7 (CPU)
Any Prt IO Cy
Any Print IO Cy
LSR Sel 4 (CPU)
Print LSR Load CS Request
Prt Ld LSR IO
Clock 1 C or 3 C or 5
BZ
Print Buffer 2 Busy
Diag 5-235
FC142
Modify Prt LSR By 128
Clock 2
SD3C
Clk 2 Thru 3
FC302
Clock 2 Thru 3
FB632
(gate address modify)
DBI Bit 0
DBI
Assembler
Diag
4-020
DBI (CPU)

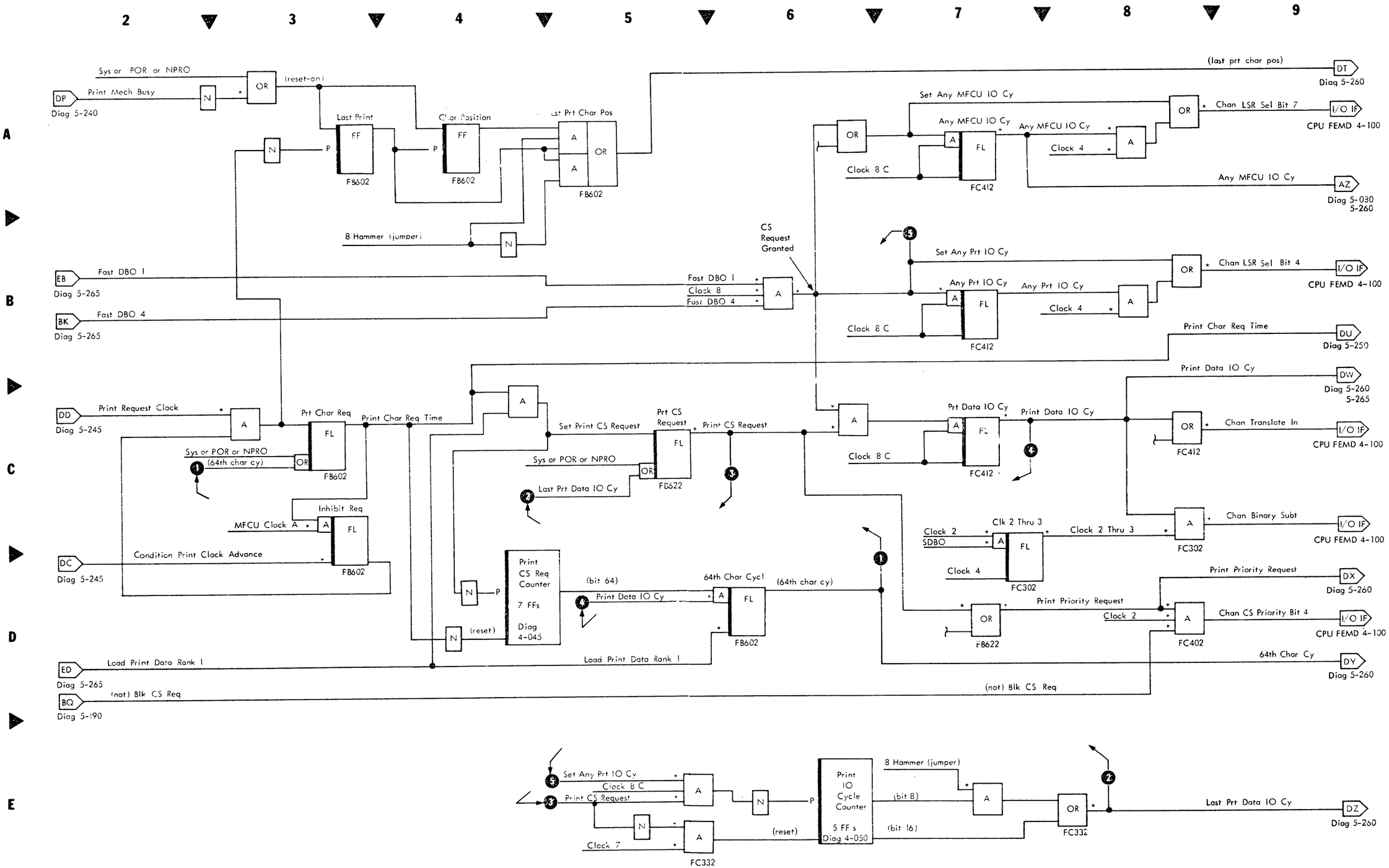
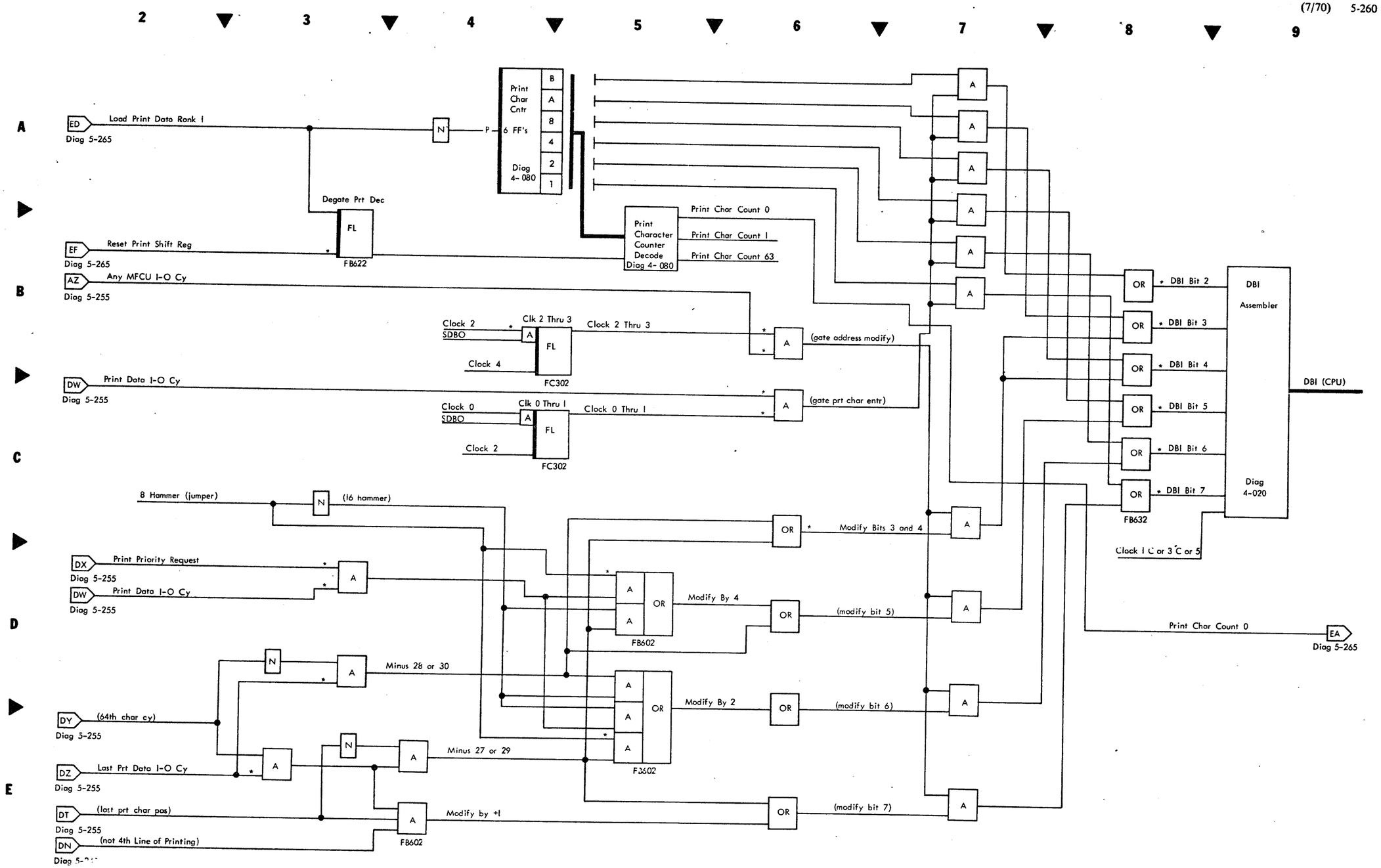


Diagram 5-255. Print/Feed Cycle Steal Channel Controls 1 (Part 12 of 14)

Diagram 5-260. Print/Feed Cycle Steal Channel Controls 2 (Part 13 of 14)



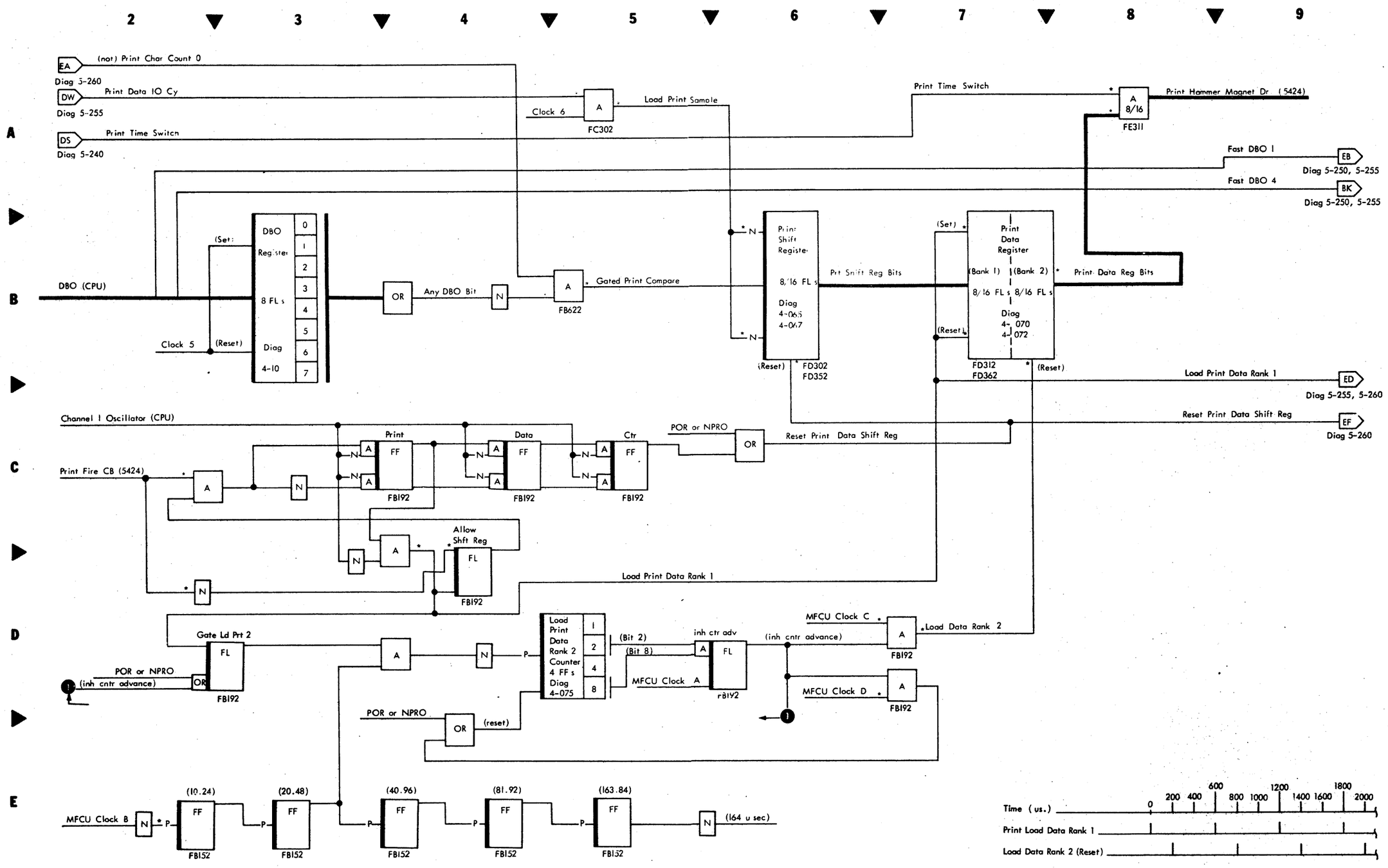
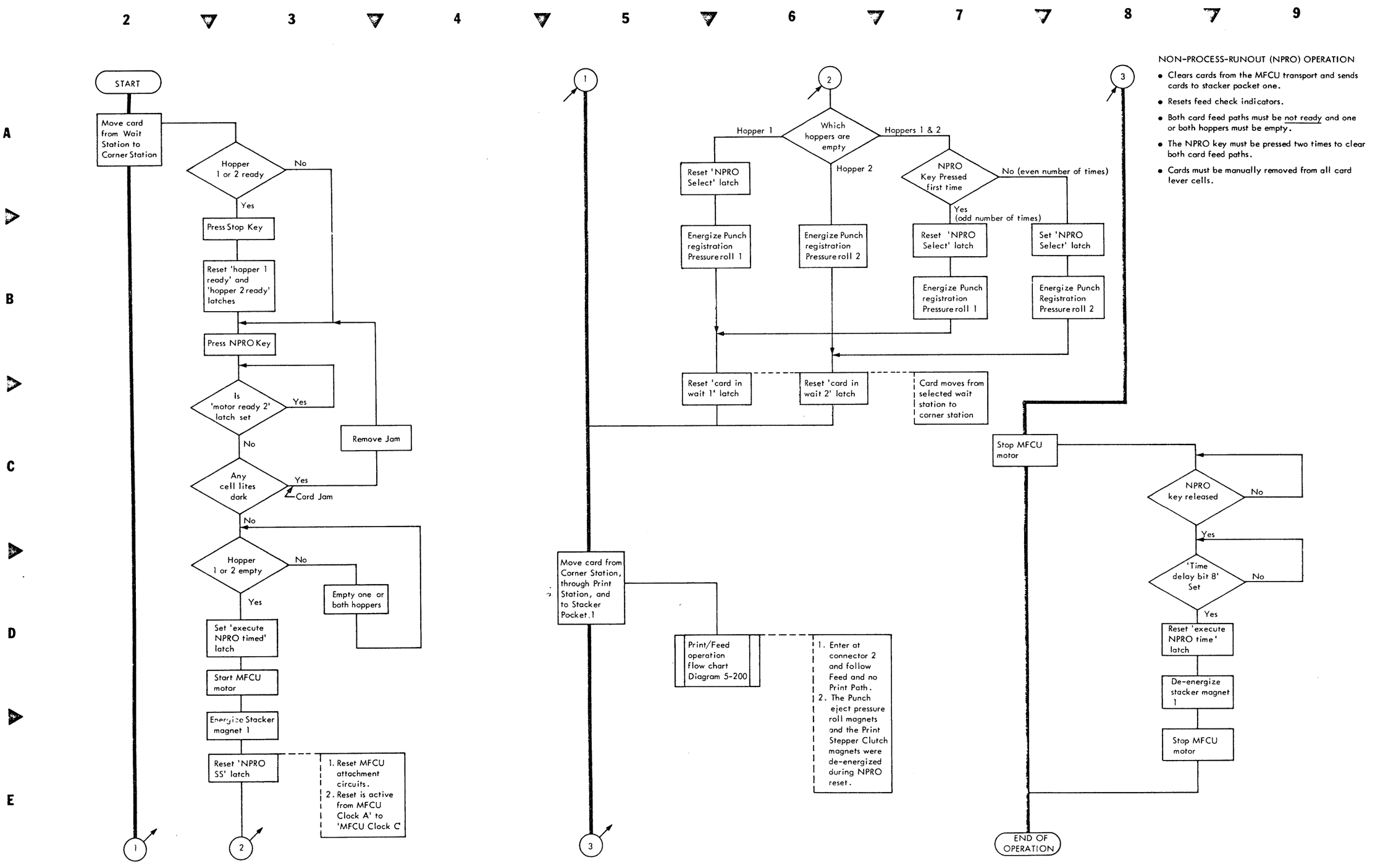


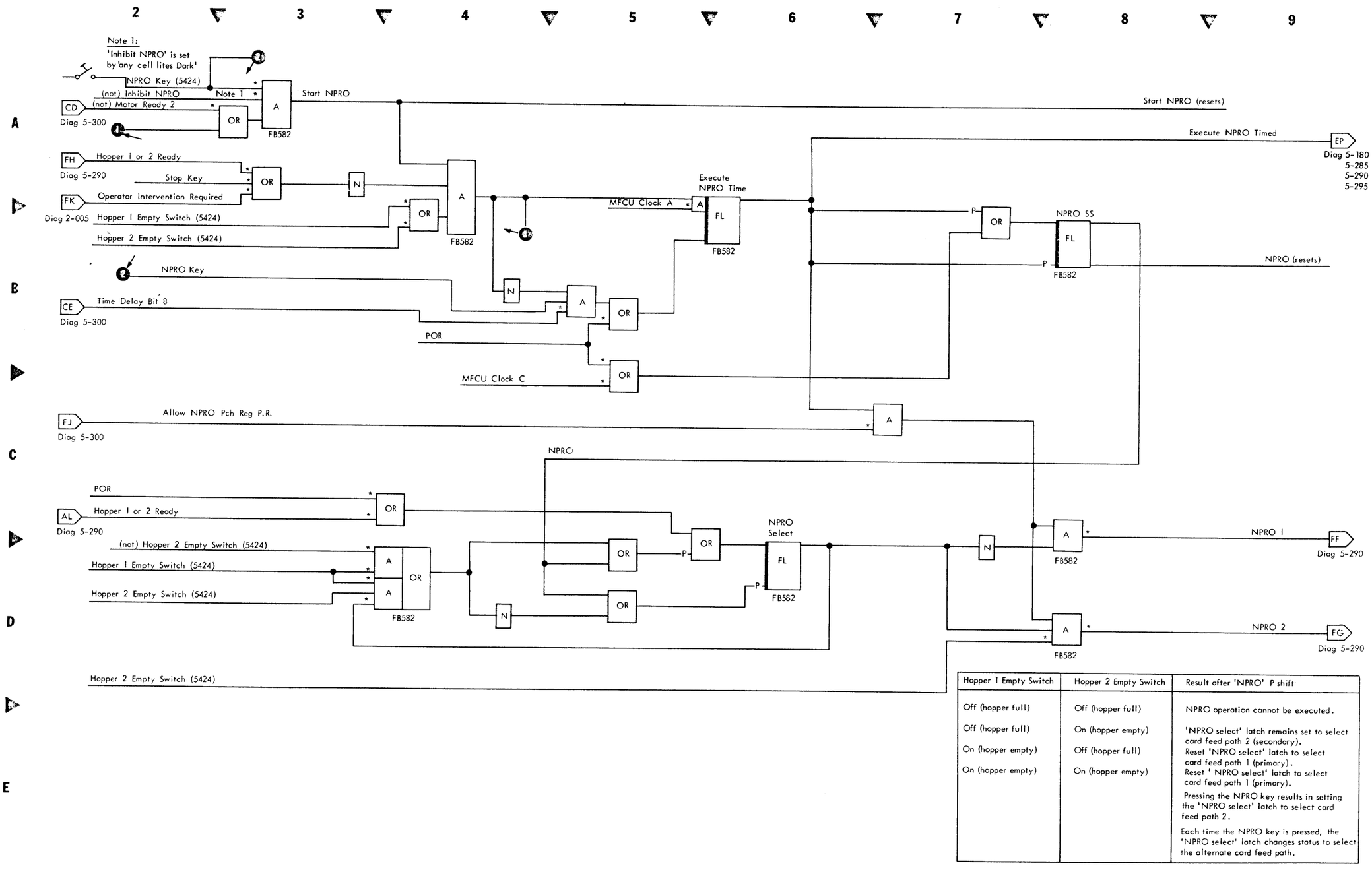
Diagram 5-265. Print/Feed Cycle Steal 5424 Controls (Part 14 of 14)



NON-PROCESS-RUNOUT (NPRO) OPERATION

- Clears cards from the MFCU transport and sends cards to stacker pocket one.
- Resets feed check indicators.
- Both card feed paths must be not ready and one or both hoppers must be empty.
- The NPRO key must be pressed two times to clear both card feed paths.
- Cards must be manually removed from all card lever cells.

Diagram 5-275. NPRO Operation Flowchart (Part 1 of 3)



Hopper 1 Empty Switch	Hopper 2 Empty Switch	Result after 'NPRO' P shift
Off (hopper full)	Off (hopper full)	NPRO operation cannot be executed.
Off (hopper full)	On (hopper empty)	'NPRO select' latch remains set to select card feed path 2 (secondary).
On (hopper empty)	Off (hopper full)	Reset 'NPRO select' latch to select card feed path 1 (primary).
On (hopper empty)	On (hopper empty)	Reset ' NPRO select' latch to select card feed path 1 (primary).
		Pressing the NPRO key results in setting the 'NPRO select' latch to select card feed path 2.
		Each time the NPRO key is pressed, the 'NPRO select' latch changes status to select the alternate card feed path.

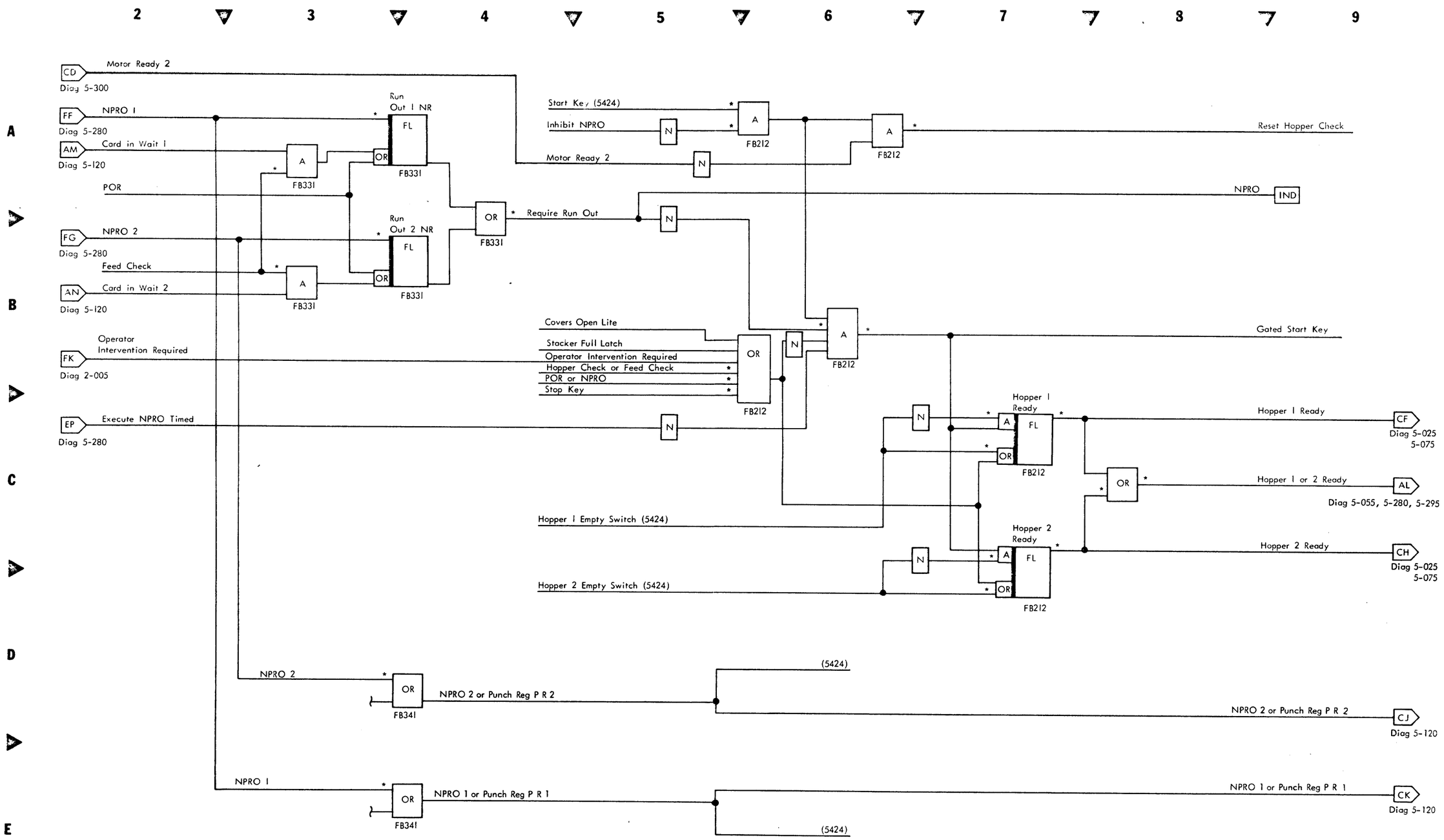
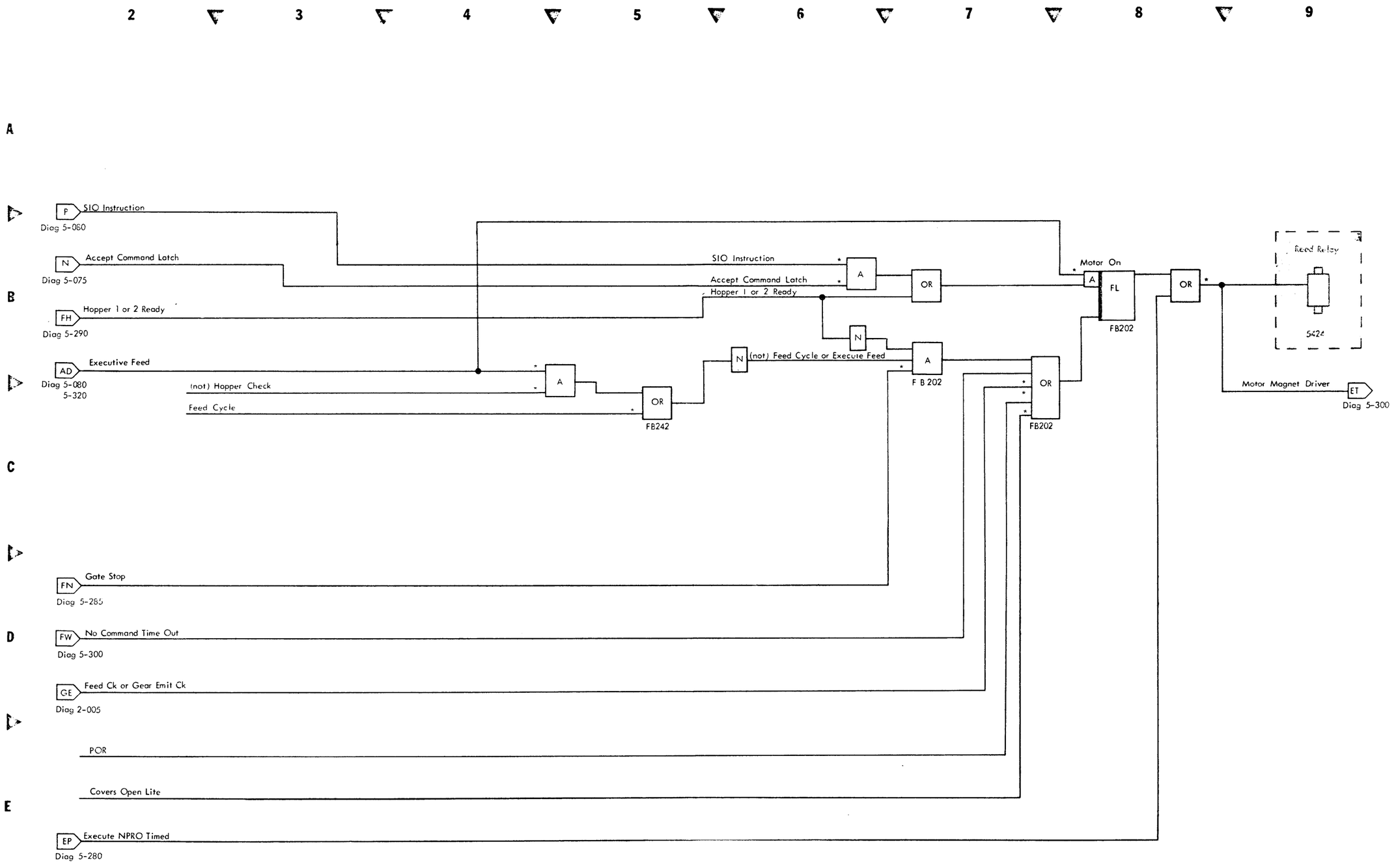


Diagram 5-290. NPRO Card Feed Controls and Hopper Controls (Part 3 of 3)


2
3
4
5
6
7
8
9
A
B
C
D
E
P
SIO Instruction
Diag 5-060
N
Accept Command Latch
Diag 5-075
FH
Hopper 1 or 2 Ready
Diag 5-290
AD
Executive Feed
Diag 5-080
5-320
(not) Hopper Check
Feed Cycle
A
OR
FB242
N
(not) Feed Cycle or Execute Feed
A
F B 202
SIO Instruction
Accept Command Latch
Hopper 1 or 2 Ready
A
OR
N
OR
FB202
Motor On
A
FL
FB202
OR
Reed Relay
5424
Motor Magnet Driver
ET
Diag 5-300
FN
Gate Stop
Diag 5-285
FW
No Command Time Out
Diag 5-300
GE
Feed Ck or Gear Emit Ck
Diag 2-005
POR
Covers Open Lite
EP
Execute NPRO Timed
Diag 5-280

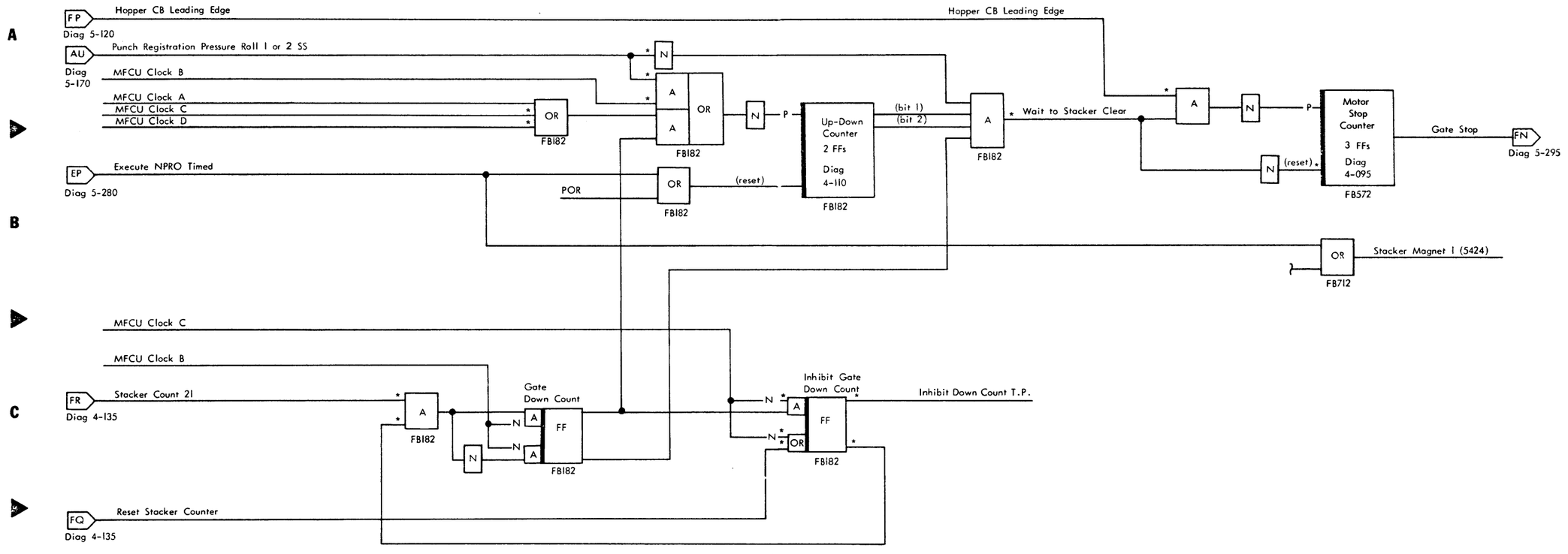
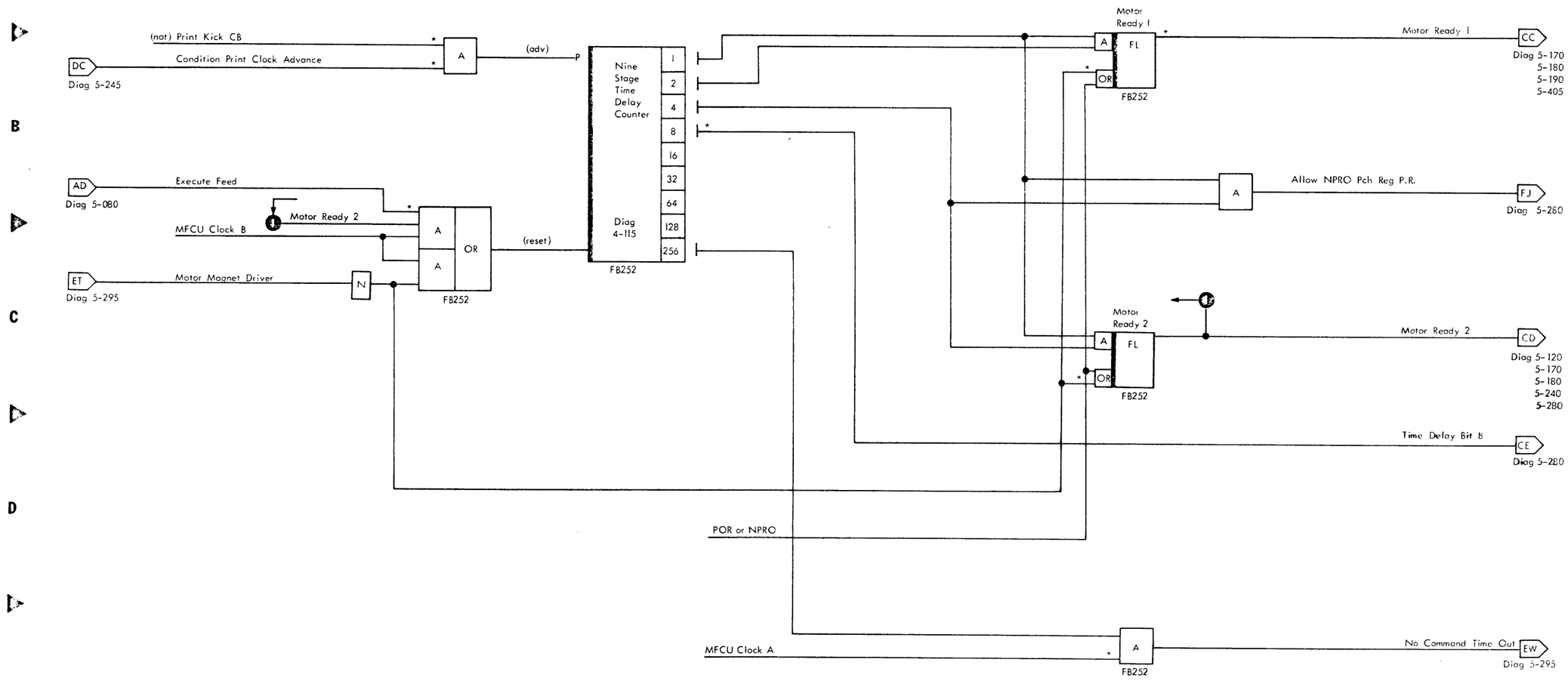
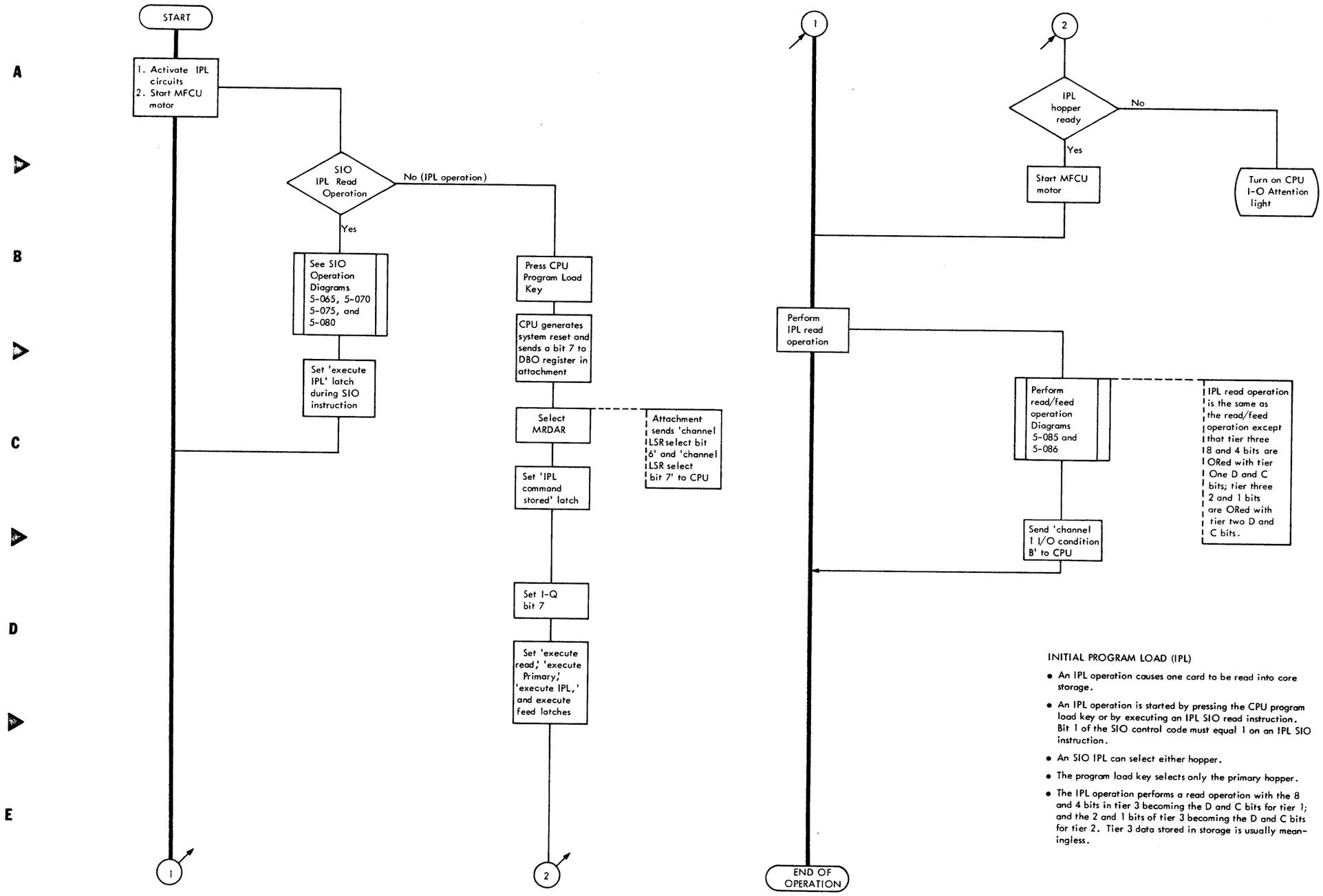


Diagram 5-297. Motor Controls (Part 2 of 3)

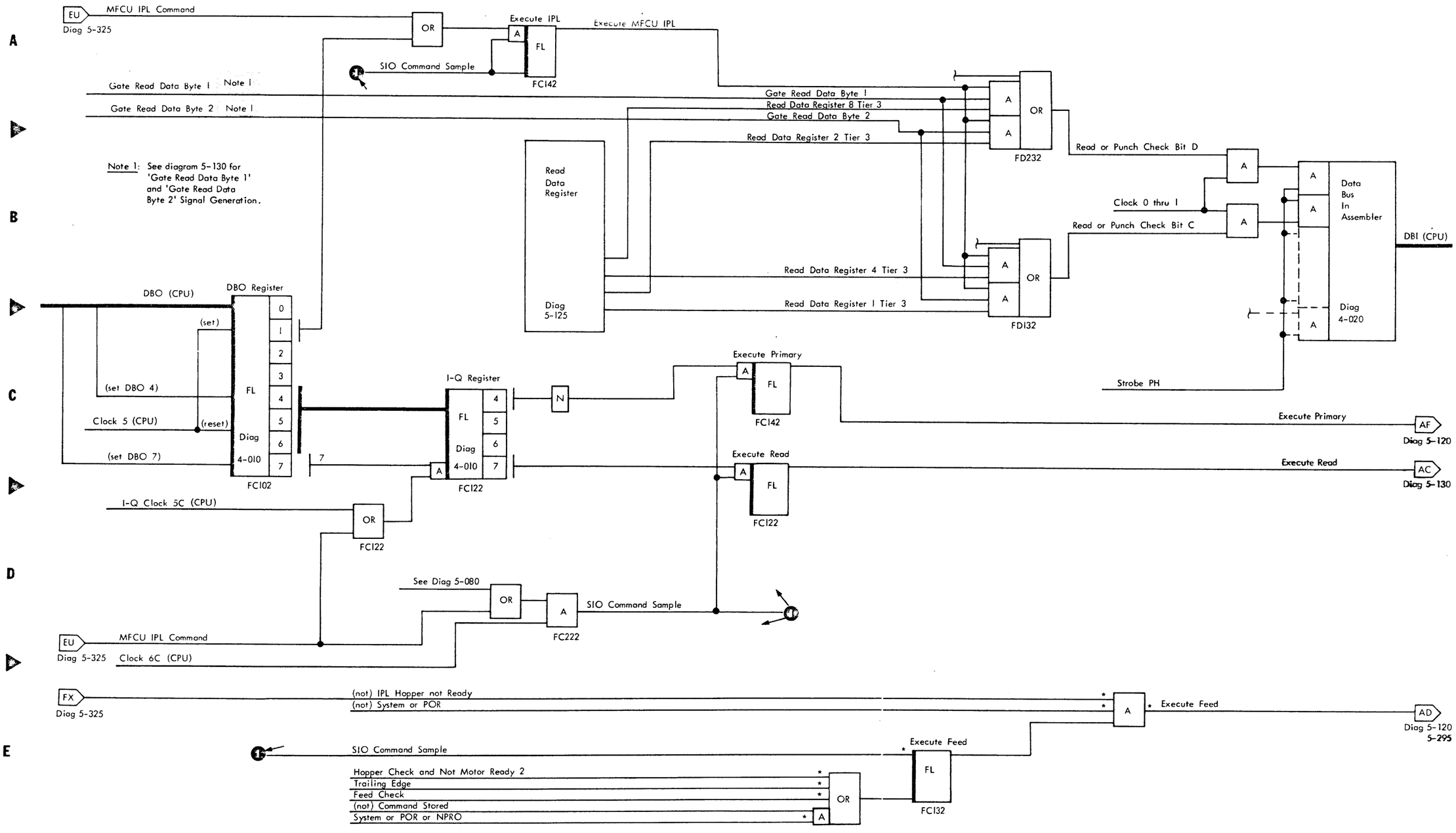

2
3
4
5
6
7
8
9
A
B
C
D
E
(not) Print Kick CB
Condition Print Clock Advance
DC
Diag 5-245
A
(adv)
P
Nine Stage Time Delay Counter
1
2
4
8
16
32
64
128
256
Diag 4-115
FB252
Motor Ready 1
A
FL
OR
FB252
Motor Ready 1
CC
Diag 5-170
5-180
5-190
5-405
AD
Execute Feed
Diag 5-080
Motor Ready 2
MFCU Clock B
A
A
OR
(reset)
FB252
A
Allow NPRO Pch Reg P.R.
FJ
Diag 5-280
ET
Motor Magnet Driver
Diag 5-295
N
FB252
Motor Ready 2
A
FL
OR
FB252
Motor Ready 2
CD
Diag 5-120
5-170
5-180
5-240
5-280
Time Delay Bit 8
CE
Diag 5-280
POR or NPRO
MFCU Clock A
A
FB252
No Command Time Out
EW
Diag 5-295



INITIAL PROGRAM LOAD (IPL)

- An IPL operation causes one card to be read into core storage.
- An IPL operation is started by pressing the CPU program load key or by executing an IPL SIO read instruction. Bit 1 of the SIO control code must equal 1 on an IPL SIO instruction.
- An SIO IPL can select either hopper.
- The program load key selects only the primary hopper.
- The IPL operation performs a read operation with the 8 and 4 bits in tier 3 becoming the D and C bits for tier 1; and the 2 and 1 bits of tier 3 becoming the D and C bits for tier 2. Tier 3 data stored in storage is usually meaningless.

Diagram 5-315. IPL Operation Flowchart (Part 1 of 3)


2
3
4
5
6
7
8
9
A
B
C
D
E
EU
MFCU IPL Command
Diag 5-325
OR
Execute IPL
A
FL
FC142
Execute MFCU IPL
SIO Command Sample
Gate Read Data Byte 1 Note 1
Gate Read Data Byte 2 Note 1
Note 1: See diagram 5-130 for 'Gate Read Data Byte 1' and 'Gate Read Data Byte 2' Signal Generation.
Read Data Register
Diag 5-125
Gate Read Data Byte 1
Read Data Register 8 Tier 3
Gate Read Data Byte 2
Read Data Register 2 Tier 3
Read Data Register 4 Tier 3
Read Data Register 1 Tier 3
FD232
FD132
Read or Punch Check Bit D
Clock 0 thru 1
Read or Punch Check Bit C
Data Bus In Assembler
Diag 4-020
DBI (CPU)
Strobe PH
DBO (CPU)
DBO Register
(set)
(set DBO 4)
Clock 5 (CPU)
(reset)
(set DBO 7)
FL
Diag 4-010
FC102
I-Q Register
FC122
N
7
I-Q Clock 5C (CPU)
Execute Primary
FC142
Execute Read
FC122
AF
Diag 5-120
AC
Diag 5-130
See Diag 5-080
FC222
MFCU IPL Command
Clock 6C (CPU)
FX
(not) IPL Hopper not Ready
(not) System or POR
Execute Feed
AD
Diag 5-120
5-295
SIO Command Sample
Hopper Check and Not Motor Ready 2
Trailing Edge
Feed Check
(not) Command Stored
System or POR or NPRO
FC132

2 3 4 5 6 7 8 9

A

B

C

D

E

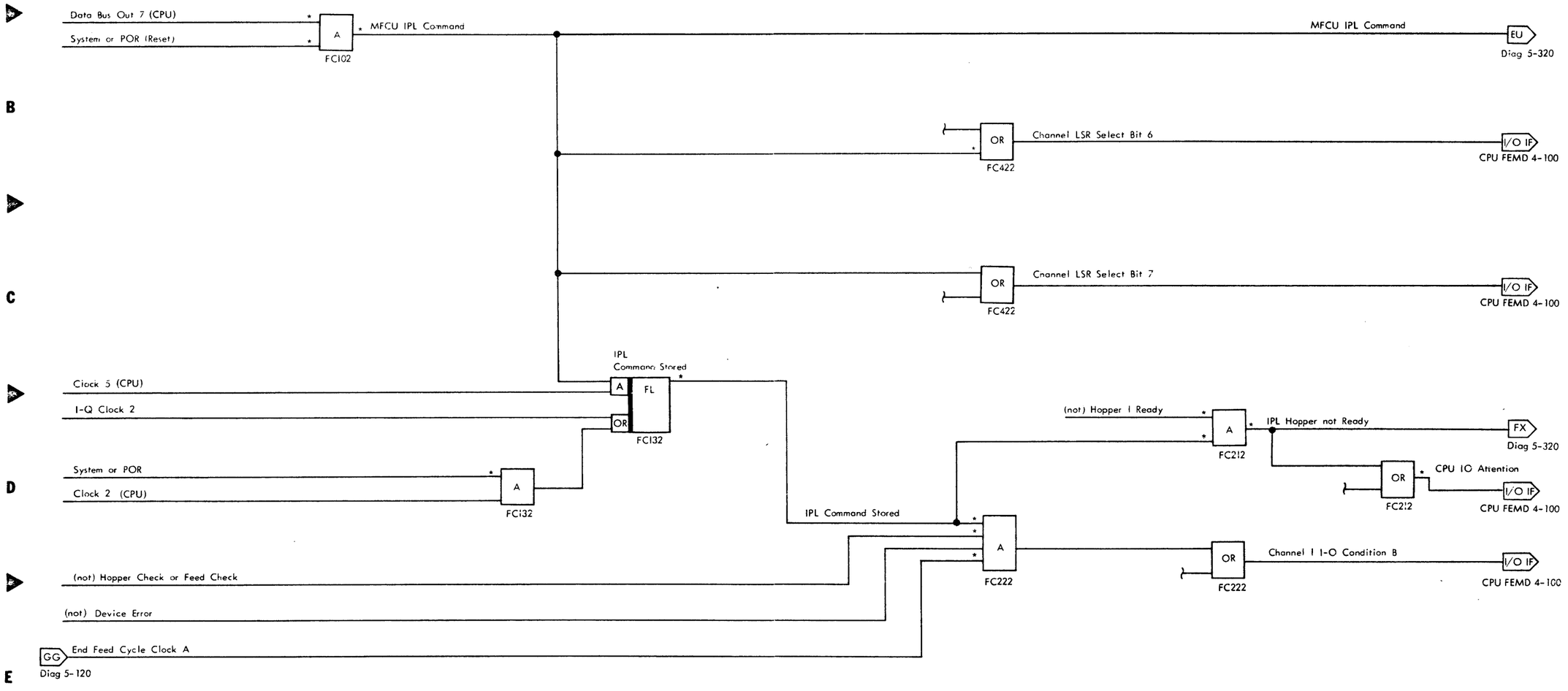
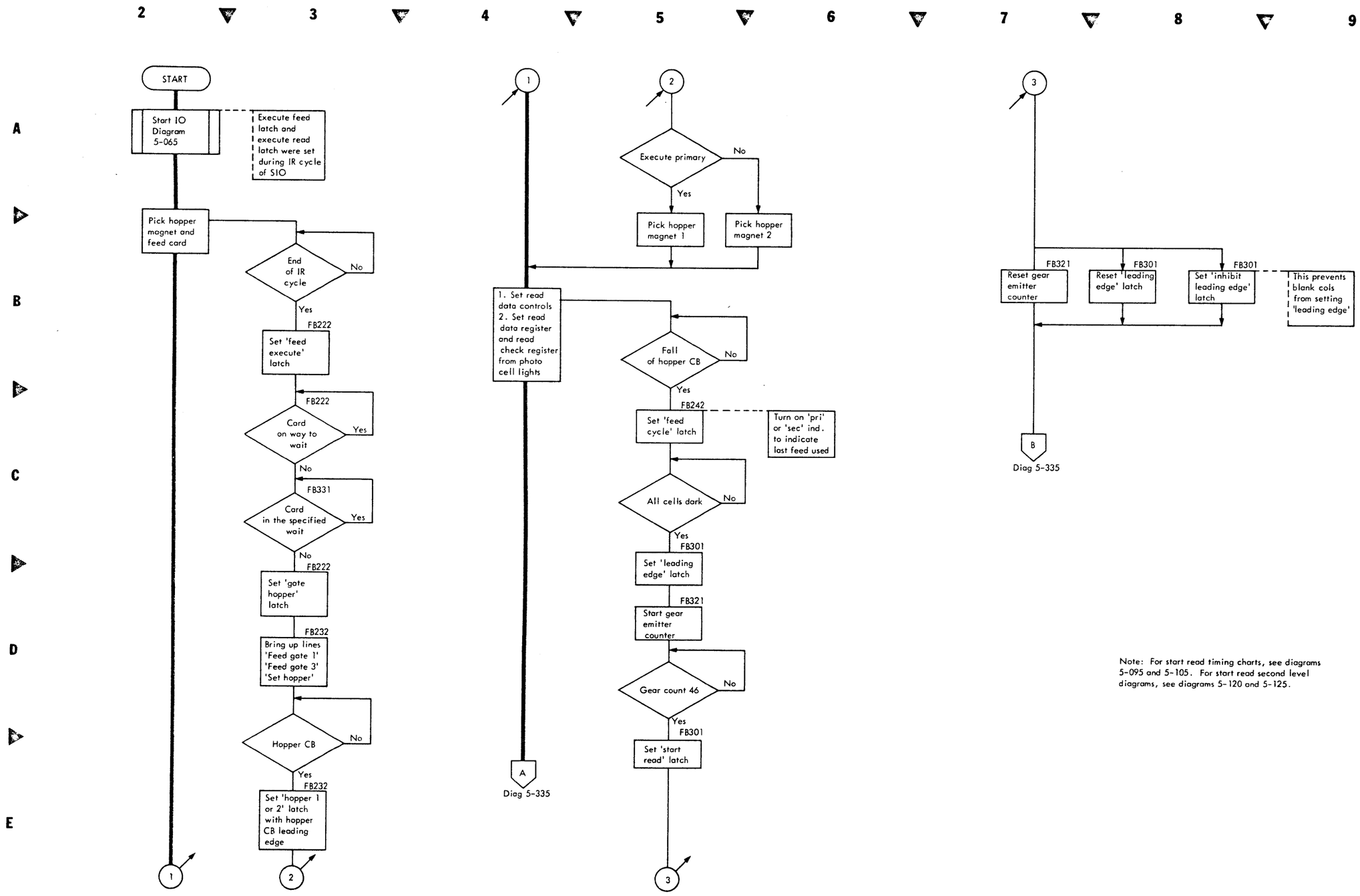
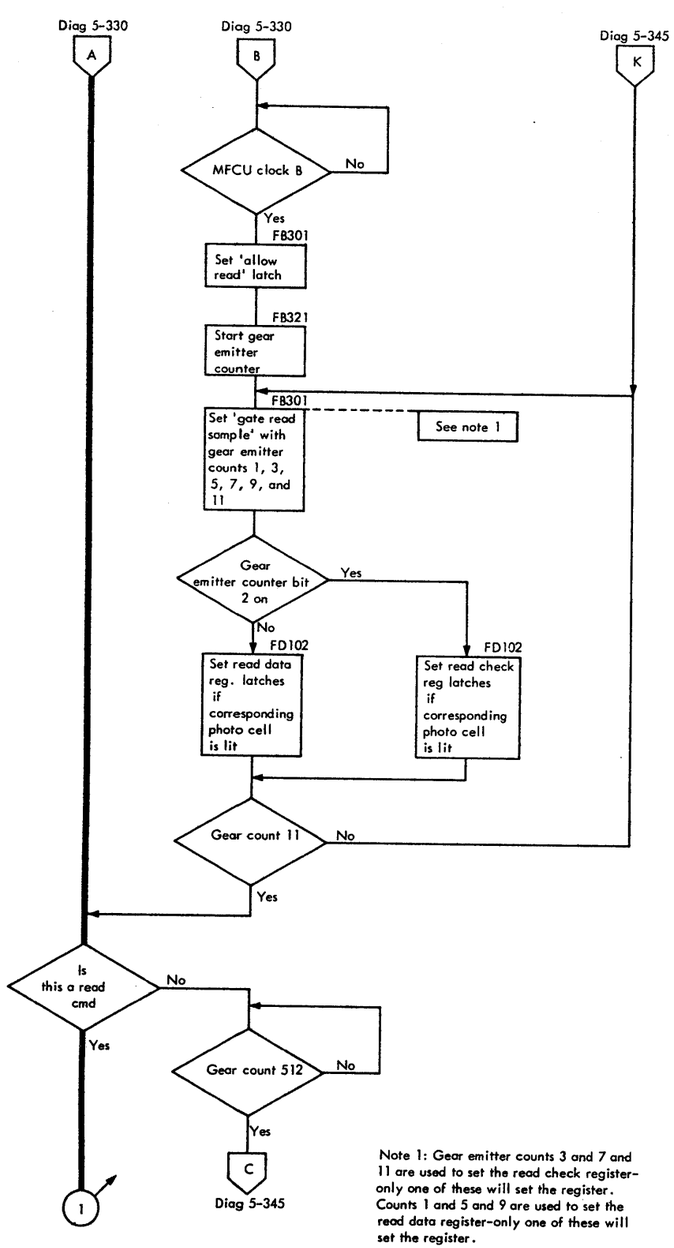


Diagram 5-325. Program Load Key IPL Operation (Part 3 of 3)



Note: For start read timing charts, see diagrams 5-095 and 5-105. For start read second level diagrams, see diagrams 5-120 and 5-125.



Note 1: Gear emitter counts 3 and 7 and 11 are used to set the read check register-only one of these will set the register. Counts 1 and 5 and 9 are used to set the read data register-only one of these will set the register.

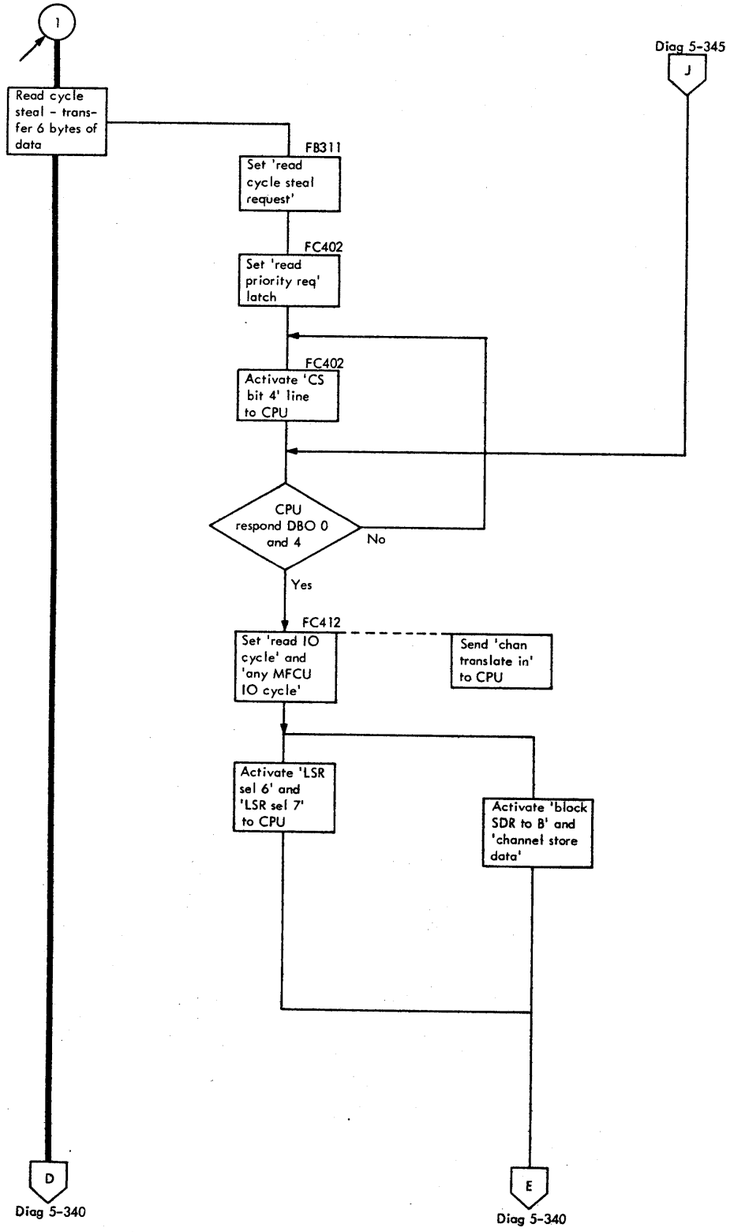
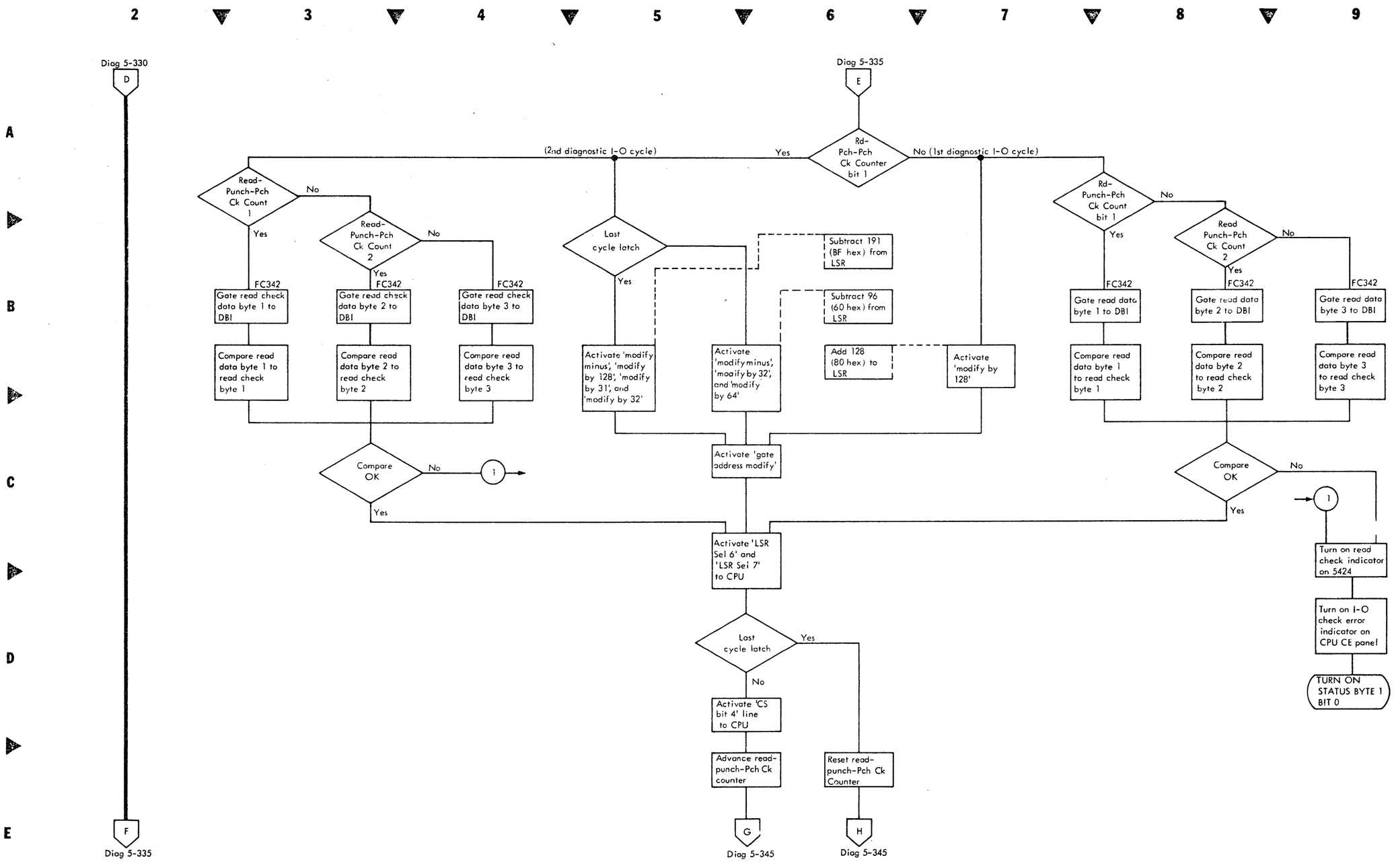


Diagram 5-335. Diagnostic Read/Feed Operation Flowchart (Part 2 of 9)


2
3
4
5
6
7
8
9
A
B
C
D
E
Diag 5-330
D
Diag 5-335
E
Rd-Pch-Pch Ck Counter bit 1
Yes
No (1st diagnostic I-O cycle)
(2nd diagnostic I-O cycle)
Read-Punch-Pch Ck Count 1
No
Yes
Read-Punch-Pch Ck Count 2
No
Yes
FC342
Gate read check data byte 1 to DBI
Gate read check data byte 2 to DBI
Gate read check data byte 3 to DBI
Compare read data byte 1 to read check byte 1
Compare read data byte 2 to read check byte 2
Compare read data byte 3 to read check byte 3
Compare OK
No
1
Yes
Last cycle latch
Yes
Activate 'modify minus', 'modify by 128', 'modify by 31', and 'modify by 32'
Activate 'modify minus', 'modify by 32', and 'modify by 64'
Subtract 191 (BF hex) from LSR
Subtract 96 (60 hex) from LSR
Add 128 (80 hex) to LSR
Activate 'modify by 128'
Activate 'gate address modify'
Activate 'LSR Sel 6' and 'LSR Sel 7' to CPU
Last cycle latch
Yes
No
Activate 'CS bit 4' line to CPU
Advance read-punch-Pch Ck counter
Reset read-punch-Pch Ck Counter
G
H
Diag 5-345
Diag 5-345
Rd-Punch-Pch Ck Count bit 1
No
Yes
Read Punch-Pch Ck Count 2
No
Yes
FC342
Gate read data byte 1 to DBI
Gate read data byte 2 to DBI
Gate read data byte 3 to DBI
Compare read data byte 1 to read check byte 1
Compare read data byte 2 to read check byte 2
Compare read data byte 3 to read check byte 3
Compare OK
No
Yes
1
Turn on read check indicator on 5424
Turn on I-O check error indicator on CPU CE panel
TURN ON STATUS BYTE 1 BIT 0
F
Diag 5-335

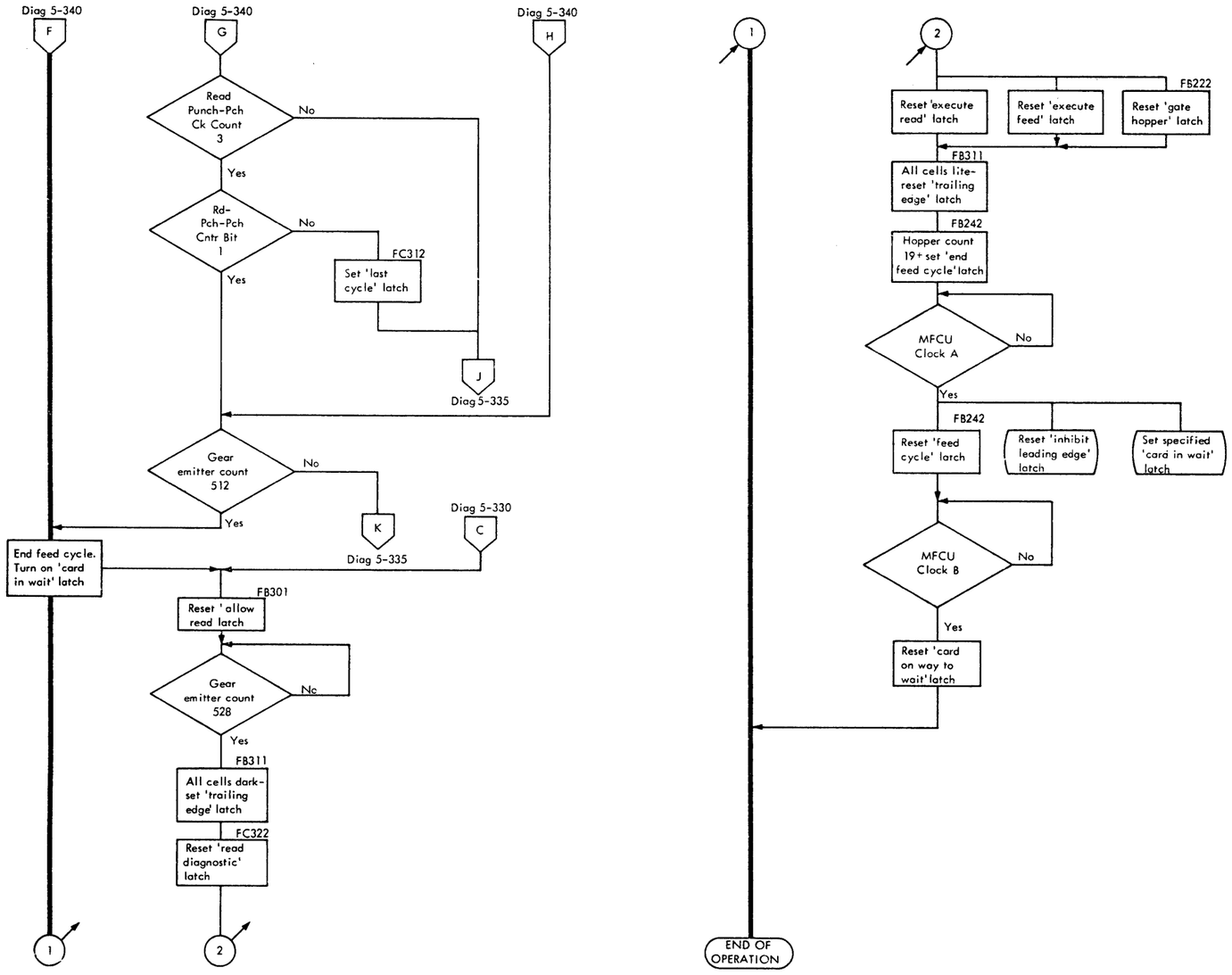
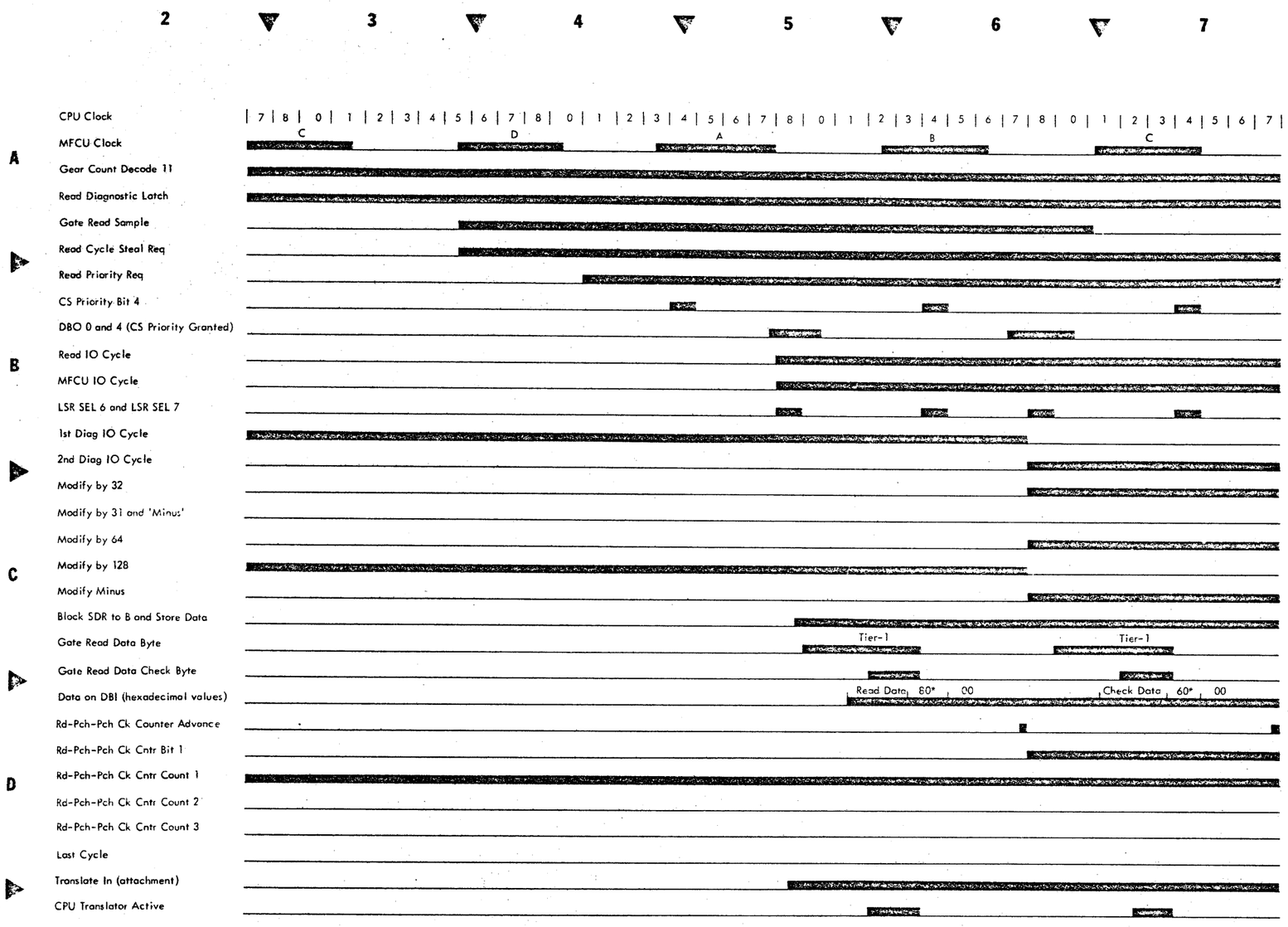
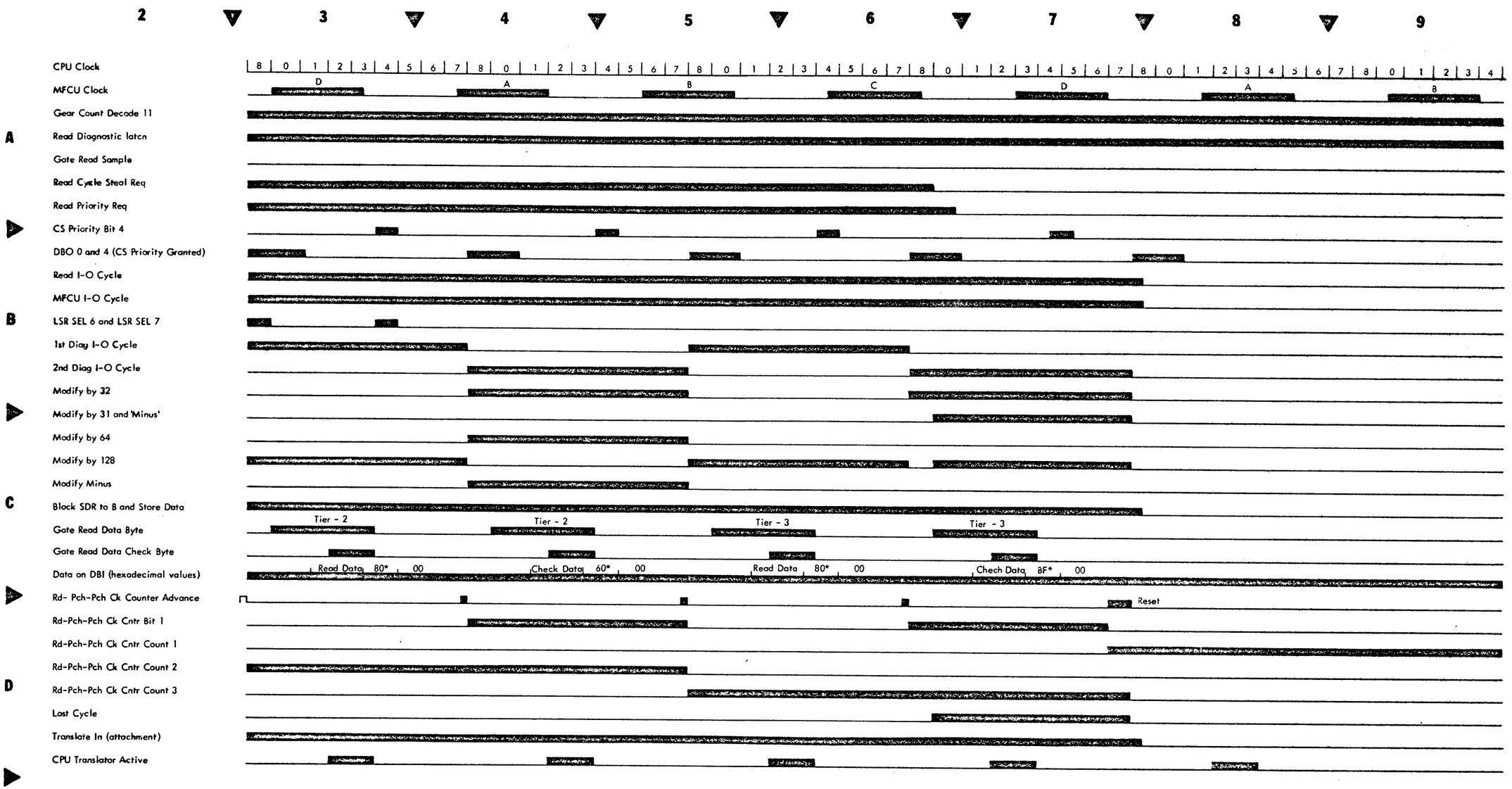


Diagram 5-345. Diagnostic Read/Feed Operation Flowchart (Part 4 of 9)



Timing chart continued on Diagram 5-355

Note: * Hexadecimal Value for LSR Address Modification
a. 60 Hex = 96 Decimal
b. 80 Hex = 128 Decimal
c. BF Hex = 191 Decimal



Notes:
* Hexadecimal Value for LSR Address Modification

a. 60 Hex = 96 Decimal
b. 80 Hex = 128 Decimal
c. BF Hex = 191 Decimal

Diagram 5-355. Diagnostic Read Cycle Steal Request Timing Chart (Part 6 of 9)

2 3 4 5 6 7 8 9

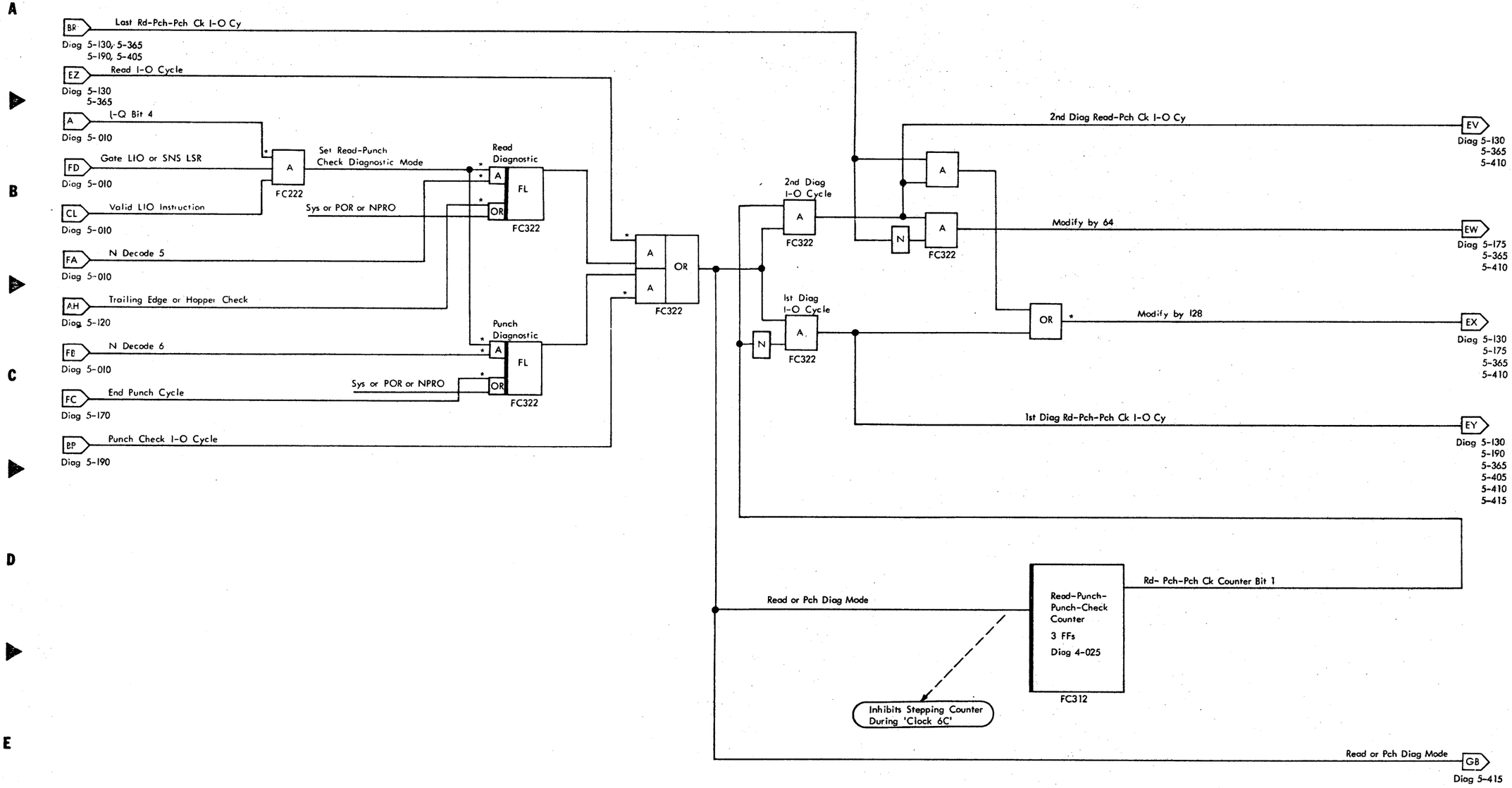
A

B

C

D

E



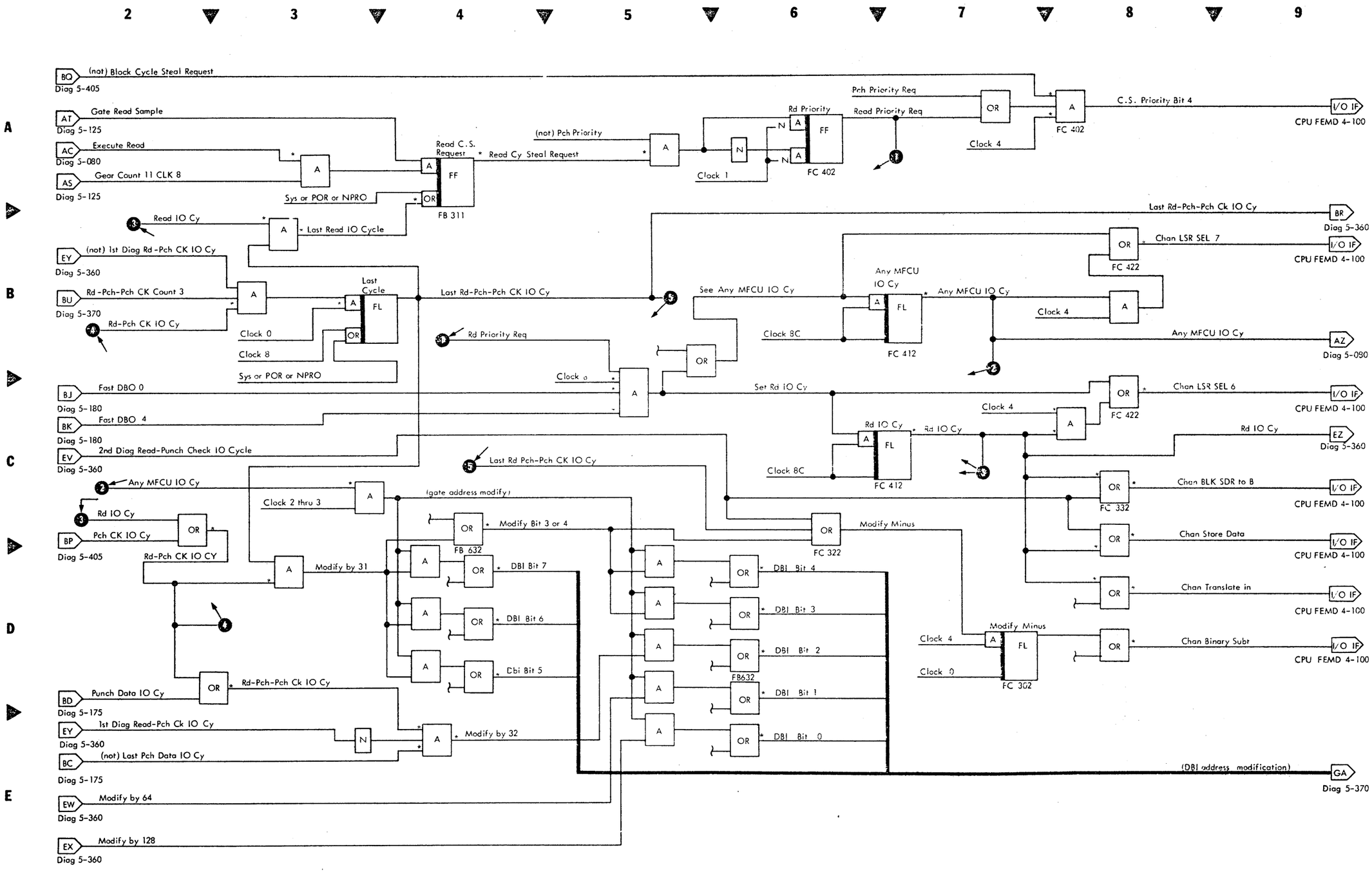


Diagram 5-365. Diagnostic Read Cycle Steal Request (Part 8 of 9)

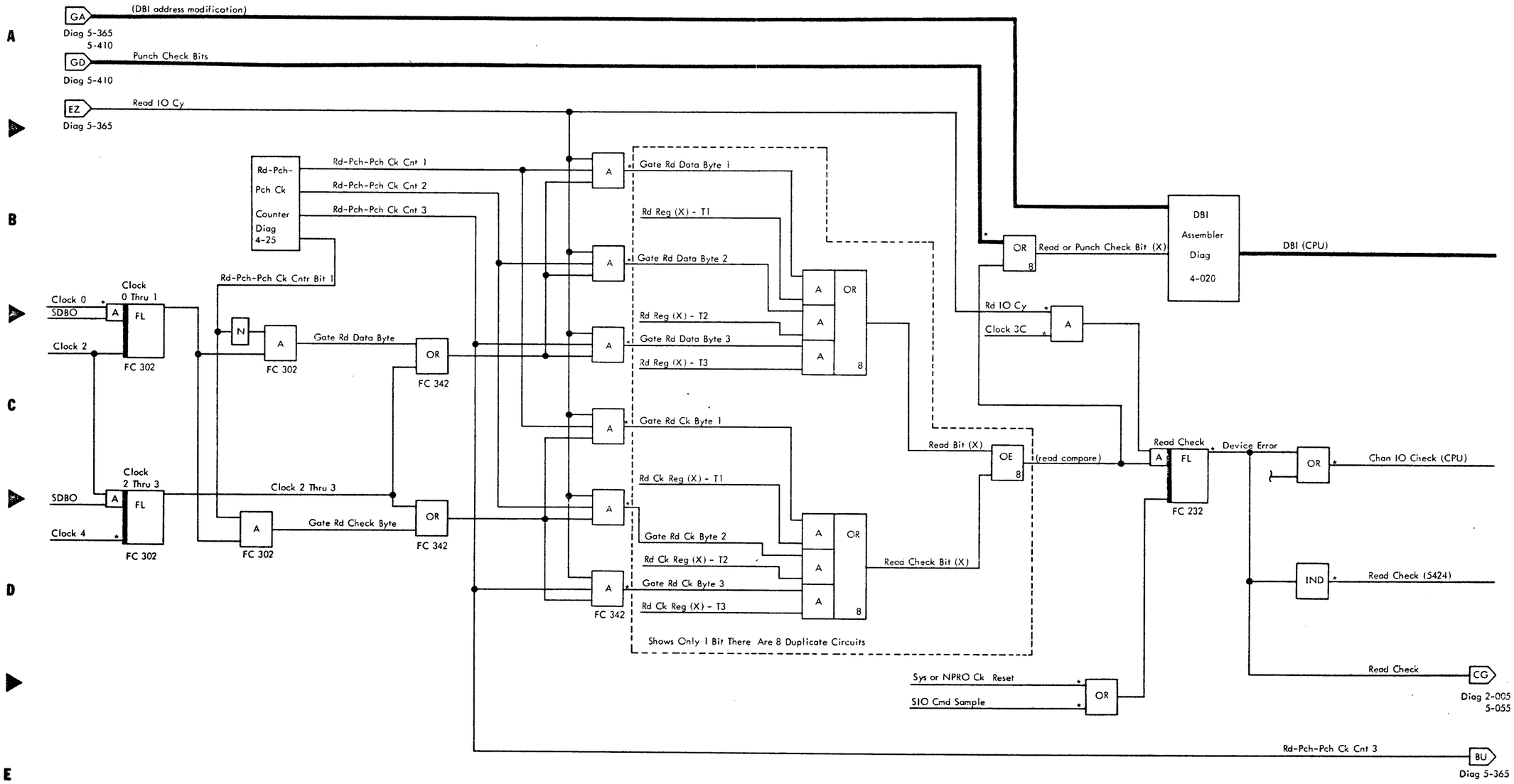
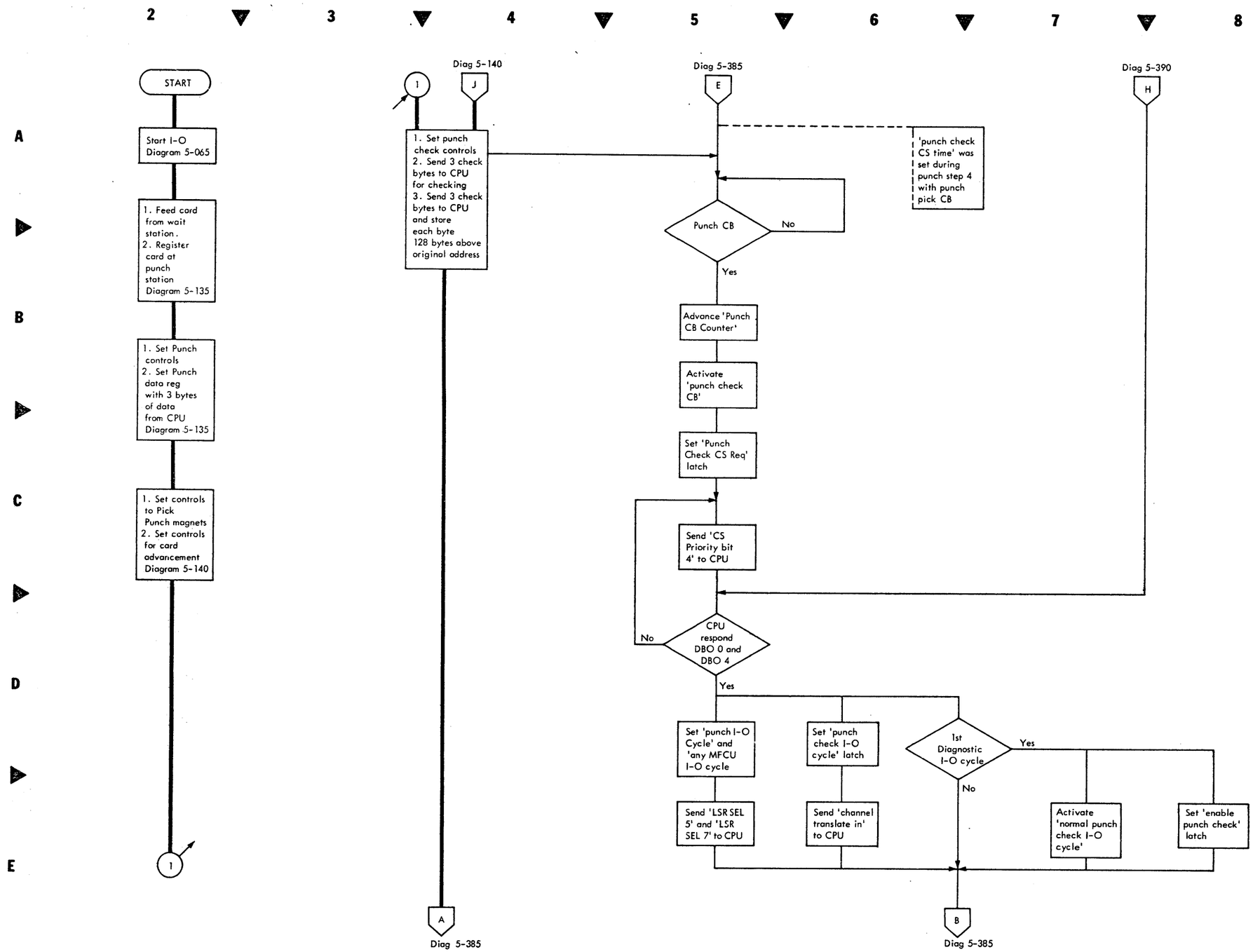
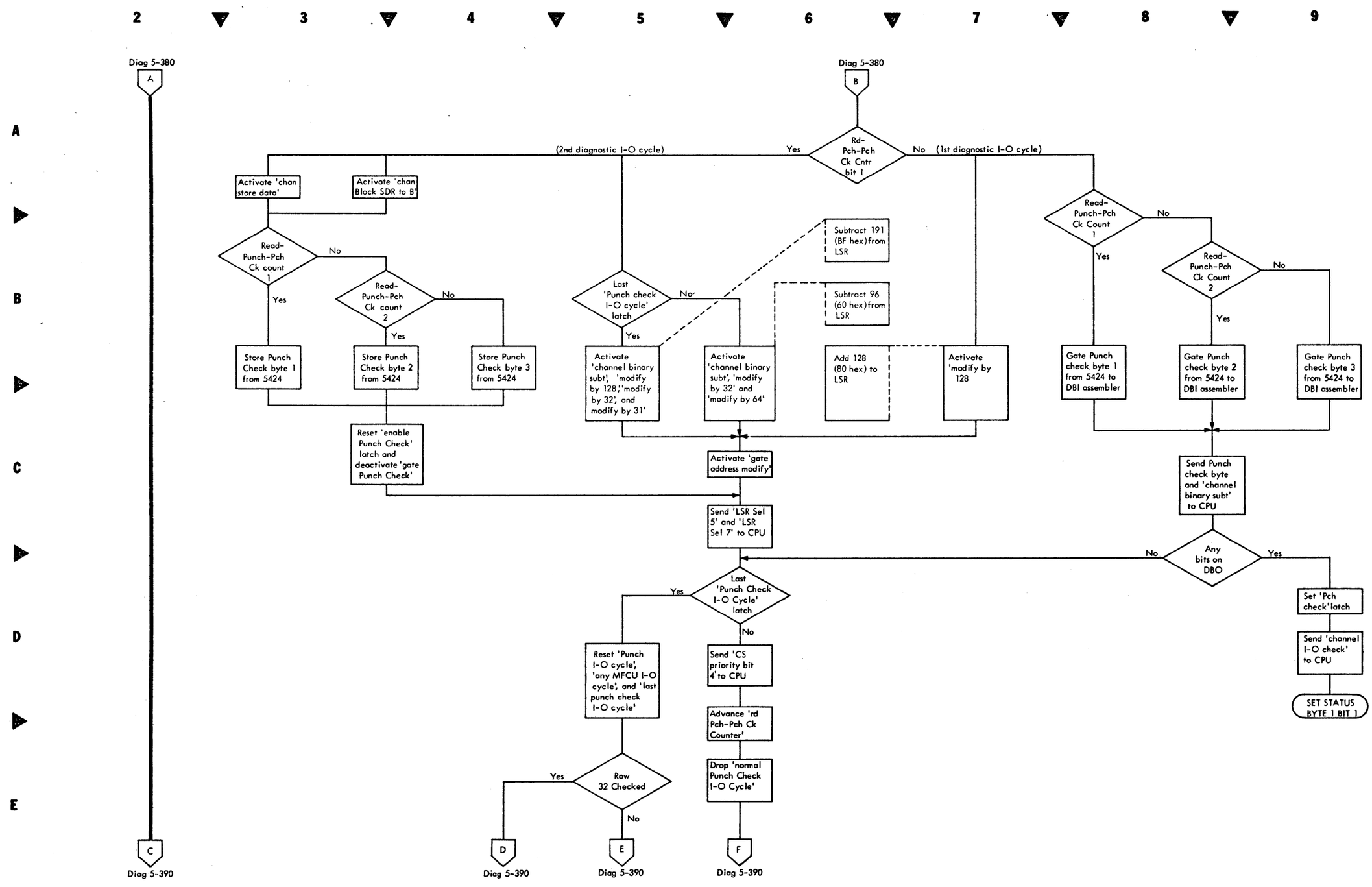


Diagram 5-370. Diagnostic Read-Punch Data Transfer (Part 9 of 9)


2
3
4
5
6
7
8
9
A
B
C
D
E
START
Start I-O Diagram 5-065
1. Feed card from wait station.
2. Register card at punch station
Diagram 5-135
1. Set Punch controls
2. Set Punch data reg with 3 bytes of data from CPU
Diagram 5-135
1. Set controls to Pick Punch magnets
2. Set controls for card advancement
Diagram 5-140
1
Diag 5-140
J
1. Set punch check controls
2. Send 3 check bytes to CPU for checking
3. Send 3 check bytes to CPU and store each byte 128 bytes above original address
A
Diag 5-385
Diag 5-385
E
'punch check CS time' was set during punch step 4 with punch pick CB
Punch CB
No
Yes
Advance 'Punch CB Counter'
Activate 'punch check CB'
Set 'Punch Check CS Req' latch
Send 'CS Priority bit 4' to CPU
CPU respond DBO 0 and DBO 4
No
Yes
Set 'punch I-O Cycle' and 'any MFCU I-O cycle
Set 'punch check I-O cycle' latch
1st Diagnostic I-O cycle
Yes
No
Send 'LSR SEL 5' and 'LSR SEL 7' to CPU
Send 'channel translate in' to CPU
Activate 'normal punch check I-O cycle'
Set 'enable punch check' latch
B
Diag 5-385
Diag 5-390
H


2
3
4
5
6
7
8
9
A
B
C
D
E
Diag 5-380
A
Diag 5-380
B
Rd-Pch-Pch Ck Cntr bit 1
Yes
No
(2nd diagnostic I-O cycle)
(1st diagnostic I-O cycle)
Activate 'chan store data'
Activate 'chan Block SDR to B'
Read-Punch-Pch Ck count 1
Read-Punch-Pch Ck count 2
Store Punch Check byte 1 from 5424
Store Punch Check byte 2 from 5424
Store Punch Check byte 3 from 5424
Reset 'enable Punch Check' latch and deactivate 'gate Punch Check'
Last 'Punch check I-O cycle' latch
Subtract 191 (BF hex) from LSR
Subtract 96 (60 hex) from LSR
Add 128 (80 hex) to LSR
Activate 'channel binary subt', 'modify by 128,''modify by 32', and modify by 31'
Activate 'channel binary subt', 'modify by 32' and 'modify by 64'
Activate 'modify by 128
Activate 'gate address modify'
Send 'LSR Sel 5' and 'LSR Sel 7' to CPU
Read-Punch-Pch Ck Count 1
Read-Punch-Pch Ck Count 2
Gate Punch check byte 1 from 5424 to DBI assembler
Gate Punch check byte 2 from 5424 to DBI assembler
Gate Punch check byte 3 from 5424 to DBI assembler
Send Punch check byte and 'channel binary subt' to CPU
Any bits on DBO
Set 'Pch check' latch
Send 'channel I-O check' to CPU
SET STATUS BYTE 1 BIT 1
Last 'Punch Check I-O Cycle' latch
Reset 'Punch I-O cycle', 'any MFCU I-O cycle', and 'last punch check I-O cycle'
Send 'CS priority bit 4' to CPU
Advance 'rd Pch-Pch Ck Counter'
Drop 'normal Punch Check I-O Cycle'
Row 32 Checked
C
Diag 5-390
D
Diag 5-390
E
Diag 5-390
F
Diag 5-390

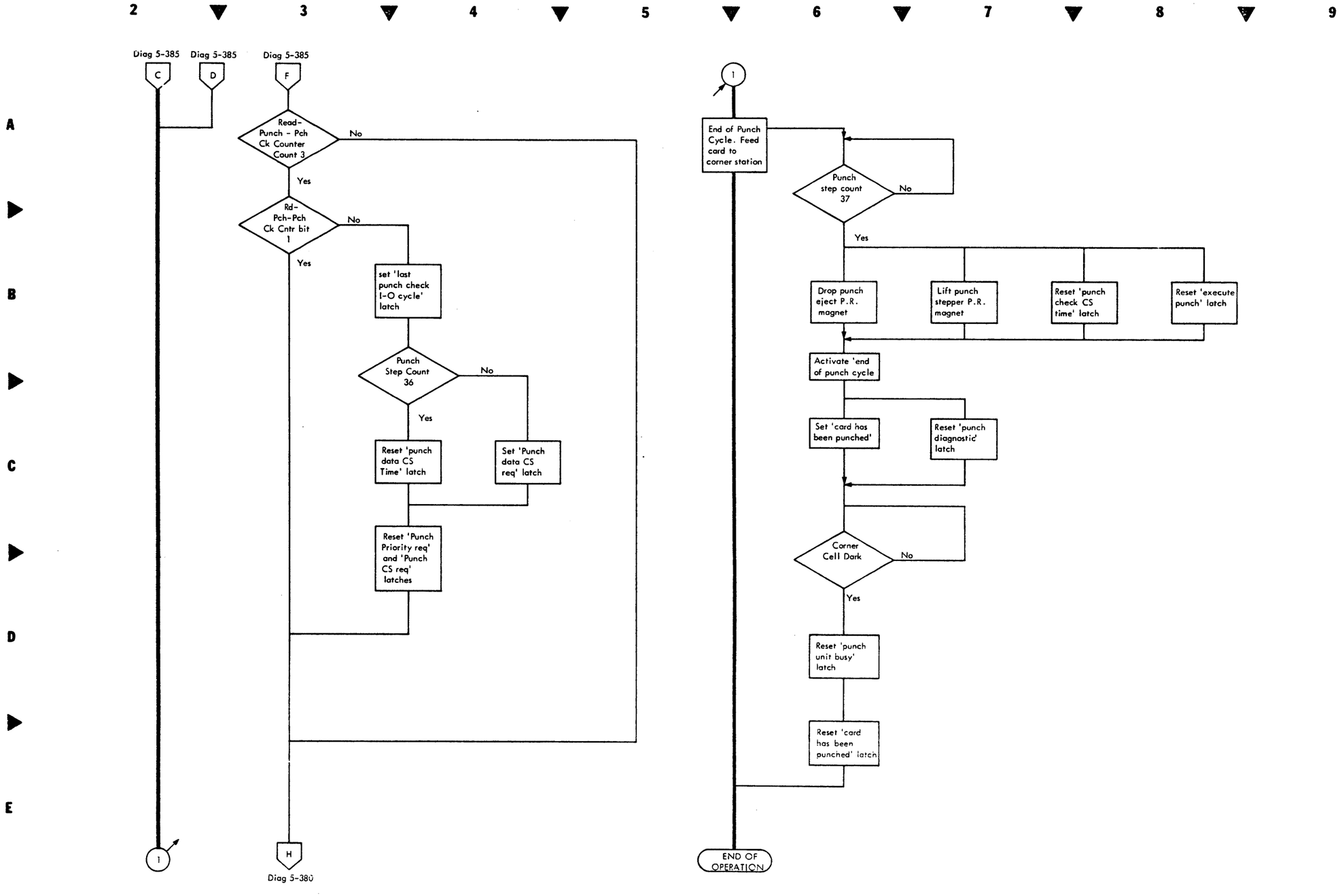
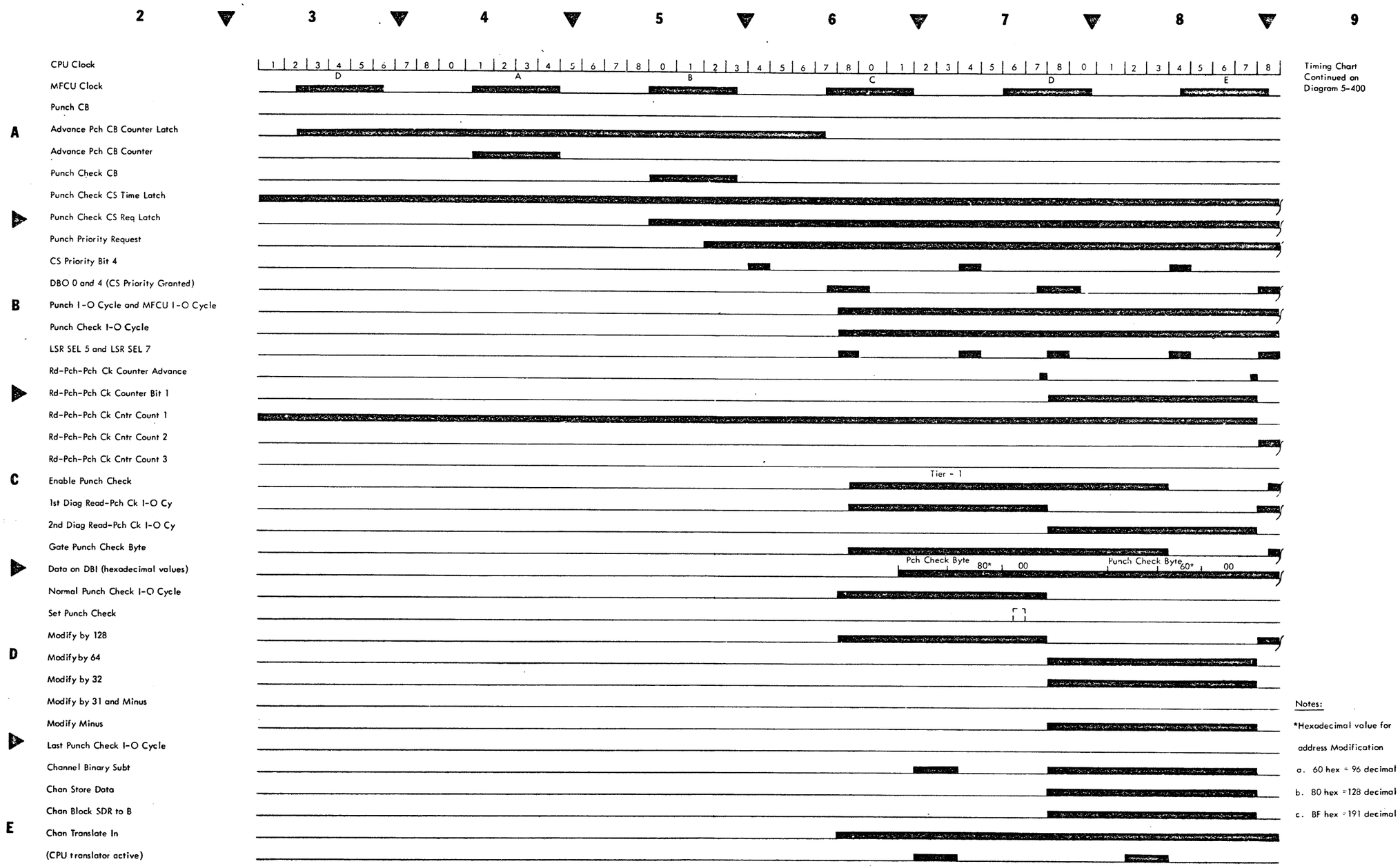


Diagram 5-390. Diagnostic Punch/Feed Operation Flowchart (Part 3 of 8)

Diagram 5-395. Diagnostic Punch/Feed Timing Chart (Part 4 of 8)



Timing Chart Continued on Diagram 5-400

Notes:

*Hexadecimal value for address Modification

a. 60 hex = 96 decimal

b. 80 hex =128 decimal

c. BF hex =191 decimal

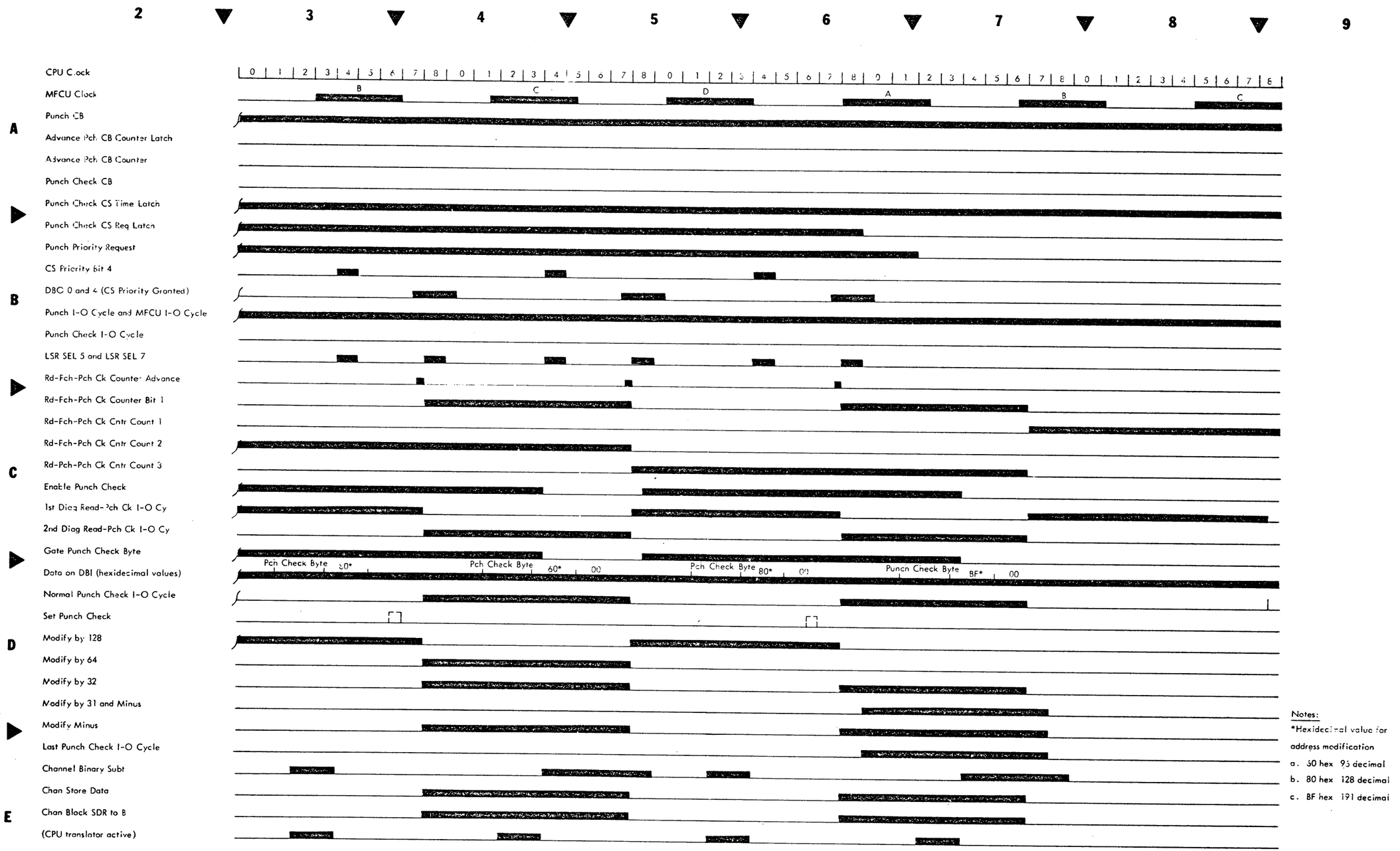


Diagram 5-400. Diagnostic Punch/Feed Timing Chart (Part 5 of 8)

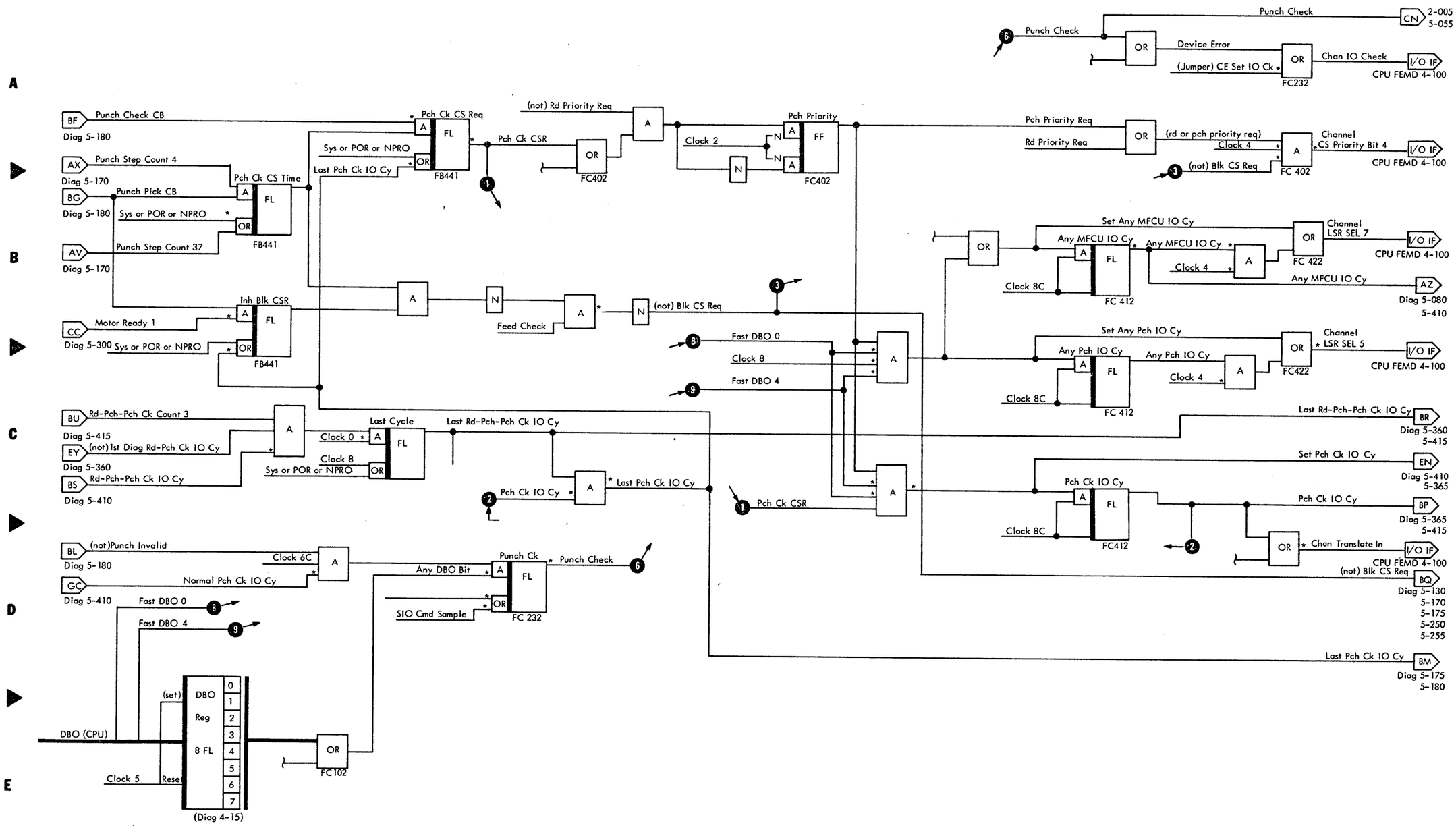


Diagram 5-405. Diagnostic Punch Check Cycle Steal Channel Controls (Part 6 of 8)

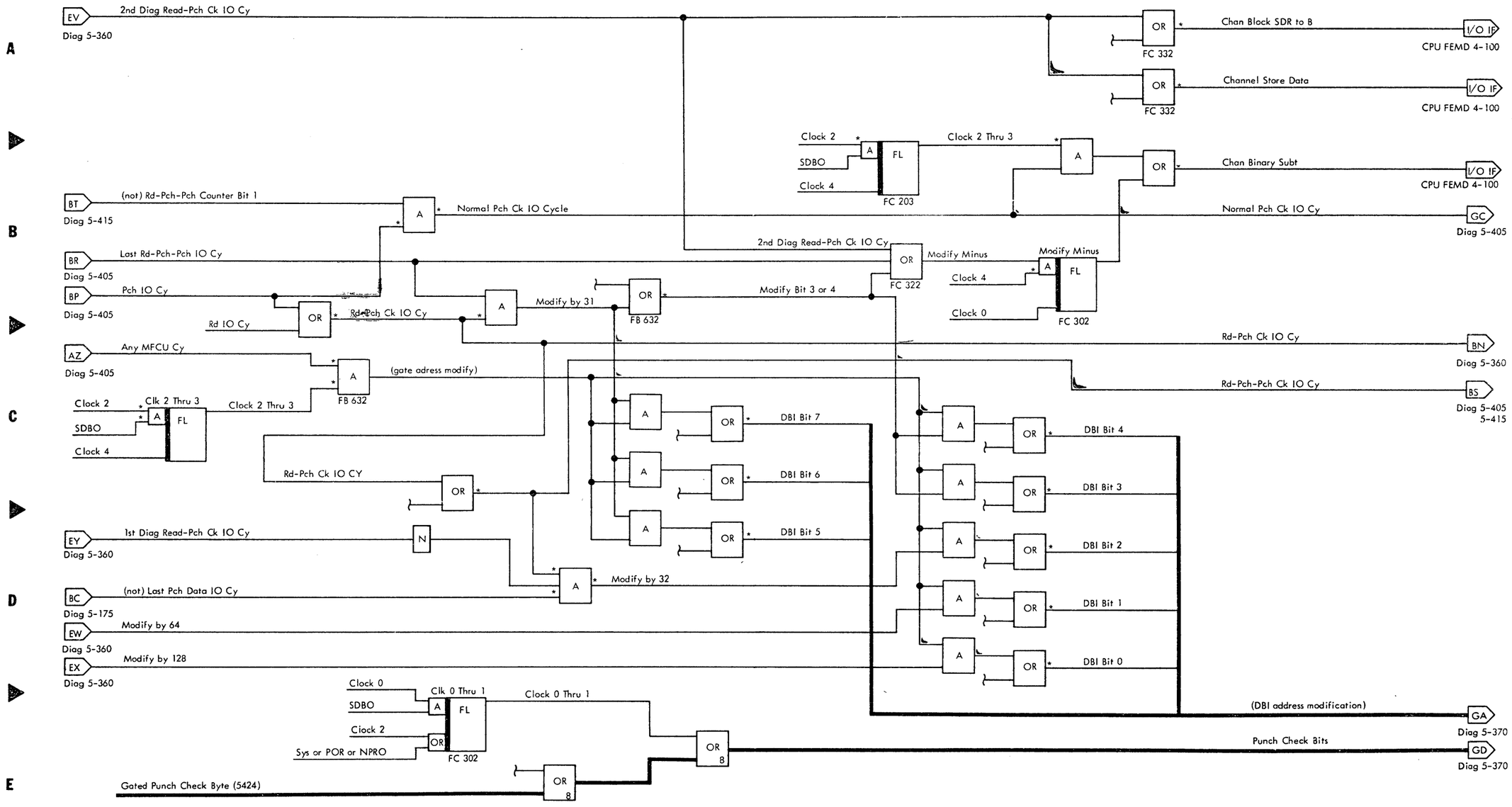
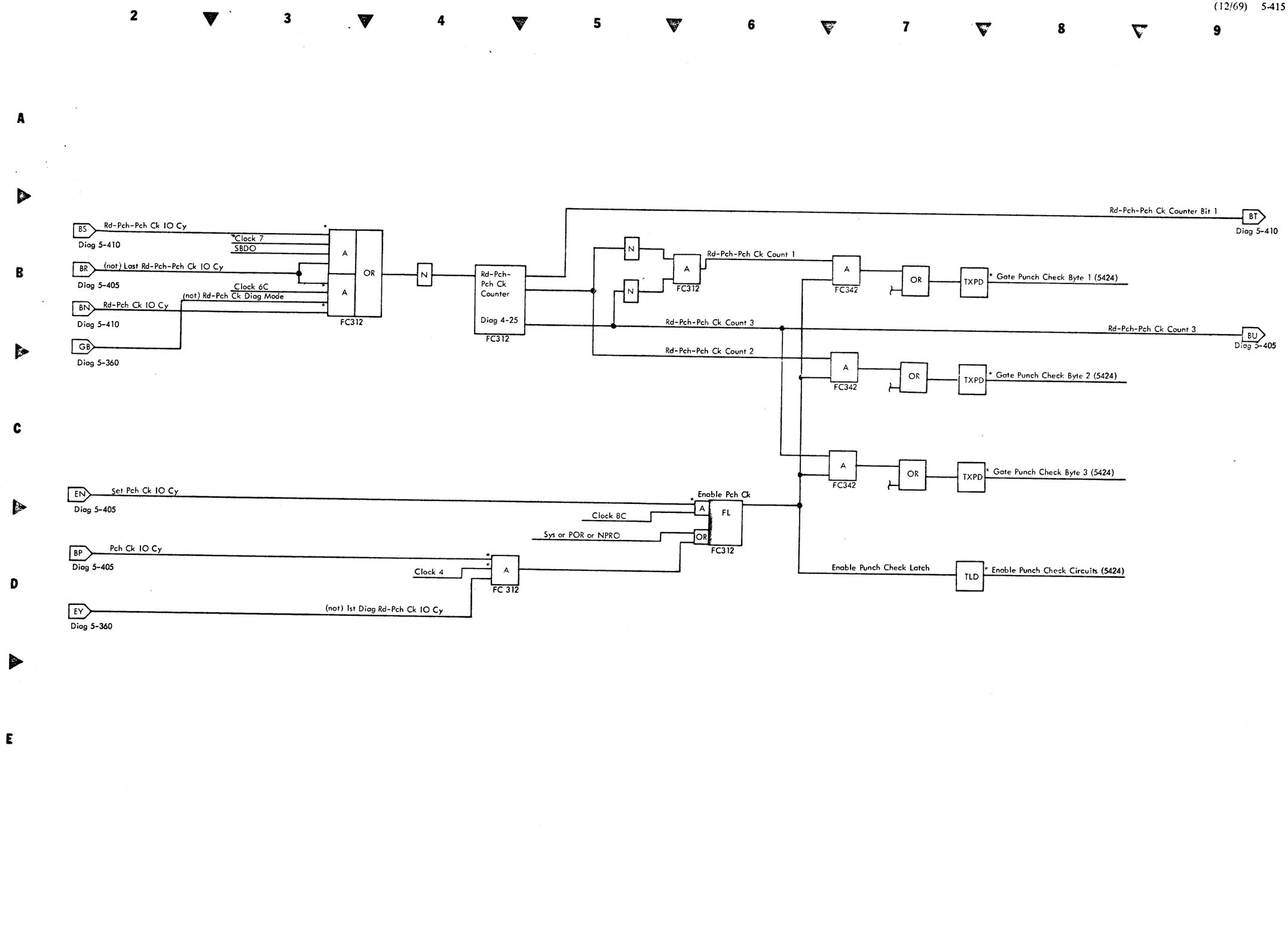


Diagram 5-410. Diagnostic Punch/Feed Address Modification and Check Data Transfer (Part 7 of 8)


2
3
4
5
6
7
8
9
A
B
C
D
E
BS
Rd-Pch-Pch Ck 10 Cy
Diag 5-410
BR
(not) Last Rd-Pch-Pch Ck 10 Cy
Diag 5-405
BN
Rd-Pch Ck 10 Cy
Diag 5-410
GB
Diag 5-360
Clock 7
SBDO
Clock 6C
(not) Rd-Pch Ck Diag Mode
A
A
OR
FC312
N
Rd-Pch-Pch Ck Counter
Diag 4-25
FC312
Rd-Pch-Pch Ck Counter Bit 1
BT
Diag 5-410
N
N
A
FC312
Rd-Pch-Pch Ck Count 1
A
FC342
OR
TXPD
* Gate Punch Check Byte 1 (5424)
Rd-Pch-Pch Ck Count 3
Rd-Pch-Pch Ck Count 3
BU
Diag 5-405
Rd-Pch-Pch Ck Count 2
A
FC342
OR
TXPD
* Gate Punch Check Byte 2 (5424)
A
FC342
OR
TXPD
* Gate Punch Check Byte 3 (5424)
EN
Set Pch Ck 10 Cy
Diag 5-405
BP
Pch Ck 10 Cy
Diag 5-405
EY
(not) 1st Diag Rd-Pch Ck 10 Cy
Diag 5-360
Clock 4
A
FC 312
Enable Pch Ck
Clock 8C
Sys or POR or NPRO
A
OR
FL
FC312
Enable Punch Check Latch
TLD
* Enable Punch Check Circuits (5424)

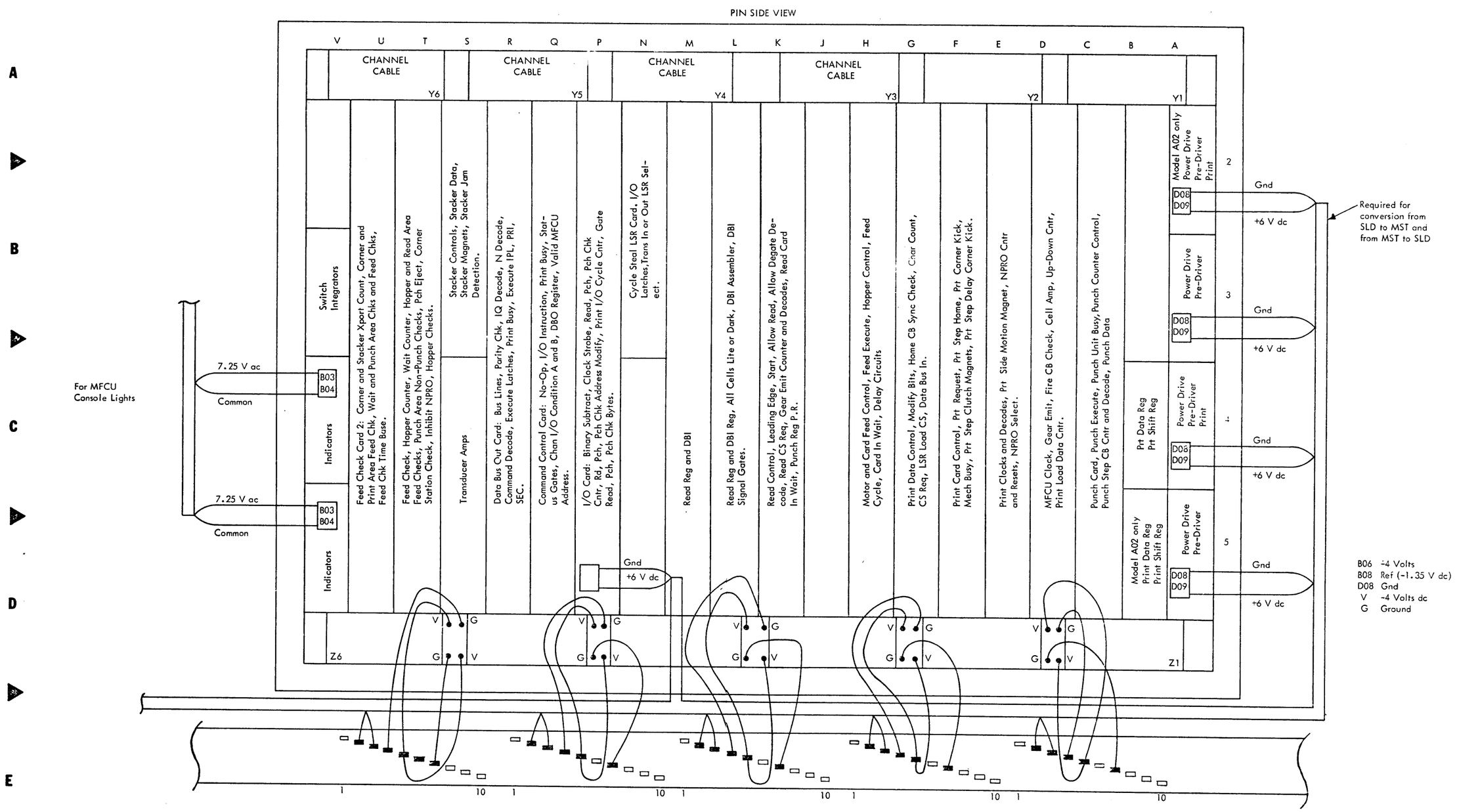


Diagram 6-005. 5424 Attachment Panel and Power Distribution

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