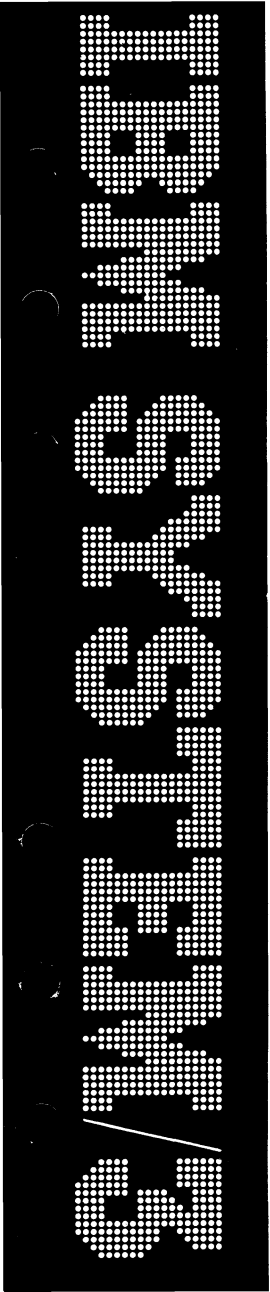

IBM System/3 Field Engineering Handbook

Second Edition (October 1970)
This is a major revision of, and makes ZY29-4046-0 obsolete.

A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be addressed to IBM Corporation, FE Technical Operations, Department 900, Rochester, Minnesota 55901.

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INDEX (continued)

ABBREVIATIONS

AAR	Operand 2 Address Register
ALD	Automated Logic Diagram
ALU	Arithmetic and Logic Unit
APL	Advance Program Level
ARR	Address Recall Register
Asynchronous	Without regular time relationships
BAR	Operand 1 Address Register
Bit	Binary digit; smallest unit of information
BM	Bill of Material
BSCA	Binary Synchronous Communications Adapter
BSM	Basic Storage Module
Byte	Eight bits of information plus parity bit
Channel	A hardware device that connects the CPU and main storage with the I/O control units
CPU	Central Processing Unit
CRR	Condition Recall Register
DBI	Data Bus In
DBO	Data Bus Out
DCF	Disk Control Field
DCP	Diagnostic Control Program
DFC	Dual Feed Carriage
DFCR	Disk File Control Register
DFDR	Disk File Data Register
DPF	Dual Program Feature
DRR	Data Recall Register
DSD	Disk Storage Drive
EC	Engineering Change
ECA	Engineering Change Announcement
FBM	Field Bill of Material
FEALD	Field Engineering Automated Logic Diagram
FIP	Fault Isolation Program
IAR	Instruction Address Register
Interrupt	A signal from an I/O device wanting service which causes the central processor to cease its normal execution of instructions and branch out to a new instruction stream.
I/O	Input-Output
IPL	Initial Program Load
ITC	Initial Table of Contents
K	Thousand
L	Length Count
LCR	Length Count Register
LCRR	Length Count Recall Register
LPDAR	Line Printer Data Address Register
LPIAR	Line Printer Image Address Register
LSR	Local Store Register
MES	Miscellaneous Equipment Specification
MFCU	Multi-Function Card Unit

ABBREVIATIONS (continued)

MLC	Machine Level Control
MPCAR	MFCU Punch Data Address Register
MPTAR	MFCU Print Data Address Register
MRDAR	MFCU Read Data Address Register
MST	Monolithic System Technology
PAIR	Product Analysis Incident Report
PEB	Printer Electronic Board
PSR	Program Status Register
REA	Request for Engineering Action
RPQ	Request Price Quotation
SAR	Storage Address Register
SDR	Storage Data Register
SIOC	Serial Input/Output Channel
SLD	Solid Logic Dense
SLT	Solid Logic Technology
SMS	Standard Modular System
S/Z	Sense/Inhibit
TAP	Timing Analysis Program
UCS	Universal Character Set
XR1	Index Register 1
XR2	Index Register 2
XR	Index Register
XRD	X Read
XWR	X Write
YRD	Y Read
YWR	Y Write
Z	Inhibit

ACCESS PANELS ON THE SYSTEM/3

Access Panel	
Area	Panel
CPU, memory and attachment	A
MFCU–mech	D
elec	E, F
Printer–mech	G
PCB elec	H
PEB elec	I
Power Supplies	
+60Vdc	H
–4Vdc +6Vdc	A or B
Memory	A or B
+24Vdc	E
BSCA	
Med Speed –12Vdc	J
Console	C
Cables	F
Power Control Board	J,A
Documents	K

5410 BOARDS AND POWER SUPPLY LOCATIONS

Front View With Gates open

5410 POWER SUPPLY LOCATION
(Printed Circuit Power Sequence Panel)

Console and A Gate Removed

5410 CONSOLE LIGHTS/SWITCHES

Note: Switches should only be altered with the system in a stop state.

ADDRESS/DATA SWITCHES

These switches are used to set up addresses or data. An address can be loaded into the Storage Address Register. Data can be entered into main storage.

CE KEY SWITCH

This key switch, when switched to the CE position, prevents the customer Usage Meter from running.

CE MODE SELECTOR

This rotary switch selects one of the three processor operating modes: the normal PROCESS mode, the STEP mode, or the TEST mode. PROCESS is the mode for normal programmed system operation.

A. In the STEP mode, the rotary switch setting controls the manner in which the processor performs the stored program.
   1. *Instruction Step.* Each depression and release of the Start key causes one complete instruction to be performed. The I-Phase is performed while the key is pressed, and the E-Phase, if any, when it is released.
   2. *Machine Cycle Step.* Each Start key depression and release advances the instruction through one machine cycle. Depression of the key causes data in storage to be accessed, modified as required, and result to be displayed in the ALU indicators of the console display. Upon release of the key, depending upon the operation being performed, either the old data or the new result is written back into storage.
   3. *Clock Step.* Each depression of the Start key causes the clock to advance through an odd-numbered clock, and each release through an even-numbered one.

      Note: If no DPF on the system, the halt ID lights will not light.

      Note: The integrity of I/O data transfers is preserved by allowing the clock to 'idle' from I-Phase end of every executable Start I/O instruction, until data transfer to or from the device is complete.

B. The switch settings under the TEST mode permit the following:
   1. *Alter SAR.* The address, set up in the address switches, is transferred into SAR by the Start key via the current IAR. Both SAR and IAR are modified.
   2. *Alter Storage.* Depression of the Start key transfers data, set up in the rightmost two Data Switches, into the A register. Releasing the key causes this data to be placed in the storage location specified by SAR and into the Q register.
   3. *Display Storage.* The contents of the storage location specified by SAR are transferred into the B register when the Start key is pressed. These contents are rewritten into storage when the key is released, and are also transferred into the Q register.

      Note: The STORAGE TEST SWITCH must be in the STEP position to avoid a processor check when changing the CE MODE SELECTOR from ALTER STORAGE position to DISPLAY STORAGE position and vice versa. Invalid address are not checked for while the system is in the TEST mode.

5410 CONSOLE LIGHTS/SWITCHES (continued)

ADDRESS COMPARE SWITCH

This switch allows stopping the program when the setting of the (Address/Data) switches matches SAR. This switch will only be functional when the register display is positioned to SAR and the system is in the PROCESS mode.

With the switch in the RUN position, comparison of address switches to SAR via the register display is performed, but no processor stop is initiated when a match occurs. The 'matched' signal is provided as a CE 'sync' point.

When the switch is in the STOP position, a match of the address switches and the register display results in a processor stop at the completion of the storage read-write cycle.

The processor is restarted by activating the Start key.

Note: The integrity of I/O data transfers is preserved. The contents of SAR do not necessarily match the setting of the address switches at stop time.

I/O CHECK SWITCH

This switch, when on, forces the processor to come to an immediate stop on certain I/O errors.

The switch is normally set to RUN. With the switch set to STOP, the processor stops on an I/O error with the console display frozen to indicate the processor status at the time the error stop occurred, and the I/O device turns ON the I/O check light.

A check reset followed by the Start key is the normal restart after an I/O error stop.

Note: When the I/O check switch is in the STOP position and an I/O error occurs, the processor check light will turn ON.

PARITY CHECK SWITCH

This switch enables override of the processor parity errors.

The switch is normally set to STOP. This causes the processor to come to an immediate stop whenever a parity error is detected. A check reset followed by the Start key is the normal restart after a parity stop. With the parity switch in the RUN position, parity errors are detected and displayed, but the processor is not stopped.

ADDRESS COMPARE LIGHT

This light is on whenever the address switches match the contents of the Storage Address Register, the register display is positioned to SAR and the address compare switch is in the STOP position.

5410 CONSOLE LIGHTS/SWITCHES (continued)

SYSTEM RESET KEY

A system reset causes the system to enter an immediate 'idle' state. All I/O machine registers, controls, and status indicators are reset and the processor clock is allowed to 'idle'. A complete program restart is normally required after a system reset.

The following LSR's are reset to zero by a system reset:

P1 - IAR
P1 - PSR
P2 - PSR

The other LSR's are not changed by a system reset.

Note: The CE mode selector must be in process mode for the system reset key to be effective.

CHECK RESET KEY

This pushbutton is pressed to cause a reset of the Processors and/or I/O check conditions, and also resets a system power check to allow a power on retry.

A check reset removes the current error conditions, thus allowing the processor to resume its operation after the Start key is depressed.

FILE WRITE SWITCH

This switch when in the OFF position will inhibit all writing on all disk surfaces.

DPF Switches

P1 Switch - Dual Program Level One. When OFF, inhibits branching into Program Level One.
P2 Switch - Dual Program Level Two. When OFF, inhibits branching into Program Level Two.

Warning - Unpredictable errors will occur if both P1 and P2 switches are off.

5410 CONSOLE LIGHTS/SWITCHES (continued)

STORAGE TEST SWITCH

This switch enables the altering or displaying of storage as follows:

A. In the STEP position, a storage location is accessed with each depression of the Start key.
B. In the RUN position, following the Start key depression, core storage is exercised by accessing either the same location repetively or all of core sequentially (see Address Increment Switch).

ADDRESS INCREMENT SWITCH

This switch enables address incrementing when in the CE test modes of Alter or Display storage. With the switch in the ON position, the contents of SAR are incremented by one after each storage access. When the switch is in the OFF position, SAR is not incrementing.

I/O OVERLAP SWITCH

This switch modifies control of the system so that I/O operations may be executed in either an overlap or a non-overlap mode. With the switch in the normal ON position, I/O operations are executed in an overlap mode. When the switch is in the OFF position, I/O operation is completed prior to execution of the next sequential instruction.

LSR DISPLAY SELECTOR (Should be in the normal position when processing.)

This rotary switch selects the Local Storage Register (LSR) whose contents are to be displayed.

LSR's that can be manually selected for display via this switch are: IAR, ARR, XR1, and XR2.

Refer to MST Tie-Up Data for procedure to display other LSRs.

When the switch is in the Normal or OFF position, the system controls the selection and display of the LSR's. If the switch is in other than the Normal position, the specified LSR is selected and its contents are available for display whenever the processor clock is stopped, or if the clock is running, when no CPU machine cycles and no I/O data transfer cycles are being taken. In the OFF position LSR selection by the CPU is inhibited and if no I/O device is selecting an LSR, the LSR display will have all bits OFF.

5410 CONSOLE LIGHTS/SWITCHES (continued)

I/O Check Light

This light is turned on when the following I/O errors are detected:

1442

1. A SIO instruction is issued to the 1442 and the NO-OP bit is on.

2. Whenever the 1442 Attachment detects the following:
   - Punch check
   - Read reg
   - Overrun
   - Any condition that turns on the 1442 check light

This light is turned OFF by a system reset, a check reset, an NPRO, the SNS instruction which senses the NO-OP bit (if a NO-OP was the cause), or by a SIO instruction to the 1442 in the case of a read check or a punch check.

5424 MFCU

1. An SIO instruction is issued to the 5424 and the NO-OP bit is ON.

2. Whenever the 5424 Attachment detects the following:
   PRINT DATA CHECK
   PRINT CLUTCH CHECK
   PUNCH CHECK
   PUNCH INVALID CHECK
   READ CHECK

This light is turned OFF by a system reset, a check reset, or an NPRO for all of the above checks. It may also be reset by the SNS instruction to the MFCU in the case of NO-OP, print data check, print clutch check or a punch invalid check, or by a SIO instruction to the MFCU in the case of a read check or a punch check.

SIOC

Indicates a data transfer register parity error occurred.

This light is turned off by a system reset, check reset or by a SIO instruction.

I/O Check Light

PRINTER - 5203

1. A SIO instruction is issued to the 5203 and the 5203 check light is ON.

2. Whenever the 5203 Attachment detects the following:
   INCREMENTOR FAILURE CHECK
   HAMMER ECHO CHECK
   ANY HAMMER ON CHECK

This light is turned off by a system reset, a check reset, the printer start key or by the SNS instruction which senses the check bit.

FILE - 5444

None

KEYBOARD PRINTER 5471

None

KEYBOARD - 5475

None

BSCA

Indicates a unit check has occurred. See BSCA SNS inst, N code 011, byte 2 for specific error.

This light is turned off by a system reset, a check reset, or through programming in the case of retry.

5410 CONSOLE LIGHTS/SWITCHES (continued)

BSCA Panel

(X) DT TERM READY
Lights when the BSCA is enabled and the data terminal ready line to the MODEM is on. In case of the connect data set to line requirement, the indicator lights when the connect data set to line signal is activated.

(X) TEST MODE
Lights when an SIO instruction has been issued by the program to place the BSCA in test mode.

(X) BSCA ATTN
Lights when the BSCA rejects an SIO instruction because operator intervention is required because:

1. The data set ready latch is off when a receive, receive and transmit, or receive initial SIO instruction is executed.
2. The auto call unit power is off or the data line is occupied when an SIO auto call or an SIO receive initial instruction is executed (switched networks).
3. The BSCA is disabled.
4. The external test switch is on and the BSCA is not in test mode. An SIO control instruction is used to enable the BSCA and to place the BSCA in test mode.
5. If the data ready signal from the MODEM is de-activated unexpectedly while the BSCA is enabled.

(X) TSM MODE
Lights when the BSCA is to perform a transmit operation.

(X) RECEIVE MODE
Lights when the BSCA is to perform a receive operation.

(X) RECEIVE INITIAL
Lights when a receive initial SIO instruction is received. It turns off at the end of the receive initial operation.

(X) CONTROL MODE
(Station Select Feature) Lights when an EOT sequence is detected in a transmit, receive, or receive initial monitor operation. It turns off by the decode of an SOH or STX or a receive timeout.

(X) ACU PWR OFF
(Auto Call Feature) Lights when the auto call unit has power off.

5410 CONSOLE LIGHTS/SWITCHES (continued)

BSCA Panel

(X) DATA MODE
Lights when an SOH or STX is decoded during a transmit or a receive operation. It is turned off at the end of the operation.

(X) DT SET READY
Lights when the data set ready line from the MODEM is active and the MODEM is ready for use.

(X) EXT TEST SW
Lights when the switch at the MODEM end of the medium speed MODEM cable is in the test position or the switch on the CPU CE panel for high-speed feature is in the local test position.

(X) TSM TRIGGER
Lights when the transmit trigger is at a binary zero state (equivalent to a space on the communication line).

(X) RECEIVE TRIGGER
Lights when the receive trigger is at a binary zero state (equivalent to a space on the communication line).

(X) UNIT CHECK
Lights when unit check condition exists. Turned on by any bit in status byte 2 (see SNS inst "N" code 011).

(X) DIGIT PRESENT
(Auto Call Unit Feature) Lights when the BSCA has a digit present on the auto call unit interface to be used for dialing.

(X) DT LINE IN USE
(Auto Call Unit Feature) Lights when the data line occupied from the ACU is active.

(X) CLEAR TO SEND
Lights when the line from the MODEM is active. The BSCA may now transmit.

(X) CHAR PHASE
Lights when the adapter has established character synchronization with the transmitting station by receiving two successive SYN characters. The indicator is turned off at the end of the receive operation.

(X) BUSY
Lights when the BSCA is executing a receive initial, transmit and receive, auto call, receive, or loop test instruction.

(X) CALL REQUEST
(Auto Call Unit Feature) Lights when the BSCA receives an auto call SIO instruction and is performing an auto call operation.

5410 CONSOLE LIGHTS/SWITCHES (continued)

PROCESSOR CHECKS

I/O LSR	Indicates selection of an LSR by an I/O device was not performed correctly.
LSR F1	Parity is incorrect on the output of the LSR Feature 1.
LSR F2	Parity is incorrect on the output of the LSR Feature 2.
LSR HI	Parity is incorrect on the output of the LSR High.
LSR LO	Parity is incorrect on the output of the basic LSR Low.
SAR HI	Parity is incorrect in the Storage Address Register High.
SAR LO	Parity is incorrect in the Storage Address Register Low.
INV ADDR	Indicates that the SAR contains an invalid address.
SDR	Parity is incorrect in the Storage Data Register.
CAR	Indicates the carry out of the ALU is incorrect.
A/B	Indicates the A or B Register has incorrect parity.
ALU	Indicates the output of the ALU has incorrect parity.
DBI	Parity is incorrect on the CPU end of the Data Bus In.
CPU DBO	Parity is incorrect on the CPU end of the Data Bus Out.
OP/Q	Parity is incorrect in the OP Register or Q Register.
INV OP	Indicates an invalid OP Code in the OP Register.
CHAN DBO	Parity is incorrect on the I/O Device end of the Data Bus Out.
INV Q	Indicates an invalid Q byte is present in an I/O instruction.

I/O ATTENTION

The I/O attention light indicates to the operator that one or more of the attached I/O devices requires attention caused by a 'normal' I/O condition. 'Normal' is defined as: empty hopper, full stacker, out of forms, etc. as opposed to check conditions.

Recovery - Operator must determine cause of indication, rectify the cause and return device to the READY status.

Note: Refer to individual devices for 'normal' definition, recovery and/or restart procedures for that device.

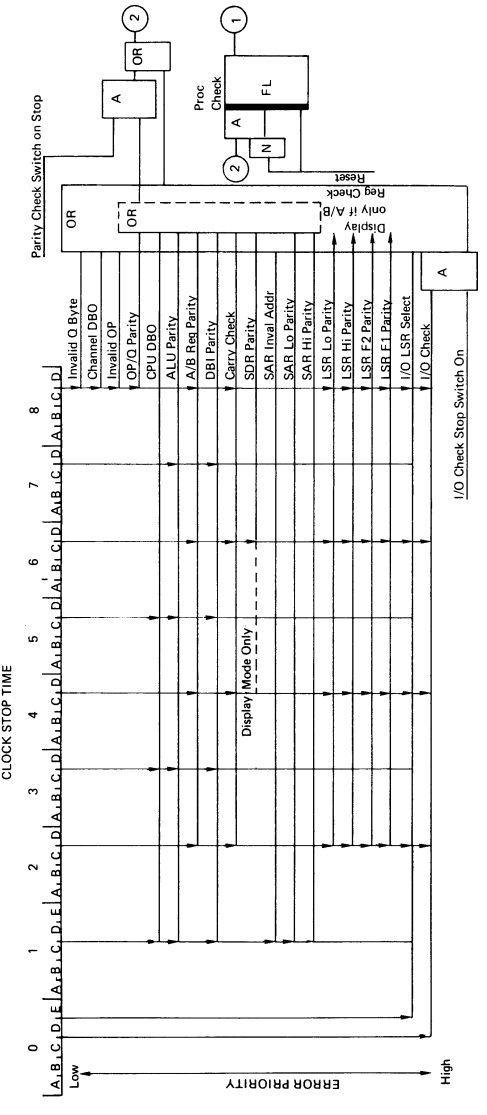
UNIT CHECK

TESTABLE INDICATORS

Unit check handling of testable indicators is controlled by software.

Restart procedures are conveyed to the operator via programmed HALT operation, HALT IDENTIFIER'S displayed on the console and recovery/restart procedure listings.

PROCESS CHECK ERROR PRIORITY



	During Which Operation Check Is Given					Under Which Photo Cell Condition Check is Given					
	Every Operation	Punch Operation	Non-Punch Operation	Print Operation	Non-Print Operation	Covered Late	Uncovered Late	Uncovered Early	Never Dark	Dark Without Feed Cycle	
Hopper Check	x								Hopper Cell		Card never covered cell.
Feed Check 1	x					Hopper Cell					Card covered cell late.
Feed Check 2	x					Read Cells					Card late getting to read station.
Feed Check 3										Read Cells	Card in read station between feed cycles.
Feed Check 4	x						Read Cells				Card too long in read station.
Feed Check 5	x									Prepunch	Card left wait station without punch registration pressure roll.
Feed Check 6			x			Prepunch					Card late to prepunch cell.
Feed Check 7		x				Prepunch					Card late to prepunch cell in punch operation.
Feed Check 8		x						Prepunch			Card out of registration in punch operation.
Feed Check 9			x				Prepunch				Card too long in punch station.
Feed Check 10		x					Prepunch				Card out of registration in punch operation.
Feed Check 11			x			Corner					Card late to corner non-punch operation.
Feed Check 12		x				Corner					Card late to corner punch operation.
Feed Check 13	x							Corner			Card left corner without kicker.
Feed Check 14					x		Corner				Card left corner late non-print operation.
Feed Check 15				x			Corner				Card left corner late print operation.
Feed Check 16					x	Postprint					Card too long in print station.
Feed Check 17				x		Postprint					Card early or late leaving print station.
Feed Check 18							Postprint				Card too slow to stacker transport.
Feed Check 19	Stacker							Jam			
Feed Check 20	Gear emitter check or fire CB check										

For other 5424 checks refer to 5424 SNS bytes (N code 011, byte 1)

5203 PRINTER CHECKS

This light is turned on when the accuracy of printing is questionable. The errors are displayed with a programmed halt.

The errors that turn on the light are:

*a. Carriage sync check
b. Carriage space check
c. Forms jam
*d. Incrementor failure
*e. Hammer echo check
*f. Any hammer on check
*g. Chain sync check
*h. Incrementer sync/slip check
*i. Thermal check

The error cause can be determined by the unique halt indicator or by probing the following points. The check must not be reset prior to probing. A *Down Level* indicates an error.

SOCKET LOCATION = A-B1K4

CHECK	PIN		PIN	CHECK
HMR ECHO	D02	0 0	B02	ANY HMR ON
		0 0	B03	FORMS JAM
		0 0	B05	THERMAL
		0 0	B10	INCR SYNC/SLIP
CHAIN SYNC	D11	0 0		
CARR SPACE	D12	0 0		
INCR FAIL	D13	0 0	B13	CARR SYNC

*These checks will drop 60vdc to the printer.

BSCA ERROR CONDITIONS

Timeout

1. Receive operation with the adapter in the busy state.
2. Auto call operation terminated by an abandon call and retry signal from the ACU, indicating that a connection was not established.

CRC/LRC/VRC

1. Block check character compare error.
2. Vertical redundancy check using USASCII code.

Adapter Check - Transmit

1. DBI register parity check.
2. I/O cycle steal overrun.
3. LSR or shift register parity check.
4. Transmit control register check.

Adapter Check - Receive

1. DBI register parity check.
2. I/O cycle steal overrun.
3. LSR or shift register parity check.

Invalid ASCII Character

Invalid ASCII character fetched from core during ASCII transmission.

Abortive Disconnect

With the BSCA enabled, the data set ready latch comes on and then goes off indicating release of the connection and causing data terminal ready to go off.

Disconnect Timeout

On a switched network, this error is set whenever a disconnect timeout occurs. It causes data terminal ready to go off.

Affected Instructions	Condition	Program Test	Result
Receive, Transmit & Receive, Receive Initial (Non-SW/MP)	Data Set Ready Latch Off	Status Bit [2] TIO NR [3] (Non-SW/MP)	Instruction Rejected I/O Attention Indicator BSCA Attention Indicator
Auto Call or Receive Initial (SW)	ACU Power Off or Data Line Occupied On	TIO NR Status Bit [1]	Instruction Rejected I/O Attention Indicator BSCA Attention Indicator
LIO except 110 or SIO except Control	Busy	TIO Busy	Instruction Rejected
SIO except Control	BSCA Disabled or External Test Switch On and Test Mode Disabled	TIO NR TIO NR	Instruction Rejected I/O Attention Indicator BSCA Attention Indicator
None	Data Set Ready Latch On and Data Set Ready Off		I/O Attention Indicator BSCA Attention Indicator

1. Status Byte 1, Bit 7 Data Line Occupied

2. Status Byte 1, Bit 6 Data Set Ready Condition

3. Not Ready includes Data Set Ready Latch Off on a non-switched, point-to-point or multipoint network.

5471, SIOC, 5444 ERROR CONDITIONS

5471 CONSOLE I/O ERROR CONDITIONS

Keyboard Check
Parity error was detected coming from the reed switches.

Keyboard Translator Check
Parity error detected coming from keyboard code to System/3 card code translator.

Printer Translator Check
Parity error was detected coming from System/3 card code to tilt-rotate code translator.

Printer Malfunction
Describes generally the malfunction of printer feedback contacts. This condition is caused by any of the following:

a. Printer cycle too long.
b. Printer extra cycle.
c. Printer feedback too late.

SIOC ERROR CONDITIONS

I/O Check Light
Indicates a data transfer parity check condition.

I/O Attention Light
This light along with the SIOC indicator shows operator intervention required on attached I/O device.

5444 ERROR CONDITIONS

The following "file unsafe" conditions drop file ready.

1. Write Unsafe
   a. Write selected and no write transitions detected.
   b. Write selected and multiple heads selected.
   c. Write not selected and write current source on.

2. Erase Unsafe
   a. Write selected and erase current source not on.
   b. Write not selected and erase current on.

3. Read/Write Selection Unsafe
   a. Read selected and either write or erase selected.
   b. Carriage accessing and either write or erase selected.

Unsafe will set equipment check.

For all other file errors, refer to file SNS bytes.

ENVIRONMENTAL RECORDING

CARD SYSTEM

Errors detected during an RPG object program run will be stored in the communications area starting at core location /0180/. Forty-two bytes have been reserved for this, broken into two sections of 10 and 32 bytes. The 6-byte section is used to record 5203 hammer echo checks. Each of the 6 bytes will contain the failing print position. (Refer to Table 3 in the 5203 map charts.) In case more than six errors have occured, only the last six will be shown. The 32-byte section is made up of eight 4-byte sections showing the last eight errors to occur. Each 4-byte section will contain the Q, R, and 2 sense bytes of data about the failing instruction. These 42 bytes of information along with the date will be punched out into a card during a system installation run. This card will be merged with the system initialization program deck and will be the card just preceding the end card. This data will be the error data accumulated since the last system initialization run.

The card format for the card punched out is:
Col 1 - W
Col 2 thru 65 - Error history table in hex. Eight sections of 4 bytes each containing the Q, R, and 2 sense bytes.
Col 66 thru 77 - 5203 hammer echo check data
Col 78 thru 93 - Reserved
Col 94 thru 96 - Date (coded)
(Card format effective with SIP Vers 1 Mod 3)

DISK SYSTEM

Statistical Data Recording (SDR)

Statistical data is recorded in a table occupying sectors X'0C' through X'18'. This table consists of 512 two-byte counters. Each device is allotted an area consistent with the number of distinguishable errors possible for that device. Devices such as the 5444 and BSCA will have counters to record both temporary and permanent error occurrences. A permanent error is defined as one which persists throughout the maximum number of retries outlined in the device's error recovery procedures. A temporary error is defined as one where recovery occurs before the maximum number of retries.

For example:

Disk File

	Overrun	Data Check in ID	
Temp	2 bytes	2 bytes	etc
Perm	2 bytes	2 bytes	etc

ENVIRONMENTAL RECORDING (continued)

Out Board Recording (OBR)

Each error, whether temporary or permanent, is entered in a history table. This table is two sectors long (sectors 1C and 20 and provides 63 8-byte entries. The first four bytes of this sector will be two 2-byte displacements. The first will be the displacement of the next available entry in the table and the second will be the end of the table. This table will be recursive and no overflow or stop logic will be provided. The 64th time an entry is made, it will overlay the first entry; the 65th time will overlay the second, etc. Therefore, the table will always contain entries for the 63 most recent errors.

The basic entry for each device will consist of the following:

Q	R	PRIMARY SENSE REGISTER	DEVICE DEPENDENT INFO
1 byte	1 byte	2 bytes	4 bytes

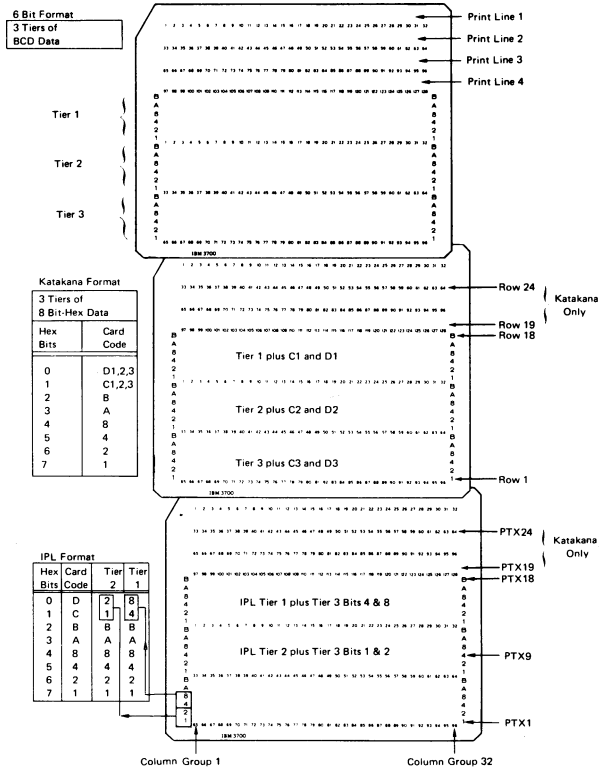
Disk errors will require two entries (16 bytes).

In addition to SDR and OBR recording, statistics are kept on each disk volume to help detect surface degradation. Each volume has an area to record the number of write and non-write SIOs issued to that volume, a count of temporary errors and a table of permanent errors occurring on that volume. A master table of all writes and non-writes issued to each unit on the system is kept on cylinder 0, sector 0C. Control SIOs are not included in these statistics.

The master table for a dual drive, full capacity system looks like this:

		Displacement X'0C' ↓ Writes & Verifies	Reads & Scans
DRIVE 1	REM	4 bytes	4 bytes
	FIXED	4 bytes	4 bytes
DRIVE 2	REM	4 bytes	4 bytes
	FIXED	4 bytes	4 bytes

96 COLUMN CARD LAYOUT



HEX AND DECIMAL CONVERSION/ADDITION

To find the decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the Hex number, locate the next lower decimal number and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

BYTE 0123		4567		BYTE 0123		4567		BYTE 0123		4567	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
6		5		4		3		2		1	

HEXADECIMAL ADDITION

	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

CODE CONVERSION CHART

1-39 33-69

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
000	00	C		4	1	00000000	
001	01	DCBA 1		A @	A 3	00000001	
002	02	DCBA 2		B @	B 3	00000010	
003	03	DCBA 21		C @	C 3	00000011	
004	04	DCBA 4	ZAZ	D @	D 3	00000100	
005	05	DCBA 4 1		E @	E 3	00000101	
006	06	DCBA 42	AZ	F @	F 3	00000110	
007	07	DCBA 421	SZ	G @	G 3	00000111	
008	08	DCBA8	MVX	H @	H 3	00001000	
009	09	DCBA8 1		I @	I 3	00001001	
010	0A	CBA8 2	ED	¢ 4	¢ 1	00001010	
011	0B	CBA8 21	ITC	. 4	. 1	00001011	
012	0C	CBA84	MVC	< 4	< 1	00001100	
013	0D	CBA84 1	CLC	(4	(1	00001101	
014	0E	CBA842	ALC	+ 4	+ 1	00001110	
015	0F	CBA8421	SLC	| 4	| 1	00001111	
016	10	C A8 2		& 4	& 1	00010000	
017	11	DCB 1		J @	J 3	00010001	
018	12	DCB 2		K @	K 3	00010010	
019	13	DCB 21		L @	L 3	00010011	
020	14	DCB 4	ZAZ	M @	M 3	00010100	
021	15	DCB 4 1		N @	N 3	00010101	
022	16	DCB 42	AZ	O @	O 3	00010110	
023	17	DCB 421	SZ	P @	P 3	00010111	
024	18	DCB 8	MVX	Q @	Q 3	00011000	
025	19	DCB 8 1		R @	R 3	00011001	
026	1A	CB 8 2	ED	! 4	! 1	00011010	
027	1B	CB 8 21	ITC	$ 4	$ 1	00011011	
028	1C	CB 84	MVC	* 4	* 1	00011100	
029	1D	CB 84 1	CLC	) 4	) 1	00011101	
030	1E	CB 842	ALC	; 4	; 1	00011110	
031	1F	CB 8421	SLC	¬ 4	¬ 1	00011111	
032	20	CB		- 4	- 1	00100000	
033	21	C A 1		/ 4	/ 1	00100001	
034	22	DC A 2		S @	S 3	00100010	
035	23	DC A 21		T @	T 3	00100011	
036	24	DC A 4	ZAZ	U @	U 3	00100100	
037	25	DC A 4 1		V @	V 3	00100101	
038	26	DC A 42	AZ	W @	W 3	00100110	
039	27	DC A 421	SZ	X @	X 3	00100111	
040	28	DC A8	MVX	Y @	Y 3	00101000	
041	29	DC A8 1		Z @	Z 3	00101001	
042	2A	DCBA	ED	} @	} 3	00101010	
043	2B	C A8 21	ITC	, 4	, 1	00101011	
044	2C	C A84	MVC	% 4	% 1	00101100	
045	2D	C A84 1	CLC	_ 4	_ 1	00101101	
046	2E	C A842	ALC	> 4	> 1	00101110	
047	2F	C A8421	SLC	? 4	? 1	00101111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
048	30	DC A	SNS	0 @	0 3	00110000	
049	31	DC 1	LIO	1 @	1 3	00110001	
050	32	DC 2		2 @	2 3	00110010	
051	33	DC 21		3 @	3 3	00110011	
052	34	DC 4	ST	4 @	4 3	00110100	
053	35	DC 4 1	L	5 @	5 3	00110101	
054	36	DC 42	A	6 @	6 3	00110110	
055	37	DC 421		7 @	7 3	00110111	
056	38	DC 8	TBN	8 @	8 3	00111000	
057	39	DC 8 1	TBF	9 @	9 3	00111001	
058	3A	C 8 2	SBN	: 4	: 1	00111010	
059	3B	C 8 21	SBF	# 4	# 1	00111011	
060	3C	C 84	MVI	@ 4	@ 1	00111100	
061	3D	C 84 1	CLI	' 4	' 1	00111101	
062	3E	C 842		= 4	= 1	00111110	
063	3F	C 8421		" 4	" 1	00111111	
064	40	None				01000000	Space
065	41	D BA 1		A 8	A 2	01000001	
066	42	D BA 2		B 8	B 2	01000010	
067	43	D BA 21		C 8	C 2	01000011	
068	44	D BA 4	ZAZ	D 8	D 2	01000100	
069	45	D BA 4 1		E 8	E 2	01000101	
070	46	D BA 42	AZ	F 8	F 2	01000110	
071	47	D BA 421	SZ	G 8	G 2	01000111	
072	48	D BA8	MVX	H 8	H 2	01001000	
073	49	D BA8 1		I 8	I 2	01001001	
074	4A	BA8 2	ED	¢	¢	01001010	¢
075	4B	BA8 21	ITC	.	.	01001011	.
076	4C	BA84	MVC	<	<	01001100	<
077	4D	BA84 1	CLC	(	(	01001101	(
078	4E	BA842	ALC	+	+	01001110	+
079	4F	BA8421	SLC	I	I	01001111	I
080	50	A8 2		&	&	01010000	&
081	51	D B 1		J 8	J 2	01010001	
082	52	D B 2		K 8	K 2	01010010	
083	53	D B 21		L 8	L 2	01010011	
084	54	D B 4	ZAZ	M 8	M 2	01010100	
085	55	D B 4 1		N 8	N 2	01010101	
086	56	D B 42	AZ	O 8	O 2	01010110	
087	57	D B 421	SZ	P 8	P 2	01010111	
088	58	D B 8	MVX	Q 8	Q 2	01011000	
089	59	D B 8 1		R 8	R 2	01011001	
090	5A	B 8 2	ED	!	!	01011010	!
091	5B	B 8 21	ITC	$	$	01011011	$
092	5C	B 84	MVC	*	*	01011100	*
093	5D	B 84 1	CLC	)	)	01011101	)
094	5E	B 842	ALC	;	;	01011110	;
095	5F	B 8421	SLC	¬	¬	01011111	¬

If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
096	60	B		–	–	01100000	–
097	61	A 1		/	/	01100001	/
098	62	D A 2		S 8	S 2	01100010	
099	63	D A 21		T 8	T 2	01100011	
100	64	D A 4	ZAZ	U 8	U 2	01100100	
101	65	D A 4 1		V 8	V 2	01100101	
102	66	D A 42	AZ	W 8	W 2	01100110	
103	67	D A 421	SZ	X 8	X 2	01100111	
104	68	D A8	MVX	Y 8	Y 2	01101000	
105	69	D A8 1		Z 8	Z 2	01101001	
106	6A	D BA	ED	} 8	} 2	01101010	
107	6B	A8 21	ITC	,	,	01101011	,
108	6C	A84	MVC	%	%	01101100	%
109	6D	A84 1	CLC	_	_	01101101	_
110	6E	A842	ALC	>	>	01101110	>
111	6F	A8421	SLC	?	?	01101111	?
112	70	D A	SNS	0 8	0 2	01110000	
113	71	D 1	LIO	1 8	1 2	01110001	
114	72	D 2		2 8	2 2	01110010	
115	73	D 21		3 8	3 2	01110011	
116	74	D 4	ST	4 8	4 2	01110100	
117	75	D 4 1	L	5 8	5 2	01110101	
118	76	D 42	A	6 8	6 2	01110110	
119	77	D 421		7 8	7 2	01110111	
120	78	D 8	TBN	8 8	8 2	01111000	
121	79	D 8 1	TBF	9 8	9 2	01111001	
122	7A	8 2	SBN	:	:	01111010	:
123	7B	8 21	SBF	#	#	01111011	#
124	7C	84	MVI	@	@	01111100	@
125	7D	84 1	CLI	'	'	01111101	'
126	7E	842		=	=	01111110	=
127	7F	8421		"	"	01111111	"
128	80	DC			3	10000000	
129	81	CBA 1		A 4	A 1	10000001	
130	82	CBA 2		B 4	B 1	10000010	
131	83	CBA 21		C 4	C 1	10000011	
132	84	CBA 4	ZAZ	D 4	D 1	10000100	
133	85	CBA 4 1		E 4	E 1	10000101	
134	86	CBA 42	AZ	F 4	F 1	10000110	
135	87	CBA 421	SZ	G 4	G 1	10000111	
136	88	CBA8	MVX	H 4	H 1	10001000	
137	89	CBA8 1		I 4	I 1	10001001	
138	8A	DCBA8 2	ED	c @	c 3	10001010	
139	8B	DCBA8 21	ITC	. @	. 3	10001011	
140	8C	DCBA84	MVC	< @	< 3	10001100	
141	8D	DCBA84 1	CLC	(@	(3	10001101	
142	8E	DCBA842	ALC	+ @	+ 3	10001110	
143	8F	DCBA8421	SLC	I @	I 3	10001111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
144	90	CBA		} 4	} 1	10010000	
145	91	CB 1		J 4	J 1	10010001	
146	92	CB 2		K 4	K 1	10010010	
147	93	CB 21		L 4	L 1	10010011	
148	94	CB 4	ZAZ	M 4	M 1	10010100	
149	95	CB 4 1		N 4	N 1	10010101	
150	96	CB 42	AZ	O 4	O 1	10010110	
151	97	CB 421	SZ	P 4	P 1	10010111	
152	98	CB 8	MVX	Q 4	Q 1	10011000	
153	99	CB 8 1		I 4	I 1	10011001	
154	9A	DCB 8 2	ED	! @	! 3	10011010	
155	9B	DCB 8 21	ITC	$ @	$ 3	10011011	
156	9C	DCB 84	MVC	* @	* 3	10011100	
157	9D	DCB 84 1	CLC	) @	) 3	10011101	
158	9E	DCB 842	ALC	; @	; 3	10011110	
159	9F	DCB 8421	SLC	¬ @	¬ 3	10011111	
160	A0	DCB		– @	– 3	10100000	
161	A1	DC A 1		/ @	/ 3	10100001	
162	A2	C A 2		S 4	S 1	10100010	
163	A3	C A 21		T 4	T 1	10100011	
164	A4	C A 4	ZAZ	U 4	U 1	10100100	
165	A5	C A 4 1		V 4	V 1	10100101	
166	A6	C A 42	AZ	W 4	W 1	10100110	
167	A7	C A 421	SZ	X 4	X 1	10100111	
168	A8	C A8	MVX	Y 4	Y 1	10101000	
169	A9	C A8 1		Z 4	Z 1	10101001	
170	AA	DC A8 2	ED	& @	& 3	10101010	
171	AB	DC A8 21	ITC	, @	, 3	10101011	
172	AC	DC A84	MVC	% @	% 3	10101100	
173	AD	DC A84 1	CLC	— @	— 3	10101101	
174	AE	DC A842	ALC	> @	> 3	10101110	
175	AF	DC A8421	SLC	? @	? 3	10101111	
176	B0	C A	SNS	0 4	0 1	10110000	
177	B1	C 1	LIO	1 4	1 1	10110001	
178	B2	C 2		2 4	2 1	10110010	
179	B3	C 21		3 4	3 1	10110011	
180	B4	C 4	ST	4 4	4 1	10110100	
181	B5	C 4 1	L	5 4	5 1	10110101	
182	B6	C 42	A	6 4	6 1	10110110	
183	B7	C 421		7 4	7 1	10110111	
184	B8	C 8	TBN	8 4	8 1	10111000	
185	B9	C 8 1	TBF	9 4	9 1	10111001	
186	BA	DC 8 2	SBN	: @	: 3	10111010	
187	BB	DC 8 21	SBF	# @	# 3	10111011	
188	BC	DC 84	MVI	@ @	@ 3	10111100	
189	BD	DC 84 1	CLI	' @	' 3	10111101	
190	BE	DC 842		= @	= 3	10111110	
191	BF	DC 8421		" @	" 3	10111111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
192	C0	D	BC	& 8	& 2	11000000	
193	C1	BA 1	TIO	A	A	11000001	A
194	C2	BA 2	LA	B	B	11000010	B
195	C3	BA 21		C	C	11000011	C
196	C4	BA 4		D	D	11000100	D
197	C5	BA 4 1		E	E	11000101	E
198	C6	BA 42		F	F	11000110	F
199	C7	BA 421		G	G	11000111	G
200	C8	BA8		H	H	11001000	H
201	C9	BA8 1		I	I	11001001	I
202	CA	D BA8 2		¢ 8	¢ 2	11001010	
203	CB	D BA8 21		. 8	. 2	11001011	
204	CC	D BA84		< 8	< 2	11001100	
205	CD	D BA84 1		(8	(2	11001101	
206	CE	D BA842		+ 8	+ 2	11001110	
207	CF	D BA8421		| 8	| 2	11001111	
208	D0	BA	BC	}	}	11010000	}
209	D1	B 1	TIO	J	J	11010001	J
210	D2	B 2	LA	K	K	11010010	K
211	D3	B 21		L	L	11010011	L
212	D4	B 4		M	M	11010100	M
213	D5	B 4 1		N	N	11010101	N
214	D6	B 42		O	O	11010110	O
215	D7	B 421		P	P	11010111	P
216	D8	B 8		Q	Q	11011000	Q
217	D9	B 8 1		R	R	11011001	R
218	DA	D B 8 2		! 8	! 2	11011010	
219	DB	D B 8 21		$ 8	$ 2	11011011	
220	DC	D B 84		* 8	* 2	11011100	
221	DD	D B 84 1		) 8	) 2	11011101	
222	DE	D B 842		; 8	; 2	11011110	
223	DF	D B 8421		¬ 8	¬ 2	11011111	
224	E0	D B	BC	- 8	- 2	11100000	
225	E1	D A 1	TIO	/ 8	/ 2	11100001	
226	E2	A 2	LA	S	S	11100010	S
227	E3	A 21		T	T	11100011	T
228	E4	A 4		U	U	11100100	U
229	E5	A 4 1		V	V	11100101	V
230	E6	A 42		W	W	11100110	W
231	E7	A 421		X	X	11100111	X
232	E8	A8		Y	Y	11101000	Y
233	E9	A8 1		Z	Z	11101001	Z
234	EA	D A8 2		¢ 8	¢ 2	11101010	
235	EB	D A8 21		, 8	, 2	11101011	
236	EC	D A84		% 8	% 2	11101100	
237	ED	D A84 1		_ 8	_ 2	11101101	
238	EE	D A842		> 8	> 2	11101110	
239	EF	D A8421		? 8	? 2	11101111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
240	F0	A	HPL	0	0	11110000	0
241	F1	1	APL	1	1	11110001	1
242	F2	2	JC	2	2	11110010	2
243	F3	21	SIO	3	3	11110011	3
244	F4	4		4	4	11110100	4
245	F5	4 1		5	5	11110101	5
246	F6	42		6	6	11110110	6
247	F7	421		7	7	11110111	7
248	F8	8		8	8	11111000	8
249	F9	8 1		9	9	11111001	9
250	FA	D 8 2		: 8	: 2	11111010	
251	FB	D 8 21		# 8	# 2	11111011	
252	FC	D 84		@ 8	@ 2	11111100	
253	FD	D 84 1		' 8	' 2	11111101	
254	FE	D 842		= 8	= 2	11111110	
255	FF	D 8421		" 8	" 2	11111111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

*Tier 3 character addition table

Tier 3 card bits required by tier 1 character \ Tier 3 card bits required by tier 2 character	0	1	2	3 (1+2 bits)
	4	5 (4+1 bits)	6 (4+2 bits)	7 (4+2+1 bits)
	8	9 (8+1 bits)	: (8+2 bits)	# (8+2+1 bits)
	@ (4+8 bits)	' (8+4+1 bits)	= (8+4+2 bits)	" (8+4+2+1 bits)

5424 MFCU TYPEWHEEL PATTERN

Position	Char	Hex	BCD
1	—	This Char not Used	
2	1	F1	1
3	2	F2	2
4	3	F3	21
5	4	F4	4
6	5	F5	4 1
7	6	F6	42
8	7	F7	421
9	8	F8	8
10	9	F9	8 1
11	:	7A	8 2
12	#	7B	8 21
13	@	7C	84
14	'	7D	84 1
15	=	7E	842
16	"	7F	8421
17	Ø	F0	A
18	/	61	A 1
19	S	E2	A 2
20	T	E3	A 21
21	U	E4	A 4
22	V	E5	A 4 1
23	W	E6	A 42
24	X	E7	A 421
25	Y	E8	A8
26	Z	E9	A8 1
27	&	50	A8 2
28	,	6B	A8 21
29	%	6C	A84
30	–	6D	A84 1
31	>	6E	A842
32	?	6F	A8421

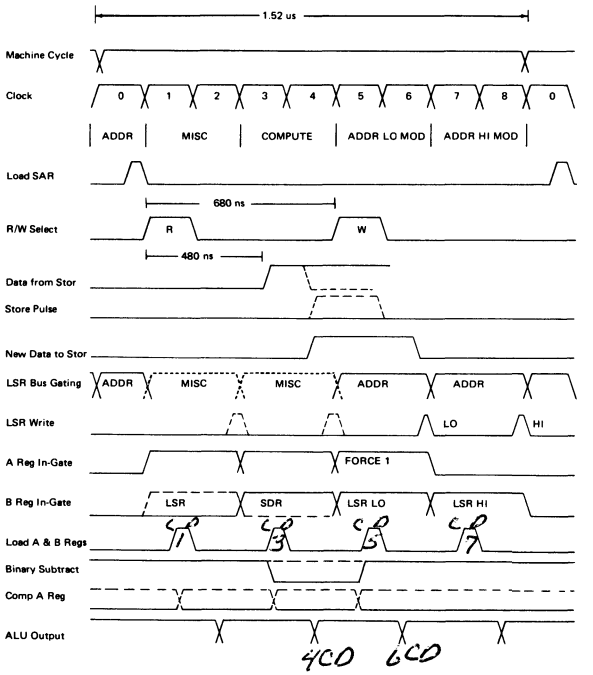
Position	Char	Hex	BCD
33	–	60	B
34	J	D1	B 1
35	K	D2	B 2
36	L	D3	B 21
37	M	D4	B 4
38	N	D5	B 4 1
39	O	D6	B 42
40	P	D7	B 421
41	Q	D8	B 8
42	R	D9	B 8 1
43	!	5A	B 8 2
44	$	5B	B 8 21
45	*	5C	B 84
46	)	5D	B 84 1
47	;	5E	B 842
48	¬	5F	B 8421
49	}	DO	BA
50	A	C1	BA 1
51	B	C2	BA 2
52	C	C3	BA 21
53	D	C4	BA 4
54	E	C5	BA 4 1
55	F	C6	BA 42
56	G	C7	BA 421
57	H	C8	BA8
58	I	C9	BA8 1
59	Ç	4A	BA8 2
60	.	4B	BA8 21
61	<	4C	BA84
62	(	4D	BA84 1
63	+	4E	BA842
64	|	4F	BA8421

5203 CHAIN PATTERN

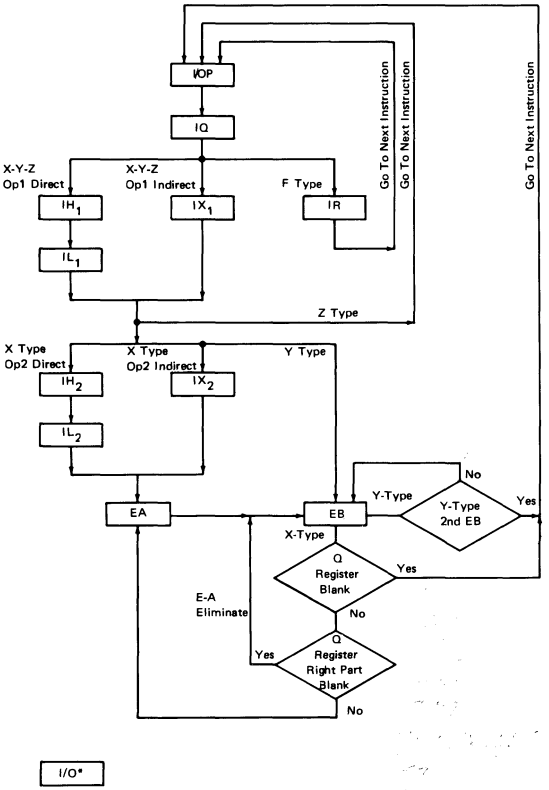
Hex Character	Chain Character	Chain Position	BCD CODE B	A	8	4	2	1
F1	1	1						1
F2	2	2					2	
F3	3	3					2	1
F4	4	4				4		
F5	5	5				4		1
F6	6	6				4	2	
F7	7	7				4	2	1
F8	8	8			8			
F9	9	9			8			1
F0	0	10			8		2	
7B	#	11			8		2	1
7C	@	12			8	4		
61	/	13		A				1
E2	S	14		A			2	
E3	T	15		A			2	1
E4	U	16		A		4		
E5	V	17		A		4		1
E6	W	18		A		4	2	
E7	X	19		A		4	2	1
E8	Y	20		A	8			
E9	Z	21		A	8			1
50	¢	22		A	8		2	
6B	,	23		A	8		2	1
6C	%	24		A	8	4		
D1	J	25	B					1
D2	K	26	B				2	
D3	L	27	B				2	1
D4	M	28	B			4		
D5	N	29	B			4		1
D6	O	20	B			4	2	
D7	P	31	B			4	2	1
D8	Q	32	B		8			
D9	R	33	B		8			1
60	–	34	B		8		2	
5B	$	35	B		8		2	1
5C	*	36	B		8	4		
C1	A	37	B	A				1
C2	B	38	B	A			2	
C3	C	39	B	A			2	1
C4	D	40	B	A		4		
C5	E	41	B	A		4		1
C6	F	42	B	A		4	2	
C7	G	43	B	A		4	2	1
C8	H	44	B	A	8			
C9	I	45	B	A	8			1
4E	+	46	B	A	8		2	
4B	.	47	B	A	8		2	1
7D	'	48			8	4		1

LC ARRAY

CPU BASIC TIMINGS



CPU CYCLE PATTERNS



* Can be performed between any of the 11 above cycles.

CPU CYCLES

IOp	=	Op code moved from storage to Op code register
IQ	=	Q code moved from storage to Q register
IR	=	Third instruction cycle when instruction uses no addresses
IX1	=	Establishes first operand address in BAR when first operand is indirectly addressed
IH1	=	Establishes high order byte of first operand in the high order byte of BAR when first operand is directly addressed
IL1	=	Establishes low order byte of first operand in the low order byte of BAR when first operand is directly addressed
IX2	=	Establishes second operand address in the AAR when the second operand is indirectly addressed
IH2	=	Establishes the high order byte of second operand in the AAR when the second operand is directly addressed
IL2	=	Establishes the low order byte of second operand in the AAR when the second operand is directly addressed
EA	=	Moves a byte of the second operand from storage, operates on it and returns it to storage
EB	=	Moves a byte of the first operand from storage, operates on it and returns it to storage

INSTRUCTION CYCLE PATTERNS

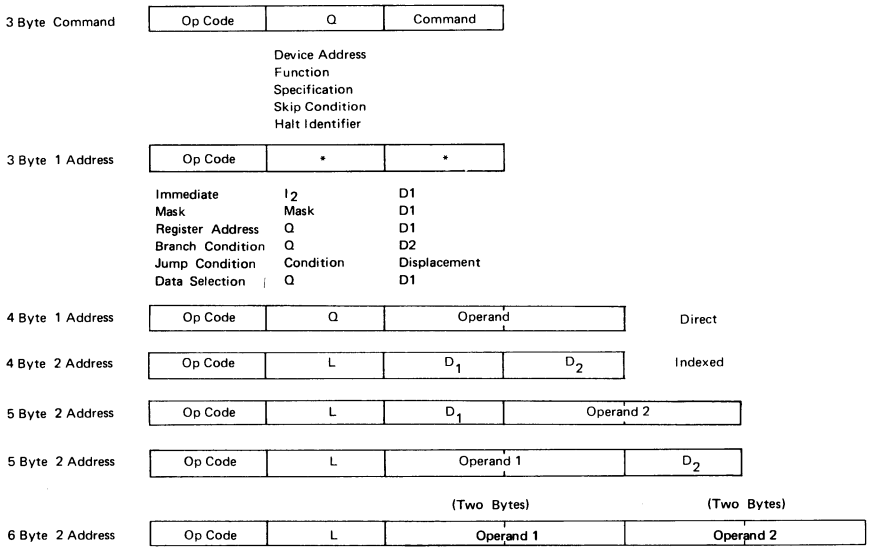
Op	Mnem	Op	Q	R	X_1	H_1	L_1	X_2	H_2	L_2	A	B
04	ZAZ	x	x			x	x		x	x	x	x
06	AZ	x	x			x	x		x	x	x	x
07	SZ	x	x			x	x		x	x	x	x
08	MVX	x	x			x	x		x	x	x	x
0A	ED	x	x			x	x		x	x	x	x
0B	ITC	x	x			x	x		x	x	x	x
0C	MVC	x	x			x	x		x	x	x	x
0D	CLC	x	x			x	x		x	x	x	x
0E	ALC	x	x			x	x		x	x	x	x
0F	SLC	x	x			x	x		x	x	x	x
14	ZAZ	x	x			x	x	x			x	x
16	AZ	x	x			x	x	x			x	x
17	SZ	x	x			x	x	x			x	x
18	MVX	x	x			x	x	x			x	x
1A	ED	x	x			x	x	x			x	x
1B	ITC	x	x			x	x	x			x	x
1C	MVC	x	x			x	x	x			x	x
1D	CLC	x	x			x	x	x			x	x
1E	ALC	x	x			x	x	x			x	x
1F	SLC	x	x			x	x	x			x	x
24	ZAZ	x	x			x	x	x			x	x
26	AZ	x	x			x	x	x			x	x
27	SZ	x	x			x	x	x			x	x
28	MVX	x	x			x	x	x			x	x
2A	ED	x	x			x	x	x			x	x
2B	ITC	x	x			x	x	x			x	x
2C	MVC	x	x			x	x	x			x	x
2D	CLC	x	x			x	x	x			x	x
2E	ALC	x	x			x	x	x			x	x
2F	SLC	x	x			x	x	x			x	x
30	SNS	x	x			x	x					x
31	LIO	x	x			x	x					x
34	ST	x	x			x	x					x
35	L	x	x			x	x					x
36	A	x	x			x	x					x
38	TBN	x	x			x	x					x
39	TBF	x	x			x	x					x
3A	SBN	x	x			x	x					x
3B	SBF	x	x			x	x					x
3C	MVI	x	x			x	x					x
3D	CLI	x	x			x	x					x
44	ZAZ	x	x		x				x	x	x	x
46	AZ	x	x		x				x	x	x	x
47	SZ	x	x		x				x	x	x	x
48	MVX	x	x		x				x	x	x	x
4A	ED	x	x		x				x	x	x	x
4B	ITC	x	x		x				x	x	x	x
4C	MVC	x	x		x				x	x	x	x
4D	CLC	x	x		x				x	x	x	x
4E	ALC	x	x		x				x	x	x	x
4F	SLC	x	x		x				x	x	x	x
54	ZAZ	x	x		x			x			x	x
56	AZ	x	x		x			x			x	x
57	SZ	x	x		x			x			x	x
58	MVX	x	x		x			x			x	x

INSTRUCTION CYCLE PATTERNS (continued)

Op	Mnem	Op	Q	R	X_1	H_1	L_1	X_2	H_2	L_2	A	B
5A	ED	x	x		x			x			x	x
5B	ITC	x	x		x			x			x	x
5C	MVC	x	x		x			x			x	x
5D	CLC	x	x		x			x			x	x
5E	ALC	x	x		x			x			x	x
5F	SLC	x	x		x			x			x	x
64	ZAZ	x	x		x			x			x	x
66	AZ	x	x		x			x			x	x
67	SZ	x	x		x			x			x	x
68	MVX	x	x		x			x			x	x
6A	ED	x	x		x			x			x	x
6B	ITC	x	x		x			x			x	x
6C	MVC	x	x		x			x			x	x
6D	CLC	x	x		x			x			x	x
6E	ALC	x	x		x			x			x	x
6F	SLC	x	x		x			x			x	x
70	SNS	x	x		x							x
71	LIO	x	x		x							x
74	ST	x	x		x							x
75	L	x	x		x							x
76	A	x	x		x							x
78	TBN	x	x		x							x
79	TBF	x	x		x							x
7A	SBN	x	x		x							x
7B	SBF	x	x		x							x
7C	MVI	x	x		x							x
7D	CLI	x	x		x							x
84	ZAZ	x	x		x				x	x	x	x
86	AZ	x	x		x				x	x	x	x
87	SZ	x	x		x				x	x	x	x
88	MVX	x	x		x				x	x	x	x
8A	ED	x	x		x				x	x	x	x
8B	ITC	x	x		x				x	x	x	x
8C	MVC	x	x		x				x	x	x	x
8D	CLC	x	x		x				x	x	x	x
8E	ALC	x	x		x				x	x	x	x
8F	SLC	x	x		x				x	x	x	x
94	ZAZ	x	x		x			x			x	x
96	AZ	x	x		x			x			x	x
97	SZ	x	x		x			x			x	x
98	MVX	x	x		x			x			x	x
9A	ED	x	x		x			x			x	x
9B	ITC	x	x		x			x			x	x
9C	MVC	x	x		x			x			x	x
9D	CLC	x	x		x			x			x	x
9E	ALC	x	x		x			x			x	x
9F	SLC	x	x		x			x			x	x
A4	ZAZ	x	x		x			x			x	x
A6	AZ	x	x		x			x			x	x
A7	SZ	x	x		x			x			x	x
A8	MVX	x	x		x			x			x	x
AA	ED	x	x		x			x			x	x
AB	ITC	x	x		x			x			x	x
AC	MVC	x	x		x			x			x	x

INSTRUCTION CYCLE PATTERNS (continued)

Op	Mnem	Op	Q	R	X_1	H_1	L_1	X_2	H_2	L_2	A	B
AD	CLC	x	x		x			x			x	x
AE	ALC	x	x		x			x			x	x
AF	SLC	x	x		x			x			x	x
B0	SNS	x	x		x							x
B1	LIO	x	x		x							x
B4	ST	x	x		x							x
B5	L	x	x		x							x
B6	A	x	x		x							x
B8	TBM	x	x		x							x
B9	TBF	x	x		x							x
BA	SBN	x	x		x							x
BB	SBF	x	x		x							x
BC	MVI	x	x		x							x
BD	CLI	x	x		x							x
C0	BC	x	x			x	x					
C1	TIO	x	x			x	x					
C2	LA	x	x			x	x					
D0	BC	x	x		x							
D1	TIO	x	x		x							
D2	LA	x	x		x							
E0	BC	x	x		x							
E1	TIO	x	x		x							
E2	LA	x	x		x							
F0	HPL	x	x	x								
F1	APL	x	x	x								
F2	JC	x	x	x								
F3	SIO	x	x	x								


3 Byte Command
Op Code
Q
Command
Device Address
Function
Specification
Skip Condition
Halt Identifier
3 Byte 1 Address
Op Code
*
*
Immediate
Mask
Register Address
Branch Condition
Jump Condition
Data Selection
I2
Mask
Q
Q
Condition
Q
D1
D1
D1
D2
Displacement
D1
4 Byte 1 Address
Op Code
Q
Operand
Direct
4 Byte 2 Address
Op Code
L
D1
D2
Indexed
5 Byte 2 Address
Op Code
L
D1
Operand 2
5 Byte 2 Address
Op Code
L
Operand 1
D2
(Two Bytes)
(Two Bytes)
6 Byte 2 Address
Op Code
L
Operand 1
Operand 2

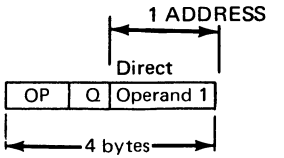
	Mnem	Op	Q	Operands	Comments
Two Address Instruction	ZAZ	4	L_1L_2		Zero and add zoned
	AZ	6	L_1L_2		Add zoned decimal
	SZ	7	L_1L_2		Subtract zoned decimal
	MVX	8			Move hex characters
	ED	A	L_1		Edit
	ITC	B	L_1		Insert and test characters
	MVC	C	L		Move characters
	CLC	D	L		Compare logical characters
	ALC	E	L		Add logical characters
	SLC	F	L		Subtract logical characters
		0		Op1 Op2	Op1 direct, Op2 direct
		1		Op1 Op2	Op1 direct, Op2 indexed by XR1
		2		Op1 Op2	Op1 direct, Op2 indexed by XR2
		4		Op1 Op2	Op1 indexed by XR1, Op2 direct
		5		Op1 Op2	Op1 indexed by XR1, Op2 indexed by XR1
		6		Op1 Op2	Op1 indexed by XR1, Op2 indexed by XR2
		8		Op1 Op2	Op1 indexed by XR2, Op2 direct
		9		Op1 Op2	Op1 indexed by XR2, Op2 indexed by XR1
		A		Op1 Op2	Op1 indexed by XR2, Op2 indexed by XR2

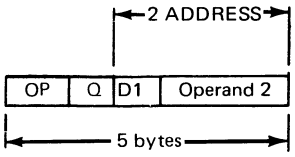
One Address Instruction (Non-Branch)	SNS	0	DA|M|N				Sense I/O
	LIO	1	DA|M|N				Load I/O
	ST	4	Reg				Store register
	L	5	Reg				Load register
	A	6	Reg				Add to register
	TBN	8	Mask				Test bits on
	TBF	9	Mask				Test bits off
	SBN	A	Mask				Set bits on
	SBF	B	Mask				Set bits off
	MVI	C	I_2				Move logical immediate
	CLI	D	I_2				Compare logical immediate
		3		Op1 Addr			Op1 direct
		7		Op1			Op1 indexed by XR1
		B		Op1			Op1 indexed by XR2
One Address Instruction (Branch)	BC	0	Cond.				Branch on condition
	TIO	1	DA|M|N				Test I/O and branch
	LA	2	Bit 6-XR2 Bit 7-XR1				Load address
		C		Op 1 Addr			Op 1 direct
		D		Op 1			Op 1 indexed by XR1
		E		Op 1			Op 1 indexed by XR2
Command Instruction	HPL	F0	Tens	Unit			Halt program level
	APL	F1	DA|M|N	N U			Advance program level
	JC	F2	Cond.	Number of bytes to jump			Jump on condition
	SIO	F3	DA|M|N	Control			Start I/O

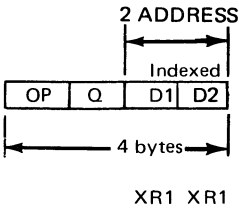
INSTRUCTION FORMAT REFERENCE

OP	MNEMONIC	TYPE
04	ZAZ	
06	AZ	2 ADDRESS
07	SZ	
08	MVX	Direct
0A	ED	OP | Q | Operand 1 | Operand 2
0B	ITC	
0C	MVC	6 bytes
0D	CLC	
0E	ALC	
0F	SLC	
14	ZAZ	
16	AZ	2 ADDR
17	SZ	
18	MVX	Direct Indexed
1A	ED	OP | Q | Operand 1 | D2
1B	ITC	
1C	MVC	5 bytes
1D	CLC	
1E	ALC	XR1
1F	SLC	
24	ZAZ	
26	AZ	2 ADDR
27	SZ	
28	MVX	Direct Indexed
2A	ED	OP | Q | Operand 1 | D2
2B	ITC	
2C	MVC	5 bytes
2D	CLC	
2E	ALC	XR2
2F	SLC	

OP	MNEMONIC	TYPE
30	SNS	
31	LIO	
34	ST	
35	L	
36	A	
38	TBN	
39	TBF	
3A	SBN	
3B	SBF	
3C	MVI	
3D	CLI	
44	ZAZ	
46	AZ	
47	SZ	
48	MVX	
4A	ED	
4B	ITC	
4C	MVC	
4D	CLC	
4E	ALC	
4F	SLC	
54	ZAZ	
56	AZ	
57	SZ	
58	MVX	
5A	ED	
5B	ITC	
5C	MVC	
5D	CLC	
5E	ALC	
5F	SLC	

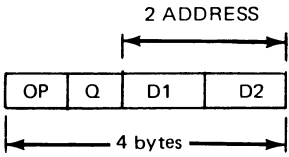


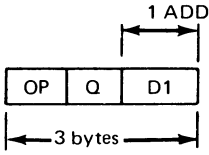


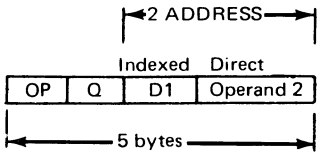


INSTRUCTION FORMAT REFERENCE (continued)

OP	MNEMONIC	TYPE
64	ZAZ	
66	AZ	
67	SZ	
68	MVX	
6A	ED	
6B	ITC	
6C	MVC	
6D	CLC	
6E	ALC	
6F	SLC	
70	SNS	
71	LIO	
74	ST	
75	L	
76	A	
78	TBN	
79	TBF	
7A	SBN	
7B	SBF	
7C	MVI	
7D	CLI	
84	ZAZ	
86	AZ	
87	SZ	
88	MVX	
8A	ED	
8B	ITC	
8C	MVC	
8D	CLC	
8E	ALC	
8F	SLC	





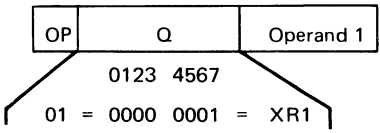


OP	MNEMONIC	TYPE
94	ZAZ	
96	AZ	2 ADDRESS
97	SZ	
98	MVX	Indexed
9A	ED	OP Q D1 D2
9B	ITC	
9C	MVC	4 bytes
9D	CLC	
9E	ALC	XR2 XR1
9F	SLC	
A4	ZAZ	
A6	AZ	2 ADDRESS
A7	SZ	
A8	MVX	Indexed
AA	ED	OP Q D1 D2
AB	ITC	
AC	MVC	4 bytes
AD	CLC	
AE	ALC	XR2 XR2
AF	SLC	
B0	SNS	
B1	LIO	1 ADDRESS
B4	ST	
B5	L	Indexed
B6	A	OP Q D1
B8	TBN	
B9	TDF	3 bytes
BA	SBN	
BB	SBF	
BC	MVI	XR2
BD	CLI	

INSTRUCTION FORMAT REFERENCE (continued)

OP	MNEMONIC	TYPE
C0	BC	Direct
C1	TIO	OP Q Address
C2	LA	4 bytes
D0	BC	
D1	TIO	OP Q D2 +XR1
D2	LA	3 bytes
E0	BC	
E1	TIO	OP Q D2 +XR2
E2	LA	3 bytes
F0	HPL	
F1	APL	
F2	JC	OP Q R
F3	SIO	3 bytes

LOAD & STORE REGISTER Q CODES



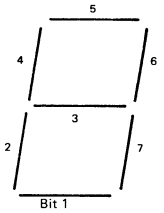
01	=	0000 0001	=	XR1
02	=	0000 0010	=	XR2
04	=	0000 0100	=	PSR
08	=	0000 1000	=	ARR
10	=	0001 0000	=	IAR
20	=	0010 0000	=	P1 - IAR
40	=	0100 0000	=	P2 - IAR
80	=	1000 0000	=	IAR - 0
C0	=	1100 0000	=	IAR - 1
A0	=	1010 0000	=	IAR - 2
90	=	1001 0000	=	IAR - 3
88	=	1000 1000	=	IAR - 4

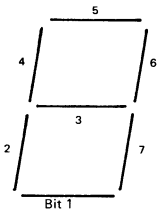
HALT IDENTIFIERS

HALT Identifiers

F0	TENS	UNITS

Hex Value	Character Displayed
00 Blank	
02 Quote	
03	
07	
1B	
10 Dash	
3B	
3C	
3E	
3F	
57	
5D	
5F	
63	
68	
6B	
6C	
6F	
76	
7C	
7D	
7F	

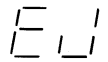




EXAMPLE:

F0	7C	63

DISPLAYS



Note: Not the same as 5475 keyboard indicators - See 5475 LIO.

CONDITION REGISTER SETTINGS

Binary Value	8	4	2	1	8	4	2	1
Bits	0	1	2	3	4	5	6	7
Meaning			*B0	Test False	**D0	HI	LO	EQ
DECIMAL								
ADD Decimal			–	–	overflow	> zero	< zero	zero
SUB Decimal			–	–	overflow	> zero	< zero	zero
ZERO & ADD			–	–		> zero	< zero	zero
LOGICAL								
ADD Logical			overflow	–	–	Carry	No Carry	zero
SUB Logical			–	–	–	1>2	1<2	zero
COMPARE			–	–	–	1>2	1<2	EQ
CLI						1>I	1<I	1 = I
EDIT (second operand)			–	–	–	> zero	< zero	zero
Test Bits ON			–	Note 1	–	–	–	–
Test Bits OFF			–	Note 2	–	–	–	–
BRANCH ON CONDITION	X		–	Note 3	–	–	–	–

When ONE, branch if any of the tested bits are ON
When ZERO, branch when all the tested bits are OFF

*B0 = Binary overflow
**D0 = Decimal overflow

1. Selected bits are not all one.
2. Selected bits are not all zero
3. Turn off if tested.

LOCAL STORE REGISTERS

BASE SYSTEM

HIGH	LOW	LSR Acronym
Program level 1 instruction address register		P1-IAR
Program level 1 address recall register		P1-ARR
Operand 2 address register		AAR
Spare		
Program level 1 index register 1		P1-XR1
Length count recall register	Condition recall register	P1-PSR
Operand 1 address register		BAR
MFCU print data address register		MPTAR
Program level 1 index register 2		P1-XR2
Line printer data address register		LPDAR
Line printer image address register		LPIAR
MFCU punch data address register		MPCAR
MFCU read address register		MRDAR
Length count registers	Data recall register	LCR DRR
Interrupt level 1 instruction address register		IAR-1
Interrupt level 1 address recall register		ARR-1

FEATURE 1

HIGH	LOW	LSR Acronym
Program level 2 instruction address register		P2-IAR
Program level 2 address recall register		P2-ARR
Bi-sync comm adapter address register		BSCAR
Serial I/O channel address register		SIAR
Program level 2 status register		P2-PSR
Interrupt level 4 instruction address register		IAR-4
Interrupt level 4 address recall register		ARR-4
Disk file control address register		DFCR
Program level 2 index register 2		P2-XR2
Spare		Spare
Interrupt level 2 instruction address register		IAR-2
Interrupt level 2 address recall register		ARR-2
Disk file data address register		DFDR
Program level 2 index register 1		P2-XR1
Interrupt level 0, instruction address register		IAR-0
Interrupt level 0 address recall register		ARR-0

Cycle Steal Request Priority Assignments

Priority*	CPU Clock at Attmt	CPU Clock	Request Bit Line	Priority Assignment P 0 1 2 3 4 5 6 7	Device
1	0	1	7	1 0 0 1 0 0 0 0 1	File Seek
2	0	1	6	1 0 0 1 0 0 0 1 0	Unassigned
3	0	1	5	1 0 0 1 0 0 1 0 0	Unassigned
4	0	1	4	1 0 0 1 0 1 0 0 0	Unassigned
5	0	1	3	1 0 0 1 1 0 0 0 0	Unassigned
6	2	3	7	1 0 1 0 0 0 0 0 1	Unassigned
7	2	3	6	1 0 1 0 0 0 0 1 0	Unassigned
8	2	3	5	1 0 1 0 0 0 1 0 0	Unassigned
9	2	3	4	1 0 1 0 0 1 0 0 0	MFCU Prt
10	2	3	3	1 0 1 0 1 0 0 0 0	Custom Sys
11	4	5	7	1 1 0 0 0 0 0 0 1	Unassigned
12	4	5	6	1 1 0 0 0 0 0 1 0	Unassigned
13	4	5	5	1 1 0 0 0 0 1 0 0	Unassigned
14	4	5	4	1 1 0 0 0 1 0 0 0	MFCU Rd-Pch
15	4	5	3	1 1 0 0 1 0 0 0 0	BSCA
16	6	7	7	0 0 0 0 0 0 0 0 1	Unassigned
17	6	7	6	0 0 0 0 0 0 0 1 0	SIOC
18	6	7	5	0 0 0 0 0 0 1 0 0	5203 Printer
19	6	7	4	0 0 0 0 0 1 0 0 0	Unassigned
20	6	7	3	0 0 0 0 1 0 0 0 0	File Rd/Wr

*Priority is from lowest to highest

I/O ATTACHMENT CONDITION					I/O Condition A	I/O Condition B	CPU REACTION
I - Q Cycle of any I/O Instruction	Incorrect DBO Parity				1	1	Processor checks stop with channel DBO check light on
	Correct DBO Parity	Q Byte not Correct			0	0	Processor check stop with Q byte invalid check light on
		Correct Q Byte	SNS Instruction		0	1	Proceed to next sequential instr
			SIO or LIO Instr	Reject Instr	1	0	Retry I/O instruction
				Accept Instr	0	1	Proceed to next sequential instr
			TIO or APL Instr	Condition not Met	0	1	Proceed to next sequential instr
				Condition Met	1	0	Branch to effective address
SIO I-R, LIO E-B, & I/O Cycles	INCORRECT DBO PARITY				1	1	Processor check stop with channel DBO check light on
	CORRECT DBO PARITY				0	0	Continue as normal

TEST I/O AND BRANCH (TIO) INSTRUCTION FORMATS

Op Code	Q Code			Control Code	
	DA	M	N		
0 7	8 11	12	13 15	16	
C1					Direct addressing – Operand 1 = 2 bytes
D1					Indexed by XR-1 – Operand 1 = 1 byte
E1					Indexed by XR-2 – Operand 1 = 1 byte
	1111				Device address MFCU (F)
		0			Primary
		1			Secondary
			000		Feed not ready or error
5424 MFCU			001		Read feed busy (condition 1)
			010		Punch data busy (condition 2)
			011		Condition 1 or 2
			100		Print data busy (condition 4)
			101		Condition 1 or 4
			110		Condition 2 or 4
			111		Condition 1, 2 or 4
				xxxx xxxx	Branch to address if condition met Op codes D1 and E1 are indexed
	1110				Device address printer (E)
		0			Left carriage
		1			Right carriage
			000		Not ready
5203 Printer			001		Invalid
			010		Print buffer busy
			011		Invalid
			100		Carriage busy
			101		Invalid
			110		Printer busy
			111		Invalid
				xxxx xxxx	Branch to address if condition met Op codes D1 and E1 are indexed
5471	0001				Device address keyboard (1)
and 5475					Test I/O is invalid and will result in invalid Q byte processor check.
	1010				Device address disk drive 1 (A)
	1011				Device address disk drive 2 (B)
		0			Removable disk
		1			Fixed disk
5444 Disk			000		Not ready or error*
			010		Busy - Data transfer in process
			100		Scan found
			*		*Condition may vary depending on Disk drive selected - Refer to status byte
				xxxx xxxx	Branch to address if condition is met
	0000				Device address DPF (0)
		0			Must be zero
DPF			0xx		Program level 1
			1xx		Program level 2
			x00		Cancel program level — Tests setting of DPF switch
			x01		Load program level from MFCU — Tests setting of DPF switch
			x10		Load from console I/O — Tests setting of DPF switch
			*	xxxx xxxx	Branch to address if condition is met Op codes D1 and E1 are indexed

* Note: All other N codes invalid

TEST I/O AND BRANCH (TIO) INSTRUCTION FORMATS (continued)

Op Code	Q Code			Control Code	
	DA	M	N		
0 7	8 11	12	13 15	16	
C1					Direct Addressing – Operand 1 = 2 bytes
D1					Indexed by XR-1 – Operand 1 = 1 byte
E1					Indexed by SR-2 – Operand 1 = 1 byte
	0011				Device address SIOC (3)
		0			Must be zero
			000		Test for SIOC not ready
			010		Test for SIOC busy Note: All other N codes invalid
				xxxx xxxx	Branch to address if condition is met D1 and E1 are indexed
	1000				Device address BSCA (8)
		0			Must be zero
			000		Not ready / Unit check
			001		Op end interrupt
			010		Busy
BSCA			011		ITB interrupt
			100		Interrupt pending
			101		Invalid
			110		New data
			111		Invalid
				xxxx xxxx	Branch to address if condition is met D1 and E1 are indexed
	0101				Device address 1442 (5)
		0			Must be zero
			000		Test for 1442 not ready
1442			010		Test for 1442 busy Note: All other N codes invalid
				xxxx xxxx	Branch to address if condition is met D1 and E1 are indexed

LOAD I/O (LIO) INSTRUCTION FORMATS

Op Code	Q Code			Operand 1	
	DA	M	N		
0 7	8 11	12	13 15	16	
31					Direct addressing – Operand 1 = 2 bytes
71					Indexed by XR-1 – Operand 1 = 1 byte
B1					Indexed by XR-2 – Operand 1 = 1 byte
	1110				Device address line printer (E)
		0			M-bit is not used, a zero is preferred
5203 Printer			000		Load form length. One byte for each carriage
			100		Select line printer image address register
			110		Select line printer data address register
					Note: All other N codes invalid
	1111				Device address MFCU (F)
		0			Normal mode
5424 MFCU		1			Diagnostic mode
			100		MFCU print address register
			101		MFCU read address register
			110		MFCU punch address register
					Note: All other N codes invalid
	1010				Device address disk drive 1 (A)
5444 Disk	1011				Device address disk drive 2 (B)
		0			M-bit not used
			011		Diagnostic CE
			100		DFDR
			110		DFCR
					Note: All other N codes invalid
	0001				Device address keyboard (1)
5475 Keyboard		0	000		M and N must be zero

Data at operand Address-1								Data at operand 1 Address							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
							Prog 1 ID								Prog 2 ID
1	2	3	4	5	6	7		8	9	10	11	12	13	14	
Indicator 1								Indicator 2							

LOAD I/O (LIO) INSTRUCTION FORMATS (continued)

Op Code	Q Code			Operand 1	
	DA	M	N		
0 7	8 11	12	13 15	16	
31					Direct addressing—Operand 1 = 2 bytes
71					Indexed by XR-1—Operand 1 = 1 byte
B1					Indexed by XR-2—Operand 1 = 1 byte
SIOC	0011				Device address SIOC (3)
		0			Must be zero
			001		Load I/O function register
			010		Load SIOC length count register
			100		Load SIOC data address register
			101		Load data transfer register
					Note: All other N codes invalid.
5471 Printer Keyboard	0001				Device address printer keyboard (1)
		1			Select printer must be a 1, 0 is invalid. Storage address can be one byte or two bytes in length (direct addressed, or indexed). The character to be printed is loaded from the first operand address - 1. All other N codes invalid.
			000		Load EBCDIC character to be printed (N code must be zero)
BSCA	1000				Device address BSCA (8)
		0			Must be zero
			001		Stop address register
			010		Transition address register
			100		Current address register
			110		Current address register (not subject to busy)
					Note: All other N codes invalid.
1442	0101				Device address 1442 (5)
		0			Must be zero
			000		Load punch LCR
			100		Load 1442 DAR
					Note: All other N codes invalid.

START I/O (SIO) INSTRUCTION FORMATS

Op Code	Q Code			Control Code		
	DA	M	N			
0 7	8 11	12	13 15	16	23	
F3						
	1110					Device address printer (E)
		0				Left carriage is used (single feed carriage)
		1				Right carriage is used
			000			Space only
			001			Invalid
			010			Print followed by spacing
			011			Invalid
			100			Skip only
			101			Invalid
5203 Printer			110			Print followed by skip
			111			Invalid
				0000	0000	No space
				0000	0001	One space
				0000	0010	Double space
				0000	0011	Triple space
				0000	0001	Skip to line 1
				0000	0010	Skip to line 2
				↓↓↓↓	↓↓↓↓	↓ ↓
				0110	1111	Skip to line 110
				0111	0000	Skip to line 112
						A number greater than 3 is not permitted and will result in a space zero operation.
						A number greater than /00F0/ may result in a carriage runaway. 112 lines are the maximum length of a form (8 lines per inch).
	1111					Device Address MFCU (F)
		0				Primary card path is used
		1				Secondary card path is used
			000			Feed
			001			Read
			010			Punch feed
			011			Punch read
			100			Print feed
			101			Print read
			110			Punch print feed
5424 MFCU			111			Punch print read
				0		Printbuffer 1 is used
				1		Printbuffer 2 is used
				1		8 bit IPL read
				1		Print 4 lines
				x		Reserved
					x	Reserved
					000	No selection
					100	Select stacker 4
					101	Select stacker 1
					110	Select stacker 2
					111	Select stacker 3
	0001	0	0000			Device Address Keyboard, M and N must be zero
				1		Program numeric shift
				1		Program lower shift
				1		Turn error indicator on
					1	Restore key
5475 Keyboard					1	Unlock keyboard
					0	Disable interrupt
					1	Enable interrupt
					1	Turn off interrupt request

START I/C (SIO) INSTRUCTION FORMATS (continued)

Op Code	Q Code			Control Code		
	DA	M	N			
0 7	8 11	12	13 15	16	23	
F3						
	1000					Device address BSCA (8)
		0				Must be zero
			000			Control
			001			Receive
			010			Transmit and receive
			011			Receive initial
			100			Auto call
			101			Invalid
			110			Loop test
			111			Invalid
				1xxx	x	If a 1, bits 1, 2, 3, and 4 of control code are effective
BSCA				0xxx	x	If a 0, bits 1, 2, 3, and 4 of control code are disregarded
				1		Enable BSCA
				0		Disable BSCA
				1		Enable test mode
				0		Disable test mode
				1		Enable step mode
				0		Disable step mode
					x	Spare (no effect)
					1	Start two second timeout
					0	Cancel two second timeout
					1	Enable interrupt
					0	Disable interrupt
					1	Reset interrupt request
					0	No action
						Note: The control code is effective with every "N" code function except that the start two second timeout must be used only with the control function ("N" = 000).
	0001					Device address - printer keyboard - (1)
		0				Select keyboard
			000			Must be zero – All other N codes invalid
				00xx	0xxx	Zero indicates unused position - Must be zero
				1		Turn on request pending indicator
				0		Turn off request pending indicator
				1		Turn on proceed indicator
				0		Turn off proceed indicator
5471					1	Enable request key interrupts
Printer					0	Disable request key interrupts
Key-					1	Enable data key interrupts
board					0	Disable data key interrupts
					1	Reset request or data key interrupts
		1				Select printer
			000			Must be zero – All other N codes invalid
				1		Start print
				0		Don't print
				1		Start carrier return (and index)
				0		Don't carrier return
				1		Force a printer feedback switch response
				1		Force a printer long function switch response
					0	Not used - Must be zero
					1	Enable printer interrupt
					0	Disable printer interrupt
					1	Degate printer magnets
					1	Reset printer interrupt

START I/O (SIO) INSTRUCTION FORMATS (continued

Op Code	Q Code			Control Code			
	DA	M	N				
0 7	8 11	12	13 15	16		23	
F3							
	1010						Device address disk drive 1 (A)
	1011						Device address disk drive 2 (B)
		0					Removable disk
5444		1					Fixed disk
Disk			000	0000	0000		Control - Seek
			001	0000	0000		Read - Data
			001	0000	0001		Read - Identifier
			001	0000	0010		Read - Diagnostic
			001	0000	0011		Read - Verify
			010	0000	0000		Write - Data
			010	0000	0001		Write - Identifier
			011	0000	0000		Scan - Equal
			011	0000	0001		Scan - Low or equal
			011	0000	0010		Scan - High or equal
							Note: 1. Bits 16-21 are not used by the attachment 2. All other N codes invalid.
	0011						Device address SIOC (3)
		0					Not used - A zero is preferred
			000	0000	0001		Reset interrupt request
			000	0000	0010		Enable interrupt ability
			000	0000	0100		Reset interrupt ability
			000	0000	1000		Remove SIOC from busy state
			000	0001	0000		Set interrupt request
			001	0000	0000		Read I/O device
			010	0000	0000		Write I/O device
SIOC			011				I/O Control 1
				1			I/O Select 8
				1			I/O Select 7
				1			I/O Select 6
				1			I/O Select 5
					1		I/O Select 4
					1		I/O Select 3
					1		I/O Select 2
					1		I/O Select 1
			100				I/O Control 2
				1			I/O Select 14
				1			I/O Select 13
				1			I/O Select 12
				1			I/O Select 11
					1		I/O Select 10
					1		I/O Select 9
					1		I/O Unit 2 Select
					1		I/O Unit 1 Select
	0000	0	000				Device address - DPF - M and N must be zero
				0000	0		Not used
					1		Enable dual programming mode
DPF					0		Disable dual programming mode
					1		Enable interrupt level 0 (system control panel interrupt)key
					0		Disable interrupt level 0
					1		Reset interrupt request 0
	0101						Device address - 1442 RPQ (5)
		0					Must be zero
			000				Feed
			001				Read translate mode
1442			010				Punch and feed
			011				Read C1 mode
			100				Punch - No feed
							Note: All other N codes invalid. Select stacker 2. x indicates "don't care" bits. Any other control code combination than 001 is invalid and will result in the card going to stacker 1.
				xxxx	x001		

These control codes may also be used with N codes 001 or 010 below

All other N codes invalid.

All other N codes invalid.

SENSE (SNS) INSTRUCTION FORMATS

5424 MFCU SENSE (SNS)

Op Code 0 7	Q Code 8 11 DA	12 M	13 15 N	16 Operand 1		
30				Operand 1 = 2 bytes	Direct addressing	Byte 1 = Operand 1 address
70				Operand 1 = 1 byte	Indexed by XR-1	Byte 2 = Operand 1 address-1
B0				Operand 1 = 1 byte	Indexed by XR-2	
	1111			Device address for MFCU (F)		
		0		Must be zero		
					Low Core Address	High Core Address
			000		Byte 2 (EB2)	Byte 1 (EB1)
					0 Punch CB	0 Hopper 1 or 2 magnet
					1 Punch strobe	1 Hopper cell covered
					2 Punch magnet one	2 Gear count 1, 3, 5, 7, 9, 11
					3 Ind 1 Byte 2 bit 3 (spare)	3 Read cell one exposed
					4 Print time	4 Read cell 18 exposed
					5 Print fire CB	5 Allow read
					6 Print magnet 1 (A1) 9(A2)	6 Hopper CB
					7 Ind 1 Byte 2 bit 7 (spare)	7 Ind 1 Byte 1 bit 7 (spare)
			001		0 Corner kick magnet	0 Punch registration roll 1 or 2
					1 Print stepper clutch magnet	1 Prepunch cell covered
					2 Post-print cell covered	2 Punch gate magnet
					3 Print inject CB	3 Punch eject roll magnet
					4 Print kick CB	4 Punch stepper roll magnet
					5 Print stepped CB	5 Corner cell covered
					6 Print allow, punch execute	6 Punch stepper CB
					7 Ind 2 Byte 2 bit 7 (spare)	7 Ind 2 Byte 1 bit 7 (spare)
			011		0 Print buffer 1 busy	0 Read check
					1 Print buffer 2 busy	1 Punch check
					2 Card in wait 1	2 Punch invalid
					3 Card in wait 2	3 Print data check
					4 Reserved	4 Print clutch check
					5 Hopper cycle not complete	5 Hopper check
					6 Card in transport counter bit 2	6 Feed check
					7 Card in transport counter bit 1	7 No op
			010	Invalid		
			100	MFCU print address register		Stores register
			101	MFCU read address register		Contents at
			110	MFCU punch address register		operand address 1 and
			111	Invalid		operand address 1 minus one.
				xxxx xxxx	Operand address (sense bytes destination)	

SENSE (SNS) INSTRUCTION FORMATS (continued)

5203 PRINTER SENSE (SNS)

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	1110			Device address printer (E)		
		0		Must be zero		
					Low Core Address	High Core Address
			000		Byte 2 (EB2)	Byte 1 (EB1)
					0	0
					1	1
					2	2
					3 Left carriage	3 Right carriage
					4 line location	4 line location
					5	5
					6	6
					7	7
			001		0	0 Not printing - contains
					1 Binary amount to	1 character in chain counter
					2 be added or sub-	2 equal to character at
					3 tracted to the line	3 print position 1.
					4 printer data address	4 Printing - contains char-
					5 register	5 acter in chain counter in-
					6 (LPDAR)	6 dicating character at
					7	7 position being addressed.
			010		0 Left or right carriage emitter	0 Hammer shift clutch
					1 Execute print latch	1 Print start SS - emitter pulse
					2 Chain emitter SS	2 Left or right carriage clutch
					3 PSS 1	3 Print cycle 1
					4 Print time	4 Print cycle 2
					5 CE sense bit latched	5 Print cycle 3
					6 HMR unit at extreme left (M1)	6 Hammer set latch
					7 Home gate	7 Hammer bar right
			011		0 Carrier sync check	0 Chain sync check
					1 Carriage space check	1 Incrementer sync check
					2 Forms jam check	2 Hammer unit thermal check
					3 Incrementer failure check	3 Not used
					4 CE sense bit latched	4
					5 Hammer echo check	5 48 character chain installed
					6 Any hammer on check	6 Unprintable character
					7 No op	7 CE sense bit
			100		0	0
					1	1
					2	2
					3 LPIAR - Hi	3 LPIAR - Lo
					4	4
					5	5
					6	6
					7	7
			101		Invalid	
			110		0	0
					1	1
					2	2
					3 LPDAR - Hi	3 LPDAR - Lo
					4	4
					5	5
					6	6
					7	7
			111		Invalid	
				xxxx xxxx	Operand address (sense bytes destinations)	

SENSE (SNS) INSTRUCTION FORMATS (continued)

5444 FILE SENSE (SNS)

Op Code 0 7	Q Code DA 8 11	Q Code M 12	Q Code N 13 15	Operand 1 16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
80				Operand 1 = 1 byte Indexed by XR-2		
	1010			Device address disk drive 1 (A)		
	1011			Device address disk drive 2 (B)		
		0		Removable disk		
		1		Fixed disk		
				Low Core Address	High Core Address	
				Byte 2 (EB2)	Byte 1 (EB1)	
			000	Invalid		
			001	Invalid		
			010	0 No op Byte 0 1 Inverventión required 2 Missing address marker 3 Equipment check 4 Data check 5 No record found 6 Track condition check 7 Seek check	0 Scan equal hit 1 1 Cylinder zero 2 End of cylinder 3 Seek busy 4 100 cylinder 5 Overrun 6 Reserved 7 Disk drive 2 sel	
			011	0 Unsafe 2 1 TAP line A 2 TAP line B 3 TAP line C 4 Index 5 Head settling 6 Jumperable CE bit 7 Reserved	0 Reserved 3 1 Jumperable CE bit 2 Jumperable CE bit 3 Not bit ring inhibit 4 Standard write trigger 5 Condition priority request 6 Bit ring 0 7 Not CC reg position 17	
			100	DFDR		
			101	Invalid		
			110	DFCR		
			111	Invalid		
			xxxx xxxx	Operand address (sense bytes destination)		

SENSE (SNS) INSTRUCTION FORMATS (continued)

BSCA SENSE

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	1000			Device address BSCA (8)		
		0		Must be zero		
				Low core address	High core address	
				Byte 2 (EB2)	Byte 1 (EB1)	
			000	0 Reserved	0 Reserved	
				1 Bit time counter 4	1 Reserved	
				2 Bit time counter 2	2 Reserved	
				3 Bit time counter 1	3 Reserved	
				4 Reserved	4 Block cycle steal request (ITB, BCC or VRC check)	
				5 Transmit trigger	5 LSR/shift reg parity check	
				6 Receive trigger	6 I/O cycle steal overrun	
				7 CE SNS bit	7 DBI parity check	
			001	Stop address register		
			010	Transition address register		
			011	0 Timeout	0 Reserved	
				1 CRC/LRC/VRC	1 Reserved	
				2 Adapter check on transmit	2 Reserved	
				3 Adapter check on receive	3 Reserved	
				4 Invalid ASCII character	4 Reserved	
				5 Abortive disconnect	5 Reserved	
				6 Disconnect timeout	6 Data set ready	
				7 Reserved	7 Data line occupied	
			100	Current address register		
			101	Invalid		
			110	0 } CRC high (zeros for ASCII) 7	0 } CRC low (LRC for ASCII) 7	
			111	Invalid		
				xxxx xxxx	Operand address (sense byte destination)	

SENSE (SNS) INSTRUCTION FORMATS (continued)

5471 CONSOLE I/O SENSE (SNS)

Op Code	Q Code: DA	Q Code: M	Q Code: N	Operand 1		
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	0001			Device address 5471 (1)		
		0		Selects keyboard		
		1		Selects printer		
				Low Core Address	High Core Address	
				Byte 2 (EB2)	Byte 1 (EB1)	
	001			0 Spare	0 Req key int pending	
				1 Spare	1 End or cancel int pending	
				2 B	2 Cancel key	
				3 A	3 End key	
				4 8 Card code	4 Return or data key interrupt pending	
				5 4	5 Return key	
				6 2	6 Keyboard translator check	
				7 1	7 Keyboard data check	
	011			0 Keyboard mode switch	0 Request key enabled	
				1 P	1 Data key enabled	
				2 B	2 Strobe switch	
				3 A Keyboard	3 Strobe switch sampled	
				4 8 code	4 Request-end-cancel key	
				5 4	5 Request-end-cancel key sampled	
				6 2	6 Keyboard shifting	
				7 1	7 Reserved	
				Printer (M bit 1)		
	001			0 Enable printer	0 Printer interrupt pending	
				1 5.24 msec	1 Reserved	
				2 2.68 sec	2 Unprintable character	
				3 Cycle FL	3 Printer busy	
				4 Reserved	4 End of line	
				5 Feedback too late	5 End of form	
				6 Extra cycle	6 Print translator check	
				7 Cycle too long	7 Printer malfunction	
	011			0 Shift mode switch	0 Lower shift required	
				1 No print	1 Upper shift required	
				2 T2	2 Reserved	
				3 T1	3 Feedback switch	
				4 R5	4 Feedback switch sampled	
				5 R2A	5 Long function switch	
				6 R2	6 Long function switch sampled	
				7 R1	7 CE SNS bit (active for MST down level at A-B2N2U06)	
		*				
			xxxx xxxx	Operand address (sense bytes destinations)		

* Note: All other N codes invalid

SENSE (SNS) INSTRUCTION FORMATS (continued)

5475 KEYBOARD SENSE (SNS)

Op Code	Q Code			Operand 1			
	DA	M	N				
0	7 8 11	12	13 15	16			
30				Operand 1 = 2 bytes Direct addressing		Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1		Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2			
	0001			Device address for keyboard (1)			
		0		Must be zero			
					Low Core Address		High Core Address
			001		Byte 2 (EB2)		Byte 1 (EB1)
					0		0 Print switch on
					1		1 Spare
					2		2 Lower shift key
					3 Data character		3 Invalid character detected
					4 keyed (EBCDIC)		4 Spare
					5		5 Multipunch interrupt
					6		6 Spare
					7		7 Data key interrupt
			010				
					0 Program 1 key		0 Auto skip/auto dup on
					1 Program 2 key		1 Record erase actuated
					2 Program load switch actuated		2
					3 Release key		3 Program switch on
					4 Field erase key		4 Skip key
					5 Error reset key		5 Dup key
					6 Read key		6 Auto rec rel sw
					7 Right adjust key		7 Functional key interrupt
			011				
					0		0 Keyboard enable
					1		1 Any function key
					2		2 Bail forward contacts
					3		3 Unlock keyboard signal
					4 Not available		4 Bail forward trig
			*		5		5 Toggle switch latch
					6		6 Any data key
					7		7 CE sense switch
				xxxx xxxx	Operand address (sense bytes destination)		
					Note: Signal jumpered to A-B2 M2P03		

* Note: All other N codes invalid

SENSE (SNS) INSTRUCTION FORMATS (continued)

SIOC SENSE

Op Code	Q Code			Operand 1		
0 7	DA 8 11	M 12	N 13 15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address +1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	0011			Device address SIOC (3)		
		0		Must be zero		
				Low core address	High core address	
				Byte 2 (EB2)	Byte 1 (EB1)	
			000	Invalid		
			001	0 Write mode set service response	Diag mode	
				1 Reset service response after 6 msec	Spare	
				2 Transfer line 2 EOT	Latch trans line 4	
				3 Transfer line 1 EOT	Latch trans line 3	
				4 Odd parity	Latch trans line 1	
				5 Decrement DAR	Trans line 3 reset disc latch	
				6 Latch I/O 1 select	Reset disc latch after 6 msec	
				7 Slave (trans line 6 & 7 latch)	Trans line 5 reset disc latch	
			010	0 Spare	0	Length count register
				1 End request	1	
				2 Interrupt pending	2	
				3 I/O attention	3	
				4 Data trans reg parity check	4	
				5 No op latch	5	
				6 LCR overflow	6	
				7 I/O ready	7	
			011	0 I/O ID bit 8	I/O trans line 8	
				1 I/O ID bit 4	I/O trans line 7	
				2 I/O ID bit 2	I/O trans line 6	
				3 I/O ID bit 1	I/O trans line 5	
				4 I/O device attached	I/O trans line 4	
				5 I/O transfer line 11	I/O trans line 3	
				6 I/O transfer line 10	I/O trans line 2	
				7 I/O transfer line 9	I/O trans line 1	
			100	0 DAR high 7	0 DAR low 7	
			101	0 SIOC request latch	0	Data transfer reg
				1 Service request	1	
				2 Service response	2	
				3 Interrupt enable	3	
				4 I/O disconnect	4	
				5 Write cell	5	
				6 Read cell	6	
				7 I/O selected	7	
			110	Invalid		
			111	Invalid		
			xxxx xxxx	Operand address (sense bytes destinations)		

SENSE (SNS) INSTRUCTION FORMATS (continued)

1442 SENSE (SNS)

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	0101			Device address 1442 (5)		
		0		Must be zero		
				Low Core Address	High Core Address	
			011	Byte 2 (EB2)	Byte 1 (EB1)	
				0 Not assigned	0 Read compare	
				1 Not assigned	1 Last card indicator	
				2 Not assigned	2 Punch check	
				3 Read station jam	3 Data overrun	
				4 Hopper misfeed	4 I/O attention	
				5 Feed clutch	5 No-op latch	
				6 Punch station jam	6 Feed check	
				7 Transport jam	7 Invalid card code	
			001	0 Not assigned	0 All cells on	
				1 Not assigned	1 Read cells 7, 8, 9	
				2 Not assigned	2 Read cells 4, 5, 6	
				3 Punch incremental drive CB A	3 Read cells 1, 2, 3	
				4 Punch CB 2	4 Read cells 12, 11, 0	
				5 Punch CB 1	5 Read emitter	
				6 Punch incremental drive CB B	6 Feed CB 2, 3, 4	
				7 CE diagnostic bit 1	7 Feed CB 1	
			010	0 Punch echo 9	0 Punch echo 1	
				1 Punch echo 8	1 Punch echo 0	
				2 Punch echo 7	2 Punch echo 11	
				3 Punch echo 6	3 Punch echo 12	
				4 Punch echo 5	4 Punch echo valid	
				5 Punch echo 4	5 Not assigned	
				6 Punch echo 3	6 Punch cell dark	
				7 Punch echo 2	7 CE diagnostic bit 2	
			100	Store 1442 DAR		
			*	xxxx xxxx	Operand address (sense bytes destinations)	

* Note: All other N codes invalid

SENSE (SNS) INSTRUCTION FORMATS (continued)

5410 CPU SENSE (SNS)

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing		Byte 1 = Operand 1 address
70				Operand 1 = 1 byte Indexed by XR-1		Byte 2 = Operand 1 address-1
B0				Operand 1 = 1 byte Indexed by XR-2		
	0000				Device address CPU (0)	
		0			Must be zero	
					Low Core Address	High Core Address
			000		Byte 2 (EB2)	Byte 1 (EB1)
					0 1 2 3 Address switch 1	0 1 2 3 Address switch 3
			*		4 5 6 7 Address switch 2	4 5 6 7 Address switch 4
				xxxx xxxx	Operand address (sense bytes destinations)	

* Note: All other N codes invalid

SHORT EXERCISER PROGRAMS

MFCU SHORT EXERCISER PROGRAMS

Feed Primary Card

Address:

0000	F3F000	Start I/O - feed primary
0003	C0000000	Branch back to address 0000

Punch Primary Card

Address:

0000	F3F000	Start I/O - Fill primary wait station
0003	31F6000F	Load I/O - load MPCAR
0007	F3F200	Start I/O - feed and punch primary
000A	C0000003	Branch back to address 0003
000E	0200	Address of MPCAR
0200		Data to be punched

Read Primary Card

Address:

0000	31F5000C	Load I/O - MRDAR
0004	F3F100	Start I/O - read primary
0007	C0000000	Branch back to address 0000
000B	0200	Address of MRDAR

Feed Secondary Card

Address:

0000	F3F800	Start I/O - feed primary
0003	C0000000	Branch back to address 0000

Punch Secondary Card

Address:

0000	F3F800	Start I/O - Fill secondary wait station
0003	31F6000F	Load I/O - load MPCAR
0007	F3FA00	Start I/O - feed and punch secondary
000A	C0000003	Branch back to address 0000
000E	0200	Address of MPCAR
0200		Data to be punched

Read Secondary Card

Address:

0000	31F5000C	Load I/O - MRDAR
0004	F3F900	Start I/O - read secondary
0007	C0000000	Branch back to address 0000
000B	0200	Address of MRDAR

SHORT EXERCISER PROGRAMS (continued)

PRINT FROM PRIMARY

0000	F3F000	Start I/O - Fill primary wait station
0003	31F4000F	Load I/O - Load MPTAR
0007	F3F400	Start I/O - Print primary
000A	C0000003	Branch to 0003
000E	0200	
0200		Data to be printed

PRINT FROM SECONDARY

Same as Print from Primary with these changes:

0001 to F8
0008 to FC

REPRODUCE

Data cards in Primary
Blanks in Secondary
OVERLAP Switch OFF

0000	F3F800	Fill secondary wait station
0003	31F4001A	Load I/O - MPTAR
0007	31F5001A	Load I/O - MRDAR
000B	F3F100	Start I/O - Read primary
000E	31F6001A	Load I/O - MPCAR
0012	F3FE07	Start I/O - Punch print secondary
0015	C0000007	Branch to 0007
0019	0200	

5471 SHORT EXERCISER PROGRAMS

TYPEWRITER FUNCTION (no carriage return)

Addr		
0000	F31011	Reset int pending, turn on proceed
0003	30110200	Sense
0007	38080200	TBN for return or data key init pending
000B	C0900003	Test false, branch if condition true
000F	31180200	Load data register with character keyed
0013	F31880	Start print
0016	C0000000	Unconditional branch to 0000

SHORT EXERCISER PROGRAMS (continued)

PRINT CHARACTER (with EOL carriage return)

Addr		
0000	31180201	Load data register with character
0004	F31880	Start print
0007	30190300	Sense
000B	38080300	TBN for EOL
000F	C0900004	Test false, branch if condition true
0013	F31840	Carriage return and index
0016	C0000004	Unconditional branch
0200	F8	Character to be printed

5203 - PRINT Hs

Alter all of storage to 40

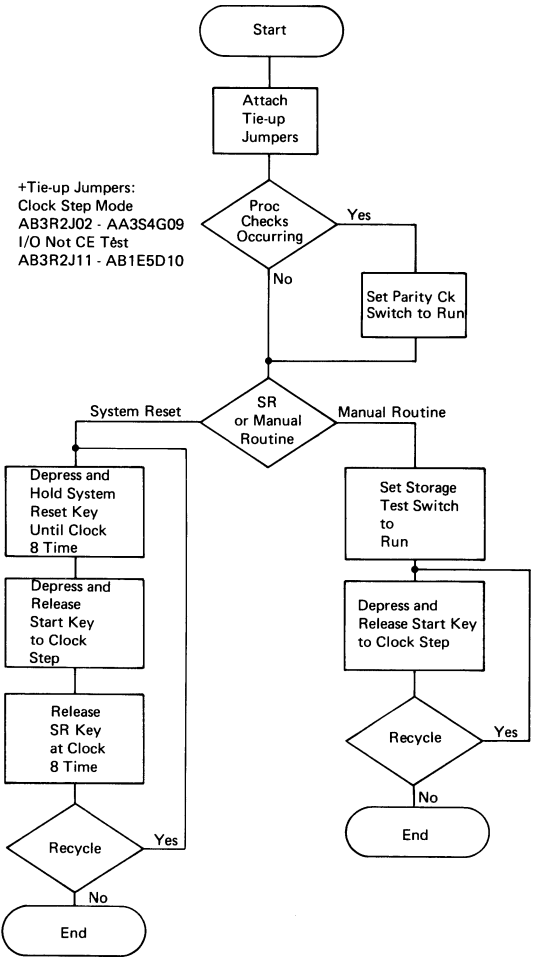
Addr		
0000	31E40022	Load I/O - Load LPIAR
0004	31E60022	Load I/O - Load LPDAR
0008	C1E60008	Test I/O busy
000C	3CC8012B	Set up chain image (one "H" at position 44)
0010	3CC801FF	Move "H" to data buffer
0014	0C8301FE01FF	Fill data buffer (017C-01FF) with "Hs"
001A	F3E2XX	Print and space XX = 01 = Space 1 XX = 02 = Space 2 XX = 03 = Space 3
001D	C0000008	Branch to address 0008
0021	0100	Data for load I/O

5410 SERVICE AIDS

SINGLE CYCLE SYSTEM RESET AND MANUAL ROUTINE

This service aid is a procedure for clock stepping through system reset or the 5410 test modes. (ie alter SAR, alter storage or display storage)

+Tie-up Jumpers:
Clock Step Mode
AB3R2J02 - AA3S4G09
I/O Not CE Test
AB3R2J11 - AB1E5D10



5410 SERVICE AIDS (continued)

Power Supply Service Aids

NORMAL CONDITIONS WITH ON/OFF SWITCH OFF, MAIN CB ON, AND LINE SOURCE ON:

A +24VDC control voltage is available (TP2=24VDC).

B K1 is energized (convenience outlet on).

C K2 is energized (no thermal condition).

D Lamp test switch is active (only thermal and power check lights will light with lamp test).

NORMAL VOLTAGE MEASUREMENTS (WITH ALL REGULATOR CARDS IN PLACE)

The following measurements were made with a WESTON 901 DC meter. The values given should be considered representative of a standard configured System/3 (5410, 5203, and 5424). Any significant deviation from the voltages given identify a possible power supply malfunction.

	E1 to E2	E3 to E4	E9 to E10	E13 to E14
–4V	10.4	4.8	20.4	4.15
+6V	12.7	6.0	20.6	5.9
–30V	47.5	30.0	20.6	30.0

Point to ground measurements:

All the point to ground measurements are relative to the regulator voltage setting (given above at E13 to E14).

	E1	E2	E3	E4	E5	E6	E7
–4V	+5.9	–4.5	–4.4	0	+5.9	+2.7	+2.7
+6V	+12.6	0	0	+5.9	+12.7	+7.3	+7.6
–30V	+17.9	–30	–30	0	+17.9	+.7	+.7

E8	E9	E10	E11	E12	E13	E14
+26.6	+20.6	+.3	+1.2	0	–4.0	0
+26.6	+26.6	+5.9	+6.0	+5.9	0	+5.9
+26.6	+20.4	–.1	+.1	0	–30.0	–.1

NORMAL VOLTAGE MEASUREMENTS (WITH ASSOCIATED REGULATOR CARD REMOVED)

The following measurements were made with the regulator card associated with the voltage in question removed (ie, if the +6V regulator card is removed, the -4V and -30V cards should remain in their sockets and only the "+6V" voltages should be checked).

The following measurements were made with a WESTON 901 DC meter. The values given should be considered representative of a standard configured System/3 (5410, 5203, and 5424). Any significant deviation from the voltages given identify a possible power supply malfunction.

	E1 to E2	E3 to E4	E9 to E10	E13 to E14
* –4V	15.8	0	31.0	0
* * +6V	13.0	.6	21.2	.6
* * * –30V	48.5	2.4	21.0	2.4

* With –4v regulator card removed only
* * With +6v regulator card removed only
* * * With –30v regulator card removed only

Point to ground measurements with same conditions as stated in previous table.

	E1	E2	E3	E4	E5	E6	E7
–4V	+15.8	0	0	0	+15.8	0	0
+6V	+13.1	0	0	–1.5	+13.1	–.6	–.6
–30V	+46	–2.4	–2.4	0	+46	–.1	–.1

E8	E9	E10	E11	E12	E13	E14
+27.4	+31.0	0	0	0	0	0
+27.2	+20.8	–.6	–.6	–.6	0	–.6
+27.0	+21.0	0	0	0	–2.4	0

TEST POINT 13 ERROR INFORMATION

If TP13 identifies the power failure, either a +6V OV/OC condition exists or a -4V UV condition exists. If with certainty the -4V power supply is ascertained as not oscillating so that TP12 never indicates a failure, one of the following has occurred:

A A noise spike on the -4V power supply output has caused the system to fail.

B The -4V regulator output is maladjusted or the -4V AXE card is out of adjustment.

C A +6V OV/OC condition prevails.

For cases (A) and (B), the failure can be verified by removing the clip-on wire, on terminal TB1-3 of the +6V regulator. If a retry demonstrates that the system does not fail, verification is complete.

The -4V SMS AX card is adjusted to power the system down if the -4V supply goes below -3.5V.

If TP13 identifies a failure with the wire on TB1-3 removed (AXE circuit removed), a -4V UV condition did not cause the power check. A +6V OV/OC condition prevails.

TEST POINT 14 ERROR INFORMATION

If TP14 identifies the power failure, either a -30V OV/OC condition prevails or a +6V UV condition exists. If with certainty the +6V power supply is ascertained as not oscillating so that TP13 never identifies a fail-use, one of the following has occurred:

A A noise spike on the +6V power supply output has caused the system to fail.

B The +6V UV control setting located on the -30V regulator card or +6V regulator voltage level is mal-adjusted.

C A -30V OV/OC condition prevails.

The +6V UV sense connection on the -30V regulator (TB-1-1) cannot be disconnected to isolate a +6V UV noise spike problem (case A). The -30V regulator card will not operate unless +6V is available at TB1-1. A +6V UV condition sensed by the -30V regulator card will cause the system to immediately power down. If noise can be eliminated, and the +6V regulator output is correctly adjusted the fail-ure is identified as a -30V OV/OC condition.

24V SPECIAL BULK SUPPLY

When experiencing power on problems, and the special 24V bulk supply is in question, a quick service check for the presence of the 24V supply is to depress lamp test switch while power is off and observe the thermal check and power check lights. If they light, the 24V supply is present

INVERTER

An inverter for CE use is located at A-A1B3R02 Logic page KA232.

OC AND UV FAILURES

Normally the power supply itself cannot cause an OC power supply failure. If an OC condition prevails, and I/O device, logic circuits, or cables have caused the failure. If the power supply is abnormally overloaded, an OC condition will always prevail over an UV condition. Even though the regulated power supply voltage may drop, normally the OC sensing by the regulator will have powered the system down before UV can be detected.

PROCEDURE TO ISOLATE REGULATOR ASM/CARD FAILURES

On sequence up failures (TP-2 - TP-9) you can isolate failures to the unit by placing the regulator card out of the failing supply, into the -4V regulator card slot. This procedure is explained in the 5410 Power Supply MAPS, and must be followed or damage may result.

PROCEDURE TO IDENTIFY A SHORT TO GROUND (FRAME) -- FOR -4V AND +6V VOLTAGES

A Measure the resistance with the CE volt/ohm meter between the ground bar (brass plate or DC common located directly behind the CPU console. Refer to logic page ZB 512 in 5410 ALD volume 3) and any frame in the 5410 CPU housing. Resistance must not exceed 1.0 ohms on the R X 1 scale.

B Remove the ground straps between the ground bar and frame ground.

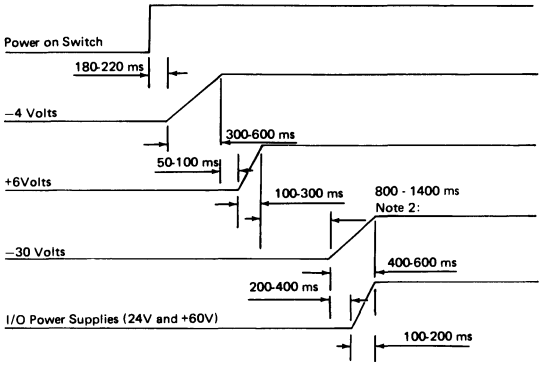
C Measure the resistance between these two points.

D The reading must exceed 5 megohms on the R X 1000 scale (normally no movement of the pointer after 3 seconds for capacitive discharge).

E If reading exceeds 5 megohms, a short to ground does not exist.

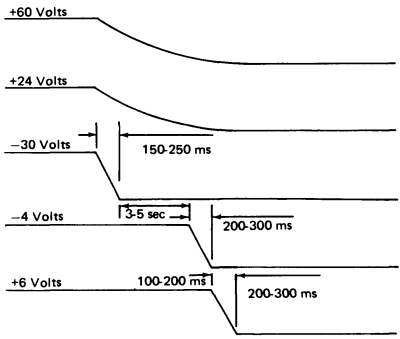
F If the measured resistance is low (less than 5 megohms), a short to ground exists. Remove one cable at a time from the ground bar (brass plate) until the faulty circuit is located.

POWER SEQUENCE



Note 1: +24 volt control voltage is on whenever the mainline switch is on.
Note 2: 500 – 960 ms for 5410 with printed circuit power sequence panel (EC816683H).

❶ Power On Sequence



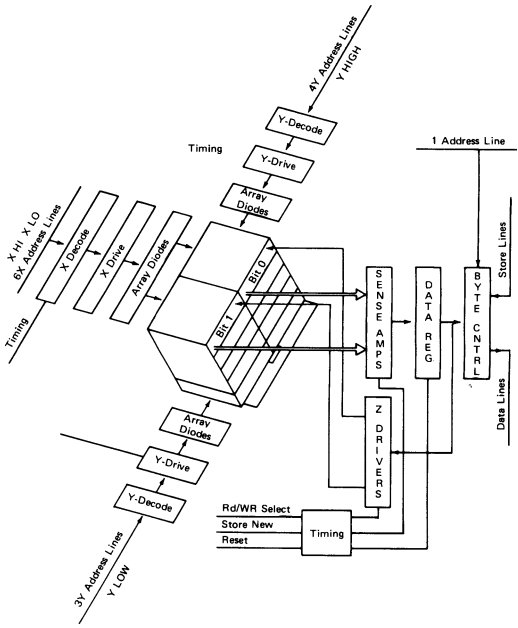
Note: +24 volt control voltage is on whenever main line switch is on.

❷ Power Off Sequence

POWER CHECK/THERMAL INDICATIONS

FAULT	POWER ON/ OFF SWITCH	INDICATORS		ACTION
		POWER CHECK	THERMAL	
Internal Power Supply Malfunction	On	On	Off	1. Turn power switch to OFF 2. Correct problem 3. Depress Check Reset 4. Turn power ON
Thermal Condition	On	On	On	1. Turn power switch to OFF 2. Power check indicator goes off 3. Thermal light stays on until condition is removed
Customer Power Source Loss	On	On	On	1. Turn power switch to OFF 2. All indicators turn OFF 3. Turn power switch to ON and continue operation
Emergency Power Off (EPO) Activated	On	Off	Off	1. Turn power switch to OFF 2. Correct problem 3. Restore EPO interlock 4. Turn power switch to ON

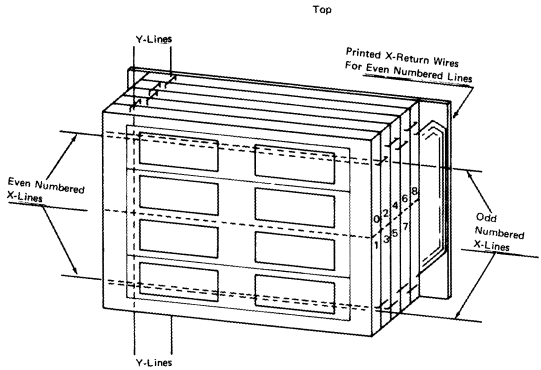
BSM ADDRESSING



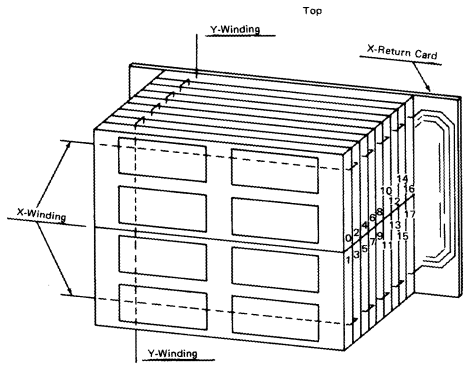
SAR Bits	One Byte (9-Bit) Readout Addressing			Binary	Decode/Remarks
15	8K	16K	24K	1	X-Lo Order
14	B	B	or	2	
13	Y	Y	32K	4	
12	T	T	B	8	X-Hi Order
11	E	E	Y	16	
10			T	32	
9	B	B	E	64	Y-Lo Order
8	S	S		128	
7	M	M	B	256	
6			S	512	Y-Hi Order
5			M	1024	
4				2048	
3				4096	
2				8192	Byte Control
1				16384	2nd BSM Selected
0	NOT USED				

Read Current Source
Read Current Direction
To other Read Gates
To 15 other Read Gates
To 15 other Read Gates
To other Read Gates
A Read Control
A Read Gate
A Read Gate
A Read Control
A Address Decode
A Address Decode
A Write Control
A Write Gate
A Write Gate
A Write Control
To other Write Gates
To other Write Gates
S32EF Diodes
Array
S32EF Diodes
To 15 other Write Gates
To 15 other Write Gates
Write Current Source
Write Current Direction
Timing
A
Z Drive
Sense AMP.
Set Bit 'N'
Reset
Data Reg. Bit 'N'
Data Bit Out
Inhibit/Sense
Note: Z-Sense wire runs parallel to the X lines.

BSM LAYOUT

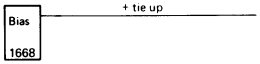


8K BSM



16K BSM

MST TIE-UP/LSR DISPLAY DATA



NOTE: DO NOT TIE DOWN any MST net. UNUSED INPUTS can be tied down to ensure a down level.

1. You can tie up any MST signal line.
2. In most cases a floating line will appear as a down level.
3. Be aware of stubs when you float lines.
4. Be aware of opening terminators.
5. Be careful not to tie up SLD nets with MST tieup voltages.

Tie-Up Points
A Gate

Device	+Tie-Up
5203 B1 Board	B1-E5D10
5424 A3 Board	A3-S4G09

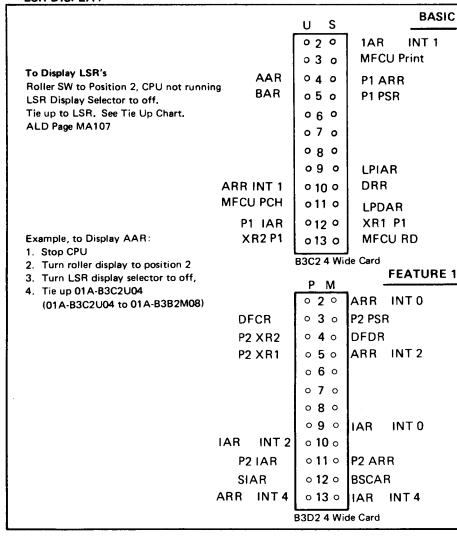
Tie-Up Points
B Gate

Device	+Tie-Up
BSCA A2 Board	A2-T2J03

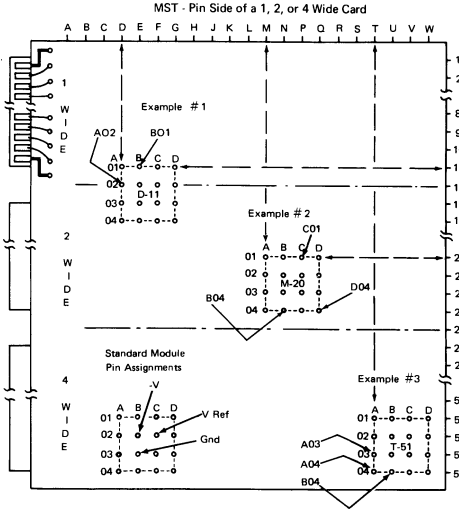
LSR DISPLAY

To Display LSR's
Roller SW to Position 2, CPU not running
LSR Display Selector to off.
Tie up to LSR. See Tie Up Chart.
ALD Page MA107

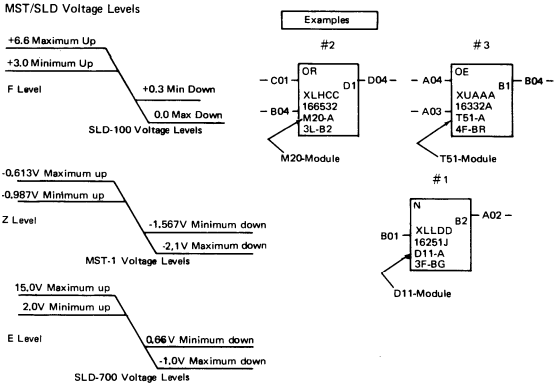
Example, to Display AAR:
1. Stop CPU
2. Turn roller display to position 2
3. Turn LSR display selector to off,
4. Tie up 01A-B3C2U04 (01A-B3C2U04 to 01A-B3B2M08)



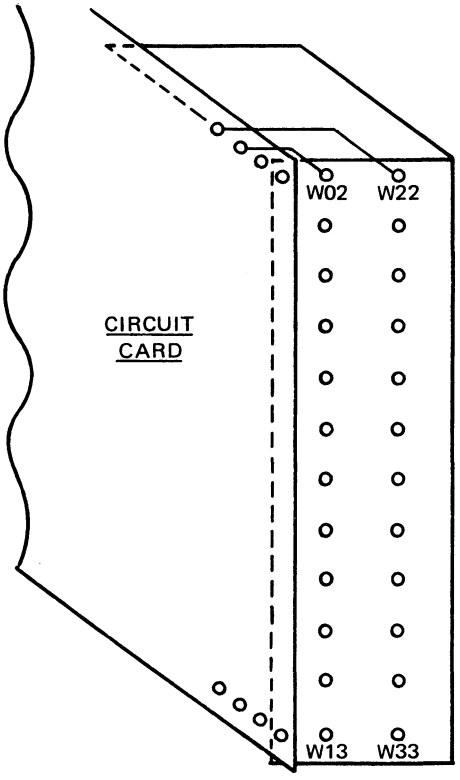
MST CARD LAYOUT



MST/SLD Voltage Levels



CIRCUIT CARD/REAR CONNECTOR



REAR VIEW

NOTE: View is facing rear of the circuit card with cable connector removed.

Card Row
Card Column
PIN SIDE
1
2
3
4
5
6
Y6
Y5
Y4
Y3
Y2
Y1
V U T S R Q P N M L K J H G F E D C B A
Z6
Z5
Z5
Z3
Z2
Z1
Cross-over Connector Position

Pin Location
D B
J G
P M
U S
1 Wide
2 Wide
4 Wide

NOTE: Cross-over Connector Position is not used on Pin Location Call-out.

DIAGNOSTIC PROBE

Probe Test Points
EC 816624

MST - Probe Test Up
01A-A3F2G12
Probe Test Down
01A-A3F2U07

SLD - Probe Test Up
01A-B1S4D09
Probe Test Down
Any Ground Pin

A CE diagnostic probe is provided to indicate line levels. This probe must be connected to the board-pin side at the voltage crossover pins.

Diagnostic probe indications as used in MAPS:

Level Up = Red light is on and stays on after an action is taken. No reference is made as to what the level is at the time the probe is placed on the pin.

Level Down = Green light is on and stays on even after an action is taken. No reference is made as to what the level is at the time the probe is placed on the pin.

Line Pulsing = Both the red and the green lights will be on-or on alternately.

Pulse on Line = Red and green lights will make one of the following transitions: (a) red to green to red (b) green to red to green, or if using the gate capability only one light may blink on and then return to both lights off.

Level Change Up/Down = Lights will change from green to red (up) or red to green (down) when the requested action is taken.

An open line = Both indicators off.

DIAGNOSTIC PROBE (continued)

The diagnostic probe is capable of measuring MST -1, SLD 100 and 700 signal levels. The probe uses -4V and ground for power. The use of any other voltage may cause damage to the probe. These voltages are obtained through a cable and power connector which connects to crossover power connectors on the gate. It is imperative that the correct orientation of the power plug be observed when working on other than MST boards.

Functionally, the probe has two input tips (one SLD, the other MST), two lamps (one for up and one for down) and two gating pins (one plus, the other minus). The user selects the proper probe tip (SLD or MST) and probes the desired pin, if the signal is an up level, the up light will come on, if the signal is down level the down light will come on. If the line is pulsing, both lamps will be on simultaneously or alternately depending on the frequency.

A voltage pin or an open pin will turn both lamps off. A 'floater' will, in most cases, appear as an open pin (both lights off). However, under certain circumstances, the floater will appear as a down level. To insure a 'floater' will not result in an improper decision, the MAP charts ask "Is the level up", when a floating condition is suspected.

Gating is accomplished by jumpering the desired gate to a pin on the board. These gates are designed for MST signal levels only. Once a gate is connected both indicator lamps will be held off until the correct polarity gate occurs, i.e., an MST up level for the plus gate or an MST down level for the minus gate. When the correct gate level is present the probe re-assumes normal operation until the gating signal ends.

The MST probe will respond to a 30 NS pulse and the SLD probe will respond to a 200 NS pulse (worst case). Each lamp operates independently of the other and will remain on for approximately 75 milliseconds once triggered. Both lamps are field replaceable. (See commonly used parts list for P/N.)

5444 SERVICE AIDS

Read/Write Safety

During Read and Write operations certain conditions are monitored by the File circuits. In an Unsafe Condition a Data Unsafe line to the FCU is raised, the R/W heads are unloaded, and file ready is deconditioned.

This can be reset only by stopping the file and restarting. In the Unsafe Condition all Write and Read operations are permanently inhibited. All other file operations should be inhibited by the FCU.

The following unsafe conditions cause a Data Unsafe signal to the FCU to be raised. They are divided within the file into the three groups shown to aid in diagnosing error conditions.

1. Write Unsafe
   a. Write selected and no write transitions detected.
   b. Write selected and multiple heads selected.
   c. Write not selected and write current source on.
2. Erase Unsafe
   a. Write selected and erase current source not on.
   b. Write not selected and erase current on.
3. Read/Write selection unsafe
   a. Read selected and either write or erase selected.
   b. Carriage accessing and either write or erase selected.

CE Disk Cartridge Restricted Tracks

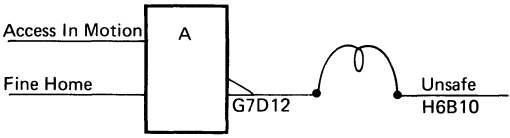
Never write on tracks 004, 005, and 006, or 071, 072, 073, 074, 075. Writing on these tracks will destroy the alignment data which can only be rewritten by returning to the plant for rewriting on the special CE Cartridge writer tool. When using the CE cartridge always check the cylinder number before writing.

5444 TAP PROCEDURE

The jumper on Y-W1-H6B10 must not be connected until just before the tap run is started.

If the actuator needs to be moved, remove jumper on H6B10 prior to using the CE switches to reposition actuator.

The actuator must be positioned on a track divisible by 10 (10, 20, 30 etc) before jumper is replaced on H6B10.



Refer to 5444 File MAP Charts Appendix B, page 900 for a detailed description of TAP procedures.

To reset unsafe condition jumper

Y - WIH6D12 to Y - WIH6J08

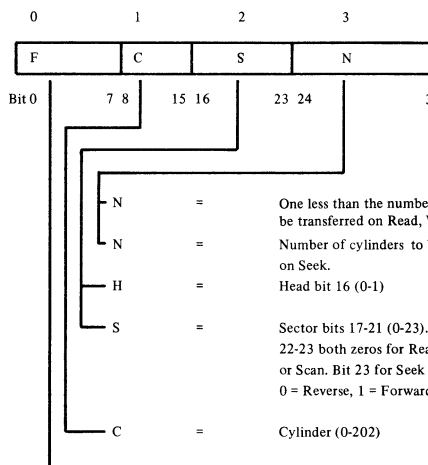
Tap lines A, B, and C may be used to monitor the three unsafe condition latches during customer operation via the CE sense bits. To do this, place the following jumpers on the 5444 board.

	FN230		FN260
Write unsafe (tap line A)	Y - WIH6G03	to	Y - WIG7B04
Select unsafe (tap line B)	Y - WIH6B10	to	Y - WIG7B03
Erase unsafe (tap line C)	Y - WIH6G04	to	Y - WIG7B05

5444 CONTROL AND ADDRESS REGISTER

DISK FILE CONTROL REGISTER

The DFCR Disk File Control Register contains the two byte address of the four byte Disk Control Field in storage. The format of the four byte Disk Control Field in core is:

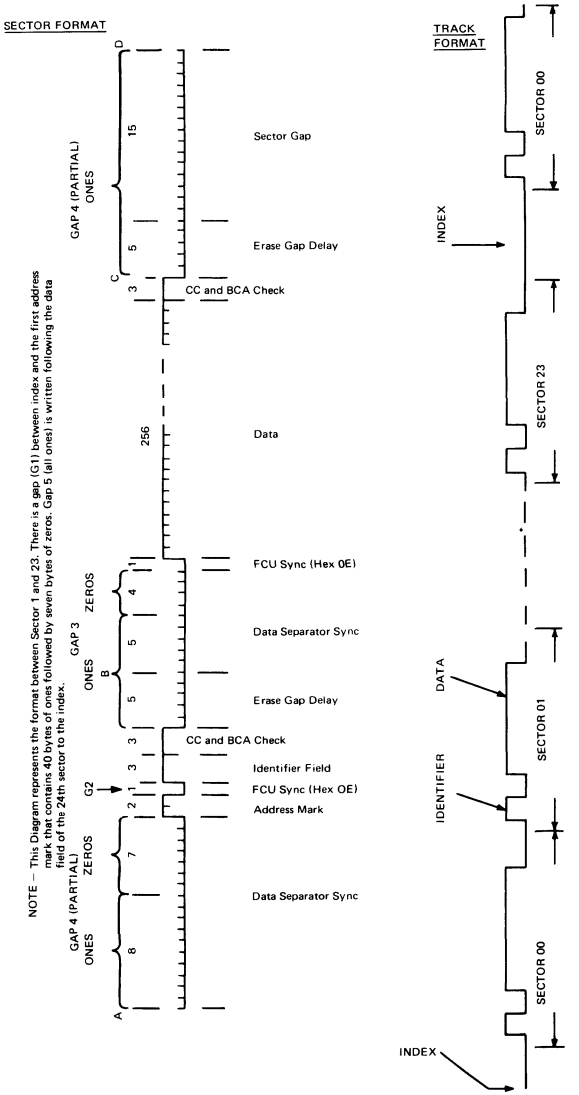


The Seek operation uses the S, and N bytes of the Disk Control Field.

DISK FILE DATA REGISTER

The DFDR keeps track of the memory address of the current data byte.

5444 SECTOR AND TRACK FORMATS



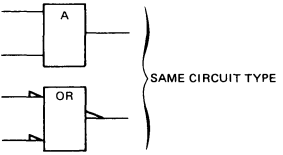
* Output signals of Data Separator Circuits, not available at the 5444

C = Clock pulse
C̄ = Missing clock pulse
1 = '1' data bit
0 = '0' (not one) data bit

LOGIC SYMBOLOGY

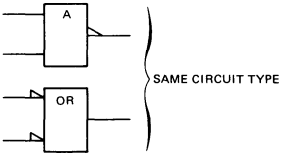
Positive AND

The output of the Positive AND is in its more positive condition when and only when all of the inputs are in their more positive condition.



Positive AND INVERT

The output of the Positive AND INVERT is in its more negative condition when and only when all of the inputs are in their more positive condition.

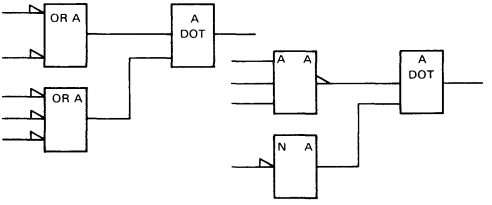


ODD COUNT

This is a device whose output will be at its indicated polarity when and only when an odd number (1-3-5-7, etc.) of its inputs are at their indicated polarity.

DOT OR and DOT AND

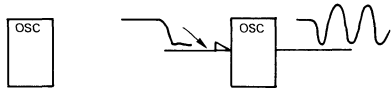
Basic function whose outputs are connected externally so that the connection performs an AND or OR operation (dot AND, dot OR) shall be identified by having an additional A or OR placed in the block to the right of the primary block function symbol.



LOGIC SYMBOLOGY (continued)

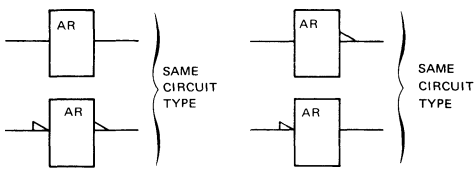
OSCILLATOR

This is a device which produces a uniform repetitive output either continuously or during the application of an input signal of the polarity indicated. It is desirable to show the frequency in the block title.



AMPLIFIER

This is a device whose fundamental purpose is to provide adequate driving energy and appropriate impedance matching to other devices. Its output will be at its indicated polarity when and only when its input is at its indicated polarity. An AMPLIFIER has only one logic input.



Non-Standard Logic Signal Voltage

An AMPLIFIER having input or output of other than standard logic signal voltage shall be made recognizable through labeling at the block.

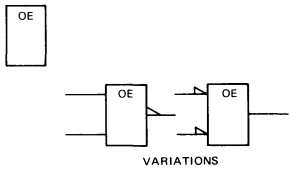
EVEN COUNT

This is a device whose output will be at its indicated polarity when and only when an even number (0-2-4-6, etc.) of its inputs are at their indicated polarity.

LOGIC SYMBOLOGY (continued)

EXCLUSIVE OR

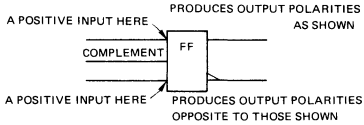
The output of an EXCLUSIVE OR will be at its indicated polarity when one and only one of its inputs is at its indicated polarity.



VARIATIONS

FLIP FLOP

This is a device which has two stable states. One of these is called the 1-state or set state, the other is the 0-state or clear state. The device normally has two outputs, a 1 output and a 0 output. In the ALD's a line from the upper part of the block will be assumed to be the 1 output and a line from the lower part of the block will be assumed to be the 0 output. The FLIP FLOP is in the 1 state when its 1 output (the upper output on the ALD) is at its indicated polarity. The 1 output and 0 output of a FLIP FLOP are always opposite in polarity.



Operation

(a) Application of a signal of indicated polarity to the line opposite the 1 output will cause the outputs of the block to assume their indicated polarities.

(b) Application of a signal of indicated polarity to the line opposite the 0 output will cause the outputs to assume polarities opposite to those indicated.

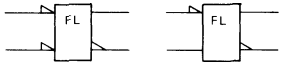
(c) Application of a signal of indicated polarity to a line centered between the two line already mentioned, or to both the set and clear inputs simultaneously, will change the state of the FLIP FLOP (complement the FLIP FLOP).

LOGIC SYMBOLOGY (continued)

FLIP FLOP LATCH or FLIP LATCH

The definition of this device is the same as that given for FLIP FLOP except that simultaneous application of signals of indicated polarity at the 1 input and the 0 input will cause the 1 output and 0 output to both go to the negative polarity or both go to the positive polarity (depending upon the characteristics of the particular circuit type) for the duration of such simultaneous input application. Complement input is not applicable to this block.

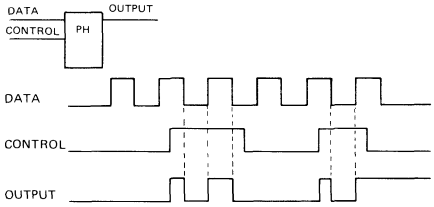
Note: Combination circuits that have both AC inputs (will complement if set and reset are applied simultaneously) and DC inputs that will cause both outputs to go to the same polarity, if applied simultaneously, will be shown as an FF. These circuits may also have a DC gate controlling the AC input.



VARIATIONS

POLARITY HOLD

This is a device whose output will be at its indicated polarity whenever the data line and the control line are at their indicated polarity. When the control input is caused to go to opposite polarity to that indicated, the output will hold to whatever polarity it possesses at that moment.



SPECIAL

A SPECIAL block will have its function adequately described by wording on the diagram page.

LOGIC SYMBOLOGY (continued)

LIMITER

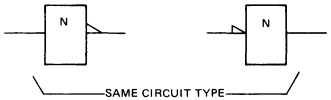
This is a device that limits one or both extremes of a waveform to a predetermined level without distortion of the remaining waveform.

SIGNAL MODE CONVERTER

This is a device that provides the necessary conversion or translation between signal lines having different signal reference values—current mode to voltage mode, voltage mode to voltage mode, etc.

INVERTER

This is a device whose output is in the more positive condition as a result of its input being in the more negative condition and vice versa.



SINGLESHOT

This is a device whose output will change for a specified time to the indicated polarity upon the application of an input signal of the indicated polarity.

VARIATION

TIME DELAY

This is a device whose primary function is the time delay of a signal without distortion of the signal.

FUNCTIONAL LOGIC SYMBOLOGY

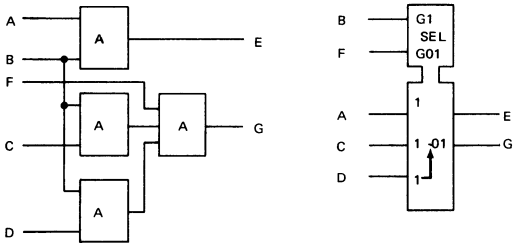
The Functional Logic Blocks used in System/3 ALD's consist of Selectors, Registers and Decodes.

SELECTOR

The Selector consists of:

a. Two or more OR's having common input or output gating.
b. Two or more AND's having common input or output gating.
c. A combination of a and b.

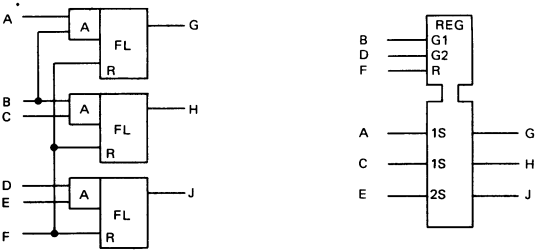
EXAMPLE



REGISTER

The Register consists of associated storage elements, such as FF, FL, PH, with common reset or control lines. Common gating may be included.

EXAMPLE

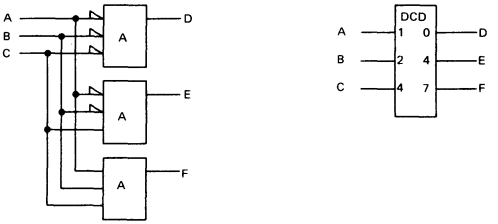


FUNCTIONAL LOGIC SYMBOLOGY (continued)

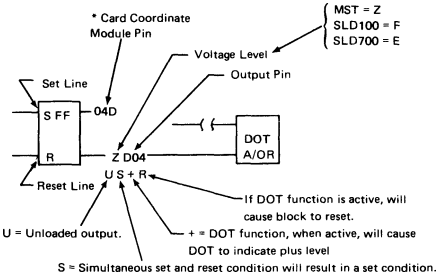
DECODE

The Decode Block contains inputs and outputs which are assigned numeric values. An output line is active when its numeric value is equal to the sum of the values of all active input lines. When all input lines are inactive the output sum is zero.

EXAMPLE



Character Modifiers are characters (alpha and symbol) printed around the blocks. These define the blocks specific operation.



The load for an unloaded output can be found by tracing the net to its termination. The load will be specified by an * on the line and noted on the bottom of the FEALD page.

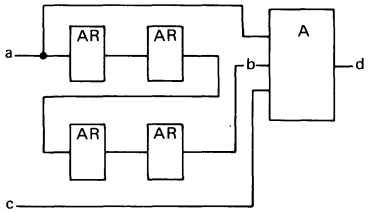
*The module pin will appear when the line does not connect to a board pin.

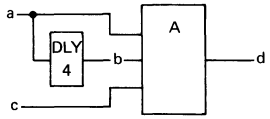
FUNCTIONAL LOGIC SYMBOLOGY (continued)

DELAY

A delay block will be generated by the FEALD program when two or more circuit elements, intended primarily for delay purposes, are removed.

EXAMPLE

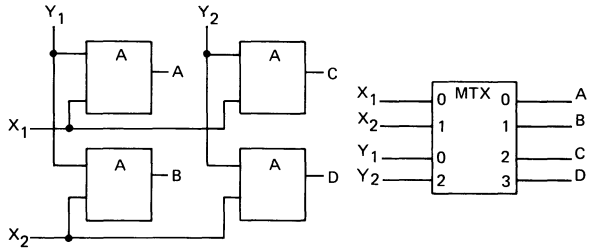




MATRIX

A matrix relates to an addressing scheme, where two or more groups of lines are used for addressing. A combination of one active line in each group will select a specific storage position.

EXAMPLE



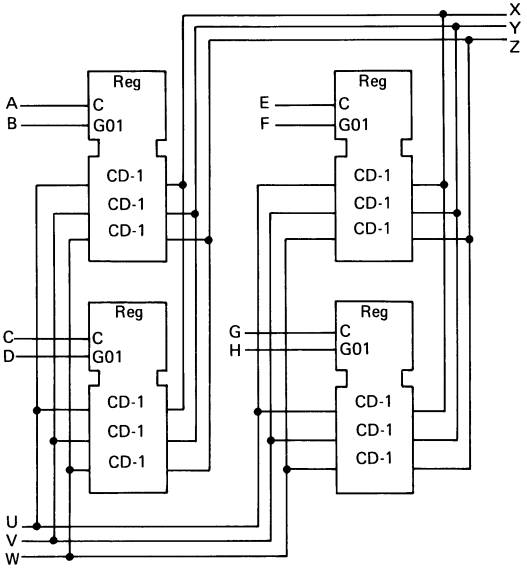
The input lines are arranged in groups. One active line in each group will give one active output.

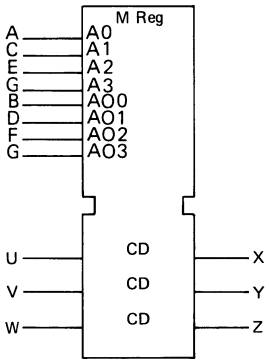
FUNCTIONAL LOGIC SYMBOLOGY (continued)

MULTIPLE REGISTER

The M reg consists of associated registers with common data in and out. The register which reads in or out is determined by individual controls and gates.

EXAMPLE





LOGIC PAGE PREFIXES

Circuits	Prefix-FEALD
25 MHz oscillator	KA
5444 Logic	FN
5471 Controls	GC
A and B registers	RA
ALU	AV
ALU controls	KY
Base LSR controls	KL
Base LSR and SAR low	MA
Cable page	WA
Card socket listing	AI
CE mode and toggle switches	PA
Channel and attachment interface (MFCU)	WN
Channel and attachment interface (printer)	WP
Channel in	KE
Channel 1 out exit lines	WB
Clock controls	KC
CPU to storage lines	WS
Cycle controls	KD
Data bus out—bank 2	MC
DBI and MFCU data registers	FD
DBO and command control (MFCU)	FC
Display and check	KB
Display selector drum	PC
Drum indicators	PB
Dual program feature	KT
File control unit	GD
In phase terminated TLDs	MD
Interrupt 1 to 4	KM
Keyboard service	GK
Main storage	MM
MFCU box	FG
MFCU box	WM
MFCU controls	FB
Op and Q registers	RN
Power to 5444	YF
Power drivers	FE
Printer box	YB
Printer controls	FP
Register controls	KG
Serial I/O channel	GS
Socket listing	A1
Socket listing	MO
Use meter control	CR
Voltage service	YE

LOGIC VERSIONS

Logic Versions 5410

VERSION FEATURE

	CPU
000	Basic Machine with Dual Program
001	5475 - Attachment
002	5471 - Attachment
003	Basic Machine without DPF
	MFCU Attachment
000	Basic 5424 Attachment
021	6-Bit MFCU
000	Katakana (W/T only)
	Printer Attachment
000	Basic 5203 Attachment
	File Attachment
000	Basic 5444 Attachment
	SIOC
000	Basic SIOC Attachment

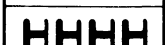
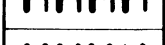
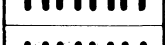
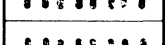
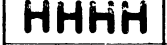
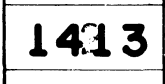
Example:

F MFCU
B
1
0 Page number
1
021 6-Bit MFCU

BSCA

	EBCDIC – USASCII		High - Low		PT PT	M PT	SW	WTSW	Autocall
000	X			X					
031	X		X		X				X
032	X			X	X				
033	X			X		X			
034	X			X			X		
035	X			X				X	
036		X	X		X				
037		X		X	X				
038		X		X		X			
339		X		X			X		
040		X		X				X	
041		X		X					X

PRINT QUALITY GLOSSARY OF TERMS

	CUTOFF (LEFT)
	CUTOFF (RIGHT)
	END TO END DENSITY
	SINGLE POSITION DENSITY
	DARK LEGS OR STROKES
	EXTRANEOUS INK
	HORIZONTAL REGISTRATION
	LIGHT BOTTOMS
	LIGHT TOPS
	PHANTOM PRINTING
	SHADOW PRINTING
	SLUR
	STROKE WIDTH (NARROW and WIDE)
	VERTICAL REGISTRATION
	VOIDS
	WIGGLERS

OSCILLOSCOPE SERVICE AIDS

BABYSITTER (Single Sweep Mode)

Indicates the sensing of a pulse of predetermined amplitude. The trigger level is generally set to 1/2 of the expected pulse amplitude.

1. To set the trigger level

CHANNEL CONTROLS	
CH 1 VOLTS/DIV	Determined by desired pulse amplitude
CH 1 INPUT	GND
MODE	CH 1
TRIGGER	NORMAL
SWEEP CONTROLS	
HORIZONTAL DISPLAY	A
A SWEEP MODE	NORMAL
A & B TIME/DIV	50 MS
A TRIGGERING	
SLOPE	+
COUPLING	DC
SOURCE	INT

Set the dot to the desired trigger level on the screen with the CH 1 position control. Adjust the TRIGGER LEVEL CONTROL to give a sweep. Reposition the dot to the base line on the screen.

2. Single sweep operation

CH 1 INPUT	DC
A SWEEP MODE	SINGLE SWEEP

Check trigger level by arming the scope by depressing the reset button and its green lite will come on. Move the spot up and check to see that a sweep is triggered when the trace reaches the preset level. The light will be turned off by a sweep and must be reset to arm the scope.

Reset the dot to your base line, arm the scope and place the channel 1 probe on the point you wish to monitor.

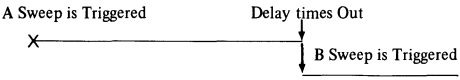
SHOOT THE MOON

Used to indicate the presence of a single high-speed pulse of a definite amplitude.

The calibration and setup is identical to the BABYSITTER except that the A SWEEP MODE is NORMAL and the trace is out of focus to enable it to be easily seen.

OSCILLOSCOPE SERVICE AIDS (continued)

DELAYED SWEEP



1. Display the desired trace with HORIZONTAL DISPLAY on A
2. Set B SWEEP MODE to B STARTS AFTER DELAY TIME
3. Set HORIZONTAL DISPLAY on A INTENSIFIED DURING B
   Adjust the DELAY-TIME MULTIPLIER until the intensified portion of the trace starts just before the desired pulse to be observed on the trace.
4. Pull DELAYED SWEEP KNOB out and adjust the B Sweep to display only the intensified pulse desired.
5. Set a SWEEP LENGTH to B ENDS A
6. Set HORIZONTAL DISPLAY to DELAYED SWEEP B
7. The DELAY-TIME MULTIPLIER may now also be used to analyze other pulses on the trace.
8. If the B trace is unstable:
   a. Set B SWEEP MODE to B TRIGGERABLE AFTER DELAY TIME
   b. Adjust the B TRIGGERING CONTROLS for a steady trace with the B TRIGGER SOURCE on INT or use an EXT TRIG for B

COMMONLY USED PARTS

COMMONLY USED PARTS		
P/N	ITEM	WHERE USED
453163	Probe Tip	Diagnostic Probe
454612	Lamp	Diagnostic Probe
817971	Probe	Diagnostic Probe
829117	Jumper Wires 6"	
829118	Jumper Wires 18"	
G229-4075	Error Log Sheet	5410
2391023	Lamp	Console 5410 5424 Backlite
2391062	Lamp	Console 5410 – Power & Thermal
2391121	Lamp	Console 5410 – Stop Light
2391653	Lamp	5424 – Read Lamp
2588263	Jumper Wires 12"	
2590223	Air Filter	5410 – A Gate
2590287	Air Filter	5410 – Regulator
2594238	Pin Extender	
5232826	Air Filter	5410 – Bulk Supply
5372183	Lamp	Console 5410 – Address Compare and I/O Check

5203 - Commonly used electrical parts are found on Logic Page YB-251

NOTES

FORCE CLOCK RUN B3R2T2 → B3C2M8
SPARE INVERTER @ B3R2 B03 IN D02 OUT
5203 HOME TIEDOWN A1B1M9U407
A1B1F2J13
TIE-UP A2S3M13 & A3T2E43

NOTES

NOTES

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Circle one of the comments and explain in the space provided:

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Explanation:

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