Contents

FRAME LOCATION TABLE

Page	Frame	Card
2-1	C13	1-1
2-3	C15	1-1
2-7	D01	1-1
2-8	D02	1-1
2-9	D03	1-1
2-10	D04	1-1
2-11	D05	1-1
2-20	D14	1-1
2-22	D17	1-1
2-24	E01	1-1
2-25	E02	1-1
2-26	E03	1-1
3-1	E07	1-1

Contents

FRAME LOCATION TABLE

Page	Frame	Card
3-1	E07	1-1
4-1	A11	1-2
4-3	A13	1-2
4-8	B01	1-2
4-9	B02	1-2
4-10	B03	1-2
5-1	B15	1-2
5-2	B16	1-2
5-4	B18	1-2

Contents

FRAME LOCATION TABLE

Page	Frame	Card
5-4	B18	1-2
5-6	C02	1-2
5-7	C03	1-2
5-8	C04	1-2
5-9	C06	1-2

INDEX

INDEX

CONTINUED ON

FRAME _ A10 __

CHECKS

ADJUSTMENTS

AND REMOVALS

A10

Chapter 4. Checks, Adjustments, and Removals

Section 1. Basic Unit

The only adjustments and repairs possible in the CPU are to the power supplies (see Chapter 5). Fr. B15 and the bridge basic storage module (BSM). If 8K, 12K, or 16K of storage is installed in the CPU, it is in an 8K or 16K BSM at location 01A-B4. If 24K or 32K of storage is installed in the CPU, three types of BSMs can be used. For early systems, 24K of storage uses an 8K BSM and a 16K BSM chained together. For later systems, a 32K BSM is used for both 24K and 32K of storage. A 48K storage system uses a 32K BSM and a 16K BSM chained together; 64K storage (RPQ S40048) uses two 32K BSMs. When two BSMs are chained (dual BSMs), they are at locations 01A-B4 and 01A-A4 in the CPU. When one 32K BSM is used, it is at location 01A-B4.

Storage Capacity	BSM Sizes Required 8K		16K		32K
8K	1				
12K			1		
16K			1		
24K	1	and	1	or	1
32K			2	or	1
48K			1	and	1
64K					2

For reliable storage operation, the BSM diagnostics should run two minutes without errors when the -30 volt XYZ drive voltage is biased 1.2 volts in either direction from its initial setting. If BSM operation is unreliable, either a fault exists, XYZ drive voltage (-30V) reoptimization is required, or strobe setting and -30V reoptimization is required.

Proper settings for the -30V power supply and the strobe settings for each BSM are recorded on a decal located on the XYZ current limiting resistor cover (Figures 4-1, 4-2, and 4-2B). Fr. A12

Note: The memory thermistor automatically changes the -30V power supply to compensate for temperature changes. For each degree F temperature change there is a 75 mV change to the -30V power supply.

The only repairs possible on the BSM are card replacement, voltage and strobe adjustments, and repair of minor (visible) shorts or open circuits. Major array failures (shorted diodes, internal opens, etc.) necessitate BSM replacement.

Most problems fall into two categories of component failures:

1. Circuit failures (card, loose connector, etc.)
2. Array failures (shorted lines, open line, diode, etc.)

Intermittent or random failures are treated separately.

4

All

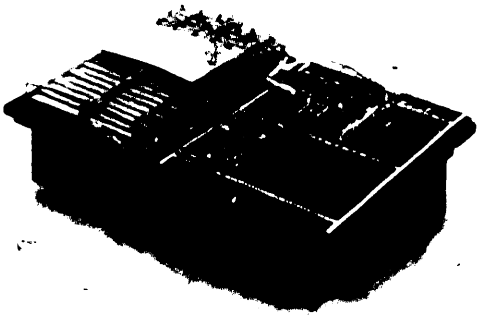


Figure 4-1. 8K Basic Storage Module (Probe Side)

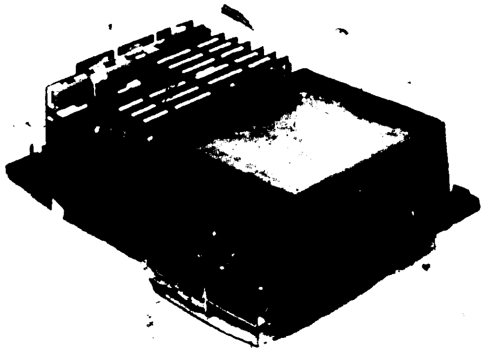


Figure 4-1A. 8K Basic Storage Module (Card Side)

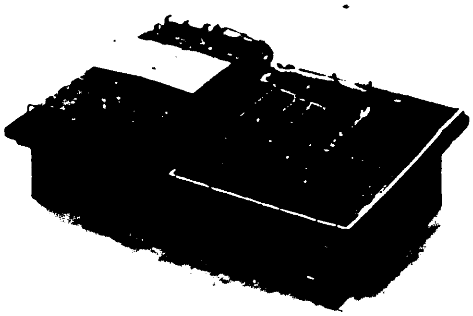


Figure 4-2. 16K Basic Storage Module (Probe Side)

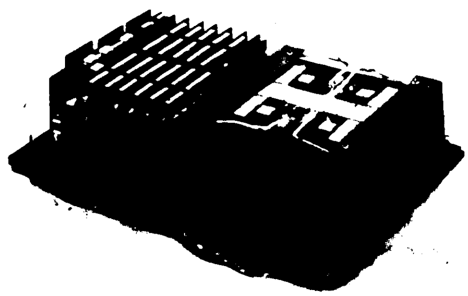


Figure 4-2A. 16K Basic Storage Module (Card Side)

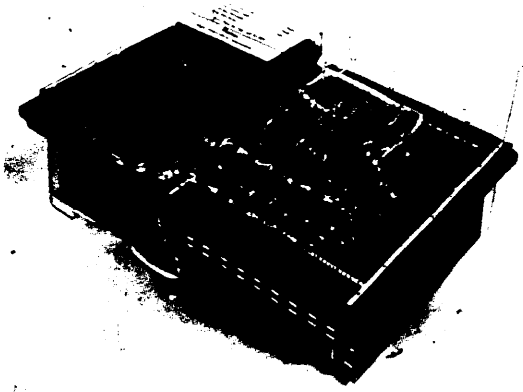


Figure 4-2B. 32K Basic Storage Module (Probe Side)

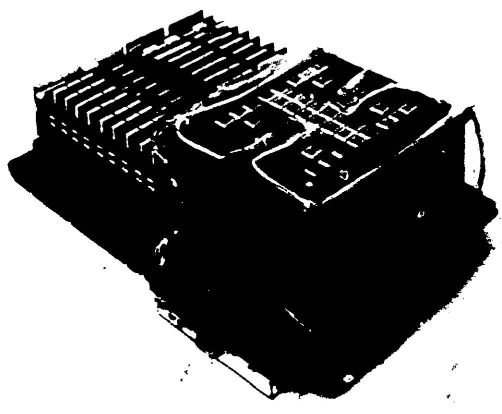


Figure 4-2C. 32K Basic Storage Module (Card Side)

4.1 FAULT LOCATION

If a failing pattern is not already evident, try manually storing and displaying or scanning storage to establish a pattern. If this fails, run storage diagnostics.

4.1.1 Circuit Failures

All BSM problems should be approached as if there has been a circuit failure. Circuit failures (card, connector, etc.) can be broken into distinct patterns. For example:

- Single bit all addresses
- Single bit - one block of addresses
- Multiple bits - all addresses
- Multiple bits one block of addresses

The 'all addresses' failure could be caused by the drive current source card or the control driver card (Figure 4-3). Fr. A14 The 'block of addresses' failure could be caused by a defective gate driver card. For example, if SAR bits 7, 8, and 9 are always active in the failing address, the chart in Figure 4-3 Fr. A14 indicates the failure could be the Y-lo gate driver.

Single-bit or multiple-bit failures can be caused by a sense/inhibit card which also contains the SDR latch for that bit.

Card location:

Note: Bits 9-17 are 0-8 when SAR bit 2 is active. Bits 8 and 17 are the P bit.

Bits	8K BSM	16K BSM
0, 1, 2	XXJ4	XXJ4
3, 4, 5	XXH4	XXH4
6, 7, 8	XXG4	XXG4
9, 10, 11	–	XXF4
12, 13, 14	–	XXE4
15, 16, 17	–	XXD4

Bits	32K BSM
0, 1	XXK4
2, 3	XXJ4
4, 5	XXH4
6, 7	XXG4
8, 9	XXF4
10, 11	XXE4
12, 13	XXD4
14, 15	XXC4
16, 17	XXB4

Multiple-bit failures at all addresses can also be caused by the strobe driver card. (For card location, see ALD page SR224.)

Using bridge MAP charts (trouble analysis flowcharts) allows repair of most of the failures by swapping or replacing cards. Use the CE pocket meter and diagnostic probe for help in locating and repairing the trouble.

4.1.2 Array Failures

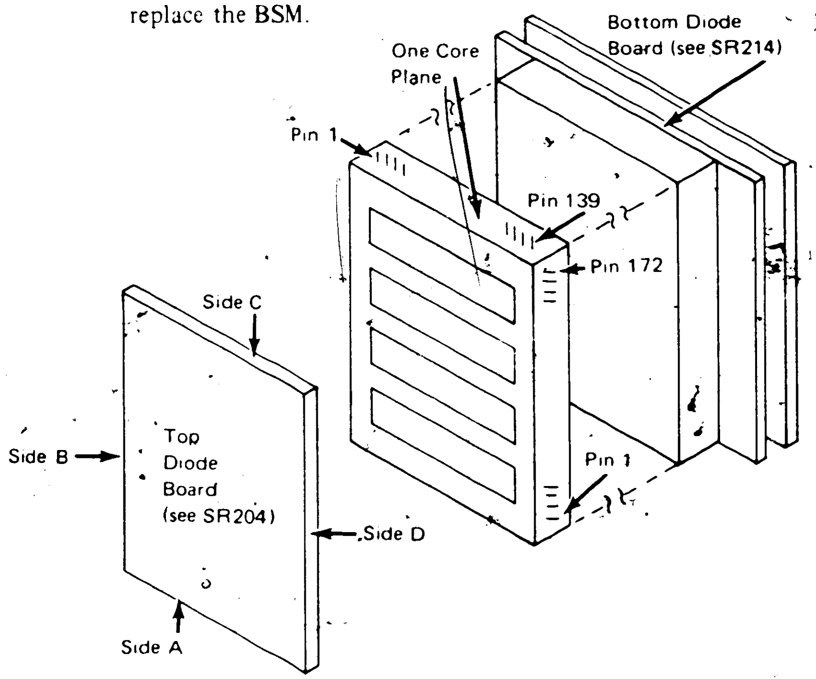
If the array fails, replacement is necessary unless the failure can be traced to cabling defects, visual defects, or an open diode. Trouble caused by open diodes can be replaced by patching a new diode across the open one. Shorted diodes require replacing the array.

4.1.2.1 Single Bit, Multiple Address Failures

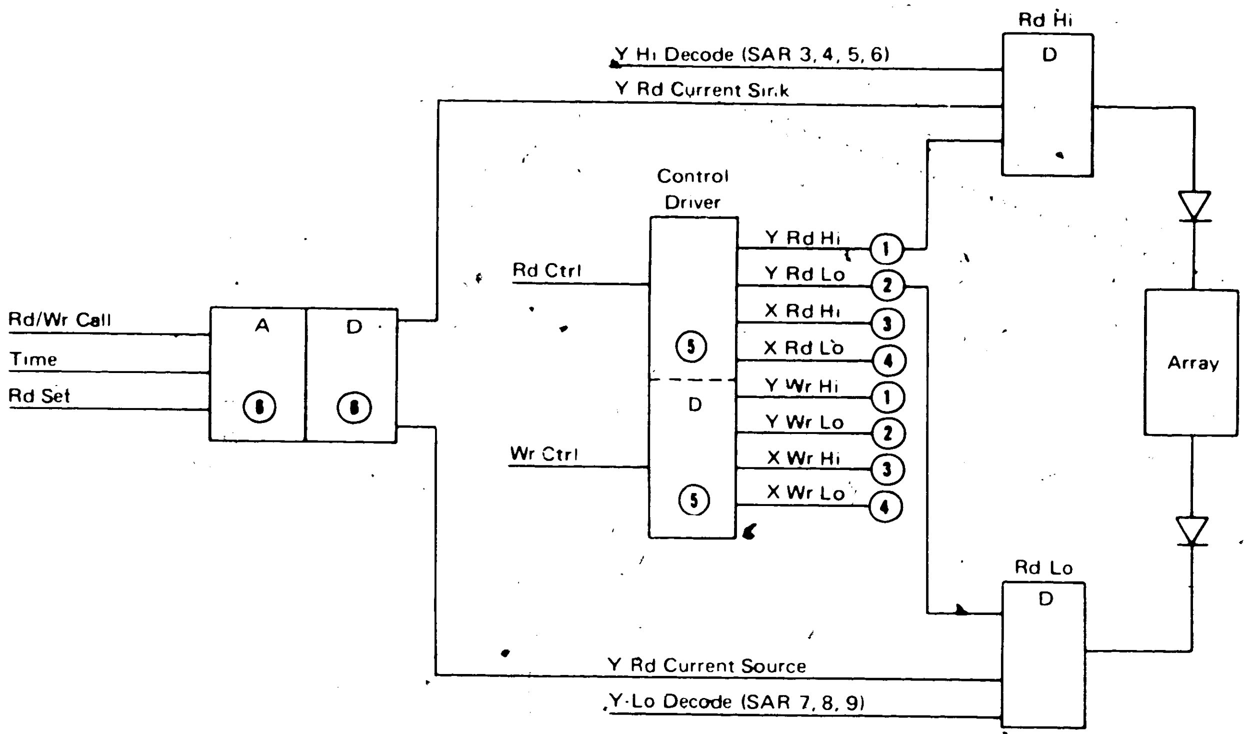
A sense/inhibit (S/Z) problem usually shows up as an extra or missing bit throughout an 8K block of storage (each S/Z line passes through 8,192 cores). If the S/Z card is not at fault, check the wiring to the Z load resistor. (Refer to SR071-076 and to SR264 for locations.) Check that -30 volts appears on pin 2 of the affected resistor.

Check also for a broken S/Z wire between the array and the back panel pins on the sense amplifier. (See Figure 4-2D for the numbering of the pins on a core plane.) A complete S/Z winding resistance should measure approximately 14.0 ohms. If the open or shorted S/Z winding is within the core plane, replace the BSM.

4



• Figure 4-2D. Numbering of Core Plane Pins



SAR Bits	1	2	(1) Y Hi (Gate-Driver Location)	(2) Y Lo	(3) X Hi	(3) X Hi B	(4) X Lo	(5) X-Y Gate Control Driver	(6) X-Y Rd/Wr Drive Current Source
			3 4 5 6	7 8 9	10 11	12	13 14 15		
8K-16K BSM	BSM Selection	Byte Control (not used on 8K)	XXG2 XXH2	XXF2	XXE2	Not Used	XXD2	XXB2	XXJ2
24K-32K BSM	Segment Selection		XXH2 XXJ2	XXG2	XXF2	XXE2		XXC2	XXK2
ALD Page ⟶			SR061 SR062 SR063 SR064	SR051 SR052	SR041 SR042	SR043 SR044	SR031 SR032	SR021	SR022

Figure 4-3. X or Y Drive System

4.1.2.2 Multiple Bits, Multiple Address Failures

If this type of failure cannot be corrected by card swapping or replacement, an array fault probably exists. If the failure is related to a combination of more than one address pattern, suspect a short between drive lines.

4.1.2.2.1 Continuity Check of X-Y Drive Lines: The charts on SR174 and SR184 (8K or 16K BSM) or SR234 and (32K BSM) describe all X- and Y-drive lines and contain all the points (terminals) for performing a continuity check. The following example and section 4.1.2.2.2 Fr. A15 refer to an 8K or 16K BSM, which uses figure 4-4 Fr. A16 and the charts found on SR174 and 184. (For a 32K BSM, use charts found on SR234 and 244).

Example: This example is for the failing X-address of 000110 in an 8K or 16K BSM. X-read current is shown from left to right through the array X-winding. X-write current is shown from right to left through the same array X-winding.

(In the following discussion, column numbers refer to the chart on SR174.) Starting from the X-read lo gate, D2G10 (column 13) current flows: To terminal 56 on the top diode board (column 12), through a diode in diode pack 25 on the top diode board (column 11), to pin 161 on top diode board (column 9), through the X-winding to pin 12 on the top diode board (column 7), through a diode in diode pack 32 on the top diode board (column 6), to terminal 4 on the top diode board (column 3) to the X-read hi gate, E2B12 (column 2).

Likewise, it can be seen that X-write current flows from the X-write hi gate, S2D11 (column 4), in the reverse direction through the X-winding, to the X-write lo gate, D2J09 (column 15).

4.1.2.2.2 Locating an Open Diode: Because of the complex connections of the isolation diodes, a continuity check is difficult. To locate an open diode, use the method described next. The cards named are for the same failing X-address (000110) discussed in Section 4.1.2.2.1Fr. A14 Refer also to Figure 4-5.Fr. A17

1. Turn off power.

2. Remove X gate cards D2 and E2.

3. Probe the points shown with the ohmmeter; be sure to observe the polarity of the meter as indicated by the + or -. Expected meter readings are infinity (∞) or some resistance (R, unpredictable because of circuit variations and the meter in use).

An open or shorted drive line may also be verified by scoping the current source resistors. See Figure 4-16Fr. A18 for the waveform of the Y-read current source with either an open drive line or two drive lines shorted together (see SR264). If either is correct, an open diode is likely. Make a continuity check to determine which of the two diodes in the line is open.

If an open diode exists, the charts of SR174 and SR184 will indicate the polarity of the diode to be replaced. See the bottom of Figure 4-4 for diode locations with respect to the charts.

4.1.2.2.3 Replacing an Open Diode: An individual diode cannot be removed since it is part of a module containing 16 diodes. Replacement consists of soldering an individual GY diode (part 2414891) over the defective one. (A shorted diode calls for replacement of the BSM.)

When replacing a diode, use thermal set compound (part 814007) as a heat sink. Wrap one end of a yellow wire to the wrap terminal on the diode board and solder the other end to the diode. Solder the remaining end of the diode to the solderable pin on the edge of the diode board. After diode replacement, check for reliable BSM operation.

4.1.2.2.4 Exposing Bottom Diode Board: If an open Y-drive line exists and the fault cannot be located on the top diode board, remove the BSM to expose the bottom diode board.

1. Disconnect all cables to the BSM.

2. Remove all the cards.

3. Remove the BSM (weight–approximately 18 pounds) and lay the unit on a table with the card side down, pin side up.

4. Loosen the 4 nuts which hold the array onto the board. It is now connected by only the drives and sense-inhibit cables.

   Note: It is now possible to raise the board separately leaving the array resting on the table and expose the bottom diode board, or you may continue.

5. Turn the unit over. Support the array since it is connected only by wiring.

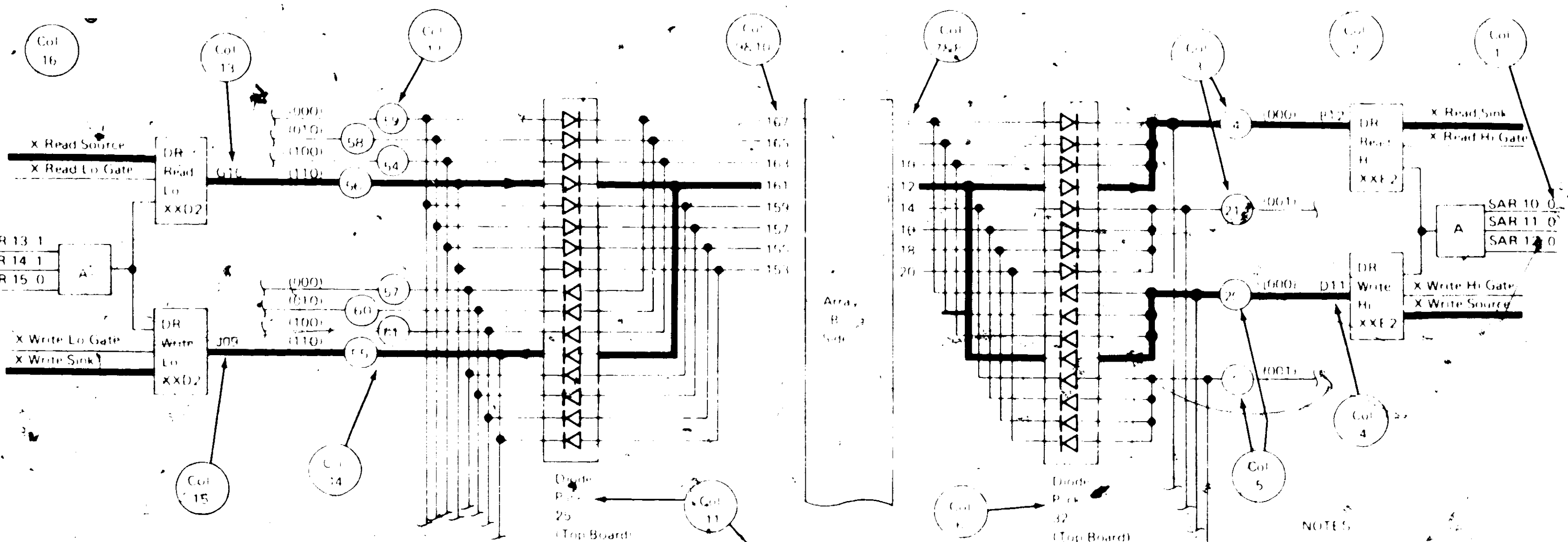
6. Pull the array out vertically and turn it over so that the top side is down and lying on the card sockets. The bottom diode board is now completely exposed.

4

4.1.2.2.5 BSM Replacement: Most systems supply -30 volts to the BSM with a single 'mini-bus' connector. (See SR264 for distribution points.) Earlier systems supplied -30V with jumpers on the board. This includes the associated D08 ground pins.

When replacing a BSM it is necessary to save the jumpers for use on the new BSM if your system does not use the 'mini-bus' connector.

For dual BSM systems some wiring changes to the new BSM may be required. Refer to the SR2XX pages in the BSM logic manual for card plug charts and wiring add/delete lists. Note that the new BSM is shipped without a byte control card and without the terminator cards. These cards must be removed from the old BSM and used with the new one. Any reference in these SR2XX pages to "1st BSM" means location 01A-B4 and "2nd BSM" means location 01A-A4.

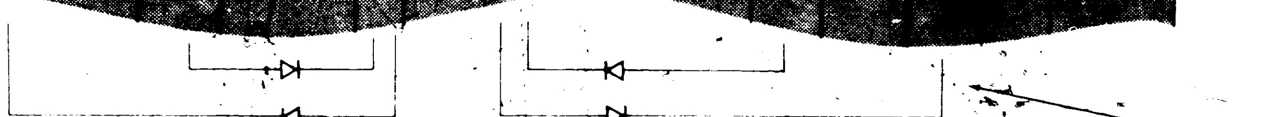


NOTES

1. Circled numbers refer to columns on chart.
2. Refer to chart for SR 184 for Y Drive Selection.
3. Refer to SR 204 224 for physical locations.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
HI ORDER										LOW ORDER					
HI ORDER ADDRESS	DRIVE LINE PINS				DIODE PACK HI ORDER TOP BOARD	CORE LINE GOING				DIODE PACK LOW ORDER TOP BOARD	DRIVE LINE PINS				LOW ORDER ADDRESS
	READ SINK		WRITE SOURCE			FROM		TO			READ SOURCE		WRITE SINK		
SAR BITS 10 11 12	LARGE BOARD	TOP DIODE BOARD	LARGE BOARD	TOP DIODE BOARD	PACK NO.	PIN NO.	ARRAY SIDE	PIN NO.	ARRAY SIDE	PACK NO.	TOP DIODE BOARD	LARGE BOARD	TOP DIODE BOARD	LARGE BOARD	SAR BITS 13 14 15
	L2B12	4	L2D11	20	32	12	B	161	B	25	56	D2G10	55	D2J09	1 1 0

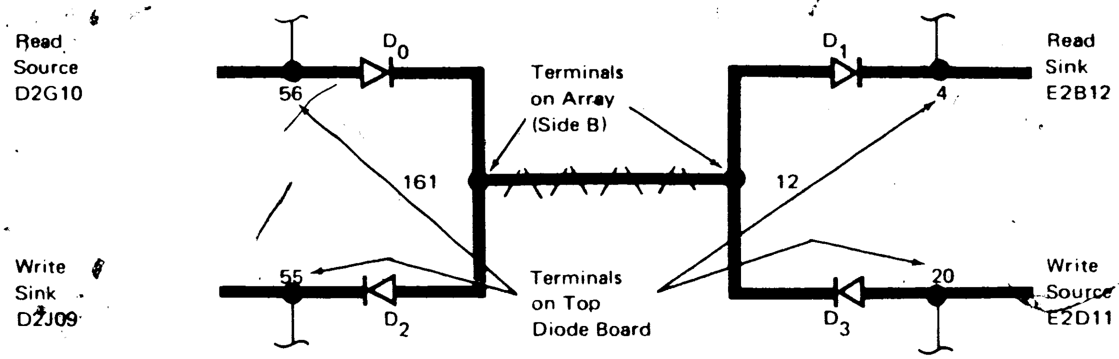
SR 174



5098B

Figure 4-4. X-Drive Selection

Example: Locating an open diode associated with the failing X-address of 000110 (SAR Bits 10-15)



IMPORTANT: Remove X-Gate Cards D2 and E2

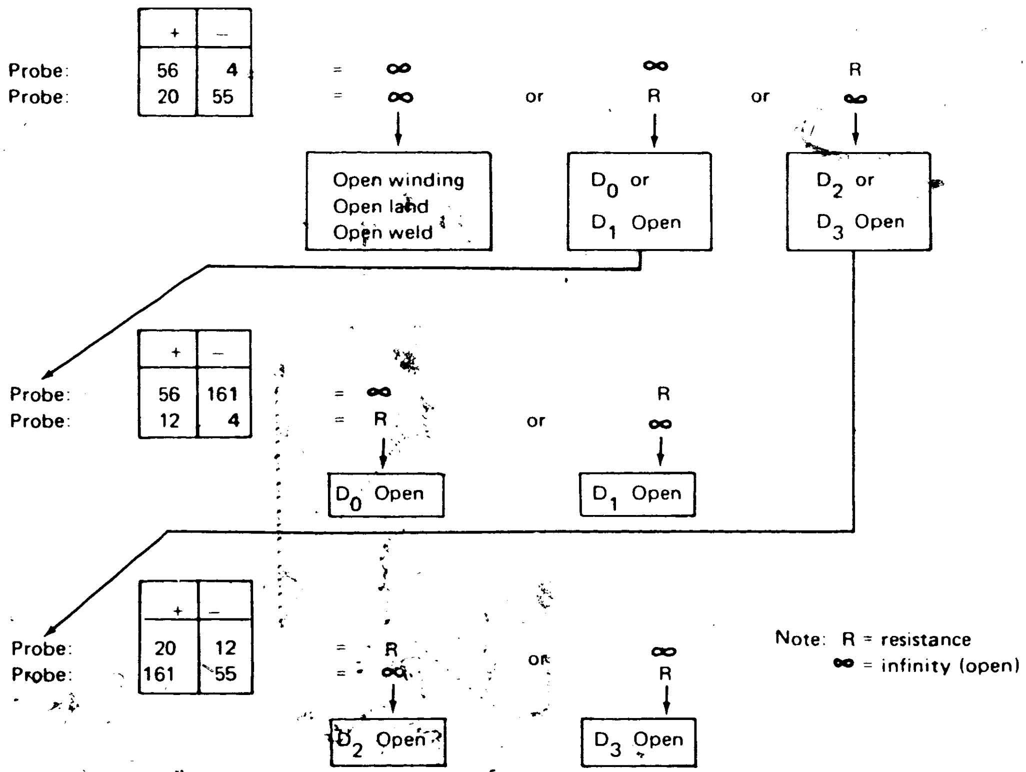


Figure 4-5. Example-Locating an Open Diode (8K or 16K BSM)

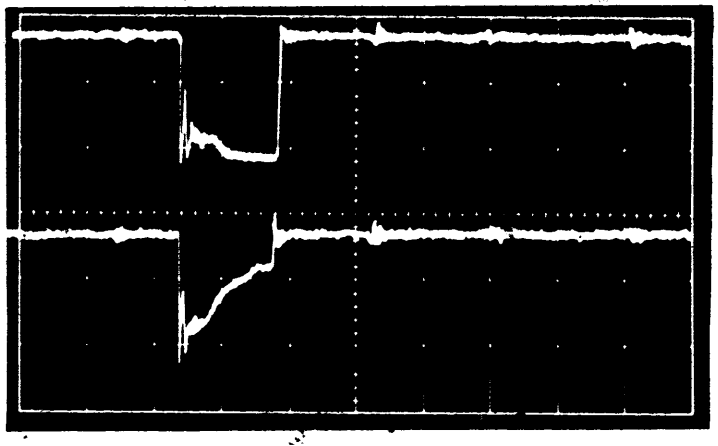
4

Switch Name	Setting
CE Mode Selector	Alter Storage
Storage Test	Run
Address Increment	Off

OPEN DRIVE LINE

This is a composite picture which shows a good drive line, and an open drive line (broken weld in array).

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset



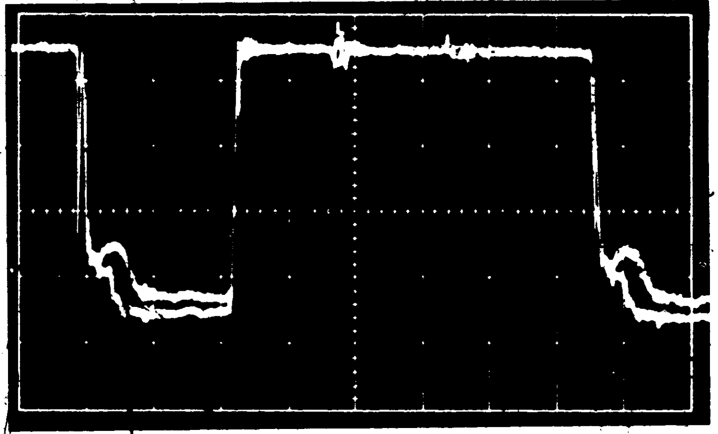
Good drive line measured at 10 V/cm
B4J2D05 (8K-16K BSM)
B4K2D05 (32K BSM)
'Y Read Current Source Resistor'

Open drive line measured at 10 V/cm
B4J2D05 (8K-16K BSM)
B4K2D05 (32K BSM)
'Y Read Current Source Resistor'

This is a double exposure picture. The highest down level shows a good drive line. The lowest down level shows 2 drive lines shorted together.

Note: These points are in series with the current source transformer primary therefore indirectly shows the failure.

SHORTED DRIVE LINE



5 V/cm
B4J2D05 (8K-16K BSM)
B4K2D05 (32K BSM)
'Y Read Current Source Resistor'

*Ground

Figure 4-16. BSM Waveforms

Duplicated Illustration

4.1.2.3 Poor Solder Connections and Welds

If a problem appears to be an open diode or an internal open within the array, a complete resistance check should be made. Any poor solder connections or welds should be resoldered.

Also check for an open land pattern in the X-return card (for an X-drive line). If there is an open land pattern, use a piece of #30 wire to repair the break.

See the *5410 Service Aid* on resoldering the connections.

4.1.2.4 Shorts Between Drive Lines

Shorts between X- or Y-drive lines usually show up as dropping one or more bits of two addresses. In almost all cases, analysis of the failing addresses shows that two adjacent X- or Y-drive lines are the problem. Once the two lines have been located, make a resistance check of the lines, moving from one end of the array to the other. Because of the resistance of the windings, less resistance is seen as you get closer to the short.

In almost all cases, the short is either some foreign material between two adjacent pins or two pins touching. A visual check with a strong light may show the short. However, if foreign material is causing the short, it may not be visible. Try passing a piece of paper between the pins at the area of the short.

4.1.2.5 Defective Cores

A defective core position usually shows up as dropping a single bit in a single address. This type of problem can be caused by the individual core losing its magnetic properties because it is cracked, chipped, or broken.

Vary the -30V drive voltage and the strobe setting to see if the rate of failure changes. If you are unable to obtain a reliable operating position, BSM replacement is necessary. See Sections 4.2 and 4.3 **Fr. B02** for drive voltage and strobe reoptimization.

4.1.3 Intermittent or Random Failures

If a failure pattern cannot be determined, check the following for possible failures causes:

1. Using an oscilloscope, probe the:

   a. XY drive voltage pulses on the XY read and write current source resistors and compare them to those in Figures 4-7, **Fr. B04** 4-8, **Fr. B05** 4-9, **Fr. B06** and 4-10. **Fr. B07**

   Note: Probe pins 1 and 3, which are common. No pulse will be observed on resistor pin 2, since it is ground.

   b. Z drive voltage pulses on the Z (inhibit) current limiting resistors and compare them to those shown in Figure 4-11. **Fr. B08**

   Note: No pulse is observed on resistor pin 2 since it is the -30V power supply connection. Note also that the magnitude of the pulses may vary slightly if the XYZ drive voltage setting is not at -30V. (XYZ drive voltage supply is a temperature correcting supply.)

   c. Control driver (Figure 4-12). **Fr. B09**

   d. Strobe driver (Figure 4-13). **Fr. B10**

   Note: If the strobe driver card is replaced, strobe jumpers must be put in the new strobe driver card.

2. Check for improper setting of the -30V, +6V, -4V, -14V, and/or +3V. (Use a Weston* 901 meter or equivalent when adjusting these voltages.)

   Note: The +3V supply should be adjusted with reference to +6V. This results in a negative reading (Section 5.2.1). **Fr. B15**

3. Check the voltage connectors to the large circuit board (SR264).

4. Check if back panel resistor assemblies (not XYZ resistors) are misplugged (SR264).

5. Check for loose interface cables or terminator cards (SR201, 224, 228, 229).

6. Check for improper MST-1 levels at the interface.

*Trademark of Weston, Inc.

4.2 XYZ DRIVE VOLTAGE (-30V) REOPTIMIZATION (ALL SYSTEMS)

Reverify drive voltage marginal limits whenever replacing S/Z, timing, driver source, or strobe driver cards.

To reoptimize the drive voltage:

1. Loop storage diagnostics # 97. (Use the proper switch settings for the storage size of the system.)

2. Determine the lower drive voltage (−30V) limit by slowly decreasing the drive voltage reading until an error occurs. Record the last operating voltage as the lower limit. If system reset and start does not start the diagnostic, set the drive voltage close to normal and reload the diagnostic. Determine the upper limit by slowly increasing the voltage reading until an error occurs (do not exceed a more negative voltage than −35V). Record the last operating voltage (or −35V) at the upper limit.

   Note: The BSM should run error free for a minimum of 30 seconds at the last operating point.

3. Set the XYZ drive voltage (−30 volts) to the optimum drive voltage which is the average of the upper and the lower BSM limits.

4. If the difference between the upper and lower limits is less than 2.4V, strobe reoptimization may be necessary.

Note: When reoptimizing the drive voltage or strobe setting, a thermometer (part 5392366 or any standard thermometer) placed at the base of the array should read between 68 degrees and 86 degrees F. The voltage may be reoptimized outside of this range, but a check at the normal temperature should be made as soon as possible.

4.3 STROBE SETTING REOPTIMIZATION (8K-16K-32K SINGLE BSM)

To reoptimize the strobe setting:

1. Loop storage diagnostics #97. (Use the proper switch settings for the storage size of the system.)

2. Refer to the decal on the XYZ current limiting resistor cover (Figures 4-1, 4-2, 4-2B). **Fr. A12** Use the present strobe setting, and determine the upper and lower XYZ drive voltage limit, which is explained by 4.2, step 2. Record these limits as Figure 4-6 **Fr. B03** point A and B show. Repeat 4.2 step 2 for strobe setting 10, 20, and 30 nanoseconds before and after the present strobe setting. Strobe settings are made on the strobe driver card (SR254).

   Note: These test settings may be wirewrapped on the strobe card but the final setting *must* be made with the jumpers (part 5159491) because the card pins are not 'squared off' as they must be for reliable wirewrap connections.

   Plot the XYZ drive voltage limits as Figure 4-7 **Fr. B04** shows. Set final strobe timing midway between points where the XYZ driver voltage limits start to drop off.

3. Set the optimum drive voltage (−30V) which is the average of the upper and lower BSM limits at the selected strobe setting (Figure 4-6). **Fr. B03**

4. BSM access time is measured when Rd Call/Write Call becomes active in the BSM until all sense data latches are active. (Measure access time while writing all ones into the BSM.) Access time must be 445 nanoseconds or less. If necessary, reset the strobe setting to obtain 445 nanoseconds or less. The minimum 2.4V spread for XYZ voltage must still be met at the new setting.

Note: If the strobe driver card is replaced, strobe jumpers must be put in the new strobe driver card.

4

4.4 STROBE SETTING REOPTIMIZATION (24-32K-48K DUAL BSM)

1. Optimize low-address BSM (1st BSM at location 01A-B4) as described in 4.3, Fr. B02 with the switches set to test only the lower (01A-B4) BSM. (This BSM is either 16K or 32K depending on the total system memory size.)

2. Optimize high-address BSM (2nd BSM at location 01A-A4) as described in 4.3 Fr. B02 using the program 97 option which tests only the high BSM.

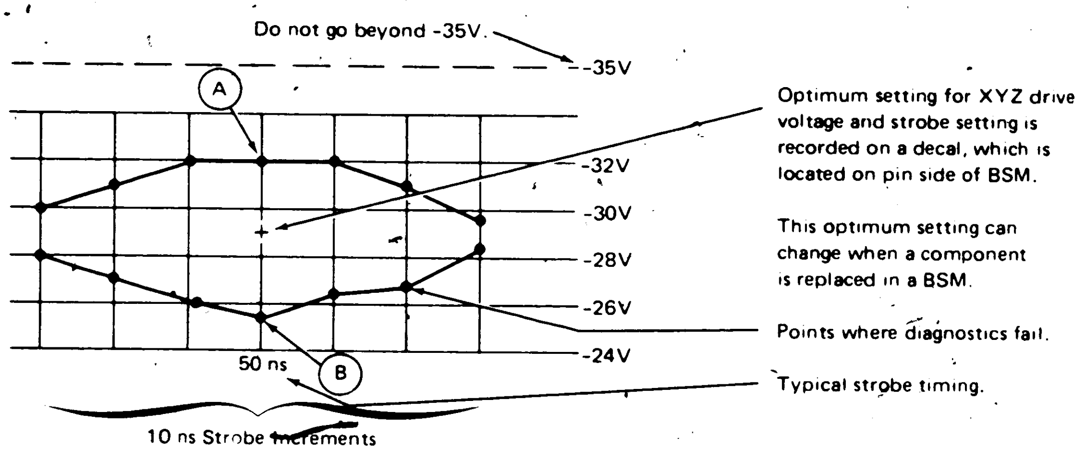


Figure 4-6. Optimization–Strobe and XYZ Drive Voltage

4.5 STROBE SETTING REOPTIMIZATION (64K DUAL BSM; RPQ 540048)

1. Optimize the low-address BSM (at location 01A-A4) as described in Section 4.3 Fr. B02 with the program switches set to test 32K storage addresses.

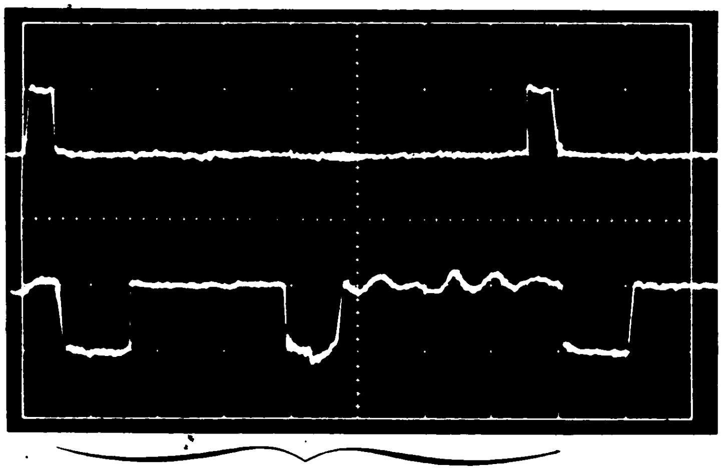
2. Jumper 01A-B3B2M08 to 01A-B3B2G03. This forces '2nd BSM select' to the active level.

3. Optimize the high-address BSM (at location 01A-A4) as described in Section 4.3 Fr. B02 with the program switches set to test 32K storage addresses.

4. Remove the jumper added in step 2.

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

RESET
and
RD CALL WR CALL



Sync:	Plus External
Time Base:	200ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset

Channel 1

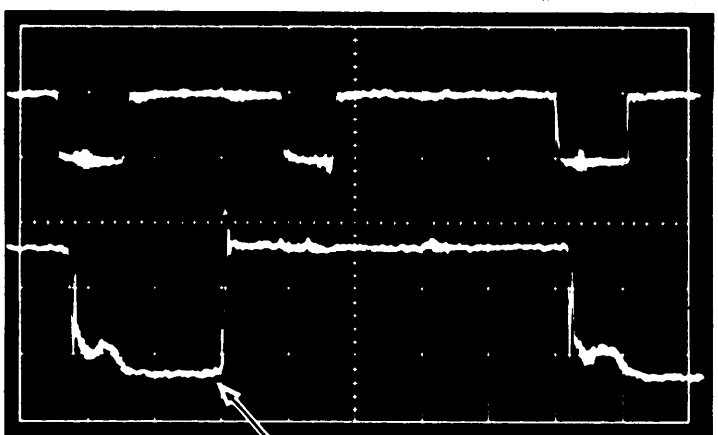
Vertical Gain:	1 V/cm
Signal Pin:	B4B3G03 (8K-16K BSM) B4B2G03 (32K BSM)
Signal Name:	Reset

Channel 2

Vertical Gain:	1 V/cm
Signal Pin:	B4A2B02 (8K-16K-32K BSM)
Signal Name:	Rd Call Wr Call

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

RD CALL WR CALL
and
X RD CURRENT SOURCE RESISTOR



Sync:	Plus External
Time Base:	200ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset

Channel 1

Vertical Gain:	1 V/cm
Signal Pin:	B4A2B02 (8K-16K-32K BSM)
Signal Name:	Rd Call Wr Call

Channel 2

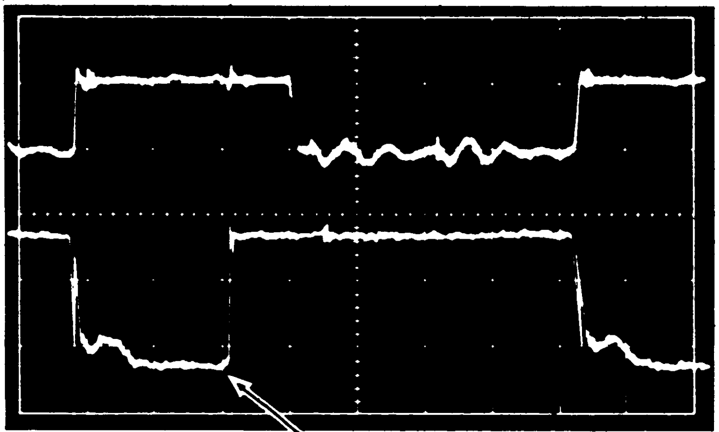
Vertical Gain:	10 V/cm
Signal Pin:	B4J2G05 (8K-16K BSM) B4K2G05 (32K BSM)
Signal Name:	X Rd Current Source Resistor

*Ground

Figure 4-7. BSM Waveforms

READ TIME
and
X RD CURRENT SOURCE RESISTOR

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

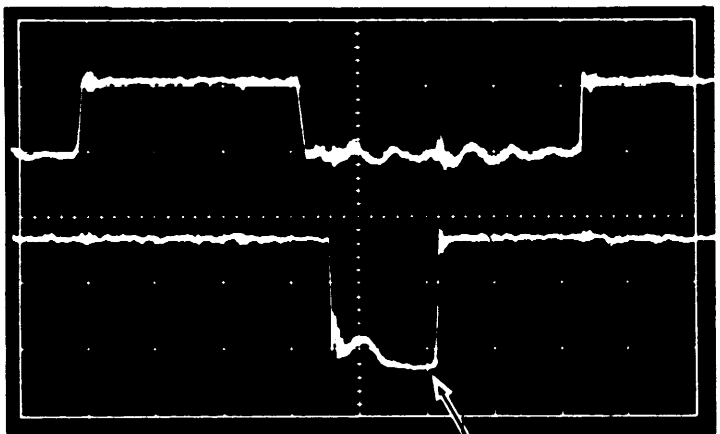


Lower level determined by -30Vdc setting

Sync:	Plus External
Time Base:	200ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset
Channel 1	
Vertical Gain:	1 V/cm
Signal Pin:	B4J2J13 (8K-16K BSM) B4K2J13 (32K BSM)
Signal Name:	Read Time
Channel 2	
Vertical Gain:	10 V/cm
Signal Pin:	B4J2G05 (8K-16K BSM) B4K2G05 (32K BSM)
Signal Name:	X Rd Current Source Resistor

READ TIME
and
X WRITE CURRENT SOURCE RESISTOR

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



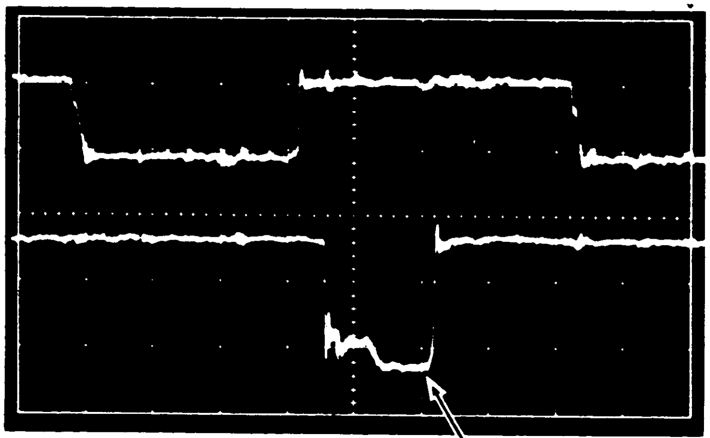
Lower level determined by -30Vdc setting

Sync:	Plus External
Time Base:	200ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset
Channel 1	
Vertical Gain:	1 V/cm
Signal Pin:	B4J2J13 (8K-16K BSM) B4K2J13 (32K BSM)
Signal Name:	Read Time
Channel 2	
Vertical Gain:	10 V/cm
Signal Pin:	B4J2J10 (8K-16K BSM) B4K2J10 (32K BSM)
Signal Name:	X Write Current Source Resistor

*Ground

Figure 4-8. BSM Waveforms

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



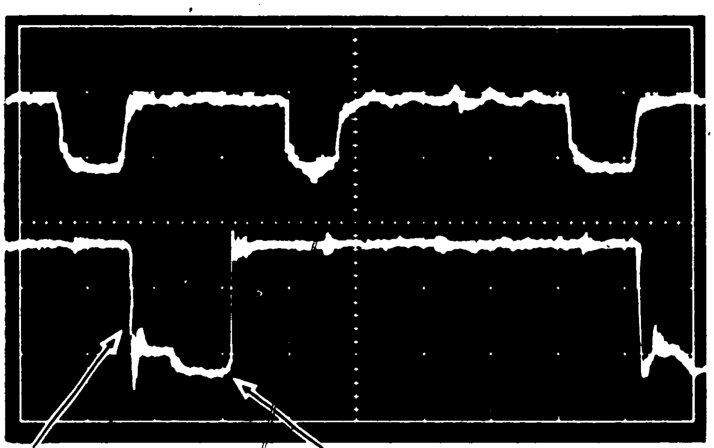
WRITE TIME
and
X WRITE CURRENT SOURCE RESISTOR

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4J2B03 (8K-16K BSM)
B4K2B03 (32K BSM)
Signal Name: Write Time

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J2J10 (8K-16K BSM)
B4K2J10 (32K BSM)
Signal Name: X Write Current Source Resistor

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



RD CALL WR CALL
and
Y READ CURRENT SOURCE RESISTOR

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4A2B02 (8K-16K-32K BSM)
Signal Name: Rd Call Wr Call

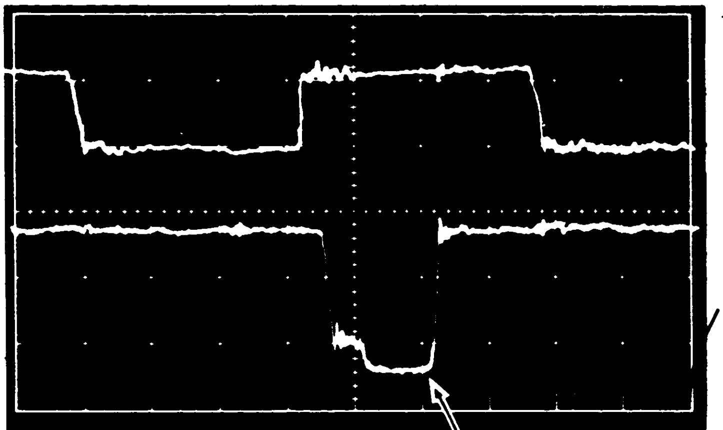
Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J2D05 (8K-16K BSM)
B4K2D05 (32K BSM)
Signal Name: Y Read Current Source Resistor

Figure 4-9. BSM Waveforms

4

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

WRITE TIME
and
Y WRITE CURRENT SOURCE RESISTOR



Lower level determined by -30Vdc setting

Sync:	Plus External
Time Base:	200ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset

Channel 1

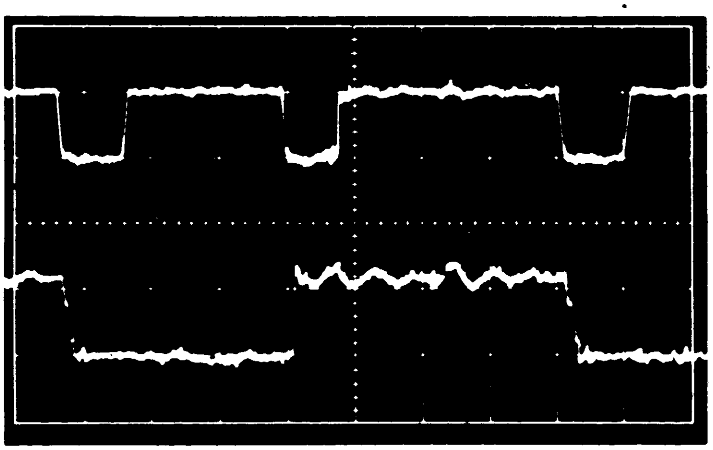
Vertical Gain:	1 V/cm
Signal Pin:	B4J2B03 (8K-16K BSM)
	B4K2B03 (32K BSM)
Signal Name:	Write Time

Channel 2

Vertical Gain:	10 V/cm
Signal Pin:	B4J2D07 (8K-16K BSM)
	B4K2D07 (32K BSM)
Signal Name:	Y Write Current Source Resistor

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

RD CALL WR CALL
and
WRITE TIME



Sync:	Plus External
Time Base:	200ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset

Channel 1

Vertical Gain:	1 V/cm
Signal Pin:	B4A2B02 (8K-16K-32K BSM)
Signal Name:	Rd Call Wr Call

Channel 2

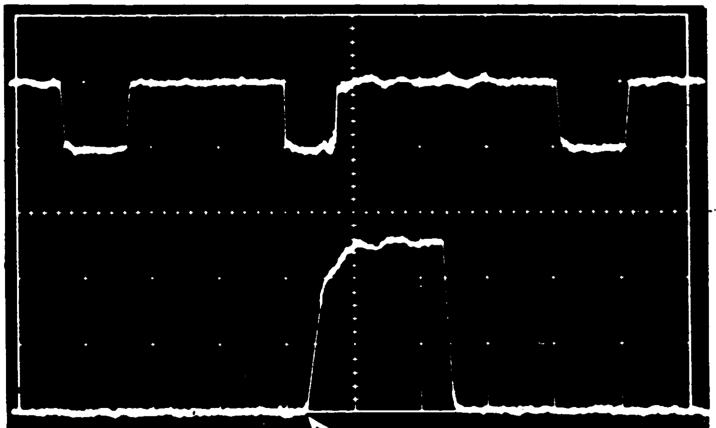
Vertical Gain:	1 V/cm
Signal Pin:	B4J2B03 (8K-16K BSM)
	B4K2B03 (32K BSM)
Signal Name:	Write Time

*Ground

Figure 4-10. BSM Waveforms

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

RD CALL WR CALL
and
Z LOAD BIT 0

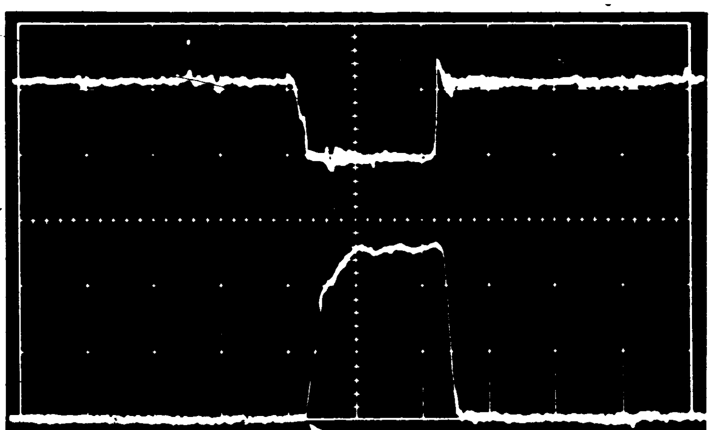


Lower level determined by -30Vdc setting

Sync:	Plus External
Time Base:	200ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset
Channel 1	
Vertical Gain:	1 V/cm
Signal Pin:	B4A2B02 (8K-16K-32K BSM)
Signal Name:	Rd Call Wr Call
Channel 2	
Vertical Gain:	10 V/cm
Signal Pin:	B4J4G10 (8K-16K BSM) B4K4J07 (32K BSM)
Signal Name:	Z Load Bit 0

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

INHIBIT BYTE 1
INHIBIT A BITS 0-5
INHIBIT B BITS 0-5
and
Z LOAD BIT 0



*Ground

Lower level determined by -30Vdc setting

Sync:	Plus External	
Time Base:	200ns/cm	
Sync Pin:	B4A1D11	
Signal Name:	Reset	
Channel 1		
Vertical Gain:	1 V/cm	
Signal Pin:	B4J4G04	8K-16K BSM
Signal Name:	Inhibit Byte 1	8K-16K BSM
Signal Pin:	B4K4J04	32K BSM
Signal Name:	Inhibit A Bits 0-5	32K BSM
Signal Pin:	B4K4G07	32K BSM
Signal Name:	Inhibit B Bits 0-5	32K BSM
Channel 2		
Vertical Gain:	10 V/cm	
Signal Pin:	B4J4G10 (8K-16K BSM) B4K4J07 (32K BSM)	
Signal Name:	Z Load Bit 0	

Figure 4-11. BSM Waveforms

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

RD CONTROL
and
X RD LO GATE CTRL

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

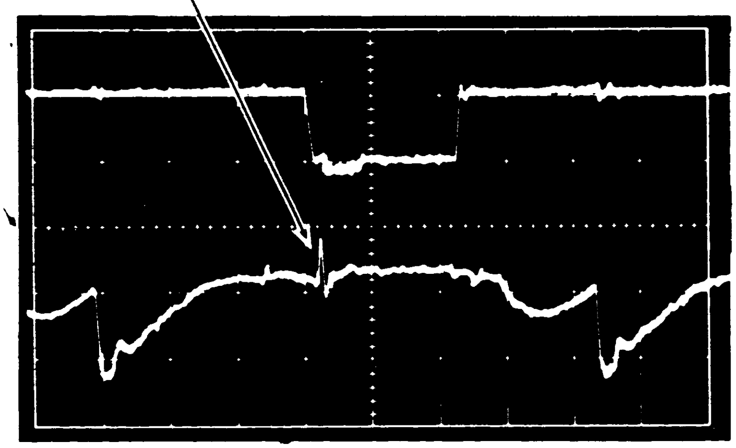
Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4B2B03 (8K-16K BSM)
B4C2B03 (32K BSM)
Signal Name: Rd Control

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4B2D10 (8K-16K BSM)
B4C2D10 (32K BSM)
Signal Name: X Rd Lo Gate Ctrl

X Rd or Y Wr Lo Gate Ctrl signal is shown for reference only. This is a current waveform and can be a different level at similar test points in a BSM, and can be a different level at the same test point and different BSMs.

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

WR CTRL
and
X WR LO GATE CTRL



Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4B2B04 (8K-16K BSM)
B4C2B04 (32K BSM)
Signal Name: Wr Ctrl

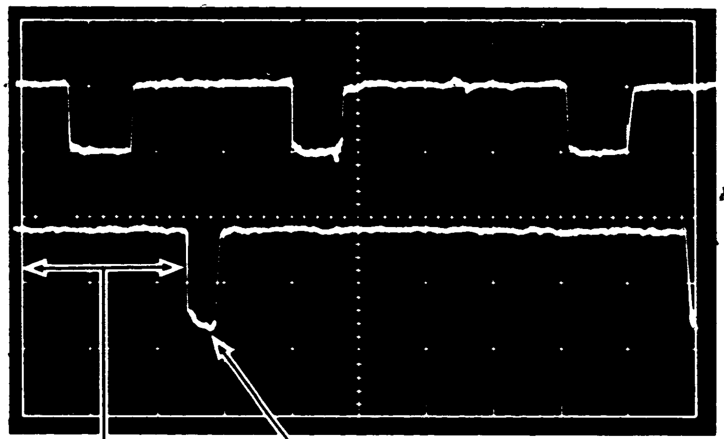
Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4B2D06 (8K-16K BSM)
B4C2D06 (32K BSM)
Signal Name: X Wr Lo Gate Ctrl

*Ground

Figure 4-12. BSM Waveforms

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

RD CALL WR CALL
and
STROBE BITS 0-8



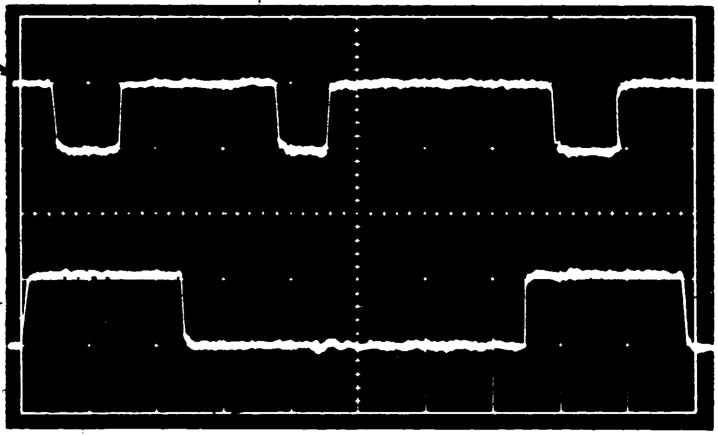
This time is determined by the BSM strobe card adjustment

For a 32K BSM this signal is about 25ns wider

Sync:	Plus External
Time Base:	200ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset
Channel 1	
Vertical Gain:	1 V/cm
Signal Pin:	B4A2B02 (8K-16K-32K BSM)
Signal Name:	Rd Call Wr Call
Channel 2	
Vertical Gain:	5 V/cm
Signal Pin:	B4B5D10 (8K-16K BSM) B4C3D10 (32K BSM)
Signal Name:	Strobe Bits 0-8

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'FF'
Storage Test	Run
Address Increment	On

RD CALL WR CALL
and
SENSE BIT 0



Sync:	Plus External
Time Base:	200ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset
Channel 1	
Vertical Gain:	1 V/cm
Signal Pin:	B4A2B02 (8K-16K-32K BSM)
Signal Name:	Rd Call Wr Call
Channel 2	
Vertical Gain:	1 V/cm
Signal Pin:	B4J4B05 (8K-16K BSM) B4K4D10 (32K BSM)
Signal Name:	Sense Bit 0

*Ground

Figure 4-13. BSM Waveforms

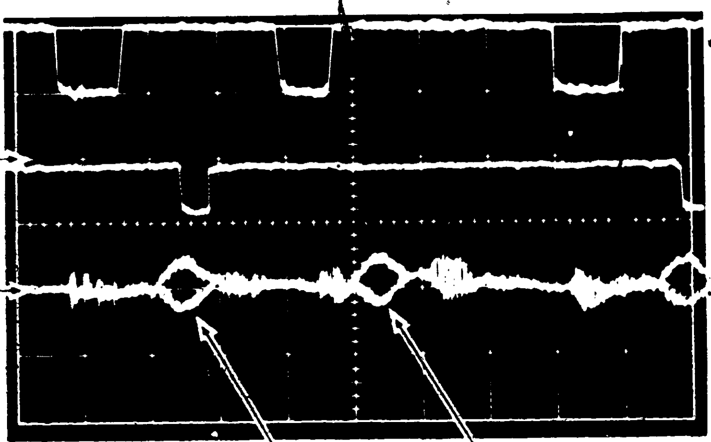
4

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'FF'
Storage Test	Run
Address Increment	On

CORE OUTPUT WRITING '1' IN ALL BIT POSITIONS

This is a 'three exposure' picture. 'Rd Call Wr Call', and 'Strobe' are shown only for time reference points.

Sync: Plus External
Time Base: 200 ns/cm
Sync Pin: B4A1D11
Signal Name: Reset



Ground

Ground

Rd Call Wr Call B4A2B02
1 V/cm (8K-16K-32K BSM)

Strobe Bits 0-8 B4J4B07 (8K-16K BSM)
10 V/cm B4C3D10 (32K BSM)

Core output writing '1' in all bit positions.
(Grounded)

Cores being changed from '0' to '1' at write time. Any one address can be positive or negative.

Cores being changed from '1' to '0' at read time. Any one address can be positive or negative.

Note: Core output measured with a Tektronix* 453 scope as follows.
Channel 1 and 2 set for 100 mV/cm
'Mode' switch set to 'Add'
Channel 2 'Invert' switch pull on
Channel 1 signal pin – B4J4B02 (8K-16K BSM)
B4K4B02 (32K BSM)
Channel 2 signal pin – B4J4D02 (8K-16K BSM)
B4K4D02 (32K BSM)

Figure 4-14 BSM Waveforms

*Trademark of Tektronix, Incorporated

BII

These are 'Three' exposure pictures. 'Rd Call Wr Call' and 'Strobe' are included for horizontal references.

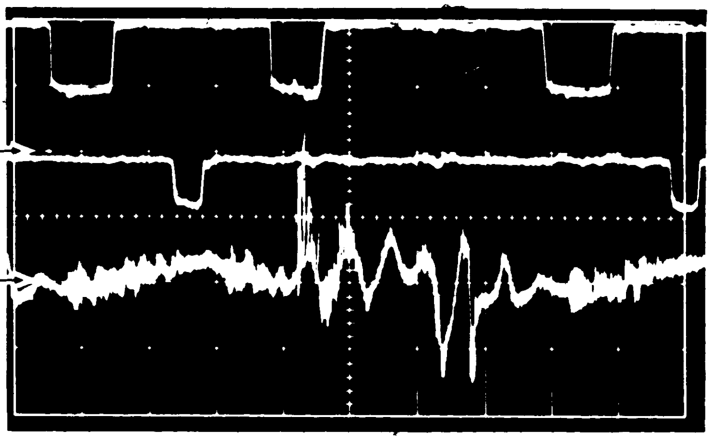
Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

CORE OUTPUT WRITING '0' IN ALL BIT POSITIONS

Sync:	Plus External
Time Base:	200 ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset

Ground

Ground



Rd Call Wr Call B4A2B02
1 V/cm (8K-16K-32K BSM)

Strobe Bits 0-8 B4J4B07 (8K-16K BSM)
10 V/cm B4C3D10 (32K BSM)

Core output writing '0' in all bit positions. See Note on Figure 4-14. Fr. B11

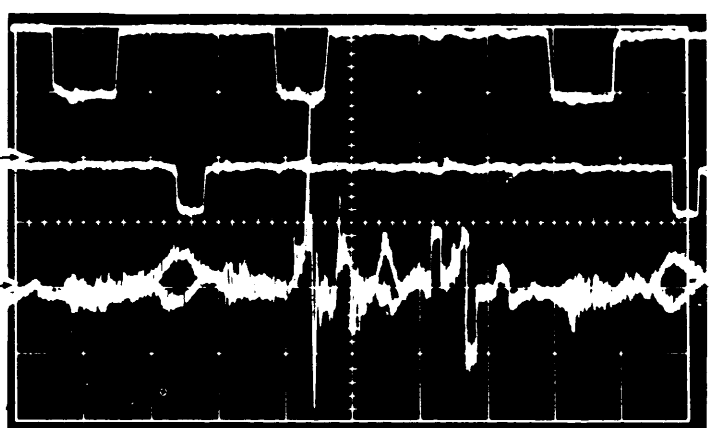
Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'80'
Storage Test	Run
Address Increment	On

CORE OUTPUT WRITING '1' IN THIS BIT POSITION AND '0' IN ALL OTHER BIT POSITIONS

Sync:	Plus External
Time Base:	200 ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset

Ground

Ground



Rd Call Wr Call B4A2B02 (8K-16K-32K BSM)
1 V/cm

Strobe Bits 0-8 B4J4B07 (8K-16K BSM)
10 V/cm B4C3D10 (32K BSM)

Core output writing '1' in this bit position and '0' in all other bit positions. See Note on Figure 4-14. Fr. B11

Figure 4-15. BSM Waveforms

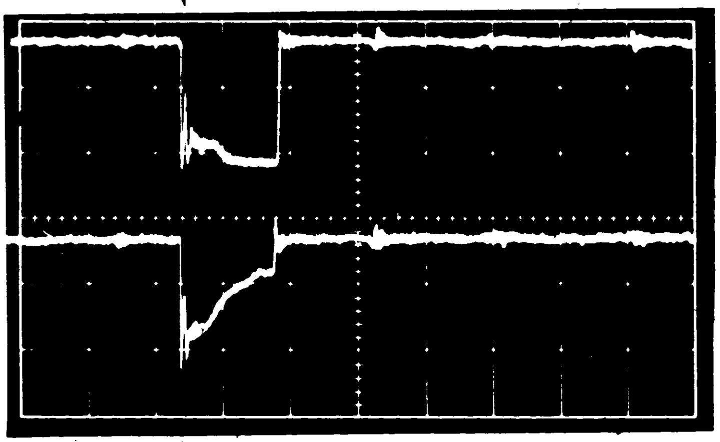
4

Switch Name	Setting
CE Mode Selector	Alter Storage
Storage Test	Run
Address Increment	Off

OPEN DRIVE LINE

This is a composite picture which shows a good drive line, and an open drive line (broken weld in array).

Sync:	Plus External
Time Base:	200 ns/cm
Sync Pin:	B4A1D11
Signal Name:	Reset



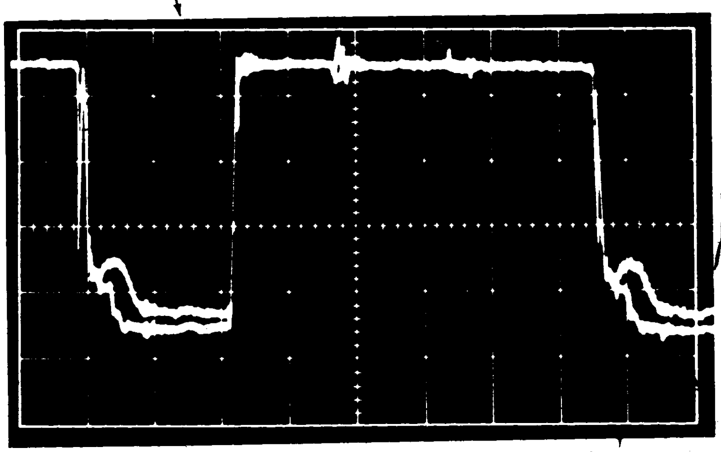
Good drive line measured at
10 V/cm
B4J2D05 (8K-16K BSM)
B4K2D05 (32K BSM)
'Y Read Current Source Resistor'

Open drive line measured at
10 V/cm
B4J2D05 (8K-16K BSM)
B4K2D05 (32K BSM)
'Y Read Current Source Resistor'

This is a double exposure picture. This highest down level shows a good drive line. The lowest down level shows two drive lines shorted together.

SHORTED DRIVE LINE

5 V/cm
B4J2D05 (8K-16K BSM)
B4K2D05 (32K BSM)
'Y Read Current Source Resistor'



*Ground

Figure 4-16. BSM Waveforms

B13

POWER
AND
COOLING

B14

Section 1. Basic Unit

Danger
After the emergency power switch is opened, power is available at K1, K3, and K9 input terminals and at transformer (T1) terminals. If the redesigned power control box is installed (printed circuit relay panel), power is not applied to the input terminals of K9 after an emergency power off.

Replacements of power supply components generally follow the replacement philosophy of the system; that is, replacement is limited to voltage regulator cards, fuses, and relays. However, in some cases it will be necessary to replace the series regulator and the filter capacitors.

5.1 INPUT POWER REQUIREMENTS

The input power requirements for System/3 are 3-phase power at 30A. Domestic and World Trade input voltage requirements are:

1. 60 Hertz–200 Vac, 208 Vac, and 230 Vac (± 10%).
2. 50 Hertz–200 Vac, 220 Vac, 235 Vac, 380 Vac, and 408 Vac (± 10%).
3. Procedures for converting 208 Vac input to 230 Vac input can be found in *5410 Logic*, page YA100.

5.2 POWER SUPPLY OUTPUTS

Figure 5-1 shows the power supply outputs, the location of each supply, and the primary use of each supply. The system supplies -30V, +6V, and -4V. The +6V and -30V generate (respectively) an internal BSM +3V and -14V. (The -30V is a temperature compensated drive voltage for use in the BSM.)

A BASIC SYSTEM SUPPLIES

Supply	Amperes	Where Used	Location
-4V	70A	Logic Voltage	CPU
+6V	15A	Logic Voltage	CPU
-30V	9.5A	Storage	CPU
+24V	25A	MFCU	MFCU
+60V	11A	Printer, MFCU	Printer
+24V	5A	Control Voltage	CPU
+3V		Storage*	CPU
-14V		Storage*	CPU
7.25 Vac	**	Indicator Lamps	CPU
41 Vac		Use Meter***	CPU

* +6V supply voltage dropped to +3V in storage module. -30V supply voltage dropped to -14V in storage module. (See Figure 5-2 for card locations.) Fr. B16

** 25A in early design machines, 16A in redesigned power control box only.

*** Applies to redesigned power control box only.

B FEATURE SUPPLIES

Supply	Where Used	Location
-12V	BSCA	CPU
-3V	1442	CPU
+3V	1442	CPU
+6V*	Special Features	CPU

*Replaces 15A logic voltage supply when installed.

Figure 5-1. Power Supply Outputs

5.2.1 Checks and Adjustments

All voltage measurements should be made in a normal environment (temperature between 68 degrees and 86 degrees F) with a *recently calibrated* Weston 901 meter or its equivalent.

BSM +3 Volt and -14 Volt Supplies

Determine the CPU storage capacity and storage configuration before checking or adjusting the +3V or the -14V power supply (Figure 5-2).

The +3 V supply used by BSM is adjusted by connecting the meter leads to the test points (Figure 5-2). Then adjust potentiometer on the upper half of the BSM power-supply card. The +3V is set by referencing it to the +6V supply (meter reading will be +3V).

The -14 V supply used by BSM is adjusted by connecting the meter leads to the test points (Figure 5-2). Then adjust the potentiometer on the lower half of the BSM power supply card.

See paragraphs 5.5 **Fr. C02** and 5.6 **Fr. C03** for the adjustment of the -4V and +6V supplies. See paragraph 4.2 **Fr. B02** for the adjustment of the -30V supply.

5.2.2 Power Supply Unloading Procedures

Figure 5-3 represents each power supply regulator in System/3. Each terminal shown serves the same function on all the regulators in the system. The only difference is the applied input voltage (E1 to E2) and the resulting output voltages (E3 to E4).

Terminal point E8 receives an error output signal which causes the system to power down immediately. An overcurrent, overvoltage, or undervoltage condition generates the signal. Removal of terminal E8 wires prevents the system from detecting a power supply failure. To prevent possible component damage, avoid removing any wires from E8.

Terminal point E12 serves as the start connection to a regulator. In the unloading procedures that follow the removal of wires from terminal E12 prevents start up for a particular regulator.

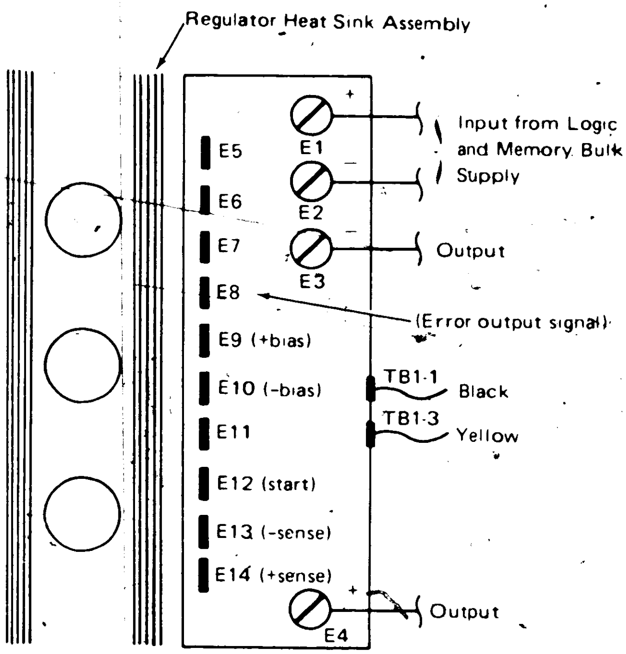


Figure 5-3 Power Supply Regulator

BSM Sizes Required		Installed CPU Storage Capacity and Configuration							Test Points			
		8K	12K	16K	24K	32K	48K	64K	+3 Volts		-14 Volts	
									Minus	Plus	Minus	Plus
8K BSM		X			X				01A-B4C4J03	01A-B4C4B11	01A-B4C4J11	01A-B4C4G08
16K BSM	1st BSM		X	X		X and	X		01A-B4C4J03	01A-B4C4B11	01A-B4C4J11	01A-B4C4G08
	2nd BSM				X or	X or	and		01A-A4C4J03	01A-A4C4J03	01A-A4C4J11	01A-A4C4G08
32K BSM					X	X	X	2	01A-B4A4J03	01A-B4A4B11	01A-B4A4J11	01A-B4A4G08

● Figure 5-2 BSM +3V and -14V Storage Capacity and Supply Test Points

5.2.2.1 -4 Volt Regulator Unloading

Caution
Never turn on power with the -4V regulator unloaded unless the correct jumpers are installed. Otherwise, component damage to the 5424 or 5203 may result if +6V is applied to the attachment board of these devices (A-B1 and A-A3 boards) without -4V.

Danger
When the -4V regulator is unloaded the bulk supply may go into oscillations. This may cause the resonant capacitor in the bulk supply to explode. Limit power on time with the regulator unloaded to 30 seconds, keep the bulk supply cover on, and wear safety glasses.

To unload the -4V regulator **on the basic machine:**

1. Turn off power.
2. Remove ac connectors J2 and J3 from base of CPU.
3. Remove all cables from E3 and E13.
4. Install jumper from E3 to E13.
5. Turn on power and make power checks.

To unload the -4V regulator when the -4V **add-on regulator** is installed:

1. Turn off power.
2. Remove ac connectors J2 and J3 from base of CPU.
3. Remove all cables from E3, E4, E12, E13, and E14.
4. Remove all cables from E2 of -4V add-on regulator.
5. Install jumpers:
   E4 to E14
   E3 to E13 (on both regulators)
   E12 to E14
6. Turn on power and make power checks.

Because the above procedure prevents the +6V and the -30V supplies from sequencing up, the power check light is on.

5.2.2.2 +6 Volt Regulator Unloading

Caution
Never turn on power with the +6V regulator cables removed unless the correct jumpers are installed. Otherwise, damage to the CPU BSM results if the BSM receives -30V without +6V.

To unload the +6V regulator:

1. Turn off power.
2. Remove ac connectors J2 and J3 from base of CPU.
3. Remove E4, E12, E14, and TB1-3 (-4V UV 'ax drive' line).
4. Install jumpers:
   E4 to E14
   E12 to E14
5. Turn on power and make power checks.

Because the above procedure prevents the -30V supply from sequencing up, the power check light is on.

5.2.2.3 -30 Volt Regulator Unloading

To unload the -30V regulator:

1. Turn off power.
2. Remove ac connectors J2 and J3 from base of CPU.
3. Remove all cables from E3.
4. Remove cables from terminal position 8 on A gate lower laminar bus (adjacent to A-B4).
5. Install jumper from E3 to E13.
6. Turn on power and make power checks.

Because the above procedure prevents the +60V supply from sequencing up, the power check light is on.

5

5.3 POWER SEQUENCING

The +24V control voltage controls power sequencing. The power supplies sequence up:

1. -4V basic logic voltage. (If installed, the -4V add-on regulator and the -4V logic supplies #2 [Feature] and #3 [Feature] also come on at the same time.)
2. +6V logic voltage
3. -30V storage supply voltage
4. +24V (5424) and +60V (5203) supplies

Refer to diagrams 6-005 and 6-010 (for early design power control); diagrams 6-015 and 6-020 (for the redesigned power control) in *IBM 5410 Processing Unit Diagrams*, SY31-0202, for power-on sequencing.

5.4 ADJUSTMENT OF THE -4 VOLT POWER SUPPLY

Caution
Check the overcurrent adjustment whenever replacing a -4V regulator card.

5.4.1 Overcurrent Adjustment

5.4.1.1 For Regulator Card Part 5808959 (See Figure 5-4 for Identification)

1. Connect the meter across the 4V load between brass plate #2 (-4V) and brass plate #1 (ground) behind the CPU console.
2. Set the voltage adjustment potentiometer (Figure 5-4) Fr. C01 to -4.6V. Do not go beyond this. Turn the over current potentiometer counter clockwise until the machine powers down. (If you cannot reach -4.6V before the regulator trips, turn the overcurrent adjustment clockwise until you can just reach -4.6V before the regulator trips.)
3. When the overcurrent adjustment trips, the machine will power down.
4. Turn the voltage adjustment potentiometer down until the machine can be powered up. The overcurrent adjustment is now correct.
5. Adjust the voltage adjustment potentiometer (5.4.2).

5.4.1.2 For Regulator Card Part 5860519 (See Figure 5-4 Fr. C01 for Identification)

No adjustment for overcurrent protection is necessary.

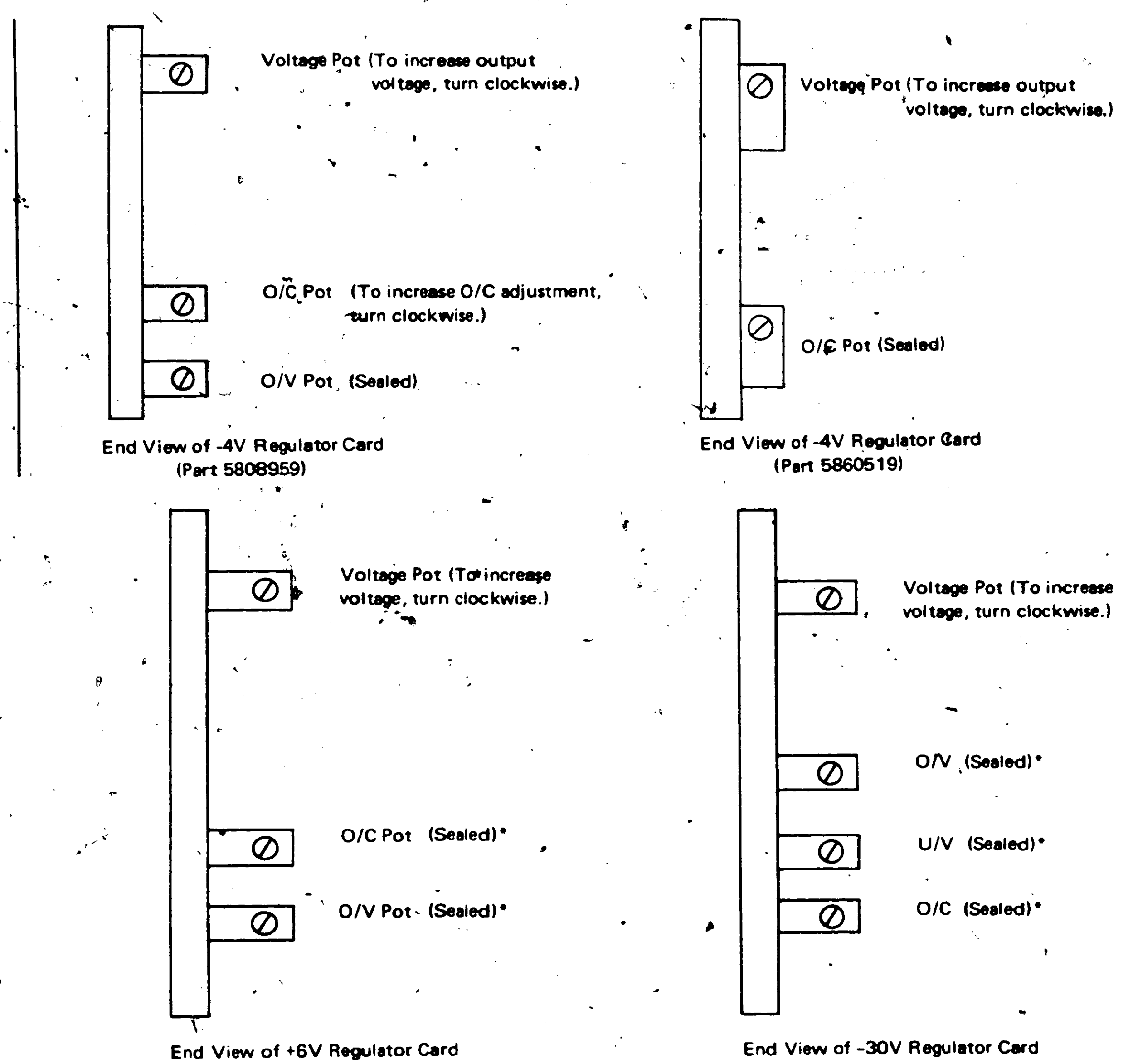
5.4.2 Voltage Adjustment

1. Connect meter between brass plate #2 (-4V) and brass plate #1 (ground) behind the CPU console.
2. Set voltage for -4.15V.
3. Connect meter across A-A3C2B06 (-4V) and A-A3C2D08 (ground). This voltage should fall between -3.85V and -4.15V.
4. Connect the meter across PEBTB 2-7 (ground) and PEBTB 2-8 (-4V) on the printer electronics gate. This voltage should measure between -4.15V and -3.85V.
5. If voltage measured in either step 3 or step 4 is out of tolerance, readjust the -4V supply.

5.4.3 Overvoltage Adjustment

There is no field adjustment for overvoltage. It is set and sealed at the time of manufacture. Replace -4V regulator card if overvoltage condition fails to trip regulator. (Be sure to check the overcurrent adjustment.)

CONTINUED ON FRAME C01



*These potentiometers are not on the redesigned power supplies.

Figure 5-4. Regulator Card

5

C01

5.4.4 Undervoltage Adjustment

There is no field adjustment for undervoltage detection. It is set and sealed at the time of manufacture.

Note: A -4V supply undervoltage condition (less than -3.5V) results in a +6V supply failure indication (TP13 = +24V, Figure 5-5).

5.5 ADJUSTMENT OF THE +6 VOLT POWER SUPPLY

5.5.1 Voltage Adjustment

1. Connect meter between brass plate #3 (+6V terminal) and brass plate #1 (ground terminal) behind the CPU console.

2. Set voltage adjustment potentiometer (Figure 5-4) for +6V. Fr. C01

   Note: This adjustment has no plus or minus tolerance. Set as close to +6V as possible.

5.5.2 Overvoltage–Overcurrent Adjustment

There are no field adjustments for overcurrent or overvoltage in this power supply. They are set and sealed at the time of manufacture. Replace +6V regulator card if overcurrent or overvoltage conditions fail to trip the regulator.

5.5.3 Undervoltage Adjustment

There is no field adjustment for undervoltage detection. It is set and sealed at the time of manufacture.

Note: A +6V supply undervoltage condition (5.28 Vdc) results in a +30V supply failure indication (TP14 = +24V Figure 5-5).

Test Point	Relay #	Type of Failure	Supply Checked
◎ TP 1	–	–	+24V Ground
◎ TP 2	K5	Sequence	-4V Basic logic supply (includes add-on)
◎ TP 3	K17	Sequence	-4V Logic supply #2 Feature (B gate)
◎ TP 4	K19	Sequence	-4V Logic supply #3 Feature (B gate)
◎ TP 5	K6	Sequence	+6V Basic
◎ TP 6	K8	Sequence	-30V Basic
◎ TP 7	K10	Sequence	+24V Basic (located in MFCU)
◎ TP 8	K11	Sequence	+60V Basic (located in 5203 Printer)
◎ TP 9	K30	Sequence	Feature P/S
◎ TP 10	K18	OV/OC	-4V Logic supply #3 Feature (B gate)
◎ TP 11	K16	OV/OC	-4V Logic supply #2 Feature (B gate)
◎ TP 12	K13	OV/OC	-4V Basic logic supply (includes add-on)
◎ TP 13	K14	OV/OC	+6V Basic
		UV	-4V Basic
◎ TP 14	K15	OV/OC	-30V Basic
		UV	+6V Basic

Read 24Vdc at TP2-9 when indicated voltage is missing.

Read 24Vdc at TP10-14 when indicated fault condition occurs. (24Vdc is present in TP2 also.)

Note: 24Vdc is normally at TP2 when CB-1 is on and the power on/off switch is off.

Figure 5-5. Power Supply Test Points

5.6 ADJUSTMENT OF THE -30 VOLT POWER SUPPLY

See paragraph 4.2 Fr. B02 for adjustment of the -30V power supply.

5.7 POWER CHECK LAMP

The power check lamp comes on during power on sequence and goes off when the power on sequence is completed. It also comes on when an overtemperature condition occurs or wherever any power trouble is present. (See Figure 5-6 for power check/thermal light characteristcs.) A power on reset occurs every time the power check lamp comes on. The power check lamp stays off if the 24 Vdc output of the control transformer/rectifier pack (T/R Pac) is missing. (Refer to Figure 5-5 Fr. C02 for test points (TPs) for the power system.)

The machine powers down in any of the conditions detected in TP10-14. Twenty-four volts will be readable in TP10-14 until a check reset switch is pressed. Loss of either the -4V or +6V while the machine is running powers down the system and 24V will be present at TP10-14 (Figure 5-5). Loss of -30V or +24V while the machine is running will not cause power down but the power on reset will stop operations of the machine.

If the power on sequence is not completed, the power check lamp will remain on and the TPs from TP2 to TP9 will indicate where the sequence stopped.

5.8 24 VOLT CONTROL VOLTAGE

If the 24 volt control supply is questionable when experiencing power on problems, a quick service check for this 24V supply can be made by pressing the lamp test switch while power is off and observing the thermal check and power check lights. If they light, the 24V supply is present.

FAULT	POWER ON/ OFF SWITCH	INDICATORS		ACTION
		POWER CHECK	THERMAL	
Internal Power Supply Malfunction	On	On	Off	1. Turn power off. 2. Correct problem. 3. Press check reset. 4. Turn power on.
Thermal Condition	On	On	On	1. Turn power off. 2. Power check indicator goes off. 3. Thermal light stays on until condition is removed.
Customer Power Source Loss	On	On	On	1. Turn power off. 2. All indicators turn off. 3. Turn power on and continue operation.
Emergency Power Off (EPO) Activated	On	Off	Off	1. Turn power off. 2. Correct problem. 3. Restore EPO interlock. 4. Turn power on.

Figure 5-6. Power Check/Thermal Check Indications

5

5.9 -4 VOLT ADD-ON REGULATOR

-4 Volt Regulator, Overcurrent and Overvoltage

When installing features or feature prerequisites on the A-gate, the overcurrent on the -4V regulator must be adjusted to a minimum of 15 percent over nominal load.

Caution
Check the overcurrent adjustment whenever replacing a -4V regulator card.

To adjust:

1. Increase the overcurrent adjustment until the system can be powered up.
2. Adjust overcurrent for the -4V power supply (5.4.1)Fr. B18
3. Adjust voltage for the -4V power supply (5.4.2)Fr. B18

5.10 B-GATE -4 VOLT LOGIC SUPPLY #2

5.10.1 Overcurrent Adjustment

5.10.1.1 For Regulator Card Part 5808959 (See Figure 5-4 Fr. C05 *for Identification)*

Caution
Check the overcurrent adjustment whenever replacing a -4V regulator card.

1. *Note:* The top screw on the upper laminar bus is position 10.

   Connect the meter across the -4V load between position 6 and ground (position 7) on B-gate upper laminar bus.
2. Set the voltage adjustment potentiometer (Figure 5-4)Fr. C05 to -4.6V. Do not go beyond this.
3. Turn the overcurrent potentiometer (Figure 5-4)Fr. C05 *counterclockwise* until the regulator trips to cause a power down. If you cannot reach -4.6V before the regulator trips, turn the overcurrent adjustment clockwise until you can just reach -4.6V before the regulator trips.
4. Turn the voltage adjustment potentiometer down until the machine can be powered up. Now the overcurrent adjustment is set.
5. Adjust the voltage adjustment potentiometer (5.10.2).

5.10.1.2 For Regulator Card Part 5860519 (See Figure 5-4 Fr. C05 *for Identification)*

No adjustment for overcurrent protection is necessary.

5.10.2 Voltage Adjustment

1. *Note:* The top screw on the upper laminar bus is position 10.

   Connect the meter across the -4V load between position 6 and ground (position 7) on B-gate upper laminar bus.
2. Set the voltage adjustment potentiometer (Figure 5-4)Fr. C05 to -4.05V.

5.10.3 Overvoltage Adjustment

There is no field adjustment for overvoltage. It is set and sealed at the time of manufacture. Replace regulator card if overvoltage condition fails to trip regulator. (Be sure to check the overcurrent adjustment.)

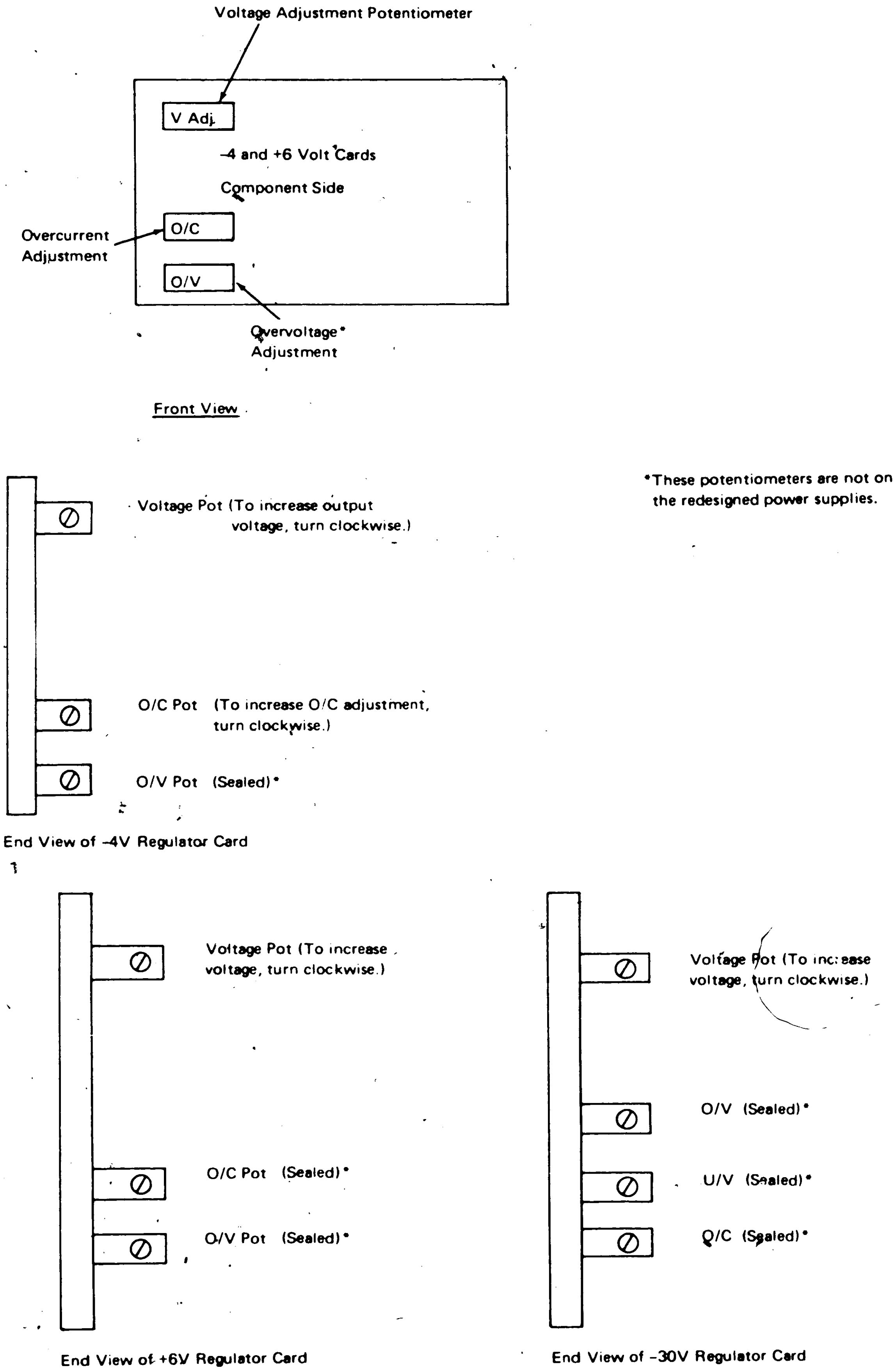


Figure 5-4. Regulator Card

Duplicated Illustration

5.11 B-GATE -4 VOLT LOGIC SUPPLY #3

5.11.1 Overcurrent Adjustment

5.11.1.1 For Regulator Card Part 5808959 (See Figure 5-4 Fr. C05 *for Identification)*

Caution
Check the overcurrent adjustment whenever replacing a -4V regulator card.

1. Connect the meter across the -4V load between position 6 and ground (position 7) on B-gate lower laminar bus.

2. Set the voltage adjustment potentiometer (Figure 5-4) Fr. C05 to -4.6V. Do not go beyond this.

3. Turn the overcurrent potentiometer (Figure 5-4, Fr. C05 *counterclockwise* until the regulator trips to cause a power down. If you cannot reach -4.6V before the regulator trips, turn the overcurrent adjustment clockwise until you can just reach -4.6V before the regulator trips.

4. Turn the voltage adjustment potentiometer down until the machine can be powered up. Now the overcurrent adjustment is set.

5. Adjust the voltage adjustment potentiometer (5.11.2).

5.11.1.2 For Regulator Card Part 5860519 (See Figure 5-4 Fr. C05 *for Identification)*

No adjustment for overcurrent protection is necessary.

5.11.2 Voltage Adjustment

1. Connect the meter across the -4V load between position 6 and ground (position 7) on B-gate upper laminar bus.

2. Set the voltage adjustment potentiometer (Figure 5-4) Fr. C05 to -4.05V.

5.11.3 Overvoltage Adjustment

There is no field adjustment for overvoltage. It is set and sealed at the time of manufacture. Replace regulator card if overvoltage condition fails to trip regulator. (Be sure to check the overcurrent adjustment.)

LOCATIONS

C07

Chapter 6. Locations

This chapter shows System/3 component locations in the following figures:

- Figure 6-1 – Shows access panels.
- Figure 6-2 **Fr. C09** – Shows CPU gate locations.
- Figure 6-3 **Fr. C09** – Shows power supplies in the CPU for the early design power control.
- Figure 6-4 **Fr. C10** – Shows power supplies for the redesigned power control.
- Figure 6-5 **Fr. C11** – Shows the number 1 logic and memory bulk supply for both the early design and the redesigned power control.

Figure 6-6 **Fr. C12** – Shows the keys, switches, and indicator locations on the CE control panel.

ACESS PANEL	
Area	**Panel**
CPU, memory and attachment	A
MFCU–mechanical	D
electrical	E, F
Printer–mechanical	G
PCB electrical	H
PEB electrical	I
Power Supplies +60 Vdc	H
–4 Vdc +6 Vdc	A or B
+6 V Expansion	J
Memory	A or B
BSCA +24 Vdc	E
Med Speed – 12 Vdc	J
Console	C
Cables	F
Power Control Board	J, A
Documents	K

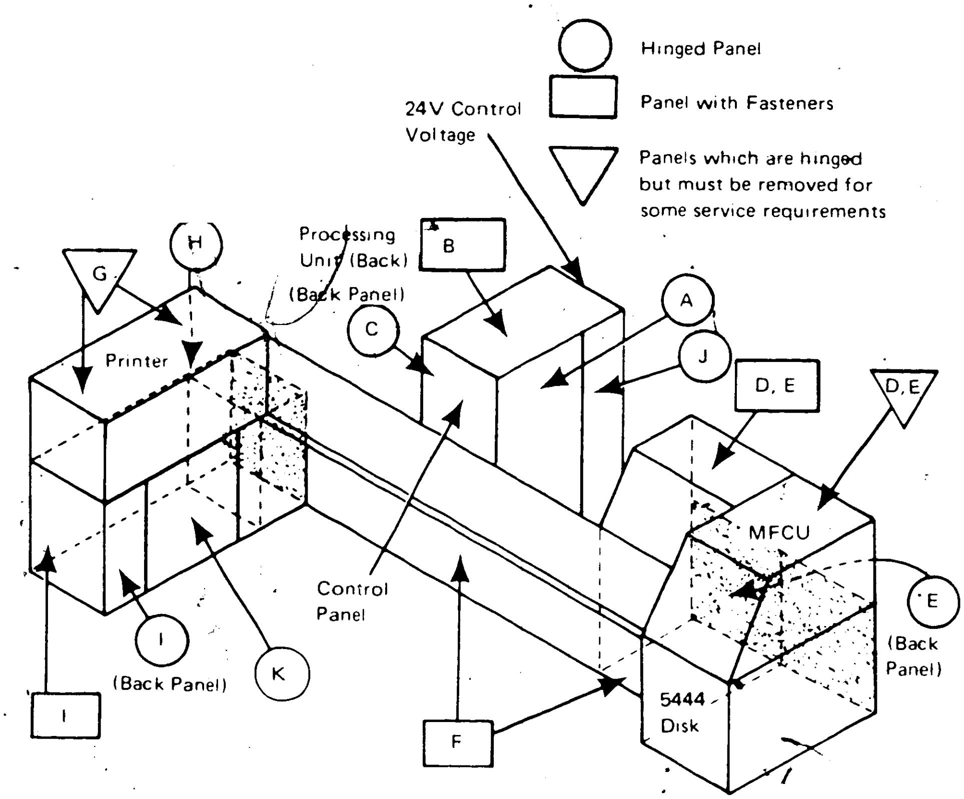


Figure 6-1. Access Panels on the System/3

6

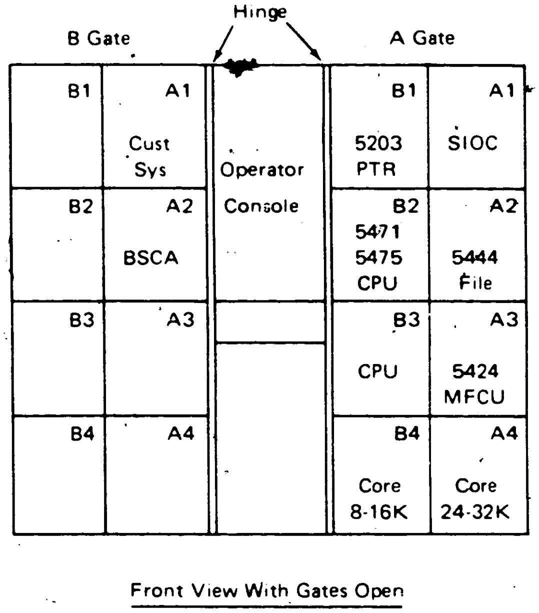


Figure 6-2. CPU Gate Locations (Boards)

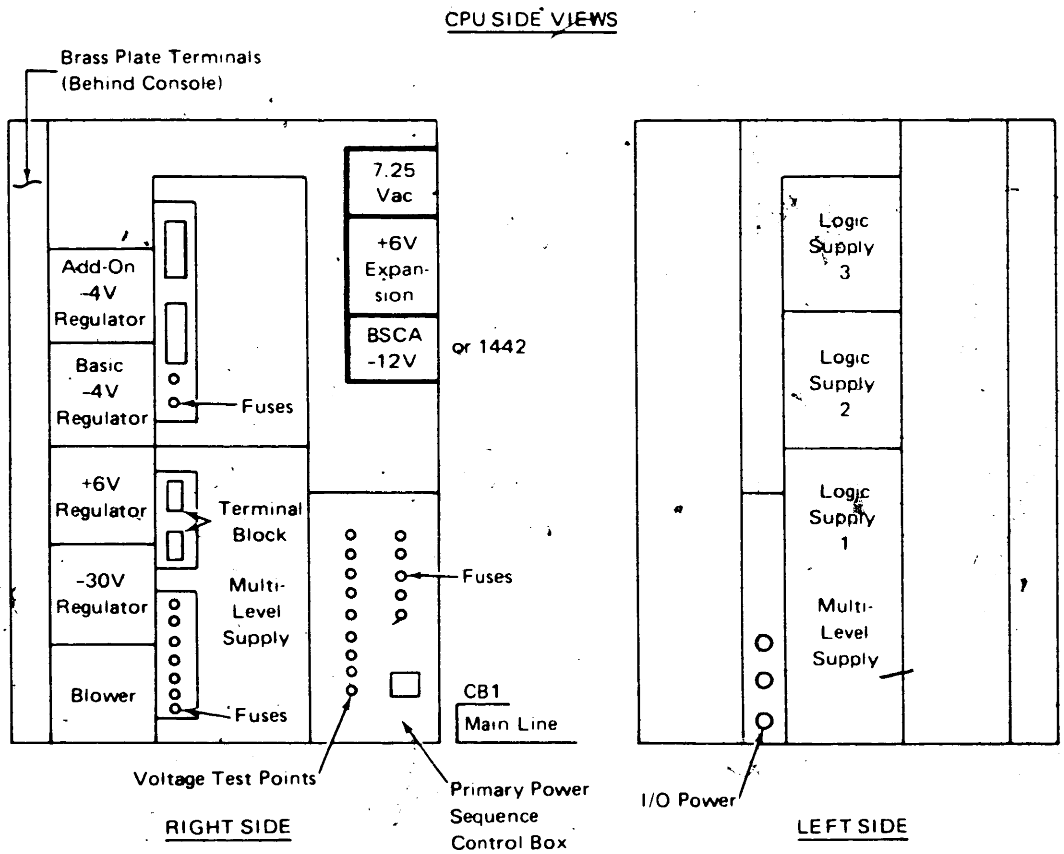
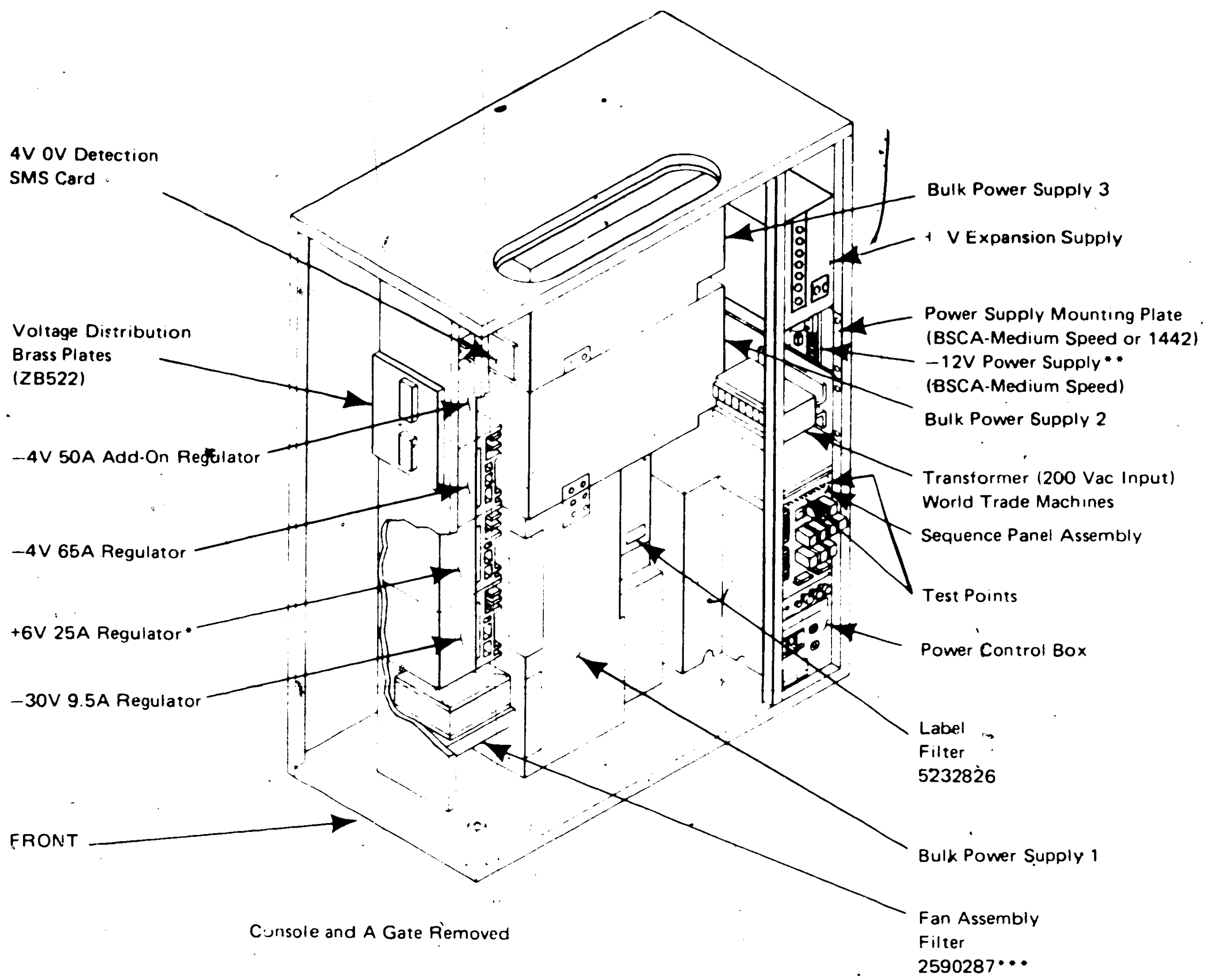


Figure 6-3. CPU Power Supplies (Early Design)



* Replaced with a +6V 40A regulator when the +6V expansion supply is installed.

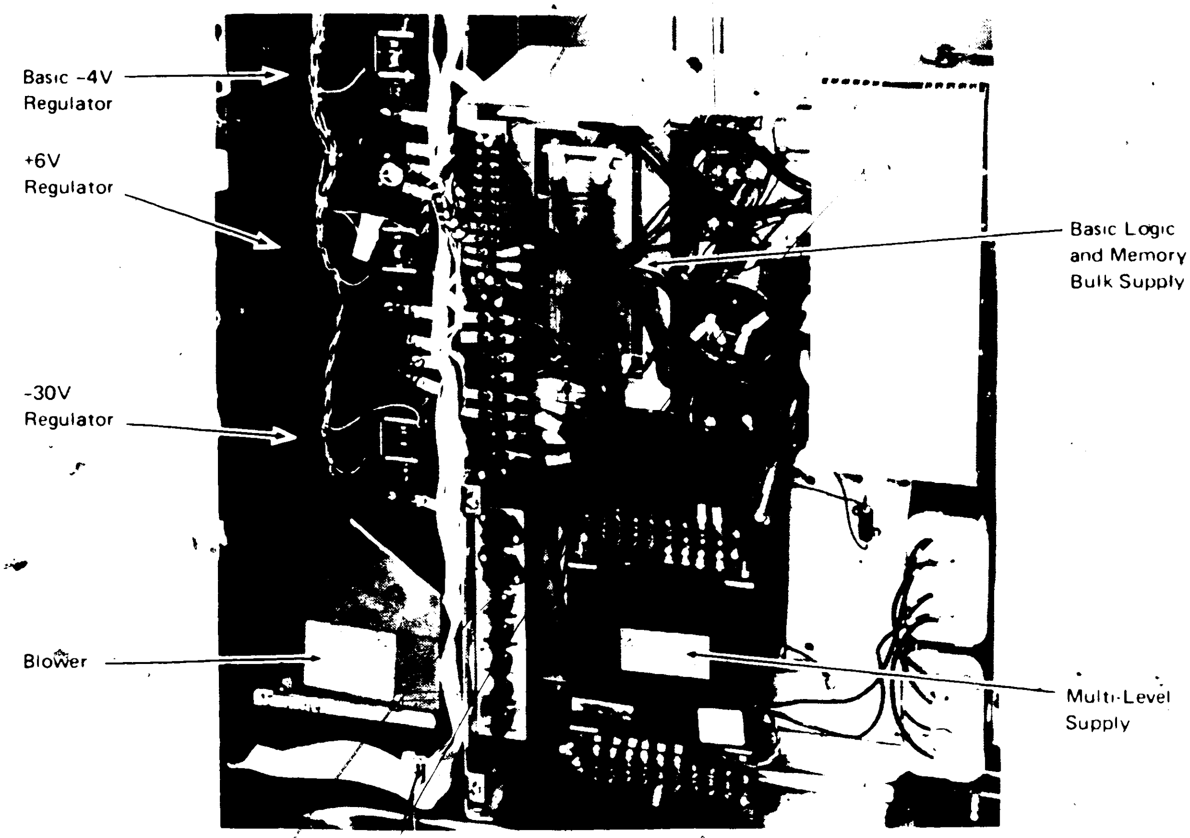
** Replaced with a ±12V supply when the MLTA is installed.

*** Finger guard (7369722) replaces filter when the bulk power supply is installed.

● Figure 6-4. CPU Power Supplies (Redesign Power Control)

6

A Early Design Bulk Supply



B Redesigned Bulk Supply

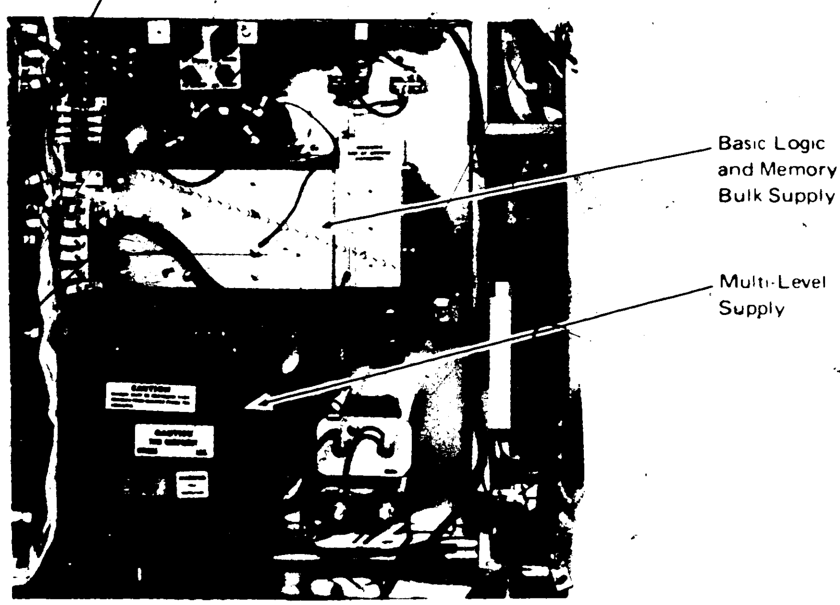


Figure 6-5. Number 1 Logic and Memory Bulk Supply

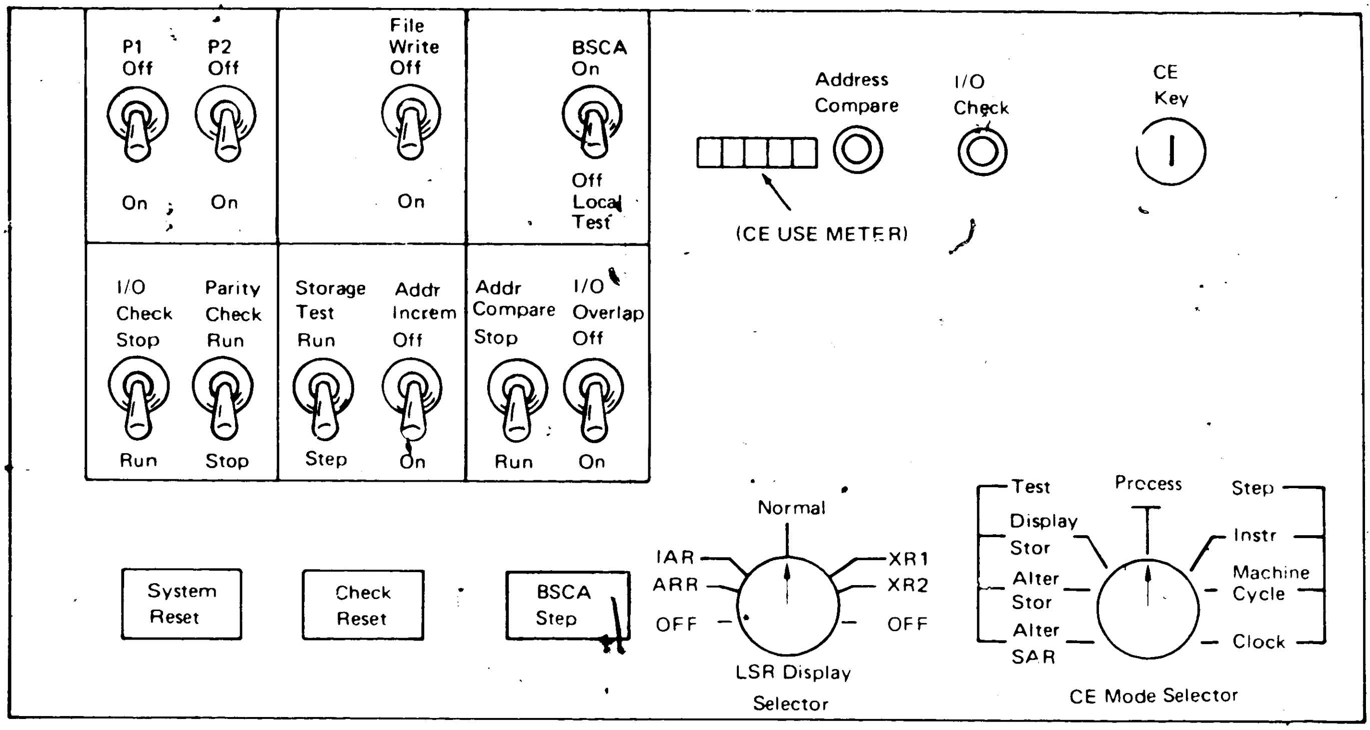


Figure 6-6. CE Control Panel

6

SPECIAL

CIRCUITS

C13

There are no special circuits in the 5410 CPU.

A

WORLD

TRADE

C15

Appendix B. World Trade

The input power requirements for World Trade machines are as follows:

50 Hertz--200, 220, 235, 380, and 408Vac.