IBM Field Engineering
Theory-Maintenance

System/3 Model 6
5406 Processing Unit and Attachments

SY34-0022-1

Preface

This manual is a combined theory-diagram and maintenance manual for the 5406 Processing Unit. It is divided into eleven sections, and with the following exceptions it is a self-contained manual:

1. Sections 2 through 6 are the diagrams for the processing unit, and must be used in conjunction with the Field Engineering Theory of Operations Manual, *IBM System/3 Model 6 5406 Processing Unit,* Order No. SY34-0023.
2. Section 8 is the disk file attachment manual which is a separate theory-diagram manual. The Field Engineering Theory-Diagrams Manual (*IBM System/3 5444 Disk Storage Drive Attachment,* Order No. SY34-0021) can be inserted, in sequence, in this manual.
3. The binary synchronous communications adapter (BSCA) and serial input output channel (SIOC) feature attachment manuals are separate theory-diagrams manuals which are also required if these features are present on the system.

The eleven sections of the manual are as follows:

Section	*Title*	
1	System Maintenance	
2	Error Conditions	CPU Sections
3	Data Flow	
4	Functional Units	
5	Operations	
6	Power and Cooling	
7	Keyboard and Console	
8	Disk File Attachment (separate manual)	
9	Printer and Ledger Card Device Attachments	
10	Data Recorder Attachments	
11	CRT Attachment	

Other manuals necessary to understand and service the IBM System/3 Model 6 are:

1. Field Engineering Parts Catalog, *IBM 5406 Processing Unit,* Order No. S134-0001
2. Field Engineering Maintenance Diagrams, *IBM System/3 Serial I/O Channel Attachment,* Order No. SY31-0275
3. Field Engineering Maintenance Diagrams, *IBM System/3 Binary Synchronous Communications Adapter,* Order No. SY31-0258
4. Field Engineering Theory-Maintenance Diagrams, *IBM 5496 Data Recorder Online Feature,* Order No. SY31-0279
5. Field Engineering Theory-Maintenance Manual, *Elastic Diaphragm Encoded Keyboards,* Order No. SY27-0073
6. Maintenance Library Theory-Maintenance Manual, *IBM 2222 Printer Models 1 and 2,* Order No. SY24-3585

Second Edition (February 1971)

This is a revision of, and obsoletes SY34-0022-0. Changes and corrections were made to all chapters and sections. The basic content and format remain the same.

Within this manual, System/3 machines made for use in the United States are referred to as domestic machines, machines made for use in countries other than the United States are referred to as World Trade machines.

Changes to the information in this manual will be reported in subsequent revisions or supplements.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.

A form for readers' comments is provided at the back of this publication. If the form has been removed, send your comments to IBM Corporation, General System Division, Systems Publications, Department 707, Boca Raton, Florida 33432.

Abbreviations

AAR	A field Address Register
ALD	Automated Logic Diagram
ALU	Arithmetic Logic Unit
ARR	Address Recall Register
BAR	B field Address Register
BSCA	Binary Synchronous Communications Adapter
BSM	Basic Storage Module
CPU	Central Processing Unit
CR	Condition Register
CRR	Condition Recall Register
CRTAR	CRT Address Register
DA	Device Address
DBI	Data Bus In
DBO	Data Bus Out
DFCR	Disk File Control Register
DFDR	Disk File Data Register
DPF	Dual Program Feature (not used on the 5406)
DRAR	Data Recorder Address Register
DRR	Data Recall Register
EBCDIC	Extended Binary Coded Decimal Interchange Code
IAR	Instruction Address Register
I/O	Input–Output
K	Thousand
LCD	Ledger Card Device
LCR	Length Count Register
LCRR	Length Count Recall Register
LLAR	Locate Line Address Register
LSR	Local Storage Register
MAP	Maintenance Analysis Procedure
MST	Monolithic System Technology
PC	Parity Check
PCAR	Print Command Address Register
PDAR	Print Data Address Register
PG	Parity Generate
POR	Power On Reset
PSR	Program Status Register
SAR	Storage Address Register
SDR	Storage Data Register
SIOC	Serial Input Output Channel
XR	Index Register

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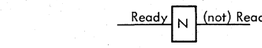
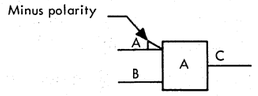
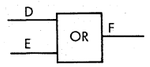
Legend



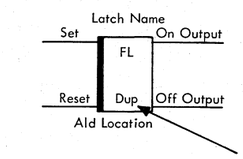
Negator inverts logic on positive logic diagrams



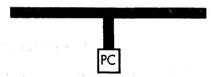
"A" and "B" must be active for "C" to be active



"D" or "E" active causes "F" to be active

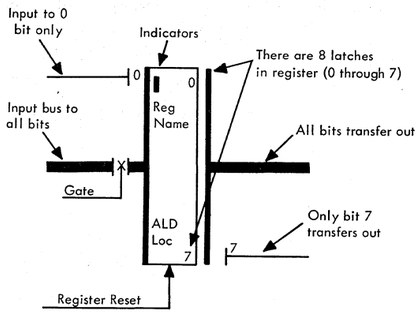


Flip flops or flip latches that are shown on another diagram



Parity Check on Bus Line

Parity Generator (Correct parity is generated.)



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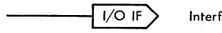
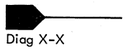


Interface Connector



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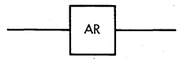
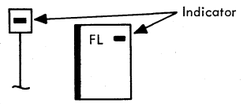


Amplifier



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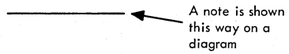
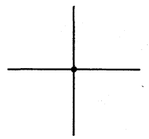
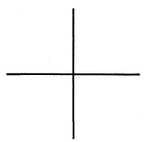


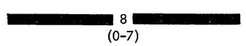
A note is shown this way on a diagram



Joining Lines



Lines cross over but do not join



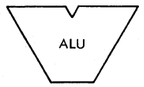
8 lines on bus bits 0,1,2,3, 4,5,6 and 7

Boolean Algebra Symbols

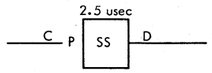
• In a line name means "And"

+ In a line name means "Or"

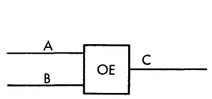
(xx - - - x) Indicates a line name that does not exist as an actual ALD name, but used to better explain the function of a line or block



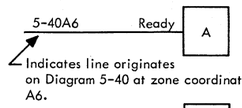
Arithmetic Logic Unit (located in the CPU)

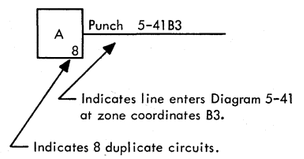


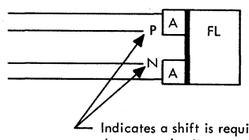
Single Shot
A positive shift on "C" causes a 2.5 usec shift on "D"



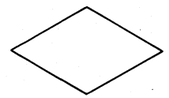
Exclusive OR
Either "A" or "B" must be active for "C" to be active, but if both are active or neither active "C" will be inactive.



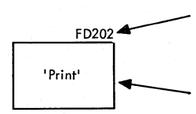




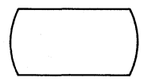
* Indicates a point that can be scoped on back-panel pins.



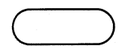
Decision Block on a Flowchart (Asks a question)



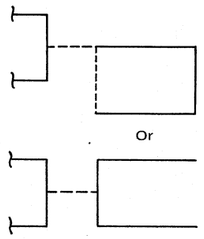
Single quotes in the block indicate a line name, flip latch, or flip flop name

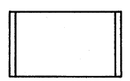


Keying Operation on Flowchart



Terminal on a flowchart





Refers to another Flowchart

Legend

REGISTER (REG)

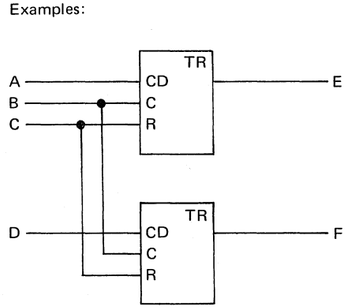
- A register is a functional logic block consisting of a group of associated triggers (TR) with common lines such as reset (R), control (C), etc. Common gates may also be included.
- Common Section.

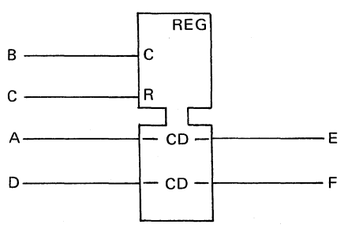
  Contains lines common to one or more logic elements.
- Data Section

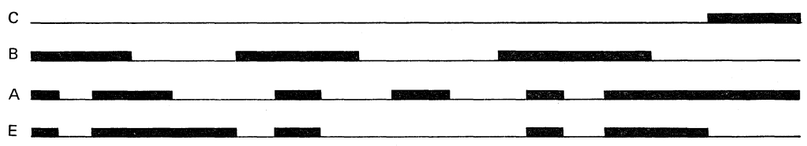
  The inputs and/or outputs shall be grouped and shall be interconnected with lines and connecting symbol.
- Name

  The common section shall have the name "REG".

Examples:







DECODER (DCD)

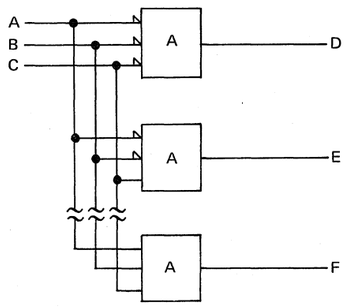
- A functional logic block in which inputs and outputs are assigned numeric values. An output line is active when and only when its value (number) is equal to the sum of the values of all active input lines.
- Note: At any given time there is only one sum. If all input lines are inactive, the sum is zero.
- Common Section.

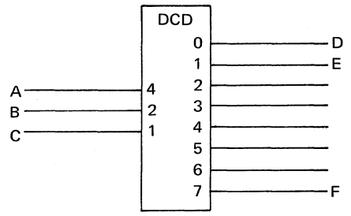
  When gating is used, the gating line and gated line shall be cross-related by labeling with a letter, rather than a numeral. These common lines shall be drawn to the common section. The common section is not used if there are no common lines.
- Data Section.

  The inputs to a decode block shall be number 1, 2, 4, 8, 16, etc. The outputs shall be numbered to reflect the sum of the active inputs required for each decode output.
- Name

  The common section (when used) shall have the name "DCD"; when the common section is not used, the data section shall have the name "DCD".

Example 1: Decoder without gating.





Section 1. System Maintenance

This section of the combined theory-maintenance manual (FETMM) contains the maintenance procedures for the 5406. It is divided into six chapters as follows:

Chapter 1. Reference Data
Chapter 2. Console and Maintenance Facilities
Chapter 3. Preventive Maintenance
Chapter 4. Checks, Adjustments, and Removals
Chapter 5. Power and Cooling
Chapter 6. Locations

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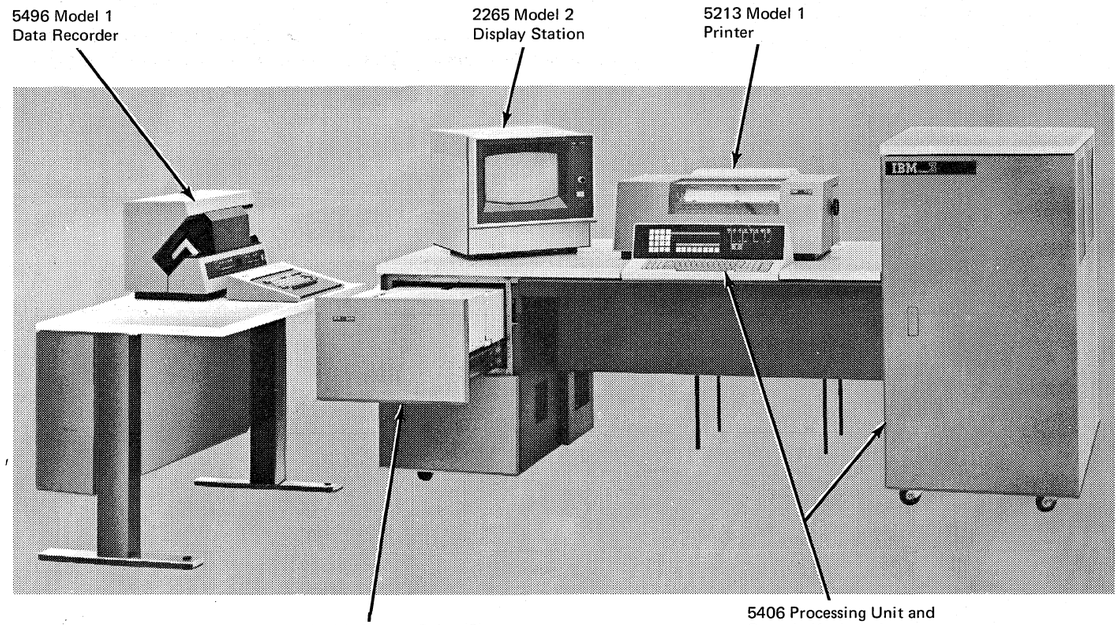

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Safety

PERSONAL SAFETY

Ensure your own safety by making it an everyday practice to use caution at all times and by being aware of potentially dangerous areas of the machine. Be sure to read and follow the safety suggestions in Form No. 229-1264, a pocket-sized card issued to all IBM Customer Engineers.

Remember:

- Loose clothing can become entangled in moving parts of the machine.
- Drive belts, because of their internal cable construction, can cause serious injury. Do not crank a machine by pulling on the drive belts.
- Heat sinks are at an electrical potential. Do not short heat sinks to each other or to the machine side frame.
- Always unplug machine power and wait one full minute before attempting repairs or adjustments in the power supply area.
- Voltages developed in the resonant circuit of regulating power supplies are apt to be much greater than the line voltages.
- Follow the specific safety precautions that accompany many of the adjustment procedures in this manual.

EQUIPMENT SAFETY

Electrical

Always replace blown fuses with fuses of the same type and rating. Using fuses of a different type or higher rating could result in component damage.

Remove power from the machine before replacing MST cards, magnets, or solenoids. Failure to do this could result in damage to a card being replaced or to other cards in the net.

Mechanical

Do not operate the machine under power with units disassembled, removed, or maladjusted. Keep tools clear of the mechanism when the machine is operating under power.

CAUTION

Do not use IBM cleaning fluid on plastic parts.

Chapter 1. Reference Data

This section contains charts, listings, and diagrams giving general information for diagnosing system failures.

The following sections of this manual (sections 2 through 11) contain the flowcharts, timing charts, and diagrams for the central processing unit and attachments. The reference material found in this chapter is a collection of the most frequently used data found in these chapters. For more detailed information on any of the data found in this chapter, refer to the chapter that fully explains the area that you are working on.

For diagnostic techniques, refer to the maintenance analysis procedures (MAP) chart user's guide. The MAP charts help to isolate machine troubles without the use of an oscilloscope.

	Mnem	Op	Q	Operands	Comments
Two Address Instruction	ZAZ	X4	L_1L_2		Zero and add zoned
	AZ	X6	L_1L_2		Add zoned decimal
	SZ	X7	L_1L_2		Subtract zoned decimal
	MVX	X8			Move hex characters
	ED	XA	L_1		Edit
	ITC	XB	L_1		Insert and test characters
	MVC	XC	L		Move characters
	CLC	XD	L		Compare logical characters
	ALC	XE	L		Add logical characters
	SLC	XF	L		Subtract logical characters
		0		Op1 | Op2	Op1 direct, Op2 direct
		1		Op1 | Op2	Op1 direct, Op2 indexed by XR1
		2		Op1 | Op2	Op1 direct, Op2 indexed by XR2
		4		Op1 | Op2	Op1 indexed by XR1, Op2 direct
		5		Op1 | Op2	Op1 indexed by XR1, Op2 indexed by XR1
		6		Op1 | Op2	Op1 indexed by XR1, Op2 indexed by XR2
		8		Op1 | Op2	Op1 indexed by XR2, Op2 direct
		9		Op1 | Op2	Op1 indexed by XR2, Op2 indexed by XR1
		A		Op1 | Op2	Op1 indexed by XR2, Op2 indexed by XR2
One Address Instruction (Non-Branch)	SNS	Y0	DA|M|N		Sense I/O
	LIO	Y1	DA|M|N		Load I/O
	ST	Y4	Reg		Store register
	L	Y5	Reg		Load register
	A	Y6	Reg		Add to register
	TBN	Y8	Mask		Test bits on
	TBF	Y9	Mask		Test bits off
	SBN	YA	Mask		Set bits on
	SBF	YB	Mask		Set bits off
	MVI	YC	I_2		Move logical immediate
	CLI	YD	I_2		Compare logical immediate
		3		Op1 Addr	Op1 direct
		7		Op1	Op1 indexed by XR1
		B		Op1	Op1 indexed by XR2
One Address Instruction (Branch)	BC	Z0	Cond.		Branch on condition
	TIO	Z1	DA|M|N		Test I/O and branch
	LA	Z2	Bit 6-XR2 Bit 7-XR1		Load address
		C		Op2	Op2 direct
		D		Op2	Op2 indexed by XR1
		E		Op2	Op2 indexed by XR2
Command Instruction	HPL	F0	Tens	Unit	Halt program level
	APL	F1	DA|M|N	N U	Advance program level
	JC	F2	Cond.	Number of bytes to jump	Jump on condition
	SIO	F3	DA|M|N	Control	Start I/O

BR0610

Bits 0-3 \ Bits 4-7	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Q Code One Byte	Operands: First	Operands: Second	Total Instr Length	Type
0					ZAZ		AZ	SZ	MVX		ED	ITC	MVC	CLC	ALC	SLC		2 Bytes Direct		6	X
1					ZAZ		AZ	SZ	MVX		ED	ITC	MVC	CLC	ALC	SLC		2 Bytes Direct	1 Byte Disp. Index by XR1	5	X
2					ZAZ		AZ	SZ	MVX		ED	ITC	MVC	CLC	ALC	SLC		2 Bytes Direct	1 Byte Disp. Index by XR2	5	X
3	SNS	LIO			ST	L	A		TBN	TBF	SBN	SBF	MVI	CLI				2 Bytes Direct		4	Y
4					ZAZ		AZ	SZ	MVX		ED	ITC	MVC	CLC	ALC	SLC		1 Byte Displacement Indexed By XR1	2 Bytes Direct	5	X
5					ZAZ		AZ	SZ	MVX		ED	ITC	MVC	CLC	ALC	SLC		1 Byte Displacement Indexed By XR1	1 Byte Disp. Index by XR1	4	X
6					ZAZ		AZ	SZ	MVX		ED	ITC	MVC	CLC	ALC	SLC		1 Byte Displacement Indexed By XR1	1 Byte Disp. Index by XR2	4	X
7	SNS	LIO			ST	L	A		TBN	TBF	SBN	SBF	MVI	CLI				1 Byte Displacement Indexed By XR1		3	Y
8					ZAZ		AZ	SZ	MVX		ED	ITC	MVC	CLC	ALC	SLC		1 Byte Displacement Indexed By XR2	2 Bytes Direct	5	X
9					ZAZ		AZ	SZ	MVX		ED	ITC	MVC	CLC	ALC	SLC		1 Byte Displacement Indexed By XR2	1 Byte Disp. Index by XR1	4	X
A					ZAZ		AZ	SZ	MVX		ED	ITC	MVC	CLC	ALC	SLC		1 Byte Displacement Indexed By XR2	1 Byte Disp. Index by XR2	4	X
B	SNS	LIO			ST	L	A		TBN	TBF	SBN	SBF	MVC	CLI				1 Byte Displacement Indexed By XR2		3	Y
C	BC	TIO	LA															2 Bytes Direct		4	Z
D	BC	TIO	LA															1 Byte Disp. Index by XR1		3	Z
E	BC	TIO	LA															1 Byte Disp. Index by XR2		3	Z
F	HPL	APL	JC	SIO																3	F

Legend

OP BITS 0123

X 2 address instruction (can be indexed by bits 0–3)

Y 1 address instruction (can be indexed by bits 0 and 1)

Z 1 address instruction (can be indexed by bits 2 and 3)

F Command instruction

BR0611

Op	Mnem	Op	Q	R	X_1	H_1	L_1	X_2	H_2	L_2	A	B
04	ZAZ	x	x			x	x		x	x	x	x
06	AZ	x	x			x	x		x	x	x	x
07	SZ	x	x			x	x		x	x	x	x
08	MVX	x	x			x	x		x	x	x	x
0A	ED	x	x			x	x		x	x	x	x
0B	ITC	x	x			x	x		x	x	x	x
0C	MVC	x	x			x	x		x	x	x	x
0D	CLC	x	x			x	x		x	x	x	x
0E	ALC	x	x			x	x		x	x	x	x
0F	SLC	x	x			x	x		x	x	x	x
14	ZAZ	x	x			x	x	x			x	x
16	AZ	x	x			x	x	x			x	x
17	SZ	x	x			x	x	x			x	x
18	MVX	x	x			x	x	x			x	x
1A	ED	x	x			x	x	x			x	x
1B	ITC	x	x			x	x	x			x	x
1C	MVC	x	x			x	x	x			x	x
1D	CLC	x	x			x	x	x			x	x
1E	ALC	x	x			x	x	x			x	x
1F	SLC	x	x			x	x	x			x	x
24	ZAZ	x	x			x	x	x			x	x
26	AZ	x	x			x	x	x			x	x
27	SZ	x	x			x	x	x			x	x
28	MVX	x	x			x	x	x			x	x
2A	ED	x	x			x	x	x			x	x
2B	ITC	x	x			x	x	x			x	x
2C	MVC	x	x			x	x	x			x	x
2D	CLC	x	x			x	x	x			x	x
2E	ALC	x	x			x	x	x			x	x
2F	SLC	x	x			x	x	x			x	x
30	SNS	x	x			x	x					x
31	LIO	x	x			x	x					x
34	ST	x	x			x	x					x
35	L	x	x			x	x					x
36	A	x	x			x	x					x
38	TBN	x	x			x	x					x
39	TBF	x	x			x	x					x
3A	SBN	x	x			x	x					x
3B	SBF	x	x			x	x					x
3C	MVI	x	x			x	x					x
3D	CLI	x	x			x	x					x
44	ZAZ	x	x		x				x	x	x	x
46	AZ	x	x		x				x	x	x	x
47	SZ	x	x		x				x	x	x	x
48	MVX	x	x		x				x	x	x	x
4A	ED	x	x		x				x	x	x	x

Op	Mnem	Op	Q	R	X_1	H_1	L_1	X_2	H_2	L_2	A	B
4B	ITC	x	x		x				x	x	x	x
4C	MVC	x	x		x				x	x	x	x
4D	CLC	x	x		x				x	x	x	x
4E	ALC	x	x		x				x	x	x	x
4F	SLC	x	x		x				x	x	x	x
54	ZAZ	x	x		x			x			x	x
56	AZ	x	x		x			x			x	x
57	SZ	x	x		x			x			x	x
58	MVX	x	x		x			x			x	x
5A	ED	x	x		x			x			x	x
5B	ITC	x	x		x			x			x	x
5C	MVC	x	x		x			x			x	x
5D	CLC	x	x		x			x			x	x
5E	ALC	x	x		x			x			x	x
5F	SLC	x	x		x			x			x	x
64	ZAZ	x	x		x			x			x	x
66	AZ	x	x		x			x			x	x
67	SZ	x	x		x			x			x	x
68	MVX	x	x		x			x			x	x
6A	ED	x	x		x			x			x	x
6B	ITC	x	x		x			x			x	x
6C	MVC	x	x		x			x			x	x
6D	CLC	x	x		x			x			x	x
6E	ALC	x	x		x			x			x	x
6F	SLC	x	x		x			x			x	x
70	SNS	x	x		x							x
71	LIO	x	x		x							x
74	ST	x	x		x							x
75	L	x	x		x							x
76	A	x	x		x							x
78	TBN	x	x		x							x
79	TBF	x	x		x							x
7A	SBN	x	x		x							x
7B	SBF	x	x		x							x
7C	MVI	x	x		x							x
7D	CLI	x	x		x							x
84	ZAZ	x	x		x				x	x	x	x
86	AZ	x	x		x				x	x	x	x
87	SZ	x	x		x				x	x	x	x
88	MVX	x	x		x				x	x	x	x
8A	ED	x	x		x				x	x	x	x
8B	ITC	x	x		x				x	x	x	x
8C	MVC	x	x		x				x	x	x	x
8D	CLC	x	x		x				x	x	x	x
8E	ALC	x	x		x				x	x	x	x
8F	SLC	x	x		x				x	x	x	x

Op	Mnem	Op	Q	R	X_1	H_1	L_1	X_2	H_2	L_2	A	B
94	ZAZ	x	x		x			x			x	x
96	AZ	x	x		x			x			x	x
97	SZ	x	x		x			x			x	x
98	MVX	x	x		x			x			x	x
9A	ED	x	x		x			x			x	x
9B	ITC	x	x		x			x			x	x
9C	MVC	x	x		x			x			x	x
9D	CLC	x	x		x			x			x	x
9E	ALC	x	x		x			x			x	x
9F	SLC	x	x		x			x			x	x
A4	ZAZ	x	x		x			x			x	x
A6	AZ	x	x		x			x			x	x
A7	SZ	x	x		x			x			x	x
A8	MVX	x	x		x			x			x	x
AA	ED	x	x		x			x			x	x
AB	ITC	x	x		x			x			x	x
AC	MVC	x	x		x			x			x	x
AD	CLC	x	x		x			x			x	x
AE	ALC	x	x		x			x			x	x
AF	SLC	x	x		x			x			x	x
B0	SNS	x	x		x							x
B1	LIO	x	x		x							x
B4	ST	x	x		x							x
B5	L	x	x		x							x
B6	A	x	x		x							x
B8	TBM	x	x		x							x
B9	TBF	x	x		x							x
BA	SBN	x	x		x							x
BB	SBF	x	x		x							x
BC	MVI	x	x		x							x
BD	CLI	x	x		x							x
C0	BC	x	x			x	x					
C1	TIO	x	x			x	x					
C2	LA	x	x			x	x					
D0	BC	x	x		x							
D1	TIO	x	x		x							
D2	LA	x	x		x							
E0	BC	x	x		x							
E1	TIO	x	x		x							
E2	LA	x	x		x							
F0	HPL	x	x	x								
F1	APL	x	x	x								
F2	JC	x	x	x								
F3	SIO	x	x	x								

BR0612

Op Code Z1	Q Code DA	M	N	Address Operand 1		
0 7	8 11	12	13 15	16 XX		
C1				2 Bytes		Direct Addressing (H1L1)
D1				1 Byte		Indexed by XR1
E1				1 Byte		Indexed by XR2
5213/ 2222 Printer	E					Device Address Serial Printer
		0				Selects Printer
			000			Unit Check
			001			End of Forms
			010			Busy
			011			Busy or End of Forms
			100			Element at Left Margin
			101			End of Forms or Element at Left Margin
			110			Element at Left Margin or Busy
			111			End of Forms, Element at Left Margin or Busy
		1				Selects LCD
			000			Unit Check
			001			Last Printable Line
			010			LCD Busy
			011			LSR Busy
			10X			Read ID Busy
			11X			Card Not Aligned
				XXXX	XXXX	Branch to address if condition met
5496 Data Recorder	F					Device Address Data Recorder
		0				M bit is not used, it should be zero.
			X1X			Busy
			X0X			I/O Check or Not Ready
				XXXX	XXXX	Branch to address if condition met
2265 CRT	9					Device Address CRT
		0				M Bit is not used, it should be zero.
			X1X			CRT Busy
			X0X			CRT Check (D Reg Parity Error or CRT Not Ready)
				XXXX	XXXX	Branch to address if condition met
5406 Keyboard	1					Device Address Keyboard
	Test I/O is invalid and will result in invalid Q byte processor check.					
5444 File	A					Device Address Drive 1 (Spindle 0)
	B					Device Address Drive 2 (Spindle 1)
		0				M bit is not used.
			000			Not Ready or Error
			010			Busy-Data Transfer in Process
			100			Scan Found
BSCA	8					Device Address BSCA
		0				M bit is not used.
			000			Not Ready/Unit Check
			001			Op End Interrupt
			010			Busy
			011			ITB Interrupt
			100			Interrupt Pending
			110			New Data
SIOC	3					Device Address SIOC
		0				M bit is not used.
			000			SIOC Not Ready
			010			SIOC Busy
				XXXX	XXXX	Branch to address if condition met

Op Code Z1	Q Code DA	M	N	D1 Indexed Displacement

Note: An X means bit can be a "1" or "0".

BR0614A

Op Code	Q Code			Address		
Y1	DA	M	N	Operand 1		
0 7	8 11	12	13 15	16 23		
31				2 Bytes		Direct Addressing (H1L1)
71				1 Byte		Indexed by XR1
B1				1 Byte		Indexed by XR2
	E					Device Address Serial Printer
5213/ 2222 Printer		0				Selects Printer
		1				Selects LCD
			00X			LLAR
			01X			Control LIO
			10X			PDAR
			11X			PCAR
5496 Data Recorder	F					Device Address Data Recorder
		0				M bit is not used, it should be zero.
			000			DRAR
2265 CRT	9					Device Address CRT
		0				M bit is not used, it should be zero.
			XXX			CRTAR
5406 Keyboard	1					Device Address Keyboard
		X				M bit is not used, a zero is preferred.
			X00			Turn Off Command Lights
			X01			Turn On Command Lights
			X1X			Turn On/Off Field/Operation Lights
5444 Disk	A					Device Address Drive 1 (Spindle 0)
	B					Device Address Drive 2 (Spindle 1)
		0				M bit is not used.
			000			Invalid
			001			Invalid
			010			Invalid
			011			Diagnostic CE
			100			DFDR
			101			Invalid
			110			DFCR
			111			Invalid
SIOC	3					Device Address SIOC
		0				M bit is not used.
			001			I/O Function Register
			010			SIOC Length Count Register
			100			SIAR
			101			Data Transfer Register
BSCA	8					Device Address BSCA
		0				M bit is not used.
			001			Stop Address Register
			010			Transition Address Register
			100			BSCAR
			110			BSCAR (Diagnostic)

Op Code	Q Code	M	N	D1
Y1	DA	M	N	Displacement

Note: An X means bit can be a "1" or "0".

BR0615A

Op Code	Q Code			Command		
F3	DA	M	N	Control Code		
0 7	8 11	12	13 15	16 23 8421	8421	
5213/ 2222 Printer	E					Device Address Serial Printer
		0	XXX		0	Selects Printer N field is not used, zeros are preferred. Serial Print Operation
		1			1	Bi-directional Print Operation
			XXX		0	Selects LCD Start I/O (reads first command byte)
					1	Read all line finder marks (Diagnostic)
5496 Data Recorder	F					Device Address Data Recorder
		0				M bit is not used, it should be zero.
			X01			Read a Card
			X10			Punch a Card
			X11			Diagnostic Data
			X00			Diagnostic Cycle Steal
				XXXX	XXXX	Data used in diagnostic data
2265 CRT	9					Device Address CRT
		0				M bit is not used, it should be zero.
			X1X			Display
			X0X			Halt
				XXXX	XXXX	Data used in halt
5406 Keyboard	1					Device Address Keyboard
		X	XXX			M bit is not used, it should be zero. N field is not used, it should be zero.
				XX10	0000	CE Diagnostic (Set Interrupt Request)
				XX01	0000	Reset Parity Check
				XX00	1000	Drop Bail (Lock Keyboard)
				XX00	0100	Pick Up Bail (Unlock Keyboard)
				XX00	0010	Enable Interrupt
				XX00	0000	Disable Interrupt
				XX00	0001	Turn Off Current Interrupt Request
5444 File	A					Device Address Drive 1 (Spindle 0)
	B					Device Address Drive 2 (Spindle 1)
		0				Removable Disk
		1				Fixed Disk
			000			Control Seek
			001			Read
				XXX0	XX00	Read Data
				XXX0	XX01	Read Identifier
				XXX0	XX10	Read Diagnostic
				XXX0	XX11	Read Verify
			010			Write
				XXX0	XX00	Write Data
				XXX0	XX01	Write Identifier
			011			Scan
				XXX0	XX00	Scan Equal
				XXX0	XX01	Scan Low or Equal
				XXX0	XX10	Scan High or Equal

Note. An X means bit can be a "1" or "0".

Op Code	Q Code			Command		
F3	DA	M	N	Control Code		
0 7	8 11	12	13 15	16 23 8421	8421	
BSCA	8					Device Address BSCA
		0				M bit must be zero.
			000			Control
				X000	0100	Start 2 Second Timeout
			001			Receive
			010			Transmit and Receive
			011			Receive Initial
			100			Auto Call
			110			Loop Test
				X000	0001	Reset Interrupt Request
				X000	0010	Enable Interrupt
				X000	0000	Disable Interrupt
				X000	0000	Cancel 2 Second Timeout
				1000	1000	Enable Reserved Mode
				1000	0000	Disable Reserved Mode
				1001	0000	Enable Step Mode
				1000	0000	Disable Step Mode
				1010	0000	Enable Test Mode
				1000	0000	Disable Test Mode
				1100	0000	Enable BSCA
				1000	0000	Disable BSCA
SIOC	3					Device Address SIOC
		0				M bit is not used.
			000			Always Accepted
			001			Read I/O Device
			010			Write I/O Device
				0000	0001	Reset Interrupt Request
				0000	0010	Enable Interrupt
				0000	0100	Disable Interrupt
				0000	1000	Reset SIOC Adapter Busy
				0001	0000	Set Interrupt Request
			011			I/O Control Byte 1
				0000	0001	I/O 1 Select
				0000	0010	I/O 2 Select
				0000	0100	I/O 3 Select
				0000	1000	I/O 4 Select
				0001	0000	I/O 5 Select
				0010	0000	I/O 6 Select
				0100	0000	I/O 7 Select
				1000	0000	I/O 8 Select
			100			I/O Control Byte 2
				0000	0001	I/O Unit 1 Select
				0000	0010	I/O Unit 2 Select
				0000	0100	I/O 9 Select
				0000	1000	I/O 10 Select
				0001	0000	I/O 11 Select
				0010	0000	I/O 12 Select
				0100	0000	I/O 13 Select
				1000	0000	I/O 14 Select

Note. An X means bit can be a "1" or "0".

BR0616A

Keyboard Sense Instruction

Op Code	Q Code			Address		
Y0	DA	M	N	Operand 1		
0 7	8 11	12	13 15	16 XX		
30 70 B0				2 Bytes 1 Byte 1 Byte		Direct Addressing (H1L1) Indexed by XR1 Indexed by XR2
	1					Device Address Keyboard
5406 Keyboard		X	XXX			M bit is not used, zero is preferred. N field is not used, zero's are preferred. Byte 1 0 Parity Check 1 Data Character Identifier 2 Command Key Identifier 3 Function Character Identifier 4 World Trade Identifier 5 Keyboard Ready 6 Typamatic Key Identifier 7 Not Used
				XXXX	XXXX	Operand Address (Sense Byte Destination)

Op Code	Q Code			D1	
Y0	DA	M	N	Displacement	
					Byte 2 0 1 2 3 4 5 6 7 Contains the coded representation of the key position that was keyed.

Byte 1 = Operand Address
Byte 2 = Operand Address −1

Note. An X means bit can be a "1" or "0".

BR0617A

Printer Sense Instruction

Op Code	Q Code			Address		
Y0	DA	M	N	Operand 1		
0 7	8 11	12	13 15	16 XX		
30 70 B0				2 Bytes 1 Byte 1 Byte		Direct Addressing (H1L1) Indexed by XR1 Indexed by XR2
	E					Device Address Serial Printer
5213/ 2222 Printer		0	010			Select Printer Byte 1 0 Horizontal Cycle Check 1 Data Check 2 Margin Check 3 Sync Check 4 Ros Check 5 Vertical Cycle Check 6 Primary Carriage EOF 7 Invalid Command
			011			Byte 3 0 High Speed Latch 1 Matrix Output Hammer Dr1 2 Matrix Output Hammer Dr2 3 Matrix Output Hammer Dr3 4 Matrix Output Hammer Dr4 5 Matrix Output Hammer Dr5 6 Matrix Output Hammer Dr6 7 Matrix Output Hammer Dr7
			00X			LLAR—Hi
			10X			PDAR—Hi
			11X			PCAR—Hi
		1	010			Select LCD Byte 1 0 Sense Amp Check 1 Card Skew Check 2 Drive Check 3 Read Mark Check 4 5 Line Finder Mark Check 6 Card In Switch On 7 Card Out Switch On
			011			Byte 3* 0 SS 1—Skip Line 1 SS 2—Skip Line 2 Late Mark 3 Special Tie Up (always off) 4 Card Alignment SS 5 Spare 6 Spare 7 Stop SS
				XXXX	XXXX	Operand Address (Sense Bytes Destination)

Op Code	Q Code			D1	
Y0	DA	M	N	Displacement	
					Byte 2 0 Count End Latch 1 Print Left Command 2 Matrix Counter Trigger 1 3 Matrix Counter Trigger 2 4 Matrix Counter Trigger 4 5 Printer Ready 6 SS 2 7 SS 1 or SS 1 Overlap
					Byte 4 0 SS A 1 SS 3 2 Stepper Trigger A 3 Stepper Trigger B 4 SS Z 5 SS Y 6 SS X 7 SS W
					LLAR—Lo
					PDAR—Lo
					PCAR—Lo
					Byte 2 0 Sense Amp 1 1 Sense Amp 2 2 Sense Amp 3 3 Sense Amp 4 4 Timing Pulse 5 Drive Check SS 6 Activate LCD Feed Clutch 7 Hold Busy SS
					Byte 4 0 5213 Printer Attached 1 Not Vertical Forms Control 2 Not Bi-directional Print Feature 3 Secondary Carriage EOF 4 Not Rm sw 1 Slow and Not LM sw 2 Stop 5 Rm sw 2 Stop or LM sw 1 Slow 6 Primary or Secondary Forms Motion Contact 7 Primary Forms Emitter Advance

Byte 1 or 3 = Operand Address
Byte 2 or 4 = Operand Address -1

* If LCD feature is not installed, then this byte will be hex 00.

Note. An X means bit can be a "1" or "0".

BR0618A

Data Recorder and CRT Sense Instruction

Op Code	Q Code			Address	
Y0	DA	M	N	Operand 1	
0 7	8 11	12	13 15	16 XX	
30 70 B0				2 Bytes 1 Byte 1 Byte	Direct Addressing (H1L1) Indexed by XR1 Indexed by XR2
5496 Data Recorder	F				Device Address Data Recorder
		0	X1X		M bit is not used, it should be zero. Byte 1 0 Off Line 1 Transport Jam 2 Stacker Full, Hopper Empty, or Hopper Jam 3 Not Used 4 Incorrect Card Code 5 Compare Error on Read or Punch IO Cycles or Failure to Take Read Cycle Steals 6 Reserved for FE use. 7 Reserved for FE use. Byte 2 (0 1 2 3 4 5 6 7) Contents of 5496 Entry Register
			X0X		DRAR-Lo / DRAR-Hi
2265 CRT	9				Device Address CRT
		0	X1X		M bit is not used, it should be zero. Byte 1 0 Write Op (Diagnostic Only) 1 Start Character Generator (Diagnostic Only) 2 Step-Display (Diagnostic Only) 3 Cycle Steal Request (Diagnostic Only) 4 Display Reset (Diagnostic Only) 5 Data Register Parity Check 6 Display Not Ready 7 Cycle Steal Acknowledged (Diagnostic Only) Byte 2 (0 1 2 3 4 5 6 7) Contents of the Data Register
			X0X		CRTAR-Lo / CRTAR-Hi

Op Code	D1	
Y0	DA M N	Displacement

Byte 1 = Operand Address
Byte 2 = Operand Address –1

Note. An X means bit can be a "1" or "0".

BR0619A

Disk File Sense Instruction

Op Code	Q Code			Address	
Y0	DA	M	N	Operand 1	
30 70 B0				2 Bytes 1 Byte 1 Byte	Direct Addressing (H1L1) Indexed by XR1 Indexed by XR2
5444 File	A				Device Address Drive 1 (Spindle 0)
	B				Device Address Drive 2 (Spindle 1)
		0			Removable Disk
		1			Fixed Disk
			010		Byte 0 0 No Op 1 Intervention Required 2 Missing Address Mark 3 Equipment Check 4 Data Check 5 No Record Found 6 Track Condition Check 7 Seek Check Byte 1 0 Scan Equal Hit 1 Cylinder Zero 2 End of Cylinder 3 Seek Busy 4 100 Cylinder 5 Overrun 6 Status Address A 7 Status Address B
			011		Byte 2 0 Unsafe 1 Tap Line A 2 Tap Line B 3 Tap Line C 4 Index 5 Head Settling 6 CE Bit 7 Model 6 Byte 3 0 CE Bit 1 CE Bit 2 CE Bit 3 Not Bit Ring Inhibit 4 Standard Write Trigger 5 Condition Priority Request 6 Bit Ring 0 7 Not CC Register Position 17
			100		DFDR-Hi / DFDR-Lo
			110		DFCR-Hi / DFCR-Lo

Op Code	D1	
Y0	DA M N	Displacement

Byte 1 or 3 = Operand Address
Byte 0 or 2 = Operand Address -1

Note. An X means bit can be a "1" or "0".

BR0620A

BSCA Sense Instruction

Op Code	Q Code			Address	
Y0	DA	M	N	Operand 1	
0 7	8 11	12	13 15	16 23	
30				2 Bytes	Direct Addressing (H1L1)
70				1 Byte	Indexed by XR1
B0				1 Byte	Indexed by XR2
	8				Device Address BSCA
		0	000		M bit is not used. Byte 1 Diagnostic 0 Not Assigned 1 Not Assigned 2 Not Assigned 3 Not Assigned 4 ITB, BCC or VRC Check 5 LSR/Shift Register Parity Check 6 I/O Cycle Steal Overrun 7 DBI Parity Check — Byte 2 Diagnostic 0 Not Assigned 1 Bit Time Counter 4 2 Bit Time Counter 2 3 Bit Time Counter 1 4 Not Assigned 5 Transmit Trigger 6 Receive Trigger 7 CE Sense Bit
BSCA			011		Byte 1 Status 0 Not Assigned 1 Not Assigned 2 Not Assigned 3 Not Assigned 4 Not Assigned 5 Not Assigned 6 Data Set Ready 7 Data Line Occupied — Byte 2 Status 0 Timeout 1 CRC/LRC/VRC Check 2 Adapter Check on Transmit 3 Adapter Check on Receive 4 Invalid USASCII Character 5 Abortive Disconnect 6 Disconnect Timeout 7 Not Assigned
			001		Stop Address Register — Lo — Stop Address Register — Hi
			010		Transition Address Reg — Lo — Transition Address Reg — Hi
			100		BSCAR - Lo — BSCAR — Hi
			110		CRC Buffer — Lo — CRC Buffer — Hi
			110		LRC Buffer — For USASCII
				XXXX XXXX	Operand Address (Sense Byte Destination)

Op Code | Q Code | D1 | Y0 | DA | M | N | Displacement

Byte 1 = Operand Address
Byte 2 = Operand Address −1

Note. An X means bit can be a "1" or "0".

BR0622A

SIOC Sense Instruction

Op Code	Q Code			Address	
Y0	DA	M	N	Operand 1	
0 7	8 11	12	13 15	16 23	
30				2 Bytes	Direct Addressing (H1L1)
70				1 Byte	Indexed by XR1
B0				1 Byte	Indexed by XR2
	3				Device Address SIOC
		0	001		Byte 1 M bit is not used. Function Register 0 Diagnostic Mode 1 Spare 2 Latch Transfer Line 4 3 Latch Transfer Line 3 4 Latch Transfer Line 1 5 Transfer Line 3 Reset Disconnect Latch 6 Reset Disconnect Latch after 6 usec 7 Transfer Line 5 Reset Disconnect Latch — Byte 2 Function Register 0 Write Mode Set Service Response 1 Reset Service Response after 6 usec 2 Transfer Line 2 EOT 3 Transfer Line 1 EOT 4 Even Parity 5 Decrement DAR 6 Latch I/O 1 Select 7 Slave
SIOC			011		1st Data Byte 0 I/O Transfer Line 8 1 I/O Transfer Line 7 2 I/O Transfer Line 6 3 I/O Transfer Line 5 4 I/O Transfer Line 4 5 I/O Transfer Line 3 6 I/O Transfer Line 2 7 I/O Transfer Line 1 — 2nd Data Byte 0 I/O ID Bit 8 1 I/O ID Bit 4 2 I/O ID Bit 2 3 I/O ID Bit 1 4 I/O Device Attached 5 I/O Transfer Line 11 6 I/O Transfer Line 10 7 I/O Transfer Line 9
					A "1" in each bit position represents an active condition.
			010		Length Count Register (Byte 1) 0 1 2 3 4 5 6 7 — Contents of the Length Count Register — Status Byte (Byte 2) 0 Spare 1 End Request 2 Interrupt Pending 3 I/O Attention 4 Data Transfer Register Parity Check 5 No Operation 6 LCR Overflow 7 I/O Ready
			101		Data Transfer Register (Byte 1) 0 1 2 3 4 5 6 7 — Contents of the Data Transfer Register — Diagnostic Byte (Byte 2) 0 SIOC Request Latch 1 Service Request 2 Service Response 3 Interrupt Enable 4 I/O Disconnect 5 Write Call 6 Read Call 7 I/O Selected
			100		SIAR-Lo — SIAR-Hi
				XXXX XXXX	Operand Address (Sense Byte Destination)

Op Code | Q Code | D1 | Y0 | DA | M | N | Displacement

Byte 1 = Operand Address
Byte 2 = Operand Address −1

Note. An X means bit can be a "1" or "0".

BR0621A

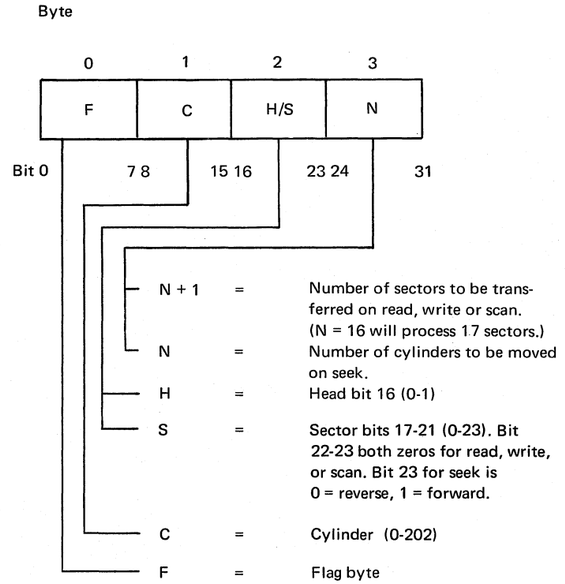
Printer Command Byte

Bit 0	Command Chain
Bit 1	*Print Data
Bit 2	*Horizontal Tab Right
Bit 3	*Horizontal Tab Left
Bit 4	*Primary Carriage Skip
Bit 5	Element Return
Bit 6	Secondary Carriage Index
Bit 7	Primary Carriage Index

*If bit is on a count byte must follow.

BR0623

Format of Disk Control Field



The seek operation uses the H/S and N bytes of the disk control field.

Hexadecimal Values for Head and Sector Selection

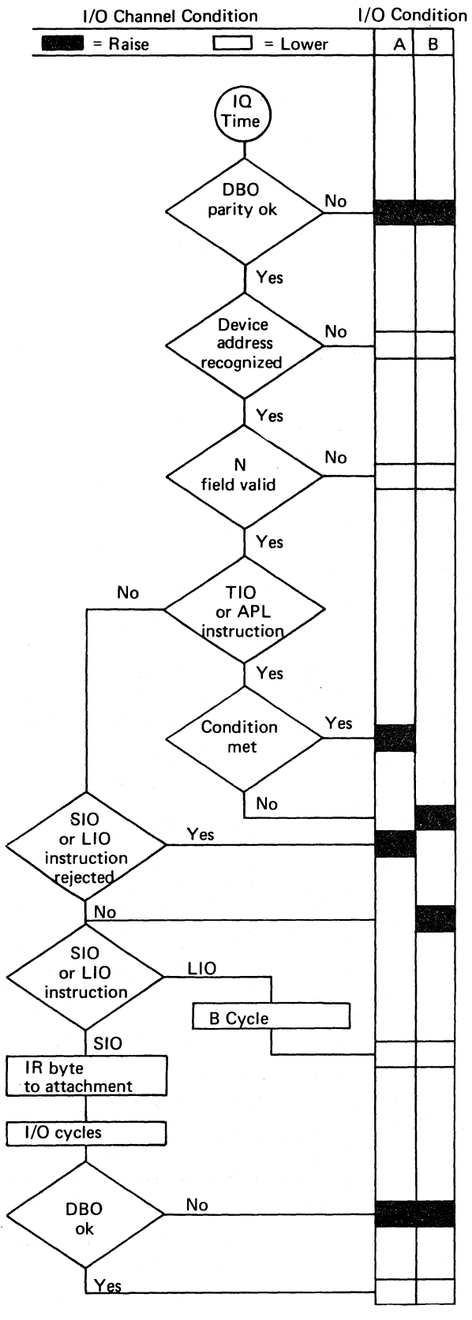
Dec Hex	Dec Hex	Dec Hex	Dec Hex	Dec Hex	Dec Hex
00 = 00	08 = 20	16 = 40	24 = 80	32 = A0	40 = C0
01 = 04	09 = 24	17 = 44	25 = 84	33 = A4	41 = C4
02 = 08	10 = 28	18 = 48	26 = 88	34 = A8	42 = C8
03 = 0C	11 = 2C	19 = 4C	27 = 8C	35 = AC	43 = CC
04 = 10	12 = 30	20 = 50	28 = 90	36 = B0	44 = D0
05 = 14	13 = 34	21 = 54	29 = 94	37 = B4	45 = D4
06 = 18	14 = 38	22 = 58	30 = 98	38 = B8	46 = D8
07 = 1C	15 = 3C	23 = 5C	31 = 9C	39 = BC	47 = DC
Upper Head			Lower Head		

BR0624A

Op Code	Q Code			Operand 1	Byte 1 = Operand Address Byte 2 = Operand Address -1
	DA	M	N		
0 7	8 11	12	13 15	16 23	
3 0					Direct Addressing
7 0					Indexed by XR1
B 0					Indexed by XR2
	0000				Device Address CPU
		0			M Bit (not used)
			000		Byte 2 EB2: 0 1 2 3 Address Switch 1; 4 5 6 7 Address Switch 2 Byte 1 EB1: 0 1 2 3 Address Switch 3; 4 5 6 7 Address Switch 4
				xxxxxxxx	Operand Address (Sense bytes destinations)

Note. An X means bit can be a "1" or "0".

BR0625A



BR0626

Condition Register Settings

Bits	2	3	4	5	6	7
Decimal Arith			Over-flow	Result is Positive	Result is Negative	Result is Zero
Binary Value	2	1	8	4	2	1
Compare Logical				Op 1 > Op2	Op 1 < Op2	Op 1 = Op2
Sub Logical				B>A	B<A	A=B
Add Logical and Add Register	Over-flow			Carry and Not Zero Result	No Carry and Not Zero Result	Result is Zero
Edit				Positive	Negative	Source is Zero
Test Bits		Test False				
Branch on Condition *		Test False Reset if Tested	Over-flow Reset if Tested			
Condition	Binary Over-flow	False	Decimal Over-flow	High or Positive	Low or Negative	Equal or Zero

* Q bit 0 = 0 absence of condition.
Q bit 0 = 1 presence of condition.

BR0627

To find the decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the Hex number, locate the next lower decimal number and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

BYTE				BYTE				BYTE			
0123		4567		0123		4567		0123		4567	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0 0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
6		5		4		3		2		1	

BR0628

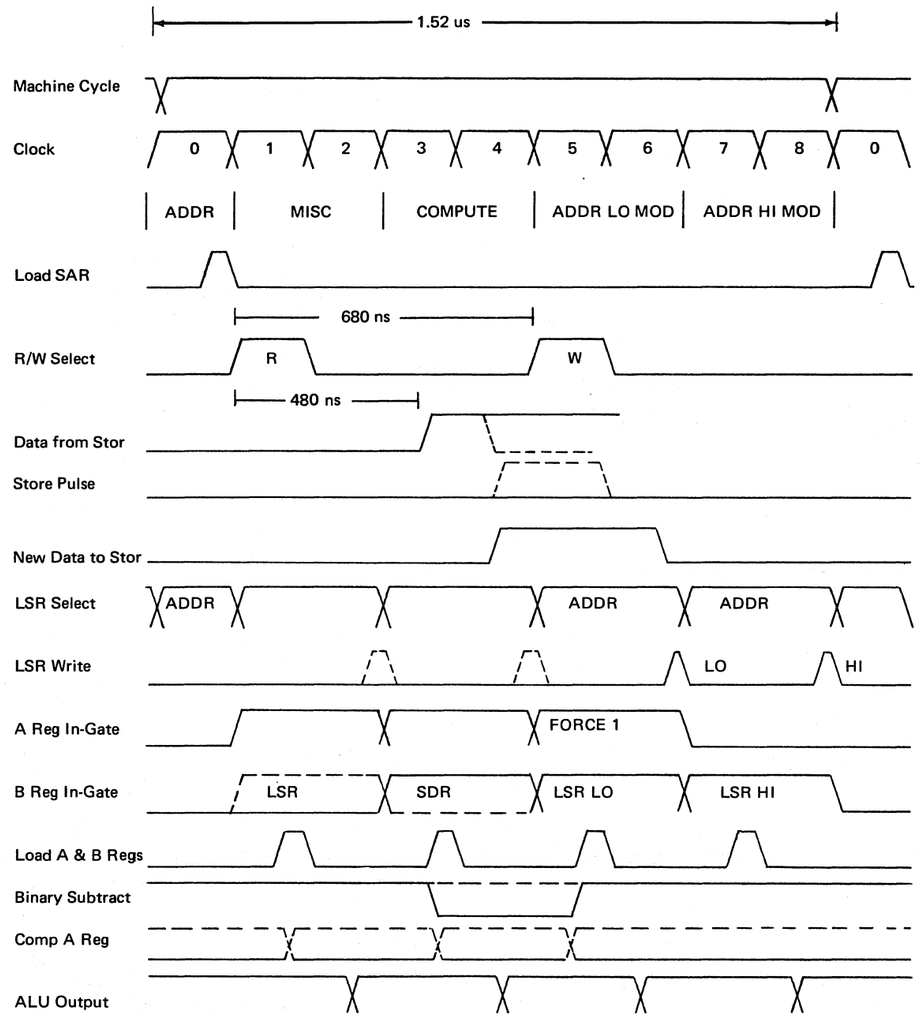
	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

BR0629

I/O Device Priorities

Priority	Attmt Clock	CPU Clock	Request Bit Line	Priority Assignment P 0 1 2 3 4 5 6 7	Model 5406
20 Lo	0	1	7	1 0 0 1 0 0 0 0 1	File Seek
19	0	1	6	1 0 0 1 0 0 0 1 0	Unassigned
18	0	1	5	1 0 0 1 0 0 1 0 0	Unassigned
17	0	1	4	1 0 0 1 0 1 0 0 0	Unassigned
16	0	1	3	1 0 0 1 1 0 0 0 0	Unassigned
15	2	3	7	1 0 1 0 0 0 0 0 1	Unassigned
14	2	3	6	1 0 1 0 0 0 0 1 0	Unassigned
13	2	3	5	1 0 1 0 0 0 1 0 0	CRT
12	2	3	4	1 0 1 0 0 1 0 0 0	Data Recorder
11	2	3	3	1 0 1 0 1 0 0 0 0	Unassigned
10	4	5	7	1 1 0 0 0 0 0 0 1	Unassigned
9	4	5	6	1 1 0 0 0 0 0 1 0	Unassigned
8	4	5	5	1 1 0 0 0 0 1 0 0	Unassigned
7	4	5	4	1 1 0 0 0 1 0 0 0	Unassigned
6	4	5	3	1 1 0 0 1 0 0 0 0	BSCA
5	6	7	7	0 0 0 0 0 0 0 0 1	Unassigned
4	6	7	6	0 0 0 0 0 0 0 1 0	SIOC
3	6	7	5	0 0 0 0 0 0 1 0 0	Printer
2	6	7	4	0 0 0 0 0 1 0 0 0	Unassigned
1 Hi	6	7	3	0 0 0 0 1 0 0 0 0	File Read/Write

BR0630



BR0631

Local Store Registers (Base System)

LSR No	High	Low	LSR Acronym
01	Instruction Address Register		IAR
02	Address Recall Register		ARR
03	Operand 2 Address Register		AAR
04	LCD Locate Line Address Register*		LLAR
05	Index Register 1		XR1
06	Length Count Recall Reg	Condition Recall Reg	PSR
07	Operand 1 Address Register		BAR
08	Disk File Control Register		DFCR
09	Index Register 2		XR2
10	Printer Data Address Register		PDAR
11	Printer Command Address Register		PCAR
12	Data Recorder Address Register		DRAR
13	Disk File Data Register		DFDR
14	Length Count Register	Data Recall Register	LCR DRR
15	Interrupt Level 1 Instruction Address Register		IAR-1
16	Interrupt Level 1 Address Recall Register		ARR-1

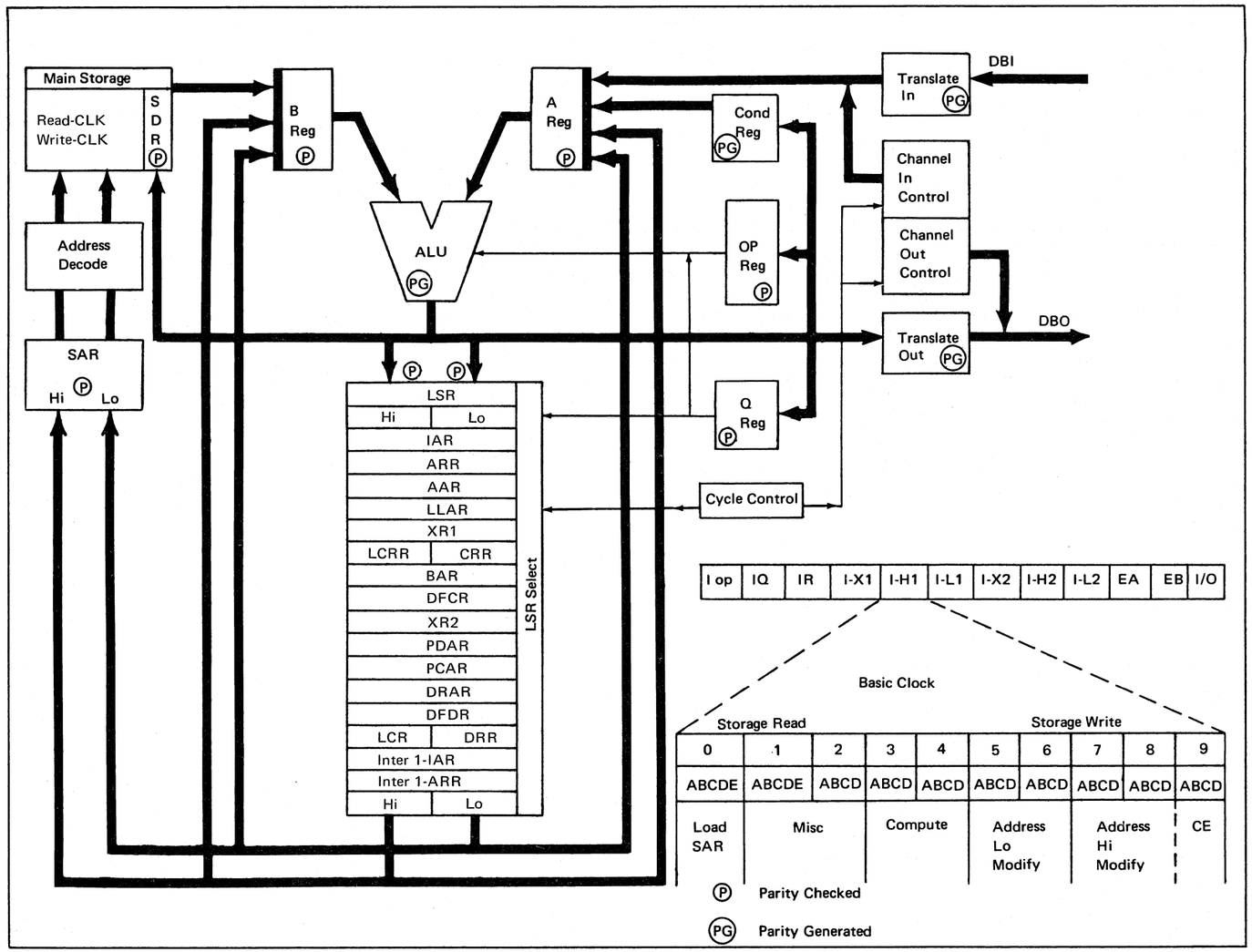
*This LSR is used by the CRT (CRTAR) when the LCD feature is not installed. When both the CRT and LCD features are installed, the CRTAR is located in feature LSR number 10.

Local Storage Registers (Feature)

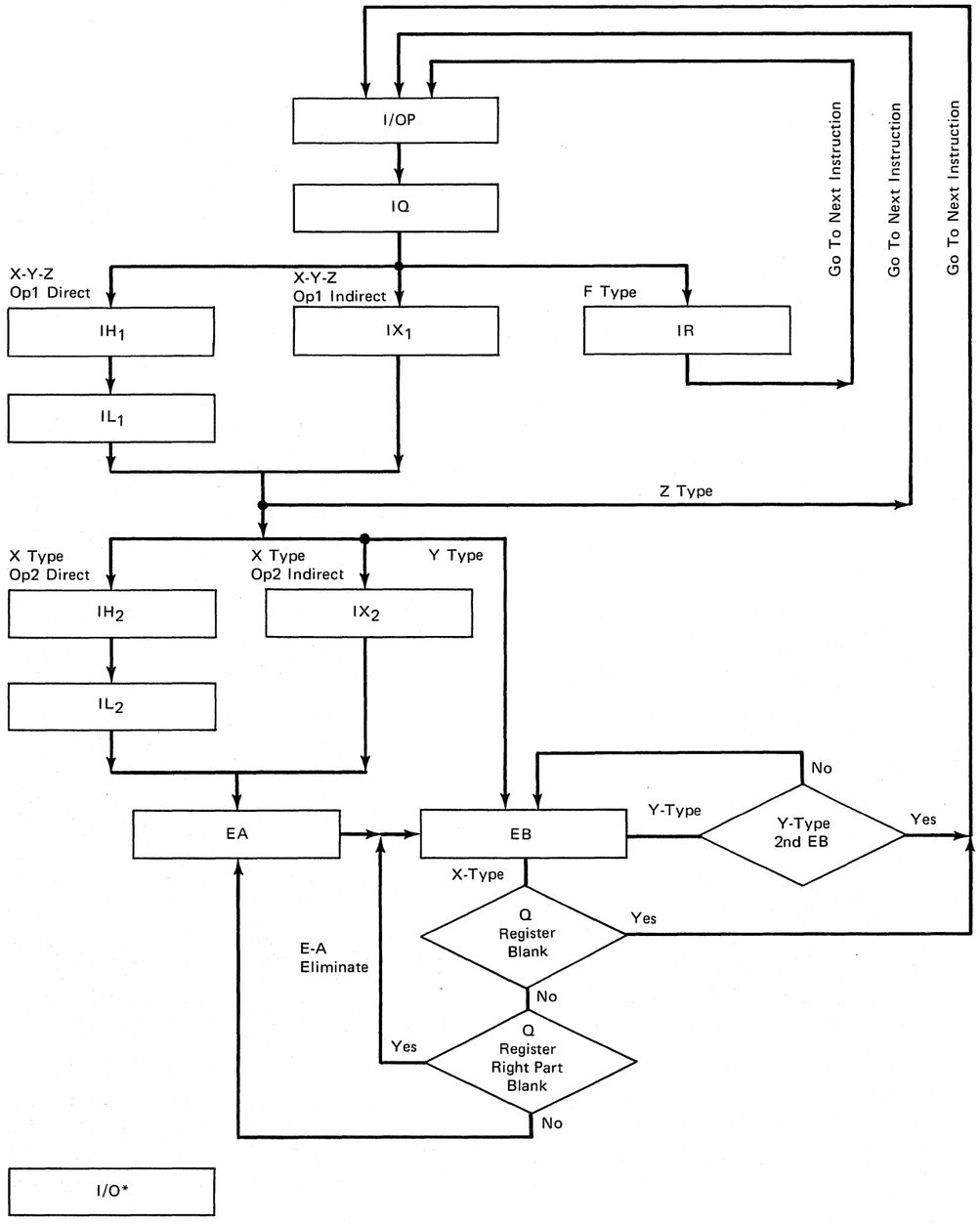
LSR No	High	Low	LSR Acronym
01	Spare		
02	Spare		
03	BSCA Address Register		BSCAR
04	SIOC Address Register		SIAR
05	Spare		
06	Interrupt Level 4 Instruction Address Register		IAR-4
07	Interrupt Level 4 Address Recall Register		ARR-4
08	Spare		
09	Spare		
10	CRT Address Register		CRTAR
11	Interrupt Level 2 Instruction Address Register		IAR-2
12	Interrupt Level 2 Address Recall Register		ARR-2
13	Spare		
14	Spare		
15	Spare		
16	Spare		

BR0632

System/3 Data Flow



BR0633



* Can be performed between any of the 11 above cycles.

BR0634

Bit Position	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	6	7	0	1	2	3	4	5	6	7
Function	Zone				Digit				Zone				Digit				Zone				Digit				Zone		Digit		Sign*				Digit			
																													Low-Order Byte							

*Sign Configurations:		
Binary	Hexadecimal	Function
1010	A	Alternate Plus
1011	B	ASCII-8 Minus
1100	C	Alternate Plus
1101	D	Standard Minus
1110	E	Alternate Plus
1111	F	Standard Plus

BR0635

Dec Val	Hex Val	Card Code DCBA8421	Mnem	EBCDIC	Symbol
000	00	DC		00000000	
001	01	DCBA 1		00000001	
002	02	DCBA 2		00000010	
003	03	DCBA 21		00000011	
004	04	DCBA 4	ZAZ	00000100	
005	05	DCBA 4 1		00000101	
006	06	DCBA 42	AZ	00000110	
007	07	DCBA 421	SZ	00000111	
008	08	DCBA8	MVX	00001000	
009	09	DCBA8 1		00001001	
010	0A	CBA8 2	ED	00001010	
011	0B	CBA8 21	ITC	00001011	
012	0C	CBA84	MVC	00001100	
013	0D	CBA84 1	CLC	00001101	
014	0E	CBA842	ALC	00001110	
015	0F	CBA8421	SLC	00001111	
016	10	C A8 2		00010000	
017	11	DCB 1		00010001	
018	12	DCB 2		00010010	
019	13	DCB 21		00010011	
020	14	DCB 4	ZAZ	00010100	
021	15	DCB 4 1		00010101	
022	16	DCB 42	AZ	00010110	
023	17	DCB 421	SZ	00010111	
024	18	DCB 8	MVX	00011000	
025	19	DCB 8 1		00011001	
026	1A	CB 8 2	ED	00011010	
027	1B	CB 8 21	ITC	00011011	
028	1C	CB 84	MVC	00011100	
029	1D	CB 84 1	CLC	00011101	
030	1E	CB 842	ALC	00011110	
031	1F	CB 8421	SLC	00011111	
032	20	CB		00100000	
033	21	C A 1		00100001	
034	22	DC A 2		00100010	
035	23	DC A 21		00100011	
036	24	DC A 4	ZAZ	00100100	
037	25	DC A 4 1		00100101	
038	26	DC A 42	AZ	00100110	
039	27	DC A 421	SZ	00100111	
040	28	DC A8	MVX	00101000	
041	29	DC A8 1		00101001	
042	2A	DCBA	ED	00101010	
043	2B	C A8 21	ITC	00101011	
044	2C	C A84	MVC	00101100	
045	2D	C A84 1	CLC	00101101	
046	2E	C A842	ALC	00101110	
047	2F	C A8421	SLC	00101111	

Dec Val	Hex Val	Card Code DCBA8421	Mnem	EBCDIC	Symbol
048	30	DC A	SNS	00110000	
049	31	DC 1	LIO	00110001	
050	32	DC 2		00110010	
051	33	DC 21		00110011	
052	34	DC 4	ST	00110100	
053	35	DC 4 1	L	00110101	
054	36	DC 42	A	00110110	
055	37	DC 421		00110111	
056	38	DC 8	TBN	00111000	
057	39	DC 8 1	TBF	00111001	
058	3A	C 8 2	SBN	00111010	
059	3B	C 8 21	SBF	00111011	
060	3C	C 84	MVI	00111100	
061	3D	C 84 1	CLI	00111101	
062	3E	C 842		00111110	
063	3F	C 8421		00111111	
064	40	None		01000000	Space
065	41	D BA 1		01000001	
066	42	D BA 2		01000010	
067	43	D BA 21		01000011	
068	44	D BA 4	ZAZ	01000100	
069	45	D BA 4 1		01000101	
070	46	D BA 42	AZ	01000110	
071	47	D BA 421	SZ	01000111	
072	48	D BA8	MVX	01001000	
073	49	D BA8 1		01001001	
074	4A	BA8 2	ED	01001010	¢
075	4B	BA8 21	ITC	01001011	
076	4C	BA84	MVC	01001100	<
077	4D	BA84 1	CLC	01001101	(
078	4E	BA842	ALC	01001110	+
079	4F	BA8421	SLC	01001111	I
080	50	A8 2		01010000	&
081	51	D B 1		01010001	
082	52	D B 2		01010010	
083	53	D B 21		01010011	
084	54	D B 4	ZAZ	01010100	
085	55	D B 4 1		01010101	
086	56	D B 42	AZ	01010110	
087	57	D B 421	SZ	01010111	
088	58	D B 8	MVX	01011000	
089	59	D B 8 1		01011001	
090	5A	B 8 2	ED	01011010	!
091	5B	B 8 21	ITC	01011011	$
092	5C	B 84	MVC	01011100	*
093	5D	B 84 1	CLC	01011101	)
094	5E	B 842	ALC	01011110	;
095	5F	B 8421	SLC	01011111	¬

Dec Val	Hex Val	Card Code DCBA8421	Mnem	EBCDIC	Symbol
096	60	B		01100000	–
097	61	A 1		01100001	/
098	62	D A 2		01100010	
099	63	D A 21		01100011	
100	64	D A 4	ZAZ	01100100	
101	65	D A 4 1		01100101	
102	66	D A 42	AZ	01100110	
103	67	D A 421	SZ	01100111	
104	68	D A8	MVX	01101000	
105	69	D A8 1		01101001	
106	6A	D BA8 2	ED	01101010	
107	6B	A8 21	ITC	01101011	,
108	6C	A84	MVC	01101100	%
109	6D	A84 1	CLC	01101101	
110	6E	A842	ALC	01101110	>
111	6F	A8421	SLC	01101111	?
112	70	D A	SNS	01110000	
113	71	D 1	LIO	01110001	
114	72	D 2		01110C10	
115	73	D 21		01110011	
116	74	D 4	ST	01110100	
117	75	D 4 1	L	01110101	
118	76	D 42	A	01110110	
119	77	D 421		01110111	
120	78	D 8	TBN	01111000	
121	79	D 8 1	TBF	01111001	
122	7A	8 2	SBN	01111010	:
123	7B	8 21	SBF	01111011	#
124	7C	84	MVI	01111100	@
125	7D	84 1	CLI	01111101	'
126	7E	842		01111110	=
127	7F	8421		01111111	"
128	80	DC		10000000	
129	81	CBA 1		10000001	
130	82	CBA 2		10000010	
131	83	CBA 21		10000011	
132	84	CBA 4	ZAZ	10000100	
133	85	CBA 4 1		10000101	
134	86	CBA 42	AZ	10000110	
135	87	CBA 421	SZ	10000111	
136	88	CBA8	MVX	10001000	
137	89	CBA8 1		10001001	
138	8A	DCBA8 2	ED	10001010	
139	8B	DCBA8 21	ITC	10001011	
140	8C	DCBA84	MVC	10001100	
141	8D	DCBA84 1	CLC	10001101	
142	8E	DCBA842	ALC	10001110	
143	8F	DCBA8421	SLC	10001111	

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Dec Val	Hex Val	Card Code DCBA8421	Mnem	EBCDIC	Symbol
144	90	CBA		10010000	
145	91	CB 1		10010001	
146	92	CB 2		10010010	
147	93	CB 21		10010011	
148	94	CB 4	ZAZ	10010100	
149	95	CB 4 1		10010101	
150	96	CB 42	AZ	10010110	
151	97	CB 421	SZ	10010111	
152	98	CB 8	MVX	10011000	
153	99	CB 8 1		10011001	
154	9A	DCB 8 2	ED	10011010	
155	9B	DCB 8 21	ITC	10011011	
156	9C	DCB 84	MVC	10011100	
157	9D	DCB 84 1	CLC	10011101	
158	9E	DCB 842	ALC	10011110	
159	9F	DCB 8421	SLC	10011111	
160	A0	DCB		10100000	
161	A1	DC A 1		10100001	
162	A2	C A 2		10100010	
163	A3	C A 21		10100011	
164	A4	C A 4	ZAZ	10100100	
165	A5	C A 4 1		10100101	
166	A6	C A 42	AZ	10100110	
167	A7	C A 421	SZ	10100111	
168	A8	C A8	MVX	10101000	
169	A9	C A8 1		10101001	
170	AA	DC A8 2	ED	10101010	
171	AB	DC A8 21	ITC	10101011	
172	AC	DC A84	MVC	10101100	
173	AD	DC A84 1	CLC	10101101	
174	AE	DC A842	ALC	10101110	
175	AF	DC A8421	SLC	10101111	
176	B0	C A	SNS	10110000	
177	B1	C 1	LIO	10110001	
178	B2	C 2		10110010	
179	B3	C 21		10110011	
180	B4	C 4	ST	10110100	
181	B5	C 4 1	L	10110101	
182	B6	C 42	A	10110110	
183	B7	C 421		10110111	
184	B8	C 8	TBN	10111000	
185	B9	C 8 1	TBF	10111001	
186	BA	DC 8 2	SBN	10111010	
187	BB	DC 8 21	SBF	10111011	
188	BC	DC 84	MVI	10111100	
189	BD	DC 84 1	CLI	10111101	
190	BE	DC 842		10111110	
191	BF	DC 8421		10111111	

Dec Val	Hex Val	Card Code DCBA8421	Mnem	EBCDIC	Symbol
192	C0	D	BC	11000000	
193	C1	BA 1	TIO	11000001	A
194	C2	BA 2	LA	11000010	B
195	C3	BA 21		11000011	C
196	C4	BA 4		11000100	D
197	C5	BA 4 1		11000101	E
198	C6	BA 42		11000110	F
199	C7	BA 421		11000111	G
200	C8	BA8		11001000	H
201	C9	BA8 1		11001001	I
202	CA	D BA8 2		11001010	
203	CB	D BA8 21		11001011	
204	CC	D BA84		11001100	
205	CD	D BA84 1		11001101	
206	CE	D BA842		11001110	
207	CF	D BA8421		11001111	
208	D0	BA	BC	11010000	}
209	D1	B 1	TIO	11010001	J
210	D2	B 2	LA	11010010	K
211	D3	B 21		11010011	L
212	D4	B 4		11010100	M
213	D5	B 4 1		11010101	N
214	D6	B 42		11010110	O
215	D7	B 421		11010111	P
216	D8	B 8		11011000	Q
217	D9	B 8 1		11011001	R
218	DA	D B 8 2		11011010	
219	DB	D B 8 21		11011011	
220	DC	D B 84		11011100	
221	DD	D B 84 1		11011101	
222	DE	D B 842		11011110	
223	DF	D B 8421		11011111	

Dec Val	Hex Val	Card Code DCBA8421	Mnem	EBCDIC	Symbol
224	E0	D B	BC	11100000	
225	E1	D A 1	TIO	11100001	
226	E2	A 2	LA	11100010	S
227	E3	21		11100011	T
228	E4	A 4		11100100	U
229	E5	A 4 1		11100101	V
230	E6	A 42		11100110	W
231	E7	A 421		11100111	X
232	E8	A8		11101000	Y
233	E9	A8 1		11101001	Z
234	EA	D A8 2		11101010	
235	EB	D A8 21		11101011	
236	EC	D A84		11101100	
237	ED	D A84 1		11101101	
238	EE	D A842		11101110	
239	EF	D A8421		11101111	
240	F0	A	HPL	11110000	0
241	F1	1	APL	11110001	1
242	F2	2	JC	11110010	2
243	F3	21	SIO	11110011	3
244	F4	4		11110100	4
245	F5	4 1		11110101	5
246	F6	42		11110110	6
247	F7	421		11110111	7
248	F8	8		11111000	8
249	F9	8 1		11111001	9
250	FA	D 8 2		11111010	
251	FB	D 8 21		11111011	
252	FC	D 84		11111100	
253	FD	D 84 1		11111101	
254	FE	D 842		11111110	
255	FF	D 8421		11111111	

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EBCDIC	Hex Val	Symbol	EBCDIC	Hex Val	Symbol and Cursor
0100 0000	40		0000 0000	00	
0100 0001	41	A	0000 0001	01	A
0100 0010	42	B	0000 0010	02	B
0100 0011	43	C	0000 0011	03	C
0100 0100	44	D	0000 0100	04	D
0100 0101	45	E	0000 0101	05	E
0100 0110	46	F	0000 0110	06	F
0100 0111	47	G	0000 0111	07	G
0100 1000	48	H	0000 1000	08	H
0100 1001	49	I	0000 1001	09	I
0100 1010	4A	¢	0000 1010	0A	¢
0100 1011	4B	.	0000 1011	0B	.
0100 1100	4C	<	0000 1100	0C	<
0100 1101	4D	(	0000 1101	0D	(
0100 1110	4E	+	0000 1110	0E	+
0100 1111	4F	|	0000 1111	0F	|
0101 0000	50	&	0001 0000	10	&
0101 0001	51	J	0001 0001	11	J
0101 0010	52	K	0001 0010	12	K
0101 0011	53	L	0001 0011	13	L
0101 0100	54	M	0001 0100	14	M
0101 0101	55	N	0001 0101	15	N
0101 0110	56	O	0001 0110	16	O
0101 0111	57	P	0001 0111	17	P
0101 1000	58	Q	0001 1000	18	Q
0101 1001	59	R	0001 1001	19	R
0101 1010	5A	↑	0001 1010	1A	↑
0101 1011	5B	$	0001 1011	1B	$
0101 1100	5C	*	0001 1100	1C	*
0101 1101	5D	)	0001 1101	1D	)
0101 1110	5E	;	0001 1110	1E	;
0101 1111	5F	¬	0001 1111	1F	¬

EBCDIC	Hex Val	Symbol	EBCDIC	Hex Val	Symbol and Cursor
0110 0000	60	-	0010 0000	20	-
0110 0001	61	/	0010 0001	21	/
0110 0010	62	S	0010 0010	22	S
0110 0011	63	T	0010 0011	23	T
0110 0100	64	U	0010 0100	24	U
0110 0101	65	V	0010 0101	25	V
0110 0110	66	W	0010 0110	26	W
0110 0111	67	X	0010 0111	27	X
0110 1000	68	Y	0010 1000	28	Y
0110 1001	69	Z	0010 1001	29	Z
0110 1010	6A		0010 1010	2A	
0110 1011	6B	,	0010 1011	2B	,
0110 1100	6C	%	0010 1100	2C	%
0110 1101	6D	_	0010 1101	2D	_
0110 1110	6E	>	0010 1110	2E	>
0110 1111	6F	?	0010 1111	2F	?
0111 0000	70	0	0011 0000	30	0
0111 0001	71	1	0011 0001	31	1
0111 0010	72	2	0011 0010	32	2
0111 0011	73	3	0011 0011	33	3
0111 0100	74	4	0011 0100	34	4
0111 0101	75	5	0011 0101	35	5
0111 0110	76	6	0011 0110	36	6
0111 0111	77	7	0011 0111	37	7
0111 1000	78	8	0011 1000	38	8
0111 1001	79	9	0011 1001	39	9
0111 1010	7A	:	0011 1010	3A	:
0111 1011	7B	#	0011 1011	3B	#
0111 1100	7C	@	0011 1100	3C	@
0111 1101	7D	'	0011 1101	3D	'
0111 1110	7E	=	0011 1110	3E	=
0111 1111	7F	≠	0011 1111	3F	≠

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CPU Tie-downs

The following tie-downs are required when the following memory features are installed:

Feature	Pin Location	To
12K or 16K memory	A-B2B2J02	A-B2B2B10
16K memory	A-B2B2B10	A-B2B2J04

2265 II Attachment Tie-down

If the LCD attachment is installed with the 2265 attachment, the tie-down required is 01A-B1N2G12 to 01A-B1Q2D12.

5444 Disk Attachment Tie-downs

Signal Name	Jumper from pin (on board A-A1)	TO: (on board A-A1)		
		If Model 1	If 1 or 2 Model 2(s)	If Model 2 and 3 Together
-100 Cylinder	R2G07	T2U07	T2G13	T2G13
-Model 6 CPU	R2P11	R2U11	T2U07	R2U11
+ Model 3 Ready	T2M08	T2J11	T2J11	T2U07
+'Spin 1 data unsafe'	C4J12	C4J08	Remove	Remove

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Chapter 2. Console and Maintenance Facilities

2.1 INTEGRATED MAINTENANCE PACKAGE (IMP)

System failures in the 5406 system, its I/O devices and attachments, are diagnosed with the aid of the IMP.

The IMP ties all maintenance equipment and information together and requires a minimum of recall about detail circuit operation.

The IMP consists of the following:

1. Maintenance Analysis Procedure (MAP) charts
2. CE aids
3. Diagnostic programs
4. FE education and FE publications

MAP charts are systematic flowcharts of failure analysis. Failure symptoms and/or a coded halt in a diagnostic program indicates the map chart to start with.

CE aids are: the CE probe, CE sense bits, single pin extenders, and MST card extenders. The MAP charts refer to these aids and call out when they are to be used.

Diagnostic programs are loaded and controlled by a diagnostic control program (DCP). The DCP may be modified by the CE to call specific test programs into use or perform a specific operation. Halts may occur during operation of the DCP or a diagnostic program that refers to a MAP chart for further diagnostic procedures.

FE education and FE publications expand on overall system and I/O device operation to aid in free-lance troubleshooting in the event that other IMP procedures fail to locate a problem.

For further information about IMP, MAPs, or the DCP, refer to the *Integrated Maintenance Package User's Guide,* the MAP charts, or the *Diagnostic Control Program User's Guide.* Each section contains a description and specific operating instructions for its use.

2.2 CONSOLE

The operator console contains the switches and lights necessary for operator control of the system. It is divided into two sections: system indicator lights, and system control switches.

2.2.1 System Indicator Lights

The system indicator lights section is divided into six parts. They are: system check lights, halt code indicator lights, field/operation indicator lights, keyboard ready light, command key indicator lights, and the system power on light.

Individual attention lights are provided for disk 1, disk 2, CRT, ledger card device, data recorder, SIOC, BSCA, and the printer. The processor check light is also displayed on the console.

The nine halt indicator lights, which are under program control, indicate to the operator a cause for system halt. The stop light (not under program control) indicates a halt when the stop switch is pressed.

The field/operation group of lights consists of eight lights that may be labeled by use of a plastic overlay. The program uses these lights to inform the operator at what point in the program he may enter specific data fields or take specific action.

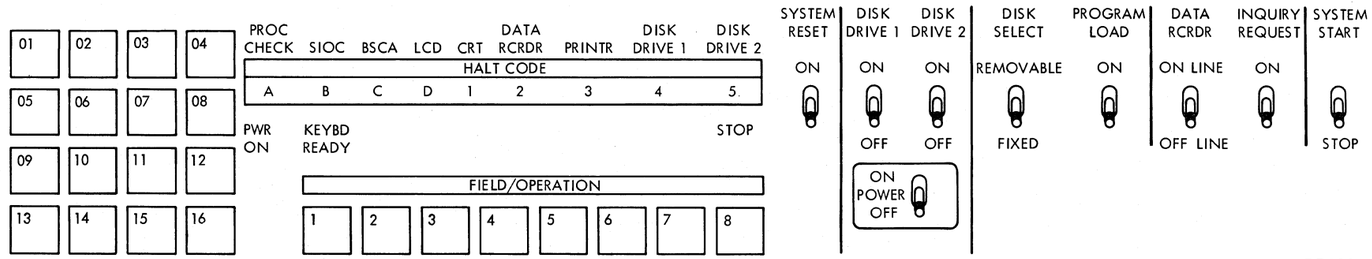
The command key indicator light group consists of eight (standard) or sixteen (feature) lights that are associated with the command keys on the operator keyboard. Command key indicator lights are turned on or off by program control (LIO instruction). In addition, the program can light a specific command key light whenever there is a need to communicate a predefined condition to the operator. Plastic overlays are provided for the lights so that the significant meaning for a light can be changed by typing on the overlay.

Processor Check Light (PROC CHECK)

The processor check light turns on whenever an invalid op code, CPU parity error or invalid SAR condition is detected. It is also turned on when an invalid Q code is detected. If the check stop switch (on the CE console) is set to STOP, the processor check light is turned on when an I/O parity error is detected. It is turned off by system reset or by pressing the check reset key on the CE panel. Any of these errors cause the processing unit to come to an immediate stop. The clock is stopped and the input/output data may be lost. The specific error that caused the stop is displayed on the CE console display section.

I/O Attention Lights

Any of the following lights on indicates that the corresponding I/O device has been issued a start I/O instruction but is not ready to operate. A not ready condition can be caused by power not being on, or by some condition involving the paper or cards to be handled by the I/O device. The I/O attention indicators are SIOC, BSCA ATTN, LCD, CRT, DATA RCRDR, PRINTER, DISK DRIVE 1, and DISK DRIVE 2. The specific conditions that cause each I/O light to turn on are discussed under the individual I/O devices.



Halt Code Lights

These lights are turned on by the individual bits (nine) and the halt identifier bytes of the halt program level instruction.

Power On Light

This light is turned on when system power-on sequencing has been successfully completed and stays on until system power is turned off.

Keyboard Ready Light (KEYBD READY)

This light is on when the keyboard has been enabled and unlocked.

Stop Light

This light is turned on when the system start switch is moved to the stop position and is turned off by moving the system start switch to the start position, or by system reset.

Field/Operation Lights

These lights are turned on by a load I/O instruction. The meaning of each light is determined by the program being used. A plastic overlay is provided for the field/operation lights so that appropriate labels can be applied. These labels identify the particular meaning given to the lights by the programmer. Once turned on, the field/operation lights remain on until another load I/O instruction specifying the field/operation lights is executed.

Command Key Lights

These lights are controlled by the load I/O instruction. Separate load I/O instructions are used to turn the command lights on or off. Once turned on, command lights remain on until a load I/O instruction turns them off, or until a system reset takes place. A plastic overlay is provided for the command lights so that appropriate labels can be assigned to each command light in order to identify the particular meaning given to the light by the programmer.

2.2.2 System Control Switches

The system control switches section includes those switches required for system powering, program loading, system starting, stopping, resetting, and I/O selection.

Lamp Test

This switch, located behind the hinged command indicator panel, is used to check for faulty indicator lamps.

System Reset Switch

When this switch is moved to the on position, a system reset occurs. A system reset causes the system to idle (become inactive) and resets all I/O and machine registers, I/O controls, and status indicators. The program IAR and the program status register LSR's are reset to zero in a system reset.

Normally, a complete program restart is required after a system reset has been performed.

Disk Drive 1 and Disk Drive 2 Switches

These switches apply electrical power to their respective disk drive motors.

Disk Select Switch

This switch selects the disk from which the initial program load will be performed. When the switch is moved to the removable position, sector zero of cylinder zero of the removable disk is used for program loading. Similarly, when the switch is in the fixed position, sector zero of cylinder zero of the fixed disk on disk drive one is used for program loading.

Program Load Switch

This switch initiates loading the program into main storage. The following actions occur when this switch is on:

1. All I/O and machine registers, controls, and status indicators are reset.
2. The instruction address register is set to zero.
3. The disk file data address register is reset to zero. The record in cylinder zero, sector zero on one of the disks in disk drive one is read into storage starting at location 0000. The disk that provides the first record is selected by the setting of the disk select switch on the console.

When the program load switch is released, the processing unit executes the instructions read into storage from cylinder zero, sector zero, starting at location 0000.

If disk drive one is not ready, the I/O attention light is turned on. When the program load switch is operated, it is necessary only to make disk drive one ready to complete the program load function.

Data Recorder Switch (DATA RCRDR)

Moving this switch to the on-line position places the data recorder under program control when the verify-punch switch on the data recorder is in the punch position. The data recorder keyboard is disabled. Data can be entered into the system from the data recorder reading station or punched at the data recorder punching station. Data and control can be entered from the system keyboard under program control.

Moving this switch to the off-line position places the data recorder under its own control and allows it to function as a normal (off-line) data recorder.

Note. Switches on the data recorder must be properly set for the data recorder to operate under program control (see page 10-109).

Inquiry Request Switch

This switch is mounted on the console, and although this key is not under keyboard bail interlock control, it operates as though it were a key on the keyboard. Moving this switch to the on position causes the data and status bytes to be stored in the keyboard attachment circuitry. Interrupt level one must be enabled for the CPU to recognize this switch. The status byte has the function key bit (bit 3) on and the data byte contains the unique data character code for the inquiry request key (0001 0001).

With the inquiry request switch on, the interrupt request latch sets if the program enabled the interrupt. At interrupt poll time, the interrupt request latch output will activate the 'interrupt polled KB' line which forces a keyboard bit 1 to the local storage register through the DBI channel. This signals a keyboard interrupt request to the CPU. When the CPU accepts the keyboard interrupt request, a sense instruction is issued to the keyboard to allow the data and status bytes (generated by the inquiry request switch) to enter the CPU on the DBI channel. These bytes point to the main storage location containing the keyboard sub routine to unlock the keyboard and turn on the keyboard ready indicator.

Prior to the initiation of the inquiry request signal, the keyboard is locked (bail bar forward) and the interrupt is enabled.

System Start Switch

When this switch is moved to the start position the processor resets the halt code lights and resumes normal operation. When this switch is moved to the stop position the processor halts at the end of the operation in process. This halt is indicated by turning on the stop light on the console. I/O data transfers are completed without loss of information. The system can be restarted without loss of information only by setting the switch to the start position.

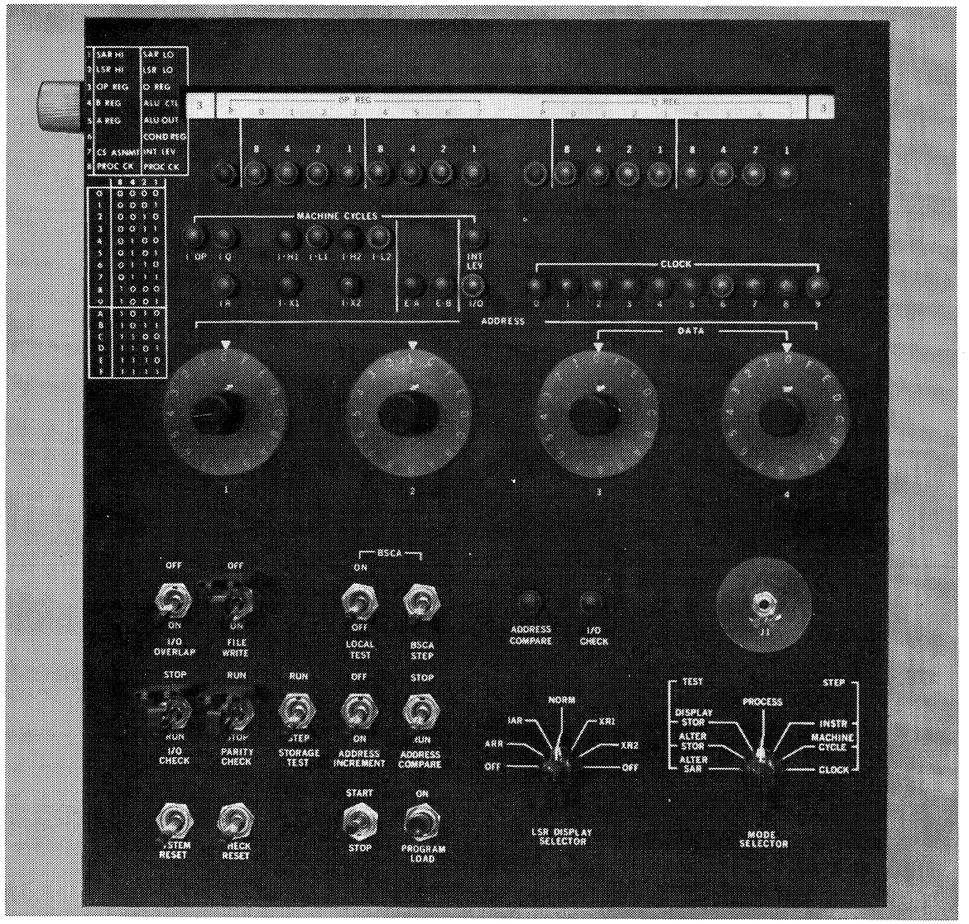
Power ON-OFF Switch

This switch controls the main electrical power to the system. When it is moved to the on position a partial system reset is generated and a power up sequence is started. The partial system reset prevents any I/O operations from starting until they are requested. The power up sequence is performed to apply the various voltages within the system in a manner to protect information in main storage. The on position of the power switch is interlocked with power supply safety circuits (overload protection and thermal circuits) and logic gate thermal protection. The system will not power up until the interlock circuits are complete.

In the off position, the system sequences the system power off in a manner to protect the information in main storage and opens the main power to the system. If an abnormal power off occurs (such as an electrical failure), the system will not sequence down properly and information in main storage may not be preserved.

2.3 FIELD ENGINEER CONSOLE PANEL

The FE control panel contains those switches and lights necessary for the field engineer to maintain the system. These controls and indicators are hidden behind a hinged panel and normally not used for customer operation. However, some of the switches on the FE console must be positioned correctly for the system to process in customer mode. The FE panel is located at the end of the CPU and may be removed from its normal mounting by lifting it upward. Support feet underneath the panel can be turned cross-wise to support the panel in an upright position. The cable attached to the panel is long enough to allow the panel to be placed on top of the CPU in position to be viewed while servicing the main gate of the CPU.



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2.3.1 CE Display Indicators

CE Rotary Display

The rotary display unit consists of a row of 18 lights and eight legend strips mounted on an eight position roller. At any one time, only one of the eight strips is visible through a cutout in the console above the row of lights. A knob in the upper-left corner of the panel is attached to the roller to turn it to each of the eight positions. Turning the roller to each legend position selects the register or check condition as defined in the legend strip and connects each light to indicate the conditions of the signals. The over-all view of the eight legend strips and a description of each position is shown below.

1	SAR HI	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7	SAR LO
2	LSR HI	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7	LSR LO
3	OP REG	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7	QREG
4	B REG	P	0	1	2	3	4	5	6	7		DIG CAR	DEC	RE COMP	ADD	SUB	TEMP CAR	AND	OR	ALU CTL
5	A REG	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7	ALU OUT
6											P			BIN OVF	TF	DEC OVF	HI	LO	EQ	COND REG
7	CSASNMT	P	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7	INT LEV
8	PROC CHK	I/O LSR	LSR F1	LSR F2	LSR HI	LSR LO	SAR HI	SAR LO	INV ADD	SDR	CAR	DBI	A/B	ALU	CPU DBO	OD/Q	INV OP	CHAN DBO	INV Q	PROC CHK

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1. SAR HI/SAR LO. Displays the contents of storage address register high and low.
2. LSR HI/LSR LO. Displays the contents of the LSR selected by the LSR display selector.
3. OP REG. Displays the contents of the op register.
   Q REG. Displays the contents of the Q register.
4. B REG. Displays the contents of the B register.
   ALU CTL. The state of the following ALU controls are displayed:

   DIG CAR (digital carry)
   DEC (decimal instruction)
   RE COMP (recomplement)
   ADD (addition)
   SUB (subtraction)
   TEMP CAR (temporary carry)
   AND
   OR
5. A REG. Displays the contents of the A register.
   ALU OUT. Displays the contents of the output of the ALU.

6. COND REG. The contents of the condition register is displayed as follows:

   BIN OVF (binary overflow)
   TF (test false)
   DEC OVF (decimal overflow)
   HI (high)
   LO (low)
   EQ (equal)

7. CS ASNMT. Cycle steal assignment is displayed as it is presented to the I/O devices on the I/O interface.
   INT LEV. Interrupt level indicates which I/O device is interrupting the program.

8. PROC CHK. The processor checks are displayed as follows:

   I/O LSR. Indicates selection of an LSR by an I/O device was not performed correctly.
   LSR F1. Parity is incorrect on the output of the LSR feature 1.
   LSR F2. Parity is incorrect on the output of the LSR feature 2. (This feature LSR is not used currently by the Model 6, but this position is reserved in the event of future expansion.)
   LSR HI. Parity is incorrect on the output of the basic LSR high.
   LSR LO. Parity is incorrect on the output of the LSR low.
   SAR HI. Parity is incorrect in the storage address register high.
   SAR LO. Parity is incorrect in the storage address register low.
   INV ADDR. The SAR contains an invalid address.
   SDR. Parity in the storage data register is incorrect.
   CAR. The carry out of the ALU is incorrect.
   DBI. Parity is incorrect in the data bus in register.
   A/B. Parity is incorrect in the A register or in the B register.
   ALU. Parity is incorrect in the ALU register.
   CPU DBO. Parity is incorrect on the CPU end of the data bus out to the I/O devices.
   OP/Q. Parity is incorrect in the op register or the Q register.
   INV OP. Invalid op code in the op register.
   CHAN DBO. Parity is incorrect on the I/O device end of the data bus out from the CPU.
   INV Q. An invalid Q byte is present in an I/O instruction.

Refer to the *Field Engineering Handbook System/3 Model 6,* order number ZY25-5501 for information to determine which check occurred first.

Machine Cycles

Twelve indicator lamps represent the twelve CPU machine cycles. They identify the processor cycle just completed in all modes of operation. However, when the CE mode selector switch is in clock step mode, the lamps indicate the cycle in progress. Except during an I/O cycle, no machine cycle indicator is on if (1) the CE mode switch is in the test position, (2) a system reset has occurred, or (3) an address compare stop has occurred, or (4) the stop key has been operated.

INT LEV

The interrupt level lamp indicates if any interrupt level is being serviced.

Clock

Ten lamps indicate machine clock cycles 0 through 9. If the CE mode selector switch is in one of the test or step modes, the clock is stopped at 9. In step mode the machine can be stepped through each cycle. Normal (process) mode uses only clock cycles 0 through 8.

Address Compare Lamp

This lamp comes on when the address set in the address/data switches matches the SAR. For this to occur, the rotary display switch must be in position 1(SAR). The system will not stop when the data matches unless the address compare switch is on. However, a sync point is available to indicate when an equal compare is made. See ALD KE 141.

I/O Check Lamp

This lamp is turned on when unit checks are detected by an addressed I/O device. The I/O check lamp can be turned off with a system reset, check reset or by the I/O attachment de-activating the I/O check interface line.

2.3.2 CE Controls

Address/Data Switches

These switches are used to set up addresses or data. Switches 1 through 4 can be used to load a 16 bit address into SAR. Switches 3 and 4 enter data into main storage: either 4 bits (switch 4) or 8 bits (switches 3 and 4) can be entered.

I/O Overlap Switch

This switch modifies control of the system so that I/O operations may be executed in either an overlap or a non-overlap mode. With the switch turned to the normal position of ON, I/O operations are executed in an overlap mode. When the switch is turned off, the I/O operation is completed before the next sequential instruction is executed. A mechanical interlock on the FE panel cover insures that the I/O overlap switch is in the on position with the cover closed.

File Write Switch

In the off position, this switch prevents writing on all disk surfaces. Its primary purpose is to permit analysis of file write problems without destroying information written on the file. A mechanical interlock on the FE panel cover insures that the file write switch is on, with the cover closed.

BSCA Switches (Local Test and BSCA Step)

The BSCA must be in a SIO test mode of operation for these switches to be effective. In the test mode, the switches allow the following actions:

Local Test Switch. Placing the BSCA in test mode removes the BSCA from the communications line for diagnostic testing purposes. Data transmitted is sent to the receive trigger to allow wrap-around operation. Test mode is used in conjunction with the external test switch. With the external test switch turned off, data is sent directly from the transmit trigger to the receive trigger; with the switch turned on, data is sent from the transmit trigger to the modem and then back to the receive trigger. The external test switch is located at the modem end of the medium speed cable. For high speed modems the switch is located on the CPU CE control panel.

BSCA Step Switch. Step mode allows stepping through a test operation by using the BSCA step key located on the CPU CE panel. The stepping operation can also be performed by using the machine cycle step or clock step and the CPU start key to step through each data phase and BCC phase within the bit time.

I/O Check Switch

This switch, when set to stop, forces the processor to an immediate stop on an I/O error. The console display is frozen to indicate the processor status at the time the error stop occurred. For normal operation, this switch is set to RUN.

To restart after an I/O error, activate CHECK RESET and then the start key.

Parity Switch

This switch, normally set to STOP, forces the processor to stop whenever a parity error is detected. Normal restart after a parity stop is to press CHECK RESET and then the start key. With the parity switch set to RUN, all parity errors are detected and displayed, but the processor stops for only some of the errors. The parity errors I/O LSR, INV ADR, INV OP, CHAN DBO, and INV Q are not affected by the setting of the parity switch and the processor will always stop on these errors. For all other errors, the processor will continue to run when the switch is in the run position.

Storage Test Switch

In the step position, a storage location is accessed with each depression of the start key. In the run position and the start key pressed, main storage is exercised by accessing either the same location repetitively or all of core sequentially.

Note: The storage test switch must be in the step position to avoid a processor check when changing the CE mode selector from alter storage position to display storage position or vice versa.

Address Increment Switch

This switch allows address incrementing when in the CE test modes of alter or display storage. With the switch on, the contents of SAR are incremented by 1 after each storage access. When the switch is off, SAR is not incremented.

Address Compare Switch

This switch allows a compare of the address/data switch setting and the register display when the register display is turned to SAR. When the address compare switch is in the run position, the address switch setting is compared to SAR through the register display, but no processor stop is initiated when a match occurs. The matched signal is provided as a sync point.

When the switch is in the stop position, a match of the address switches and the register display causes a processor stop at the completion of the storage read-write cycle. The processor is restarted by pressing the start key. I/O data transfer takes place without loss of information. The contents of SAR do not necessarily match the setting of the address switches when the processor stops.

System Reset Key

When this key is pressed, it resets all I/O registers, CPU registers, controls, and status registers, including the program status register (PSR) and the current IAR (P1 or P2 IAR) register to zero. System reset is operable only when the CE mode selector is set to the process mode.

Check Reset Key

This key resets the processor and I/O check conditions. Check reset removes the current error conditions and allows the processor to resume its operation after the start key is pressed. It also resets the system power-check function and allows a power-on retry.

Start/Stop Switch

In the start position, this switch takes the processor out of the stop or halt state, turns off the program stop lights, and allows the processor to resume its normal operation.

In the stop position, the processor halts at the end of the operation in progress. The halt state of the CPU is indicated by the stop indicator on the system keyboard console. I/O data is transferred completely and without loss of information. The processor can be restarted, without loss of information by placing the switch in the start position.

LSR Display Selector

This rotary switch selects the local store register (LSR) to be displayed in position 2 of the rotary display switch. The LSR's that can be displayed are the instruction address register (IAR), address recall register (ARR), index register 1 (XR1), and index register 2 (XR2). The selected LSR is displayed whenever the CPU is not in CPU or I/O cycles. When this switch is in the normal position, as it should be when the system is in operation, the CPU controls the selection and display of LSR's.

The off position is for CE use. In this position LSR's other than IAR, ARR, XR1, XR2, may be displayed by selecting the desired LSR manually as follows:

1. Turn the LSR display switch to OFF.
2. Turn the rotary display switch to position 2. (LSR Hi-Lo).
3. Tie up the desired LSR to −0.75 volts as shown below.

BASIC

To Display LSR's
Roller SW to Position 2, CPU not running
LSR Display Selector to off.
Tie up to LSR. See Tie Up Chart.

	U	S	
	o	2	o IAR INT 1
LLAR/CRT	o	3	o DFCR
AAR	o	4	o ARR/IAR
BAR	o	5	o PSR
	o	6	o
	o	7	o
	o	8	o
	o	9	o PCAR
ARR INT 1	o	10	o DRR/LCR
DRAR	o	11	o PDAR
IAR/ARR	o	12	o XR1
XR2	o	13	o DFDR

A-B2C2 ALD Page MA107

FEATURE 1

Example, to Display AAR:
1. Stop CPU
2. Turn roller display to position 2
3. Turn LSR display selector to off
4. Tie up B2-C2M08 to B2-C2U04.

	P	M	
	o	2	o
	o	3	o
	o	4	o
	o	5	o ARR INT 2
	o	6	o
	o	7	o
	o	8	o
	o	9	o
IAR INT 2	o	10	o CRTAR
	o	11	o
SIAR	o	12	o BSCAR
ARR INT 4	o	13	o IAR INT 4

A-B2D2 ALD page MA212

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Tie up chart

Device	+ Tie up	ALD Page
CPU	B2C2M08 B2B2M08	MA122 MA177
Disk	A1T2G13 A1S2M13 A1F2J04	GD201 GD211 GD326
Data Recorder	B1R2S09 B1T2G10	RP201 RP311
CRT	B1Q2D12	CT101
Keyboard	B1M2G11	PK024
Channel	B1J2P13	KE161
Printer	A2Q2D04 A2Q3D04 A2U2D04 A2S2J10 A2R2B04 A2M2G12	PR111 PR121 PR123 PR221 PR232 PR271
SIOC (B gate)	A1S4G08	

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CE Mode Selector Switch

This rotary switch selects one of three processor operating modes: process mode and two positions for CE use, test mode and step mode.

Process Mode. Process mode is the normal position for customer operation of the system. The CE mode switch should be left in this position before returning the system back to the customer for use.

Test Mode. In the test mode, data in core storage can be displayed by the CE panel indicators. Data set up in the address/data switches 3 and 4 can be entered into core storage, or the SAR address can be altered. A functional description of each test position is as follows:

1. *Display Storage.* The contents of main storage at the address specified by SAR, are transferred to the B register when the start key is operated. When the start key is released, the data is rewritten back into storage and transferred to the Q register.

   Note: In the test mode, invalid storage addresses are not checked, therefore the following SAR (Hi) bits are ignored:

   8K memory bits 0, 1, and 2,
   12/16K memory bits 0 and 1.

   A processor check will occur if the CE mode selector is changed from the alter storage position to display storage (or the reverse) and the storage test switch is not in the step position.
2. *Alter Storage.* Data set up in address/data switches 3 and 4, is transferred to the A register when the start key is operated. When the start key is released, the data is written into core storage at the address specified by SAR, and transferred into the Q register. Data may also be entered into main storage with the system console keyboard. This procedure is useful for hand-entering several continuous bytes of data into core storage. Data can be entered from the keyboard as follows:

   a. Load SAR with the main storage address where the first data byte is to be entered as per the instruction in alter SAR.
   b. Set the address increment switch to ON, and the storage test switch to STEP.
   c. Hexadecimal characters can now be entered by typing on the keyboard. Each byte is entered as two key strokes. After each second key stroke the hexadecimal character is entered into main storage and the address in SAR is incremented by one.

   Only the keyboard keys 0 through 9, and A through F can be used to enter data. The use of any other keyboard key results in a keyboard lockup. To unlock the keyboard, note the address in SAR, and perform a system reset to unlock the keyboard. Then reload SAR and retype the byte entered in error.
3. *Alter SAR.* An address set up in the address/data switches 1 through 4 is transferred into SAR through the IAR when the start key is operated. The IAR address will be the same as the address in SAR after an alter SAR operation.

   Note: When the CE selector switch is rotated through the alter storage position, it causes a keyboard bail reset and unlocks the keyboard. If this action is undesired, a system reset should be performed to relock the keyboard.

Step Mode. There are three positions in the step mode of operation. Each position controls the manner in which the processor performs the stored program.

1. *Instruction Step.* This mode causes one complete instruction to be performed with each operation of the start switch. The I-phase is performed when the switch is activated and the E-phase, if any, when the start switch is released.
2. *Machine Cycle Step.* This mode advances a program instruction through one machine cycle with each operation of the start switch. When the start switch is activated, data in storage is accessed, modified as required and the result displayed in the FE panel indicators. When the start key is released, the original data or the result (depending on the instruction operation) is written back into storage.
3. *Clock Step.* This mode advances the CPU clock through an odd-numbered clock cycle with each operation of the start switch, and an even-numbered clock cycle on the release of the start key.

   Note: The clock is allowed to run at the end of the I-phase during a start I/O instruction, until the I/O data transfer is complete. In the step mode, the start key is not functional during the time a I/O device is transferring data.

   Halt identifier lights do not turn on when the CPU is in the clock step mode.

Program Load Switch (Pushbutton)

This switch is functionally the same as the one on the keyboard console and initiates loading a program into main storage. The following actions occur when this switch is on:

1. All I/O and machine registers, controls, and status indicators are reset.
2. The instruction address register is set to zero.
3. The disk file data address register is reset to zero. The record in cylinder zero, sector zero on one of the disks in disk drive one is read into storage starting at location 0000. The disk that provides the first record is selected by the setting of the disk select switch on the console.

When the program load switch is released, the processing unit executes the instructions read into storage from cylinder zero, sector zero, starting at location 0000.

If disk drive one is not ready, the I/O attention light is turned on. When the program load switch is operated, it is necessary only to make disk drive one ready to complete the program load function.

J1

This jack is for connecting the alternate program load device (APLD) output signal to the CPU for diagnostic program loading or updating programs.

2.4 ERROR LOG AND STATISTICAL DATA RECORDING

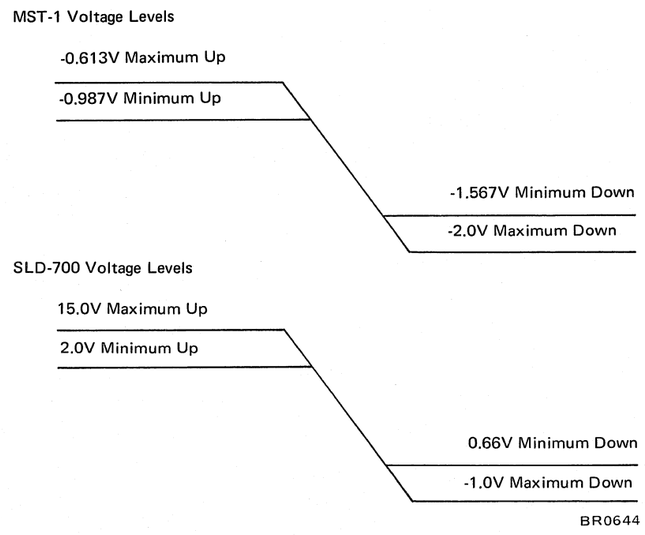
The System/3 Model 6 accumulates two types of error recording. All I/O device errors are recorded in an area called *out board recording* (OBR). Various counts of temporary errors (ones subsequently overcome by retry) and other statistical data are recorded in an area called *statistical data recording* (SDR). OBR I/O errors cause the Q, R, sense bytes and other data to be recorded in the OBR table located on sectors 7 and 8 of the fixed disk on drive 1. The most current OBR entry is found by using the first two bytes of sector 7 as displacement from the beginning of sector 7.

Sectors 3 through 6 contain 512 two-byte counters which are used to accumulate statistics about temporary and permanent I/O errors which have occurred. This data in these counters is called *statistical data recording*. SDR data is recorded on sectors 3 through 6 of the fixed disk on drive 1.

The OBR and SDR data are retrieved from the disk and printed on the printer by the CE utility program ERAP. The ERAP ID is FF7 and is called in via DCP.

2.5 VOLTAGE LEVELS

Acceptable voltage levels for monolithic system technology (MST)-1 and solid logic dense (SLD) 700 technology are:



2.6 ERROR RECOVERY PROCEDURES

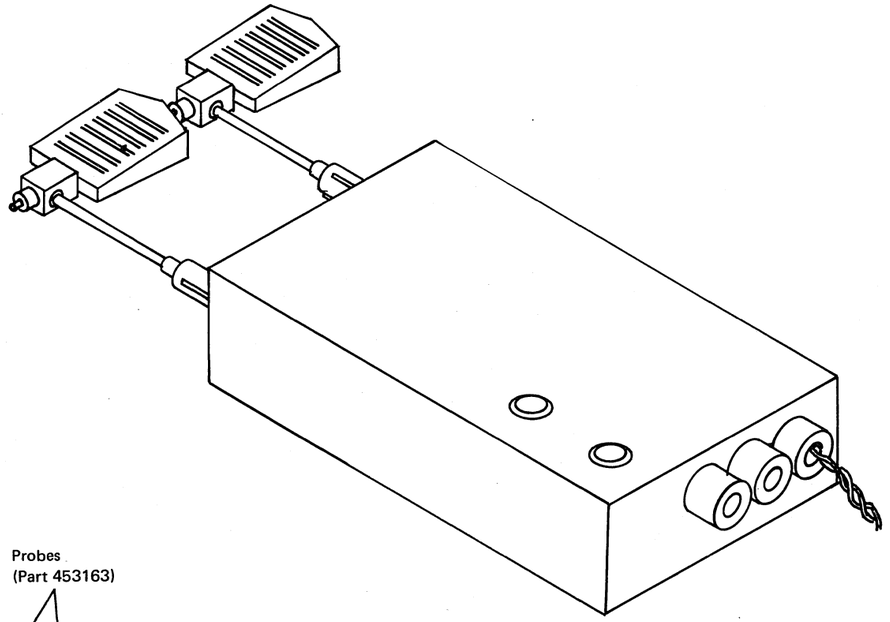
Refer to the system operating guide for operator recovery procedures indicated by the I/O attention lights on the console.

2.7 SPECIAL TOOLS

The following special tools used in troubleshooting System/3 are either included in the System/3 shipping group or are available from the branch office. See the *Integrated Maintenance Package User's Guide* for detailed descriptions of the tools.

2.7.1 CE Diagnostic Probe

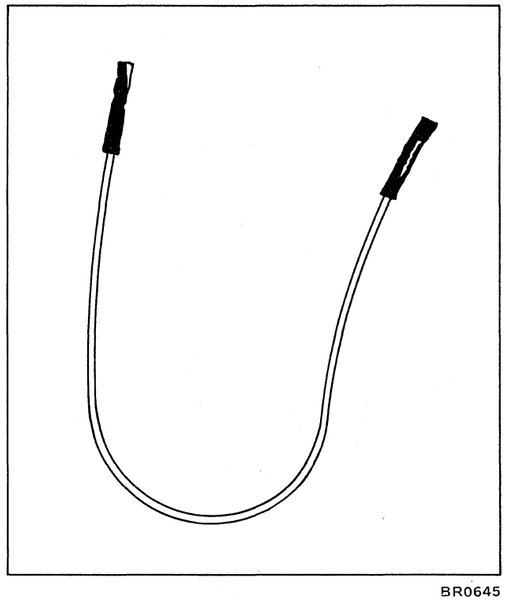
The CE diagnostic probe (see figure to the right, part 817971) acts as a free-running oscilloscope which replaces scope usage for most System/3 service calls. The probe can measure SLD 100/700 and MST-1 signal levels. The probe also has two MST-1 gates for gated operation. Consult the *Integrated Maintenance Package User's Guide* for specific levels that trigger the probe. The lamps (part 454612) and probe tips (part 453163), shown in the disassembled view of the probe (shown to the right), are field replaceable.



BR0646

2.7.2 Jumper Wires

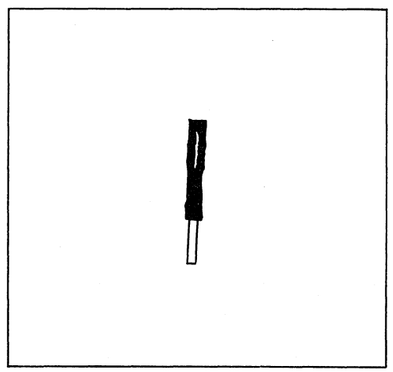
Six jumper wires (see figure below) are included in each 5406 shipping group; two 6 inch wires (part 829117), two 12 inch wires (part 2588263) and two 18 inch wires (part 829118). These jumpers are for use with the MAP charts and diagnostic programs.



BR0645

2.7.3 Single Pin Extenders

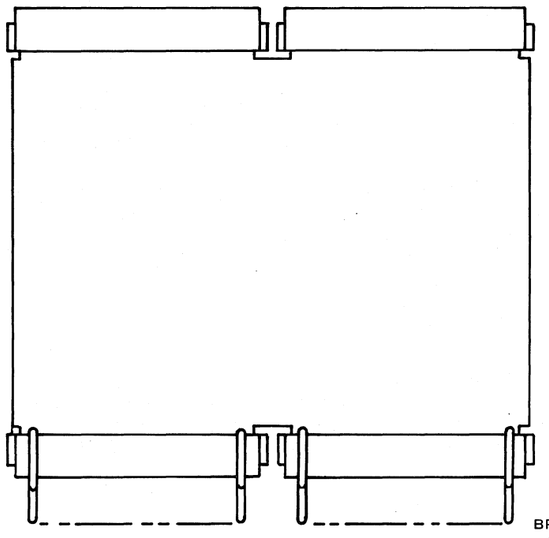
The single pin extender (shown below, part 2594238) is used to extend board pins when using the CE meter to measure voltage levels. The use of these pins eliminates shorting to adjacent pins when using the meter leads.



BR0647

2.7.4 MST-1 Card Extender

The MST-1 card extender (shown below, part 2360068) allows the CE to extend a card above the tops of adjacent cards on a board. This makes the module pins on the back of the card more accessible for probing with a scope or the diagnostic probe. These card extenders are stocked at the branch office.



BR0648

2.8 ALTERNATE PROGRAM LOAD DEVICE

The alternate program load device (APLD) is a cassette tape recorder that serves as an alternate input device to the Model 6. It is used to load file diagnostics when they are unavailable from the file due to a malfunction. It is also used to put revisions into the disk resident diagnostic program libraries.

2.8.1 Interface Circuits

The APLD attachment contains only pulse shaping circuitry. Error detection, tape speed synchronization, noise elimination, signal detection, data separation, and de-serialization functions are all performed by the tape loader program.

The interface circuits are contained on a single wide two high MST-1 card which is located on the printer attachment board (location A-A2B4). The function of the interface circuits is to convert the tape audio signals to machine readable MST-1 levels. They consist of:

1. 60 Hz noise filter
2. Comparator
3. Shaper
4. Level Converter
5. Polarity Hold Latch

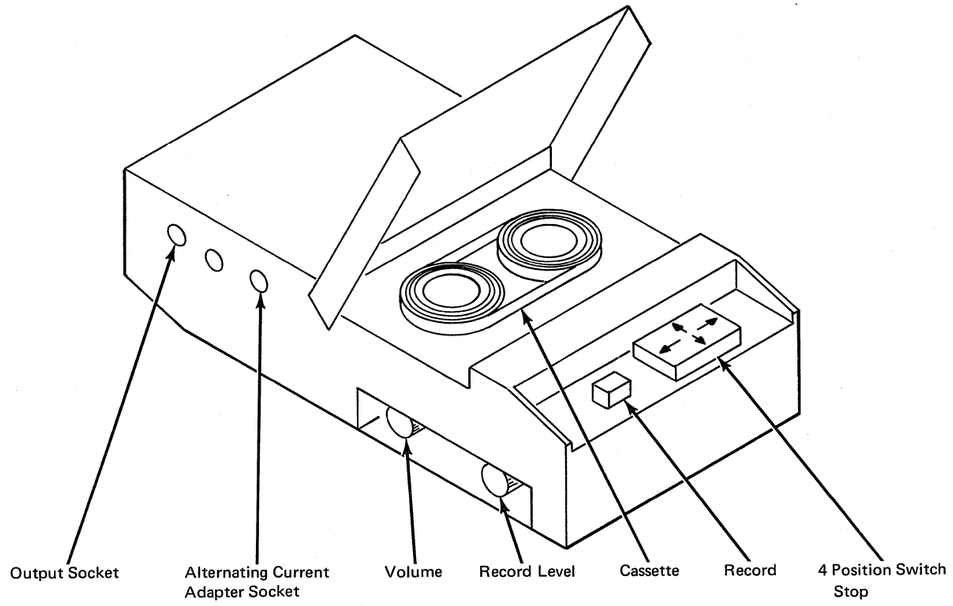
The read signal is first filtered to eliminate 60 Hz noise. It is then compared to a reference voltage, and a signal is generated at the comparator output when a positive input signal swing is detected. The generated comparator signal is shaped to the write signal pulse width by a single shot shaper. Then it is converted in the level converter to the desired logic level. The output of the level converter goes to a polarity hold latch which is conditioned during clock 2 of each CPU cycle. The output of the polarity hold latch is OR'ed with the 'printer busy' line. During a read data sample, the 'printer busy' condition is tested by performing a test I/O. When 'printer busy' is present during the sample, a binary 1 is placed in core. When it is not present during the sample, a binary 0 is placed in core.

2.8.2 Tapes

There are two types of tapes used with the alternate program load device.

1. The first type of tape consists of the tape loader and the diagnostic control program (DCP). To load this tape, a 38 byte bootstrap program must be manually entered into core. Following the loader and DCP, there are a number of file section programs.

2. The second type of tape takes the place of card input decks used with the editor program. This tape allows the editor to function nearly unchanged from its normal mode, except that the card read routine is overlayed with a tape read routine. The tape consists of card images of the editor data deck (one card per tape record). During operation, each time the editor program calls for a card input, a tape image of the card is read in rather than the card. To use the card image tapes, DCP and the editor programs must be fully loaded.



2.8.3 Programs

To load programs from tape, refer to the procedures contained in the *FE Diagnostic User's Guide.*

Bootstrap Loader

The bootstrap loader is a thirty-eight (38) byte manually entered program used to bring in the normal tape loader when the file is inoperable. This program contains no automatic tape speed synchronism, but instructions are provided in the tape MAPS for modification of timing constants if retry is required.

Bootstrap Loader:

Storage Address	Program	Program Description
005D	C202005D	Load address XR2 (005D)
0061	AFD9FFFF	SLC (branch from itself 218 times)
0065	E1E20E	TIO (for busy branch to 006B)
0068	E08708	BC to 0065
006B	ACFFFFFF	MVC 256 (approximately 772 us)
006F	AC62FFFF	MVC 99 (approximately 303 us)
0073	BA01FF	SBN (set bit on) at 015C
0076	E1E21F	TIO — (for busy branch to 007C)
0079	BB01FF	SBF at 01FC (set off)
007C	AED9FFFF	ALC (218 position binary counter)
0080	E02008	BC — binary overflow

Tape Loader (Normal)

The tape loader is a three hundred fifty (350) byte tape read program with the following features:

1. Tape speed synchronization.
2. Error detection (record hash total).
3. Specification for length of data record and address where data is to be placed in memory.
4. Record number.
5. FE communication via command and field indicator lights.
6. Record identification (any normal input card for diagnostic control program and/or section programs).
7. Bit count (overflows beyond 8 bits are ignored).
8. Provision for restart in case of soft tape errors.

Diagnostic Control Program (DCP)

This is the standard DCP modified for tape use, and can be read in from the cassette so that it can be used with the file diagnostics.

2.8.4 File Diagnostics

These are the complete set of file diagnostic programs in sequential order. They are coupled with the MAPS for fault locating.

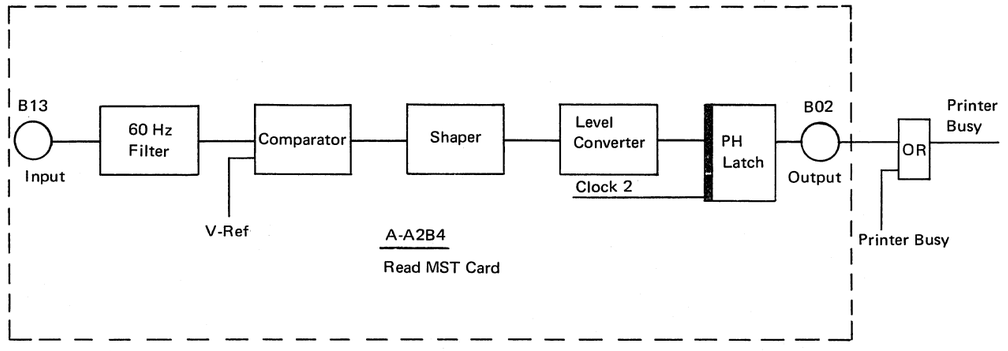
2.8.5 APLD Setup

1. Connect the 7.5 Vac adapter from the ac adapter socket to the ac convenience outlet.
2. Connect the shielded audio cable from the cassette output socket to J1 on the CE panel.

   Note: When the audio cable is plugged into the cassette output socket, the cassette speaker is disabled.
3. The volume control setting should be approximately 6.
4. The read MST card is plugged into location A-A2B4.

2.8.6 Maintenance

For maintenance of the tape cassette, refer to the manufacturers handbook issued with the tape cassette.



BR0650

Chapter 3. Preventive Maintenance

3.1 SCHEDULED MAINTENANCE

The preventive maintenance philosophy for the System/3 Model 6 is that it is done during unscheduled interrupts whenever possible. When an unscheduled interrupt does not occur on a system within the time limits specified below, scheduled maintenance is performed as follows:

1. Blowers—check every six months for proper operation.
2. Filters—replace every six months, if necessary.
3. Memory—no preventive maintenance is performed if the memory is operating properly. If adjustments are required, the XYZ drive voltage is varied from −30V by ±1.2V while exercising the BSM with a worst case pattern. This should establish an operating point. Adjustments are made using the voltmeter specified in chapter 4.

Chapter 4. Checks, Adjustments, and Removals

4.1 MONOLITHIC SYSTEM TECHNOLOGY (MST) MAINTENANCE

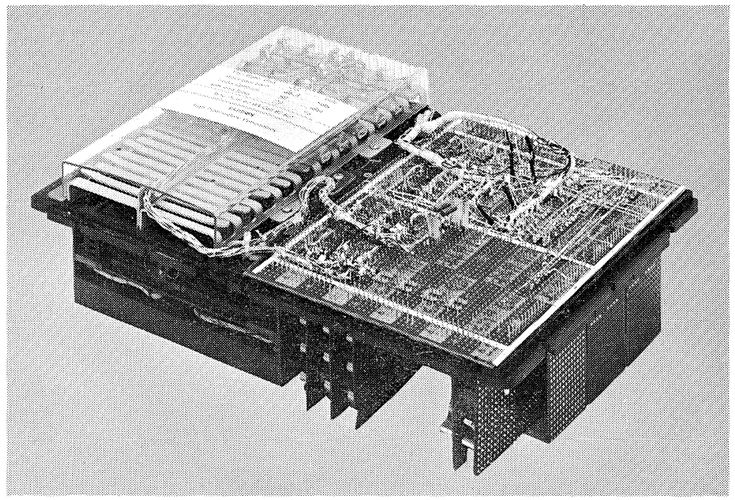
All normal maintenance procedures for monolithic system technology components are found in the IBM Field Engineering Theory of Operations Manual, *Monolithic System Technology Packaging, Tools, and Wiring Change Procedure.* This manual includes information regarding:

MST packaging
Tools
Wiring change procedure
Emergency card repair

4.2 MONOLITHIC TECHNOLOGY SYSTEM CARDS

The lettering within a logical block on a systems diagram page gives the location of that block in the card gates. It also indicates other pertinent data as described in the MST packaging FETOM (described above). Identification of pins, panels, rows, and columns is also described in this manual.

Logic block locations within the system diagrams are shown on system diagram card location charts. The system index contains the machine features indexing of automated logic diagrams (ALDS) and maintenance diagrams.



8K Basic Storage Module (Probe Side)

BR1749

4.3 BRIDGE BASIC STORAGE MODULE (BSM)

For reliable storage operation, the BSM diagnostics should run 2 minutes without errors when the –30 volt XYZ drive voltage is biased 1.2 volts in either direction from its initial setting. If BSM operation is unreliable, a fault exists, or XYZ drive voltage (–30V) reoptimization is required, or strobe setting and –30V reoptimization is required.

Proper setting for the –30V power supply and the strobe settings for each BSM are recorded on a decal located on the XYZ current limiting resistor cover (see the figure to the right).

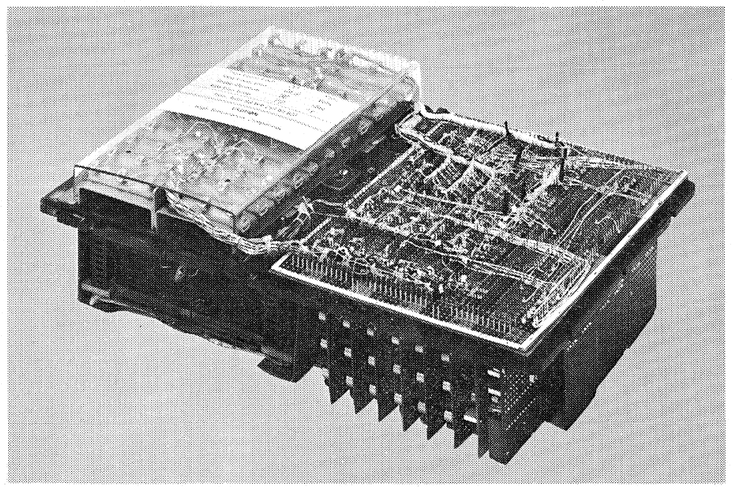
Note: The –30V power supply is self-adjusting for temperature and adjusts by –75 mV for each degree Fahrenheit temperature rise.

If the BSM operation is unreliable, a fault should be the first problem suspected. The only repairs possible are card replacement, voltage and strobe adjustments, and repair of minor (visible) shorts, open diodes, or open circuits. Major array failures (shorted diodes, internal opens, etc.) necessitate BSM replacement.

Most problems fall into 2 categories of component failures.

1. Normal circuit failures (card, loose connector, etc.)
2. Array failures (shorted lines, open line, diode, etc.)

Intermittent or random failures are treated separately.

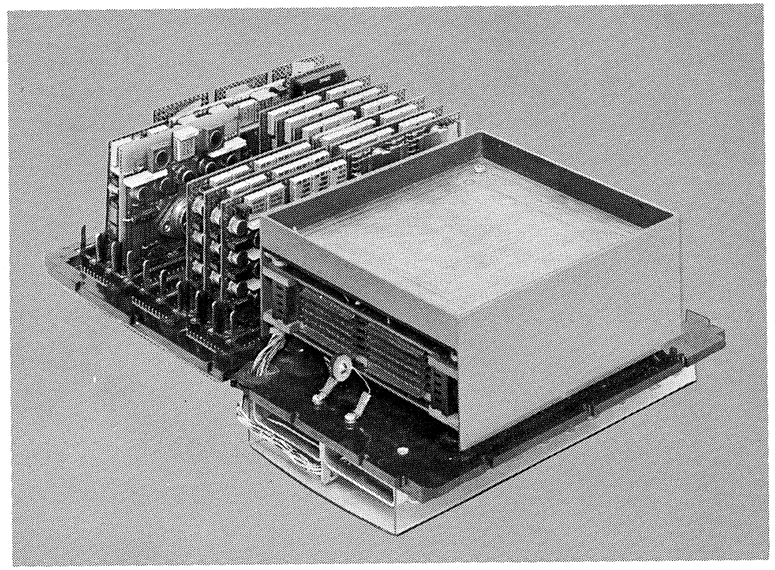


16K Basic Storage Module (Probe Side)

BR1750

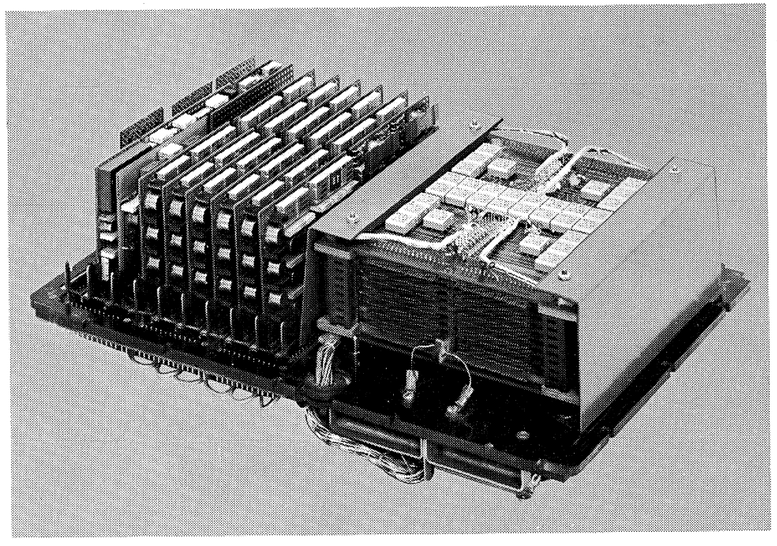
4.3.1 Fault Location

If a failing pattern is not already evident, try manually storing and displaying or scanning storage to establish a pattern. If this fails, run the storage diagnostics.



8K Basic Storage Module (Card Side)

BR1751



16K Basic Storage Module (Card Side)

BR1752

4.3.1.1 Circuit Failures

All BSM problems should be approached as if there has been a circuit failure. Circuit failures (card, connector, etc.) can be broken into distinct patterns. For example:

- Single bit—all addresses
- Single bit—one block of addresses
- Multiple bits—all addresses
- Multiple bits—one block of addresses

The 'all addresses' failure could be caused by the drive current source card or the control driver card. The 'block of addresses' failure could be caused by a defective gate driver card. For example, if SAR bit 7, 8 or 9 are always active in the failing address, the chart in the figure indicates the failure could be the Y-Lo gate driver.

Single-bit or multiple-bit failures may be caused by a sense/inhibit card which also contains the SDR latch for that bit.

Card location

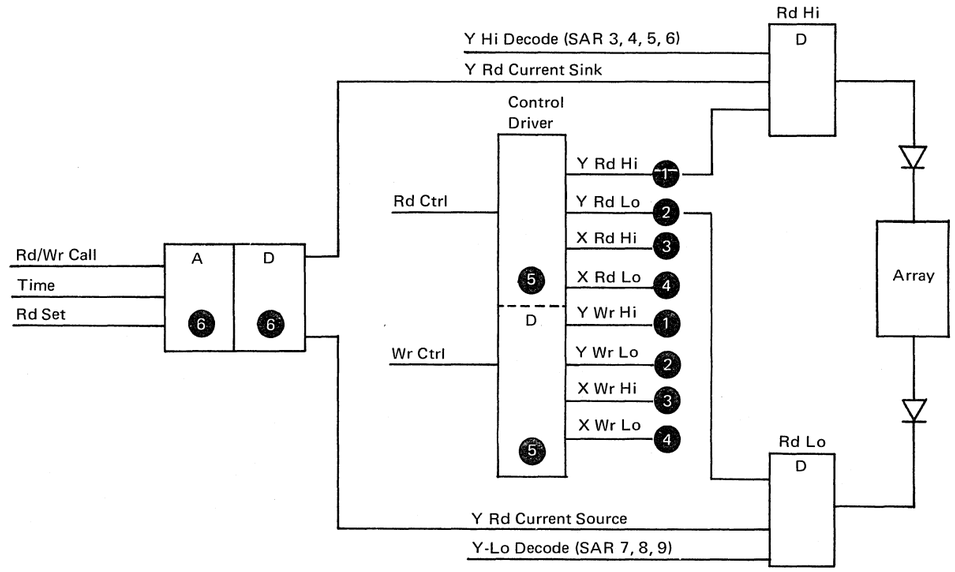
Bits	8K BSM	16K BSM
0, 1, 2	XXJ4	XXJ4
3, 4, 5	XXH4	XXH4
6, 7, 8	XXG4	XXG4
9, 10, 11	—	XXF4
12, 13, 14	—	XXE4
15, 16, 17	—	XXD4

Note: Bits 9-17 are 0-8 when SAR bit 2 is active. Bit 8 and 17 is the P bit

BR1753

Multiple-bit failures at all addresses may also be caused by the strobe driver card. (For card location, see ALD page SR224.)

Using bridge map charts (trouble analysis flowcharts) allows repair of most of the failures by swapping or replacing cards. Use the CE pocket meter and diagnostic probe for help in locating and repairing the trouble.



			❶	❷	❸		❹	❺	❻
			Gate-Driver Location					X-Y Gate Control Driver	X-Y Rd/Wr Drive Current Source
			Y Hi	Y Lo	X Hi	X Hi B	X Lo		
SAR Bits	1	2	3 4 5 6	7 8 9	10	11 12	13 14 15		
8K-16K BSM	BSM Selection	Byte Control (not used on 8K)	XXG2 XXH2	XXF2	XXE2	Not Used	XXD2	XXB2	XXJ2
ALD Page →			SR061 SR062	SR051	SR041	SR043	SR031	SR021	SR022

BR1754

4.3.2 Array Failures

If the array fails, replacement is necessary unless the failure can be traced to cabling defects, visual defects, or an open diode. Trouble caused by open diodes can be repaired by patching a new diode across the open one. Shorted diodes require replacing the array.

4.3.2.1 Single Bit, Multiple Address Failures

A sense/inhibit (S/Z) problem usually shows up as an extra or missing bit throughout an 8K block of storage (each sense/inhibit line passes through 8,192 cores). If the sense/inhibit card is not at fault, check the wiring to the inhibit current limiting resistor. (Refer to SR071-076 and to SR264 for locations.) Check that –30 volts appears on pin 2 of the affected resistor.

Check also for a broken S/Z wire between the array and the back panel pins on the sense amplifier. A complete S/Z winding resistance should measure approximately 14.0 ohms. If the open or shorted S/Z winding is within the core plane, replace the BSM.

4.3.2.2 Multiple Bits, Multiple Address Failures

If this type of failure cannot be corrected by card swapping or replacement, an array fault probably exists. If the failure is related to a combination of more than one address pattern, suspect a short between drive lines.

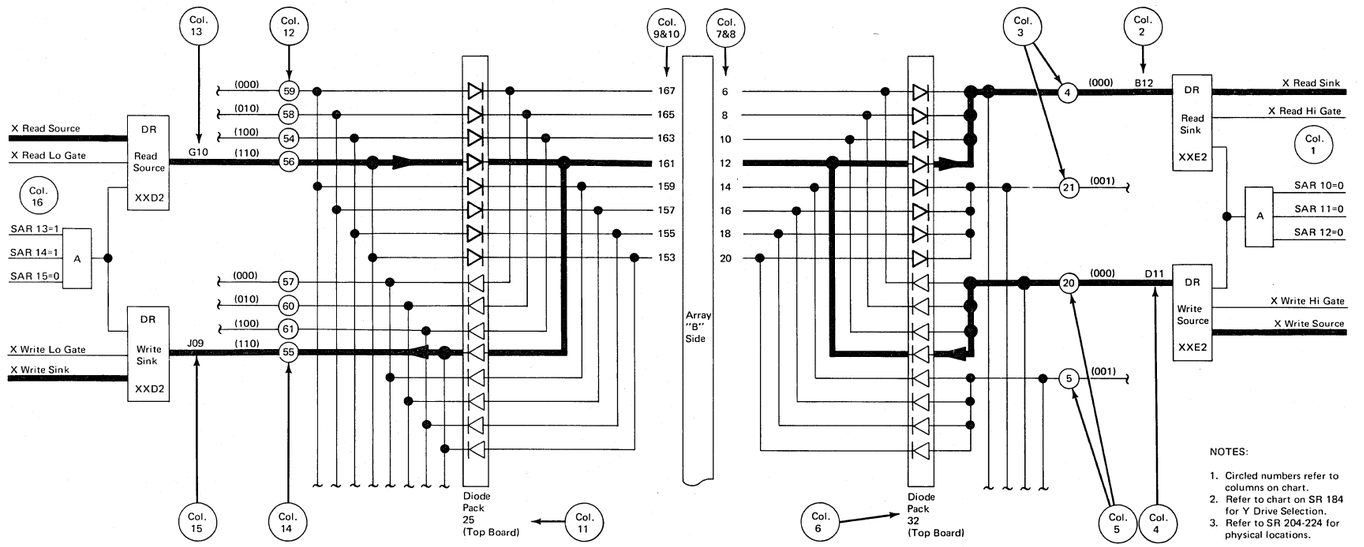
4.3.2.2.1 Continuity Check of XY Drive Lines. The charts on SR174 and SR184 describe all X and Y drive lines and contain all the points (terminals) for performing a continuity check. Example: See the figure to the right.

This example is for the failing X-address of 000110. X-read current is shown from left to right through the array X-winding. X-write current is shown from right to left through the same array X-winding.

(In the following discussion, column numbers refer to the chart on SR174.) Starting from the X-read lo gate, D2G10 (column 13) current flows to terminal 56 on the top diode board (column 12), through a diode in diode pack 25 on the top diode board (column 11), to pin 161 on top diode board (column 9), through the X-winding to pin 12 on the top diode board (column 7), through a diode in diode pack 32 on the top diode board (column 6), to terminal 4 on the top diode board (column 3) to the X-read hi gate, E2B12 (column 2).

Likewise, it can be seen that X-write current flows from the X-write hi gate, S2D11 (column 4), in the reverse direction through the X-winding, to the X-write lo gate, D2J09 (column 15).

4.3.2.2.2 Locating an Open Diode. Because of the complex connections of the isolation diodes, a continuity check is difficult. To locate an open diode, use the method described next. The cards named are for the same failing X-address (000110) discussed in Section 4.3.2.2.1. Refer also to the figure on the next page, "Locating an Open Diode."



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
HI ORDER										LOW ORDER					
HI ORDER ADDRESS	DRIVE LINE PINS				DIODE PACK HI ORDER TOP BOARD	CORE LINE GOING				DIODE PACK LOW ORDER TOP BOARD	DRIVE LINE PINS				LOW ORDER ADDRESS
	READ SINK		WRITE SOURCE			FROM		TO			READ SOURCE		WRITE SINK		
SAR BITS 10 11 12	LARGE BOARD	TOP DIODE BOARD	LARGE BOARD	TOP DIODE BOARD	PACK NO.	PIN NO.	ARRAY SIDE	PIN NO.	ARRAY SIDE	PACK NO.	TOP DIODE BOARD	LARGE BOARD	TOP DIODE BOARD	LARGE BOARD	SAR BITS 13 14 15
										SR 174					
	E2B12	4	E2D11	20	32	12	B	161	B	25	56	D2G10	55	D2J09	1 1 0

Diode Locations

BR0654A

1. Turn off power.
2. Remove X gate cards D2 and E2.
3. Probe the points shown with the ohmmeter; be sure to observe the polarity of the meter as indicated by the + or –. Expected meter readings are infinity (∞) or some resistance (R, unpredictable because of circuit variations and the meter in use).

An open drive line may also be verified by scoping the source driver load resistor on the resistor panel. See page 1-408 "Scope Pictures F" for the waveform of the Y-read current source with and without an open diode (see SR264). This method will identify an open array drive line if both YRD and YWR appear open. If either is correct, an open diode is likely. Make a continuity check to determine which of the two diodes in the line is open.

If an open diode exists, the charts of SR174 and SR184 indicate the polarity of the diode to be replaced. See the bottom of the figure above for diode locations with respect to the charts.

4.3.2.2.2 Replacing an Open Diode. An individual diode cannot be removed since it is part of a module containing 16 diodes. Replacement consists of soldering an individual GY diode (part 2414891) over the defective one. (A shorted diode calls for replacement of the BSM.)

When replacing a diode, use thermal set compound (part 814007) as a heat sink. Wrap one end of a yellow wire to the wrap terminal on the diode board and solder the other end to the diode. Solder the remaining end of the diode to the solderable pin on the edge of the diode board. After diode replacement, check for reliable BSM operation.

4.3.2.2.4 Exposing Bottom Diode Board. If an open Y-drive line exists and the fault cannot be located on the top diode board, remove the BSM to expose the bottom diode board.

1. Disconnect all cables to the BSM.
2. Remove all the cards.
3. Remove the BSM (weight—approximately 18 pounds) and lay the unit on a table with the card side down, pin side up.
4. Loosen the 4 nuts which hold the array onto the board. It is now connected by only the drive and sense-inhibit cables.

   Note: It is now possible to raise the board separately leaving the array resting on the table and expose the bottom diode board, or you may continue.
5. Turn the unit over. Support the array since it is connected only by wiring.
6. Pull the array out vertically and turn it over so that the top side is down and lying on the card sockets. The bottom diode board is now completely exposed.

4.3.2.2.5 BSM Replacement. Some systems supply –30 volts to the BSM with a single 'mini-bus' connector to the following points: C5D09, D5D09, E5D09, F5D09, G5D09, H5D09, and J5D09 (see SR264). Earlier systems supplied –30V with a single wire to C5D09. The remaining points were jumpered on the board. This includes the associated D08 ground pins.

When replacing a BSM it may be necessary to save the jumpers for use on the new BSM if your system does not use the 'mini-bus' connector.

4.3.2.3 Poor Solder Connections and Welds

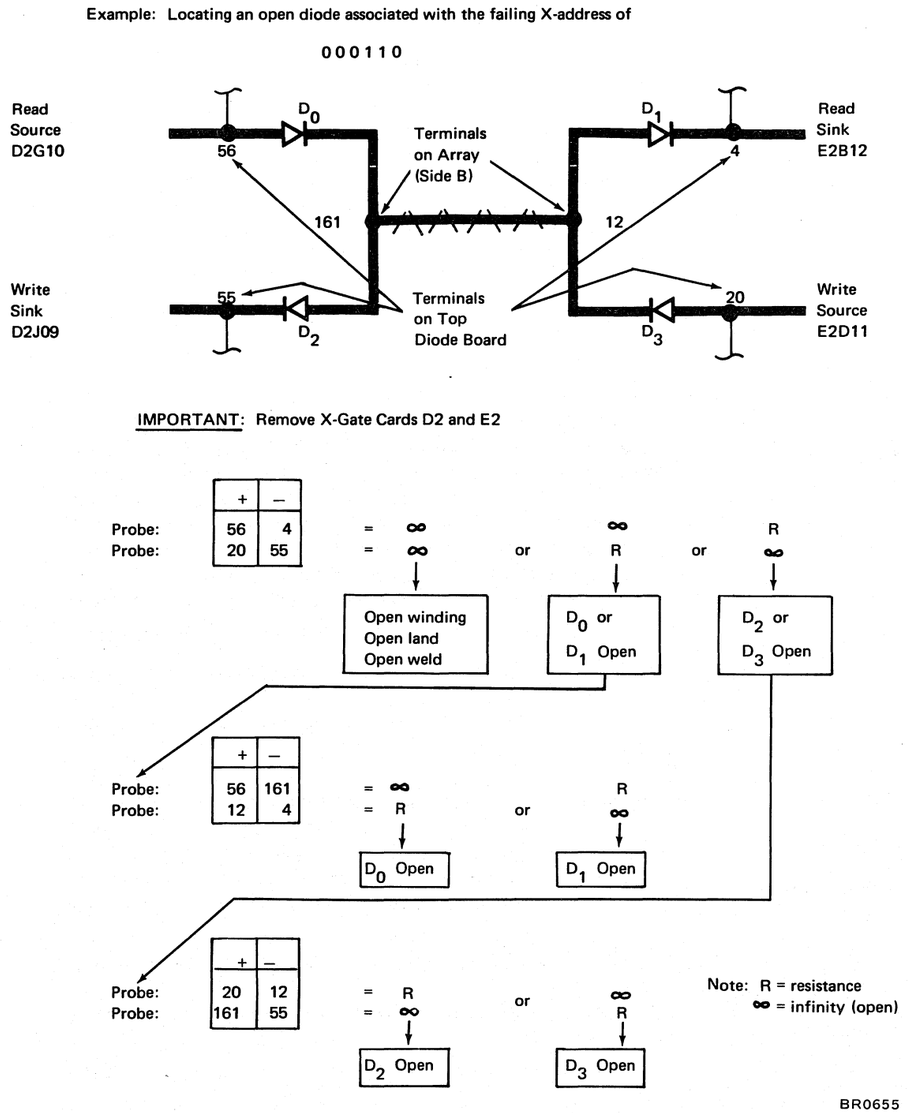
If a problem appears to be an open diode or an internal open within the array, a complete resistance check should be made. Any poor solder connections or welds should be resoldered.

Also check for an open land pattern in the X-return card (for an X-drive line). If there is an open land pattern, use a piece of #30 wire to repair the break.

4.3.2.4 Shorts Between Drive Lines

Shorts between X- or Y-drive lines usually show up as dropping one or more bits of two addresses. In almost all cases, analysis of the failing addresses shows that two adjacent X- or Y-drive lines are the problem. Once the two lines are located, make a resistance check of the lines, moving from one end of the array to the other. Because of the resistance of the windings, less resistance is seen as you get closer to the short.

In almost all cases, the short is either some foreign material between two adjacent pins or two pins touching. A visual check with a strong light may show the short. However, if foreign material is causing the short, it may not be visible. Try passing a piece of paper between the pins at the area of the short.



4.3.2.5 Defective Cores

A defective core position usually shows up as dropping a single bit in a single address. This type of problem can be caused by the individual core losing its magnetic properties because it is cracked, chipped, or broken.

Vary the −30V drive voltage and the strobe setting to see if the rate of failure changes. If you are unable to obtain a reliable operating position, BSM replacement is necessary. See 4.3.4 and 4.3.5 for drive voltage and strobe reoptimization.

4.3.3 Intermittent or Random Failures

If a failure pattern cannot be determined, check the following for possible failure causes.

1. Using an oscilloscope, probe the:
   a. XY drive voltage pulses on the XY read and write current limiting resistors and compare them to those shown in BSM waveforms B, C, D and E, page 1-407 and 1-408.

      Note: Probe pins 1 and 3 are common. No pulse can be observed on resistor pin 2, since it is ground.

   b. Z drive voltage pulses on the Z (inhibit) current limiting resistors and compare them to those shown in BSM waveform F, page 1-408A.

      Note: No pulse can be observed on resistor pin 2 since it is the −30V power supply connection. Note also that the magnitude of the pulses may vary slightly if the XYZ drive voltage setting is not at −30V. (XYZ drive voltage supply is a temperature correcting supply.)

   c. Control driver (BSM waveform G, page 1-408A).
   d. Strobe driver (BSM waveform H, page 1-408B).
2. Check for improper setting of the −30V, +6V, −4V, −14V, and/or +3V. (Use a Weston 901 meter or equivalent when adjusting these voltages.)

   Note: The +3V supply should be adjusted with reference to +6V. This results in a negative reading.
3. Check the voltage connectors to the large circuit board. (See SR264.)
4. Check to see if the back panel resistor assemblies are misplugged. (See SR264.)
5. Check for loose interface cables or terminator cards. (See SR 201, 224, 228, 229.)
6. Check for improper MST-1 levels at the interface.

4.3.4 XYZ Drive Voltage (−30V) Reoptimization (8-16K)

Reverify drive voltage marginal limits whenever replacing S/Z, timing, driver source, or strobe driver cards.

To reoptimize the drive voltage:

1. Loop storage diagnostics no. 96.
2. Determine the upper drive voltage (−30V) limit by slowly decreasing the drive voltage reading until an error occurs. Record the last operating voltage as the upper limit. If system reset and start does not start the diagnostic, set the drive voltage close to normal and reload the diagnostic. Determine the lower limit by slowly increasing the voltage reading until an error occurs (do not exceed a more negative voltage than −35V). Record the last operating voltage (or −35V) as the lower limit.

   Note: The BSM should run error free for a minimum of 30 seconds at the last operating point.
3. The optimum drive voltage is the average of the upper and the lower BSM limits.
4. If the difference between the upper and lower limits is less than 2.4 volts, strobe reoptimization may be necessary.

   Note: When reoptimizing the drive voltage or strobe setting, a thermometer (part 5392366 or any standard thermometer) placed at the base of the array should read between 68 degrees and 86 degrees Fahrenheit. The voltage may be reoptimized outside of this range, but a check at the current temperature should be made as soon as possible.

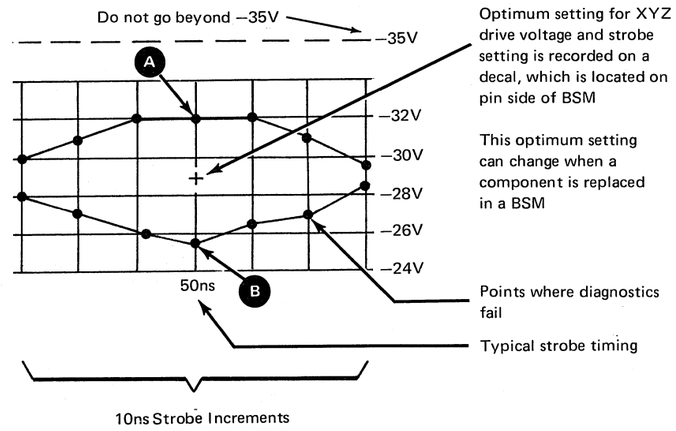
4.3.5 Strobe Setting Reoptimization (8-16K)

To reoptimize the strobe setting:

1. Loop storage diagnostics no. 96.
2. Refer to the decal on the XYZ current limiting resistor cover. Use the present strobe setting and determine the upper and lower XYZ drive voltage limit, which is explained by 4.3.4 step 2. Record these limits as shown by point A and B in scope picture A (on this page). Repeat 4.3.4 step 2 for strobe setting 10, 20 and 30 ns before and after the present strobe setting. Strobe settings are made on the strobe driver card (SR254). Plot the XYZ drive voltage limits as shown in the figure. Set final strobe timing between points where the XYZ driver voltage limits start to drop off.
3. If the difference between the upper and lower limits is less than 2.4 volts, a fault probably exists which must be corrected before further reoptimization is attempted.
4. Set the optimum drive voltage (−30V) which is the average of the upper and lower BSM limits at the selected strobe setting.
5. BSM access time is measured from when 'Rd call/Write call' becomes active, until all sense data latches are active. (Measure access time while writing all ones into the BSM.) Access time must be 445ns or less. If necessary, reset the strobe setting to obtain 445ns or less.

   The minimum 2.4 volt spread for XYZ voltage must still be met at the new setting.

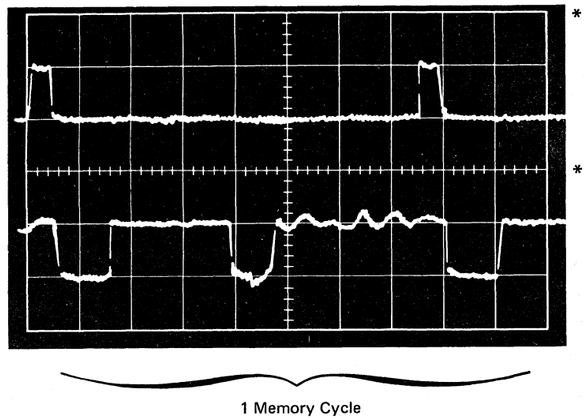
   Note. If the strobe driver card is replaced, strobe jumpers must be put in the new strobe driver card.



Scope Picture A
Optimization—Strobe and XYZ Drive Voltage

BR1775

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



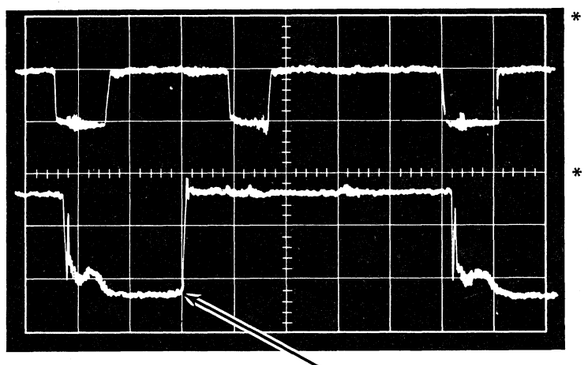
1 Memory Cycle

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4B3G03 (8K-16K BSM)
Signal Name: Reset

Channel 2
Vertical Gain: 1 V/cm
Signal Pin: B4A2B02 (8K-16K BSM)
Signal Name: Rd Call Wr Call

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



*Ground

Lower level determined by -30Vdc setting

BSM Waveforms B

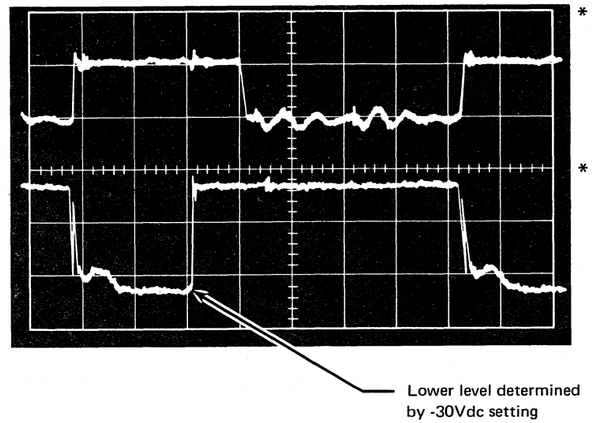
Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4A2B02 (8K-16K BSM)
Signal Name: Rd Call Wr Call

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J2G05 (8K-16K BSM)
Signal Name: X Rd Current Source Resistor

BR0657A

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



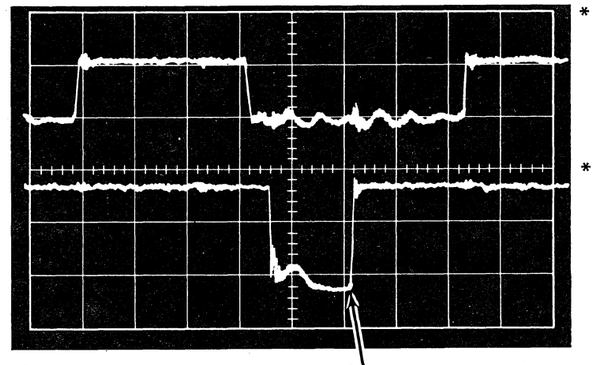
Lower level determined by -30Vdc setting

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4J2J13 (8K-16K BSM)
Signal Name: Read Time

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J2G05 (8K-16K BSM)
Signal Name: X Rd Current Source Resistor

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



*Ground

Lower level determined by -30Vdc setting

BSM Waveforms C

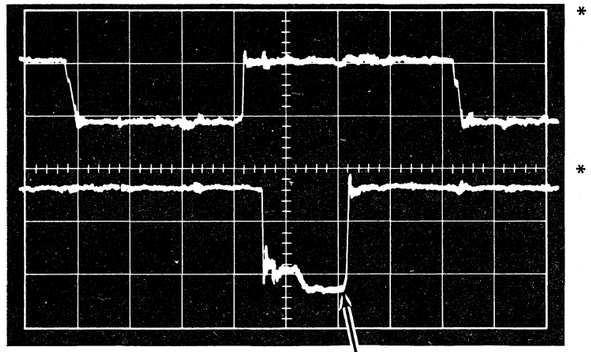
Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4J2J13 (8K-16K BSM)
Signal Name: Read Time

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J2J10 (8K-16K BSM)
Signal Name: X Write Current Source Resistor

BR0658A

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

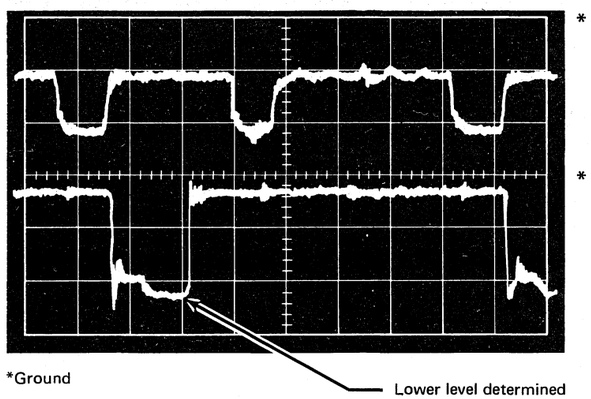


Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4J2B03 (8K-16K BSM)
Signal Name: Write Time

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J2J10 (8K-16K BSM)
Signal Name: X Write Current Source Resistor

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



*Ground

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

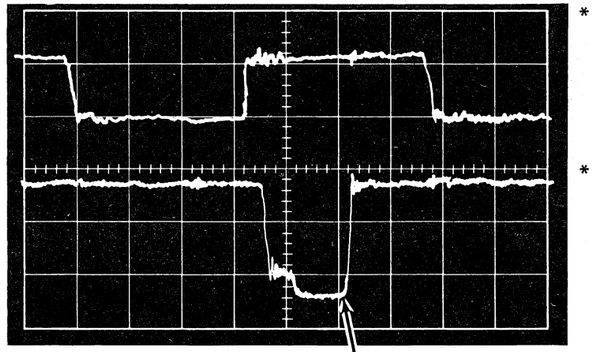
Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4A2B02 (8K-16K BSM)
Signal Name: Rd Call Wr Call

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J2D05 (8K-16K BSM)
Signal Name: Y Read Current Source Resistor

BSM Waveforms D

BR0659A

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

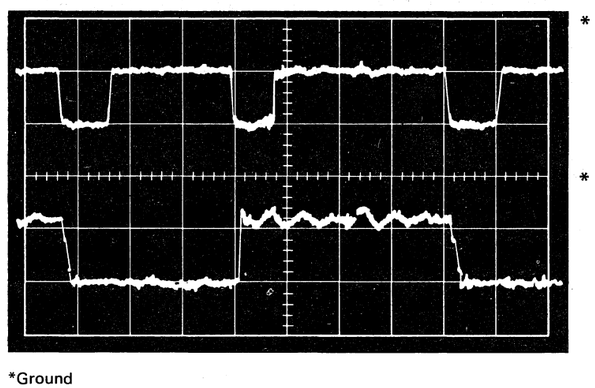


Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4J2B03 (8K-16K BSM)
Signal Name: Write Time

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J2D07 (8K-16K BSM)
Signal Name: Y Write Current Source Resistor

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



*Ground

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

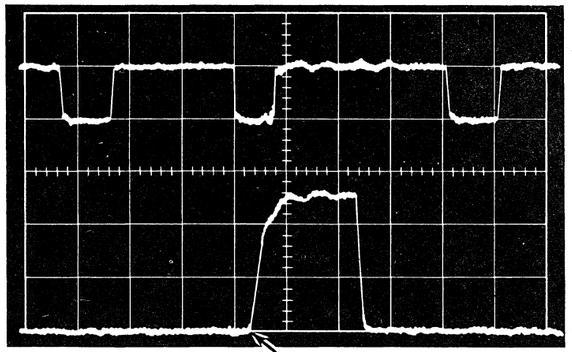
Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4A2B02 (8K-16K BSM)
Signal Name: Rd Call Wr Call

Channel 2
Vertical Gain: 1 V/cm
Signal Pin: B4J2B03 (8K-16K BSM)
Signal Name: Write Time

BSM Waveforms E

BR0660A

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



Sync: Plus External
Time Base: 200ns/cm

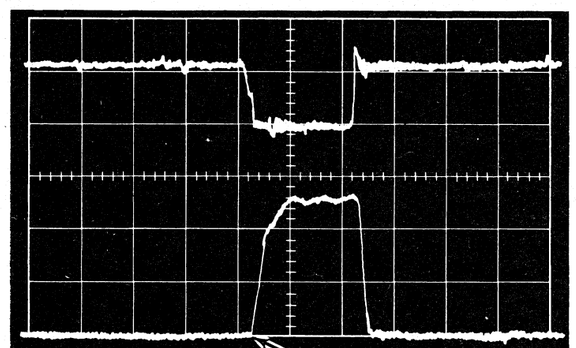
Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4A2B02 (8K-16K BSM)
Signal Name: Rd Call Wr Call

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J4G10 (8K-16K BSM)
Signal Name: Z Load Bit 0

Lower level determined by -30Vdc setting

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4J4J04 } 8K-16K BSM
Signal Name: Inhibit Byte 1

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4J4G10 (8K-16K BSM)
Signal Name: Z Load Bit 0

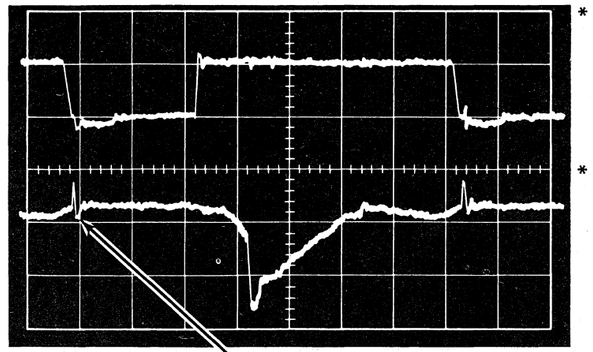
*Ground

Lower level determined by -30Vdc setting

BSM Waveforms F

BR0661A

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



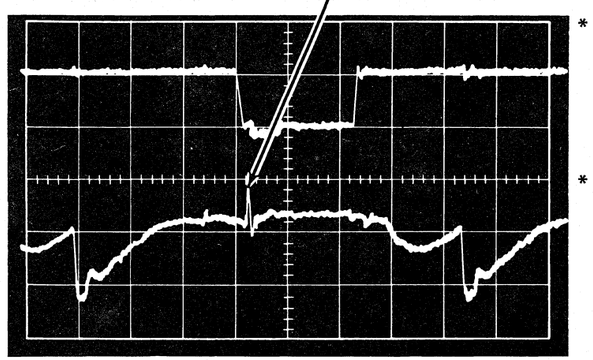
Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4B2B03 (8K-16K BSM)
Signal Name: Rd Control

Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4B2D10 (8K-16K BSM)
Signal Name: X Rd Lo Gate Ctrl

X Rd or Y Wr Lo Gate Ctrl signal is shown for reference only. This is a current waveform and can be a different level at similar test points in a BSM, and can be a different level at the same test point and different BSMs.

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4B2B04 (8K-16K BSM)
Signal Name: Wr Ctrl

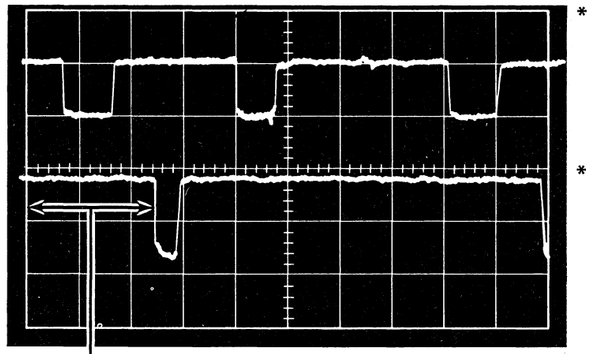
Channel 2
Vertical Gain: 10 V/cm
Signal Pin: B4B2D06 (8K-16K BSM)
Signal Name: X Wr Lo Gate Ctrl

*Ground

BSM Waveforms G

BR1756

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On



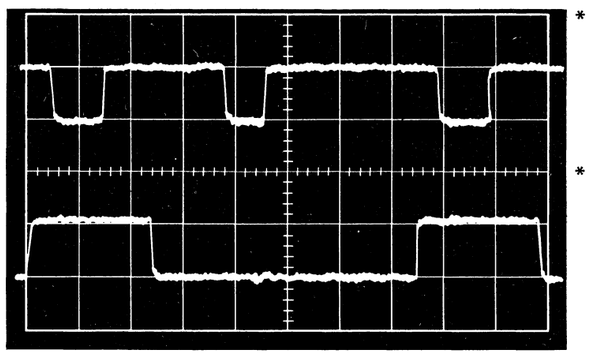
This time is determined by the BSM strobe card adjustment

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4A2B02 (8K-16K BSM)
Signal Name: Rd Call Wr Call

Channel 2
Vertical Gain: 5 V/cm
Signal Pin: B4B5D10 (8K-16K BSM)
Signal Name: Strobe Bits 0-8

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'FF'
Storage Test	Run
Address Increment	On



Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

Channel 1
Vertical Gain: 1 V/cm
Signal Pin: B4A2B02 (8K-16K BSM)
Signal Name: Rd Call Wr Call

Channel 2
Vertical Gain: 1 V/cm
Signal Pin: B4J4B05 (8K-16K BSM)
Signal Name: Sense Bit 0

*Ground

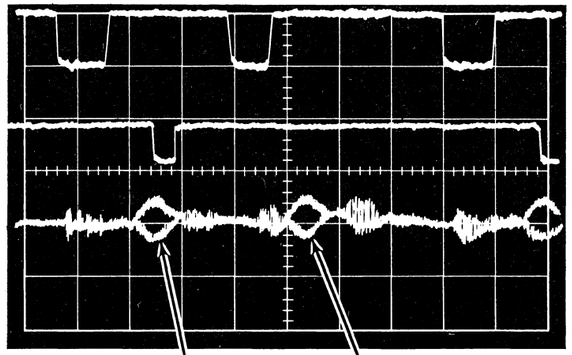
BSM Waveforms H

BR1757

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'FF'
Storage Test	Run
Address Increment	On

This is a 'three exposure' picture. 'Rd Call Wr Call', and 'Strobe' are shown only for time reference points.

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset



Rd Call Wr Call B4A2B02
1 V/cm (8K-16K BSM)

Strobe Bits 0-8 B4J4B07 (8K-16K BSM)
10 V/cm

* Core output writing '1' in all bit positions.

Cores being changed from '0' to '1' at write time. Any one address can be positive or negative.

Cores being changed from '1' to '0' at read time. Any one address can be positive or negative.

Note: Core output measured with Tektronix® 453 scope as follows:
Channel 1 and 2 set for 100 Mv/cm
'Mode' switch set to 'Add'
Channel 2 'Invert' switch set to 'Add'
Channel 1 signal pin – B4J4B02 (8K-16K BSM)
Channel 2 signal pin – B4J4D02 (8K-16K BSM)

*Ground

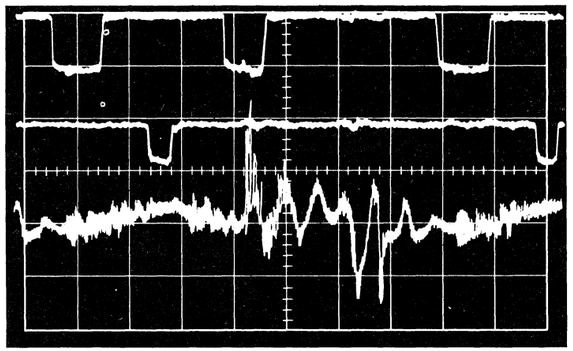
BSM Waveforms

BR1758

These are 'Three' exposure pictures. 'Rd Call Wr Call' and 'Strobe' are included for horizontal references.

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'00'
Storage Test	Run
Address Increment	On

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset



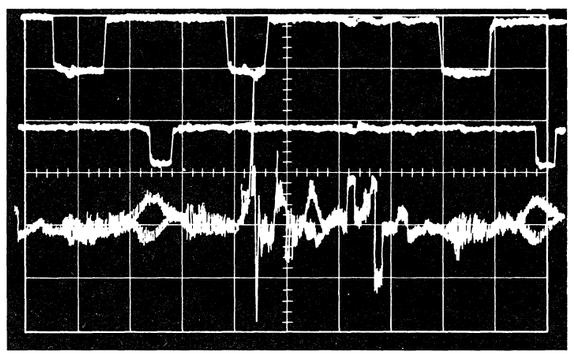
Rd Call Wr Call B4A2B02
1 V/cm (8K-16K BSM)

Strobe Bits 0-8 B4J4B07 (8K-16K BSM)

* Core output writing '0' in all bit positions. See Note on waveform located on right hand side of page 1-408B.

Switch Name	Setting
CE Mode Selector	Alter Storage
Data	'80'
Storage Test	Run
Address Increment	On

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset



Rd Call Wr Call B4A2B02 (8K-16K BSM)
1 V/cm

Strobe Bits 0-8 B4J4B07 (8K-16K BSM)
10 V/cm

* Core output writing '1' in this bit position and '0' in all other bit positions. See Note on waveform located on right hand side of page 1-408B.

*Ground

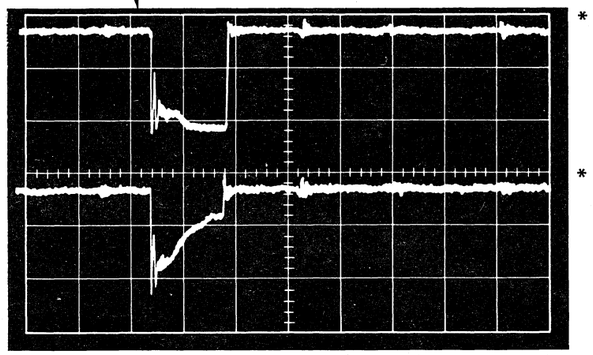
BSM Waveforms

BR1759

Switch Name	Setting
CE Mode Selector	Alter Storage
Storage Test	Run
Address Increment	Off

Sync: Plus External
Time Base: 200ns/cm
Sync Pin: B4A1D11
Signal Name: Reset

This is a composite picture which shows a good drive line, and an open drive line (broken weld in array).

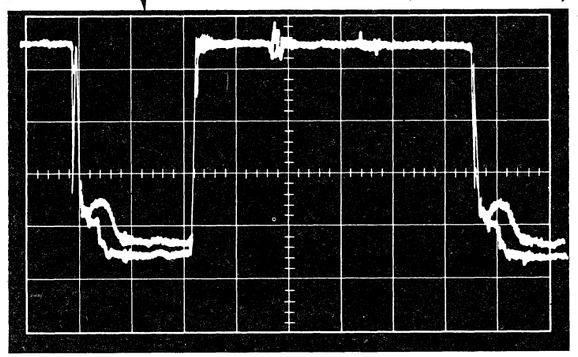


* Good drive line measured at
10 V/cm
B4J2D05 (8K-16K BSM)
'Y Read Current Source Resistor'

* Open drive line measured at
10 V/cm
B4J2D05 (8K-16K BSM)
'Y Read Current Source Resistor'

This is a double exposure picture. The highest down level shows a good drive line. The lowest down level shows 2 drive lines shorted together.

Note: These points are in series with the current source transformer primary therefore indirectly shows the failure.



* 5 V/cm
B4J2D05 (8K-16K BSM)
'Y Read Current Source Resistor'

*Ground

BSM Waveforms

BR1760

4.4 KEYBOARD

For maintenance information on the basic keyboard, refer to the Field Engineering Theory-Maintenance Manual, *Elastic Diaphragm Encoded Keyboards,* Order No. SY27-0073.

Refer to the figure at the right for the location of components to be removed.

4.4.1 Keyboard Removal

1. Remove power from the system.
2. Pull forward the top left hand side of the console panel (over the command lights). Remove the switch cover on the right hand side of the console by pulling it straight forward.
3. Loosen, but do not remove (1) the screw above and to the left of the lamp test switch, (2) the screw at the top right corner of the switch mounting plate.
4. Remove the two screws that mount the keyboard to the console pan. These screws are located under the front of the table top of the machine.
5. Remove the console cover by pulling it straight up and towards you.
6. Remove the two screws (one on each side) of the console panel.
7. Pivot the console panel back out of the way.
8. Remove the four nuts (one on each corner) of the keyboard mounting bracket.
9. Disconnect the signal cable located on the left hand side and under the encode board.
10. Remove the yellow wire from the lower contact of the inquiry request switch.
11. Disconnect the plug connector. It may be necessary to lift the keyboard up and to the right to gain access to this plug.
12. Lift the keyboard up and out of the machine.

4.4.2 Keyboard Replacement

Note: Check that all leaf springs are in their proper position relative to their respective key lever.

1. Perform the above steps in the reverse order.
2. Check that there are no binds between the console cover and the keyboard. If there are, loosen the four nuts that mount the keyboard and reposition the keyboard until there are no binds between the keys and the console cover.

4.4.3 Console Lamps

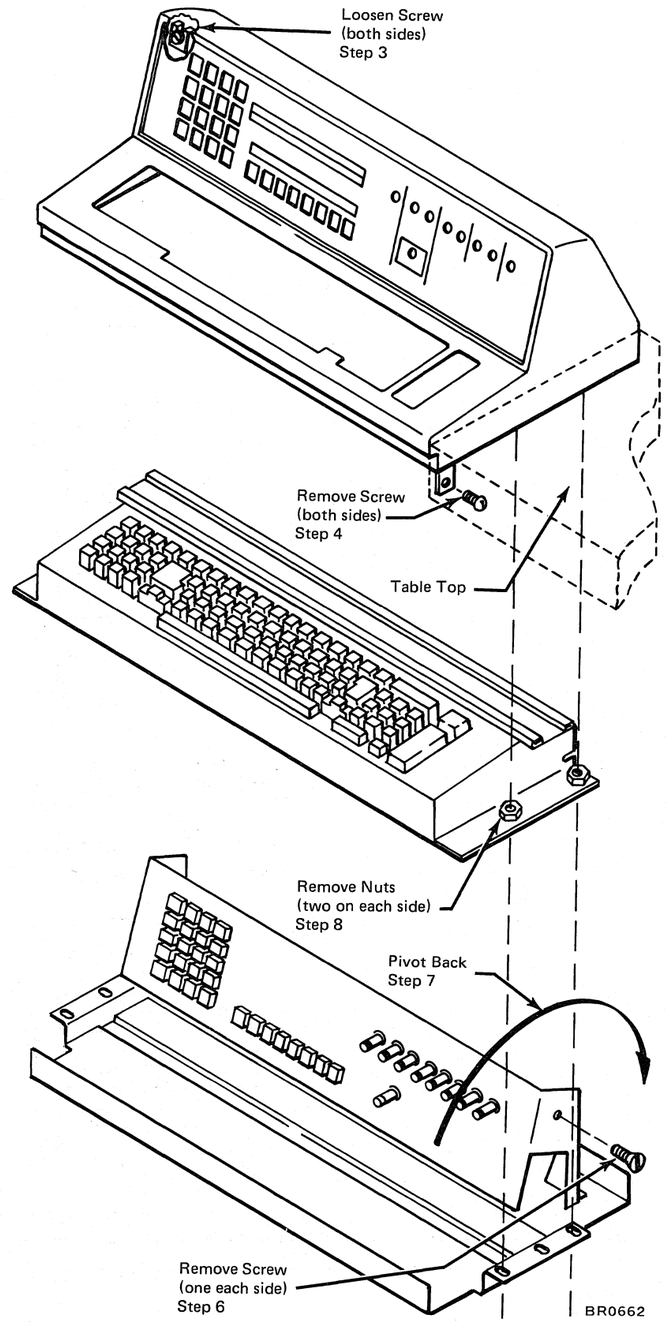
Test the console indicator lamps with the CE lamp test switch.

4.4.3.1 Lamp Removal

1. Pull the console panel forward to expose the lamps.
2. Remove the faulty lamp by pulling it forward out of the panel.
3. Insert a new lamp in its place by pushing it backwards into the socket.

4.4.4 Keyboard Encode Board

Troubleshooting procedures for the keyboard encode board can be found in the system automated logics on pages PK030 and PK031. Information on these pages includes keyboard voltages, bail magnet voltages, and test points for weighted codes.



4.5 SINGLE SHOTS

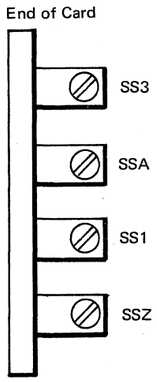
All single shot adjustment procedures are covered in the MAP charts. They should be adjusted to the time durations called out in the MAP charts or the ALDs. The description of single shots on this page should be used to locate the single shot on the board and in the ALDs.

4.5.1 Use Meter Single Shot

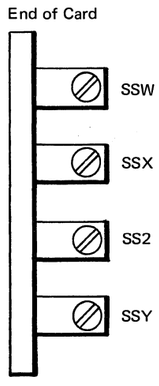
The use meter single shot is located on gate A, board B1, card S4 (A-B1S4). Refer to ALD page CR101 for the duration of the pulse.

4.5.2 Printer Attachment Single Shots

The illustration below shows the location of the printer attachment single shots.



Gate A, Board A2, Card Q2 (A-A2Q2)
ALD Pages PR111 and PR112



Gate A, Board A2, Card Q3 (A-A2Q3) ALD Pages PR121 and PR122

Single shot 1A (pin feed carriage) is located on Gate A, Board A2, Card U2 (A-A2U2), ALD Page PR123.

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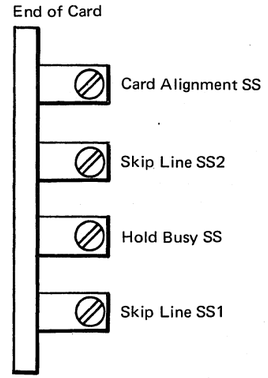
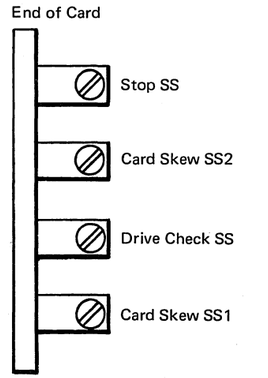
4.5.3 Ledger Card Device Attachment Single Shots

The illustration below shows the location of the ledger card device attachment single shots.



Gate A, Board A2, Card D4 (A-A2D4)
ALD Pages PR711 and PR712



Gate A, Board A2, Card D5 (A-A2D5)
ALD Pages PR721 and PR722

BR0664

4.6 DISK DRIVE

Note: If system power is off, the file drawers may be opened by inserting a small screwdriver in an opening in the right hand file side cover and lifting the interposer. The drawer may then be opened in a normal manner.

4.6.1 Disk Drive Service Position

To move the file to its rear service position, follow the steps below:

1. Open the file drawer and loosen four front cover mounting screws (A) and remove front cover. Remove the two lower screws (A) from the slide base.
2. Remove the cover at the rear of the file enclosure.

   Note: If the lower file drawer is to be moved to the rear service position, remove bracket (B).
3. The file slide mounting base may now be pushed to its rear service position.

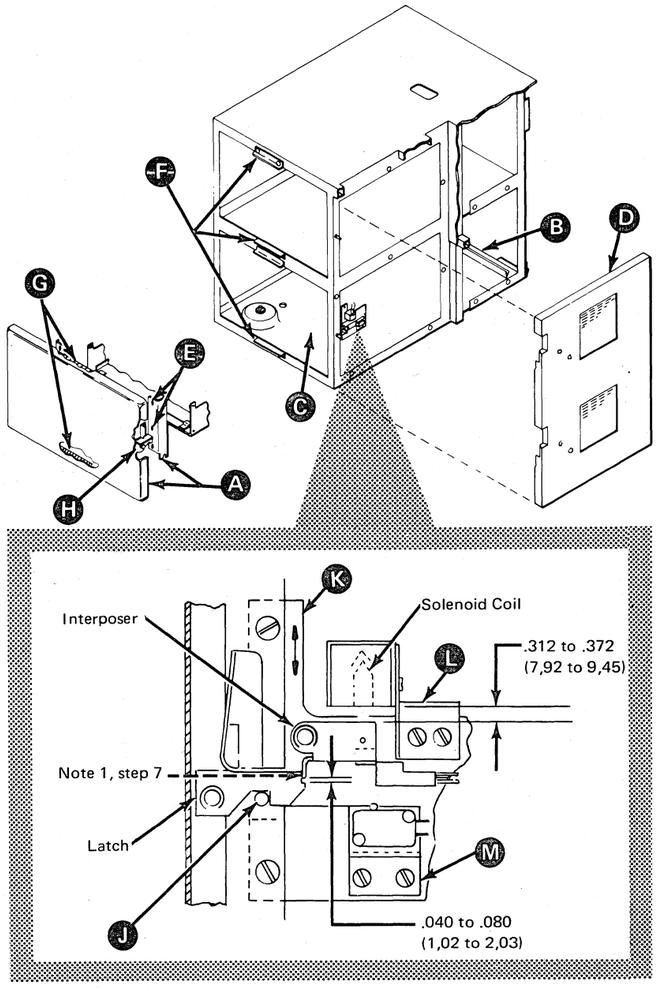
4.6.2 File Drawer Interlock Adjustment

1. Move the upper and lower drawer (if installed) to the rear service position.

   Note: If a second 5444 is not installed, remove the lower front cover (C). Two screws hold the lower cover in place and these screws are accessible when the top slide base is moved to the rear service position.
2. Remove the right hand side cover (D). The 8 screws that hold the side cover in place are accessible when the drawers are moved to the rear service position.

   Note: Adjustments in items 3 and 4 need not be made unless the front covers are out of alignment.
3. Reinstall the drawer front covers and adjust vertically with screws (E) so that the top edge of the upper cover is 1/4 inch below and parallel with the lower surface of the table top.
   a. If a second 5444 is installed, (lower drawer) adjust the lower front cover so that the bottom edge is flush with the lower edge of the system frame with screws (E).
   b. If a second file is not installed, adjust the lower front cover (C) as in adjustment 3a.
4. Adjust the EMC blades (F) (top and bottom for each drawer) so the blade enters the center of the finger stock (G) located in the cover.
5. Adjust the drawer latch retaining nut (H) so the latch is horizontal in its rest position. (This is a preliminary adjustment.)
6. The latch stud (J) is adjusted to hold the drawer securely closed and still allow the drawer latch to release and latch easily.

   Note. The adjustment made in step 5 should not keep the drawer latch from resting on the latch stud (J) when the drawer is closed. Re-adjust the drawer latch retaining nut, if necessary, to meet this requirement.

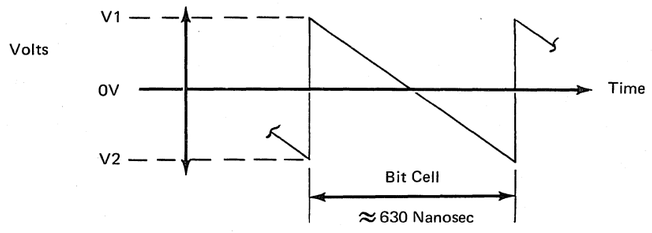


BR0665A

7. Move the interlock mounting bracket (K) vertically so interposer to latch (interlock surfaces) clearance is .040 to .080 inches. The drawer latch must be holding against the latch stud (in a closed position), and the interposer should be butted against the drawer latch as shown in note 1 in the figure.
8. Adjust the solenoid bracket (L) so that the solenoid coil is from .312 to .372 inches above the interposer when the interposer is at rest. The bottom surface of the solenoid coil must remain parallel to the top edge of the interposer during this adjustment.
9. Adjust the switch bracket (M) to close the switch contacts when the drawer is closed. The switch contacts should not transfer when the .060 to .080 inch travel of the latch is moved up toward the interposer. After this adjustment is made, insure that the switch actuator does not raise above the top surface of latch stud (J) when the drawer is open. This is to prevent damage to the switch actuator, by the drawer latch, when the drawer is closed.
10. The solenoid should attract the interposer to its released position when the system power is turned on and the disk drive power is off. The interposer should freely drop to prevent the drawer from being opened when the system power is turned off.

4.6.3 Data Separator Adjustment

1. Remove card in location A-A1J2 to select 'read gate spin 0' and 'read gate' for data separator A card.
2. Disable '+spin 0 read data' and '+spin 1 read data' inputs to data separator A, with jumpers to −4 volts (D4G13 to D4B06) and (D4J13 to D4G06).
3. Disable 'ratio circuit 2' output on data separator A with jumper to logic ground (D4B07 to D4D08).
4. Jumper '3.177 MHz oscillator output' signal on oscillator card (D3D07) into data separator A card (D4G03).
5. Observe 'ramp' waveform on data separator B output (E4G02).
6. Adjust potentiometer on data separator B card (A-A1E4) until 'ramp' waveform is swinging equally about logic ground with a ±100 millivolt tolerance (i.e., V1 should equal V2 within ±100 mV).



BR0666

4.7 DATA RECORDER FE LATCH

A spare latch in the data recorder is used as a FE latch to aid in trouble-shooting (with the MAP charts or for general troubleshooting). This latch is used when the data recorder is located away from the central processing unit and it is impossible to view the CE probe when operating the console.

The following procedures apply to questions asked by the MAP charts for the data recorder.

4.7.1 "Pulse on Line?"

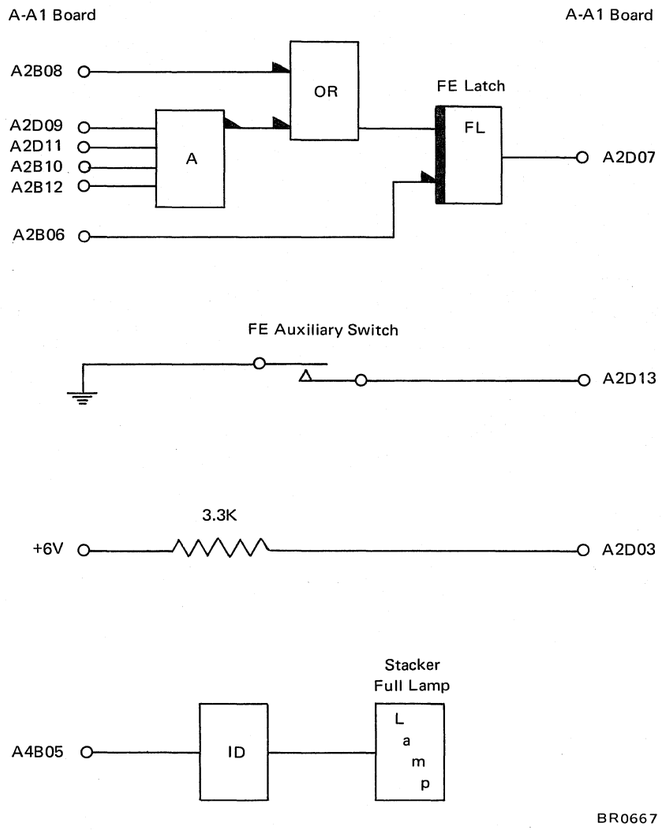
1. Check point to be monitored with CE probe. If point is up, jumper it to A-A1A2B08. Jumper A-A1A2D09 to ground. If point is down, jumper it to A-A1A2D09.
2. Momentarily apply a minus SLD pulse or ground to A-A1A2B06 to reset the FE latch.
3. Jumper A-A1A2D07 to the CE probe input. Rerun the program.
4. If a pulse occurs, A-A1A2D07 is plus and the probe red light or up light is on.

4.7.2 "Level Change Down?"

1. Jumper A-A1A2D09 to ground to negate the 4-way AND block.
2. Momentarily apply a minus SLD pulse or ground to A-A1A2B06 to reset the FE latch.
3. Jumper A-A1A2B08 to the point to be monitored.
4. Jumper A-A1A2D07 to the CE probe input. Rerun the program.
5. If the level changes down, A-A1A2D07 is plus and the probe red light or up light is on.

4.7.3 "Level Change Plus?"

1. Check point to be monitored with CE probe directly to see if already minus or down (it should be in this state to check for plus change).
2. Jumper point to be monitored to A-A1A2D09.
3. Momentarily apply a minus SLD pulse or ground to A-A1A2B06 to reset the FE latch.
4. Jumper A-A1A2D07 to CE probe input. Rerun the program.
5. If the level changes plus, A-A1A2D07 is plus and the probe red light or up light is on.



Chapter 5. Power and Cooling

DANGER

Unless CB1 is turned off, power is available at K1 and K2 input terminals and at transformer (T3) terminals. The 24 volt control voltage is also not turned off.

Replacements of power supply components generally follows the replacement philosophy of the system; that is, replacement is limited to voltage regulator cards, fuses, and relays. However, in some cases it will be necessary to replace the series regulator and the filter capacitors.

5.1 INPUT POWER REQUIREMENTS

The input power requirements for the System/3 Model 6 are:

1. 60 Hertz—200, 208, and 230 Vac 3 phase at 30 amps
2. 50 Hertz—200, 220, 235, 380, and 408 Vac 3 phase at 30 amps

5.2 POWER SUPPLY OUTPUTS

The power supply outputs and the location of each supply are shown below. The primary use of each of the supplies is also given. The using system supplies −30V, +6V, and −4V to the BSM. An internal BSM +3V and V sense (−14V) is generated from the +6V and the −30V respectively. The −30V is a temperature compensated drive voltage.

In power sequencing, the −30V is the last up and the first down, with respect to the −4V and +6V.

Power Supply	Location	Primary Use
-4 Vdc at 70 amps	CPU	Logic Voltage
+6 Vdc at 12 amps	CPU	Logic Voltage
-30 Vdc at 9.5 amps	CPU	Storage Supply
+24 Vdc at 25 amps	CPU	I/O Units
+24 Vdc	CPU	Control Voltage for Power Sequencing
-12 Vdc	CPU	BSCA (medium speed only)
-4 Vdc at 32 amps	CPU	B gate only (used in non-printed circuit board sequence panel machines only)
-4 Vdc at 32 amps	CPU	B gate only (used in printed circuit board sequence panel machines only)

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5.2.1 Checks and Adjustments

All voltage measurements should be made in a normal environment (temperature between 68 degrees and 86 degrees Fahrenheit) with a Weston 901 meter or its equivalent.

The +3V supply may be adjusted by connecting meter leads to C4J03 (minus) and C4G11 (plus). Then adjust potentiometer on the upper half of card C4 (board B3 for up to 16K storage). The +3V is set by referencing it to the +6V (meter reading will be 3V).

The 14V supply may be adjusted by using the lower potentiometer on the same card (C4). Connect meter leads to C4J11 (minus) and C4D08 (plus) and adjust for 14 ± 0.05 volts.

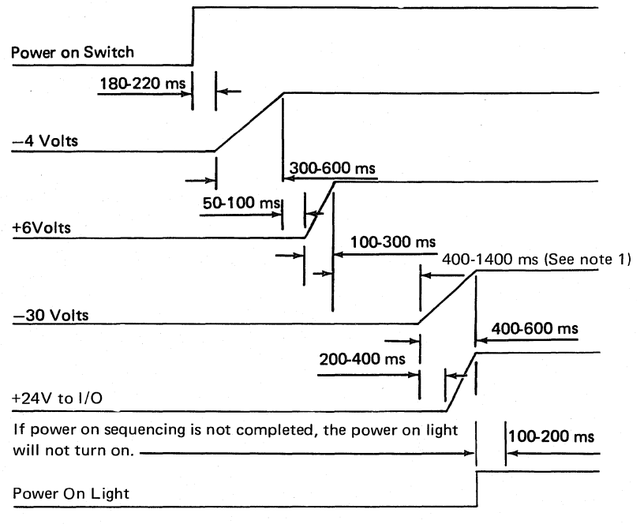
See 5.5 and 5.6 for the adjustment of the −4V and +6V supplies. See 4.3.4 for the adjustment of the −30V supply.

5.3 POWER SEQUENCING

Power sequencing is controlled by the 24 Vdc control voltage. The power supplies come on in the following order:

1. −4V logic voltage
2. +6 Vdc logic voltage
3. −30 Vdc storage supply
4. +24 Vdc supply

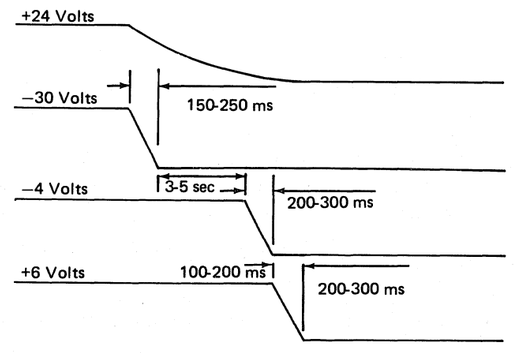
Power On Sequence



Note: +24 Volt control voltage is on whenever the main line switch is on.
Note 1: For machines with printed circuit board sequence panel, the delay of −30V is approximately 500 ms.

BR0669A

Power Off Sequence



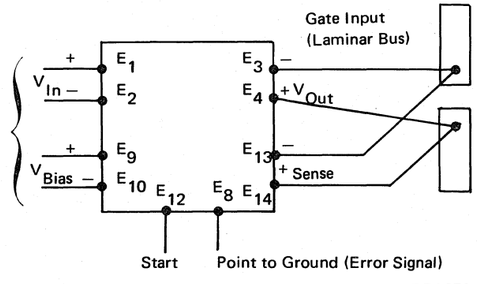
Note: +24 volt control voltage is on whenever main line switch is on.

BR0670A

5.4 MST REGULATORS

The monolithic solid technology (MST) regulator trips when the system experiences an overcurrent condition (approximately 15% above the set current) or an overvoltage condition (4.7 volts). When this regulator trips, the system powers down and thus is protected from high currents and voltages. Refer to the figure below for a graphic representation of the MST regulator. Also note the following:

1. E12 must be tied to the up (most positive) level.
2. E8 goes to ground when the regulator trips (overcurrent or overvoltage condition).
3. E8 of the −30 Vdc regulator goes to ground when the output of the +6 Vdc regulator is lower than 5.28V.



BR0671

5.5 ADJUSTMENT OF THE –4 VOLT POWER SUPPLY

5.5.1 Overcurrent Adjustment

1. Connect the meter across the 4 volt load between E2 (–4V) and E4 (ground) on regulator.
2. Adjust the voltage adjustment potentiometer (shown below) to –4.6V. Do not go beyond this. Set the overcurrent regulator to trip. If you cannot reach –4.6V before the regulator trips, turn the overcurrent adjustment clockwise until you can reach –4.6V before it trips.
3. When the overcurrent adjustment trips, the machine will power down.
4. Turn the voltage adjustment back down and power up the machine.
5. Adjust the voltage adjustment potentiometer as given in 5.5.2.

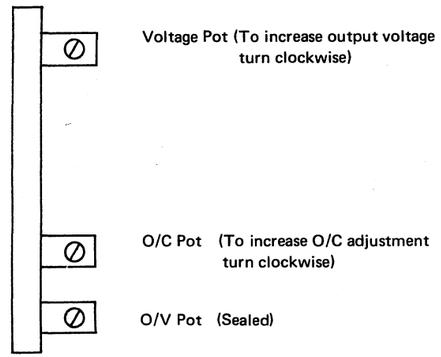
5.5.2 Voltage Adjustment

1. Connect meter between E2 (–4V) and E4 (ground) on regulator.
2. Adjust voltage for –4.15V.
3. Connect meter across A-B1C2B06 (–4V) and A-B1C2D08 (ground). This voltage should fall between –3.85 volts and –4.15 volts.
4. If voltage measured in step 3 is out of tolerance, readjust the –4 volt supply.

5.5.3 Overvoltage Adjustment

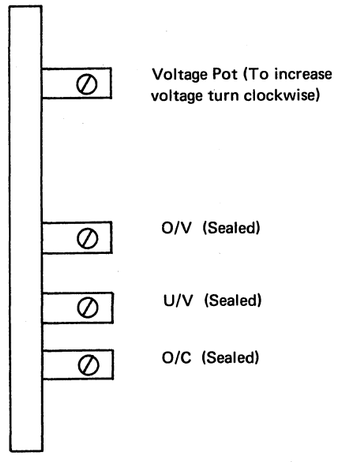
There is no field adjustment for overvoltage. It is set and sealed at the time of manufacture. Replace regulator card if overvoltage condition fails to trip regulator (5.4).

BR0672



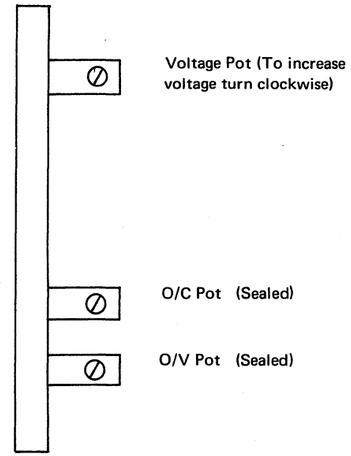
End View of 4 Volt Regulator Card

BR0673



End View of 30 Volt Regulator Card

BR0674



End View of 6 Volt Regulator Card

BR0675

5.6 ADJUSTMENT OF THE +6 VOLT POWER SUPPLY

5.6.1 Voltage Adjustment

1. Connect meter between E4 (+6 volt terminal) and E2 (ground terminal) on regulator.
2. Adjust voltage adjustment potentiometer (shown above) for +6.00 volts.

   Note: This adjustment has no plus or minus tolerance. Set as close to +6.00 volts as possible.

5.6.2 Overvoltage—Overcurrent Adjustment

There are no field adjustments for overcurrent or overvoltage in this power supply. They are set and sealed at the time of manufacture. Replace regulator card if overcurrent or overvoltage conditions fails to trip the regulator.

5.7 ADJUSTMENT OF THE –30 VOLT POWER SUPPLY

Refer to 4.3.4 for adjustment of the –30V power supply.

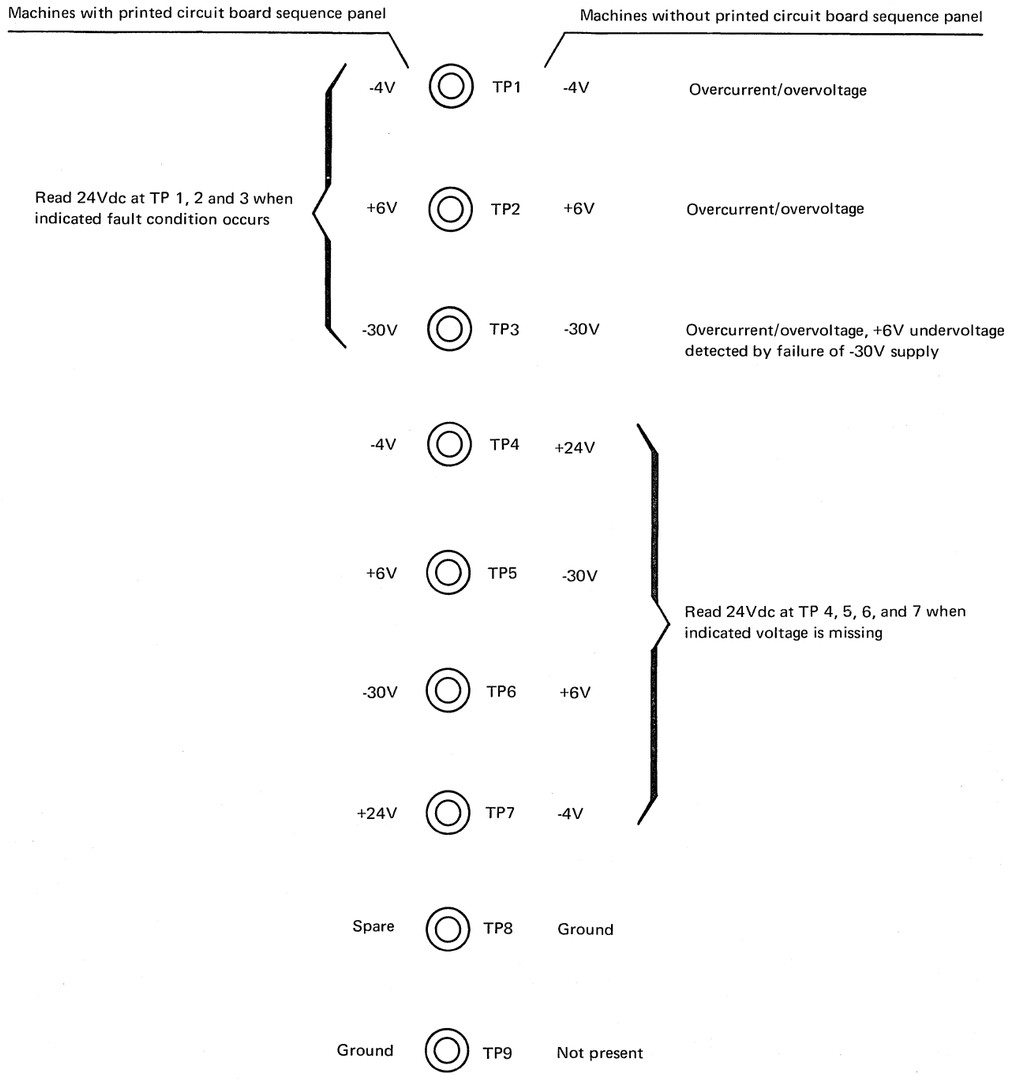
5.8 POWER SUPPLY TEST POINTS

Refer to the figure to the right for test points (TPs) for the power system.

The machine powers down in any of the conditions detected at TP1,2, or 3. Twenty-four volts is readable at TP1,2, or 3 until the system reset switch is pressed. Loss of either the -4V or +6V while the machine is running powers down the system and 24V is present at TP1 (loss of -4V) or TP2 (loss of +6V). Loss of -30V or +24V while the machine is running does not cause power down, but causes a power on reset that stops operation of the machine. Any regulator power fault condition (overvoltage/overcurrent) will drop system power.

FAULT	POWER ON/ OFF SWITCH	THERMAL INDICATOR	ACTION
Internal power supply malfunction	On	Off	1. Turn power switch to off 2. Correct problem 3. Press System Reset 4. Turn power on
Thermal condition	On	On	1. Turn power switch to off 2. Power on indicator is off 3. Thermal light stays on until condition is removed
Customer power source loss	On	On	1. Turn power switch to off 2. All indicators turn off 3. Turn power switch to on and continue operation

BR0676A



BR0677A

5.9 ISOLATION OF AC AND DC GROUND

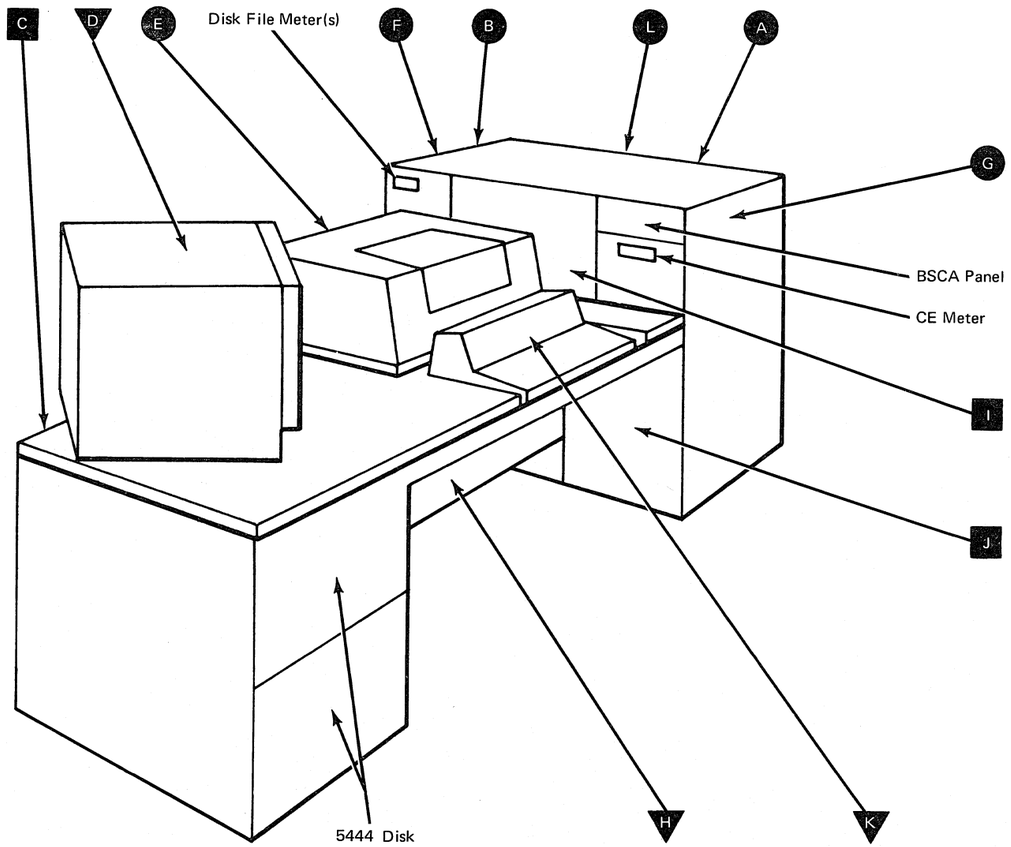
1. Disconnect the flexible aluminum power distribution system (FAPDS) and the black wire fastened to the top right hand side of the regulator stack.
2. Disconnect the black wire on position 8 of the frame ground lugs located on the right inner panel of the primary power box.
3. If a CRT is on the system, disconnect the dc cable to TB4 position 6 and 9, and the CRT flat yellow ribbon cable from the I/O disconnect. See page 1-605 for disconnect and TB4 locations.
4. If a data recorder is attached to the system, disconnect the shield wire from the interconnecting bulk signal cable. The shield is fastened to the bottom plate of the machine frame in the rear of the machine.
5. A short is indicated by zero ohms from any dc common point to the frame.

Chapter 6. Locations

The figure on this page shows the locations of the covers and access panels on the 5406.

Access Panel	
Area	Panel
Logic Gate A, CPU, Memory and Attachments	A
Logic Gate B, BSCA and SIOC	B
Rear access to disk mechanics and electrical units.	C
Access to CRT mechanics and electrical units.	D
Access to printer mechanics.	E
Power Supplies	F
CE Panel	G
Cables	H
Primary Power Box	I
Secondary Power Box	J
Keyboard mechanics and Encode Board.	K
Ferro's	L

BR0678

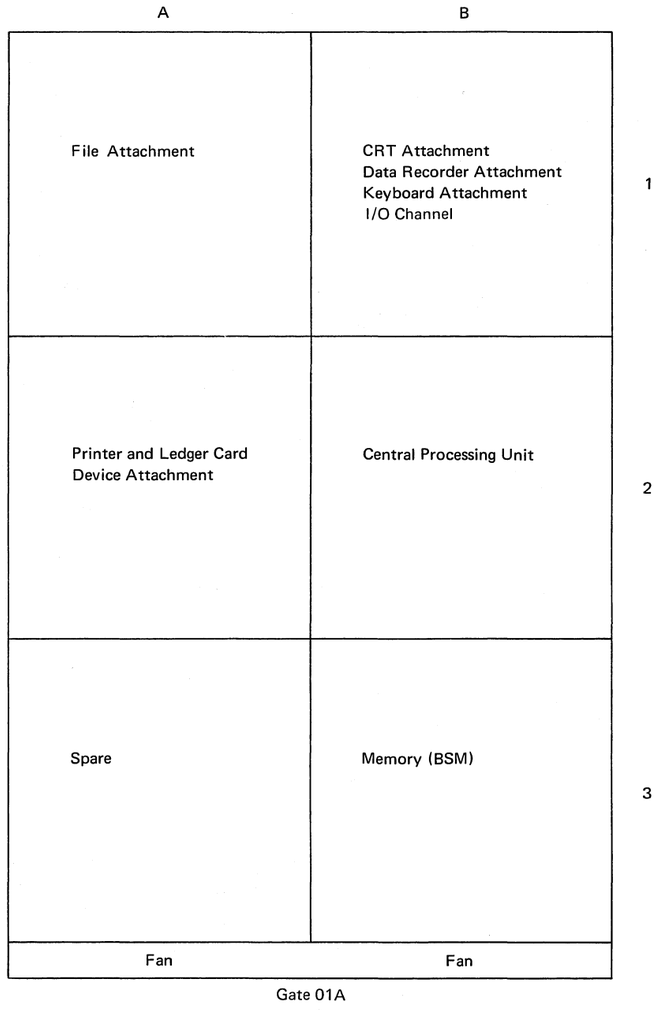


Hinged Panel

Panel with Fasteners

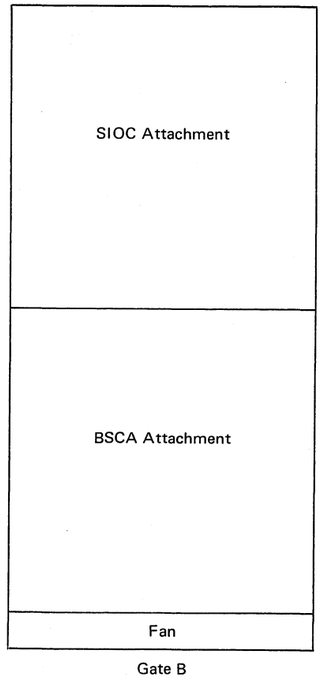
Panels which are not easily accessible, but must be removed for some service requirements.

BR0679



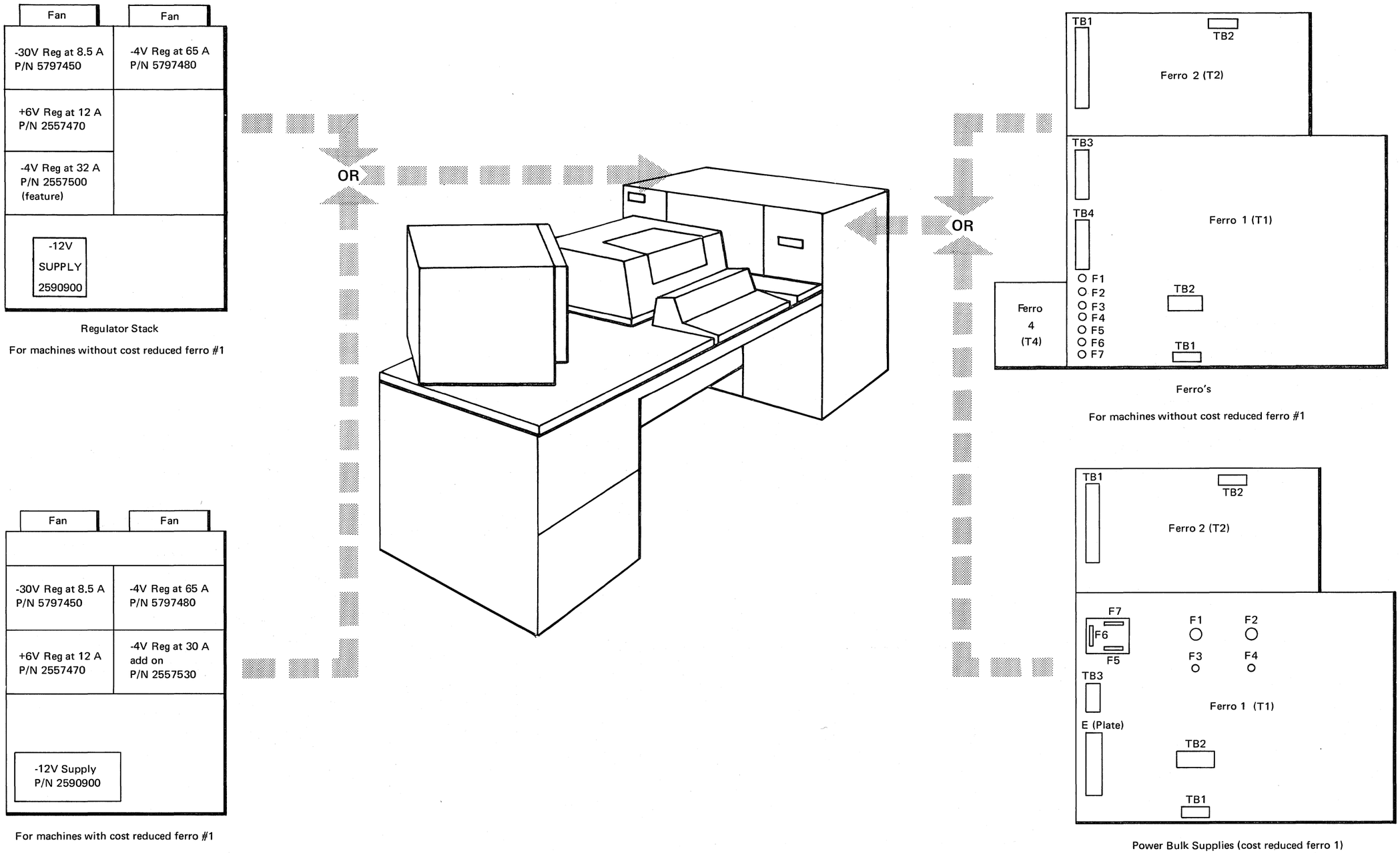
Gate 01A

BR0680A



Gate B

BR0681



Regulator Stack

For machines without cost reduced ferro #1

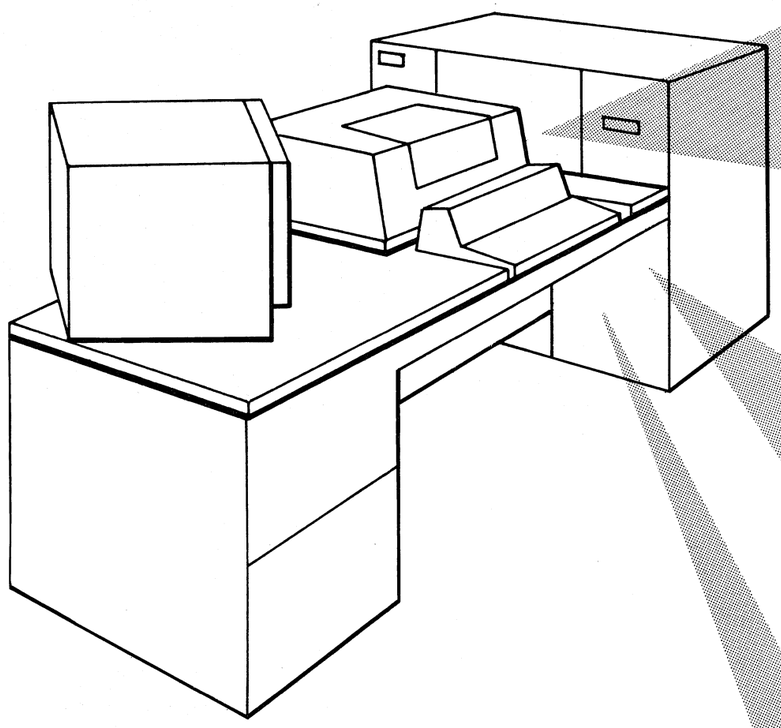
Ferro's

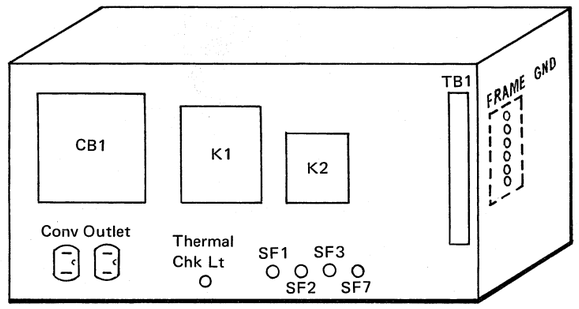
For machines without cost reduced ferro #1

For machines with cost reduced ferro #1

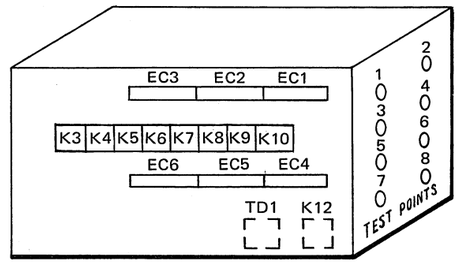
Power Bulk Supplies (cost reduced ferro 1)

BR0682A



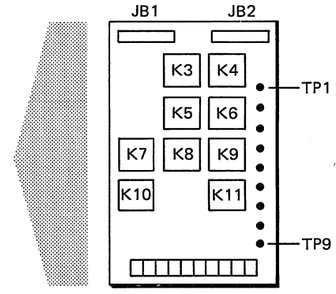


Primary Power Box - Front View
For machines with or without printed circuit board sequence panel

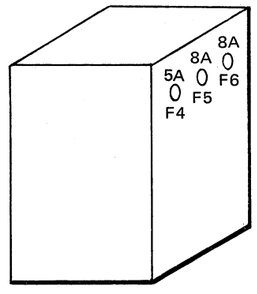


Secondary Power Box - Front View
For machine without printed circuit board sequence panel

OR

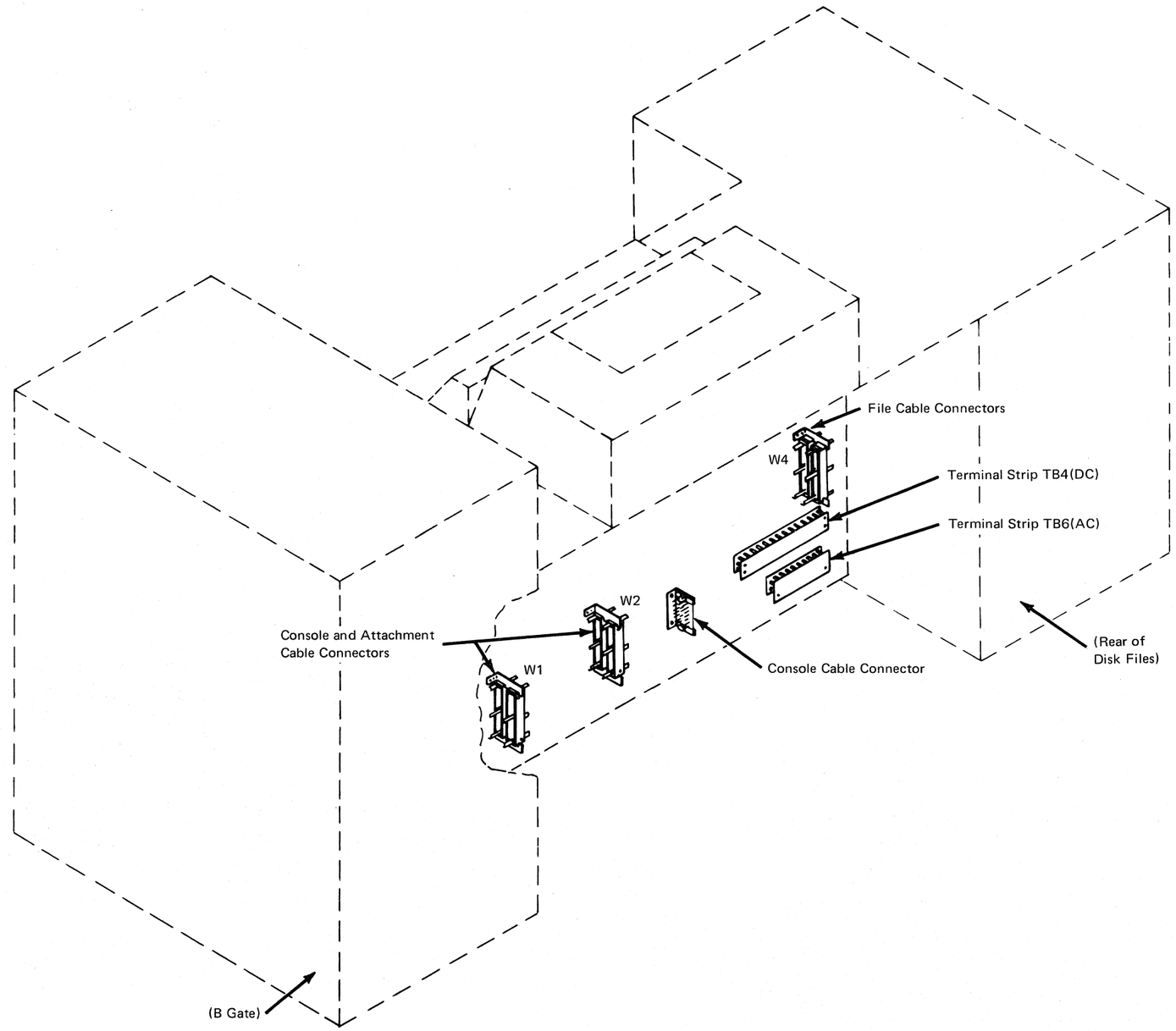


Printed Circuit Board Sequence Panel - Front View



+24V Control Asm (T3)
For machines with or without printed circuit board sequence panel

BR0683A



Power and Cable Channel

BR0613A

Appendix A. Special Circuits

There are no special circuits on the 5406 processing unit.

Appendix B. World Trade

The input power requirements for World Trade machines are as follows:

50 Hz – 380/408 V ac for Y input
220/235 V ac for △ input
200 V ac for Japan

60 Hz – 200 V ac for Japan

Sections 2 through 6. Processing Unit

These sections of the 5406 FETMM contain the maintenance diagrams for the processing unit. These diagrams are to be used with the Field Engineering Theory of Operations Manual (*IBM System/3 Model 6 5406 Processing Unit*, Order No. SY34-0023) to fully explain the operation of the processing unit.

The sections are:

Section 2. Error Conditions
Section 3. Data Flow
Section 4. Functional Units
Section 5. Operations
Section 6. Power and Cooling

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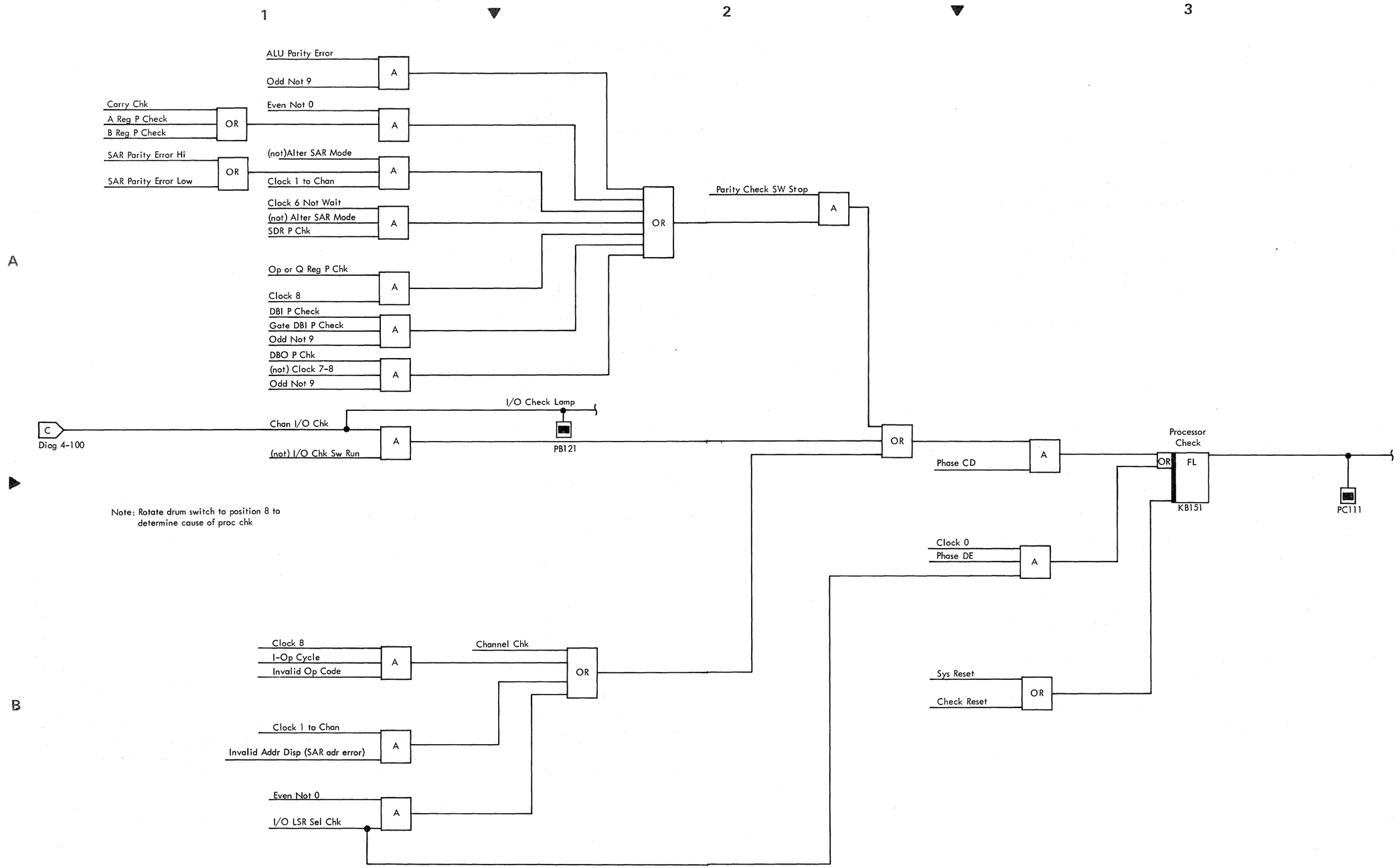
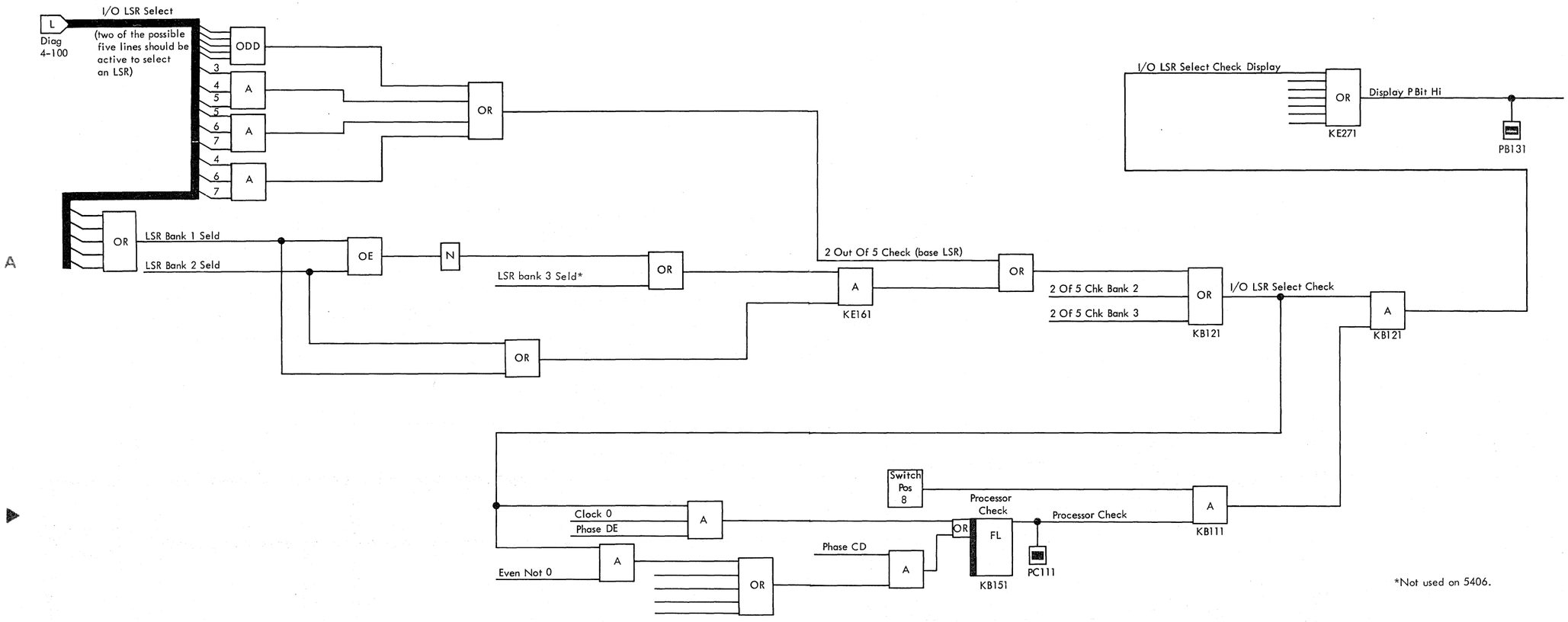
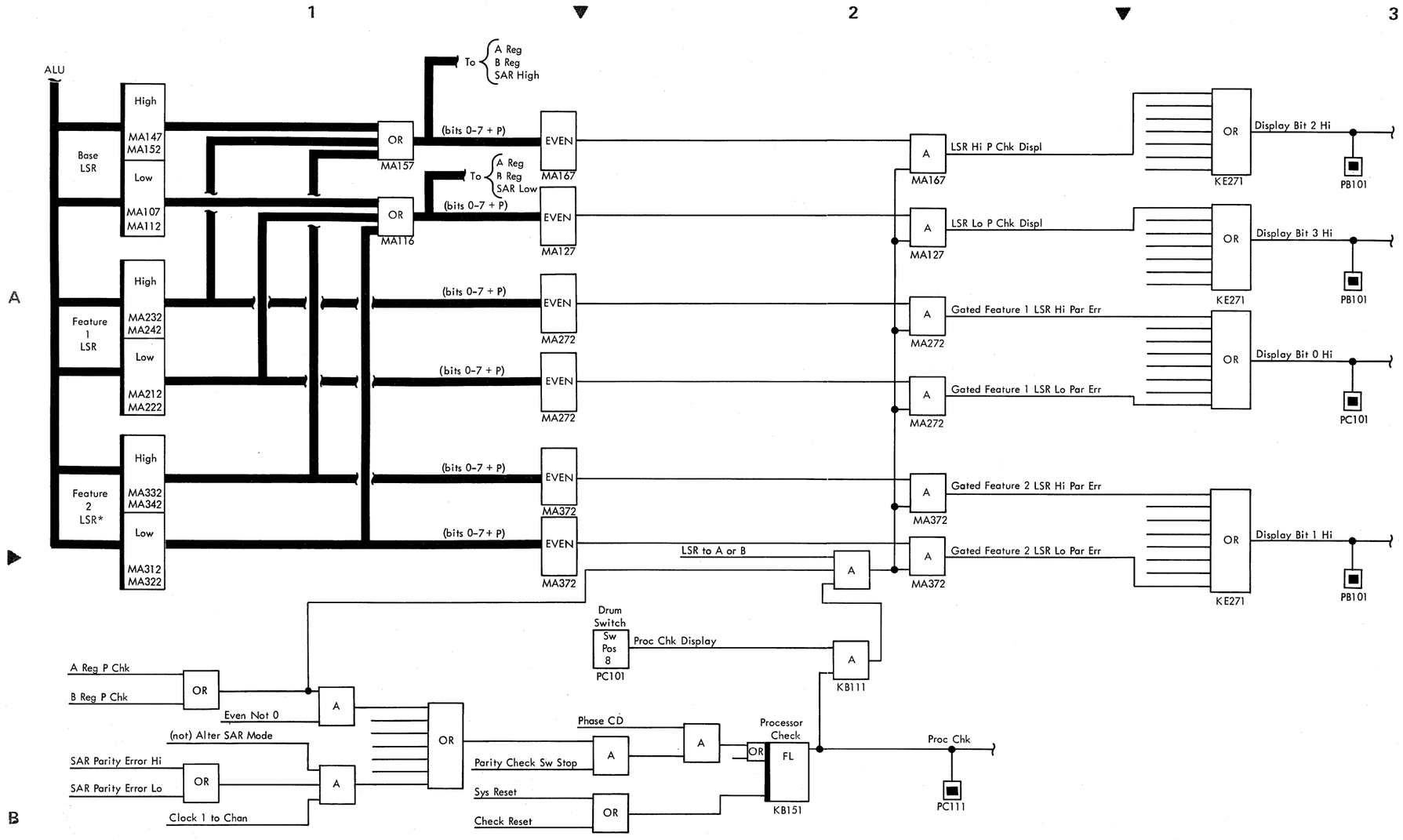
Power Sequencing (2 Parts) 6-010, 6-011


1
2
3
A
B
ALU Parity Error
Odd Not 9
Carry Chk
A Reg P Check
B Reg P Check
OR
Even Not 0
SAR Parity Error Hi
SAR Parity Error Low
(not)Alter SAR Mode
Clock 1 to Chan
Clock 6 Not Wait
(not) Alter SAR Mode
SDR P Chk
Op or Q Reg P Chk
Clock 8
DBI P Check
Gate DBI P Check
Odd Not 9
DBO P Chk
(not) Clock 7-8
Odd Not 9
A
OR
Parity Check SW Stop
I/O Check Lamp
C
Diag 4-100
Chan I/O Chk
(not) I/O Chk Sw Run
PB121
Phase CD
Processor Check
FL
KB151
PC111
Note: Rotate drum switch to position 8 to determine cause of proc chk
Clock 0
Phase DE
Sys Reset
Check Reset
Clock 8
I-Op Cycle
Invalid Op Code
Channel Chk
Clock 1 to Chan
Invalid Addr Disp (SAR adr error)
Even Not 0
I/O LSR Sel Chk



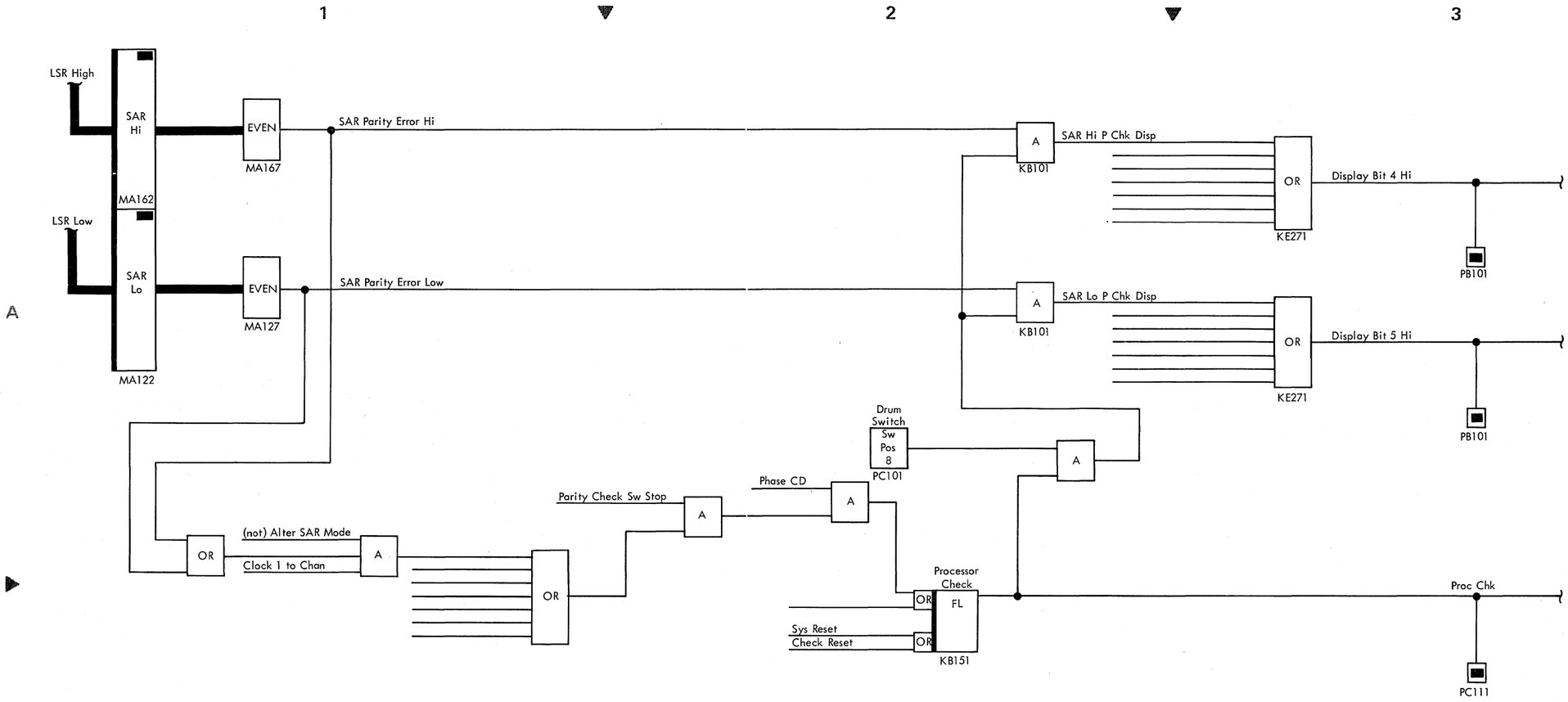
*Not used on 5406.



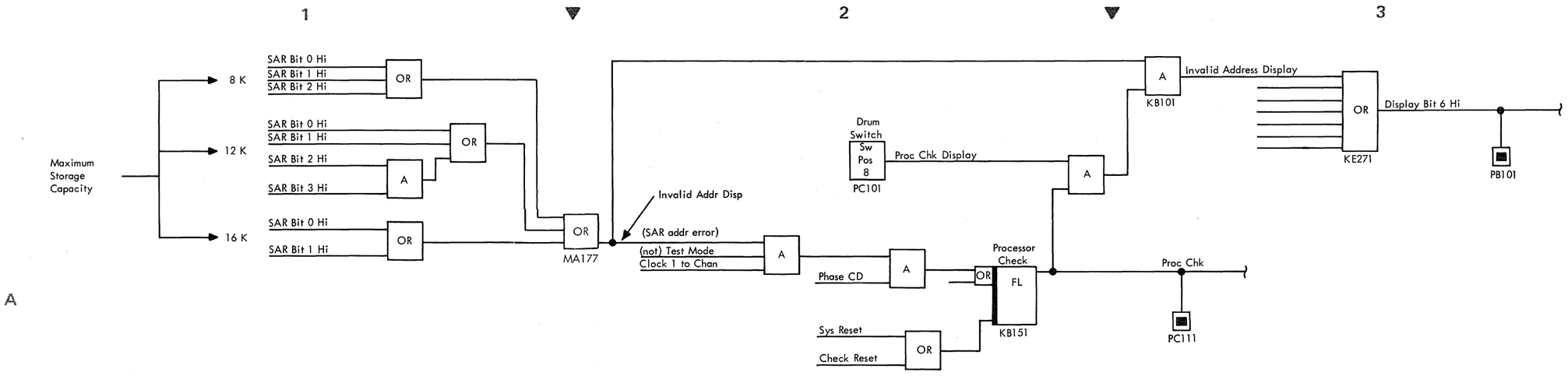
Error Location	Lighted Bits 0	1	2	3
Base LSR High			X	
Base LSR Low				X
Feat 1 LSR High	X		X	
Feat 1 LSR Low	X			X
Feat 2 LSR High		X	X	
Feat 2 LSR Low		X		X

Note: Machine is stopped by either A register, B register or SAR parity error. Drum switch position 1 displays SAR contents, 2 displays LSR contents, 4 displays B register contents, and 5 displays A register contents

*Not used on 5406.



Note: Rotate drum switch to position 1 to display SAR contents

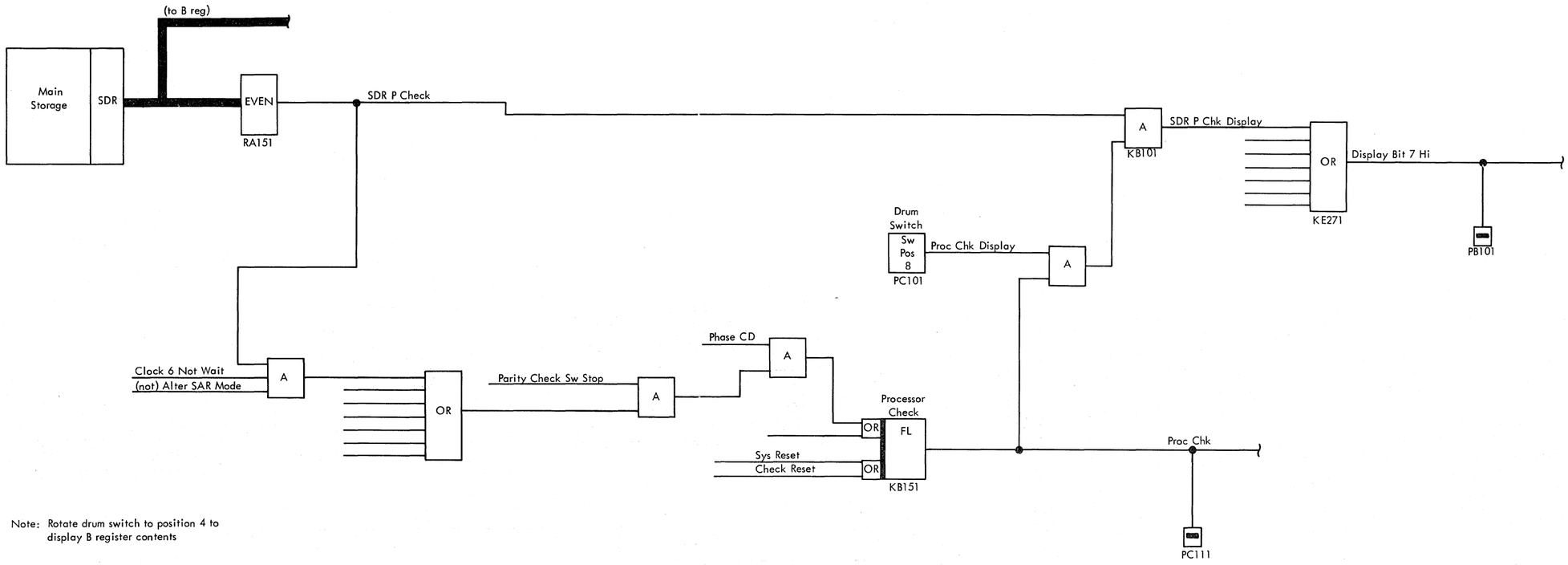


Note: Rotate drum switch to position 1 to display SAR contents

B

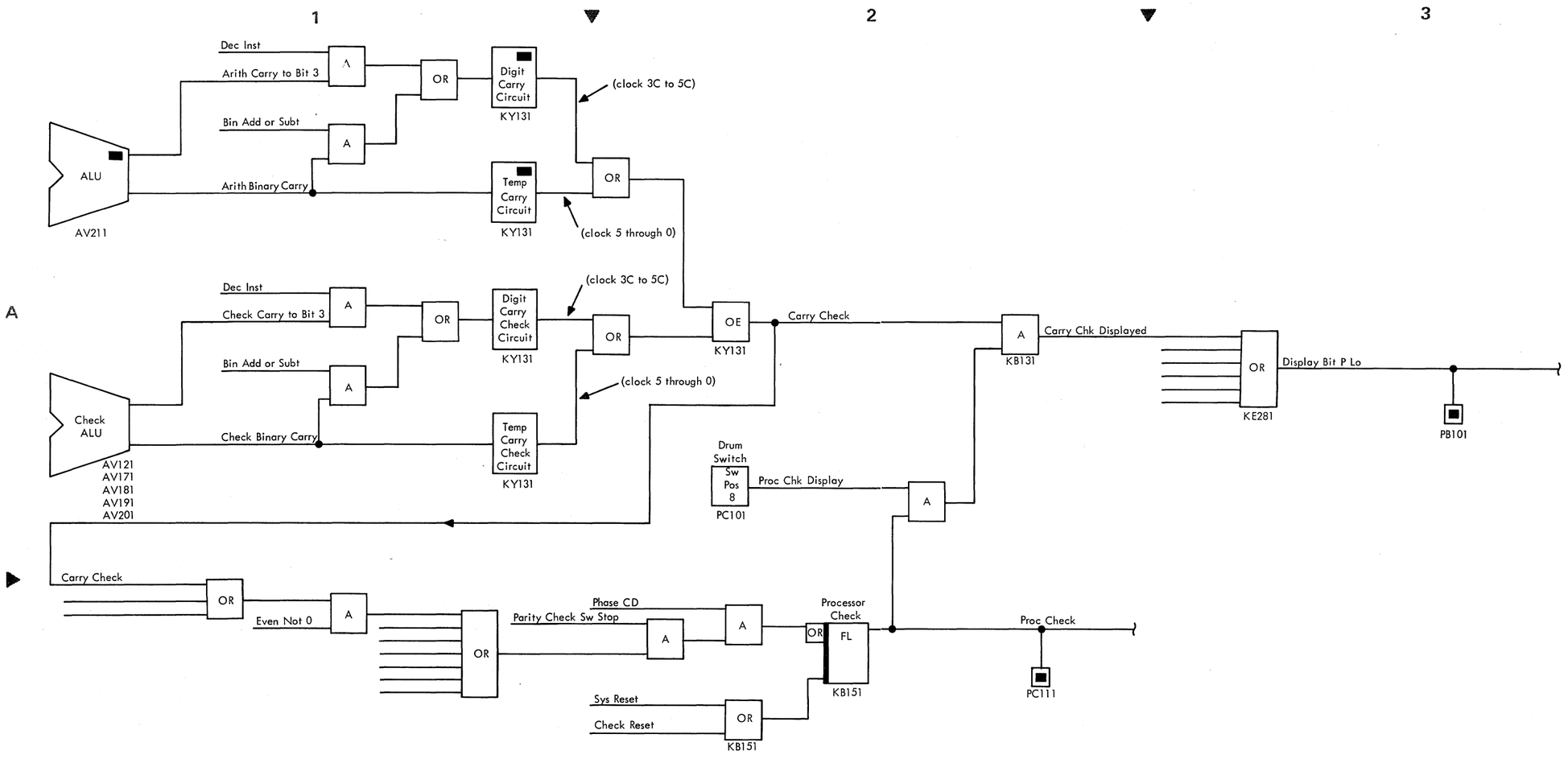
1 2 3

A

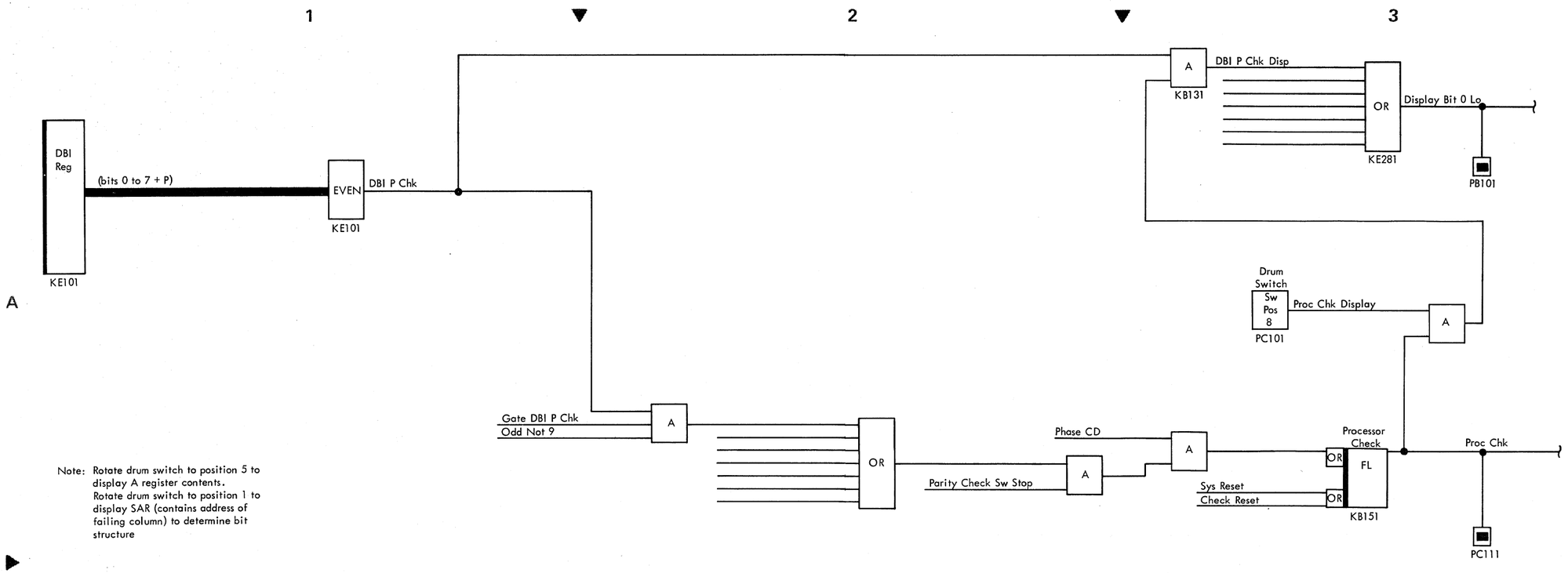


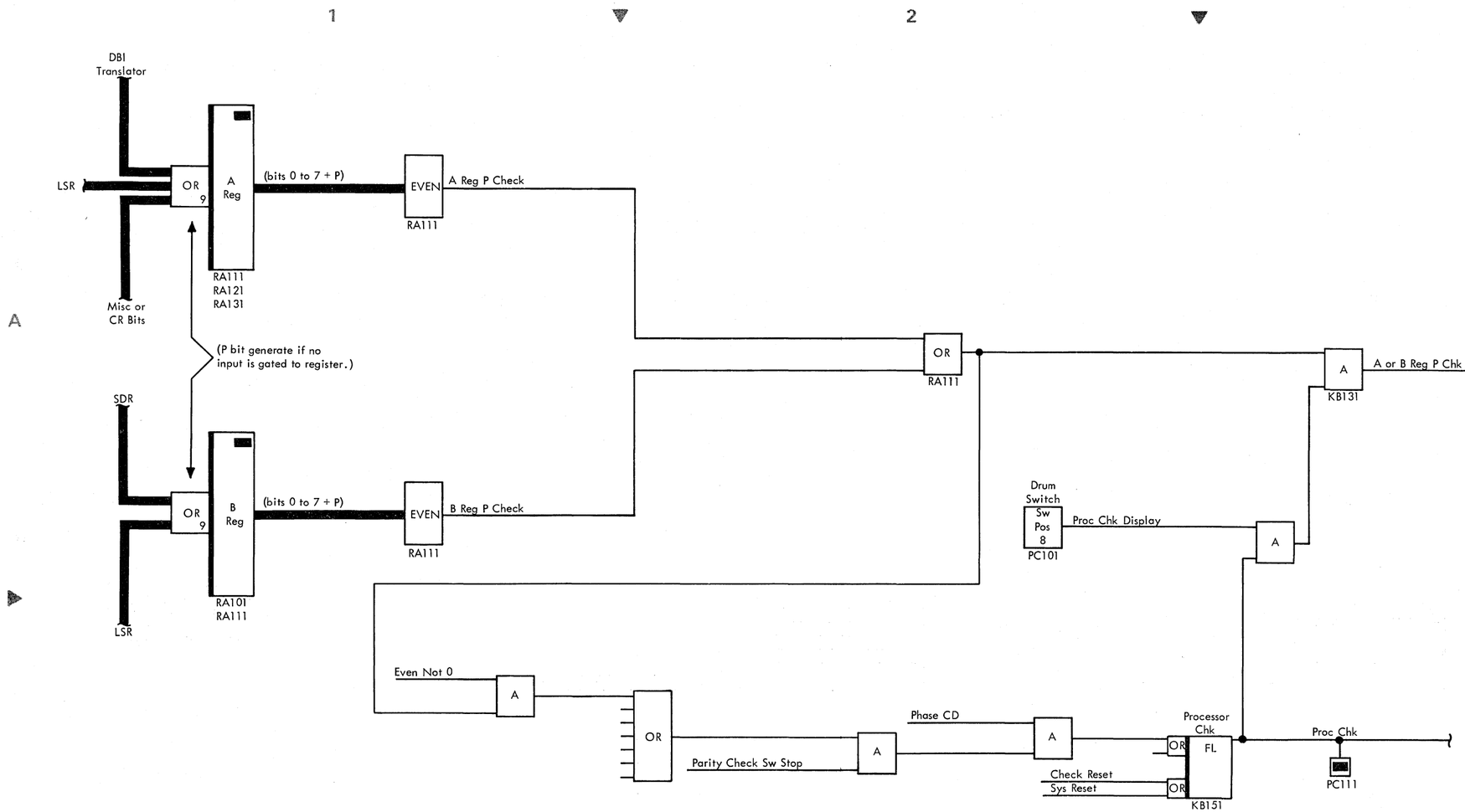
▶ Note: Rotate drum switch to position 4 to display B register contents

B

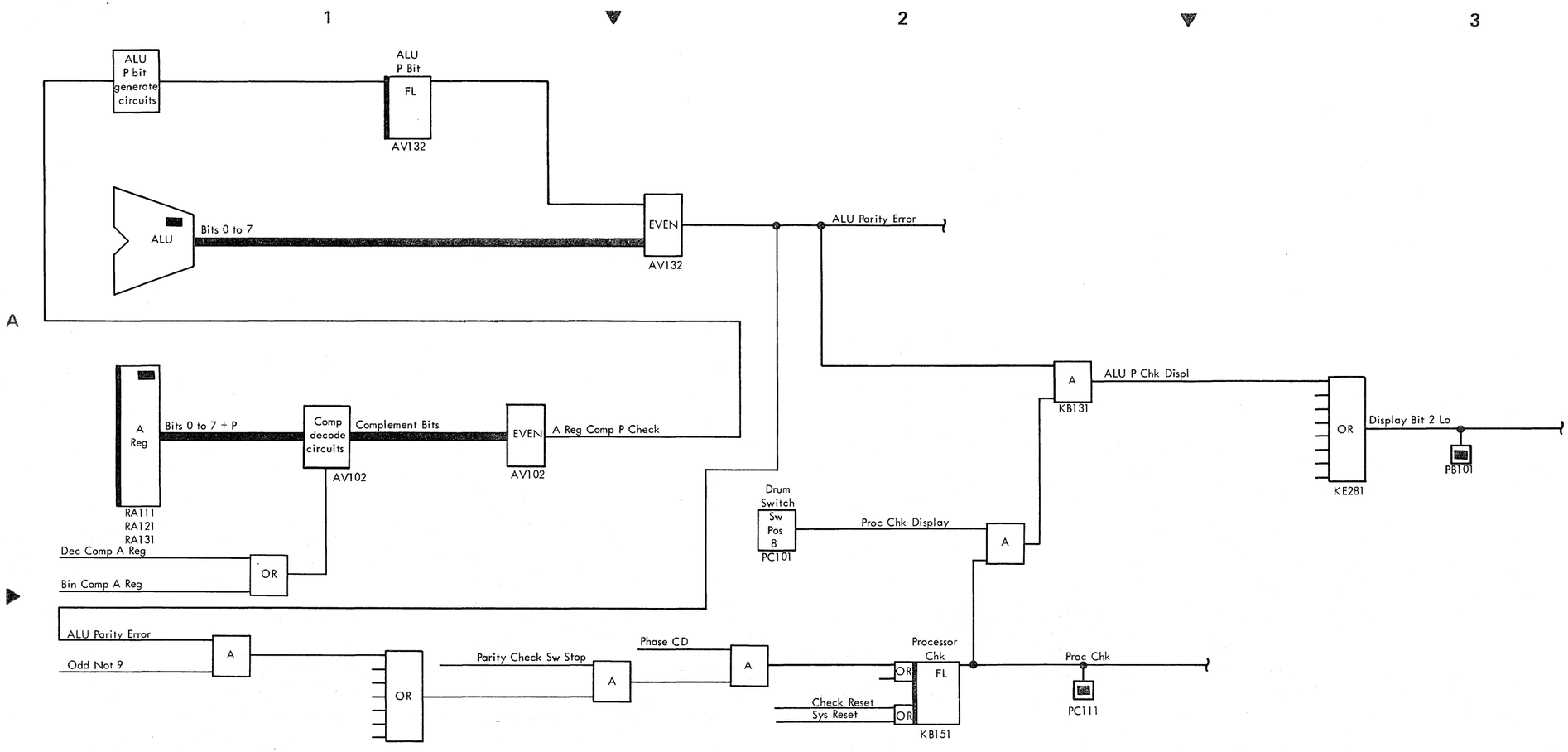


Note: Rotate drum switch to position 5 to display ALU output, position 4 to display ALU controls and carrys

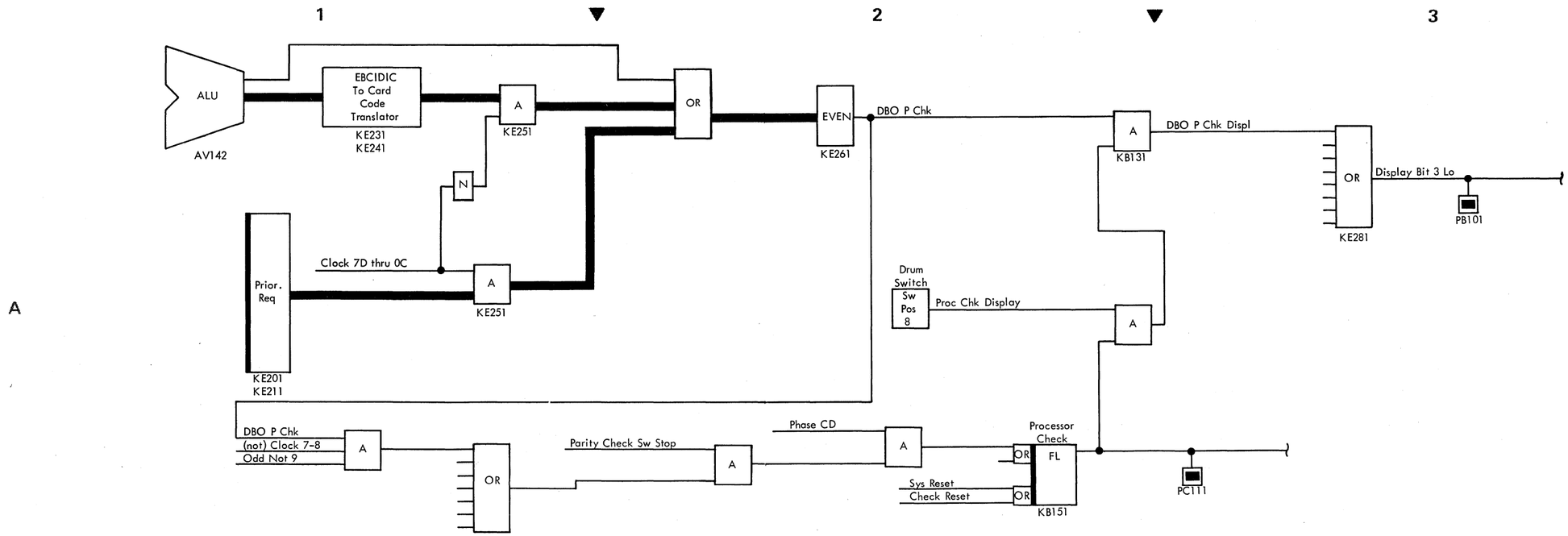

1
2
3
A
B
DBI Reg
(bits 0 to 7 + P)
KE101
EVEN
DBI P Chk
KE101
A
KB131
DBI P Chk Disp
OR
KE281
Display Bit 0 Lo
PB101
Drum Switch
Sw Pos 8
PC101
Proc Chk Display
A
Gate DBI P Chk
Odd Not 9
A
OR
Phase CD
A
Parity Check Sw Stop
A
Processor Check
OR
FL
Sys Reset
Check Reset
OR
KB151
Proc Chk
PC111
Note: Rotate drum switch to position 5 to display A register contents. Rotate drum switch to position 1 to display SAR (contains address of failing column) to determine bit structure



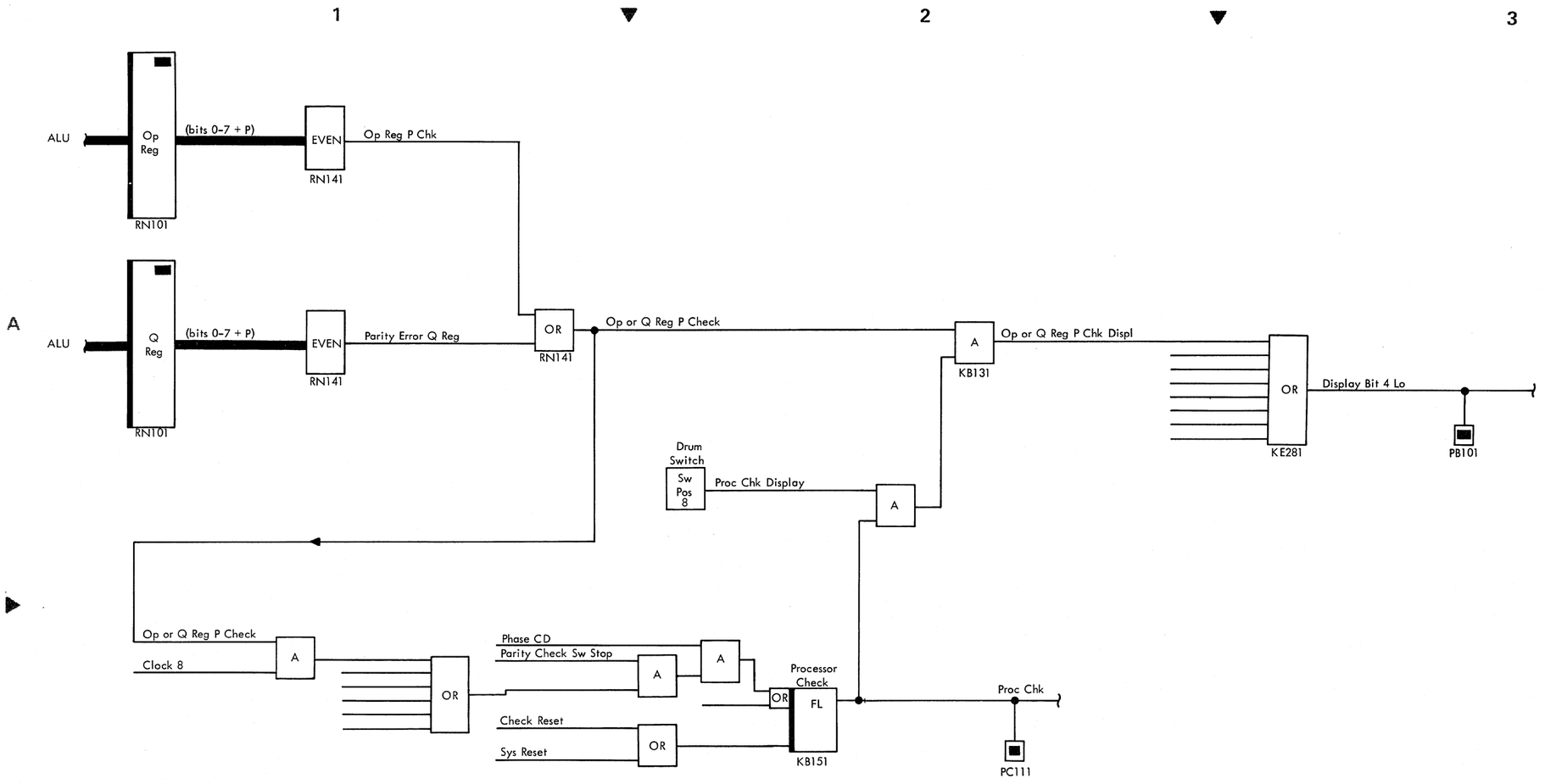
B Note: Rotate drum switch to position 5 to display A register contents, position 4 to display B register contents



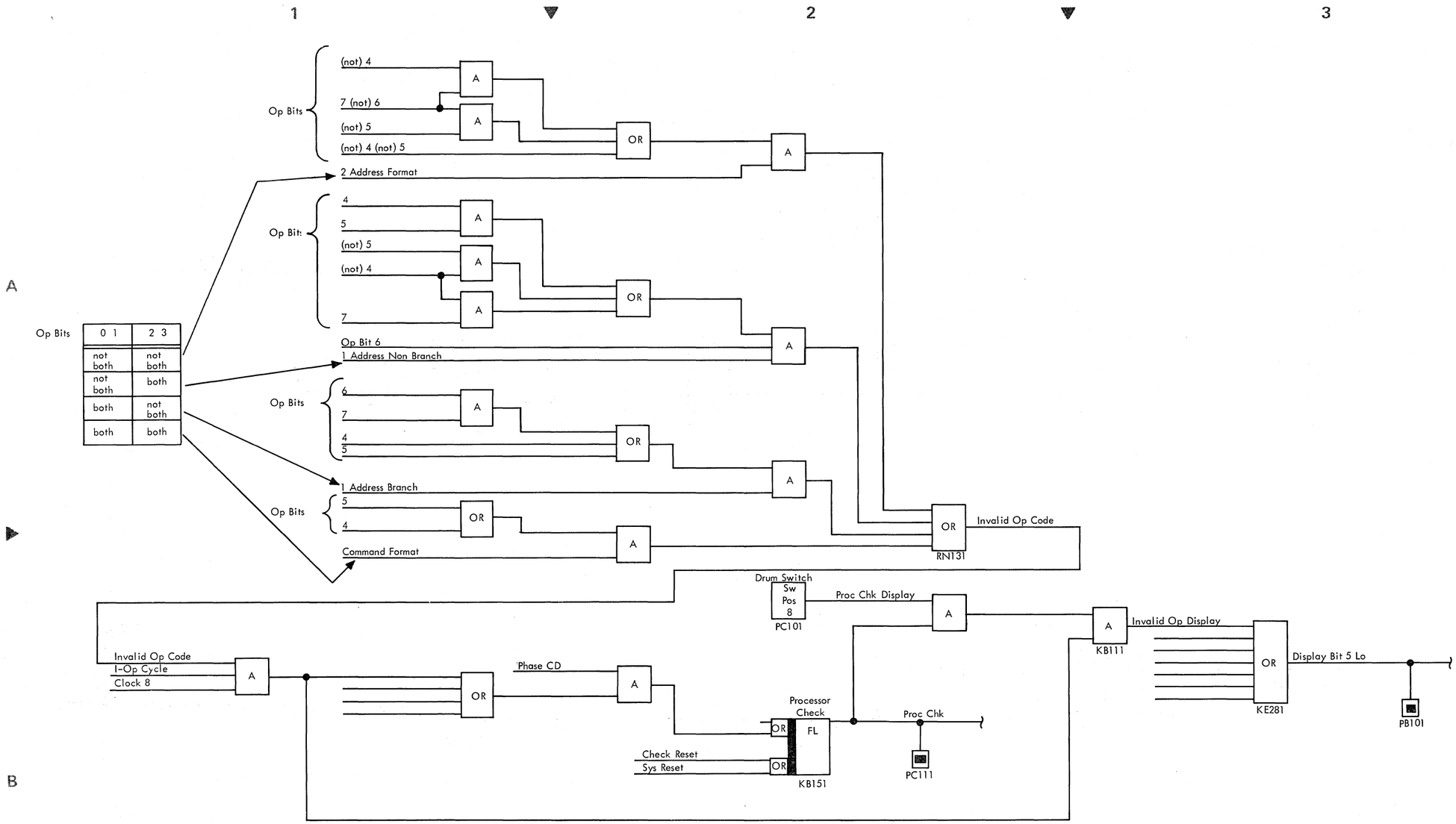
Note: Rotate drum switch to position 5 to display ALU and A register contents



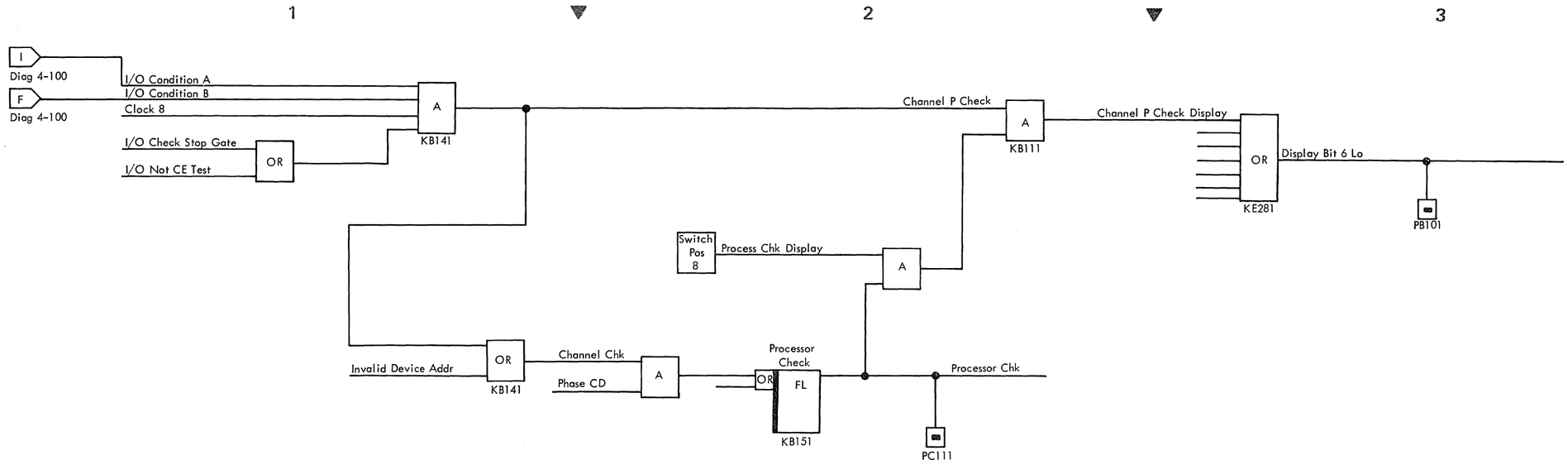
▶ Note: Rotate drum switch to position 7 to display CS priority bits, position 5 to display ALU output

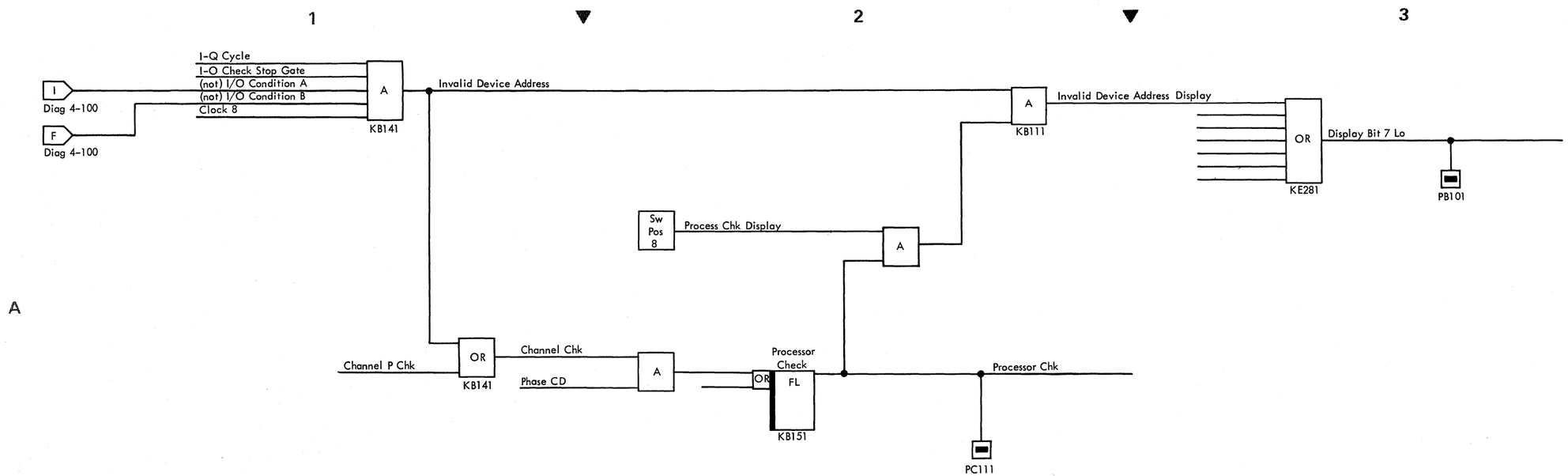


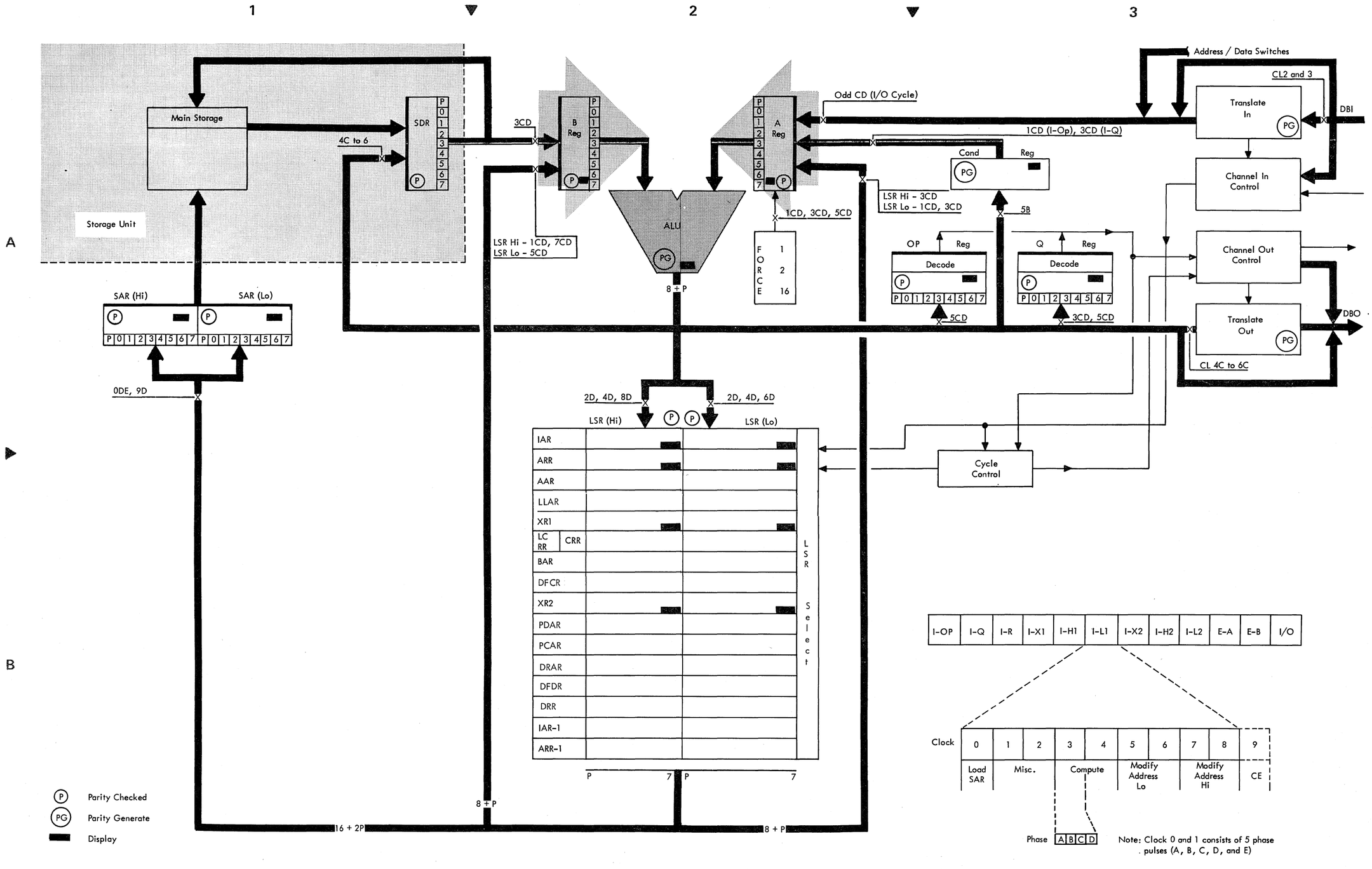
Note: Rotate drum switch to position 3 to display Op and Q registers contents



Note: Rotate drum switch to position 3 to display Op register contents


1
2
3
I
Diag 4-100
F
Diag 4-100
I/O Condition A
I/O Condition B
Clock 8
A
KB141
I/O Check Stop Gate
I/O Not CE Test
OR
Channel P Check
A
KB111
Channel P Check Display
OR
KE281
Display Bit 6 Lo
PB101
Switch Pos 8
Process Chk Display
A
Invalid Device Addr
OR
KB141
Channel Chk
Phase CD
A
Processor Check
OR
FL
KB151
Processor Chk
PC111
A
B

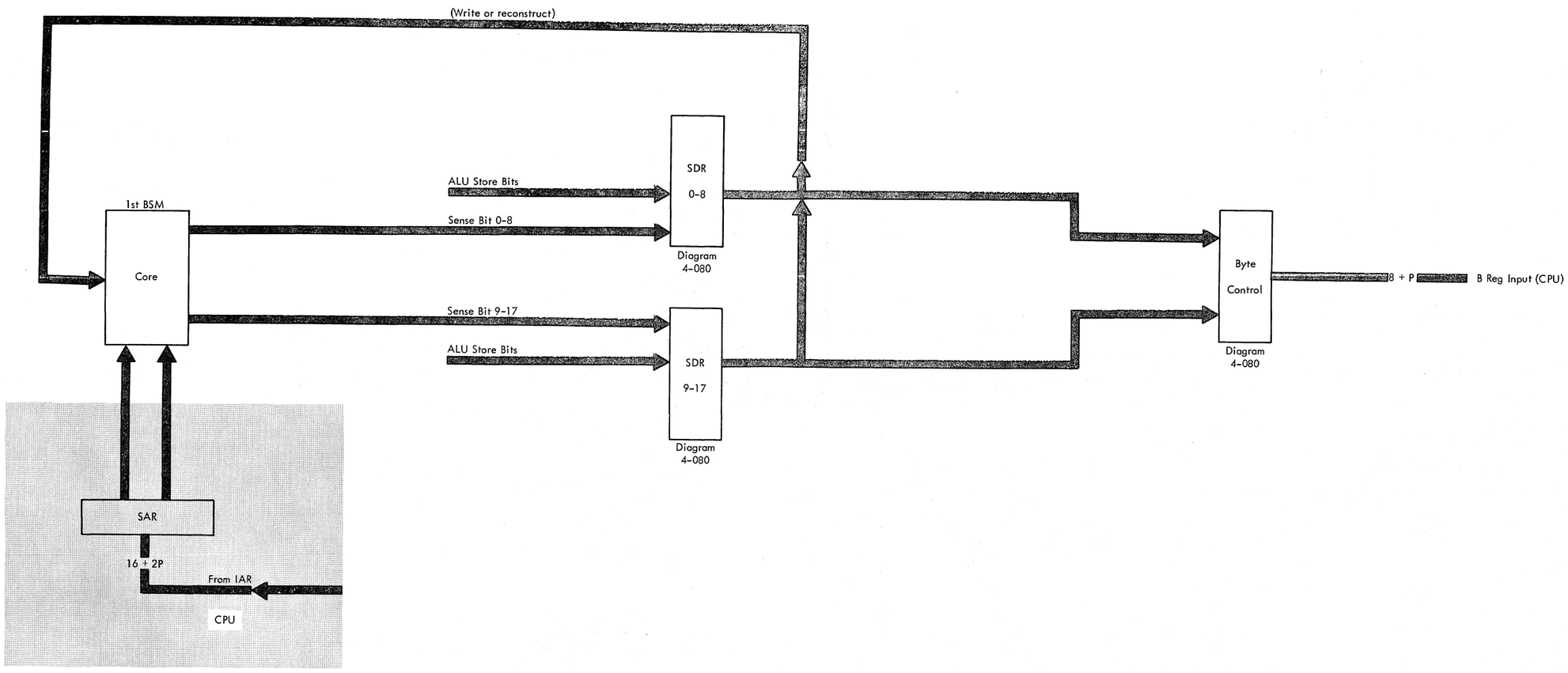

1
2
3
A
B
I-Q Cycle
I-O Check Stop Gate
(not) I/O Condition A
(not) I/O Condition B
Clock 8
I
Diag 4-100
F
Diag 4-100
A
KB141
Invalid Device Address
A
KB111
Invalid Device Address Display
OR
KE281
Display Bit 7 Lo
PB101
Sw Pos 8
Process Chk Display
A
OR
KB141
Channel P Chk
Channel Chk
Phase CD
A
Processor Check
OR
FL
KB151
Processor Chk
PC111



5406 CPU–Data Flow
CPU Data Flow

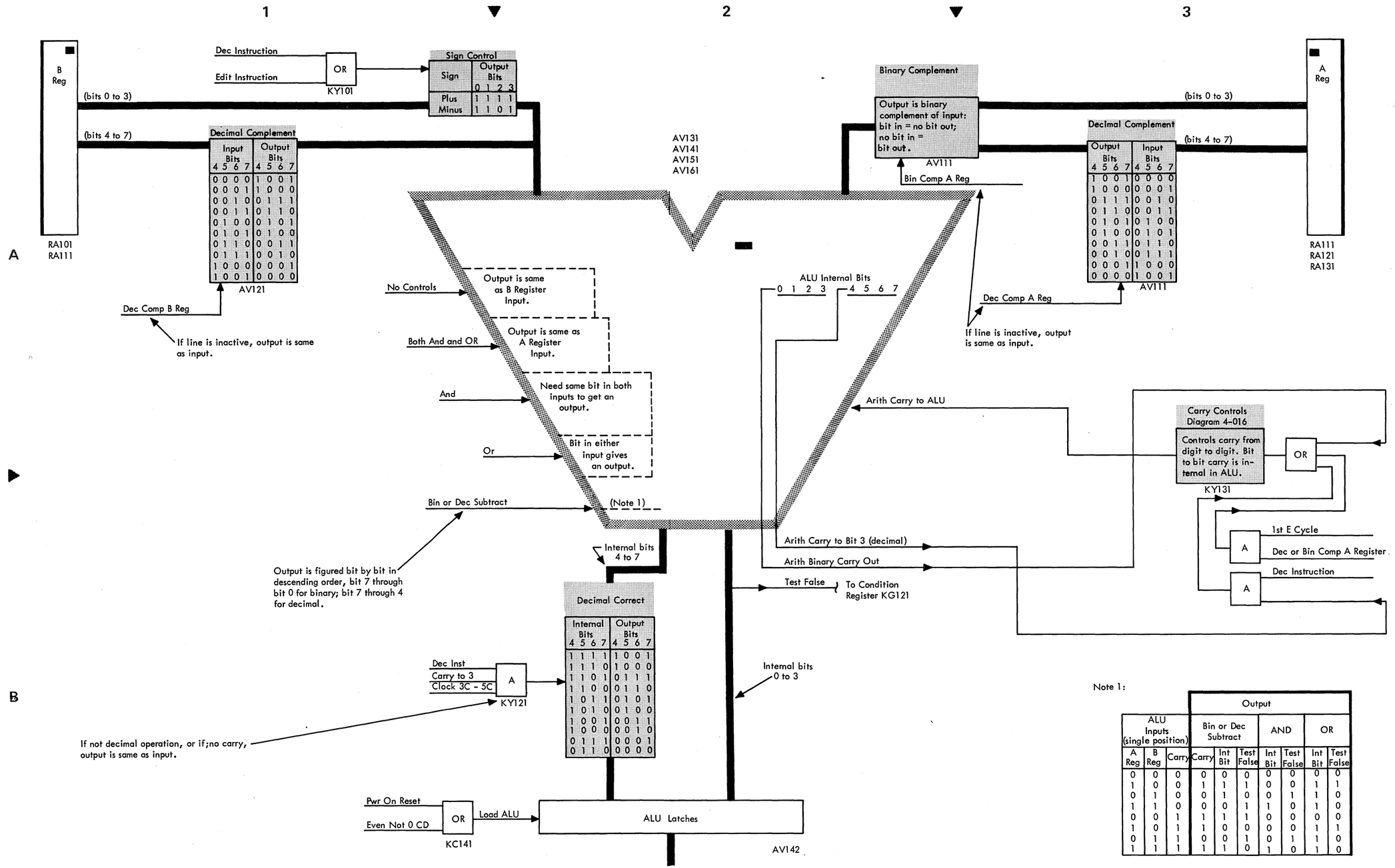
1 2 3

A



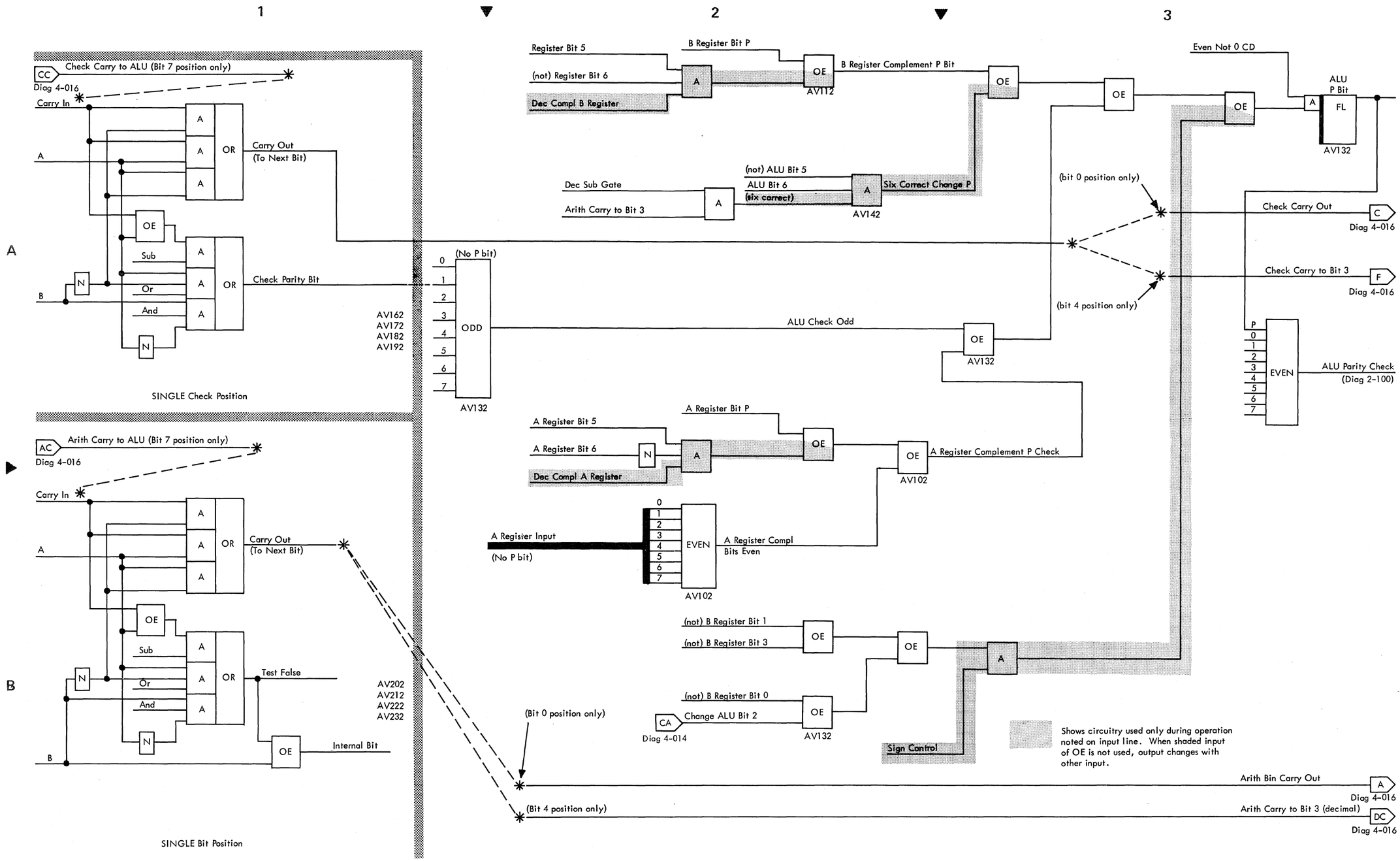
B

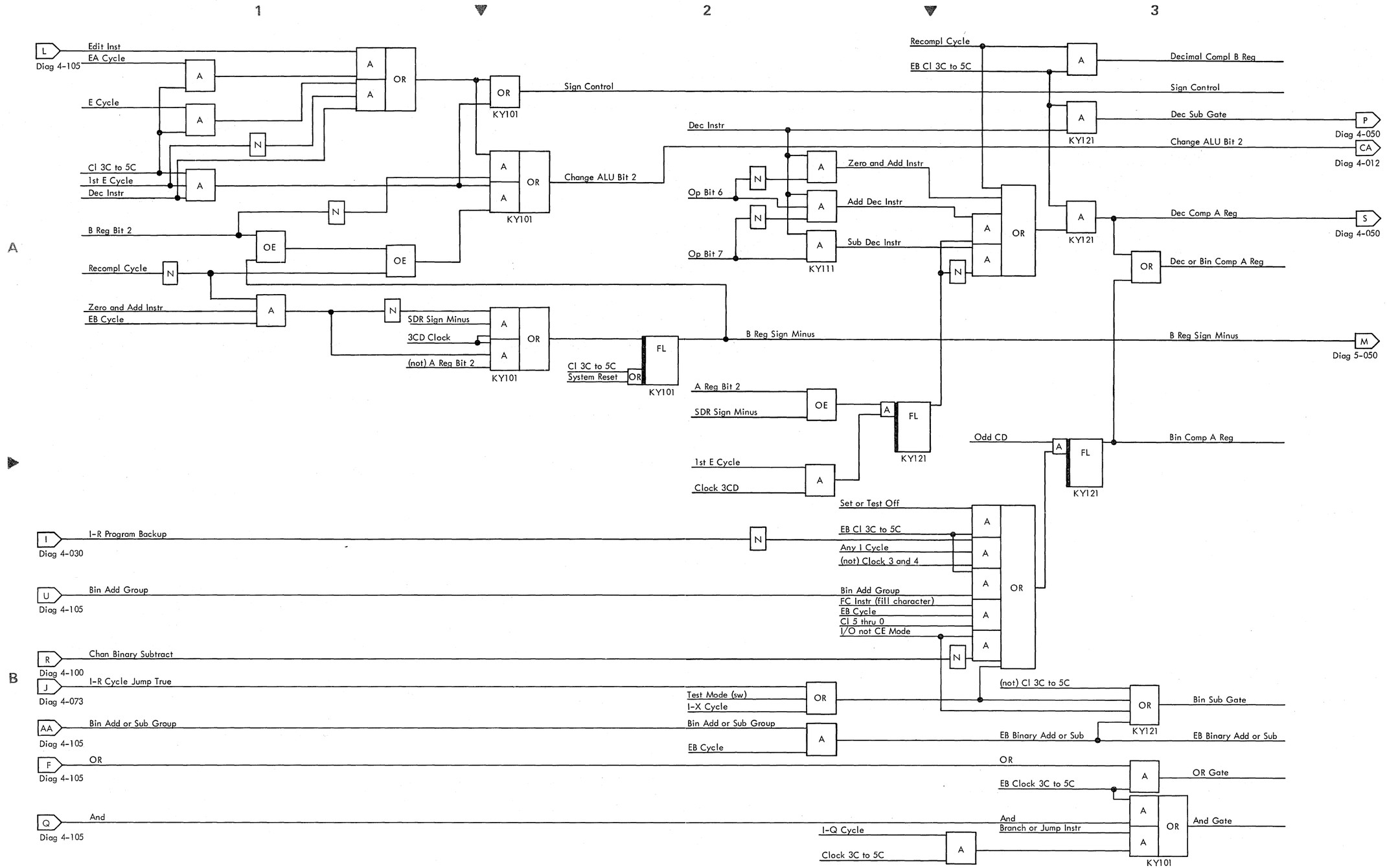
5406 CPU–Data Flow
Storage Data Flow

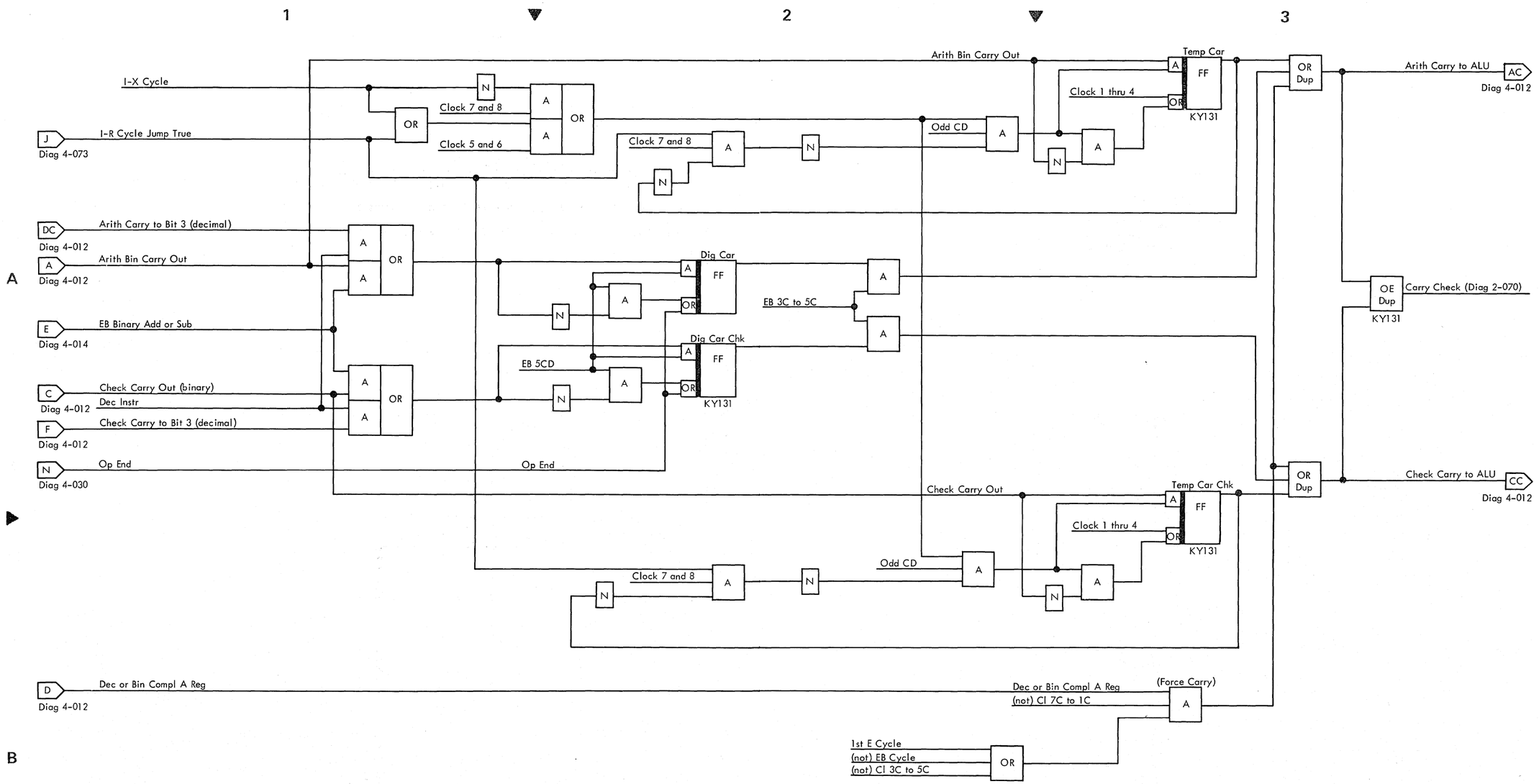


Note 1:

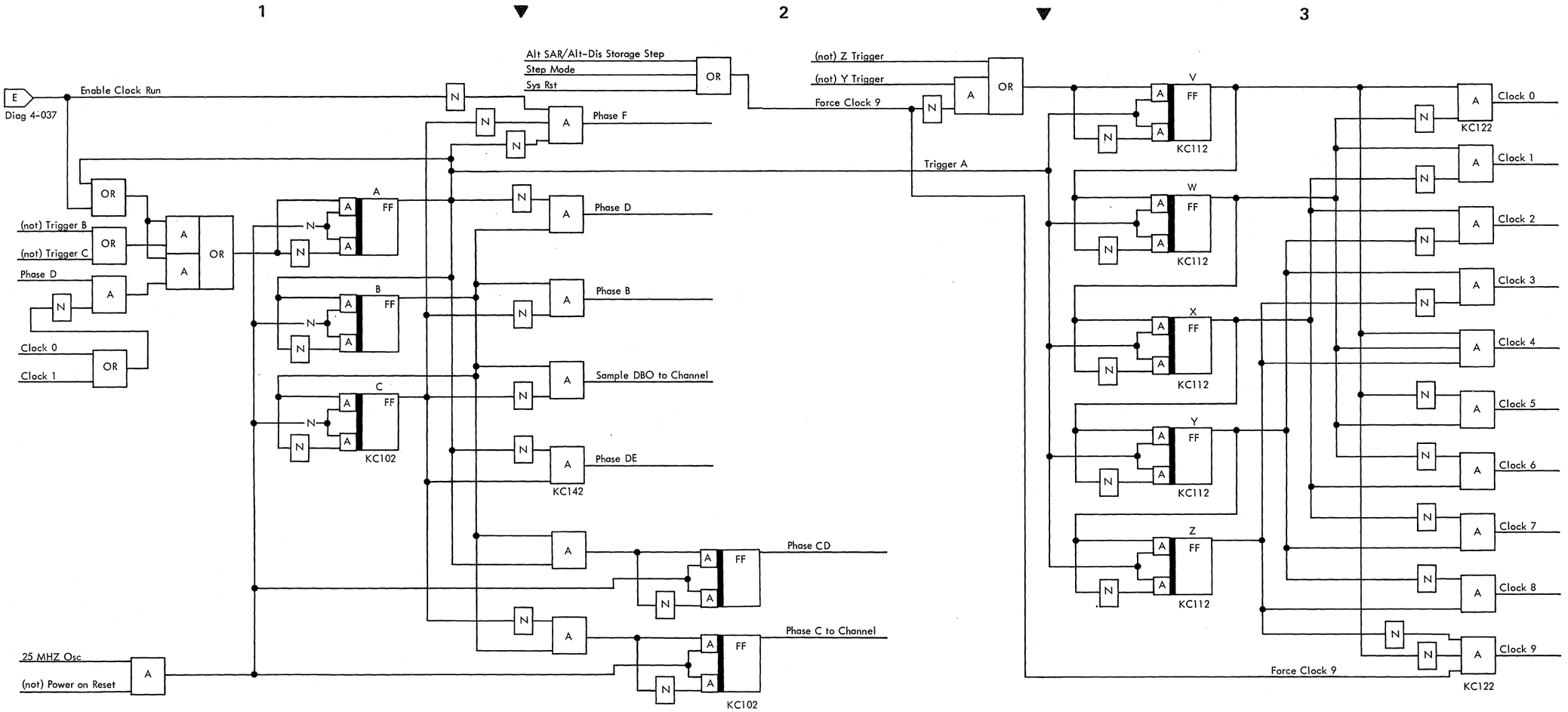
ALU Inputs (single position)			Output						
			Bin or Dec Subtract			AND		OR	
A Reg	B Reg	Carry	Carry	Int Bit	Test False	Int Bit	Test False	Int Bit	Test False
0	0	0	0	0	1	0	0	0	0
1	0	0	1	1	0	0	0	1	1
0	1	0	0	1	0	0	1	1	0
1	1	0	0	0	1	1	0	1	0
0	0	1	1	0	1	0	0	0	0
1	0	1	1	0	0	0	0	1	1
0	1	1	0	1	0	0	1	1	0
1	1	1	1	0	0	1	0	1	0


1
2
3
A
B
CC
Check Carry to ALU (Bit 7 position only)
Diag 4-016
Carry In
A
B
A
A
A
OR
Carry Out
(To Next Bit)
OE
Sub
Or
And
N
A
A
A
OR
Check Parity Bit
AV162
AV172
AV182
AV192
SINGLE Check Position
AC
Arith Carry to ALU (Bit 7 position only)
Diag 4-016
Carry In
A
B
Carry Out
(To Next Bit)
Sub
Or
And
Test False
Internal Bit
AV202
AV212
AV222
AV232
SINGLE Bit Position
Register Bit 5
(not) Register Bit 6
Dec Compl B Register
B Register Bit P
B Register Complement P Bit
AV112
Dec Sub Gate
Arith Carry to Bit 3
(not) ALU Bit 5
ALU Bit 6
(six correct)
Six Correct Change P
AV142
(No P bit)
ODD
AV132
ALU Check Odd
A Register Bit 5
A Register Bit 6
Dec Compl A Register
A Register Bit P
A Register Complement P Check
AV102
A Register Input
(No P bit)
EVEN
A Register Compl
Bits Even
AV102
(not) B Register Bit 1
(not) B Register Bit 3
(not) B Register Bit 0
CA
Change ALU Bit 2
Diag 4-014
AV132
Sign Control
(Bit 0 position only)
(Bit 4 position only)
Even Not 0 CD
ALU
P Bit
FL
AV132
(bit 0 position only)
(bit 4 position only)
Check Carry Out
C
Diag 4-016
Check Carry to Bit 3
F
Diag 4-016
P
EVEN
ALU Parity Check
(Diag 2-100)
Shows circuitry used only during operation noted on input line. When shaded input of OE is not used, output changes with other input.
Arith Bin Carry Out
A
Diag 4-016
Arith Carry to Bit 3 (decimal)
DC
Diag 4-016

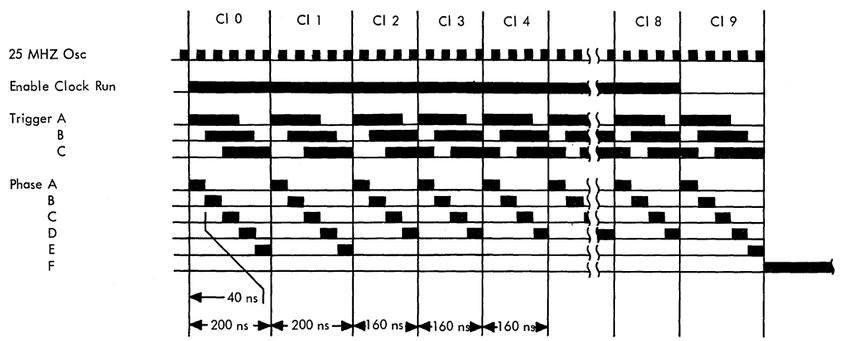

1
2
3
A
B
L
Diag 4-105
Edit Inst
EA Cycle
E Cycle
Cl 3C to 5C
1st E Cycle
Dec Instr
B Reg Bit 2
Recompl Cycle
Zero and Add Instr
EB Cycle
A
OR
N
OE
KY101
Sign Control
Change ALU Bit 2
SDR Sign Minus
3CD Clock
(not) A Reg Bit 2
FL
Cl 3C to 5C
System Reset
B Reg Sign Minus
Op Bit 6
Op Bit 7
KY111
Add Dec Instr
Sub Dec Instr
KY121
EB Cl 3C to 5C
Decimal Compl B Reg
Dec Sub Gate
P
Diag 4-050
Change ALU Bit 2
CA
Diag 4-012
Dec Comp A Reg
S
Diag 4-050
Dec or Bin Comp A Reg
B Reg Sign Minus
M
Diag 5-050
A Reg Bit 2
SDR Sign Minus
1st E Cycle
Clock 3CD
Odd CD
Bin Comp A Reg
Set or Test Off
I-R Program Backup
I
Diag 4-030
EB Cl 3C to 5C
Any 1 Cycle
(not) Clock 3 and 4
Bin Add Group
U
Diag 4-105
FC Instr (fill character)
EB Cycle
Cl 5 thru 0
I/O not CE Mode
Chan Binary Subtract
R
Diag 4-100
I-R Cycle Jump True
J
Diag 4-073
Test Mode (sw)
I-X Cycle
(not) Cl 3C to 5C
Bin Sub Gate
Bin Add or Sub Group
AA
Diag 4-105
EB Binary Add or Sub
OR
F
Diag 4-105
EB Clock 3C to 5C
OR Gate
And
Q
Diag 4-105
I-Q Cycle
Clock 3C to 5C
Branch or Jump Instr
And Gate

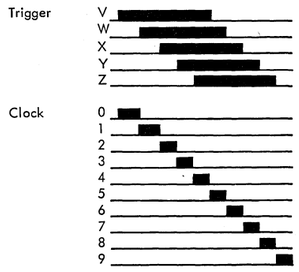

1
2
3
A
B
I-X Cycle
J
I-R Cycle Jump True
Diag 4-073
N
Clock 7 and 8
Clock 5 and 6
OR
A
Arith Bin Carry Out
Temp Car
FF
KY131
Clock 1 thru 4
Odd CD
OR Dup
Arith Carry to ALU
AC
Diag 4-012
DC
Arith Carry to Bit 3 (decimal)
Diag 4-012
Arith Bin Carry Out
Diag 4-012
Dig Car
EB 3C to 5C
OE Dup
Carry Check (Diag 2-070)
EB Binary Add or Sub
Diag 4-014
Dig Car Chk
EB 5CD
C
Check Carry Out (binary)
Dec Instr
Diag 4-012
F
Check Carry to Bit 3 (decimal)
Diag 4-012
N
Op End
Diag 4-030
Check Carry Out
Check Carry to ALU
CC
Diag 4-012
D
Dec or Bin Compl A Reg
Diag 4-012
(Force Carry)
(not) CI 7C to 1C
1st E Cycle
(not) EB Cycle
(not) CI 3C to 5C

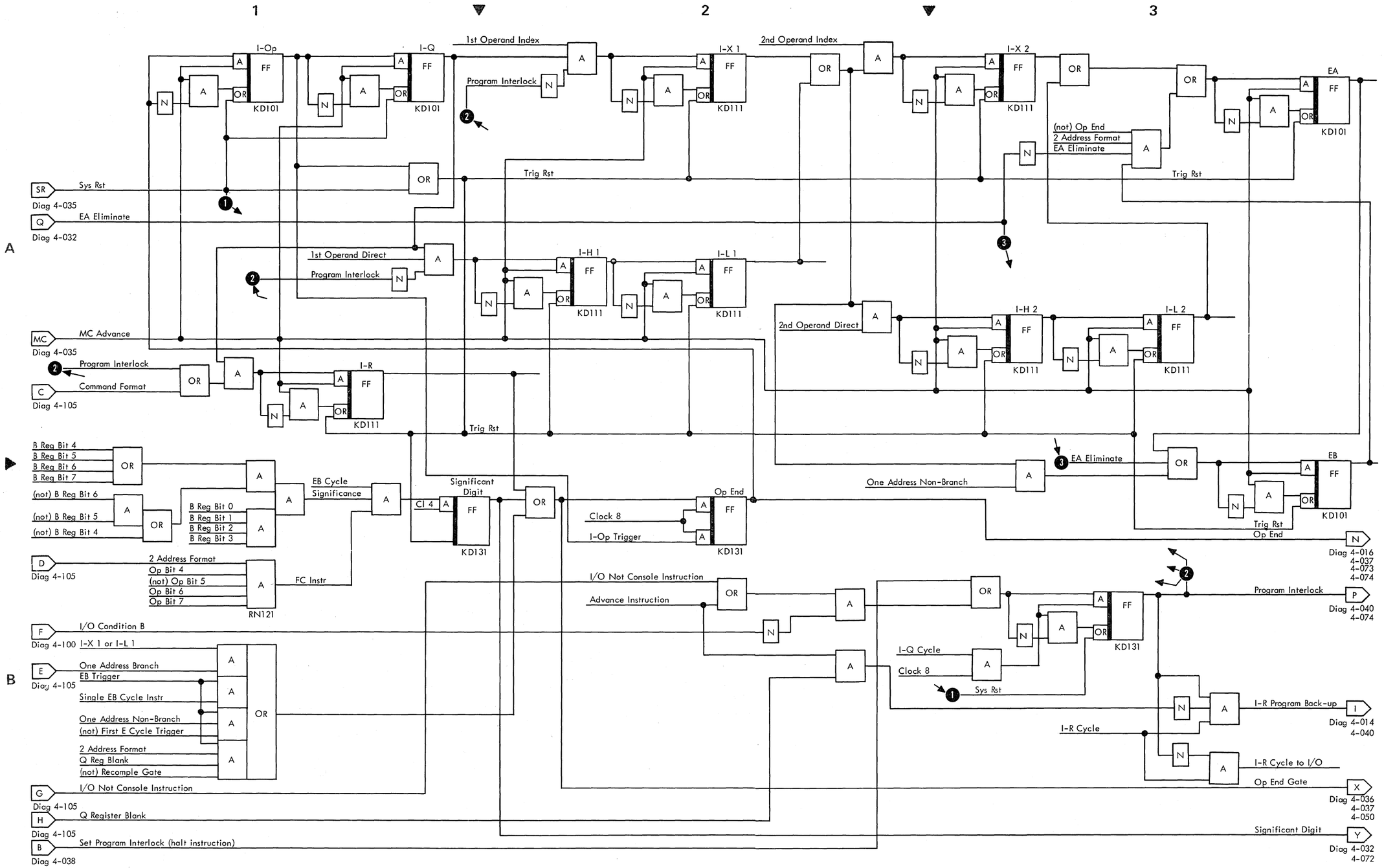
A

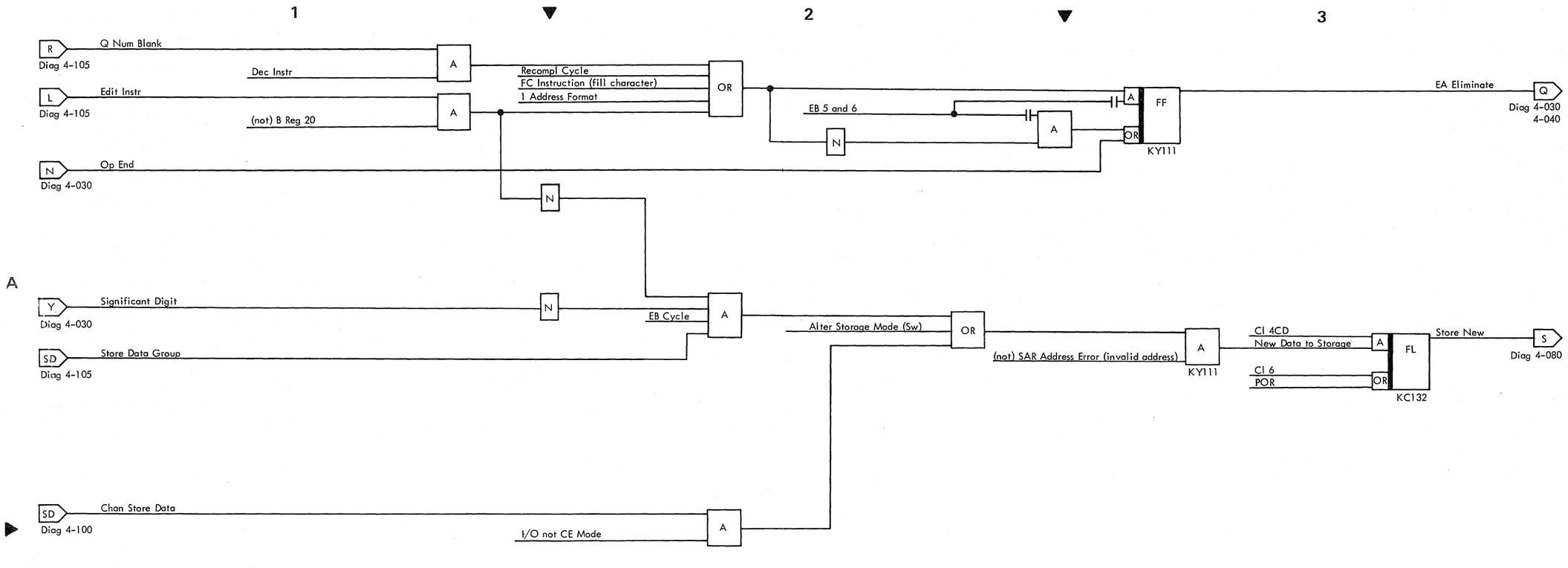

1
2
3
E
Diag 4-037
Enable Clock Run
Alt SAR/Alt-Dis Storage Step
Step Mode
Sys Rst
(not) Z Trigger
(not) Y Trigger
Force Clock 9
Trigger A
(not) Trigger B
(not) Trigger C
Phase D
Clock 0
Clock 1
Phase F
Phase D
Phase B
Sample DBO to Channel
Phase DE
Phase CD
Phase C to Channel
25 MHZ Osc
(not) Power on Reset
A
B
C
FF
KC102
KC142
V
W
X
Y
Z
KC112
Clock 0
Clock 1
Clock 2
Clock 3
Clock 4
Clock 5
Clock 6
Clock 7
Clock 8
Clock 9
KC122
Force Clock 9

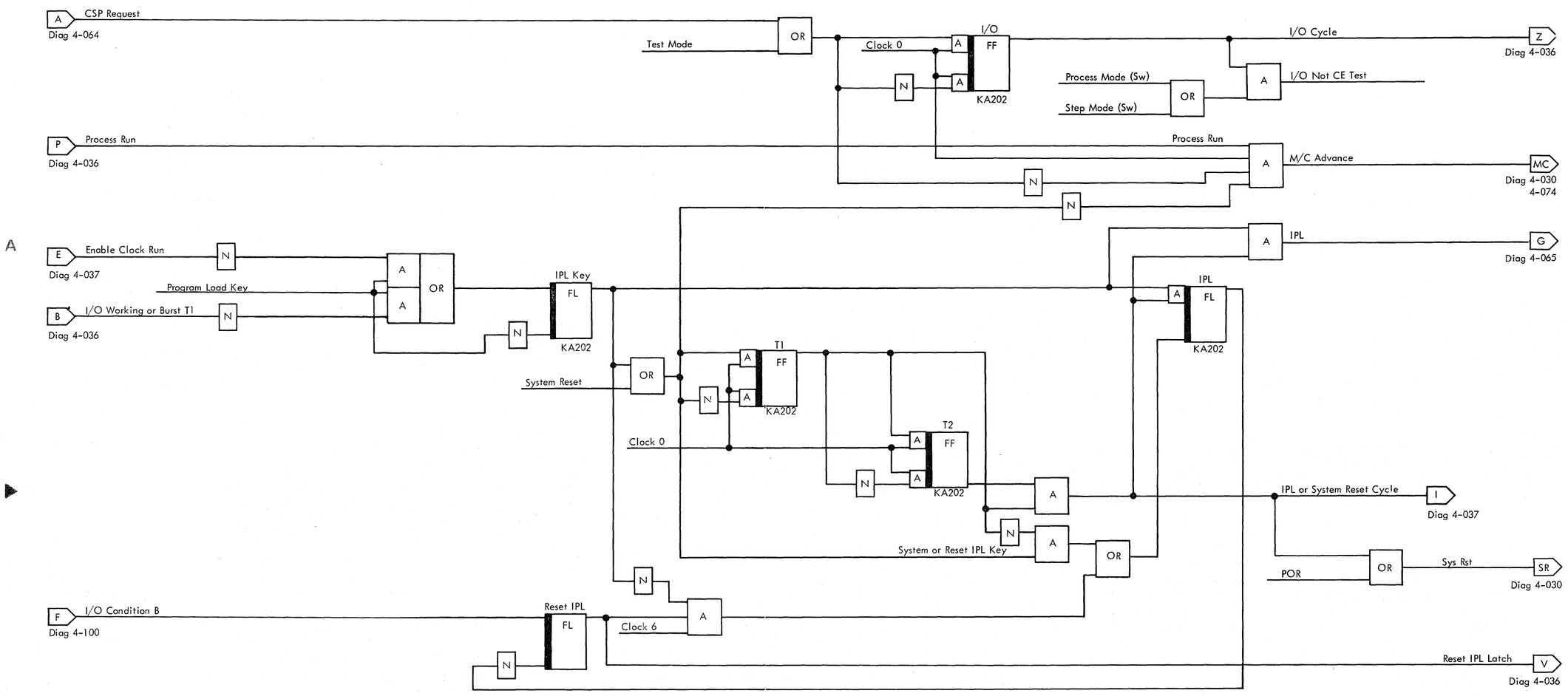
B

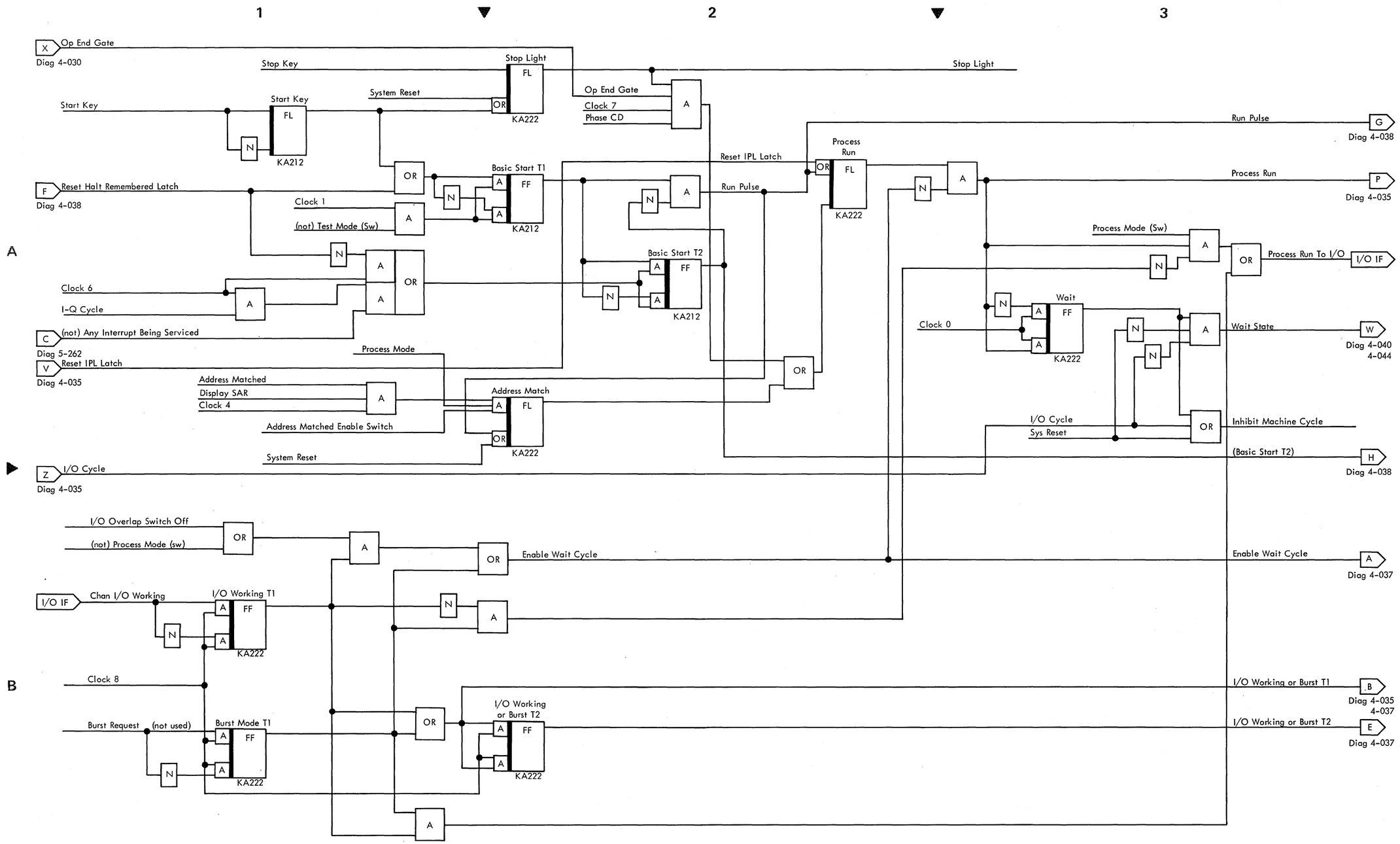

CI 0
CI 1
CI 2
CI 3
CI 4
CI 8
CI 9
25 MHZ Osc
Enable Clock Run
Trigger A
B
C
Phase A
B
C
D
E
F
40 ns
200 ns
200 ns
160 ns
160 ns
160 ns

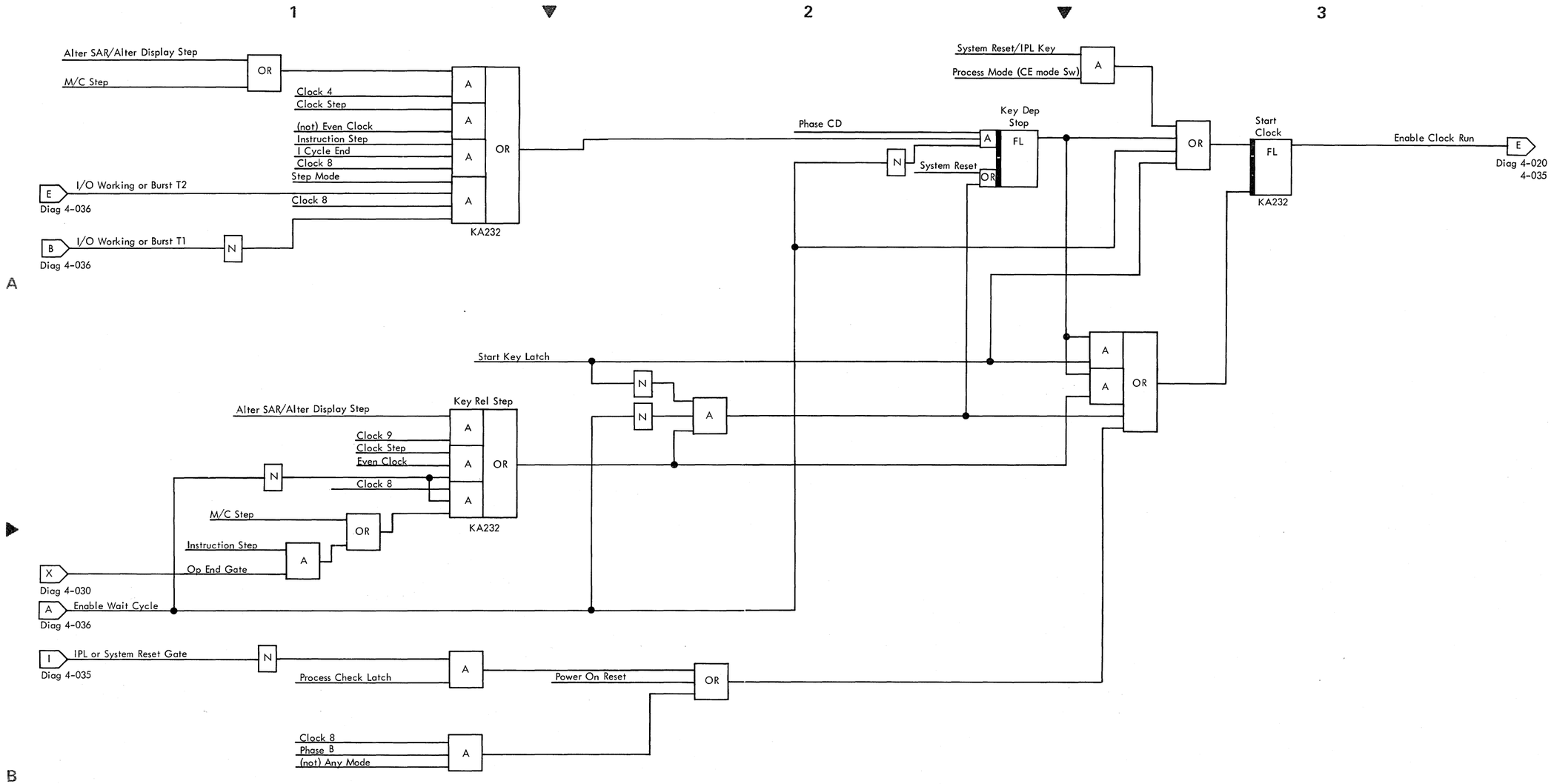

Trigger
V
W
X
Y
Z
Clock
0
1
2
3
4
5
6
7
8
9

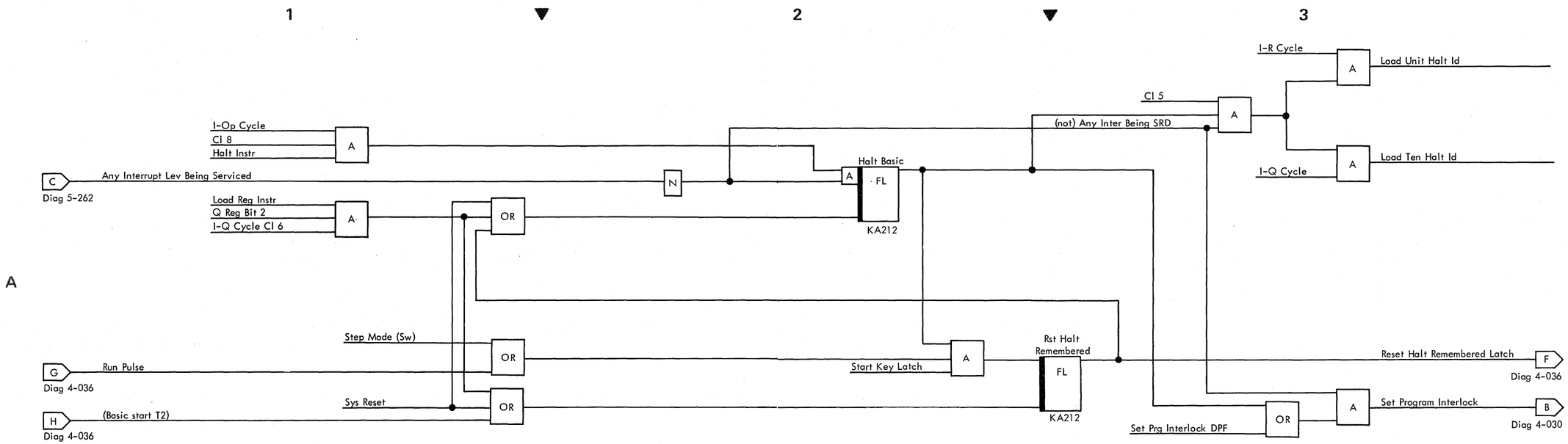

1
2
3
A
B
I-Op
I-Q
1st Operand Index
I-X 1
2nd Operand Index
I-X 2
EA
KD101
KD111
KD131
FF
A
OR
N
Program Interlock
Trig Rst
(not) Op End
2 Address Format
EA Eliminate
SR
Sys Rst
Diag 4-035
Q
EA Eliminate
Diag 4-032
1st Operand Direct
I-H 1
I-L 1
2nd Operand Direct
I-H 2
I-L 2
MC
MC Advance
Diag 4-035
C
Command Format
Diag 4-105
I-R
B Reg Bit 4
B Reg Bit 5
B Reg Bit 6
B Reg Bit 7
(not) B Reg Bit 6
(not) B Reg Bit 5
(not) B Reg Bit 4
B Reg Bit 0
B Reg Bit 1
B Reg Bit 2
B Reg Bit 3
EB Cycle
Significance
Significant
Digit
CI 4
Clock 8
I-Op Trigger
Op End
EB
One Address Non-Branch
EA Eliminate
Trig Rst
Op End
N
Diag 4-016
4-037
4-073
4-074
D
Diag 4-105
2 Address Format
Op Bit 4
(not) Op Bit 5
Op Bit 6
Op Bit 7
RN121
FC Instr
I/O Not Console Instruction
Advance Instruction
Program Interlock
P
Diag 4-040
4-074
F
Diag 4-100
I/O Condition B
I-X 1 or I-L 1
E
Diag 4-105
One Address Branch
EB Trigger
Single EB Cycle Instr
One Address Non-Branch
(not) First E Cycle Trigger
2 Address Format
Q Reg Blank
(not) Recomple Gate
I-Q Cycle
Clock 8
Sys Rst
I-R Cycle
I-R Program Back-up
I
Diag 4-014
4-040
I-R Cycle to I/O
Op End Gate
X
Diag 4-036
4-037
4-050
G
Diag 4-105
I/O Not Console Instruction
H
Diag 4-105
Q Register Blank
B
Diag 4-038
Set Program Interlock (halt instruction)
Significant Digit
Y
Diag 4-032
4-072

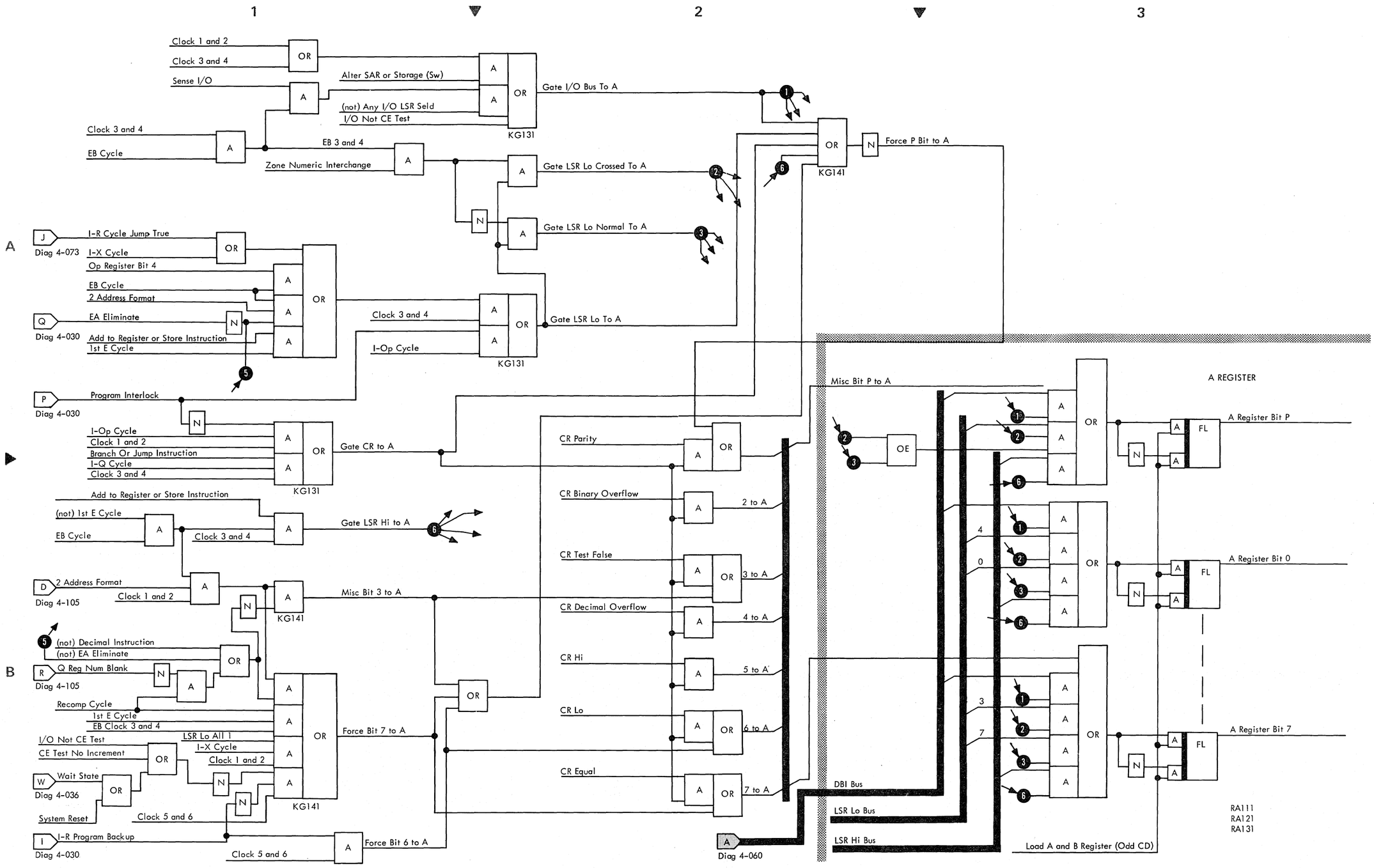

1
2
3
A
B
R
Q Num Blank
Diag 4-105
Dec Instr
A
L
Edit Instr
Diag 4-105
(not) B Reg 20
A
Recompl Cycle
FC Instruction (fill character)
1 Address Format
OR
EB 5 and 6
N
A
A
OR
FF
KY111
EA Eliminate
Q
Diag 4-030
4-040
N
Op End
Diag 4-030
N
Y
Significant Digit
Diag 4-030
N
EB Cycle
A
Alter Storage Mode (Sw)
OR
SD
Store Data Group
Diag 4-105
(not) SAR Address Error (invalid address)
A
KY111
CI 4CD
New Data to Storage
CI 6
POR
A
OR
FL
KC132
Store New
S
Diag 4-080
SD
Chan Store Data
Diag 4-100
I/O not CE Mode
A


1
2
3
A
B
CSP Request
Diag 4-064
Test Mode
OR
Clock 0
I/O
FF
KA202
N
Process Mode (Sw)
Step Mode (Sw)
OR
A
I/O Cycle
Z
Diag 4-036
I/O Not CE Test
P
Process Run
Diag 4-036
Process Run
M/C Advance
MC
Diag 4-030
4-074
E
Enable Clock Run
Diag 4-037
Program Load Key
B
I/O Working or Burst T1
Diag 4-036
IPL Key
FL
KA202
System Reset
T1
T2
Clock 0
IPL
G
Diag 4-065
IPL or System Reset Cycle
I
Diag 4-037
System or Reset IPL Key
POR
Sys Rst
SR
Diag 4-030
F
I/O Condition B
Diag 4-100
Reset IPL
Clock 6
Reset IPL Latch
V
Diag 4-036

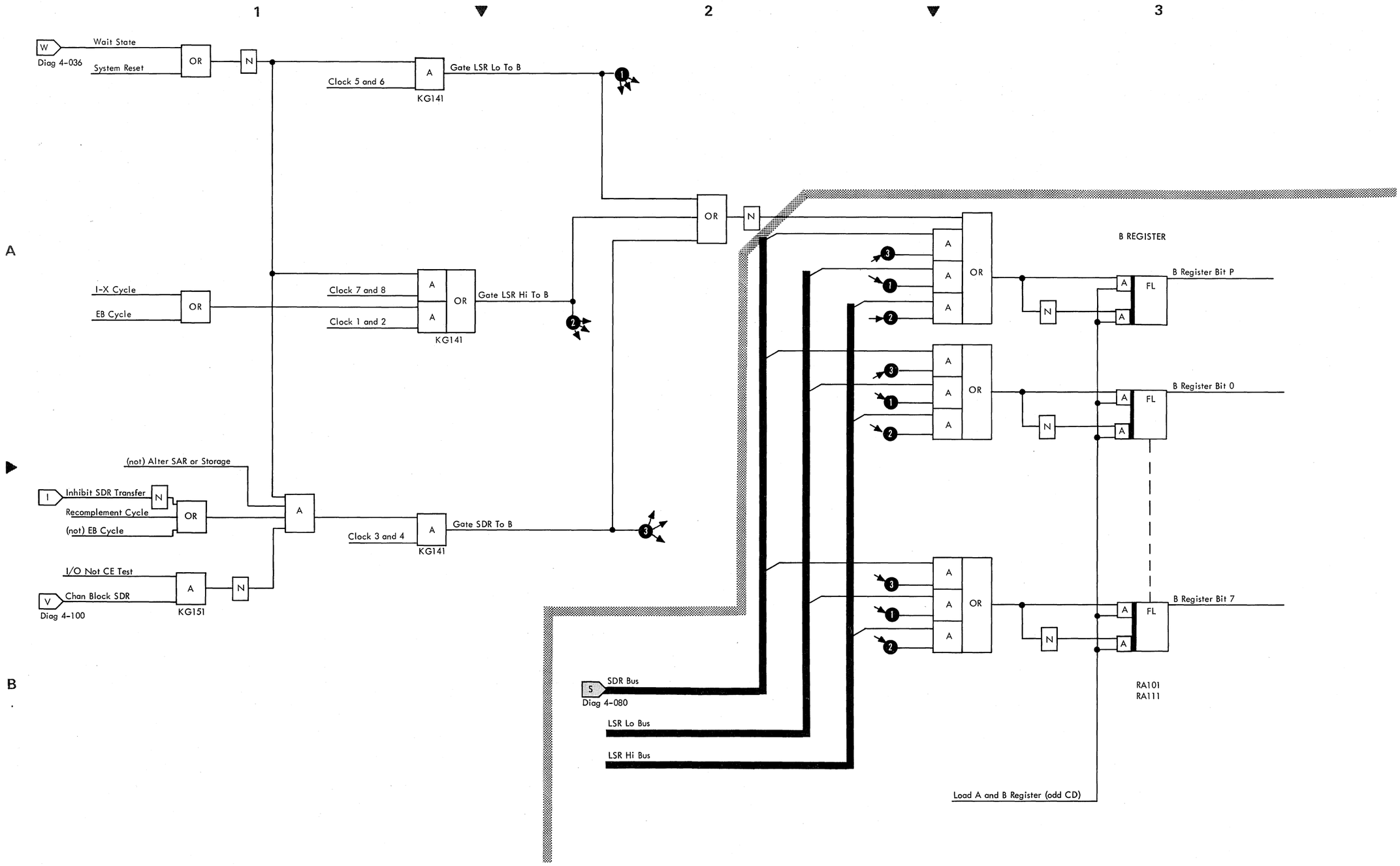

1
2
3
A
B
X Op End Gate
Diag 4-030
Stop Key
Stop Light
FL
System Reset
OR
KA222
Start Key
Start Key
FL
N
KA212
Op End Gate
Clock 7
Phase CD
A
Stop Light
Run Pulse
G
Diag 4-038
Process Run
P
Diag 4-035
F Reset Halt Remembered Latch
Diag 4-038
OR
Basic Start T1
A
N
FF
A
KA212
Clock 1
(not) Test Mode (Sw)
A
Reset IPL Latch
Process Run
OR
FL
KA222
N
A
Run Pulse
Process Mode (Sw)
Process Run To I/O
I/O IF
N
A
OR
Basic Start T2
A
FF
A
KA212
N
Clock 6
I-Q Cycle
A
A
A
OR
C (not) Any Interrupt Being Serviced
Diag 5-262
V Reset IPL Latch
Diag 4-035
Process Mode
Address Matched
Display SAR
Clock 4
A
Address Match
A
FL
OR
KA222
Address Matched Enable Switch
System Reset
OR
Wait
N
A
FF
A
KA222
Clock 0
N
N
A
Wait State
W
Diag 4-040
4-044
I/O Cycle
Sys Reset
OR
Inhibit Machine Cycle
(Basic Start T2)
H
Diag 4-038
Z I/O Cycle
Diag 4-035
I/O Overlap Switch Off
(not) Process Mode (sw)
OR
A
OR
Enable Wait Cycle
Enable Wait Cycle
A
Diag 4-037
I/O IF
Chan I/O Working
I/O Working T1
A
FF
A
KA222
N
N
A
Clock 8
I/O Working or Burst T1
B
Diag 4-035
4-037
Burst Request
(not used)
Burst Mode T1
A
FF
A
KA222
N
OR
I/O Working
or Burst T2
A
FF
A
KA222
I/O Working or Burst T2
E
Diag 4-037
A

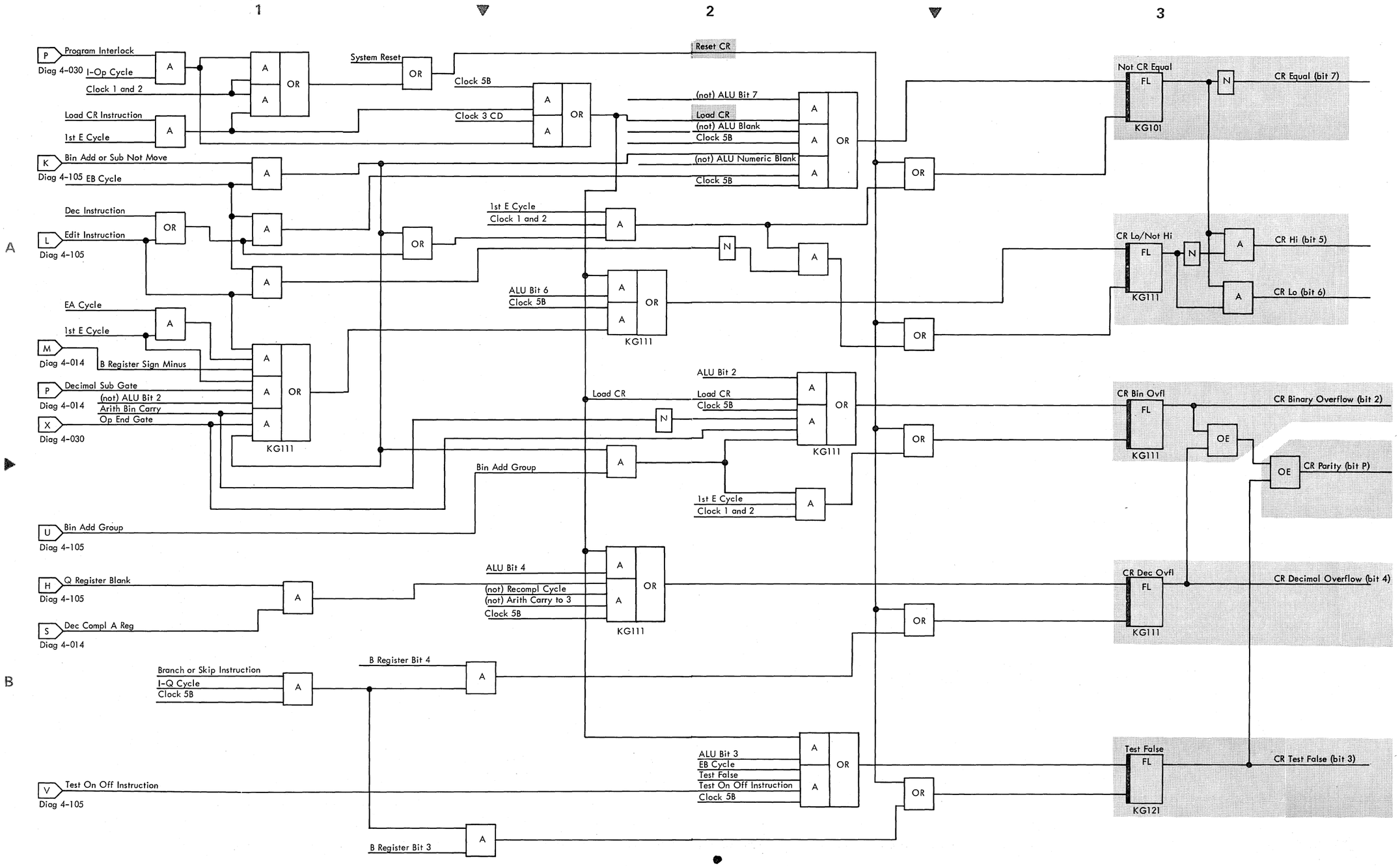

1
2
3
A
B
Alter SAR/Alter Display Step
M/C Step
OR
Clock 4
Clock Step
(not) Even Clock
Instruction Step
1 Cycle End
Clock 8
Step Mode
A
OR
KA232
E
I/O Working or Burst T2
Diag 4-036
Clock 8
B
I/O Working or Burst T1
Diag 4-036
N
Phase CD
System Reset/IPL Key
Process Mode (CE mode Sw)
Key Dep Stop
FL
System Reset
Start Clock
Enable Clock Run
Diag 4-020
4-035
Start Key Latch
Key Rel Step
Clock 9
Clock Step
Even Clock
Clock 8
M/C Step
Instruction Step
Op End Gate
X
Diag 4-030
A
Enable Wait Cycle
Diag 4-036
I
IPL or System Reset Gate
Diag 4-035
Process Check Latch
Power On Reset
Clock 8
Phase B
(not) Any Mode

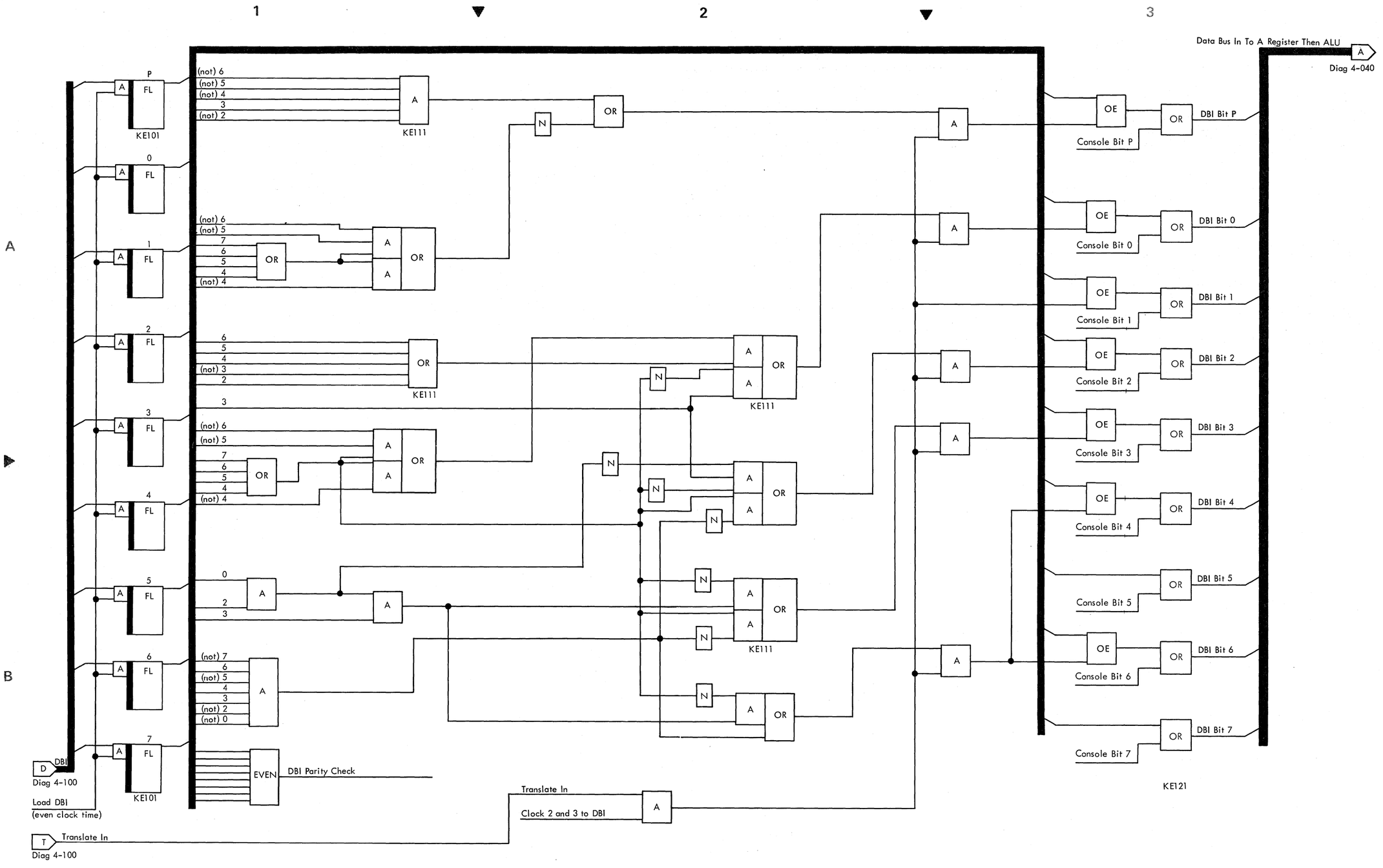

1
2
3
A
B
I-Op Cycle
CI 8
Halt Instr
A
C
Any Interrupt Lev Being Serviced
Diag 5-262
N
Load Reg Instr
Q Reg Bit 2
I-Q Cycle CI 6
A
OR
Halt Basic
A
FL
KA212
(not) Any Inter Being SRD
CI 5
A
I-R Cycle
A
Load Unit Halt Id
I-Q Cycle
A
Load Ten Halt Id
Step Mode (Sw)
OR
G
Run Pulse
Diag 4-036
Start Key Latch
A
Rst Halt
Remembered
FL
KA212
Reset Halt Remembered Latch
F
Diag 4-036
Sys Reset
OR
H
(Basic start T2)
Diag 4-036
Set Prg Interlock DPF
OR
A
Set Program Interlock
B
Diag 4-030

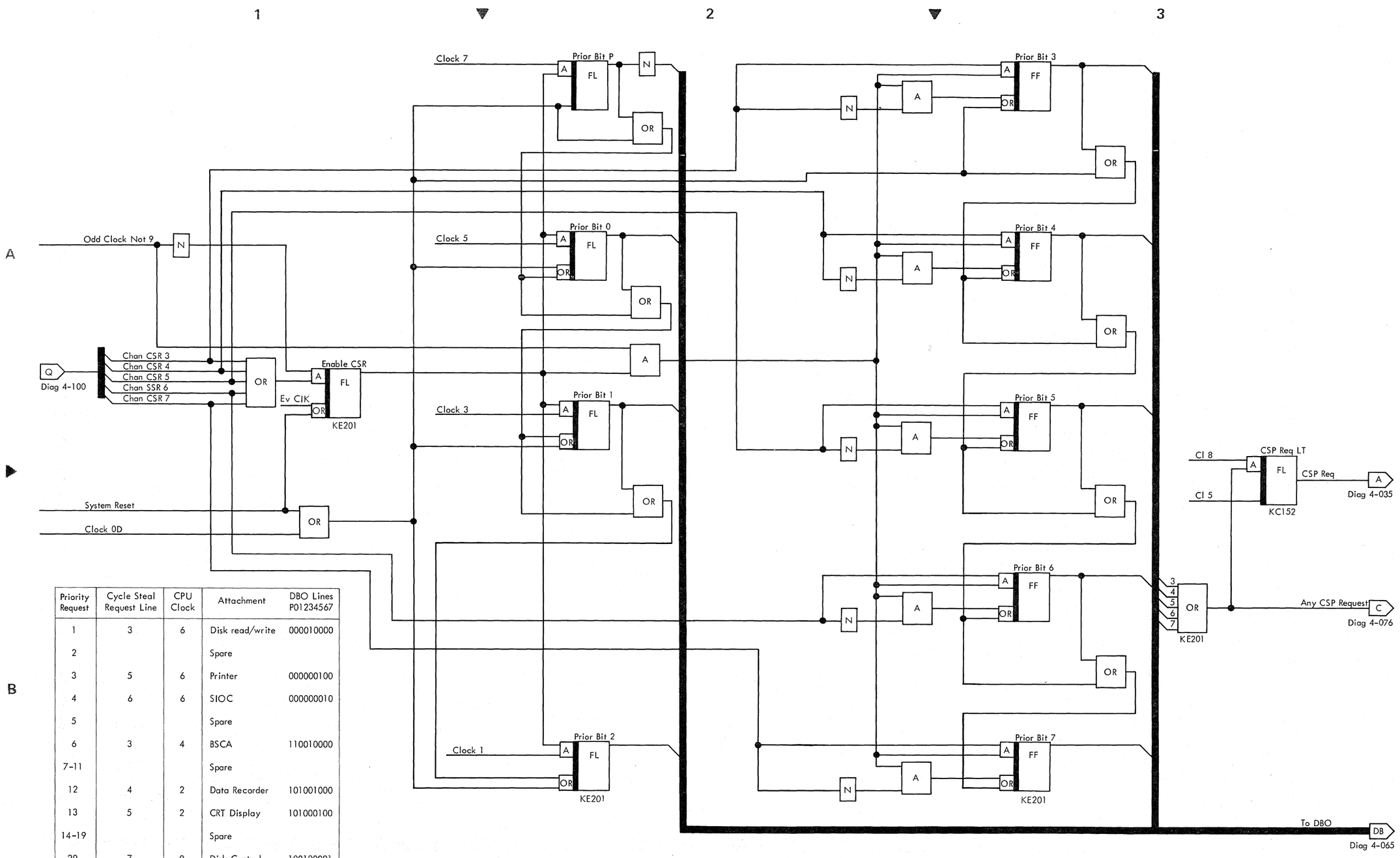


5406 CPU–Functional Units
A Register Controls


1
2
3
A
B
W
Wait State
Diag 4-036
System Reset
OR
N
Clock 5 and 6
A
Gate LSR Lo To B
KG141
I-X Cycle
EB Cycle
OR
Clock 7 and 8
Clock 1 and 2
A
A
OR
Gate LSR Hi To B
KG141
(not) Alter SAR or Storage
I
Inhibit SDR Transfer
Recomplement Cycle
(not) EB Cycle
OR
A
Clock 3 and 4
A
Gate SDR To B
KG141
I/O Not CE Test
V
Chan Block SDR
Diag 4-100
A
N
KG151
OR
N
B REGISTER
A
A
A
OR
B Register Bit P
N
A
A
FL
A
OR
B Register Bit 0
N
A
A
FL
A
OR
B Register Bit 7
N
A
A
FL
RA101
RA111
S
SDR Bus
Diag 4-080
LSR Lo Bus
LSR Hi Bus
Load A and B Register (odd CD)

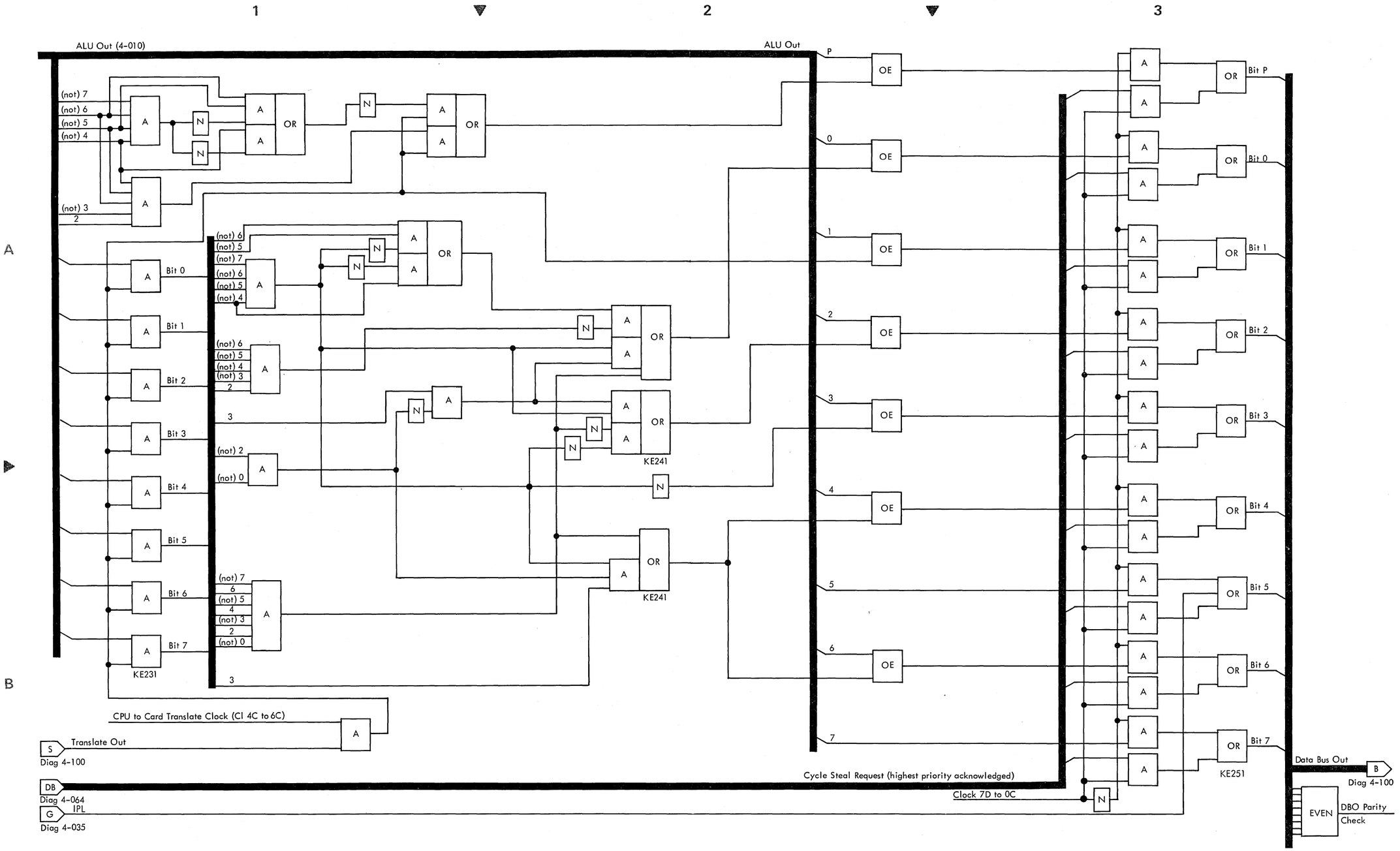

1
2
3
A
B
Reset CR
System Reset
OR
Clock 5B
Clock 3 CD
P Program Interlock
Diag 4-030 I-Op Cycle
Clock 1 and 2
Load CR Instruction
1st E Cycle
K Bin Add or Sub Not Move
Diag 4-105 EB Cycle
Dec Instruction
L Edit Instruction
Diag 4-105
EA Cycle
1st E Cycle
M
Diag 4-014 B Register Sign Minus
P Decimal Sub Gate
Diag 4-014 (not) ALU Bit 2
Arith Bin Carry
X Op End Gate
Diag 4-030
KG111
Bin Add Group
U Bin Add Group
Diag 4-105
H Q Register Blank
Diag 4-105
S Dec Compl A Reg
Diag 4-014
Branch or Skip Instruction
I-Q Cycle
Clock 5B
B Register Bit 4
B Register Bit 3
V Test On Off Instruction
Diag 4-105
(not) ALU Bit 7
Load CR
(not) ALU Blank
Clock 5B
(not) ALU Numeric Blank
Clock 5B
1st E Cycle
Clock 1 and 2
ALU Bit 6
Clock 5B
Load CR
ALU Bit 2
Load CR
Clock 5B
1st E Cycle
Clock 1 and 2
ALU Bit 4
(not) Recompl Cycle
(not) Arith Carry to 3
Clock 5B
ALU Bit 3
EB Cycle
Test False
Test On Off Instruction
Clock 5B
N
FL
KG101
Not CR Equal
CR Equal (bit 7)
KG111
CR Lo/Not Hi
CR Hi (bit 5)
CR Lo (bit 6)
KG111
CR Bin Ovfl
CR Binary Overflow (bit 2)
OE
CR Parity (bit P)
KG111
CR Dec Ovfl
CR Decimal Overflow (bit 4)
KG111
Test False
CR Test False (bit 3)
KG121

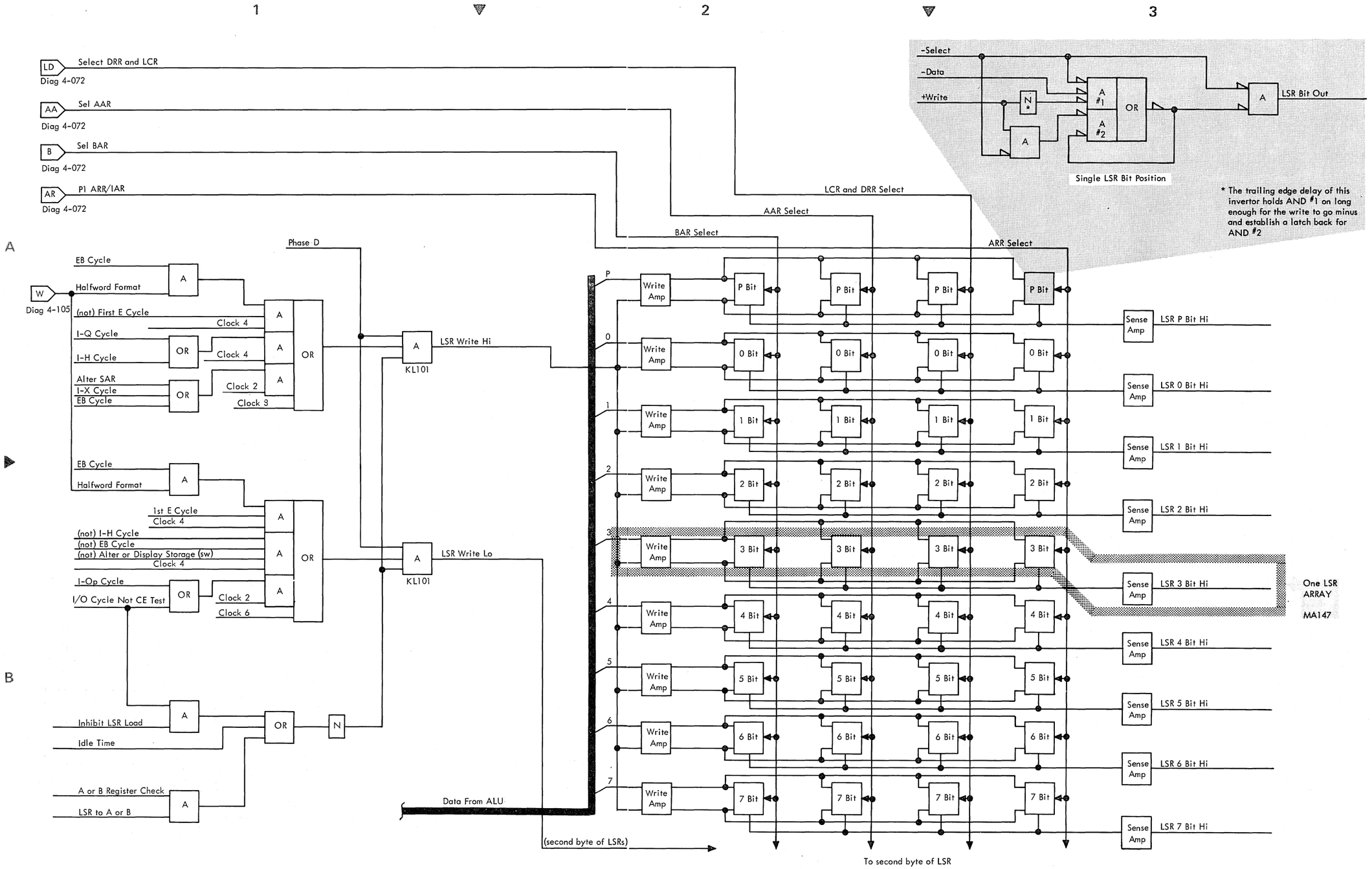

1
2
3
A
B
P
0
1
2
3
4
5
6
7
FL
KE101
(not) 6
(not) 5
(not) 4
3
(not) 2
KE111
OR
N
7
6
5
(not) 3
2
0
(not) 7
(not) 0
EVEN
DBI Parity Check
DBI
D
Diag 4-100
Load DBI
(even clock time)
T
Translate In
Diag 4-100
Translate In
Clock 2 and 3 to DBI
Data Bus In To A Register Then ALU
Diag 4-040
OE
Console Bit P
Console Bit 0
Console Bit 1
Console Bit 2
Console Bit 3
Console Bit 4
Console Bit 5
Console Bit 6
Console Bit 7
DBI Bit P
DBI Bit 0
DBI Bit 1
DBI Bit 2
DBI Bit 3
DBI Bit 4
DBI Bit 5
DBI Bit 6
DBI Bit 7
KE121

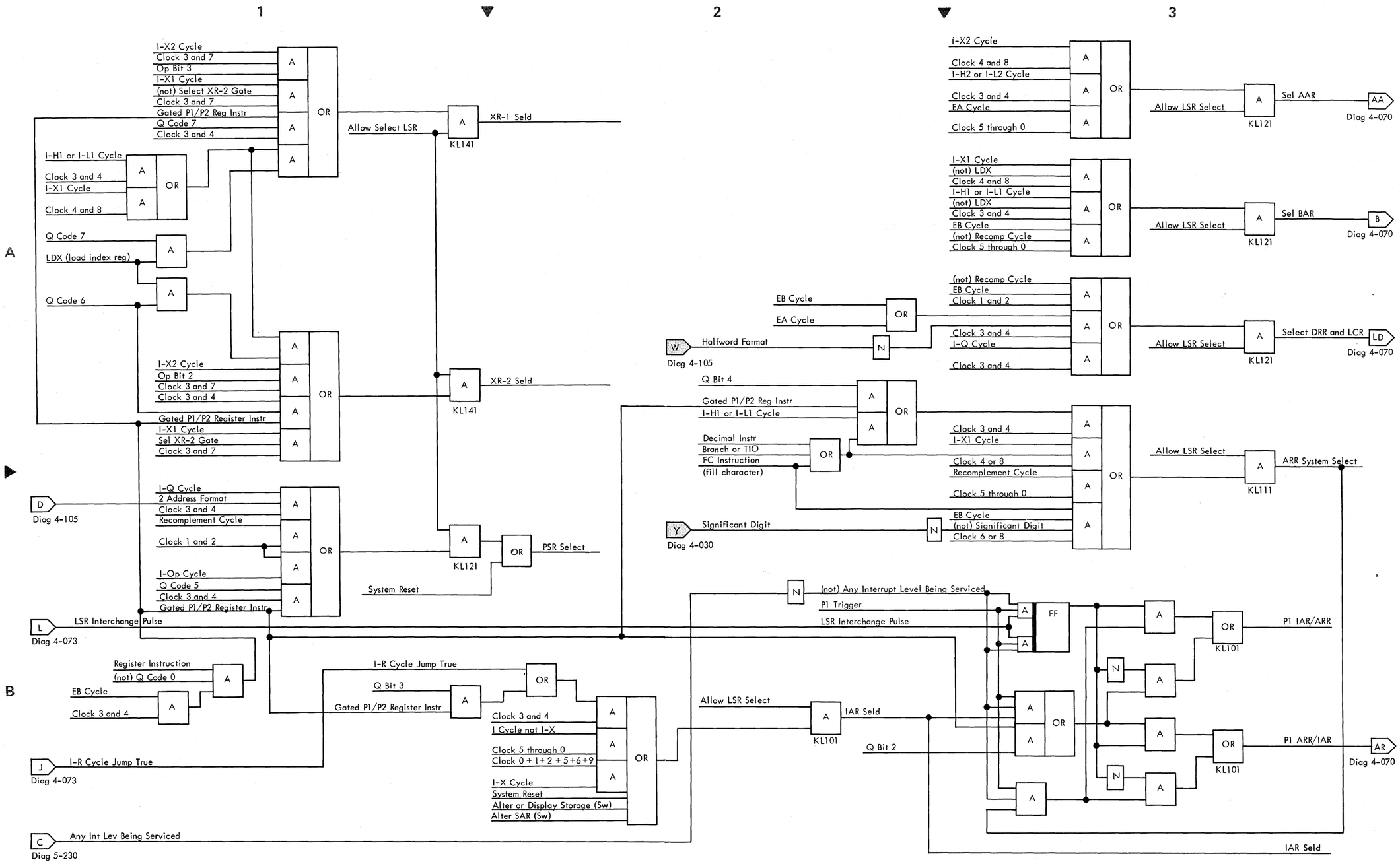


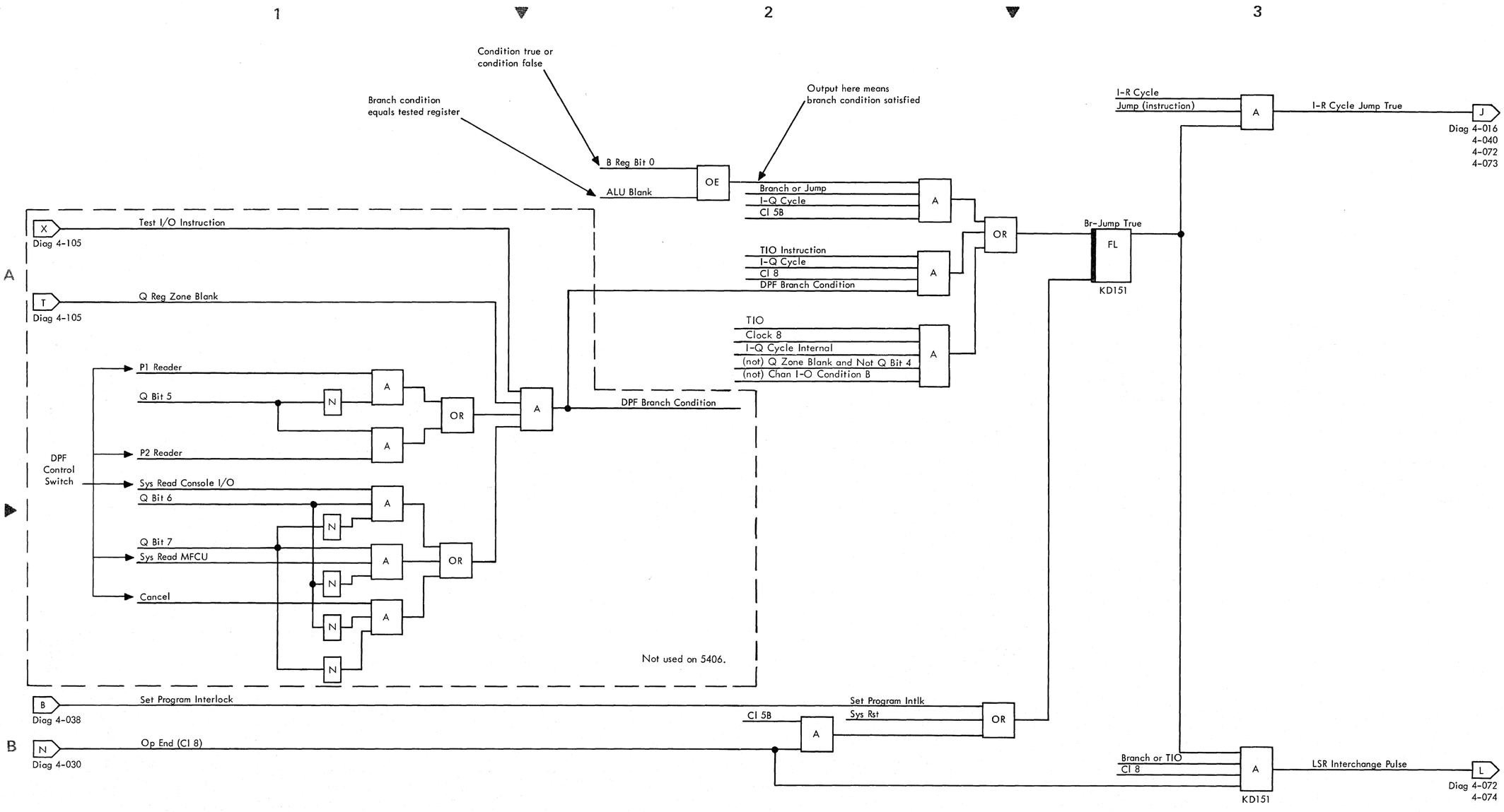
Priority Request	Cycle Steal Request Line	CPU Clock	Attachment	DBO Lines P01234567
1	3	6	Disk read/write	000010000
2			Spare	
3	5	6	Printer	000000100
4	6	6	SIOC	000000010
5			Spare	
6	3	4	BSCA	110010000
7-11			Spare	
12	4	2	Data Recorder	101001000
13	5	2	CRT Display	101000100
14-19			Spare	
20	7	0	Disk Control	100100001

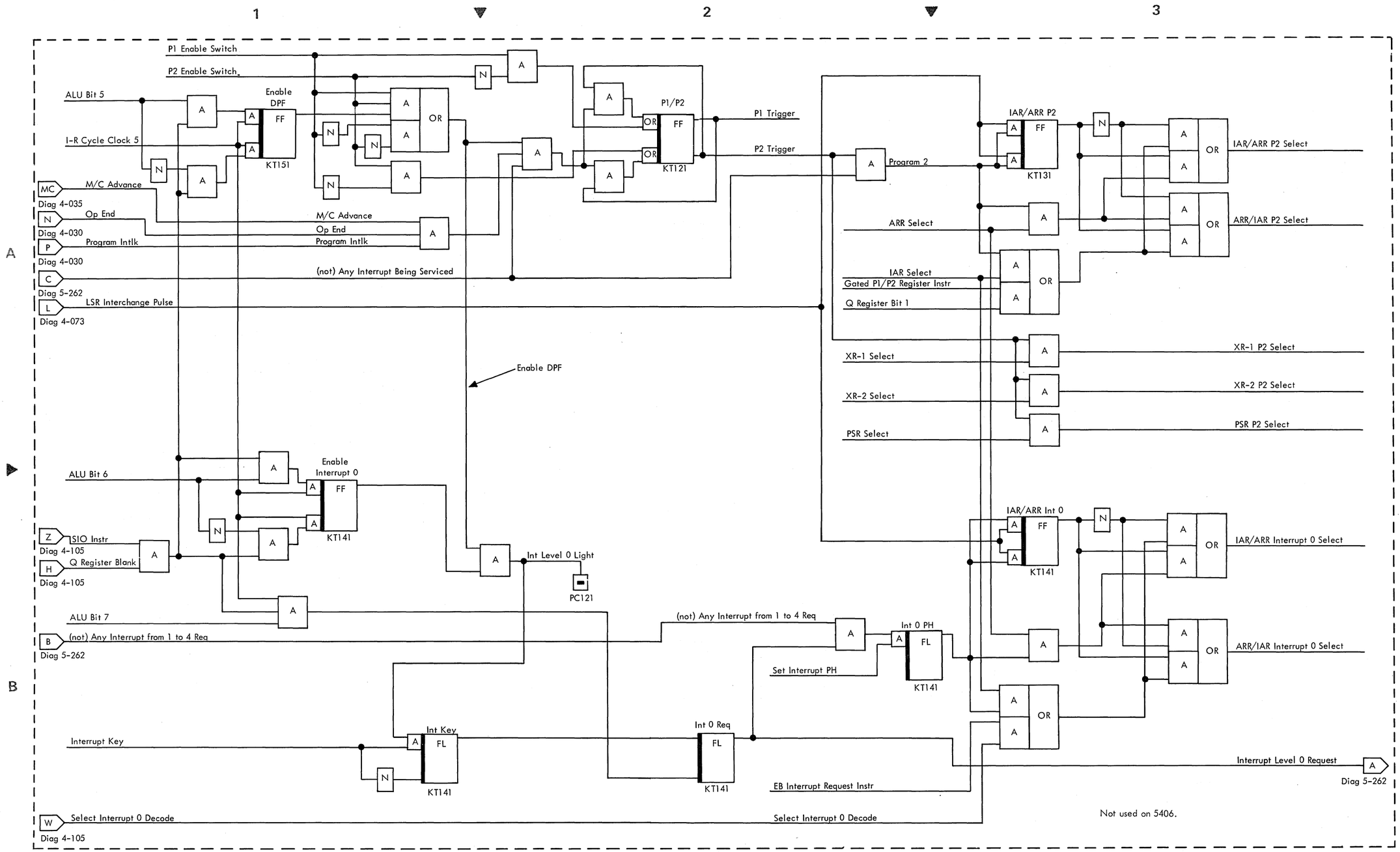
5406 CPU–Functional Units
Cycle Steal Request Priority Assignment

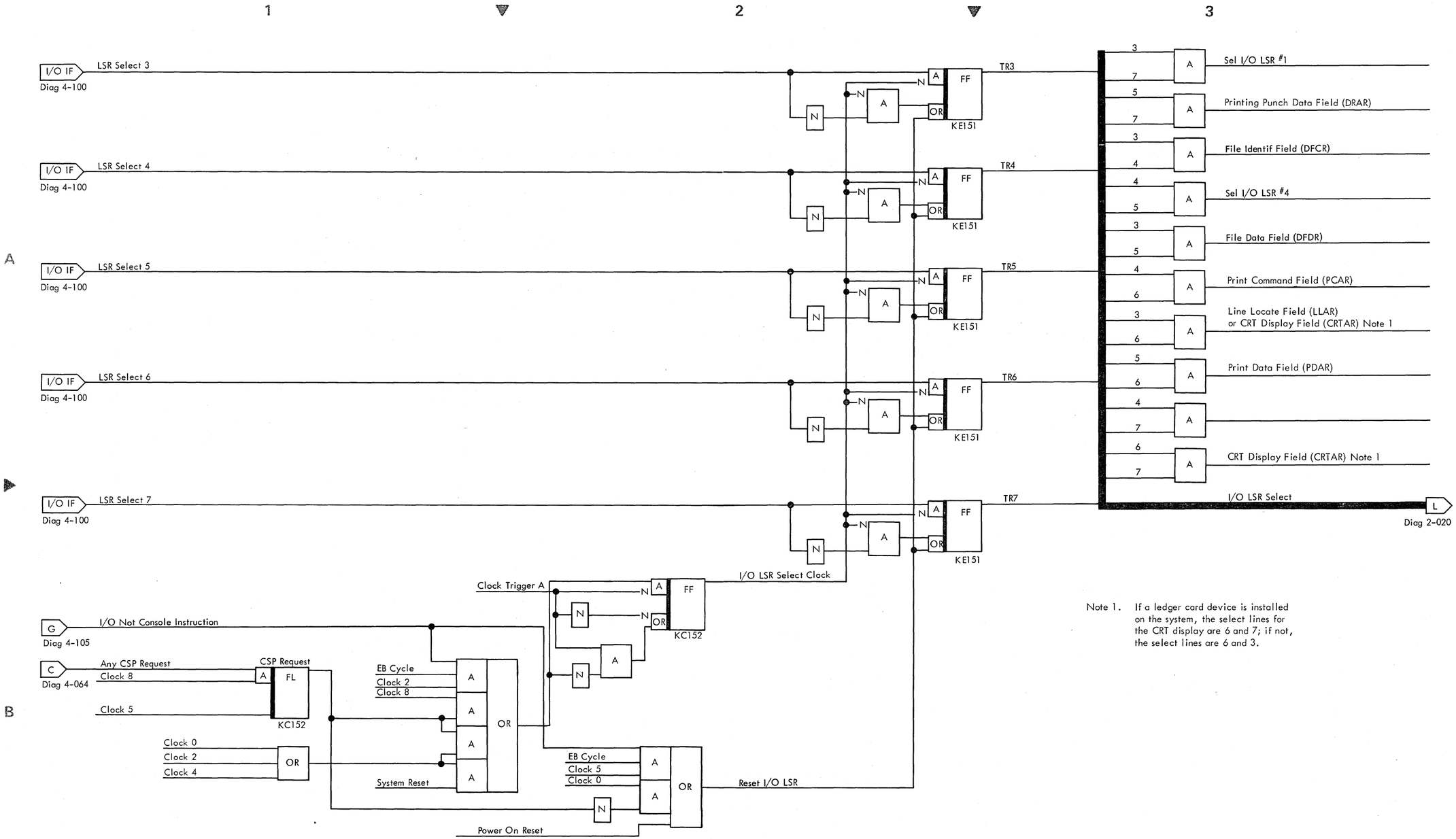

1
2
3
A
B
ALU Out (4-010)
ALU Out
(not) 7
(not) 6
(not) 5
(not) 4
(not) 3
2
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
KE231
KE241
KE241
KE251
A
N
OR
OE
P
0
1
2
3
4
5
6
7
Bit P
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
CPU to Card Translate Clock (Cl 4C to 6C)
S
Translate Out
Diag 4-100
DB
Diag 4-064
G
IPL
Diag 4-035
Cycle Steal Request (highest priority acknowledged)
Clock 7D to 0C
Data Bus Out
B
Diag 4-100
EVEN
DBO Parity
Check


1
2
3
LD
Select DRR and LCR
Diag 4-072
AA
Sel AAR
Diag 4-072
B
Sel BAR
Diag 4-072
AR
P1 ARR/IAR
Diag 4-072
LCR and DRR Select
AAR Select
BAR Select
ARR Select
Phase D
A
B
W
Diag 4-105
EB Cycle
Halfword Format
(not) First E Cycle
Clock 4
I-Q Cycle
I-H Cycle
Alter SAR
I-X Cycle
EB Cycle
Clock 2
Clock 3
1st E Cycle
(not) I-H Cycle
(not) EB Cycle
(not) Alter or Display Storage (sw)
I-Op Cycle
I/O Cycle Not CE Test
Clock 6
Inhibit LSR Load
Idle Time
A or B Register Check
LSR to A or B
KL101
LSR Write Hi
LSR Write Lo
Data From ALU
(second byte of LSRs)
To second byte of LSR
Write Amp
P Bit
0 Bit
1 Bit
2 Bit
3 Bit
4 Bit
5 Bit
6 Bit
7 Bit
Sense Amp
LSR P Bit Hi
LSR 0 Bit Hi
LSR 1 Bit Hi
LSR 2 Bit Hi
LSR 3 Bit Hi
LSR 4 Bit Hi
LSR 5 Bit Hi
LSR 6 Bit Hi
LSR 7 Bit Hi
One LSR ARRAY
MA147
-Select
-Data
+Write
LSR Bit Out
Single LSR Bit Position
* The trailing edge delay of this invertor holds AND #1 on long enough for the write to go minus and establish a latch back for AND #2

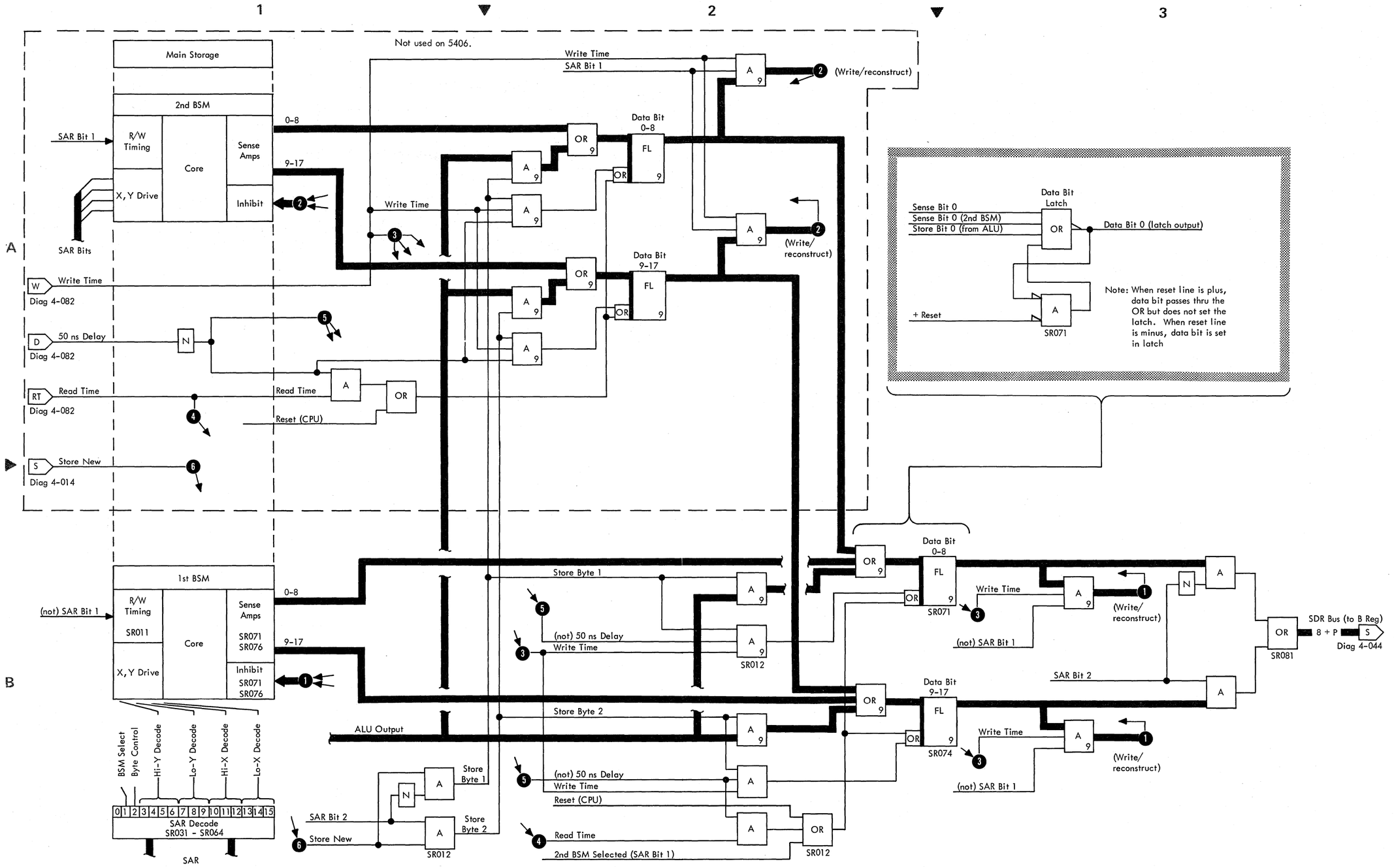

1
2
3
A
B
I-X2 Cycle
Clock 3 and 7
Op Bit 3
I-X1 Cycle
(not) Select XR-2 Gate
Clock 3 and 7
Gated P1/P2 Reg Instr
Q Code 7
Clock 3 and 4
OR
Allow Select LSR
XR-1 Seld
KL141
I-H1 or I-L1 Cycle
Clock 3 and 4
I-X1 Cycle
Clock 4 and 8
Q Code 7
LDX (load index reg)
Q Code 6
I-X2 Cycle
Op Bit 2
Clock 3 and 7
Clock 3 and 4
XR-2 Seld
Gated P1/P2 Register Instr
I-X1 Cycle
Sel XR-2 Gate
Clock 3 and 7
I-Q Cycle
2 Address Format
Clock 3 and 4
Recomplement Cycle
Clock 1 and 2
I-Op Cycle
Q Code 5
Clock 3 and 4
Gated P1/P2 Register Instr
KL121
PSR Select
System Reset
D
Diag 4-105
L
LSR Interchange Pulse
Diag 4-073
Register Instruction
(not) Q Code 0
EB Cycle
Clock 3 and 4
I-R Cycle Jump True
Q Bit 3
Gated P1/P2 Register Instr
Clock 3 and 4
I Cycle not I-X
Clock 5 through 0
Clock 0 + 1 + 2 + 5 + 6 + 9
I-X Cycle
System Reset
Alter or Display Storage (Sw)
Alter SAR (Sw)
J
I-R Cycle Jump True
Diag 4-073
C
Any Int Lev Being Serviced
Diag 5-230
i-X2 Cycle
Clock 4 and 8
I-H2 or I-L2 Cycle
Clock 3 and 4
EA Cycle
Clock 5 through 0
Allow LSR Select
Sel AAR
AA
Diag 4-070
I-X1 Cycle
(not) LDX
Clock 4 and 8
I-H1 or I-L1 Cycle
(not) LDX
Clock 3 and 4
EB Cycle
(not) Recomp Cycle
Clock 5 through 0
Sel BAR
B
(not) Recomp Cycle
EB Cycle
Clock 1 and 2
EA Cycle
Clock 3 and 4
I-Q Cycle
Halfword Format
W
Diag 4-105
Clock 3 and 4
Select DRR and LCR
LD
Q Bit 4
Gated P1/P2 Reg Instr
I-H1 or I-L1 Cycle
Decimal Instr
Branch or TIO
FC Instruction
(fill character)
Clock 3 and 4
I-X1 Cycle
Clock 4 or 8
Recomplement Cycle
Clock 5 through 0
Allow LSR Select
ARR System Select
KL111
Y
Significant Digit
Diag 4-030
EB Cycle
(not) Significant Digit
Clock 6 or 8
N
(not) Any Interrupt Level Being Serviced
P1 Trigger
LSR Interchange Pulse
FF
P1 IAR/ARR
KL101
Allow LSR Select
IAR Seld
Q Bit 2
P1 ARR/IAR
AR
Diag 4-070
IAR Seld


1
2
3
Condition true or condition false
Branch condition equals tested register
Output here means branch condition satisfied
B Reg Bit 0
ALU Blank
OE
Branch or Jump
I-Q Cycle
CI 5B
A
TIO Instruction
I-Q Cycle
CI 8
DPF Branch Condition
A
TIO
Clock 8
I-Q Cycle Internal
(not) Q Zone Blank and Not Q Bit 4
(not) Chan I-O Condition B
A
OR
Br-Jump True
FL
KD151
I-R Cycle
Jump (instruction)
A
I-R Cycle Jump True
J
Diag 4-016
4-040
4-072
4-073
A
X
Diag 4-105
Test I/O Instruction
T
Diag 4-105
Q Reg Zone Blank
P1 Reader
Q Bit 5
N
A
OR
A
DPF Branch Condition
P2 Reader
DPF Control Switch
Sys Read Console I/O
Q Bit 6
A
N
Q Bit 7
Sys Read MFCU
A
OR
N
Cancel
A
N
N
Not used on 5406.
B
Diag 4-038
Set Program Interlock
Set Program Intlk
Sys Rst
CI 5B
A
OR
B
N
Diag 4-030
Op End (CI 8)
Branch or TIO
CI 8
A
KD151
LSR Interchange Pulse
L
Diag 4-072
4-074

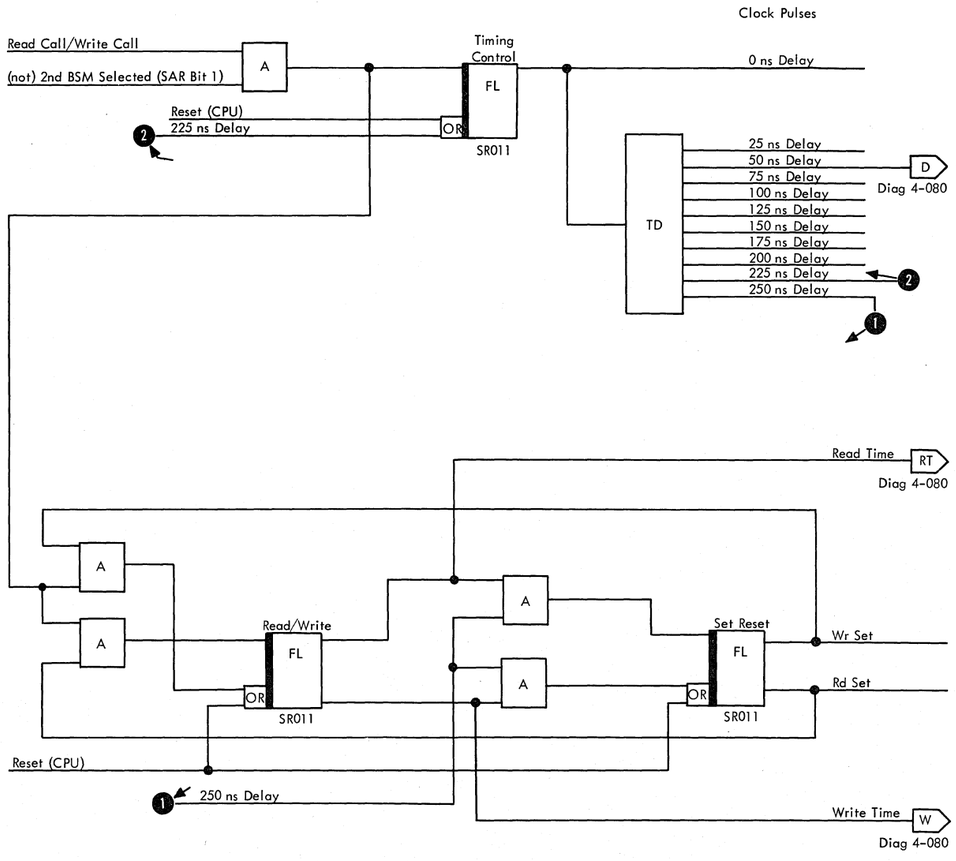

1
2
3
A
B
P1 Enable Switch
P2 Enable Switch
ALU Bit 5
I-R Cycle Clock 5
Enable DPF
FF
KT151
M/C Advance
Diag 4-035
Op End
Diag 4-030
Program Intlk
Diag 4-030
(not) Any Interrupt Being Serviced
LSR Interchange Pulse
Diag 5-262
Diag 4-073
P1/P2
OR
KT121
P1 Trigger
P2 Trigger
Program 2
IAR/ARR P2
KT131
IAR/ARR P2 Select
ARR Select
ARR/IAR P2 Select
IAR Select
Gated P1/P2 Register Instr
Q Register Bit 1
XR-1 Select
XR-1 P2 Select
XR-2 Select
XR-2 P2 Select
PSR Select
PSR P2 Select
Enable DPF
Enable Interrupt 0
ALU Bit 6
SIO Instr
Diag 4-105
Q Register Blank
Diag 4-105
KT141
Int Level 0 Light
PC121
IAR/ARR Int 0
IAR/ARR Interrupt 0 Select
ALU Bit 7
(not) Any Interrupt from 1 to 4 Req
Diag 5-262
Int 0 PH
FL
Set Interrupt PH
ARR/IAR Interrupt 0 Select
Int Key
Interrupt Key
Int 0 Req
EB Interrupt Request Instr
Interrupt Level 0 Request
Diag 5-262
Select Interrupt 0 Decode
Diag 4-105
Not used on 5406.



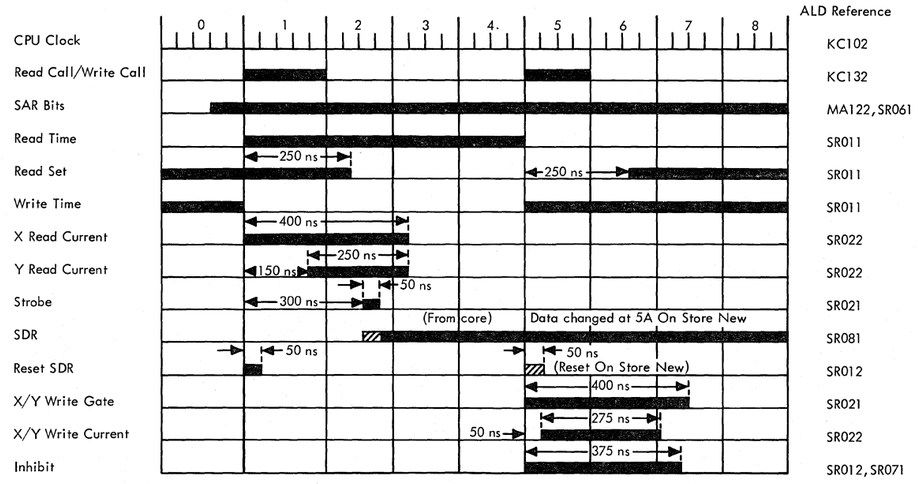
Note 1. If a ledger card device is installed on the system, the select lines for the CRT display are 6 and 7; if not, the select lines are 6 and 3.


1
2
3
A
B
Main Storage
2nd BSM
SAR Bit 1
R/W Timing
Core
Sense Amps
X, Y Drive
Inhibit
SAR Bits
0-8
9-17
Not used on 5406.
Write Time
SAR Bit 1
(Write/reconstruct)
Data Bit 0-8
Data Bit 9-17
FL
OR
A
N
W Write Time
Diag 4-082
D 50 ns Delay
Diag 4-082
RT Read Time
Diag 4-082
Read Time
Reset (CPU)
S Store New
Diag 4-014
1st BSM
(not) SAR Bit 1
SR011
SR071 SR076
Store Byte 1
Store Byte 2
ALU Output
(not) 50 ns Delay
Write Time
Reset (CPU)
Read Time
2nd BSM Selected (SAR Bit 1)
SR012
SR071
SR074
SR081
(not) SAR Bit 1
SAR Bit 2
Store New
Store Byte 1
Store Byte 2
(Write/ reconstruct)
SDR Bus (to B Reg)
8 + P
Diag 4-044
BSM Select
Byte Control
Hi-Y Decode
Lo-Y Decode
Hi-X Decode
Lo-X Decode
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
SAR Decode
SR031 – SR064
SAR
Data Bit Latch
Sense Bit 0
Sense Bit 0 (2nd BSM)
Store Bit 0 (from ALU)
Data Bit 0 (latch output)
+ Reset
SR071
Note: When reset line is plus, data bit passes thru the OR but does not set the latch. When reset line is minus, data bit is set in latch

A


Clock Pulses
Read Call/Write Call
(not) 2nd BSM Selected (SAR Bit 1)
A
Timing Control
FL
OR
SR011
0 ns Delay
Reset (CPU)
225 ns Delay
25 ns Delay
50 ns Delay
75 ns Delay
100 ns Delay
125 ns Delay
150 ns Delay
175 ns Delay
200 ns Delay
225 ns Delay
250 ns Delay
TD
D
Diag 4-080
Read Time
RT
Diag 4-080
Read/Write
Set Reset
Wr Set
Rd Set
Reset (CPU)
250 ns Delay
Write Time
W
Diag 4-080

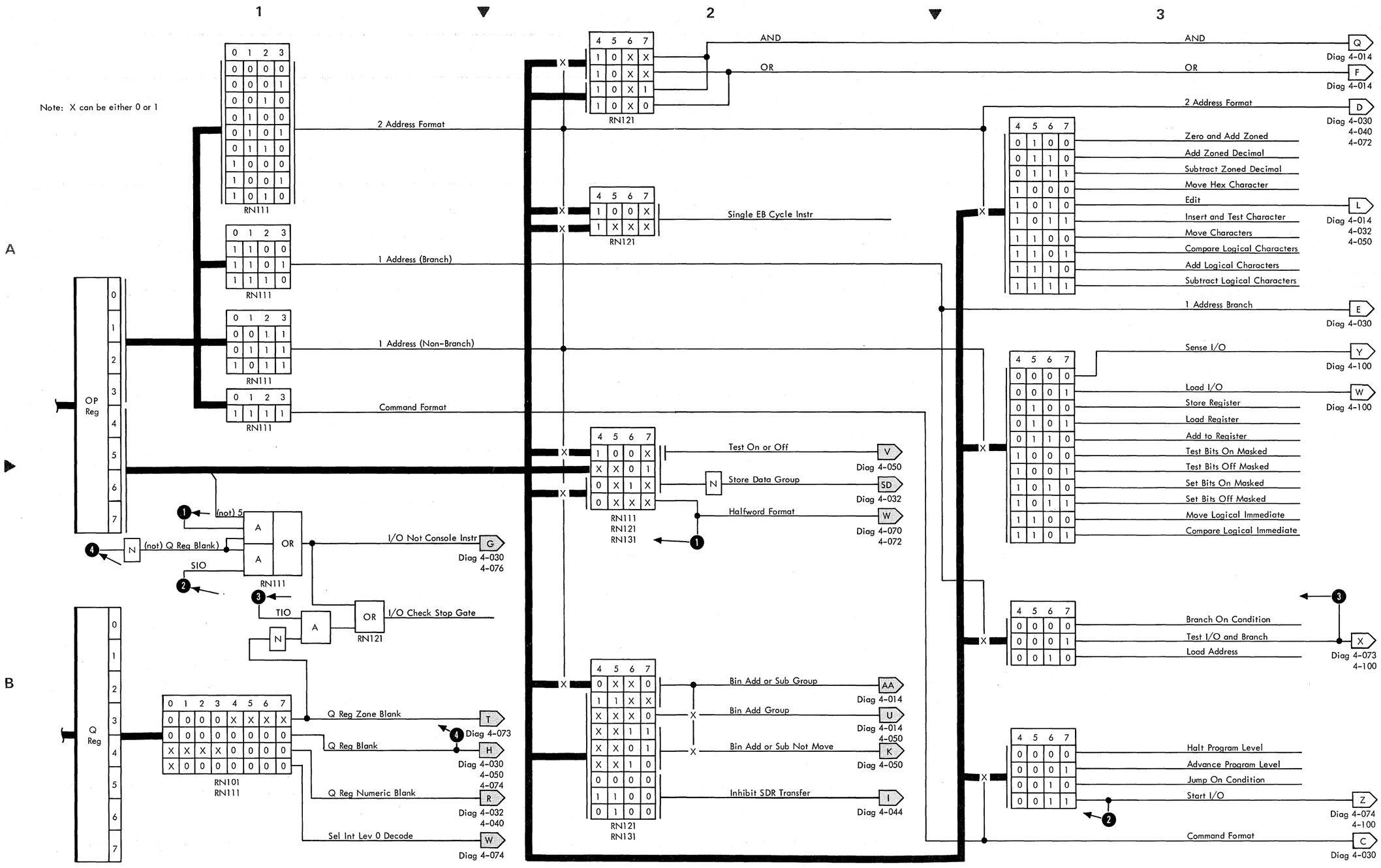
B


ALD Reference
CPU Clock
KC102
Read Call/Write Call
KC132
SAR Bits
MA122, SR061
Read Time
SR011
Read Set
SR011
Write Time
SR011
X Read Current
SR022
Y Read Current
SR022
Strobe
SR021
SDR
SR081
Reset SDR
SR012
X/Y Write Gate
SR021
X/Y Write Current
SR022
Inhibit
SR012, SR071
250 ns
400 ns
150 ns
50 ns
300 ns
(From core)
Data changed at 5A On Store New
(Reset On Store New)
275 ns
375 ns

1 2 3

I/O IF	Chan 1 Data Bus In	DBI	D	Diag 4-060
B Diag 4-100	Data Bus Out	Chan 1 Data Bus Out	I/O IF	
I/O IF	Chan I/O Check	Chan I/O Check	C	Diag 2-010
I/O IF	Chan 1 I/O Condition A	I/O Condition A	I	Diag 2-140 2-150
I/O IF	Chan 1 I/O Condition B	I/O Condition B	F	Diag 2-140 2-150 4-030 4-035
I/O IF	Chan LSR Select Bit 3-7	I/O LSR Select 3-7	L	Diag 2-020 4-076
I/O IF	Chan Translate In	Translate In	T	Diag 4-100
I/O IF	Chan Translate Out	Translate Out	S	Diag 4-065
I/O IF	Chan Binary Subtract	Chan Binary Subtract	R	Diag 4-014
I/O IF	Chan Store Data	Chan Store Data	SD	Diag 4-032
I/O IF	Chan Block SDR to B	Chan Block SDR	V	Diag 4-044
I/O IF	Channel CS Priority Bit	Chan CSR 3-7	Q	Diag 4-064
W Diag 4-105	LIO Instr	LIO Instr	I/O IF	
X Diag 4-105	TIO Instr	TIO Instr	I/O IF	
Y Diag 4-105	SNS Instr	SNS Instr	I/O IF	
Z Diag 4-105	SIO Instr	SIO Instr	I/O IF	

Note: Some of these lines may be referred to as 'Chan 2'.


1
2
3
Note: X can be either 0 or 1
A
B
OP Reg
Q Reg
RN111
RN121
RN101
RN131
2 Address Format
1 Address (Branch)
1 Address (Non-Branch)
Command Format
(not) 5
(not) Q Reg Blank
SIO
TIO
I/O Not Console Instr
I/O Check Stop Gate
Q Reg Zone Blank
Q Reg Blank
Q Reg Numeric Blank
Sel Int Lev 0 Decode
Diag 4-073
Diag 4-030 4-050 4-074
Diag 4-032 4-040
Diag 4-074
Diag 4-030 4-076
AND
OR
Single EB Cycle Instr
Test On or Off
Store Data Group
Halfword Format
Diag 4-050
Diag 4-032
Diag 4-070 4-072
Bin Add or Sub Group
Bin Add Group
Bin Add or Sub Not Move
Inhibit SDR Transfer
Diag 4-014
Diag 4-050
Diag 4-044
Diag 4-014
Diag 4-030
Diag 4-014 4-032 4-050
Diag 4-100
Diag 4-073 4-100
Diag 4-074 4-100
Diag 4-030
Zero and Add Zoned
Add Zoned Decimal
Subtract Zoned Decimal
Move Hex Character
Edit
Insert and Test Character
Move Characters
Compare Logical Characters
Add Logical Characters
Subtract Logical Characters
Load I/O
Store Register
Load Register
Add to Register
Test Bits On Masked
Test Bits Off Masked
Set Bits On Masked
Set Bits Off Masked
Move Logical Immediate
Compare Logical Immediate
Branch On Condition
Test I/O and Branch
Load Address
Halt Program Level
Advance Program Level
Jump On Condition
Start I/O

1 2 3

DIAGRAM	INSTRUCTIONS		OP BITS 0 1 2 3 4 5 6 7	ALD REFERENCE	SIGNAL NAME	AND	OR	STORE DATA GRP	BIN ADD OR SUB GRP	BIN ADD GROUP	BIN ADD/SUB NOT MOVE	INH SDR X-FER	SINGLE EB CY INST	I/O NOT CONSL INST	I/O CHK STOP GATE	TIO INST (ADV OR TIO)	BR OR SKIP	HALT	ADVANCE	SKIP	SIO INST	BR OR TIO INST	1 ADDRESS BRANCH	TEST I/O	LDX INST (LOAD INDEX REG)	HALFWORD FORM	SET OR TEST OFF	TEST ON OR OFF	REGISTER INSTR	ADD TO REG OR STORE INST	SENSE I/O INST	CHAN LOAD I/O INST	LOAD REG INST	LOAD CR	EDIT INSTR	FILL CHARAC INST	MOVE ZONE	MOVE NUM	ZONE NUM INTCHG	DECIMAL INSTR
														(Q REG NOT BLK)	(Q REG NOT BLK)																									
5-100	Zero and Add Zoned	ZAZ	X 0100	KY101				X				X																											X
5-100	Add Zoned Decimal	AZ	X 0110	KY101				X																														X
5-100	Subtract Zoned Decimal	SZ	X 0111	RN131				X																														X
5-070	Move Hex Character	MVX	X 1000	RN131	X	X	X						X																						✳ ($\overline{Q6}$)	✳ (Q6)	✳ (Q6 + Q7)	
5-110	Edit	ED	X 1010	RN131	X	X	X																												X				
5-120	Insert & Test Characters	ITC	X 1011	RN131	X	X	X																													X			
5-080	Move Characters	MVC	X 1100	RN131			X	X	X		X																												
5-080	Compare Logical Character	CLC	X 1101	RN131				X		X																													
5-080	Add Logical Character	ALC	X 1110	RN131			X	X	X	X																													
▶ 5-080	Subtract Logical Character	SLC	X 1111	RN131			X	X		X																													
5-170	Sense I/O	SNS	Y 0000	RN131			X	X	X		X		✳	✳																				X					
5-160	Load I/O	LIO	Y 0001	RN131									✳	✳																				X					
5-060	Store Register	ST	Y 0100	RN131			X	X	X		X																							X					
5-060	Load Register	L	Y 0101	RN131																														X					
5-060	Add to Register	A	Y 0110	RN131			X	X	X																									X					
5-050	Test Bits On Masked	TBN	Y 1000	RN131		X						X																						X					
5-050	Test Bits Off Masked	TBF	Y 1001	RN131	X							X																						X					
5-050	Set Bits On Masked	SBN	Y 1010	RN131		X	X					X																						X					
5-050	Set Bits Off Masked	SBF	Y 1011	RN131	X		X					X																						X					
B 5-090	Move Logical Immediate	MVI	Y 1100	RN131			X	X	X		X	X																											
5-090	Compare Logic Immediate	CLI	Y 1101	RN131				X		X		X																											
5-130	Branch On Condition	BC	Z 0000	RN131			⊗				⊗					X									X	X													
5-180	Test I/O and Branch	TIO	Z 0001	RN131											✳	X										X		X											
5-190	Load Address	LA	Z 0010	RN131			⊗																																
5-210	Halt Program Level	HPL	F 0000	RN131			⊗				⊗							X																					
5-200	Advance Prog Level	APL	F 0001	RN131												X			X																				
5-140	Jump On Condition	JC	F 0010	RN131			⊗										X			X																			
5-150	Start I/O	SIO	F 0011	RN131			⊗								✳	✳					X																		

Notes: ✳ Conditioned by Q Reg Bits

⊗ Line developed but not used in this operation

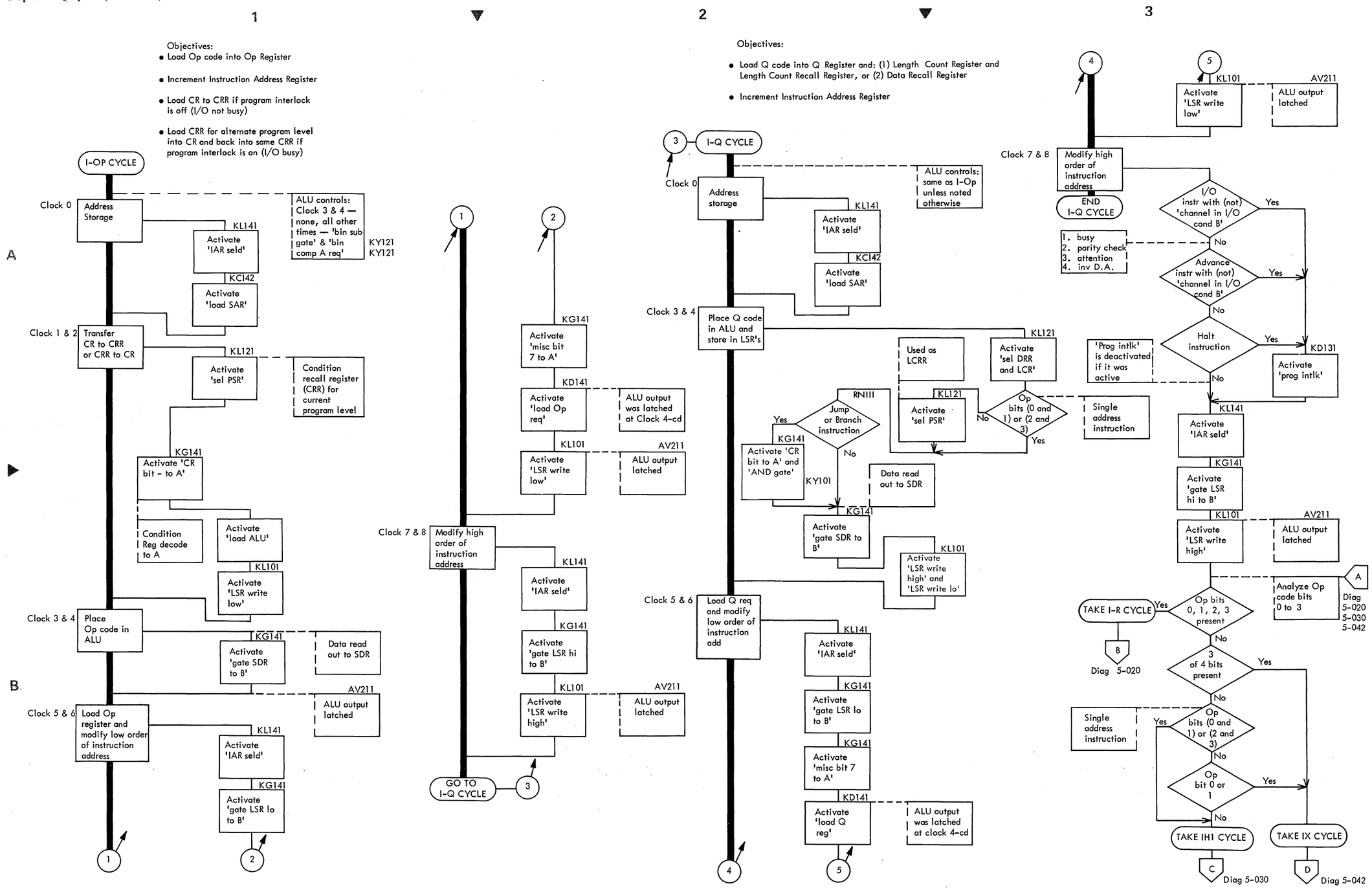
OP BITS 0123

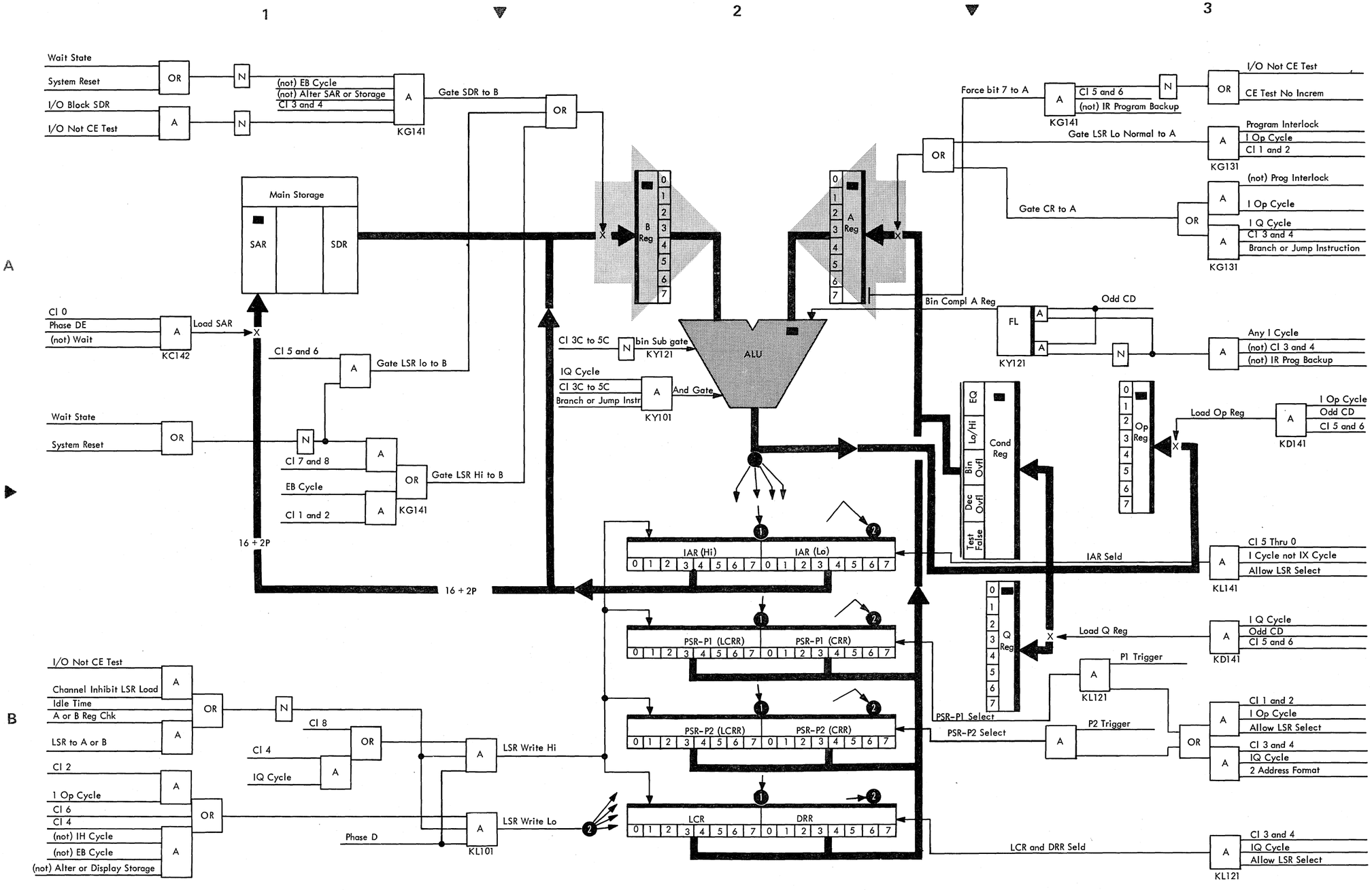
X 2 address instruction (can be indexed by bits 0-3)

Y 1 address instruction (can be indexed by bits 0 and 1)

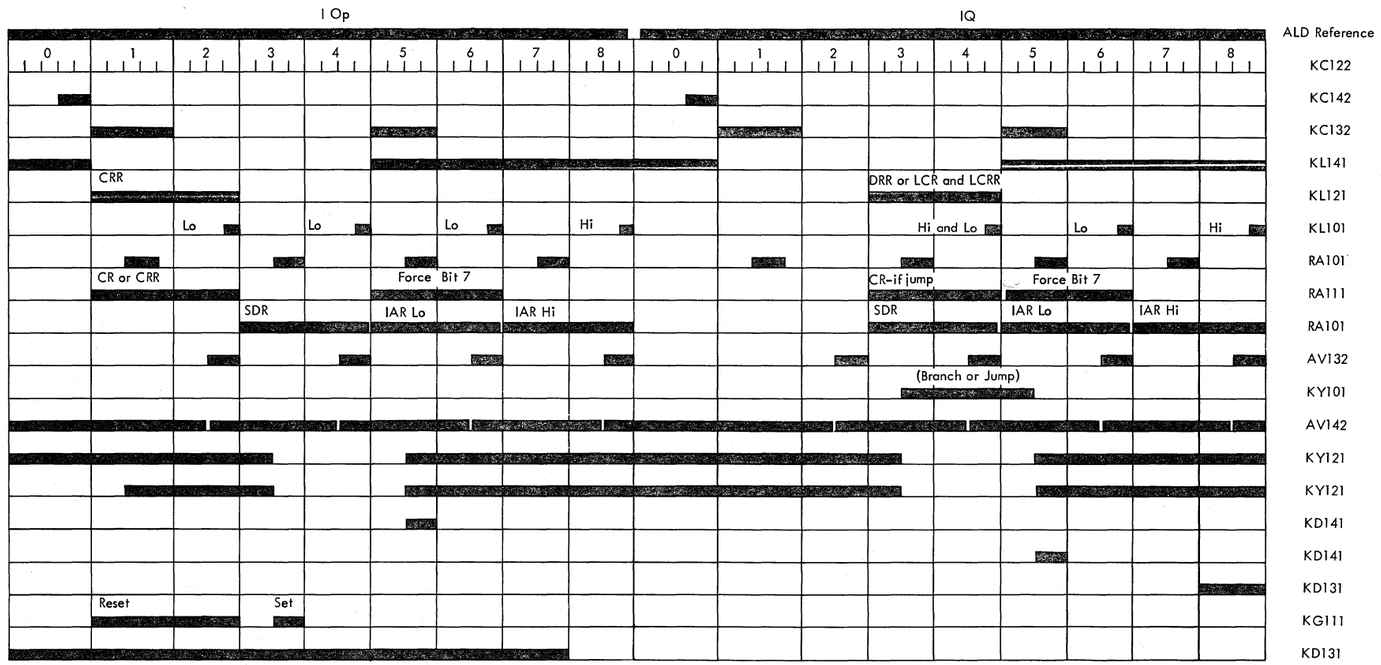
Z 1 address instruction (can be indexed by bits 2 and 3)

F Command instruction


1
Objectives:
• Load Op code into Op Register
• Increment Instruction Address Register
• Load CR to CRR if program interlock is off (I/O not busy)
• Load CRR for alternate program level into CR and back into same CRR if program interlock is on (I/O busy)
I-OP CYCLE
Clock 0
Address Storage
ALU controls: Clock 3 & 4 — none, all other times — 'bin sub gate' & 'bin comp A req'
KY121
KY121
KL141
Activate 'IAR seld'
KCI42
Activate 'load SAR'
A
Clock 1 & 2
Transfer CR to CRR or CRR to CR
KL121
Activate 'sel PSR'
Condition recall register (CRR) for current program level
KG141
Activate 'CR bit - to A'
Condition Reg decode to A
Activate 'load ALU'
KL101
Activate 'LSR write low'
Clock 3 & 4
Place Op code in ALU
KG141
Activate 'gate SDR to B'
Data read out to SDR
B
AV211
ALU output latched
Clock 5 & 6
Load Op register and modify low order of instruction address
KL141
Activate 'IAR seld'
KG141
Activate 'gate LSR lo to B'
1
2
2
KG141
Activate 'misc bit 7 to A'
KD141
Activate 'load Op req'
ALU output was latched at Clock 4-cd
KL101
Activate 'LSR write low'
AV211
ALU output latched
Clock 7 & 8
Modify high order of instruction address
KL141
Activate 'IAR seld'
KG141
Activate 'gate LSR hi to B'
KL101
Activate 'LSR write high'
AV211
ALU output latched
GO TO I-Q CYCLE
3
2
Objectives:
• Load Q code into Q Register and: (1) Length Count Register and Length Count Recall Register, or (2) Data Recall Register
• Increment Instruction Address Register
3
I-Q CYCLE
Clock 0
Address storage
ALU controls: same as I-Op unless noted otherwise
KL141
Activate 'IAR seld'
KCI42
Activate 'load SAR'
Clock 3 & 4
Place Q code in ALU and store in LSR's
KL121
Activate 'sel DRR and LCR'
Used as LCRR
KL121
Activate 'sel PSR'
RNIII
Jump or Branch instruction
Yes
No
KG141
Activate 'CR bit to A' and 'AND gate'
KY101
Data read out to SDR
KG141
Activate 'gate SDR to B'
KL101
Activate 'LSR write high' and 'LSR write lo'
Op bits (0 and 1) or (2 and 3)
No
Yes
Single address instruction
Clock 5 & 6
Load Q req and modify low order of instruction add
KL141
Activate 'IAR seld'
KG141
Activate 'gate LSR lo to B'
KG141
Activate 'misc bit 7 to A'
KD141
Activate 'load Q reg'
ALU output was latched at clock 4-cd
4
5
4
5
KL101
Activate 'LSR write low'
AV211
ALU output latched
Clock 7 & 8
Modify high order of instruction address
END I-Q CYCLE
1. busy
2. parity check
3. attention
4. inv D.A.
I/O instr with (not) 'channel in I/O cond B'
Yes
No
Advance instr with (not) 'channel in I/O cond B'
Yes
No
Halt instruction
Yes
No
'Prog intlk' is deactivated if it was active
KD131
Activate 'prog intlk'
KL141
Activate 'IAR seld'
KG141
Activate 'gate LSR hi to B'
KL101
Activate 'LSR write high'
AV211
ALU output latched
A
Analyze Op code bits 0 to 3
Diag 5-020 5-030 5-042
TAKE I-R CYCLE
Yes
Op bits 0, 1, 2, 3 present
No
B
Diag 5-020
3 of 4 bits present
Yes
No
Single address instruction
Yes
Op bits (0 and 1) or (2 and 3)
No
Op bit 0 or 1
Yes
No
TAKE IH1 CYCLE
TAKE IX CYCLE
C
Diag 5-030
D
Diag 5-042


1
2
3
A
B
Wait State
System Reset
I/O Block SDR
I/O Not CE Test
OR
N
A
(not) EB Cycle
(not) Alter SAR or Storage
Cl 3 and 4
KG141
Gate SDR to B
Main Storage
SAR
SDR
Cl 0
Phase DE
(not) Wait
KC142
Load SAR
Cl 5 and 6
Gate LSR lo to B
Cl 7 and 8
EB Cycle
Cl 1 and 2
Gate LSR Hi to B
16 + 2P
B Reg
A Reg
ALU
Cl 3C to 5C
bin Sub gate
KY121
IQ Cycle
Branch or Jump Instr
And Gate
KY101
Force bit 7 to A
Cl 5 and 6
(not) IR Program Backup
Gate LSR Lo Normal to A
Gate CR to A
I/O Not CE Test
CE Test No Increm
Program Interlock
I Op Cycle
Cl 1 and 2
KG131
(not) Prog Interlock
I Op Cycle
I Q Cycle
Cl 3 and 4
Branch or Jump Instruction
Bin Compl A Reg
FL
Odd CD
Any I Cycle
(not) Cl 3 and 4
(not) IR Prog Backup
EQ
Lo/Hi
Bin Ovfl
Dec Ovfl
Test False
Cond Reg
Op Reg
Load Op Reg
I Op Cycle
Odd CD
Cl 5 and 6
KD141
IAR (Hi)
IAR (Lo)
IAR Seld
Cl 5 Thru 0
I Cycle not IX Cycle
Allow LSR Select
KL141
Q Reg
Load Q Reg
I Q Cycle
Odd CD
Cl 5 and 6
P1 Trigger
KL121
PSR-P1 (LCRR)
PSR-P1 (CRR)
PSR-P1 Select
PSR-P2 (LCRR)
PSR-P2 (CRR)
PSR-P2 Select
P2 Trigger
Cl 1 and 2
I Op Cycle
Allow LSR Select
Cl 3 and 4
IQ Cycle
2 Address Format
I/O Not CE Test
Channel Inhibit LSR Load
Idle Time
A or B Reg Chk
LSR to A or B
Cl 2
1 Op Cycle
Cl 6
Cl 4
(not) IH Cycle
(not) EB Cycle
(not) Alter or Display Storage
Cl 8
Cl 4
IQ Cycle
LSR Write Hi
LSR Write Lo
Phase D
KL101
LCR
DRR
LCR and DRR Seld
Cl 3 and 4
IQ Cycle
Allow LSR Select
KL121

1 2 3


I Op
IQ
Cycle
Clock
0 1 2 3 4 5 6 7 8 0 1 2 3 4 5 6 7 8
ALD Reference
Load SAR KC122
Read Call/Write Call KC142
IAR Select KC132
LSR Select KL141
LSR Load KL121
Load A and B Reg KL101
A Reg Input RA101
B Reg Input RA111
Load ALU RA101
ALU Control (and) AV132
ALU Output KY101
Bin Sub Gate AV142
Bin Compl A Reg KY121
Load Op Reg KY121
Load Q Reg KD141
Set/Reset Prog Intlk KD141
Condition Reg KD131
Op End KG111
KD131
CRR
DRR or LCR and LCRR
Lo
Lo
Lo
Hi
Hi and Lo
Lo
Hi
CR or CRR
Force Bit 7
CR-if jump
Force Bit 7
SDR
IAR Lo
IAR Hi
SDR
IAR Lo
IAR Hi
(Branch or Jump)
Reset
Set

A

B

1

Objectives:

- Execute command instruction, unless program interlocked
- Increment or decrement Instruction Address Register

Diag. 5-010 B

I-R CYCLE

clock 0 — Address storage

A

Refer to Diagram 5-010 Point A to determine which type of cycle to take after I-Q cycle

Activate 'IAR seld' KL141

Activate 'load SAR' KC142

clock 3 & 4 — Add to address in IAR for Jump instruction with condition satisfied

Data read out to SDR

Activate 'gate SDR to B' KG141

Jump instruction with condition satisfied (Diagram 5-022 9-A)

No → 2

Yes

B

Activate 'gate LSR lo normal to A' KG131

1

3

2

1

3

Activate 'bin comp A reg' and 'bin sub gate' KY121 KY121

Activate 'IAR seld' KL141

2

Activate 'LSR write low' KL101 — ALU output latched AV211

clock 5 & 6 — Increment or decrement low order of instruction address

Activate 'IAR seld' KL141

Activate 'gate LSR lo to B' KG141

'Prog intlk' KD131

Yes → Activate 'IR program backup' KD151

No

Activate 'misc bit 7 to A' KG141

Activate 'bin comp A reg' KY121

Activate 'misc bit 6 to A' KG141

Activate 'bin sub gate' KY121

Activate 'LSR write low' KL101 — ALU output latched AV211

clock 7 & 8 — Increment or decrement high order of instruction address

Activate 'IAR seld KL141

Activate 'gate LSR hi to B' KG141

5

4

3

5

4

Activate 'bin sub gate' KY121

'Prog intlk' KD131

Yes

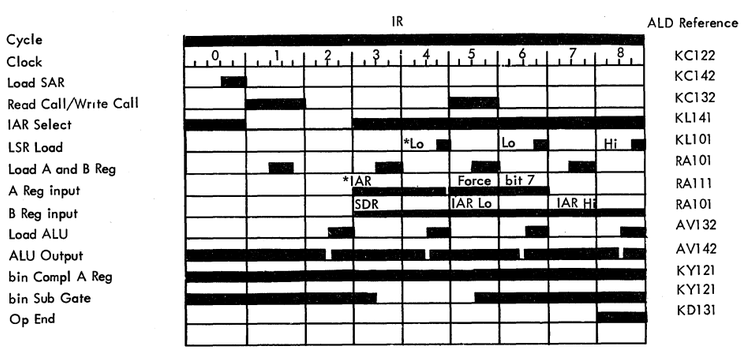
No

Activate 'bin comp A reg' KY121

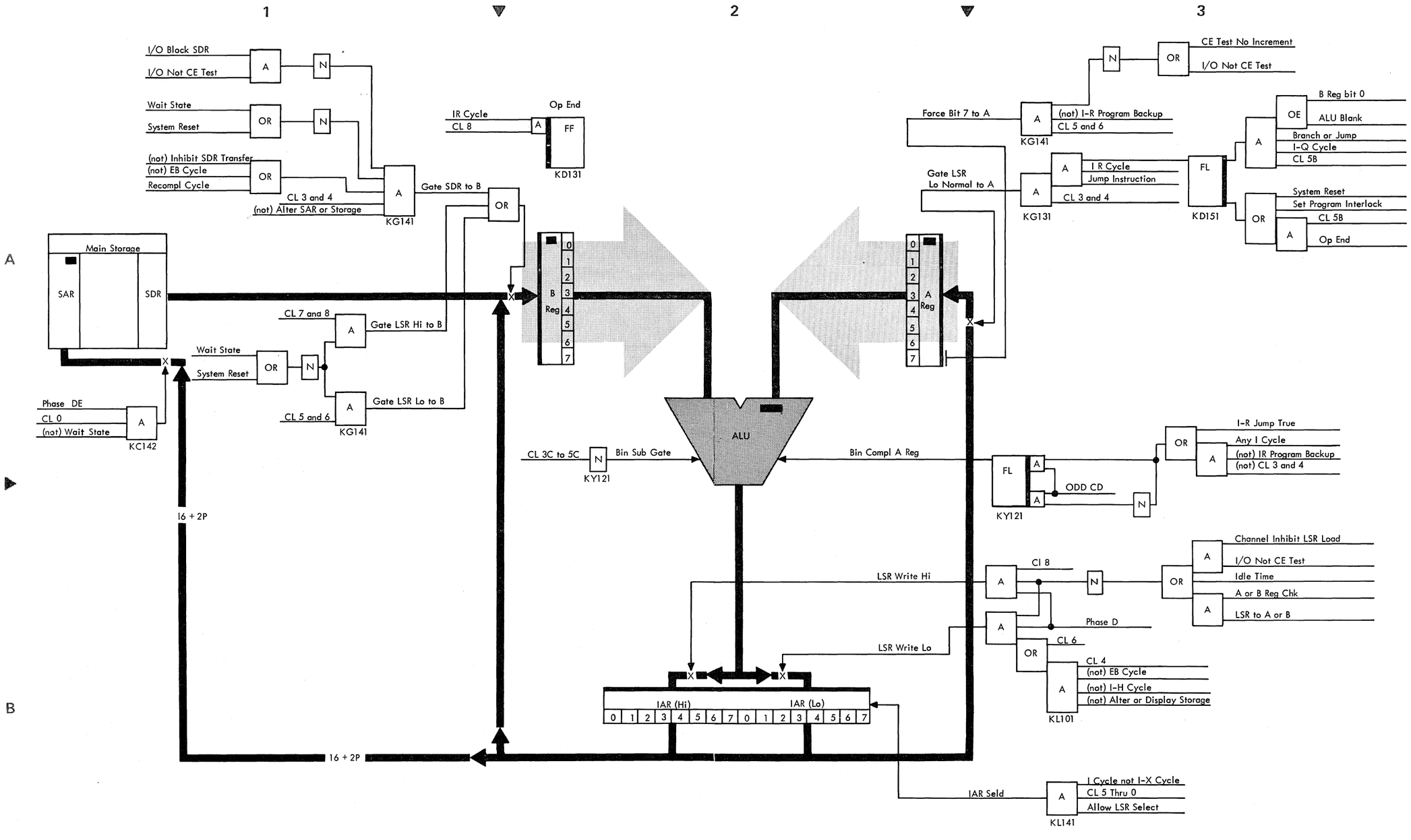
Turn on 'Op end' trigger KD131

Activate 'LSR write high' KL101 — ALU Output latched AV211

END OF OPERATION



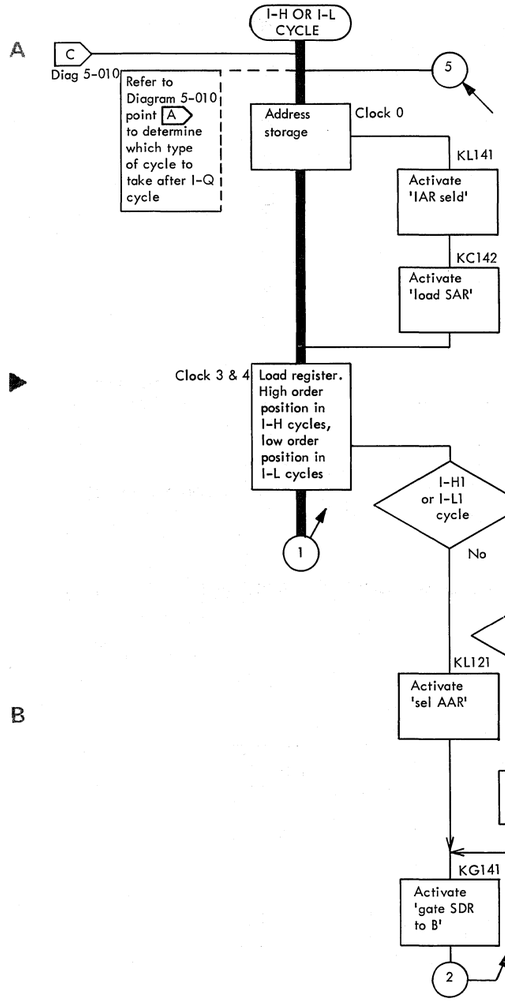
* Jump Instruction only

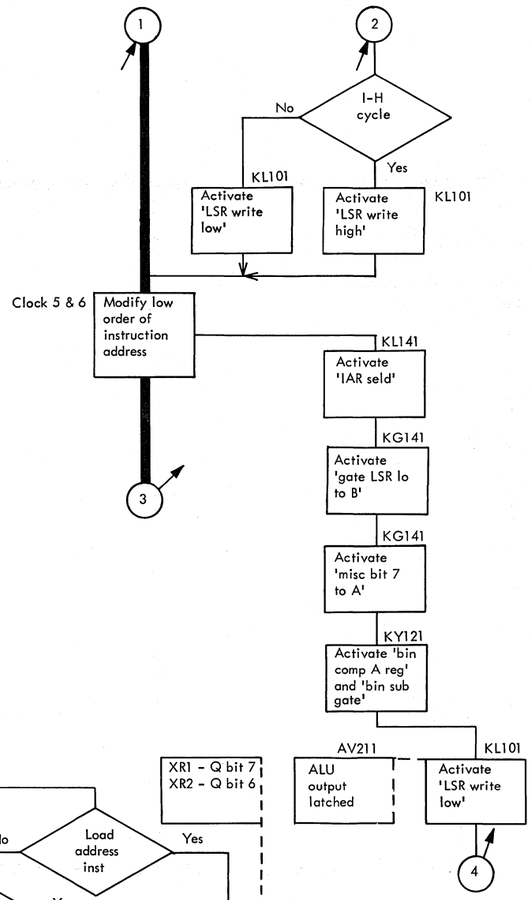

1
2
3
A
B
I/O Block SDR
I/O Not CE Test
Wait State
System Reset
(not) Inhibit SDR Transfer
(not) EB Cycle
Recompl Cycle
CL 3 and 4
(not) Alter SAR or Storage
KG141
Gate SDR to B
IR Cycle
CL 8
Op End
FF
KD131
Main Storage
SAR
SDR
B Reg
CL 7 and 8
Gate LSR Hi to B
Wait State
System Reset
Gate LSR Lo to B
CL 5 and 6
KG141
Phase DE
CL 0
(not) Wait State
KC142
16 + 2P
CL 3C to 5C
KY121
Bin Sub Gate
ALU
Bin Compl A Reg
A Reg
Force Bit 7 to A
Gate LSR
Lo Normal to A
CE Test No Increment
I/O Not CE Test
(not) I-R Program Backup
CL 5 and 6
KG141
I R Cycle
Jump Instruction
CL 3 and 4
KG131
FL
KD151
B Reg bit 0
ALU Blank
Branch or Jump
I-Q Cycle
CL 5B
System Reset
Set Program Interlock
CL 5B
Op End
I-R Jump True
Any I Cycle
(not) IR Program Backup
(not) CL 3 and 4
ODD CD
KY121
LSR Write Hi
LSR Write Lo
CI 8
Phase D
CL 6
CL 4
(not) EB Cycle
(not) I-H Cycle
(not) Alter or Display Storage
KL101
Channel Inhibit LSR Load
I/O Not CE Test
Idle Time
A or B Reg Chk
LSR to A or B
IAR (Hi)
IAR (Lo)
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
IAR Seld
I Cycle not I-X Cycle
CL 5 Thru 0
Allow LSR Select
KL141

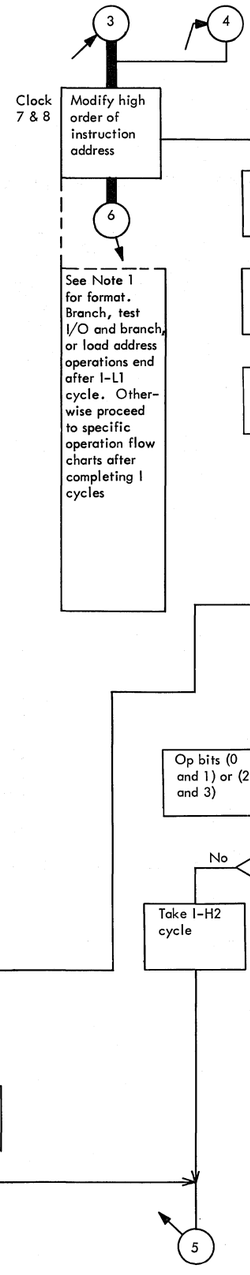
1

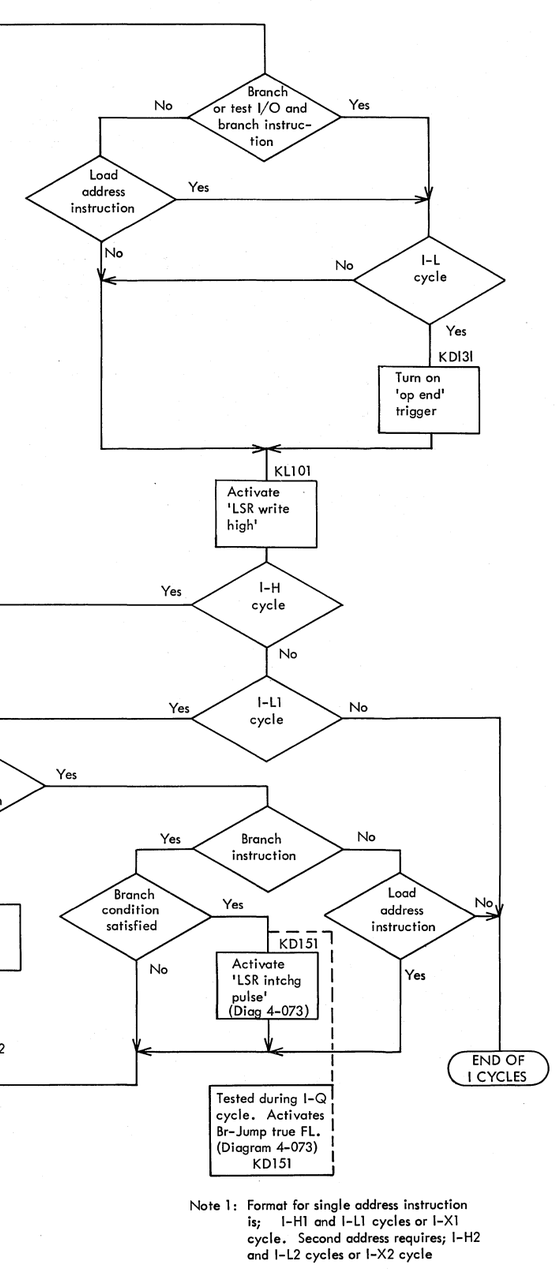
Objectives:

- Load B Address Register except during load address instruction
- Load selected Index Register for load address instruction
- Load A Address Register for second address
- Load Adress Recall Register for branch or decimal instructions

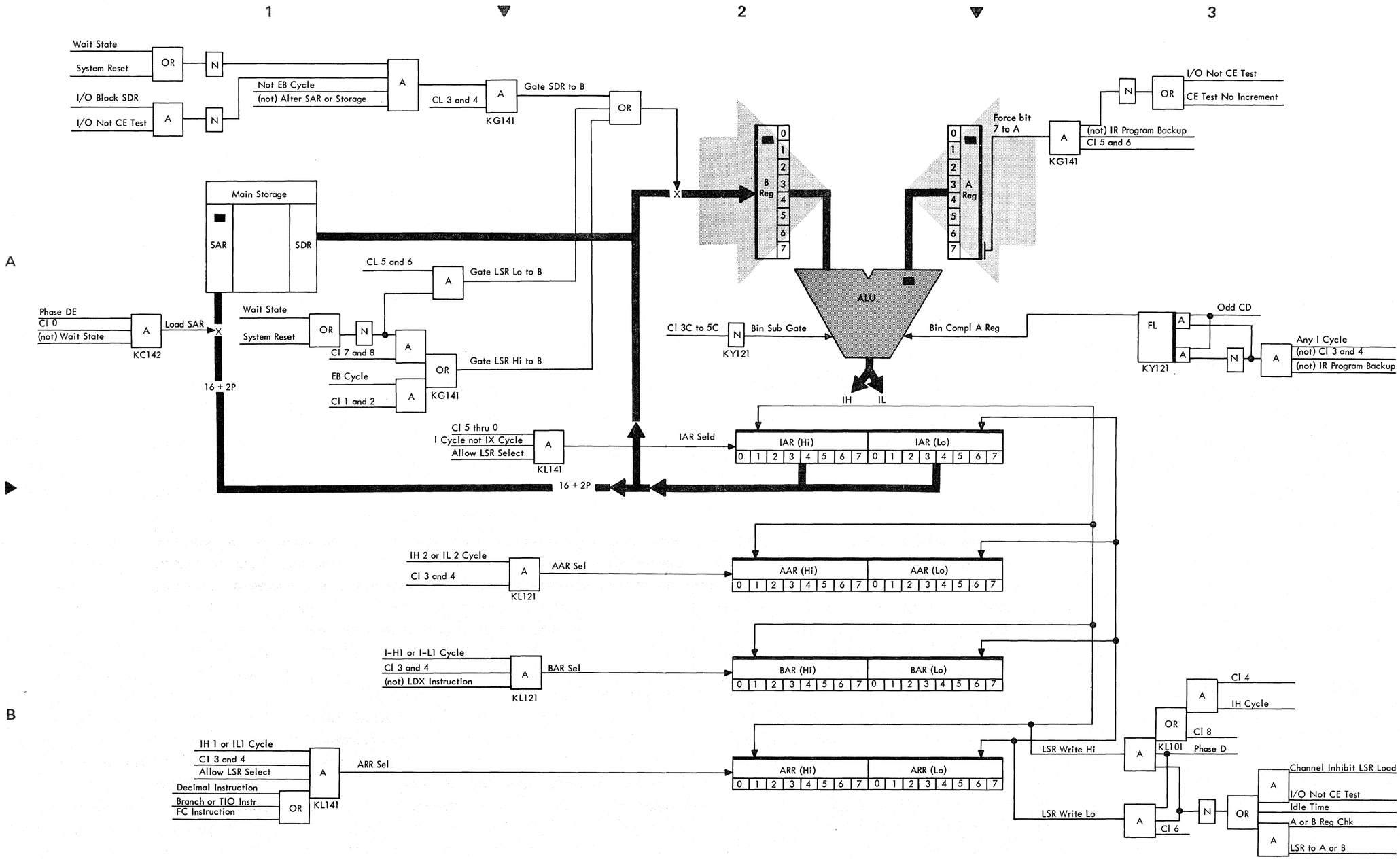




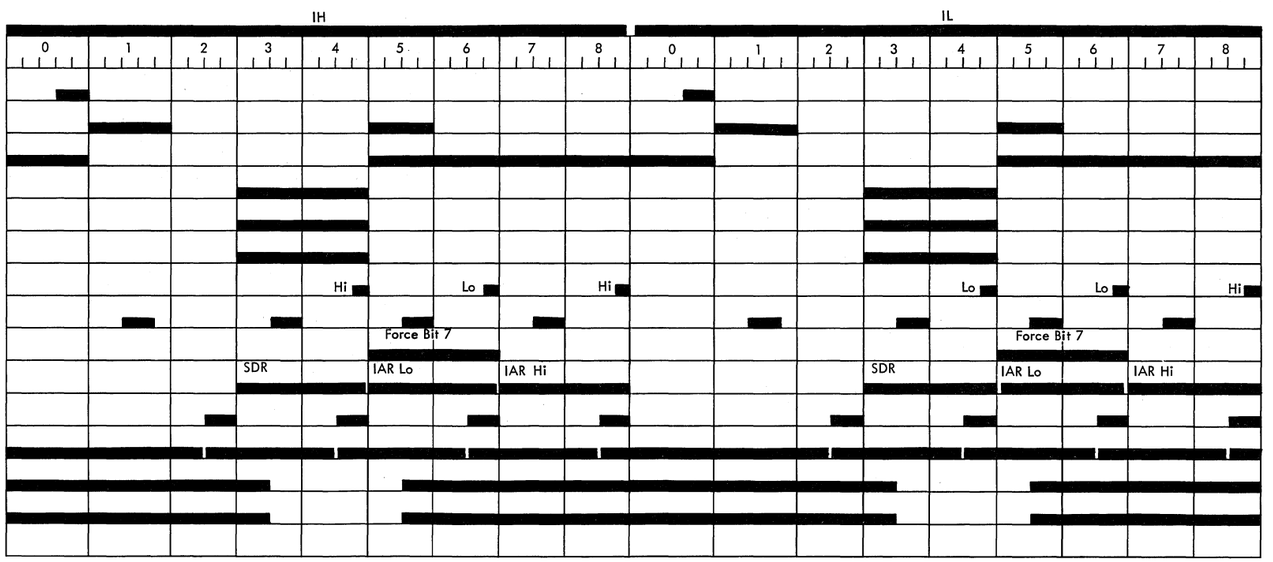




Note 1: Format for single address instruction is; I-H1 and I-L1 cycles or I-X1 cycle. Second address requires; I-H2 and I-L2 cycles or I-X2 cycle


1
2
3
A
B
Wait State
System Reset
OR
N
I/O Block SDR
I/O Not CE Test
A
N
Not EB Cycle
(not) Alter SAR or Storage
A
CL 3 and 4
A
KG141
Gate SDR to B
OR
Main Storage
SAR
SDR
X
B Reg
0 1 2 3 4 5 6 7
A Reg
0 1 2 3 4 5 6 7
Force bit 7 to A
A
KG141
(not) IR Program Backup
CI 5 and 6
N
OR
I/O Not CE Test
CE Test No Increment
CL 5 and 6
A
Gate LSR Lo to B
Phase DE
CI 0
(not) Wait State
A
KC142
Load SAR
X
16 + 2P
Wait State
System Reset
OR
N
CI 7 and 8
A
EB Cycle
CI 1 and 2
A
OR
KG141
Gate LSR Hi to B
ALU
CI 3C to 5C
N
KY121
Bin Sub Gate
Bin Compl A Reg
FL
A
A
KY121
Odd CD
N
A
Any I Cycle
(not) CI 3 and 4
(not) IR Program Backup
IH
IL
CI 5 thru 0
I Cycle not IX Cycle
Allow LSR Select
A
KL141
IAR Seld
IAR (Hi)
0 1 2 3 4 5 6 7
IAR (Lo)
0 1 2 3 4 5 6 7
16 + 2P
IH 2 or IL 2 Cycle
CI 3 and 4
A
KL121
AAR Sel
AAR (Hi)
0 1 2 3 4 5 6 7
AAR (Lo)
0 1 2 3 4 5 6 7
I-H1 or I-L1 Cycle
CI 3 and 4
(not) LDX Instruction
A
KL121
BAR Sel
BAR (Hi)
0 1 2 3 4 5 6 7
BAR (Lo)
0 1 2 3 4 5 6 7
IH 1 or IL1 Cycle
CI 3 and 4
Allow LSR Select
Decimal Instruction
Branch or TIO Instr
FC Instruction
A
OR
KL141
ARR Sel
ARR (Hi)
0 1 2 3 4 5 6 7
ARR (Lo)
0 1 2 3 4 5 6 7
CI 4
A
IH Cycle
OR
CI 8
KL101
Phase D
LSR Write Hi
A
LSR Write Lo
A
CI 6
N
OR
Channel Inhibit LSR Load
A
I/O Not CE Test
Idle Time
A or B Reg Chk
A
LSR to A or B

1 ▼ 2 ▼ 3



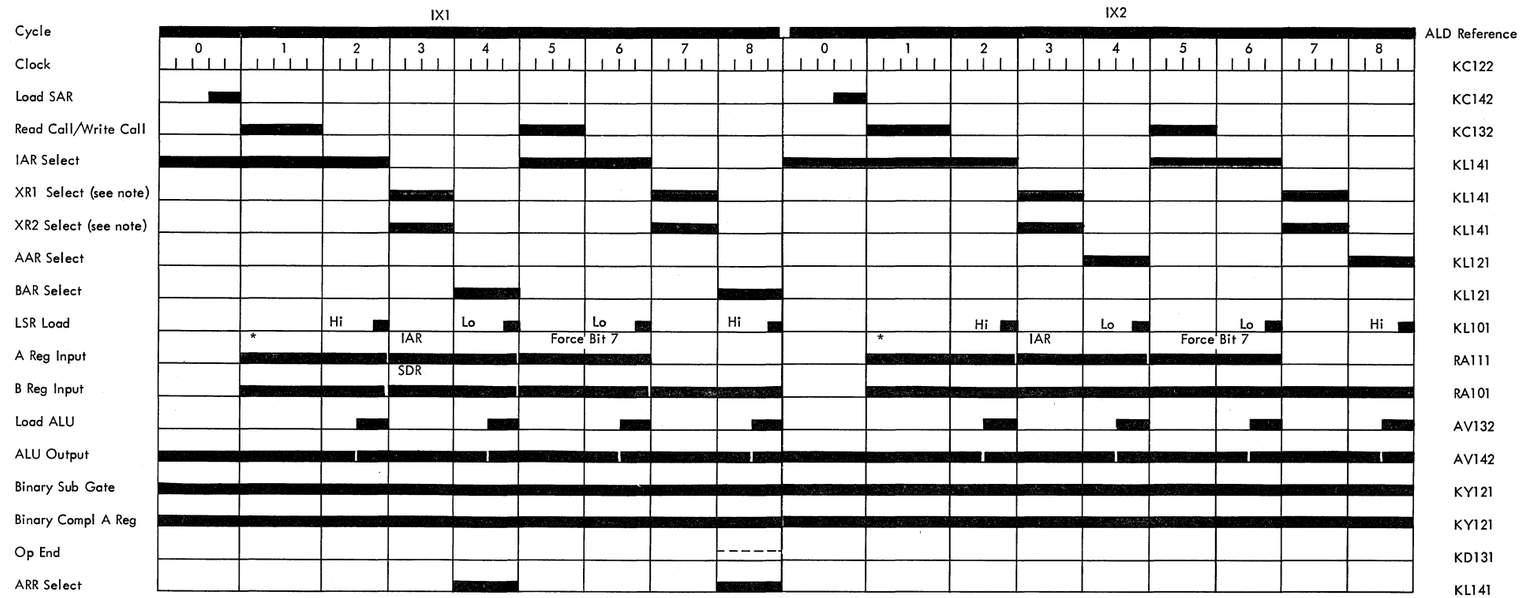
ALD Reference
KC122
KC142
KC132
KL141
KL121
KL121
KL141
KL101
RA101
RA111
RA101
AV132
AV142
KY121
KY121

* Load ARR during IH1 and IL1 if BC, TIO or Decimal Instruction

A

B

1 ▼ 2 ▼ 3



A

* Force bit 7 if IAR Lo contains all 1's
(Predicts a carry from IAR-Lo)

NOTE: The contents of Op Register bits 0 thru 3 determine which Index Register is used.

B

Instruction Format	Op Bits 0	1	2	3	B Address Register	A Address Register
2 Address	0	0	0	0	2 bytes from Storage Unchanged	2 bytes from Storage Unchanged
	0	0	0	1		1 byte from Storage Added to Address from XR1
	0	0	1	0		1 byte from Storage Added to Address from XR2
	0	1	0	0	1 byte from Storage Added to Address from XR1	2 bytes from Storage Unchanged
	0	1	0	1		1 byte from Storage Added to Address from XR1
	0	1	1	0		1 byte from Storage Added to Address from XR2
	1	0	0	0	1 byte from Storage Added to Address from XR2	2 bytes from Storage Unchanged
	1	0	0	1		1 byte from Storage Added to Address from XR1
	1	0	1	0		1 byte from Storage Added to Address from XR2

Instruction Format	Op Bits 0	1	2	3	B Address Register
1 Address (non-branch)	0	0	1	1	2 bytes from Storage Unchanged
	0	1	1	1	1 byte from Storage Added to Address from XR1
	1	0	1	1	1 byte from Storage Added to Address from XR2
1 Address (Branch)	1	1	0	0	2 bytes from Storage Unchanged
	1	1	0	1	1 byte from Storage Added to Address from XR1
	1	1	1	0	1 byte from Storage Added to Address from XR2
Command	1	1	1	1	———

1 2 3

Objectives:
- Add address to contents of Index Register
- Load B Address Register unless load address instruction
- Load selected index register if load address instruction
- Load A Register for second address
- Load Address Recall Register for Branch or Decimal operations

I-X CYCLE

D Diag 5-010

Clock 0: Address storage

Activate 'IAR seld' KL141

Activate 'load SAR' KC142

A

Refer to diagram 5-010 point A to determine which type of cycle to take after I-Q cycle

Clock 1 & 2: Increment high order of instruction address

Activate 'IAR seld' KL141

Activate 'gate LSR hi to B' KG141

Low order of IAR will carry to high when incremented

MA121 LSR low F-F: No / Yes

Activate 'misc bit 7 to A' KG141

Activate 'bin comp A reg' and 'bin sub gate' KY121

Activate 'LSR write high' KL101

B

Clock 3 & 4: Load low order of selected register

(1) (2)

(2)

I-X1 cycle: No / Yes

single address instruction: No / Yes

Activate 'XR1 seld' or 'XR2 seld' KL141

XR1 for Op bit 1. XR2 for Op bit 0

XR1 for Op bit 3. XR2 for op bit 2

XR1 for Op bit 1 (not) bit 0 or Op bit 3 (not) bit 2 . XR2 for Op bit 0 (not) 1 or Op bit 2 (not) 3

Activate 'gate LSR lo normal to A' KG131

Activate 'gate SDR to B' KG141

Activate 'bin comp A req' and 'bin sub gate' KY121

Clock 4: Deactivate 'XR1 seld' or 'XR2 seld' KL141

Load address instruction: No / Yes

I-X1 cycle: No / Yes

Activate 'XR1 seld' or 'XR2 seld' KL141

Activate 'sel BAR' KL121

XR1 - Q bit 7
XR2 - Q bit 6

Branch or decimal instruction: No / Yes

Activate 'ARR seld' KL141

Activate 'sel AAR' KL121

Activate 'LSR write low' KL101

(1)

(1)

Clock 5 & 6: Increment low order of instruction address

Activate 'IAR seld' KL141

If computation resulted in a carry, 'temp carry' gives 'arith carry out' for clock 7 computation

Activate 'gate LSR lo to B' KG141

Activate 'misc bit 7 to A' KG141

Activate 'bin comp A req' and 'bin sub gate' KY121

Activate 'LSR write low' KL101

Clock 7 & 8: Load high order of selected register

Activate 'XR1 seld' or 'XR2 seld' KL141

Select same index register selected at clock 3

See Note 1 for format. Branch, test I/O and branch, or load address operations end after I-X1 cycle. Otherwise proceed to specific operation flow charts after completing I-cycles

Activate 'gate LSR hi to B' KG141

Activate 'bin comp A reg' and 'bin sub gate' KY121

Clock 8: Deactivate 'XR1 seld' or 'XR2 seld' KL141

Activate 'sel BAR,' 'ARR seld,' 'sel AAR,' 'XR1 seld,' or 'XR2 seld' KL121 KL141 KL121 KL141 KL141

Select same register selected at clock 4

Branch or test I/O and branch instruction: No / Yes

Load address instruction: Yes / No

Turn on 'Op end' trigger KD131

(3)

(3)

Activate 'LSR write high' KL101

I-X1 cycle: No / Yes

Op bits (0 and 1) or (2 and 3)

Single address instruction: Yes / No

Op bit 2 or Op bit 3: Yes / No

Take I-X2 cycle

(4)

Take I-H2 cycle

C

Diag 5-030

Branch instruction: No / Yes

Load address instruction: No / Yes

Branch condition satisfied: No / Yes

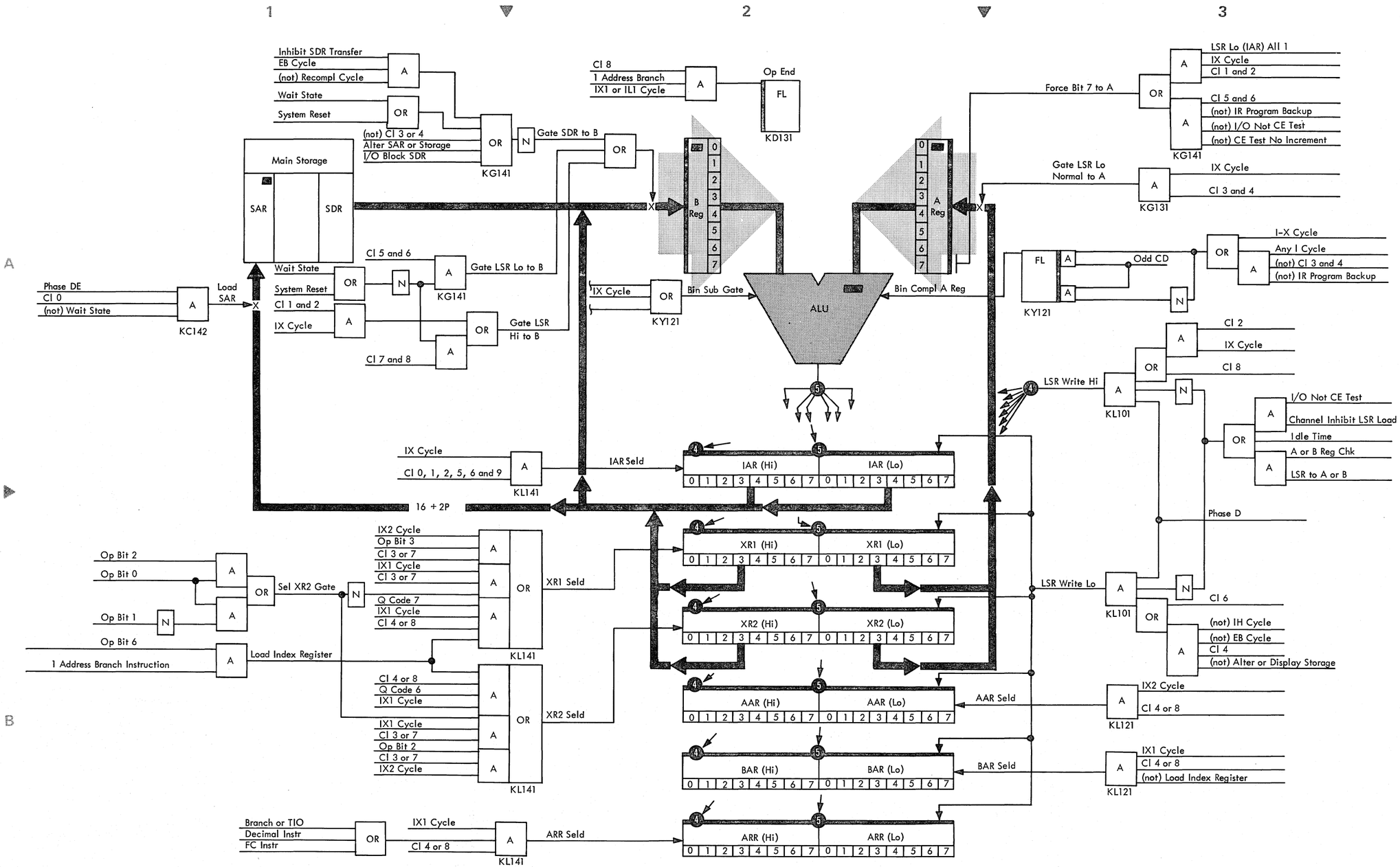
Activate 'LSR intchg pulse' KD151

END OF OPERATION

END OF I CYCLES

Tested during I-Q cycle. Activates Br-Jump true FL. (Diagram 4-073) KD151

Note 1: Format for single address instruction is; I-H1 and I-L1 cycles or I-X1 cycle. Second address requires; I-H2 and I-L2 cycles or I-X2 cycle.


1
2
3
A
B
Inhibit SDR Transfer
EB Cycle
(not) Recompl Cycle
Wait State
System Reset
(not) CI 3 or 4
Alter SAR or Storage
I/O Block SDR
KG141
Gate SDR to B
Main Storage
SAR
SDR
CI 8
1 Address Branch
IX1 or IL1 Cycle
Op End
FL
KD131
B Reg
A Reg
Force Bit 7 to A
LSR Lo (IAR) All 1
IX Cycle
CI 1 and 2
CI 5 and 6
(not) IR Program Backup
(not) I/O Not CE Test
(not) CE Test No Increment
Gate LSR Lo Normal to A
IX Cycle
CI 3 and 4
KG131
Phase DE
CI 0
(not) Wait State
Load SAR
KC142
Wait State
System Reset
CI 1 and 2
IX Cycle
CI 7 and 8
CI 5 and 6
Gate LSR Lo to B
Gate LSR Hi to B
IX Cycle
Bin Sub Gate
KY121
ALU
Bin Compl A Reg
Odd CD
I-X Cycle
Any I Cycle
(not) CI 3 and 4
(not) IR Program Backup
LSR Write Hi
CI 2
IX Cycle
CI 8
KL101
I/O Not CE Test
Channel Inhibit LSR Load
Idle Time
A or B Reg Chk
LSR to A or B
Phase D
IX Cycle
CI 0, 1, 2, 5, 6 and 9
KL141
IAR Seld
IAR (Hi)
IAR (Lo)
16 + 2P
XR1 (Hi)
XR1 (Lo)
XR2 (Hi)
XR2 (Lo)
AAR (Hi)
AAR (Lo)
BAR (Hi)
BAR (Lo)
ARR (Hi)
ARR (Lo)
LSR Write Lo
CI 6
(not) IH Cycle
(not) EB Cycle
CI 4
(not) Alter or Display Storage
IX2 Cycle
Op Bit 3
CI 3 or 7
IX1 Cycle
CI 3 or 7
Q Code 7
IX1 Cycle
CI 4 or 8
XR1 Seld
Op Bit 2
Op Bit 0
Op Bit 1
Sel XR2 Gate
Op Bit 6
1 Address Branch Instruction
Load Index Register
CI 4 or 8
Q Code 6
IX1 Cycle
IX1 Cycle
CI 3 or 7
Op Bit 2
CI 3 or 7
IX2 Cycle
XR2 Seld
AAR Seld
IX2 Cycle
CI 4 or 8
KL121
BAR Seld
IX1 Cycle
CI 4 or 8
(not) Load Index Register
Branch or TIO
Decimal Instr
FC Instr
IX1 Cycle
CI 4 or 8
ARR Seld

1

Objectives:

bits 0 1 2 3 4 5 6 7
Set Bits On Masked Op Code X X 1 1 1 0 1 0

- If a bit is present in the Q code, turn on the corresponding bit in the storage location specified by the B Address Register
- Do not change bits which correspond with bits not present in the Q code

bits 0 1 2 3 4 5 6 7
Set Bits Off Masked Op Code X X 1 1 1 0 1 1

- If a bit is present in the Q code, turn off the corresponding bit in the storage location specified by the B Address Register
- Do not change bits which correspond with bits not present in the Q code

A

bits 0 1 2 3 4 5 6 7
Test Bits On Masked Op Code X X 1 1 1 0 0 0

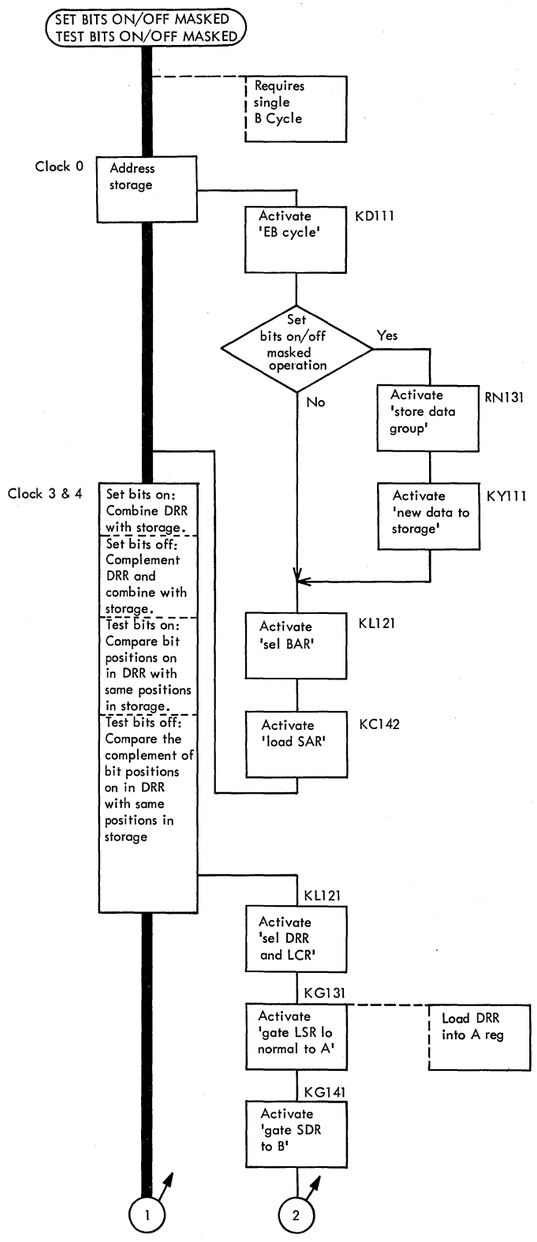
- If a bit is present in the Q code, test to see if the corresponding bit in the storage location specified by the B Address Register is on
- Ignore bits which correspond with bits not present in the Q code.
- Turn on 'test false' latch if selected bits are not all on

bits 0 1 2 3 4 5 6 7
Test Bits Off Masked Op Code X X 1 1 1 0 0 1

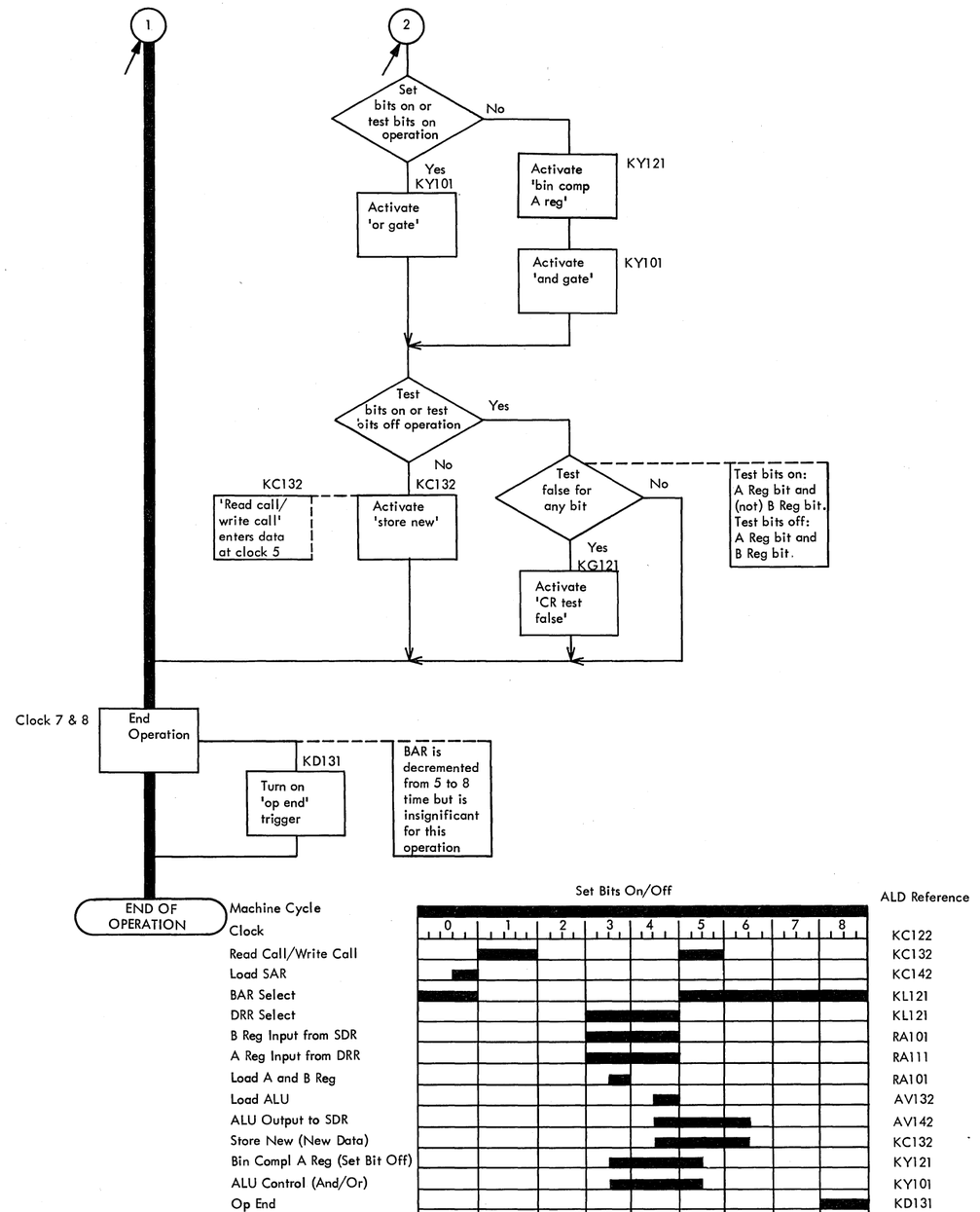
- If a bit is present in the Q code, test to see if the corresponding bit in the storage location specified by the B Address Register is off
- Ignore bits which correspond with bits not present in the Q code
- Turn on 'test false' latch if selected bits are not all off

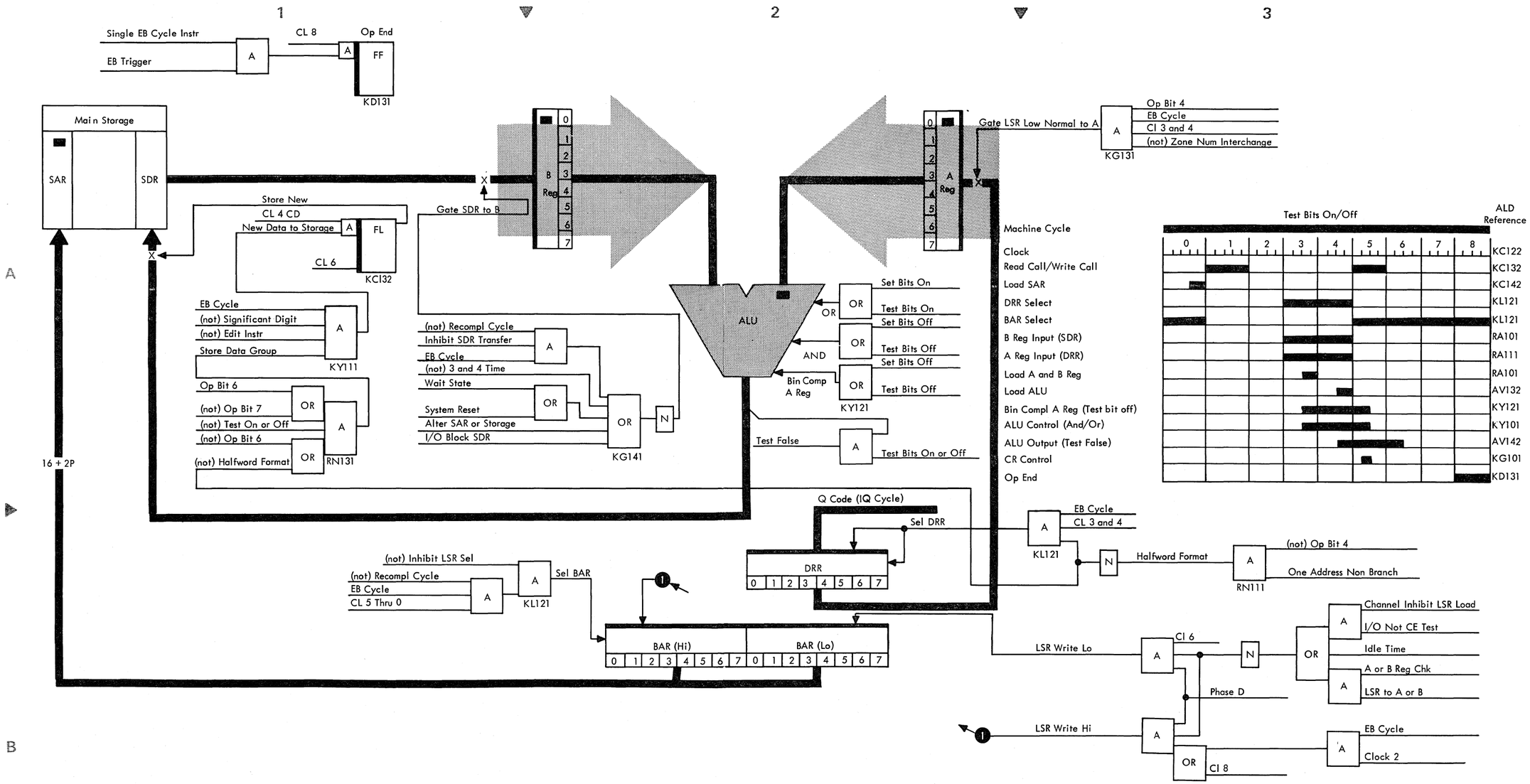
B

2



3




1
2
3
A
B
Single EB Cycle Instr
EB Trigger
A
CL 8
A
Op End
FF
KD131
Main Storage
SAR
SDR
X
Store New
CL 4 CD
New Data to Storage
A
FL
CL 6
KC132
EB Cycle
(not) Significant Digit
(not) Edit Instr
Store Data Group
A
KY111
Op Bit 6
(not) Op Bit 7
(not) Test On or Off
(not) Op Bit 6
OR
A
(not) Halfword Format
OR
RN131
16 + 2P
Gate SDR to B
B Reg
0 1 2 3 4 5 6 7
(not) Recompl Cycle
Inhibit SDR Transfer
A
EB Cycle
(not) 3 and 4 Time
Wait State
System Reset
Alter SAR or Storage
I/O Block SDR
OR
OR
N
KG141
ALU
AND
OR
Set Bits On
Test Bits On
Set Bits Off
Test Bits Off
Bin Comp A Reg
OR
Set Bits Off
Test Bits Off
KY121
Test False
A
Test Bits On or Off
A Reg
Gate LSR Low Normal to A
A
KG131
Op Bit 4
EB Cycle
CI 3 and 4
(not) Zone Num Interchange
Machine Cycle
Clock
Read Call/Write Call
Load SAR
DRR Select
BAR Select
B Reg Input (SDR)
A Reg Input (DRR)
Load A and B Reg
Load ALU
Bin Compl A Reg (Test bit off)
ALU Control (And/Or)
ALU Output (Test False)
CR Control
Op End
Test Bits On/Off
ALD Reference
0 1 2 3 4 5 6 7 8
KC122
KC132
KC142
KL121
KL121
RA101
RA111
RA101
AV132
KY121
KY101
AV142
KG101
KD131
Q Code (IQ Cycle)
Sel DRR
DRR
0 1 2 3 4 5 6 7
EB Cycle
CL 3 and 4
A
KL121
N
Halfword Format
A
RN111
(not) Op Bit 4
One Address Non Branch
(not) Inhibit LSR Sel
(not) Recompl Cycle
EB Cycle
CL 5 Thru 0
A
A
KL121
Sel BAR
1
BAR (Hi)
0 1 2 3 4 5 6 7
BAR (Lo)
0 1 2 3 4 5 6 7
LSR Write Lo
A
CI 6
N
OR
A
Channel Inhibit LSR Load
I/O Not CE Test
Idle Time
A or B Reg Chk
A
LSR to A or B
Phase D
1
LSR Write Hi
A
OR
CI 8
A
EB Cycle
Clock 2

Objectives:

		bits - 0 1 2 3 4 5 6 7
Store Register	Op Code	X X 1 1 0 1 0 0

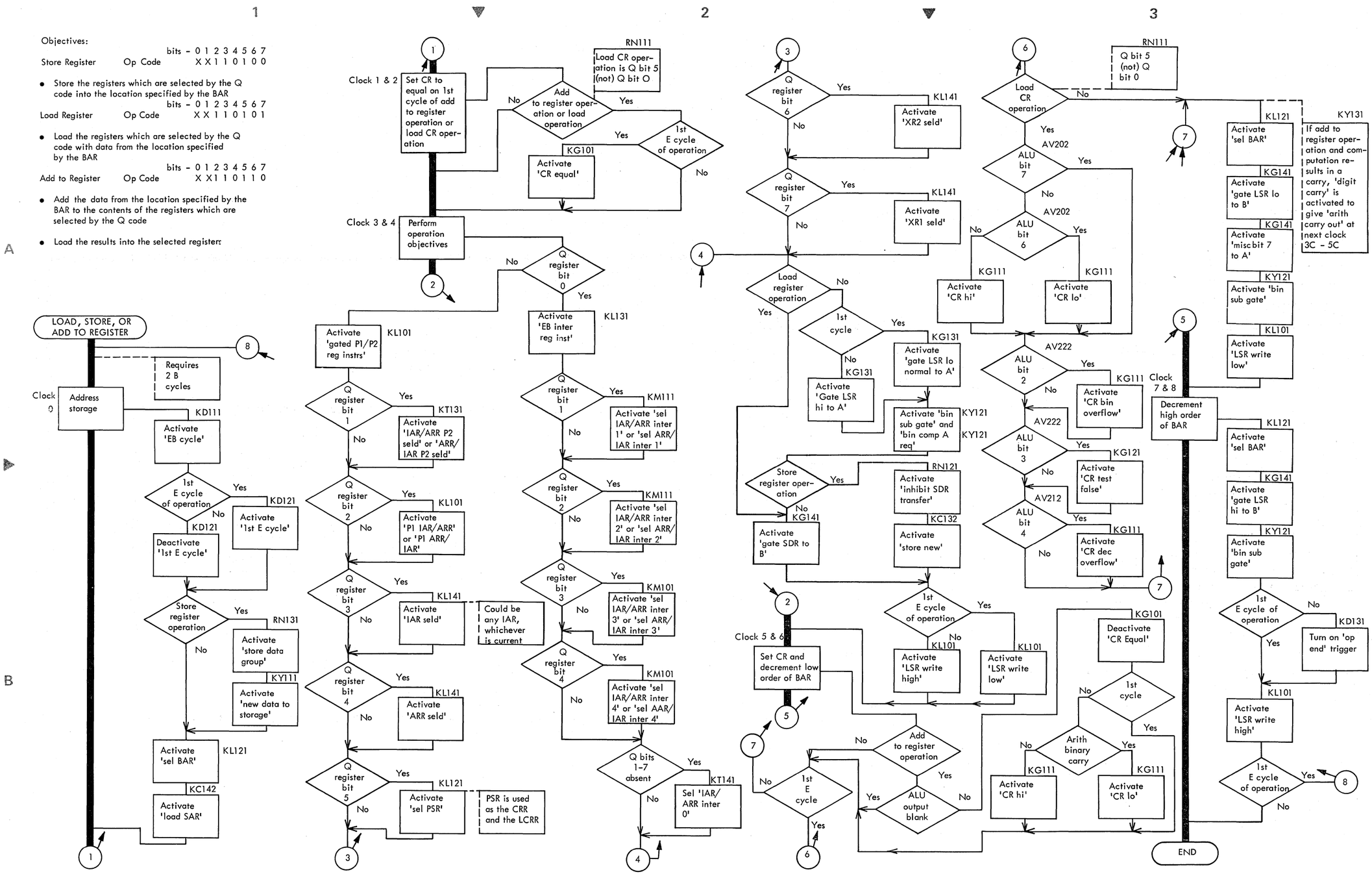
- Store the registers which are selected by the Q code into the location specified by the BAR

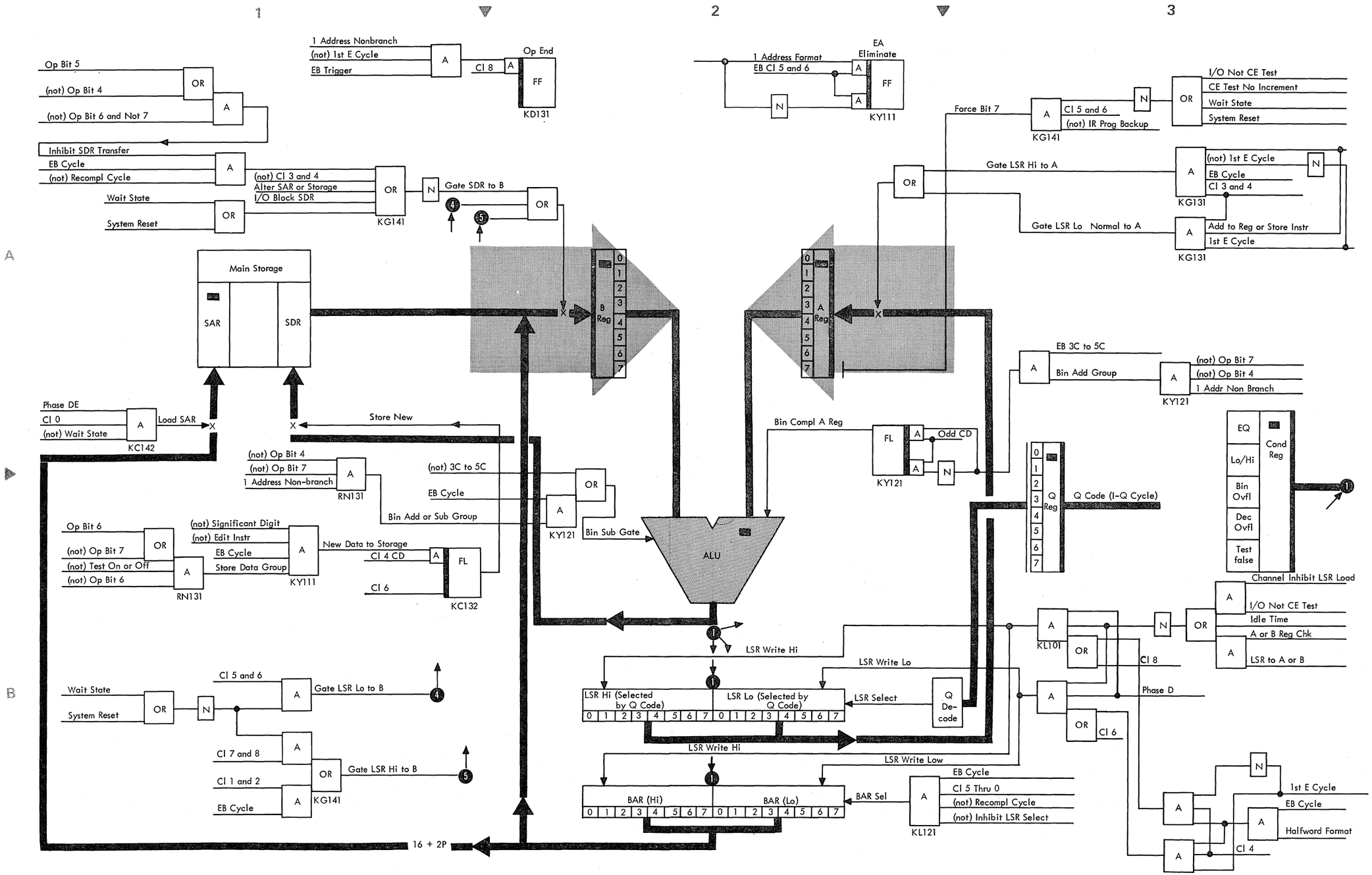
		bits - 0 1 2 3 4 5 6 7
Load Register	Op Code	X X 1 1 0 1 0 1

- Load the registers which are selected by the Q code with data from the location specified by the BAR

		bits - 0 1 2 3 4 5 6 7
Add to Register	Op Code	X X 1 1 0 1 1 0

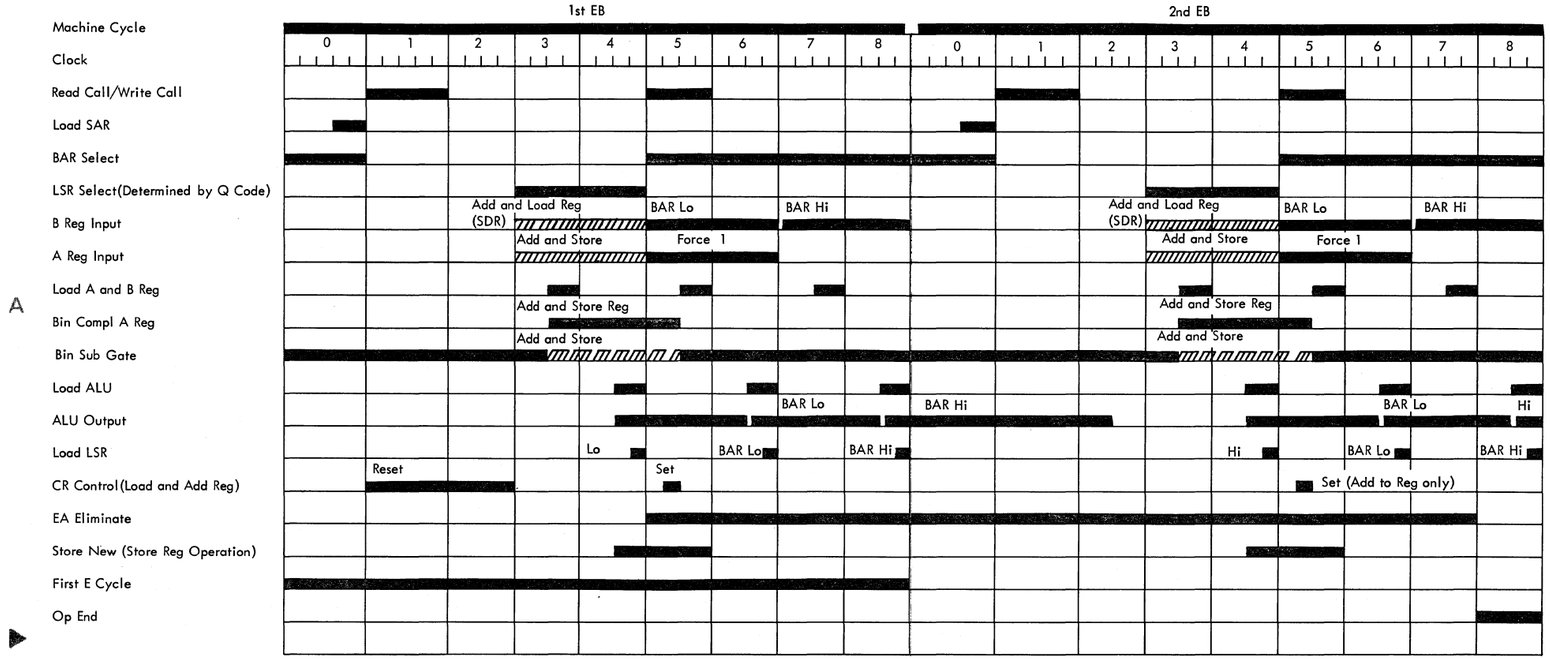
- Add the data from the location specified by the BAR to the contents of the registers which are selected by the Q code
- Load the results into the selected register




1
2
3
A
B
1 Address Nonbranch
(not) 1st E Cycle
EB Trigger
A
Op End
Cl 8
FF
KD131
Op Bit 5
(not) Op Bit 4
OR
A
(not) Op Bit 6 and Not 7
Inhibit SDR Transfer
EB Cycle
(not) Recompl Cycle
A
(not) Cl 3 and 4
Alter SAR or Storage
I/O Block SDR
OR
KG141
N
Gate SDR to B
Wait State
System Reset
OR
OR
Main Storage
SAR
SDR
B Reg
A Reg
X
Phase DE
Cl 0
(not) Wait State
A
Load SAR
KC142
Store New
(not) Op Bit 4
(not) Op Bit 7
1 Address Non-branch
A
RN131
(not) 3C to 5C
EB Cycle
Bin Add or Sub Group
OR
A
KY121
Bin Sub Gate
ALU
Op Bit 6
(not) Op Bit 7
(not) Test On or Off
(not) Op Bit 6
OR
A
RN131
(not) Significant Digit
(not) Edit Instr
EB Cycle
Store Data Group
A
KY111
New Data to Storage
Cl 4 CD
Cl 6
A
FL
KC132
1 Address Format
EB Cl 5 and 6
A
N
A
FF
KY111
EA Eliminate
Force Bit 7
A
Cl 5 and 6
(not) IR Prog Backup
KG141
N
OR
I/O Not CE Test
CE Test No Increment
Wait State
System Reset
Gate LSR Hi to A
OR
A
(not) 1st E Cycle
EB Cycle
Cl 3 and 4
KG131
N
Gate LSR Lo Normal to A
A
Add to Reg or Store Instr
1st E Cycle
KG131
Bin Compl A Reg
FL
A
Odd CD
A
N
KY121
Q Reg
Q Code (I-Q Cycle)
EB 3C to 5C
A
Bin Add Group
A
(not) Op Bit 7
(not) Op Bit 4
1 Addr Non Branch
KY121
EQ
Lo/Hi
Bin Ovfl
Dec Ovfl
Test false
Cond Reg
Channel Inhibit LSR Load
A
I/O Not CE Test
Idle Time
A or B Reg Chk
A
LSR to A or B
KL101
A
OR
Cl 8
N
OR
Phase D
A
OR
Cl 6
LSR Write Hi
LSR Write Lo
LSR Hi (Selected by Q Code)
LSR Lo (Selected by Q Code)
LSR Select
Q De-code
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
LSR Write Hi
LSR Write Low
BAR (Hi)
BAR (Lo)
BAR Sel
A
EB Cycle
Cl 5 Thru 0
(not) Recompl Cycle
(not) Inhibit LSR Select
KL121
Wait State
System Reset
OR
N
Cl 5 and 6
A
Gate LSR Lo to B
Cl 7 and 8
Cl 1 and 2
EB Cycle
A
OR
A
KG141
Gate LSR Hi to B
16 + 2P
N
A
1st E Cycle
EB Cycle
A
Halfword Format
A
Cl 4

1 ▼ 2 ▼ 3

A



ALD Reference
KC122
KC132
KC142
KL121
KL121
RA101
RA111
RA101
KY121
KY101
AV132
AV142
KL101
KG111
KY111
KC132
KD111
KD131

LSR Selection		
Q Code bits	With Q bit 0	With No Q bit 0
1	Interrupt 1 IAR	P2-IAR
2	Interrupt 2 IAR	P1-IAR
3	Interrupt 3 IAR	IAR
4	Interrupt 4 IAR	ARR
5	———	PSR
6	———	XR2
7	———	XR1
No other bits	Interrupt 0 IAR	———

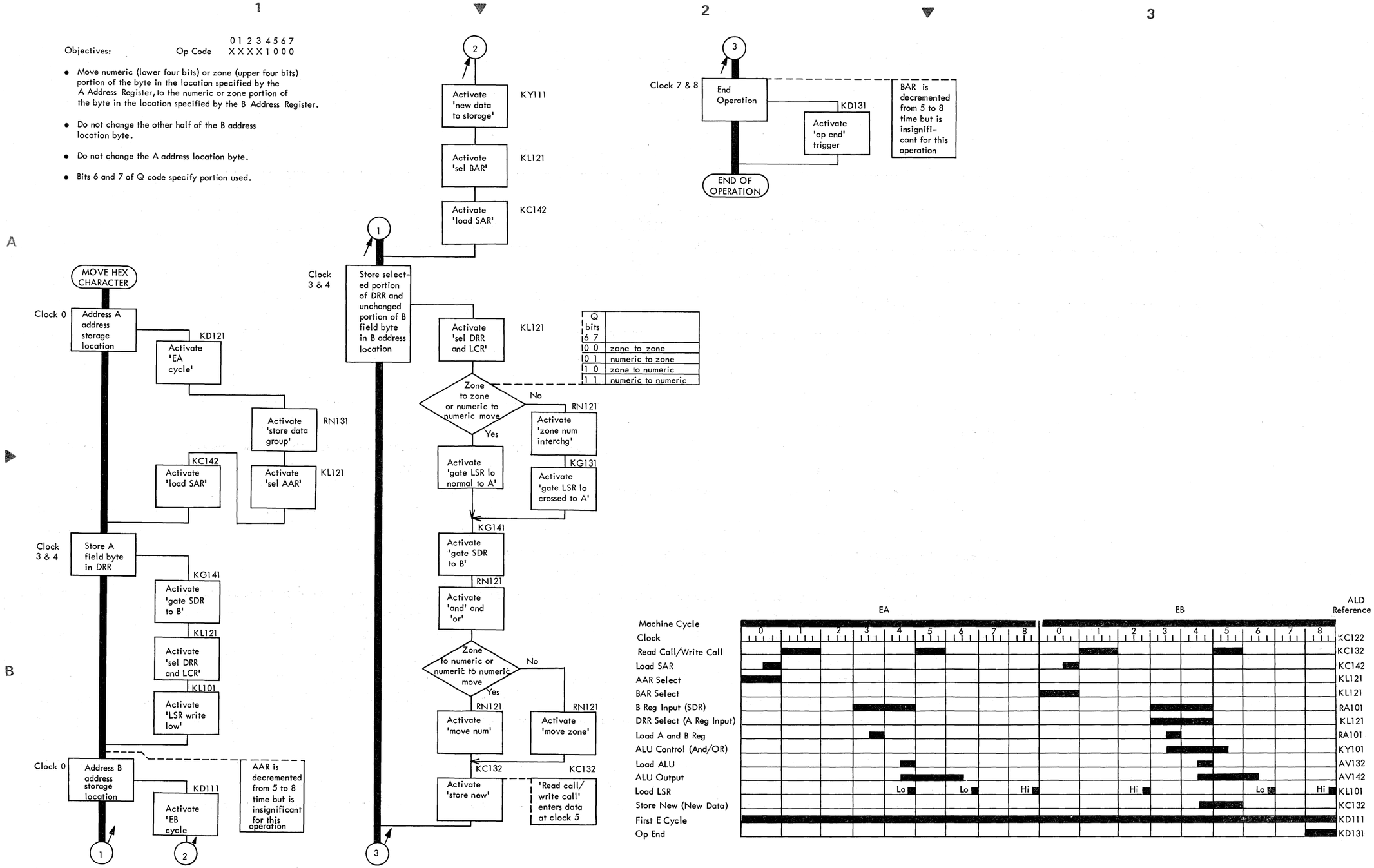
B

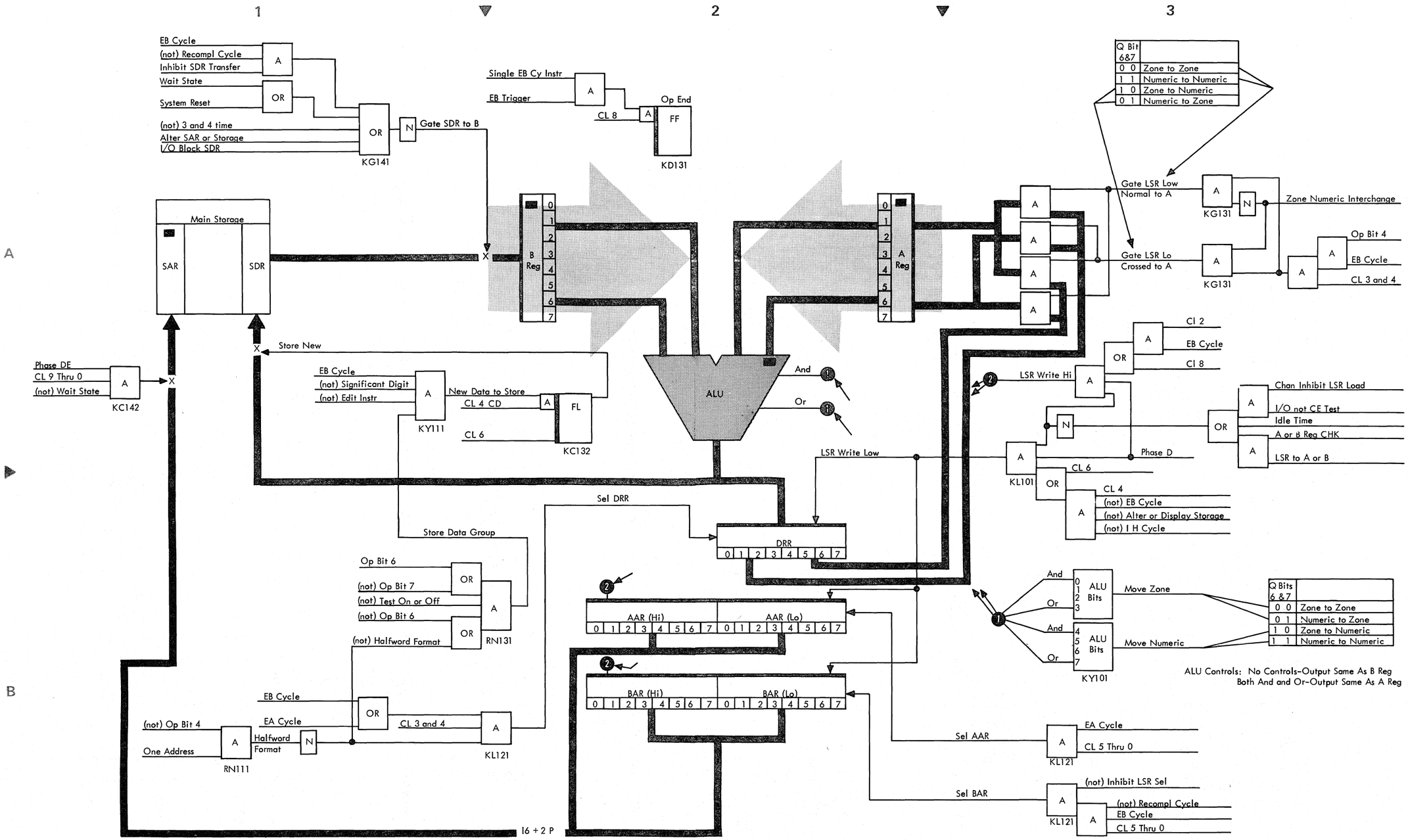
Condition Register						
Operation	Equal	Low	High	Binary Overflow	Test False	Decimal Overflow
Load PSR	If ALU bit 7	If ALU bit 6, not 7	If ALU not bit 6 or 7	If ALU bit 2	If ALU bit 3	If ALU bit 4
Add to Register	If Result is zero	If Result is not zero and a high order carry	If Result is not zero and no high order carry	If Result is too large for Register (no high order carry)	———	———

1 2 3

Objectives: Op Code 0 1 2 3 4 5 6 7 = X X X X 1 0 0 0

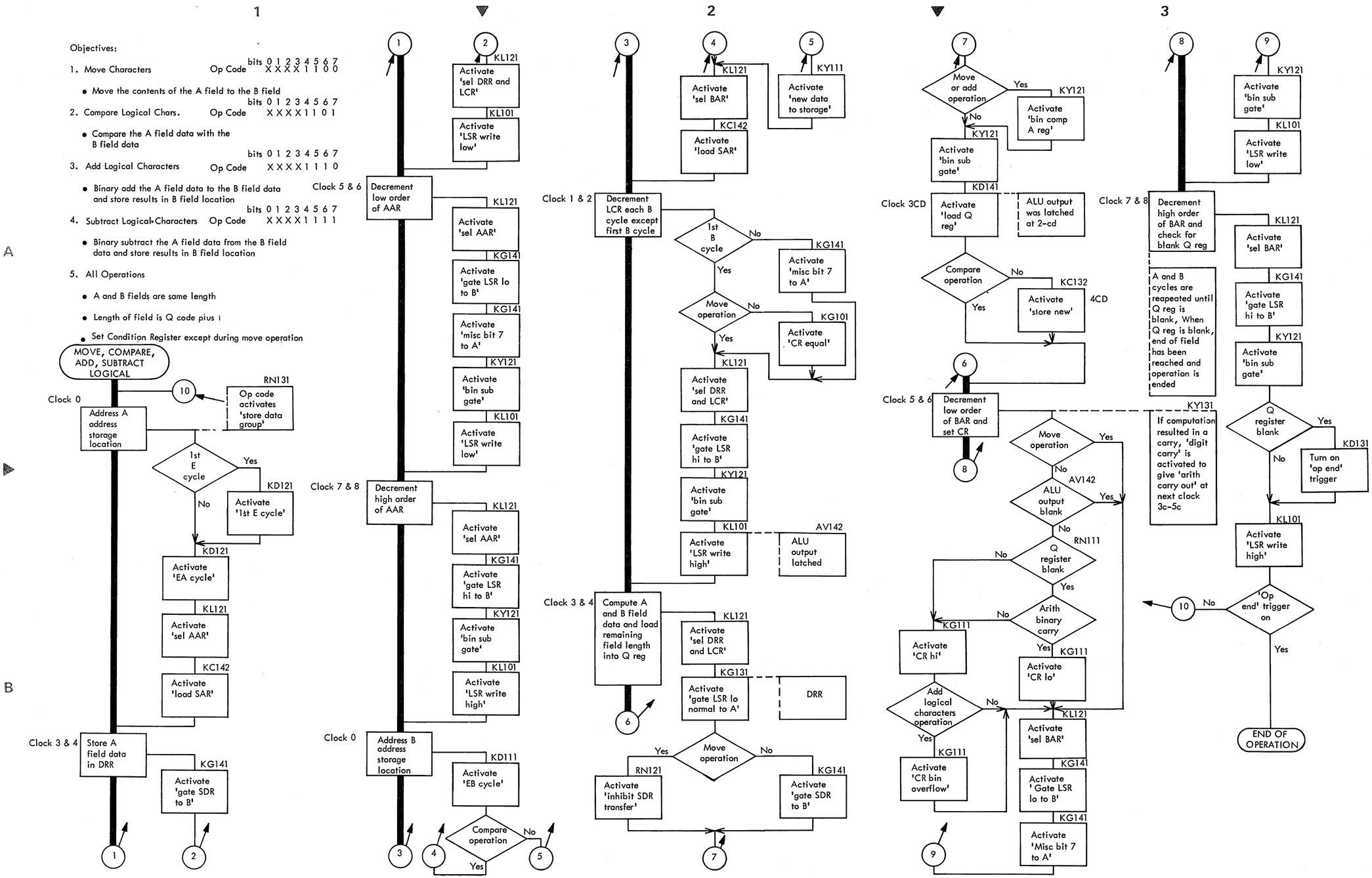
- Move numeric (lower four bits) or zone (upper four bits) portion of the byte in the location specified by the A Address Register, to the numeric or zone portion of the byte in the location specified by the B Address Register.
- Do not change the other half of the B address location byte.
- Do not change the A address location byte.
- Bits 6 and 7 of Q code specify portion used.

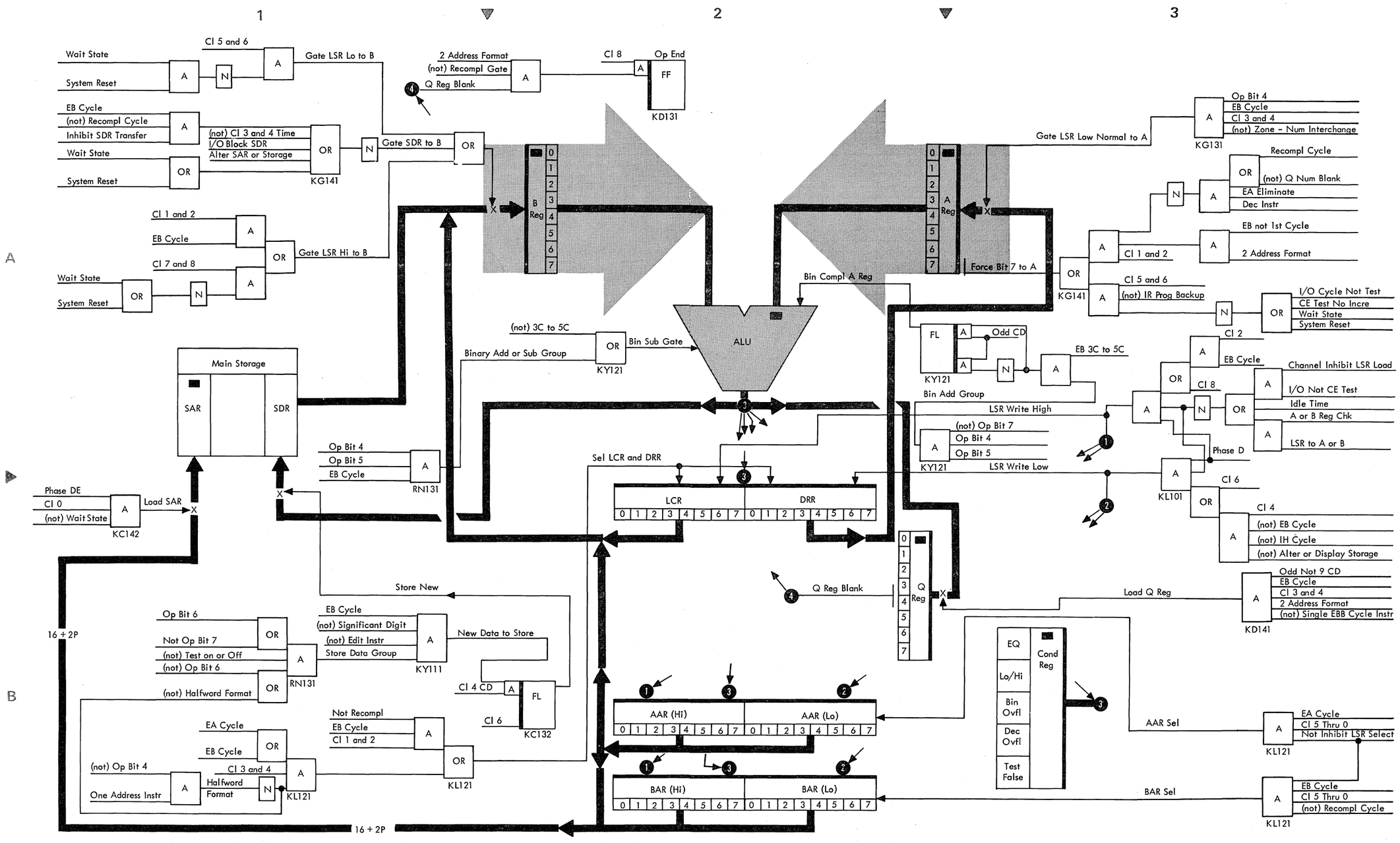


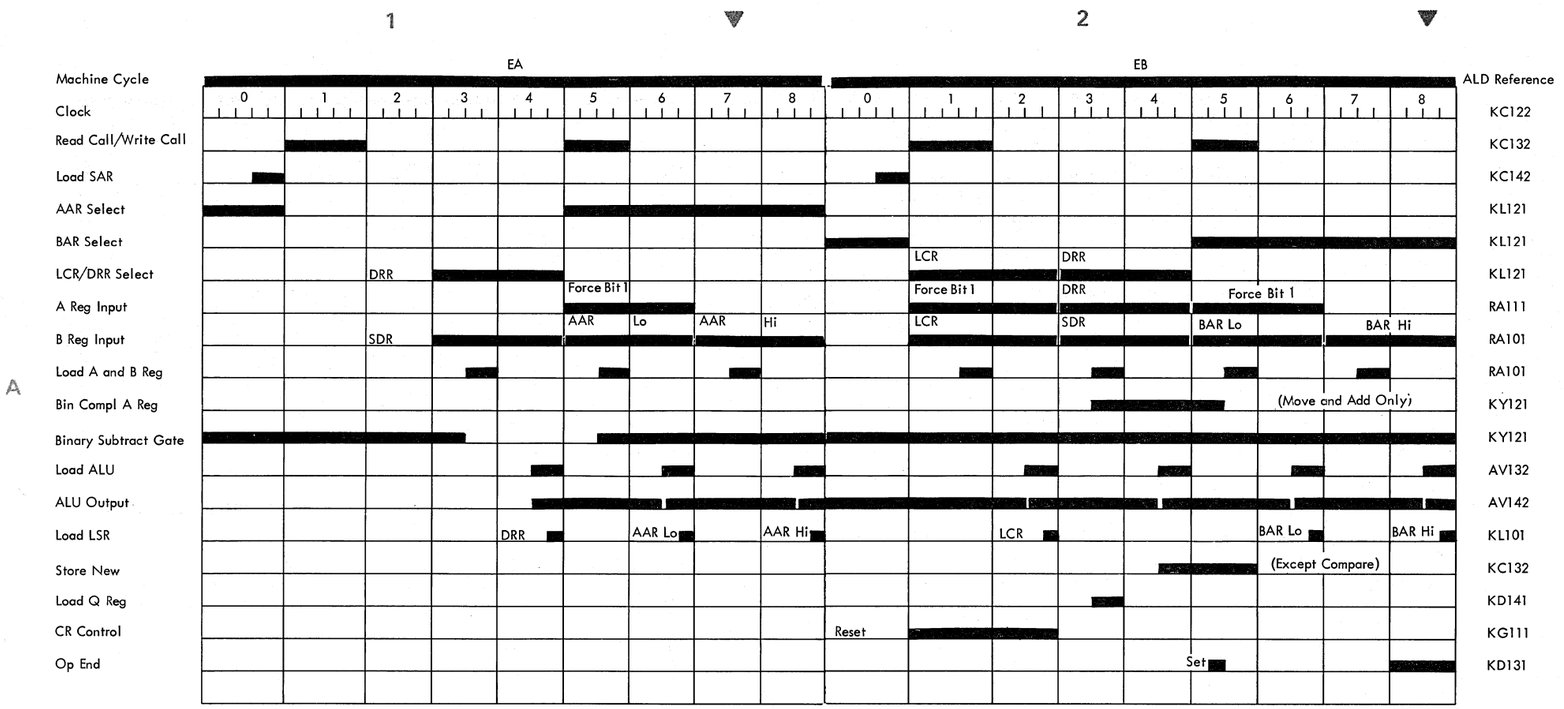

1
2
3
A
B
EB Cycle
(not) Recompl Cycle
Inhibit SDR Transfer
Wait State
System Reset
A
OR
(not) 3 and 4 time
Alter SAR or Storage
I/O Block SDR
OR
N
Gate SDR to B
KG141
Single EB Cy Instr
EB Trigger
A
CL 8
A
Op End
FF
KD131
Q Bit 6&7
0 0 Zone to Zone
1 1 Numeric to Numeric
1 0 Zone to Numeric
0 1 Numeric to Zone
Main Storage
SAR
SDR
X
B Reg
0 1 2 3 4 5 6 7
A Reg
0 1 2 3 4 5 6 7
ALU
And
Or
Gate LSR Low Normal to A
Gate LSR Lo Crossed to A
A
KG131
N
Zone Numeric Interchange
Op Bit 4
EB Cycle
CL 3 and 4
Store New
Phase DE
CL 9 Thru 0
(not) Wait State
A
KC142
EB Cycle
(not) Significant Digit
(not) Edit Instr
A
KY111
New Data to Store
CL 4 CD
CL 6
A
FL
KC132
Cl 2
EB Cycle
Cl 8
OR
LSR Write Hi
Chan Inhibit LSR Load
I/O not CE Test
Idle Time
A or B Reg CHK
LSR to A or B
LSR Write Low
Phase D
CL 6
KL101
CL 4
(not) EB Cycle
(not) Alter or Display Storage
(not) I H Cycle
Sel DRR
Store Data Group
DRR
0 1 2 3 4 5 6 7
Op Bit 6
(not) Op Bit 7
(not) Test On or Off
(not) Op Bit 6
(not) Halfword Format
RN131
AAR (Hi)
AAR (Lo)
BAR (Hi)
BAR (Lo)
ALU Bits
Move Zone
Move Numeric
KY101
Q Bits 6 & 7
0 0 Zone to Zone
0 1 Numeric to Zone
1 0 Zone to Numeric
1 1 Numeric to Numeric
ALU Controls: No Controls-Output Same As B Reg
Both And and Or-Output Same As A Reg
EB Cycle
EA Cycle
(not) Op Bit 4
One Address
Halfword Format
RN111
CL 3 and 4
KL121
Sel AAR
Sel BAR
EA Cycle
CL 5 Thru 0
(not) Inhibit LSR Sel
(not) Recompl Cycle
EB Cycle
CL 5 Thru 0
16 + 2 P

Objectives:

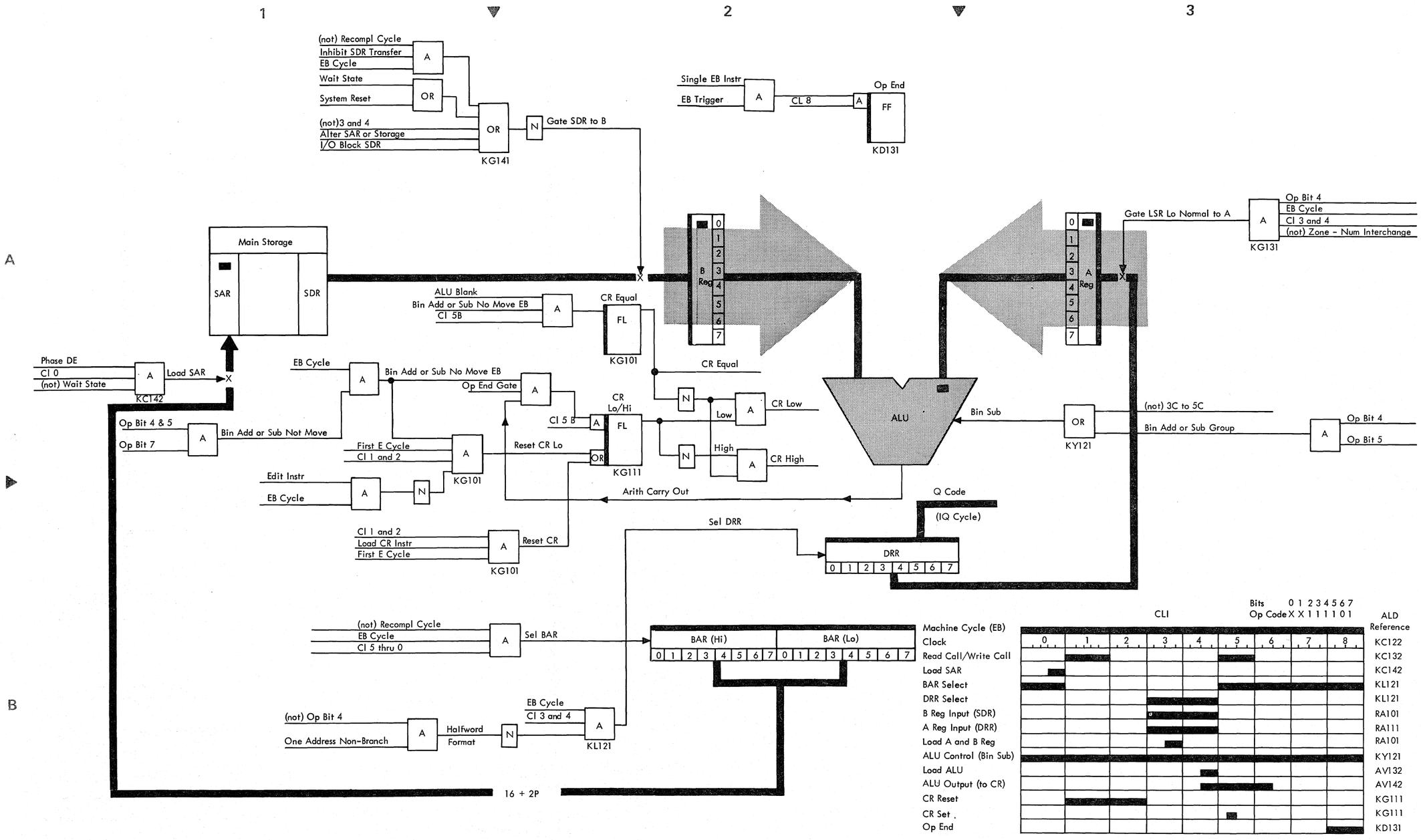
1. Move Characters — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 1 1 0 0
   - Move the contents of the A field to the B field
2. Compare Logical Chars. — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 1 1 0 1
   - Compare the A field data with the B field data
3. Add Logical Characters — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 1 1 1 0
   - Binary add the A field data to the B field data and store results in B field location
4. Subtract Logical Characters — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 1 1 1 1
   - Binary subtract the A field data from the B field data and store results in B field location
5. All Operations
   - A and B fields are same length
   - Length of field is Q code plus 1
   - Set Condition Register except during move operation




1
2
3
A
B
Wait State
System Reset
Cl 5 and 6
Gate LSR Lo to B
EB Cycle
(not) Recompl Cycle
Inhibit SDR Transfer
Wait State
System Reset
(not) Cl 3 and 4 Time
I/O Block SDR
Alter SAR or Storage
KG141
Gate SDR to B
Cl 1 and 2
EB Cycle
Cl 7 and 8
Wait State
System Reset
Gate LSR Hi to B
2 Address Format
(not) Recompl Gate
Q Reg Blank
Cl 8
Op End
FF
KD131
B Reg
A Reg
Gate LSR Low Normal to A
Op Bit 4
EB Cycle
Cl 3 and 4
(not) Zone - Num Interchange
KG131
Recompl Cycle
(not) Q Num Blank
EA Eliminate
Dec Instr
EB not 1st Cycle
2 Address Format
Cl 1 and 2
Cl 5 and 6
(not) IR Prog Backup
KG141
Force Bit 7 to A
Bin Compl A Reg
I/O Cycle Not Test
CE Test No Incre
Wait State
System Reset
(not) 3C to 5C
Binary Add or Sub Group
Bin Sub Gate
KY121
ALU
FL
Odd CD
KY121
EB 3C to 5C
Bin Add Group
LSR Write High
(not) Op Bit 7
Op Bit 4
Op Bit 5
KY121
LSR Write Low
Cl 2
EB Cycle
Cl 8
Channel Inhibit LSR Load
I/O Not CE Test
Idle Time
A or B Reg Chk
LSR to A or B
Phase D
KL101
Cl 6
Cl 4
(not) EB Cycle
(not) IH Cycle
(not) Alter or Display Storage
Main Storage
SAR
SDR
Op Bit 4
Op Bit 5
EB Cycle
RN131
Sel LCR and DRR
LCR
DRR
Phase DE
Cl 0
(not) Wait State
Load SAR
KC142
16 + 2P
Store New
Op Bit 6
Not Op Bit 7
(not) Test on or Off
(not) Op Bit 6
RN131
(not) Halfword Format
EB Cycle
(not) Significant Digit
(not) Edit Instr
Store Data Group
KY111
New Data to Store
Cl 4 CD
Cl 6
FL
KC132
Not Recompl
EB Cycle
Cl 1 and 2
EA Cycle
EB Cycle
Cl 3 and 4
(not) Op Bit 4
One Address Instr
Halfword Format
KL121
Q Reg Blank
Q Reg
Load Q Reg
Odd Not 9 CD
EB Cycle
Cl 3 and 4
2 Address Format
(not) Single EBB Cycle Instr
KD141
AAR (Hi)
AAR (Lo)
BAR (Hi)
BAR (Lo)
EQ
Lo/Hi
Bin Ovfl
Dec Ovfl
Test False
Cond Reg
AAR Sel
BAR Sel
EA Cycle
Cl 5 Thru 0
Not Inhibit LSR Select
KL121
EB Cycle
Cl 5 Thru 0
(not) Recompl Cycle
KL121



Condition Register				
Operation	Equal	Low	High	Binary Overflow
Move				
Add	If Result is zero	If Result not zero and a high order carry	If Result not zero and no high order carry	Result too large for field (no high order carry)
Subtract	If A field equals B field	If B field is lower than A field	If B field is higher than A field	
Compare	If A field equals B field	If B field is lower than A field	If B field is higher than A field	


1
2
3
A
B
(not) Recompl Cycle
Inhibit SDR Transfer
EB Cycle
Wait State
System Reset
(not)3 and 4
Alter SAR or Storage
I/O Block SDR
A
OR
OR
N
KG141
Gate SDR to B
Single EB Instr
EB Trigger
A
CL 8
A
Op End
FF
KD131
Main Storage
SAR
SDR
X
B Reg
0 1 2 3 4 5 6 7
ALU Blank
Bin Add or Sub No Move EB
Cl 5B
A
CR Equal
FL
KG101
CR Equal
Phase DE
Cl 0
(not) Wait State
A
Load SAR
X
KC142
EB Cycle
A
Bin Add or Sub No Move EB
Op End Gate
A
CR Lo/Hi
Cl 5 B
A
FL
KG111
N
Low
A
CR Low
N
High
A
CR High
Op Bit 4 & 5
Op Bit 7
A
Bin Add or Sub Not Move
First E Cycle
Cl 1 and 2
A
KG101
Reset CR Lo
OR
Edit Instr
EB Cycle
A
N
KG101
Arith Carry Out
ALU
Bin Sub
OR
KY121
(not) 3C to 5C
Bin Add or Sub Group
A
Op Bit 4
Op Bit 5
Gate LSR Lo Normal to A
A
Op Bit 4
EB Cycle
Cl 3 and 4
(not) Zone - Num Interchange
KG131
A Reg
0 1 2 3 4 5 6 7
Q Code
(IQ Cycle)
Sel DRR
DRR
0 1 2 3 4 5 6 7
Cl 1 and 2
Load CR Instr
First E Cycle
A
Reset CR
KG101
(not) Recompl Cycle
EB Cycle
Cl 5 thru 0
A
Sel BAR
BAR (Hi)
BAR (Lo)
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
(not) Op Bit 4
One Address Non-Branch
A
Halfword Format
N
EB Cycle
Cl 3 and 4
A
KL121
16 + 2P
Bits 0 1 2 3 4 5 6 7
Op Code X X 1 1 1 1 0 1
CLI
ALD Reference
Machine Cycle (EB)
Clock
Read Call/Write Call
Load SAR
BAR Select
DRR Select
B Reg Input (SDR)
A Reg Input (DRR)
Load A and B Reg
ALU Control (Bin Sub)
Load ALU
ALU Output (to CR)
CR Reset
CR Set
Op End
0 1 2 3 4 5 6 7 8
KC122
KC132
KC142
KL121
KL121
RA101
RA111
RA101
KY121
AV132
AV142
KG111
KG111
KD131

1

Objectives

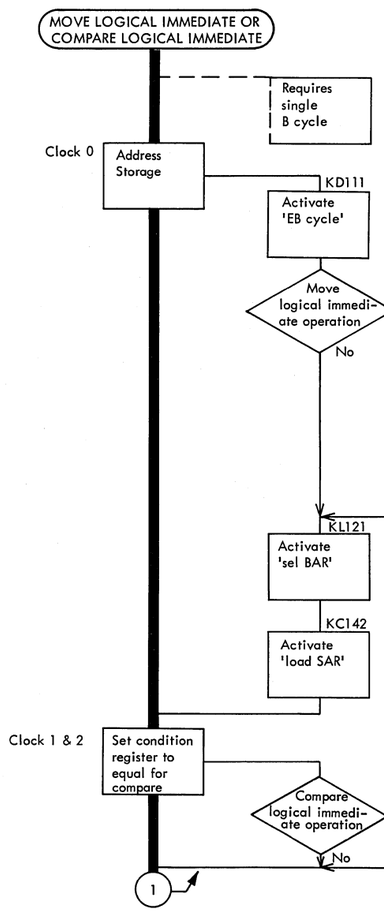
		bits 0 1 2 3 4 5 6 7
Move Logical Immediate	Op Code	X X 1 1 1 1 0 0

- Store the Q code, which is located in the Data Recall Register, in the location specified by the B Address Register

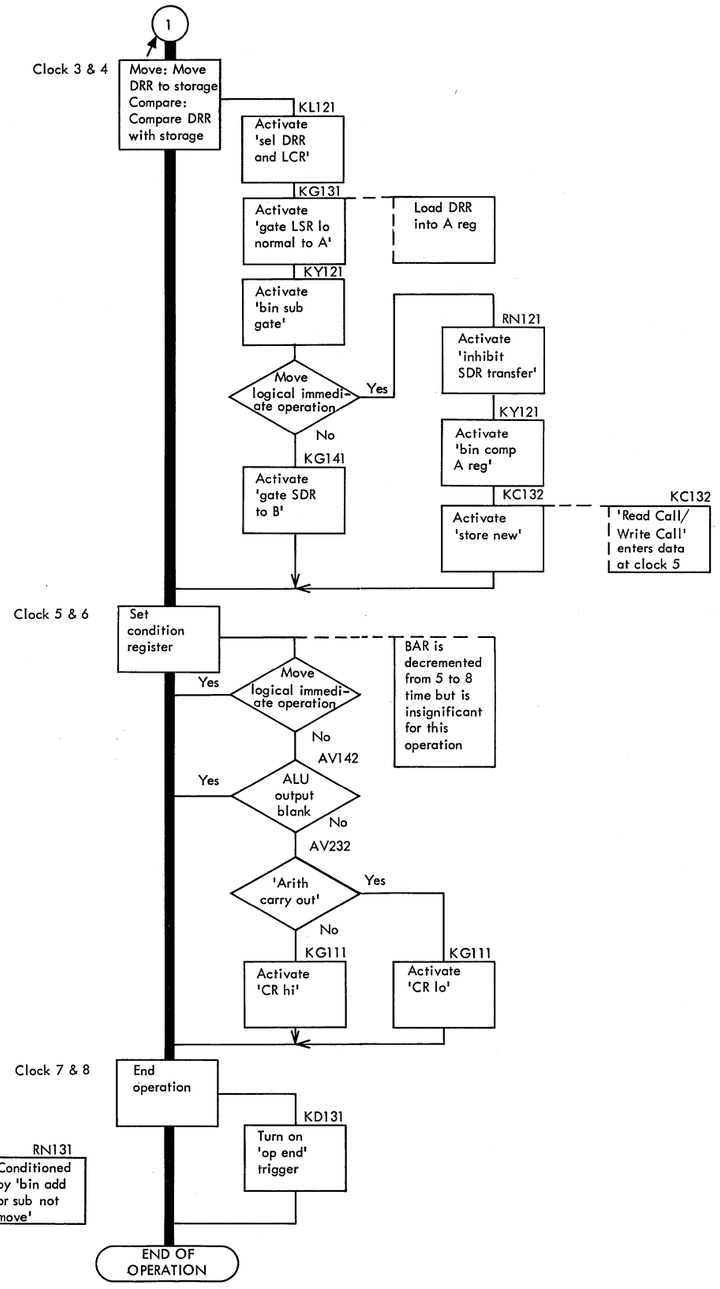
		bits 0 1 2 3 4 5 6 7
Compare Logical Immediate	Op Code	X X 1 1 1 1 0 1

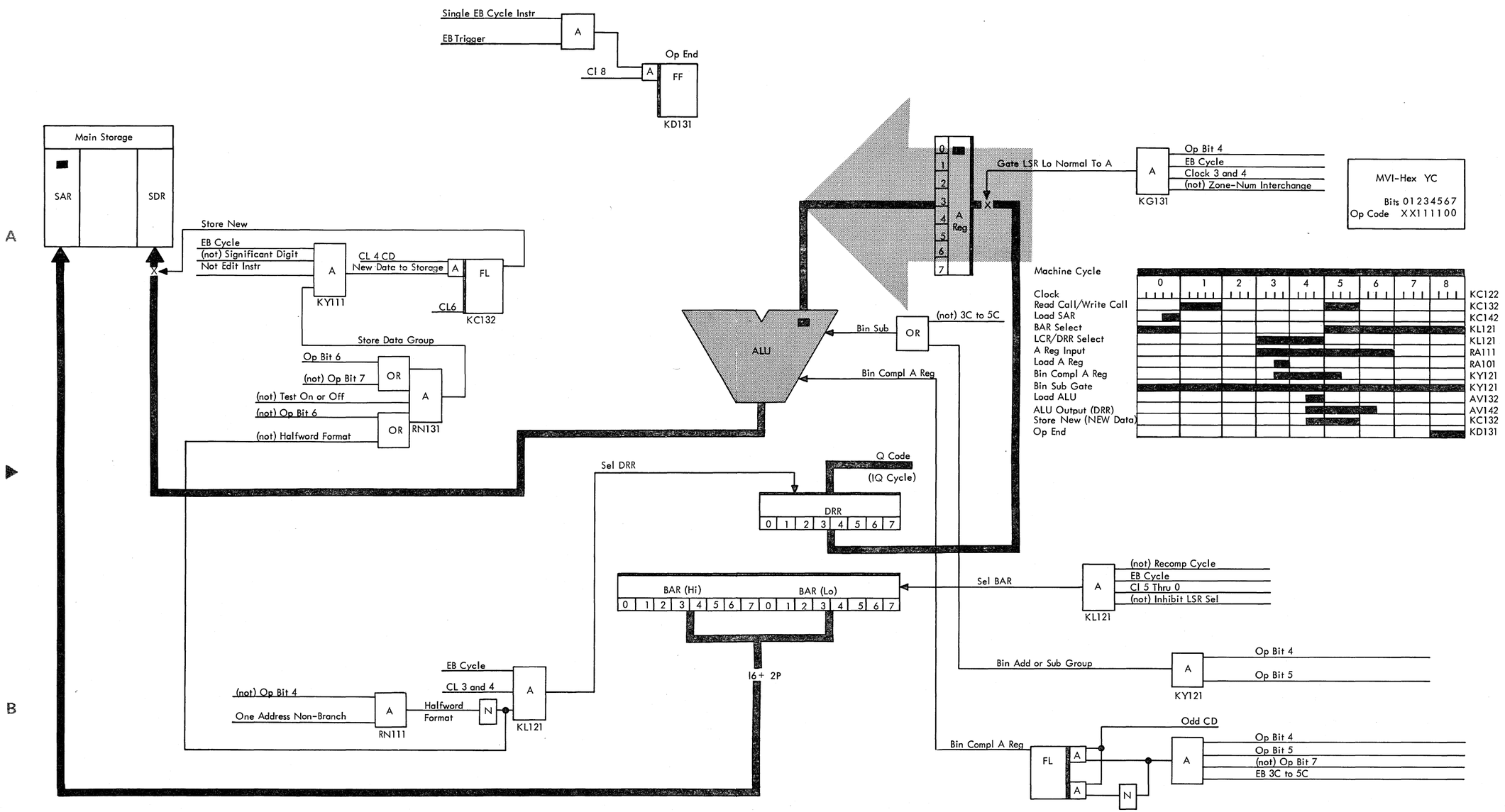
- Compare the Q code, which is located in the Data Recall Register, with the data in the location specified by the B Address Register
- Record the result of the comparison in the Condition Register

A



B



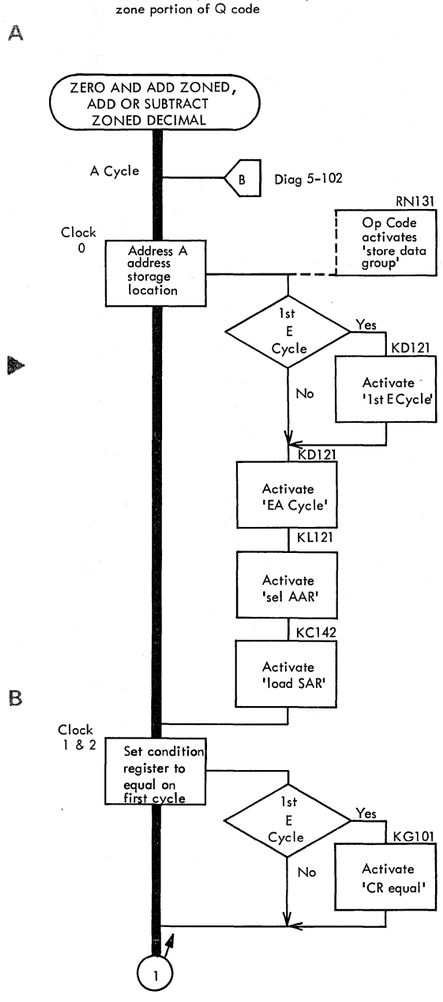

Single EB Cycle Instr
EB Trigger
A
Op End
CI 8
A
FF
KD131
Main Storage
SAR
SDR
A
Store New
EB Cycle
(not) Significant Digit
Not Edit Instr
A
KY111
CL 4 CD
New Data to Storage
A
FL
CL6
KC132
Store Data Group
Op Bit 6
(not) Op Bit 7
OR
(not) Test On or Off
(not) Op Bit 6
OR
A
RN131
(not) Halfword Format
0 1 2 3 4 5 6 7
A Reg
X
Gate LSR Lo Normal To A
A
KG131
Op Bit 4
EB Cycle
Clock 3 and 4
(not) Zone-Num Interchange
MVI-Hex YC
Bits 01234567
Op Code XX111100
Machine Cycle
0 1 2 3 4 5 6 7 8
Clock KC122
Read Call/Write Call KC132
Load SAR KC142
BAR Select KL121
LCR/DRR Select KL121
A Reg Input RA111
Load A Reg RA101
Bin Compl A Reg KY121
Bin Sub Gate KY121
Load ALU AV132
ALU Output (DRR) AV142
Store New (NEW Data) KC132
Op End KD131
ALU
Bin Sub
OR
(not) 3C to 5C
Bin Compl A Reg
Sel DRR
Q Code
(IQ Cycle)
DRR
0 1 2 3 4 5 6 7
BAR (Hi)
BAR (Lo)
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
16÷ 2P
Sel BAR
A
KL121
(not) Recomp Cycle
EB Cycle
CI 5 Thru 0
(not) Inhibit LSR Sel
Bin Add or Sub Group
A
KY121
Op Bit 4
Op Bit 5
EB Cycle
CL 3 and 4
(not) Op Bit 4
One Address Non-Branch
A
RN111
Halfword Format
N
A
KL121
Bin Compl A Reg
FL
A
A
N
Odd CD
A
Op Bit 4
Op Bit 5
(not) Op Bit 7
EB 3C to 5C

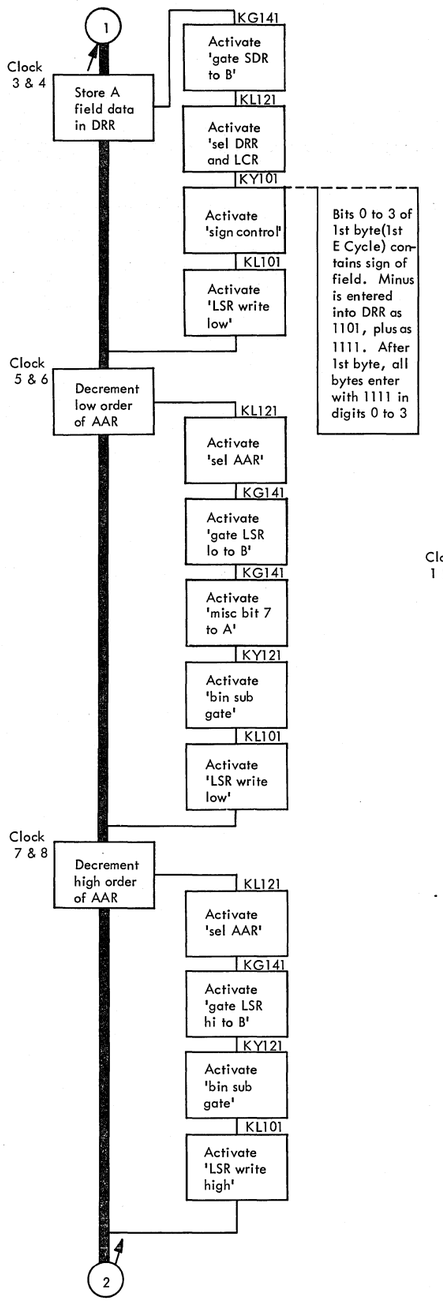
Objectives:

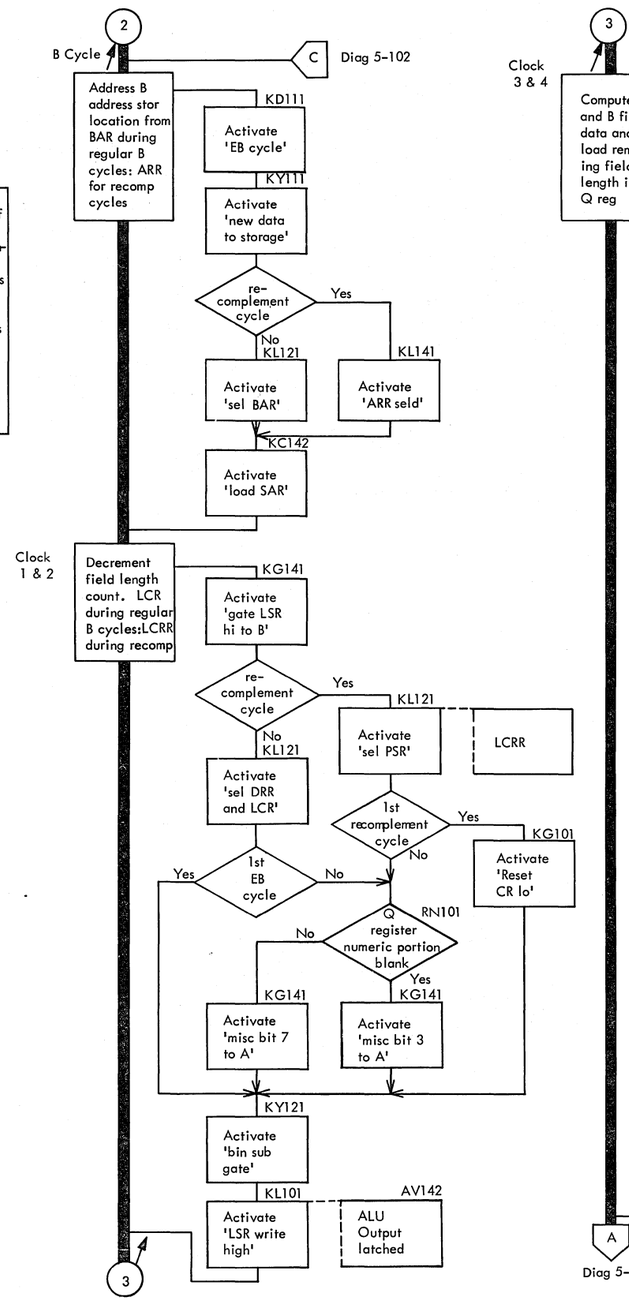
1. Zero and Add Zoned — bits 0 1 2 3 4 5 6 7, Op Code X X X X 0 1 0 0
   - Decimally add A field data to zeros and place results in B field location

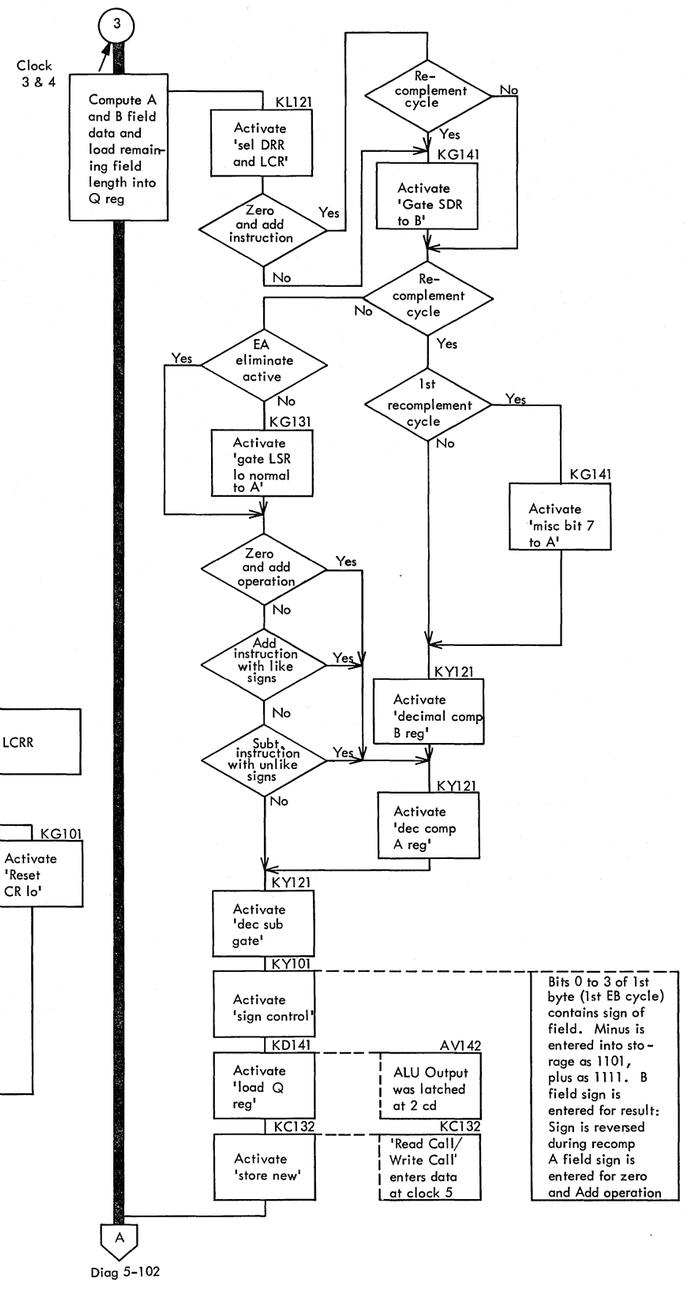
2. Add Zoned Decimal — bits 0 1 2 3 4 5 6 7, Op Code X X X X 0 1 1 0
   Subtract Zoned Decimal — X X X X 0 1 1 1
   - Decimally add A field data to B field or subtract A field data from B field
   - Instruction and signs of fields determine add or subtract function

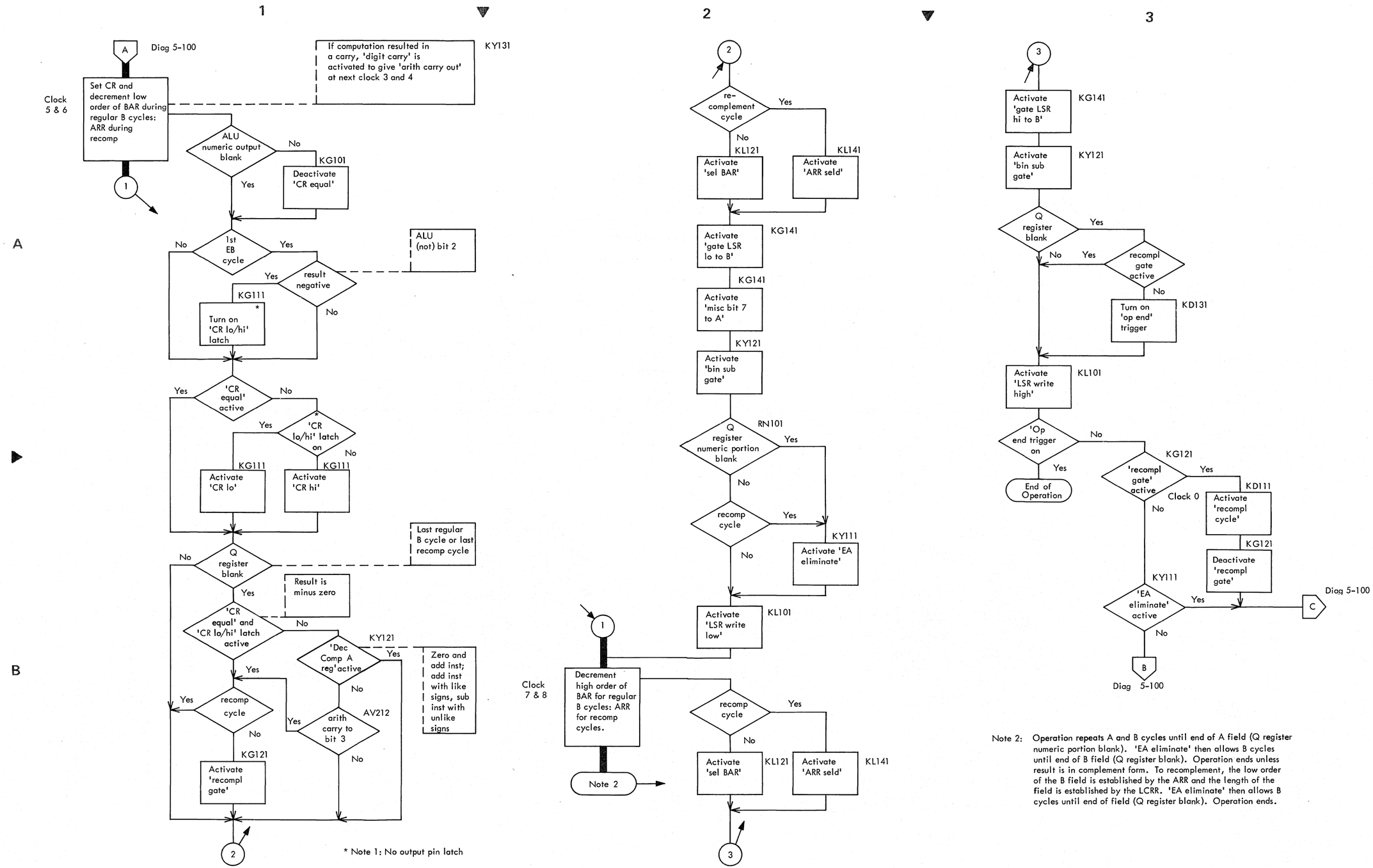
3. All Operations
   - Length of A field is numeric portion of Q code + 1
   - B field is longer than A field by amount in zone portion of Q code





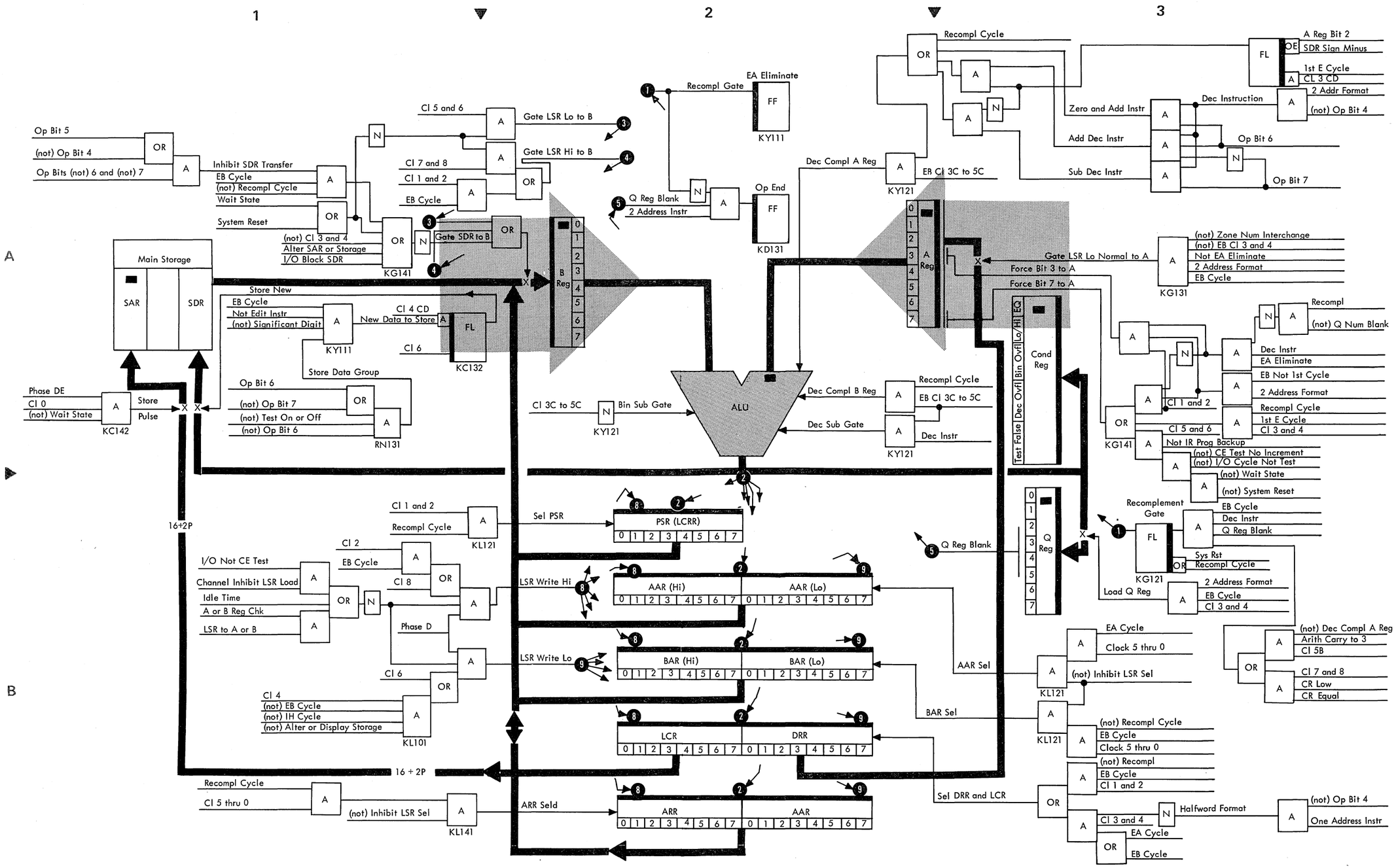


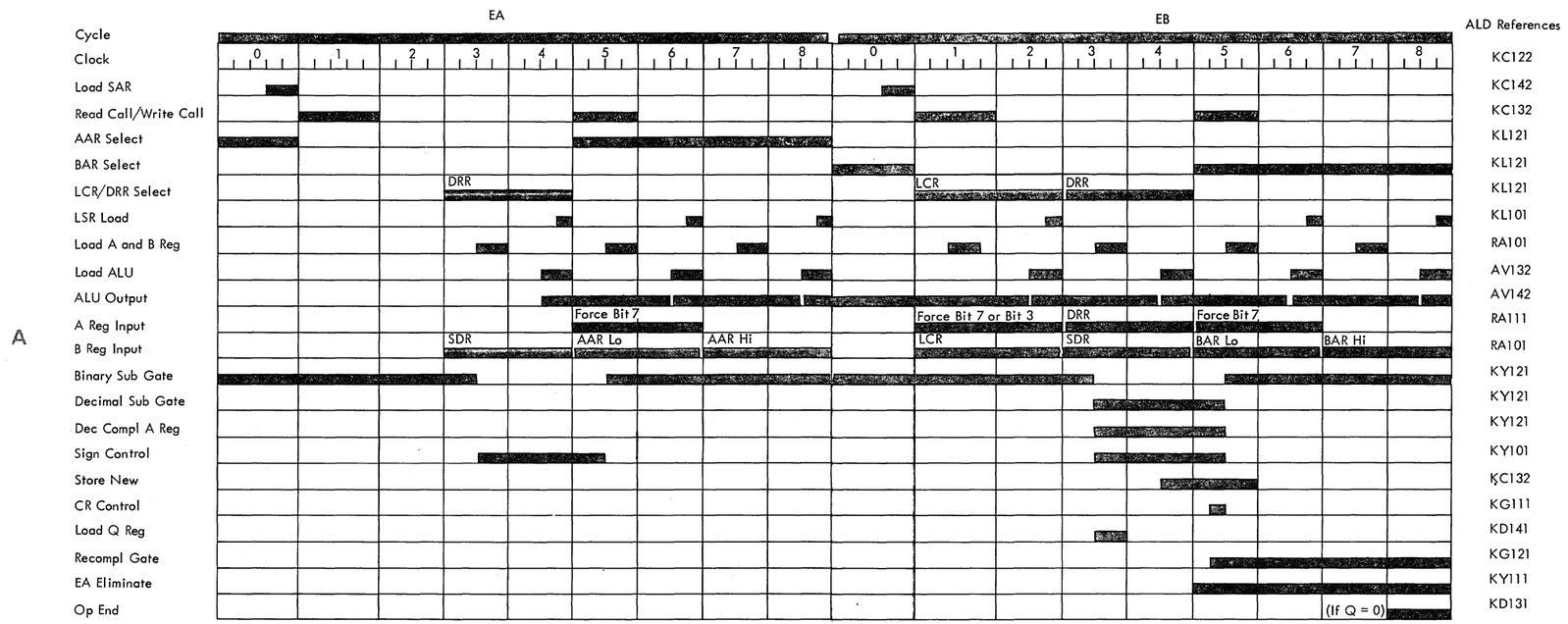




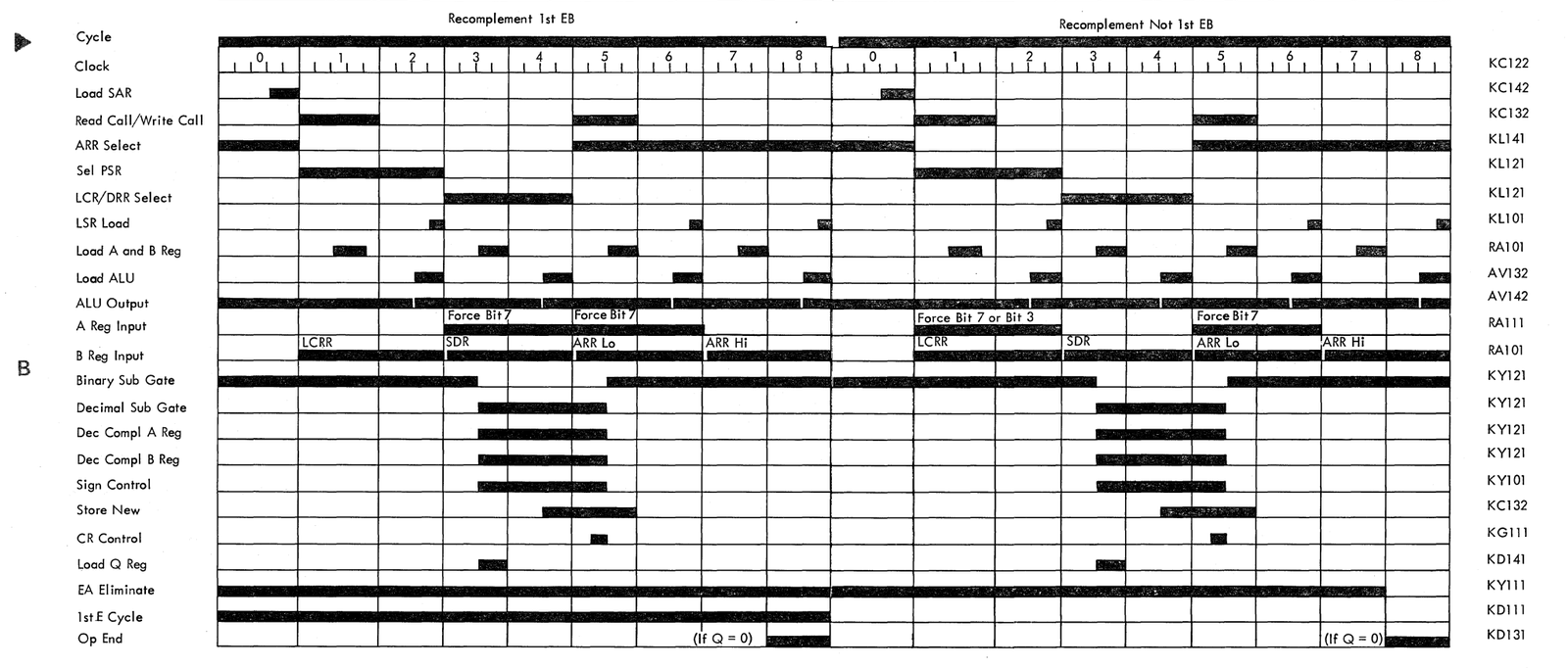
Note 2: Operation repeats A and B cycles until end of A field (Q register numeric portion blank). 'EA eliminate' then allows B cycles until end of B field (Q register blank). Operation ends unless result is in complement form. To recomplement, the low order of the B field is established by the ARR and the length of the field is established by the LCRR. 'EA eliminate' then allows B cycles until end of field (Q register blank). Operation ends.

5406 CPU–Operations
Zero and Add Zoned and Add or Subtract Zoned Decimal (Part 2 of 4)


1
2
3
A
B
Op Bit 5
(not) Op Bit 4
Op Bits (not) 6 and (not) 7
OR
A
Inhibit SDR Transfer
EB Cycle
(not) Recompl Cycle
Wait State
System Reset
(not) Cl 3 and 4
Alter SAR or Storage
I/O Block SDR
KG141
Cl 5 and 6
Cl 7 and 8
Cl 1 and 2
EB Cycle
Gate LSR Lo to B
Gate LSR Hi to B
Gate SDR to B
N
Recompl Gate
EA Eliminate
FF
KY111
Q Reg Blank
2 Address Instr
Op End
KD131
Dec Compl A Reg
EB Cl 3C to 5C
KY121
Recompl Cycle
Zero and Add Instr
Add Dec Instr
Sub Dec Instr
Dec Instruction
Op Bit 6
Op Bit 7
2 Addr Format
(not) Op Bit 4
A Reg Bit 2
SDR Sign Minus
1st E Cycle
CL 3 CD
FL
OE
Main Storage
SAR
SDR
Store New
EB Cycle
Not Edit Instr
(not) Significant Digit
Cl 4 CD
New Data to Store
Cl 6
KY111
KC132
Store Data Group
Op Bit 6
(not) Op Bit 7
(not) Test On or Off
(not) Op Bit 6
RN131
B Reg
A Reg
Gate LSR Lo Normal to A
Force Bit 3 to A
Force Bit 7 to A
(not) Zone Num Interchange
(not) EB Cl 3 and 4
Not EA Eliminate
2 Address Format
EB Cycle
KG131
Phase DE
Cl 0
(not) Wait State
Store
Pulse
KC142
Cl 3C to 5C
Bin Sub Gate
KY121
ALU
Dec Compl B Reg
Dec Sub Gate
Dec Instr
Test False
Dec Ovfl
Bin Ovfl
Lo/Hi
EQ
Cond Reg
Recompl
(not) Q Num Blank
Dec Instr
EA Eliminate
EB Not 1st Cycle
2 Address Format
Recompl Cycle
1st E Cycle
Cl 3 and 4
Cl 1 and 2
Cl 5 and 6
Not IR Prog Backup
(not) CE Test No Increment
(not) I/O Cycle Not Test
(not) Wait State
(not) System Reset
EB Cycle
Dec Instr
Q Reg Blank
Recomplement Gate
Sys Rst
Recompl Cycle
Load Q Reg
2 Address Format
EB Cycle
Cl 3 and 4
KG121
16+2P
Cl 1 and 2
Recompl Cycle
KL121
Sel PSR
PSR (LCRR)
Cl 2
EB Cycle
I/O Not CE Test
Channel Inhibit LSR Load
Idle Time
A or B Reg Chk
LSR to A or B
Cl 8
Phase D
Cl 6
Cl 4
(not) EB Cycle
(not) IH Cycle
(not) Alter or Display Storage
KL101
LSR Write Hi
LSR Write Lo
AAR (Hi)
AAR (Lo)
BAR (Hi)
BAR (Lo)
LCR
DRR
ARR
AAR
ARR Seld
Recompl Cycle
Cl 5 thru 0
(not) Inhibit LSR Sel
KL141
16 + 2P
Q Reg
Q Reg Blank
AAR Sel
BAR Sel
Sel DRR and LCR
EA Cycle
Clock 5 thru 0
(not) Inhibit LSR Sel
KL121
(not) Dec Compl A Reg
Arith Carry to 3
Cl 5B
Cl 7 and 8
CR Low
CR Equal
(not) Recompl Cycle
EB Cycle
Clock 5 thru 0
(not) Recompl
EB Cycle
Cl 1 and 2
Halfword Format
Cl 3 and 4
EA Cycle
EB Cycle
(not) Op Bit 4
One Address Instr



Condition Register				
Operation	Equal	Low	High	Decimal Ovfl
Zero and Add Zoned	Result is Zero	Result is Minus	Result is Plus	———
Add or Sub Zoned	Result is Zero	Result is Minus	Result is Plus	Result is too large for field



Objectives:

bits 0 1 2 3 4 5 6 7
Edit Op Code X X X X 1 0 1 0

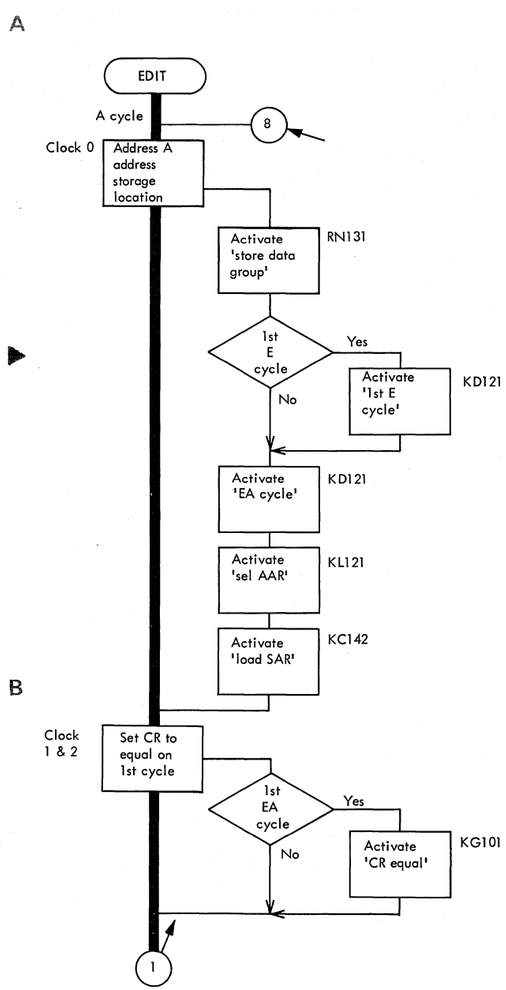
- Replace hex 2/0 in B field with A field data
- Skip other characters in B field leaving them as they were
- Length of B field is Q code + 1
- A field sign stored in condition register

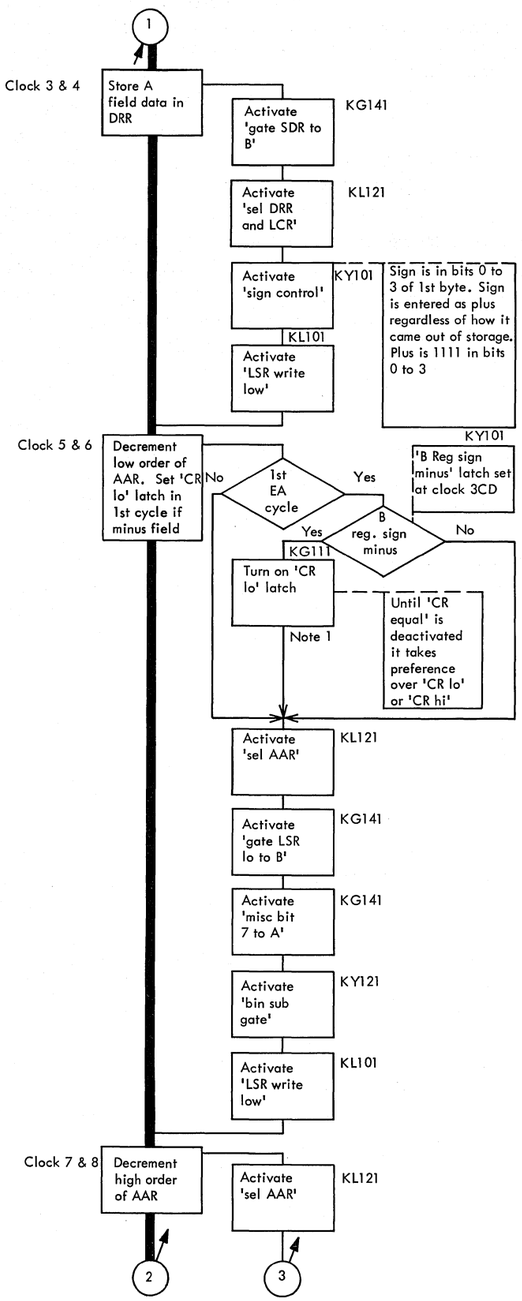
EXAMPLE:

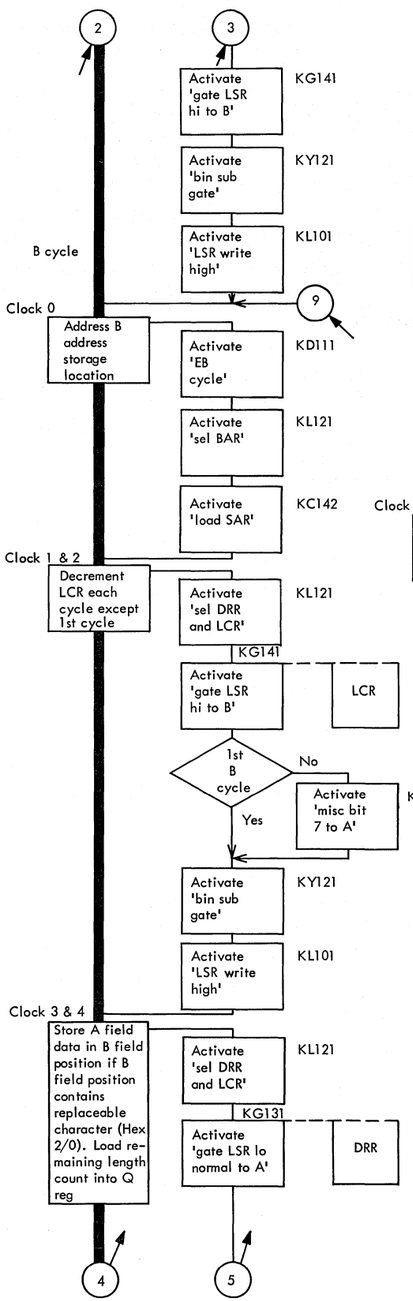
Q code = 9

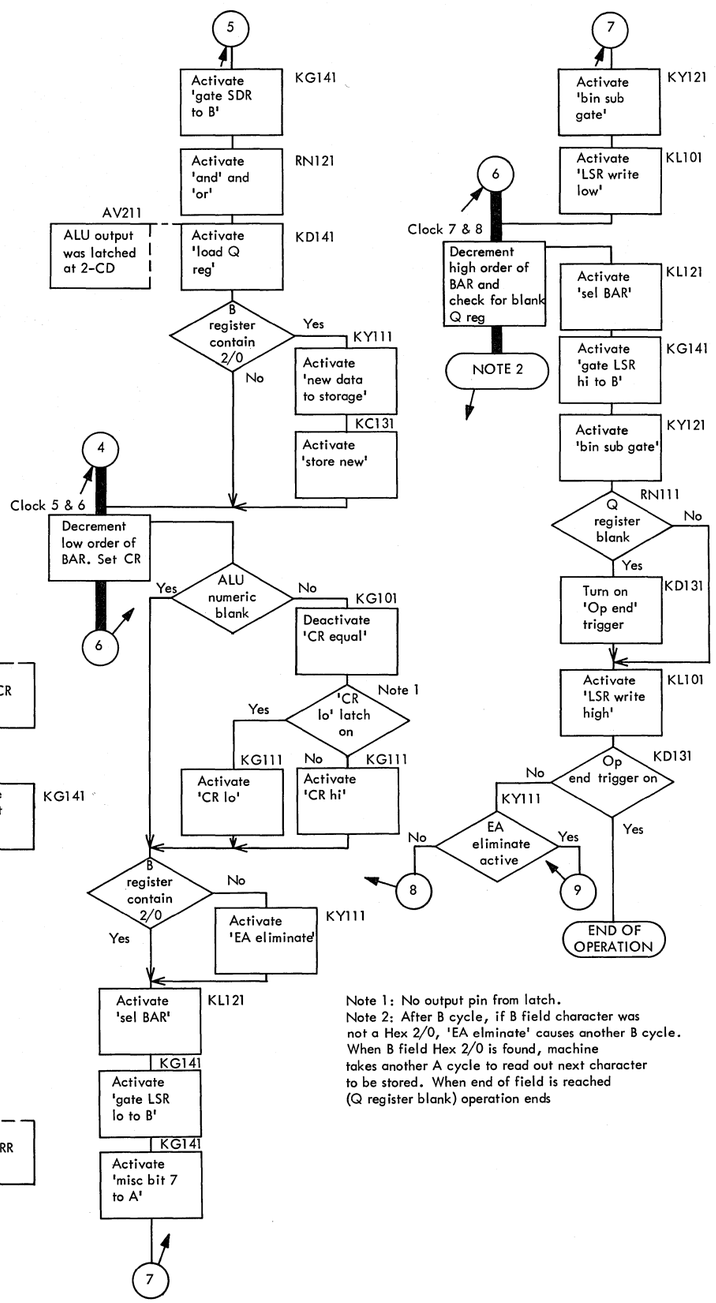
B field before edit	X,XXX.XX	
A field	090715	blank
B field after edit	0,907.15	

X=Replaceable Character (2/0)

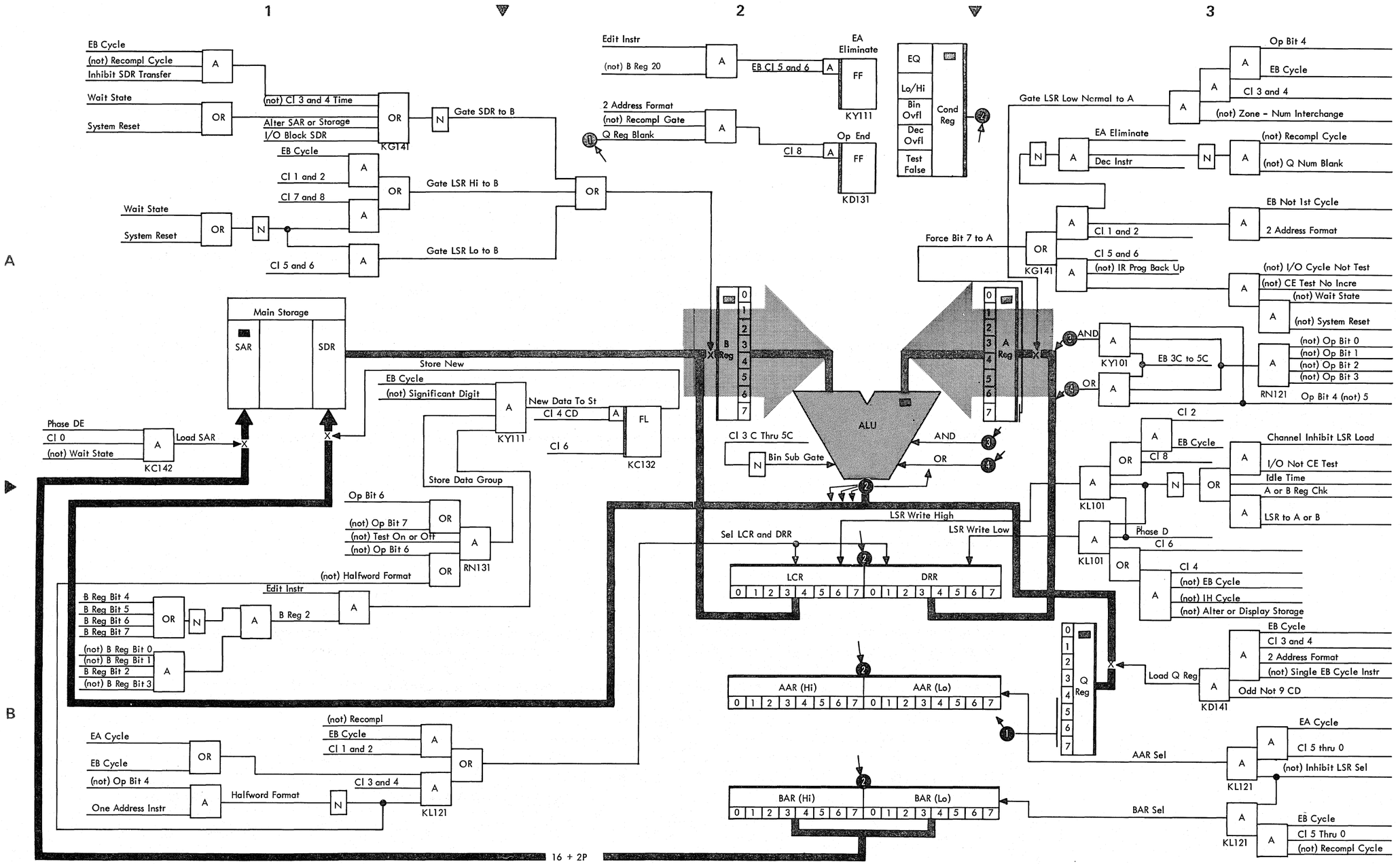


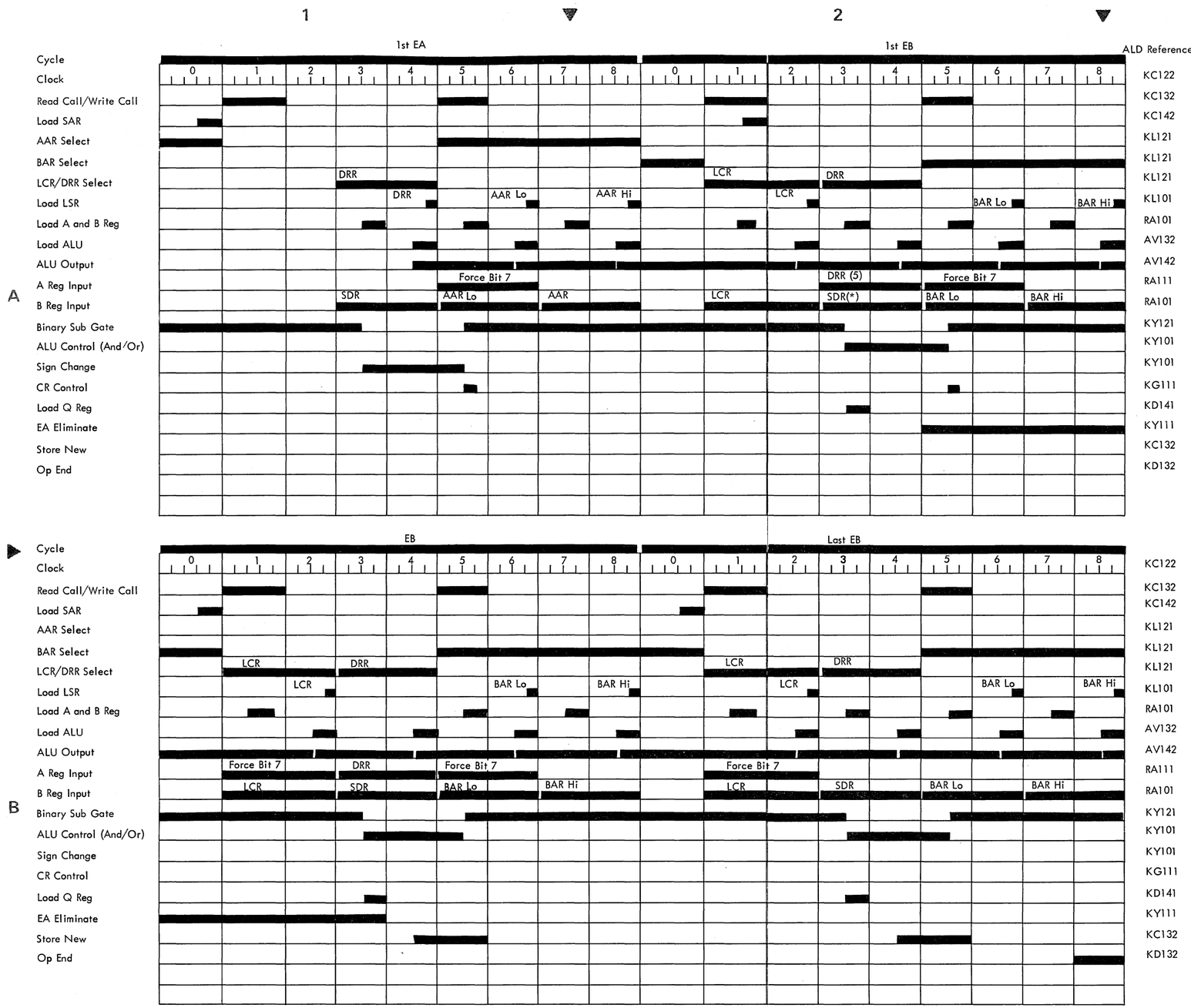






Note 1: No output pin from latch.
Note 2: After B cycle, if B field character was not a Hex 2/0, 'EA elminate' causes another B cycle. When B field Hex 2/0 is found, machine takes another A cycle to read out next character to be stored. When end of field is reached (Q register blank) operation ends


1
2
3
A
B
EB Cycle
(not) Recompl Cycle
Inhibit SDR Transfer
Wait State
System Reset
OR
A
(not) Cl 3 and 4 Time
Alter SAR or Storage
I/O Block SDR
KG141
N
Gate SDR to B
EB Cycle
Cl 1 and 2
Cl 7 and 8
Gate LSR Hi to B
Gate LSR Lo to B
Cl 5 and 6
Edit Instr
(not) B Reg 20
EB Cl 5 and 6
EA Eliminate
FF
KY111
2 Address Format
(not) Recompl Gate
Q Reg Blank
Op End
Cl 8
KD131
EQ
Lo/Hi
Bin Ovfl
Dec Ovfl
Test False
Cond Reg
Gate LSR Low Normal to A
Op Bit 4
EB Cycle
Cl 3 and 4
(not) Zone - Num Interchange
EA Eliminate
Dec Instr
(not) Recompl Cycle
(not) Q Num Blank
Force Bit 7 to A
EB Not 1st Cycle
2 Address Format
Cl 1 and 2
Cl 5 and 6
(not) IR Prog Back Up
KG141
(not) I/O Cycle Not Test
(not) CE Test No Incre
(not) Wait State
(not) System Reset
Main Storage
SAR
SDR
Store New
B Reg
A Reg
ALU
AND
OR
KY101
EB 3C to 5C
(not) Op Bit 0
(not) Op Bit 1
(not) Op Bit 2
(not) Op Bit 3
RN121
Op Bit 4 (not) 5
Phase DE
Cl 0
(not) Wait State
Load SAR
KC142
EB Cycle
(not) Significant Digit
New Data To St
Cl 4 CD
FL
Cl 6
KC132
Cl 3 C Thru 5C
Bin Sub Gate
Cl 2
Channel Inhibit LSR Load
I/O Not CE Test
Idle Time
A or B Reg Chk
LSR to A or B
KL101
Store Data Group
Op Bit 6
(not) Op Bit 7
(not) Test On or Off
(not) Op Bit 6
(not) Halfword Format
RN131
Sel LCR and DRR
LSR Write High
LSR Write Low
LCR
DRR
Phase D
Cl 6
Cl 4
(not) EB Cycle
(not) IH Cycle
(not) Alter or Display Storage
B Reg Bit 4
B Reg Bit 5
B Reg Bit 6
B Reg Bit 7
(not) B Reg Bit 0
(not) B Reg Bit 1
B Reg Bit 2
(not) B Reg Bit 3
Edit Instr
B Reg 2
AAR (Hi)
AAR (Lo)
Q Reg
Load Q Reg
EB Cycle
Cl 3 and 4
2 Address Format
(not) Single EB Cycle Instr
Odd Not 9 CD
KD141
(not) Recompl
EB Cycle
Cl 1 and 2
EA Cycle
EB Cycle
(not) Op Bit 4
One Address Instr
Halfword Format
Cl 3 and 4
KL121
EA Cycle
Cl 5 thru 0
(not) Inhibit LSR Sel
AAR Sel
BAR (Hi)
BAR (Lo)
BAR Sel
EB Cycle
Cl 5 Thru 0
(not) Recompl Cycle
16 + 2P



Cycle	A	B	B	B	A	B	A	B	B	A	B	A	B	A	B	B
B Register	5	*	bl	X	1	X	7	·	X	0	X	9	X	0	,	X
A Register			5	5	5		1		7	7		0		9		0	0
Data Recall Register	5		5	5	5	1	1	7	7	7	0	0	9	9	0	0	0
Regenerate	5		*	bl		1		7	·		0		9		0	,	
New Data					5		1			7		0		9			0
Length Count	9		9	8	7	7		6	6	5	4	4	3	3	2	2	1	0

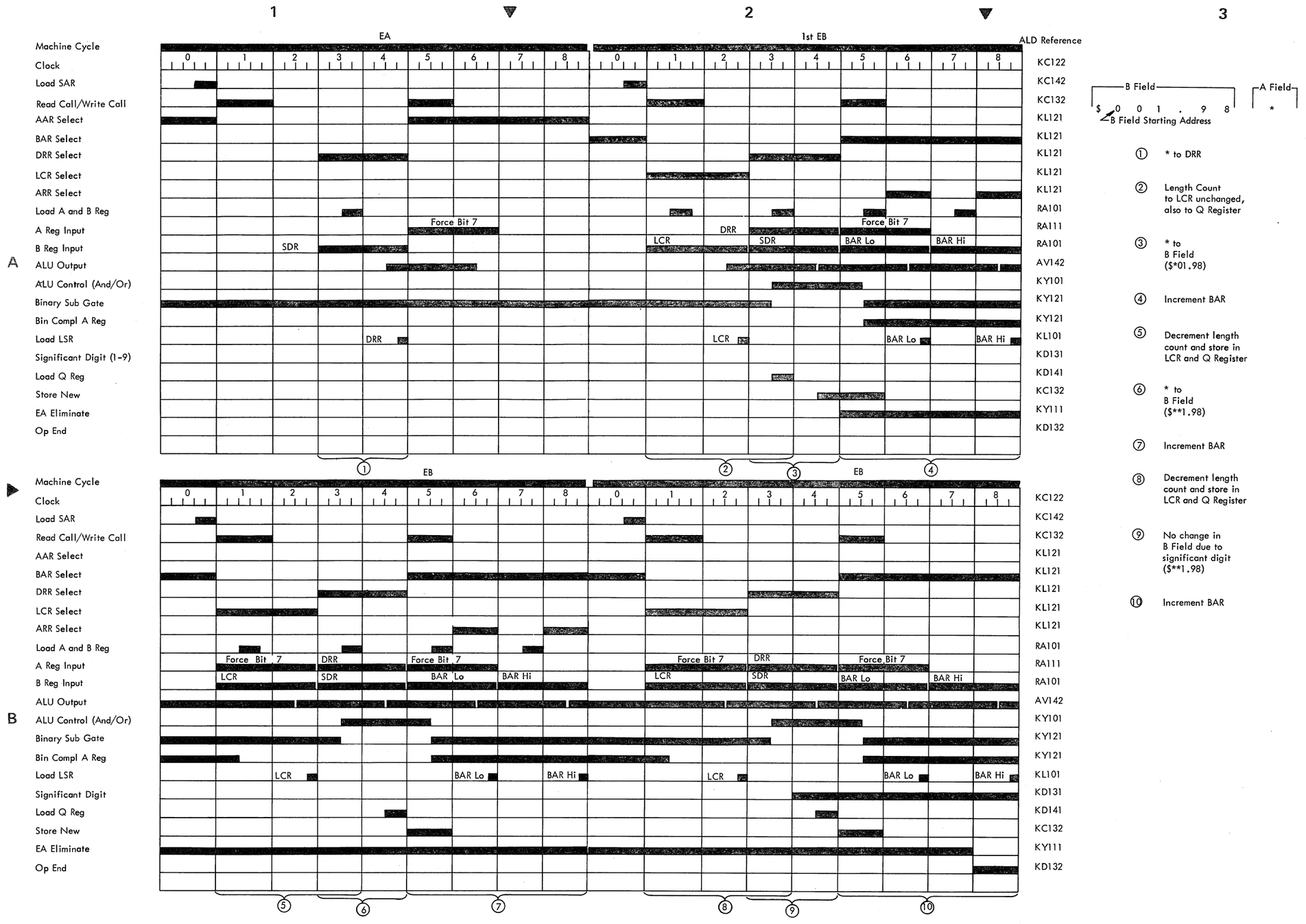
X = Replaceable Character

A Field 090715

B Field before edit X,XXX.XX *

B Field after edit 0,907.15 *
blank

Note: Since the A and B registers are loaded each odd CD clock time, the figures shown apply only to clock 3 and 4 time when the main storage data is being analyzed.



5406 CPU–Operations
Insert and Test Characters (Part 1 of 3)

1

Objectives:

	bits 0 1 2 3 4 5 6 7
Insert and Test Character Op Code	X X X X 1 0 1 1

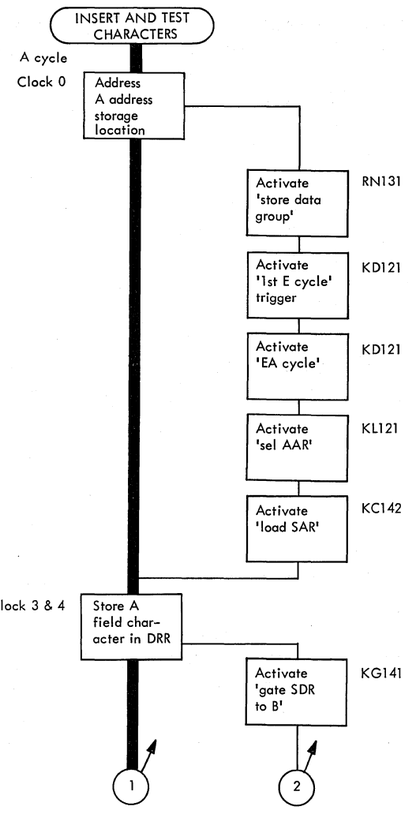
- Replace all characters to left of first significant digit in B field with A field character
- Only numeric characters 1 to 9 are considered significant digits
- Length of B field is Q code + 1
- A field is only 1 character in length

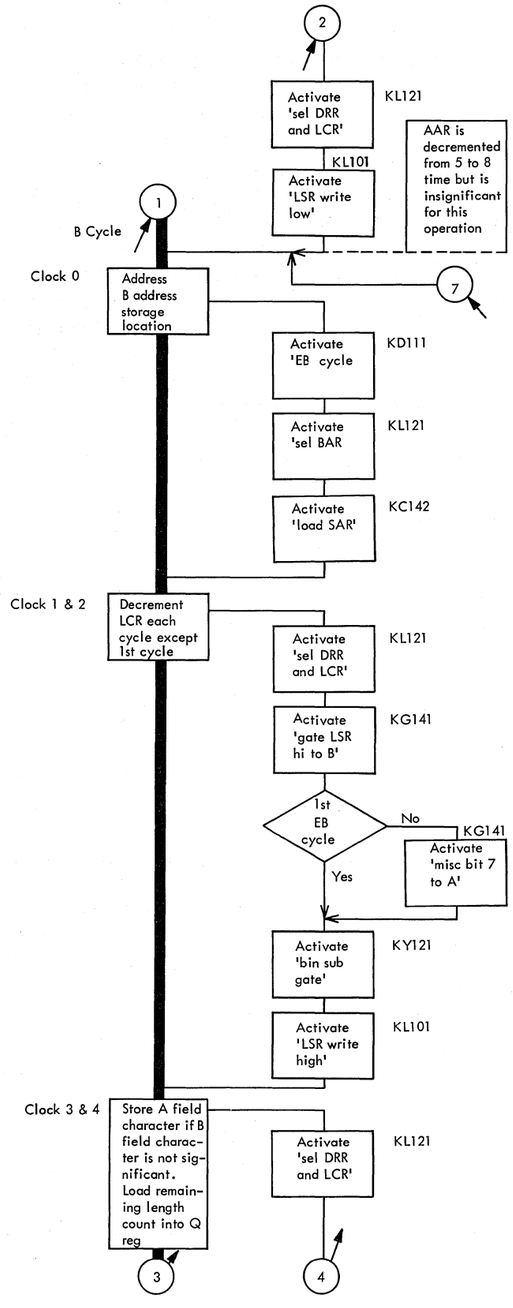
EXAMPLE:

Edited field before operation 0,907.15 *
A field character *
Edited field after operation **907.15 *
B field starting address

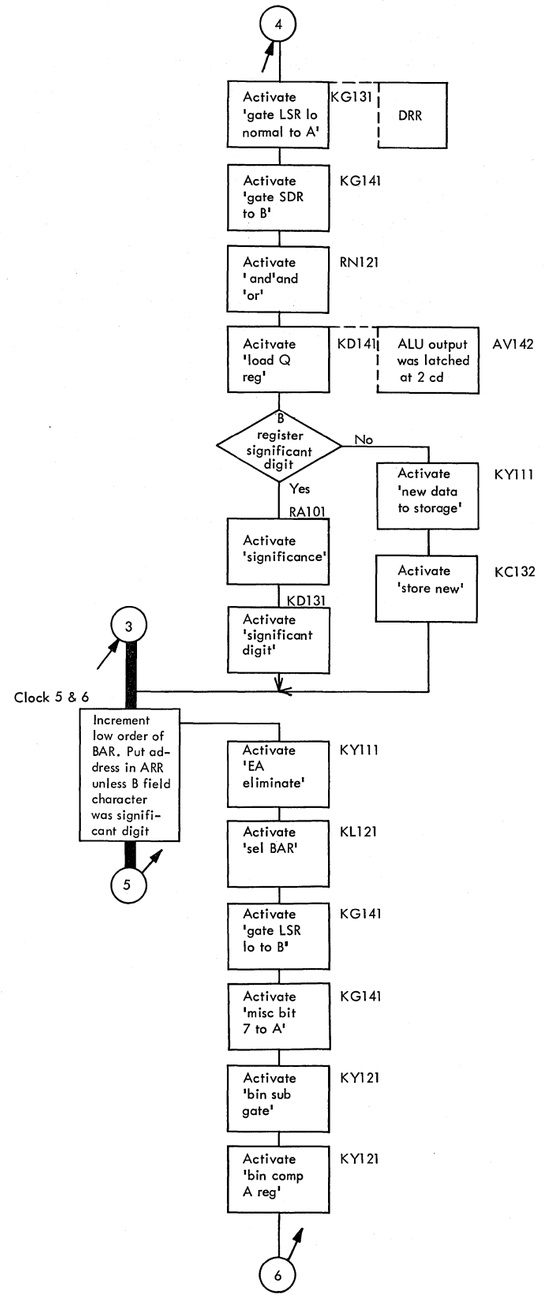
blank

A

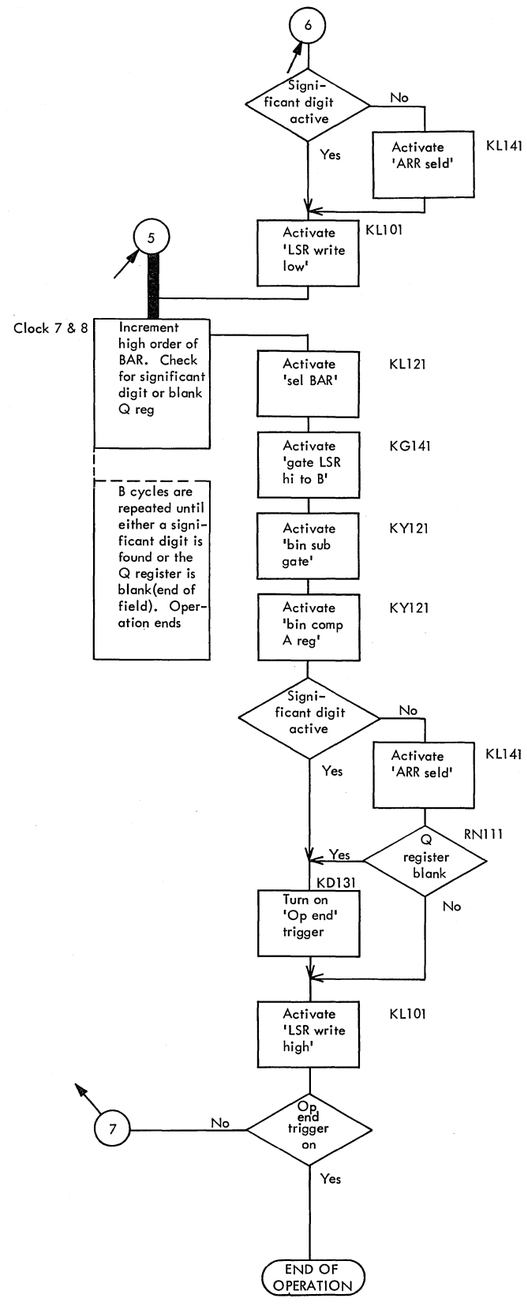


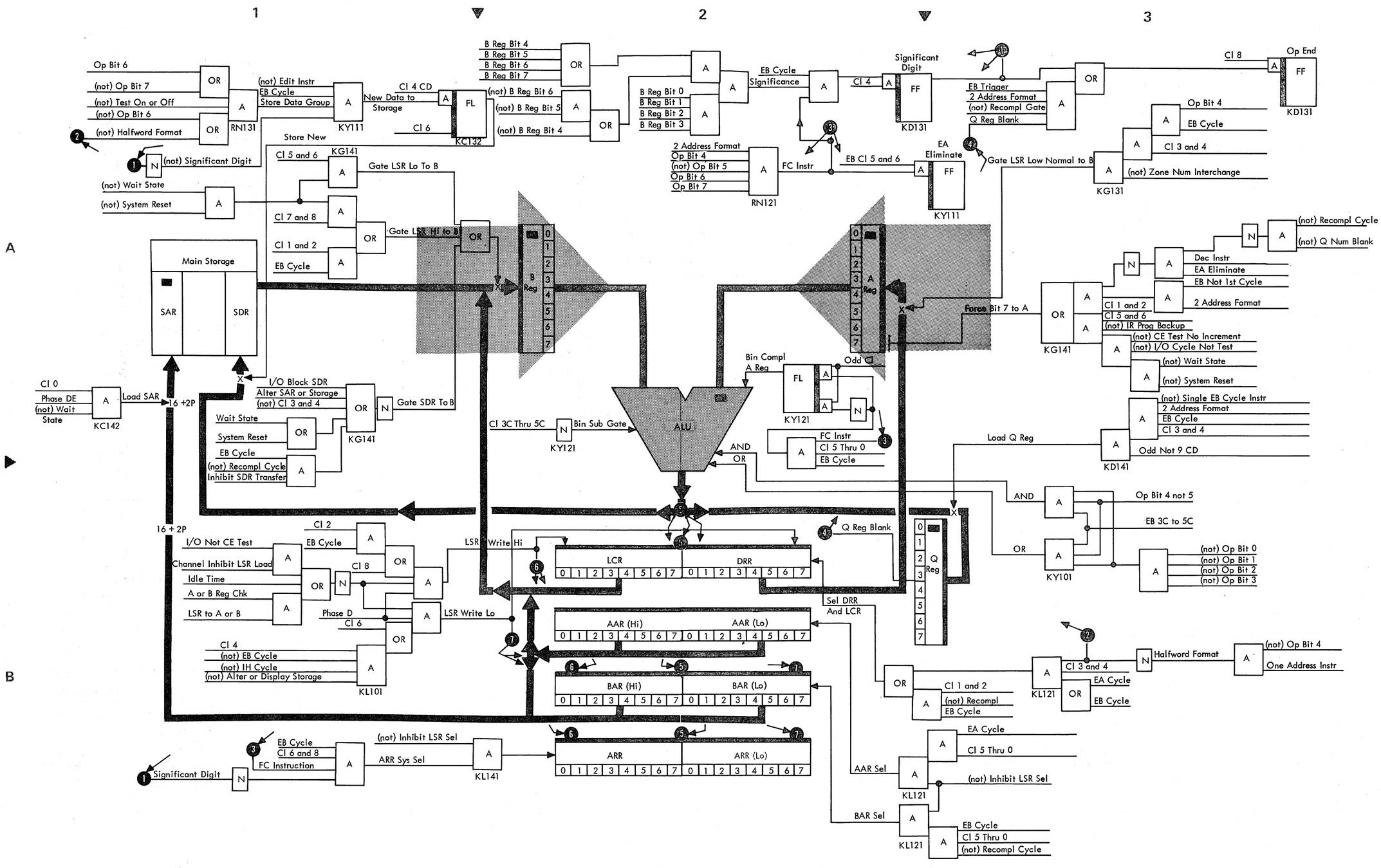


2



3




1
2
3
A
B
Op Bit 6
(not) Op Bit 7
(not) Test On or Off
(not) Op Bit 6
(not) Halfword Format
OR
A
RN131
(not) Edit Instr
EB Cycle
Store Data Group
KY111
New Data to Storage
CI 4 CD
CI 6
FL
KC132
(not) Significant Digit
N
(not) Wait State
(not) System Reset
Store New
CI 5 and 6
KG141
Gate LSR Lo To B
CI 7 and 8
Gate LSR Hi to B
CI 1 and 2
EB Cycle
Main Storage
SAR
SDR
B Reg
CI 0
Phase DE
(not) Wait State
KC142
Load SAR
16 +2P
I/O Block SDR
Alter SAR or Storage
(not) CI 3 and 4
Gate SDR To B
Wait State
System Reset
EB Cycle
(not) Recompl Cycle
Inhibit SDR Transfer
B Reg Bit 4
B Reg Bit 5
B Reg Bit 6
B Reg Bit 7
(not) B Reg Bit 6
(not) B Reg Bit 5
(not) B Reg Bit 4
B Reg Bit 0
B Reg Bit 1
B Reg Bit 2
B Reg Bit 3
2 Address Format
Op Bit 4
(not) Op Bit 5
Op Bit 6
Op Bit 7
RN121
FC Instr
EB Cycle
Significance
CI 4
Significant Digit
FF
KD131
EB Cl 5 and 6
EA Eliminate
KY111
EB Trigger
2 Address Format
(not) Recompl Gate
Q Reg Blank
Gate LSR Low Normal to B
CI 8
Op End
Op Bit 4
CI 3 and 4
(not) Zone Num Interchange
KG131
Bin Compl A Reg
Odd
KY121
CI 3C Thru 5C
Bin Sub Gate
ALU
AND
OR
FC Instr
CI 5 Thru 0
EB Cycle
A Reg
Force Bit 7 to A
Load Q Reg
KD141
Dec Instr
EA Eliminate
EB Not 1st Cycle
2 Address Format
CI 1 and 2
CI 5 and 6
(not) IR Prog Backup
KG141
(not) CE Test No Increment
(not) I/O Cycle Not Test
(not) Wait State
(not) System Reset
(not) Single EB Cycle Instr
2 Address Format
EB Cycle
CI 3 and 4
Odd Not 9 CD
(not) Recompl Cycle
(not) Q Num Blank
Q Reg
Q Reg Blank
AND
OR
Op Bit 4 not 5
EB 3C to 5C
KY101
(not) Op Bit 0
(not) Op Bit 1
(not) Op Bit 2
(not) Op Bit 3
16 + 2P
CI 2
I/O Not CE Test
EB Cycle
Channel Inhibit LSR Load
Idle Time
A or B Reg Chk
LSR to A or B
CI 8
Phase D
CI 6
LSR Write Hi
LSR Write Lo
CI 4
(not) EB Cycle
(not) IH Cycle
(not) Alter or Display Storage
KL101
LCR
DRR
AAR (Hi)
AAR (Lo)
BAR (Hi)
BAR (Lo)
ARR
ARR (Lo)
Sel DRR And LCR
CI 1 and 2
(not) Recompl
EB Cycle
KL121
CI 3 and 4
Halfword Format
(not) Op Bit 4
One Address Instr
EA Cycle
EB Cycle
Significant Digit
EB Cycle
CI 6 and 8
FC Instruction
(not) Inhibit LSR Sel
ARR Sys Sel
KL141
AAR Sel
BAR Sel
EA Cycle
CI 5 Thru 0
(not) Inhibit LSR Sel
EB Cycle
CI 5 Thru 0
(not) Recompl Cycle

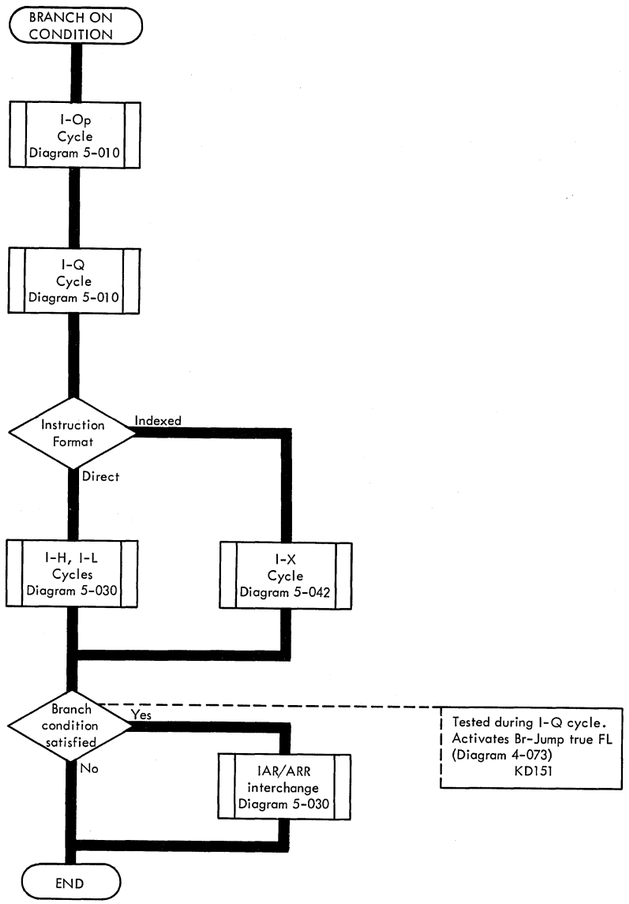
1

Branch on Condition

Bits	0	1	2	3	4	5	6	7
Op Code	1	1	X	X	0	0	0	0

- Condition register is tested for condition specified in Q code
- Branch to address is placed in ARR
- Bit 0 of Q code is used to specify if the branch is performed on condition true or condition false
- IAR/ARR interchange if tested condition is satisfied
- Take I-H and I-L or I-X cycle

SEE DIAGRAM 5-030 (I-H, I-L)
5-042 (I-X)



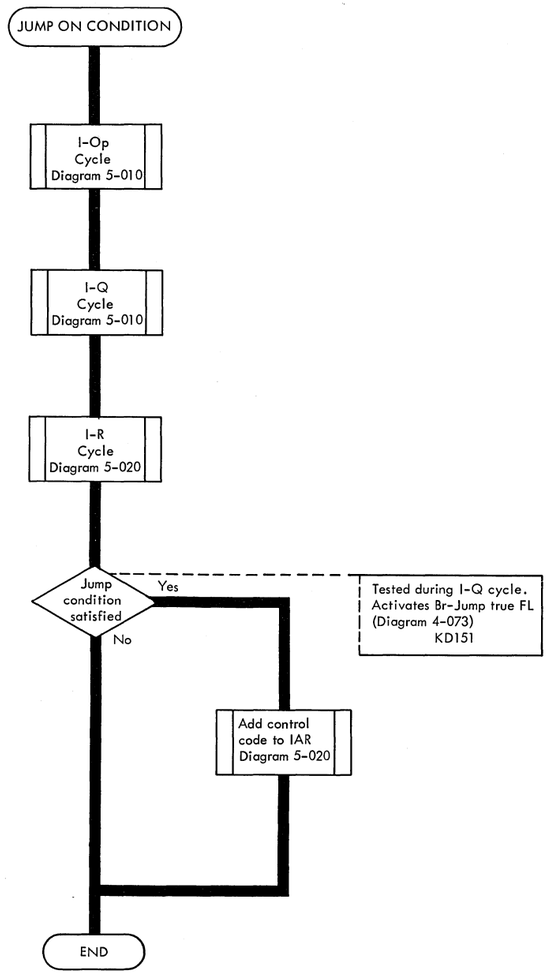
2

Jump On Condition

Bits	0	1	2	3	4	5	6	7
Op Code	1	1	1	1	0	0	1	0

- Condition register is tested for condition specified in Q code
- If tested condition is satisfied, control code is added to IAR for next sequential instruction
- Q code bit 0 is used to specify if jump is performed on condition true or condition false
- Take I-R cycle

SEE DIAGRAM 5-020



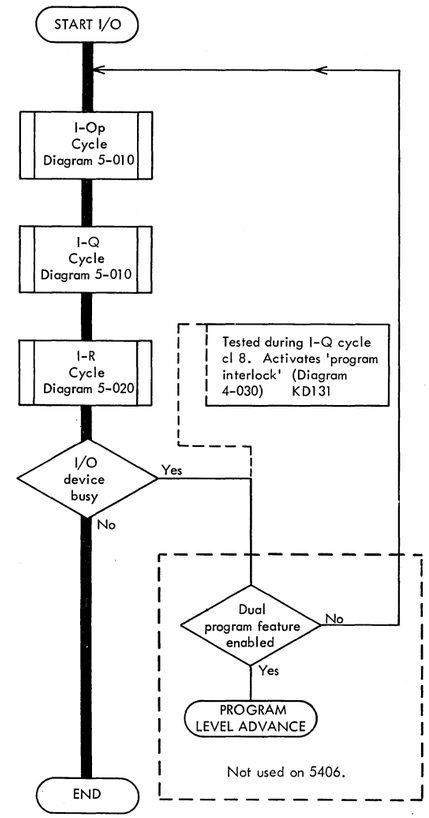
3

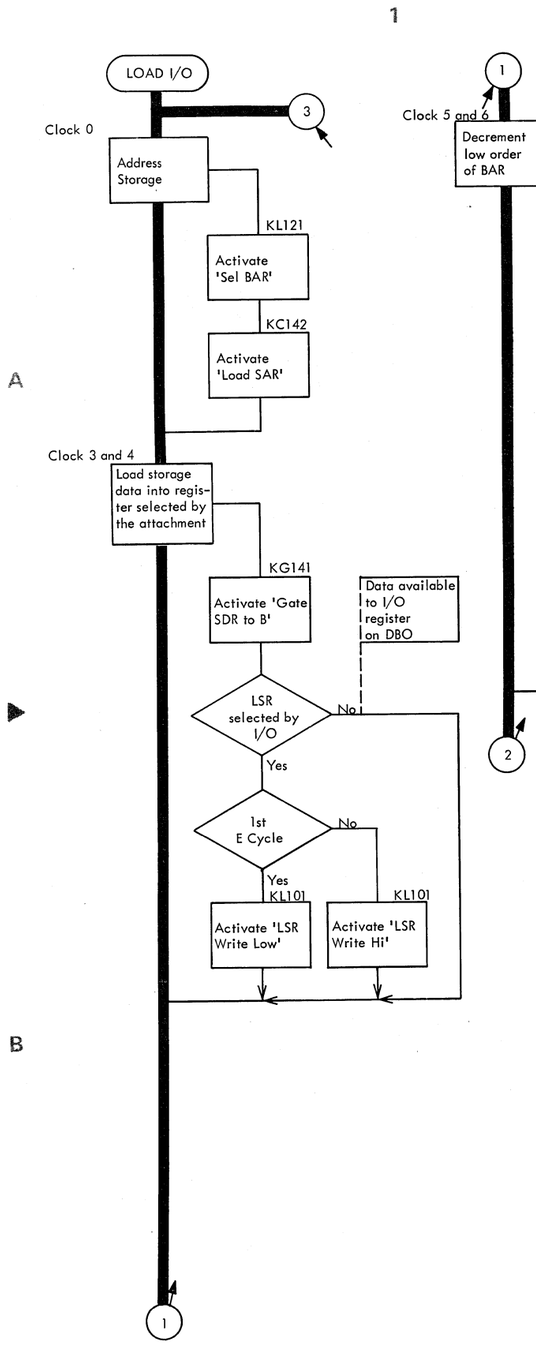
Start I/O

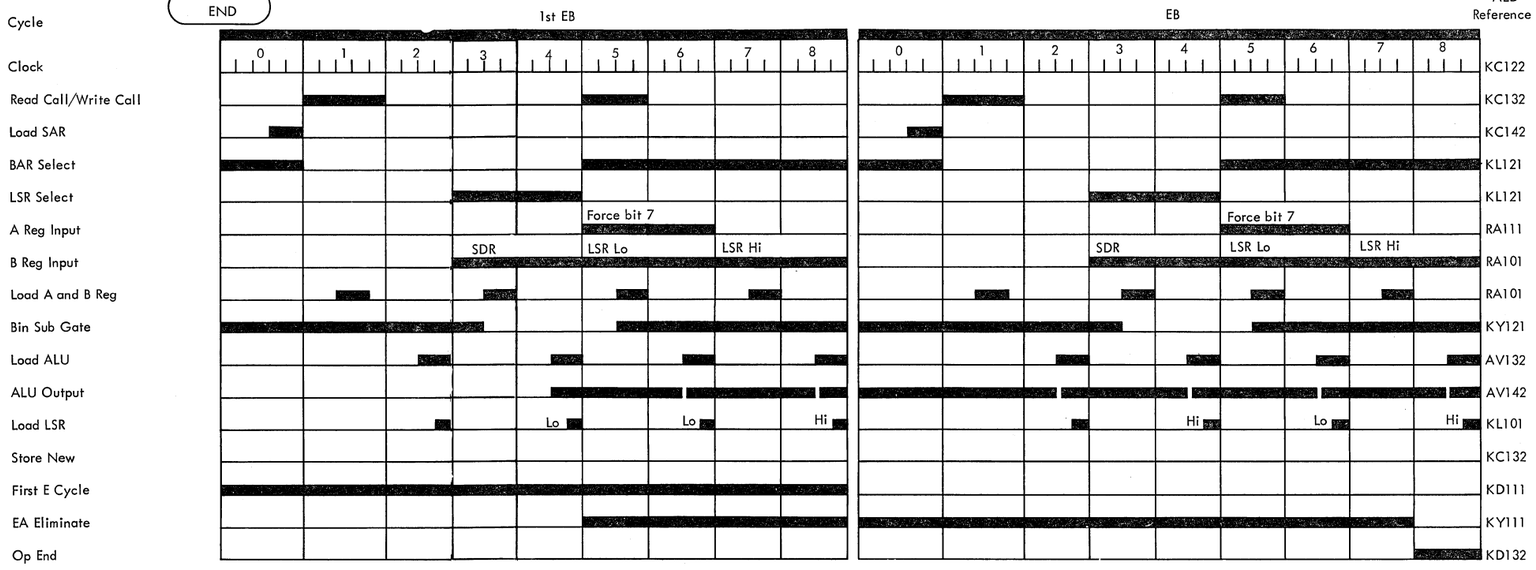
Bits	0	1	2	3	4	5	6	7
Op Code	1	1	1	1	0	0	1	1

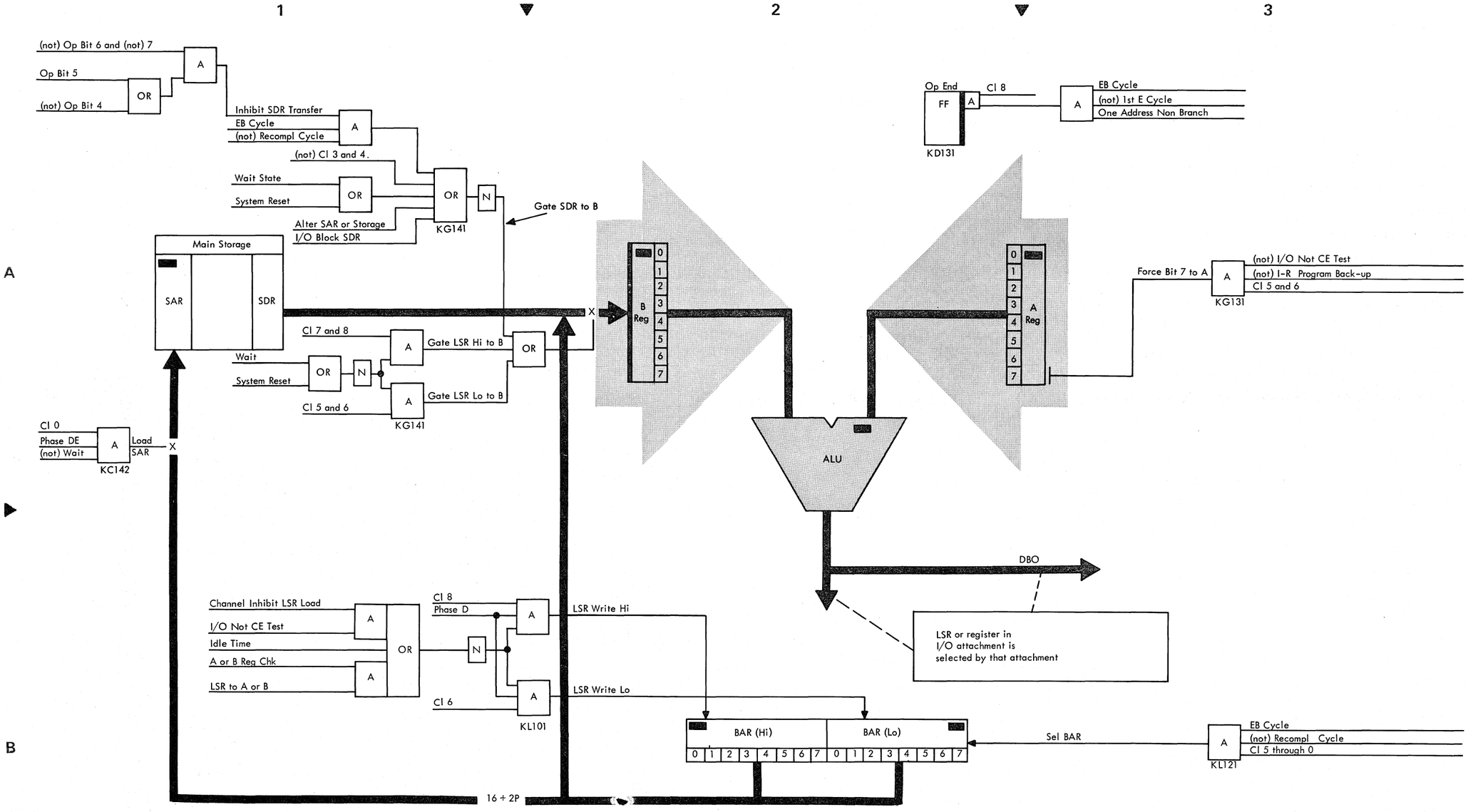
- Start I/O device or enable/disable dual programming feature — Not used on 5406.
- Q code contains device address and function to be performed (read, punch, etc)
- Control code contains additional instruction for device
- I/O device busy causes; (1) program to loop on SIO instruction if dual programming is not installed, or (2) program level advance if dual programming is installed and enabled — Not used on 5406.
- Take I-R Cycle

SEE DIAGRAM 5-020

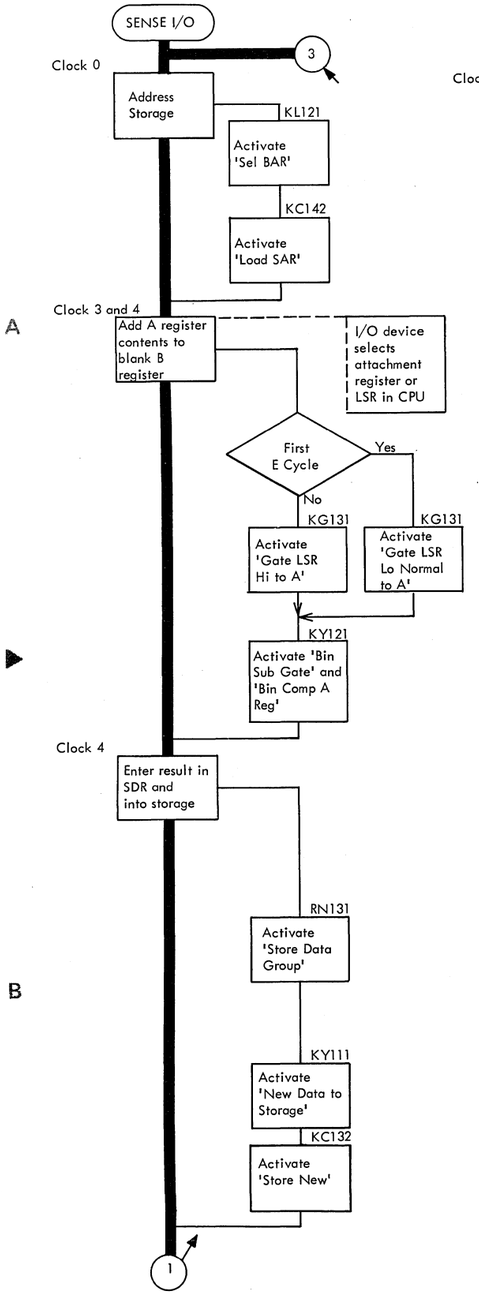


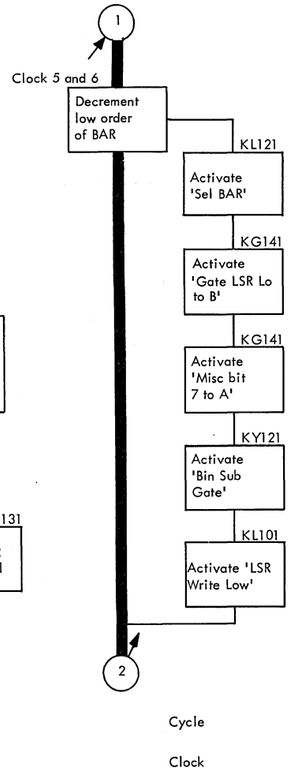

1
2
3
LOAD I/O
Clock 0
Address Storage
KL121
Activate 'Sel BAR'
KC142
Activate 'Load SAR'
A
Clock 3 and 4
Load storage data into register selected by the attachment
KG141
Activate 'Gate SDR to B'
Data available to I/O register on DBO
LSR selected by I/O
No
Yes
1st E Cycle
No
Yes
KL101
Activate 'LSR Write Low'
KL101
Activate 'LSR Write Hi'
B
1
Clock 5 and 6
Decrement low order of BAR
KL121
Activate 'Sel BAR'
KG141
Activate 'Gate LSR Lo to B'
KG141
Activate 'Misc Bit 7 to A'
KY121
Activate 'Bin Sub Gate'
KL101
Activate 'LSR Write Low'
2
2
Clock 7 and 8
Decrement high order of BAR
KL121
Activate 'Sel BAR'
KG141
Activate 'Gate LSR, Hi to B'
KY121
Activate 'Bin Sub Gate'
KL101
Activate 'LSR Write Hi'
3
Yes
First E Cycle
No
KD131
Turn on 'Op End'
END

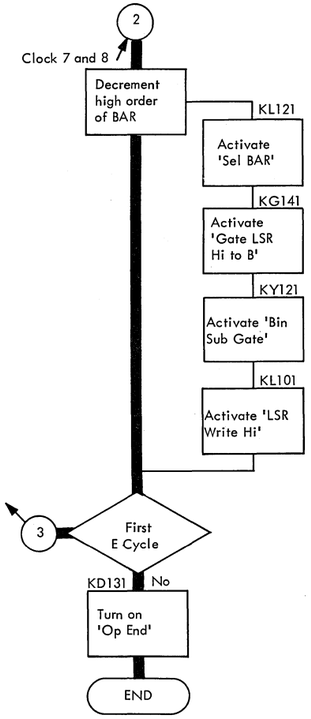

Cycle
1st EB
EB
ALD Reference
0 1 2 3 4 5 6 7 8
Clock
Read Call/Write Call
Load SAR
BAR Select
LSR Select
A Reg Input
B Reg Input
Load A and B Reg
Bin Sub Gate
Load ALU
ALU Output
Load LSR
Store New
First E Cycle
EA Eliminate
Op End
Force bit 7
SDR
LSR Lo
LSR Hi
Lo
Hi
KC122
KC132
KC142
KL121
KL121
RA111
RA101
RA101
KY121
AV132
AV142
KL101
KC132
KD111
KY111
KD132


1
2
3
A
B
(not) Op Bit 6 and (not) 7
Op Bit 5
(not) Op Bit 4
OR
A
Inhibit SDR Transfer
EB Cycle
(not) Recompl Cycle
(not) Cl 3 and 4.
Wait State
System Reset
Alter SAR or Storage
I/O Block SDR
N
KG141
Gate SDR to B
Main Storage
SAR
SDR
X
B Reg
Cl 7 and 8
Gate LSR Hi to B
Wait
System Reset
Gate LSR Lo to B
Cl 5 and 6
KG141
Cl 0
Phase DE
(not) Wait
Load SAR
KC142
Op End
FF
Cl 8
KD131
EB Cycle
(not) 1st E Cycle
One Address Non Branch
A Reg
ALU
Force Bit 7 to A
(not) I/O Not CE Test
(not) I-R Program Back-up
Cl 5 and 6
KG131
DBO
LSR or register in
I/O attachment is
selected by that attachment
Channel Inhibit LSR Load
I/O Not CE Test
Idle Time
A or B Reg Chk
LSR to A or B
Cl 8
Phase D
Cl 6
KL101
LSR Write Hi
LSR Write Lo
BAR (Hi)
BAR (Lo)
Sel BAR
EB Cycle
(not) Recompl Cycle
Cl 5 through 0
KL121
16 + 2P

1 ▼ 2 ▼ 3





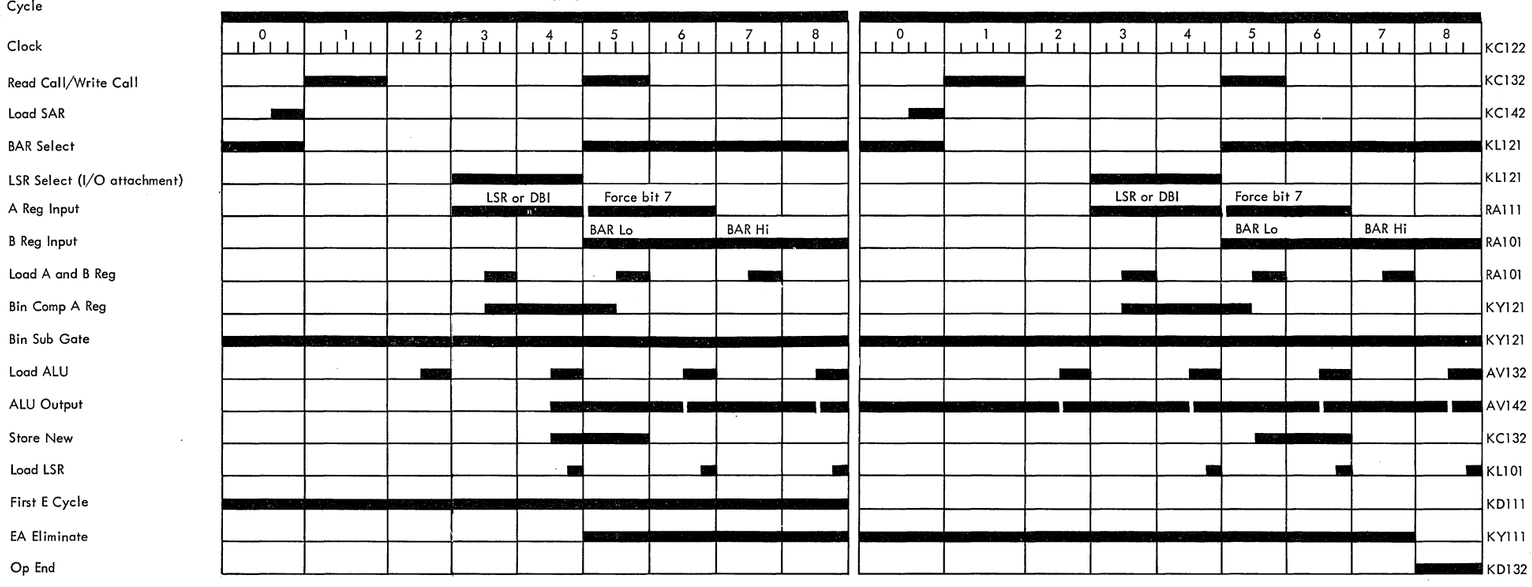


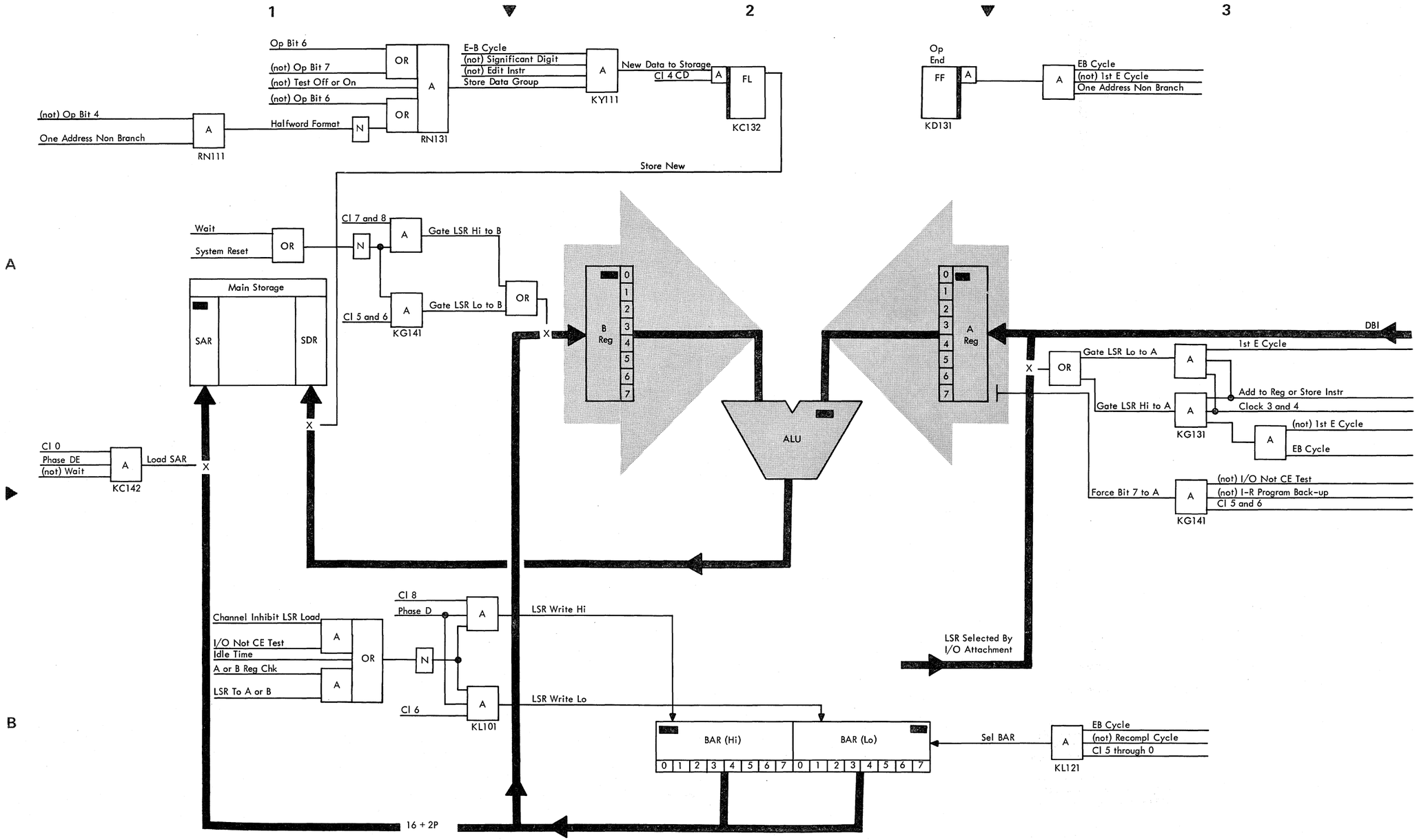
Sense I/O

Bits	0	1	2	3	4	5	6	7
Op Code	0	0	X	X	0	0	0	0

Objective:

- Move two bytes from register selected by I/O attachment to storage



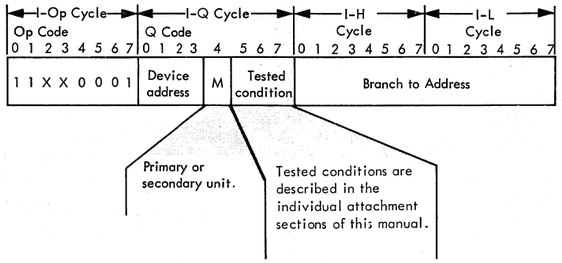

1
2
3
A
B
Op Bit 6
(not) Op Bit 7
(not) Test Off or On
(not) Op Bit 6
OR
OR
A
RN131
E-B Cycle
(not) Significant Digit
(not) Edit Instr
Store Data Group
A
KY111
New Data to Storage
Cl 4 CD
A
FL
KC132
(not) Op Bit 4
One Address Non Branch
A
RN111
Halfword Format
N
Op End
FF
A
KD131
A
EB Cycle
(not) 1st E Cycle
One Address Non Branch
Store New
Wait
System Reset
OR
Cl 7 and 8
N
A
Gate LSR Hi to B
Cl 5 and 6
A
KG141
Gate LSR Lo to B
OR
Main Storage
SAR
SDR
X
B Reg
0 1 2 3 4 5 6 7
ALU
A Reg
0 1 2 3 4 5 6 7
DBI
X
OR
Gate LSR Lo to A
A
1st E Cycle
Gate LSR Hi to A
A
KG131
Add to Reg or Store Instr
Clock 3 and 4
A
(not) 1st E Cycle
EB Cycle
(not) I/O Not CE Test
Force Bit 7 to A
A
KG141
(not) I-R Program Back-up
Cl 5 and 6
Cl 0
Phase DE
(not) Wait
A
KC142
Load SAR
X
Cl 8
Phase D
A
LSR Write Hi
Channel Inhibit LSR Load
I/O Not CE Test
Idle Time
A or B Reg Chk
LSR To A or B
A
A
OR
N
LSR Selected By
I/O Attachment
Cl 6
A
KL101
LSR Write Lo
BAR (Hi)
BAR (Lo)
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
Sel BAR
A
KL121
EB Cycle
(not) Recompl Cycle
Cl 5 through 0
16 + 2P

1 2 3

Test I/O and Branch

- Test for I/O condition specified in Q code N field
- Branch to address is loaded into ARR
- IAR/ARR interchange occurs if tested condition is satisfied
- Take I-H and I-L or I-X cycle

SEE DIAGRAM 5-030 (I-H, I-L)
5-042 (I-X)



Line Activated by Any Device	Significance
'I/O Condition B' only	Correct address, valid N code, condition for branching not met--proceed with next sequential instruction
'I/O Condition A' only	Correct address, valid N code, condition for branching met--branch to new address
Both lines	Incorrect parity--causes processor check and DBO parity check
Neither line	Invalid address or N code --causes processor check and invalid device address

A

B

Load Address

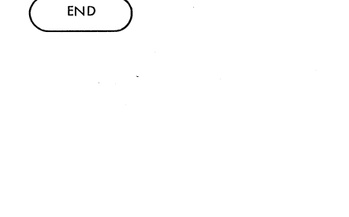
Bits	0	1	2	3	4	5	6	7
Op Code	1	1	X	X	0	0	1	0

- Load one or two bytes from storage into one of the two index registers
- If instruction format is four bytes, load two byte address into index register selected by Q code bits 6 and 7
- If instruction format is three bytes, add last instruction byte to index register selected by Op Code bits 2 and 3. Then load result into index register selected by Q code bits 6 and 7
- Take I-H and I-L cycles (four byte format)

SEE DIAGRAM 5-030

- Take I-X cycle (three byte format)

SEE DIAGRAM 5-042



1

Advance Program Level

Bits	0	1	2	3	4	5	6	7
Op Code	1	1	1	1	0	0	0	1

Basic Machine

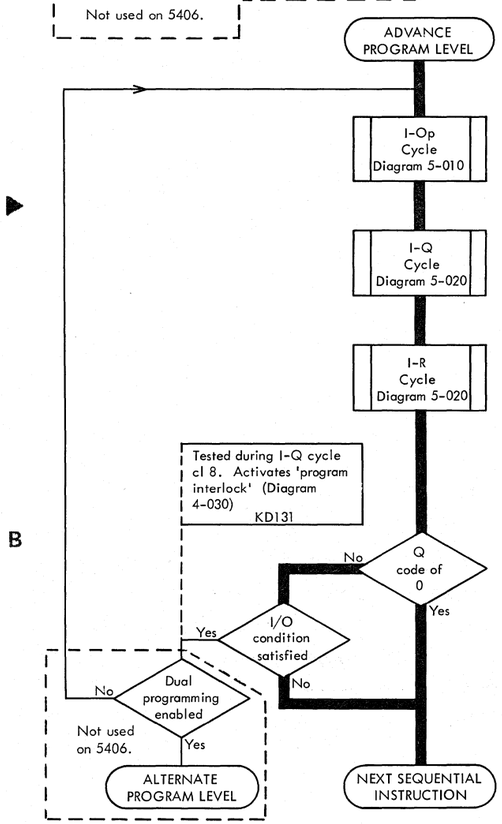
- Test for I/O condition specified in Q code N field
- Loop on APL instruction until condition tested for no longer exists
- Q code N field of all zeros causes automatic advance to next sequential instruction
- Take I-R cycle SEE DIAGRAM 5-020

Dual Program Feature Enabled

- Test for I/O condition specified in Q code N field
- Program level advance if condition is satisfied
- Program status register (PSR) contains recall information for returning to original program
- Take I-R cycle SEE DIAGRAM 5-020

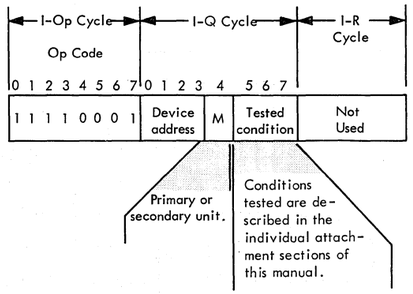
Not used on 5406.

A



▶

▼ 2



Line Activated by Any Device	Significance
'I/O Condition B' only	Correct address, valid N code, device not busy and doesn't need attention --instruction accepted
'I/O Condition A' only	Correct address, valid N code, device busy or needs attention--instruction rejected
Both lines	Incorrect parity--causes processor check and DBO parity check
Neither line	Invalid address or N code --causes processor check and invalid device address

▼ 3

Halt Program Level

Bits	0	1	2	3	4	5	6	7
Op Code	1	1	1	1	0	0	0	0

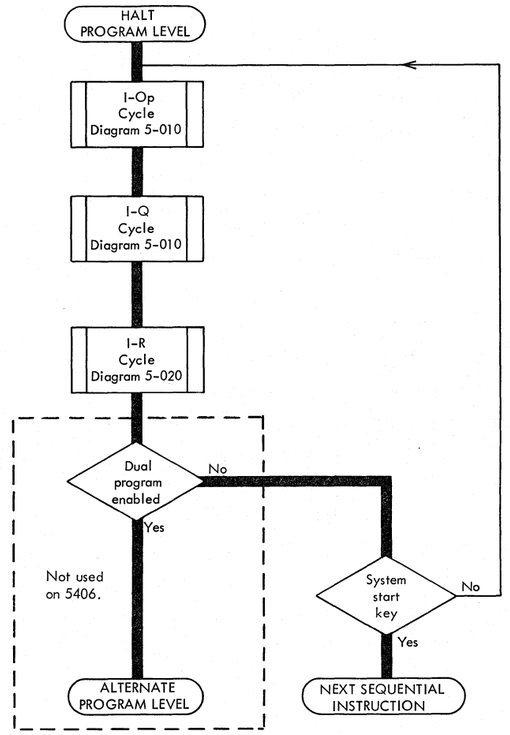
Basic Machine

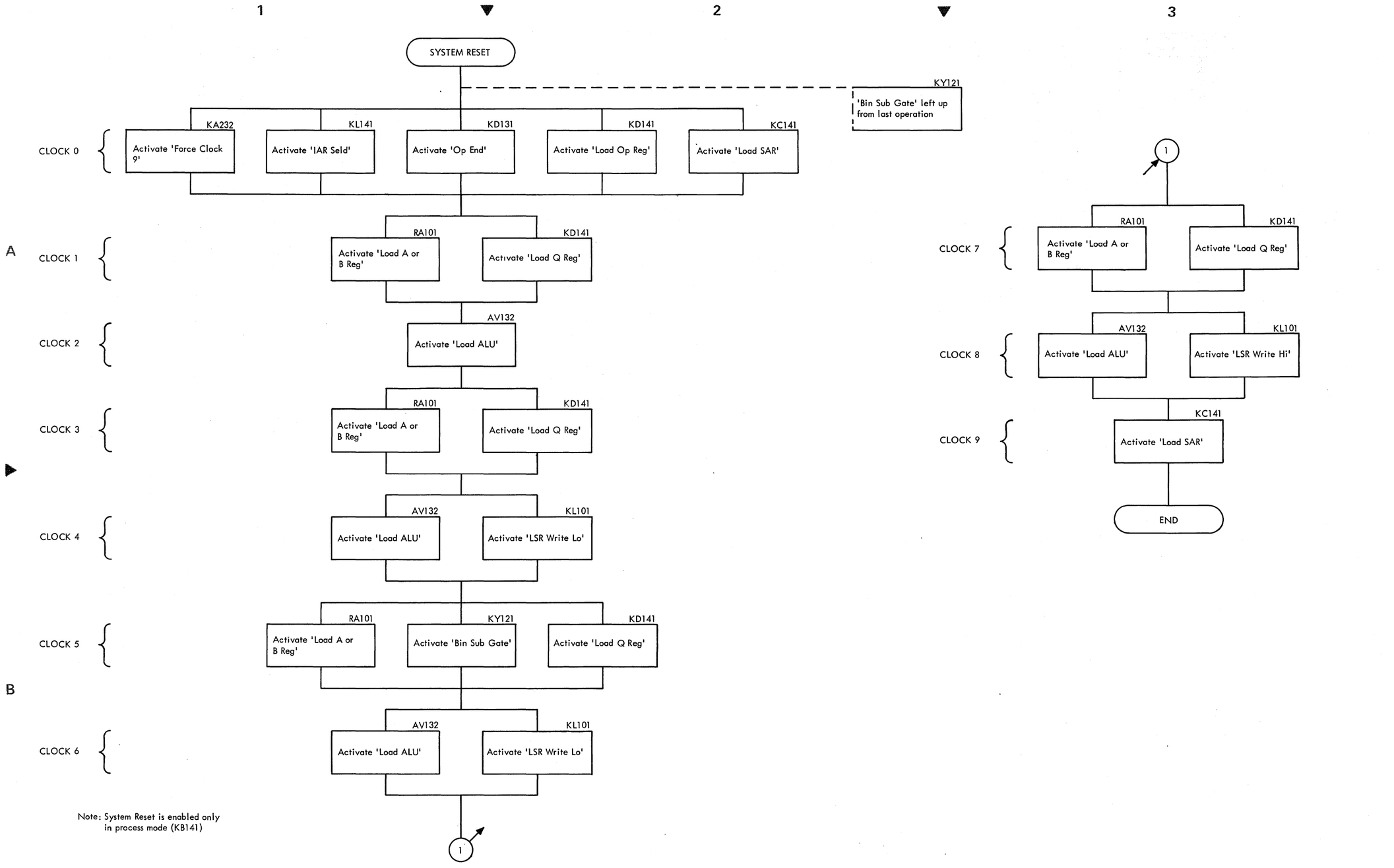
- Prevents execution of next sequential instruction
- Loops on instruction until system start key is pressed
- Instruction bytes three and four are displayed on console

Dual Program Feature Enabled

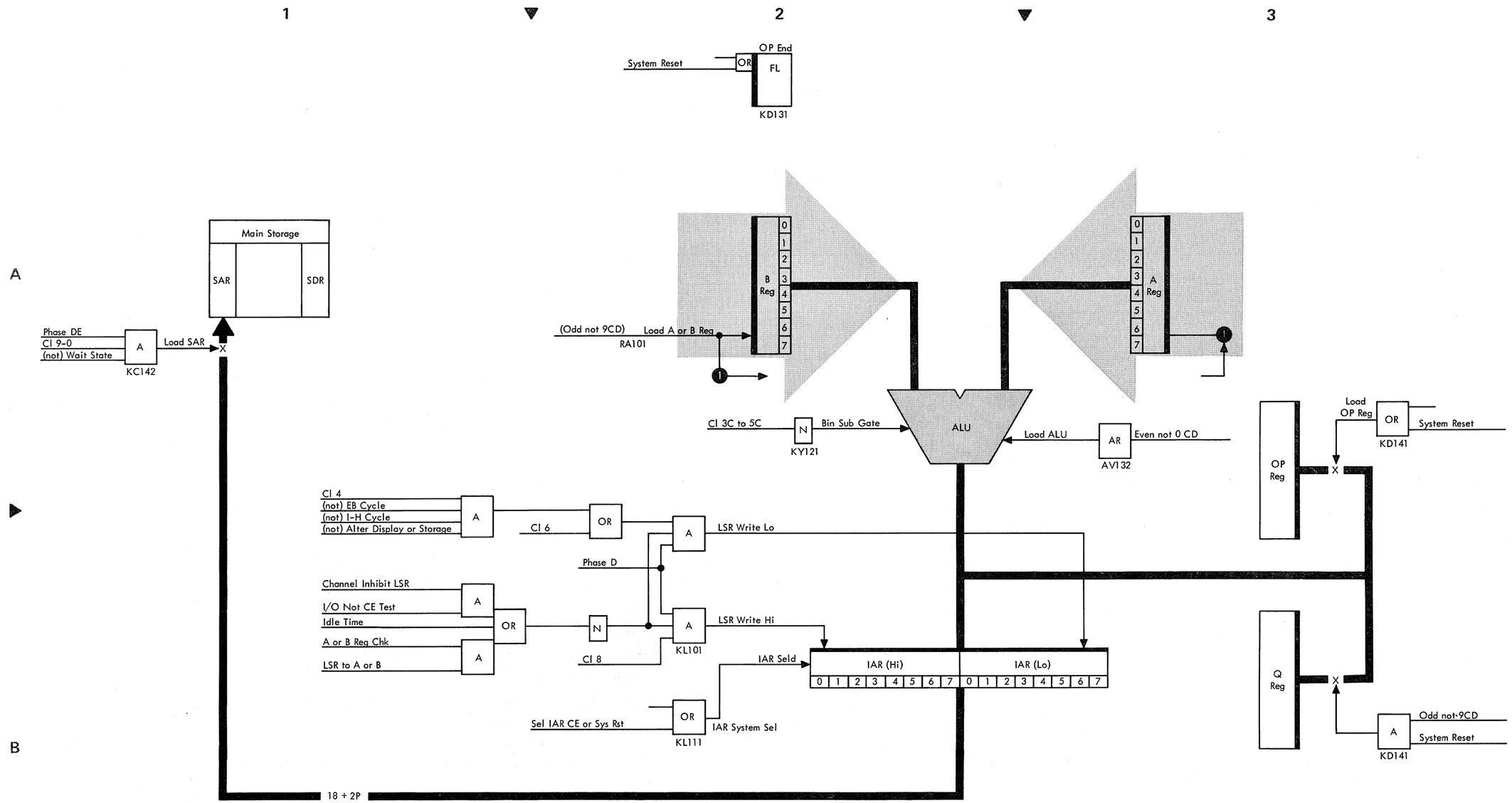
- Prevents execution of next sequential instruction
- Branches to alternate program level if DPF is enabled
- Program returns to original level if appropriate halt reset key is pressed
- Take I-R cycle SEE DIAGRAM 5-020

Not used on 5406.



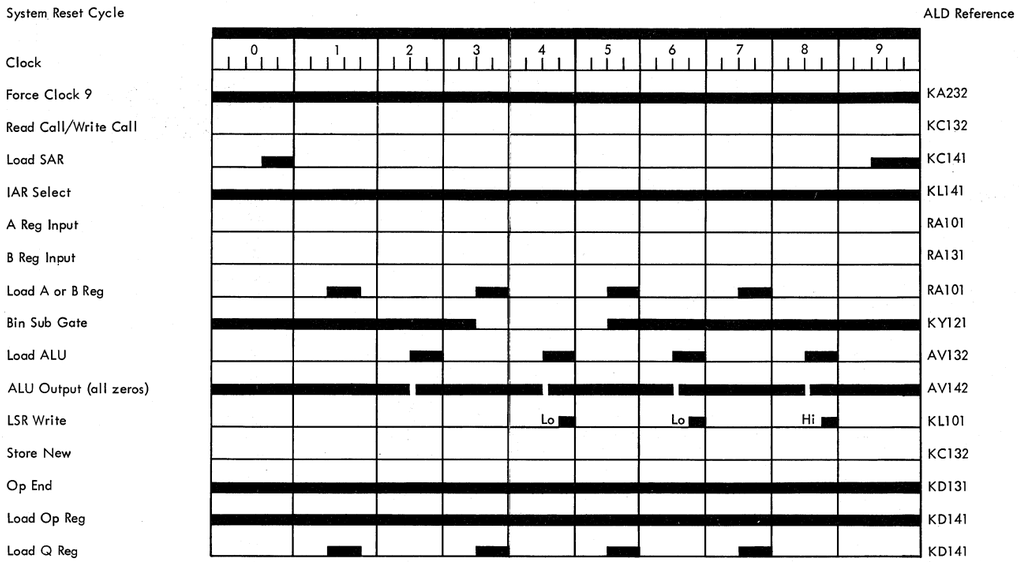


Note: System Reset is enabled only in process mode (KB141)



Note: 1. Refer to Diagram 4-020 for clock circuits
2. Refer to Diagram 4-030 for cycle controls

1 ▼ 2 ▼ 3



Note: Parity checking is disabled during System Reset

A

▶

B

1 ▼ 2 ▼ 3

Initial Program Load (IPL)

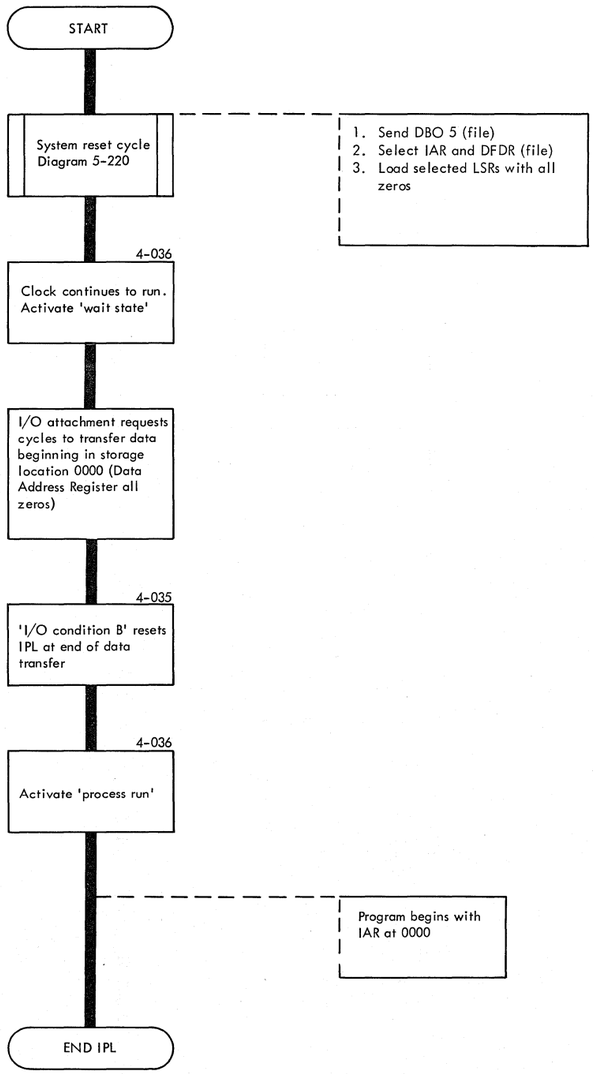
Objectives

- Program Load Key initiates system reset cycle
- Clock starts and continues to run
- System reset cycle causes:
  - (1) DBO 5 (File)
  - (2) All zeros written into IAR and DFDR (File)
- 'I/O Condition B' resets IPL latch at end of data transfer and activates process run. First I-Op cycle addresses storage position 0000 (IAR set to all zero)

A

▶

B



Alter SAR

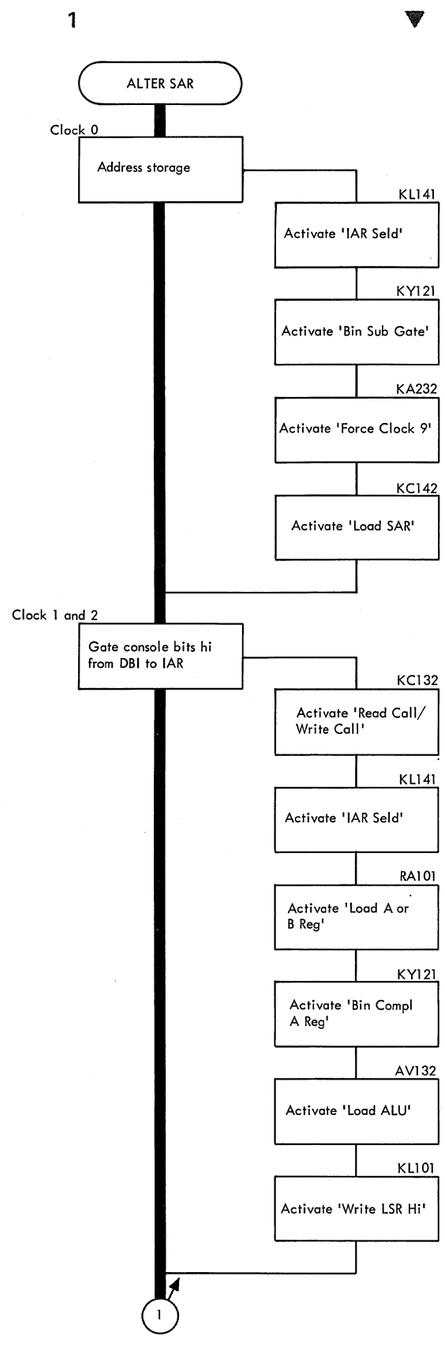
Objectives:

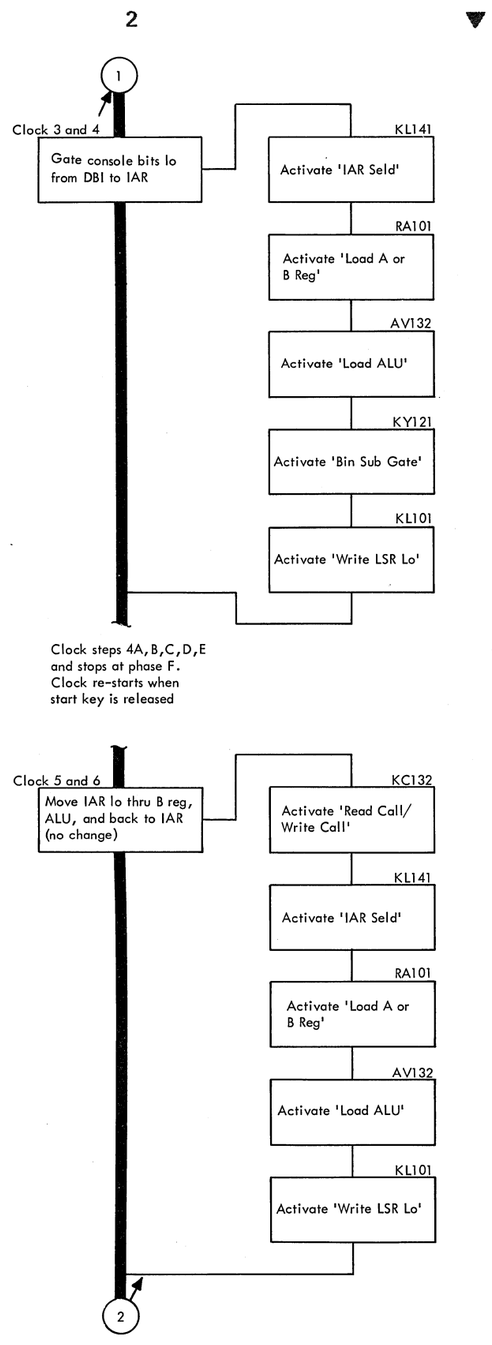
- Load contents of four console Address/Data switches into the Instruction Address Register (IAR) by way of Data Bus In, A register and ALU
- Load SAR from the IAR at clock 9 time
- When start key is pressed, the clock runs 0 thru 4. When start key is released, clock runs from 5 thru 9.

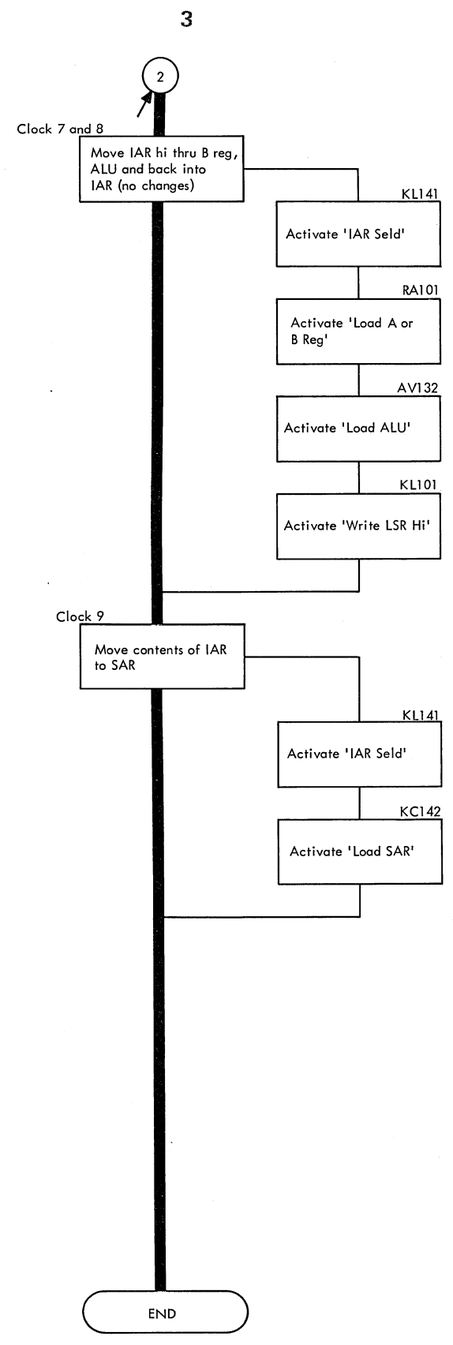
A

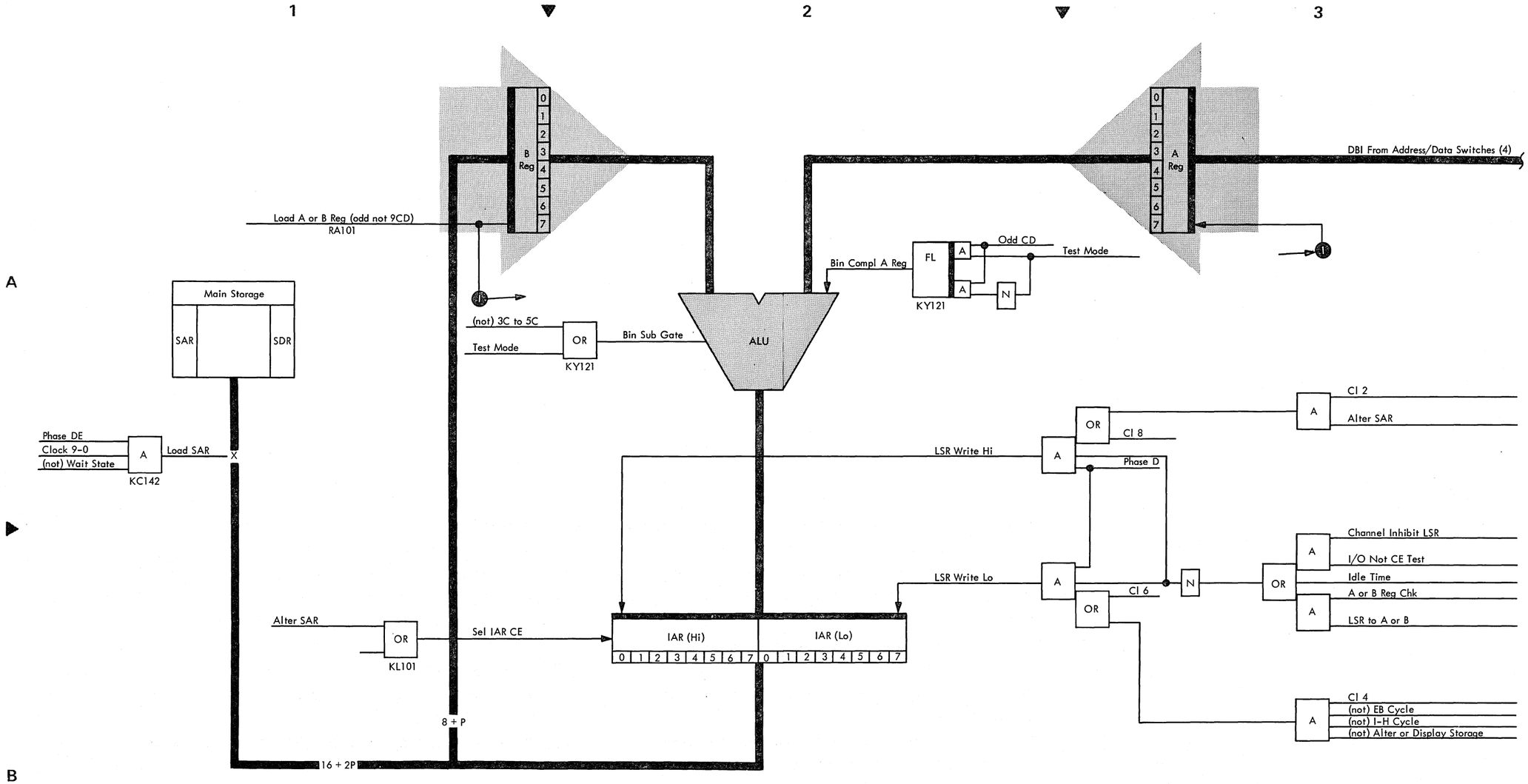
▶

B







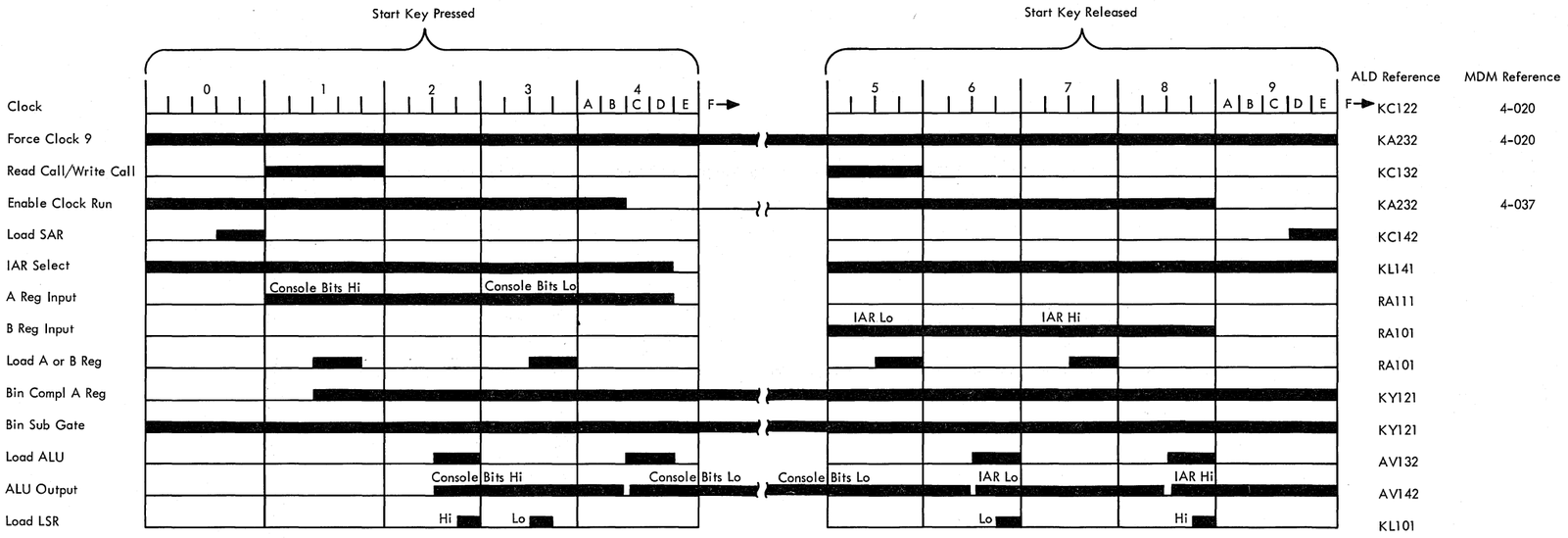


Note: Refer to diagram 4-020 for clock circuits

Refer to diagram 4-035 for Run controls

1 2 3

ALTER SAR



	ALD Reference	MDM Reference
F→	KC122	4-020
	KA232	4-020
	KC132	
	KA232	4-037
	KC142	
	KL141	
	RA111	
	RA101	
	RA101	
	KY121	
	KY121	
	AV132	
	AV142	
	KL101	

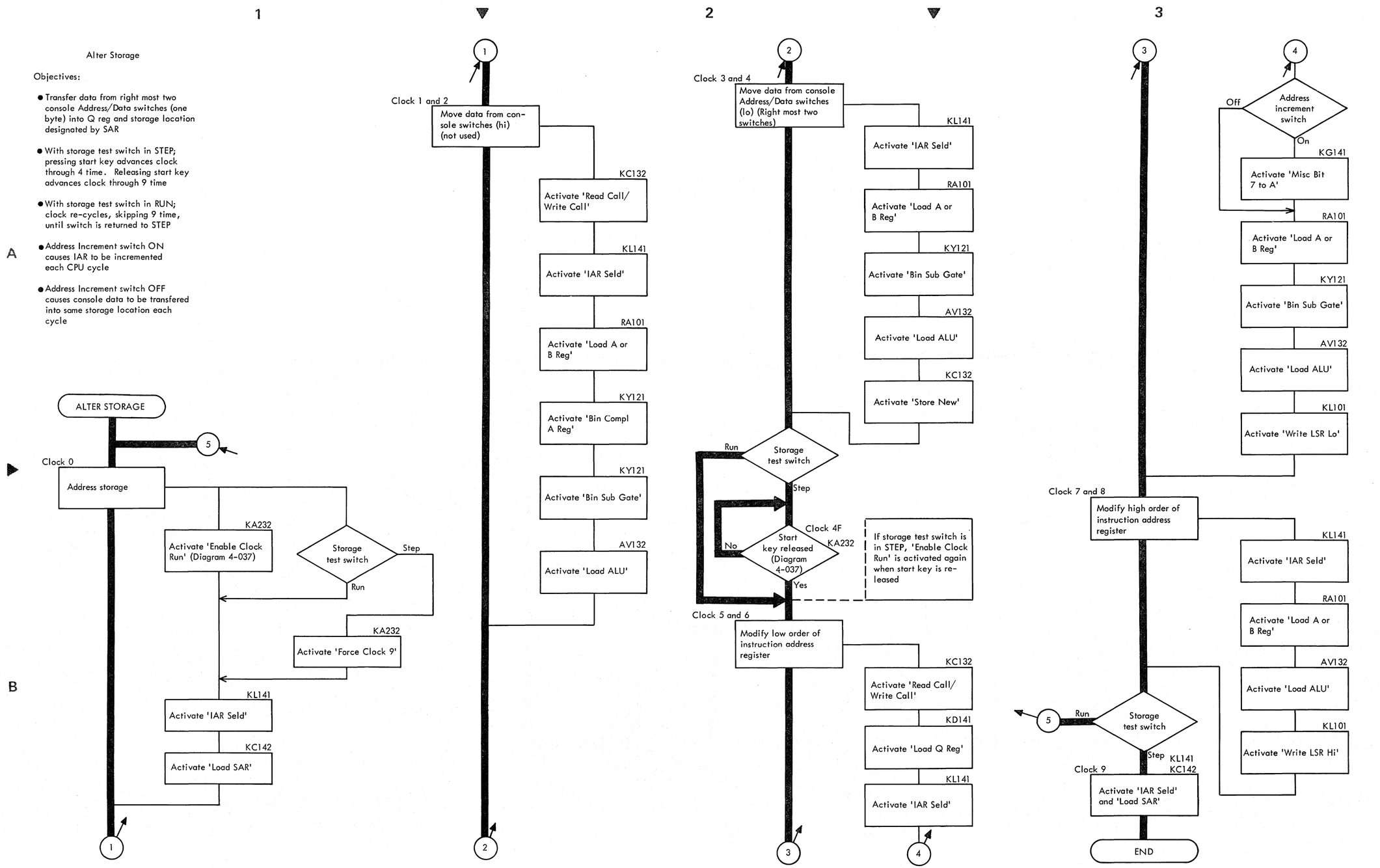
A

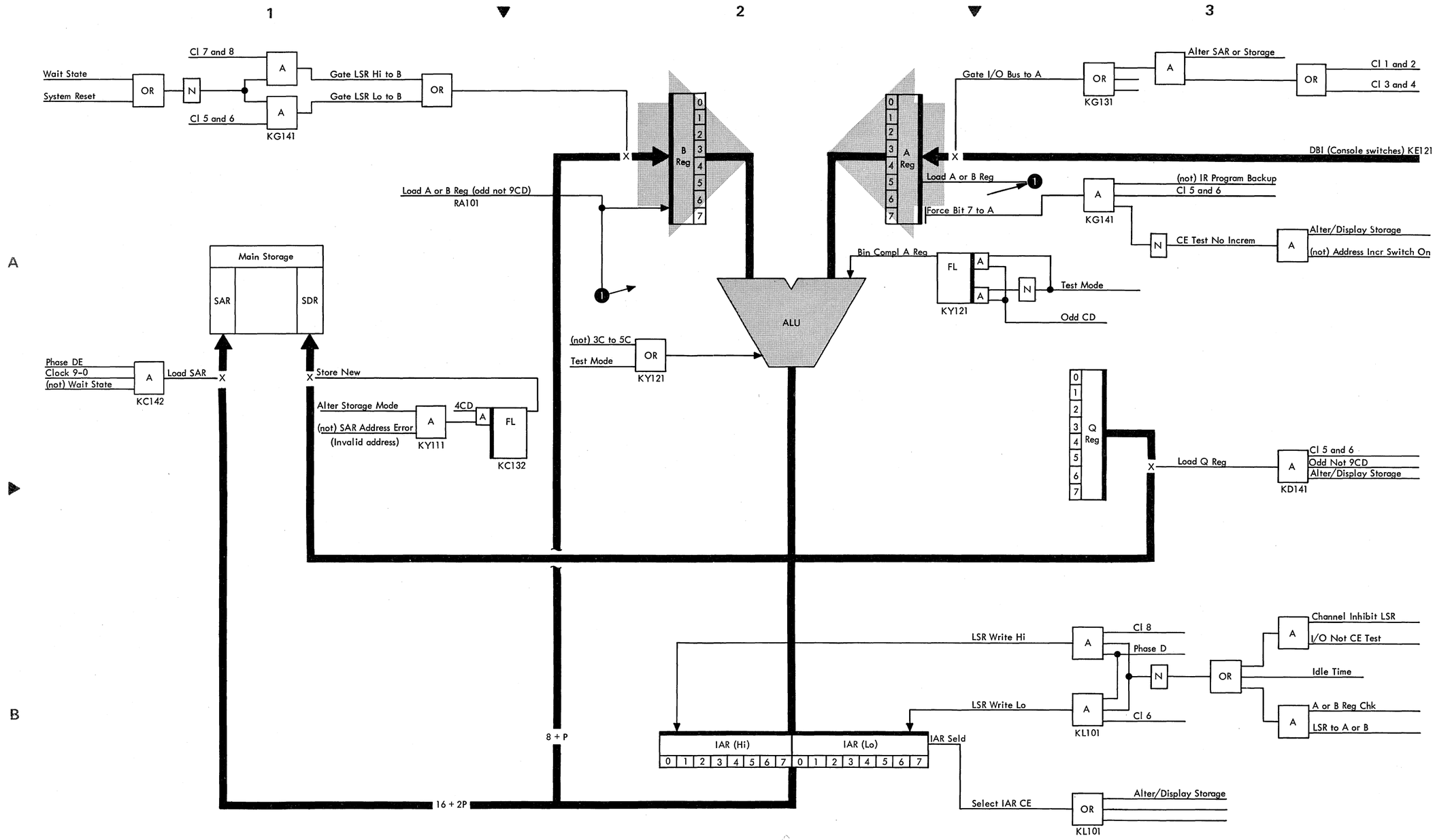
B

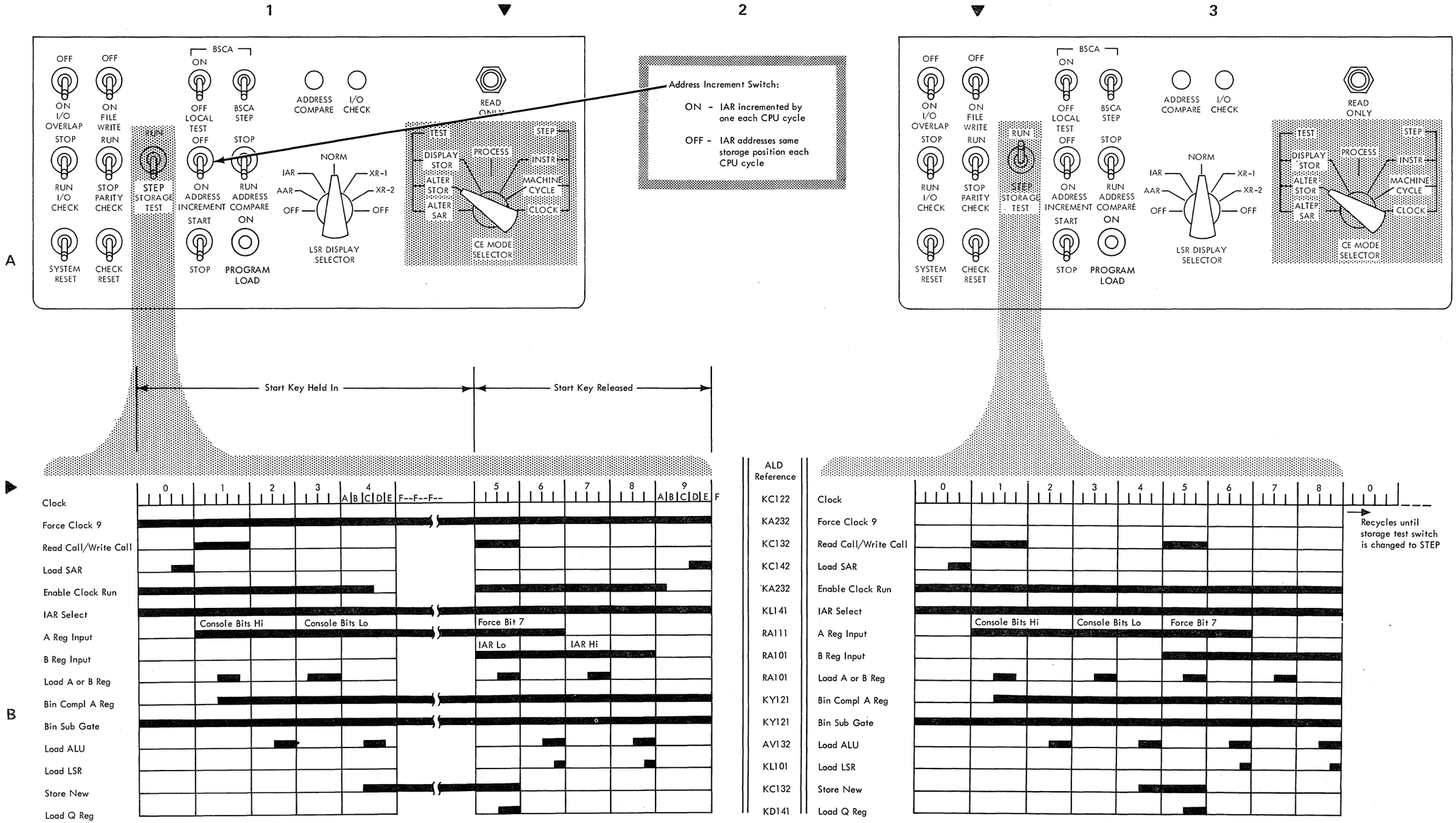
Alter Storage

Objectives:

- Transfer data from right most two console Address/Data switches (one byte) into Q reg and storage location designated by SAR
- With storage test switch in STEP; pressing start key advances clock through 4 time. Releasing start key advances clock through 9 time
- With storage test switch in RUN; clock re-cycles, skipping 9 time, until switch is returned to STEP
- Address Increment switch ON causes IAR to be incremented each CPU cycle
- Address Increment switch OFF causes console data to be transfered into same storage location each cycle



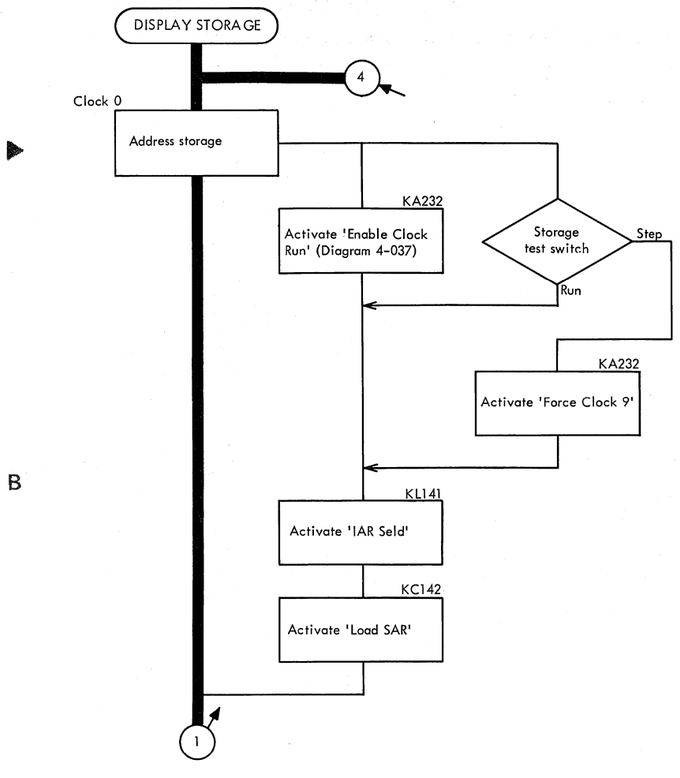

1
2
3
A
B
Wait State
System Reset
OR
N
Cl 7 and 8
Cl 5 and 6
A
KG141
Gate LSR Hi to B
Gate LSR Lo to B
OR
Load A or B Reg (odd not 9CD)
RA101
B Reg
A Reg
Gate I/O Bus to A
OR
KG131
Alter SAR or Storage
Cl 1 and 2
Cl 3 and 4
DBI (Console switches) KE121
Load A or B Reg
Force Bit 7 to A
(not) IR Program Backup
Cl 5 and 6
KG141
CE Test No Increm
Alter/Display Storage
(not) Address Incr Switch On
Bin Compl A Reg
FL
KY121
Test Mode
Odd CD
ALU
(not) 3C to 5C
Test Mode
OR
KY121
Main Storage
SAR
SDR
Phase DE
Clock 9-0
(not) Wait State
KC142
Load SAR
Store New
Alter Storage Mode
(not) SAR Address Error
(Invalid address)
KY111
4CD
FL
KC132
Q Reg
Load Q Reg
Cl 5 and 6
Odd Not 9CD
Alter/Display Storage
KD141
8 + P
16 + 2P
IAR (Hi)
IAR (Lo)
IAR Seld
LSR Write Hi
LSR Write Lo
Cl 8
Phase D
Cl 6
KL101
N
OR
Channel Inhibit LSR
I/O Not CE Test
Idle Time
A or B Reg Chk
LSR to A or B
Select IAR CE
OR
KL101
Alter/Display Storage

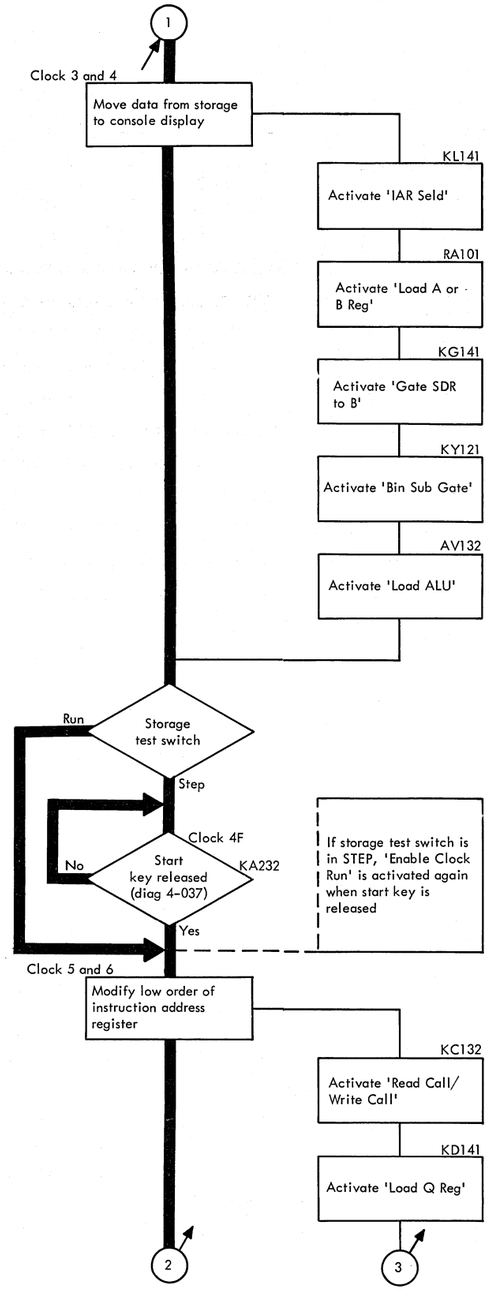

1
2
3
A
B
OFF
ON I/O OVERLAP
STOP
RUN I/O CHECK
SYSTEM RESET
OFF
ON FILE WRITE
RUN
STOP PARITY CHECK
CHECK RESET
RUN
STEP STORAGE TEST
BSCA
ON
OFF LOCAL TEST
START
STOP
BSCA STEP
STOP
RUN ADDRESS COMPARE
ON
PROGRAM LOAD
ADDRESS COMPARE
I/O CHECK
NORM
IAR
AAR
OFF
XR-1
XR-2
OFF
LSR DISPLAY SELECTOR
READ ONLY
TEST
DISPLAY STOR
ALTER STOR
ALTER SAR
PROCESS
STEP
INSTR
MACHINE CYCLE
CLOCK
CE MODE SELECTOR
Address Increment Switch:
ON - IAR incremented by one each CPU cycle
OFF - IAR addresses same storage position each CPU cycle
Start Key Held In
Start Key Released
ALD Reference
Clock
Force Clock 9
Read Call/Write Call
Load SAR
Enable Clock Run
IAR Select
A Reg Input
B Reg Input
Load A or B Reg
Bin Compl A Reg
Bin Sub Gate
Load ALU
Load LSR
Store New
Load Q Reg
KC122
KA232
KC132
KC142
KA232
KL141
RA111
RA101
RA101
KY121
KY121
AV132
KL101
KC132
KD141
Console Bits Hi
Console Bits Lo
Force Bit 7
IAR Lo
IAR Hi
Recycles until storage test switch is changed to STEP

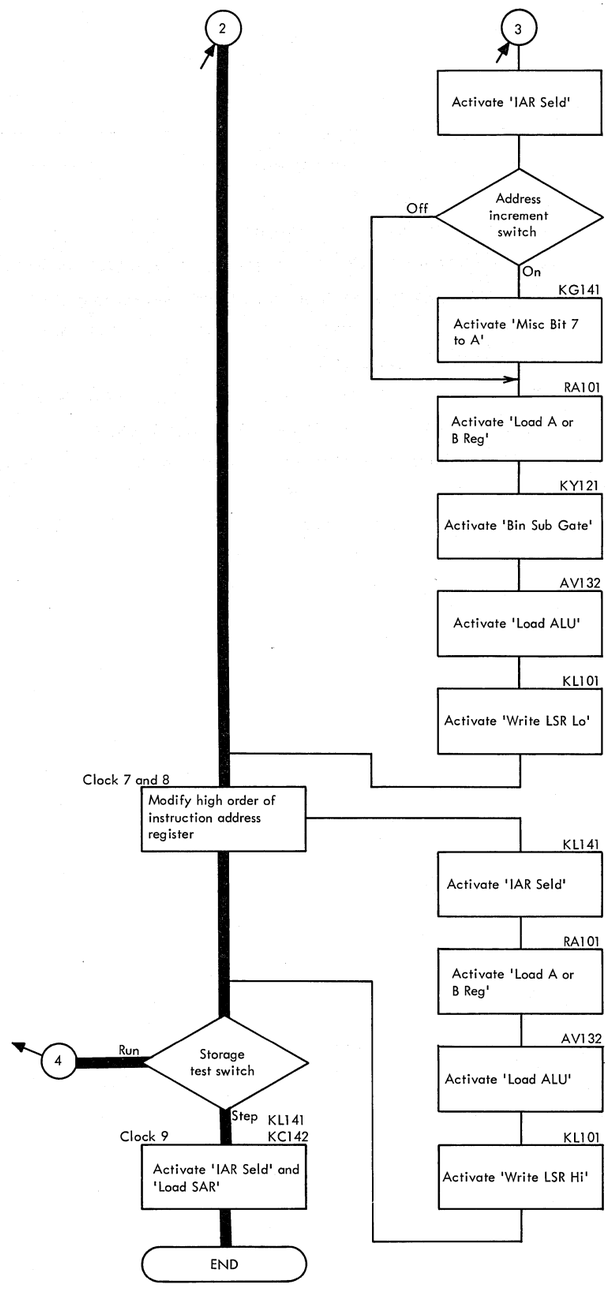
Display Storage

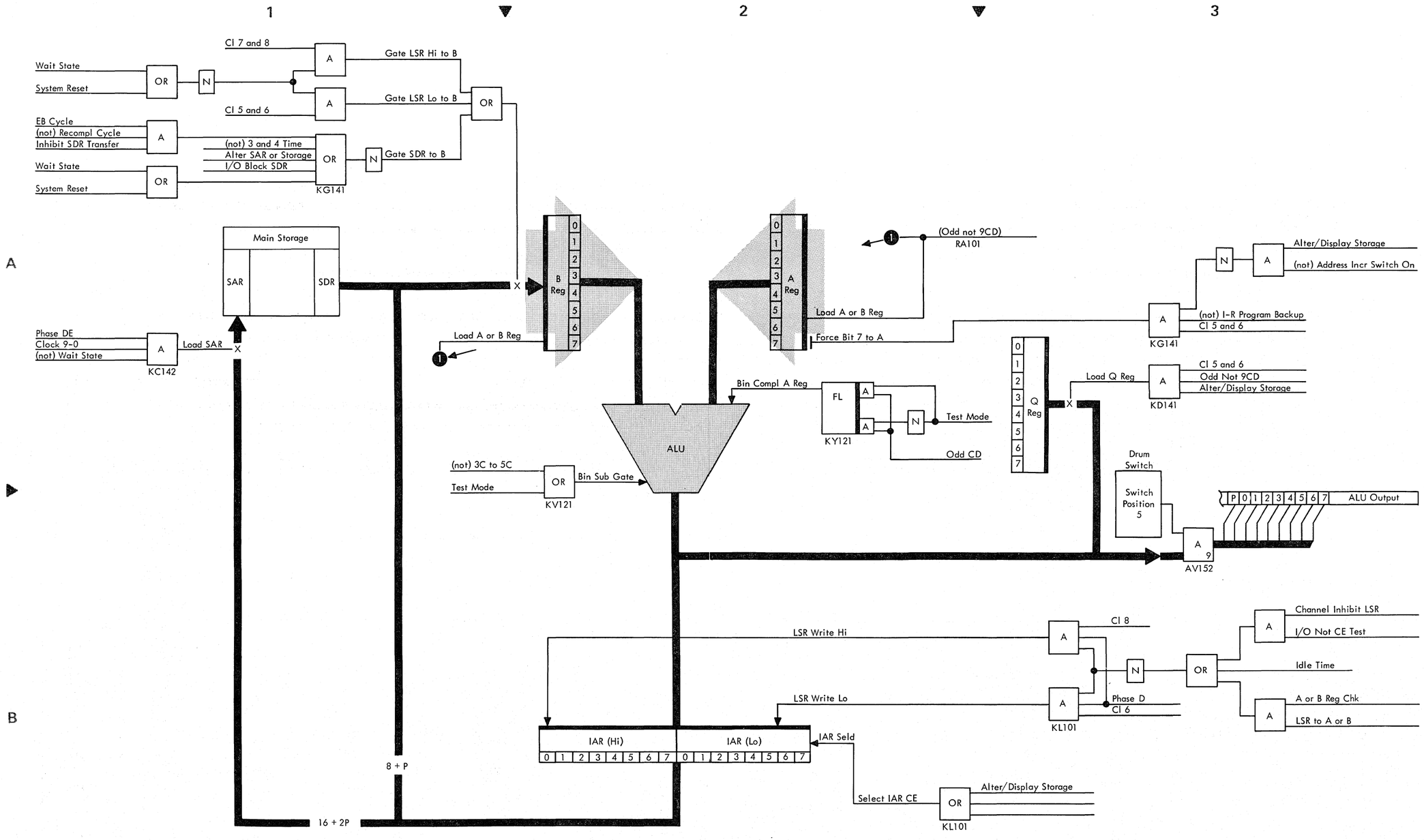
Objectives

- Transfer data from storage position addressed by SAR into Q register and display in console lights when drum switch is in position 5
- With storage test switch in STEP; pressing start key advances clock through 4 time. Releasing start key advances clock through 9 time
- With storage test switch in RUN; clock re-cycles, skipping 9 time, until switch is returned to STEP
- Address Increment switch ON causes IAR to be incremented each CPU cycle
- Address Increment switch OFF causes console data to be transfered into same storage location each cycle

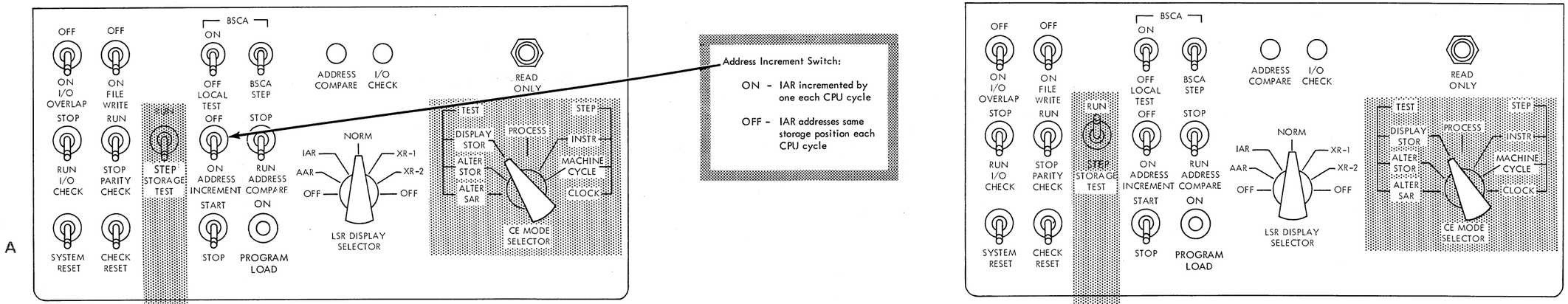







1
2
3
A
B
Wait State
System Reset
OR
N
CI 7 and 8
A
Gate LSR Hi to B
CI 5 and 6
A
Gate LSR Lo to B
OR
EB Cycle
(not) Recompl Cycle
Inhibit SDR Transfer
A
(not) 3 and 4 Time
Alter SAR or Storage
I/O Block SDR
OR
N
Gate SDR to B
Wait State
System Reset
OR
KG141
Main Storage
SAR
SDR
Phase DE
Clock 9-0
(not) Wait State
A
Load SAR
X
KC142
Load A or B Reg
B Reg
0 1 2 3 4 5 6 7
X
A Reg
0 1 2 3 4 5 6 7
(Odd not 9CD)
RA101
Load A or B Reg
Force Bit 7 to A
N
A
Alter/Display Storage
(not) Address Incr Switch On
A
(not) I-R Program Backup
CI 5 and 6
KG141
Bin Compl A Reg
FL
A
A
N
Test Mode
Odd CD
KY121
Q Reg
0 1 2 3 4 5 6 7
X
Load Q Reg
A
CI 5 and 6
Odd Not 9CD
Alter/Display Storage
KD141
ALU
(not) 3C to 5C
Test Mode
OR
Bin Sub Gate
KV121
Drum Switch
Switch Position 5
A
9
AV152
P 0 1 2 3 4 5 6 7
ALU Output
LSR Write Hi
LSR Write Lo
A
A
CI 8
Phase D
CI 6
N
OR
KL101
Channel Inhibit LSR
I/O Not CE Test
Idle Time
A or B Reg Chk
LSR to A or B
A
A
IAR (Hi)
0 1 2 3 4 5 6 7
IAR (Lo)
0 1 2 3 4 5 6 7
IAR Seld
8 + P
16 + 2P
Select IAR CE
OR
KL101
Alter/Display Storage

1 2 3



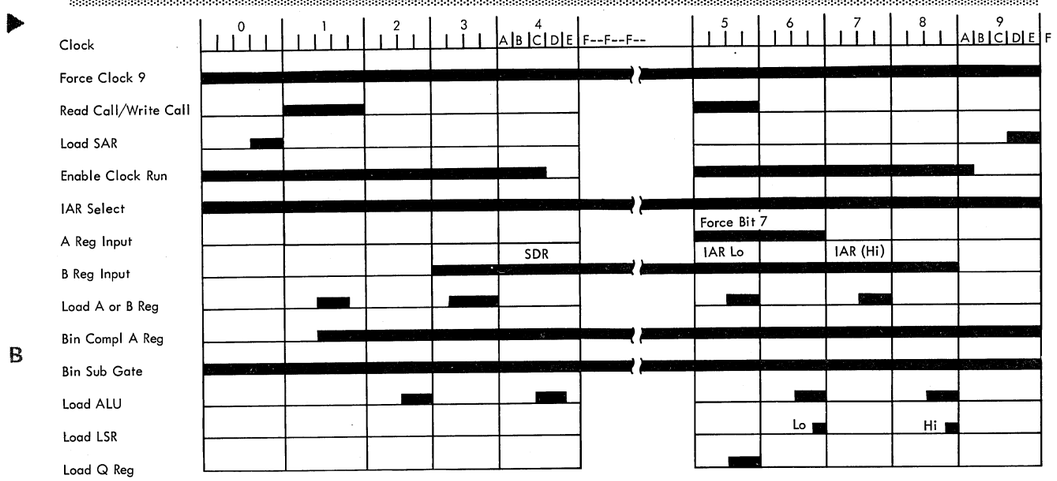
Address Increment Switch:

ON - IAR incremented by one each CPU cycle

OFF - IAR addresses same storage position each CPU cycle

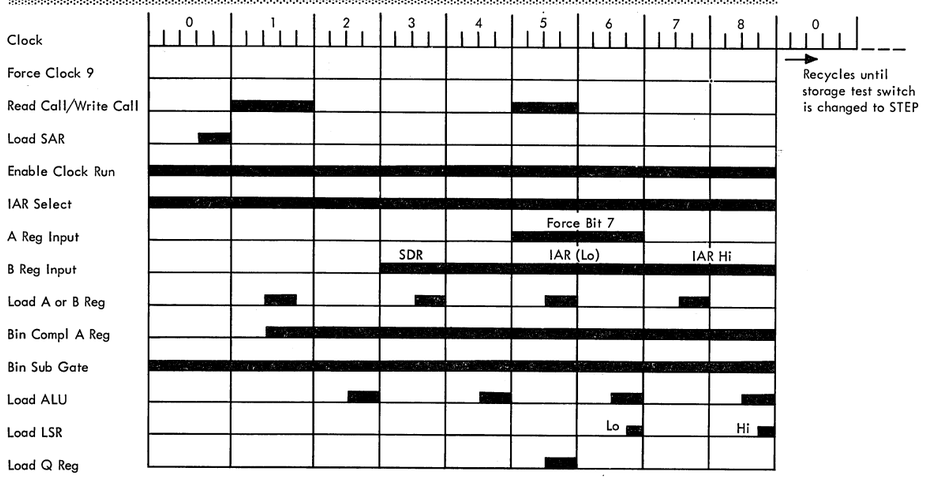
Start Key Held In — Start Key Released

A



B

ALD Reference
KC122
KA232
KC132
KC142
KA232
KL141
RA111
RA101
RA101
KY121
KY121
AV132
KL101
KD141



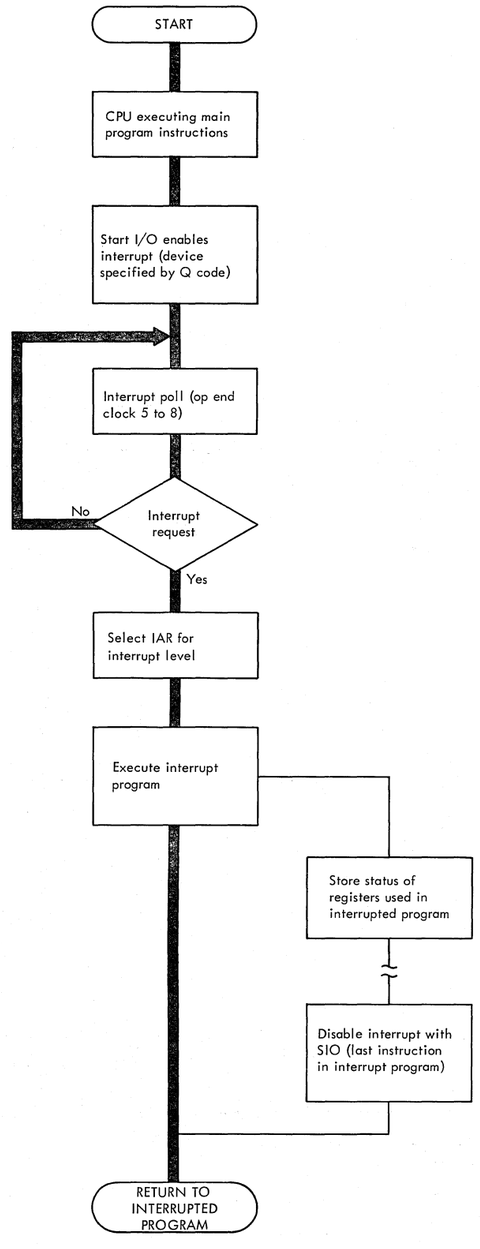
1 ▼ 2 ▼ 3

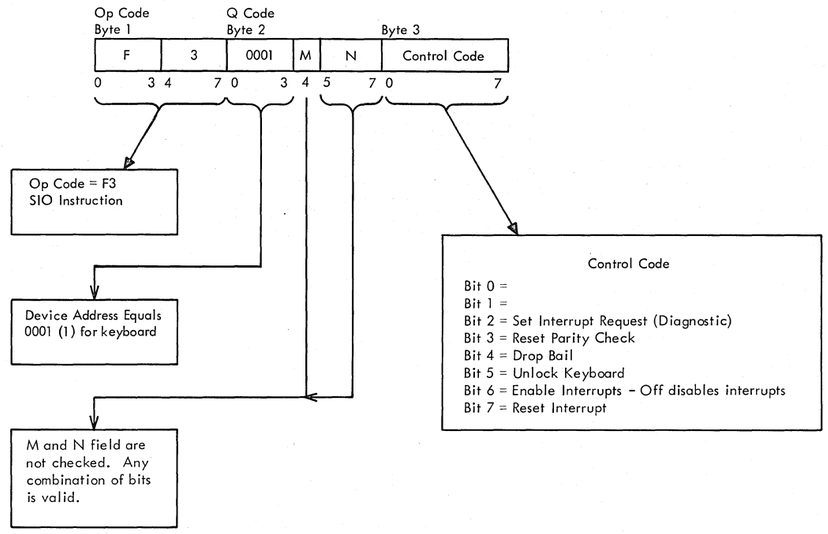
A

Interrupt

Objectives:

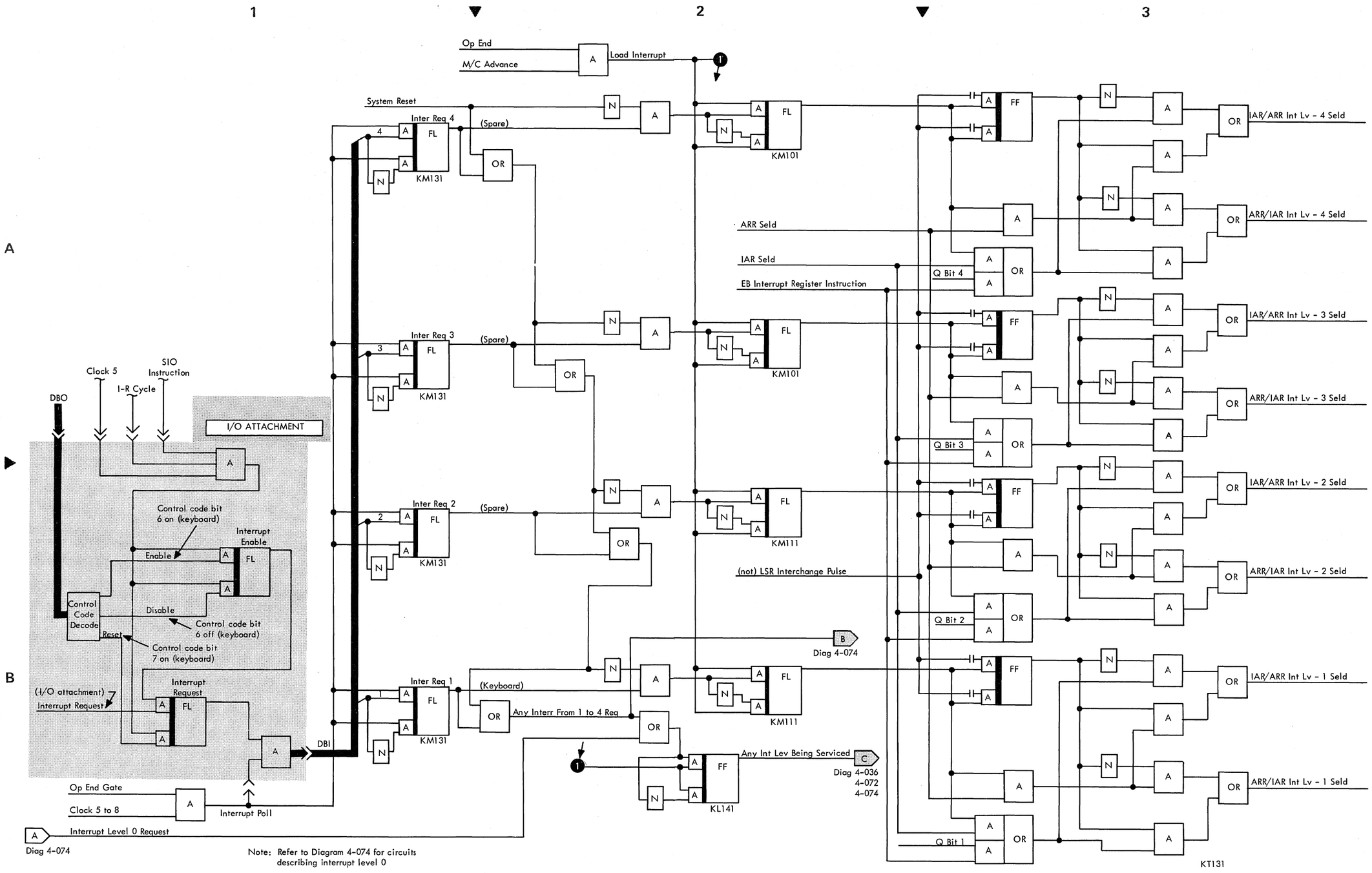
- Interrupt enable is turned on in I/O attachment by control code of SIO instruction
- I/O attachment sends interrupt request to CPU
- Interrupt occurs only after current instruction is finished
- Interrupts main program with separate program
- Highest interrupt device takes precedence over lower level devices
- Interrupt program ends with another SIO to disable interrupt





SIO Instruction Format for Keyboard (interrupt level 1)

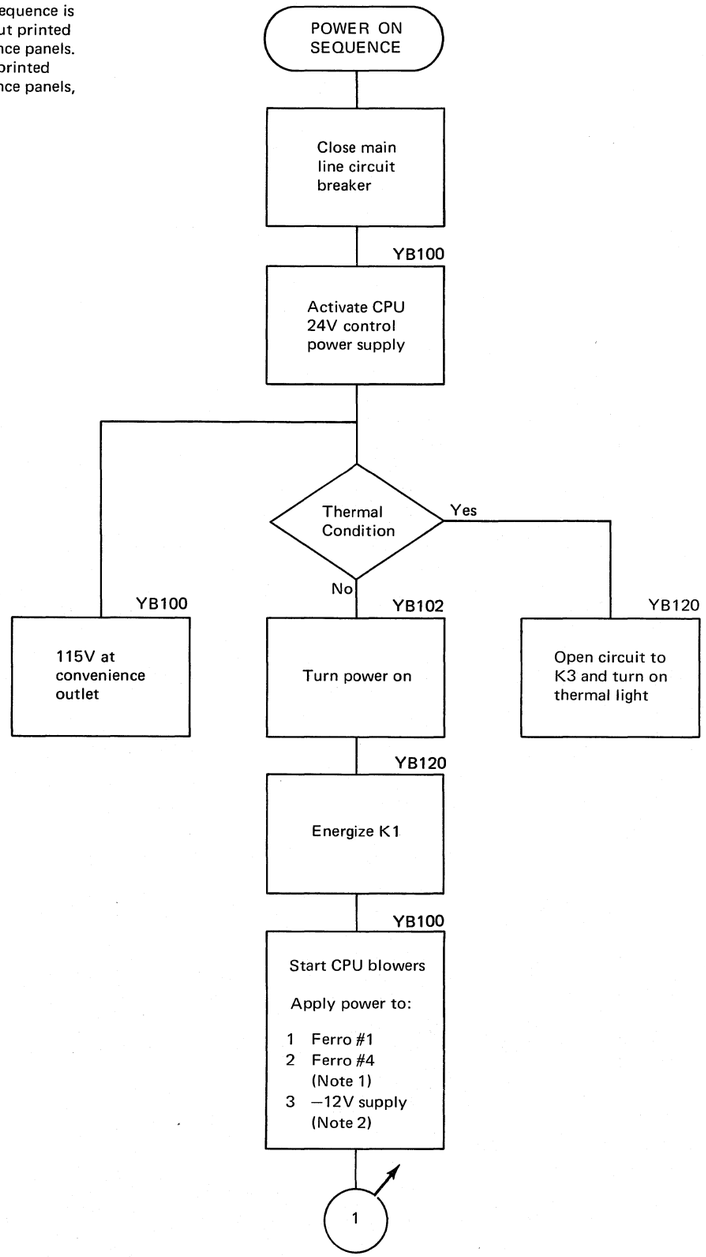
B



Note: Refer to Diagram 4-074 for circuits describing interrupt level 0

This power on-off sequence is for machines without printed circuit board sequence panels. For machines with printed circuit board sequence panels, see page 6-011.

1 ▼

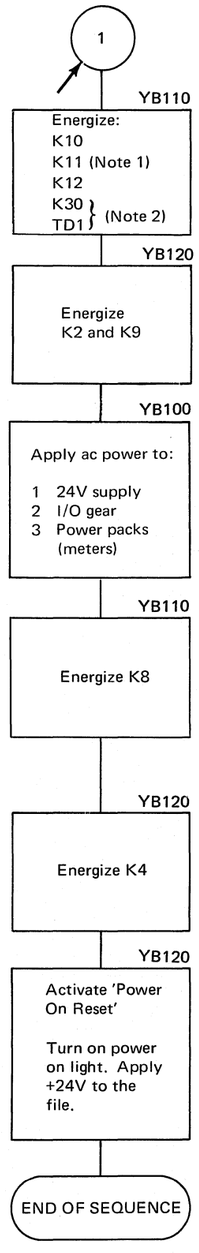


A

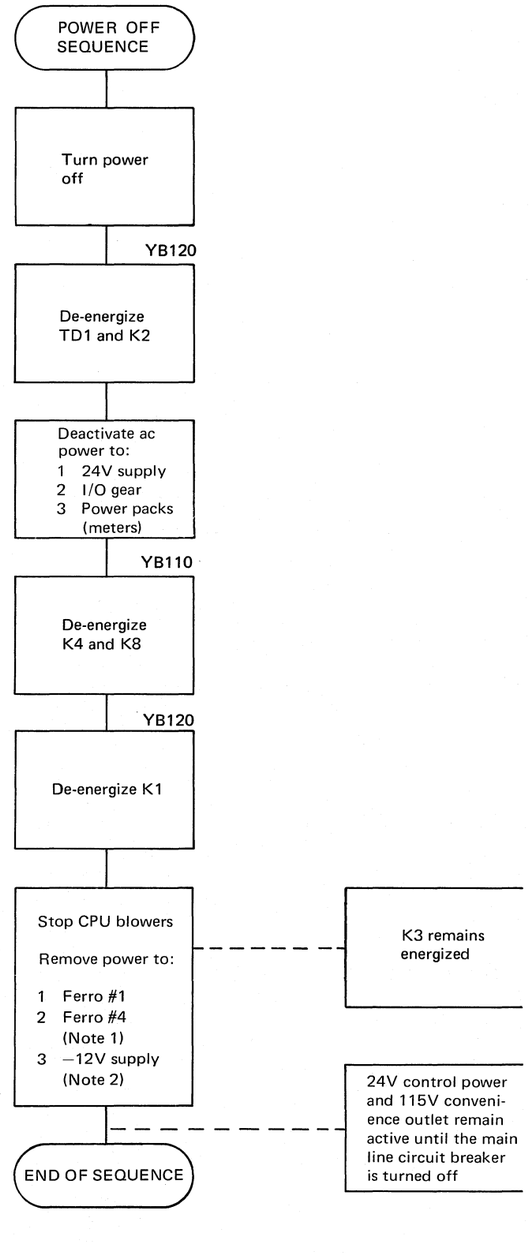
▶

B

2 ▼

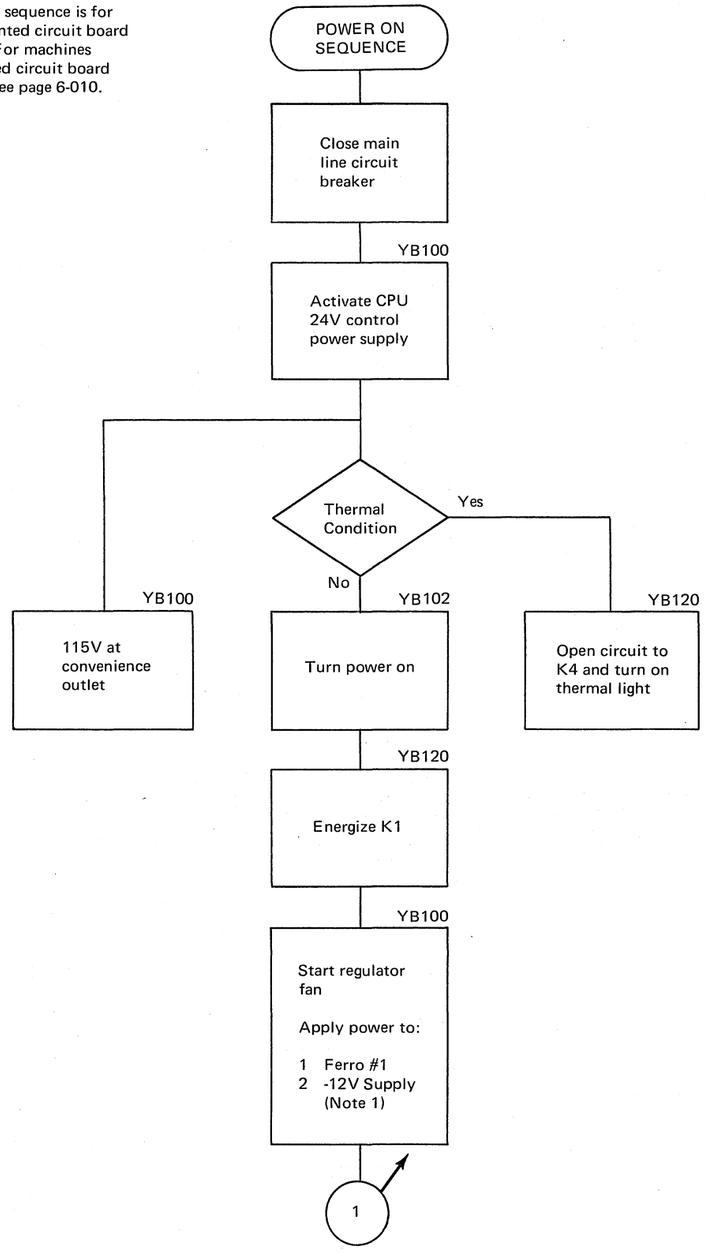


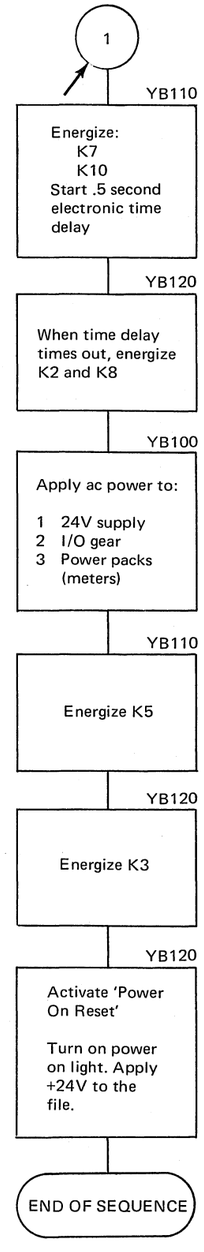
3

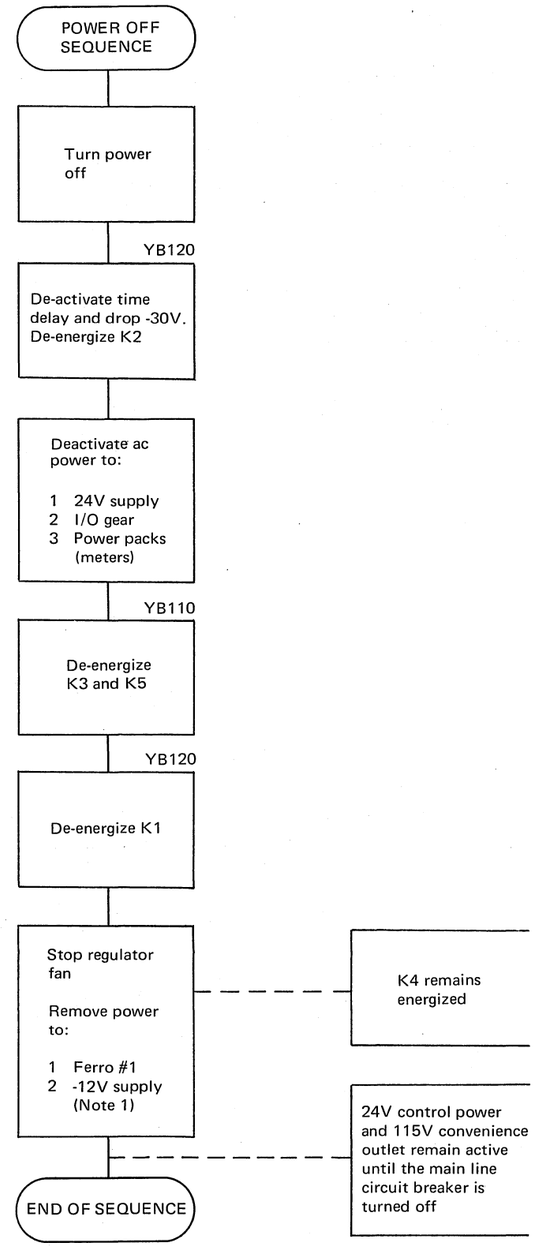


Note 1. Ferro #4 and K11 are required for B gate only (YB133).
Note 2. Required only for machines with BSCA medium speed (YB133).

This power on-off sequence is for machines with printed circuit board sequence panels. For machines without the printed circuit board sequence panels, see page 6-010.







Note 1. Required only for machine with BSCA medium speed (YB133).

Section 7. Keyboard and Console

This section of the 5406 FETMM contains the theory and maintenance diagrams for the operator console and the keyboard attachment. It consists of three chapters as follows:

Chapter 1. Introduction
Chapter 2. Functional Units
Chapter 3. Operations

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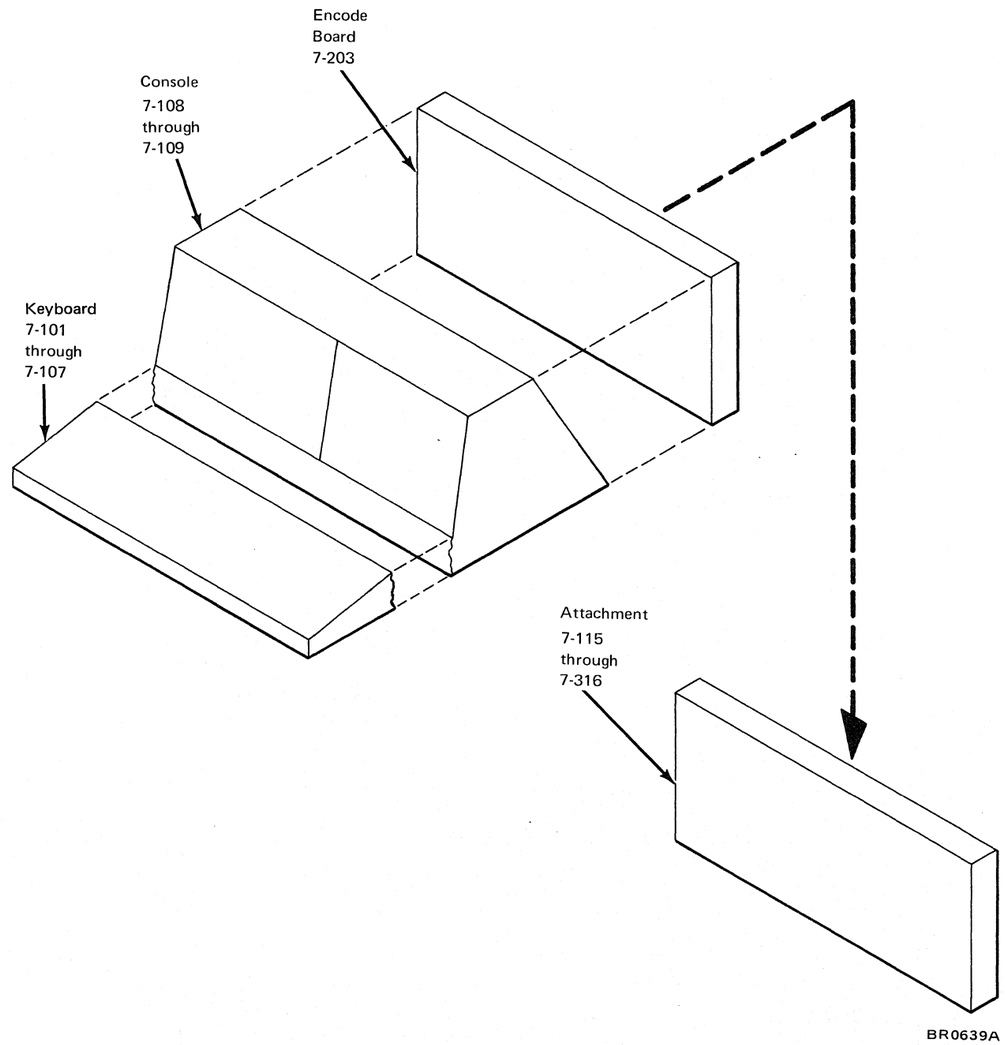
5406 KEYBOARD-CONSOLE

The model 6 can be controlled by an operator with the combination keyboard-console. The keyboard provides a means for data entry and the console provides system control and display.

This section of the 5406 FETMM contains the following information:

1. Keyboard description and key codes.
2. Console description of lights and switches.
3. Keyboard attachment including the encode board.

Electrical and mechanical timing for the keyboard appears on page 7-122. For further information concerning the basic keyboard, refer to the Field Engineering Theory-Maintenance Manual, *Elastic Diaphragm Encoded Key-Boards,* Order No. SY27-0073.



KEYBOARD

The operator keyboard-console for the model 6 provides the operator with the ability to control the system and to visually display many of the machine operations. Although comprised of two different components (the operator keyboard and the operator console), the keyboard-console is described in this section as one unit.

The keyboard and key codes are described in the first part of this section.

The keyboard is made up of four groups of keys:

Alpha-numeric and special character keys
Ten-key numeric keyboard
Function keys
Command keys

The alpha-numeric and special character keys are laid out similar to a typewriter keyboard. All of the characters found on the model B typewriter may be entered from this keyboard.

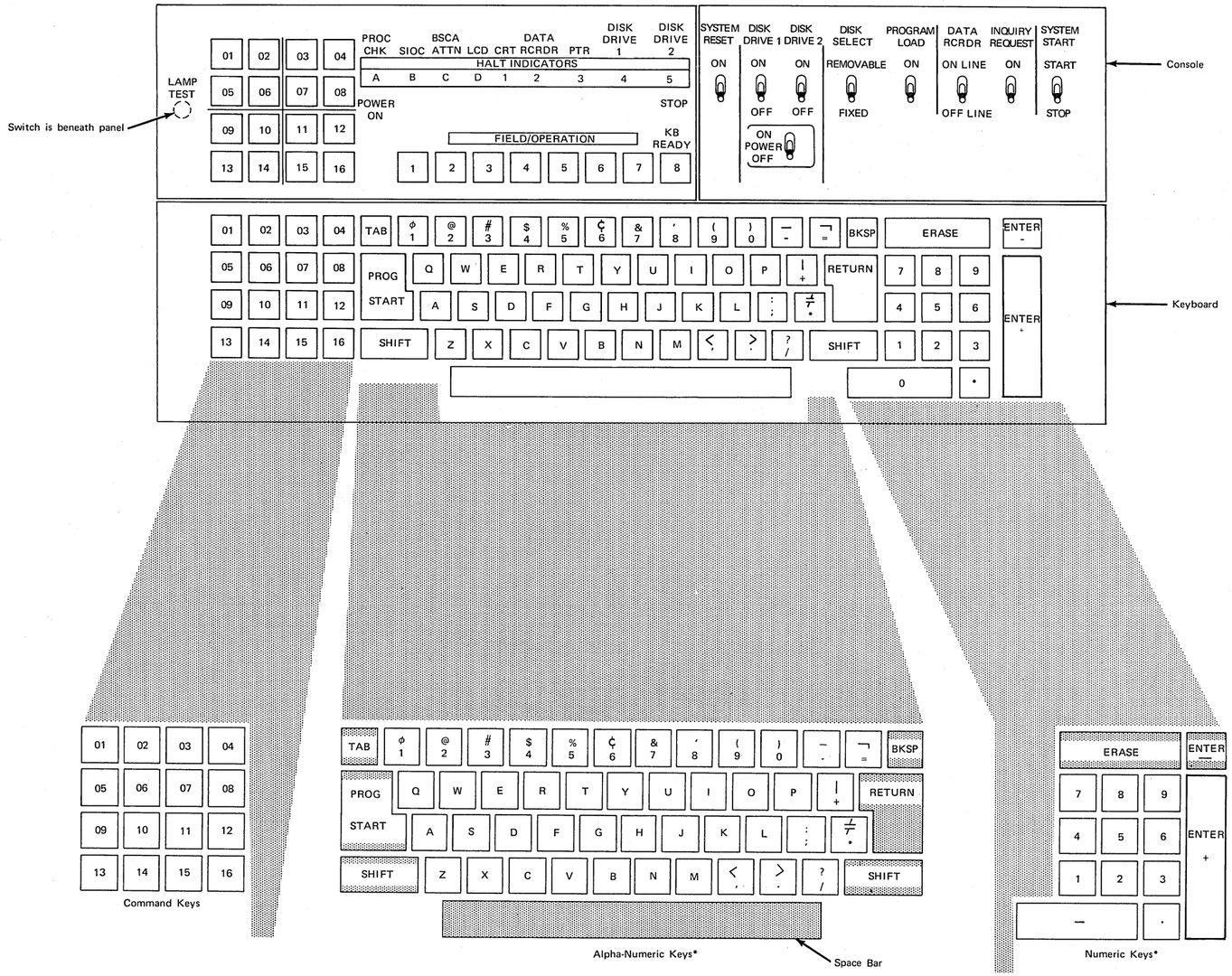
The ten-key numeric keyboard section is comprised of an adding machine type ten-key numeric cluster. Digits 0 through 9 may be entered with this section. Three of the function keys (ENTER +, ERASE, and ENTER –) are used in conjunction with these keys.

The ten function keys available are:

TAB
SHIFT (2)
BACKSPACE
INQUIRY REQUEST (located on the operator console)
PROGRAM START
RETURN
ENTER +
ENTER –
ERASE and the
Space bar.

There are eight basic command keys and indicators provided for operator influence over executing the program. The indicators are located on the operator console. Both the keys and indicators are numbered 01 through 08. An optional feature is available to increase the number of keys and indicators to 16.

The keys are mechanically interlocked in such a manner that simultaneous character generation is prevented and yet rolling of the keys is allowed. A start I/O instruction must be issued by the CPU enable keyboard interrupts, and unlock the keyboard (when operating in the process mode).



*Function keys are shaded.

BR0641A

KEY IDENTIFICATION SYSTEM

The position of each key on the keyboard is defined by the following notational system:

← L L designates keys located on the left hand side of the keyboard.
R → R designates keys located on the right hand side of the keyboard.
(a) Lower case alphabetic characters (a, b, c, d, and e) designate the key rows.
[1] Numerals represent the key position on the keyboard.

When needed, the words upper or lower are used to designate upper or lower case.

Example: Le10 is the left most key in the top row of keys.
Lc5 lower is a lower case *a.*

KEY OPERATION–PROCESS MODE

When the keyboard is ready (keyboard unlocked and interrupts enabled) and a key is pressed, an interrupt request is sent to the CPU. Two bytes are generated by pressing a key, a data byte and a status byte. These bytes are stored in the DBI assembler in the keyboard attachment. They are sent to the CPU during a sense instruction.

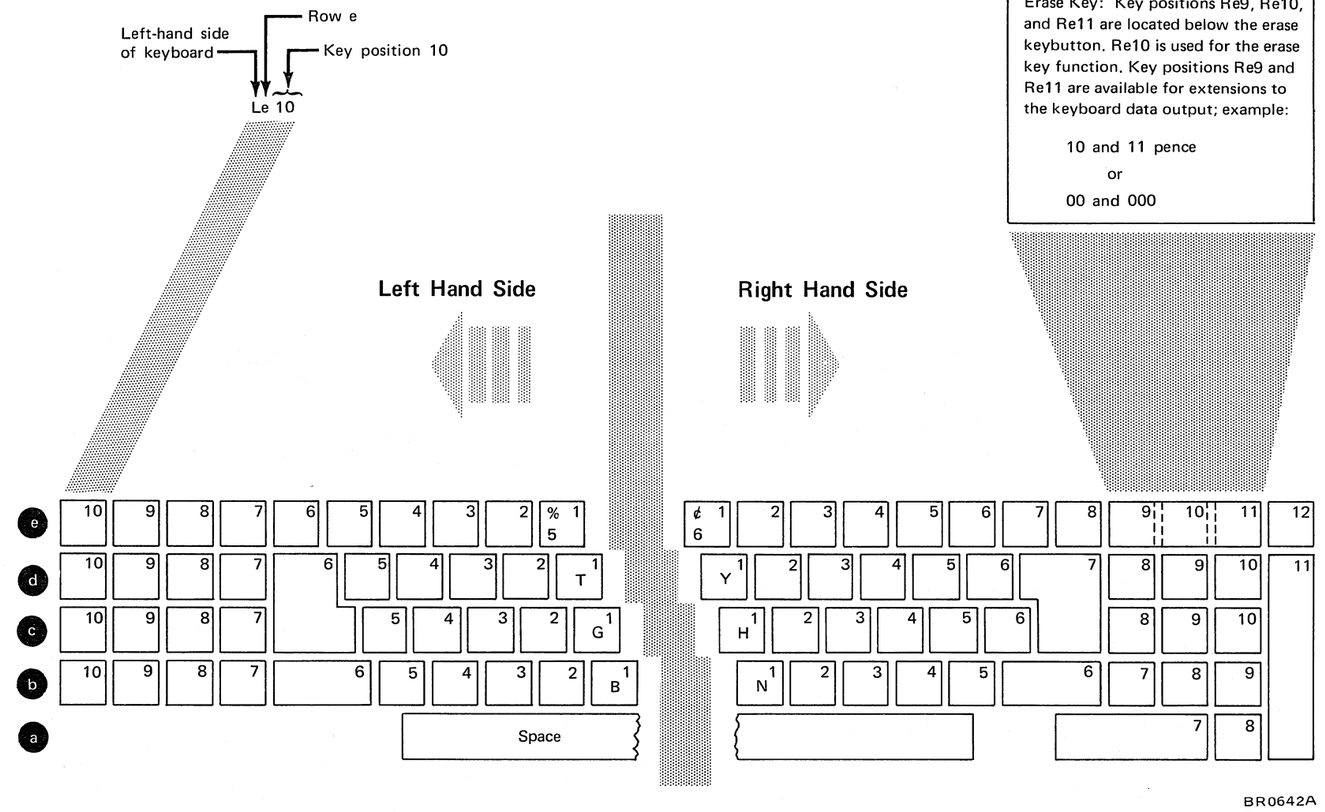
The first byte sent to the CPU is the status byte. This byte indicates the type of key pressed and the parity of the forthcoming data byte.

The second byte sent to the CPU is the data byte. The data byte is made up of a weighted code (eight bits and parity). It is called a weighted code because it represents the key position pressed rather than an EBCDIC, card code, or any other coded character that represents the graphic on the key button.

Keys that generate upper and lower case characters are controlled by the shift bar. They generate two bytes (status and data) in upper or lower shift.

The keyboard is assigned interrupt level 1. An interrupt is granted to the keyboard when no other device with a higher priority is polling for an interrupt. When the interrupt is granted, the CPU issues a sense instruction to the keyboard. During the sense instruction, the two bytes are sent to the CPU. The status byte is sent first followed by the data byte.

The status byte is stored in main storage in the address specified by the first operand address of the sense instruction. The data byte is stored in the specified operand address minus one.



WEIGHTED CODES

Each key position (except the shift key) has a weighted code assigned (8 bits plus odd parity). The command lights and field/operation lights are each assigned a weighted code so that the program can turn them on or off. The key code is sent to the CPU as the data byte of a sense instruction after that key has been pressed. The lights are turned on or off with a load I/O instruction.

The key position or light number, the weighted code, and the associated keybutton symbol (graphic) are shown for domestic and World Trade Corporation (WTC) keyboard-consoles.

Key Position	*Weighted Code 0123 4567*	*USA Key Symbol*
Le5 upper	0001 0001	↑
Le5 lower	0000 0001	1
Le4 upper	0001 0010	@
Le4 lower	0000 0010	2
Le3 upper	0001 0011	#
Le3 lower	0000 0011	3
Le2 upper	0001 0100	$
Le2 lower	0000 0100	4
Le1 upper	0001 0101	%
Le1 lower	0000 0101	5
Re1 upper	0001 0110	¢
Re1 lower	0000 0110	6
Re2 upper	0001 0111	&
Re2 lower	0000 0111	7
Re3 upper	0001 1000	'
Re3 lower	0000 1000	8
Re4 upper	0001 1001	(
Re4 lower	0000 1001	9
Re5 upper	0001 0000	)
Re5 lower	0000 0000	0 (zero)
Re6 upper	0011 1110	___ (underscore)
Re6 lower	0010 1110	–
Re7 upper	0011 1111	¬
Re7 lower	0010 1111	=
Ld5	0010 0100	Q
Ld4	0010 1010	W
Ld3	0000 1110	E
Ld2	0010 0101	R
Ld1	0010 0111	T
Rd1	0010 1100	Y
Rd2	0010 1000	U
Rd3	0001 1100	I
Rd4	0010 0010	O
Rd5	0010 0011	P
Rd6 upper	0011 1000	| (logical OR)
Rd6 lower	0011 0000	+
Ra2	0011 0001	. (See note)
Lc5	0000 1010	A
Lc4	0010 0110	S
Lc3	0000 1101	D
Lc2	0000 1111	F
Lc1	0001 1010	G
Rc1	0001 1011	H
Rc2	0001 1101	J
Rc3	0001 1110	K
Rc4	0001 1111	L
Rc5 upper	0011 1010	:
Rc5 lower	0011 0010	;
Rc6 upper	0011 1011	≠
Rc6 lower	0011 0011	*
Lb5	0010 1101	Z
Lb4	0010 1011	X
Lb3	0000 1100	C
Lb2	0010 1001	V
Lb1	0000 1011	B
Rb1	0010 0001	N
Rb2	0010 0000	M
Rb3 upper	0011 1100	<
Rb3 lower	0011 0100	,
Rb4 upper	0011 1101	>
Rb4 lower	0011 0101	.
Rb5 upper	0011 0111	?
Rb5 lower	0011 0110	/

Note: As an option for World Trade Corporation, the decimal point may be changed to a decimal comma.

Austria/Germany Key Position	*Weighted Code 0123 4567*	*WTC Character*	*Replaces USA Character*
Le4 upper	0001 0010	:	@
Le3 upper	0001 0011	;	#
Le2 upper	0001 0100	'	$
Re3 upper	0001 1000	?	'
Re7 upper	0011 1111	=	¬
Re7 lower	0010 1111	+	=
Rd1	0010 0111	Z	Y
Rd6 upper	0011 1000	¬	|
Rd6 lower	0011 0000	Ü	+
Rc5 upper	0011 1010	|	:
Rc5 lower	0011 0010	Ö	;
Rc6 lower	0011 0011	Ä	*
Lb5	0010 1101	Y	Z
Rb5 upper	0011 0111	*	?

Denmark Key Position	*Weighted Code 0123 4567*	*WTC Character*	*Replaces USA Character*
Le4 upper	0001 0010	:	@
Le3 upper	0001 0011	;	#
Le2 upper	0001 0100	'	$
Re3 upper	0001 1000	?	'
Rd6 upper	0011 1000	¬	|
Rd6 lower	0011 0000	Å	+
Re7 upper	0011 1111	=	¬
Re7 lower	0001 1111	+	=
Rc5 upper	0011 1010	|	:
Rc5 lower	0011 0010	Æ	;
Rc6 lower	0011 0011	Ø	*
Rb5 upper	0011 0111	*	?

Norway Key Position	*Weighted Code 0123 4567*	*WTC Character*	*Replaces USA Character*
Le4 upper	0001 0010	:	@
Le3 upper	0001 0011	;	#
Le2 upper	0001 0100	'	$
Re3 upper	0001 1000	?	'
Rd6 upper	0011 1000	*	|
Rd6 lower	0011 0000	/	+
Re7 upper	0011 1111	=	¬
Re7 lower	0001 1111	+	=
Rc5 upper	0011 1010	¬	:
Rc5 lower	0011 0010	Å	;
Rc6 lower	0011 0011	'	*
Rb3 lower	0011 0100	Ø	'
Rb4 lower	0011 0101	Æ	.
Rb5 upper	0011 0111	|	?
Rb5 lower	0011 0110	.	/

Belgium/France #1 Key Position	*Weighted Code 0123 4567*	*WTC Character*	*Replaces USA Character*
Le4 upper	0001 0010	'	@
Le2 upper	0001 0100	f	$
Le1 upper	0001 0101	(	%
Re1 upper	0001 0110	%	¢
Re3 upper	0001 1000	_	'
Ld5	0010 0100	A	Q
Re4 upper	0001 1001	¢	(
Ld4	0010 1010	Z	W
Re5 upper	0001 0000	à	)
Lc5	0000 1010	Q	A
Re6 upper	0011 1110	)	_
Lb5	0010 1101	W	Z

Belgium/France #2 Key Position	*Weighted Code 0123 4567*	*WTC Character*	*Replaces USA Character*
Le4 upper	0001 0010	'	@
Le2 upper	0001 0100	f	$
Le1 upper	0001 0101	(	%
Re1 upper	0001 0110	%	¢
Re3 upper	0001 1000	_	'
Re4 upper	0001 1001	¢	(
Re5 upper	0001 0000	à	)
Re6 upper	0011 1110	)	_

Finland/Sweden Key Position	*Weighted Code 0123 4567*	*WTC Character*	*Replaces USA Character*
Le4 upper	0001 0010	:	@
Le3 upper	0001 0011	;	#
Le2 upper	0001 0100	'	$
Re3 upper	0001 1000	?	'
Rd6 upper	0011 1000	*	|
Rd6 lower	0011 0000	/	+
Re7 upper	0011 1111	=	¬
Re7 lower	0001 1111	+	=
Rc5 upper	0011 1010	|	:
Rc5 lower	0011 0010	.	;
Rc6 upper	0011 1011	¬	≠
Rc6 lower	0011 0011	,	*
Rb3 lower	0011 0100	Å	,
Rb4 lower	0011 0101	Ä	.
Rb5 upper	0011 0111	≠	?
Rb5 lower	0011 0110	Ö	/

Spanish Speaking Key Position	*Weighted Code 0123 4567*	*WTC Character*	*Replaces USA Character*
Le3 upper	0001 0011	,	#
Re3 upper	0001 1000	?	'
Rc5 upper	0011 1010	<	:
Rc5 lower	0011 0010	Ñ	;
Rc6 upper	0011 1011	>	≠
Rb3 upper	0011 1100	;	<
Rb4 upper	0011 1101	:	>
Rb5 upper	0011 0111	≠	?
Le2 upper (For Spain Only)	0001 0100	Pts	$

United Kingdom

Le2 upper	0001 0100	£	$
Re1 upper	0001 0110	$	¢

Brazil/Portugal

Le2 upper	0001 0100	'	$
Le3 upper	0001 0011	Õ	#
Le4 upper	0001 0010	Ã	@
Re3 upper	0001 1000	?	'
Rc5 lower	0011 0010	M	;
Rc6 upper	0011 1011	;	≠
Rb2	0010 0000	ç	M
Rb3 lower	0011 0100	.	,
Rb4 lower	0011 0101	,	.
Rb5 upper	0011 0111	≠	?

KEYS AND LIGHTS

Command Keys

Key Position	*Code 0123 4567*	*Keytop Number*
Le10	0000 0001	01
Le9	0000 0010	02
Le8	0000 0011	03
Le7	0000 0100	04
Ld10	0000 0101	05
Ld9	0000 0110	06
Ld8	0000 0111	07
Ld7	0000 1000	08
Lc10	0000 1001	09
Lc9	0000 1010	10
Lc8	0000 1011	11
Lc7	0000 1100	12
Lb10	0000 1101	13
Lb9	0000 1110	14
Lb8	0000 1111	15
Lb7	0001 0000	16

Field/Operation Lights

Light Number	*Control Code*
1	1XXX XXXX
2	X1XX XXXX
3	XX1X XXXX
4	XXX1 XXXX
5	XXXX 1XXX
6	XXXX X1XX
7	XXXX XX1X
8	XXXX XXX1

Function Keys

Key Position	*Weighted Code 0123 4567*	*Name*
Le6	0000 0101	tab
Ld6	1000 0001	program start
Space	0100 0000	space
Rd7	0001 0101	return
Re8	0001 0110	backspace
Re10	0000 0011	erase
Rc11	1001 0001	enter +
Re12	0000 0010	enter –
Inquiry request (on console)	0001 0001	inquiry request

Numeric Keyboard Keys

Key Position	*Weighted Code 0123 4567*	*Basic Keytop Notation*
Ra1	0000 0000	0
Rb7	0000 0001	1
Rb8	0000 0010	2
Rb9	0000 0011	3
Rc8	0000 0100	4
Rc9	0000 0101	5
Rc10	0000 0110	6
Rd8	0000 0111	7
Rd9	0000 1000	8
Rd10	0000 1001	9
Re9	0000 0001	See note
Re11	0000 0010	See note

Note: These keys are located below, but not activated by, the erase key on the domestic keyboard. They are available for World Trade Corporation extensions (i.e., 10 and 11 pence or double and triple zero). When activated, they cause the status byte preceding the data byte to have bit 4 active. For the other keys in this table, the status byte will have bit 1 active.

KEY FUNCTIONS

Before a key can be operated, a keyboard start I/O instruction must be given to the CPU to enable interrupts and unlock the keys. All keys on the keyboard (except the shift key) cause an interrupt request to the CPU and generate two characters (status byte and data byte) from the keyboard into the attachment. The status and data bytes are transferred to the CPU when a sense instruction is issued to the keyboard.

Numeric Keyboard Keys

These keys are grouped on the right side of the keyboard. They are used to enter numeric data and a decimal point.

Status Byte	Data Byte
0100 0000	See "Weighted Codes"

Three function keys (Enter + Enter – and Erase) are associated with these keys for use in controlling the data entered.

Alpha-Numeric and Special Character Keys

These keys occupy the center portion of the keyboard and resemble an electric typewriter keyboard. All of the direct entry system graphics are entered from this section.

Status Byte	Data Byte
0100 0000	See "Weighted Codes"

Function Keys

The ten shaded keys (shown in the illustration on page 7-102) and the inquiry request switch on the console are called function keys. These keys are under program control to perform the function stated on the keybutton or console. Bit 3 of the status byte identifies the data byte as a function character. The programmed function of these keys follows.

Tab Key

This key has two levels of depression. When pressed down to the first level, the print element is spaced until the next programmed tab is sensed. When the key is pressed down to the second level, the weighted code continues to be sent to the CPU until the key is released. This operation is called typamatic and is accomplished through a combination of mechanical and program controls.

Status Byte	Data Byte
0001 0000	0000 0101

Backspace Key

This key has two levels of depression. When pressed down to the first level, the print element is spaced one position to the left. The program can either physically reposition the print element or merely readdress the previous address position in storage, whichever is appropriate for the operation in progress. When the key is pressed down to the second level, the weighted code continues to be sent to the CPU until the key is released. This operation is called typamatic and is accomplished through a combination of mechanical and program controls.

Status Byte	Data Byte
0001 0000	0001 0110

Program Start Key

When pressed, this key indicates to the program that the keyed in field is complete and may be acted upon; example: printed if desired.

Status Byte	Data Byte
0001 0000	0000 0001

Enter – Key

When pressed, this key indicates to the program that the keyed in field is complete and is a negative number.

Status Byte	Data Byte
0001 0000	0000 0010

Erase Key

When pressed, this key indicates to the program that the presently keyed field is to be deleted from storage.

Status Byte	Data Byte
0001 0000	0000 0011

Return Key

When pressed, this key causes the print element to return to the left margin and normally index one line. Indexing may or may not occur, depending on the program.

Status Byte	Data Byte
0001 0000	0001 0101

Enter + Key

This key indicates to the program that the keyed in field is complete and is a positive number.

Status Byte	Data Byte
0001 0000	0001 0010

Inquiry Request Switch

This switch is located on the console. Interrupt level 1 must be enabled to recognize this switch. The switch is not under keyboard bail interlock control. When activated, it normally indicates to the program that a keyboard operation is desired and requests that the keyboard be unlocked.

Status Byte	Data Byte
0001 0000	0001 0001

Space Bar

The space bar accomplishes the same result as in standard typewriter use. When this key is pressed, the print element is programmed to advance one position to the right, either by printing a blank, or a tab right command.

Status Byte	Data Byte
0001 0000	0100 0000

Shift Keys

There are two of these keys, one located on either side of the bottom row of alpha-numeric keys. These keys have the same function; they do not request an interrupt or generate a weighted code, but condition the encode logic for upper shift characters (numeric and special characters).

Command Keys

The command keys are grouped to the left side of the keyboard. Eight command keys are standard. An optional feature provides an additional eight command keys. The standard keys are labeled 01 through 08. The optional keys are labeled 09 through 16.

The program assigns functions to these keys to permit the operator to influence the execution of the program routine. Command key lights are used to signify that the associated key function is in effect.

Bit 2 of the status byte identifies the data byte as a command character. The code associated with the command keys and lights is shown in "Weighted Codes."

CONSOLE

The operator console contains the switches and lights necessary for operator control of the system. It is divided into two sections: system indicator lights, and system control switches.

System Indicator Lights

The system indicator lights section is divided into six parts. They are: system check lights, halt code indicator lights, field/operation indicator lights, keyboard ready light, command key indicator lights, and the system power on light.

Individual attention lights are provided for disk 1, disk 2, CRT, ledger card device, data recorder, SIOC, BSCA, and printer. The processor check light is also displayed on the console.

The halt indicator group of lights are provided for use under program control to indicate to the operator a cause for system halt. They are: stop light, and nine halt indicator lights.

The field/operation group of lights consists of eight lights which may be labeled by use of a plastic overlay. The program uses these lights to inform the operator at what point in the program he may enter specific data fields or take specific action.

The command key indicator light group consists of eight (standard) or sixteen (feature) lights that are associated with the command keys on the operator keyboard. When the operator presses a command key, the program lights the associated command light on the console. When a command key is pressed and the associated command light is on, the program will turn off that light. In addition, the program can light a specific command key light whenever there is a need to communicate a predefined condition to the operator. Plastic overlays are provided for the lights so that the significant meaning for a light can be changed by typing on the overlay.

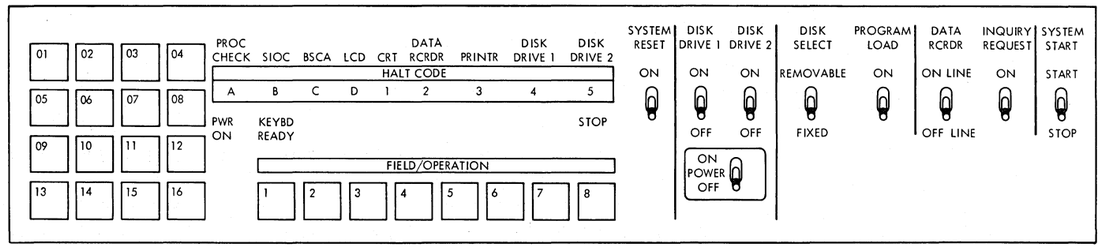
System Control Switches

The system control switches section includes those switches required for system powering, program loading, system starting, stopping, resetting, and configuring.

SWITCHES

System Start Switch

When this switch is moved to the start position the processor turns off the halt code lights and resumes normal operation. When this switch is moved to the stop position the processor halts at the end of the operation in process. This halt is indicated by turning on the stop light on the console. I/O data transfers are completed without loss of information. The system can be restarted without loss of information only by setting the switch to the start position.



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Inquiry Request Switch

This switch is mounted on the console, and although this key is not under keyboard bail interlock control, it operates as though it were a key on the keyboard. Moving this switch to the on position causes the data and status bytes to be stored in the keyboard encode circuitry. Interrupt level one must be enabled for the CPU to recognize this switch. The status byte has the function key bit (bit 3) on and the data byte contains the unique data character code for the inquiry request key (0001 0001).

Data Recorder Switch

Moving this switch to the on line position places the data recorder under program control when the verify-punch switch on the data recorder is in the punch position. The data recorder keyboard is disabled, data can be entered into the system from the data recorder reading station, data can be punched at the data recorder punching station, and data and control can be entered from the system keyboard-console.

Moving this switch to the off line position places the data recorder under its own control and allows it to function as a normal (off-line) data recorder.

Program Load Switch

This switch initiates loading the program into main storage. The following actions occur when this switch is operated to the on position:

1. All I/O and machine registers, controls, and status indicators are reset.
2. The instruction address register is set to zero.
3. The disk file data address register is reset to zero. The record in cylinder zero, sector zero on one of the disks in disk drive one is read into storage starting at location 0000. The disk that provides the first record is selected by the setting of the disk select switch on the console.

When the program load switch is released, the processing unit executes the instructions read into storage from cylinder zero, sector zero, starting at location 0000.

If disk drive one is not ready, its I/O attention light is turned on. When the program load switch is operated, it is necessary only to make disk drive one ready to complete the program load function.

Disk Select Switch

This switch selects the disk from which the initial program load will be performed. When the switch is moved to the removable position, sector zero of cylinder zero, of the removable disk is used for program loading. Similarly, when the switch is in the fixed position, sector zero of cylinder zero, of the fixed disk on disk drive one is used for program loading.

Disk Drive 1 and Disk Drive 2 Switches

These switches turn power on or off to the disk drive motors.

Power Switch

This switch controls the power to the system. When this switch is turned on, a system reset is performed in such a manner that no I/O operations are performed until explicitly directed. Unless the stop switch is actuated before power off switch is used, the integrity of data in storage is not quaranteed after this switch is operated. When the switch is turned off, power is dropped in the CPU and all I/O devices connected to the system.

When the switch is turned on, the keyboard is locked, all indicator lights are turned off, and interrupts are disabled. An initializing start I/O instruction is required to unlock the keyboard and enable interrupts to allow keyboard operation ('KB Ready').

CONSOLE LIGHTS

Processor Check Light

The processor check light turns on when an invalid op code or parity error is detected in the CPU. It is also turned on when an invalid Q code is detected. It is turned off by system reset or pressing the check reset key on the CE panel. Any of these errors causes the processing unit to come to an immediate stop, the clock is stopped and the input/output data may be lost. The specific error that caused the stop is displayed on the CE console.

I/O Attention Lights

When any one of the following lights is on, it indicates that the corresponding I/O device has been issued a start I/O instruction but it is not ready to operate. A not ready condition can be caused by power not being on or by some condition involving the paper or cards to be handled by the I/O device. The I/O attention indicators are SIOC, BSCA ATTN, LCD, CRT, DATA RCRDR, PRINTER, DISK DRIVE 1, and DISK DRIVE 2. The specific conditions that cause each I/O light to turn on are discussed under the individual I/O devices.

Halt Code Lights

These lights are turned on by the individual bits (nine), and the halt indicator, halt identifier bytes of the halt program level instruction.

Power On Light

This light is turned on when system-power-on sequencing has been successfully completed and stays on until system power is turned off.

Keyboard Ready Light

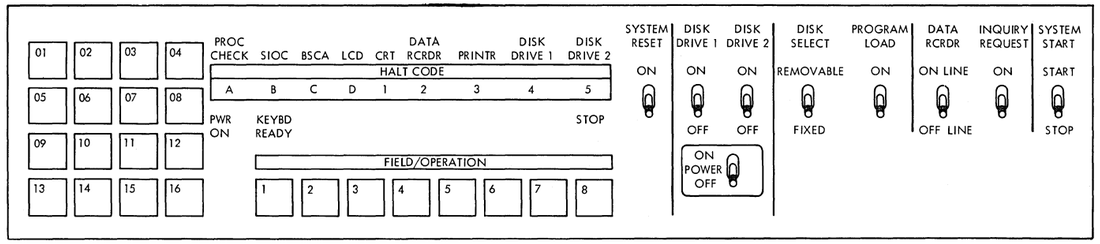
This light is on when the keyboard has been enabled and unlocked.

Stop Light

This light is turned on when the system start switch is moved to the stop position and is turned off by moving the system start switch to the start position, or by system reset.

Field/Operation Lights

These lights are turned on by a load I/O operation. The meaning of each light is determined by the program being used. A plastic overlay is provided for the field/operation lights so that appropriate labels can be applied. These labels identify the particular meaning given to the lights by the programmer. Once turned on, the field/operation lights remain on until another load I/O specifying the field/operation lights is executed.



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Command Key Lights

These lights are controlled by the load I/O instruction. Separate load I/O instructions are used for turning on or turning off command lights. Once turned on, command lights remain on until a load I/O instruction turns them off, or until a system reset takes place. A plastic overlay is provided for the command lights so that appropriate labels can be assigned to each command light in order to identify the particular meaning given to the light by the programmer.

(Pages 7-110 through 7-114 deleted.)

KEYBOARD ATTACHMENT

The keyboard attachment is the interface between the processing unit and the operator keyboard. The attachment consists of five circuit cards. Two of these cards are MST circuitry and are two-high, four-wide cards located in 01-frame, A-gate, on B1-board, at L2 and M2 (B1L2 and B1M2). The other three cards are used to convert the keyboard SLT circuitry outputs to MST. These three cards are located at B1G2, B1K2, and B1K3.

Keyboard/CPU Interface

The keyboard console and attachment operate under program control. The attachment communicates with the CPU during interrupts; information is sent to the CPU main storage upon receiving a sense I/O instruction.

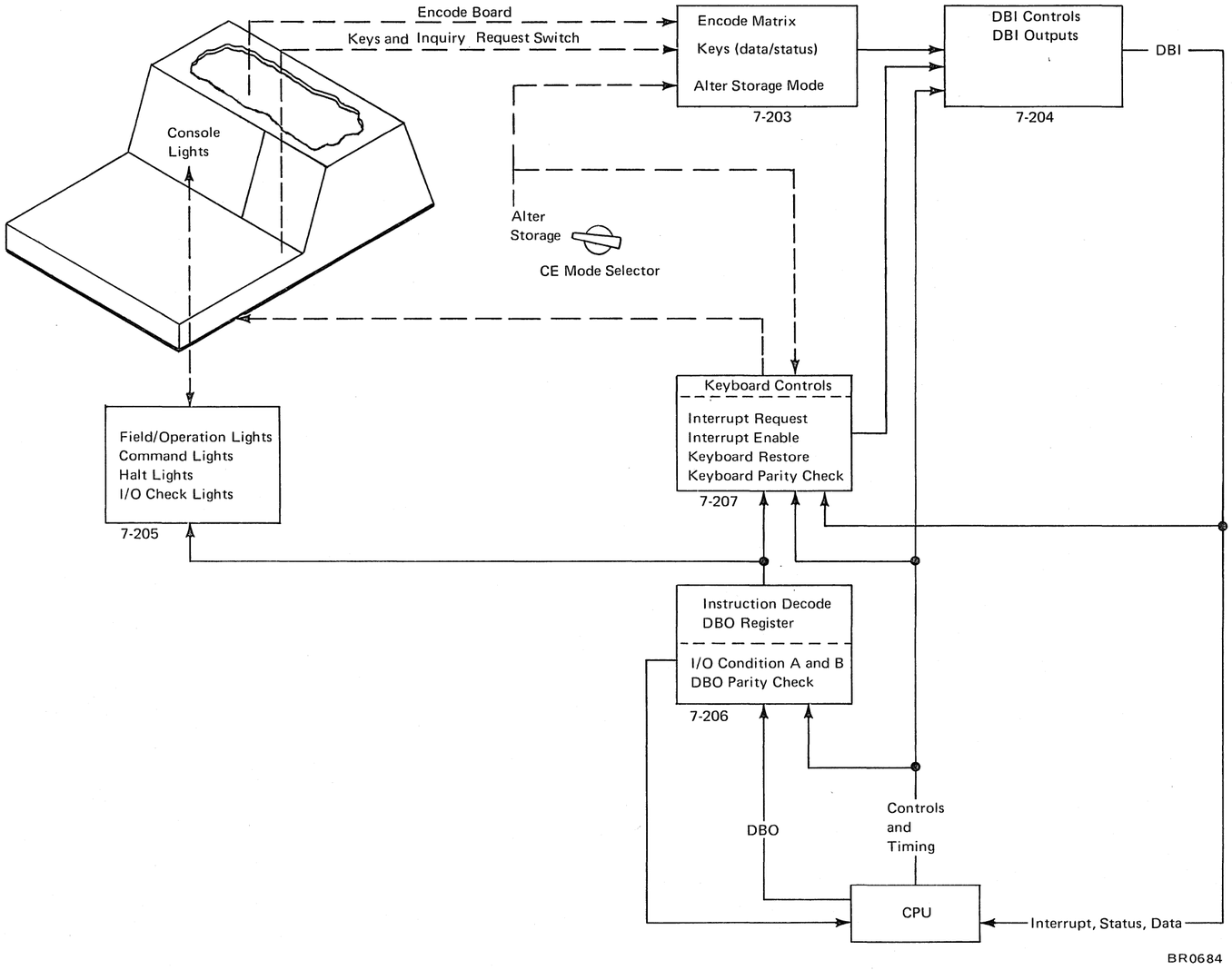
The attachment operates on interrupt level number one, which is interrupt number four in interrupt priority (lowest level).

All instructions are sent to the attachment on data bus out lines and control lines. The attachment decodes the instructions to determine whether the operation is a load I/O, start I/O, or sense I/O, and turns on a latch to set up controls for the forthcoming data information.

The keyboard keys are disabled until a start I/O instruction (with the appropriate bits active in the control code) restores them. Once the keyboard is restored, and interrupts are enabled, information can be keyed. Pressing one of the keyboard keys causes two actions:

1. Two bytes are stored in the keyboard attachment circuitry. The first of these bytes is a status byte that defines whether: (1) the key pressed is a data character key, a command key, a function key, or a World Trade key; (2) the keyboard is ready; or (3) the key is a typamatic key. The second byte is the data byte.
2. An interrupt request on interrupt level 1 is generated.

If no higher priority interrupt is being serviced, the CPU honors the interrupt request and branches to the interrupt subroutine. The interrupt subroutine must perform a sense I/O instruction to transfer the two bytes stored in the attachment circuitry into storage. The routine must also restore the keyboard and reset the interrupt request by issuing another start I/O instruction.



(Pages 7-110 through 7-114 deleted.)

LOAD I/O INSTRUCTION

- Three or four bytes make up the load I/O instruction.
- The load I/O instruction selects the keyboard when the device address equals 1 (hexadecimal).
- The M field of the load I/O instruction is not used by the keyboard and may be any value.
- The N field of the load I/O instruction is bit significant in the two low order bits and the high order bit (bit 5 of the Q byte) may be either 0 or 1.
- The control byte transfers the one byte field located at the operand address and the one byte field at the operand address minus one (which is not used) to the attachment circuitry.
- This instruction is used to turn on or off field/operation indicators or to turn on or off command indicators.

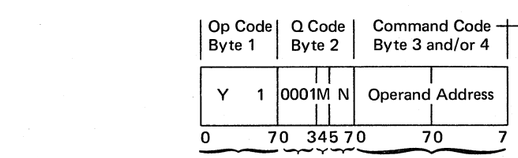
This instruction causes two bytes of information to be sent to the keyboard attachment for the purpose of controlling lights on the console.

The instruction is composed of three or four bytes. The first byte is the op code, a Y1 (hexadecimal) for a load I/O instruction. The second byte contains the device address (hexadecimal 1 for the keyboard), an M bit that may be either 0 or 1, and the N code that selects either the command lights or the field/operation lights. The byte field located at the operand address is transferred to the attachment for turning on or off individual lights within the group selected by the N code.

Load I/O Turn On Command Lights

- The N field equals X01.
- Two bytes of information are sent from main storage to the attachment; the first byte from the main storage address specified by the operand one address, and the second byte from the address of the first operand address minus one.
- The first byte is the active byte and selects the desired command key lights to be turned on for one of the two following reasons:
  1. The corresponding command key was pressed on the keyboard.
  2. The program desired to turn on the light as a communication to the operator.
- The second byte of information sent to the attachment is not used.
- The command light whose decimal label corresponds to the decimal value of the binary number in the rightmost byte of the operand is turned on.
- If only the eight basic command keys are installed, binary values more than 8 in the operand byte are ignored.

LOAD I/O (LIO) INSTRUCTION FORMAT



The command code (two-byte field located at the operand one address and operand one address minus one) is sent from the CPU to the attachment on DBO lines. The rightmost byte (operand one address) of the operand is bit significant in turning on or off specific lights in the group defined in the N field. The leftmost byte (operand one address minus one) is not used.

Op Code = Y1 (hexadecimal)
Y can = 0011 or
0111 or
1011

Device Address = 1.
This is DBO 3 bit on during IO cycle for keyboard.

M field is not used for the keyboard attachment. It can be either 1 or 0.

N field - Defines the group of lights to be turned on or off. Only bits 6 and 7 are bit significant (bit 5 can be any value).

N = 010 LIO Field/Operation Lights

Light No.	Command Code 0 1 2 3 4 5 6 7
1	1XXX XXXX
2	X1XX XXXX
3	XX1X XXXX
4	XXX1 XXXX
5	XXXX 1XXX
6	XXXX X1XX
7	XXXX XX1X
8	XXXX XXX1

The active bit (1) as shown will turn on the light in the light number column. The selection of a light or lights will automatically turn off the non-selected lights. All bits being zero will turn off all the lights.

N = 001 LIO Turn On Command Lights

N = 000 LIO Turn Off Command Lights

Light No.	Command Code	Light No.	Command Code
01	0000 0001	09	0000 1001
02	0000 0010	10	0000 1010
03	0000 0011	11	0000 1011
04	0000 0100	12	0000 1100
05	0000 0101	13	0000 1101
06	0000 0110	14	0000 1110
07	0000 0111	15	0000 1111
08	0000 1000	16	0001 0000

Command codes other than those shown here will be accepted by the attachment, but no command light will be turned on or off as a result.

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Load I/O Turn Off Command Lights

- The N field equals X00.
- Two bytes of information are sent from main storage to the attachment; the first byte from the main storage address specified by the operand one address, and the second byte from the address of the first operand address minus one.
- The first byte is the active byte and selects the desired command key lights to be turned off for one of the two following reasons:
  1. The corresponding key was pressed on the keyboard when the light was on.
  2. The program desired to turn the light off as a communication to the operator.
- The second byte of information sent to the attachment is not used.
- The selected command key function is no longer active after the program turns the light off as a communication to the operator (see 2. above).
- The command light whose decimal label corresponds to the decimal value of the binary number in the rightmost byte of the operand is turned off.
- If only the eight basic command keys are installed, binary values more than 8 in the operand byte are ignored.

Load I/O Field/Operation Lights

- The N field equals X1X.
- Two bytes of information are sent from main storage to the attachment; the first byte from the main storage address specified by the operand one address, and the second byte from the address of the first operand address minus one.
- The first byte is the active byte and selects the desired field/operation lights to be turned on.
- The selection of specific lights to be turned on automatically resets all the non-selected lights (hexadecimal 00 turns off all the lights).
- The second byte of information sent to the attachment from main storage is not used.

TEST I/O AND ADVANCE PROGRAM LEVEL INSTRUCTION

Test I/O (TIO) Instruction

- The keyboard attachment does not respond to this instruction.
- Issuing this instruction to the keyboard console results in a processor check with invalid Q indication issued with the keyboard console device address.

Advance Program Level (APL) Instruction

- The keyboard attachment does not respond to this instruction.
- Issuing this instruction to the keyboard console results in a processor check with invalid Q indication issued with the keyboard console device address.

SENSE I/O INSTRUCTION

- Four bytes make up the sense instruction.
- The sense instruction selects the keyboard when the device address equals 1 (hexadecimal).
- The M and N fields of the sense instruction are not used by the keyboard and may be any value.
- This instruction places the data available in the keyboard attachment into the field in storage specified by the first operand address.

The sense instruction is composed of four bytes. The first byte is the op code, a Y0 (hexadecimal) for a sense instruction. The second byte contains the device address (DA), and an M and N field that are not used. The third and fourth bytes contain the address of the low order byte of the two byte field where the sense bytes will be stored.

Response to Sense Keyboard Instruction

- The code for the key position pressed is transferred from the attachment circuitry to the CPU.

In response to a sense keyboard instruction, two bytes (representing the key position pressed) are gated on 'data bus in' (DBI) for storage in the two-byte field specified by the first operand address minus one, and the first operand address.

The high-order byte stored in storage is a status byte and is bit significant. This byte defines the low-order byte that is to be transferred to the CPU on the next cycle.

The second byte (low-order) in storage contains the unique bit configuration for the particular key position pressed.

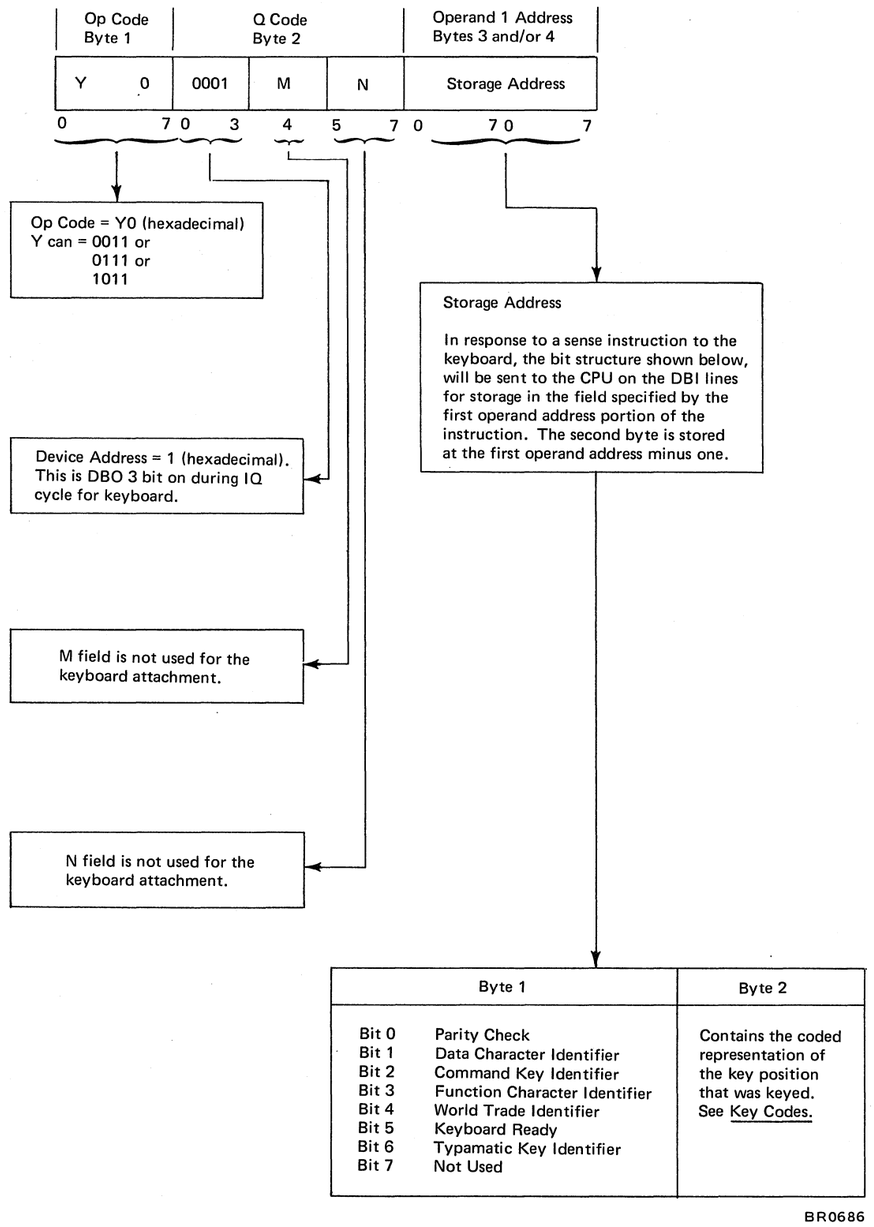
If a sense keyboard instruction is issued by the program before a key is pressed (no interrupt request generated), the status byte will be:

parity check
1000 0000

the second byte (data or function character keyed) will be:

0000 0000

SENSE I/O (SNS) INSTRUCTION FORMAT



START I/O INSTRUCTION

- Three bytes make up the start I/O instruction.
- The start I/O instruction selects the keyboard when the device address equals 1 (hexadecimal).
- The M and N fields of the start I/O instruction are not used by the keyboard and may be any value.
- The control code of the start I/O instruction causes the keyboard and attachment circuitry to perform the operations specified by the control code.

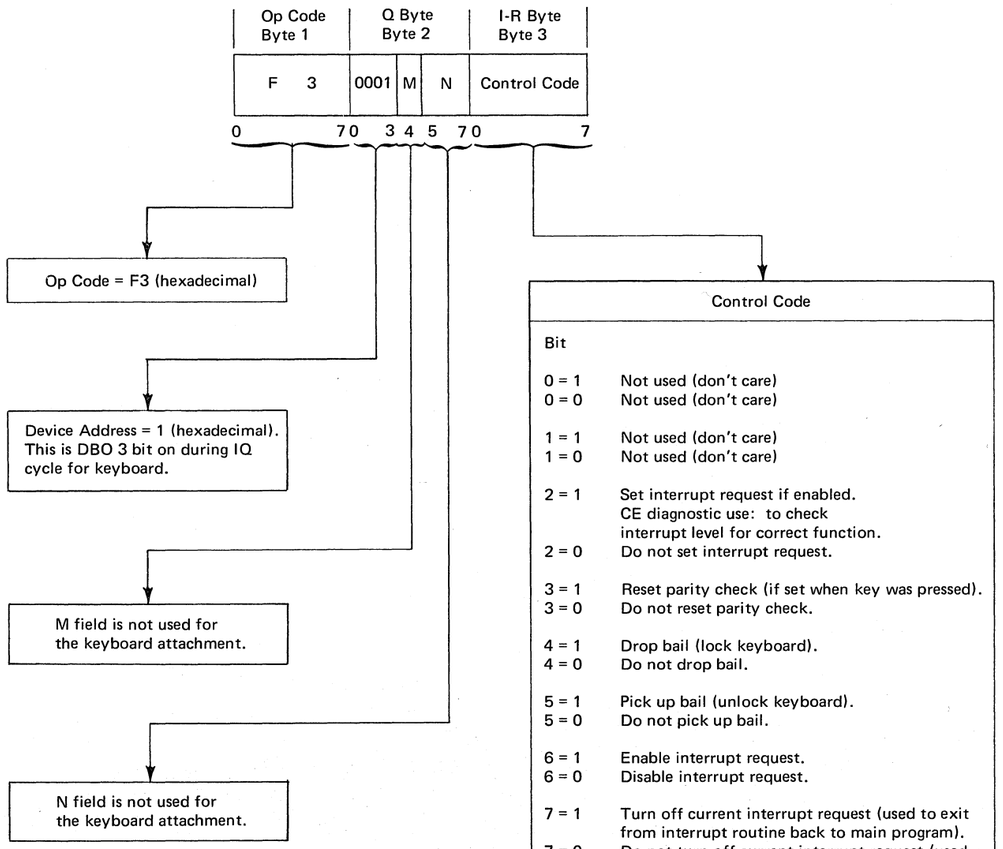
This instruction is composed of three bytes. The first byte is the op code, a F3 (hexadecimal) for a start I/O instruction; the second byte contains the device address (a hexadecimal 1 assigned to the keyboard) and the M and N fields (not used in the attachment circuitry); and the third byte contains the control code to provide control information for the keyboard operation.

The control code of the start I/O instruction is used by the programmer to:

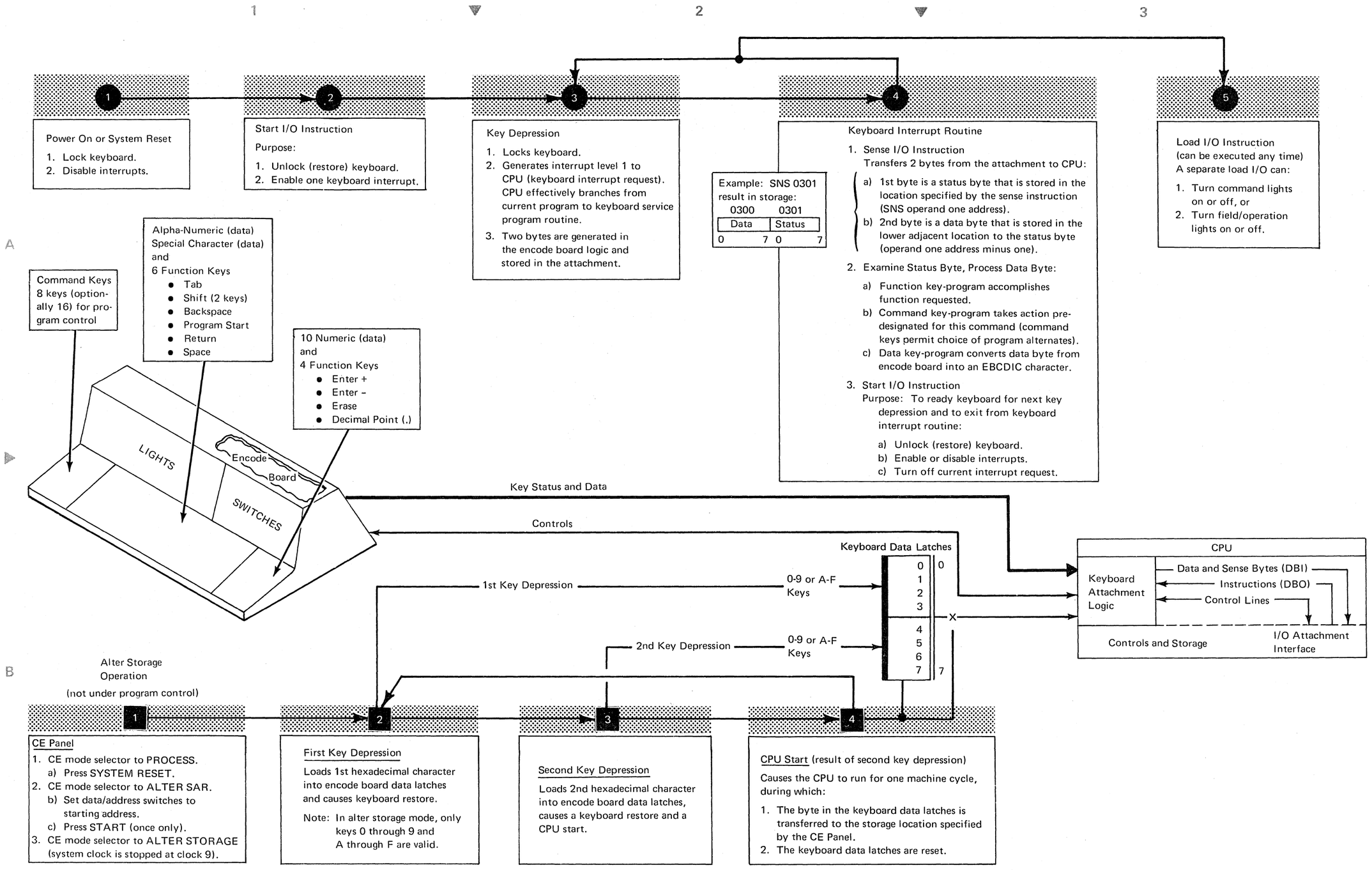
1. Reset previously sensed parity checks.
2. Lock or unlock the keyboard.
3. Enable or disable interrupts.
4. Turn off current interrupt requests.
5. Restore (unlock) the keyboard (required to prepare the keyboard for a succeeding key depression).
6. Cause an interrupt request (see bit 2 in "Control Code" chart).

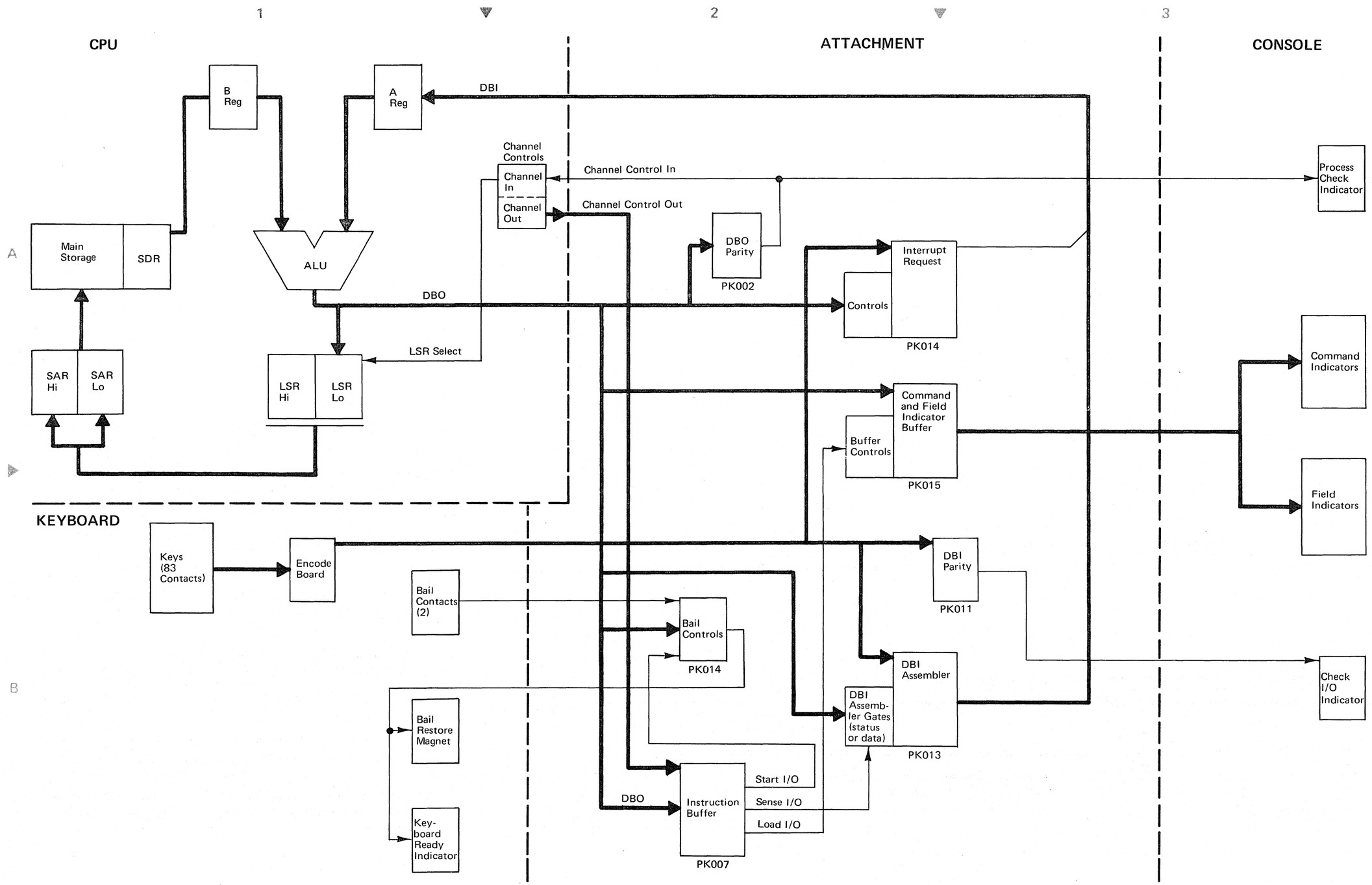
The restore keyboard function, necessary to unlock the keyboard for a succeeding key operation, is accomplished by issuing a start I/O instruction with both bits 4 and 5 present. All bit combinations of the control field are valid and all operations will be performed if the appropriate bits are on, except that bits 2 and 7 on will not result in interrupt request being set.

START I/O (SIO) INSTRUCTION FORMAT



BR0687


1
2
3
A
B
1
Power On or System Reset
1. Lock keyboard.
2. Disable interrupts.
2
Start I/O Instruction
Purpose:
1. Unlock (restore) keyboard.
2. Enable one keyboard interrupt.
3
Key Depression
1. Locks keyboard.
2. Generates interrupt level 1 to CPU (keyboard interrupt request). CPU effectively branches from current program to keyboard service program routine.
3. Two bytes are generated in the encode board logic and stored in the attachment.
Example: SNS 0301
result in storage:
0300 0301
Data Status
0 7 0 7
4
Keyboard Interrupt Routine
1. Sense I/O Instruction
Transfers 2 bytes from the attachment to CPU:
a) 1st byte is a status byte that is stored in the location specified by the sense instruction (SNS operand one address).
b) 2nd byte is a data byte that is stored in the lower adjacent location to the status byte (operand one address minus one).
2. Examine Status Byte, Process Data Byte:
a) Function key-program accomplishes function requested.
b) Command key-program takes action predesignated for this command (command keys permit choice of program alternates).
c) Data key-program converts data byte from encode board into an EBCDIC character.
3. Start I/O Instruction
Purpose: To ready keyboard for next key depression and to exit from keyboard interrupt routine:
a) Unlock (restore) keyboard.
b) Enable or disable interrupts.
c) Turn off current interrupt request.
5
Load I/O Instruction
(can be executed any time)
A separate load I/O can:
1. Turn command lights on or off, or
2. Turn field/operation lights on or off.
Command Keys
8 keys (optionally 16) for program control
Alpha-Numeric (data)
Special Character (data)
and
6 Function Keys
Tab
Shift (2 keys)
Backspace
Program Start
Return
Space
10 Numeric (data)
and
4 Function Keys
Enter +
Enter –
Erase
Decimal Point (.)
LIGHTS
Encode
Board
SWITCHES
Key Status and Data
Controls
Keyboard Data Latches
0
1
2
3
4
5
6
7
0
X
7
1st Key Depression
2nd Key Depression
0-9 or A-F Keys
0-9 or A-F Keys
CPU
Keyboard Attachment Logic
Data and Sense Bytes (DBI)
Instructions (DBO)
Control Lines
Controls and Storage
I/O Attachment Interface
Alter Storage Operation
(not under program control)
1
CE Panel
1. CE mode selector to PROCESS.
a) Press SYSTEM RESET.
2. CE mode selector to ALTER SAR.
b) Set data/address switches to starting address.
c) Press START (once only).
3. CE mode selector to ALTER STORAGE (system clock is stopped at clock 9).
2
First Key Depression
Loads 1st hexadecimal character into encode board data latches and causes keyboard restore.
Note: In alter storage mode, only keys 0 through 9 and A through F are valid.
3
Second Key Depression
Loads 2nd hexadecimal character into encode board data latches, causes a keyboard restore and a CPU start.
4
CPU Start (result of second key depression)
Causes the CPU to run for one machine cycle, during which:
1. The byte in the keyboard data latches is transferred to the storage location specified by the CE Panel.
2. The keyboard data latches are reset.

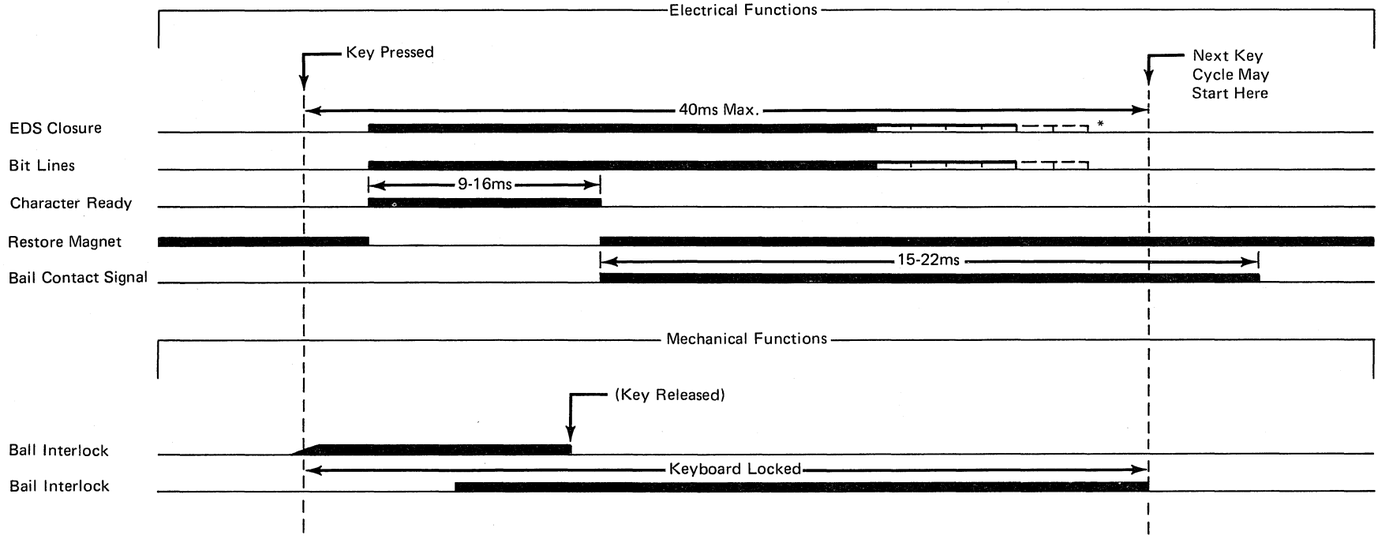


KEYBOARD ATTACHMENT—Introduction
Data Flow

KEYBOARD TIMING

The figure at the right shows the basic keyboard timing. The variable electrical and mechanical timings are shown in relation to the maximum time between key cycles. Their duration is determined as follows:

- Elastic Diaphragm Switch (EDS) Closure–Closes as soon as the interposer clears the latch spring. It remains closed until the restore is nearly complete. Time of restore is determined by the system and is, therefore, variable.
- Bit Lines–Coincident with the EDS closure.
- Character Ready–Brought up by the bit lines and reset by 'bail contact.' Restore is controlled by the system; thus the rise of 'bail contact' is variable.
- Restore Magnet–De-energized when the system accepts data and picked when the bail closes the bail contacts. Mechanical travel time of the bail determines the time the contacts close.
- Bail Contact Signal–Begins when the restore bail closes the contacts and is held up by a circuit delay after the contacts open. The duration is variable depending on the time the contacts are held closed by the restore bail.
- Ball Interlock–The duration is determined by the operator releasing the keylever.
- Bail Interlock–The duration is directly related to the mechanical travel of the bail.



Chapter 2. Functional Units

INTRODUCTION TO FUNCTIONAL UNITS

Chapter 2 contains the functional units of the keyboard attachment. The first page of the chapter is a board layout of the keyboard attachment. It is broken down into cards and contains the following information:

1. Card locations.
2. Circuits found on that card.
3. ALD page reference numbers that describe the circuits found on the card.
4. Card type number. The part number of the card will change each time that the card has an engineering change to it. The card type number however, will always stay the same.

The card location number appears on each page, or section of a page, that describes the circuitry on that card. For example, M2 on a page refers to the DBI assembler.

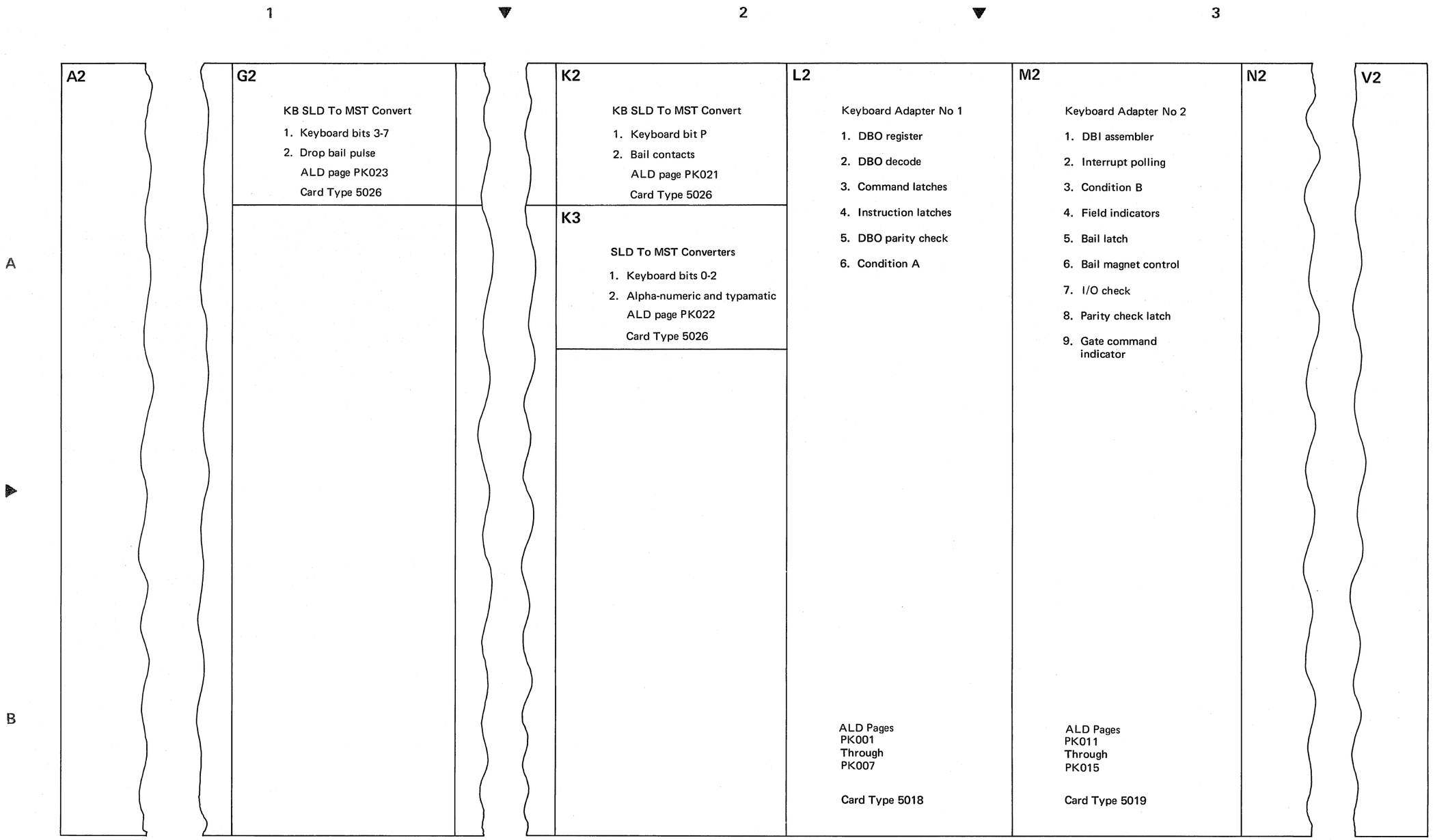
Symbols

There are two symbols that must be understood in order to read this chapter. They are:

1. 1 Numbers in squares.
2. A Letters in circles.

If only one of these symbols appears on a page, it will be numbers in squares. They are placed next to a functional unit, and correspond to the same number in a square on the facing page. Next to the symbol on the facing page, an explanation of that functional unit can be found.

If both numbers in squares and letters in circles are found on a page, the numbers refer to a reading order of the basic operation of a group of functional units. These numbers refer to corresponding numbers on the same or facing page, that when read consecutively explain the data flow between functional units. The letters in circles refer to operation of just the functional unit, the same as numbers in squares do when they are the only symbol on the page. This is the only application for letters in circles.



Keyboard Attachment Board B1* on Gate A (A-B1)

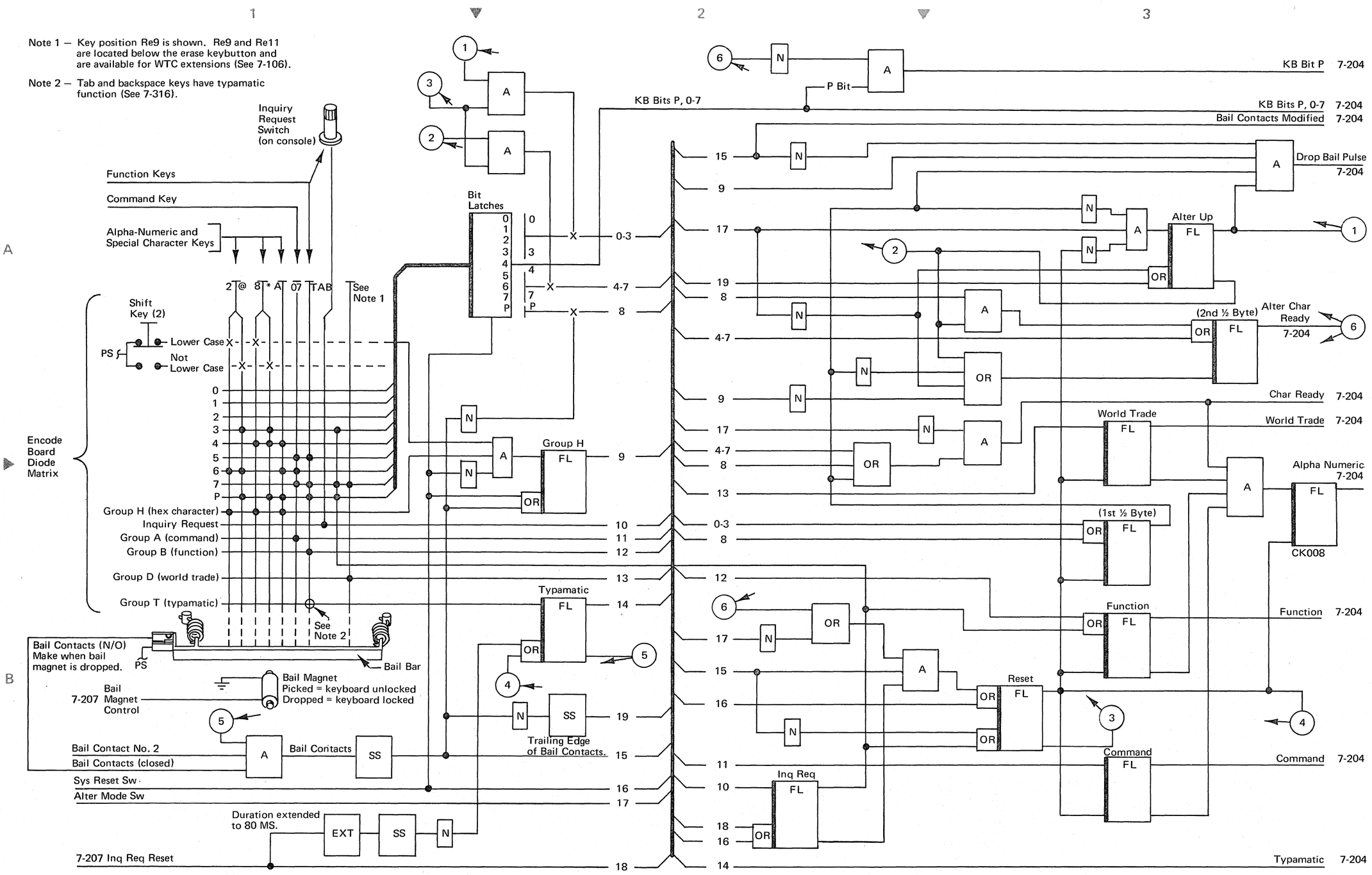
(card side)

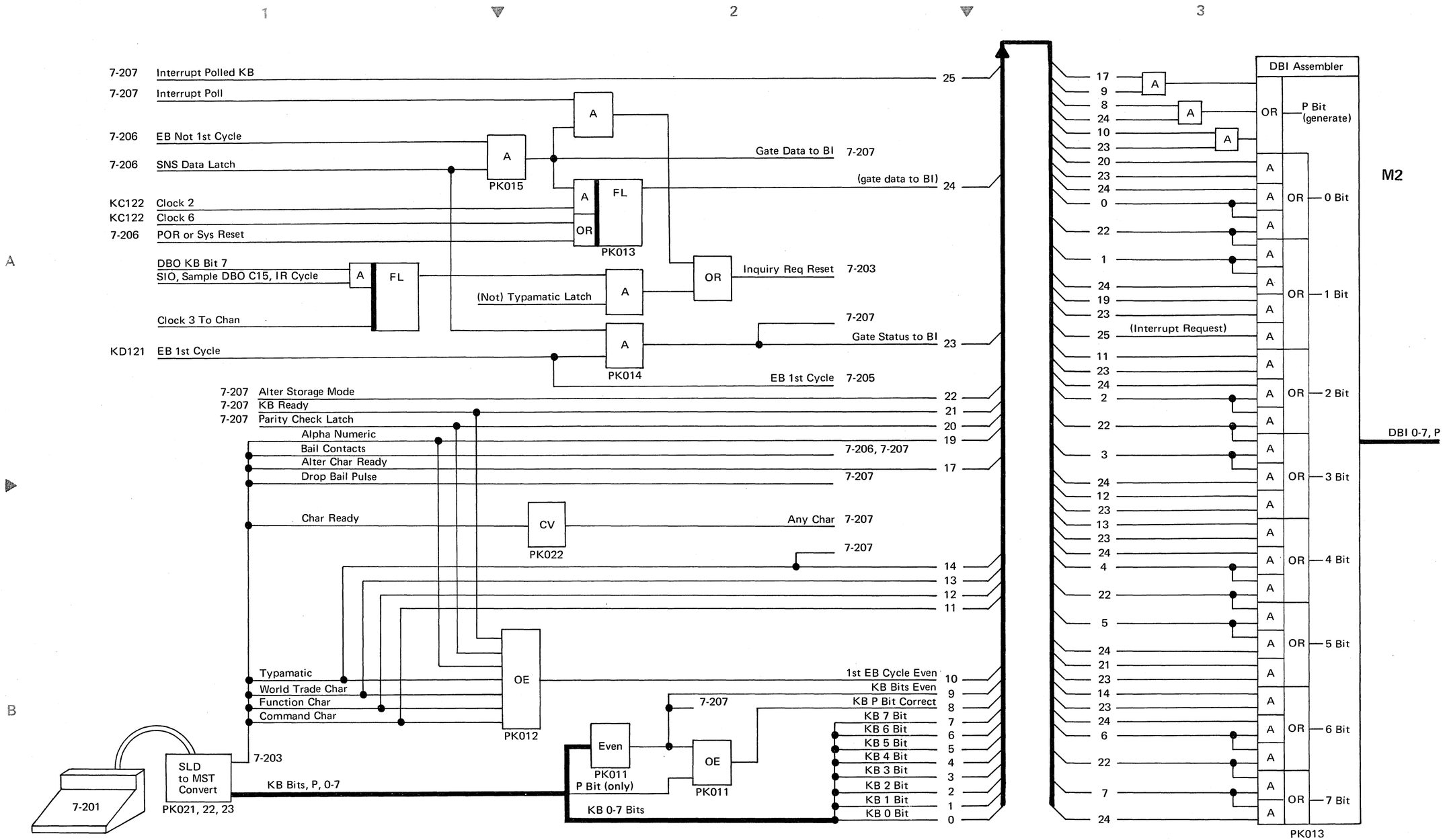
*Board B1 also contains:

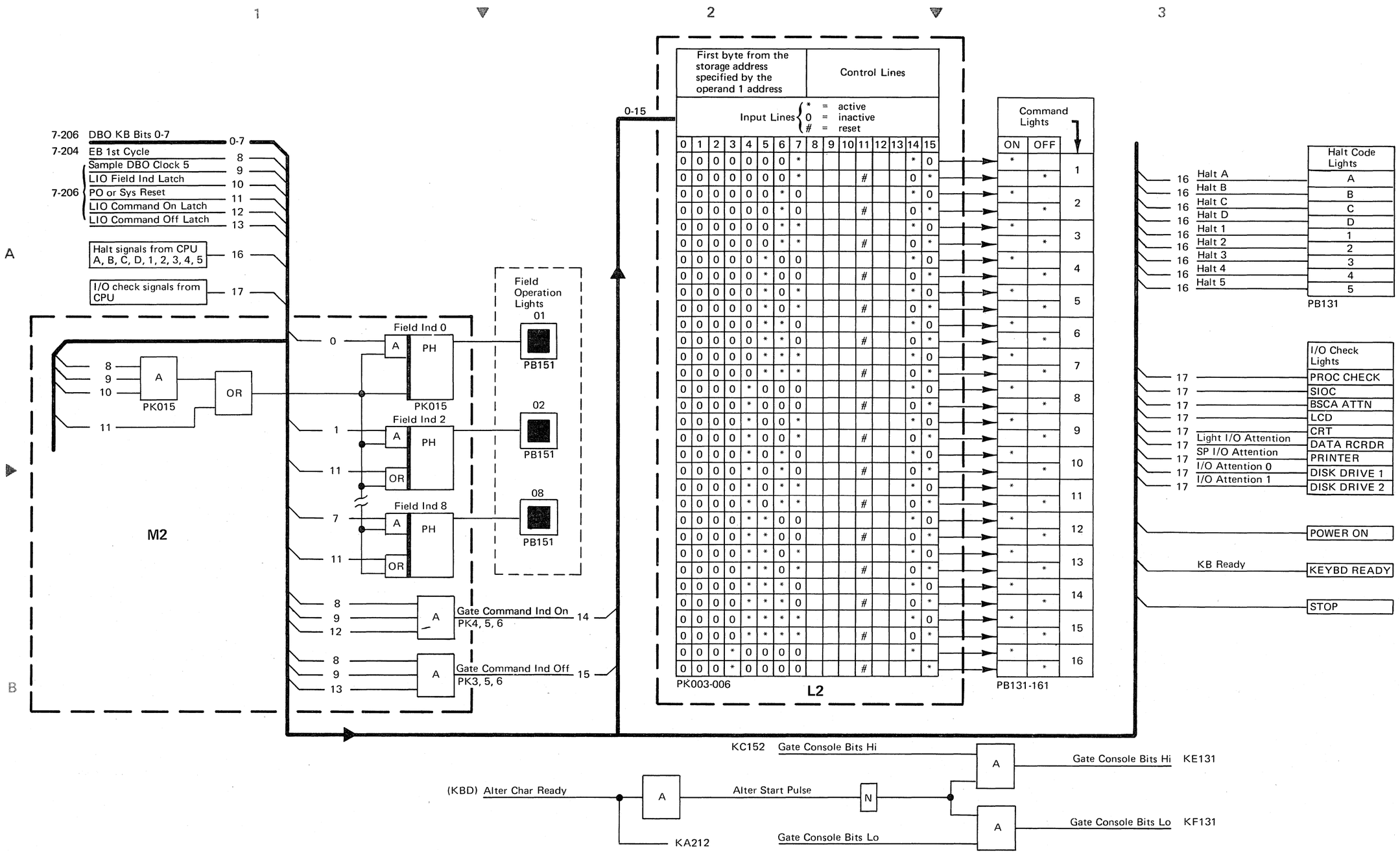
1. Channel banks.
2. Data recorder attachment.
3. CRT attachment.

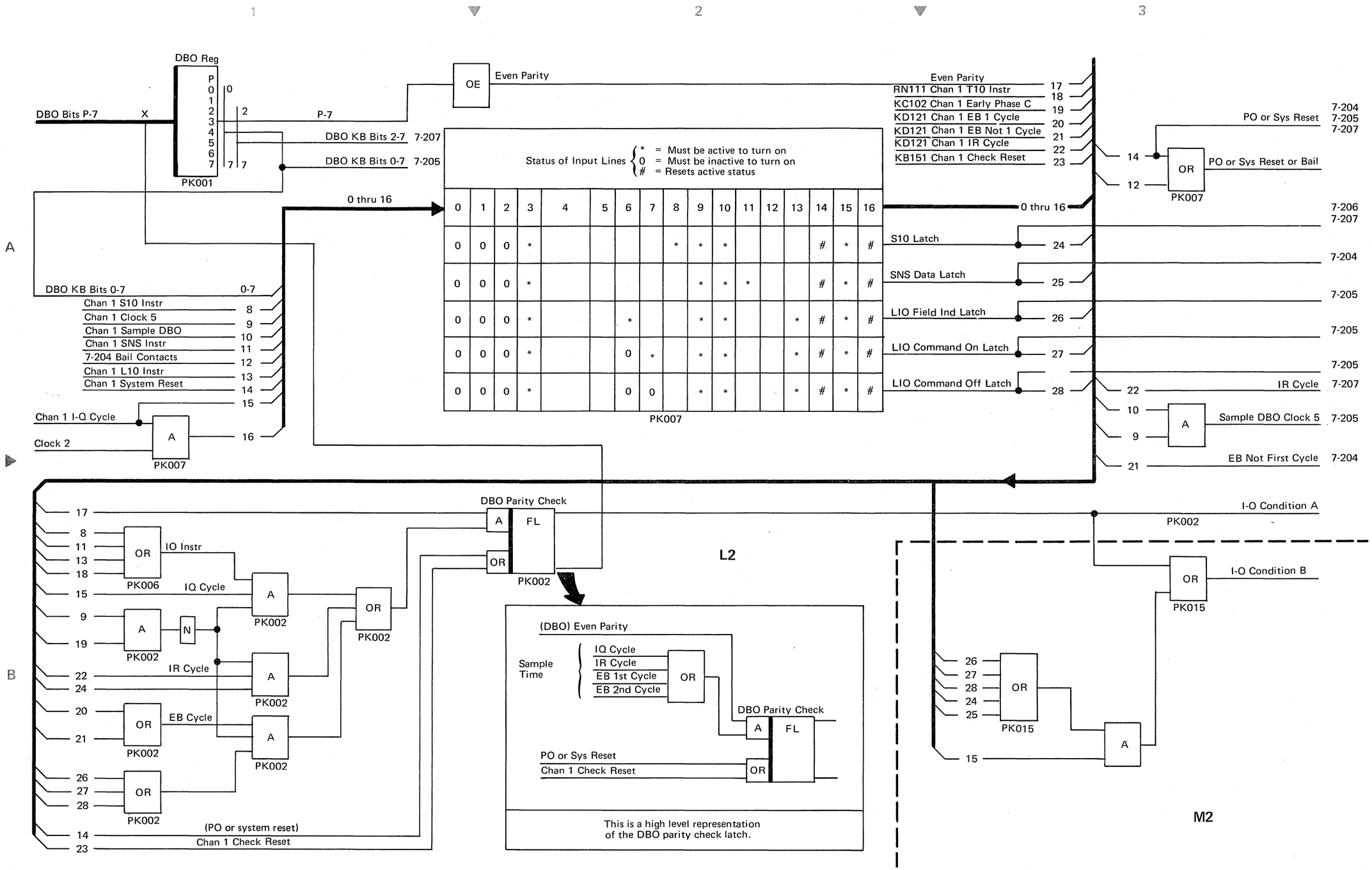
Note 1 — Key position Re9 is shown. Re9 and Re11 are located below the erase keybutton and are available for WTC extensions (See 7-106).

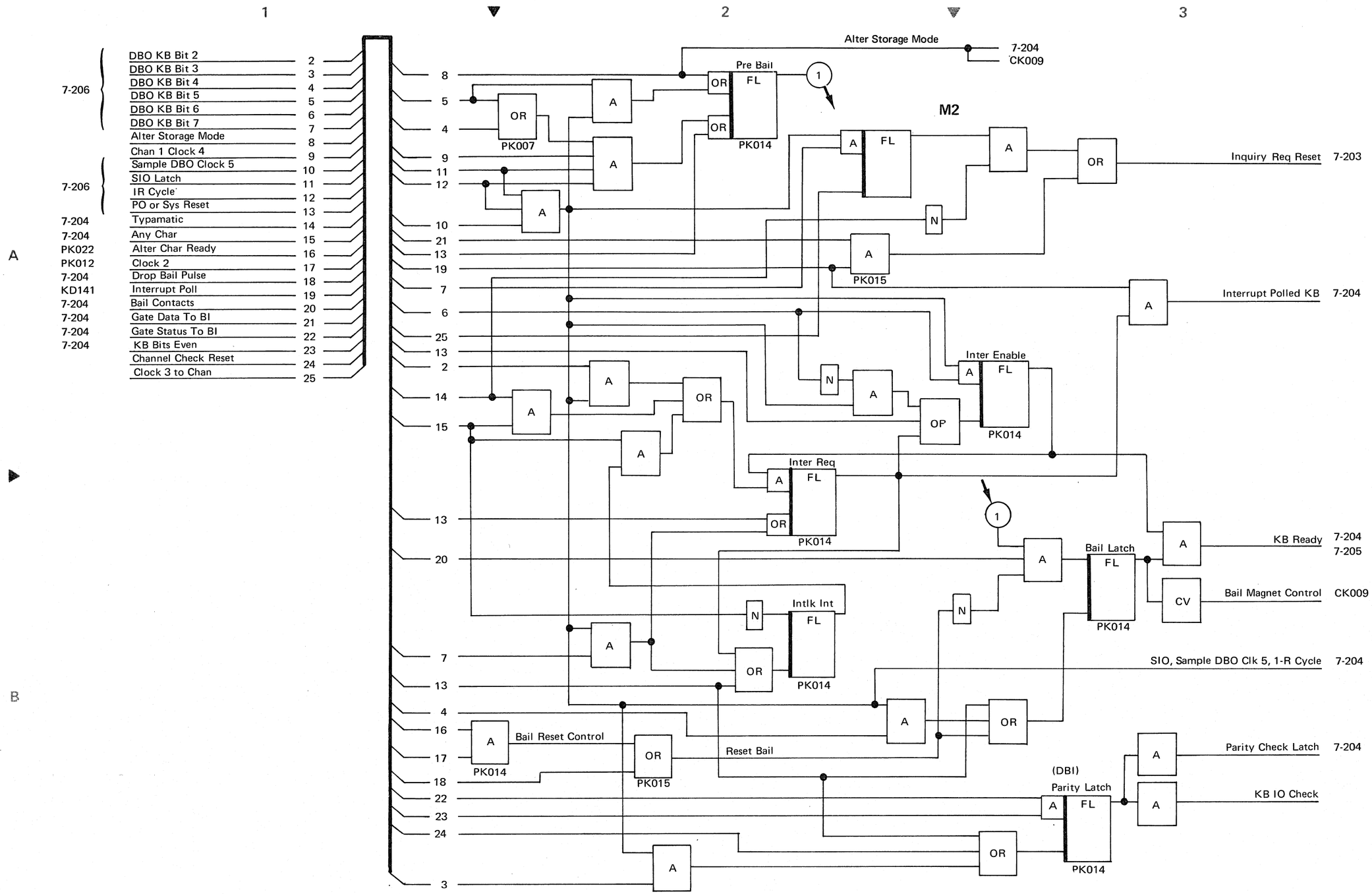
Note 2 — Tab and backspace keys have typamatic function (See 7-316).




1
2
3
A
B
7-207 Interrupt Polled KB
7-207 Interrupt Poll
7-206 EB Not 1st Cycle
7-206 SNS Data Latch
KC122 Clock 2
KC122 Clock 6
7-206 POR or Sys Reset
DBO KB Bit 7
SIO, Sample DBO C15, IR Cycle
Clock 3 To Chan
KD121 EB 1st Cycle
PK015
PK013
PK014
Gate Data to BI 7-207
(gate data to BI)
Inquiry Req Reset 7-203
(Not) Typamatic Latch
7-207 Gate Status to BI
EB 1st Cycle 7-205
7-207 Alter Storage Mode
7-207 KB Ready
7-207 Parity Check Latch
Alpha Numeric
Bail Contacts
Alter Char Ready
Drop Bail Pulse
7-206, 7-207
7-207
Char Ready
CV
PK022
Any Char 7-207
7-207
Typamatic
World Trade Char
Function Char
Command Char
OE
PK012
1st EB Cycle Even
KB Bits Even
KB P Bit Correct
KB 7 Bit
KB 6 Bit
KB 5 Bit
KB 4 Bit
KB 3 Bit
KB 2 Bit
KB 1 Bit
KB 0 Bit
7-207
Even
PK011
P Bit (only)
OE
PK011
KB 0-7 Bits
7-203
SLD
to MST
Convert
PK021, 22, 23
KB Bits, P, 0-7
7-201
25
24
23
22
21
20
19
17
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
M2
DBI Assembler
P Bit
(generate)
0 Bit
1 Bit
2 Bit
3 Bit
4 Bit
5 Bit
6 Bit
7 Bit
(Interrupt Request)
DBI 0-7, P
PK013


1
2
3
A
B
7-206 DBO KB Bits 0-7
7-204 EB 1st Cycle
Sample DBO Clock 5
LIO Field Ind Latch
7-206 PO or Sys Reset
LIO Command On Latch
LIO Command Off Latch
0-7
8
9
10
11
12
13
Halt signals from CPU A, B, C, D, 1, 2, 3, 4, 5
16
I/O check signals from CPU
17
M2
PK015
Field Ind 0
Field Ind 2
Field Ind 8
PH
Field Operation Lights
01
02
08
PB151
Gate Command Ind On
PK4, 5, 6
14
Gate Command Ind Off
PK3, 5, 6
15
0-15
First byte from the storage address specified by the operand 1 address
Control Lines
Input Lines
* = active
0 = inactive
# = reset
PK003-006
L2
Command Lights
ON
OFF
PB131-161
Halt Code Lights
Halt A
Halt B
Halt C
Halt D
Halt 1
Halt 2
Halt 3
Halt 4
Halt 5
A
B
C
D
1
2
3
4
5
PB131
I/O Check Lights
PROC CHECK
SIOC
BSCA ATTN
LCD
CRT
DATA RCRDR
PRINTER
DISK DRIVE 1
DISK DRIVE 2
Light I/O Attention
SP I/O Attention
I/O Attention 0
I/O Attention 1
POWER ON
KB Ready
KEYBD READY
STOP
KC152 Gate Console Bits Hi
Gate Console Bits Hi KE131
(KBD) Alter Char Ready
Alter Start Pulse
Gate Console Bits Lo KF131
KA212
Gate Console Bits Lo


1
2
3
A
B
DBO Reg
P
0
1
2
3
4
5
6
7
PK001
DBO Bits P-7
X
P-7
OE
Even Parity
DBO KB Bits 2-7 7-207
DBO KB Bits 0-7 7-205
Status of Input Lines
* = Must be active to turn on
0 = Must be inactive to turn on
# = Resets active status
0 thru 16
PK007
Even Parity
RN111 Chan 1 T10 Instr
KC102 Chan 1 Early Phase C
KD121 Chan 1 EB 1 Cycle
KD121 Chan 1 EB Not 1 Cycle
KD121 Chan 1 IR Cycle
KB151 Chan 1 Check Reset
S10 Latch
SNS Data Latch
LIO Field Ind Latch
LIO Command On Latch
LIO Command Off Latch
PO or Sys Reset
PO or Sys Reset or Bail
OR
PK007
IR Cycle
Sample DBO Clock 5
EB Not First Cycle
A
DBO KB Bits 0-7
Chan 1 S10 Instr
Chan 1 Clock 5
Chan 1 Sample DBO
Chan 1 SNS Instr
7-204 Bail Contacts
Chan 1 L10 Instr
Chan 1 System Reset
Chan 1 I-Q Cycle
Clock 2
DBO Parity Check
FL
I-O Condition A
PK002
I-O Condition B
PK015
IO Instr
IQ Cycle
IR Cycle
EB Cycle
N
PK006
(PO or system reset)
Chan 1 Check Reset
L2
(DBO) Even Parity
Sample Time
IQ Cycle
IR Cycle
EB 1st Cycle
EB 2nd Cycle
This is a high level representation of the DBO parity check latch.
M2


1
2
3
A
B
7-206
DBO KB Bit 2
DBO KB Bit 3
DBO KB Bit 4
DBO KB Bit 5
DBO KB Bit 6
DBO KB Bit 7
Alter Storage Mode
Chan 1 Clock 4
7-206
Sample DBO Clock 5
SIO Latch
IR Cycle
PO or Sys Reset
7-204 Typamatic
7-204 Any Char
PK022 Alter Char Ready
PK012 Clock 2
7-204 Drop Bail Pulse
KD141 Interrupt Poll
7-204 Bail Contacts
7-204 Gate Data To BI
7-204 Gate Status To BI
7-204 KB Bits Even
Channel Check Reset
Clock 3 to Chan
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
8 5 4 9 11 12 10 21 13 19 7 6 25 13 2 14 15 13 20 7 13 4 16 17 18 22 23 24 3
Alter Storage Mode
7-204 CK009
Pre Bail
FL
PK014
OR
PK007
M2
Inquiry Req Reset 7-203
PK015
Interrupt Polled KB 7-204
Inter Enable
Inter Req
Intlk Int
Bail Latch
KB Ready 7-204 7-205
Bail Magnet Control CK009
SIO, Sample DBO Clk 5, 1-R Cycle 7-204
Bail Reset Control
Reset Bail
(DBI) Parity Latch
Parity Check Latch 7-204
KB IO Check

Chapter 3. Operations

INTRODUCTION TO OPERATIONS

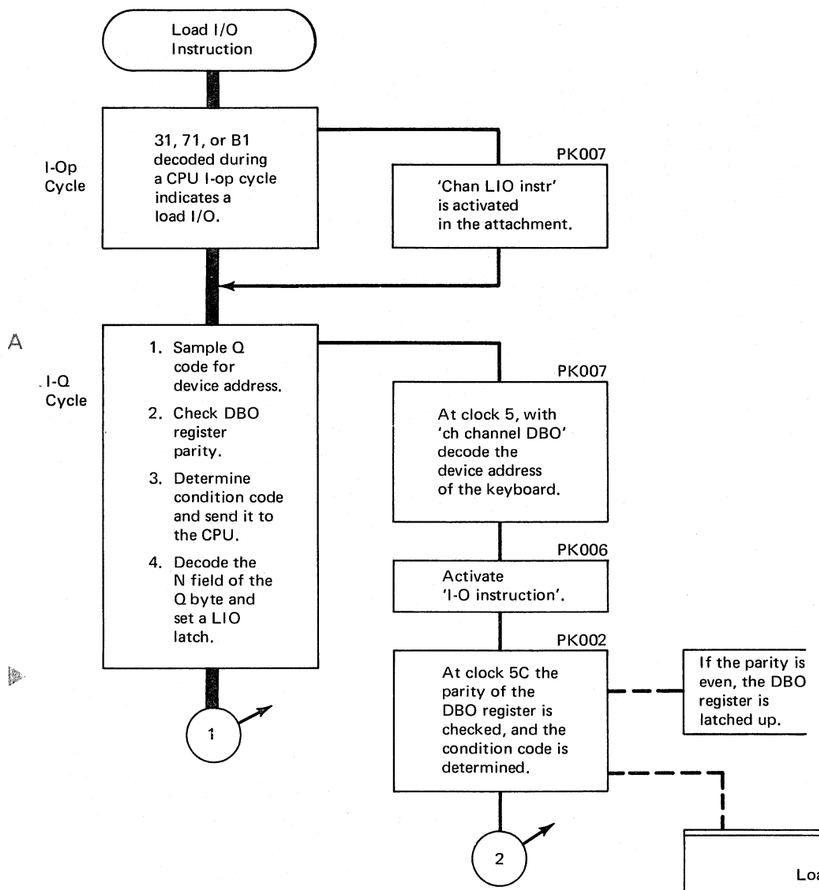
Chapter 3 contains the detailed flowcharts and timing charts of the operations performed by the keyboard attachment.

Flowcharts

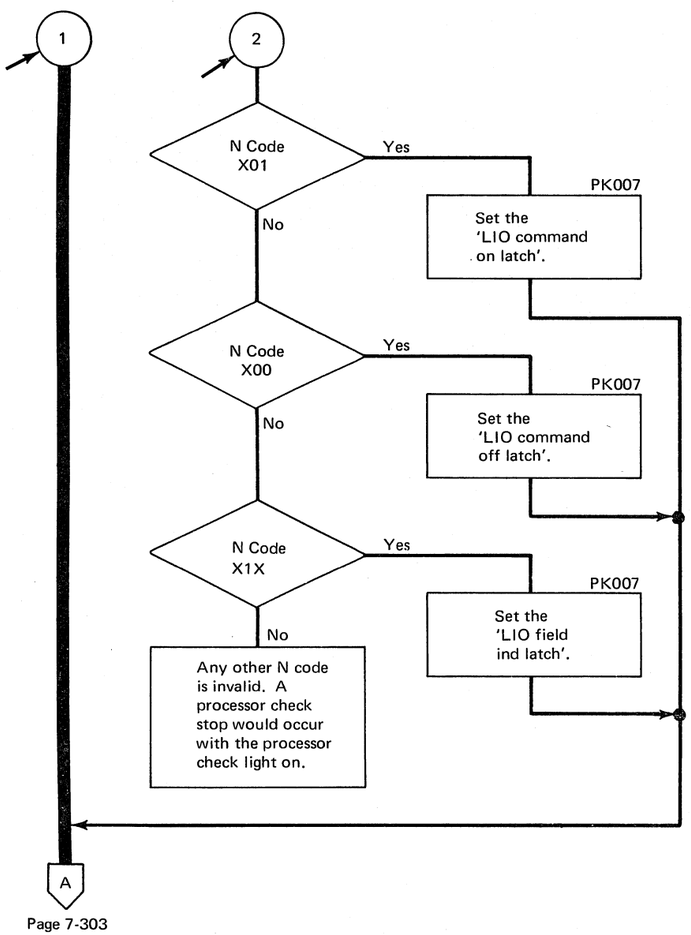
The flowcharts contain three levels of information. By reading down the heavy dark lines, the reader can learn the major objectives of the operation. The second level of information is obtained by reading the information in the boxes that branch off the heavy dark line. The information that is contained in each block in a heavy dark line is explained in the blocks that branch off from it. The third level of information is contained in the note blocks (open ended blocks) that branch off the second level blocks. Information in these blocks is intended to explain why an action has been performed.

Timing Charts

The timing charts in this chapter are to be used to supplement the information found in the flowcharts.

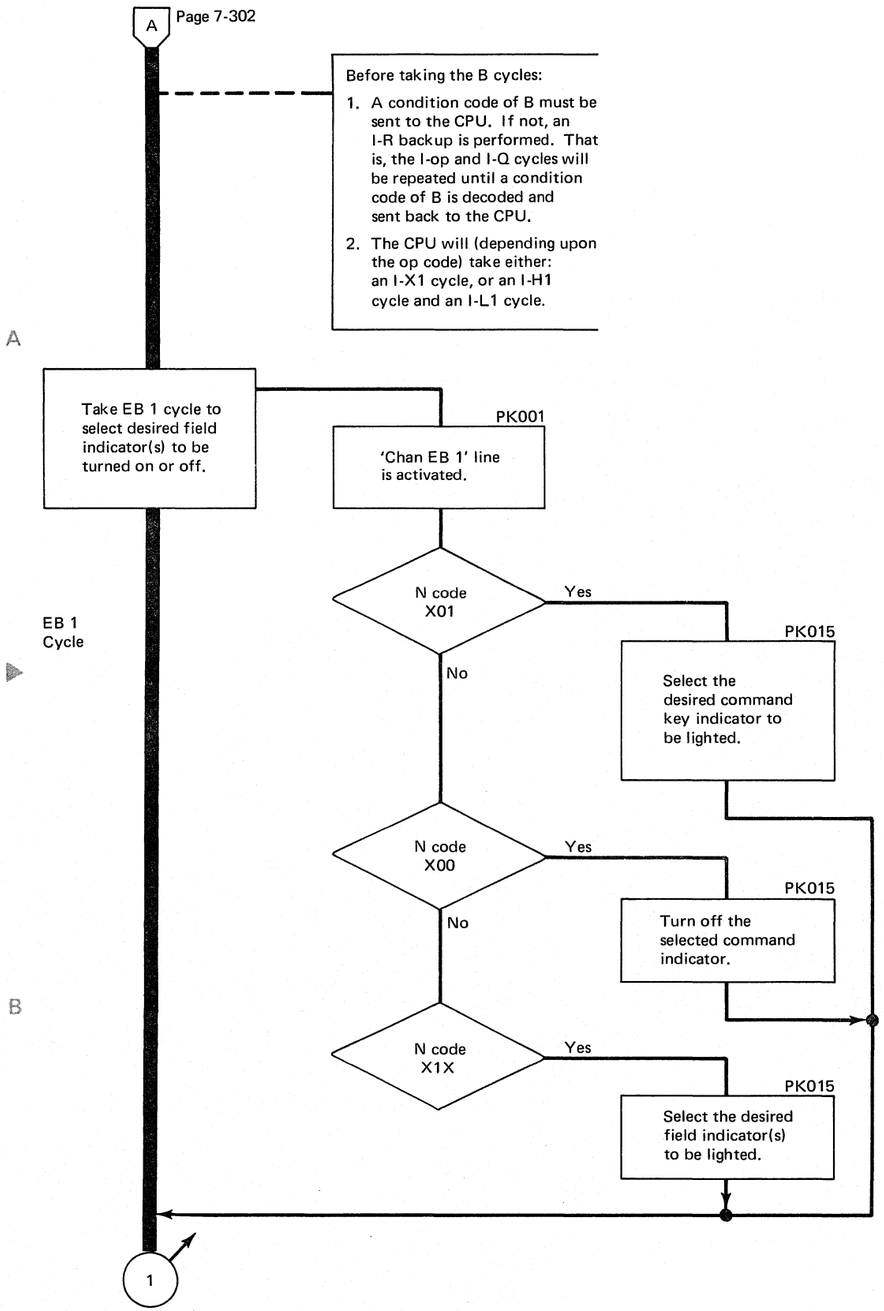


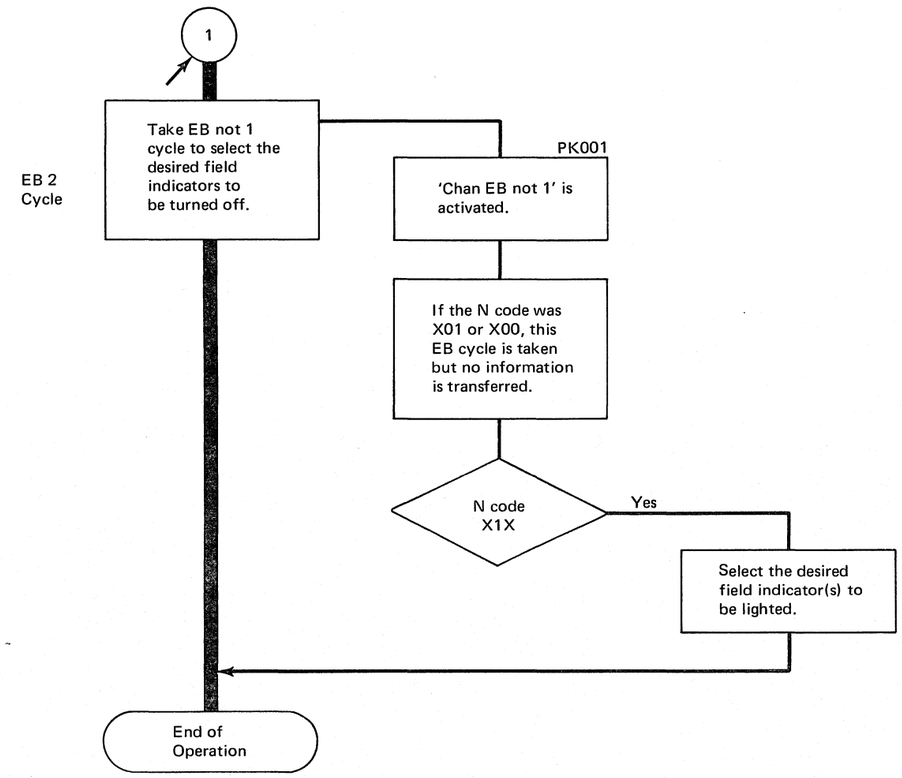
Load I/O I-Q Byte Condition				I/O Condition A	I/O Condition B
Incorrect DBO Parity				1	1
Correct DBO Parity	Device address not recognized or N field invalid.			0	0
	Device address recognized and N field valid.	Load I/O	Rejected	1	0
			Accepted	0	1
Load I/O , E-B Cycles		Incorrect DBO Parity		1	1
		Correct DBO Parity		0	0



Page 7-303

X = bit not checked.





X = Bit not checked.

KEYBOARD ATTACHMENT–Operations
Load I/O Instruction Flowchart (Part 2 of 2)

LOAD I/O INSTRUCTION TIMING CHART

Load I/O Operation

- The CPU decodes the op code of the instruction and activates the control line 'chan LIO instr' in the attachment.
- The attachment takes an I-Q cycle to:
  1. Decode the Q byte for the device address.
  2. Determine the condition code and send it back to the CPU.
  3. Decode the N code of the Q byte to set a load I/O latch in the attachment.
- Take EB cycles to:
  1. Turn on a command indicator.
  2. Turn off a command indicator.
  3. Turn on field indicator(s).

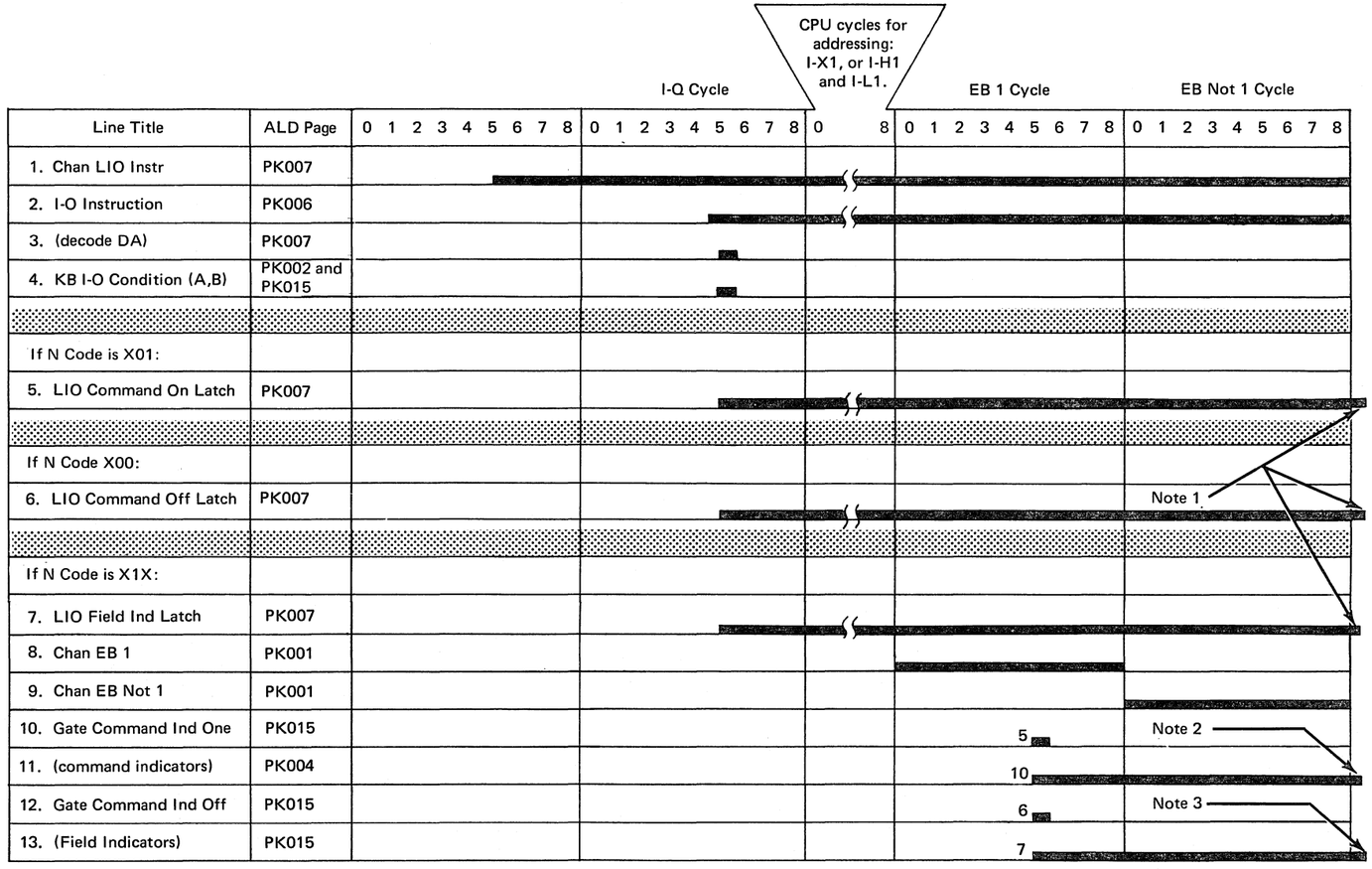
EB Cycles

The CPU gates the first byte from the main storage location specified by the operand one address through the DBO register to turn on or off the desired command indicator or field indicator(s) latches. The output of the latches control the on or off status of the lights.

If a load I/O instruction is issued to turn on or off command lights with codes other than those shown in "Weighted Codes," the instruction is accepted, but no command lights are turned on or off.

A load I/O instruction issued to turn on field indicator(s) resets the non-selected field indicator latches. All bit combinations are valid for turning on the individual field indicators (all eight indicators can be turned on with one load I/O instruction). When all bits are zero, all of the field indicators are turned off.

The second byte transferred from the main storage location specified by the operand one address minus one is also gated to the DBO register, but it is not used.



Note 1. Reset at clock 2 of the next I-Q cycle.

Note 2. Will be reset by next 'gate command ind off' pulse.

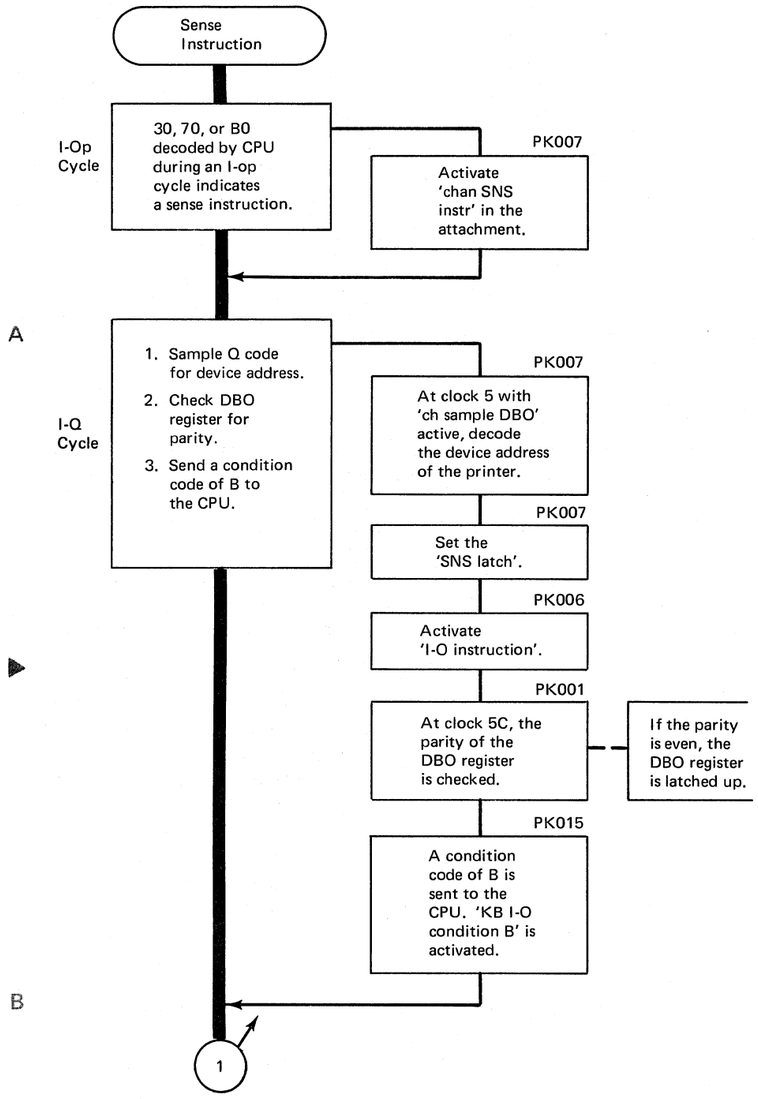
Note 3. Will be reset by the next 'LIO field ind latch' pulse.

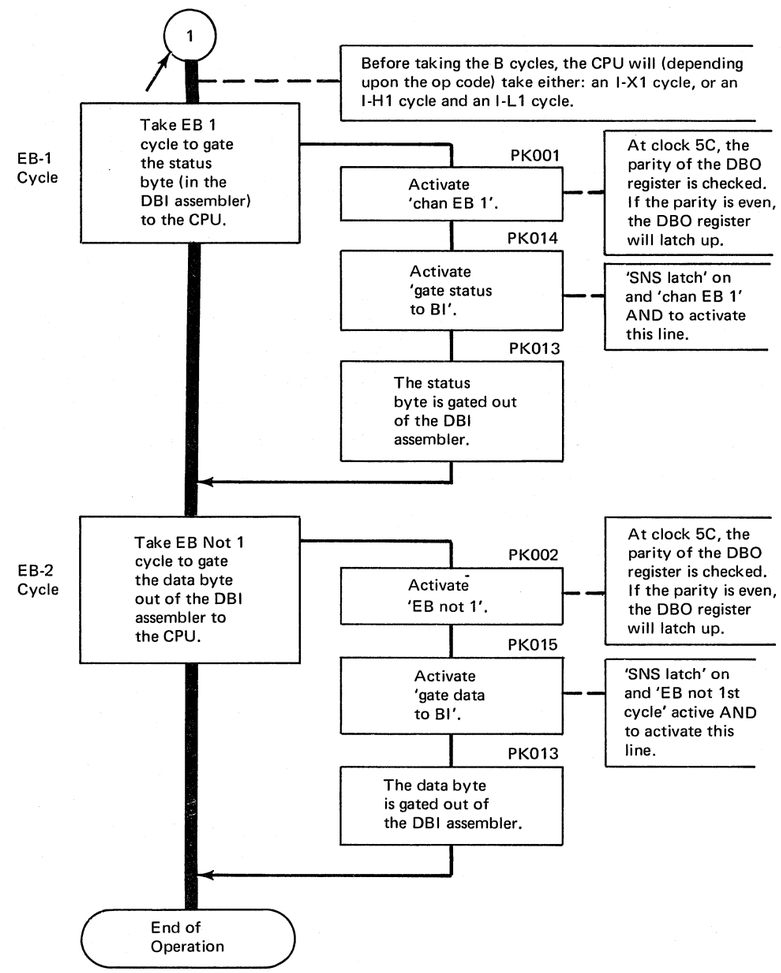
BR0688

1 2 3

A

B


Sense Instruction
I-Op Cycle
30, 70, or B0 decoded by CPU during an I-op cycle indicates a sense instruction.
PK007
Activate 'chan SNS instr' in the attachment.
I-Q Cycle
1. Sample Q code for device address.
2. Check DBO register for parity.
3. Send a condition code of B to the CPU.
PK007
At clock 5 with 'ch sample DBO' active, decode the device address of the printer.
PK007
Set the 'SNS latch'.
PK006
Activate 'I-O instruction'.
PK001
At clock 5C, the parity of the DBO register is checked.
If the parity is even, the DBO register is latched up.
PK015
A condition code of B is sent to the CPU. 'KB I-O condition B' is activated.
1


1
Before taking the B cycles, the CPU will (depending upon the op code) take either: an I-X1 cycle, or an I-H1 cycle and an I-L1 cycle.
EB-1 Cycle
Take EB 1 cycle to gate the status byte (in the DBI assembler) to the CPU.
PK001
Activate 'chan EB 1'.
At clock 5C, the parity of the DBO register is checked. If the parity is even, the DBO register will latch up.
PK014
Activate 'gate status to BI'.
'SNS latch' on and 'chan EB 1' AND to activate this line.
PK013
The status byte is gated out of the DBI assembler.
EB-2 Cycle
Take EB Not 1 cycle to gate the data byte out of the DBI assembler to the CPU.
PK002
Activate 'EB not 1'.
At clock 5C, the parity of the DBO register is checked. If the parity is even, the DBO register will latch up.
PK015
Activate 'gate data to BI'.
'SNS latch' on and 'EB not 1st cycle' active AND to activate this line.
PK013
The data byte is gated out of the DBI assembler.
End of Operation

SENSE I/O INSTRUCTION TIMING CHART

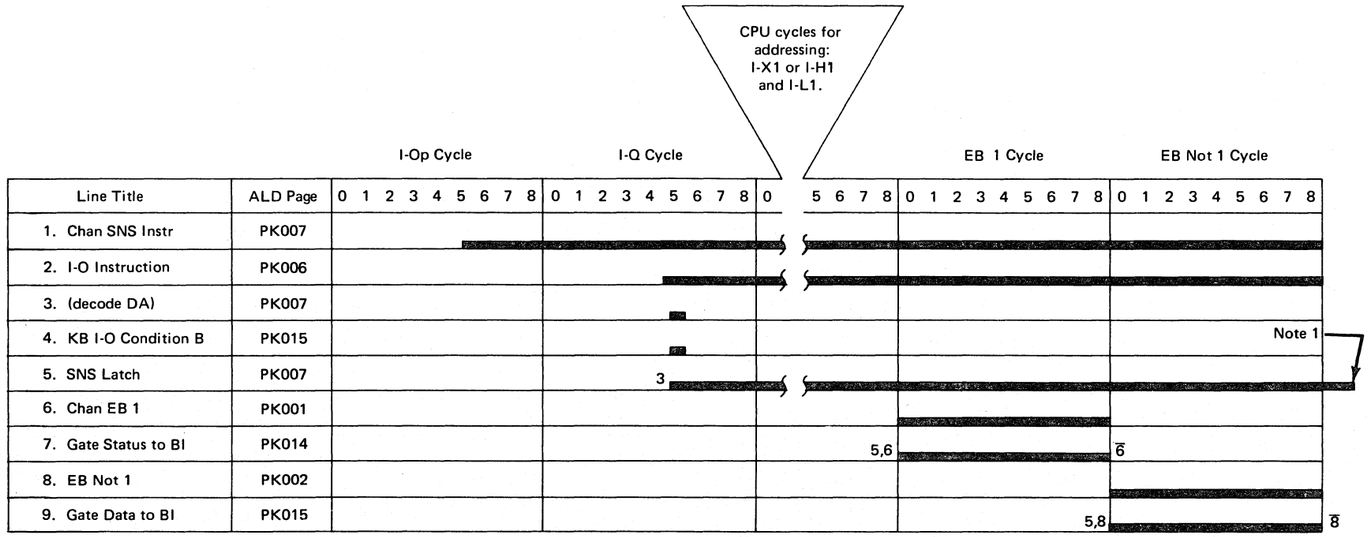
Sense Operation

- The CPU decodes the op code of the instruction and activates the control line 'chan SNS instr'.
- The attachment takes an I-Q cycle to:
  1. Decode the Q byte for the device address.
  2. Send a condition code of B back to the CPU.
  3. Set the 'SNS latch'.
- The attachment takes an EB 1 cycle to gate the status byte out of the DBI assembler to send it to the CPU.
- The attachment takes an EB not 1 cycle to gate the data byte out of the DBI assembler to send it to the CPU.

EB Cycles

Prior to the EB cycles, the data and status bytes (generated by a previously pressed key) are stored in the encode board. The status byte is the first byte to be gated to the CPU. This byte identifies the type of key that was pressed. The CPU stores this byte in the field specified by the operand portion of the sense instruction. The bit significance of this byte makes the program aware of the type of data that is contained in the data byte.

The data byte is gated to the CPU during the EB not 1 cycle. This byte is stored at the operand address minus one (as indicated by the operand portion of the sense instruction). The program in the CPU uses this data byte as a displacement, and adds it to a base address. The resulting address points to the core location that contains the EBCDIC code for that key.



Note 1. Reset at clock 2 of the next I-Q cycle.

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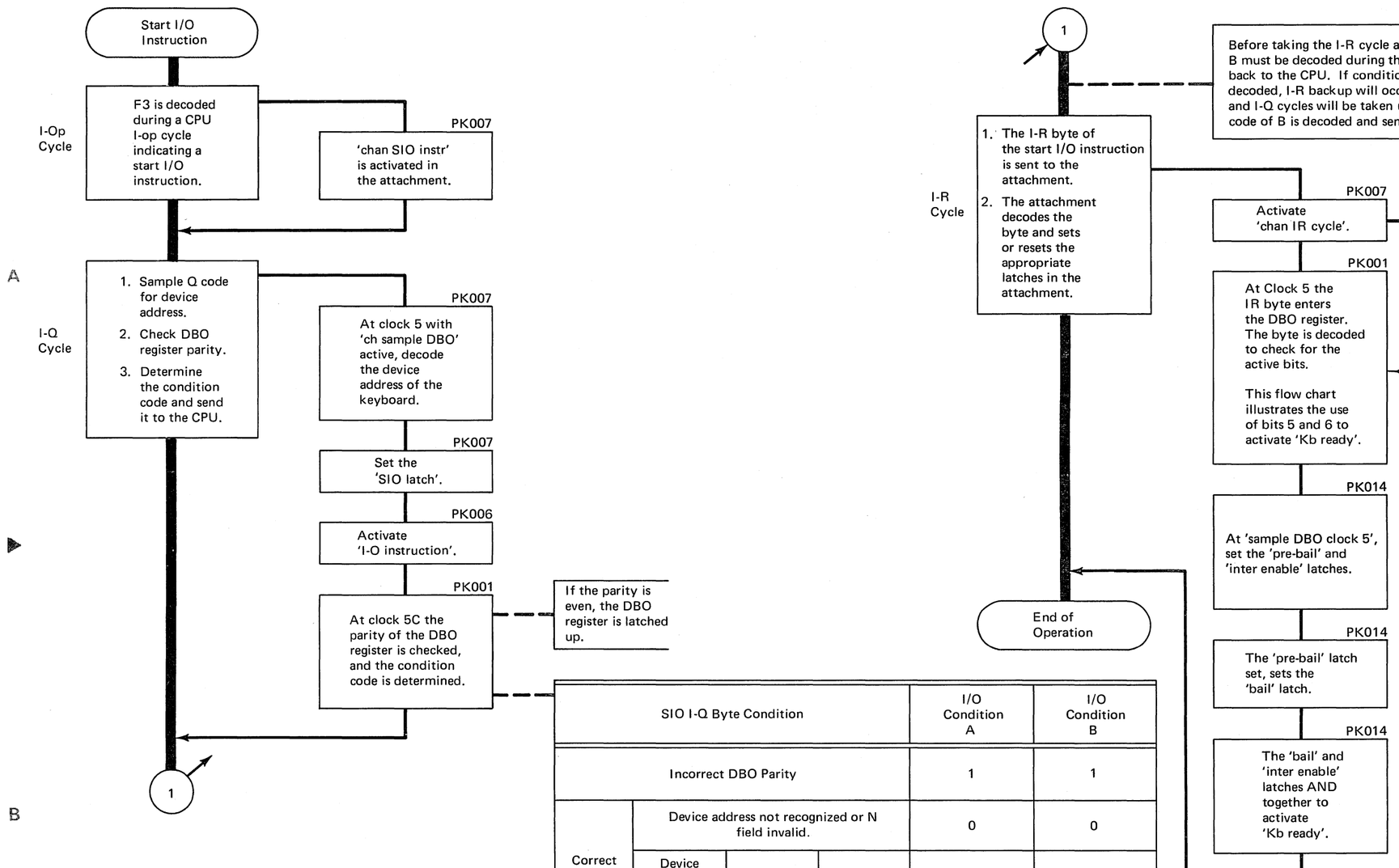
1 2 3



SIO I-Q Byte Condition				I/O Condition A	I/O Condition B
Incorrect DBO Parity				1	1
Correct DBO Parity	Device address not recognized or N field invalid.			0	0
	Device address recognized and N field valid	Start I/O	Rejected	1	0
			Accepted	0	1
Start I/O I-R Byte, and I-O Cycle Condition		Incorrect DBO Parity		1	1
		Correct DBO Parity		0	0

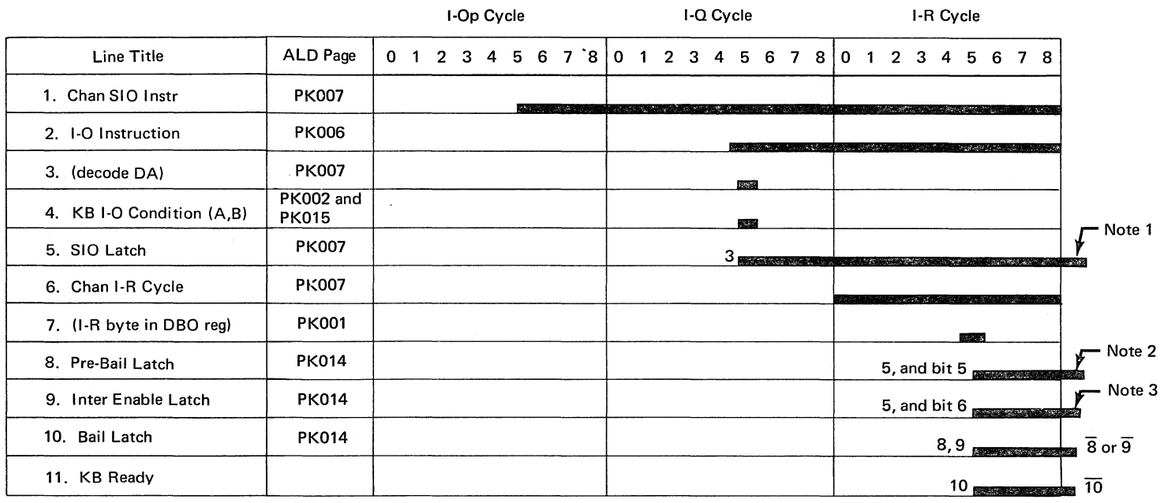
START I/O INSTRUCTION TIMING CHART

Start I/O Operation

- The CPU decodes the op code of the instruction and activates the control line 'chan SIO instr'.
- The attachment takes an I-Q cycle to:
  1. Decode the Q byte for the device address.
  2. Determine the condition code and send it back to the CPU.
  3. Set the 'SIO latch'.
- The attachment takes an I-R cycle to decode the I-R byte.
- The bits in the I-R byte set or reset latches in the attachment in preparation for a keyboard operation.

I-R Byte

The bits present in the I-R byte are determined by the main program in the CPU. Bits 4 and 5 must both be present to restore the keyboard. All bit combinations of the I-R byte are valid. All functions associated with each bit are performed except for the following, if bits 2 and 7 are both present, interrupt request is not set.



Note 1. Reset at clock 2 of next I-Q cycle.

Note 2. Reset at clock 4 of next I-R cycle if DBO bits 4 or 5 are present.

Note 3. Reset at sample DBO clock 5 of next I-R cycle if 'DB Kb bit 6 ckt 2' is inactive.

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KEY OPERATION–PROGRAMMED

- A start I/O instruction is given to enable interrupts.
- Interrupt request is generated by pressing any key (except the shift key).
- A sense instruction from the CPU gates two encoded bytes from the DBI assembler in the attachment to the CPU. These two bytes represent the key position (the key that was pressed).
- A second start I/O instruction is issued to restore the keyboard.

Before the keys on the keyboard can be operative, a start I/O instruction must be issued to enable interrupts, restore the keyboard, and unlock the keys.

When a key is pressed, its EDS latch spring is released and the elastic diaphragm is pressed through a hole in the separator by the actuator spring projection. The diaphragm common conductor contacts the normally open contact on the substrate, which completes the circuit to the encode circuit board.

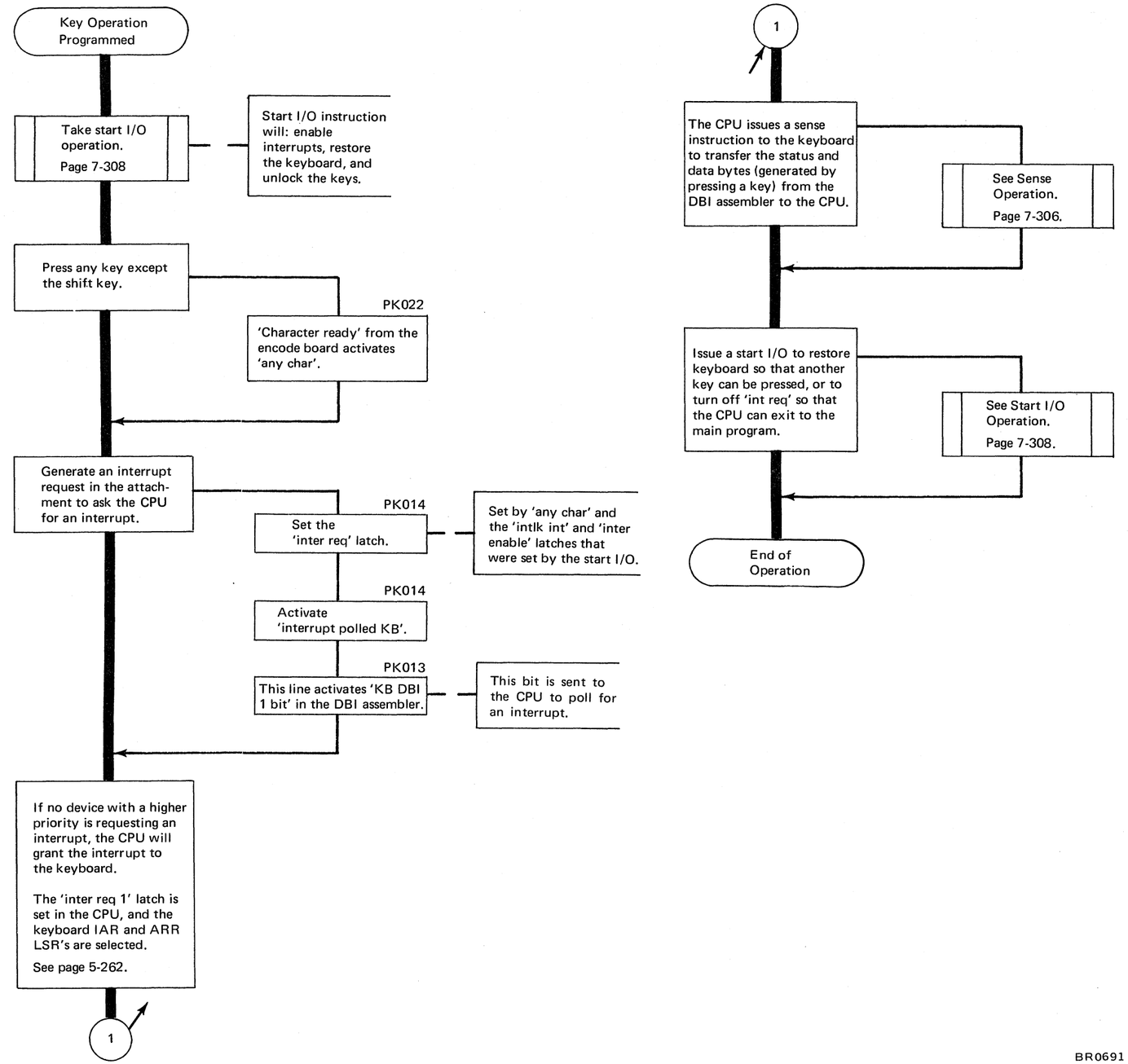
Pressing a key generates 'character ready' in the encode board which is sent to the attachment circuitry. 'Char ready' (and all other lines from the encode board) is converted from an SLD logic level to an MST logic level in the attachment. After the logic conversion, the line is called 'any char'.

The diode logic circuits of the encode board, decodes the output of the key that was pressed (EDS switch) into two bytes of information. The data byte is stored in the encode board bit latches, and the function latches that represent the bits to make up the status byte are also located in the encode board.

An interrupt request is generated by raising the 'interrupt polled KB' line. This line is activated by channel interrupt poll ANDed with the interrupt request latch which is set on by the 'any char' line and the 'intlk int' and 'inter enable' latches that were set earlier by the start I/O instruction. 'Interrupt polled KB' is sent to the DBI assembler to gate 'KB DBI 1 bit' to the CPU to request an interrupt.

When the interrupt is granted by the CPU (interrupt level 1 for the keyboard), the CPU branches to the keyboard interrupt routine. A sense instruction is issued to the attachment to transfer the two bytes from the bit latches through the DBI assembler onto DBI.

The interrupt routine can now issue a second start I/O instruction with bits 4 and 5 active in the I-R byte of the control code to restore the keyboard in order that another key can be pressed. Depending on the main program in process, the start I/O instruction can turn off the 'int req' latch with bit 7 active in the control code. This turn off interrupt request instruction causes the CPU to exit from the keyboard interrupt routine and return to the main program.



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KEYBOARD INTERRUPT REQUEST

- A start I/O instruction is issued to the keyboard attachment to: unlock the keyboard, restore the keys, and enable interrupts.
- Pressing a key on the keyboard, or the inquiry request key on the console, turns on the 'inter req' (interrupt request) latch in the attachment.
- With 'interrupt poll' active in the attachment at clock 5-7 time and the 'int req' latch on in the attachment, the 'interrupt polled KB' line in the attachment gates 'KB DBI 1 bit' out of the DBI assembler to request an interrupt.
- If no interrupts with a higher priority are pending and the program in progress is at the end of an instruction, the main program is interrupted by a branch to the keyboard interrupt routine.
- The keyboard interrupt routine issues a sense instruction to the keyboard attachment and allows the two bytes (generated as the result of pressing a key) onto DBI.
- After sensing the two bytes of information generated by pressing the key, the keyboard is restored (enabled) when the keyboard interrupt routine issues a start I/O instruction. The keyboard keys can now be operated again.

The keyboard interrupt level has a separate IAR and ARR in the CPU local storage registers so that the IAR and ARR for the main program are not disturbed. Local storage register 15 contains the interrupt level 1 instruction address register (IAR-1), and local storage register 16 contains the interrupt level 1 address recall register (ARR-1) for the keyboard.

The interrupt routine performed is established by the interrupt priority latches. As in the case of cycle steal, the highest interrupt level device takes precedence over lower level devices. The keyboard is assigned interrupt level 1 which is the lowest level in priority. Therefore, it is possible for any other interrupt routine to interrupt the keyboard. However, each device maintains its interrupt request until it is satisfied. The lower level priority device finishes its routine upon completion of the higher level routine.

The stored program controls the ability of the keyboard to interrupt by enabling and disabling the keyboard through the use of start I/O instructions. Once an interrupt has occurred, it is also ended by a start I/O instruction.

During the I-Q cycle, keyboard selection occurs in the same manner as any start I/O instruction. At clock 5 of the I-R cycle, the control code (I-R byte) is sent to the attachment on DBO. The control code is decoded by the attachment to turn on the 'inter enable' latch. This latch remains on until another start I/O instruction is sent to the attachment to reset (disable) the latch.

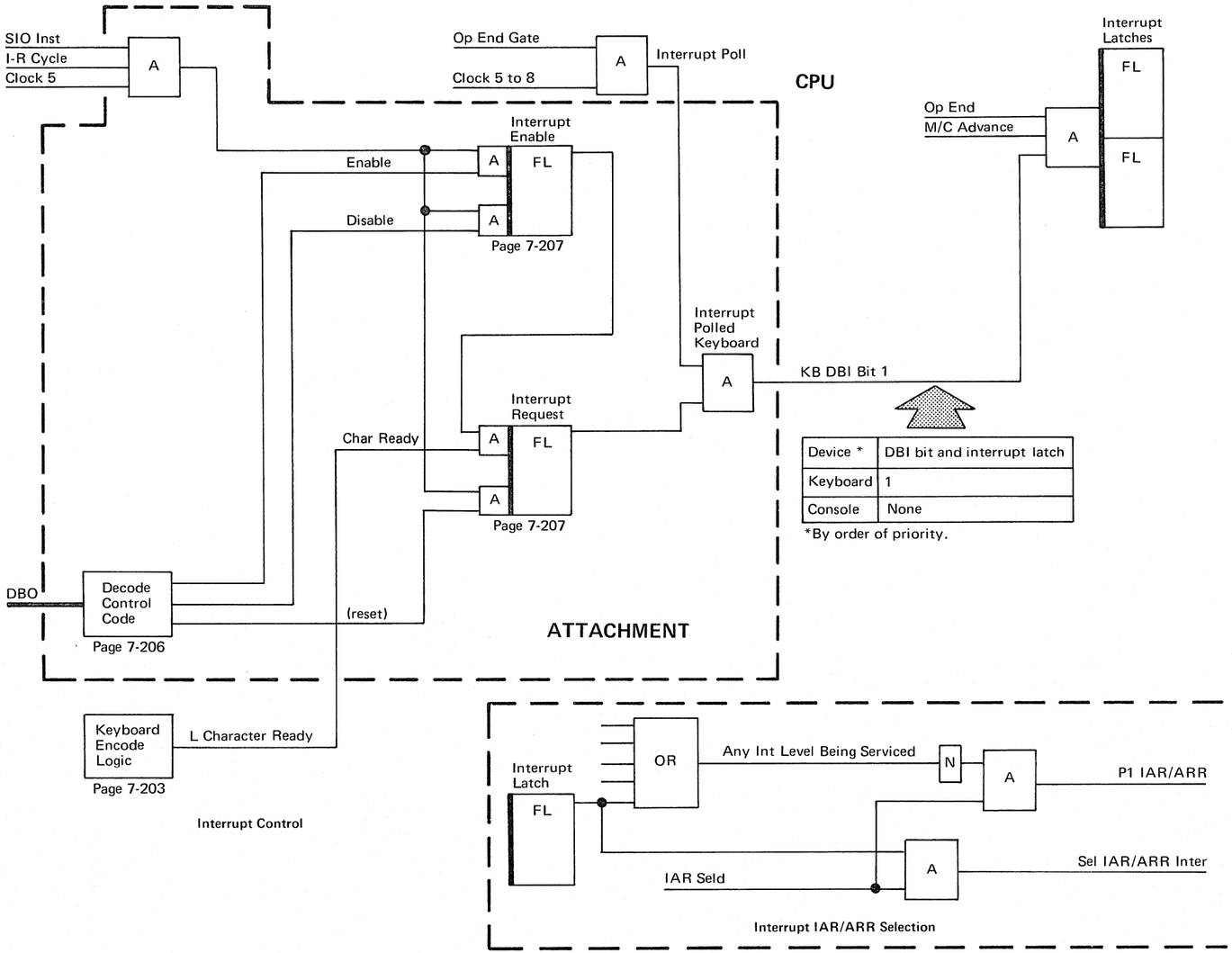
When a key is pressed on the keyboard, the 'inter req' latch is turned on. At the end of the operation being performed in the CPU, 'interrupt poll' is sent to the keyboard attachment. This activates 'interrupt polled KB' in the attachment. This line gates 'KB DBI 1 bit' out of the DBI assembler to turn on the interrupt latch for the keyboard in the CPU. If more than one device is requesting an interrupt, only the highest level priority latch is turned on.

With any interrupt latch on, the selection of the normal IAR/ARR (P1 or P2) is blocked and the IAR/ARR for the active interrupt level latch is selected. The interrupt request latch in the attachment stays on until it is reset by a start I/O instruction.

Upon recognizing the keyboard interrupt, the CPU issues a sense instruction to the keyboard attachment. The instruction decodes the contents of the DBI assembler, which is the coded character of the key that was pressed. The output of the DBI assembler is sent to the CPU on DBI.

With this information, the stored program in the CPU determines the cause of the interrupt, branches to that routine, and performs the required operation. When the operation is complete, the CPU can issue another start I/O instruction to the attachment.

Refer to the flowchart on page 7-310 for the operation. The only difference is that a keyboard interrupt can be generated by pressing either the inquiry request key or a data key.



ALTER STORAGE OPERATION

The alter mode of the keyboard is used to key in test programs and subroutines. The operation of the keyboard in this mode is intended for field engineering use as an aid in locating machine troubles by checking and testing machine functions.

When the CE mode selector switch is at the alter storage position, the system stops at clock 9, and the bail contact modified signal (generated by the bail contacts being closed) turns on the bail latch. The bail latch output signal turns on the bail magnet driver which provides current through the bail magnet coils. This causes the bail bar to move back and unlock the keyboard. The 'alter up' latch (page 7-203) sets and the keyboard unlocks.

Keys A through F, and 0 through 9 are the only keys that can be used in alter storage mode. Depression of any other key causes the bail bar to go forward and lock the keyboard. If this occurs, position the CE mode selector switch to the process position and press SYSTEM RESET. The keyboard unlocks and allows the return to alter storage mode. Before continuing, an alter SAR must be performed.

Data entered form the keyboard begins at storage address 0000, unless an alter SAR is made to a specific starting address.

For this description of the encode board refer to page 7-201.

First Key Depression (Odd Key Count)

- Depress key.
- EDS switch closes, allowing current through its contacts and associated diodes in the encode board.
- The output of the diode gives the proper inputs to the bit latches to obtain the hexadecimal value for the key pressed (first half byte).
- These lines also provide inputs to the 'group H' latch. This latch determines that the key pressed is a valid hexadecimal character.
- Bits 0, 1, 2, and 3 are gated by the 'alter up' latch output to turn on the '1st 1/2 byte' latch. If either zero (0) key is depressed, the P bit turns on the first half byte latch.
- With '1st 1/2 byte' latch on, one input to the 'alter up' latch is removed.
- At this time data is gated through the DBI assembler onto DBI, but it is not accepted by the CPU because it is idling at clock 9 time. However, the keyboard is restored (unlocked) to allow entering the second half byte from the keyboard.

Keyboard Restore

- 'Alter up' latch ANDed with 'group H' latch, '1st 1/2 byte' latch and (not) 'bail contacts' generate a 'drop bail pulse' line.
- This line turns off the bail latch, causing the bail magnet current to drop and the bail bar moves forward under spring tension.
- The bail contacts close generating a 'bail contact' signal, which:
  1. Turns off the 'group H' latch.
  2. Turns off the 'P bit' latch.
  3. Turns on the 'bail latch'.
- The 'bail latch' causes the bail magnets to receive current to draw the bail bar back and unlock the keyboard.
- When the bail contacts open, the 'bail reset' line is activated to turn off the 'alter up' latch.
- The active bits, representing the hexadecimal key that was pressed, now make up the first half byte of data. The keyboard is unlocked and ready for the second half byte of data (even key count) to be entered.

Second Key Depression (Even Key Count)

- Depress key.
- EDS switch closes, allowing current through its contacts and associated diodes in the encode board.
- The output of the diode gives the proper inputs to the bit latches to obtain the hexadecimal value for the key pressed (second half byte).
- With the 'alter up' latch off, the lower group of bit latches (4, 5, 6, and 7) are gated to form the second half byte (hexadecimal).
- The '2nd 1/2 byte' latch is turned on by bit 4, 5, 6, 7, or P with 'alter up' latch off.
- 'Alt char ready' is now activated.
- 'Alt char ready' turns on the 'system start' latch in the CPU to start the system.
- 'Clock 2' ANDed with 'alt char ready' turns off the 'bail latch' and locks the keyboard.
- The CE mode selector switch in the alter storage position gates the keyboard bit latch outputs out of the DBI assembler.
- With the 'bail latch' off, the bail contacts:
  1. Turn off the 'P bit', 'group H', and 'alter up' latches.
  2. Turn on the 'bail latch'.
  3. The 'bail contact' line ANDed with 'alter char ready', and (not) 'inq req' latch turns on the 'reset' latch.
  4. The 'reset' latch resets the bit latches (0 through 3 and 4 through 7).
- The 'alter up' latch remains off until the 'reset' latch is turned off. When it comes on again, the keyboard is ready for the next odd-key depression.

Zero Key Depression

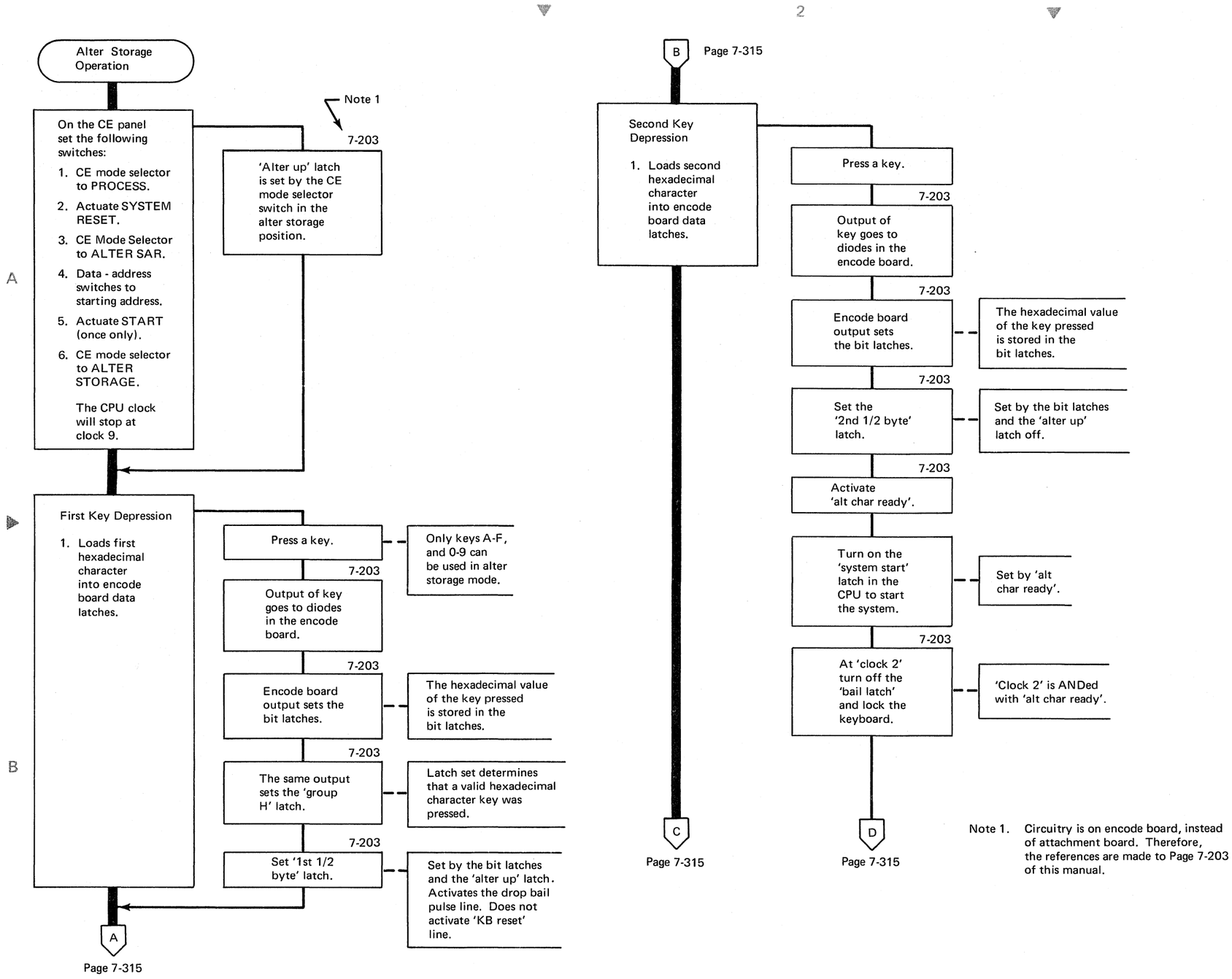
When the zero key is pressed, no hexadecimal character is generated, but the 'P bit' latch is set. This latch being set turns on the '1st 1/2 byte' latch. The 'P bit' latch ANDed with the 'alter up' latch off, turns on the '2nd 1/2 byte' latch. This generates an 'alter char ready' signal but no DBI bits when the 0 through 7 bit latches are not activated by the encode board circuit diodes.

The 'P bit' latch turns on both half byte latches, but only:

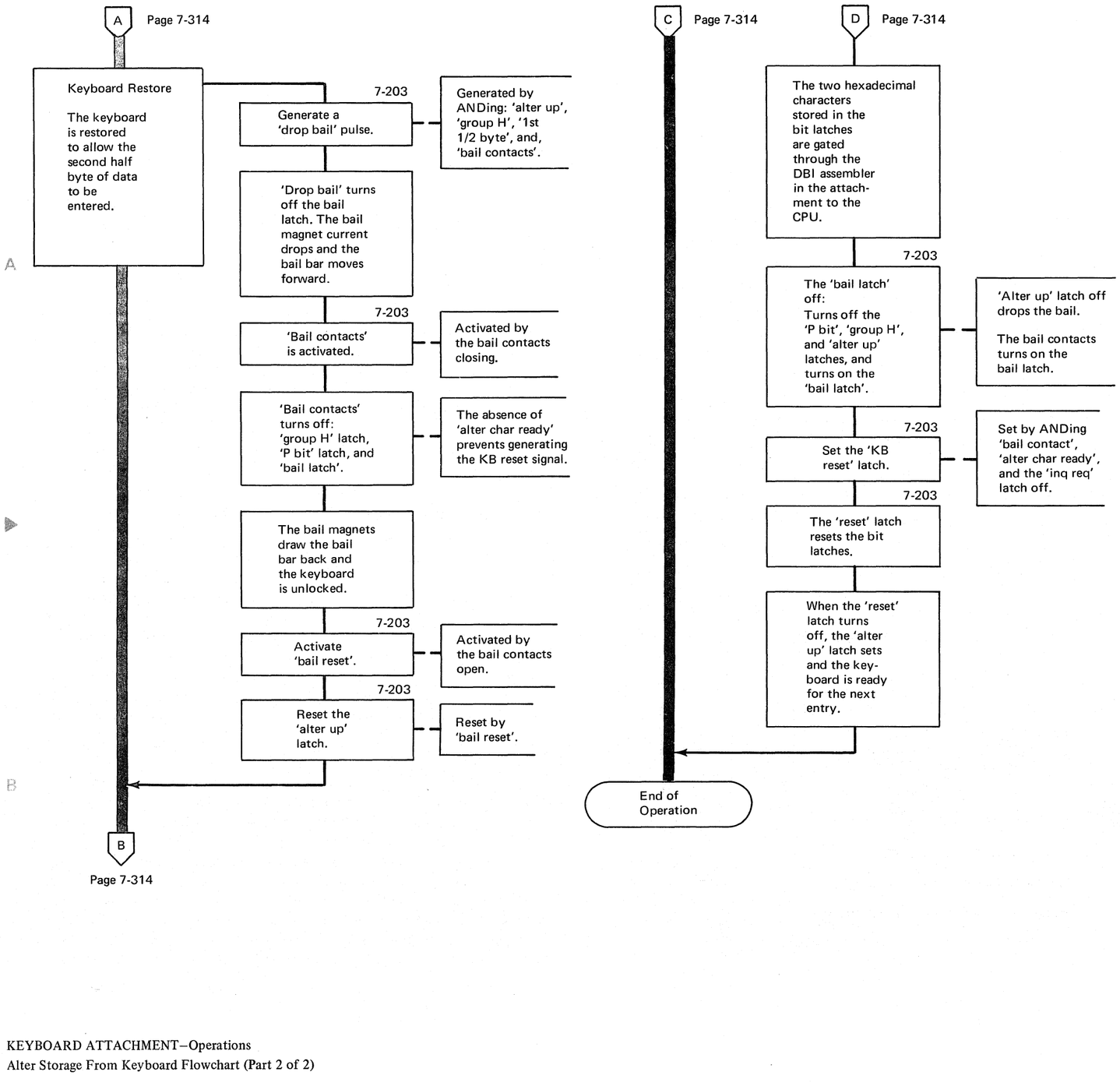
1. The '1st 1/2 byte' latch when a key is pressed on an odd key count.
2. The '2nd 1/2 byte' latch when a key is pressed on an even key count.

This is done by ANDing (not) 'alter up' and 'P bit' to turn on the '2nd 1/2 byte' latch a zero key is pressed on an even key count.

The 'P bit' line is active when any key giving an even number of bits is pressed (the P bit to the attachment is blocked by 'alter char ready'). Since 'P bit' does not enter the system DBI from the encode board in alter storage mode, the 'P bit' is generated in the attachment circuits and ANDed with the 'alter char ready' line. This allows correct parity to enter the CPU.



Note 1. Circuitry is on encode board, instead of attachment board. Therefore, the references are made to Page 7-203 of this manual.



KEYBOARD ATTACHMENT–Operations
Alter Storage From Keyboard Flowchart (Part 2 of 2)

TYPAMATIC OPERATION

Typamatic keys (tab and backspace) have two operational levels or stops. The first level permits a single operation and is indicated by a spring loaded stop when a light key stroke is used. The second level allows a repeat action without repeated key strokes. A heavy key stroke will push the key lever through the spring loaded first stop into the typamatic level. This repeats the key function as long as the key is held in the lower level.

The typamatic function is indicated by the lower level of the key lever. However, the typamatic function is performed by the control program.

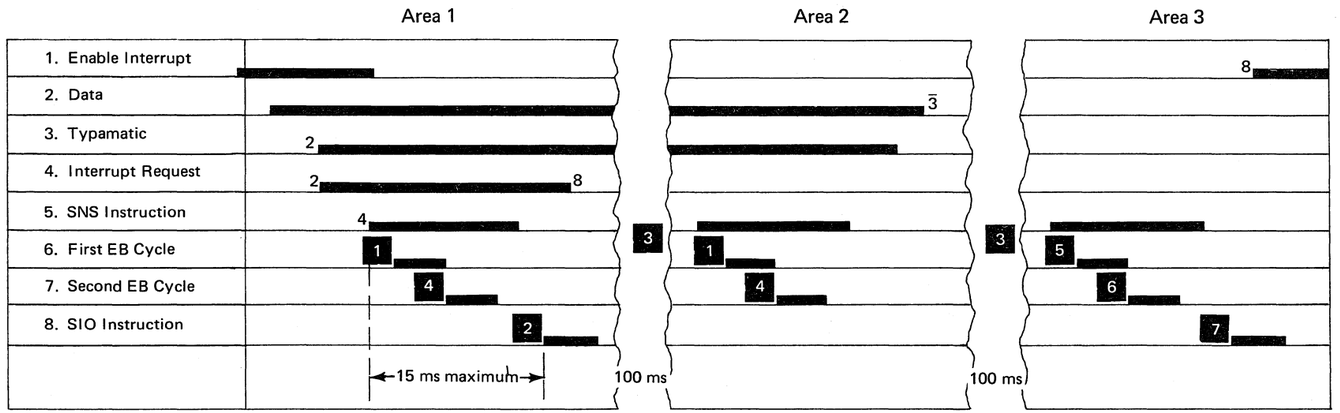
Refer to the timing chart on this page for the following description of the typamatic operation.

Area 1 (In Timing Chart)

1. Assume that the keyboard is ready (enabled and unlocked).
2. The operator presses the tab or backspace key.
3. Data bits are stored in the bit latches in the keyboard encode board.
4. These bits are recognized as typamatic bits (bit 3 and bit 6 are prepared to be sensed on the first EB cycle of a sense instruction).
5. The next time the 'interrupt poll' line is activated, a system level 1 interrupt will occur (unless a higher level interrupt or cycle steal has been requested).
6. During the subroutine of the program, a sense instruction is given to the keyboard.
   a. First EB cycle–bit 3 (function) and bit 6 are sensed to indicate a typamatic operation.
   b. Second EB cycle–data is sensed (tab or backspace).
7. A start I/O instruction is given to the keyboard with bit 4 on in the control code to drop the bail and lock the keyboard. The start I/O instruction must occur within 15 ms of the sense instruction.
8. A time out of approximately 100 ms for the software begins. This time is required to maintain a 10 cycle per second rate for the CRT cursor. See "Note 2."
9. During the time out, the CRT cursor or print element can be moved one increment in the appropriate direction.

Area 2 (In Timing Chart)

1. The typamatic operation is still in process.
2. A sense instruction is issued to the keyboard at the end of the 100 ms time out.
   a. First EB cycle–bit 3 and bit 6 are again sensed indicating a typamatic operation.
   b. Second EB cycle–data is again sensed (tab or backspace).
3. The 100 ms time out occurs again.
4. The CRT cursor or the print element can again be moved.



1. DBI bits 3 and 6 identify typamatic character to the program.
2. Start I/O instruction must have bit 4 on in the control code to drop the bail and unlock the keyboard.
3. Program time out required for 10 cycle per second maximum cursor or print element rate.
4. Data byte is transferred (identifies tab or backspace key).
5. No typamatic bit (6) is sensed in the status byte (the key was released).
6. No data bits are sensed in the data byte (only the P bit).
7. Start I/O instruction has bits 3 (to reset parity check), 5 (to pick the bail and unlock the keyboard), 6 (to enable interrupts), and 7 (to reset the current interrupt request) on.

Note 1. When tab or backspace keys are depressed, bits 3 and 6 of the first sense byte are on. This is true even if the keys are not fully depressed.

Note 2. Parity checks or additional incrementing may occur if approximate time intervals are not maintained.

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Area 3 (In Timing Chart)

1. The operator has released the key and therefore the typamatic operation is no longer in process.
2. A sense instruction is issued to the keyboard.
   a. First EB cycle–the typamatic bits (3 and 6) are no longer present. Bit 0 is sensed.
   b. Second EB cycle–data is sensed, only bit P is present.
3. A start I/O instruction is issued to the keyboard. The control code must have bit 3 on (to reset bit 0), bit 5 on (to pick the bail and unlock the keyboard), bit 6 on (to enable interrupts), and bit 7 on (to reset the current interrupt request).

Section 9. Printer and Ledger Card Device Attachments

This section of the 5406 FETMM contains the theory and maintenance diagrams for the 5213 and 2222 Printer attachment and ledger card device attachment. It consists of six chapters as follows:

Chapter 1. Introduction to the Printer Attachment
Chapter 2. Functional Units of the Printer Attachment
Chapter 3. Operations of the Printer Attachment
Chapter 4. Introduction to the Ledger Card Device Attachment
Chapter 5. Functional Units of the Ledger Card Device Attachment
Chapter 6. Operations of the Ledger Card Device Attachment

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Chapter 1. Introduction

PRINTER ATTACHMENT

The IBM 5213/2222 Printer attachment provides a means for the attached 5213 or 2222 Printer to use the facilities of the IBM 5406 Processing Unit to communicate with main storage. The attachment provides the communication lines between the printer and the processing unit and controls the transfer of all information between the two.

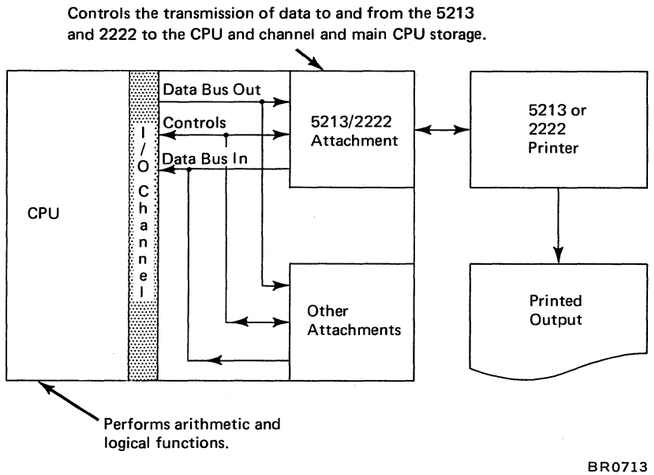
A ledger card device attachment is a part of the printer attachment if a 2222 Printer is installed. The ledger card device attachment is described separately in chapters 4, 5, and 6 of this section (section 9).

The attachment circuitry is MST-1 logic, physically located on gate A, board A2 in the 5406 Processing Unit. The control interface lines between the attachment board and the electronics board are SLD-100 levels. Conversion to MST occurs at the attachment board.

The communications path between the processing unit and the printer attachment is through the I/O channel. Using this channel, data and control information is transferred from the processing unit, and status is sent to the processing unit under control of stored program instructions.

During the process of exchanging information, the printer and the processing unit operate together in multiplexer mode. This means the information transfer takes place between processing unit cycles on a priority basis with other devices.

By the means of a fixed-cycle steal priority, I/O cycles may be interleaved between any two processing unit cycles.



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PRINTER

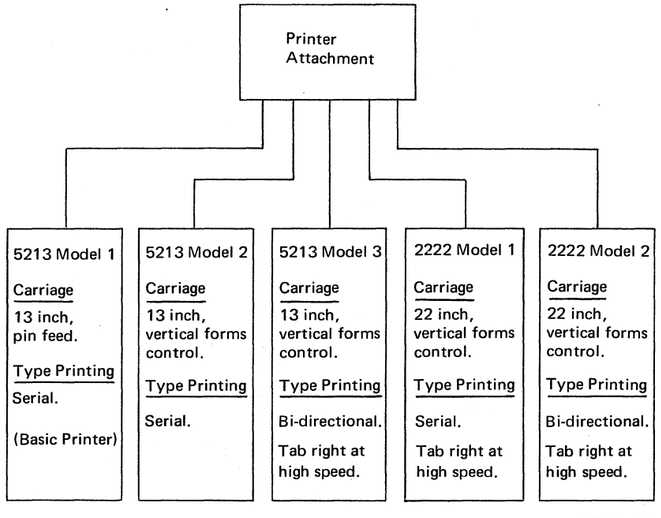
The 5406 Printer attachment has the capability of controlling five different models of printers (one printer per system), each of which is available in a variety of optional features. The basic printer is a 13 inch carriage serial printer which prints at a rate of 85 characters per second.

The five models of printers available are:

1. The IBM 5213 Printer Model 1 can print 132 characters per line at 85 characters per second. Forms are moved by a pin feed platen with single or double spacing selectable by the operator.
2. The IBM 5213 Printer Model 2 has the same characteristics of the Model 1, except the carriage is controlled by a pin feed tractor with tapeless vertical forms control.
3. The IBM 5213 Printer Model 3 can print 132 characters per line at 85 characters per second or functions as a bi-directional printer that can print approximately fifty 96-character lines per minute. Forms movement is controlled by a pin feed tractor with tapeless vertical forms control.
4. The IBM 2222 Printer Model 1 can print 220 characters at 85 characters per second. Forms are handled with a dual pin feed tractor with tapeless vertical forms control (on the primary carriage only).

   The 2222 Printer also has as a standard feature a ledger card device. The ledger card device allows feeding, printing, and identification of ledger cards.
5. The IBM 2222 Printer Model 2 has the same characteristics as the Model 1 Printer, except that it is a bi-directional printer. It can print approximately fifty 96-character lines per minute.

The following illustration shows the combinations of printers and features available.



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Vertical forms control allows skipping a number of lines from 2 to 256. The pin feed carriage on the 5213 Model 1 can space one or two lines by setting the manual control on the printer to the proper position.

Printing Principle

Printing is done by a print head capable of making seven dots in a vertical arrangement. The print head is moved across the paper from left to right or from right to left at a constant velocity. As the print head moves through one character space, the head can produce dots in any of seven horizontal positions. A restriction is applied, however, that none of the vertical dot positions can produce a dot in two consecutive horizontal dot positions. Therefore, the maximum number of horizontal dots that can be produced by any dot position on the print head is four.

Printer Functions

The serial printer (printing without the line printing feature) prints with the print head moving from left to right. The bi-directional printing feature allows printing with the print head moving either from left to right or right to left. The characters that can be printed and the bit patterns (EBCDIC code) in storage that caused each character to be printed are shown on page 9-102.

In addition to printing data, the following functions can be performed:

1. Tab right
2. Tab left
3. Element return
4. Primary carriage index
5. Primary carriage skip (vertical forms control tractor only)
6. Secondary carriage single index (dual feed carriage)

Dual Feed Carriage

Dual feed carriage is a standard feature of the 2222 Printer. Vertical forms control is utilized on the primary feed carriage with the ability to vertically space or skip. The secondary feed carriage is a single vertical space carriage. Vertical motion on the secondary carriage can overlap all other printer functions except printing.

Ledger Card Device

The ledger card device on the 2222 Printer allows the feeding, checking, and printing of data on ledger cards. The ledger card device is designed to interfere as little as possible with paper handling and readability of data printed on forms. Printing and forms motion of the ledger card are under control of the program.

For identification purposes and checking that the proper document is being printed on, space is provided for printing coded numeric identification in the upper right edge of the card and for reading such coded notation.

The ledger card device also has a function that allows feeding the cards and locating the first available print line. Provision is also made for automatically signalling to the program when no print lines are available.

The right edge of the ledger card is always positioned in the farthest right printing positions of the 22 inch printer. The last 6 print positions on the ledger card (positions 215–220) are reserved for the line finder marks and two identification number (ID) code marks. These marks are printed in positions 216, 218, and 220. Except for the print mark code, no printing should be done beyond position 214.

The line finder marks are used for locating the next available print line. A line finder must be printed for each line printed to prevent over-printing the next time line posting of the same ledger card takes place.

PRINTER FEATURES

Bi-directional Printing

Bi-directional printing (line printing) is a standard feature of the 5213 Printer Model 3, and the 2222 Printer Model 2. This allows printing with the print head moving either left to right or right to left. Printing can be performed at a rate of approximately fifty 96-character lines per minute. Printing more characters results in a slower throughput; printing fewer characters results in a higher throughput.

LOCAL STORAGE REGISTERS (LSR)

There are three local storage registers (located in the CPU) that are assigned to the printer attachment. Two of these are used in print operations, and the third is used with the ledger card device (LCD).

Print Data Address Register (PDAR)

The PDAR contains the leftmost or starting address of the data field when issuing a print command. This address has no core boundary restrictions.

This LSR must be reinitialized after each print command when not printing consecutive core fields. The LSR content points to the last printed character location plus one at the completion of a print command.

Print Command Address Register (PCAR)

The PCAR contains the leftmost storage address of the command field. The byte at this address contains the first command to be executed.

Locate Line Address Register (LLAR)

The LLAR is used only with the ledger card device to locate the next printable line and to detect the last printable line.

BITS 2, 3 / BITS 0, 1

BITS 4567	00 00	00 01	00 10	00 11	01 00	01 01	01 10	01 11	10 00	10 01	10 10	10 11	11 00	11 01	11 10	11 11
0000	blnk	&	-	0	blnk	&	-	0	blnk	&	-	0	blnk	&	-	0
0001	A	J	/	1	A	J	/	1	A	J	/	1	A	J	/	1
0010	B	K	S	2	B	K	S	2	B	K	S	2	B	K	S	2
0011	C	L	T	3	C	L	T	3	C	L	T	3	C	L	T	3
0100	D	M	U	4	D	M	U	4	D	M	U	4	D	M	U	4
0101	E	N	V	5	E	N	V	5	E	N	V	5	E	N	V	5
0110	F	O	W	9	F	O	W	6	F	O	W	6	F	O	W	6
0111	G	P	X	7	G	P	X	7	G	P	X	7	G	P	X	7
1000	H	Q	Y	8	H	Q	Y	8	H	Q	Y	8	H	Q	Y	8
1001	I	R	Z	9	I	R	Z	9	I	R	Z	9	I	R	Z	9
1010	¢	↑		:	¢	↑	See Note 1	:	¢	↑		:	¢	↑		:
1011	.	$	,	#	.	$	,	#	.	$	,	#	.	$	,	#
1100	<	*	%	@	<	*	%	@	<	*	%	@	<	*	%	@
1101	(	)	_	'	(	)	_	¬	(	)	_	'	(	)	_	'
1110	+	;	>	=	+	;	>	=	+	;	>	=	+	;	>	=
1111	|	¬	?	≠	|	¬	?	≠	|	¬	?	≠	|	¬	?	≠

BR0715A

Note 1. Code XX101010 will print a special dash used by the ledger card device for ID marks and line finder marks.

Shared LSR's

The ledger card device uses the PCAR and the PDAR along with the printer. The PCAR is used in the same manner by both devices. In LCD operations, the PDAR contains the leftmost or starting address of the identification (ID) number that will be read from the ledger card. The address has no core boundary restrictions. The LSR content points to the last position of the ID number plus one at the completion of the feed, read ID, and locate next print line command; or feed, read ID, and eject command.

CHARACTER SET

The basic printer attachment provides 62 print characters plus blank. This does not include the special dash used by the ledger card device.

The chart below shows the normal EBCDIC code used to print the basic character set (a wedge in the corner of the block denotes a character in the basic set). All other blocks show the fold (bits 0 and 1), or what will print if presented to the attachment.

LOAD I/O INSTRUCTION

- The load I/O instruction consists of three or four bytes (three if indexing is used).
- The load I/O instruction selects the matrix printer or the LCD if the device address equals E (hexadecimal).
- Two bytes in storage, addressed by the operand address, are loaded into the destination specified by the N code of the Q byte.

The load I/O instruction is composed of three or four bytes. The first byte is the op code, a Y1 (hexadecimal) which indicates a load I/O operation. The second byte is the Q byte which contains the device address, an M code, and an N code. The third and/or fourth bytes indicate the address of the information to be loaded into the local storage register (LSR), or in the case of a control load I/O indicate the address of a byte in main storage which is bit significant as a diagnostic aid.

Q Byte Description

The upper four bits (bits 0-3) specify the device address of the matrix printer E (hexadecimal). Bit 4 is the M code which is used to determine if the instruction is for the printer (bit 4 = 0), or if it is for the ledger card device (bit 4 = 1). The lower three bits are the N code or the function code.

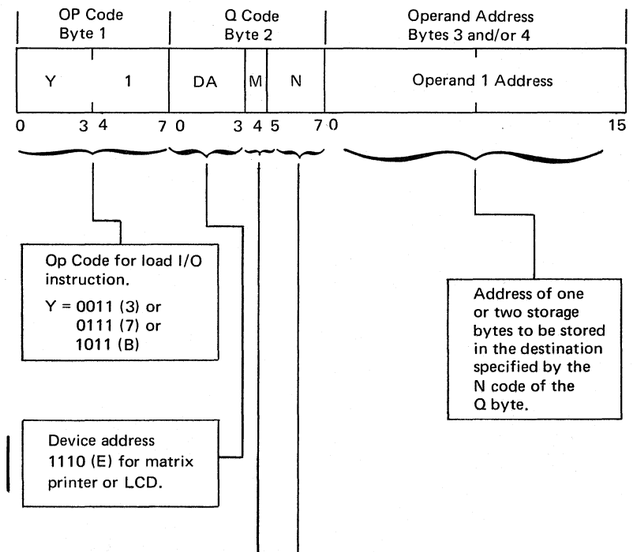
Operand Address

The operand address of the load I/O instruction can serve one of two purposes. It can contain the address of storage bytes to be stored in the LSR selected for loading, or it can contain the address of the storage byte which is bit significant for diagnostic testing.

Parity and Error Conditions

The load I/O instruction is accepted only if the printer is not busy (except for a control load I/O which is always accepted). A parity error detected by the attachment results in a processor check stop and the processor check light comes on.

LOAD I/O (LIO) INSTRUCTION FORMAT



N Code

Bits 5 6 7	Destination
0 1 X	Control LIO—bit significant
	Bit
	0 Diagnostic block high speed or LCD diagnostic reset (on = set, off = reset).
	1 Force DBO check. (Printer only)
	2 Force diagnostic stepper emitter advance pulse or LCD emitter pulse.
	3 Force diagnostic print gate emitter, vertical advance pulse, or LCD sense cells off (on = set, off = reset).
	4 Diagnostic mode (on = set, off = reset).
	5 Integrated emitter or LCD card in switch (on = set, off = reset).
	6 Use 2nd EOF latch or LCD card out switch (on = set, off = reset).
	7 End of forms indicator latch (on = set, off = reset). (Printer only)
1 0 X	Print data address register (PDAR)
1 1 X	Print command address register (PCAR)
0 0 X	Locate line address register (LLAR)—(LCD only)

X means bit can be a "1" or "0".

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TEST I/O INSTRUCTION

- The test I/O instruction consists of three or four bytes (three bytes if indexing is used).
- The test I/O instruction selects the matrix printer or the LCD when the device address equals E (hexadecimal).
- The test I/O instruction tests for:

Printer	*Ledger card device*
1. Unit check	1. Unit check
2. End of forms	2. Last printable line
3. Busy	3. LCD busy
4. Element at left margin	4. LSR busy
	5. Read ID busy
	6. Card not aligned

The test I/O instruction is composed of either three or four bytes. The first byte is the op code, a Z1 (hexadecimal) which indicates a test I/O operation. The second byte is the Q byte which contains the device address, an M code, and an N code. The third and fourth bytes contain the branch to address if the condition tested for is met.

Q Byte Description

The upper four bits (bits 0-3) specify the device address for the matrix printer, E (hexadecimal). Bit 4 is the M code which is used to determine if the instruction is for the printer (bit 4 = 0), or if it is for the ledger card device (bit 4 = 1). The lower three bits (bits 5-7) are the N code which determines the test to be performed.

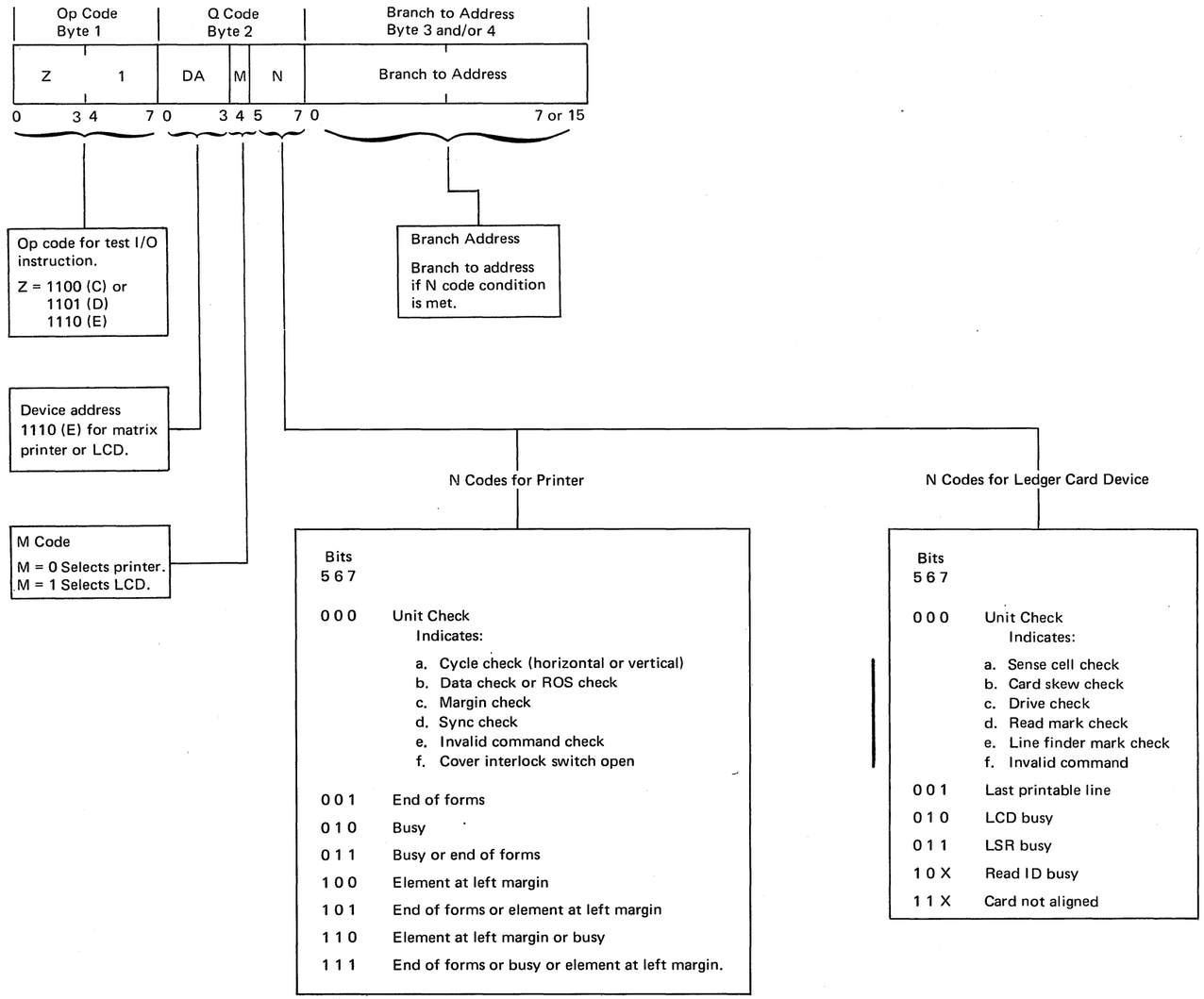
Branch To Address

The branch to address contains the address to be branched to if the conditions tested for as specified by the N code are met. It is either one or two bytes long depending upon the op code.

Parity and Error Conditions

Odd parity must be maintained in the test I/O instruction. A parity error detected by the attachment results in a processor check stop, and the processor check light comes on.

TEST I/O (TIO) INSTRUCTION FORMAT



X means bit can be a "1" or "0".

Note. In the case of combined tests, any one of the tested conditions will cause the branch to occur.

BR0718B

LCD TIO Test Condition Description

Unit Check indicates any one of the LCD check conditions as shown in the TIO format diagram.

Last Printable Line indicates (1) that the last allowable print line is positioned at the platen or, (2) all the print lines have been used and the ledger card was ejected from the LCD. A sense I/O instruction must be issued to determine which of the two conditions exist. If the SNS instruction determines that either the card in switch or card out switch is made, condition 1 exists, if neither switch is made, condition 2 exists.

LCD Busy indicates that the LCD is executing an SIO instruction.

LSR Busy indicates:

1. A printer chained command is in progress.
2. A printer count command is in progress.
3. An LCD feed, read ID, and locate next line operation is in progress.
4. An LCD feed, read ID, and eject command is in progress and the ID number has not been transferred into main storage.
5. An LCD read all line finder marks command is in progress and all the line finder marks have not been read.
6. An LCD read back and eject command is in progress and the line finder mark has not been read.
7. An LCD index command is in progress.

Note. If the LCD LSR busy condition is true (active), printer and LCD operations cannot be overlapped.

Read ID Busy indicates that the ledger card ID number is being read from the ledger card and transferred into main storage. This condition is present during feed, read ID, and locate; or feed, read ID, and eject operations only. During a read all line finder marks command, read ID busy is active until 43 bytes (the complete card) have been read.

Card Not Aligned indicates that the ledger card is not aligned at the first feed rolls in the LCD. This condition must be present before issuing the following commands: feed, read ID, and locate; feed, read ID, and eject; and read all line finder marks. This test will also cause the LCD I/O attention light to turn on, and raise the LCD card gate if a card is not in the LCD.

ADVANCE PROGRAM LEVEL INSTRUCTION

- The advance program level instruction consists of three bytes.
- The advance program level instruction selects the matrix printer or the LCD when the device address equals E (hexadecimal).
- The advance program level instruction tests for:

	Printer		*Ledger Card Device*
1.	Unit check	1.	Unit check
2.	End of forms	2.	Last printable line
3.	Busy	3.	LCD busy
4.	Element at left margin	4.	LSR busy
		5.	Read ID busy
		6.	Card not aligned

The advance program level instruction is composed of three bytes. The first byte is the op code, an F1 (hexadecimal) which indicates an advance program level operation. The second byte is the Q code which contains the device address, an M code, and an N code. The third byte is not used.

Q Byte Description

The upper four bits (bits 0-3) specify the device address for the matrix printer, E (hexadecimal). Bit 4 is the M code which is used to determine if the instruction is for the printer (bit 4 = 0), or if it is for the ledger card device (bit 4 = 1). The lower three bits (bits 5-7) are the N code which determines the test to be performed.

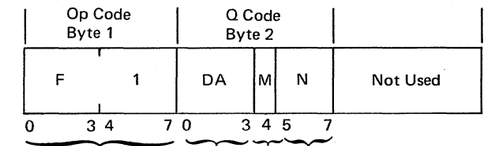
Application

If the specified conditions tested for do not exist, the operation becomes equivalent to a no-op, and proceeds to the next sequential instruction. If the specified condition is present, the operation causes the CPU to loop (IR backup) on the APL instruction until the specified condition is no longer present, and then proceeds to execute the next sequential instruction.

Parity and Error Conditions

Odd parity must be maintained in the advance program level instruction. A parity error detected by the attachment results in a processor check stop, and the processor check light comes on.

ADVANCE PROGRAM LEVEL (APL) INSTRUCTION FORMAT



Op code for advance program level instruction.

Device address 1110 (E) for matrix printer or LCD .

M Code
M = 0 Selects printer.
M = 1 Selects LCD.

N Codes for Printer

Bits 5 6 7	
0 0 0	Unit Check Indicates: a. Cycle check (horizontal or vertical) b. Data check or ROS check c. Margin check d. Sync check e. Invalid command check f. Cover interlock switch open
0 0 1	End of forms
0 1 0	Busy
0 1 1	Busy or end of forms
1 0 0	Element at left margin
1 0 1	End of forms or element at left margin
1 1 0	Element at left margin or busy
1 1 1	End of forms or busy or element at left margin.

N Codes for Ledger Card Device

Bits 5 6 7	
0 0 0	Unit Check Indicates: a. Sense cell check b. Card skew check c. Drive check d. Read mark check e. Line finder mark check f. Invalid command
0 0 1	Last printable line
0 1 0	LCD busy
0 1 1	LSR busy
1 0 X	Read ID busy
1 1 X	Card not aligned

X means bit can be a "1" or "0".

Note. In the case of combined tests, any one of the tested conditions will cause an IR backup to occur.

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LCD TIO Test Condition Description

Unit Check indicates any one of the LCD check conditions as shown in the TIO format diagram.

Last Printable Line indicates (1) that the last allowable print line is positioned at the platen or, (2) all the print lines have been used and the ledger card was ejected from the LCD. A sense I/O instruction must be issued to determine which of the two conditions exist. If the SNS instruction determines that either the card in switch or card out switch is made, condition 1 exists, if neither switch is made, condition 2 exists.

LCD Busy indicates that the LCD is executing an SIO instruction.

LSR Busy indicates:

1. A printer chained command is in progress.
2. A printer count command is in progress.
3. An LCD feed, read ID, and locate next line operation is in progress.
4. An LCD feed, read ID, and eject command is in progress and the ID number has not been transferred into main storage.
5. An LCD read all line finder marks command is in progress and all the line finder marks have not been read.
6. An LCD read back and eject command is in progress and the line finder mark has not been read.
7. An LCD index command is in progress.

Note. If the LCD LSR busy condition is true (active), printer and LCD operations cannot be overlapped.

Read ID Busy indicates that the ledger card ID number is being read from the ledger card and transferred into main storage. This condition is present during feed, read ID, and locate; or feed, read ID, and eject operations only. During a read all line finder marks command, read ID busy is active until 43 bytes (the complete card) have been read.

Card Not Aligned indicates that the ledger card is not aligned at the first feed rolls in the LCD. This condition must be present before issuing the following commands: feed, read ID, and locate; feed, read ID, and eject; and read all line finder marks. This test will also cause the LCD I/O attention light to turn on, and raise the LCD card gate if a card is not in the LCD.

SENSE I/O INSTRUCTION

- The sense instruction consists of three or four bytes (three if indexing is used).
- The sense instruction selects the matrix printer or the LCD when the device address equals E (hexadecimal).
- Data from the area specified by the N code is placed in main storage in the location specified by the operand address.
- The sense instruction can be used at any time, whether the printer is busy or not.

The sense instruction is composed of three or four bytes. The first byte is the op code, a Y0 (hexadecimal) which indicates a sense operation. The second byte is the Q bye which contains the device address, an M code, and an N code. The third and fourth bytes specify the area in main storage to store the sense information.

Q Byte Description

The upper four bits (bits 0-3) specify the device address for the matrix printer, E (hexadecimal). Bit 4 is the M code which is used to determine if the instruction is for the printer (bit 4 = 0), or if it is for the ledger card device (bit 4 = 1). The lower three bits (bits 5-7) are the N code.

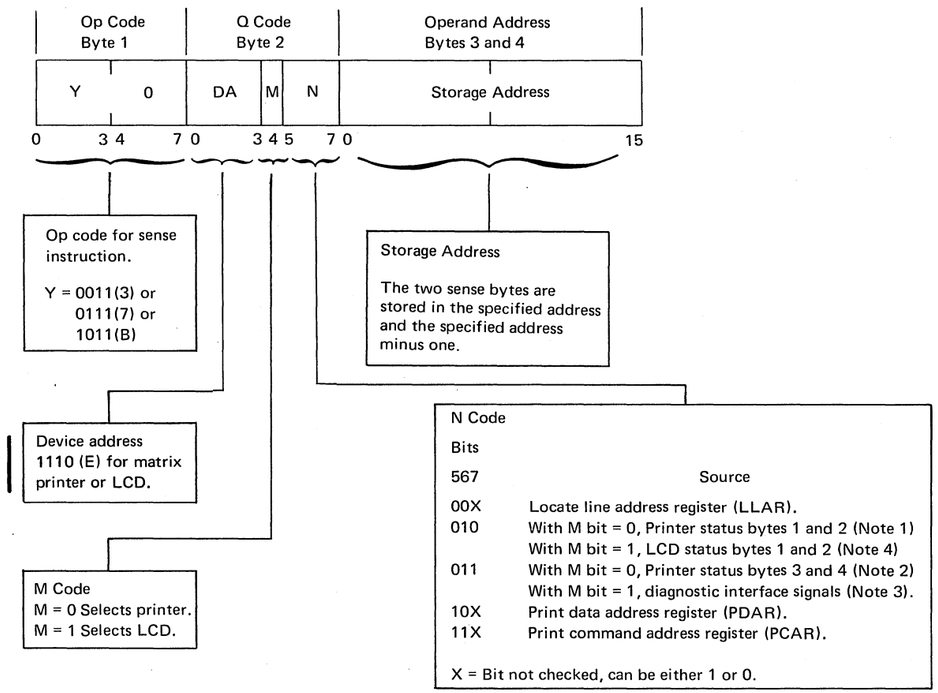
Operand Address

The operand address of the sense instruction specifies the location in main storage in which to store the sense information.

Parity and Error Conditions

The sense instruction is accepted at any time by the printer. A parity error detected by the attachment results in a processor check stop and the processor check light comes on.

SENSE I/O (SNS) INSTRUCTION FORMAT



Note 1. Status bytes 1 and 2

Bit	Status Byte 2 (oper addr -1)	Bit	Status Byte 1 (oper addr)
0	Count end latch	0	Horizontal cycle check
1	Print left command	1	Data check
2	Matrix counter trigger 1	2	Margin check
3	Matrix counter trigger 2	3	Sync check
4	Matrix counter trigger 4	4	ROS check
5	Printer ready	5	Vertical cycle check
6	SS2	6	Primary carriage EOF
7	SS1	7	Invalid command

Note 2. Status bytes 3 and 4

Bit	Status Byte 4 (oper addr -1)	Bit	Status Byte 3 (oper addr)
0	SSA	0	Secondary carriage EOF
1	SS3	1	Matrix output hammer dr 1
2	Stepper trigger A	2	Matrix output hammer dr 2
3	Stepper trigger B	3	Matrix output hammer dr 3
4	SSZ	4	Matrix output hammer dr 4
5	SSY	5	Matrix output hammer dr 5
6	SSX	6	Matrix output hammer dr 6
7	SSW	7	Matrix output hammer dr 7

Note 3. Diagnostic device interface signals

Bit	LCD Signals* (oper addr)	Bit	Printer Device Signals (oper addr -1)
0	Skip line SS1	0	5213 printer attached
1	Skip line SS2	1	Not vertical forms control
2	Late mark	2	Not bi-directional print feature
3	Special tie-off	3	Secondary carriage EOF
4	Card alignment SS	4	Not Rm sw 1 slow and not Lm sw 2 stop
5	Spare	5	Rm sw 2 stop or Lm sw 1 slow
6	Spare	6	Primary or secondary forms motion contact
7	Stop SS	7	Primary forms emitter advance

*If the LCD is not installed, this byte will be hex 00 with proper parity.

Note 4. Ledger card device status bytes 1 and 2

Bit	Status Byte 2 (oper addr -1)	Bit	Status Byte 1 (oper addr)
0	Sense amp 1	0	Sense amp check
1	Sense amp 2	1	Card skew check
2	Sense amp 3	2	Drive check
3	Sense amp 4	3	Read mark check
4	Timing pulse	4	Line finder mark check
5	Drive check SS	5	Invalid command check
6	Activate LCD feed clutch	6	Card in switch on
7	Hold busy SS	7	Card out switch on

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START I/O INSTRUCTION

- The start I/O instruction consists of three bytes.
- The start I/O instruction selects the matrix printer or the LCD when the device address equals E (hexadecimal).
- The start I/O instruction initiates cycle steals to obtain printer or LCD commands.

The start I/O instruction is composed of three bytes. The first byte is the op code, an F3 (hexadecimal) which indicates a start I/O operation. The second byte is the Q byte which contains the device address, an M code, and an N code. The third byte is the I-R byte which contains the control code. The start I/O instruction has only one function, to initiate cycle stealing to obtain commands for the printer or LCD.

Q Byte Description

The upper four bits (bits 0–3) specify the device address of the matrix printer, E (hexadecimal). Bit 4 is the M code which is used to determine if the instruction is for the printer (bit 4 = 0), or if it is for the ledger card device (bit 4 = 1). The last three bits are the N code and are not used for a printer start I/O instruction.

I-R Byte (Control Code)

The I-R byte contains the control code. For the printer, it specifies if the operation to be performed is a serial or a bi-directional print operation. For the LCD, it specifies if a diagnostic read all line finder marks operation, or a normal LCD operation is to be performed.

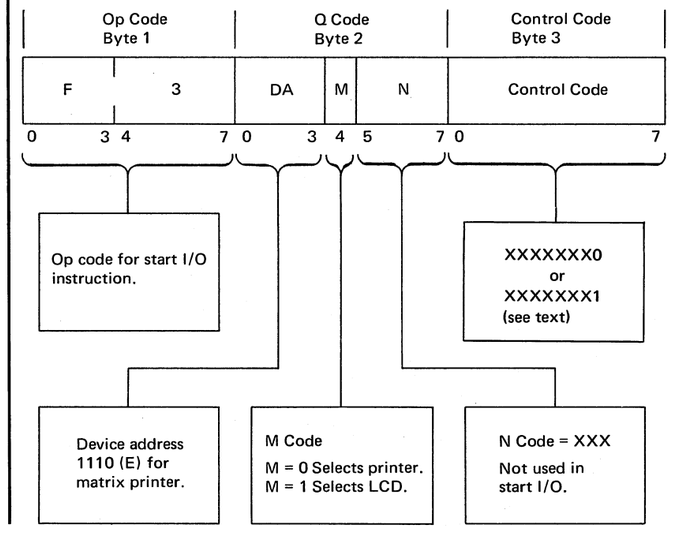
A control code of XXXXXXX0 specifies a serial print operation or a normal LCD operation.

A control code of XXXXXXX1 specifies a bi-directional print operation or a diagnostic read all line finder marks operation for the LCD.

Parity and Error Conditions

Odd parity must be maintained in the start I/O instruction. If a parity error is detected in the attachment, a processor check stop occurs and the processor check light comes on. Program interlock is effective if a printer busy condition is detected, or if operator intervention is required as indicated by the I/O attention light.

START I/O (SIO) INSTRUCTION FORMAT



X = Bit not checked, can be either 1 or 0.

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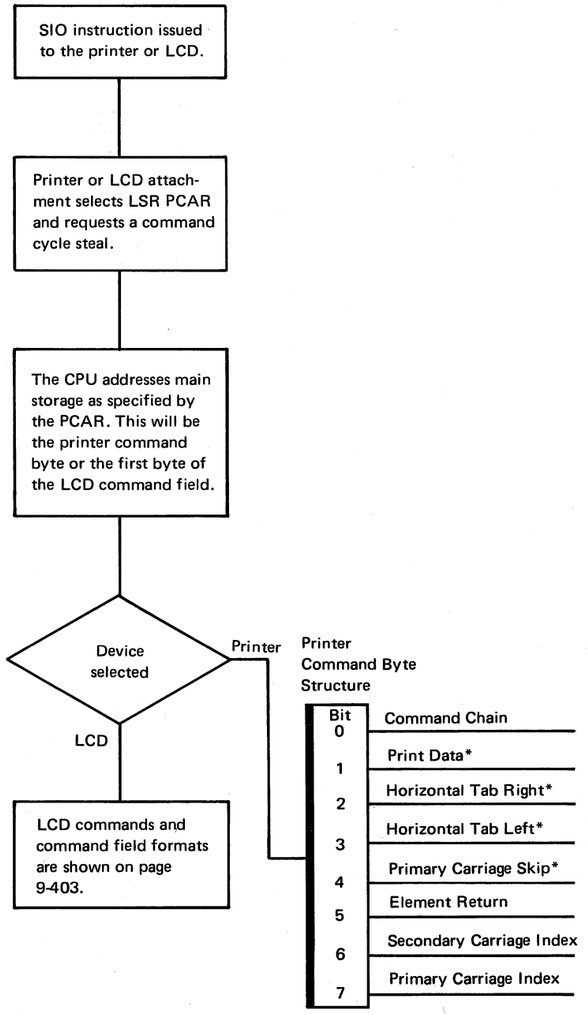
BASIC SIO OPERATION FOR THE PRINTER OR LCD



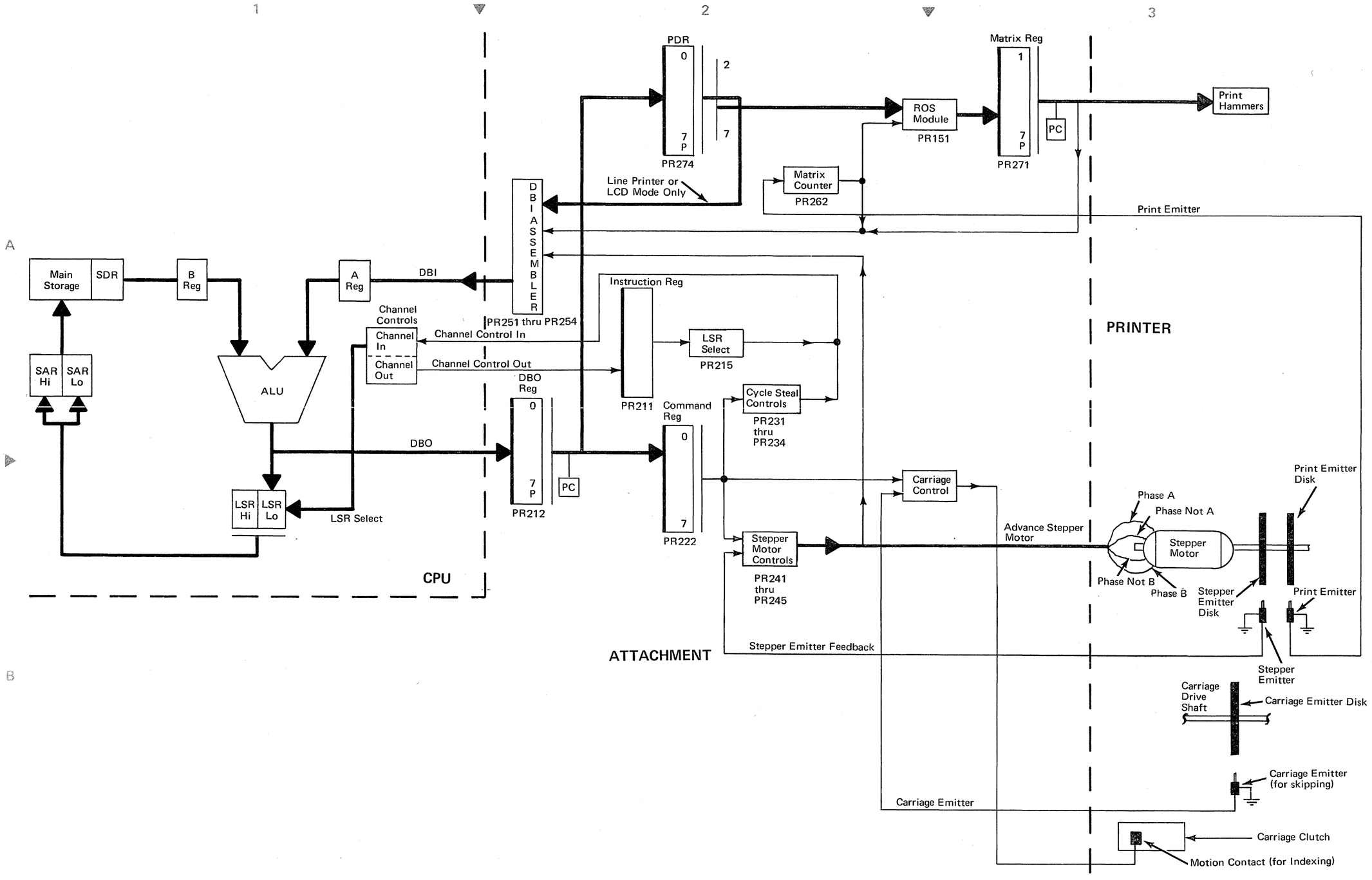
*Requires a count byte if bit is on.

BR2500

Error	Description	Recovery	Notes
Horizontal Cycle Check	A horizontal cycle check will occur if there is no response from the motion contact within 35ms after a horizontal action command was initiated by the attachment (print, tab, or element return commands).	The PCAR is pointing one position beyond the position that failed. If the attachment indicates no other problems, the program may subtract 1 from the PCAR and give a start I/O to retry the same command.	If a horizontal cycle check occurs during a command which had a vertical command included in the same command byte, the vertical command will have been attempted and properly completed, if possible. In this case the recovery routine should involve only the re-issuance of the horizontal command.
Data Check	A data check is a parity check detected by the attachment data register during a cycle steal to obtain a data character. The character in error will not be printed. If the character in error was not the last character to be printed, the next sequential character will also have been spaced over by the time the print element comes to rest.	1. To resume operation at the point where the data check occurred use the following procedure. If machine has bi-directional print feature, issue a sense I/O to determine the status of the print left command. If this bit is off, continue with this recovery procedure. If this bit is on, skip to paragraph 3. The PCAR will be pointing at the byte directly to the right (+1) of the count byte of the command that failed. Issue a sense I/O to the PCAR and retain the address. Subtract 2 from it, and issue a load I/O to load the PCAR with the results. The PCAR is now pointing to the command in which the error occurred. Subtract 1 from the originally stored PCAR address to obtain the count address. Issue a sense I/O status to check the status of the 'count end' bit. If it is off, use a value of (X = 2) in the following procedure. If it is on, use a value of (X = 1). Add (X) to the content of the count byte just determined. Issue a sense I/O to the PDAR. Subtract (X) to determine the address of the character in error. Issue a load I/O to load the PDAR with this address. Reposition the print element to the left (X) print positions. The attachment will attempt to print the same character in the correct position, if a start I/O instruction is issued with bit 7 of the IR byte off. 2. If a complete retry of the print operation is desired, use the following procedure. Enter a programmed halt state. Upon depression of START, the element should be positioned at (software) left margin on the next line and the entire print operation retried. This can be a retry of the entire last chained operation called for by the program, rather than a retry of the last physical print function. 3. Issue a Sense I/O PCAR and retain the address. Subtract two from the address and store the result in the PCAR via a load I/O instruction. This will have repositioned the PCAR to the command in which the error occurred.	

Error	Description	Recovery	Notes
		Then subtract one from the originally stored PCAR address to obtain the count address. Sense I/O status, and check the status of the "count-end" bit. If it is off, use (X=2) in the following procedure and (X=1) if it is on. Add (X) to the content of the count byte just determined. Sense I/O PDAR. Add (X) to determine the address of the character in error. Load I/O PDAR this address. Reposition the print elements to the right (X) print positions. At this time, if a Start I/O instruction with IR bit 7 "on" is given, the attachment will attempt to print the same character in the correct position. If desired, the complete retry procedure given in paragraph 2 may be used.	
Margin Check	The 'margin check' latch is set, and motion is terminated under the following conditions. If the count byte is not zero when the left margin switch is encountered during a horizontal left count command, or if the count byte is not zero when the right margin switch is encountered during a horizontal right command.	The element should be re-oriented to the (software) left margin. If the left margin status bit is not on, an element return command must be given.	1. A margin check will not occur on element return commands. 2. At error detection, the PCAR may be pointing at the next command or at the count byte (see Data Check error recovery).
Sync Check	A sync check can be caused by either of the following conditions. 1. Either less than seven or more than seven horizontal print gate emitter pulses were received from the printer during movement through any character position. 2. The counter keeping track of the stepper motor is not in synchronization with the counter keeping track of the print gate emitter pulses.	A programmed halt state must be entered and the operator may be given the following options: visually check the print out and continue, use a program check point to restart and reprint only the form in error, or restart the complete job. The recovery procedure may also automatically reposition the print element at (software) left margin on the next line and retry the entire last print operation as per Data Check error recovery procedure 1.	1. When a sync check is detected, it is stored in a hardware latch. The attachment corrects itself, and the operation continues until normal count end. A print command which resulted in a sync check would have been properly completed, but possibly one character may not have been properly printed. Sync checks may occur on all horizontal commands except element return. 2. If a sync check occurs on a tab command, the operator should be encouraged to continue as the recorrect function should be successful almost 100% of the time.

Error	Description	Recovery	Notes
ROS Check	A ROS check is a parity check on one of the seven bytes which make up one print character as it is being read out of the ROS module to be printed. Printing is immediately suppressed and the operation is terminated. If the character in error was not the last character to be printed, the next sequential character will also have been spaced over by the time the print element comes to rest.	Same as data check.	It is possible that the first portion of the character was printed and error recovery will continue to overprint this portion. Normally this should not cause any harm, and successful retry will complete the character.
Vertical Cycle Check	A vertical cycle check occurs when no feedback response is received from the printer within 35ms (120ms on pin feed printers) after a vertical action command was initiated by the printer attachment. This includes primary index, primary skip, and secondary index commands.	Same as Horizontal Cycle Check.	1. If a vertical cycle check occurs during a command which had a horizontal command included in the same command byte, the horizontal command will have been attempted and completed properly if possible. In this case the recovery routine should involve only the reissuance of the vertical command. 2. Because either a primary or secondary response will imply carriage motion, it is suggested to issue primary and secondary commands separately.
Invalid Command	An invalid command was issued to the printer attachment. The invalid command will not be executed, the command chain will be broken, and the attachment immediately drops busy.	The contents of the PCAR must be decremented by 1 to point to the command issued. This address should be checked to insure that it is the expected commanded address. If it is, issue another start I/O instruction to retry.	
Data Bus Out Check	A data bus out check is a parity check on data bus out during the compute portion of a CPU cycle which is directly affecting the printer attachment. This includes I-Q, I-R, B cycles, and during printer attachment cycle steals.	None.	The CPU will be forced to a hard halt at the end of the cycle in which the DBO check was detected. The CPU processor check indicator will be turned on.


1
2
3
A
B
PDR
0
7
P
PR274
2
7
ROS Module
PR151
Matrix Reg
1
7
P
PR271
PC
Print Hammers
Matrix Counter
PR262
Line Printer or LCD Mode Only
Print Emitter
D B I A S S E M B L E R
PR251 thru PR254
Main Storage
SDR
B Reg
A Reg
DBI
Instruction Reg
Channel Controls
Channel In
Channel Out
Channel Control In
Channel Control Out
LSR Select
PR215
PR211
SAR Hi
SAR Lo
ALU
DBO Reg
Command Reg
Cycle Steal Controls
PR231 thru PR234
DBO
0
7
P
PR212
PC
0
7
PR222
LSR Hi
LSR Lo
LSR Select
CPU
PRINTER
Print Emitter Disk
Carriage Control
Phase A
Phase Not A
Advance Stepper Motor
Stepper Motor
Phase Not B
Phase B
Stepper Emitter Disk
Print Emitter
Stepper Motor Controls
PR241 thru PR245
Stepper Emitter Feedback
ATTACHMENT
Stepper Emitter
Carriage Drive Shaft
Carriage Emitter Disk
Carriage Emitter (for skipping)
Carriage Emitter
Carriage Clutch
Motion Contact (for Indexing)

Chapter 2. Functional Units

INTRODUCTION TO FUNCTIONAL UNITS

Chapter 2 contains the functional units of the printer attachment and the error checking circuits.

The first page of the chapter is a board layout of the printer attachment. It is broken down into cards and contains the following information:

1. Card locations.
2. Circuits found on that card.
3. ALD page reference numbers that describe the circuits found on the card.
4. Card type number. The part number of the card changes each time that the card has an engineering change to it. The card type number, however, always stays the same.

The card location number appears on each page, or section of a page, that describes the circuitry on that card. For example, N2 on a page refers to the DBI assembler.

Symbols

Figures within this chapter contain the symbols: 1 numbers in squares, and A letters in circles. These symbols refer to text marked with an identical symbol, that describes the function of the unit marked in the figure.

A2	B2 Printer Sense Amplifier Cable ALD Page PR023	C2 Sense Amplifier #1 ALD Page PR131	D2	E2** LCD DBI 1. LCD DBI assembler 2. Read I-O data assembler 3. Pulse width circuits 4. Diagnostic LIO controls 5. Pulse generator circuits 6. Sense cells	F2** Cycle Steal 1. Cycle steal controls 2. Count end 3. LSR select 4. Channel in controls 5. Test I/O	G2** Commands 1. Command controls 2. Busy 3. Drive latch 4. Manual eject 5. Invalid command check 6. Error checks a. Sense cell b. Alignment c. I-O check d. Unit e. Drive f. Print mark g. Read back 7. Switch latches a. Card gate b. Card in switch c. Card out switch d. Card aligned e. Card edge switch f. Edge of card g. Last line h. Index to last	H2** Last Line 1. Document end condition 2. LSR and cycle steal 3. Document end steal ALD Pages PR841 and PR842 Card Type 6883	J2	K2 Horizontal High Speed 1. High speed interlocks 2. Double shift controls ALD Pages PR821 and PR822 Card Type 3381	L2 Line Printing 1. Bi-directional feature ALD Pages PR411 and PR412 Card Type 3379	M2 Matrix Controls 1. ROS matrix 2. ROS latch output 3. Parity checking 4. Character set quartering 5. Print data register 6. Print matrix	N2 DBI 1. DBI assembler 2. Predrivers a. Print hammers b. Stepper motor	P2 Stepper Motor 1. Stepper motor controls 2. Printer controls 3. Stepper motor shift and speed controls	Q2 SS1 SS3 SSA SSZ ALD Pages PR111 and PR112 Card Type 3368	R2 Cycle Steal 1. Cycle steal controls 2. LSR controls 3. Counter advance 4. Fire SS1 5. Fire SS2 6. Fire SS3 7. Fire SSA 8. Clock pulses 9. Count end controls	S2 Commands 1. Command register 2. Error checking a. Sync check b. Margin check c. Margin halt d. I/O check e. Unit check f. Data check g. ROS check 3. Cycle checking a. Horizontal b. Vertical 4. Magnet gates a. Primary motion contact b. Secondary motion contact c. Print drivers	T2 Initial Selection 1. Channel instruction register 2. DBO register 3. DBO decode 4. LSR selection 5. DBI gating 6. Diagnostic LIO controls 7. Condition register	U2 Pin Feed Carriage SS1 ALD Page PR123 Card Type 3376	V2 Miscellaneous Channel #1
A3	B3** LCD Sense Amplifier Cable ALD Page PR025	C3 Sense Amplifier #2 ALD Page PR132	D3					J3											U3 Zener Power Supply for ROS	V3 DBI Channel #2
A4 Meter and Tape Cable ALD Page PR041	B4 Diagnostic Tape Input Card ALD Page PR141	C4 Sense Amplifier #3 ALD Page PR133	D4** LCD SS 1. Skip line SS1 2. Skip line SS2 3. Hold busy 4. Card alignment ALD Pages PR711 and PR712 Card Type 3366				H4	J4	K4	L4 ROS Matrix Module ALD Page PR151 Card Type 7737									U4 Clock Channel #3 (Terminator)	V4 Clock Channel #3
A5 Driver Cable ALD Page PR022	B5 Integrator Cable ALD Page PR021	C5 22 Inch Printer 1. Motion contacts 2. LCD interface ALD Page PR641 Card Type 3382	D5** LCD SS 1. Stop 2. Drive busy ALD Pages PR721 and PR722 Card Type 3377	Card Type 3385	ALD Pages PR821 thru PR825 Card Type 3384	ALD Pages PR811 thru PR815 Card Type 3383	H5	J5	K5	L5	ALD Pages PR271 thru PR275 Card Type 3375	ALD Pages PR251 thru PR256 Card Type 3370	ALD Pages PR241 thru PR245 Card Type 3374	ALD Pages PR261 and PR262 Card Type 3369	ALD Pages PR231 thru PR234 Card Type 3373	ALD Pages PR221 thru PR224 Card Type 3372	ALD Pages PR211 thru PR216 Card Type 3371	U5 DBO Channel #4 (Terminator)	V5 DBO Channel #4

**Card locations for ledger card device.

Printer Attachment Board A2 on Gate A (A-A2) (Card Side)

PRINTER SINGLE SHOTS

Single Shot One (SS1)

- SS1 is active for a duration of 35 ms.
- It is used to check for mechanical motion (both horizontal and vertical).

SS1 is fired during each command cycle steal. Within 35 ms after it has fired, an electrical pulse must be received from the printer. If no pulse is received from the printer, a horizontal or vertical (depending upon the command) check occurs.

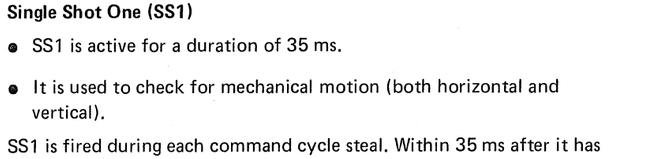
Horizontal Cycle Check

The 'horiz cy inlk' latch is set during the command cycle steal for every horizontal command. At the same time, SS1 is fired. Before SS1 times out (35 ms), the printer must activate the line '+6V right integrated emitter' to reset the 'horiz cy inlk' latch. If this latch is not reset before SS1 times out, a horizontal cycle check occurs.

Vertical Cycle Check

The 'vert cy inlk' latch is set during the command cycle steal for every vertical command. At the same time, SS1 is fired. Before SS1 times out (35 ms), the printer must activate either 'SP prim motion contact' (for a vertical index command to the primary carriage) or 'SP sec motion contact' (for a vertical index command to the secondary carriage) to reset the 'vert cy inlk' latch. If a skip command is issued, a primary vertical emitter signal must be received before SS1 times out. If the 'vert cy inlk' latch is not reset before SS1 times out, a vertical cycle check occurs.

If commands are given simultaneously to both the primary and secondary carriages, only one of them can reset the 'vert cy inlk' latch. Both carriages have motion contacts, but there is only one interlock latch. Therefore, if both carriages receive vertical commands simultaneously, only one of them is checked for motion.

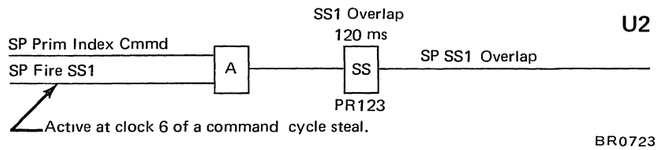


Single Shot One—Overlap (SS1 Overlap)

- SS1 overlap is active for a duration of 120 ms.
- It is used on printers with pin feed platens.
- It is fired at the same time as SS1, and has the same function as SS1.

The SS1 overlap single shot is used only on printers with pin feed platens. The mechanical action in these printers is slower and therefore more time is required to respond to electrical signals. SS1 overlap is fired at the same time as SS1. The result is a 120 ms duration pulse (instead of a 35 ms pulse) to give the printer more time to respond.

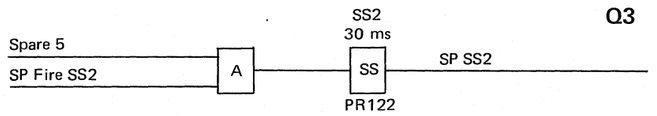
SS1 overlap checks for horizontal and vertical cycle checks the same way as SS1 does. Refer to "Single Shot One (SS1)" for a description of how it checks for cycle checks.



Single Shot Two (SS2)

- SS2 is active for a duration of 30 ms.
- It is fired at the end of each command to allow for mechanical settling down of the printer.

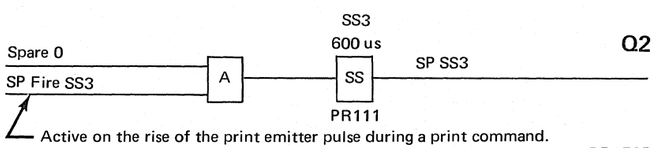
SS2 is fired at the end of every horizontal and vertical command to allow for mechanical settling down of the mechanics in the printer. It cannot be fired until SS1 has timed out.



Single Shot Three (SS3)

- SS3 is active for a duration of 600 μs.
- SS3 is used to gate the print drivers that fire the print hammers.

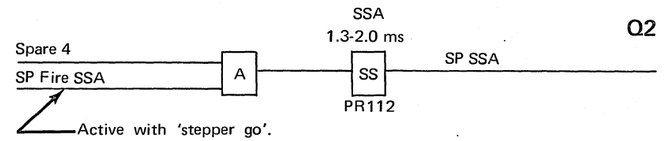
SS3 is print time. It gates the print drivers to fire the print hammers. It is fired seven times per character.



Single Shot A (SSA)

- SSA is active for a duration of 1.3 to 2.0 ms.
- It starts mechanical motion of the stepper motor by providing the first advance pulse to it.

SSA is used to start the stepper motor. It provides the first advance pulse to it.

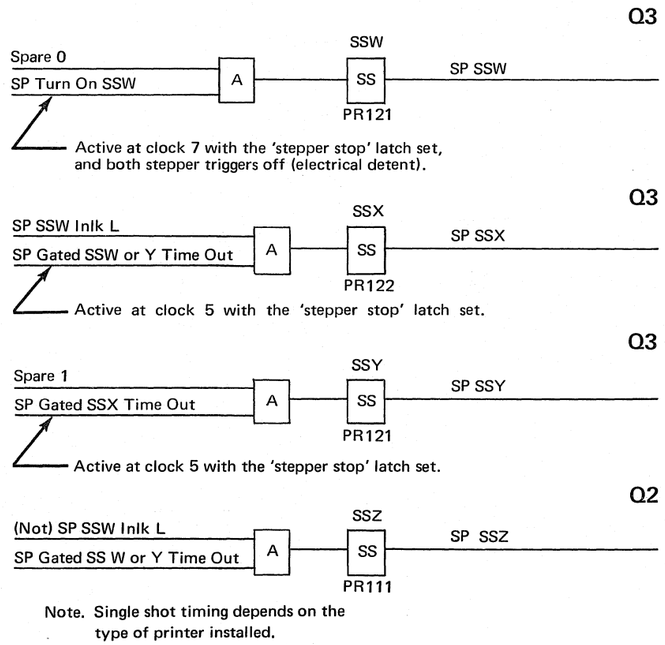


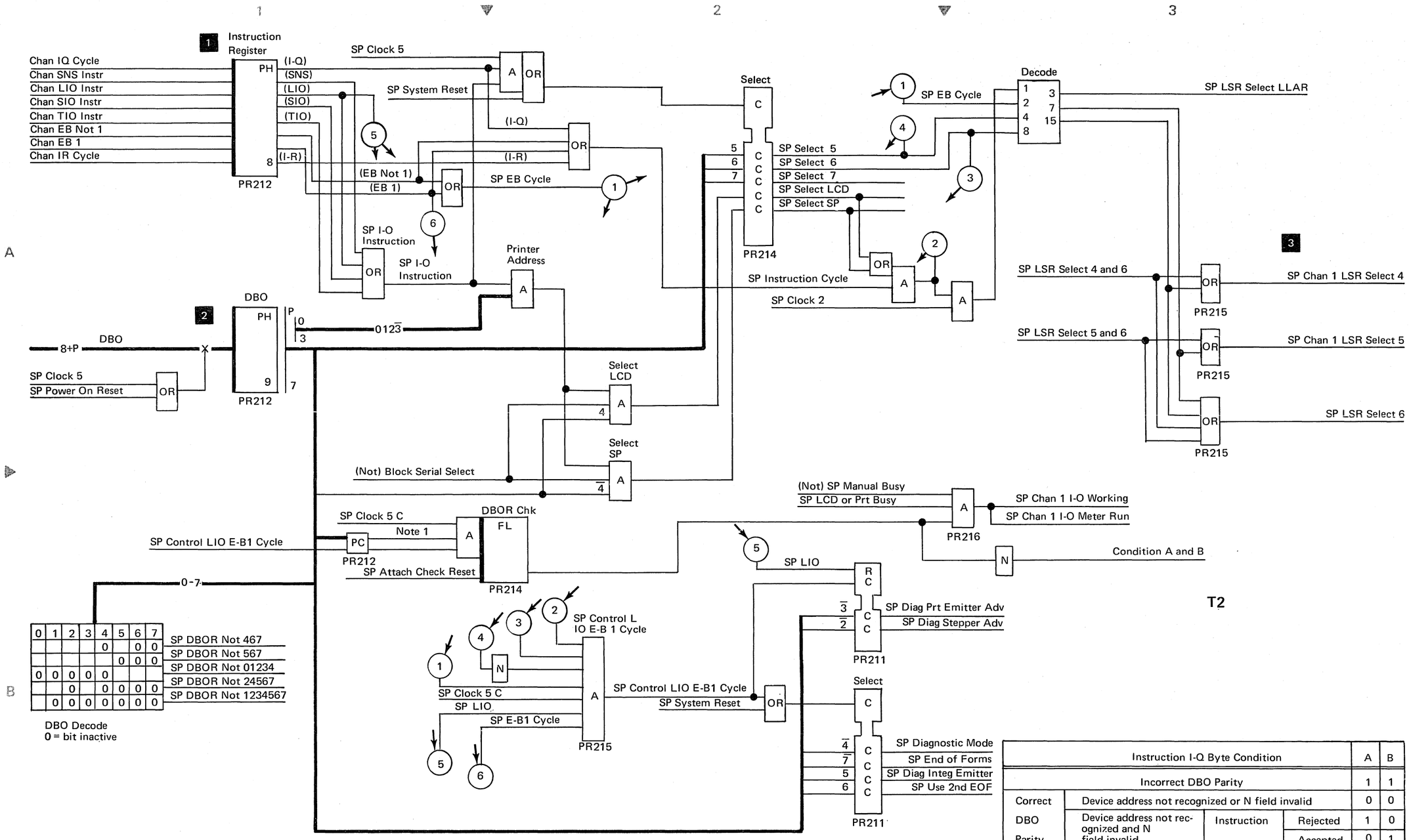
Single Shot W (SSW), Single Shot X (SSX), Single Shot Y (SSY), and Single Shot Z (SSZ)

- Settings dependent on the type of printer installed.
- These single shots are used to stop the stepper motor.

	5213 Printer	2222 Printer
SSW is active for a duration of	1.3 ms	1.45 ms
SSX is active for a duration of	1.6 ms	1.45 ms
SSY is active for a duration of	2.2 ms	2.1 ms
SSZ is active for a duration of	4.0 ms	2.8 ms

These four single shots are the stop single shots. They supply the last four advance pulses to the stepper motor. They are fired in sequence (SSW, SSX, SSY, and SSZ). Each one has a longer duration time than the one previously fired. As a result the stepper motor slows down and stops.





Note 1. The 'DBOR ck' latch can be set during one of the following times:
1. at clock 5 of the I-Q cycle during and I-O instruction, or
2. during cycle stealing with 'SP steal cycle' active.

Instruction I-Q Byte Condition				A	B
Incorrect DBO Parity				1	1
Correct DBO Parity	Device address not recognized or N field invalid			0	0
	Device address not recognized and N field invalid.	Instruction	Rejected	1	0
			Accepted	0	1
I-R Byte, and I-O Cycle Condition	Incorrect DBO Parity			1	1
	Correct DBO Parity			0	0

1 INSTRUCTION REGISTER

- The instruction register consists of eight polarity hold latches.
- Latches set determine the instruction and the cycle to be taken by the attachment.
- Latches have active outputs when their inputs are inactive.

The four instruction lines (SIO, LIO, TIO, and SNS) indicate the presence of an instruction in the CPU register. If the printer attachment decodes its device address and a condition code acceptable to the instruction latch set, the instruction will be performed in the cycle that is called for by the instruction register.

2 DATA BUS OUT (DBO) REGISTER

- The data bus out register consists of nine polarity hold latches, eight for data and one for parity.
- All data from the CPU enters the attachment through the DBO register and sets the appropriate latches.
- Latches have active outputs if their inputs are inactive (except for the 5 bit latch which is also used for cycle steal priority.

Eight data bits and one parity bit are transferred to the printer attachment from the CPU by the data bus out (DBO) lines. These data bits are sent to the DBO parity check circuits and to the DBO latches.

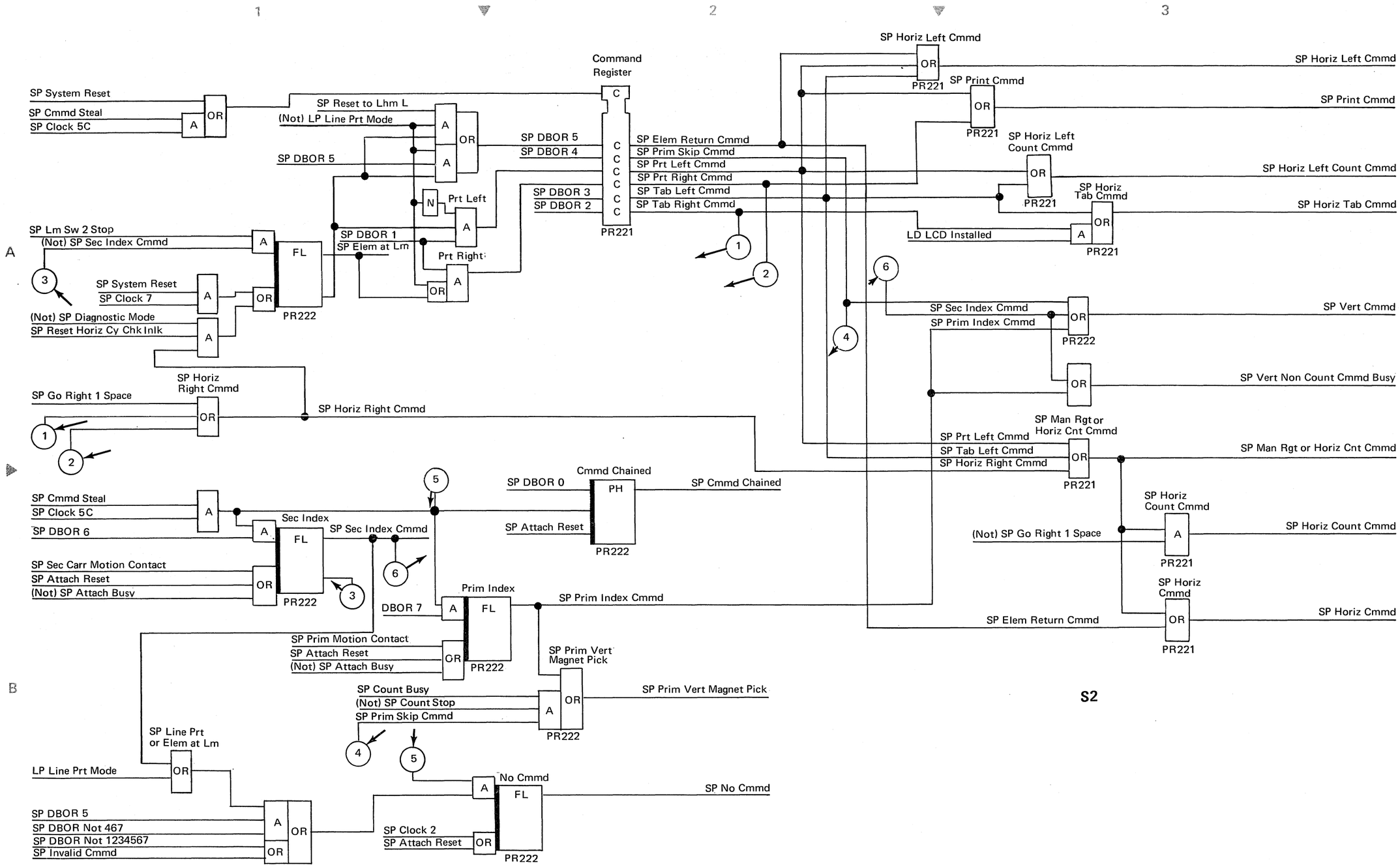
The parity check circuits check each data byte sent to the attachment for odd parity.

Data sent over to the DBO lines is set into the DBO register at CPU clock 5 time. At the next CPU clock 5 time, new data is set into the registers or the registers are reset.

3 LOCAL STORAGE REGISTER (LSR) SELECT

- Local storage register select selects printer attachment LSR's (located in the CPU) to obtain print and carriage information, and to modify the LSR's.
- LSR select lines 4 and 6 select the print command address register (PCAR).
- LSR select lines 5 and 6 select the print data address register (PDAR).
- LSR select lines 3 and 6 select the locate line address register.

The LSR select circuitry is used to select the appropriate LSR to obtain print data, a command or a count. After obtaining this data, the LSR is reselected for updating.


1
2
3
A
B
SP System Reset
SP Cmmd Steal
SP Clock 5C
OR
A
SP Reset to Lhm L
(Not) LP Line Prt Mode
SP DBOR 5
Command Register
C
SP DBOR 5
SP DBOR 4
SP DBOR 3
SP DBOR 2
SP Elem Return Cmmd
SP Prim Skip Cmmd
SP Prt Left Cmmd
SP Prt Right Cmmd
SP Tab Left Cmmd
SP Tab Right Cmmd
PR221
N
Prt Left
Prt Right
SP Lm Sw 2 Stop
(Not) SP Sec Index Cmmd
SP DBOR 1
SP Elem at Lm
FL
PR222
SP System Reset
SP Clock 7
(Not) SP Diagnostic Mode
SP Reset Horiz Cy Chk Inlk
SP Horiz Right Cmmd
SP Go Right 1 Space
SP Horiz Left Cmmd
SP Print Cmmd
SP Horiz Left Count Cmmd
SP Horiz Tab Cmmd
LD LCD Installed
SP Sec Index Cmmd
SP Prim Index Cmmd
SP Vert Cmmd
SP Vert Non Count Cmmd Busy
SP Man Rgt or Horiz Cnt Cmmd
SP Prt Left Cmmd
SP Tab Left Cmmd
SP Horiz Right Cmmd
SP Horiz Count Cmmd
(Not) SP Go Right 1 Space
SP Horiz Cmmd
SP Elem Return Cmmd
Cmmd Chained
SP DBOR 0
PH
SP Cmmd Chained
SP Attach Reset
SP Cmmd Steal
SP Clock 5C
SP DBOR 6
Sec Index
SP Sec Index Cmmd
SP Sec Carr Motion Contact
SP Attach Reset
(Not) SP Attach Busy
Prim Index
DBOR 7
SP Prim Motion Contact
SP Attach Reset
(Not) SP Attach Busy
SP Prim Vert Magnet Pick
SP Count Busy
(Not) SP Count Stop
SP Prim Skip Cmmd
SP Line Prt or Elem at Lm
LP Line Prt Mode
SP DBOR 5
SP DBOR Not 467
SP DBOR Not 1234567
SP Invalid Cmmd
No Cmmd
SP No Cmmd
SP Clock 2
SP Attach Reset
S2

Data Bus In (DBI) Assembler

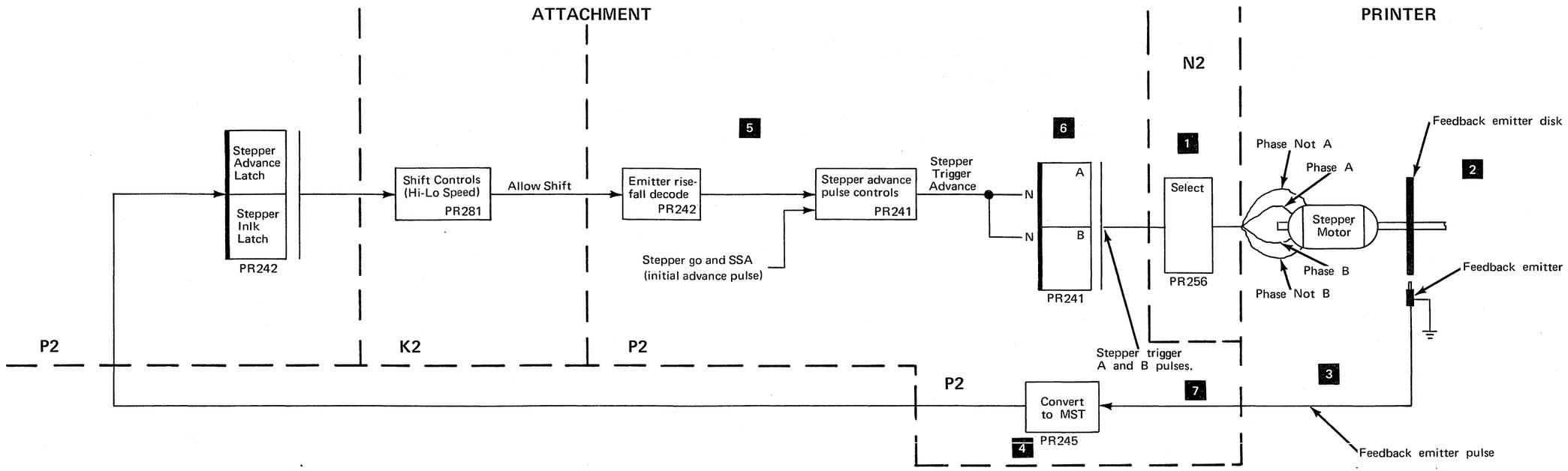
- The DBI assembler consists of nine latches and a decode circuit.
- It separates all data to be sent to the CPU on DBI into data bits.

All data from the attachment that is to be sent to the CPU is assembled in the DBI assembler and gated out during E-B cycles (with the exception of the force P bits).

N2

SP Gate 1	SP Gate 2	SP Gate 3	SP Gate 4	SP Gate 5	LD Status 3 PR831	LD Status 1 PR831	LD Status 2 PR831	PR021	
SP Horiz Cycle Check	SP Count End	Secondary Carriage EOF	SP SSA	5213 Printer attached	LD Skip Line SS1	LD Sense Amp Check L	LD Sense Amp 1	SP Force DBI Bit 0	Ch Data Bus In 0 / PR252
SP Data Check	SP Prt Left Cmmd	SP Matrix Output 1	SP SS3	Not Vertical Forms Control	LD Skip Line SS2	LD Card Skew Check L	LD Sense Amp 2	SP Force DBI Bit 1	Ch Data Bus In 1 / PR252
SP Margin Check	SP Matrix Counter Trigger 1	SP Matrix Output 2	SP Stepper Tr A	Not Bi-directional Printer Feature	LD Late Mark L	LD Drive Check L	LD Sense Amp 3	SP Force DBI Bit 2	Ch Data Bus In 2 / PR252
SP Sync Check	SP Matrix Counter Trigger 2	SP Matrix Output 3	SP Stepper Tr B	SP Secondary EOF	LD Special Tip-off	LD Read Mark Check L	LD Sense Amp 4	SP Force DBI Bit 3	Ch Data Bus In 3 / PR253
SP ROS Check	SP Matrix Counter Trigger 4	SP Matrix Output 4	SP SSZ	Not SP Lm Sw 2 Stop and Not Rm Sw 1 Slow	LD Card Alignment SS	LD Line Finder Mark Check L	LD Timing Pulse	SP Force DBI Bit 4	Ch Data Bus In 4 / PR253
SP Vert Cycle Check	Printer Ready	SP Matrix Output 5	SP SSY	SP Rm Sw 2 Stop or SP Lm Sw 1 Slow	Spare	LD Invalid Cmmd Check	LD Drive Check SS	SP Force DBI Bit 5	Ch Data Bus In 5 / PR253
SP Primary EOF	SP SS2	SP Matrix Output 6	SP SSX	SP Primary or Secondary Motion Contact	Spare	LD Card In Switch On	LD Activate LCD Feed Clutch	SP Force DBI Bit 6	Ch Data Bus In 6 / PR254
SP Invalid Command	SP SS1	SP Matrix Output 7	SP SSW	SP Vert Emit Adv	LD Stop SS	LD Card In Switch On	LD Hold Busy SS	SP Force DBI Bit 7	Ch Data Bus In 7 / PR254
								SP Force DBI Bit P	Ch DBI Bit P / PR251

E-B1 Cycle									
E-B Not 1 Cycle									
M Code 4									
N Code 5									
N Code 6									
N Code 7									

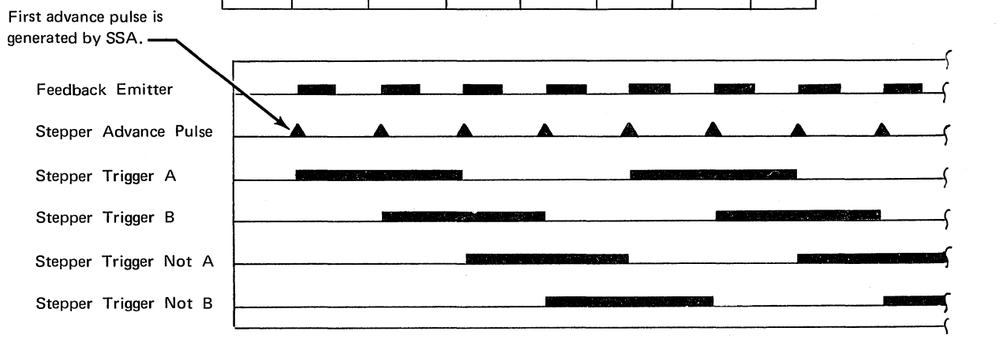


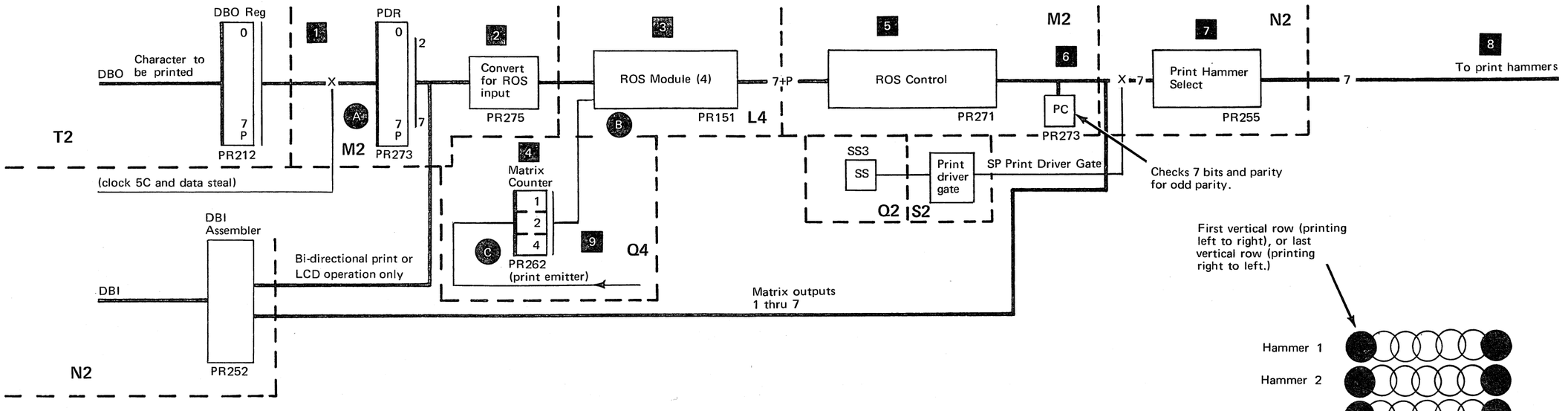
STEPPER MOTOR OPERATION

The stepper motor controls the horizontal movement of the print element during printing, tab operations, and element return.

1. Advance pulse to motor causes rotor to move.
2. Emitter wheel mounted on rotor shaft rotates past the feedback emitter.
3. Emitter pulse generated by feedback emitter returns to the attachment.
4. Attachment circuitry converts the emitter pulse to MST.
5. This pulse is decoded by the attachment circuitry to generate an advance pulse to the stepper triggers.
6. The stepper triggers generate another advance pulse to the stepper motor.
7. Another feedback emitter pulse is generated and the cycle is repeated.

Motor Advance Pulse Sequence (Forward)				Motor Advance Pulse Sequence (Reverse)				
Phase A	Phase Not A	Phase B	Phase Not B	Phase A	Phase Not A	Phase B	Phase Not B	
OFF	ON	OFF	ON	OFF	ON	OFF	ON	→ Electrical detent
ON	OFF	OFF	ON	OFF	ON	ON	OFF	
ON	OFF	ON	OFF	ON	OFF	ON	OFF	
OFF	ON	ON	OFF	ON	OFF	OFF	ON	
OFF	ON	OFF	ON	OFF	ON	OFF	ON	→ Electrical detent





BASIC PRINT OPERATION

1. During a data cycle steal, the character to be printed is brought over from main storage and placed in the DBO register. At clock 5C time the character is gated into the print data register (PDR).

2. The contents of bit positions 2 through 7 of the PDR are converted to ROS inputs. These inputs remain active at the ROS module until the character is printed (for 7 print emitter pulses).

3. The ROS module converts the active input lines into the character to be printed.

4. The matrix counter advances to a count of one upon receiving the first print emitter pulse.

5. The matrix trigger one being on, gates the first of seven outputs per character from the ROS module to the ROS control. Since the character is printed on a seven by seven matrix, the ROS module is gated seven times by the matrix counter (advanced by the seven print emitter pulses).

6. The output of the ROS control is checked for the correct ROS parity (odd).

7. The print hammer select determines which hammers are to be fired in print position one (for the first vertical row of the character) and sends pulses to the printer to energize the selected print magnets.

8. The selected hammers are fired and another print emitter pulse is sent to the matrix counter.

9. The matrix counter advances to two and gates the ROS module. This operation continues until all seven print emitter pulses have been received and the print hammers have fired seven times to complete the character.

A PRINT DATA REGISTER (PDR)

- Consists of nine flip latches, eight for the data character and one for parity.
- Retains the data character during printing.

During the data cycle steal the character to be printed is stored in the PDR. The two through seven positions are used to determine the ROS character to be printed. The data character is held in the PDR until the character is printed and is replaced with the next character to be printed during the next data cycle steal.

B READ ONLY STORAGE (ROS) MODULE

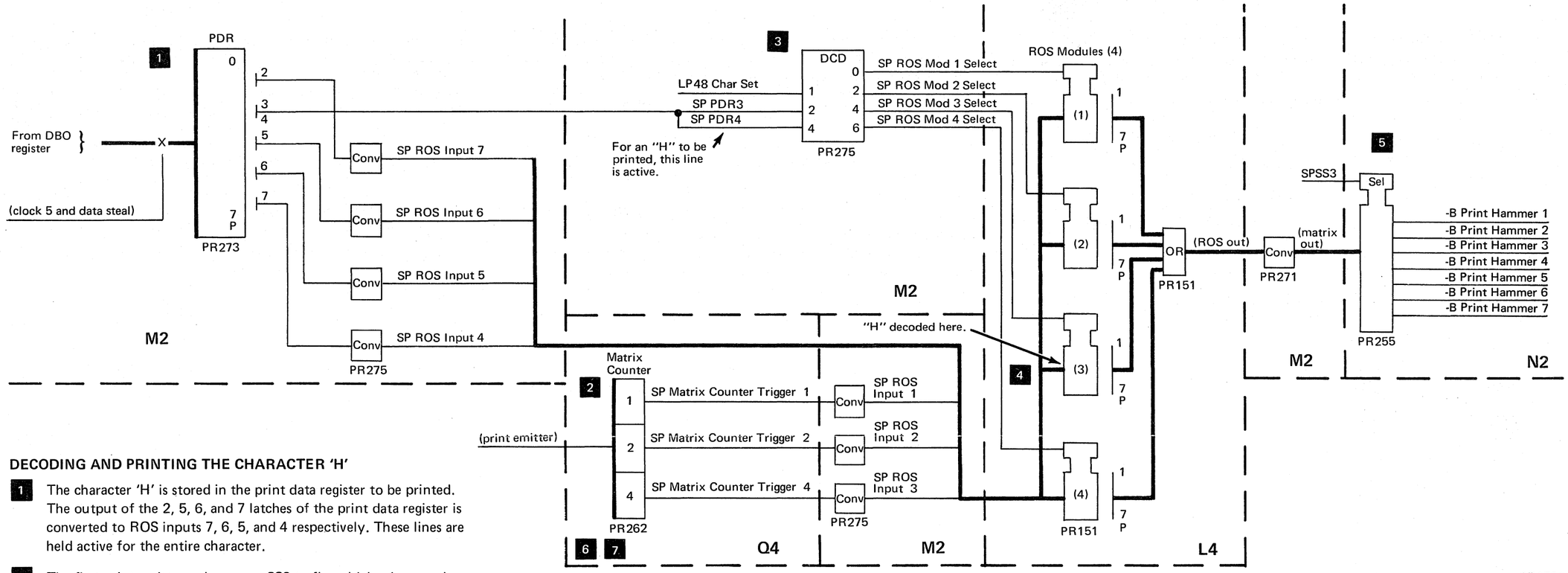
- Consists of four modules.
- Translates the output of the PDR into the character to be printed.

The ROS module translates the output of the PDR into a printable character. The ROS module has an active output seven times per character (gated by the matrix counter), once for each vertical row of the seven by seven matrix that forms the character.

C MATRIX COUNTER

- Consists of three flip-flop triggers.
- Is advanced by the print emitter.
- Binarily counts to seven to gate the ROS module.
- Resets to zero after counting to seven.

The matrix counter counts the print emitter pulses (seven per character) and gates the ROS module seven times per character. The seven matrix counter pulses must fall within the time that the integrated emitter is active. If not, a sync check occurs.



BR0730

DECODING AND PRINTING THE CHARACTER 'H'

1 The character 'H' is stored in the print data register to be printed. The output of the 2, 5, 6, and 7 latches of the print data register is converted to ROS inputs 7, 6, 5, and 4 respectively. These lines are held active for the entire character.

2 The first print emitter pulse causes SS3 to fire which advances the matrix counter to one. With matrix counter one active, 'SP ROS input 1' is activated.

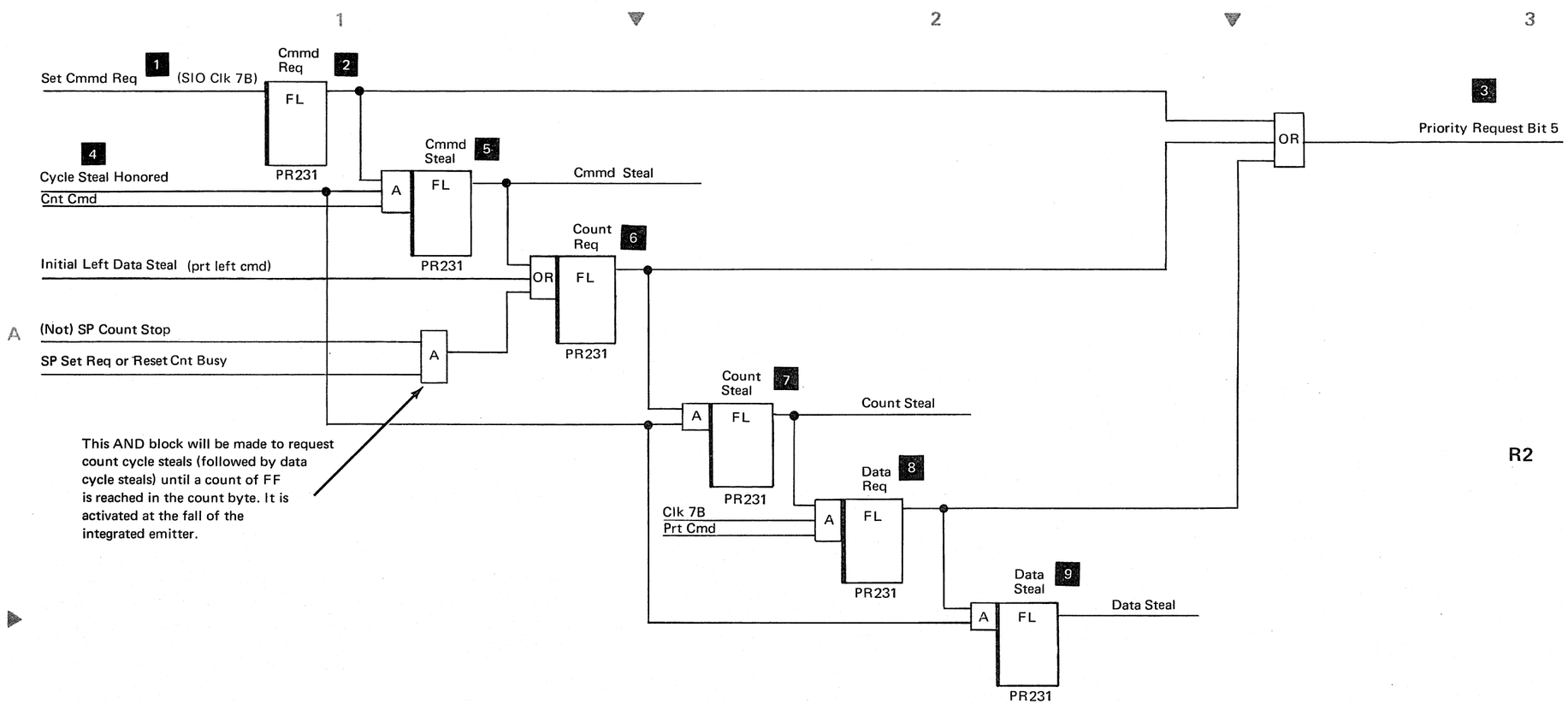
3 The decode for an 'H' is stored in the third ROS module. Therefore, print data register latch 4 is active and decodes to select the third ROS module by activating 'SP ROS mod 3 select'. This ROS module stays selected for the entire character.

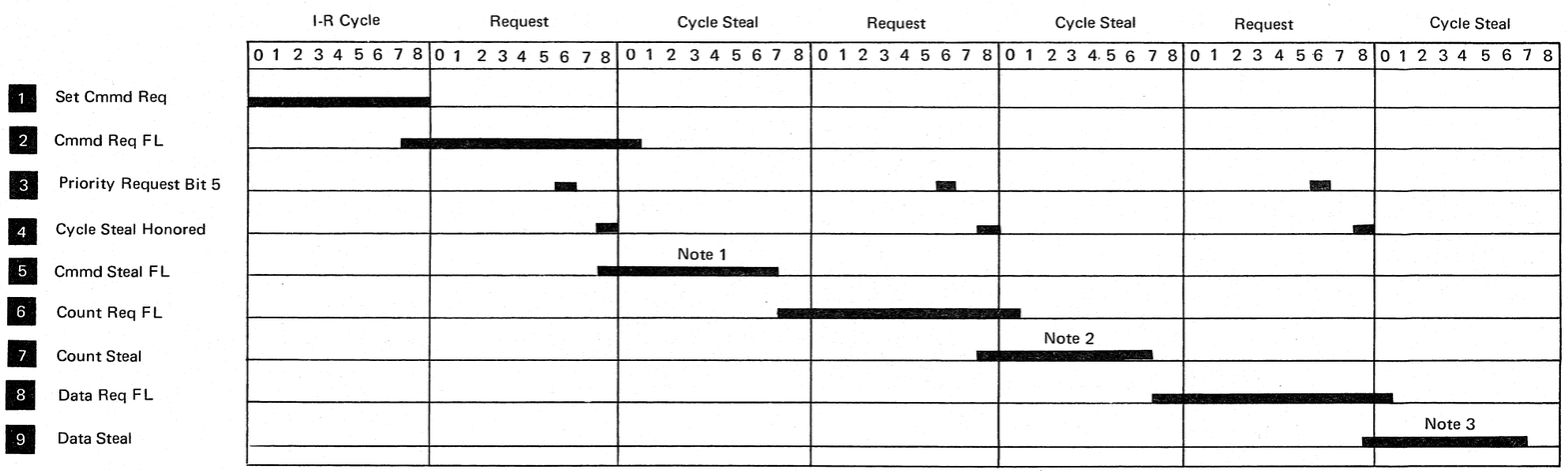
4 The ROS module decodes the first vertical row of the character 'H' to be printed, and selects all of the print hammers.

5 All of the hammers fire at SS3 for 600 μs, and the first vertical row of the character is printed. SS3 was actually fired prior to the time that the matrix counter was stepped to one, but the hammers could not respond at this time.

6 The second print emitter pulse causes SS3 to fire again. The matrix counter advances to two, and the second vertical row of the character is decoded in the ROS module. This time no hammers are selected.

7 This procedure is repeated until the matrix counter has advanced to a count of seven, and all vertical rows of the character have been printed. After the seventh print emitter pulse, the integrated emitter falls and a count cycle is requested unless the attachment has reached 'count end'.





Note 1: Take cycle steal to get command from PCAR.

Note 2: If required, take a cycle steal to get count from PCAR.

Note 3: Take cycle steal to get print data from PDAR.

Note 4: Commands with count bytes require only one command cycle steal. After the first command, count, and data cycle steals; the sequence is count and data cycle steals until count end is reached.

Horizontal Cycle Check

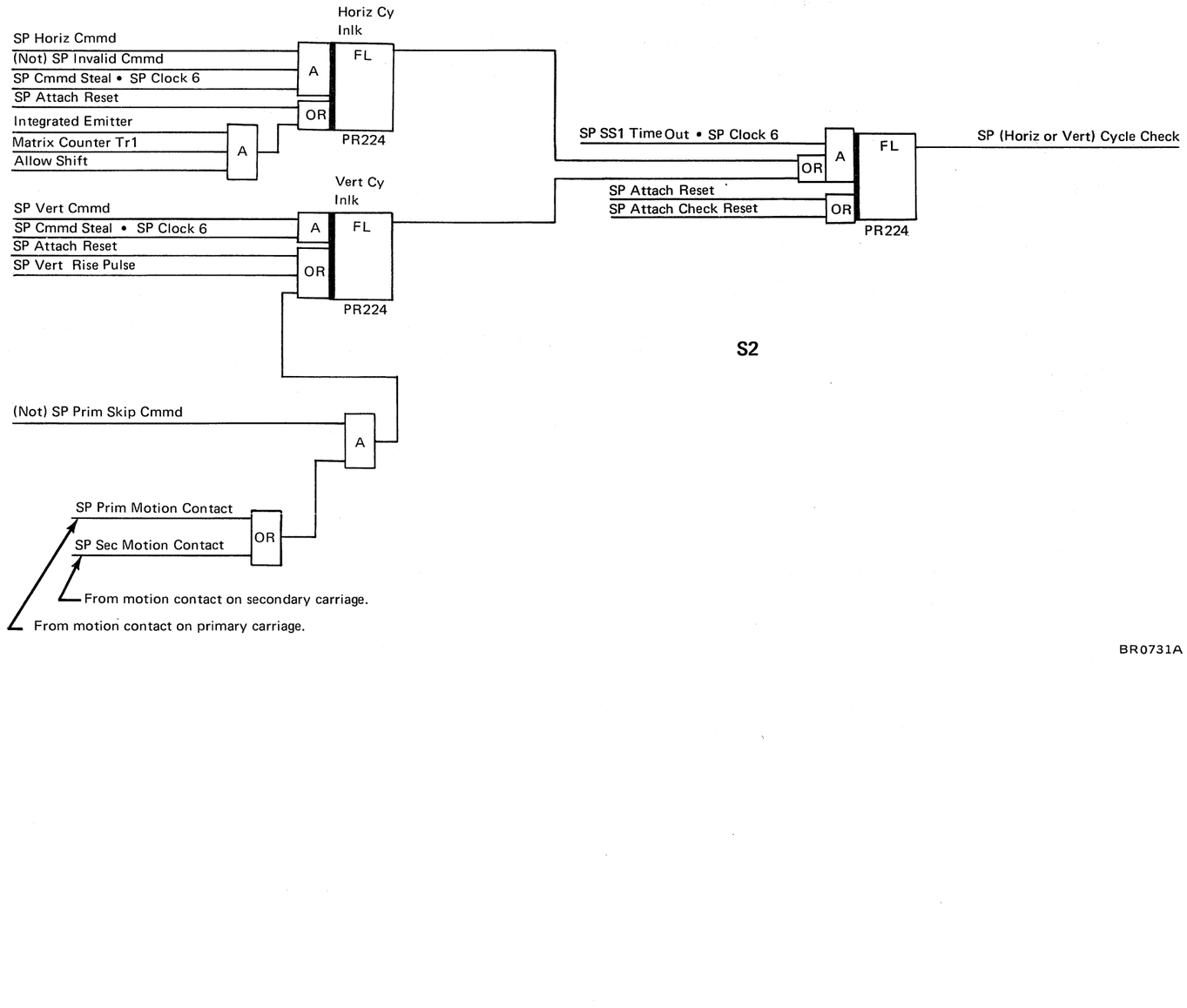
A horizontal cycle check occurs when a horizontal command (print, tab, or element return) is given to the printer and no feedback response is received from the printer within 35 ms (SS1 time out). The check for this condition is as follows:

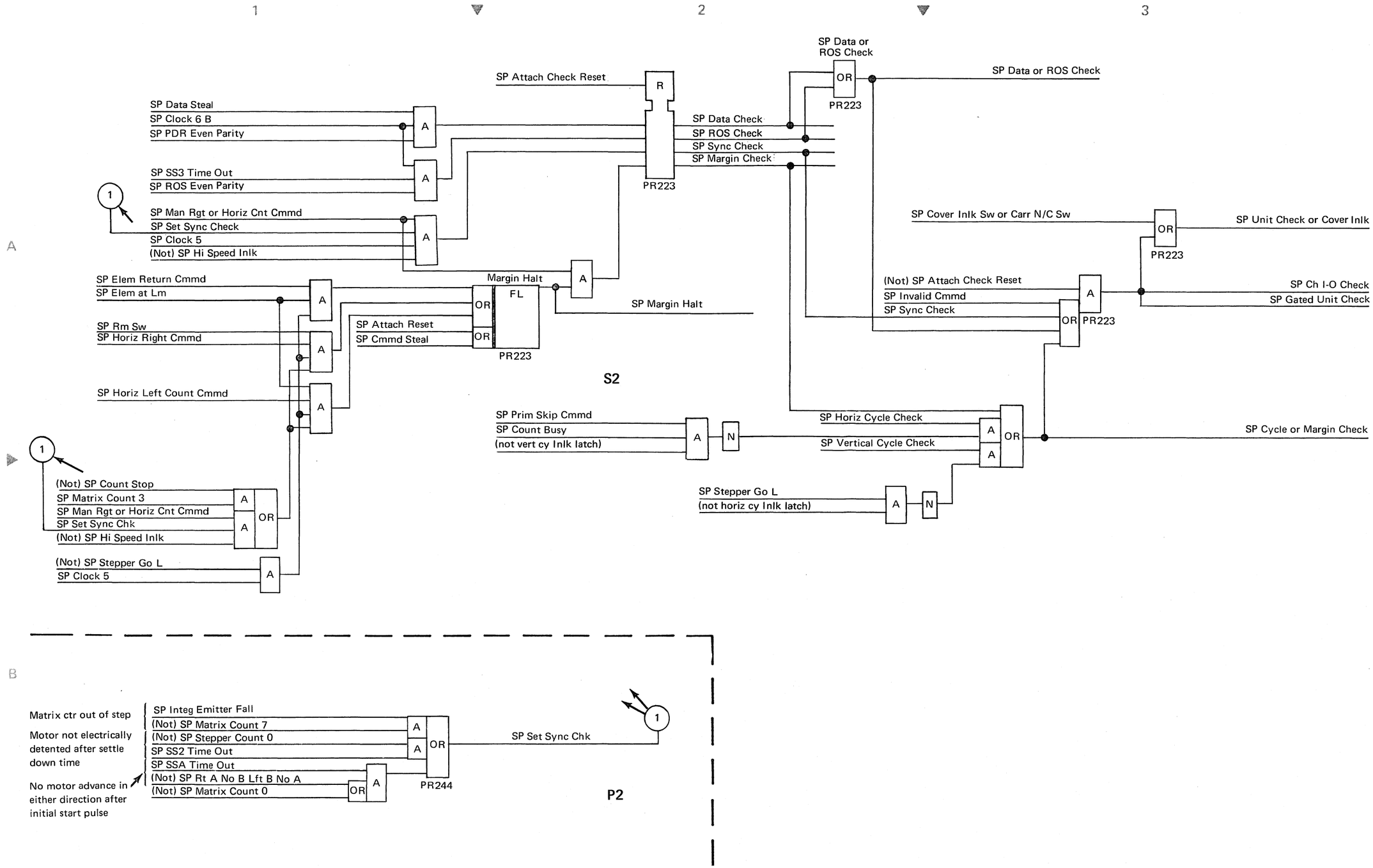
- A horizontal command is given.
- SS1 is fired (it is active for 35 ms).
- The 'horiz cy inlk' latch is set.
- The printer should activate 'matrix counter tr1' indicating that mechanical motion has taken place.
- 'Matrix counter tr1' activates 'SP reset horiz cy chk inlk' to reset the 'horiz cy inlk' latch.
- If the response ('matrix counter tr1') is not received within 35 ms, SS1 times out and the 'horiz cy inlk' latch remains set causing a horizontal cycle check.

Vertical Cycle Check

A vertical cycle check occurs when a vertical command (primary index, secondary index, or skip) is given to the printer and no feedback response is received from the printer within 35 ms (SS1 time out). For printers with pin feed platens, a response time of 120 ms is allowed for primary index commands. This is because these printers have a slower mechanical response time. The procedure for checking for vertical cycle checks is as follows:

- A vertical command is given.
- SS1 is fired (it is active for 35 ms). If the command is a primary index command for a pin feed platen printer, SS1 overlap also is fired (it is active for 120 ms).
- The 'vert cy inlk' latch is set.
- The printer should respond with a motion contact pulse. The response to a command to a primary carriage activates 'SP prim motion contact'. The response to a command to a secondary carriage activates 'SP sec motion contact'. These lines active indicate that mechanical motion has taken place.
- Either of these lines active resets the 'vert cy inlk' latch. On a skip command, the carriage emitter pulse resets the 'vert cy inlk' latch.
- If these responses are not received within 35 ms (120 ms for pin feed platen printers), the 'vert cy inlk' latch does not reset and a vertical cycle check occurs.




1
2
3
A
B
SP Attach Check Reset
R
PR223
SP Data Steal
SP Clock 6 B
SP PDR Even Parity
SP SS3 Time Out
SP ROS Even Parity
SP Man Rgt or Horiz Cnt Cmmd
SP Set Sync Check
SP Clock 5
(Not) SP Hi Speed Inlk
A
SP Data Check
SP ROS Check
SP Sync Check
SP Margin Check
SP Data or ROS Check
OR
PR223
SP Data or ROS Check
SP Cover Inlk Sw or Carr N/C Sw
OR
PR223
SP Unit Check or Cover Inlk
(Not) SP Attach Check Reset
SP Invalid Cmmd
SP Sync Check
A
OR
PR223
SP Ch I-O Check
SP Gated Unit Check
Margin Halt
FL
PR223
SP Margin Halt
SP Elem Return Cmmd
SP Elem at Lm
SP Rm Sw
SP Horiz Right Cmmd
SP Horiz Left Count Cmmd
SP Attach Reset
SP Cmmd Steal
OR
S2
SP Prim Skip Cmmd
SP Count Busy
(not vert cy Inlk latch)
N
SP Horiz Cycle Check
SP Vertical Cycle Check
SP Cycle or Margin Check
SP Stepper Go L
(not horiz cy Inlk latch)
(Not) SP Count Stop
SP Matrix Count 3
SP Man Rgt or Horiz Cnt Cmmd
SP Set Sync Chk
(Not) SP Hi Speed Inlk
(Not) SP Stepper Go L
SP Clock 5
Matrix ctr out of step
Motor not electrically detented after settle down time
No motor advance in either direction after initial start pulse
SP Integ Emitter Fall
(Not) SP Matrix Count 7
(Not) SP Stepper Count 0
SP SS2 Time Out
SP SSA Time Out
(Not) SP Rt A No B Lft B No A
(Not) SP Matrix Count 0
PR244
SP Set Sync Chk
P2

Chapter 3. Operations

INTRODUCTION TO OPERATIONS

Chapter 3 contains detailed flowcharts and timing charts of the operations performed by the printer attachment.

Flowcharts

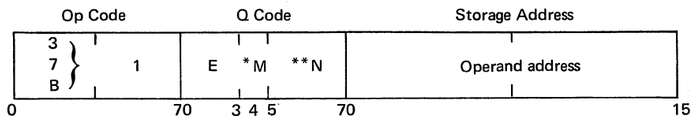
The flowcharts contain three levels of information. By reading down the heavy dark lines, the reader can learn the major objectives of the operation. The second level of information is obtained by reading the information in the boxes that branch off the heavy dark line. The information that is contained in each block in a heavy dark line is explained in the blocks that branch off from it.

The third level of information is contained in the note blocks (open ended blocks) that branch off the second level blocks. Information in these blocks is intended to explain why an action has been performed.

Timing Charts

The timing charts in this chapter are to be used to supplement the information found in the flowcharts.

1



* M bit is 0 unless the LCD device is installed and the load I/O is for the LCD.

** = Bits tested for by the attachment.

A

Load I/O Instruction

31, 71, or B1 decoded during a CPU I-Op cycle indicates a load I/O.

PR011

'Ch LIO instruction' is activated in the attachment.

I-Op Cycle

1. Sample Q code for device address.
2. Determine and notify CPU of condition code.

PR211

Activate 'SP I-O instruction'.

PR213

If DA is E (1110), activate 'SP DBOR 012 not 3'.

PR214

At 'SP clock 5' set the 'select SP' latch.

If M bit is 0, set 'select SP' latch.
If M bit is 1, set 'select LCD' latch.

PR216

Determine the condition code and activate 'Ch 1 I-O condition A' and/or 'Ch 1 I-O condition B'.

I-Q Cycle

B

1

2

1

Before taking the B cycle(s):

1. Condition code B (except for a control load I/O) must be sent to the CPU. If not, an I-R back-up is performed. That is, the I-Op and I-Q cycles will be repeated until a condition code of B is decoded and sent back to the CPU.
2. The CPU will (depending upon the Op code) take either: an I-X1 cycle, or an I-H1 cycle and an I-L1 cycle.

Take B cycle (s) to:

1. Perform a control load function, or
2. Select the PCAR, or
3. Select the PDAR, or
4. Select the LLAR.

E-B Cycles

N code 01X (control code LIO)

Yes

PR215

At 'SP clock 5C' activate 'SP control LIO E-B1 cycle'.

No

N code 10X (load PDAR LIO)

Yes

PR211

Activate 'SP E-B cycle' for two B cycles. Once by activating 'Ch E-B 1 cycle' and next 'Ch E-B not 1 cycle'.

PR215

During the B cycles, the 'Ch LSR select 5' and 'Ch LSR select 6' lines are active. During the first B cycle, the PDAR lo order byte is addressed; during the second B cycle, the hi order byte is addressed.

No

3

2

Load I/O I-Q Byte Condition				I/O Condition A	I/O Condition B
Incorrect DBO Parity				1	1
Correct DBO Parity	Device address not recognized or N field invalid.			0	0
	Device address recognized and N field valid.	LIO	Rejected	1	0
			Accepted	0	1
Load I/O E-B Cycles	Incorrect DBO Parity			1	1
	Correct DBO Parity			0	0

2

3

N code 11X (load PCAR LIO)

Yes

PR211

Activate 'SP E-B cycle' for two B cycles. First by activating 'Ch E-B 1 cycle' then 'Ch E-B not 1 cycle'.

PR215

During the B cycles, the 'Ch LSR select 4' and 'Ch LSR select 6' are activated. During the first B cycle the PCAR lo order byte is addressed; during the second B cycle the hi order byte is addressed.

No

2

N code 00X (load LLAR LIO)

Yes

PR211

Activate 'SP E-B cycle' for two B cycles. First by activating 'Ch E-B 1 cycle' then 'Ch E-B not 1 cycle'.

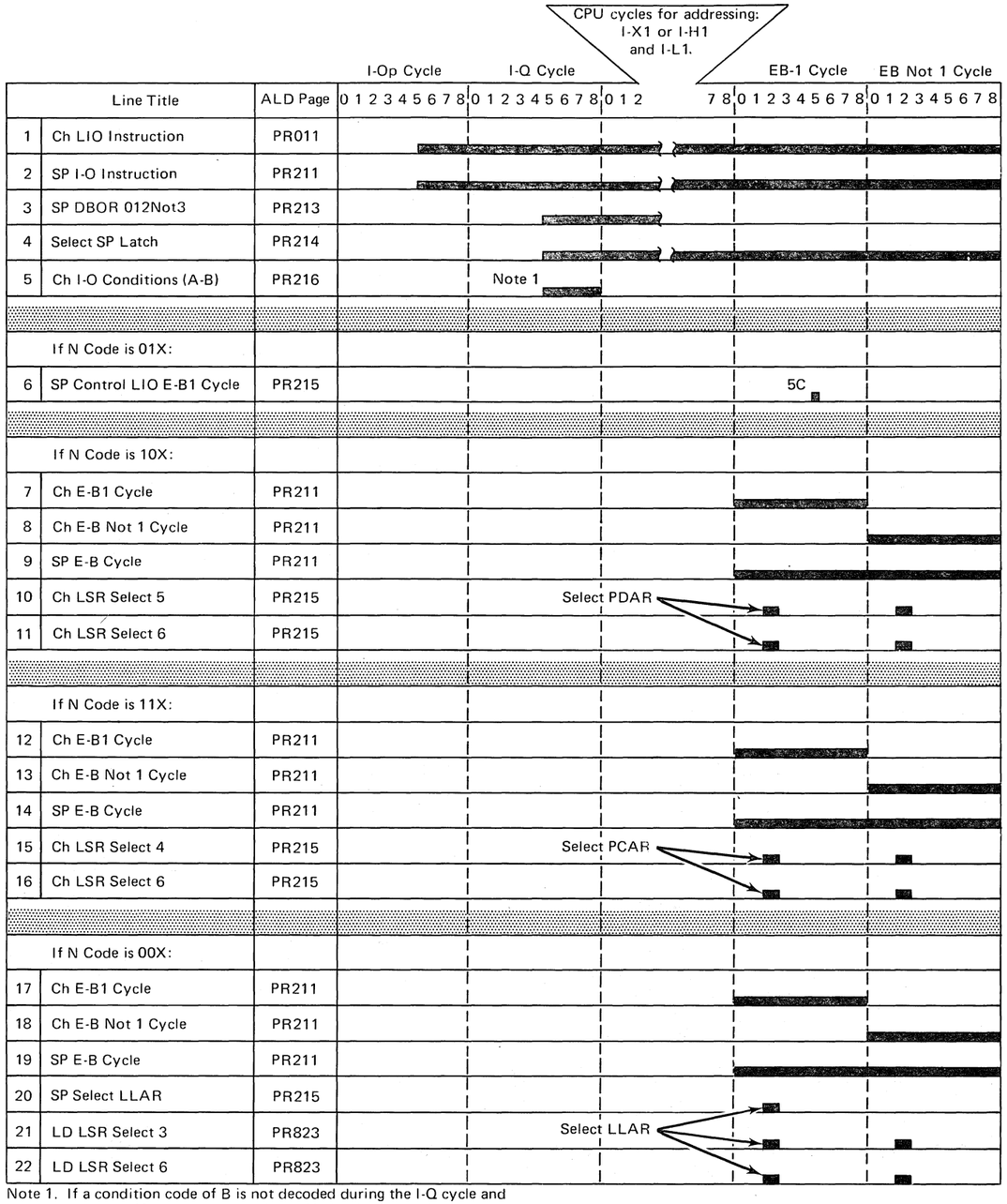
PR215

During the B cycles the 'SP LSR select LLAR' line is activated. During the first B cycle the LLAR lo order byte is addressed. During the second B cycle the Hi order byte is addressed.

No

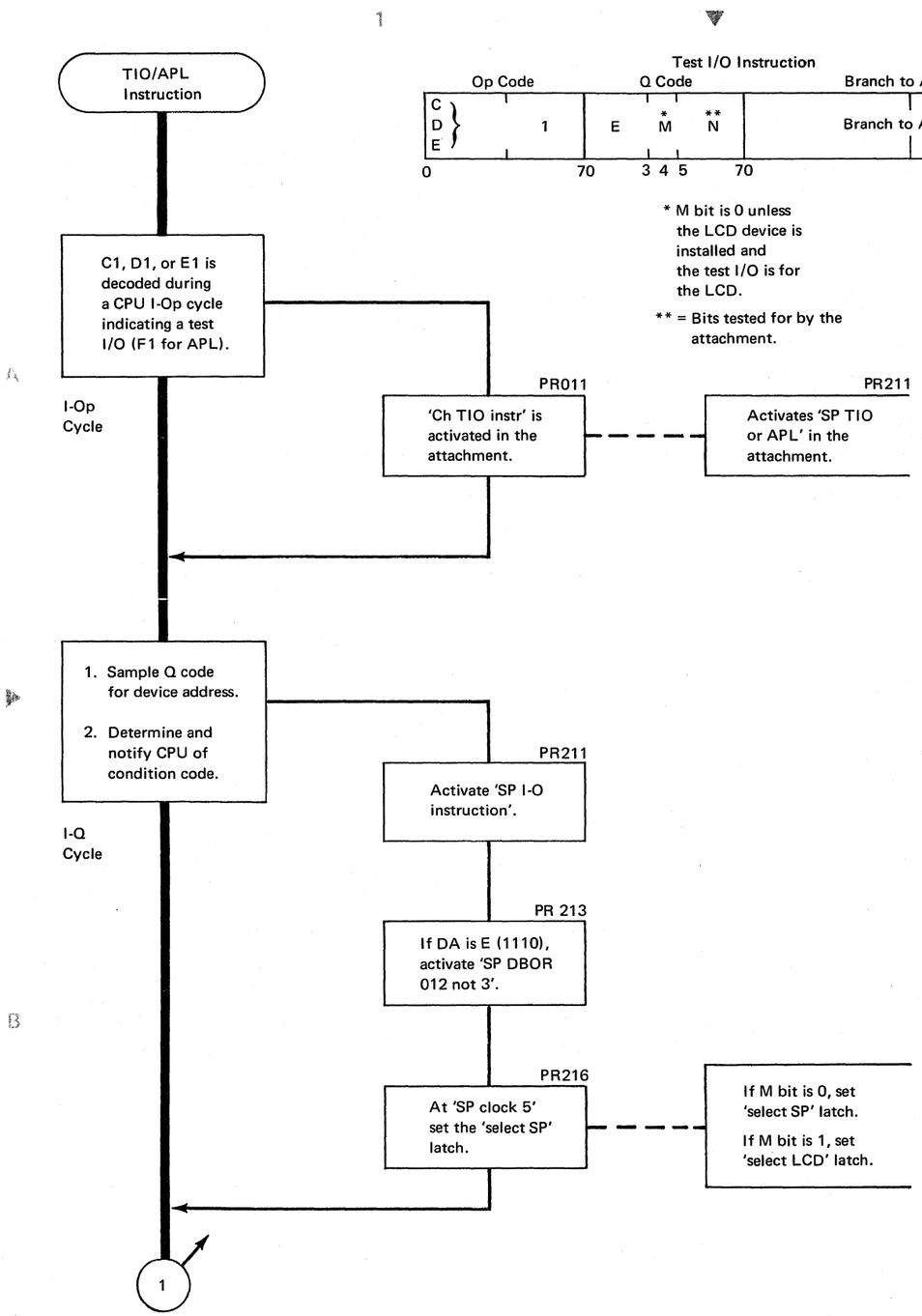
Any other N code is invalid. A processor check stop would occur and the processor check light would come on.

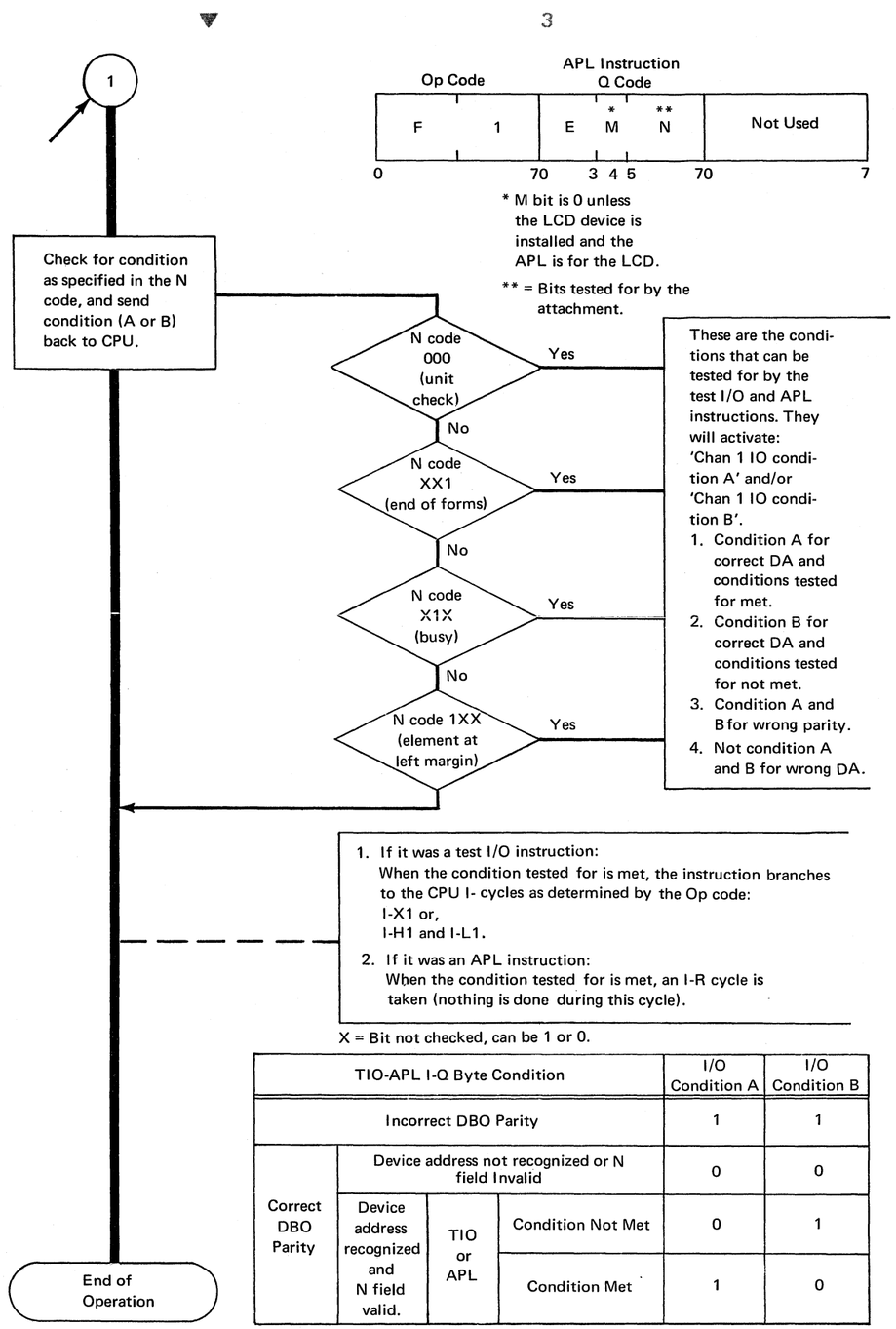
End of Operation



	Line Title	ALD Page
1	Ch LIO Instruction	PR011
2	SP I-O Instruction	PR211
3	SP DBOR 012Not3	PR213
4	Select SP Latch	PR214
5	Ch I-O Conditions (A-B)	PR216
	If N Code is 01X:	
6	SP Control LIO E-B1 Cycle	PR215
	If N Code is 10X:	
7	Ch E-B1 Cycle	PR211
8	Ch E-B Not 1 Cycle	PR211
9	SP E-B Cycle	PR211
10	Ch LSR Select 5	PR215
11	Ch LSR Select 6	PR215
	If N Code is 11X:	
12	Ch E-B1 Cycle	PR211
13	Ch E-B Not 1 Cycle	PR211
14	SP E-B Cycle	PR211
15	Ch LSR Select 4	PR215
16	Ch LSR Select 6	PR215
	If N Code is 00X:	
17	Ch E-B1 Cycle	PR211
18	Ch E-B Not 1 Cycle	PR211
19	SP E-B Cycle	PR211
20	SP Select LLAR	PR215
21	LD LSR Select 3	PR823
22	LD LSR Select 6	PR823

Note 1. If a condition code of B is not decoded during the I-Q cycle and the load I/O is not a control load I/O, I-R back up takes place.

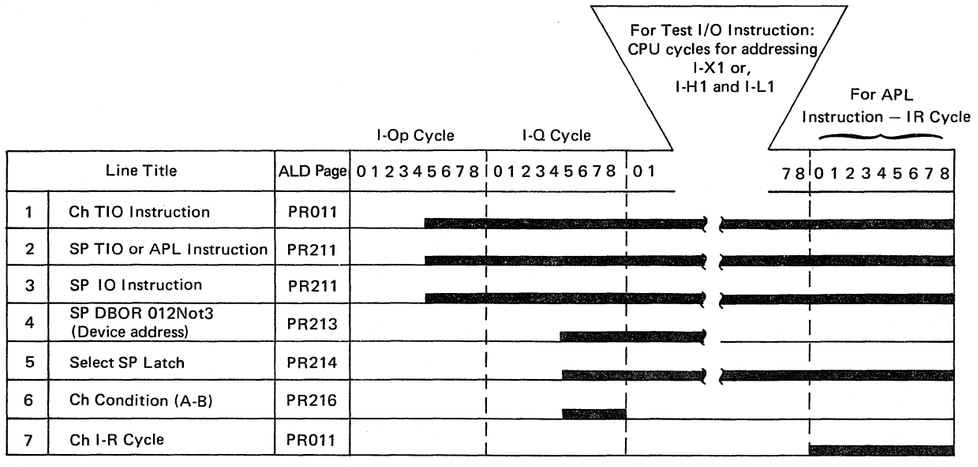




X = Bit not checked, can be 1 or 0.

TIO-APL I-Q Byte Condition				I/O Condition A	I/O Condition B
Incorrect DBO Parity				1	1
Correct DBO Parity	Device address not recognized or N field Invalid			0	0
	Device address recognized and N field valid.	TIO or APL	Condition Not Met	0	1
			Condition Met	1	0

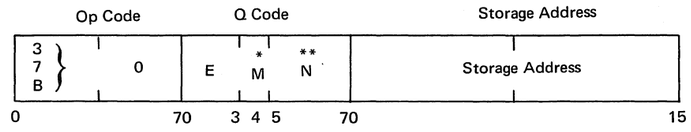
A



	Line Title	ALD Page
1	Ch TIO Instruction	PR011
2	SP TIO or APL Instruction	PR211
3	SP IO Instruction	PR211
4	SP DBOR 012Not3 (Device address)	PR213
5	Select SP Latch	PR214
6	Ch Condition (A-B)	PR216
7	Ch I-R Cycle	PR011

B

1 2 3



*M bit is 0 unless the LCD device is installed and the sense instruction is for the LCD.

** = Bits tested for by the attachment.

M	N	1st B Cycle (Lo Order Byte)	2nd B Cycle (Hi Order Byte)
0		Store Status 1	Store Status 2
0		FE Diagnostic Aid Status 3	FE Diagnostic Aid Status 4
X		Store PDAR LO	Store PDAR Hi
X		Store PCAR LO	Store PCAR Hi
X		Store LLAR LO	Store LLAR Hi
1		Store Status	Store Diagnostic Byte
1	—	LCD Signals	Printer Device Signals

X = Bit not checked.

A

Sense Instruction

30, 70, or B0 decoded by CPU during an I-Op cycle indicates a sense instruction.

PR011

'Ch SNS instr' is activated in the attachment.

I-Op Cycle

1. Sample Q code for device address.
2. Raise 'Ch I-O condition B'.

PR211

Activate 'SP I-O instruction'.

I-Q Cycle

PR213

If DA is E (1110), activate 'SP DBOR 012 not 3'.

PR214

At 'SP clock 5' set the 'select SP' latch.

If M bit is 0, set 'select SP' latch. If M bit is 1, set 'select LCD' latch.

PR216

Activate 'Ch I-O condition B'.

B

1

Before taking the B cycle(s):

The CPU will (depending upon the Op code) take either: an I-X1 cycle or an I-H1 cycle and an I-L1 cycle.

Take E-B1 cycle. Decode M and N codes to determine what the sense instruction is for, and send sense information back to CPU on DBI.

E-B1 Cycle

PR211

Activate 'SP E-B1 cycle'.

PR215

Activate 'SP gate status 1 or 3'.

'SP select 7' active

Yes

No

PR251

Activate 'SP gate 1'.

PR251

Activate 'SP gate 3'.

These lines will gate the sense information (as specified by the M and N codes - see above) in the DBI assembler.

Take E-B not 1 cycle. Decode M and N codes to determine what the sense instruction is for, and send sense information back to CPU on DBI.

E-B Not 1 Cycle

PR211

Activate 'SP E-B not 1 cycle'.

2

3

PR215

Activate 'SP gate status 2 or 4'.

'SP select 7' active

Yes

No

PR251

Activate 'SP gate 2'.

PR251

Activate 'SP gate 4'.

These lines will gate the sense information (as specified by the M and N codes - see above) in the DBI assembler.

End of Operation

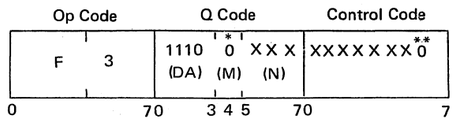
A

CPU cycles for addressing:
I-X1, or I-H1 and I-L1.

	Line Title	ALD Page	I-Op Cycle 0 1 2 3 4 5 6 7 8	I-Q Cycle 0 1 2 3 4 5 6 7 8	0 1	EB-1 Cycle 7 8	0 1 2 3 4 5 6 7 8	EB Not 1 Cycle 0 1 2 3 4 5 6 7 8
1	Ch SNS Instruction	PR011						
2	SP I-O Instruction	PR211						
3	SP DBOR 012Not3	PR213						
4	Select SP Latch	PR214						
5	SP E-B1 Cycle	PR211						
6	SP Gate Status 1 or 3	PR215						
7	SP E-B Not 1 Cycle	PR211						
8	SP Gate Status 2 or 4	PR215						

B

1 2 3



*M Bit is 0 unless the LCD device is installed and the start I/0 is for the LCD

** 0 for Serial Print
1 for Bi-directional print

x=Bit not checked, can be either 1 or 0.

A

Start I/O Instruction

F3 is decoded during a CPU I-Op cycle indicating a start I/O .

PR011
'Ch SIO instr' is activated in the attachment.

I-Op Cycle

1. Sample Q code for device address.
2. Determine and notify CPU of condition code.

PR211
Activate 'SP I-O instruction'.

PR213
If DA is E (1110), activate 'SP DBOR 012 not 3'.

PR214
At 'SP clock 5' set the 'select SP' latch.

If M bit is 0, set 'select SP' latch. If M bit is 1, set 'select LCD' latch.

PR216
Determine condition code and activate 'Ch I-0 condition A' and/or 'Ch I-0 condition B'.

I-Q Cycle

1

B

1

Before taking the I-R cycle a condition code of B must be decoded during the I-Q cycle and sent to the CPU. If condition code B is not decoded, I-R back up will occur; that is I-Op I-Q, and I-R cycles will be taken until a condition code of B is decoded and sent to the CPU.

1. Examine control code. If Bit 7 is 0, it will be a serial print operation. If Bit 7 is a 1, it will be a bi-directional operation.
2. Request a cycle steal.

I-R Cycle

PR214
Activate 'SP selected SIO I-R cycle'.

If a 1 is detected in Bit 7, at 'SP clock 5C' the 'line prt mode' latch is set.

PR261
Activate 'SP set command request'.

PR231
Set the 'Cmd req' latch at 'SP clock 7B'.

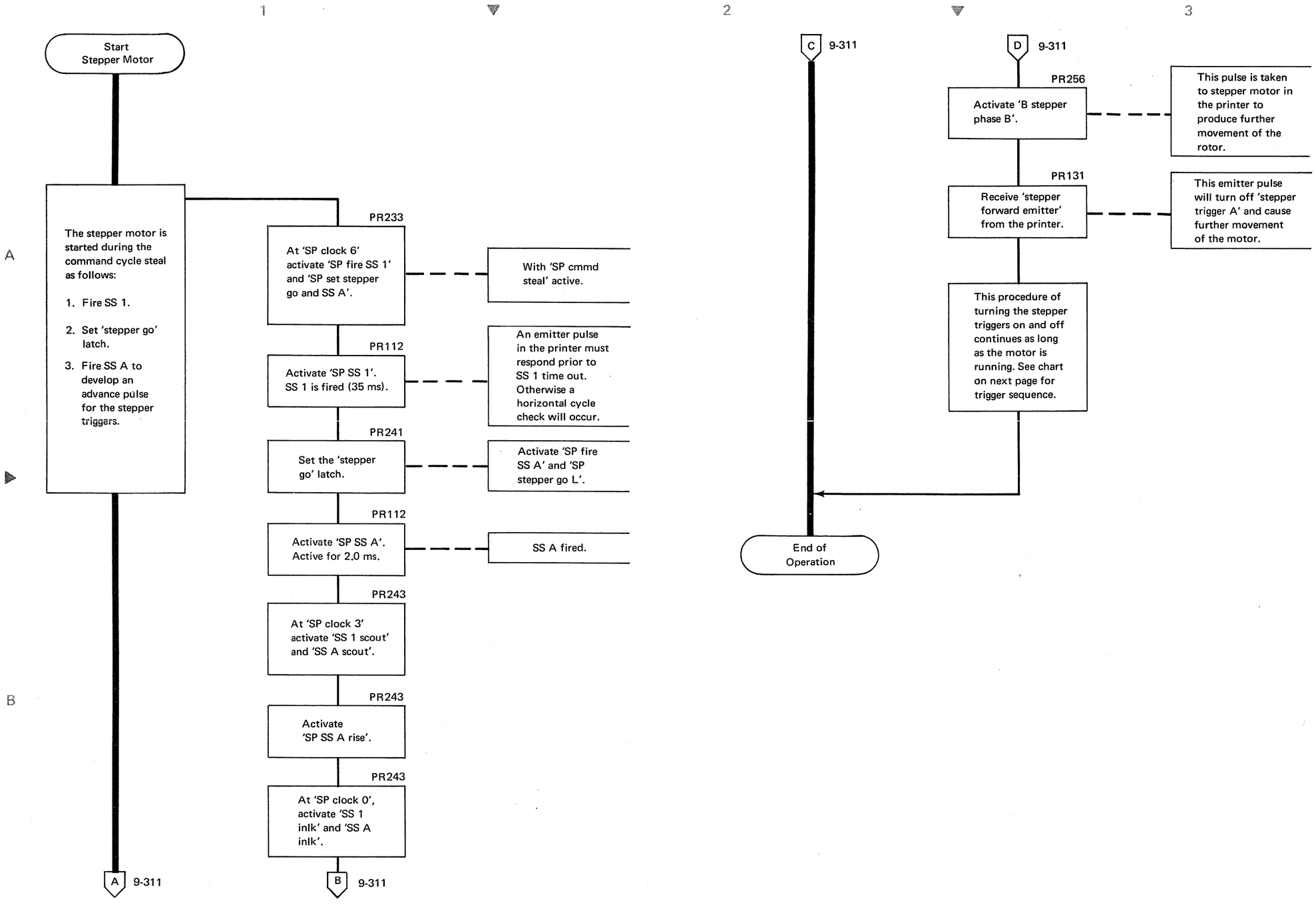
PR231
At 'SP clock 6', activate 'Ch priority request bit 5'.

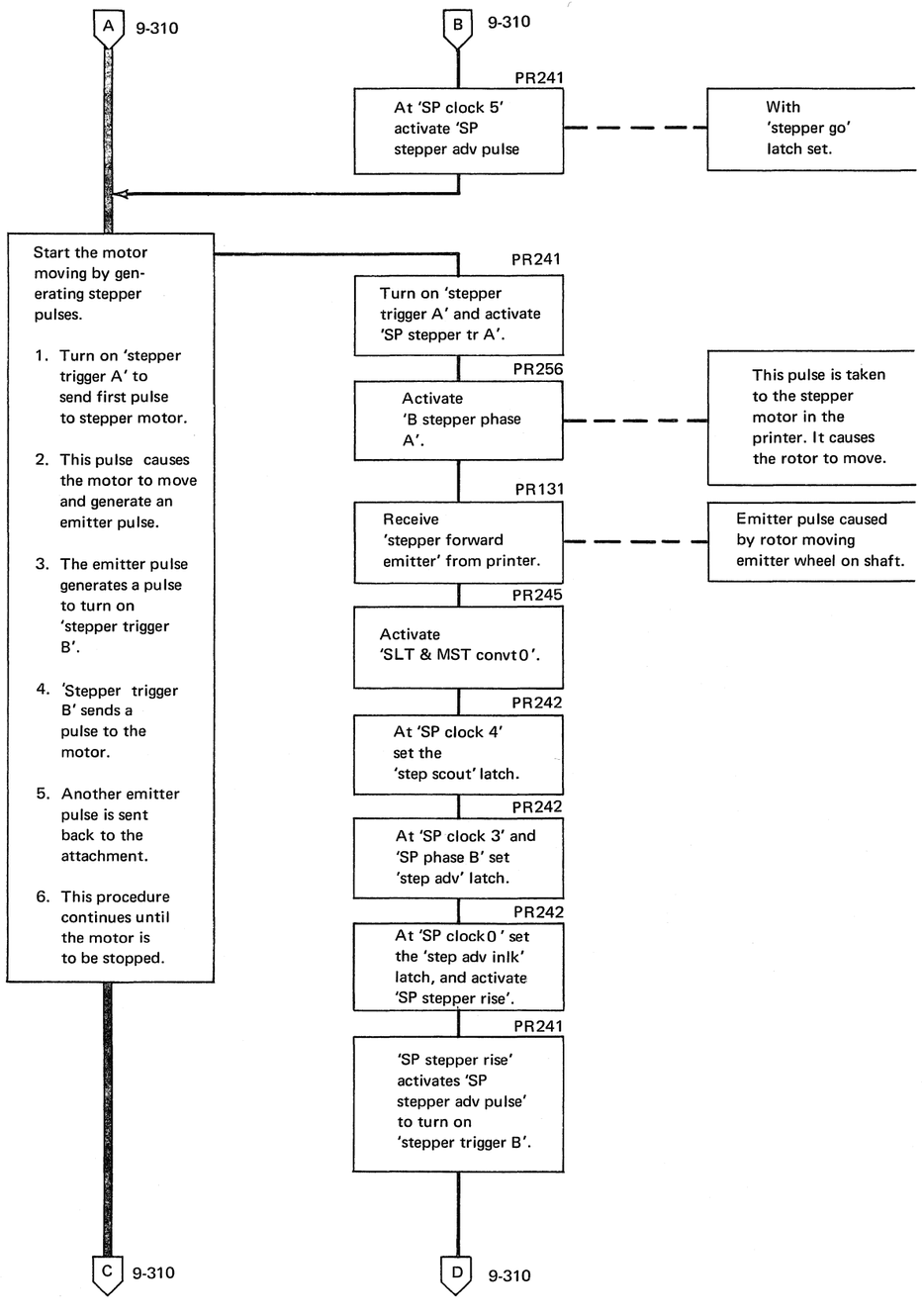
This line active activates 'SP chan 1 cyc steal req 5' to request a cycle steal from the CPU.

End of Operation

Start I/O I–Q Byte Condition				I/O Condition A	I/O Condition B
Incorrect DBO Parity				1	1
Correct DBO Parity	Device address not recognized or N field invalid.			0	0
	Device address recognized and N field valid.	Start I/O	Rejected	1	0
			Accepted	0	1
SIO I-R Byte, and I-O Cycle Condition	Incorrect DBO Parity			1	1
	Correct DBO Parity			0	0

	Line Title	ALD Page	I-Op Cycle 0 1 2 3 4 5 6 7 8	I-Q Cycle 0 1 2 3 4 5 6 7 8	I-R Cycle 0 1 2 3 4 5 6 7 8
1	Ch SIO Instr	PR011			
2	SP DBOR 012Not3	PR213	(decode device address)		
3	Select SP Latch	PR214			
4	Ch I-O Condition (A/B)	PR216			
5	SP Selected SIO I-R Cycle	PR214			
6	SP Set Cmmd Request	PR261			
7	Bi-directional Print Mode	PR411			
8	Command Request Latch	PR231			7B


1
2
3
Start Stepper Motor
The stepper motor is started during the command cycle steal as follows:
1. Fire SS 1.
2. Set 'stepper go' latch.
3. Fire SS A to develop an advance pulse for the stepper triggers.
PR233
At 'SP clock 6' activate 'SP fire SS 1' and 'SP set stepper go and SS A'.
With 'SP cmmd steal' active.
PR112
Activate 'SP SS 1'. SS 1 is fired (35 ms).
An emitter pulse in the printer must respond prior to SS 1 time out. Otherwise a horizontal cycle check will occur.
PR241
Set the 'stepper go' latch.
Activate 'SP fire SS A' and 'SP stepper go L'.
PR112
Activate 'SP SS A'. Active for 2.0 ms.
SS A fired.
PR243
At 'SP clock 3' activate 'SS 1 scout' and 'SS A scout'.
PR243
Activate 'SP SS A rise'.
PR243
At 'SP clock 0', activate 'SS 1 inlk' and 'SS A inlk'.
A 9-311
B 9-311
C 9-311
D 9-311
PR256
Activate 'B stepper phase B'.
This pulse is taken to stepper motor in the printer to produce further movement of the rotor.
PR131
Receive 'stepper forward emitter' from the printer.
This emitter pulse will turn off 'stepper trigger A' and cause further movement of the motor.
This procedure of turning the stepper triggers on and off continues as long as the motor is running. See chart on next page for trigger sequence.
End of Operation



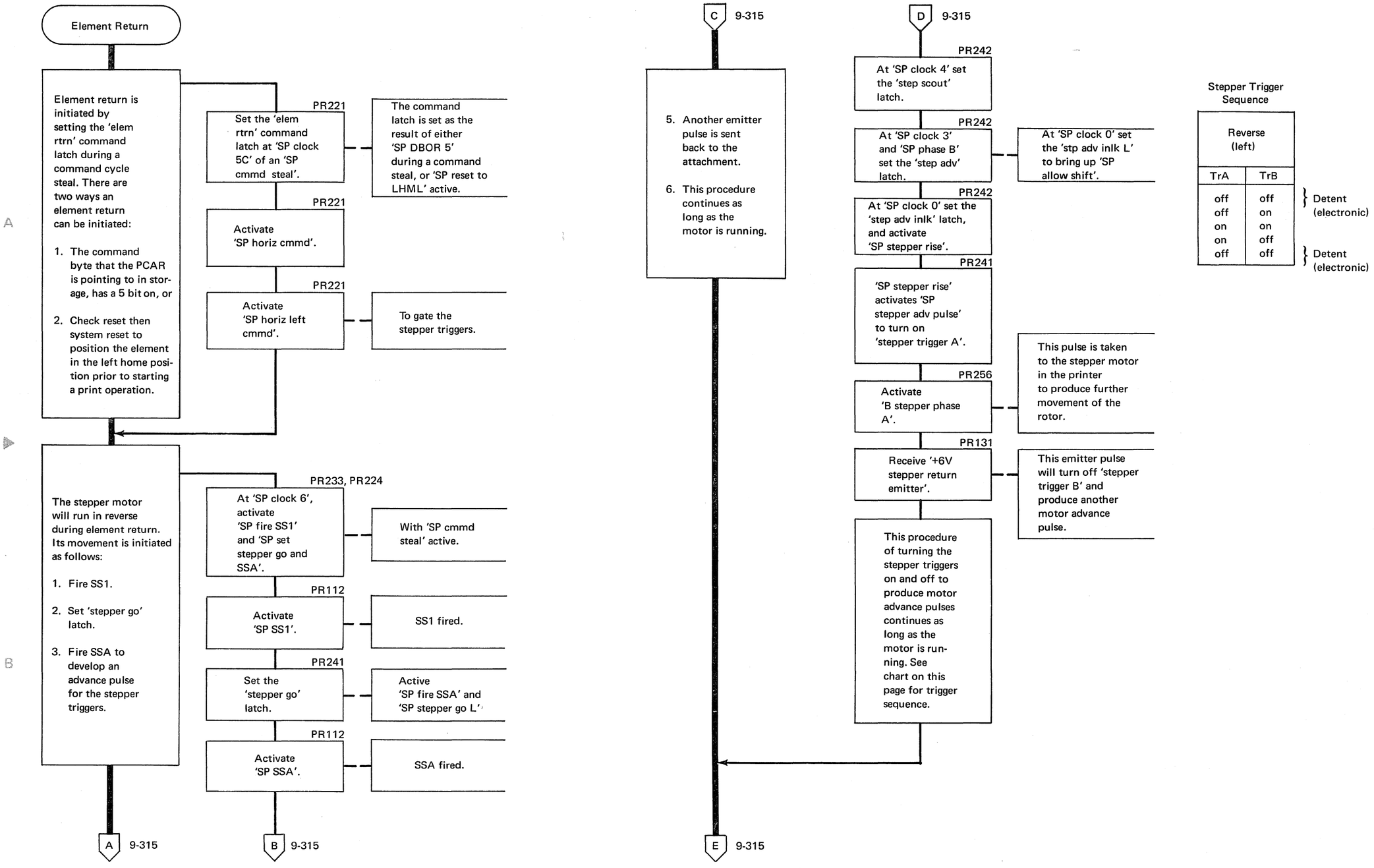
Stepper Trigger Sequence

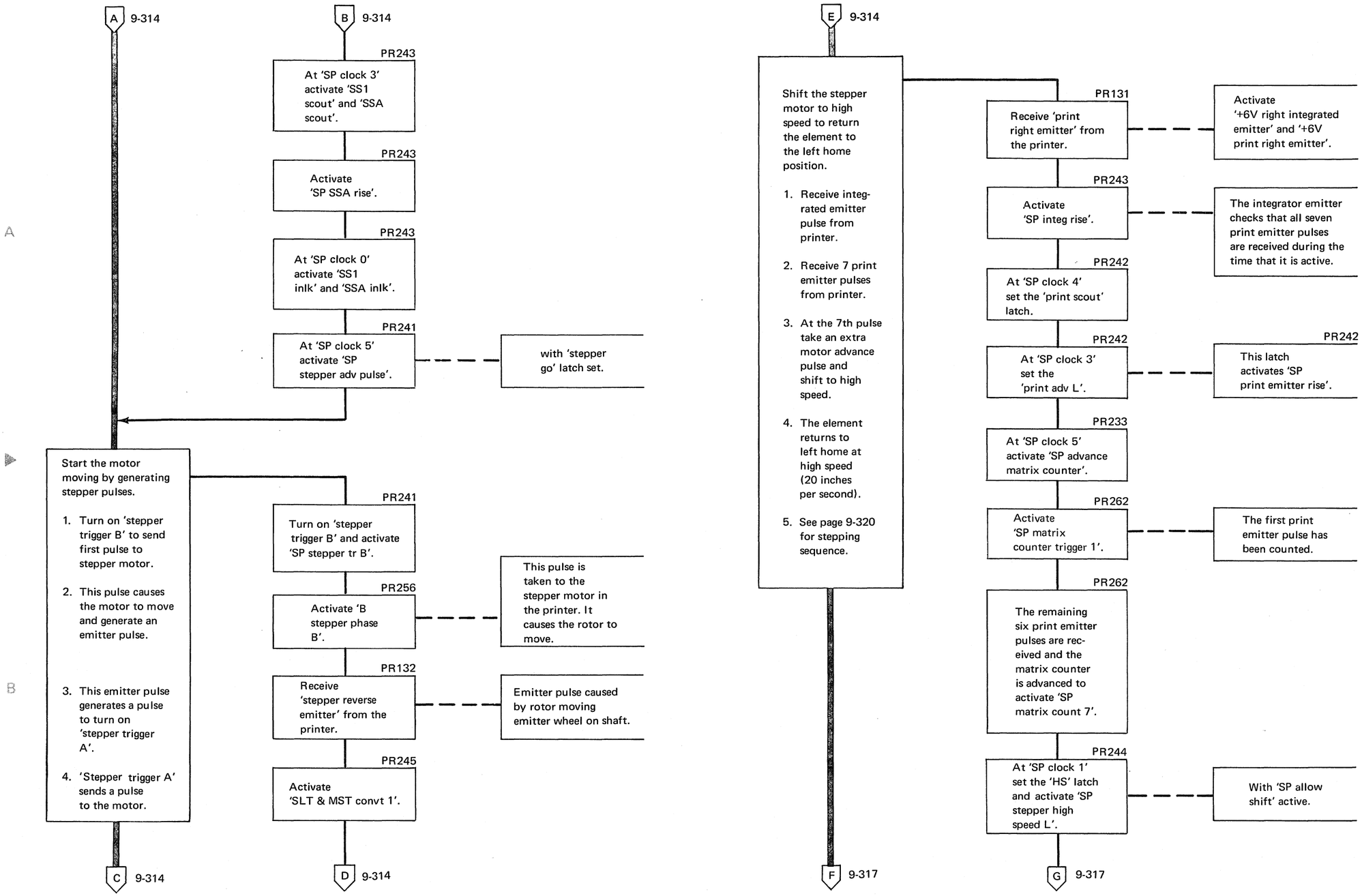
Forward (right)		Reverse (left)		
TrA	TrB	TrA	TrB	
off	off	off	off	} Detent (electronic)
on	off	off	on	
on	on	on	on	
off	on	on	off	
off	off	off	off	} Detent (electronic)

5406 PRINTER ATTACHMENT–Operations
Stepper Motor Start-Move Right (Part 2 of 2)

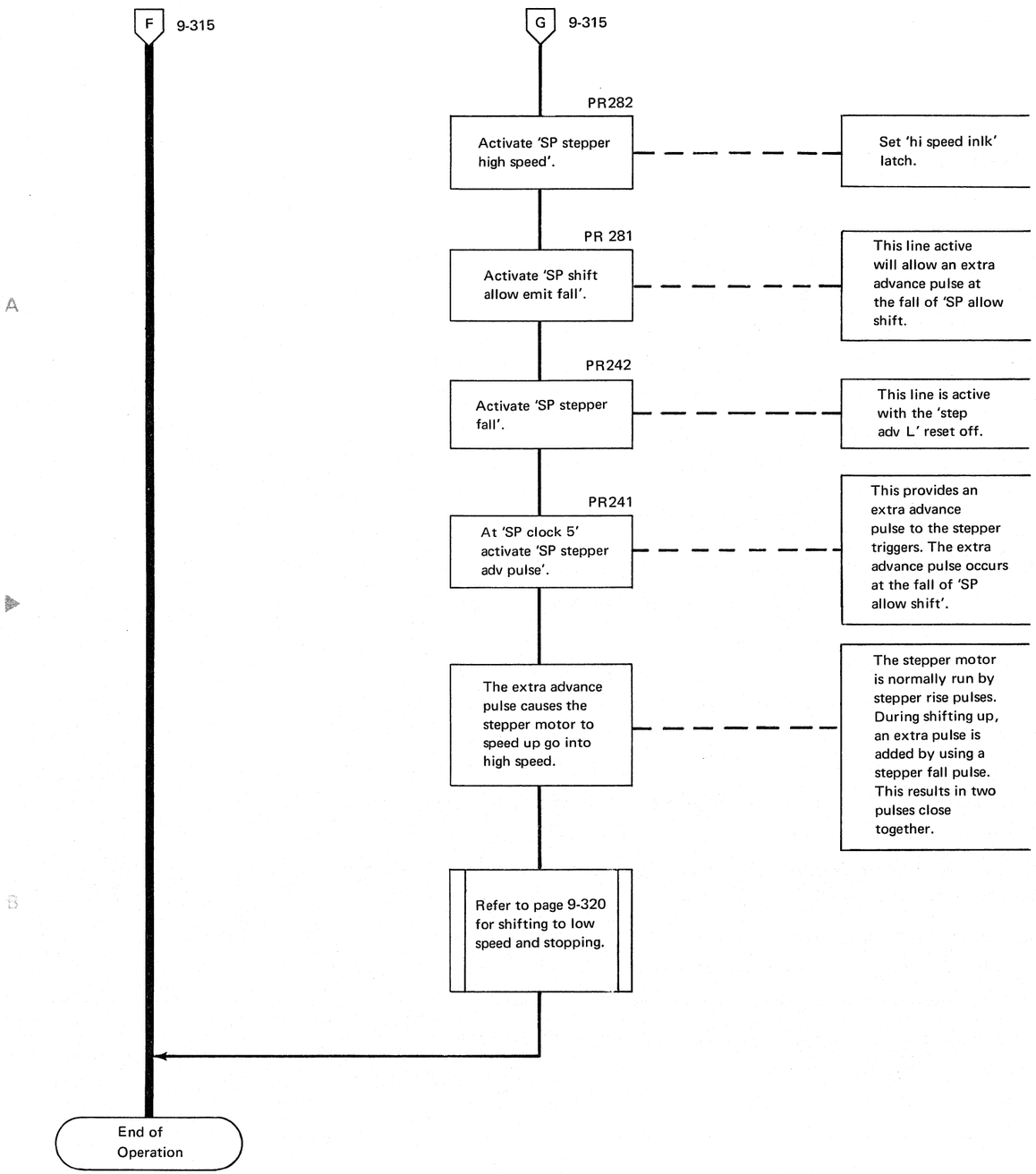
	Line Title	ALD Page	78 | 0 1 2 3 4 5 6 7 8 | 0 1 2 3 4 5 6 7 8
1	Command Steal Latch	PR231	Clock 8 — Microseconds | Milliseconds
2	SP SS1	PR233	Clock 6, 1 — Clock 7D
3	SP Set Stepper Go and SSA	PR224	Clock 6, 1
4	Stepper Go Latch	PR241	Clock 6, 3
5	SP SSA	PR112	Clock 6, 3 — 2.0 ms
6	SS1 Scout	PR243	Clock 3, 2
7	SSA Scout	PR243	Clock 3, 5 — Clock 3, $\overline{5}$
8	SP SSA Rise	PR243	Clock 3, 5, 7, To — Clock 0, 10
9	SS1 Inlk	PR243	Clock 0, 6
10	SSA Inlk	PR243	Clock 0, 7 — Clock 0, $\overline{7}$
11	SP Stepper Advance Pulse	PR241	Clock 5, 8 (13) — 22 Rise (R) 23 R 24 R 13 R 22 R 23 R 24 R 13 R 22 R
12	Stepper A Trigger	PR241	Clock 5, 4, 11 — Clock 5
13	B Stepper Phase A	PR256	12 — $\overline{12}$
14	+6V Stepper Forward Emitter	PR131	≈ 983 usec
15	Step Scout Latch	PR242	Clock 4, $\overline{5}$, 14 — Clock 3, 16
16	Step Adv Latch	PR242	Clock 3, 15 — Clock 3, 15, 17
17	Step Adv Inlk Latch	PR242	Clock 0, 16 — Clock 0
18	SP Stepper Rise Note 1	PR242	Clock 3 to Clock 0
19	SP Stepper Fall Note 1	PR242	Clock 3 to Clock 0
20	SP Allow Shift	PR242	Clock 0, 16, 17 — Clock 3, $\overline{16}$ or $\overline{17}$
21	Stepper B Trigger	PR241	Clock 5, 4, 11 — Clock 5
22	B Stepper Phase B	PR256	21 — $\overline{21}$
23	B Stepper Phase Not A	PR256	$\overline{13}$ — 13
24	B Stepper Phase Not B	PR256	$\overline{22}$ — 22

Note 1. Stepper rise is generated by the leading edge of the stepper emitter feedback pulse.
Stepper fall is generated by the trailing end of the stepper emitter feedback pulse.


1
2
3
A
B
Element Return
Element return is initiated by setting the 'elem rtrn' command latch during a command cycle steal. There are two ways an element return can be initiated:
1. The command byte that the PCAR is pointing to in storage, has a 5 bit on, or
2. Check reset then system reset to position the element in the left home position prior to starting a print operation.
PR221
Set the 'elem rtrn' command latch at 'SP clock 5C' of an 'SP cmmd steal'.
The command latch is set as the result of either 'SP DBOR 5' during a command steal, or 'SP reset to LHML' active.
PR221
Activate 'SP horiz cmmd'.
PR221
Activate 'SP horiz left cmmd'.
To gate the stepper triggers.
The stepper motor will run in reverse during element return. Its movement is initiated as follows:
1. Fire SS1.
2. Set 'stepper go' latch.
3. Fire SSA to develop an advance pulse for the stepper triggers.
PR233, PR224
At 'SP clock 6', activate 'SP fire SS1' and 'SP set stepper go and SSA'.
With 'SP cmmd steal' active.
PR112
Activate 'SP SS1'.
SS1 fired.
PR241
Set the 'stepper go' latch.
Active 'SP fire SSA' and 'SP stepper go L'
PR112
Activate 'SP SSA'.
SSA fired.
A 9-315
B 9-315
C 9-315
5. Another emitter pulse is sent back to the attachment.
6. This procedure continues as long as the motor is running.
D 9-315
PR242
At 'SP clock 4' set the 'step scout' latch.
PR242
At 'SP clock 3' and 'SP phase B' set the 'step adv' latch.
At 'SP clock 0' set the 'stp adv inlk L' to bring up 'SP allow shift'.
PR242
At 'SP clock 0' set the 'step adv inlk' latch, and activate 'SP stepper rise'.
PR241
'SP stepper rise' activates 'SP stepper adv pulse' to turn on 'stepper trigger A'.
This pulse is taken to the stepper motor in the printer to produce further movement of the rotor.
PR256
Activate 'B stepper phase A'.
PR131
Receive '+6V stepper return emitter'.
This emitter pulse will turn off 'stepper trigger B' and produce another motor advance pulse.
This procedure of turning the stepper triggers on and off to produce motor advance pulses continues as long as the motor is running. See chart on this page for trigger sequence.
E 9-315
Stepper Trigger Sequence
Reverse (left)
TrA TrB
off off
off on
on on
on off
off off
Detent (electronic)
Detent (electronic)



5406 PRINTER ATTACHMENT–Operations
Element Return (Part 2 of 3)

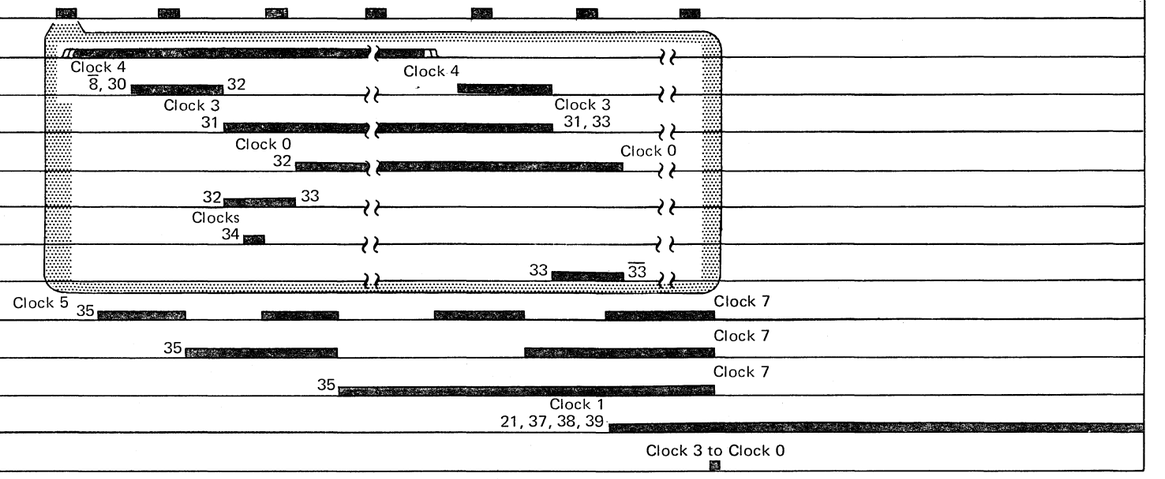


5406 PRINTER ATTACHMENT–Operations
Element Return (Part 3 of 3)

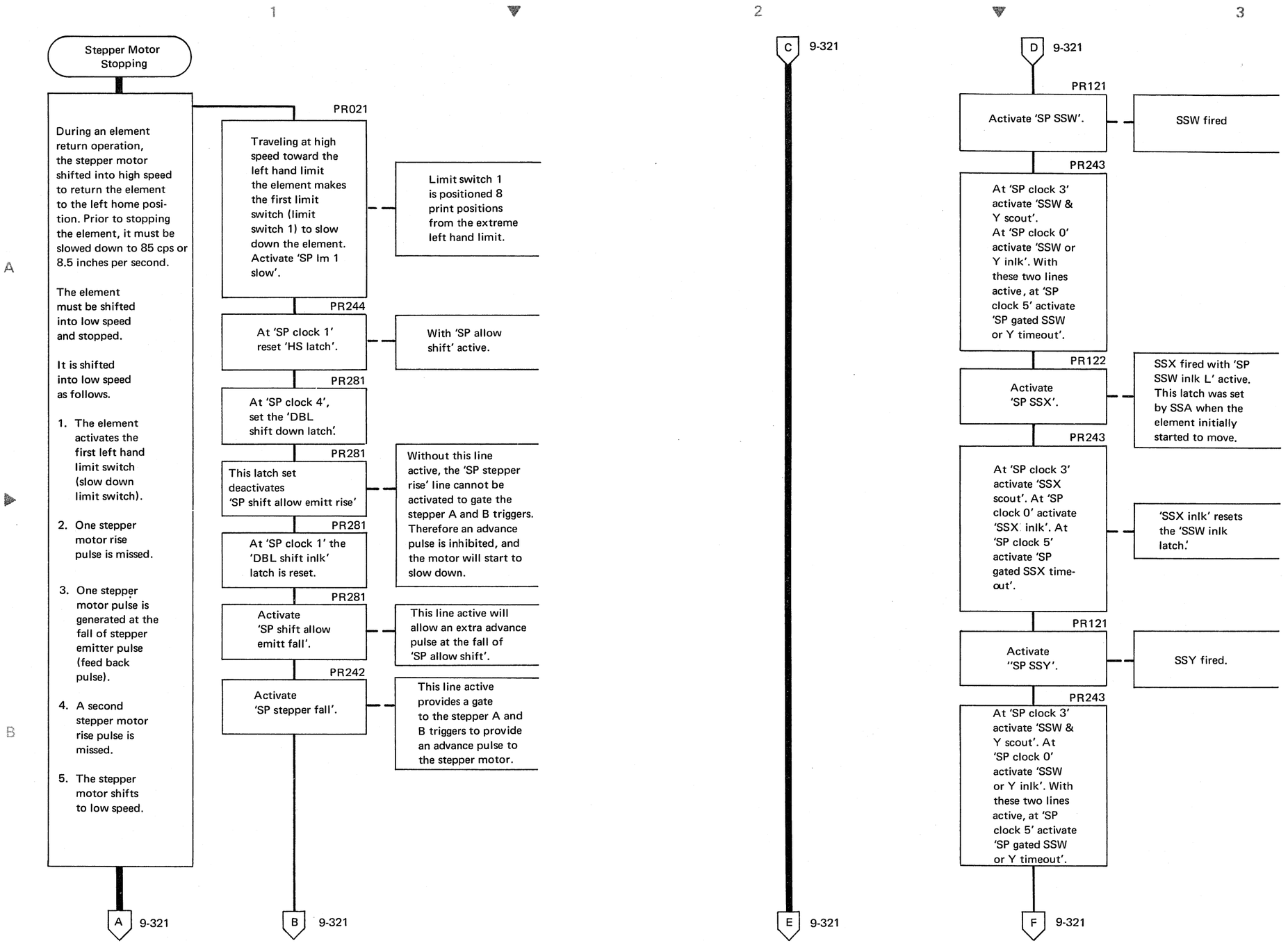
1 2 3

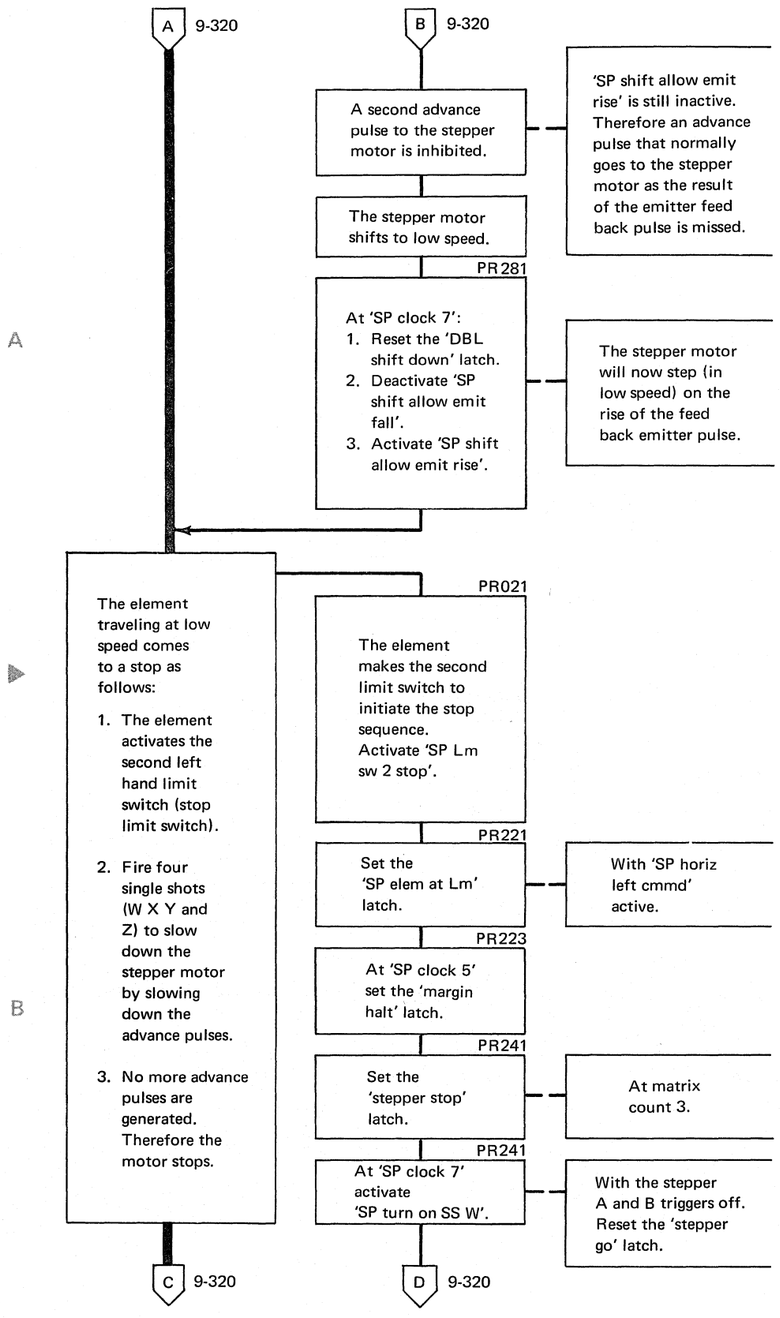
		Line Title	ALD Page	78 012345678 012345678 0
	1	Command Steal Latch	PR231	Clock 7D; Milliseconds; Microseconds
	2	Elem Rtrn Latch	PR221	Clock 5C 1
	3	SP Horiz Cmmd	PR221	Clock 5C 2
	4	SP Horiz Left Cmmd	PR221	Clock 5C 2
	5	SP SS1	PR233	Clock 6 1
	6	SP Set Stepper Go and SSA	PR224	Clock 6 1
	7	Stepper Go Latch	PR241	Clock 6 6
A	8	SP SSA	PR112	Clock 6 6; 2.0 ms
	9	SS1 Scout	PR243	Clock 3 5
	10	SSA Scout	PR243	Clock 3 8; Clock 3 $\overline{8}$
	11	SSA Rise	PR243	Clock 3 8, 10, $\overline{13}$; Clock 0 13
	12	SS1 Inlk	PR243	Clock 0 9
	13	SSA Inlk	PR243	Clock 0 10; Clock 0 $\overline{10}$
	14	SP Stepper Advance Pulse	PR241	Clock 5 11; Rise (R) 26; 27 R 28 R 16 R R R R R R R R Fall R R R R R R R R
	15	Stepper B Trigger	PR241	Clock 5 7, 14; Clock 5
	16	B Stepper Phase B	PR256	15; $\overline{15}$
▶	17	Stepper Reverse Emitter	PR132	≈ 932 usec; ≈ 491 usec
	18	Step Scout Latch	PR242	Clock 3 $\overline{8}$, 17
	19	Step Adv Latch	PR242	Clock 3 18; Clock 3 18, 20
	20	Step Adv Inlk Latch	PR242	Clock 0 19; Clock 0
	21	SP Allow Shift	PR242	Clock 0 19, 20; Clock 3 $\overline{19}$
	22	Stepper Emitter Rise Note 1	PR242	Clock 3 to Clock 0
	23	Stepper Emitter Fall Note 1	PR242	Clock 3 to Clock 0
	24	Stepper A Trigger	PR241	Clock 5
	25	B Stepper Phase A	PR256	$\overline{24}$
B	26	B Stepper Phase Not B	PR256	$\overline{15}$; 15
	27	B Stepper Phase Not A	PR256	$\overline{25}$; 25
	28	SP Integ Emitter	PR243	

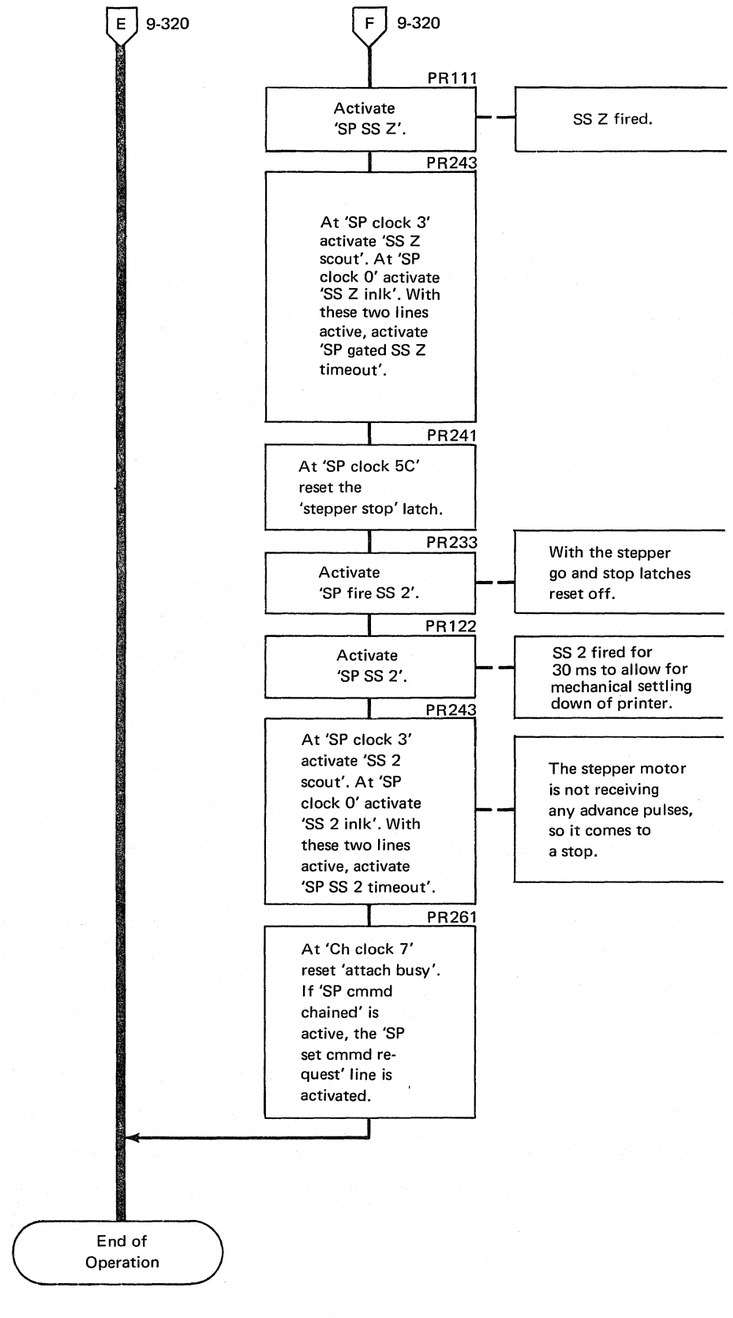
	Line Title	ALD Page	78 012345678 012345678
29	+6V Print Right Emitter	PR131	
30	+6V Print Right Emitter	PR131	
31	Print Scout Latch	PR242	
32	Print Adv Latch	PR242	
33	Print Adv Inlk Latch	PR242	
34	SP Print Emitter Rise	PR242	
35	SP Advance Matrix Counter	PR233	
36	SP Print Emitter Fall	PR242	
37	SP Matrix Counter TR1	PR262	
38	SP Matrix Counter TR2	PR262	
39	SP Matrix Counter TR4	PR262	
40	SP Stepper Hi Speed Latch	PR244	
41	SP Integ Fall	PR243	



Note 1: Stepper rise is generated by the leading edge of the stepper emitter feedback pulse.
Stepper fall is generated by the trailing edge of the stepper emitter feedback pulse.


1
2
3
Stepper Motor Stopping
During an element return operation, the stepper motor shifted into high speed to return the element to the left home position. Prior to stopping the element, it must be slowed down to 85 cps or 8.5 inches per second.
The element must be shifted into low speed and stopped.
It is shifted into low speed as follows.
1. The element activates the first left hand limit switch (slow down limit switch).
2. One stepper motor rise pulse is missed.
3. One stepper motor pulse is generated at the fall of stepper emitter pulse (feed back pulse).
4. A second stepper motor rise pulse is missed.
5. The stepper motor shifts to low speed.
A
B
PR021
Traveling at high speed toward the left hand limit the element makes the first limit switch (limit switch 1) to slow down the element. Activate 'SP lm 1 slow'.
Limit switch 1 is positioned 8 print positions from the extreme left hand limit.
PR244
At 'SP clock 1' reset 'HS latch'.
With 'SP allow shift' active.
PR281
At 'SP clock 4', set the 'DBL shift down latch'.
PR281
This latch set deactivates 'SP shift allow emitt rise'
Without this line active, the 'SP stepper rise' line cannot be activated to gate the stepper A and B triggers. Therefore an advance pulse is inhibited, and the motor will start to slow down.
PR281
At 'SP clock 1' the 'DBL shift inlk' latch is reset.
PR281
Activate 'SP shift allow emitt fall'.
This line active will allow an extra advance pulse at the fall of 'SP allow shift'.
PR242
Activate 'SP stepper fall'.
This line active provides a gate to the stepper A and B triggers to provide an advance pulse to the stepper motor.
A 9-321
B 9-321
C 9-321
E 9-321
D 9-321
F 9-321
PR121
Activate 'SP SSW'.
SSW fired
PR243
At 'SP clock 3' activate 'SSW & Y scout'. At 'SP clock 0' activate 'SSW or Y inlk'. With these two lines active, at 'SP clock 5' activate 'SP gated SSW or Y timeout'.
PR122
Activate 'SP SSX'.
SSX fired with 'SP SSW inlk L' active. This latch was set by SSA when the element initially started to move.
PR243
At 'SP clock 3' activate 'SSX scout'. At 'SP clock 0' activate 'SSX inlk'. At 'SP clock 5' activate 'SP gated SSX time-out'.
'SSX inlk' resets the 'SSW inlk latch.'
PR121
Activate "SP SSY'.
SSY fired.
PR243
At 'SP clock 3' activate 'SSW & Y scout'. At 'SP clock 0' activate 'SSW or Y inlk'. With these two lines active, at 'SP clock 5' activate 'SP gated SSW or Y timeout'.

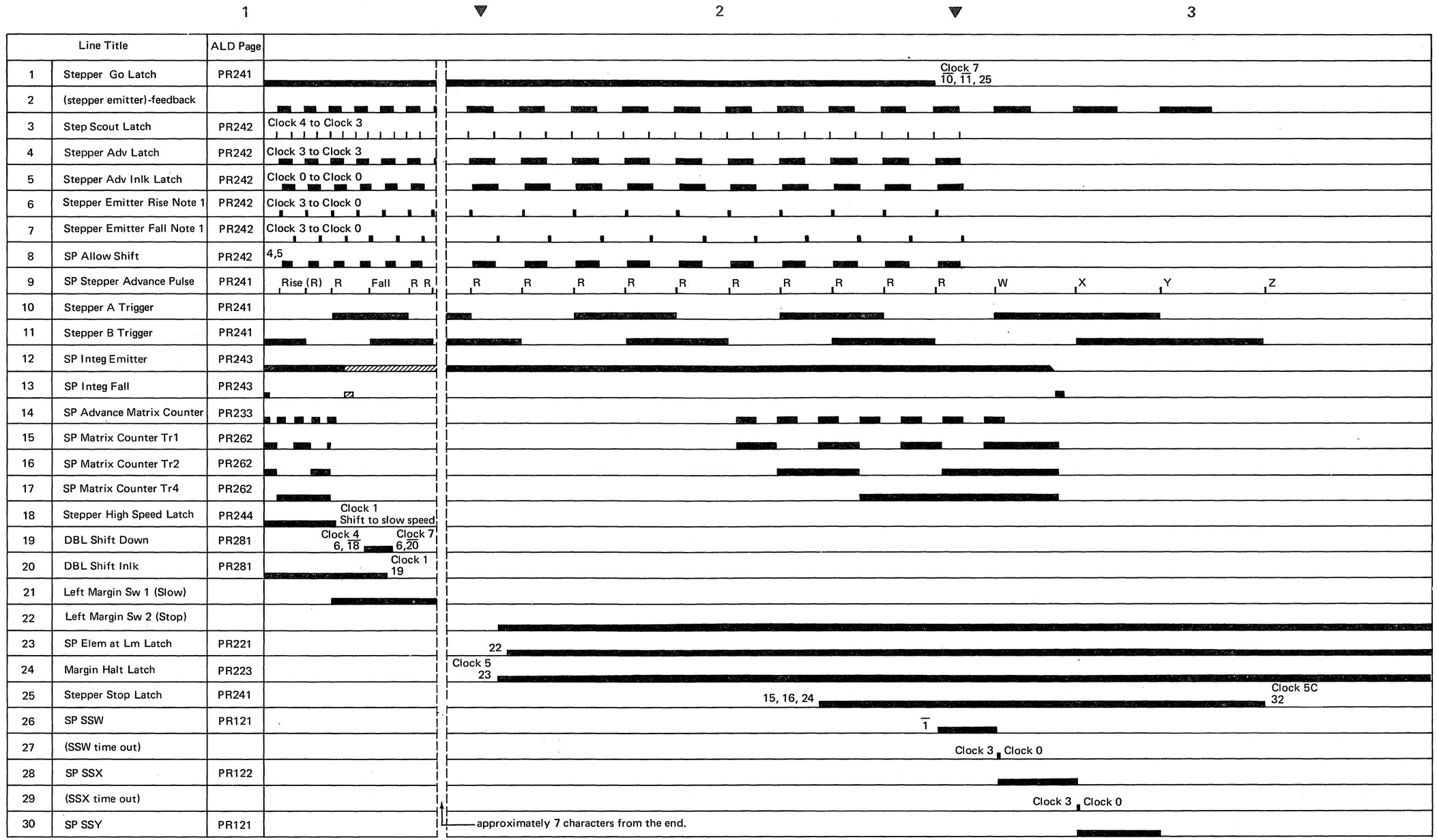




5406 PRINTER ATTACHMENT–Operations
Stepper Motor Stopping (Part 2 of 2)

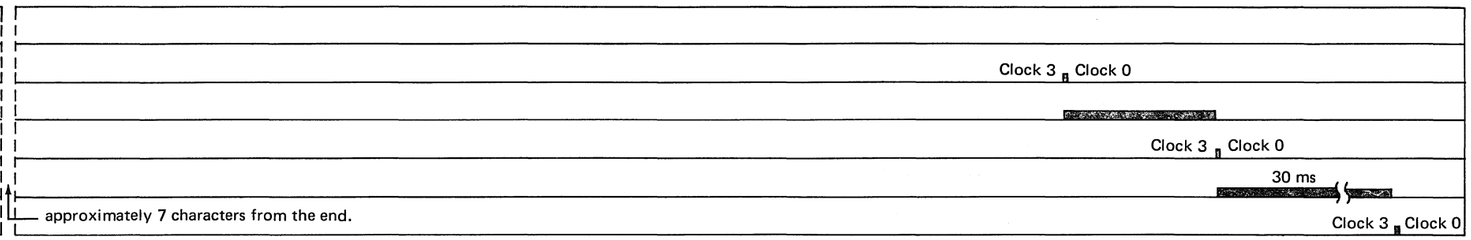
Stepper Motor Stopping Timing Chart (Part 1 of 2)

		Line Title	ALD Page
	1	Stepper Go Latch	PR241
	2	(stepper emitter)-feedback	
	3	Step Scout Latch	PR242
	4	Stepper Adv Latch	PR242
	5	Stepper Adv Inlk Latch	PR242
	6	Stepper Emitter Rise Note 1	PR242
	7	Stepper Emitter Fall Note 1	PR242
A	8	SP Allow Shift	PR242
	9	SP Stepper Advance Pulse	PR241
	10	Stepper A Trigger	PR241
	11	Stepper B Trigger	PR241
	12	SP Integ Emitter	PR243
	13	SP Integ Fall	PR243
	14	SP Advance Matrix Counter	PR233
	15	SP Matrix Counter Tr1	PR262
	16	SP Matrix Counter Tr2	PR262
▶	17	SP Matrix Counter Tr4	PR262
	18	Stepper High Speed Latch	PR244
	19	DBL Shift Down	PR281
	20	DBL Shift Inlk	PR281
	21	Left Margin Sw 1 (Slow)	
	22	Left Margin Sw 2 (Stop)	
	23	SP Elem at Lm Latch	PR221
	24	Margin Halt Latch	PR223
	25	Stepper Stop Latch	PR241
B	26	SP SSW	PR121
	27	(SSW time out)	
	28	SP SSX	PR122
	29	(SSX time out)	
	30	SP SSY	PR121



1 2 3

	Line Title	ALD Page	
31	(SSY time out)		
32	SP SSZ	PR111	
33	(SSZ time out)		
34	SP SS2	PR122	
35	(SS2 time out)		



Note 1. Stepper rise is generated by the leading edge of the stepper emitter feedback pulse.
Stepper fall is generated by the trailing edge of the stepper emitter feedback pulse.

A

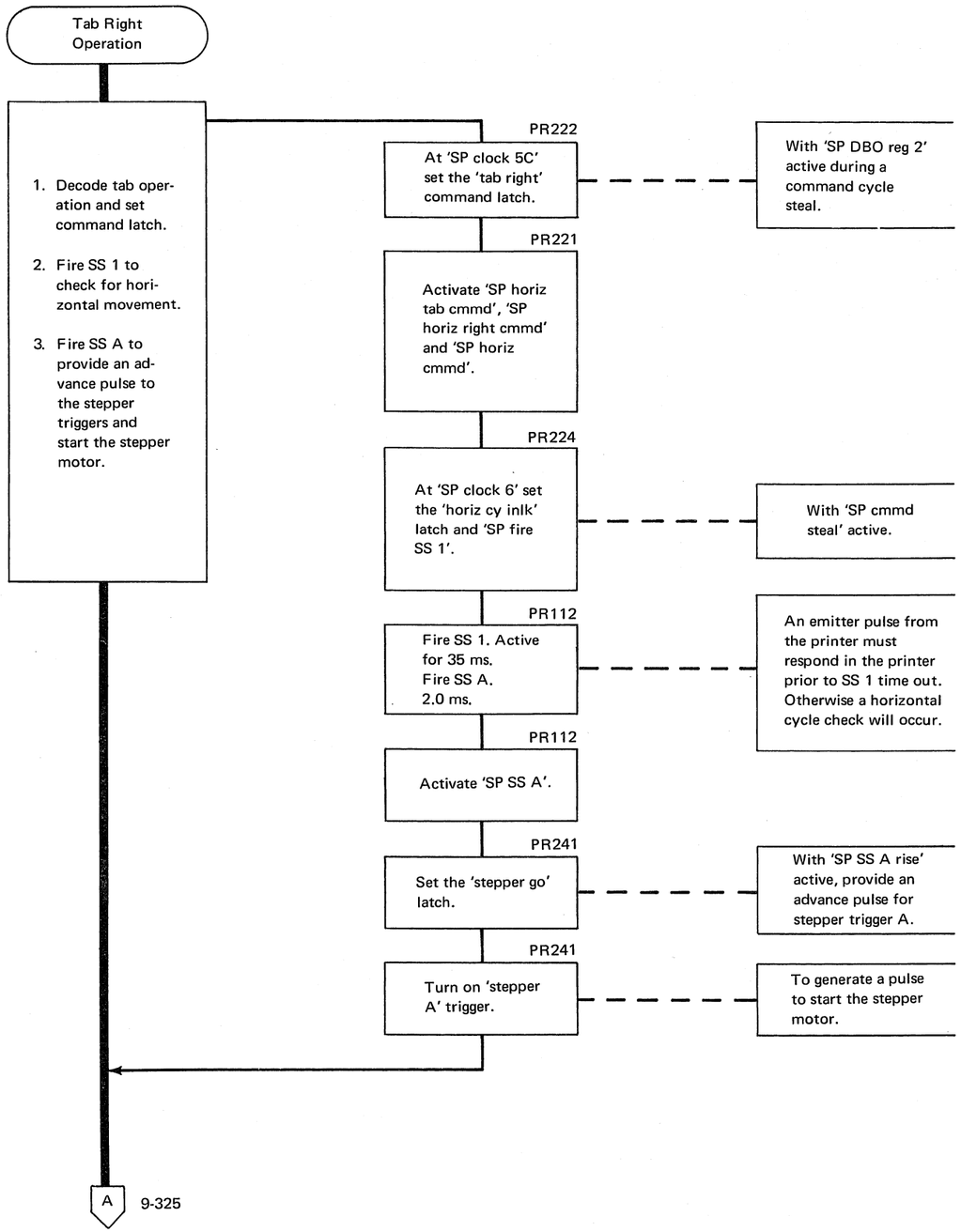
B

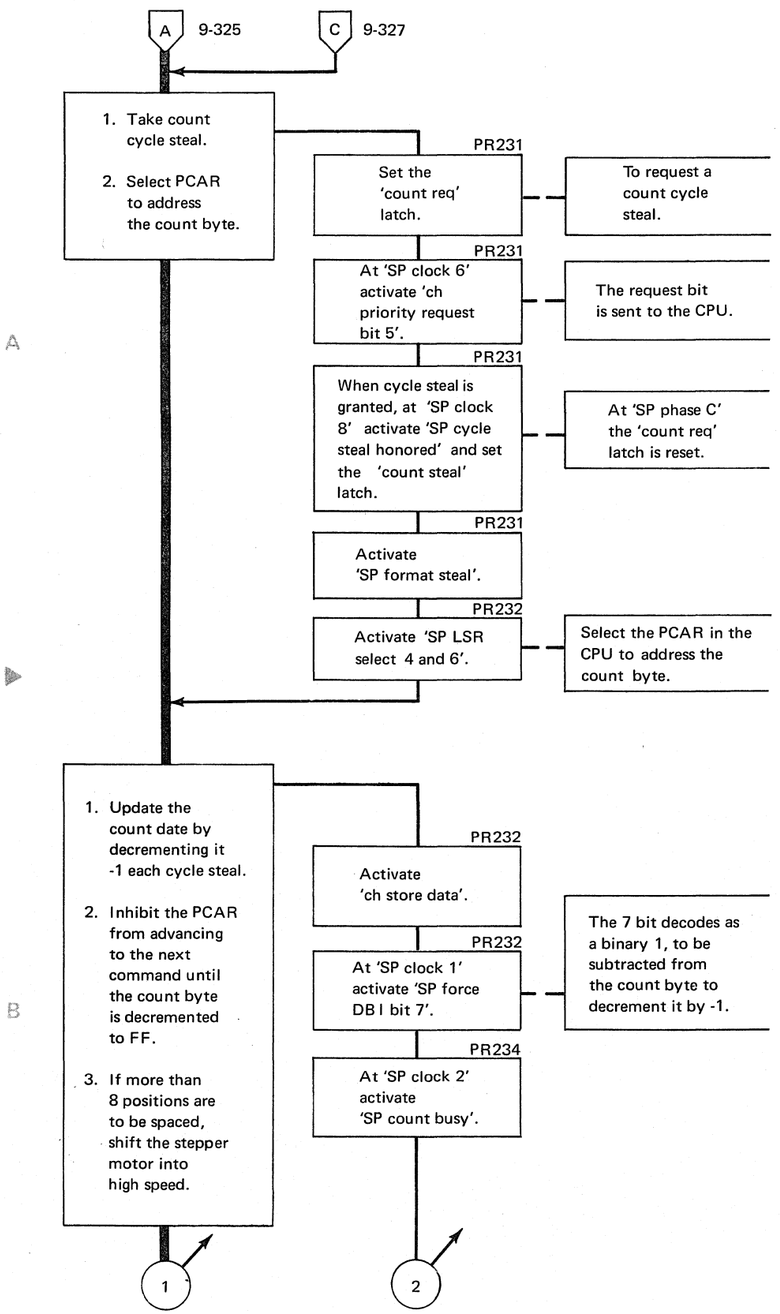
TAB RIGHT OPERATION

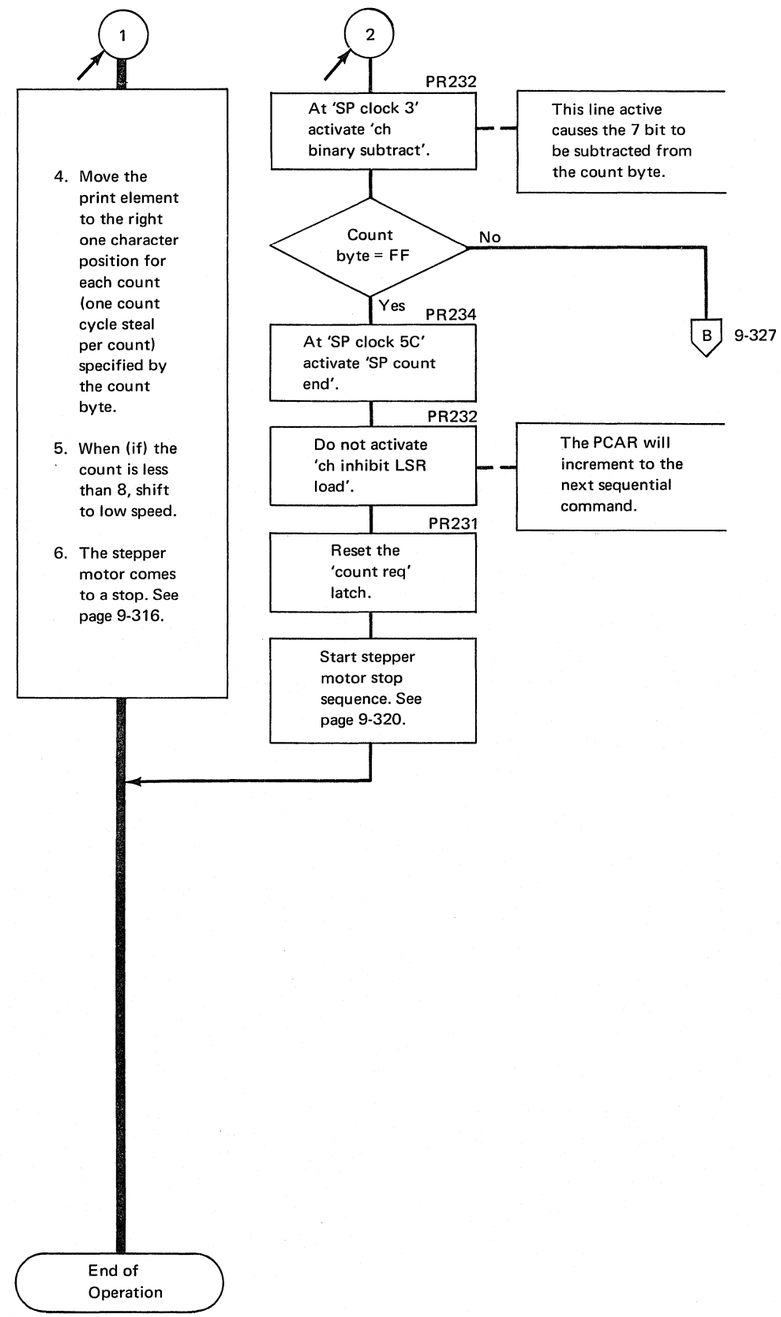
The tab right operation moves the print element to the right a number of character positions specified by the count byte. On printers with 22 inch carriages or bi-directional printing, tabs of more than eight character positions begin at high speed. Tabbing at high speed continues until a count of eight is detected in the count byte. At this time the print element is shifted down into low speed to complete the operation.

Printers with 13 inch carriages without bi-directional printing always tab right at low speed.

- During a command cycle steal the 'tab right' latch is set.
- SS1 is fired to check for a horizontal cycle check.
- SSA is fired to start the stepper motor.
- A count cycle steal is requested.
- A count cycle steal is granted and the PCAR is selected.
- The PCAR addresses the count byte and it is modified –1 in the ALU and placed back in main storage.
- The stepper motor moves the print element one character position.
- Count cycles are taken until the count byte equals FF and 'SP count end' is raised in the attachment.



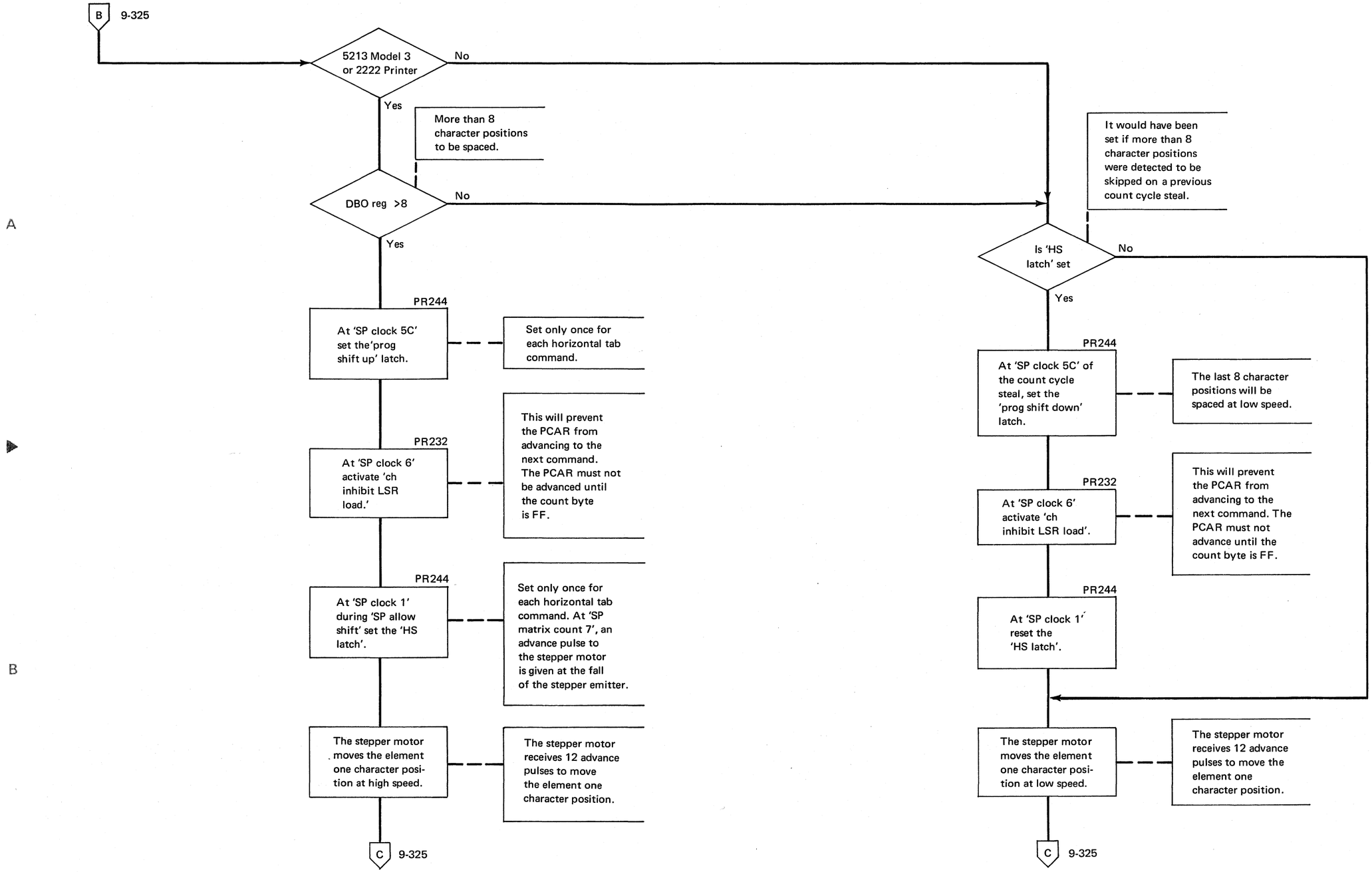




5406 PRINTER ATTACHMENT–Operations
Tab Right (Part 2 of 3)

A

B


B 9-325
5213 Model 3 or 2222 Printer
No
Yes
More than 8 character positions to be spaced.
DBO reg >8
No
Yes
It would have been set if more than 8 character positions were detected to be skipped on a previous count cycle steal.
Is 'HS latch' set
No
Yes
PR244
At 'SP clock 5C' set the 'prog shift up' latch.
Set only once for each horizontal tab command.
PR244
At 'SP clock 5C' of the count cycle steal, set the 'prog shift down' latch.
The last 8 character positions will be spaced at low speed.
PR232
At 'SP clock 6' activate 'ch inhibit LSR load.'
This will prevent the PCAR from advancing to the next command. The PCAR must not be advanced until the count byte is FF.
PR232
At 'SP clock 6' activate 'ch inhibit LSR load'.
This will prevent the PCAR from advancing to the next command. The PCAR must not advance until the count byte is FF.
PR244
At 'SP clock 1' during 'SP allow shift' set the 'HS latch'.
Set only once for each horizontal tab command. At 'SP matrix count 7', an advance pulse to the stepper motor is given at the fall of the stepper emitter.
PR244
At 'SP clock 1' reset the 'HS latch'.
The stepper motor moves the element one character position at high speed.
The stepper motor receives 12 advance pulses to move the element one character position.
The stepper motor moves the element one character position at low speed.
The stepper motor receives 12 advance pulses to move the element one character position.
C 9-325
C 9-325

1 2 3

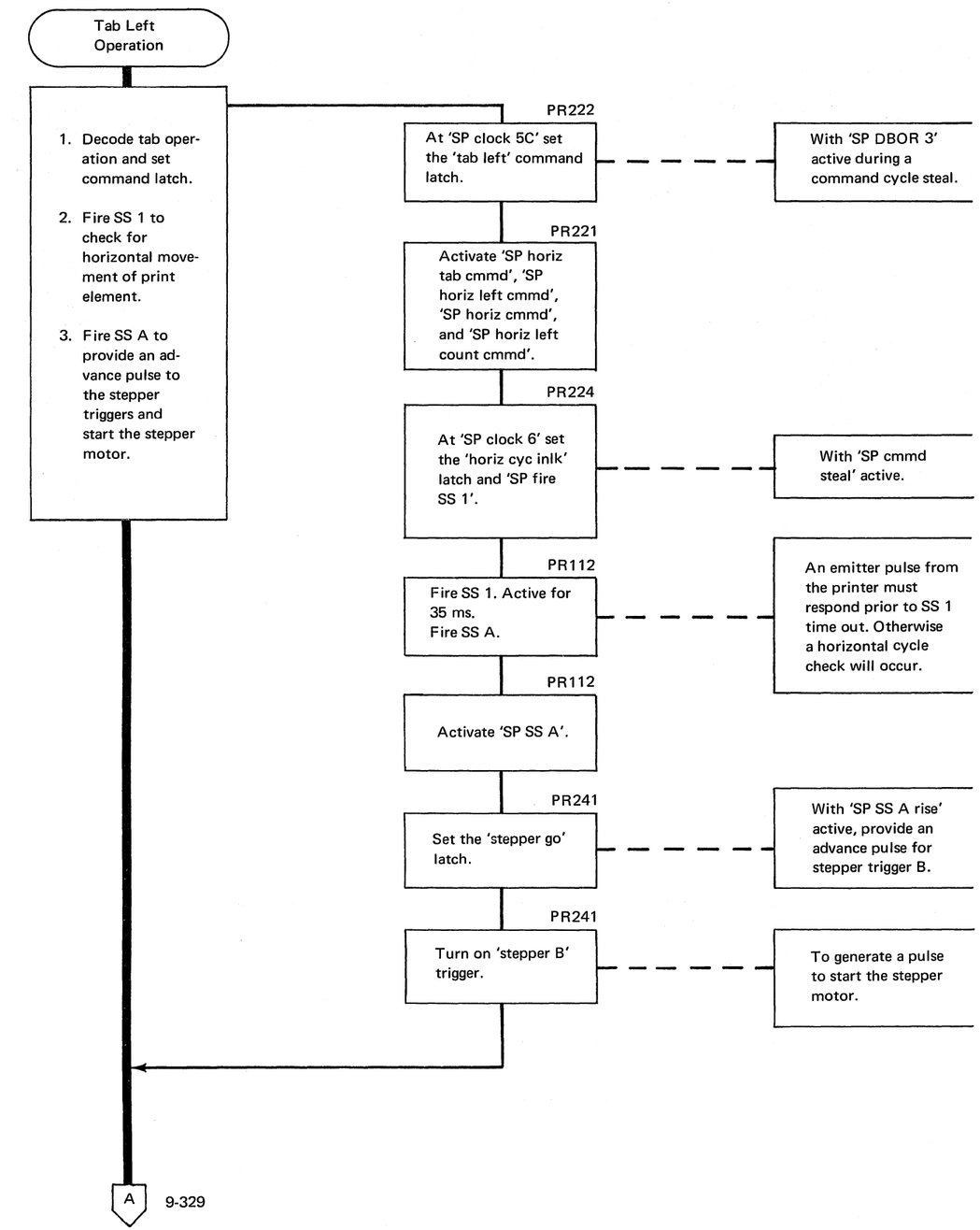
TAB LEFT OPERATION

The tab left operation moves the print element to the left a number of character positions specified by the count byte. Tabs of more than eight character positions begin at high speed and continue until a count of eight is detected in the count byte. At this time the print element is shifted down into low speed to complete the operation.

- During a command cycle steal the 'tab left' latch is set.
- SS1 is fired to check for a horizontal cycle check.
- SSA is fired to start the stepper motor.
- A count cycle steal is requested.

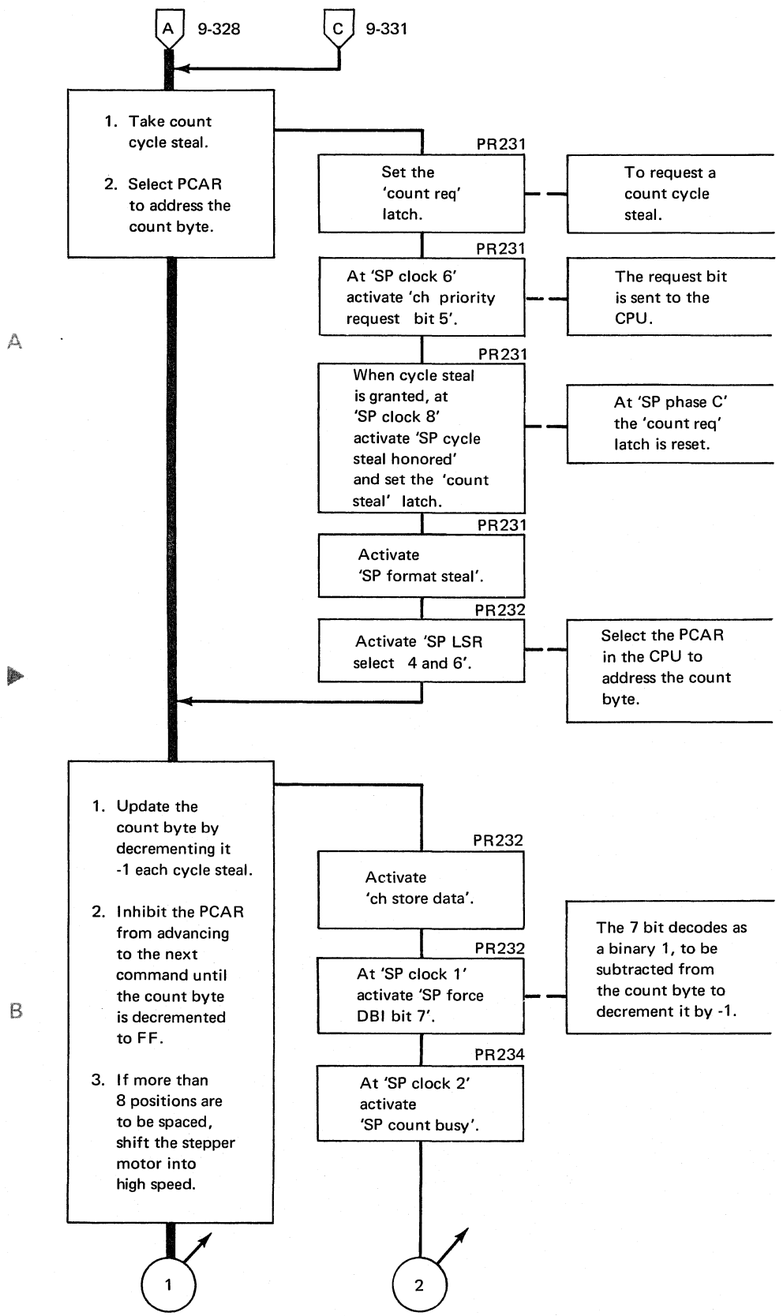
A

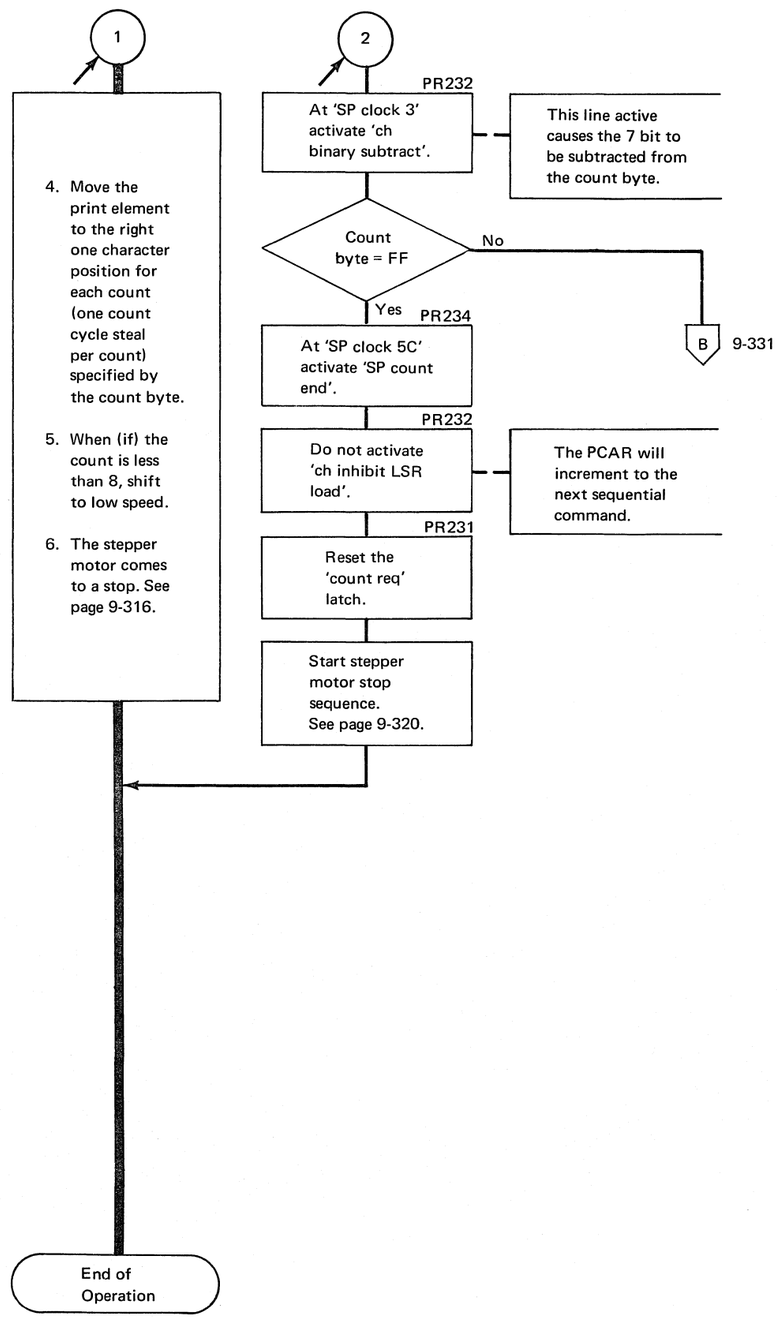
- A count cycle steal is granted and the PCAR is selected.
- The PCAR addresses the count byte and it is modified −1 in the ALU and placed back in main storage.
- The stepper motor moves the print element one print position.
- Count cycle steals are taken until the count byte equals FF and 'SP count end' is raised in the attachment.



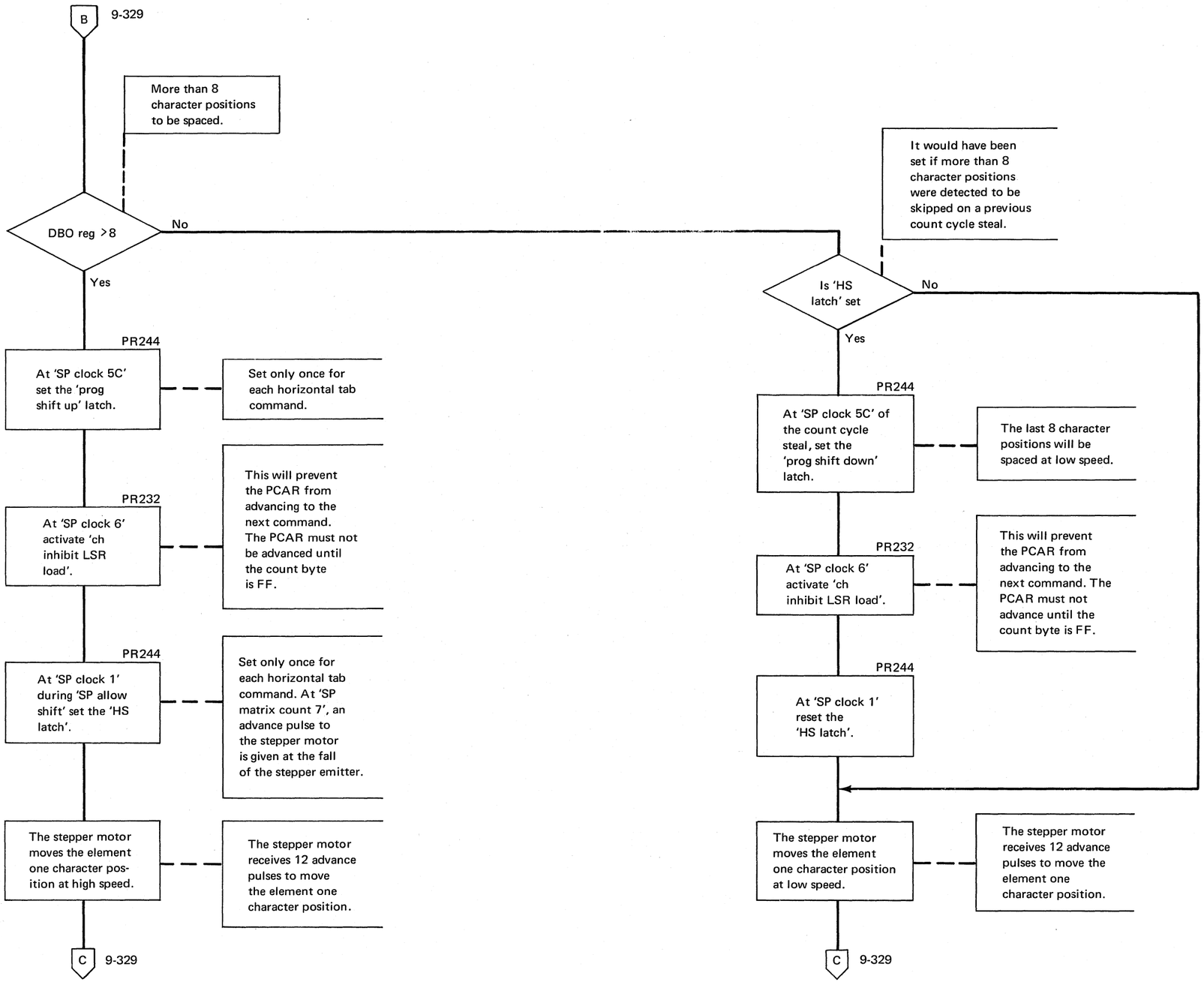
B

A 9-329





5406 PRINTER ATTACHMENT–Operations
Tab Left (Part 2 of 3)

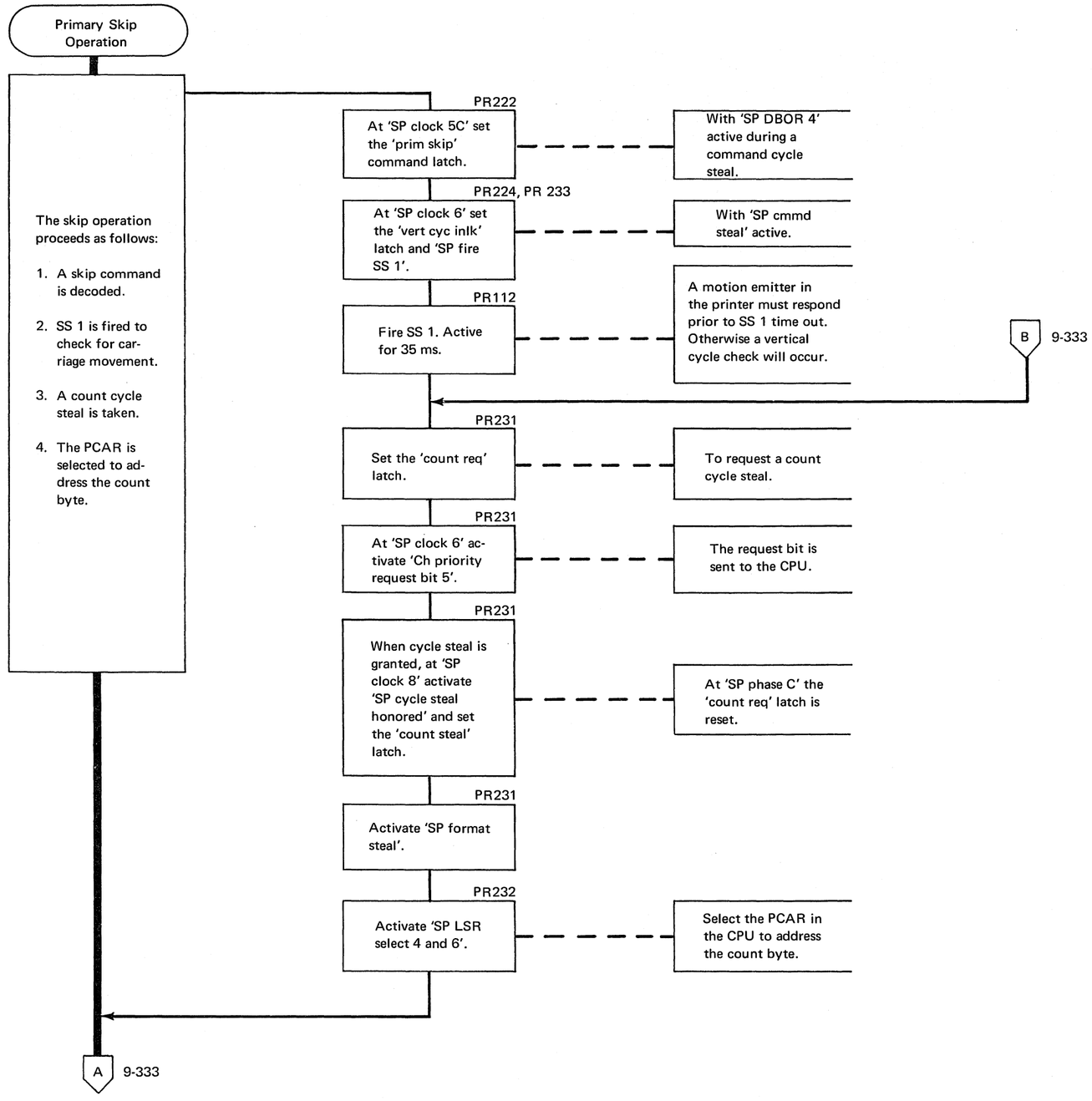


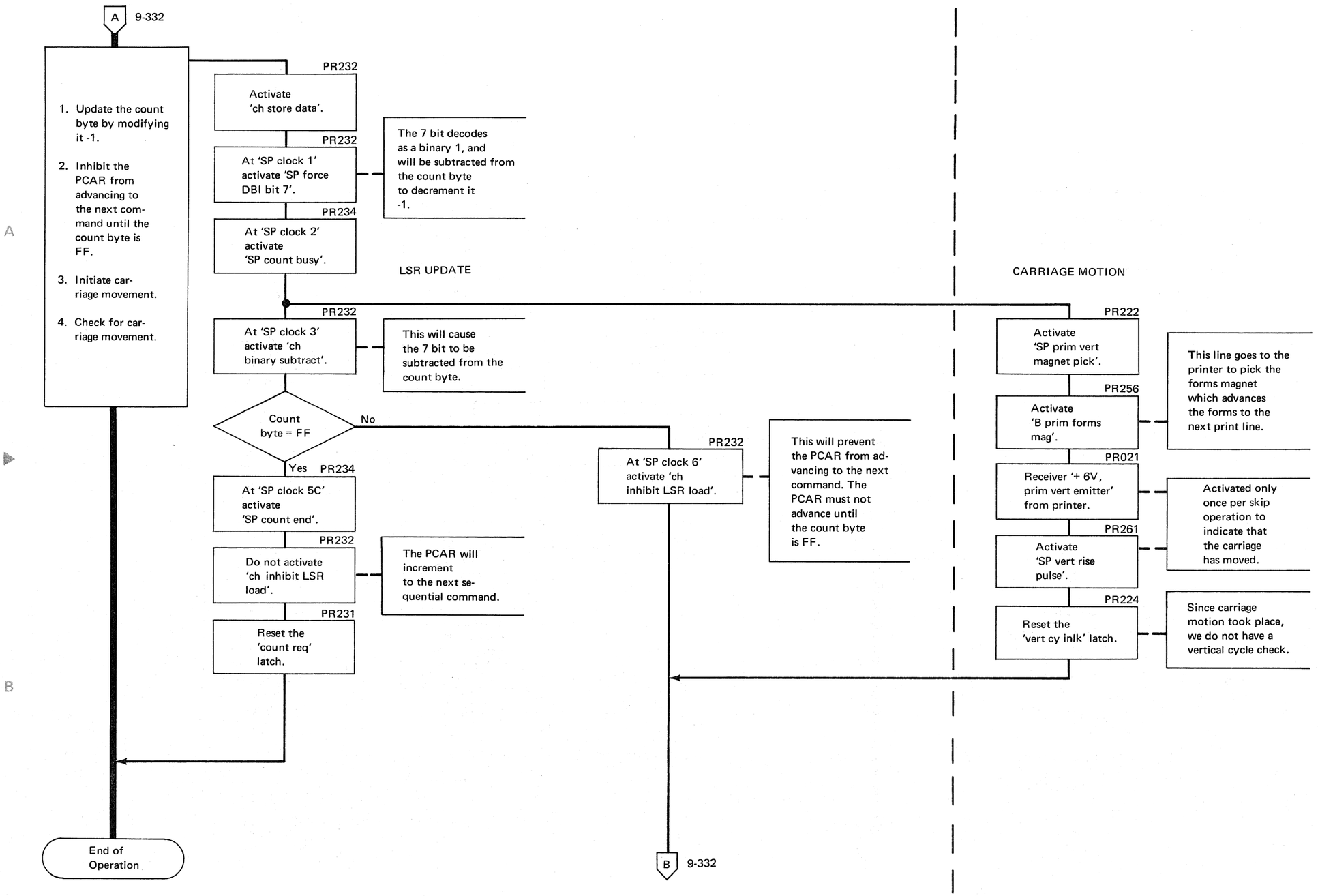
5406 PRINTER ATTACHMENT–Operations
Tab Left (Part 3 of 3)

PRIMARY SKIP OPERATION

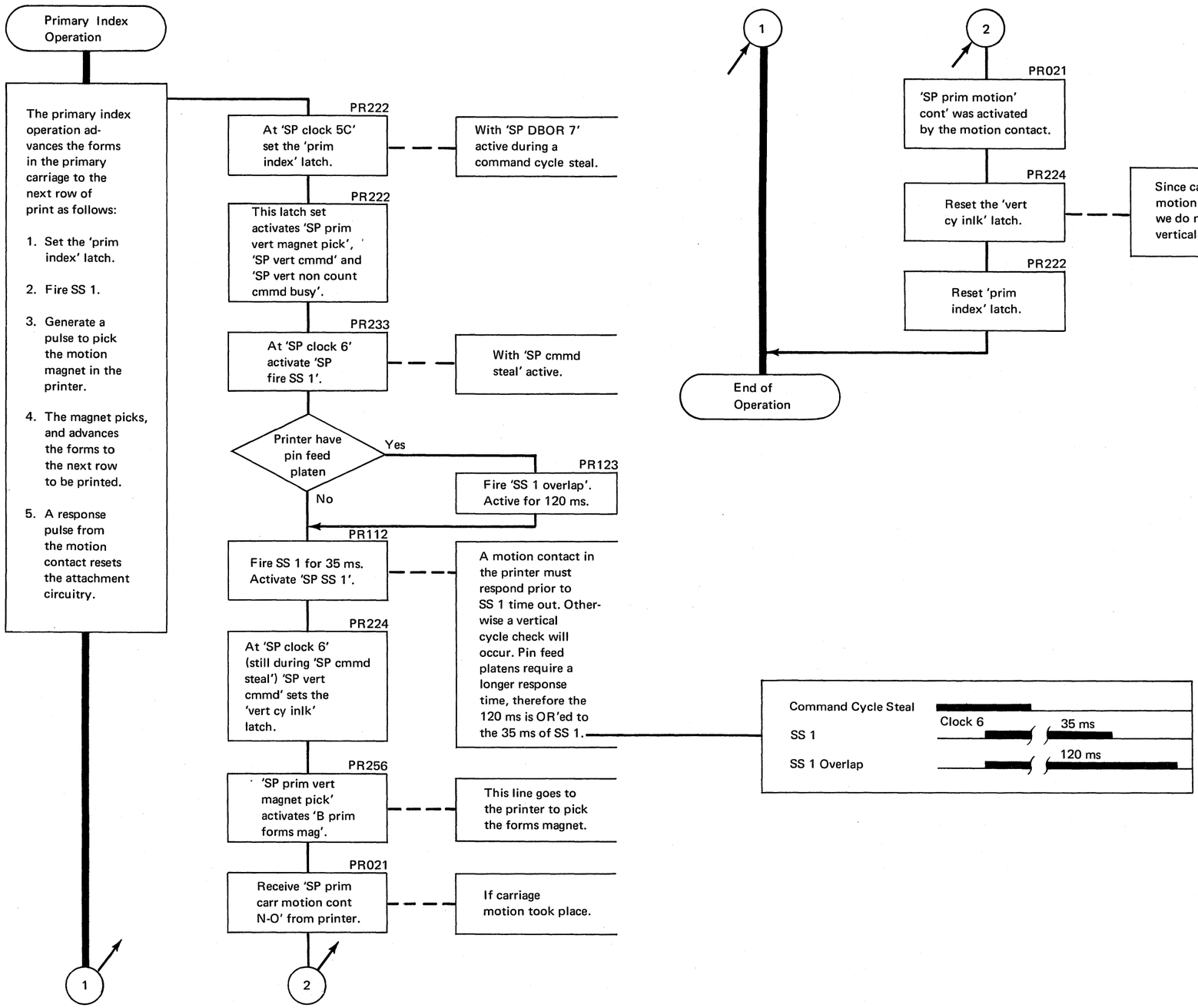
A skip operation can take place only on a primary carriage. Any number of lines from 2 to 256 may be skipped. The number of lines to be skipped is contained in the count byte in main storage (addressed by the PCAR). One count cycle steal must be taken for each line to be skipped. Count cycle steals are taken until the count byte is FF.

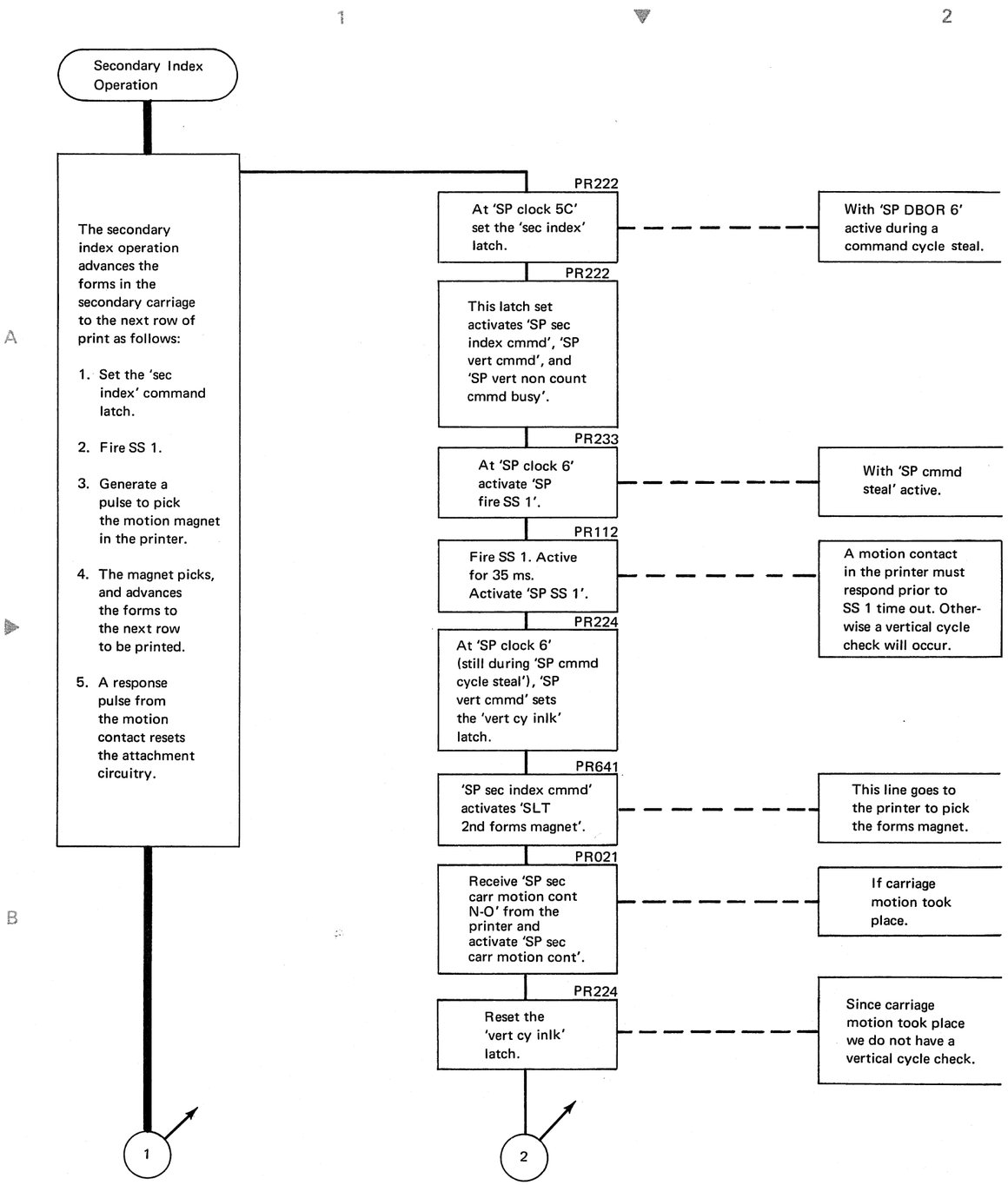
- During a command cycle steal the 'prim skip' latch is set.
- SS1 is fired to check for a vertical cycle check.
- A count cycle steal is requested.
- The count cycle steal is granted and the PCAR is selected.
- The PCAR addresses the count byte and it is modified −1 in the ALU and placed back in main storage.
- The attachment generates a pulse to pick the forms magnet in the printer.
- The printer advances the forms one print line.
- The motion emitter in the printer sends a response to the attachment to reset attachment vertical cycle check circuitry.
- Count cycle steals are taken until the count byte equals FF and 'SP count end' is raised in the attachment.

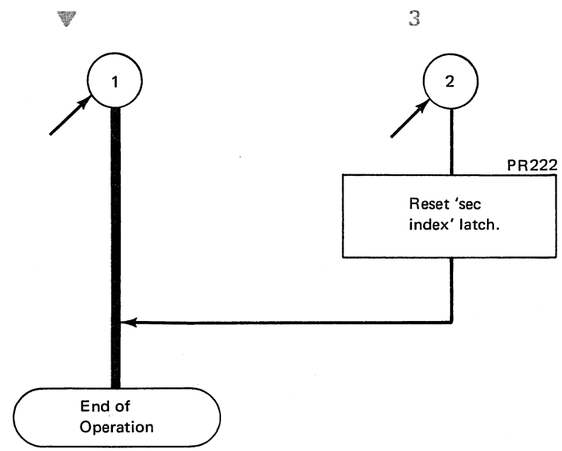


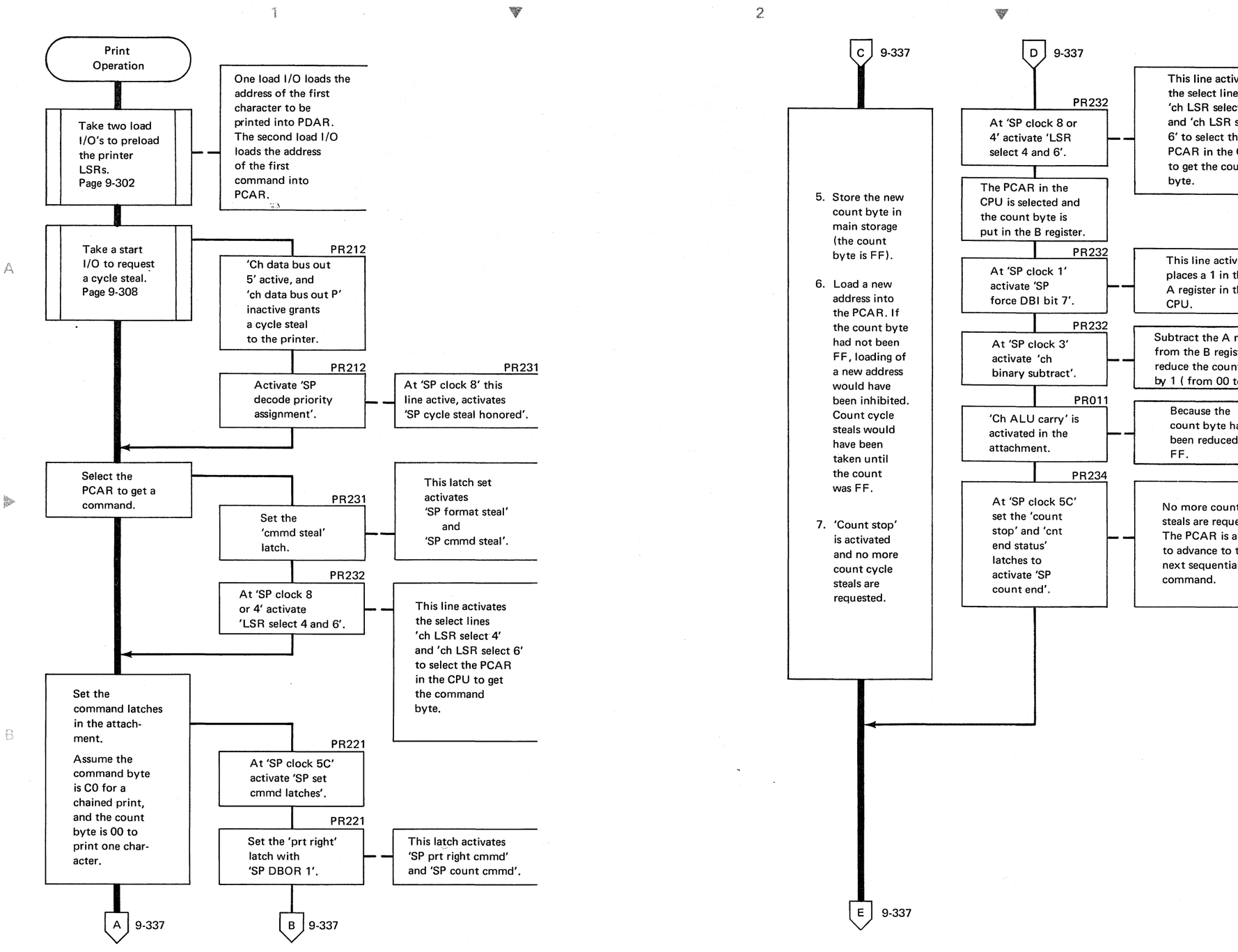


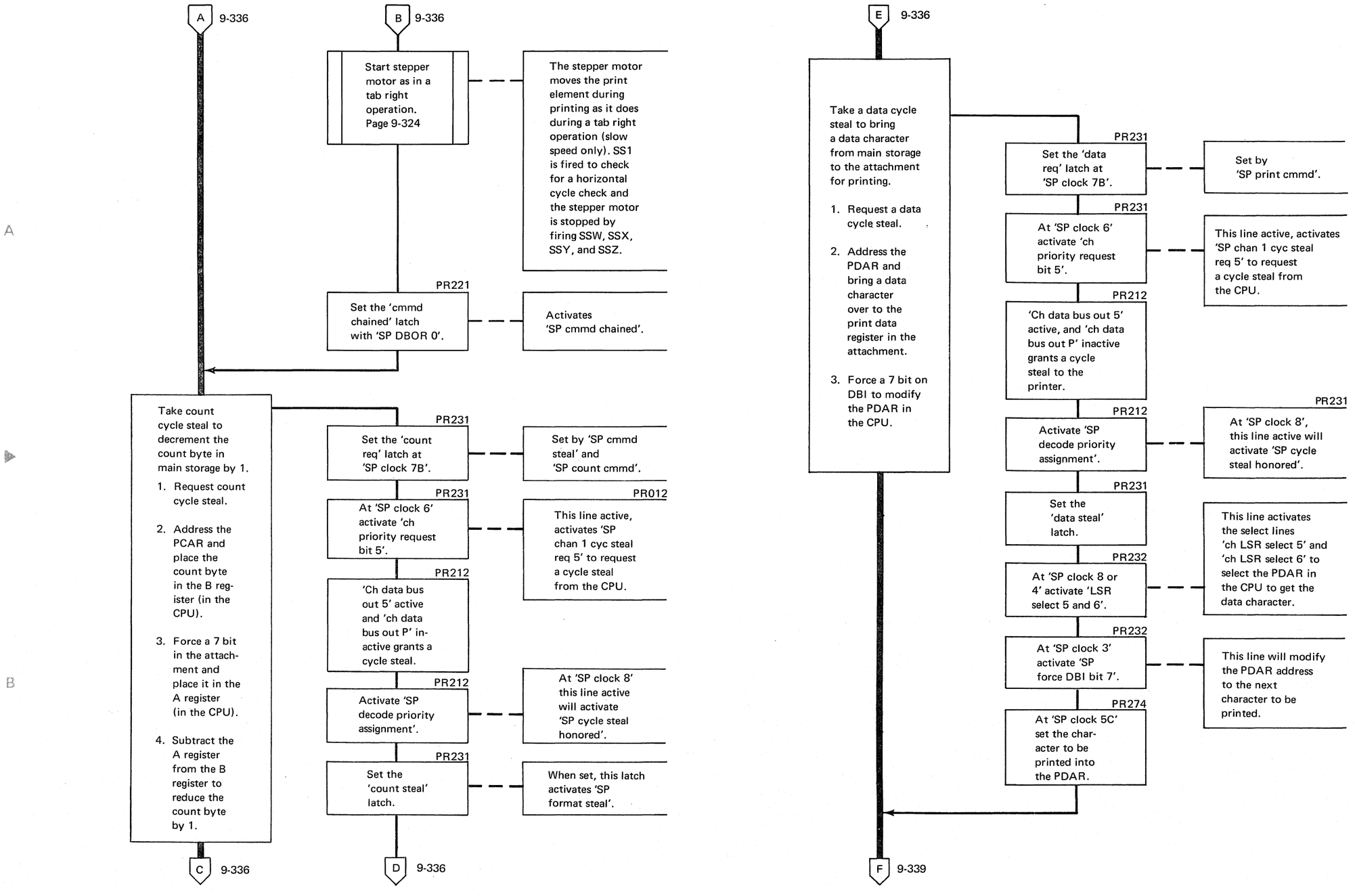
5406 PRINTER ATTACHMENT–Operations
Primary Skip (Part 2 of 2)


1
2
3
Primary Index Operation
The primary index operation advances the forms in the primary carriage to the next row of print as follows:
1. Set the 'prim index' latch.
2. Fire SS 1.
3. Generate a pulse to pick the motion magnet in the printer.
4. The magnet picks, and advances the forms to the next row to be printed.
5. A response pulse from the motion contact resets the attachment circuitry.
PR222
At 'SP clock 5C' set the 'prim index' latch.
With 'SP DBOR 7' active during a command cycle steal.
PR222
This latch set activates 'SP prim vert magnet pick', 'SP vert cmmd' and 'SP vert non count cmmd busy'.
PR233
At 'SP clock 6' activate 'SP fire SS 1'.
With 'SP cmmd steal' active.
Printer have pin feed platen
Yes
No
PR123
Fire 'SS 1 overlap'. Active for 120 ms.
PR112
Fire SS 1 for 35 ms. Activate 'SP SS 1'.
A motion contact in the printer must respond prior to SS 1 time out. Otherwise a vertical cycle check will occur. Pin feed platens require a longer response time, therefore the 120 ms is OR'ed to the 35 ms of SS 1.
PR224
At 'SP clock 6' (still during 'SP cmmd steal') 'SP vert cmmd' sets the 'vert cy inlk' latch.
PR256
'SP prim vert magnet pick' activates 'B prim forms mag'.
This line goes to the printer to pick the forms magnet.
PR021
Receive 'SP prim carr motion cont N-O' from printer.
If carriage motion took place.
1
2
Command Cycle Steal
SS 1
SS 1 Overlap
Clock 6
35 ms
120 ms
1
2
PR021
'SP prim motion' cont' was activated by the motion contact.
PR224
Reset the 'vert cy inlk' latch.
Since carriage motion took place, we do not have a vertical cycle check.
PR222
Reset 'prim index' latch.
End of Operation

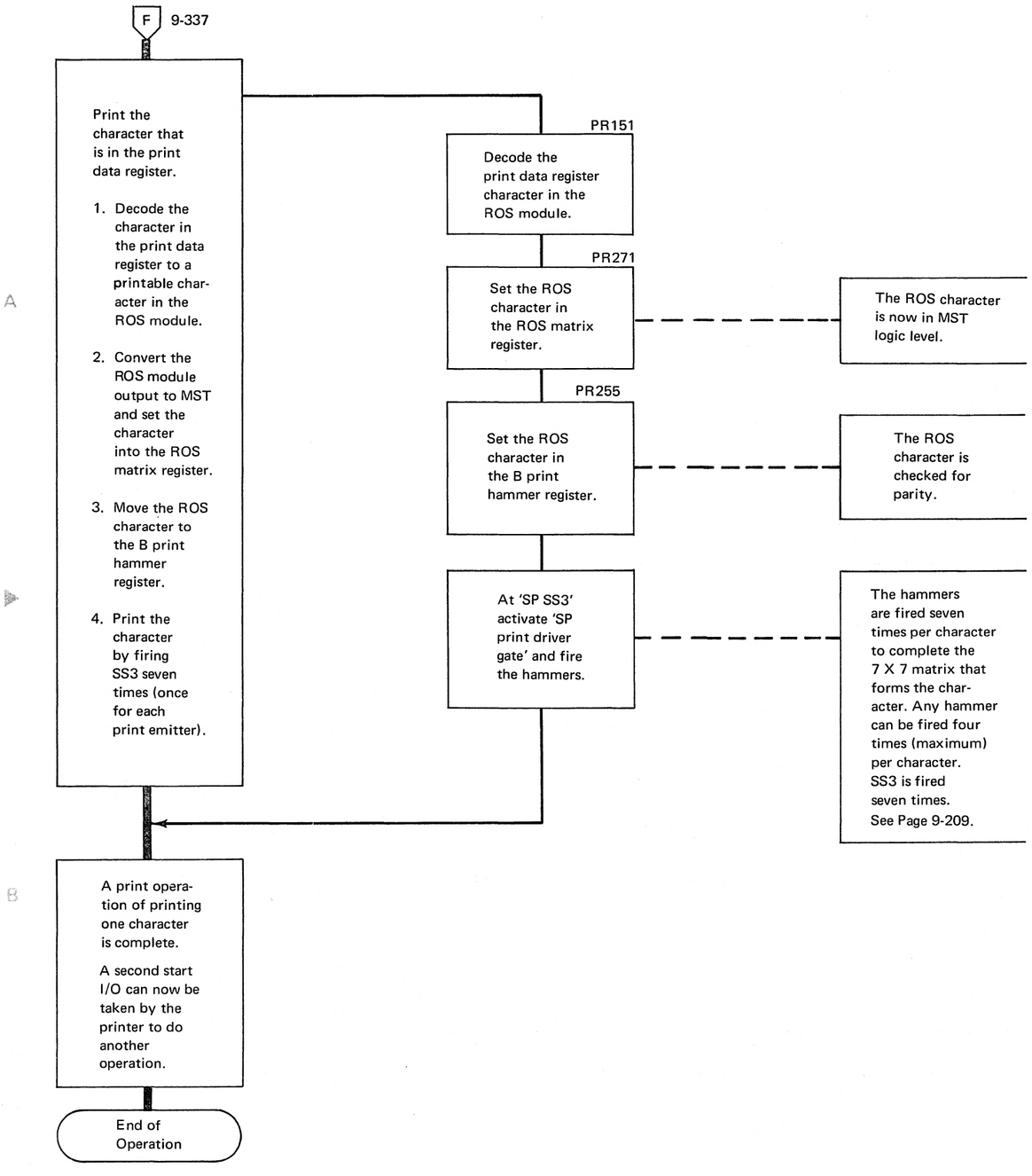

1
2
Secondary Index Operation
The secondary index operation advances the forms in the secondary carriage to the next row of print as follows:
1. Set the 'sec index' command latch.
2. Fire SS 1.
3. Generate a pulse to pick the motion magnet in the printer.
4. The magnet picks, and advances the forms to the next row to be printed.
5. A response pulse from the motion contact resets the attachment circuitry.
PR222
At 'SP clock 5C' set the 'sec index' latch.
With 'SP DBOR 6' active during a command cycle steal.
PR222
This latch set activates 'SP sec index cmmd', 'SP vert cmmd', and 'SP vert non count cmmd busy'.
PR233
At 'SP clock 6' activate 'SP fire SS 1'.
With 'SP cmmd steal' active.
PR112
Fire SS 1. Active for 35 ms. Activate 'SP SS 1'.
A motion contact in the printer must respond prior to SS 1 time out. Otherwise a vertical cycle check will occur.
PR224
At 'SP clock 6' (still during 'SP cmmd cycle steal'), 'SP vert cmmd' sets the 'vert cy inlk' latch.
PR641
'SP sec index cmmd' activates 'SLT 2nd forms magnet'.
This line goes to the printer to pick the forms magnet.
PR021
Receive 'SP sec carr motion cont N-O' from the printer and activate 'SP sec carr motion cont'.
If carriage motion took place.
PR224
Reset the 'vert cy inlk' latch.
Since carriage motion took place we do not have a vertical cycle check.
1
2
A
B


3
1
2
PR222
Reset 'sec index' latch.
End of Operation

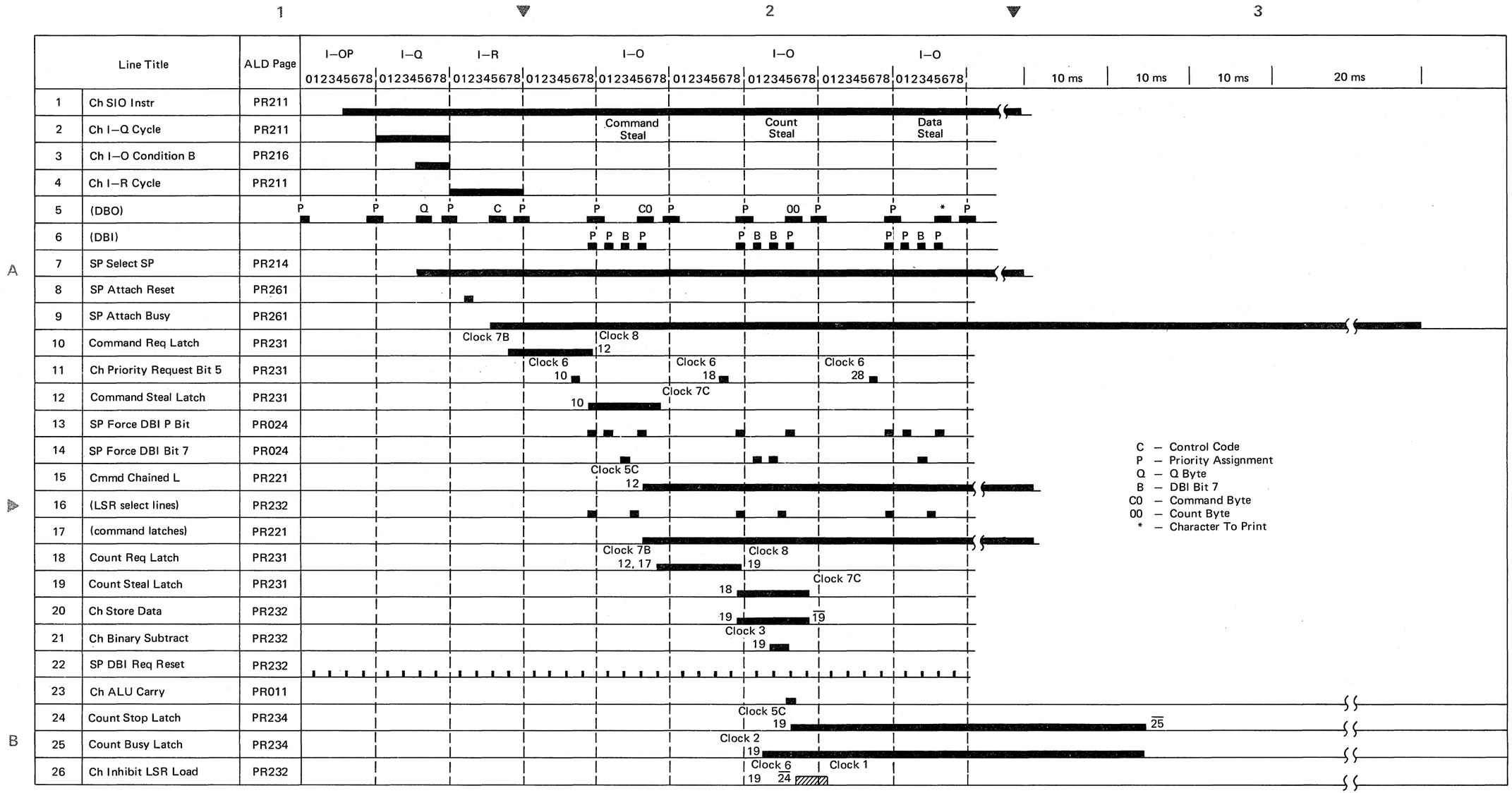

1
2
3
Print Operation
Take two load I/O's to preload the printer LSRs. Page 9-302
One load I/O loads the address of the first character to be printed into PDAR. The second load I/O loads the address of the first command into PCAR.
Take a start I/O to request a cycle steal. Page 9-308
PR212
'Ch data bus out 5' active, and 'ch data bus out P' inactive grants a cycle steal to the printer.
PR212
Activate 'SP decode priority assignment'.
PR231
At 'SP clock 8' this line active, activates 'SP cycle steal honored'.
Select the PCAR to get a command.
PR231
Set the 'cmmd steal' latch.
This latch set activates 'SP format steal' and 'SP cmmd steal'.
PR232
At 'SP clock 8 or 4' activate 'LSR select 4 and 6'.
This line activates the select lines 'ch LSR select 4' and 'ch LSR select 6' to select the PCAR in the CPU to get the command byte.
Set the command latches in the attachment.
Assume the command byte is C0 for a chained print, and the count byte is 00 to print one character.
PR221
At 'SP clock 5C' activate 'SP set cmmd latches'.
PR221
Set the 'prt right' latch with 'SP DBOR 1'.
This latch activates 'SP prt right cmmd' and 'SP count cmmd'.
A 9-337
B 9-337
C 9-337
D 9-337
5. Store the new count byte in main storage (the count byte is FF).
6. Load a new address into the PCAR. If the count byte had not been FF, loading of a new address would have been inhibited. Count cycle steals would have been taken until the count was FF.
7. 'Count stop' is activated and no more count cycle steals are requested.
PR232
At 'SP clock 8 or 4' activate 'LSR select 4 and 6'.
This line activates the select lines 'ch LSR select 4' and 'ch LSR select 6' to select the PCAR in the CPU to get the count byte.
The PCAR in the CPU is selected and the count byte is put in the B register.
PR232
At 'SP clock 1' activate 'SP force DBI bit 7'.
This line active places a 1 in the A register in the CPU.
PR232
At 'SP clock 3' activate 'ch binary subtract'.
Subtract the A register from the B register to reduce the count byte by 1 (from 00 to FF).
PR011
'Ch ALU carry' is activated in the attachment.
Because the count byte has been reduced to FF.
PR234
At 'SP clock 5C' set the 'count stop' and 'cnt end status' latches to activate 'SP count end'.
No more count cycle steals are requested. The PCAR is allowed to advance to the next sequential command.
E 9-337

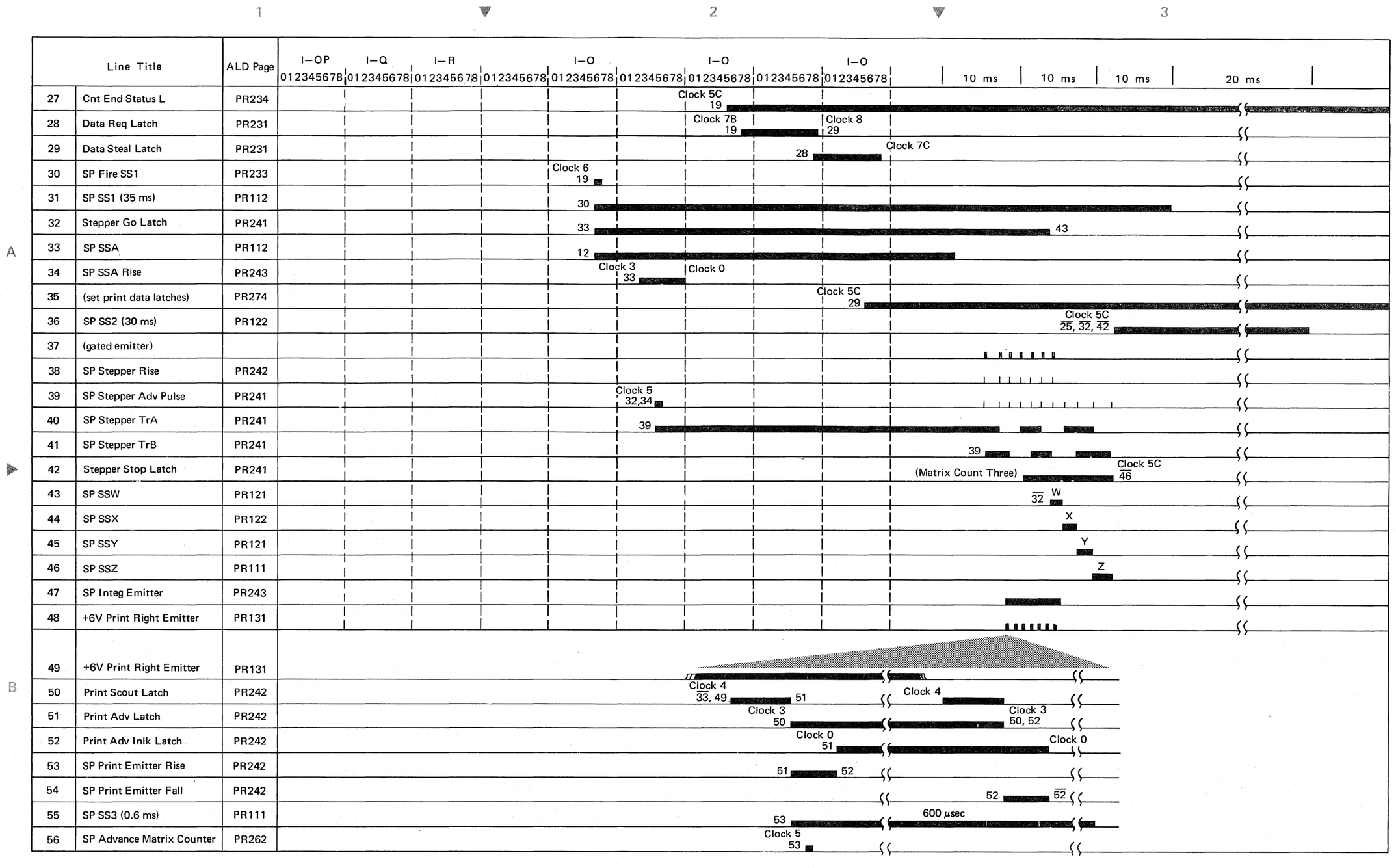


5406 PRINTER ATTACHMENT–Operations
Print Operation (Part 2 of 3)



5406 PRINTER ATTACHMENT–Operations
Print Operation (Part 3 of 3)


1
2
3
Line Title
ALD Page
I–OP
I–Q
I–R
I–O
I–O
I–O
012345678
10 ms
10 ms
10 ms
20 ms
1 Ch SIO Instr PR211
2 Ch I–Q Cycle PR211
3 Ch I–O Condition B PR216
4 Ch I–R Cycle PR211
5 (DBO) P P Q P C P P C0 P P 00 P P * P
6 (DBI) P P B P P B B P P P B P
A
7 SP Select SP PR214
8 SP Attach Reset PR261
9 SP Attach Busy PR261
10 Command Req Latch PR231 Clock 7B Clock 8 12
11 Ch Priority Request Bit 5 PR231 Clock 6 10 Clock 6 18 Clock 6 28
12 Command Steal Latch PR231 Clock 7C 10
13 SP Force DBI P Bit PR024
14 SP Force DBI Bit 7 PR024
15 Cmmd Chained L PR221 Clock 5C 12
16 (LSR select lines) PR232
17 (command latches) PR221
18 Count Req Latch PR231 Clock 7B 12, 17 Clock 8 19
19 Count Steal Latch PR231 Clock 7C 18
20 Ch Store Data PR232 19 19
21 Ch Binary Subtract PR232 Clock 3 19
22 SP DBI Req Reset PR232
23 Ch ALU Carry PR011
24 Count Stop Latch PR234 Clock 5C 19 25
B
25 Count Busy Latch PR234 Clock 2 19
26 Ch Inhibit LSR Load PR232 Clock 6 19 24 Clock 1
Command Steal
Count Steal
Data Steal
C – Control Code
P – Priority Assignment
Q – Q Byte
B – DBI Bit 7
C0 – Command Byte
00 – Count Byte
* – Character To Print



	Line Title	ALD Page
27	Cnt End Status L	PR234
28	Data Req Latch	PR231
29	Data Steal Latch	PR231
30	SP Fire SS1	PR233
31	SP SS1 (35 ms)	PR112
32	Stepper Go Latch	PR241
33	SP SSA	PR112
34	SP SSA Rise	PR243
35	(set print data latches)	PR274
36	SP SS2 (30 ms)	PR122
37	(gated emitter)	
38	SP Stepper Rise	PR242
39	SP Stepper Adv Pulse	PR241
40	SP Stepper TrA	PR241
41	SP Stepper TrB	PR241
42	Stepper Stop Latch	PR241
43	SP SSW	PR121
44	SP SSX	PR122
45	SP SSY	PR121
46	SP SSZ	PR111
47	SP Integ Emitter	PR243
48	+6V Print Right Emitter	PR131
49	+6V Print Right Emitter	PR131
50	Print Scout Latch	PR242
51	Print Adv Latch	PR242
52	Print Adv Inlk Latch	PR242
53	SP Print Emitter Rise	PR242
54	SP Print Emitter Fall	PR242
55	SP SS3 (0.6 ms)	PR111
56	SP Advance Matrix Counter	PR262

BI-DIRECTIONAL PRINT OPERATION

Printing in bi-directional print mode is accomplished in the same manner as it is in serial print mode. There are two basic requirements that must be met in bi-directional printing. These are:

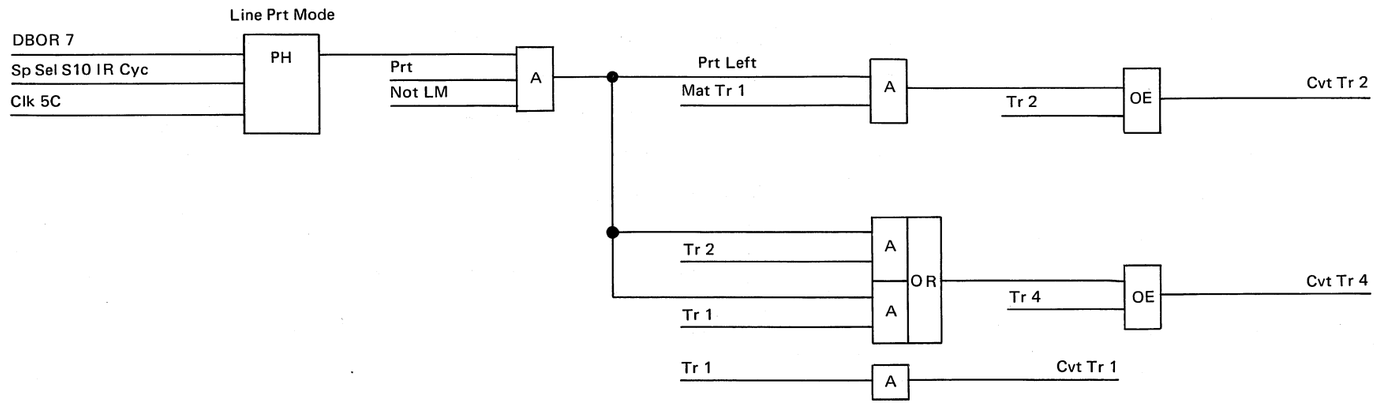
1. All lines to be printed should be of the same length (it is possible with some programs to vary line length).
2. When printing from right to left, the count byte must be added (by the attachment) to the PDAR so that the last character in the data field is printed first.

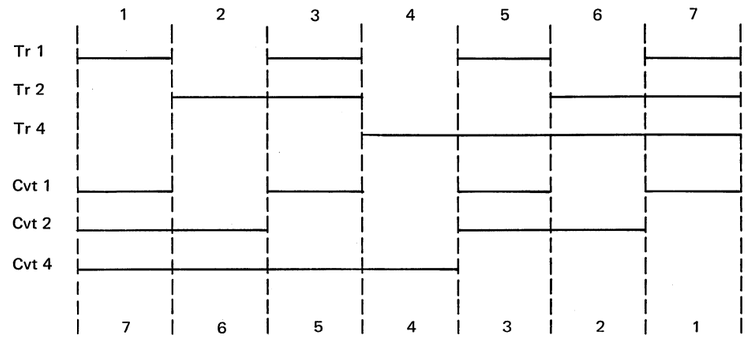
In order to print the last character first (printing right to left only), an initial count cycle steal and data cycle steal are taken. The procedure is as follows:

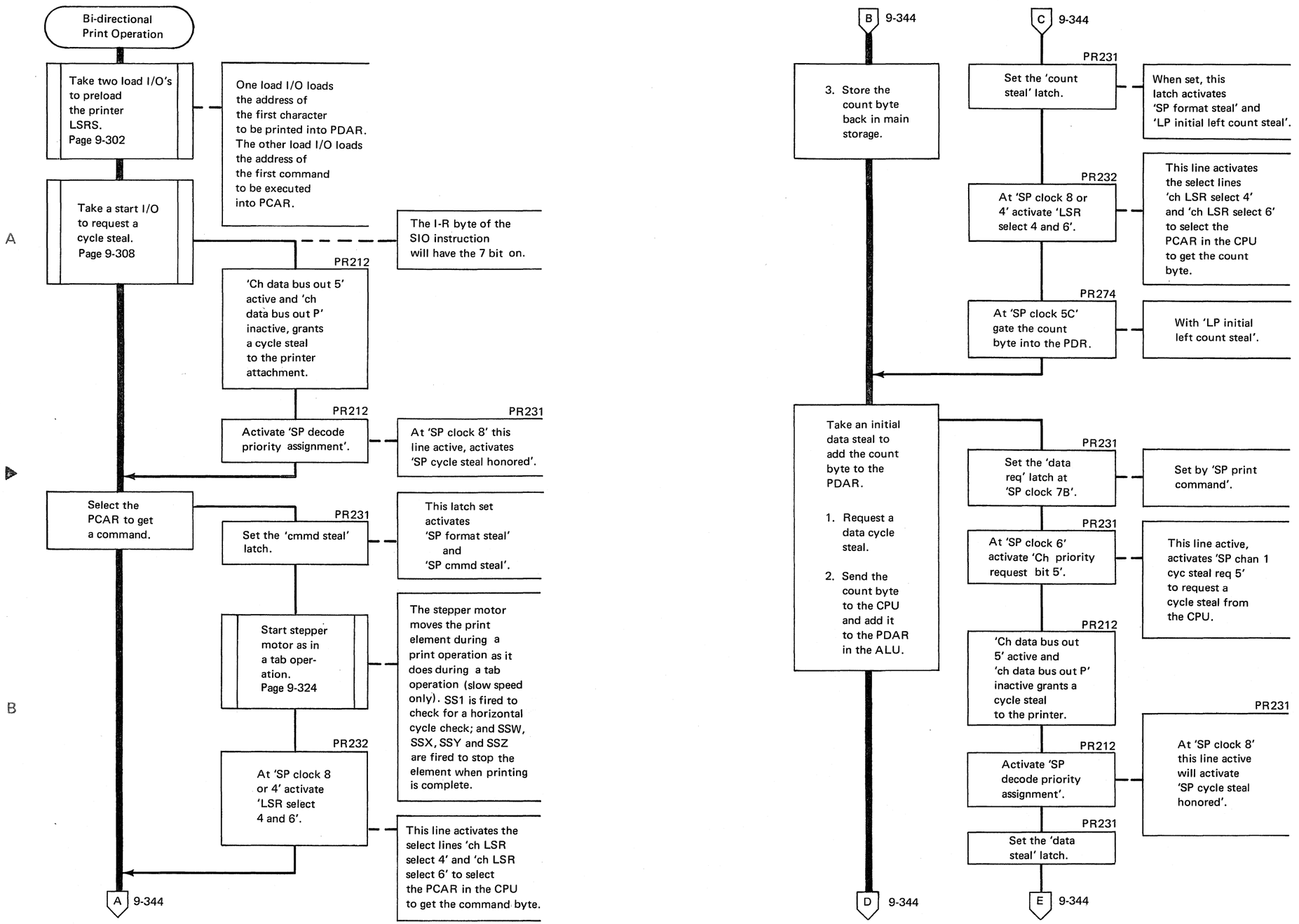
- Take an initial count cycle steal and place the count byte in the print data register in the printer attachment. This count cycle steal is the same as any other count cycle steal except that the count byte is not decremented in the CPU, and that the count byte is brought over to the printer attachment.
- Take an initial data cycle steal and send the count byte from the print data register to the CPU. In the CPU it is added to the PDAR address through the ALU. During this data cycle steal, nothing is brought over to the attachment. The PDAR is not decremented –1, but instead the count byte is added to the contents of PDAR.
- The PDAR is now pointing at the last data character in the print field. When printing begins on a normal count and data cycle steal basis, the last character in the field is printed. The data field is decremented until the count byte goes to FF (data is taken out of storage from right to left, instead of from left to right).

It is important to remember that the above procedure (initialize left operation) takes place only when the print element is at the right hand limit. Also, the right hand limit is variable according to the program. Printing from left to right requires no initial cycle steals.

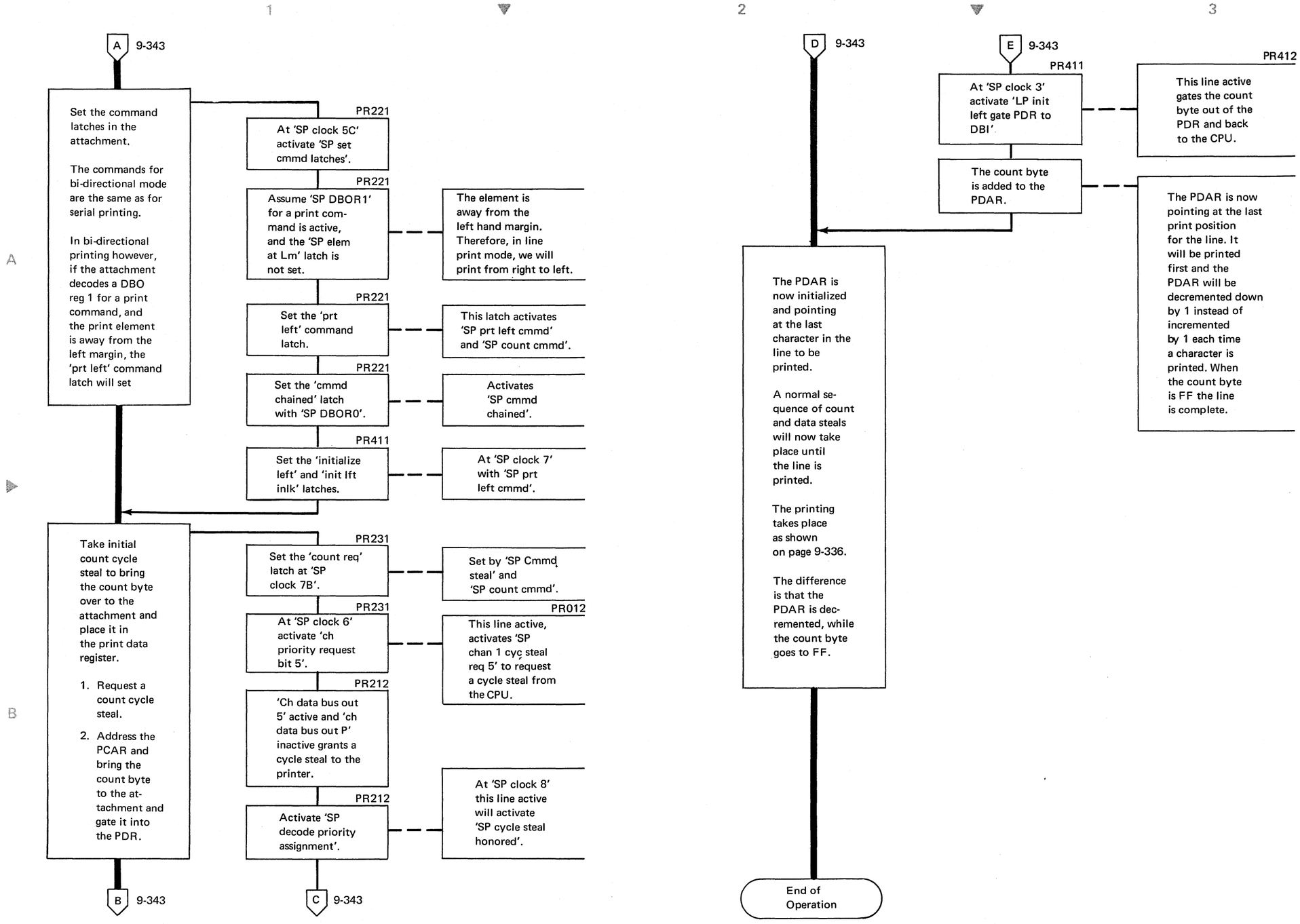
The following flowchart of the bi-directional print operation shows only the initialize left operation. The actual printing and stepper motor operations are the same as shown in the serial print flowchart, except that the matrix counters must be decoded so that line seven prints first in a bi-directional print operation.







5406 PRINTER ATTACHMENT–Operations
Bi-directional Print Operation (Part 2 of 3)


1
2
3
A
B
A 9-343
Set the command latches in the attachment.
The commands for bi-directional mode are the same as for serial printing.
In bi-directional printing however, if the attachment decodes a DBO reg 1 for a print command, and the print element is away from the left margin, the 'prt left' command latch will set
PR221
At 'SP clock 5C' activate 'SP set cmmd latches'.
PR221
Assume 'SP DBOR1' for a print command is active, and the 'SP elem at Lm' latch is not set.
The element is away from the left hand margin. Therefore, in line print mode, we will print from right to left.
PR221
Set the 'prt left' command latch.
This latch activates 'SP prt left cmmd' and 'SP count cmmd'.
PR221
Set the 'cmmd chained' latch with 'SP DBOR0'.
Activates 'SP cmmd chained'.
PR411
Set the 'initialize left' and 'init lft inlk' latches.
At 'SP clock 7' with 'SP prt left cmmd'.
Take initial count cycle steal to bring the count byte over to the attachment and place it in the print data register.
1. Request a count cycle steal.
2. Address the PCAR and bring the count byte to the attachment and gate it into the PDR.
PR231
Set the 'count req' latch at 'SP clock 7B'.
Set by 'SP Cmmd steal' and 'SP count cmmd'.
PR231
At 'SP clock 6' activate 'ch priority request bit 5'.
PR012
This line active, activates 'SP chan 1 cyc steal req 5' to request a cycle steal from the CPU.
PR212
'Ch data bus out 5' active and 'ch data bus out P' inactive grants a cycle steal to the printer.
PR212
Activate 'SP decode priority assignment'.
At 'SP clock 8' this line active will activate 'SP cycle steal honored'.
B 9-343
C 9-343
D 9-343
E 9-343
PR411
At 'SP clock 3' activate 'LP init left gate PDR to DBI'.
PR412
This line active gates the count byte out of the PDR and back to the CPU.
The count byte is added to the PDAR.
The PDAR is now pointing at the last print position for the line. It will be printed first and the PDAR will be decremented down by 1 instead of incremented by 1 each time a character is printed. When the count byte is FF the line is complete.
The PDAR is now initialized and pointing at the last character in the line to be printed.
A normal sequence of count and data steals will now take place until the line is printed.
The printing takes place as shown on page 9-336.
The difference is that the PDAR is decremented, while the count byte goes to FF.
End of Operation

1 ▼ 2 ▼ 3

	Line Title	ALD Page	I–OP / I–Q / I–R / I–O / I–O / I–O / I–O / I–O / I–O (0 1 2 3 4 5 6 7 8)
1	Ch SIO Instr	PR211	Clock 5
2	SP Selected SIO I–R Cycle	PR214	Command Steal; Initial Count Steal; Initial Data Steal; Count Steal; Data Steal
3	SP Attach Reset	PR261	Clock 2
4	SP Attach Busy	PR261	Clock 5
5	SP Set Cmmd Req	PR261	Clock 7B
6	Command Req Latch	PR231	Clock 7B 2; Clock 8C
7	Ch Priority Request Bit 5	PR231	Clock 6 6; Clock 6 13; Clock 6 15; Clock 6 17; Clock 6 19
8	SP Cycle Steal Honored	PR231	Clock 8; Clock 8; Clock 8; Clock 8; Clock 8
9	Command Steal Latch	PR231	Clock 8 6; Clock 7C
10	Print Left Latch	PR221	Clock 5C 9
11	Initialize Left Latch	PR411	Clock 7 9, 10; Clock 7 20
12	Init Left Inlk Latch	PR411	Clock 7 11; Clock 3
13	Count Req Latch	PR231	Clock 7B 9; Clock 8C 14
14	Count Steal (initial)	PR231	Clock 8 13; Clock 7C
15	Data Request	PR231	Clock 7B 14; Clock 8C 16
16	Data Steal (initial)	PR231	Clock 8 15; Clock 7C
17	Count Req Latch	PR231	Clock 7B 16; Clock 8C 18
18	Count Steal Latch	PR231	Clock 8 17; Clock 7C
19	Data Request Latch	PR231	Clock 7B 18; Clock 8C 20
20	Data Steal Latch	PR231	Clock 8 19; Clock 7C
21	(gate count into PDR)	PR274	Clock 5C 14
22	(gate count into DBI)	PR251	Clock 3; To Add Count To PDAR
23	SP Force Binary Subt	PR024	To Increment PCAR; Decrements Count Byte; To Decrement PDAR; Clock 5; Clock 7
24	SP Force DBI Bit 7	PR024	Clock 3; Clock 3; Clock 1; Clock 3; Clock 3; Decrements PDAR
25	Ch Inhibit LSR Load	PR232	Clock 6 14; Clock 1; Clock 6 18; Clock 1
26	Ch Store Data	PR232	Clock 8 14; Clock 7C 14; Clock 8 18; Clock 7C 18

LEDGER CARD DEVICE ATTACHMENT

The ledger card device (LCD) attachment contains the logic circuits to control all LCD operations. The LCD attachment responds to LCD program instructions, requests cycle steals from the CPU, controls the resulting I/O cycle, error checks, and provides status information about the LCD attachment to the program.

The LCD attachment is a standard feature for the 2222 Printer. It is located in the printer attachment board (A-A2) and shares considerable circuitry with the printer attachment.

Program instruction format and device codes (E hexadecimal) are the same for both the printer and ledger card device. The M code of an instruction determines the device selection. An M code of 0 selects the printer, and an M code of 1 selects the LCD.

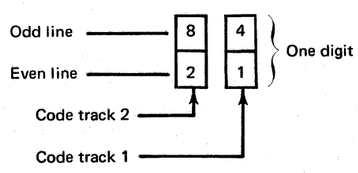
There are three local storage registers used by the LCD attachment, two of the three are shared with the printer.

Ledger Card Format

The ledger card format is shown in the illustration to the right. Print positions 215 through 220 are reserved for line finder and ID number marks. No printing other than these marks should occur beyond print position 214. Marks are printed on the card by the printer under program control. Refer to page 9-102 for further information on print marks. Each printed line must have a line finder mark or the line will be overprinted when the card is reinserted into the LCD.

ID Number

Each digit of the ID number is encoded on the ledger card as a 8-4-2-1 bit code. Bit values are determined by the way they are arranged and printed on the card as shown.



Each digit of the ID number requires two lines to encode it.

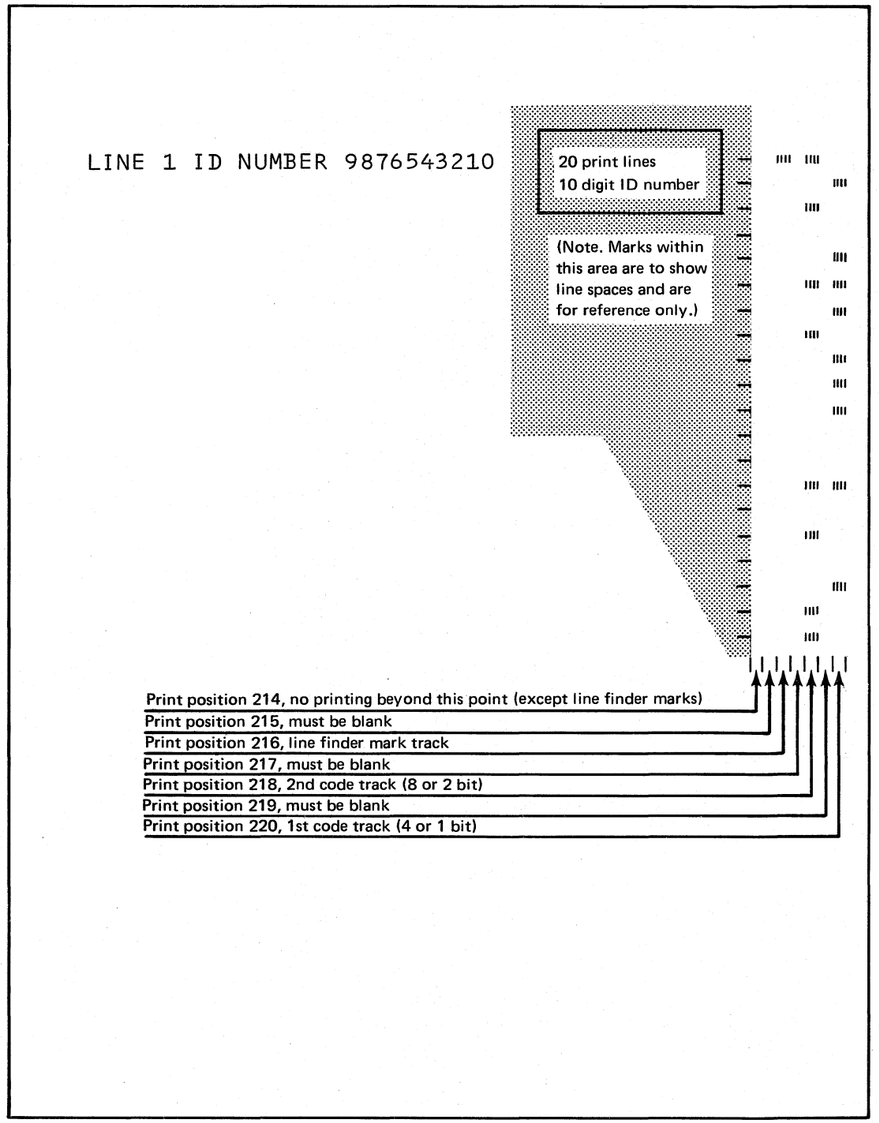
Ledger card dimensions

	Maximum	Minimum
Length	11 inches	8 inches
Width	14 inches	6 inches

Margins

Top	1 inch
Bottom	.833 inches

Ledger card shown printing side up



Indicators and Controls

There is one indicator and one manual control for the LCD. The indicator is the LCD I/O attention light on the keyboard console. It lights when a ledger card can be inserted into the LCD and turns off when the LCD operation starts.

The card eject switch, located on the printer cover (to the right of the LCD input chute), is the only manual control. When the card eject switch is operated, it causes a ledger card in the LCD to be ejected. This switch is interlocked to prevent a manual eject operation if a program initiated operation is in progress at the printer or LCD.

Local Storage Registers

There are three local storage registers assigned to the LCD attachment. They are the print data address register (PDAR), print command address register (PCAR), and the locate line address register (LLAR).

The PCAR and PDAR local storage registers are shared with the printer. If printer and LCD operations are overlapped, care must be exercised to prevent changing an LSR address before an operation is complete. The PDAR contains the address of the main storage location where LCD data (ID number) is stored. The PCAR contains the address of the main storage location where the command field (a control field) for the LCD is located.

The locate line address register (LLAR) is not shared with the printer. This register is used for two LCD operations: feed, read ID, and locate; and index. This register contains the main storage address of a two byte field that is used as two separate decrementing counters. This field is initialized to 110E (hexadecimal) at the start of an LCD operation.

Program Instructions

There are four program instructions for the LCD: load I/O (LIO), test I/O (TIO), sense I/O (SNS), and start I/O (SIO).

Load I/O instructions load the LSRs with an address in main storage where data and control fields for the LCD are located. A control LIO instruction is available for diagnostic testing of the LCD attachment under program control.

Test I/O instructions test the LCD attachment for operation status. It also prepares the LCD to accept a ledger card before an LCD operation is started.

Sense I/O instructions can store the address in an LSR at a main storage location, or sense the error and status conditions in the LCD and transfer the results into main storage.

Start I/O instructions perform only one function, to start an LCD operation. An LCD start I/O instruction does not have any control information to determine what operation the LCD is to perform (except for diagnostic operations). The start I/O causes the LCD attachment to request a cycle steal to obtain the necessary control information from a control field located in main storage.

The format of these instructions is the same as for the printer. Refer to pages 9-105 through 9-109 for further description and format illustrations.

Ledger Card Device Operations

The LCD can perform the following six operations.

- Feed, read ID, and locate next print line
- Feed, read ID, and eject
- Read all line finder marks
- Read back and eject
- Index
- Eject

Feed, Read ID, and Locate Next Print Line

This operation causes the LCD to:

1. Feed the ledger card into the LCD.
2. Read the ID number from the ledger card and transfer it into main storage.
3. Feed the ledger card until the next available print line is positioned at the printer platen and stop the card feed.

Feed, Read ID, and Eject

This operation causes the LCD to:

1. Feed the ledger card into the LCD.
2. Read the ID number from the ledger card and transfer it into main storage.
3. Feed the ledger card through the LCD and eject it into the LCD stacker.

Read All Line Finder Marks

This operation causes the LCD to:

1. Feed a ledger card into the LCD.
2. Read the line finder marks (if any) printed on the ledger card. Each mark is read twice, once as it passes the lower sense station (sense cell 3) and again when it passes the upper sense station (sense cell 4).
3. Generate a data byte for each two lines read from the card. By bit assignments within each byte, indicate if a line finder mark was read and what sense station it was read from. Transfer the data byte to main storage.

Read Back and Eject

This operation causes the LCD to:

1. Start ejecting the card from the LCD. (Note, the card was stopped with the last printed line positioned at the platen when this operation started.)
2. Read the line finder mark that was located at the platen when this operation started as it passes sense cell 4.
3. Indicate if the line finder mark was read by (1) ejecting the card from the LCD, or (2) if the line finder mark was not read, stop the LCD feed and indicate a read mark check.

Index

This operation causes the LCD to move the ledger card to the next sequential print line.

Eject

This operation causes the ledger card to eject from the LCD into the LCD stacker.

A *programmed* eject is started when an LCD start I/O instruction is issued and the command field in core is an eject.

A *manual* eject is started when the card eject switch is operated. This operation can not be started if a program initiated operation is in progress at the printer or LCD.

The card eject switch must be held in its operated position to eject the card. The manual eject operation will stop as soon as the switch is released.

Commands

LCD operations are not performed directly by issuing program instructions to the LCD attachment. All LCD operations are divided into one or four smaller instructions referred to as commands. Commands are one byte in length and are located in main storage. The command or group of commands required to perform one operation is referred to as a command field. The address where the first byte of the command field is located in main storage is loaded into the PCAR LSR, before the beginning of an LCD operation.

Some commands require an additional control byte, called a count byte. Count bytes are used as a decrementing counter and determine how long a command instruction is to be executed. If a count byte is required, it must immediately follow the command byte it is associated with.

Commands are accessed by the LCD attachment by requesting cycle steals from the CPU and addressing the LSR (PCAR) that contains the command field address. As each command enters the LCD attachment, it sets a register that gates the attachment to control the LCD and perform the command. If the command has a count byte, the LCD attachment executes the command until the count byte decrements to FF (hexadecimal). Each byte in the command field is executed, in sequence, by the LCD attachment until the end of the command field is reached.

There are eight LCD commands. Their bit codes, the function they perform, and if they require a count byte, is shown in the following illustration.

Command name	Bit code	Count byte required and if so, its value.	Function
Eject	00	No	Eject the ledger card from the LCD.
Index	01	No	Move the ledger card to the next sequential print line. If the bottom edge of the ledger card is above the lower sense station, decrement the 0E byte of the 110E field 1 for each index command issued.
Read mark eject	02	Yes—08 (count of 9)	Start the LCD card feed. When the line that was positioned at the printer platen when this command was issued passes sense cell 4, see if a line finder mark was read. If a line finder mark was read, eject the card. If no mark was read, set a read mark check.
Sense amp check	03	Yes—05 (count of 6)	Instructs the LCD attachment to check the lower sense cells in the LCD for an operational status. If they are not functioning correctly, a sense amp check is set.
Card skew check	04	Yes—00 (count of 1)	Instructs the LCD attachment to check sense cells 1, 2, and 3 for an inactive condition. If any of the cells are active after the 7th line feed, set a card skew check.
Locate ID	05	Yes—04 (count of 5)	Instructs the LCD attachment to feed the top edge of the ledger card 6 line spaces above the lower sense station. This moves the top margin of the ledger card above the cells and in a position to start reading the first printed line where the ID number begins.
Read ID and locate	06	Yes—13 (count of 20)	Instructs the LCD attachment to read the 20 line ID number (10 digits) and at the same time, search for missing line finder marks. When 2 missing line finder marks are found in succession, start decrementing the 11 byte of the 110E field at the LLAR address.
Read ID and eject	07	Yes—13 (count of 20)	This operation is the same as read locate except the LCD attachment does not check for line finder marks. The ledger card is ejected after reading the ID number.

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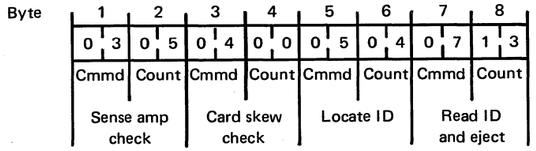
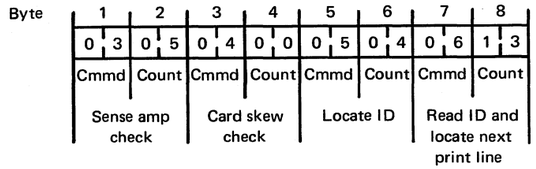
Command Field Formats

The commands required for each LCD operation, their sequence and count byte relationship is shown in the following illustrations. The LCD commands for each operation are fixed and must be issued as shown.

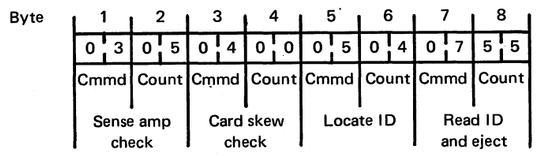
Feed, read ID and eject



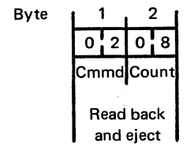
Feed, read ID, and locate next print line



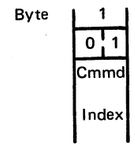
Read all line finder marks



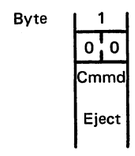
Read mark and eject



Index



Eject



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General Operation of the LCD

The program is responsible for:

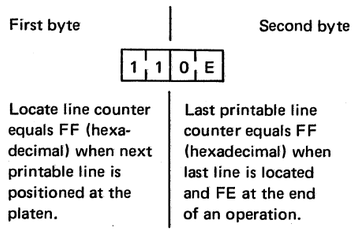
1. Generating the command field for the operation to be performed.
2. Loading the LSRs.
3. Loading the next printable line and the last printable line counters with the 110E value if the operation is a feed, read ID, and locate.

The last program instruction, before starting a feed, read ID, and locate; feed, read ID, and eject; or a read all line finder marks operation, is a TIO for card not aligned. This instruction causes the LCD to raise the card gate and light the LCD I/O attention light on the keyboard console, indicating that a ledger card can be inserted into the LCD. The program will *loop* on the TIO instruction until a ledger card is inserted into the LCD and is aligned at the pinch point of the first feed rolls. When the card is properly aligned within the LCD, the TIO instruction for card not aligned is unconditioned and the program performs an LCD SIO instruction.

One of three operations can be issued to feed the ledger card into the LCD: feed, read ID, and locate next print line; feed, read ID, and eject; or read all line finder marks. Each of these operations synchronizes the LCD attachment, the ledger card, and the LCD with each other when the ledger card is aligned at the first feed rolls in the LCD. From this point on, the LCD attachment is kept in step with the LCD timing pulses received from the LCD. Each timing pulse is generated on a line for line basis. The LCD attachment uses this signal to request cycle steals from the CPU, to access the command field, and to decrement the count bytes. As each count byte is decremented to FF (hexadecimal) the next command byte is accessed. This action continues until the command field has been executed. It is important to recall the mechanical layout of the LCD and the ledger card format to understand the command field function.

Next Printable Line and Last Printable Line Detection

A two byte field, addressed by the LLAR, is used as two separate decrementing counters to detect the next printable line and the last printable line on the ledger card. The format of the field is shown below.



The first byte is the locate line counter and contains the value of 11 (hexadecimal) at the start of an operation. Its purpose is to cause a feed of 18 line spaces after the LCD attachment detects the next available print line.

The reason for this delay is because the lower read station, where the line finder marks are sensed, is 20 line spaces from where the next line should stop at the printer platen. In addition, the LCD attachment must sense 2 missing line finder marks in succession before the attachment recognizes the next printable line. Therefore the locate line counter equals 17 (decimal) to cause a 20 line lapse. (Two lines for missing line finder marks plus one timing pulse to decrement the 11 byte (hexadecimal) to FF.)

The 11 (hexadecimal) value is decremented with each LCD timing pulse, after the two missing line finder marks are detected, until the count becomes FF (hexadecimal). This value generates a control signal to stop the LCD feed. The actual value in byte one will be FE (hexadecimal) when the operation is complete.

The second byte contains the value of 0E (hexadecimal), and is the last printable line counter. When the 0E byte decrements to FF (hexadecimal), it generates a signal that may be sensed with a TIO instruction. When the bottom edge of the ledger card passes the lower read station, the 0E byte is decremented with each timing pulse. In this manner, when 14 line spaces have passed after the bottom of the ledger card was sensed, the last printable line is positioned at the printer platen. (The actual distance between the lower sense station and the platen is 20 linespaces, but allowance must be made for the 5 linespace margin at the bottom of the card plus 1 for decrementing the count to FF.)

Note, the 110E value must not be reinitialized for an index operation because the last printable line count would be invalid.

Line Finder Mark Detection

A line finder mark is printed at the end of each printed line. The LCD attachment uses the absence of line finder marks to detect the next printable line on the ledger card. Two conditions are checked for by the LCD attachment during line finder mark detection.

1. The line finder mark printed at the last printed line on the ledger card should not be late in relation to the LCD emitter pulse. If this condition is detected, an extra line space must be skipped before the ledger card is stopped at the printer platen to prevent overprinting of lines on the ledger card.
2. If an extra line space is skipped because a line finder mark is detected late, the attachment checks that the last printable line has not been detected. This is to prevent the skipped line from being stopped beyond the last available print line on the ledger card. If this condition exists, the ledger card is ejected from the LCD.

Error Detection

The LCD attachment checks for six error conditions during LCD operations. If any of the LCD errors are detected, the LCD card feed is stopped and a status condition is generated to indicate which error occurred. For LCD error conditions and their description, refer to page 9-523.

Chapter 5. LCD Functional Units

This chapter divides the LCD attachment circuits into seven major units.

- LCD pulse generate and sense cell latches
- Command control, diagnostic LIO control, and LCD attachment resets
- DBI assembler and channel in controls
- Cycle steal and LSR selection
- Read ID data assembler
- LCD controls
- LCD attachment error conditions

Each unit contains second level diagrams showing the interconnection with other units and ALD references. Some units contain simplified diagrams and timing charts.

Signal lines on the second level diagrams are labeled to indicate where the signal originates. 9-XXX numbers refer to pages within this manual where the source of the signal is located. PRXXX references are to printer attachment ALDs where the signal is generated but is not shown in this manual. Clock signals are not referenced.

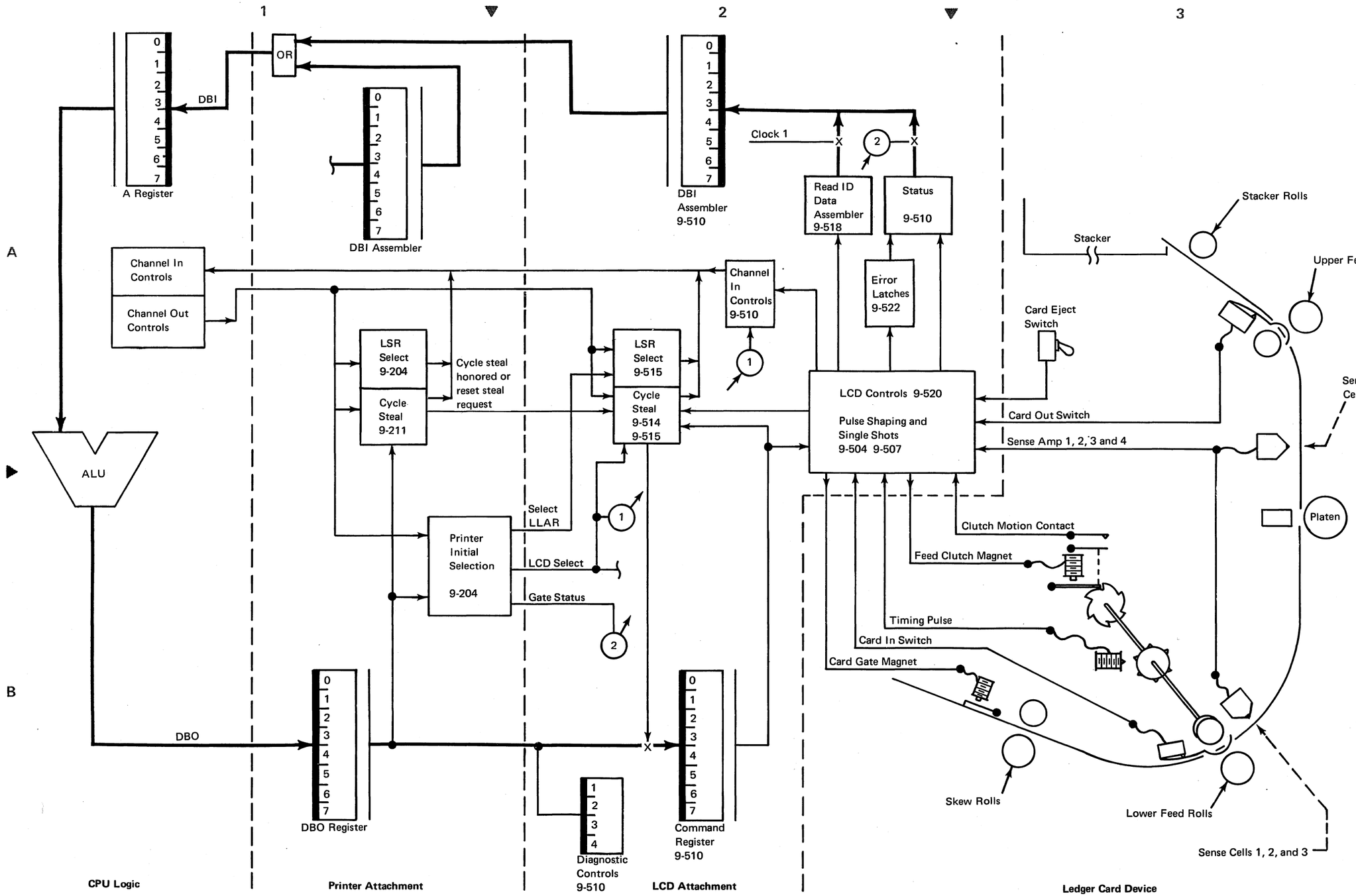
The timing charts are for instructional use only, to show overall signal relationship. For exact timing references, refer to the ALDs.

The complex units are explained in detail. Objectives only are given for units that are basically self-explanatory.

A data flow diagram is included at the beginning of this chapter. It shows the relationship of the functional units and serves as an index to locate the page where the functional unit is described.

Printer circuits that are shared with the LCD attachment are shown in the printer chapters 2 and 3. Refer to pages 9-202, 9-204 and 9-211 for the major units.

Refer to page 9-202 for the LCD and printer attachments board layout.


1
2
3
A
B
0
1
2
3
4
5
6
7
OR
DBI
A Register
DBI Assembler
DBI Assembler 9-510
Clock 1
2
Read ID Data Assembler 9-518
Status 9-510
Channel In Controls
Channel Out Controls
Channel In Controls 9-510
Error Latches 9-522
LSR Select 9-204
Cycle Steal 9-211
Cycle steal honored or reset steal request
LSR Select 9-515
Cycle Steal 9-514 9-515
1
LCD Controls 9-520
Pulse Shaping and Single Shots 9-504 9-507
Card Eject Switch
Stacker Rolls
Stacker
Upper Feed Rolls
Sense Cell 4
Card Out Switch
Sense Amp 1, 2, 3 and 4
ALU
Select LLAR
Printer Initial Selection 9-204
LCD Select
Gate Status
2
Platen
Clutch Motion Contact
Feed Clutch Magnet
Timing Pulse
Card In Switch
Card Gate Magnet
DBO
DBO Register
Diagnostic Controls 9-510
Command Register 9-510
Skew Rolls
Lower Feed Rolls
Sense Cells 1, 2, and 3
CPU Logic
Printer Attachment
LCD Attachment
Ledger Card Device

LCD PULSE GENERATE AND SENSE CELL LATCHES

This functional unit:

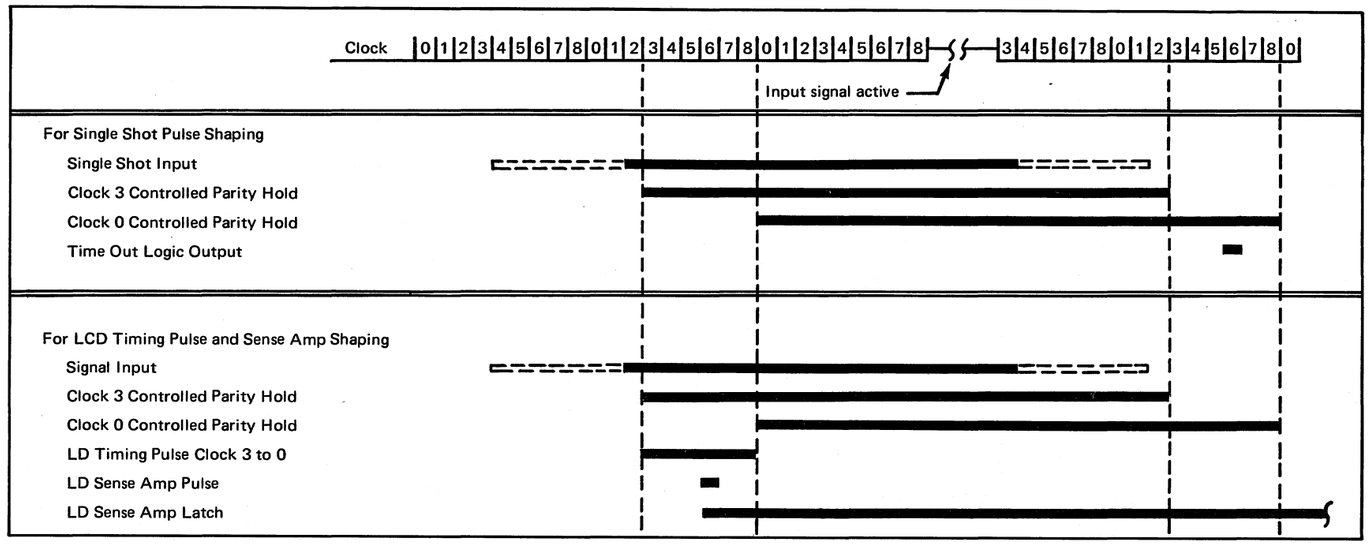
- Receives signals from the LCD.
- Synchronizes and shapes signals for the LCD attachment.
- Detects missing or late line finder marks.
- Generates timing gates.
- Contains the sense cell latches.

Pulse Shaping

Signals from the LCD to the LCD attachment, and LCD single shot output signals are passed through pulse shaping logic. Pulse shaping:

1. Insures an input signal is at least clock 3 through clock 0 time in length to distinguish between a desired signal and electrical noise on the signal line.
2. Synchronizes the input signal to the LCD attachment clock times. This results in the input signal starting and ending at definite clock times.
3. Breaks input signals, that are long in duration, into pulses that indicate a change in signal status.

Each signal line that requires pulse shaping, is fed into a circuit containing two polarity holds. The manner in which the polarity holds operate to shape a signal is shown by the timing chart on this page.



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LCD Emitter Pulse

This signal is generated midway between clutch ratchet teeth whenever the LCD feed clutch is energized. The first emitter pulse occurs approximately 30 ms after the feed clutch is energized and approximately 14 ms thereafter. Timing pulses are shaped by the pulse shaping circuits, and result in a signal that is clock 3 through clock 0 in duration. LCD timing pulses control the LCD attachment on a line for line basis.

Sense Cell Latches

There are four sense cell latches, one for each of the LCD sense cells. These latches are set when a sense cell detects a mark on the ledger card and are reset at the end of each LCD timing pulse.

Single Shots

Six single shots develop timing gates in the LCD attachment. The purpose of each single shot is as follows:

1. *LD stop single shot* produces a pulse 2 ms after each LCD timing pulse. Its output is the LD stop pulse and is the final condition to reset the LCD drive latch and stop the LCD feed clutch.
2. *LD skip line single shot 1* and *LD skip line single shot 2* are used together to generate a gate 10.5 ms after each LCD emitter pulse. This gate conditions the LCD attachment to define any line finder mark sensed after this gate is active, as *late*. LD skip SS1 is fired by each LCD emitter pulse; its only function is to fire LD skip SS2. Two single shots are needed because of single shot recovery requirements.
3. *LD drive check single shot* generates a 45 ms gate to set the drive check latch if an LCD timing pulse is not sensed at the LCD attachment within 45 ms after a feed instruction is issued to the LCD. This is to insure mechanical motion was started after a feed instruction was issued. The LD drive check single shot is fired at the start of each SIO instruction.
4. *LD hold busy single shot* is fired whenever the LCD drive latch is reset. This prevents the LCD attachment busy signal from becoming inactive until 55 ms after an LCD feed operation has ended. This delay is to allow mechanical motion to stop before another operation is issued to the LCD.
5. *LD card alignment single shot* is fired when a ledger card is aligned at the pinch point of the first feed rolls and transfers the card in switch. The card alignment single shot generates a gate to prevent an LCD feed operation from starting until 250 ms after the card in switch has transferred. This is to insure that the ledger card is fully aligned at the pinch point of the first feed rolls before card feed begins.

Line Finder Mark Detection

The latches: late gate, late mark, 1st miss, 2nd miss, and skip line function together to provide line finder mark control to the LCD attachment.

Refer to the timing chart on page 9-505 for the timing relationship of these latches.

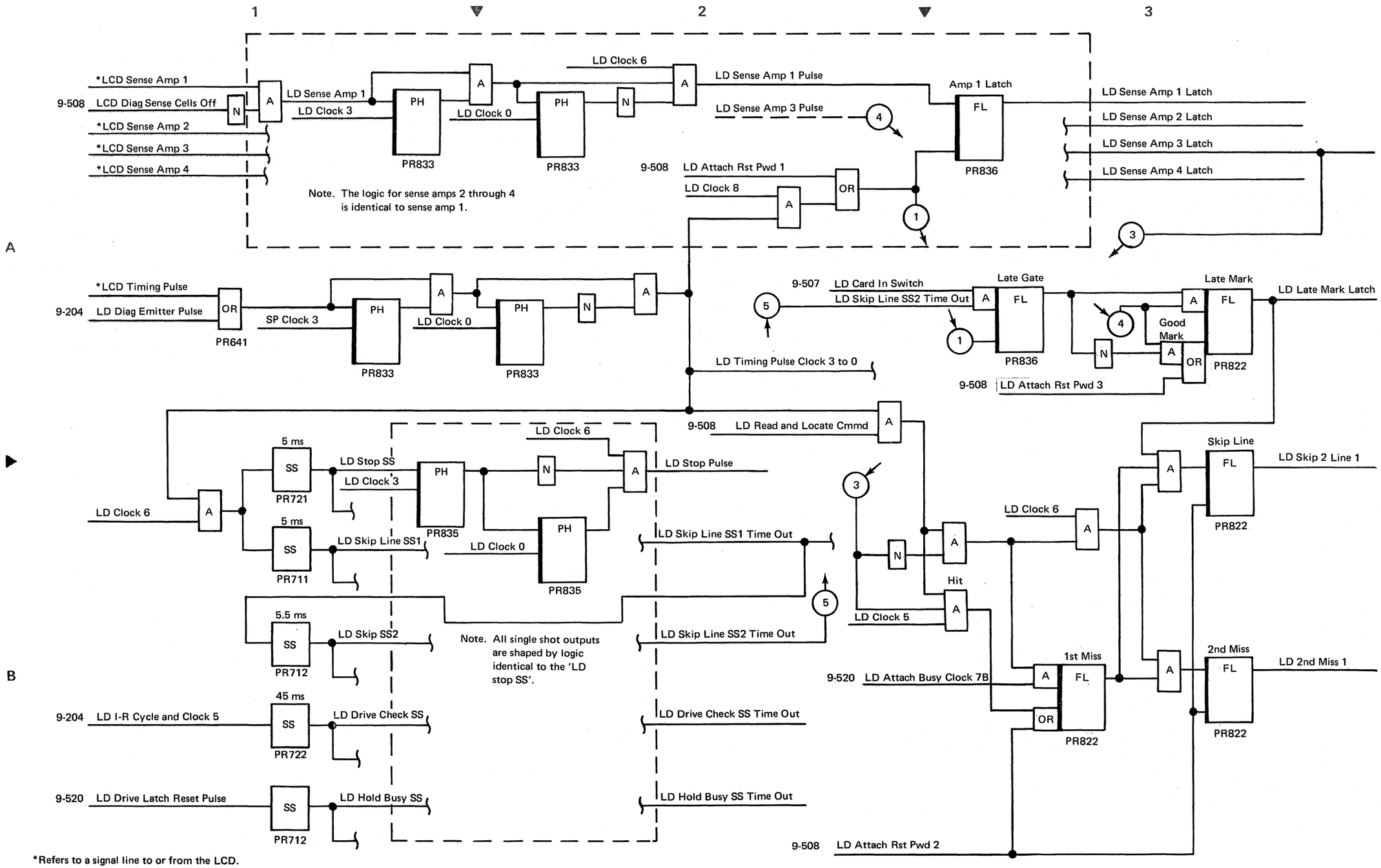
Late gate latch conditions the late mark latch 10.5 ms after each LCD timing pulse. If a line finder mark is sensed before the late gate latch is reset, the late mark latch is set to indicate that a line finder mark was detected late.

First and second miss latches indicate the number of line spaces on the ledger card that were read and no line finder marks were found. Two missing line finder marks in succession is a signal to the LCD attachment to stop the LCD feed after feeding 18 more line spaces. (Unless the last line finder mark was late, feed 19 line spaces before stopping the card feed.) This positions the next printable line on the ledger card at the printer platen. The skip line latch is set, if the last line finder mark read was sensed late to cause the extra line feed.

LCD Card Position Detection

The card-in and card-out switches in the LCD, set latches in the LCD attachment. After pulse shaping, these signals control the LCD attachment in regard to card position within the LCD. 250 ms after the card in switch latch is set, the card alignment latch is set to indicate that a ledger card is positioned at the pinch point of the feed rolls and a card feed operation can begin.

The card gate latch activates the LCD card gate, and controls when a ledger card can be inserted into the LCD. This latch is set by an LCD TIO instruction for card not aligned.



*Refers to a signal line to or from the LCD.

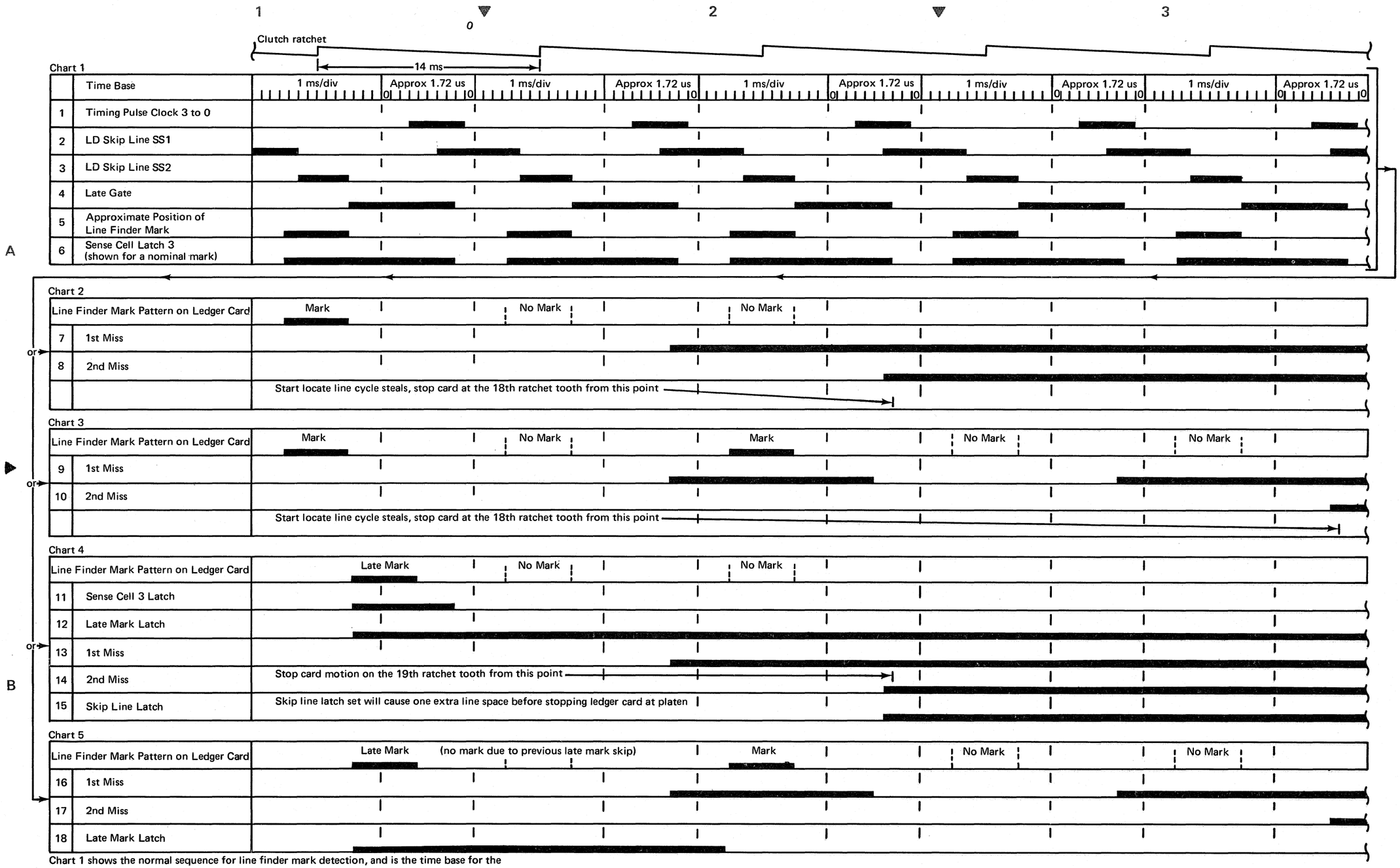
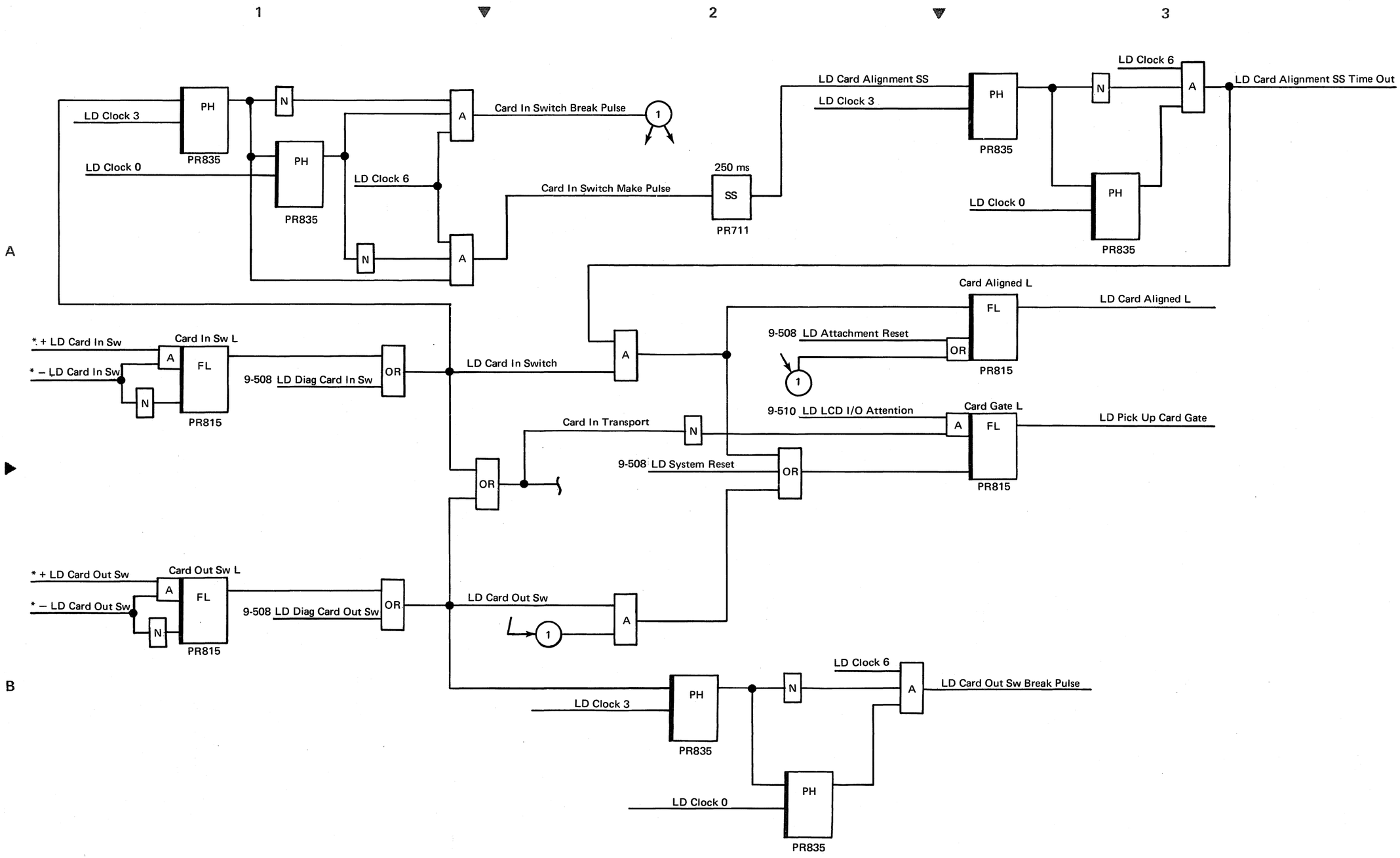
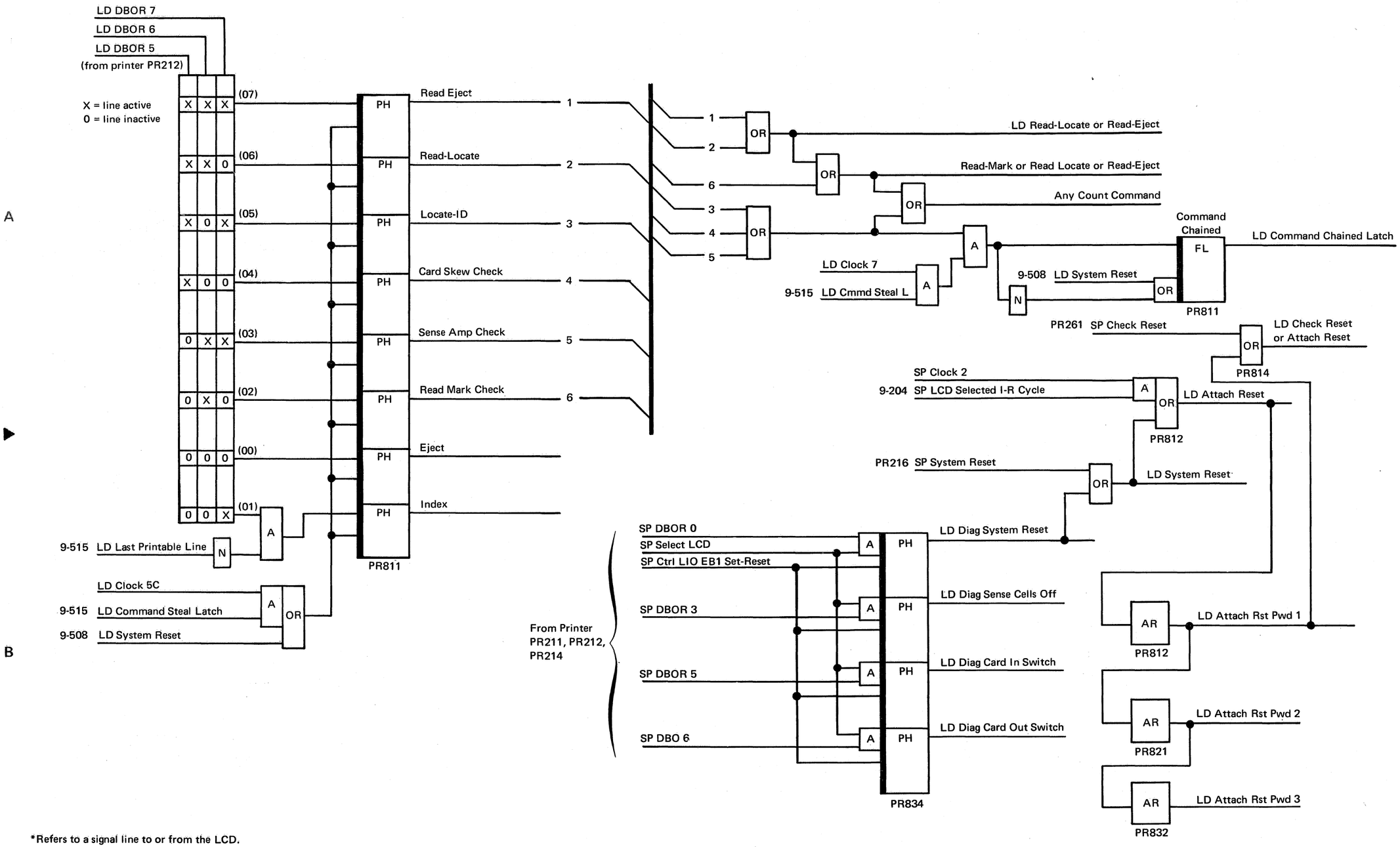


Chart 1 shows the normal sequence for line finder mark detection, and is the time base for the other 4 charts. Charts 2, 3, 4, and 5 are ending sequences for 4 different line finder mark patterns.



*Refers to a signal line to or from the LCD.



*Refers to a signal line to or from the LCD.

COMMAND CONTROL, DIAGNOSTIC LIO CONTROL, AND LCD ATTACHMENT RESETS

This functional unit:

- Contains the command register and its controls.
- Contains the control LIO (diagnostic) register.
- Shows the LCD attachment reset.

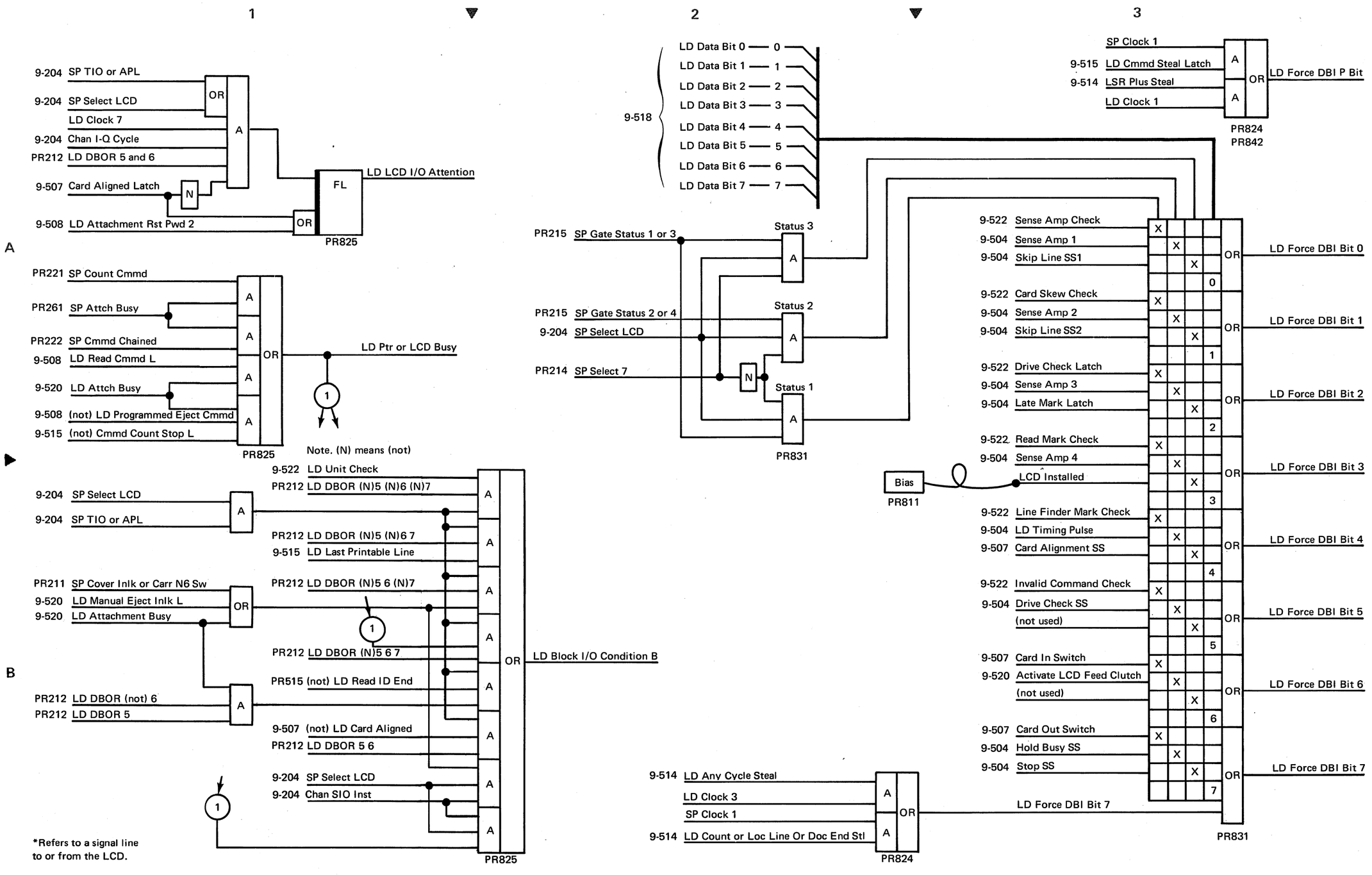
Command Register

- Sets during a command cycle steal when a command byte is on the DBO.
- Output is fed into a decode network to group similar commands, and set the command chained latch if there are additional commands in the command field for the specific operation.
- Gates the LCD attachment to perform one of eight commands.

Diagnostic Control Register and Reset Network

- Sets during the EB1 cycle of a control LIO instruction.
- Simulates LCD attachment signals with polarity holds set from the DBO lines during a control LIO instruction.

The LCD attachment reset network prepares the LCD attachment for an operation by conditioning the latches in the attachment to specific set or reset states.


1
2
3
A
B
9-204 SP TIO or APL
9-204 SP Select LCD
LD Clock 7
9-204 Chan I-Q Cycle
PR212 LD DBOR 5 and 6
9-507 Card Aligned Latch
9-508 LD Attachment Rst Pwd 2
OR
A
N
FL
LD LCD I/O Attention
PR825
PR221 SP Count Cmmd
PR261 SP Attch Busy
PR222 SP Cmmd Chained
9-508 LD Read Cmmd L
9-520 LD Attch Busy
9-508 (not) LD Programmed Eject Cmmd
9-515 (not) Cmmd Count Stop L
LD Ptr or LCD Busy
1
Note. (N) means (not)
9-522 LD Unit Check
PR212 LD DBOR (N)5 (N)6 (N)7
9-204 SP Select LCD
9-204 SP TIO or APL
PR212 LD DBOR (N)5 (N)6 7
9-515 LD Last Printable Line
PR211 SP Cover Inlk or Carr N6 Sw
9-520 LD Manual Eject Inlk L
9-520 LD Attachment Busy
PR212 LD DBOR (N)5 6 (N)7
PR212 LD DBOR (N)5 6 7
PR515 (not) LD Read ID End
PR212 LD DBOR (not) 6
PR212 LD DBOR 5
9-507 (not) LD Card Aligned
PR212 LD DBOR 5 6
9-204 SP Select LCD
9-204 Chan SIO Inst
LD Block I/O Condition B
*Refers to a signal line to or from the LCD.
9-518
LD Data Bit 0 — 0
LD Data Bit 1 — 1
LD Data Bit 2 — 2
LD Data Bit 3 — 3
LD Data Bit 4 — 4
LD Data Bit 5 — 5
LD Data Bit 6 — 6
LD Data Bit 7 — 7
PR215 SP Gate Status 1 or 3
PR215 SP Gate Status 2 or 4
9-204 SP Select LCD
PR214 SP Select 7
Status 3
Status 2
Status 1
PR831
SP Clock 1
9-515 LD Cmmd Steal Latch
9-514 LSR Plus Steal
LD Clock 1
LD Force DBI P Bit
PR824
PR842
9-522 Sense Amp Check
9-504 Sense Amp 1
9-504 Skip Line SS1
LD Force DBI Bit 0
9-522 Card Skew Check
9-504 Sense Amp 2
9-504 Skip Line SS2
LD Force DBI Bit 1
9-522 Drive Check Latch
9-504 Sense Amp 3
9-504 Late Mark Latch
LD Force DBI Bit 2
9-522 Read Mark Check
9-504 Sense Amp 4
LCD Installed
LD Force DBI Bit 3
Bias
PR811
9-522 Line Finder Mark Check
9-504 LD Timing Pulse
9-507 Card Alignment SS
LD Force DBI Bit 4
9-522 Invalid Command Check
9-504 Drive Check SS
(not used)
LD Force DBI Bit 5
9-507 Card In Switch
9-520 Activate LCD Feed Clutch
(not used)
LD Force DBI Bit 6
9-507 Card Out Switch
9-504 Hold Busy SS
9-504 Stop SS
LD Force DBI Bit 7
9-514 LD Any Cycle Steal
LD Clock 3
SP Clock 1
9-514 LD Count or Loc Line Or Doc End Stl
LD Force DBI Bit 7
PR824
PR831

DBI ASSEMBLER AND CHANNEL IN CONTROLS

This functional unit:

- Gates LCD attachment data and status bytes onto the DBI.
- Generates constants for LSR address and storage modification.
- Controls the I/O condition B response to SIO and TIO instructions.
- Controls the LCD I/O attention light on the keyboard console.

CYCLE STEAL AND LSR SELECTION

This functional unit:

- Requests cycle steals from the CPU.
- Selects one of the three LSRs assigned to the LCD attachment.
- Controls the channel ALU binary subtract line.
- Can prevent a constant, placed on the DBI, from modifying an LSR address.
- Indicates when a count byte, or either byte of the 110E field, has decremented to FF.
- Indicates when the last printable line on the ledger card has been detected.
- Indicates when the last count byte of a command field has been processed for the operation in progress.
- Detects when the bottom edge of the ledger card is past the lower sense cells.

Cycle Steal Requests and Cycle Steal Cycles

Cycle steal requests are made by the LCD attachment to access the LCD command field, the LCD data field, and a field that contains two one-byte counters. All fields are located in CPU main storage. The need for an I/O cycle is indicated when the LCD attachment sets a request latch. When the CPU acknowledges the request, a second latch is set in the attachment to gate the use of the I/O cycle. Timing charts showing most of the LCD cycle steal functions may be found on pages 9-516 and 9-517. The purpose of each LCD cycle steal is as follows.

Command Requests and Command Steal Cycles

Command requests are made by the LCD attachment to access the command bytes in the command field and set the LCD attachment command register. During this cycle:

1. The PCAR LSR is selected.
2. When the command byte is on the DBO, set the LCD command register.
3. Check that the command byte is valid.
4. If the command byte is not the last one of the command field, set the command chained latch.
5. Increment the PCAR address by one.

Count Requests and Count Steal Cycles

Count requests are made to decrement the count byte. During this cycle:

1. The PCAR LSR is selected.
2. ALU binary subtract is conditioned to decrement the count byte.
3. Inhibit LSR load is active to prevent the LSR address from incrementing until the count byte decrements to FF.
4. Count end latch is set when the count byte decrements to FF.
5. When the ID field has been read into main storage, a signal is generated to set the condition latch and activate 'LD read ID end.'

(The last two conditions are dependent on the LCD operations being executed.)

Data Requests and Data Steal Cycles

Data requests are made to transfer into main storage (1) an assembled digit of the ledger card ID number or, (2) during a read all line finder marks operation, a byte that indicates the presence of line finder marks. During this cycle:

1. The PDAR LSR is selected.
2. The data byte is gated onto the DBI.
3. PDAR address is incremented by one.

Locate Line Requests and Locate Line Steal Cycles

Locate line requests are made to decrement the 11 byte of the 110E field. When the 11 byte decrements to FF, stop the LCD feed clutch to position the next printable line on the ledger card at the printer platen. During this cycle:

1. The LLAR LSR is selected.
2. Decrement the 11 byte of the 110E field by one.
3. When the 11 byte decrements to FF, set the LLAR equals FF latch, and if the skip line latch is not set, reset the stop latch.

LSR Plus Requests and LSR Plus Cycles, Document End Requests, and Document End Cycles

These requests are always made in sequence. Their purpose is to decrement the 0E byte of the 110E field in order that the last printable line on the ledger card can be detected. During the LSR plus cycle:

1. The LLAR LSR is selected.
2. The LLAR address is incremented by one.
3. Request a document end steal.

During the document end steal:

1. The 0E byte is decremented by one.
2. Set the last line latch if the 0E byte decrements to FF.
3. Decrement the LLAR address by one.

LSR Selection

Cycle steals select an LAR to address one of the three LCD fields in main storage: LSR PCAR address the command field, LSR PDAR addresses the data field, LSR LLAR addresses the field that contains 110E.

Count End Latch

This latch is set whenever a count field has decremented to FF and, depending upon the operation being executed, it may condition the LCD attachment to:

1. Set the last line latch.
2. Set the count stop latch.
3. Decondition the signal 'inhibit LSR load' to allow the address in the selected LSR to increment.
4. Request another command cycle steal.

Inhibit LSR Load

When this signal is active, it prevents the CPU from incrementing the address in the selected LSR. An example would be when a count byte is being decremented, the PCAR address must not be changed until the count byte decrements to FF.

Count Stop Latch

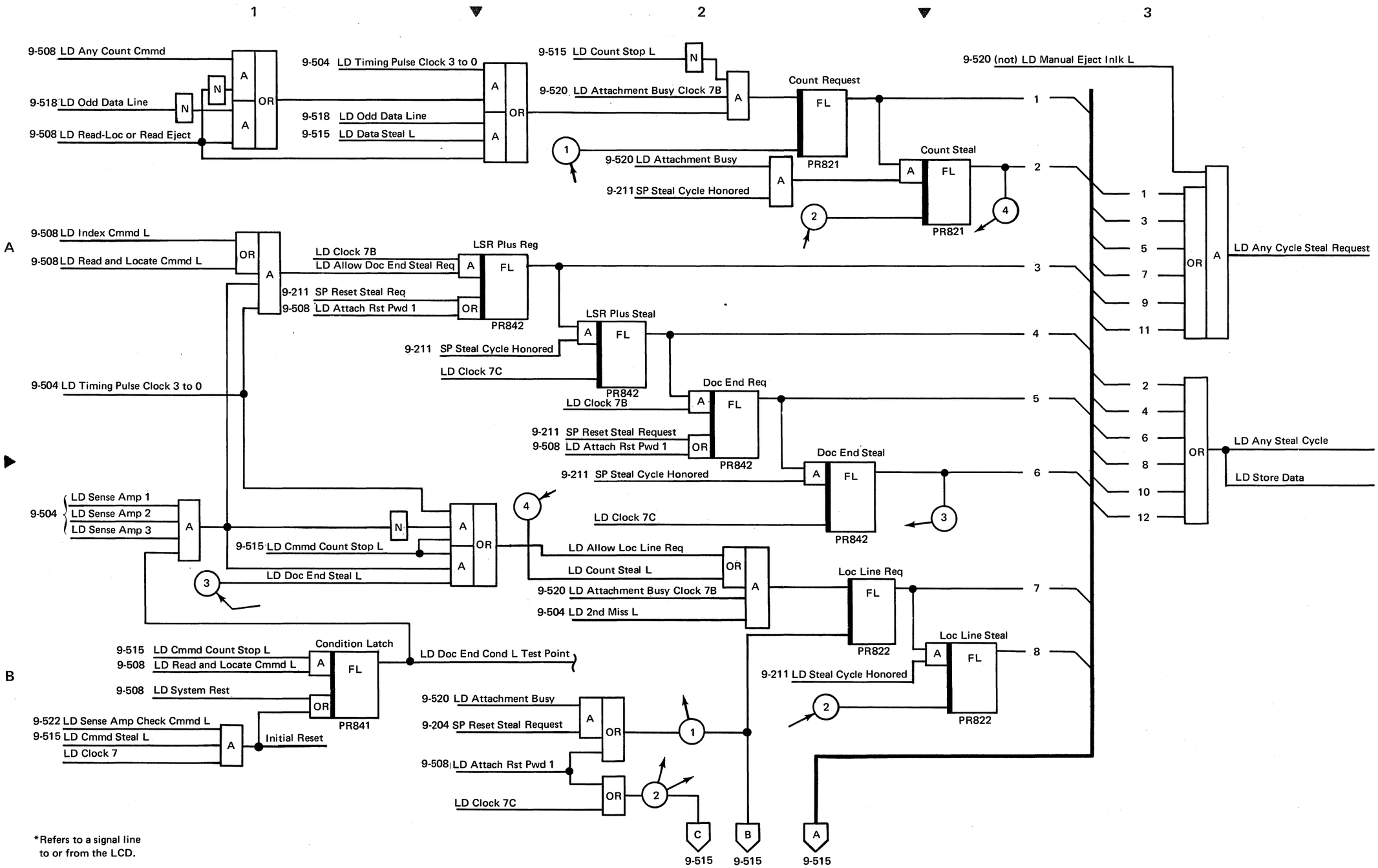
This latch is set when the read locate, read eject, or read mark eject command count byte (byte 8 of the command field) decrements to FF. This signals the end of the command field for feed, read ID, and locate; feed, read ID, and eject; or read all line finder marks operations. The output from this latch is a gate to set the condition latch and is one condition to activate the read ID end signal.

Condition Latch

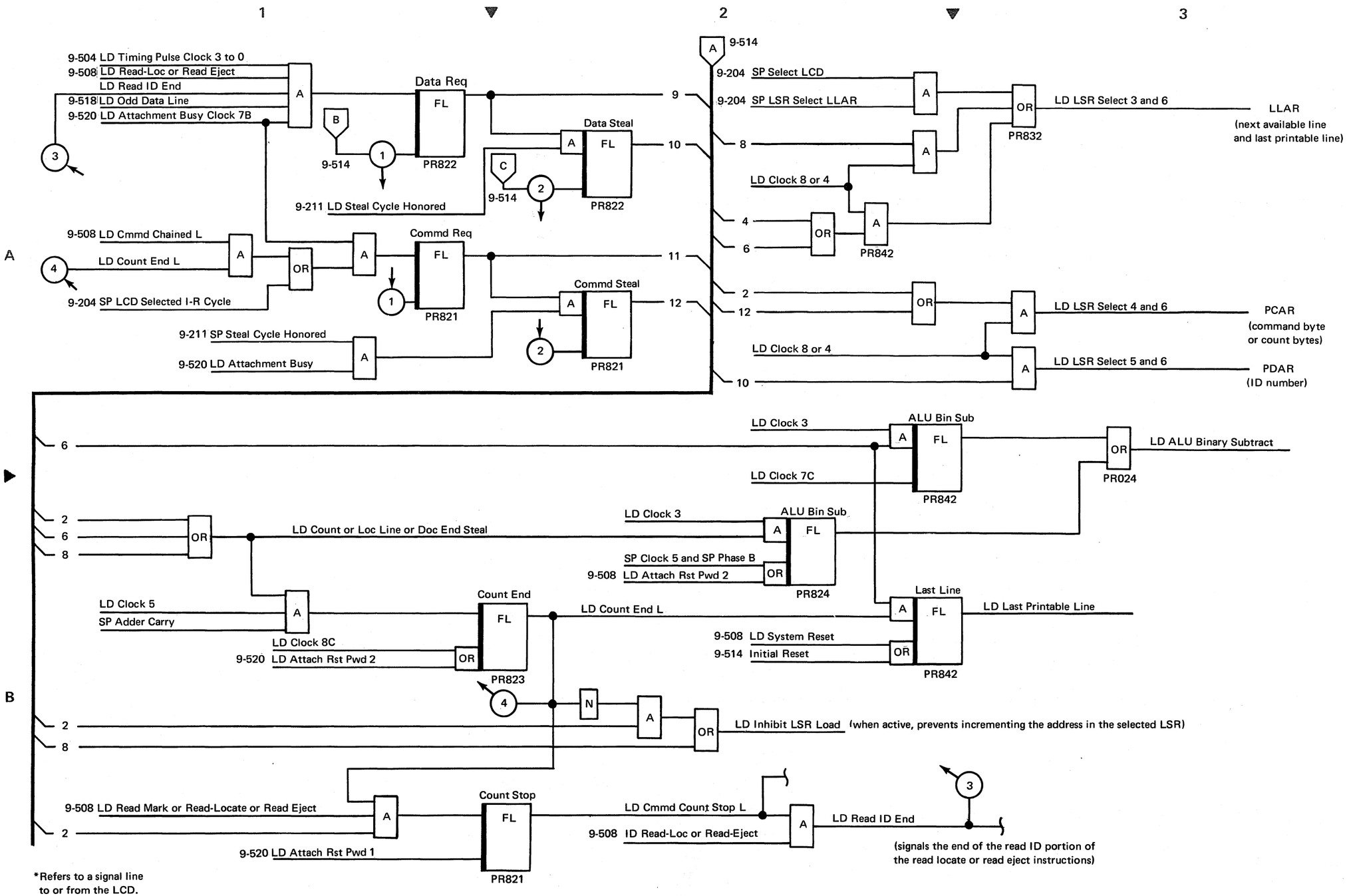
The condition latch determines when to allow LSR plus and document end requests. It is set during a feed, read ID, and locate operation when the count stop latch is set. Note that the condition latch is not reset with the LCD attachment reset signal. This is necessary to prevent the condition latch from resetting when an LCD index operation is issued to the LCD after a feed, read ID, and locate operation.

Read ID End

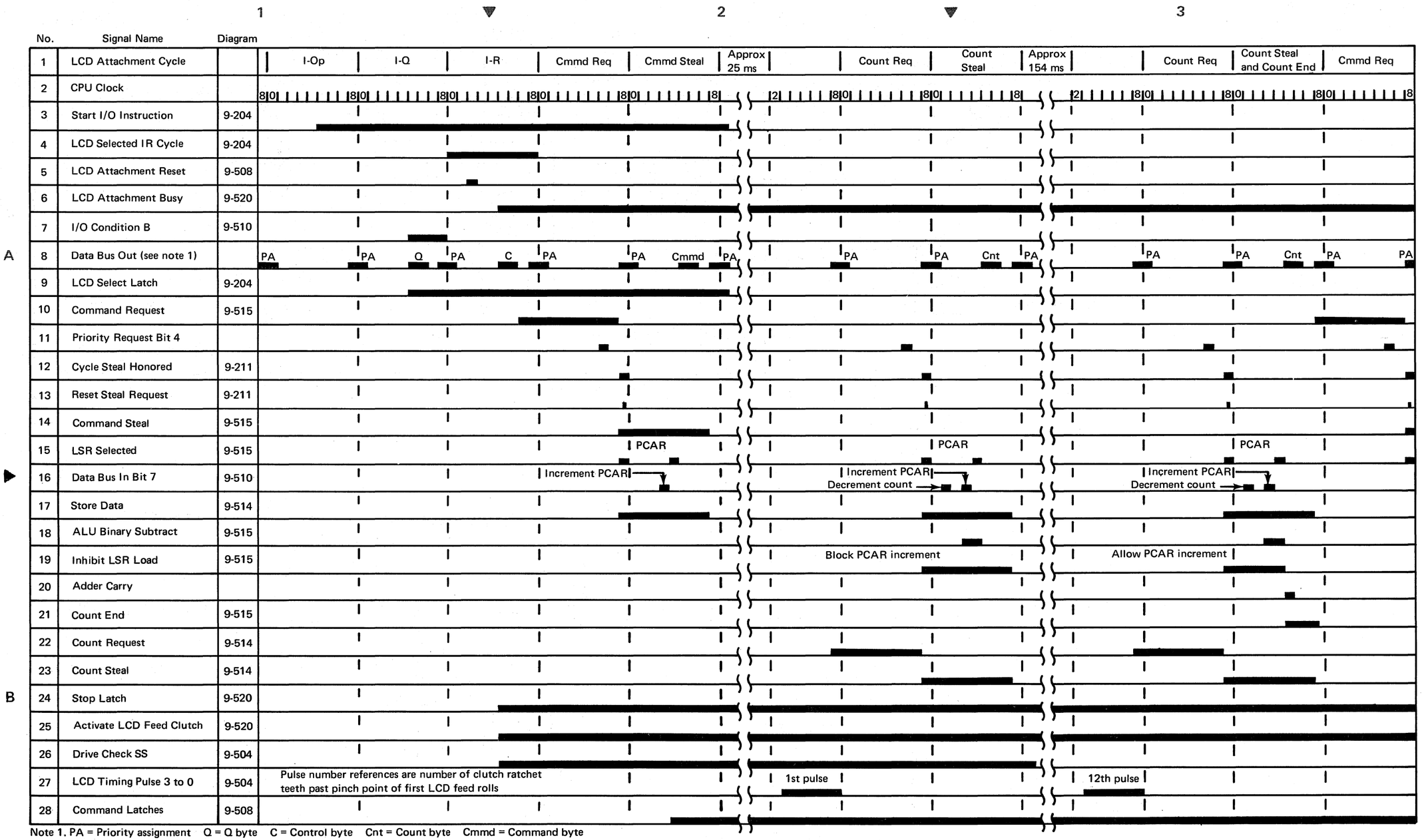
The 'LD read ID' end signal is active when the ID number, read from the ledger card, has been transferred into main storage. It can only be conditioned during two instructions: feed, read ID, and locate; and feed, read ID, and eject. The condition of this signal line determines the LCD attachment response to an LCD TIO read ID busy instruction.



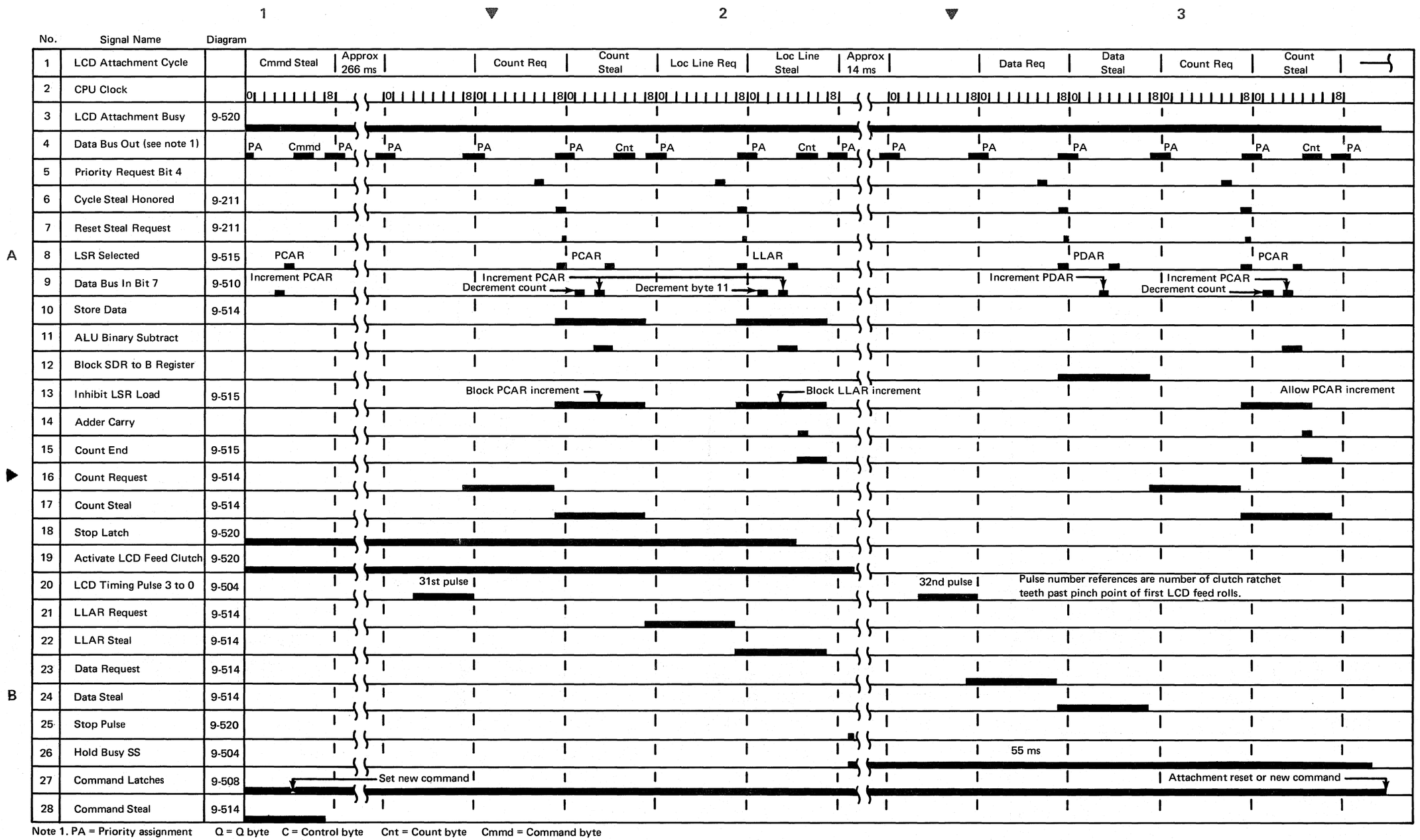
*Refers to a signal line to or from the LCD.



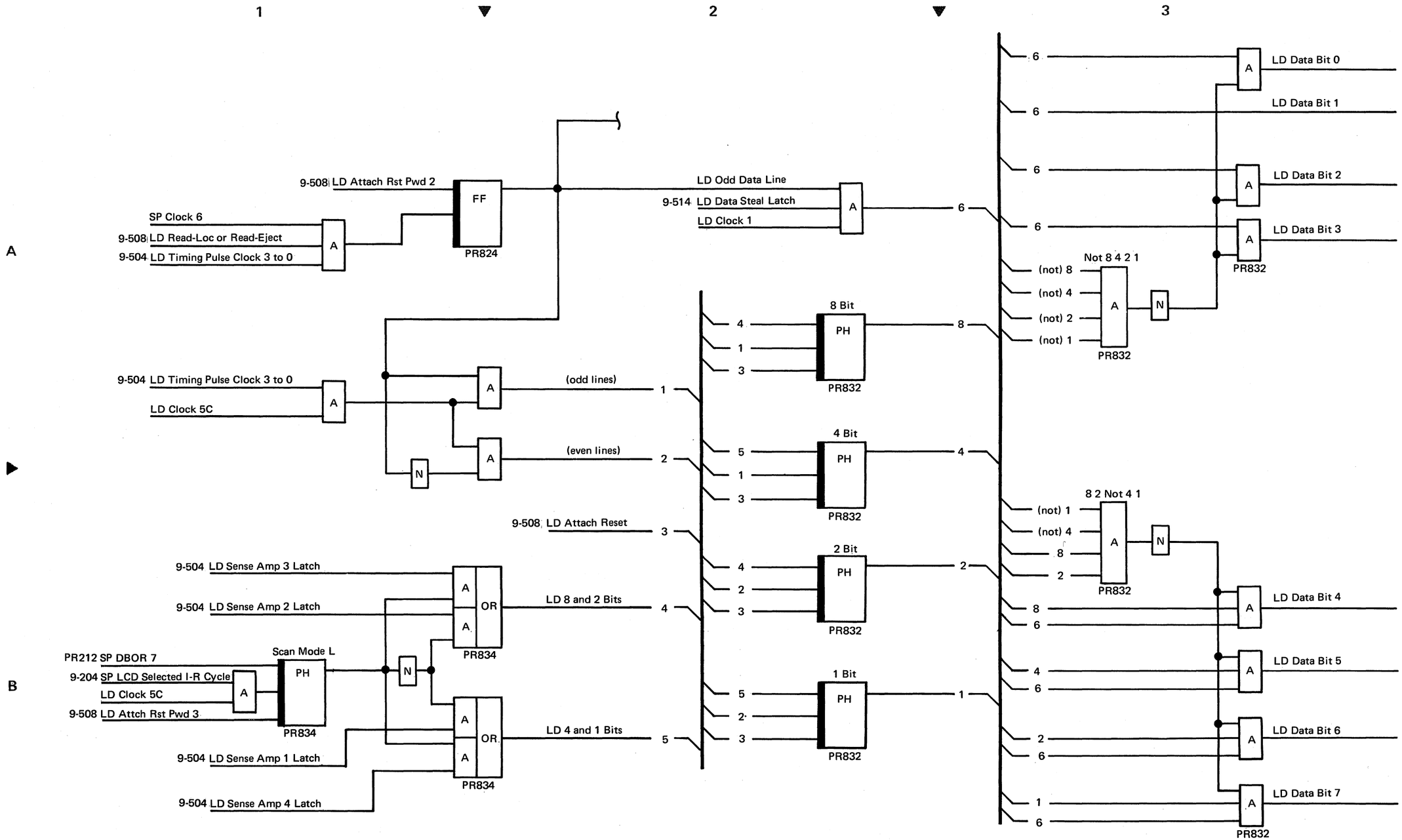
LCD ATTACHMENT–Functional Units
Cycle Steal and LSR Selection (Part 3 of 5)



Note 1. PA = Priority assignment Q = Q byte C = Control byte Cnt = Count byte Cmmd = Command byte



Note 1. PA = Priority assignment Q = Q byte C = Control byte Cnt = Count byte Cmmd = Command byte



*Refers to a signal line to or from the LCD.

READ ID DATA ASSEMBLER

This functional unit:

- Assembles each digit of the ID number into an 8 bit byte.
- Decodes a blank in the ID number to 40 (hexadecimal).
- Decodes digits 0 through 9 in the ID number to F0 through F9 (hexadecimal).
- Operates in one of two modes, normal or diagnostic.

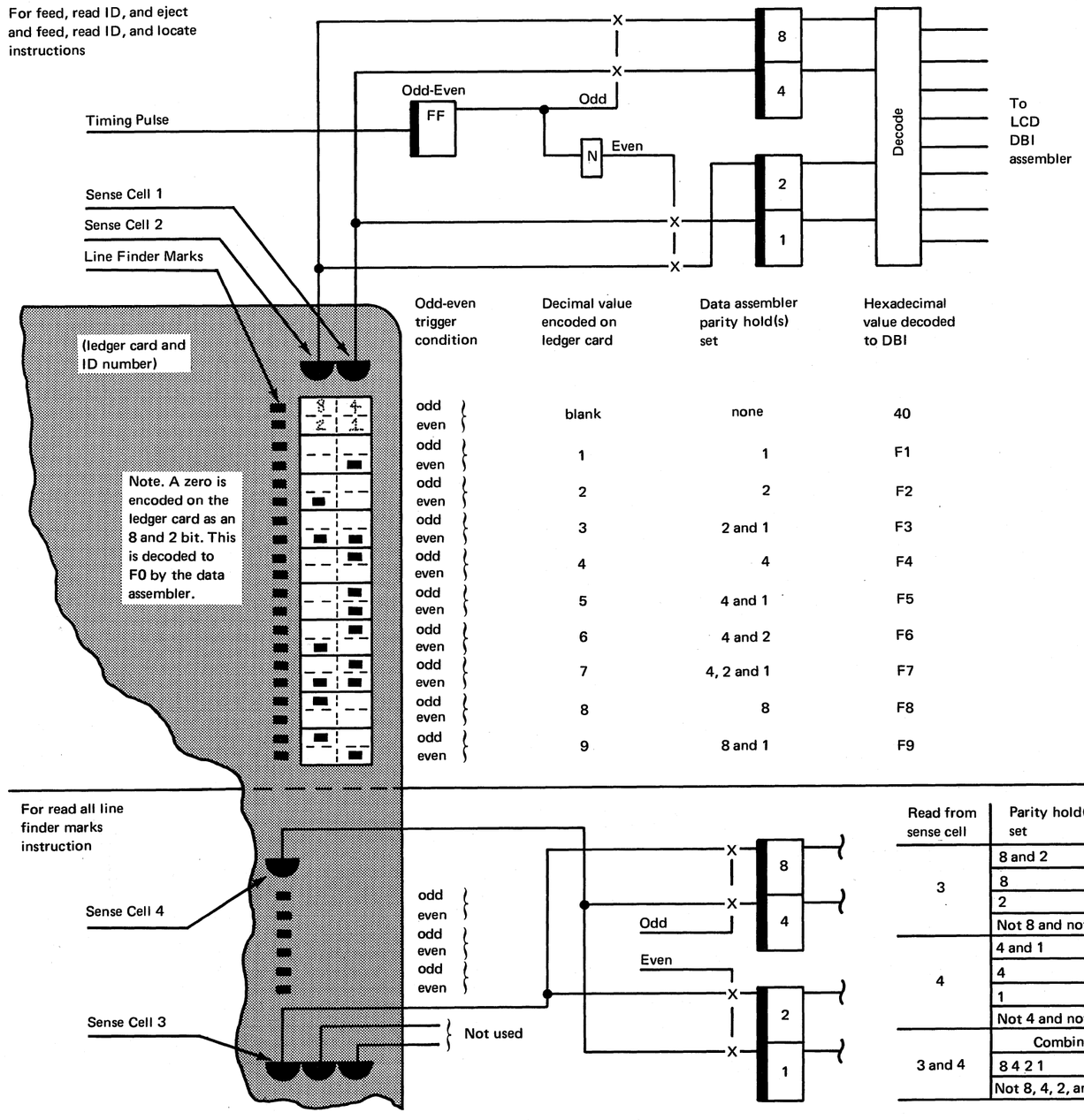
The illustration at the right shows the basic operation of the data assembler. The upper part of the illustration shows how the data assembler functions during feed, read ID, and locate; and feed, read ID, and eject operations. The lower part of the illustration shows the data assembler operation for the read all line finder marks operation.

In the operation shown by the upper part of the illustration:

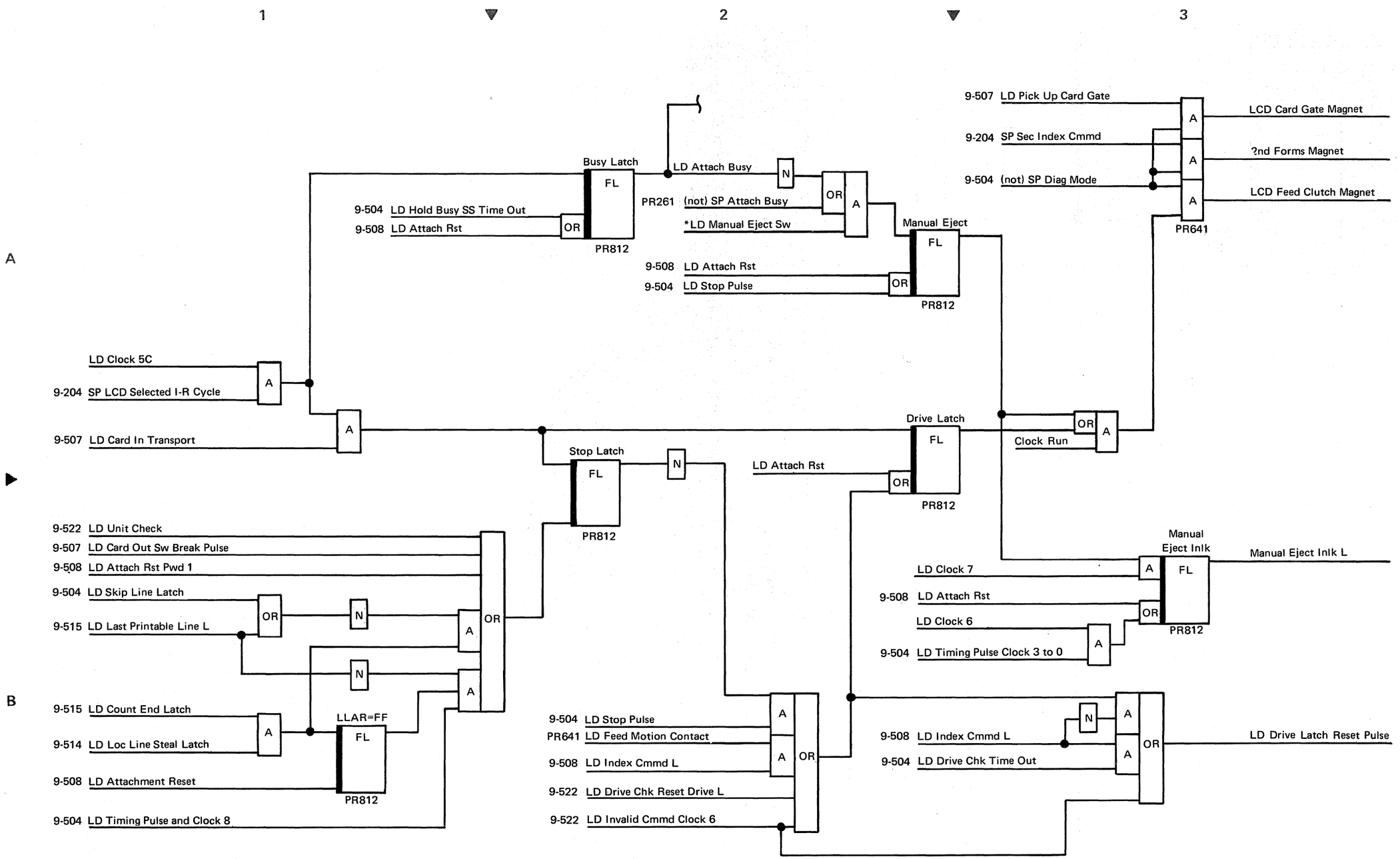
- Two lines are read from the ledger card for each digit in the ID number.
- The 8 and 4 bits are read on odd lines.
- The 2 and 1 bits are read on even lines.
- Marks are read from LCD sense cells 1 and 2.

In the operation shown by the lower part of the illustration:

- The SIO IR cycle set the scan mode latch.
- Line finder marks are read by LCD sense cells 3 and 4.



Read from sense cell	Parity hold(s) set	Decode to
3	8 and 2	FA
	8	F8
	2	F2
	Not 8 and not 2	40
4	4 and 1	F5
	4	F4
	1	F1
	Not 4 and not 2	40
3 and 4	Combinations of above	
	8 4 2 1	FF
	Not 8, 4, 2, and 1	40



*Refers to a signal line to or from the LCD.

LCD CONTROLS

This functional unit:

- Indicates when the LCD attachment is busy.
- Prevents a manual eject operation when the printer or LCD attachment is busy.
- Contains the LCD feed clutch start-stop circuits.

Busy Latch

The busy latch is set at the start of an LCD start I/O instruction and remains set until after an LCD operation ends, and the hold busy single shot times out.

Manual Eject Latch

The manual eject latch prevents the manually operated card eject switch from starting a feed operation whenever the printer or LCD attachment is busy.

Manual Eject Interlock Latch

While performing a manual eject operation, the manual eject interlock latch:

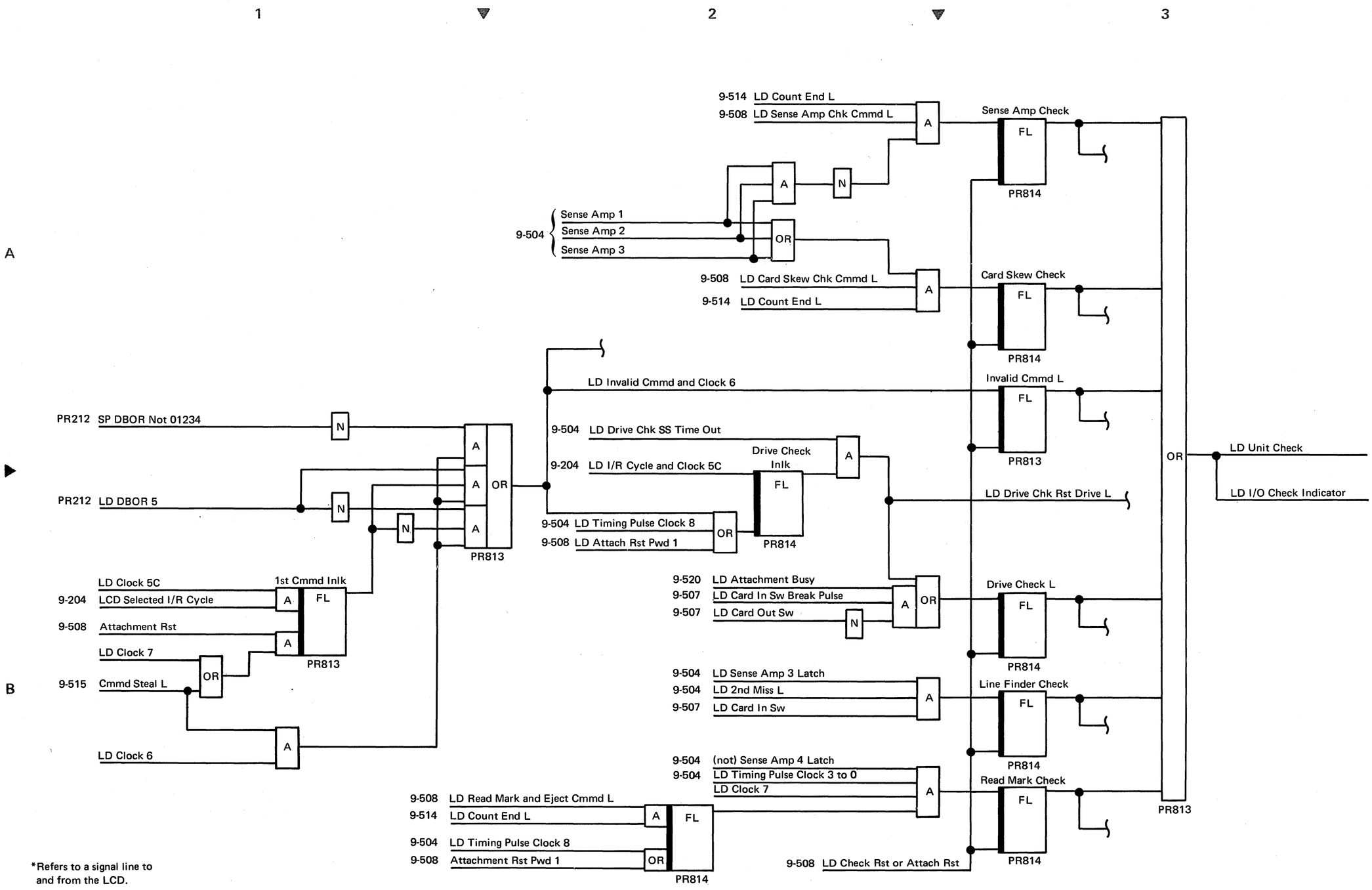
1. Prevents LCD cycle steal requests from reaching the CPU.
2. Blocks the I/O condition B signal to the CPU.

Drive Latch and Stop Latch

The stop and drive latches control the LCD feed clutch magnet. The drive latch is set to activate the clutch magnet and start the LCD drive. To stop a feed operation, two signals are needed. One signal controls when the feed operation should end. The second signal is required to drop the armature into the clutch ratchet (at the proper time) to engage the next clutch ratchet tooth. If this precaution is not observed, the armature could fall too late in relation to the next clutch ratchet tooth, to stop the clutch at the desired line position.

In operation, the LCD attachment resets the stop latch to signal when a feed operation is to end, and allow the next stop pulse (emitter pulse) to reset the drive latch to deactivate the clutch magnet.

For an index operation, the clutch motion contact resets the drive latch, allowing only one line space per index instruction.



*Refers to a signal line to and from the LCD.

LCD ATTACHMENT ERROR CONDITIONS

This functional unit:

- Detects Error conditions.
- Conditions unit check if an error is detected.
- Stops any operation in progress when any error condition is detected.

The LCD attachment checks for proper operation of LCD operations and commands. If an abnormal condition occurs during an operation, one of six error latches is set. Any of the six error conditions will cause a unit check and immediately stops the LCD operation in progress. The LCD check conditions are as follows.

1. *Sense amp check.* This check may be set during the first command for: feed, read ID, and locate; feed, read ID, and eject; and read all line finder marks operations. It insures that sense cells one, two and three are not activated by the leading edge of the ledger card, after the 6th timing pulse of a card feed. Normally the leading edge of the ledger card should cover the lower sense cells 6-1/2 line spaces beyond the pinch point of the first feed rolls.
2. *Card skew check.* This check may be set during the second command for: feed, read ID, and locate; feed, read ID, and eject; and read all line finder marks operations. It insures that the top edge of the ledger card covered the lower sense cells after the 7th line space beyond the pinch point of the first feed rolls. If any sense cell (one, two, or three) is not active, it indicates (1) that the card has not reached the lower read station at the correct time, (2) that the card is skewed in the card path, or (3) one of the sense cells is not functioning correctly.
3. *Invalid command check.* This check may be set during each command steal. It checks for two conditions.
   a. The first byte of any command field must be 00, 01, 02, or 03. The LCD attachment sets the invalid check latch if DBO lines 0, 1, 2, 3, 4, and 5 are active during the first command steal of a command field.
   b. Command bytes 3, 5, and 7 of a command string must be coded 04, 05, 06, or 07. The LCD attachment sets the invalid check latch if DBO line 5 is not active during the 2nd, 3rd, and 4th command steal cycles.
4. *Drive check.* This check indicates that mechanical motion was not started in the LCD after a feed operation was issued. To prevent this check, an LCD timing pulse must be sensed by the LCD attachment within 45 ms after a feed operation was issued to the LCD. At the start of an operation, the drive check interlock latch is set and the drive check single shot is fired. If an LCD timing pulse does not reset the drive check interlock latch before the drive check single shot times out, the drive check latch is set.
5. *Line finder mark check.* This check can be set only during a feed, read ID, and locate next print line operation. It indicates that after two successive line finder marks were found missing (2nd miss latch is set), another line finder mark was sensed at the lower sense station.
6. *Read mark check.* This check can be set during a read back and eject operation. It indicates that the line positioned at the printer platen when the read back and eject operation was issued, did not have a readable line finder mark when that line passed sense cell 4. Sense cell 4 is located 9 line spaces above the printer platen, therefore the check for the line finder mark must be delayed until the ledger card has moved 9 line spaces from the printer platen.

Chapter 6. Ledger Card Device Attachment Operations

This chapter explains how the LCD operations are performed. LCD instructions load I/O, test I/O, sense I/O, and start I/O are the same as for the printer and are explained in Chapter 3.

Operations are arranged in the following order.

- Feed, read ID, and locate next print line; and feed, read ID, and eject.
- Index
- Read back and eject
- Eject
- Read all line finder marks (diagnostic)

All of the operations except read all line finder marks, are explained in three parts. First the objectives of the operation are given, followed by an operational data flow diagram and one or more timing charts.

Operational data flow diagrams are of the two level type. The boxes connected by a heavy line explain the major functions of the operation. The boxes to the right of the heavy lines and connected by a lighter line, explain the details.

The timing charts show the overall relationship of the signals needed to perform an operation. They are referenced to the functional units in Chapter 5 by listing the page where the logic that generates the signal can be found. A note is included on each timing chart that states the assumptions made about the marks on the card and other pertinent information.

FEED, READ ID, AND LOCATE NEXT PRINT LINE; FEED, READ ID, AND EJECT

These operations are similar. Both operations feed the ledger card into the ledger card device and read the ID number from the card into main storage. The difference in operation occurs after the ID number is read from the ledger card.

Feed, Read ID, and Locate Next Print Line

Feed, read ID, and locate next print line checks for line finder marks while feeding the card into the LCD. When two consecutive line finder marks are found missing, the LCD attachment signals the LCD to stop feeding the ledger card when the next available print line is positioned at the platen. If a line finder mark is sensed late (in a position to cause overprinting of a line), the LCD attachment signals the LCD to feed one additional print line beyond the normal stopping point, before stopping the card.

Information can now be printed on the card by the printer, each line must be followed by a line finder mark. An LCD index instruction can be issued to move the ledger card to the next sequential print line. However, the program must check for a last printable line condition (a TIO instruction) before printing to insure that the card has not moved beyond the last available print position on the ledger card.

To remove the card from the LCD, the program can issue either a read mark and eject or an eject instruction to the LCD. For information about these operations, see pages 9-619 and 9-623.

Feed, Read ID, and Eject

Feed, read ID, and eject does not check for line finder marks. After the LCD has read the ID number from the ledger card, the card continues to feed through the LCD and into the stacker.

Before either of these operations begins, the system program must issue LIO instructions to load the local storage registers with the following addresses.

- PCAR with the storage address of the first byte of a command field.
- PDAR with the storage address where the first byte of the ID number is to be read into.
- LLAR with the storage address of a two byte field that contains 110E (hexadecimal). This LSR is used only for the feed, read ID, and locate instruction.

One of the following command fields must be created at the PCAR address.

For feed, read ID and locate next print line.

03	05	04	00	05	04	06	13

For feed, read ID, and eject.

03	05	04	00	05	04	07	13

Next, a test I/O instruction is performed to check for card not aligned. This causes the LCD to:

1. Block I/O condition B.
2. Light the LCD I/O attention lamp on the keyboard console.
3. Raise the card gate in the LCD so that a card can be inserted.

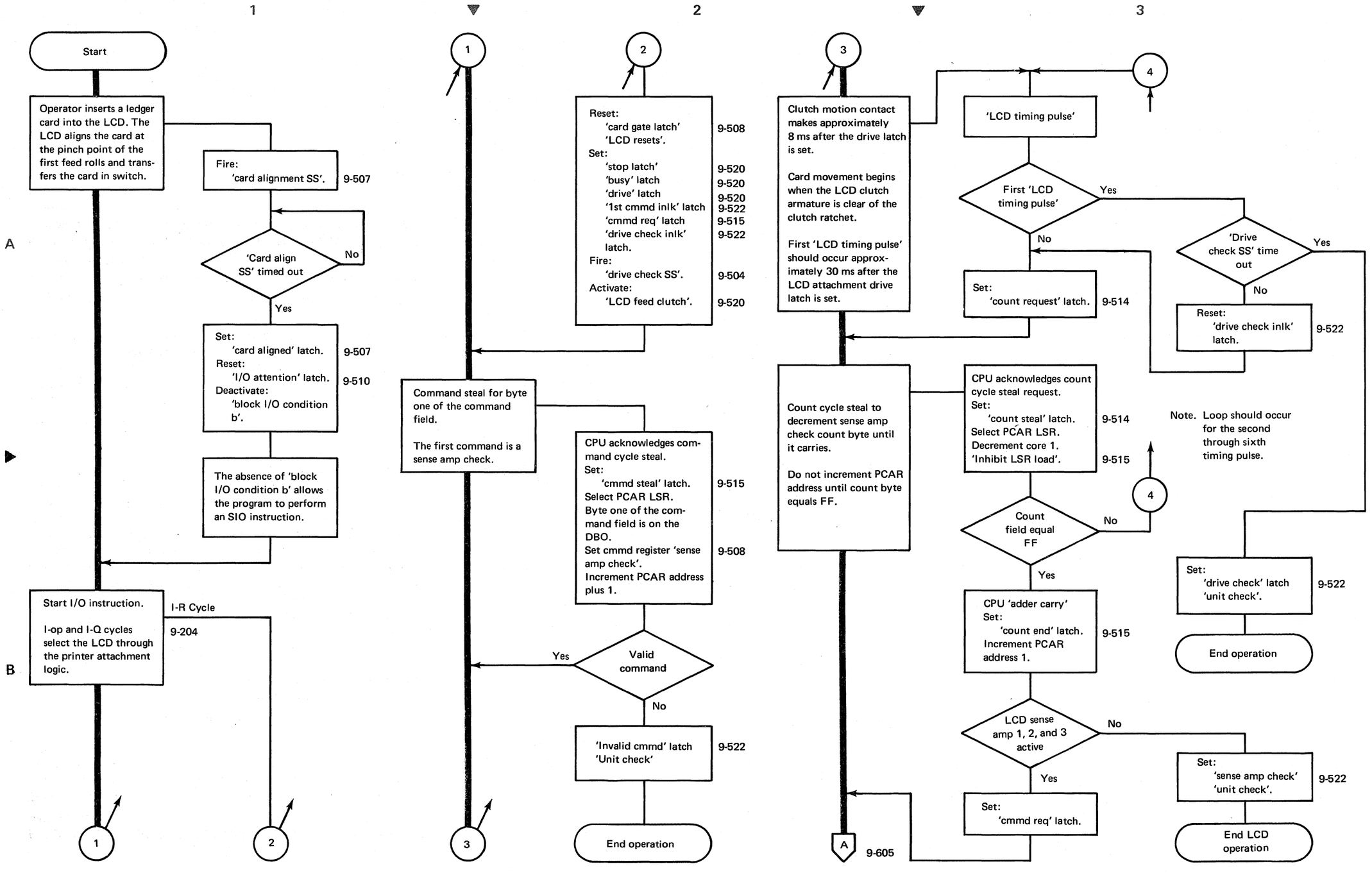
Note, the TIO instruction should also check for, not unit check, not LCD busy, and not LSR busy.

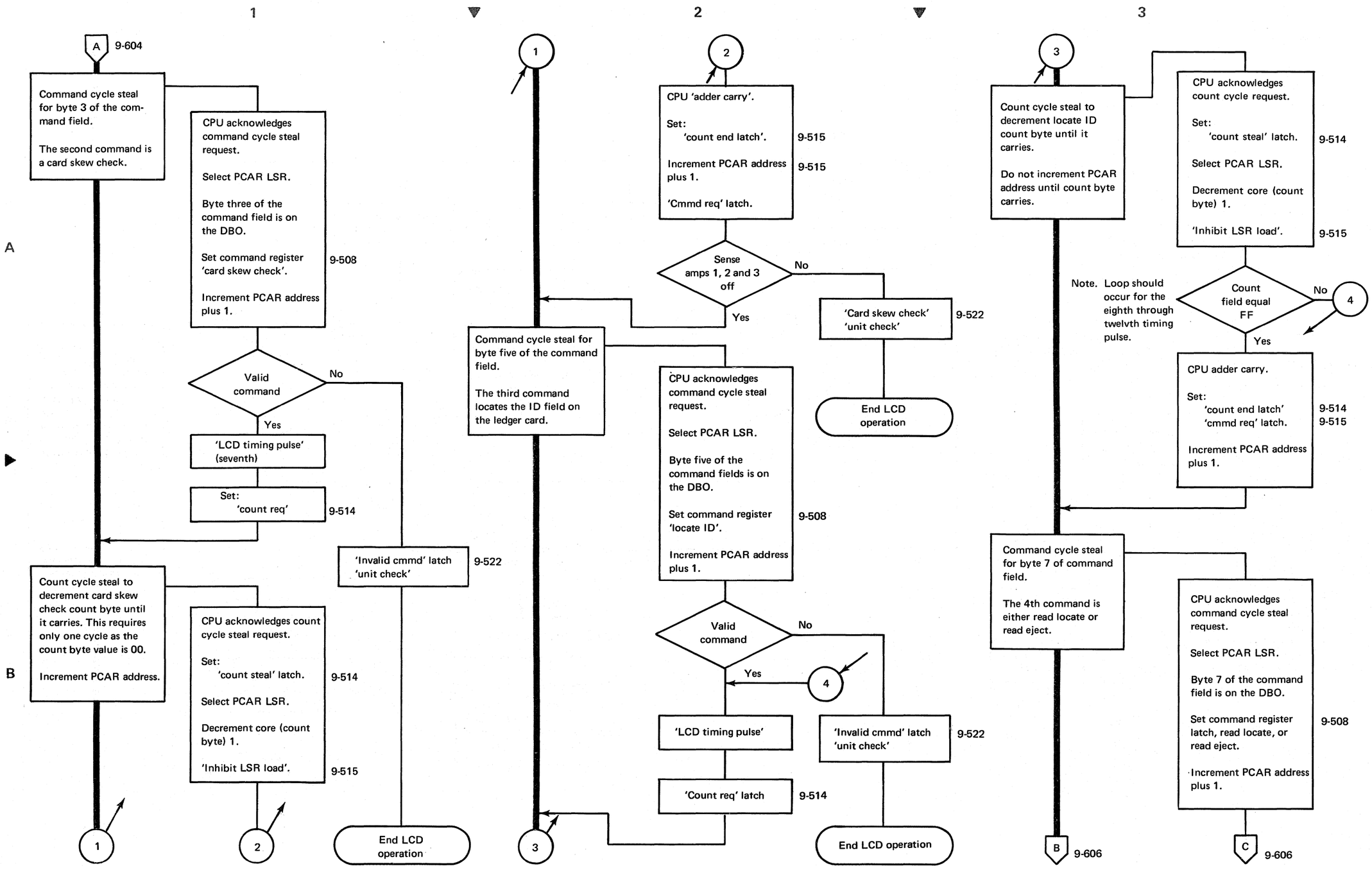
The LCD I/O attention light on is a signal to the operator to insert a ledger card into the LCD.

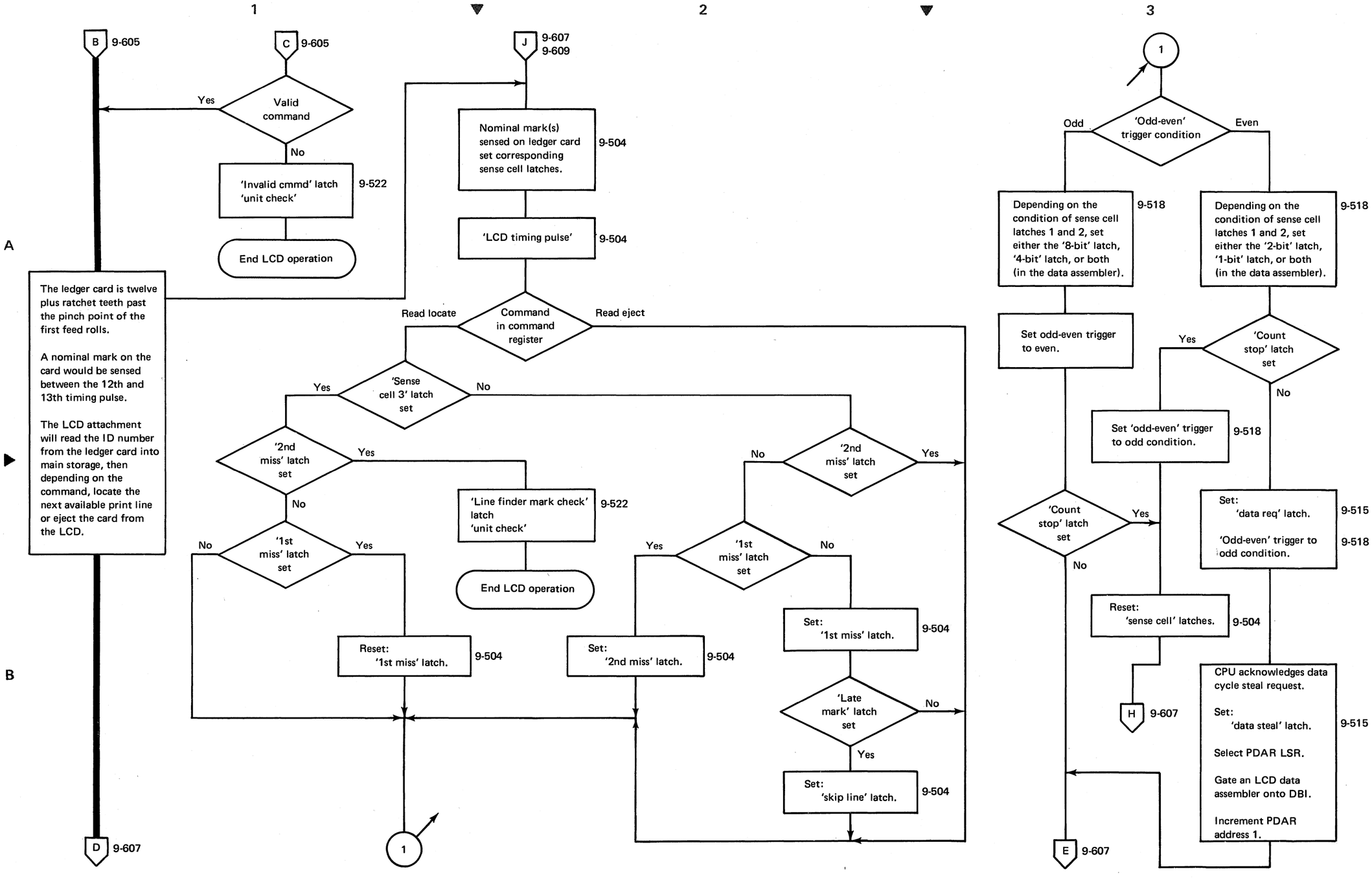
The program does not have to wait until the operations are completely finished to examine the ID number. Even though the LCD is busy, a TIO instruction check for not read ID busy will indicate when the ID number has been transferred into main storage.

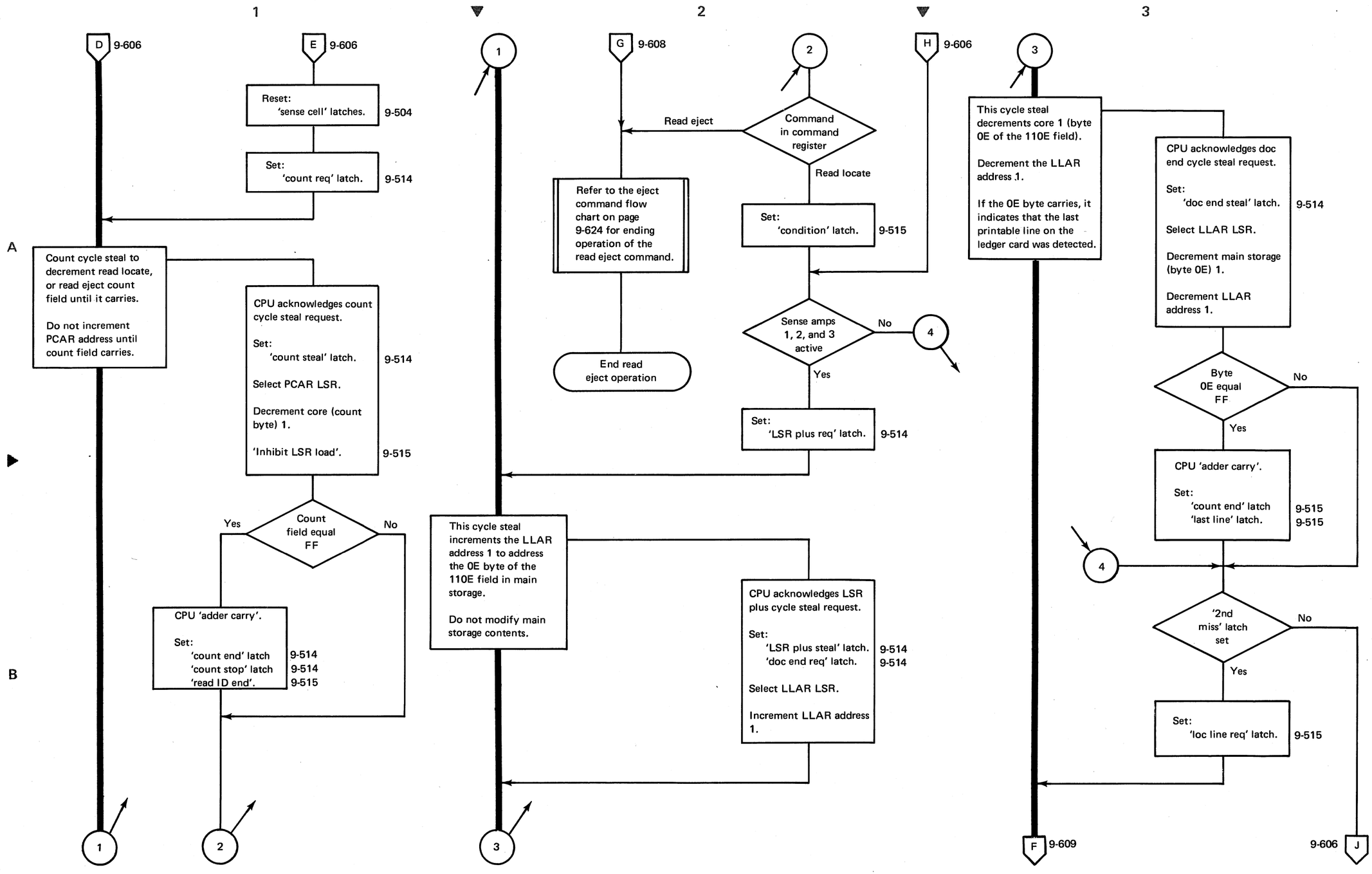
After these operations are finished, the program should check for not unit check before starting another operation. If the instruction was a feed, read ID, and locate; not last printable line condition should also be checked for.

If a feed, read ID, and locate next print line instruction is issued to the LCD and the ledger card does not have an ID number, (blank card) the ID data field at the PDAR address will be filled with 40 (hexadecimal) and the ledger card will stop with the first printable line positioned at the printer platen.

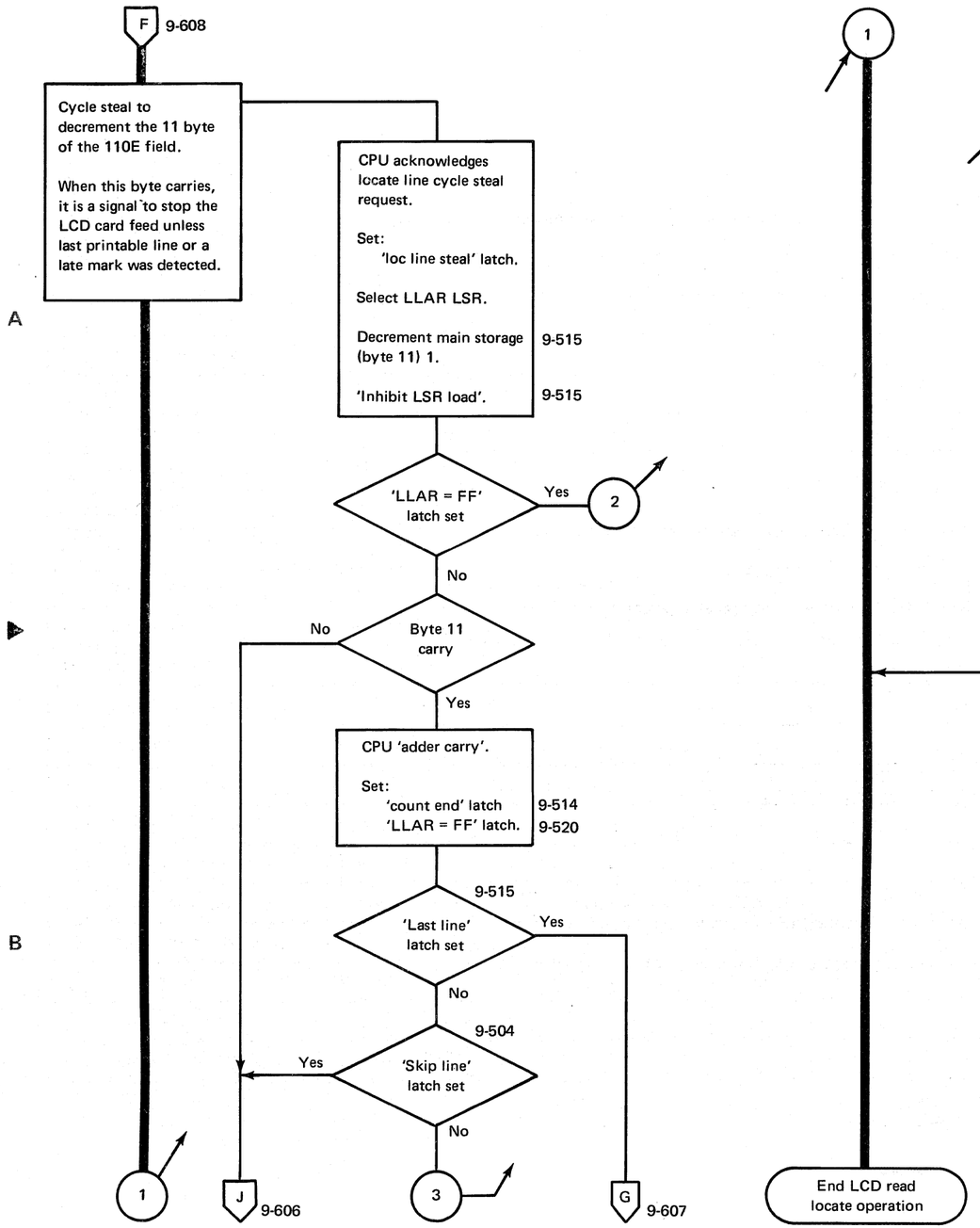

1
2
3
Start
Operator inserts a ledger card into the LCD. The LCD aligns the card at the pinch point of the first feed rolls and transfers the card in switch.
Fire:
'card alignment SS'. 9-507
'Card align SS' timed out
No
Yes
Set:
'card aligned' latch. 9-507
Reset:
'I/O attention' latch. 9-510
Deactivate:
'block I/O condition b'.
The absence of 'block I/O condition b' allows the program to perform an SIO instruction.
A
Start I/O instruction.
I-op and I-Q cycles select the LCD through the printer attachment logic.
I-R Cycle
9-204
B
1
2
Reset:
'card gate latch' 9-508
'LCD resets'.
Set:
'stop latch' 9-520
'busy' latch 9-520
'drive' latch 9-520
'1st cmmd inlk' latch 9-522
'cmmd req' latch 9-515
'drive check inlk' latch. 9-522
Fire:
'drive check SS'. 9-504
Activate:
'LCD feed clutch'. 9-520
Command steal for byte one of the command field.
The first command is a sense amp check.
CPU acknowledges command cycle steal.
Set:
'cmmd steal' latch. 9-515
Select PCAR LSR.
Byte one of the command field is on the DBO.
Set cmmd register 'sense amp check'. 9-508
Increment PCAR address plus 1.
Yes
Valid command
No
'Invalid cmmd' latch 9-522
'Unit check'
End operation
3
3
Clutch motion contact makes approximately 8 ms after the drive latch is set.
Card movement begins when the LCD clutch armature is clear of the clutch ratchet.
First 'LCD timing pulse' should occur approximately 30 ms after the LCD attachment drive latch is set.
4
'LCD timing pulse'
First 'LCD timing pulse'
Yes
No
'Drive check SS' time out
Yes
No
Set:
'count request' latch. 9-514
Reset:
'drive check inlk' latch. 9-522
Count cycle steal to decrement sense amp check count byte until it carries.
Do not increment PCAR address until count byte equals FF.
CPU acknowledges count cycle steal request.
Set:
'count steal' latch. 9-514
Select PCAR LSR.
Decrement core 1.
'Inhibit LSR load'. 9-515
Note. Loop should occur for the second through sixth timing pulse.
4
Count field equal FF
No
Yes
CPU 'adder carry'
Set:
'count end' latch. 9-515
Increment PCAR address 1.
Set:
'drive check' latch 9-522
'unit check'.
End operation
LCD sense amp 1, 2, and 3 active
No
Yes
Set:
'sense amp check' 9-522
'unit check'.
Set:
'cmmd req' latch.
End LCD operation
A 9-605

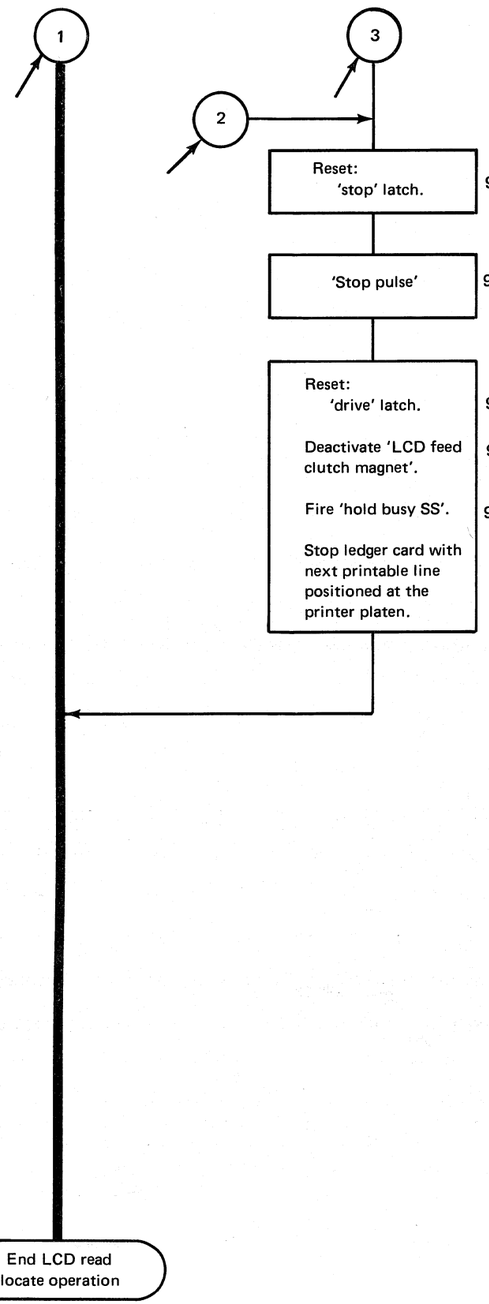

1
2
3
A
9-604
Command cycle steal for byte 3 of the command field.
The second command is a card skew check.
CPU acknowledges command cycle steal request.
Select PCAR LSR.
Byte three of the command field is on the DBO.
Set command register 'card skew check'.
9-508
Increment PCAR address plus 1.
Valid command
No
Yes
'LCD timing pulse' (seventh)
Set: 'count req'
9-514
'Invalid cmmd' latch 'unit check'
9-522
End LCD operation
Count cycle steal to decrement card skew check count byte until it carries. This requires only one cycle as the count byte value is 00.
Increment PCAR address.
CPU acknowledges count cycle steal request.
Set: 'count steal' latch.
9-514
Select PCAR LSR.
Decrement core (count byte) 1.
'Inhibit LSR load'.
9-515
B
1
2
1
2
CPU 'adder carry'.
Set: 'count end latch'.
9-515
Increment PCAR address plus 1.
9-515
'Cmmd req' latch.
Sense amps 1, 2 and 3 off
No
Yes
'Card skew check' 'unit check'
9-522
End LCD operation
Command cycle steal for byte five of the command field.
The third command locates the ID field on the ledger card.
CPU acknowledges command cycle steal request.
Select PCAR LSR.
Byte five of the command fields is on the DBO.
Set command register 'locate ID'.
9-508
Increment PCAR address plus 1.
Valid command
No
Yes
4
'LCD timing pulse'
'Invalid cmmd' latch 'unit check'
9-522
'Count req' latch
9-514
End LCD operation
3
3
Count cycle steal to decrement locate ID count byte until it carries.
Do not increment PCAR address until count byte carries.
CPU acknowledges count cycle request.
Set: 'count steal' latch.
9-514
Select PCAR LSR.
Decrement core (count byte) 1.
'Inhibit LSR load'.
9-515
Note. Loop should occur for the eighth through twelvth timing pulse.
Count field equal FF
No
4
Yes
CPU adder carry.
Set: 'count end latch'
'cmmd req' latch.
9-514
9-515
Increment PCAR address plus 1.
Command cycle steal for byte 7 of command field.
The 4th command is either read locate or read eject.
CPU acknowledges command cycle steal request.
Select PCAR LSR.
Byte 7 of the command field is on the DBO.
Set command register latch, read locate, or read eject.
9-508
Increment PCAR address plus 1.
B
9-606
C
9-606


1
2
3
B 9-605
C 9-605
J 9-607 9-609
Yes
Valid command
No
'Invalid cmmd' latch 'unit check'
9-522
End LCD operation
Nominal mark(s) sensed on ledger card set corresponding sense cell latches.
9-504
'LCD timing pulse'
9-504
A
The ledger card is twelve plus ratchet teeth past the pinch point of the first feed rolls.
A nominal mark on the card would be sensed between the 12th and 13th timing pulse.
The LCD attachment will read the ID number from the ledger card into main storage, then depending on the command, locate the next available print line or eject the card from the LCD.
Read locate
Command in command register
Read eject
Yes
'Sense cell 3' latch set
No
'2nd miss' latch set
Yes
No
'Line finder mark check' latch 'unit check'
9-522
End LCD operation
No
'1st miss' latch set
Yes
Reset: '1st miss' latch.
9-504
No
'2nd miss' latch set
Yes
Yes
'1st miss' latch set
No
Set: '2nd miss' latch.
9-504
Set: '1st miss' latch.
9-504
'Late mark' latch set
No
Yes
Set: 'skip line' latch.
9-504
B
D 9-607
1
1
Odd
'Odd-even' trigger condition
Even
Depending on the condition of sense cell latches 1 and 2, set either the '8-bit' latch, '4-bit' latch, or both (in the data assembler).
9-518
Depending on the condition of sense cell latches 1 and 2, set either the '2-bit' latch, '1-bit' latch, or both (in the data assembler).
9-518
Set odd-even trigger to even.
Yes
'Count stop' latch set
No
Set 'odd-even' trigger to odd condition.
9-518
'Count stop' latch set
Yes
No
Set:
'data req' latch.
9-515
'Odd-even' trigger to odd condition.
9-518
Reset: 'sense cell' latches.
9-504
H 9-607
CPU acknowledges data cycle steal request.
Set:
'data steal' latch.
9-515
Select PDAR LSR.
Gate an LCD data assembler onto DBI.
Increment PDAR address 1.
E 9-607

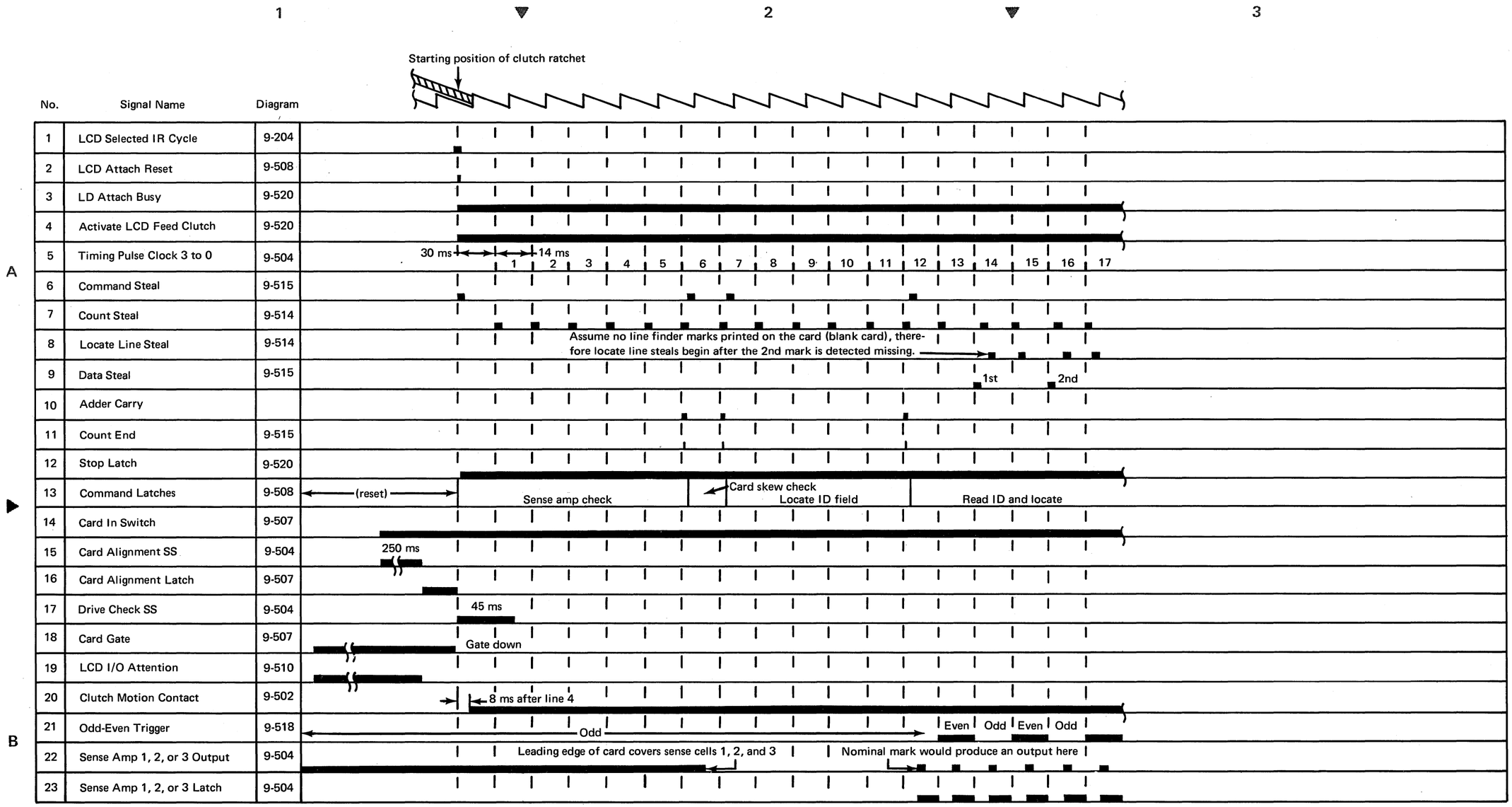

1
2
3
D 9-606
E 9-606
Reset:
'sense cell' latches. 9-504
Set:
'count req' latch. 9-514
A
Count cycle steal to decrement read locate, or read eject count field until it carries.
Do not increment PCAR address until count field carries.
CPU acknowledges count cycle steal request.
Set:
'count steal' latch. 9-514
Select PCAR LSR.
Decrement core (count byte) 1.
'Inhibit LSR load'. 9-515
Yes
Count field equal FF
No
CPU 'adder carry'.
Set:
'count end' latch 9-514
'count stop' latch 9-514
'read ID end'. 9-515
B
1
2
1
G 9-608
Read eject
Refer to the eject command flow chart on page 9-624 for ending operation of the read eject command.
End read eject operation
2
Command in command register
Read locate
Set:
'condition' latch. 9-515
Sense amps 1, 2, and 3 active
No
4
Yes
Set:
'LSR plus req' latch. 9-514
This cycle steal increments the LLAR address 1 to address the 0E byte of the 110E field in main storage.
Do not modify main storage contents.
CPU acknowledges LSR plus cycle steal request.
Set:
'LSR plus steal' latch. 9-514
'doc end req' latch. 9-514
Select LLAR LSR.
Increment LLAR address 1.
3
H 9-606
3
This cycle steal decrements core 1 (byte 0E of the 110E field).
Decrement the LLAR address 1.
If the 0E byte carries, it indicates that the last printable line on the ledger card was detected.
CPU acknowledges doc end cycle steal request.
Set:
'doc end steal' latch. 9-514
Select LLAR LSR.
Decrement main storage (byte 0E) 1.
Decrement LLAR address 1.
Byte 0E equal FF
No
Yes
CPU 'adder carry'.
Set:
'count end' latch 9-515
'last line' latch. 9-515
4
'2nd miss' latch set
No
Yes
Set:
'loc line req' latch. 9-515
F 9-609
9-606 J

1 2 3

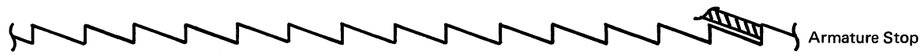




LCD ATTACHMENT–Operations
Feed, Read ID, and Locate-Eject (Part 6 of 10)



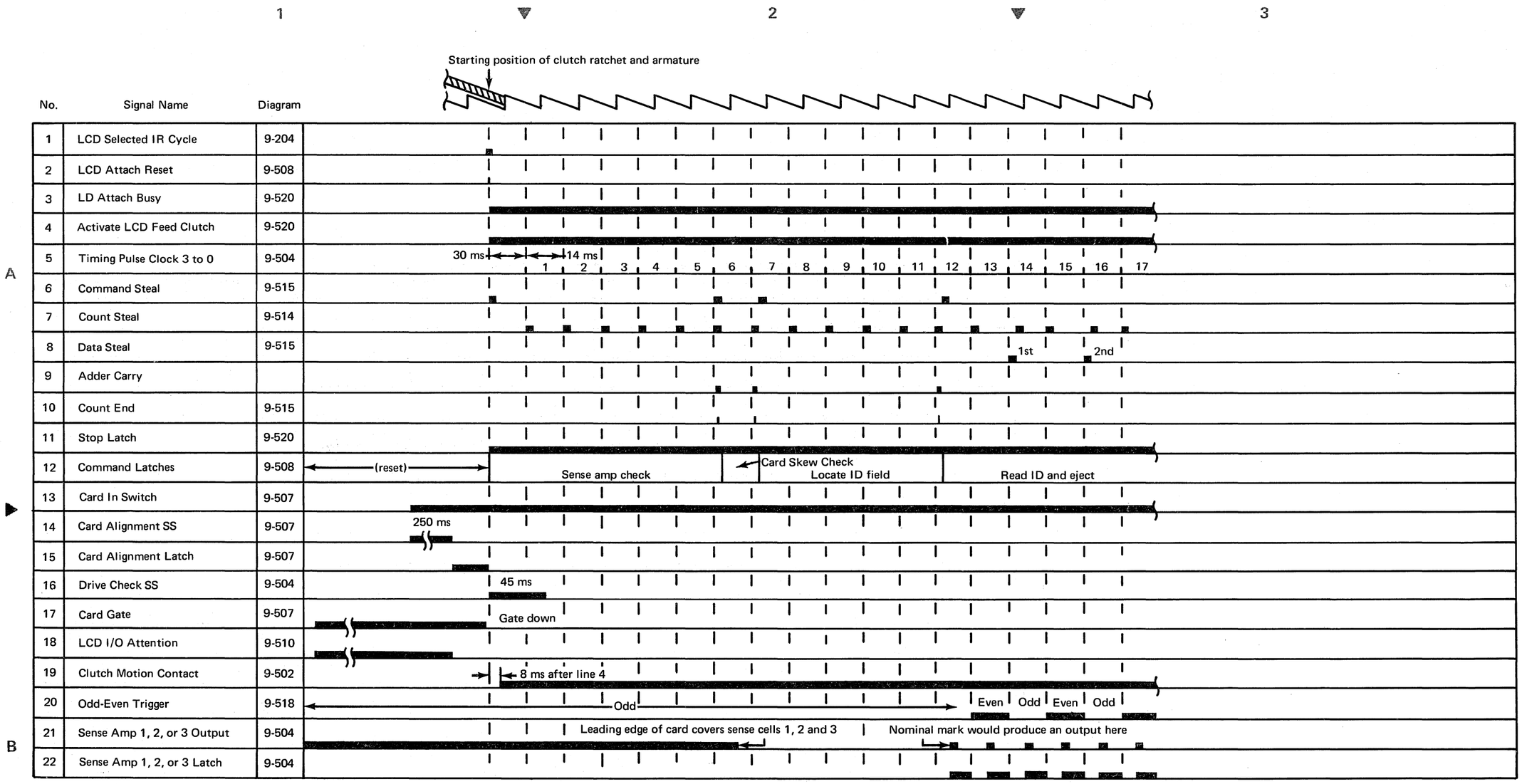
Feed, Read ID and Locate Operation



No.	Signal Name	Diagram
1	Timing Pulse Clock 3 to 0	9-504
2	LCD Attach Busy	9-520
3	Activate LCD Feed Clutch	9-520
4	Count Steal	9-514
5	Data Steal	9-515
6	Locate Line Steal	9-514
7	Command Count Stop	9-515
8	Read ID End	9-515
9	Adder Carry	—
10	Count End	9-515
11	Stop Latch	9-520
12	Stop Pulse	9-504
13	Command Latches	9-508
14	Card In Switch	9-507
15	Clutch Motion Contact	9-502
16	Odd-Even Trigger	9-518
17	Sense Amp 1, 2, or 3 Output	9-504
18	Sense Amp 1, 2, or 3 Latches	9-504
19	Document End Condition Latch	9-514
20	Hold Busy SS	9-504

Feed, Read ID and Locate Operation

Stop ledger card with first print line positioned at the printer platen. A late mark was not detected so that the card stops in a normal manner (no extra line space).

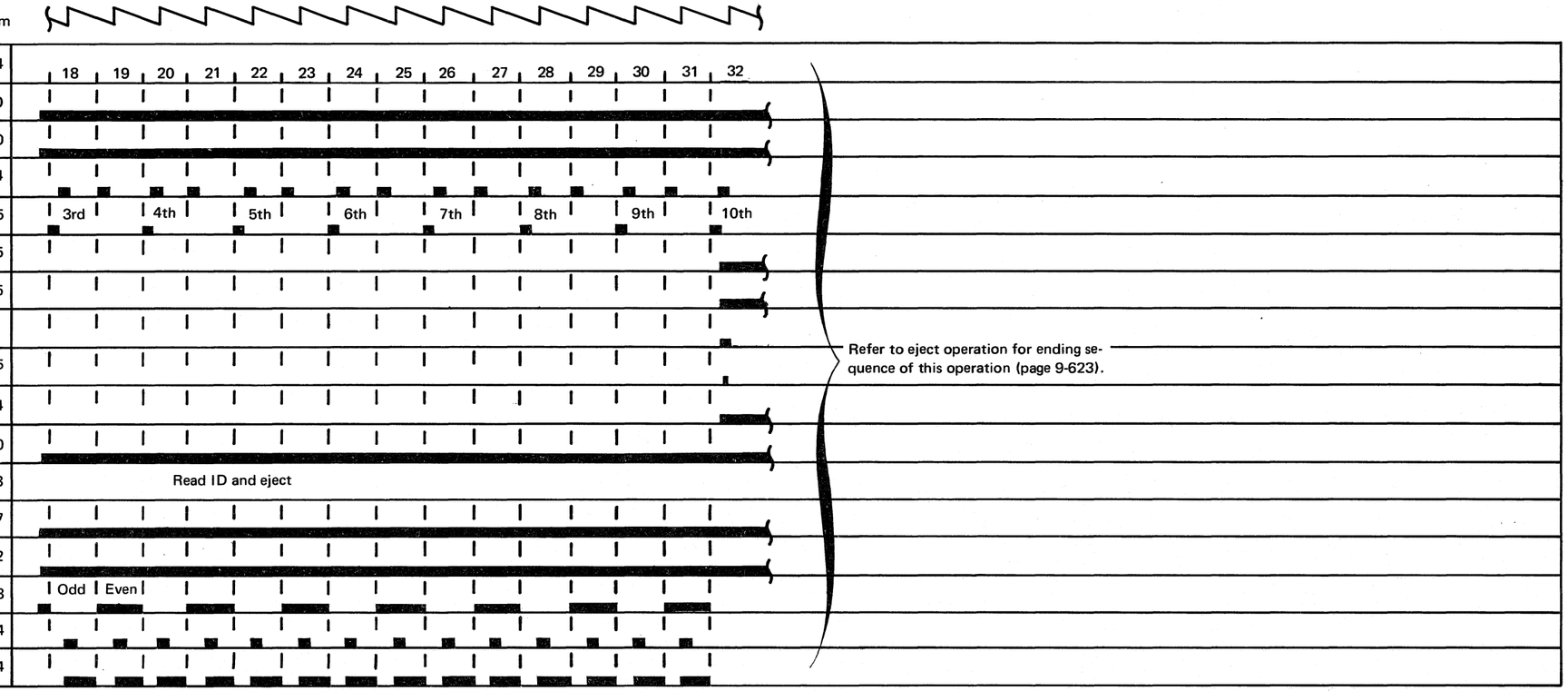


Feed, read ID and eject operation

1 ▼ 2 ▼ 3

A

No.	Signal Name	Diagram
1	Timing Pulse Clock 3 to 0	9-504
2	LCD Attach Busy	9-520
3	Activate LCD Feed Clutch	9-520
4	Count Steal	9-514
5	Data Steal	9-515
6	Command Count Stop	9-515
7	Read ID End	9-515
8	Adder Carry	
9	Count End	9-515
10	Document End Condition Latch	9-514
11	Stop Latch	9-520
12	Command Latches	9-508
13	Card In Switch	9-507
14	Clutch Motion Contact	9-502
15	Odd-Even Trigger	9-518
16	Sense Amp 1, 2, or 3 Output	9-504
17	Sense Amp 1, 2, or 3 Latches	9-504



▶

Feed, read ID, and eject operation

B

INDEX

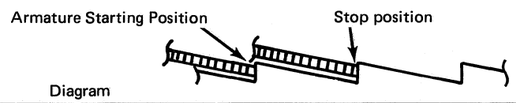
The index instruction moves the ledger card to the next sequential print line. If the bottom edge of the ledger card is above the lower sense station, LSR plus and document end cycle steal requests are made to decrement the 0E byte of the 110E field.

Before starting an index operation, the program should issue TIO instructions to check for: not unit check, not LCD busy, not LSR busy, and not last printable line.

An LIO instruction is issued to:

1. Load the LSR PCAR with the command field address. LSR PDAR is not used.
2. LLAR must contain the address of the 110E field; the 110E field must not be reinitialized.

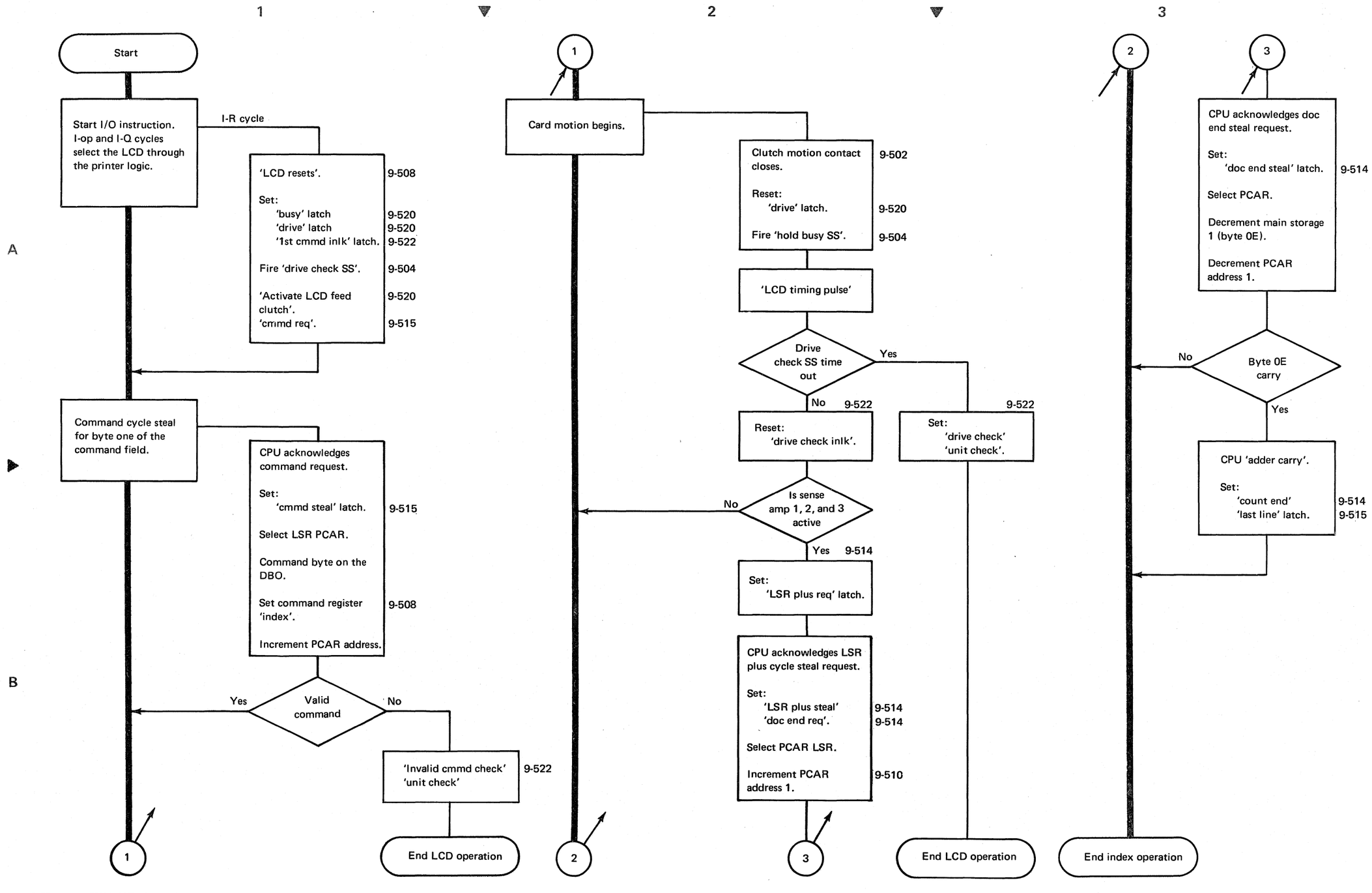
Generate the command field 01 at the PCAR address.



No.	Signal Name	Diagram	1 ▼ 2 ▼ 3
1	LCD Selected I-R Cycle	9-204	
2	LCD Attachment Reset	9-508	
3	LCD Attachment Busy	9-520	
4	Activate Feed Clutch	9-520	
5	Timing Pulse Clock 3 to 0	9-504	30 ms ← 33
A 6	Command Steal	9-515	
7	LSR Plus and Doc End Cycle Steals	9-514	These cycle steal requests are made only if the bottom edge of the ledger card is past the lower read station. They decrement the last printable line byte (Byte 0E of the 110E field).
8	Command Count Stop	9-515	
9	Read ID End	9-515	
10	Stop Latch	9-520	
11	Command Latches	9-508	Index — Reset with attachment reset or next command steal
12	Card In Switch	9-507	
13	Card Out Switch	9-507	This signal depends on the position of the ledger card in the LCD. Active 41 ratchet teeth past pinch point of first feed rolls.
▶ 14	Drive Check SS	9-504	45 ms
15	Hold Busy SS	9-504	55 ms
16	Clutch Motion Contact	9-502	→ ← 8 ms

Assume ledger card stopped at the 1st print line positioned at the platen before index operation began. This index operation moved the ledger card to print line 2.

B



LCD ATTACHMENT–Operations
Index (Part 3 of 3)

READ BACK AND EJECT

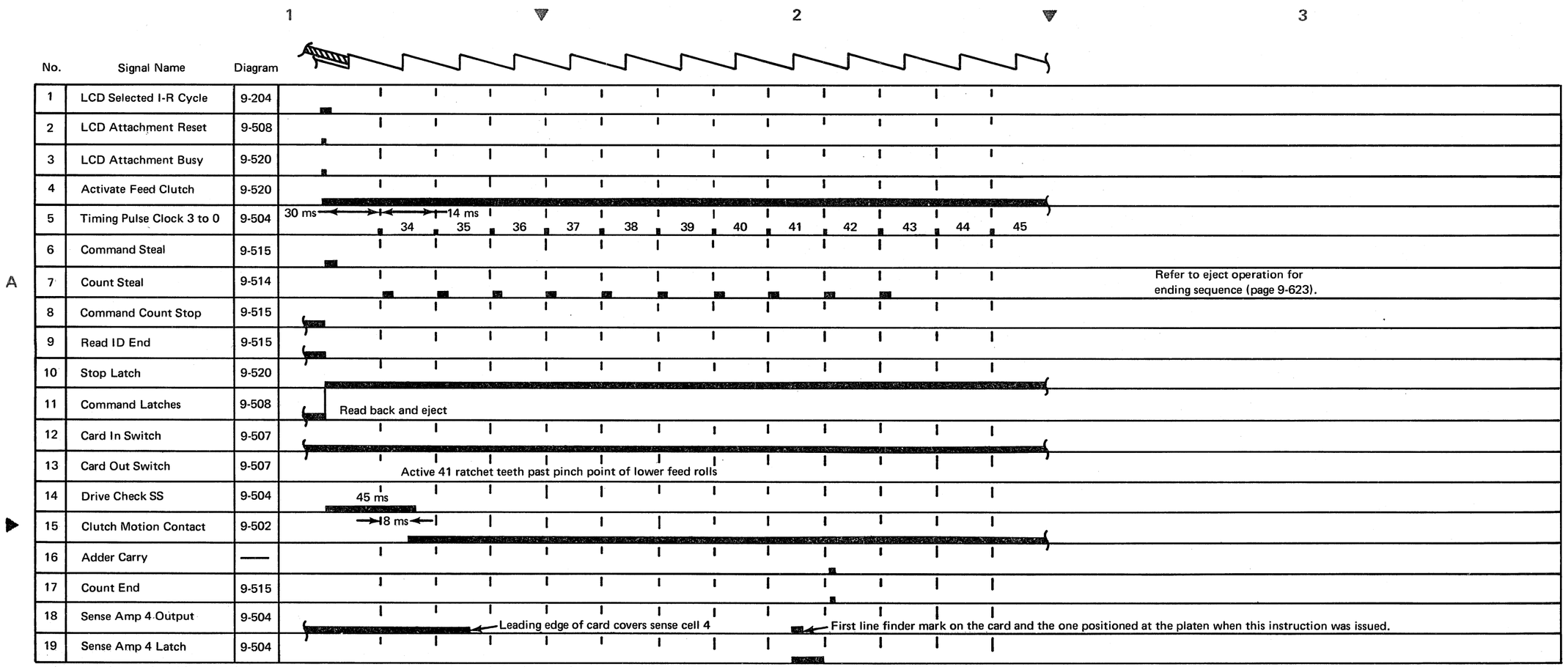
This operation is issued to eject the ledger card from the LCD and check that the last line finder mark (the one that is positioned at the printer platen when this instruction was issued) can be read by sense cell 4 as the ledger card is ejected from the LCD.

After the ledger card feed starts, the command count byte is decremented with each LCD timing pulse. When the count field decrements to FF, the attachment samples sense cell 4 to see if a line finder mark was read at the 9th line after LCD card feed started. If sense cell 4 did not sense a line finder mark, the read mark check latch is set, and the card feed is stopped. If sense cell 4 did read a mark, the card continues to eject from the LCD and into the stacker.

Before starting a read back and eject operation, the program should issue TIO instructions to check for, not unit check, not LCD busy, and not LSR busy.

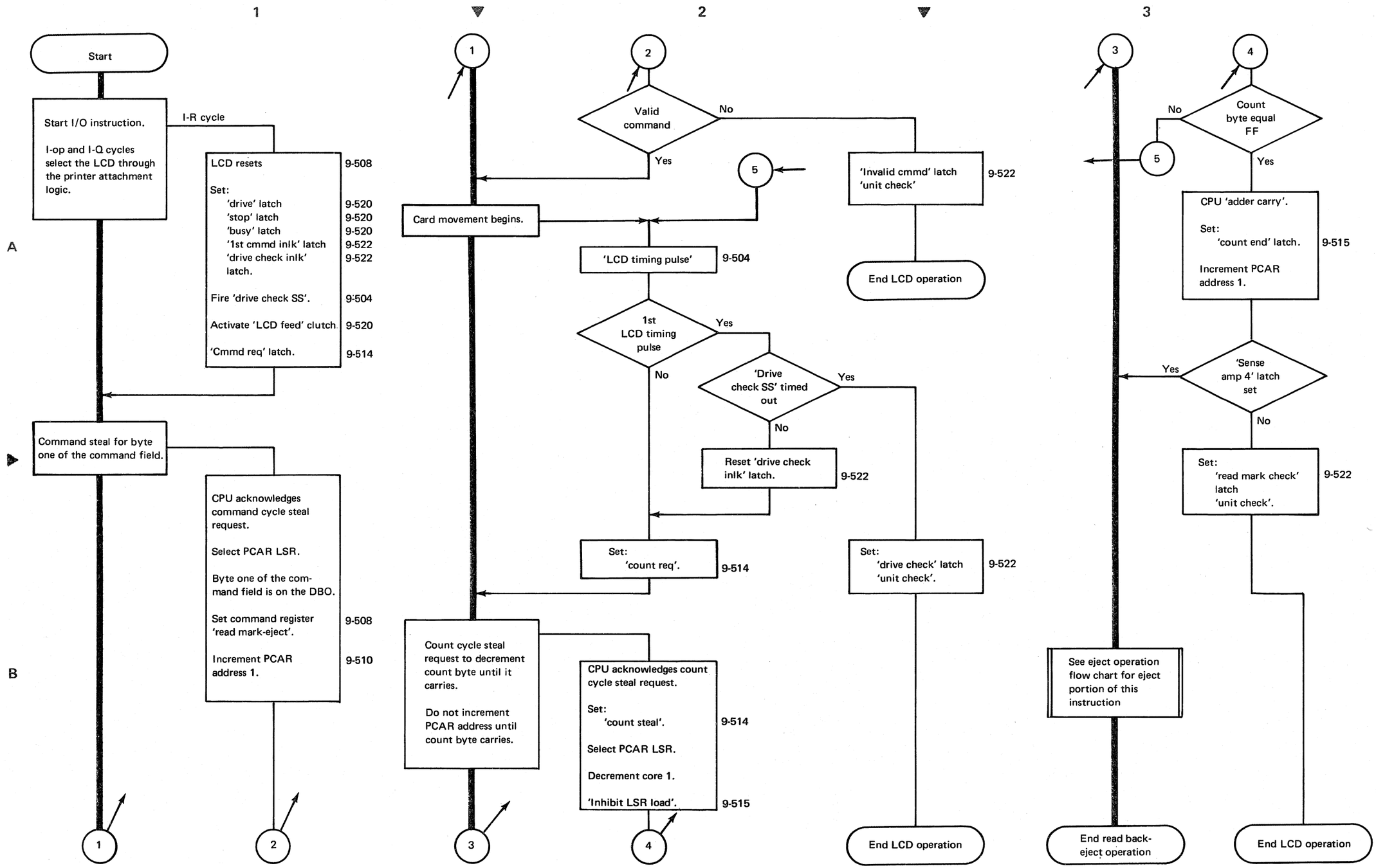
An LIO instruction is issued to load the LSR PCAR with the address of the command field. LSRs PDAR and LLAR are not used for this instruction.

Generate the command field 02 08 at the PCAR address.



No.	Signal Name	Diagram
1	LCD Selected I-R Cycle	9-204
2	LCD Attachment Reset	9-508
3	LCD Attachment Busy	9-520
4	Activate Feed Clutch	9-520
5	Timing Pulse Clock 3 to 0	9-504
6	Command Steal	9-515
7	Count Steal	9-514
8	Command Count Stop	9-515
9	Read ID End	9-515
10	Stop Latch	9-520
11	Command Latches	9-508
12	Card In Switch	9-507
13	Card Out Switch	9-507
14	Drive Check SS	9-504
15	Clutch Motion Contact	9-502
16	Adder Carry	——
17	Count End	9-515
18	Sense Amp 4 Output	9-504
19	Sense Amp 4 Latch	9-504

Assume ledger card positioned with print line 1 positioned at the printer platen when this operation was started. A line finder mark printed at line 1 is read at sense cell 4, 9 line spaces later.



LCD ATTACHMENT—Operations
Read Mark and Eject (Part 3 of 3)

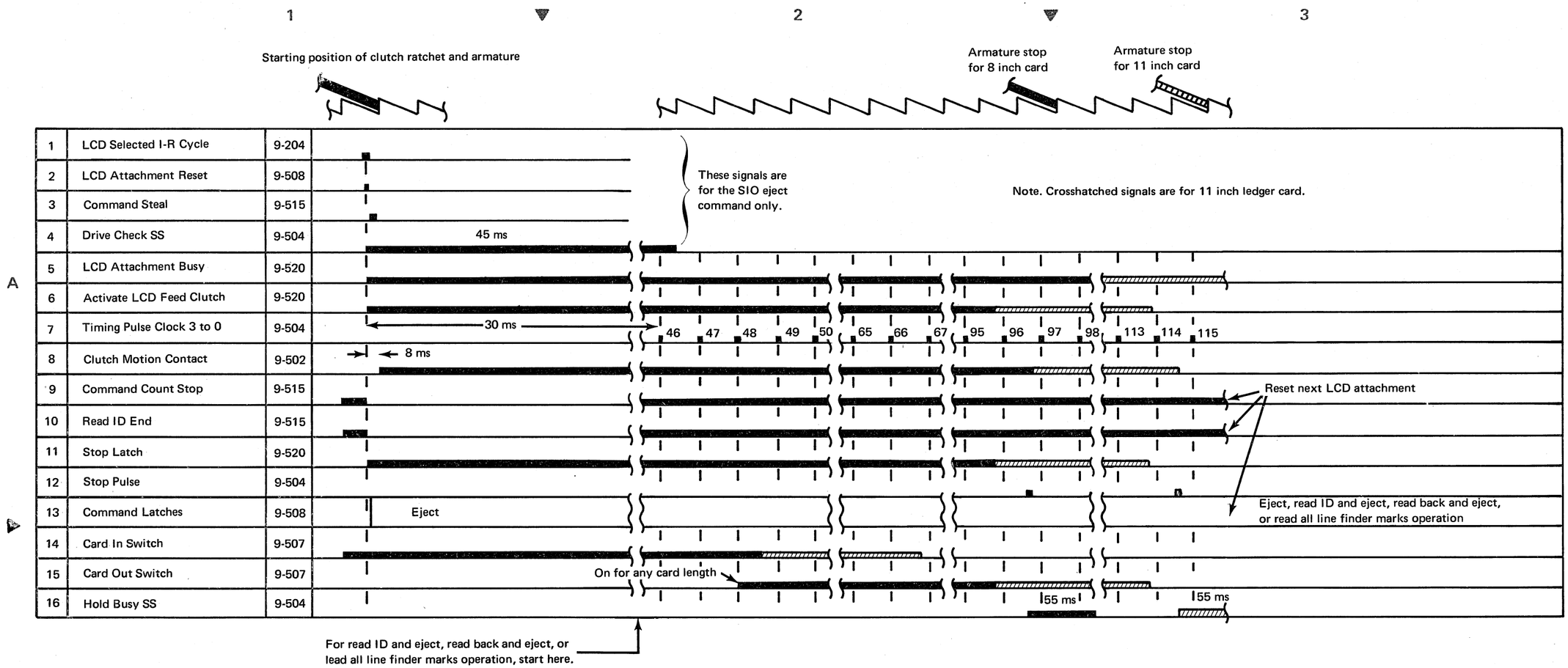
EJECT

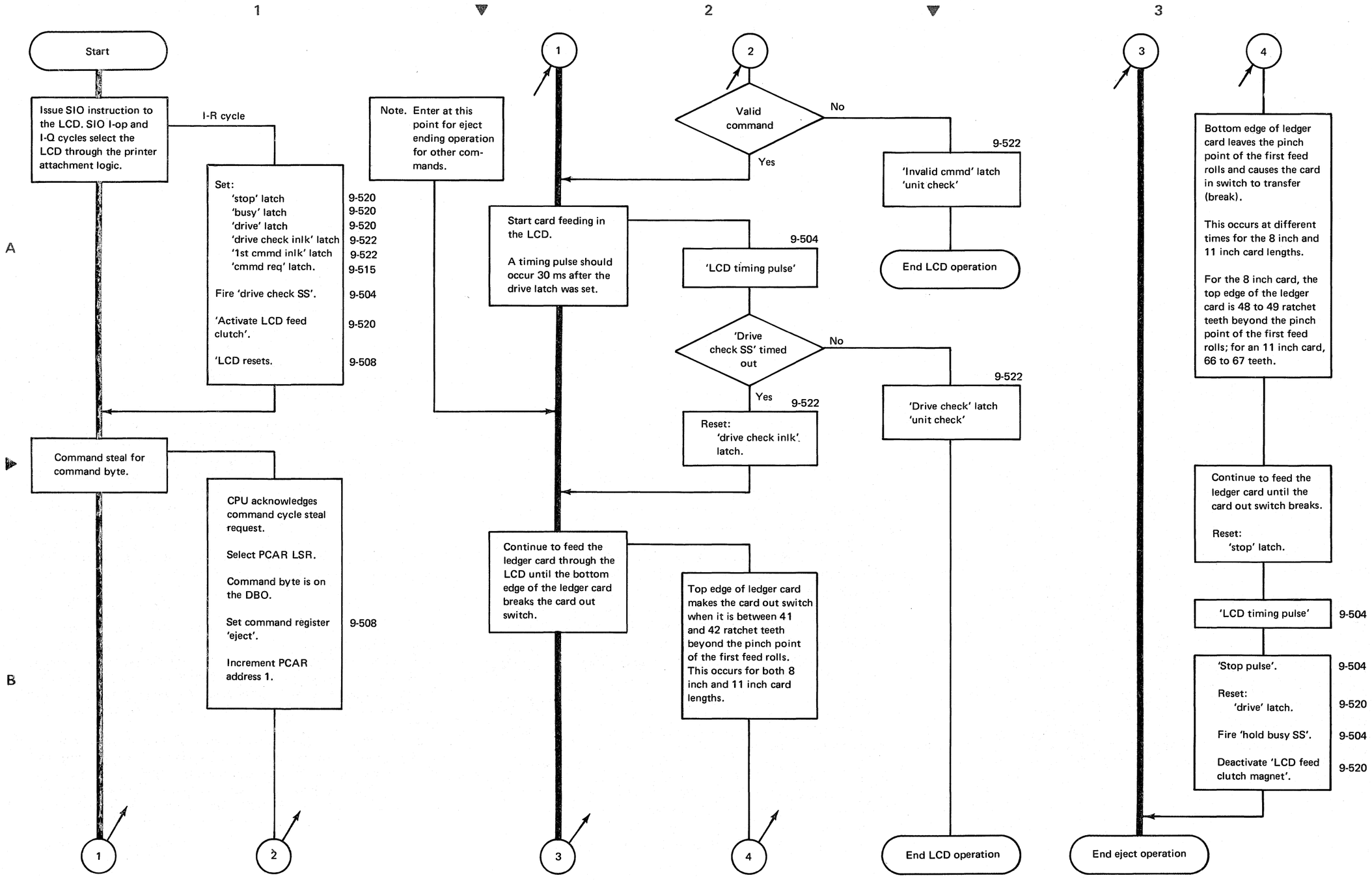
This operation is issued to eject the ledger card out of the LCD and into the stacker. This operation should only be used after an I/O check is detected.

Before starting an eject operation, the program should issue TIO instructions to check for not LCD busy and not LSR busy.

An LIO instruction is issued to load the PCAR with a command field address. LSRs LLAR and PDAR are not used during this operation.

Generate the command field 00 at the PCAR address.


1
2
3
Starting position of clutch ratchet and armature
Armature stop for 8 inch card
Armature stop for 11 inch card
1 LCD Selected I-R Cycle 9-204
2 LCD Attachment Reset 9-508
3 Command Steal 9-515
4 Drive Check SS 9-504
5 LCD Attachment Busy 9-520
6 Activate LCD Feed Clutch 9-520
7 Timing Pulse Clock 3 to 0 9-504
8 Clutch Motion Contact 9-502
9 Command Count Stop 9-515
10 Read ID End 9-515
11 Stop Latch 9-520
12 Stop Pulse 9-504
13 Command Latches 9-508
14 Card In Switch 9-507
15 Card Out Switch 9-507
16 Hold Busy SS 9-504
These signals are for the SIO eject command only.
Note. Crosshatched signals are for 11 inch ledger card.
45 ms
30 ms
46 47 48 49 50 65 66 67 95 96 97 98 113 114 115
8 ms
Reset next LCD attachment
Eject
Eject, read ID and eject, read back and eject, or read all line finder marks operation
On for any card length
55 ms
55 ms
For read ID and eject, read back and eject, or lead all line finder marks operation, start here.



LCD ATTACHMENT—Operations
Eject (Part 3 of 3)

READ ALL LINE FINDER MARKS

This is a diagnostic operation to read each line finder mark on the ledger card at two different sense stations. Each sense cell indicates if a line finder mark was read and at what line from the ledger card by setting bits in main storage. Each sense cell has specific bit assignments in order that the data read from the first sense station may later be compared to the data read by the second sense station. The system program performs the compare operation.

Line finder marks are first read by sense cell 3, located in the lower read station of the LCD. Twenty-nine line spaces later, the same mark is read at sense cell 4, located in the upper read station. Sense cell 4 does not respond to line finder marks that produce a weak output. Therefore, after the data is in main storage and the program has compared the data (bits) read by both stations, weak output producing line finder marks can be detected.

Data Field

The illustration on this page shows how line finder marks, read from the ledger card during a read all line finder marks instruction, are indicated in main storage.

Bit positions zero through 3 will be either an F (hexadecimal) or a 4 (hexadecimal). Bit positions 4 through 7, when set to a one bit, indicate the presence of line finder marks on the ledger card.

The numbers shown in bit positions 4 through 7 correspond to line numbers on the ledger card. Line 1 is at the top of the card, line 56 is at the bottom. Numbers within parentheses represent lines read at sense cell 3, numbers not in parentheses are lines read at sense cell 4.

Each byte can represent from one to 4 lines read from the ledger card depending on the position of the ledger card within the LCD at the time the byte was read. Example, PDAR address 0200 represents lines 1 and 2 read from the ledger card by sense cell 3. PDAR address 020E shows lines 29 and 30 read by sense cell 3 and line 1 read by sense cell 4. PDAR address 020F shows lines 31 and 32 read by sense cell 3 and lines 2 and 3 read by sense cell 4. PDAR address 022A shows line 56 read by sense cell 4.

Bit positions zero through 3 will be an F (hexadecimal) for each byte that has at least one line finder mark in the lines indicated in bits 4 through 7, if no line finder marks are read, bits zero through 3 will be a 4 (hexadecimal). For those lines that represent lines read by sense cells 3 and 4, any line finder mark sensed by either sense cell, will cause bits 0 through 3 to be an F (hexadecimal).

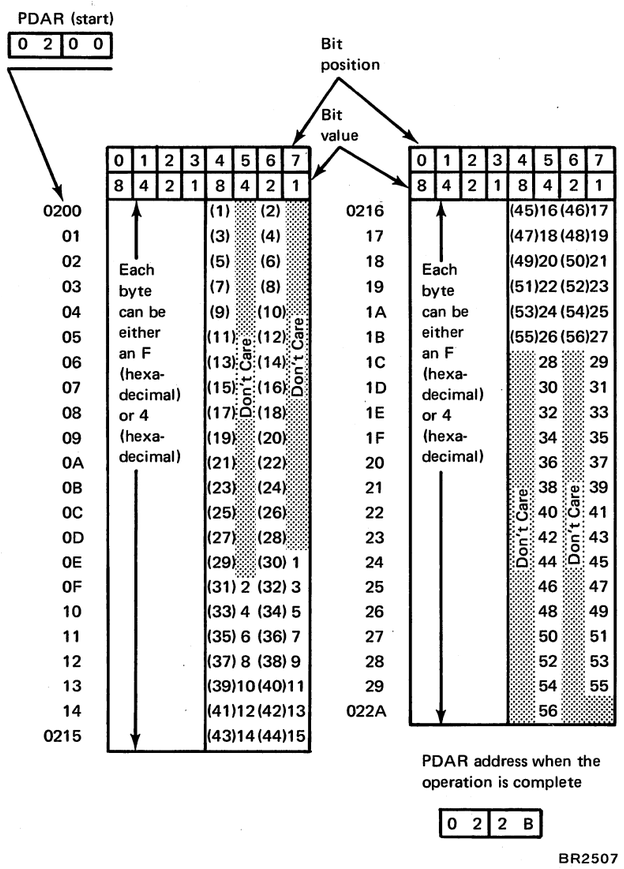
The maximum length card is always read (56 lines). This requires 43 bytes of storage to contain the data from both sense cells. (Two lines per byte = 28 bytes, plus 29 lines separation between sense stations = 15 bytes for a total of 43 bytes.)

Read All Line Finder Marks Operation

This instruction is similar in operation to a feed, read ID, and eject command and therefore data flow diagrams and timing charts are not shown. Only the exceptions will be explained.

The SIO control code for this instruction must be XXXXXXX1 to set the scan latch, shown on page 9-515. The scan latch degates sense cell 1 and 2 into the data assembler and gates sense cell 3 and 4 instead.

The read ID, and eject command count byte equals 55 (hexadecimal). This is to prevent setting the count end latch after reading the 20 line ID number as in the feed, read ID, and eject operation. By not setting the count end latch, the condition latch is not set to allow LSR plus and document end cycle steal requests.



Section 10. Data Recorder Attachment

This section of the 5406 FETMM contains the theory and maintenance diagrams for the 5496 Data Recorder attachment. It consists of three chapters as follows:

Chapter 1. Introduction
Chapter 2. Functional Units
Chapter 3. Operations

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Chapter 1. Introduction

DATA RECORDER ATTACHMENT

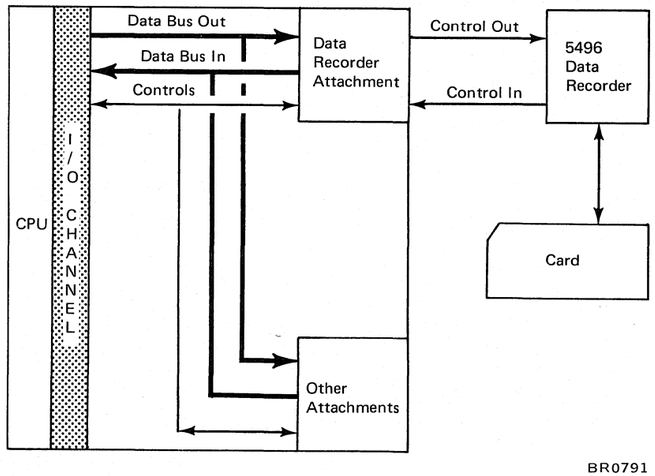
The IBM 5496 Data Recorder attachment provides a means for the Model 6 to use the 5496 Data Recorder as an input-output device for reading and punching the System/3 card. The attachment provides the interface between the delay line memory in the data recorder and main storage in the 5406 Processing Unit. Information transferred between these two storage devices is controlled by the attachment.

The attachment circuitry is MST-1 logic, physically located on gate A, board B1 in the 5406 Processing Unit. The interface between the system and the data recorder is a cable consisting of data and control lines.

The communications path between the central processing unit and the data recorder attachment is through the I/O channel. Using this channel, data and control information is transferred from the central processing unit to the attachment and data (from the delay line storage in the data recorder) is transferred from the attachment to the central processing unit. Also through the I/O channel, status is sent to the central processing unit under control of stored programmed instructions.

During the process of exchanging information, the attachment and central processing unit operate together in multiplexer mode. This means that the information transfer takes place between central processing unit cycles on a priority basis with other devices.

By means of a fixed cycle steal priority, I/O cycles may be interleaved between any two central processing unit cycles to fetch or store data to and from the attachment.



BR0791

Local Storage Register

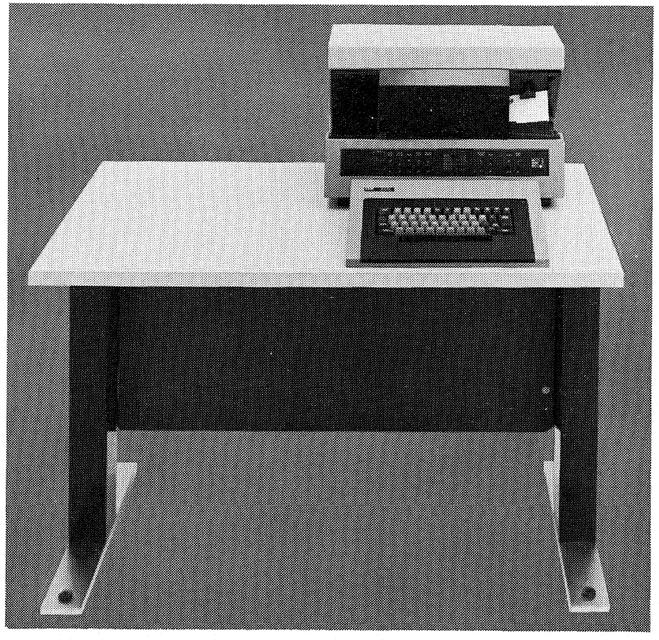
The local storage register in the central processing unit assigned to the data recorder attachment is the data recorder address register (DRAR). It must contain the leftmost or starting address of the data field in main storage when issuing a read or punch command.

Priority Request

The data recorder attachment uses the cycle steal method of communicating with main storage in the central processing unit. It is assigned priority clock two, request bit line four. This is twelfth in the order of priorities from highest to lowest. The select lines used by the attachment to request a cycle steal are lines five and seven.

DATA RECORDER

The IBM 5496 Model 1 Data Recorder with the online read/punch feature is used for the System/3 Model 6. With this feature installed, the model 6 can use the data recorder to read and punch the System/3 card. The data recorder can also be operated offline as a normal data recorder.



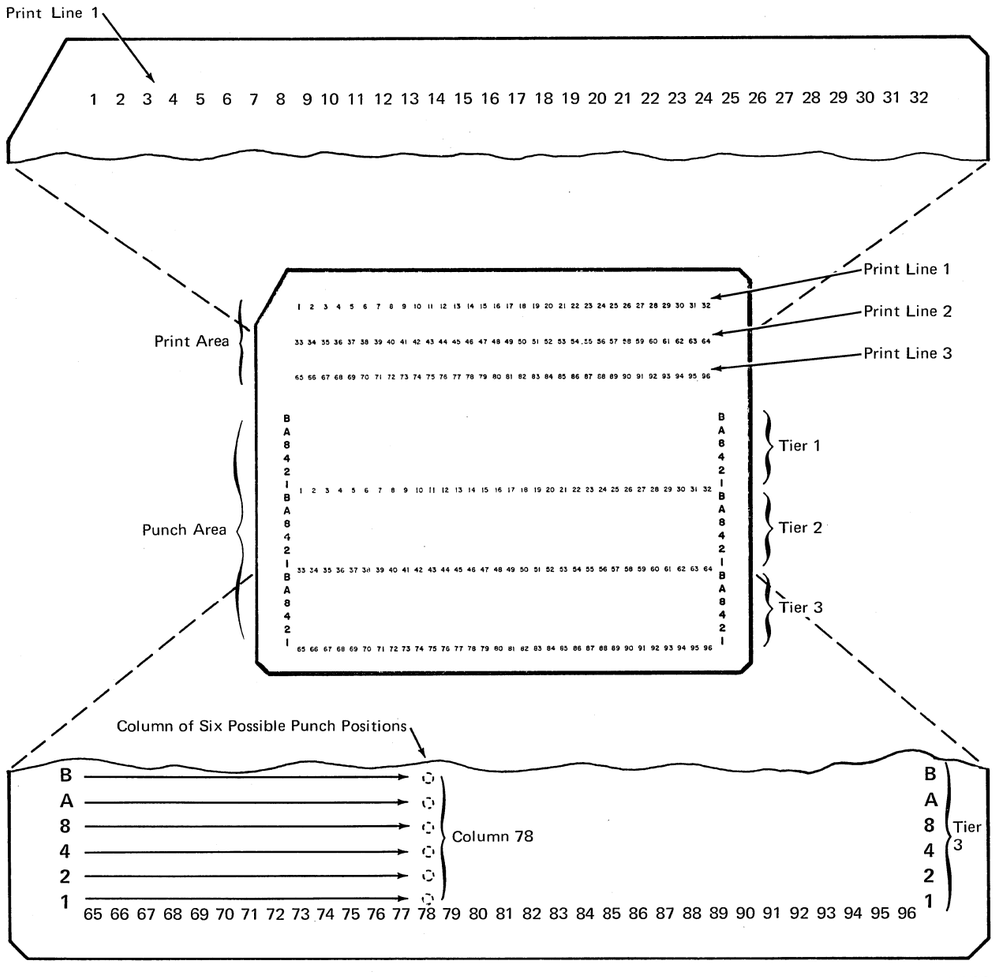
BR0792

96 COLUMN CARD

The 96 column card is divided into two sections. The upper section of the card is the print area and the lower section is the punch area. The lower section (punch area) is divided into three horizontal sections called tiers. Each tier contains 32 vertical groups of six punch positions. Each group of six punch positions is a card column. The punch positions are B, A, 8, 4, 2, and 1 from the top of the tier to the bottom.

The 96 card columns are arranged 32 columns in each tier as follows:

Tier 1 Columns 1-32
Tier 2 Columns 33-64
Tier 3 Columns 65-96



BR0793

All of the information contained on one card (from column 1 through column 96) is called a record, regardless of how many characters are punched in it.

CHARACTER SET

Any one of 64 different combinations of the six punch positions (six-bit card code) may be punched in a card column. The print area has 128 print positions numbered from 1 to 128; 96 of these correspond with the numbers in the punch area. Print positions 97 to 128 are available for use by other System/3 devices.

			Alphabetic Characters																										
			A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
Punch Positions	Zone	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B								
		A	A	A	A	A	A	A	A	A											A	A	A	A	A	A	A	A
	Digit	8							8	8									8	8							8	8
		4				4	4	4	4					4	4	4	4					4	4	4	4			
		2		2	2			2	2				2	2			2	2			2	2			2	2		
		1	1		1		1		1		1	1		1		1		1		1		1		1		1		1

BR0794

			Numeric Characters									
			0	1	2	3	4	5	6	7	8	9
Punch Positions	Zone	B										
		A	A									
	Digit	8									8	8
		4					4	4	4	4		
		2			2	2			2	2		
		1		1		1		1		1		1

BR0795

			Special Characters																										
			}	¢	.	<	(	+	|	!	$	*	)	;	¬	-	/	&	,	%	–	>	?	:	#	@	'	=	"	¢
Punch Positions	Zone	B	B	B	B	B	B	B	B	B	B	B	B	B	B														
		A	A	A	A	A	A	A	A								A	A	A	A	A	A	A						
	Digit	8		8	8	8	8	8	8	8	8	8	8	8			8	8	8	8	8	8	8	8	8	8	8	8	
		4				4	4	4	4			4	4	4	4					4	4	4	4			4	4	4	
		2		2	2			2	2	2	2			2	2			2	2			2	2	2	2			2	2	
		1			1		1		1		1		1		1		1		1		1		1		1		1		1	

Note: A blank character is represented by a column containing no punches. There is no printed graphic representation of the blank character.

BR0796

OFFLINE OPERATION

The two offline operations of the 5496 are data recording and verifying. The data recording operation consists of data entry by the operator, punching, and optional printing. The verifying operation consists of reading a previously punched card and comparing the data with corresponding (but identical if no errors have occurred) data being reentered by the operator.

The 5496 has a delay line buffer (memory) that is used in both data recording and verifying operations. For data recording, the buffer:

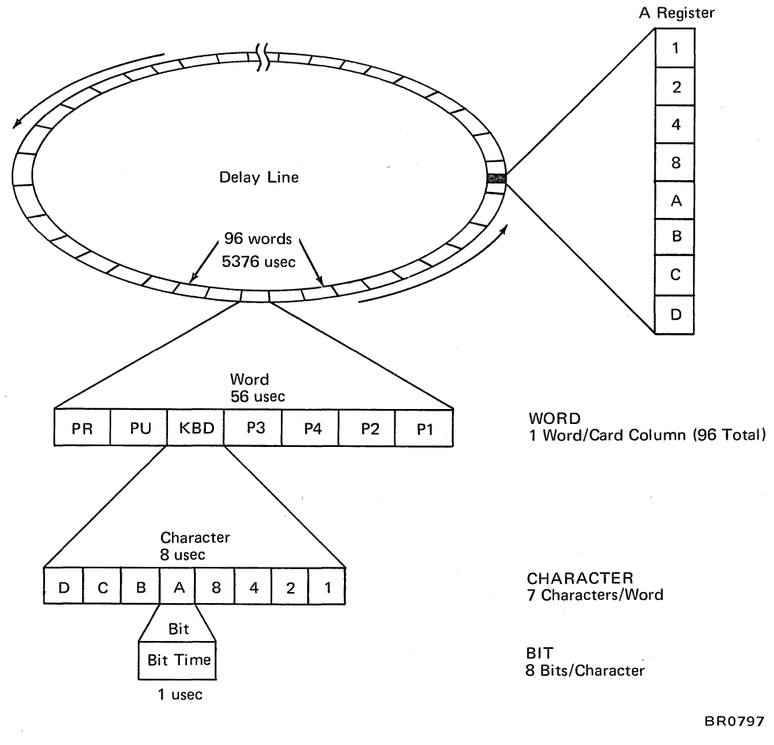
1. Allows the operator to store up to four programs for selection and use during data entry.
2. Allows the operator to enter a complete record (96 columns), correcting any detected errors as they are made before the card is punched.
3. Allows complete overlap of:
   a. Operator entry for card 3
   b. Punching of card 2
   c. Printing of card 1

For verifying, the delay line allows the characters from a previously punched card to be compared with corresponding characters as they are being reentered by the operator. First, the previously punched card is completely read into the delay line. Then, as characters are reentered they are compared to the corresponding characters on the delay line. If a non-compare occurs, the keyboard is locked and the error indicator is turned on.

MEMORY ORGANIZATION

As shown below, the delay line is divided into 96 words (corresponding to the 96 card columns) numbered 1 through 96. Each word is made up of seven characters: P1, P2, P4, and P3, corresponding to the four levels of stored program; KBD, the area into which input data from the keyboard is entered; and PU and PR, the respective areas from which punching and printing occur.

Each character on the delay line is made up of eight bits: bit 1, 2, 4, 8, A, B, C, and D. The character is sent to the delay line bit-by-bit and is continuously regenerated through the line, through an 8-bit register (the A register) and back onto the delay line until the data is replaced with new data or until machine power is interrupted. Bits are shifted through the line at one microsecond intervals. Each interval is called a bit time. The character times are eight microseconds and the words are 56 microseconds long. The memory cycle for a 96 word record is 5376 data bits. The eight bits in the A register are a part of the 5376-bit storage capacity.

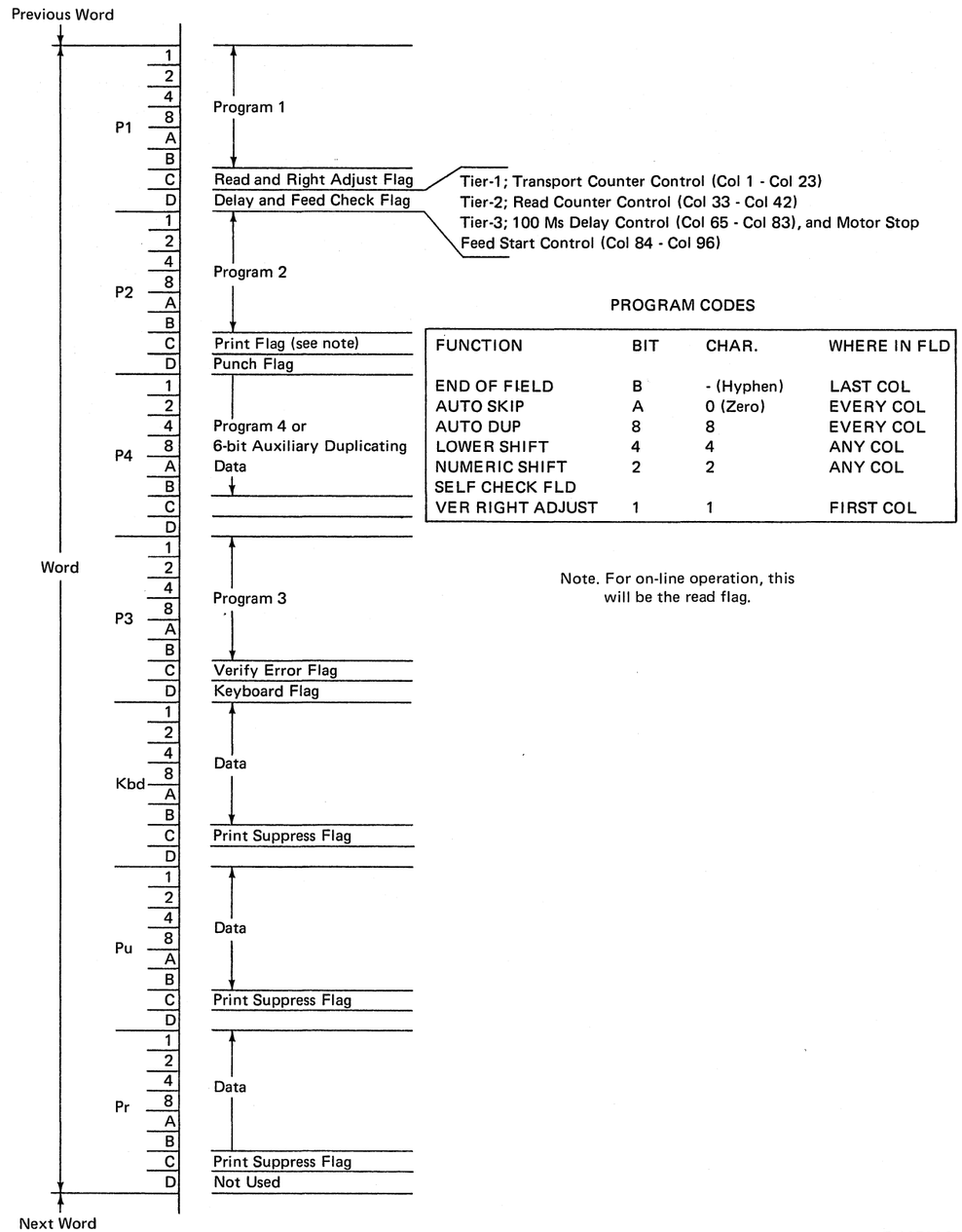


FLAG BITS

The figure to the right shows all the 56 bits contained in a word in memory. The four basic functions of read, data entry, punch, and print are controlled by reserved bit locations, called flag bits, written in the delay line memory.

A flag bit is a bit in memory defined by a particular bit time in a particular character of a word. (P3 bit time 'D' is the flag bit for the KBD area.) Before performing one of the functions, a flag bit for that function is written into each word in memory. When the control logic for a particular function calls for that function, a search for the first flag is initiated, starting in word 1 (column 1). When the first flag is found, that column is operated on and its flag bit is erased so that when the search for the next available column is started, the next word will contain the first flag bit. When all flags for the function are erased, the operation is complete.

Due to the physical layout of the 96 column card, reading, punching, and printing require that one column from each of the three punch tiers (three card columns: 1, 33, 65; 2, 34, 66; etc.) must be operated on during each search cycle. Therefore, two additional first flag scans of the delay line are started beginning in words 33 and 65 respectively, to permit operating on all three tiers at the time the card is in a position to be read, punched, or printed.



PROGRAM CODES

FUNCTION	BIT	CHAR.	WHERE IN FLD
END OF FIELD	B	- (Hyphen)	LAST COL
AUTO SKIP	A	0 (Zero)	EVERY COL
AUTO DUP	8	8	EVERY COL
LOWER SHIFT	4	4	ANY COL
NUMERIC SHIFT	2	2	ANY COL
SELF CHECK FLD			
VER RIGHT ADJUST	1	1	FIRST COL

Note. For on-line operation, this will be the read flag.

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PROGRAM CONTROL

The 5496 Data Recorder can operate with or without program control. To operate with program control, the program coding is first punched into a card to define areas of data fields in the card. The program card is then read into one of the four program areas on the delay line. Program level 1 (area P1) is the home program (machine operation is returned to this program level when the program switch on the operator panel is first turned on). Only one program level is effective at a time, but program levels can be changed at any time during the entry of a record. During data entry, the active program level defines the length and type of data fields to be entered for the record. Data fields are defined as manual, auto skip, and auto duplicate. Consecutive columns that must be keyed by the operator constitute a manual field. Consecutive columns in the card that are to be skipped are auto skip fields. Consecutive columns that are to receive the same data in every card are auto duplicate fields.

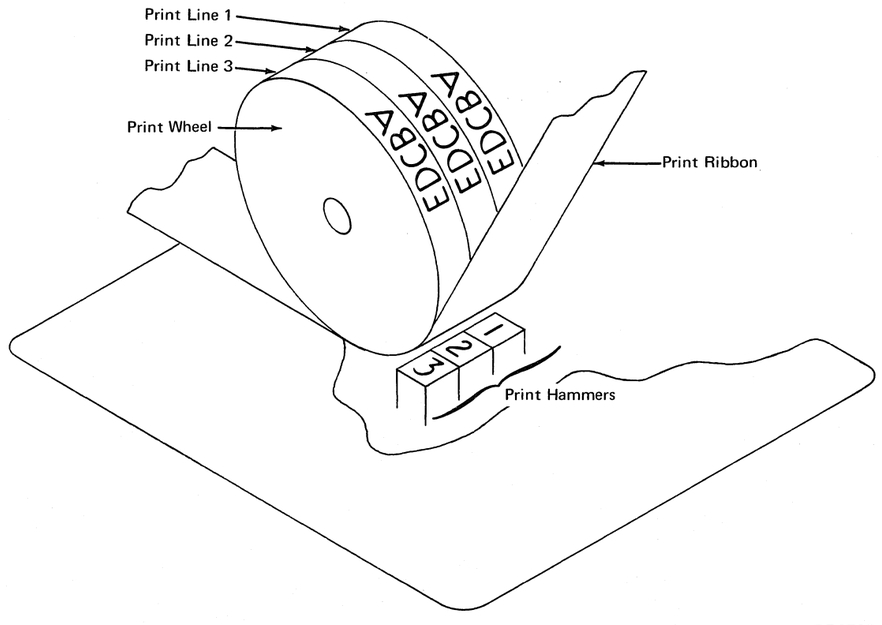
DATA RECORDING

Data can be either key-entered into the KBD area of memory or duplicated from the preceding record by transferring the appropriate data from the PU area in memory. This entry of data is not synchronous to card movement and punching. Data entry is controlled only by the rate of keying and program controls. A column indicator shows the next column in memory which will receive data. This indicator has no timing relationship to punching or printing. When 96 columns of data have been entered, a blank card (skip or release causes entry of blanks) is fed from the hopper, registered, and the entered data is transferred from the KBD area in memory to the PU area in memory. The card is incremented through the punch station at a rate of 20 increments/second (effective rate of 60 columns per second), punching as required while the card is stopped after each increment. After the card has moved 32 increments during punching, a printing operation begins if the print switch was on when keying occurred for the record. If the print switch was on, print flags are written into memory and the record is transferred from the PU area to the PR area in storage.

The printer consists of a continuously running wheel that has three sets of 63 characters engraved on the periphery; the 64th character is a space and is blank on the print wheel. The figure shows how the print wheel is mounted above the card and the three print hammers are mounted below the card path. The print station is 33 columns from the punch station. When column 32 is being punched in the card, column 0 is at the print station. After the card clears the punch station, another card can be fed from the hopper and punching can start on this card. This means that printing of record 1, punching of record 2, and data entry for record 3 can occur simultaneously.

A card is read into memory by pressing the read key. This action moves the top card in the hopper into the transport to be read. Data is read from the card into the PU area in storage enabling that card to be remade. All or portions of the card can be duplicated in the next record.

To synchronize the card movement with the circuit operations, certain controls are used. A card sensor control detects that a card has moved from the hopper to the transport rolls. A magnetic emitter driven with the transport mechanics provides three transport control pulses. 'Transport dwell' designates the start of dwell time, 'punch on' turns the punches on, and 'punch off' turns the punches off. These pulses also synchronize the control logic with card location for reading, punching, and printing.



BR0799

There are circuits to check for misfeed, hopper jam, or transport jam conditions which are indicated by a feed check light on the operator panel. The operator panel also contains the column indicator which:

1. Indicates to the operator the next card data column to be acted upon, and
2. Is used in conjunction with the CE panel to display the bits of any storage position. The CE panel is located on the end of the electronics gate in the 5496.

Details of the 5496 Data Recorder Model 1 are contained in the following manuals:

IBM 5496 Data Recorder Operator's Guide, Order No. GA21-9086
IBM 5496 Data Recorder Field Engineering Theory of Operations Manual, Order No. SY31-0220
IBM 5496 Data Recorder Field Engineering Maintenance Diagrams Manual, Order No. SY31-0221
IBM 5496 Data Recorder Field Engineering Maintenance Manual, Order No. SY31-0219

ONLINE OPERATION

Online and offline control of the data recorder is determined by the setting of the 'DATA RCRDR' switch on the CPU operator console. Setting the DATA RCRDR switch to ON LINE places the data recorder under control of the CPU program if the 5496 is otherwise ready. Conditions of the 5496 that prevent program operation are:

1. Stacker full
2. Hopper empty
3. Hopper jam
4. Transport jam
5. Punch/verify switch on VERIFY
6. Auto record release switch set to OFF

While under program control, all the keyboard keys on the 5496 are held restored to prevent accidental operator intervention. (The release key is unlocked in the event of a feed error or a card jam to permit the operator to clear the trouble from the machine.) The online/offline switch can be set to OFF LINE at any time. However, an operation in progress at the time of setting the switch is completed and the 5496 becomes an offline device after the successful completion of this operation.

The 5496, when used as an online printing punch and card reader, is attached to the model 6 through a cable of 25 feet maximum length. This cable contains the signal lines necessary for connecting the 5496 to the data recorder attachment in the processing unit. The data recorder attachment controls operations of the 5496 which are initiated by the processor program. Information is transferred to and from processor storage by using the cycle steal capabilities of the CPU. The delay line buffer in the 5496 allows the CPU to overlap data recorder operations with operations of other I/O devices controlled by the system.

The two online functions of the 5496 are card reading and card punching. Both functions, however, cannot be performed on the same card in one operation. (A card punched by the data recorder on command from the CPU program must be reinserted in the card hopper to be read under program control.) In a card read operation, the CPU program issues a start I/O instruction which causes the 5496 to read data from a card into the delay line storage. The data is transferred from the delay line in the 5496 to CPU storage with 96 cycle steal cycles. This data in 6-bit card code is translated into 8-bit EBCDIC by a translator on the data bus in (DBI) with each transfer of a data character to the CPU. The character codes figure on this page shows both the card code and EBCDIC for the 64 character set used by the 5496.

In a card punch operation, the data is transferred from CPU storage to the 5496 delay line via cycle steal cycles until an entire record has been transferred (96 cycle steals). This data from the CPU is translated from 8-bit EBCDIC to 6-bit card code by a translator on data bus out (DBO) with each transfer of a data character to the data recorder. When the 96 data characters have been transferred, the data recorder circuits feed the top card from the hopper into the punch station and punch the data into the card. Printing of punched data is under control of the print switch located on the operator panel of the 5496 Data Recorder. An entire card must be read or punched with each operation initiated by the CPU. Any programs previously entered into the 5496 delay line as a result of an offline operation are not effective when the 5496 is operated as an online device.

EBCDIC Binary Bit Position								Hex	5496 Card Code Punch Positions						Character Graphic
0	1	2	3	4	5	6	7		B	A	8	4	2	1	
1	1	0	0	0	0	0	1	C 1	B	A				1	A
1	1	0	0	0	0	1	0	C 2	B	A			2		B
1	1	0	0	0	0	1	1	C 3	B	A			2	1	C
1	1	0	0	0	1	0	0	C 4	B	A		4			D
1	1	0	0	0	1	0	1	C 5	B	A		4		1	E
1	1	0	0	0	1	1	0	C 6	B	A		4	2		F
1	1	0	0	0	1	1	1	C 7	B	A		4	2	1	G
1	1	0	0	1	0	0	0	C 8	B	A	8				H
1	1	0	0	1	0	0	1	C 9	B	A	8			1	I
1	1	0	1	0	0	0	1	D 1	B					1	J
1	1	0	1	0	0	1	0	D 2	B				2		K
1	1	0	1	0	0	1	1	D 3	B				2	1	L
1	1	0	1	0	1	0	0	D 4	B			4			M
1	1	0	1	0	1	0	1	D 5	B			4		1	N
1	1	0	1	0	1	1	0	D 6	B			4	2		O
1	1	0	1	0	1	1	1	D 7	B			4	2	1	P
1	1	0	1	1	0	0	0	D 8	B		8				Q
1	1	0	1	1	0	0	1	D 9	B		8			1	R
1	1	1	0	0	0	1	0	E 2		A			2		S
1	1	1	0	0	0	1	1	E 3		A			2	1	T
1	1	1	0	0	1	0	0	E 4		A		4			U
1	1	1	0	0	1	0	1	E 5		A		4		1	V
1	1	1	0	0	1	1	0	E 6		A		4	2		W
1	1	1	0	0	1	1	1	E 7		A		4	2	1	X
1	1	1	0	1	0	0	0	E 8		A	8				Y
1	1	1	0	1	0	0	1	E 9		A	8			1	Z
1	1	1	1	0	0	0	1	F 1						1	1
1	1	1	1	0	0	1	0	F 2					2		2
1	1	1	1	0	0	1	1	F 3					2	1	3
1	1	1	1	0	1	0	0	F 4				4			4
1	1	1	1	0	1	0	1	F 5				4		1	5
1	1	1	1	0	1	1	0	F 6				4	2		6
1	1	1	1	0	1	1	1	F 7				4	2	1	7
1	1	1	1	1	0	0	0	F 8			8				8
1	1	1	1	1	0	0	1	F 9			8			1	9
1	1	1	1	0	0	0	0	F 0		A					0

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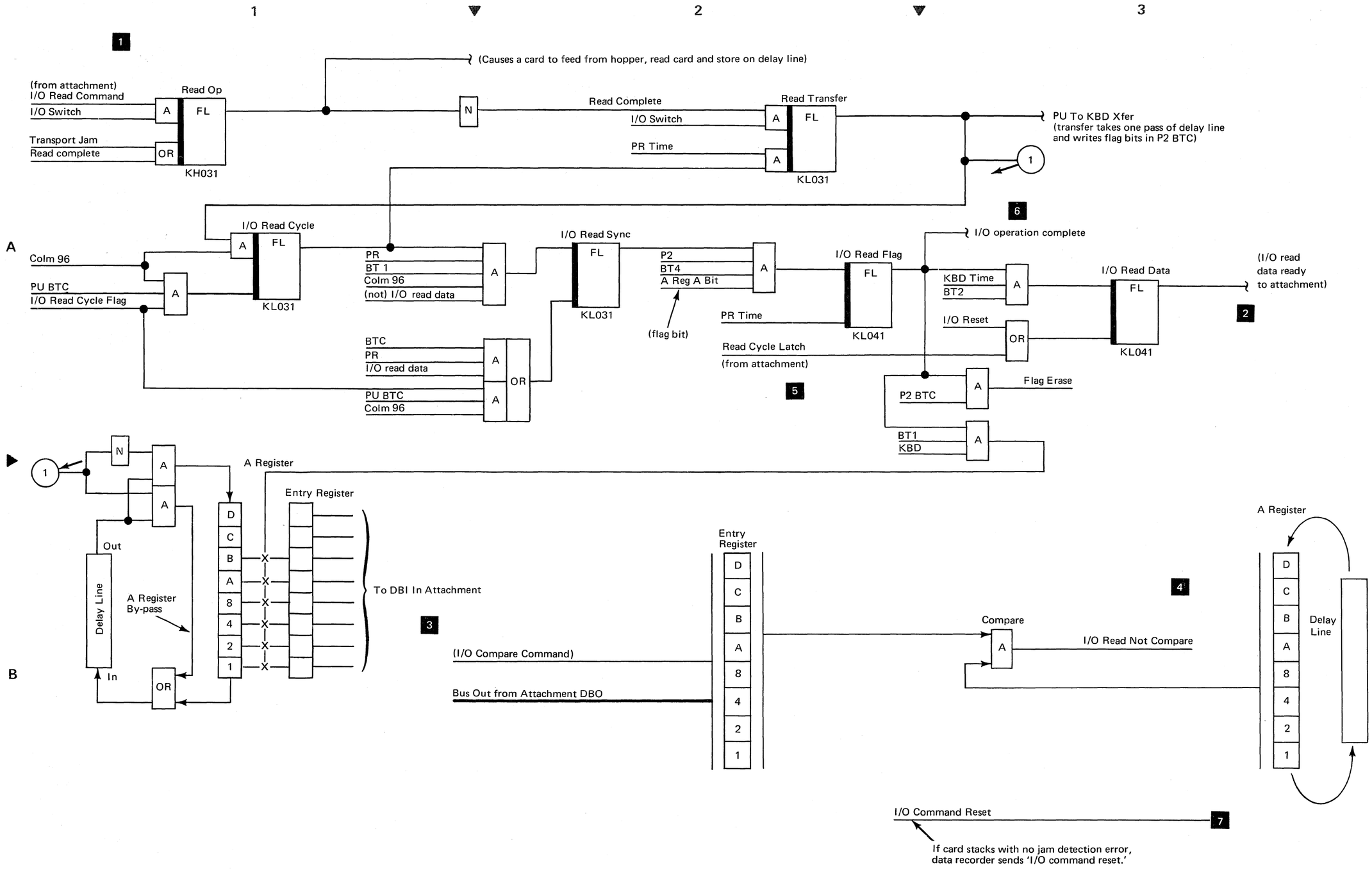
EBCDIC Binary Bit Position								Hex	5496 Card Code Punch Positions						Character Graphic
0	1	2	3	4	5	6	7		B	A	8	4	2	1	
1	1	0	0	0	0	0	0	C 0	B	A					}
0	1	0	0	1	0	1	0	4 A	B	A	8		2		¢
0	1	0	0	1	0	1	1	4 B	B	A	8		2	1	. (period)
0	1	0	0	1	1	0	0	4 C	B	A	8	4			<
0	1	0	0	1	1	0	1	4 D	B	A	8	4		1	(
0	1	0	0	1	1	1	0	4 E	B	A	8	4	2		+
0	1	0	0	1	1	1	1	4 F	B	A	8	4	2	1	| (logical OR)
0	1	0	1	1	0	1	0	5 A	B		8		2		!
0	1	0	1	1	0	1	1	5 B	B		8		2	1	$
0	1	0	1	1	1	0	0	5 C	B		8	4			*
0	1	0	1	1	1	0	1	5 D	B		8	4		1	)
0	1	0	1	1	1	1	0	5 E	B		8	4	2		;
0	1	0	1	1	1	1	1	5 F	B		8	4	2	1	¬ (logical NOT)
0	1	1	0	0	0	0	0	6 0	B						— (dash)
0	1	1	0	0	0	0	1	6 1		A				1	/
0	1	0	1	0	0	0	0	5 0		A	8		2		&
0	1	1	0	1	0	1	1	6 B		A	8		2	1	,
0	1	1	0	1	1	0	0	6 C		A	8	4			%
0	1	1	0	1	1	0	1	6 D		A	8	4		1	_ (underscore)
0	1	1	0	1	1	1	0	6 E		A	8	4	2		>
0	1	1	0	1	1	1	1	6 F		A	8	4	2	1	?
0	1	1	1	1	0	1	0	7 A			8		2		:
0	1	1	1	1	0	1	1	7 B			8		2	1	#
0	1	1	1	1	1	0	0	7 C			8	4			@
0	1	1	1	1	1	0	1	7 D			8	4		1	'
0	1	1	1	1	1	1	0	7 E			8	4	2		=
0	1	1	1	1	1	1	1	7 F			8	4	2	1	"
0	1	0	0	0	0	0	0	4 0	no punches						blank (space)

Note: A blank character is represented by a column containing no punches. There is no printed graphic representation of the blank character.

BR0800


1
2
3
(Causes a card to feed from hopper, read card and store on delay line)
(from attachment)
I/O Read Command
I/O Switch
Transport Jam
Read complete
Read Op
A
OR
FL
KH031
N
Read Complete
I/O Switch
PR Time
Read Transfer
KL031
PU To KBD Xfer
(transfer takes one pass of delay line and writes flag bits in P2 BTC)
I/O Read Cycle
KL031
Colm 96
PU BTC
I/O Read Cycle Flag
PR
BT 1
Colm 96
(not) I/O read data
I/O Read Sync
KL031
P2
BT4
A Reg A Bit
(flag bit)
I/O Read Flag
KL041
PR Time
BTC
PR
I/O read data
PU BTC
Colm 96
Read Cycle Latch
(from attachment)
I/O operation complete
KBD Time
BT2
I/O Reset
I/O Read Data
KL041
(I/O read data ready to attachment)
P2 BTC
Flag Erase
BT1
KBD
A Register
Entry Register
Out
Delay Line
A Register By-pass
In
To DBI In Attachment
(I/O Compare Command)
Bus Out from Attachment DBO
Compare
I/O Read Not Compare
Delay Line
I/O Command Reset
If card stacks with no jam detection error, data recorder sends 'I/O command reset.'

5496 READ OPERATION

To use the 5496 Data Recorder as an input-output device for the model 6 system, perform the following steps:

- Set the following switches on the data recorder (see figure on this page):
  1. Program switch to OFF.
  2. Verify switch to PUNCH.
  3. Auto record release switch to AUTO.

- On the central processing unit console, position the data recorder online switch to ON LINE. This activates the line 'I/O switch' in the data recorder attachment which is the major control line in the attachment. In the data recorder, this line performs a record erase and holds this line active which locks out all of the keys and most of the switches on the operator console (of the data recorder). The record erase is inhibited during a feed check condition to allow operator recovery. If no error condition exists in the 5496, the 'I/O ready' line is activated.

To read prepunched data cards, the operator loads the cards in the 5496 hopper and sets up the machine as stated above. The data recorder attachment issues the I/O read command signal. This sets the 'read op' latch and a normal read operation is initiated. (Refer to 1 .)

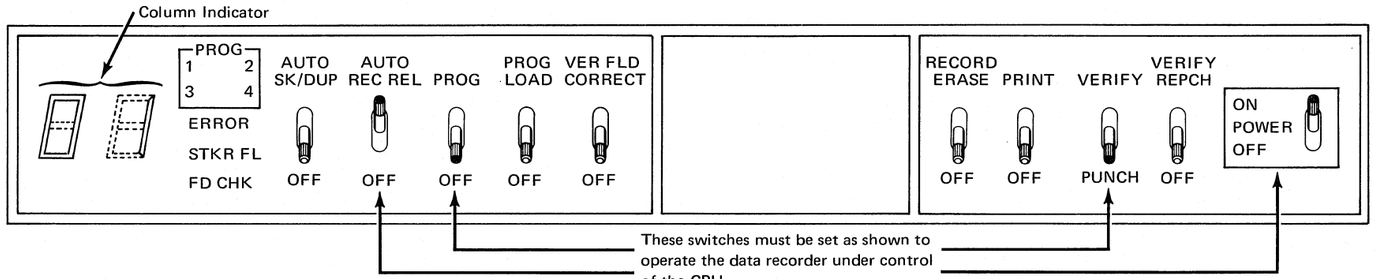
The data from the cards is read into the PU section of delay line memory. Read flags P1, BT-C are used for this transfer. At the completion of the read operation the signal 'read complete' sets the 'I/O read transfer' latch. This latch is on for one memory cycle, and transfers the data in the PU section to the KBD section (the KBD section is used for data transfer and the punch section is used with the compare command) of memory without erasing the PU section. It also writes a flag bit in P2 BTC of every section of memory. At the end of the read transfer cycle (5.4 ms), the 'I/O read transfer' latch is reset. With the 'I/O read cycle' latch set, the 'I/O read sync' latch can be set at Col 96, PR, BT1 and CLB time. This allows the 'I/O read flag' latch to start searching for flags in P2 BTC starting in Col 1. When a flag bit is found, the 'I/O read flag' latch is set at P2 BT4 and CLB time and the following sequence of events occurs:

1. The column indicator is updated to indicate the column that is being transferred to the user.
2. The flag (P2 BTC) is erased.
3. The entry register is reset at P2 time.

At KBD BT1 and CLB time the A register is transferred to the entry register, and this data appears on the I/O bus out to the user; and at KBD BT2 the 'I/O read data' latch is set which brings up the 'read data ready' line (refer to 2) to the attachment. At this time the I/O data is valid and the attachment can sample the I/O bus out. The attachment puts the data on the I/O bus out (refer to 3). The entry register is reset and the I/O bus out data is loaded into the entry register at KBD BTC. The data in the entry register is then compared to the A register at PU time (via the data recorder verify circuits) and if a non compare is present, the 'read non compare' line (refer to 4) is active to the user at PU BT2. The I/O compare command is active when the data recorder is online to the System/3 Model 6.

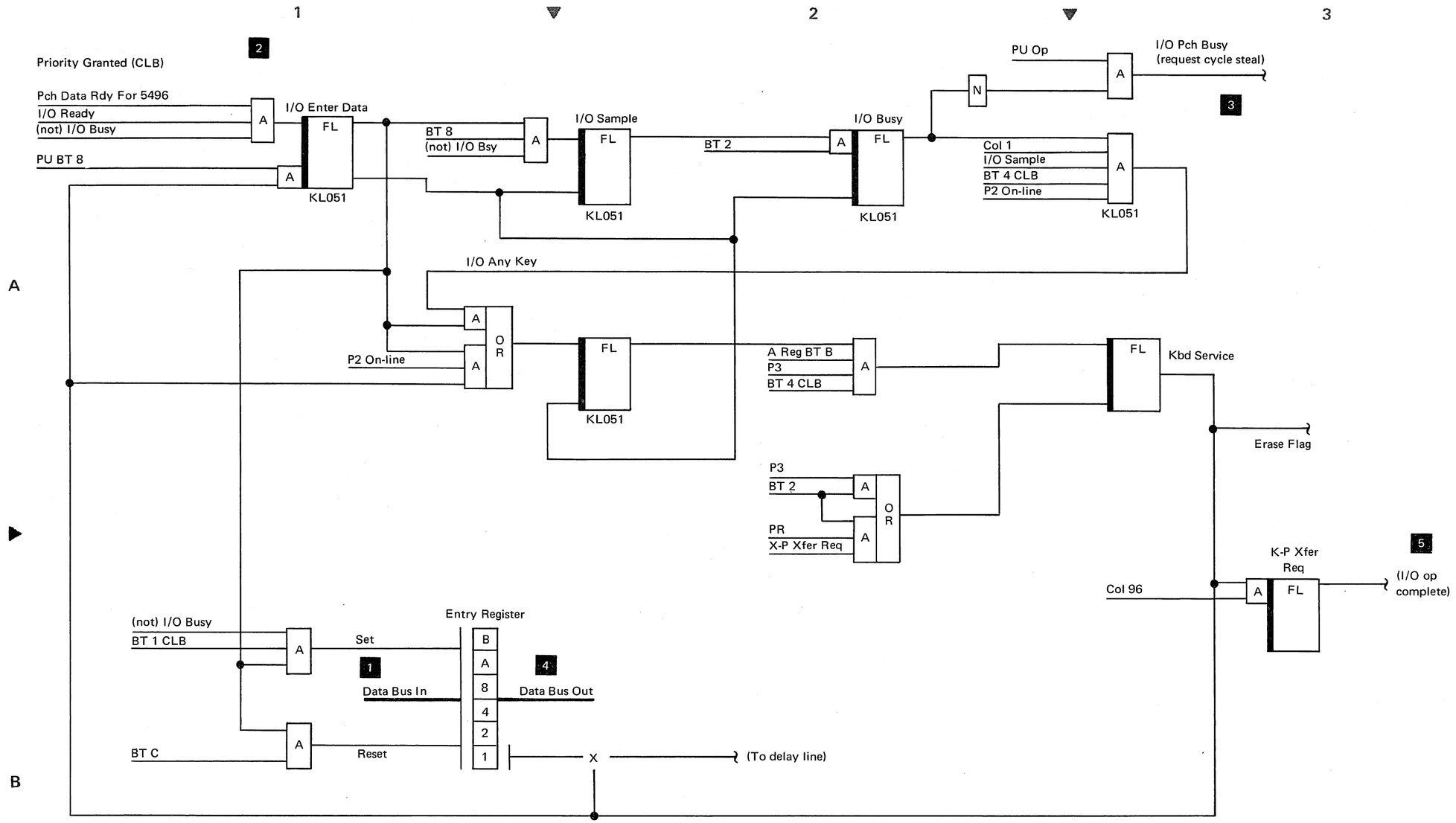
When the 'read data ready' line (refer to 2) is active, the user also has the responsibility to bring up the 'read cycle' line (refer to 5) to reset the 'I/O read data' latch. If the 'read cycle' line is active before the next PR BTC time, the 'I/O read sync' latch is not reset and therefore the next data transfer occurs 56 μsec after the first data transfer. If the 'read cycle' line is active after PR BTC, a minimum delay of approximately 5.4 msec occurs. There is no restriction on the attachment relevant to the minimum data transfer rate. The data transfer continues until the 'I/O read flag' latch is set at Col 96 time by the flag in Col 96 P2 BTC. With the 'I/O read flag' latch set, Col 96 PU will reset the 'I/O read cycle' latch and the 'I/O read sync' latch. This signal is also sent to the attachment as 'operation complete' (refer to 6). After the last column is read, the card continues to pass through the transport and a check is made to insure that the card cleared the read station. If the card clears the read station, a signal, 'command reset', is sent to the attachment (refer to 7).

The attachment can issue another I/O read command after receiving 'command reset' from the 5496.



Data Recorder Operators Panel

BR0801


1
2
3
A
B
Priority Granted (CLB)
Pch Data Rdy For 5496
I/O Ready
(not) I/O Busy
PU BT 8
A
I/O Enter Data
FL
KL051
BT 8
(not) I/O Bsy
I/O Sample
BT 2
I/O Busy
PU Op
N
I/O Pch Busy
(request cycle steal)
Col 1
I/O Sample
BT 4 CLB
P2 On-line
I/O Any Key
O
R
A Reg BT B
P3
BT 4 CLB
Kbd Service
Erase Flag
P3
BT 2
PR
X-P Xfer Req
K-P Xfer
Req
Col 96
(I/O op
complete)
(not) I/O Busy
BT 1 CLB
Set
Entry Register
B
A
8
4
2
1
Data Bus In
Data Bus Out
BT C
Reset
X
(To delay line)

5496 PUNCH OPERATION

To use the 5496 Data Recorder as an input-output device for the model 6, perform the following steps:

- Set the following switches on the data recorder:
  1. Program switch to OFF.
  2. Verify switch to PUNCH.
  3. Auto record release switch to AUTO.
- On the central processing unit console, position the data recorder online switch to ON LINE. This activates the line 'I/O switch' in the data recorder attachment and is the major control line in the attachment. In the data recorder, this line performs a record erase and holds this line active which locks out all of the keys and most of the switches on the operator console (of the data recorder). The record erase is inhibited during a feed check condition to allow operator recovery. If no error condition exists in the 5496, the 'I/O ready' line is activated.

To punch data cards, the operator sets up the 5496 as in the read operation, and loads the hopper with cards to be punched. The cards can be prepunched and data added, or they can be blank cards. If printing is desired, the operator must turn on the print switch on the 5496 console.

Any number of data columns can be punched in a card up to a maximum of 96 columns. All 96 columns must be entered. The columns to be skipped are loaded with blanks.

The I/O punch operation simulates a keyboard entry operation. The attachment puts the data to be entered on the I/O bus in lines (refer to 1) and then brings up the 'I/O enter data' line (refer to 2). This sets the 'I/O enter data' latch. The following BT8, the 'I/O sample' latch is set. The following BTC resets the entry register, and the next BT1 and CLB loads the I/O data bus into the entry register. The following BT2 sets the 'I/O busy' latch which brings up the 'I/O busy' line (refer to 3) to signal the attachment to drop the 'I/O enter data' line. The I/O bus in data is now available to the attachment on the I/O bus out and the attachment can do a compare to test for valid data transfer (refer to 4).

The following Col 1 P2 BT4 and CLB, the 'I/O any key' latch is set. This allows a normal keyboard service cycle which starts a search for KBD flags. When a KBD flag is found, the 'KBD' latch is set and the data is entered into delay line memory at KBD time. The following PU BT8 resets the 'I/O enter data' latch, 'I/O sample' latch, 'I/O busy' latch, and the 'I/O any key' latch. Resetting of the 'I/O busy latch drops the 'I/O busy' line to the attachment and tells it that the 5496 is ready for the next data input. If the attachment brings up the 'I/O enter data' line before the end of the next P2 time, the next data transfer is entered into memory 56 μsec after the first data transfer, which is the maximum data transfer rate. If the attachment fails to enter new data before the end of P2 time, a minimum delay of approximately 5.4 ms occurs before the next data transfer into memory. There is no minimum data transfer rate.

When the data for column 96 is entered, the signal 'set K-P transfer req fl' is generated, and this is sent to the attachment as 'operation complete' (refer to 5). Because the auto record release switch is set to AUTO, the 5496 now feeds a card from the hopper, and a normal punch and print operation is performed.

If a feed check occurs and a card fails to feed from the hopper, the signal, 'I/O hopper jam' is sent to the attachment. The signal 'I/O feed check' is sent to the attachment if a card jam occurs in the transport. If a feed check occurs, the keyboard function release key is unlocked and the operator uses normal feed check recovery procedures to clear the condition. A feed check also drops the signal 'I/O ready' until the feed check condition is cleared.

The I/O bus lines can be tested by bringing up the diagnostic command to the 5496. This allows the data on the I/O bus in lines to be gated to the I/O bus out lines and allows the user to exercise the data lines for diagnostic purposes.

LOAD I/O INSTRUCTION

- The load I/O instruction consists of three or four bytes.
- The load I/O instruction selects the data recorder when the device address equals F (hexadecimal).
- Two bytes in storage addressed by the operand address, are loaded into the data recorder address register (DRAR).

The load I/O instruction is used to load the DRAR, which is located in the CPU local store register (LSR), with the starting address used for a start I/O read, or punch operation. The load I/O instruction must be executed prior to each start I/O read, or punch instruction issued.

Q Byte Description

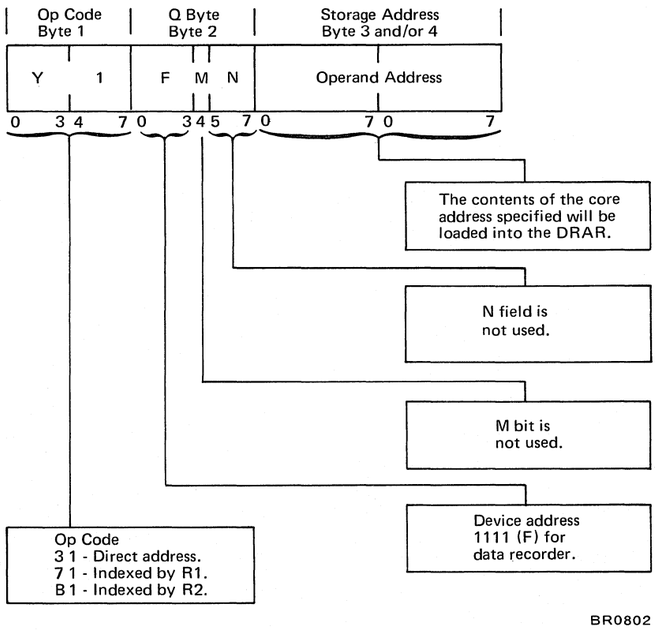
The upper four bits (bits 0-3) specify the device address of the data recorder. Bit 4 is the M bit. This bit is not presently used, and should be zero to allow for future use. Bits 5, 6, and 7 are the N field. In this instruction the N field is not used and should always be zero.

The load I/O instruction is accepted only if the data recorder is not busy. If the device addressed by the load I/O instruction is busy, the load I/O instruction shall be equivalent to a wait until the condition is no longer present. When the condition is no longer present, the load I/O instruction shall be executed.

Parity and Error Conditions

A parity error detected by the attachment results in a processor check stop, and the processor check light comes on.

LOAD I/O (LIO) INSTRUCTION FORMAT



BR0802

TEST I/O AND BRANCH INSTRUCTION

- The test I/O instruction consists of three or four bytes.
- The test I/O instruction selects the data recorder when the device address equals F (hexadecimal).
- The test I/O instruction tests for the following conditions:
  1. Busy
  2. I/O check or not ready

The test I/O instruction tests for a specific condition designated by its Q byte. If the condition tested for exists, the test I/O causes a branch to the operand address.

Q Byte Description

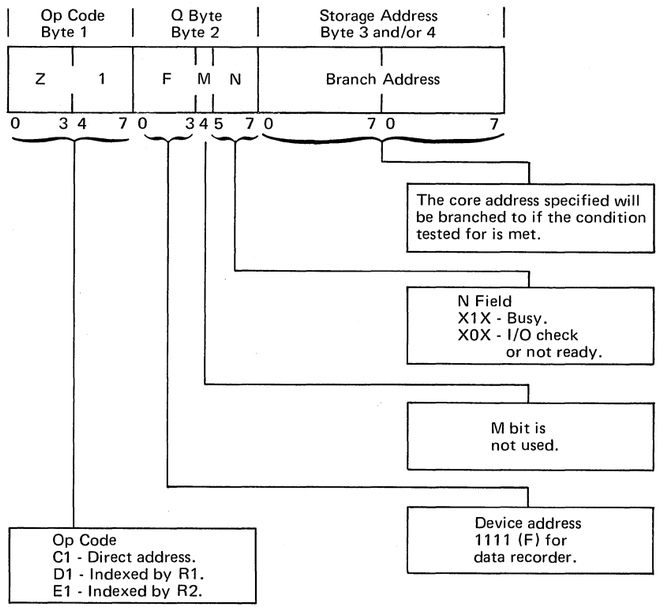
The upper four bits (0-3) specify the device address of the data recorder. Bit 4 is the M bit. This bit is not presently used and should be zero to allow for future use. Bits 5, 6, and 7 are the N field. The N field is used to specify the condition to be tested for.

The data recorder always accepts a test I/O instruction.

Parity and Error Conditions

A parity error detected by the attachment results in a processor check stop, and the processor check light comes on.

TEST I/O (TIO) INSTRUCTION FORMAT



BR0803

ADVANCE PROGRAM LEVEL INSTRUCTION

- The advance program level instruction consists of three bytes.
- The advance program level instruction selects the data recorder when the device address equals F (hexadecimal).
- The advance program level instruction tests the data recorder for conditions of busy, and I/O check or not ready.

The advance program level operation causes the program to loop until the condition tested for is no longer present, and then proceeds to execute the next sequential instruction.The unconditional advance becomes equivalent to a no op.

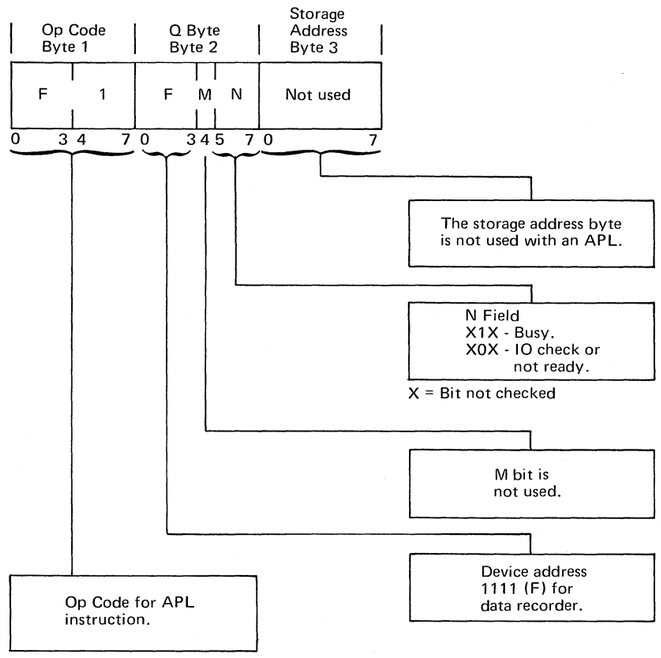
Q Byte Description

The upper four bits (0-3) specify the device address of the data recorder. Bit 4 is the M bit. This bit is not presently used and should be zero to allow for future use. Bits 5, 6, and 7 are the N field. The N field is used to specify the condition to be tested for.

Parity and Error Conditions

A parity error detected by the attachment results in a processor check stop, and the processor check light comes on.

ADVANCE PROGRAM LEVEL (APL) INSTRUCTION FORMAT



BR0804

SENSE I/O INSTRUCTION

- The sense instruction consists of three or four bytes.
- The sense instruction selects the data recorder when the device address equals F (hexadecimal).
- When bit 6 of the N field equals 0, the DRAR is stored in the storage address specified.
- When bit 6 of the N field equals 1, two status bytes are loaded into the storage address specified.

The purpose of this instruction is to store data from an I/O attachment or an LSR assigned to the attachment into the main storage location of the effective address.

Q Byte Description

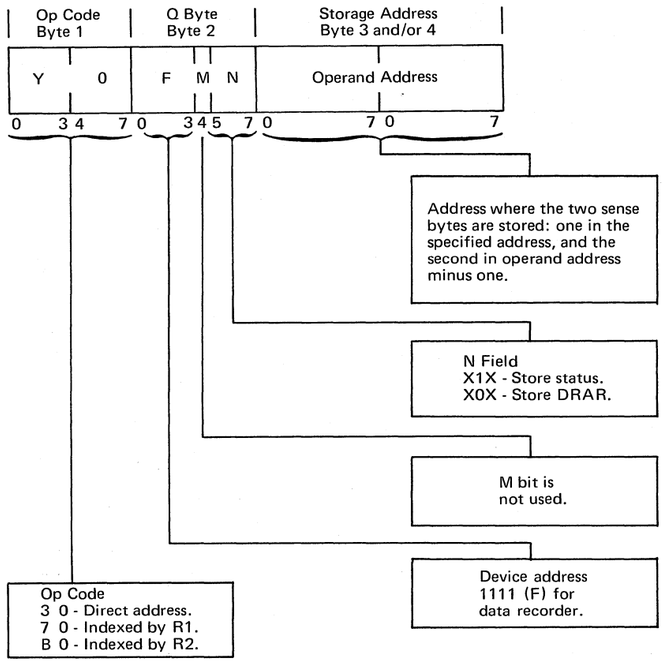
The upper four bits (0-3) specify the device address of the data recorder. Bit 4 is the M bit. This bit is not presently used and should be zero to allow for future use. Bits 5, 6, and 7 are the N field. Bits 5 and 7 of the N field are not used and should be zero. Bit 6 of the N field is used to determine if the LSR, or two status bytes are to be stored in the specified address.

The data recorder always accepts a sense instruction.

Parity and Error Conditions

A parity error detected by the attachment results in a processor check stop, and the processor check light comes on.

SENSE (SNS) INSTRUCTION FORMAT



First Byte

Bit

0 Off line.
1 Transport jam.
2 Stacker full, hopper empty, or hopper jam.
3 Not used.
4 Incorrect card code.
5 Compare error on read or punch I/O cycle or failure to take 96 cycle steals.
6 Reserved for FE use.
7 Reserved for FE use.

Second Byte

This byte is a diagnostic data byte located in the multi-purpose register. The diagnostic data byte was originally sent to the data recorder by a diagnostic start I/O.

BR0805A

START I/O INSTRUCTION

- The start I/O instruction consists of three bytes.
- The start I/O instruction selects the data recorder when the device address equals F (hexadecimal).
- The start I/O instruction is issued to the data recorder to read a card or punch and print a card.
- Printing is performed only if the print switch on the data recorder is on.

The purpose of the start I/O instruction is to command the I/O attachment to initiate a data transfer operation between the data recorder and the CPU main storage.

Q Byte Description

The upper four bits (0-3) specify the device address of the data recorder. Bit 4 is the M bit. The M bit is not presently used and should be zero to allow for future use. Bits 5, 6, and 7 are the N field. Bit 5 of the N field is not used and should be zero. Bits 6 and 7 of the N field are used to specify a read or punch and print operation.

Any start I/O command issued to the data recorder when offline lights the I/O attention lamp. It may be turned off by system reset or by switching the online/offline switch to ON LINE. Any start I/O instruction issued to the data recorder when online and busy, is looped until busy drops.

Parity and Error Conditions

A parity error detected by the attachment results in a processor check stop, and the processor check light comes on.

DIAGNOSTIC INSTRUCTIONS

Diagnostic Start I/O

Device Address: 1111 (F)

M Bit: Not presently used, but should be zero to allow for future use.

N Field:

Bit 5 6 7
X 1 1—Diagnostic (data)

This command is issued to test the punch and read logic circuitry used in communicating between the CPU and the data recorder. A byte of data is issued to the data recorder attachment during the control code cycle of the diagnostic start I/O instruction.

This byte is translated from EBCDIC to card code by the channel. It is sent to the data recorder attachment, where it is stored in the DBO and presented to the data recorder. It then returns to the attachment for comparison.

Following this instruction with a sense instruction provides the following information:

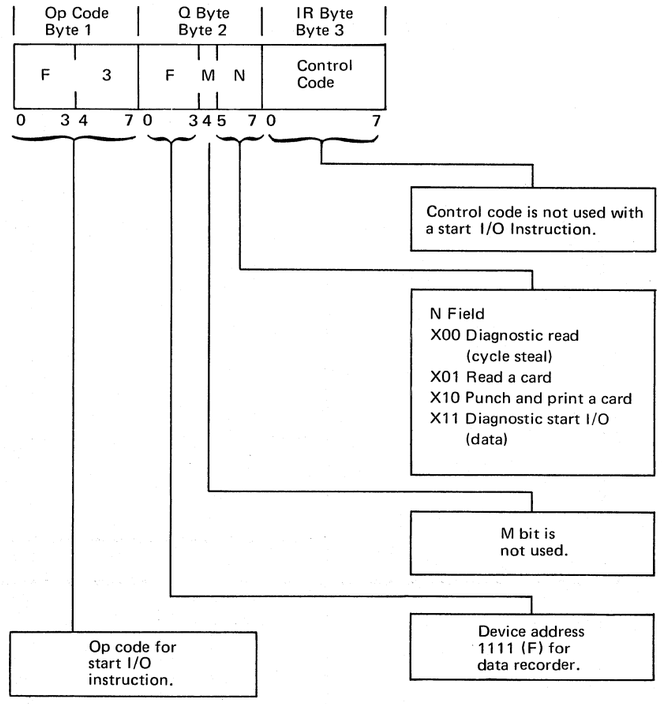
1. First byte—bit 5: This bit is on if the byte sent to the data recorder did not match the byte returned by the data recorder. The bit being on would indicate a problem in the data recorder or the interface between the data recorder and the attachment.
2. Second byte: This byte contains the data given to the attachment on the previous diagnostic start I/O (in case of a compare error, this is not the same as the byte returned by the data recorder). If this byte does not agree with the byte sent on the diagnostic start I/O, it would indicate a problem in either the attachment or the channel translator(s).

Note: The sense instruction must be issued before the next start I/O instruction to make the comparison valid, since the byte of data issued during the diagnostic start I/O instruction is reset by the next start I/O instruction. The data recorder is in a diagnostic mode of operation until system reset is depressed, or any other start I/O instruction is issued. The data byte is also latched up until the diagnostic mode is terminated. No card motion takes place.

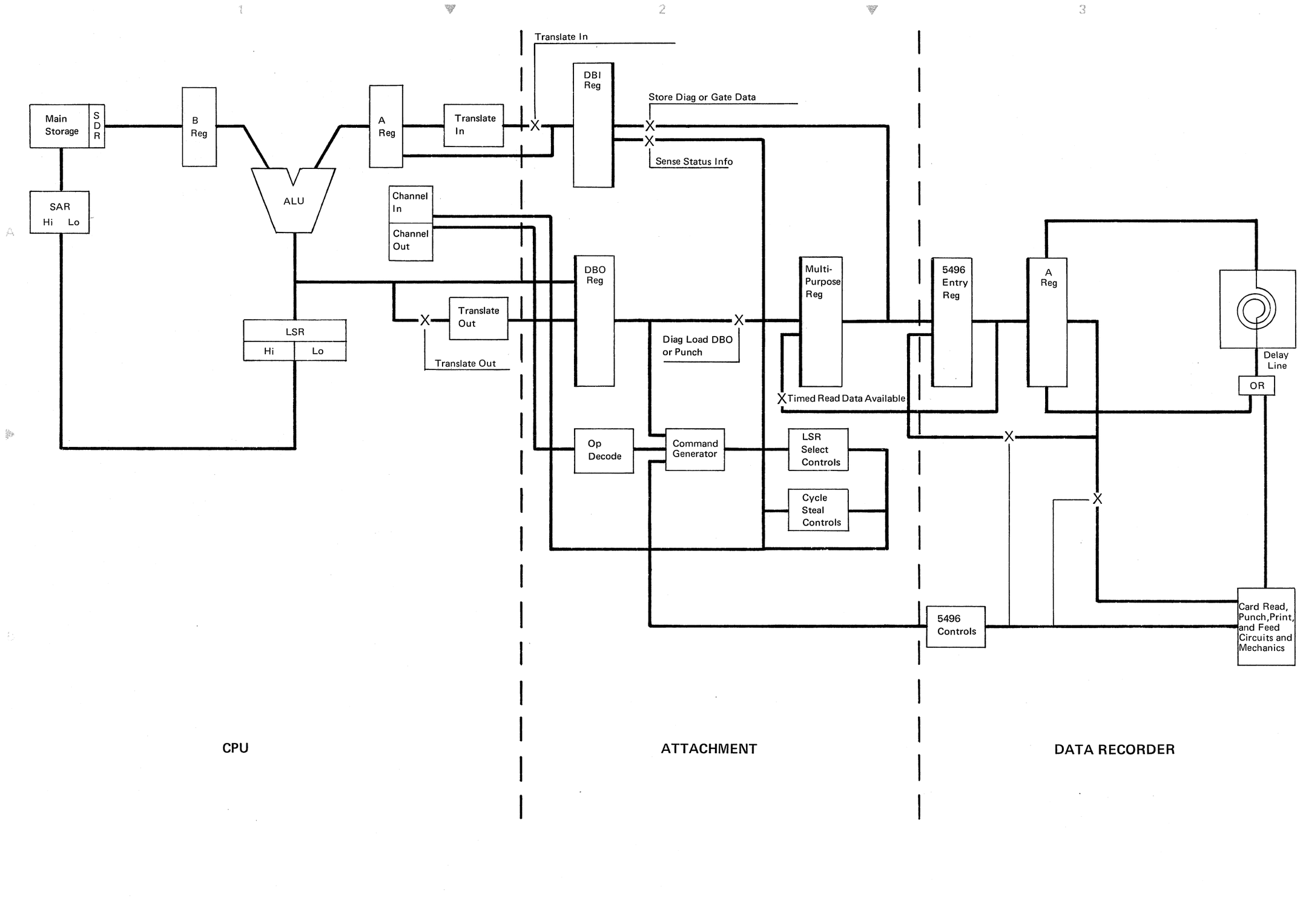
Bit 5 6 7
X 0 0—Diagnostic read (cycle steal)

This command causes the attachment to take one cycle steal and insert a blank (hexadecimal 40) into the core location specified by the current contents of the data recorder local store register. No mechanical motion takes place. As with all other start I/O instructions for the data recorder, the instruction is executed only if the data recorder is ready and not busy.

START I/O (SIO) INSTRUCTION FORMAT



BR0806A


1
2
3
Translate In
DBI Reg
Store Diag or Gate Data
Main Storage
S D R
B Reg
A Reg
Translate In
Sense Status Info
SAR
Hi Lo
ALU
Channel In
Channel Out
DBO Reg
Multi-Purpose Reg
5496 Entry Reg
A Reg
Delay Line
OR
LSR
Hi Lo
Translate Out
Translate Out
Diag Load DBO or Punch
Timed Read Data Available
Op Decode
Command Generator
LSR Select Controls
Cycle Steal Controls
5496 Controls
Card Read, Punch, Print, and Feed Circuits and Mechanics
CPU
ATTACHMENT
DATA RECORDER

Chapter 2. Functional Units

INTRODUCTION TO FUNCTIONAL UNITS

Chapter 2 contains the functional units of the data recorder attachment.

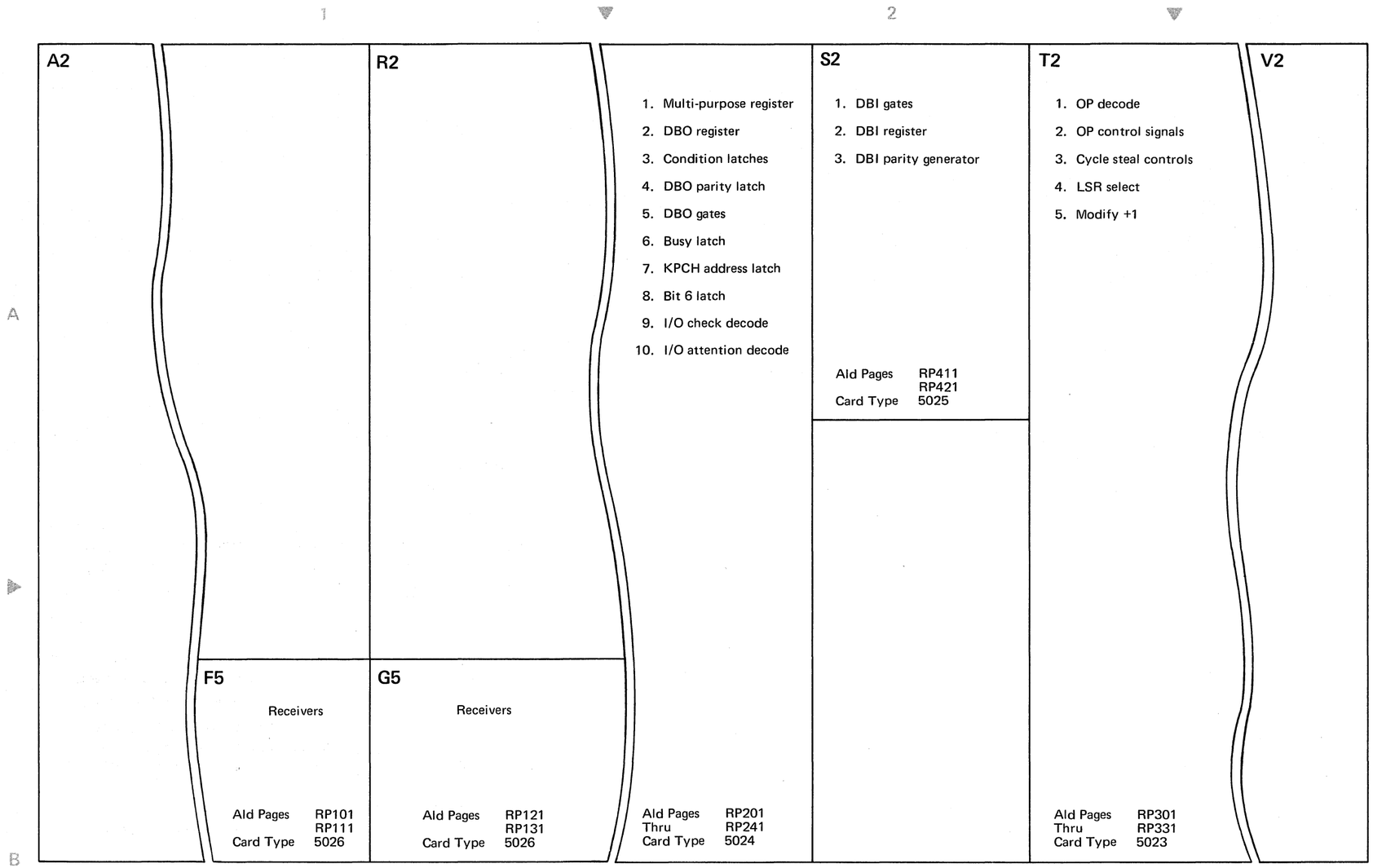
The first page of the chapter is a board layout of the data recorder attachment. It is broken down into cards and contains the following information:

1. Card locations.
2. Circuits found on that card.
3. ALD page reference numbers that describe the circuits found on the card.
4. Card type number. The part number of the card changes each time that card has an engineering change to it. The card type number, however, always stays the same.

The card location number appears on each page, or section of a page, that describes the circuitry on that card. For example, S2 on a page refers to the DBI assembler.

Symbols

Figures within this chapter contain the symbols: 1 numbers in squares, and A letters in circles. These symbols refer to text, marked with an identical symbol, that describes or explains the function of the unit marked in the figure.



5496 Cards

Card Location U2

2 Wide Card

On line read transfer and entry control.

On line punch control.

Card Type 5943

Card Location T2

2 Wide Card

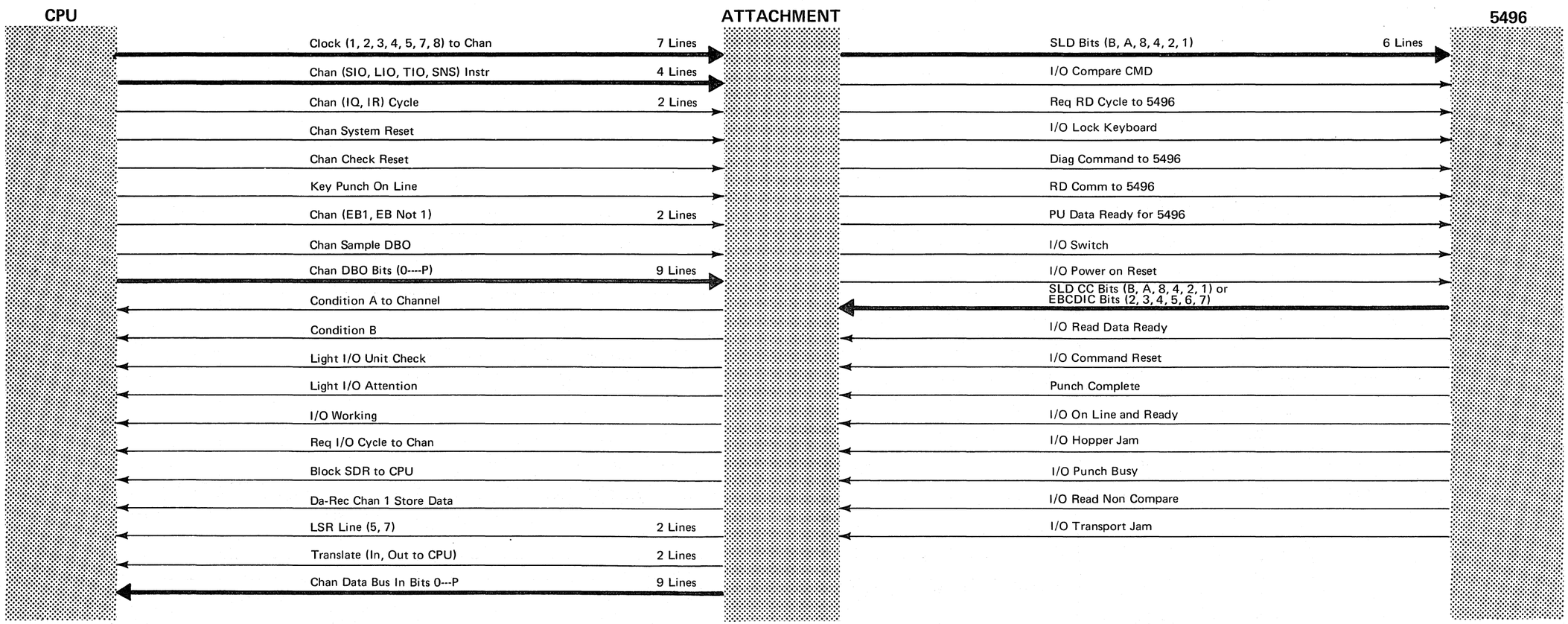
On line control and data entry.

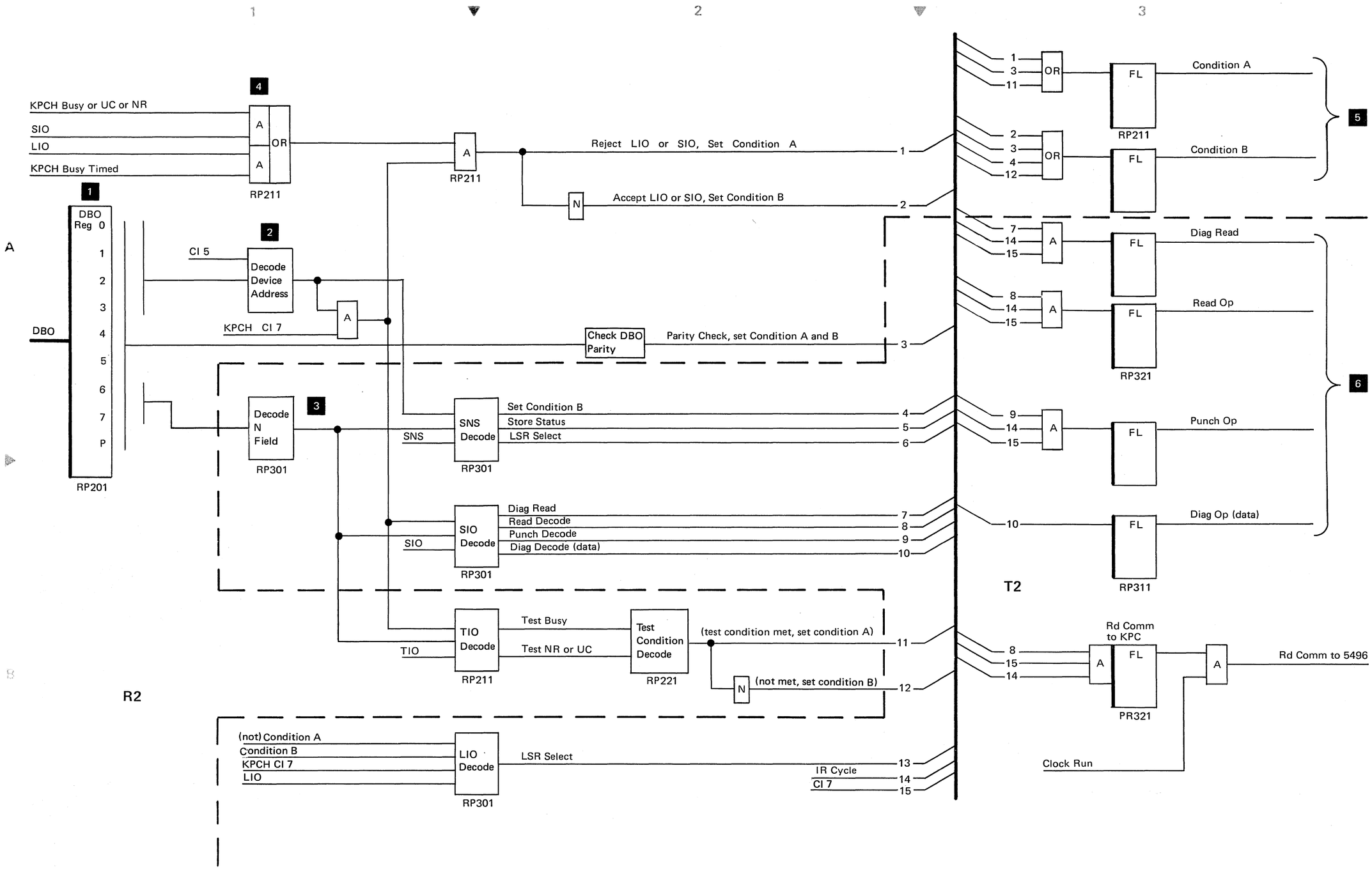
Card Type 5942

Data Recorder Attachment Board B1 on Gate A (A-B1)
(Card side)

*Board B1 also contains:

1. Channel Banks.
2. Keyboard Attachment.
3. CRT Attachment.


CPU
ATTACHMENT
5496
Clock (1, 2, 3, 4, 5, 7, 8) to Chan
7 Lines
Chan (SIO, LIO, TIO, SNS) Instr
4 Lines
Chan (IQ, IR) Cycle
2 Lines
Chan System Reset
Chan Check Reset
Key Punch On Line
Chan (EB1, EB Not 1)
2 Lines
Chan Sample DBO
Chan DBO Bits (0----P)
9 Lines
Condition A to Channel
Condition B
Light I/O Unit Check
Light I/O Attention
I/O Working
Req I/O Cycle to Chan
Block SDR to CPU
Da-Rec Chan 1 Store Data
LSR Line (5, 7)
2 Lines
Translate (In, Out to CPU)
2 Lines
Chan Data Bus In Bits 0---P
9 Lines
SLD Bits (B, A, 8, 4, 2, 1)
6 Lines
I/O Compare CMD
Req RD Cycle to 5496
I/O Lock Keyboard
Diag Command to 5496
RD Comm to 5496
PU Data Ready for 5496
I/O Switch
I/O Power on Reset
SLD CC Bits (B, A, 8, 4, 2, 1) or
EBCDIC Bits (2, 3, 4, 5, 6, 7)
I/O Read Data Ready
I/O Command Reset
Punch Complete
I/O On Line and Ready
I/O Hopper Jam
I/O Punch Busy
I/O Read Non Compare
I/O Transport Jam


1
2
3
4
KPCH Busy or UC or NR
SIO
LIO
KPCH Busy Timed
A
OR
A
RP211
A
RP211
Reject LIO or SIO, Set Condition A
1
N
Accept LIO or SIO, Set Condition B
2
1
DBO Reg 0
1
2
3
4
5
6
7
P
RP201
DBO
2
CI 5
Decode Device Address
A
KPCH CI 7
Check DBO Parity
Parity Check, set Condition A and B
3
3
Decode N Field
RP301
SNS
SNS Decode
RP301
Set Condition B
Store Status
LSR Select
4
5
6
SIO
SIO Decode
RP301
Diag Read
Read Decode
Punch Decode
Diag Decode (data)
7
8
9
10
TIO
TIO Decode
RP211
Test Busy
Test NR or UC
Test Condition Decode
RP221
(test condition met, set condition A)
11
N
(not met, set condition B)
12
(not) Condition A
Condition B
KPCH CI 7
LIO
LIO Decode
RP301
LSR Select
IR Cycle
CI 7
13
14
15
R2
T2
1
3
11
OR
FL
RP211
Condition A
5
2
3
4
12
OR
FL
Condition B
7
14
15
A
FL
RP321
Diag Read
6
8
14
15
A
FL
Read Op
9
14
15
A
FL
Punch Op
10
FL
RP311
Diag Op (data)
Rd Comm to KPC
8
15
14
A
FL
PR321
A
Rd Comm to 5496
Clock Run

INITIAL SELECTION

1 **Data Bus Out (DBO) Register**

a. At clock 5 of the IQ cycle, the IQ byte is set in the DBO register.
b. Parity is checked and if invalid, condition A and B are set, and the inverse of DBO is set in the DBO register.
c. If parity is valid, the data recorder attachment uses the IQ byte to decode the device address and the N field.

2 **Decode Device Address**

a. DBO register bits (0-3) equal to F (hexadecimal 1111), selects the data recorder.
b. Decoding the device address allows the data recorder attachment to decode the I/O instruction.

3 **Decode N Field**

a. DBO register bit 6 sets the bit 6 latch.
b. DBO register bit 7 and the bit 6 latch are used to decode the N field according to the following table:

Instruction	Bit 6 latch	DBO register bit 7	Decode
Load I/O	not used	not used	LSR select
Sense I/O	0	not used	LSR select
	1	not used	Store status
Test I/O or Advance Program Level	0	not used	Test not ready, or I/O check
	1	not used	Test busy
Start I/O	0	0	Diag read (Cycle Steal)
	0	1	Read decode
	1	0	Punch decode
	1	1	Diag decode (data)

BR0807A

4 **Accept or Reject Load I/O or Start I/O**

a. A load I/O is rejected by setting condition A if busy is up, and accepted by setting condition B if not busy.
b. A start I/O is rejected by setting condition A if the attachment is busy, or if the data recorder is not ready, and accepted by setting condition B when these conditions are not present.
c. Start I/O resets unit check (if set) and if the attachment accepts the command, raises I/O condition B.

5 **Condition A and B Latches**

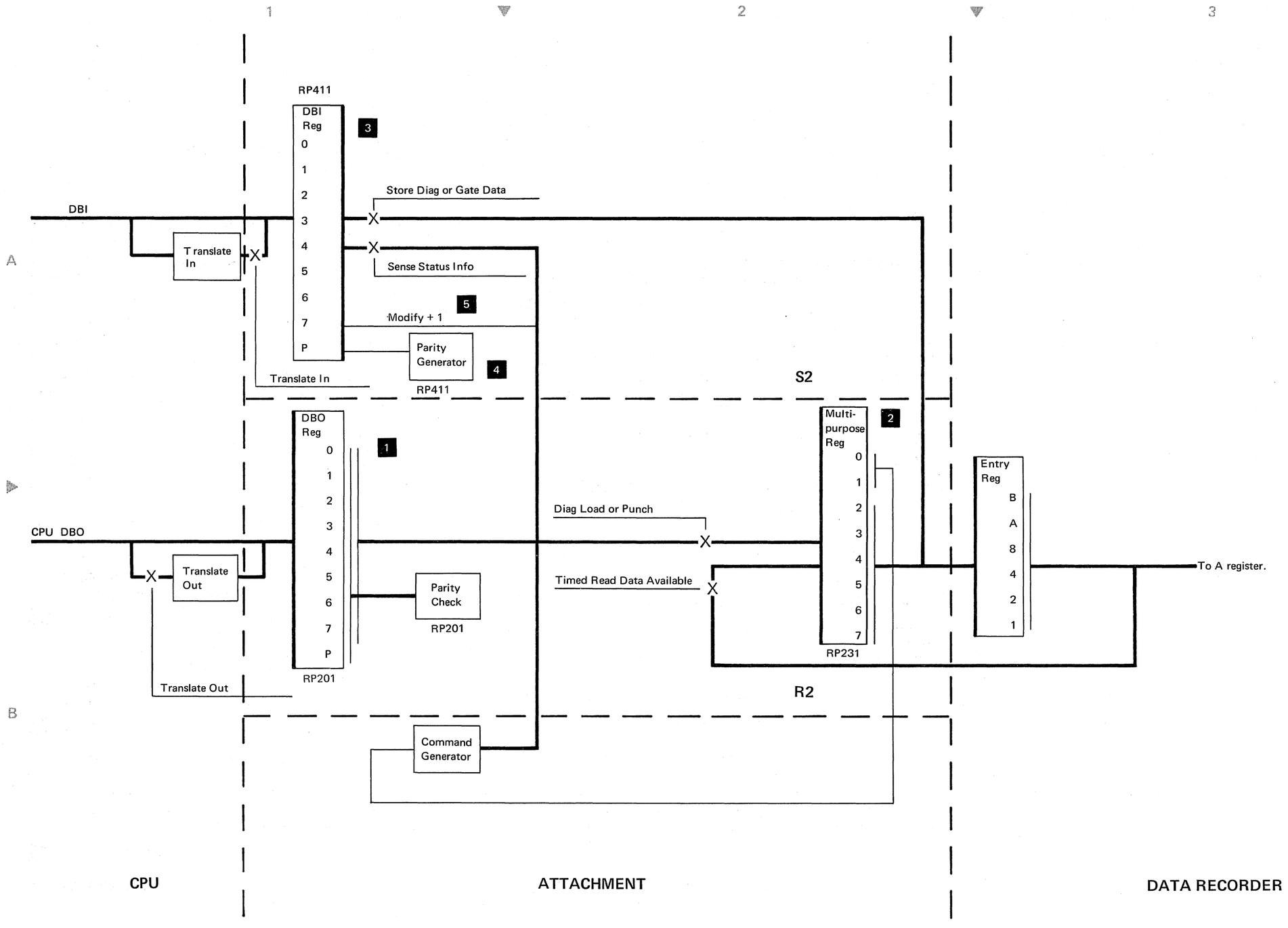
These latches are set according to the following table:

I/O Attachment Condition					I/O Condition A	I/O Condition B
I-Q Cycle of Any I/O Instruction	Incorrect DBO Parity				1	1
	Correct DBO Parity	Q Byte Not Correct			0	0
		Correct Q Byte	Sense Instruction		0	1
			SIO or LIO Instruction	Reject Instruction	1	0
				Accept Instruction	0	1
			TIO or APL Instruction	Condition Not Met	0	1
				Condition Met	1	0
SIO I-R, LIO E-B, and I/O Cycles	Incorrect DBO Parity				1	1
	Correct DBO Parity				0	0

BR0808

6 **During a Start I/O**

a. The 'diag op' (data) latch is set at clock 5 of the IQ cycle, or
b. The 'diag read', 'read op', or 'punch op' latch is set at clock 7 of the IR cycle.


1
2
3
A
B
RP411
DBI Reg
0
1
2
3
4
5
6
7
P
3
DBI
Store Diag or Gate Data
Translate In
Sense Status Info
5
Modify + 1
Parity Generator
4
Translate In
RP411
S2
DBO Reg
0
1
2
3
4
5
6
7
P
1
RP201
Multi-purpose Reg
0
1
2
3
4
5
6
7
2
RP231
Entry Reg
B
A
8
4
2
1
Diag Load or Punch
CPU DBO
Translate Out
Parity Check
RP201
Timed Read Data Available
To A register.
Translate Out
R2
Command Generator
CPU
ATTACHMENT
DATA RECORDER

1 **DBO REGISTER**

a. During each I/O instruction IQ cycle, the IQ byte is available to the DBO register at clock 5.
b. During start I/O IR cycle, the start I/O control code is translated, and made available to the DBO register at clock 5.
c. During a punch cycle, a translated byte of data is available to the DBO register at clock 5.

2 **MULTI-PURPOSE REGISTER**

a. During a diagnostic start I/O (data) IR cycle, or a punch cycle, the multi-purpose register is loaded with the contents of the DBO register at clock 5.
b. During a read operation, the multi-purpose register is loaded with the contents of the 5496 entry register at clock 8 of the CPU cycle, during which a cycle steal is requested.
c. Bits 0, and 1 of the multi-purpose register are used to check for incorrect card code during a punch cycle, or a diagnostic start I/O (data).

3 **DBI ASSEMBLER**

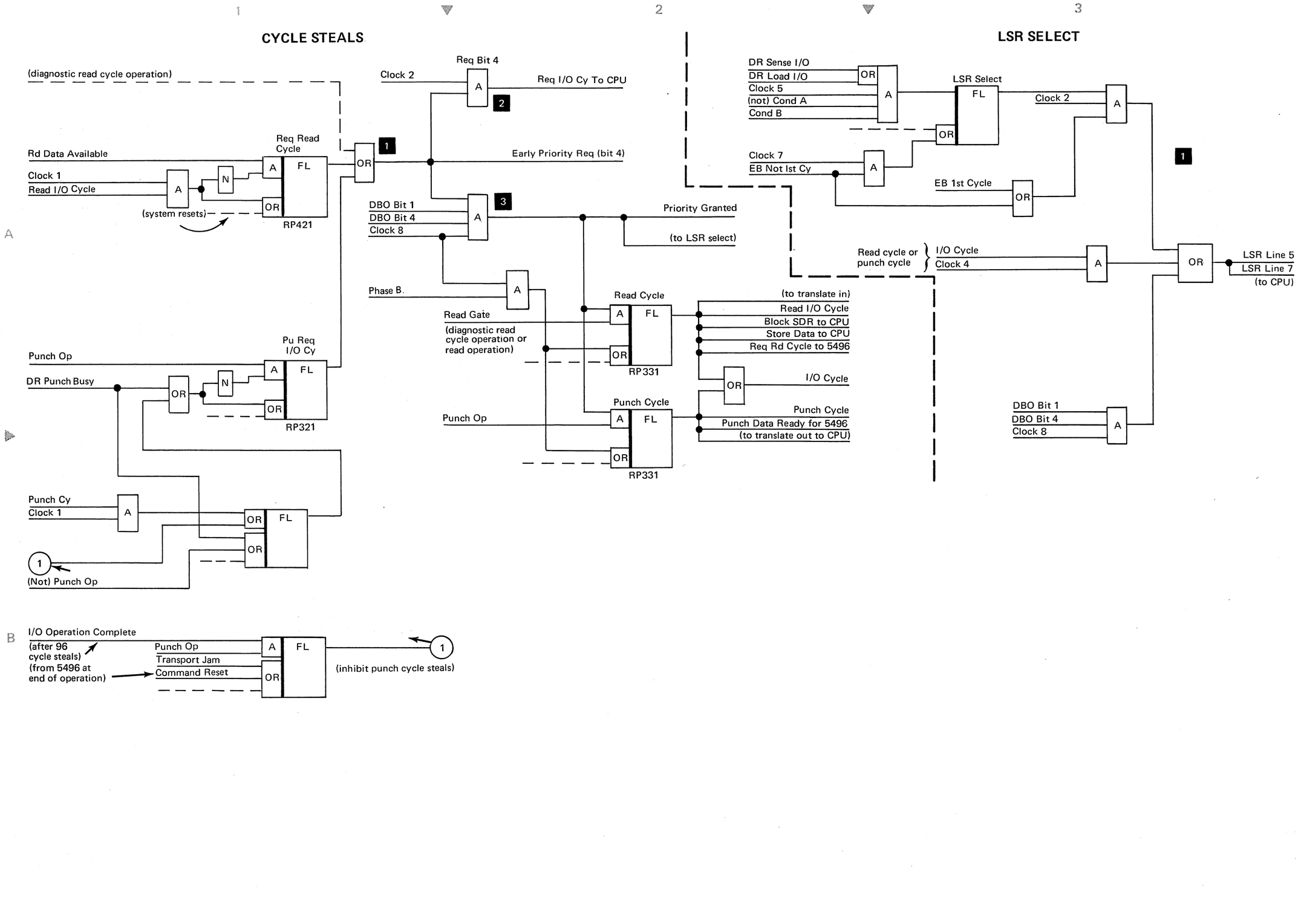
a. During a 'SNS EB 1' cycle, the DBI assembler is loaded with sense status information at clock 2. This status byte is placed in CPU main storage without being translated.
b. During a 'SNS EB Not 1' cycle, the DBI assembler is loaded with the contents of the multi-purpose register at clock 2. This byte of data (diagnostic byte) is translated prior to being placed in CPU main storage.
c. During a read operation the DBI assembler is loaded with the contents of the multi-purpose register at clock 1 of a read I/O cycle. This byte of data is translated prior to placing in CPU main storage.

4 **PARITY GENERATOR**

The parity generator is used during a sense instruction, punch cycle, or read cycle to maintain correct parity in the DBI register.

5 **MODIFY +1**

Modify +1 sets bit 7 of the DBI register at clock 3 of an I/O cycle. The DBI register is then used to modify the data recorder LSR.


CYCLE STEALS
LSR SELECT
(diagnostic read cycle operation)
Clock 2
Req Bit 4
Req I/O Cy To CPU
Rd Data Available
Clock 1
Read I/O Cycle
Req Read Cycle
(system resets)
RP421
Early Priority Req (bit 4)
DBO Bit 1
DBO Bit 4
Clock 8
Priority Granted
(to LSR select)
Phase B
Read Gate
(diagnostic read cycle operation or read operation)
Read Cycle
RP331
(to translate in)
Read I/O Cycle
Block SDR to CPU
Store Data to CPU
Req Rd Cycle to 5496
I/O Cycle
Punch Op
DR Punch Busy
Pu Req I/O Cy
RP321
Punch Cycle
Punch Data Ready for 5496
(to translate out to CPU)
Punch Cy
Clock 1
(Not) Punch Op
I/O Operation Complete
(after 96 cycle steals)
(from 5496 at end of operation)
Punch Op
Transport Jam
Command Reset
(inhibit punch cycle steals)
DR Sense I/O
DR Load I/O
Clock 5
(not) Cond A
Cond B
LSR Select
Clock 7
EB Not Ist Cy
EB 1st Cycle
Read cycle or punch cycle
I/O Cycle
Clock 4
LSR Line 5
LSR Line 7
(to CPU)

CYCLE STEALS

1. The data recorder attachment requests cycle steals during the following operations:

   a. Diagnostic read
   b. Read
   c. Punch

2. To request a cycle steal, the request bit 4 AND is activated which generates 'req IO cycle' to CPU. This line is activated at clock 2 of each machine cycle until the request is granted.

3. The CPU grants a cycle steal to the data recorder attachment by setting DBO bits 1 and 4.

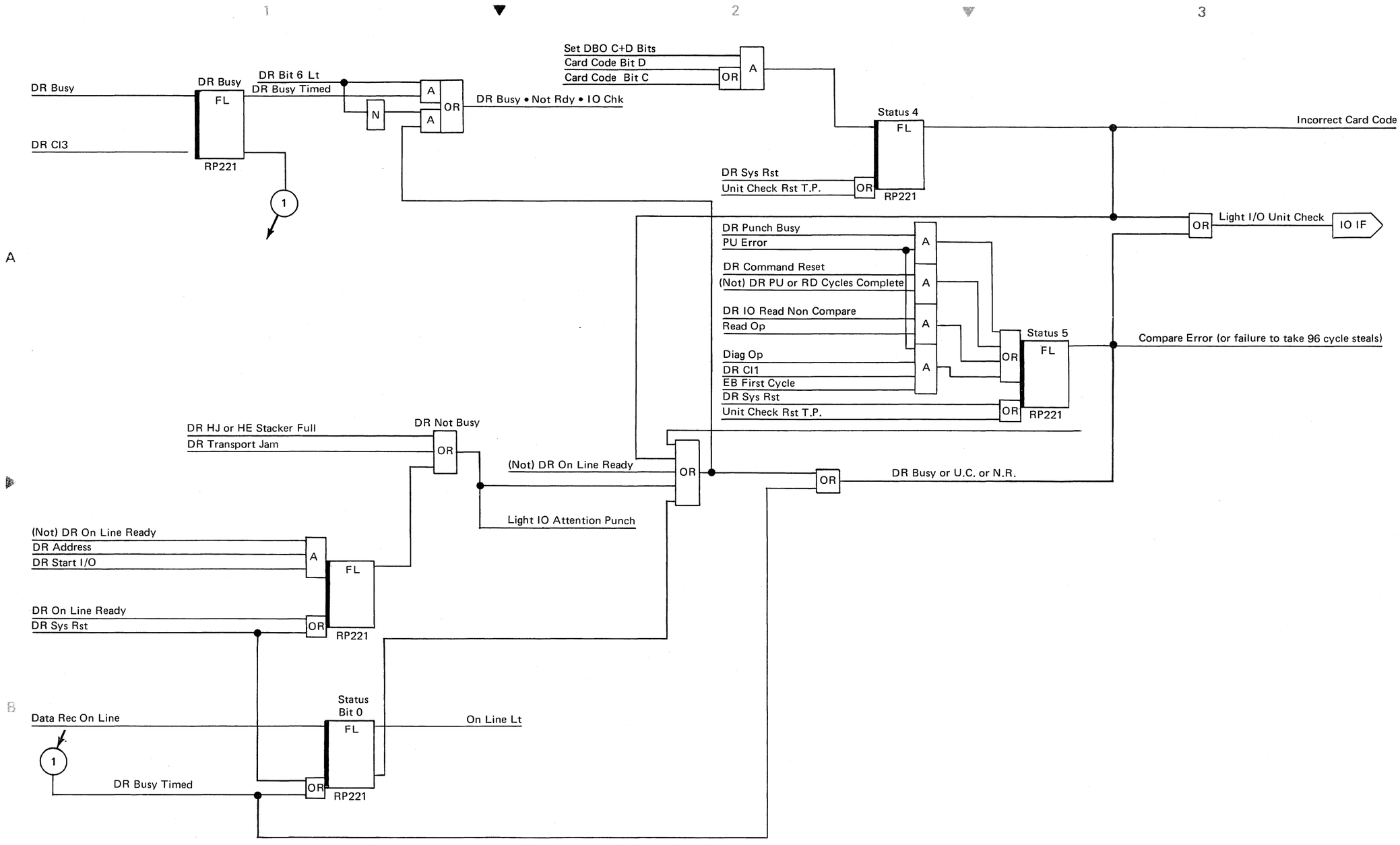
LSR SELECT

1. The data recorder LSR (DRAR) is selected during the following:

   a. Load I/O, clock 2 of EB cycles
   b. Sense LSR, clock 2 of EB cycles
   c. I/O cycle clock 4
   d. Cycle steal priority granted, clock 8

   To select the DRAR, activate LSR select lines 5 and 7.

DATA RECORDER ATTACHMENT–Functional Units
Cycle Steal and LSR Select Controls (Part 2 of 2)


1
2
3
A
B
DR Busy
DR Busy
FL
RP221
DR CI3
DR Bit 6 Lt
DR Busy Timed
N
A
A
OR
DR Busy • Not Rdy • IO Chk
1
Set DBO C+D Bits
Card Code Bit D
Card Code Bit C
OR
A
Status 4
FL
RP221
DR Sys Rst
Unit Check Rst T.P.
OR
Incorrect Card Code
OR
Light I/O Unit Check
IO IF
DR Punch Busy
PU Error
DR Command Reset
(Not) DR PU or RD Cycles Complete
DR IO Read Non Compare
Read Op
Diag Op
DR CI1
EB First Cycle
DR Sys Rst
Unit Check Rst T.P.
A
A
A
A
OR
OR
Status 5
FL
RP221
Compare Error (or failure to take 96 cycle steals)
DR HJ or HE Stacker Full
DR Transport Jam
OR
DR Not Busy
(Not) DR On Line Ready
OR
OR
DR Busy or U.C. or N.R.
Light IO Attention Punch
(Not) DR On Line Ready
DR Address
DR Start I/O
A
FL
DR On Line Ready
DR Sys Rst
OR
RP221
Status
Bit 0
FL
RP221
Data Rec On Line
On Line Lt
1
DR Busy Timed
OR

Chapter 3. Operations

INTRODUCTION TO OPERATIONS

Chapter 3 contains the detailed flowcharts and timing charts of the operations performed by the data recorder attachment.

Flowcharts

The flowcharts contain three levels of information. By reading down the heavy dark lines, the reader can learn the major objectives of the operation. The second level of information is obtained by reading the information in the boxes that branch off the heavy dark line. The information that is contained in each block in a heavy dark line is explained in the blocks that branch off from it.

The third level of information is contained in the note blocks (open ended blocks) that branch off the second level blocks. Information in these blocks is intended to explain why an action has been performed.

Timing Charts

The timing charts in this chapter are to be used to supplement the information found in the flowcharts.

1 2 3

LOAD I/O INSTRUCTION

I-Op Cycle. The load I/O instruction tag is available to the data recorder attachment, but no action takes place until the IQ cycle.

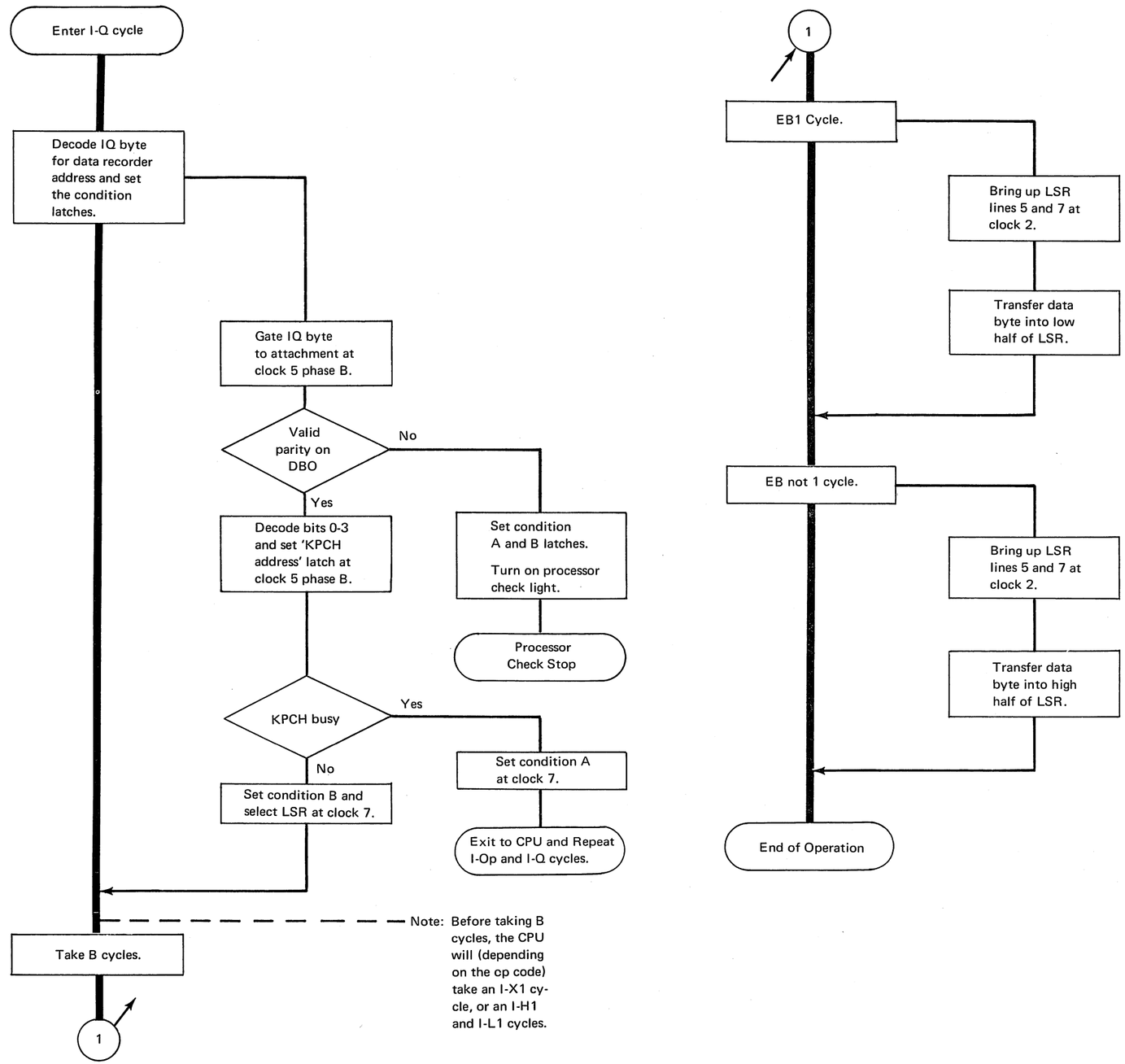
IQ Cycle. The data recorder attachment checks DBO parity, decodes the instruction address, and sets the condition latches.

EB1 Cycle. The DRAR is selected and the first data byte is transferred into LSR Lo.

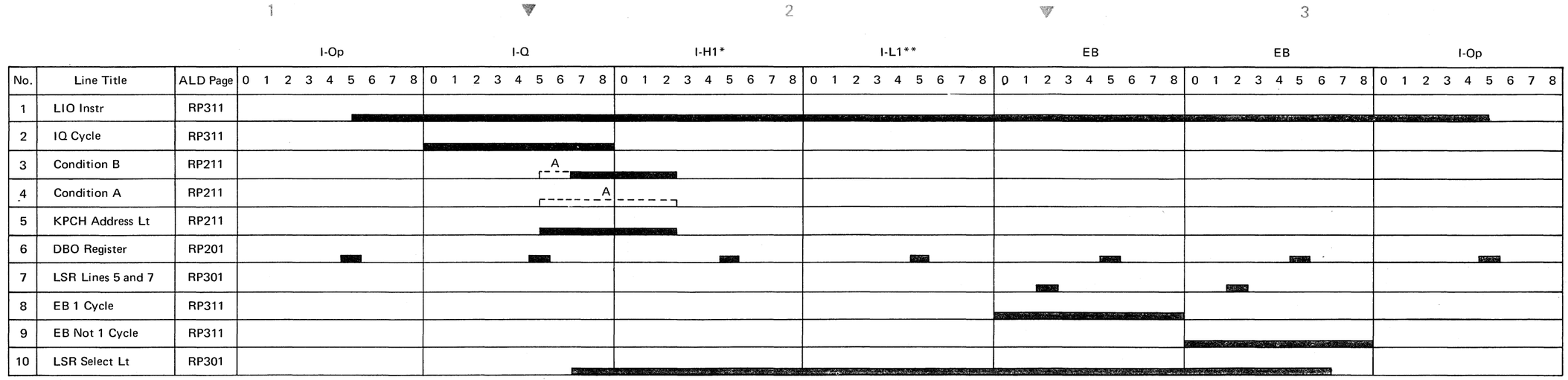
EB Not 1 Cycle. The DRAR is selected and the second data byte is transferred into LSR Hi.

A

B



1 2 3



No.	Line Title	ALD Page	I-Op 0 1 2 3 4 5 6 7 8	I-Q 0 1 2 3 4 5 6 7 8	I-H1* 0 1 2 3 4 5 6 7 8	I-L1** 0 1 2 3 4 5 6 7 8	EB 0 1 2 3 4 5 6 7 8	EB 0 1 2 3 4 5 6 7 8	I-Op 0 1 2 3 4 5 6 7 8
1	LIO Instr	RP311							
2	IQ Cycle	RP311							
3	Condition B	RP211		A					
4	Condition A	RP211		A					
5	KPCH Address Lt	RP211							
6	DBO Register	RP201							
7	LSR Lines 5 and 7	RP301							
8	EB 1 Cycle	RP311							
9	EB Not 1 Cycle	RP311							
10	LSR Select Lt	RP301							

* For index format I-H1 is I-X1.
** For index format I-L1 does not exist.
A - Signal up if DBO parity in error.

1 2 3

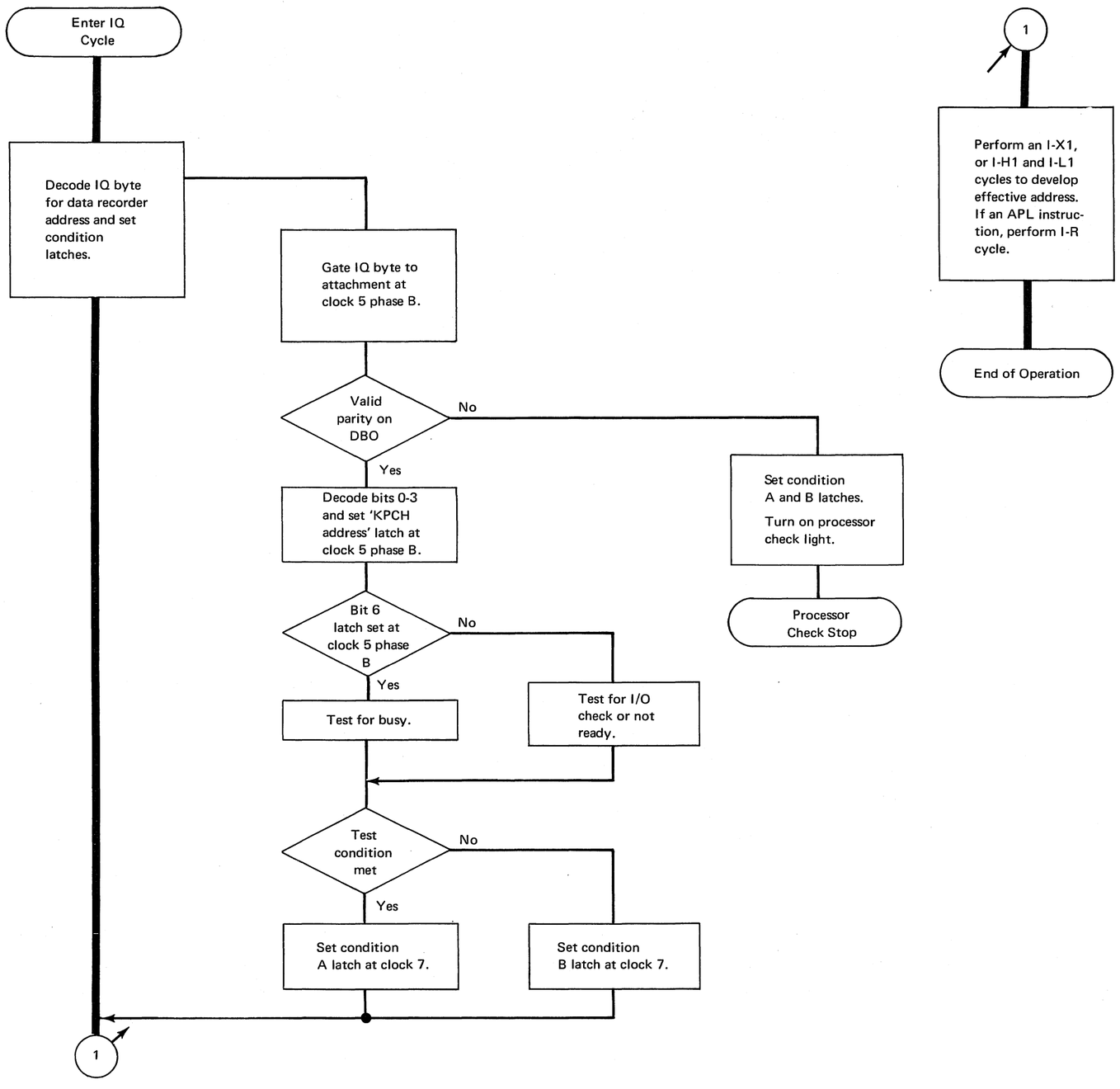
TEST I/O OR APL INSTRUCTIONS

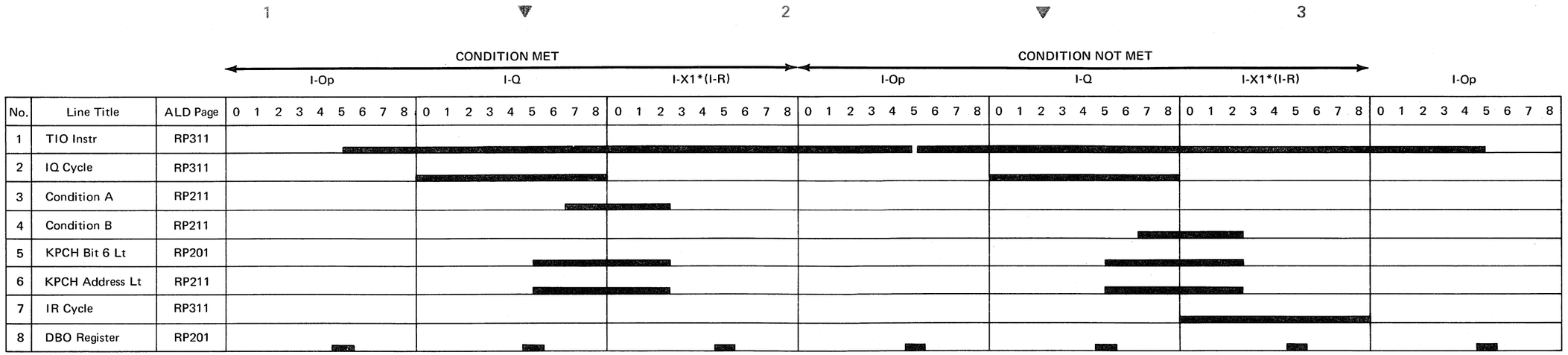
I-Op Cycle. The test I/O instruction tag is available to the data recorder attachment, but no action takes place until the IQ cycle.

IQ Cycle. The data recorder attachment checks DBO parity, decodes the instruction address, and sets the condition latches. Setting condition A causes a program branch. Setting condition B causes the CPU to proceed to the next sequential instruction.

A

B





* For direct address format I-X1 is I-H1 followed by I-L1
IR cycle follows IQ during an APL.

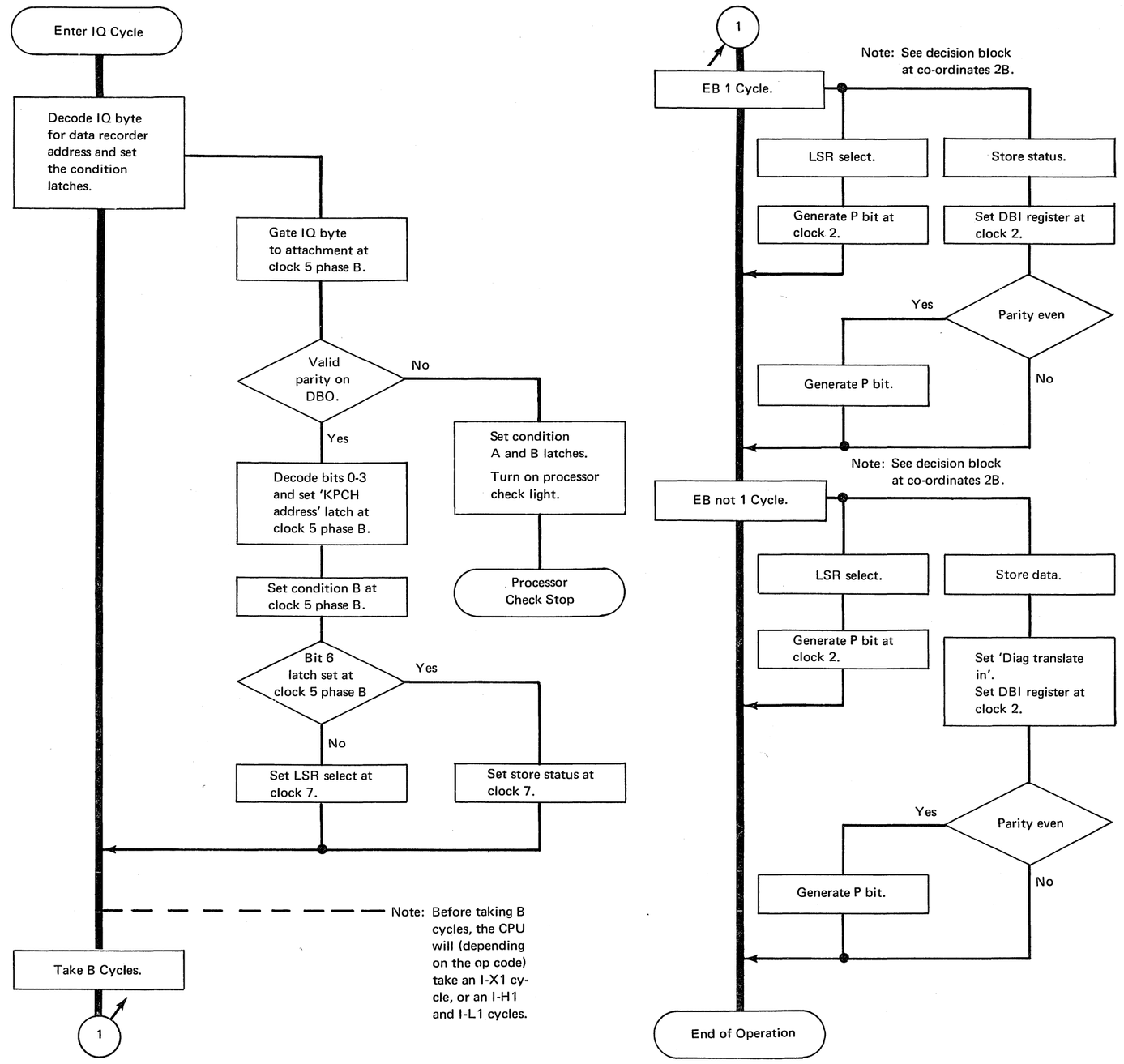
SENSE INSTRUCTION

I-Op Cycle. The sense instruction tag is available to the data recorder attachment, but no action takes place until the IQ cycle.

IQ Cycle. The data recorder attachment checks DBO parity, decodes the instruction address, and sets the condition latches.

EB1 Cycle. Either the first data byte, or the DRAR LSR Lo, is stored in the CPU main storage address specified.

EB Not 1. Either the second data byte, or the DRAR LSR Hi, is stored in the CPU main storage address specified minus one.



1 2 3

No.	Line Title	ALD Page	I-Op 0 1 2 3 4 5 6 7 8	I-Q 0 1 2 3 4 5 6 7 8	I-H1* 0 1 2 3 4 5 6 7 8	I-L1** 0 1 2 3 4 5 6 7 8	EB 0 1 2 3 4 5 6 7 8	EB 0 1 2 3 4 5 6 7 8	I-Op 0 1 2 3 4 5 6 7 8
1	SNS Instruction	RP311							
2	IQ Cycle	RP311							
3	Condition B	RP211							
4	Condition A	RP211		A					
5	KPCH Address Lt	RP211							
6	KPCH Bit 6 Lt	RP201		B					
7	Store Status Lt	RP301							
8	LSR Select Lt	RP301							
9	EB 1 Cycle	RP311							
10	EB Not 1 Cycle	RP311							
11	Generate P Bit	RP301							
12	Diag Translate In	RP301							
13	DBI Register	RP421							
14	LSR Lines 5 and 7	RP301							
15	DBO Register	RP201							

* For index format I-H1 is I-L1.
** For index format I-L1 does not exist.
A- Signal up if DBO parity in error.
B- Signal up for store status.

READ OPERATION

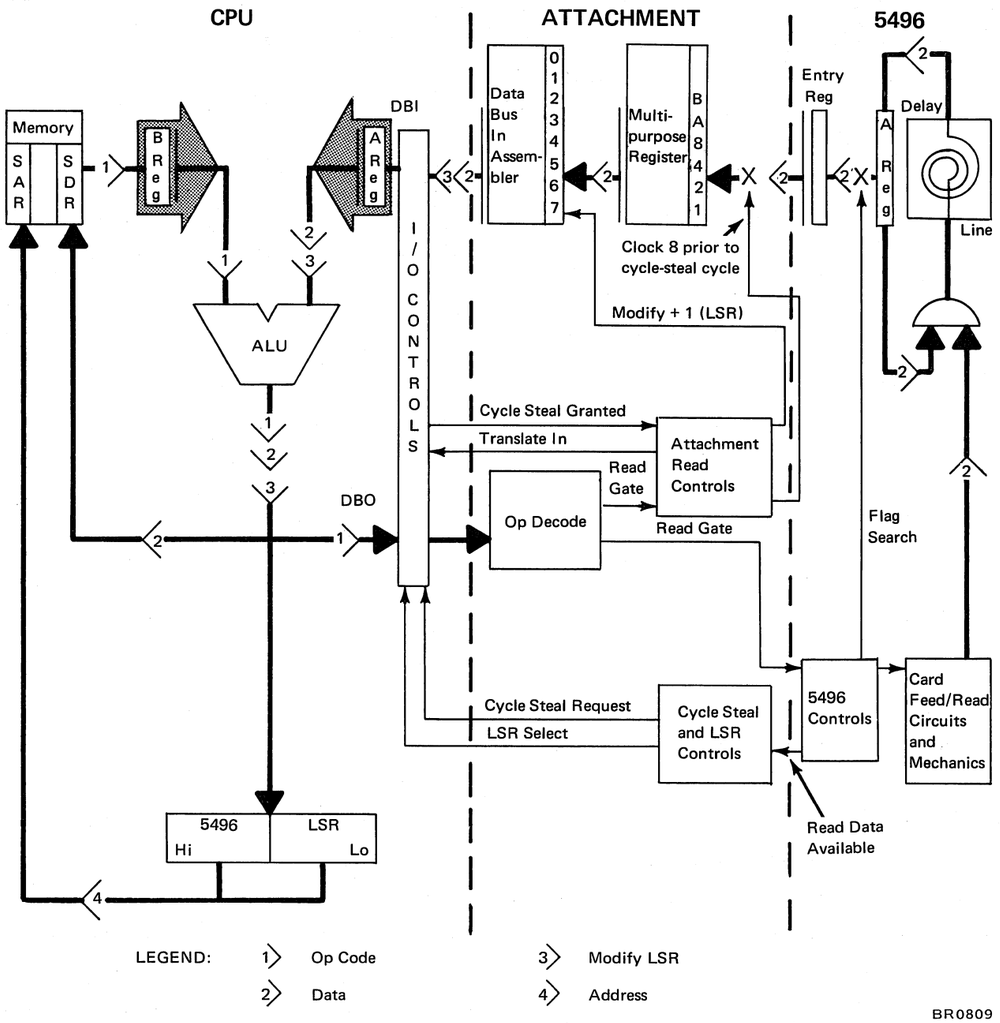
A read operation is started on the 5496 if bits 6 and 7 equal 0 and 1 respectively in the Q byte. During the CPU I-R cycle, the 'read op' latch is set for the operation and a read command is issued to the 5496. The read command causes the 5496 to read a punched card onto the delay line. This read operation, which is under control of the 5496 circuits once it has been initiated by the attachment, is identical to an operator pressing the read key on the 5496 in an offline operation.

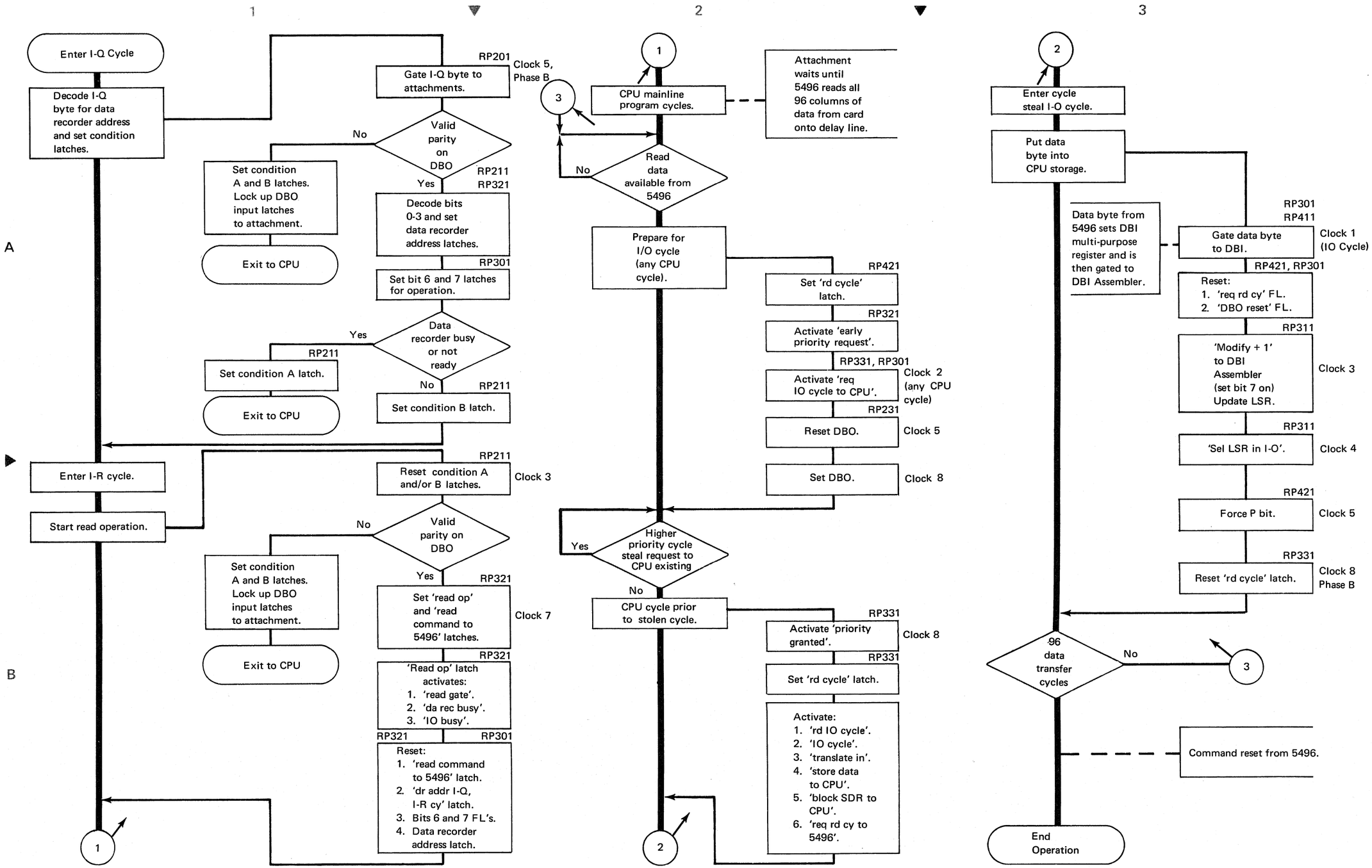
The 5496 read cycle feeds a card from the hopper, reads the data from the card (placing the data in the proper word on the delay line), and stacks the card in the stacker. After the entire card has been read onto the delay line, the 5496 signals the attachment that the first column of data is ready to be sent to CPU storage.

To transfer the data from the delay line to the CPU storage, the data recorder attachment steals a machine cycle from the CPU and signals the 5496 to make the next column of data available for transfer to the CPU. When the data is available, another cycle is stolen to transfer the data to storage. This sequence of data-available/stolen cycle continues until 96 data bytes (an entire card) have been transferred.

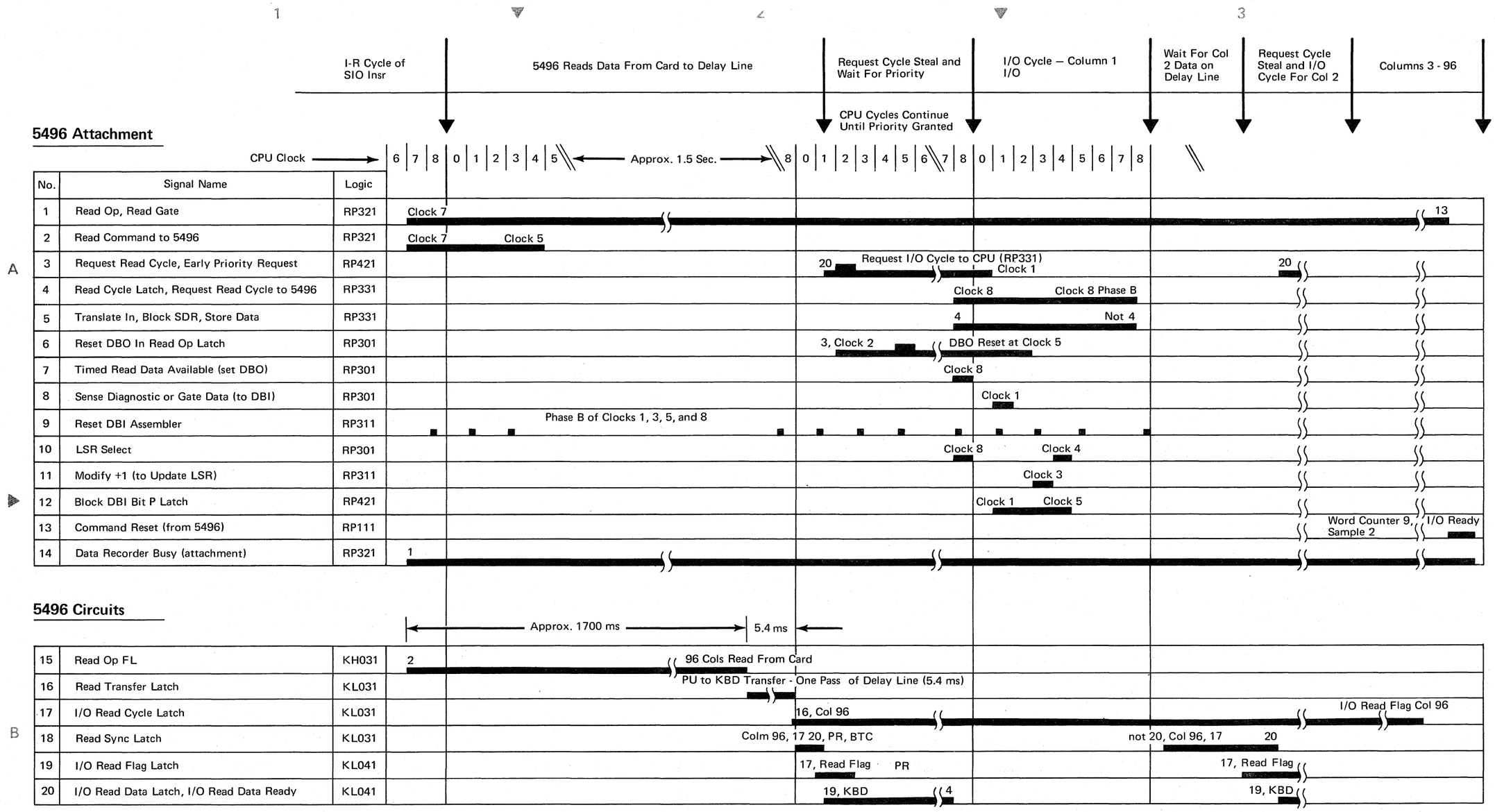
At the end of the data transfer, the 'read op' latch is reset and the operation ends. Error conditions other than parity checks must be detected by a sense instruction.

The flowchart of the operation gives a more detailed description of the read operation for the data recorder attachment.





DATA RECORDER ATTACHMENT–Operations
Read Operation Flowchart (Part 2 of 2)


1
2
3
I-R Cycle of SIO Insr
5496 Reads Data From Card to Delay Line
Request Cycle Steal and Wait For Priority
I/O Cycle – Column 1 I/O
Wait For Col 2 Data on Delay Line
Request Cycle Steal and I/O Cycle For Col 2
Columns 3 - 96
CPU Cycles Continue Until Priority Granted
CPU Clock
6 7 8 0 1 2 3 4 5
Approx. 1.5 Sec.
8 0 1 2 3 4 5 6 7 8 0 1 2 3 4 5 6 7 8
5496 Attachment
No.
Signal Name
Logic
1 Read Op, Read Gate RP321
Clock 7
13
2 Read Command to 5496 RP321
Clock 7
Clock 5
3 Request Read Cycle, Early Priority Request RP421
20
Request I/O Cycle to CPU (RP331)
Clock 1
20
4 Read Cycle Latch, Request Read Cycle to 5496 RP331
Clock 8
Clock 8 Phase B
5 Translate In, Block SDR, Store Data RP331
4
Not 4
6 Reset DBO In Read Op Latch RP301
3, Clock 2
DBO Reset at Clock 5
7 Timed Read Data Available (set DBO) RP301
Clock 8
8 Sense Diagnostic or Gate Data (to DBI) RP301
Clock 1
9 Reset DBI Assembler RP311
Phase B of Clocks 1, 3, 5, and 8
10 LSR Select RP301
Clock 8
Clock 4
11 Modify +1 (to Update LSR) RP311
Clock 3
12 Block DBI Bit P Latch RP421
Clock 1
Clock 5
13 Command Reset (from 5496) RP111
Word Counter 9, Sample 2
I/O Ready
14 Data Recorder Busy (attachment) RP321
1
5496 Circuits
Approx. 1700 ms
5.4 ms
15 Read Op FL KH031
2
96 Cols Read From Card
16 Read Transfer Latch KL031
PU to KBD Transfer - One Pass of Delay Line (5.4 ms)
17 I/O Read Cycle Latch KL031
16, Col 96
I/O Read Flag Col 96
18 Read Sync Latch KL031
Colm 96, 17 20, PR, BTC
not 20, Col 96, 17
20
19 I/O Read Flag Latch KL041
17, Read Flag
PR
17, Read Flag
20 I/O Read Data Latch, I/O Read Data Ready KL041
19, KBD
4
19, KBD

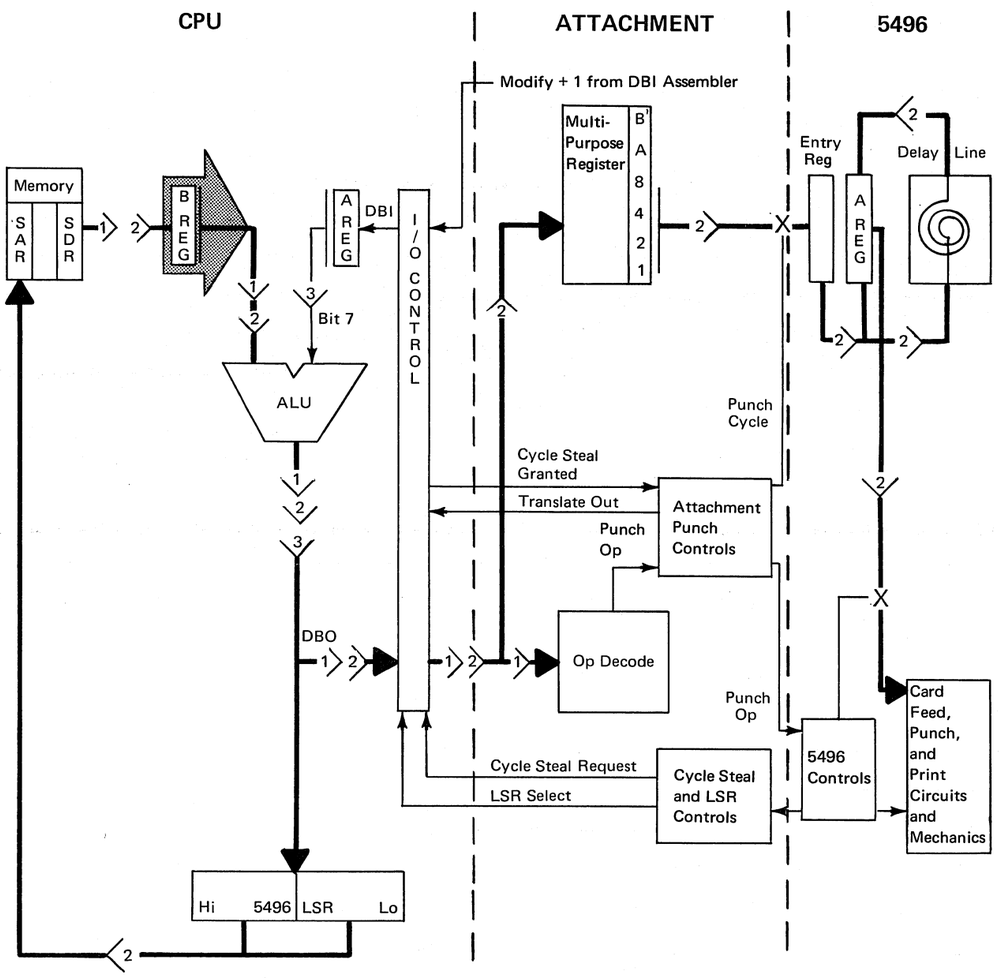
PUNCH OPERATION

A punch operation is started on the 5496 if bits 6 and 7 equal 1 and 0 respectively in the Q byte. During the CPU I-R cycle, the 'punch op' latch is set for the operation and a cycle steal is requested from the CPU. When the cycle steal is granted by the CPU, the attachment transfers the first data byte from storage to the delay line in the 5496 (during the stolen cycle). The data recorder attachment continues transferring data bytes to the delay line with cycle steal operations until 96 bytes have been transferred. The transfer of data bytes 2 through 96 are requested by the 5496. The 'da rec punch busy' line is active during the time the 5496 is placing the data byte on the delay line. After the byte is placed in the proper delay line word, the 5496 drops the busy line to request another data byte from the CPU.

After 96 data bytes are transferred, the 5496 feeds a card from the hopper, punches the data into the card, prints the graphic characters represented by the data if desired, and stacks the card in the stacker. This operation of card feeding, punching, printing, and stacking is under complete control of the 5496 circuits once the 96 data bytes have been transferred from storage to the 5496 delay line. The data recorder circuits also signal the attachment that the operation is complete when the card is stacked in the 5496. This operation complete signal (command reset) resets the 'punch op' latch and the operation ends.

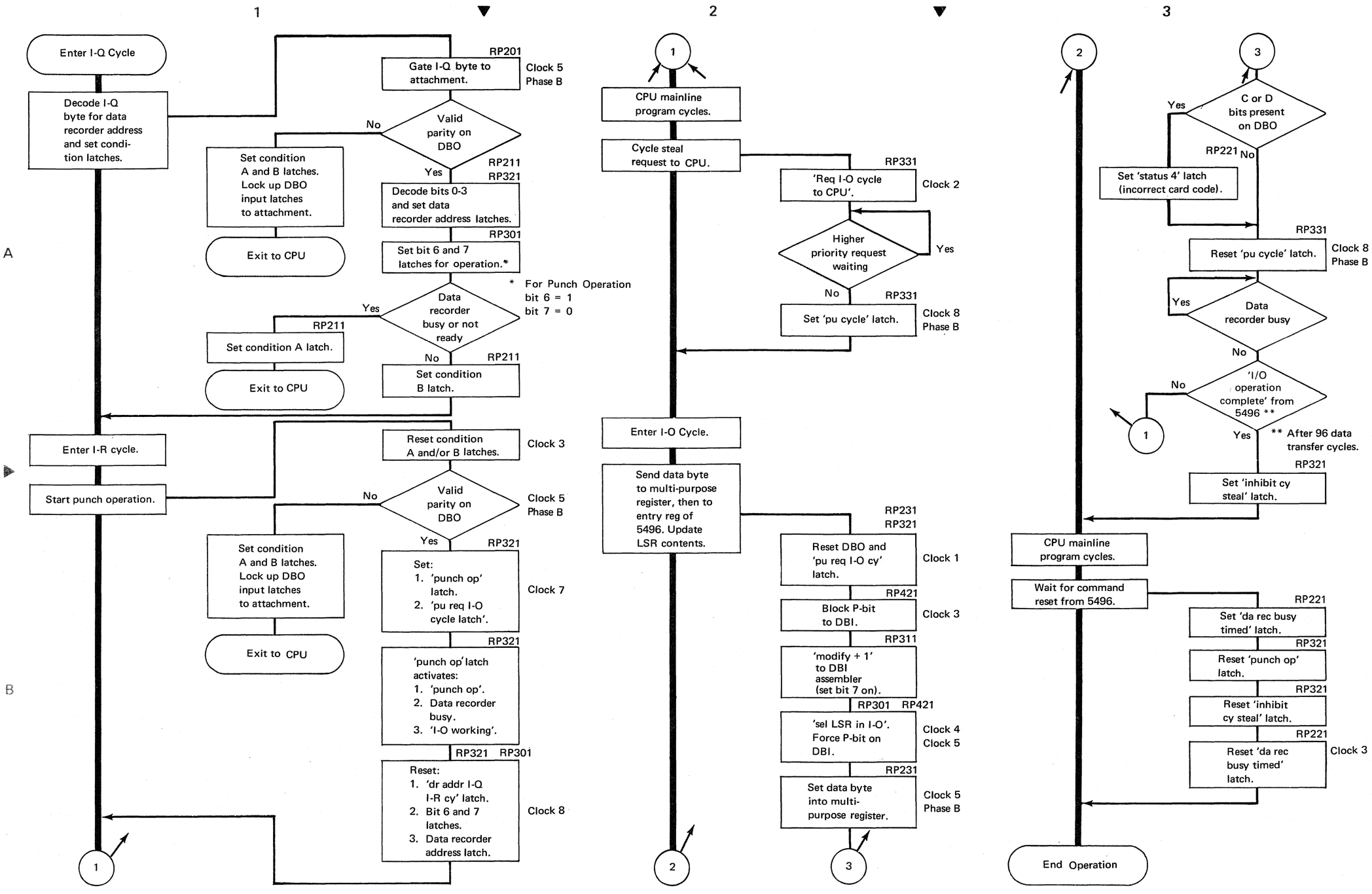
Error conditions other than parity checks must be detected by a sense instruction. If at any time the EBCDIC data from CPU storage is translated into a card code containing C or D bits (an invalid card code), the error is indicated by setting the 'status 4' latch and by lighting the I/O unit check light on the FE console in the CPU. The 5496 punches the translated bit code into the card (without the C and D bits) and prints the closest graphic that the 5496 can decipher from that bit configuration.

The flowchart of the operation gives a more detailed description of the punch operation for the data recorder attachment.

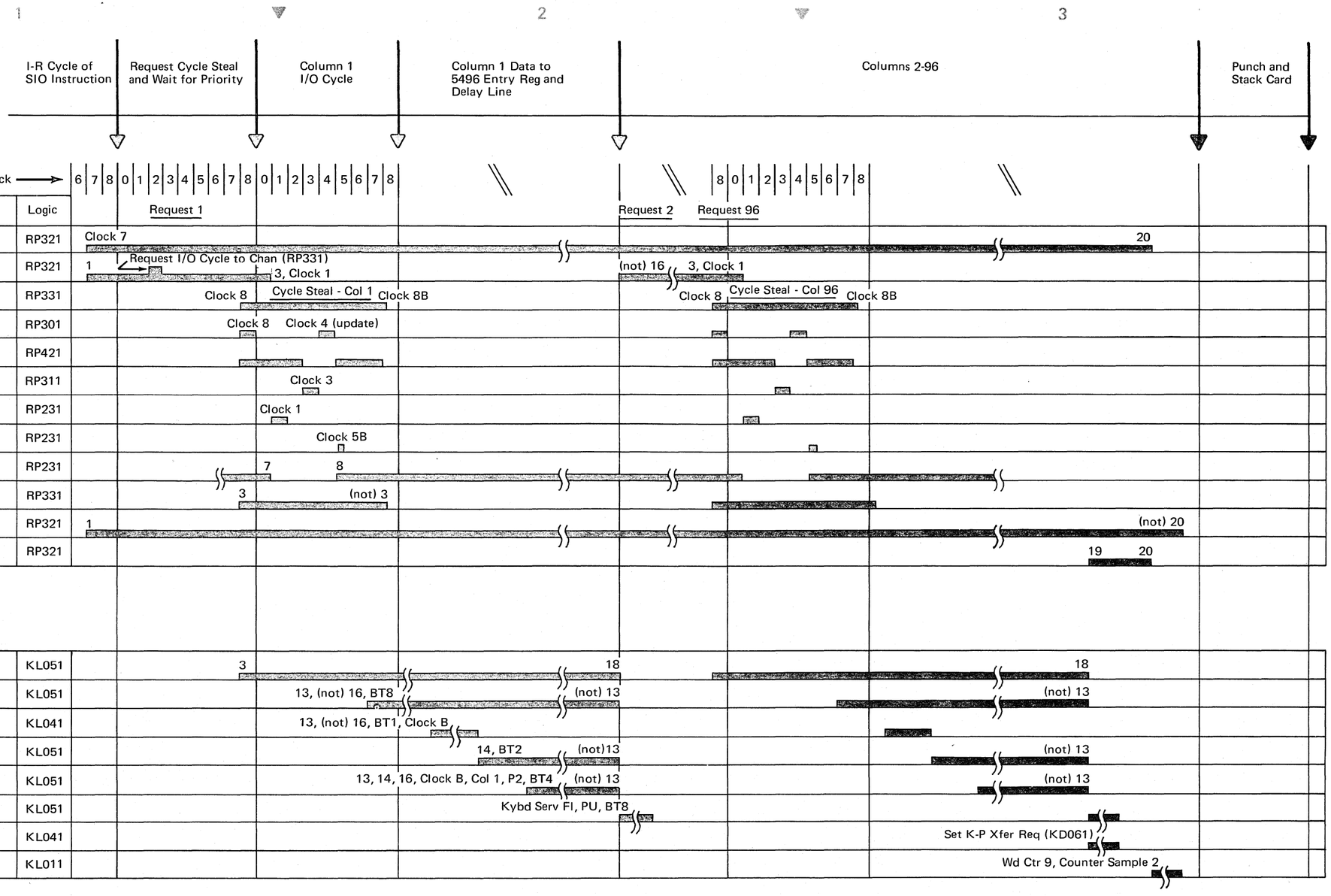


Legend: 1 Op Code, 2 Data, 3 Modify LSR, 4 Address

BR0810



DATA RECORDER ATTACHMENT–Operations
Punch Operation Flowchart (Part 2 of 2)



5496 Attachment

No.	Signal Name	Logic
1	Punch Op Latch	RP321
2	Punch Req I/O Cycle Latch	RP321
3	Punch Cycle Latch (cycle steal)	RP331
4	LSR Line 5 and 7 (select LSR)	RP301
5	Force P Bit on DBI	RP421
6	Modify +1	RP311
7	(multipurpose register reset)	RP231
8	(multipurpose register set)	RP231
9	(data in multipurpose register)	RP231
10	Translate Out to CPU	RP331
11	I/O Working	RP321
12	(inhibit punch cycle steal) FL	RP321

5496 Circuits

No.	Signal Name	Logic
13	I/O Enter Data Latch	KL051
14	I/O Sample Latch	KL051
15	Load I/O Data (entry reg set)	KL041
16	I/O Busy Latch	KL051
17	I/O Any Key Latch	KL051
18	(reset for I/O enter data latch)	KL051
19	I/O Operation Complete	KL041
20	I/O Command Reset	KL011

DIAGNOSTIC DATA OPERATION

A diagnostic data operation is started in the data recorder attachment if bits 6 and 7 equal 11 in the Q byte. During the I-R cycle of the CPU instruction, the data byte is sent to the 5496 attachment multi-purpose register. The data byte is then sent to the entry register of the 5496, which returns the data to the multi-purpose register for checking. At the end of the I-R cycle, the data byte remains latched-up on the data bus lines so that the field engineer can check voltage levels when searching for the cause of a trouble. The data bus circuits in the attachment can also be checked through programming by issuing a sense instruction following a start I/O diagnostic data instruction. The sense instruction provides the following information.

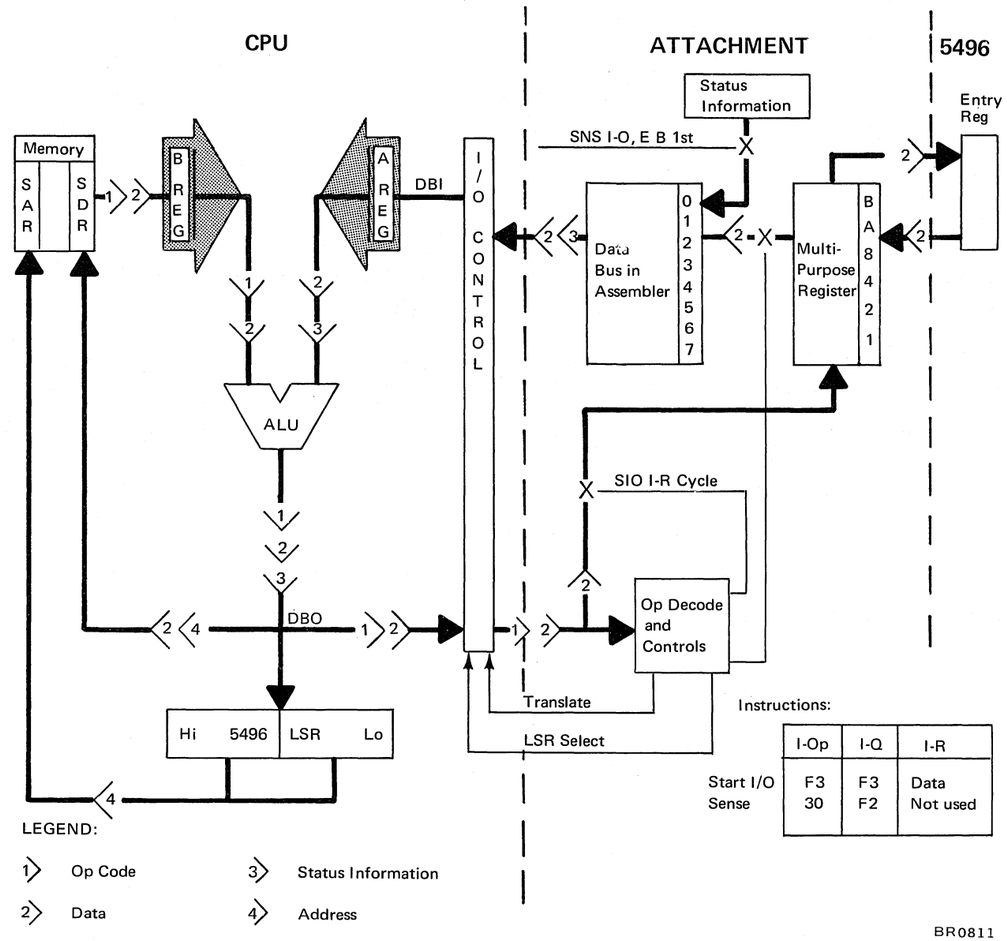
First Byte–Bit 5: This bit is on if the byte sent to the 5496 did not match the byte returned by the 5496. Otherwise this bit is off. The bit being on would indicate a problem either in the 5496 or the interface between the 5496 and the attachment.

Second Byte: This byte contains the data given to the attachment on the previous diagnostic start I/O. (In case of a compare error, this is not the same as the byte returned by the 5496.) If this byte does not agree with the byte sent on the diagnostic start I/O, it would indicate a problem in either the attachment or the CPU translator(s).

The block diagram shows the data flow for the start I/O diagnostic data operation.

- A start I/O loads data byte onto data lines at 'I-R cycle', 'clock 5', 'phase B'. Data is static up to, but not including, data bus in assembler.
- A sense instruction puts a data byte in the core location following the status byte.
- Translate signal:

  Active during 'I-R cycle' for data byte.
  Forced for 'SNS EB not 1st' byte.



DIAGNOSTIC CYCLE STEAL OPERATION

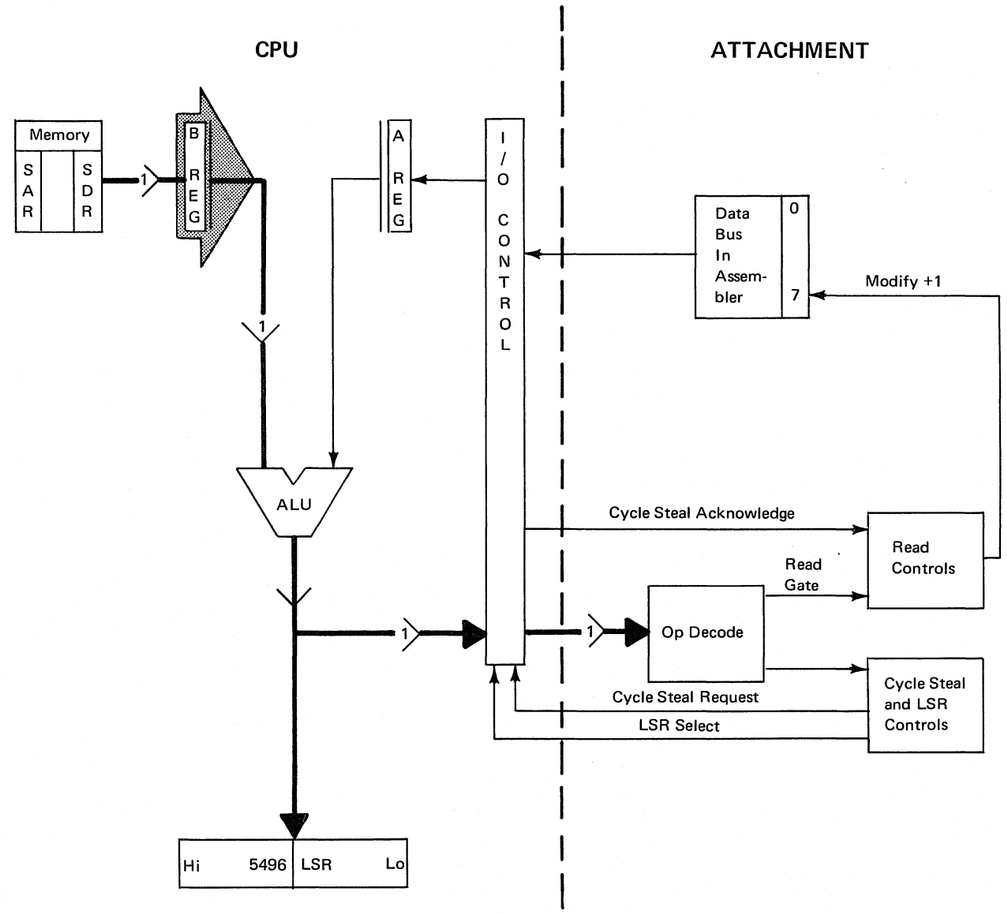
A diagnostic cycle steal operation is initiated in the data recorder attachment if bits 6 and 7 equal 00 in the Q byte. At the time the diagnostic cycle steal instruction is decoded, an 'early priority request' is made in the attachment and the read line is activated. At clock 2 time of the following cycle (I-R cycle), a cycle steal request is made to the CPU. When the request is granted, bit 7 of the data bus in assembler is set on so that the contents of the data recorder attachment LSR are incremented by +1. Following the cycle steal operation, the programmer can compare the contents of the LSR with its contents prior to the stolen cycle. (The programmer should load a known value into the LSR before the start I/O diagnostic cycle steal is issued.)

This diagnostic operation checks the cycle steal and LSR control circuits in the data recorder attachment. The block diagram shows the data flow for the diagnostic cycle steal operation.

- Start I/O diagnostic cycle steal decodes at clock 5 of I-Q cycle.
- Diagnostic cycle steal decode latch (RP311):

  Set at 'I-Q cycle sample' (decode time).
  Reset at 'rd I/O cycle', 'clock 1'.

  Note: 'rd I/O cy' latch operates as in a normal read cycle steal due to read gate being forced on.



LEGEND: 1 Op Code

BR0812

Section 11. CRT Attachment

This section of the 5406 FETMM contains the theory and maintenance diagrams for the 2265 Display Station Model 2 attachment. It consists of three chapters as follows:

Chapter 1. Introduction
Chapter 2. Functional Units
Chapter 3. Operations

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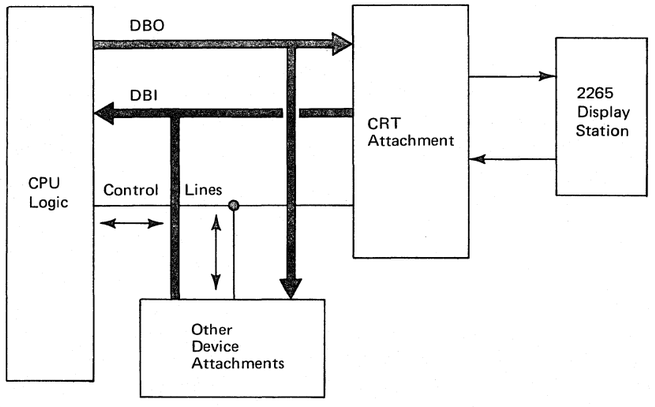
CRT ATTACHMENT

The IBM 2265 Display Station attachment is the interface between the display station and the CPU. It provides a means for the display station to use the facilities of the CPU to communicate with main storage. The attachment is located in the main gate of the CPU in position A-B1 and uses three, four wide cards.

Instructions and data from the CPU are sent to the attachment via the data bus out (DBO) lines. Attachment information is returned to the CPU via the data bus in (DBI) lines. Control and timing signals not under program control are sent and received via control lines between the attachment and CPU.



The CRT attachment contains logic to:

1. Decode program instructions
2. Detect error conditions
3. Generate cycle steal requests (CSR)
4. Address the LSR assigned to the CRT (CRTAR)
5. Modify the LSR address (generate constants)
6. Check the LSR address to detect when 960 characters have been displayed
7. Generate timing signals required by the display station for a display operation
8. Indicate attachment and display station status (operating and error conditions)

Program Instructions

The CRT uses four program instructions. Each instruction is decoded by the CRT attachment to develop gate signals to initiate and control the specific operation as defined in the instruction Q and R bytes. Only instructions with the CRT address in the device address are accepted by the CRT attachment. The CRT address is 1001 (9).

The program instructions are as follows:

1. Load I/O (LIO)
2. Test I/O (TIO)
3. Sense I/O (SNS)
4. Start I/O (SIO)

Load I/O addresses the LSR assigned to the CRT to (1) load a core storage address of the CRT data field into the LSR, (2) gate the CRT attachment to retain the address where the data field began, and (3) reset the display station CRT beam to the upper left corner of the screen.

Test I/O is used by the program to test operating or error conditions of the CRT attachment and display station. Program branching may result from the indications returned from the test I/O instruction.

Sense I/O transfers CRT status information or the address in the CRT LSR into main storage to be used by the program.

Start I/O initiates or halts a CRT display operation. The start I/O halt may be used in diagnostic programs to check the operational status of the CRT attachment.

Error Detection

The CRT attachment checks for the following error conditions:

1. Data parity
2. Display station not ready

Data parity is checked at the DBO at all times. On each cycle steal granted to the CRT, parity is checked within the CRT attachment at the data register. (The data register stores the data byte received from the CPU.) Any parity error condition forces the CPU to a hard halt at the end of the cycle in which the parity check was detected. All parity checks are latched (retained) in the attachment in order to be checked by program instructions (test I/O or sense I/O). Parity check conditions are reset by:

1. System reset
2. Check reset
3. The CRT attachment accepting a SIO instruction

A CRT not ready condition occurs when a start I/O instruction is issued to the CRT device and the display station power is not on. Not ready condition is indicated at the operator's console by lighting the CRT I/O attention lamp. The lamp remains lit until the CRT is made ready (power is restored to the display unit).

Cycle Steal Requests

Cycle steal requests are generated by the CRT attachment to signal the CPU to transfer data to the CRT or to modify the CRTAR (LSR) address. The CRTAR is selected during a cycle steal request to locate the main storage address of the data field (it may be a byte within the data field) or to modify the CRTAR address. CRT attachment cycle steal requests are thirteenth in priority of the cycle steal I/O devices. The CRT cycle steal request may be overridden by a higher priority I/O device and requires the CRT to keep issuing its cycle steal request until the CPU acknowledges the request by returning DBO bits 1 and 5. This signals the CRT attachment that the next machine cycle is granted to the CRT and is referred to as an I/O cycle.

Local Storage Addressing

Local storage register CRTAR is addressed by the CRT attachment by selecting LSR select lines 3 and 6, without ledger card device (with ledger card device installed on the printer, CRTAR is addressed with LSR select lines 6 and 7). The CRTAR is addressed during:

1. Cycle steal requests (CSR)
2. A load I/O instruction cycle
3. A sense I/O instruction

Cycle steal cycles address the CRTAR to locate the data field address and to modify the LSR address.

Load I/O instruction addresses CRTAR to load the LSR with the main storage address of the first byte of the data field.

Sense I/O instructions address the CRTAR to sense the address presently in the LSR and transfer the information into main storage.

Constants

Constants are generated by the CRT attachment to increment or decrement the CRTAR address. Constants are returned to the CPU during a cycle steal request, by activating DBI lines that represent the binary value of the desired constant. The constants generated are:

1. +1 (DBI line 7 during the modify lo cycle)
2. −192 (DBI lines 0 and 1 during the modify lo cycle)
3. −768 (DBI lines 6 and 7 during the modify hi cycle)

Modify plus one is generated each data transfer cycle steal to increment the LSR address to the next data byte in the data field. The LSR address is incremented by one until the LSR address is 960 above the starting address of the data field which indicates the end of the data field. A cycle steal request is then made to subtract 960 from the incremented address in the LSR to return it to the starting address of the display field so the CRT can display the data again. Subtract 960 must be broken into two times, as the LSR address contains two bytes. During the modify lo cycle, 192 is subtracted from the LSR lo byte, during the modify hi cycle 768 is subtracted from the LSR hi byte.

Local Storage Register Address Increment Checking

The LSR address must be checked for each increment of 64 or 960 above the starting address of the data field address.

Each increment of 64 of the LSR address indicates that the display station has displayed 64 characters (one line on the CRT screen) and the display station needs a retrace signal (to move the CRT beam back to the left side of the CRT screen). An increment of 960 indicates that the display station has displayed 15 lines and a restore signal is needed (to move the CRT beam to the upper left corner of the CRT screen in position to start another display cycle).

Attachment logic detects each increment of 64 and 960 in the LSR address and develops the signals to initiate a retrace or restore cycle in the display station.

Note: The data field starts on a XX01 boundary; therefore the 64th or 960th character is indicated when the LSR address is 65 or 961 respectively.

CRT Attachment Timing

CRT attachment logic provides the following timing signals to the display station:

1. Step display
2. Start character generator
3. Reset display

Step display indexes the CRT beam to the next character position on the CRT screen. The 65th step display signal, which indicates the end of a line display, causes the display station to move the CRT beam to the left edge of the CRT screen, and the CRT attachment to generate a time-out signal (approximately 288 μs) to allow the display station time to complete the retrace. Step display signals are generated at the start of each character display cycle and are 4.5 μs in duration.

Start character generator signals the display station to start displaying a character. This signal is active 6 μs after the beginning of step display and is 1.5 μs in duration.

Reset display initiates a restore cycle in the display station (moves the CRT beam to the upper left corner of the CRT screen) and starts a delay in the CRT attachment to allow the display station to complete the restore cycle. This signal is also active when the attachment detects that the LSR address has incremented 960.

CRT Attachment Status

A sense I/O instruction causes the CRT attachment to gate the CRT attachment error latch and signal line conditions (status) onto the DBI and the information transferred to main storage. A test I/O instruction tests the CRT attachment for error or busy conditions and causes the attachment to return an indication about the result of the test to the CPU (I/O condition A and I/O condition B signals).

IBM 2265 DISPLAY STATION MODEL 2

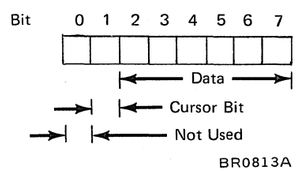
The 2265 Display Station Model 2 provides visual access to data in main storage. Data is displayed on a cathode ray tube (CRT) in the display station in 15 lines of 64 characters in each line (960 characters). A character position marker (cursor) may be displayed at each character position either with or without the character. The cursor and character display are under program control.

System Console

There are no controls for the display station on the system console, only an indicator that lights when a program instruction is issued to the CRT and the CRT is not ready (power is off at the display station). The CRT I/O attention indicator remains lit until the CRT is made ready (power is turned on at the display station) or a system or check reset is performed. A system reset stops a display operation if one is in progress.

Data

The character set for the display station consists of 64 characters, each character is encoded in a 6 bit EBCDIC sub-set. The seventh bit is for cursor control. Format of the data byte for the CRT is as shown:



Each character may have a cursor displayed with it if bit 1 equals 0. No cursor is displayed if bit 1 equals 1.

The following table shows the characters the CRT can display and the 6 bit code for each.

Code Bit 01234567	Character	Code Bit 01234567	Character
000000	Blank	100000	-
000001	A	100001	/
000010	B	100010	S
000011	C	100011	T
000100	D	100100	U
000101	E	100101	V
000110	F	100110	W
000111	G	100111	X
001000	H	101000	Y
001001	I	101001	Z
001010	¢	101010	Blank
001011	.	101011	,
001100	<	101100	%
001101	(	101101	_
001110	+	101110	>
001111	|	101111	?
010000	&	110000	0
010001	J	110001	1
010010	K	110010	2
010011	L	110011	3
010100	M	110100	4
010101	N	110101	5
010110	O	110110	6
010111	P	110111	7
011000	Q	111000	8
011001	R	111001	9
011010	↑	111010	:
011011	$	111011	#
011100	*	111100	@
011101	)	111101	'
011110	;	111110	=
011111	¬	111111	≠

Bit 0 is not used.

Bit 1 is the cursor bit.

BR0814A

The data to be displayed is located in the display field in main storage.

If bit 1 = 0 a cursor is displayed with the character.
If bit 1 = 1 the cursor is not displayed.
If bit 1 = 0 and bits 2 through 7 = 0, only a cursor is displayed.

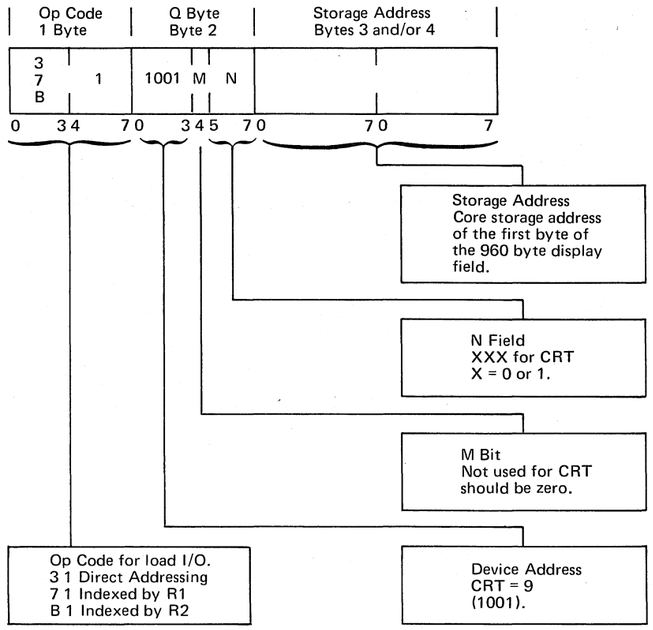
Local Storage Register

A local storage register (LSR), located in the CPU, is assigned to the CRT display station. This register (CRTAR) contains the address of the CRT display field in main storage. The display field contains the data to be displayed on the CRT display station screen. Before the start of a display operation, the CRTAR must be loaded with the main storage address of the first data byte in the display field. As each data byte is displayed, the LSR (CRTAR) address is updated by one so the next data byte is addressed when the LSR is addressed again.

The display field is a sequential 960 byte area in core that may start at any XX01 address. (XX is any hexadecimal address that is 960 bytes less than maximum core capacity.) The entire field (960 bytes) is displayed.

LOAD I/O (LIO) INSTRUCTION FORMAT

This instruction is issued to the CRT attachment to load the LSR (CRTAR) assigned to the CRT with the starting address of the display field in core storage. The format of the load I/O instruction is:



BR0816

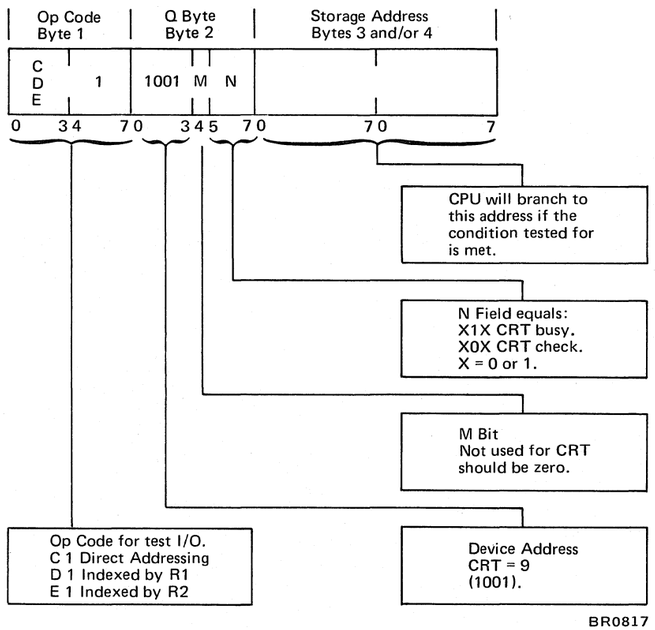
A display station CRT beam reset occurs during a load I/O instruction. (CRT beam is moved to the upper left corner of the CRT screen.) The CRT attachment starts a 288 μs delay to allow time for the display station to complete the reset. This delay interlocks the attachment so that other instructions (except sense and test I/O) cannot start until the delay times out.

A ready condition in the display station is not needed for the load I/O instruction execution. If the CRT attachment is busy (in a display operation), the load I/O instruction is rejected by the CRT attachment and causes the CPU to reissue the load I/O instruction. (The CRT attachment is always busy when executing a SIO display instruction, therefore the CPU will hang in a loop (IR backup) until the system power is turned off or a system reset is performed.)

The CRT attachment must retain where the display field was started in main storage in order to check the LSR address for each increment of 64 and 960. The load I/O instruction is ANDed with the DBO lines and Not EB 1 cycle to set the required latches in the attachment.

TEST I/O (TIO) INSTRUCTION FORMAT

The test I/O and branch instruction test the CRT attachment for error or busy conditions and branches the CPU to a specific address if the condition tested for is met. The format of the test I/O instruction is:



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Conditions that can be tested in the CRT are:

1. CRT busy
2. CRT check

CRT Busy (N Field Code = X1X)

A busy condition exists when the attachment is executing a start I/O display instruction.

CRT Check (N Field Code = X0X)

The following conditions cause a CRT check:

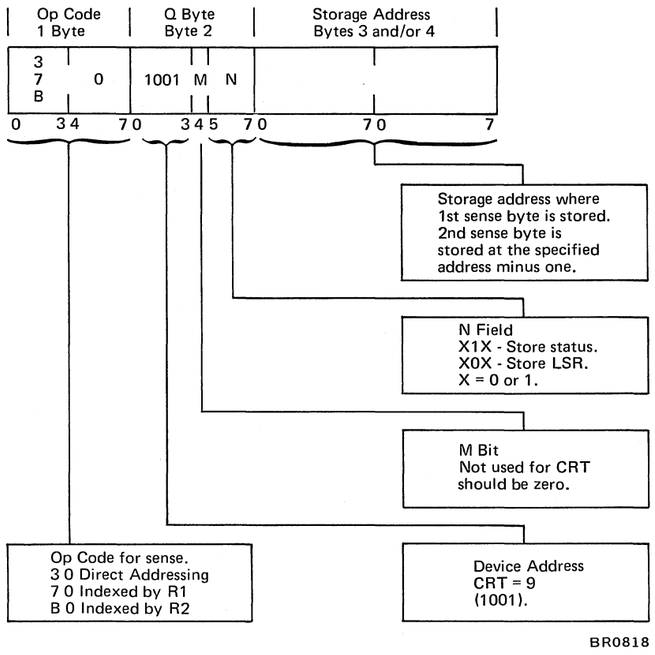
1. A parity error in the data register of the CRT attachment. (The data register contains the data byte for the CRT display.)
2. CRT display station not ready. This indicates that power to the display station is off. (Power on indicator on the 2265 is not lit.) The display station is made ready by restoring power to it.

The test I/O instruction is always executed.

SENSE I/O (SNS) INSTRUCTION FORMAT

A sense instruction is issued to the CRT attachment to transfer the attachment status or LSR (CRTAR) information into main storage.

The format of the SNS instruction is:



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Store Status (N Field Code = X1X)

Two bytes of attachment status are transferred into main storage at the address specified by the storage address of the instruction. Status byte one is placed in the address as specified in the sense operand one address, status byte two is placed in storage at the operand one address minus one.

The status bytes are as follows:

Status Byte One

First E-B Cycle (Operand 1 Address)

Bit 0 Write op (diagnostic only)
Bit 1 Start char gen (diagnostic only)
Bit 2 Step-display (diagnostic only)
Bit 3 Cycle steal request (diagnostic only)
Bit 4 Display reset (diagnostic only)
Bit 5 Data register parity check
Bit 6 Display not ready
Bit 7 Cycle steal acknowledged (diagnostic only)

Status Byte Two

E-B Not First Cycle (Operand 1 Address Minus One)

Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
} Contents of the data register

Bit P (regenerated)

Status bits 0 through 4, and bit 7 of status byte one and status byte two are used for diagnostic programs only. The diagnostic bits in status byte one are CRT attachment signal lines of the same name. The bits of status byte two are the data register outputs 0 through 7.

Store LSR (N Field Code = X0X)

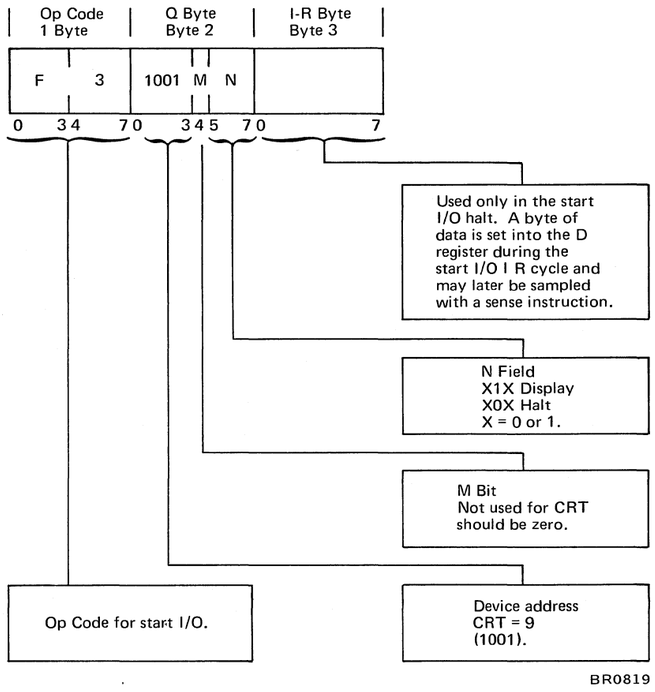
The LSR address is stored at the operand one address specified in the instruction.

A sense instruction is always executed.

START I/O (SIO) INSTRUCTION FORMAT

A start I/O instruction is issued to the display station to start or halt a display operation. The halt instruction may also be used for diagnostic purposes.

The format of the start I/O instruction is:



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Display (N Field = X1X)

The CRT attachment decodes the start I/O instruction when the device address in the Q byte equals nine (hexadecimal 1001). If the N field of the Q byte equals X1X (X may be either a one or zero) the CRT attachment is conditioned to start a display of the characters in the display field on the CRT screen. After the start I/O I-Q and I-R cycles are complete, the CRT attachment generates cycle steal requests. Each I/O cycle addresses the CRTAR (LSR) for the location of the display field and increments the LSR address by one so that the next selection of the CRTAR addresses the next sequential character in the display field. A data character is sent to the CRT attachment during the I/O cycle and this character is displayed on the CRT screen. As soon as the character is displayed, another cycle steal request is made for the next character in the display field. This action is repeated until the LSR address has incremented 64 (or a multiple of 64) above the starting address of the display field. Each increment of 64 in the LSR address indicates that 64 characters have been displayed and a retrace is needed in the display station. A retrace delay of approximately 273 to 288 microseconds is started to allow time for the CRT beam to move to the left edge of the CRT screen in position for the next line of display. No cycle steal requests are made during the delay time-out. Cycle steal requests are started again when the retrace delay times out.

When the LSR address has incremented 960 above the starting address of the display field (actual address in the LSR is 961 because the display field starts on a XX01 boundary), a restore operation is needed in the CRT (end of frame) to return the CRT beam to the upper left corner in position to start a frame of display again. The same delay described for retrace is started for beam repositioning. The LSR address is decremented by –960 during the restore cycle, so that the CRT begins its display back at the start of the display field. Cycle steal requests are made after each character display to refresh the CRT screen at a rate of approximately 54 frames per second. If a new load I/O instruction is not issued to a new start I/O display instruction, the attachment begins its display with the character located at the current address in the CRTAR. The start I/O display instruction is accepted by the CRT attachment only when it is not busy and the display station is ready.

The CRT attachment is always busy when executing a SIO instruction. If a SIO instruction is issued to a busy CRT attachment, the CPU will operate in IR backup mode until the system power is turned off or a system reset is performed.

Halt (N Field = X0X)

A start I/O halt instruction is issued to the CRT to:

1. Stop a display operation.
2. Determine if data flow to the CRT attachment is correct.

A start I/O halt stops the display on the CRT and ends further cycle steal requests. A start I/O display instruction must be reissued to the CRT before a display operation starts again.

For diagnostic purposes, a start I/O halt loads the data register in the CRT attachment with a data character during the I-R cycle of the instruction. The data register may then be sensed with a sense instruction and compared to the data sent to the data register to determine if the data was transferred to the CRT attachment correctly.

The CRT attachment accepts a start I/O halt instruction at any time.

Chapter 2. Functional Units

INTRODUCTION TO FUNCTIONAL UNITS

Chapter 2 contains the functional units of the CRT attachment and the error checking circuits.

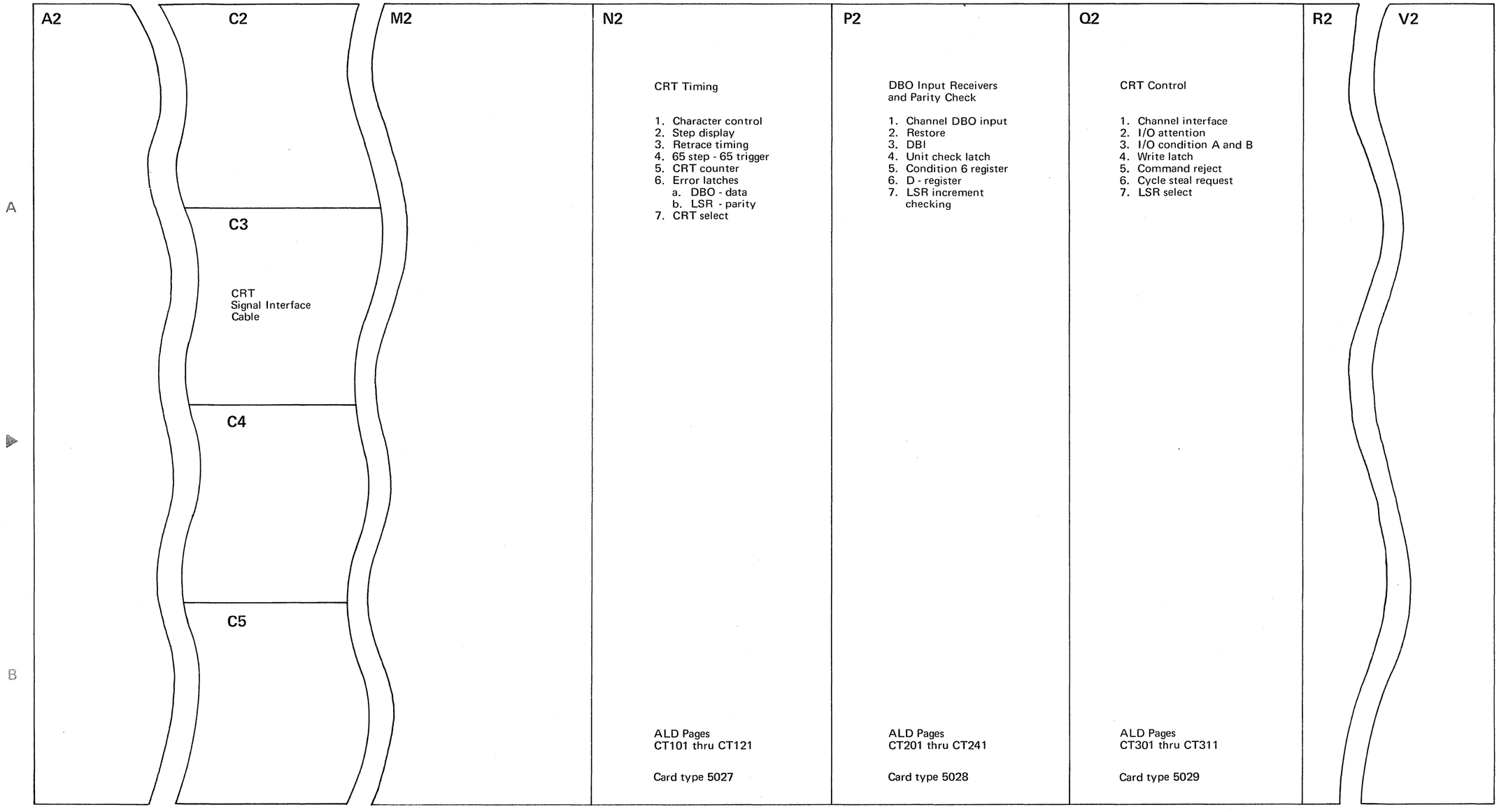
The first page of the chapter is a board layout of the CRT attachment. It is broken down into cards and contains the following information:

1. Card locations.
2. Circuits found on that card.
3. ALD page reference numbers that describe the circuits found on the card.
4. Card type number. The part number of the card will change each time that the card has an engineering change to it. The card type number, however, will always stay the same.

The card location number appears on each page, or section of a page, that describes the circuitry on that card. For example, Q2 on a page refers to LSR select.

Symbols

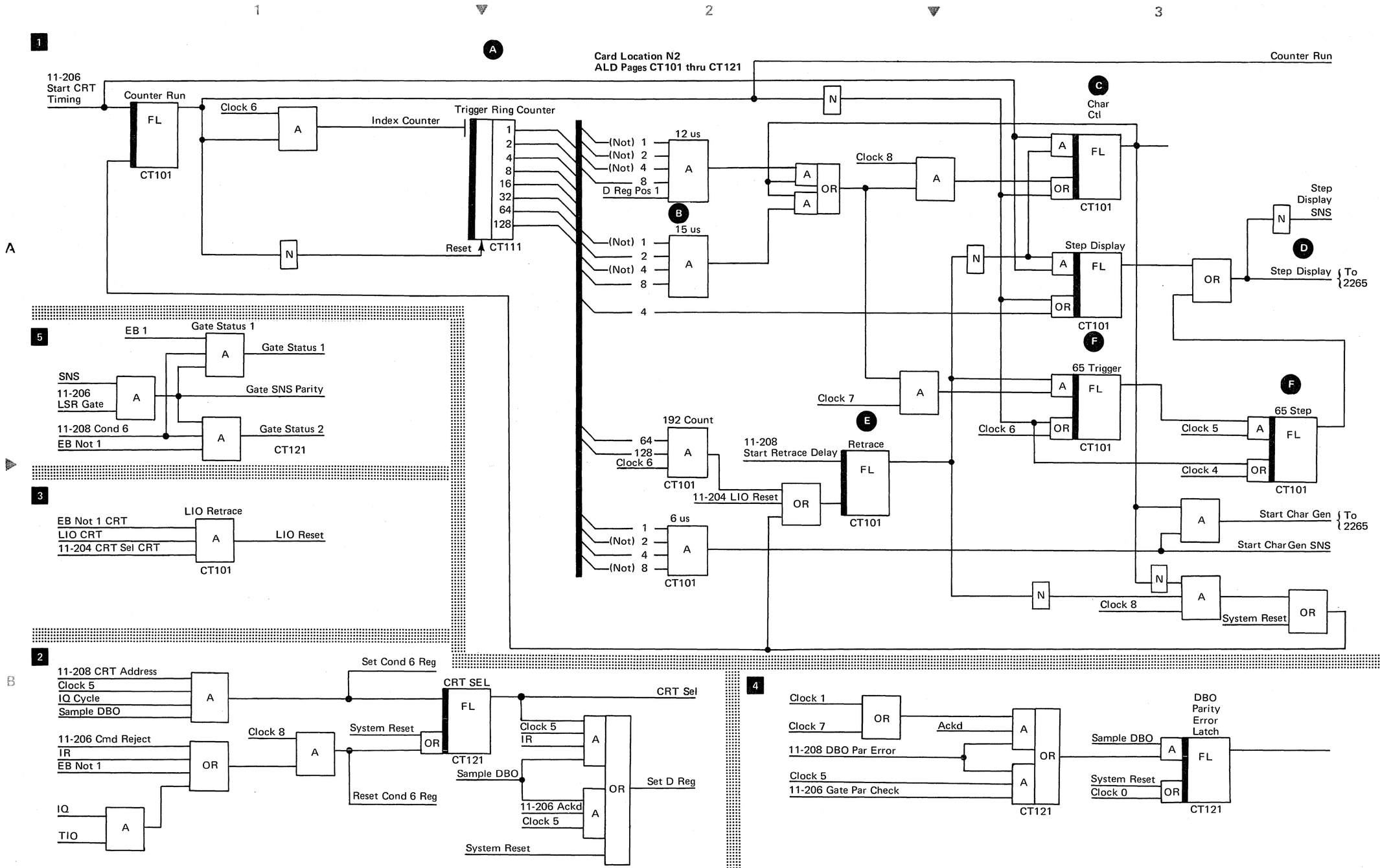
Figures within this chapter contain the symbols: 1 numbers in squares, and A letters in circles. These symbols refer to text, marked with an identical symbol, that describes or explains the function of the unit marked in the figure.



CRT Attachment Board B1* on Gate A (A-B1)

Board B1 also contains:

1. Channel banks
2. Keyboard attachment
3. Data recorder
attachment


Card Location N2
ALD Pages CT101 thru CT121
11-206 Start CRT Timing
Counter Run
FL
CT101
Clock 6
A
Index Counter
Trigger Ring Counter
1
2
4
8
16
32
64
128
Reset
CT111
N
(Not) 1
(Not) 2
(Not) 4
8
D Reg Pos 1
12 us
15 us
OR
Clock 8
Char Ctl
Step Display
Step Display SNS
Step Display
To 2265
65 Trigger
65 Step
Clock 5
Clock 4
Clock 7
Clock 6
192 Count
64
128
11-208 Start Retrace Delay
Retrace
11-204 LIO Reset
6 us
Start Char Gen
To 2265
Start Char Gen SNS
System Reset
EB 1
Gate Status 1
SNS
11-206 LSR Gate
Gate SNS Parity
11-208 Cond 6
EB Not 1
Gate Status 2
CT121
LIO Retrace
LIO CRT
11-204 CRT Sel CRT
LIO Reset
11-208 CRT Address
Clock 5
IQ Cycle
Sample DBO
11-206 Cmd Reject
IR
IQ
TIO
Set Cond 6 Reg
Reset Cond 6 Reg
CRT SEL
CRT Sel
Sample DBO
11-206 Ackd
Set D Reg
Clock 1
Ackd
11-208 DBO Par Error
11-206 Gate Par Check
DBO Parity Error Latch
Clock 0

1 CRT DISPLAY STATION TIMING

A CRT display station basic timing is provided with the trigger ring counter and its decoding logic. The counter is indexed at the trailing edge of each clock 6 time when the 'counter run' latch is set. During a display operation a cycle steal is requested whenever 'counter run' is not active.

B Twelve microsecond decode ANDed with a 'D register' one bit position gates the turn off of the 'character control' latch when the counter indexes to 8. This is the time required by the CRT to display a character without a cursor. The 'D register' input signals the decode block if a cursor is not to be displayed with this character. If a cursor is to be displayed, the 'D register' input prevents the turn off of the 'character control' latch until a later time. Fifteen microsecond decode turns off the 'character control' latch at counter 10 time and provides the timing to the CRT when a cursor is displayed with the character.

C 'Character control' latch is set at the start of each character display cycle. It remains set for either 12 or 15 microseconds depending on which turn off decode block gates its reset at clock 8 time. 'Character control' is active for the length of time to display one character (with or without a cursor) and includes the time to index the CRT beam to the next position. 'Character control' ANDed with another counter decode condition, '6 microsecond', activates the CRT interface line 'start character generator'.

D 'Step display' latch is set at the same time that 'character control' is set. 'Step display' remains set until counter four time. The 'step display' latch generates a CRT interface signal of the same name and is used to index the CRT beam to the next character position on the CRT screen. 'Step display' is active for 4.5 microseconds.

E The 'retrace' latch is active to generate a timing delay in the CRT attachment to allow time for a CRT beam retrace or restore operation. 'Retrace' latch active prevents 'character control' from generating a reset counter run signal and allows the counter to index to a count of 192. The time of the delay generated may vary due to the actual count in the counter at the time 'retrace' is active, but is 273 to 288 microseconds. 'Retrace' latch is reset when the counter reaches 192 and during load I/O commands.

F '65 trigger' and '65 step' latch are set at the end of a line display (64th character) to delay the step display signal to the CRT unit. The 65th step display signal resets a counter in the display unit to move the CRT beam back to the left side of the CRT screen to begin another line of display. Without delaying the step display signal, the CRT may distort (cut off) the trailing portion of character or cursor strokes for the 64th character, due to an early retrace signal.

2 CRT ATTACHMENT SELECTION

'CRT select' is set during the I-Q cycle of an I/O instruction and is the gate to indicate that the information on the DBO is for the CRT. A gate to set the condition register is generated at this time.

3 RESET FOR LOAD I/O INSTRUCTION

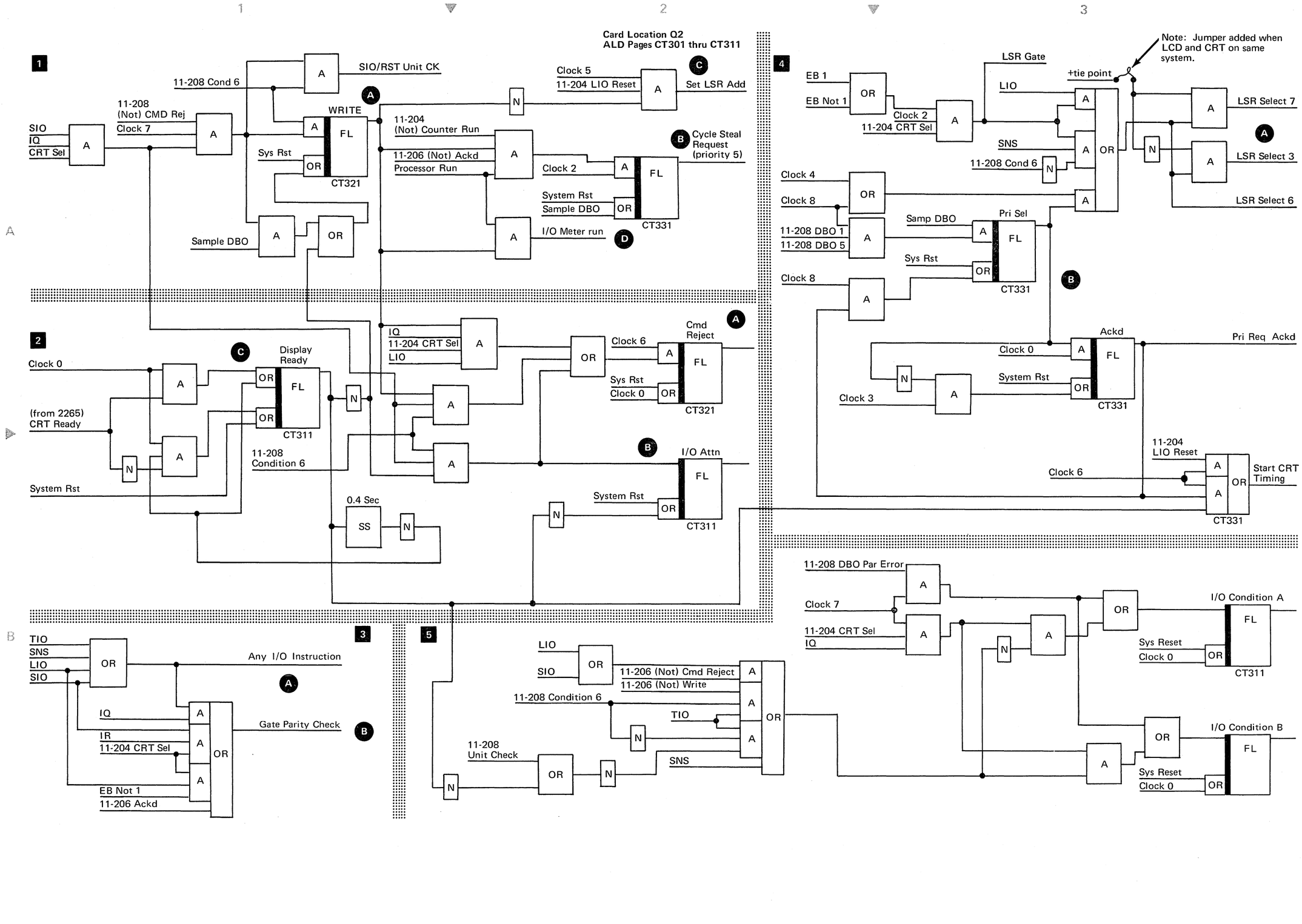
'LIO reset' is generated at 'EB not 1' cycle to indicate the last machine cycle of a load I/O instruction.

4 DBO PARITY ERROR

'DBO parity latch' is set whenever an error (parity) is detected on DBO at clock 5 time in an I/O instruction, or clock 1, 5, or 7 time during a cycle steal cycle.

5 STATUS GATES FOR SENSE INSTRUCTION

Gate status one and gate status two are generated to gate the sense bytes onto DBI at 'EB-1' and 'EB not 1' respectively. The parity of the sense bytes may not be odd, therefore a parity generate signal 'gate sense parity' is provided at each sense byte time.


Card Location Q2
ALD Pages CT301 thru CT311
1
2
3
4
5
SIO/RST Unit CK
11-208 Cond 6
11-208 (Not) CMD Rej
Clock 7
SIO
IO
CRT Sel
WRITE
Sys Rst
CT321
Sample DBO
11-204 (Not) Counter Run
11-206 (Not) Ackd
Processor Run
Clock 5
11-204 LIO Reset
Set LSR Add
Cycle Steal Request (priority 5)
Clock 2
System Rst
Sample DBO
CT331
I/O Meter run
Clock 0
(from 2265) CRT Ready
Display Ready
CT311
11-208 Condition 6
System Rst
0.4 Sec
SS
IO
11-204 CRT Sel
LIO
Clock 6
Cmd Reject
I/O Attn
TIO
SNS
LIO
SIO
Any I/O Instruction
IR
Gate Parity Check
EB Not 1
11-206 Ackd
11-206 (Not) Cmd Reject
11-206 (Not) Write
11-208 Unit Check
LSR Gate
+tie point
Note: Jumper added when LCD and CRT on same system.
EB 1
LSR Select 7
LSR Select 3
LSR Select 6
SNS
Clock 4
Clock 8
11-208 DBO 1
11-208 DBO 5
Samp DBO
Pri Sel
Ackd
Pri Req Ackd
Clock 3
11-204 LIO Reset
Start CRT Timing
11-208 DBO Par Error
I/O Condition A
I/O Condition B
Sys Reset

1 CYCLE STEAL REQUEST

A The 'write' latch is set when a CRT start I/O display instruction is decoded. The 'write' latch is turned off by a start I/O halt instruction or by the CRT display station going to a (not) ready condition (power off).

B Cycle steal requests are made when: (1) the CRT 'write' latch is on, (2) 'counter run' is inactive, (3) the display station is not timing out for a restore or retrace delay, and (4) 'processor run' is active.

C 'Set LSR address' gates the 'not 6' and 'not 7' latches during the 2nd cycle of a load I/O instruction. LSR hi address is on the DBO at this time.

D 'I/O meter run' is on if the 'write' latch is on and conditions for 'process run' are met.

2 ERROR DETECTION

A 'Command reject' and 'I/O attention' indicate conditions of the CRT display unit and CRT attachment status. 'Command reject' latch is set if:

1. The 'write' latch is set and a load I/O instruction attempted.
2. The 'write' latch is set and a start I/O (display) is attempted. Start I/O halt instruction is always executed.
3. A start I/O display instruction is attempted and the display station is not ready (power off).

B 'I/O attention' latch is set if a start I/O instruction is attempted and the display station is not ready.

C The 'CRT ready' line from the 2265 is sampled with clock zero. The 'display ready' latch is set if the ready line is active. A single shot stabilizes the turn on of the 'display ready' latch if the ready line is erratic.

3 I/O INSTRUCTION

A This logic is active when the CRT attachment is decoding an I/O instruction.

B 'Gate parity check' is a condition to set the 'parity error' latch if the DBO parity is even during the following times:

1. An I/O instruction I-Q cycle
2. A start I/O instruction I-R cycle
3. An I/O cycle
4. A load I/O instruction during EB not 1 cycle

4 LSR SELECT

A The CRTAR (LSR) is addressed with LSR select lines 3 and 6 if the ledger card device is not installed on the system printer. If ledger card is installed, CRTAR is selected with LSR select lines 6 and 7. The LSR is selected for:

1. A load I/O instruction to load the starting address of the data field into the LSR.
2. An I/O cycle to modify the LSR address plus 1 for each I/O cycle or to subtract 960 from the updated address.
3. A sense instruction to sense the address in the LSR and transfer the information into core storage.

B 'Pri select' latch is set when the CPU acknowledges a CRT I/O cycle request by returning DBO 1 and 5 active at clock 8 time. 'Ack'd' is set at clock 0 time to extend LSR selection into the next adjacent CPU cycle for LSR address increment checking and to modify the LSR address. 'Ack'd' ANDed with clock 6 starts the CRT timing cycle.

5 I/O CONDITION A AND B CONTROL

I/O condition A and B are used together to indicate to the CPU (1) the status of the CRT attachment when an instruction is issued to it, and (2) error conditions during an operation.

I/O Attachment Condition					I/O Condition A	I/O Condition B	CPU Reaction
I-Q Cycle of Any I/O Instruction	Incorrect DBO Parity				1	1	Processor Check Stop
	Correct DBO Parity	Q Byte Not Correct			0	0	Processor Check Stop
		Correct Q Byte	Sense Instruction		0	1	Proceed to Next Sequential Instruction
			SIO or LIO Instruction	Reject Instruction	1	0	Retry I/O Instruction
				Accept Instruction	0	1	Proceed to Next Sequential Instruction
			Test I/O	Condition Not Met	0	1	Proceed to Next Sequential Instruction
				Condition Met	1	0	Branch to Effective Address
SIO I-R, LIO E-B, and I/O Cycles	Incorrect DBO Parity				1	1	Processor Check Stop
	Correct DBO Parity				0	0	Continue as Normal

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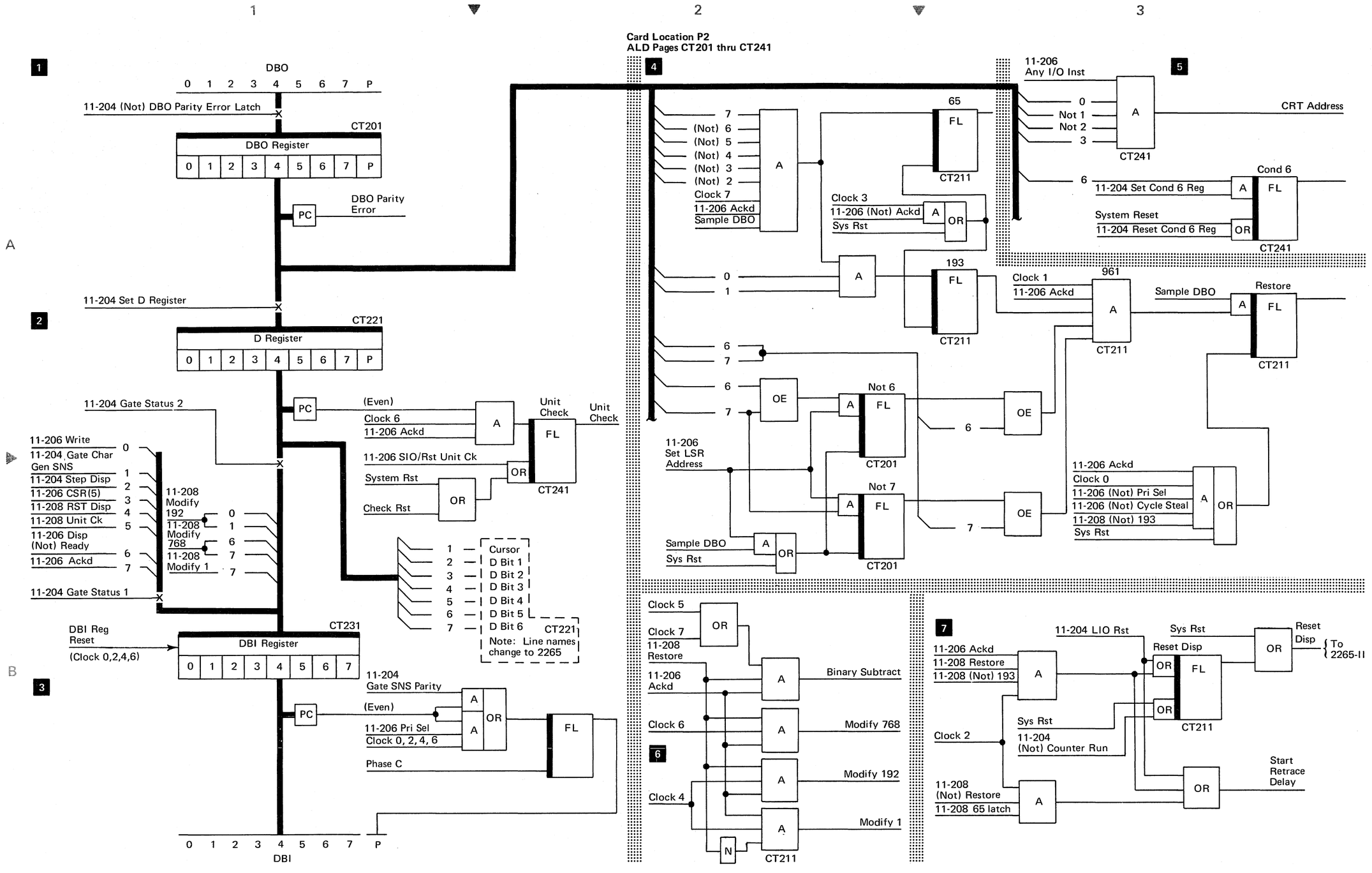

1
2
3
Card Location P2
ALD Pages CT201 thru CT241
DBO
0 1 2 3 4 5 6 7 P
11-204 (Not) DBO Parity Error Latch
CT201
DBO Register
DBO Parity Error
PC
11-204 Set D Register
CT221
D Register
11-204 Gate Status 2
(Even)
Clock 6
11-206 Ackd
11-206 SIO/Rst Unit Ck
System Rst
Check Rst
Unit Check
FL
CT241
11-206 Write
11-204 Gate Char Gen SNS
11-204 Step Disp
11-206 CSR(5)
11-208 RST Disp
11-208 Unit Ck
11-206 Disp (Not) Ready
11-206 Ackd
11-204 Gate Status 1
11-208 Modify 192
11-208 Modify 768
11-208 Modify 1
Cursor
D Bit 1
D Bit 2
D Bit 3
D Bit 4
D Bit 5
D Bit 6
CT221
Note: Line names change to 2265
DBI Reg Reset
(Clock 0,2,4,6)
CT231
DBI Register
11-204 Gate SNS Parity
(Even)
11-206 Pri Sel
Clock 0, 2, 4, 6
Phase C
DBI
4
5
11-206 Any I/O Inst
CRT Address
CT241
Cond 6
11-204 Set Cond 6 Reg
System Reset
11-204 Reset Cond 6 Reg
Clock 3
11-206 (Not) Ackd
Sys Rst
65
CT211
193
961
Clock 1
Sample DBO
Restore
11-206 Set LSR Address
Not 6
Not 7
CT201
11-206 Ackd
Clock 0
11-206 (Not) Pri Sel
11-206 (Not) Cycle Steal
11-208 (Not) 193
Clock 5
Clock 7
11-208 Restore
Binary Subtract
Modify 768
Modify 192
Modify 1
Clock 4
6
7
11-204 LIO Rst
Reset Disp
To 2265-II
11-208 (Not) 193
Clock 2
11-204 (Not) Counter Run
11-208 (Not) Restore
11-208 65 latch
Start Retrace Delay

1 DBO REGISTER

- Receives data and control information from DBO.
- Output is parity checked.
- Latches up (retains its status) when a DBO register parity error is detected.
- Output is gated into other CRT attachment logic.

2 DATA REGISTER (D REGISTER)

- Is set during a start I/O I-R cycle or during an I/O cycle.
- Status may be sensed with a sense instruction.
- Positions 1 through 7 are gated to the display station and contain data for the CRT display. Position 1 is the cursor bit, 2 through 7 are data.
- Output is parity checked. If an error is detected, unit check latch is set.

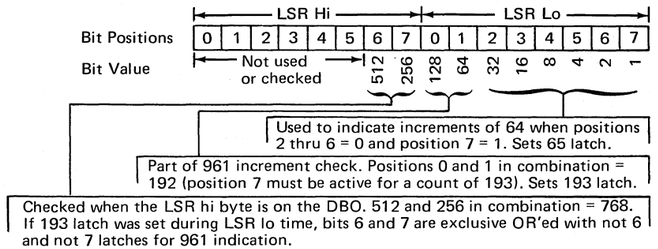
3 DBI REGISTER

- Output is parity checked. A parity bit is generated if one is needed.
- Is reset at sample DBO time during clock 0, 2, 4, and 6 time. The 'parity bit' latch is reset at each phase C time.
- Input may be from three sources: (1) 'D register' output, (2) CRT status, and (3) constants generator, modify +1, −192 and −768.

4 LSR ADDRESS 64 and 960 INCREMENT CHECK

The data field for the CRT display station may start at any hexadecimal XX01 address. (XX is any core address that is 960 bytes less than maximum core capacity.) The CRT attachment must retain an indication of where the data field was started in order to check for each increment of 960 above the starting address. This indication is needed in the attachment to signal the end of the data field and perform a restore cycle in the display station. A hexadecimal count of 960 requires more bit positions than a hexadecimal byte contains; therefore the two least significant bits of the LSR hi address are used to extend the count to include 960.

Format of the bit value assignment of the LSR address:



BR0821A

Note: The data field starts on a XX01 boundary, therefore the LSR address indicates 65 for an increment of 64 or 961 for an increment of 960.

During a load I/O instruction when the LSR is loaded with the address of the display data field, two latches ('not 6' and 'not 7') are set or reset together to retain the binary boundary (256 or 512) at which the data field address started. The 'not 6', 'not 7' latches are set during the second cycle of the load I/O EB cycles when the LSR hi portion of the address is on DBO.

The conditions to set-reset the 'not 6', 'not 7' latches are as shown:

DBO 6 and	Bits 7		Not 6	Not 7
0	0	———	0	0
0	1	———	1	1
1	0	———	1	0
1	1	———	0	1

0 = latch reset or inactive condition
1 = latch set or active condition.

BR0822A

The 960 count is spread across two LSR address bytes. Each byte is on the DBO at separate times. As a result, the 960 increment check must be made at two different times. During the time the LSR lo address byte is on DBO, it is checked for an increment of 192. If the 192 check is positive, the 193 latch is set to gate a check for 768 in the LSR hi byte. During the time the LSR hi address byte is on the DBO, gated by the '193' latch, the DBO lines are exclusive O Red (OE) with the 'not 6', and 'not 7' latches to check for an increment of 961.

The conditions needed to set the 961 signal are as shown:

DBO 6 and	Bits 7		Not 6	Not 7	
0	0	———	1	1	and '193' latch = 961
1	1	———	0	0	
1	0	———	0	1	
0	1	———	1	0	

BR0823A

During the time the LSR lo address is on DBO, DBO lines 2 through 6 are checked for zero and line 7 is checked for 1. If lines 2 through 6 are zero and line 7 is 1, this indicates an increment of 64. The '65' latch is set to gate the CRT attachment for a retrace operation.

5 CRT ADDRESS–CONDITION 6 REGISTER

These lines are conditioned from the DBO register. The CRT address is indicated when DBO bits 0 through 3 equal 1001 (9).

'Condition 6' register is set when bit 6 of the Q byte of an I/O instruction equals a 1 (active state). I/O instructions for the CRT have only two options (i.e.: start I/O display or halt). 'Condition 6' register gates the attachment logic for one option when it is set and the other option when it is reset.

6 CONSTANTS

This logic:

- Provides constants to increment or decrement the LSR address. +1 is generated each I/O cycle to increment the LSR address to the next data character in the display field. −192 and −768 decrement the LSR address when the end of the data field is indicated. −192 and −768 modify the LSR lo and hi respectively.
- 'Binary subtract' is active during the time −192 and −768 are generated to cause the ALU (in the CPU) to subtract.

7 RESET DISPLAY

This logic:

- Is part of an interface to the 2265 II
- Resets the display unit beam to the upper left corner of the CRT
- Starts a 288 (approximately) microsecond delay within the CRT attachment to allow time for the CRT beam to restore or retrace
- Starts a reset display when:
  1. A load I/O operation is issued to the CRT.
  2. 'System reset' is active.
  3. The LSR address has incremented 960.

Chapter 3. Operations

INTRODUCTION TO OPERATIONS

Chapter 3 contains detailed flowcharts and timing charts of the operations performed by the CRT display station attachment.

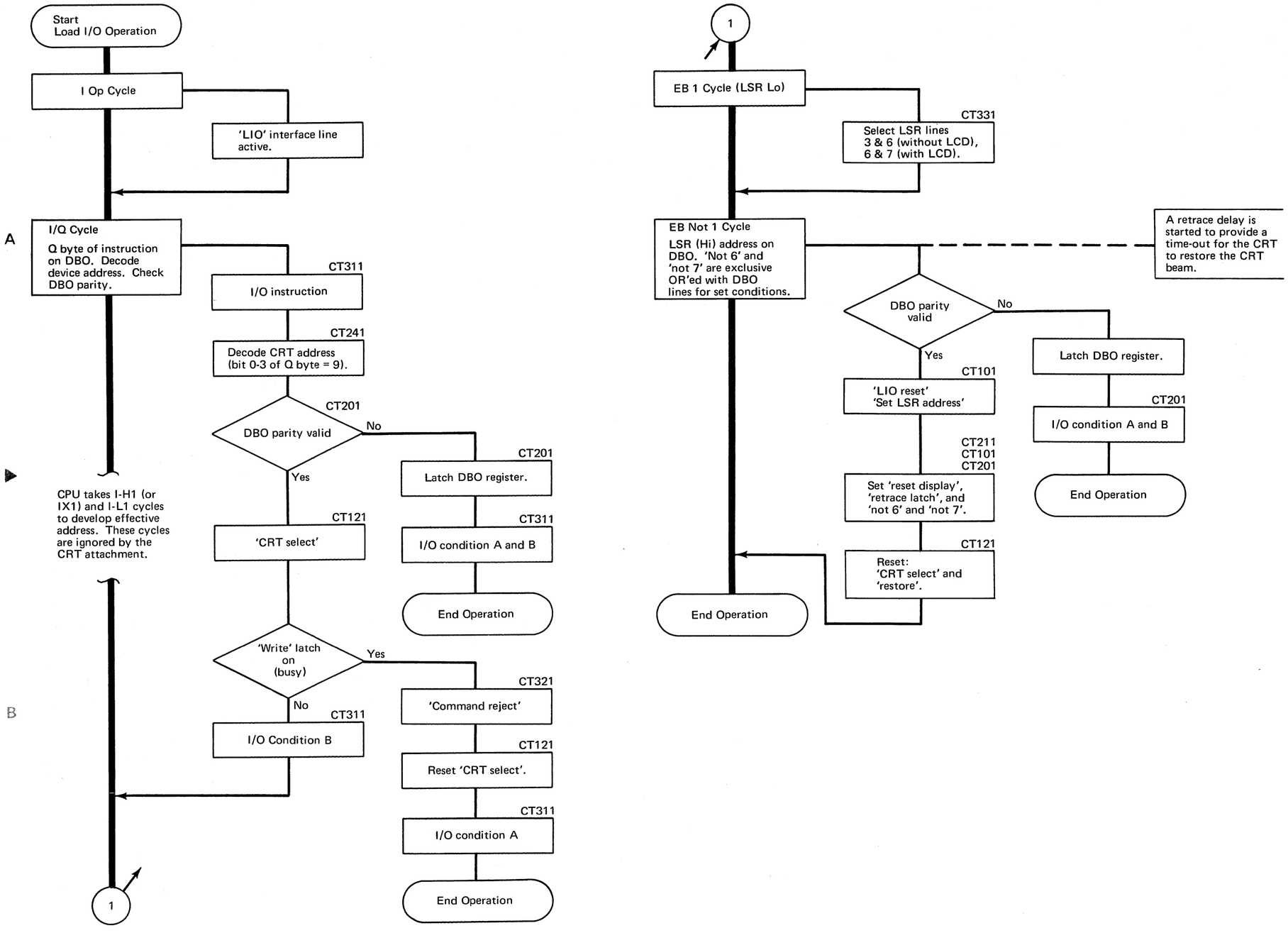
Flowcharts

The flowcharts contain three levels of information. By reading down the heavy dark lines, the reader can learn the major objectives of the operation. The second level of information is obtained by reading the information in the boxes that branch off the heavy dark line. The information that is contained in each block in a heavy dark line is explained in the blocks that branch off from it. The third level of information is contained in the note blocks (open ended blocks) that branch off the second level blocks. Information in these blocks is intended to explain why an action has been performed.

Timing Charts

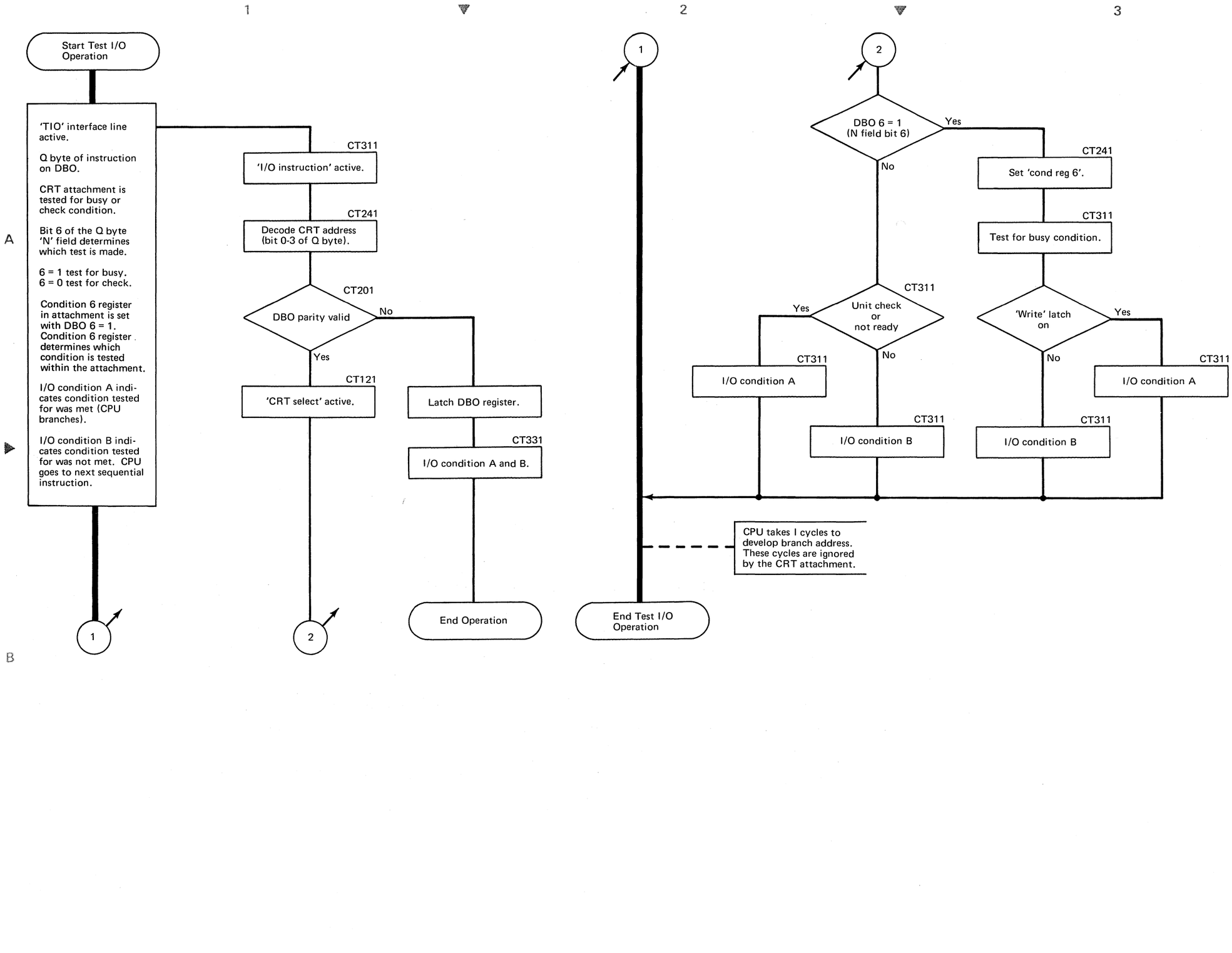
The timing charts in this chapter are to be used to supplement the information found in the flowcharts.

1 ▼ 2 ▼ 3


Start
Load I/O Operation
I Op Cycle
'LIO' interface line active.
A
I/Q Cycle
Q byte of instruction on DBO. Decode device address. Check DBO parity.
CT311
I/O instruction
CT241
Decode CRT address (bit 0-3 of Q byte = 9).
CT201
DBO parity valid
No
Yes
CT201
Latch DBO register.
CT311
I/O condition A and B
End Operation
CT121
'CRT select'
'Write' latch on (busy)
Yes
No
CT321
'Command reject'
CT311
I/O Condition B
CT121
Reset 'CRT select'.
CT311
I/O condition A
End Operation
CPU takes I-H1 (or IX1) and I-L1 cycles to develop effective address. These cycles are ignored by the CRT attachment.
B
1
1
EB 1 Cycle (LSR Lo)
CT331
Select LSR lines 3 & 6 (without LCD), 6 & 7 (with LCD).
EB Not 1 Cycle
LSR (Hi) address on DBO. 'Not 6' and 'not 7' are exclusive OR'ed with DBO lines for set conditions.
A retrace delay is started to provide a time-out for the CRT to restore the CRT beam.
DBO parity valid
No
Yes
Latch DBO register.
CT101
'LIO reset'
'Set LSR address'
CT201
I/O condition A and B
CT211
CT101
CT201
Set 'reset display', 'retrace latch', and 'not 6' and 'not 7'.
End Operation
CT121
Reset:
'CRT select' and 'restore'.
End Operation

			I-Q								EB 1								EB Not 1																	
		Clock	5	6	7	8	0	1	2	3	4	5	6	7	8	0	1	2	3	4	5	6	7	8	0	1	2	3	4	5	6	7	8	0	1	2	3	4	5
No.	Signal Name	Logic	CPU I-H1 or I-L1 Cycles																																		
1	LIO	CT301																																			
2	IQ	CT121																																			
3	EB 1	CT121																																			
4	EB Not 1	CT301																																			
5	CRT Address on DBO	CT241																																			
6	Data Parity	CT121																																			
7	CRT Select	CT311																																			
8	I/O Condition A or B	CT311																																			
9	LSR Select (DBO Lines 3 & 6 or 6 & 7 with LCD)	CT331															(Lo)																				
10	Command Reject (if busy-write latch set)	CT321																																			
11	LIO Reset	CT101																																			
12	Start CRT Timing	CT331																																			
13	Reset Display	CT211																																			
14	Set LSR Addr (See $\overline{6}$, $\overline{7}$ latches if corresponding DBI line active)	CT101																																			
15	Reset $\overline{6}$, $\overline{7}$ latches	CT201																																			

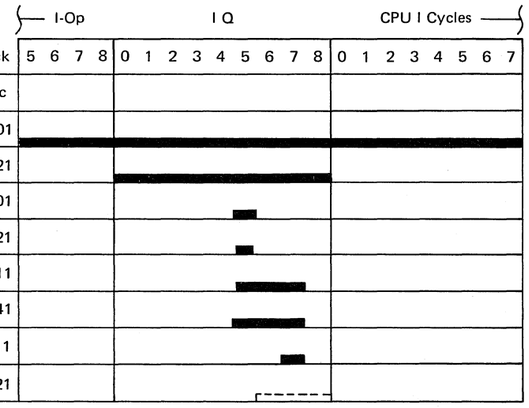
(Hi) — LSR (Hi) — (Hi) — 288 usec delay


1
2
3
A
B
Start Test I/O Operation
'TIO' interface line active.
Q byte of instruction on DBO.
CRT attachment is tested for busy or check condition.
Bit 6 of the Q byte 'N' field determines which test is made.
6 = 1 test for busy.
6 = 0 test for check.
Condition 6 register in attachment is set with DBO 6 = 1. Condition 6 register determines which condition is tested within the attachment.
I/O condition A indicates condition tested for was met (CPU branches).
I/O condition B indicates condition tested for was not met. CPU goes to next sequential instruction.
1
CT311
'I/O instruction' active.
CT241
Decode CRT address (bit 0-3 of Q byte).
CT201
DBO parity valid
No
Yes
CT121
'CRT select' active.
Latch DBO register.
CT331
I/O condition A and B.
End Operation
2
1
2
DBO 6 = 1 (N field bit 6)
Yes
No
CT241
Set 'cond reg 6'.
CT311
Test for busy condition.
CT311
Unit check or not ready
Yes
No
CT311
I/O condition A
CT311
I/O condition B
'Write' latch on
Yes
No
CT311
I/O condition A
CT311
I/O condition B
CPU takes I cycles to develop branch address. These cycles are ignored by the CRT attachment.
End Test I/O Operation

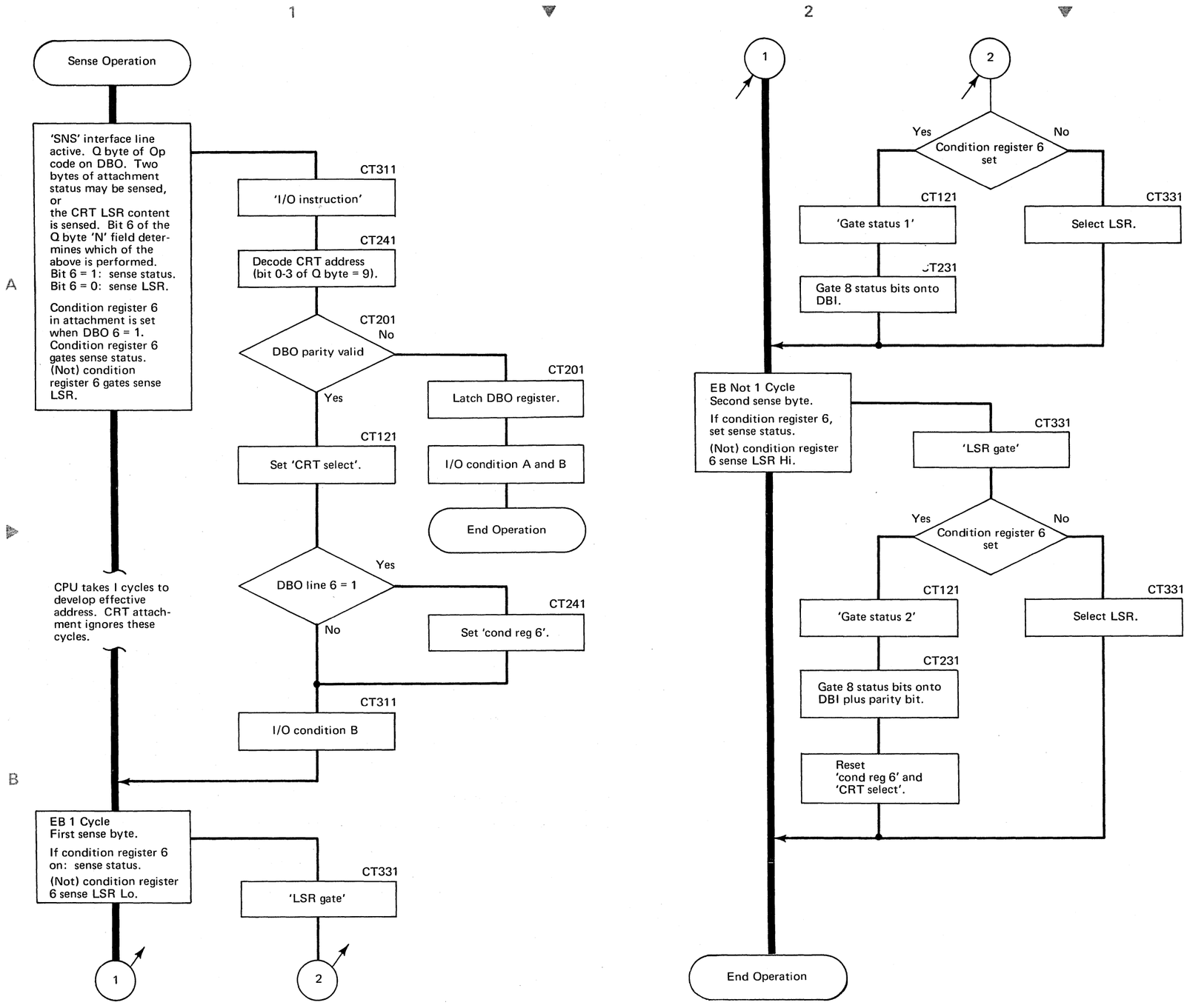
1 2 3

A

No.	Signal Name	Logic
1	TIO	CT301
2	IQ	CT121
3	Data Valid on DBO	CT201
4	Data Parity	CT121
5	CRT Select	CT311
6	Condition Register 6 (if test for busy)	CT241
7	I/O Condition A or B	CT311
8	Command Reject (if parity error)	CT321



B

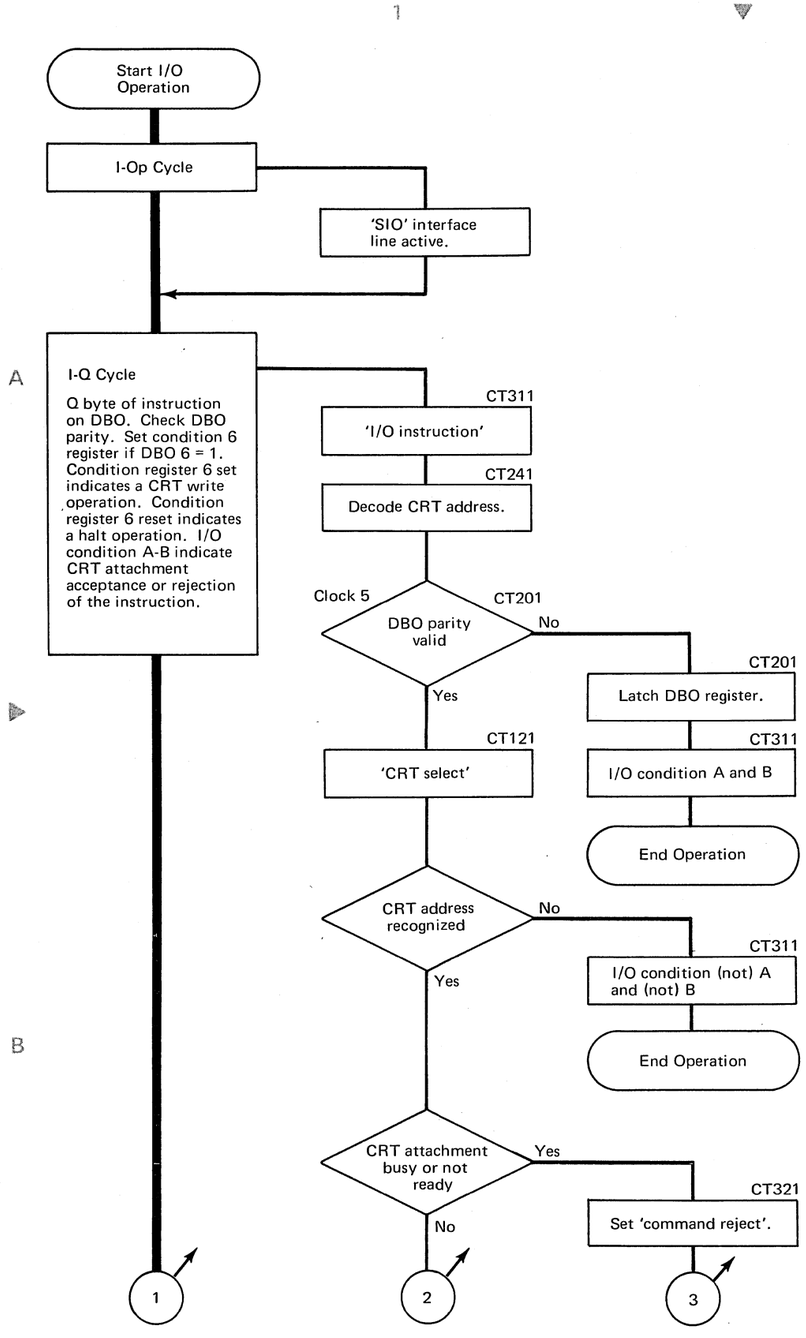

1
2
3
A
B
Sense Operation
'SNS' interface line active. Q byte of Op code on DBO. Two bytes of attachment status may be sensed, or the CRT LSR content is sensed. Bit 6 of the Q byte 'N' field determines which of the above is performed. Bit 6 = 1: sense status. Bit 6 = 0: sense LSR.
Condition register 6 in attachment is set when DBO 6 = 1. Condition register 6 gates sense status. (Not) condition register 6 gates sense LSR.
CPU takes I cycles to develop effective address. CRT attachment ignores these cycles.
CT311
'I/O instruction'
CT241
Decode CRT address (bit 0-3 of Q byte = 9).
CT201
DBO parity valid
No
Yes
CT201
Latch DBO register.
I/O condition A and B
End Operation
CT121
Set 'CRT select'.
Yes
DBO line 6 = 1
No
CT241
Set 'cond reg 6'.
CT311
I/O condition B
EB 1 Cycle
First sense byte.
If condition register 6 on: sense status.
(Not) condition register 6 sense LSR Lo.
CT331
'LSR gate'
1
2
1
2
Yes
Condition register 6 set
No
CT121
'Gate status 1'
CT231
Gate 8 status bits onto DBI.
CT331
Select LSR.
EB Not 1 Cycle
Second sense byte.
If condition register 6, set sense status.
(Not) condition register 6 sense LSR Hi.
CT331
'LSR gate'
Yes
Condition register 6 set
No
CT121
'Gate status 2'
CT231
Gate 8 status bits onto DBI plus parity bit.
Reset 'cond reg 6' and 'CRT select'.
CT331
Select LSR.
End Operation

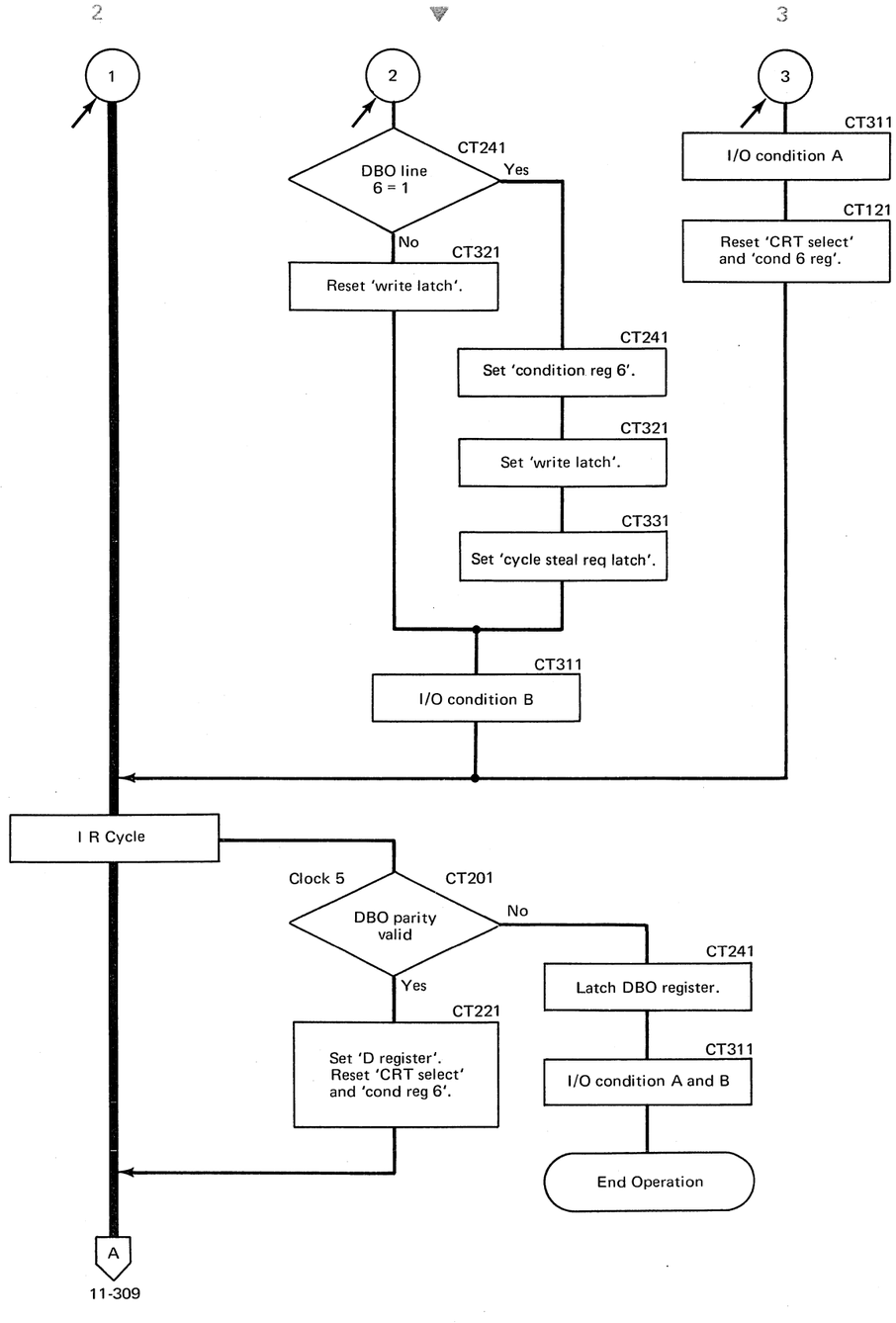
1 2 3

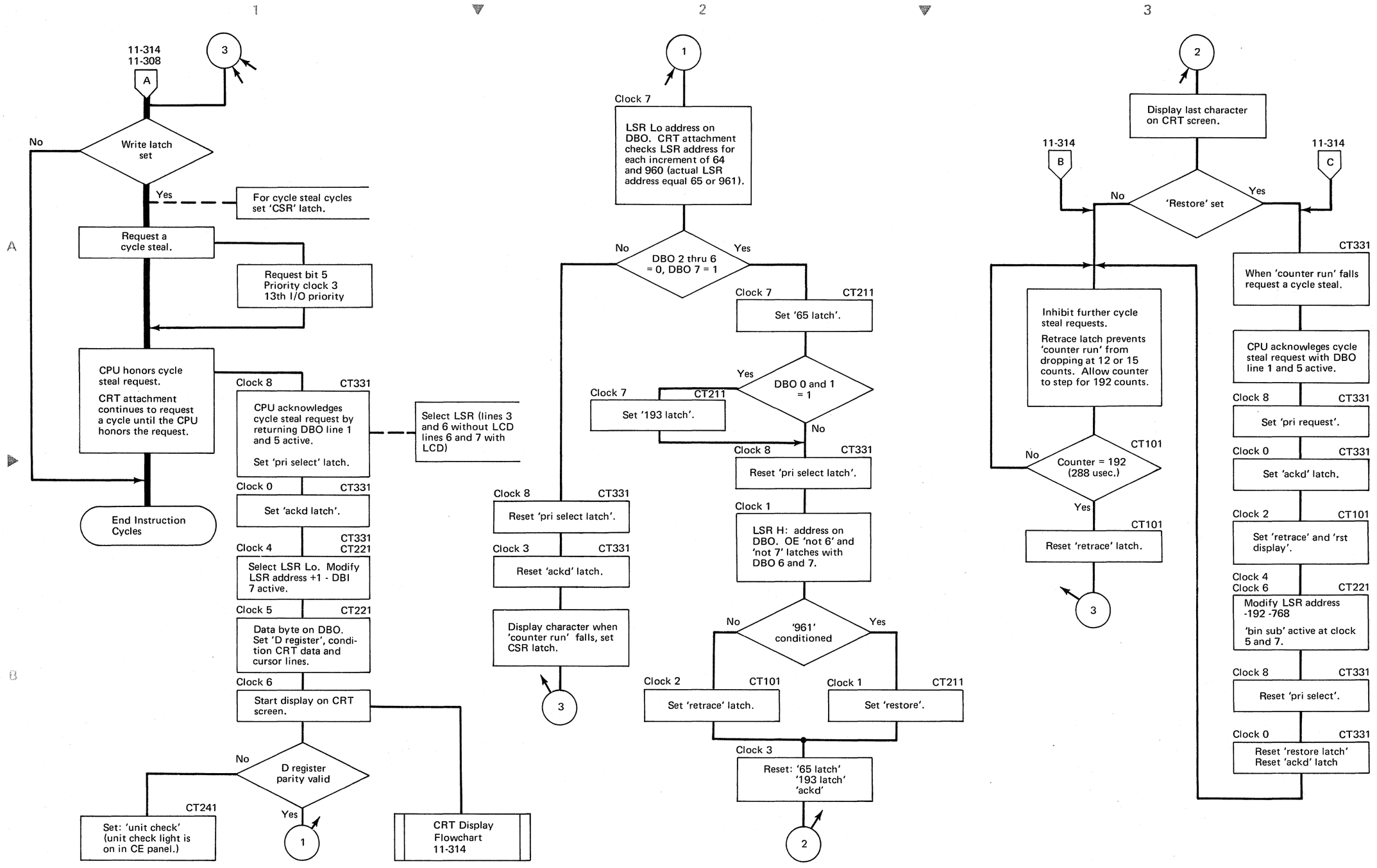
A

No.	Signal Name	Logic	Clock: 5 6 7 8	0 1 2 3 4 5 6 7 8	0 1 2 3 4 5 6 7 8	0 1 2 3 4 5 6 7 8	0 1 2 3 4 5
			I-Op	I Q	EB 1	EB Not 1	
1	SNS	CT301					
2	IQ	CT121					
3	EB 1	CT121					
4	EB 2	CT301					
5	Data Valid on DBO	CT201					
6	Data Parity	CT121					
7	CRT Select	CT311					
8	Condition Register 6 (if sense status)	CT241					
9	I/O Condition A or B	CT311					
10	Command Reject (if parity error)	CT321					
11	LSR Select (if store LSR)	CT331			Lo	Hi	
12	Gate Status Bytes	CT121			Status byte 1	Status byte 2	
13	DBI Register Reset	CT331					
14	DBI Parity Reset	CT201		each phase C			

B


1
Start I/O Operation
I-Op Cycle
'SIO' interface line active.
A
I-Q Cycle
Q byte of instruction on DBO. Check DBO parity. Set condition 6 register if DBO 6 = 1. Condition register 6 set indicates a CRT write operation. Condition register 6 reset indicates a halt operation. I/O condition A-B indicate CRT attachment acceptance or rejection of the instruction.
CT311
'I/O instruction'
CT241
Decode CRT address.
Clock 5
CT201
DBO parity valid
No
Yes
CT201
Latch DBO register.
CT311
I/O condition A and B
End Operation
CT121
'CRT select'
CRT address recognized
No
Yes
CT311
I/O condition (not) A and (not) B
End Operation
B
CRT attachment busy or not ready
Yes
No
CT321
Set 'command reject'.
1
2
3


1
2
3
CT241
DBO line 6 = 1
Yes
No
CT321
Reset 'write latch'.
CT241
Set 'condition reg 6'.
CT321
Set 'write latch'.
CT331
Set 'cycle steal req latch'.
CT311
I/O condition B
CT311
I/O condition A
CT121
Reset 'CRT select' and 'cond 6 reg'.
I R Cycle
Clock 5
CT201
DBO parity valid
No
Yes
CT241
Latch DBO register.
CT311
I/O condition A and B
End Operation
CT221
Set 'D register'. Reset 'CRT select' and 'cond reg 6'.
A
11-309



CRT ATTACHMENT–Operations
Start I/O Instruction Flowchart (Part 2 of 2)

1 2 3

I-Op | IQ | IR | I/O Cycle(s)

Clock: 5 6 7 8 | 0 1 2 3 4 5 6 7 8 | 0 1 2 3 4 5 6 7 8 | 0 1 2 3 4 5 6 7 8 | 0

No.	Signal Name	Logic
1	SIO	CT301
2	IQ	CT121
3	IR	CT301
4	Data Valid on DBO	CT201
5	Sample DBO Parity	CT121
6	CRT Select	CT311
7	Condition Reg 6 (if write op)	CT241
8	I/O Condition A or B	CT311
9	Check Reset	CT301
10	Command Reject (if display (Not) ready or second SIO and 'write' active)	CT321
11	Reset Cond Reg 6	CT241
12	Set Cond Reg 6 (if write op, DBO 6 = 1)	CT241
13	Write Latch (Write Command)	CT321
14	Cycle Steal Request	CT331

A

Select Inactive Here if Command is Rejected.

Drops With Next SIO Command.

Request cycle steal cycle until CPU honors request.

▶ Start I/O Write Operation and First Cycle Steal Request

B

1 2 3

A

No.	Signal Name	Logic	Clock 0 1 2 3 4 5 6 7 8	0 1 2 3 4 5 6 7 8	0 1 2 3 4 5 6 7 8	0 1 2 3 4 5 6 7 8
1	Cycle steal request	CT331				
2	Data on DBO	CT201	Pri assign (DBO 1 & 5)	Data LSR Lo	LSR Hi	
3	Sample DBO	CT121				
4	Pri Select	CT331				
5	Pri Req Ack'd	CT331				
6	LSR Select	CT331				
7	Data on DBI	CT231		P P +1 Lo 0 Hi		
8	Set D Reg.	CT331				
9	Start CRT Timing	CT331				
10	Data Reg to CRT	CT221				
11	Test DBO for Retrace	CT211		(Clock 7)		
12	65 latch (if DBO 2 thru 6 = 0 DBO 7 = 1)	CT201				
13	193 latch (if DBO 0 and 1 each = 1	CT201				
14	Test LSR for Restore (961 Count)	CT201				
15	Restore latch (if Hi plus Lo = 961)	CT211				
16	Retrace latch	CT101				

I/O Cycle - Modify CRTAR Address Plus One

B

1 2 3

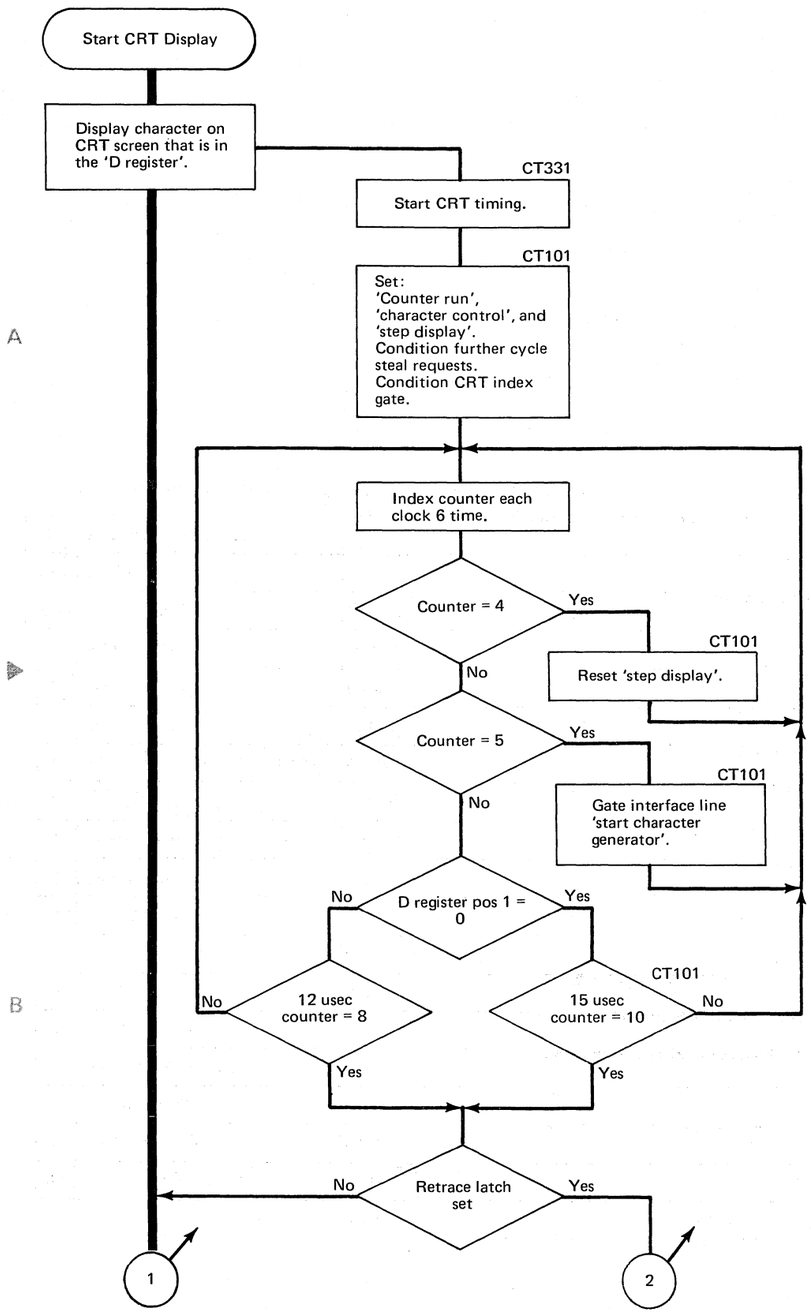
A

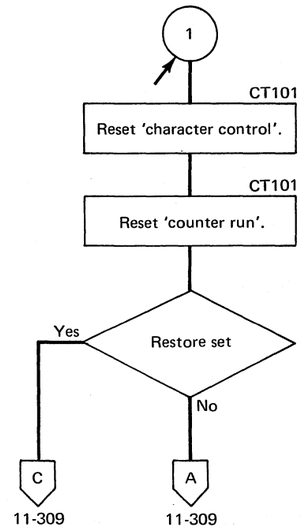
No.	Signal Name	Logic	Clock: 2 3 4 5 6 7 8 | 0 1 2 3 4 5 6 7 8 | 0 1 2 3 4 | 6 7 8 | 0 1 2 3 4 5 6 7 8 | 0 1 2 3 4 5 6 7 8 | 0
			Cycle Steal Request; → A cycle steal request is made during this interval to modify LSR -960.
1	Data Valid on DBO	CT201	Data LSR Lo; LSR Hi; Data LSR Lo; LSR Hi
2	Set 'Pri Select' latch	CT331	
3	Primary Select CRT	CT331	
4	Pri Req Ack'd	CT331	
5	Data on DBI	CT231	P P +1 Lo +0 Hi; P P -192 Lo -768 Hi
6	Set D Reg	CT121	
7	Start CRT Timing	CT331	
8	Data Reg to CRT	CT221	
9	Strobe for 65, 193 latch set	CT301	
10	65 Latch if DBO 7 = 1 and DBO 2 thru 6 = 0	CT201	
11	193 Latch (if DBO 0 & 1 active)	CT201	
12	Strobe for Restore	CT211	
13	Restore Latch	CT211	
14	Retrace Latch	CT101	273 usec to 288 usec
15	Step Display	CT101	
16	Bin Sub	CT211	
17	LSR Select Lines 3 & 7	CT331	

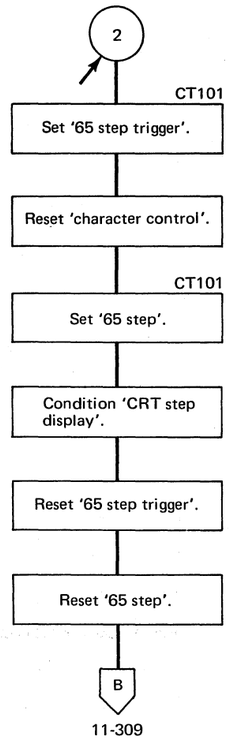
Cycle Steal Request — LSR address = 961 — Subtract 960 from LSR address

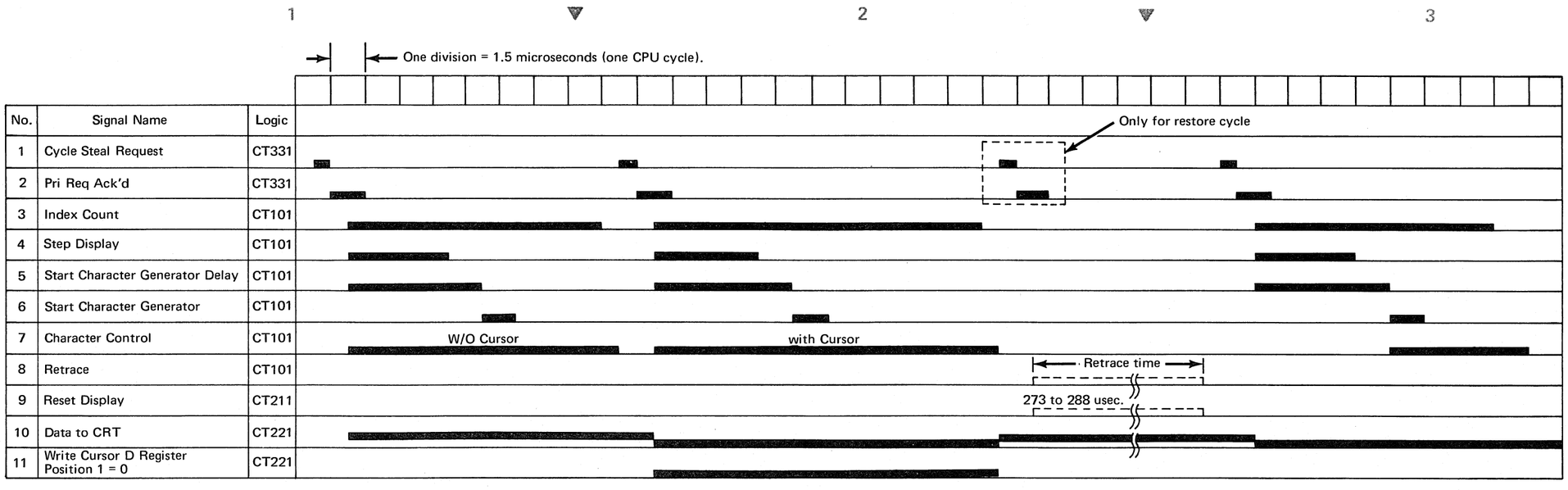
B

1 2 3


Start CRT Display
Display character on CRT screen that is in the 'D register'.
CT331
Start CRT timing.
CT101
Set:
'Counter run',
'character control', and
'step display'.
Condition further cycle steal requests.
Condition CRT index gate.
Index counter each clock 6 time.
Counter = 4
Yes
CT101
Reset 'step display'.
No
Counter = 5
Yes
CT101
Gate interface line 'start character generator'.
No
D register pos 1 = 0
No
Yes
CT101
12 usec counter = 8
No
15 usec counter = 10
No
Yes
Yes
Retrace latch set
No
Yes
1
2


1
CT101
Reset 'character control'.
CT101
Reset 'counter run'.
Restore set
Yes
No
C
11-309
A
11-309


2
CT101
Set '65 step trigger'.
Reset 'character control'.
CT101
Set '65 step'.
Condition 'CRT step display'.
Reset '65 step trigger'.
Reset '65 step'.
B
11-309



No.	Signal Name	Logic
1	Cycle Steal Request	CT331
2	Pri Req Ack'd	CT331
3	Index Count	CT101
4	Step Display	CT101
5	Start Character Generator Delay	CT101
6	Start Character Generator	CT101
7	Character Control	CT101
8	Retrace	CT101
9	Reset Display	CT211
10	Data to CRT	CT221
11	Write Cursor D Register Position 1 = 0	CT221

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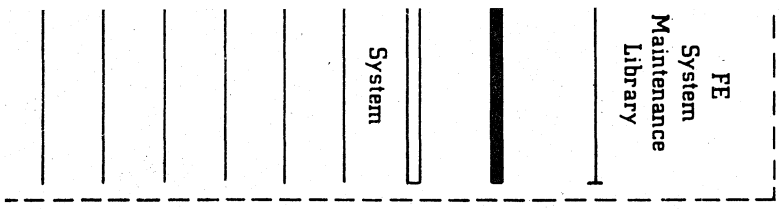

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