PRICE $2.00

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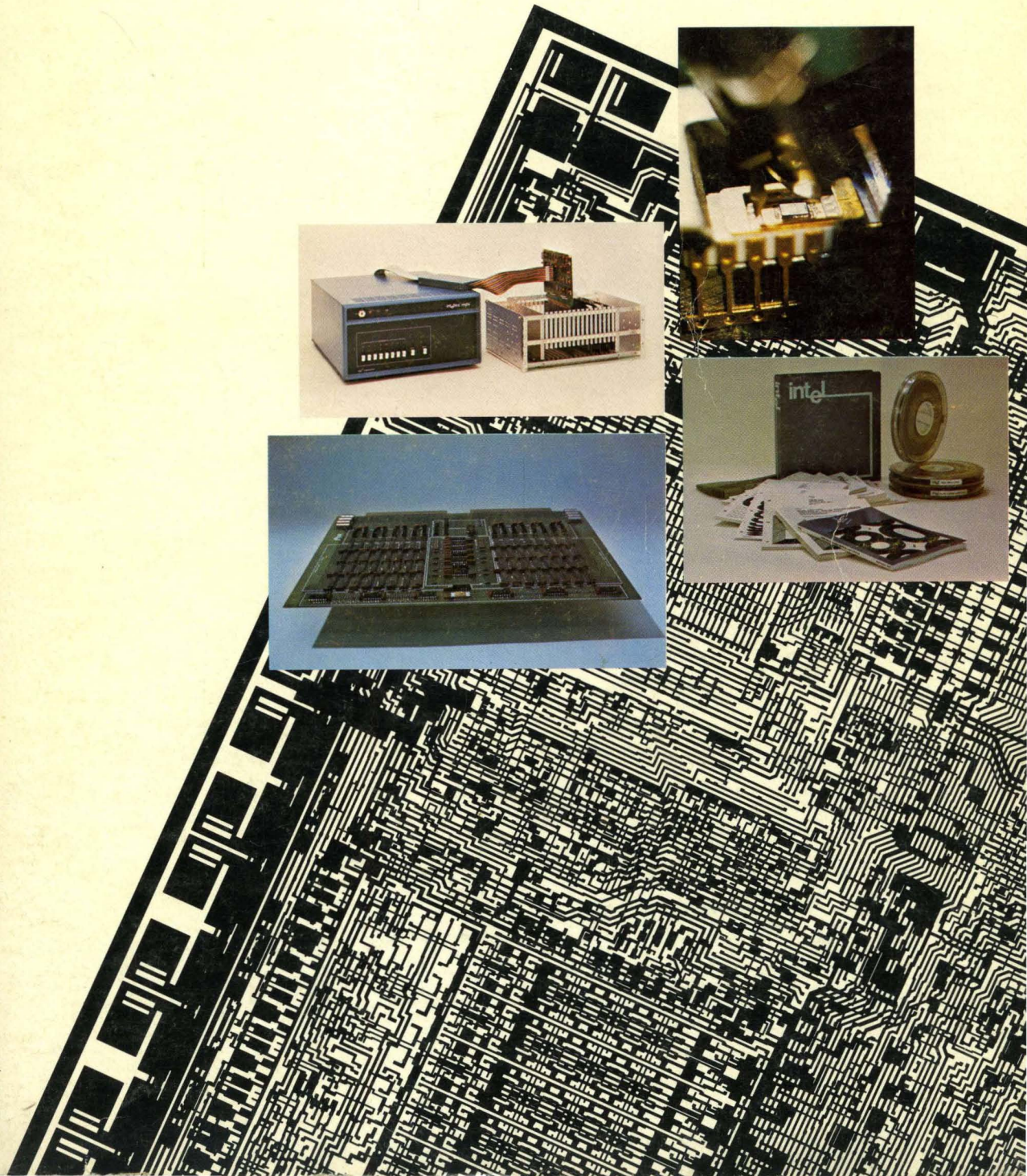
data catalog 1976



INTEL

Intel was organized in 1968 to exploit the rapidly growing technology of Integrated Electronics, from whence the corporation derives its name. During its brief history it has become the world's largest supplier of MOS circuits, and is in the top ten producers of all semiconductor devices. This data catalog covers most Intel standard component, memory system and microcomputer development system products. For a list of other Intel literature, see page 12-10.

On the cover

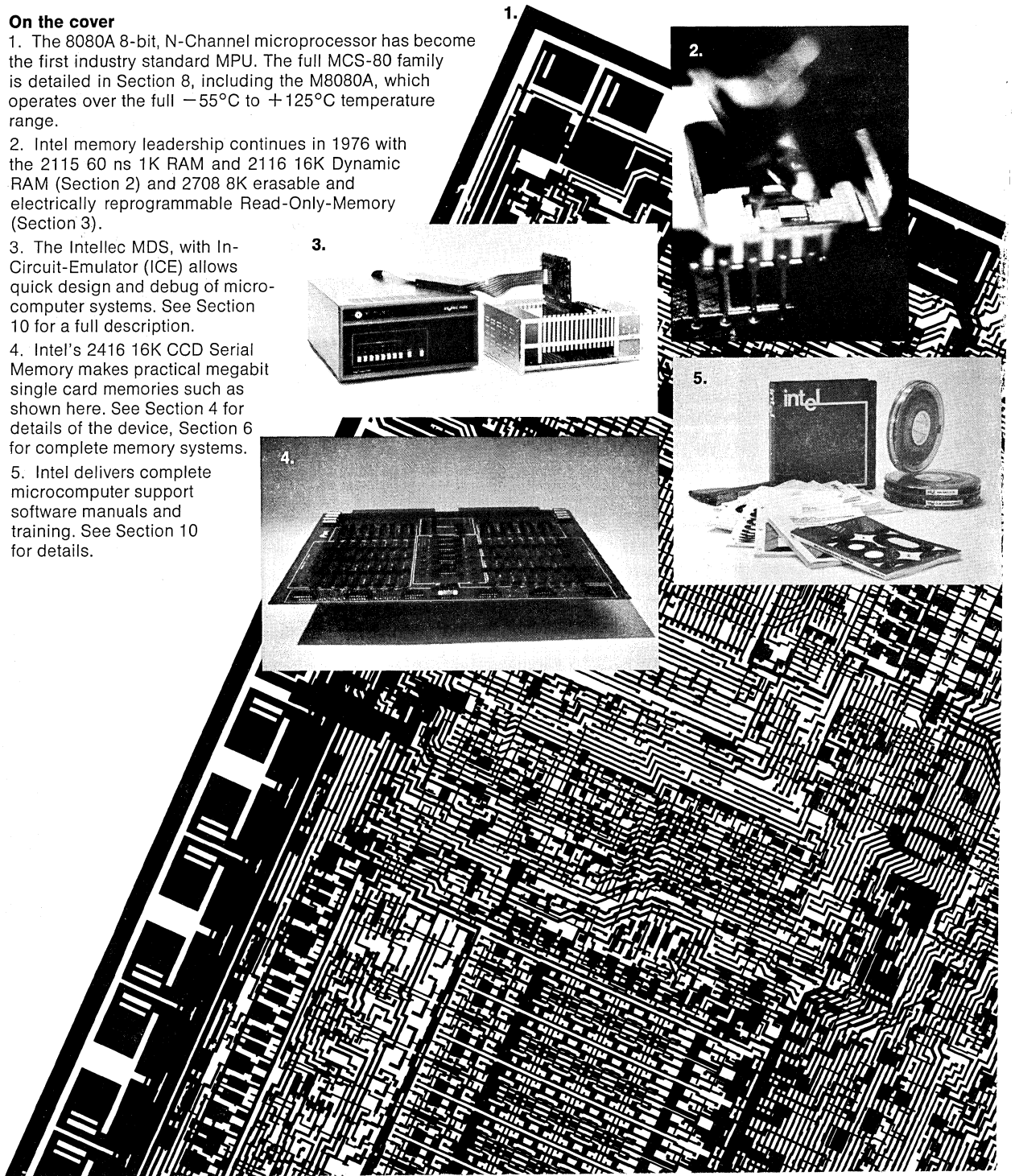
1. The 8080A 8-bit, N-Channel microprocessor has become the first industry standard MPU. The full MCS-80 family is detailed in Section 8, including the M8080A, which operates over the full −55°C to +125°C temperature range.

2. Intel memory leadership continues in 1976 with the 2115 60 ns 1K RAM and 2116 16K Dynamic RAM (Section 2) and 2708 8K erasable and electrically reprogrammable Read-Only-Memory (Section 3).

3. The Intellec MDS, with In-Circuit-Emulator (ICE) allows quick design and debug of micro-computer systems. See Section 10 for a full description.

4. Intel's 2416 16K CCD Serial Memory makes practical megabit single card memories such as shown here. See Section 4 for details of the device, Section 6 for complete memory systems.

5. Intel delivers complete microcomputer support software manuals and training. See Section 10 for details.



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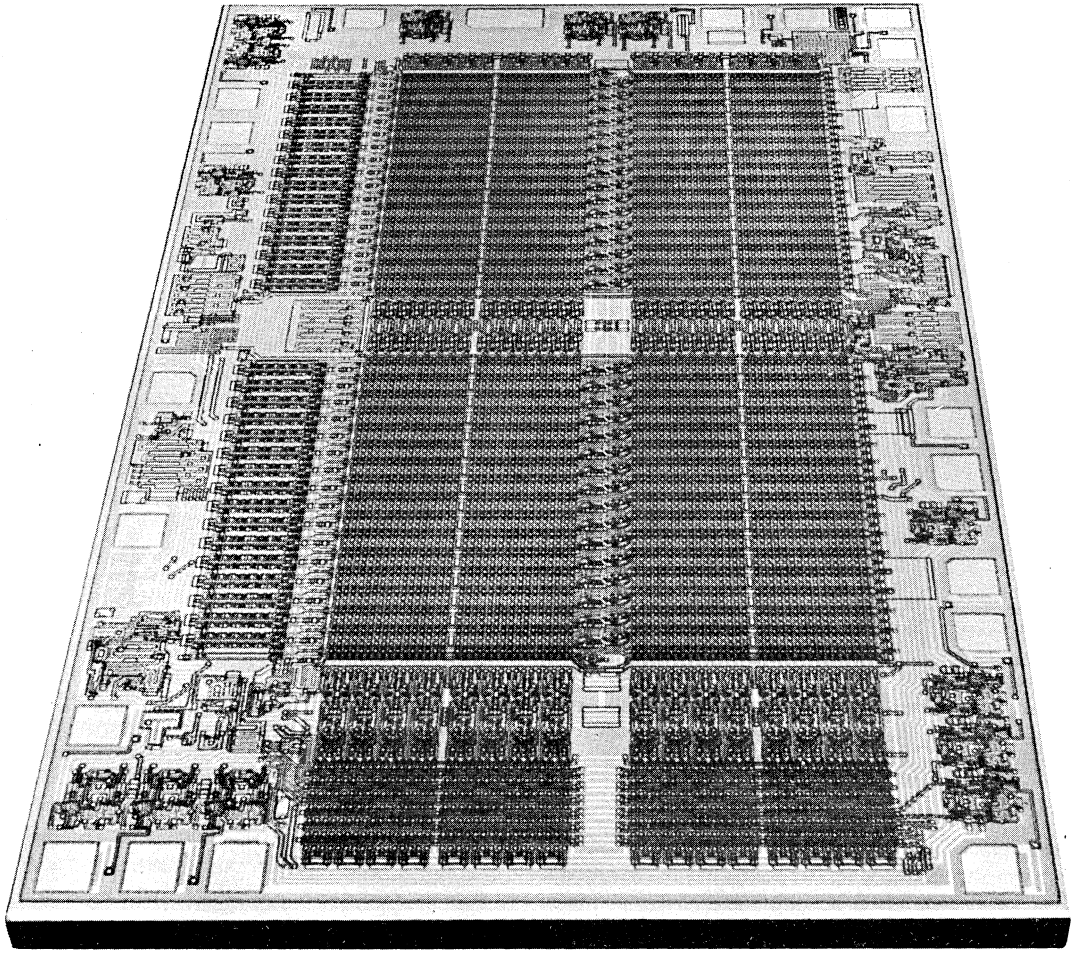
RANDOM ACCESS MEMORIES



RANDOM ACCESS MEMORIES

	Type	No. Of Bits	Description	Organization	Electrical Characteristics Over Temperature				
					Access Time Max.	Cycle Time Max.	Power Dissipation Max.[1] Operating/Standby	Supplies [V]	Page No.
SILICON GATE MOS	1101A	256	Static Fully Decoded	256 x 1	1500ns	1500ns	685mW/340mW	+5,-9	2-4
	1101A1	256	Hi-Speed Static Fully Decoded	256 x 1	1000ns	1000ns	685mW/340mW	+5,-9	2-4
	1103	1024	Dynamic Fully Decoded	1024 x 1	300ns	580ns	400mW/67mW	+16,+19	2-8
	1103-1	1024	Dynamic Fully Decoded	1024 x 1	150ns	340ns	400mW/76mW	+19,+22	2-13
	1103A	1024	Dynamic Fully Decoded	1024 x 1	205ns	580ns	400mW/64mW	+16,+19	2-16
	1103A-1	1024	Dynamic Fully Decoded	1024 x 1	145ns	340ns	625mW/10mW	+19,+22	2-21
	1103A-2	1024	Dynamic Fully Decoded	1024 x 1	145ns	400ns	570mW/10mW	+19,+22	2-26
	2101A	1024	Static, Separate I/O	256 x 4	350ns	350ns	300mW	+5	2-30
	2101A-2	1024	Static, Separate I/O	256 x 4	250ns	250ns	350mW	+5	2-30
	2101A-4	1024	Static, Separate I/O	256 x 4	450ns	450ns	300mW	+5	2-30
	2101	1024	Static, Separate I/O	256 x 4	1000ns	1000ns	350mW	+5	2-34
	2101-1	1024	Static, Separate I/O	256 x 4	500ns	500ns	350mW	+5	2-34
	2101-2	1024	Static, Separate I/O	256 x 4	650ns	650ns	350mW	+5	2-34
	2102A	1024	High Speed Static	1024 x 1	350ns	350ns	275mW	+5	2-38
	2102A-2	1024	High Speed Static	1024 x 1	250ns	250ns	325mW	+5	2-38
	2102A-4	1024	High Speed Static	1024 x 1	450ns	450ns	275mW	+5	2-38
	2102A-6	1024	High Speed Static	1024 x 1	650ns	650ns	275mW	+5	2-38
	2102AL	1024	Low Standby Power Static	1024 x 1	350ns	350ns	165mW/35mW	+5	2-38
	2102AL-2	1024	Low Standby Power Static	1024 x 1	250ns	250ns	325mW/42mW	+5	2-38
	2102AL-4	1024	Low Standby Power Static	1024 x 1	450ns	450ns	165mW/35mW	+5	2-38
	M2102A-4	1024	Static, T_A = -55°C to +125C	1024 x 1	450ns	450ns	350mW	+5	2-42
	M2102A-6	1024	Static, T_A = -55°C to +125C	1024 x 1	650ns	650ns	350mW	+5	2-42
	2104	4096	16 Pin Dynamic	4096 x 1	350ns	500ns	744mW/37mW	+12,+5,-5	2-44
	2104-2	4096	16 Pin Dynamic	4096 x 1	250ns	375ns	744mW/37mW	+12,+5,-5	2-44
	2104-4	4096	16 Pin Dynamic	4096 x 1	300ns	425ns	756mW/36mW	+12,+5,-5	2-44
	2107A	4096	22 Pin Dynamic	4096 x 1	300ns	700ns	458mW/10mW	+12,+5,-5	2-52
	2107A-1	4096	22 Pin Dynamic	4096 x 1	280ns	550ns	516mW/16mW	+12,+5,-5	2-52
	2107A-4	4096	22 Pin Dynamic	4096 x 1	350ns	840ns	405mW/10mW	+12,+5,-5	2-52
	2107A-5	4096	22 Pin Dynamic	4096 x 1	420ns	970ns	376mW/11mW	+12,+5,-5	2-52
	2107B	4096	22 Pin Dynamic	4096 x 1	200ns	400ns	648mW/12mW	+12,+5,-5	2-58
	2107B-4	4096	22 Pin Dynamic	4096 x 1	270ns	470ns	648mW/13mW	+12,+5,-5	2-58
	2107B-6	4096	22 Pin Dynamic	4096 x 1	350ns	800ns	840mW/25mW	+12,+5,-5	2-58

Note 1: Power Dissipation calculated with maximum power supply current and nominal supply voltages.

RANDOM ACCESS MEMORIES (CONTINUED)

	Type	No. Of Bits	Description	Organization	Electrical Characteristics Over Temperature				
					Access Time Max.	Cycle Time Max.	Power Dissipation Max.[1] Operating/Standby	Supplies [V]	Page No.
SILICON GATE MOS	2111A	1024	Static, Common I/O with Output Deselect	256 x 4	350ns	350ns	300mW	+5	2-64
	2111A-2	1024	Static, Common I/O with Output Deselect	256 x 4	250ns	250ns	350mW	+5	2-64
	2111A-4	1024	Static, Common I/O with Output Deselect	256 x 4	450ns	450ns	300mW	+5	2-64
	2111	1024	Static, Common I/O with Output Deselect	256 x 4	1000ns	1000ns	350mW	+5	2-68
	2111-1	1024	Static, Common I/O with Output Deselect	256 x 4	500ns	500ns	350mW	+5	2-68
	2111-2	1024	Static, Common I/O with Output Deselect	256 x 4	650ns	650ns	350mW	+5	2-68
	2112A	1024	Static, Common I/O without Output Deselect	256 x 4	350ns	350ns	300mW	+5	2-72
	2112A-2	1024	Static, Common I/O without Output Deselect	256 x 4	250ns	250ns	350mW	+5	2-72
	2112A-4	1024	Static, Common I/O without Output Deselect	256 x 4	450ns	450ns	300mW	+5	2-72
	2112	1024	Static, Common I/O without Output Deselect	256 x 4	1000ns	1000ns	350mW	+5	2-77
	2112-2	1024	Static, Common I/O without Output Deselect	256 x 4	650ns	650ns	350mW	+5	2-77
	2115	1024	Open Collector Static	1024 x 1	95ns	95ns	525mW	+5	2-81
	2115-2	1024	Open Collector Static	1024 x 1	70ns	70ns	625mW	+5	2-81
	2115L	1024	Low Power Static	1024 x 1	95ns	95ns	325mW	+5	2-81
	2116	16384	16K Dynamic	16K x 1	250ns	375ns	900mW/24mW	+12,+5,	2-86
	2125	1024	Three-State Static	1024 x 1	95ns	95ns	525mW	+5	2-81
	2125-2	1024	Three-State Static	1024 x 1	70ns	70ns	625mW	+5	2-81
	2125L	1024	Low Power Static	1024 x 1	95ns	95ns	325mW	+5	2-81
SCHOTTKY BIPOLAR	3101	64	Fully Decoded	16 x 4	60ns	60ns	525mW	+5	2-87
	3101A	64	High Speed Fully Decoded	16 x 4	35ns	35ns	525mW	+5	2-87
	M3101	64	Fully Decoded (-55°C to +125°C)	16 x 4	75ns	75ns	546mW	+5	2-91
	M3101A	64	High Speed Fully Decoded (-55°C to +125°C)	16 x 4	45ns	45ns	546mW	+5	2-91
	3104	16	Content Addressable Memory	4 x 4	30ns	40ns	625mW	+5	2-93
	3106	256	High Speed Fully Decoded (With Three-State Output)	256 x 1	80ns	80ns	650mW	+5	2-97
	3106A	256	High Speed Fully Decoded (With Three-State Output)	256 x 1	60ns	70ns	650mW	+5	2-97
	3106-8	256	High Speed Fully Decoded (With Three-State Output)	256 x 1	80ns	80ns	650mW	+5	2-97
	3107	256	High Speed Fully Decoded (With Open Collector Output)	256 x 1	80ns	80ns	650mW	+5	2-97
	3107A	256	High Speed Fuly Decoded (With Open Collector Output)	256 x 1	60ns	70ns	650mW	+5	2-97
	3107-8	256	High Speed Fully Decoded (With Open Collector Output)	256 x 1	60ns	70ns	650mW	+5	2-97
SIICON GATE CMOS	5101	1024	Static CMOS RAM	256 x 4	650ns	650ns	135mW/75uW	+5	2-101
	5101-1	1024	Static CMOS RAM	256 x 4	450ns	450ns	135mW/75uW	+5	2-101
	5101-3	1024	Static CMOS RAM	256 x 4	650ns	650ns	135mW/1mW	+5	2-101
	5101-8	1024	Static CMOS RAM	256 x 4	800ns	800ns	150mW/2.5mW	+5	2-101
	5101L	1024	Static CMOS RAM	256 x 4	650ns	650ns	135mW/30uW	+5	2-101
	5101L-1	1024	Static CMOS RAM	256 x 4	450ns	450ns	135mW/30uW	+5	2-101
	5101L-3	1024	Static CMOS RAM	256 x 4	650ns	650ns	135mW/400uW	+5	2-101

Note 1: Power Dissipation calculated with maximum power supply current and nominal supply voltages.

1101A, 1101A1

256 BIT FULLY DECODED RANDOM ACCESS MEMORY

- **Access Time -- Typically Below 650 nsec - 1101A1, 850 nsec - 1101A**
- **Low Power Standby Mode**
- **Low Power Dissipation -- Typically less than 1.5 mW/bit during access**
- **Directly DTL and TTL Compatible**
- **Three-state Output -- OR-tie Capability**
- **Simple Memory Expansion -- Chip Select Input Lead**
- **Fully Decoded --On Chip Address Decode and Sense**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration**

The 1101A is an improved version of the 1101 which requires only two power supplies (+5V and −9V) for operation. The 1101A is a direct pin for pin replacement for the 1101.

The Intel® 1101A is a 256 word by 1 bit random access memory element using normally off P-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks to operate.

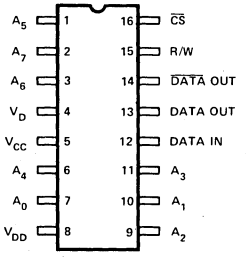
The 1101A is designed primarily for small buffer storage applications where high performance, low cost, and ease of interfacing with other standard logic circuits are important design objectives. The unit will directly interface with standard bipolar integrated logic circuits (TTL, DTL, etc.) The data output buffers are capable of driving TTL loads **directly**. A separate chip select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

For applications requiring a faster access time we recommend the 1101A1 which is a selection from the 1101A and has a guaranteed maximum access time of 1.0 μsec.

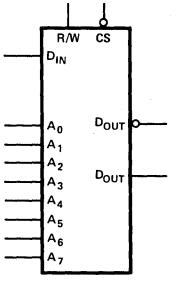
The Intel 1101A is fabricated with **silicon gate technology**. This **low threshold** technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's **silicon gate technology** also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



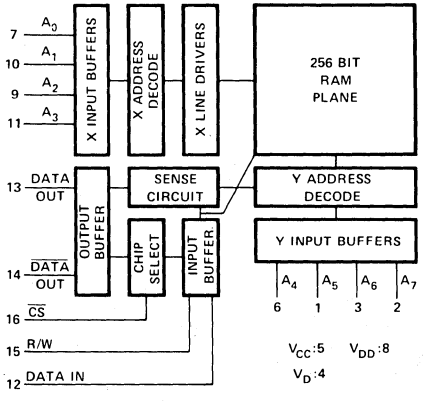
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	$\overline{CS}$	CHIP SELECT
A_0–A_7	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT		

BLOCK DIAGRAM



Absolute Maximum Ratings[1]

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.5V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	−20V
Power Dissipation	1 WATT

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = −9V ± 5%, V_D = −9V ± 5%, unless otherwise specified

SYMBOL	TEST	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)		<1.0	500	nA	V_{IN} = 0.0 V
I_{LO}	OUTPUT LEAKAGE CURRENT		<1.0	500	nA	V_{OUT} = 0.0 V, $\overline{CS}$ = V_{CC} −2
I_{DD1}	POWER SUPPLY CURRENT, V_{DD}		13	19	mA	T_A = 25°C
I_{DD2}	POWER SUPPLY CURRENT, V_{DD}			25	mA	T_A = 0°C
I_{D1}	POWER SUPPLY CURRENT, V_D		12	18	mA	T_A = 25°C,
I_{D2}	POWER SUPPLY CURRENT, V_D			24	mA	T_A = 0°C,
						Continuous Operation I_{OL} = 0.0 mA
V_{IL}	**INPUT "LOW" VOLTAGE**	−10		V_{CC}−4.5	V	
V_{IH}[3]	**INPUT "HIGH" VOLTAGE**	V_{CC}−2		V_{CC}+0.3	V	
I_{OLI}	OUTPUT SINK CURRENT	3.0	8		mA	V_{OUT} = +0.45 V, T_A = +25°C
I_{OL2}	OUTPUT SINK CURRENT	2.0			mA	V_{OUT} = +0.45 V, T_A = +70°C
I_{CF}	OUTPUT CLAMP CURRENT		6	13	mA	V_{OUT} = −1.0 V
I_{OHI}	OUTPUT SOURCE CURRENT	−3.0	−8		mA	V_{OUT} = 0.0 V, T_A = +25°C
I_{OH2}	OUTPUT SOURCE CURRENT	−2.0	−7		mA	V_{OUT} = 0.0 V, T_A = +70°C
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	I_{OL} = 2.0 mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	+3.5	+4.9		V	I_{OH} = −100μA
C_{IN}[4]	INPUT CAPACITANCE (ALL INPUT PINS)		7	10	pF	V_{IN} = V_{CC}
C_{OUT}[4]	OUTPUT CAPACITANCE		7	10	pF	V_{OUT} = V_{CC}
C_V[4]	V_D POWER SUPPLY CAPACITANCE		20	35	pF	V_D = V_{CC}
						f = 1 MHz, T_A = 25°C

Note 1: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are at nominal voltages and T_A = 25°C.

Note 3: A TTL driving the 1101A, 1101A1 must have its output high ≥ V_{CC}−2 even if it is loaded by other bipolar gates.

Note 4: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_D = −9V ± 5%, V_{DD} = −9V ± 5%

READ CYCLE

SYMBOL	TEST		MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle	1101A	1.5			µsec
		1101A1	1.0			µsec
t_{AC}	Address to Chip Select Delay	1101A			1.2(1)	µsec
		1101A1			0.7(1)	µsec
t_A	Access Time	1101A		0.85	1.5	µsec
		1101A1		0.65	1.0	µsec
t_{OH}	Previous Read Data Valid		0.05			µsec

WRITE CYCLE

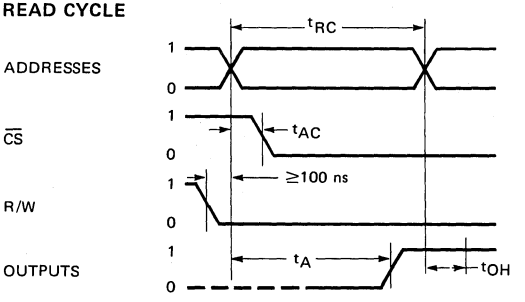
t_{WC}	Write Cycle	0.8			µsec
t_{WD}	Address to Write Pulse Delay	0.3			µsec
t_{WP}	Write Pulse Width	0.4			µsec
t_{DW}	Data Set up Time	0.3			µsec
t_{DH}	Data Hold Time	0.1			µsec

CHIP SELECT AND DESELECT

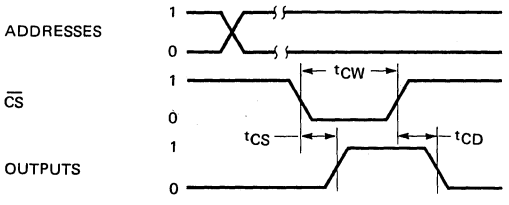
t_{CW}	Chip Select Pulse Width	0.4			µsec
t_{CS}	Access Time Through Chip Select Input		0.2	0.3	µsec
t_{CD}	Chip Deselect Time		0.1	0.3	µsec

CONDITIONS OF TEST:
Input pulse amplitudes: 0 to 5V, Input pulse rise and fall time: 10 nsec. Speed measurements referenced to 1.5V levels (unless otherwise noted). Output load is 1 TTL gate and C_L = 20 pF; measurements made at output of TTL gate ($t_{PD} \leq 10$ nsec)

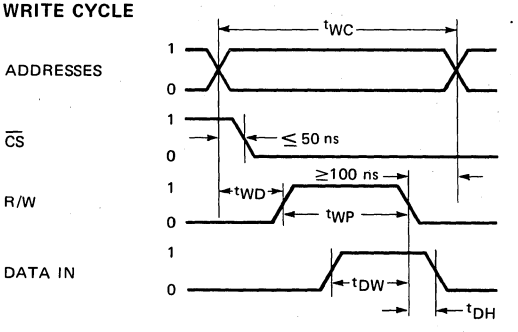
READ CYCLE



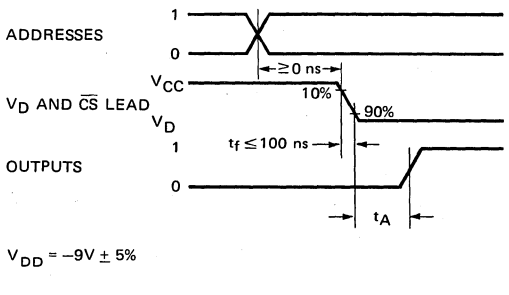
CHIP SELECT AND DESELECT



WRITE CYCLE



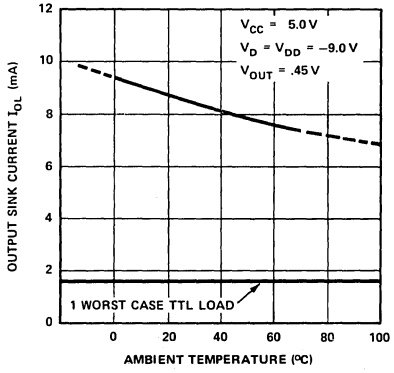
POWER SWITCHING OF V_D



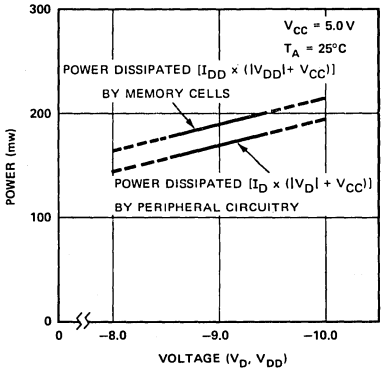
Note 1: Maximum value for t_{AC} measured at minimum read cycle.

Typical D. C. Characteristics

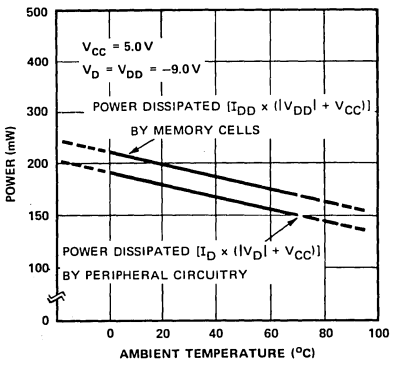
OUTPUT SINK CURRENT VS TEMPERATURE



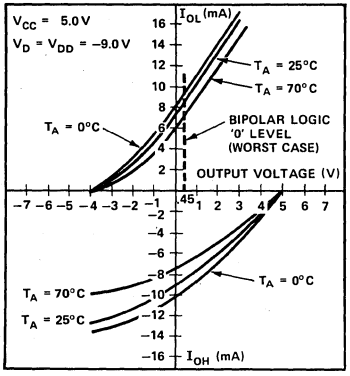
POWER DISSIPATION VS VOLTAGE



POWER DISSIPATION VS TEMPERATURE

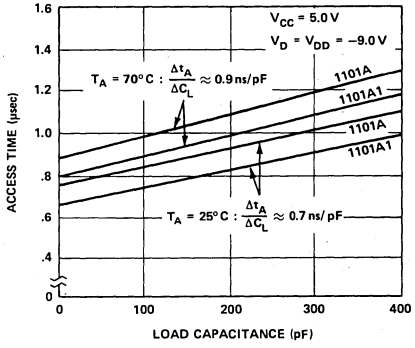


OUTPUT CURRENT VS OUTPUT VOLTAGE

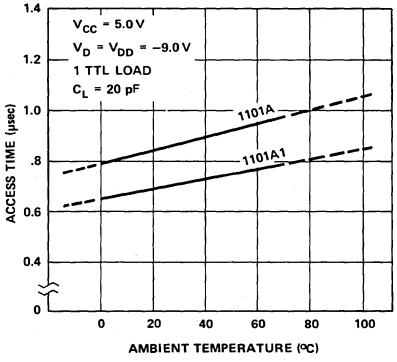


Typical A. C. Characteristics

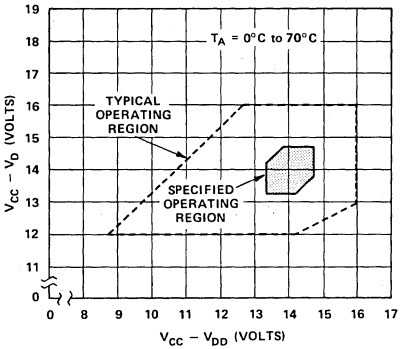
ACCESS TIME VS.
LOAD CAPACITANCE



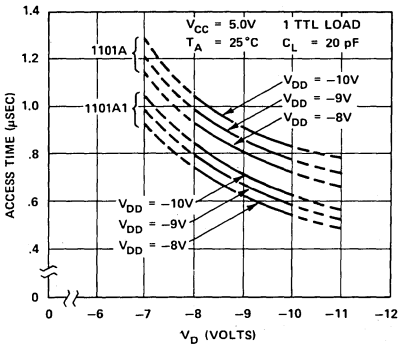
ACCESS TIME VS.
TEMPERATURE



1101A/1101A1
OPERATING REGION



ACCESS TIME VS.
SUPPLY VOLTAGE



FULLY DECODED RANDOM ACCESS 1024 BIT DYNAMIC MEMORY

- **Low Power Dissipation — Dissipates Power Primarily on Selected Chips**
- **Access Time — 300 nsec**
- **Cycle Time — 580 nsec**
- **Refresh Period... 2 milliseconds for 0—70° C Ambient**
- **OR-Tie Capability**
- **Simple Memory Expansion — Chip Enable Input Lead**
- **Fully Decoded—on Chip Address Decode**
- **Inputs Protected—All Inputs Have Protection Against Static Charge**
- **Ceramic and Plastic Package -- 18 Pin Dual In-Line Configuration.**

The Intel®1103 is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

It is a 1024 word by 1 bit random access memory element using normally off *P*-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18 pin dual in-line package. It uses dynamic circuitry and primarily dissipates power only during precharge.

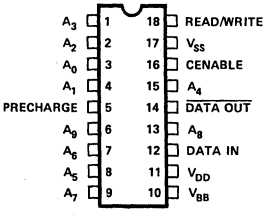
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds.

A separate **cenable** (chip enable) lead allows easy selection of an individual package when outputs are OR-tied.

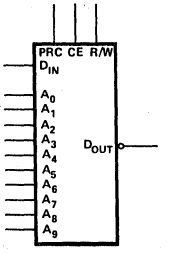
The Intel 1103 is fabricated with **silicon gate technology.** This **low threshold** technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

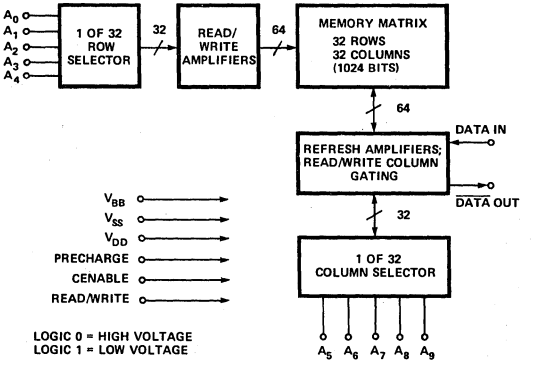
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	PRC	PRECHARGE INPUT
A_0–A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	D_{OUT}	DATA OUTPUT

Maximum Guaranteed Ratings*

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to 0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Power Dissipation	1.0 W

*COMMENT:

Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to +70°C, $V_{SS}^{(1)}$ = 16V ± 5%, $(V_{BB} - V_{SS})^{(6)}$ = 3V to 4V, V_{DD} = 0V unless otherwise specified

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)			1	μA	V_{IN} = 0V
I_{LO}	OUTPUT LEAKAGE CURRENT			1	μA	V_{OUT} = 0V
I_{BB}	**V_{BB} SUPPLY CURRENT**			100	μA	
$I_{DD1}^{(2)}$	SUPPLY CURRENT DURING T_{PC}		37	56	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = V_{SS}; T_A = 25°C
$I_{DD2}^{(2)}$	SUPPLY CURRENT DURING T_{OV}		38	59	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = 0V; T_A = 25°C
$I_{DD3}^{(2)}$	SUPPLY CURRENT DURING T_{POV}		5.5	11	mA	PRECHARGE = V_{SS} CENABLE = 0V; T_A = 25°C
$I_{DD4}^{(2)}$	SUPPLY CURRENT DURING T_{CP}		3	4	mA	PRECHARGE = V_{SS} CENABLE = V_{SS}; T_A = 25°C
$I_{DD}^{(5)}{}_{AV}$	**AVERAGE SUPPLY CURRENT**		**17**	**25**	**mA**	**CYCLE TIME = 580 ns; PRECHARGE WIDTH = 190 ns; T_A = 25°C**
$V_{IL1}^{(7)}$	INPUT LOW VOLTAGE (ALL ADDRESS & DATA-IN LINES)	V_{SS}−17		V_{SS}−14.2	V	T_A = 0°C
$V_{IL2}^{(7)}$	INPUT LOW VOLTAGE (ALL ADDRESS & DATA-IN LINES)	V_{SS}−17		V_{SS}−14.5	V	T_A = 70°C
$V_{IL3}^{(7,8)}$	INPUT LOW VOLTAGE (PRECHARGE CENABLE & READ/WRITE INPUTS)	V_{SS}−17		V_{SS}−14.7	V	T_A = 0°C
$V_{IL4}^{(7,8)}$	INPUT LOW VOLTAGE (PRECHARGE CENABLE& READ/WRITE INPUTS)	V_{SS}−17		V_{SS}−15.0	V	T_A = 70°C
$V_{IH1}^{(7)}$	INPUT HIGH VOLTAGE (ALL INPUTS)	V_{SS}−1		V_{SS}+1	V	T_A = 0°C
$V_{IH2}^{(7)}$	INPUT HIGH VOLTAGE (ALL INPUTS)	V_{SS}−0.7		V_{SS}+1	V	T_A = 70°C
I_{OH1}	**OUTPUT HIGH CURRENT**	**600**	**900**	**4000**	μA	T_A = 25°C
I_{OH2}	**OUTPUT HIGH CURRENT**	**500**	**800**	**4000**	μA	T_A = 70°C
I_{OL}	OUTPUT LOW CURRENT	See Note 3				R_{LOAD} = 100 Ω (4)
V_{OH1}	OUTPUT HIGH VOLTAGE	60	90	400	mV	T_A = 25°C,
V_{OH2}	OUTPUT HIGH VOLTAGE	50	80	400	mV	T_A = 70°C,
V_{OL}	OUTPUT LOW VOLTAGE	See Note 3				

Note 1: The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.

Note 2: See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.

Note 3: The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.

Note 4: This value of load resistance is used for measurement purposes. In applications the resistance may range from 100 Ω to 1 kΩ.

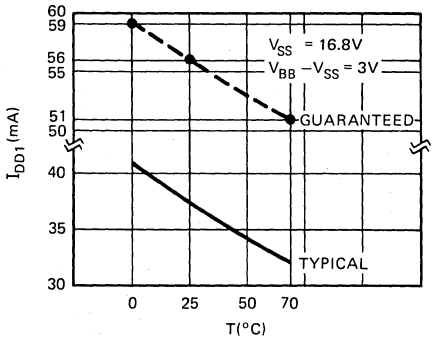
Note 5: This parameter is periodically sampled and is not 100% tested.

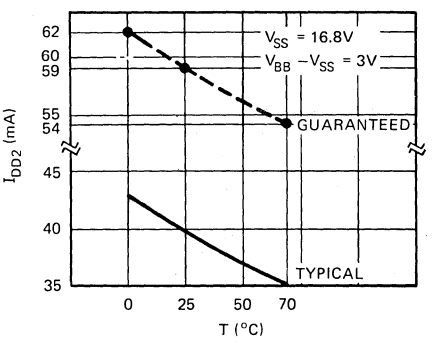
Note 6: $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.

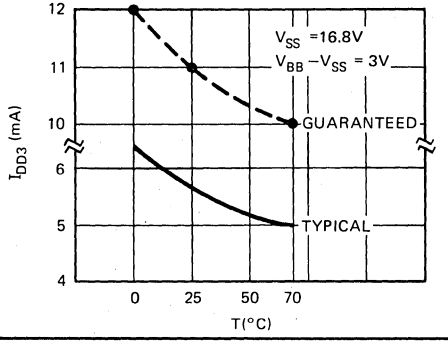
Note 7: The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value in between 0°C and 70°C can be calculated by using a straight-line relationship.

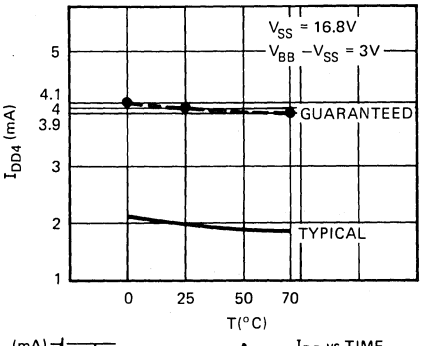
Note 8: The maximum values for V_{IL} (for precharge, cenable & read/write) may be increased to V_{SS}−14.2 @ 0°C and V_{SS}−14.5 @ 70°C (same values as those specified for the address & data-in lines) with a 40ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.

Supply Current vs Temperature

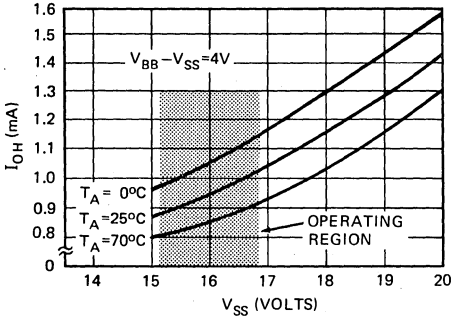


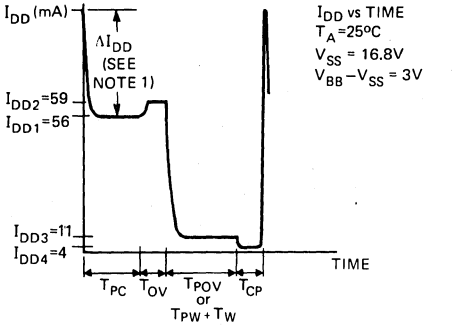






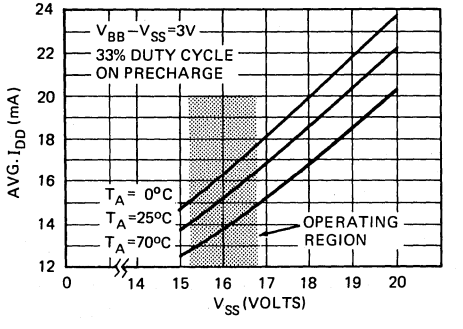
Typical Characteristics

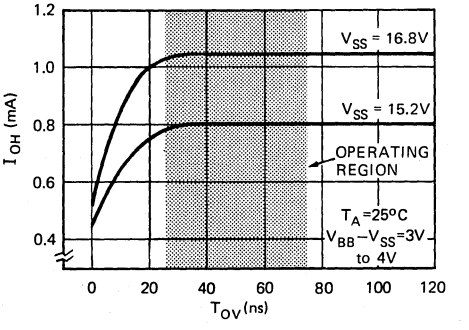




Note 1. ΔI_{DD} is due to charging of internal device node capacitance at precharge

Note 2. These values are taken from a single pulse measurement





AC Characteristics T_A = 0°C to 70°C, V_{SS} = 16 ± 5%, (V_{BB} − V_{SS}) = 3.0V to 4.0V, V_{DD} = 0V

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	**TIME BETWEEN REFRESH**			**2**	**ms**	
t_{AC} (1)	ADDRESS TO CENABLE SET UP TIME	115			ns	
t_{CA}	CENABLE TO ADDRESS HOLD TIME	20			ns	
t_{PC} (1)	PRECHARGE TO CENABLE DELAY	125			ns	
t_{CP}	CENABLE TO PRECHARGE DELAY	85			ns	
t_{OV}	PRECHARGE & CENABLE OVERLAP, LOW	25		75	ns	t_T = 20ns
t_{OVH}	PRECHARGE & CENABLE OVERLAP, HIGH			140	ns	t_T = 20ns
t_{OVM}	PRECHARGE & CENABLE OVERLAP, 50% POINTS	45		95	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC} (1)	**READ CYCLE**	**480**			**ns**	
t_{PCV}	PRECHARGE TO END OF CENABLE	165		500	ns	
t_{PO}	END OF PRECHARGE TO OUTPUT DELAY			120	ns	
t_{ACC1} (1)	**ADDRESS TO OUTPUT ACCESS**	**300**			**ns**	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$; t_T = 20 ns, C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV
t_{ACC2} (1)	**PRECHARGE TO OUTPUT ACCESS**	**310**			**ns**	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$; t_T = 20 ns, C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC} (1)	**WRITE CYCLE**	**580**			**ns**	t_T = 20 ns
t_{RWC} (1)	**READ/WRITE CYCLE**	**580**			**ns**	t_T = 20 ns
t_{PW}	PRECHARGE TO READ/WRITE DELAY	165		500	ns	
t_{WP}	READ/WRITE PULSE WIDTH	50			ns	
t_W	READ/WRITE SET UP TIME	80			ns	
t_{DW}	DATA SET UP TIME	105			ns	
t_{DH}	DATA HOLD TIME	10			ns	
t_{PO}	END OF PRECHARGE TO OUTPUT DELAY			120	ns	C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV
t_{CW}	RELATIONSHIP BETWEEN CENABLE AND READ/WRITE			0	ns	C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV

Note 1: These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS}−14.2V @ 0°C and V_{SS}−14.5V @ 70°C as defined on page 2.

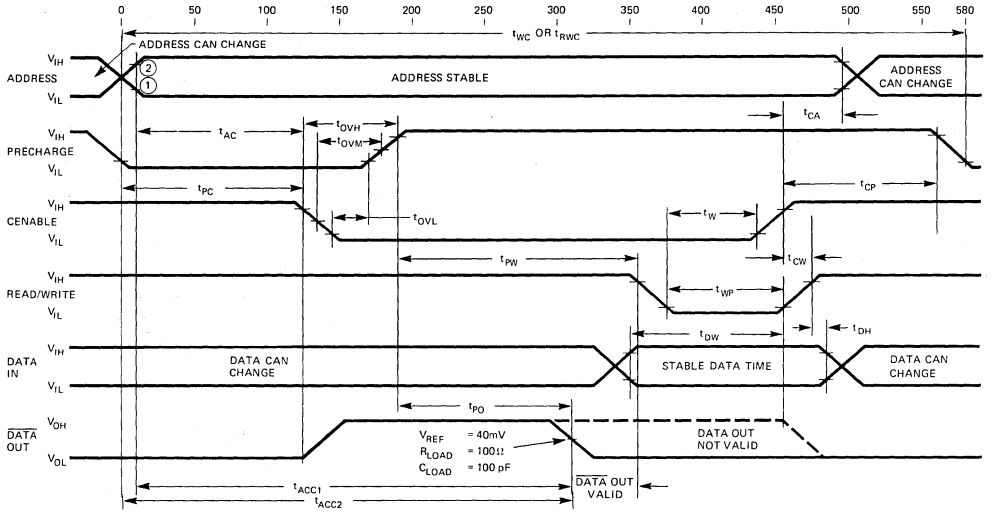
*CAPACITANCE T_A = 25°C

SYMBOL	TEST	TYP.	PLASTIC PKG. MAX.	CERAMIC PKG. MAX.	UNIT	CONDITIONS
C_{AD}	ADDRESS CAPACITANCE	5	7	12	pF	V_{IN} = V_{SS}; f = 1 MHz, All Unused Pins Are At A.C. Ground
C_{PR}	PRECHARGE CAPACITANCE	15	18	19.5	pF	V_{IN} = V_{SS}; f = 1 MHz, All Unused Pins Are At A.C. Ground
C_{CE}	CENABLE CAPACITANCE	15	18	21	pF	V_{IN} = V_{SS}; f = 1 MHz, All Unused Pins Are At A.C. Ground
C_{RW}	READ/WRITE CAPACITANCE	11	15	19.5	pF	V_{IN} = V_{SS}; f = 1 MHz, All Unused Pins Are At A.C. Ground
C_{IN1}	DATA INPUT CAPACITANCE	4	5	7.5	pF	CENABLE = 0V, V_{IN} = V_{SS}; f = 1 MHz, All Unused Pins Are At A.C. Ground
C_{IN2}	DATA INPUT CAPACITANCE	2	4	6.5	pF	CENABLE = V_{SS}, V_{IN} = V_{SS}; f = 1 MHz, All Unused Pins Are At A.C. Ground
C_{OUT}	DATA OUTPUT CAPACITANCE	2	3	7	pF	V_{OUT} = 0V; f = 1 MHz, All Unused Pins Are At A.C. Ground

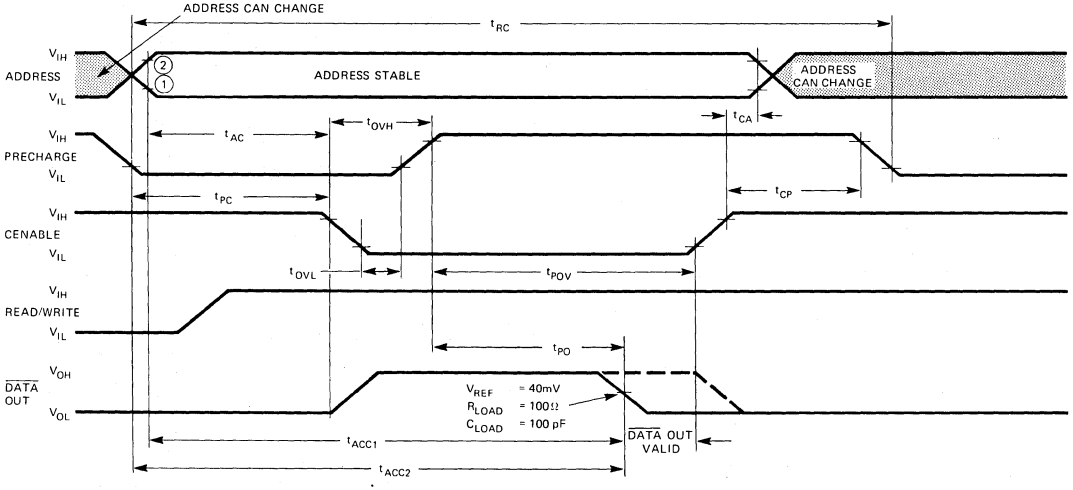
*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTE ① V_{DD} + 2V
NOTE ② V_{SS} - 2V
t_T IS DEFINED AS THE TRANSITIONS BETWEEN THESE TWO POINTS

NOTE 3 t_{DW} IS REFERENCED TO POINT ① OF THE RISING EDGE OF CENABLE OR READ/WRITE WHICHEVER OCCURS FIRST

NOTE 4 t_{DH} IS REFERENCED TO POINT ② OF THE RISING EDGE OF CENABLE OR READ/WRITE WHICHEVER OCCURS FIRST

The Intel®1103-1 is a high speed 1024 bit dynamic random access memory and is the high speed version of the standard 1103. The DC and AC Characteristics for the 1103-1 are given in the following three pages. The absolute maximum ratings for the 1103-1 are the same as for the 1103 on page 2-8.

- **Access Time — 150 nsec**
- **Cycle Time — 340 nsec**

D.C. and Operating Characteristics

(T_A = 0°C to +55°C, V_{SS}[1] = 19V ±5% ($V_{BB} - V_{SS}$)[6] = 3V to 4V, V_{DD} = 0V unless otherwise specified)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)			**10**	**μA**	**V_{IN} = 0V**
I_{LO}	OUTPUT LEAKAGE CURRENT			10	μA	V_{OUT} = 0V
I_{BB}	**V_{BB} SUPPLY CURRENT**			**100**	**μA**	
I_{DD1}[2]	SUPPLY CURRENT DURING T_{PC}		45	60	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = V_{SS} T_A = 25°C
I_{DD2}[2]	SUPPLY CURRENT DURING T_{OV}		50	68.5	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = 0V T_A = 25°C
I_{DD3}[2]	SUPPLY CURRENT DURING T_{POV}		8.5	11	mA	PRECHARGE = V_{SS} CENABLE = 0V T_A = 25°C
I_{DD4}[2]	SUPPLY CURRENT DURING T_{CP}		3.0	4	mA	PRECHARGE = V_{SS} CENABLE = V_{SS} T_A = 25°C
$I_{DD\,AVG}$[5]	**AVERAGE SUPPLY CURRENT**		20	**23**	**mA**	**CYCLE TIME = 340 ns PRECHARGE WIDTH@50% 105ns, T_A = 25°C**
V_{IL}	INPUT LOW VOLTAGE	V_{SS} − 20		V_{SS} − 18	V	
V_{IH}	INPUT HIGH VOLTAGE	V_{SS} − 1		V_{SS} + 1	V	
I_{OH1}	**OUTPUT HIGH CURRENT**	**1150**	**1300**	**7000**	**μA**	**T_A = 25°C**
I_{OH2}	**OUTPUT HIGH CURRENT**	**900**	**1150**	**7000**	**μA**	**T_A = 55°C**
I_{OL}[3]	OUTPUT LOW CURRENT		See Note 3			**R_{LOAD}[4] = 100 Ω**
V_{OH1}	OUTPUT HIGH VOLTAGE	115	130	700	mV	T_A = 25°C,
V_{OH2}	OUTPUT HIGH VOLTAGE	90	115	700	mV	T_A = 55°C,
V_{OL}[3]	OUTPUT LOW VOLTAGE		See Note 3			

Note 1: The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).

Note 2: See Supply Current vs. Temperature (p. 2-9) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.

Note 3: The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.

Note 4: This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

Note 5: This parameter is periodically sampled and is not 100% tested.

Note 6: (V_{BB} − V_{SS}) supply should be applied at or before V_{SS}.

AC Characteristics (T_A = 0°C to 55°C, V_{SS} = 19 ± 5%, $V_{BB} - V_{SS}$ = 3.0V to 4.0V, V_{DD} = 0V)

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	**TIME BETWEEN REFRESH**			**1**	**ms**	
t_{AC}	ADDRESS TO CENABLE SET UP TIME	30			ns	
t_{CA}	CENABLE TO ADDRESS HOLD TIME	10			ns	
t_{PC}	PRECHARGE TO CENABLE DELAY	60			ns	
t_{CP}	CENABLE TO PRECHARGE DELAY	40			ns	
t_{OVL}	PRECHARGE & CENABLE OVERLAP, LOW	5		30	ns	t_T = 20ns
t_{OVH}	PRECHARGE & CENABLE OVERLAP, HIGH			85	ns	t_T = 20ns
t_{OVM}	PRECHARGE & CENABLE OVERLAP, 50% POINTS	25		50	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC}(1)	**READ CYCLE**	**300**			**ns**	**t_T = 20 ns**
t_{POV}	PRECHARGE TO END OF CENABLE	115		500	ns	
t_{PO}(1)	END OF PRECHARGE TO OUTPUT DELAY			75	ns	C_{LOAD}=50 pF R_{LOAD}=100Ω V_{REF}=80 mV
t_{ACC1}(1)	**ADDRESS TO OUTPUT ACCESS**	**150**			**ns**	**$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$** C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV
t_{ACC2}(1)	**PRECHARGE TO OUTPUT ACCESS**	**180**			**ns**	**$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$** C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}	**WRITE CYCLE**	**340**			**ns**	**t_T = 20 ns**
t_{RWC}(1)	**READ/WRITE CYCLE**	**340**			**ns**	
t_{PW}	PRECHARGE TO READ/WRITE DELAY	115		500	ns	
t_{WP}	READ/WRITE PULSE WIDTH	20			ns	
t_W	READ/WRITE SET UP TIME	20			ns	
t_{DW}	DATA SET UP TIME	40			ns	
t_{DH}	DATA HOLD TIME	10			ns	
t_{PO}(1)	END OF PRECHARGE TO OUTPUT DELAY			75	ns	C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV
t_{CW}	RELATIONSHIP BETWEEN CENABLE AND READ/WRITE			0	ns	

NOTE 1: These times will degrade by 35 nsec if a V_{REF} point of*40 mV is chosen instead of the 80 mV point defined in the spec.

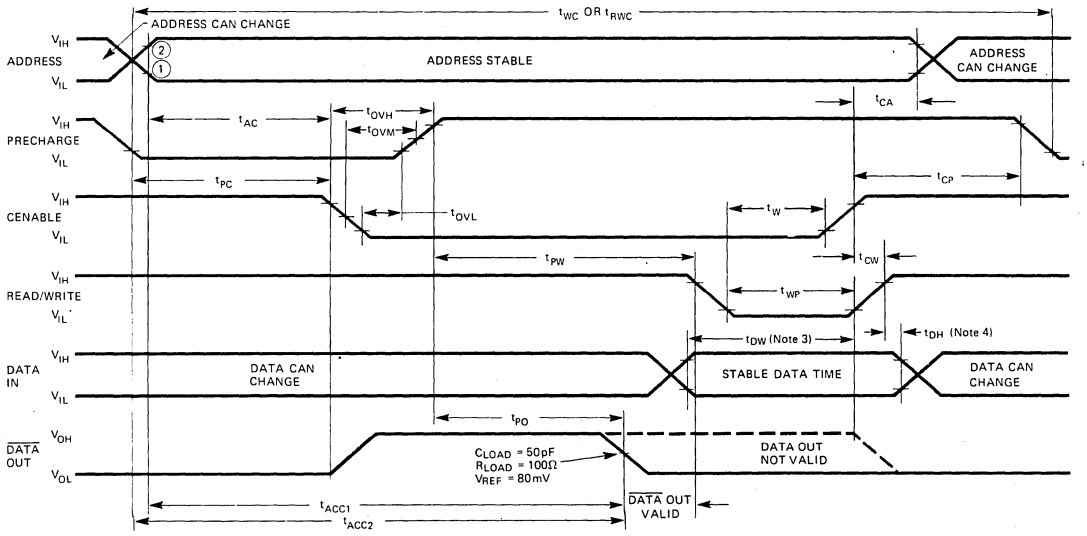
*CAPACITANCE T_A = 25°C

SYMBOL	TEST	TYP.	PLASTIC PKG. MAX.	CERAMIC PKG. MAX.	UNIT	CONDITIONS
C_{AD}	ADDRESS CAPACITANCE	5	7	12	pF	$V_{IN} = V_{SS}$
C_{PR}	PRECHARGE CAPACITANCE	15	18	19.5	pF	$V_{IN} = V_{SS}$
C_{CE}	CENABLE CAPACITANCE	15	18	21	pF	$V_{IN} = V_{SS}$
C_{RW}	READ/WRITE CAPACITANCE	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	DATA INPUT CAPACITANCE	4	5	7.5	pF	CENABLE = 0V $V_{IN} = V_{SS}$
C_{IN2}	DATA INPUT CAPACITANCE	2	4	6.5	pF	CENABLE = V_{SS} $V_{IN} = V_{SS}$
C_{OUT}	DATA OUTPUT CAPACITANCE	2	3	7	pF	V_{OUT} = 0V

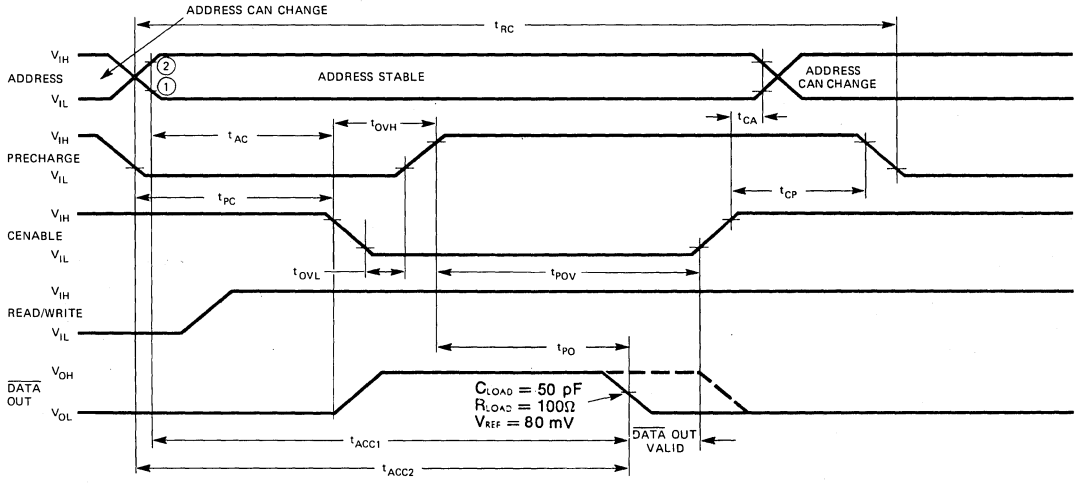
f = 1 MHz, All Unused Pins Are At A.C. Ground

*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.

WRITE OR READ/WRITE CYCLE



READ CYCLE



NOTE ① V_{DD} + 2V, NOTE ② V_{SS} − 2V] t_T IS DEFINED AS THE TRANSITIONS BETWEEN THESE TWO POINTS

NOTE 3 t_{DW} IS REFERENCED TO POINT ① OF THE RISING EDGE OF CHIP ENABLE OR READ/WRITE WHICHEVER OCCURS FIRST

NOTE 4 t_{DH} IS REFERENCED TO POINT ② OF THE RISING EDGE OF CHIP ENABLE OR READ/WRITE WHICHEVER OCCURS FIRST

1103A

FULLY DECODED RANDOM ACCESS 1024 BIT DYNAMIC MEMORY

- *No Precharge Required -- Critical Precharge Timing is Eliminated
- Electrically Equivalent to 1103 -- Pin-for-Pin/Functionally Compatible
- Fast Access Time -- 205ns max.
- Low Standby Power Dissipation -- 2 µW/Bit typical
- Address Registers Incorporated on the Chip
- Simple Memory Expansion -- Chip Enable Input Lead
- Inputs Protected -- All Inputs Have Protection Against Static Charge
- Ceramic and Plastic Package -- 18-Pin DIP

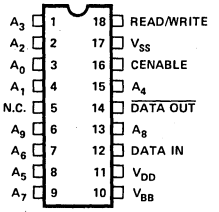
The 1103A is a 1024 word by 1 bit dynamic RAM. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives. The 1103A is electrically equivalent to the 1103.

1103A systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

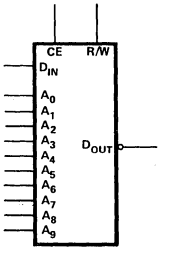
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every two milliseconds. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

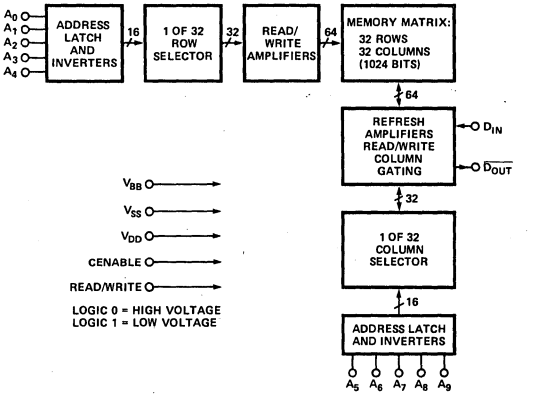
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to 70°C

Storage Temperature ..... −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} ..... −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} ..... −25V to 0.3V

Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

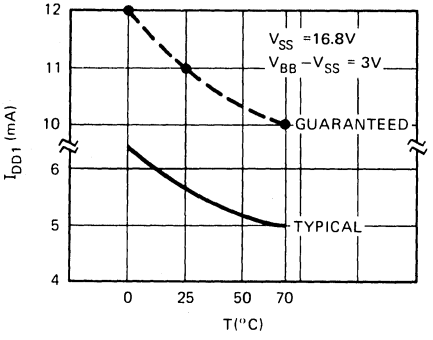
T_A = 0°C to +70°C, V_{SS} [1] = 16V ± 5%, (V_{BB} − V_{SS}) [2] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

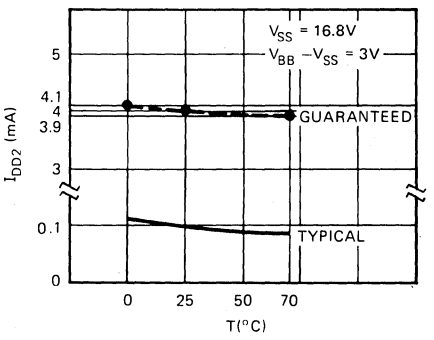
Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			1	μA	V_{IN} = 0V
I_{LO}	Output Leakage Current			1	μA	V_{OUT} = 0V
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		4	11	mA	Cenable = 0V; T_A = 25°C
I_{DD2}	Supply Current During Cenable Off		0.1	4	mA	Cenable = V_{SS}; T_A = 25°C
I_{DDAV}	Average Supply Current		17	25	mA	Cycle Time = 580ns; T_A = 25°C
V_{IL}	Input Low Voltage	V_{DD} −1		V_{DD} +1	V	
V_{IH}	Input High Voltage	V_{SS} −1		V_{SS} +1	V	
I_{OH1}	Output High Current	600	1800	4000	μA	T_A = 25°C
I_{OH2}	Output High Current	500	1500	4000	μA	T_A = 70°C
I_{OL}	Output Low Current	See Note Three				R_{LOAD}[4] = 100Ω
V_{OH1}	Output High Voltage	60	180	400	mV	T_A = 25°C
V_{OH2}	Output High Voltage	50	150	400	mV	T_A = 70°C
V_{OL}	Output Low Voltage	See Note Three				

NOTES:

1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. (V_{BB} −V_{SS}) supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

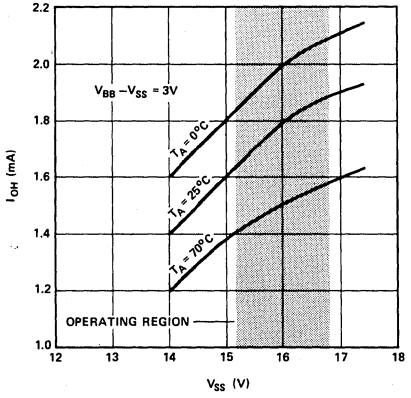
Supply Current vs Temperature



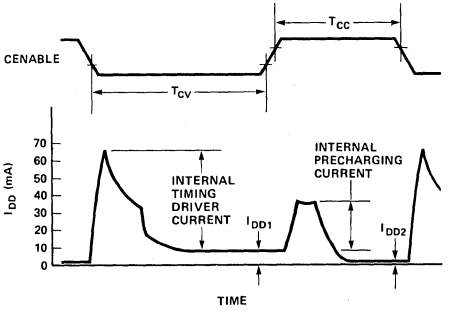


Typical Characteristics

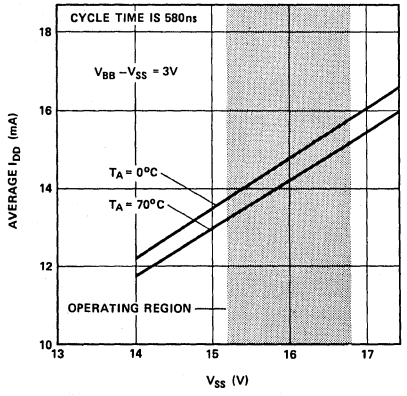
OUTPUT HIGH CURRENT
VS. SUPPLY VOLTAGE



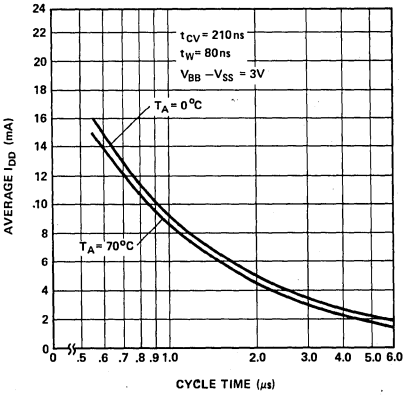
I_{DD} VS. CENABLE



AVERAGE I_{DD} VS.
SUPPLY VOLTAGE



AVERAGE I_{DD} VS.
1103A CYCLE TIME



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{SS} = 16V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	230		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	480		ns	$t_T = 20ns$; $C_{LOAD} = 100pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 40mV$
t_{CV}	Cenable on Time	210	500	ns	
t_{CO}	Cenable Output Delay		185	ns	
t_{ACC}	**ADDRESS TO OUTPUT ACCESS**		205	ns	$t_{ACC} = t_{AC\ MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	580		ns	$t_T = 20ns$
t_{RWC}	Read/Write Cycle	580		ns	
t_{CW}	Cenable to Read/Write Delay	210	500	ns	
t_{WP}	Read/Write Pulse Width	50		ns	
t_W	Read/Write Set Up Time	80		ns	
t_{DW}	Data Set Up Time	105		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		185	ns	$C_{LOAD} = 100pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 40mV$
t_{WC}	Read/Write to Cenable	0		ns	

CAPACITANCE[1] $T_A = 25°C$

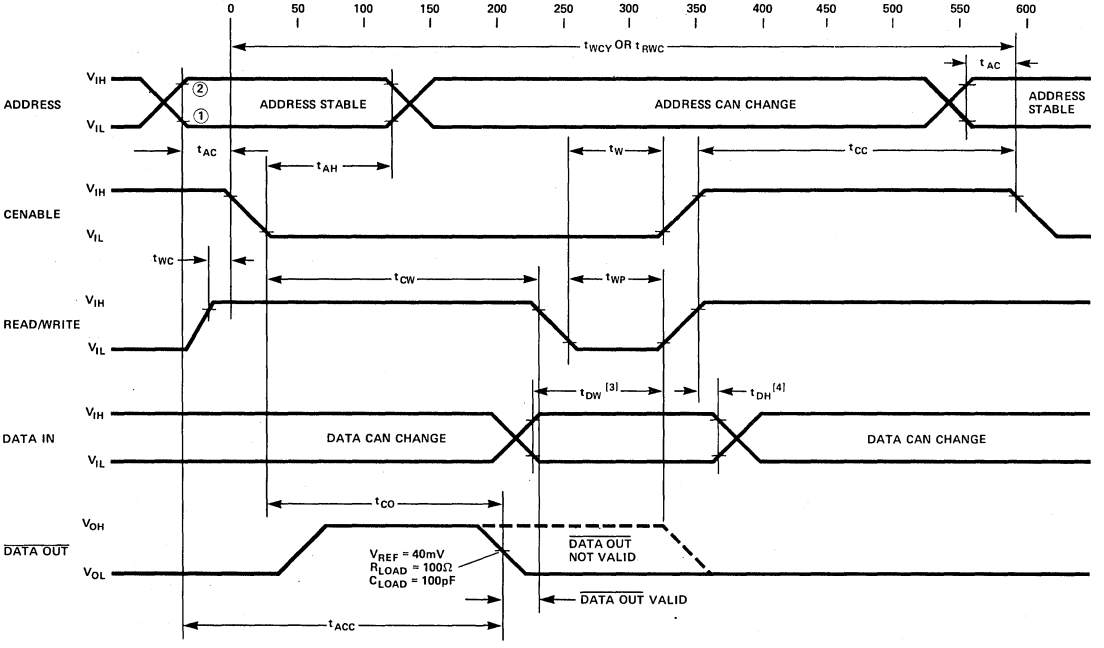
Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V; $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$; $V_{OUT} = 0V$

f = 1MHz. All unused pins are at A.C. ground.

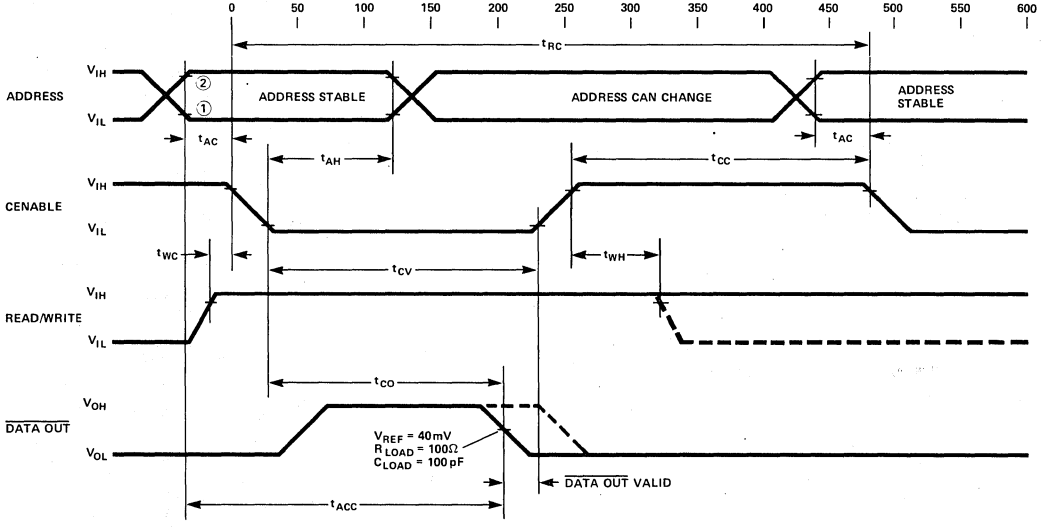
NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTES:

1. V_{DD} + 2V
2. V_{SS} − 2V

t_T is defined as the transition between these two points.

3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of Read/Write.

FULLY DECODED RANDOM ACCESS 1024 BIT DYNAMIC MEMORY

- **High Speed 1103A — Access Time — 145 ns / Cycle Time — 340 ns**
- ***No Precharge Required -- Critical Precharge Timing is Eliminated**
- **Low Standby Power Dissipation -- 0.2 µW/Bit Typical**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion -- Chip Enable Input Lead**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

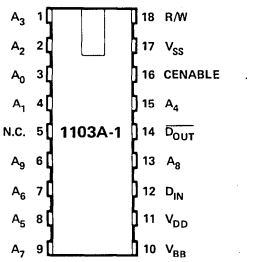
The Intel®1103A-1 is a high speed 1024 bit dynamic random access memory and is the fastest version of the standard 1103A. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

1103A-1 systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

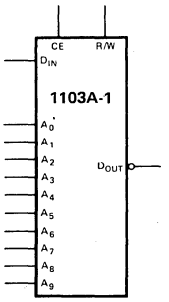
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every one millisecond. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A-1 is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



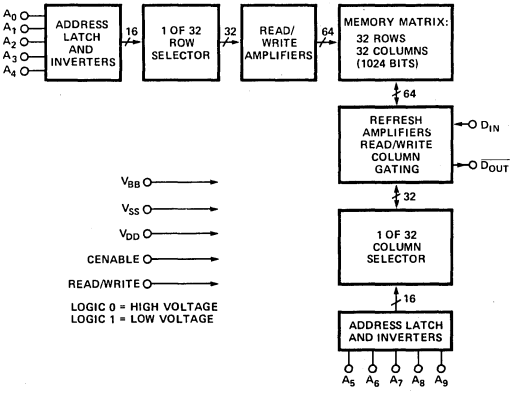
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} . . . . . −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . . −25V to 0.3V

Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

$T_A = 0°C$ to $+55°C$, V_{SS}[1] $= 19V \pm 5\%$, $(V_{BB} - V_{SS})$[2] $= 3V$ to $4V$, $V_{DD} = 0V$ unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	$V_{IN} = 0V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 0V$
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		7	11	mA	Cenable = 0V; $T_A = 25°C$
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; $T_A = 25°C$
I_{DDAV}	Average Supply Current		25	33	mA	Cycle Time = 340ns; $T_A = 25°C$
V_{IL}	Input Low Voltage	$V_{DD} - 1$		$V_{DD} + 1$	V	
V_{IH}	Input High Voltage	$V_{SS} - 1$		$V_{SS} + 1$	V	
I_{OH1}	Output High Current	1150	1800	7000	μA	$T_A = 25°C$
I_{OH2}	Output High Current	900	1600	7000	μA	$T_A = 55°C$
I_{OL}	Output Low Current	See Note Three				R_{LOAD}[4] $= 100\Omega$
V_{OH1}	Output High Voltage	115	180	700	mV	$T_A = 25°C$
V_{OH2}	Output High Voltage	90	160	700	mV	$T_A = 55°C$
V_{OL}	Output Low Voltage	See Note Three				

NOTES:

1. The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.
2. $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

A.C. Characteristics $T_A = 0°C$ to $55°C$, $V_{SS} = 19V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$.

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	120		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	300		ns	$t_T = 20ns$; $C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 80mV$
t_{CV}	Cenable on Time	140	500	ns	
t_{CO}	Cenable Output Delay		125	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		145	ns	$t_{ACC} = t_{AC\ MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	340		ns	$t_T = 20ns$
t_{RWC}	Read/Write Cycle	340		ns	
t_{CW}	Cenable to Read/Write Delay	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		125	ns	$C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 80mV$
t_{WC}	Read/Write to Cenable	0		ns	

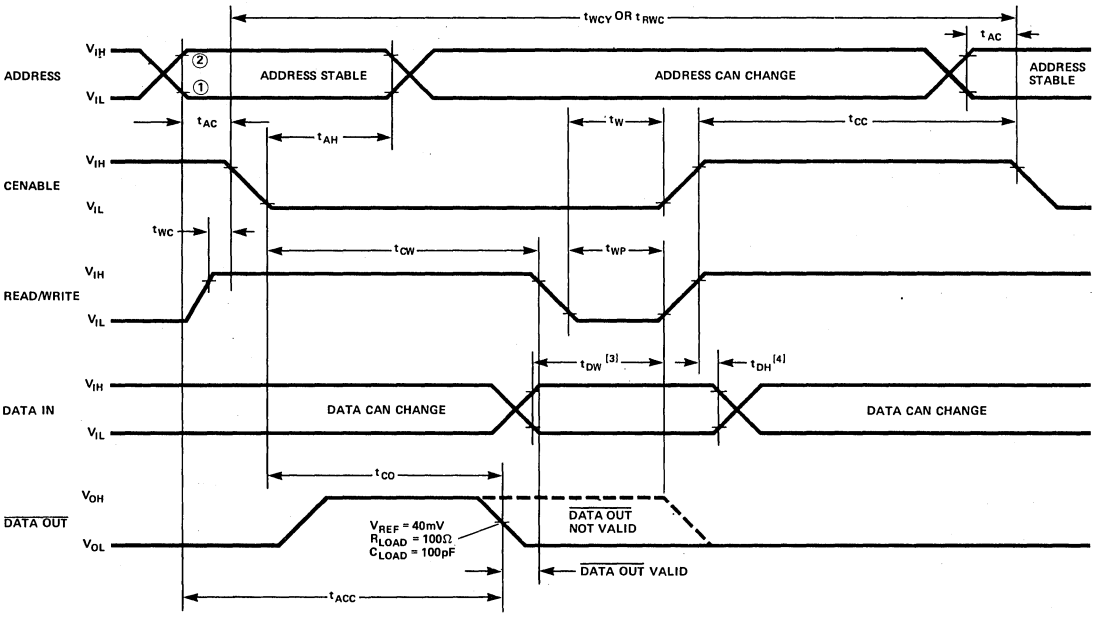
CAPACITANCE[1] $T_A = 25°C$

Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V; $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$; $V_{OUT} = 0V$

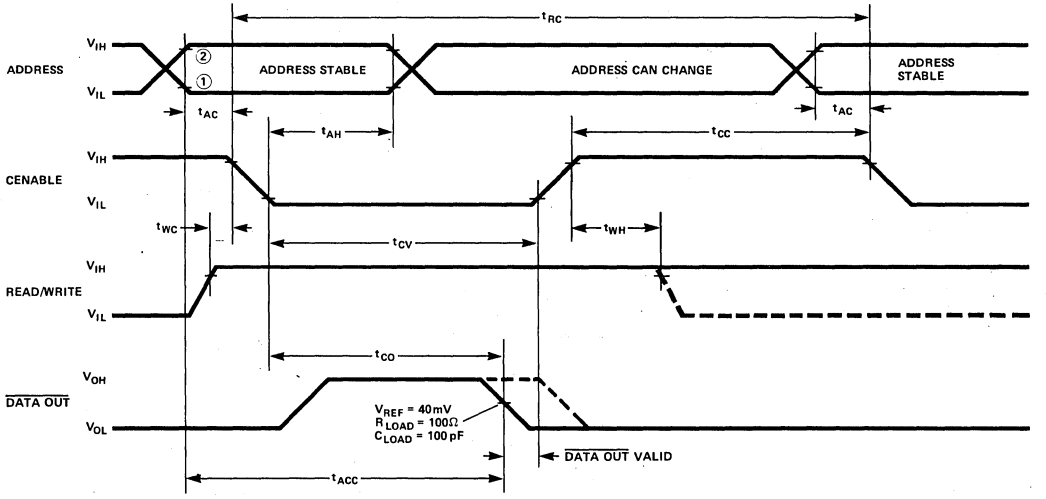
f = 1MHz. All unused pins are at A.C. ground.

NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE



READ CYCLE

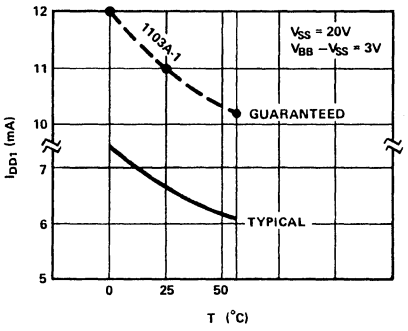


NOTES:
1. V_{DD} + 2V
2. V_{SS} − 2V

t_T is defined as the transition between these two points.

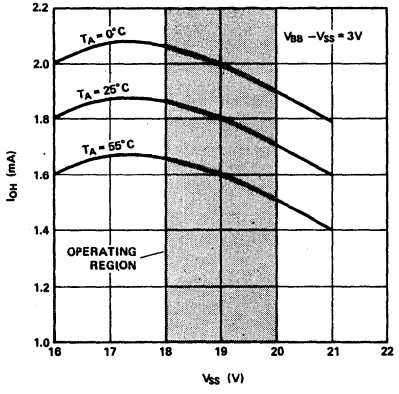
3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of Read/Write.

Supply Current vs Temperature

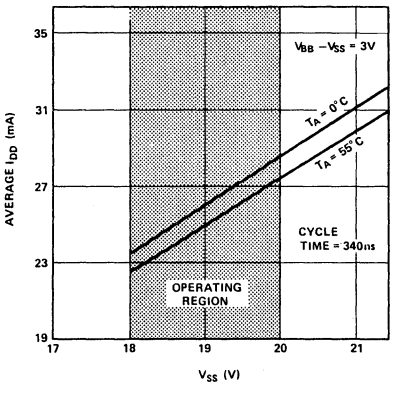


Typical Characteristics

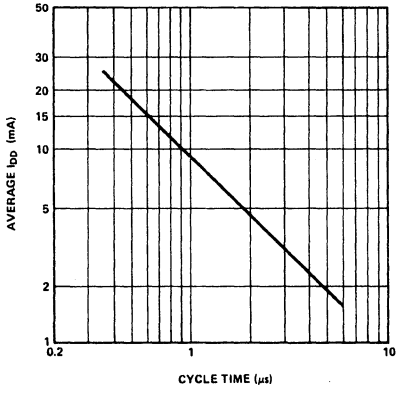
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



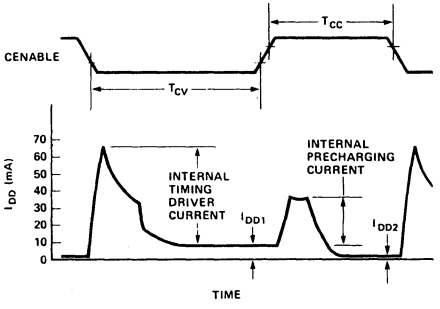
AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. CYCLE TIME



I_{DD} VS. CENABLE



RAMS

FULLY DECODED RANDOM ACCESS 1024 BIT DYNAMIC MEMORY

- **High Speed 1103A — Access Time — 145ns/Cycle Time — 400ns**
- ***No Precharge Required -- Critical Precharge Timing is Eliminated**
- **Low Standby Power Dissipation -- 0.2 µW/Bit Typical**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion -- Chip Enable Input Lead**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

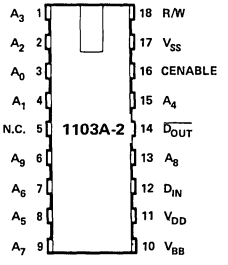
The Intel®1130A-2 is a high speed 1024 bit dynamic random access memory and is the 400ns cycle time version of the standard 1103A. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

1103A-2 systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

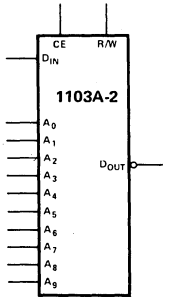
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every one millisecond. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A-2 is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



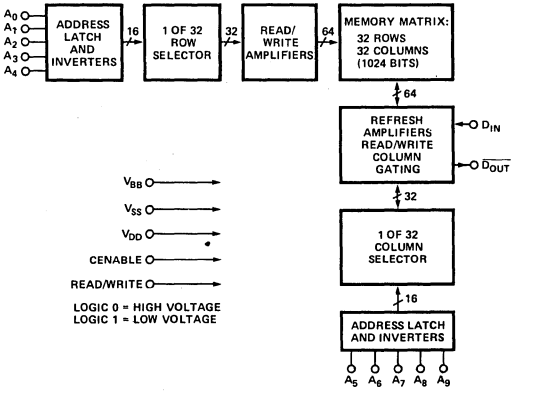
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to 70°C

Storage Temperature ..... −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} ..... −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} ..... −25V to 0.3V

Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to + 55°C, V_{SS}[1] = 19V ± 5%, (V_{BB} −V_{SS})[2] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		7	11	mA	Cenable = 0V; T_A = 25°C
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; T_A = 25°C
I_{DDAV}	Average Supply Current		22	30	mA	Cycle Time = 400ns; T_A = 25°C
V_{IL}	Input Low Voltage	V_{DD} −1		V_{DD} +1	V	
V_{IH}	Input High Voltage	V_{SS} −1		V_{SS} +1	V	
I_{OH1}	Output High Current	1150	1800	7000	μA	T_A = 25°C
I_{OH2}	Output High Current	900	1600	7000	μA	T_A = 55°C
I_{OL}	Output Low Current	See Note Three				R_{LOAD}[4] = 100Ω
V_{OH1}	Output High Voltage	115	180	700	mV	T_A = 25°C
V_{OH2}	Output High Voltage	90	160	700	mV	T_A = 55°C
V_{OL}	Output Low Voltage	See Note Three				

NOTES:

1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. (V_{BB} −V_{SS}) supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

A.C. Characteristics $T_A = 0°C$ to $55°C$, $V_{SS} = 19V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$.

READ, WRITE, AND READ/WRITE CYCLE

Refer to page 2-23 for definitions.

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	180		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	360		ns	$t_T = 20ns$; $C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 80mV$
t_{CV}	Cenable on Time	140	500	ns	
t_{CO}	Cenable Output Delay		125	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		145	ns	$t_{ACC} = t_{AC\ MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	400		ns	$t_T = 20ns$
t_{RWC}	Read/Write Cycle	400		ns	
t_{CW}	Cenable to Read/Write Delay	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		125	ns	$C_{LOAD} = 50pF$, $R_{LOAD} = 100\Omega$, $V_{REF} = 80mV$
t_{WC}	Read/Write to Cenable	0		ns	

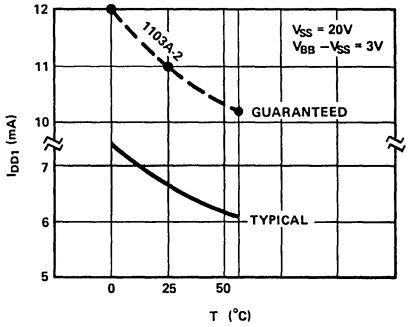
CAPACITANCE[1] $T_A = 25°C$

Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V, $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$, $V_{OUT} = 0V$

f = 1MHz. All unused pins are at A.C. ground.

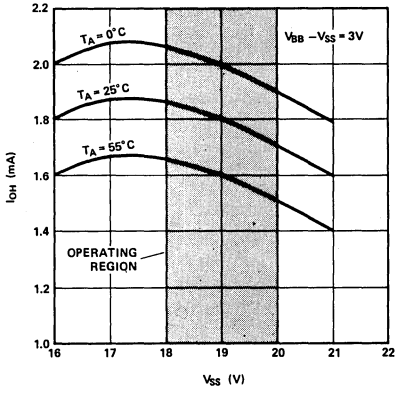
NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

Supply Current vs Temperature

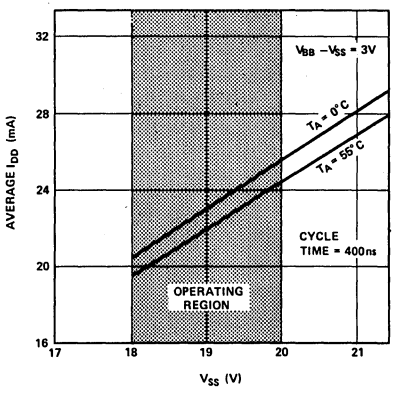


Typical Characteristics

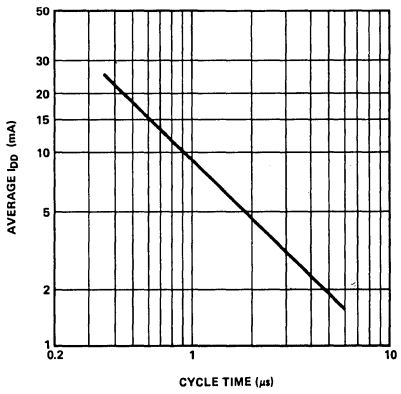
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



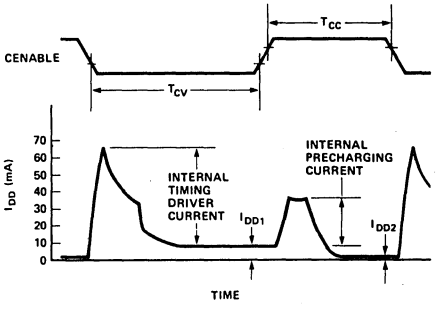
AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. CYCLE TIME



I_{DD} VS. CENABLE



2101A

256 x 4 RAM WITH SEPARATE I/O

2101A-2	250 ns Max.
2101A	350 ns Max.
2101A-4	450 ns Max.

- **256 x 4 Organization to Meet Needs for Small System Memories**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Statis MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 22 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150mW**
- **Three-State Output: OR-Tie Capability**
- **Output Disable Provided for Ease of Use in Common Data Bus Systems**

The Intel® 2101A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

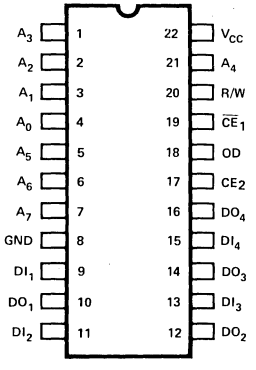
The 2101A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bi-directional logic in a common I/O system.

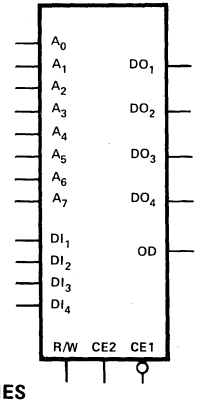
The Intel® 2101A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



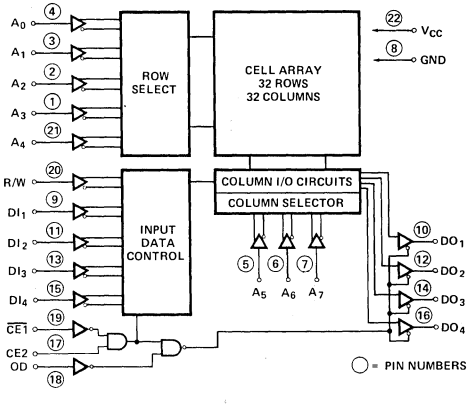
LOGIC SYMBOL



PIN NAMES

DI_1-DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1-DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

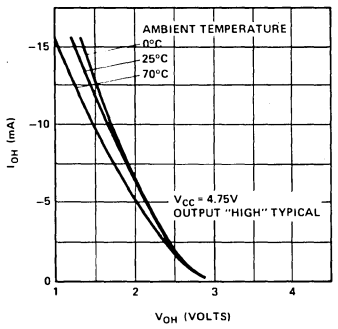
D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

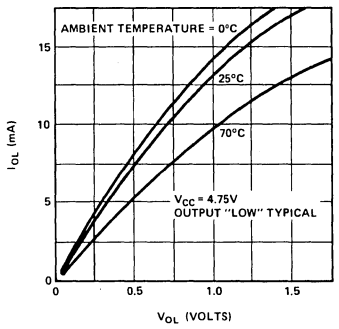
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current[2]			1	10	µA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	I/O Leakage Current[2]			-1	-10	µA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current	2101A, 2101A-4		35	55	mA	V_{IN} = 5.25V, I_O = 0mA, T_A = 25°C
		2101A-2		45	65		
I_{CC2}	Power Supply Current	2101A, 2101A-4			60	mA	V_{IN} = 5.25V, I_O = 0mA, T_A = 0°C
		2101A-2			70		
V_{IL}	Input "Low" Voltage		-0.5		+0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2101A, 2101A-2	2.4			V	I_{OH} = -200µA
		2101A-4	2.4			V	I_{OH} = -150µA

Typical D. C. Characteristics

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. Characteristics for 2101A-2 (250 ns Access Time)

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	
t_A	Access Time			250	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			180	ns	
t_{OD}	Output Disable To Output			130	ns	Timing Reference = 1.5V
t_{DF}[3]	Data Output to High Z State	0		180	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	150			ns	
t_{DW}	Data Setup	150			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	150			ns	and C_L = 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.8 Volt and 2.0 Volts

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

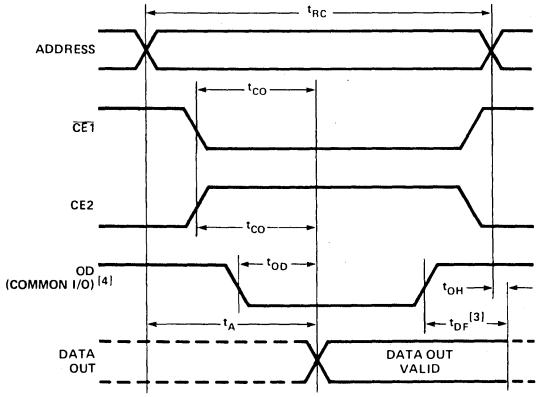
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[2] $T_A = 25°C$, f = 1MHz

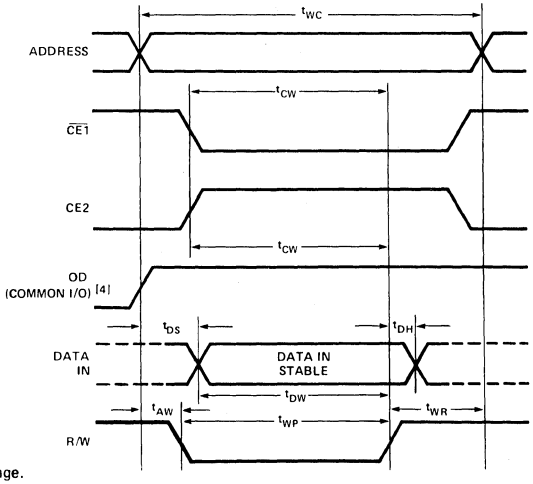
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.
4. OD should be tied low for separate I/O operation.

2101A (350 ns Access Time)
A.C. Characteristics

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			350	ns	
t_{CO}	Chip Enable To Output			240	ns	
t_{OD}	Output Disable To Output			180	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	220			ns	t_r, t_f = 20ns Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	200			ns	
t_{DW}	Data Setup	200			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	200			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

2101A-4 (450 ns Access Time)
A.C. Characteristics

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	t_r, t_f = 20ns Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.

2101, 2101-1, 2101-2

1024 BIT (256 x 4) STATIC MOS RAM WITH SEPARATE I/O

- **256 x 4 Organization to Meet Needs for Small System Memories**
- **Access Time — 0.5 to 1 μsec Max.**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Simple Memory Expansion — Chip Enable Input**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 22 Pin Plastic Dual-In-Line Configuration**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**
- **Output Disable Provided for Ease of Use in Common Data Bus Systems**

The Intel®2101 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

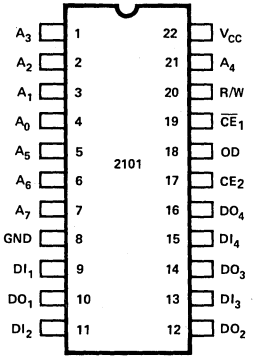
The 2101 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bidirectional logic in a common I/O system.

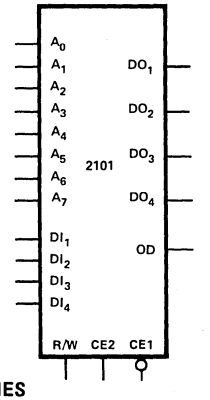
The Intel 2101 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



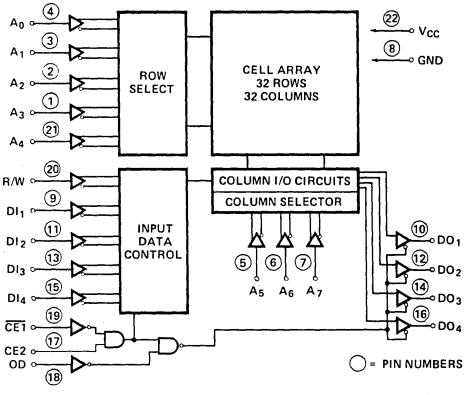
LOGIC SYMBOL



PIN NAMES

DI_1-DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1-DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

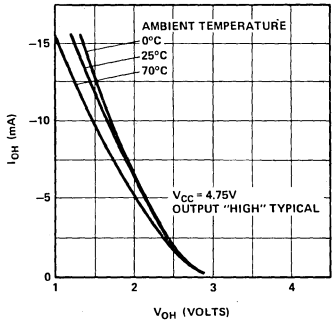
D.C. and Operating Characteristics for 2101, 2101-1, 2101-2

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

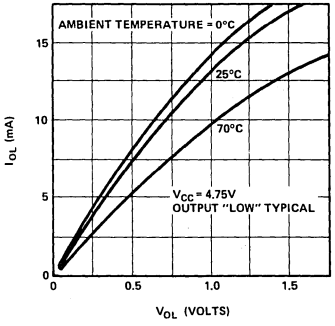
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current[2]			15	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	I/O Leakage Current[2]			-50	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150 μA

Typical D. C. Characteristics

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Input and Output tied together.

A.C. Characteristics for 2101

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	1,000			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			1,000	ns	
t_{CO}	Chip Enable To Output			800	ns	
t_{OD}	Output Disable To Output			700	ns	
t_{DF}[3]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	1,000			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	900			ns	
t_{DW}	Data Setup	700			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	750			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	200			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

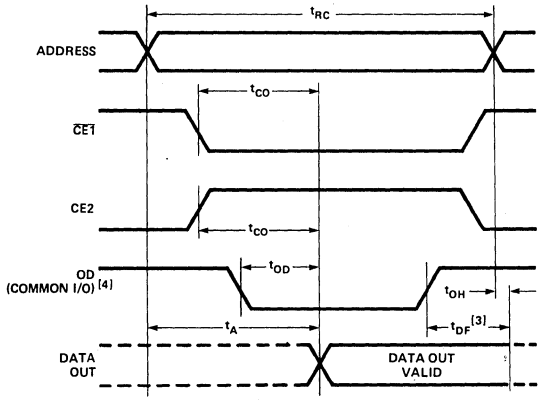
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[2] T_A = 25°C, f = 1MHz

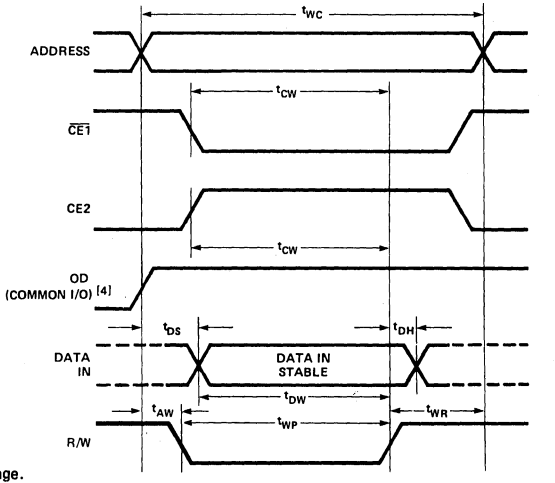
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.
4. OD should be tied low for separate I/O operation.

2101-1 (500 ns Access Time)
A.C. Characteristics for 2101-1

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	500			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			500	ns	
t_{CO}	Chip Enable To Output			350	ns	
t_{OD}	Output Disable To Output			300	ns	
t_{DF}[2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	500			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	100			ns	
t_{CW}	Chip Enable To Write	400			ns	
t_{DW}	Data Setup	280			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	300			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

2101-2 (650 ns Access Time)
A.C. Characteristics for 2101-2

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			650	ns	
t_{CO}	Chip Enable To Output			400	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}[2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.

2102A, 2102AL

1K (1K x 1) STATIC RAM

P/N	Standby Pwr. (mW)	Operating Pwr. (mW)	Access (ns)
2102AL-4	35	174	450
2102AL	35	174	350
2102AL-2	42	342	250
2102A-2	—	342	250
2102A	—	289	350
2102A-4	—	289	450
2102A-6	—	289	650

- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Standby Power Mode (2102AL)**
- **Three-State Output: OR-Tie Capability**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Dual-In-Line Configuration**

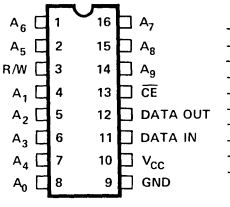
The Intel® 2102A is a high speed 1024 word by one bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operated. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. *A low standby power version (2102AL) is also available. It has all the same operating characteristics of the 2102A with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.*

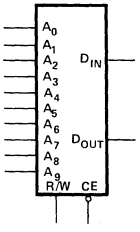
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



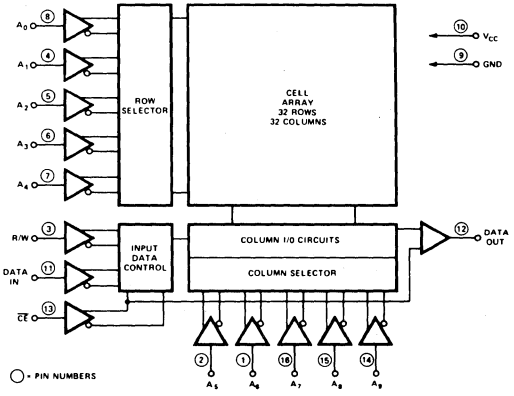
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	2102A, 2102A-4 2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102A-2, 2102AL-2 Limits Min.	Typ.[1]	Max.	2101A-6 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10		1	10		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current		1	5		1	5		1	5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current		-1	-10		-1	-10		-1	-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		33	Note 2		45	65		33	55	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	-0.5		0.65	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			2.4			2.2			V	I_{OH} = -100μA

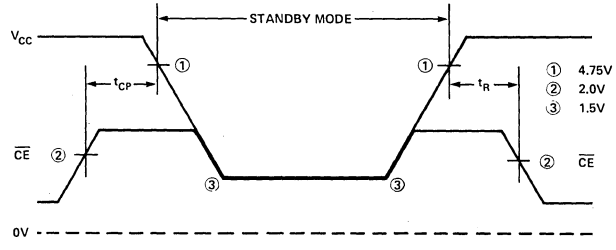
Notes: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. The maximum I_{CC} value is 55mA for the 2102A and 2102A-4, and 33mA for the 2102AL and 2102AL-4.

Standby Characteristics 2102AL, 2102AL-2, and 2102AL-4

T_A = 0°C to 70°C

Symbol	Parameter	2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102AL-2 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	1.5			1.5			V	
V_{CES}[2]	$\overline{CE}$ Bias in Standby	2.0			2.0			V	2.0V≤V_{PD}≤V_{CC} Max.
		V_{PD}			V_{PD}			V	1.5V≤V_{PD}< 2.0V
I_{PD1}	Standby Current		15	23		20	28	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current		20	30		25	38	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			0			ns	
t_R[3]	Standby Recovery Time	t_{RC}			t_{RC}			ns	

STANDBY WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
3. t_R = t_{RC} (READ CYCLE TIME).

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

READ CYCLE

Symbol	Parameter	2102A-2, 2102AL-2 Limits (ns) Min.	Max.	2102A, 2102AL Limits (ns) Min.	Max.	2102A-4, 2102AL-4 Limits (ns) Min.	Max.	2102A-6 Limits (ns) Min.	Max.
t_{RC}	Read Cycle	250		350		450		650	
t_A	Access Time		250		350		450		650
t_{CO}	Chip Enable to Output Time		130		180		230		400
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40		50	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0	

WRITE CYCLE

t_{WC}	Write Cycle	250	350	450	650
t_{AW}	Address to Write Setup Time	20	20	20	200
t_{WP}	Write Pulse Width	180	250	300	400
t_{WR}	Write Recovery Time	0	0	0	50
t_{DW}	Data Setup Time	180	250	300	450
t_{DH}	Data Hold Time	0	0	0	20
t_{CW}	Chip Enable to Write Setup Time	180	250	300	550

A.C. CONDITIONS OF TEST

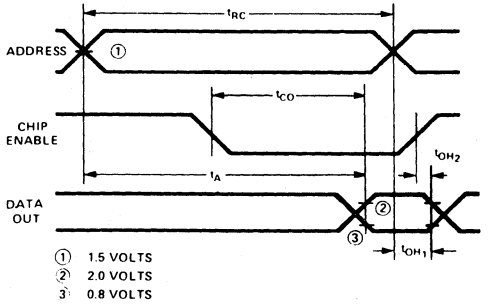
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

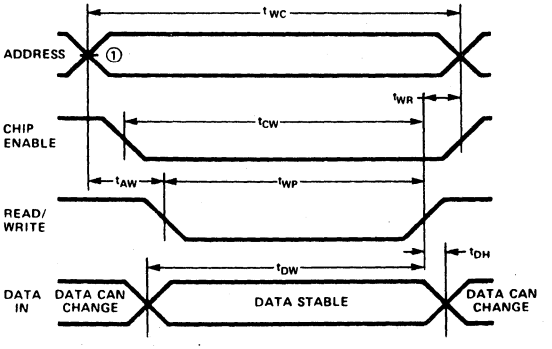
SYMBOL	TEST	LIMITS (pF) TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



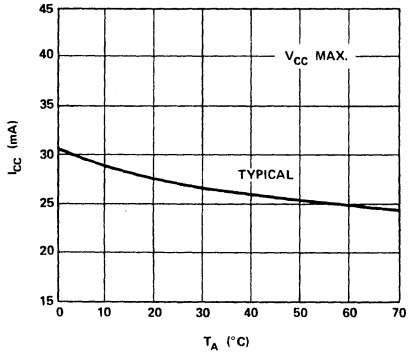
WRITE CYCLE



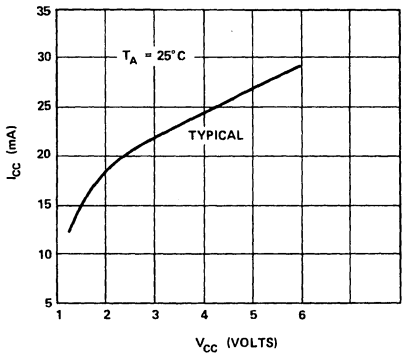
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Typical D. C. and A. C. Characteristics

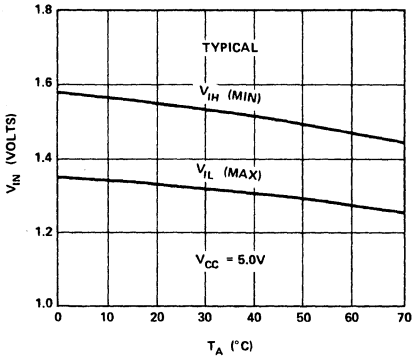
POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



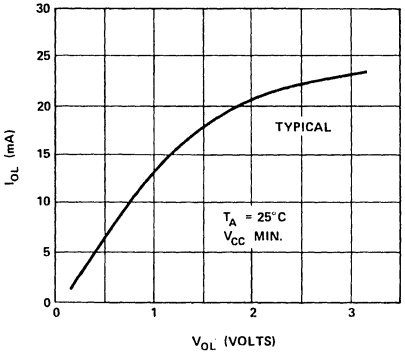
POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



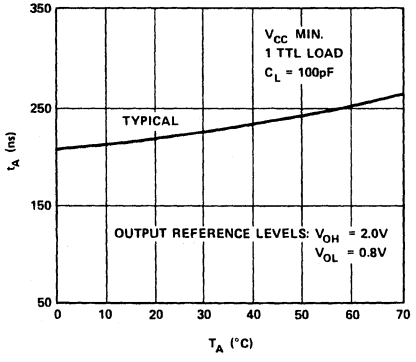
V_{IN} LIMITS VS. TEMPERATURE



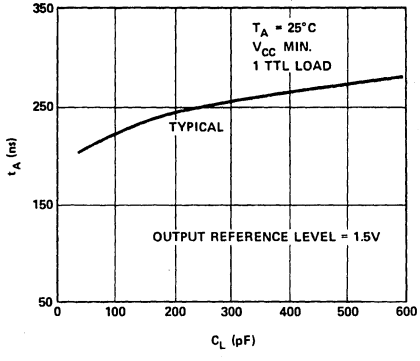
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



M2102A-4, M2102A-6

MILITARY TEMPERATURE RANGE 1K STATIC RAM

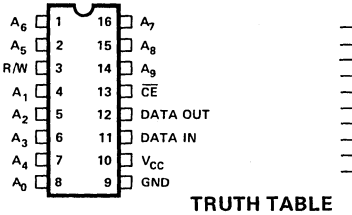
M2102A-4	450 ns Max.
M2102A-6	650 ns Max.

- 10% V_{CC} Supply Tolerance
- Directly TTL Compatible: All Inputs and Output
- Low Power: 385mW Max.
- Three State Output: OR-Tie Capability
- 16 Pin Hermetic Dual-In-Line Package

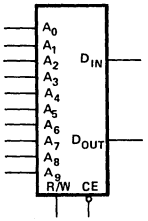
The Intel® M2102A is a high speed 1K x 1 RAM specified over the -55°C to +125°C temperature range. The RAM uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The Intel® M2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . −65°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . −0.6V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter		Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
I_{LI}	Input Load Current				10	μA	V_{IN} = 0 to 5.5V
I_{LOH}	Output Leakage Current				10	μA	$\overline{CE}$ = Min. V_{IH} , V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current	M2102A-4			-50	μA	$\overline{CE}$ = Min. V_{IH} , V_{OUT} = 0.45V
		M2102A-6			-100		
I_{CC1}	Power Supply Current			30	60	mA	All Inputs = 5.5V, Data Out Open, T_A = 25°C
I_{CC2}	Power Supply Current				70	mA	All Inputs = 5.5V, Data Out Open, T_A = -55°C
V_{IL}	Input "Low" Voltage	M2102A-4	-0.5		0.8	V	
		M2102A-6	-0.5		0.65		
V_{IH}	Input "High" Voltage	M2102A-4	2.0		V_{CC}	V	
		M2102A-6	2.2		V_{CC}		
V_{OL}	Output "Low" Voltage				0.45	V	M2102A-4 I_{OL} = 2.1mA / M2102A-6 I_{OL} = 1.9mA
V_{OH}	Output "High" Voltage		2.2			V	I_{OH} = 100μA

NOTE 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	M2102A-4 Limits (ns)		M2102A-6 Limits (ns)	
		Min.	Max.	Min.	Max.
READ CYCLE					
t_{RC}	Read Cycle	450		650	
t_A	Access Time		450		650
t_{CO}	Chip Enable to Output Time		230		400
t_{OH1}	Previous Read Data Valid with Respect to Address	40		50	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0	
WRITE CYCLE					
t_{WC}	Write Cycle	450		650	
t_{AW}	Address to Write Setup Time	20		200	
t_{WP}	Write Pulse Width	300		400	
t_{WR}	Write Recovery Time	0		50	
t_{DW}	Data Setup Time	300		450	
t_{DH}	Data Hold Time	0		100	
t_{CW}	Chip Enable to Write Setup Time	300		550	

A.C. CONDITIONS OF TEST

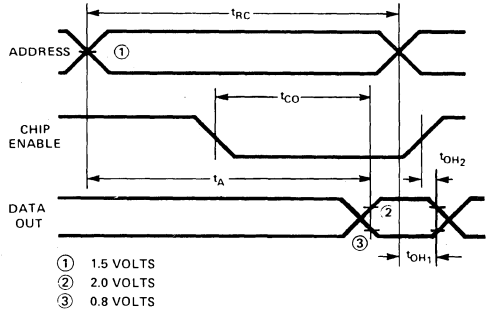
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1 MHz

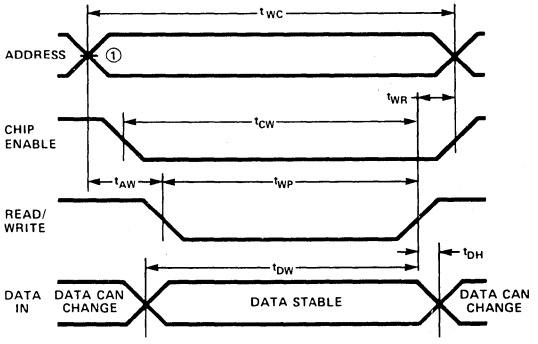
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25° C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

2104, 2104-2, 2104-4

4096 x 1 BIT DYNAMIC RAM

	2104-2	2104-4	2104
Max. Access Time (ns)	250	300	350
Read, Write Cycle (ns)	375	425	500
Read-Modify-Write Cycle (ns)	515	595	700

- **Highest Density 4K RAM— Industry Standard 16 Pin Package**
- **Low Standby Power**
- **All Inputs Including Clocks TTL Compatible**
- **Standard Power Supplies +12V, +5V, −5V**
- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion— Chip Select**
- **Output is Three State, TTL Compatible; Data is Latched and Valid into Next Cycle**

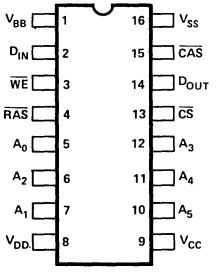
The Intel®2104 is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density. The 2104 uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2104 allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

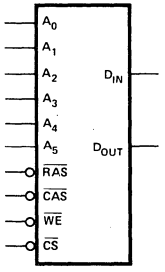
The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104 on 6 address input pins. The two 6 bit address words are latched into the 2104 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2 milliseconds.

PIN CONFIGURATION



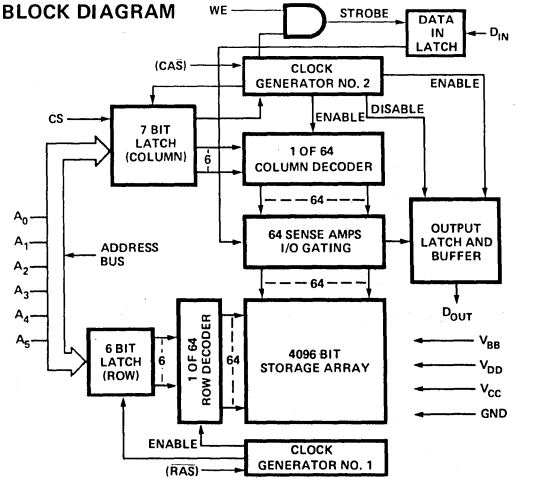
LOGIC DIAGRAM



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} ..... +25V to -0.3V
Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} ..... +20V to -0.3V
Power Dissipation 1.25W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics [1]

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Input Load Current (any input)			10	µA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state			10	µA	Chip deselected
I_{DD1}[3]	V_{DD} Supply Current		1	2	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected.
I_{DDAV}[3]	Average V_{DD} Current: 2104-4		46	60	mA	Cycle time = Min. T_A = 25°C
	2104, 2104-2		45	59	mA	t_{RP} = Min.
I_{CC1}[4]	V_{CC} Supply Current when deselected			10	µA	
I_{BB}[3]	Average V_{BB} Current			75	µA	
V_{IL}	Input Low Voltage (any input)	-1.0		0.6	V	
V_{IH}	Input High Voltage (any input)	2.4		V_{CC}+1	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5.0mA

A.C. Characteristics [1]

T_A=0°C to 70°C, V_{DD}=12V ±5%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

Capacitance [5] T_A = 25°C

Symbol	Test	Plastic And Ceramic Pkg. Typ.	Max.	Unit	Conditions
C_{AD}	Address Capacitance		10	pF	V_{IN} = V_{SS}
C_C	$\overline{CAS}$, $\overline{RAS}$, $\overline{CS}$ Capacitance		7	pF	V_{IN} = V_{SS}
C_{OUT}	Data Output Capacitance		8	pF	V_{OUT} = 0V
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance		10	pF	V_{IN} = V_{SS}

Notes:
1. All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} current flows to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I\Delta t}{\Delta V}$$ with the current equal to a constant 20mA.

A.C. Characteristics [1]

T_A=0°C to 70°C, V_{DD}=12V ±5%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES

Symbol	Parameter	2104 Min.	2104 Max.	2104-2 Min.	2104-2 Max.	2104-4 Min.	2104-4 Max.	Unit
t_{REF}	Time Between Refresh		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	150		125		125		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	110	2000	80	2000	90	2000	ns
t_{AS}	Address or $\overline{CS}$ Set-Up Time	0		0		0		ns
t_{AH}	Address or $\overline{CS}$ Hold Time	100		80		80		ns
t_{AR}	$\overline{RAS}$ to Address Hold Time	250		180		210		ns
t_{CRL}[3]	$\overline{RAS}$ to $\overline{CAS}$ Trailing Edge Lead Time	-50	+50	-40	+40	-50	+50	ns
t_{OFF}	Output Buffer Turn Off Delay	0	100	0	100	0	100	ns
t_{CAC}[4]	Access Time From $\overline{CAS}$		200		150		170	ns
t_{RAC}[4]	Access Time From $\overline{RAS}$		350		250		300	ns

READ CYCLE

Symbol	Parameter	2104 Min.	2104 Max.	2104-2 Min.	2104-2 Max.	2104-4 Min.	2104-4 Max.	Unit
t_{CYC}[5]	Random Read or Write Cycle Time	500		375		425		ns
t_{CPW}	$\overline{CAS}$ Pulse Width	200	10000	150	10000	170	10000	ns
t_{RPW}	$\overline{RAS}$ Pulse Width	350	10000	250	10000	300	10000	ns
t_{RSH}	$\overline{RAS}$ Hold Time	200		150		170		ns
t_{CSH}	$\overline{CAS}$ Hold Time	350		250		300		ns
t_{RCH}	Read Command Hold Time	80		80		80		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns

WRITE CYCLE

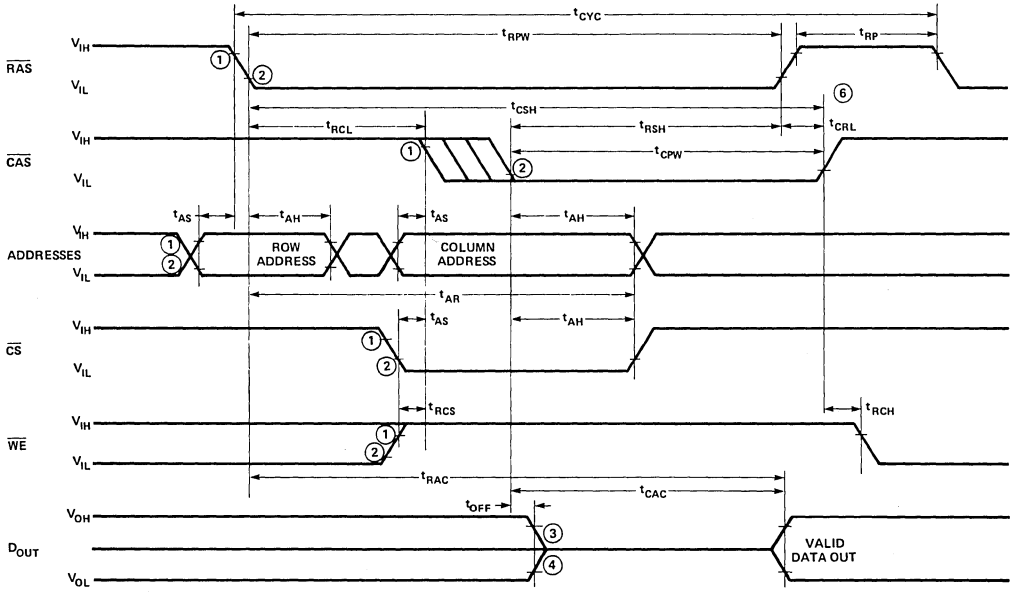
Symbol	Parameter	2104 Min.	2104 Max.	2104-2 Min.	2104-2 Max.	2104-4 Min.	2104-4 Max.	Unit
t_{CYC}[5]	Random Read or Write Cycle Time	500		375		425		ns
t_{CPW}	$\overline{CAS}$ Pulse Width	200	10000	150	10000	170	10000	ns
t_{RPW}	$\overline{RAS}$ Pulse Width	350	10000	250	10000	300	10000	ns
t_{RSH}	$\overline{RAS}$ Hold Time	200		150		170		ns
t_{CSH}	$\overline{CAS}$ Hold Time	350		250		300		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	200		150		170		ns
t_{WCH}	Write Command Hold Time	150		110		130		ns
t_{WP}	Write Command Pulse Width	200		150		170		ns
t_{DS}	Data In Set-Up Time	0		0		0		ns
t_{DH}	Data In Hold Time	200		150		170		ns

Notes:

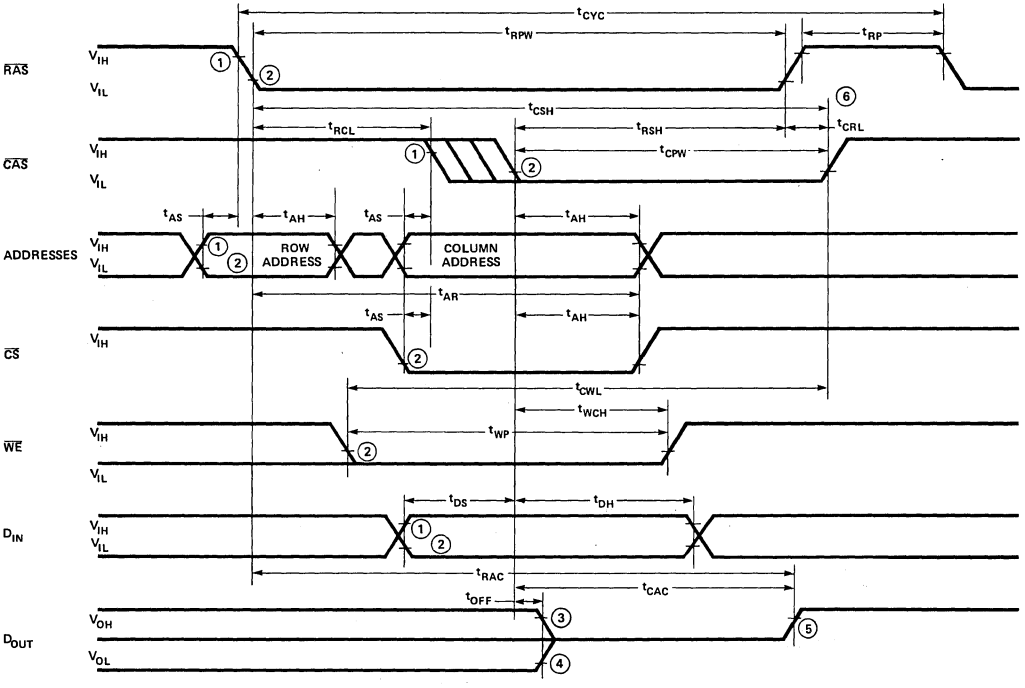
1. All voltages referenced to V_{SS}.
2. $\overline{CAS}$ must remain at V_{IH} a minimum of t_{RCLMIN} after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before t_{RCL} of $t_{RAC} - t_T - t_{CAC}$ as described in the Applications Information on page 2-49.
3. t_{CRL} is measured from $\overline{RAS}$ to $\overline{CAS}$.
4. Load = 1 TTL and 50pF. See Application Information — Read Cycle section for relations between access time and t_{RCL}.
5. The minimum cycle timing does not allow for t_T or skews.

Waveforms

READ CYCLE



WRITE CYCLE



See page 2-48 for NOTES.

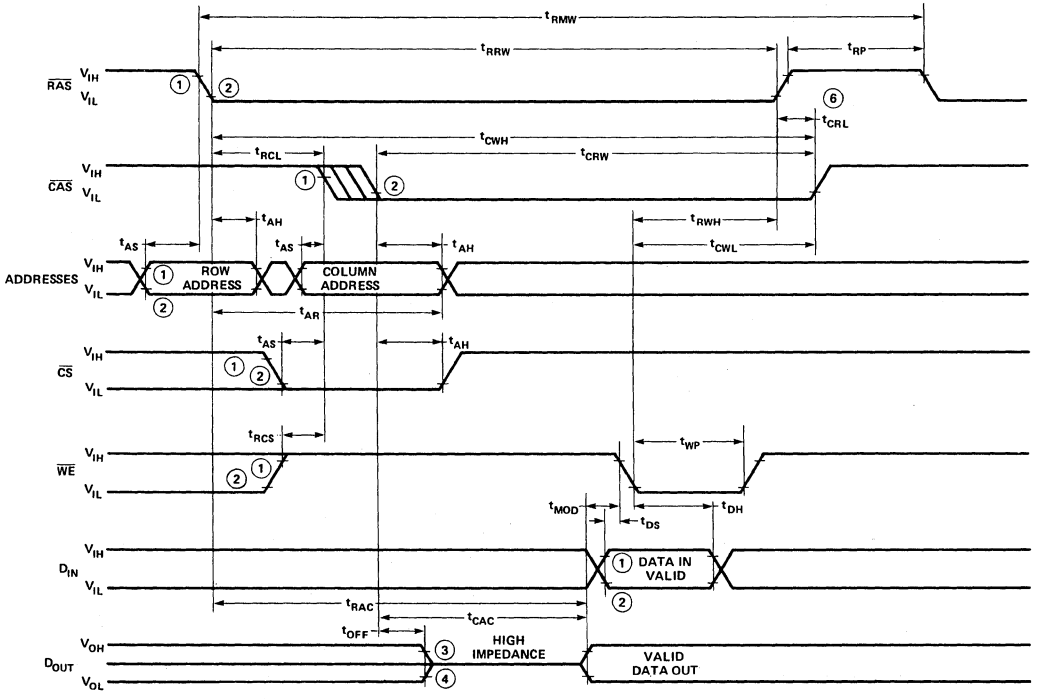
A.C. Characteristics T_A=0°C to 70°C, V_{DD}=12V ±5%, V_{CC}=5V±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ MODIFY WRITE CYCLE

Symbol	Parameter	2104 Min.	2104 Max.	2104-2 Min.	2104-2 Max.	2104-4 Min.	2104-4 Max.	Unit
t_{RMW}	Read Modify Write Cycle Time	700		515		595		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	400	10000	290	10000	340	10000	ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	550	10000	390	10000	470	10000	ns
t_{RWH}	RMW Cycle $\overline{RAS}$ Hold Time	200		150		170		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	550		390		470		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	200		150		170		ns
t_{WP}	Write Command Pulse Width	200		150		170		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{MOD}	Modify Time	0		0		0		ns
t_{DS}	Data In Set-Up Time	0		0		0		ns
t_{DH}	Data In Hold Time	200		150		170		ns

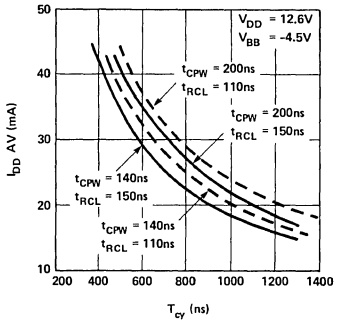
Waveforms

READ MODIFY WRITE CYCLE

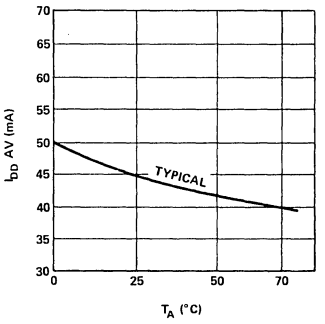


Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. If $\overline{WE}$ goes low while $\overline{CAS}$ is low, D_{OUT} could go to either V_{OL} or V_{OH} after t_{CAC}. D_{OUT} will go to V_{OH} as shown on page 4 (Write Cycle Waveforms) if $\overline{WE}$ goes low before $\overline{CAS}$ goes low. In a Read-Modify-Write cycle, D_{OUT} is data read and does not change during the Modify-Write portion of the cycle.
6. For minimum cycle timing, t_{CRL} must be -0 to +40 ns for 2104-2 and -0 to +50 ns for 2104 and 2104-4.

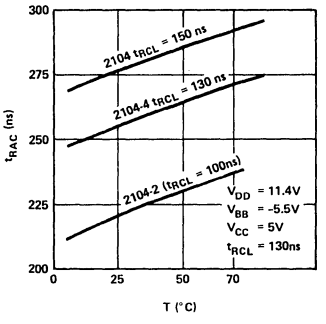
TYPICAL I_{DD} AV VS. CYCLE TIME



I_{DD} AV VS. TEMPERATURE



TYPICAL ACCESS TIME VS. TEMPERATURE



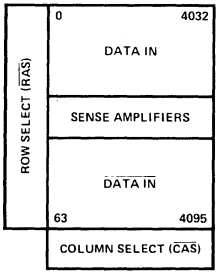
Applications

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, $\overline{CAS}$, strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select ($\overline{CS}$) which enables the data out buffer.

An address map of the 2104 is shown below. Address "0" corresponds to all addresses at V_{IL}. Note that data is stored in half of the memory as a logic inversion of the data presented at the input pin as shown. This inversion is completely transparent to the user (i.e., data stored in memory as a "1" or "0" at the input will when subsequently accessed, appear as a "1" or "0" respectively at the output).

2104 Address Map



DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until $\overline{CAS}$ becomes valid.

Note that Chip Select ($\overline{CS}$) does not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in system access time since the decode time for chip select does not enter into the calculation for access time.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104 convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104 system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during $\overline{CAS}$. The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid until a subsequent $\overline{CAS}$ is given to the device by a Read, Write, Read-Modify-Write or Refresh cycle. Data-out goes to a high impedance state for all non-selected devices.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCL} + t_T + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe lead time, t_{RCL}, and transition time, t_T, are system dependent timing parameters. For example, substituting the device parameters of the 2104-4 and assuming a TTL level transition time of 5ns yields:

3. $t_{ACC} = t_{RAC}$ = 300ns for 90nsec $\leqslant t_{RCL} \leqslant$ 125nsec

OR

4. $t_{ACC} = t_{RCL} + t_T + t_{CAC} = t_{RCL}$ +175ns for $t_{RCL} >$ 125ns.

Note that if 90 nsec $\leqslant t_{RCL} \leqslant$ 125 nsec, device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCL} >$ 125 nsec, access time is determined by equation 4. This 35ns interval (shown in the t_{RCL} inequality in equation 3) in which the falling edge of CAS can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This allowance for a t_{RCL} skew is designed in at the device level to allow minimum access times to be achieved in practical system designs.

WRITE CYCLE

A Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low before or during $\overline{CAS}$. If Write Enable goes low at or before $\overline{CAS}$ goes low, the input data must be valid at or before the falling edge of $\overline{CAS}$. D_{OUT} will go to V_{OH} as shown

on page 4 (Write Cycle) if $\overline{WE}$ goes low before $\overline{CAS}$ goes low. If Write Enable goes low after $\overline{CAS}$, data in must be valid at or before the falling edge of $\overline{WE}$. Data out goes to a high impedance state following the leading edge of $\overline{CAS}$. If $\overline{WE}$ goes low while $\overline{CAS}$ is low, D_{OUT} could go to either V_{OL} or V_{OH} after t_{CAC}.

READ-MODIFY-WRITE CYCLE

A Read-Modify-Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low after access time, t_{ACC}, with $\overline{RAS}$ and $\overline{CAS}$ low. Data in must be valid at or before the falling edge of $\overline{WE}$. In a read-modify-write cycle D_{OUT} is data read and does not change during the modify-write portion of the cycle.

$\overline{CAS}$ ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104 by performing a $\overline{CAS}$ Only Cycle. Receipt of a $\overline{CAS}$ without a $\overline{RAS}$ deselects the 2104 and forces the Data Output to the high-impedance state. This places the 2104 in its lowest power, standby condition as will be discussed in the POWER DISSIPATION section below. The cycle timing and $\overline{CAS}$ timing should be just as if a nomal $\overline{RAS}$/$\overline{CAS}$ cycle was being performed.

CHIP SELECTION/DESELECTION

The 2104 is selected by driving $\overline{CS}$ low during a Read, Write, or Read-Modify-Write cycle. A device is deselected by 1) driving $\overline{CS}$ high during a Read, Write, or Read-Modify-Write cycle or 2) performing a $\overline{CAS}$ Only cycle independent of the state of $\overline{CS}$.

REFRESH CYCLES

Each of the 64 rows internal to the 2104 must be refreshed every 2 msec to maintain data. Any data cycle (Read, Write, Read-Modify-Write) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell.

$\overline{RAS}$/$\overline{CAS}$ TIMING

The device clocks, $\overline{RAS}$ and $\overline{CAS}$, contol operation of the 2104. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RPW} and t_{CPW} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low, must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP}, has been met.

The timing relationship of the leading edges of $\overline{RAS}$ and $\overline{CAS}$ is defined by t_{RCL} and is discussed in the READ CYCLE section above. The trailing edge relationship is defined by t_{RSH}, t_{CSH}, and t_{CRL}. The first two parameters define the minimum time during a memory cycle that $\overline{RAS}$ and $\overline{CAS}$ are both low (minimum hold times). Both the minimum clock widths and hold times must be met for proper operation.

For example, using t_T = 5ns and the 2104-4 device parameters: t_{RCL} = 90ns, t_{RPW} = 300nsec, and t_{CPW} = 170nsec; the trailing edge of $\overline{CAS}$ would occur at time (t) where:

$$t = t_{RCL}+t_T+t_{CPW} = 90ns + 5ns + 170ns$$
$$= 265ns$$

however, t_{CSH} = 300ns, and, therefore, t_{CPW} would need to be lengthened such that:

$$t_{CPW} \text{ (actual)} = 170ns + (300ns - 265ns) = 205ns$$

in order to meet the minimum t_{CSH} requirement.

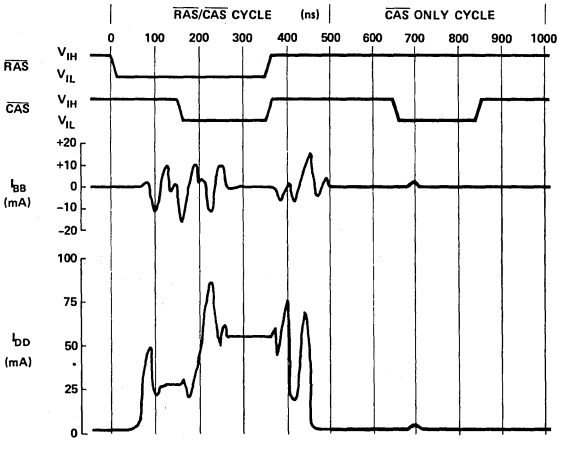
The third parameter, t_{CRL}, defines the lead (−) or lag (+) time allowable for $\overline{CAS}$ with respect to $\overline{RAS}$. If all minimum timing requirements for $\overline{RAS}$ and $\overline{CAS}$ are met, the $\overline{CAS}$ trailing edge may lead the $\overline{RAS}$ trailing edge by up to 10ns or lag by up to 70ns. In a memory cycle with all minimum timing specifications used, $\overline{CAS}$ may lag $\overline{RAS}$ but cannot lead $\overline{RAS}$ since t_{CSH} would be violated if $\overline{CAS}$ led $\overline{RAS}$.

POWER DISSIPATION

Operating

The power dissipation of a continuously operating 2104 device is the sum of $V_{DD} \times I_{DDAV}$ and $V_{BB} \times I_{BB}$. For a cycle time of 425ns (including a t_{RP} of 125ns) the typical power dissipation is 552mW.

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}$/$\overline{CAS}$ cycle and a $\overline{CAS}$ only cycle. It is evident from examination of the current waveforms that the major portion of the device power dissipation is the $V_{DD} \times I_{DDAV}$ component. Since the average value of I_{DD} is used to compute the power dissipation and I_{DD} is high only while $\overline{RAS}$ and $\overline{CAS}$ are low, minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are preferred even with long cycle times to minimize power dissipation.



TYPICAL SUPPLY CURRENTS VS. TIME

STANDBY-REFRESH ONLY

The standby power-refresh only is calculated by the following equation:

5. $P_{REF} = P_{OP} \times (64 \frac{t_{CYC}}{t_{REF}}) + P_{SB} (1\text{-}64 \frac{t_{CYC}}{t_{REF}})$

Where: P_{REF} = Standby power-refresh only.
P_{OP} = Power dissipation-continuous operation.
t_{CYC} = Cycle time for a Refresh cycle.
t_{REF} = Time between refresh.
P_{SB} = Standby power dissipation.

The standby power dissipation P_{SB} is given by:

6. $P_{SB} = V_{DD} \times I_{DD1} + V_{BB} \times I_{BB}$.

For example, in the 2104-4, the typical power dissipated in a standby-refresh only mode with the device deselected ($\overline{CS}$ high) is 19mW. If the device is selected ($\overline{CS}$ low) during a refresh cycle, the typical power dissipated is 31mW. This is the result of the internal output buffer circuitry being turned on. Since needless power is dissipated for this condition, it is recommended that the device be deselected during standby-refresh only operation.

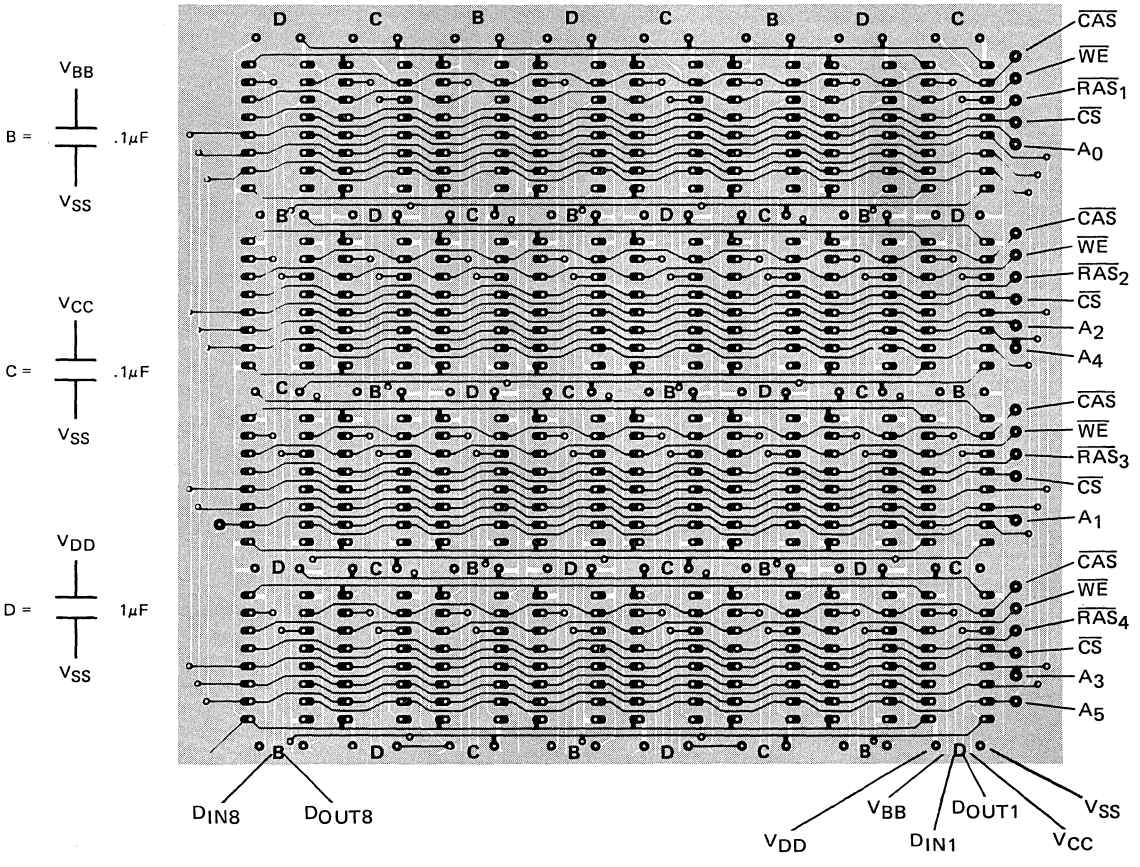
Note that when calculating the standby power for a 2104 memory system it is not necessary to include the power dissipated by TTL to MOS level converters. These converters are incorporated internally to the 2104 and are included in the previous power calculations.

SYSTEM LAYOUT AND DECOUPLING

A two sided memory array layout is shown below.

Decoupling is indicated by a "D" for V_{DD} to V_{SS} and "B" for V_{BB} to V_{SS}. I_{DD} and I_{BB} current surges at $\overline{RAS}$ and $\overline{CAS}$ make adequate decoupling of these supplies important. It is recommended that 1.0μF high frequency, low inductance capacitors be used between V_{DD} and V_{SS} on double sided boards. 0.1μF capacitors can be used between V_{BB} and V_{SS}. V_{CC} to V_{SS} decoupling is indicated by a "C" and 0.1μF capacitors are recommended. For each 36 devices a 100μF tantalum or equivalent capacitor should be placed from V_{DD} to V_{SS} near the array. An equal or slightly smaller bulk capacitor should be placed between V_{BB} and V_{SS} on the memory card.

Note that all power lines (including V_{SS}) are grided both horizontally and vertically at each memory device. This minimizes the power distribution impedance and enhances the effect of the decoupling capacitors.



Two Sided Layout for 16K x 8 Memory

2107A

4096 x 1 BIT DYNAMIC RAM

Product	2107A-1	2107A	2107A-4	2107A-5
Access Time	280 ns	300 ns	350 ns	420 ns

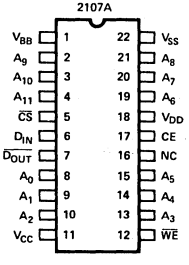
- **Low Cost Per Bit**
- **Low Standby Power**
- **Easy System Interface**
- **Only One High Voltage Input Signal—Chip Enable**
- **Low Level Address, Data, Write Enable, Chip Select Inputs**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion: Chip Select Input Lead**
- **Fully Decoded: On Chip Address Decode**
- **Output is Three State and TTL Compatible**
- **Ceramic and Plastic 22-Pin DIPs**

The Intel 2107A is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107A uses dynamic circuitry which reduces the operation and standby power dissipation.

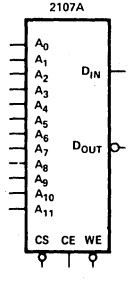
Reading information from the memory is non-destructive. Refreshing is accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107A is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies.

PIN CONFIGURATION



LOGIC SYMBOL

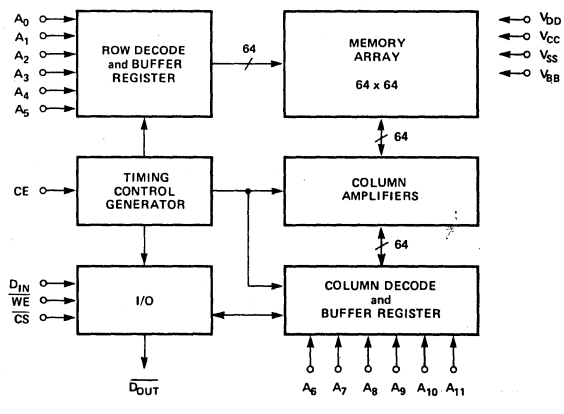


PIN NAMES

D_{IN}	DATA INPUT	CE	CHIP ENABLE
A_0-A_{11}	ADDRESS INPUTS*	$\overline{D_{OUT}}$	DATA OUTPUT
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	NC	NOT CONNECTED

*Refresh Addresses A_0-A_5.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to 70°C

Storage Temperature ..... −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} ..... +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} ..... +20V to −0.3V

Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB}[1] = -5V ± 5%, V_{SS} = 0V, unless otherwise notes.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	μA	CE = -1V to +.8V or $\overline{CS}$ = 3.5V, V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		.1	100	μA	CE = -1V to +.8V
I_{DD2}	V_{DD} Supply Current during CE on[5]		14	22	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\ AV}$	Average V_{DD} Supply Current	(See Table 1)				T_A = 25°C, Fig. 1,3
I_{CC1}	V_{CC} Supply Current during CE off		.01	10	μA	CE = -1V to +.8V
I_{CC2}	V_{CC} Supply Current during CE on		5	10	mA	CE = V_{IHC}, T_A = 25°C
$I_{CC\ AV}$	Average V_{CC} Supply Current	(See Table 1)				T_A = 25°C, Fig. 2,4
I_{BB}	V_{BB} Supply Current		1	100	μA	
V_{IL}	Input Low Voltage[4]	−1.0		0.8	V	
V_{IH}	Input High Voltage[4]	3.5		V_{CC} +1	V	
V_{ILC}	CE Input Low Voltage[4]	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD} −1		V_{DD} +1	V	
V_{OL}	Output Low Voltage[4]	0.0		0.45	V	I_{OL} = 1.7mA, Fig. 6
V_{OH}	Output High Voltage[4]	2.4		V_{CC}	V	I_{OH} = -100μA, Fig. 5

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. Referenced to V_{SS} unless otherwise noted.
5. For 2107A-4 and 2107A-5 I_{DD2} is 25mA max.

A. C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameters	2107A		2107A-1		2107A-4		2107A-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF} [1]	Time Between Refresh		2		1		2		2	ms
t_{AC}	Address to CE Set Up Time	0		0		0		0		ns
t_{AH}	Address Hold Time	100		100		100		100		ns
t_{CC}	CE Off Time	180		100		200		250		ns
t_T	CE Transition Time		50		50		50		50	ns
t_{CF}	CE Off to Output High Impedance State	0		0		0		0		ns

READ CYCLE

Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{RCY} [2]	Read Cycle Time	500		420		570		690		ns
t_{CER}	CE On Time During Read	280	3000	280	3000	330	3000	400	300	ns
t_{CO}	CE Output Delay		280		260		330		400	ns
t_{ACC} [3]	Address to Output Access		300		280		350		420	ns
t_{WL}	CE to $\overline{WE}$ Low	0		0		0		0		ns
t_{WC}	$\overline{WE}$ to CE on	0		0		0		0		ns

WRITE CYCLE

Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{WCY} [2]	Write Cycle Time	700		550		840		970		ns
t_{CEW}	CE Width During Write	480	3000	410	3000	600	3000	680	3000	ns
t_W	$\overline{WE}$ to CE Off	340		250		400		450		ns
t_{CW}	CE to $\overline{WE}$ High	300		250		—		—		ns
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		0		ns
t_{CD} [4]	CE to D_{IN} Set Up		50		50		50		50	ns
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns
t_{WP}	$\overline{WE}$ Pulse Width	150		150		200		200		ns
t_{WW} [5]	$\overline{WE}$ Wait	0		0		170		200		ns
t_{WC}	$\overline{WE}$ to CE On	0		0		0		0		ns

Capacitance [6] $T_A = 25°C$

Symbol	Test	Plastic And Ceramic Pkg. Typ.	Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$, $\overline{WE}$, D_{IN}	3	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	3	6	pF	$V_{OUT} = 0V$

Notes:
1. For plastic 2107A-4 and 2107A-5 $t_{REF} = 1mS$.
2. $t_T = 20ns$
3. $C_{LOAD} = 50$ pf; Load = 1 TTL; Ref = 2.0V for high, 0.8V for low; $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$.
4. t_{CD} applies only when $t_W > t_{CEW} - 50ns$.
5. The 2107A and 2107A-1 should not be operated with t_{WW} in the 50 to 170 ns range.
6. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with the current equal to a constant 20mA.

D.C. Characteristics

FIGURE 1
I_{DD} AVERAGE VS. TEMPERATURE

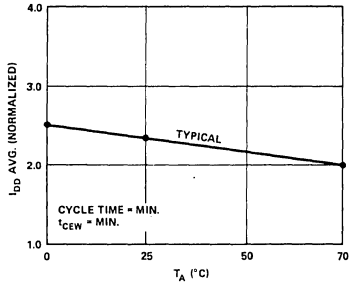


FIGURE 2
I_{CC} AVERAGE VS. TEMPERATURE

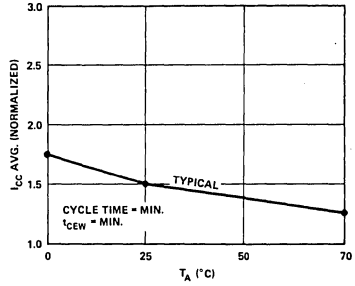


FIGURE 3
TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

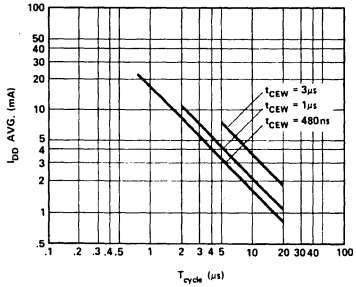


FIGURE 4
TYPICAL I_{CC} AVERAGE VS. CYCLE TIME

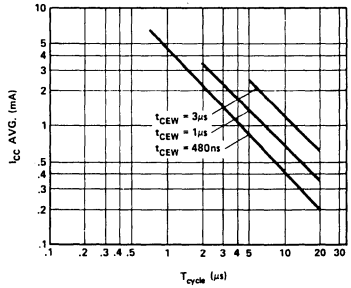


FIGURE 5
TYPICAL I_{OH} VS. V_{OH}

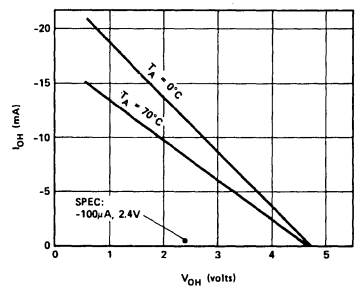


FIGURE 6
TYPICAL I_{OL} VS. V_{OL}

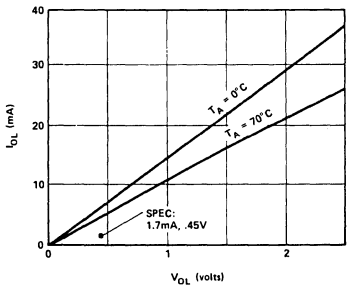


FIGURE 7
TYPICAL REFRESH VS. TEMPERATURE

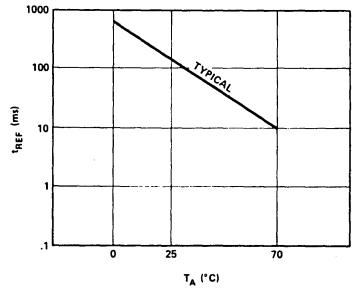


FIGURE 8
TYPICAL ACCESS TIME VS. TEMPERATURE

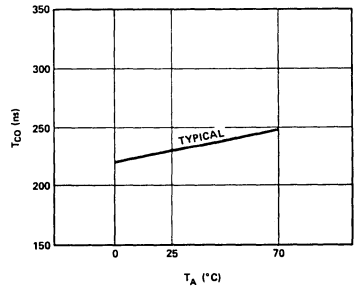


Table 1. I_{DDAV} and I_{CCAV} Characteristics.

Product	I_{DDAV} (Typ)	I_{DDAV} (Max)	I_{CCAV} (Typ)	I_{CCAV} (Max)	Cycle	t_{CEW}
2107A	23mA	34mA	6mA	10mA	700ns	480ns
2107A-1	28mA	38mA	8mA	12mA	550ns	410ns
2107A-4	22mA	33mA	5mA	9mA	840ns	600ns
2107A-5	18mA	28mA	4mA	8mA	970ns	680ns

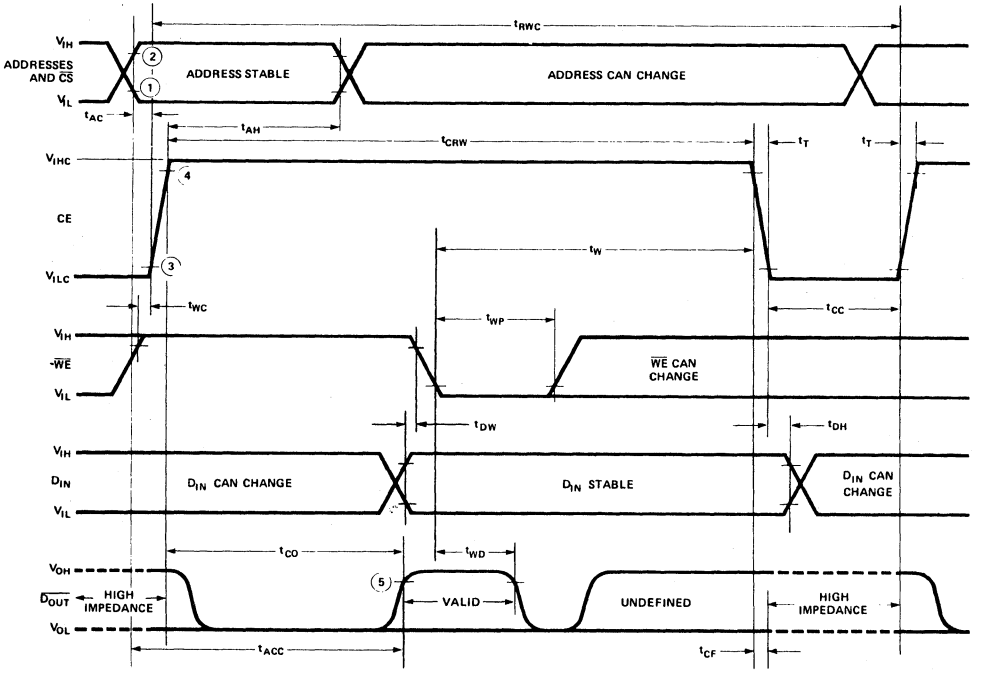
Read Modify Write Cycle

Symbol	Parameters	2107A		2107A-1		2107A-4		2107A-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWC}[1]	Read Modify Write (RMW) Cycle Time	840		670		970		1140		ns
t_{CRW}[2]	CE Width During RMW	620	3000	530	3000	730	3000	850	3000	ns
t_{WC}	$\overline{WE}$ to CE on	0		0		0		0		ns
t_W	$\overline{WE}$ to CE off	340		250		400		450		ns
t_{WP}	$\overline{WE}$ Pulse Width	150		150		200		200		ns
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		0		ns
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns
t_{CO}	CE to Output Delay		280		260		330		400	ns
t_{ACC}[3]	Access Time		300		280		350		420	ns
t_{WD}	$\overline{D_{OUT}}$ Valid After $\overline{WE}$	0		0		0		0		ns

Notes: 1. t_T = 20ns

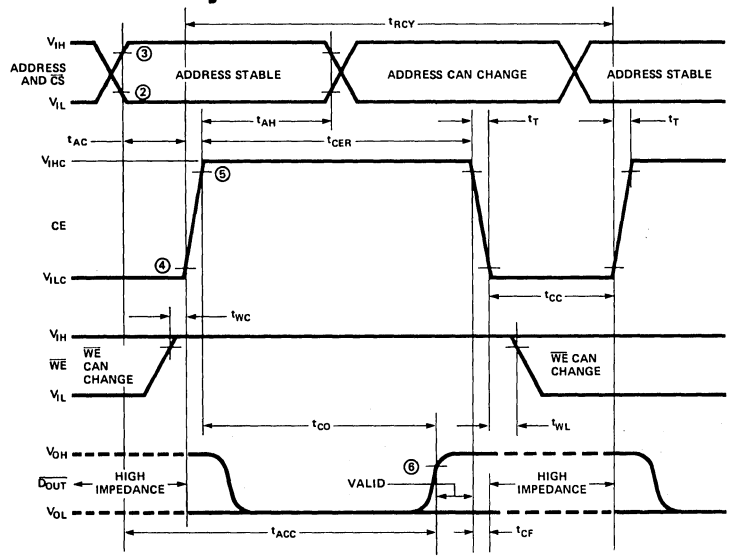
2. $t_{CRW} - t_W = t_{CO}$

3. C_{LOAD} = 50 pf; Load = One TTL Gate; Ref = 2.0V for High, 0.8V for low; $t_{ACC} = t_{AC} + t_{CO}$ + 1 TTL

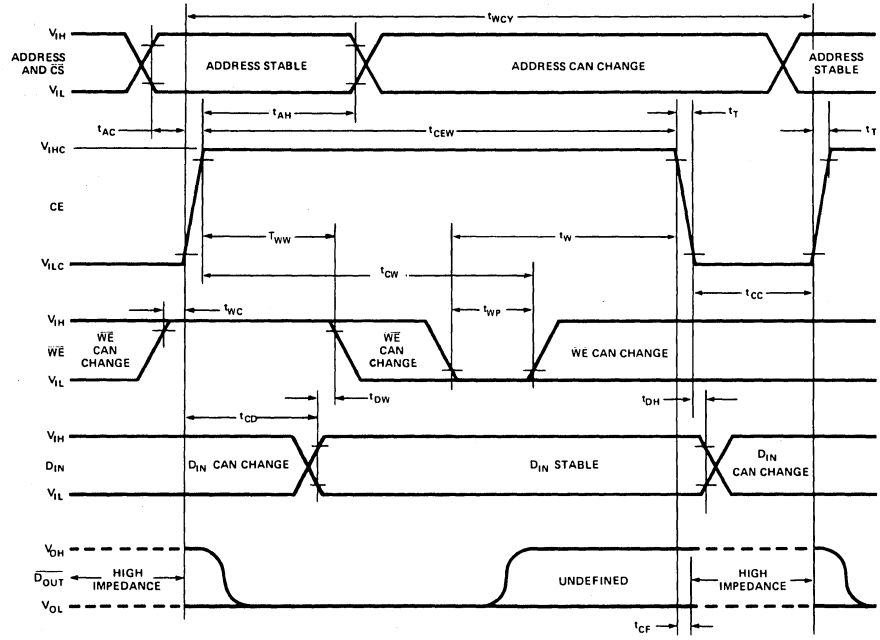


NOTES:
1. V_{SS} + 1.5V is the reference level for measuring timing of the address CS, WE, and D_{IN}.
2. V_{SS} + 3.0V is the reference level for measuring timing of the address, CS, WE, and D_{IN}.
3. V_{SS} + 2.0V is the reference level for measuring timing of CE.
4. V_{DD} -2V is the reference level for measuring timing of CE.
5. V_{SS} + 2.0V is the reference level for measuring the timing of D_{OUT}.

Read and Refresh Cycle [1]



Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{SS} + 1.5V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{SS} + 3.0V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} + 2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} + 2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.

4096 BIT DYNAMIC RAM

	2107B	2107B-4	2107B-6
Access Time	200ns	270ns	350ns
Read,Write Cycle	400ns	470ns	800ns
RMW Cycle	520ns	590ns	960ns

- **Low Cost Per Bit**
- **Low Standby Power**
- **Easy System Interface**
- **Only One High Voltage Input Signal — Chip Enable**
- **TTL Compatible — All Address, Data, Write Enable, Chip Select Inputs**
- **Refresh Period — 2ms for 2107B, 2107B-4, 1ms for 2107B-6**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion — Chip Select Input Lead**
- **Fully Decoded — On Chip Address Decode**
- **Output is Three State and TTL Compatible**
- **Industry Standard 22-Pin Configuration**

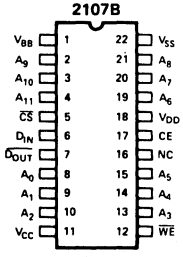
The Intel®2107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107B uses dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 2107A.

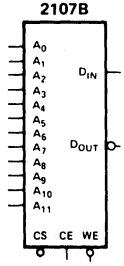
PIN CONFIGURATION

2107B



LOGIC SYMBOL

2107B

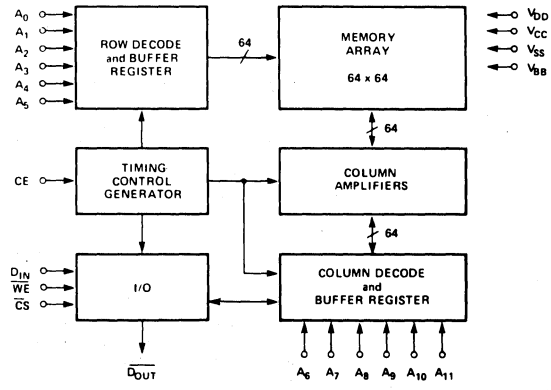


PIN NAMES

A_0-A_{11}	ADDRESS INPUTS*	V_{BB}	POWER (-5V)
CE	CHIP ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	V_{DD}	POWER (+12V)
D_{IN}	DATA INPUT	V_{SS}	GROUND
$\overline{D_{OUT}}$	DATA OUTPUT	$\overline{WE}$	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A_0-A_5.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . . +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} . . . . . +20V to −0.3V

Power Dissipation 1.25W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±10%, V_{BB} [1] = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$ CE = V_{ILC} or V_{IHC}
I_{LC}	Input Load Current		.01	2	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200[5]	μA	CE = -1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on			60	mA	CE = V_{IHC}, $\overline{CS}$ = V_{IL}
$I_{DD\ AV}$	Average V_{DD} Current		38	54	mA	$\overline{CS}$ = V_{IL} ; T_A = 25°C; Min cycle time, Min t_{CE}
I_{CC1}[4]	V_{CC} Supply Current during CE off		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB}	V_{BB} Supply Current		5	100	μA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	t_T = 20ns
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	t_T = 20ns
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.
5. Maximum I_{DD1} for 2107B-6 is 250 μA.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	2107B		2107B-4		2107B-6		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Time Between Refresh		2		2		1	ms	
t_{AC}	Address to CE Set Up Time	0		0		10		ns	3
t_{AH}	Address Hold Time	100		100		100		ns	
t_{CC}	CE Off Time	130		130		380		ns	
t_T	CE Transition Time	10	40	10	40	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		0		0		ns	

READ CYCLE

Symbol	Parameter	2107B		2107B-4		2107B-6		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		800		ns	4
t_{CE}	CE On Time	230	4000	300	4000	380	4000	ns	
t_{CO}	CE Output Delay		180		250		320	ns	5
t_{ACC}	Address to Output Access		200		270		350	ns	6
t_{WL}	CE to $\overline{WE}$	0		0		0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		ns	

WRITE CYCLE

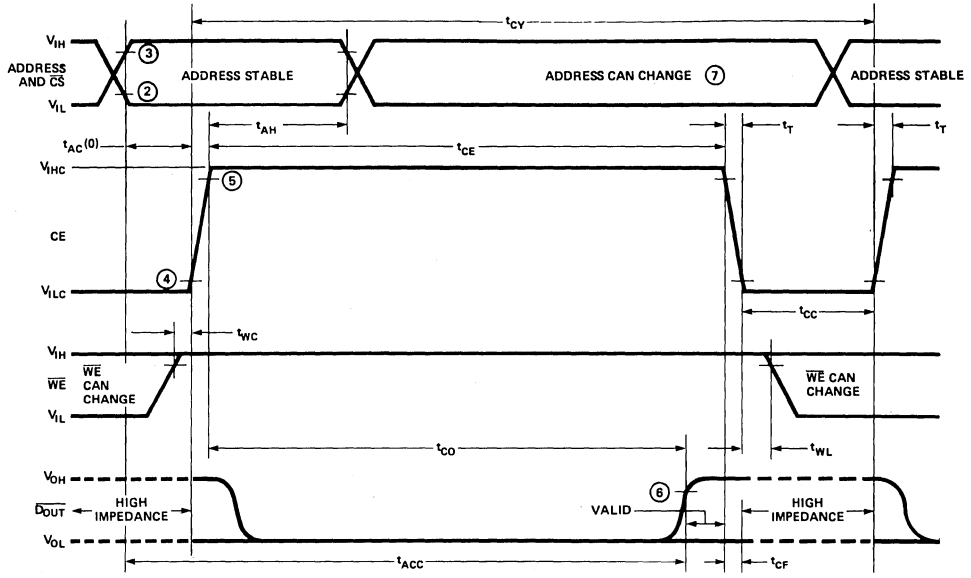
Symbol	Parameter	2107B		2107B-4		2107B-6		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		800		ns	4
t_{CE}	CE On Time	230	4000	300	4000	380	4000	ns	
t_W	$\overline{WE}$ to CE Off	150		150		200		ns	
t_{CW}	CE to $\overline{WE}$	150		150		150		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		ns	1
t_{DH}	D_{IN} Hold Time	0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		100		ns	

Capacitance[2] $T_A = 25°C$

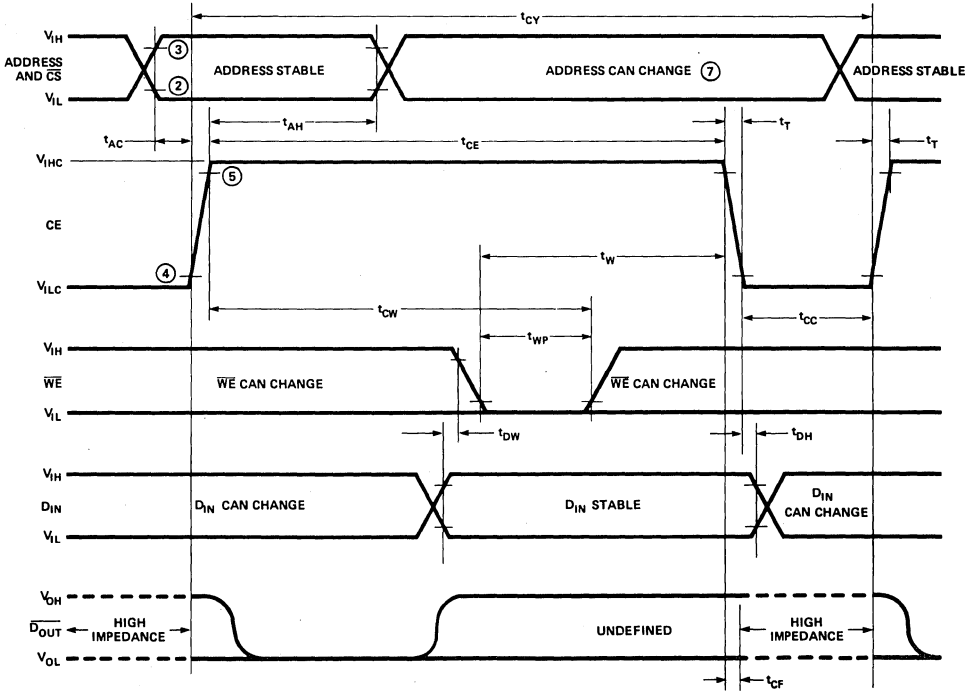
Symbol	Test	Plastic And Ceramic Pkg. Typ.	Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$	4	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	$V_{OUT} = 0V$
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	8	10	pF	$V_{IN} = V_{SS}$

Notes: 1. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
2. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation.
$C = \frac{I\Delta t}{\Delta V}$ with the current equal to a constant 20mA.
3. t_{AC} is measured from end of address transition.
4. $t_T = 20ns$
5. $C_{LOAD} = 50pF$, Load = One TTL Gate, Ref = 2.0V.
6. $t_{ACC} = t_{AC} + t_{CO} + 1t_T$

Read and Refresh Cycle [1]



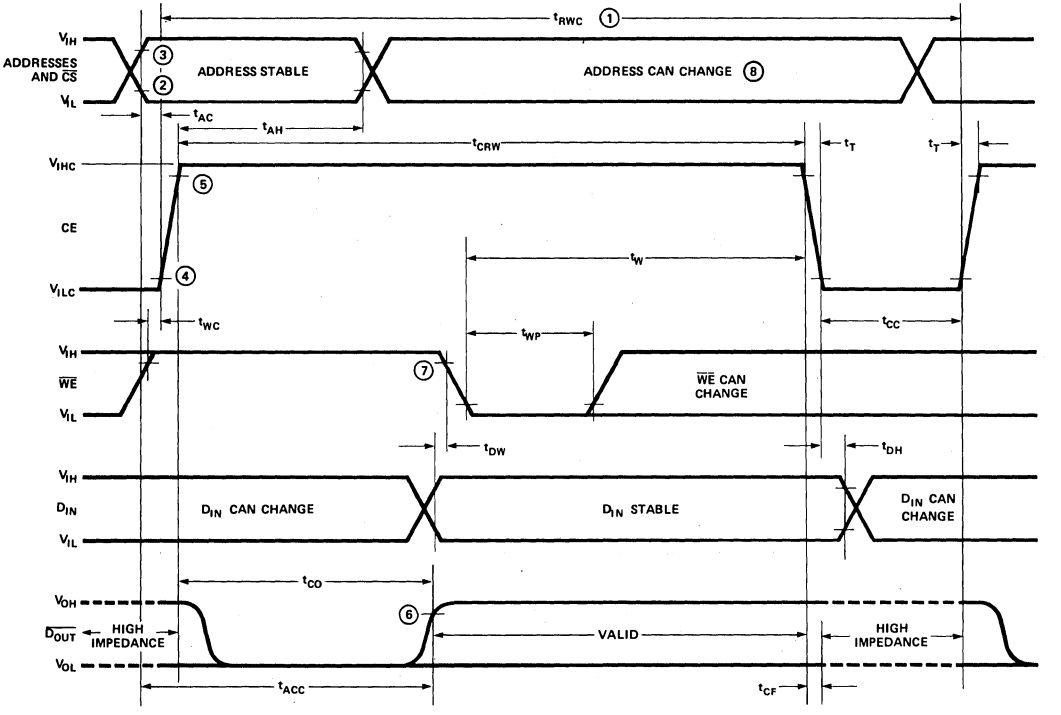
Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $D_{\overline{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Read Modify Write Cycle[1]

Symbol	Parameter	2107B		2107B-4		2107B-6		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWC}	Read Modify Write (RMW) Cycle Time	520		590		960		ns
t_{CRW}	CE Width During RMW	350	4000	420	4000	540	3000	ns
t_{WC}	$\overline{WE}$ to CE on	0		0		0		ns
t_W	$\overline{WE}$ to CE off	150		150		200		ns
t_{WP}	$\overline{WE}$ Pulse Width	50		50		100		ns
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		ns
t_{DH}	D_{IN} Hold Time	0		0		0		ns
t_{CO}	CE to Output Delay		180		250		320	ns
t_{ACC}	Access Time ($t_{ACC} = t_{AC} + t_{CO} + 1t_T$)		200		270		350	ns



NOTES:
1. Minimum cycle timing is based on t_T of 20ns.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$. C_{LOAD} = 50pF. Load = One TTL Gate.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Typical Characteristics

Fig. 1. I_{DD} AV VS. TEMPERATURE

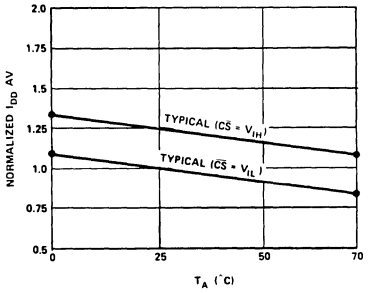


Fig. 2. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

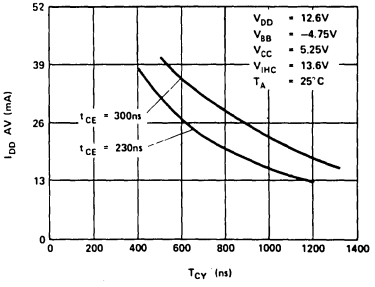


Fig. 3. I_{DD2} VS. TEMPERATURE

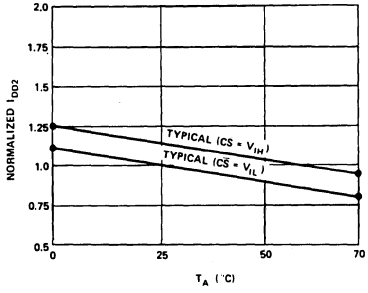
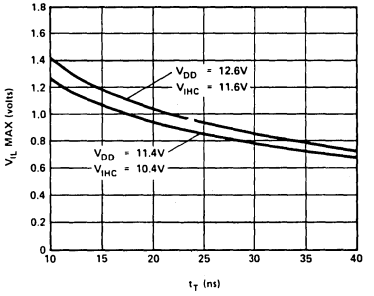
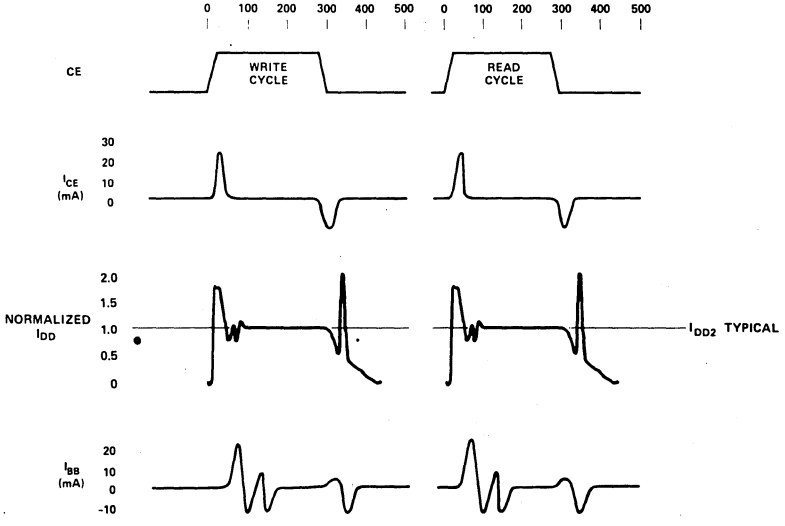


Fig. 4. TYPICAL V_{IL} MAX VS. CE RISE TIME



Typical Current Transients vs. Time



For additional typical characteristics and applications information please refer to Intel Application Note AP-10, "Memory System Design With the Intel 2107B 4K RAM" or Intel's Memory Design Handbook.

2111A
256 x 4 RAM WITH COMMON I/O AND OUTPUT DISABLE

2111A-2	250 ns Max.
2111A	350 ns Max.
2111A-4	450 ns Max.

- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible: All Inputs and Output
- Static MOS: No Clocks or Refreshing Required
- Simple Memory Expansion: Chip Enable Input
- Fully Decoded: On Chip Address Decode
- Inputs Protected: All Inputs Have Protection Against Static Charge
- Low Cost Packaging: 18 Pin Plastic Dual In-Line Configuration
- Low Power: Typically 150mW
- Three-State Output: OR-Tie Capability

The Intel® 2111A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

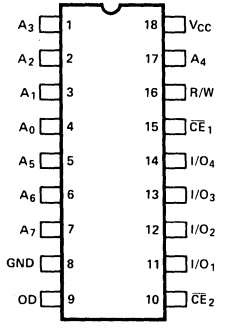
The 2111A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

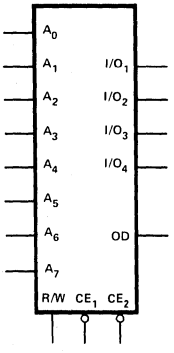
The Intel® 2111A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



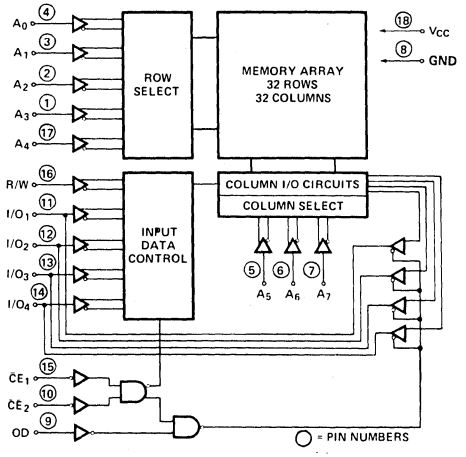
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1-I/O_4	DATA INPUT/OUTPUT

BLOCK DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

COMMENT:

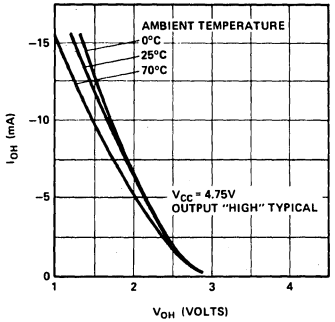
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

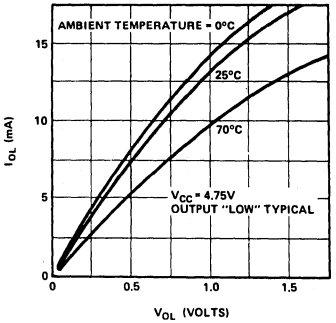
T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current		1	10	µA	$\overline{CE}_1$ = $\overline{CE}_2$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current		-1	-10	µA	$\overline{CE}_1$ = $\overline{CE}_2$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current 2111A, 2111A-4		35	55	mA	V_{IN} = 5.25V
	2111A-2		45	65		$I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current 2111A, 2111A-4			60	mA	V_{IN} = 5.25V
	2111A-2			70		$I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage 2111A, 2111A-2	2.4			V	I_{OH} = -200µA
	2111A-4	2.4			V	I_{OH} = -150µA

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. Characteristics for 2111A-2 (250ns Access Time)

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	
t_A	Access Time			250	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			180	ns	
t_{OD}	Output Disable To Output			130	ns	Timing Reference = 1.5V
t_{DF}[3]	Data Output to High Z State	0		180	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	150			ns	
t_{DW}	Data Setup	150			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	150			ns	and C_L = 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: 0.8 Volt and 2.0 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

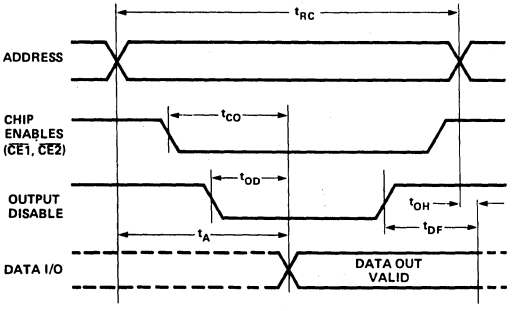
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[2] T_A = 25°C, f = 1MHz

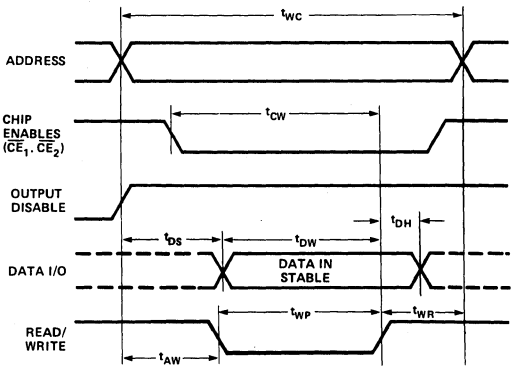
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	10	15

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

2111A (350 ns Access Time)
A.C. Characteristics

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	$t_r, t_f = 20ns$ Timing Reference = 1.5V Load = 1 TTL Gate and $C_L = 100pF$.
t_A	Access Time			350	ns	
t_{CO}	Chip Enable To Output			240	ns	
t_{OD}	Output Disable To Output			180	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	220			ns	$t_r, t_f = 20ns$ Timing Reference = 1.5V Load = 1 TTL Gate and $C_L = 100pF$.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	200			ns	
t_{DW}	Data Setup	200			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	200			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

2111A-4 (450 ns Access Time)
A.C. Characteristics

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	$t_r, t_f = 20ns$ Timing Reference = 1.5V Load = 1 TTL Gate and $C_L = 100pF$.
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	$t_r, t_f = 20ns$ Timing Reference = 1.5V Load = 1 TTL Gate and $C_L = 100pF$.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

2111, 2111-1, 2111-2

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

- **Organization 256 Words by 4 Bits**
- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Access Time — 0.5 to 1 μsec Max.**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 18 Pin Plastic Dual-In-Line Configuration**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**

The Intel®2111 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

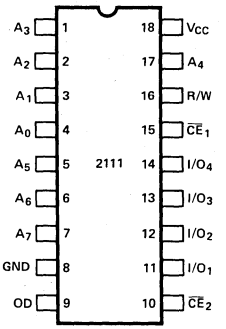
The 2111 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

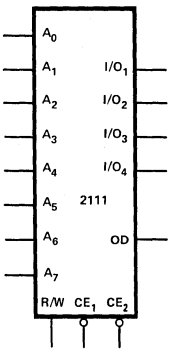
The Intel 2111 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



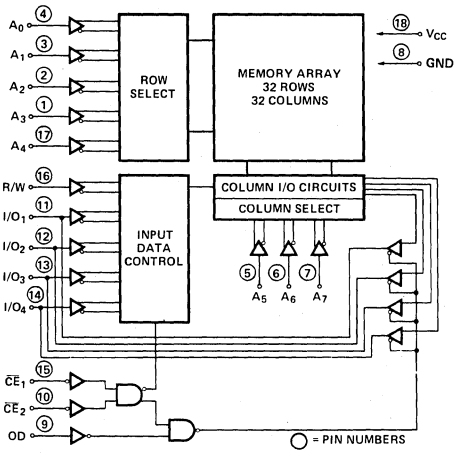
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1- I/O_4	DATA INPUT/OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

COMMENT:

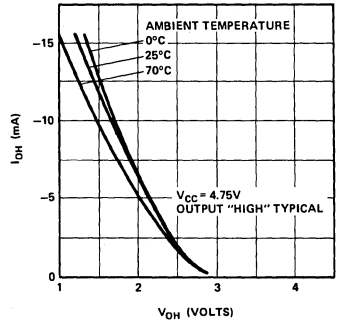
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics for 2111, 2111-1, 2111-2

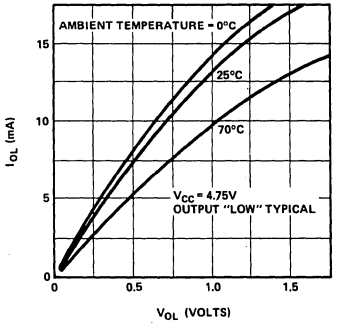
T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE}_1$ = $\overline{CE}_2$=2.2V, $V_{I/O}$=4.0V
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE}_1$ = $\overline{CE}_2$=2.2V, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		+0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.2			V	I_{OH} = -150 μA

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTE: 1. Typical values are for T_A = 25° C and nominal supply voltage.

A.C. Characteristics for 2111

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	1,000			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			1,000	ns	
t_{CO}	Chip Enable To Output			800	ns	
t_{OD}	Output Disable To Output			700	ns	
t_{DF}[3]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	1,000			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	900			ns	
t_{DW}	Data Setup	700			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	750			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	200			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

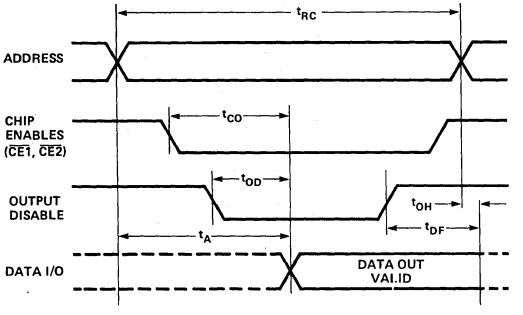
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[2] $T_A = 25°C$, f = 1MHz

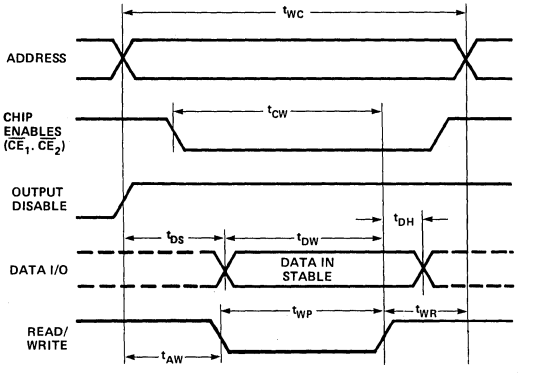
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	10	15

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

2111-1 (500 ns Access Time)

A.C. Characteristics for 2111-1

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	500			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			500	ns	
t_{CO}	Chip Enable To Output			350	ns	
t_{OD}	Output Disable To Output			300	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	500			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	100			ns	
t_{CW}	Chip Enable To Write	400			ns	
t_{DW}	Data Setup	280			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	300			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

2111-2 (650 ns Access Time)

A.C. Characteristics for 2111-2

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			650	ns	
t_{CO}	Chip Enable To Output			400	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, $\overline{CE}_2$, or OD, whichever occurs first.

2112A

256 x 4 RAM WITH COMMON DATA I/O

2112A-2	250 ns Max.
2112A	350 ns Max.
2112A-4	450 ns Max.

- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150mW**
- **Three-State Output: OR-Tie Capability**

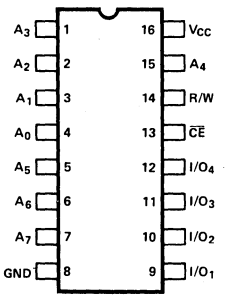
The Intel® 2112A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2112A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

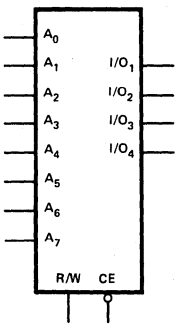
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2112A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



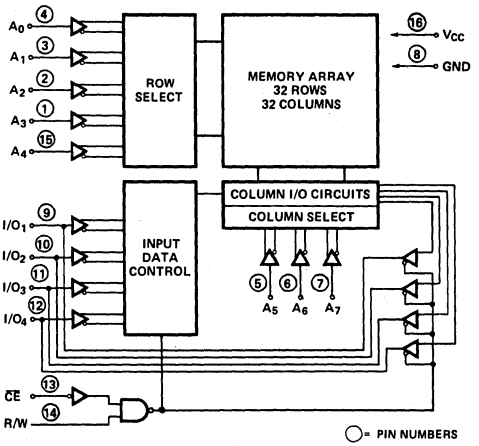
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

BLOCK DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

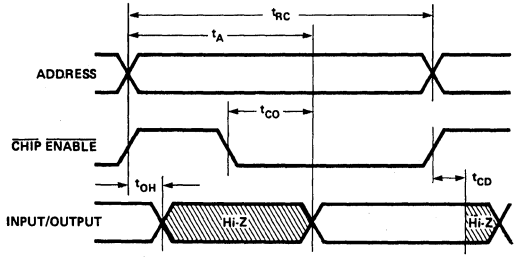
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			1	10	μA	$\overline{CE}$ = 2.0V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-1	-10	μA	$\overline{CE}$ = 2.0V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current	2112A, 2112A-4		35	55	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
		2112A-2		45	65		
I_{CC2}	Power Supply Current	2112A, 2112A-4			60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
		2112A-2			70		
V_{IL}	Input "Low" Voltage		-0.5		0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2mA
V_{OH}	Output "High" Voltage	2112A, 2112A-2	2.4			V	I_{OH} = -200μA
		2112A-4	2.4			V	I_{OH} = -150μA

A.C. Characteristics for 2112A-2

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	t_r, t_f = 20ns
t_A	Access Time			250	ns	
t_{CO}	Chip Enable To Output Time			180	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		120	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

READ CYCLE WAVEFORMS



Capacitance[2] T_A = 25°C, f = 1 MHz

Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics for 2112A-2 (Continued)

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

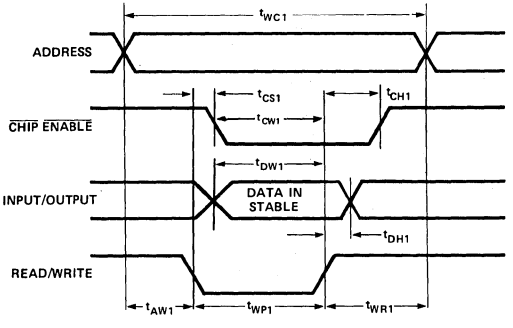
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	200			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	
t_{DW1}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	180			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable To Write Setup Time	180			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

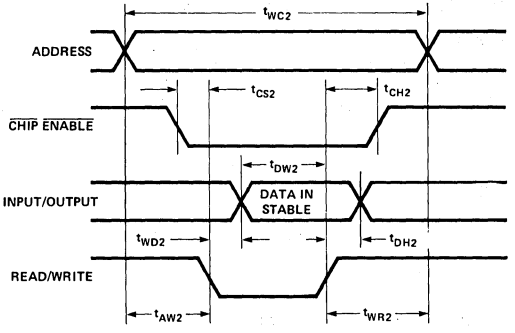
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	
t_{DW2}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	120			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

Write Cycle Waveforms

WRITE CYCLE #1



WRITE CYCLE #2



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. Characteristics for 2112A

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns
t_A	Access Time			350	ns	
t_{CO}	Chip Enable To Output Time			240	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		200	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	270			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	
t_{DW1}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	250			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	250			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	470			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	
t_{DW2}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	200			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

A.C. Characteristics for 2112A-4

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output Time			310	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		260	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	
t_{DW1}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	300			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	300			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	580			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	V_{IN} = +0.65V to +2.2V
t_{DW2}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	260			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON DATA I/O

- **Organization 256 Words by 4 Bits**
- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Static MOS: No Clocks or Refreshing Required**
- **Access Time: 0.65 to 1 μsec Max.**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150mW**
- **Three-State Output: OR-Tie Capability**

The Intel® 2112 is a 256 word by 4-bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data. Common input/output pins are provided.

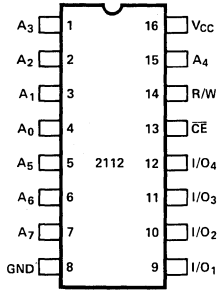
The 2112 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

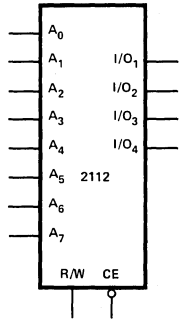
The Intel® 2112 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



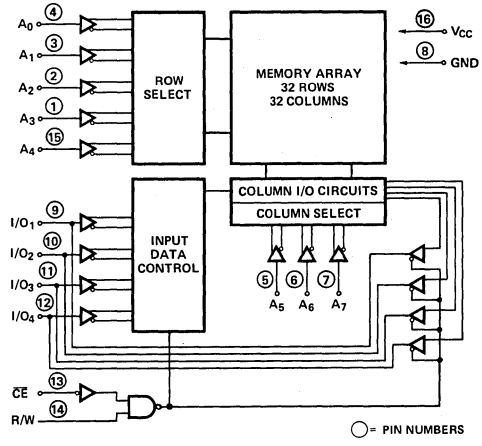
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70° C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics for 2112, 2112-2

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

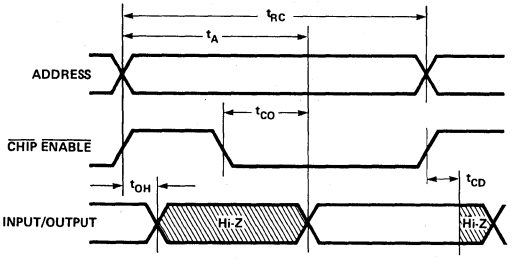
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	µA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-50	µA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150µA

A.C. Characteristics for 2112

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	1,000			ns	t_r, t_f = 20ns
t_A	Access Time			1,000	ns	V_{IN} = +0.65V to +2.2V
t_{CO}	Chip Enable To Output Time			800	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		200	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

READ CYCLE WAVEFORMS



Capacitance[2] T_A = 25°C, f = 1 MHz

Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

NOTES:
1. Typical values are for T_A = 25° C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics for 2112 (Continued)

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

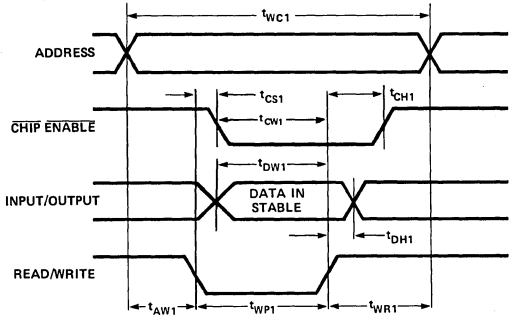
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	850			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	150			ns	V_{IN} = +0.65V to +2.2V
t_{DW1}	Write Setup Time	650			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	650			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	50			ns	
t_{DH1}	Data Hold Time	100			ns	
t_{CW1}	Chip Enable To Write Setup Time	650			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

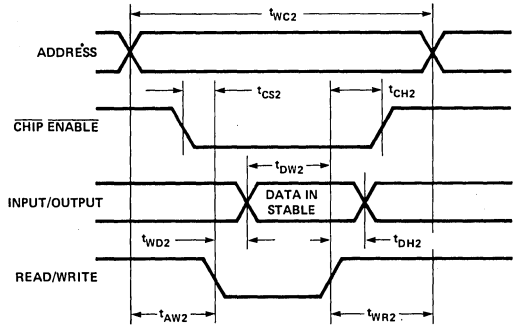
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	1050			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	150			ns	V_{IN} = +0.65V to +2.2V
t_{DW2}	Write Setup Time	650			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	200			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	50			ns	
t_{DH2}	Data Hold Time	100			ns	

Write Cycle Waveforms

WRITE CYCLE #1



WRITE CYCLE #2



NOTE: 1. Typical values are for T_A = 25° C and nominal supply voltage.

2112-2 (650 ns Access Time)

A.C. Characteristics for 2112-2

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	$t_r, t_f = 20ns$
t_A	Access Time			650	ns	$V_{IN} = +0.65V$ to $+2.2V$
t_{CO}	Chip Enable To Output Time			500	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		150	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and $C_L = 100pF$.

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	500			ns	$t_r, t_f = 20ns$
t_{AW1}	Address To Write Setup Time	100			ns	$V_{IN} = +0.65V$ to $+2.2V$
t_{DW1}	Write Setup Time	280			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	350			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and $C_L = 100pF$.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	50			ns	
t_{DH1}	Data Hold Time	50			ns	
t_{CW1}	Chip Enable to Write Setup Time	350			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	650			ns	$t_r, t_f = 20ns$
t_{AW2}	Address To Write Setup Time	100			ns	$V_{IN} = +0.65V$ to $+2.2V$
t_{DW2}	Write Setup Time	280			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	200			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and $C_L = 100pF$.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	50			ns	
t_{DH2}	Data Hold Time	50			ns	

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

1024 X 1 HIGH SPEED STATIC RAM

	2115-2, 2125-2	2115, 2125	2115L, 2125L
Typ. T_{AA} (ns)	55	75	75
Typ. I_{CC} (mA)	80	75	50

- **Fully Pin Compatible to 93415 (2115) and 93425 (2125)**
- **Low Operating Power Dissipation: Typical 0.2mW/bit (2115L, 2125L)**
- **TTL Inputs and Output**
- **Single +5V Supply**
- **Uncommitted Collector* (2115) and Three-State (2125) Output**
- **Non-Inverting Data Output**
- **Standard 16 Pin Dual In-Line Package**

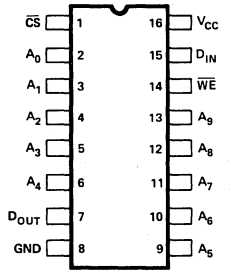
The Intel® 2115 and 2125 family are fully static read/write random access memories organized as 1024 words by 1 bit. These RAMs are designed for buffer control storage and high performance main memory applications. They are compatible with TTL logic families in all respects: inputs, output, and a single +5V supply. Both uncommitted collector* and three-state output are available.

The 2115 and 2125 family offers high performance, low power dissipation, and system cost savings. Fast system speed is achieved by using the 2115-2 and 2125-2. The 2115L and 2125L gives low system power dissipation, only 0.2mW/bit typical. The 2115 and 2125 are ideal for slower performance systems where cost is a prime factor.

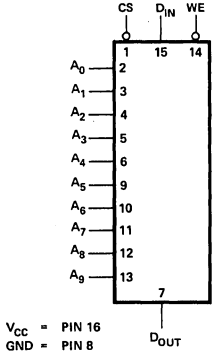
The 2115 and 2125 family is fabricated with N-channel MOS silicon gate technology. This technology allows the design and production of high speed MOS RAMs which are compatible to the performance of bipolar RAMs, but offering the advantage of lower power dissipation and cost.

*The 2115 is a MOS device and the output is actually an uncommitted drain.

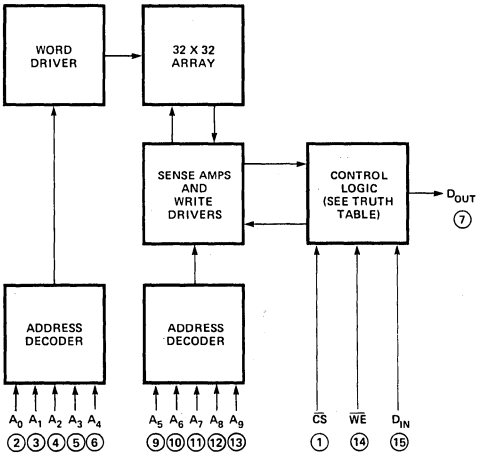
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

TRUTH TABLE

INPUTS			OUTPUT 2115 FAMILY	OUTPUT 2125 FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	NOT SELECTED
L	L	L	H	HIGH Z	WRITE "0"
L	L	H	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
All Output or Supply Voltages . . . . . -0.5 to +7 Volts
All Input Voltages . . . . . -0.5 to +5.5 Volts
D.C. Output Current 20mA

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics [1] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V_{OL1}	2115-2 Output Low Voltage			0.45	V	I_{OL} = 16mA
V_{OL2}	2115, 2115L Output Low Voltage			0.45	V	I_{OL} = 12mA
V_{OL3}	2125 Family Output Low Voltage			0.45	V	I_{OL} = 7mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		-1	-40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
I_{CEX}	2115 Family Output Leakage Current		10	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	2125 Family Output Current (High Z)		10	50	μA	V_{CC} =Max., V_{OUT} = 0.5V/2.4V
I_{OS} [2]	2125 Family Current Short Circuit to Ground			-100	mA	V_{CC} = 4.5V
V_{OH}	2125 Family Output High Voltage	2.4			V	I_{OH} = -3.2mA
I_{CCL}	2115L, 2125L Power Supply Current		50	65	mA	All Inputs Grounded, Output Open
I_{CC1}	2115, 2125, Power Supply Current		75	100	mA	All Inputs Grounded, Output Open
I_{CC2}	2115-2, 2125-2 Power Supply Current		80	125	mA	All Inputs Grounded, Output Open

Notes:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (@ 400 f_{PM} air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W.
2. Duration of short circuit current should not exceed 1 second.

2115 Family A.C. Characteristics[1] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

READ CYCLE

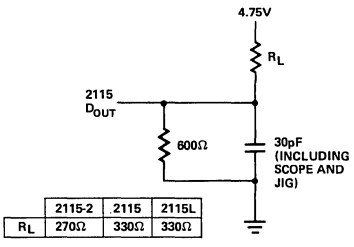
Symbol	Test	2115-2 Limits Min.	Typ.	Max.	2115 Limits Min.	Typ.	Max.	2115L Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5		40	5		45	5		50	ns
t_{RCS}	Chip Select Recovery Time			40			40			40	ns
t_{AA}	**Address Access Time**		55	70		75	95		75	95	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			ns

WRITE CYCLE

Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{WS}	Write Enable Time			40			40			40	ns
t_{WR}	Write Recovery Time	5		45	5		45	5		50	ns
t_W	Write Pulse Width	50			50			50			ns
t_{WSD}	Data Set-Up Time Prior to Write	5			5			15			ns
t_{WHD}	Data Hold Time After Write	5			5			15			ns
t_{WSA}	Address Set-Up Time	15			30			30			ns
t_{WHA}	Address Hold Time	5			5			15			ns
t_{WSCS}	Chip Select Set-Up Time	5			5			15			ns
t_{WHCS}	Chip Select Hold Time	5			5			15			ns

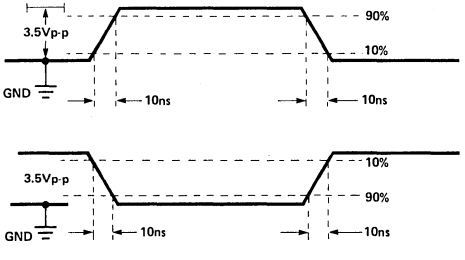
TEST CONDITIONS

A.C. AND D.C. LOADING CONDITIONS

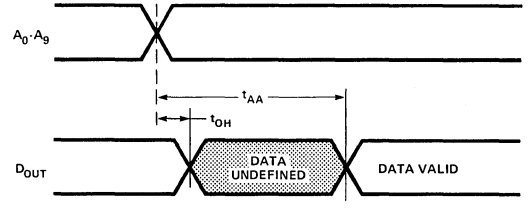


	2115-2	2115	2115L
R_L	270Ω	330Ω	330Ω

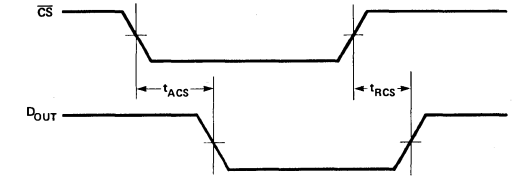
ALL INPUT PULSES



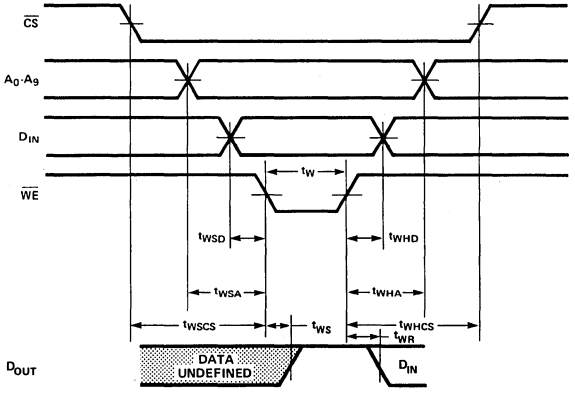
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

2125 Family A.C. Characteristics[1] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

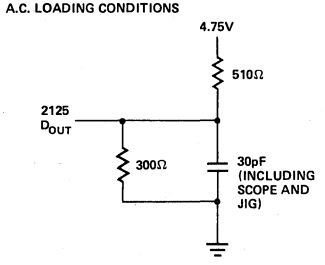
READ CYCLE

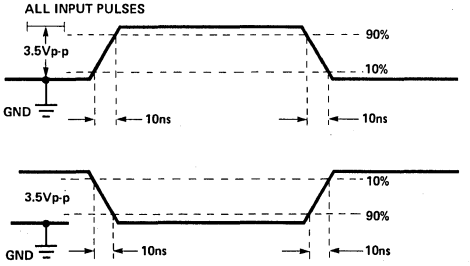
Symbol	Test	2125-2 Limits Min.	Typ.	Max	2125 Limits Min.	Typ.	Max.	2125L Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5		40	5		45	5		50	ns
t_{ZRCS}	Chip Select to HIGH Z			40			40			40	ns
t_{AA}	Address Access Time		55	70		75	95		75	95	ns
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			ns

WRITE CYCLE

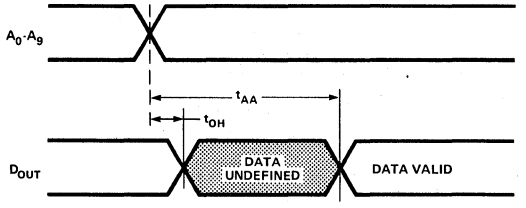
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ZWS}	Write Enable to HIGH Z			40			40			40	ns
t_{WR}	Write Recovery Time	5		45	5		45	5		50	ns
t_W	Write Pulse Width	50			50			50			ns
t_{WSD}	Data Set-Up Time Prior to Write	5			5			15			ns
t_{WHD}	Data Hold Time After Write	5			5			15			ns
t_{WSA}	Address Set Up Time	15			30			30			ns
t_{WHA}	Address Hold Time	5			5			15			ns
t_{WSCS}	Chip Select Set-Up Time	5			5			15			ns
t_{WHCS}	Chip Select Hold Time	5			5			15			ns

TEST CONDITIONS

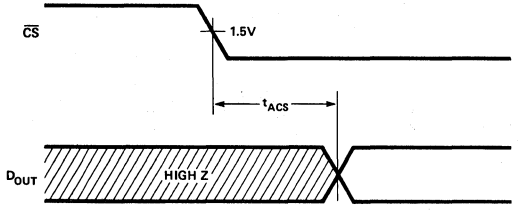




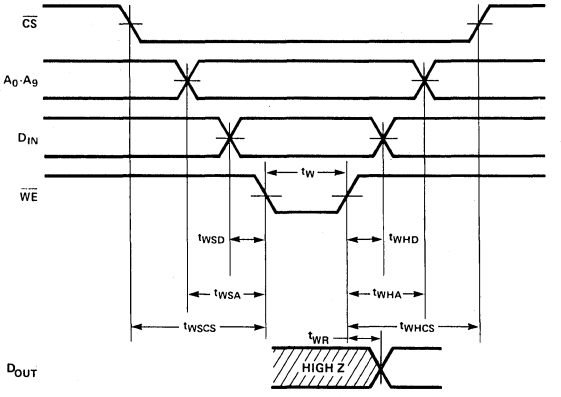
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT

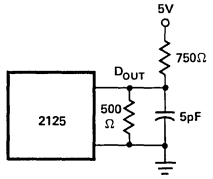


WRITE CYCLE

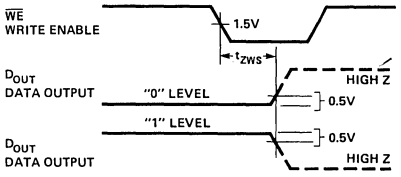


(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

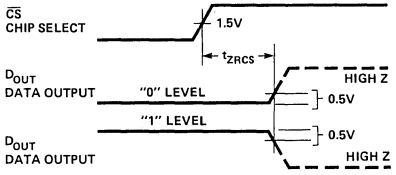
2125 FAMILY WRITE ENABLE TO HIGH Z DELAY



LOAD 1



2125 FAMILY PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{ZXX} parameters are measured at a delta of 0.5V from the logic level and using Load 1.)

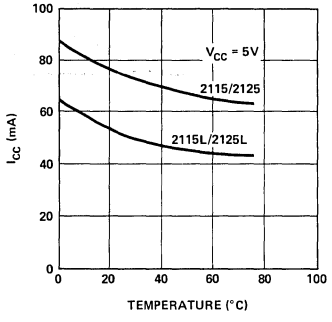
2115/2125 FAMILY CAPACITANCE* V_{CC} = 5V, f = 1 MHz, T_A = 25°C

Symbol	Test	2115 Family Limits Typ.	2115 Family Limits Max.	2125 Family Limits Typ.	2125 Family Limits Max.	Units	Test Conditions
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	$\overline{CS}$=5V, All other inputs = 0V, Output Open

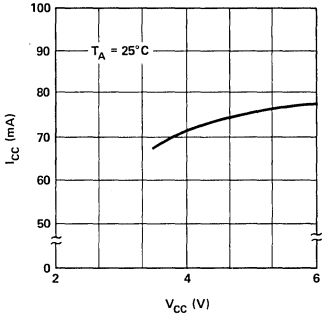
*This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

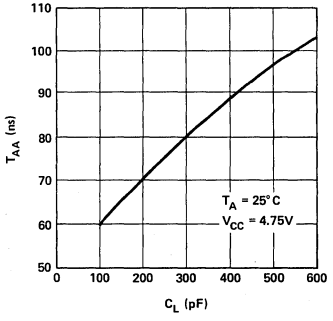
I_{CC} VS. TEMPERATURE



I_{CC} VS. V_{CC}



ACCESS TIME VS. CAPACITANCE



16,384-BIT DYNAMIC MOS RANDOM ACCESS MEMORY

The Intel® 2116 is a 16K x 1 dynamic N-Channel MOS RAM fabricated with Intel's highly reliable silicon gate technology and packaged in a standard 16 pin DIP. It uses a single transistor cell for low cost, low power, high speed and high packing density. Two clocks, $\overline{CAS}$ and $\overline{RAS}$, multiplex the address inputs with non-critical timing requirements.

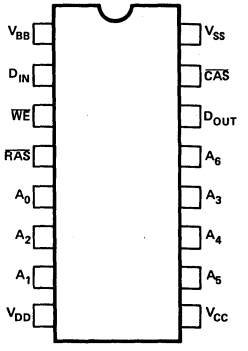
The industry standard pin configuration of the 2116 will enable systems using the 2104 type 4K RAMs to be easily upgraded to 16K capabilities.

The 2116 family offers identical power dissipation, access and cycle times to those of the 2104, 2104-2, and 2104-4. All input and output levels of the 2116 are TTL compatible. The output is three-state.

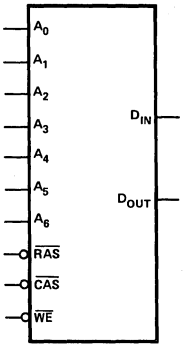
EXPECTED CHARACTERISTICS

Ambient Temperature Range: 0° C to 70° C
Nominal V_{DD}: 12V
Nominal V_{CC}: +5V
Nominal V_{BB}: −5V
Nominal V_{SS}: 0V
V_{IL} Range: −1.0V to 0.8V
V_{IH} Range: 2.4 to V_{DD} +1V
Maximum V_{OL}: 0.4V
Minimum V_{OH}: 2.4V
Maximum Operating Power: <900mW
Maximum Standby Power: 24mW
Maximum Access Times: 250, 300, 350ns
Minimum Cycle Times: 375, 425, 500ns
Maximum Refresh Time: 2ms

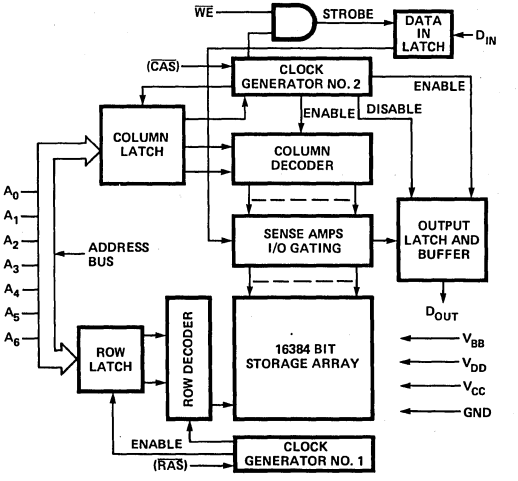
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

HIGH SPEED FULLY DECODED 64 BIT MEMORY

- **Fast Access Time -- 35 nsec. max. over 0-75° C Temperature Range.** (3101A)
- **Simple Memory Expansion through Chip Select Input -- 17 nsec. max. over 0-75° C Temperature Range.** (3101A)
- **DTL and TTL Compatible -- Low Input Load Current: 0.25mA. max.**
- **OR-Tie Capability -- Open Collector Outputs.**
- **Fully Decoded -- on Chip Address Decode and Buffer.**
- **Minimum Line Reflection -- Low Voltage Diode Input Clamp.**
- **Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration.**

The Intel® 3101 and 3101A are high speed fully decoded 64 bit random access memories, organized 16 words by 4 bits. Their high speed makes them ideal in scratch pad applications. An unselected chip will not generate noise at its output during writing of a selected chip. The output is held high on an unselected chip regardless of the state of the read/write signal.

The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices with gold diffusion processes.

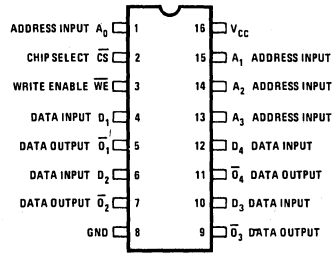
The Intel 3101 and 3101A are packaged in either hermetically sealed 16 pin ceramic packages, or in low cost silicone packages, and their performance is specified over a temperature range from 0°C to 75°C.

The storage cells are addressed through an on chip 1 of 16 binary decoder using four input address leads.

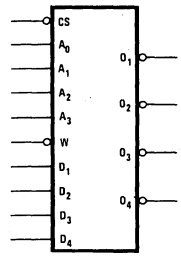
A separate Chip Select lead allows easy selection of an individual package when outputs are OR-tied.

In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

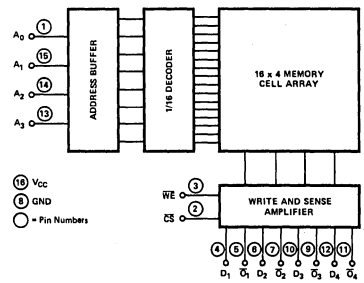
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_1–D_4	DATA INPUTS	$\overline{CS}$	CHIP SELECT INPUT
A_0–A_3	ADDRESS INPUTS	$\overline{O}_1$–$\overline{O}_4$	DATA OUTPUTS
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)

TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
LOW	LOW	WRITE	HIGH
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
HIGH	LOW	–	HIGH
HIGH	HIGH	–	HIGH

Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		100 mA

*COMMENT:

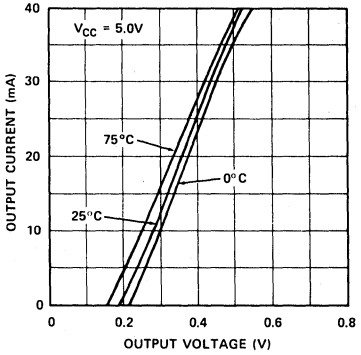
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

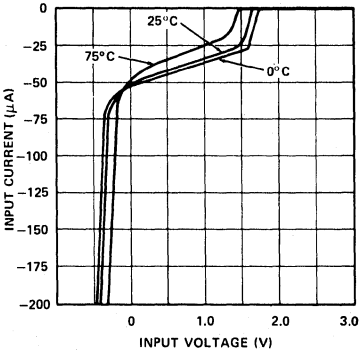
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_A =0.45V
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_D =0.45V
I_{FW}	WRITE INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_W =0.45V
I_{FS}	CHIP SELECT INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_S =0.45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_A =5.25V
I_{RD}	DATA INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_D =5.25V
I_{RW}	WRITE INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_W =5.25V
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_S =5.25V
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_A =−5.0 mA
V_{CD}	DATA INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_D =−5.0 mA
V_{CW}	WRITE INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_W =−5.0 mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_S =−5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} =4.75V, I_{OL} = 15 mA Memory Stores "Low"
I_{CEX}	OUTPUT LEAKAGE CURRENT		100	μA	V_{CC} =5.25V, V_{CEX} =5.25V V_S =2.5V
I_{CC}	POWER SUPPLY CURRENT		105	mA	V_{CC} =5.25V, V_A =V_S =V_D =0V
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} =5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} =5.0V

Typical Characteristics

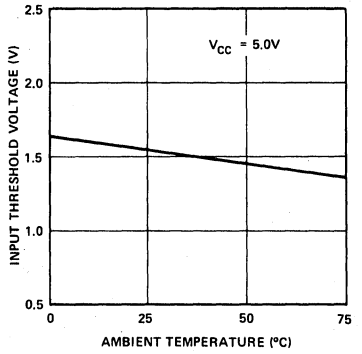
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE



Switching Characteristics

Conditions of Test:

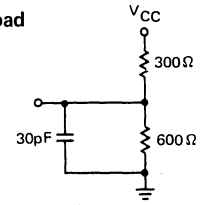
Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

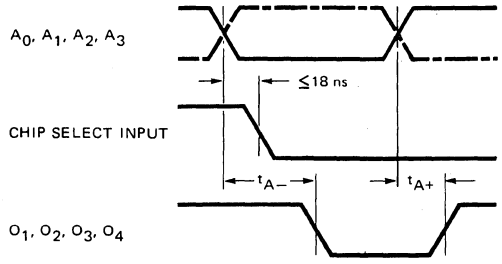
Output loading is 15mA and 30 pF

15 mA Test Load

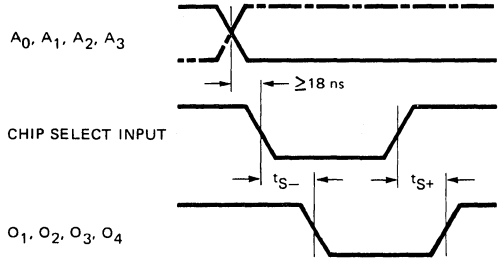


READ CYCLE

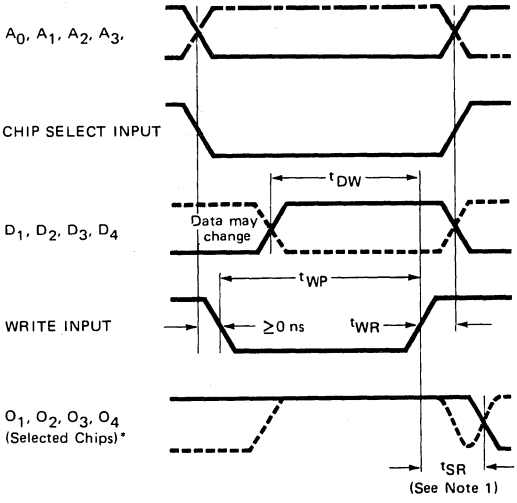
Address to Output Delay



Chip Select to Output Delay



WRITE CYCLE



*Outputs of unselected chips remain high during write cycle.

NOTE 1: t_{SR} is associated with a read cycle following a write cycle and does not affect the access time.

A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

READ CYCLE					
SYMBOL	PARAMETER	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{S+}, t_{S-}	Chip Select to Output Delay	5	17	5	42
t_{A-}, t_{A+}	Address to Output Delay	10	35	10	60

WRITE CYCLE					
SYMBOL	TEST	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{SR}	Sense Amplifier Recovery Time		35		50
t_{WP}	Write Pulse Width	25		40	
t_{DW}	Data-Write Overlap Time	25		40	
t_{WR}	Write Recovery Time	0		5	

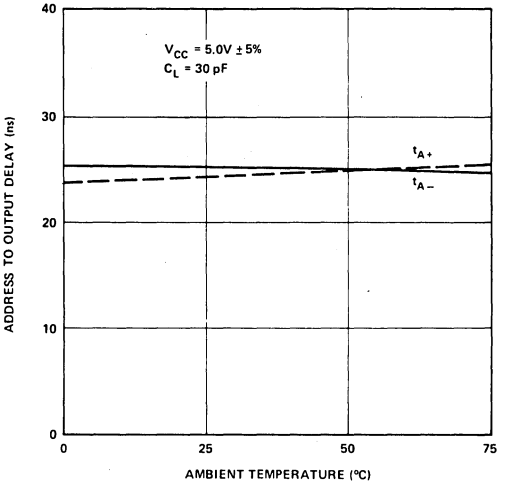
CAPACITANCE(2) T_A = 25°C

C_{IN}	INPUT CAPACITANCE (All Pins)	10 pF maximum
C_{OUT}	OUTPUT CAPACITANCE	12 pF maximum

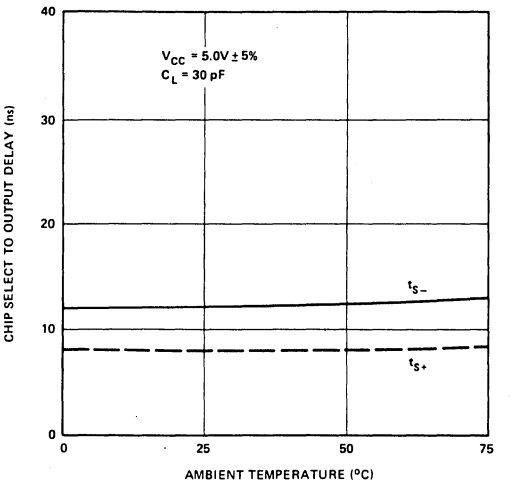
NOTE 2: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

Typical A.C. Characteristics

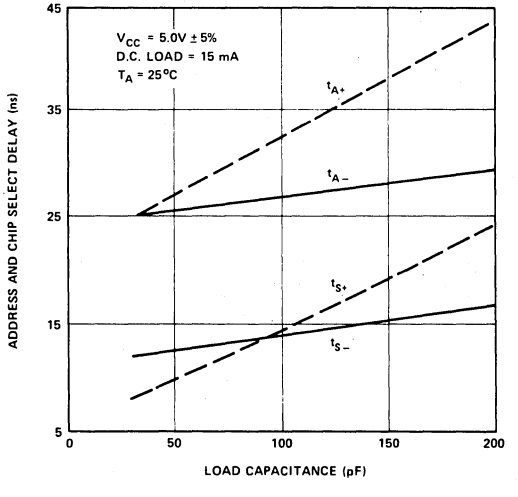
ADDRESS TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



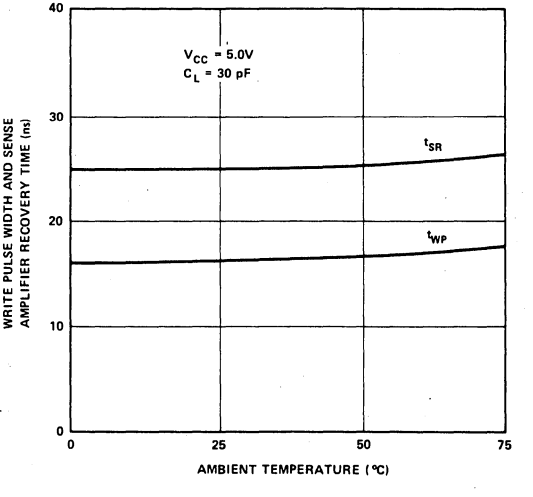
CHIP SELECT TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



ADDRESS & CHIP SELECT TO OUTPUT DELAY
VS.
LOAD CAPACITANCE



WRITE PULSE WIDTH & SENSE
AMPLIFIER RECOVERY TIME
VS. AMBIENT TEMPERATURE



M3101, M3101A

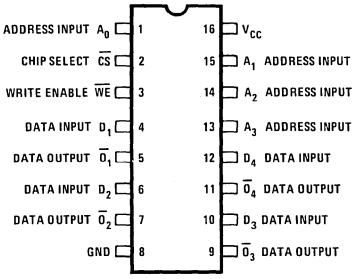
MILITARY TEMP.

HIGH SPEED FULLY DECODED 64 BIT MEMORY

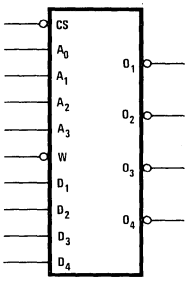
- **Military Temperature Range —55°C to +125°C**
- **Fast Access Time—45ns Maximum (M3101A)**
- **OR-Tie Capability— Open Collector Outputs**
- **Standard Packaging—16 Pin Dual In-Line Lead Configuration**

The M3101 and M3101A are military temperature range RAMs, organized as 16 words by 4-bits. Their high speed makes them ideal in scratch pad and small buffer memory applications. The M3101 and M3101A are fabricated with using Schottky barrier diode clamped transistors which results in higher speed performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION



LOGIC SYMBOL



TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
LOW	LOW	WRITE	HIGH
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
HIGH	LOW	–	HIGH
HIGH	HIGH	–	HIGH

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 15°C to +55°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics T_A = –55°C to +125°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FD}	Data Input Load Current		-0.25	mA	V_{CC}=5.25V, V_D=0.45V
I_{FW}	Write Input Load Current		-0.25	mA	V_{CC}=5.25V, V_W=0.45V
I_{FS}	Chip Select Input Load Current		-0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current		10	μA	V_{CC}=5.25V, V_A=5.25V
I_{RD}	Data Input Leakage Current		10	μA	V_{CC}=5.25V, V_D=5.25V
I_{RW}	Write Input Leakage Current		10	μA	V_{CC}=5.25V, V_W=5.25V
I_{RS}	Chip Select Input Leakage Current		10	μA	V_{CC}=5.25V, V_S=5.25V
V_{CA}	Address Input Clamp Voltage		-1.0	V	V_{CC}=4.75V, I_A=-5.0mA
V_{CD}	Data Input Clamp Voltage		-1.0	V	V_{CC}=4.75V, I_D=-5.0mA
V_{CW}	Write Input Clamp Voltage		-1.0	V	V_{CC}=4.75V, I_W=-5.0mA
V_{CS}	Chip Select Input Clamp Voltage		-1.0	V	V_{CC}=4.75V, I_S=-5.0mA
V_{OL}	Output "Low" Voltage		0.45	V	V_{CC}=4.75V, I_{OL}=10mA Memory Stores "Low"
I_{CEX}	Output Leakage Current		100	μA	V_{CC}=5.25V, V_{CEX}=5.25V, V_S=2.5V
I_{CC}	Power Supply Current		105	mA	V_{CC}=5.25V, V_A=V_S=V_D=0V
V_{IL}	Input "Low" Voltage		0.80	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.1		V	V_{CC}=5.0V

MILITARY TEMP.

A.C. Characteristics $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 5\%$

READ CYCLE					
SYMBOL	PARAMETER	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{S+}, t_{S-}	Chip Select to Output Delay	5	25	5	55
t_{A-}, t_{A+}	Address to Output Delay	10	45	10	75

WRITE CYCLE					
SYMBOL	TEST	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{SR}	Sense Amplifier Recovery Time		40		50
t_{WP}	Write Pulse Width	35		40	
t_{DW}	Data-Write Overlap Time	35		40	
t_{WR}	Write Recovery Time	0		0	

CAPACITANCE[1] $T_A = 25°C$

C_{IN}	INPUT CAPACITANCE (All Pins)	10 pF maximum
C_{OUT}	OUTPUT CAPACITANCE	12 pF maximum

NOTE 1: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and $T_A = 25°C$.

Conditions of Test:

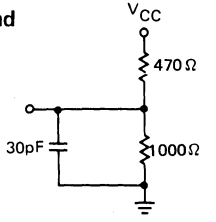
Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

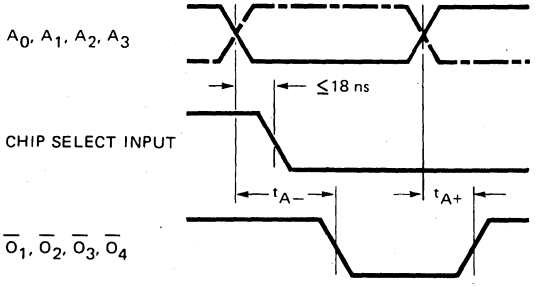
Output loading is 10 mA and 30 pF

10 mA Test Load

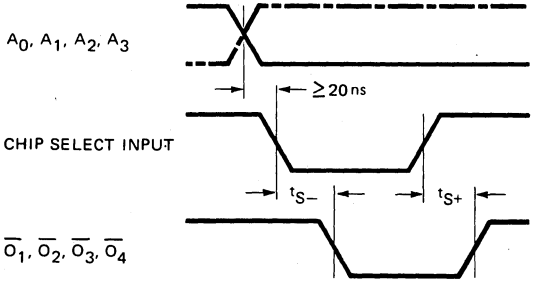


READ CYCLE

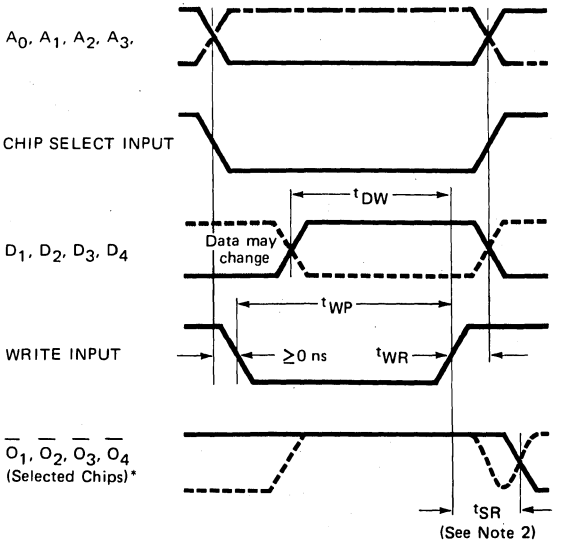
Address to Output Delay



Chip Select to Output Delay



WRITE CYCLE



*Outputs of unselected chips remain high during write cycle.

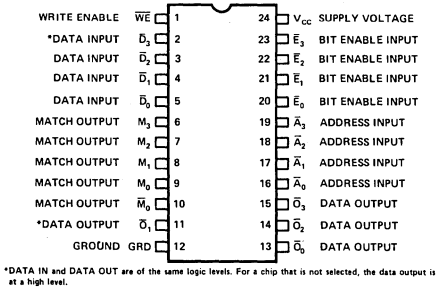
NOTE 2: t_{SR} is associated with a read cycle following a write cycle and does not affect the access time.

HIGH SPEED 16 BIT CONTENT ADDRESSABLE MEMORY

- Organization—4 Words x 4 Bits
- Max. Delay of 30 nsec Over 0° C to 75° C Temperature
- Open Collector Outputs—OR Tie Capability
- High Current Sinking Capability—15 mA max.
- Low Input Load Current—0.25 mA max.
- DTL & TTL Compatible
- Bit Enable Input—Bit Masking
- Standard 24 Pin Dual In-Line

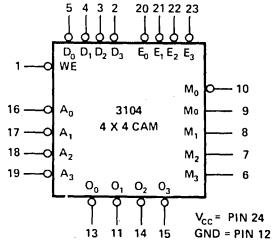
The Intel®3104 is a high speed 16 bit Content Addressable Memory (CAM). It is a linear select 4 word by 4 bit array which is designed to compare data on its inputs with data already stored in its memory and to indicate a match when these data are identical. This equality search is performed on all bits in parallel. The 3104 can also be used as a read/write RAM with linear selection addressing.

PIN CONFIGURATION

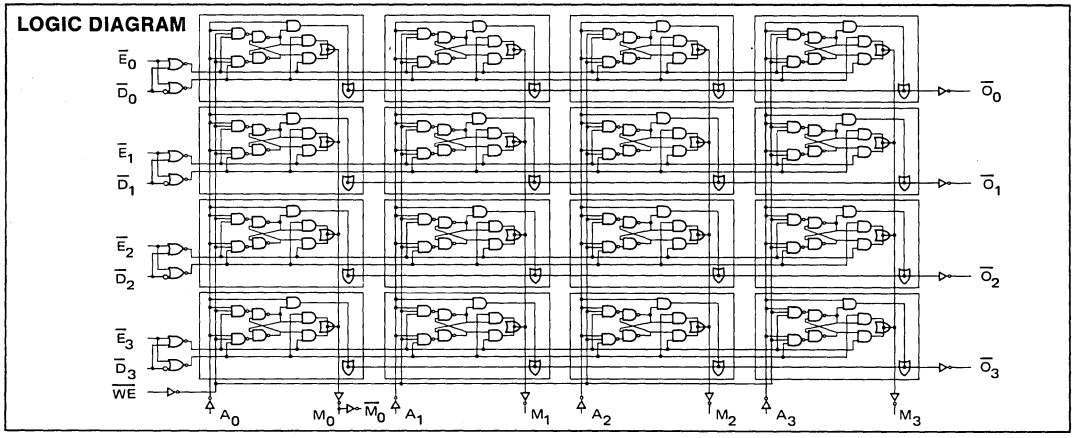


*DATA IN and DATA OUT are of the same logic levels. For a chip that is not selected, the data output is at a high level.

LOGIC SYMBOL



LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	−65°C to +125°C
Storage Temperature	−65°C to +160°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

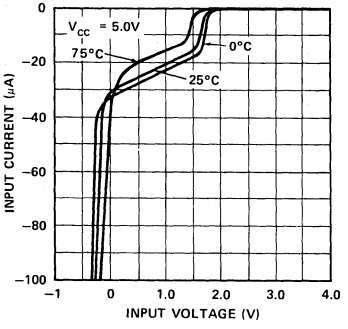
D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT			−0.25	mA	V_{CC} = 5.25V V_A = .45V
I_{FE}	BIT ENABLE INPUT LOAD CURRENT			−0.25	mA	V_{CC} = 5.25V V_E = .45V
I_{FW}	WRITE ENABLE INPUT LOAD CURRENT			−0.25	mA	V_{CC} = 5.25V V_W = .45V
I_{FD}	DATA INPUT LOAD CURRENT			−0.25	mA	V_{CC} = 5.25V V_D = .45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT			10	μA	V_{CC} = 5.25V V_A = 5.25V
I_{RE}	BIT ENABLE INPUT LEAKAGE CURRENT			10	μA	V_{CC} = 5.25V V_E = 5.25V
I_{RW}	WRITE ENABLE INPUT LEAKAGE CURRENT			10	μA	V_{CC} = 5.25V V_W = 5.25V
I_{RD}	DATA INPUT LEAKAGE CURRENT			10	μA	V_{CC} = 5.25V V_D = 5.25V
I_{CEX}	OUTPUT LEAKAGE CURRENT (ALL OUTPUTS)			50	μA	V_{CC} = 5.25V V_{CEX} = 5.25V
V_{OL}	OUTPUT "LOW" VOLTAGE (ALL OUTPUTS)			0.45	V	V_{CC} = 4.75V I_{OL} = 15mA
V_{IL}	INPUT "LOW" VOLTAGE (ALL INPUTS)			0.85	V	V_{CC} = 5V
V_{IH}	INPUT "HIGH" VOLTAGE (ALL INPUTS)	2.0			V	V_{CC} = 5V
I_{CC}	POWER SUPPLY CURRENT			125	mA	V_{CC} = 5.25V OUTPUTS HIGH
C_{IN}**	INPUT CAPACITANCE		5		pF	V_{IN} = +2.0V, V_{CC} = 0.0V f = 1 MHz
C_{OUT}**	OUTPUT CAPACITANCE		8		pF	V_{OUT} = +2.0V, V_{CC} = 0.0V f = 1 MHz

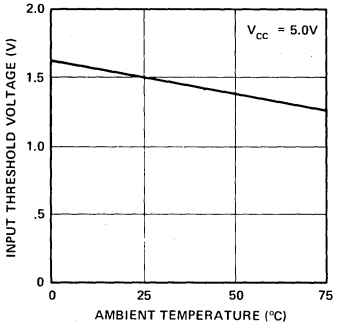
**This parameter is periodically sampled and is not 100% tested.

Typical D.C. Characteristics

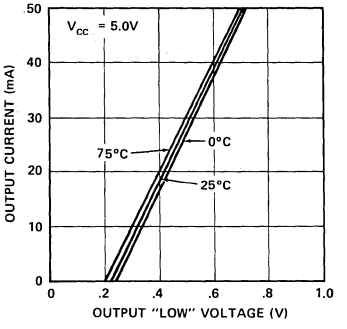
INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE

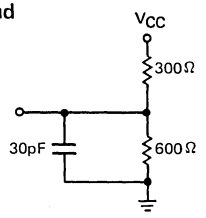


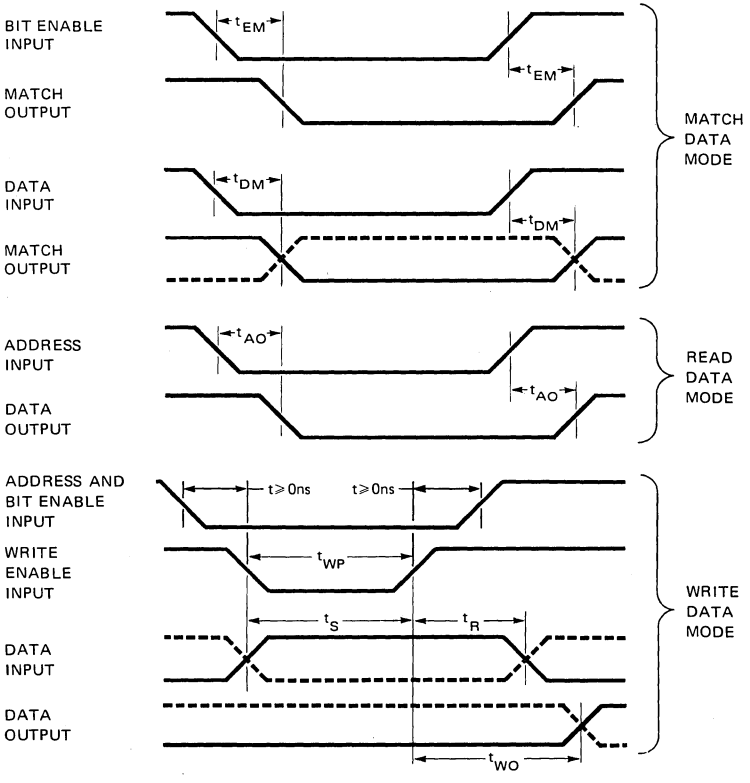
Switching Characteristics

Conditions of Test:

- Input Pulse amplitudes · · 2.5V
- Input pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts
- Speed measurements are made at 1.5 volt levels
- Output loading is 15 mA and 30 pF

15mA Test Load





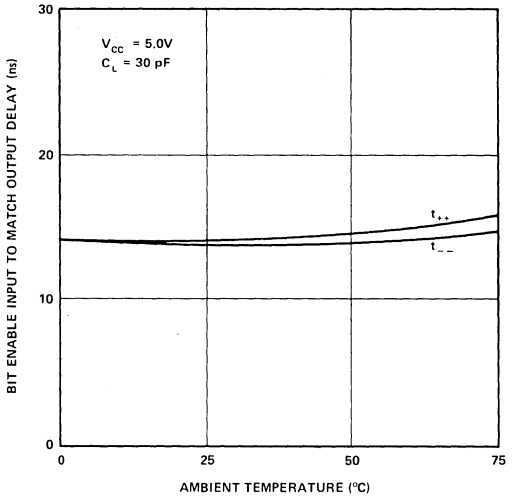
A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_{EM}	BIT ENABLE INPUT TO MATCH OUTPUT DELAY		15	30	ns
t_{DM}	DATA INPUT TO MATCH OUTPUT DELAY		16	30	ns
t_{AO}	ADDRESS INPUT TO OUTPUT DELAY		14	30	ns
t_{WP}	WRITE ENABLE PULSE WIDTH	40	25		ns
t_{WO}	WRITE ENABLE TO OUTPUT DELAY		–	40	ns
t_S	SET-UP TIME ON DATA INPUT		–	40	ns
t_R	RELEASE TIME ON DATA INPUT	0	–		ns

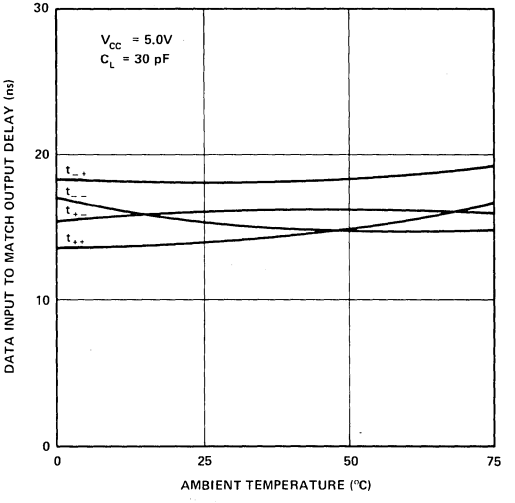
Note 1. Typical values are at nominal voltages and T_A = 25°C.

Typical A.C. Characteristics

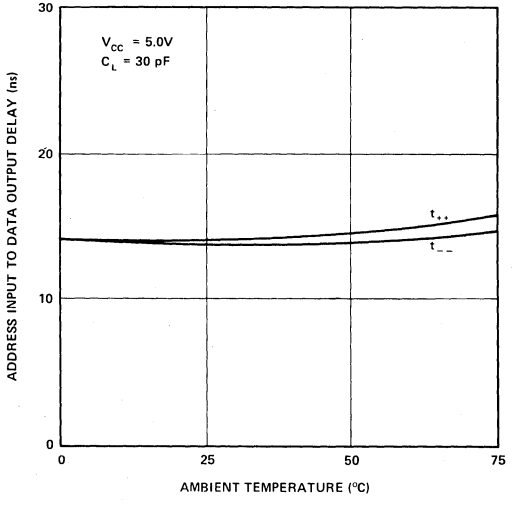
BIT ENABLE INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



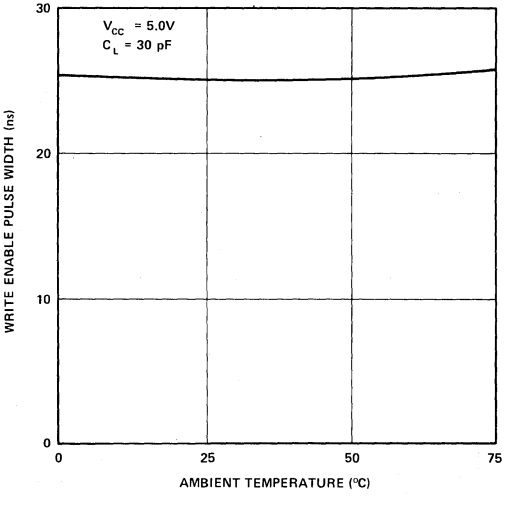
DATA INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



ADDRESS INPUT TO DATA OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. TEMPERATURE



3106A, 3106, 3106-8, 3107A, 3107, 3107-8

HIGH SPEED FULLY DECODED 256 BIT RAM

- **Fast Access Time—60 nsec max. over 0° to 75° C Temperature Range and ±5% Supply Voltage Tolerance – –3106A and 3107A**
- **Fully Decoded—On Chip Address Decode and Buffer**
- **DTL and TTL Compatible—Low Input Load Current: 0.25mA max.**
- **Open Collector (3107A, 3107, 3107-8) or Three State (3106A, 3106, 3106-8) Output**
- **Simple Memory Expansion through 3 Chip Select Inputs**
- **Minimum Line Reflection—Low Voltage Diode Input Clamp**
- **Standard Packaging--16 Pin DIP**

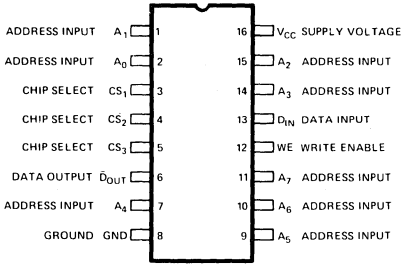
The Intel® 3106A and 3107A family are high speed, fully decoded, 256 bit read/write random access memories. Their organization is 256 words by 1-bit. These devices are designed for high speed scratch pad, buffer, and distributed main memory applications. The 3106A and 3107A are higher speed versions of the 3106 and 3107. The 3106-8 and 3107-8 are ideal for slower performance systems where low system cost is a prime factor.

All devices feature three chip-select inputs. The 3106A, 3106, and 3106-8 have a three-state output and the 3107A, 3107, and 3107-8 provide the user with the popular open collector output. On-chip address decoding and the high speed chip-select facilitate easy memory expansion.

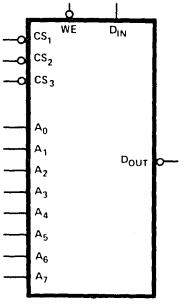
The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process. The performance of these devices is specified over a temperature range from 0°C to +75°C.

The 3106 and 3107 families are compatible with TTL and DTL logic circuits.

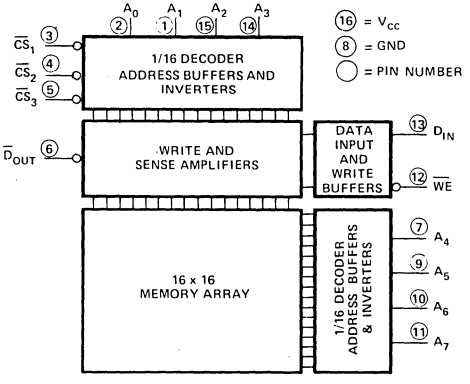
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	$\overline{CS}_1$–$\overline{CS}_3$	CHIP SELECT
A_0–A_7	ADDRESS INPUTS	$\overline{D}_{OUT}$	DATA OUTPUT
$\overline{WE}$	WRITE ENABLE INPUT		

TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
ALL LOW	LOW	WRITE	COMPLEMENT OF DATA INPUT
ALL LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
ONE OR MORE HIGH	DON'T CARE	HOLD	**3106A,3106,3106-8** HIGH IMPEDANCE STATE
			3107A,3107,3107-8 HIGH

Absolute Maximum Ratings*

Temperature Under Bias	−55° C to +125° C
Storage Temperature	−65° C to +160° C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.(1)	LIMITS MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT ALL INPUTS			−0.25	mA	V_{CC} = 5.25V V_{IN} = 0.45V
I_R	INPUT LEAKAGE CURRENT, ALL INPUTS			10	μA	V_{CC} = 4.75V V_R = 5.25V
V_C	INPUT CLAMP VOLTAGE, ALL INPUTS			−1.0	V	V_{CC} = 4.75V I_{IN} = −5.0 mA
V_{OL}	OUTPUT LOW VOLTAGE			0.45	V	V_{CC} = 4.75V I_{OL} = 15 mA
I_{CEX}	OUTPUT LEAKAGE CURRENT			100	μA	V_{CC} = V_{CEX} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		90	130	mA	V_{CC} = 5.25V ALL INPUTS OPEN
V_{IL}	INPUT LOW VOLTAGE			0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT HIGH VOLTAGE	2.0			V	
	3106A, 3106, 3106-8 ONLY					
$\|I_O\|$	OUTPUT LEAKAGE FOR HIGH IMPEDANCE STATE			100	μA	V_{CC} = 5.25V V_O = 0.45V/5.25V
I_{SC}	OUTPUT SHORT CIRCUIT CURRENT	−15		−65	mA	V_O = 0V V_{CC} = 5V
V_{OH}	OUTPUT HIGH VOLTAGE	2.4			V	I_O = 3.2 mA V_{CC} = 4.75V

(1) Typical values are for T_A = 25° C and nominal supply voltages.

A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

READ CYCLE					
SYMBOL	TEST		LIMITS (ns) MIN.	TYP.	MAX.
t_{A-}, t_{A+}	ADDRESS TO OUTPUT DELAY (ALL CHIP SELECTS LOW)	3106A/3107A	15	40	60
		3106, 3107, 3106-8,3107-8	15	50	80
t_{S-}, t_{S+}	CHIP SELECT TO OUTPUT DELAY (ALL ADDRESS INPUTS STABLE)		5	25	40

WRITE CYCLE					
SYMBOL	TEST		LIMITS (ns) MIN.	TYP.	MAX.
t_{WP}	WRITE ENABLE PULSE WIDTH	3106A,3107A	50	35	
		3106,3107	60	45	
		3106-8,3107-8	80	70	
t_{SR}	TIME INPUT DATA APPEARS AT THE OUTPUT FOLLOWING A WRITE COMMAND. t_{WP}≥MIN. LIMIT			10	25

3106A, 3106, 3106-8 ONLY

SYMBOL	TEST	MIN.	MAX.
t_{ON}	TIME OUTPUT REACHES LOW IMPEDANCE STATE AFTER CHIP ENABLED	0	
t_{OFF}	TIME OUTPUT REACHES HIGH IMPEDANCE STATE AFTER CHIP DISABLED		20

CAPACITANCE, T_A = 25°C

SYMBOL	TEST	PACKAGE	LIMITS (pF) TYP.	MAX.
C_{IN}*	INPUT CAPACITANCE (ALL INPUT PINS)	PLASTIC	6	8
	ALL DEVICES	CERDIP	7	10
C_{OUT}*	OUTPUT CAPACITANCE	PLASTIC	8	11
	ALL DEVICES	CERDIP	9	13

*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

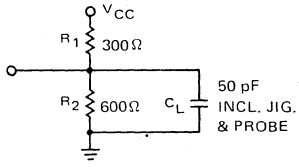
Conditions of Test:

Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times: 5 nanoseconds between 1 volt and 2 volts

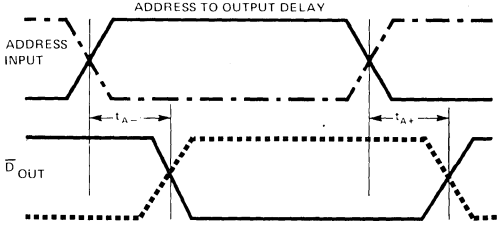
Measurements made at 1.5 volt level

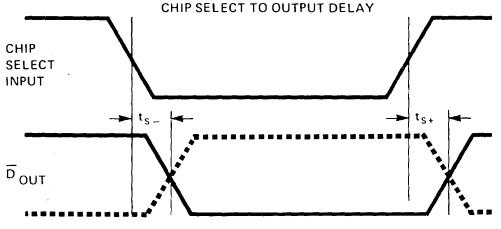
Test Load



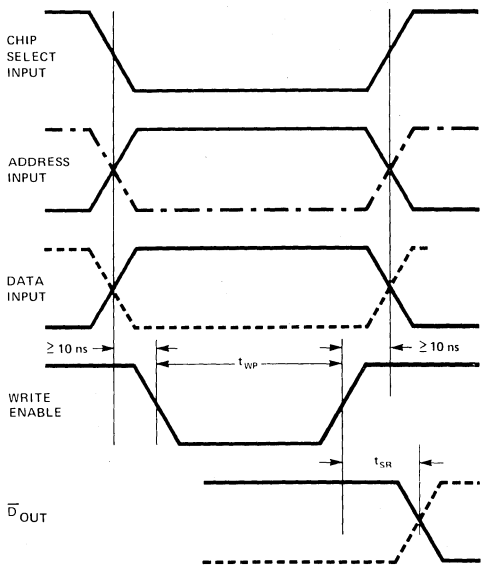
Waveforms

READ CYCLE



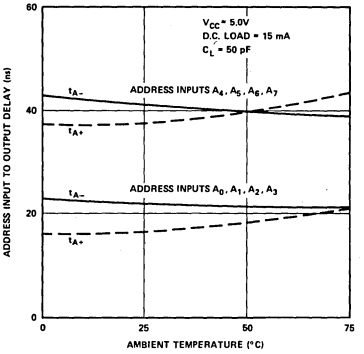


WRITE CYCLE

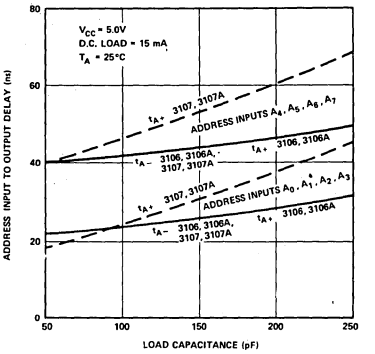


Typical A. C. Characteristics

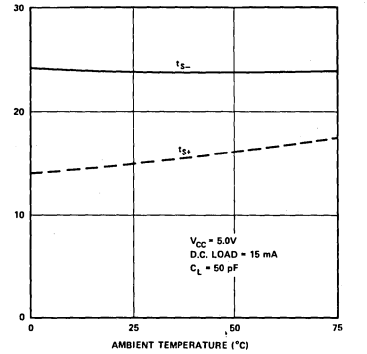
ADDRESS INPUT TO OUTPUT DELAY VS TEMPERATURE (3106, 3106A, 3107, 3107A)



ADDRESS INPUT TO OUTPUT DELAY VS LOAD CAPACITANCE (3106, 3106A, 3107, 3107A)

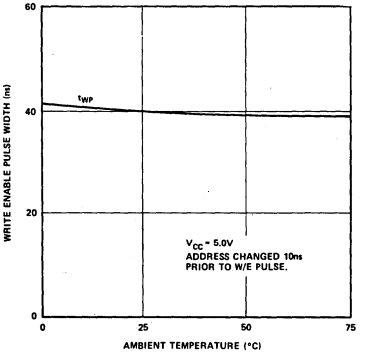


CHIP SELECT TO OUTPUT DELAY VS TEMPERATURE (3106, 3106A, 3107, 3107A)

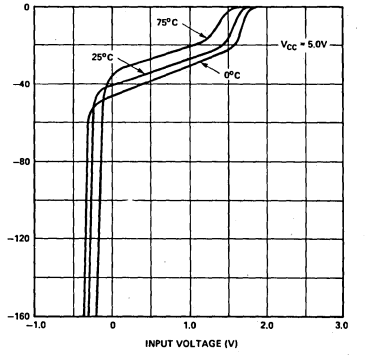


Typical D. C. Characteristics

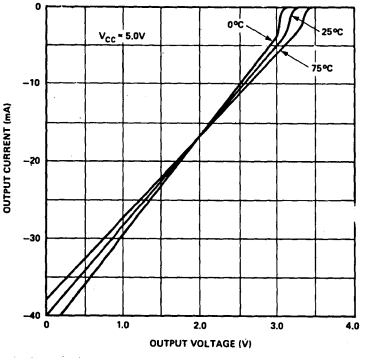
WRITE ENABLE PULSE WIDTH VS TEMPERATURE (3106, 3106A, 3107, 3107A)



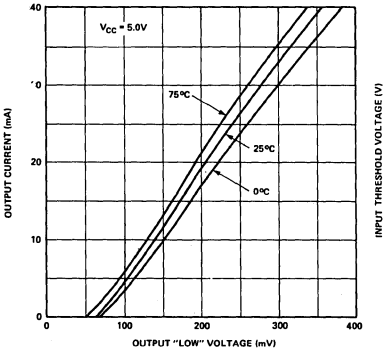
INPUT CURRENT VS INPUT VOLTAGE (3106, 3106A, 3107, 3107A)



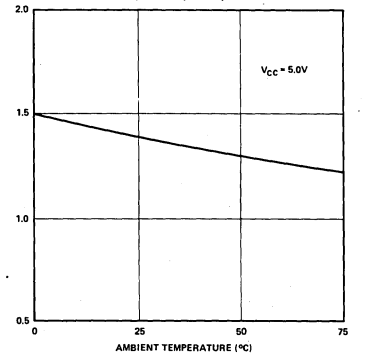
OUTPUT "HIGH" VOLTAGE VS OUTPUT CURRENT (3106 & 3106A ONLY)



OUTPUT "LOW" VOLTAGE VS OUTPUT CURRENT (3106, 3106A, 3107, 3107A)



INPUT THRESHOLD VOLTAGE VS TEMPERATURE (3106, 3106A, 3107, 3107A)



5101, 5101L

1024 BIT (256 x 4) STATIC CMOS RAM

P/N	Typ. Current @ 2V (μA)	Typ. Standby Current (μA)	Max Access (ns)
5101L	0.14	0.2	650
5101L-1	0.9	1.5	450
5101L-3	0.7	1.0	650
5101-1	—	1.5	450
5101	—	0.2	650
5101-3	—	1.0	650
5101-8	—	10.0	800

- **Single +5V Power Supply**
- **Ideal for Battery Operation (5101L)**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Three-State Output**

The Intel® 5101 and 5101L are ultra-low power 1024 bit (256 words x 4-bits) static RAMs fabricated with an advanced ion-implanted silicon gate CMOS technology. The devices have two chip enable inputs. Minimum standby current is drawn by these devices when CE_2 is at a low level. When deselected the 5101 draws from the single 5 volt supply only 15 microamps. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

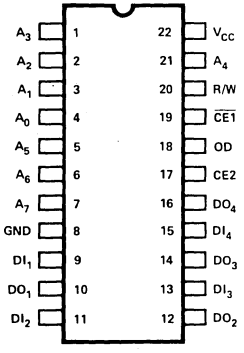
The 5101 uses fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 has separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

The 5101L is identical to the 5101 with the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

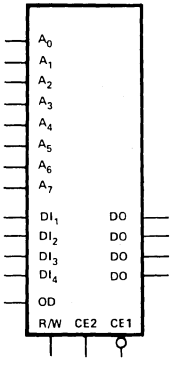
A pin compatible N-channel static RAM, the Intel® 2101A, is also available for low cost applications where a 256 x 4 organization is needed.

The Intel ion-implanted, silicon gate, complementary MOS (CMOS) allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION



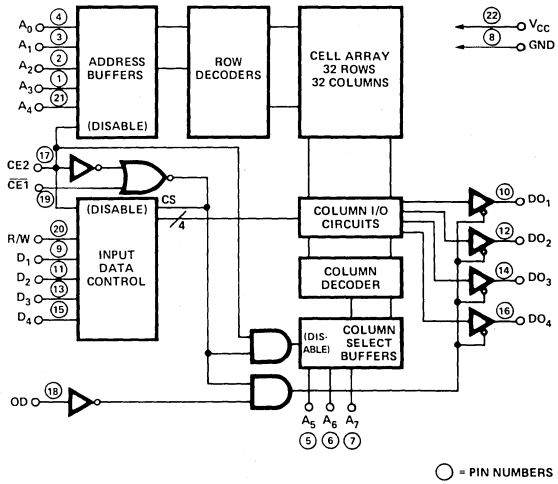
LOGIC SYMBOL



TRUTH TABLE

$\overline{CE_1}$	CE_2	OD	R/W	D_{IN}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

BLOCK DIAGRAM



Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . . .–10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

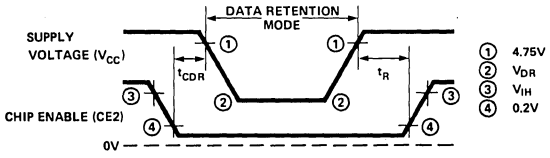
Symbol	Parameter	5101 (Except 5101-8) and 5101L Family Limits Min.	Typ.[1]	Max.	5101-8 Limits Min.	Typ.[1]	Max.	Units	Test Conditions
I_{LI}[2]	Input Current		5			5		nA	
$\|I_{LO}\|$[2]	Output Leakage Current			1			2	µA	$\overline{CE1}$ = 2.2V, V_{OUT} = 0 to V_{CC}
I_{CC1}	Operating Current		9	22		11	25	mA	V_{IN} = V_{CC}, Except $\overline{CE1} \leqslant 0.65V$, Outputs Open
I_{CC2}	Operating Current		13	27		15	30	mA	V_{IN} = 2.2V, Except $\overline{CE1} \leqslant 0.65V$, Outputs Open
I_{CCL1}[2]	5101 and 5101-1 Standby Current			15			—	µA	CE2 ⩽ 0.2V, V_{CC} = 5V ±5%
I_{CCL2}[2]	5101-3 Standby Current		1	200			—	µA	CE2 ⩽ 0.2V, V_{CC} = 5V ±5%
I_{CCL3}[2]	5101-8 Standby Current			—		10	50	µA	CE2 ⩽ 0.2V, V_{CC} = 5V ±5%, T_A = 25°C
I_{CCL4}[2]	5101-8 Standby Current			—			500	µA	CE2 ⩽ 0.2V, V_{CC} = 5V ±5%, T_A = 70°C
V_{IL}	Input Low Voltage	-0.3		0.65	-0.3		0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = 1.0mA

Low V_{CC} Data Retention Characteristics (For 5101L, 5101L-1, and 5101L-3) T_A = 0°C to 70°C

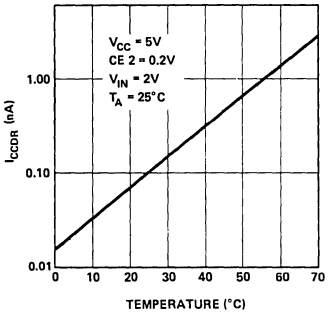
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2 ⩽ 0.2V	
I_{CCDR1}	5101L or 5101L-1 Data Retention Current		0.14	15	µA		V_{DR} = 2.0V
I_{CCDR2}	5101L-3 Data Retention Current		0.7	200	µA		V_{DR} = 2.0V
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I_{CCL} measurement. 3. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Typical I_{CCDR} Vs. Temperature



A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

READ CYCLE

Symbol	Parameter	5101-1, 5101L-1 Limits (ns) Min.	Max.	5101, 5101-3, 5101L and 5101L-3 Limits (ns) Min.	Max.	5101-8 Limits (ns) Min.	Max.
t_{RC}	Read Cycle	450		650		800	
t_A	Access Time		450		650		800
t_{CO1}	Chip Enable ($\overline{CE}$ 1) to Output		400		600		800
t_{CO2}	Chip Enable (CE 2) to Output		500		700		850
t_{OD}	Output Disable to Output		250		350		450
t_{DF}	Data Output to High Z State	0	130	0	150	0	200
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0		0		0	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0	
WRITE CYCLE							
t_{WC}	Write Cycle	450		650		800	
t_{AW}	Write Delay	130		150		200	
t_{CW1}	Chip Enable ($\overline{CE}$ 1) to Write	350		550		650	
t_{CW2}	Chip Enable (CE 2) to Write	350		550		650	
t_{DW}	Data Setup	250		400		450	
t_{DH}	Data Hold	50		100		100	
t_{WP}	Write Pulse	250		400		450	
t_{WR}	Write Recovery	50		50		100	
t_{DS}	Output Disable Setup	130		150		200	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

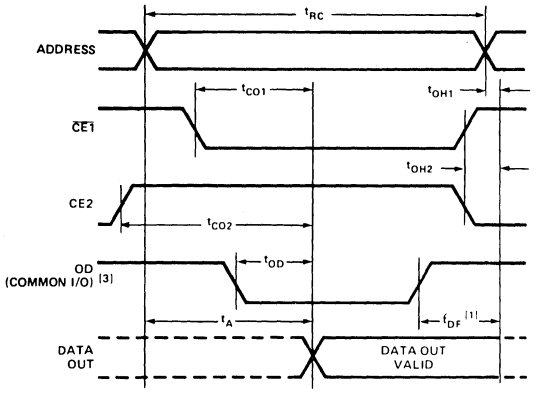
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[2] T_A = 25°C, f = 1MHz

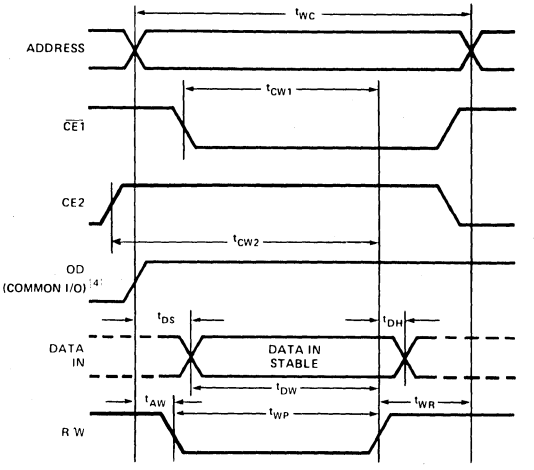
Symbol	Test	Limits (pF) Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

Waveforms

READ CYCLE



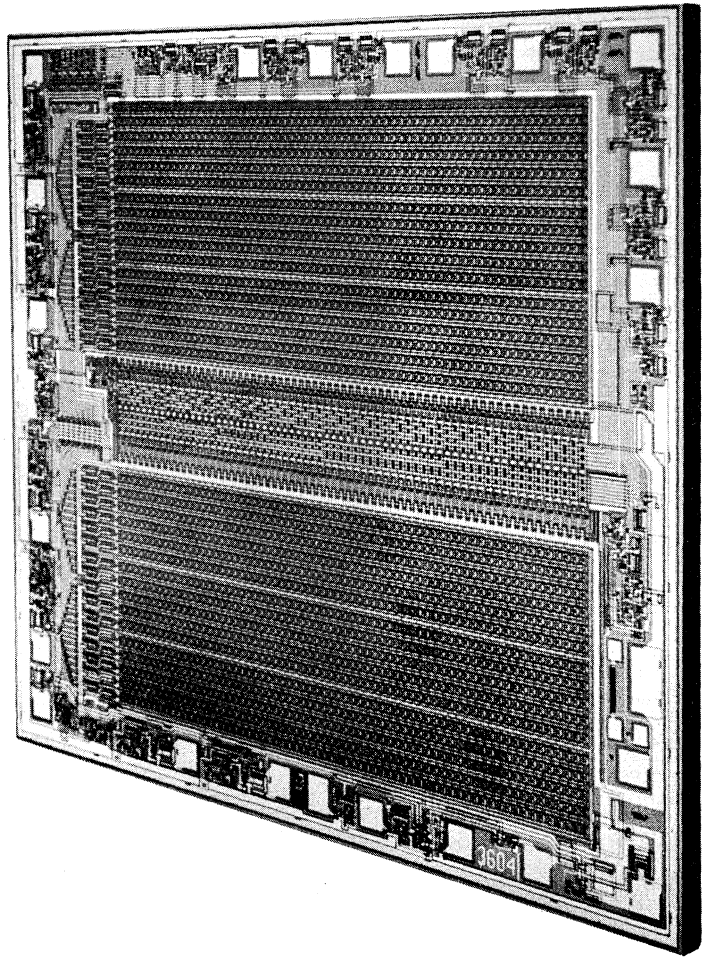
WRITE CYCLE



NOTES:
1. Typical values are for $T_A = 25^\circ C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. OD may be tied low for separate I/O operation.
4. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

3

READ ONLY MEMORIES



MOS ROM AND PROM FAMILY

	Type	No Of Bits	Organization	Output[1]	Maximum Access (ns)	Maximum Power Dissipation (mW)	Operating Temperature Range (°C)	Power Supply (V)	Page No.
SILICON GATE MOS ROM	1302	2048	256 x8	T.S.	1 us	885	0 to 70	5V ± 5% -9V ± 5%	3-5
	2308	8192	1024 x 8	T.S.	450	775	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%	3-16
	2316A	16384	2048 x8	T.S.	850	515	0 to 70	5V ± 5%	3-20
SILICON GATE MOS PROM	1702A	2048	256 x8	T.S.	1 us	885	0 to 70	5V ± 5% -9V ± 5%	3-9
	1702AL	2048	256 x8	T.S.	1 us	221	0 to 70	5V ± 5% -9V ± 5%	3-13
	1702A-2	2048	256 x8	T.S.	650	959	0 to 70	5V ± 5% -9V ± 5%	3-9
	1702AL-2	2048	256 x8	T.S.	650	221	0 to 70	5V ± 5% -9V ± 5%	3-13
	1702A-6	2048	256 x8	T.S.	1.5 us	885	0 to 70	5V ± 5% -9V ± 5%	3-9
	2704	4096	512 x 8	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%	3-23
	2708	8192	1024 x 8	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%	3-23

Note 1: O.C. and T.S. are open collector and three-state output respectively.

BIPOLAR ROM AND PROM FAMILY

	Type	No. Of Bits	Organization	Output [1]	Maximum Access (ns)	Maximum Power Dissipation [2] (mW)	Operating Temperature Range (°C)	Power Supply (V)	Page No.
SCHOTTKY BIPOLAR ROMs	3301A	1024	256 x4	O.C.	45	657	0 to 75	5V ± 5%	3-26
	M3301A	1024	256 x4	O.C.	60	657	-55 to 125	5V ± 5%	3-29
	3302A	2048	512 x 4	O.C.	70	735	0 to 75	5V ± 5%	3-31
	3302A-4	2048	512 x 4	O.C.	90	735	0 to 75	5V ± 5%	3-31
	3302AL6	2048	512 x 4	O.C.	90	580/240	0 to 75	5V ± 5%	3-31
	3322A	2048	512 x 4	T.S.	70	735	0 to 75	5V ± 5%	3-31
	3322A-4	2048	512 x 4	T.S.	90	735	0 to 75	5V ± 5%	3-31
	3322AL6	2048	512 x 4	T.S.	90	580/240	0 to 75	5V ± 5%	3-31
	3304A	4096	512 x 8	O.C.	70	998	0 to 75	5V ± 5%	3-34
	3304A-4	4096	512 x 8	O.C.	90	998	0 to 75	5V ± 5%	3-34
	3304AL6	4096	512 x 8	O.C.	90	735/240	0 to 75	5V ± 5%	3-34
	3324A	4096	512 x 8	T.S.	70	998	0 to 75	5V ± 5%	3-34
	3324A-4	4096	512 x 8	T.S.	90	998	0 to 75	5V ± 5%	3-34
SCHOTTKY BIPOLAR PROMs	3601	1024	256 x4	O.C.	70	685	0 to 75	5V ± 5%	3-37
	3601-1	1024	256 x4	O.C.	50	685	0 to 75	5V ± 5%	3-37
	M3601	1024	256 x4	O.C.	90	685	-55 to 125	5V ± 5%	3-41
	3621	1024	256 x4	T.S.	70	685	0 to 75	5V ± 5%	3-37
	3621-1	1024	256 x4	T.S.	50	685	0 to 75	5V ± 5%	3-37
	3602	2048	512 x 4	O.C.	70	735	0 to 75	5V ± 5%	3-43
	3602-4	2048	512 x 4	O.C.	90	735	0 to 75	5V ± 5%	3-43
	3602L-6	2048	512 x 4	O.C.	90	580/240	0 to 75	5V ± 5%	3-43
	3622	2048	512 x 4	T.S.	70	735	0 to 75	5V ± 5%	3-43
	3622-4	2048	512 x 4	T.S.	90	735	0 to 75	5V ± 5%	3-43
	3622L-6	2048	512 x 4	T.S.	90	580/240	0 to 75	5V ± 5%	3-43
	3604	4096	512 x 8	O.C.	70	998	0 to 75	5V ± 5%	3-46
	3604-4	4096	512 x 8	O.C.	90	998	0 to 75	5V ± 5%	3-46
	3604L-6	4096	512 x 8	O.C.	90	735/240	0 to 75	5V ± 5%	3-46
	3624	4096	512 x 8	T.S.	70	998	0 to 75	5V ± 5%	3-46
	3624-4	4096	512 x 8	T.S.	90	998	0 to 75	5V ± 5%	3-46
	M3604	4096	512 x 8	O.C.	90	1045	-55 to 125	5V ± 10%	3-49
	M3604-6	4096	512 x 8	O.C.	120	770/250	-30 to 125	5V ± 5%	3-49
	3605	4096	1024 x 4	O.C.	50	787	0 to 75	5V ± 5%	3-52
	3605-1	4096	1024 x 4	O.C.	70	787	0 to 75	5V ±5%	3-52
	M3624	4096	512 x 8	T.S.	90	1045	-55 to 125	5V ± 10%	3-49
	3625	4096	1024 x 4	T.S.	70	787	0 to 75	5V ± 5%	3-52
	3625-1	4096	1024 x 4	T.S.	50	787	0 to 75	5V ± 5%	3-52

Note 1: O.C. and T.S. are open collector and three-state output respectively.
Note 2: The "L" series devices have a low power dissipation option.

ROM and PROM Programming Instructions	3-55

BIPOLAR PROM CROSS REFERENCE

Part Number	Prefix and Manufacturer	Organization	Intel Part Number	
			Direct Replacement	For New Designs[1]
1024-5	HPROM-Harris	256 x 4	3621	
1024A-2	HPROM-Harris	256 x 4	M3601	
1024A-5	HPROM-Harris	256 x 4	3601	
27S10C	AMD	256 x 4	3601	
27S10M	AMD	256 x 4	M3601	
27S11C	AMD	256 x 4	3621	
27S11M	AMD	256 x 4	M3621	
5300	MMI	256 x 4	M3601	
5300-1	MMI	256 x 4	M3601	
5340	MMI	512 x 8	M3604	
5341-1	MMI	512 x 8	M3624	
54S387	SN-TI	256 x 4	M3601	
54S387	DM-National	256 x 4	M3601	
5603AC	IM-Intersil	256 x 4	3601	
5603AM	IM-Intersil	256 x 4	M3601	
5604C	IM-Intersil	512 x 4	3602	
5605C	IM-Intersil	512 x 8	3604	
5623C	IM-Intersil	256 x 4	3621	
5624C	IM-Intersil	512 x 4	3622	
5625C	IM-Intersil	512 x 8	3624	
6300	MMI	256 x 4	3601	
6300-1	MMI	256 x 4	3601-1	
6301	MMI	256 x 4	3621	
6301-1	MMI	256 x 4	3621	
6305	MMI	512 x 4	3602	
6305-1	MMI	512 x 4	3602	
6306	MMI	512 x 4	3622	
6306-1	MMI	512 x 4	3622	
6340	MMI	512 x 8	3604	
6341-1	MMI	512 x 8	3624	
6350	MMI	1024 x 4		3605
6351	MMI	1024 x 4		3625

Part Number	Prefix and Manufacturer	Organization	Intel Part Number	
			Direct Replacement	For New Designs[1]
74S287	SN-TI	256 x 4	3621-1	
74S287	DM-National	256 x 4	3621-1	
74S387	SN-TI	256 x 4	3601-1	
74S387	DM-National	256 x 4	3601-1	
7573	DM-National	256 x 4	M3601	
7610-2	HM-Harris	256 x 4		M3601
7610-5	HM-Harris	256 x 4	3601-1	
7611-5	HM-Harris	256 x 4	3621-1	
7620-5	HM-Harris	512 x 4	3602	
7621-5	HM-Harris	512 x 4	3622	
7640-2	HM-Harris	512 x 8		M3604
7640-5	HM-Harris	512 x 8	3604	
7641-2	HM-Harris	512 x 8		M3624
7641-5	HM-Harris	512 x 8	3624	
7642-5	HM-Harris	1024 x 4	3605	
7643-5	HM-Harris	1024 x 4	3625	
82S115	N-Signetics	512 x 8		3624
82S115	S-Signetics	512 x 8	M3624	
82S126	N-Signetics	256 x 4	3601-1	
82S126	S-Signetics	256 x 4		M3601
82S129	N-Signetics	256 x 4	3621-1	
82S130	N-Signetics	512 x 4		3602
82S131	N-Signetcis	512 x 4		3622
8573	DM-National	256 x 4	3601	
8574	DM-National	256 x 4	3621	
93416C	Fairchild	256 x 4	3601	
93416M	Fairchild	256 x 4		M3601
93426C	Fairchild	256 x 4	3621	
93436C	Fairchild	512 x 4		3602
93438C	Fairchild	512 x 8		3604
93438M	Fairchild	512 x 8		M3604
93446C	Fairchild	512 x 4		3622
93448C	Fairchild	512 x 8		3624
93448M	Fairchild	512 x 8		M3624

Note 1. The Intel® PROMs have the same pin configuration and differ only in access time from the PROMs in the first column. The exceptions are the 6350, 6351 and 82S115 which have different pin configurations.

2048 BIT MASK PROGRAMMABLE READ ONLY MEMORY

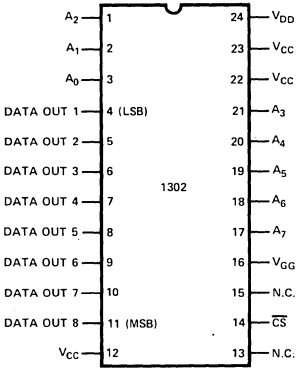
- **Fully Decoded, 256x8 Organization**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-state Output -- OR-tie Capability**
- **Static MOS -- No Clocks Required**
- **Simple Memory Expansion -- Chip Select Input Lead**
- **24-pin Dual-In-Line Hermetically Sealed Ceramic Package**

The Intel®1302 is a fully decoded 256 word by 8-bit metal mask ROM. It is ideal for large volume production runs of systems initially using the 1702A erasable and electrically programmable ROM. The 1302 has the same pinning as the 1602A/1702A.

The 1302 is entirely static — no clocks are required. Inputs and outputs of the 1302 are DTL and TTL compatible. The output is three-state for OR-tie capability. A separate chip select input allows easy memory expansion. The 1302 is packaged in a 24 pin dual-in-line hermetically sealed ceramic package.

The 1302 is fabricated with p-channel silicon gate technology. This low threshold allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

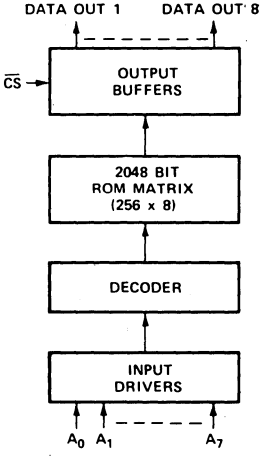
PIN CONFIGURATION



PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: LOGIC 1 AT INPUT AND OUTPUT IS A HIGH AND LOGIC 0 IS LOW.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... −65°C to +125°C
Soldering Temperature of Leads (10 sec) ..... +300°C
Power Dissipation ..... 2 Watts
Input Voltages and Supply
Voltages with respect to V_{CC} .....+0.5V to −20V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = −9V±5%, V_{GG}[1] = −9V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP[2]	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	µA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1	µA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DDO}	Power Supply Current		5	10	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC}−2 I_{OL} = 0.0mA, T_A = 25°C
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$=0.0 I_{OL} =0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA , T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
						Continuous Operation
I_{GG}	Gate Supply Current			1	µA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}−2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100 µA

Note 1. V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} increases in proportion to V_{GG} duty cycle.
Note 2. Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0° C to +70° C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay		.700	1	µs
t_{DVGG}	Clocked V_{GG} set up	1			µs
t_{CS}	Chip select delay			200	ns
t_{CO}	Output delay from $\overline{CS}$			500	ns
t_{OD}	Output deselect			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	µs

Note 1. The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Capacitance* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		5	10	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		5	10	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Clocked V_{GG} Mode)			30	pF	

*This parameter is periodically sampled and is not 100% tested.

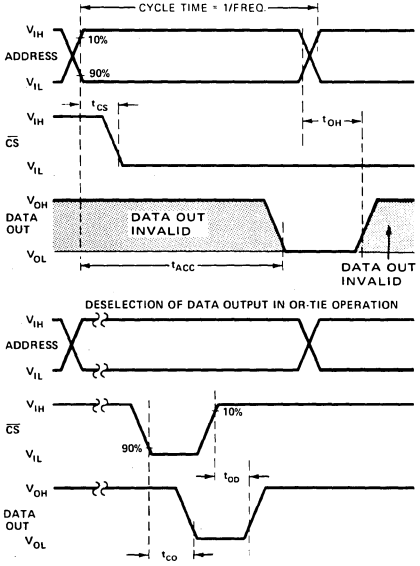
Switching Characteristics

Conditions of Test:

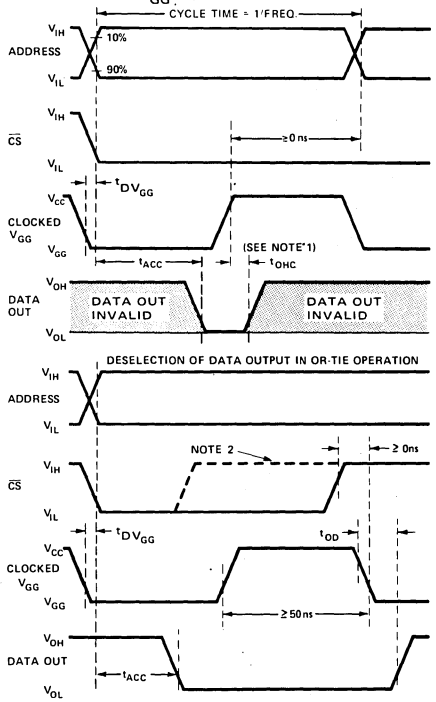
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD} ≤15 ns)

A) Constant V_{GG} Operation



B) Clocked V_{GG} Operation

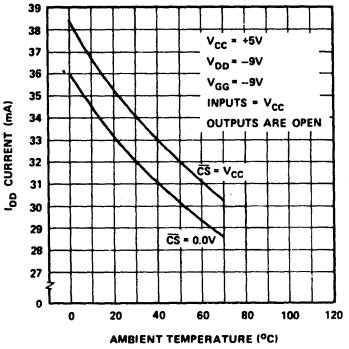


NOTE 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

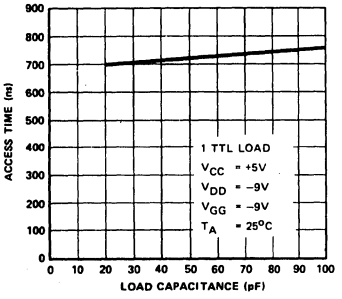
NOTE 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

Typical Characteristics

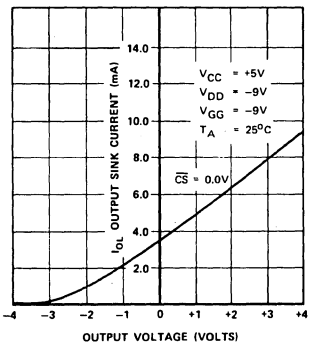
I_{DD} CURRENT VS. TEMPERATURE



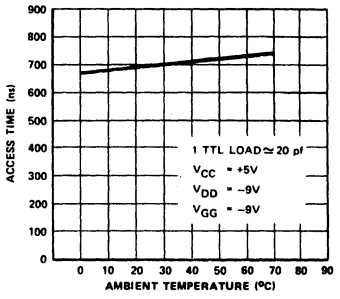
ACCESS TIME VS. LOAD CAPACITANCE



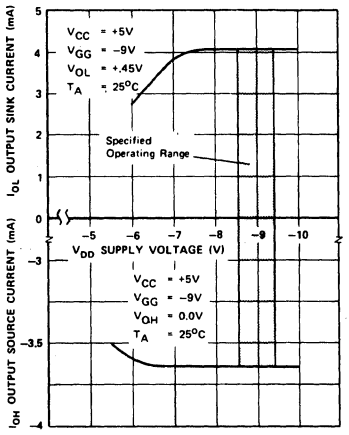
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



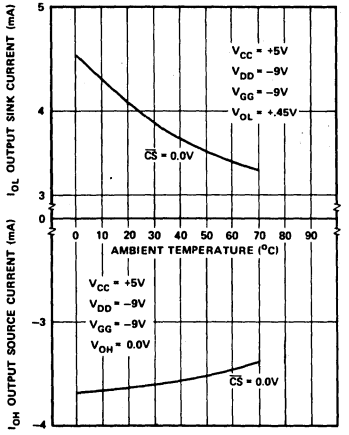
ACCESS TIME VS. TEMPERATURE



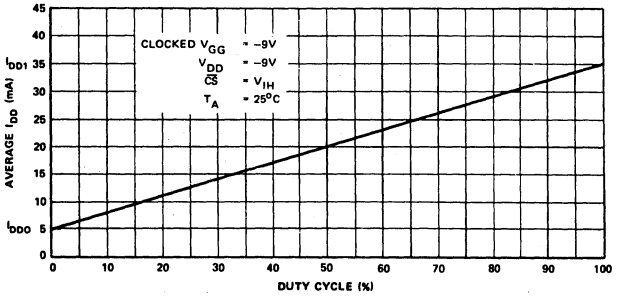
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



OUTPUT CURRENT VS. TEMPERATURE



AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



1702A

2K (256 x 8) UV ERASABLE PROM

1702A-2	0.65 us Max.
1702A	1.0 us Max.
1702A-6	1.5 us Max.

- **Fast Access Time: Max. 650 ns (1702A–2)**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

The 1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The 1702A undergoes complete programming and functional testing prior to shipment, thus insuring 100% programmability.

Initially all 2048 bits of the 1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702A to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

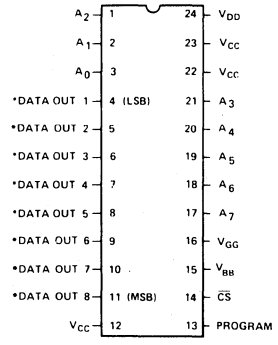
The circuitry of the 1702A is completely static. No clocks are required. Access times from 650ns to 1.5μs are available. A 1702AL family is available (see 1702AL data sheets for specifications) for those systems requiring lower power dissipation than the 1702A.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is also available for large volume production runs of systems initially using the 1702A.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

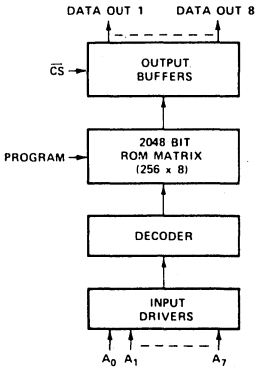


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702A differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the ROM and PROM Programming instructions section, pages 3-57.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG} = -9V ±5%, unless otherwise noted.

READ OPERATION

Symbol	Test	1702A, 1702A-6 Limits Min.	Typ.[1]	Max.	1702A-2 Limits Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50		40	60	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		37	55	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		43	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		7	13	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		6	12	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH1}	Addr. Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
V_{IH2}	Chip Sel. Input High Volt.	V_{CC}-2		V_{CC}+0.3	V_{CC}-1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

Note 1: Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

Symbol	Test	1702A Limits Min.	1702A Limits Max.	1702A-2 Limits Min.	1702A-2 Limits Max.	1702A-6 Limits Min.	1702A-6 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6		0.66	MHz
t_{OH}	Previous Read Data Valid		0.1		0.1		0.1	μs
t_{ACC}	Address to Output Delay		1		0.65		1.5	μs
t_{CS}	Chip Select Delay		0.1		0.3		0.6	μs
t_{CO}	Output Delay From $\overline{CS}$		0.9		0.35		0.9	μs
t_{OD}	Output Deselect		0.3		0.3		0.3	μs

Capacitance* T_A = 25°C

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	

*This parameter is periodically sampled and is not 100% tested.

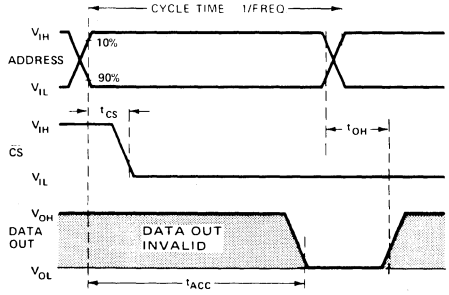
Switching Characteristics

Conditions of Test:

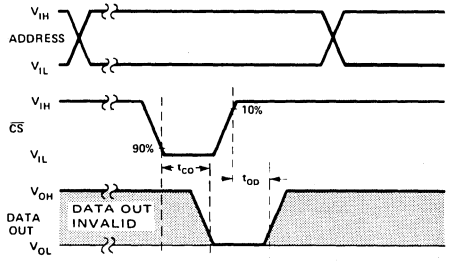
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L=15pF

A) READ OPERATION

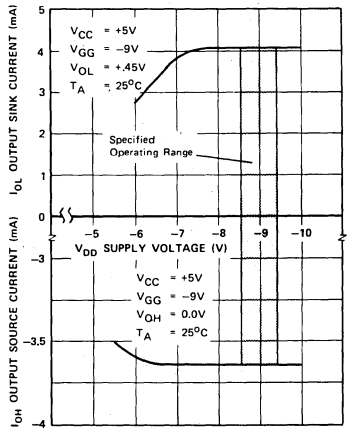


B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION

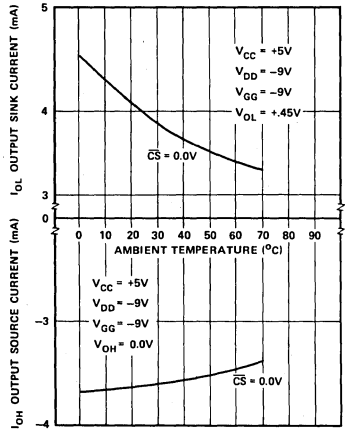


Typical Characteristics

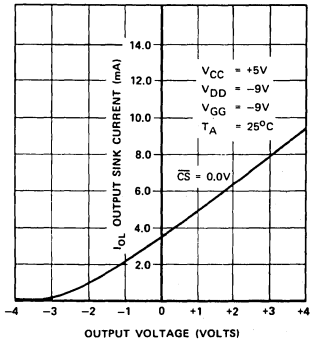
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



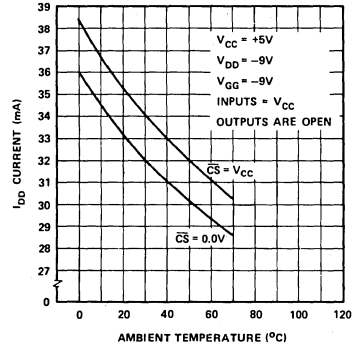
OUTPUT CURRENT VS. TEMPERATURE



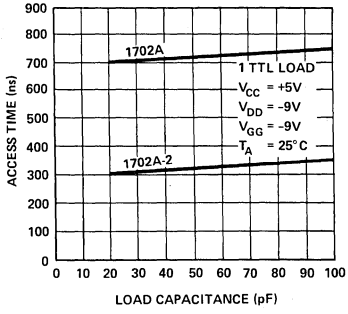
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



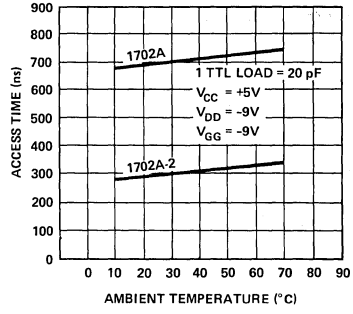
I_{DD} CURRENT VS. TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



1702AL, 1702AL2

2K (256 x 8) UV ERASABLE LOW POWER PROM

Part No.	MAXIMUM ACCESS (μs)	t_{DVGG} (μs)
1702AL	1.0	0.4
1702AL-2	0.65	0.3

- **Clocked V_{GG} Mode for Low Power Dissipation**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

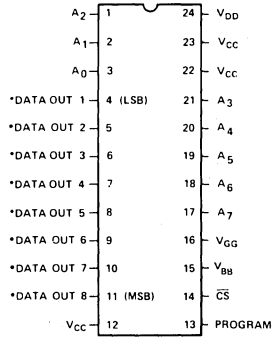
The 1702AL is a 256 word by 8 bit electrically programmable ROM and is the same chip as the industry standard 1702A. The programming and erasing specifications are identical to the 1702A. The 1702AL operates with the V_{GG} clocked to reduce the power dissipation.

Initially all 2048 bits of the 1702AL are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702AL is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702AL to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The 1702AL is fabricated with silicon gate technology. This low threshold technology allows the design and production of high performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

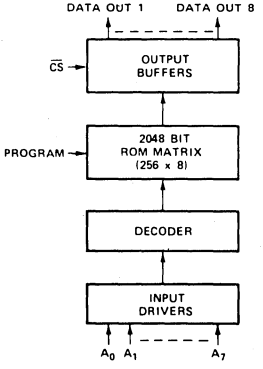


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702AL differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the ROM and PROM Programming Instructions section, pages 3-57.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 (CS)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	Clocked V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

READ OPERATION

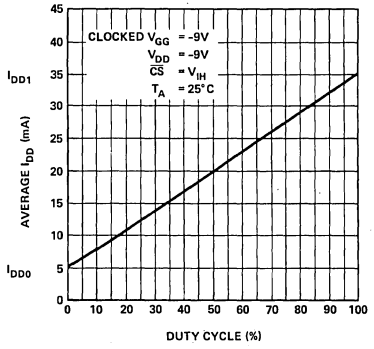
T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG}[1] = -9V ±5%, unless otherwise noted.

Symbol	Test	1702AL Limits Min.	Typ.[2]	Max.	1702AL-2 Limits Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC}-2
I_{DDO1}[1]	Power Supply Current		7	10		7	10	mA	T_A=25°C $\overline{CS}$=V_{IH}, V_{GG}=V_{CC},
I_{DDO2}	Power Supply Current			15			15	mA	T_A=0°C I_{OL}=0.0mA
I_{DD1}[1]	Power Supply Current		35	50		35	50	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		32	46	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		38	60	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		5.5	8	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		5	7	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

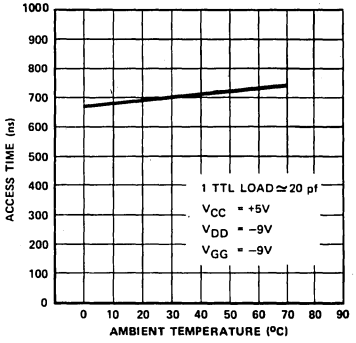
NOTES: 1. The 1702AL is operated with the V_{GG} clocked to obtain low power dissipation. The average I_{DD} will vary between I_{DDO} and I_{DD1} (at 25°C) depending on the V_{GG} duty cycle (see curve opposite). 2. Typical values are at nominal voltage and T_A = 25°C.

Typical Characteristics

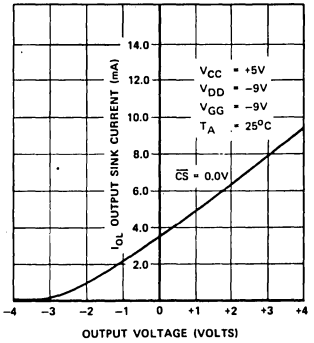
AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



ACCESS TIME VS. TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5% unless otherwise noted

Symbol	Test	1702AL Limits Min.	1702AL Limits Max.	1702AL-2 Limits Min.	1702AL-2 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6	MHz
t_{ACC}	Address to output delay		1		0.65	μs
t_{DVGG}	Clocked V_{GG} set up	0.4		0.3		μs
t_{CS}	Chip select delay		0.1		0.3	μs
t_{CO}	Output delay from $\overline{CS}$		0.9		0.35	μs
t_{OD}	Output deselect		0.3		0.3	μs
t_{OHC}	Data out hold in clocked V_{GG} mode		5		5	μs

Capacitance

T_A = 25°C

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	V_{IN} = V_{CC}, $\overline{CS}$ = V_{CC}, V_{OUT} = V_{CC}, V_{GG} = V_{CC} — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Note 1)		30	pF	

*This parameter is periodically sampled and is not 100% tested.

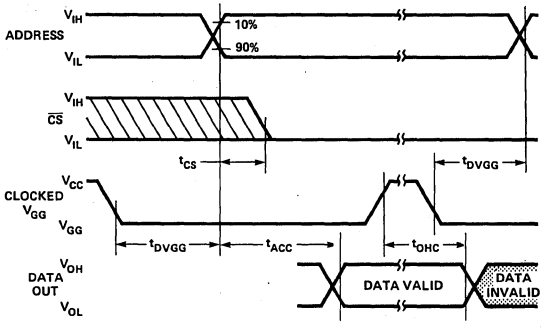
Switching Characteristics

Conditions of Test:

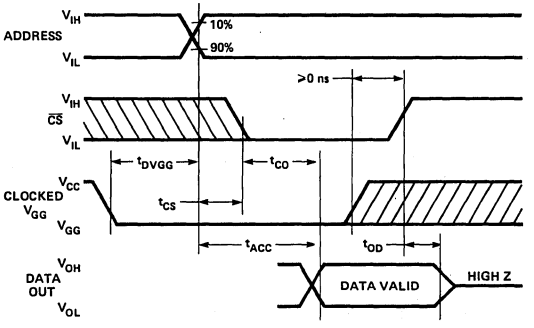
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L = 15pF

A. READ OPERATION



B. DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



ROMs

8192 BIT STATIC MOS READ ONLY MEMORY

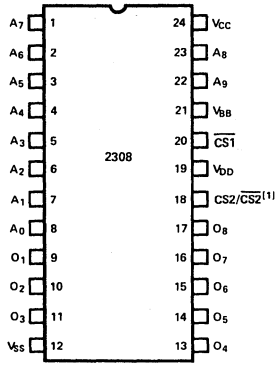
- **Fast Access Time: 450 ns**
- **Standard Power Supplies: +12V, ±5V**
- **TTL Compatible: All Inputs and Outputs**
- **Programmable Chip Select Input for Easy Memory Expansion**
- **Three-State Output: OR-Tie Capability**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Pin Compatible to 2708 PROM**

The Intel 2308 is a 8192 bit static MOS read only memory organized as 1024 words by 8-bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

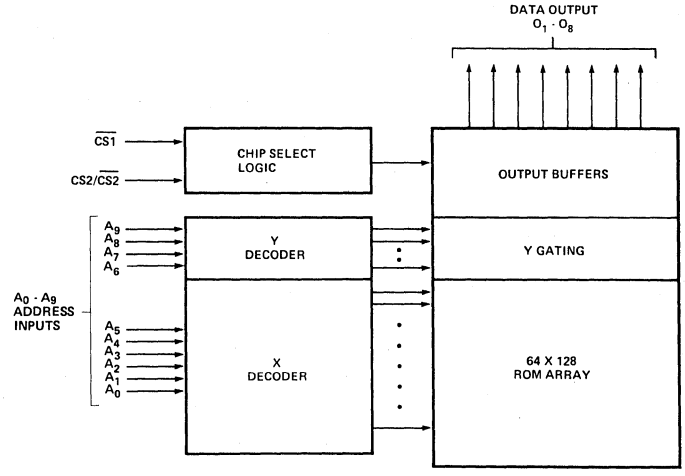
The inputs and outputs are TTL compatible. The chip select input (CS2/$\overline{CS2}$) is programmable. An active high or low level chip select input can be defined by the designer and the desired chip select logic level is fixed at Intel during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion. The pin compatible UV erasable 2708 PROM is available for initial system prototyping.

The 2308 read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS_1}$	CHIP SELECT INPUT
CS2/$\overline{CS2}$[1]	PROGRAMMABLE CHIP SELECT INPUT

NOTE 1. The CS2/$\overline{CS2}$ LOGIC LEVELS MUST BE SPECIFIED BY THE USER AS EITHER A LOGIC 1 (V_{IH}) OR LOGIC 0 (V_{IL}). A LOGIC 0 SHOULD BE SPECIFIED IN ORDER TO BE COMPATIBLE WITH THE 2708.

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To V_{BB} . . . . . -0.3V to 20V
Power Dissipation . . . . . 1.0 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

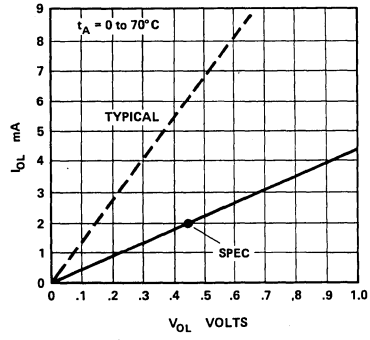
D.C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%; V_{DD} = 12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V Unless Otherwise Specified.

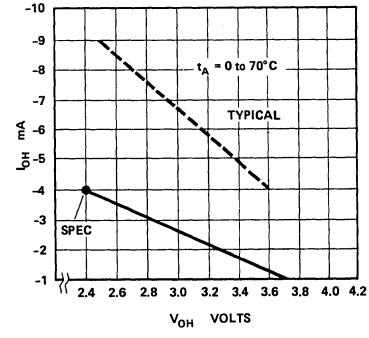
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins Except $\overline{CS_1}$)		1	10	μA	V_{IN} = 0 to 5.25V
I_{LCL}	Input Load Current on $\overline{CS_1}$			1.6	mA	V_{IN} = 0.45V
I_{LPC}	Input Peak Load Current on $\overline{CS_1}$			4	mA	0.8V ≤ V_{IN} < 3.3V
I_{LKC}	Input Leakage Current on $\overline{CS_1}$			10	μA	V_{IN} = 3.3V to 5.25V
I_{LO}	Output Leakage Current			10	μA	Chip Deselected
V_{IL}	Input "Low" Voltage	V_{SS}-1		0.8V	V	
V_{IH}	Input "High" Voltage	3.3		V_{CC}+1.0	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2mA
V_{OH1}	Output "High" Voltage	2.4			V	I_{OH} = -4mA
V_{OH2}	Output "High" Voltage	3.7			V	I_{OH} = -1mA
I_{CC}	Power Supply Current V_{CC}		0.8	2	mA	
I_{DD}	Power Supply Current V_{DD}		32	60	mA	
I_{BB}	Power Supply Current V_{BB}		0.01	1	mA	
P_D	Power Dissipation			775	mW	

NOTE 1: Typical values for T_A = 25°C and nominal supply voltage

D.C. OUTPUT CHARACTERISTICS



D.C. OUTPUT CHARACTERISTICS



A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%; V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Specified.

Symbol	Parameter	Limits[2]		Unit
		Typ.	Max.	
t_{ACC}	Address to Output Delay Time	200	450	ns
t_{CO1}	Chip Select 1 to Output Delay Time	85	160	ns
t_{CO2}	Chip Select 2 to Output Delay Time	125	220	ns
t_{DF}	Chip Deselect to Output Data Float Time	125	220	ns

NOTE 2: Refer to conditions of Test for A.C. Characteristics. Add 50 nanoseconds (worst case) to specified values at V_{OH} = 3.7V @ I_{OH} = -1mA, C_L = 100pF.

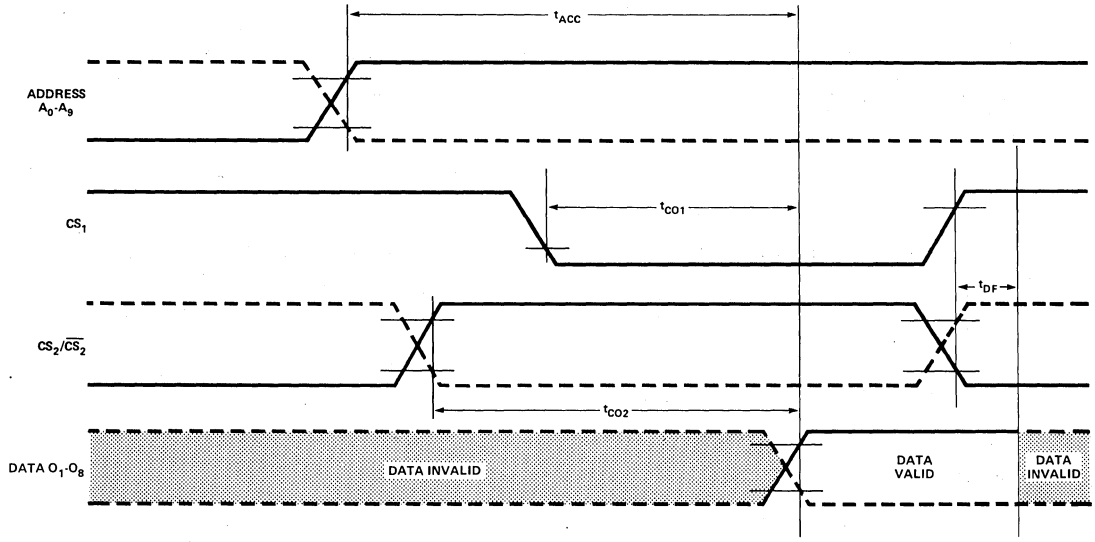
CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . . 1 TTL Gate, and C_{LOAD} = 100pF
Input Pulse Levels . . . . . .65V to 3.3V
Input Pulse Rise and Fall Times . . . . . 20 nsec
Timing Measurement Reference Level
. . . . . 2.4V V_{IH}, V_{OH}; 0.8V V_{IL}, V_{OL}

CAPACITANCE* T_A = 25°C, f = 1 MHz, V_{BB} = -5V, V_{DD}, V_{CC} and all other pins tied to V_{SS}.

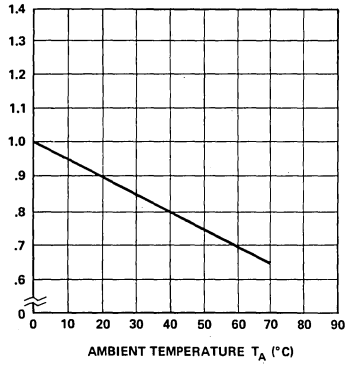
Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	Input Capacitance		6pF
C_{OUT}	Output Capacitance		12pF

*This parameter is periodically sampled and is not 100% tested.

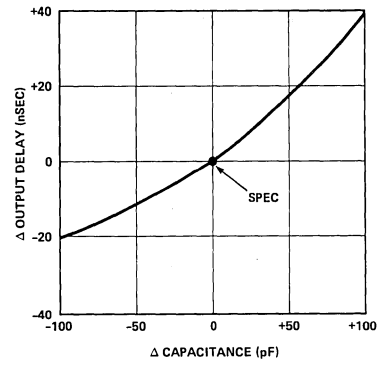


Typical Characteristics (Nominal supply voltages unless otherwise noted.)

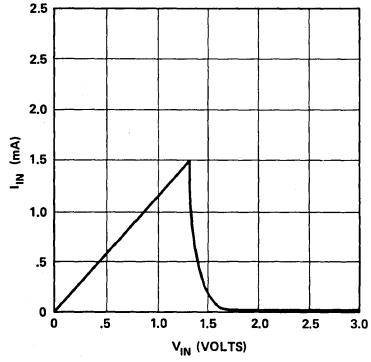
I_{DD} VS. TEMPERATURE
(NORMALIZED)



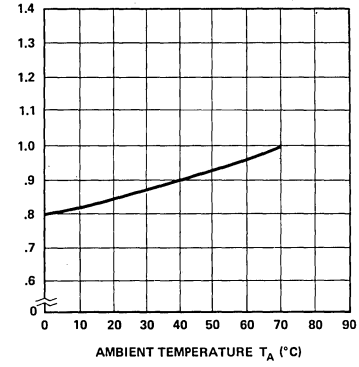
Δ OUTPUT CAPACITANCE
VS. Δ OUTPUT DELAY



$\overline{CS_1}$ INPUT
CHARACTERISTICS



T_{ACC} VS. TEMPERATURE
(NORMALIZED)



16,384 BIT STATIC MOS READ ONLY MEMORY

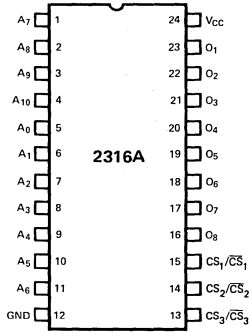
- **Single +5 Volts Power Supply Voltage**
- **Guaranteed 850ns Access Time**
- **Directly TTL Compatible—All Inputs and Outputs**
- **Three Programmable Chip Select Inputs for Easy Memory Expansion**
- **Three-State Output—OR-Tie Capability**
- **Fully Decoded—On Chip Address Decode**
- **Inputs Protected—All Inputs Have Protection Against Static Charge**

The Intel 2316A is a 16,384 bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 2316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

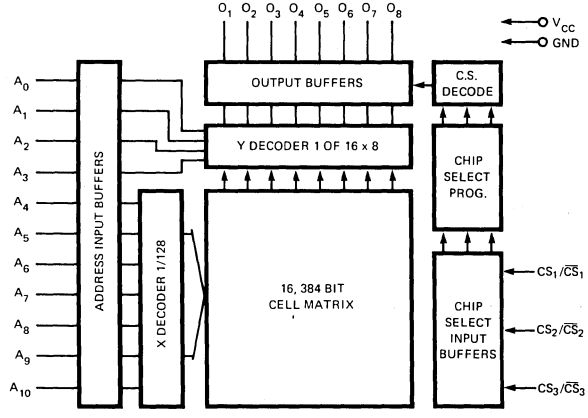
PIN CONFIGURATION



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
CS_1-CS_3	PROGRAMMABLE CHIP SELECT INPUTS

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

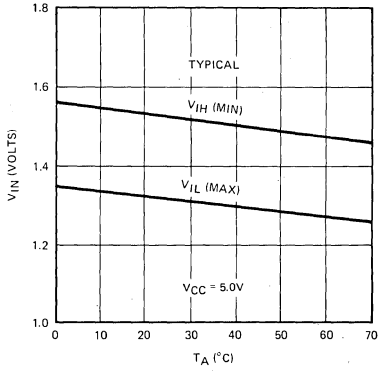
D.C. and Operating Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	μA	CS = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			-20	μA	CS = 2.2V, V_{OUT} = 0.45V
I_{CC}	Power Supply Current		40	98	mA	All inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100 μA

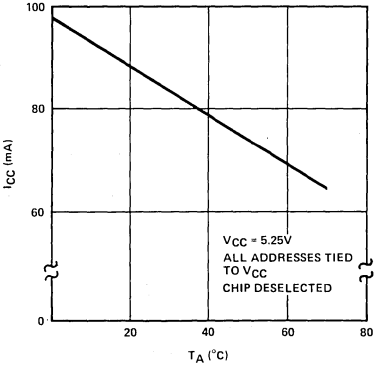
(1) Typical values for T_A = 25°C and nominal supply voltage.

Typical D.C. Characteristics

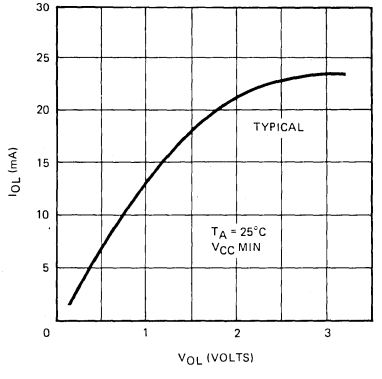
V_{IN} LIMITS VS. TEMPERATURE



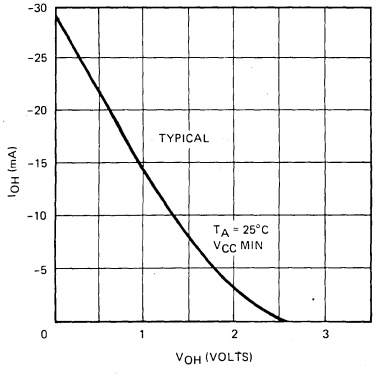
STATIC I_{CC} VS. AMBIENT TEMPERATURE WORST CASE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_A	Address to Output Delay Time		400	850	nS
t_{CO}	Chip Select to Output Enable Delay Time			300	nS
t_{DF}	Chip Deselect to Output Data Float Delay Time	0		300	nS

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

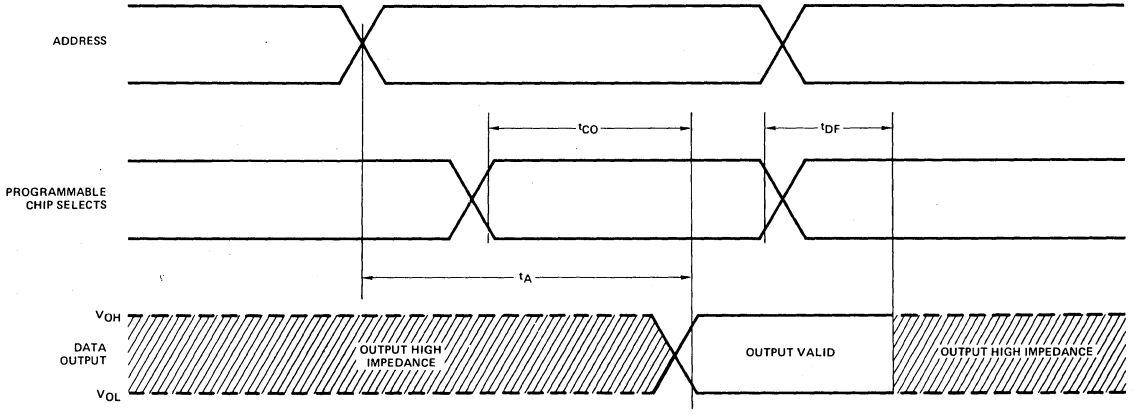
Output Load . . . 1 TTL Gate, and C_{LOAD} = 100 pF
Input Pulse Levels . . . . . 0.8 to 2.0V
Input Pulse Rise and Fall Times . (10% to 90%) 20 nS
Timing Measurement Reference Level
Input 1.5V
Output . . . . . 0.45V to 2.2V

CAPACITANCE(2) $T_A = 25°C$, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

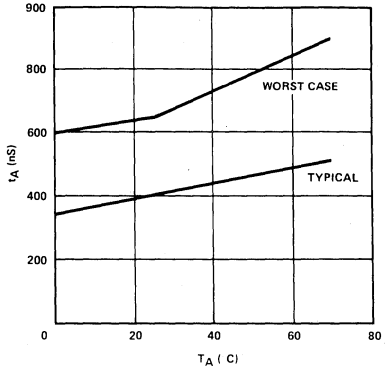
(2) This parameter is periodically sampled and is not 100% tested.

A.C. Waveforms

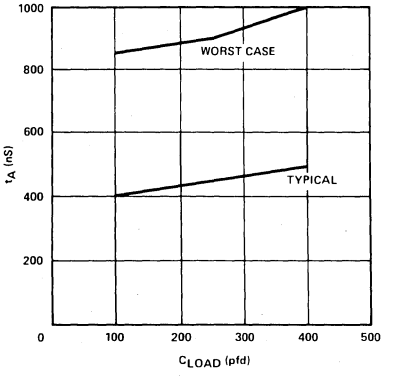


Typical A.C. Characteristics

ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



8K AND 4K UV ERASABLE PROM

- 2708 1024x8 Organization
- 2704 512x8 Organization

- Fast Programming — Typ. 100 sec. For All 8K Bits
- Low Power During Programming
- Access Time — 450 ns Max.
- Standard Power Supplies — +12V, +5V, -5V
- Static — No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Three-State Output — OR-Tie Capability

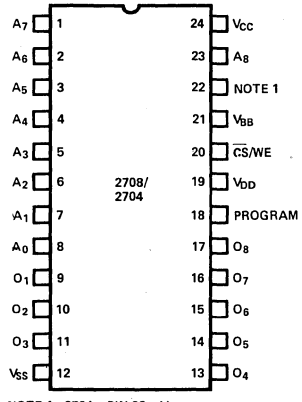
The Intel 2708/2704 are high speed 8192/4096 bit erasable and electrically reprogrammable ROM's (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 2708/2704 are packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

A pin for pin mask programmed ROM, the Intel 2308, is available for large volume production runs of systems initially using the 2708.

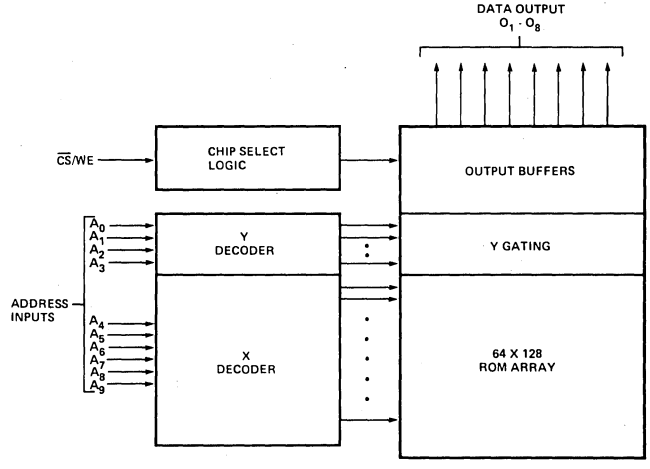
The 2708/2704 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATIONS



NOTE 1. 2704: PIN 22 = V_{SS}.
2708: PIN 22 = A_9.

BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER						
MODE	9-11, 13-17	12	18	19	20	21	24
READ	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
PROGRAM	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

PROGRAMMING

The programming specifications are in the ROM and PROM Programming Instructions (see page 3-59).

Absolute Maximum Ratings*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to -0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to -0.3V
All Input or Output Voltages With Respect to V_{BB} During Read	+15V to -0.3V
$\overline{CS}$/WE Input With Respect to V_{BB} During Programming	+20V to -0.3V
Program Input With Respect to V_{BB}	+35V to -0 3V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

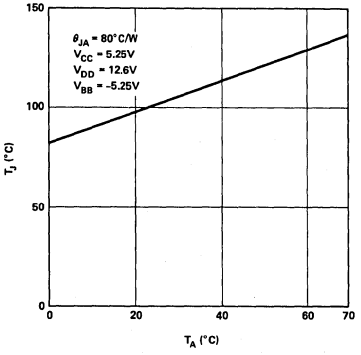
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.25 V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V
I_{DD}[2]	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}[2]	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}[2]	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.

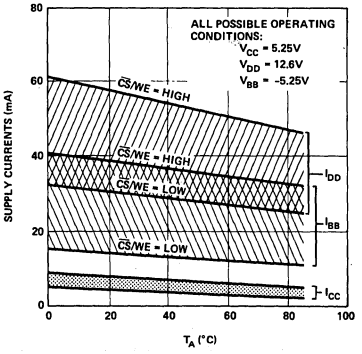
2. The total power dissipation of the 2704/2708 is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

Typical D.C. Characteristics

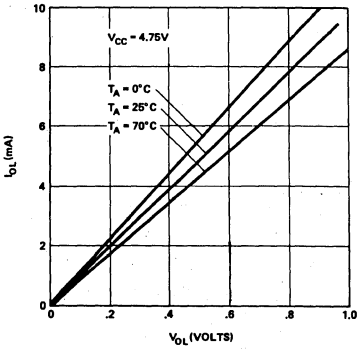
MAXIMUM JUNCTION TEMPERATURE VS. AMBIENT TEMPERATURE



RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
$t_{\overline{CO}}$	Chip Select to Output Delay		60	120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance[1] $T_A = 25°C$, f = 1MHz

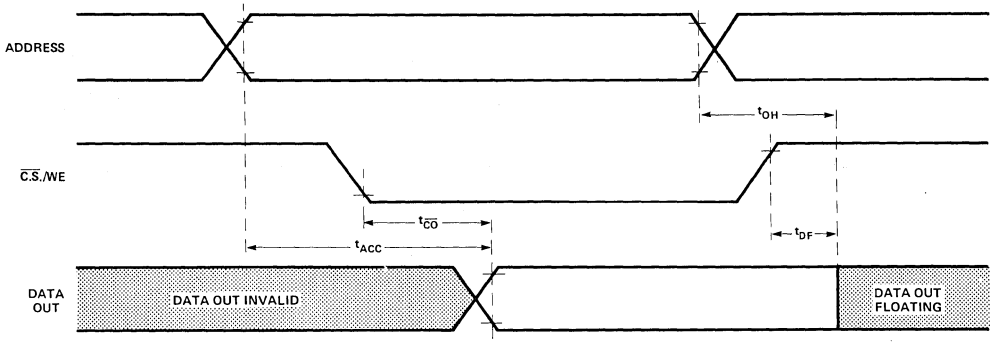
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN}=0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT}=0V$

Note 1. This parameter is periodically sampled and not 100% tested.

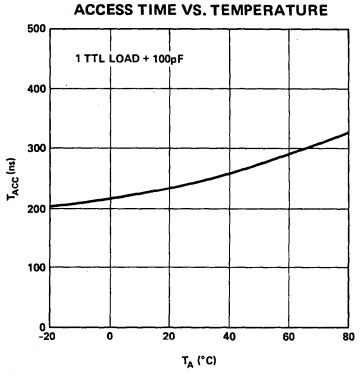
A.C. Test Conditions:

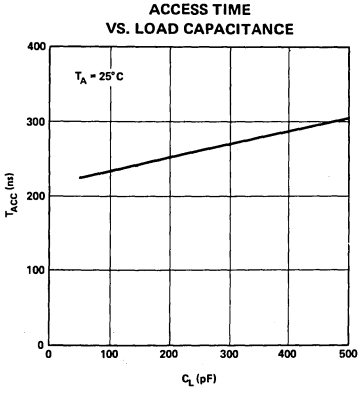
Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤20ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

Waveforms



Typical A.C. Characteristics





3301A

HIGH SPEED FULLY DECODED 1024 BIT READ ONLY MEMORY

- **Fast Access Time--45 nsec Maximum over Temperature and Supply Voltage Variation.**
- **Low Power Dissipation--0.5 mW/bit typical.**
- **DTL and TTL Compatible--Input Loading is .25 mA max.--Outputs sink 15 mA.**
- **OR-Tie Capability--Open Collector Outputs**
- **Simple Memory Expansion--2 Chip Select Input Leads.**
- **Fully Decoded--on Chip Address Decode and Buffer.**
- **Minimum Line Reflection--Low Voltage Diode Input Clamp.**
- **Standard Packaging--16 Pin Dual In-Line Lead Configuration.**

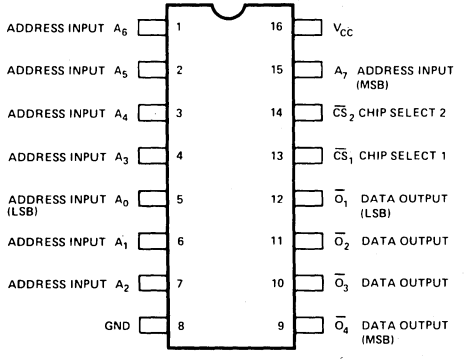
The 3301A is a fully decoded 1024 bit read only memory organized as 256 words by 4 bits. It is a higher speed version of the 3301 and is a direct pin for pin replacement of the 3301. Its performance is specified over the complete ambient temperature range of 0°C to 75°C and a V_{CC} supply voltage range of 5V ± 5%. The 3301A is programmed at the final step of processing which allows fast turnaround.

The OR tie capability and the 2 chip select inputs of the 3301A allow easy memory expansion into larger word and bit lengths.

The 3301A is mask programmed to customized patterns. Ideal applications are in microprogramming and table look up.

The 3301A is manufactured using Schottky barrier diode clamped transistors which allows higher switching speeds than those devices made with conventional gold diffusion process.

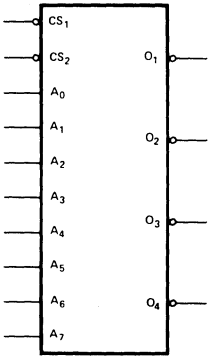
PIN CONFIGURATION



PIN NAMES

A_0–A_7	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$	CHIP SELECT INPUTS
$\overline{O}_1$–$\overline{O}_4$	DATA OUTPUTS

LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias	−65°to +125°C
Storage Temperature	−65°to +160°C
Output or Supply Voltages	−0.5V to 7 Volts
All Input Voltages	-1.1 to 5.5V
Output Currents	100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC}= +5.0V ±5%, T_A= 0°C to +75°C

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.(1)	LIMITS MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT			−0.25	mA	V_{CC}= 5.25V, V_A = 0.45V
I_{FS}	CHIP SELECT INPUT LOAD CURRENT			−0.25	mA	V_{CC}= 5.25V, V_S = 0.45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT			40	μA	V_{CC}= 5.25V, V_A = 5.25V
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT			40	μA	V_{CC}= 5.25V, V_S = 5.25V
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE			−1.0	V	V_{CC}= 4.75V, I_A = −5.0mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE			−1.0	V	V_{CC}= 4.75V, I_S = −5.0mA
V_{OL}	OUTPUT LOW VOLTAGE			0.45	V	V_{CC}= 4.75V, I_{OL} = 15mA
I_{CEX}	OUTPUT LEAKAGE CURRENT			100	μA	V_{CC}= 5.25V, V_{CE} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		90	125	mA	V_{CC}= 5.25V, $V_{A0} \rightarrow V_{A7}$ = 0V V_{S0} = V_{S1} = 0V
V_{IL}	INPUT "LOW" VOLTAGE			0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0			V	V_{CC} = 5.0V

Note 1: Typical values are at 25°C and at nominal voltage.

Switching Characteristics

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	LIMIT TYP.(1)	LIMIT MAX.	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	25	45	ns	Both C.S. lines must be at ground potential to activate the ROM.
t_{S++}, t_{S--}	Chip Select to Output Delay	13	20	ns	

NOTE 1: Typical values are at 25°C and at nominal voltage.

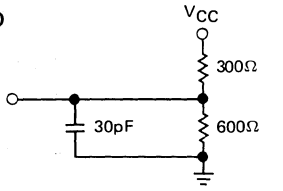
Capacitance(2) T_A = 25°C

SYMBOL	PARAMETER	LIMIT PLASTIC TYP.	LIMIT PLASTIC MAX.	LIMIT CERDIP TYP.	LIMIT CERDIP MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	5	8	6	10	pF	V_{CC} = 5V V_{INA} = 2.5V
C_{INS}	Chip Select Input Capacitance	5	8	5	10	pF	V_{CC} = 5V V_{INS} = 2.5V
C_{OUT}	Output Capacitance	7	10	8	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

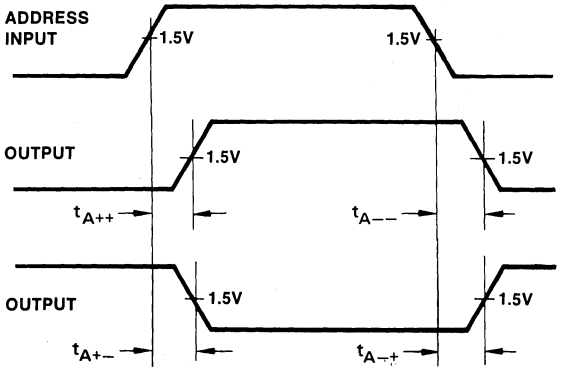
NOTE 2: This parameter is only periodically sampled and is not 100% tested.

Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

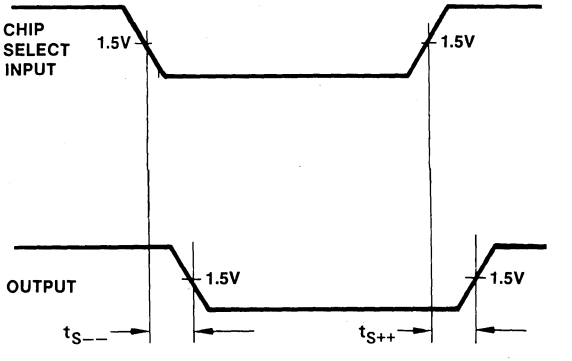
15 mA TEST LOAD



ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY

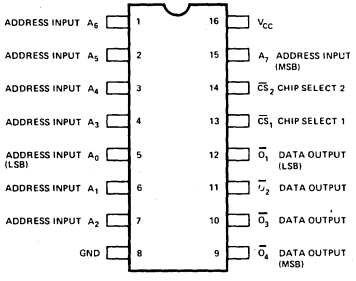


HIGH SPEED 1024 BIT READ ONLY MEMORY

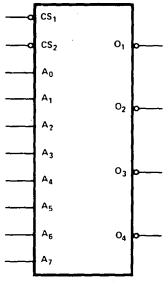
- **Military Temperature Range −55°C to +125°C**
- **Fast Access Time—60 nsec Maximum**
- **OR-Tie Capability— Open Collector Outputs**
- **Standard Packaging — 16 Pin Hermetic Dual In-Line Configuration**

The M3301A is a military temperature range ROM, organized as 256 words by 4-bits. It is mask programmed to customized patterns. Initial circuit prototyping can be performed before going into volume production by using the pin compatible M3601 PROM.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-65°C to +150°C
Storage Temperature	-65°C to +160°C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	-1.3 to 5.5V
Output Currents	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

All limits apply for V_{CC} = +5.0V ±5%, T_A = -55°C to +125°C, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.7	-1.2	V	V_{CC} = 4.75V, I_A = -5.0mA
V_{CS}	Chip Select Input Clamp Voltage		-0.7	-1.2	V	V_{CC} = 4.75V, I_S = -5.0mA
V_{CS}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 10mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC}	Power Supply Current		90	125	mA	V_{CC} = 5.25V, $V_{A0} \rightarrow V_{A7}$ = 0V, V_{CC} = 5.25V, $V_{S0} = V_{S1}$ = 0V
V_{IL}	Input "Low" Voltage			0.80	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.1			V	V_{CC} = 5.0V

NOTE 1: Typical values are at 25°C and at nominal voltage.

A. C. Characteristics V_{CC} = +5V ± 5%, T_A = -55°C to + 125°C

SYMBOL	PARAMETER	MAX. LIMIT	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	ns	Both C.S. lines must be at ground potential to activate the ROM.
t_{S++}, t_{S--}	Chip Select to Output Delay	30	ns	

Capacitance [1] T_A = 25°C

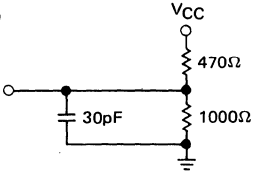
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V	V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

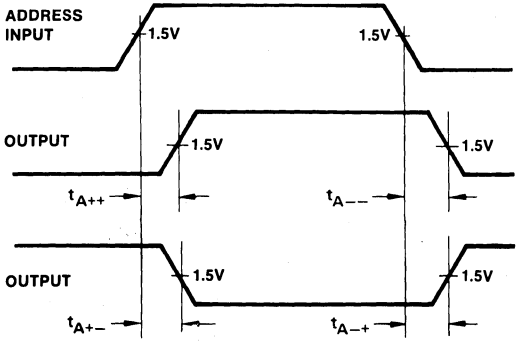
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test - 2.5 MHz

10 mA TEST LOAD

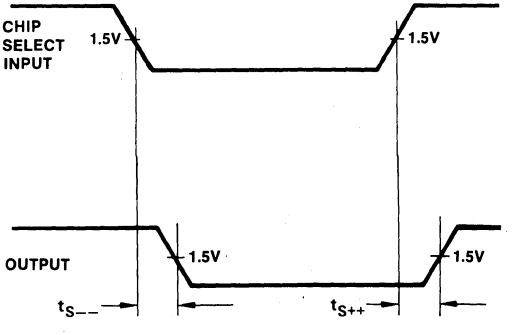


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3302A, 3302A-4, 3302AL6, 3322A, 3322A-4, 3322AL6

HIGH SPEED 2048 BIT READ ONLY MEMORY

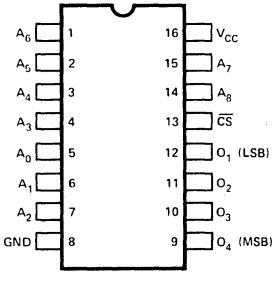
- **Fast Access Time—70ns (3302A, 3322A) Over Temperature and Supply Voltage Variation**
- **Low Standby Power Dissipation (3302AL6) — 115 μW/bit**
- **Fully Decoded—on Chip Address Decode and Buffer**
- **DTL and TTL Compatible—Input Loading is 0.25 mA max—Output Sink is 15 mA**
- **Open Collector (3302A, 3302A-4, 3302AL6) and Three State (3322A, 3322A-4, 3322AL6) Outputs**
- **Simple Memory Expansion—Single Chip Select Input Lead**
- **Standard Packaging—16 Pin Dual In-Line Lead Configuration**

The 3302A and 3322A device families are high density 2048 bit (512 words by 4-bit) ROMs. Electrical performance is specified over the complete ambient temperature range 0°C to 75°C and V_{CC} supply voltage range of 5V ±5%. The 3302A and 3322A ROM families are pin compatible with the Intel® 3602 and 3622 PROM families. Consequently initial circuit prototyping can be performed using the pin compatible PROMs.

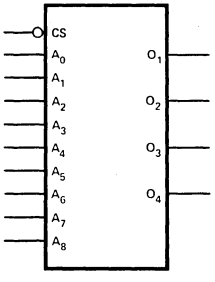
The 3302A-4 and 3322A-4 are ideal for slower performance systems (>90 ns) where low system cost is a prime factor. For those systems requiring low power dissipation, one should consider the 3302AL6/3322AL6. Not only does the 3302AL6/3322AL6 dissipate 20% less active power than the 3302/3322, but it also has an added low standby power dissipation feature. Whenever the 3302AL6/3322AL6 is deselected, power dissipation is reduced by 70%.

The 3302A and 3322A device families are manufactured using Schottky barrier diode clamped transistors which results in higher speed performance than equivalent devices made with gold diffusion process.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC1}	Power Supply Current (3302, 3302-4, 3322, 3322-4)			140	mA	V_{CC} = 5.25V, V_{A0} - V_{A8} = 0V, $\overline{CS}$ = 0V
I_{CC2}	Power Supply Current (3302L-6, 3322L-6) Active			110	mA	V_{CC} = 5.25V, $\overline{CS}$ = 0.45V
	Standby			45	mA	$\overline{CS}$ = 2.4V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3322A, 3322A-4, 3322AL6 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	µA	V_O = 5.25V or 0.45V, V_{CC} = 5.25V, $\overline{CS}$ = 2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC} = 5.00V, T_A = 25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMIT 3302A 3322A	MAX. LIMIT 3302A-4 3322A-4	MAX. LIMIT 3302AL6 3322AL6	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	70	90	90	ns	$\overline{CS}$ = V_{IL} to Select the ROM
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	120	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

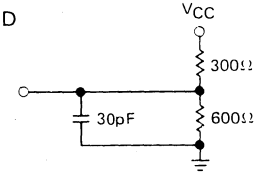
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

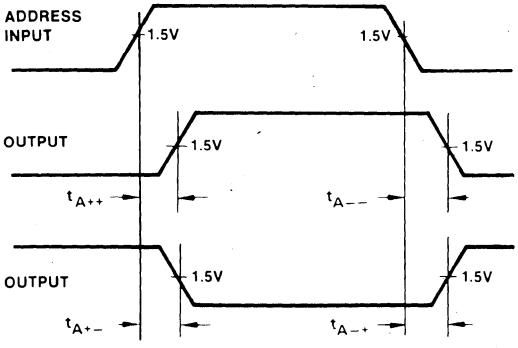
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

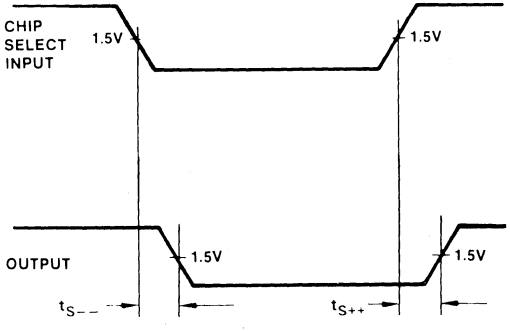


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3304A, 3304A-4, 3304AL6, 3324A, 3324A-4

HIGH SPEED 4096 BIT READ ONLY MEMORY

- **Fast Access Time—70ns (3304A, 3324A) Over Temperature and Supply Voltage Variation**
- **Low Standby Power Dissipation (3304AL6)—60 μW/bit**
- **Fully Decoded—on Chip Address Decode and Buffer**
- **DTL and TTL Compatible—Input Loading is 0.25 mA max—Output Sink is 15 mA**
- **Open Collector (3304A, 3304A-4, 3304AL6) and Three State (3324A, 3324A-4) Outputs**
- **Simple Memory Expansion—4 Chip Select Input Leads**
- **Standard Packaging—24 Pin Dual In-Line Lead Configuration**

The 3304A and 3324A device families are high density 4096 bit (512 words by 8-bit) ROMs. Electrical performance is specified over the complete ambient temperature range of 0°C to 75°C and V_{CC} supply voltage range of 5V ±5%. The 3304A and 3324A ROM families are pin compatible with the Intel 3604 and 3624 PROM families. Consequently initial circuit prototyping can be performed using the pin compatible PROMs.

The 3304A-4 and 3324A-4 are ideal for slower performance systems (> 90 ns) where low system cost is a prime factor. For those systems requiring low power dissipation, one should consider the 3304AL6. Not only does the 3304AL6 dissipate 20% less active power than the 3304A, but is also has an added low standby power dissipation feature. Whenever the 3304AL6 is deselected, power dissipation is reduced by 70%.

The 3304A and 3324A device families are manufactured using Schottky barrier diode clamped transistors which results in higher speed performance than equivalent devices made with gold diffusion process.

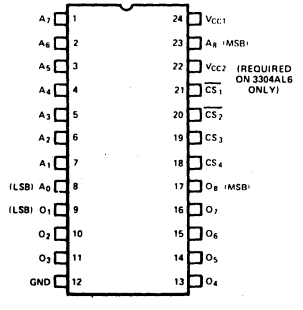
Mode/Pin Connection		Pin 22	Pin 24
Read:	3304A, 3304A-4, 3324A, 3324A-4	No Connect or 5V	5V
	3304AL6	+5V	No Connect
Standby Power:	3304AL6	Power dissipation is automatically reduced whenever the 3304AL6 is deselected.	

PIN NAMES

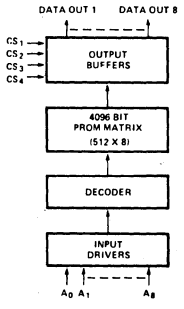
A_0–A_8	ADDRESS INPUTS
$\overline{CS_1}$–$\overline{CS_2}$, CS_3–CS_4 [1]	CHIP SELECT INPUTS
O_1–O_8	DATA OUTPUTS

[1] To select the ROM $\overline{CS_1} = \overline{CS_2} = 0$ and $CS_3 = CS_4 = 1$.

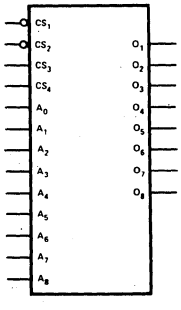
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC}=5.25V, V_A=5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC}=5.25V, V_S=5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_A= -10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_S= -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.75V, I_{OL}= 15mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC}=5.25V, V_{CE}=5.25V
I_{CC1}	Power Supply Current (3304A, 3304A-4)			190	mA	V_{CC1}=5.25V, $V_{A0}\rightarrow V_{A8}$=0V, $\overline{CS}_1=\overline{CS}_2$=0V, $CS_3=CS_4$=5.25V
I_{CC2}	Power Supply Current (3324A, 3324A-4)			190	mA	V_{CC1}=5.25V, $V_{A0}\rightarrow V_{A8}$=0V, $\overline{CS}_1=\overline{CS}_2$=0V, $CS_3=CS_4$=5.25V
I_{CC}	Power Supply Current (3304AL6) Active			140	mA	V_{CC2}=5.25V, V_{CC1}=Open $\overline{CS}_1=\overline{CS}_2$=0.45V, $CS_3=CS_4$=2.4V
	Standby			45	mA	$\overline{CS}_1=\overline{CS}_2$=2.5V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}=5.0V

3324A, 3324A-4 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	µA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1=\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMIT 3304A 3324A	MAX. LIMIT 3304A-4 3324A-4	MAX. LIMIT 3304AL6	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	70	90	**90**	ns	$\overline{CS}$ = V_{IL} to Select the PROM
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	120	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

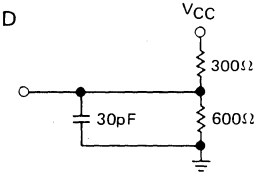
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	**15**	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

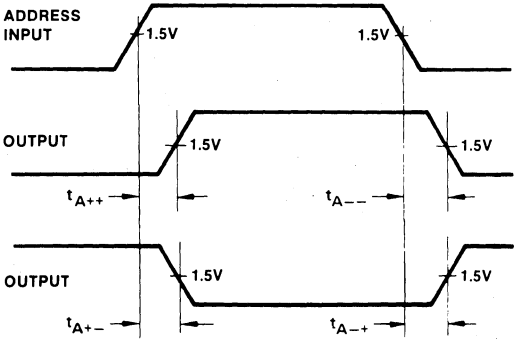
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

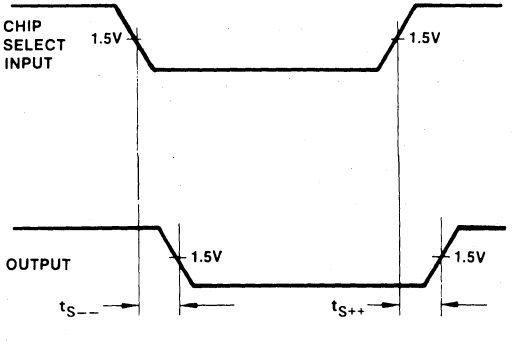


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3601, 3621

256 x 4 HIGH SPEED RAM

3601-1, 3621-1	50 ns Max.
3601, 3621	70 ns Max.

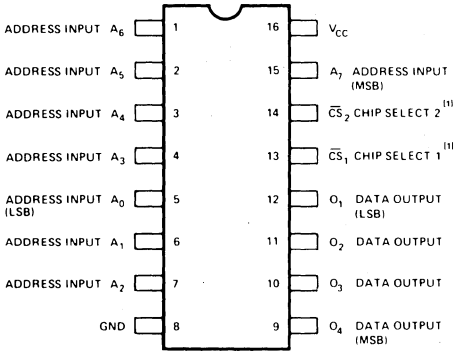
- **Low Power Dissipation: 0.5 mW/Bit Typical**
- **Open Collector (3601) and Three-State Outputs (3621)**
- **Fast Programming: 1 ms/Bit Typically**
- **Polycrystalline Silicon Fuse**
- **16 Pin Dual In-Line Hermetic Package**

The Intel® 3601/3621 is a 1024 bit PROM ideally suited for uses where fast turnaround and pattern experimentations are important, such as in prototypes or in small productions volume systems. The 3601 is manufactured with all outputs low, and logic high output levels can be electrically programmed in selected bit locations. The 3621 has its outputs initially high and logic low output levels are programmed. The same address inputs are used for both programming and reading.

A higher system performance is achieved by using the 3601-1 or 3621-1. These PROMs give a 25% system speed improvement over the 3601 or 3621.

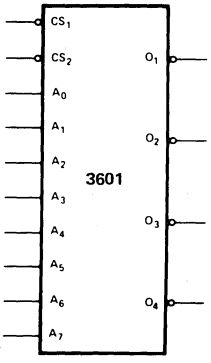
The 3601/3621 is manufactured with the highly reliable polycrystalline silicon fuse and the fast switching Schottky barrier diode technology.

PIN CONFIGURATION

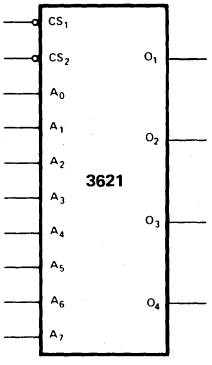


NOTE 1. DURING PROGRAMMING, THE PROGRAM PULSE MAY BE APPLIED TO EITHER $\overline{CS}_1$ OR $\overline{CS}_2$ FOR THE 3621 FAMILY. THE PROGRAM PULSE IS APPLIED TO $\overline{CS}_2$ FOR THE 3601 FAMILY.

LOGIC SYMBOL



LOGIC SYMBOL



PIN NAMES

A_0–A_7	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$	CHIP SELECT INPUTS
O_1–O_4	DATA OUTPUTS

Absolute Maximum Ratings*

Temperature Under Bias	−65°C to +125°C
Storage Temperature	−65°C to +160°C
Output or Supply Voltages	−0.5V to 7 Volts
All Input Voltages	-1.6V to 5.5V
Output Currents	100mA

Programming Only:

	3601	3621
Output or V_{CC} Voltages	10.25V	13V
$\overline{CS_2}$ Voltage	15.5V	15.5V
$\overline{CS_2}$ Current	100mA	150mA
V_{CC} Current	500mA	600mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C Unless Otherwise Specified.

Symbol	Parameter	Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CC}	Power Supply Current		90	130	mA	V_{CC}=5.25V, $V_{A0} \rightarrow V_{A7}$ = 0V $\overline{CS_1}$ = $\overline{CS_2}$ = 0V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

FOR 3621, 3621-1 ONLY

Symbol	Parameter	Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
I_O	Output Leakage for High Impedance Stage			40	μA	V_O =5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS_1}$=$\overline{CS_2}$=2.4V
I_{SC}[2]	Output Short Circuit Current			-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	MAXIMUM LIMITS			UNIT	CONDITIONS
		0°C	25°C	75°C		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	3601-1 and 3621-1 Address to Output Delay	50	50	50	ns	Both C.S. lines must be at ground potential to activate the PROM.
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	3601 and 3621 Address to Output Delay	70	60	70	ns	
t_{S++}, t_{S--}	Chip Select to Output Delay	25	25	25	ns	

ROMs

Capacitance [1] T_A = 25°C

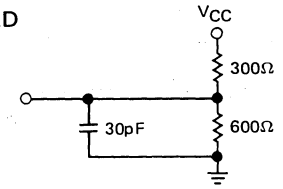
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V	V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

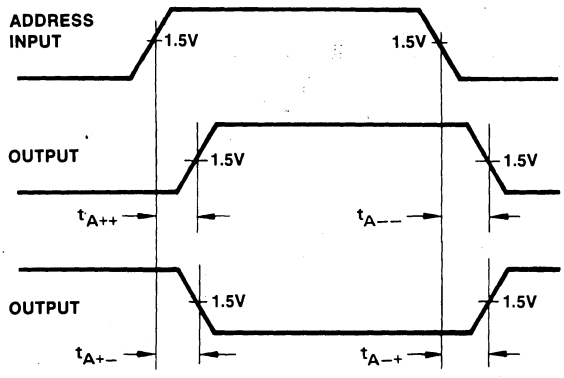
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

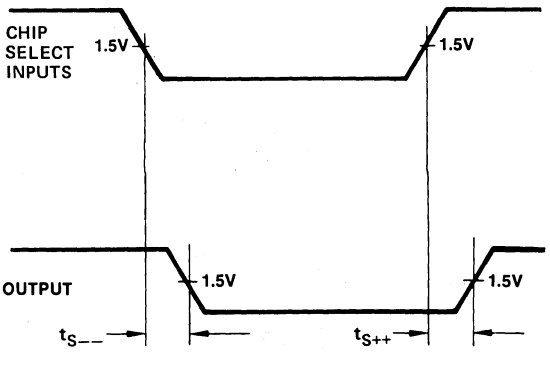


Waveforms

ADDRESS TO OUTPUT DELAY

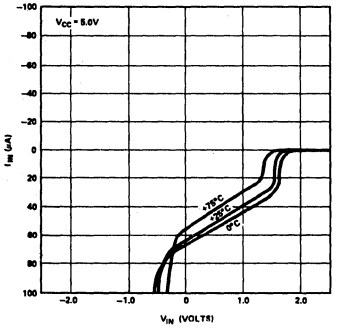


CHIP SELECT TO OUTPUT DELAY

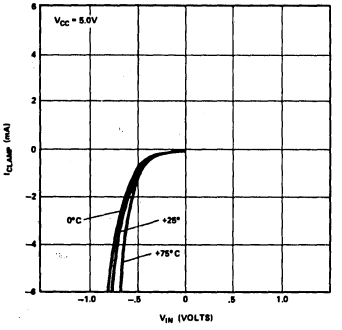


Typical D. C. Characteristics

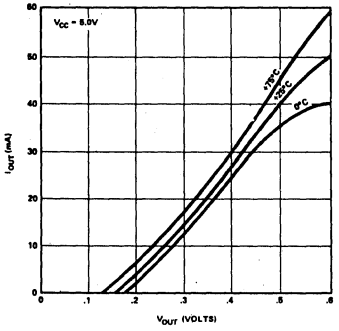
INPUT CURRENT
VS. INPUT VOLTAGE



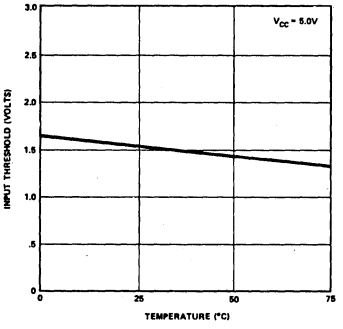
INPUT CLAMP CURRENT
VS. INPUT VOLTAGE



OUTPUT CURRENT
VS. OUTPUT "LOW" VOLTAGE

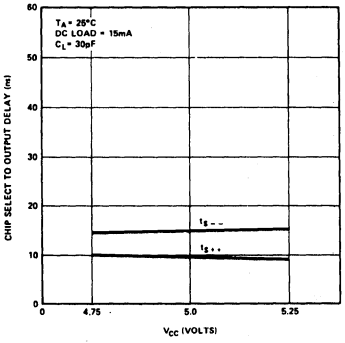


INPUT THRESHOLD
VS. TEMPERATURE

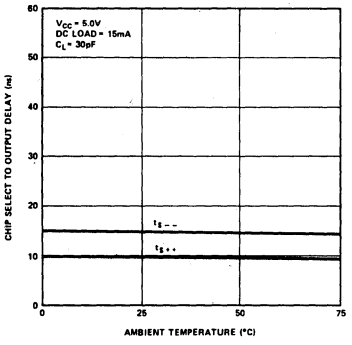


Typical A. C. Characteristics

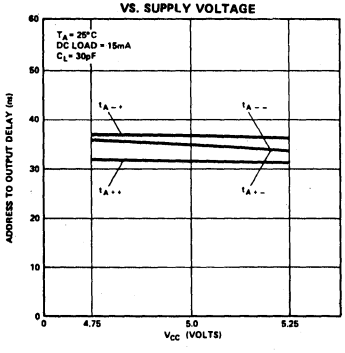
SELECT TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



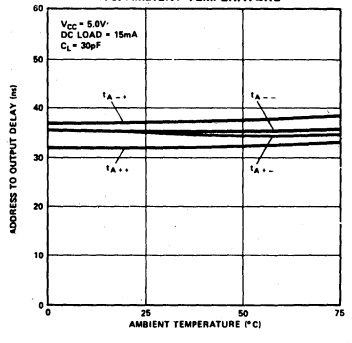
SELECT TO OUTPUT DELAY
VS. AMBIENT TEMPERATURE



ADDRESS TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



ADDRESS TO OUTPUT DELAY
VS. AMBIENT TEMPERATURE



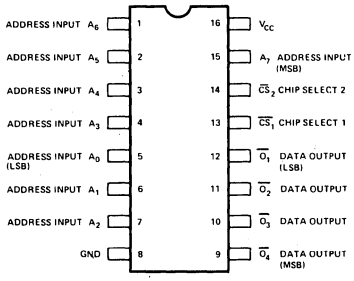
M3601

HIGH SPEED ELECTRICALLY PROGRAMMABLE 1024 BIT READ ONLY MEMORY

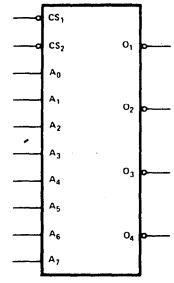
- **Military Temperature Range −55°C to +125°C**
- **Fast Access Time—90 nsec Maximum**
- **Fast Programming—1 ms/bit Typically**
- **Open Collector Outputs**
- **Standard Packaging — 16 Pin Hermetic Dual In-Line Lead Configuration**

The M3601 is a military temperature range PROM, organized as 256 words by 4-bits. The PROM is manufactured with all outputs low and logic output high levels can be electrically programmed in selected bit locations. The M3601 is pin compatible with the Intel metal mask ROM M3301A.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-65°C to +150°C
Storage Temperature	-65°C to +160°C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	-1.3 to 5.5V
Output Currents	100mA
Programming Only:	
Output or V_{CC} Voltages	10.25V
CS_2 Voltage	15.25V
V_{CC} Current	500mA
CS_2 Current	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

All limits apply for V_{CC} = +5.0V ±5%, T_A = -55°C to +125°C, unless otherwise specified.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.7	-1.2	V	V_{CC} = 4.75V, I_A = -5.0mA
V_{CS}	Chip Select Input Clamp Voltage		-0.7	-1.2	V	V_{CC} = 4.75V, I_S = -5.0mA
V_{CS}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 10mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC}	Power Supply Current		90	130	mA	V_{CC} = 5.25V, $V_{A0} \rightarrow V_{A7}$ = 0V, $V_{S0} = V_{S1}$ = 0V
V_{IL}	Input "Low" Voltage			0.80	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.1			V	V_{CC} = 5.0V

NOTE 1: Typical values are at 25°C and at nominal voltage.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = -55°C to +125°C

SYMBOL	PARAMETER	MAX. LIMIT	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	90	ns	Both C.S. lines must be at ground potential to activate the PROM.
t_{S++}, t_{S--}	Chip Select to Output Delay	35	ns	

Capacitance [1] T_A = 25°C

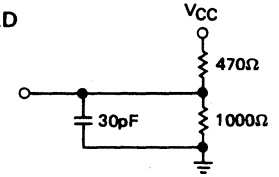
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V	V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

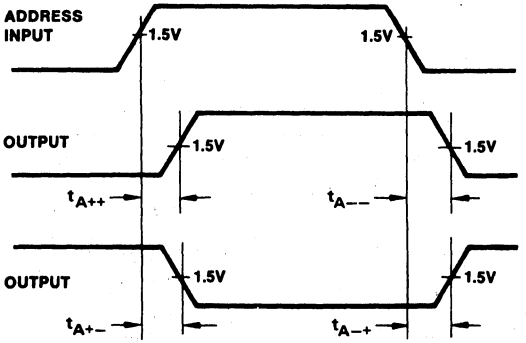
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test - 2.5 MHz

10 mA TEST LOAD

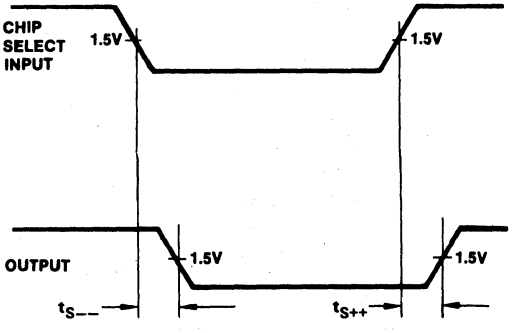


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3602, 3602-4, 3602L-6, 3622, 3622-4, 3622L-6

HIGH SPEED ELECTRICALLY PROGRAMMABLE 2048 BIT READ ONLY MEMORY

- **Fast Access Time — 70ns (3602, 3622)**
- **Low Standby Power Dissipation (3602L-6, 3622L-6) — 115 μW/bit**
- **Open Collector (3602, 3602-4, 3602L-6) or Three-State (3622, 3622-4, 3622L-6) Outputs**
- **Fast Programming — 1 ms/bit Typically**
- **Polycrystalline Silicon Fuse**
- **Standard Packaging — 16 Pin Dual In-Line Configuration**

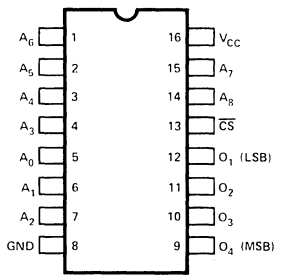
The 3602 and 3622 device families are high density 2048 bit (512 words by 4-bits) PROMs suitable for uses where fast turn-around and pattern experimentation are important such as in prototypes or in small production volume systems. For those systems requiring low power dissipation, one should consider the 3602L-6 or 3622L-6. Both the 3602L-6 and 3622L-6 have a low standby power dissipation feature. Whenever these two devices are deselected, power dissipation is reduced substantially over the active power dissipation. The 3602-4 and 3622-4 are ideal for slower performance systems (>90ns) where low system cost is a prime factor.

The PROMs are pin compatible with the Intel metal mask ROMs 3302A, 3302A-4, 3302AL6, 3322A, 3322A-4 and 3322AL6. The ROMs offer system cost savings over the PROMs when in large volume production.

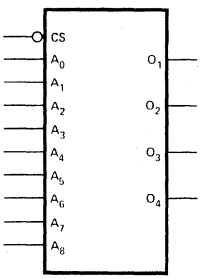
The PROMs are manufactured with all outputs high and logic low levels can be electrically programmed in selected bit locations.

The 3602 and 3622 device families are monolithic, high speed, Schottky clamped TTL arrays with polycrystalline silicon fuses. The Schottky barrier diode clamped transistors allow faster switching speeds than those devices made with the conventional gold diffusion processes.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6V to 5.6V
Output Currents 100mA
Programming Only:
Output or V_{CC} Voltages 13V
$\overline{CS}$ Voltage 15.5V
V_{CC} Current 600mA
$\overline{CS}$ Current 150mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC1}	Power Supply Current (3602, 3602-4, 3622, 3622-4)			140	mA	V_{CC}=5.25V, V_{A0}→V_{A8}=0V $\overline{CS}$ = 0V
I_{CC2}	Power Supply Current (3602L-6, 3622L-6) Active			110	mA	V_{CC}=5.25V $\overline{CS}$ = 0.45V
	Standby			45	mA	$\overline{CS}$ = 2.4V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3622, 3622-4, 3622L-6 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	µA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC}=4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMIT 3602 3622	MAX. LIMIT 3602-4 3622-4	MAX. LIMIT 3602L-6 3622L-6	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	70	90	90	ns	$\overline{CS}$ = V_{IL} to Select the PROM
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	120	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

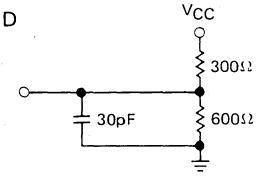
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

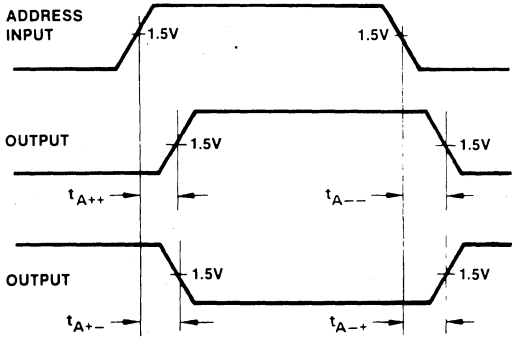
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

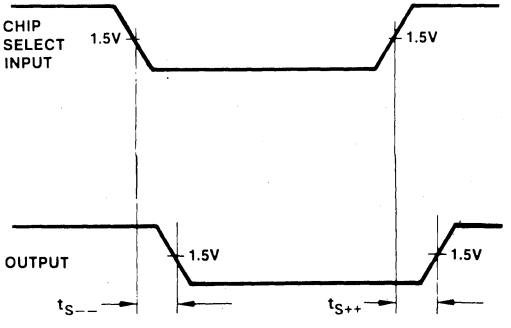


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



HIGH SPEED ELECTRICALLY PROGRAMMABLE 4096 BIT READ ONLY MEMORY

- **Fast Access Time — 70 ns (3604, 3624)**
- **Low Standby Power Dissipation (3604L-6) — 60 μW/bit**
- **Open Collector (3604, 3604-4, 3604L-6) or Three-State (3624, 3624-4) Outputs**
- **Fast Programming — 1 ms/bit Typically**
- **Polycrystalline Silicon Fuse**
- **Standard Packaging — 24 Pin Dual In-Line Configuration**

The 3604 and 3624 device families are high density 4096 bit (512 words by 8-bits) PROMs suitable for uses where fast turn-around and pattern experimentation are important such as in prototypes or in small production volume systems. For those systems requiring low power dissipation, one should consider the 3604L-6. The 3604L-6 has a low standby power dissipation feature. Whenever the 3604L-6 is deselected, power dissipation is reduced substantially over the active power dissipation. The 3604-4 and 3624-4 are ideal for slower performance systems (>90ns) where low system cost is a prime factor.

The PROMs are pin compatible with the respective Intel metal mask ROMs 3304A, 3304A-4, 3304AL6, 3324, and 3324-4. The ROMs offer system cost savings over the PROMs when in large volume production.

The PROMs are manufactured with all outputs high. Logic low levels can be electrically programmed in selected bit locations.

The 3604 and 3624 device families are monolithic, high speed, Schottky clamped TTL arrays with polycrystalline silicon fuses. The Schottky barrier diode clamped transistors allow faster switching speeds than those devices made with the conventional gold diffusion processes.

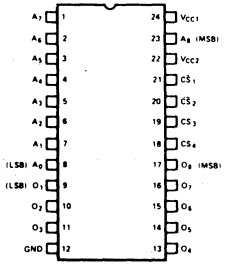
Mode/Pin Connection		Pin 22	Pin 24
Read:	3604, 3604-4, 3624, 3624-4	No Connect or 5V	5V
	3604L-6	+5V	No Connect
Program:	3604, 3604-4, 3624, 3624-4	Pulsed 12.5V	Pulsed 12.5V
	3604L-6	Pulsed 12.5V	Pulsed 12.5V
Standby Power:	3604L-6	Power dissipation is automatically reduced whenever the 3604L-6 is deselected.	

PIN NAMES

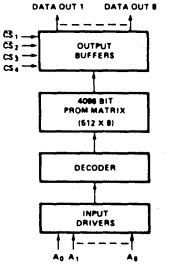
A_0–A_8	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$, CS_3–CS_4 [1]	CHIP SELECT INPUTS
O_1–O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = 0$ and $CS_3 = CS_4 = 1$.

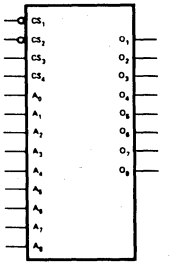
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6 to 5.5V
Output Currents 100mA
Programming Only:
Output or V_{CC} Voltages 13V
$\overline{CS}_1$ Voltage 15.5V
V_{CC} Current 600mA
$\overline{CS}_1$ Current 150mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC}=5.25V, V_A=5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC}=5.25V, V_S=5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_A=-10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_S= -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.75V, I_{OL}=15mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC}=5.25V, V_{CE}=5.25V
I_{CC1}	Power Supply Current (3604, 3604-4)			190	mA	V_{CC1}=5.25V, $V_{A0}\rightarrow V_{A8}$=0V, $\overline{CS}_1=\overline{CS}_2$=0V, $CS_3=CS_4$=5.25V
I_{CC2}	Power Supply Current (3624, 3624-4)			190	mA	V_{CC1}=5.25V, $V_{A0}\rightarrow V_{A8}$=0V, $\overline{CS}_1=\overline{CS}_2$=0V, $CS_3=CS_4$=5.25V
I_{CC}	Power Supply Current (3604L-6) Active			140	mA	V_{CC2}=5.25V, V_{CC1}=Open $\overline{CS}_1=\overline{CS}_2$=0.45V, $CS_3=CS_4$=2.4V
	Standby			45	mA	$\overline{CS}_1=\overline{CS}_2$=2.5V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}=5.0V

3624, 3624-4 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	µA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1=\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC}=4.75V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMIT 3604 3624	MAX. LIMIT 3604-4 3624-4	MAX. LIMIT 3604L-6	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	70	90	90	ns	$\overline{CS_1} = \overline{CS_2} = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to Select the PROM.
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	120	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

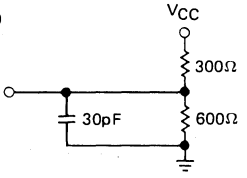
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

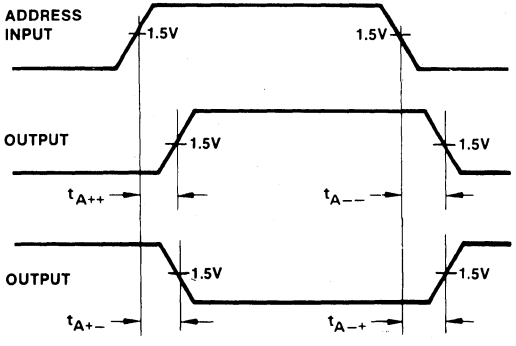
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

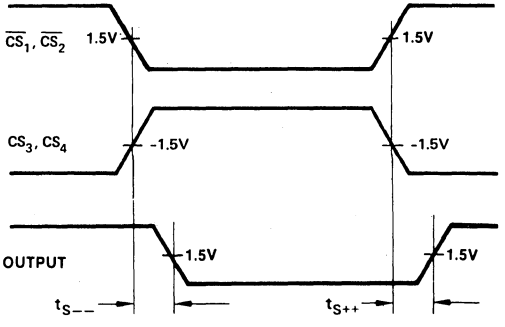


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



HIGH SPEED ELECTRICALLY PROGRAMMABLE 4096 BIT READ ONLY MEMORY

- **Military Temperature Range**
- **Fast Access Time—90 ns (M3604, M3624)**
- **Low Standby Power Dissipation (M3604-6)—60 μW/bit**
- **Open Collector (M3604, M3604-6) or Three-State (M3624) Outputs**
- **Fast Programming—1 ms/bit Typically**
- **Polycrystalline Silicon Fuse**
- **Standard Packaging — 24 Pin Hermetic Dual-In-Line Lead Configuration**

The M3604, M3604-6, and M3624 are high density 4096 bit (512 words by 8-bits) PROMs suitable for uses where fast turnaround and pattern experimentation are important such as in prototypes or in small production volume systems. The M3604/M3624 are specified over the full temperature range of -55°C to +125°C and the M3604-6 over the extended temperature range of -30°C to +125°C. For those systems requiring low power dissipation, one should consider the M3604-6. The M3604-6 has a low standby power dissipation feature. Whenever the M3604-6 is deselected, power dissipation is reduced substantially over the active power dissipation.

The PROMs are manufactured with all outputs high. Logic low levels can be electrically programmed in selected bit locations. The M3604 and M3624 device families are monolithic, high speed, Schottky clamped TTL arrays with polycrystalline silicon fuses.

Mode/Pin Connection		Pin 22	Pin 24
Read:	M3604, M3624	No Connect or 5V	5V
	M3604-6	+5V	No Connect
Program:	M3604, M3624	Pulsed 12.5V	Pulsed 12.5V
	M3604-6	Pulsed 12.5V	Pulsed 12.5V
Standby Power:	M3604-6	Power dissipation is automatically reduced whenever the M3604-6 is deselected.	

ORDERING INFORMATION:

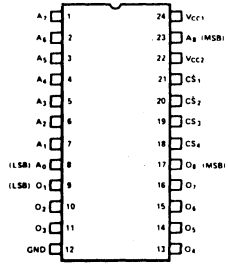
MD3604: Open Collector – 4K
MD3604-6: Open Collector – Low Standby Power 4K
MD3624: Three State – 4K

PIN NAMES

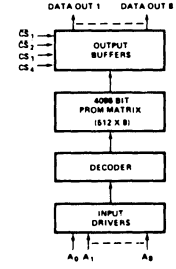
A_0–A_8	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$, CS_3–CS_4	CHIP SELECT INPUTS [1]
O_1–O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = 0$ and $CS_3 = CS_4 = 1$.

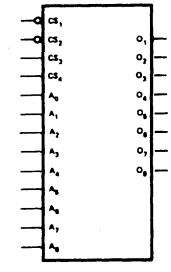
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +135 C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6V to 5.6V
Output Currents 100mA
Programming Only:
Output or V_{CC} Voltages 13V
$\overline{CS}_1$ Voltage 15.5V
V_{CC} Current 600mA
$\overline{CS}_1$ Current 150mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

V_{CC} = +5.0V ±10%, T_A = −55°C to +125°C for M3604, M3624
V_{CC} = +5.0V ± 5%, T_A = −30°C to +125°C for M3604-6

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}= Max, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}= Max, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}= Max, V_A= Max
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}= Max, V_S= Max
V_{CA}	Address Input Clamp Voltage		-0.9	−1.5	V	V_{CC}= Min, I_A= −10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	−1.5	V	V_{CC}= Min, I_S= −10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}= Min, I_{OL}= 10mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC}= Max, V_{CE}= Max
I_{CC1}	Power Supply Current (M3604)			190	mA	V_{CC1}= Max, V_{A0}→V_{A8}=0V, $\overline{CS}_1$=$\overline{CS}_2$=0V, CS_3=CS_4= 5.5V
I_{CC2}	Power Supply Current (M3624)			190	mA	V_{CC1}= Max, V_{A0}→V_{A8}=0V, $\overline{CS}_1$=$\overline{CS}_2$=0V, CS_3=CS_4= 5.5V
I_{CC}	Power Supply Current (M3604-6) Active			140	mA	V_{CC2}= Max, V_{CC1}=Open $\overline{CS}_1$=$\overline{CS}_2$=0.45V, CS_3=CS_4=2.4V
	Standby			45	mA	$\overline{CS}_1$=$\overline{CS}_2$=2.5V
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC}= 5.0V, T_A=25°C
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}= 5.0V, T_A=25°C

M3624 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	μA	V_O= Max or 0.45V, V_{CC}= Max, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 5V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics

V_{CC} = +5.0V ±10%, T_A = −55°C to +125°C for M3604, M3624
V_{CC} = +5.0V ± 5%, T_A = −30°C to +125°C for M3604-6

SYMBOL	PARAMETER	MAX. LIMIT		UNIT	CONDITIONS
		M3604 M3624	M3604-6		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	90	120	ns	$\overline{CS_1}$ = $\overline{CS_2}$ = V_{IL} and CS_3 = CS_4 = V_{IH} to Select the PROM
t_{S++}	Chip Select to Output Delay	45	45	ns	
t_{S--}	Chip Select to Output Delay	45	160	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

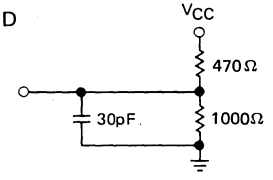
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

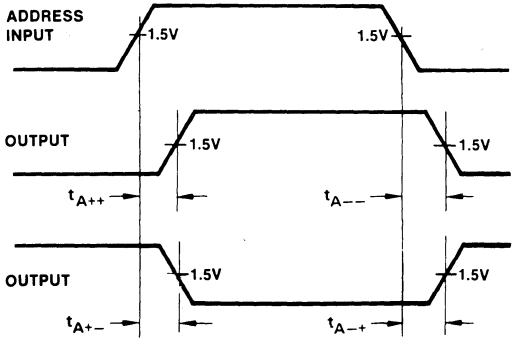
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test - 2.5 MHz

10 mA TEST LOAD

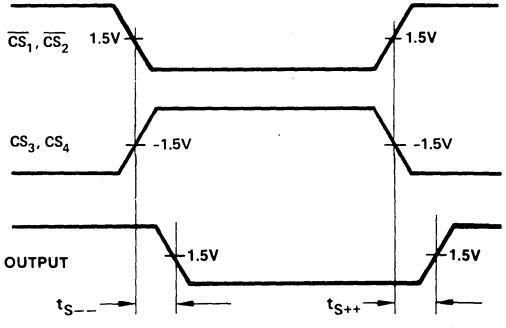


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



ROMs

3605, 3625

NEW PRODUCT

HIGH SPEED 1K x 4 PROM

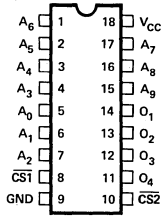
3605-1, 3625-1	50 ns Max.
3605, 3625	70 ns Max.

- **Fast Access Time: 35ns Typically**
- **Low Power Dissipation: 0.14 mW/bit Typically**
- **Fast Programming: 1 ms/bit Typically**
- **Open Collector (3605) and Three-State (3625) Outputs**
- **Hermetic 18 Pin DIP**

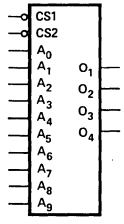
The 3605/3625 is a high density 4096 bit PROM suitable for uses where fast turnaround and pattern experimentation are important such as in prototypes or in small production volume systems. The PROMs are manufactured with all outputs high and logic low levels can be electrically programmed in selected bit locations.

The 3605/3625 is a monolithic, high speed, Schottky clamped TTL memory array with polycrystalline silicon fuses. The Schottky barrier diode clamped transistors allow faster switching speeds than those devices made with the conventional gold diffusion processes.

PIN CONFIGURATION



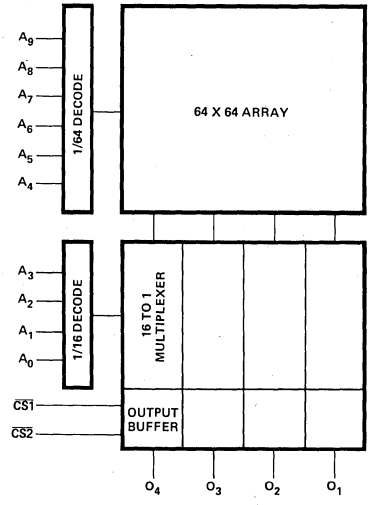
LOGIC SYMBOL



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
$O_1 - O_4$	OUTPUTS

BLOCK DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA
Programming Only:
  Output or V_{CC} Voltages 13V
  $\overline{CS}_1$ Voltage 15.5V
  V_{CC} Current 600mA
  $\overline{CS}_1$ Current 150mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC}= +5.0V ±5%, T_A= 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC}=5.25V, V_A=5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC}=5.25V, V_S=5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_A=-10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_S=-10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.75V, I_{OL}=15mA
I_{CEX}	3605 Output Leakage Current			100	µA	V_{CC}=5.25V, V_{CE}=5.25V
I_{CC}	Power Supply Current		110	150	mA	V_{CC1}=5.25V, $V_{A0}\rightarrow V_{A9}$=0V, $\overline{CS}_1=\overline{CS}_2$=0V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}=5.0V

3625, 3625-1 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	µA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1=\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Max. Limits 3605-1 3625-1	Max. Limits 3605 3625	Unit	Conditions
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	50	70	ns	$\overline{CS}_1=\overline{CS}_2=V_{IL}$ to select the PROM.
t_{S++}	Chip Select to Output Delay	25	30	ns	
t_{S--}	Chip Select to Output Delay	25	30	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

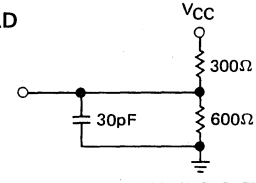
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

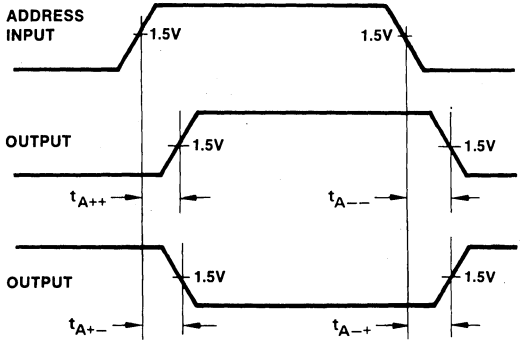
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15mA TEST LOAD

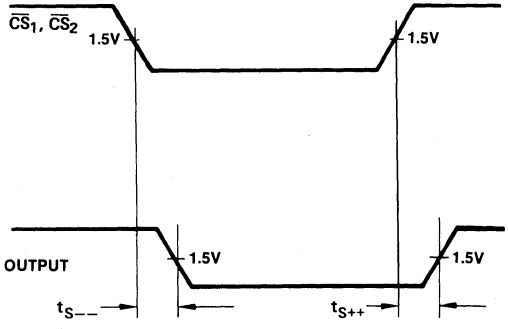


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



I. ROM and PROM Truth Table Format

Programming information should be sent in the form of computer punched cards or punched paper tape. When using the 7600C or MCS programmers, punched paper tape should be used. In all cases, a printout of the truth table should be accompanied with the order.

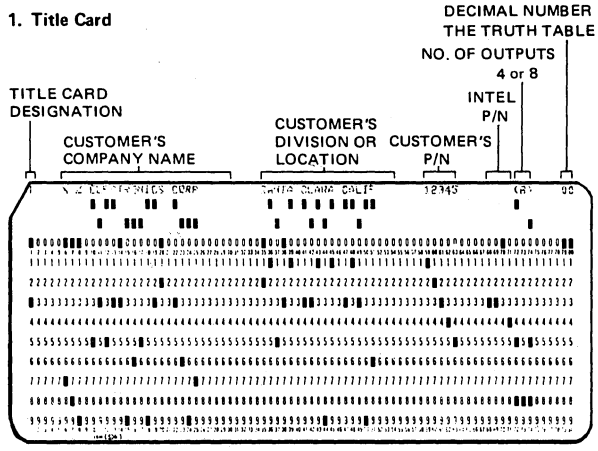
The following general format is applicable to the programming information sent to Intel:

1. A data field should start with the most significant bit and end with the least significant bit.
2. The data field should consist of P's and N's. A P is to indicate a high level output (most positive) and an N a low level output (most negative). If the programming information is sent on a punched paper tape, then a start character, B, and an end character, F, must be used in the data field.

A. PUNCHED CARD FORMAT

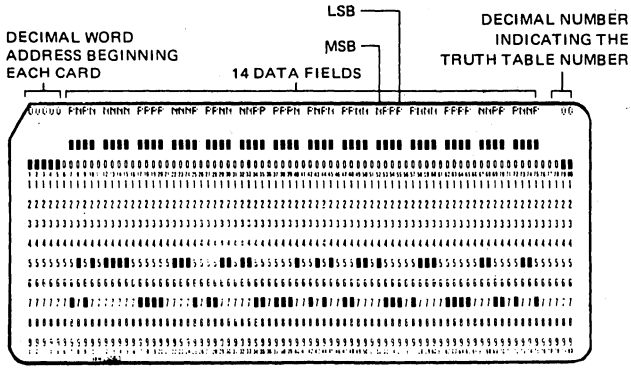
An 80 column Hollerith card (preferably interpreted) punched by an IBM 026 or 029 keypunch should be submitted. The first card will be a title card. The format is as follows:

1. Title Card



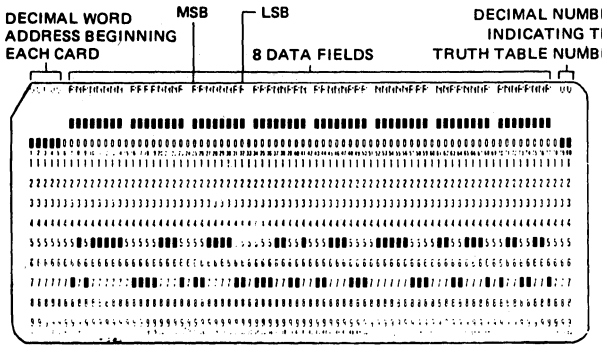
Column	Data
1	Punch a T
2-5	Blank
6-30	Customer Company Name
31-34	Blank
35-54	Customer's Company Division or location
55-58	Blank
59-63	Customer Part Number
64-67	Blank
68-74	Punch the Intel 4 digit basic part number and in () the number of output bits, e.g. 1702 (8), 3304 (8), 3301 (4), or 3601 (4).
75-78	Blank
79-80	Punch a 2 digit decimal number to identify the truth table number. The first truth table will be ØØ, second Ø1, third Ø3, etc.

2. For a N words x 4 bit organization only, cards 2 and the following cards should be punched as shown: Each card specifies the 4 bit output of 14 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØ14, ØØØ28, etc.
6	Blank
7-10	Data Field
11	Blank
12-15	Data Field
16	Blank
17-20	Data Field
21	Blank
22-25	Data Field
26	Blank
27-30	Data Field
31	Blank
32-35	Data Field
36	Blank
37-40	Data Field
41	Blank
42-45	Data Field
46	Blank
47-50	Data Field
51	Blank
52-55	Data Field
56	Blank
57-60	Data Field
61	Blank
62-65	Data Field
66	Blank
67-70	Data Field
71	Blank
72-75	Data Field
76-78	Blank
79-80	Punch same 2 digit decimal number as in title card.

3. For a N words x 8-bit organization only, cards 2 and the following cards should be punched as shown. Each card specifies the 8-bit output of 8 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØØ8, ØØØ16, etc.
6	Blank
7-14	Data Field
15	Blank
16-23	Data Field
24	Blank
25-32	Data Field
33	Blank
34-41	Data Field
42	Blank
43-50	Data Field
51	Blank
52-59	Data Field
60	Blank
61-68	Data Field
69	Blank
70-77	Data Field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

B. PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces.

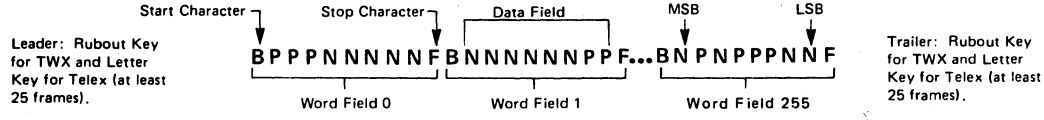
BPNF Format

The format requirements are as follows:

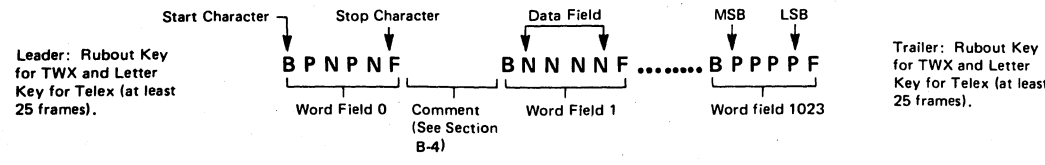
1. All word fields are to be punched in consecutive order, starting with word field Ø (all addresses low). There must be exactly N word fields for the N x 8 or N x 4 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for the N x 8 or N x 4 organization respectively.

   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

Example of BPNF 256 x 8 format (N = 256):



Example of 512 x 4 format (N = 512):



II. MOS PROM ERASING PROCEDURE

The 1702A, 1702AL, 2704, and 2708 is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 2537A. The recommended integrated dose (i.e., VV intensity x exposure time) is 6W-sec/cm^2 for the 1702A/1702AL and 10W-sec/cm^2 for the 2704/2708. An example of an ultraviolet source which can erase the 1702A/1702AL in 10 to 20 minutes or the 2704/2708 in 20 to 30 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the PROM should be placed about one inch away from the lamp tubes.

Two manufacturers of the S52 are Ultra-Violet Products, Inc. (San Gabriel, Calif.) and Product Specialties, Inc. (Issaquah, Washington).

III. MOS PROM PROGRAMMING INSTRUCTIONS

A. 1702A and 1702AL Family

Initially, all 2048 bits of the PROM are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode. All 8 address bits must be in the binary complement state when pulsed V_{CC} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25μsec after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10μsec before the program pulse is applied. The addresses should be programmed in the sequence 0 through 255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (-48V) will program a "1" and a high data input level (ground) will leave a "0". All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals. See page 2 of the data sheet for required pin connections during programming.

1702A, 1702AL

D.C. and Operating Characteristics for Programming Operation

T_A = 25°C, V_{CC} = 0V, V_{BB} = + 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI1P}	Address and Data Input Load Current			10	mA	V_{IN} = -48V
I_{LI2P}	Program and V_{GG} Load Current			10	mA	V_{IN} = -48V
I_{BB}[1]	V_{BB} Supply Load Current		10		mA	
I_{DDP}[2]	Peak I_{DD} Supply Load Current		200		mA	V_{DD} = V_{PROG} = -48V, V_{GG} = -35V
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	-46		-48	V	
V_{IL2P}	Address Input Low Voltage	-40		-48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	-46		-48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	-35		-40	V	

Notes: 1. The V_{BB} supply must be limited to 100mA max. current to prevent damage to the device.
2. I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μsec. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.

1702A, 1702AL
A.C. Characteristics for Programming Operation

$T_{AMBIENT}$ = 25°C, V_{CC} = 0V, V_{BB} = + 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

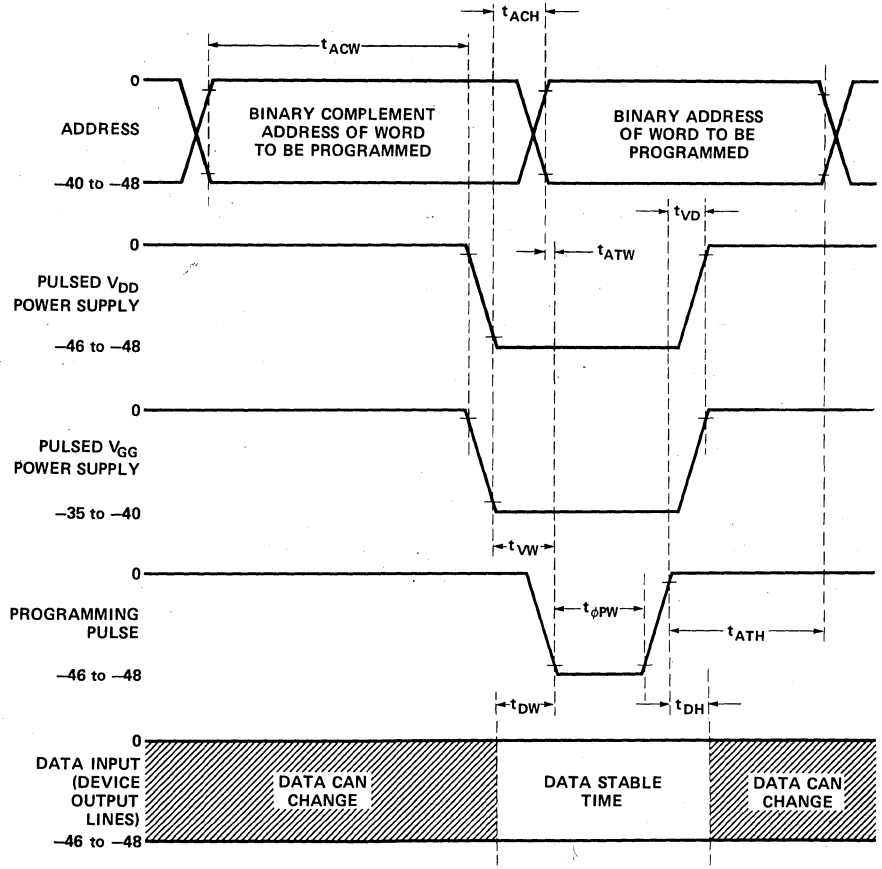
Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
	Duty Cycle (V_{DD}, V_{GG})			20	%	
$t_{\phi PW}$	Program Pulse Width		2	3	ms	V_{GG} = -35V, V_{DD} = V_{PROG} = -48V
t_{DW}	Data Set-Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD}, V_{GG} Set-Up	100			μs	
t_{VD}	V_{DD}, V_{GG} Hold	10		100	μs	
t_{ACW}	Address Complement Set-Up	25			μs	
t_{ACH}	Address Complement Hold	25			μs	
t_{ATW}	Address True Set-Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

PROGRAM WAVEFORMS

Conditions of Test:

Input pulse rise and fall times ≤ 1μsec

$\overline{CS}$ = 0V



B. 2708/2704 Family

Initially, and after each erasure, all bits of the 2708/2704 are in the "1" state (Output High). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the $\overline{CS}$/WE input (Pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8-bits in parallel, to the data output lines (O_1-O_8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up one program pulse per address is applied to the program input (Pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to $N \times t_{PW} \geqslant 100$ ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops through all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Examples (Using $N \times t_{PW} \geqslant 100$ ms)

Example 1: All 8096 bits are to be programmed with a 0.5 ms program pulse width.

The minimum number of program loops is 200. One program loop consists of words 0 to 1023.

Example 2: Words 0 to 100 and 500 to 600 are to be programmed. All other bits are "don't care". The program pulse width is 0.75 ms.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's.

Example 3: Same requirements as example 2 but the PROM is now to be *updated* to include data for words 750 to 770.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's. Addresses 0 to 100 and 500 to 600 must be re-programmed with their original data pattern.

2704, 2708
PROGRAM CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

D.C. Programming Characteristics

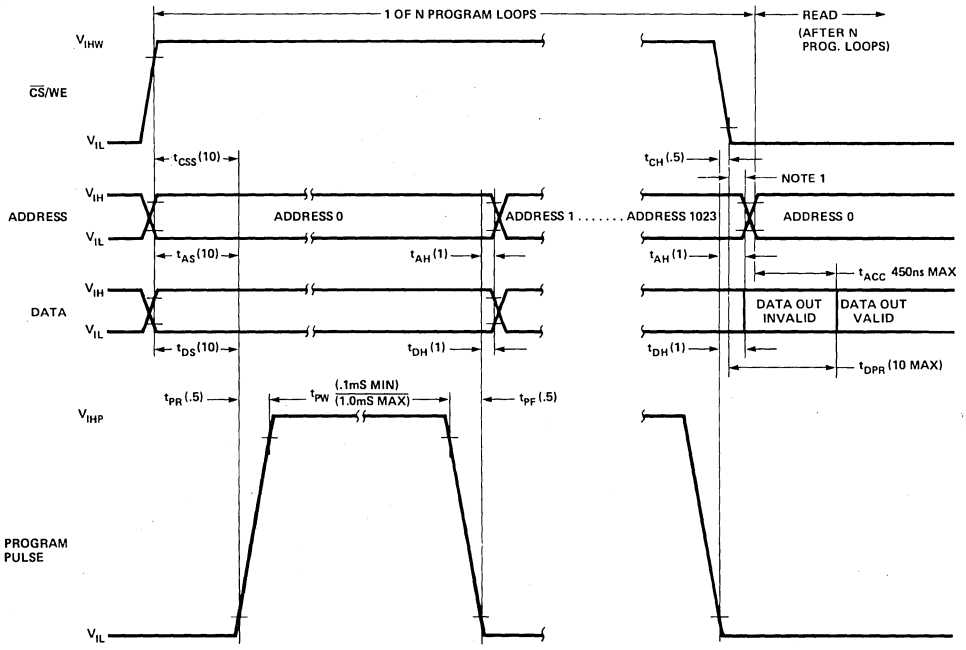
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current			10	μA	V_{IN} = 5.25V
I_{IPL}	Program Pulse Source Current			3	mA	
I_{IPH}	Program Pulse Sink Current			20	mA	
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Level (except Program)	V_{SS}		0.65	V	
V_{IH}	Input High Level for all Addresses and Data	3.0		V_{CC}+1	V	
V_{IHW}	$\overline{CS}$/WE Input High Level	11.4		12.6	V	Referenced to V_{SS}
V_{IHP}	Program Pulse High Level	25		27	V	Referenced to V_{SS}
V_{ILP}	Program Pulse Low Level	V_{SS}		1	V	V_{IHP} - V_{ILP} = 25V min.

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

2704, 2708
Programming Waveforms



NOTE 1. THE $\overline{CS}/WE$ TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION.

NOTE 2. NUMBERS IN ( ) INDICATE MINIMUM TIMING IN μS UNLESS OTHERWISE SPECIFIED.

IV. BIPOLAR PROM PROGRAMMING INSTRUCTIONS

A. Programming the 3601 (or 3601-1)

The 3601 may be programmed using the basic circuit of Figure 1. Address inputs are at standard TTL levels. Only one output may be programmed at a time. The output to be programmed must be connected to V_{CC} through a 300Ω resistor. This will force the proper programming current (3-6mA) into the output when the V_{CC} supply is later raised to 10V. All other outputs must be held at a TTL low level (0.4V).

The programming pulse generator produces a series of pulses to the 3601 V_{CC} and CS_2 leads. V_{CC} is pulsed from a low of 4.5 ± .25V to a high of 10 ± .25V, while CS_2 is pulsed from a low of ground (TTL logic 0) to a high of 15 ± 0.5V. It is important to accuractly maintain these voltage levels, otherwise, improper programming may result. The pulses applied must maintain a duty cycle of 50 ± 10% and start with an initial width of 1 (± 10%) μs, and increase linearly over a period of approximately 100ms to a maximum width of 8 (± 10%) μs. Typical devices have their fuse blown within 1ms, but occasionally a fuse may take up to 400ms. During the application of the program pulse, current to CS_2 must be limited to 100mA. The output of the 3601 is sensed when $\overline{CS_2}$ is at a TTL low level output. A programmed bit will have a TTL high output. After a fuse is blown, the V_{CC} and $\overline{CS_2}$ pulse trains must be applied for another 500μs. The characteristics of the pulse train are shown in Figure 2.

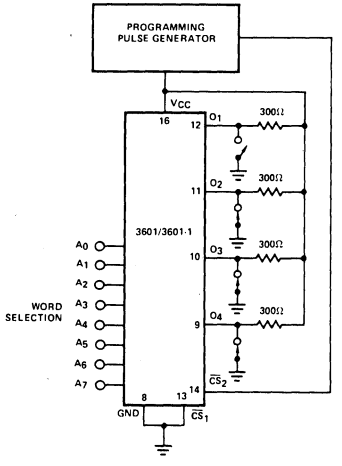


Figure 1. 3601 Programming.

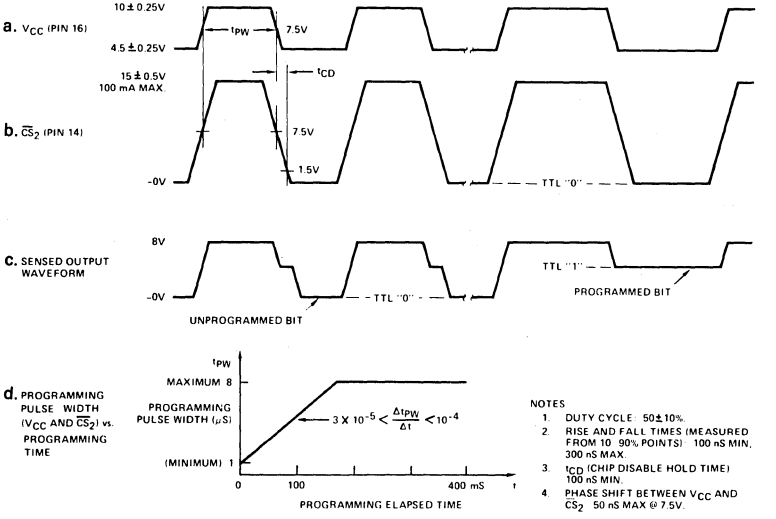
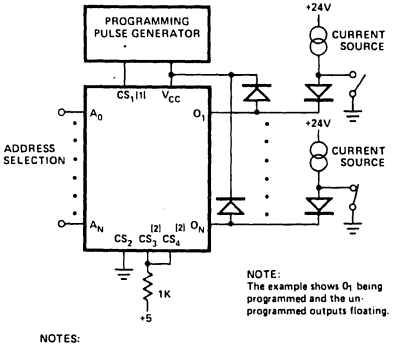


Figure 2. Pulses During Programming.

B. Programming the 3621, 2K, and 4K Bipolar PROM Families

The Intel® 3621, 2K and 4K bipolar PROMs families are programmed using the basic circuit of Figure 1. Initially all bits are in a logic 1 (high) state. Only one output may be programmed at a time. The programming current (5mA ± 10%) is forced into the output to be programmed by a current source. The current should be clamped to V_{CC} by a silicon diode. All other outputs must be allowed to float such that the outputs are allowed to rise one diode above V_{CC} (12.5V).

For simplicity of the programming description, reference will be made only to V_{CC}, however, this term includes both the V_{CC1} and V_{CC2} of the 4K PROM. There is only one V_{CC} for the 3621 and 2K PROMs. Programming pulses must be applied to both V_{CC} and $\overline{CS}$. A series of pulses is applied to the V_{CC} and $\overline{CS_1}$ (or $\overline{CS_2}$ for the 3621) leads as shown in Figure 2a and 2b respectively. The pulse applied must maintain a duty cycle of 50 ± 10% and start with an initial width of 1 (±10%) μs, and increase linearly over a period of approximately 100ms to a maximum of 8 (±10%) μs. Typical devices have their fuse blown within 1ms, but occasionally a fuse may take up to 400ms. During the application of the program pulse, the V_{CC} current must be limited to 600mA and the $\overline{CS_1}$ current to 150mA. A programmed bit will have a TTL low level. After a fuse is blown, the V_{CC} and $\overline{CS_1}$ pulse trains must be applied (the pulse width still linearly increasing to a maximum of 8μs) for another 500μs.



NOTES:
1. FOR THE 3621 FAMILY ONLY, THE PROGRAM PULSE MAY BE APPLIED TO EITHER CS_1 OR CS_2.
2. CS_3, CS_4 ARE ONLY FOR THE 4K PROM.

Figure 1. 3621, 2K, and 4K Bipolar PROM Family Programmer.

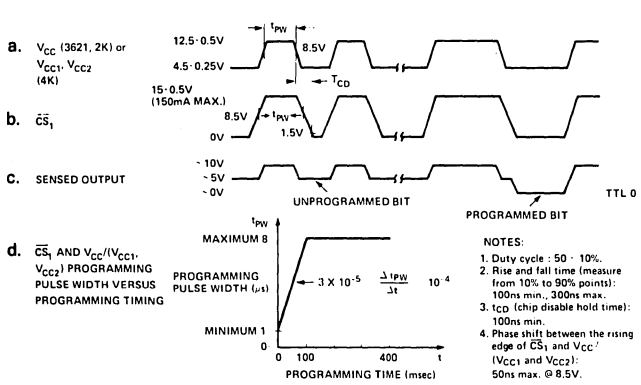


Figure 2. Pulses During Programming.

IV. UNIVERSAL PROM PROGRAMMER

Available from Intel MCS Department.

- **PROM Programming peripheral capable of programming the following Intel PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704A, and 8708 families.**
- **Personality cards used for specific Intel PROM programming requirements.**
- **Zero insertion force sockets for both 16-pin and 24-pin PROMs.**
- **Flexible power source for system logic and programming pulse generation.**
- **PROM programming verification facility.**
- **Stand alone or rack mountable.**
- **Fully compatible with the Intellec® MDS Microcomputer Development System.**

The Universal PROM Programmer is capable of programming and verifying the following Intel® PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704, and 8708 families. It is a peripheral device which interfaces with a suitable control device such as the Intellec® MDS microcomputer development system. The control device transfers commands, memory addresses, control information and data to the PROM Programmer enabling it to program or read a particular PROM.

The Universal PROM Programmer consists of a controller module, two personality card sockets, front panel, power supplies, chassis, and when used with the Intellec MDS a suitable interconnection cable.

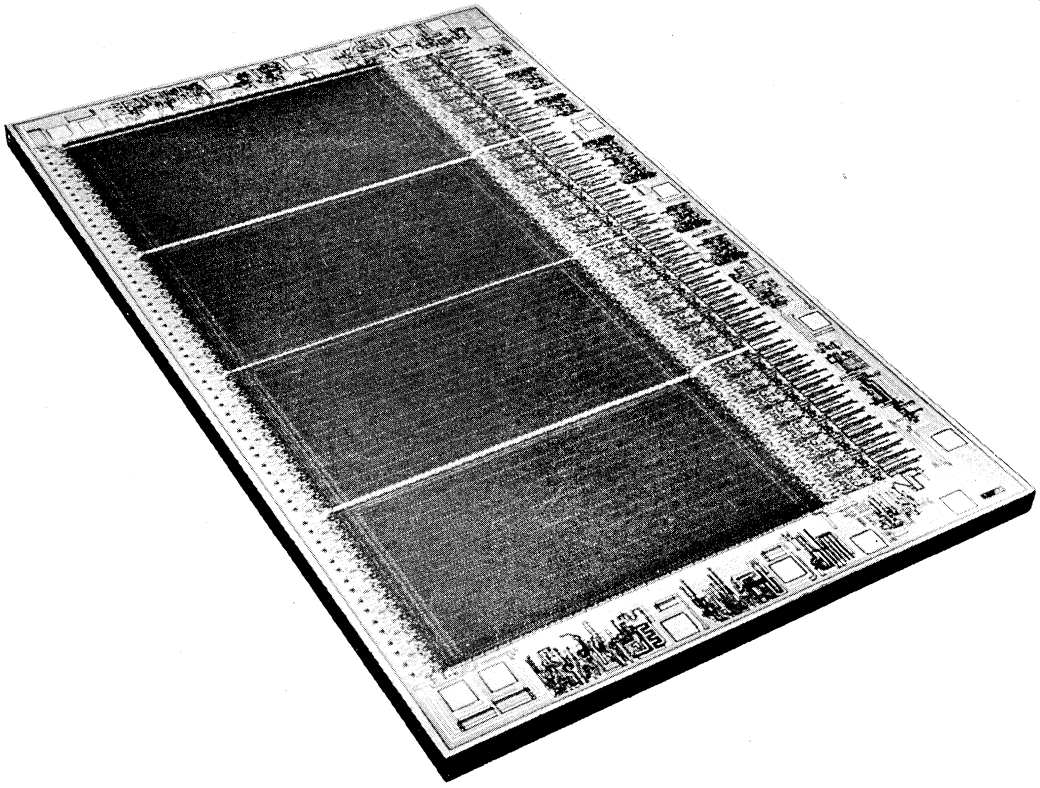
An Intel® 4040 based intelligent controller monitors the interface to the control device and supervises the command generation and data transfer interface between the selected PROM personality card and the control device. The 4040 CPU operates in conjunction with a fixed central control program residing in an Intel® 4001 ROM. Each Intel® PROM to be programmed is driven by a unique personality card which contains the appropriate pulse generation functions and driver circuitry. Hence, programming and verifying any Intel® PROM may be accomplished by selecting and plugging in the appropriate personality card option. The front panel contains a power-on switch and indicator, reset switch, and two zero-force insertion sockets (one 16-pin and one 24-pin or two 24-pin). A central power supply provides regulated power for system logic and ±40 and +70 volts for PROM programming pulse generation.

When used with the Intellec® MDS PROM programming commands are initiated from the Intellec® MDS system console and are implemented by programs in the Intellec® MDS. The desired PROM image is loaded into Intellec® MDS RAM through a user selected input medium (e.g., TTY, diskette drive, high speed paper tape reader). Next, the PROM programming command is issued specifying the location of the programming data, the socket option, the "nibble" option (upper or lower four bits of an 8-bit RAM data byte), and PROM starting address. The PROM programming algorithm programs each specified PROM location, compares the resulting PROM word with the source data, and regenerates program pulses when necessary. The Intellec® MDS system monitor contains a compare feature which allows specified sections of programmed PROM to be compared with MDS resident RAM. A transfer feature which can be used to copy the contents of a PROM to MDS RAM for PROM duplication is also included.

The Universal PROM Programmer may be used as a table top unit or mounted in a standard 19" RETMA cabinet.

4

SERIAL MEMORIES



SERIAL MEMORIES

	Type	No. Of Bits	Description	Electrical Characteristics Over Temperature						
				Data Rep. Rate		Power Dissipation Max.[1]	Input Output Levels	Clock Levels	Supplies[V]	Page No.
				Min.	Max.					
SILICON GATE MOS	1402A	1024	Quad 256-Bit Dynamic	10kHz	5MHz	500mW	TTL	MOS/TTL	5, -5 or 5, -9	4-3
	1403A	1024	Dual 512-Bit Dynamic	10kHz	5MHz	500mW	TTL	MOS/TTL	5, -5 or 5, -9	4-3
	1404A	1024	1024-Bit Dynamic	10kHz	5MHz	500mW	TTL	MOS/TTL	5, -5 or 5, -9	4-3
	1405A	512	Dynamic Recirculating	10kHz	2MHz	400mW	TTL	MOS/TTL	5, -5, or 5, -9	4-7
	2401	2048	Dual 1024-Bit Dynamic Recirculating	25kHz	1MHz	350mW	TTL	TTL	+5	4-11
	2405	1024	1024-Bit Dynamic Recirculating	25kHz	1MHz	350mW	TTL	TTL	+5	4-11
	2416	16,384	CCD Serial Memory	125kHz	2MHz	300mW	TTL	MOS	+12, -5	4-15

Note: Power Dissipation calculated with maximum power supply current and nominal supply voltages.

1402A, 1403A, 1404A

1024 BIT DYNAMIC SHIFT REGISTER

- **Guaranteed 5 MHz Operation over Temperature Range**
- **Low Power Dissipation --.1 mW/bit at 1 MHz**
- **DTL, TTL Compatible**
- **Low Clock Capacitance -- 140 pF**
- **Low Clock Leakage -- ≤ 1 μA**
- **Inputs Protected Against Static Charge**
- **Standard Packaging -- 8 Lead Metal Can, 16 Pin Ceramic Dual In-Line**
- **Three Standard Configurations -- Quad 256 Bit -- 1402A, Dual 512 Bit -- 1403A, Single 1024 Bit -- 1404A**

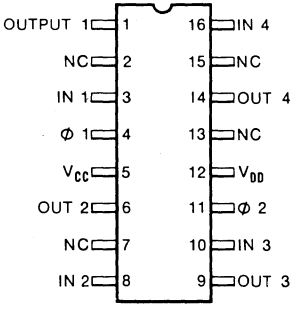
The 1402A/1403A/1404A are direct pin for pin replacements for the 1402/1403/1404. Due to "on chip" multiplexing the data rate is twice the clock rate. Data is shifted one bit on each clock pulse (both ϕ_1 and ϕ_2).

The 1402A/1403A/1404A family is ideally suited for usage in low cost serial memories or delay line applications. A high speed data rate of 5 MHz is easily obtained at the power supplies of +5V and −5V. The 1402A/3A/4A are capable of operating at the power supply voltages of +5V, −9V as well as +5V, −5V.

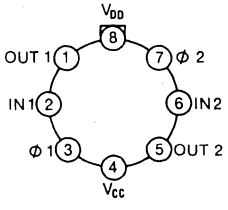
The input to the shift register can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The design of the output stage provides driving capability for both MOS and bipolar IC's.

Use of low threshold **silicon gate technology** allows high speed (5 MHz guaranteed) while reducing power dissipation by a factor of **two** and clock input capacitance by a factor of **three** compared to equivalent products manufactured by conventional technologies.

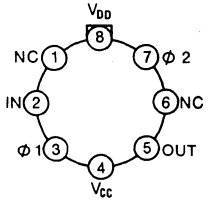
PIN CONFIGURATION



C1402A/P1402A



M1403A



M1404A

Absolute Maximum Ratings[1]

Temperature Under Bias	0°C to 70°C	Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.5V to −20V
Storage Temperature	−65°C to +160°C		
Power Dissipation[2]	1 Watt		

D.C. Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = −5V ±5% or −9V ±5%

SYMBOL	TEST	MIN.	TYP[3]	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current		<10	500	nA	T_A =25°C
I_{LO}	Output Leakage Current		<10	1000	nA	V_{OUT}=0.0V, T_A=25°C
I_{LC}	Clock Leakage Current		10	1000	nA	Max. V_{ILC}, T_A=25°C
V_{IL}	Input "Low" Voltage	V_{CC}−10		V_{CC}−4.2	V	
V_{IH}	Input "High" Voltage	V_{CC}−1.5		V_{CC}+.3	V	

V_{DD} = −5V ±5%

I_{DD1}	Power Supply Current		40	50	mA	T_A=25°C: Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −17V
I_{DD2}	Power Supply Current			56	mA	T_C=0°C: Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −17V
V_{ILC}	Clock Input Low Voltage	V_{CC}−17		V_{CC}−15	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1}=3K to V_{DD}, I_{OL}= 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1}=3K to V_{DD}, I_{OH}= −100 µA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.4	V_{CC}−1		V	R_{L2}=4.7K to V_{DD} (See p. 6 for connection)

V_{DD} = −9V ±5%

I_{DD3}	Power Supply Current		30	40	mA	T_A=25°C: Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −14.7V
I_{DD4}	Power Supply Current			45	mA	T_C=0°C: Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −14.7V
V_{ILC}	Clock Input Low Voltage	V_{CC}−14.7		V_{CC}−12.6	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1}=4.7K to V_{DD}, I_{OL}= 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1}=4.7K to V_{DD}, I_{OH}=−100µA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.4	V_{CC}−1		V	R_{L2}=6.2K to V_{DD}, R_{L3}=3.9K to V_{CC} (See p. 6 for connection)

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 1 watt dissipation is not to be construed as an operating rating (see note 1). For operating at elevated temperatures the device must be derated based as shown on page 3. When operating at V_{DD} = −5V±5% the maximum duty cycle is 33% and at V_{DD}=−9V+5% the maximum duty cycle is 26%. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $[t_{\phi PW} + \frac{1}{2}(t_R + t_F)]$x clock rate.

Note 3: Typical values are at T_A = 25°C and at nominal voltages.

A.C. Characteristics T_A = 0°C to 70°C; V_{CC} = +5V ±5%

SYMBOL	TEST	V_{DD} =−5V ±5% (Test Load 1)		V_{DD} =−9V ±5% (Test Load 2)		UNIT
		MIN.	MAX.	MIN.	MAX.	
Frequency	Clock Rep Rate		2.5		1.5	MHz
Frequency	Data Rep Rate	Note 1	5.0	Note 1	3.0	MHz
$t_{\phi PW}$	Clock Pulse Width	.130	10	.170	10	µsec
$t_{\phi D}$	Clock Pulse Delay	10	Note 1	10	Note 1	nsec
t_R, t_F	Clock Pulse Transition		1000		1000	nsec
t_{DW}	Data Write Time (Set Up)	30		60		nsec
t_{DH}	Data To Clock Hold Time	20		20		nsec
t_{A+},t_{A-}	Clock To Data Out Delay		90		110	nsec

CAPACITANCE[2] V_{CC}= +5V ±5%, V_{DD}= −5V ±5% or −9V ±5%, T_A = 25°C

SYMBOL	TEST	TYP.	MAX.	CONDITIONS
C_{IN}	Input Capacitance	5 pF	10 pF	V_{IN} = V_{CC}
C_{OUT}	Output Capacitance	5 pF	10 pF	V_{OUT} = V_{CC}
C_ϕ	Clock Capacitance	110 pF	140 pF	V_ϕ = V_{CC}
$C_{\phi 1\,\phi 2}$	Clock to Clock Capacitance	11 pF	16 pF	V_ϕ = V_{CC}

f = 1 MHz

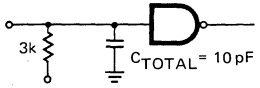
Note 1: See page 5 for guaranteed curve. Note 2: This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test

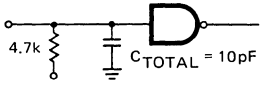
Input rise and fall times: 10 nsec
Output load is 1 TTL gate

TEST LOAD 1



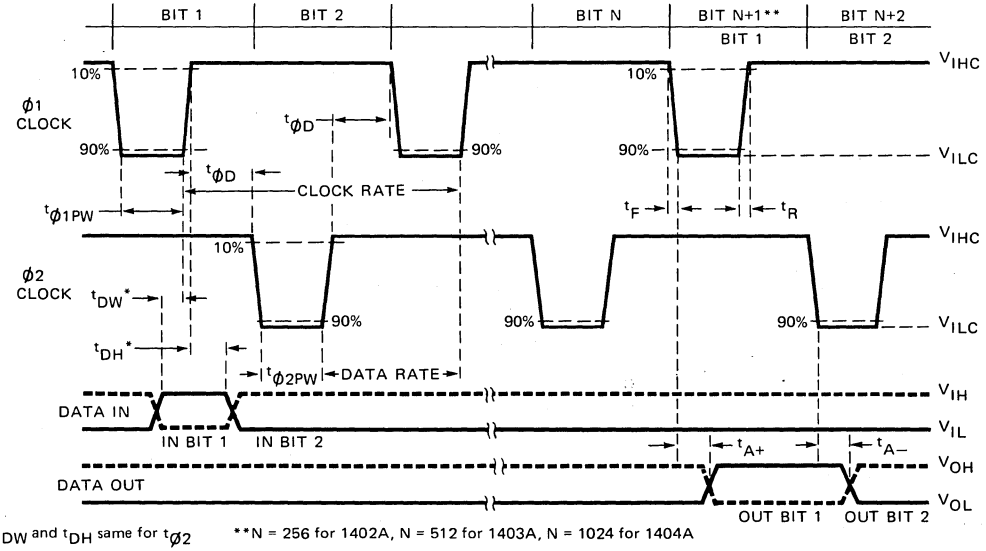
V_{DD}= −5V ± 5%

TEST LOAD 2



V_{DD}= −9V ± 5%

Timing Diagram

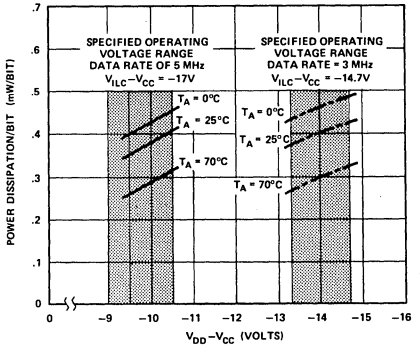


*t_{DW} and t_{DH} same for $t_{\phi 2}$ **N = 256 for 1402A, N = 512 for 1403A, N = 1024 for 1404A

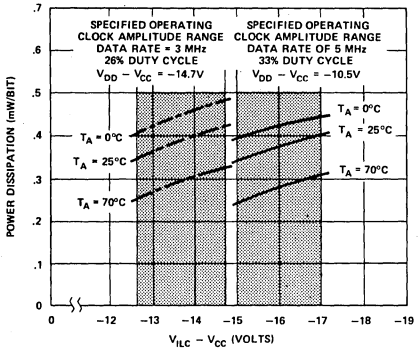
SERIAL MEMORIES

Typical Characteristics

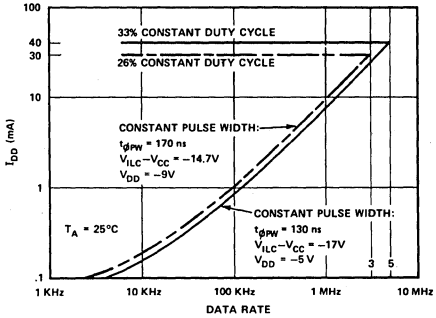
POWER DISSIPATION / BIT VS SUPPLY VOLTAGE



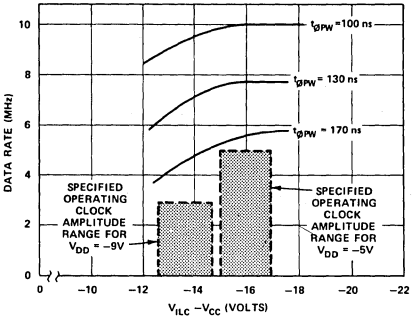
POWER DISSIPATION / BIT VS CLOCK AMPLITUDE



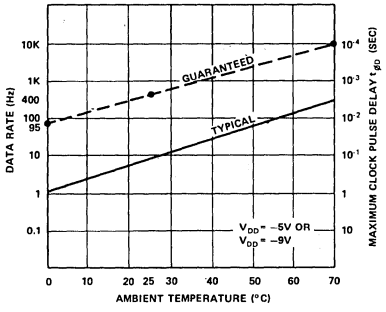
I_{DD} CURRENT VS DATA RATE



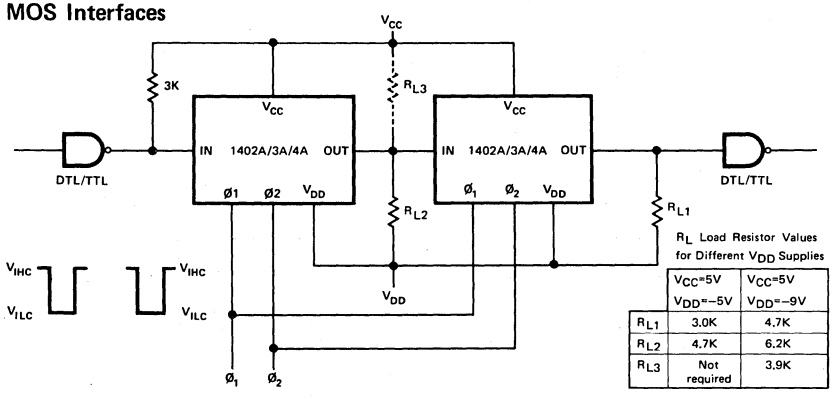
MAXIMUM DATA RATE VS CLOCK AMPLITUDE



MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS TEMPERATURE



DTL/TTL MOS Interfaces



R_L Load Resistor Values for Different V_{DD} Supplies

	V_{CC}=5V, V_{DD}=−5V	V_{CC}=5V, V_{DD}=−9V
R_{L1}	3.0K	4.7K
R_{L2}	4.7K	6.2K
R_{L3}	Not required	3.9K

512 BIT DYNAMIC RECIRCULATING SHIFT REGISTER

- **High Frequency Operation -- 2 MHz Guaranteed over Temperature.**
- **DTL, TTL Compatible**
- **Write/Recirculate and Read Controls Incorporated on the Chip**
- **Low Power Dissipation--.3 mW/bit at 1 MHz**
- **Low Clock Capacitance--85 pF**
- **Low Clock Leakage -- ≤1 uA at —17 V**
- **Simple Two Dimensional Memory Matrix Organization -- 2 Chip Select Controls**
- **Inputs Protected Against Static Charge**
- **Standard Packaging--10 Lead Low Profile TO-99**

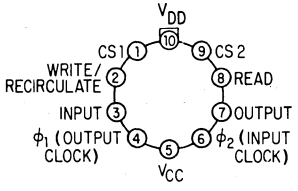
The 1405A is a 512 bit dynamic recirculating shift register and is a direct pin replacement for the 1405. The 1405A is capable of operating at power supply voltages of +5V, —9V as well as +5V, —5V. A high speed recirculating data rate of 2 MHz over the temperature is easily obtained at the +5, —5 power supplies.

Write/recirculate and read controls eliminate the need for external logic elements when recirculating data. In addition, any number of devices can be combined to form a multi-dimensional memory array. For this purpose two chip select controls have been provided.

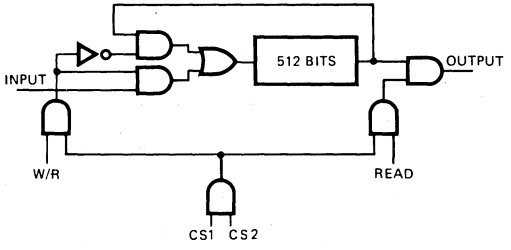
These registers can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for both MOS and bipolar IC's as well as OR-tieing of shift registers. The 1405A is ideally suited for usage in low cost memories or delay line applications.

Use of low threshold **silicon gate technology** allows high speed (2 MHz guaranteed) while reducing power dissipation by a factor of **two** and clock input capacitance by a factor of **three** over equivalent products manufactured by conventional technologies.

PIN CONFIGURATION



LOGIC DIAGRAM



MODE \ PIN	W/R (2)	CS1 (1)	CS2 (9)	READ (8)
WRITE	1	1	1	1 or 0
RECIRCULATE(1)	1 or 0	1 or 0	1 or 0	1 or 0
READ	1 or 0	1	1	1

Note 1: Either W/R, CS1, or CS2 must be a "0" during Recirculation.
A logic 1 is defined as a high input and a logic 0 as a low input.

Maximum Guaranteed Ratings *

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +160°C
Power Dissipation(1)	600 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+.3V to −20V

* COMMENT:

Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = −5V ± 5%

SYMBOL	TEST	MIN.	TYP.(2)	MAX.	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	1000	nA	$V_{IN} = V_{IH}$ to V_{IL}
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	V_{OUT} = 0.0V
I_{LC}	CLOCK LEAKAGE CURRENT		10	1000	nA	$V_{ILC}=V_{CC}-17V$
I_{DD1}	POWER SUPPLY CURRENT		25	40	mA	T_A=25°C, Output at Logic "0", 2 MHz Data Rate, 40% Duty Cycle, Continuous Operation,
I_{DD2}	POWER SUPPLY CURRENT			45	mA	T_C=0°C, $V_{ILC}=V_{CC}-17V$
V_{ILC1}	CLOCK INPUT LOW VOLTAGE	$V_{CC}-17$		$V_{CC}-14.5$	V	
V_{IHC}	CLOCK INPUT HIGH VOLTAGE	$V_{CC}-1$		$V_{CC}+.3$	V	
V_{IL}	INPUT "LOW" VOLTAGE	$V_{CC}-10$		$V_{CC}-4.2$	V	
V_{IH1}	INPUT "HIGH" VOLTAGE	$V_{CC}-1.5$		$V_{CC}+.3$	V	
V_{OL}	OUTPUT LOW VOLTAGE		−.3	0.5	V	R_{L1}=3K to V_{DD}, I_{OL}= 1.6 mA
V_{OH}	OUTPUT HIGH VOLTAGE DRIVING TTL	2.4	3.5		V	R_{L1}=3K to V_{DD}, I_{OH}= −100 μA
V_{OH1}	OUTPUT HIGH VOLTAGE DRIVING MOS	$V_{CC}-1.4$	$V_{CC}-1$		V	R_{L2}=5.6K to V_{DD} (see p. 6 for connection)

V_{DD} = −9V ± 5%

I_{LI}	INPUT LOAD CURRENT		10	1000	nA	$V_{IN} = V_{IH}$ to V_{IL}
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	V_{OUT} = 0.0V
I_{LC}	CLOCK LEAKAGE CURRENT		10	1000	nA	$V_{ILC}=V_{CC}-14.7V$
I_{DD3}	POWER SUPPLY CURRENT		20	31	mA	T_A =25°C, Output at Logic "0", 1.5 MHz Data Rate, 36% Duty Cycle, Continuous Operation,
I_{DD4}	POWER SUPPLY CURRENT			36	mA	T_C =0°C, $V_{ILC}=V_{CC}-14.7V$
V_{ILC2}	CLOCK INPUT LOW VOLTAGE	$V_{CC}-14.7$		$V_{CC}-12.6$	V	
V_{IHC}	CLOCK INPUT HIGH VOLTAGE	$V_{CC}-1$		$V_{CC}+.3$	V	
V_{IL}	INPUT "LOW" VOLTAGE	$V_{CC}-10$		$V_{CC}-4.2$	V	
V_{IH2}	INPUT "HIGH" VOLTAGE	$V_{CC}-1.5$		$V_{CC}+.3$	V	
V_{OL}	OUTPUT LOW VOLTAGE		−.3	0.5	V	R_{L1}=5.6K to V_{DD} I_{OL}= 1.6 mA
V_{OH}	OUTPUT HIGH VOLTAGE DRIVING TTL	2.4	3.5		V	R_{L1}=5.6K to V_{DD}, I_{OH}=−100 μA
V_{OH1}	OUTPUT HIGH VOLTAGE DRIVING MOS	$V_{CC}-1.4$	$V_{CC}-1$		V	R_{L2}=6.2K to V_{DD} (See p. 6 for R_{L3}=3.9K to V_{CC} connection)

Note 1: For operating at elevated temperatures the device must be derated based as shown on page 3. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $[t_{\phi PW} + \frac{1}{2}(t_R + t_F)]$ x clock rate.

Note 2: Typical values are at T_A = 25°C and at nominal voltages.

A.C. Characteristics $T_A = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$; $C_L = 20pF$; 1 TTL Load

SYMBOL	TEST	$V_{DD} = -5V \pm 5\%$ $V_{ILC}=V_{CC}-14.5$ to $V_{CC}-17$ $R_L = 3$ K		$V_{DD} = -9V \pm 5\%$ $V_{ILC}=V_{CC}-12.6$ to $V_{CC}-14.7$ $R_L = 5.6$ K		UNIT
		MIN.	MAX.	MIN.	MAX.	
Frequency	CLOCK DATA REP RATE	200 Hz @ 25°C(1)	2	200Hz @ 25°C(1)	1.5	MHz
$t_{\phi PW}$	CLOCK PULSE WIDTH	0.200	10	.240	10	μsec
$t_{\phi D}$	CLOCK PULSE DELAY	30	Note 1	30	Note 1	nsec
Duty Cycle(2)	CLOCK DUTY CYCLE		40		36	%
t_R;t_F	CLOCK PULSE TRANSITION		1		1	μsec
t_{DW}	DATA WRITE (SETUP) TIME	100		100		nsec
t_{DH}	DATA TO CLOCK HOLD TIME	20		20		nsec
t_{A+}; t_{A-}	CLOCK TO DATA OUT DELAY		250		250	nsec
t_{R-}; t_{CS-}; t_{WR-}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		0		nsec
t_{R+}; t_{CS+}; t_{WR+}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		0		nsec

CAPACITANCE(3) $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$ or $-9V \pm 5\%$, $T_A = 25°C$

SYMBOL	TEST	TYP.	MAX.	CONDITIONS	
C_{IN}	INPUT CAPACITANCE	3	5 pF	$V_{IN} = V_{CC}$	f = 1 MHz
C_{OUT}	OUTPUT CAPACITANCE	2	5 pF	$V_{OUT} = V_{CC}$	
C_ϕ	CLOCK CAPACITANCE	75	85 pF	$V_\phi = V_{CC}$	
$C_{\phi_1\text{-}\phi_2}$	CLOCK TO CLOCK CAPACITANCE	6	10 pF	$V_\phi = V_{CC}$	

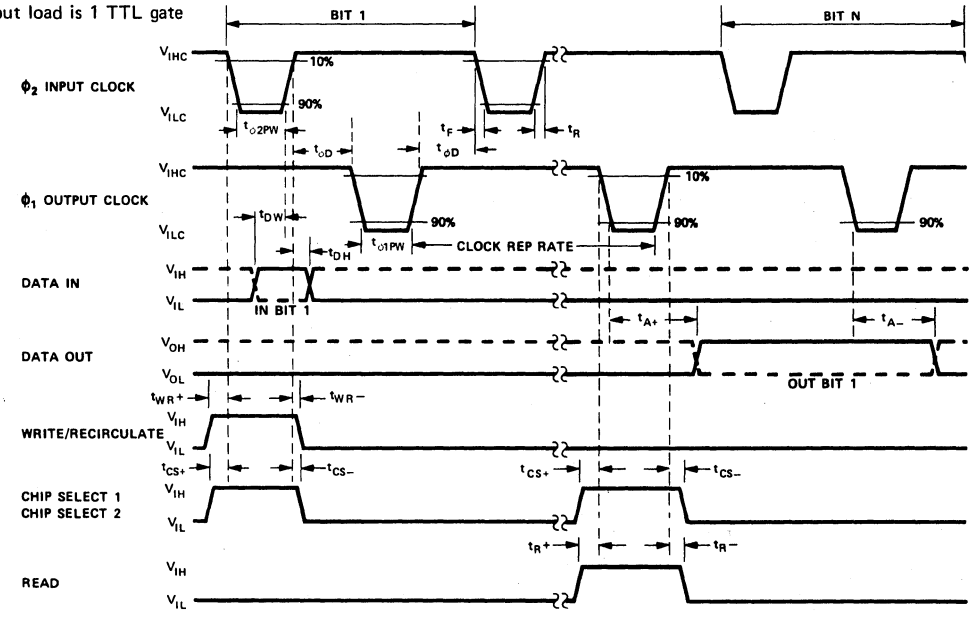
Note 1: See curve of Min Data Rate, and Max Clock Delay vs. Temp. on page 5. Note 2: Duty Cycle = $[t_{\phi PW} + \frac{1}{2}(t_R + t_F)]$ x clock rate.
Note 3: This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test

Input rise and fall times: 10 nsec
Output load is 1 TTL gate

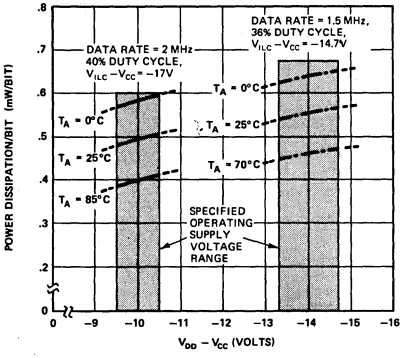
Timing Diagram



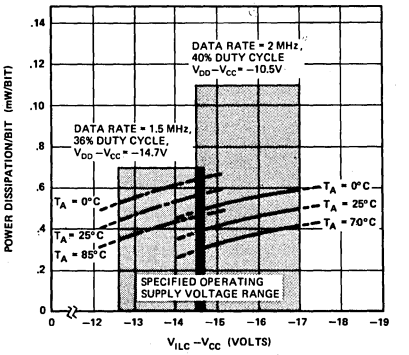
SERIAL MEMORIES

Typical Characteristics

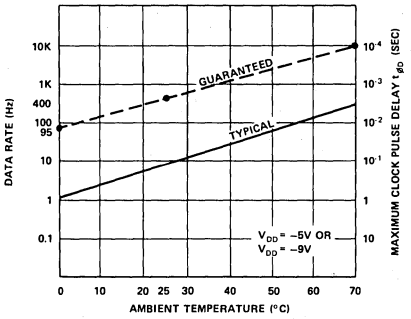
POWER DISSIPATION/BIT VS. SUPPLY VOLTAGE



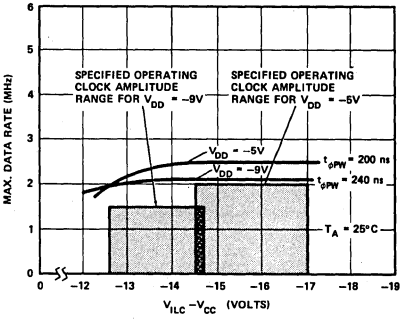
POWER DISSIPATION/BIT VS. CLOCK AMPLITUDE



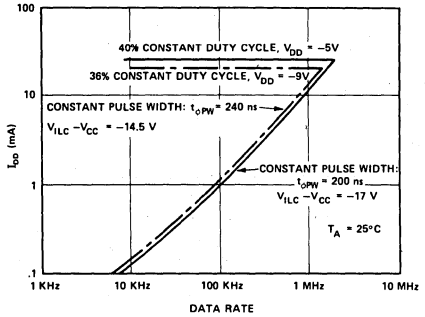
MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS TEMPERATURE



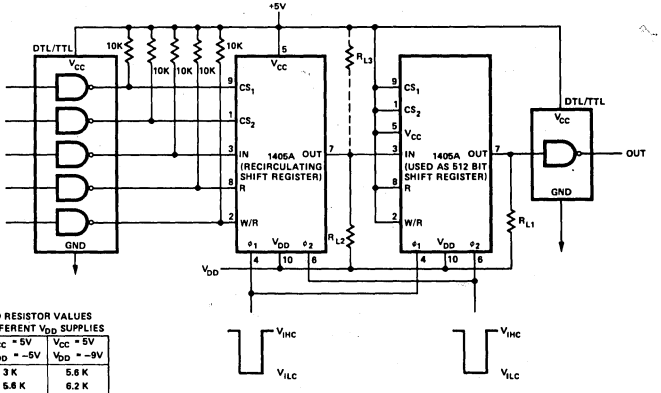
MAXIMUM DATA RATE VS. CLOCK AMPLITUDE



I_{DD} CURRENT VS. DATA RATE



DTL/TTL/MOS Interfaces



R_L LOAD RESISTOR VALUES FOR DIFFERENT V_{DD} SUPPLIES

	V_{CC} = 5V, V_{DD} = −5V	V_{CC} = 5V, V_{DD} = −9V
R_{L1}	3 K	5.6 K
R_{L2}	5.6 K	6.2 K
R_{L3}	not required	3.9 K

2048/1024 BIT DYNAMIC RECIRCULATING SHIFT REGISTERS

- **Single Supply Voltage -- +5 Volts**
- **Fully TTL Compatible -- Inputs, Outputs and Clock**
- **Single Phase Clock**
- **Guaranteed 1 MHz Operation with 100 pF Load, over Temperature Range**
- **Low Power Dissipation -- 120 μw/bit typically at 1 MHz**
- **Low Clock Capacitance -- 7 pF**
- **Write/Recirculate and Chip Select Logic Incorporated on Chip**
- **Standard Configurations -- Dual 1024 Bit -- 2401 Single 1024 Bit -- 2405**

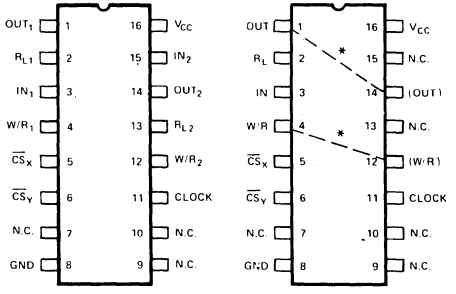
The 2401/2405 are 2048/1024 bit dynamic recirculating shift registers. They are directly TTL compatible in all respects: inputs, outputs, clock and a single +5 volt power supply.

Write/recirculate controls are provided to eliminate the need for external logic elements when recirculating data.

Two chip select inputs have been provided to allow easy selection of an individual package when outputs of several devices have been "OR-tied". A separate internal "pullup" resistor (R_L) is provided which can be externally connected to the output pin to achieve full signal swing.

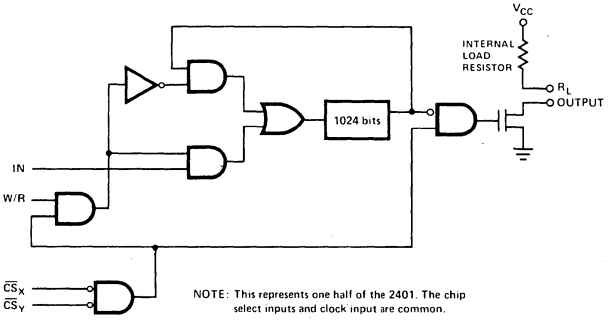
This Intel shift register family is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy to use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible, including clocks.

PIN CONFIGURATIONS



* DASH LINES INDICATE NECESSARY EXTERNAL PRINTED CIRCUIT BOARD CONNECTIONS FOR PROPER OPERATION OF THE 2405. (SEE APPLICATION SECTION)

LOGIC DIAGRAM



NOTE: This represents one half of the 2401. The chip select inputs and clock input are common.

PIN NAMES

IN	DATA INPUT	OUT	DATA OUTPUT
W/R	WRITE/RECIRCULATE CONTROL	R_L	INTERNAL LOAD RESISTOR
$\overline{CS}_X$, $\overline{CS}_Y$	CHIP SELECT INPUT	N.C.	NO CONNECTION

TRUTH TABLE

FUNCTION	PIN SYMBOL W/R	$\overline{CS}_X$	$\overline{CS}_Y$
WRITE MODE	H	L	L
RECIRCULATE	L	X	X
	X	H	X
	X	X	H
READ MODE	X	L	L

H = Logic High Level L = Logic Low Level
X = Don't Care Condition

Absolute Maximum Ratings*

Ambient Temperature Under Bias: 0° C to 70° C
Storage Temperature: −65° C to +150° C
Power Dissipation: 1W
Voltage on Any Pin with Respect to Ground: −0.5V to +7V

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

T_A = 0°to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

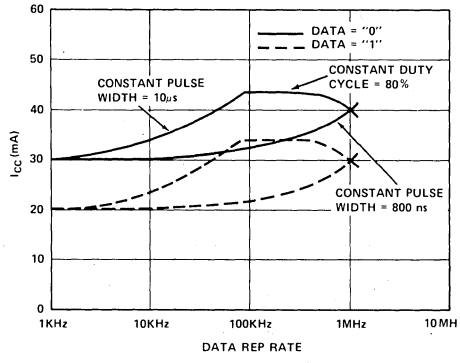
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.[1]	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{LI}	INPUT LEAKAGE			10	μA	V_{IN} = 5.25V
I_{LO}	OUTPUT LEAKAGE			100	μA	V_{OUT} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		45 50	70 80	mA mA	T_A = 25°C, V_{CC} = 5.25V; T_A = 0°C, 80% DUTY CYCLE
V_{IH}	INPUT HIGH LEVEL VOLTAGE (ALL INPUTS)	2.2		5.25	V	
V_{IL}	INPUT LOW LEVEL VOLTAGE (ALL INPUTS)	-0.3		0.65	V	
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE	2.4		V_{CC}	V	I_{OH} = -1mA, R_L = 1.5K ± 5% ohms, external
V_{OL}	OUTPUT LOW LEVEL VOLTAGE	0		0.45	V	I_{OL} = 5.0mA, R_L = 1.5K ± 5% ohms, external[2]

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. The following was used to calculate I_{OL}.

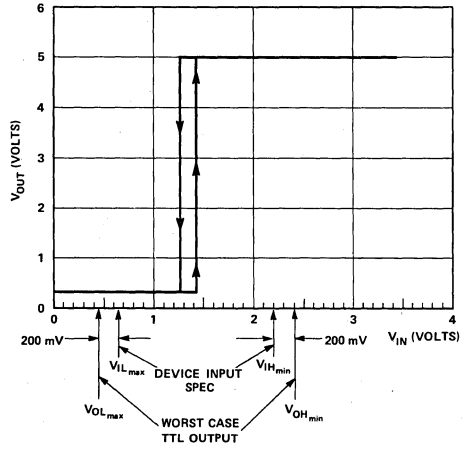
$$I_{OL} = \frac{V_{CC}\ (max.) - V_{OL}\ (max.)}{R_L\ (min.)} + I_{LI}\ (TTL\ device) = \frac{5.25 - 0.45}{1.425} + 1.6 = 4.97mA.$$

Also note that the internal load resistor, R_{LI}, has a value ranging from 500 ohms minimum to 2,200 ohms maximum. The internal load resistor can be used when driving from one 2401/2405 to another 2401/2405 or to other MOS inputs.

POWER SUPPLY CURRENT (I_{CC}) VS. DATA REP RATE



EFFECTIVE INPUT CHARACTERISTIC



A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

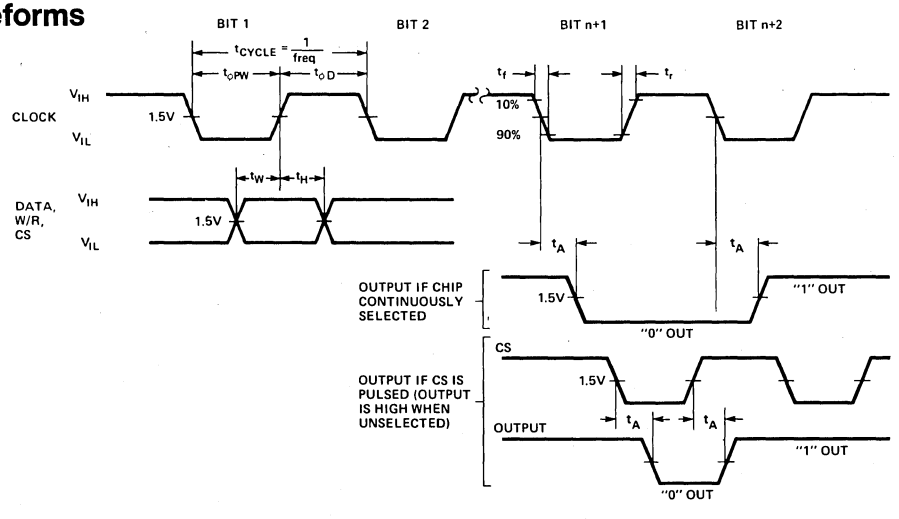
SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
FREQ. MAX.	MAX. DATA REP. RATE			1	MHz	
FREQ. MIN.	MIN. DATA REP. RATE	1 25[1]			KHz KHz	T_A = 25° C T_A = 70° C
$t_{\phi PW}$	CLOCK PULSE WIDTH	0.80		10	μs	
$t_{\phi D}$	CLOCK PULSE DELAY	0.20 0.20		1000 40	μs μs	T_A = 25° C T_A = 70° C
t_r , t_f	CLOCK RISE AND FALL TIME			50	ns	
t_W	WRITE TIME	200			ns	
t_H	HOLD TIME	150			ns	
t_A	ACCESS TIME FROM CLOCK OR CHIP SELECT		250	500	ns	R_L = 1.5K ± 5% ohm, EXTERNAL C_L = 100pF ONE TTL LOAD

NOTE: 1. 100 kHz in plastic (P) package.

Capacitance T_A = 25° C

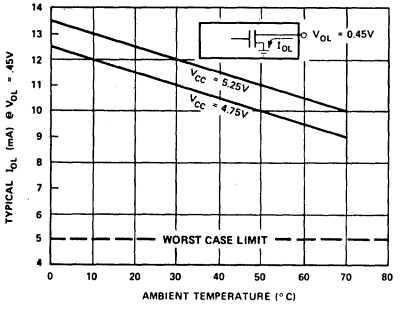
SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
C_{IN}	DATA, W/R & CS INPUT CAPACITANCE		4	7	pF	ALL PINS AT AC GROUND; 250 mV PEAK TO PEAK, 1 MHz
C_{OUT}	OUTPUT CAPACITANCE		10	14	pF	
C_ϕ	CLOCK CAPACITANCE		4	7	pF	

Waveforms

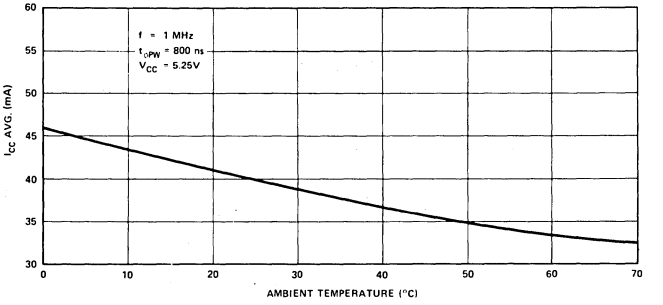


D. C. Characteristics

TEMPERATURE DEPENDENCE OF OUTPUT LOW LEVEL SINK CAPABILITY

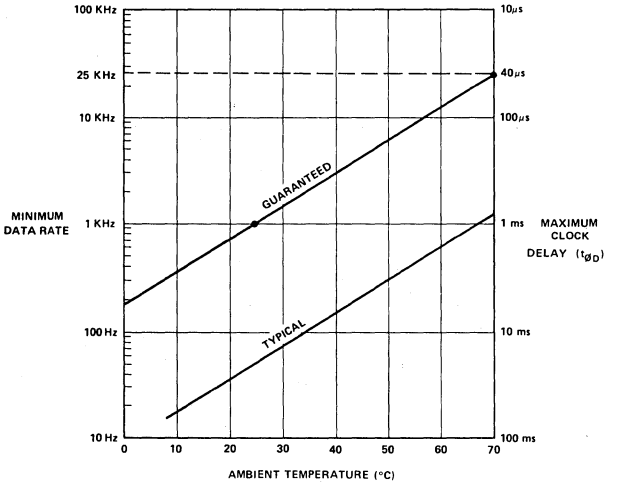


POWER SUPPLY CURRENT (I_{CC}) VS. AMBIENT TEMPERATURE (°C)

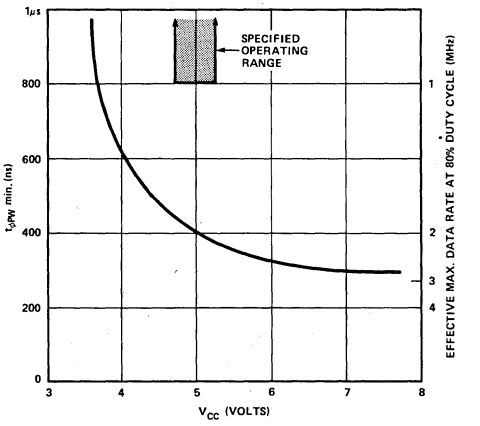


A. C. Characteristics

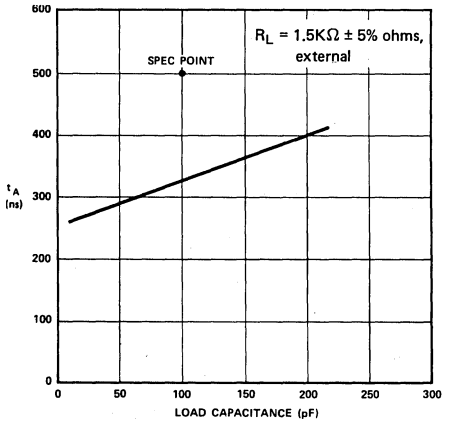
MINIMUM DATA RATE AND MAXIMUM CLOCK DELAY VS. AMBIENT TEMPERATURE FOR CERAMIC (C) PACKAGE



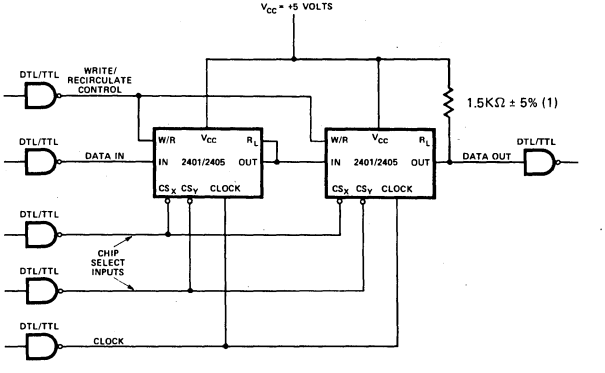
MINIMUM CLOCK PULSE WIDTH AND EFFECTIVE MAXIMUM DATA RATE AT 80% DUTY CYCLE VS. POWER SUPPLY VOLTAGE (V_{CC})



ACCESS TIME VS. LOAD CAPACITANCE



Typical Application Of TTL Compatible Shift Registers



NOTE (1): The 2401/2405 is directly compatible device to device. An external 1.5KΩ ± 5% load resistor is recommended for driving one TTL load with the 2401/2405 output.

2416

16,384 BIT CCD SERIAL MEMORY

▪ Organization: 64 Recirculating Shift Registers of 256 Bits Each

- **Avg. Latency Time Under 100 μs**
- **Max. Serial Data Transfer Rate —2 mega bits/sec.**
- **Address Registers Incorporated on Chip**
- **Standard Power Supplies— +12V, −5V**
- **Open Drain Output**
- **Combined Read/Write Cycles Allowed**
- **Compatible to Intel® 5244 CCD Driver**

SERIAL MEMORIES

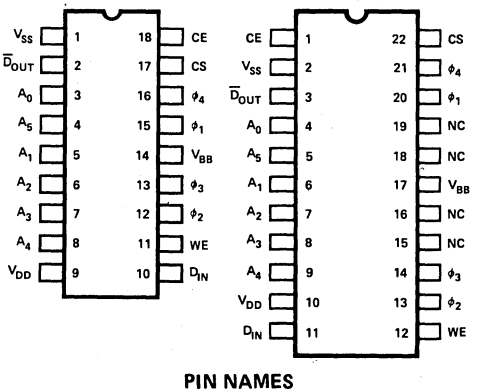
The Intel®2416 is a 16,384 bit CCD serial memory designed for low-cost memory applications requiring average latency times to under 100 μs. To achieve low latency time the memory was organized in the form of 64 independent recirculating shift registers of 256 bits each. Any one of the 64 shift registers can be accessed by applying an appropriate 6-bit address input.

The shift registers recirculate data automatically as long as the four-phase CCD clocks (ϕ_1 . . . ϕ_4) are continuously applied and no write command is given. A one-bit shift is initiated in all 64 registers following a low-to-high transition of either ϕ_2 or ϕ_4. After the shift operation the contents of the 64 registers at the bit location involved are available for non-destructive reading, and/or for modification. I/O functions are accomplished in a manner similar to that of a 64-bit dynamic RAM. At the next shift cycle, the contents of the 64 accessible bits (whether modified or not) are transferred forward into the respective registers and the contents of the next bit of each register become accessible. No I/O function can be performed during the shift operation itself.

The Intel 2416 generates and uses an internal reference voltage which requires some time to stabilize after the power supplies and four phase clocks have been turned on. No I/O functions should be performed until the four-phase CCD clocks have executed at least 4000 shift cycles with power supplies at operating voltages. After this start-up period, no special action is needed to keep the internal reference voltage stable.

The 2416 is fabricated using Intel's advanced high voltage N-channel Silicon Gate MOS process.

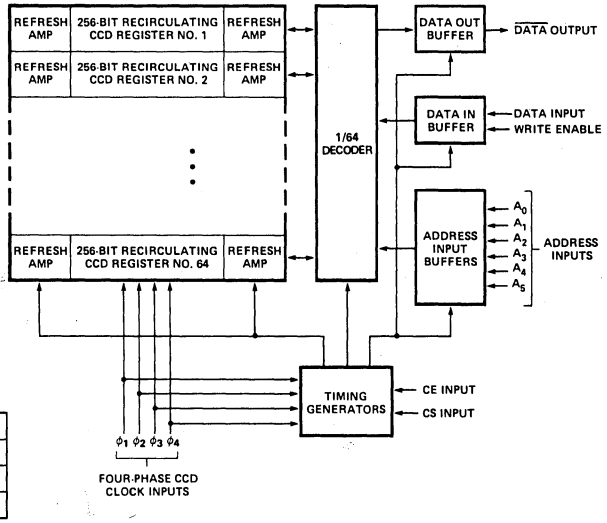
PIN CONFIGURATIONS



PIN NAMES

A_0-A_5	ADDRESS INPUTS	CE	CHIP ENABLE INPUT
D_{IN}	DATA INPUT	ϕ_1-ϕ_4	CCD CLOCK INPUTS
WE	WRITE ENABLE INPUT	V_{DD}, V_{SS}, V_{BB}	POWER SUPPLIES
CS	CHIP SELECT INPUT	$\overline{D}_{OUT}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . . +25V to -0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . . +20V to -0.3V
Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{BB}[1] = -5V ±5%, V_{SS} = 0V, unless otherwise specified.

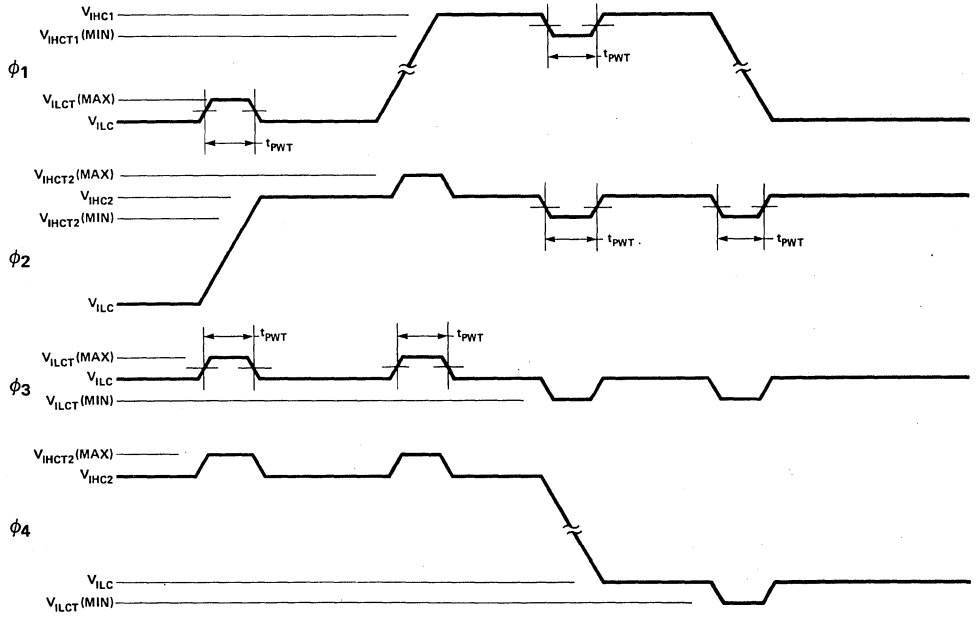
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Leakage Current		1	10	µA	V_{IN} = 0V
I_{LO}	Output Leakage Current		1	10	µA	CE = 0V, V_{OUT} = 0V
I_{OL}	Output Low Current	3			mA	V_{OL} = .45V
I_{OH}	Output High Current			10	µA	V_{OH} = +5V
I_{DDAV1}	Average V_{DD} Supply Current for Shift Cycles Only			Note 2	mA	
I_{DDAV2}[3]	Average V_{DD} Supply Current		15	25	mA	
I_{BB}	Average V_{BB} Supply Current		100	200	µA	
V_{IL}	Input Low Voltage, All Inputs Except $\phi_1 \ldots \phi_4$	-1.0		0.8	V	
V_{IH1}	Input High Voltage, All Inputs Except D_{IN} and $\phi_1 \ldots \phi_4$	V_{DD}-1		V_{DD}+1	V	
V_{IHD}	D_{IN} Input High Voltage	3.5		V_{DD}+1	V	
V_{ILC}[4]	$\phi_1 \ldots \phi_4$ Input Low Voltage dc	-2.0		0.6	V	
V_{ILCT}	$\phi_1 \ldots \phi_4$ Input Low Voltage w/Coupling	-2.0[5]		1.2[6]	V	
V_{IHC1}	ϕ_1 and ϕ_3 Input High Voltage dc	V_{DD}-1		V_{DD}+2	V	
V_{IHCT1}	ϕ_1 and ϕ_3 Input High Voltage w/Coupling	V_{DD}-1.6[6]		V_{DD}+2[5]	V	
V_{IHC2}	ϕ_2 and ϕ_4 Input High Voltage dc	V_{DD}-0.6		V_{DD}+2	V	
V_{IHCT2}	ϕ_2 and ϕ_4 Input High Voltage w/Coupling	V_{DD}-1.2[6]		V_{DD}+2[5]	V	
t_{PWT}	Cross Coupling Voltage Pulse Width			Note 7	ns	Pulse width measured at 0.8V and V_{DD}-1.2V (ϕ_1 and ϕ_3) or V_{DD}-0.8V (ϕ_2 and ϕ_4)

Notes: 1. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB}.

2. For shift only mode $I_{DD} = 2.0mA + \frac{15mA}{t_{\phi/2}\ (\text{in } \mu s)}$

3. I_{DDAV2} is for combined shift and data I/O cycles.
4. The difference in the low level reference voltages between all four clock phases must not exceed 0.5 volts.
5. These voltage levels with coupling are within the specified dc range and are not, therefore, subject to t_{PWT} restrictions.
6. These voltage levels with coupling are outside specified dc ranges and must be restricted to t_{PWT} pulse widths.
7. The maximum clock cross coupled pulse width is the sum of the clock transition time (t_T) plus 20ns.

$\phi_1 \ldots \phi_4$ CROSS-COUPLING

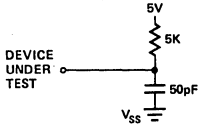


A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.

SHIFT ONLY CYCLES

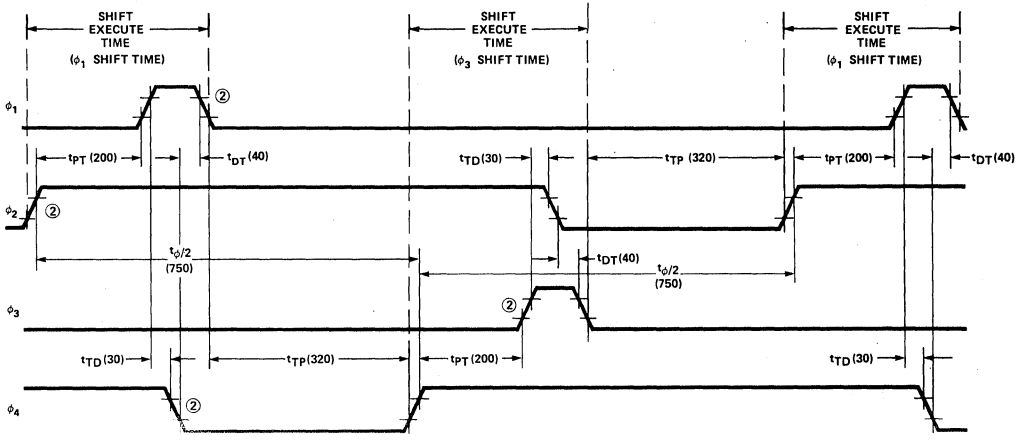
Symbol	Parameter	Min.	Max.	Unit	Conditions
$t_{\phi}/2$	Half Clock Period for $\phi_1 \ldots \phi_4$	750[1]	10,000	ns	t_T = 40nsec
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
t_{TP}	ϕ_1 Off to ϕ_4 On, ϕ_3 Off to ϕ_2 On	320		ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	

$\bar{D}_{OUT}$ TEST LOAD



Note: 1. The 750ns Half Clock Period will be met for 30ns $\leq t_T \leq$ 40ns. Values of $t_T >$ 40ns lengthen $t_{\phi}/2$.

WAVEFORMS (Numbers in parentheses are for minimum cycle timing in ns)



Note: 2. +2.0V and V_{DD}-2.0V are the reference low and high level respectively for measuring the timing of ϕ_1, ϕ_2, ϕ_3 and ϕ_4.

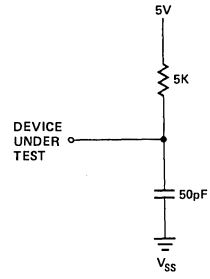
SERIAL MEMORIES

A.C. Characteristics

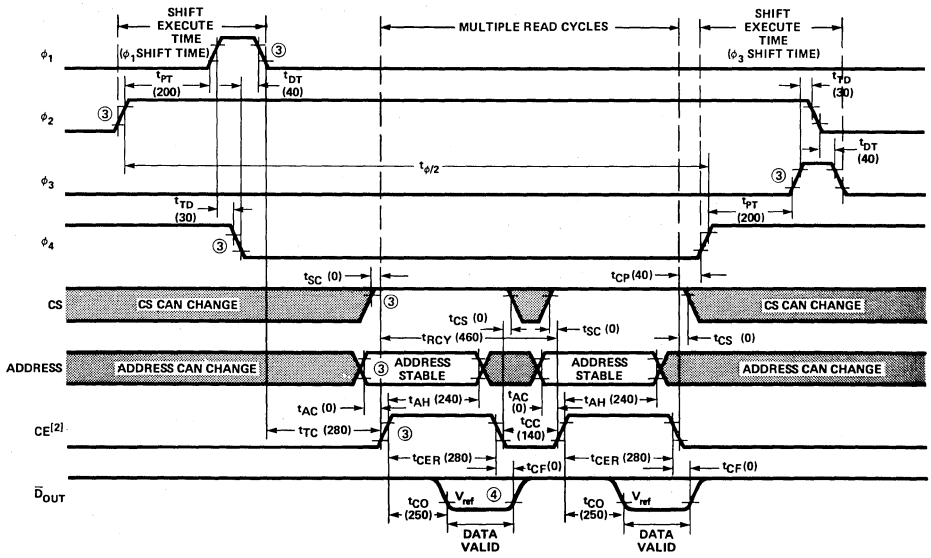
SHIFT–READ–READ–...–READ–SHIFT CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	READ Cycle Time	460		ns	
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	t_T = 40ns
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	t_{T1} = 20ns
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$		10,000	ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	
t_{T1}	Transition Times for Inputs Other Than $\phi_1 \ldots \phi_4$		100	ns	
t_{TC}	ϕ_1 or ϕ_3 Off to CE On	280		ns	
t_{SC}	CS to CE Set-Up Time	0		ns	
t_{AC}	Address to CD Set-Up Time	0		ns	
t_{AH}	Address Hold Time	240		ns	
t_{CS}	CE to CS Hold Time	0		ns	
t_{CC}	CE Off Time	140		ns	
t_{CP}	CE Off to ϕ_2 or ϕ_4 On	40		ns	
t_{CER}	CE On Time	280		ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	
t_{CO}	CE to $\overline{D}_{OUT}$ Valid	250		ns	

$\overline{D}_{OUT}$ TEST LOAD



WAVEFORMS[1] (Numbers in parentheses are for minimum cycle timing in ns)



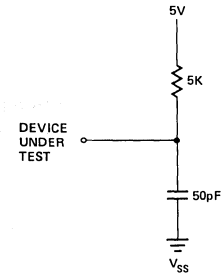
NOTES:
1. WE must be continuously low during the READ cycle.
2. When CE is off, the 2416 output level is determined by the external output termination.
3. +2.0V and V_{DD}-2.0V are the reference low and high level respectively for measuring the timing of $\phi_1 \ldots \phi_4$, CE, CS and addresses.
4. +0.8V is the reference level for measuring the timing of $\overline{D}_{OUT}$.

A.C. Characteristics

SHIFT–WRITE–WRITE–...–WRITE–SHIFT CYCLE

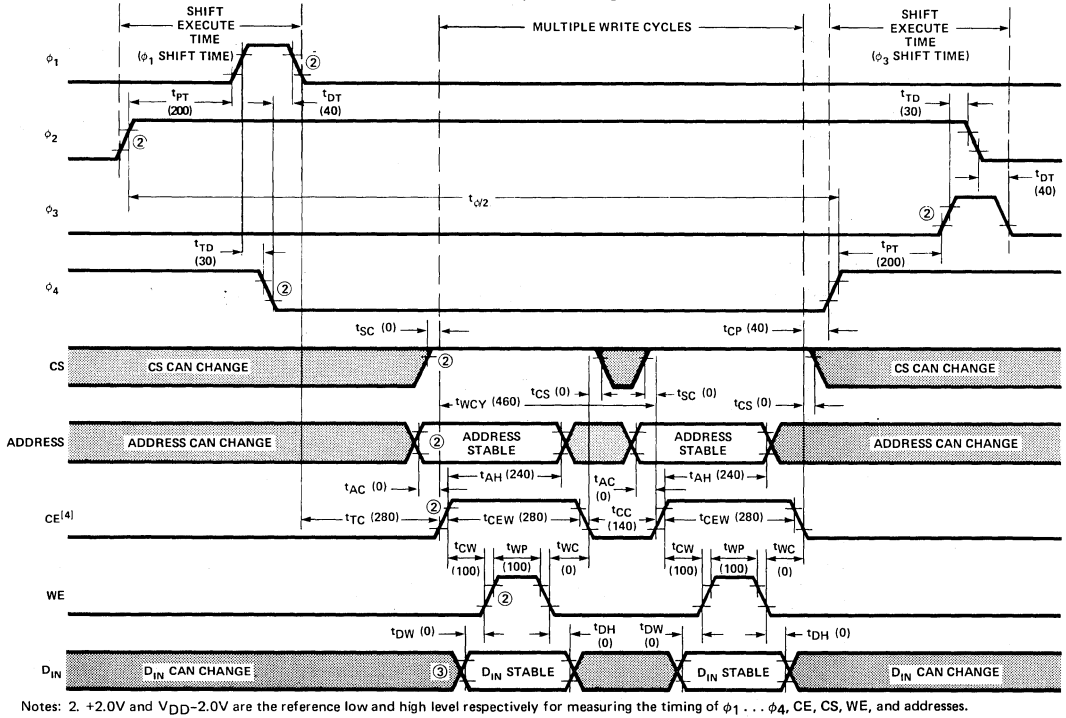
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	WRITE Cycle Time	460		ns	
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	t_T = 40ns
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	t_{T1} = 20ns
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$		10,000	ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	
t_{T1}	Transition Times for Inputs Other Than $\phi_1 \ldots \phi_4$		100	ns	
t_{TC}	ϕ_1 or ϕ_3 Off to CE On	280		ns	
t_{SC}	CS to CE Set-Up Time	0		ns	
t_{AC}	Address to CE Set-Up Time	0		ns	
t_{AH}	Address Hold Time	240		ns	
t_{CS}	CE to CS Hold Time	0		ns	
t_{CC}	CE Off Time	140		ns	
t_{CP}	CE Off to ϕ_2 or ϕ_4 On	40		ns	
t_{CEW}	CE On Time	280[1]		ns	
t_{CW}	CE to WE Set-Up Time	100[1]		ns	
t_{DW}	D_{IN} to WE Set-Up	0		ns	
t_{WP}	WE Pulse Width	100[1]		ns	
t_{WC}	WE Off to CE Off	0[1]		ns	
t_{DH}	D_{IN} Hold Time	0		ns	

$\bar{D}_{OUT}$ TEST LOAD



Note: 1. The minimum t_{CW}, t_{WP} and t_{WC} times with appropriate transitions do not necessarily add up to the minimum t_{CEW}. This allows the user flexibility in setting the WE Pulse Width edges without affecting either t_{CEW} or the WRITE Cycle Time, t_{WCY}.

WAVEFORMS (Numbers in parentheses are for minimum cycle timing in ns)



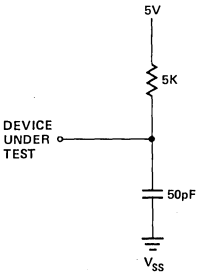
Notes: 2. +2.0V and V_{DD}–2.0V are the reference low and high level respectively for measuring the timing of $\phi_1 \ldots \phi_4$, CE, CS, WE, and addresses.
3. +1.5V and +3.0V are the reference low and high level respectively for measuring the timing of D_{IN}.

SERIAL MEMORIES

A.C. Characteristics SHIFT–RMW–RMW– . . . –RMW–SHIFT CYCLE

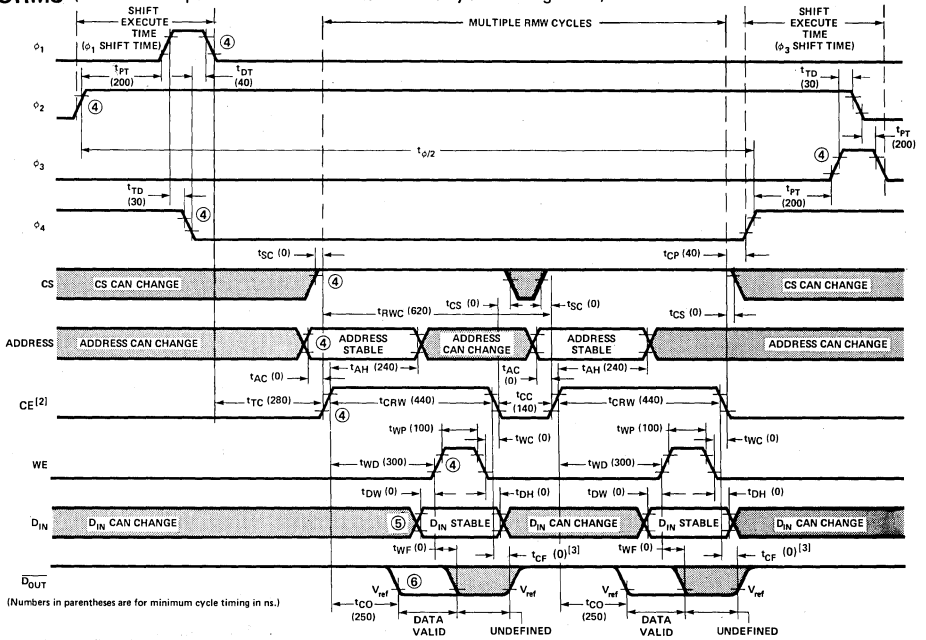
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	READ-MODIFY-WRITE Cycle Time	620		ns	
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	t_T = 40ns
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	t_{T1} = 20ns
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$		10,000	ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	
t_{T1}	Transition Times for Inputs Other Than $\phi_1 \ldots \phi_4$		100	ns	
t_{TC}	ϕ_1 or ϕ_3 Off to CE On	280		ns	
t_{SC}	CS to CE Set-Up Time	0		ns	
t_{AC}	Address to CE Set-Up Time	0		ns	
t_{AH}	Address Hold Time	240		ns	
t_{CS}	CE to CS Hold Time	0		ns	
t_{CC}	CE Off Time	140		ns	
t_{CP}	CE Off to ϕ_2 or ϕ_4 On	40		ns	
t_{CRW}	CE On Time	440[1]		ns	
t_{CO}	CE On to $\overline{D}_{OUT}$ Valid	250		ns	
t_{DW}	D_{IN} to WE Set-Up Time	0		ns	
t_{WP}	WE Pulse Width	100[1]		ns	
t_{WC}	WE Off to CE Off	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WD}	CE On to WE On	300[1]		ns	
t_{WF}	WE to $\overline{D}_{OUT}$ Undefined	0		ns	

$\overline{D}_{OUT}$ TEST LOAD



Note: 1. The minimum t_{WD} and t_{WP} times with appropriate transitions do not necessarily add up to the minimum t_{CRW}. This allows the user flexibility in setting the WE Pulse Width edges without affecting either t_{CRW} or the READ-MODIFY-WRITE Cycle Time, t_{RWC}.

WAVEFORMS (Numbers in parentheses are for minimum cycle timing in ns)



Notes: 2. When CE is off, the 2416 output level is determined by the external output termination.
3. The parameter t_{CF} is the same as in the Shift-Read-Shift Cycle on page 4.
4. +2.0V and V_{DD}-2.0V are the reference low and high level respectively for measuring the timing of $\phi_1 \ldots \phi_4$, CE, CS, WE, and addresses.
5. +1.5V and +3.0V are the reference low and high level respectively for measuring the timing of D_{IN}.
6. +0.8V is the reference level for measuring the timing of $\overline{D}_{OUT}$.

A.C. Characteristics

CAPACITANCE[1] $T_A = 25°C$

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Address, D_{IN}, CS, CE, WE Capacitance	4	6	pF	$V_{IN} = V_{SS}$
C_{OUT}	$\overline{D}_{OUT}$ Capacitance	3	5	pF	$V_{OUT} = V_{SS}$
$C_{\phi1}$[1], $C_{\phi3}$[2]	ϕ_1, ϕ_3 Input Capacitance	350	500	pF	$V_\phi = V_{SS}$
$C_{\phi2}$[1], $C_{\phi4}$[2]	ϕ_2, ϕ_4 Input Capacitance	480	700	pF	$V_\phi = V_{SS}$
$C_{\phi1-\phi2}$	Clock ϕ_1 To Clock ϕ_2 Capacitance	120	175	pF	$V_\phi = V_{SS}$
$C_{\phi1-\phi4}$	Clock ϕ_1 To Clock ϕ_4 Capacitance	150	200	pF	$V_\phi = V_{SS}$
$C_{\phi3-\phi2}$	Clock ϕ_3 To Clock ϕ_2 Capacitance	150	200	pF	$V_\phi = V_{SS}$
$C_{\phi3-\phi4}$	Clock ϕ_3 To Clock ϕ_4 Capacitance	120	175	pF	$V_\phi = V_{SS}$

Notes: 1. This parameter is periodically sampled and is not 100% tested.
2. The $C_{\phi1}$ .... $C_{\phi4}$ input clock capacitance includes the clock to clock capacitance. The equivalent input capacitance is given below.

SERIAL MEMORIES

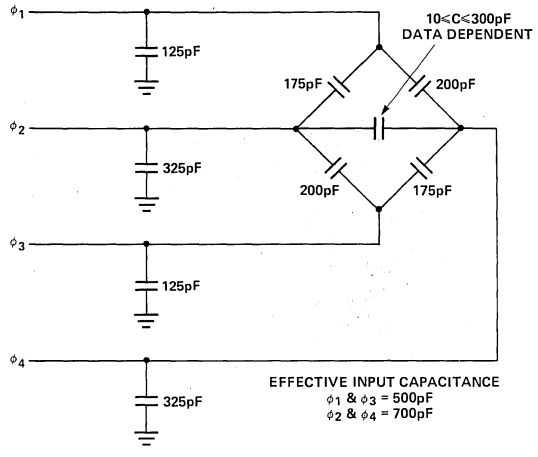
Four-Phase Clock Inputs

The four-phase clock inputs are internally connected to long electrodes used for several thin-oxide gates, resulting in high capacitance to the substrate on the clock inputs. In addition, considerable cross-coupling between adjacent clock exists due to the overlapping structure of the electrodes. The figure to the right shows the circuit equivalent of the clock inputs, indicating maximum capacitance values.

The equivalent circuit suggests two opposed clock driver requirements:

1. Ability to drive high-capacitance loads quickly.
2. Ability to suppress cross-coupled current transients.

The first requirement could ordinarily be met rather easily, if it weren't for the fact that the cross-coupled current, I, is proportional to the rate of change of the voltage, i.e., $I = C\frac{dv}{dt}$. For the quiescent driver to hold the coupled voltage to a minimum, the driver must have very low output impedance. However, when this driver becomes active the low output impedance increases the slope of the transitions which in turn increases coupling currents to the other drivers. This suggests that a driver have a controlled output transition time and a low output impedance characteristic in the quiescent state (high or low level). The Intel® 5244 meets these requirements.



5244 — CCD Clock Driver

The Intel® 5244 is a CMOS implemented fully TTL input compatible high voltage MOS driver, designed especially for the four phase clock inputs of the 2416. The device features very low DC power dissipation from a single +12V supply with output characteristics directly compatible with the 2416 clock input requirements.

The 5244 uses internal circuitry to control the cross-coupled voltage transients between the clock phases generated by the 2416. This internal circuitry limits the transition time to a specified range so that excessively fast transitions (<30ns) do not occur on the clock line. The entire operation is transparent to the user.

The 5244 is designed to drive four 2416s, but can drive fewer devices when loaded with additional capacitance to prevent a speedup in the transition times. Additional information on this and other aspects of the 5244 can be found on the 5244 data sheet.

Application Information

The Intel® 2416 is a charge coupled device (CCD) containing 16,384 bits of dynamic shift register storage available in a standard 18 pin plastic package. To minimize latency time (access time to any given bit in the device), the 2416 has been organized as 64 registers containing 256 bits each and, therefore, any bit can be accessed with a maximum of 255 shift operations. Since the minimum shift cycle requires 750 ns, the maximum latency time for the 2416 is less than 200μsec.

Access to the 64 recirculating registers is performed in a random access mode. A six bit address selects one of the 64 registers for read, write, or read/modify/write operations. These random access operations are performed between shift operations, and can be performed in any number or sequence as long as the basic shift frequency is maintained.

Because of substrate leakage currents the charge coupled storage mechanism is dynamic in nature. To satisfy the refresh requirements of the 2416, one shift operation must be performed every ten microseconds. A shift operation is completed on the falling edge of clock phase ϕ_1 or ϕ_3 and random access cycles may occur only between (1) the falling edge of ϕ_1 and the rising edge of ϕ_4 or (2) the falling edge of ϕ_3 and the rising edge of ϕ_2. This refresh requirement limits the number of random access cycles between successive shift operations to a maximum of 16.

Random access operations are performed in a manner which is very similar to any random access memory (RAM). All random access cycles are initiated with the rising edge and terminated with the falling edge of CE (Chip Enable). Read operations are performed when WE (Write Enable) remains low throughout a CE cycle. Data is strobed into the memory whenever WE is strobed high during a CE cycle as illustrated in the appropriate timing diagrams. CS (Chip Select) controls only the input and output circuits and is only effective when CE is high.

Typical Current Transients vs. Time

The oscilloscope photos in Figures 1 and 2 show typical I_{DD} current transients during shift and I/O cycles. The typical I_{BB} current during a shift cycle is shown in Figure 3.

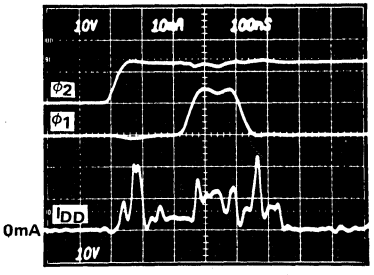


Figure 1. I_{DD} transient current during shift cycles.
I_{DD} scale: 10mA/div.

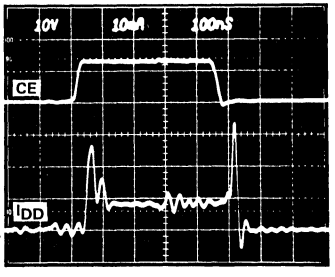


Figure 2. I_{DD} transient current during I/O cycles.
I_{DD} scale: 10mA/div.

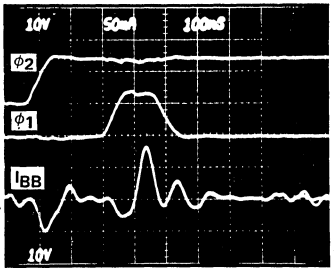
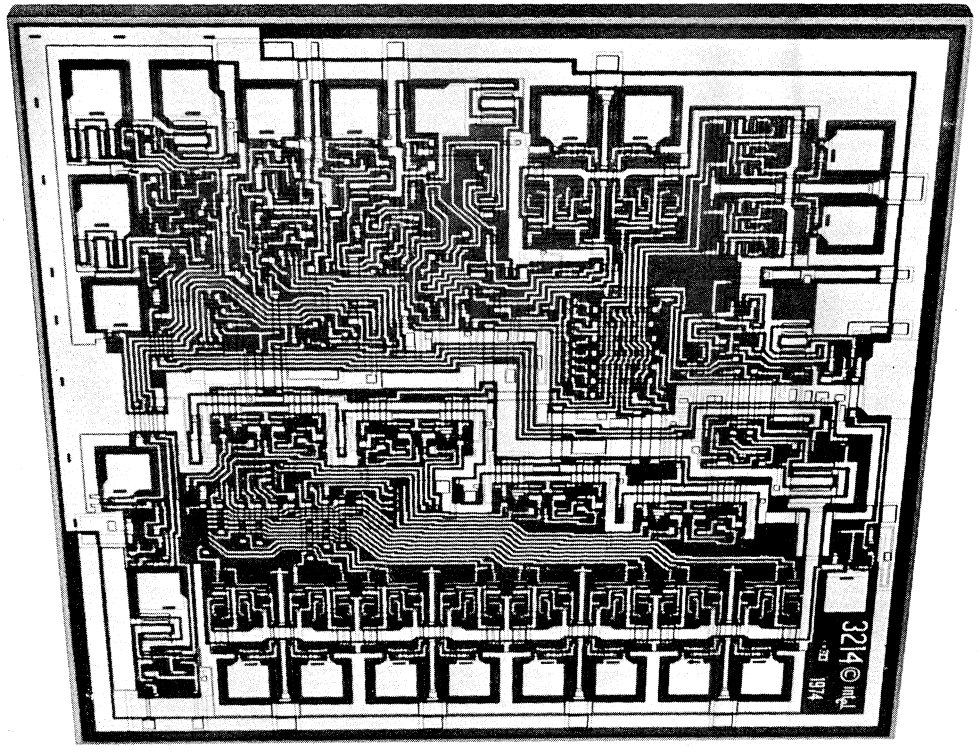


Figure 3. I_{BB} transient current during a shift cycle.
I_{BB} scale: 50mA/div.

5

MEMORY SUPPORT CIRCUITS



MEMORY SUPPORT CIRCUITS

	Type	Description	Electrical Characteristics Over Temperature		Supplies [V]	Page No.
			Input to Output Delay Maximum	Power Dissipation[1] Maximum		
SCHOTTKY BIPOLAR	3205	1 of 8 Binary Decoder	18ns	350mW	+5	5-3
	3207A	Quad Bipolar to MOS Level Shifter and Driver	25ns	900mW	+5,+16,+19	5-7
	3207A-1	Quad Bipolar to MOS Level Shifter and Driver	25ns	1040mW	+5,+19,+22	5-11
	3208A	Hex Sense Amp for MOS Memories	20ns	600mW	+5	5-13
	3222	4K Dynamic RAM Refresh Controller	—	600mW	+5	5-19
	3232	4K Dynamic RAM Address Multiplexer and Refresh Counter	20ns	675mW	+5	5-25
	3242	16K Dynamic RAM Address Multiplexer and Refresh Counter	20ns	—	+5	5-29
	3245	Quad TTL to MOS Driver for 4K RAMs	32ns	388mW	+12,+5	5-30
	3246	Quad ECL to MOS Driver for 4K RAMs	30ns	186mW	-5.2,+5,+12	5-34
	3404	High Speed 6-Bit Latch	12ns	375mW	+5	5-3
	3408A	Hex Sense Amp and Latch for MOS Memories	25ns	625mW	+5	5-13
CMOS	5234	Quad CMOS to MOS Driver for 4K RAMs	20ns	120mW	12	5-38
	5235	Quad Low Power TTL to MOS Driver for 4K RAMs	125ns	240mW	12	5-42
	5235-1	High Speed Quad Low Power TTL to MOS Driver for 4K RAMs	95ns	240mW	12	5-42
	5244	Quad CCD Driver	90ns	1260mW	12	5-46

Note 1: Power Dissipation calculated with maximum power supply current and nominal supply voltages.

3205 HIGH SPEED 1 OUT OF 8 BINARY DECODER
3404 HIGH SPEED 6-BIT LATCH

- **18ns Max. Delay Over 0°C to 75°C Temperature: 3205**
- **12ns Max. Data to Output Delay Over 0°C to 75°C Temperature: 3404**
- **Directly Compatible With DTL and TTL Logic Circuits**
- **Low Input Load Current: .25mA Max., 1/6 Standard TTL Input Load**
- **Minimum Line Reflection: Low Voltage Diode Input Clamp**
- **Outputs Sink 10mA Min.**
- **16-Pin Dual In-Line Package**
- **Simple Expansion: Enable Inputs**

3205

The 3205 decoder can be used for expansion of systems which utilize memory components with active low chip select input. When the 3205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 3205 allow easy memory expansion. For very large memory systems, 3205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

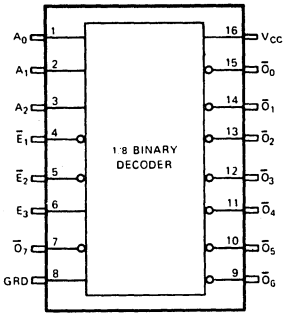
3404

The Intel 3404 contains six high speed latches organized as independent 4-bit and 2-bit latches. They are designed for use as memory data registers, address registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low".

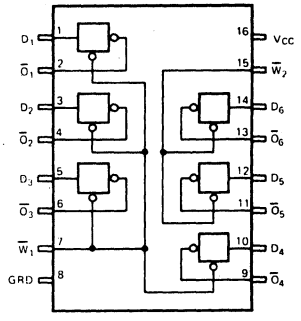
The Intel 3404 is packaged in a standard 16-pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION

3205



3404



Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		125 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

3205, 3404

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	V_{CC} = 5.25V, V_F = 0.45V
I_R	INPUT LEAKAGE CURRENT		10	µA	V_{CC} = 5.25V, V_R = 5.25V
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	V_{CC} = 4.75V, I_C = −5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} = 4.75V, I_{OL} = 10.0 mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	V_{CC} = 4.75V, I_{OH} = −1.5 mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	V_{CC} = 5.0V, V_{OUT} = 0V
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	V_{CC} = 5.0V, I_{OX} = 40 mA

3205 ONLY

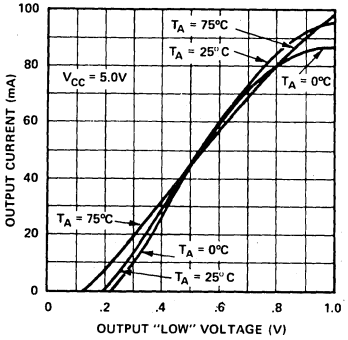
I_{CC}	POWER SUPPLY CURRENT		70	mA	V_{CC} = 5.25V

3404 ONLY

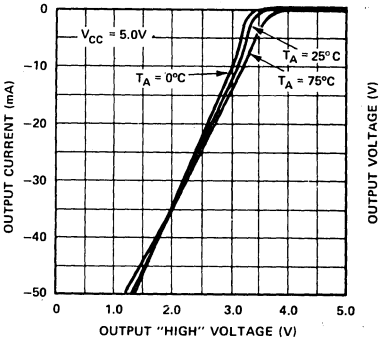
I_{CC}	POWER SUPPLY CURRENT		75	mA	V_{CC} =5.25V
I_{FW1}	WRITE ENABLE LOAD CURRENT PIN 7		−1.00	mA	V_{CC}=5.25V, V_W=0.45V
I_{FW2}	WRITE ENABLE LOAD CURRENT PIN 15		−0.50	mA	V_{CC}=5.25V, V_W=0.45V
I_{RW}	WRITE ENABLE LEAKAGE CURRENT		10	µA	V_R=5.25V

Typical Characteristics

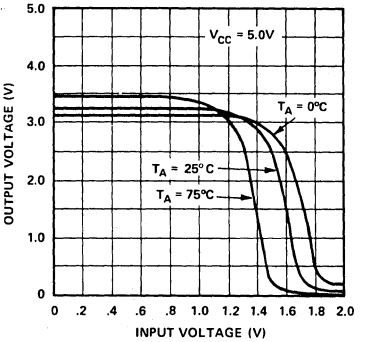
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



DATA TRANSFER FUNCTION



3205 - HIGH SPEED 1 OUT OF 8 BINARY DECODER

Switching Characteristics

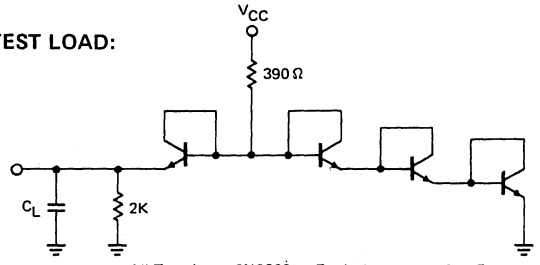
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

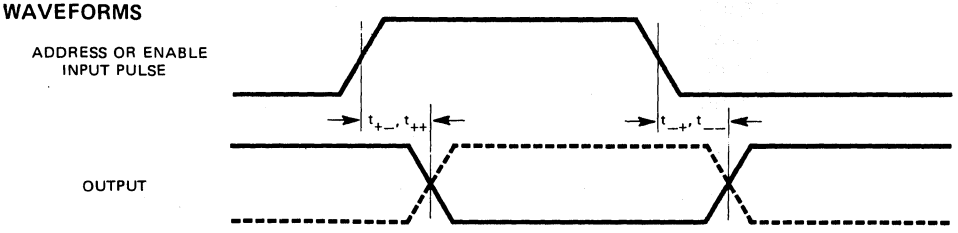
Measurements are made at 1.5V

TEST LOAD:



All Transistors 2N2369 or Equivalent. C_L = 30 pF

TEST WAVEFORMS



A.C. Characteristics

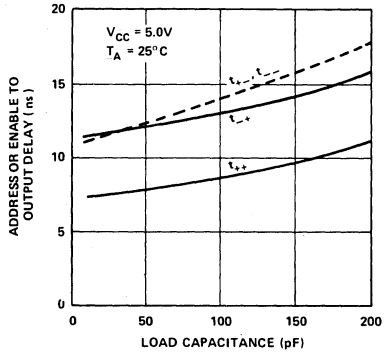
T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} [1]	INPUT CAPACITANCE	P3205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C3205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

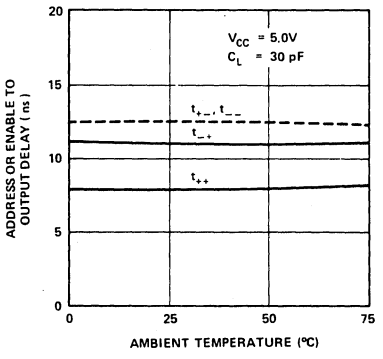
1. This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

ADDRESS OR ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



MEMORY SUPPORT

3404 - 6-BIT LATCH
Switching Characteristics

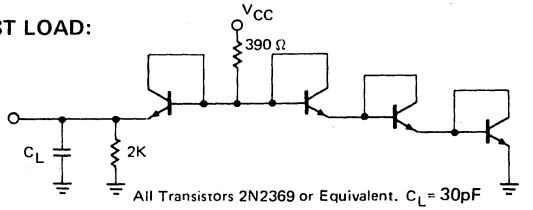
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

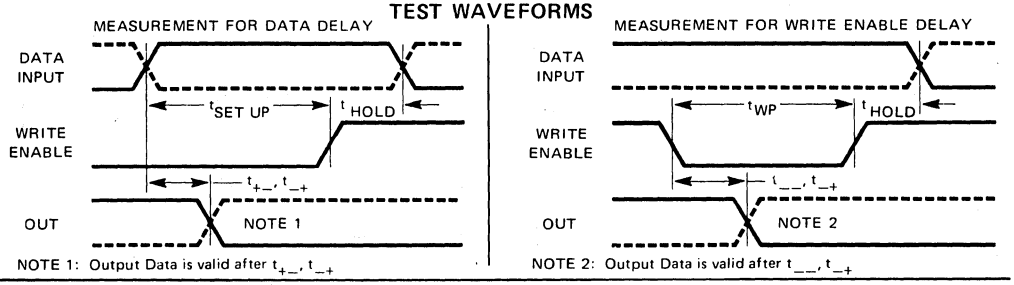
Input rise and fall times: 5 nsec between 1V and 2V

Measurements are made at 1.5V

TEST LOAD:



TEST WAVEFORMS



NOTE 1: Output Data is valid after t_{+-}, t_{-+}

NOTE 2: Output Data is valid after t_{--}, t_{-+}

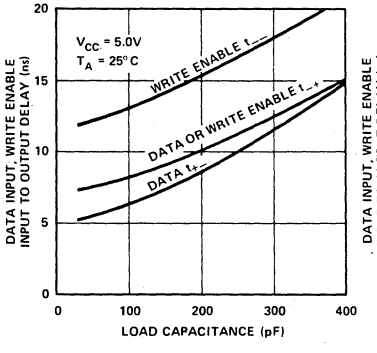
A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{+-},t_{-+}	DATA TO OUTPUT DELAY				12	ns	
t_{--},t_{-+}	WRITE ENABLE TO OUTPUT DELAY				17	ns	
$t_{SET\ UP}$	TIME DATA MUST BE PRESENT BEFORE RISING EDGE OF WRITE ENABLE		12			ns	
t_{HOLD}	TIME DATA MUST REMAIN AFTER RISING EDGE OF WRITE ENABLE		8			ns	
t_{WP}	WRITE ENABLE PULSE WIDTH		15			ns	
C_{IND}(3)	DATA INPUT CAPACITANCE	P3404		4		pF	f = 1 MHz, V_{CC} = 0V
		C3404		5		pF	V_{BIAS} = 2.0V, T_A = 25°C
C_{INW}(3)	WRITE ENABLE CAPACITANCE	P3404		7		pF	f = 1 MHz, V_{CC} = 0V
		C3404		8		pF	V_{BIAS} = 2.0V, T_A = 25°C

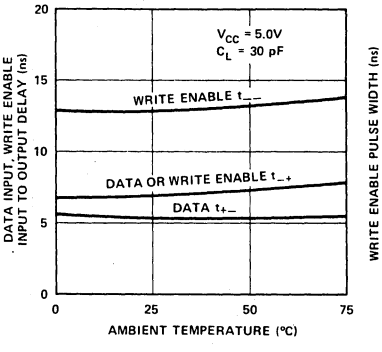
NOTE 3: This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

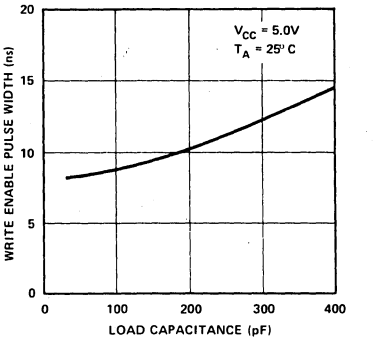
DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. LOAD CAPACITANCE



MEMORY SUPPORT

QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

- **High Speed, 45 nsec Max.-- Delay + Transition Time Over Temperature with 200 pF Load**
- **TTL & DTL Compatible Inputs**
- **1103 and 1103A Memory Compatible at Output**
- **Simplifies Design -- Replaces Discrete Components**
- **Easy to Use -- Operates from Standard Bipolar and MOS Supplies**
- **Minimum Line Reflection -- Input and Output Clamp Diodes**
- **High Input Breakdown Voltage-- 19 Volts**
- **CerDIP Package -- 16 Pin DIP**

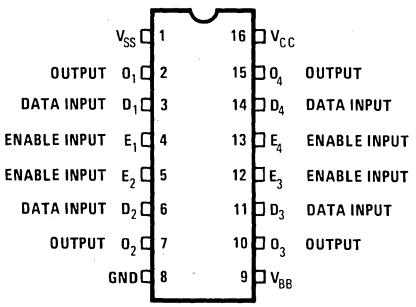
The 3207A is a Quad Bipolar-to-MOS level shifter and driver which accepts TTL and DTL input signals, and provides high output current and voltage suitable for driving MOS circuits. It is particularly suitable for driving the 1103 and 1103A memory chips. The circuit operates from a 5 volt TTL power supply, and V_{SS} and V_{BB} power supplies from the 1103 and 1103A.

The device features two common enable inputs per pair of devices which permits some logic to be done at their inputs, such as cenable and precharge decoding for the 1103 and 1103A.

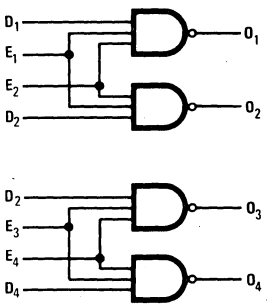
For the TTL inputs a logic "1" is V_{IH} and a logic "0" is V_{IL}. The 3207A outputs correspond to a logic "1" as V_{OL} and a logic "0" as V_{OH} for driving MOS inputs.

The 3207A is packaged in a hermetically sealed 16 pin ceramic dual-in-line package. The device performance is specified over the same temperature range as the 1103 and 1103A, i.e. from 0°C to +70°C.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature..... −65°C to +160°C
All Input Voltages and V_{SS}..... −1.0 to +21V
Supply Voltage V_{CC} ..... −1.0 to +7V
All Outputs and Supply Voltage
V_{BB} with respect to GND ..... −1.0 to +25V
Power Dissipation at 25°C..... 2 Watts (1)

*COMMENT
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) Refer to the graph of Junction Temperature versus Total Power Dissipation on page 5-10 for other temperatures.

D. C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 16V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	$V_D = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{FE}	ENABLE INPUT LOAD CURRENT		−0.50	mA	$V_E = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	$V_D = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	$V_E = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{OL}	OUTPUT "LOW" VOLTAGE		.8 .7 .6	V(0°C) V(25°C) V(70°C)	$I_{OL} = 500\mu A$, $V_{CC} = 4.75V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	$V_{SS} - .7$ $V_{SS} - .6$ $V_{SS} - .5$		V(0°C) V(25°C) V(70°C)	$I_{OH} = -500\mu A$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 0.85V
V_{OH} (MAX.)			$V_{SS} + 1.0$	V	$I_{OH} = 5mA$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$
I_{OL}	OUTPUT SINK CURRENT	100		mA	$V_O = 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$, $V_E = V_D = 2.0V$
I_{OH}	OUTPUT SOURCE CURRENT	−100		mA	$V_O = V_{SS} - 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$ $V_{BB} = 19V$, $V_E = V_D = 0.85V$
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
C_{IN}	INPUT CAPACITANCE	8(Typical)		pF	$V_{BIAS} = 2.0V$, $V_{CC} = 0V$

POWER SUPPLY CURRENT DRAIN:
All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		21	mA	
P_{TOTAL}	Total Power Dissipation		900	mW	

All Outputs "High"

I_{CC}	Current from V_{CC}		33	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Grounded
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		3	mA	
P_{TOTAL}	Total Power Dissipation		250	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

I_{CC}	Current from V_{CC}		0	mA	$V_{CC} = 0V$, $V_{SS} = 16.8V$, $V_{BB} = 16.8V$
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		250	μA	
P_{TOTAL}	Total Power Dissipation		10	mW	

MEMORY SUPPORT

Switching Characteristics

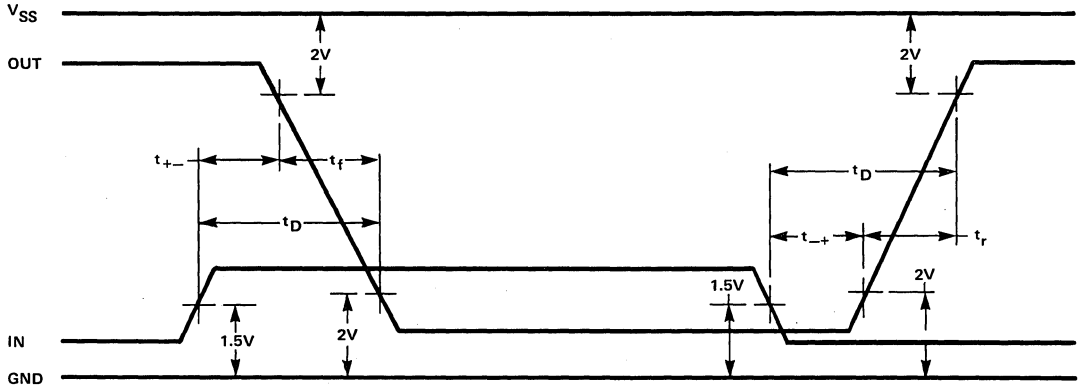
A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 16V ±5%, V_{BB} = V_{SS} +3 to 4V, f = 2 MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		C_L = 100 pF		C_L = 200 pF		DELAY DIFFERENTIAL[1] C_L = 200 pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	20	10	30	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

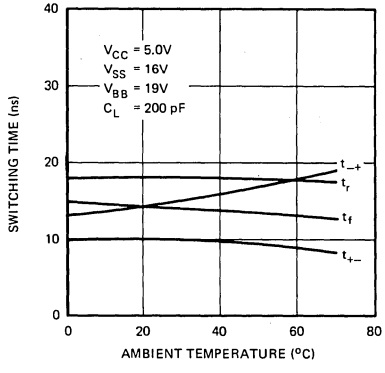
(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

Waveforms

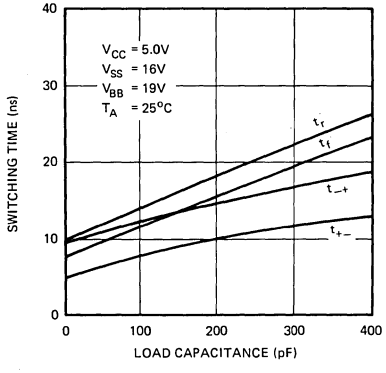


Typical Characteristics

SWITCHING TIME VS. AMBIENT TEMPERATURE



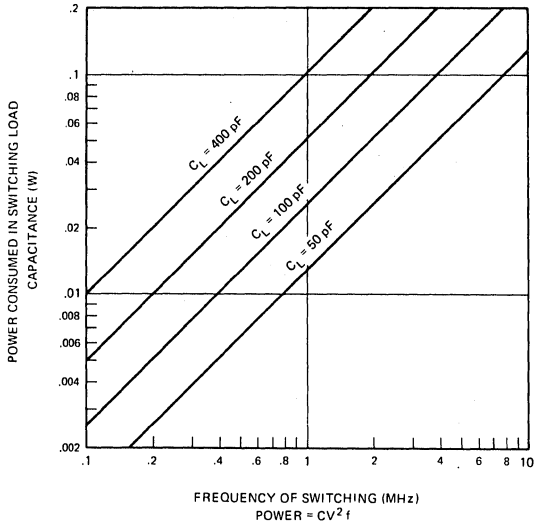
SWITCHING TIME VS. LOAD CAPACITANCE



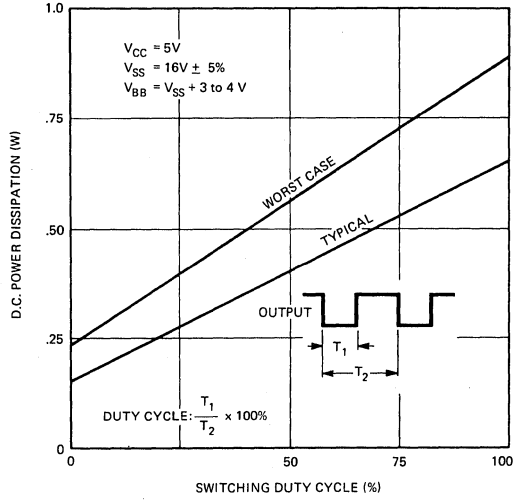
MEMORY SUPPORT

Power and Switching Characteristics

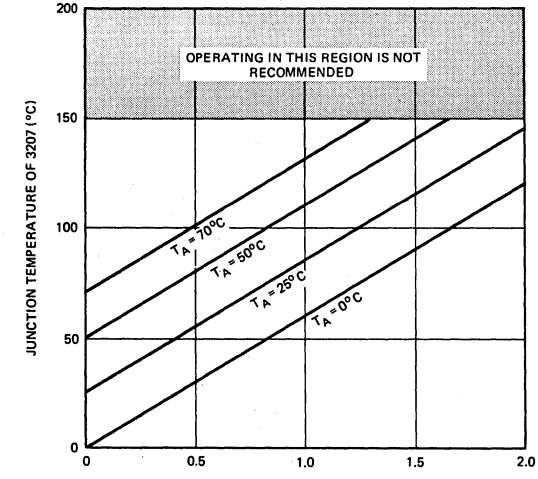
POWER CONSUMED IN CHARGING AND DISCHARGING LOAD CAPACITANCE OVER 0V TO 16V INTERVAL



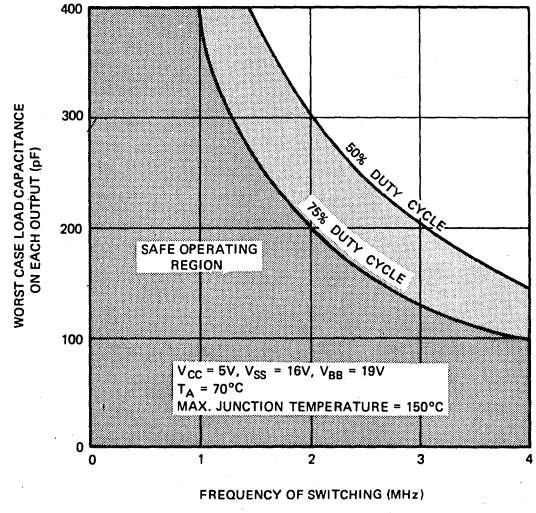
NO LOAD D.C. POWER DISSIPATION VS. OPERATING DUTY CYCLE



JUNCTION TEMPERATURE VS. TOTAL POWER DISSIPATION OF THE CIRCUIT



WORST CASELOAD CAPACITANCE ON EACH OUTPUT VS. FREQUENCY OF SWITCHING



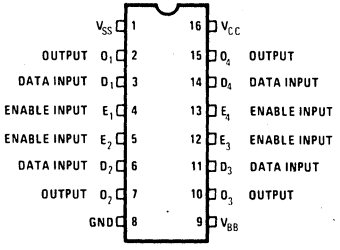
MEMORY SUPPORT

QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

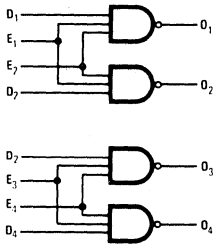
- **Power Supply Voltage Compatible with the High Voltage 1103-1**
- **1103-1 Memory Compatible at Output**

The Intel 3207A-1 is the high voltage version of the standard 3207A, and is compatible with the 1103-1. The 3207A-1 has all the same features as the standard 3207A. The absolute maximum ratings and pin configuration are repeated below for convenience, while the DC and AC characteristics appear below and on the next page.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to +55°C
Storage Temperature . . . . . –65° C to +160°C
All Input Voltages . . . . . –1.0 to +21 Volts
Supply Voltage V_{CC} . . . . . –1.0 to +7.0 Volts
All Outputs and Supply Voltages V_{BB} and V_{SS} with respect to GND . . . . . –1.0 to +25 Volts
Power Dissipation at 25°C . . . . . 2 Watts

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MEMORY SUPPORT

D. C. Characteristics $T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
I_{FD}	DATA INPUT LOAD CURRENT		–0.25	mA	V_D = .45V, V_{CC} = 5.25V, All Other Inputs at 5.25V, V_{SS} = 19V, V_{BB} = 23V
I_{FE}	ENABLE INPUT LOAD CURRENT		–0.50	mA	V_E = .45V, V_{CC} = 5.25V, All Other Inputs at 5.25V, V_{SS} = 19V, V_{BB} = 23V
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	V_D = 19V, V_{CC} = 5.0V, All Other Inputs Grounded, V_{SS} = 19V, V_{BB} = 23V
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	V_E = 19V, V_{CC} = 5.0V, All Other Inputs Grounded, V_{SS} = 19V, V_{BB} = 23V
V_{OL}	OUTPUT "LOW" VOLTAGE		0.8 0.7 0.6	V(0°C) V(25°C) V(55°C)	I_{OL} = 500μA, V_{CC} = 4.75V V_{SS} = 19V, V_{BB} = 23V All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	V_{SS} –0.7 V_{SS} –0.6 V_{SS} –0.5		V(0°C) V(25°C) V(55°C)	I_{OH} = –500μA, V_{CC} = 5.0V V_{SS} = 19V, V_{BB} = 23V All Inputs at 0.85V
V_{OH} (MAX.)			V_{SS} + 1.0	V	I_{OH} = 5mA, V_{CC} = 5.0V V_{SS} = 19V, V_{BB} = 23V
I_{OL}	OUTPUT SINK CURRENT	100		mA	V_O = 4V, V_{CC} = 5.0V, V_{SS} = 19V, V_{BB} = 23V, V_E = V_D = 2.0V
I_{OH}	OUTPUT SOURCE CURRENT	–100		mA	V_O = V_{SS} –4V, V_{CC} = 5.0V, V_{SS} = 19V V_{BB} = 23V, V_E = V_D = 0.85V
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	V_{CC} = 5.0V, V_{SS} = 19V, V_{BB} = 23V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V, V_{SS} = 19V, V_{BB} = 23V
C_{IN}	INPUT CAPACITANCE		8(Typical)	pF	V_{BIAS} = 2.0V, V_{CC} = 0V

D.C. Characteristics (Continued) $T_A = 0°C$ to $+55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

POWER SUPPLY CURRENT DRAIN:
All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		25	mA	
P_{TOTAL}	Total Power Dissipation		1040	mW	

All Outputs "High"

I_{CC}	Current from V_{CC}		33	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Grounded
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		5	mA	
P_{TOTAL}	Total Power Dissipation		297	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

I_{CC}	Current from V_{CC}		0	mA	$V_{CC} = 0V$, $V_{SS} = 20V$, $V_{BB} = 20V$
I_{SS}	Current from V_{SS}		500	μA	
I_{BB}	Current from V_{BB}		500	μA	
P_{TOTAL}	Total Power Dissipation		15	mW	

MEMORY SUPPORT

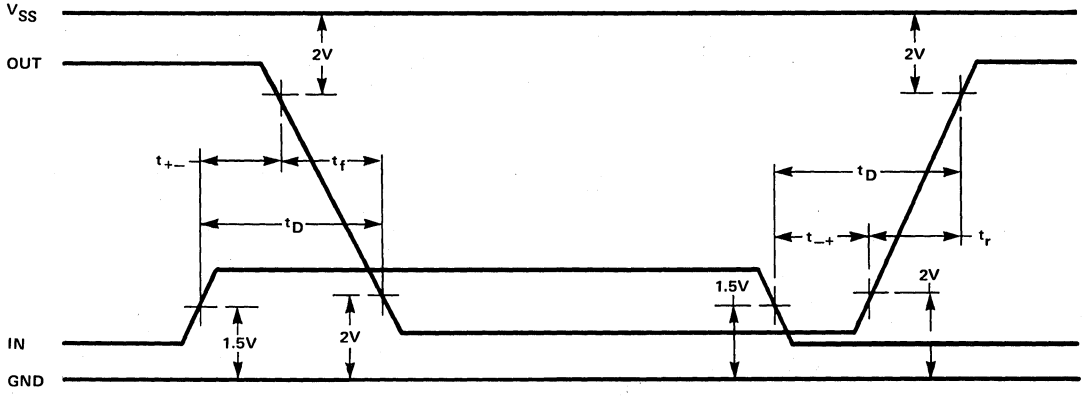
A.C. Characteristics

$T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} = V_{SS} + 3$ to $4V$, $f = 2$ MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		$C_L = 100$ pF		$C_L = 200$ pF		DELAY DIFFERENTIAL[1] $C_L = 200$ pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	25	10	35	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

Waveforms



HEX BIPOLAR SENSE AMPLIFIERS FOR MOS CIRCUITS

3208A HEX SENSE AMPLIFIER
3408A HEX SENSE AMPLIFIER WITH LATCHES

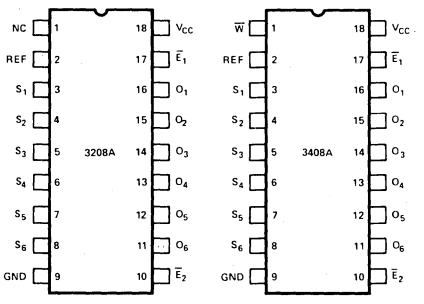
- **High Speed—20 nsec. max.**
- **Wire-OR Capability— Open Collector Output..3208A Three-State Output 3408A**
- **Single 5 V Power Supply**
- **Input Level Compatible with 1103 Output**
- **Two Enable Inputs**
- **Minimum Line Reflection .... Low Voltage Diode Input Clamp**
- **Plastic 18 Pin Dual In-Line Package**
- **Schottky TTL**

The Intel 3208A is a high speed hex sense amplifier designed to sense the output signals of the 1103 memory. The device features two separate enable inputs each controlling the output state of three sense amplifiers, and a common voltage reference input. OR-tie capability is available with the 3208A open collector TTL compatible output.

The 3408A is a hex sense amplifier with a latch circuit connected to each amplifier. The sensed data may be stored in the latches through application of a write pulse. The 3408A has three-state TTL outputs, hence in the non-enabled state the outputs float allowing wire-OR memory expansion. The latches may be bypassed by grounding the write input pin. Under this condition, the 3408A functions as a hex sense amplifier.

The 3208A and 3408A operate from a single +5 volt power supply. Device performance is specified over the complete ambient temperature range of 0°C to 70°C and over a V_{CC} supply voltage range of 5 volts ±5%. The 3208A and 3408A are packaged in an 18 pin plastic dual in-line package.

PIN CONFIGURATIONS

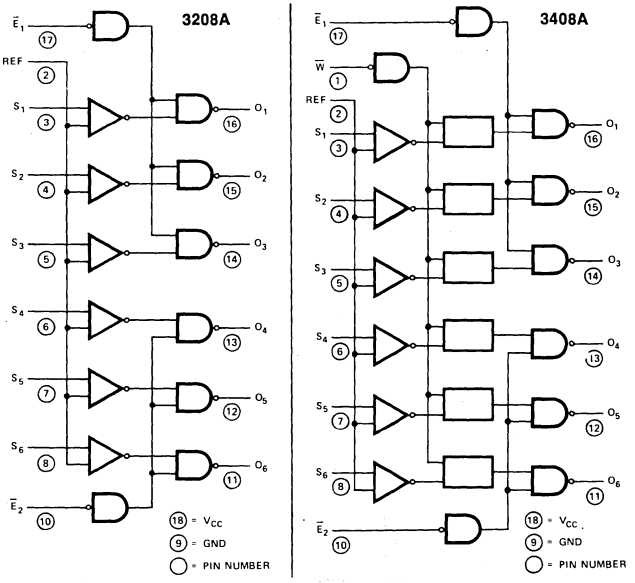


3208A 3408A

PIN NAMES

$S_1, S_2, S_3, S_4, S_5, S_6$	SENSE AMP INPUTS
$\bar{E}_1, \bar{E}_2$	ENABLE INPUTS
REF	REFERENCE INPUT
$O_1, O_2, O_3, O_4, O_5, O_6$	OUTPUTS (Non-inverting)
$\bar{W}$	WRITE INPUT (3408A only)

BLOCK DIAGRAMS



Absolute Maximum Ratings*

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +160°C
All Outputs or Supply Voltage	−0.5 to +7 Volts
All TTL Input Voltages	−1 to +5.5 Volts
All Sense Input Voltages	−1 to +1 Volt
Output Currents Total	300 mA
Input Current	125 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at this or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics for 3208A $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
I_{FE}	INPUT LOAD CURRENT ON ENABLE INPUT			−0.25	mA	$V_{CC} = 5.25V$ $V_F = 0.45V$
I_{RE}	INPUT LEAKAGE CURRENT ON ENABLE INPUT			20	μA	$V_{CC} = 4.75V$ $V_R = 5.25V$
V_{IH}	INPUT "HIGH" VOLTAGE ON ENABLE INPUT	2.0			V	$V_{CC} = 5.0V$
V_{IL}	INPUT "LOW" VOLTAGE ON ENABLE INPUT			0.85	V	$V_{CC} = 5.0V$
V_{OL}	OUTPUT "LOW" VOLTAGE			0.45	V	$V_{CC} = 4.75V$ $I_{OL} = 10mA$
I_{CEX}	OUTPUT LEAKAGE CURRENT			100	μA	$V_{CC} = 5.25V$ $V_{CEX} = 5.25V$
I_{REF}	INPUT CURRENT ON REFERENCE INPUT			−150	μA	$V_{CC} = 5.25V$ $V_{REF} = 100mV$
I_S	INPUT CURRENT ON SENSE AMP INPUT			−25	μA	$V_{CC} = 5.25V$ $V_S = 100mV$
V_{SH}	INPUT "HIGH" VOLTAGE FOR SENSE AMP INPUT	V_{REF}			mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{SL}	INPUT "LOW" VOLTAGE FOR SENSE AMP INPUT			$V_{REF} - 50$	mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{REF}	OPERATING RANGE OF REFERENCE VOLTAGE	100		200	mV	$V_{CC} = 4.75$ to $5.25V$
I_{CC}	POWER SUPPLY CURRENT			120	mA	$V_{CC} = 5.25V$
V_C	INPUT CLAMP VOLTAGE ON ALL INPUTS			−1.0	V	$V_{CC} = 4.75V$ $I_C = -5.0mA$
V_{SD}	SENSE INPUT CLAMP DIODE VOLTAGE			1.0	V	$V_{CC} = 5.0V$ $I_D = 5.0mA$

3208A TRUTH TABLE

INPUTS		OUTPUT
Sense Amp	Enable	
$<V_{REF} - 50mV$	L	L
$>V_{REF}$	L	H
X	H	H

X = Don't care

D. C. Characteristics for 3408A $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
I_{FE}	INPUT LOAD CURRENT ON ENABLE INPUT			−0.25	mA	$V_{CC} = 5.25V$ $V_F = 0.45V$
I_{RE}	INPUT LEAKAGE CURRENT ON ENABLE INPUT			20	μA	$V_{CC} = 4.75V$ $V_R = 5.25V$
I_{FW}	INPUT LOAD CURRENT ON WRITE INPUT			−0.25	mA	$V_{CC} = 5.25V$ $V_F = 0.45V$
I_{RW}	INPUT LEAKAGE CURRENT ON WRITE INPUT			20	μA	$V_{CC} = 4.75V$ $V_R = 5.25V$
V_{IH}	INPUT "HIGH" VOLTAGE ON ENABLE AND WRITE INPUT	2.0			V	$V_{CC} = 5.0V$
V_{IL}	INPUT "LOW" VOLTAGE ON ENABLE AND WRITE INPUT			0.85	V	$V_{CC} = 5.0V$
V_{OL}	OUTPUT "LOW" VOLTAGE			0.45	V	$V_{CC} = 4.75V$ $I_{OL} = 10mA$
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.4			V	$V_{CC} = 4.75V$ $I_{OH} = -1.5mA$
$\|I_O\|$	OUTPUT LEAKAGE CURRENT FOR HIGH IMPEDANCE STATE			100	μA	$V_{CC} = 5.25V$ $V_O = 0.45V/5.25V$
I_{SC}	OUTPUT SHORT CIRCUIT CURRENT	−40		−100	mA	$V_{CC} = 5.0V$ $V_O = 0V$
I_{REF}	INPUT CURRENT ON REFERENCE INPUT			−150	μA	$V_{CC} = 5.25V$ $V_{REF} = 100mV$
I_S	INPUT CURRENT ON SENSE INPUT			−25	μA	$V_{CC} = 5.25V$ $V_S = 100mV$
V_{SH}	INPUT "HIGH" VOLTAGE FOR SENSE AMP INPUT	V_{REF}			mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{SL}	INPUT "LOW" VOLTAGE FOR SENSE AMP INPUT			V_{REF} −60	mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{REF}	OPERATING RANGE OF REFERENCE VOLTAGE	100		200	mV	$V_{CC} = 4.75$ to $5.25V$
I_{CC}	POWER SUPPLY CURRENT			125	mA	$V_{CC} = 5.25V$
V_C	INPUT CLAMP VOLTAGE ON ALL INPUTS			−1.0	V	$V_{CC} = 4.75V$ $I_C = -5.0V$
V_{SD}	SENSE INPUT CLAMP DIODE VOLTAGE			1.0	V	$V_{CC} = 5.0V$ $I_D = 5.0mA$

3408A TRUTH TABLE

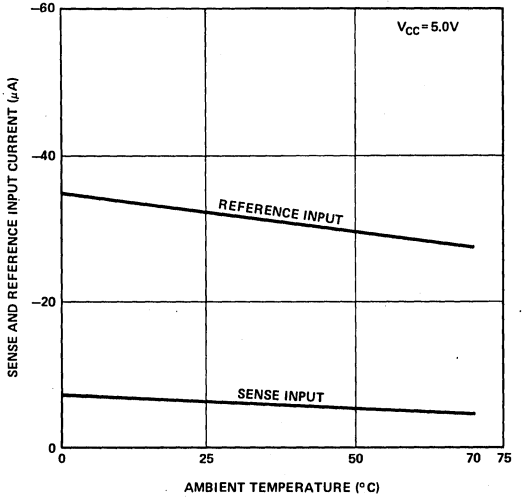
INPUTS			OUTPUT
Sense Amp	Enable	Write	
$< V_{REF}$ −60mV	L	L	L
$> V_{REF}$	L	L	H
X	L	H	Previous Data Stored
X	H	X	High Z*

X = Don't care
*The output of the 3408A is three-state, hence when not enabled the output is a high impedance.

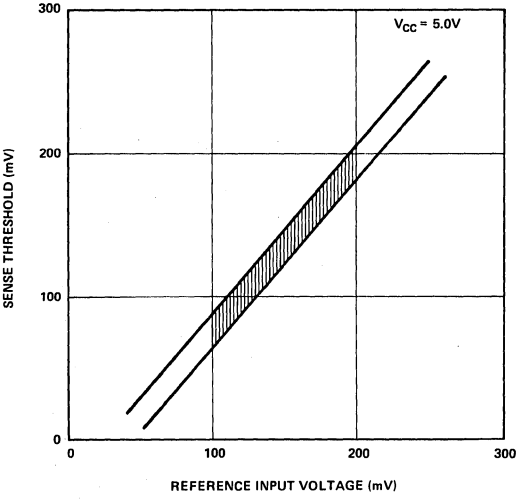
MEMORY SUPPORT

Typical D. C. Characteristics for 3208A/3408A

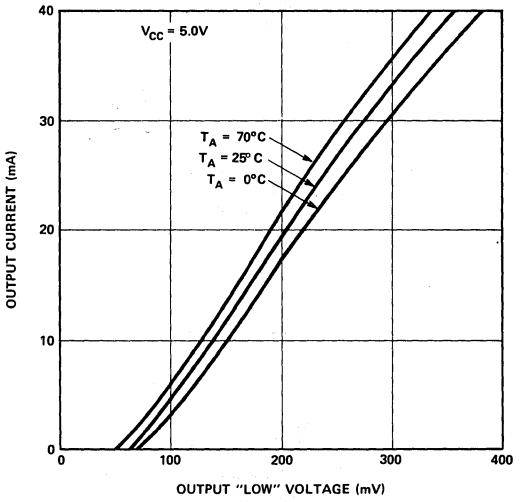
SENSE AND REFERENCE INPUT CURRENT VS. AMBIENT TEMPERATURE



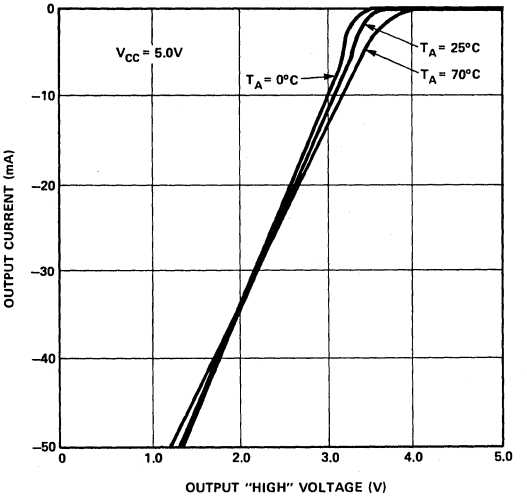
SENSE THRESHOLD VS. REFERENCE INPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

3208A

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{S-}	SENSE AMP INPUT TO OUTPUT DELAY			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E-}	ENABLE INPUT TO OUTPUT DELAY			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E+}				25		

3408A

t_{WP}	WRITE PULSE WIDTH	30			ns	D.C. LOAD = 10mA C_L = 30pF
t_{S-}	SENSE AMP INPUT TO OUTPUT DELAY			25	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E-}	ENABLE INPUT TO OUTPUT DELAY, LATCH STORES "LOW"			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E+}	ENABLE INPUT TO OUTPUT DELAY, LATCH STORES "HIGH"			25	ns	D.C. LOAD = 10mA C_L = 30 pF

Capacitance[1] $T_A = 25°C$, f = 1 MHz

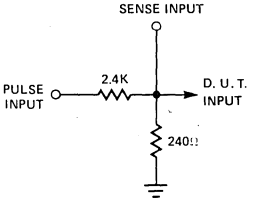
SYMBOL	TEST	LIMITS TYP.	LIMITS MAX.
C_O	V_{CC} = 0V, V_{BIAS} = 2.0V	8	12
C_{INE}	ENABLE INPUT V_{CC} = 0V, V_{BIAS} = 2.0V	6	10
C_{INS}	SENSE INPUT V_{CC} = 0V, V_{BIAS} = 0V	6	10

(1) This parameter is periodically sampled and is not 100% tested.

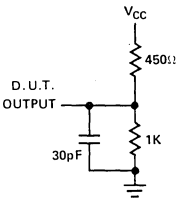
Switching Characteristics

CONDITIONS OF TEST

- Input Pulse amplitude: 2.5V for all TTL compatible inputs and 2.5V through a resistor network as shown below for sense input.
- Input Pulse rise and fall times: 5ns.
- Speed measurements are made at 1.5V for all TTL compatible inputs and outputs, and for sense input, see network and waveforms below. V_{REF} is set at 150mV.

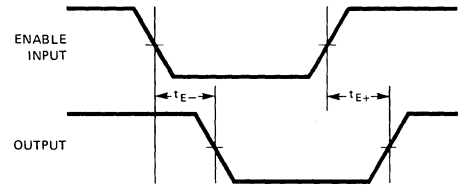


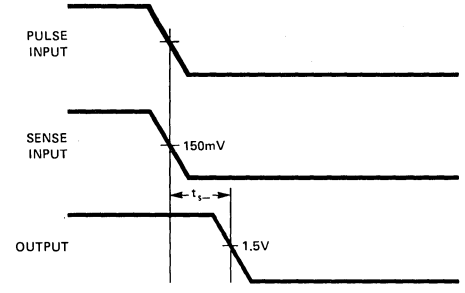
10mA TEST LOAD



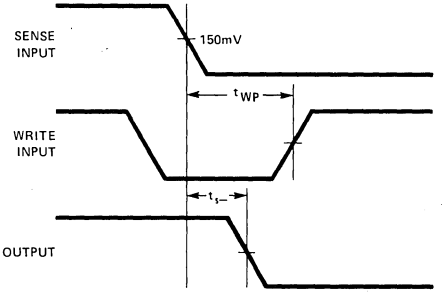
Waveforms

3208A/3408A





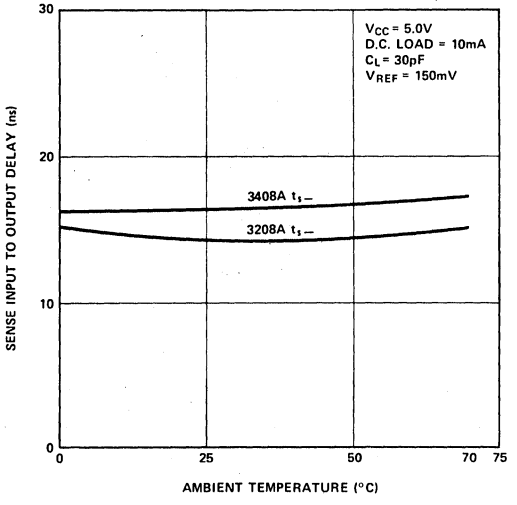
3408A ONLY



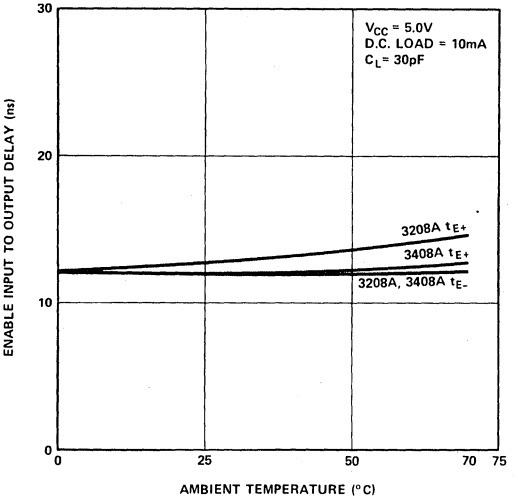
MEMORY SUPPORT

Typical A. C. Characteristics

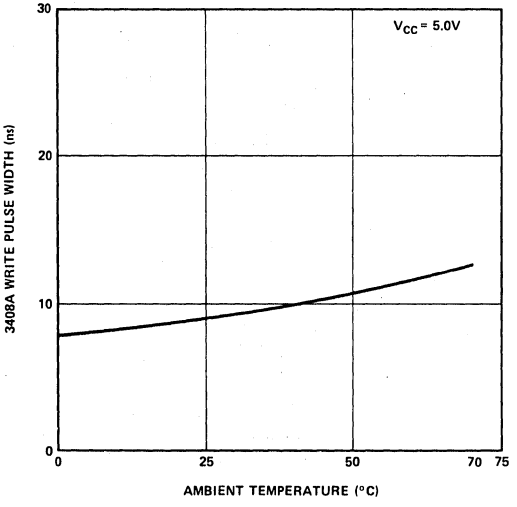
SENSE INPUT TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



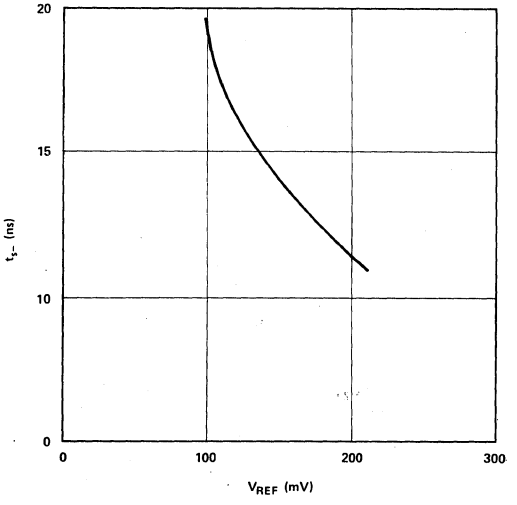
ENABLE INPUT TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



3408A WRITE PULSE WIDTH VS. AMBIENT TEMPERATURE



SENSE INPUT TO OUTPUT DELAY VS. REFERENCE INPUT VOLTAGE



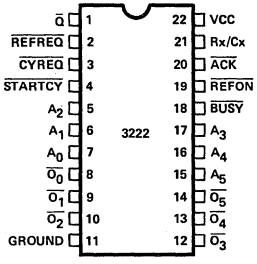
REFRESH CONTROLLER FOR 4K DYNAMIC RANDOM ACCESS MEMORIES

- **Ideal for use in 2107A, 2107B Systems**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 22-Pin DIP**
- **Adjustable Refresh Timing Oscillator**
- **6-Bit Address Multiplexer**
- **6-Bit Refresh Address Counter**
- **Refresh Cycle Controller**

The Intel® 3222 is a refresh controller for dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). The device contains an accurate refresh timer (whose frequency can be set by an external resistor and capacitor), plus all necessary control and I/O circuitry to provide for the refresh requirements of dynamic RAMs. The chip's high performance makes it especially suitable for use with high speed N-channel RAMs like the Intel® 2107B. The 3222 is well suited for asynchronous dynamic memory systems.

The 3222 operates from a single +5 volt power supply and is specified for operation over a 0°C to 75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process.

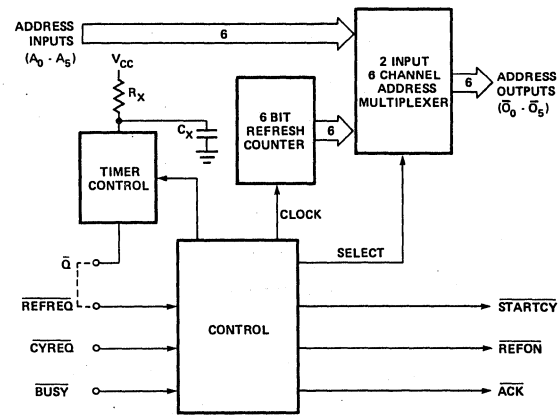
PIN CONFIGURATION



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	$\overline{O}_0$ - $\overline{O}_5$	ADDRESS OUTPUTS
$\overline{ACK}$	ACKNOWLEDGE OUTPUT	$\overline{Q}$	INTERNAL REFRESH REQUEST LATCH OUTPUT
$\overline{BUSY}$	BUSY INPUT	$\overline{REFON}$	REFRESH ON OUTPUT
$\overline{CYREQ}$	CYCLE REQUEST INPUT	$\overline{REFREQ}$	REFRESH REQUEST INPUT
		RxCx	RC TIE POINT
		$\overline{STARTCY}$	START CYCLE OUTPUT
		V_{CC}	+5V SUPPLY

BLOCK DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65° to +125°C
Storage Temperature . . . . . -65° to +160°C
All Input, Output or Supply Voltages . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA
Power Dissipation . . . . . 1 W

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FB}	Input Load Current $\overline{BUSY}$		0.40	1	mA	V_{IN} = 0.45V
I_{FO}	Input Load Current All Other Inputs		0.05	0.25	mA	V_{IN} = 0.45V
I_{RB}	Input Leakage Current $\overline{BUSY}$		<1	50	μA	V_{IN} = V_{CC}
I_{RO}	Input Leakage Current All Other Inputs		<1	20	μA	V_{IN} = 5.25V
V_{CLAMP}	Input Clamp Voltage		-0.76	-1	V	I_C = -5.0mA
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{CC}	Power Supply Current		91	120	mA	V_{CC} = 5.25V
I_{SC}	Output High Short Circuit Current		-48	-70	mA	V_{OUT} = 0V V_{CC} = 5.25V
V_{OL}	Output Low Voltage		0.32	0.45	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.6	3.1		V	I_{OH} = -1mA V_{CC} = 4.75V
V_{OH1}	Output High Voltage (All Other Outputs)	2.4	3.0		V	I_{OH} = -1mA V_{CC} = 4.75V

Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

Capacitance[2], T_A = 25°C

Symbol	Test	Limits (pF) Typ.	Max.	Conditions
C_{IN} (Address)	Input Capacitance	5	10	V_{bias} = 2.0V
C_{IN} ($\overline{CYREQ}$)	Input Capacitance	6	10	V_{CC} = 0V
C_{IN} ($\overline{BUSY}$)	Input Capacitance	20	30	f = 1MHz

Note 2: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C. Load = 1 TTL, C_L = 15pF.
Conditions of Test: Input pulse amplitude: 3V, Input rise and fall times: 5ns between 1V and 2V. Measurements are made at 1.5V.

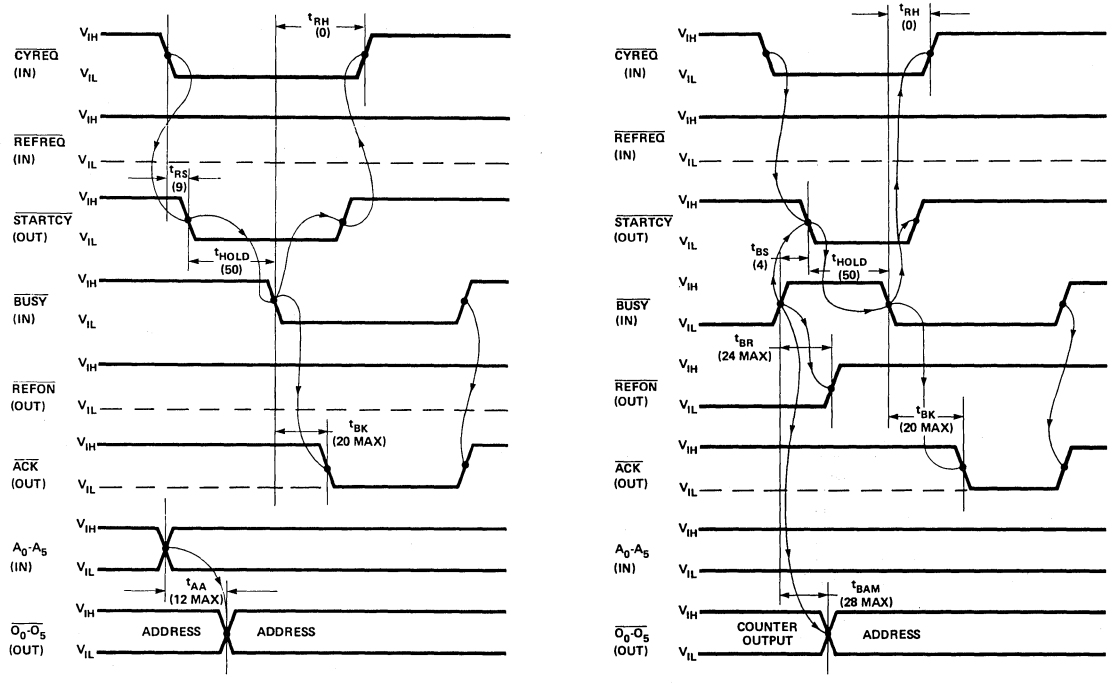
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
t_{AA}	Address In to Address Out		7	12	ns	$\overline{BUSY}$ = V_{IH}
t_{BAM}	$\overline{BUSY}$ In to Address Out		21	28	ns	
t_{BAR}	$\overline{BUSY}$ In to Counter Out		18	27	ns	
t_{BK}	$\overline{BUSY}$ In to $\overline{ACK}$ Out		14	20	ns	$\overline{REFREQ}$ = V_{IH}, $\overline{CYREQ}$ = V_{IL}
t_{BR}	$\overline{BUSY}$ In to $\overline{REFON}$ Out		15	24	ns	
t_{BS}	$\overline{BUSY}$ In to $\overline{STARTCY}$ Out	4	7	14	ns	$\overline{CYREQ}$ = V_{IL}
t_{HOLD}	$\overline{BUSY}$ Hold Time	50			ns	External Delay between $\overline{STARTCY}$ and $\overline{BUSY}$
t_{RH}	$\overline{CYREQ}$ or $\overline{REFREQ}$ Hold Time	0			ns	External Delay after $\overline{BUSY}$
t_{RR}	$\overline{REFREQ}$ to $\overline{REFON}$		18	26	ns	$\overline{CYREQ}$ and $\overline{BUSY}$ = V_{IH}, No priority contention between $\overline{REFREQ}$ and $\overline{CYREQ}$
t_{RRC}	$\overline{REFREQ}$ to $\overline{REFON}$		33	45	ns	$\overline{BUSY}$ = V_{IH}
t_{RS}	$\overline{CYREQ}$ or $\overline{REFREQ}$ In to $\overline{STARTCY}$ Out	9	14	21	ns	$\overline{BUSY}$ = V_{IH}
t_{Setup}	$\overline{BUSY}$ Setup Time	120			ns	$\overline{BUSY}$ = V_{IL} During Refresh

Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

A. SYSTEM MEMORY CYCLE WITH MEMORY NOT BUSY

B. SYSTEM MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING REFRESH CYCLE)

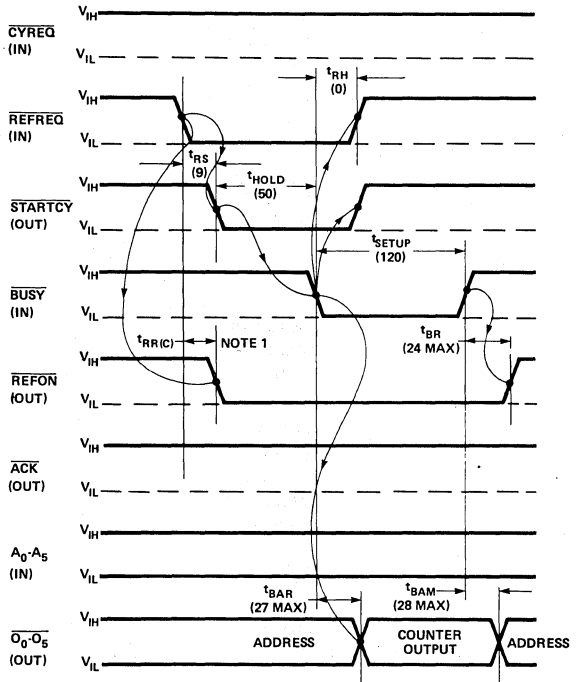
(Numbers in parentheses are minimum values in ns unless otherwise specified.)



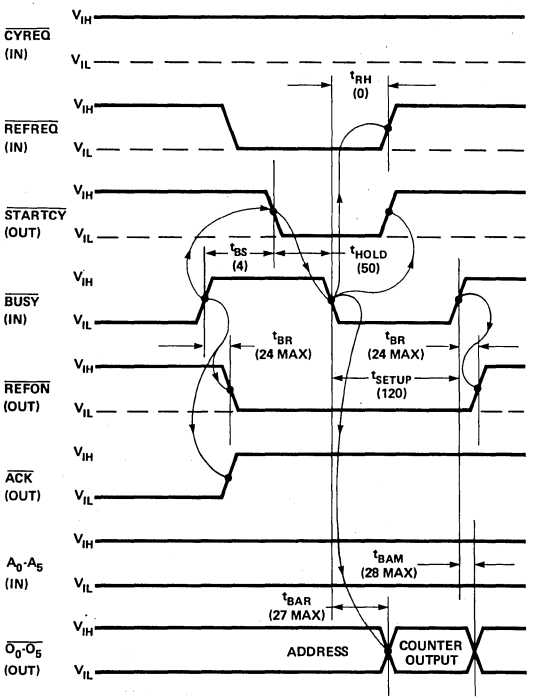
C. REFRESH MEMORY CYCLE WITH MEMORY NOT BUSY

D. REFRESH MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING SYSTEM CYCLE)

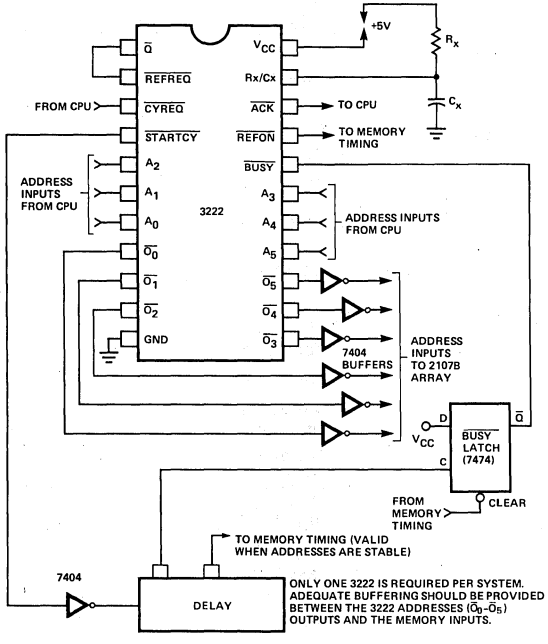
(Numbers in parentheses are minimum values in ns unless otherwise specified.)



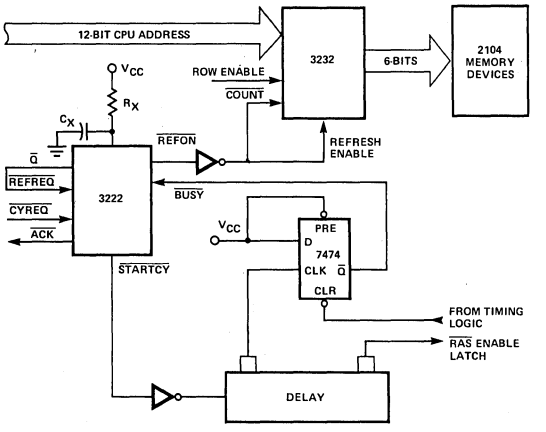
NOTE 1: t_{RR} (26ns MAX) IF PRIORITY CONTENTION IS ELIMINATED; t_{RRC}



E. TYPICAL APPLICATION OF 3222 REFRESH CONTROLLER IN A 2107B SYSTEM



F. USE OF 3222 FOR REFRESH TIMING AND CONTROL IN A 2104 SYSTEM



PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{Q}$	Output of the internal Refresh Request latch. This pin may be connected to the Refresh Request input ($\overline{REFREQ}$) directly for asynchronous sequential mode refresh or indirectly through control logic for burst mode or synchronous mode refresh (see text).
2	$\overline{REFREQ}$	Refresh Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a system cycle request did not occur first.
3	$\overline{CYREQ}$	System Memory Cycle Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a refresh request did not occur first.
4	$\overline{STARTCY}$	Output signal indicating to external circuitry that a memory cycle (system or refresh) is to begin. See text for timing considerations for a refresh cycle.
5-7 15-17	A_0-A_5	Low order system address inputs. These addresses are multiplexed to the address output pins ($\overline{O}_0$-$\overline{O}_5$) during a system cycle.
8-10	$\overline{O}_0$-$\overline{O}_5$	Low order memory address outputs. During a system cycle these outputs give the low order (A_0-A_5) address of a memory access. During a refresh cycle these outputs give the refresh address (generated internal to the 3222).
11	GROUND	Ground.
18	$\overline{BUSY}$	An externally generated signal which the 3222 monitors to determine memory system status. If $\overline{BUSY}$ is high the memory is not busy and a system or refresh cycle may begin. If $\overline{BUSY}$ is low the memory is being accessed for a data I/O or refresh cycle and no other cycle may begin.
19	$\overline{REFON}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a refresh cycle (Refresh On).
20	$\overline{ACK}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a system cycle (system cycle request accepted and acknowledged).
21	RX/CX	Connection point for the RC network which determines the refresh period for sequential refresh mode. (See Refresh Control section).
22	V_{CC}	+5 volt supply.

FUNCTIONAL DESCRIPTION

The Intel® 3222 performs the four basic functions of a refresh controller by:

1. Providing a refresh timing oscillator.
2. Generating six bit refresh addresses.
3. Multiplexing refresh and system addresses to the six low order address inputs ($\overline{O}_0$-$\overline{O}_5$).
4. Providing control signals for both refresh and memory cycle accesses.

As shown in the pin configuration figure, the 3222 has as inputs the six low order (A_0-A_5) system addresses. These addresses are internally multiplexed with six internally generated refresh addresses. The output of these multiplexers provide the six low order addresses to the memory array.

The block diagram shows the four main circuit categories of the 3222. An explanation of the workings of each of these categories is given in the Device Operation section from a users point of view.

DEVICE OPERATION

Operation of the Intel® 3222 Refresh Controller is most easily explained by considering five conditions presented by the three input control lines Cycle Request ($\overline{CYREQ}$), Refresh Request ($\overline{REFREQ}$), and System Busy ($\overline{BUSY}$). These conditions are:

1. System memory cycle request — memory not busy ($\overline{BUSY}$ = High)
2. System memory cycle request — memory busy ($\overline{BUSY}$ =Low)
3. Refresh cycle request — memory not busy ($\overline{BUSY}$ = High)
4. Refresh cycle request — memory busy ($\overline{BUSY}$ =Low)
5. Simultaneous system memory cycle and refresh cycle requests.

Condition 5 is actually a subset of the four previous conditions and is included for completeness.

As is implied in the five conditions, the response of the 3222 to both refresh and memory cycles is dependent on the state of the $\overline{BUSY}$ input. The $\overline{BUSY}$ signal is generated externally to the 3222 and, when low, defines the time when the memory is performing a cycle (refresh or memory access). It is important to assure that $\overline{BUSY}$ is low for the *entire* memory cycle time. Interference may occur in asynchronous memory systems if the $\overline{BUSY}$ input goes high prematurely. (An asynchronous memory system is one in which the refresh and memory cycle requests occur independent of each other.)

System Memory Cycle Request — Memory Not Busy

This section details operation of the 3222 when the memory is not busy and a request for a system memory cycle is made (See Figure A for timing sequences). The request for a memory cycle is made by the $\overline{CYREQ}$ input going low. The Start Cycle output $\overline{STARTCY}$ goes low at t_{RS} after $\overline{CYREQ}$. $\overline{STARTCY}$ is used for two purposes:

1. To set the external $\overline{BUSY}$ latch. (See Figure E.)
2. To initiate memory system timing (after appropriate delay).

The required delay time depends on system configuration and associated delay paths for both Chip Enable (2107B input signal) and system addresses.

The low going $\overline{BUSY}$ input causes the internally generated Start Cycle output to go high and the Acknowledge output $\overline{ACK}$ to go low (after t_{BK} time). The Acknowledge output confirms that the requested system memory cycle has been accepted by the 3222. Note that the cycle request input may be returned to the high state when the $\overline{BUSY}$ input goes low. However, at the designer's discretion, the cycle request line may remain low until "just prior" to $\overline{BUSY}$ returning high. (If $\overline{BUSY}$ goes high before $\overline{CYREQ}$ goes high, another memory access may inadvertently be started.)

When the memory is not busy and a cycle request has been made, the low order system address delay through the 3222 is t_{AA} nsec. When the 3222 is not busy, the low order system addresses (A_0-A_5) are gated through to the output ($\overline{O}_0$-$\overline{O}_5$) independent of any other input.

System Memory Cycle Request — Memory Busy

The major differences between a system memory cycle request when the system is busy and when it is not busy (as previously described) are:

1. The Start Cycle output $\overline{STARTCY}$ does not go low until t_{BS} after the rising edge of the $\overline{BUSY}$ input. (Even though the $\overline{CYREQ}$ input is low.)
2. Output addresses $\overline{O}_0$-$\overline{O}_5$ change at or before t_{AA} time if the previous cycle was a system cycle request and change at or before t_{BAM} if the previous cycle was a Refresh Cycle request. (Note that the longer delay is after a refresh cycle.) See Figure B for definition of terms.

Note that for a system memory cycle following a refresh cycle, the refresh on output $\overline{REFON}$ goes high at or before t_{BR} relative to $\overline{BUSY}$ going high. Since the Acknowledge output $\overline{ACK}$ can not go low until after t_{HOLD} there is no ambiguity between $\overline{REFON}$ and $\overline{ACK}$. The memory is always defined as being in a refresh cycle, system cycle or no cycle.

Refresh Cycle — Memory Not Busy

Operation of the 3222 for a refresh request with the memory not busy (see Figure C) is similar to a system cycle request under the same condition. A refresh cycle is initiated by the Refresh Request input ($\overline{REFREQ}$) going low. This low going input causes both the Start Cycle output, $\overline{STARTCY}$, and Refresh On output, $\overline{REFON}$, to go low at t and t_{RRC} (or t_{RR}) time respectively. The low going edge of $\overline{STARTCY}$ is used to set the external $\overline{BUSY}$ latch low. As in the previous two cases, the $\overline{BUSY}$ input must remain low for the entire cycle required by the memory. As in the previous two cases, the low going $\overline{BUSY}$ drives the $\overline{STARTCY}$ output high.

Refresh Cycle — Memory Busy

For this condition, it is assumed that the previous cycle was a system access cycle. Timing conditions for this operation are shown in Figure D. Here, the $\overline{STARTCY}$ input goes low t_{BS} after $\overline{BUSY}$ returns high from the previous cycle. As before, $\overline{REFON}$ goes low t_{BR} after $\overline{BUSY}$ goes high. After t_{HOLD}, relative to $\overline{STARTCY}$, $\overline{BUSY}$ again goes low and places the low order refresh addresses on the address outputs ($\overline{O}_0$-$\overline{O}_5$) after t_{BAR} time. Internal refresh timing is performed in a manner identical to that described in Refresh Cycle-Memory Not Busy section.

Simultaneous Refresh and Memory System Cycle Request

The simultaneous request for a refresh and memory system access is almost a certainty in asynchronous systems. It is, therefore, necessary to have circuitry in any refresh controller capable of resolving the attendent ambiguity with minimum additional delay. The Intel® 3222 Refresh Controller has just such a circuit. (All timing parameters specified for asynchronous operation assume that a refresh and memory system request can occur at the same time.) A latch internal to the 3222 decides which signal ($\overline{CYREQ}$ or $\overline{REFREQ}$) it will accept if both occur simultaneously, and conditions the other control circuits appropriately. If a refresh cycle was accepted, $\overline{REFON}$ will go low at the appropriate time. If a memory system access was accepted then $\overline{ACK}$ will go low at the appropriate time.

Refresh Control

The 3222 controls both burst and distributed refresh modes. The burst refresh mode requires that $\overline{REFREQ}$ be generated externally to the 3222 since refresh is completed in 64 consecutive cycles every 2ms. A system requiring distributed refresh timing, however can be controlled either by the 3222 or by external circuitry. If refresh timing is to be controlled by the 3222 the output $\overline{Q}$ is tied to the $\overline{REFREQ}$ input. Timing is controlled by an oscillator internal to the 3222. The desired refresh timing interval is determined by:

1. $\frac{t_{REF}}{r} = .63\ R_xC_x$

   Where:

   t_{REF} = the total time between refreshes (e.g. 2msec) in msec.

   r = the number of rows to be refreshed on the memory device (for the 2107B r = 64).

   R_X = external timing resistance in KΩ (3K to 10K)

   C_x = external timing capacitance in μf. (0.005μf to 0.02μf)

The 3222's oscillator stability is guaranteed to be ±2% for a given part and ±6% from part to part, both over the ranges $0°C \leq T_A \leq 75°C$ and $V_{CC} = 5.0V \pm 5\%$.

Figure F shows how the 3222 may be used to control refresh in a 2104 system.

MEMORY SUPPORT

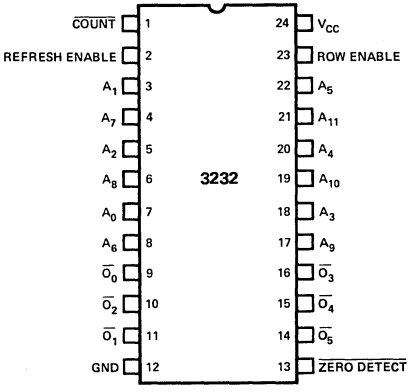
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 4K DYNAMIC RAMs

- **Ideal For 2104**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 24-Pin DIP**
- **Address Input to Output Delay: 9ns Maximum Driving 15pF, 25ns Maximum Driving 250pF**
- **Suitable For Either Distributed Or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**

The Intel® 3232 contains an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). It multiplexes twelve bits of system supplied address to six output address pins. The device also contains a 6 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3232 makes it especially suitable for use with high speed N-channel RAMs like the 2104.

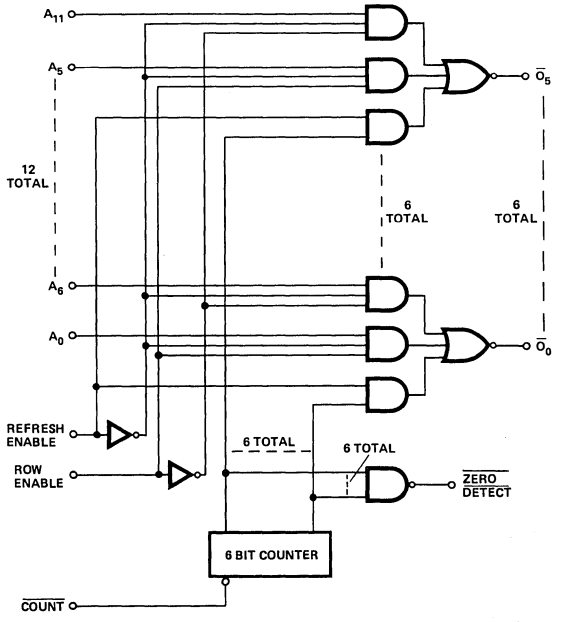
The 3232 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range.

PIN CONFIGURATION



NOTE: A_0 THROUGH A_5 ARE ROW ADDRESSES.
A_6 THROUGH A_{11} ARE COLUMN ADDRESSES.

LOGIC DIAGRAM



TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_5)
L	L	COLUMN ADDRESS (A_6 THROUGH A_{11})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES A ZERO IN THE REFRESH ADDRESS (USED IN BURST REFRESH MODE).

Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Temperature Under Bias ..... -65° to +125°C
Storage Temperature ..... -65° to +160°C
All Input, Output, or
Supply Voltages .....-0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

All Limits Apply for V_{CC} = 5.0V ±10%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	V_{IN} = 0.45V
I_R	Input Leakage Current		0	10	μA	V_{IN} = 5.5V
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O_0}$-$\overline{O_5}$)	2.8	4.0		V	I_{OH} = −1mA
V_{OH1}	Output High Voltage ($\overline{Zero\ Detect}$)	2.4	3.3		V	I_{OH} = −1mA
I_{CC}	Power Supply Current		100	150	mA	V_{CC} = 5.5V

Note 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

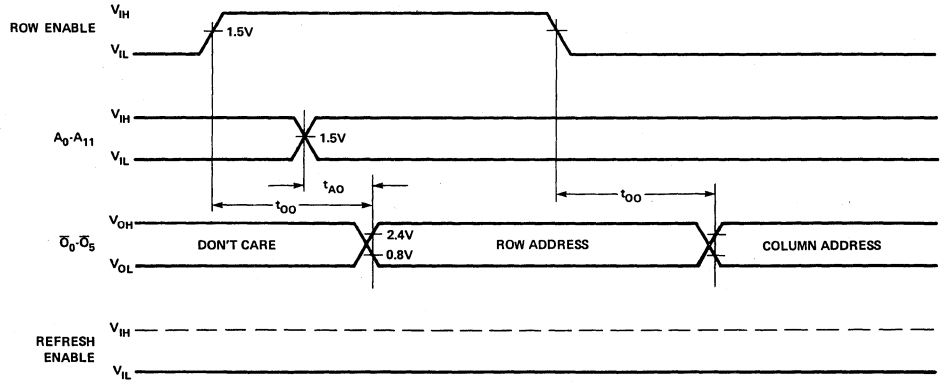
SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low(1) (2)
t_{AOI}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	18	ns	Refresh Enable = Low(1) (2)
t_{OOI}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	20	ns	Note 1, 2
t_{EOI}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{\text{Count}}$ to Output	15	40	60	ns	Refresh Enable = High(1) (2)
t_{COI}	$\overline{\text{Count}}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency	5			MHz	
t_{CPW}	$\overline{\text{Count}}$ Pulse Width	35			ns	
t_{CZ}	$\overline{\text{Count}}$ to $\overline{\text{Zero Detect}}$			70	ns	Note 2

Note 1: V_{CC} = 5.0V, T_A = 25°C
2: C_L = 15pF

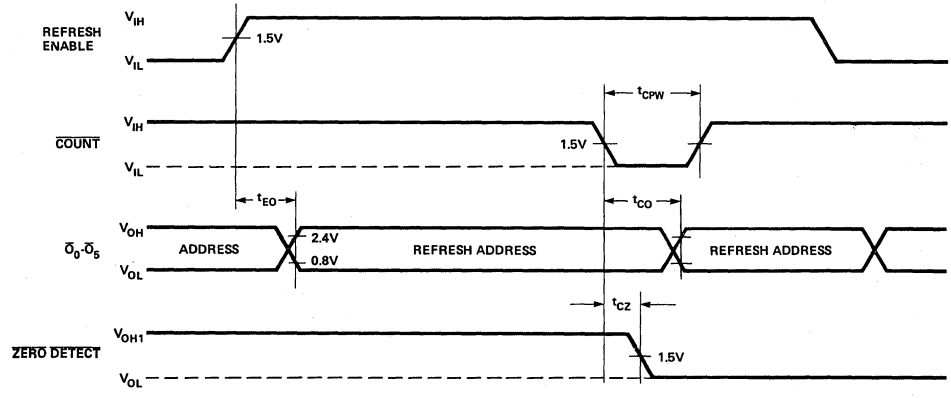
MEMORY SUPPORT

A.C. TIMING WAVEFORMS (Typically used with 2104)

NORMAL CYCLE



REFRESH CYCLE



PIN NAMES AND FUNCTIONS

Pin. No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input	Active low input increments internal six bit counter by one for each count pulse in.
2	Refresh Enable Input	Active high input which determines whether the 3232 is in refresh mode (H) or address enable (L).
7,3,5,18, 20,22	A_0-A_5 Inputs	Row Address inputs.
8,4,6,17, 19,21	A_6-A_{11} Inputs	Column address inputs.
9,11,10, 16,15,14	$\overline{O}_0$-$\overline{O}_5$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
12	GND	Power supply ground.
13	$\overline{\text{Zero}}$ $\overline{\text{Detect}}$ Output	Active low output which senses that all six bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
23	Row Enable Input	High input selects row, low input selects column addresses of the driven memories.
24	V_{CC}	+5V power supply input.

DEVICE OPERATION

The Intel® 3232 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the 6 outputs of the internal 6 bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$-$\overline{O}_5$) through all 64 row addresses. When the counter sequences to all zeros, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output goes low signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output is valid only after t_{CZ} following the low going edge of $\overline{\text{Count}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of rows in the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2104, $t_{REFRESH}$ = 2msec and n = 64, therefore one row is refreshed each 31 μsec. Following the refresh cycle at row n_x, the $\overline{\text{Count}}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The $\overline{\text{Count}}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All twelve system address lines are applied to the inputs of the 3232. When Refresh Enable is low and Row Enable is high, input addresses A_0-A_5 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_6-A_{11} are gated to the outputs and applied to the driven memories.

Figure 1 shows a typical connection between the 3232 and the 2104 4K dynamic RAM. When the memory devices are driven directly by the 3232, the address applied to the memory devices is the inverse of the address at the 3232 inputs due to the inverted outputs of the 3232. This should be remembered when checking out the memory system.

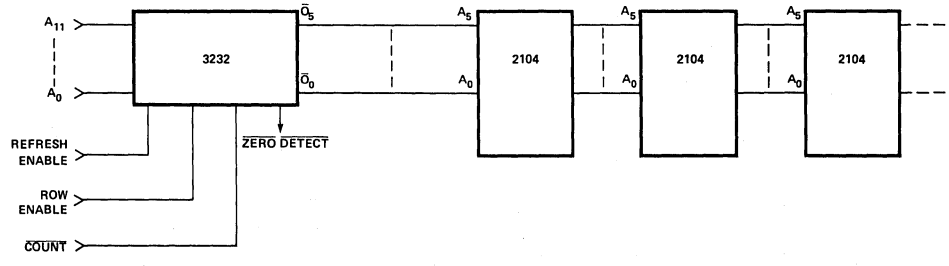


Figure 1. Typical Connection of 3232 and 2104 Memories.

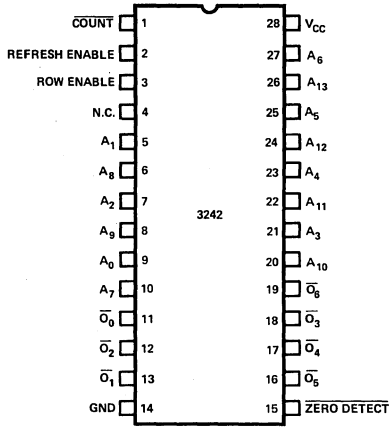
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 16K DYNAMIC RAMs

- **Ideal For 2116**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 28-Pin DIP**
- **Suitable For Either Distributed Or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**
- **Address Input to Output Delay: 9ns Maximum Driving 15 pF, 25ns Maximum Driving 250pF**

The Intel® 3242 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to 7 output address pins. The device also contains a 7 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3242 makes it especially suitable for use with high speed N-channel RAMs like the 2116.

The 3242 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range.

PIN CONFIGURATION



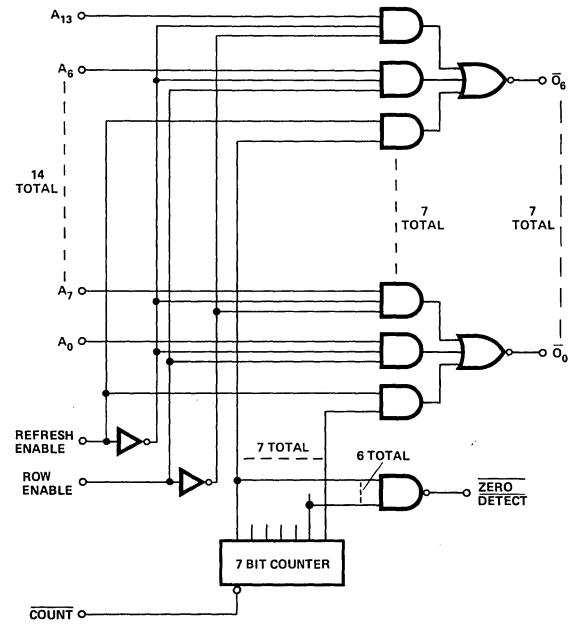
NOTE: A_0 THROUGH A_6 ARE ROW ADDRESSES.
A_7 THROUGH A_{13} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_6)
L	L	COLUMN ADDRESS (A_7 THROUGH A_{13})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES ZERO IN THE FIRST 6 SIGNIFICANT REFRESH COUNTER BITS (USED IN BURST REFRESH MODE)

LOGIC DIAGRAM



QUAD TTL-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

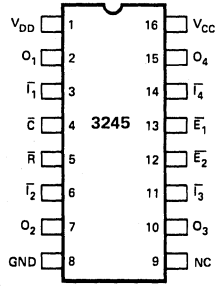
- **Fully Compatible With 4K RAMs Without Requiring Extra Supply Or External Devices**
- **High Speed, 32 nsec Max. — Delay + Transition Time**
- **Low Power — 75mW Typical Per Channel**
- **High Density — Four Drivers in One Package**
- **TTL & DTL Compatible Inputs**
- **CerDIP Package — 16 Pin DIP**
- **Only +5 and +12 Volt Supplies Required**

The Intel® 3245 is a Quad Bipolar-to-MOS driver which accepts TTL and DTL input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107B. The circuit operates from two power supplies which are 5 and 12 volts. Input and output clamp diodes minimize line reflections.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system designs. The internal gating structure of the 3245 eliminates gating delays and minimizes package count.

The 3245 is fabricated by means of Intel's highly reliable Schottky bipolar process and is specified for operation over a 0 to +75°C ambient temperature range.

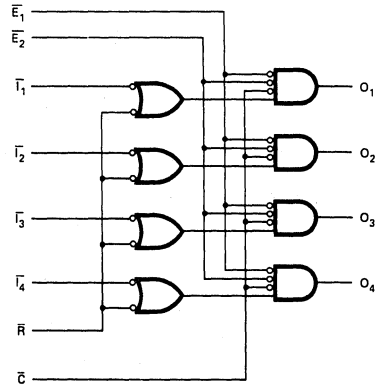
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	NC	NOT CONNECTED

LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature. . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 to +7V
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -1.0 to V_{DD}
Outputs for Clock Driver. . . . . -1.0 to V_{DD} +1V
Power Dissipation at 25°C 2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$		-0.25	mA	V_F = 0.45V
I_{FE}	Input Load Current, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$		-1.0	mA	V_F = 0.45V
I_{RD}	Data Input Leakage Current		10	μA	V_R = 5.0V
I_{RE}	Enable Input Leakage Current		40	μA	V_R = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5mA, V_{IH} = 2V
		-1.0		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.50		V	I_{OH} = -1mA, V_{IL} = 0.8V
			V_{DD}+1.0	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs		0.8	V	
V_{IH}	Input High Voltage, All Inputs	2		V	

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions — Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	23	30	mA	High	
I_{DD}	Current from V_{DD}	19	26	mA		
P_{D1}	Power Dissipation	365	485	mW		
	Power Per Channel	91	121	mW		V_{CC} = 5.25V
I_{CC}	Current from V_{CC}	29	39	mA	Low	V_{DD} = 12.6V
I_{DD}	Current from V_{DD}	12	15	mA		
P_{D2}	Power Dissipation	300	388	mW		
	Power Per Channel	75	97	mW		

MEMORY SUPPORT

A.C. Characteristics T_A = 0° to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	5	11		ns	R_{SERIES} = 0
t_{DR}	Delay Plus Rise Time		20	32	ns	R_{SERIES} = 0
t_{+-}	Input to Output Delay	3	7		ns	R_{SERIES} = 0
t_{DF}	Delay Plus Fall Time		18	32	ns	R_{SERIES} = 0
t_T	Output Transition Time	10	17	25	ns	R_{SERIES} = 20Ω
t_{DR}	Delay Plus Rise Time		27	38	ns	R_{SERIES} = 20Ω
t_{DF}	Delay Plus Fall Time		25	38	ns	R_{SERIES} = 20Ω

NOTES: 1. C_L = 150pF
2. C_L = 200pF
3. C_L = 250pF
These values represent a range of total stray plus clock capacitance for nine 4K RAMs.
4. Typical values are measured at 25°C.

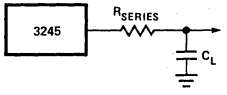
Capacitance* T_A = 25°C

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance, $\overline{I_1}$,$\overline{I_2}$,$\overline{I_3}$,$\overline{I_4}$	5	8	pF
C_{IN}	Input Capacitance, $\overline{R}$,$\overline{C}$,$\overline{E_1}$,$\overline{E_2}$	8	12	pF

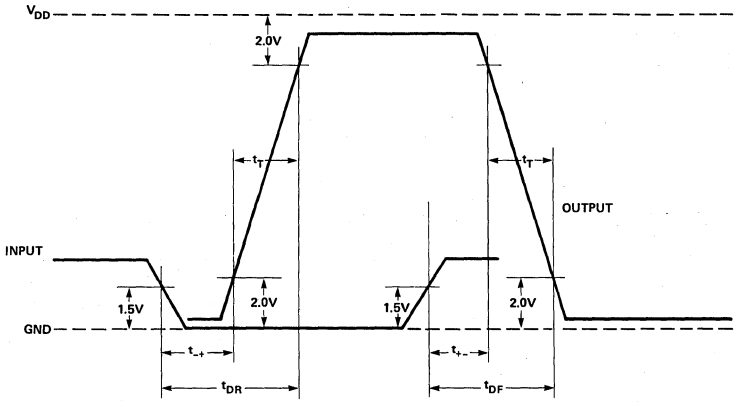
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 3.0V
Input Pulse Rise and Fall Times: 5 ns between 1 volt and 2 volts
Measurement Points: See Waveforms

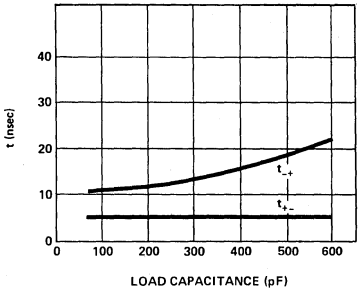


Waveforms

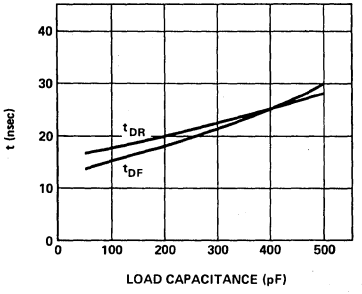


Typical Characteristics

INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE



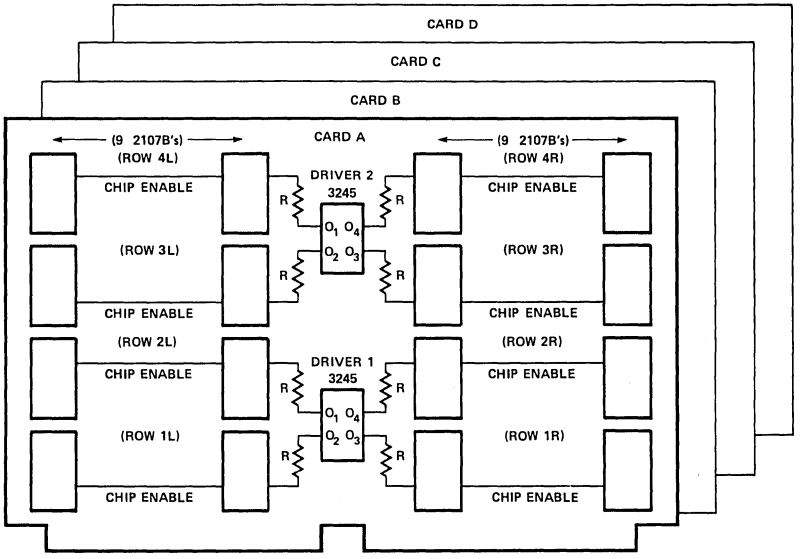
DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE



MEMORY SUPPORT

Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 3245 quad high voltage driver for the chip enable inputs. A single 3245 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



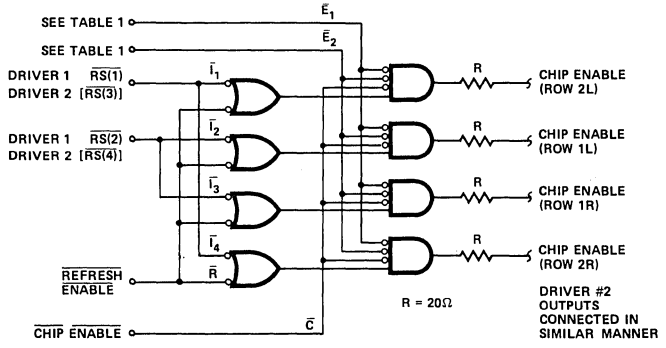
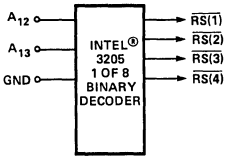
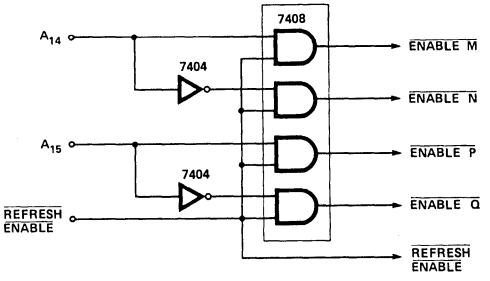


TABLE 1.

CARD	INPUTS $\bar{E}_1$	INPUTS $\bar{E}_2$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
C	ENABLE N	ENABLE P
D	ENABLE N	ENABLE Q





QUAD ECL-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

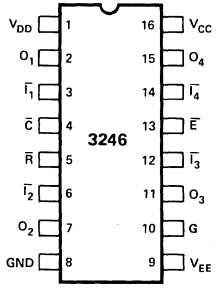
- **Fully Compatible With 4K RAMs Without Requiring Extra Supply Or External Devices.**
- **High Speed, 30 nsec Max. — Delay + Rise Time**
- **10K ECL Compatible Inputs**
- **High Density — Four Drivers In One Package**
- **CerDIP Package — 16 Pin DIP**

The Intel® 3246 is a Quad Bipolar-to-MOS driver which accepts ECL input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107 or 2105. The circuit operates from three power supplies which are 5, -5.2, and 12 volts. Input and output clamp diodes minimize line reflections.

The device features a common enable input, a refresh select input, and a clock control input for simplified system designs. The internal gating structure of the 3246 eliminates gating delays and minimizes package count.

The 3246 is fabricated by means of Intel's Schottky Bipolar technology to assure high performance over the 0°C to +75°C ambient temperature range.

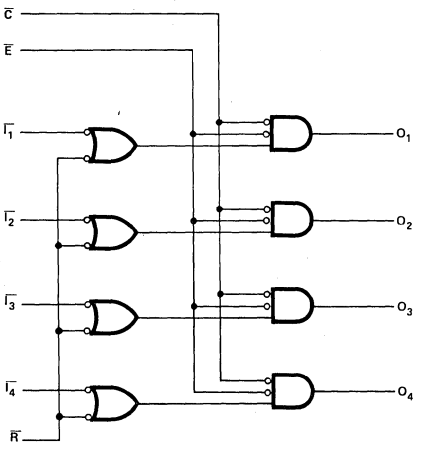
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E}$	ENABLE INPUT	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	V_{EE}	-5.2V POWER SUPPLY
		G	GROUND REFERENCE

LOGIC DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 to +7V
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
Supply Voltage, V_{EE} . . . . . -7.0 to +0.5V
All Input Voltages . . . . . V_{EE} to +0.5V
Outputs for Clock Driver . . . . . -1.0 to V_{DD} +1V
Power Dissipation at 25°C 2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%, V_{EE} = -5.2V ±5%

Symbol	Parameter	Min.	Typ[1]	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\overline{I_1}$, $\overline{I_2}$, $\overline{I_3}$, $\overline{I_4}$		0.3	0.5	mA	V_F = -0.8V
I_{FE}	Input Load Current, $\overline{R}$,$\overline{C}$,$\overline{E}$		1.0	2.0	mA	V_F = -0.8V
V_{OL}	Output Low Voltage		0.2	0.45	V	I_{OL}=5mA, V_{IH}=-1.025V
		-0.5			V	I_{OL} = -1mA
V_{OH}	Output High Voltage	V_{DD}-0.5	V_{DD}-0.2		V	I_{OH}=-1mA, V_{IL}=-1.520V
			V_{DD}	V_{DD}+0.5	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs			-1.520	V	
V_{IH}	Input High Voltage, All Inputs	-1.025			V	

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

Symbol	Parameter	Typ.[1]	Max.	Unit	Test Conditions — Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	20	27	mA	High	V_{CC} = 5.25V V_{DD} = 12.6V V_{EE} = -5.46V
I_{DD}	Current from V_{DD}	23	31	mA		
I_{EE}	Current from V_{EE}	-35	-42	mA		
P_{D1}	Power Dissipation	586	762	mW		
	Power Per Channel	146	190	mW		
I_{CC}	Current from V_{CC}	17	24	mA	Low	
I_{DD}	Current from V_{DD}	14	22	mA		
I_{EE}	Current from V_{EE}	-29	-36	mA		
P_{D2}	Power Dissipation	424	600	mW		
	Power Per Channel	106	150	mW		

Note: 1. Typical values are for T_A = 25°C and nominal power supply voltages.

A.C. Characteristics $T_A = 0°$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$, $V_{EE} = -5.2V \pm 5\%$

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	8	12		ns	$R_{SERIES} = 0$
t_{DR}	Delay Plus Rise Time		18	30	ns	$R_{SERIES} = 0$
t_{+-}	Input to Output Delay	8	13		ns	$R_{SERIES} = 0$
t_{DF}	Delay Plus Fall Time		25	35	ns	$R_{SERIES} = 0$
t_T	Output Rise Time	10	13	23	ns	$R_{SERIES} = 20\Omega$
t_{DR}	Delay Plus Rise Time		23	34	ns	$R_{SERIES} = 20\Omega$
t_{DF}	Delay Plus Fall Time		30	40	ns	$R_{SERIES} = 20\Omega$

NOTES: 1. $C_L = 150pF$
2. $C_L = 200pF$
3. $C_L = 250pF$

These values represent a range of total stray plus clock capacitance for nine 4K RAMs.

4. Typical values are measured at 25°C.

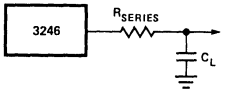
Capacitance* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance, $\overline{I_1}, \overline{I_2}, \overline{I_3}, \overline{I_4}, \overline{R}$	4	7	pF
C_{IN}	Input Capacitance, $\overline{C}, \overline{E}$	8	12	pF

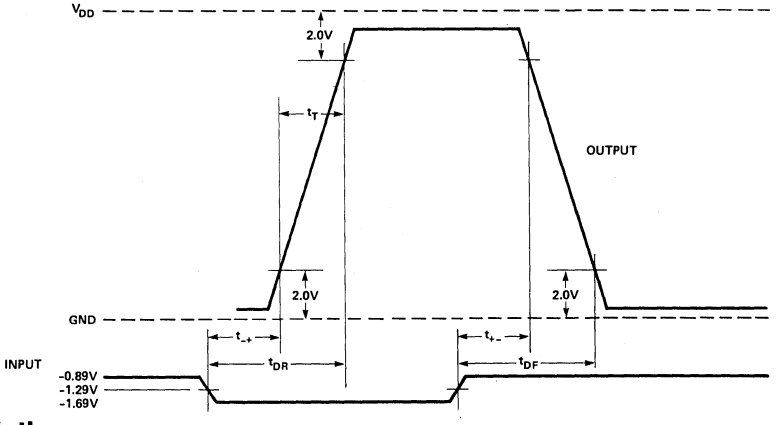
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = -1V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 0.8V
Input Pulse Rise and Fall Times: 5 ns (between 10% and 90% Points)
Measurement Points: See Waveforms

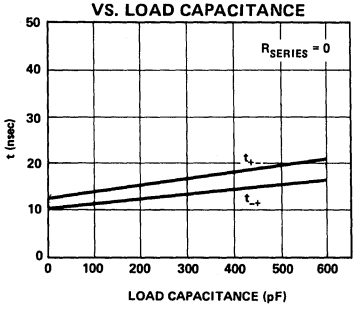


Waveforms

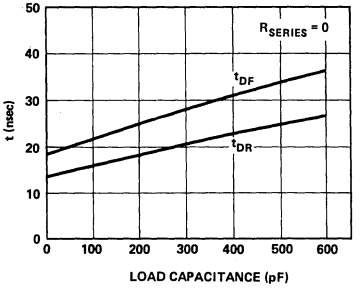


Typical Characteristics

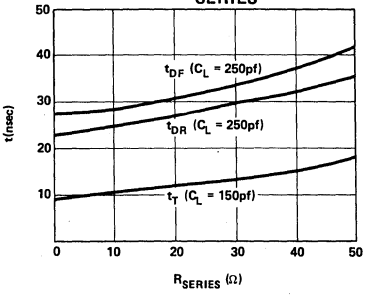
INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE



DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE

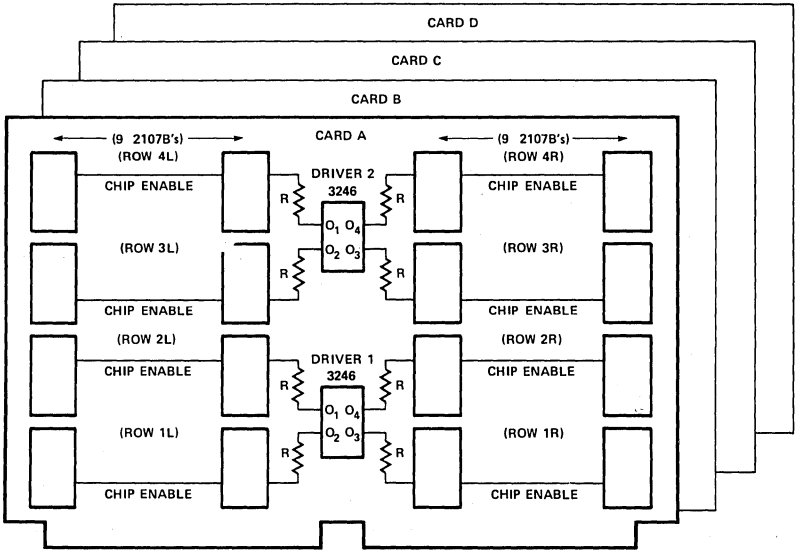


DELAY PLUS TRANSITION TIME VS. R_{SERIES}



Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 3246 quad high voltage driver for the chip enable inputs. A single 3246 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



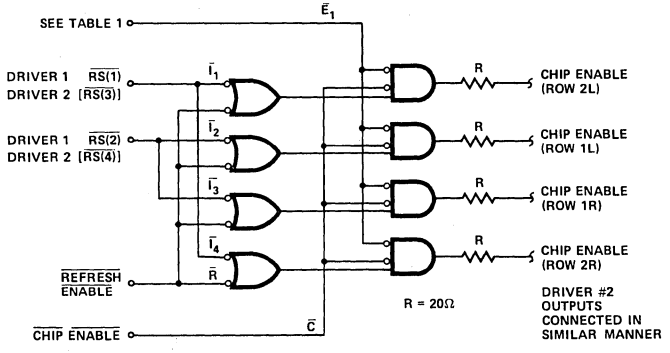
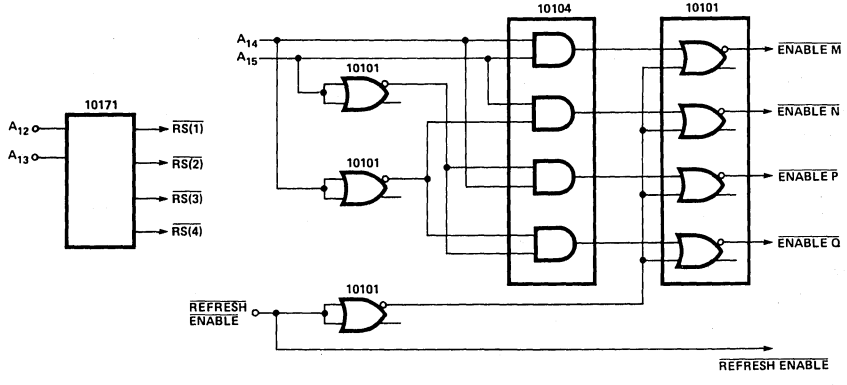


TABLE 1.

CARD	INPUTS E_1
A	$\overline{\text{ENABLE M}}$
B	$\overline{\text{ENABLE N}}$
C	$\overline{\text{ENABLE P}}$
D	$\overline{\text{ENABLE Q}}$



QUAD CMOS-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

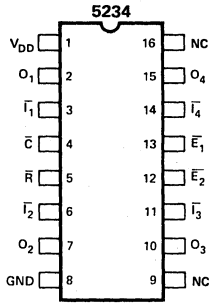
- **CMOS Technology for Very Low Power: Suitable for Battery Backup**
- **High Density: Four Drivers in One Package**
- **Internal Gating Structure Minimizes Package Count**
- **CMOS Compatible Inputs**
- **CerDIP Package: 16 Pin DIP**
- **Only One Power Supply Required, +12V (±10%)**

The Intel® 5234 is a Quad CMOS-to-MOS driver which accepts CMOS input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107A or 2107B. The circuit operates from a single 12 volt power supply.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system design.

The Intel ion-implanted, silicon gate, Complementary MOS (CMOS) process allows the design and production of very low power drivers.

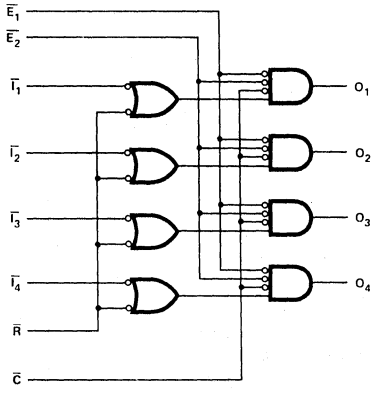
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	$\overline{C}$	CLOCK CONTROL INPUT
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
		NC	NOT CONNECTED

LOGIC DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -0.5 to (V_{DD}+0.5V)
Outputs for Clock Driver . . . . . -0.5 to (V_{DD}+0.5V)
Power Dissipation at 25°C 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = 12V ±10%.

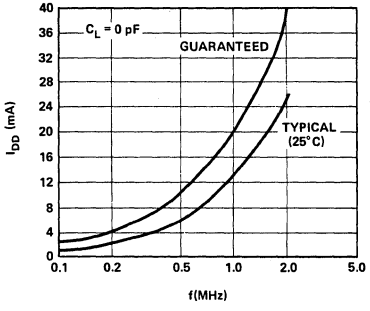
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Load Current			0.1	µA	V_{IN} = 0 to V_{DD}
V_{OL}	Output Low Voltage		0.15	0.4	V	I_{OL} = 5mA
		-1.0	-0.15			I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.4	V_{DD}-0.15		V	I_{OH} = -5mA
			V_{DD}+.15	V_{DD}+0.5		I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs			2.0	V	
V_{IH}	Input High Voltage, All Inputs	V_{DD}-2.0			V	
I_{DD}	Supply Current		0.1	100	µA	V_{DD} = 13.2V, f = 0
I_{DD1}	Supply Current		13	20	mA	V_{DD} = 13.2V, f = 1MHz, C_L = 0, (See Figure 1)

Note 1: Typical values are at 25° C and nominal voltage.

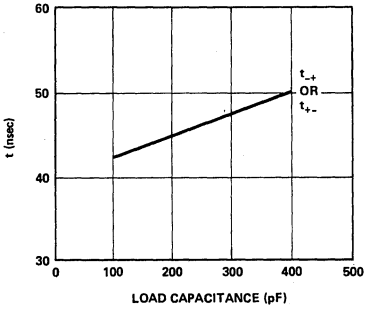
Typical Characteristics

FIGURE 1

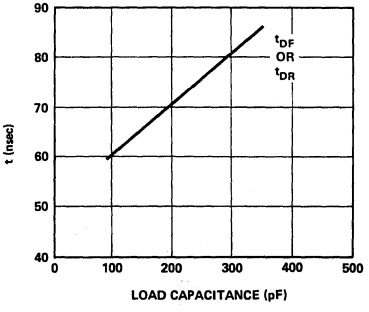
POWER SUPPLY CURRENT VS. FREQUENCY (ALL 4 CHANNELS SWITCHING)



INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE



DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE



MEMORY SUPPORT

A.C. Characteristics $T_A = 0°$ to $70°C$, $V_{DD} = 12V \pm 10\%$.

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit
t_{-+}	Input to Output Delay	20	45		ns
t_{DR}	Delay Plus Rise Time		70	100	ns
t_{+-}	Input to Output Delay	20	45		ns
t_{DF}	Delay Plus Fall Time		70	100	ns
t_T	Output Transition Time	10	25	40	ns

NOTES: 1. $C_L = 150pF$
2. $C_L = 200pF$
3. $C_L = 250pF$

These values represent a range of total stray plus clock capacitance for nine 4K RAMs.

4. Typical values are measured at 25° C.

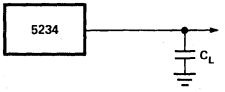
Capacitance* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	8	14	pF

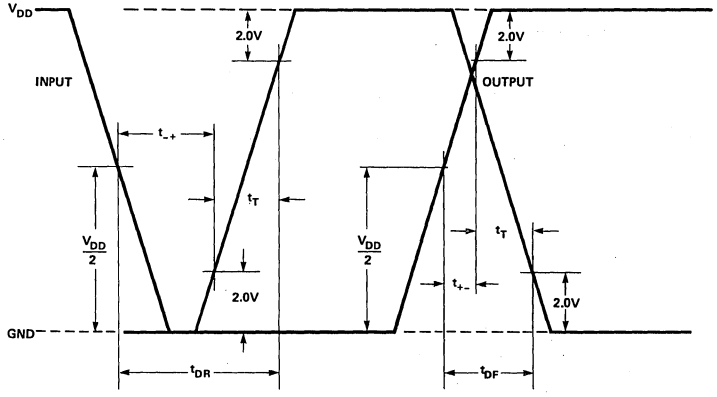
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 0 to V_{DD}
Input Pulse Rise and Fall Times: 40 ns between 10% and 90% points
Measurement Points: See Waveforms



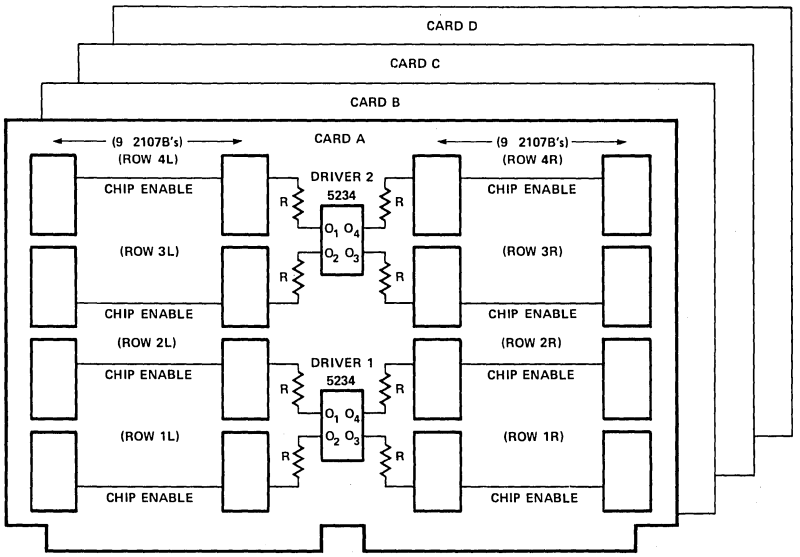
Waveforms



MEMORY SUPPORT

Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 5234 quad high voltage driver for the chip enable inputs. A single 5234 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



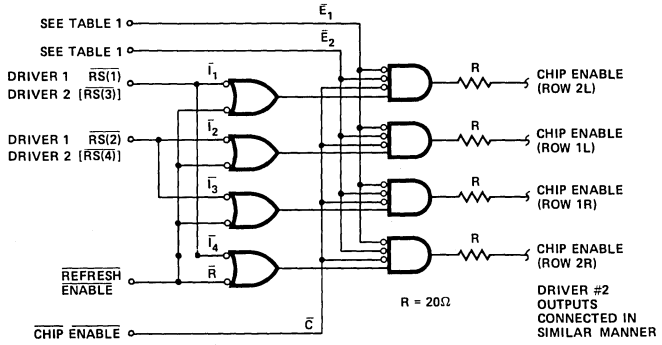
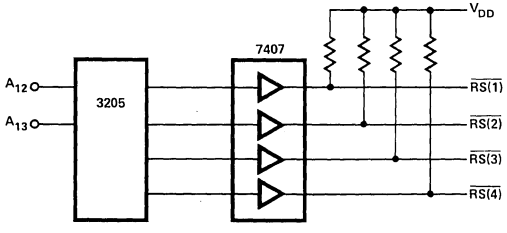
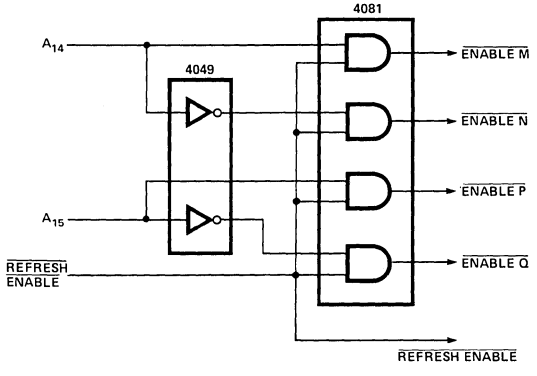


TABLE 1.

CARD	INPUTS $\bar{E}_1$	INPUTS $\bar{E}_2$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
C	ENABLE N	ENABLE P
D	ENABLE N	ENABLE Q





MEMORY SUPPORT

QUAD TTL-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

- **CMOS Technology for Very Low Power: Suitable for Battery Backup**
- **High Density: Four Drivers in One Package**
- **Internal Gating Structure Minimizes Package Count**
- **TTL & DTL Compatible Inputs**
- **CerDIP Package: 16 Pin DIP**
- **Only One Power Supply Required, +12V (±10%)**

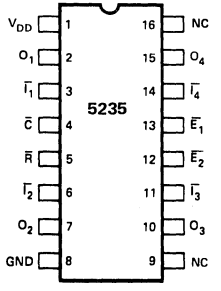
The Intel® 5235 and 5235-1 are Low Power Quad TTL-to-MOS drivers which accept TTL and DTL input levels. They provide high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107A or 2107B. The circuit operates from a single 12 volt power supply.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system design.

The 5235-1 is a selection of the 5235 and is guaranteed for 95ns maximum delay plus transition time while driving a 250pF load.

The Intel ion-implanted, silicon gate Complementary MOS (CMOS) process allows the design and production of very low power drivers.

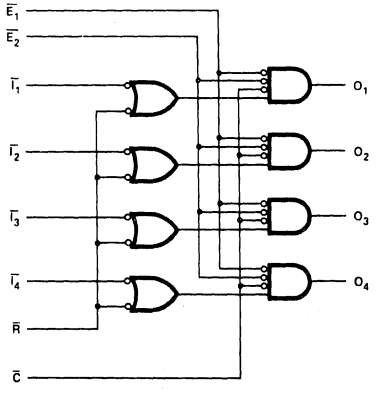
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	$\overline{C}$	CLOCK CONTROL INPUT
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
		NC	NOT CONNECTED

LOGIC DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -0.5 to (V_{DD}+0.5V)
Outputs for Clock Driver . . . . . -0.5 to (V_{DD}+0.5V)
Power Dissipation at 25°C 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to 70°C, V_{DD} = 12V ±10%.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Load Current		0.1	10	μA	V_{IN} = ≤0.4V or ≥2.4V
V_{OL}	Output Low Voltage		0.15	0.4	V	I_{OL} = 5mA
		-1.0	-0.15		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.4	V_{DD}-0.15		V	I_{OH} = -5mA
			V_{DD}+0.15	V_{DD}+0.5	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs			0.8	V	
V_{IH}	Input High Voltage, All Inputs	2.0			V	
I_{DD0}	Supply Current		1.0	2.0	mA	f = 0MHz; V_{DD}=13.2V, V_{IN}≤0.4V or V_{IN}≥2.4V, C_L = 0pf.
I_{DD1}	Supply Current		12	20	mA	f = 1MHz (See Figure 1); V_{DD}=13.2V, V_{IN}≤0.4V or V_{IN}≥2.4V, C_L = 0pf.

Note 1: Typical values are at 25°C and nominal voltage.

Typical Characteristics

Figure 1.
POWER SUPPLY CURRENT VS. FREQUENCY
(ALL 4 CHANNELS SWITCHING)

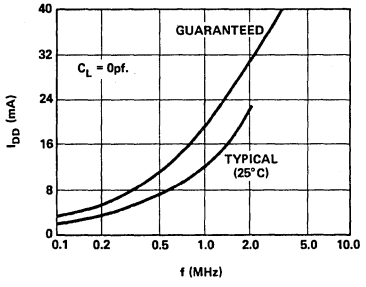


Figure 2.
DELAY PLUS TRANSITION TIME
VS. LOAD CAPACITANCE

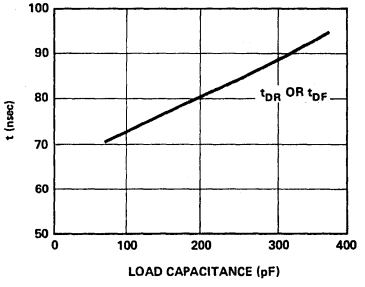


Figure 3.
DELAY PLUS TRANSITION TIME
VS. INPUT VOLTAGE

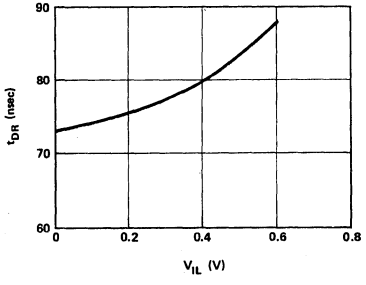
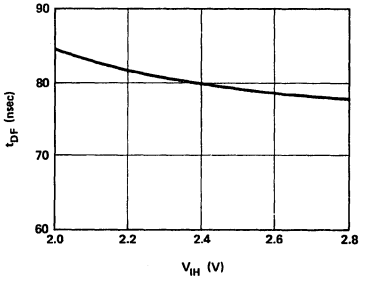


Figure 4.
DELAY PLUS TRANSITION TIME
VS. INPUT VOLTAGE



MEMORY SUPPORT

A.C. Characteristics $T_A = 0°$ to $70°C$, $V_{DD} = 12V \pm 10\%$.

Symbol	Parameter	5235-1			5235			Unit
		Min.[1]	Typ.[2,4]	Max.[3]	Min.[1]	Typ.[2,4]	Max.[3]	
t_{-+}	Input to Output Delay	20	55		20	70		ns
t_{DR}	Delay Plus Rise Time		75	95		95	125	ns
t_{+-}	Input to Output Delay	20	55		20	70		ns
t_{DF}	Delay Plus Fall Time		75	95		95	125	ns
t_T	Transition Time	10	20	40	10	25	40	ns

NOTES: 1. $C_L = 150pF$
2. $C_L = 200pF$
3. $C_L = 250pF$

These values represent a range of total stray plus clock capacitance for nine 4K RAMs.

4. Typical values are measured at 25°C, and nominal voltage.

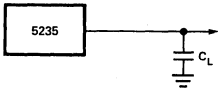
Capacitance* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	8	14	pF

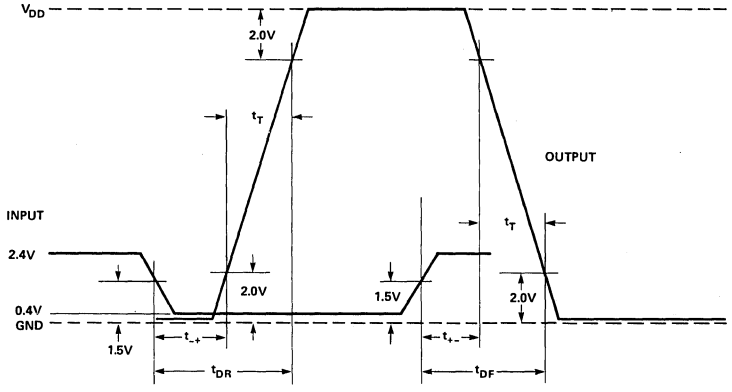
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 2.0V
Input Pulse Rise and Fall Times: 5 ns between 0.9 volt and 1.9 volts
Measurement Points: See Waveforms



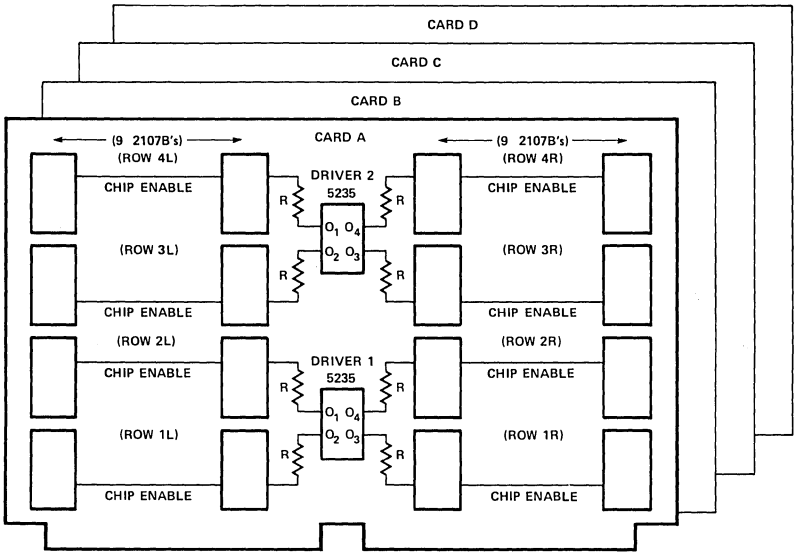
Waveforms



MEMORY SUPPORT

Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 5235 quad high voltage driver for the chip enable inputs. A single 5235 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



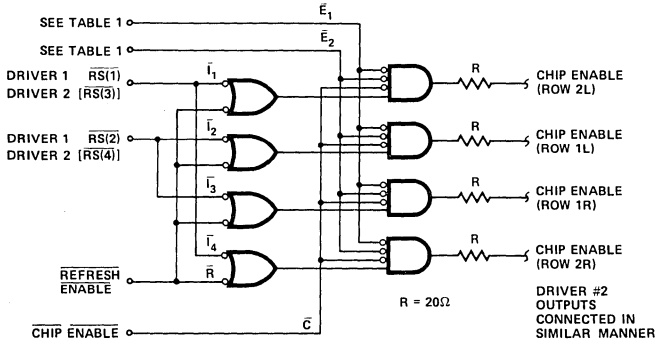
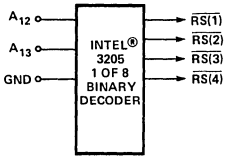
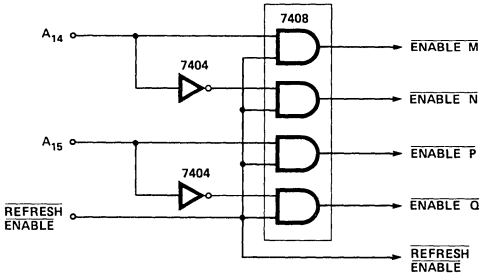


TABLE 1.

CARD	INPUTS $\bar{E}_1$	INPUTS $\bar{E}_2$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
C	ENABLE N	ENABLE P
D	ENABLE N	ENABLE Q





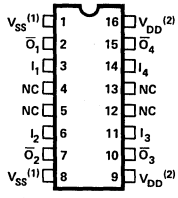
QUAD CCD CLOCK DRIVER

- **Internal Circuitry Minimizes CCD Clock Cross-Coupling Voltage Transients**
- **Drives Four 2416s**
- **Low Standby Power Dissipation: 24mW Typically**
- **TTL Inputs**
- **Single +12V Supply**
- **Standard 16 Pin Dual In-Line Package**

The 5244 is a quad clock driver which provides high capacitive drive suitable for driving charge coupled memories. The 5244 features very low D.C. power dissipation from a single 12V supply with output characteristics directly compatible with the 2416 clock input requirements. Internal circuitry controls the cross-coupled voltage transients between the clock phases generated by the 2416 and limits the transition time so that excessively fast transitions do not occur on the clock line.

The 5244 is fabricated using an advanced ion-implanted, silicon gate, CMOS process.

PIN CONFIGURATION

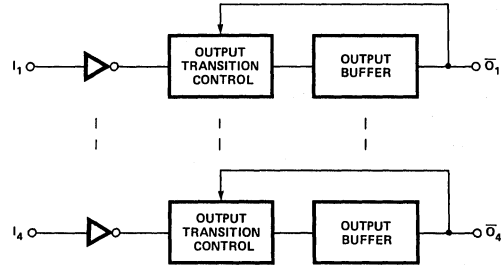


NOTES: 1. BOTH PIN 1 AND 8 MUST BE CONNECTED TO V_{SS}.
2. BOTH PIN 9 AND 16 MUST BE CONNECTED TO V_{DD}.

PIN NAMES

$I_1 - I_4$	TTL INPUT
$\overline{O}_1 - \overline{O}_4$	DRIVER OUTPUT
V_{DD}	+12V POWER SUPPLY
NC	NOT CONNECTED
V_{SS}	GROUND

BLOCK DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to 80°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage with Respect to Vss ..... -0.5 to +14V
All Input Voltages ..... -0.5 to (V_{DD}+1V)
Outputs ..... -1V to (V_{DD} +1)
Power Dissipation 1.35W

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{SS} = 0V

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{IL}	Low Level Input Current	-10	±0.1	10	μA	$V_{IN} \leqslant V_{IL}$
I_{IH}	High Level Input Current	-10	±0.1	10	μA	$V_{IN} \geqslant V_{IH}$
V_{IL}	Input Low Voltage		+1.2	+0.85	V	
V_{IH}	Input High Voltage	+2.0	+1.5		V	
V_{OL}	Output Low Voltage	0	0.03	+0.2	V	I_{OL} = 5mA
V_{OH}	Output High Voltage	V_{DD}-0.2	V_{DD}-.03	V_{DD}	V	I_{OH} = -5mA
I_{DD0}	Standby Current		2.0	4.0	mA	$V_{IN} \geqslant V_{IH}$, $V_{IN} \leqslant V_{IL}$, f = 0 MHz
I_{DD1}	Operating Current		75	105	mA	$V_{IN} \geqslant V_{IH}$ or $V_{IN} \leqslant V_{IL}$, f = 0.67 MHz [2]

A.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{SS} = 0V, Note 2

Symbol	Parameter	Limits Driving 4 2416's Min.	Typ.	Max.	Units
V_{OLT}	Transient Cross-Coupled Output Low Voltage	-0.8	±0.5	+0.8	V
V_{OHT}	Transient Cross-Coupled Output High Voltage	V_{DD}-0.8	V_{DD}±0.5	V_{DD}+0.8	V
t_{PWT}	Transient Cross-Coupled Output Pulse Width			Note 1	ns
Δt_D	Differential Delay of t_{DLH} and t_{DHL} for Drivers in the Same Package			15	ns
t_{DLH1}	Input Low to Output High Delay Time, ϕ_1 or ϕ_3	30	50		ns
t_{DHL1}	Input High to Output Low Delay Time, ϕ_1 or ϕ_3	30	50		ns
t_{TLH1}	Output Rise Time, ϕ_1 or ϕ_3	30	50	75	ns
t_{THL1}	Output Fall Time, ϕ_1 or ϕ_3	30	50	75	ns
t_{PLH1}	Input to Output Delay Plus Rise Time, ϕ_1 or ϕ_3		100	160	ns
t_{PHL1}	Input to Output Delay Plus Fall Time, ϕ_1 or ϕ_3		100	150	ns
t_{DLH2}	Input Low to Output High Delay Time, ϕ_2 or ϕ_4	30	55		ns
t_{DHL2}	Input High to Output Low Delay Time, ϕ_2 or ϕ_4	30	55		ns
t_{TLH2}	Output Rise Time, ϕ_2 or ϕ_4	30	55	85	ns
t_{THL2}	Output Fall Time, ϕ_2 or ϕ_4	30	55	90	ns
t_{PLH2}	Input to Output Delay Plus Rise Time, ϕ_2 or ϕ_4		110	175	ns
t_{PHL2}	Input to Output Delay Plus Fall Time, ϕ_2 or ϕ_4		110	170	ns

Notes: 1. The maximum t_{PWT} is the sum of the output transition time (rise or fall) plus 5ns.
2. Output Load = four 2416 clock inputs or equivalent per Figure 2.

CAPACITANCE* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	8	14	pf	f = 1 MHz, V_{bias} = 2V, V_{DD} = 0V

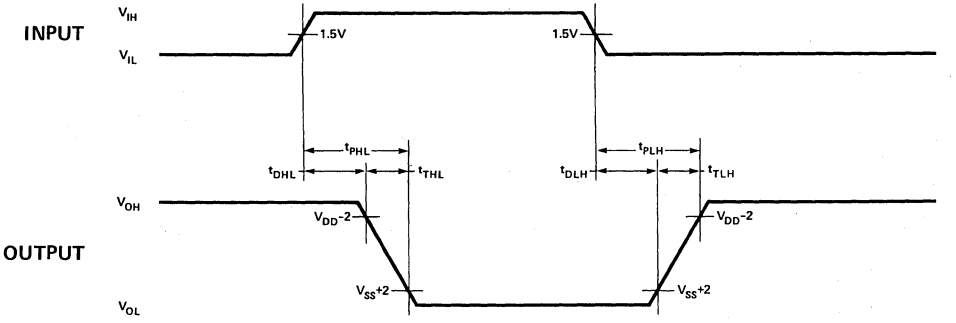
*This parameter is periodically sampled and is not 100% tested.

A.C. Test Conditions

1. TTL Input Levels = 0.4V to 2.4V
2. Output Load = Four 2416 clock inputs or equivalent per Figure 2
3. Cross Coupled Voltage Pulse Width measured at ± 0.4V and V_{DD} ± 0.4V

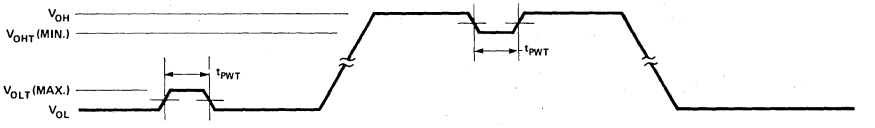
Waveforms

A. INPUT TO OUTPUT DELAY

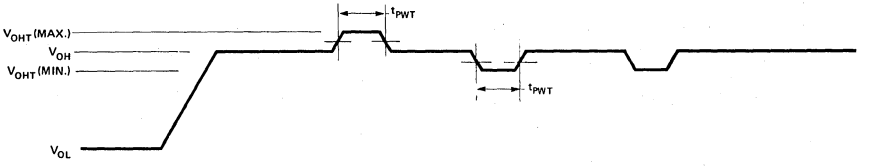


B. 5244 OUTPUT CROSS-COUPLED VOLTAGE (DRIVING FOUR 2416'S)

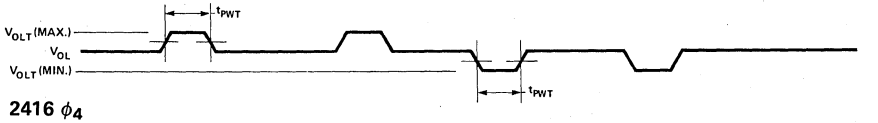
5244 OUTPUT DRIVING 2416 ϕ_1



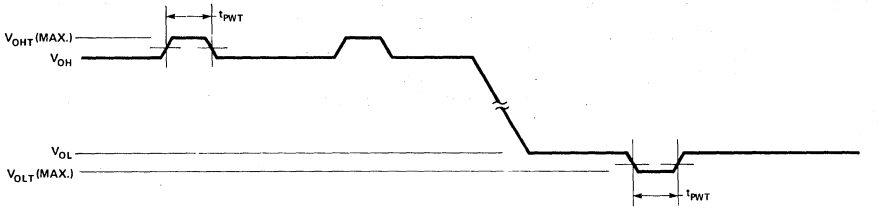
5244 OUTPUT DRIVING 2416 ϕ_2



5244 OUTPUT DRIVING 2416 ϕ_3

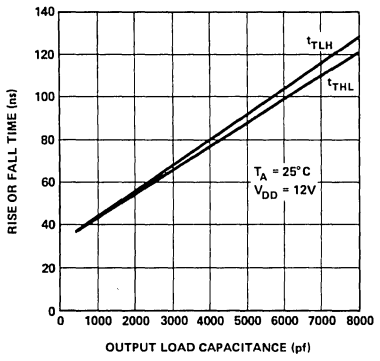


5244 OUTPUT DRIVING 2416 ϕ_4

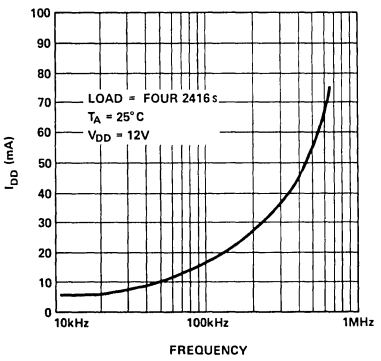


Typical Characteristics

OUTPUT RISE AND FALL TIME VS. CAPACITANCE



I_{DD} VS. FREQUENCY



Application Information

The 5244 is a TTL to MOS level converter designed to drive very high capacitive loads with no required additional external components. Its primary application is to drive the clock phase inputs of the Intel ® 2416, a 16,384 word x 1 bit charge coupled device.

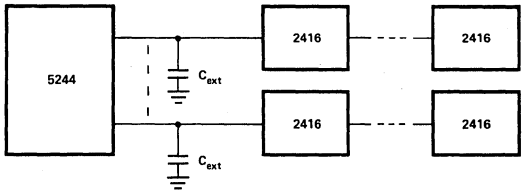
DRIVING THE 2416

The 5244 is designed to drive the clock phase inputs of four 2416s and meet or exceed the electrical specifications of these inputs. The 2416 clock specifications of special interest to the system designs are:

1. Clock transition time.
2. Clock to clock voltage coupling.

Clock Transition Control

The 5244 will meet the min/max clock transition time requirement of the 2416 when driving four 2416s. However, when driving less than four 2416s an external capacitor (C_{ext}) must be added to assure that the minimum clock transition time (30ns) is adhered to. The maximum clock transition time for the 5244 will not be exceeded if C_{ext} is chosen according to the recommendations in Figure 1.



C_{ext} = (4-N) C_ϕ
WHERE C_ϕ = TYPICAL 2416 INPUT CLOCK CAPACITANCE.
A VALUE FOR C_ϕ WITHIN THE RANGE OF 300pF TO 400pF WILL WORK FOR ALL CLOCKS, $\phi_1 \ldots \phi_4$.
N = NUMBER OF 2416s PER 5244 OUTPUT.

Figure 1. External Loading Requirements When Driving Fewer Than Four 2416s.

Clock to Clock Voltage Coupling

The equivalent circuit of the 2416 clock phase inputs is shown in Figure 2. The magnitude and duration of the cross-coupling are graphically presented in Waveform B and specified in the A.C. Characteristics. Figure 3, on the next page, shows the noise margin between these specifications and the 2416 input requirements.

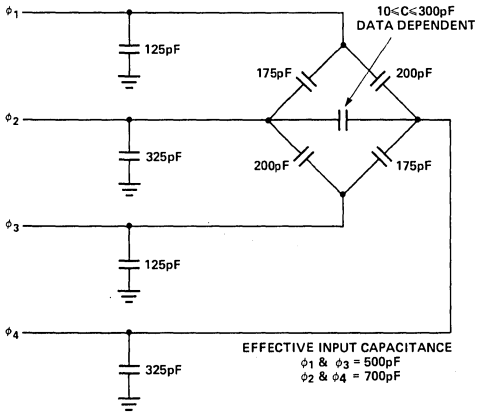


Figure 2. 2416 Equivalent Capacitance Circuit. (Maximum values shown.)

MEMORY SUPPORT

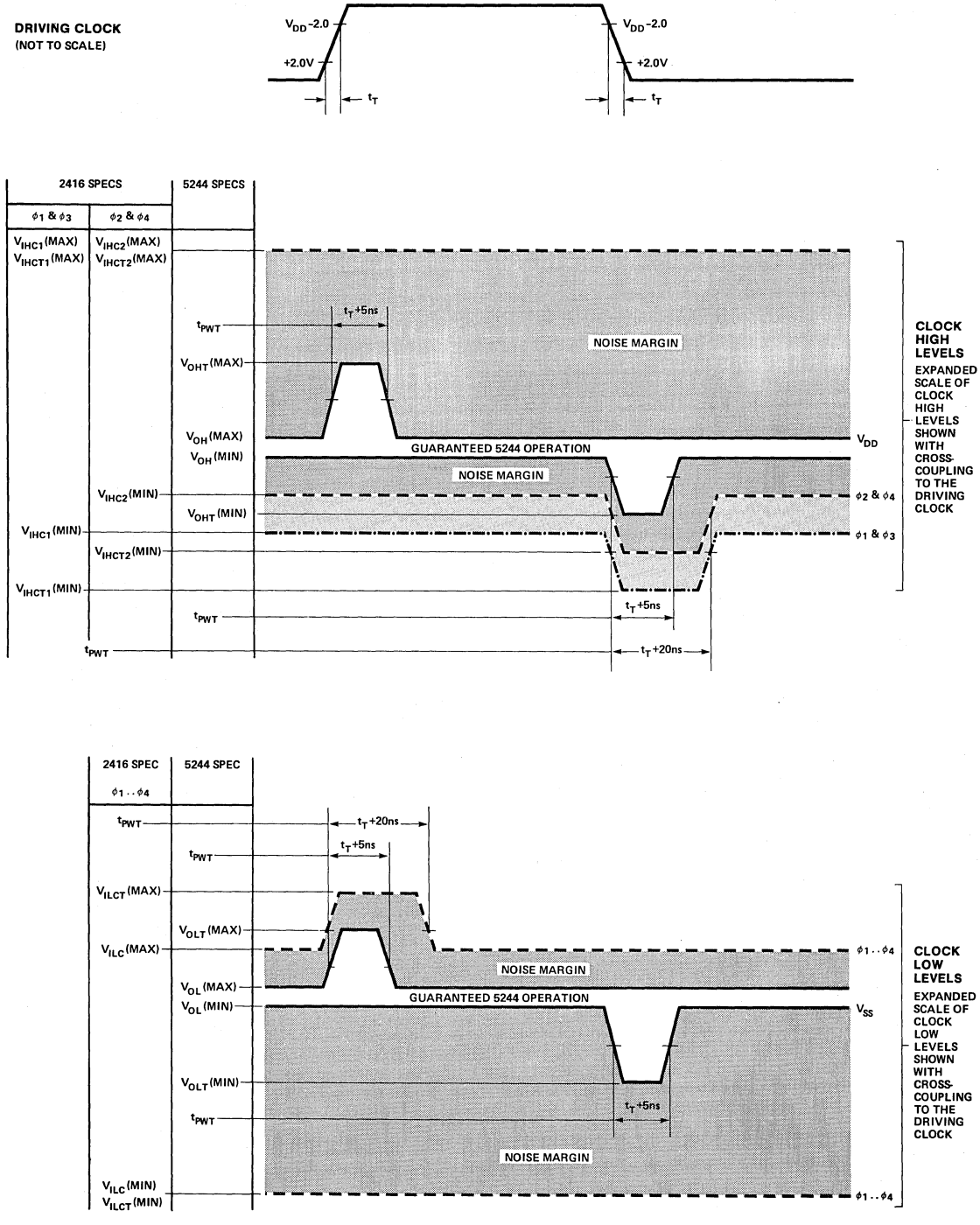
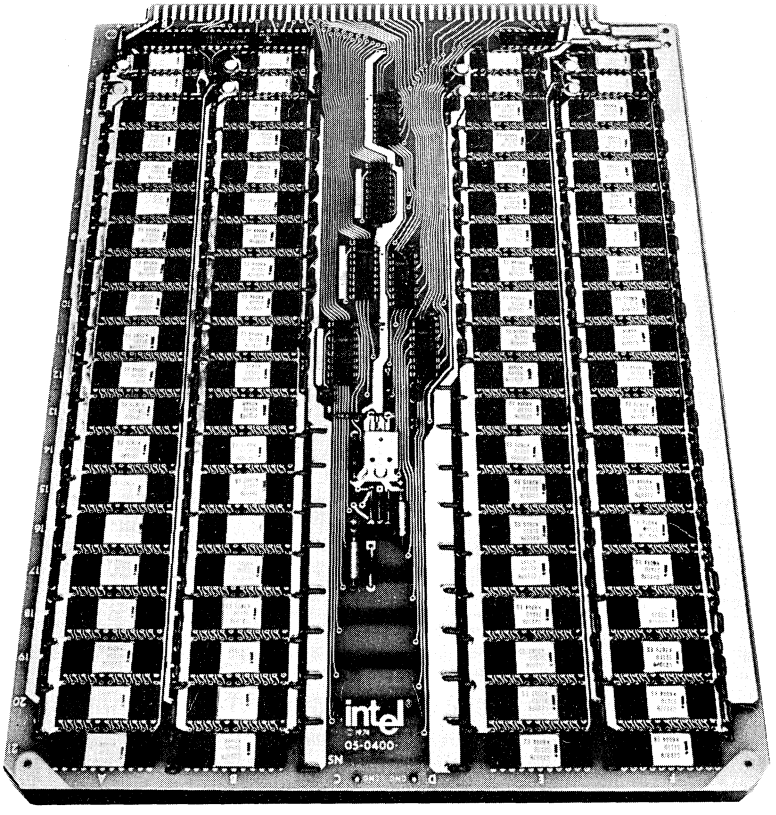


Figure 3. Noise Margins Between 5244 Output Specs and 2416 ϕ_1 . . . ϕ_4 Input Requirements.

6

MEMORY SYSTEMS

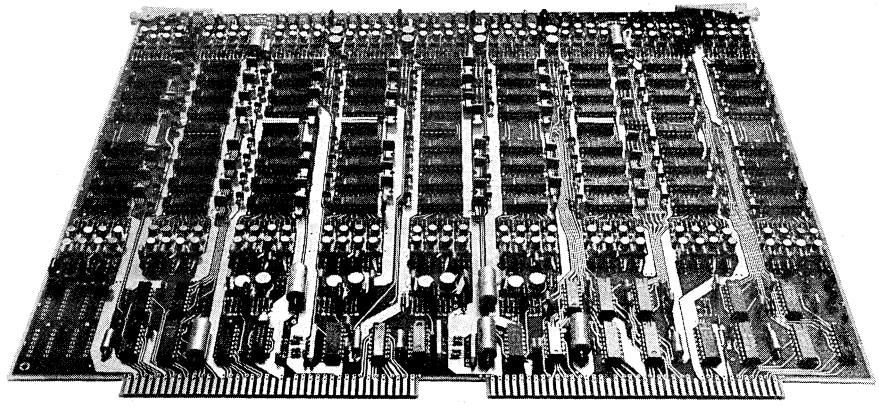


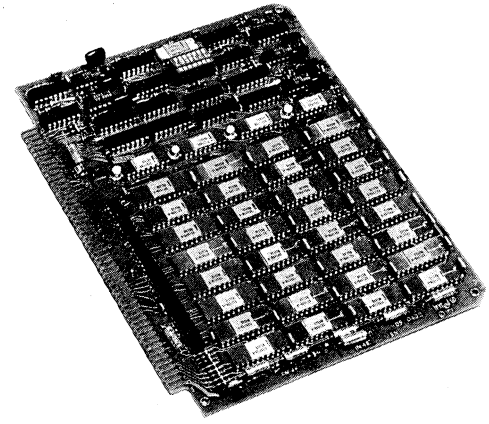
MEMORY SYSTEMS

Type	Description	No. of Words (Per Card)	Word Length (Bits)	Access Time	Cycle Time	Supplies (V)	Page
in-10	RAM System	8K	8–18	275 ns	450 ns	+23.2 +19.7 +5	6-4
in-26	RAM System	4K	4–10	375 ns	375 ns	+5	6-6
in-40	RAM System	32K	8–18	330 ns	500 ns	+5 –5	6-8
in-50	RAM System	1K	2–10	100 ns	100 ns	+5	6-10
in-60	Serial Memory System	20K	8–10	500 ns	N/A	+5	6-12
in-64	Serial Memory System	88K	1–2	60 ns	N/A	+5	6-14
in-65	Serial Memory System	131K	8–9	550 ns	N/A	+17 +12 +5 –5	6-16
in-4711	PDP-11 Add-in	16K	16–18	150 ns	520 ns	From PDP-11	6-18
in-4716	Interdata 7/16 and 7/32 Add-in	16K	17	300 ns	1000 ns	+15 +5 –15	6-20
in-477	CRT Refresh Memory	16K	16	600 ns	850 ns	+12 +5 –5	6-22
in-481	8008, 8080 RAM Memory	16K	8	450 ns	600 ns	+12 +5 –9	6-24

MEMORY SYSTEMS

Intel Memory Systems Division offers standard and custom memory systems ranging from single board assemblies to multi-mega byte systems. Advanced 1K, 4K RAMS along with 16K CCD Serial memory components are utilized for highest performance and lowest cost.

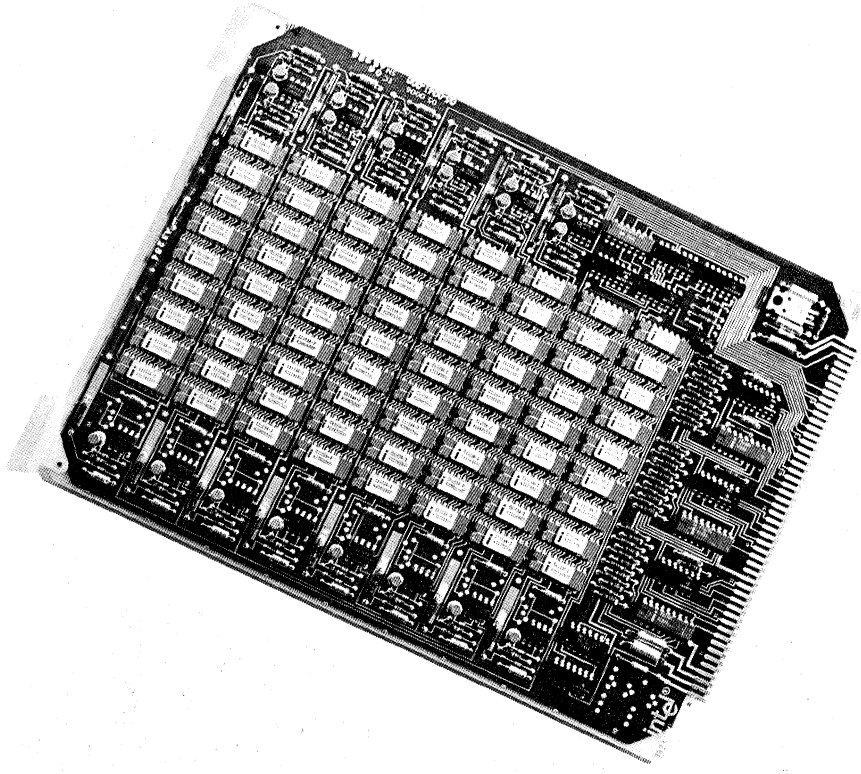




in-10

RANDOM ACCESS MEMORY SYSTEM

The in-10 represents the most economical approach to moderate size, high speed memory systems. The in-10 series of RAM systems is designed to provide high reliability and low price. This series features a basic 4K x 18 or 8K x 9 configuration consisting of two plug-in boards: A memory board (MU) and a control board (CU). The control board is capable of operating up to 32K words x 18 bits or 65K words x 9 bits (8 cards).



in-10 FEATURES:

- Low Cost Memory
- High Reliability
- Modular Expandability
- Module Interchangeability
- Automatic Refresh
- TTL Compatible
- Byte Control (2 Zones Maximum)
- Module Select
- Fast Cycle Time
- Low Power Requirements
- Compact Size
- Field Expandable
- Address Register
- Data Register (Optional)
- Basic System Available As 4K x 18 or 8K x 9

SPECIFICATIONS

Capacity:

1024, 2048, 4096, 8192 words expandable in cards to 32,768 x 18 or 65,536 x 9 capacity.

Word Length:

8, 9, 10, 12, 16 or 18 bits in a single memory card. Longer word lengths can be accommodated by combining memory cards.

Cycle Time: (Read, Write)

in-10A	450 nanoseconds
in-10	450 nanoseconds
in-12	675 nanoseconds
in-14	850 nanoseconds

Access Time: (Read)

in-10A	275 nanoseconds
in-10	325 nanoseconds
in-12	450 nanoseconds
in-14	500 nanoseconds

Dimensions:

Memory Board: (4K x 18 or 8K x 9)	8.175 Inches High 10.5 Inches Deep 0.5 Inches—Mounting Centers

To expand to 32K x 18 add 0.5 inches per memory card. Only one control card (CU) is needed for systems up to 32K x 18 or 64K x 9.

Memory System: (32K x 18)	8.175 Inches High 10.5 Inches Deep 5.0 Inches Wide

Mating Connector: See page 6-30.

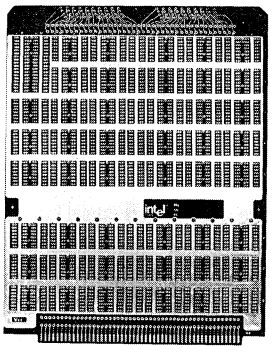
Operational Modes:

Read, Write
Read/Modify/Write (Optional)

Interface Characteristics:

TTL Compatible
Standard Input Lines:
- Cycle Initiate
- Byte Control
- Read/Write

Standard Output Lines:
- Data Available
- Memory Busy



UT-10/40 Series Interface Board

D.C. Power Requirements:

in-10:

Voltage	Regulation
+ 3.5V (Stacked on +19.7V)	±10%
+19.7V	±5%
+ 5.0V	±5%

57 Watts (operating 4K x 18), 25 Watts standby power (per each additional 4K)

in-10A:

57 Watts (operating 4K x 18), 7.5 Watts standby power (per each additional 4K)

in-12 & 14:

Voltage	Regulation
+ 3.5V (Stacked on +16.7V)	±10%
+16.7V	±5%
+ 5.0V	±5%

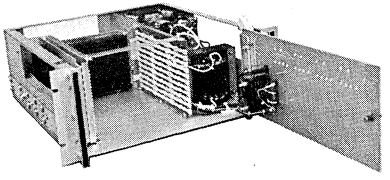
46 Watts (operating 4K x 18), 16 Watts standby power (per each additional 4K)

Environment:

Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating.

Special Options:

Intel offers this system mounted in a card chassis, or complete system. Options seen below, and others, can be found on pages 26 to 29.



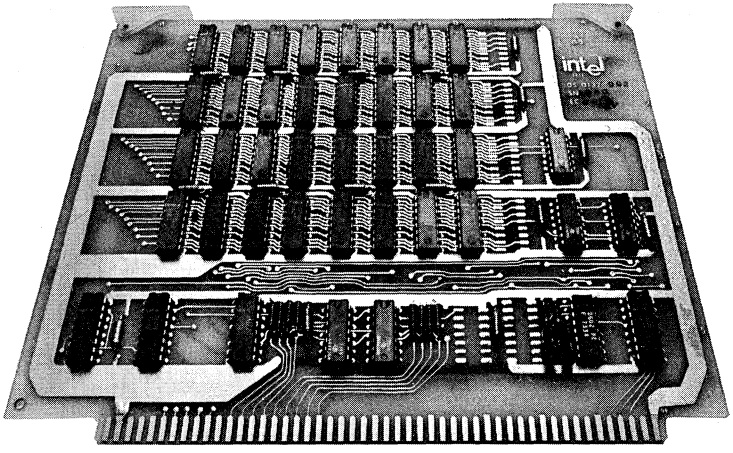
in-Minichassis

MEMORY SYSTEMS

in-26

RANDOM ACCESS MEMORY SYSTEM

The in-26 is an extremely easy memory system to use. The in-26 is a static memory system designed to meet the high reliability and low cost requirements of random access buffer storage applications. Featuring a complete memory system on a single PC board, this memory board has a maximum capacity of 4K x 10 and multiple cards can be used to configure systems up to a maximum capacity of 65K x 10. It can also be provided in smaller capacities by depopulating the memory boards. The compact size of this system makes it ideal for use as buffer storage for various computer peripheral applications. This memory system can be easily modified to interface with the Intel 4 and 8 bit micro processors, 4004, 4040, 8008 and 8080.



in-26 FEATURES:

- Low Cost Memory
- High Reliability
- Modular Expandability
- Module Interchangeability
- Fast Cycle Time
- Low Power Requirements
- TTL Compatible
- Compact Size
- Field Expandable
- One Power Supply Voltage
- Address Registers
- Single Board System
- Board Select

SPECIFICATIONS

Capacity:

1024, 2048, and 4096 words expandable to 65K words by the addition of memory cards.

Word Length:

4, 6, 8, 9, 10 bits per card. Longer words can be made by adding additional memory cards.

Cycle Time:

in-26	900 nanoseconds
in-26-1	650 nanoseconds
in-26-2	475 nanoseconds
in-26-3	375 nanoseconds

Access Time:

in-26	900 nanoseconds
in-26-1	650 nanoseconds
in-26-2	475 nanoseconds
in-26-3	375 nanoseconds

Dimensions:

Memory Board:	8.175 Inches High
(4K x 10)	6.0 Inches Deep
	0.5 Inches— Mounting Centers

Mating Connector: See page 6-30.

Operational Modes:

Read,Write

Interface Characteristics:

TTL Compatible—Open collector or terminated three-state

Standard Input Lines:

Cycle Initiate
Board Select
Read/Write
Byte Control

D.C. Power Requirements:

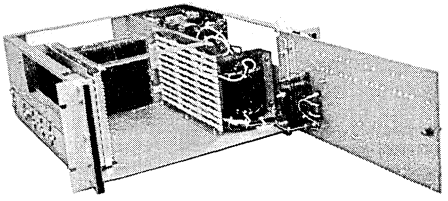
in-26:	+5.0V	±5%;	1.25 Amps Typical
			3.0 Amps Max.

Environment:

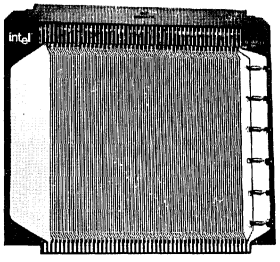
Temperature:	0°C to +50°C operating ambient
	−40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating.
	Up to 50,000 feet non-operating.

Special Options:

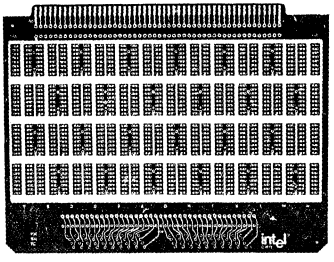
Intel also offers the in-26 mounted in a card chassis. This chassis is available in a variety of sizes and can be set up for future expansion of the memory without changing the basic chassis. Options seen below, and others, can be found on pages 26 to 29.



in-Minichassis



EX-26/50 Extender Board

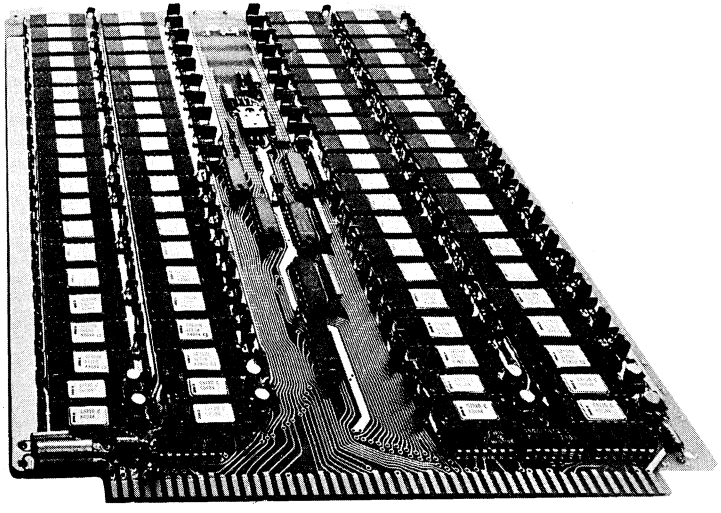


UT-26/50 Series Interface Board

in-40

RANDOM ACCESS MEMORY SYSTEM

The in-40 is one of the highest density memory systems now available. The system uses high performance Intel 2107B, a 4K RAM Memory component. Fast cycle and access times are provided along with this high density. The interchangeable memory unit (MU) allows expansion in increments of 16K x 18 or 32K x 9 with no adjustments. A single control unit (CU) handles up to 128K x 18 or 256K x 9 making this our lowest cost-per-bit storage available.



in-40 FEATURES:

- Low Cost Memory
- High Reliability
- High Density
- Modular Expandability
- Module Interchangeability
- Automatic Refresh
- Fast Cycle Time
- TTL Compatible
- Low Power Requirements
- Compact Size
- Field Expandable
- Byte Control (2 Zones Maximum)
- Module Select
- Address Register
- Data Register (Optional)
- Basic System Available As 16K x 18 or 32K x 9

SPECIFICATIONS

Capacity:

4096, 8192, 16,384, 32,768 words expandable in cards to 131,072 x 18 or 262,144 x 9 capacity.

Word Length:

8, 9, 10, 12, 16, or 18 bits in a single memory card. Longer word lengths can be accommodated by combining memory cards.

Cycle Time:

in-40	500 nanoseconds
in-42	550 nanoseconds
in-44	875 nanoseconds

Access Time:

in-40	330 nanoseconds
in-42	400 nanoseconds
in-44	480 nanoseconds

Dimensions:

Memory Board:	8.175 Inches High
(16K x 18 or 32K x 9)	10.5 Inches Deep
	0.5 Inches—Mounting Centers

Mating Connector: See page 6-30.

Operational Mode: Read (NDRO), Write

Interface Characteristics:

TTL Compatible

Standard Input Lines:

- Cycle Initiate
- Byte Control
- Read/Write

Standard Output Lines:

- Data Available
- Memory Busy

D.C. Power Requirements:

MU-40: Selected

Voltage	Current (Max.)	Regulation
+12.0V	1.9 Amps	±5%
+ 5.0V	1.2 Amps	±5%
− 5.0V	<10.0 Milliamps	±5%

Unselected

Voltage	Current (Max.)	Regulation
+12.0V	0.142 Amps	±5%
+ 5.0V	1.2 Amps	±5%
− 5.0V	<10.0 Milliamps	±5%

D.C. Power Requirements (cont.):

CU-40:

Voltage	Current (Max.)	Regulation
+5.0V	2.8 Amps	±5%
−5.0V	0.32 Amps	±5%

Environment:

Temperature:	0°C to +50°C operating ambient
	−40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating.
	Up to 50,000 feet non-operating.

Refresh:

The need for refresh cycles is self determined by the CU-40. For normally configured CU's, at the end of the refresh time out interval the CU either initiates a special refresh cycle or steals the next cycle for refresh if a regular memory cycle is in progress. An optional CU-40 configuration allows external control of refreshing to the extent that automatic cycle stealing is inhibited. At the end of the refresh time out, the CU asserts a refresh request signal that indicates a refresh cycle is required. At the user's discretion, a refresh grant signal is issued which then initiates a refresh cycle.

Special Options:

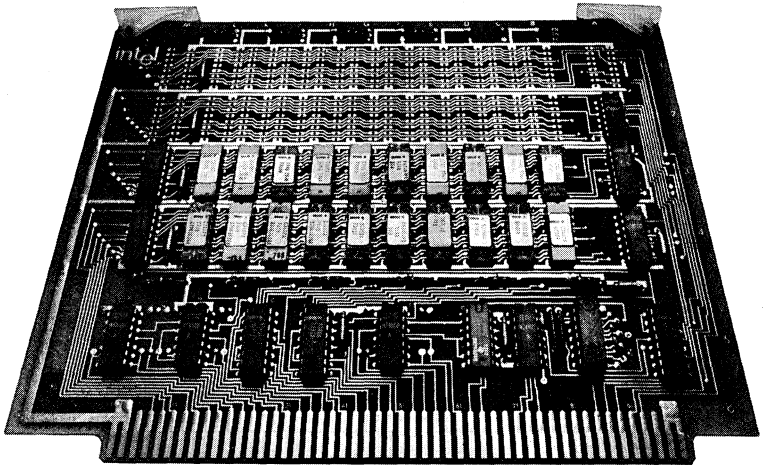
Intel offers the in-40 in a card chassis designed for mounting in 19″ and 24″ relay racks. UT-40 socket cards allow easy wire wrapping of custom interfaces in the card chassis. See pages 26 to 29 for more accessory information.

Another option is the in-41E Euroboard. Intel's Euroboard dimensions are 160mm high x 233.4 mm deep x 12.7 mm wide. See your local Intel representative for additional specifications.

in-50

RANDOM ACCESS MEMORY SYSTEM

The in-50 is designed to meet the needs of control memory, disk controllers, scratch pad and signal processing applications. The in-50 provides the fastest access and cycle times possible in a TTL compatible memory system. Utilizing Bipolar technology and solid-state integrated circuitry, this memory provides high reliability and performance at low costs. This memory system features a basic size of 1024 words by 10 bits per memory card. It can be expanded to any word or bit length by the use of additional memory cards. Each system includes all address and data registers.



in-50 FEATURES:

- Low Cost Memory
- High Reliability
- Modular Expandability
- Module Interchangeability
- Fast Cycle Time
- Low Power Requirements
- Compact Size
- Field Expandable
- One Power Supply Voltage
- Fully Buffered System
- Module Select
- Address Registers
- Data Registers
- Single Board System
- Open Collector Outputs
- TTL Compatible

SPECIFICATIONS

Capacity:

256, 512 and 1024 words per memory card. Larger sizes are feasible by the addition of memory cards.

Word Length:

2, 4, 6, 7, 8, 9, 10 bits per card. Longer words can be accomplished by the use of additional memory cards.

Cycle Time:

in-50	100 nanoseconds
in-52	150 nanoseconds

Access Time:

in-50	100 nanoseconds
in-52	150 nanoseconds

Dimensions:

Memory Board: (1K x 10)	8.175 Inches High 6.0 Inches Deep 0.5 Inches—Mounting Centers

Mating Connector: See page 6-30.

Operational Modes:

Read (NDRO), Write

Interface Characteristics:

TTL Compatible

Standard Input Lines:

Cycle Request
Read/Write

Standard Output Lines:

Data Available

D.C. Power Requirement:

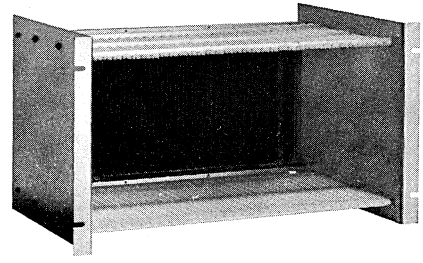
+5.0V ±5% 5.5 Amps per memory card

Environment:

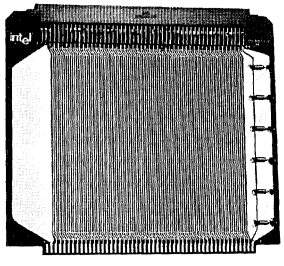
Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating.

Special Options:

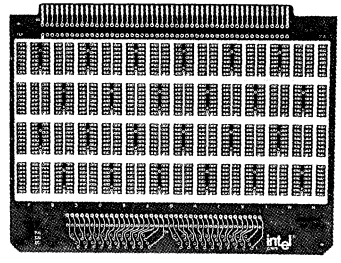
The in-50 is available in various word and bit lengths. The card chassis is completely wire wrapped with I/O connectors for mounting in 19″ relay racks. It can also be equipped with a power supply that is also mountable in a 19″ relay rack. Options seen below, and others, can be found on pages 26 to 29.



in-Unichassis



EX-26/50 Extender Board

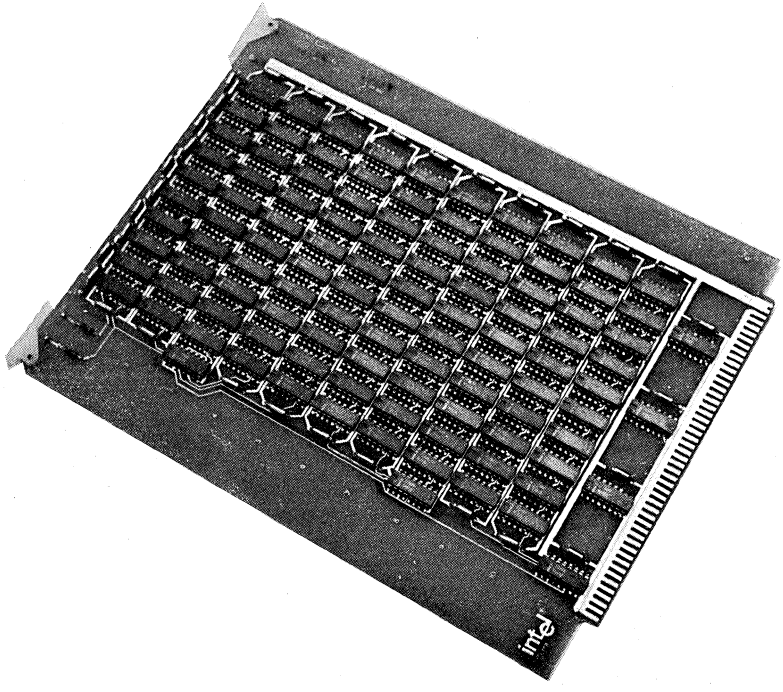


UT-26/50 Series Interface Board

in-60

SERIAL MEMORY SYSTEM

The in-60 is designed to meet the high reliability and low cost requirements of large volume storage and CRT refresh applications. The in-60 features the use of a single voltage power supply and MOS N-channel silicon gate technology. This system is available as a self-contained 20,000 words by 10 bits memory unit, or is expandable to virtually any size in either word or bit length by the use of additional memory cards. The in-60 is designed for replacement of small fixed head disks and for CRT refresh applications.



in-60 FEATURES:

- Low Cost Memory
- High Reliability
- Modular Expandability
- Module Interchangeability
- Field Expandable
- One Power Supply Voltage
- Compact Size
- Adjustable Clocking
- Fully Buffered
- Single Phase Clocking
- TTL Compatible
- Single Board System

SPECIFICATIONS

Capacity:

Up to 20,000 words per memory card. Larger sizes are capable by the addition of memory cards.

Word Length:

6, 7, 8, 9, 10 bits per memory card. Longer words are made by combining memory cards.

Clock Rate:	1 megaHertz to 25 kiloHertz
Access Time:	500 Nanoseconds
Dimensions:	8.175 Inches High 10.5 Inches Deep 0.5 Inches—Mounting Centers

Mating Connector: See page 6-30.

Interface Characteristics:

TTL Compatible

Data Input:

Up to 10 lines, single ended

Data Output:

Up to 10 lines, single ended

Data Input Control:

1 line (clock), single ended

D.C. Power Requirement:

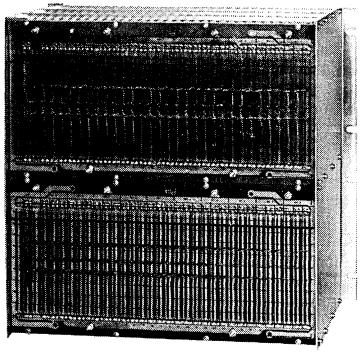
+5.0V ±5% at 7.0 Amps (Max.)

Environment:

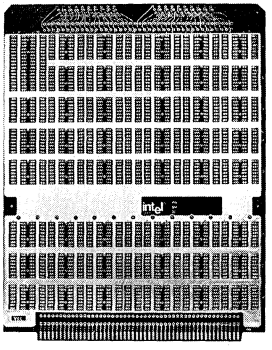
Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating.

Special Options:

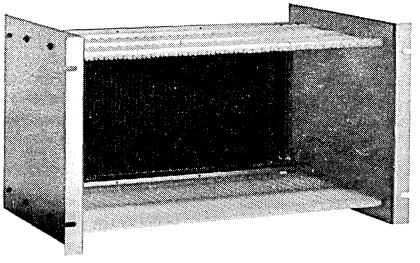
Intel also offers the in-60 mounted in a card chassis wire-wrapped to the size ordered. This chassis can be mounted in a 19″ relay rack. A power supply is also available for this system that will mount below the memory chassis. The power unit is modular and can supply up to a full card chassis of memory. A blower assembly is also available for this system. This blower assembly draws air from the front, back, or below to properly cool the memory card chassis. Options seen below, and others, can be found on pages 26 to 29.



in-CHS-II



UT-10/40
Series Interface Board

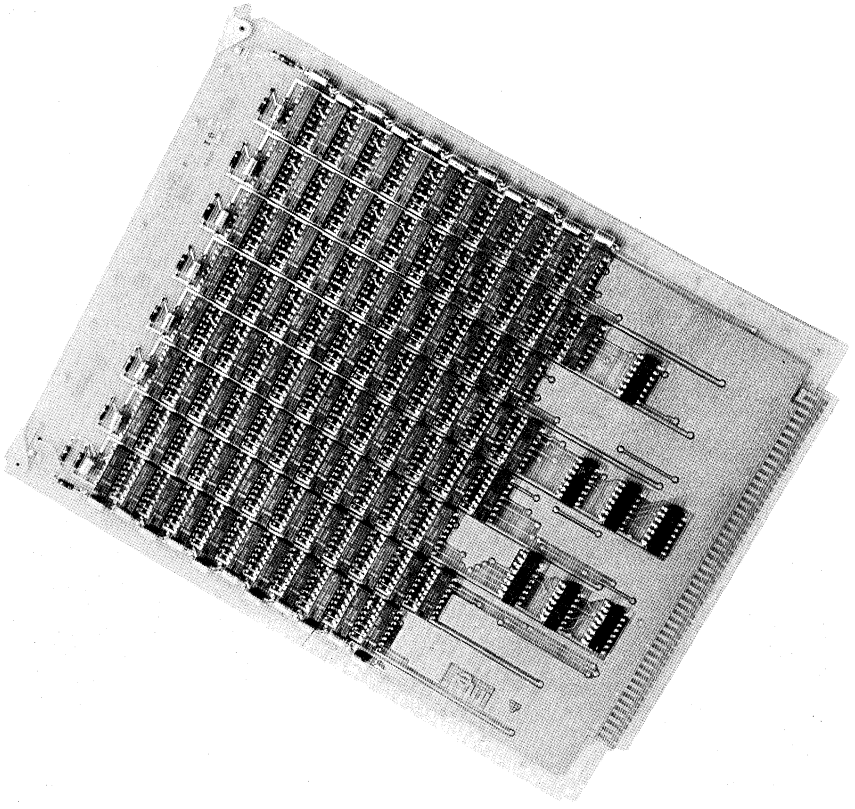


in-Unichassis

in-64

SERIAL MEMORY SYSTEM

The in-64 is designed to meet the high reliability and low cost requirements of large volume storage and CRT refresh applications. The in-64 features the use of a single power supply and MOS N-channel silicon gate technology. This system is available as a self-contained 88K words, with 1 bit or 2 bits per word depending on your requirements. It can be expanded to virtually any size, in either word or bit length, by the use of additional memory cards. The in-64 features a compact size, high reliability and ease of expansion.



in-64 FEATURES:

- Low Cost Memory
- High Reliability
- Modular Expandability
- Field Expandable
- One Power Supply Voltage
- Compact Size
- Adjustable Clocking
- Fully Buffered
- TTL Compatible
- Single Board System
- Single Phase Clocking

SPECIFICATIONS

Capacity:

Up to 88,000 words per memory card. Larger sizes are feasible by the addition of memory cards.

Word Length:

in-64	1 or 2 bits per memory card

Longer words are made possible by combining memory cards.

Clock Rate:

in-64:	10 MHz to 200 KHz

Access Time:

in-64	60 nanoseconds

Dimensions:

8.175 Inches High
10.5 Inches Deep
0.5 Inches—Mounting Centers

Mating Connector: See page 6-30.

Interface Characteristics:

TTL Compatible
Data Input:

in-64	2 lines, single ended

Data Output:

in-64	4 lines, single ended (2 Data Out, +2 Data Out)

Data Input Control:

2 lines (clock), single ended
(Collect/Recirculate, Clock)

D.C. Power Requirement:

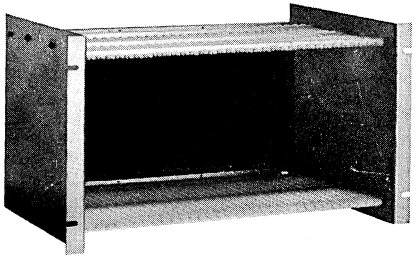
+5.0V	±5% at 6.0 Amps (Max.)

Environment:

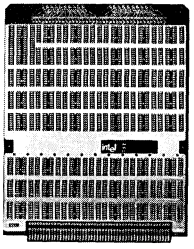
Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating.

Special Options:

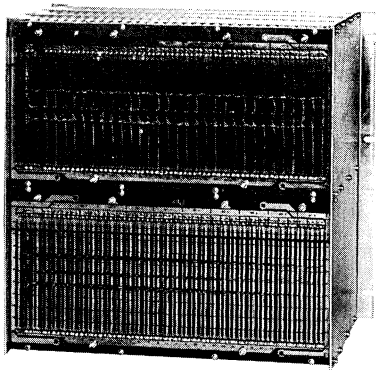
Intel also offers the in-64 mounted in a card chassis wire-wrapped to the size ordered. This chassis can be mounted in a 19″ relay rack. A power supply is also available for this system that will mount below the memory chassis. The power unit is modular and can supply up to a full card chassis of memory. A blower assembly is also available for this system. This blower assembly draws air from the front, back, or below to properly cool the memory card chassis. Options seen below, and others, can be found on pages 26 to 29.



in-Unichassis



UT-10/40
Series Interface Board



in-CHS-II

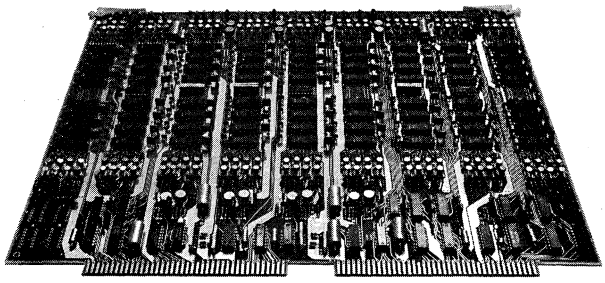
in-65

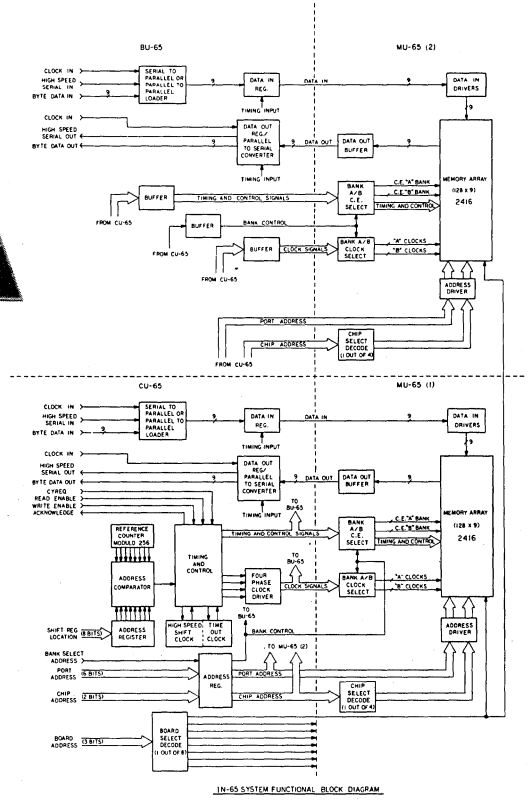
CCD MEMORY SYSTEM

The in-65 is a very economical CCD memory system designed around the Intel 2416. This product is best described and utilized as a Block-Oriented Random Access Memory. The system can be used to randomly address blocks of data and then transfer data sequentially within the data block at a very high data rate.

The system consists of three board types: The memory unit (MU-65), the control unit (CU-65), and the buffer unit (BU-65). The memory unit has a maximum capacity of 1,179,648 bits and is configured as 128K x 8 or 128K x 9 bits. The 9th bit can be either a data or parity bit. The CU-65 provides all interface, timing and control logic for up to 8 MU-65's. The BU-65 is synchronized to the CU-65 and provides for word length expansion.

The large capacity, high performance characteristics and economy of the in-65 make it ideally suited for disc and drum replacement, magnetic tape loop replacement and large CRT refresh applications.





IN-65 SYSTEM FUNCTIONAL BLOCK DIAGRAM

in-65 FEATURES:

- Low Cost
- Short Latency Time (125 μsec. ave.)
- High Data Rate (550 nano sec. per word)
- Randomly Accessible Data Blocks
- High Reliability
- High Density
- Simple Asynchronous Interface
- Fully Buffered
- Modular Expandability
- Module Interchangeability
- Options:
  - Byte Parity
  - Address Monitor Outputs

SPECIFICATIONS

Capacity:

Basic MU-65 capacity is 131,072 words. The system is expandable in cards to 1,048,576 words while using only one CU-65.

Word Length:

Basic word length is 8 or 9 bits, and is expandable in multiples of 8 or 9 bits by addition of BU-65's to a maximum of 72 bits.

Shift Rate:

825 ns when seeking new random address
10 μsec when in standby for data retention

Data Transfer Rate:

10 μsec to 550 nsec (per 9 bit byte or word)
16.4 megahertz (serial transfer) for one MU-65

Dimensions:

All cards (MU-65, CU-65, BU-65)	15.0 inches high 12.0 inches deep 0.625 Inches—Mounting Centers

Operational Modes:

Read (NDRO)	Serial bits, paralleled bytes or words
Write	Serial bits, paralleled bytes or words

Interface Characteristics:

TTL Compatible, Asynchronous

D.C. Power Requirements:

MU-65 (max)		Operating (max shift rate)	Standby or min. shift rate
+17V DC	±5%	at 2.8 amps	0.4 amps
+12V DC	±5%	at 2.8 amps	0.4 amps
− 5V DC	±5%	at 2.8 amps	0.4 amps
+ 5V DC	±5%	at 0.75 amps	0.75 amps
CU-65 (max)			
+5V DC	±5%	at 5.0 amps	
−5V DC	±5%	at 0.4 amps	
BU-65 (max)			
+5V DC	±5%	at 3.0 amps	
−5V DC	±5%	at 0.3 amps	

Environment:

Temperature:	0°C to +50°C operating ambient
	−40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
	0 to 10,000 feet operating
	Up to 50,000 feet non-operating

Special Options:

Intel offers a broad line of accessories designed specifically for use with the in-65. This includes backplanes, custom interface card, chassis, power supplies and cooling units. These units are available for 19″ and 24″ standard racks.

in-4711

PDP-11 ADD-IN SEMICONDUCTOR MEMORY

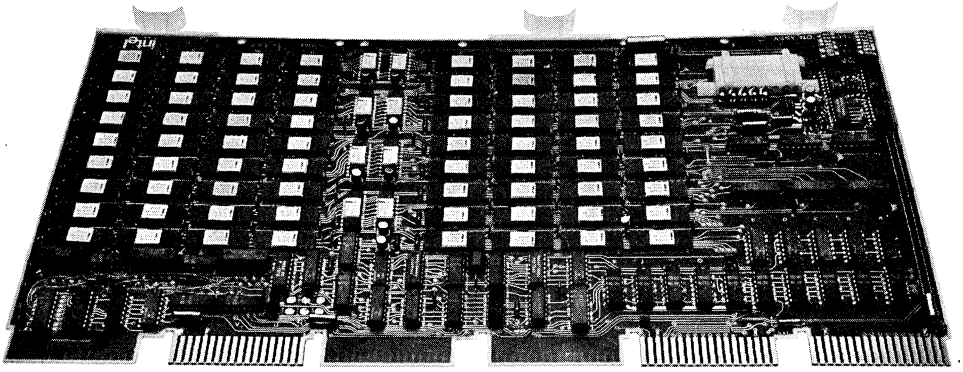
The Intel in-4711 is designed for use in all models and configurations of the DEC PDP-11® computer family able to accommodate a "Hex Height" memory card and its associated options. It utilizes the Intel 2107B 4K dynamic RAM component. The 16K x 16 (18 bit optional) memory and all refresh and control circuitry are contained on a single PC card. Power conversion can be done either with a separate "Quad Height" DC to DC PC regulator card that provides power for up to four in-4711's or with an on-board DC to DC converter for each in-4711-1. The in-4711 and in-4711-1 can be used in a system with 8K core modules, with compatability with 16K core modules available for volume requirements.

Active power consumption at 30 watts is less than half that of the core memory it replaces. This allows wider operating margin on the power supply as well as a cooler running overall system. The system is 3-5 times more dense than core.

Read and write cycle times of 520 nanoseconds allow significant speed improvement. Interleave operation with two memories is possible for maximum throughput.

Quick address select changes are possible through the use of on-board DIP switches.

Write access time of 150 nanoseconds frees up the unibus at least 50 nanoseconds faster. Byte operation is also standard.



in-4711 FEATURES:

- Low Cost Memory
- Fast Cycle Time
- Low Power Requirements
- High Reliability
- Module Interchangeability
- Modular Expandability
- Compact Size
- Byte Operation
- Address Select Switches
- Two Way Interleave (16K Boundaries)
- Compatible with both DEC PDP-11® Memory Management and Byte Parity Options

SPECIFICATIONS

Capacity:

8K and 16K words per board

Word Length:

16 or 18 bits

Cycle Time:

Read	520 nanoseconds
Write	520 nanoseconds

Access Time:

Read	450 nanoseconds
Write	150 nanoseconds

Dimensions:

Memory Board (Hex)	15.4	Inches High
	8.4	Inches Deep
	0.375	Inches Wide
*DC/DC Converter Board (Quad)		
	10.875	Inches High
	0.84	Inches Deep
	0.375	Inches Wide

Operational Modes:

Read Word
Write Word
Read Byte
Write Byte

*Converts 8K core voltages to the required in-4711 voltages.

Interface Characteristics: (Unibus Compatible)

TTL Compatible
Standard Input Controls:
- Cycle Initiate (MSYN)
- Byte Select (CO)
- Read/Write (CI)
- Address Lines (AO-A17)
- Data Lines (DO-D15)
- Slave Sync (SSYN)
- Initialize (INIT)

D.C. Power Requirements:

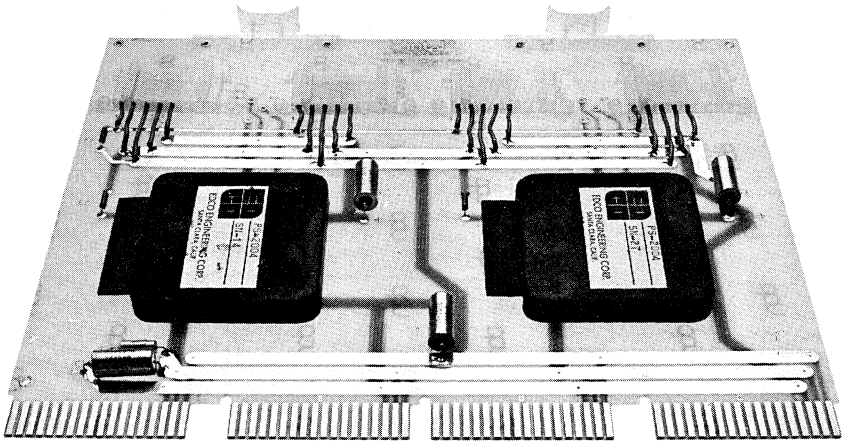
17.5 Watts	Typical
29.4 Watts	Max.

Environment:

Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating.

Special Options:

16K core compatibility available on a custom basis for volume requirements.



DC/DC CONVERTER BOARD (R/11)

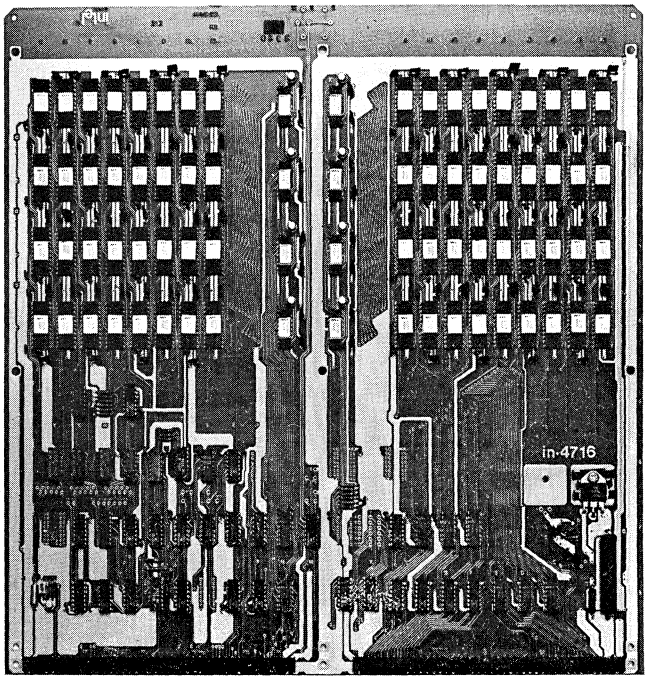
in-4716

7/16 ADD-IN SEMICONDUCTOR MEMORY

The Intel in-4716 is designed to be plug-to-plug compatible with the Interdata® MODEL 7/16 BASIC Minicomputer. The in-4716 consists of one printed circuit card which contains a 16K word by 17 bit memory storage area, plus all control, refresh and interface logic needed to operate the memory unit.

The Intel 2107B 4K dynamic RAM is utilized in the in-4716, thereby providing non-destructive data read out, high density and high reliability all at a very attractive price.

The worst case active power consumption for the in-4716 is 36 watts which is less than half that of the core memory it replaces. This allows wider operating margins on the power supply, as well as a cooler running overall system.



in-4716 FEATURES:

- Low Cost Memory
- Fast Cycle Time
- Low Power Requirements
- High Reliability
- Module Interchangeability
- Modular Expandability
- Compact Size
- Single Board System
- Byte Operation
- Address Select Switches

SPECIFICATIONS

Capacity:

8192, 12288 & 16384 words. Expandable to 32768 words by addition of a second memory card.

Word Length:

17 bits (including parity)

Cycle Time: One Microsecond

Access Time: 300 nanoseconds

Dimensions:

Memory Board (16K x 17)	14.88 Inches High 15.38 Inches Deep 0.40 Inches Wide

Operational Mode:

Clear/Write
Read/Restore
Refresh

Interface Characteristics:

TTL Compatible
Data Input:
Memory Data 00-16 (MD000-160) 17 lines
16 lines data, 1 line (16) parity
Data Output:
Memory Strobe 00-16 (MS000-160) 17 lines
16 lines data, 1 line (16) parity
Address Input:
Memory address 00-14 (MA000-140) 15 lines
Control Signals:
All control lines are single-ended
Standard Input Lines:
Enable ϕ
Access Control ϕ
Early Read ϕ
Temperature Sensing A
Standard Output Lines:
Request ϕ
Access Control ϕ
(to other devices)
Temperature Sensing B

D.C. Power Requirement:

Voltage	Selected Current (Max.)	Unselected Current (Max.)	Regulation
+15.0V	1.3 Amps	0.2 Amps	±5%
+ 5.0V	3.0 Amps	3.0 Amps	±5%
−15.0V	85.0 Milliamps	85.0 Milliamps	±5%

Environment:

Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 50,000 feet non-operating

Refresh:

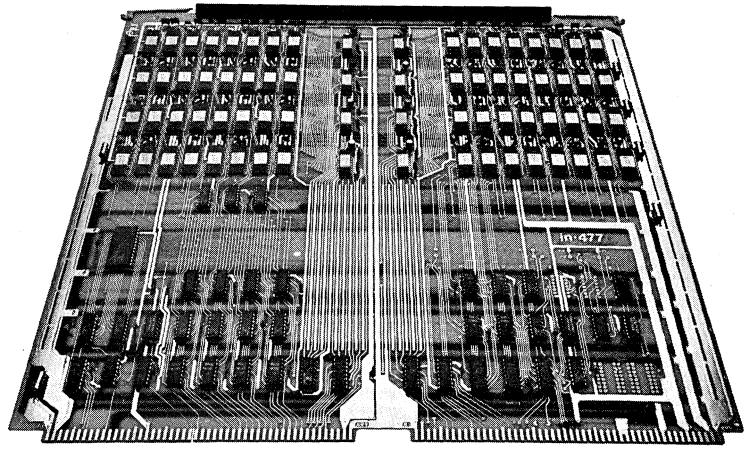
Refresh cycles are requested by the memory which time out intervals of 30 microseconds, ±10% (i.e., 1/64th of the memory retention time).

The Refresh cycle is initiated after the memory sends a Request signal to the processor. The next enable pulse is used to initiate a Refresh cycle, and the following ERO (Early Read signal) generates the cycle. A Refresh cycle is identical to a bus cycle, except that all memory chips on the memory card are enabled at the same time.

in-477

CRT DISPLAY RANDOM ACCESS MEMORY SYSTEM

The in-477 memory card is designed for storage and retrieval of digital video image data. Each card has a capacity of 256K (K = 1024) bits, which will drive a 512 x 512 CRT display. Cards may be operated in parallel to create a gray scale or multi-color displays. The card may be operated in a single bit per cycle serial mode, or a sixteen bit parallel mode. The card contains a sixteen bit parallel-to-serial register with external clocking and loading, to permit a serial bit read out at higher speeds than the normal card cycle time. Refreshing of the data in the n-channel MOS RAM's is normally achieved by sequential scanning of the memory for display refresh purposes. For special applications, the card can be refreshed externally at a rate of 64 times every 2 millisec, rather than 256 times every 2 millisec during the normal display refresh scan. This is accomplished by refreshing one row in all 64 RAM's on the card at once. A clear memory mode allows setting all memory locations to either a one or zero state in a simplified manner, if desired for initialize, reset, erase or other purposes.



in-477 FEATURES:

- Low cost 2107 4K RAM utilized
- Customer controlled refresh
- Paralleled and serial word and single bit modes of operation
- Allows RANDOM INSTANTANEOUS up dating of data
- Single boards can be used for character/graphic displays
- Multiple boards can be used for Gray scale and color displays
- Designed for use with 512 x 512 CRT MATRIX
- Simplified clear/erase memory mode
- Multiple speeds available by selecting 2107 components

SPECIFICATIONS

Capacity:

256K bits, organized as 16K x 16, or 256K x 1

Cycle Time: 850 nanoseconds

Access Time: 600 nanoseconds

Retention Time: Two milliseconds

Dimensions:

Memory Board	15.0 Inches High 15.0 Inches Deep 0.5 Inches— Mounting Centers

Mating Connectors:

Contact Factory

Operational Mode:

Write Word	(Parallel 16 bit data word transfer)
Read Word	(Parallel 16 bit data word transfer)
Write Bit	(Single bit data transfer)
Read Bit	(Single bit data transfer)
Read Word	(Serial 16 bit data word transfer)
Clear Set	

Interface Characteristics:

Address Input: 18 lines (TTL)

Data Input/Output:

16 lines for parallel word modes, 1 line for serial word mode, plus 1 line for single bit modes, all open collector, bidirectional lines

Serial Output (High Speed):

1 line, TTL active pull up/pull down

Control Input Lines:

Clock enable
Write enable
Word/Bit select
Mode enable
Card select
Write time gate
Clear memory enable
Shift register load
Serial shift clock

D.C. Power Requirement:

Voltage	Selected Current (Max.)	Regulation
+ 5.0V	3.00 Amps	±5%
+12.0V	1.50 Amps	±5%
− 5.0V	0.05 Amps	±5%

Environment:

Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	Up to 10,000 feet operating Up to 50,000 feet non-operating

Interface Voltages:

TTL Levels for all inputs and outputs

Special Options:

Access and cycle times of 280 nanoseconds and 450 nanoseconds respectively can be provided on a custom basis for volume requirements. (Note: these times allow 25 nanoseconds address settling time prior to starting a memory cycle.)

in-481

16K × 8 MICROPROCESSOR COMPATIBLE MEMORY SYSTEM

The in-481 is a 16K x 8 Random Access Memory that utilizes the Intel 2107B 4K Dynamic RAM chip. The memory and all refresh and control circuitry are on one PC board. The in-481 is expandable to a maximum of 64K x 8 by the use of four memory cards. The in-481 card is designed to interface directly with the IMM8-82 and the IMM8-83 CPU cards. Since the characteristics of these two cards are governed by either the 8008 or the 8080 microprocessors, it is also possible to use the in-481 with any CPU using these devices. The physical size of the in-481 is the same as the IMM Series. The address, data I/O, and power pin-outs are the same as the IMM6-28.

Applications*

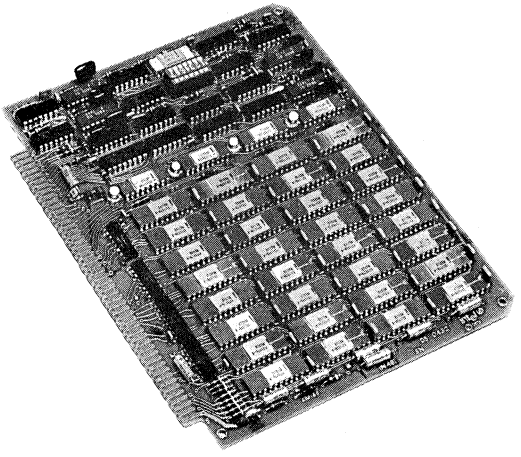
8008

When using the in-481 in an 8008 or 8008-1 microprocessor based system, the access and cycle times are such that WAIT states need not be entered. All refresh, write and read cycle requests are synchronized to specific CPU states and requests. This means that the in-481 is totally transparent to the CPU. During normal CPU operation all refreshing is done during the T_1 state of the 8008; during a HALT or HOLD state the memory refresh is synchronized to the ϕ_1 clock and occurs every 7.5 μsec. It should be noted, that a power-up reset circuit initializes all control circuitry on the in-481.

8080

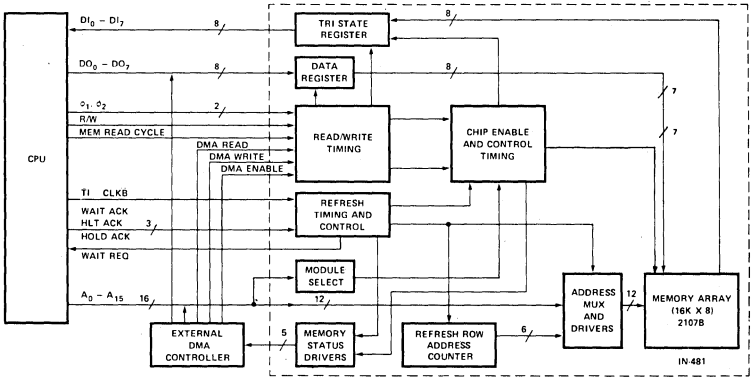
When using the in-481 in an 8080 microprocessor based system, the memory components used are faster in both cycle and access times in order to minimize the total number of WAIT cycle requests. All refresh, read and write cycle requests are again synchronized to specific CPU states or requests. Because of the 2.0 μsec instruction cycle time of the 8080, a single WAIT state or a possible double WAIT state is required during memory refresh. A memory refresh is initiated once every 31 μsec and it is synchronized to the positive edge of SYNC during the T_1 state. Normally a single WAIT state between T_2 and T_3 states is required if the memory is in the

*While the in-481 and in-481-1 are designed to work with the IMM8-82 and IMM8-83, they are not intended for use in the INTELLEC 8/MOD8 or INTELLEC 8/MOD80 since the current requirements of the in-481 and in-481-1 exceed the 60mA capacity of the INTELLEC +12V power supply.



in-481 FEATURES:

- IMM8-82 and IMM8-83 Compatible
- Automatic Refresh
- Modular Expandability
- Module Interchangeability
- Very High Density
- Board Select
- On Board 4K Address Select
- On Board 4K Enable/Disable
- Input and Output Data Registers
- Low Standby Power



Applications (Continued)

process of performing a read operation. If, however, a write cycle had been initiated during T_3 of the previous subcycle a double WAIT state is requested by the in-481. During the HOLD and HALT states, the refresh requests are synchronized to the ϕ_1 clock and they occur with a period of 25 μsec. It should be noted again that the power-up reset circuit initializes all control circuitry.

DMA

A DMA option is made possible in both 8008 and 8080 systems by means of the HOLD features. The HOLD ACK signal in both the IMM8-82 and IMM8-83 frees the control lines of the in-481 and the in-481-1. This signal is also used by the in-481 to disable the MEM READ CYCLE control input thereby enabling DMA control of the memory. Since refresh is synchronized to the ϕ_1 clock, and since additional state lines are brought out from the in-481, an access control circuit can be implemented to perform DMA. After completion of DMA, the HOLD and WAIT requests to the CPU card are disabled, and memory operation proceds as normal.

SPECIFICATIONS

Dimensions:

8.00 inches x 6.18 inches with 0.5 inch mounting centers.

Capacity:

16K x 8 expandable to 64K x 8 by use of four memory cards

Cycle Time:

in-481	1100 nanoseconds
in-481-1	600 nanoseconds

Access Time:

in-481	650 nanoseconds
in-481-1	450 nanoseconds

Power:

+5V	1.0A
+12V	0.9A
−9V*	30mA

* (−9V is zenered to −5V; optional −5VDC at 5mA)

Operational Modes:

Read (NDRO)
Write

Environment:

Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 50,000 feet non-operating

Connector Type:

Amp	1-67878-0
Winchester	HW50D0111
Viking	3VH50/ICN5
Sylvania	7900-0281-X

PIN NO.	8008	8080
1		
2		
3	GND	GND
4	GND	GND
5	WAIT ACK	WAIT ACK
6	TI	CLK B
7	DMA READ	DMA READ
8	PWR RESET	PWR RESET
9	*WE	*WE
10	NC	ϕ2
11	MAD 0	MAD 0
12	MAD 1	MAD 1
13	MAD 2	MAD 2
14	MAD 3	MAD 3
15	MAD 4	MAD 4
16	MAD 5	MAD 5
17	MAD 6	MAD 6
18	MAD 7	MAD 7
19	MAD 8	MAD 8
20	MAD 9	MAD 9
21	WAIT REQ	WAIT REQ
22		
23	MDI 0	MDI 0
24	DB 0	DB 0
25	MDI 1	MDI 1
26	DB 1	DB 1
27	MDI 3	MDI 3
28	DB 3	DB 3
29	MDI 2	MDI 2
30	DB 2	DB 2
31	MDI 5	MDI 5
32	DB 5	DB 5
33	MDI 4	MDI 4
34	DB 4	DB 4

PIN NO.	8008	8080
35	MDI 7	MDI 7
36	DB7	DB 7
37	MDI 6	MDI 6
38	DB 6	DB 6
39	SYS ENC	SYS ENC
40		
41	ADD ENA	ADD ENA
42	ADD ENB	ADD ENB
43	−9V	−9V
44	−9V	−9V
45	DMA READ ENABLE	DMA READ ENABLE
46	HOLD ACK	HOLD ACK
47		
48		
49	+12V	+12V
50	+12V	+12V
51		
52		
53		
54		
55		
56		
57		
58		
59	MAD 13	MAD 13
60	MAD 12	MAD 12
61		
62		
63	MA 14	MA 14
64		
65	MAD 15	MAD 15
66	MAD 14	MAD 14
67	DB IN	MEM READ CYC
68	MA 15	MA 15
69		

PIN NO.	8008	8080
70		
71	*READ	*READ
72		
73	HALT ACK	HALT ACK
74	SYNCA	DMA ϕ2 DISABLE
75		
76		
77		
78		
79		
80		
81		
82		
83		
84		
85	*REF	*REF
86		
87	*BUSY	*BUSY
88	*ENREF	*ENREF
89		
90		
91	GND	GND
92	GND	GND
93		
94	MAD 11	MAD 11
95	R/W	R/W
96	MAD 10	MAD 10
97		
98	ϕ1	ϕ1
99	+5	+5
100	+5	+5

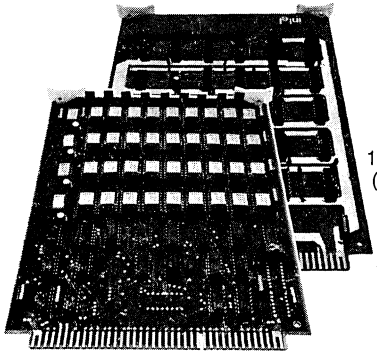
*Status signals from in-481.

MEMORY SYSTEMS

CUSTOM MEMORY CARDS

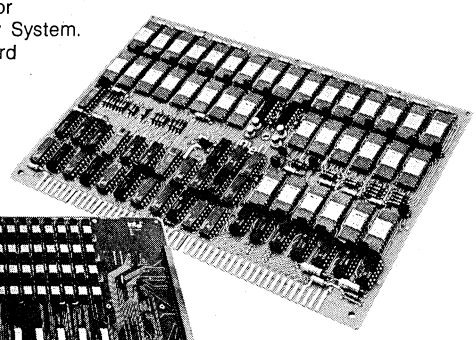
The following are examples of custom memory systems that have been designed exclusively for various OEM customers. These cards vary greatly in size, configuration and usage. Each card was designed to meet the individual needs of an OEM customer. In each case, our staff met the particular electrical, mechanical and environmental constraints placed on the card. In each case our staff's background and knowledge of semiconductor memories produced smooth production flow, reliable products and on-time deliveries that met the specifications.

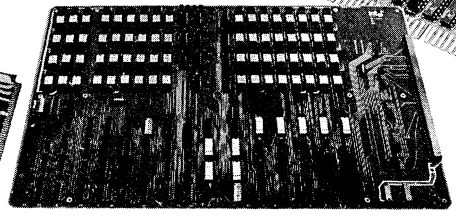
Intel's custom board capabilities are not limited to 4K RAM components. Custom boards have been designed around almost every serial, RAM, ROM and PROM component manufactured by Intel. When Intel plans a new component, Memory Systems is enlisted to design a system and evaluate the prototypes long before the component is announced. A custom board customer can beat his competition to the delivery of a new system by using the first experienced systems designers with that component: Intel Memory Systems.



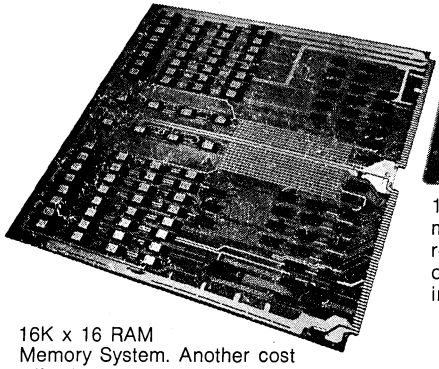
16K x 8 Two Card Microprocessor (Intel 8080) Compatible Memory System. A single timing and control card operates up to four memory cards thus reducing overall memory systems cost.

8K x 18 Memory System with on-board byte control logic and external timing and refresh control. Card is designed to replace an expensive core memory used with a custom-designed processor.

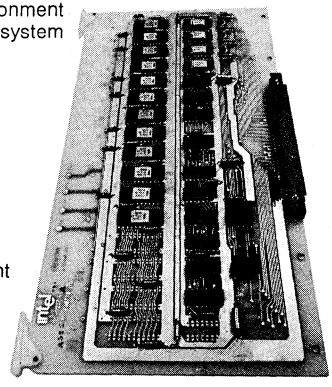




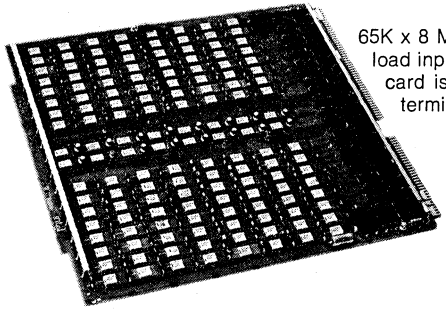
16K x 17 RAM Memory System used by a major industrial giant with stringent reliability requirements in the demanding environment of a numerical control application. This system includes a power save feature.



16K x 16 RAM Memory System. Another cost effective use of our 4K chip design for a CRT type application.



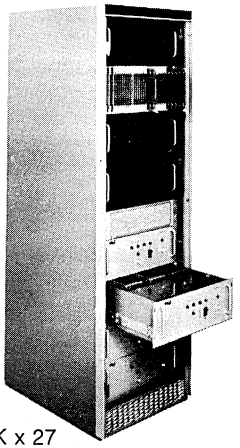
4K x 12 to 4K x 16 RAM Memory System with external timing and control. Used to replace an expensive core memory in an intelligent terminal CRT display.



65K x 8 Memory System with a 32 bit parallel load input and an 8 bit wide serial output. The card is used for CRT refresh in an intelligent terminal.

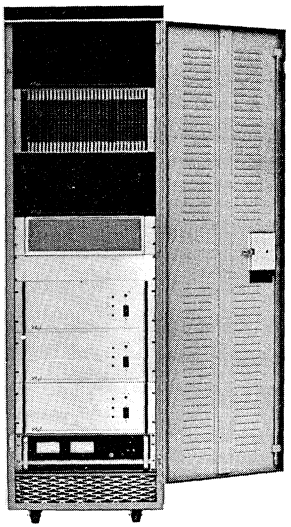
MEMORY CABINETS

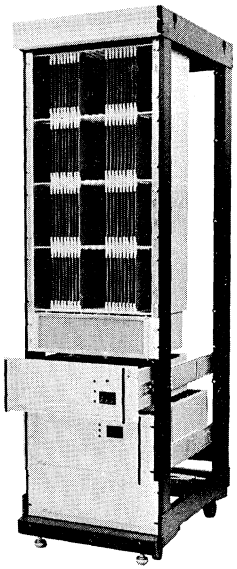
The in-Series Memory Cards are available as individual units or in complete systems. Intel features a number of memory cabinets that can accommodate a variety of memory capacities. Cabinets are designed to allow customers maximum freedom in specifying memory configurations. These cabinets contain power supplies, cooling and interface connections. The following photographs show the various types that are available for off-the-shelf delivery.



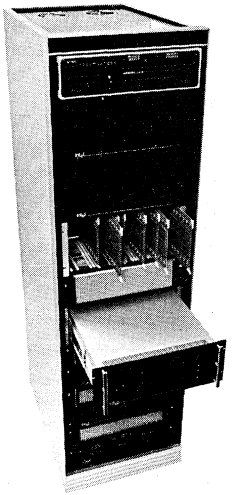
in-CAB-SHB Memory Cabinet features a capacity of up to 96K x 63 bits or 388K x 16 bits, including power supplies and cooling. This cabinet is 70″ high by 36″ deep and is 19″ wide. It is accessible from both front and rear and is mounted on casters. It has room in the rear for additional interface logic chassis.

in-CAB-BHB Memory Cabinet features a capacity of up to 262K x 27 bits. It has ample space for power supplies, and has optional battery back-up capability, including batteries, for a 1 hour back-up support. This cabinet is 80″ high by 30″ deep and is 19″ wide. Accessible from both the front and rear, it contains its own cooling fans and is mounted with casters for easy movement.





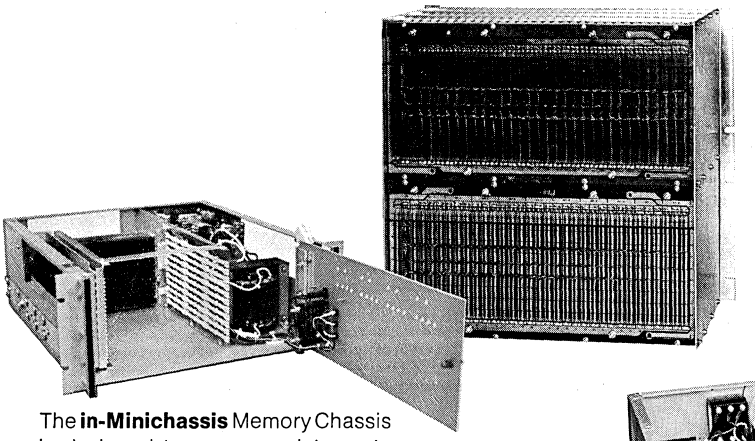
in-CAB-HB Memory Cabinet can accommodate up to 96 MU-10/MU-40 series cards. This memory cabinet is 72″ high, 19″ wide and 30″ deep. It is designed to be free-standing and contains room for cooling fans, power supplies and interface cabling. The memory size can vary from 32K x 144 to 256K x 18 bits. All power supplies are mounted on slides for easy access.



in-CAB-LB Memory Cabinet features a low profile with space for up to 32K x 128 bits of in-10, or 4 times that of in-40 memory, including power supplies and cooling. It is only 48″ high x 30″ deep and is 19″ wide. It is free-standing and comes with casters for easy movement.

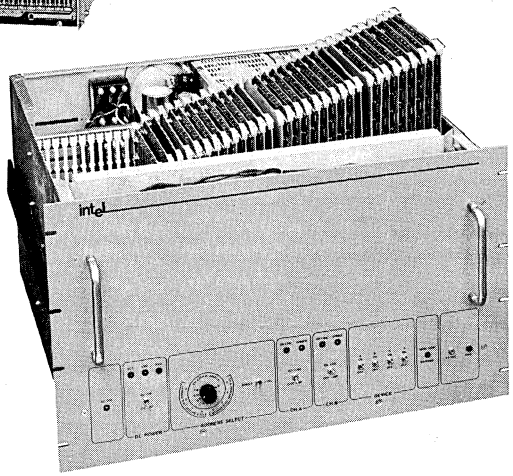
CARD CHASSIS

The in-Series Memory Systems are designed in modular form for ease of conversion into a variety of sizes and configurations. These standard chassis were designed to accommodate specific customer applications. These are shown in the following photographs. Our Intel sales representative can help you with your particular application.

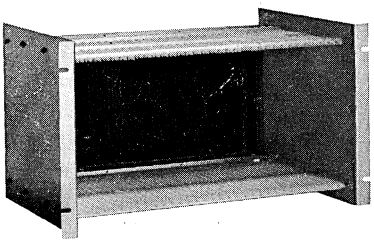


The **in-CHS-II** Memory Chassis is designed to accommodate up to 66 memory and control cards. It features the use of segmented PC back planes for use in configuring large memory systems. This chassis is designed for use in making large word length memory systems. It is 20″ high, 12″ deep, mountable in a 19″ relay rack, and can be used with in-CAB memory cabinets.

The **in-Minichassis** Memory Chassis is designed to accommodate up to 8 memory cards. The memory cards are mounted horizontally with room for a control card and 1 UT-10/40 interface card. This mini-chassis is 7″ high and includes power supplies and cooling fans. It is mounted on slides for ease of movement in and out. All connections are made from the rear of the unit and it can be mounted in a 19″ relay rack. A front panel is optional and includes a circuit breaker and indicator lights. This unit features the use of a PC back plane for all power and ground connections.



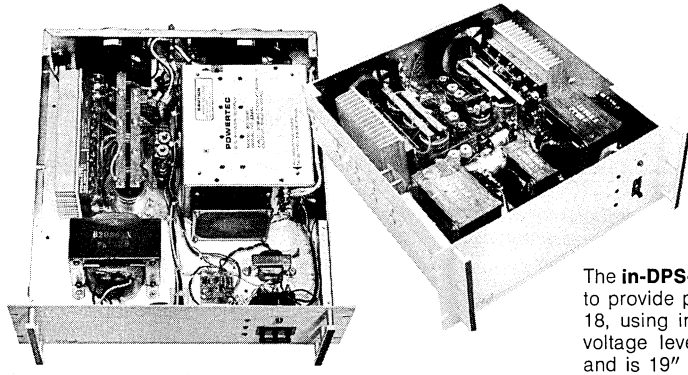
The **in-Jumbochassis** is designed for memory systems that may be mounted in a 24″ cabinet. With integral power supplies and fan assemblies, it measures only 14″ H x 24″ W x 24″ D. Forty-three card slots are available to house thousands of combinations of standard-sized Intel memory cards. For example, a 128K x 18 or 256K x 9 in-10 system, or a 512K x 18 or 1024K x 9 in-40 system can be housed with seven I/O slots left over for address and data buffers or for other custom logic.



The **in-Unichassis** Memory Chassis is designed to accommodate up to 33 memory and control cards for mounting in a 19″ relay rack. This chassis features the use of a full PC back plane with internal power and ground. The chassis can be wired for a number of memory sizes and configurations, and also be used in multiples for even larger memory configurations. It is 10.5″ high, 12″ deep, and can be used with in-CAB memory cabinet.

POWER SUPPLIES

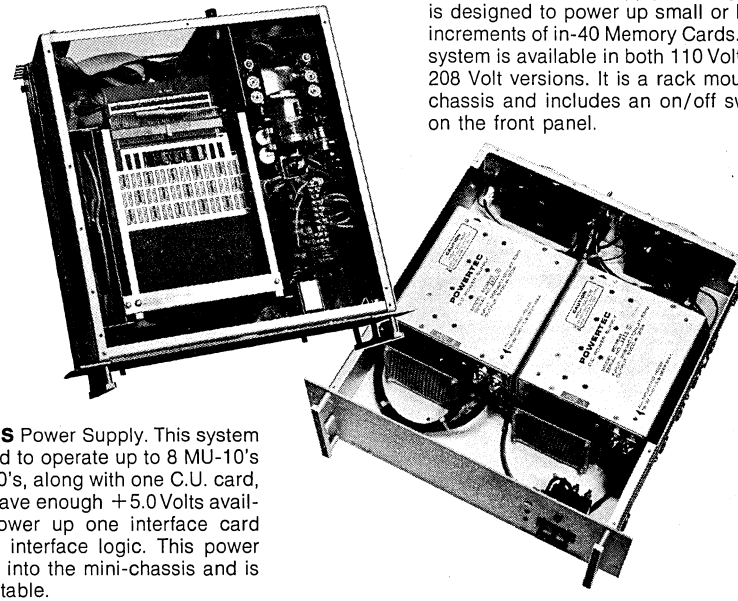
The in-Series Memory Systems are designed in modular form allowing conversion into a variety of sizes and configurations. To accommodate these various memory sizes, Intel has designed standard power supply modules for use in configuring these systems. The following photographs show standard power supply modules that are available. Contact your Intel Memory Systems representative for the one that fits your particular application.



The **in-SPS** Power Supply. This power system is designed to supply both large and small amounts of +5.0 Volts. This power system is especially suited for use with the in-26/in-50/in-60/in-62 Memory Cards. It is a rack mountable chassis, and includes an on/off switch on the front panel.

The **in-DPS-3** Power Supply is designed to provide power to 190K x 9 or 96K x 18, using individual supplies for each voltage level. This supply is 7″ high and is 19″ rack mountable. It features a circuit breaker and has individual indicator lights mounted on the front. It has its own internal cooling, and is recommended for use with the in-10 Series Memory System.

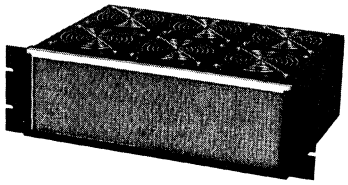
The **in-LPS** Power Supply. This system is designed to power up small or large increments of in-40 Memory Cards. This system is available in both 110 Volt and 208 Volt versions. It is a rack mounted chassis and includes an on/off switch on the front panel.



The **in-MPS** Power Supply. This system is designed to operate up to 8 MU-10's or 8 MU-40's, along with one C.U. card, and also have enough +5.0 Volts available to power up one interface card containing interface logic. This power supply fits into the mini-chassis and is rack mountable.

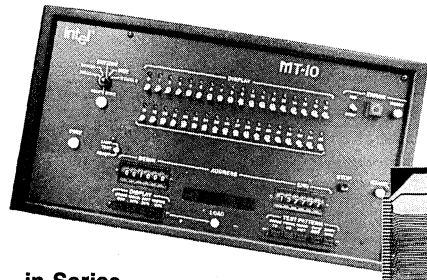
ACCESSORIES

The in-Series is available in card chassis, and with modular power supplies that can be mounted alongside, below, or behind the memory cards. Other accessories like extender boards, interface boards and fan assemblies are also available and listed below.



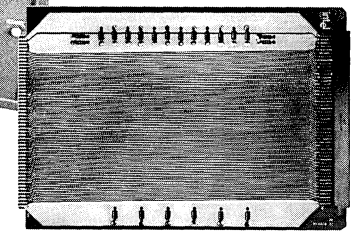
in-Series Fan Assembly

This fan assembly is designed for mounting in a 19″ relay rack. Used for blowing air, or drawing air, upward through the in-series card chassis, this unit can receive air from the front, rear or underneath, and send adequate air flow through up to 4 card chassis stacked upon each other.



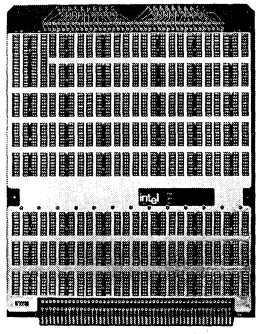
in-Series MT-10/40 System Exercisor

This system exercisor is designed to test up to 36 bits of information and address up to 262 thousand words of memory. The tester is mountable on the front of the memory unit by use of self-contained magnetic devices and is set up to be pluggable into the backplane of the memory system.



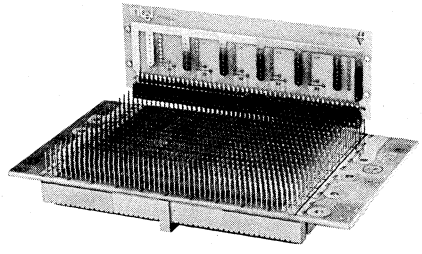
in-Series Extender Board

This extender board is designed to provide the user with full access to any in-series memory card. The extender board plugs directly into the back panel connector and allows full view of any of the in-series cards.



UT 10/40 Series Interface Board

This board is designed for use in assembling custom interfaces to use with in-10/40 series memory systems. The interface board can be used with I.C. sockets, with up to 18 pins, and can be wirewrapped for quick interface connections. This I/O board plugs directly into the in-10/40 series connector slots. 2 slots are available to accommodate up to 40 pin sockets.



in-Series Interface Connector

This unique connector scheme is designed to provide inexpensive, yet reliable, interconnections to the in-Series memory systems. It fits over the in-Series back panel wire wrap pins and forms a tight interconnection. The connector is then fitted with flat cable for connection to other parts of the system in which it is being used.

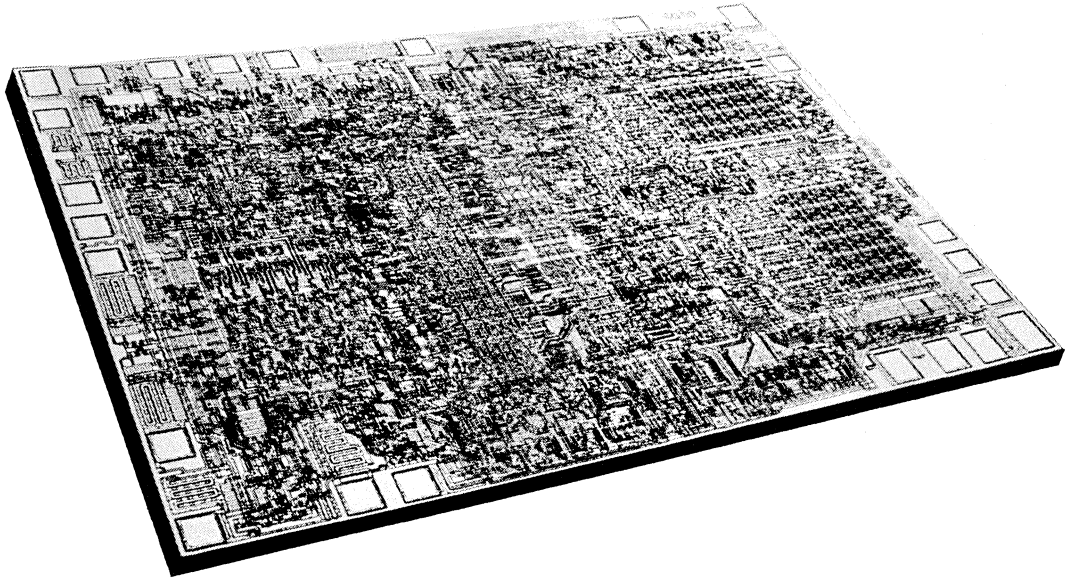
Memory Board Mating Connectors Are:

Amp	1-67878-0
Winchester	HW50DO111
Viking	3VH50/ICN5
Sylvania	7900-0281-X

MEMORY SYSTEMS

7

MCS-40™ MICROCOMPUTER SYSTEM



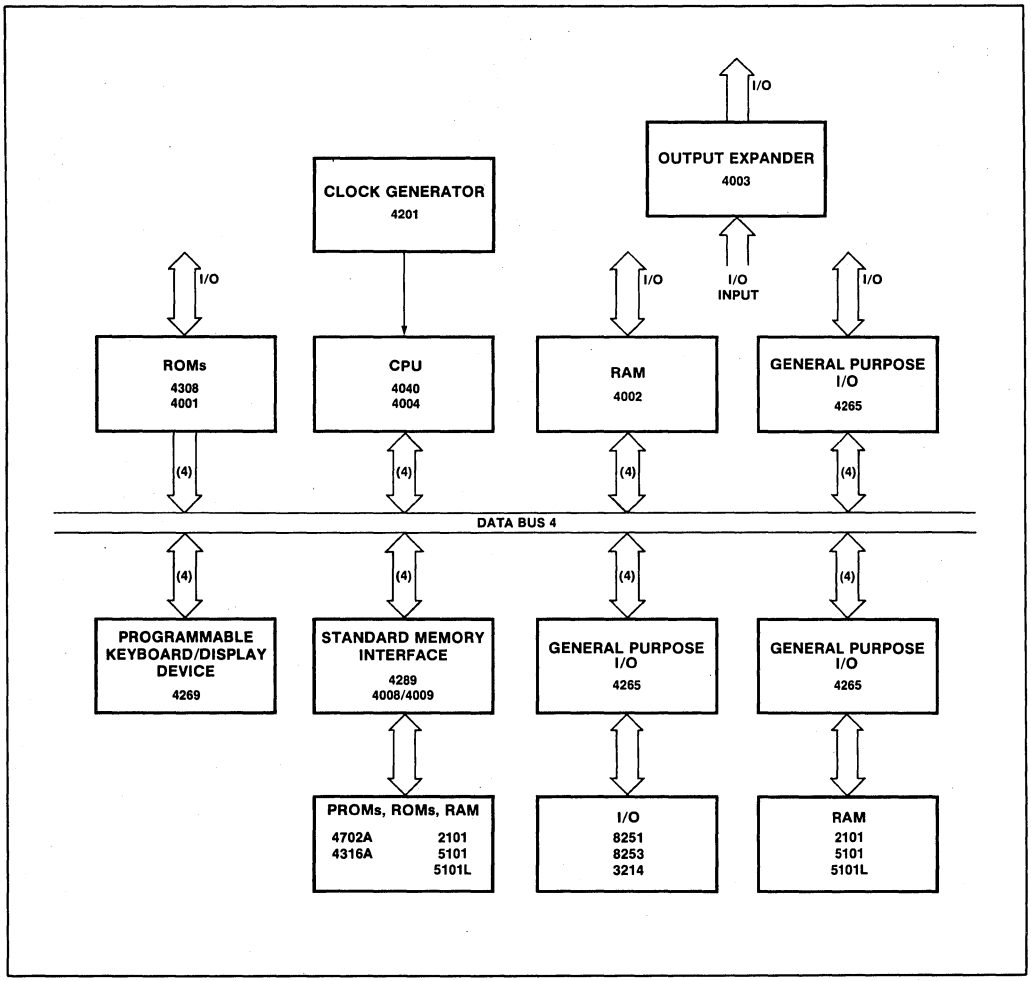
MCS-40™ MICROCOMPUTER SYSTEM

Type	Group	Description	Page No.
4040	CPU	Central Processor Unit	7-4
4004	CPU	Central Processor Unit	7-11
4003	I/O	10-Bit Shift Register	7-18
4265	I/O	Programmable General Purpose I/O	7-22
4269	I/O	Programmable Keyboard/Display Device	7-39
4201	Peripherals	Clock Generator	7-53
4008/4009	Peripherals	Standard Memory Interface Component Pair	7-59
4289	Peripherals	Standard Memory Interface	7-65
4002	RAMs	320-Bit RAM/4 Output Lines	7-76
4101	RAMs	256 x 4 NMOS RAM	7-82
4001	ROMs	256 x 8 ROM/4 I/O Lines	7-85
4308	ROMs	1024 x 8 ROM/16 I/O Lines	7-94
4316A	ROMs	2048 x 8 ROM	7-104
4702A	PROMs	256 x 8 Erasable PROM	7-107
MCS-4/40	Kits	Prototype Systems	7-110

MCS-40™ MICROCOMPUTER SYSTEM

The MCS-40 microcomputer family (the expanded MCS-4 family) is the world's largest selling family of microcomputers. This family of components has been in use for a wide variety of computer and control applications since 1971. The MCS-40 is a system which provides its users with an advanced generation of components geared for random logic replacement and all designs which require the unique advantage of a general purpose computer. The MCS-40 comes with a comprehensive product development program consisting of hardware and software development aids and a large network of regional application engineers to draw upon.

The 4004 and 4040 are complete 4-bit parallel central processing units (CPUs). The 4040 has a complete instruction set of 60 instructions, including Arithmetic, Interrupt, Logical Operations, I/O Instructions, Register Instructions, ROM Bank Switching, Register Bank Switching, Interrupt Disable and Enable. The 4004 has a total of 46 instructions all of which are part of the 4040 instruction set and are mutually compatible.



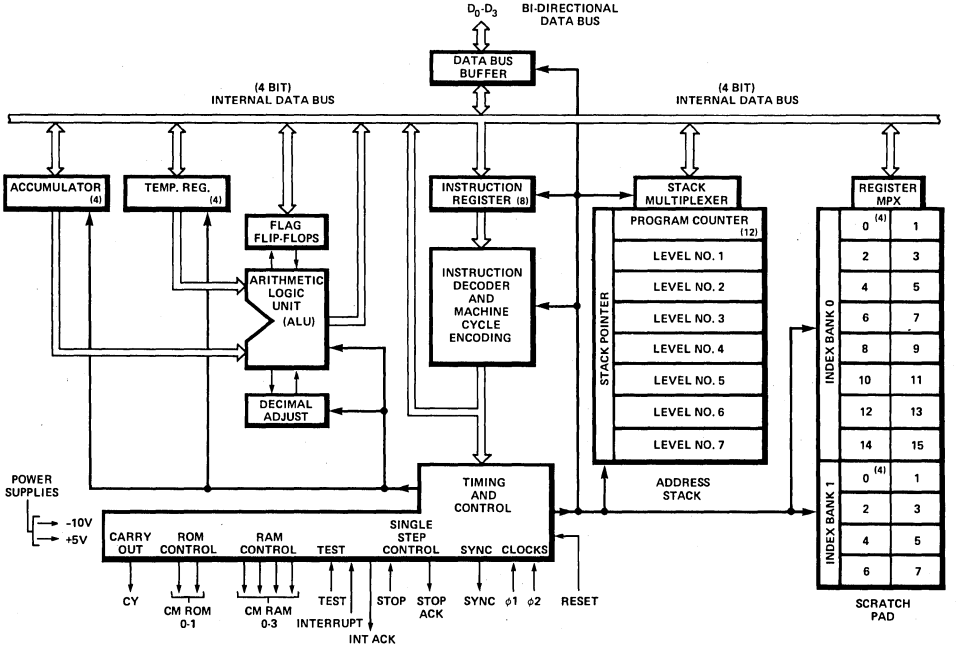
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- **Functionally and Electrically Upward Compatible to 4004 CPU**
- **14 Additional Instructions (60 total) Including Logical Operations and Read Program Memory**
- **Interrupt Capability**
- **Single Step Operation**
- **8K Byte Memory Addressing Capability**
- **24 Index Registers**
- **Subroutine Nesting to 7 Levels**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

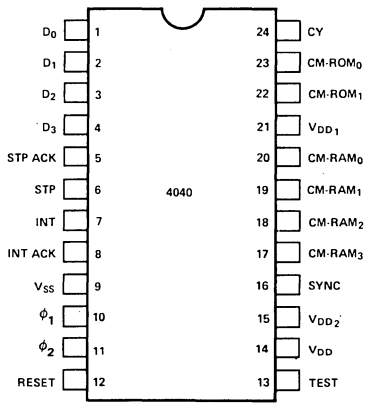
The Intel® 4040 is a complete 4-bit parallel central processing unit (CPU). The CPU can directly address 4K eight bit instruction words or 8K with a bank switch. Seven levels of subroutine nesting, including interrupt, and 24 randomly accessable index registers (24x4) are provided as convenient facilities for the designer. The index registers may be used for addressing or for scratch pad memory for storing computation results. The interrupt feature permits a normal program sequence to be interrupted, with normal program execution continuing after the interrupt service routine is completed. Provisions have also been made to permit single-stepping the CPU using the STOP and ACKNOWLEDGE signals.

The 4040 is an enhanced version of the 4004 and as such retains all the functional capability of that device. It will execute all the 4004 instructions, and is also electrically compatible with all components used with a 4004 CPU.

BLOCK DIAGRAM



Pin Description



D_0-D_3

BIDIRECTIONAL DATA BUS. All address and data communication between the processor and the RAM and ROM chips occurs on these 4 lines.

STP

STOP input. A logic "1" level on this input causes the processor to enter the STOP mode.

STPA

STOP ACKNOWLEDGE output. This signal is present when the processor is in the stopped state. Output is "open drain" requiring pull-down resistor to V_{DD}.

INT

INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

INTA

INTERRUPT ACKNOWLEDGE output. This signal acknowledges receipt of an INTERRUPT signal and prevents additional INTERRUPTS from entering the processor. It remains active until cleared by the execution of the new BRANCH BACK and SRC (BBS) instruction. The output is "open drain" requiring a pull-down resistor to V_{DD}.

RESET

RESET input. A logic "1" level at this input clears all flag and status registers and forces the program counter to zero. To completely clear all address and index registers, RESET must be applied for 96 clock cycles (12 machine cycles).

TEST

TEST input. The logical state of this signal may be tested with the JCN instruction.

SYNC

SYNC output. Synchronization signal generated by the processor and sent to ROM and RAM chips. It indicates the beginning of an instruction cycle.

CM-RAM_0 – CM-RAM_3

CM-RAM outputs. These are bank selection signals for the 4002 RAM chips in the system.

CM-ROM_0 – CM-ROM_1

CM-ROM outputs. These are bank selection signals for program ROM chips in the system.

CY

CARRY output. The state of the carry flip-flop is present on this output and updated each X_1 time. Output is "open-drain" requiring pull down resistor to V_{DD}.

ϕ_1, ϕ_2	Two phase clock inputs
V_{SS}	Most positive voltage
V_{DD}	V_{SS}–15V ±5% – Main supply voltage
*V_{DD1}	V_{SS}–15V ±5% – Timing supply voltage
**V_{DD2}	– Output buffer supply voltage

*For low power operation
**May vary depending on system interface

Instruction Set Format

A. Machine Instructions

- 1 word instruction – 8-bits requiring 8 clock periods (1 instruction cycle)
- 2 word instruction – 16-bits requiring 16 clock periods (2 instruction cycles)

Each instruction is divided into two 4-bit fields. The upper 4-bits is the OPR field containing the operation code. The lower 4-bits is the OPA field containing the modifier. For two word instructions, the second word contains address information or data.

The upper 4-bits (OPR) will always be fetched before the lower 4-bits (OPA) during M_1 and M_2 times respectively.

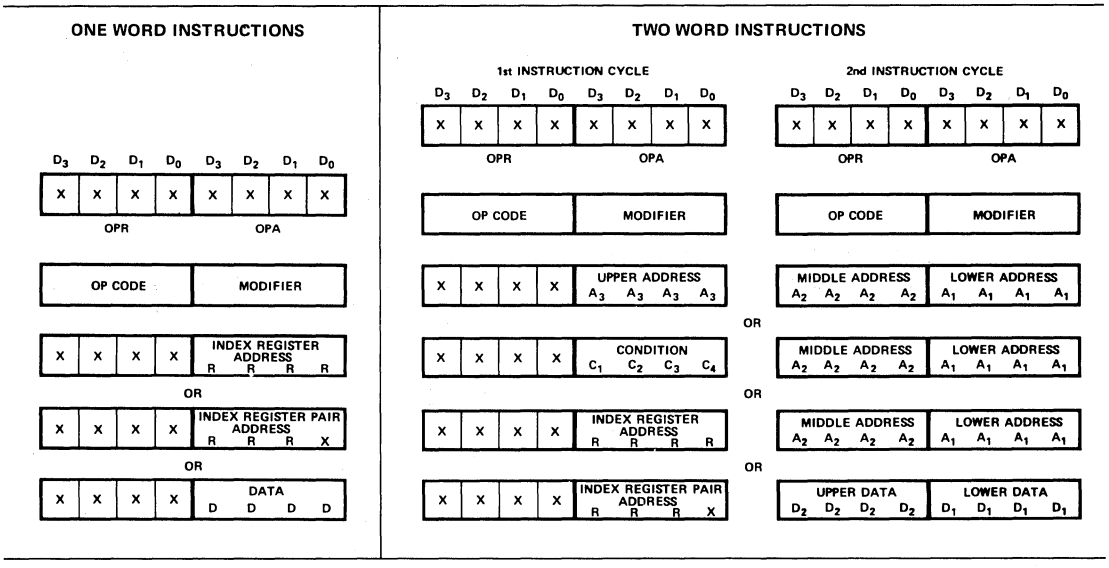


Table I. Machine Instruction Format.

B. Input/Output and RAM Instructions and Accumulator Group Instructions

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed. Table II illustrates the contents of each 4-bit field.

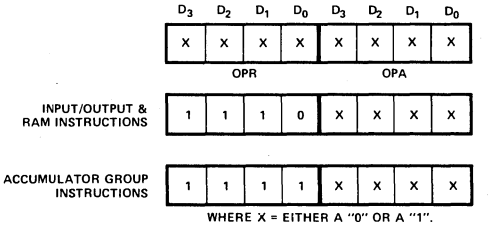


Table II. I/O and Accumulator Group Instruction Formats.

4040 Instruction Set

Summary of Processor Instructions

*Two Cycle Instructions

Mnemonic	Description	Instruction Code OPR D_3	D_2	D_1	D_0	OPA D_3	D_2	D_1	D_0
	MACHINE GROUP								
NOP	No Operation	0	0	0	0	0	0	0	0
HLT	Halt	0	0	0	0	0	0	0	1
BBS	Branch Back and SRC	0	0	0	0	0	0	1	0
LCR	Command Register to Accumulator	0	0	0	0	0	0	1	1
OR4	Logical OR, Index Register 4 and Accumulator	0	0	0	0	0	1	0	0
OR5	Logical OR, Index Register 5 and Accumulator	0	0	0	0	0	1	0	1
AN6	Logical AND, Index Register 6 and Accumulator	0	0	0	0	0	1	1	0
AN7	Logical AND, Index Register 7 and Accumulator	0	0	0	0	0	1	1	1
DB0	Designate ROM Bank 0	0	0	0	0	1	0	0	0
DB1	Designate ROM Bank 1	0	0	0	0	1	0	0	1
SB0	Select Index Register Bank 0	0	0	0	0	1	0	1	0
SB1	Select Index Register Bank 1	0	0	0	0	1	0	1	1
EIN	Enable Interrupt	0	0	0	0	1	1	0	0
DIN	Disable Interrupt	0	0	0	0	1	1	0	1
RPM	Read Program Memory, Half-Byte per Instruction	0	0	0	0	1	1	1	0
*JCN	Jump Conditional to Address	0	0	0	1	C_1	C_2	C_3	C_4
	$A_2A_2A_2A_2A_1A_1A_1A_1$	A_2	A_2	A_2	A_2	A_1	A_1	A_1	A_1
	Condition Code, $C_1C_2C_3C_4$								
*FIM	Fetch Immediate, ROM Data D_2D_1	0	0	1	0	R	R	R	0
	to Index Register Pair RRR	D_2	D_2	D_2	D_2	D_1	D_1	D_1	D_1
SRC	Send Register Control	0	0	1	0	R	R	R	1
FIN	Fetch Indirect, Data from ROM to Index Register Pair RRR	0	0	1	1	R	R	R	0
JIN	Jump Indirect to Address in Register Pair RRR	0	0	1	1	R	R	R	1
*JUN	Jump Unconditional to Address	0	1	0	0	A_3	A_3	A_3	A_3
	$A_3A_2A_1$	A_2	A_2	A_2	A_2	A_1	A_1	A_1	A_1
*JMS	Jump to Subroutine at Address	0	1	0	1	A_3	A_3	A_3	A_3
	$A_3A_2A_1$	A_2	A_2	A_2	A_2	A_1	A_1	A_1	A_1
INC	Increment Register RRRR	0	1	1	0	R	R	R	R
*ISZ	Increment Register RRRR. Go to	0	1	1	1	R	R	R	R
	Address A_2A_1 if result is not zero, otherwise go to next instruction	A_2	A_2	A_2	A_2	A_1	A_1	A_1	A_1
ADD	Add Register RRRR to Accumulator with Carry	1	0	0	0	R	R	R	R
SUB	Subtract Register RRRR from Accumulator with Borrow	1	0	0	1	R	R	R	R
LD	Load Contents of Register RRRR to Accumulator	1	0	1	0	R	R	R	R
XCH	Exchange Contents of Register RRRR and Accumulator	1	0	1	1	R	R	R	R
BBL	Branch Back and Load Data DDDD to Accumulator	1	1	0	0	D	D	D	D
LDM	Load Data DDDD to Accumulator	1	1	0	1	D	D	D	D

Mnemonic	Description	Instruction Code OPR D_3	D_2	D_1	D_0	OPA D_3	D_2	D_1	D_0
	I/O and RAM GROUP								
WRM	Accumulator to Selected RAM Main Memory Character	1	1	1	0	0	0	0	0
WMP	Accumulator to Selected RAM Output Port	1	1	1	0	0	0	0	1
WRR	Accumulator to Selected ROM Output Port	1	1	1	0	0	0	1	0
WPM	Accumulator to Selected Half-Byte in Read/Write Program Memory	1	1	1	0	0	0	1	1
WR0	Accumulator to Selected RAM Status Character 0	1	1	1	0	0	1	0	0
WR1	Accumulator to Selected RAM Status Character 1	1	1	1	0	0	1	0	1
WR2	Accumulator to Selected RAM Status Character 2	1	1	1	0	0	1	1	0
WR3	Accumulator to Selected RAM Status Character 3	1	1	1	0	0	1	1	1
SBM	Subtract Selected RAM Main Memory Character from Accumulator with Borrow	1	1	1	0	1	0	0	0
RDM	Selected RAM Main Memory Character to Accumulator	1	1	1	0	1	0	0	1
RDR	Selected ROM Input Port to Accumulator	1	1	1	0	1	0	1	0
ADM	Add Selected RAM Main Memory Character to Accumulator with Carry	1	1	1	0	1	0	1	1
RD0	Selected RAM Status Character 0 to Accumulator	1	1	1	0	1	1	0	0
RD1	Selected RAM Status Character 1 to Accumulator	1	1	1	0	1	1	0	1
RD2	Selected RAM Status Character 2 to Accumulator	1	1	1	0	1	1	1	0
RD3	Selected RAM Status Character 3 to Accumulator	1	1	1	0	1	1	1	1
	ACCUMULATOR GROUP								
CLB	Clear Accumulator and Carry	1	1	1	1	0	0	0	0
CLC	Clear Carry	1	1	1	1	0	0	0	1
IAC	Increment Accumulator	1	1	1	1	0	0	1	0
CMC	Complement Carry	1	1	1	1	0	0	1	1
CMA	Complement Accumulator	1	1	1	1	0	1	0	0
RAL	Rotate Left, Accumulator and Carry	1	1	1	1	0	1	0	1
RAR	Rotate Right, Accumulator and Carry	1	1	1	1	0	1	1	0
TCC	Transmit Carry to Accumulator, Clear Carry	1	1	1	1	0	1	1	1
DAC	Decrement Accumulator	1	1	1	1	1	0	0	0
TCS	Transfer Carry Subtract and Clear Carry	1	1	1	1	1	0	0	1
STC	Set Carry	1	1	1	1	1	0	1	0
DAA	Decimal Adjust Accumulator	1	1	1	1	1	0	1	1
KBP	Keyboard Process	1	1	1	1	1	1	0	0
DCL	Designal Command Line	1	1	1	1	1	1	0	1

NOTES:

(1) The condition code is assigned as follows:
- $C_1 = 1$ Invert jump condition
- $C_1 = 0$ Not invert jump condition
- $C_2 = 1$ Jump if accumulator is zero
- $C_3 = 1$ Jump if carry/link is a 1
- $C_4 = 1$ Jump if test signal is a 0

(2) RRR is the address of 1 of 8 index register pairs in the CPU.

(3) RRRR is the address of 1 of 16 index registers in the CPU.

(4) Each RAM chip has 4 registers, each with twenty 4-bit characters subdivided into 16 main memory characters and 4 status characters. Chip number, RAM register and main memory character are addressed by an SRC instruction. For the selected chip and register, however, status character locations are selected by the instruction code (OPA).

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to V_{SS}	+0.5V to -20V
Power Dissipation	1.0 Watt

**COMMENT:*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

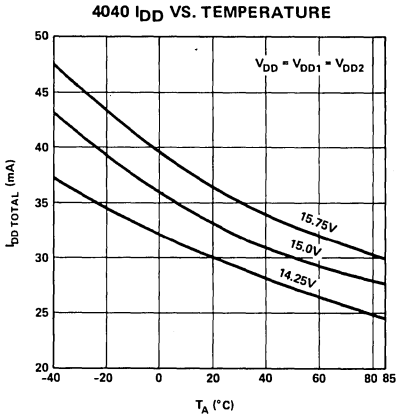
D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; 4040 V_{DD1} = V_{DD2} = V_{DD}; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}): Unless Otherwise specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{SB}	Standby Supply Current (V_{DD1} + V_{DD2})		3	5	mA	T_A = 25°C, V_{DD} = V_{SS}
I_{DD} (total)	Supply Current (V_{DD} + V_{DD1} + V_{DD2})		40	60	mA	T_A = 25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	4040 TEST and INT inputs
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT}=-12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT}=V_{SS}
I_{OL}	CM-ROM Sinking Current	6.5	12		mA	V_{OUT}=V_{SS}
I_{OL}	CM-RAM Sinking Current	2.5	6		mA	V_{OUT}=V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL}=0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-ROM Output Resistance, Data Line "0" Level		320	600	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-RAM Output Resistance, Data Line "0" Level		1.1	1.8	kΩ	V_{OUT}=V_{SS}-.5V
R_{OH}	INTA, CY, STPA Output Resistance "0" Level		1.1	1.8	kΩ	V_{OUT}=V_{SS}-.5V
CAPACITANCE						
C_{ϕ}	Clock Capacitance		17	25	pF	V_{IN}=V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN}=V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN}=V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN}=V_{SS}

Typical D.C. Characteristics



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{SS} - V_{DD} = 15V \pm 5\%$

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Times			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_{WRPM}	Data-In Write Time-RPM Instruction	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{HRPM}	Data-In Hold Time-RPM Instruction	40	20		ns	
t_H[3]	Data Bus Hold Time During X_2-X_3 Transition.	150			ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}[5]	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	Data Lines			700	ns	200pF Data Lines[4]
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT}=20pF
t_{DEL}	CY, STPACK, INTACK Delay			2.0	μsec	

NOTES:
1. t_H measured with $t_{\phi R}$ = 10nsec.
2. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to the 4040 at X_2 always enter a float state until the 4040 takes over the data bus at X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. $C_{DATA\ BUS}$ = 200pF if 4008 and 4009 or 4289 is used.
5. The 4040 accumulator is gated out at X_1 time at ϕ_1 leading edge, and the t_{ACC} is 930 nsec + $t_{\phi D2}$.

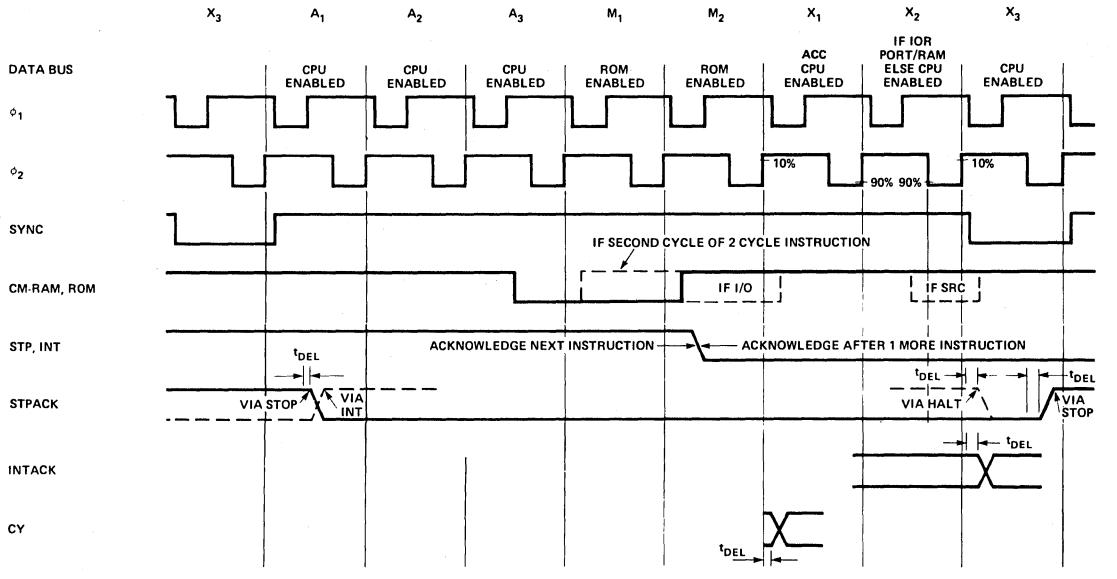


Figure 1. Timing Diagram.

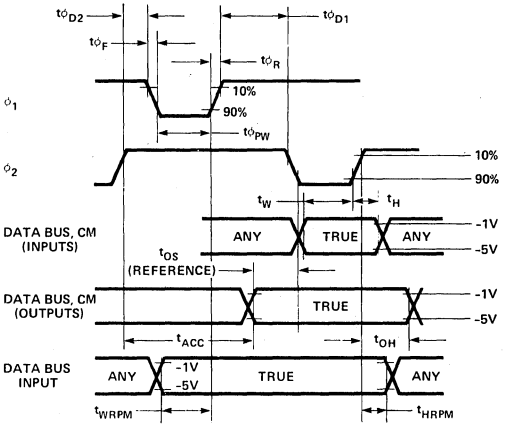


Figure 2. Timing Detail.

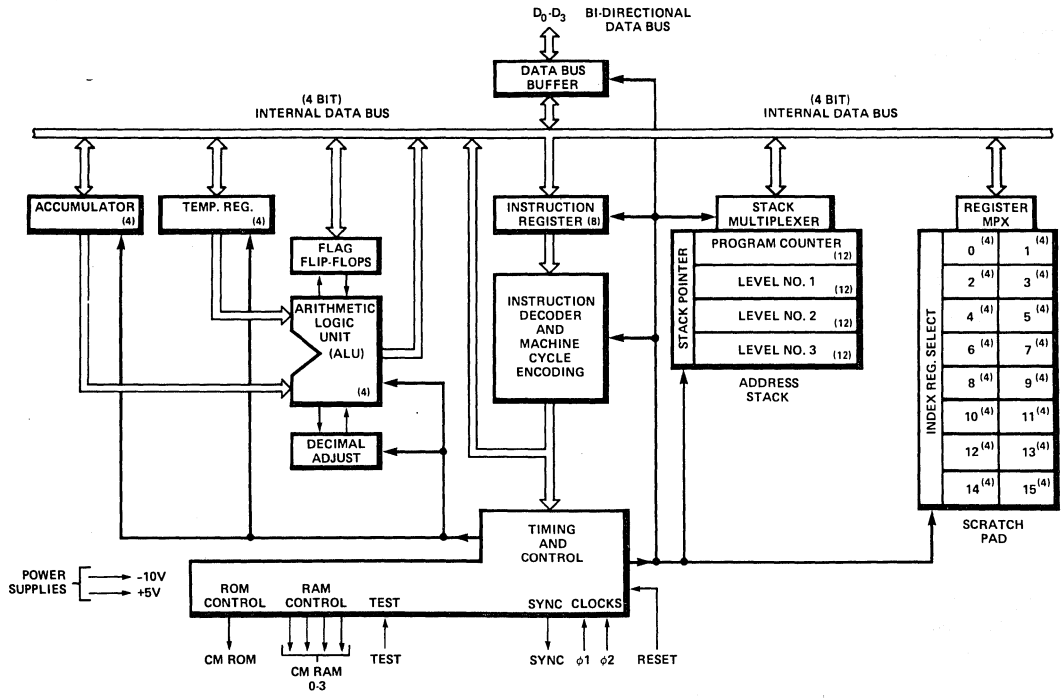
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- 4-Bit Parallel CPU With 46 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes
- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-40 ROMs and RAMs
- Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- Standard Operating Temperature Range of 0° to 70° C
- Also Available With -40° to +85° C Operating Range

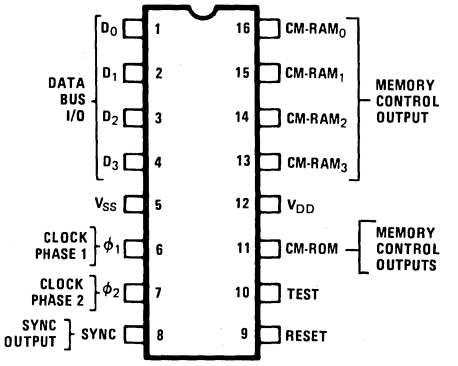
The Intel® 4004 is a complete 4-bit parallel central processing unit (CPU). The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.



Pin Description



D_0-D_3

BIDIRECTIONAL DATA BUS. All address and data communication between the processor and the RAM and ROM chips occurs on these 4 lines.

RESET

RESET input. A logic "1" level at this input clears all flags and status registers and forces the program counter to zero. To completely clear all address and index registers, RESET must be applied for 64 clock cycles (8 machine cycles).

TEST

TEST input. The logical state of this signal may be tested with the JCN instruction.

SYNC

SYNC output. Synchronization signal generated by the processor and set to the ROM and RAM chips. It indicates the beginning of an instruction cycle.

CM-ROM

CM-ROM output. This is the ROM selection signal sent out by the processor when data is required from program memory.

CM-RAM_0 – CM-RAM_3

CM-RAM outputs. These are the bank selection signals for the 4002 RAM chips in the system.

ϕ_1, ϕ_2

Two phase clock inputs.

V_{SS}

Most positive voltage.

V_{DD}

V_{SS} -15 ±5% main supply voltage.

Instruction Set Format

A. Machine Instructions

- 1 word instruction – 8-bits requiring 8 clock periods (instruction cycle).
- 2 word instruction – 16-bits requiring 16 clock periods (2 instruction cycles).

Each instruction is divided into two four-bit fields. The upper 4-bits is the OPR field containing the operation code. The lower 4-bits is the OPA field containing the modifier. For two word instructions, the second word contains address information or data.

The upper 4-bits (OPR) will always be fetched before the lower 4-bits (OPA) during M_1 and M_2 times respectively.

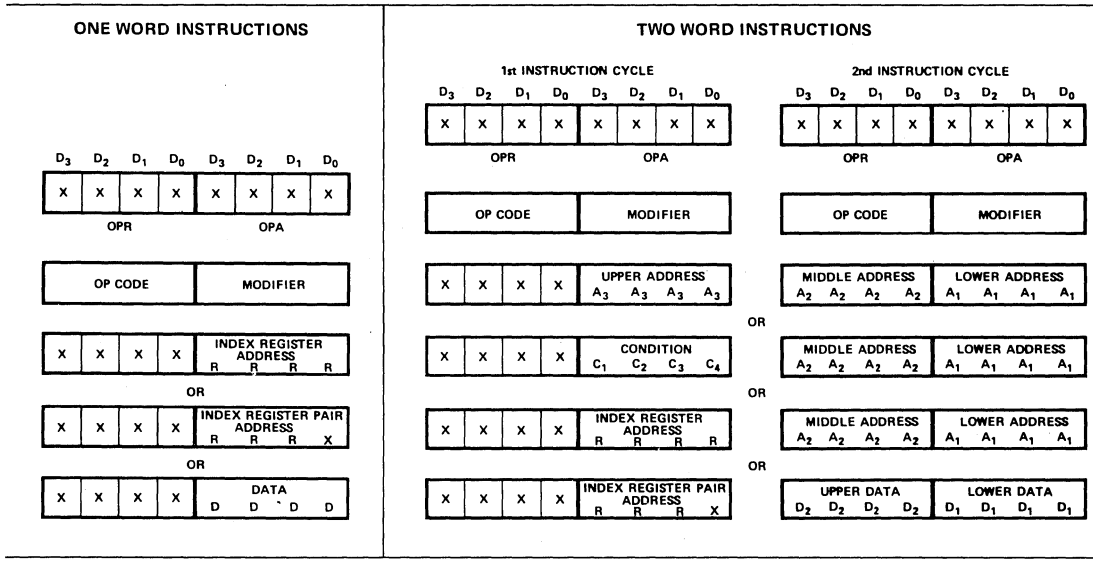


Table I. Machine Instruction Format

B. Input/Output and RAM Instructions and Accumulator Group Instructions

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed. Table II illustrates the contents of each 4-bit field.

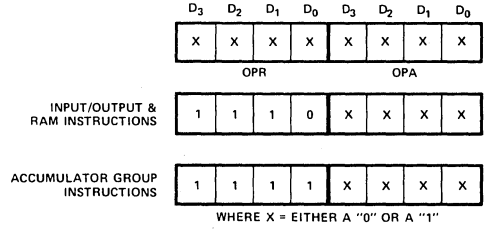


Table II. I/O and Accumulator Group Instruction Formats

4004 Instruction Set

[Those instructions preceded by an asterisk (*) are 2 word instructions that occupy 2 successive locations in ROM]

MACHINE INSTRUCTIONS (Logic 1 = Low Voltage = Negative Voltage (V_{DD}); Logic 0 = High Voltage = (V_{SS})

MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
NOP	0 0 0 0	0 0 0 0	No operation.
*JCN	0 0 0 1 $A_2 A_2 A_2 A_2$	$C_1 C_2 C_3 C_4$ $A_1 A_1 A_1 A_1$	Jump to ROM address A_2 A_2 A_2 A_2. A_1 A_1 A_1 A_1 (within the same ROM that contains this JCN instruction) if condition C_1 C_2 C_3 C_4 [1] is true, otherwise skip (go to the next instruction in sequence).
*FIM	0 0 1 0 $D_2 D_2 D_2 D_2$	R R R 0 $D_1 D_1 D_1 D_1$	Fetch immediate (direct) from ROM Data D_2, D_1 to index register pair location RRR.[2]
SRC	0 0 1 0	R R R 1	Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the Instruction Cycle.
FIN	0 0 1 1	R R R 0	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.
JIN	0 0 1 1	R R R 1	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the Instruction Cycle.
*JUN	0 1 0 0 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump unconditional to ROM address A_3, A_2, A_1.
*JMS	0 1 0 1 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump to subroutine ROM address A_3, A_2, A_1, save old address. (Up 1 level in stack.)
INC	0 1 1 0	R R R R	Increment contents of register RRRR. [3]
*ISZ	0 1 1 1 $A_2 A_2 A_2 A_2$	R R R R $A_1 A_1 A_1 A_1$	Increment contents of register RRRR. Go to ROM address A_2, A_1 (within the same ROM that contains this ISZ instruction) if result $\neq 0$, otherwise skip (go to the next instruction in sequence).
ADD	1 0 0 0	R R R R	Add contents of register RRRR to accumulator with carry.
SUB	1 0 0 1	R R R R	Subtract contents of register RRRR to accumulator with borrow.
LD	1 0 1 0	R R R R	Load contents of register RRRR to accumulator.
XCH	1 0 1 1	R R R R	Exchange contents of index register RRRR and accumulator.
BBL	1 1 0 0	D D D D	Branch back (down 1 level in stack) and load data DDDD to accumulator.
LDM	1 1 0 1	D D D D	Load data DDDD to accumulator.

INPUT/OUTPUT AND RAM INSTRUCTIONS for the following devices: 4001, 4002, 4008, 4009, and 4289*

(The RAM's and ROM's operated on in the I/O and RAM instructions have been previously selected by the last SRC instruction executed.)

MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
WRM	1 1 1 0	0 0 0 0	Write the contents of the accumulator into the previously selected RAM main memory character.
WMP	1 1 1 0	0 0 0 1	Write the contents of the accumulator into the previously selected RAM output port.
WRR	1 1 1 0	0 0 1 0	Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)
WPM	1 1 1 0	0 0 1 1	Write the contents of the accumulator into the previously selected half byte of read/write program memory (for use with 4008/4009 or 4289)
WRϕ [4]	1 1 1 0	0 1 0 0	Write the contents of the accumulator into the previously selected RAM status character 0.
WR1 [4]	1 1 1 0	0 1 0 1	Write the contents of the accumulator into the previously selected RAM status character 1.
WR2 [4]	1 1 1 0	0 1 1 0	Write the contents of the accumulator into the previously selected RAM status character 2.
WR3 [4]	1 1 1 0	0 1 1 1	Write the contents of the accumulator into the previously selected RAM status character 3.
SBM	1 1 1 0	1 0 0 0	Subtract the previously selected RAM main memory character from accumulator with borrow.
RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator.
RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)
ADM	1 1 1 0	1 0 1 1	Add the previously selected RAM main memory character to accumulator with carry.
RDϕ [4]	1 1 1 0	1 1 0 0	Read the previously selected RAM status character 0 into accumulator.
RD1 [4]	1 1 1 0	1 1 0 1	Read the previously selected RAM status character 1 into accumulator.
RD2 [4]	1 1 1 0	1 1 1 0	Read the previously selected RAM status character 2 into accumulator.
RD3 [4]	1 1 1 0	1 1 1 1	Read the previously selected RAM status character 3 into accumulator.

*For explanation of 4265 and 4269 I/O instructions, see the 4265 and 4269 data sheets.

ACCUMULATOR GROUP INSTRUCTIONS

CLB	1 1 1 1	0 0 0 0	Clear both. (Accumulator and carry)
CLC	1 1 1 1	0 0 0 1	Clear carry.
IAC	1 1 1 1	0 0 1 0	Increment accumulator.
CMC	1 1 1 1	0 0 1 1	Complement carry.
CMA	1 1 1 1	0 1 0 0	Complement accumulator.
RAL	1 1 1 1	0 1 0 1	Rotate left. (Accumulator and carry)
RAR	1 1 1 1	0 1 1 0	Rotate right. (Accumulator and carry)
TCC	1 1 1 1	0 1 1 1	Transmit carry to accumulator and clear carry.
DAC	1 1 1 1	1 0 0 0	Decrement accumulator.
TCS	1 1 1 1	1 0 0 1	Transfer carry subtract and clear carry.
STC	1 1 1 1	1 0 1 0	Set carry.
DAA	1 1 1 1	1 0 1 1	Decimal adjust accumulator.
KBP	1 1 1 1	1 1 0 0	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
DCL	1 1 1 1	1 1 0 1	Designate command line.

NOTES: [1] The condition code is assigned as follows:

C_1 = 1 Invert jump condition
C_1 = 0 Not invert jump condition
C_2 = 1 Jump if accumulator is zero
C_3 = 1 Jump if carry/link is a 1
C_4 = 1 Jump if test signal is a 0

[2] RRR is the address of 1 of 8 index register pairs in the CPU.

[3] RRRR is the address of 1 of 16 index registers in the CPU.

[4] Each RAM chip has 4 registers, each with twenty 4-bit characters subdivided into 16 main memory characters and 4 status characters. Chip number, RAM register and main memory character are addressed by an SRC instruction. For the selected chip and register, however, status character locations are selected by the instruction code (OPA).

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

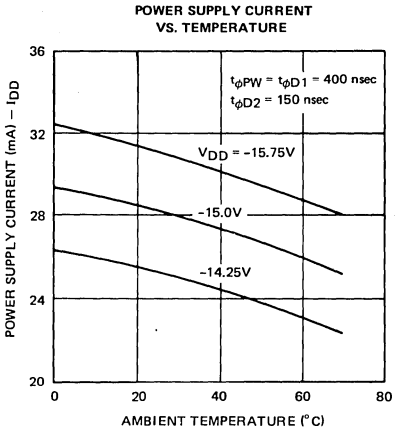
D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ± 5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		30	40	mA	T_A=25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL}=V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	4004 TEST Input
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT}=-12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitance Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT}=V_{SS}
I_{OL}	CM-ROM Sinking Current	6.5	12		mA	V_{OUT}=V_{SS}
I_{OL}	CM-RAM Sinking Current	2.5	6		mA	V_{OUT}=V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL}=0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-ROM Output Resistance, Data Line "0" Level		320	600	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-RAM Output Resistance, Data Line "0" Level		1.1	1.8	kΩ	V_{OUT}=V_{SS}-.5V
CAPACITANCE						
C_{ϕ}	Clock Capacitance		14	20	pF	V_{IN}=V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN}=V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN}=V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN}=V_{SS}

Typical D.C. Characteristics



A.C. Characteristics

T_A=0°C to 70°C, V_{SS}-V_{DD} = 15V ±5%

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t_{\phi R}$	Clock Rise Time			50	ns	
$t_{\phi F}$	Clock Fall Times			50	ns	
$t_{\phi PW}$	Clock Width	380		480	ns	
$t_{\phi D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t_{\phi D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_H[3]	Data Bus Hold Time During M_2-X_1 and and X_2-X_3 Transition.	150			ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	Data Lines			700	ns	200pF Data Lines[4]
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT}=20pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to the 4004 at M_2 and X_2 always enter a float state until the 4004 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. $C_{DATA\ BUS}$ = 200pF if 4008 and 4009 or 4289 is used.

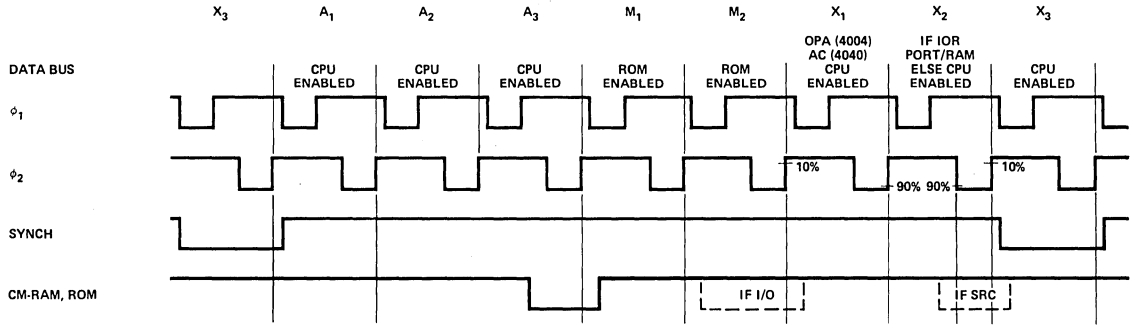


Figure 1. Timing Diagram.

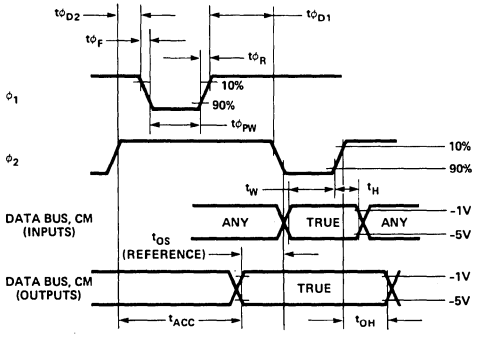


Figure 2. Timing Detail.

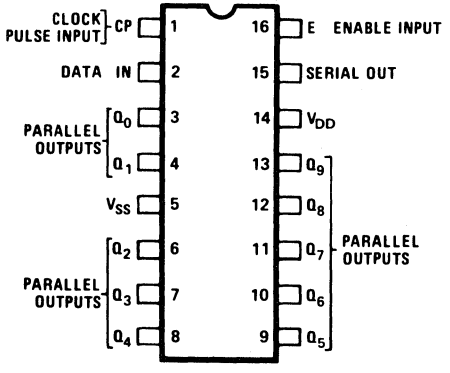
10 BIT SHIFT REGISTER/OUTPUT EXPANDER

- 10 Bit Serial-In/Parallel Out
- Serial-Out Capability for Additional I/O Expansion
- 16 Pin Dual-In-Line Package
- Easy Expansion of I/O Output Capability
- Enable Output Control
- Standard Operating Temperature Range of 0° to 70°C

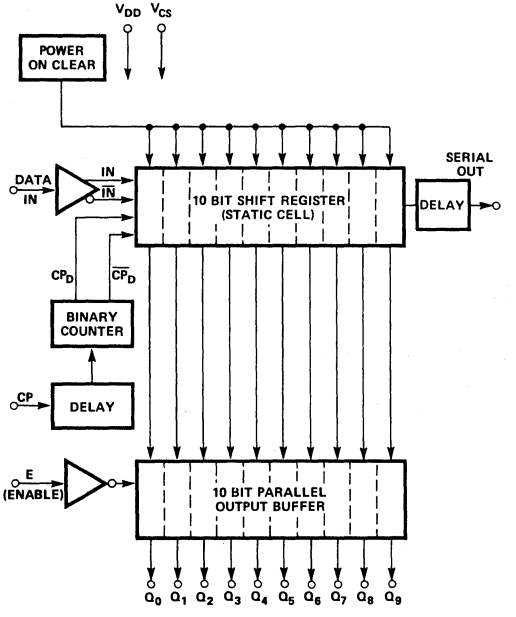
The 4003 is a 10 bit serial-in, parallel-out, serial-out shift register with enable logic. The 4003 is used to expand the number of ROM and RAM I/O ports to communicate with peripheral devices such as keyboards, printers, displays, readers, teletypewriters, etc.

The 4003 is a single phase static shift register; however, the clock pulse (CP) maximum width is limited to 10 msec. Data-in and CP can be simultaneous. To avoid race conditions, CP is internally delayed.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation	Description of Function
1	CP	The clock pulse input. A "0" (V_{SS}) to "1" (V_{DD}) transition will shift data in.
2	DATA IN	Serial data input line.
3	O_0	Parallel data output lines, when enabled. Each pin may be made TTL compatible with a 5.6K pull-down resistor to V_{DD}.
4	O_1	
6	O_2	
7	O_3	
8	O_4	
9	O_5	
10	O_6	
11	O_7	
12	O_8	
13	O_9	
5	V_{SS}	Most positive supply voltage.
14	V_{DD}	Main supply voltage value must be V_{SS} - 15.0V ± 5% (-10v for TTL operation)
15	Serial out	Serial data output.
16	E	Enable, when E = "1" (V_{DD}) the output lines contain valid data. When E = "0" (V_{SS}) the output lines are at V_{SS}.

Functional Description

The 4003 is designed to be typically appended to an MCS-40 I/O port. This can be the I/O port of a 4001, 4002, 4289, 4308, or a 4265. One I/O line is assigned to be the Enable (E), another the Clock (CP), and still another the Serial Data-Input. For example, to access the 4003 a subroutine of sequential outputs consisting of Data, clock pulse on, Enable — followed by an output of clock pulse off and Enable, will serially load the 4003.

Data is loaded serially and is available in parallel on 10 output lines which are accessed through enable logic. When enabled (E = 1 -- V_{DD}), the shift register contents are read out; when not enabled (E = 0 -- V_{SS}), the parallel-out lines are at Logic "0" (V_{SS}). The serial-out line is not affected by the enable logic to allow longer word cascading.

Data is also available serially permitting an indefinite number of similar devices to be cascaded together to provide shift register length multiples of 10.

The data shifting is controlled by the CP signal. An internal power-on-clear circuit will clear the shift register (outputs = 0 or V_{SS}) between the application of the supply voltage and the first CP signal.

The 4003 output buffers are useful for multiple key depression rejection when a 4003 is used in conjunction with a keyboard. In this mode if up to three output lines are connected together, the state of the output is high (Logic "0" or V_{SS}) if at least one line is high.

Another typical application of the 4003 is for Keyboard or Display Scanning where a single bit of Logic "1" is shifted through the 4003 and is used to activate the various digits, keyboard rows, etc.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

T_A = 0°C to +70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec, $t_{\phi D2}$ = 150 nsec, unless otherwise specified.

Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}), Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}).

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		5.0	8.5	mA	t_{WL} = t_{WH} = 8μsec; T_A = 25°C
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3		
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
I/O OUTPUT CHARACTERISTICS						
I_{OL}	Parallel Out Pins Sinking Current, "1" Level	0.6	1.0		mA	V_{OUT} = 0V. For TTL compatibility a 5.6KΩ (±10%) resistor between output and V_{DD} should be added.[2]
I_{OL}	Serial Out Sinking Current, "1" Level	1.0	2.0		mA	V_{OUT} = 0V
V_{OL}	Output Low Voltage	V_{SS}-11	V_{SS}-7.5	V_{SS}-6.5	V	I_{OL} = 10μA
R_{OH}	Parallel-Out Pins Output Resistance "0" Level		400	750	Ω	V_{OUT} = -0.5V
R_{OH}	Serial Out Output Resistance "0" Level		650	1200	Ω	V_{OUT} = -0.5V

Notes: 1. Typical values are to T_A = 25°C and Nominal Supply Voltages.

2. For TTL compatibility on the I/O lines the supply voltages should be V_{DD} = -10V ±5%; V_{SS} = +5V ±5%.

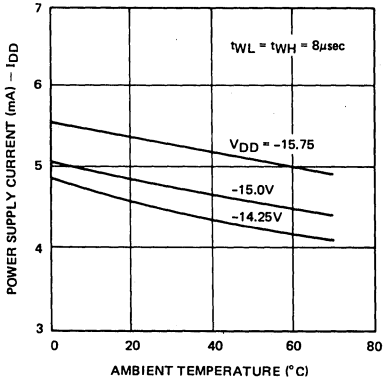
CAPACITANCE

f = 1 MHz; V_{IN} = 0V; T_A = 25°C; Unmeasured Pins Grounded.

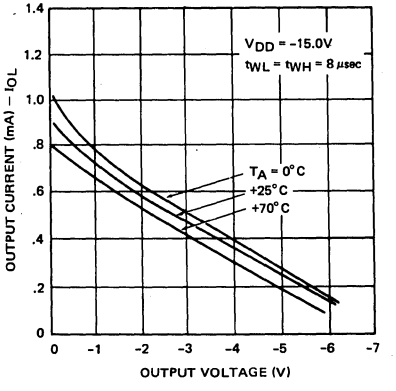
Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF

Typical D.C. Characteristics

POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



MCS-40

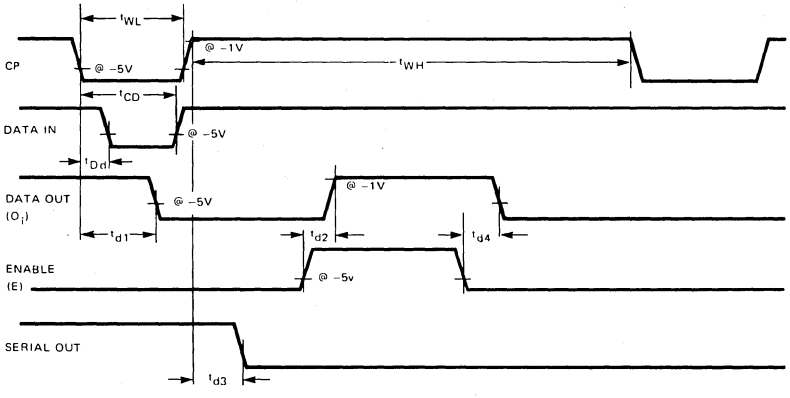
A.C. Characteristics

T_A = 0°C to +70°C; V_{DD} = -15 ±5%, V_{SS} = GND

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{WL}	CP Low Width	6		10,000	μsec	
t_{WH}[1]	CP High Width	6			μsec	
t_{CD}	Clock-On to Data-Off Time	3			μsec	
t_{Dd}[2]	CP to Data Set Delay			250	nsec	
t_{d1}	CP to Data Out Delay	250		1750	nsec	
t_{d2}	Enable to Data Out Delay			350	nsec	C_{OUT} = 20pF
t_{d3}	CP to Serial Out Delay	200		1250	nsec	C_{OUT} = 20pF
t_{d4}	Enable to Data Out Delay			1.0	μsec	C_{OUT} = 20pF

Notes: 1. t_{WH} can be any time greater than 6μsec.
2. Data can occur prior to CP.

Timing Diagram



PROGRAMMABLE GENERAL PURPOSE I/O DEVICE

- **Multi-Mode 14 Operating Modes**
- **16 Lines of I/O Capability**
- **Bit Set/Reset**
- **Multiplexable Outputs**
- **Eight Bit Transfer Mode**
- **Interfaces to 8080 Peripherals**
- **Synchronous and Asynchronous Interface**
- **Strobed Buffer Inputs and Outputs**
- **TTL Interface**
- **Up to Eight 4265s Per System**
- **Interface to Standard RAMs**
- **28 Pin Dual-In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C (-40° to +85°C Operating Range to be Available First Quarter 1976)**

The 4265 is a general purpose I/O device designed to interface with the MCS-40™ microcomputer family. This device provides four software programmable 4-bit I/O ports which can be configured to allow any one of fourteen unique operating modes for interfacing to data memory or a variety of user peripheral devices.

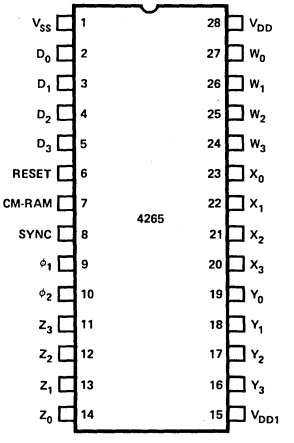
A single MCS-40 system can accomodate up to four 4265s (one per CM-RAM) without external logic or up to eight 4265s with one external decoder.

The 4265 resides on the MCS-40 data bus and uses the same selection procedure as 4002 RAM device. A valid compare selects the 4265 for MCS-40 I/O commands. As in the case of the 4002 or any MCS-40 peripheral circuit, selection occurs only when the proper SRC code and the CM signal are present simultaneously.

The 4265 provides an extremely flexible, general purpose I/O system capable of handling 4- or 8-bit input or output data. One of fourteen basic operating modes can be selected (software programmable) as described below.

Port Z is TTL compatible with any TTL device. Ports W, X, and Y are low-power TTL compatible.

PIN CONFIGURATION

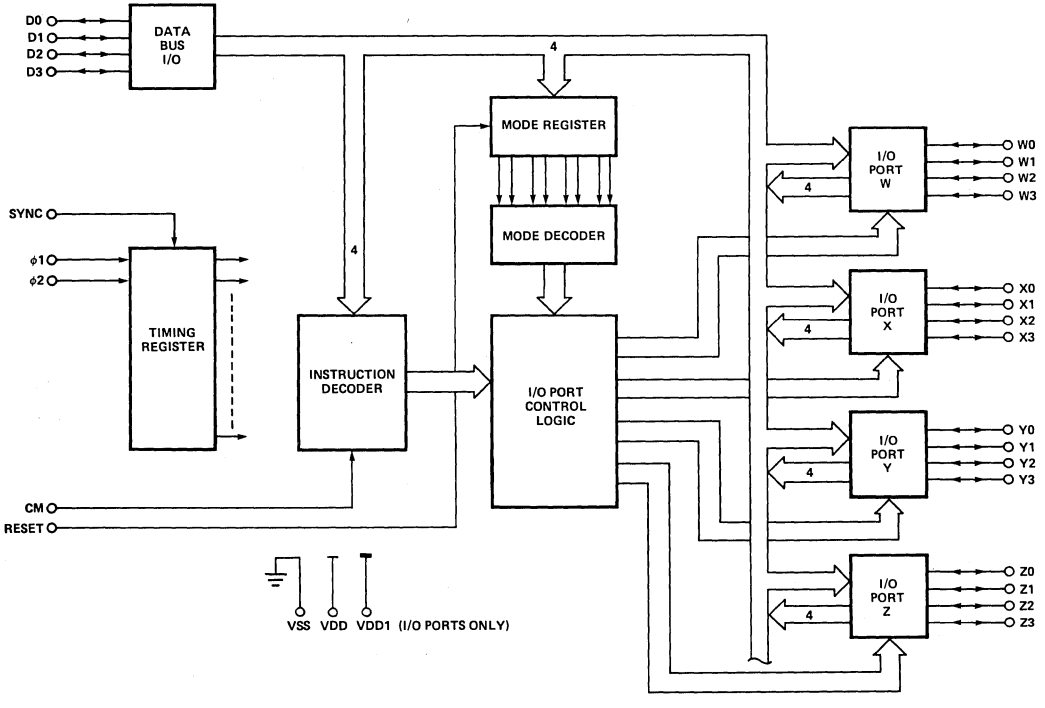


Pin Description

Pin No.	Designation	Function
2-5	D0-D3	Bi-directional data bus. All address, instruction and data communication between processor and I/O ports are transferred on this port.
6	RESET	A negative level (V_{DD}) applied to this pin clears all storage elements, places the 4265 in the Reset Mode and deselects the device.
7	CM	Command input driven by a CM-RAM output of the processor. Used for decoding SRC, RDM, WRM, WMP, SBM, ADM, WR0-3 and RD0-3.
9-10	ϕ1-ϕ2	Non-overlapping clock signals which determine timing.

Pin No.	Designation	Function
8	SYNC	Synchronization signal generated by the processor; indicates the beginning of an instruction.
24-27	W3-W0	Four programmable I/O ports having different functional designation depending on 4265 mode of operation. A data bus "1" negative true (V_{DD}) will appear on a port as a "1" positive true (V_{SS}). These ports are TTL compatible.
20-23	X3-X0	
16-19	Y3-Y0	
11-14	Z3-Z0	
28	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.
15	V_{DD1}	Supply voltage for I/O ports.
1	V_{SS}	Most positive supply voltage (V_{DD1} = 0V, V_{SS} = 5V for TTL I/O ports).
28 = TOTAL PINS		

4265 HARDWARE BLOCK DIAGRAM



MCS-40

4265 PROGRAMMABLE MODES

OPERATING MODES

- Mode 1 — 8-Bit Asynchronous I/O Port (Bidirectional)
  4-Bit Input Port (Unbuffered)
- Mode 2 — 8-Bit Asynchronous I/O Port (Bidirectional)
  4-Bit Output Port
- Mode 3 — 8-Bit Synchronous I/O Port (Bidirectional)
  4-Bit Synchronous Output Port
- Mode 4 — Four 4-Bit Output Ports
- Mode 5 — Three 4-Bit Output Ports
  One 4-Bit Input Port (Unbuffered)
- Mode 6 — Two 4-Bit Output Ports
  Two 4-Bit Input Ports (Unbuffered)
- Mode 7 — One 4-Bit Output Port
  Three 4-Bit Input Ports (Unbuffered)
- Mode 8 — Three 4-Bit Synchronous Output Ports
- Mode 9 — Two 4-Bit Synchronous Output Ports
  One 4-Bit Asynchronous Input Port

OPERATING MODES

- Mode 10 — One 4-Bit Synchronous Output Port
  Two 4-Bit Asynchronous Input Ports
- Mode 11 — Three 4-Bit Asynchronous Input Ports
- Mode 12 — 8-Bit Address Port
  4-Bit Synchronous I/O Port (Bidirectional)
  2 Device Selection Control Signals
- Mode 13 — 8-Bit Address Port
  4-Bit Asynchronous I/O Port (Bidirectional)

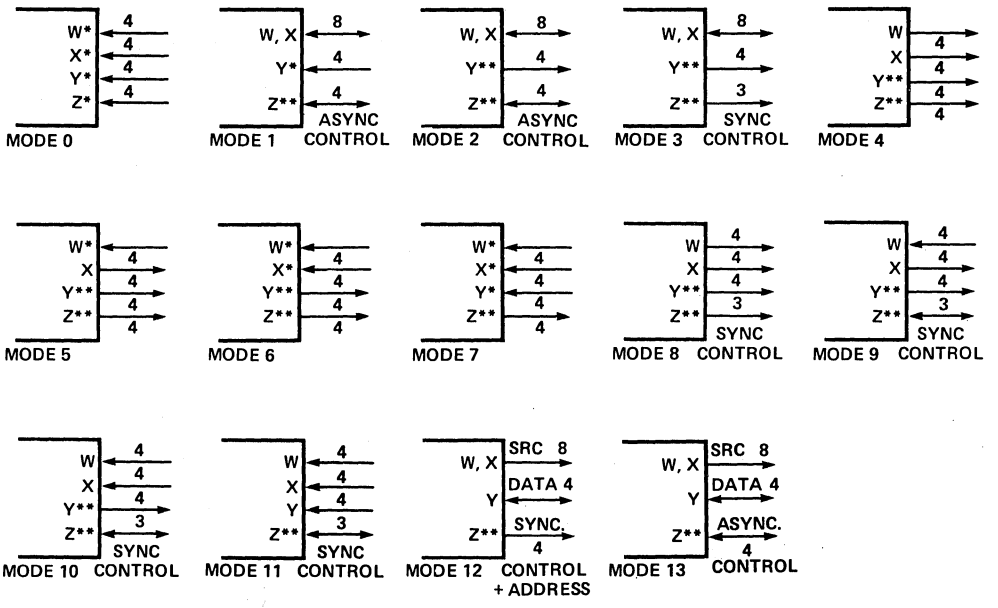
CONTROL AND OPERATING MODE

- Mode 0 — Four 4-Bit Input Ports (Unbuffered)
  Resets I/O Buffers

CONTROL MODES

- Mode 14 — Disables all output buffers, allowing another 4265 to be multiplexed at the port level.
- Mode 15 — Enables output buffers, previous mode restored.

4265 MODE DIAGRAM



* UNBUFFERED INPUT PORTS.

**THE LINES ON THESE PORTS ARE SUBJECT TO THE BIT SET COMMAND.

Functional Description

Control Functions: Two types of operations are possible with the 4265. The device (once selected) can be programmed to one of fourteen basic operating modes. This is accomplished by executing a WMP instruction which sends the 4-bit content of the CPU's Accumulator to the 4265 where it is decoded and used to logically configure the device. A second Control operation makes use of the WRM instruction to select one of eight output lines (Port Y or Z) and perform a SET or RESET operation on that line. This is accomplished by interpreting the 4-bit Accumulator value as follows: The upper three bits select one of eight output latches; the least significant bit determines whether a SET or RESET operation is to be performed.

Data Transfer Functions: The remaining eleven instructions provide four WRITE operations (WR0, WR1, WR2, WR3) and seven READ operations (RD0, RD1, RD2, RD3, ADM, SBM, RDM). These allow data in 4-bit or 8-bit format to be transmitted between the 4265 and external I/O devices or memory devices (all transfers between processor and 4265 are 4-bit transfers).

The sixteen lines of the 4265 are grouped into four ports, four bits each referred to as W, X, Y and Z. The ports can be interrogated by a RD0-3 corresponding to ports W - Z respectively. This means that even when a port is designated as a control port or an output port, the state of the port can be inputted by a RD0-3 instruction (except in modes 12 and 13). The WR0-3 instruction will load the ports W - Z designated outputs. When a port is specifically designated as an input port, it will not respond to an output type instruction (WR0-3, WRM, etc.). See specific mode selection for details.

When port Y or Z is designated an output, regardless of the mode, then it will respond to the Bit Set command. The Bit Set Command allows the user to set the polarity of a single bit without affecting any other bit. This is particularly useful when the output port of interest drives control lines tied to the user system. The user can selectively alter the bit polarity. To alter a bit, the MCS-40 WRM command is utilized.

The 4265 is selected via the CM-RAM line and an appropriate MCS-40™ SRC command. The upper two bits of data at X2 of an SRC instruction with the CM-RAM signal are compared with an address code internal to the 4265. One standard code is available, a code of 2. This allows one 4265 per CM-RAM or up to four per system without additional logic. By using one external decoder and the ability of the DCL (Designate Command Line) instruction to code the CM-RAM lines, up to eight 4265s can be used in a system. Other peripheral devices can share a CM-RAM line with the 4265 (except Mode 12 and 13). For example, a CM-RAM line can contain three 4002 RAMs and one 4265.

The operating modes of the 4265 are selected under program control by the processor. When a 4265 is designed into a specific application, one functional mode is selected. With the possible exception of RESET, ENABLE, and DISABLE, a functional change in mode should not be initiated by the software once the part is designed into a specific application. Since mode selection is done with software, the system's "power up" software routine should sequentially establish the mode of each 4265 prior to "main body" program initiation. The mode selection is accomplished with the accumulator operand of the WMP command.

MODE DEFINITION AND TIMING

Detailed Description of Operating Modes

Table 1 provides a listing of the basic operating modes and the appropriate port configuration as determined by the Accumulator value sent to the 4265 during execution of the WMP instruction. A description of each mode is found in the following sections.

Table 1. Detailed Description of 4265 Operating Modes.

Mode	Port W	Port X	Port Y	Port Z			
0	Input port, unbuffered	Input port, unbuffered	Input port, unbuffered	Input port, unbuffered			
1	Bi-directional; Outputs enabled by signal Z0; When enabled output assumes value loaded by WR0.	Bi-directional; Outputs enabled by signal Z0; When enabled output assumes value loaded by WR1.	Unbuffered input port	Bit 0 Asynchronous input used to enable data out on Ports W, X.	Bit 1 Asynchronous input used to load data to Port W, X input buffers.	Bit 2 Output signal which is normally at V_{SS}. Goes to V_{DD1} on execution of WR 1. Returns to V_{SS} on trailing edge of Z0.	Bit 3 Output signal which is normally at V_{SS}. Goes to V_{DD1} on trailing edge of Z1 and remains at V_{DD1} until execution of RD1.
2	Bi-directional; Output enabled by signal Z0; When enabled output assumes value loaded by WR0.	Bi-directional; Outputs enabled by signal Z0; When enabled output assumes value loaded by WR1.	Buffered output port				
3	Bi-directional; Outputs enabled during WR1 cycle. Output assumes value loaded by WR0.	Bi-directional; Outputs enabled during WR1 cycle. Output assumes value loaded by WR1.	Buffered output port	Synchronous output. Normally at V_{SS}; goes to V_{DD1} during execution of WR 1.	Synchronous output. Normally at V_{SS}; goes to V_{DD1} during RD1 instructions.	Synchronous output. Normally at V_{SS}; goes to V_{DD1} during WR2 instructions.	Unassigned. Line is an output and can be set with WRM. Normally at V_{SS} after mode 3 set.
4	Buffered output port	Buffered output port	Buffered output port	Buffered output port			
5	Unbuffered input port	Buffered output port	Buffered output port	Buffered output port			
6	Unbuffered input port	Unbuffered input port	Buffered output port	Buffered output port			
7	Unbuffered input port	Unbuffered input port	Unbuffered input port	Buffered output port			
8	Buffered output port	Buffered output port	Buffered output port	Output signal normally at V_{SS}; goes to V_{DD1} during WR0.	Output signal normally at V_{SS}; goes to V_{DD1} during WR 1.	Output signal normally at V_{SS}; goes to V_{DD1} during WR2.	Unassigned output. Normally at V_{SS} after mode 8 set.
9	Buffered input port, loaded by signal Z0.	Buffered output port	Buffered output port	Input signal used to load Port W asynchronously.	Output signal normally at V_{SS}; goes to V_{DD1} during WR1.	Output signal normally at V_{SS}; goes to V_{DD1} during WR2.	Unassigned output. Normally at V_{SS} after mode 9 set.
10	Buffered input port, loaded by signal Z0.	Buffered input port, loaded by signal Z1.	Buffered output port	Input signal used to load Port W asynchronously.	Input signal used load Port X asynchronously.	Output signal normally at V_{SS}; goes to V_{DD1} during WR2.	Unassigned output. Normally at V_{SS} after mode 10 set.
11	Buffered input port, loaded by signal Z0.	Buffered input port, loaded by signal Z1.	Buffered input port, loaded by signal Z2.	Input signal used to load Port W asynchronously.	Input signal used to load Port X asynchronously.	Input signal used to load Port Y asynchronously.	Unassigned output. Normally at V_{SS} after mode 11 set.
12	Buffered output port, loaded by SRC instructions—contains upper 4-bits of SRC data.	Buffered output port, loaded by SRC instructions—contains lower 4-bits of SRC data.	Bi-directional; Outputs enabled at any WR instruction; input port unbuffered.	Output signal normally at V_{SS}; goes to V_{DD1} during any WR instruction.	Output signal normally at V_{SS}; goes to V_{DD1} during any RD instruction.	Output signal which is loaded with address bit corresponding to WR or RD operation.	Output signal which is loaded with address bit corresponding to WR or RD operation.
13	Buffered output port, loaded by SRC instructions—contains upper 4-bits of SRC data.	Buffered output port, loaded by SRC instructions—contains lower 4-bits of SRC data.	Bi-directional; Outputs enabled by signal Z0; Inputs loaded by signal Z1.	Asynchronous input used to enable data out on Port Y.	Asynchronous input used to load data to Port Y input buffers.	Output signal normally at V_{SS}; goes to V_{DD1} on execution of WR instruction. Returns to V_{SS} on trailing edge of Z0.	Output signal normally at V_{SS}; goes to V_{DD1} on trailing edge of Z1 and remains at V_{DD1} until execution of RD instruction.
14	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.
15	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.

a. Reset Mode – Mode 0

WMP Operand – 0000

Mode Description: The Reset Mode provides for a programmable reset. Reset will clear all I/O buffers; however, reset will not clear the chip select flip-flop. Hence, the 4265 will remain selected and enabled after a programmable reset. A negative 1 level (V_{DD}) on the RESET pin will cause a response similar to the Reset Mode. The only difference is that the 4265 will be enabled but deselected.

Port Description: Ports W, X, Y, and Z are unbuffered input. Hence, they can be read with RD0-3, transferring the state of the port lines into the accumulator. A positive "1" (V_{SS}) will appear in the accumulator as a negative true "1" (V_{DD}). Port Y will also respond to the RDM, SBM and ADM instructions.

b. 8-Bit Asynchronous I/O Mode with Input – Mode 1

WMP Operand – 0001

Mode Description: The 8-bit I/O mode is used to transfer bi-directional data bytes between the MCS-40™ and the peripheral circuits. Four control lines (Port Z) allow an asynchronous information transfer. Two signals are associated with the input function and two with the output function. Port Y is defined as an unbuffered input.

Port Description

Port W, X — These two ports are combined to transfer 8-bits of I/O under asynchronous control of Port Z. Port W will be loaded with a WR0 and Port X will be loaded with WR1. The WR1 will initiate the write "handshake" on Port Z. When the two ports are interrogated, a sequential RD0 and RD1 will cause the IA line to be deactivated.

Port Y — This port is an unbuffered input, interrogated with an RD2, RDM, ADM or SBM instruction.

Port Z

Z0	OA	Output acknowledge to the 4265 from the users logic. This signal is activated by the users logic (made negative) in response to the OI signal. The OA signal will enable the 4265 output buffer onto Ports W and X. It should be sufficiently long to allow the transfer.
Z2	OI	Output initiate from the 4265. This signal will be generated when Port X has been loaded via a WR1. Port W and Port X should be loaded in the WR0-WR1 sequence. When the OI signal is active, the external device will request data with the OA. The trailing edge of OA will cause the 4265 to remove the OI. If no OA response is received, OI will be active until the next WR0, where it will be removed until the next WR1.

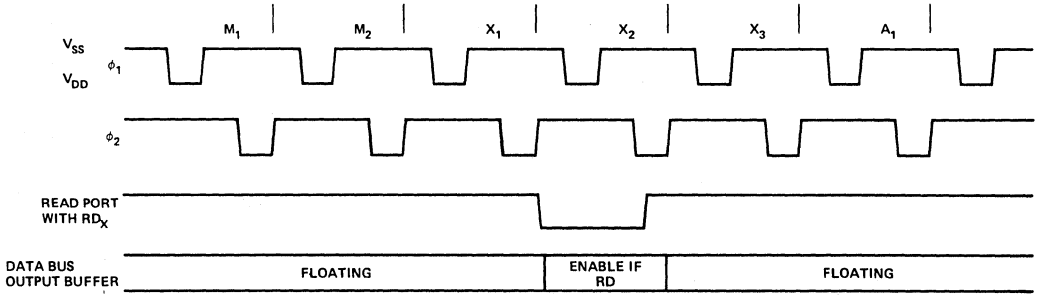


Figure 1. 4265 Mode 0 Timing.

Z1	II	Input initiate to the 4265 from the users logic. The signal will be used as a strobe signal to latch the 8-bit contents of the Port W, X lines into the respective buffers. Data is transferred on the negative to the positive transition. This transition will cause the IA signal to be set.
Z3	IA	Output from the 4265. The IA signal will transition to the positive state when an RD1 command is executed. This indicates that the processor has interrogated Port W, X buffer. The processor should read the data in the sequence of RD0 followed by an RD1.

c. 8-Bit Asynchronous I/O Mode with Output – Mode 2

WMP Operand – 0010

Mode Description: Same as for Mode 1, except Port Y is a buffered output port.

Port Description: Port W, X, Z; same as for Mode 1. Port Y: This port is a buffered output port which can be loaded with a WR2 instruction and can be read by an RD2, RDM, ADM, and SBM.

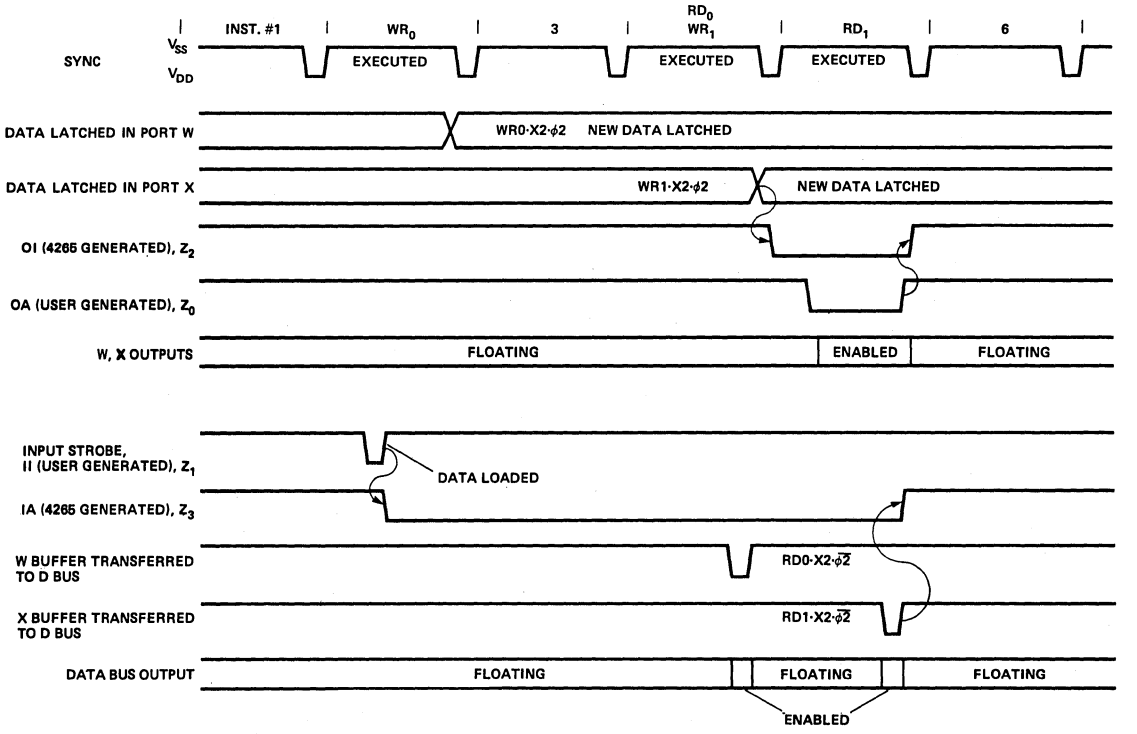


Figure 2. 4265 Modes 1 and 2 Timing.

d. 8-Bit Synchronous I/O Mode with Output — Mode 3

WMP Operand — 0011

Mode Description: This mode is functionally similar to Modes 1 and 2 in terms of its byte transfer feature. However, the transfer control is synchronous. Port W, X are buffered outputs or unbuffered inputs, depending on the direction of transfer. Port Z provides the synchronous strobe control. Port Y is a buffered output port.

Port Description

Port W, X — These two ports are combined to transfer bi-directional 8-bit information under synchronous control. Output data should be loaded into Ports W, X with the WR0-WR1 sequence. The input of information should be sequentially read with an RD0 followed by an RD1.

Port Y — This port is a 4-bit output port. Information is valid during the output strobe of a WR2 command. The output strobe is the Z2 line of the Z port. This port may also be read with an RD2, RDM, ADM and SBM.

Port Z

Z0 OS — Output strobe from 4265. This line is valid during a WR1 command. Information from the output buffers of Ports W and X is present at Ports W and X output lines only during the signal.

Z1 IS — Input strobe from 4265. This line is valid during an RD0 command. Information is taken off the Port W, X lines and is latched in the Port W, X buffers. The RD0 will read the information pertaining to Port W. RD1 will input information pertaining to Port X. The ports must be read by RD0 followed by an RD1. Data will be latched in the W and X Ports with the RD0. Information should be valid at the trailing edge of IS.

Z2 YS — Port Y strobe from the 4265. This line is valid during a WR2 command. Information will be valid at the Port Y output buffer during this strobe.

Z3 — This line is not used. It can be bit set/reset under program control.

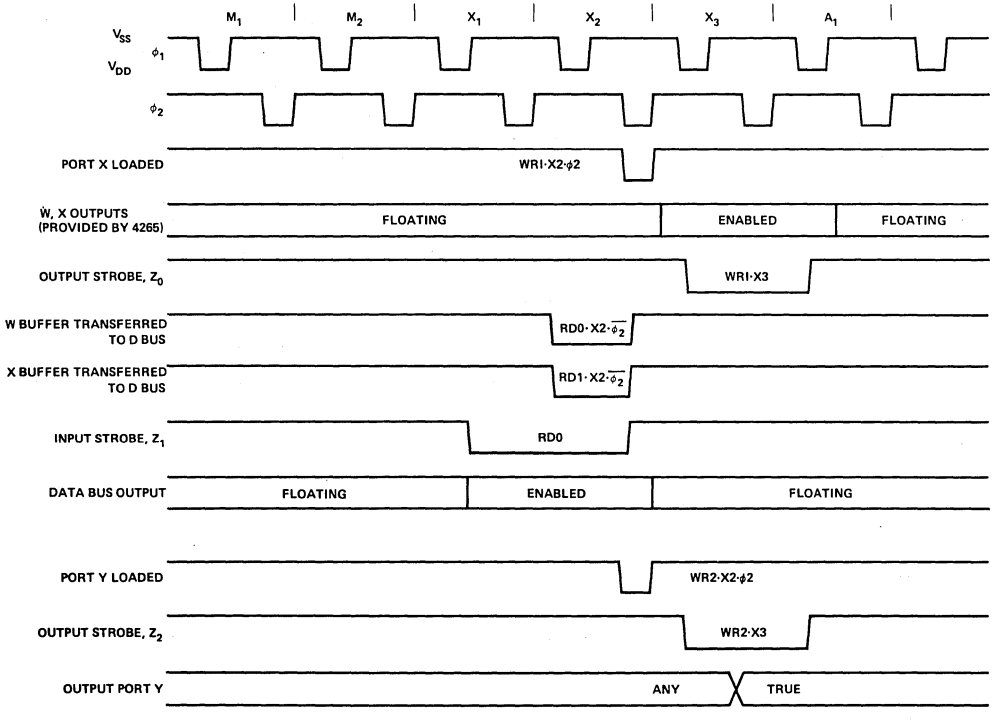


Figure 3. 4265 Mode 3 Timing.

e. Four Port Programmable I/O Modes — Modes 4-7

WMP Operand — 0100-0111

Mode Description: These modes consist of four combinations of static buffered outputs and unbuffered inputs. When combined with the Reset Mode, all combinations of inputs and outputs on four ports are possible.

Port Description: The following five modes have static buffered outputs (0) or unbuffered inputs (I).

WMP	Port:	W	X	Y	Z
0100		0	0	0	0
0101		I	0	0	0
0110		I	I	0	0
0111		I	I	I	0
0000 (reset mode)		I	I	I	I

Those ports of Y and Z designated outputs are subject to bit set/reset capability. All output buffers may be read with the respective RDx (RD0-RD3). Port Y will respond to RDM, ADM and SBM in addition to RD2.

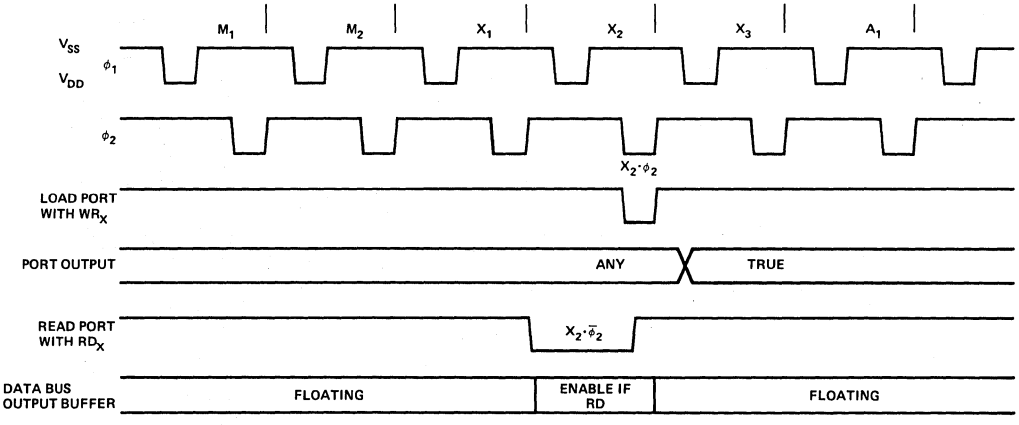


Figure 4. 4265 Modes 4-7 Timing.

f. Three Port Programmable I/O Mode with Synchronous Output and Asynchronous Input Port – Modes 8-11

WMP Operand – 1000-1011

Mode Description: Each 4-bit port can be configured as a buffered input or buffered output port and each has its own control line for synchronizing data transfers. As an example, if in Mode 8, when the processor executes a WR0 instruction, 4-bits of data are transferred to the Port W output buffer and subsequently to the Port W output lines. Output Strobe Z0 serves as a data valid signal which can be used by external logic to latch the data. In Mode 11, Input Strobe Z0 is used to latch the 4-bit data appearing on the Port W lines into the Port W input buffer. The Input Strobe is user generated.

Port Description: The following five modes have synchronous outputs (0) or asynchronous inputs (1):

WMP	Port:	W	X	Y	Z0	Z1	Z2	Z3
1000		0	0	0	W	W	W	X
1001		I	0	0	R	W	W	X
1010		I	I	0	R	R	W	X
1011		I	I	I	R	R	R	X

Where: R = input strobe independent of instruction executed
W = output strobe (WR0-2) from 4265
X = not used

Port Y will respond to RDM, SBM and ADM in the same way as an RD2. Z3 is unused and may be bit set/reset. All output buffers may also be read with the respective RDx.

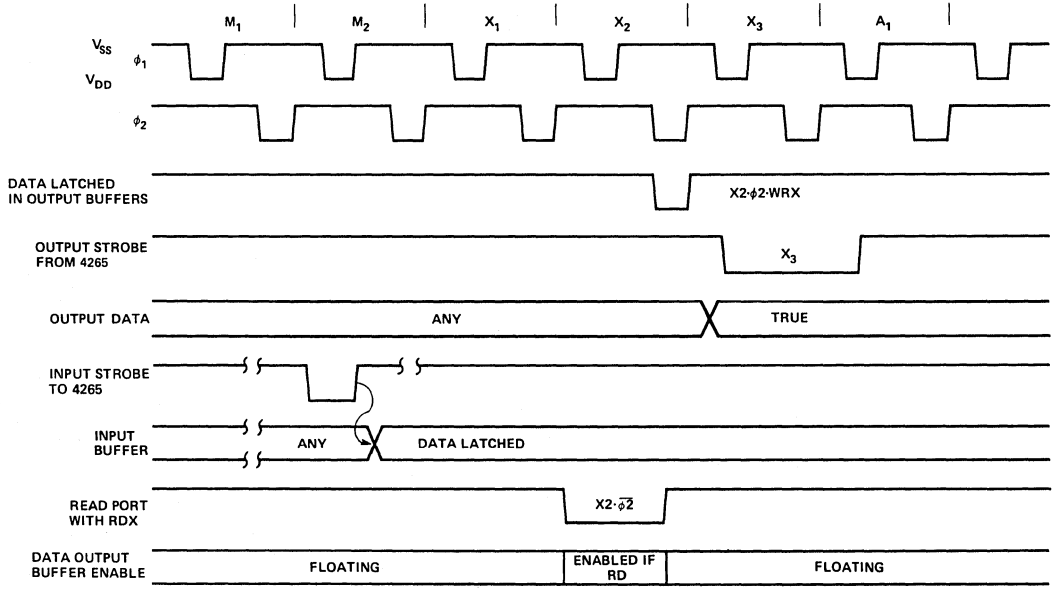


Figure 5. 4265 Modes 8-11 Timing.

g. 4-Bit I/O with 8-Bit SRC Address and 4-Bit Synchronous Control Port – Mode 12

WMP Operand – 1100

Mode Description: In this mode, the most recent 8-bit SRC operand is displayed on Port W and X. The 4265 will treat all SRC instructions as being valid as long as the CM-RAM line for this 4265 has been selected by an appropriate DCL (Designate Command Line) instruction. Ports W and X will change each time they receive an SRC and CM-RAM. The 4-bit data port (Port Y) will perform bi-directional synchronous I/O. The port output buffer may be loaded with a WR0-3 and the port input buffer will be read with RD0-RD3, RDM, SBM or ADM. The control port will provide mutually exclusive input or output strobes depending on the current instruction. Two of the control lines may be used for device selection. This mode can be used to interface up to 1K of external storage (RAM-2111, 4101, 5101) or a multitude of external I/O devices. Once this mode is programmed, all SRC values will not be treated as 4265 selection or deselection instructions.

Port Description

Port W, X — This port will display the most recent SRC and will be altered with each SRC when selected. Otherwise, the output is static.

Port Y — This is a bi-directional data port that will latch data with a RD0-RD3, RDM, ADM, and SBM. The port will output data with a WR0-WR3.

Port Z

Z0 OS — Output strobe from 4265. Active during WR0-WR3. Data will be valid during this strobe.

Z1 IS — Input strobe from 4265. Active during RD0-RD3, RDM, SBM, and ADM. The leading edge of this strobe will cause the user to provide valid data to be latched by Port Y by the trailing edge of IS.

Z2, Z3 — 2-bit address port used for memory or device selection. Both lines will be preset to 00 by selection of this mode. They will retain the value of the previous RDx or WRx instruction so that each selection can respond to RDM, SBM and ADM. If, for example an I/O sequence consists of an RD3 followed by an ADM, Z3 and Z2 will be at 11 state by the RD3 and remain in that state for the ADM command. If the third I/O command is a WR0, the Z3 and Z2 will be placed to the 00 state.

Effect of RDx and WRx Instructions:

Z3	Z2	
0	0	RD0, WR0
0	1	RD1, WR1
1	0	RD2, WR2
1	1	RD3, WR3
No Change		RDM, ADM, SBM

(Positive True)

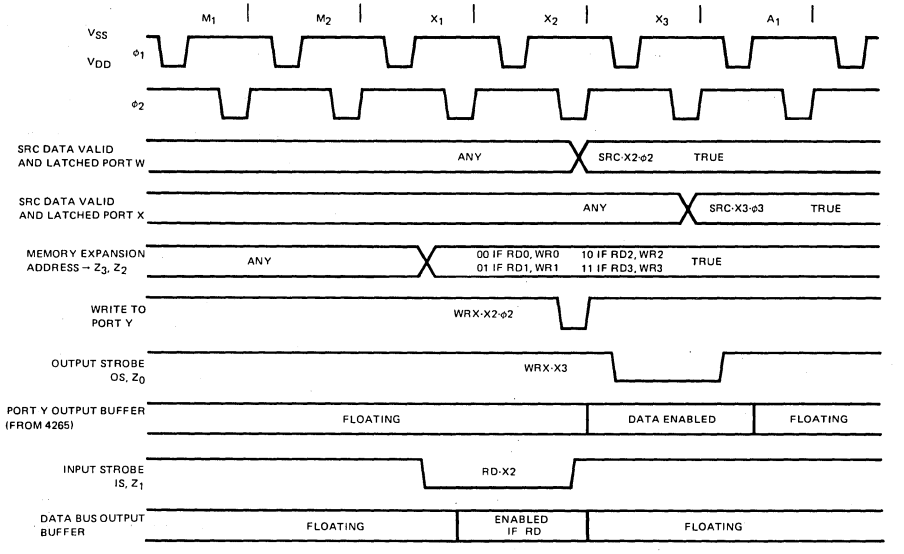


Figure 6. 4265 Mode 12 Timing.

h. 4-Bit I/O Mode with 8-Bit Address Port and 4-Bit Asynchronous Control Port — Mode 13

WMP Operand — 1101

Mode Description: This mode is functionally similar to Mode 12. Port W, X are loaded with the SRC value. Port Y is a bi-directional data port. Port Z is a 4-bit asynchronous control port similar to Mode 1 and 2.

Port Description

Port W, X		Same as Mode 12.
Port Y		Bi-directional port similar to Port W and Port X in mode 1.
Port Z		
Z0	OA*	Output acknowledge to 4265.
Z2	OI*	Output initiate from 4265, active during WRx.
Z1	II*	Input initiate to 4265.
Z3	IA*	Input acknowledge from 4265 active during RDx, RDM, ADM or SBM.

*Refer to Mode 1, Port Z. Note that in mode 13, Port Z controls data transmission in Port Y, not Ports W and X.

i. Disable/Enable

WMP Operands 1110 and 1111 do not cause mode change; they disable or enable the 4265 GP I/O.

WMP 1110 - chip disable:

a. All output buffers are disabled - I/O lines are in floating conditions.
b. The 4265's status (mode, chip select FF, data buffers) is not changed. Hence:
   1. Previous buffered inputs can be read by the CPU from designated ports (a disabled 4265 cannot have its input buffers loaded).
   2. Data on unbuffered inputs can be read directly from external lines.
   3. Previous buffered outputs can be changed on designated ports.
   4. Bit set/reset can be initiated.
   5. Any mode change can be initiated.
   6. The chip can be deselected by an SRC or by a RESET signal.

WMP 1111 - chip enable:
Restoration of normal operation, according to existing mode.

Note: When the 4265 is transferred from reset mode to any other mode, the chip is automatically enabled, so that no programmed enabling is required after reset.

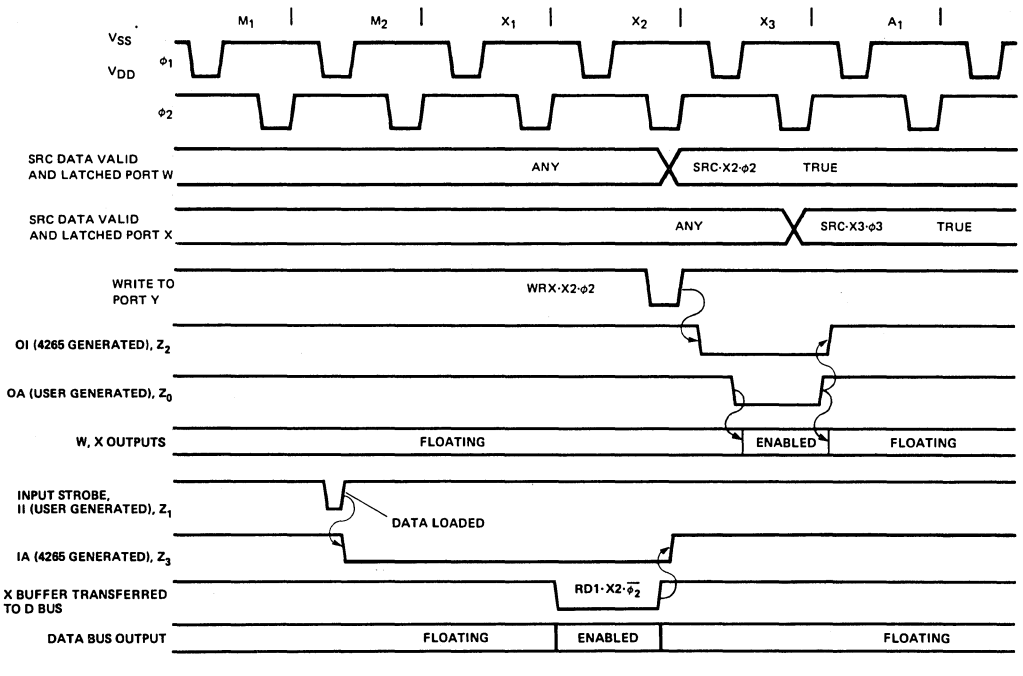


Figure 7. 4265 Mode 13 Timing.

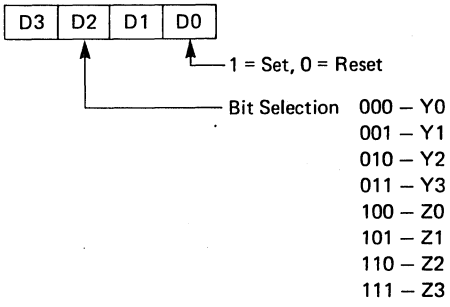
An unselected 4265 can have its input buffers loaded by a user generated strobe if it is in a buffered input mode. A disabled 4265 cannot have its input buffers loaded. Execution of a RDx instruction will result in transfer of the contents of the appropriate input or output buffer for a previously buffered port regardless of whether the 4265 is enabled. If the input was previously unbuffered and the 4265 is disabled, the contents of the port I/O lines will be transferred to the CPU with an RDx. DISABLE and ENABLE do not cause a change from a previously designated mode.

4265 States After Reset and Mode Change

A reset 4265 is automatically enabled and is in Mode 0. If reset occurs by means of external RESET signal, the 4265 will also be deselected. Any mode change which changes Port Z to a control port will reset the Port Z output buffers to their "off" state (V_{SS}). Z_2 and Z_3 in mode 12 are an exception in that these lines go to an inactive state of V_{DD1}. Note that Port Z is a control port in all modes except modes 4-7 and RESET mode. Any mode change which leaves Port Z in a non-control port will leave Port Z output buffers in their previous state.

Bit Set/Reset Operation

This function is performed by decoding the accumulator operand of the WRM instruction. This function can be used in any output port of the programmed configurations and allows individual bit control on Ports Y and Z. Decoding of the WRM operand is as follows:



Care should be taken when bit setting and resetting control bits of Port Z as these bits will also be changing as a function of their synchronous or asynchronous control functions.

4265 I/O Instructions

Table 2 provides a summary of MCS-40 I/O instructions used with the 4265.

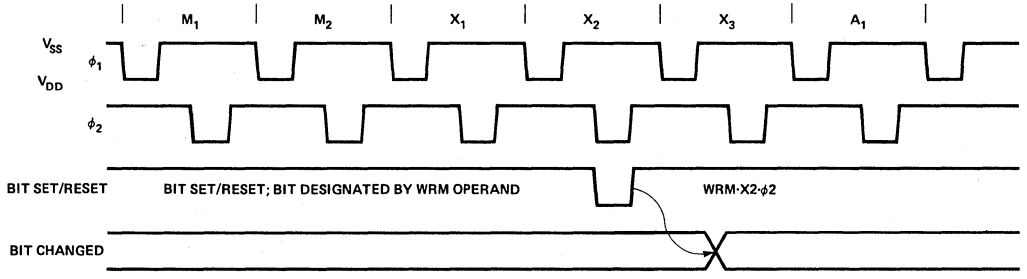


Figure 8. Bit Set/Reset Operation Timing.

Table 2. 4265 I/O Instruction.

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION		
				Mode Independent Operations		
E0	WRM	1 1 1 0	0 0 0 0	The port Y or port Z bit designated by D_3 D_2 D_1 of the accumulator is set or reset according to D_0 (1=set, 0=reset).[1]		
E1	WMP	1 1 1 0	0 0 0 1	Sets the mode of the 4265 to the value contained in the accumulator.[2]		
				Mode Dependent Operations		
				Mode 1-3	**Mode 0, 4-11**	**Mode 12 and 13**
2-	SRC	0 0 1 0	R R R 1	For modes 0-11, the contents of register pair RRR are used to select the 4265 chip (first two bits of first register will contain 10 or 11, depending on chip address)		(RRR_{even})→ Port W (RRR_{odd})→ Port X
E4	WR0	1 1 1 0	0 1 0 0	(ACC)→ Port W	(ACC)→ Port W[1]	(ACC)→ Port Y
E5	WR1	1 1 1 0	0 1 0 1	(ACC)→ Port X	(ACC)→ Port X[1]	(ACC)→ Port Y
E6	WR2	1 1 1 0	0 1 1 0	(ACC)→ Port Y[1]	(ACC)→ Port Y[1]	(ACC)→ Port Y
E7	WR3	1 1 1 0	0 1 1 1	—	(ACC)→ Port Z[1,3]	(ACC)→ Port Y
EC	RD0	1 1 1 0	1 1 0 0	(Port W)→ ACC	(Port W)→ ACC	(Port Y)→ ACC
ED	RD1	1 1 1 0	1 1 0 1	(Port X)→ ACC	(Port X)→ ACC	(Port Y)→ ACC
EE	RD2	1 1 1 0	1 1 1 0	(Port Y)→ ACC	(Port Y)→ ACC	(Port Y)→ ACC
EF	RD3	1 1 1 0	1 1 1 1	(Port Z)→ ACC	(Port Z)→ ACC	(Port Y)→ ACC
E9	RDM	1 1 1 0	1 0 0 1	(Port Y)→ ACC	(Port Y)→ ACC	(Port Y)→ ACC
EB	ADM	1 1 1 0	1 0 1 1	(Port Y)+(ACC) +CY→ACC	(Port Y)+ACC +CY→ACC	(Port Y)+ACC +CY→ACC
E8	SBM	1 1 1 0	1 0 0 0	(ACC)−(Port Y) −CY→ACC	(ACC)−(Port Y) −CY→ACC	(ACC)−(Port Y) −CY→ACC

NOTES:
1. Action if Port is designated as Output Port; otherwise, no action.
2. WMP 1110 disables all I/O ports. WMP 1111 enables all I/O ports. In both cases, the mode is not changed.
3. No action in Modes 8-11.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400nsec; $t_{\phi D2}$ = 150nsec; V_{DD1} = V_{SS} -5V; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OH}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Supply Current		35		mA	T_A = 25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IHD}	Data Bus Inputs	V_{SS}-1.5		V_{SS}+.3	V	
V_{IHIO}	I/O Port Inputs	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILD}	Data Bus Inputs	V_{DD}		V_{SS}-5.5	V	
V_{ILIO}	I/O Port Inputs	V_{DD}		V_{SS}-4.2	V	
V_{ILR}	Reset Input	V_{DD}		V_{SS}-4.2	V	
V_{IHR}	Reset Input	V_{SS}-1.5		V_{SS}+.3	V	
OUTPUT CHARACTERISTICS						
V_{OHD}	Data Bus Outputs	V_{SS}-.5	V_{SS}		V	
V_{OHIO}	I/O Port Outputs	V_{SS}-.5			V	I_{OH} = -100μA
V_{OLD}	Data Bus Outputs	V_{SS}-12		V_{SS}-6.5		
V_{OLIO}	I/O Port W,X,Y Outputs			V_{DD1}+.45		I_{OL} = 400μA
V_{OLZ}	I/O Port Z Outputs			V_{DD1}+.45		I_{OL} = 1.6mA

A.C. Characteristics

T_A = 0°C to 70°C, V_{SS} -V_{DD} = 15V ±5%.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Time			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF

I/O Ports[4]

t_1	Output Settling Time		350		ns	Output Ports
t_{2A}	Output Settling Time		400		ns	Bidirectional I/O Ports (Asynchronous)
t_{2B}	Output Hold Time		400		ns	Bidirectional I/O Ports (Asynchronous)
t_{3A}	Output Settling Time		400		ns	Bidirectional I/O Ports (Synchronous)
t_{3B}	Output Hold Time		100		ns	Bidirectional I/O Ports (Synchronous)
t_{3C}	Output Strobe Write Time		300		ns	Mode 12
t_{3D}	Output Strobe Hold Time		300		ns	Mode 12
t_4	I.S. Delay		200		ns	Z_1, Modes 3, 12
t_5	"Page Select" Outputs Settling Time		600		ns	Z_2, Z_3, Mode 12
t_{6A}	Input Write Time		700		ns	Unbufferred Input Ports(Ports W,X,Y)
t_{6B}	Input Hold Time		0		ns	Unbufferred Input Ports(Ports W,X,Y)

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

4. For $C_{DATA\ BUS}$ = 500pF, $C_{PORTS\ W,X,Y}$ = 100pF; $C_{PORT\ Z}$ = 50pF.

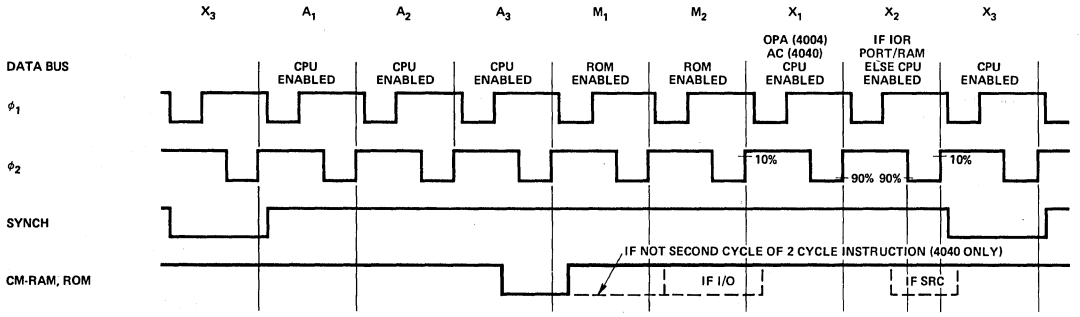


Figure 9. Timing Diagram.

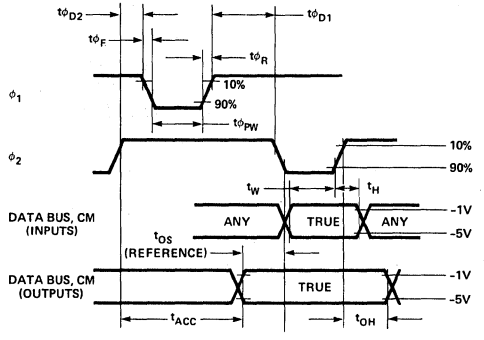


Figure 10. Timing Detail.

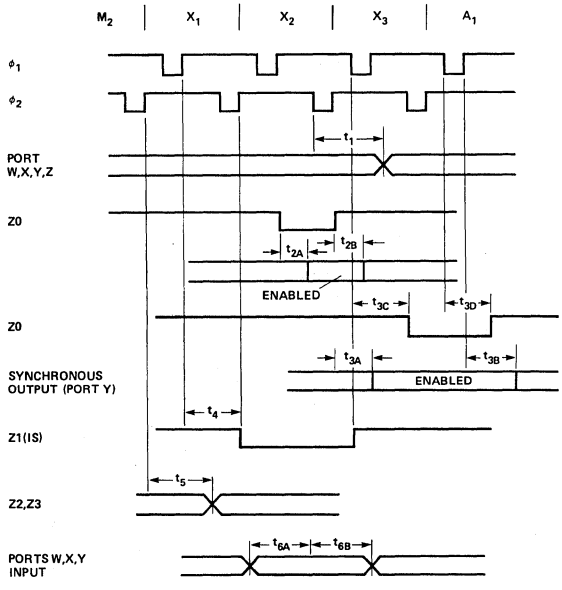


Figure 11. 4265 I/O Timing Diagram.

PROGRAMMABLE KEYBOARD DISPLAY DEVICE

(Samples Available 1st Quarter, 1976)

Keyboard Features:

- **Programmable to Interface to Encoded Keyboard (8-bit code), 64-Key Scanned Keyboard (expandable to 128 keys) or Sensor Matrix (64 sensors)**
- **8 Character FIFO Character Buffer (or RAM in Sensor Mode)**
- **2 Key Rollover and Key Debounce**
- **External Interrupt Line to Indicate When a Character Has Been Entered in Character Buffer**

Display Features:

- **Programmable to Interface to Individually Scanned Displays or Burrough's Self-Scan* Drive (16, 18, or 20 Characters)**
- **Two 16 x 4 Display Registers Recirculated Synchronously with Keyboard Scan Lines to Give Automatic Display Refresh**
- **Display Registers Loadable and Readable Selectively or Sequentially**
- **40 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C (-40° to +85°C Operating Range to be Available Second Quarter 1976)**

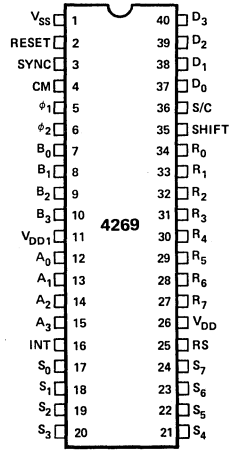
The 4269 has two separate and distinct sections: the keyboard section and the display section. The keyboard section can interface to a range of devices from a matrix of toggle or thumb switches such as found on an instrument panel up to a full typewriter style keyboard. The display section can interface to a range of devices from an array of individual LED indicators up to a gas discharge alphanumeric display.

The 4269 Programmable Keyboard Display (PKD) relieves the 4004 or 4040 CPU from continuously scanning a switch array or refreshing a display under software control. This greatly expands the CPU throughput. The 4269 can scan up to an 8 x 8 keyboard or sensor matrix (or a 2 x 8 x 8 keyboard with the use of the shift or control key input). The display portion can continuously refresh either a single 16 x 8 alphanumeric display; a single 8 x 8 alphanumeric display; a dual 16 x 4 digit display; a single 32 x 4 digit display; a 16 x 6, 18 x 6 or 20 x 6 alphanumeric gas discharge display such as the Burroughs Self-Scan*; or an array of 128 indicators.

*Self-Scan is a registered trademark of the Burroughs Corporation.

MCS-40

PIN CONFIGURATION



Pin Description

Pin No.	Designation	Function
37-40	D0-D3	Bi-directional data bus. All address, instruction and data communication between the CPU and the PKD are transmitted on these 4 pins.
5-6	ϕ_1-ϕ_2	Non-overlapping clock signals which are used to generate the basic chip timing.
2	RESET	RESET input. A low level (V_{DD}) applied to this input resets the PKD.
1	V_{SS}	Most positive supply voltage.
26	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V ±5%.
3	SYNC	Synchronization input signal driven by SYNC output of the CPU.
4	CM	Command input driven by a CM-RAM output of processor.
17-24	S0-S7	These pins are scan outputs which are used for driving either the key switch or sensor matrix and/or for strobing the display digits. Each line is mutually exclusive, active high (V_{SS}), open drain.
25	RS	The RS pin is toggled for each complete scan of the S drive. This allows for the scan of 16 digits of display data. RS=V_{SS} for the last 8 digits. This line is open drain.
12-15 7-10	A0-A3 B0-B3	These two ports provide two 16 x 4 recirculating display register outputs which are synchronized to the S drive scan. In the gas discharge display mode, A3 is reset and A2 is the clock to the gas discharge display. The 16, 18, or 20 recirculating data characters (6 bits wide) are not synchronized with the S drive scan in the gas discharge mode.
34-28	R0-R7	These pins are the return sense inputs which are connected to the 8 drive lines via the scanned key or sensor matrix. They are pulled to a low state (V_{DD}) in the sensor mode, pulsed low (V_{DD}) in the scanned keyboard mode, and pulled high upon switch closure. They are floating in the encoded keyboard mode.
35	SHIFT	This is the shift input. It is active high (V_{SS}). This pin is functional only in the scanned keyboard mode.
16	INT	This output is used to indicate when a keyboard or sensor character has been entered into the buffer. It is active low (V_{DD1}), open-sourced and may be "OR" -ed with other 4040 interrupt inputs.
11	V_{DD1}	Supply voltage for display register ports A and B and INT.
36	S/C	This pin is the control key input from the keyboard in the scanned mode. In encoded keyboard mode, this pin can be used to input the strobe pulse from an external keyboard encoder.

Functional Description

General

The 4269 Programmable Keyboard/Display (PKD) device provides an intelligent interface between an MCS-40 CPU and the keyboard and display portions of an MCS-40 design. The 4269's functions thus allow the use of sophisticated keyboards and displays without placing a large load on the CPU.

The MCS-40 data bus will provide the path for information transfer between the PKD and the 4040 or 4004 CPU. The PKD can be programmed to operate in one of three input modes and one of four output modes as defined by an instruction from the CPU. The modes are:

Input
- Sensor, Scanned
- Keyboard, Scanned
- Encoded Keyboard

Output
- Individually Scanned Display Drive
- Self-Scan Drive: 16 Characters
  18 Characters
  20 Characters

The 4269 resides on a CM-RAM line of an MCS-40 system and has a fixed RAM address, #1. Hence, there can be up to four PKD per system without additional logic, one per CM-RAM. The PKD can be accessed with the MCS-40 I/O instruction set to interrogate the keyboard buffer FIFO/sensor RAM and load or read the display registers.

The following is a list of the major keyboard features of the 4269:

1. Switch matrix, organized as an 8 x 8 scanned matrix with shift or control inputs allowing for up to 128 key inputs.
2. Two key roll over; N-key roll over capability if provided by encoded keyboards.
3. Eight character first-in-first-out (FIFO) character buffer (or RAM in the Sensor Mode).
4. External interrupt line to indicate when a character has been entered in the buffer.
5. Fixed key bounce delay of approximately 11 msec in the scanned keyboard mode @ 740 kHz MCS-40 clocks.
6. Status buffer to indicate the number of characters in the keyboard FIFO and keyboard character over-entry.
7. Sensor matrix interface with up to 64 intersections.

The 4269's major display features are:

1. Two 16 x 4 display registers which are recirculated synchronously with keyboard scan lines (at a scan frequency of 180 Hz). This allows for a free standing, scanned readout composed of individual displays.

2. Capability to drive 16, 18, or 20 character gas discharge displays directly via a 20 x 6 display register.
3. Registers are loadable and readable selectively or sequentially.

Mode Selection

The CPU communicates with the 4269 PKD by first selecting it with an SRC (Send Register Control) instruction. The first two bits of the index register pair referenced by the SRC contain 01, the binary address of the 4269 on the CM-RAM line. The 4269 is disabled until it is addressed by a first SRC. After the first SRC, a WR0 instruction is used to set the keyboard and display modes of the 4269 PKD. The CPU's accumulator will contain the information used for setting the PKD modes. The definition of a WR0 as used for a 4269 is given below:

Mnemonic	Instruction Code
WR0	1110 0100

Set the input mode and output mode of the 4269 according to the value contained in the accumulator as follows:

D_3D_2

0 0 Individual, Scanned Displays
0 1 Gas Discharge, 20 Characters
1 0 Gas Discharge, 18 Characters
1 1 Gas Discharge, 16 Characters

D_1D_0

0 0 Sensor, Scanned
0 1 Scanned Keyboard
1 0 Encoded Keyboard, Not Scanned
1 1 Not Used

After the 4269 has been reset by the external RESET signal, the keyboard input mode is set to scanned keyboard mode and the display output mode is set to gas discharge, 16 character mode. Thus, if these modes are the desired input and output modes, it is not necessary to execute the WR0 mode setting instruction.

Internal Display Registers and Pointer

The 4269 has two 16x4 display registers referred to as Display Register A and Display Register B. These two registers can be operated in the individual, scanned display mode as:

1. Two 16 x 4 hexadecimal displays;
2. One 32 x 4 hexadecimal display;
3. One 8 x 8 alphanumeric display;
4. One 16 x 8 alphanumeric display; or
5. An array of 128 indicators.

In the gas discharge modes, the A and B registers are combined and operated as a 6 x 16, 6 x 18 or 6 x 20 register. For a given 6-bit character, the least significant 4-bits will be located in a 4-bit B register location and the two most significant bits in D_1 and D_0 of the corresponding A register location.

For operations on the display registers, the 4269 PKD maintains an internal display register pointer which points to a 4-bit character in the A or B display register.

For the individual, scanned display mode, CPU I/O instructions can be addressed to either Display Register A or Display Register B, according to the register selected by an SRC instruction preceding the I/O instruction. The internal display register pointer can then be set or incremented for addressing characters in either the A or B register.

For gas discharge modes, the internal pointer can be automatically incremented, in an alternating pattern between registers A and B. The alternation pattern is A_0, B_0, A_1, B_1, etc.

In the individual, scanned display mode, the 4-bit characters of Display Register A are outputted on the A_0-A_3 lines. The 4-bit characters of Display Register B are outputted on the B_0-B_3 lines. In the gas discharge modes, the A_0-A_1 and B_0-B_3 lines output the 6-bit character. The A_2 line serves as the clock to the gas discharge display and the A_3 line as the reset to the display.

Synchronization of Scan and Return Lines

In the scanned keyboard and scanned sensor modes a logical one is shifted through a field of zeros in eight Scan(S) lines. Each S Scan line can be used to source a row of eight keys or sensors. All rows of the contact keyboard or sensor matrix will be OR-tied to the eight Return (R) lines. Thus, since only one row will be enabled due to the synchronized ones in the Scan lines, each row of the keyboard or sensor matrix can be read into the Return lines and stored in the Keyboard FIFO/Sensor RAM at the proper RAM location. The 4269 will control all of these operations automatically once it is set to the appropriate keyboard mode.

The Scan Lines are also used in the individual, scanned display mode to select one of eight display characters. The display character itself will be outputted on the A_0-A_3 or B_0-B_3 output lines. The RS output line, which is toggled for each complete scan of the S lines, allows one of sixteen A or B register display characters to be addressed. Again, the 4269 will automatically control the operation of the S and RS lines to continuously read out the characters in the 4269's internal A and B Display Registers and thus continuously refresh the actual display devices.

Note that the Scan lines can be used with both the keyboard and display interfaces since both functions require the same function, i.e., a synchronized shifting of a logical one through a field of zeros.

Software Operation

The WR0 operates on the 4269 PKD completely independent of mode as it actually sets the mode as has already been described. The WR3 is mode independent except for a blanking code and operates as shown below:

WR3

Clears the keyboard/display logic and fills the display RAM with all blanks. The display outputs are also blanked. (Blank code is all logical "1"s for individual, scanned display mode and hex 20 for the gas discharge modes.)

MODE SPECIFIC OPERATIONS

Individual, Scanned Display Mode

The instructions which are used in the individual, scanned display mode are described below:

Mnemonic **Instruction Code**
SRC **0010** **RRR1**

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted for individual, scanned display mode as follows:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 0 0	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Display Register A with the A output lines outputting display characters synchronized with the S Scan lines.
0 1 0 1	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Display Register B with the B output lines outputting display characters synchronized with the S Scan lines.
0 1 1 0	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Register A with Register A output lines being placed at V_{SS} level.
0 1 1 1	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Register B with Register B output lines being placed at V_{SS} level.

WR1 **1110** **0101**

Resets the internal display register pointer to 0 and forces display memory to blank state. Upper two bits of ACC select length of display as follows:

D_3

0 Display B is 16 nibbles deep.
1 Display B is 8 nibbles deep.

D_2

0 Display A is 16 nibbles deep.
1 Display A is 8 nibbles deep.

WRM **1110** **0000**

Loads the contents of the register addressed by the internal display register pointer with the contents of ACC; then advances the displayed data by one digit in relation to the scan line timing and increments the display register pointer.

RDM **1110** **1001**

Loads ACC with the contents of the register addressed by the display register pointer and then increments the display register pointer.

WMP **1110** **0001**

Loads the contents of the register addressed by the display register pointer with the contents of ACC.

RD3 **1110** **1111**

Loads ACC with the contents of the display register pointed to by the display register pointer.

ADM **1110** **1011**

Adds the contents of the display register pointed to by the display register pointer to the accumulator with carry.

SBM **1110** **1000**

Substracts the contents of the display register pointed to by the display register pointer from the accumulator with borrow.

NOTES:

1. If Display A or B is set to 8 nibbles deep, each digit of the display will have double the ON duty-cycle that it would have in the 16 nibble deep setting (360 Hz scan cycle vs. 180 Hz for 16 nibble deep).
2. External resetting initializes the Display A and Display B configurations to 16 nibbles deep.
3. The displayed nibbles in the 8 deep configuration will be from the least significant 8 characters of the display register. The remaining eight words remain available for random data storage by the CPU.
4. The internal display register pointer will increment through all 16 register words, regardless of the display length (8 or 16) for WRM/RDM instructions unless the pointer is reset by an appropriate SRC instruction. In the WRM case, the Display Register A or B's entire contents (used and unused portions) will be rotated.
5. An interface to a 32 x 4 hexadecimal display requires only that software recognize the A and B Display registers as the upper and lower halves of a single display.
6. An interface to a 16 x 8 alphanumeric display requires that software load the upper and lower 4-bits in the A and B registers in an appropriate alternating pattern. SRC instructions will have to proceed each load or read instruction to select the A or B half of the character.
7. If the LSD of a 16 character display is assigned to be the 15th character scanned ($S_7 = V_{SS}$ and RS = V_{SS}), and the MSD, the first character (#0) scanned ($S_0 = V_{SS}$ and RS = V_{DD}), and if loading is started at display register character 0, successive WRM instructions will shift the display data from the LSD to the MSD as in a calculator. Note that data will then be read back MSD to LSD with the RDM instruction, starting at register 0.

Gas Discharge Modes

The instructions which are used in the gas discharge display modes are described below.

Mnemonic **Instruction Code**
SRC **0010** **RRR1**

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted for gas discharge modes as follows:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 0 0	$n_3n_2n_1n_0$	Selects the nth display register character of Display Register A with display outputs continuing to output the contents of Display Registers A and B.
0 1 0 1	$n_3n_2n_3n_0$	Selects the nth display register character of Display Register B with the display outputs continuing to output the contents of Display Registers A and B.
0 1 1 0	$n_3n_2n_1n_0$	Selects the nth display register character of Display Register A and blanks the A and B display output (with hex 20).
0 1 1 1	$n_3n_2n_1n_0$	Selects the nth display register character of Display Register B and blanks the A and B display output (with hex 20).

WR1

Resets the internal display register pointer to Display Register A position 0 and forces the Display Registers to the blank code.

Note: A WR1 should follow a WR0 which changes the display mode.

WRM 1110 0000

Loads the contents of the display register location addressed by the internal display register pointer with the contents of ACC; then advances the displayed data by one digit in relation to the scan line timing, and increments the display register pointer. The display register pointer alternates between the A and B registers.

RDM 1110 1001

Loads ACC with the contents of the display register location addressed by the display register pointer and then increments the display register pointer. The display register pointer alternates between the A and B registers.

WMP 1110 0001

Loads the contents of the display register location addressed by the display register pointer with the contents of ACC.

RD3 1110 1111

Loads ACC with the contents of the display register location pointed to by the display register pointer.

ADM 1110 1011

Adds the contents of the display register pointed to by the display register pointer to the accumulator with carry.

SBM 1110 1000

Subtracts the contents of the display register pointed to by the display register pointer from the accumulator with borrow.

NOTES:

1. The alternation pattern of the display register pointer is Display Register A position 0, Display Register B position 0, Display Register A position 1, etc.
2. The upper two (four) gas discharge characters, 16-17 (16-19), can be addressed only by incrementing the internal display register pointer above 15 by a WRM or RDM instruction in 18 (20) character gas discharge mode. If the internal display register pointer has been incremented above 15, then these characters can be read or written by a RD3 or WMP instruction.
3. Successive WRM commands will shift the output data (see gas discharge display output format below) one character forward in relation to the reset pulse. This will cause a wraparound shift left on the self-scan display. Hence, starting at register 0 and loading the display RAM will give a right-justified display — MSD first.

	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
	RST	CLK	D_5	D_4	D_3	D_2	D_1	D_0
BLANK CODE:	X	X	1	0	0	0	0	0

Figure 1. Gas Discharge Display Output Format.

4. RDM will not cause any display shifting. The read order is MSD to LSD with the MSD stored in display register 0.

Scanned Sensor Mode

The instructions which are used in the scanned sensor mode are described below:

Mnemonic Instruction Code
SRC 0010 RRR1

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted for scanned sensor mode as follows:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 X X	$n_3n_2n_1X$	n_3-n_1 indicates an 8-bit sensor group to be read.

WR2 1110 0110

Clears the FIFO/RAM logic and the INT line.

RD1 1110 1110

Loads into ACC the upper 4 bits of the 8-bit sensor RAM group previously addressed by an SRC instruction.

RD2 1110 1110

Loads into ACC the lower 4 bits of the 8-bit sensor RAM group previously addressed by an SRC instruction.

NOTES:

1. In this mode, the 4269 PKD will continuously input the 64 matrix intersections of the sensor into the FIFO/Sensor RAM, which is organized as a 64-bit RAM.
2. The INT line will become active (V_{DD1}) and remain active whenever at least one intersection remains a logical one in the Sensor RAM.
3. The sensor group number set by the SRC is loaded into the internal display register pointer. Display mode instructions which change the internal display register pointer thus change the sensor group address.

Scanned Keyboard and Encoded Keyboard Modes

The instructions which are used in the scanned keyboard and encoded keyboard modes are described below:

Mnemonic Instruction Code
SRC 0010 RRR1

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted as follows for scanned and encoded keyboard modes:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 X X	X X X X	SRC used only to select 4269.

WR2 1110 0110

Clears FIFO/RAM logic, the status buffer, and the INT line.

RD1 1110 1101

Reads the first nibble of the current FIFO register position.

RD2 1110 1110

Reads the second nibble of the current FIFO register position. FIFO register position is incremented to the next position.

RD0 1110 1100

Loads ACC with the FIFO status.

NOTES:

1. The 4-bit FIFO status contains the number of valid characters (0-8) in the keyboard FIFO. However, in the event of an overrun, i.e., more than 8 characters entered, the 4-bit status will be set to a value of 15. The first eight characters entered prior to the overrun character will remain in the FIFO until cleared.
2. When a character is entered in the FIFO, the INT output pin will go to V_{DD1}. When a character is read, the INT will change from V_{DD1} to V_{SS} (open) and back to V_{DD1} until the FIFO has been emptied. If a ninth character is inputted to the PKD before one complete character has been removed, the overrun status will be set. This will cause the INT line to remain active (V_{DD1}) even after all characters have been accessed. Overrun status can only be cleared by a WR2 or WR3 command (although the first eight FIFO characters can be read). This condition allows the user to detect an overrun condition if it occurs between the time the status buffer is checked and the time all characters have been read. It should be noted that an RD2 must be initiated after an RD1 to advance to the next FIFO word even if the second nibble is not desired.
3. For a 16-key Keyboard, successive RD2 instructions will be adequate for inputting the key code.

DESIGN CONSIDERATIONS

Display Modes

General Remarks

Each Display A and Display B output is capable of driving one standard TTL load. This is done by using a V_{SS} = +5, V_{DD} = -10V and V_{DD1} = GND. The V_{DD1} pin allows the PKD to interface to a variety of commercially available display arrays via a specified circuit. Gas discharge, phosphorescent, LED, and incandescent displays can all be used with a 4269. The interface requirements are determined by the selected display device. Current into each of the Display A and Display B output lines should not exceed 1.6mA.

The two 16 x 4 Display Registers A and B provide information in hexadecimal positive logic conventions. Hence, a 0000, negative logic V_{SS} on the data bus, will be 0000 (positive logic V_{DD1}) at the A and B display output. (The above is equivalent to one level inversion between the data outputs of the PKD and the CPU accumulator.)

Individual, Scanned Display Mode

The digit selection is achieved by using the eight scan lines, S_0-S_7, and the display select line RS. The RS output is used to multiplex the eight scan strobes to give sixteen separate strobes for up to 16 digits of display. It should be noted that the LSD output position of both Display Registers A and B is gated out coincidently with S_0 time of the scan register. Following digit positions are also coincident. This feature allows an interface to 8 x 8 or 16 x 8 displays. For the first eight display digit positions, the RS output is at open drain. The remaining eight of the 16 digit positions are output sequentially with RS at V_{SS}. Sufficient active on-time (V_{SS}) is allowed at the scan strobe line (S_0-S_7) to illuminate the displayed digit. Sufficient time is also allowed between segments to extinguish segment and prevent overlapped illumination. If the 8 digit mode is selected with the WR1 instruction, the LSD will be gated out every S_0 time – not every other time.

Gas Discharge Modes (Self-Scan)

An approximate 100 μsec period, 50% duty cycle clock will be provided to the gas discharge display. A reset pulse – one clock period long – will be generated every 111th clock period for the 16/18 digit displays or every 139th clock period for 20 digit displays. Character periods are either seven clock periods long (for 16 or 20 character displays) or six clock periods long (for 18 character displays). For either case, character data is valid for the first five clock periods of the character period. Character 0 (left-most digit) starts upon the rising edge of the reset signal. The blank code is $A_1 = V_{SS}$ and A_0, B_3 - $B_0 = V_{DD1}$, with A_3 and A_2 providing reset and clock functions respectively. For the 18 character gas discharge display mode, the data outputs are blank for the 108th, 109th, and 110th clock periods.

For an aesthetic display transistor, the display register outputs can be placed into the blank mode (all outputs to V_{SS}) via an SRC during the loading of the display register. The outputs can then be unblanked via another SRC when the display register has been completely loaded.

Keyboard Modes

Scanned Sensor Mode

The sensor interface consists of two groups of eight lines, the scan strobe lines (S_0-S_7) and the return sense lines (R_0-R_7). Each scan strobe is used to enable eight return lines, giving 64 total sense strobes for each complete scan. When in the sensor mode, the two key rollover and debounce logic is inhibited. This allows multiple valid intersection connections to be inputted. The SHIFT and CONTROL inputs are ignored in this mode.

Each sensor intersection will have a RAM location reserved. The designer should group the sensors in common groups of 4. This mode is intended to be used to scan a matrix of electronic intersections or mechanical contacts. Debouncing is to be performed under software control. The INT line will remain active (V_{DD1}) whenever a valid intersection has been detected. The scan strobe cycle is the same pattern of a logical 1 (V_{SS}) shifted in a field of zeros.

The sense return lines are read out by RD1/RD2 instructions as shown in Figure 2.

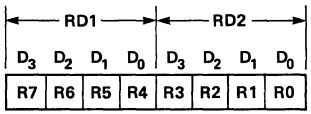


Figure 2. Sense Return.

Scanned Keyboard Mode

a. Key Depression Detection

These conditions can occur during the keyboard interrogation by the PKD (see timing diagram below).

1. Simultaneous Key Depression

   Two or more keys depressed within one complete single depression scan (approximately 11ms) is defined as a simultaneous key depression. If this condition occurs, the PKD continues to scan the keyboard and waits until one key remains depressed. It then treats the remaining key as a single key depression, as described below.

2. Single Key Depression

   When any single key (non-simultaneous) is depressed, an internal counter is started. The key code is also stored internally in a PKD temporary register with a code given by the values of the Scan and Return Lines. The PKD will then make four more complete scans of all keys. If no other keys are depressed during the fourth complete scan and the original key detected is still depressed at the end of the fourth scan, the key code is defined as a single key depression. The key code is then entered into the FIFO along with the value of the SHIFT and Control (S/C) input signals. If eight characters are already in the FIFO, the character will not be entered and the overrun will be set. When a character is entered in the FIFO, the INT line is activated to a logical "1" (V_{DD1}). If on the fourth complete scan the original key depressed is no longer depressed, the key is ignored as if it had never been depressed. This delay of four scan times, or approximately 11ms, thus provides the debounce function for the keyboard.

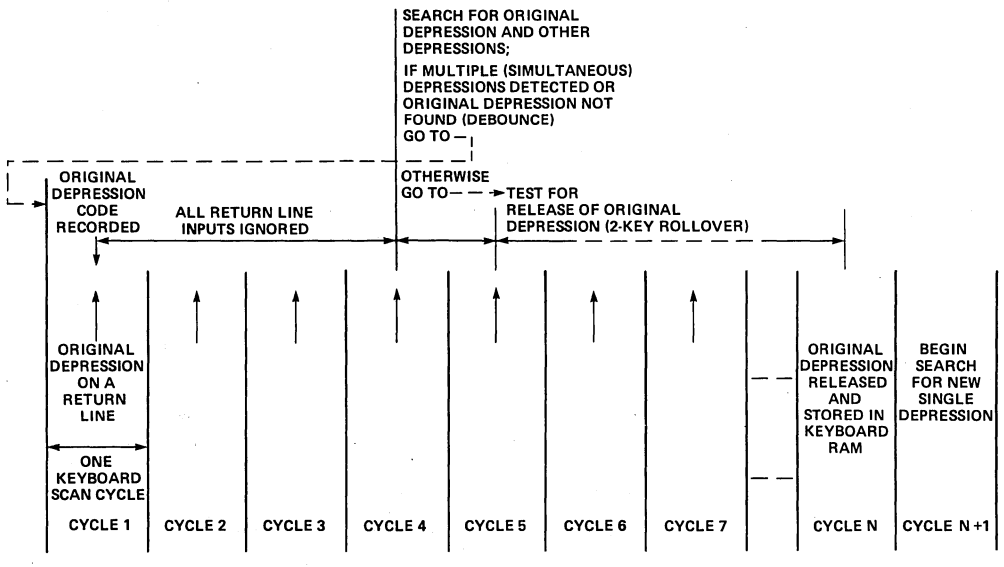


Figure 3. Keyboard Debounce and 2-Key Rollover Timing.

3. Two Key Rollover

   The two key rollover operates as follows:

   If a second key is depressed after a first key has been accepted by the PKD as a single key depression but the first key has not been released, then the second key will be treated as a new original depression after the first key has been released.

   If a second key is depressed after a first key has been accepted by the PKD as a single key depression and the second key is released before the first key is released, the second key will be ignored.

b. Key Matrix Encoding

   The keyboard matrix hardware configuration and associated matrix encoding is shown in Figures 4, 5, and 6.

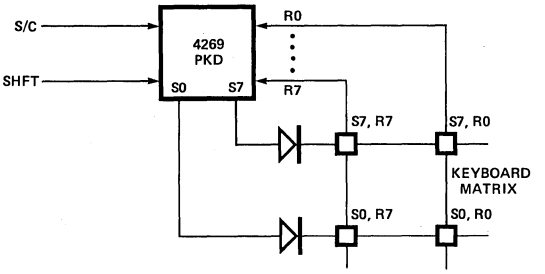


Figure 4. Hardware Configuration.

		R_0 000	R_1 001	R_2 010	R_3 011	R_4 100	R_5 101	R_6 110	R_7 111	SHIFT	S/C
S_0	000	0	1	2	3	4	5	6	7	X	X
S_1	001	8	9	10	11	12	13	14	15	X	X
S_2	010	16	17	18	19	20	21	22	23	X	X
S_3	011	24	25	26	27	28	29	30	31	X	X
S_4	100	32	33	34	35	36	37	38	39	X	X
S_5	101	40	41	42	43	44	45	46	47	X	X
S_6	110	48	49	50	51	52	53	54	55	X	X
S_7	111	56	57	58	59	60	61	62	63	X	X

Figure 5. Matrix Configuration.

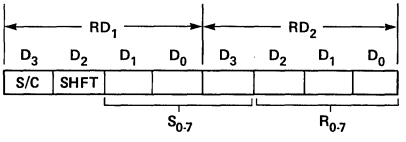


Figure 6. Key Encoding.

c. Expansion to 128 Key Scan

The basic mechanism of the PKD for scanning a 64 key matrix can be expanded to interface to a 128 key matrix. Note that the CONTROL (S/C) and SHIFT inputs cannot be used to directly encode 256 keys since the single key depression logic operates with the 6-bit matrix position code only. However, if full debounce and 2 key roll over control between two 64 key matrices is not necessary, then a configuration such as shown in Figure 7 may be used to add a seventh bit to the 6-bit matrix via the SHIFT or S/C input of the PKD. Alternately, two 4269 PKDs can be used for interfacing to the 128 keys.

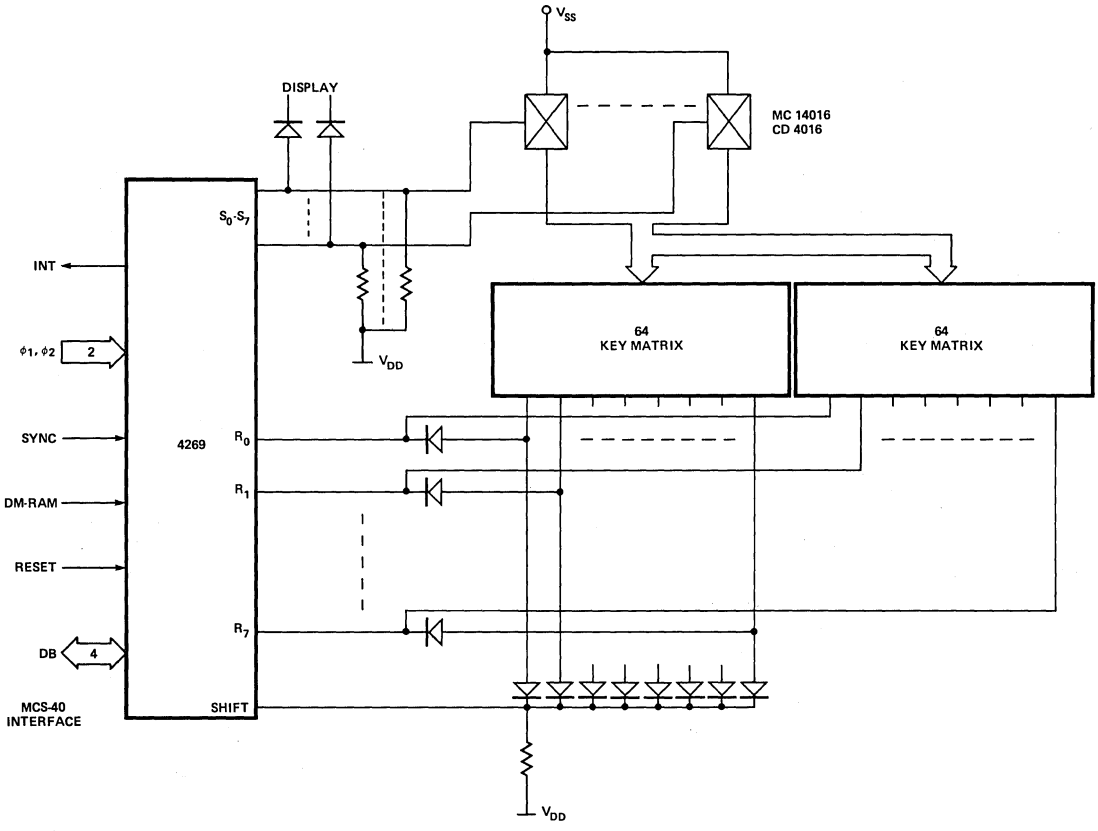


Figure 7. 128 Scanned Input Keys.

Encoded Keyboard Mode

Data Format

In the encoded keyboard mode, the eight return lines are directly loaded into the PKD's keyboard FIFO. For encoded keyboards using less than eight encoded bits, the remaining bits can be any desired signal, such as a multiplex signal between two keyboards or a special key flag.

HARDWARE DESCRIPTION

The following is a description of the major hardware elements of the 4269. Refer to the hardware block diagram shown in Figure 8.

MCS-40 Data Bus/Control Line Interface

The 4269 PKD resides on the MCS-40 data and timing bus. As such it derives its basic timing from the ϕ_1 and ϕ_2 clock signals. Synchronization and chip select information are provided by the SYNC and CM-RAM lines respectively. The Data Bus provides the 4269 with control commands and routes Keyboard/Display data between the 4269 and CPU Accumulator.

Display Registers

The 4269 is provided with RAM storage which is utilized to implement an automatically refreshed display. The display RAM (Display Registers A and B) can be configured in several different organizations under program control, including two 16 x 4 hexadecimal displays, one 32 x 4 hexadecimal display, a single 8 or 16 alphanumeric display, a single 16, 18, or 20 character gas discharge alphanumeric display, or a 128 matrix array of indicators. The display RAM output is available on A_0-A_3 for Display Register A outputs and B_0-B_3 lines for Display Register B outputs. The V_{DD1} line provides a separate negative supply reference for the A and B outputs (and INT).

S/R Counters and Debounce Logic

The S/R counters are two modulo 8 counters used to provide a unique 6-bit code for each of the 64 intersections provided by a matrix of eight Scan (S) Driver and eight Return (R) sense lines. The R counter is counted eight times for each S count. When keys, contacts, or controls are arranged in the matrix, each matrix intersection is examined for closure between the corresponding S and R line. If the 4269 is in the Scanned Keyboard Mode, an approximate 11 msec debounce time will be used to ascertain the validity of the connection. The valid 6-bit code, along with the SHIFT and S/C (control) line, is placed in the FIFO for retrieval by the CPU.

Scan Counter and Scan F/F

For each increment of the modulo 8 S counter, the Scan Counter is advanced. The register shifts a logical 1 (V_{SS}) in a field of logical zeros (open drain). The non-overlapping one is successively moved from S_0 through S_7 and around again. For each complete sequence of shifts, the scan flip-flop is toggled. This flip-flop's initial value, after RESET, is open drain.

Key Return Multiplexer

The return multiplexer selects one of the 8 return lines coming from the key array. The selection code is provided by the modulo 8 R counter. When in the Scanned Sensor Mode, all 8 R lines are entered for each scan line, and pass directly to the Sensor RAM (FIFO).

FIFO and Sensor RAM

This block is a dual function RAM of 64 bits. The RAM can serve as a keyboard character FIFO for eight 8-bit characters or as a sensor RAM to store the status of 64 intersections.

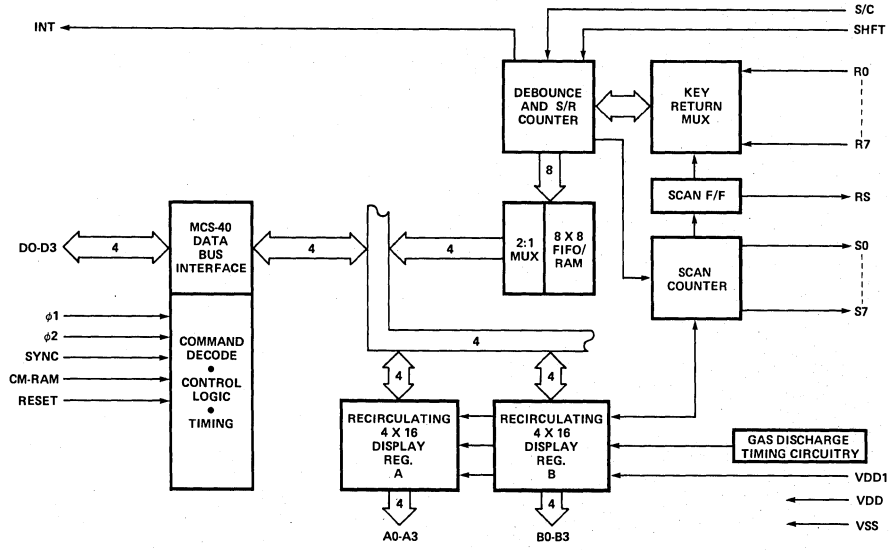


Figure 8. 4269 Hardware Block Diagram.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0° to 70°C; V_{SS} -V_{DD}= 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400nsec; $t_{\phi D2}$ = 150nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

Symbol	Parameter	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
I_{OL}	Data Bus Sinking Current	8	15		mA	V_{OUT} = V_{SS}
I_{OL}	A_{0-3}/B_{0-3} Sinking Current		2.5		mA	V_{DD1} = V_{SS} -5V, V_{OUT} = V_{DD1} + .4V
I_{OL}	Interrupt Sinking Current		150		μA	V_{OUT} = V_{DD1} +.5V
R_{OH}	Data Bus Output Resistance		150	250	Ω	V_{OUT} = V_{SS} -.5V
R_{OH}	A_{0-3}/B_{0-3} Output Resistance		4		kΩ	V_{OUT} = V_{SS} -2.6V
R_{OH}	S_{0-7} Output Resistance		250		Ω	V_{OUT} = V_{SS} -1V
R_{OH}	RS Output Resistance		350		Ω	V_{OUT} = V_{SS} -1V

A.C. Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%.

Symbol	Parameter	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
t_{CY}	Clock Period	1.3		2	μsec	
$t_{\phi R}$	Clock Rise Time			50	nsec	
$t_{\phi F}$	Clock Fall Time			50	nsec	
$t_{\phi PW}$	Clock Width	380		480	nsec	
$t_{\phi D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	nsec	
$t_{\phi D2}$	Clock Delay ϕ_2 to ϕ_1	150			nsec	
t_W	Data-In, CM, SYNC Write Time	350	100		nsec	
t_H[1,2]	Data-In, CM, SYNC Hold Time	40	20		nsec	
t_{OS}[3]	Set Time (Reference)	0			nsec	
t_{ACC}	Data Bus Access Time			930	nsec	
t_{OH}	Data Bus Hold Time	50			nsec	
t_{RTSK}	Return Line Pull-Down Time		5		μs	C = 100pF; Scanned Keyboard Mode
t_{RTSN}	Return Line Pull-Down Time		30		μs	C = 100pF; Sensor Mode

Capacitance

Symbol	Parameter	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
C_ϕ	Clock Capacitance		8		pF	V_{IN} = V_{SS}
C_{DB}	Data Bus Capacitance		14	20	pF	V_{IN} = V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN} = V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN} = V_{SS}

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. All MCS-40 components which may transmit instruction on data to a 4004 or 4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
3. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} in the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

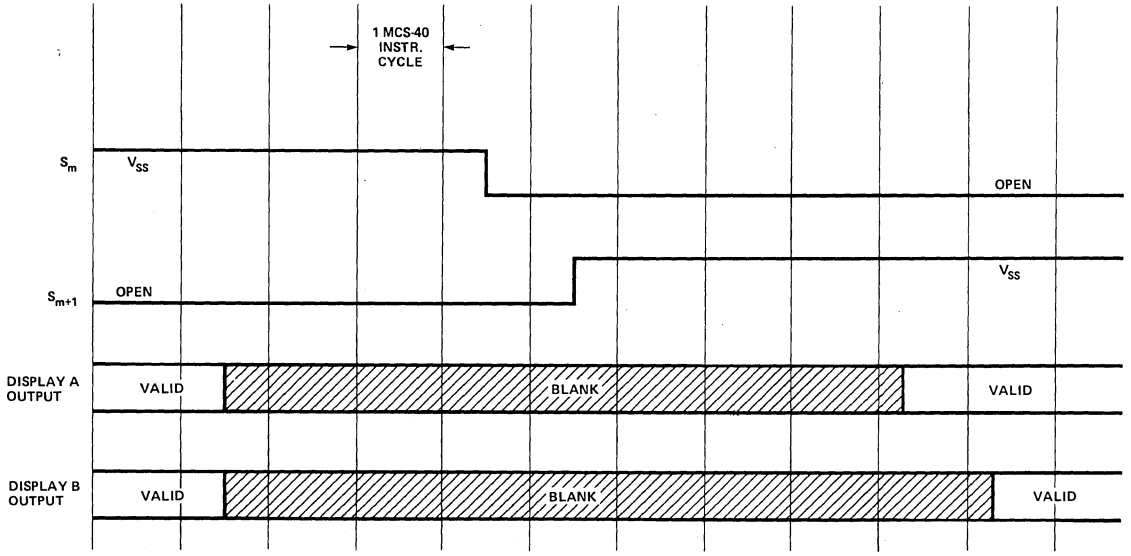


Figure 11. Data Blanking Detail - Individual Display Mode.

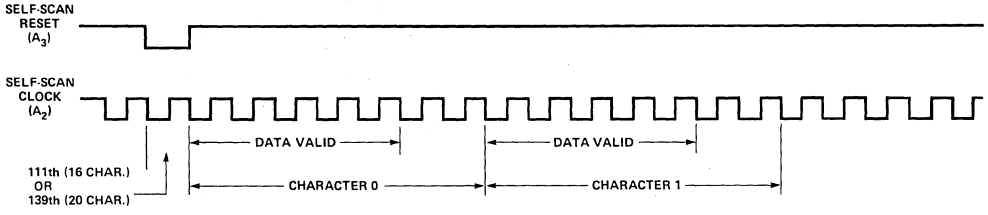


Figure 12. Gas Discharge (Self-Scan) Mode Timing - 16 or 20 Character Mode.

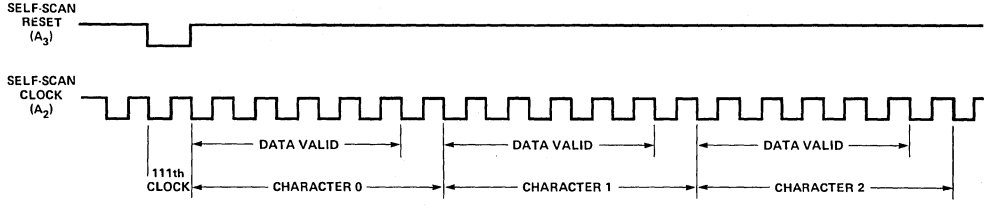


Figure 13. Gas Discharge (Self-Scan) Mode Timing - 18 Character Mode.

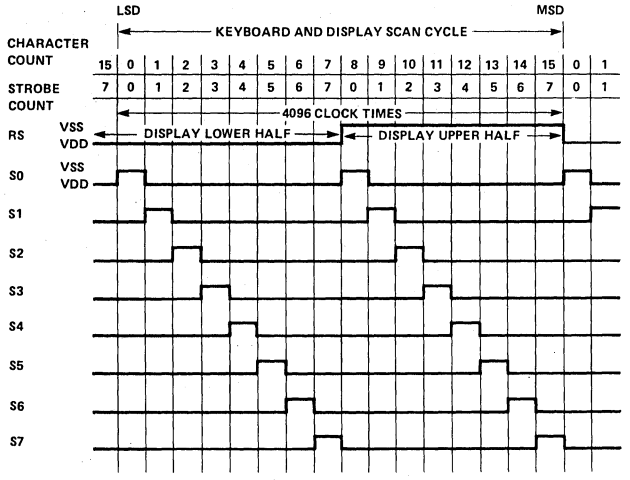


Figure 9. Individually Scanned Display Mode Timing.

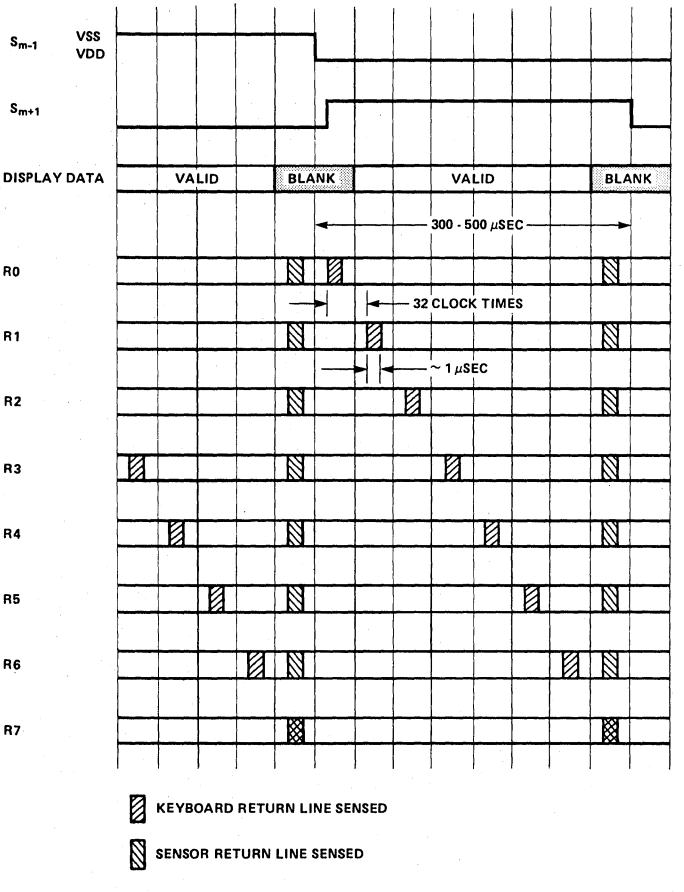


Figure 10. Detailed Timing of Strobe and Return Lines for Keyboard, Sensor, and Individual Scanned Display Modes.

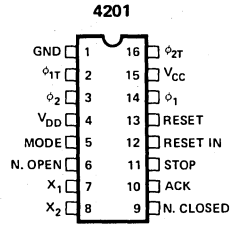
4201
CLOCK GENERATOR

- **Complete Clock Requirements for MCS-40™ Systems**
- **Crystal Controlled Oscillator (XTAL External)**
- **MOS and TTL Level Clock Outputs**
- **Provides MCS-40 Reset Function Signal**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available with -40° to +85° C Operating Range**

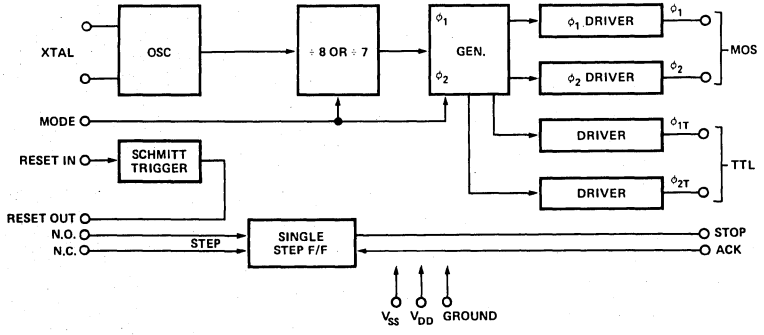
The 4201 is a CMOS integrated circuit designed to fill the clock requirements of the MCS-40 microcomputer family. The 4201 contains a crystal controlled oscillator (XTAL external), clock generation circuitry, and both MOS and TTL level clock driver circuits.

The 4201 also performs the power on reset function required by MCS-40 components and provides the logic necessary to implement the single-step function of the 4040 central processor unit.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation	Description of Function
1	GND	Circuit ground potential. This pin can be left floating for low power application. MOS clock output will be operative, TTL clock outputs will not.
2	ϕ1T	Phase 1 TTL level clock output. Positive true.
3	ϕ2	Phase 2 MOS level clock output. Directly drives all MCS-40 components.
4	V_{DD}	Main Power Supply Pin. $V_{DD} = V_{CC}$ -15V ±5%.
5	MODE	Counter mode control pin. Determines whether counter divides basic frequency by 8 or 7. Mode 1 = $V_{CC} \Rightarrow \div 7$ Mode 2 = $V_{DD} \Rightarrow \div 8$
6	N. OPEN	Input of single step circuitry to which normally open contact of SPDT switch is connected.
7	X1	External Crystal Connection. This pin may be driven by an external frequency source. X2 should be left unconnected.
8	X2	External Crystal Connection.
9	N. CLOSED	Input of single step circuitry to which normally closed contact of SPDT switch is connected.
10	ACK	Acknowledge input to single step circuitry normally connected to stop acknowledge output of 4040.
11	STOP	Stop output of singlc step circuitry normally connected to stop input of 4040. A SPDT toggle switch may be inserted in this line for RUN/HALT control.
12	RESET IN	Input to which RC network is connected to provide power-on reset timing.
13	RESET	Reset signal output which directly connects to all MCS-40 reset inputs. This signal is active low.
14	ϕ1	Phase 1 MOS level clock output. Directly drives all MCS-40 clock inputs.
15	V_{CC}	Circuit reference potential – most positive supply voltage.
16	ϕ2T	Phase 2 TTL level clock output. Positive true.

Functional Description

The 4201 consists of the following functional blocks:

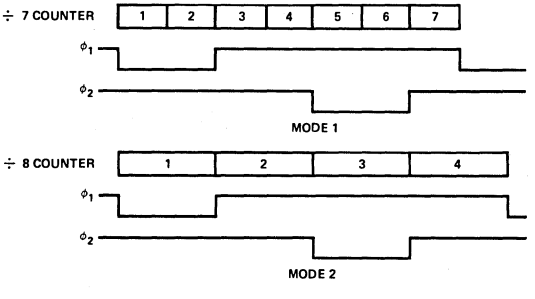
CRYSTAL OSCILLATOR

The oscillator is a simple series mode crystal-type circuit consisting of two inverters biased in the active region, and a series crystal element.

PROGRAMMABLE SHIFT REGISTER

The shift register in the 4201 divides the master clock and generates the proper states for generating the desired two-phase clock. The circuit is a seven bit dynamic device which circulates a logical "1" through a field of zeroes. The output of the various states are then combined to provide the proper clock waveforms. This provides a divide by 7 function.

In order to maintain the proper clock timing over the full operating frequency range of the MCS-40™ system, the shift register is programmable (using mode pin) as either a 7 bit or 4 bit device. When in the 4 bit mode the clock is divided by 2 and then by 4 to provide a divide by 8 function. The relationship between the phases is equal; that is, ϕ_1 pulse width, ϕ_2 pulse width, ϕ_1 to ϕ_2 and ϕ_2 to ϕ_1 times are all equal.



4201 Shift Register Modes.

PHASE DECODER

A simple gate complex is used to decode the shift register outputs to provide phase 1 and phase 2 clock waveforms. This circuitry is controlled by the mode input to achieve the two sets of timing discussed in the previous section.

OUTPUT BUFFERS

There are two sets of output buffers for the 2 phase clock. One set is the MOS level drivers designed to directly drive a full complement of MSC-40 components. The second set provides TTL compatible outputs which can drive one standard TTL load.

RESET CIRCUIT

The reset circuit is simply a level detector and driver stage. An external RC network connected between V_{DD} and V_{SS} at the reset input pin of the 4201 provides the required power-on delay.

To generate a reset, the V_{DD} supply must reach its full voltage level before the V_{SS} supply turns on.

SINGLE STEP CONTROL

The 4201 contains the necessary circuitry for allowing the 4040 CPU to execute instructions one at a time. Using the stop input and stop acknowledge output of the 4040, the 4201 generates a pulse that allows the 4040 to perform only one instruction. The stop command can be provided by a SPDT pushbutton directly since debouncing is provided by the 4201. A SPST toggle switch, in series with the $\overline{\text{STOP}}$ line, provides the Run/Halt feature.

Absolute Maximum Ratings*

Storage Temperature ..... -55°C to 150°C Ambient
Operating Temperature ..... 0°C to 70°C Ambient
Maximum Positive Voltage ..... V_{CC} +.5V
Maximum Negative Voltage ..... V_{DD} -.3V
Maximum Power Dissipation 1.0W
Maximum Supply Voltage V_{CC} -V_{DD} ..... 17V[1]
Maximum Supply Voltage V_{CC} -V_{DD} ..... 17V[2]

Notes: 1. C_{LOAD}, ϕ_1 and ϕ_2 ≥100pF.
2. C_{LOAD}, ϕ_1 and ϕ_2 = 0; R = 68Ω, V_{DD} Pin to V_{DD}; Bypass Capacitor at V_{DD} Pin.

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to 70°C; V_{CC}-V_{DD} = 15V ±5%; GND = V_{CC} -5V ±5%.

Symbol	Parameter	Limit		Units	Conditions
		Min.	Max.		
I_{LI}	Input Leakage Current		10	μA	V_{IL} = V_{DD} All inputs except X_1, X_2, N. Open, N. Closed
V_{IH}	Input High Voltage	V_{CC}-1.5	V_{CC}+.5	V	All inputs except X_1, X_2, Reset
V_{IL}	Input Low Voltage	V_{DD}	V_{CC}-13	V	All inputs except X_1, X_2, Reset
V_{OL}	Output Low Voltage	V_{DD}	V_{CC}-13.4	V	Capacitance load only
V_{OH}	Output High Voltage	V_{CC}-1.5	V_{CC}	V	Capacitance load only
V_{OL}	ϕ_{1T}, ϕ_{2T}		GND+.5	V	I_{OL} = 1.6mA
V_{OH}	ϕ_{1T}, ϕ_{2T}	V_{CC}-.75		V	I_{OH} = -400μA
I_{OL}	ϕ_1, ϕ_2 Sink Current	400		mA	V_{OUT} = V_{CC}; Pulse Width ≤1μsec
I_{OL}	ϕ_{1T}, ϕ_{2T} Sink Current	15		mA	V_{OUT} = V_{CC}
I_{OL}	Reset Sink Current	6		mA	V_{OUT} = V_{CC}
I_{OL}	Stop Sink Current	1		mA	V_{OUT} = V_{CC}
I_{OH}	ϕ_1, ϕ_2 Source Current	180		mA	V_{OUT} = V_{DD}
I_{OH}	ϕ_{1T}, ϕ_{2T} Source Current	8		mA	V_{OUT} = V_{DD}
I_{OH}	Reset Source Current	6		mA	V_{OUT} = V_{DD}
I_{OH}	Stop Source Current	1		mA	V_{OUT} = V_{DD}
I_{DD}	Average Supply Current		20	mA	5.185MHz Crystal, C_{LOAD} ϕ_1 and ϕ_2 = 20pF
V_{IL}	Reset Input Low Voltage	V_{DD}	V_{CC}-11	V	
V_{IH}	Reset Input High Voltage	V_{CC}-6.5	V_{CC}+.5	V	
R_1	Pull Up Resistance on N. Open, N. Closed	20	120	KΩ	V_{IN} = V_{DD}

Capacitance

f = 1MHz; T_A = 25°C

Symbol	Parameter	Limit		Units	Conditions
		Min.	Max.		
C_{IN}	Input Capacitance		5	pF	All Inputs except X_1, X_2
C_{OUT}	ϕ_1, ϕ_2 Output Capacitance		40	pF	
C_{OUT}	ϕ_{1T}, ϕ_{2T} Output Capacitance		10	pF	
C_{OUT}	Stop Reset Output Capacitance		5	pF	

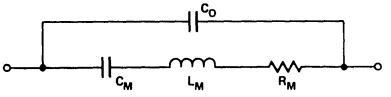
XTAL Specifications

Range: 3.5 - 5.185 MHz

Mode: Series or Parallel Resonant

Recommended: Crystek 5.185 MHz
Spec. No. CY8A or CTS
Knights 4201-5.185 or Equivalent

CTS Knights
XTAL Equivalent Circuit



$C_O \approx$ 3-5pF
$C_M \approx$ 10fF
$R_M \approx 50\Omega$
$L_M \approx \frac{1}{(2\pi f)^2 C_M}$

XTAL Capacitance Requirements: 20-30 pF

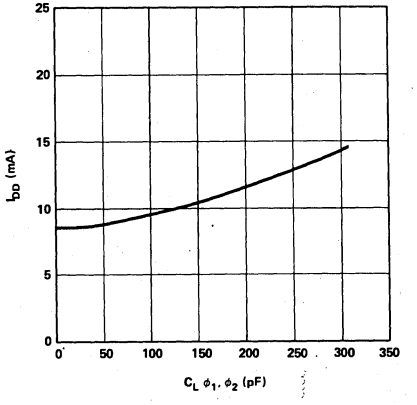
A.C. Characteristics $T_A = 0°C$ to $70°C$; $V_{CC} - V_{DD} = 15V \pm 5\%$; $G = V_{CC} - 5V \pm 5\%$

Symbol	Parameter	Limit			Units	Conditions
		Min.	Typ.	Max.		
t_{CY}	Clock Period		$t_{XTAL}*7$		ns	Mode = V_{CC}
$t_{\phi PW}$	Clock Pulse Width	$(2/7)t_{CY}-10$	$(2/7)t_{CY}$	$(2/7)t_{CY}+10$	ns	
$t_{\phi D1}$	Clock Delay from ϕ_1 to ϕ_2	$(2/7)t_{CY}-10$	$(2/7)t_{CY}$	$(2/7)t_{CY}+10$	ns	
$t_{\phi D2}$	Clock Delay from ϕ_2 to ϕ_1	$(1/7)t_{CY}-10$	$(1/7)t_{CY}$	$(1/7)t_{CY}+10$	ns	
t_{CY}	Clock Period		$t_{XTAL}*8$		ns	Mode = V_{DD}
$t_{\phi PW}$	Clock Pulse Width	$(1/4)t_{CY}-10$	$(1/4)t_{CY}$	$(1/4)t_{CY}+10$	ns	
$t_{\phi D1}$	Clock Delay from ϕ_1 to ϕ_2	$(1/4)t_{CY}-10$	$(1/4)t_{CY}$	$(1/4)t_{CY}+10$	ns	
$t_{\phi D2}$	Clock Delay from ϕ_2 to ϕ_1	$(1/4)t_{CY}-10$	$(1/4)t_{CY}$	$(1/4)t_{CY}+10$	ns	
$t_{\phi D3}$	TTL Clk to MOS Clk Skew[1]	0		40	ns	
$t_{\phi r}, t_{\phi f}$	Clock Rise and Fall Time			50	ns	C_L=300pF=ϕ_1, ϕ_2; C_L=50pF on ϕ_{1T}, ϕ_{2T}
t_D	Delay from Acknowledge to Stop			1	μs	C_L=20pF

Note: 1. See waveforms section for phase relationships between ϕ_1, $\phi_1 T$, ϕ_2, and $\phi_2 T$.
2. Proper system operation of all members of the MCS-40™ component family is guaranteed with the 4201 Clock Generator at 1.35 μsec $\leq t_{CY} \leq$ 2 μsec.

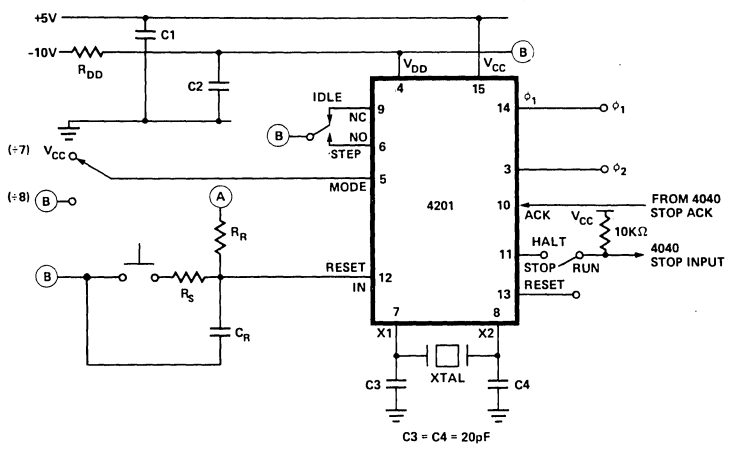
Typical Characteristics

I_{DD} CURRENT VS. LOAD CAPACITANCE



MCS-40

CLOCK GENERATOR IMPLEMENTATION



Power Supply Voltages

The purpose of R_{DD} is both to limit ϕ_1 and ϕ_2 rise times and to drop V_{DD} at the 4201 pin. Values for R_{DD} as a function of ϕ_1, ϕ_2 load capacitance are:

For C_{LOAD} <50pF; use R_{DD} = 100Ω.
For 50pF <C_{LOAD} <100pF; use R_{DD} = 68Ω.
For 100pF <C_{LOAD} <300pF; use R_{DD} = 27Ω.
For C_{LOAD} >300pF; use R_{DD} = 10Ω.

All 4201 functions requiring the V_{DD} voltage should use the pin V_{DD} or node Ⓑ on the 4201 side of resistor R_{DD}.

Operation is guaranteed with V_{CC}-V_{DD} = 15V ±5%. During system power-up or during power supply glitching, the maximum magnitude of (V_{CC}-V_{DD}) must be limited to 17 volts.

With V_{CC} = +5V, V_{DD} = -10V, bypass capacitor C1 of 1 μF and C2 of .1 μF in parallel from V_{CC} to GND and V_{DD} to GND provide excellent bypassing.

Single-Supply Systems (+15V or -15V)

Recommended 4201 circuit modifications for single supply systems are:

1. The 1 μF capacitor C1 should be between V_{DD} and V_{CC}.
2. Other capacitors shown as being grounded should be connected to V_{CC}.
3. Reset R – C should be connected to V_{CC}.
4. The current limiting resistor R_{DD} is still needed in the V_{DD} line.

Crystals

Either ÷7 or ÷8 Modes may be used. Mode equals V_{CC} for ÷7, Mode equals V_{DD} for ÷8. The XTAL range should be between 500 kHz (4 MHz XTAL, ÷8 MODE) and 740 kHz (5.185 MHz XTAL, ÷7 MODE). These XTAL may be found as standard products from CTS Knights or Crystek.

The XTAL terminals, X1 and X2, should each be tied to 20pF capacitors C3 and C4 to GND. Exact values of C3 and C4 should be selected such that total capacitance values seen at X_1 and X_2 inputs, including lead and board capacitance, are 20 - 30pF allowing proper oscillation start up following a Reset.

Reset Network

The Reset input has V_{IL} = V_{CC} -11 Volts and V_{IH} = V_{CC} -6.5 Volts, with about 1 Volt of hysteresis (Schmitt circuit).

Node Ⓐ must be tied to GND or V_{CC} = +5V; and R_R and C_R selected, such that the negative V_{DD} transition moves the Reset input below V_{IL}.

Tying node Ⓐ to GND and making C_R very large, i.e. >1μF, will allow the greatest freedom in V_{CC} and V_{DD} rise times during turn-on. Tying node Ⓐ to GND will also cause Reset after a V_{DD} glitch to GND.

The purpose of R_S at 510Ω or 1kΩ, is to limit Reset input fall time on manual Reset, so that the Reset input does not fall below V_{DD}.

TTL Clock Outputs

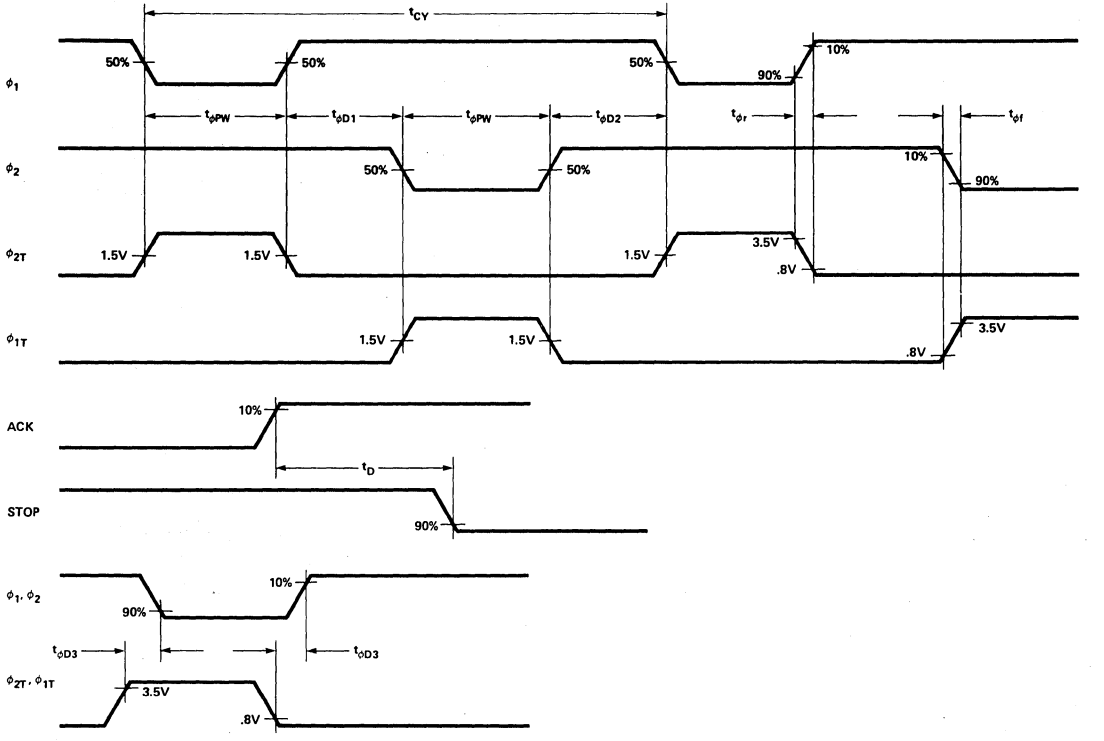
If ϕ_{1T} and ϕ_{2T} are used, GND pin should be tied to logic ground. ϕ_{1T} and ϕ_{2T} levels will be equal to V_{CC} and the GND pin level.

Unused Functions

If any of the 4201 functions listed below are not used, it is recommended that the pins be connected as described below:

1. ϕ_{1T}, ϕ_{2T} – Tie GND, ϕ_{1T}, ϕ_{2T} to V_{CC}.
2. Single Step – Tie NO to V_{CC}
   NC to Node Ⓑ (V_{DD} pin of 4201)
   STOP ACK to V_{CC}
   STOP left open
3. Reset – Tie RESET IN to V_{CC}
   RESET OUT to V_{CC}

Waveforms

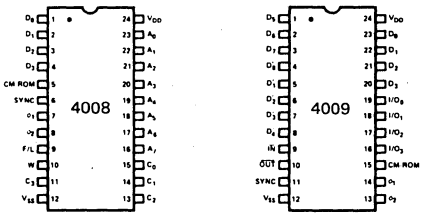

t_{CY}
ϕ_1
50%
$t_{\phi PW}$
$t_{\phi D1}$
$t_{\phi PW}$
$t_{\phi D2}$
$t_{\phi r}$
$t_{\phi f}$
10%
90%
ϕ_2
ϕ_{2T}
1.5V
3.5V
.8V
ϕ_{1T}
ACK
t_D
STOP
ϕ_1, ϕ_2
$t_{\phi D3}$
ϕ_{2T}, ϕ_{1T}

STANDARD MEMORY AND I/O INTERFACE SET

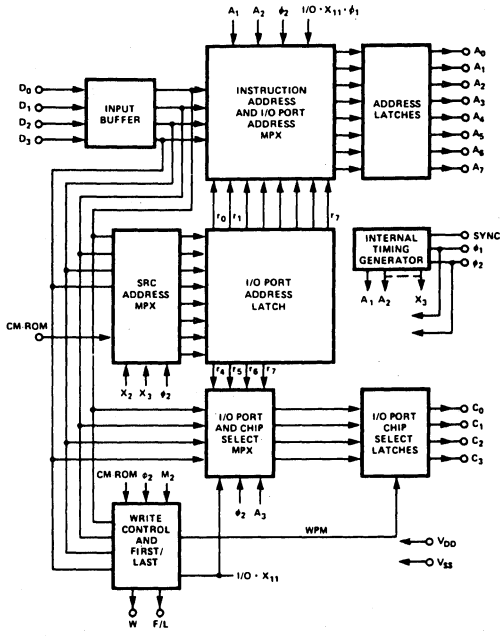
- **Direct Interface to Standard Memories**
- **Allows Write Program Memory**
- **24 Pin Dual In-Line Packages**
- **Standard Operating Temperature Range of 0° to 70 °C**

The standard memory and I/O interface set (4008/4009) provides the complete control functions performed by the 4001 or 4308 in MCS-40™ systems. The 4008/4009 are completely compatible with other members of the MCS-40 family. All activity is still under control of the CPU. One set of 4008/4009 and several TTL decoders is sufficient to interface to 4K words of program memory, sixteen four-bit input ports and sixteen four-bit output ports.

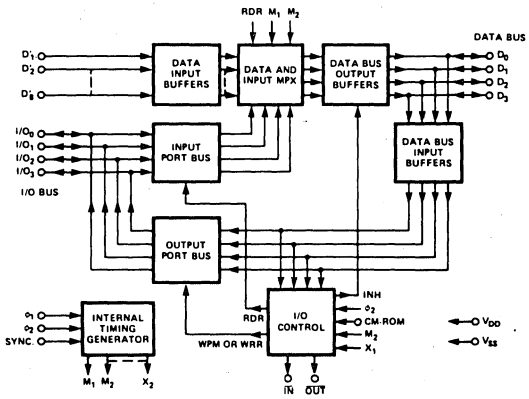
PIN CONFIGURATIONS



4008 BLOCK DIAGRAM



4009 BLOCK DIAGRAM



MCS-40

Pin Description

4008

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
7-8	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
6	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
5	CM-ROM/Neg.	Command input driven by CM-ROM output of processor. Used for decoding SRC and I/O instructions.
23-16	A_0-A_7/Pos.	Address output buffers. The demultiplexed address values generated by the 4289 from the address data supplied by the processor at A_1 and A_2.
15-13, 11	C_0-C_3/Pos.	Chip select output buffers. The address data generated by the processor at A_3, or during an SRC are transferred here.
9	F/L/Neg.	Output signal generated by the 4008 to indicate which half-byte of PROGRAM MEMORY is to be operated on.
10	W/Pos.	Output signal, active low, generated by the 4008 when the processor executes a WPM instruction.
12	V_{SS}	Most positive supply voltage.
24	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.

4009

Pin No.	Designation/ Type of Logic	Description of Function
23-20	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
5-8, 1-4	D'_1-D'_8/Pos.	The eight bits of instruction from the program memory are transferred on these 4009 pins (most significant bit is D_8).
14-13	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
11	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
15	CM-ROM/Neg.	Command input driven by CM-ROM output of Processor.
9	IN/Neg.	Output signal, active low, generated by the 4289 when the processor executes an RDR instruction.
10	OUT/Neg.	Output signal, active low (V_{DD}), generated by the 4009 when the processor executes a WRR instruction.
19-16	I/O_0-I/O_3/Pos.	Bidirectional I/O data bus. Data to and from I/O ports or data to write PROGRAM MEMORY are transferred via these pins.
23	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.
12	V_{SS}	Most positive supply voltage.

Functional Description

The 4008 is the address latch chip which interfaces the 4004 or 4040 to standard PROMs, ROMs and RAMs used for program memory. The 4008 latches the low order eight bits of the program address sent out by the CPU during A1 and A2 time. During A3 time it latches the high order four bits of the program address from the CPU. The low-order eight bits of the program address are then presented at pins A0 through A7 and the high-order four bit (also referred to as page number) are presented at pins C0 through C3. These four bits must be decoded externally and one page of program memory is selected.

The 4009 then transfers the eight bit instruction from program memory to the CPU four bits at a time at M1 and M2. The command signal sent by the CPU activates the 4009 and initiates this transfer.

When the CPU executes an SRC (Send Register Control) instruction, the 4008 responds by storing the I/O address in its eight bit SRC register. The content of this SRC register is always transferred to the address lines (A0 through A7) and the chip select lines (C0 through C3) at X1 time. The appropriate I/O port is then selected by decoding the chip select lines. The IN and OUT lines of the 4009 indicate whether an input or output operation will occur.

The 4009 is primarily an instruction and I/O transfer device. When the CPU executes an RDR (Read ROM Port) instruction, the 4009 will send an input strobe (pin 9) to enable the selected input port. It also enables I/O input buffers to transfer the input data from the I/O bus to the data bus. When the 4009 interprets a WRR (Write ROM Port) instruction, it transfers output data from the CPU to the I/O bus and sends an output strobe (pin 10) to enable the selected output port.

The WPM (Write Program Memory) instruction is used in conjunction with the 4008/4009 to write data into the RAM program memory. When an instruction is to be stored in RAM program memory, it is written in two four-bit segments. The F/L signal from the 4008 keeps track of which half is being written. When the CPU executes a WPM instruction, the chip select lines of the 4008 are jammed with "1111". In the system design this should be designated as the RAM channel. The W line on the 4008 is also activated by the WPM instruction. The previously selected SRC address on line A0 through A7 of the 4008 becomes the address of the RAM word being written. By appropriately decoding the chip select lines, the W line, and F/L, the write strobes can be generated for the memory.

The F/L line is initially high (V_{SS}) when power comes on. It then pulses low (V_{DD}) when every second WPM is executed. A high (V_{SS}) on the F/L lines means that the first four bits (OPR) are being written, and a low means that the last four bits (OPA) are being written. The 4009 transfers the segment of the instruction to the I/O bus at X2 of the WPM instruction. The SRC address sent to RAM is only 8 bits. When more than one page of RAM (256 bytes) is being written, an output port must be used to supply additional address lines for higher order addresses.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

$T_A = 0°C$ to $70°C$; $V_{SS} - V_{DD} = 15V \pm 5\%$; $t_{\phi PW} = t_{\phi D1} = 400$ nsec; $t_{\phi D2} = 150$ nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current (4008 only)		10	20	mA	$T_A = 25°C$
I_{DD}	Average Supply Current (4009 only)		13	30	mA	$T_A = 25°C$
INPUT CHARACTERISTICS—ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	μA	$V_{IL} = V_{DD}$
V_{IH}	Input High Voltage (Except Clocks)	$V_{SS}-1.5$		$V_{SS}+.3$	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		$V_{SS}-5.5$	V	
V_{IHC}	Input High Voltage Clocks	$V_{SS}-1.5$		$V_{SS}+.3$	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		$V_{SS}-13.4$	V	
OUTPUT CHARACTERISTICS—ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	$V_{OUT} = -12V$
V_{OH}	Output High Voltage	$V_{SS}-.5V$	V_{SS}		V	Capacitance Load
I_{OL}	Data Lines Sinking Current	8	15		mA	$V_{OUT} = V_{SS}$
I_{OL}[1]	Address Line Sinking Current (4008 only)	7	13		mA	$V_{OUT} = V_{SS}$
I_{OL}	In, Out, F/L, Chip Select	1.6	4		mA	$V_{OUT} = V_{SS} -4.85$
I_{OL}[2]	W Output, Sinking Current (4008 only)	2.5	5		mA	$V_{OUT} = V_{SS}$
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	$V_{SS}-12$		$V_{SS}-6.5$	V	$I_{OL} = 0.5mA$
R_{OH}	Output Resistance, Data Line "0" Level (4008 only)		150	250	Ω	$V_{OUT} = V_{SS} -.5V$
R_{OH}	Address, Chip Select Output Resistance, "0" Level (4008 only)		.6	1.2	kΩ	$V_{OUT} = V_{SS} -.5V$
R_{OH}	Output Resistance, Data Line "0" Level (4009 only)		130	250	Ω	$V_{OUT} = V_{SS} -2V$
I_{CF}[3]	Address, C/S Output "1" Clamp Current (4008 only)			16	mA	$V_{OUT} = V_{SS} -6V$
I_{CF}[3]	In, Out "1" Clamp Current (4009 only)			16	mA	$V_{OUT} = V_{SS} -6V$
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}[4]	Input High Voltage	$V_{SS}-1.5$		$V_{SS}+.3$	V	
V_{IL}	Input Low Voltage (4009 only)	V_{DD}		$V_{SS}-4.2$	V	
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	$V_{SS}-.5V$			V	$I_{OUT} = 0$
R_{OH}	I/O Output "0" Resistance (4009 only)		.25	1.0	kΩ	$V_{OUT} = V_{SS} -.5$
I_{OL}	I/O Output "1" Sink Current (4009 only)	5	12		mA	$V_{OUT} = V_{SS} -.5V$
I_{OL}	I/O Output "1" Sink Current (4009 only)	1.6	4		mA	$V_{OUT} = V_{SS} -4.85V$
I_{CF}	I/O Output "1" Clamp Current (4009 only)			16	mA	$V_{OUT} = V_{SS} -6V$
CAPACITANCE						
C_{ϕ}	Clock Capacitance		8	15	pF	$V_{IN} = V_{SS}$
C_{DB}	Data Bus Capacitance		7	10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance (4008 only)			10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance (4009 only)			15	pF	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance			10	pF	$V_{IN} = V_{SS}$

Notes: 1. The address lines will drive a TTL load if a 470Ω resistor is connected in series between the address output and the TTL input.
2. A 6.8kΩ resistor must be connected between Pin W and V_{DD} for TTL capability.
3. Resistors in series with TTL inputs may be required to limit current into V_{DD} or V_{SS} from TTL input clamp diodes.
4. TTL $V_{OH} = 2.4V$ will ensure 4009 $V_{IH} = V_{SS} -1.5$ via the 4009 latch. Refer to Figure 3.

A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{SS} - V_{DD} = 15V \pm 5\%$

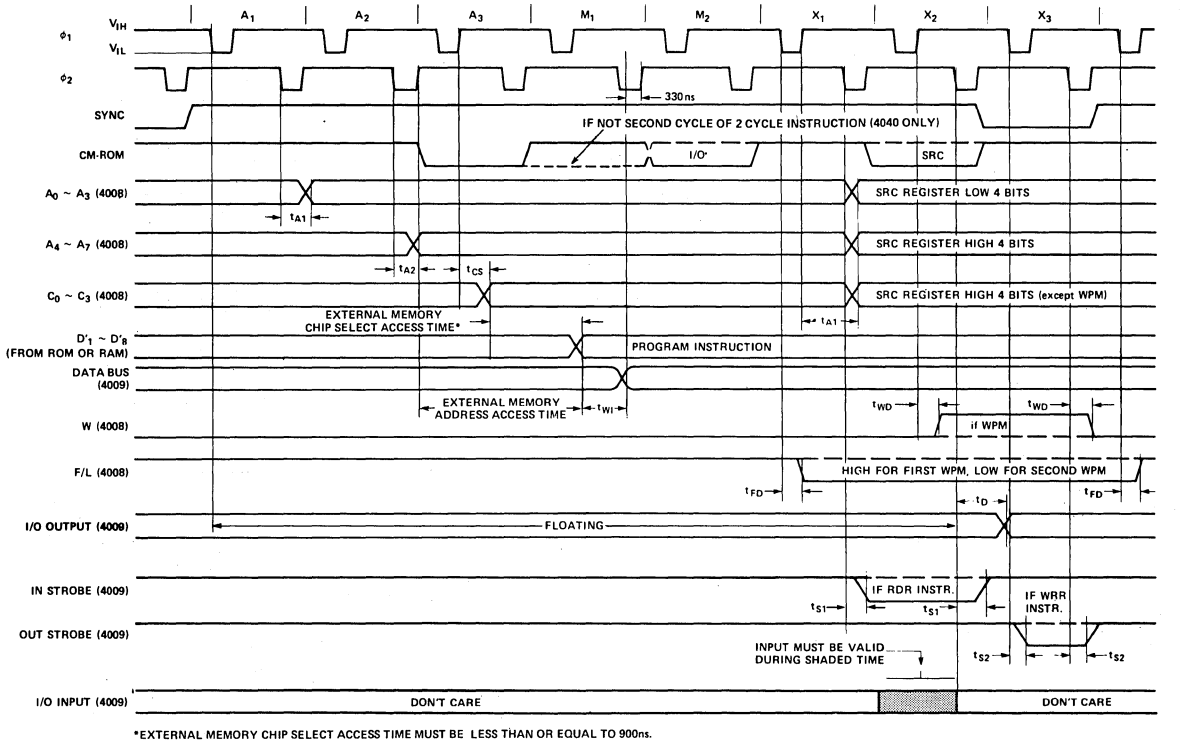
Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Times			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay $\phi 1$ to ϕ_2	400		500	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500 pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{A1}	Address to Output Delay at A_1, X_1 (4008)			580	ns	C_L = 250pF
t_{A2}	Address to Output Delay A_2 (4008)			580	ns	C_L = 250pF
t_{CS}	Chip Select Output Delay at A_3 (4008)			300	ns	C_L = 50pF
t_{WD}	W Output Delay (4008)			600	ns	C_L = 100pF
t_{FD}	F/L Output Delay (4008)	0.1		1	μs	C_L = 100pF
t_{WI}	Data In Write Time (4009)	470			ns	C_L = 200pF on data bus
t_D	I/O Output Delay (4009)			1.0	μs	C_L = 300pF
t_{S1}	IN Strobe Delay (4009)			450	ns	C_L = 50pF
t_{S2}	OUT Strobe Delay (4009)			1.0	μs	C_L = 50pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

Timing Diagram



*EXTERNAL MEMORY CHIP SELECT ACCESS TIME MUST BE LESS THAN OR EQUAL TO 900ns.

Figure 1. 4008 and 4009 Timing Diagram.

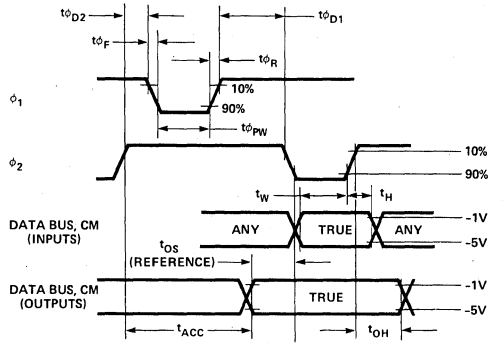
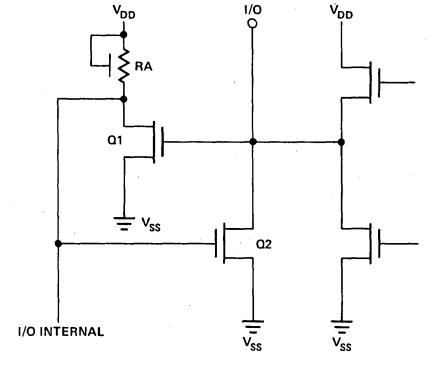


Figure 2. MCS-40 Timing Detail.



EXPLANATION:

WITH V_{SS} = +5V and V_{DD} = -10V, AN EXTERNAL TTL INPUTTING TO THE 4289 ON THE I/O LINE, RAISES THE I/O LINE TO 2.4V. THE Q1-RA INVERTER TURNS "OFF" AND Q2 PULLS THE I/O LINE TO V_{SS}. A LOW TTL SIGNAL OVERRIDES Q2. IF THE TTL OUTPUT GOES TO THE THIRD STATE, THE EXTERNAL I/O LINES REMAIN HIGH THROUGH Q2.

THE PURPOSE OF THIS CIRCUIT IS TO REMOVE RESISTORS TO V_{CC} = V_{SS} ON TTL OUTPUTS, AS R_I DOES ON 4001/4308 INPUT PORTS.

Figure 3. 4009 I/O Latch.

STANDARD MEMORY INTERFACE

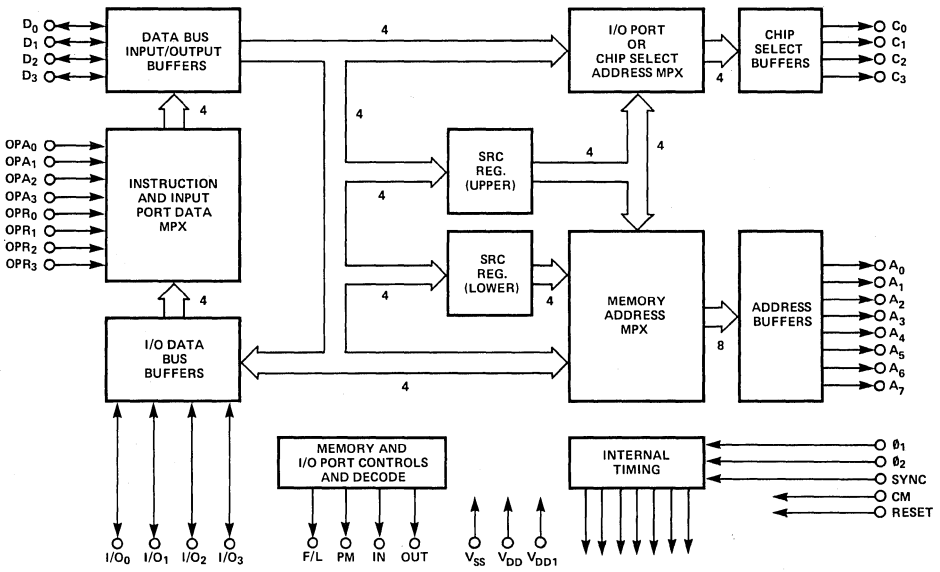
- **Direct Interface to all Standard Memories**
- **Allows Read and Write Program Memory**
- **Single Package Equivalent of 4008/4009**
- **TTL Compatible Address, Chip Select, Program Memory Data Lines**
- **40 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available With -40° to +85°C Operating Range**

The 4289 standard memory interface and I/O interface enables the CPU devices to utilize standard memory components as program data memory. Notably, PROMs (4702A), RAMs (2102) and ROMs can be arranged in a memory array to facilitate system development. Programs generated using the 4289 interface can be committed to MCS-40™ ROMs (4308 and 4001) with no change to software.

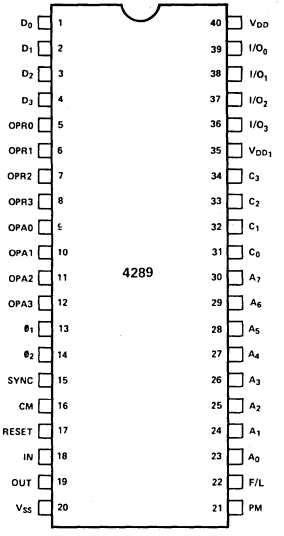
The 4289 also contains a 4 bit bi-directional I/O port and necessary steering logic to multiplex a host of I/O sources to the CPU. The Read and Write Program Memory instruction allows the user to store data and modify program memory. The device directly addresses 4K of program memory. The address is obtained sequentially during A_1-A_3 states of an instruction cycle. The eight bit instruction is presented to the CPU during M_1 and M_2 states of the instruction cycle via the four bit data bus.

The 4289 stores the SRC instruction operand as an I/O address and responds to the ROM I/O instructions (WRR and RDR) by reading or writing data to and from the processor and 4289 I/O bus.

BLOCK DIAGRAM



PIN CONFIGURATION



Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
5-8	OPR_0-OPR_3/Pos.	The high order 4 bits (OPR) of the instruction or data (RPM) from the PROGRAM MEMORY are transferred to the 4289 on these pins.
9-12	OPA_0-OPA_3/Pos.	The low order 4 bits (OPA) of the instruction or data (RPM) are transferred to the 4289 on these pins.
13-14	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
15	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
16	CM/Neg.	Command input driven by CM-ROM output of processor. Used for decoding SRC and I/O instructions.
17	RESET/Neg.	RESET input. A negative logic "1" level (V_{DD}) applied to this input resets the FIRST/LAST flip-flop.
18	IN/Neg.	Output signal, active low (V_{DD}), generated by the 4289 when the processor executes an RDR or RPM instruction.
19	OUT/Neg.	Output signal, active low (V_{DD}), generated by the 4289 when the processor executes a WRR or WPM instruction.
20	V_{SS}	Most positive supply voltage.
21	PM/Neg.	Output signal, active low (V_{DD}), generated by the 4289 when the processor executes an RPM or WPM instruction.
22	F/L/Neg.	Output signal generated by the 4289 to indicate which half-byte of PROGRAM MEMORY is to be operated on (V_{DD} = OPR, V_{SS} = OPA).
23-30	A_0-A_7/Pos.	Address output buffers. The demultiplexed address values generated by the 4289 from the address data supplied by the processor at A_1 and A_2.
31-34	C_0-C_3/Pos.	Chip select output buffers. The address data generated by the processor at A_3 or during an SRC are transferred here.
35	V_{DD1}	Supply voltage for address and chip select buffers.
36-39	I/O_3-I/O_0/Pos.	Bidirectional I/O data port. Data to and from I/O devices or data to write PROGRAM MEMORY are transferred via these pins.
40	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V ± 5%.

Functional Description

The 4289 enables the 4 bit CPU chip (4004 or 4040) to interface to standard memory components. This allows construction of prototype or small volume systems using electrically programmable ROMs or RAMs in place of 4001 or 4308 mask programmable ROMs. Since 4001s or 4308s also contain up to 16 mask programmable I/O ports, the 4289 has provisions for directly addressing 16 channels of 4 bit I/O ports. In its role as a Memory and I/O interface device, the 4289 provides three different types of operation, namely:

a. Interface to Program Memory for instruction fetch operations.
b. Interface to Input/Output ports for storing or fetching data using WRR, RDR instruction.
c. Interface to R/W Program Memory for program alteration using WPM, RPM instructions. This feature may also be used for storing or fetching data, thus allowing the use of standard R/W RAM for data storage via the 4289.

These three basic operations will be discussed in detail in the following paragraphs.

Instruction Execution

The contents of the data bus at A_1, A_2, and A_3 are latched by the 4289 and transferred to the address and chip select output buffers. The low order address at A_1 is transferred to A_0-A_3 outputs, the middle order address at A_2 is transferred to A_4-A_7 outputs and the high order address at A_3 is transferred to C_0-C_3 outputs. These 12 output lines provide the necessary address and chip select signals to interface to a 4K x 8 bit Program Memory.

The 8 bit word selected by A_0-A_7 and C_0-C_3 is transferred to the processor via the $OPR_{0\text{-}3}$, $OPA_{0\text{-}3}$ input lines and the data output buffer. The high order bits (OPR) are transferred at M_1 and the low order 4 bits (OPA) are transferred at M_2.

The 4289 has been designed to work equally well with either the 4004 or 4040 processor elements. Since the 4040 is provided with two CM-ROM controls which allow it to directly address up to 8K x 8 bits of Program Memory (4K x 8 bits selected by each CM-ROM control), two 4289s would be required for full memory capability. In this case, one 4289 would be controlled by CM-ROM0 and the other by CM-ROM1. The 4289 which receives CM at A3 would be enabled to transfer data at M_1 and M_2.

It should be noted that the two CM-ROM controls permit the simultaneous use of 4001, 4308, and 4289 in the same system. The ROM's 4001 and 4308 can be mixed and assigned to one CM-ROM control line while a single 4289 can be assigned to the other. However, within one CM-ROM control line, 4289, 4001, and 4308 cannot be mixed, since the 4289 does respond to a full 4K of memory by its design and thus would overlap program memory address with the 4001 or 4308.

I/O Port Operation

When the processor executes an I/O port instruction (WRR or RDR), a previously selected I/O port (via an SRC instruction) is enabled to receive or transmit 4 bits of data. In the case of WRR, the selected output port receives the 4 bit contents of the processor accumulator, and in the case of RDR, the selected input port transmits 4 bits of data to the processor accumulator. The 4 bit value sent out at X_2 time of the SRC instruction is used as the port address. Since the 4289 is capable of addressing 16 4 bit I/O ports, it must therefore be capable of storing the SRC address sent by the processor and presenting that address to the external I/O port selection logic for WRR or RDR instructions which follow. To accomplish this, the 4289 behaves as follows:

a. When the processor executes an SRC instruction, the 4289 stores the address sent out by the processor at X_2 and X_3. The contents of the upper 4-bits of the SRC register are transferred during every X_1 time to the chip select lines and are available for subsequent I/O instructions' port selection.
b. When the processor then executes a WRR instruction, the 4289 latches the data sent out by the processor at X_2 and transfers this data to the I/O output buffer. This buffer is enabled during X_3 and transmits the data to the selected output port. So that external port logic may be enabled to receive the data, the 4289 generates the OUT strobe signal.
c. When the processor executes an RDR instruction, the 4289 generates the IN strobe. This enables the selected input port to transmit its data to the I/O bus, where it is latched by the 4289 and transferred to the processor at X_2.

Note that in a system using ROMs, the 4 bit port number is decoded by the ROM chip itself. Where a 4289 is used, the 4 bit port number outputted at the chip select lines C_0-C_3 must be externally decoded to select the appropriate I/O device.

Read/Write Program Memory Operations

If the 4289 is used in conjunction with the 4040, both the WRITE and READ PROGRAM MEMORY (WPM/RPM) functions are directly available (only the WPM is available for 4004 systems). To accomplish these operations, the following are required:

a. A program memory address.
b. The proper control signals.
c. A means of transmitting the data to be stored or fetched.

The 4289 provides all of these as described below.

Program Memory Address

The address for an RPM or WPM operation is provided by the 8 bit contents of the SRC register. Note that the RPM or WPM instruction must have been preceded by an SRC instruction which loaded an 8-bit address into the 4289's SRC register. This 8-bit address is the full address of an 8-bit word in one Read/Write Program Memory page (256 bytes). If more than one page of Read/Write Program Memory is desired, these pages must be selected by external logic controlled via other output ports of the system. At X_1 of every instruction cycle the 8 bit value contained in the SRC register is transferred to the address output buffers A_0-A_7. This address will select 1 out of 256 program memory words.

During execution of WPM or RPM, the 4289 does not transfer the high order 4 bits of the SRC register to C_0-C_3.

Instead, it forces all 4 chip select output buffers to a logic "1" state (positive true logic or V_{SS}). This forcing of C_0-C_3 to all "1s" can be used to indicate the execution of a WPM or RPM instruction. The PM output signal is also generated whenever a proper memory operation (WPM or RPM) is being performed. If only one page of R/W memory is required, the 1111 condition on C_0-C_3 or the PM signal can be used to enable that page. If more than one page is required, an additional output port of the system along with external logic will be necessary to provide the 1 out of 16 page select function.

Since the program memory is organized as 8 bit words, and since RPM and WPM are transmitting only 4 bit words, it is also necessary to specify either the upper or lower half-byte of program memory.

This is done automatically by a FIRST/LAST flip-flop and output signal in the 4289. The state of this flip-flop is used to generate the control signal F/L which determines the proper half-byte of program memory. If F/L is a logic "1" state (V_{DD}), OPR is selected. When F/L is a logic "0" (V_{SS}), OPA is selected. The user can directly reset the FIRST/LAST flip-flop to logic "0" (V_{SS}) in the 4289 by applying a RESET signal.

Starting from a "reset" condition the FIRST/LAST flip-flop automatically toggles after executing either an RPM or WPM instruction. Hence, odd numbered program memory operations select OPA and even numbered program memory operations select OPR (starting with #1 from reset). Alternate WPM and RPM instructions should be used with care since this can cause an out of sequence with the F/L line.

The OUT strobe signal is generated only during WRR and WPM instructions. Hence, the combination of the PM signal (or C_0-C_3 = 1111) and the OUT signal can be used as a WRITE ENABLE for R/W program memory.

Program Memory Data Paths

When the processor executes the WPM instruction, the 4289 latches the data sent out at X_2 by the processor and transfers it via the I/O output buffers to the I/O port. The I/O port must be connected to the data input pins of the R/W memory chips. (Refer to Figure 2 which follows.)

If the processor (4040) executes the RPM instruction, then the entire 8 bit program memory word is transferred to the OPR_0-OPR_3 and OPA_0-OPA_3 inputs of the 4289. Depending on the state of the F/L signal, either the OPA or the OPR half-byte is automatically selected by the 4289.

Data Storage

If Read/Write Memory is interfaced to via a 4289 and is used for data storage only, the data is accessed via the WPM and RPM instructions just as Read/Write Program Memory would be accessed. The only difference that the chip select lines C_0-C_3 are never used to select the Read/Write Memory in an instruction fetch operation. The PM pulse would be used to select the Read/Write data memory.

Note that the RAM instructions RDM, WRM, WR0-WR3, RD0-RD3, SBM and ADM cannot be used to access this type of data Read/Write memory.

4008/4009 and 4289 Differences

The functional differences between a 4289 and a 4008/4009 Standard Memory Interface component pair are as follows:

1. The PM pulse of the 4289 (negative logic) is inverted in comparison with the W pulse of the 4008 (positive logic).
2. The W pulse of the 4008 begins in X2 and ends in X3. The 4289's PM pulse begins in X1 and ends in A1.
3. The OUT strobe of the 4289 goes to logical 1 (V_{DD}) for the WRR instructions and the WPM instructions. The OUT strobe of the 4009 goes to logical 1 (V_{DD}) for the WRR instruction only.

4289 Applications

The 4289 can be used to form systems of widely varying complexity. Simple systems containing only one page (256 x 8) of PROGRAM MEMORY and few I/O ports, or more complex systems requiring as many as 32 pages (8K x 8) of memory and 32 I/O ports can readily be implemented. Several examples will be described here.

1. Basic PROM Microcomputer System (Figure 1). This system contains:
   a. 1K x 8 bits of PROGRAM MEMORY (4702A PROM)
   b. 1280 bits of DATA MEMORY (4002 RAM) organized as 16 20-character registers
   c. 4 RAM output ports (4002)
   d. 4 I/O ports.

This system uses a 3205 1 out of 8 decoder to decode the input port addressed by the CPU. Two chip select signals (C_0 and C_1) are combined with the IN signal, which is activated low to indicate an input operation, to select one of four input ports. The 3205 enables one DM 7098 three-state buffer.

In a similar manner, one 3205 and the OUT signal, which is activated to indicate an output operation, are used to select one of four output ports.

2. Standard PROM and RAM Memory System (Figure 2). This system again contains 4 pages of PROM storage but, in addition, has one page of RAM storage which can be used for either PROGRAM or DATA storage by using the WPM/RPM instructions. (The RPM instruction is valid only with the 4040.) The RAM storage has been implemented with two 4101's (256 x 4 static RAM). Notice that separate WRITE ENABLE signals must be generated for the upper and lower half-bytes of RAM.

Note that the inputs to the 4101 RAMs are connected to the 4289 I/O port while their outputs are connected directly to the OPR-OPA lines.

The 4101 RAMs can be chip selected through their active low chip select lines in either of two cases:

1. By an address decode of 4 when the RAMs are addressed as Program Memory for instruction fetch.
2. By the PM signal when addressed as a RAM read or write via an RPM or WPM instruction. For write operations, the TTL logic shown selects one of the

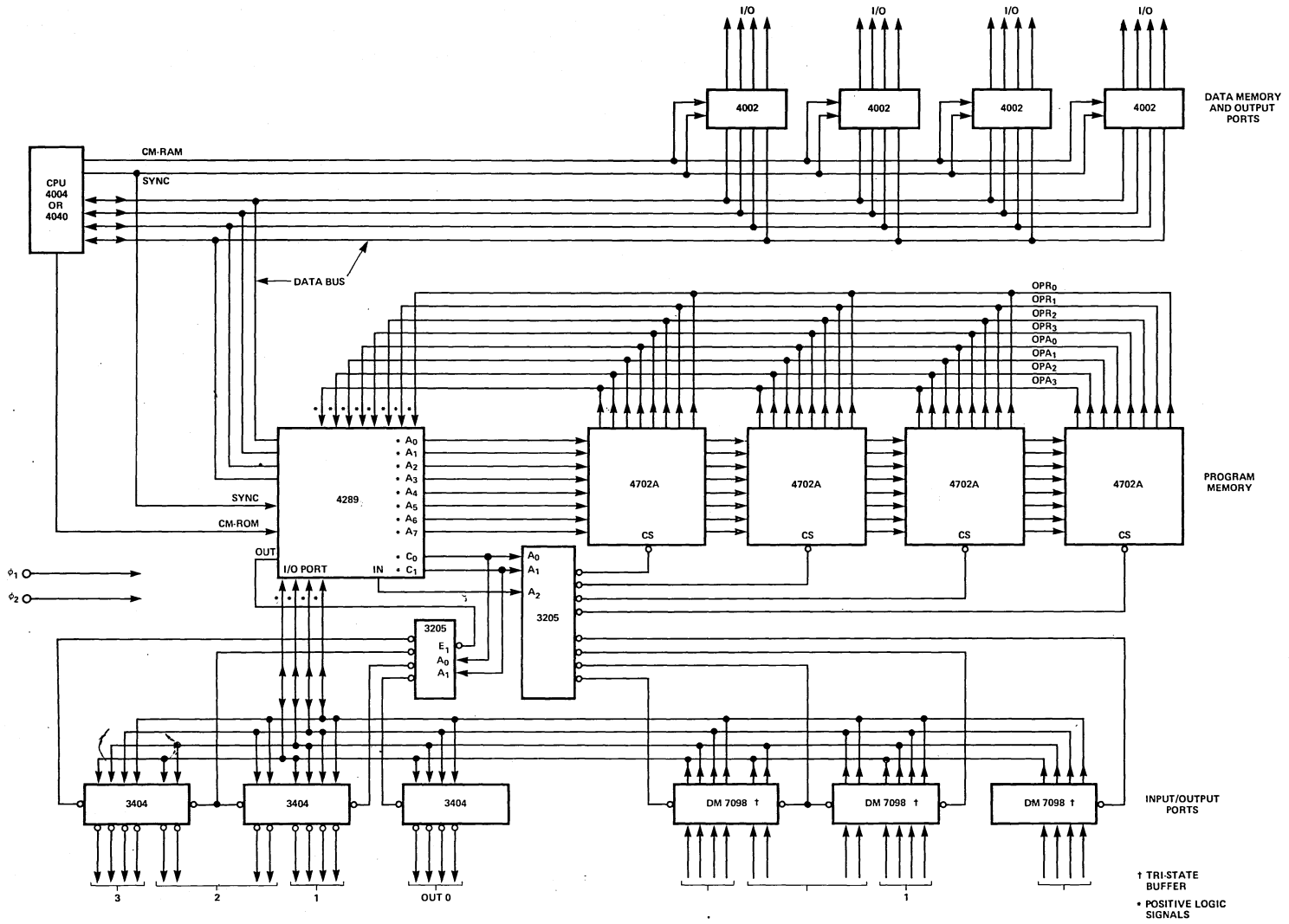


Figure 1. Basic PROM Memory System

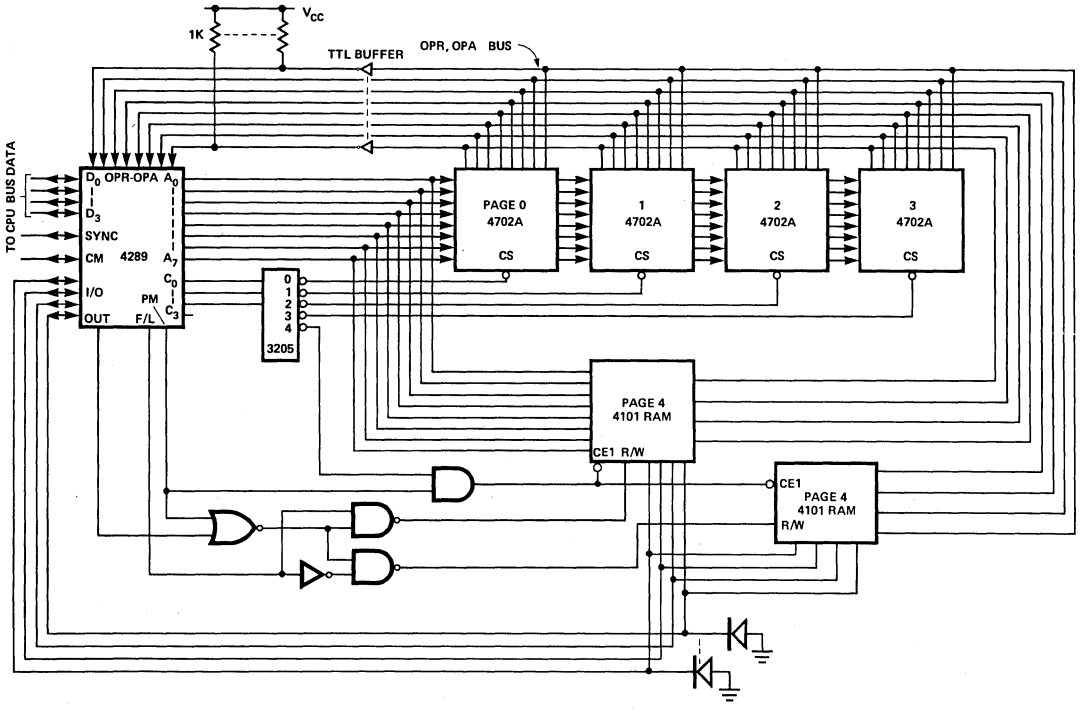


Figure 2. PROM and RAM System.

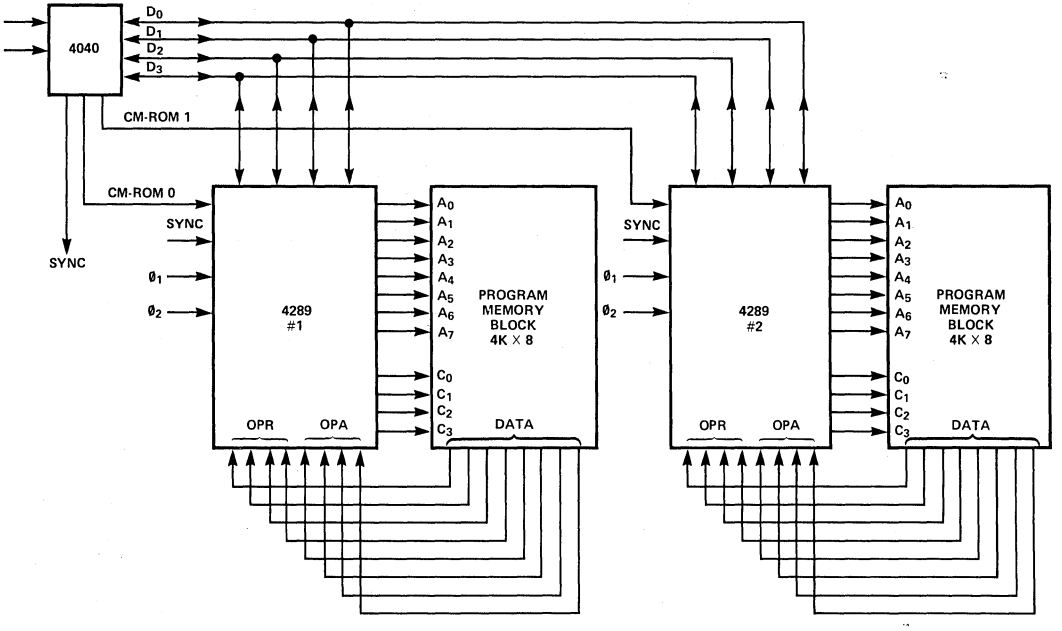


Figure 3. Two Memory Bank System.

two 4101 Read/Write lines according to the F/L signal of the 4289.

The TTL buffers are placed on the data bus to facilitate the compatability between the NMOS RAMs and the PMOS PROMS. The inverters limit the negative excursion of the PROM outputs which may damage the RAMs. The TTL pull-up is required to ensure the V_{IH} threshold level.

3. Two Memory Bank System (Figure 3). Two 4289s are used in this 4040 system giving addressability to a full 8K bytes of PROM memory. In this case each 4289 is controlled from a separate CM-ROM control signal. The CM-ROM$_0$ and CM-ROM$_1$ lines are generated by the 4040. This system cannot be implemented with the 4004.

4289, 4702A System Considerations

1. When utilizing the 4289 with more than six 4702As,a TTL buffer as shown in Figure 4 should be inserted in series with the OPR, OPA lines to achieve maximum clock rate. The buffer may be inverting or non-inverting.

   However, use of a 5.1KΩ resistor on the 4702A output to V_{SS} will allow up to 6 x 4702As to be used without TTL buffers and still achieve maximum clock rate.

2. 4702A access times to meet MCS-40 at $t_{CY} = 1.35\mu$ sec are guaranteed with pure capacitive load of 75pF and with load of 240pF plus a TTL buffer on the 4702A output.

   To operate with more than 6 x 4702A without TTL buffer, the limiting specification is t_{CO} and this increases 5 nsec/pF for capacitance above 75pF; MCS-40 t_{CY} must be increased 2.5ns/pF.

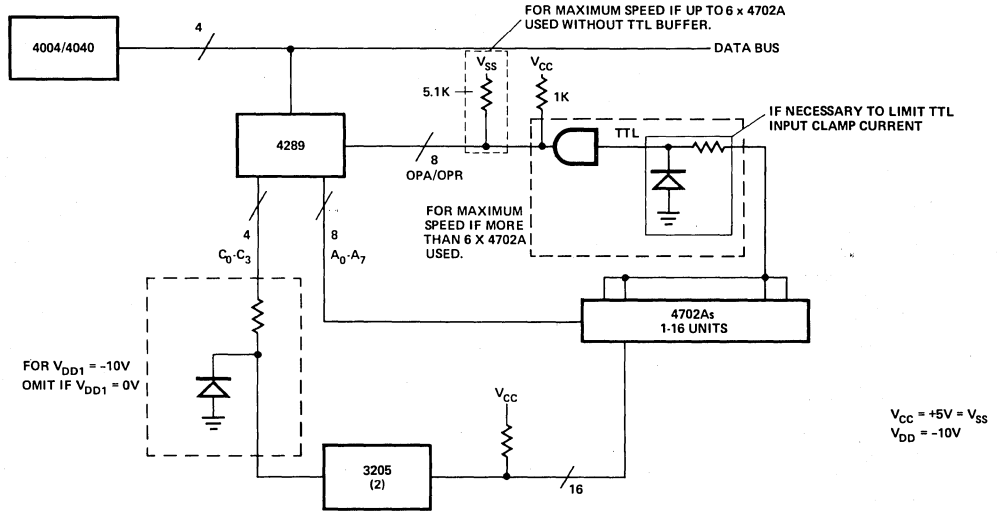


Figure 4. 4289 and 4702A Block Diagram.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; 4289 V_{DD1} = V_{SS} -5V. Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		30	40	mA	T_A = 25°C
INPUT CHARACTERISTICS—ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	µA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	OPR/OPA
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS—ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	µA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
I_{OL}[1]	Address Line Sinking Current	7	13		mA	V_{OUT} = V_{SS}, V_{DD1} = V_{DD}
I_{OL}	In, Out, F/L, PM Sinking Current, Chip Select	1.6	4		mA	V_{OUT} = V_{SS} -4.85 V_{DD1} = V_{DD}
V_{OL}[2]	Chip Select Output Low Voltage			V_{DD1}+.5	V	I_{OL} = .4mA
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT} = V_{SS} -.5V
R_{OH}	Address, Chip Select Output Resistance, "0" Level		.6	1.2	kΩ	V_{OUT} = V_{SS} -.5V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	µA	
V_{IH}[3]	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance		.25	1.0	kΩ	V_{OUT} = V_{SS}-.5
I_{OL}	I/O Output "1" Sink Current	5	12		mA	V_{OUT} = V_{SS} -.5
I_{OL}	I/O Output "1" Sink Current	1.6	4		mA	V_{OUT} = V_{SS} -4.85V
I_{CF}	I/O Output "1" Clamp Current			10	mA	V_{OUT} = V_{SS} -6V

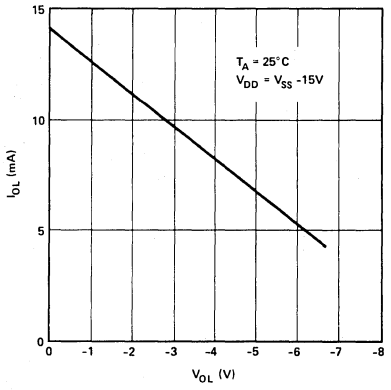
Notes: 1. The address lines will drive a TTL load if a 470Ω resistor is connected in series between the address output and the TTL input.
2. 4289 Address (A_0-A_7) Outputs are also tied to V_{DD1} but are tested with capacitive load only.
3. TTL V_{OH} = 2.4V will ensure 4289 V_{IH} = V_{SS} -1.5V via the 4289 latch. Refer to Figure 5.

D.C. and Operating Characteristics (Continued)

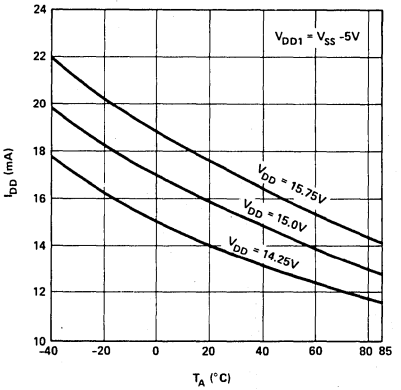
CAPACITANCE

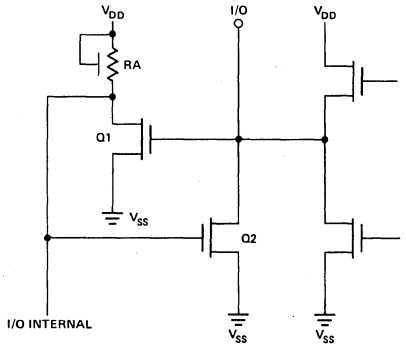
Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
C_ϕ	Clock Capacitance		14	20	pF	$V_{IN} = V_{SS}$
C_{DB}	Data Bus Capacitance		7	10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance			15	pF	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance			10	pF	$V_{IN} = V_{SS}$

4289 I_{OL} VS. V_{OL} (FOR I/O PINS)



4289 I_{DD} VS. TEMPERATURE





EXPLANATION:

WITH V_{SS} = +5V and V_{DD} = -10V, AN EXTERNAL TTL INPUTTING TO THE 4289 ON THE I/O LINE, RAISES THE I/O LINE TO 2.4V. THE Q1-RA INVERTER TURNS "OFF" AND Q2 PULLS THE I/O LINE TO V_{SS}. A LOW TTL SIGNAL OVERRIDES Q2. IF THE TTL OUTPUT GOES TO THE THIRD STATE, THE EXTERNAL I/O LINES REMAIN HIGH THROUGH Q2.

THE PURPOSE OF THIS CIRCUIT IS TO REMOVE RESISTORS TO V_{CC} = V_{SS} ON TTL OUTPUTS, AS R_I DOES ON 4001/4308 INPUT PORTS.

Figure 5. 4289 I/O Latch.

A.C. Characteristics

T_A = 0°C to 70°C, V_{SS} -V_{DD} = 15V ±5%

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Time			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{A1}[4]	ϕ_1 to Output Delay A_1		400	1000	ns	C_L = 250pF; A_0-A_3
t_{TA1}[4]	Data Bus to Output Delay A_1		500	700	ns	C_L = 250pF; A_0-A_3
t_{A2}[4]	ϕ_1 to Output Delay A_2		400	580	ns	C_L = 250pF; A_4-A_7
t_{TA2}[4]	Data Bus to Output Delay A_2		500	700	ns	C_L = 250pF; A_4-A_7
t_{CS}[4,5]	ϕ_1 to Chip Select Output Delay A_3		150	350	ns	C_L = 50pF
t_{TC}[4,5]	Data Bus to Chip Select Output Delay A_3		250	350	ns	C_L = 50pF
t_{WID}	OPR to Data Bus Delay		250	350	ns	C_{OUT} = 20pF, Data Bus
t_{SRC}	Output Delay at X_1 Time		400	700	ns	C_L = 250pF
t_{S1}	IN Strobe Delay Time			500	ns	C_L = 50pF
t_{S2}	OUT Strobe Delay Time, Falling			500	ns	C_L = 50pF
t_{FD}	F/L and PM Delay Time		300	500	ns	C_L = 100pF
$t_{W,I/O}$	I/O Input Write Time	400	250		ns	
$t_{H,I/O}$	I/O Input Hold Time	40	0		ns	
$t_{D,I/O}$	I/O Output Delay Time		400	1000	ns	C_L = 300pF
t_{WI}	Data In Write Time	350			ns	C_{OUT} = 200pF, Data Bus

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. t_{A1}, t_{A2}, t_{CS} apply if Data Bus is valid before ϕ_1 trailing edge. t_{TA}, t_{TC} apply if Data Bus becomes valid after ϕ_1 trailing edge.
5. Measured at output of 3205 decoder.

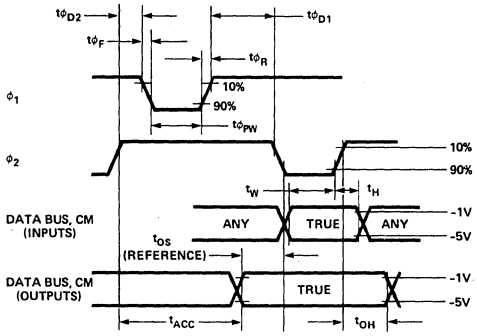


Figure 6. MCS-40 Timing Detail.

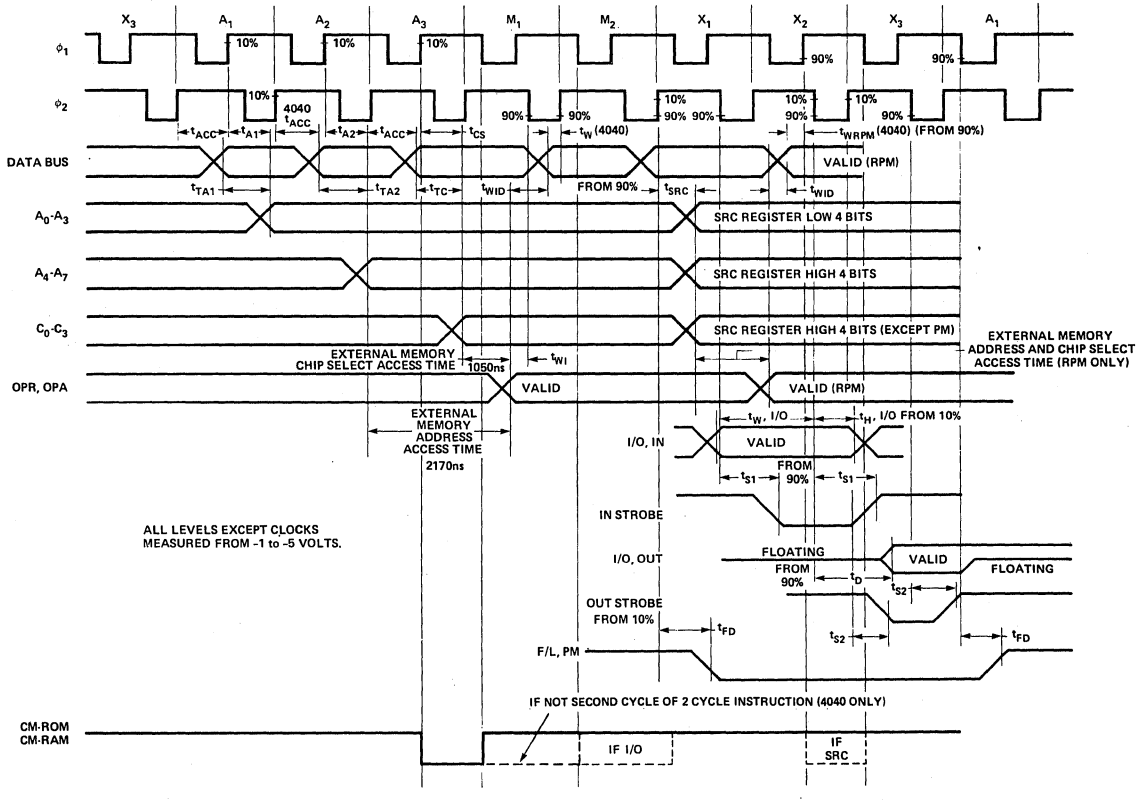


Figure 7. MCS-40 Timing Diagram for 4289.

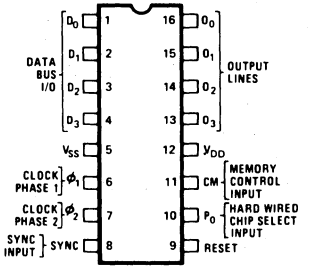
320 BIT RAM AND 4 BIT OUTPUT PORT

- **Four Registers of 20 4 Bit Characters**
- **Direct Interface to MCS-40™ 4 Bit Bus**
- **Output Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available With -40° to +85°C Operating Range**

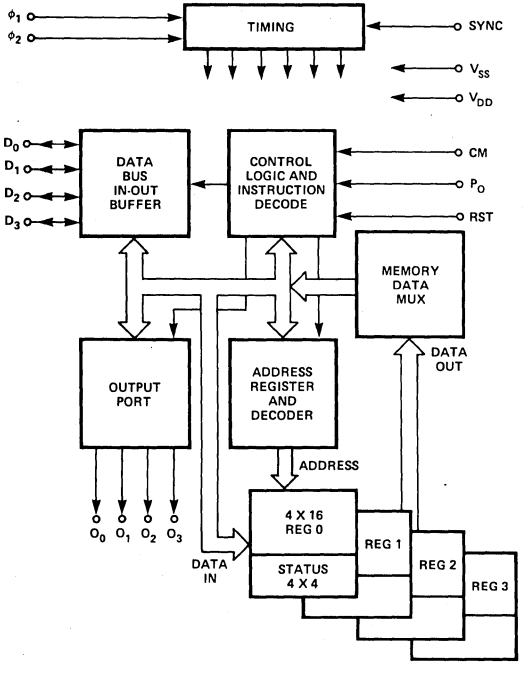
The 4002 performs two distinct functions. As a RAM it stores 320 bits arranged in 4 registers of twenty 4 bit characters each (16 main memory characters and 4 status characters). As a vehicle of communication with peripheral devices, it is provided with 4 output lines and associated control logic to perform output operations. The 4002 is a PMOS device and is compatible with all MCS-40™ components.

The 4002 is available in two options, the 4002-1 and 4002-2. Along with an external pin connected to either V_{DD} or V_{SS}, a two bit chip selection address is provided allowing a maximum of 1280 bits of 4002 RAM on a single MCS-40 CM-RAM line. Thus, the four CM-RAM lines give a maximum of 5120 bits of 4002 RAM in an MCS-40 system.

PIN CONFIGURATION



BLOCK DIAGRAM



MCS-40

Pin Description

Pin No.	Designation	Description of Function
1-4	D_0-D_3	Bidirectional data bus. All address, instruction and data communication between processor and the RAM MEMORY or the output port is transmitted on these 4 pins.
5	V_{SS}	Most positive supply voltage.
6-7	ϕ_1-ϕ_2	Non-overlapping clock signals which are used to generate the basic chip timing.
8	SYNC	Synchronization input signal driven by SYNC output of processor.
9	RESET	RESET input. A logic negative level (V_{DD}) applied to the chip will cause a clear of all output and control static flip-flops and will clear the RAM array. To completely clear the memory, RESET must be applied for at least 32 instruction cycles (256 clock periods) to allow the internal refresh counter to scan the memory. During RESET the data bus output buffers are inhibited (floating condition).
10	P_0	The chip number for a 4002 is assigned as follows:

Chip No.	4002 Option	P_0	SRC ADDRESS (RRR EVEN) D_3 D_2
0	4002-1	V_{SS}	0 0
1	4002-1	V_{DD}	0 1
2	4002-2	V_{SS}	1 0
3	4002-2	V_{DD}	1 1

11	CM	Command input driven by CM-RAM output of processor. Used for enabling the device during the decoding SRC and instructions.
12	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V ± 5%.
13-16	O_3-O_0	Four bit output port used for transferring data from the CPU to the users system. The outputs are buffered and data remains stable after the port has been loaded. This port can be made low power TTL compatible by placing a 12K pull-down resistor to V_{DD} on each pin.

Functional Description

The twenty 4 bit characters for each 4002 register are arranged as follows:

1. 16 characters addressable by an SRC instruction. Four 16 character registers constitute the "main" memory.
2. 4 characters addressable by specific RAM instructions. Four 4 character registers constitute the "status character" memory.

The status character location (0 through 3) as well as the operation to be performed on it are selected by the OPA portion of the I/O and RAM instructions.

The RAM Registers Locations, Status Characters, and Output Port are select and accessed with a corresponding RAM Instruction.

There can be up to four RAMS per RAM Bank (CM-RAM). There can be four RAM banks per system without decoding or 8 with decoding.

Bank switching is accomplished by the CPU after receiving a "DCL" (designated command line) instruction. Prior to execution of the DCL instruction the desired CM-RAM code has been stored in the accumulator (for example through an LDM instruction). During DCL the CM-RAM code is transferred from the accumulator to the CM-RAM register. The RAM bank is then selected starting with the next instruction.

If no DCL is executed prior to SRC, the CM-RAM_0 will automatically be activated at the X_2 state of the instruction cycle provided that RESET was applied at least once to the system (most likely at the start-up time).

Instruction Execution

An SRC (Send Register Control) instruction is executed to select a RAM and a character within that RAM (for a RAM read or write instruction) prior to the succeeding RAM or I/O instruction's execution.

The eight bits of the register pair addressed by the SRC instruction are interpreted as follows:

a. The first four bits sent out at X_2 time select one out of four chips and one out of four registers. The two higher order bits (D_3, D_2) select the chip and the two lower order bits (D_1, D_0) select the register.

b. The second 4-bits (X_3 time) select one 4-bit character out of 16. The address is stored in the address register of the selected chip (second 4 bits are not used for status character reads or writes or for I/O output instructions).

The following RAM and I/O output instructions are executed by the 4002.

1. RDM Read RAM character

   The content of the previously selected RAM main memory character is transferred to the accumulator. The 4 bit data in memory is unaffected.

2. RDO-3 Read RAM status characters 0-3

   The 4 bits of status characters 0-3 for the previously selected RAM register are transferred to the accumulator.

3. WRM Write accumulator into RAM character

   The accumulator content is written into the previously selected RAM main memory character location.

4. WRO-3 Write accumulator into RAM status characters 0-3

   The content of the accumulator is written into the RAM status characters 0-3 of the previously selected RAM register.

5. WMP Write memory port

   The content of the accumulator is transferred to the RAM output port of the previously selected RAM chip. The data is available on the output pins until a new WMP is executed on the same RAM chip. The content of the ACC and the carry/link are unaffected. (The LSB bit of the accumulator appears on O_0, Pin 16 of the 4002.)

6. ADM Add from memory with carry

   The content of the previously selected RAM main memory character is added to the accumulator with carry. The RAM character is unaffected.

7. SBM Subtract from memory with borrow

   The content of the previously selected RAM character is subtracted from the accumulator with borrow. The RAM character is unaffected.

Timing Considerations

Presence of CM-RAM during X_2 tells 4002's that an SRC instruction was received. For a given combination of data at X_2 on D_2, D_3, only the chip with the proper option and P_0 state will be ready for the I/O or RAM operation that follows.

When an I/O or RAM instruction is received by the CPU, the CPU will activate one CM-RAM line during M_2, in time for the 4002's to receive the OPA (2nd part of the instruction), which will specify the I/O or RAM operation to be performed.

In the I/O mode of operation, the selected 4002 chip (by SRC), after receiving the OPA of an I/O instruction (CM-RAM activated at M_2), will decode the instruction.

If the instruction is WMP, the data present on the data bus during $X_2 \cdot \phi_2$ will set the output flip-flops associated with the I/O pins. That information will be available until next WMP for peripheral devices control.

In the RAM mode, the operation is as follows: When the CPU receives an SRC instruction, it will send out the content of the designated index register pair during X_2 and X_3 and will activate one CM-RAM line at X_2 for the previously selected RAM bank.

All RAM mode instructions will be executed during the X_2 and X_3. The instruction decoding is performed during the M_2 time when the OPA portion of the instruction is decoded. The CM-RAM of the selected Bank is enabled at that time.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to V_{SS}	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

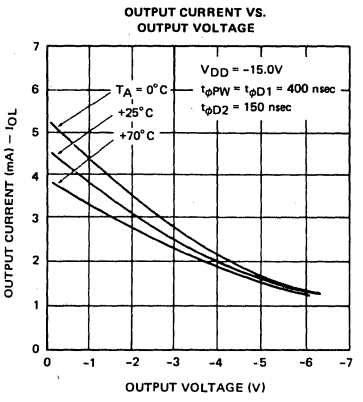
D.C. Characteristics

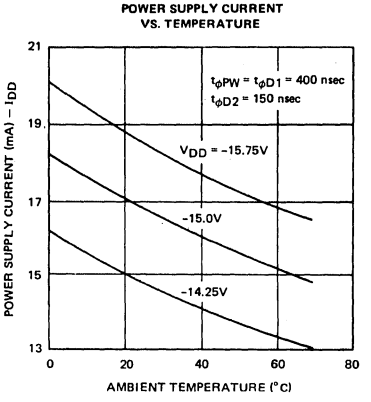
T_A = 0°C to 70°C; V_{SS}-V_{DD} = 15V ±5%; $t_{\phi PW} = t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec. Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless otherwise specified.

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
SUPPLY CURRENT						
I_{DD}	Average Supply Current		17	33	mA	T_A = 25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	µA	V_{IL}=V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS – ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	µA	V_{OUT}=-12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT}=V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL}=0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT}=0
R_{OH}	I/O Output "0" Resistance		1.2	2	kΩ	V_{OUT}=V_{SS}-.5V
I_{OL}	I/O Output "1" Sink Current	2.5	5		mA	V_{OUT}=V_{SS}-.5V
I_{OL}[1]	I/O Output "1" Sink Current	0.8	3		mA	V_{OUT}=V_{SS}-4.85V
V_{OL}	I/O Output Low Voltage	V_{SS}-12		V_{SS}-6.5	V	I_{OUT}=50µA
CAPACITANCE						
C_{ϕ}	Clock Capacitance		8	15	pF	V_{IN}=V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN}=V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN}=V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN}=V_{SS}

Note: 1. For TTL compatibility, use 12kΩ external resistor to V_{DD}.

Typical D.C. Characteristics





A.C. Characteristics

T_A = 0°C to 70°C, V_{SS}-V_{DD} = 15V ±5%.

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t_{\phi R}$	Clock Rise Time			50	ns	
$t_{\phi F}$	Clock Fall Times			50	ns	
$t_{\phi PW}$	Clock Width	380		480	ns	
$t_{\phi D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t_{\phi D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT}=20pF
t_D	I/O Output Delay			1500	ns	C_{OUT}=100pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

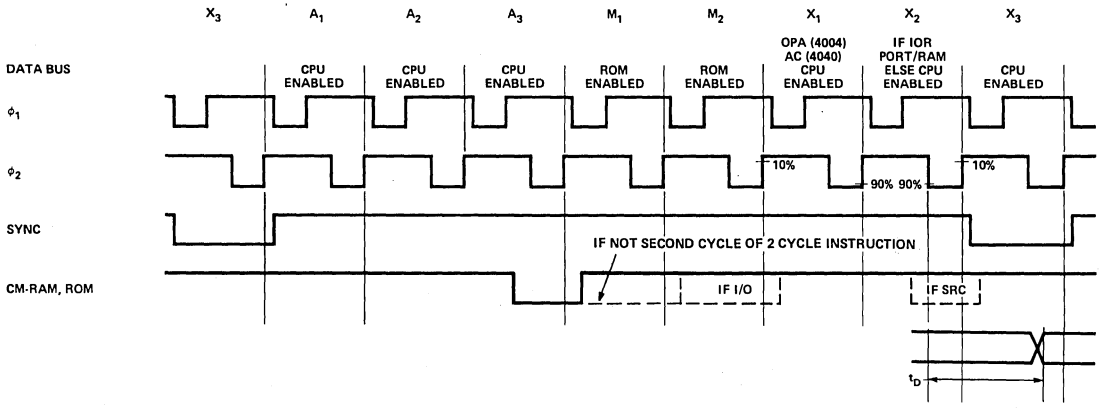


Figure 1. Timing Diagram.

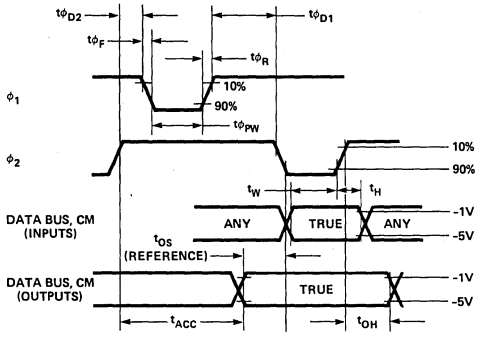


Figure 2. Timing Detail.

1024 BIT (256 x 4) STATIC MOS RAM WITH SEPARATE I/O

- 256 x 4 Organization to Meet Needs for Small System Memories
- Access Time: 1 µsec Max.
- Single +5V Supply Voltage
- Directly TTL Compatible: All Inputs and Outputs
- Statis MOS: No Clocks or Refreshing Required
- Simple Memory Expansion: Chip Enable Input
- Compatible with the 4289
- Inputs Protected: All Inputs Have Protection Against Static Charge
- Low Cost Packaging: 22 Pin Plastic Dual-In-Line Configuration
- Low Power: Typically 150mW
- Three-State Output: OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

The Intel® 4101 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 4101 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

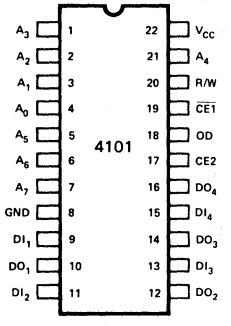
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bi-directional logic.

The Intel® 4101 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

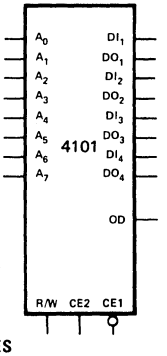
Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

MCS-40

PIN CONFIGURATION



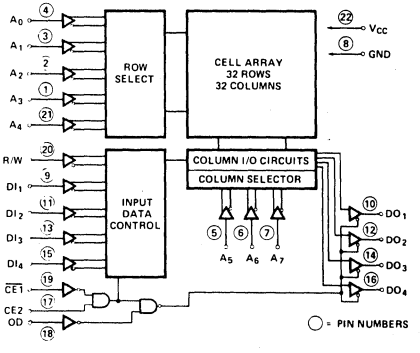
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	OD	OUTPUT DISABLE
$A_0 - A_7$	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

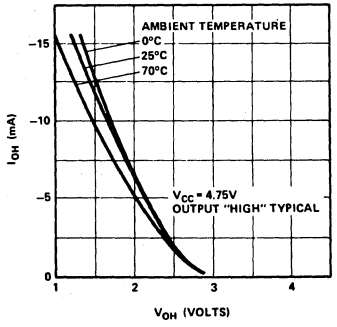
D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

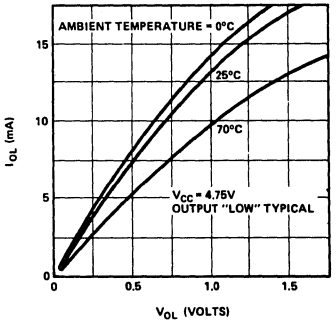
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current[2]			15	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	I/O Leakage Current[2]			-50	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150 μA

Typical D.C. Characteristics

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Input and Output tied together.

A.C. Characteristics

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	1,000			ns	
t_A	Access Time			1,000	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			800	ns	V_{IN} = +0.65V to +2.2V
t_{OD}	Output Disable To Output			700	ns	Timing Reference = 1.5V
t_{DF}[3]	Data Output to High Z State	0		200	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	1,000			ns	
t_{AW}	Write Delay	150			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	900			ns	V_{IN} = +0.65V to +2.2V
t_{DW}	Data Setup	700			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	100			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	750			ns	and C_L = 100pF.
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	200			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

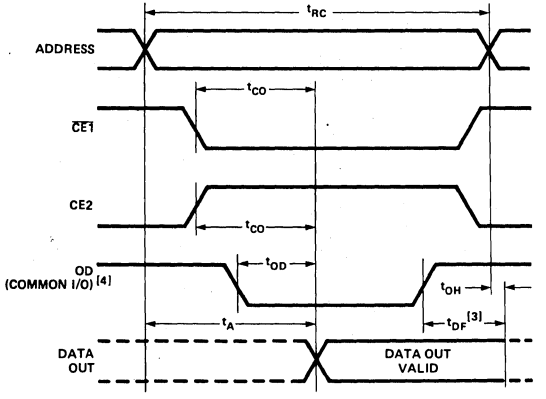
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[2] $T_A = 25°C$, f = 1MHz

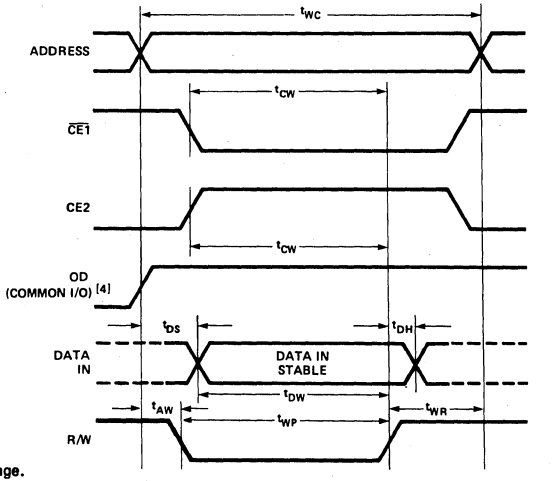
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

Waveforms

READ CYCLE



WRITE CYCLE



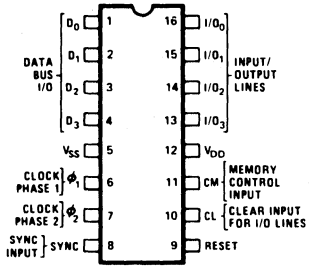
NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.
4. OD should be tied low for separate I/O operation.

256 x 8 MASK PROGRAMMABLE ROM AND 4 BIT I/O PORT

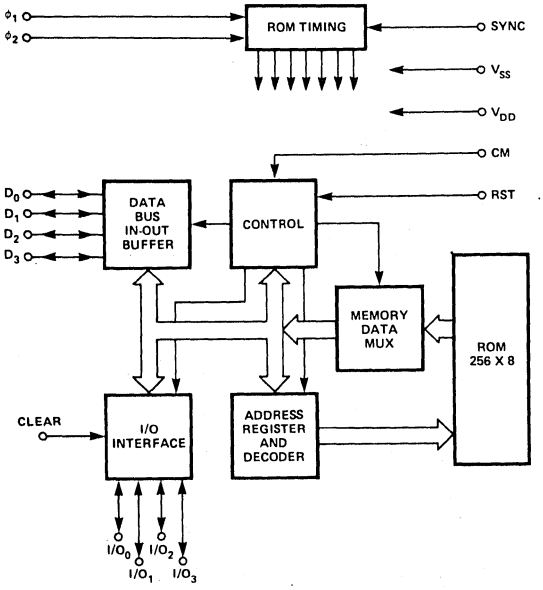
- **Direct Interface to MCS-40™ 4 Bit Data Bus**
- **I/O Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available With -40° to +85°C Operating Range**

The 4001 performs two basic and distinct functions. As a ROM it stores 256 x 8 words of program or data tables; as a vehicle of communication with peripheral devices it is provided with 4 I/O pins and associated control logic to perform input and output operations. The 4001 is a PMOS device, compatible with all other MCS-40™ devices.

PIN CONFIGURATION



BLOCK DIAGRAM



MCS-40

Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0 -D_3/Neg.	Bidirectional data bus. All address and data communication between the processor and ROM is handled by these lines.
5	V_{SS}	Most positive supply voltage.
6-7	$\phi 1$, $\phi 2$/Neg.	Non-overlapped clock signals which determine device timing.
8	SYNC/Neg.	System synchronization signal generated by processor.
9	RESET/Neg.	Reset input. A negative level (V_{DD}) on this pin will clear internal flip-flops and buffers. The input buffers are not cleared by this signal.
10	CL/Neg.	Clear input for I/O lines. A negative level on this pin will clear the I/O buffers. This pin may be driven by a TTL output and a 1K pull-up to V_{SS}.
11	CM-ROM/Neg.	Chip enable generated by the processor.
12	V_{DD}	Main supply voltage value. Must be V_{SS} – 15.0V ±5%.
13-16	I/O_0-I/O_3/Neg.	A single I/O port consisting of 4 bidirectional and selectable lines.

Functional Description

Address and data are transferred in and out by time multiplexing on 4 data bus lines. Timing is internally generated using two clock signals, ϕ_1 and ϕ_2, and a SYNC signal supplied by the CPU. Addresses are received from the CPU on three time periods following SYNC, and select 1 out of 256 words and 1 out of 16 ROM's. For that purpose, each ROM is identified as #0, 1, 2, through 15, by metal option. A Command ROM Line (CM-ROM) is also provided and it is used to select a ROM bank (group of 16 ROM's).

During the two time periods of the instruction cycle (M_1 & M_2) following the addressing time, information is transferred from the ROM to the data bus lines.

A second mode of operation of the ROM is as an Input/Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O external lines. Each chip has the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction. An external signal (CL) will asynchronously clear the output register during normal operation.

All internal flip flops (including the output register) will be reset when the RESET line goes low (V_{DD}).

I/O Options

Each I/O pin on each ROM can be uniquely chosen to be either an input or output line by metal option. Also each input or output can either be inverted or direct. When the pin is chosen as an input it may have an on-chip resistor connected to either V_{DD} or V_{SS}.

Instruction Execution

The 4001 responds to the following instructions.

1. **SRC Instruction** (Send address to ROM and RAM)

   When the CPU executes an SRC instruction it will send out 8 bits of data during X_2 and X_3 and will activate the CM-ROM and one CM-RAM line at X_2. Data at X_2, (representing the contents of the first register of the register pair addressed by the SRC instruction) with simultaneous presence of CM-ROM, is interpreted by the 4001 as the chip number of the unit that should later perform an I/O operation. Data at X_3 is ignored.

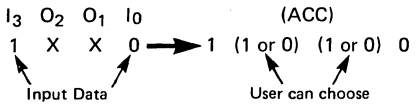
2. **WRR – Write ROM Port**

   The content of the accumulator is transferred to the ROM output port of the previously selected ROM chip. The data is available on the output pins until a new WRR is executed on the same chip. The ACC content and carry/link are unaffected. (The LSB bit of the accumulator appears on I/O_0.) No operation is performed on I/O lines coded as inputs.

3. **RDR – Read ROM Port**

   The data present at the input lines of the previously selected ROM chip is transferred to the accumulator.

   If the I/O option has both inputs and outputs within the same 4 I/O lines, the user can choose to have either "0" or "1" transferred to the accumulator for those I/O pins coded as outputs, when an RDR instruction is executed. For example, given a port with the I/O lines coded with 2 inputs and 2 outputs, when RDR is executed, the transfer is as shown below:



Timing Consideration

In the ROM mode of operation the 4001 will receive an 8 bit address during A_1 and A_2 times of the instruction cycle and a chip number, together with CM-ROM, during A_3 time. When CM-ROM is present, only the chip whose metal option code matches the chip number code sent during A_3 is allowed to send data out during the following two cycles: M_1 and M_2. The activity of the 4001 in the ROM mode ends at M_2.

The 4001 can have a chip number via the metal option from 0 – 15.

In the I/O mode of operation, the selected 4001 (by SRC), after receiving RDR will transfer the information present at its I/O pins to the data bus at X_2. If the instruction received was WRR, the data present on the data bus at $X_2 \cdot \phi_2$ will be latched on the output flip-flops associated with the I/O lines.

Ordering Information

When ordering a 4001, the following information must be specified:

1. Chip number
2. All the metal options for *each* I/O pin.
3. ROM pattern to be stored in each of the 256 locations.

A blank customer truth table is available upon request from Intel. A copy of this table is shown and blank copy can be found following the detailed 4001 characteristics.

EXAMPLES – DESIRED OPTION/CONNECTIONS REQUIRED

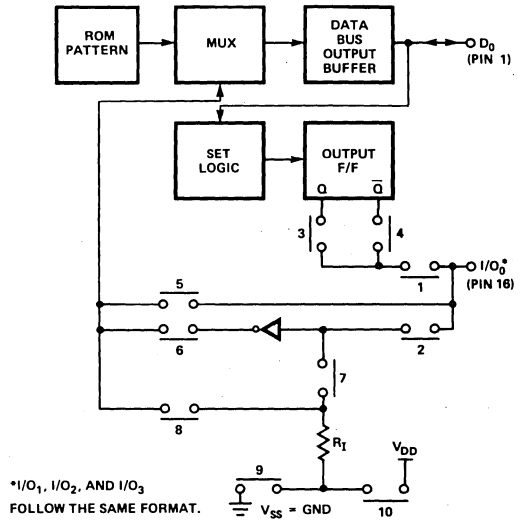
1. Non-inverting output (negative logic output) – 1 and 3 are connected.
2. Inverting output (positive logic output) – 1 and 4 are connected.
3. Non-inverting input (no input resistor – negative logic input) – only 5 is connected.
4. Inverting input (input resistor to V_{SS} – positive logic input) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD} – negative logic input) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and 2 non-inverting outputs the connection would be made as follows:

   Inputs – 2 and 6 are connected
   Outputs – 1, 3, 8 and 9 are connected or
   1, 3, 8 and 10 are connected

   If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

It should be noted that all internal logic and processing is performed in negative logic, i.e., "1" equals V_{DD} and "0" equals V_{SS}. For positive logic conversion, the inverted options should be selected.

TTL compatibility is obtained by $V_{DD} = -10V \pm 5\%$ and $V_{SS} = 5V \pm 5\%$. An external 12K resistor should be used on all outputs to insure the logic "0" state (V_{OL}).



4001 Available Metal Option for Each I/O Pin.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

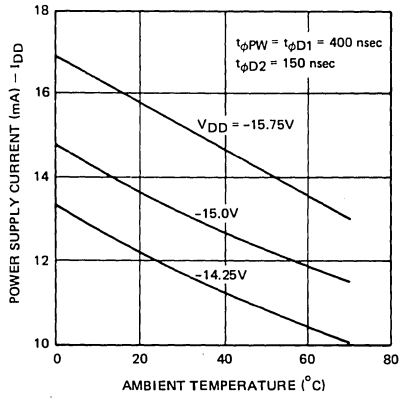
SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		15	30	mA	T_A = 25°C
INPUT CHARACTERISTICS – ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS – ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT} = V_{SS} -.5V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage, Inverting Input	V_{DD}		V_{SS}-4.2	V	
V_{IL}	Input Low Voltage, Non-inverting Input	V_{DD}		V_{SS}-6.5	V	
V_{IL}	CL Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
R_I	Input Resistance, if Used	10	18	35	kΩ	R_1 tied to V_{SS}; V_{IN} = V_{SS} -3V
R_1[1]	Input Resistance, if Used	15	25	40	kΩ	R_1 tied to V_{DD}; V_{IN} = V_{SS} -3V
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance		1.2	2	kΩ	V_{OUT} = V_{SS} -.5V
I_{OL}	I/O Output "1" Sink Current	2.5	5		mA	V_{OUT} = V_{SS} -.5V
I_{OL}[2]	I/O Output "1" Sink Current	0.8	3		mA	V_{OUT} = V_{SS} -4.85V
V_{OL}	I/O Output Low Voltage	V_{SS}-12		V_{SS}-6.5	V	I_{OUT} = 50μA
CAPACITANCE						
C_ϕ	Clock Capacitance		8	15	pF	V_{IN} = V_{SS}
C_{DB}	Data Bus Capacitance		9.5	15	pF	V_{IN} = V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN} = V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN} = V_{SS}

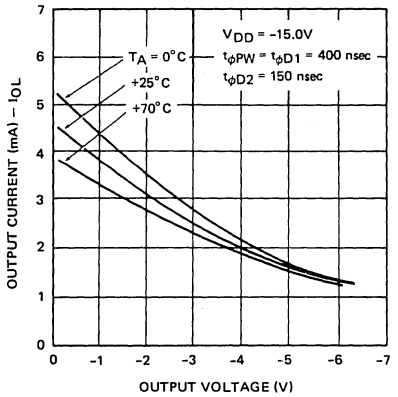
Notes: 1. R_I is large signal equivalent resistance to (V_{SS}-12) V.
2. For TTL compatibility, use 12kΩ external resistor to V_{DD}.

Typical D.C. Characteristics

POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{SS} - V_{DD} = 15V \pm 5\%$

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Times			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{IS}	I/O Input Set-Time	50			ns	
t_{IH}	I/O Input Hold-Time	100			ns	
t_D	I/O Output Delay			1500	ns	C_{OUT} = 100pF
t_C[4]	I/O Output Lines Delay on Clear			1500	ns	C_{OUT} = 100pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. CL on the 4001 is used to asynchronously clear the output flip-flops associated with the I/O lines.

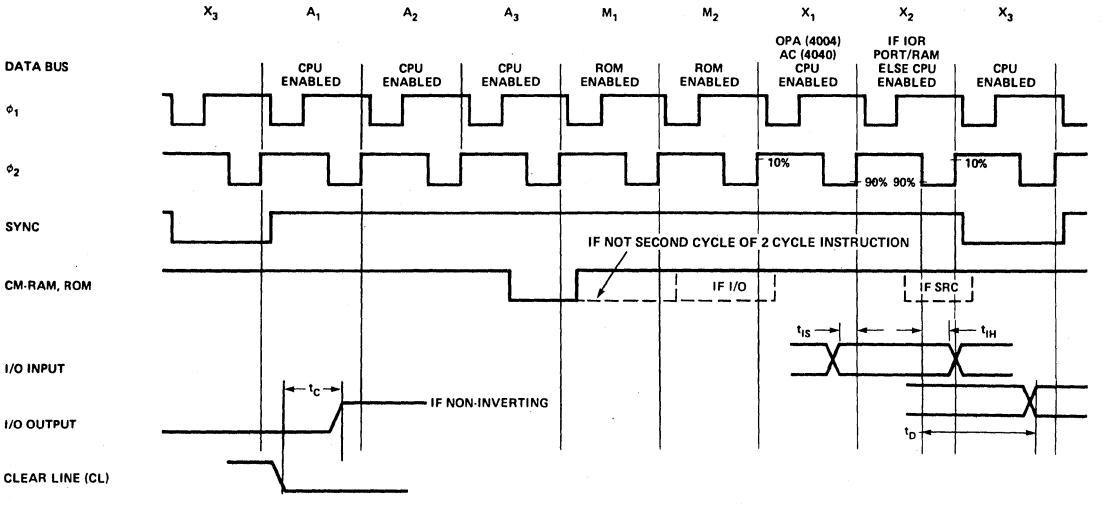


Figure 1. Timing Diagram

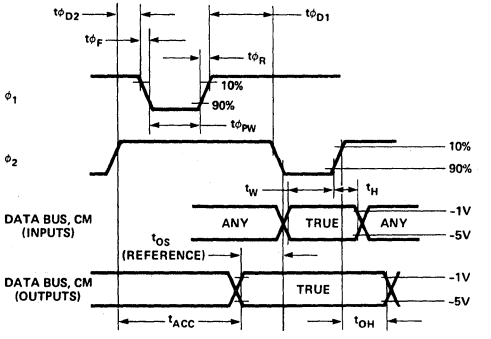


Figure 2. Timing Detail

Programming Instructions

To insure optimum handling of ROM programs and avoid delays, programs should be specified in the following format.

Paper Tape Format*

A 1" wide paper tape using 8 bit ASCII code, such as a model 33ASR teletype produces:

A. Preamble

1. Preceding the first word field and following the last word field, there should be a leader/trailer length of at least 25 characters. This should consist of rubout punches.

2. Included in the tape before the leader, and preceded by another leader, should be the customer's complete telex or twx number and if more than one pattern is being transmitted, the ROM pattern number.

3. The first ROM pattern preamble field is the device type number or ROM number. The field should be framed by an "I" and "–"

   I4001–

   This should be followed by the chip select information encoded in decimal (two digits), and enclosed by "C" and "S", as in

   "ChhS"

   The valid select digits for the 4001 are 0–15

   "C0S" – "C15S"

   Finally, the I/O options would be specified on a port-by-port basis with the connections to be made separated by commas, and enclosed in parentheses:

   "(n1, n2, n3 . . .)".

   where (n1, n2 . . .) are the option numbers associated with one I/O line. Hence, for a 4001 there will be four bracketed collections of I/O options.

   Each I/O pin has a series of 10 possible connections. These connections are consecutively numbered from 1-10. It is these numbers that should be in parentheses for each I/O pin.

   Example: "( )" indicates no connection
   "(1)" indicates only #1
   "(2,5,7)" indicates connections #2, 5 and 7.

   I/O options should be placed on the tape sequentially for the 4001 from I/O0–I/O3(4). Always avoid illegal combinations.

NOTE: Cards may also be submitted.

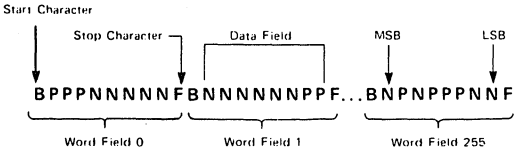
B. ROM Code

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.

2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F. Within the word field, a P results in a high level output (V_{SS} or logic 0 for MCS-40 CPUs) and a N results in a low level output (V_{DD} or logic 1 for MCS-40 CPUs).

Example of 256 x 8 format (N=256):



3. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. It may be helpful to insert the word number (as a comment) at least every four word fields.

4. Within the ROM pattern words a character, "X", may be used. Where "P" and "N" indicate a "0" and "1" setting respectively, an "X" will indicate a single bit – "Don't Care" setting. This allows the optimum default bit values to be selected by Intel. The bit value will be fixed to allow for testing. The values will be specified to the user on the Verification Listing tape.

   In the place of a standard BPNF word, a "B*nF" word may be used. This indicates that the data in the last BPNF word encountered is to be repeated for the next n words ($1 \leq n \leq 1023$). Note that if a repeat count of 4 is given in word position 10, then words 10, 11, 12, and 13 will be repeats of word 9 (except for Don't Care bits which might conceivably have different assigned values).

   To indicate that an entire block (such as the remainder of a ROM) is not used (i.e., Don't Care), a word of Don't Care data can be followed by the remaining word count in a repeat count form.

MCS® CUSTOM ROM ORDER FORM

4001 ROM

CUSTOMER_____

P.O. NUMBER_____

DATE_____

For Intel use only

S#_____ PPPP_____

STD_____ ZZ_____

_____ DD_____

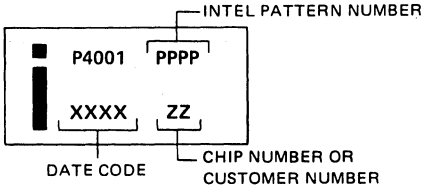
APP_____ DATE_____

All custom 4001 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4001), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).

CUSTOMER NUMBER _____



MCS-40

MASK OPTION SPECIFICATIONS

A. CHIP NUMBER _____.
(Must be specified—any number from 0 through 15—DD).

B. I/O OPTION – Specify the connection numbers for each I/O pin (next page). Examples of some of the possible I/O options are shown below:

EXAMPLES – DESIRED OPTION/CONNECTIONS REQUIRED

1. Non-inverting output – 1 and 3 are connected.
2. Inverting output – 1 and 4 are connected.
3. Non-inverting input (no input resistor) – only 5 is connected.
4. Inverting input (input resistor to V_{SS}) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD}) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and two non-inverting outputs, the connection would be made as follows:

   Inputs – 2 and 6 are connected
   Outputs – 1, 3, 8, and 9 are connected or
   1, 3, 8, and 10 are connected

   If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

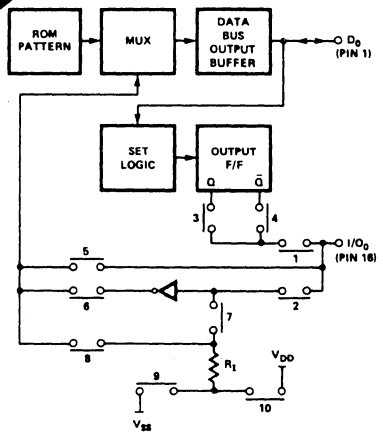
C. 4001 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Based on the particular customer pattern, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

Note that:

NOP = BPPPP PPPPF = 0000 0000

4001 I/O Options

SAMPLE

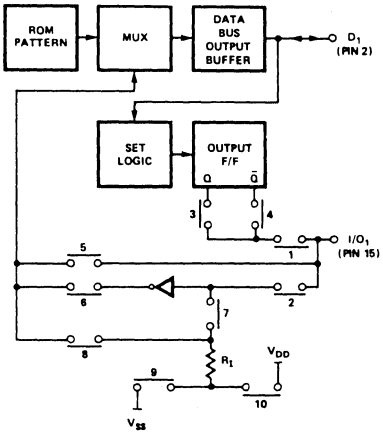


I/O_0 (PIN 16)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

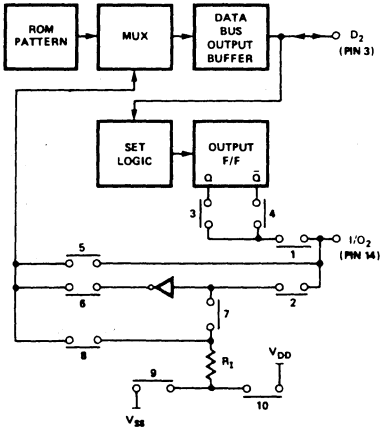


I/O_1 (PIN 15)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

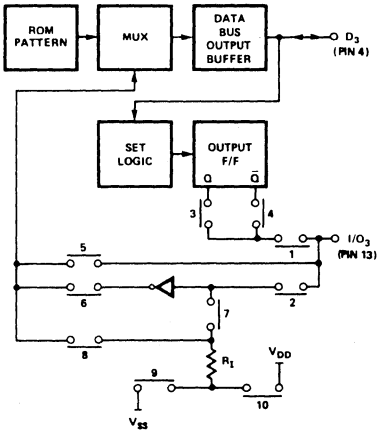


I/O_2 (PIN 14)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).



I/O_3 (PIN 13)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

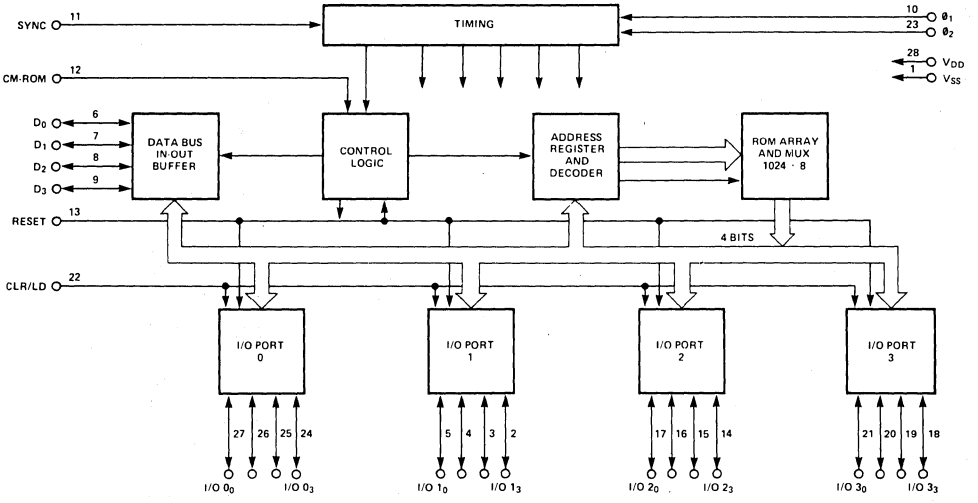
b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

1024 x 8 MASK PROGRAMMABLE ROM AND FOUR 4-BIT I/O PORTS

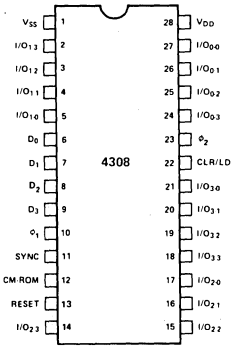
- **Direct Interface to MCS-40™ 4-Bit Data Bus**
- **Equivalent to Four 4001 ROMs**
- **Four Independent 4-Bit I/O Ports**
- **Input I/O Buffer Storage with an Optional Strobe**
- **I/O Ports Low-Power TTL Compatible**
- **28 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4308 is a 1024 x 8 bit word ROM memory with four I/O ports. It is designed for the MCS-40™ system and is operationally compatible with all existing MCS-40 elements. The 4308 is functionally identical to four 4001 chips. The 4308 has 16 I/O lines arranged in four groups of four lines.

BLOCK DIAGRAM



PIN CONFIGURATION



Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
1	V_{SS}	Most positive supply voltage.
2-5 14-17 18-21 24-27	$I/O1_3$-$I/O1_0$/Neg. $I/O2_3$-$I/O2_0$/Neg. $I/O3_3$-$I/O3_0$/Neg. $I/O0_3$-$I/O0_0$/Neg.	Four I/O ports consisting of 4 bidirectional and selectable lines.
6-9	D_0-D_3/Neg.	Bi-directional data bus. All information between processor and device is transmitted to these four pins.
10, 23	$\phi1$, $\phi2$/Neg.	Non-overlapped clock signals which determine device timing.
11	SYNC/Neg.	System synchronization signal generated by processor.
12	CM-ROM/Neg.	Chip enable generated by the processor.
13	RESET/Neg.	Reset input. A negative level (V_{DD}) on this pin will clear internal flip-flops and buffers. The input buffers are not cleared by this signal.
22	CLR/LD/Neg.	Clear/Load input. This pin is a dual function pin. It may be selected as a common Clear for those pins selected as output pins or as a Load for those pins selected as input pins. This pin should be designated for one purpose only per 4308, either Clear or Load. As a Load, a positive (V_{SS}) to negative (V_{DD}) transition will cause the I/O data to be placed in the input latch. A negative to positive transition will cause the data to be latched. The I/O pin state may be altered without changing the contents of the latch when the line is positive. As a Clear, a negative level (V_{DD}) on this line will cause the designated output latches to clear and remain cleared until a positive level (V_{SS}) is placed on the line. This line may be driven by a TTL output with a 1K pull-up resistor to V_{SS}.
28	V_{DD}	Main supply voltage. Value must be V_{SS} -15V ±5%.

Functional Description

The 4308 ROM program memory is arrayed 1024 x 8 bit words. For the program memory mode of operation, the A1 —A3 time periods of the instruction cycle are used to address the ROM contents. The 4308 decodes the first ten bits of the address to select 1 out of the 1024 words, 8 bits wide. The remaining two bits select a particular 4308, which has one of four possible metal option chip select addresses. Instruction information is available in two 4-bit segments during M_1 and M_2 time periods. A 4004 system can accommodate up to four 4308's while a 4040 system can utilize up to eight devices.

A second mode of operation of the ROM is as an Input/Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O external lines. Each chip has the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction.

All internal flip flops (including the output register) will be reset when the RESET line goes low (negative voltage).

Each of the four I/O ports of a 4308 are program selectable. Each of the four lines can be specified as either inputs or outputs via a metal mask option. A complete description of the I/O option capabilities are given below. The 4308 has an input storage buffer for utilization with those I/O pins designated as inputs. A common strobe line (CLR/LD line) allows the asynchronous loading of data from the I/O lines. The same CLR/LD strobe line can also serve as a clear to the I/O output port buffers when designated. This CLR/LD line is common to all ports on a 4308 and when toggled, will effect those I/O lines connected by the metal mask option. For an input line, if the CLR/LD strobe line is left unconnected, or if it is pulled to (V_{DD}), then the output of the buffer will follow the input.

NOTE: Since the 4308 is compatible with all components of the MCS-40 system, 4308 and 4001 can be mixed on one memory bank as long as the chip select addresses are mutually exclusive.

The following table shows the chip number relationship between 4308 and 4001.

4308		4001	
Page No.	Chip No.	Page No.	Chip No.
0-3	(0)	0-15	0-15
4-7	(1)		
8-11	(2)		
12-15	(3)		

INSTRUCTION EXECUTION

The 4308 responds to the following instructions.

1. **SRC Instruction** (Send address to ROM and RAM)

   When the CPU executes an SRC instruction it will send out 8 bits of data during X_2 and X_3 and will activate the CM-ROM and one CM-RAM line at X_2. Data at X_2 (representing the contents of the first register of the register pair addressed by the SRC instruction), with simultaneous presence of CM-ROM, is interpreted by the 4308 as the chip number of the unit that should later perform an I/O operation. Data at X_3 is ignored. After an SRC only one CM-ROM and CM-RAM device will be selected.

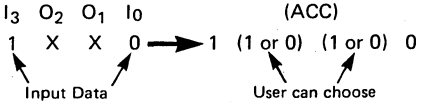
2. **WRR – Write ROM Port**

   The content of the accumulator is transferred to the ROM output port of the previously selected ROM chip. The data is available on the output pins until a new WRR is executed on the same chip. The ACC content and carry/link are unaffected. (The LSB bit of the accumulator appears on I/O_0.) No operation is performed on I/O lines coded as inputs.

3. **RDR – Read ROM Port**

   The data present at the input lines of the previously selected ROM chip is transferred to the accumulator.

   If the I/O option has both inputs and outputs within the same 4 I/O lines, the user can choose to have either "0" or "1" transferred to the accumulator for those I/O pins coded as outputs, when an RDR instruction is executed. For example, given a port with the I/O lines coded with 2 inputs and 2 outputs, when RDR is executed the transfer is as shown below:



Timing Considerations

At the beginning of each instruction sequence, a SYNC pulse is generated externally to synchronize the processor with the various components of the system. This pulse, along with the clock inputs ϕ_1 and ϕ_2, is used in the 4308 as an input to a timing register.

During time A_1, A_2, and A_3, the address is sequentially accepted from the data bus and decoded. During time A_3, the CM-ROM line will be active, and if the 2 highest order bits of the address sent at A_3 match the metal preprogrammed chip select option, the ROM will respond to the current address.

At time M_1 and M_2, the instruction OPR, OPA will be placed on the data bus for the processor.

After the SRC or Send Register Control instruction, which is used to designate a set of 4 I/O lines (1 port) on a particular ROM which are to be used for subsequent ROM I/O operations, is executed by the processor, the processor sends a 4 bit code to the ROM during X_2, and CM-ROM goes to a "1" (V_{DD}). The first two bits (D_3, D_2) of this code select a group of 1 out of 4 possible 4308, and the last two bits select a particular port (1 of 4 ports). This port remains selected until the next SRC instruction is executed.

In both the RDR and WRR operations, the CM-ROM line will become active during time M_2, and if the ROM has a previously selected I/O port, it will respond to the I/O in two ways. For a WRR accumulator, data will be transferred to an internal ROM selected output port flip-flops during X_2. Data will be available on the I/O line from time $X_3 \cdot \overline{\phi_2}$. The data will remain on the bus until a new WRR occurs, a reset occurs, or a clear (CLR/LD line) is generated. The RDR instruction will transfer information from the input port flip-flops of a previously selected port. Prior to RDR instruction, the user should insure that the input flip-flops have been loaded via the CLR/LD strobe if the load strobe is specified. If the load strobe is not specified, information on the input lines will be loaded into the accumulator at the time of the RDR.

I/O OPTIONS

The 4308 offers the following options on its I/O pins:

1. Input or output.
2. Inverted or direct (for input and output).
3. On-chip resistor connected to either V_{SS} or V_{DD} for input pins.
4. Asynchronous loading of input buffers via the CLR/LD signal.
5. Clear signal for any or all output ports via the CLR/LD signal.

Referring to the block diagram of the single I/O pin shown below which illustrates the various options available on a 4308, it should be noted that certain pin combinations are mutually exclusive and should not be specified together. There are also certain invalid combinations. The following combinations should be avoided:

8,9
5,6
3,4
10,11 – Both on a single pin and within a single 4308.

Examples of some common desired option/connections are:

a. *I/O pin inputs**

non-inverting	11, 2, 5, 7, 9 (TTL) – 2, 5, 7, 8
inverting	11, 2, 6, 7, 9 (TTL) – 2, 6, 7, 8

b. *I/O pin outputs*

non-inverting	3, 1 (10 optional)
inverting	4, 1 (10 optional)

Other combinations exist and should be used with caution.

**Option 11 need not be specified if an unbuffered input is desired. This is equivalent to a 4001 input.*

NOTE: The 4308 has the following enhancements over the 4001 as far as I/O options are concerned:

1. The capability of clearing any or all outputs with the CLR/LD signal.
2. TTL compatibility of both the inverting and non-inverting input paths for input ports.
3. The capability to select the LD option and have the input buffer become an input flip-flop and to have the CLR/LD signal become an asynchronous clock for loading data.

For TTL compatibility on the I/O lines, the supply voltage should be V_{DD} = -10V ±5%, V_{SS} = +5V ±5%. External pull-up is required for outputs.

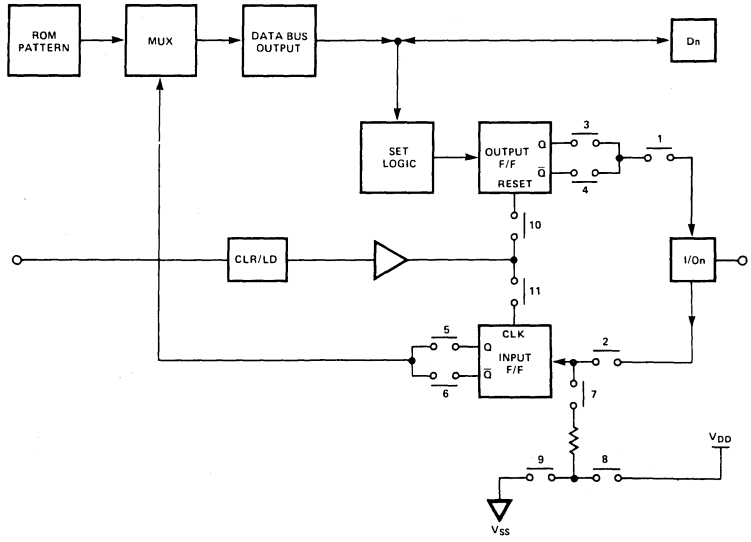


Figure 1. 4308 I/O Pin Options.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		20	40	mA	T_A = 25°C
INPUT CHARACTERISTICS (ALL INPUTS EXCEPT I/O PINS)						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	CLR/LD pin
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS – ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		200	300	Ω	V_{OUT} = V_{SS} -.5V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
V_{IL}	CLR/LD Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
R_I	Input Resistance, if Used	10	18	35	kΩ	R_I tied to V_{SS}; V_{IN} = V_{SS} -3V
R_I[1]	Input Resistance, if Used	15	25	40	kΩ	R_I tied to V_{DD}; V_{IN} = V_{SS} -3V
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance		1.2	2	kΩ	V_{OUT} = V_{SS} -.5V
I_{OL}	I/O Output "1" Sink Current	2.5	5		mA	V_{OUT} = V_{SS} -.5V
I_{OL}[2]	I/O Output "1" Sink Current	0.8	3		mA	V_{OUT} = V_{SS} -4.85V
I_{CF}	I/O Output "1" Clamp Current			4	mA	V_{OUT} = V_{SS} -6V; T_A = 70°C
V_{OL}	I/O Output Low Voltage	V_{SS}-12		V_{SS}-6.5	V	I_{OUT} = 50μA

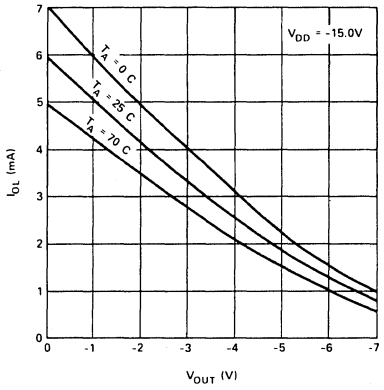
Notes: 1. R_I is large signal equivalent resistance to (V_{SS} -12) V.
2. For TTL compatability, use 12kΩ external resistor to V_{DD}.

D.C. and Operating Characteristics

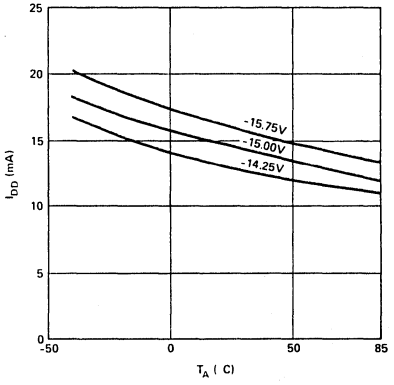
CAPACITANCE

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
C_ϕ	Clock Capacitance		14	20	pF	$V_{IN} = V_{SS}$
C_{DB}	Data Bus Capacitance		7	10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance			10	pF	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance			10	pF	$V_{IN} = V_{SS}$

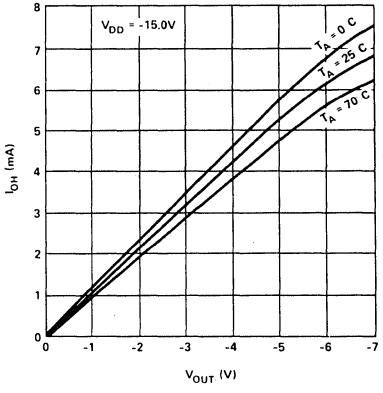
4308 OUTPUT PINS ("1" LEVEL)



4308 SUPPLY CURRENT VS. TEMPERATURE



4308 OUTPUT PINS ("0" LEVEL)



A.C. Characteristics

T_A = 0°C to 70°C, V_{SS} -V_{DD} = 15V ±5%

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Time			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines[4]
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{IS}	I/O Input Set-Time	50			ns	
t_{IH}	I/O Input Hold-Time	100			ns	
$t_{PW\ I/O}$	C/L Pulse-Width	1000	400		ns	
$t_{W\ C/L}$	C/L Write Time	350	200		ns	
$t_{H\ C/L}$	C/L Hold Time	100			ns	
t_D	I/O Output Delay			1500	ns	C_{OUT} = 100pF
t_C[5]	I/O Output Delay on C/L		750	1500	ns	C_{OUT} = 100pF
$t_{W\ \phi 2F}$[6]	Data In Write Time with Respect to ϕ_2	-30	-60		ns	

Notes:
1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. t_{ACC}, 4308 is guaranteed with $t_{\phi D2}$ = 200 nsec.
5. C/L Clears output buffer when low. C/L enters data into input buffer when low. C/L rising edge latches input buffer. Port Option 10 and 11 are mutually exclusive on any 4308.
6. Data Bus Inputs are guaranteed valid before ϕ_2 falling edge by 4004, 4040 t_{ACC}. If $t_{PW\phi 2}$ is widened, then t_{CY} is increased and Data Bus Inputs remain valid before ϕ_2 falling edge. Thus, $t_{W\phi 2F}$ is not a system constraint.

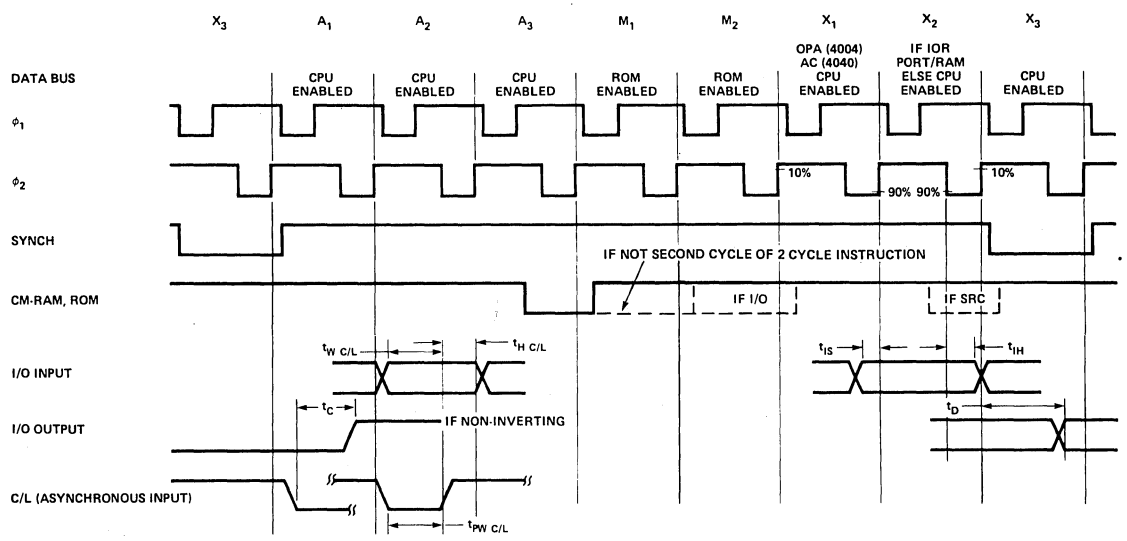


Figure 2. Timing Diagram.

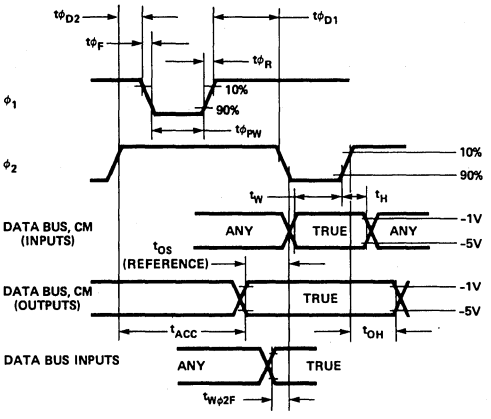


Figure 3. Timing Detail.

Programming Instruction

To insure optimum handling of ROM programs and avoid delays, programs should be specified in the following format.

Paper Tape Format*

A 1" wide paper tape using 8 bit ASCII code, such as a model 33ASR teletype produces:

A. Preamble

1. Preceding the first word field and following the last word field, there should be a leader/trailer length of at least 25 characters. This should consist of rubout punches.
2. Included in the tape before the leader, and preceded by another leader, should be the customer's complete telex or twx number and if more than one pattern is being transmitted, the ROM pattern number.
3. The first ROM pattern preamble field is the device type number or ROM number. The field should be framed by an "I" and "–"

   I4308–

   This should be followed by the chip select information encoded in decimal (two digits), and enclosed by "C" and "S", as in

   "ChhS"

   The valid select digits for the 4308 are 0–3

   "C0S" – "C3S"

   Finally, the I/O options would be specified on a port-by-port basis with the connections to be made separated by commas, and enclosed in parentheses:

   "(n1, n2, n3 . . .)".

   where (n1, n2 . . .) are the option numbers associated with one I/O line. Hence, for the 4308 there will be sixteen bracketed collections of I/O options.

   Each I/O pin has a series of 11 possible connections. These connections are consecutively numbered from 1-11. It is these numbers that should be in parentheses for each I/O pin.

   Example: "( )" indicates no connection
   "(1)" indicates only #1
   "(2,5,7)" indicates connections #2, 5 and 7.

   I/O options should be placed on the tape sequentially for the 4308, from $I/O0_0$ – $I/O3_3(16)$. Always avoid illegal combinations.

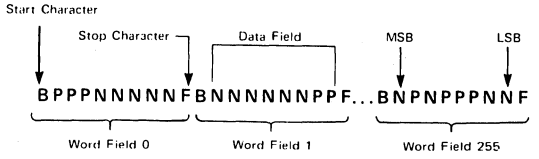
NOTE: Cards may also be submitted.

B. ROM Code

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F. Within the word field, a P results in a high level output (V_{SS} or logic 0 for MCS-40 CPUs) and a N results in a low level output (V_{DD} or logic 1 for MCS-40 CPUs).

Example of 256 x 8 format (N=256):



3. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. It may be helpful to insert the word number (as a comment) at least every four word fields.
4. Within the ROM pattern words a character, "X", may be used. Where "P" and "N" indicate a "0" and "1" setting respectively, an "X" will indicate a single bit – "Don't Care" setting. This allows the optimum default bit values to be selected by Intel. The bit value will be fixed to allow for testing. The values will be specified to the user on the Verification Listing tape.

   In the place of a standard BPNF word, a "B*nF" word may be used. This indicates that the data in the last BPNF word encountered is to be repeated for the next n words ($1 \leq n \leq 1023$). Note that if a repeat count of 4 is given in word position 10, then words 10, 11, 12, and 13 will be repeats of word 9 (except for Don't Care bits which might conceivably have different assigned values).

   To indicate that an entire block (such as the remainder of a ROM) is not used (i.e., Don't Care), a word of Don't Care data can be followed by the remaining word count in a repeat count form.

MCS® CUSTOM ROM ORDER FORM

4308 ROM

CUSTOMER _____

P.O. NUMBER _____

DATE _____

For Intel use only

S# _____ PPPP _____

STD _____ ZZ _____

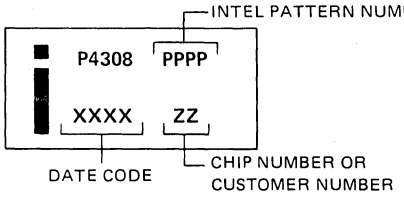
_____ DD _____

APP _____ DATE _____

All custom 4308 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4308), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).



CUSTOMER NUMBER _____

MASK OPTION SPECIFICATION

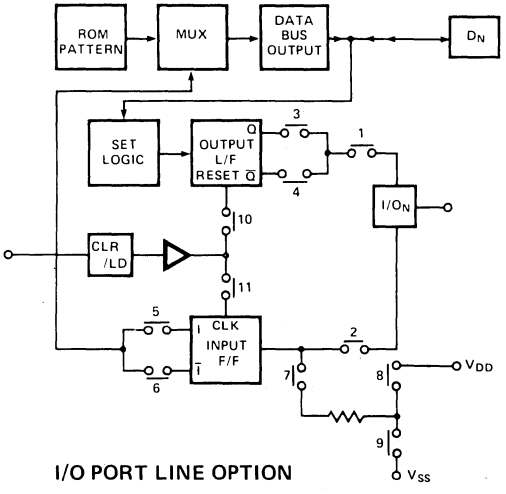
A. CHIP NUMBER _____ (Must be specified).

B. I/O OPTION – Specify the connection numbers for each I/O pin. See table below.

C. 4308 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Based on the particular customer pattern, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

Note that: NOP = BPPPP PPPPF = 0000 0000

PIN		OPTION										
I/O 0_0	27	1	2	3	4	5	6	7	8	9	10	11
I/O 0_1	26	1	2	3	4	5	6	7	8	9	10	11
I/O 0_2	25	1	2	3	4	5	6	7	8	9	10	11
I/O 0_3	24	1	2	3	4	5	6	7	8	9	10	11
I/O 1_0	5	1	2	3	4	5	6	7	8	9	10	11
I/O 1_1	4	1	2	3	4	5	6	7	8	9	10	11
I/O 1_2	3	1	2	3	4	5	6	7	8	9	10	11
I/O 1_3	2	1	2	3	4	5	6	7	8	9	10	11
I/O 2_0	17	1	2	3	4	5	6	7	8	9	10	11
I/O 2_1	16	1	2	3	4	5	6	7	8	9	10	11
I/O 2_2	15	1	2	3	4	5	6	7	8	9	10	11
I/O 2_3	14	1	2	3	4	5	6	7	8	9	10	11
I/O 3_0	21	1	2	3	4	5	6	7	8	9	10	11
I/O 3_1	20	1	2	3	4	5	6	7	8	9	10	11
I/O 3_2	19	1	2	3	4	5	6	7	8	9	10	11
I/O 3_3	18	1	2	3	4	5	6	7	8	9	10	11



I/O PORT LINE OPTION

NOTE: Options 10 and 11 cannot both be specified.

MCS-40

4316A

16,384 BIT STATIC MOS READ ONLY MEMORY

Organization: 2048 Words x 8 Bits
Access Time: 850 ns Max.

- **Single +5 Volts Power Supply Voltage**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Low Power Dissipation of 31.4 μW/Bit Maximum**
- **Three Programmable Chip Select Inputs for Easy Memory Expansion**
- **Three-State Output — OR-Tie Capability**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Interface to 4004/4040 CPU Via 4008/4009 or 4289 Standard Memory Interface**

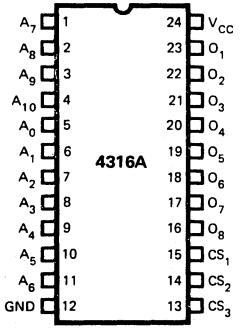
The Intel® 4316A is a 16,384-bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for microcomputer memory applications where high performance, large bit storage, and simple interfacing are important design objectives. It can be used in MCS-40 systems via the 4008/4009 or 4289 Standard Memory Interface component.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.

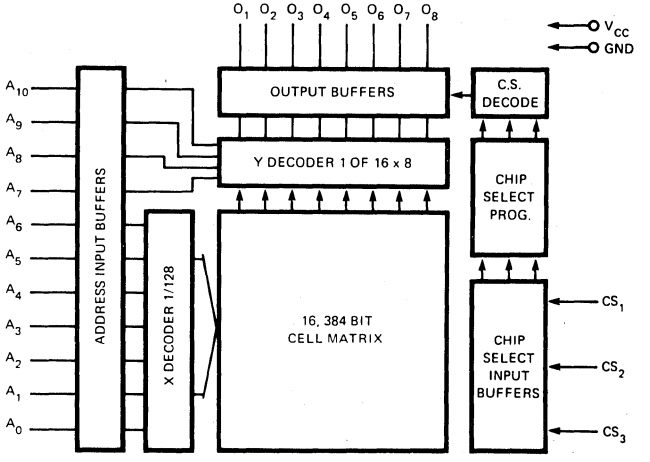
The 4316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

MCS-40

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0- A_{10}	ADDRESS INPUTS
O_1- O_8	DATA OUTPUTS
CS_1- CS_3	PROGRAMMABLE CHIP SELECT INPUTS

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect To Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	μA	CS = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			-20	μA	CS = 2.2V, V_{OUT} = 0.45V
I_{CC}	Power Supply Current		40	98	mA	All inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100 μA

(1) Typical values for T_A = 25°C and nominal supply voltage.

MCS-40

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_A	Address to Output Delay Time		400	850	nS
t_{CO}	Chip Select to Output Enable Delay Time			300	nS
t_{DF}	Chip Deselect to Output Data Float Delay Time	0		300	nS

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

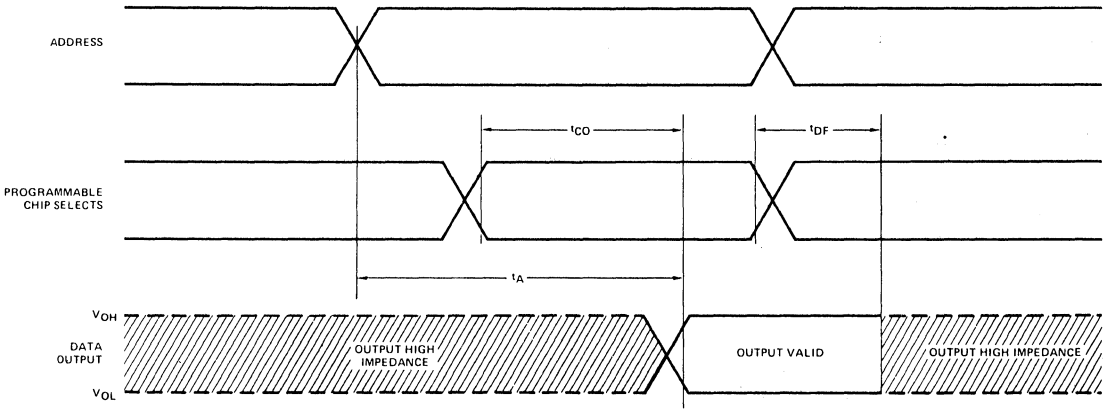
Output Load . . . 1 TTL Gate, and C_{LOAD} = 100 pF
Input Pulse Levels . . . . . 0.8 to 2.0V
Input Pulse Rise and Fall Times . (10% to 90%) 20 nS
Timing Measurement Reference Level
Input 1.5V
Output . . . . . 0.45V to 2.2V

Capacitance(2) T_A = 25°C, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

(2) This parameter is periodically sampled and is not 100% tested.

Waveforms


ADDRESS
t_{CO}
t_{DF}
PROGRAMMABLE CHIP SELECTS
t_A
V_{OH}
DATA OUTPUT
V_{OL}
OUTPUT HIGH IMPEDANCE
OUTPUT VALID
OUTPUT HIGH IMPEDANCE

REPROGRAMMABLE 2K PROM

- **Access Time: 1.7 usec Max.**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **Ultraviolet Erasable and Electronically Reprogrammable**
- **Fully Decoded, 256 x 8 Organization**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output: OR-Tie Capability**
- **Simple Memory Expansion Chip Select Input Lead**

The 4702A is a 256 word by 8 bit electrically programmable ROM ideally suited for microcomputer system development where fast turn-around and pattern experimentation are important. The 4702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

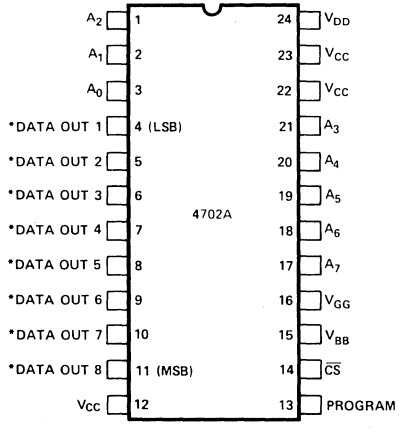
The 4702A is packaged in a 24 pin dual-in-line package with a transparent quartz lid. The transparent quartz lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. This procedure can be repeated as many times as required.

The circuitry of the 4702A is entirely static; no clocks are required.

A pin-for pin metal mask programmed ROM, the Intel® 1302A, is ideal for large volume production runs of systems initially using the 4702A.

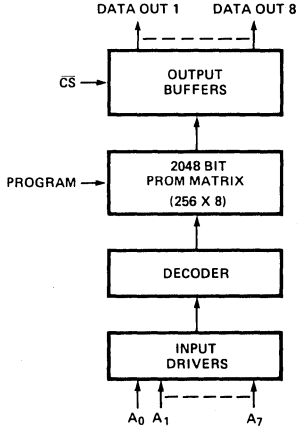
The 4702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING.

BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
DO_1- DO_2	DATA OUTPUTS

Pin Connections

The external lead connections to the 4702A differ, depending on whether the device is being programmed[1] or used in read mode. (See following table.)

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = -10V±5%, V_{GG} = -10V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DDO}	Power Supply Current		6	14	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC} −2, I_{OL} = 0.0mA, T_A = 25°C
I_{DD1}	Power Supply Current		39	54	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		36	50	mA	$\overline{CS}$=0.0, I_{OL} =0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		43	63	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
I_{GG}	Gate Supply Current			10	μA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC} −2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5			V	I_{OH} = −100 μA

Continuous Operation

Note 1: In the programming mode, the data inputs 1–8 are pins 4–11 respectively. $\overline{CS}$ = GND.
Note 2: Typical values are at nominal voltages and T_A = 25°C.

MCS-40

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = -10V ±5%, V_{GG} = -10V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay			1.7	μs
t_{CS}	Chip select delay			800	ns
t_{CO}	Output delay from $\overline{CS}$			900	ns
t_{OD}	Output deselect			300	ns

Capacitance* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		10	15	pF	

* This parameter is periodically sampled and is not 100% tested.

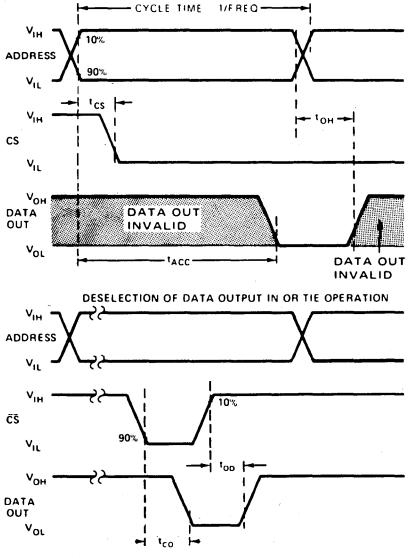
Switching Characteristics

Conditions of Test:

Input pulse amplitudes: 0 to 4V; t_R, $t_F \leqslant 50$ ns.

a) For output load = 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leqslant 15$ ns)

b) For pure capacitive load of 75pf.



MCS 4/40™ PROTOTYPE SYSTEMS

Intel distributors are now stocking two MCS-40 systems which may be used to prototype products and will make low volume manufacturing more economical. Additional prototype systems will be offered as newer microcomputer components are developed.

System Number — **System Composition**

MCS-4 System A — Prototype system for 4-bit Microcomputer with C4004 CPU. Each system includes:

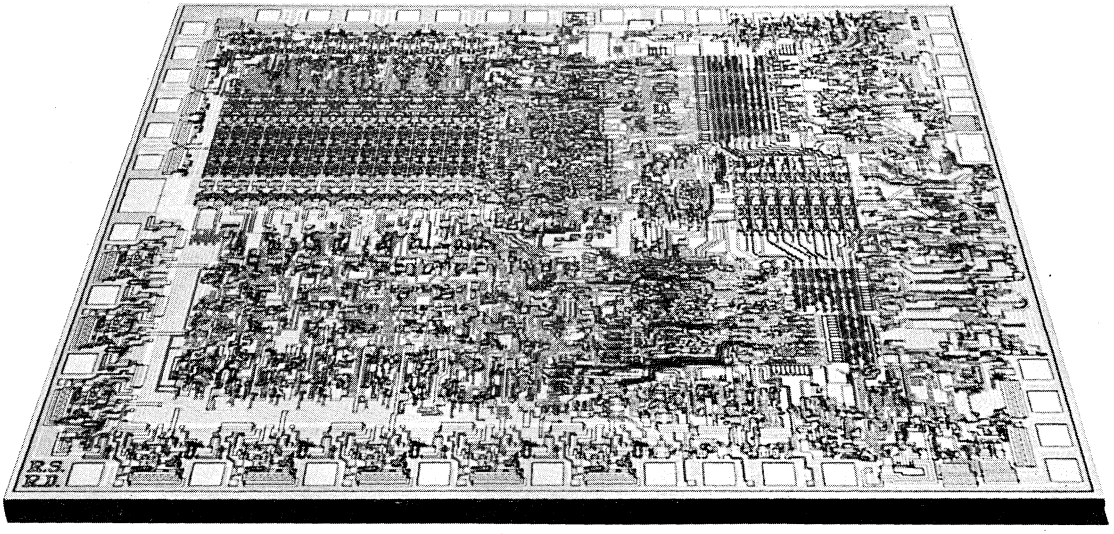
Quantity	Device
1	P4002-1
1	P4003
1	C4004
1	P4008
1	P4009
1	C4702A

MCS-40 System A — Prototype system for 4-bit Microcomputer with C4040 CPU. Each system includes:

Quantity	Device
1	P4002-1
1	P4003
1	C4040
1	P4201
1	P4289
1	C4702A

8

MCS-80™ MICROCOMPUTER SYSTEM



MCS-80™ MICROCOMPUTER SYSTEM

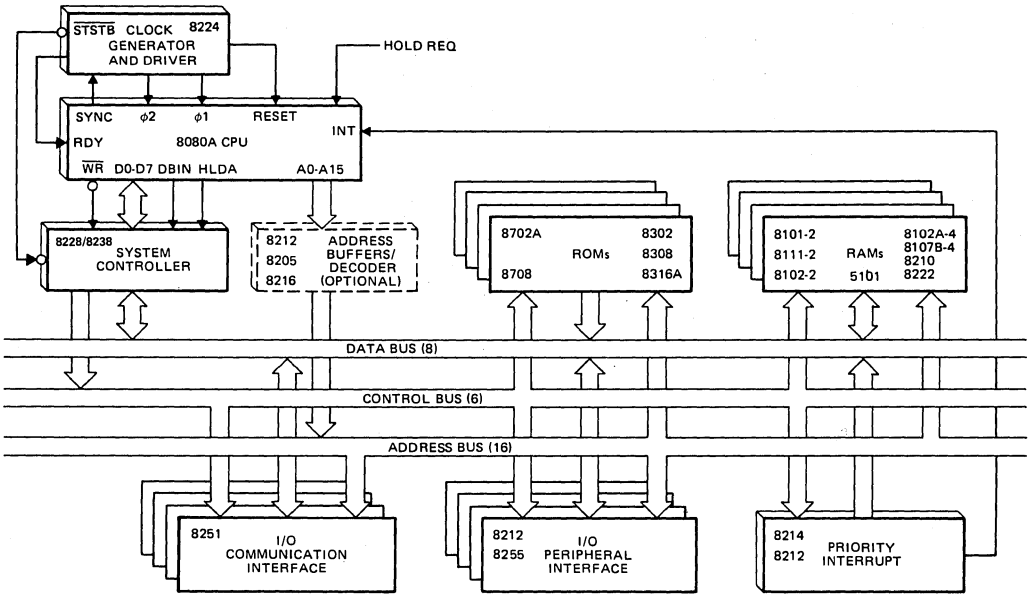
Type	Group	Description	Page No.
8080A	CPU	Central Processor	8-5
8080A-1	CPU	Central Processor (1.3μs)	8-12
8080A-2	CPU	Central Processor (1.5μs)	8-16
M8080A	CPU	Central Processor (–55° to +125°C)	8-20
8224	CPU	Clock Generator	8-25
8228/8238	CPU	System Controller	8-29
8008, 8008-1	CPU	Eight-Bit Microprocessor	8-33
8702A	ROMs	Erasable PROM (256 x 8)	8-40
8708	ROMs	Erasable 1K x 8 PROM	8-43
8302	ROMs	Mask ROM (256 x 8)	8-46
8308	ROMs	Mask ROM (1K x 8)	8-49
8316A	ROMs	Mask ROM (2K x 8)	8-52
8101-2	RAMs	Static RAM (256 x 4)	8-54
8101A-4	RAMs	Static RAM (256 x 4) 450 ns	8-57
8111-2	RAMs	Static RAM (256 x 4)	8-60
8111A-4	RAMs	Static RAM (256 x 4) 450 ns	8-63
8102A-4	RAMs	Static RAM (1K x 1) 450 ns	8-66
8107B-4	RAMs	Dynamic RAM (4K x 1)	8-69
8222	RAMs	Dynamic RAM Refresh Controller	8-74
8212	I/O	8-Bit I/O Port	8-75
8255	I/O	Programmable Peripheral Interface	8-79
8251	I/O	Programmable Communication Interface	8-85
8205	Peripherals	One of Eight Decoder	8-89
8214	Peripherals	Priority Interrupt Control Unit	8-92
8216/8226	Peripherals	4-Bit Bi-Directional Bus Driver	8-96
8253	Peripherals	Programmable Interval Timer	8-100
8257	Peripherals	Programmable DMA Controller	8-102
8259	Peripherals	Programmable Interrupt Controller	8-104

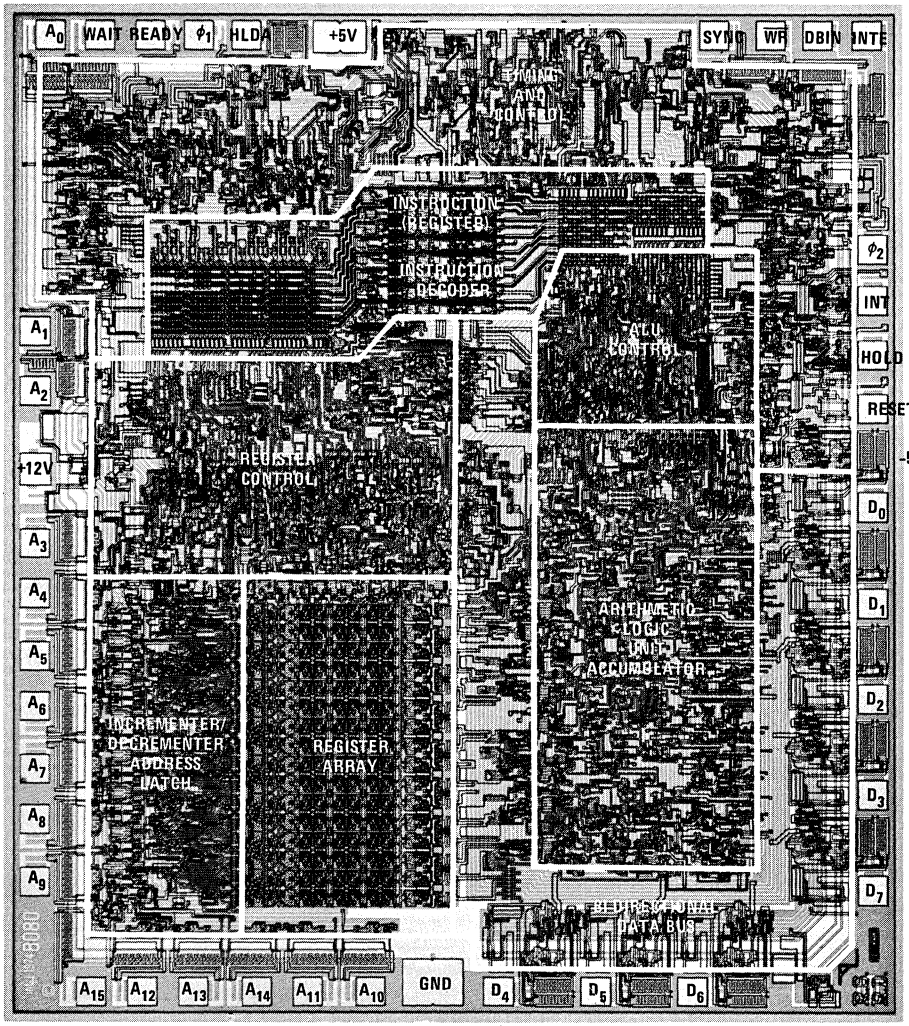
MCS-80™ MICROCOMPUTER SYSTEM

MCS-80™ components form complete systems with many optional configurations. They eliminate the problems of hardwired design by integrating control and processing functions in LSI blocks that interface with one another through a standard system bus.

The systems building blocks include:

- The basic CPU Group, which defines and drives the bus—the 8080A CPU, 8224 Clock Generator and 8228 System Controller.
- Three CPU options for higher speed and extended temperature range applications.
- Twelve I/O and peripherals options, five of which are programmable LSI devices that control and communicate with external equipment in software selectable modes.
- Memory options, including 8K erasable PROMs, 16K ROMs, low power 1K CMOS RAMs, and low cost 4K RAMs—all with industry standard configurations for ease of use and economy.





8080A CHIP PHOTOGRAPH WITH SECTIONAL DIVISIONS

8080A

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

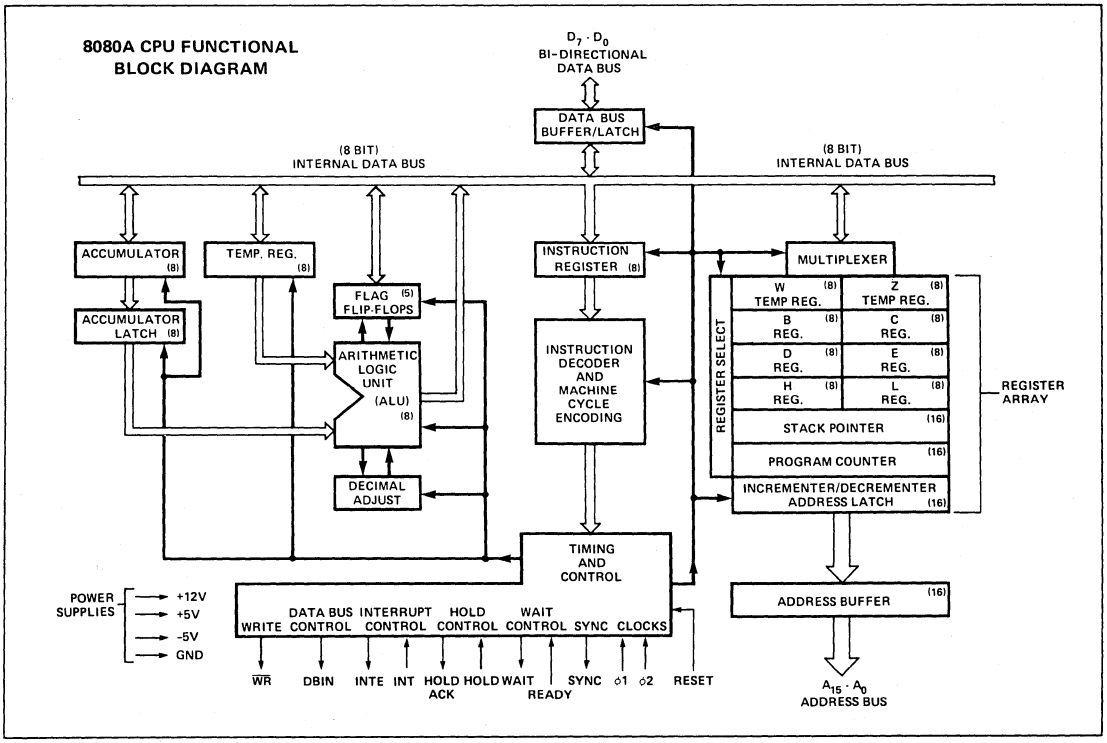
- **TTL Drive Capability**
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.



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8080A FUNCTIONAL PIN DEFINITION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A_{15}-A_0 (output three-state)
ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)
DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.

SYNC (output)
SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)
DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)
READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)
WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

$\overline{WR}$ (output)
WRITE; the $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0).

HOLD (input)
HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

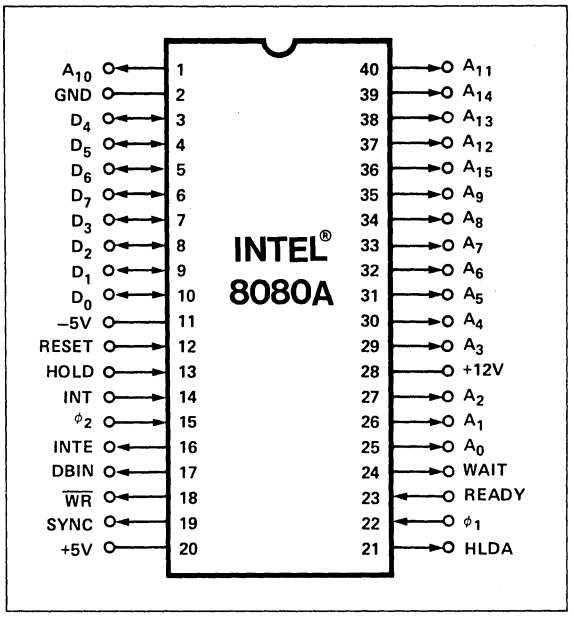
- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)
HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.



Pin Configuration

INTE (output)
INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)
INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input) [1]
RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS}	Ground Reference.
V_{DD}	+12 ± 5% Volts.
V_{CC}	+5 ± 5% Volts.
V_{BB}	-5 ±5% Volts (substrate bias).
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible)

MCS-80

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70° C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = -150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	T_{CY} = .48 μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}$ +0.8V V_{SS} +0.8V $\leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

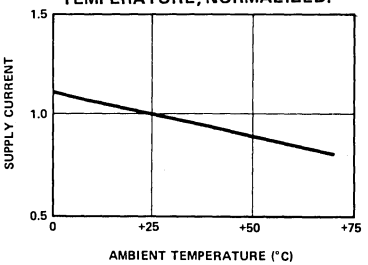
CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

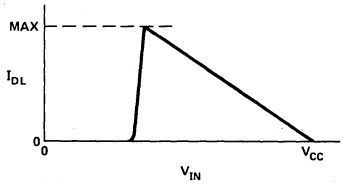
Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED.[3]



DATA BUS CHARACTERISTIC DURING DBIN



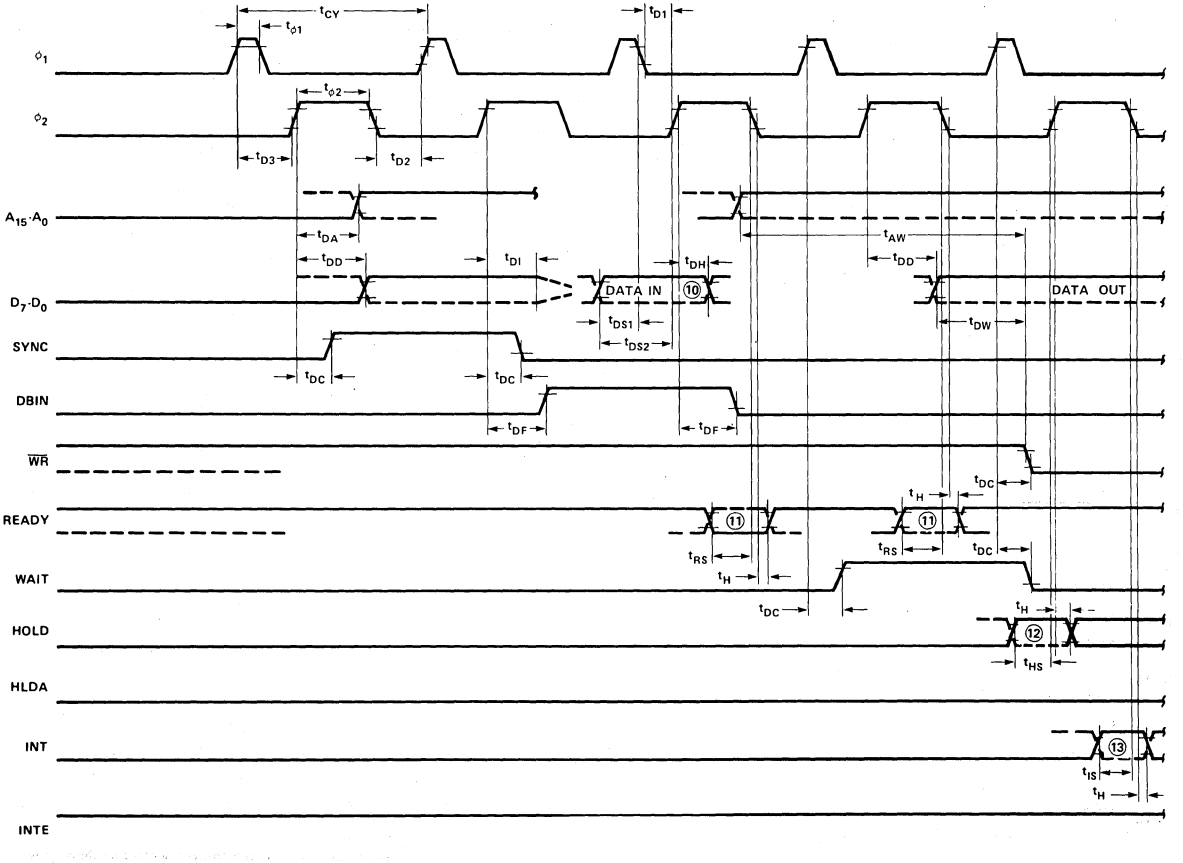
A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	70		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		200	nsec	C_L = 100pf
t_{DD}[2]	Data Output Delay From ϕ_2		220	nsec	
t_{DC}[2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		120	nsec	C_L = 50pf
t_{DF}[2]	DBIN Delay From ϕ_2	25	140	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

TIMING WAVEFORMS [14]

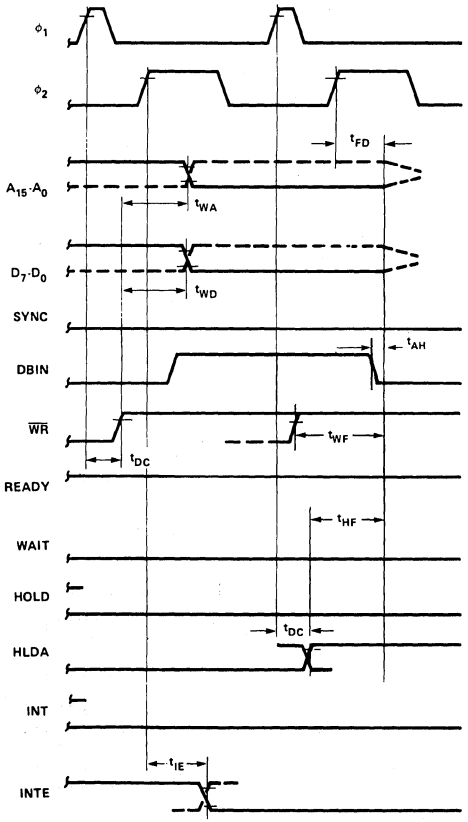
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (Continued)

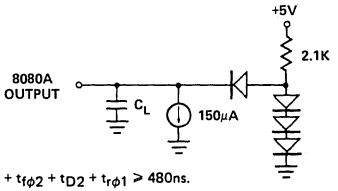
T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	120		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	120		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L=100pf: Address, Data C_L=50pf: $\overline{WR}$, HLDA, DBIN
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	



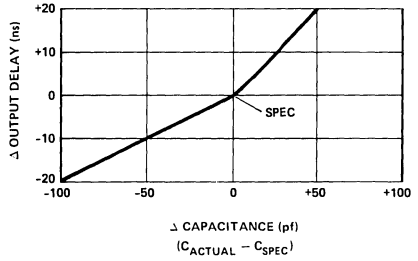
NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
$MOV_{r1,r2}$	Move register to register	0	1	D	D	D	S	S	S	5
MOV M, r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r, M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

NOTES: 1. DDD or SSS – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.
2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

8080A-1

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

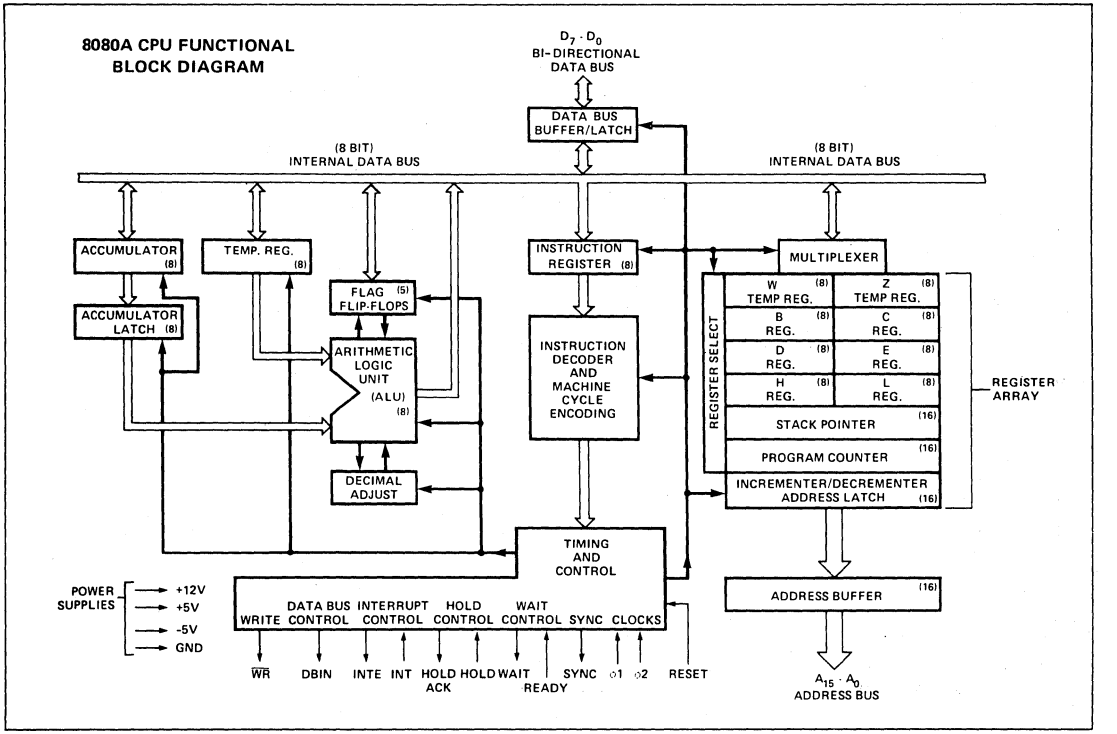
- **TTL Drive Capability**
- **1.3 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70° C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	T_{CY} = .32μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leq V_{IN} \leq V_{SS}$+0.8V V_{SS}+0.8V $\leq V_{IN} \leq V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

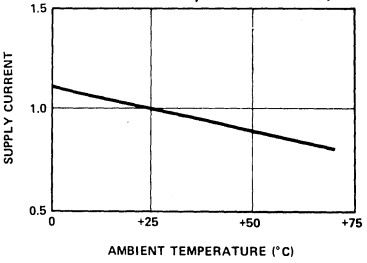
CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

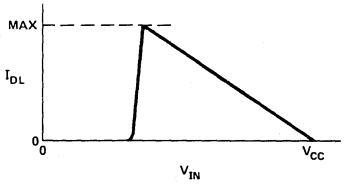
Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED.[3]



DATA BUS CHARACTERISTIC DURING DBIN



A.C. CHARACTERISTICS

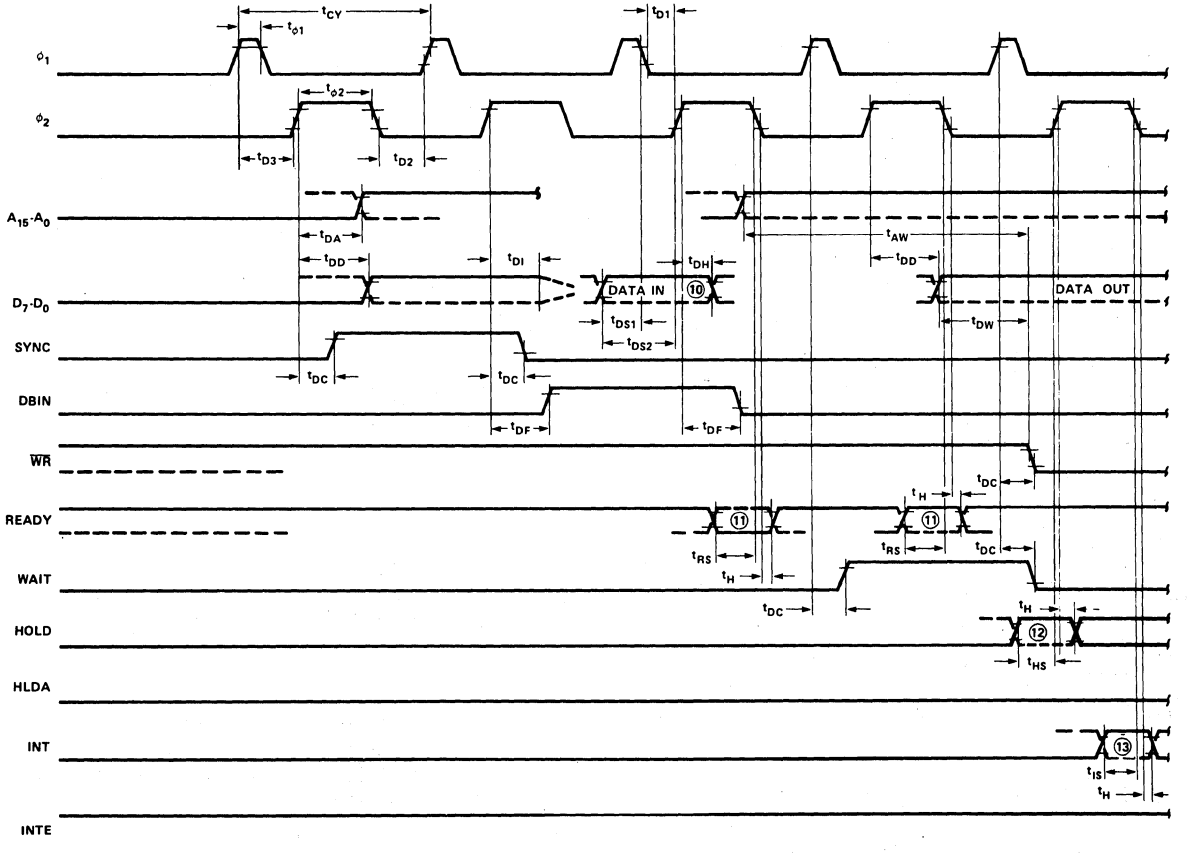
CAUTION: When operating the 8080A-1 at or near full speed, care must be taken to assure precise timing compatibility between 8080A-1, 8224 and 8228.

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	.32	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	25	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	50		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	145		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	60		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	60		nsec	
t_{DA} [2]	Address Output Delay From ϕ_2		150	nsec	C_L = 50pf
t_{DD} [2]	Data Output Delay From ϕ_2		180	nsec	
t_{DC} [2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		110	nsec	C_L = 50pf
t_{DF} [2]	DBIN Delay From ϕ_2	25	130	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	10		nsec	

TIMING WAVEFORMS [14]

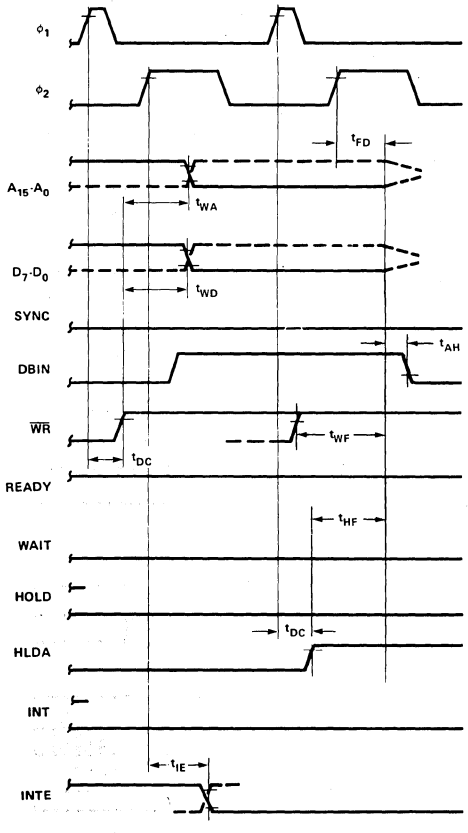
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (Continued)

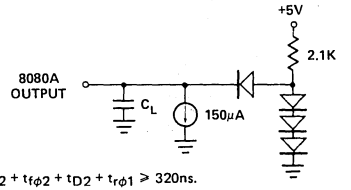
T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	120		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	90		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	120		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	100		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L = 50pf: Address, Data C_L = 50pf: $\overline{WR}$, HLDA, DBIN
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	



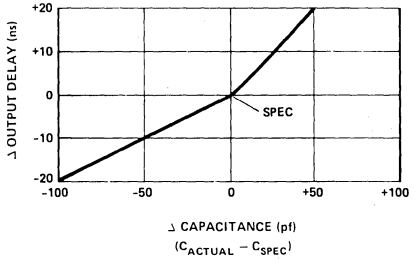
NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 320$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2}$ -110nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2}$ -150nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2}$ +10ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2}$ -50ns.
9. $t_{WF} = t_{D3} + t_{r\phi2}$ -10ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

8080A-2

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

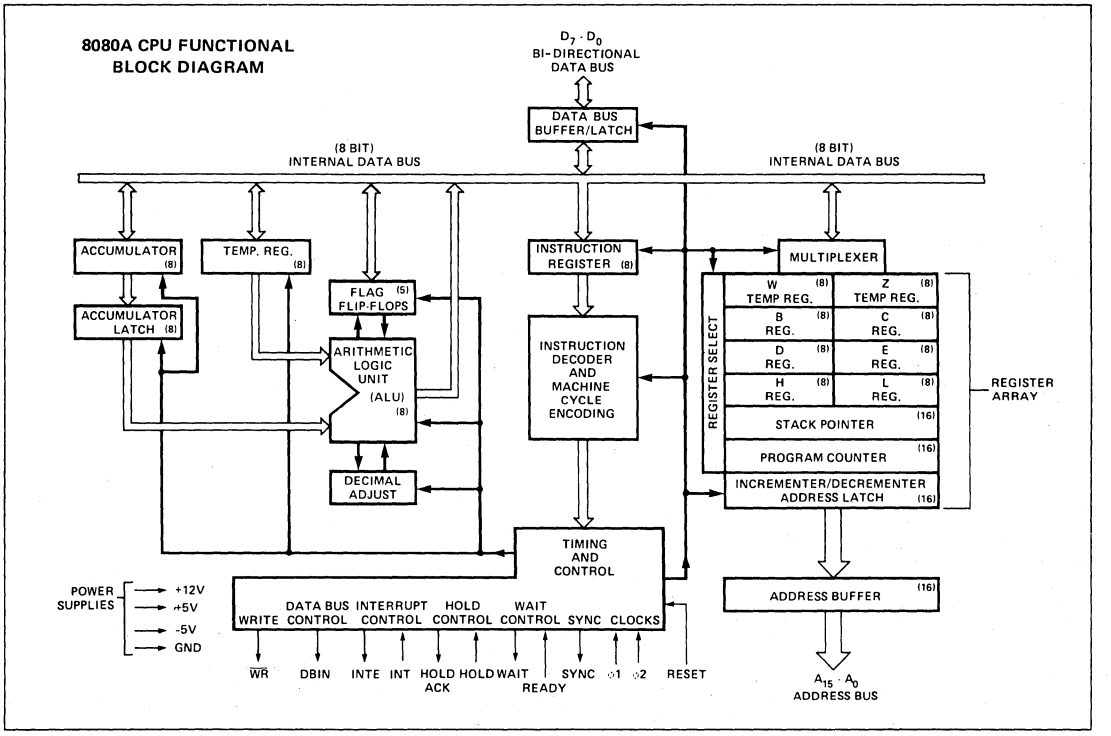
- **TTL Drive Capability**
- **1.5 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70° C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	T_{CY} = .38μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leq V_{IN} \leq V_{SS}+0.8V$ $V_{SS}+0.8V \leq V_{IN} \leq V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

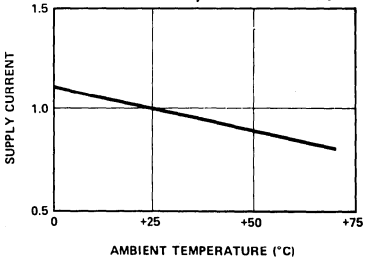
CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

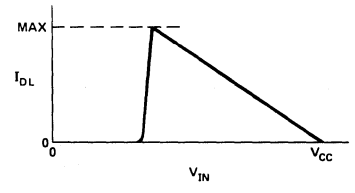
Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED.[3]



DATA BUS CHARACTERISTIC DURING DBIN



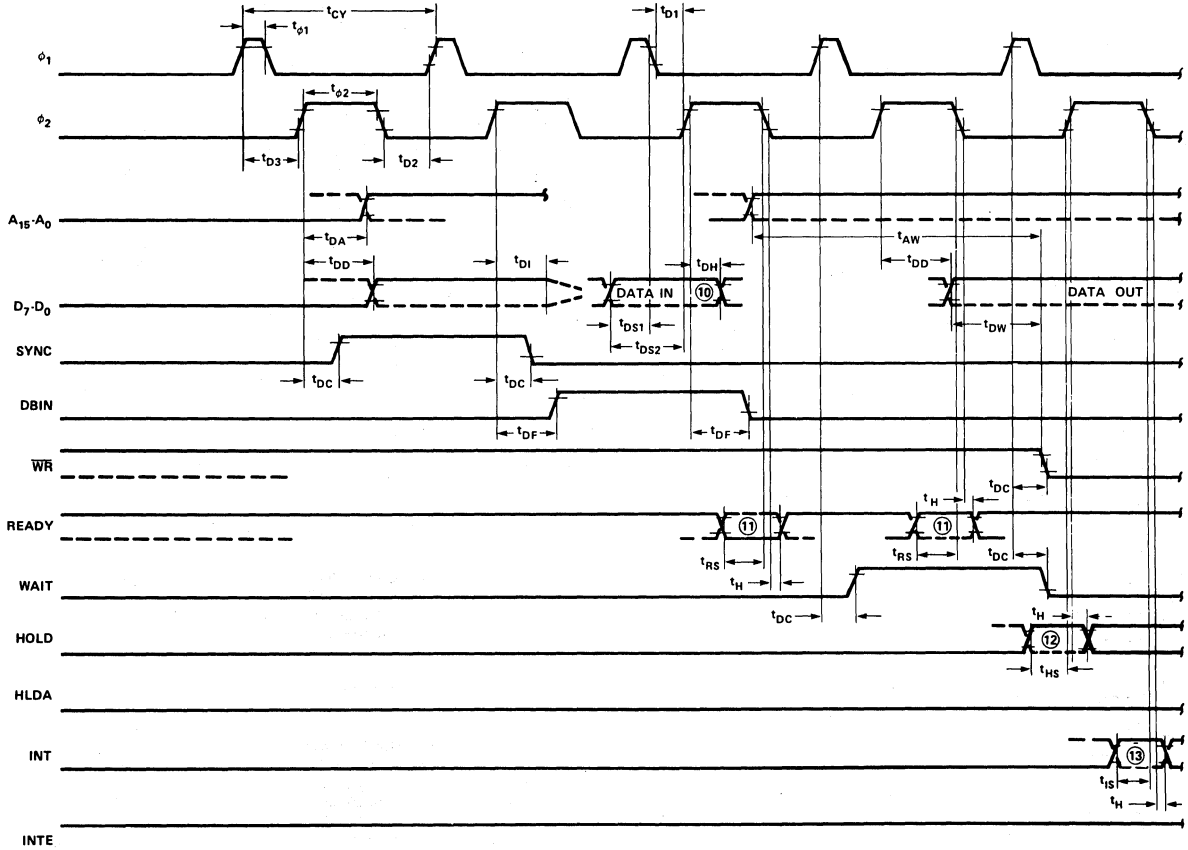
A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	.38	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	175		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	70		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	70		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		175	nsec	C_L = 100pf
t_{DD}[2]	Data Output Delay From ϕ_2		200	nsec	C_L = 100pf
t_{DC}[2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		120	nsec	C_L = 50pf
t_{DF}[2]	DBIN Delay From ϕ_2	25	140	nsec	C_L = 50pf
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	20		nsec	

TIMING WAVEFORMS [14]

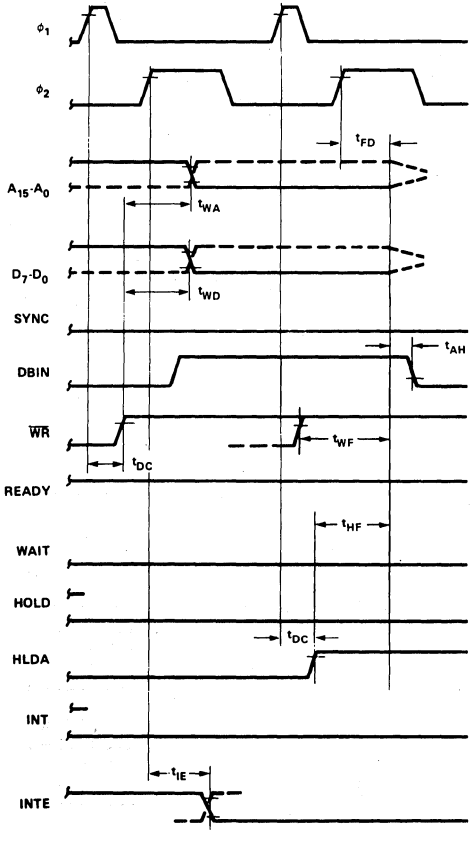
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (Continued)

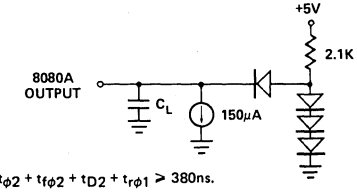
T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	130		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	90		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	120		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	100		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L=100pf: Address, Data C_L=50pf: $\overline{WR}$, HLDA, DBIN
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	



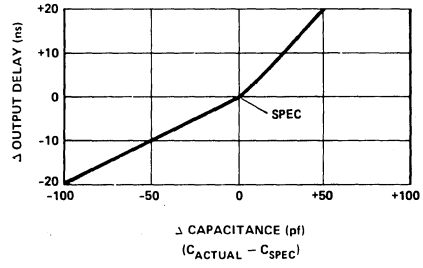
NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 380$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 130$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

MCS-80

M8080A

MILITARY TEMP

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

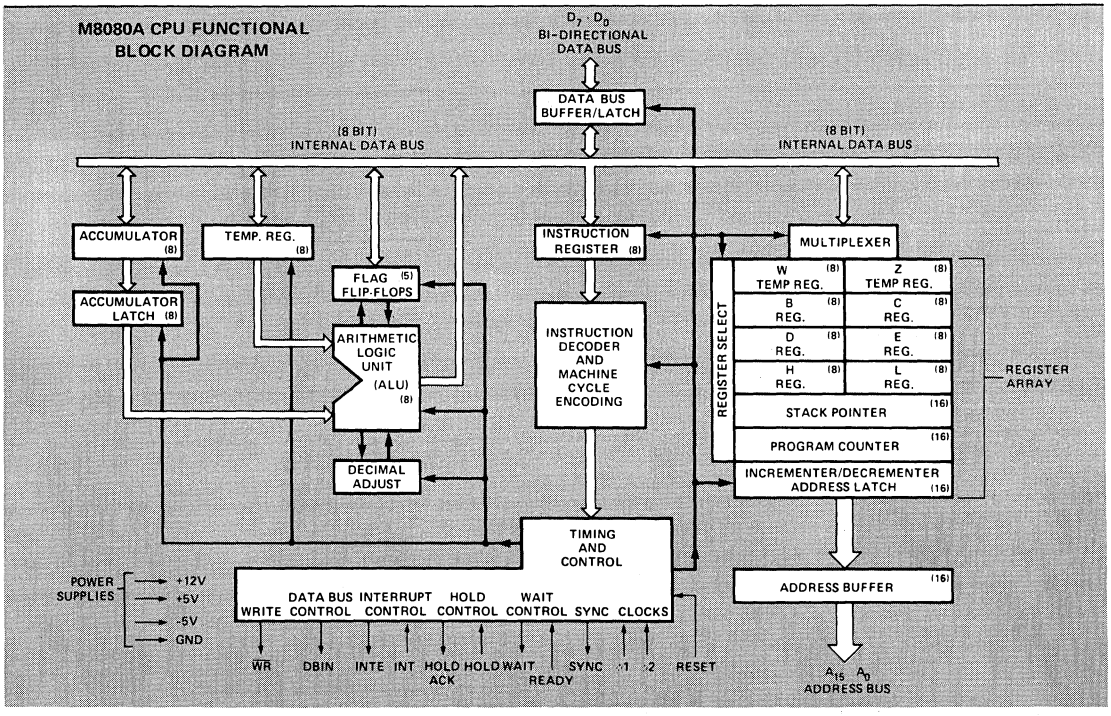
- **Full Military Temperature Range −55°C to +125°C**
- **±10% Power Supply Tolerance**
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**
- **TTL Drive Capability**

The Intel® M8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The M8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The M8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the M8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the M8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.



MCS-80

MILITARY TEMP.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.7W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	8.5		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		50	80	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	100	mA	T_{CY} = .48 μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}+0.8V$ $V_{SS}+0.8V \leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

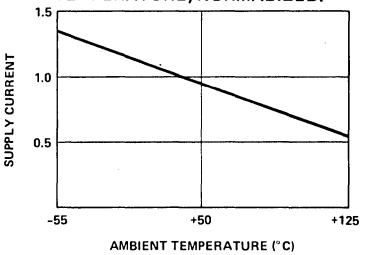
CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS} = 0V$, V_{BB} = -5V

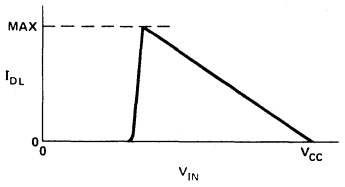
Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED. [3]



DATA BUS CHARACTERISTIC DURING DBIN



MCS-80

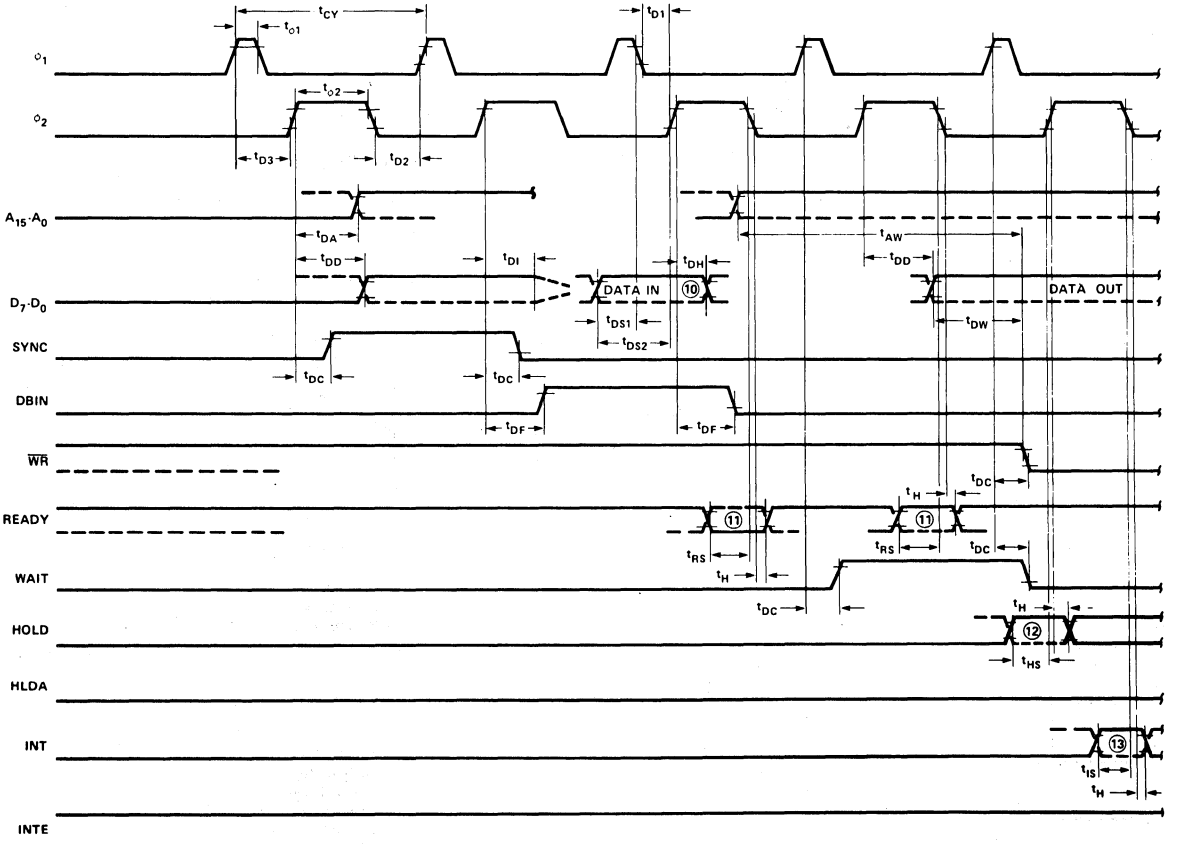
A.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY} [3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	80		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA} [2]	Address Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{DD} [2]	Data Output Delay From ϕ_2		220	nsec	
t_{DC} [2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		140	nsec	
t_{DF} [2]	DBIN Delay From ϕ_2	25	150	nsec	
t_{DI} [1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

TIMING WAVEFORMS [14]

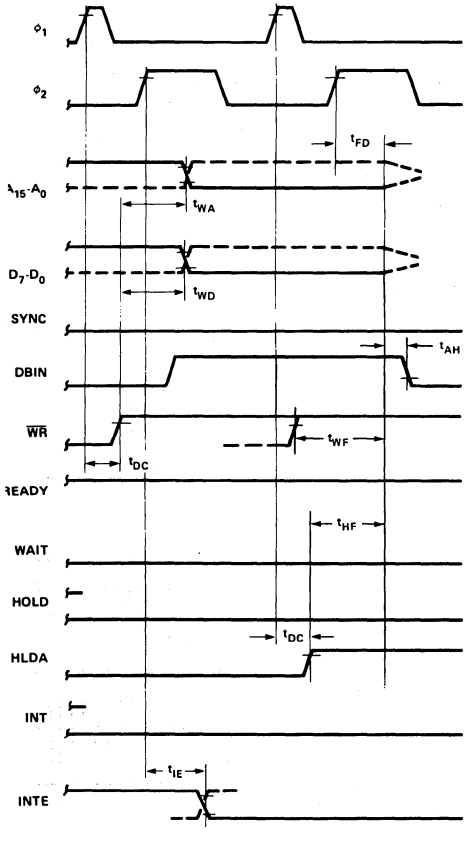
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 7.0V, "0" = 1.0V; INPUTS "1" = 3.0V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (Continued)

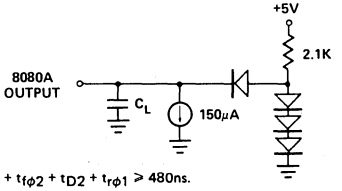
T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	130		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	50		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	120		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	120		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		130	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L = 50pf
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	



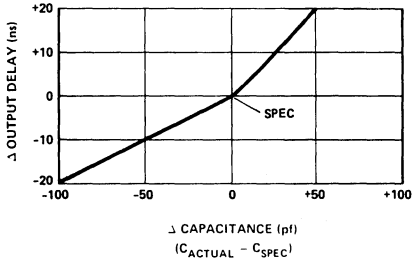
NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the M8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN $\cdot T_3$. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

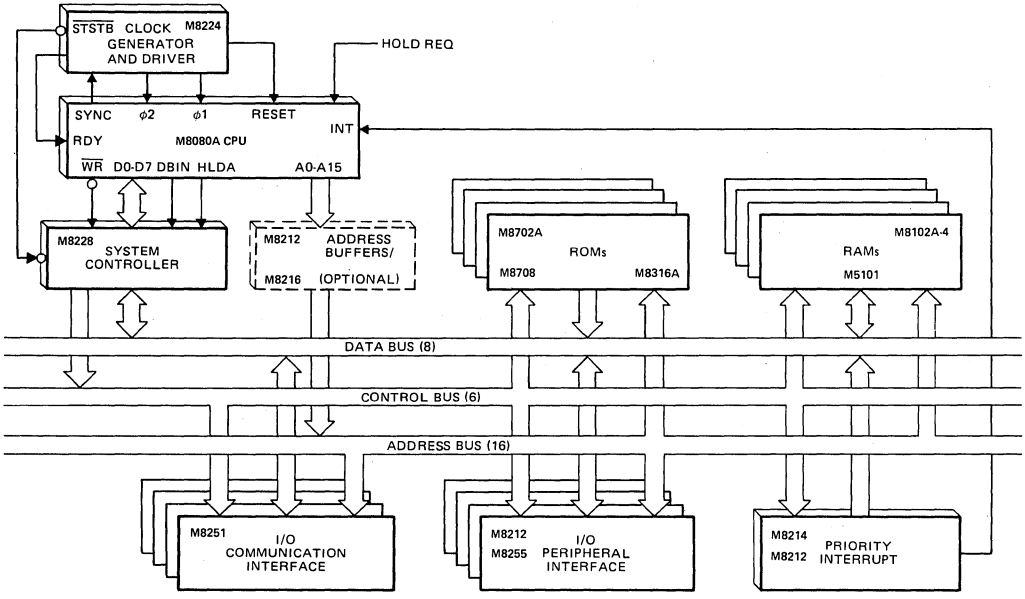
OTHER INTEL MCS-80 MILITARY TEMP PRODUCTS

AVAILABLE NOW

M8080A
M8102A-4
M5101
M8216
M8316A

COMING SOON

M8224
M8228
M8212
M8251
M8255
M8214
M8702A
M8708



Military Microcomputer System

8224

CLOCK GENERATOR AND DRIVER FOR 8080A CPU

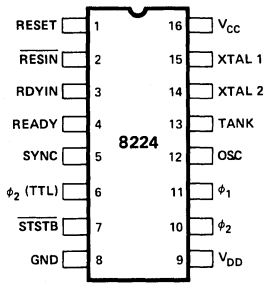
- **Single Chip Clock Generator/Driver for 8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**

The 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

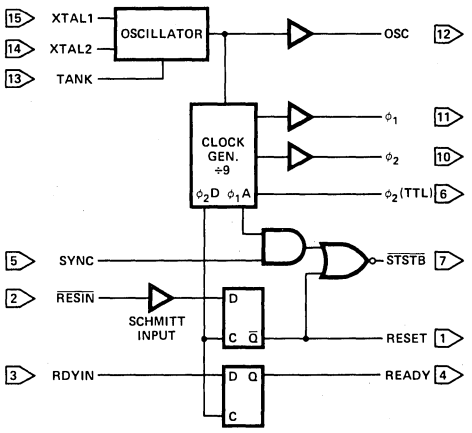
Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
φ1	8080 CLOCKS
φ2	8080 CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
φ2 (TTL)	φ2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

Absolute Maximum Ratings*

Temperature Under Bias . . . . . — 0°C to 70°C
Storage Temperature . . . . . —65°C to 150°C
Supply Voltage, V_{CC} . . . . . —0.5V to +7V
Supply Voltage, V_{DD} . . . . . —0.5V to +13.5V
Input Voltage . . . . . —1.5V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Characteristics

T_A = 0°C to 70°C; V_{CC} = +5.0V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
I_F	Input Current Loading			-.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.25V
V_C	Input Forward Clamp Voltage			1.0	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.6 2.0			V	Reset Input All Other Inputs
V_{IH}-V_{IL}	RESIN Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage			.45 .45	V V	(ϕ_1,ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} =2.5mA All Other Outputs I_{OL} = 15mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET All Other Outputs	 9.4 3.6 2.4			 V V V	 I_{OH} = -100μA I_{OH} = -100μA I_{OH} = -1mA
I_{SC}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CRYSTAL REQUIREMENTS

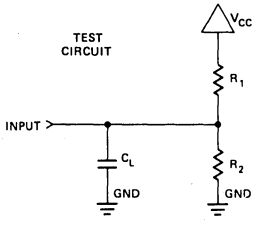
Tolerance: .005% at 0°C -70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With tank circuit use 3rd overtone mode.

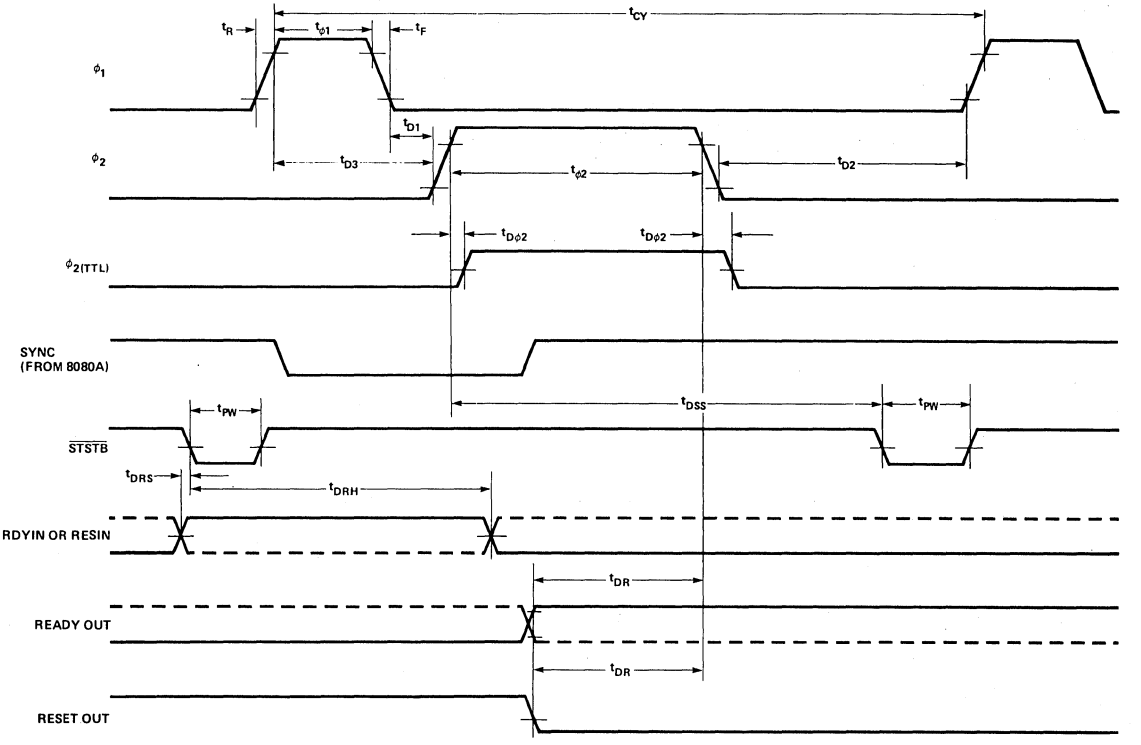
A.C. Characteristics

V_{CC} = +5.0V ± 5%; V_{DD} = +12.0V ± 5%; T_A = 0°C to 70°C

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9}$ - 20ns			ns	C_L = 20pF to 50pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9}$ - 35ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9}$ - 14ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9}$ + 20ns		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2TTL,CL=30 R_1=300Ω R_2=600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9}$ - 30ns		$\frac{6tcy}{9}$		$\overline{STSTB}$, CL=15pF R_1 = 2K R_2 = 4K
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9}$ - 15ns				
t_{DRS}	RDYIN Setup Time to Status Strobe	50ns - $\frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	RDYIN or RESIN to ϕ_2 Delay.	$\frac{4tcy}{9}$ - 25ns				Ready & Reset CL=10pF R_1=2K R_2=4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency	27			MHz	
C_{in}	Input Capacitance			8	pF	V_{CC}=+5.0V V_{DD}=+12V V_{BIAS}=2.5V f=1MHz



WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

EXAMPLE:

A.C. Characteristics (For t_{CY} = 488.28 ns)

T_A = 0°C to 70°C; V_{DD} = +5V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	Ready & Reset Loaded to 2mA/10pF
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	

MCS-80

8228/8238

SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- **Single Chip System Control for MCS™-80 Systems**
- **Built-in Bi-Directional Bus Driver for Data Bus Isolation**
- **Allows the use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28 Pin Dual In-Line Package**
- **Reduces System Package Count**
- ***8238 Has Advanced $\overline{IOW}$/$\overline{MEMW}$ For Large System Timing Control**

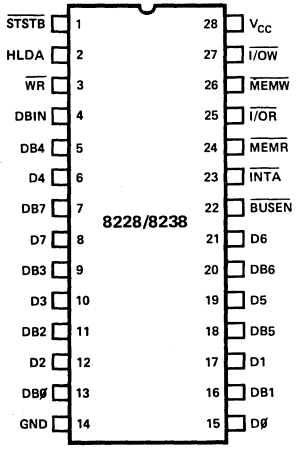
The 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems deisgner to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

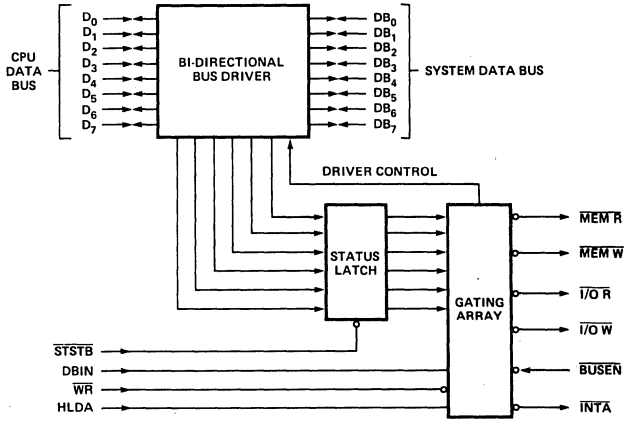
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



8228/8238 BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
$\overline{I/OR}$	I/O READ	$\overline{WR}$	WR (FROM 8080)
$\overline{I/OW}$	I/O WRITE	$\overline{BUSEN}$	BUS ENABLE INPUT
$\overline{MEMR}$	MEMORY READ	$\overline{STSTB}$	STATUS STROBE (FROM 8224)
$\overline{MEMW}$	MEMORY WRITE	V_{CC}	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

Absolute Maximum Ratings*

Temperature Under Bias . . . . . −0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . . −0.5V to +7V
Input Voltage . . . . . −1.5V to +7V
Output Current 100mA

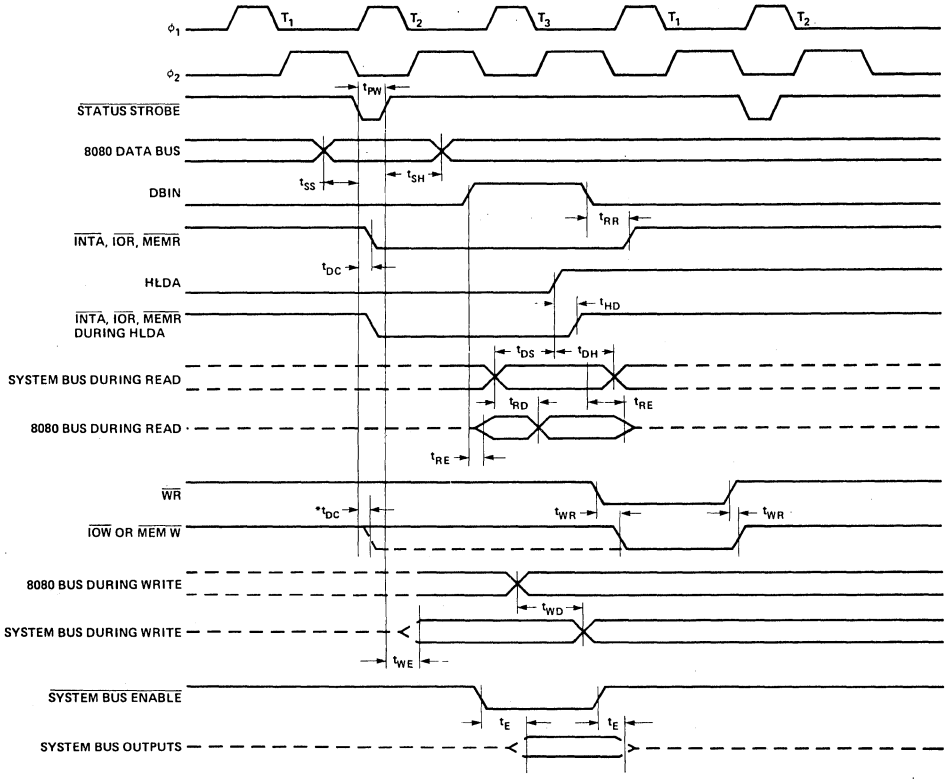
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Characteristics T_A = 0°C to 70°C; V_{CC} = 5V ±5%.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		.75	-1.0	V	V_{CC}=4.75V; I_C=-5mA
I_F	Input Load Current, $\overline{STSTB}$			500	μA	V_{CC} = 5.25V
	D_2 & D_6			750	μA	V_F = 0.45V
	D_0, D_1, D_4, D_5, & D_7			250	μA	
	All Other Inputs			250	μA	
I_R	Input Leakage Current $\overline{STSTB}$			100	μA	V_{CC} = 5.25V
	DB_0-DB_7			20	μA	V_R = 5.25V
	All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		140	190	mA	V_{CC}=5.25V
V_{OL}	Output Low Voltage, D_0-D_7			.45	V	V_{CC}=4.75V; I_{OL}=2mA
	All Other Outputs			.45	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0-D_7	3.6	3.8		V	V_{CC}=4.75V; I_{OH}=-10μA
	All Other Outputs	2.4			V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	V_{CC}=5V
$I_{O(off)}$	Off State Output Current, All Control Outputs			100	μA	V_{CC}=5.25V; V_O=5.25
				-100	μA	V_O=.45V
I_{INT}	INTA Current			5	mA	(See Figure below)

Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*ADVANCED $\overline{IOW}$/$\overline{MEMW}$ FOR 8238 ONLY.

A.C. Characteristics $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$.

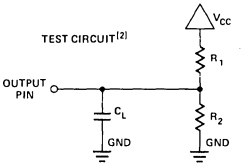
Symbol	Parameter	Limits		Units	Condition
		Min.	Max.		
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	60	ns	C_L = 100pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	C_L = 100pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	C_L = 25pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	C_L = 25pF
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	45	ns	C_L = 100pF
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	C_L = 100pF
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	C_L = 100pF
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7		30	ns	C_L = 100pF
t_{HD}	HLDA to Read Status Outputs		25	ns	
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	C_L = 100pF

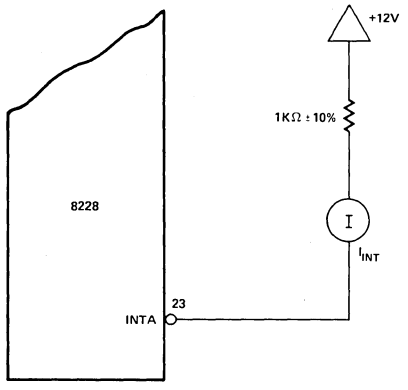
Capacitance This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

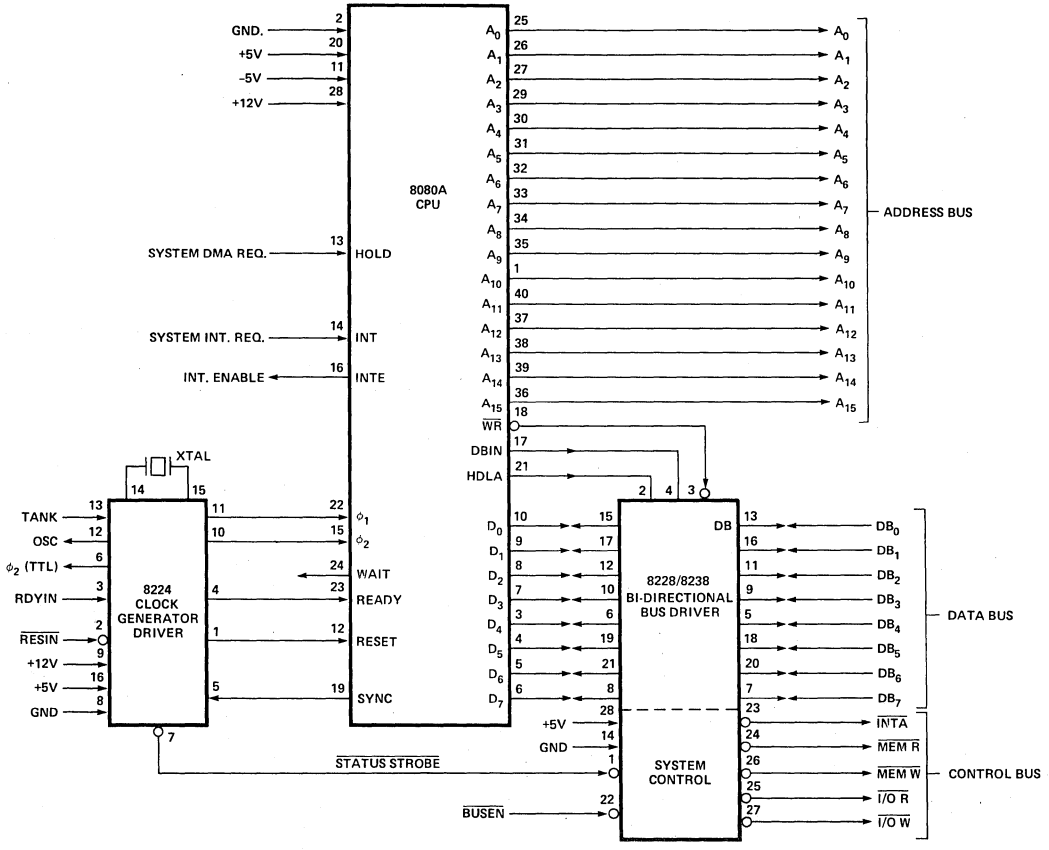
TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1MHz.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.





INTA Test Circuit (for RST 7)



CPU Standard Interface

8008/8008-1

EIGHT-BIT MICROPROCESSOR

- **Instruction Cycle Time — 12.5 μs with 8008-1 or 20 μs with 8008**
- **Directly addresses 16K x 8 bits of memory (RAM, ROM, or S.R.)**
- **Interrupt Capability**
- **48 Instructions, Data Oriented**
- **Address stack contains eight 14-bit registers (including program counter) which permit nesting of subroutines up to seven levels**

The 8008 is a single chip MOS 8-bit parallel central processor unit for the MCS-8 microcomputer system.

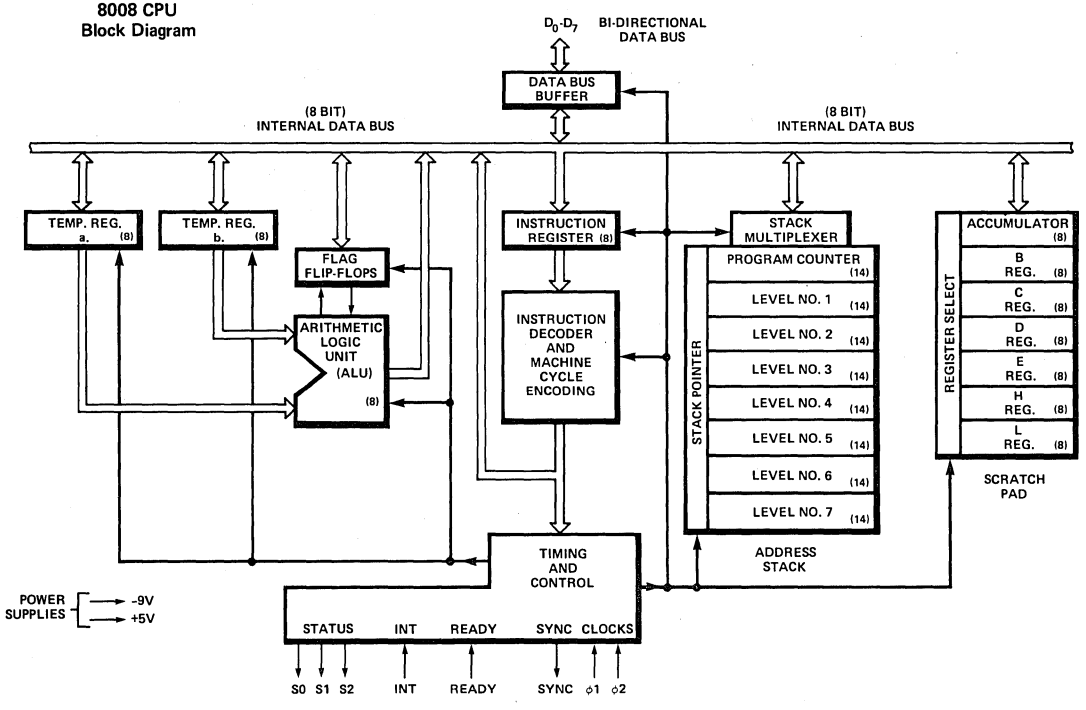
This CPU contains six 8-bit data registers, an 8-bit accumulator, two 8-bit temporary registers, four flag bits (carry, zero, sign, parity), and an 8-bit parallel binary arithmetic unit which implements addition, subtraction, and logical operations. A memory stack containing a 14-bit program counter and seven 14-bit words is used internally to store program and subroutine addresses. The 14-bit address permits the direct addressing of 16K words of memory (any mix of RAM, ROM or S.R.).

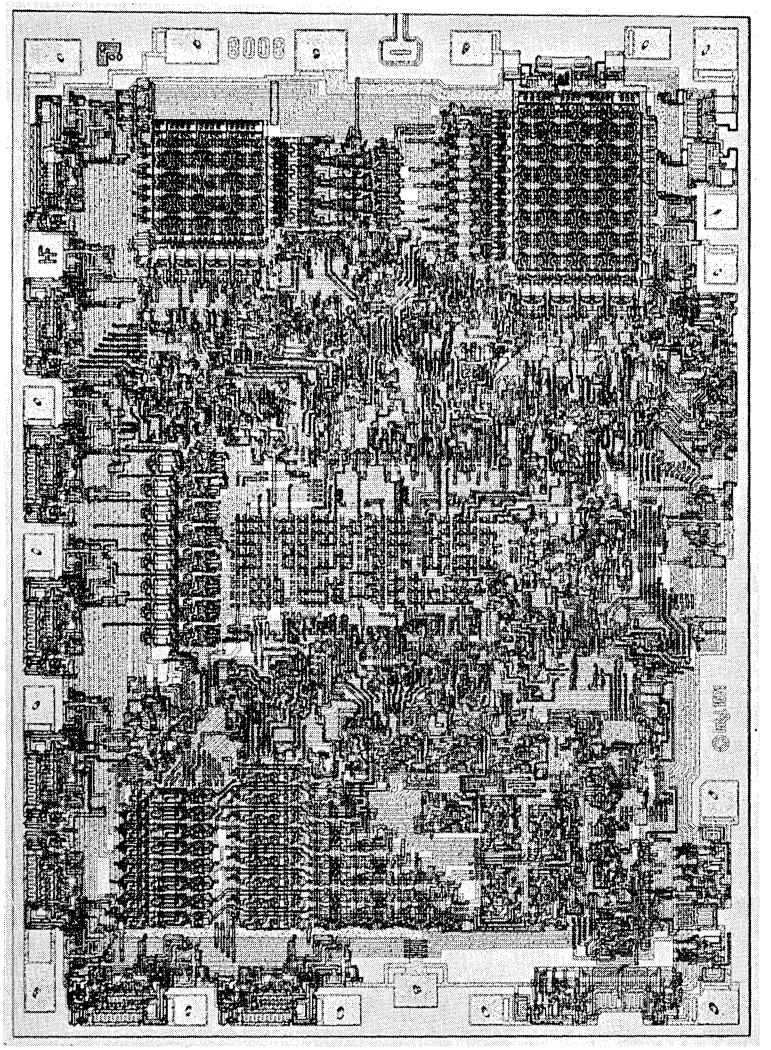
The instruction set of the 8008 consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutine.

The normal program flow of the 8008 may be interrupted through the use of the INTERRUPT control line. This allows the servicing of slow I/O peripheral devices while also executing the main program.

The READY command line synchronizes the 8008 to the memory cycle allowing any type or speed of semiconductor memory to be used.

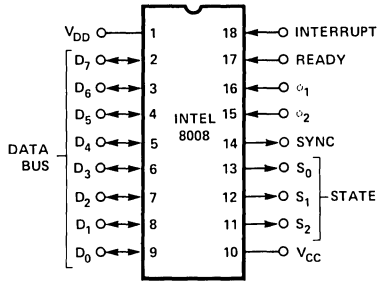
8008 CPU
Block Diagram





8008 PHOTOMICROGRAPH

8008 FUNCTIONAL PIN DESCRIPTION



D_0-D_7

BI-DIRECTIONAL DATA BUS. All address and data communication between the processor and the program memory, data memory, and I/O devices occurs on these 8 lines. Cycle control information is also available.

INT

INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

READY

READY input. This command line is used to synchronize the 8008 to the memory cycle allowing any speed memory to be used.

SYNC

SYNC output. Synchronization signal generated by the processor. It indicates the beginning of a machine cycle.

ϕ_1, ϕ_2

Two phase clock inputs.

S_0, S_1, S_2

MACHINE STATE OUTPUTS. The processor controls the use of the data bus and determines whether it will be sending or receiving data. State signals S_0, S_1, and S_2, along with SYNC inform the peripheral circuitry of the state of the processor.

V_{CC} +5V ±5%

V_{DD} -9V ±5%

BASIC INSTRUCTION SET

Data and Instruction Formats

Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, I/O arithmetic or logical, rotate or return instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	Immediate mode instructions
Three Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS	JUMP or CALL instructions
X X D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS*	*For the third byte of this instruction, D_6 and D_7 are "don't care" bits.

For the MCS-8™ a logic "1" is defined as a high level and a logic "0" is defined as a low level.

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE D_7 D_6	D_5 D_4 D_3	D_2 D_1 D_0	DESCRIPTION OF OPERATION
(1) MOV r_1, r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) MOV r, M	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
MOV M, r	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) MVI r	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
MVI M	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INR r	(5)	0 0	D D D	0 0 0	Increment the content of index register r ($r \neq A$).
DCR r	(5)	0 0	D D D	0 0 1	Decrement the content of index register r ($r \neq A$).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADD r	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADD M	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ADC r	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B from the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ADC M	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	
SUB r	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUB M	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0 B B	0 1 0 B B B	1 0 0 B B B	
SBB r	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBB M	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0 B B	0 1 1 B B B	1 0 0 B B B	

BASIC INSTRUCTION SET

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
ANA r	(5)	1 0	1 0 0	S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
ANA M	(8)	1 0	1 0 0	1 1 1	
ANI	(8)	0 0 B B	1 0 0 B B B	1 0 0 B B B	
XRA r	(5)	1 0	1 0 1	S S S	Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRA M	(8)	1 0	1 0 1	1 1 1	
XRI	(8)	0 0 B B	1 0 1 B B B	1 0 0 B B B	
ORA r	(5)	1 0	1 1 0	S S S	Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator .
ORA M	(8)	1 0	1 1 0	1 1 1	
ORI	(8)	0 0 B B	1 1 0 B B B	1 0 0 B B B	
CMP r	(5)	1 0	1 1 1	S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CMP M	(8)	1 0	1 1 1	1 1 1	
CPI	(8)	0 0 B B	1 1 1 B B B	1 0 0 B B B	
RLC	(5)	0 0	0 0 0	0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0	Rotate the content of the accumulator right through the carry.
Program Counter and Stack Control Instructions					
(4) JMP	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$.
(5) JNC, JNZ, JP, JPO	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
JC, JZ JM, JPE	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
CALL	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$. Save the current address (up one level in the stack).
CNC, CNZ, CP, CPO	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
CC, CZ, CM, CPE	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
RET	(5)	0 0	X X X	1 1 1	Unconditionally return (down one level in the stack).
RNC, RNZ, RP, RPO	(3 or 5)	0 0	0 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
RC, RZ RM, RPE	(3 or 5)	0 0	1 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).
Input/Output Instructions					
IN	(8)	0 1	0 0 M	M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00).
Machine Instruction					
HLT	(4)	0 0	0 0 0	0 0 X	Enter the STOPPED state and remain there until interrupted.
	(4)	1 1	1 1 1	1 1 1	

NOTES:
(1) SSS = Source Index Register, DDD = Destination Index Register. These registers, r_i, are designated A(accumulator–000), B(001), C(010), D(011), E(100), H(101), L(110).
(2) Memory registers are addressed by the contents of registers H & L.
(3) Additional bytes of instruction are designated by BBBBBBBB.
(4) X = "Don't Care".
(5) Flag flip-flops are defined by C_4C_3: carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−55°C to +150°C
Input Voltages and Supply Voltage With Respect to V_{CC}	+0.5 to −20V
Power Dissipation	1.0 W @ 25°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5% unless otherwise specified. Logic "1" is defined as the more positive level (V_{IH}, V_{OH}). Logic "0" is defined as the more negative level (V_{IL}, V_{OL}).

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I_{DD}	AVERAGE SUPPLY CURRENT-OUTPUTS LOADED*		30	60	mA	T_A = 25°C
I_{LI}	INPUT LEAKAGE CURRENT			10	μA	V_{IN} = 0V
V_{IL}	INPUT LOW VOLTAGE (INCLUDING CLOCKS)	V_{DD}		V_{CC}−4.2	V	
V_{IH}	INPUT HIGH VOLTAGE (INCLUDING CLOCKS)	V_{CC}−1.5		V_{CC}+0.3	V	
V_{OL}	OUTPUT LOW VOLTAGE			0.4	V	I_{OL} = 0.44mA C_L = 200 pF
V_{OH}	OUTPUT HIGH VOLTAGE	V_{CC}−1.5			V	I_{OH} = 0.2mA

*Measurements are made while the 8008 is executing a typical sequence of instructions. The test load is selected such that at V_{OL} = 0.4V, I_{OL} = 0.44mA on each output.

A.C. CHARACTERISTICS

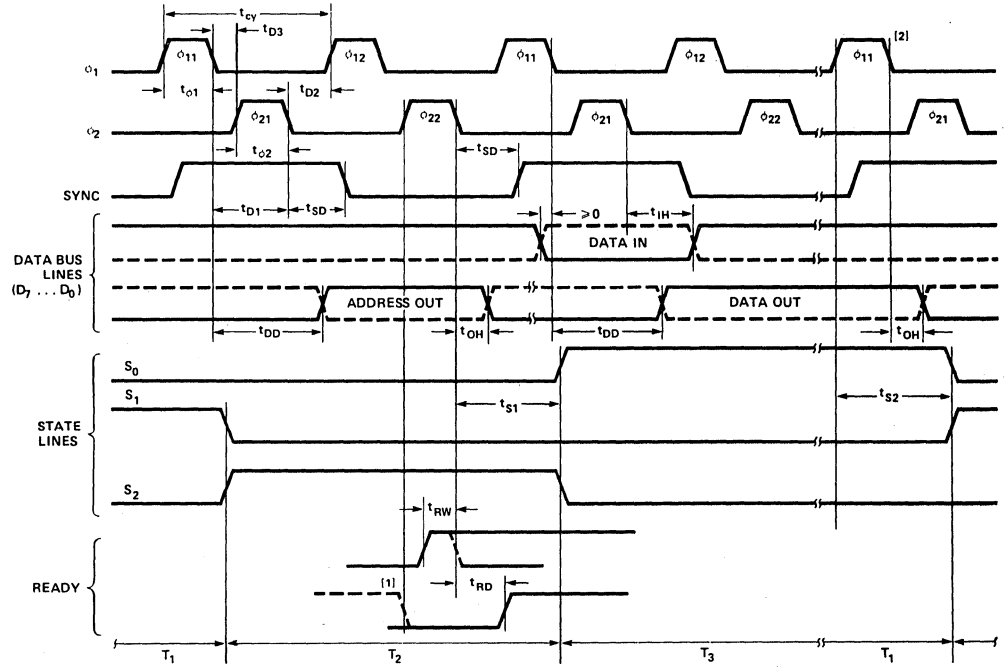
T_A = 0°C to 70°C; V_{CC} = +5V ±5%, V_{DD} = −9V ±5%. All measurements are referenced to 1.5V levels.

SYMBOL	PARAMETER	8008 LIMITS MIN.	8008 LIMITS MAX.	8008-1 LIMITS MIN.	8008-1 LIMITS MAX.	UNIT	TEST CONDITIONS
t_{CY}	CLOCK PERIOD	2	3	1.25	3	μs	t_R,t_F = 50ns
t_R,t_F	CLOCK RISE AND FALL TIMES		50		50	ns	
$t_{\phi 1}$	PULSE WIDTH OF ϕ_1	.70		.35		μs	
$t_{\phi 2}$	PULSE WIDTH OF ϕ_2	.55		.35		μs	
t_{D1}	CLOCK DELAY FROM FALLING EDGE OF ϕ_1 TO FALLING EDGE OF ϕ_2	.90	1.1		1.1	μs	
t_{D2}	CLOCK DELAY FROM ϕ_2 TO ϕ_1	.40		.35		μs	
t_{D3}	CLOCK DELAY FROM ϕ_1 TO ϕ_2	.20		.20		μs	
t_{DD}	DATA OUT DELAY		1.0		1.0	μs	C_L = 100pF
t_{OH}	HOLD TIME FOR DATA BUS OUT	.10		.10		μs	
t_{IH}	HOLD TIME FOR DATA IN	[1]		[1]		μs	
t_{SD}	SYNC OUT DELAY		.70		.70	μs	C_L = 100pF
t_{S1}	STATE OUT DELAY (ALL STATES EXCEPT T1 AND T1I)[2]		1.1		1.1	μs	C_L = 100pF
t_{S2}	STATE OUT DELAY (STATES T1 AND T1I)		1.0		1.0	μs	C_L = 100pF
t_{RW}	PULSE WIDTH OF READY DURING ϕ_{22} TO ENTER T3 STATE	.35		.35		μs	
t_{RD}	READY DELAY TO ENTER WAIT STATE	.20		.20		μs	

[1] t_{IH} MIN ≥ t_{SD}

[2] If the INTERRUPT is not used, all states have the same output delay, t_{S1}.

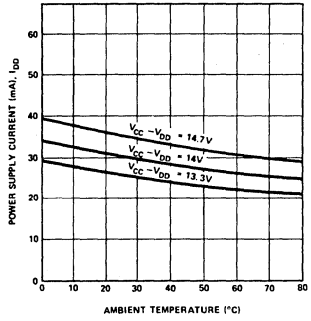
TIMING DIAGRAM



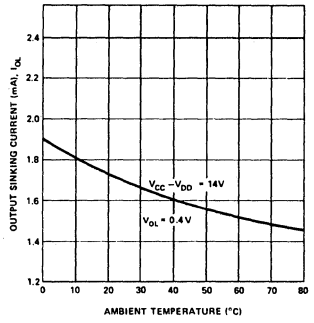
Notes: 1. READY line must be at "0" prior to ϕ_{22} of T_2 to guarantee entry into the WAIT state.
2. INTERRUPT line must not change levels within 200ns (max.) of falling edge of ϕ_1.

TYPICAL D.C. CHARACTERISTICS

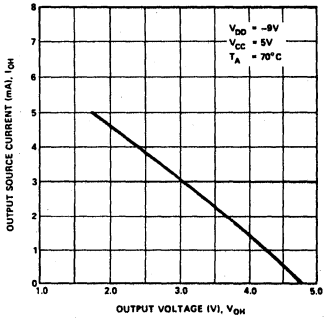
POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT SINKING CURRENT VS. TEMPERATURE

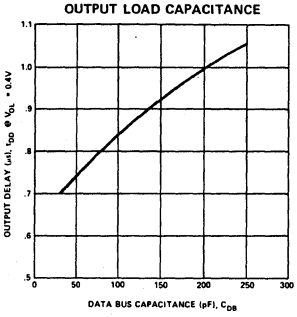


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



TYPICAL A.C. CHARACTERISTICS

DATA OUT DELAY VS. OUTPUT LOAD CAPACITANCE



CAPACITANCE f = 1MHz; T_A = 25°C; Unmeasured Pins Grounded

SYMBOL	TEST	LIMIT (pF)	
		TYP.	MAX.
C_{IN}	INPUT CAPACITANCE	5	10
C_{DB}	DATA BUS I/O CAPACITANCE	5	10
C_{OUT}	OUTPUT CAPACITANCE	5	10

MCS-80

8702A

2048 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

- **Access Time — 1.3 μsec Max.**
- **Fast Programming — 2 Minutes for All 2048 Bits**
- **Fully Decoded, 256 x 8 Organization**
- **Static MOS — No Clocks Required**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output — OR-Tie Capability**
- **Simple Memory Expansion Chip Select Input Lead**

The 8702A is a 256 word by 8 bit electrically programmable ROM ideally suited for microcomputer system development where fast turn-around and pattern experimentation are important. The 8702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The 8702A is packaged in a 24 pin dual-in line package with a transparent quartz lid. The transparent quartz lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. This procedure can be repeated as many times as required.

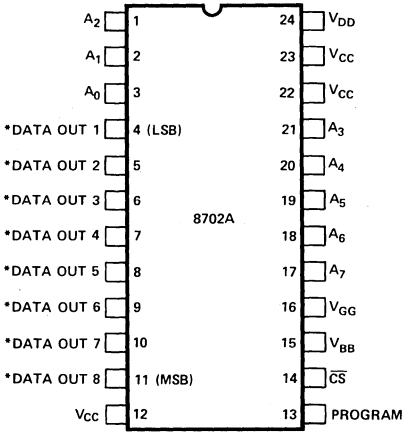
The circuitry of the 8702A is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the Intel 8302, is ideal for large volume production runs of systems initially using the 8702A.

The 8702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

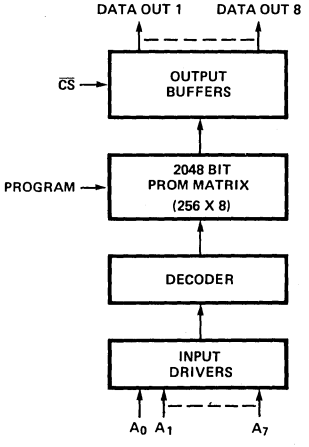
MCS-80

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING.

BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
DO_1- DO_2	DATA OUTPUTS

PIN CONNECTIONS

The external lead connections to the 8702A differ, depending on whether the device is being programmed[1] or used in read mode. (See following table.)

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = −9V±5%, V_{GG}[2] = −9V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.[3]	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			10	µA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DDO}	Power Supply Current		5	10	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC}−2, I_{OL} = 0.0mA, T_A = 25°C
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$=0.0, I_{OL} =0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
I_{GG}	Gate Supply Current			10	µA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC} −2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5			V	I_{OH} = −200 µA

Continuous Operation

Note 1: In the programming mode, the data inputs 1–8 are pins 4–11 respectively. $\overline{CS}$ = GND.
Note 2: V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} increases in proportion to V_{GG} duty cycle. (See p. 5)
Note 3: Typical values are at nominal voltages and T_A = 25° C.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay			1.3	µs
t_{DVGG}	Clocked V_{GG} set up	1.0			µs
t_{CS}	Chip select delay			400	ns
t_{CO}	Output delay from $\overline{CS}$			900	ns
t_{OD}	Output deselect			400	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	µs

Note 1. The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

CAPACITANCE* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		10	15	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Clocked V_{GG} Mode)			30	pF	

* This parameter is periodically sampled and is not 100% tested.

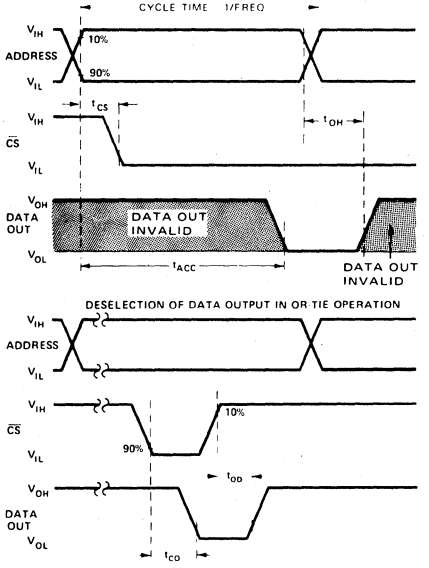
SWITCHING CHARACTERISTICS

Conditions of Test:

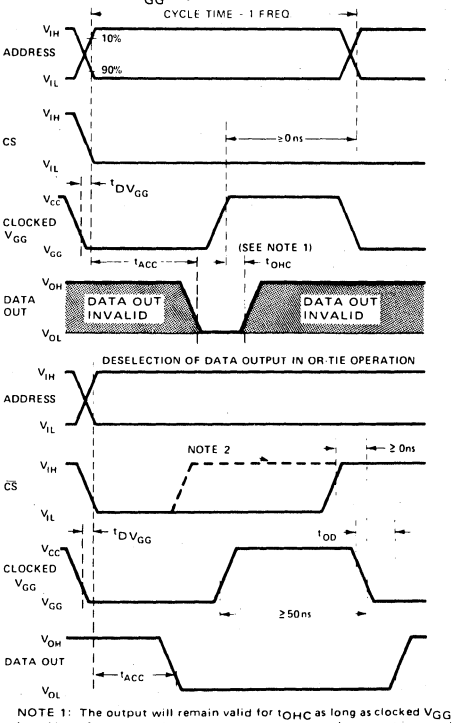
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD} ≤15 ns)

A) Constant V_{GG} Operation



B) Clocked V_{GG} Operation



NOTE 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

NOTE 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

8708

8192/4096 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

• 8708 1024x8 Organization

- **Fast Programming — Typ. 100 sec. For All 8K Bits**
- **Low Power During Programming**
- **Access Time—450 ns**
- **Standard Power Supplies— +12V, ±5V**
- **Static—No Clocks Required**
- **Inputs and Outputs TTL Compatible During Both Read and Program Modes**
- **Three-State Output—OR-Tie Capability**

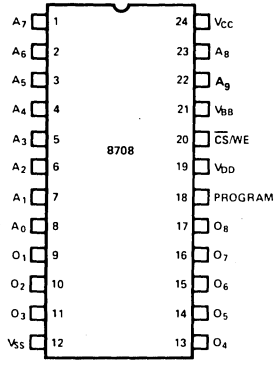
The Intel© 8708 is a high speed 8192 bit erasable and electrically reprogrammable ROM's (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 8708 is packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

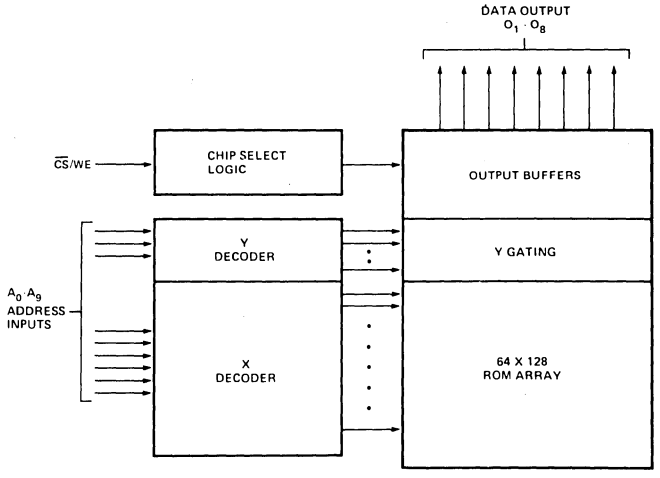
A pin for pin mask programmed ROM, the Intel© 8308, is available for large volume production runs of systems initially using the 8708.

The 8708 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

MCS-80

Absolute Maximum Ratings*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
All Input or Output Voltages with Respect to V_{BB} (except Program)	+15V to -0.3V
Program Input to V_{BB}	+35V to -0.3V
Supply Voltages V_{CC} and V_{SS} with Respect to V_{BB}	+15V to -0.3V
V_{DD} with Respect to V_{BB}	+20V to -0.3V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. The program input (Pin 18) may be tied to V_{SS} or V_{CC} during the read mode.

A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
$t_{\overline{CO}}$	Chip Select to Output Delay			120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance[1] $T_A = 25°C$, $f = 1MHz$

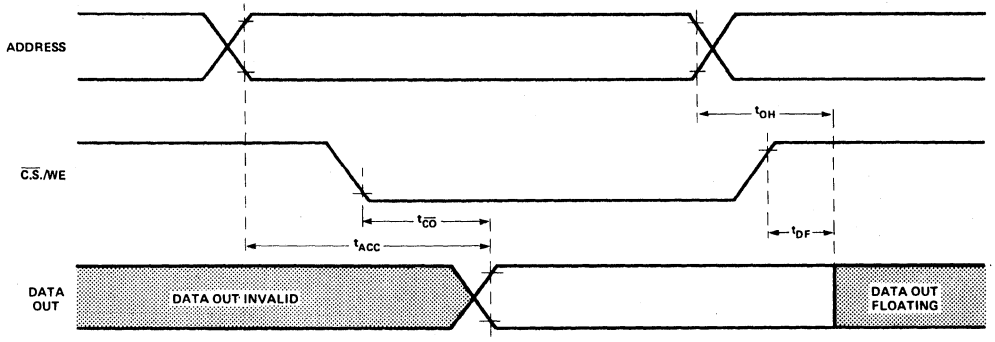
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN}=0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT}=0V$

Note 1. This parameter is periodically sampled and not 100% tested.

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ⩽20ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

Waveforms



8302

2048 BIT MASK PROGRAMMABLE READ ONLY MEMORY

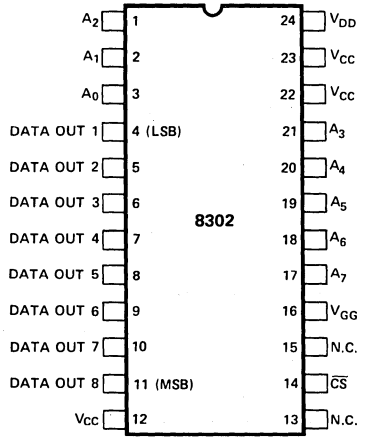
- **Access Time — 1 μsec Max.**
- **Fully Decoded, 256 x 8 Organization**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output — OR-Tie Capability**
- **Static MOS — No Clocks Required**
- **Simple Memory Expansion — Chip Select Input Lead**
- **24-Pin Dual-In-Line Hermetically Sealed Ceramic Package**

The Intel® 8302 is a fully decoded 256 word by 8 bit metal mask ROM. It is ideal for large volume production runs of microcomputer systems initially using the 8702A erasable and electrically programmable ROM. The 8302 has the same pinning as the 8702A.

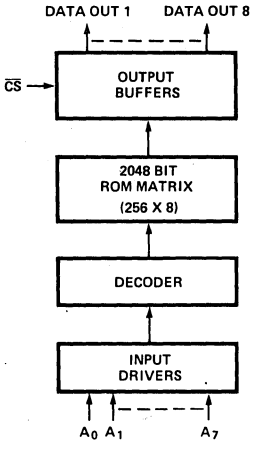
The 8302 is entirely static — no clocks are required. Inputs and outputs of the 8302 are TTL compatible. The output is three-state for OR-tie capability. A separate chip select input allows easy memory expansion. The 8302 is packaged in a 24 pin dual-in-line hermetically sealed ceramic package.

The 8302 is fabricated with p-channel silicon gate technology. This low threshold allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
DO_1-DO_8	DATA OUTPUTS

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . +0.5V to −20V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = −9V±5%, $V_{GG}^{(1)}$ = −9V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.(2)	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DDO}	Power Supply Current		5	10	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC}−2 I_{OL} = 0.0mA, T_A = 25°C
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$=0.0 I_{OL} =0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
						Continuous Operation
I_{GG}	Gate Supply Current			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC} −2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100 μA

Note 1. V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} increases in proportion to V_{GG} duty cycle.
Note 2. Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay		.700	1	µs
t_{DVGG}	Clocked V_{GG} set up	1			µs
t_{CS}	Chip select delay			200	ns
t_{CO}	Output delay from $\overline{CS}$			500	ns
t_{OD}	Output deselect			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	µs

Note 1. The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Capacitance* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		5	10	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		5	10	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Clocked V_{GG} Mode)			30	pF	

*This parameter is periodically sampled and is not 100% tested.

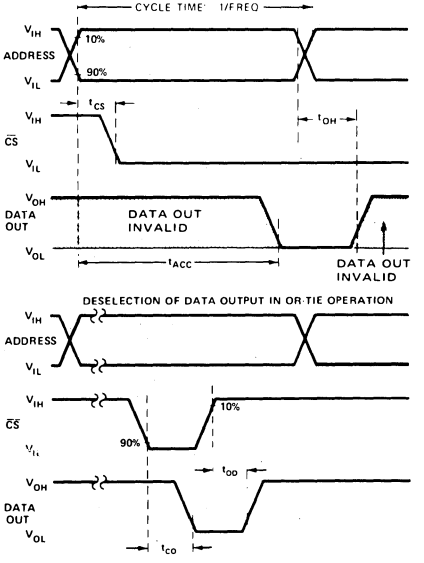
Switching Characteristics

Conditions of Test:

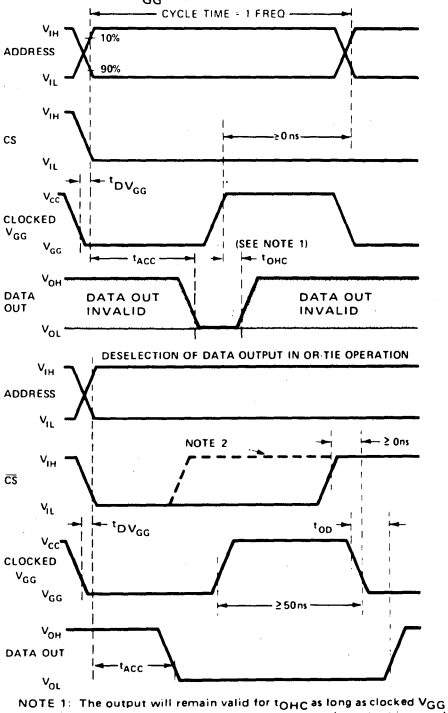
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD} ≤15 ns)

A) Constant V_{GG} Operation



B) Clocked V_{GG} Operation



NOTE 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

NOTE 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

8308

8192 BIT STATIC MOS READ ONLY MEMORY
Organization -- 1024 Words x 8 Bits

- Fast Access — 450 ns
- Directly Compatible with 8080 CPU at Maximum Processor Speed
- Two Chip Select Inputs for Easy Memory Expansion
- Directly TTL Compatible — All Inputs and Outputs
- Three State Output — OR-Tie Capability
- Fully Decoded
- Standard Power Supplies +12V DC, ±5V DC

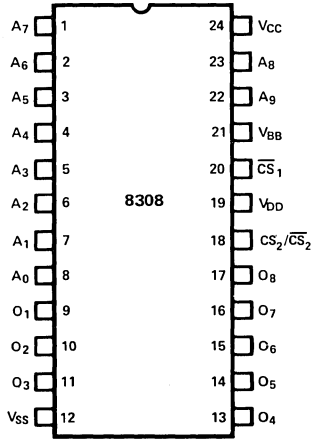
The Intel® 8308 is an 8,192 bit static MOS mask programmable Read Only Memory organized as 1024 words by 8-bits. This ROM is designed for 8080 microcomputer system applications where high performance, large bit storage, and simple interfacing are important design objectives. The inputs and outputs are fully TTL compatible.

A pin for pin compatible electrically programmed erasable ROM, the Intel® 8708, is available for system development and small quantity production use.

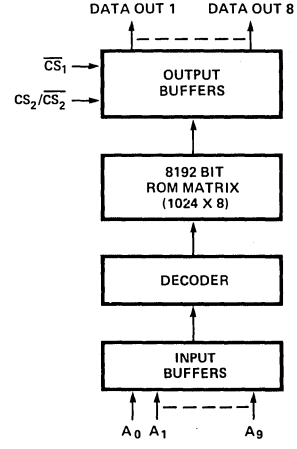
Two Chip Selects are provided — $\overline{CS}_1$ which is negative true, and $CS_2/\overline{CS}_2$ which may be programmed either negative or positive true at the mask level.

The 8308 read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0- A_9	ADDRESS INPUTS
O_1- O_8	DATA OUTPUTS
$\overline{CS}_1$, CS_2	CHIP SELECT INPUTS

MCS-80

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To V_{BB} . . . . . -0.3V to 20V
Power Dissipation . . . . . 1.0 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

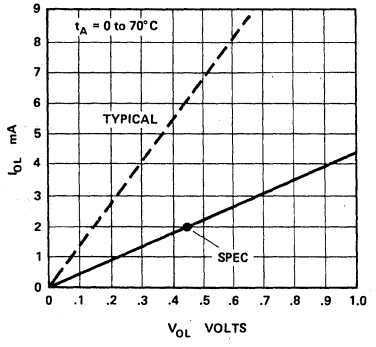
D.C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%; V_{DD} = 12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V Unless Otherwise Specified.

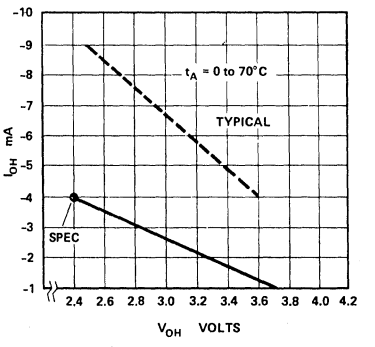
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins Except $\overline{CS}_1$)			10	μA	V_{IN} = 0 to 5.25V
I_{LCL}	Input Load Current on $\overline{CS}_1$			1.6	mA	V_{IN} = 0.45V
I_{LPC}	Input Peak Load Current on $\overline{CS}_1$			4	mA	V_{IN} = 0.8V to 3.3V
I_{LKC}	Input Leakage Current on $\overline{CS}_1$			10	μA	V_{IN} = 3.3V to 5.25V
I_{LO}	Output Leakage Current			10	μA	Chip Deselected
V_{IL}	Input "Low" Voltage	V_{SS}-1		0.8V	V	
V_{IH}	Input "High" Voltage	3.3		V_{CC}+1.0	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2mA
V_{OH1}	Output "High" Voltage	2.4			V	I_{OH} = -4mA
V_{OH2}	Output "High" Voltage	3.7			V	I_{OH} = -1mA
I_{CC}	Power Supply Current V_{CC}		.8	2	mA	
I_{DD}	Power Supply Current V_{DD}		32	60	mA	
I_{BB}	Power Supply Current V_{BB}		10μA	1	mA	
P_D	Power Dissipation			775	mW	

NOTE 1: Typical values for T_A = 25°C and nominal supply voltage

D.C. OUTPUT CHARACTERISTICS



D.C. OUTPUT CHARACTERISTICS



A.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$; $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Specified.

Symbol	Parameter	Limits[2]			Unit
		Min.	Typ.	Max.	
t_{ACC}	Address to Output Delay Time		200	450	ns
t_{CO1}	Chip Select 1 to Output Delay Time		85	160	ns
t_{CO2}	Chip Select 2 to Output Delay Time		125	220	ns
t_{DF}	Chip Deselect to Output Data Float Time		125	220	ns

NOTE 2: Refer to conditions of Test for A.C. Characteristics. Add 50 nanoseconds (worst case) to specified values at $V_{OH} = 3.7V$ @ $I_{OH} = -1mA$, $C_L = 100pF$.

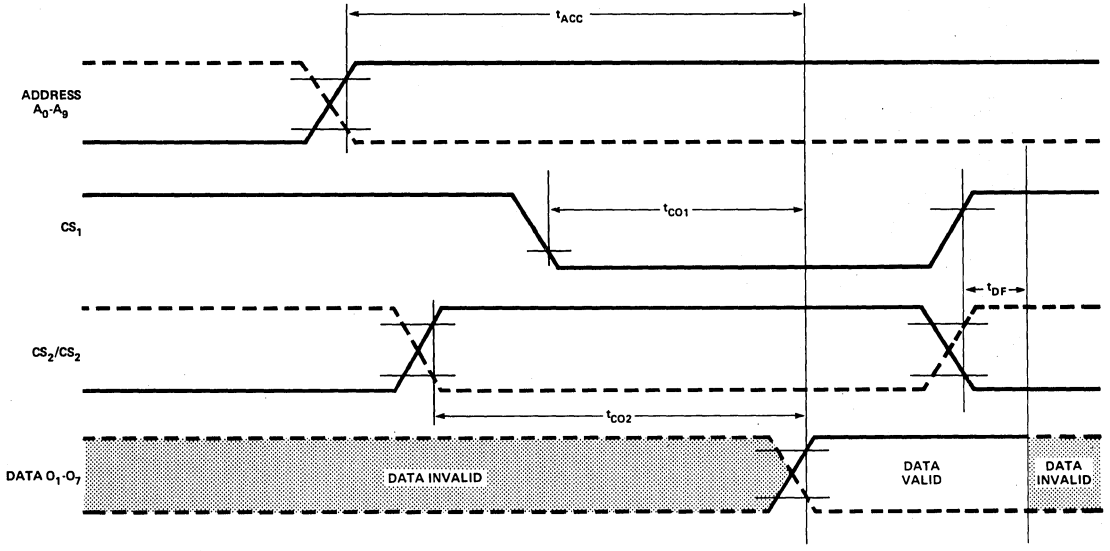
CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . . 1 TTL Gate, and $C_{LOAD} = 100pF$
Input Pulse Levels . . . . . .65V to 3.3V
Input Pulse Rise and Fall Times . . . . . 20 nsec
Timing Measurement Reference Level
. . . . . 2.4V V_{IH}, V_{OH}; 0.8V V_{IL}, V_{OL}

CAPACITANCE

$T_A = 25°C$, f = 1 MHz, $V_{BB} = -5V$, V_{DD}, V_{CC} and all other pins tied to V_{SS}.

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	Input Capacitance		6pF
C_{OUT}	Output Capacitance		12pF



8316A

16,384 BIT STATIC MOS READ ONLY MEMORY
Organization—2048 Words x 8 Bits
Access Time-850 ns max

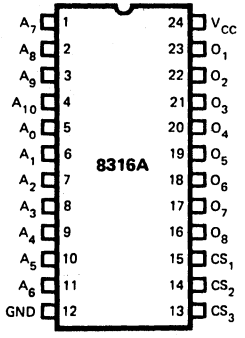
- **Single +5 Volts Power Supply Voltage**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Low Power Dissipation of 31.4 μW/Bit Maximum**
- **Three Programmable Chip Select Inputs for Easy Memory Expansion**
- **Three-State Output — OR-Tie Capability**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**

The Intel® 8316A is a 16,384-bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for microcomputer memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

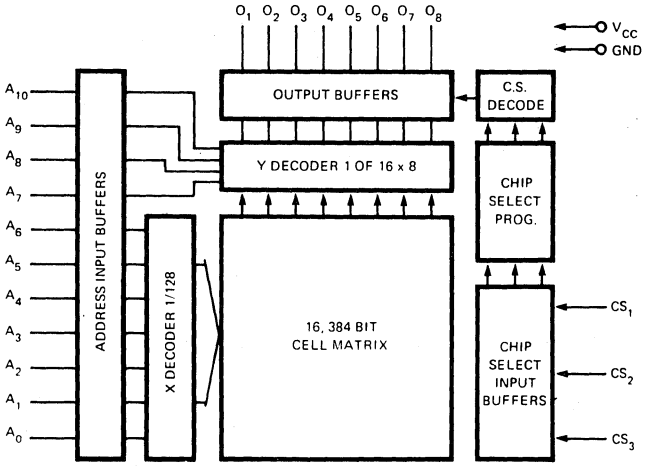
The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.

The 8316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
CS_1-CS_3	PROGRAMMABLE CHIP SELECT INPUTS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	μA	CS = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			-20	μA	CS = 2.2V, V_{OUT} = 0.45V
I_{CC}	Power Supply Current		40	98	mA	All inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100 μA

(1) Typical values for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_A	Address to Output Delay Time		400	850	nS
t_{CO}	Chip Select to Output Enable Delay Time			300	nS
t_{DF}	Chip Deselect to Output Data Float Delay Time	0		300	nS

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . 1 TTL Gate, and C_{LOAD} = 100 pF
Input Pulse Levels . . . . . 0.8 to 2.0V
Input Pulse Rise and Fall Times . (10% to 90%) 20 nS
Timing Measurement Reference Level
Input 1.5V
Output . . . . . 0.45V to 2.2V

CAPACITANCE(2) T_A = 25°C, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

(2) This parameter is periodically sampled and is not 100% tested.

8101-2

1024 BIT (256 x 4) STATIC MOS RAM WITH SEPARATE I/O

- **256 x 4 Organization to Meet Needs for Small System Memories**
- **Access Time — 850 nsec Max.**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Simple Memory Expansion — Chip Enable Input**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 22 Pin Plastic Dual-In-Line Configuration**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**
- **Output Disable Provided for Ease of Use in Common Data Bus Systems**

The Intel® 8101-2 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 8101-2 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

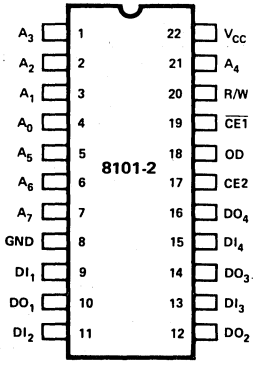
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bidirectional logic.

The Intel® 8101-2 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

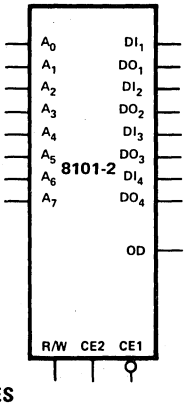
Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

MCS-80

PIN CONFIGURATION



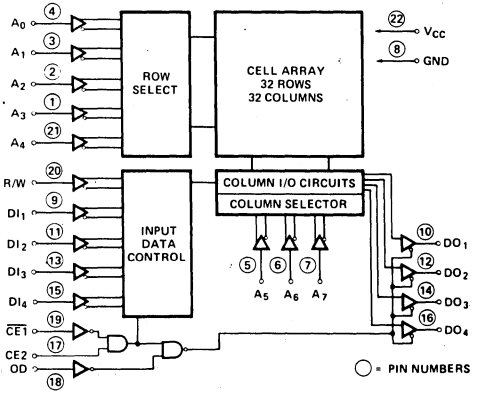
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	OD	OUTPUT DISABLE
$A_0 - A_7$	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70° C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

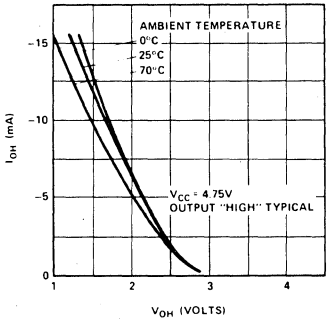
D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

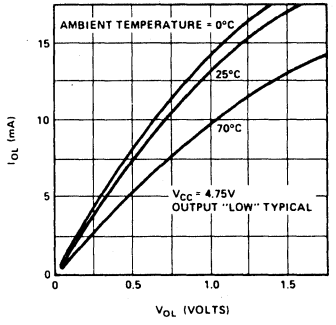
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current[2]			15	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	I/O Leakage Current[2]			-50	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150 μA

NOTE: 1. Typical values are for T_A = 25° C and nominal supply voltage.
2. Input and Output tied together.

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RCY}	Read Cycle	850			ns	(See below)
t_A	Access Time			850	ns	
t_{CO}	Chip Enable To Output			650	ns	
t_{OD}	Output Disable To Output			550	ns	
t_{DF} [1]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Data Read Valid after change of Address	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WCY}	Write Cycle	850			ns	(See below)
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	750			ns	
t_{DW}	Data Setup	500			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	630			ns	
t_{WR}	Write Recovery	50			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and C_L = 100pF

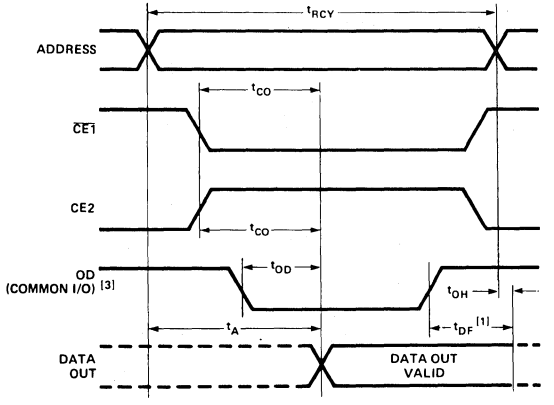
Capacitance $T_A = 25°C$, f = 1MHz

Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

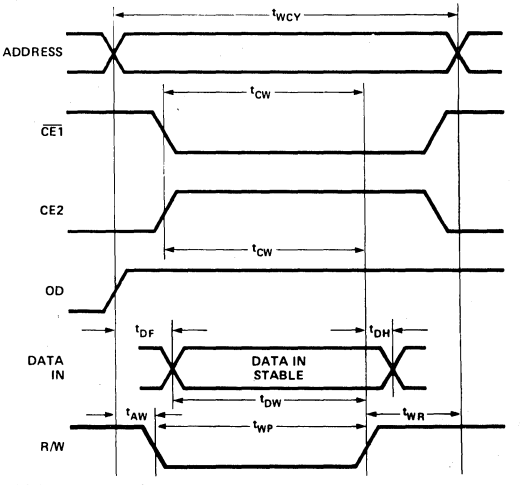
MCS-80

Waveforms

READ CYCLE



WRITE CYCLE [2]



NOTES: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.
2. During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
3. OD should be tied low for separate I/O operation.

8101A-4

1024 BIT (256 x 4) STATIC MOS RAM WITH SEPARATE I/O

- **256 x 4 Organization to Meet Needs for Small System Memories**
- **Access Time — 450 nsec Max.**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Simple Memory Expansion — Chip Enable Input**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 22 Pin Plastic Dual-In-Line Configuration**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**
- **Output Disable Provided for Ease of Use in Common Data Bus Systems**

The Intel® 8101A-4 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

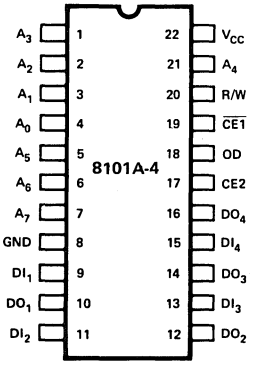
The 8101A-4 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single+5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bidirectional logic.

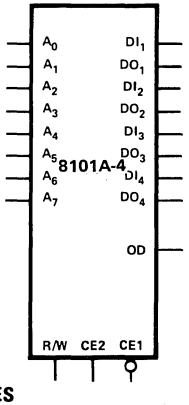
The Intel® 8101A-4 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



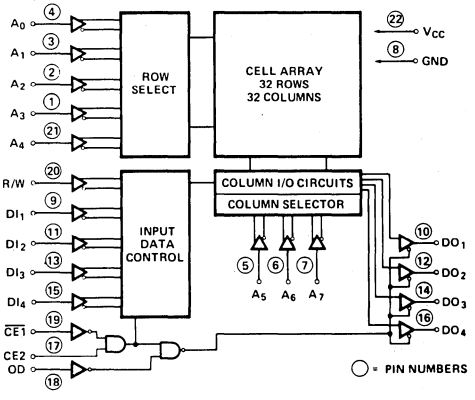
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	OD	OUTPUT DISABLE
$A_0 - A_7$	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

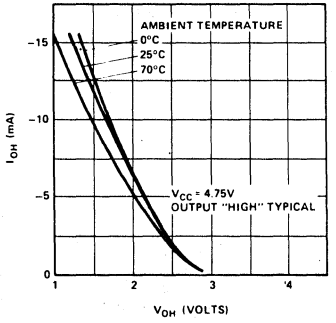
D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

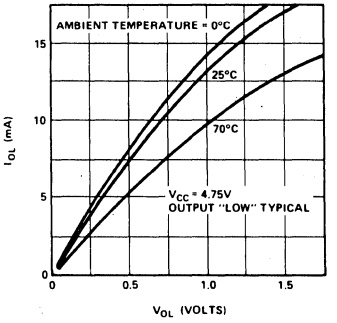
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current[2]			5	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	I/O Leakage Current[2]			−10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	55	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			60	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -150 μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Input and Output tied together.

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RCY}	Read Cycle	450			ns	(See below)
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [1]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Data Read Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WCY}	Write Cycle	270			ns	(See below)
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

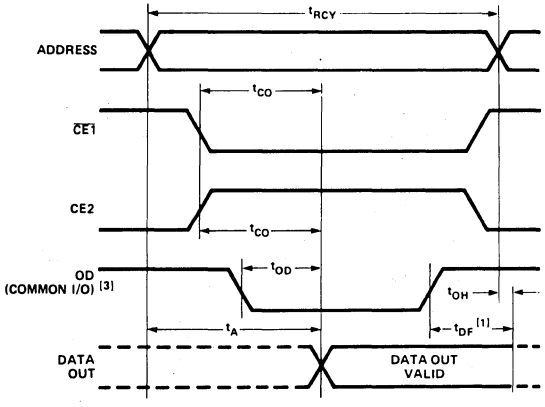
Output Load: 1 TTL Gate and $C_L = 100pF$

Capacitance $T_A = 25°C$, f = 1MHz

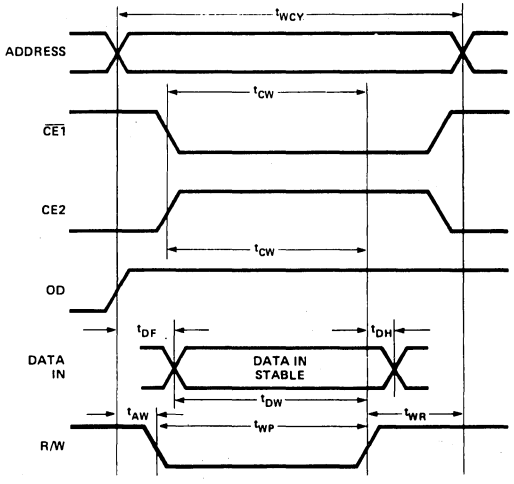
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	8	12

Waveforms

READ CYCLE



WRITE CYCLE [2]



NOTES: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.
2. During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
3. OD should be tied low for separate I/O operation.

8111-2

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

- **Organization 256 Words by 4 Bits**
- **Access Time — 850 nsec Max.**
- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 18 Pin Plastic Dual-In-Line Configuration**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**

The Intel®8111-2 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 8111-2 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

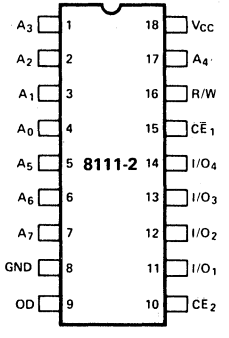
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

The Intel®8111-2 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

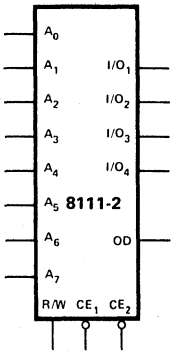
Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

MCS-80

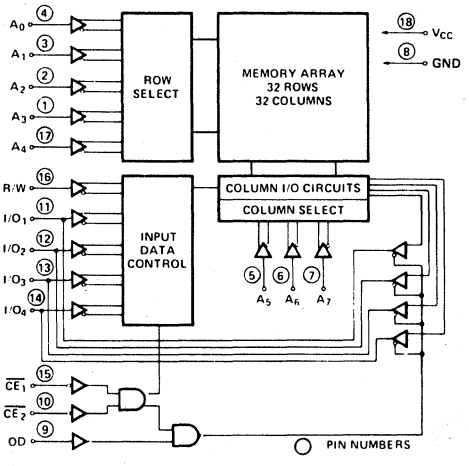
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1-I/O_4	DATA INPUT/OUTPUT

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

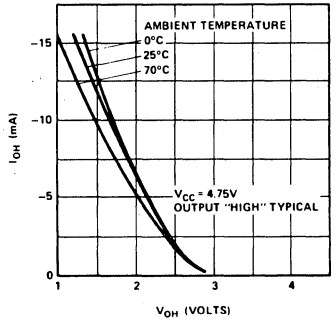
D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

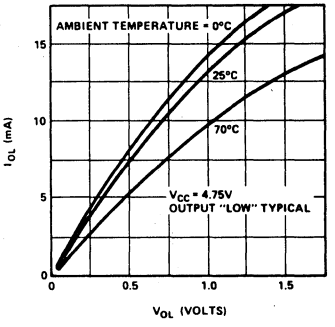
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		+0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.2			V	I_{OH} = -150 μA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RCY}	Read Cycle	850			ns	(See below)
t_A	Access Time			850	ns	
t_{CO}	Chip Enable To Output			650	ns	
t_{OD}	Output Disable To Output			550	ns	
t_{DF} [1]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Data Read Valid after change of Address	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WCY}	Write Cycle	850			ns	(See below)
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	750			ns	
t_{DW}	Data Setup	500			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	630			ns	
t_{WR}	Write Recovery	50			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

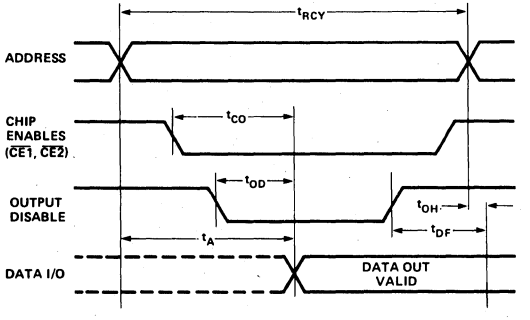
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance T_A = 25°C, f = 1MHz

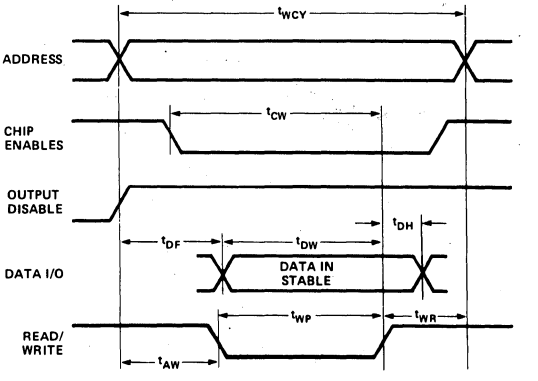
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	10	15

Waveforms

READ CYCLE



WRITE CYCLE



NOTE: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $\overline{CE2}$, or OD, whichever occurs first.

MCS-80

8111A-4

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

- **Organization 256 Words by 4 Bits**
- **Access Time — 450 nsec Max.**
- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 18 Pin Plastic Dual-In-Line Configuration**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**

The Intel® 8111A-4 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 8111A-4 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

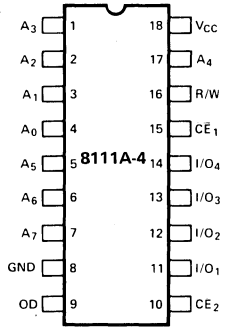
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

The Intel® 8111A-4 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

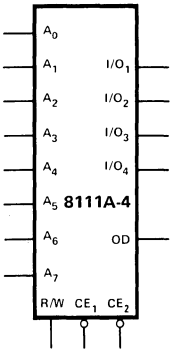
Intel's silicon gate technology also provides excellent protection against communication. This permits the use of low cost silicone packaging.

MCS-80

PIN CONFIGURATION



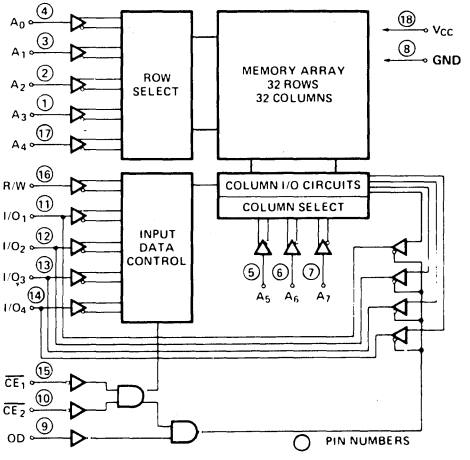
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1-I/O_4	DATA INPUT/OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

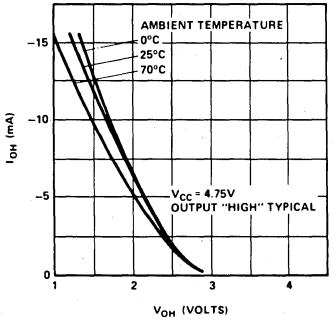
D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

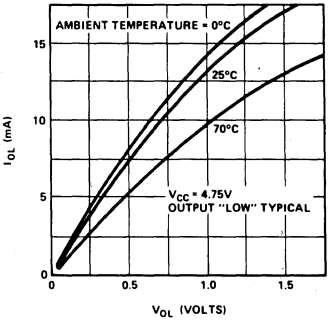
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			5	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-10	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	55	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			60	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -150 μA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RCY}	Read Cycle	450			ns	(See below)
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [1]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Data Read Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WCY}	Write Cycle	270			ns	(See below)
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

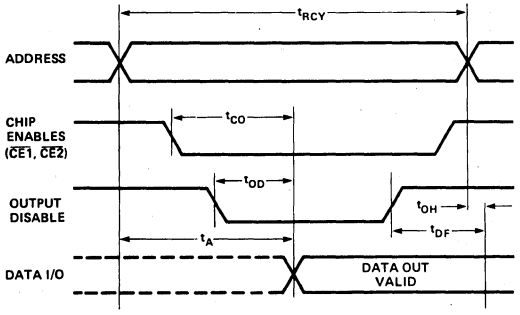
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance $T_A = 25°C$, f = 1MHz

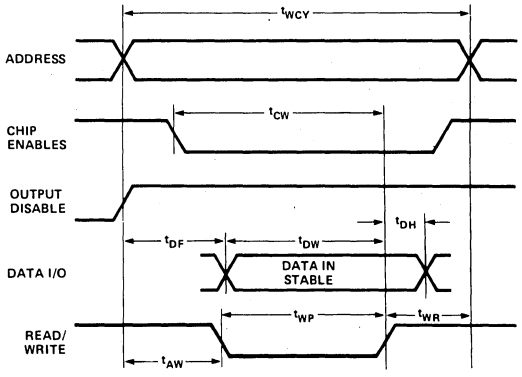
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	10	15

Waveforms

READ CYCLE



WRITE CYCLE



NOTE: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $\overline{CE2}$, or OD, whichever occurs first.

MCS-80

8102A-4
1024 BIT STATIC MOS RAM

- **Access Time — 450 ns Max.**
- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 16 Pin Plastic Dual-In-Line Configuration**

The Intel®8102A-4 is a 1024 word by one bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 8102A-4 is designed for microcomputer memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

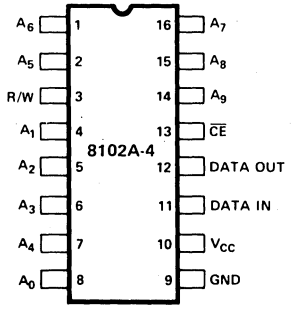
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel®8102A-4 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

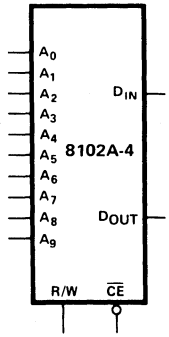
Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

MCS-80

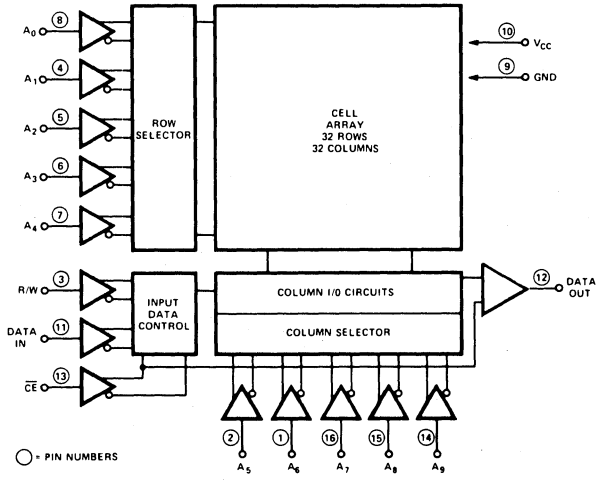
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	$\overline{CE}$	CHIP ENABLE
A_0-A_9	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

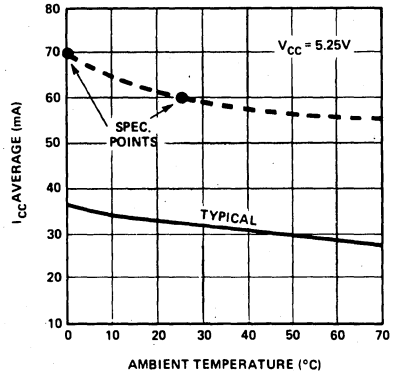
T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	OUTPUT LEAKAGE CURRENT			5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	OUTPUT LEAKAGE CURRENT			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC1}	POWER SUPPLY CURRENT		30	50	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 25°C
I_{CC2}	POWER SUPPLY CURRENT			55	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 0°C
V_{IL}	INPUT "LOW" VOLTAGE	−0.5		0.8	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			0.4	V	I_{OL} = 2.1mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.4			V	I_{OH} = −100μA

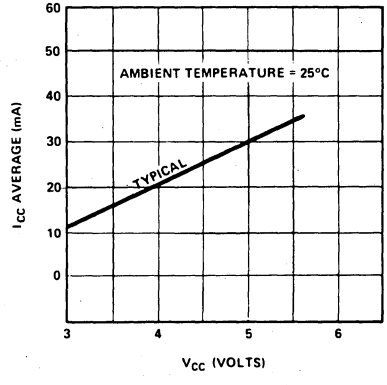
(1) Typical values are for T_A = 25°C and nominal supply voltage.

TYPICAL D.C. CHARACTERISTICS

POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



MCS-80

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
READ CYCLE					
t_{RC}	Read Cycle	450			ns
t_A	Access Time			450	ns
t_{CO}	Chip Enable to Output Time			230	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	450			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	300			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	300			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	300			ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CONDITIONS OF TEST

Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

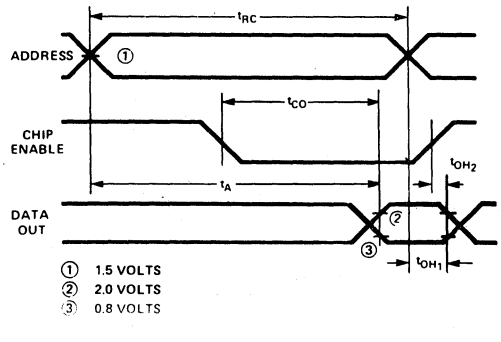
Capacitance[2] T_A = 25°C, f = 1MHz

SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

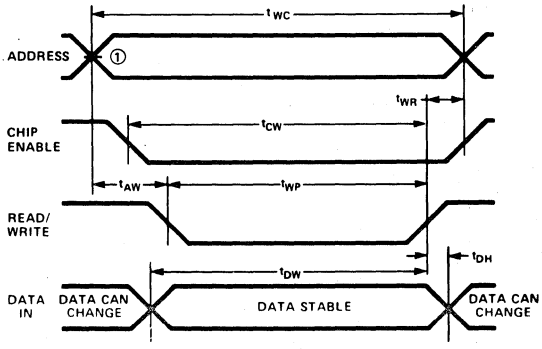
NOTE: 2. This parameter is periodically sampled and is not 100% tested.

Waveforms

READ CYCLE



WRITE CYCLE



MCS-80

8107B-4

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

* Access Time -- 270 ns max.
* Read, Write Cycle Times -- 470 ns max.
* Refresh Period -- 2 ms

- Low Cost Per Bit
- Low Standby Power
- Easy System Interface
- Only One High Voltage Input Signal — Chip Enable
- TTL Compatible -- All Address, Data, Write Enable, Chip Select Inputs
- Read-Modify-Write Cycle Time -- 590 ns
- Address Registers Incorporated on the Chip
- Simple Memory Expansion — Chip Select Input Lead
- Fully Decoded — On Chip Address Decode
- Output is Three State and TTL Compatible
- Industry Standard 22-Pin Configuration

The Intel 8107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 8107B uses dynamic circuitry which reduces the standby power dissipation.

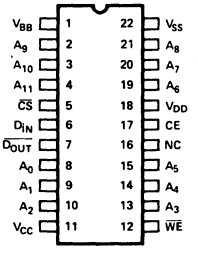
Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 8107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 8107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 8107B.

MCS-80

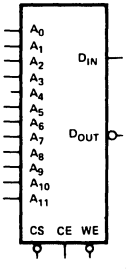
PIN CONFIGURATION

8107B



LOGIC SYMBOL

8107B

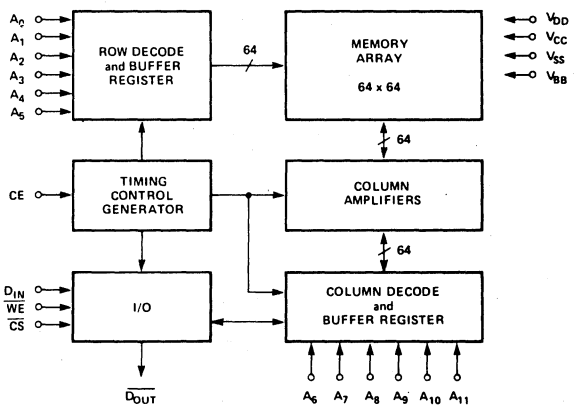


PIN NAMES

A_0-A_{11}	ADDRESS INPUTS*	V_{BB}	POWER (-5V)
CE	CHIP ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	V_{DD}	POWER (+12V)
D_{IN}	DATA INPUT	V_{SS}	GROUND
$\overline{D_{OUT}}$	DATA OUTPUT	$\overline{WE}$	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A_0-A_5.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65° C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . . +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} . . . . . +20V to −0.3V

Power Dissipation 1.25W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

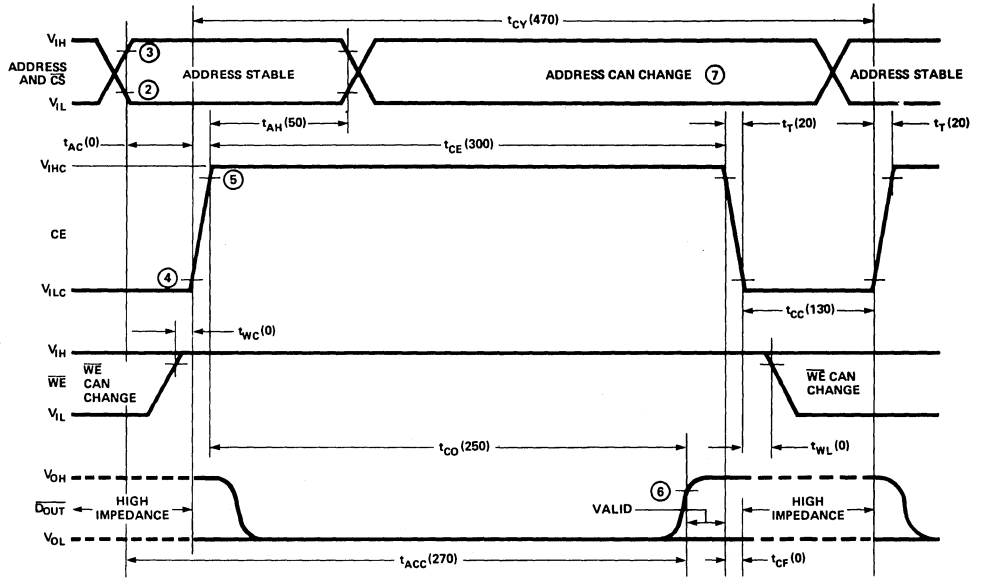
T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB}[1] = -5V ± 5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200	μA	CE = -1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on		80	100	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\ AV1}$	Average V_{DD} Current		55	80	mA	Cycle time=470ns, t_{CE} = 300ns — T_A = 25°C
$I_{DD\ AV2}$	Average V_{DD} Current		27	40	mA	Cycle time=1000ns, t_{CE} = 300ns — T_A = 25°C
I_{CC1}[4]	V_{GC} Supply Current during CE off		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB}	V_{BB} Supply Current		5	100	μA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	t_T = 20ns — See Figure 4
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0mA

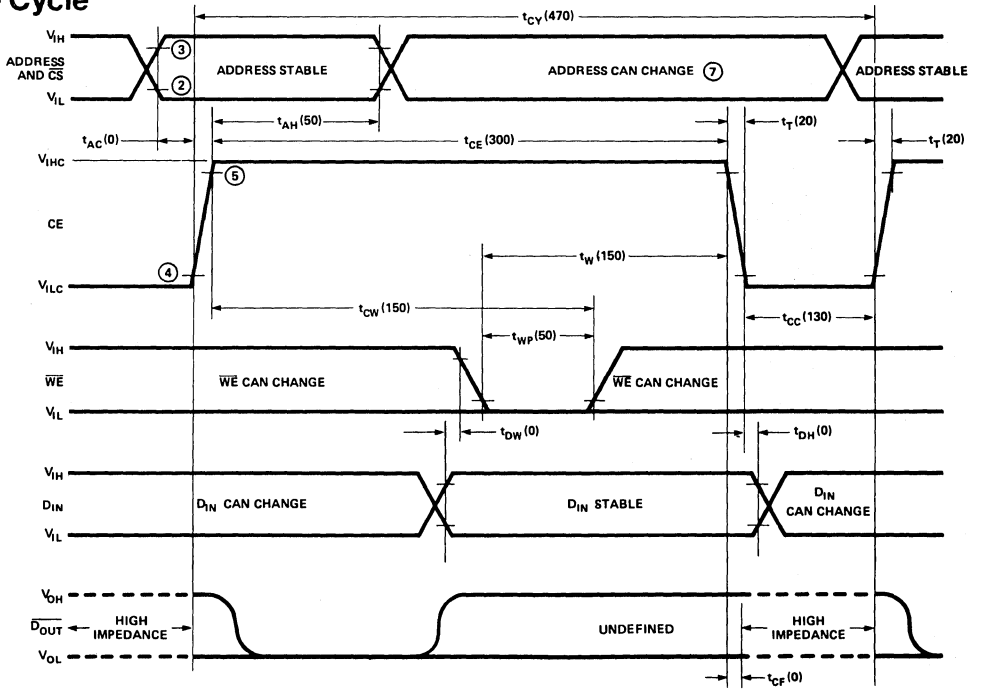
NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

Read and Refresh Cycle [1] (Numbers in parentheses are for minimum cycle timing in ns)



Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to CE Set Up Time	0		ns	t_{AC} is measured from end of address transition
t_{AH}	Address Hold Time	100		ns	
t_{CC}	CE Off Time	130		ns	
t_T	CE Transition Time	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	470		ns	$t_T = 20ns$
t_{CE}	CE On Time	300	4000	ns	
t_{CO}	CE Output Delay		250	ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{ACC}	Address to Output Access		270	ns	Ref = 2.0V.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	470		ns	$t_T = 20ns$
t_{CE}	CE On Time	300	4000	ns	
t_W	$\overline{WE}$ to CE Off	150		ns	
t_{CW}	CE to $\overline{WE}$	150		ns	
t_{DW} [2]	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	

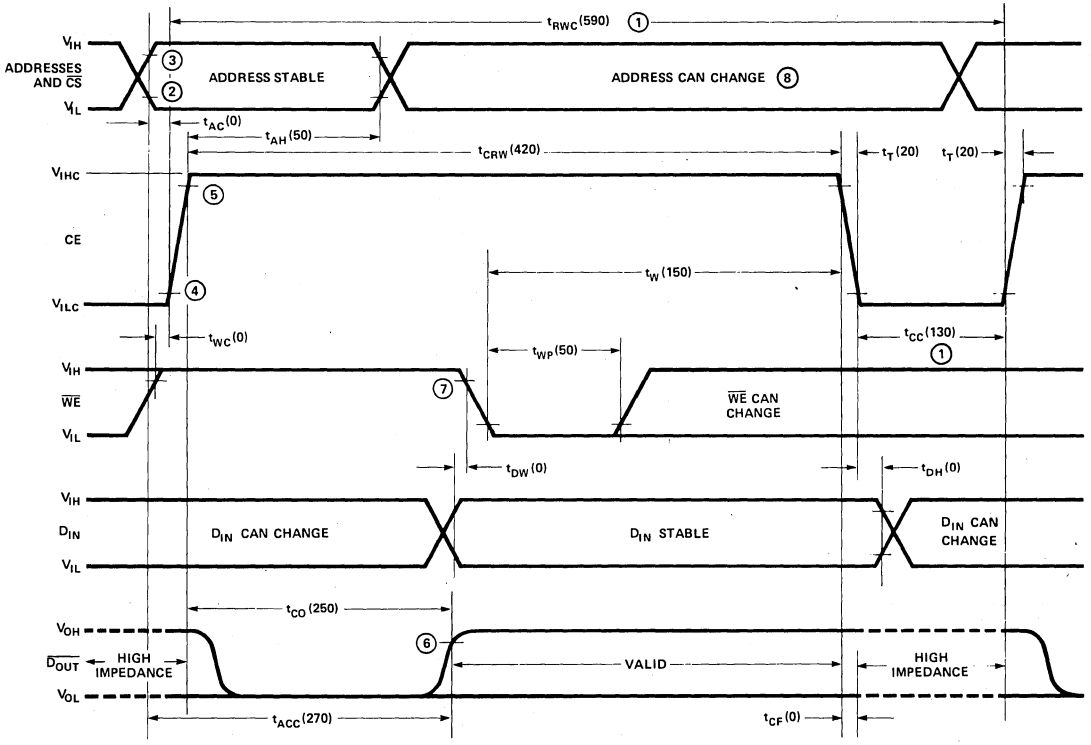
Read Modify Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	Read Modify Write(RMW) Cycle Time	590		ns	$t_T = 20ns$
t_{CRW}	CE Width During RMW	420	4000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	150		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	Ref = 2.0V
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		250	ns	
t_{ACC}	Access Time		270	ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

Read Modify Write Cycle[1]

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	Read Modify Write(RMW) Cycle Time	590		ns	t_T = 20ns
t_{CRW}	CE Width During RMW	420	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	150		ns	C_{load} = 50pF, Load = One TTL Gate, Ref = 2.0V
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		250	ns	
t_{ACC}	Access Time		270	ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

(Numbers in parentheses are for minimum cycle timing in ns.)



NOTES:
1. A.C. characteristics are guaranteed only if cumulative CE on time during t_{REF} is ⩽65% of t_{REF}. For continuous Read-Modify-Write operation, t_{CC} and t_{RWC} should be increased to at least 185ns and 645ns, respectively.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

intel®

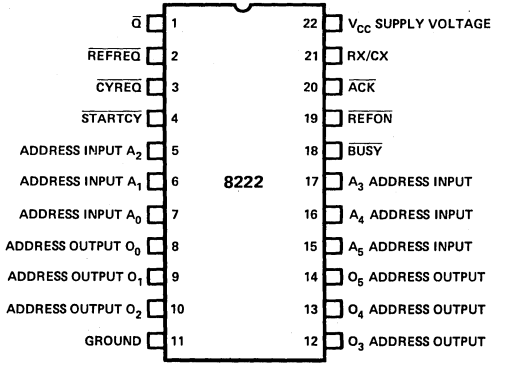
8222

DYNAMIC MEMORY REFRESH CONTROLLER

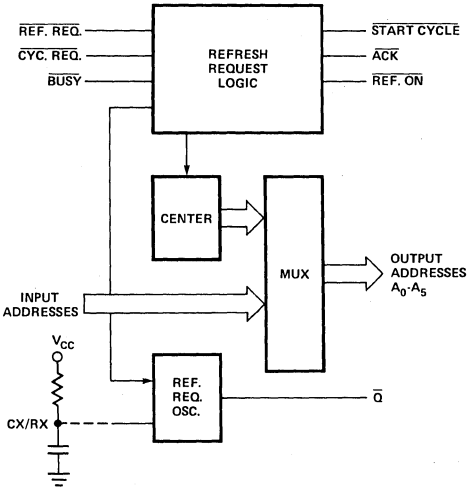
- Adjustable Refresh Request Oscillator
- Ideal for 8107A, 8107B 4K RAM Refresh
- Internal Address Multiplexer
- Up to 6 Row Input Addresses (64 x 64 Organization)

The 8222 is a refresh controller for dynamic RAMs requiring row refresh of up to 6 row input addresses (or 4K bits for 64 x 64 organization). The device contains an accurate refresh timer (whose frequency can be set by an external resistor and capacitor) plus all necessary control and I/O circuitry to provide for the refresh requirements of dynamic RAMs. The chip's high performance makes it especially suitable for use with high speed N-channel RAMs like the 8107B. The 8222 is designed for large, asynchronously driven, dynamic memory systems.

PIN CONFIGURATION



BLOCK DIAGRAM



MCS-80

8212

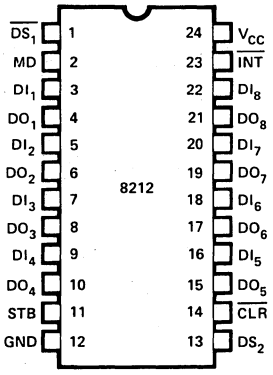
EIGHT-BIT INPUT/OUTPUT PORT

- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current — .25 mA Max.**
- **Three State Outputs**
- **Outputs Sink 15 mA**
- **3.65V Output High Voltage for Direct Interface to 8080 CPU or 8008 CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches and Multiplexers in Microcomputer Systems**
- **Reduces System Package Count**

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

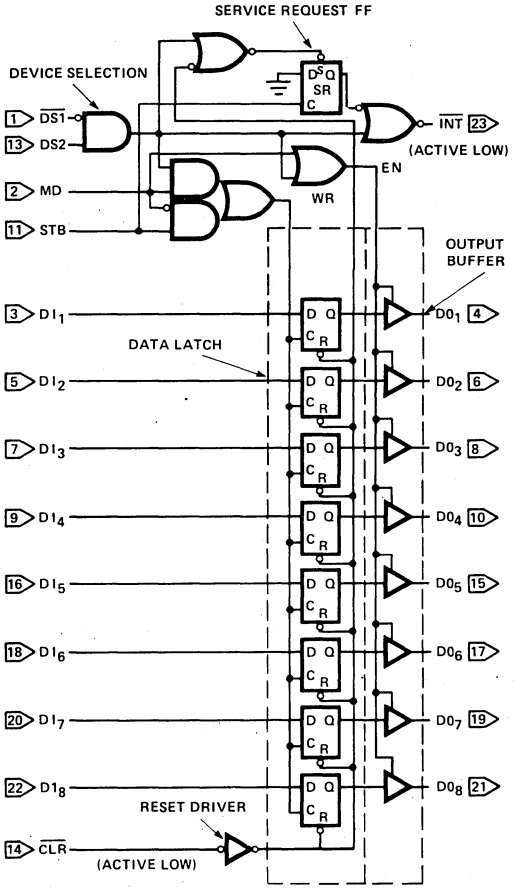
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



MCS-80

Absolute Maximum Ratings*

Temperature Under Bias Plastic . . −65°C to +75°C
Storage Temperature . . . . . −65°C to +160°C
All Output or Supply Voltages . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −1.0 to 5.5 Volts
Output Currents . . . . . 125 mA

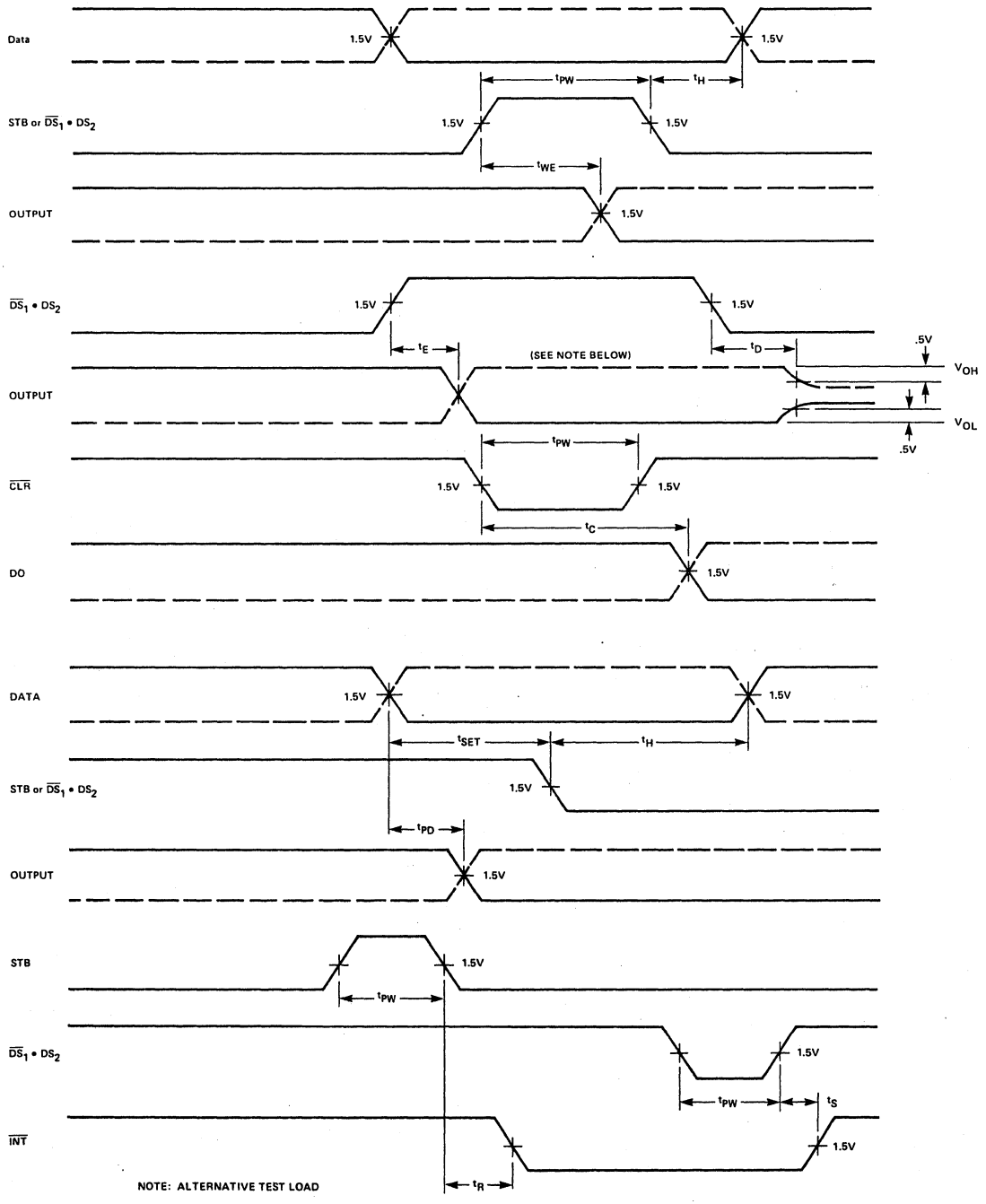
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

T_A = 0°C to +75°C V_{CC} = +5V ±5%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current ACK, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	V_R = 5.25V
I_R	Input Leakage Current MO Input			30	μA	V_R = 5.25V
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = 5.25V
V_C	Input Forward Voltage Clamp			−1	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 15 mA
V_{OH}	Output "High" Voltage	3.65	4.0		V	I_{OH} = −1 mA
I_{SC}	Short Circuit Output Current	-15		-75	mA	V_O = 0 V
I_O	Output Leakage Current High Impedance State			20	μA	V_O = .45V/5.25V
I_{CC}	Power Supply Current		90	130	mA	

Timing Diagram



A.C. Characteristics

T_A = 0°C to +75°C V_{CC} = +5V ± 5%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{pw}	Pulse Width	30			ns	
t_{pd}	Data To Output Delay			30	ns	
t_{we}	Write Enable To Output Delay			40	ns	
t_{set}	Data Setup Time	15			ns	
t_h	Data Hold Time	20			ns	
t_r	Reset To Output Delay			40	ns	
t_s	Set To Output Delay			30	ns	
t_e	Output Enable/Disable Time			45	ns	
t_c	Clear To Output Delay			55	ns	

CAPACITANCE* F = 1 MHz V_{BIAS} = 2.5V V_{CC} = +5V T_A = 25°C

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	DS_1 MD Input Capacitance	9 pF	12 pF
C_{IN}	DS_2, CK, ACK, DI_1-DI_8 Input Capacitance	5 pF	9 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	12 pF

*This parameter is sampled and not 100% tested.

MCS-80

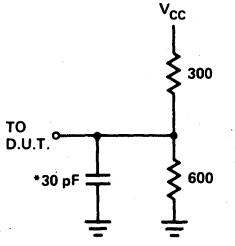
Switching Characteristics

CONDITIONS OF TEST

Input Pulse Amplitude = 2.5 V
Input Rise and Fall Times 5 ns
Between 1V and 2V Measurements made at 1.5V
with 15 mA & 30 pF Test Load

TEST LOAD

15mA & 30pF



* INCLUDING JIG & PROBE CAPACITANCE

8255

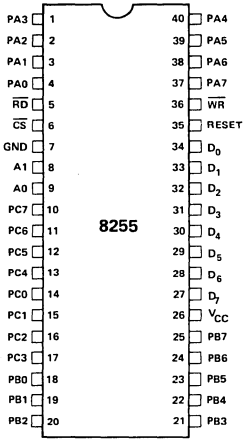
PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with MCS™-8 and MCS™-80 Microprocessor Families**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40 Pin Dual In-Line Package**
- **Reduces System Package Count**

The 8255 is a general purpose programmable I/O device designed for use with both the 8008 and 8080 microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bidirectional Bus mode which uses 8 lines for a bidirectional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255 include bit set and reset capability and the ability to source 1mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

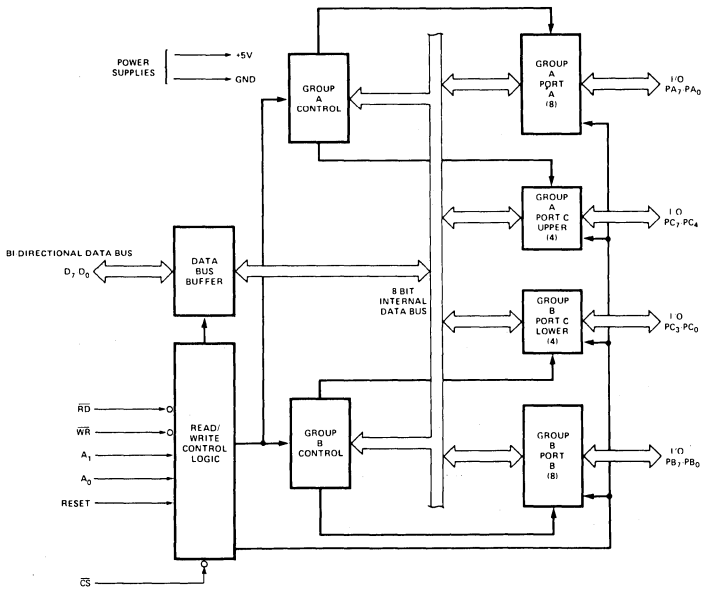
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

8255 BLOCK DIAGRAM



MCS-80

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage			.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			.4	V	$I_{OL} = 1.6mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -50\mu A$ ($-100\mu A$ for D.B. Port)
I_{OH}[1]	Darlington Drive Current		2.0		mA	$V_{OH} = 1.5V$, $R_{EXT} = 390\Omega$
I_{CC}	Power Supply Current		40		mA	

NOTE:
1. Available on 8 pins only.

MCS-80

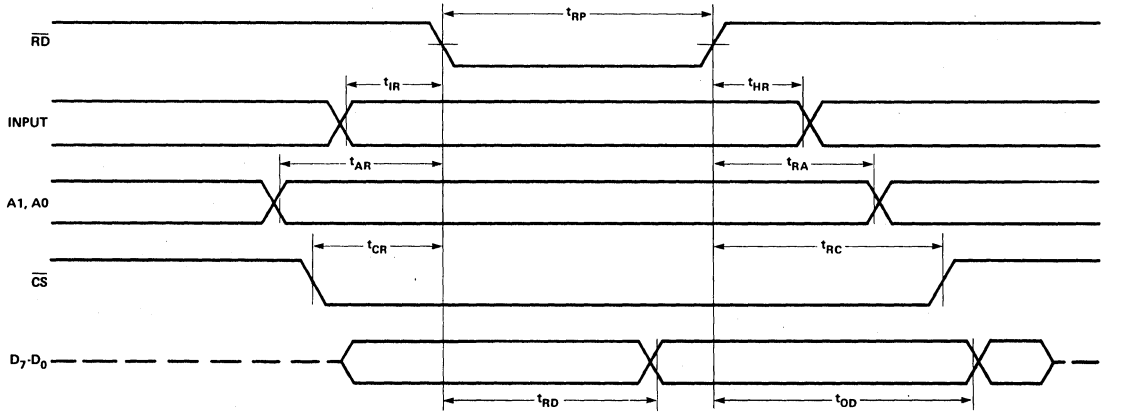
Capacitance

$T_A = 25°C$; $V_{CC} = V_{SS} = 0V$

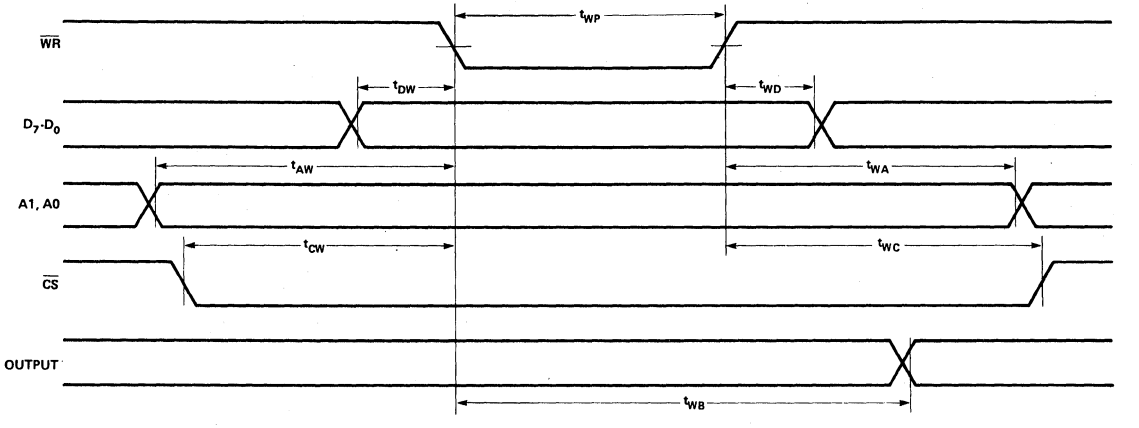
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

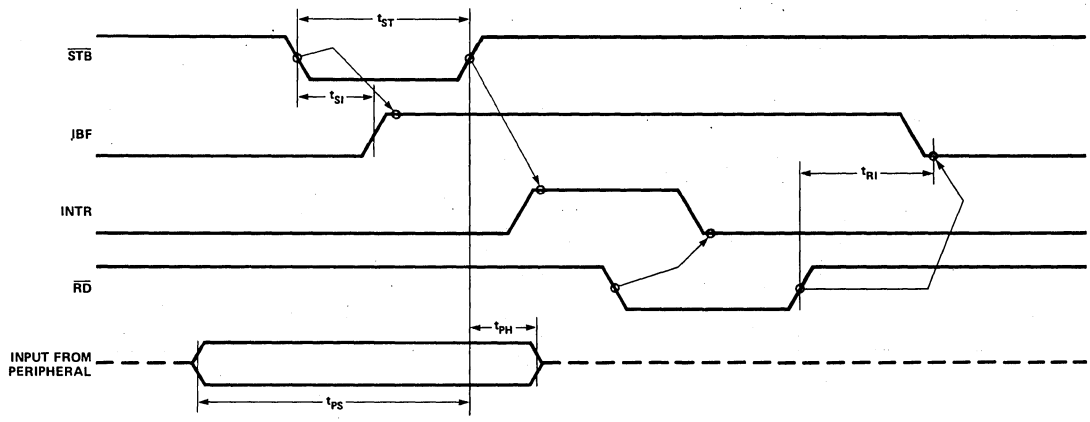
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
t_{WP}	Pulse Width of $\overline{WR}$			430	ns	
t_{DW}	Time D.B. Stable Before $\overline{WR}$	10			ns	
t_{WD}	Time D.B. Stable After $\overline{WR}$	65			ns	
t_{AW}	Time Address Stable Before $\overline{WR}$	20			ns	
t_{WA}	Time Address Stable After $\overline{WR}$	35			ns	
t_{CW}	Time CS Stable Before $\overline{WR}$	20			ns	
t_{WC}	Time CS Stable After $\overline{WR}$	35			ns	
t_{WB}	Delay From $\overline{WR}$ To Output			500	ns	
t_{RP}	Pulse Width of $\overline{RD}$	430			ns	
t_{IR}	$\overline{RD}$ Set-Up Time	50			ns	
t_{HR}	Input Hold Time	50			ns	
t_{RD}	Delay From $\overline{RD} = 0$ To System Bus	350			ns	
t_{OD}	Delay From $\overline{RD} = 1$ To System Bus	150			ns	
t_{AR}	Time Address Stable Before $\overline{RD}$	50			ns	
t_{CR}	Time $\overline{CS}$ Stable Before $\overline{RD}$	50			ns	
t_{AK}	Width Of $\overline{ACK}$ Pulse	500			ns	
t_{ST}	Width Of $\overline{STB}$ Pulse	350			ns	
t_{PS}	Set-Up Time For Peripheral	150			ns	
t_{PH}	Hold Time For Peripheral	150			ns	
t_{RA}	Hold Time for A_1, A_0 After $\overline{RD} = 1$	379			ns	
t_{RC}	Hold Time For CS After $\overline{RD} = 1$	5			ns	
t_{AD}	Time From $\overline{ACK} = 0$ To Output (Mode 2)			500	ns	
t_{KD}	Time From $\overline{ACK} = 1$ To Output Floating			300	ns	
t_{WO}	Time From $\overline{WR} = 1$ To $\overline{OBF} = 0$			300	ns	
t_{AO}	Time From $\overline{ACK} = 0$ To $\overline{OBF} = 1$			500	ns	
t_{SI}	Time From $\overline{STB} = 0$ To IBF			600	ns	
t_{RI}	Time From $\overline{RD} = 1$ To IBF = 0			300	ns	



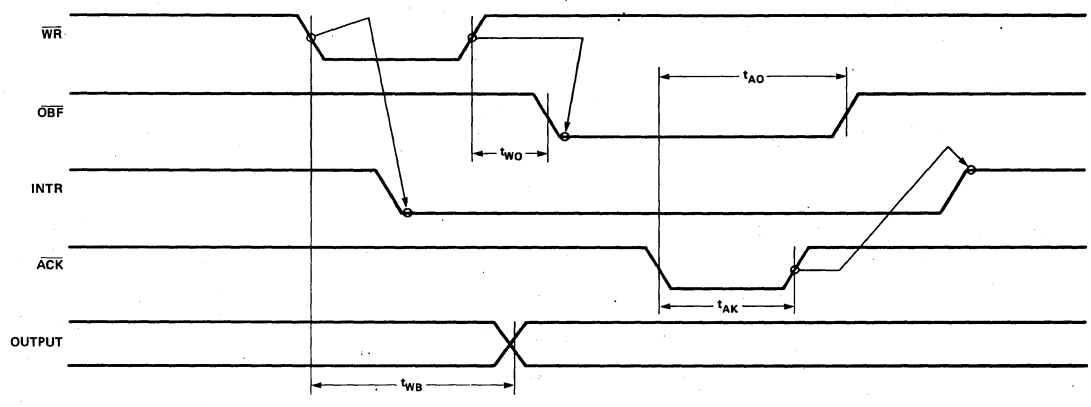
Mode 0 (Basic Input)



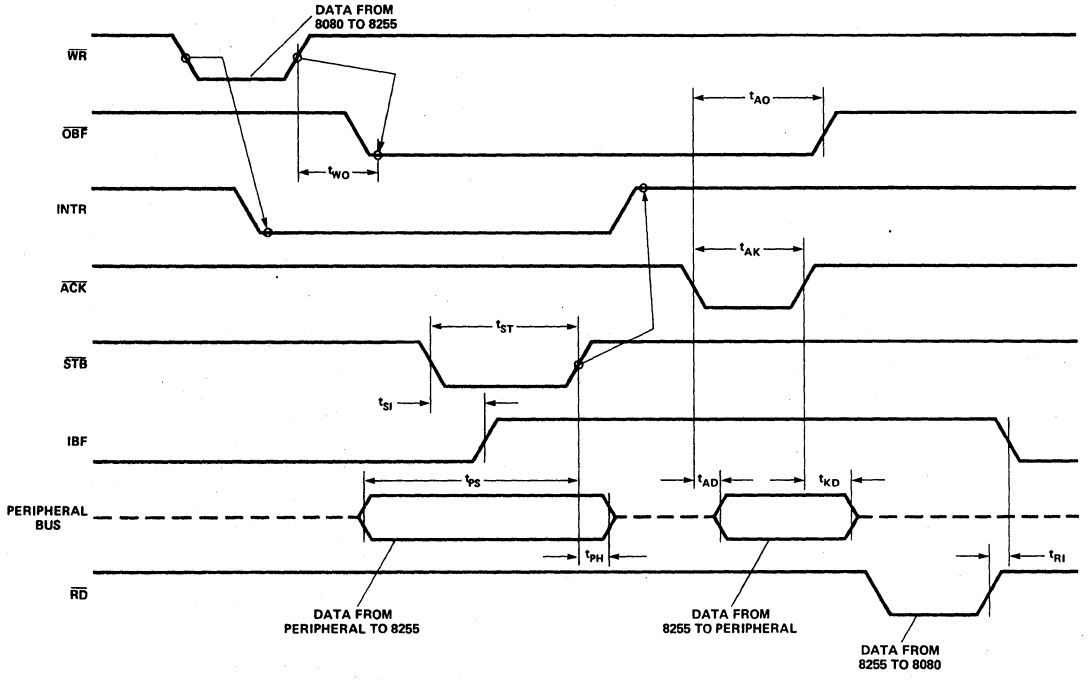
Mode 0 (Basic Output)



Mode 1 (Strobed Input)



Mode 1 (Strobed Output)



Mode 2 (Bi-directional)

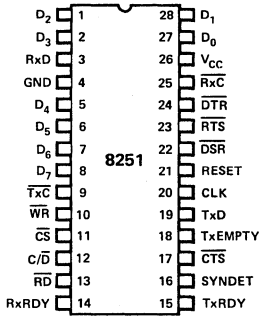
8251

PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1,16 or 64 Times Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection
- **Baud Rate —DC to 56k Baud (Sync Mode)**
  DC to 9.6k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs Are TTL Compatible**
- **Single 5 Volt Supply**
- **Single TTL Clock**

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

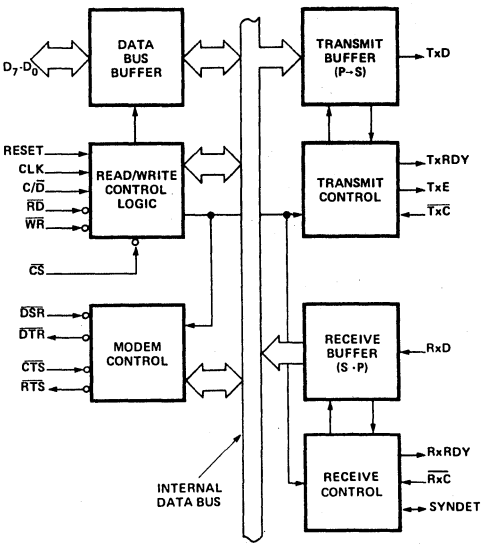
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
VCC	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



MCS-80

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Characteristics:

T_A = 0°C to 70°C; V_{CC} = 5.0V ± 5%; V_{SS} = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	V_{SS}-.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.2			V	I_{OH} = -100μA (DB_{0-7}) I_{OH} = -100μA (Others)
I_{DL}	Data Bus Leakage			–50 10	μA μA	V_{OUT} = .45V V_{OUT} = V_{CC}
I_{LI}	Input Load Current			10	μA	@ 5.5V
I_{CC}	Power Supply Current		45	80		

Capacitance

T_A = 25°C; V_{CC} = V_{SS} = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}.

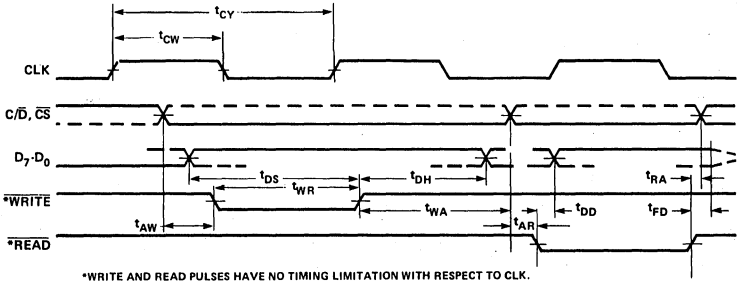
A.C. Characteristics:

$T_A = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; $V_{SS} = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	.420		1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220		300	ns	
t_R, t_F	Clock Rise and Fall Time	0		50	ns	
t_{WR}	$\overline{WRITE}$ Pulse Width	430			ns	
t_{DS}	Data Set-Up Time for $\overline{WRITE}$	200			ns	
t_{DH}	Data Hold Time for $\overline{WRITE}$	65			ns	
t_{AW}	Address Stable before $\overline{WRITE}$	20			ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	35			ns	
t_{RD}	READ Pulse Width	430			ns	
t_{DD}	Data Delay from $\overline{READ}$			350	ns	C_L=100pF
t_{DF}	$\overline{READ}$ to Data Floating	25		200	ns	C_L=100pF
t_{AR1}	Address Stable before $\overline{READ}$, CE (C/D)	50			ns	
t_{RA1}	Address Hold Time for $\overline{READ}$, CE	5			ns	
t_{RA2}	Address Hold Time for $\overline{READ}$, C/D	370			ns	
t_{DTx}	TxD Delay from Falling Edge of TxC	1			μs	C_L=100pF
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2			μs	C_L=100pF
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2			μs	C_L=100pF
f_{Tx}	Transmitter Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate	 DC DC		 56 615	 KHz KHz	
f_{Rx}	Receiver Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate	 DC DC		 56 615	 KHz KHz	
t_{Tx}	TxRDY Delay from Center of Data Bit			16	CLK Period	C_L=50pF
t_{Rx}	RxRDY Delay from Center of Data Bit	15		20	CLK Period	
t_{IS}	Internal Syndet Delay from Center of Data Bit	20		25	CLK Period	
t_{ES}	External Syndet Set-Up Time before Falling Edge of RxC			15	CLK Period	

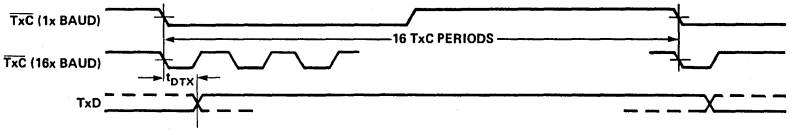
Note: The TxC and RxC frequencies have the following limitation with respect to CLK.
For ASYNC Mode, t_{Tx} or $t_{Rx} \geq 4.5\ t_{CY}$
For SYNC Mode, t_{Tx} or $t_{Rx} \geq 30\ t_{CY}$

READ AND WRITE TIMING

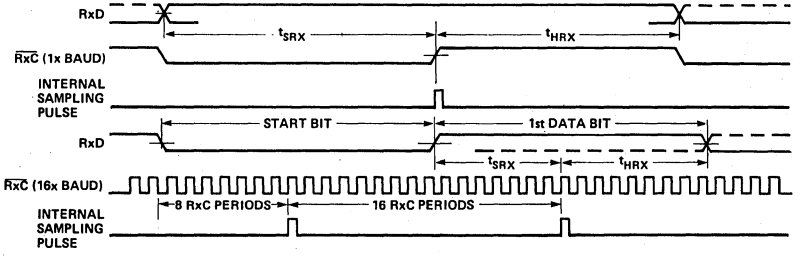


*WRITE AND READ PULSES HAVE NO TIMING LIMITATION WITH RESPECT TO CLK.

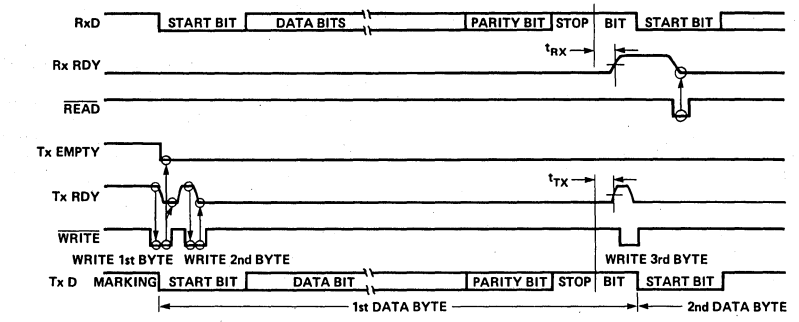
TRANSMITTER CLOCK AND DATA



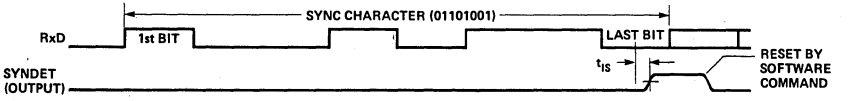
RECEIVER CLOCK AND DATA



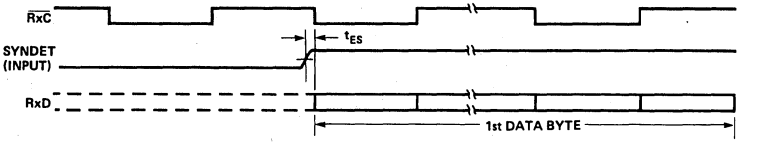
Tx RDY AND Rx RDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT



MCS-80

8205

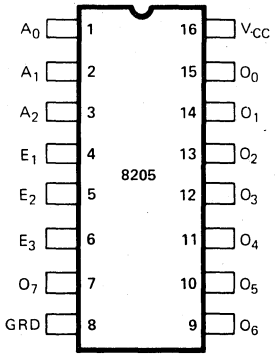
HIGH SPEED 1 OUT OF 8 BINARY DECODER

- **I/O Port or Memory Selector**
- **Simple Expansion — Enable Inputs**
- **High Speed Schottky Bipolar Technology — 18ns Max. Delay**
- **Directly Compatible with TTL Logic Circuits**
- **Low Input Load Current — .25 mA max., 1/6 Standard TTL Input Load**
- **Minimum Line Reflection — Low Voltage Diode Input Clamp**
- **Outputs Sink 10 mA min.**
- **16-Pin Dual-In-Line Ceramic or Plastic Package**

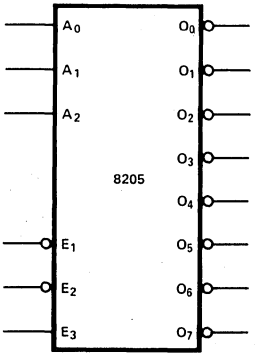
The 8205 decoder can be used for expansion of systems which utilize input ports, output ports, and memory components with active low chip select input. When the 8205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 8205 allow easy system expansion. For very large systems, 8205 decoders can be cascaded such that each decoder can drive eight other decoders for arbitrary memory expansions.

The Intel®8205 is packaged in a standard 16 pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A_0-A_2	ADDRESS INPUTS
$\overline{E_1}$-$\overline{E_3}$	ENABLE INPUTS
$\overline{O_0}$-$\overline{O_7}$	DECODED OUTPUTS

ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		125 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

8205

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	V_{CC} = 5.25V, V_F = 0.45V
I_R	INPUT LEAKAGE CURRENT		10	μA	V_{CC} = 5.25V, V_R = 5.25V
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	V_{CC} = 4.75V, I_C = −5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} = 4.75V, I_{OL} = 10.0 mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	V_{CC} = 4.75V, I_{OH} = −1.5 mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	V_{CC} = 5.0V, V_{OUT} = 0V
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	V_{CC} = 5.0V, I_{OX} = 40 mA
I_{CC}	POWER SUPPLY CURRENT		70	mA	V_{CC} = 5.25V

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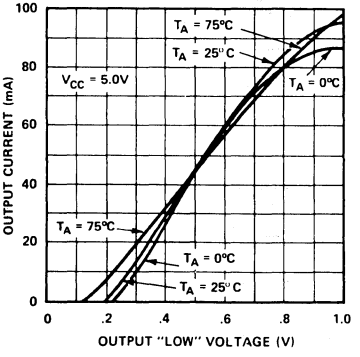
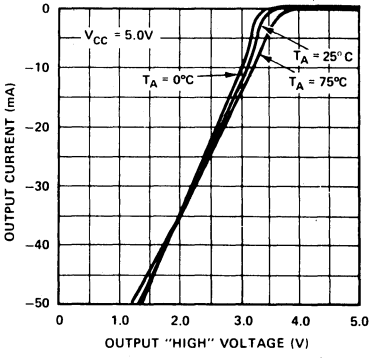
TYPICAL CHARACTERISTICS

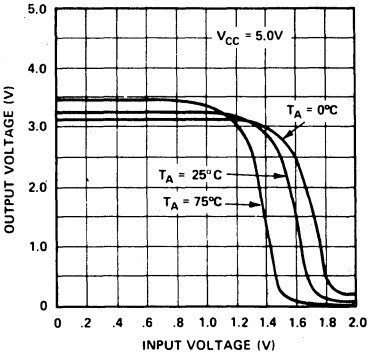
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



DATA TRANSFER FUNCTION



8205 SWITCHING CHARACTERISTICS

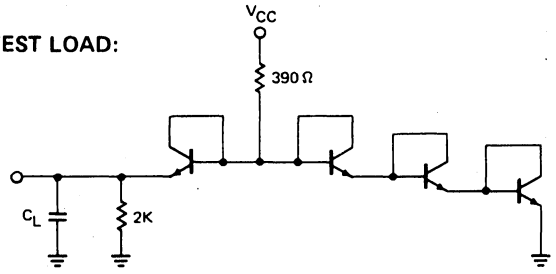
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

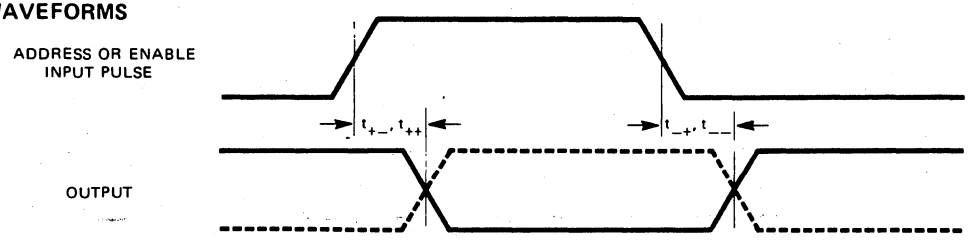
Measurements are made at 1.5V

TEST LOAD:



All Transistors 2N2369 or Equivalent. C_L = 30 pF

TEST WAVEFORMS



A.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

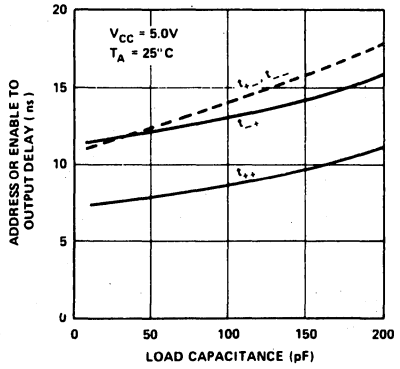
SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} (1)	INPUT CAPACITANCE	P8205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C8205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

1. This parameter is periodically sampled and is not 100% tested.

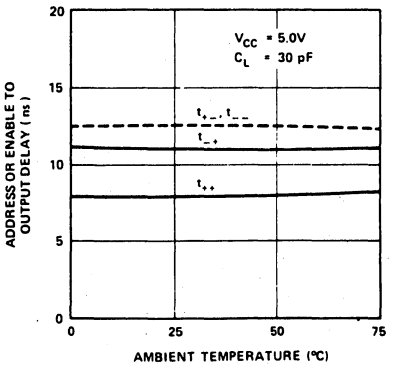
MCS-80

TYPICAL CHARACTERISTICS

ADDRESS OR ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



8214

PRIORITY INTERRUPT CONTROL UNIT

- **Eight Priority Levels**
- **Current Status Register**
- **Priority Comparator**
- **Fully Expandable**
- **High Performance (50ns)**
- **24-Pin Dual In-Line Package**

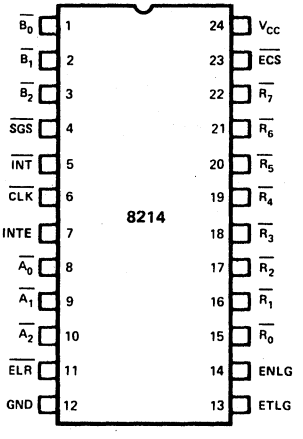
The 8214 is an eight level priority interrupt control unit designed to simplify interrupt driven microcomputer systems.

The PICU can accept eight requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

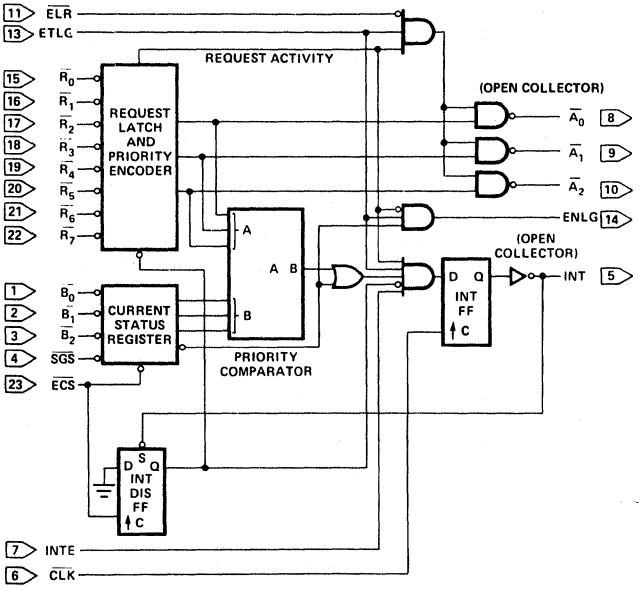
The 8214 is fully expandable by the use of open collector interrupt output and vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt driven microcomputer systems.

PIN CONFIGURATION



LOGIC DIAGRAM



PIN NAMES

INPUTS		
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)	
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS	
$\overline{SGS}$	STATUS GROUP SELECT	
$\overline{ECS}$	ENABLE CURRENT STATUS	
INTE	INTERRUPT ENABLE	
$\overline{CLK}$	CLOCK (INT F-F)	
$\overline{ELR}$	ENABLE LEVEL READ	
ETLG	ENABLE THIS LEVEL GROUP	
OUTPUTS:		
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS	OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT. LOW)	
ENLG	ENABLE NEXT LEVEL GROUP	

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D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +70°C, V_{CC} = 5V ±5%.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)			-1.0	V	I_C=-5mA
I_F	Input Forward Current: ETLG input all other inputs		-.15 -.08	-0.5 -0.25	mA mA	V_F=0.45V
I_R	Input Reverse Current: ETLG input all other inputs			80 40	μA μA	V_R=5.25V
V_{IL}	Input LOW Voltage: all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage: all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current		90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage: all outputs		.3	.45	V	I_{OL}=15mA
V_{OH}	Output HIGH Voltage: ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current: ENLG output	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$-$\overline{A_2}$			100	μA	V_{CEX}=5.25V

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
t_{CY}	$\overline{CLK}$ Cycle Time	80	50		ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	80	50		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	75	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	70	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	90	55		ns
t_{RCH}[3]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	25	ns
t_{RIS}[4]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		100	120	ns
t_{ETA}	ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	15	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	15	10		ns
t_{REN}	$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	90	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

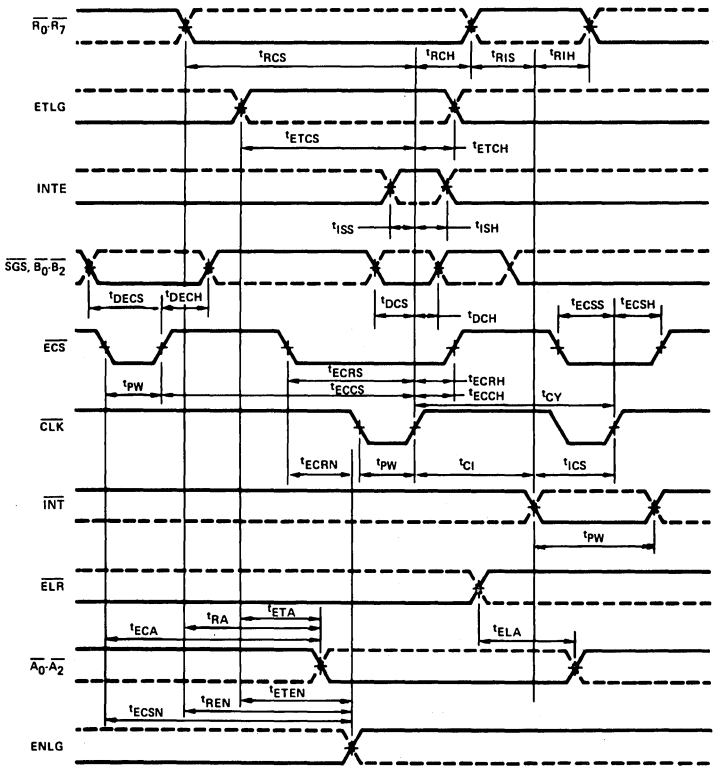
CAPACITANCE [5]

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max	
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		7	12	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5V$, $T_A = 25°C$, f = 1 MHz

NOTE 5. This parameter is periodically sampled and not 100% tested.

WAVEFORMS



NOTES:

(1) Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.

(2) Required for proper operation if ISE is enabled during next clock pulse.

(3) These times are not required for proper operation but for desired change in interrupt flip-flop.

(4) Required for new request or status to be properly loaded.

TEST CONDITIONS:

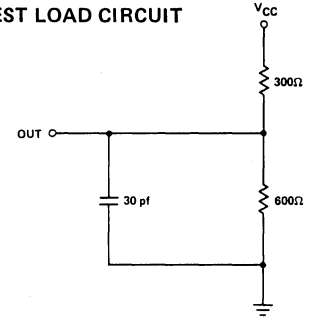
Input pulse amplitude: 2.5 volts.

Input rise and fall times: 5 ns between 1 and 2 volts.

Output loading of 15 mA and 30 pf.

Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT



8216/8226

4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER

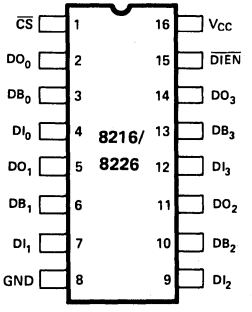
- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current — .25 mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**
- **3.65V Output High Voltage for Direct Interface to 8080 CPU**
- **Three State Outputs**
- **Reduces System Package Count**

The 8216/8226 is a 4-bit bi-directional bus driver/receiver.

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50mA I_{OL} capability.

A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

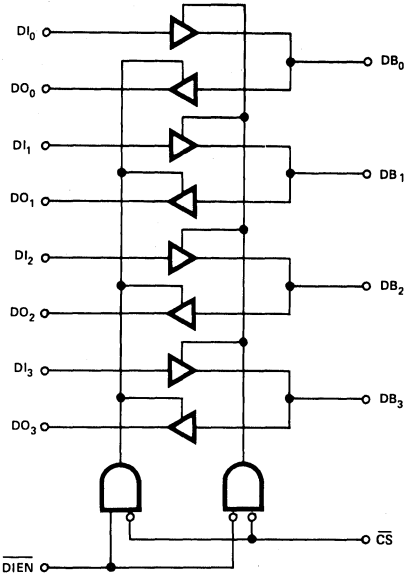
PIN CONFIGURATION



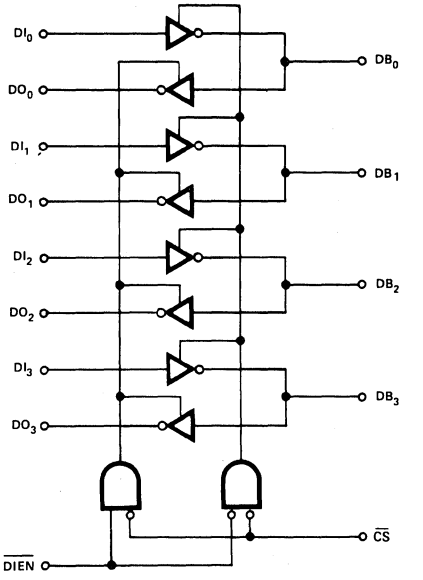
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM 8216



LOGIC DIAGRAM 8226



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D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 125 mA

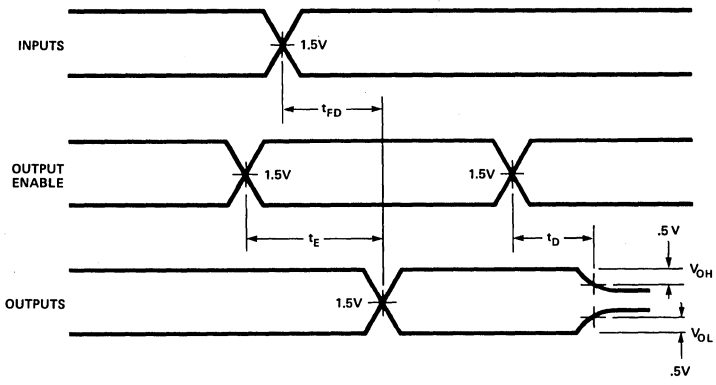
*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

T_A = 0°C to +70°C, V_{CC}=+5V ±5%

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit	Conditions
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$			-0.15	-.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs			-0.08	-.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$				20	μA	V_R = 5.25V
I_{R2}	Input Leakage Current DI Inputs				10	μA	V_R = 5.25V
V_C	Input Forward Voltage Clamp				-1	V	I_C = -5mA
V_{IL}	Input "Low" Voltage				.95	V	
V_{IH}	Input "High" Voltage		2.0			V	
$\|I_O\|$	Output Leakage Current (3-State)	DO DB			20 100	μA	V_O = 0.45V/5.25V
I_{CC}	Power Supply Current	8216		95	130	mA	
		8226		85	120	mA	
V_{OL1}	Output "Low" Voltage			0.3	.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output "Low" Voltage	8216		0.5	.6	V	DB Outputs I_{OL}=55mA
		8226		0.5	.6	V	DB Outputs I_{OL}=50mA
V_{OH1}	Output "High" Voltage		3.65	4.0		V	DO Outputs I_{OH} = -1mA
V_{OH2}	Output "High" Voltage		2.4	3.0		V	DB Outputs I_{OH} = -10mA
I_{OS}	Output Short Circuit Current		-15 -30	-35 -75	-65 -120	mA mA	DO Outputs $V_O \cong 0V$, DB Outputs V_{CC}=5.0V

NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

WAVEFORMS



A.C. CHARACTERISTICS

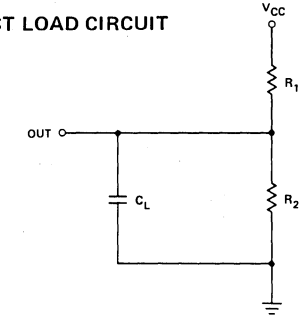
T_A = 0°C to +70°C, V_{CC} = +5V ±5%

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Conditions
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	C_L=30pF, R_1=300Ω R_2=600Ω
T_{PD2}	Input to Output Delay DB Outputs 8216		20	30	ns	C_L=300pF, R_1=90Ω
	8226		16	25	ns	R_2 = 180Ω
T_E	Output Enable Time 8216		45	65	ns	(Note 2)
	8226		35	54	ns	(Note 3)
T_D	Output Disable Time		20	35	ns	(Note 4)

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT



Capacitance[5]

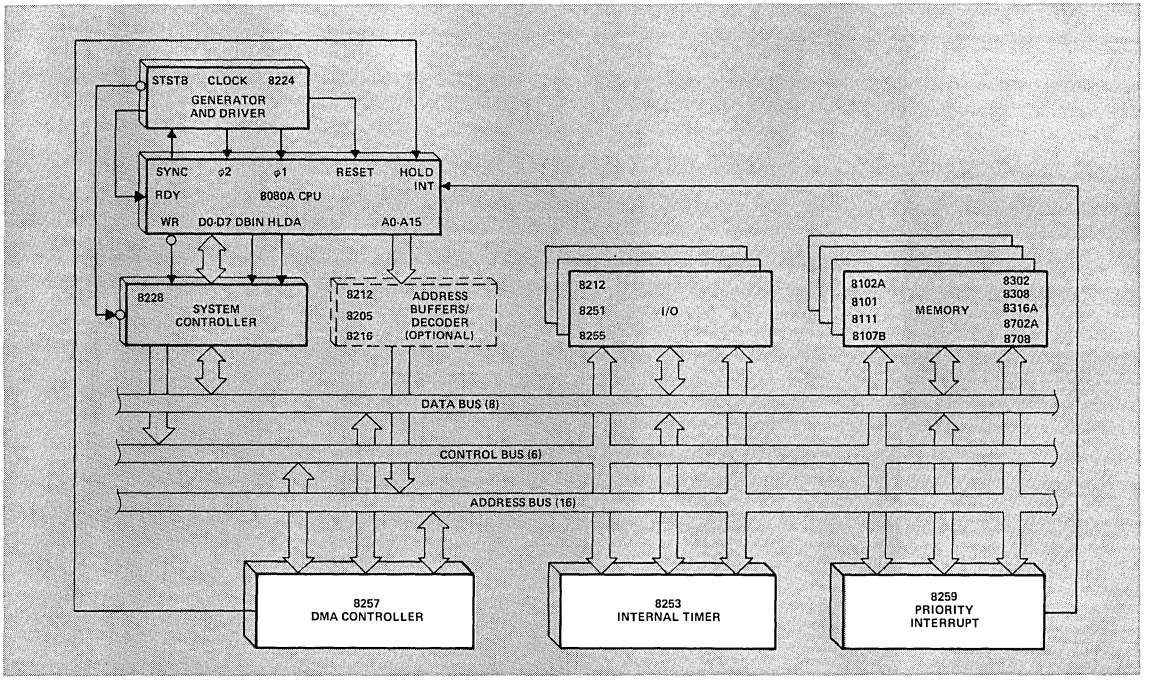
Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		4	8	pF
C_{OUT1}	Output Capacitance		6	10	pF
C_{OUT2}	Output Capacitance		13	18	pF

TEST CONDITIONS: V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 180/1KΩ; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
3. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 600/1K; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
4. DO Outputs, C_L = 5pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ; DB Outputs, C_L = 5pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
5. This parameter is periodically sampled and not 100% tested.

NEW MCS-80™ PERIPHERALS

8253
8257
8259



8253

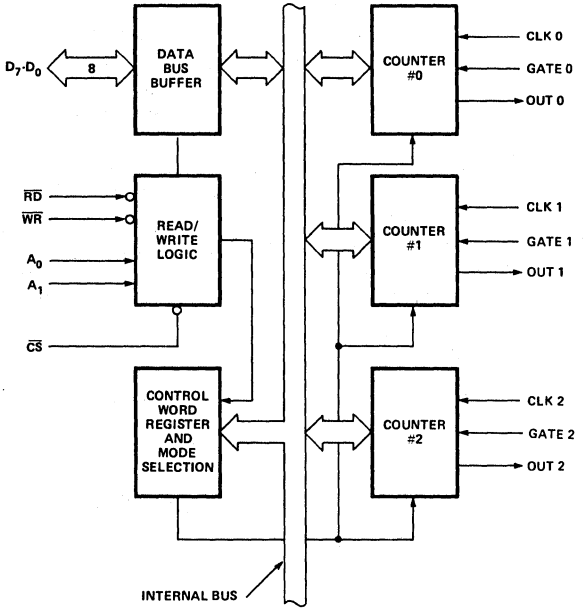
PROGRAMMABLE INTERVAL TIMER

- 3 Independent 16-Bit Counters
- DC to 3 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- 24 Pin Dual-in-line Package

The 8253 is a programmable counter/timer chip designed for use as an 8080 (or 8008) peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as three independent 16-bit counters, each with a count rate from 0Hz to 3MHz. All modes of operation are software programmable by the 8080.

BLOCK DIAGRAM



8253 PRELIMINARY FUNCTIONAL DESCRIPTION

In Microcomputer-based systems the most common interface is to a mechanical device such as a printer head or stepper motor. All such devices have inherent delays that must be accounted for if accurate and reliable performance is to be achieved. The systems software allows for such delays by programmed timing loops. This type of programming requires significant overhead and maintenance of multiple loops gets extremely complicated.

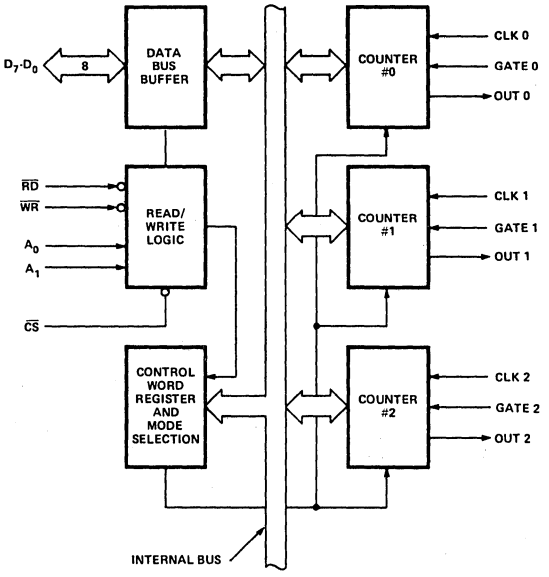
The 8253 Programmable Interval Timer is a single chip solution to system timing problems. In essence, it is a group of three 16-bit counters that are independent in nature but driven commonly as I/O peripheral ports. Instead of setting up timing loops in the system software, the programmer configures the 8253 to match his requirements. The programmer initializes one of the three counters of the 8253 with the quantity and mode desired then, upon command, the 8253 will count out the delay and interrupt the microcomputer when it has finished its task. It is easy to see that the software overhead is minimal and that multiple delays can be easily maintained by assigned interrupt levels to different counters. Other functions that are non-delay in nature and require counters can also be implemented with the 8253.

- Programmable Baud Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock

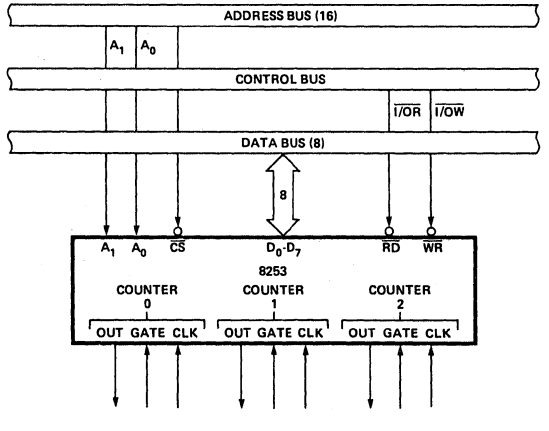
System Interface

The 8253 is a component of the MCS-80 system and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of I/O ports; three are counters and the fourth is a control register for programming. The OUT lines of each counter would normally be tied to the interrupt request inputs of the 8259.

The 8253 represents a significant improvement for solving one of the most common problems in system design and reducing software overhead.



8253 Block Diagram.



8253 System Interface.

8257

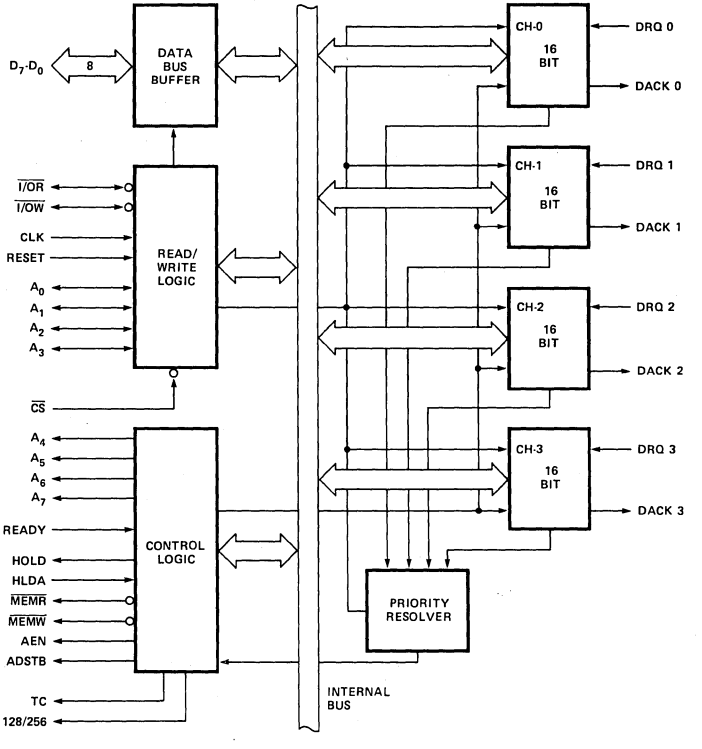
PROGRAMMABLE DMA CONTROLLER

- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal and Modulo 256/128 Outputs
- Auto Load Mode
- Single TTL Clock (ϕ2/TTL)
- Single +5V Supply
- Expandable
- 40 Pin Dual-in-Line Package

The 8257 is a Direct Memory Access (DMA) Chip which has four channels for use in 8080 microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to access or deposit data directly from or to memory. It uses the Hold feature of the 8080 to acquire the system bus. It also keeps count of the number of DMA cycles for each channel and notifies the peripheral when a programmable terminal count has been reached. Other features that it has are two mode priority logic to resolve the request among the four channels, programmable channel inhibit logic, an early write pulse option, a modulo 256/128 Mark output for sectored data transfers, an automatic load mode, a terminal count status register, and control signal timing generation during DMA cycles. There are three types of DMA cycles: Read DMA Cycle, Write DMA Cycle and Verify DMA Cycle.

The 8257 is a 40-pin, N-channel MOS chip which uses a single +5V supply and the ϕ2 (TTL) clock of the 8080 system. It is designed to work in conjunction with a single 8212 8-bit, three-state latch chip. Multiple DMA chips can be used to expand the number of channels with the aid of the 8214 Priority Interrupt Chip.

BLOCK DIAGRAM



MCS-80

8257 PRELIMINARY FUNCTIONAL DESCRIPTION

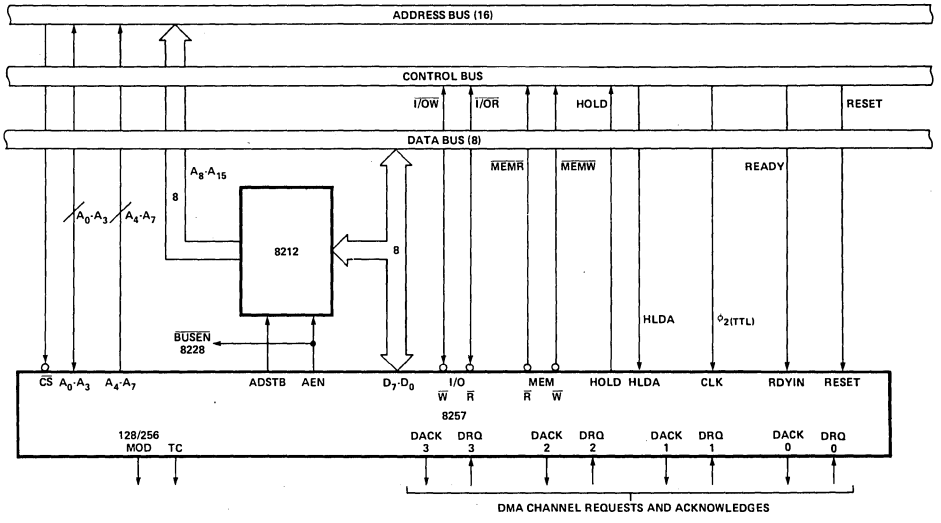
The transfer of data between a mass storage device such as a floppy disk or mag cassette and system RAM memory is often limited by the speed of the microprocessor. Removing the processor during such a transfer and letting an auxillary device manage the transfer in a more efficient manner would greatly improve the speed and make mass storage devices more attractive, even to the small system designer.

The transfer technique is called DMA (Direct Memory Access); in essence the CPU is idled so that it no longer has control of the system bus and a DMA controller takes over to manage the transfer.

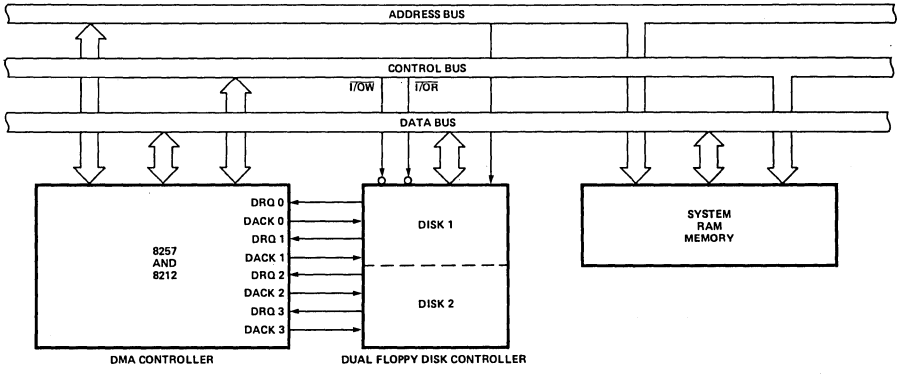
The 8257 Programmable DMA Controller is a single chip, four channel device that can efficiently manage DMA activities. Each channel is assigned a priority level so that if multi-DMA activities are required each mass storage device can be serviced, based on its importance in the system. In operation, a request is made from a peripheral device for access to the system bus. After its priority is accepted a HOLD command is ussued to the CPU, the CPU issues a HLDA and that DMA channel has complete control of the system bus. Transfers can be made in blocks, suspending the processors operation during the entire transfer or, the transfer can be made a few bytes at a time, hidden in the execution states of each instruction cycle, (cycle-stealing).

The modes and priority resolving are maintained by the system software as well as initializing each channel as to the starting address and length of transfer.

The system interface is similar to the other peripherals of the MCS-80 but an additional 8212 is necessary to control the entire address bus. A special control signal $\overline{\text{BUSEN}}$ is connected directly to the 8228 so that the data bus and control bus will be released at the proper time.



System Interface 8257.



System Application of 8257.

8259

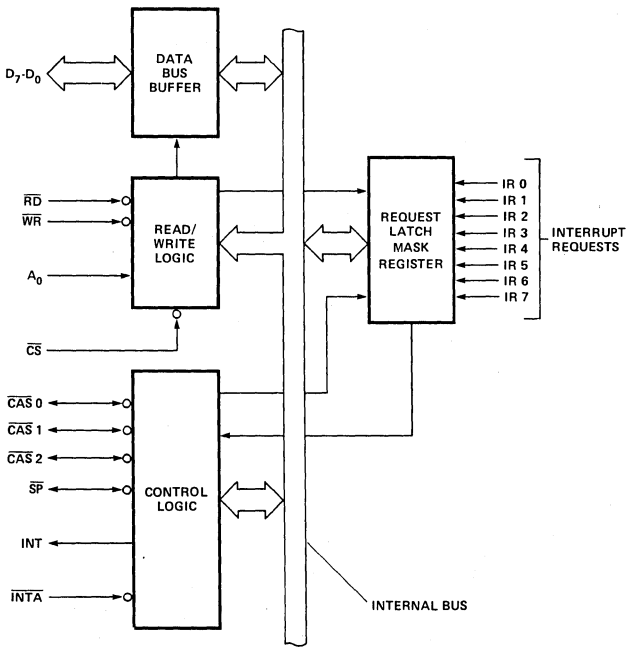
PROGRAMMABLE INTERRUPT CONTROLLER

- **Eight Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes (Algorithms)**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **28 Pin Dual-in-Line Package**

The 8259 handles up to eight vectored priority interrupts for the 8080A CPU. It is cascadable for up to 64 vectored priority interrupts, without additional circuitry. It will be packaged in a 28-pin plastic DIP, uses nMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259 is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

BLOCK DIAGRAM

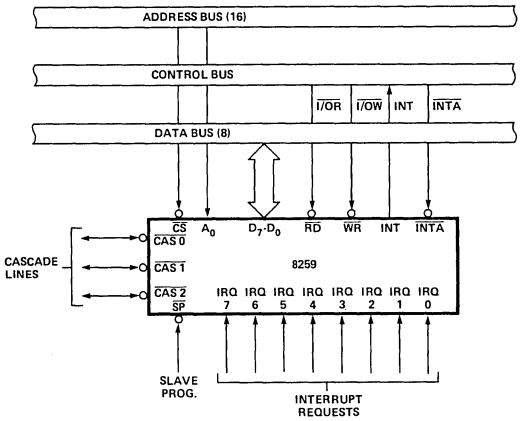


8259 PRELIMINARY FUNCTIONAL DESCRIPTION

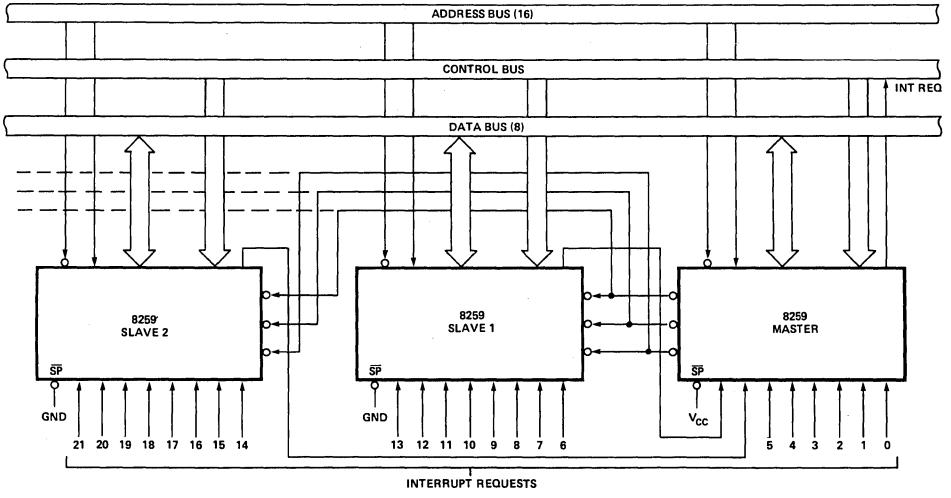
In microcomputer systems, the rate at which a peripheral device or devices can be serviced determines the total amount of system tasks that can be assigned to the control of the microprocessor. The higher the throughput the more jobs the microcomputer can do and the more cost effective it becomes. Interrupts have long been accepted as a key to improving system throughput by servicing a peripheral device only when the device has requested it to do so. Efficient managing of the interrupt requests to the CPU will have a significant effect on the overall cost effectiveness of the microcomputer system.

The 8259 Programmable Interrupt Controller is a single-chip device that can manage eight levels of requests and has built-in features for expandability to other 8259s (up to 64 levels). It is programmed by the systems software as an I/O peripheral. A selection of priority algorithms is available to the programmer so that the manner in which the requests are processed by the 8259 can be configured to match his system requirements. The priority assignments and algorithms can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

The system interface is the same as other peripheral devices in the MCS-80. A special input is provided ($\overline{SP}$) to program the 8259 as a slave or master device when expanding to more than eight levels. Basically the master accepts INT inputs from the slaves and issues a composite request to the 8080A; when it receives the $\overline{INTA}$ from the 8228 it puts the first byte on the CALL on the bus. On subsequent $\overline{INTA}$s the interrupting slave puts out the address of the vector.



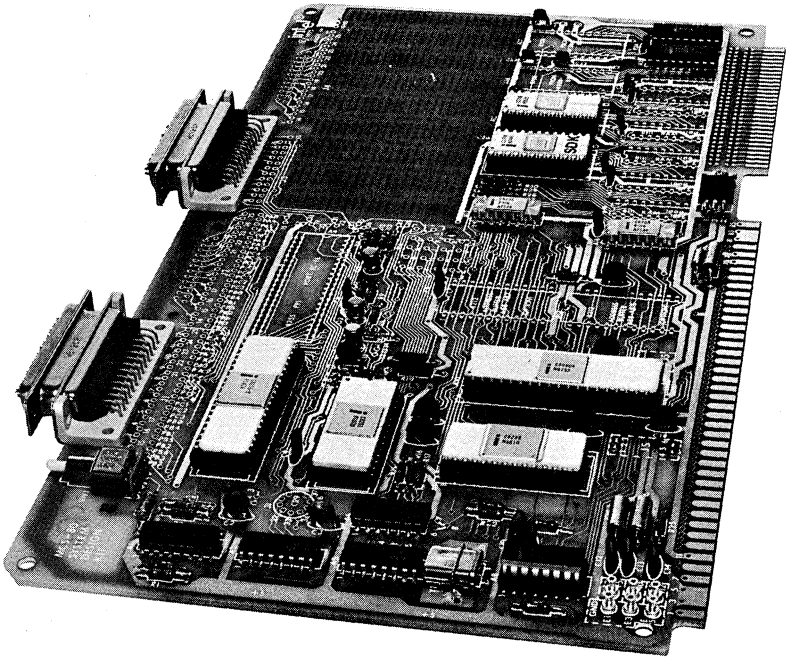
8259 System Interface.



Cascading the 8259 22 Level Controller (Expandable to 64 levels).

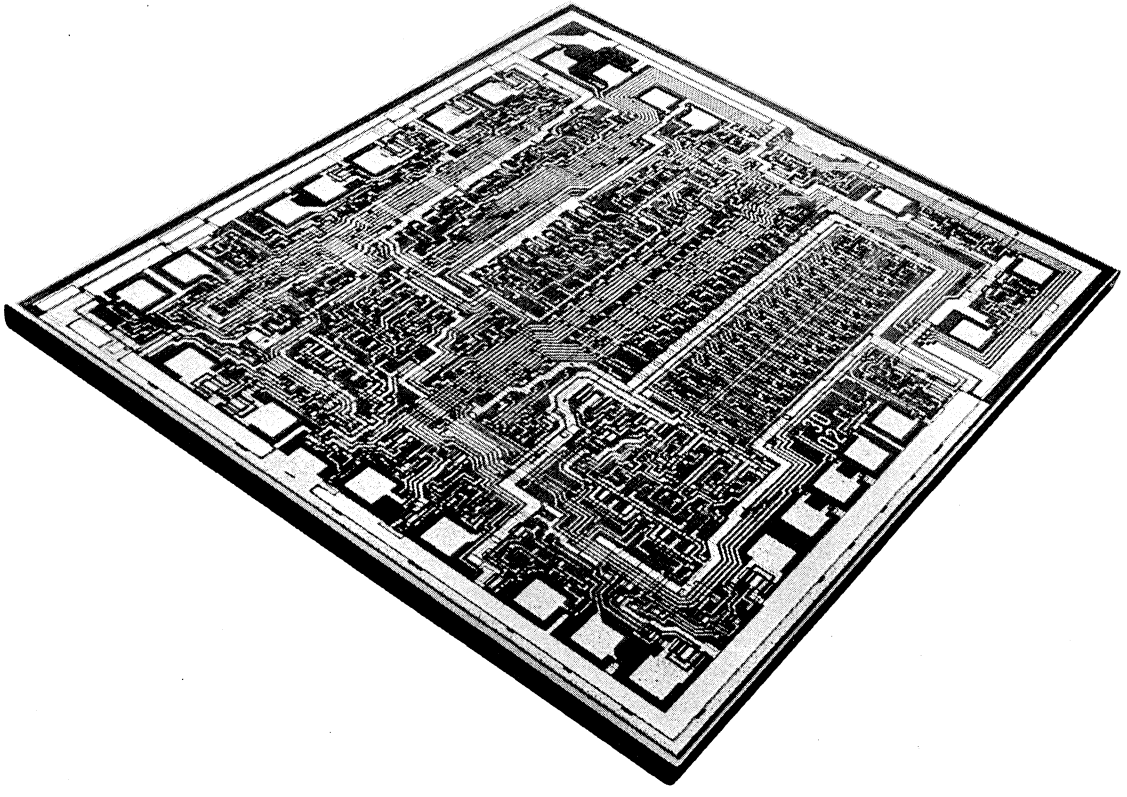
8080
SYSTEM DESIGN KIT (SDK-80)

The 8080 System Design Kit (SDK-80) is a complete, single board, microcomputer system in kit form. It contains all necessary components, including resistors, caps, crystal and miscellaneous hardware to complete construction. Included is a preprogrammed ROM that contains the system monitor for general software utilities and system diagnostics. See page 10-29 for the full details.



9

SERIES 3000 BIPOLAR MICROCOMPUTER SYSTEM



SERIES 3000
BIPOLAR MICROCOMPUTER SYSTEM

Since its introduction, the Series 3000 family of computing elements has found acceptance in a wide range of high performance applications from disk controllers to airborne central processors. The Series 3000 offers the flexibility, performance, and system integration necessary for an effective system solution for both high speed controllers and central processors.

The unique multiple bus structure of the 3002 Central Processing Element (CPE) eliminates the need for input data multiplexers or output latches. It also allows the designer to tailor the CPE's to suit his particular processing requirements. The 3001 Microprogram Control Unit (MCU) addresses up to 512 words of microprogram memory and controls both conditional and unconditional jumps within microprogram memory.

The entire component family has been designed to interconnect directly, minimizing the need for ancillary circuitry. It is available in commercial and military temperature range versions. In addition to the components, Intel has also developed a comprehensive support system to assist the user in writing microprograms, debugging hardware and microcode, and programming PROMs for both prototype and production systems.

Thus, with a complete family of components and a powerful development system, Intel provides a Total System Solution, from development to production.

3001

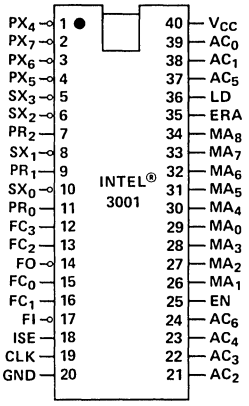
MICROPROGRAM CONTROL UNIT

The INTEL® 3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

- Maintenance of the microprogram address register.
- Selection of the next microinstruction based on the contents of the microprogram address register.
- Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence.
- Saving and testing of carry output data from the central processor (CP) array.
- Control of carry/shift input data to the CP array.
- Control of microprogram interrupts.

- **High Performance — 85 ns Cycle Time**
- **TTL and DTL Compatible**
- **Fully Buffered Three-State and Open Collector Outputs**
- **Direct Addressing of Standard Bipolar PROM or ROM**
- **512 Microinstruction Addressability**
- **Advanced Organization**
  - **9-Bit Microprogram Address Register and Bus**
  - **4-Bit Program Latch**
  - **Two Flag Registers**
- **Eleven Address Control Functions**
  - **Three Jump and Test Latch Functions**
  - **16-way Jump and Test Instruction Bus Function**
- **Eight Flag Control Functions**
  - **Four Flag Input Functions**
  - **Four Flag Output Functions**
- **40 Pin DIP**

PACKAGE CONFIGURATION



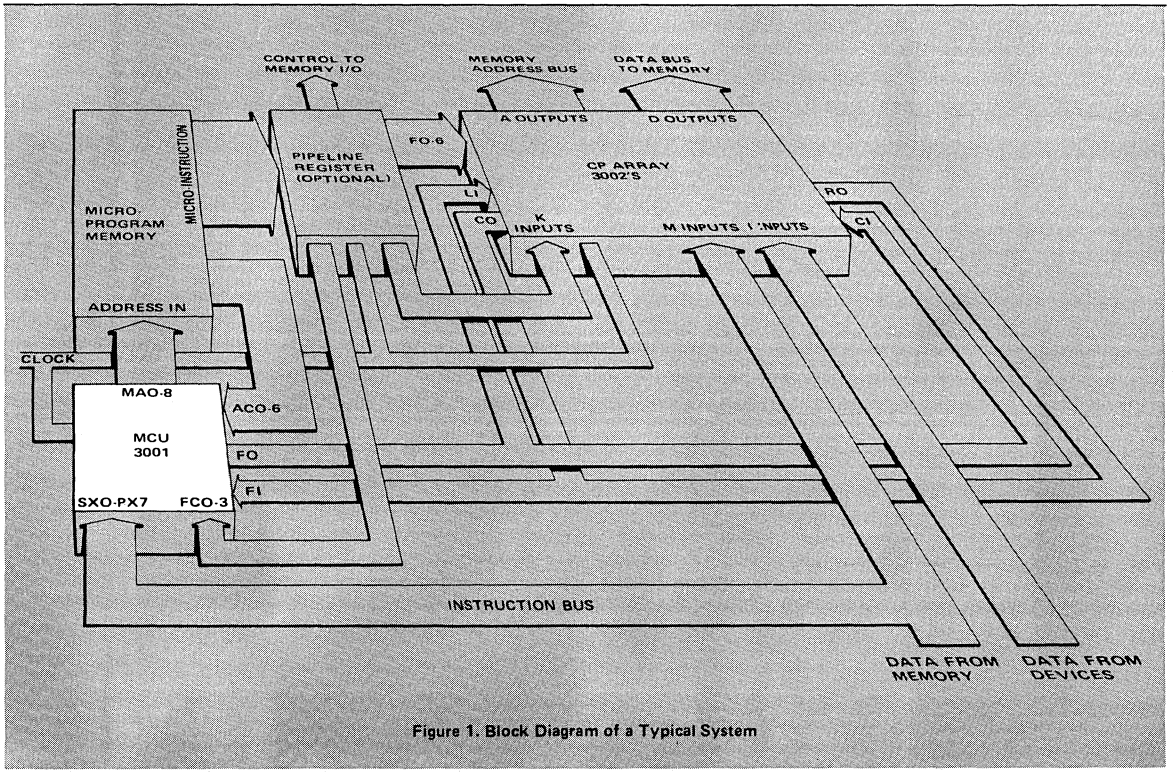


Figure 1. Block Diagram of a Typical System

SERIES 3000

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1-4	PX_4-PX_7	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	active LOW
5, 6, 8, 10	SX_0-SX_3	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	active LOW
7, 9, 11	PR_0-PR_2	PR-Latch Outputs The PR-latch outputs are asynchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	open collector
12, 13, 15, 16	FC_0-FC_3	Flag Logic Control Inputs The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	
14	FO	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	active LOW three-state
17	FI	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: the flag input data is saved in the F-latch when the clock input (CLK) is low.	active LOW
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description, page 6). It can be used to provide the strobe signal required by the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits.	
19	CLK	Clock Input	
20	GND	Ground	
21-24 37-39	AC_0-AC_6	Next Address Control Function Inputs All jump functions are selected by these control lines.	
25	EN	Enable Input When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26-29	MA_0-MA_3	Microprogram Column Address Outputs	three-state
30-34	MA_4-MA_8	Microprogram Row Address Outputs	three-state
35	ERA	Enable Row Address Input When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used with the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits to facilitate the implementation of priority interrupt systems.	
36	LD	Microprogram Address Load Input When in the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	
40	VCC	+5 Volt Supply	

NOTE:
(1) Active HIGH unless otherwise specified.

LOGICAL DESCRIPTION

The MCU performs two major control functions. First, it controls the sequence in which microinstructions are fetched from the microprogram memory. For this purpose, the MCU contains a microprogram address register and the associated logic for selecting the next microinstruction address. The second function of the MCU is the control of the two flag flip-flops that are included for interaction with the carry input and carry output logic of the CP array. The logical organization of the MCU is shown in Figure 2.

NEXT ADDRESS LOGIC

The next address logic of the MCU provides a set of conditional and unconditional address control functions. These address control functions are used to implement a jump or jump/test operation as part of every microinstruction. That is to say, each microinstruction typically contains a jump operation field that specifies the address control function, and hence, the next microprogram address.

In order to minimize the pin count of the MCU, and reduce the complexity of the next address logic, the microprogram address space is organized as a two dimensional array or matrix. Each microprogram address corresponds to a unit of the matrix at a particular row and column location. Thus, the 9-bit microprogram address is treated as specifying not one, but two addresses — the row address in the upper five bits and the column address in the lower four bits. The address matrix can therefore contain, at most, 32 row addresses and 16 column addresses for a total of 512 microinstructions.

The next address logic of the MCU makes extensive use of this two component addressing scheme. For example, from a particular row or column address, it is possible to jump unconditionally in one operation anywhere in that row or column. It is not possible, however, to jump anywhere in the address matrix. In fact, for a given location in the matrix, there is a fixed subset of microprogram addresses that may be selected as the next address. These possible jump target addresses are referred to as a jump set. Each type of MCU address control (jump) function has a jump set associated with it. Appendix C illustrates the jump set for each function.

FLAG LOGIC

The flag logic of the MCU provides a set of functions for saving the current value of the carry output of the CP array and for controlling the value of the carry input to the CP array. These two distinct flag control functions are called flag input functions and flag output functions.

The flag logic is comprised of two flip-flops, designated the C-flag and the Z-flag, along with a simple latch, called the F-latch, that indicates the current state of the carry output line of the CP array. The flag logic is used in conjunction with the carry and shift logic of the CP array to implement a variety of shift/rotate and arithmetic functions.

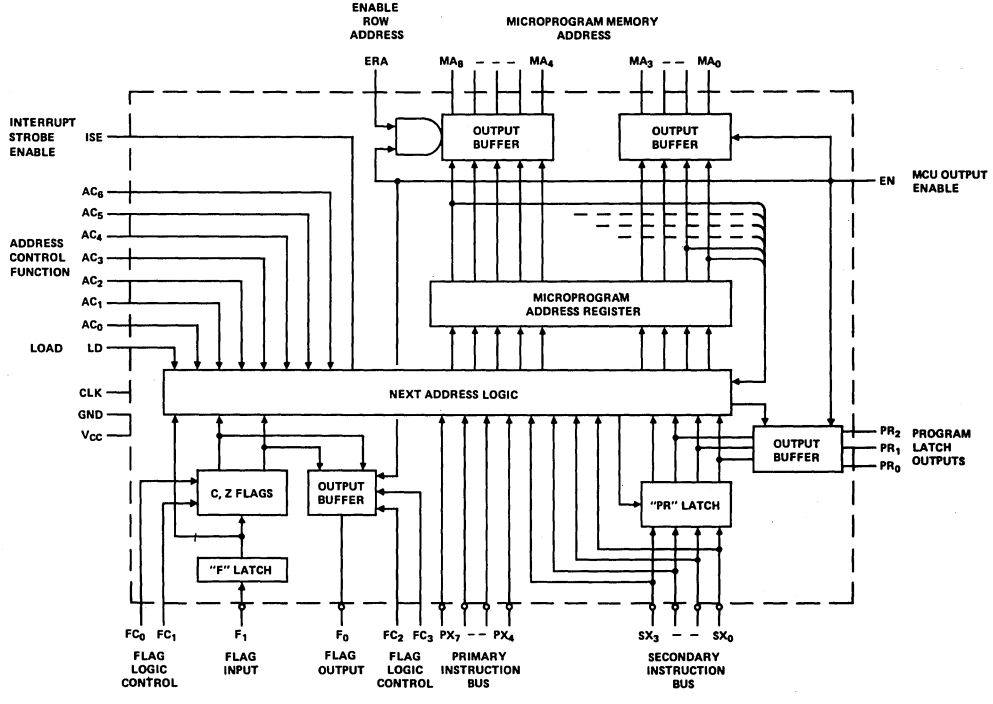


Figure 2. 3001 Block Diagram

FUNCTIONAL DESCRIPTION

ADDRESS CONTROL FUNCTIONS

The address control functions of the MCU are selected by the seven input lines designated AC_0-AC_6. On the rising edge of the clock, the 9-bit microprogram address generated by the next address logic is loaded into the microprogram address register. The next microprogram address is delivered to the microprogram memory via the nine output lines designated MA_0-MA_8. The microprogram address outputs are organized into row and column addresses as:

$$\underbrace{MA_8\ MA_7\ MA_6\ MA_5\ MA_4}_{\text{row address}}$$

$$\underbrace{MA_3\ MA_2\ MA_1\ MA_0}_{\text{column address}}$$

Each address control function is specified by a unique encoding of the data on the function input lines. From three to five bits of the data specify the particular function while the remaining bits are used to select part of either the row or column address desired. Function code formats are given in Appendix A, "Address Control Function Summary."

The following is a detailed description of each of the eleven address control functions. The symbols shown below are used throughout the description to specify row and column addresses.

Symbol	Meaning
row_n	5-bit next row address where n is the decimal row address.
col_n	4-bit next column address where n is the decimal column address.

UNCONDITIONAL ADDRESS CONTROL (JUMP) FUNCTIONS

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs to generate the next microprogram address.

Mnemonic	Function Description
JCC	Jump in current column. AC_0-AC_4 are used to select 1 of 32 row addresses in the current column, specified by MA_0-MA_3, as the next address
JZR	Jump to zero row. AC_0-AC_3 are used to select 1 of 16 column addresses in row_0, as the next address.
JCR	Jump in current row. AC_0-AC_3 are used to select 1 of 16 addresses in the current row, specified by MA_4-MA_8, as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7-MA_8, as the next row address. The current column is specified by MA_0-MA_3. The PR-latch outputs are asynchronously enabled.

FLAG CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

Mnemonic	Function Description
JFL	Jump/test F-Latch. AC_0-AC_3 are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is col_0-col_7, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the F-latch is used to select col_{10} or col_{11} as the next column address.
JCF	Jump/test C-flag. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_3 is col_0-col_7, the C-flag is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the C-flag is used to select col_{10} or col_{11} as the next column address.
JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.

PX-BUS AND PR-LATCH CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The PX-bus jump/test function uses the data on the primary instruction bus (PX_4-PX_7), the current mircoprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Mnemonic	Function Description
JPR	Jump/test PR-latch. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.

Mnemonic	Function Description
JLL	Jump/test leftmost PR-latch bits. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to

FUNCTIONAL DESCRIPTION (con't)

	select 1 of 4 possible column addresses in col_4 through col_7 as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC_0 and AC_1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} through col_{15} as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by MA_6-MA_8, as the next row address. PX_4-PX_7 are used to select 1 of 16 possible column addresses as the next column address. SX_0-SX_3 data is locked in the PR-latch at the rising edge of the clock.

FLAG CONTROL FUNCTIONS

The flag control functions of the MCU are selected by the four input lines designated FC_0-FC_3. Function code formats are given in Appendix B, "Flag Control Function Summary."

The following is a detailed description of each of the eight flag control functions.

FLAG INPUT CONTROL FUNCTIONS

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line. Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Mnemonic	Function Description
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTIONS

The flag output control functions select the value to which the flag output (FO) line will be forced.

Mnemonic	Function Description
FF0	Force FO to 0. FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

LOAD AND INTERRUPT STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active HIGH at the rising edge of the clock, the data on the primary and secondary instruction busses, PX_4-PX_7 and SX_0-SX_3, is loaded into the microprogram address register. PX_4-PX_7 are loaded into MA_0-MA_3 and SX_0-SX_3 are loaded into MA_4-MA_7. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

The interrupt strobe enable of the MCU is available on the output line designated ISE. The line is placed in the active high state whenever a JZR to col_{15} is selected as the address control function. Customarily, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so that the INTEL 3214 Priority Interrupt Control Unit may be enabled at the beginning of the fetch/execute cycle. The priority interrupt control unit may respond to the interrupt by pulling the enable row address (ERA) input line down to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC_0-AC_6. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +160°C

All Output and Supply Voltages . . . . . −0.5V to +7V

All Input Voltages . . . . . −1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to 70°C V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		−0.8	−1.0	V	I_C = −5 mA
I_F	Input Load Current:					
	CLK Input		−0.075	−0.75	mA	V_F = 0.45V
	EN Input		−0.05	−0.50	mA	
	All Other Inputs		−0.025	−0.25	mA	
I_R	Input Leakage Current:					
	CLK			120	μA	V_R = 5.25V
	EN Input			80	μA	
	All Other Inputs			40	μA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current (2)		170	240	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (MA_0-MA_8, ISE, FO)	2.4	3.0		V	I_{OH} = −1 mA
I_{OS}	Output Short Circuit Current (MA_0-MA_8, ISE, FO)	−15	−28	−60	mA	V_{CC} = 5.0V
$I_{O(off)}$	Off-State Output Current:					
	MA_0–MA_8, FO			−100	μA	V_O = 0.45V
	MA_0–MA_8, FO, PR_0–PR_2			100	μA	V_O = 5.25V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) EN input grounded, all other inputs and outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%

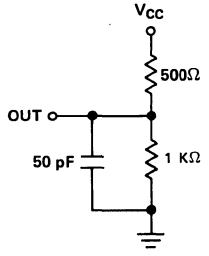
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY}	Cycle Time (2)	85	60		ns
t_{WP}	Clock Pulse Width	30	20		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC_0-AC_6	10	0		ns
t_{SK}	FC_0, FC_1	0			ns
t_{SX}	SX_0-SX_3, PX_4-PX_7	35	25		ns
t_{SI}	FI	15	5		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC_0-AC_6	5	0		ns
t_{HK}	FC_0, FC_1	0			ns
t_{HX}	SX_0-SX_3, PX_4-PX_7	20	5		ns
t_{HI}	FI	20	8		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA_0-MA_8, FO)	10	30	45	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		16	30	ns
t_{FO}	Propagation Delay from Control Inputs AC_0-AC_6 to Latch Outputs (PR_0-PR_2)		26	40	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA_0-MA_8, FO, PR_0-PR_2)		21	32	ns
t_{FI}	Propagation Delay from Control Inputs AC_0-AC_6 to Interrupt Strobe Enable Output (ISE)		24	40	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) $t_{CY} = t_{WP} + t_{SF} + t_{CO}$

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 10 mA and 50 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:



CAPACITANCE(2) T_A = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:				
	CLK, EN		11	16	pF
	All Other Inputs		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and T_A = 25°C.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C

Storage Temperature . . . . . −65°C to +160°C

All Output and Supply Voltages . . . . . −0.5V to +7V

All Input Voltages . . . . . −1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		−0.8	-1.2	V	I_C = −5 mA
I_F	Input Load Current:					
	CLK Input		-75	-750	μA	V_F = 0.45V
	EN Input		-50	-500	μA	
	All Other Inputs		-25	-250	μA	
I_R	Input Leakage Current:					
	CLK			120	μA	V_R = 5.5V
	EN Input			80	μA	
	All Other Inputs			40	μA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current (2)		170	250	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (MA_0-MA_8, ISE, FO)	2.4	3.0		V	I_{OH} = −1 mA
I_{OS}	Output Short Circuit Current (MA_0-MA_8, ISE, FO)	−15	−28	−60	mA	V_{CC} = 5.0V
$I_{O(off)}$	Off-State Output Current:					
	MA_0–MA_8, FO			−100	μA	V_O = 0.45V
	MA_0–MA_8, FO, PR_0–PR_2			100	μA	V_O = 5.5V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) EN input grounded, all other inputs and outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

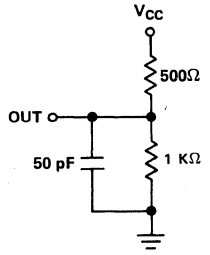
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY}	Cycle Time (2)	95	60		ns
t_{WP}	Clock Pulse Width	40	20		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC_0-AC_6	10	0		ns
t_{SK}	FC_0, FC_1	0			ns
t_{SX}	SX_0-SX_3, PX_4-PX_7	35	25		ns
t_{SI}	FI	15	5		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC_0-AC_6	5	0		ns
t_{HK}	FC_0, FC_1	0			ns
t_{HX}	SX_0-SX_3, PX_4-PX_7	25	5		ns
t_{HI}	FI	22	8		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA_0-MA_8, FO)	10	30	45	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		16	50	ns
t_{FO}	Propagation Delay from Control Inputs AC_0-AC_6 to Latch Outputs (PR_0-PR_2)		26	50	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA_0-MA_8, FO, PR_0-PR_2)		21	35	ns
t_{FI}	Propagation Delay from Control Inputs AC_0-AC_6 to Interrupt Strobe Enable Output (ISE)		24	40	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) $t_{CY} = t_{WP} + t_{SF} + t_{CO}$

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 10 mA and 50 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:

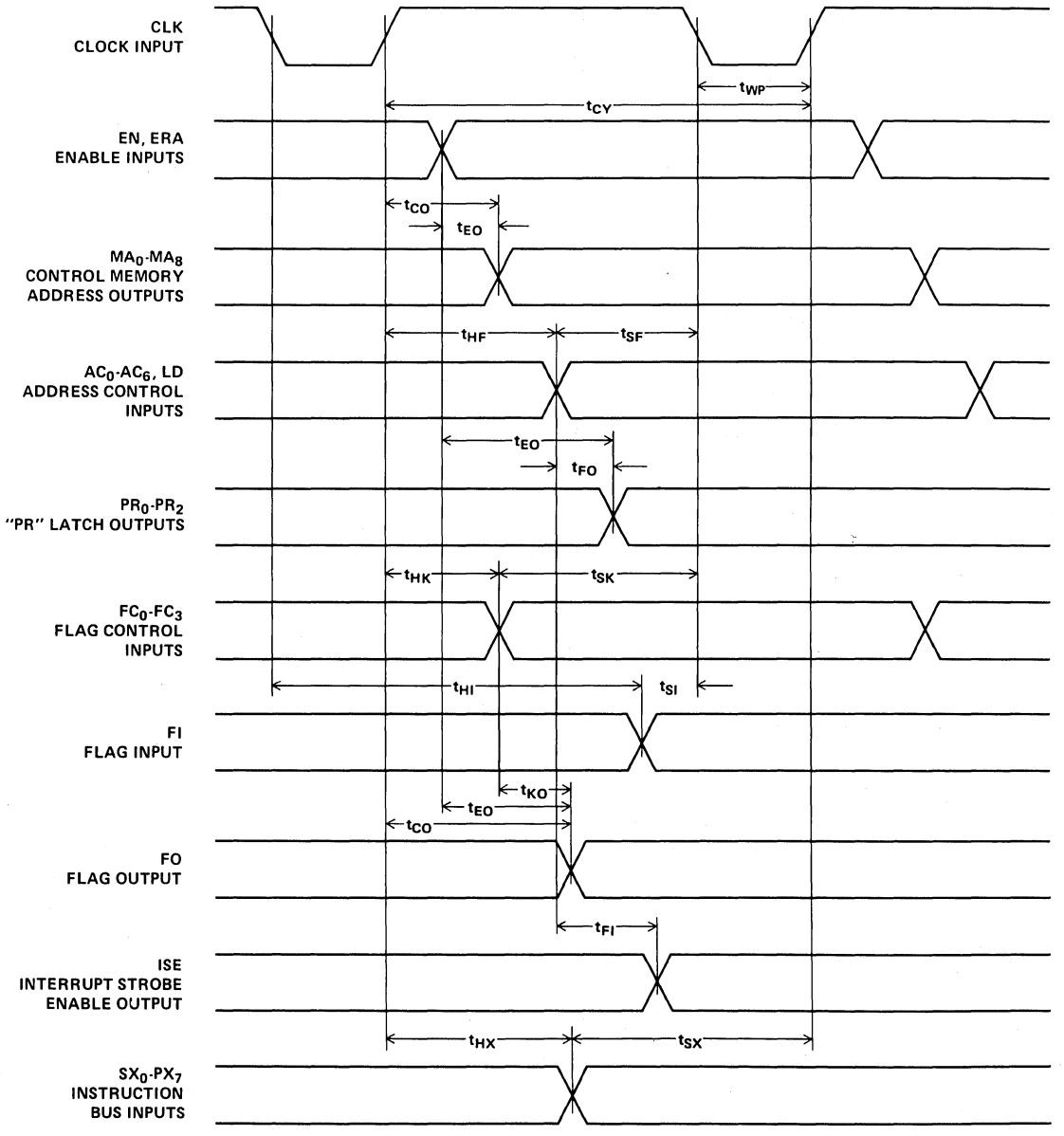


CAPACITANCE(2) T_A = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:				
	CLK, EN		11	16	pF
	All Other Inputs		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and T_A = 25°C.

3001 WAVEFORMS



3002

CENTRAL PROCESSING ELEMENT

The INTEL® 3002 Central Processing Element contains all of the circuits that represent a 2-bit wide slice through the data processing section of a digital computer. To construct a complete central processor for a given word width N, it is simply necessary to connect an array of N/2 CPE's together. When wired together in such an array, a set of CPE's provide the following capabilities:

- 2's complement arithmetic
- Logical AND, OR, NOT and exclusive-OR
- Incrementing and decrementing
- Shifting left or right
- Bit testing and zero detection
- Carry look-ahead generation
- Multiple data and address busses

High Performance – 100 ns Cycle Time

TTL and DTL Compatible

N-Bit Word Expandable Multi-Bus Organization
- 3 Input Data Busses
- 2 Three-State Fully Buffered Output Data Busses

11 General Purpose Registers

Full Function Accumulator

Independent Memory Address Register

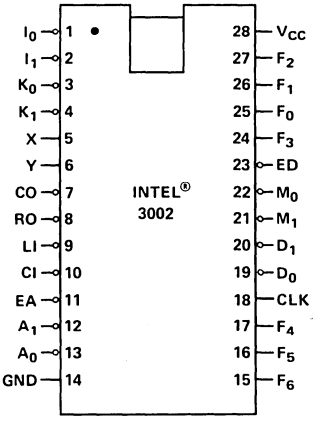
Cascade Outputs for Full Carry Look-Ahead

Versatile Functional Capability
- 8 Function Groups
- Over 40 Useful Functions
- Zero Detect and Bit Test

Single Clock

28 Pin DIP

PACKAGE CONFIGURATION



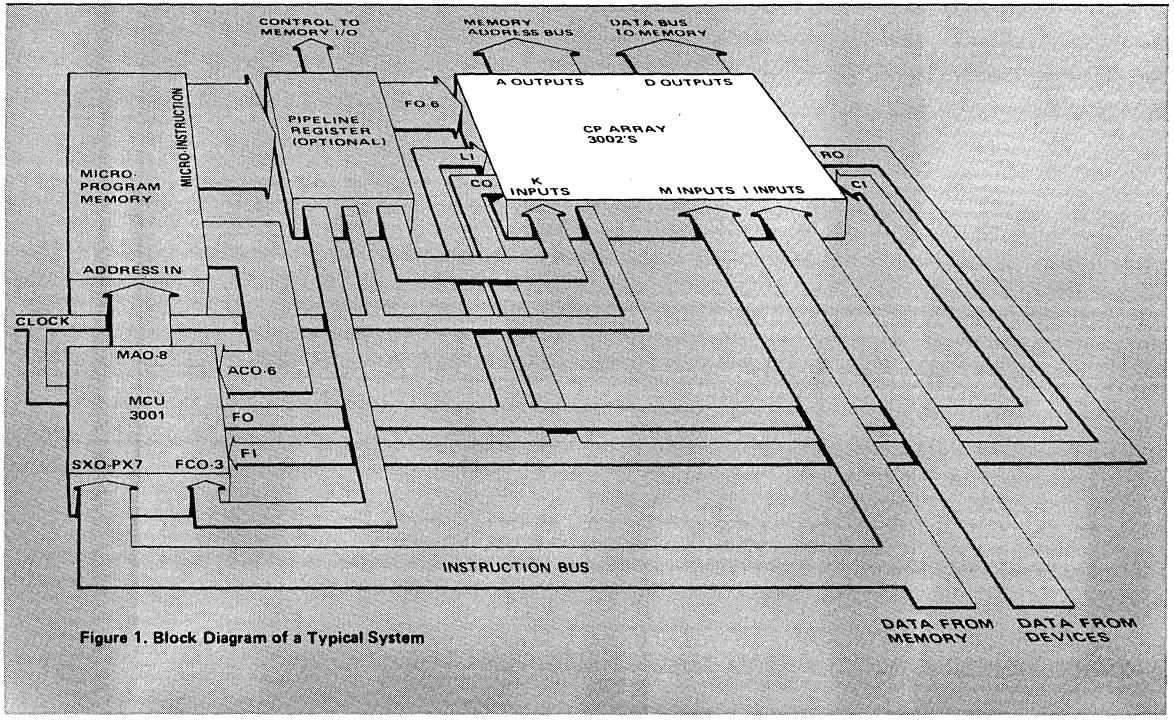


Figure 1. Block Diagram of a Typical System

SERIES 3000

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1, 2	I_0-I_1	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active LOW
3, 4	K_0-K_1	Mask Bus Inputs The mask bus inputs provide a separate input port for the microprogram memory, to allow mask or constant entry.	Active LOW
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the INTEL 3003 Look-Ahead Carry Generator.	
7	CO	Ripple Carry Output The ripple carry output is only disabled during shift right operations.	Active LOW Three-state
8	RO	Shift Right Output The shift right output is only enabled during shift right operations.	Active LOW Three-state
9	LI	Shift Right Input	Active LOW
10	CI	Carry Input	Active LOW
11	EA	Memory Address Enable Input When in the LOW state, the memory address enable input enables the memory address outputs (A_0-A_1).	Active LOW
12-13	A_0-A_1	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active LOW Three-state
14	GND	Ground	
15-17, 24-27,	F_0-F_6	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	
18	CLK	Clock Input	
19-20	D_0-D_1	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active LOW Three-state
21-22	M_0-M_1	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active LOW
23	ED	Memory Data Enable Input When in the LOW state, the memory data enable input enables the memory data outputs (D_0-D_1)	Active LOW
28	V_{CC}	+5 Volt Supply	

NOTE:
1. Active HIGH, unless otherwise specified.

LOGICAL DESCRIPTION

The CPE provides the arithmetic, logic and register functions of a 2-bit wide slice through a microprogrammed central processor. Data from external sources such as main memory, is brought into the CPE on one of the three separate input busses. Data being sent out of the CPE to external devices is carried on either of the two output busses. Within the CPE, data is stored in one of eleven scratchpad registers or in the accumulator. Data from the input busses, the registers, or the accumulator is available to the arithmetic/logic section (ALS) under the control of two internal multiplexers. Additional inputs and outputs are included for carry propagation, shifting, and micro-function selection. The complete logical organization of the CPE is shown below.

MICRO-FUNCTION BUS AND DECODER

The seven micro-function bus input lines of the CPE, designated F_0-F_6, are decoded internally to select the ALS function, generate the scratchpad address, and control the A and B multiplexers.

M-BUS AND I-BUS INPUTS

The M-bus inputs are arranged to bring data from an external main memory into the CPE. Data on the M-bus is multiplexed internally for input to the ALS.

The I-bus inputs are arranged to bring data from an external I/O system into the CPE. Data on the I-bus is also multiplexed internally, although independently of the M-bus, for input to the ALS Separation of the two busses permits a relatively lightly loaded memory bus even though a large number of I/O devices are connected to the I-bus. Alternatively, the I-bus may be wired to perform a multiple bit shift (e.g., a byte exchange) by connecting it to one of the output busses. In this case, I/O device data is gated externally onto the M-bus.

SCRATCHPAD

The scratchpad contains eleven registers designated R_0 through R_9 and T. The output of the scratchpad is multiplexed internally for input to ALS. The ALS output is returned for input into the scratchpad.

ACCUMULATOR AND D-BUS

An independent register called the accumulator (AC) is available for storing the result of an ALS operation. The output of the accumulator is multiplexed internally for input back to the ALS and is also available via a three-state output buffer on the D-bus outputs. Conventional usage of the D-bus is for data being sent to the external main memory or to external I/O devices.

A AND B MULTIPLEXERS

The A and B multiplexers select the two inputs to the ALS specified on the micro-function bus. Inputs to the A-multiplexer include the M-bus, the scratchpad, and the accumulator. The B-multiplexer selects either the I-bus, the accumulator, or the K-bus. The selected B-multiplexer input is always logically ANDed with the data on the K-bus (see below) to provide a flexible masking and bit testing capability.

ALS AND K-BUS

The ALS is capable of a variety of arithmetic and logic operations, including 2's complement addition, incrementing, and decrementing, plus logical AND, inclusive-OR, exclusive-NOR, and logical complement. The result of an ALS operation may be stored in the accumulator or one of the scratchpad registers. Separate left input and right output lines, designated LI and RO, are available for use in right shift operations. Carry input and carry output lines, designated CI and CO are provided for normal ripple carry propagation. CO and RO data are brought out via two alternately enabled tri-state buffers. In addition, standard look ahead carry outputs, designated X and Y, are available for full carry look ahead across any word length.

The ability of the K-bus to mask inputs to the ALS greatly increases the versatility of the CPE. During non-arithmetic operations in which carry propagation has no meaning, the carry circuits are used to perform a word-wise inclusive-OR of the bits, masked by the K-bus, from the register or bus selected by the function decoder. Thus, the CPE provides a flexible bit testing capability. The K-bus is also used during arithmetic operations to mask portions of the field being operated upon. An additional function of the K-bus is that of supplying constants to the CPE from the microprogram.

MEMORY ADDRESS REGISTER AND A-BUS

A separate ALS output is also available to the memory address register (MAR) and to the A-bus via a three-state output buffer. Conventional usage of the MAR and A-bus is for sending addresses to an external main memory. The MAR and A-bus may also be used to select an external device when executing I/O operations.

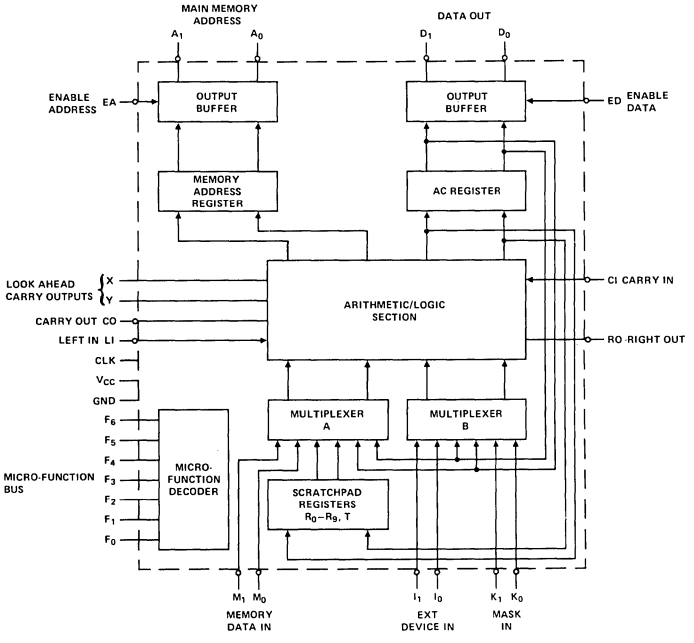


Figure 2. 3002 Block Diagram

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +160°C

All Output and Supply Voltages . . . . . −0.5V to +7V

All Input Voltages . . . . . −1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

		LIMITS				
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		−0.8	−1.0	V	I_C = −5 mA
I_F	Input Load Current:					
	F_0–F_6, CLK, K_0, K_1, EA, ED		−0.05	−0.25	mA	V_F = 0.45V
	I_0, I_1, M_0, M_1, LI		−0.85	−1.5	mA	
	CI		−2.3	−4.0	mA	
I_R	Input Leakage Current:					
	F_0–F_6, CLK, K_0, K_1, EA, ED			40	μA	V_R = 5.25V
	I_0, I_1, M_0, M_1, LI			60	μA	
	CI			180	μA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current(2)		145	190	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.3	0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (All Output Pins)	2.4	3.0		V	I_{OH} = −1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	−15	−25	−60	mA	V_{CC} = 5.0V
$I_{O(off)}$	Off State Output Current			−100	μA	V_O = 0.45V
	A_0, A_1, D_0, D_1, CO and RO			100	μA	V_O = 5.25V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage
(2) CLK input grounded, other inputs open.

A.C. CHARACTERISTICS AND WAVEFORMS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%

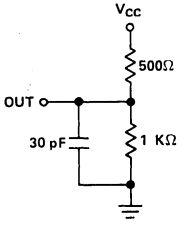
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY}	Clock Cycle Time (2)	100	70		ns
t_{WP}	Clock Pulse Width	33	20		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	60	40		ns
	Data Set-Up Time:				
t_{DS}	I_0, I_1, M_0, M_1, K_0, K_1	50	30		ns
t_{SS}	LI, CI	27	13		ns
	Data and Function Hold Time:				
t_{FH}	F_0 through F_6	5	-2		ns
t_{DH}	I_0, I_1, M_0, M_1, K_0, K_1	5	-4		ns
t_{SH}	LI, CI	15	2		ns
	Propagation Delay to X, Y, RO from:				
t_{XF}	Any Function Input		37	52	ns
t_{XD}	Any Data Input		29	42	ns
t_{XT}	Trailing Edge of CLK		40	60	ns
t_{XL}	Leading Edge of CLK	20			ns
	Propagation Delay to CO from:				
t_{CL}	Leading Edge of CLK	20			ns
t_{CT}	Trailing Edge of CLK		48	70	ns
t_{CF}	Any Function Input		43	65	ns
t_{CD}	Any Data Input		30	55	ns
t_{CC}	CI (Ripple Carry)		14	25	ns
	Propagation Delay to A_0, A_1, D_0, D_1 from:				
t_{DL}	Leading Edge of CLK	5	32	50	ns
t_{DE}	Enable Input ED, EA		12	25	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) $t_{CY} = t_{DS} + t_{DL}$.

TEST CONDITIONS:

Input pulse amplitude: 2.5 V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 10 mA and 30 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



CAPACITANCE(2) T_A = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V and T_A = 25°C.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to +125°C

Storage Temperature . . . . . −65°C to +160°C

All Output and Supply Voltages . . . . . −0.5V to +7V

All Input Voltages . . . . . −1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%.

		LIMITS				
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		−0.8	−1.2	V	I_C = −5 mA
I_F	Input Load Current:					
	F_0–F_6, CLK, K_0, K_1, EA, ED		−0.05	−0.25	mA	V_F = 0.45V
	I_0, I_1, M_0, M_1, LI		−0.85	−1.5	mA	
	CI		−2.3	−4.0	mA	
I_R	Input Leakage Current:					
	F_0-F_6, CLK, K_0, K_1, EA, ED			40	μA	V_R = 5.5V
	I_0, I_1, M_0, M_1, LI			100	μA	
	CI			250	μA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current		145	210	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.3	0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (All Output Pins)	2.4	3.0		V	I_{OH} = −1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	−15	−25	−60	mA	V_{CC} = 5.0V
$I_{O(off)}$	Off State Output Current			−100	μA	V_O = 0.45V
	A_0, A_1, D_0, D_1, CO and RO			100	μA	V_O = 5.5V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage
(2) CLK input grounded, other inputs open.

A.C. CHARACTERISTICS AND WAVEFORMS

T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%.

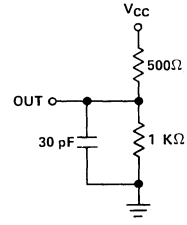
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY}	Clock Cycle Time [2]	120	70		ns
t_{WP}	Clock Pulse Width	42	20		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	70	40		ns
	Data Set-Up Time:				
t_{DS}	I_0, I_1, M_0, M_1, K_0, K_1	60	30		ns
t_{SS}	LI, CI	30	13		ns
	Data and Function Hold Time:				
t_{FH}	F_0 through F_6	5	-2		ns
t_{DH}	I_0, I_1, M_0, M_1, K_0, K_1	5	-4		ns
t_{SH}	LI, CI	15	2		ns
	Propagation Delay to X, Y, RO from:				
t_{XF}	Any Function Input		37	65	ns
t_{XD}	Any Data Input		29	55	ns
t_{XT}	Trailing Edge of CLK		40	75	ns
t_{XL}	Leading Edge of CLK	22			ns
	Propagation Delay to CO from:				
t_{CL}	Leading Edge of CLK	22			ns
t_{CT}	Trailing Edge of CLK		48	85	ns
t_{CF}	Any Function Input		43	75	ns
t_{CD}	Any Data Input		30	65	ns
t_{CC}	CI (Ripple Carry)		14	30	ns
	Propagation Delay to A_0, A_1, D_0, D_1 from:				
t_{DL}	Leading Edge of CLK	5	32	60	ns
t_{DE}	Enable Input ED, EA		12	35	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) $t_{CY} = t_{DS} + t_{DL}$

TEST CONDITIONS:

Input pulse amplitude: 2.5 V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 10 mA and 30 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:

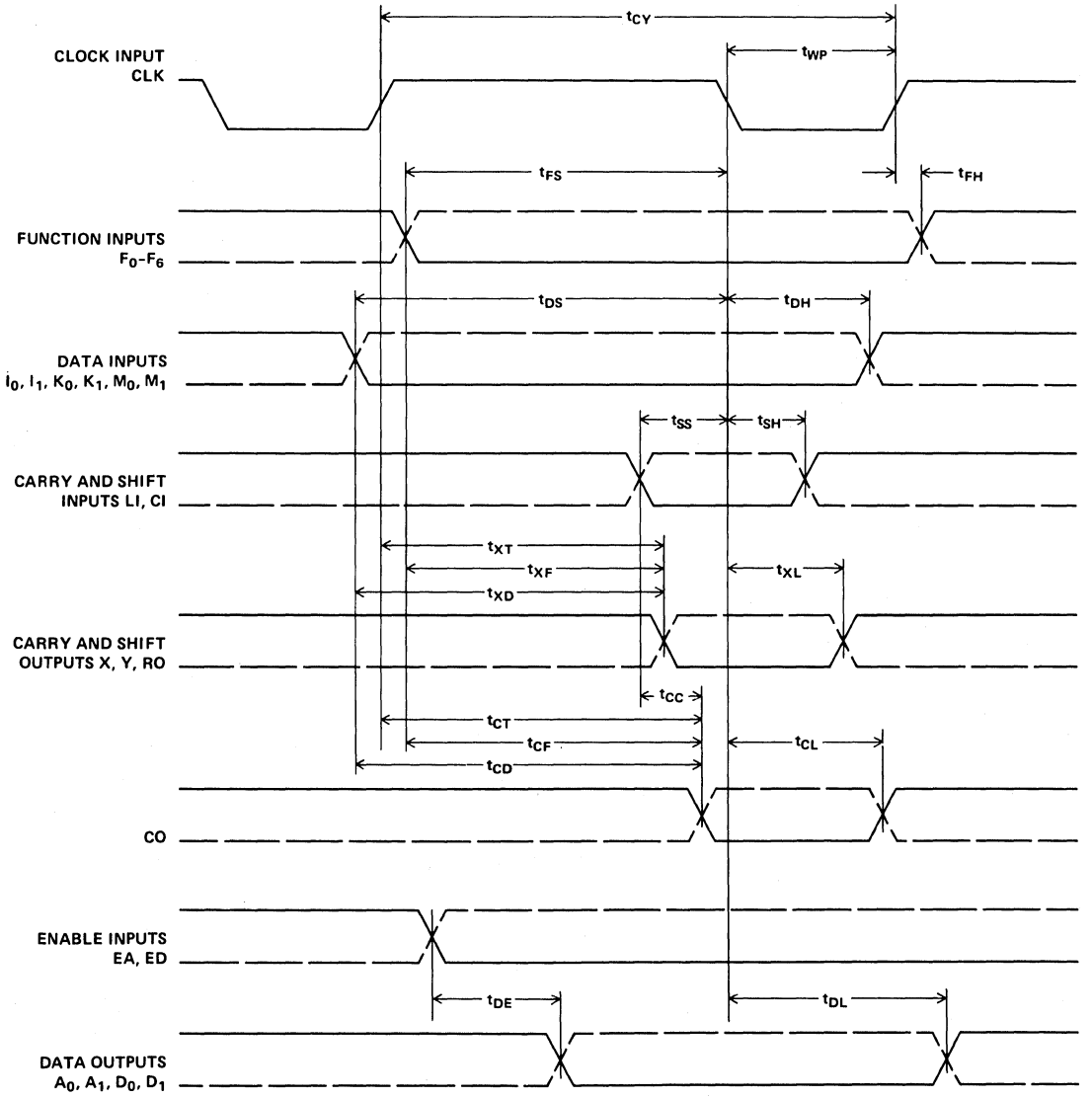


CAPACITANCE(2) T_A = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V and T_A = 25°C.

3002 WAVEFORMS



3003

LOOK-AHEAD CARRY GENERATOR

The INTEL® 3003 Look-Ahead Carry Generator (LCG) is a high speed circuit capable of anticipating a carry across a full 16-bit 3002 Central Processing Array. When used with a larger 3002 CP Array multiple 3003 carry generators provide high speed carry look-ahead capability for any word length.

The LCG accepts eight pairs of active high cascade inputs (X,Y) and an active low carry input and generates active low carries for up to eight groups of binary adders.

High Performance – 10 ns typical propagation delay

Compatible with INTEL 3001 MCU and 3002 CPE

DTL and TTL compatible

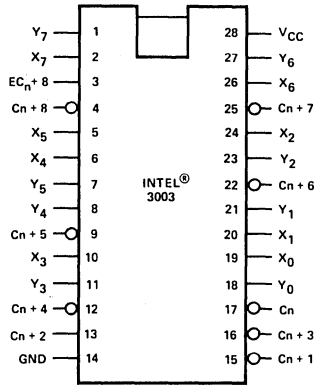
Full look-ahead across 8 adders

Low voltage diode input clamp

Expandable

28-pin DIP

PACKAGE CONFIGURATION



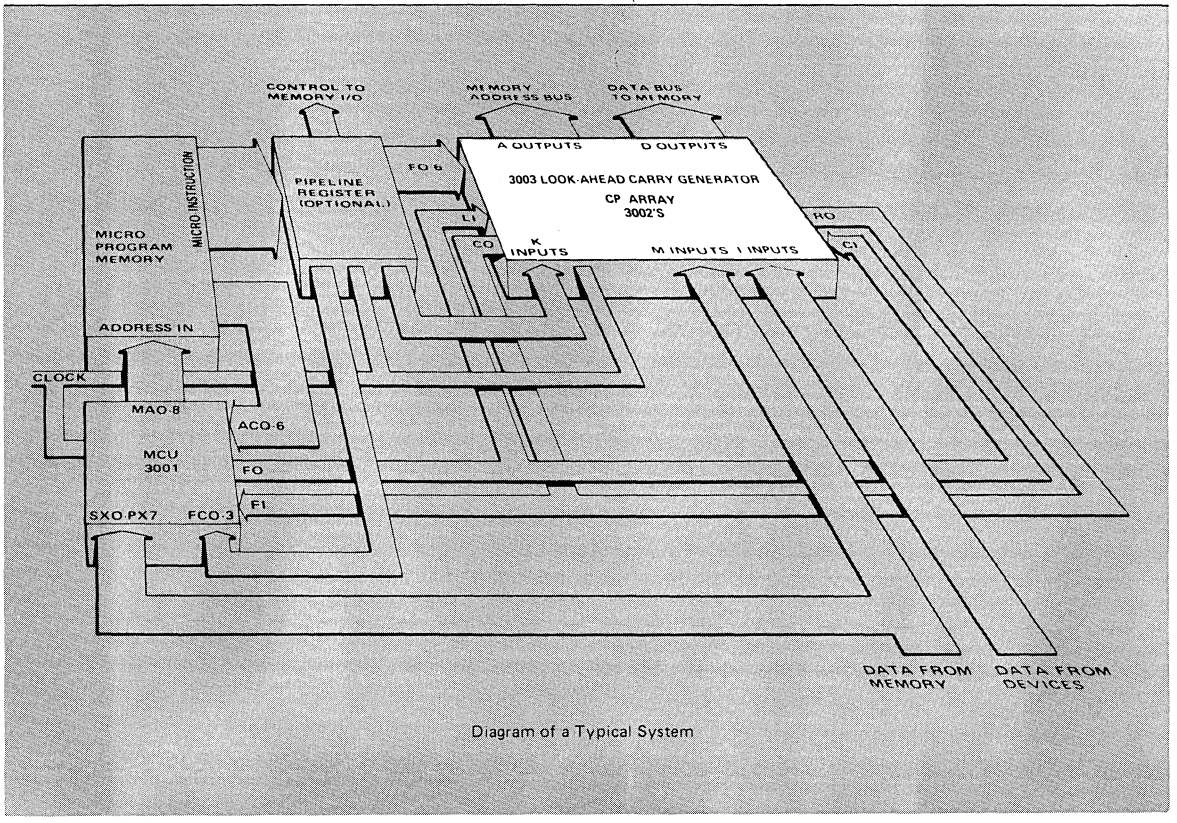


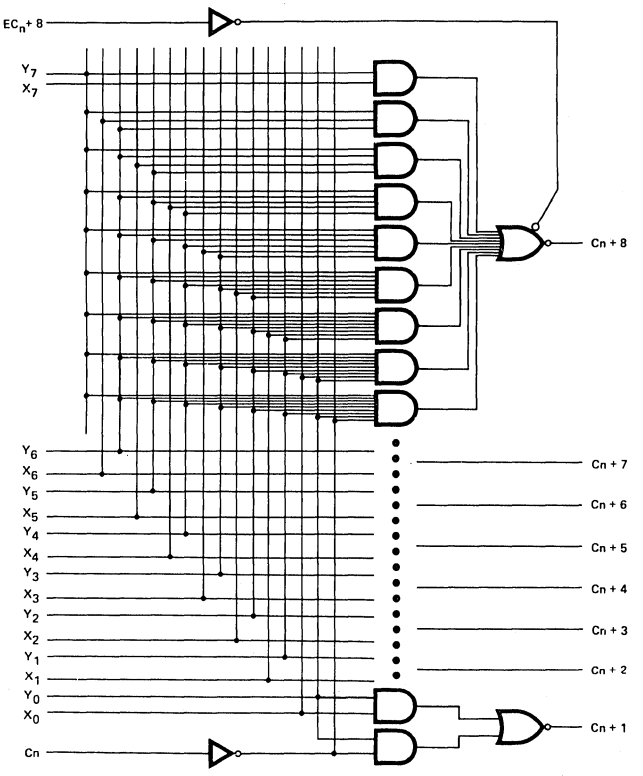
Diagram of a Typical System

SERIES 3000

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1,7,8,11 18,21,23 27	Y_0-Y_7	Standard carry look-ahead inputs	Active HIGH
2,5,6,10 19,20,24 26	X_0-X_7	Standard carry look-ahead inputs	Active HIGH
17	C_n	Carry input	Active LOW
4,9,12 13,15,16	C_{n+1}- C_{n+8}	Carry outputs	Active LOW
3	EC_{n+8}	C_{n+8} carry output enable	Active HIGH
28	V_{CC}	+5 volt supply	
14	GND	Ground	

LOGIC DIAGRAM



3003 LOGIC EQUATIONS

The 3003 Look-Ahead Generator is implemented in a compatible form for direct connection to the 3001 MCU and 3002 CPE. Logic equations for the 3003 are:

$$\overline{C_{n+1}} = Y_0X_0 + Y_0\overline{C}_n$$

$$\overline{C_{n+2}} = Y_1X_1 + Y_1Y_0X_0 + Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+3}} = Y_2X_2 + Y_2Y_1X_1 + Y_2Y_1Y_0X_0 + Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+4}} = Y_3X_3 + Y_3Y_2X_2 + Y_3Y_2Y_1X_1 + Y_3Y_2Y_1Y_0X_0 + Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+5}} = Y_4X_4 + Y_4Y_3X_3 + Y_4Y_3Y_2X_2 + Y_4Y_3Y_2Y_1X_1 + Y_4Y_3Y_2Y_1Y_0X_0 + Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+6}} = Y_5X_5 + Y_5Y_4X_4 + Y_5Y_4Y_3X_3 + Y_5Y_4Y_3Y_2X_2 + Y_5Y_4Y_3Y_2Y_1X_1 + Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+7}} = Y_6X_6 + Y_6Y_5X_5 + Y_6Y_5Y_4X_4 + Y_6Y_5Y_4Y_3X_3 + Y_6Y_5Y_4Y_3Y_2X_2 + Y_6Y_5Y_4Y_3Y_2Y_1X_1 + Y_6Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_6Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$\overline{C_{n+8}}$ = High Impedance State when $EC_n + 8$ Low

$$\overline{C_{n+8}} = Y_7X_7 + Y_7Y_6X_6 + Y_7Y_6Y_5X_5 + Y_7Y_6Y_5Y_4X_4 + Y_7Y_6Y_5Y_4Y_3X_3 + Y_7Y_6Y_5Y_4Y_3Y_2X_2 + Y_7Y_6Y_5Y_4Y_3Y_2Y_1X_1 + Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n \text{ when } EC_n + 8 \text{ high}$$

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to +125°C

Storage Temperature . . . . . -65°C to +160°C

All Output and Supply Voltages . . . . . -0.5V to +7V

All Input Voltages . . . . . -1.0V to +5.5V

Output Current . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%.

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.2	V	I_C = -5 mA
I_F	Input Load Current:					
	X_6, X_7, Cn, EC_{n+8}		-0.07	-0.25	mA	V_F = 0.45V
	Y_7, X_0-X_5,		-0.200	-0.500	mA	
	Y_o-Y_6		-0.6	-1.5	mA	
I_R	Input Leakage Current:					
	C_n and EC_n + 8			40	µA	V_{CC} = 5.25V, V_R = 5.5V
	All Other Inputs			100	µA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.1			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current		80	130	mA	All Y and EC_n + 8 high, All X and C_n low
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage (All Output Pins)	2.4	3		V	I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	-15	-40	-65	mA	V_{CC} = 5V
$I_{O(off)}$	Off-State Output Current (C_n + 8)			-100	µA	V_O = 0.45V
				+100	µA	V_O = 5.5V

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{CC} = +5.0V ±10%

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT
t_{XC}	X, Y to Outputs	3	10	25	ns
t_{CC}	Carry In to Outputs		13	40	ns
t_{EN}	Enable Time, C_n + 8		20	50	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.

MILITARY TEMP.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . -65°C to +160°C

All Output and Supply Voltages . . . . . -0.5V to +7V

All Input Voltages . . . . . -1.0V to +5.5V

Output Current . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

T_A = 0°C to +70°C V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.0	V	I_C = -5 mA
I_F	Input Load Current:					
	X_8,X_7Cn,EC_n + 8		-0.07	-0.25	mA	V_F = 0.45V
	Y_7,X_0-X_5,		-0.200	-0.500	mA	
	Y_0-Y_6		-0.6	-1.5	mA	
I_R	Input Leakage Current:					
	C_n and EC_n + 8			40	µA	V_R = 5.25V
	All Other Inputs			100	µA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current		80	130	mA	All Y and EC_n + 8 high, All X and C_n low
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage (All Output Pins)	2.4	3		V	I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	-15	-40	-65	mA	V_{CC} = 5V
$I_{O(off)}$	Off-State Output Current (C_n + 8)			-100	µA	V_O = 0.45V
				+100	µA	V_O = 5.25V

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS

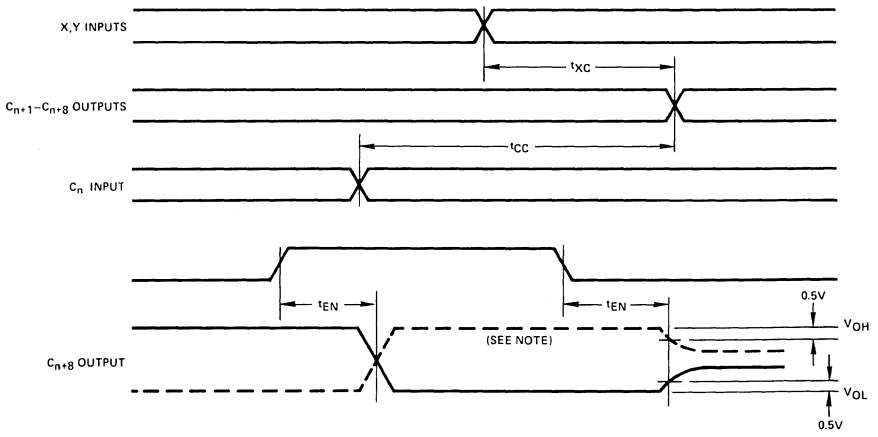
T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT
t_{XC}	X, Y to Outputs	3	10	20	ns
t_{CC}	Carry In to Outputs		13	30	ns
t_{EN}	Enable Time, C_n + 8		20	40	ns

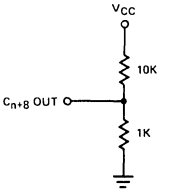
NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.

SERIES 3000

WAVEFORMS



NOTE: ALTERNATE TEST LOAD:



CAPACITANCE[2] T_A = 25°C

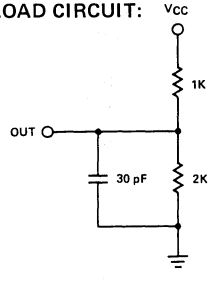
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance	All inputs		12	20	pF
C_{OUT}	Output Capacitance	C_n + 8		7	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 5.0V, V_{CC} = 5.0V and T_A = 25°C.

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 30 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



3212

MULTI-MODE LATCH BUFFER

The INTEL® 3212 Multi-Mode Latch Buffer is a versatile 8-bit latch with three-state output buffers and built-in device select logic. It also contains an independent service request flip-flop for the generation of central processor interrupts. Because of its multi-mode capabilities, one or more 3212's can be used to implement many types of interface and support systems for Series 3000 computing elements including:

- Simple data latches
- Gated data buffers
- Multiplexers
- Bi-directional bus drivers
- Interrupting input/output ports

High Performance – 50 ns Write Cycle Time

Low Input Load Current – 250 μA Maximum

Three-State Fully Buffered Outputs

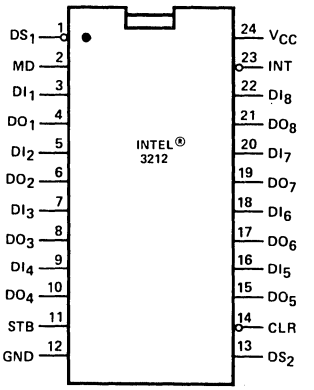
High Output Drive Capability

Independent Service Request Flip-Flop

Asynchronous Data Latch Clear

24 Pin DIP

PACKAGE CONFIGURATION



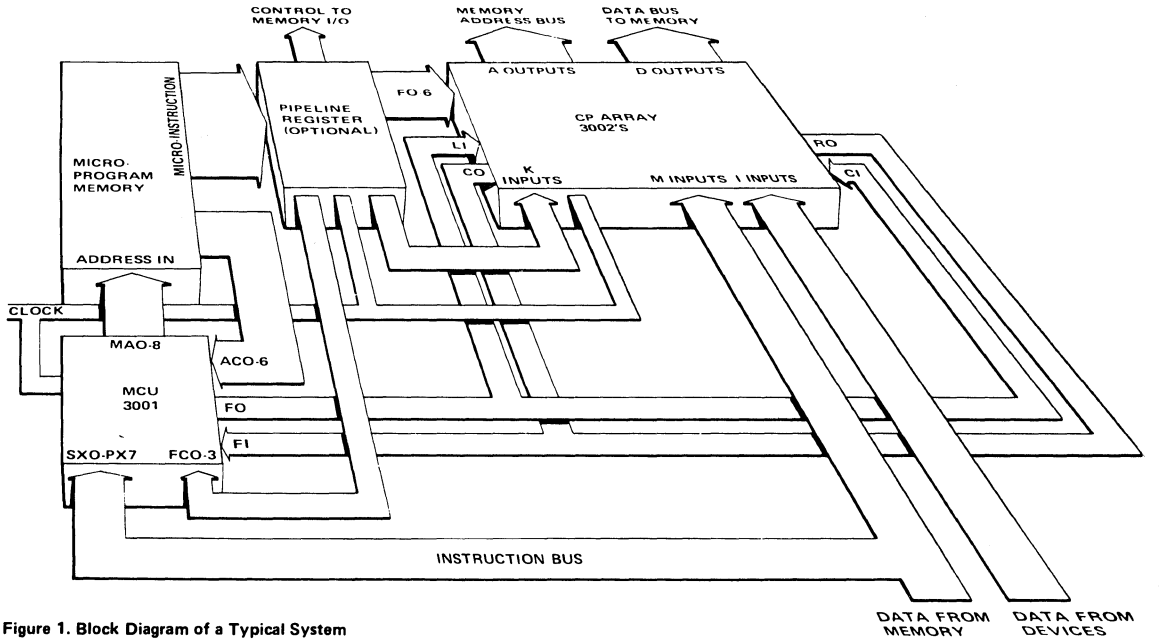


Figure 1. Block Diagram of a Typical System

SERIES 3000

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1	DS_1	Device Select Input 1	active LOW
2	MD	Mode Input When MD is high (output mode) the output buffers are enabled and the write signal to the data latches is obtained from the device select logic. When MD is low (input mode) the output buffer state is determined by the device select logic and the write signal is obtained from the strobe (STB) input.	
3, 5, 7, 9, 16, 18, 20, 22	DI_1–DI_8	Data Inputs The data inputs are connected to the D-inputs of the data latches.	
4, 6, 8, 10, 15, 17, 19, 21	DO_1–DO_8	Data Outputs The data outputs are the buffered outputs of the eight data latches.	three-state
11	STB	Strobe Input When MD is in the LOW state, the STB input provides the clock input to the data latch.	
12	GND	Ground	
13	DS_2	Device Select Input 2 When DS_1 is low and DS_2 is high, the device is selected.	
14	CLR	Clear	active LOW
23	INT	Interrupt Output The interrupt output will be active LOW (interrupting state) when either the service request flip-flop is low or the device is selected.	active LOW

NOTE:
(1) Active HIGH, unless otherwise specified.

FUNCTIONAL DESCRIPTION

The 3212 contains eight D-type data latches, eight three-state output buffers, a separate D-type service request flip-flop, and a flexible device select/mode control section.

DATA LATCHES

The Q-output of each data latch will follow the data on its corresponding date input line (DI_1–DI_8) while its clock input is high. Data will be latched when the internal write line WR is brought low. The output of each data latch is connected to a three-state, non-inverting output buffer. The internal enable line EN is bussed to each buffer. When the EN is high, the buffers are enabled and the data in each latch is available on its corresponding data output line (DO_0–DO_8).

DEVICE SELECT LOGIC

Two input lines DS_1 and $\overline{DS}_2$ are provided for device selection. When DS_1 is low and DS_2 is high, the 3212 is selected.

MODE CONTROL SECTION

The 3212 may be operated in two modes. When the mode input line MD is low, the device is in the input mode. In this mode, the output buffers are enabled whenever the 3212 is selected; the internal WR line follows the STB input line.

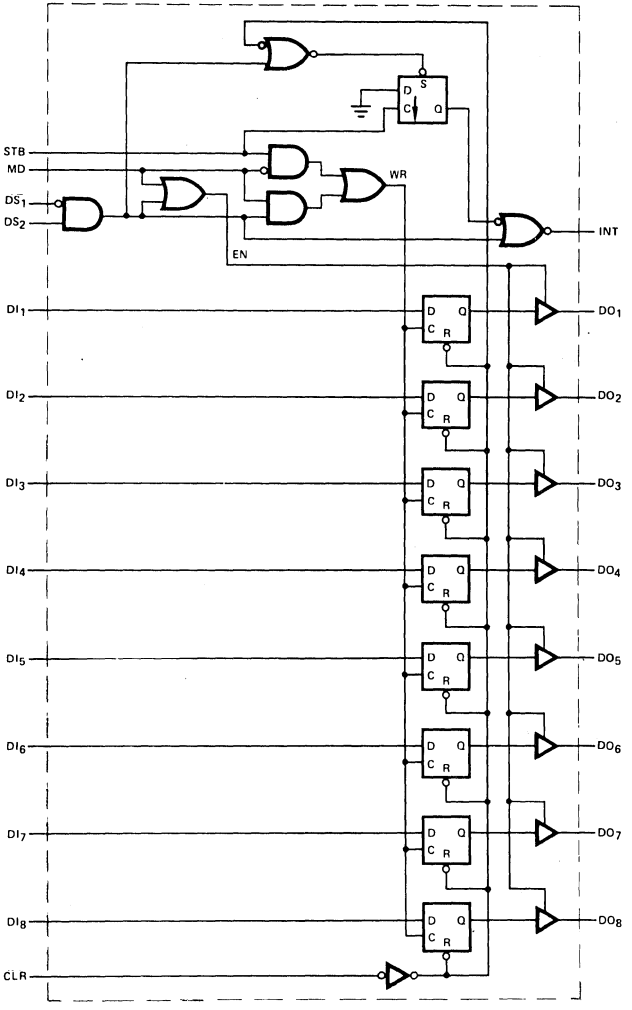
When MD is high, the device is in the output mode and, as a result, the output buffers are enabled. In this mode, the write signal for the data latch is obtained from the device select logic.

SERVICE REQUEST FLIP-FLOP AND STROBE

The service request flip-flop SR is used to generate and control central processor interrupt signals. For system reset, the SR flip-flop is placed in the non-interrupting state (i.e., SR is set) by bringing the CLR line low. This simultaneously clears (resets) the 8-bit data latch.

The Q output of the SR flip-flop is logically ORed with the output of device select logic and then inverted to provide the interrupt output INT. The 3212 is considered to be in the interrupting state when the INT output is low. This allows direct connection to the active LOW priority request inputs of the INTEL®3214 Interrupt Control Unit.

When operated in the input mode (i.e., MD low) the strobe input STB is used to synchronously write data into the data latch and place the SR flip-flop in the interrupting (reset) state. The interrupt is removed by the central processor when the interrupting 3212 is selected.



M3212 Logic Diagram

SERIES 3000

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +160°C

All Output and Supply Voltages . . . . . −0.5V to +7V

All Input Voltages . . . . . −1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +75°C V_{CC} = +5V ±5%

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_F	Input Load Current STB, DS_2, CLR, DI_1–DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current STB, DS, CLR, DI_1–DI_8 Inputs			10	μA	V_R = 5.25V
I_R	Input Leakage Current MD Input			30	μA	V_R = 5.25V
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = 5.25V
V_C	Input Forward Voltage Clamp			−1	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 15 mA
V_{OH}	Output "High" Voltage	3.65	4.0		V	I_{OH} = −1 mA
I_{SC}	Short Circuit Output Current	−15		−75	mA	V_{CC} = 5.0V
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	V_O = .45V/5.25V
I_{CC}	Power Supply Current		90	130	mA	

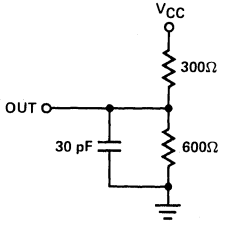
A.C. CHARACTERISTICS $T_A = 0°C$ to $75°C$, $V_{CC} = +5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	
t_{PW}	Pulse Width	25			ns	
t_{PD}	Data To Output Delay			30	ns	
t_{WE}	Write Enable To Output Delay			40	ns	
t_{SET}	Data Setup Time	15			ns	
t_H	Data Hold Time	20			ns	
t_R	Reset To Output Delay			40	ns	
t_S	Set To Output Delay			30	ns	
t_E	Output Enable Time			45	ns	C_L = 30 pf
t_C	Clear To Output Display			45	ns	

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 15 mA and 30 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:



SERIES 3000

CAPACITANCE[1]

Symbol	Test	LIMITS Min.	Typ.	Max.	Units
C_{IN}	DS_1, MD Input Capacitance		9	12	pf
C_{IN}	DS_2, CLR, STB, DI_1–DI_8 Input Capacitance		5	9	pf
C_{OUT}	DO_1–DO_8 Output Capacitance		8	12	pf

NOTE:
(1) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and $T_A = 25°C$.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C

Storage Temperature . . . . . −65°C to +160°C

All Output and Supply Voltages . . . . . −0.5V to +7V

All Input Voltages . . . . . −1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = −55°C to +125°C; V_{CC} = 5.0V ±10%

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_F	Input Load Current STB, DS_2, CLR, DI_1–DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current STB, DS, CLR, DI_1–DI_8 Inputs			10	μA	V_R = 5.5V
I_R	Input Leakage Current MD Input			30	μA	V_R = 5.5V
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = 5.5V
V_C	Input Forward Voltage Clamp			1.2	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 10 mA
V_{OH}	Output "High" Voltage	3.5	4.0		V	I_{OH} = .5 mA
I_{SC}	Short Circuit Output Current	−15		−75	mA	V_{CC} = 5.0V
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	V_O = .45V/5.5V
I_{CC}	Power Supply Current		90	145	mA	

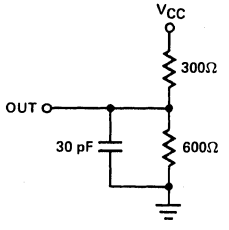
A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min.	Typ.	Max.	Unit	
t_{PW}	Pulse Width	40			ns	
t_{PD}	Data To Output Delay			30	ns	
t_{WE}	Write Enable To Output Delay			50	ns	
t_{SET}	Data Setup Time	20			ns	
t_H	Data Hold Time	30			ns	
t_R	Reset To Output Delay			55	ns	
t_S	Set To Output Delay			35	ns	
t_E	Output Enable Time			50	ns	C_L = 30 pf
t_C	Clear To Output Display			55	ns	

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 15 mA and 30 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:



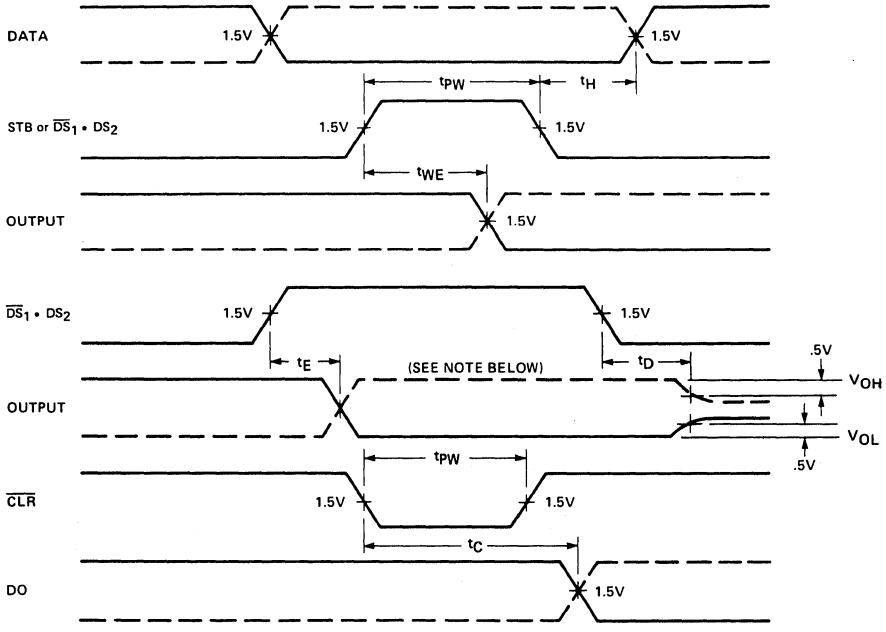
SERIES 3000

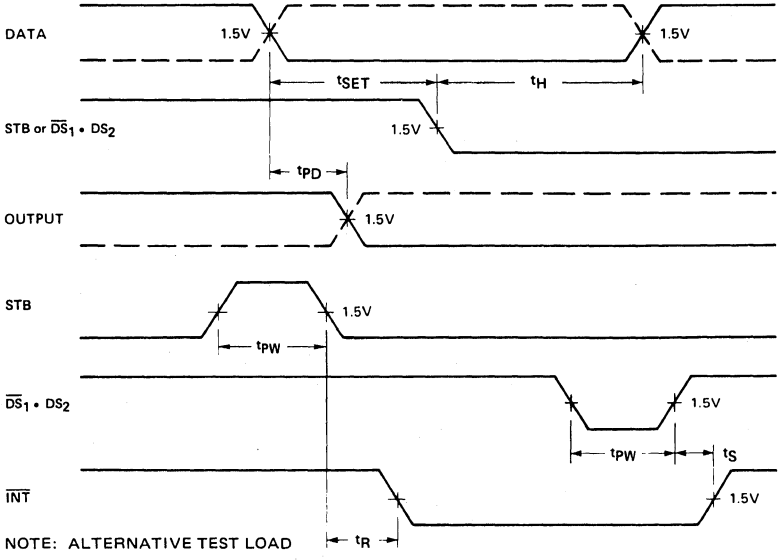
CAPACITANCE[1]

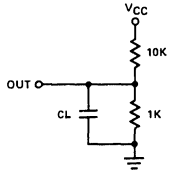
Symbol	Test	LIMITS Min.	Typ.	Max.	Units
C_{IN}	DS_1, MD Input Capacitance		9	12	pf
C_{IN}	DS_2, CLR, STB, DI_1–DI_8 Input Capacitance		5	9	pf
C_{OUT}	DO_1–DO_8 Output Capacitance		8	12	pf

NOTE:
(1) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and T_A = 25°C.

WAVEFORMS







SERIES 3000

3214

INTERRUPT CONTROL UNIT

The Intel®3214 Interrupt Control Unit (ICU) implements multi-level interrupt capability for systems designed with Series 3000 computing elements.

The ICU accepts an asynchronous interrupt strobe from the 3001 Microprogram Control Unit or a bit in microprogram memory and generates a synchronous interrupt acknowledge and an interrupt vector which may be directed to the MCU or CP Array to uniquely identify the interrupt source.

The ICU is fully expandable in 8-level increments and provides the following system capabilities:

- Eight unique priority levels per ICU
- Automatic Priority Determination
- Programmable Status
- N-level expansion capability
- Automatic interrupt vector generation

High Performance – 80 ns Cycle Time

Compatible with Intel 3001 MCU and 3002 CPE

8-Bit Priority Interrupt Request Latch

4-Bit Priority Status Latch

3-Bit Priority Encoder with Open Collector Outputs

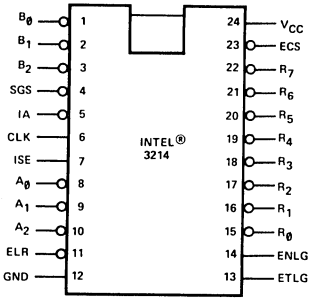
DTL and TTL Compatible

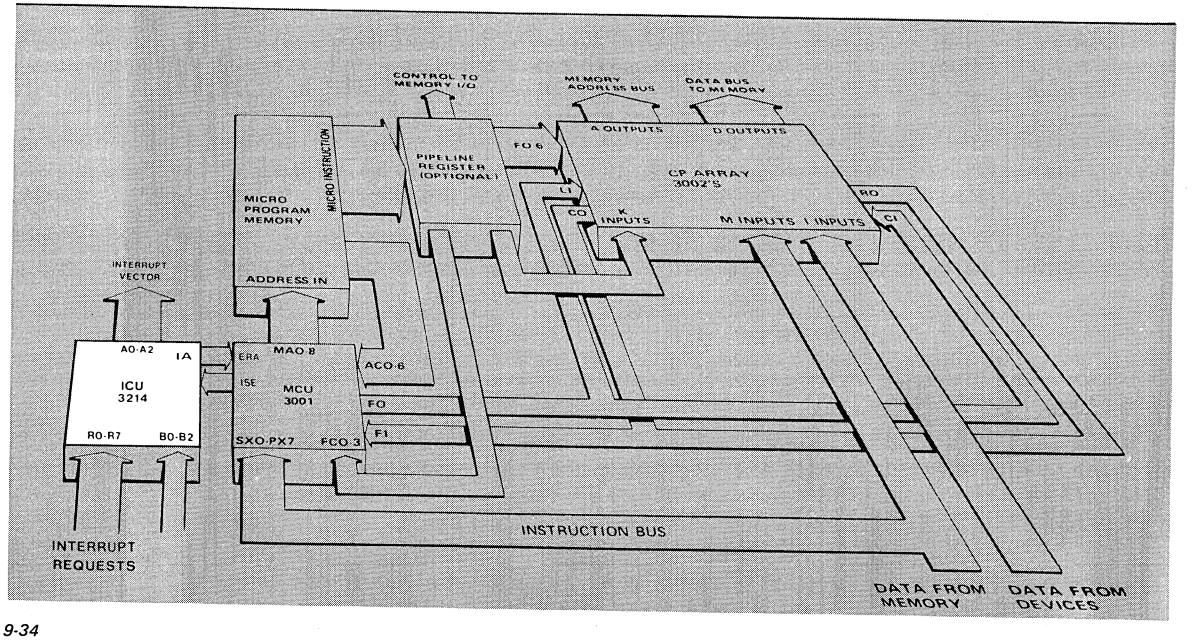
8-Level Priority Comparator

Fully Expandable

24-Pin DIP

PACKAGE CONFIGURATION





SERIES 3000

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1–3	B_0–B_2	Current Status Inputs The Current Status inputs carry the binary value modulo 8 of the current priority level to the current status latch.	Active LOW
4	SGS	Status Group Select Input The Status Group Select input informs the ICU that the current priority level does belong to the group level assigned to the ICU.	Active LOW
5	IA	Interrupt Acknowledge The Interrupt Acknowledge Output will only be active from the ICU (multi-ICU system) which has received a priority request at a level superior to the current status. It signals the controlled device (usually the processor) and the other ICUs OR-tied on the Interrupt Acknowledge line that an interrupt request has been recognized. The IA signal also sets the Interrupt Disable flip-flop (it overrides the clear function of the ECS input).	Active LOW Open-Collector Output
6	CLK	Clock Input The Clock input is used to synchronize the interrupt acknowledge with the operation of the device which it controls.	
7	ISE	Interrupt Strobe Enable Input The Interrupt Strobe Enable input informs the ICU that it is authorized to enter the interrupt mode.	
8–10	A_0–A_2	Request Level Outputs When valid, the Request Level outputs carry the binary value (modulo 8) of the highest priority request present at the priority request inputs or stored in the priority request latch. The request level outputs can become active only with the ICU which has received the highest priority request with a level superior to the current status.	Active LOW Open-Collector
11	ELR	Enable Level Read Input When active, the Enable Level Read input enables the Request Level output buffers (A_0–A_2).	Active LOW
12	GND	Ground	
13	ETLG	Enable This Level Group Input The Enable This Level Group input allows a higher priority ICU in multi-ICU systems to inhibit interrupts within the next lower priority ICU (and all the following ICUs).	
14	ENLG	Enable Next Level Group Output The Enable Next Level Group output allows the ICU to inhibit interrupts within the lower priority ICU in a multi-ICU system.	
15–22	R_0–R_7	Priority Interrupt Request Inputs The Priority Interrupt Request inputs are the inputs of the priority Interrupt Request Latch. The lowest priority level interrupt request signal is attached to R_0 and the highest is attached to R_7.	Active LOW
23	ECS	Enable Current Status Input The Enable Current Status input controls the current status latch and the clear function of the Interrupt Inhibit flip-flop.	Active LOW
24	V_{CC}	+5 Volt Supply	

NOTE:
(1) Active HIGH, unless otherwise noted.

FUNCTIONAL AND LOGICAL DESCRIPTION

The ICU adds interrupt capability to suitably microprogrammed processors or controllers. One or more of these units allows external signals called interrupt requests to cause the processor/controller to suspend execution of the active process, save its status, and initiate execution of a new task as requested by the interrupt signal.

It is customary to strobe the ICU at the end of each instruction execution. At that time, if an interrupt request is acknowledged by the ICU, the MCU is forced to follow the interrupt microprogram sequence.

Figure 1 shows the block diagram of the ICU. Interrupt requests pass through the interrupt request latch and priority encoder to the magnitude comparator. The output of the priority encoder is the binary equivalent of the highest active priority request. At the comparator, this value is compared with the Current Status (currently active priority level) contained in the current status latch. A request, if acknowledged at interrupt strobe time, will cause the interrupt flip-flop to enter the "interrupt active" state for one microinstruction cycle. This action causes the interrupt acknowledge (IA) signal to go low and sets the interrupt disable flip-flop.

The IA signal constitutes the interrupt command to the processor. It can directly force entry into the interrupt service routine as demonstrated in the appendix. As part of this routine, the microprogram normally reads the requesting level via the request level output bus. This information which is saved in the request latch can be enabled onto one of the processor input data buses using the enable level read input. Once the interrupt handler has determined the requesting level, it normally writes this level back into the current status register of the ICU. This action resets the interrupt disable flip-flop and acts to block any further request at this level or lower levels.

Entry into a macro level interrupt service routine may be vectored using the request level information to generate a subroutine address which corresponds to the level. Exit from such a macroprogram should normally restore the prior status in the current status latch.

The Enable This Level Group (ETLG) input and the Enable Next Level Group (ENLG) output can be used in a daisy chain fashion, as each ICU is capable of inhibiting interrupts from all of the following ICUs in a multiple ICU configuration.

The interrupt acknowledge flip-flop is set to the active LOW state on the rising edge of the clock when the following conditions are met:

- An active request level (R_0–R_7) is greater than the current status B_0–B_2
- The interrupt mode (ISE) is active
- ETLG is enabled
- The interrupt disable flip-flop is reset

When active, the IA signal asynchronously sets the disable flip-flop and holds the requests in the request latch until new current status information (B_0–B_2, SGS) is enabled (ECS) into the current status latch. The disable flip-flop is reset at the completion of this load operation.

During this process, ENLG will be enabled only if the following conditions are met:

- ETLG is enabled
- The current status (SGS) does not belong to this level group
- There is no active request at this level

The request level outputs A_0–A_2 and the IA output are open-collector to permit bussing of these lines in multi-ICU configuration.

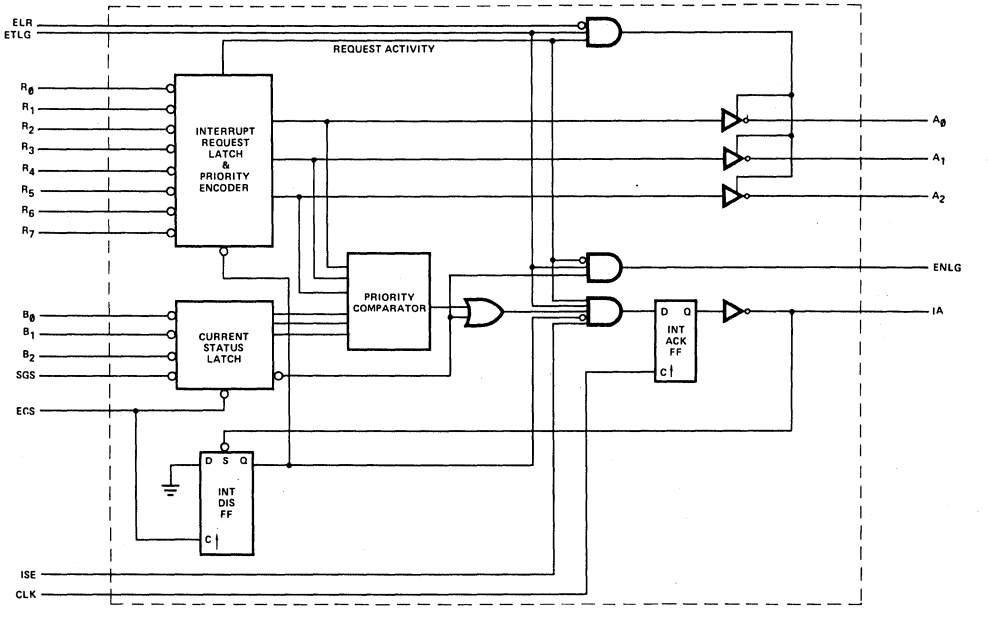


Figure 1. 3214 Block Diagram.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
- Ceramic . . . . . -65°C to +75°C
- Plastic . . . . . 0°C to +75°C

Storage Temperature . . . . . -65°C to +160°C

All Output and Supply Voltages . . . . . -0.5V to +7V

All Input Voltages . . . . . -1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER		LIMITS MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (all inputs)				-1.0	V	I_C = -5 mA
I_F	Input Forward Current:	ETLG input		-.15	-0.5	mA	V_F = 0.45V
		all other inputs		-.08	-0.25	mA	
I_R	Input Reverse Current:	ETLG input			80	μA	V_R = 5.25V
		all other inputs			40	μA	
V_{IL}	Input LOW Voltage:	all inputs			0.8	V	V_{CC} = 5.0V
V_{IH}	Input HIGH Voltage:	all inputs	2.0			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current(2)			90	130	mA	
V_{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I_{OL} = 15 mA
V_{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current:	ENLG output	-20	-35	-55	mA	V_{CC} = 5.0V
I_{CEX}	Output Leakage Current:	IA and A_0–A_2 outputs			100	μA	V_{CEX} = 5.25V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) B_0-B_2, SGS, CLK, R_0-R_4 grounded, all other inputs and all outputs open.

A.C: CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = +5V ± 5%

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
t_{CY}	CLK Cycle Time	80			ns
t_{PW}	CLK, ECS, IA Pulse Width	25	15		ns
	Interrupt Flip-Flop Next State Determination:				
t_{ISS}	ISE Set-Up Time to CLK	16	12		ns
t_{ISH}	ISE Hold Time After CLK	20	10		ns
t_{ETCS}[2]	ETLG Set-Up Time to CLK	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After CLK	20	10		ns
t_{ECCS}[3]	ECS Set-Up Time to CLK (to clear interrupt inhibit prior to CLK)	80	25		ns
t_{ECCH}[3]	ECS Hold Time After CLK (to hold interrupt inhibit)	0			ns
t_{ECRS}[3]	ECS Set-Up Time to CLK (to enable new requests through the request latch)	110	70		ns
t_{ECRH}[3]	ECS Hold Time After CLK (to hold requests in request latch)	0			
t_{ECSS}[2]	ECS Set-Up Time to CLK (to enable new status through the status latch)	75	70		ns
t_{ECSH}[2]	ECS Hold Time After CLK (to hold status in status latch)	0			ns
t_{DCS}[2]	SGS and $B_\emptyset$-B_2 Set-Up Time to CLK (current status latch enabled)	70	50		ns
t_{DCH}[2]	SGS and $B_\emptyset$-B_2 Hold Time After CLK (current status latch enabled)	0			ns
t_{RCS}[3]	$R_\emptyset$-R_7 Set-Up Time to CLK (request latch enabled)	90	55		ns
t_{RCH}[3]	$R_\emptyset$-R_7 Hold Time After CLK (request latch enabled)	0			ns
t_{ICS}	IA Set-Up Time to CLK (to set interrupt inhibit F.F. before CLK)	55	35		ns
t_{CI}	CLK to IA Propagation Delay		15	25	ns
	Contents of Request Latch and Request Level Output Status Determination:				
t_{RIS}[4]	$R_\emptyset$-R_7 Set-Up Time to IA	10	0		ns
t_{RIH}[4]	$R_\emptyset$-R_7 Hold Time After IA	35	20		ns
t_{RA}	$R_\emptyset$-R_7 to $A_\emptyset$-A_2 Propagation Delay (request latch enabled)		80	100	ns
t_{ELA}	ELR to $A_\emptyset$-A_2 Propagation Delay		40	55	ns
t_{ECA}	ECS to $A_\emptyset$-A_2 Propagation Delay (to enable new requests through request latch)		100	120	ns
t_{ETA}	ETLG to $A_\emptyset$-A_2 Propagation Delay		35	70	ns

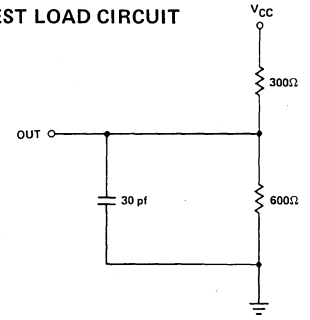
A.C. CHARACTERISTICS (CON'T)

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
	Contents of Current Priority Status Latch Determination:				
t_{DECS}[4]	SGS and $B_\emptyset$-B_2 Set-Up Time to ECS	15	10		ns
t_{DECH}[4]	SGS and $B_\emptyset$-B_2 Hold Time After ECS	15	10		ns
	Enable Next Level Group Determination:				
t_{REN}	$R_\emptyset$-R_7 to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	ECS to ENLG Propagation Delay (enabling new request through the request latch)		85	90	ns
t_{ECSN}	ECS to ENLG Propagation Delay (enabling new SGS through status latch)		35	55	ns

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) Required for proper operation if ISE is enabled during next clock pulse.
(3) These times are not required for proper operation but for desired change in interrupt flip-flop.
(4) Required for new request or status to be properly loaded.
(5) $t_{CY} = t_{ICS} + t_{CI}$

TEST CONDITIONS:
Input pulse amplitude: 2.5 volts.
Input rise and fall times: 5 ns between 1 and 2 volts.
Output loading of 15 mA and 30 pf.
Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT



CAPACITANCE(5)

T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pf
C_{OUT}	Output Capacitance		7	12	pf

TEST CONDITIONS:
V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

NOTE:
(5) This parameter is periodically sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
CerDip . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = -55°C to +125°C; V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER		LIMITS MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (all inputs)				-1.2	V	I_C = -5 mA
I_F	Input Forward Current:	ETLG input		-.15	-0.5	mA	V_F = 0.45V
		all other inputs		-.08	-0.25	mA	
I_R	Input Reverse Current:	ETLG input			80	μA	V_R = 5.5V
		all other inputs			40	μA	
V_{IL}	Input LOW Voltage:	all inputs			0.8	V	V_{CC} = 5.0V
V_{IH}	Input HIGH Voltage:	all inputs	2.0			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current(2)			90	130	mA	
V_{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I_{OL} = 10 mA
V_{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current:	ENLG output	-15	-35	-55	mA	V_{CC} = 5.0V
I_{CEX}	Output Leakage Current:	IA and A_0-A_3 outputs			100	μA	V_{CEX} = 5.5V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) B_0-B_2, SGS, CLK, R_0-R_4 grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS

T_A = -55°C to +125°C; V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
t_{CY}	CLK Cycle Time(5)	85			ns
t_{PW}	CLK, ECS, IA Pulse Width	25	15		ns
	Interrupt Flip-Flop Next State Determination:				
t_{ISS}	ISE Set-Up Time to CLK	16	12		ns
t_{ISH}	ISE Hold Time After CLK	20	10		ns
t_{ETCS}[2]	ETLG Set-Up Time to CLK	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After CLK	20	10		ns
t_{ECCS}[3]	ECS Set-Up Time to CLK (to clear interrupt inhibit prior to CLK)	85	25		ns
t_{ECCH}[3]	ECS Hold Time After CLK (to hold interrupt inhibit)	0			ns
t_{ECRS}[3]	ECS Set-Up Time to CLK (to enable new requests through the request latch)	110	70		ns
t_{ECRH}[3]	ECS Hold Time After CLK (to hold requests in request latch)	0			
t_{ECSS}[2]	ECS Set-Up Time to CLK (to enable new status through the status latch)	85	70		ns
t_{ECSH}[2]	ECS Hold Time After CLK (to hold status in status latch)	0			ns
t_{DCS}[2]	SGS and $B_Ø$-B_2 Set-Up Time to CLK (current status latch enabled)	90	50		ns
t_{DCH}[2]	SGS and $B_Ø$-B_2 Hold Time After CLK (current status latch enabled)	0			ns
t_{RCS}[3]	$R_Ø$-R_7 Set-Up Time to CLK (request latch enabled)	100	55		ns
t_{RCH}[3]	$R_Ø$-R_7 Hold Time After CLK (request latch enabled)	0			ns
t_{ICS}	IA Set-Up Time to CLK (to set interrupt inhibit F.F. before CLK)	55	35		ns
t_{CI}	CLK to IA Propagation Delay		15	30	ns
	Contents of Request Latch and Request Level Output Status Determination:				
t_{RIS}[4]	$R_Ø$-R_7 Set-Up Time to IA	10	0		ns
t_{RIH}[4]	$R_Ø$-R_7 Hold Time After IA	35	20		ns
t_{RA}	$R_Ø$-R_7 to $A_Ø$-A_2 Propagation Delay (request latch enabled)		80	100	ns
t_{ELA}	ELR to $A_Ø$-A_2 Propagation Delay		40	55	ns
t_{ECA}	ECS to $A_Ø$-A_2 Propagation Delay (to enable new requests through request latch)		100	130	ns
t_{ETA}	ETLG to $A_Ø$-A_2 Propagation Delay		35	70	ns

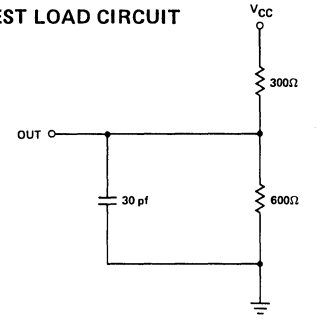
A.C. CHARACTERISTICS (CON'T)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP(1)	LIMITS MAX	UNIT
	Contents of Current Priority Status Latch Determination:				
t_{DECS}[4]	SGS and $B_Ø$-B_2 Set-Up Time to ECS	20	10		ns
t_{DECH}[4]	SGS and $B_Ø$-B_2 Hold Time After ECS	20	10		ns
	Enable Next Level Group Determination:				
t_{REN}	$R_Ø$-R_7 to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	30	ns
t_{ECRN}	ECS to ENLG Propagation Delay (enabling new request through the request latch)		85	110	ns
t_{ECSN}	ECS to ENLG Propagation Delay (enabling new SGS through status latch)		35	55	ns

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) Required for proper operation if ISE is enabled during next clock pulse.
(3) These times are not required for proper operation but for desired change in interrupt flip-flop.
(4) Required for new request or status to be properly loaded.
(5) $t_{CY} = t_{ICS} + t_{CI}$

TEST CONDITIONS:
Input pulse amplitude: 2.5 volts.
Input rise and fall times: 5 ns between 1 and 2 volts.
Output loading of 15 mA and 30 pf.
Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT



SERIES 3000

CAPACITANCE(5)

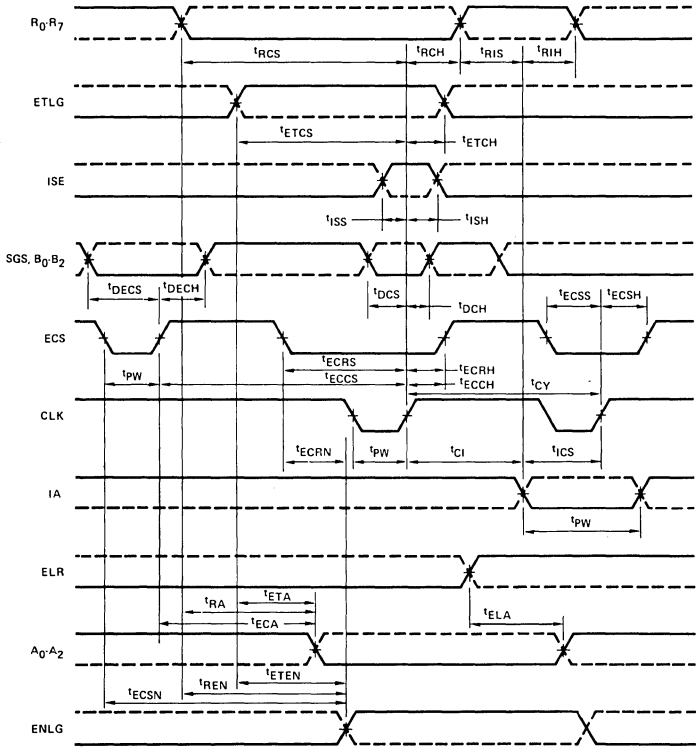
T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP(1)	LIMITS MAX	UNIT
C_{IN}	Input Capacitance		5	10	pf
C_{OUT}	Output Capacitance		7	12	pf

TEST CONDITIONS:
V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

NOTE:
(5) This parameter is periodically sampled and not 100% tested.

WAVEFORMS


R_0-R_7
t_{RCS}
t_{RCH}
t_{RIS}
t_{RIH}
ETLG
t_{ETCS}
t_{ETCH}
ISE
t_{ISS}
t_{ISH}
SGS, B_0-B_2
t_{DECS}
t_{DECH}
t_{DCS}
t_{DCH}
t_{ECSS}
t_{ECSH}
ECS
t_{ECRS}
t_{ECCS}
t_{ECRH}
t_{ECCH}
t_{PW}
t_{CY}
CLK
t_{ECRN}
t_{PW}
t_{CI}
t_{ICS}
IA
t_{PW}
ELR
t_{RA}
t_{ETA}
t_{ECA}
t_{ELA}
A_0-A_2
t_{ETEN}
t_{REN}
t_{ECSN}
ENLG

3216/3226

PARALLEL BIDIRECTIONAL BUS DRIVER

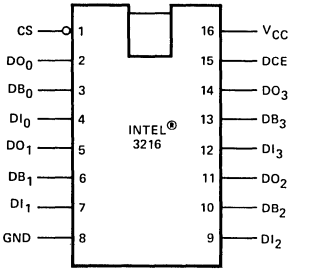
The INTEL® 3216 is a high-speed 4-bit Parallel, Bidirectional Bus Driver. Its three-state outputs enable it to isolate and drive external bus structures associated with Series 3000 systems

The INTEL 3226 is a high-speed 4-bit Parallel, Inverting Bidirectional Bus Driver. Its three-state outputs enable it to isolate and drive external bus structures associated with Series 3000 systems.

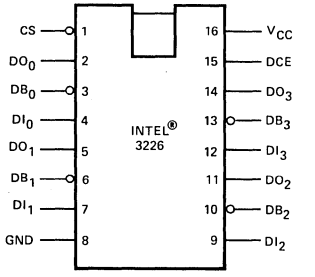
The 3216/3226 driver and receiver gates have three state outputs with PNP inputs. When the drivers or receivers are tri-stated the inputs are disabled, presenting a low current load, typically less than 40 μamps, to the system bus structure.

- **High Performance—25 ns typical propagation delay**
- **Low Input Load Current—0.25 mA maximum**
- **High Output Drive Capability for Driving System Data Busses**
- **Three-State Outputs**
- **TTL Compatible**
- **16-pin DIP**

PACKAGE CONFIGURATION

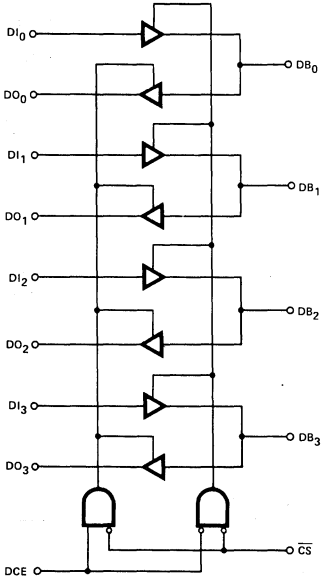


3216

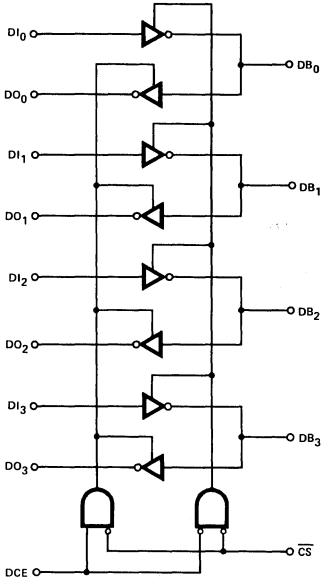


3226

LOGIC DIAGRAM 3216



LOGIC DIAGRAM 3226



SERIES 3000

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias

Ceramic	-65°C to +75°C
Plastic	0°C to +75°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	125 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

T_A = 0°C to +75°C, V_{CC} = +5.0V ±5%

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Condition
I_F	Input Load Current					
	DCE, $\overline{CS}$ Inputs		-0.15	-0.5	mA	V_F = 0.45V
	All Other Inputs		-0.08	-0.25	mA	
I_R	Input Leakage Current					
	DCE, $\overline{CS}$ Inputs			80	µA	V_R = 5.25V
	DI Inputs			40	µA	
V_C	Input Clamp Voltage			-1	V	I_C = -5mA
V_{IL}	Input Low Voltage			0.95	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	V_{CC} = 5.0V
V_{OL1}	Output Low Voltage		0.3	0.45	V	DO Outputs I_{OL}=15mA
	DO, DB Outputs					DB Outputs I_{OL}=25mA
V_{OL2}	Output Low Voltage		0.5	0.6	V	DB Outputs I_{OL} = 50mA
	DB Outputs Only					
V_{OH1}	Output High Voltage	3.65	4.0		V	I_{OH}=-1mA
	DO Outputs Only					
V_{OH2}	Output High Voltage	2.4	3.0		V	I_{OH}=-10mA
	DB Outputs Only					
I_{SC}	Output Short Circuit Current					
	DO Outputs	-15	-35	-65	mA	V_{CC} = 5.0V
	DB Outputs	-30	-75	-120	mA	
$\|I_O\|$	Output Leakage Current					
	High Impedance State					
	DO Outputs			20	µA	V_O=0.45V/5.25V
	DB Outputs			100	µA	
I_{CC}	Power Supply Current 3216		95	130	mA	
	3226		85	120	mA	

NOTE: Typical values are for T_A = 25°C

SERIES 3000

A.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = +5.0V ±5%

Symbol	Parameter		Limit Min.	Typ.	Max.	Unit	Condition
T_{PD1}	Input to Output Delay DO Outputs	3216		15	25	ns	C_L=30pF, R_1=300Ω, R_2=600Ω
		3226		14	25		
T_{PD2}	Input to Output Delay DB Outputs	3216		19	30	ns	C_L=300pF, R_1=90Ω, R_2=180Ω
		3226		16	25		
T_E	Output Enable Time DCE, CS	3216		42	65	ns(2)	DO Outputs: C_L=30pF, R_1=300Ω/10KΩ, R_2=600Ω/1KΩ
		3226		36	54		DB Outputs: C_L=300pF, R_1=90Ω/10KΩ, R_2=180Ω/1KΩ
T_D	Output Disable Time DCE, CS			16	35	ns(2)	DO Outputs: C_L=5pF, R_1=300Ω/10KΩ, R_2=600Ω/1KΩ
							DB Outputs: C_L=5pF, R_1=90Ω/10KΩ, R_2=180Ω/1KΩ

NOTE: (1) Typical values are for T_A = 25°C and nominal supply voltage.

(2) The test load circuit is set for worst case source and sink loading on the outputs. The two resistor values for R1 and R2 correspond to worst case sink and source loading, respectively.

CAPACITANCE(2) T_A = 25°C

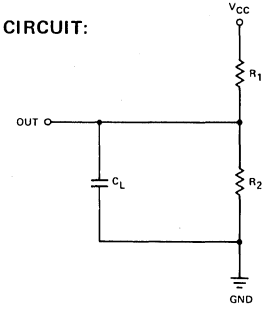
Symbol	Parameter	Limit Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance		4	6	pF
C_{OUT}	Output Capacitance				
	DO Outputs		6	10	pF
	DB Outputs		13	18	pF

Note:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V and T_A = 25°C.

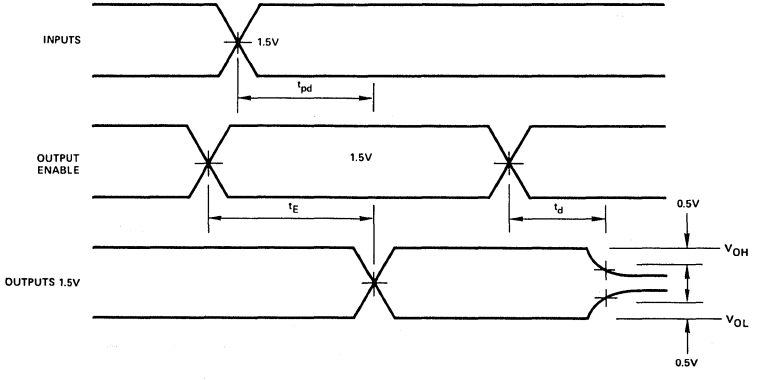
TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



WAVEFORMS



SERIES 3000

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
Ceramic . . . . . -65°C to +75°C

Storage Temperature . . . . . -65°C to +160°C

All Output and Supply Voltages . . . . . -0.5V to +7V

All Input Voltages . . . . . -1.0V to +5.5V

Output Currents . . . . . 125 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

T_A = -55°C to +125°C, V_{CC} = +5.0V ±10%

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Condition
I_F	Input Load Current					
	DCE, $\overline{CS}$ Inputs		-0.15	-0.5	mA	V_F = 0.45V
	All Other Inputs		-0.08	-0.25	mA	
I_R	Input Leakage Current					
	DCE, $\overline{CS}$ Inputs			80	µA	V_R = 5.5V
	DI Inputs			40	µA	
V_C	Input Clamp Voltage			-1.2	V	I_C = -5mA
V_{IL}	Input Low Voltage M3216			0.95	V	V_{CC} = 5.0V
	M3226			0.90	V	
V_{IH}	Input High Voltage	2.0			V	V_{CC} = 5.0V
V_{OL1}	Output Low Voltage DO, DB Outputs		0.3	0.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output Low Voltage DB Outputs Only		0.5	0.6	V	DB Outputs I_{OL} = 45mA
V_{OH1}	Output High Voltage DO Outputs Only	3.4	3.8		V	I_{OH}=-0.5mA I_{OH}=-2.0mA
V_{OH2}	Output High Voltage DB Outputs Only	2.4	3.0		V	I_{OH}=-5mA
I_{SC}	Output Short Circuit Current					
	DO Outputs	-15	-35	-65	mA	V_{CC} = 5.0V
	DB Outputs	-30	-75	-120	mA	
$\lvert I_O \rvert$	Output Leakage Current High Impedance State					
	DO Outputs			20	µA	V_O=0.45V/5.5V
	DB Outputs			100	µA	
I_{CC}	Power Supply Current M3216		95	130	mA	
	M3226		85	120	mA	

NOTE: Typical values are for T_A = 25°C

SERIES 3000

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter		Limit Min.	Typ.	Max.	Unit	Condition
T_{PD1}	Input to Output Delay DO Outputs			15	25	ns	C_L=30pF, R_1=300Ω, R_2=600Ω
T_{PD2}	Input to Output Delay DB Outputs	M3216		19	33	ns	C_L=300pF, R_1=90Ω, R_2=180Ω
		M3226		16	25		
T_E	Output Enable Time	M3216		42	75	ns(2)	DO Outputs: C_L=30pF, R_1=300Ω/10KΩ, R_2=600Ω/1KΩ
		M3226		36	62		DB Outputs: C_L=300pF, R_1=90Ω/10KΩ, R_2=180Ω/1KΩ
T_D	Output Disable Time	M3216		16	40	ns(2)	DO Outputs: C_L=5pF, R_1=300Ω/10KΩ, R_2=600Ω/1KΩ
		M3226		16	38		DB Outputs: C_L=5pF, R_1=90Ω/10KΩ, R_2=180Ω/1KΩ

NOTE: (1) Typical values are for T_A = 25°C and nominal supply voltage.

(2) The test load circuit is set for worst case source and sink loading on the outputs. The two resistor values for R1 and R2 correspond to worst case sink and source loading, respectively.

CAPACITANCE(2) T_A = 25°C

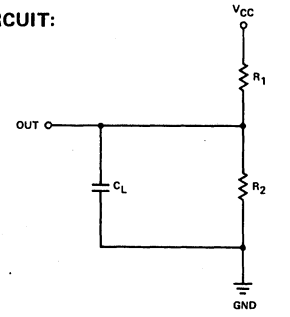
Symbol	Parameter	Limit Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance		4	6	pF
C_{OUT}	Output Capacitance				
	DO Outputs		6	10	pF
	DB Outputs		13	18	pF

Note:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V and T_A = 25°C.

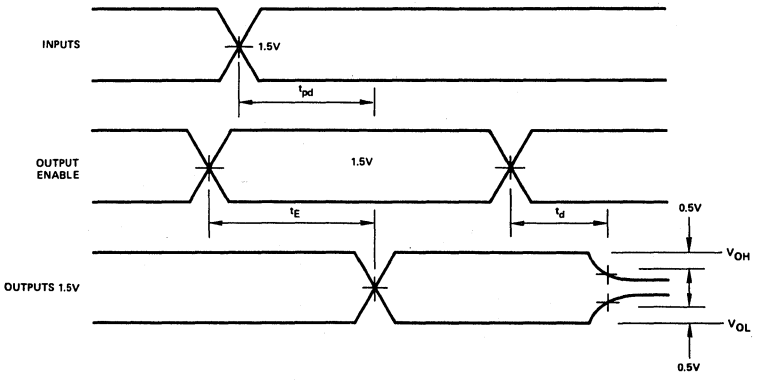
TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



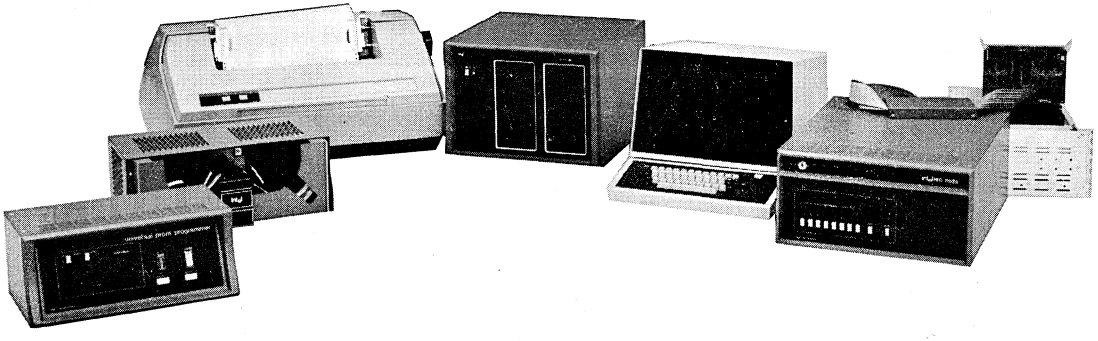
WAVEFORMS



SERIES 3000

10

DEVELOPMENT SYSTEMS



MICROCOMPUTER DEVELOPMENT SYSTEMS

This section contains information necessary to select the appropriate Intel design aids required to facilitate microprocessor hardware and software development. Design aids cover the broad range from the Intellec® MDS system with its in-circuit emulator options for both the Intel 8080 (ICE-80) and the Series 3000 Bipolar Microcomputer (ICE-30), to the extensive User's Program Library and a selection of 3 and 4 day Microcomputer Workshops. The purpose of development aids is to shorten the design cycle and thus save time and money in the development and production of microcomputer-based products.

MDS-800 INTELLEC® MDS MICROCOMPUTER DEVELOPMENT SYSTEM

Modular microcomputer development system for development and implementation of MCS™-80 and Series 3000 Microcomputer Systems

Intel 8080 microprocessor, with 2 μs cycle time and 78 instructions, controls all Intellec MDS functions.

16K bytes RAM memory expandable to 64K bytes.

2K bytes ROM memory expandable to 14K bytes.

Hardware interfaces and software drivers provided for TTY, CRT, line printer, high speed paper tape reader, high speed paper tape punch, and Universal PROM Programmer.

Universal bus structure with multiprocessor and DMA capabilities.

Eight level nested, maskable, priority interrupt system.

Optional PROM programmer peripheral capable of programming all Intel PROMs.

ICE (In-Circuit Emulator) options extend Intellec MDS diagnostic capabilities into user configured system allowing real time emulation of user processors.

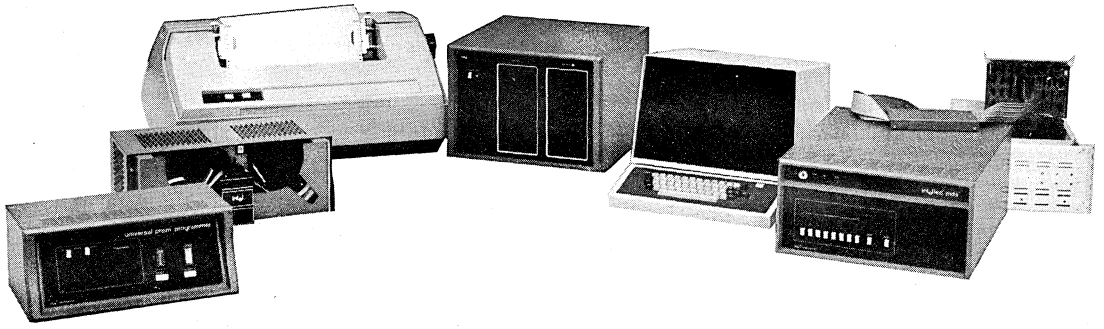
Optional I/O modules expandable in groups of four 8-bit input and output ports to a maximum of 88 ports (all TTL compatible).

ROM resident system monitor includes all necessary functions for program loading, debugging, and execution.

RAM resident macro assembler used to assemble all 8080 machine instructions with full macro and conditional assembly capabilities.

RAM resident text editor with powerful string search, substitution, insertion, and deletion commands.

The Intellec® MDS is a modular microcomputer development system containing all necessary hardware and software to develop and implement Intel MCS™-80 and Series 3000 microcomputer systems. The addition of MDS options and peripherals provides the user with a complete in-circuit microcomputer development system, supporting product design from program development through prototype debug, to production and field test.



INTELLEC® MDS HARDWARE

The standard Intellec® MDS consists of four microcomputer modules (CPU, 16K RAM Memory, Front Panel Control, and Monitor), an interconnecting printed circuit motherboard, power supplies, fans, a chassis, and a front panel. Modular expansion capability is provided by 14 additional sockets on the motherboard.

The CPU module uses Intel's powerful NMOS 8-bit 8080 microprocessor. The 8080's 2 μs cycle time, 78 instructions, unlimited subroutine nesting, vectored interrupt, and DMA capabilities are fully utilized by the Intellec MDS. Bus control logic resolves bus contention conflicts between the CPU module and other modules capable of acquiring control of the bus. The CPU module interfaces with a sixteen line address bus and a bidirectional eight line data bus. 8080 status signals are decoded and utilized for memory and I/O operations. An eight-level, nested interrupt priority system, complete with an interrupt priority push-down stack, resolves contention for 8080 interrupt servicing.

The RAM memory module contains 16K bytes of Intel 2107 dynamic RAM which operates at full processor speed. All necessary address decoding and refresh logic is contained on the module.

The front panel control module provides system initialization, priority arbitration, and real time clock functions. System initialization routines reside in a 256 byte, PROM resident, bootstrap loader. An eight-level priority arbitration network resolves bus contention requests among potential bus masters. A 1 ms interrupt request generator, which can be disabled under program control, provides real time clock functions. A 10 ms automatic time-out feature is also provided to force an interrupt request if nonexistent memory or I/O is addressed.

The Monitor module contains the Intellec MDS system monitor and all Intellec MDS peripheral interface hardware. The system monitor resides in a 2K byte Intel 8316 ROM. The module contains all necessary control and data transfer circuitry to interface with the following Intellec MDS peripherals:

- Teletype
- CRT
- High Speed Paper Tape Reader
- High Speed Paper Tape Punch
- PROM Programmer
- Line Printer

The Intellec MDS universal bus structure enables several CPU and DMA devices to share the bus by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal which is derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure contains provisions for up to 16-bit address and data transfers and is not limited to any one Intel microcomputer family.

The Intellec MDS front panel is intended to augment the primary user interaction medium, the system console. The simplicity of the front panel coupled with the power of the system monitor provides an efficient user/Intellec interface. The front panel contains eight interrupt request switches with corresponding indicators, CPU RUN and HALT status indicators, a bootstrap loader switch, RESET switch, and a POWER ON switch and indicator.

The basic Intellec MDS capabilities may be significantly enhanced by the addition of the following optional features.

ICE (In-Circuit Emulator) extends Intellec MDS diagnositc capabilities into user configured systems. The Intellec MDS resident ICE processor operates in conjunction with the MDS host CPU and interfaces to the user system via an external cable. The ICE processor replaces the user system processor providing real time emulation capability. MDS resident memory and I/O may be substituted for equivalent user system elements, allowing the hardware designer to sequentially develop his system by integrating MDS and user system hardware. MDS display and debug hardware eliminate the need for specially constructed user system equivalents. Augmenting these capabilities are such powerful ICE debug functions as setting breakpoints, tracing program flow, single stepping, examining and altering CPU registers and memory locations.

The Universal PROM Programmer is an Intellec MDS peripheral capable of programming and verifying the following Intel PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704, and 8708. Programming and verification operations are initiated from the Intellec MDS system console and are controlled by programs resident in the Intellec MDS and Universal PROM Programmer.

The addition of a single or dual drive Diskette Operating System significantly reduces program development time. An intelligent controller, constructed around Intel's powerful Series 3000 computing elements, provides diskette interface and control. Intel's software operating system (IDOS) in conjunction with the diskette operating system hardware provides a highly efficient and easy to use method of assembling, editing, and executing programs.

Customized user I/O requirements may be satisfied by adding I/O modules. Each I/O module contains four 8-bit input ports (latched or unlatched), four 8-bit latched output ports (with adjustable strobe pulses), and eight system interrupt lines. All inputs and outputs are TTL compatible. Optional I/O may be expanded to a maximum of 44 input and 44 output ports.

Memory may be expanded by adding RAM or PROM modules in user defined combinations. Up to 64K bytes of RAM may be added in 16K byte increments. PROM (Intel 8702A) may be added in 256 byte increments by adding PROM modules with socket capacity for 6K bytes and populating each module with the desired number of PROMs. Maximum PROM capacity is 12K bytes. RAM/PROM memory overlap is resolved by giving PROM priority.

DMA (direct memory access) modules work in conjunction with the Intellec MDS universal bus to maximize the efficiency of data transfers between MDS memory and selected I/O devices. Each module contains all the necessary control and data transfer logic to implement a complete DMA channel.

A ROM simulator composed of high speed bipolar RAM emulates Series 3000 bipolar microprogram ROM memory. Each ROM simulator module may be used in 512 X 16 or 1024 X 8 configurations.

INTELLEC® MDS SOFTWARE

Resident software provided with the Intellec® MDS includes the system monitor, 8080 macro assembler and text editor. Used together, these three programs simplify program preparation and speed the debugging task.

The system monitor provides complete control over operation of the Intellec MDS. All necessary functions for program loading and execution are provided. Additional commands provide extensive debug facilities and PROM programming functions. System peripherals may be dynamically assigned either via monitor commands or through calls to the system monitor's I/O subroutines.

Programs may be loaded from the reader device in either BNPF or hexadecimal format. Utility commands which aid in the execution and checkout of programs include:

- initialize memory to a constant
- move a block of memory to another location
- display memory
- modify RAM memory
- examine and modify CPU registers
- set breakpoints
- initiate execution at any given address
- perform hexadecimal arithmetic
- examine and modify the interrupt mask

The Intellec MDS System Monitor contains a powerful and easily expandable input/output system, which is built around four logical device types; console device, reader device, punch device and list device. Associated with each logical device may be any one of four physical devices. The user controls physical device assignment to each logical device through a System command.

Drivers are provided in the system monitor for the Universal PROM Programmer, ASR 33 teletype, high speed paper tape reader, high speed paper tape punch, line printer, and CRT. The user may write his own drivers for other peripheral devices and easily link them to the system monitor.

All system peripherals may be accessed simply by calling I/O subroutines in the system monitor. In addition, the user may dynamically reconfigure his system by monitor commands or by calling system subroutines which can assign a different physical device to each logical device. The user may also determine the current system peripheral configuration, check I/O status and determine the size of available memory.

The monitor is written in 8080 Assembly Language and resides in 2K bytes of ROM memory.

The Intellec MDS Resident Assembler translates symbolic 8080 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation.

Conditional assembly permits the assembler to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

The assembler performs its function in three passes. The first pass builds the symbol table. The second pass produces a source listing and provides error diagnostics. The third pass produces the object code. If the punch and list devices are separate (e.g. a high speed punch or printer is available) passes 2 and 3 may be combined into one pass.

Object code produced by the assembler is in hexadecimal format. It may be loaded directly into the Intellec MDS for execution and debugging or may be converted by the system monitor to BNPF format for ROM programming.

The assembler is written in PL/M[T.M.]-80, Intel's high level systems programming language. It occupies 12K bytes of RAM memory including space for over 800 symbols. The symbol table size may be expanded to a maximum of 6500 symbols by adding RAM memory. All I/O in the assembler is done through the system monitor, enabling the assembler to take advantage of the monitor's I/O system. The assembler is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec MDS.

The Intellec MDS editor is a comprehensive tool for the entry and correction of assembly language programs for the Intel 8080 microcomputer. Its command set allows manipulation of either entire lines of text or individual characters within a line.

Programs may be entered directly from the console keyboard or from the system reader device. Text is stored internally in the editor's workspace, and may be edited with the following commands:

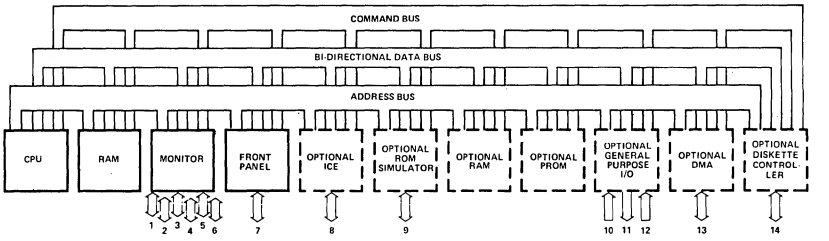
- string insertion or deletion
- string search
- string substitution

To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

The contents of the workspace may be listed to the system console or written to the system list or punch device for future use.

The text editor is written in PL/M[T.M.]-80. It occupies 8K bytes of RAM memory, including over 4500 bytes of workspace. The workspace may be expanded to a maximum of 58K bytes by adding RAM memory. All I/O in the editor is done through the system monitor, enabling the editor to take advantage of the monitor's I/O system. The editor is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec MDS.



NOTES:
1. PROM PROGRAMMER DATA/STATUS/COMMANDS
2. HIGH SPEED PUNCH DATA/STATUS/COMMANDS
3. HIGH SPEED READER DATA/STATUS/COMMANDS
4. PRINTER DATA/STATUS/COMMANDS
5. CRT DATA/STATUS/COMMANDS
6. TTY DATA/STATUS/COMMANDS
7. FRONT PANEL STATUS/SWITCH INPUTS
8. USER SYSTEM CPU OR MCU PIN SIGNALS
9. USER SYSTEM ROM PIN SIGNALS
10. EIGHT INTERRUPT LINES
11. FOUR 8-BIT OUTPUT PORTS
12. FOUR 8-BIT INPUT PORTS
13. DMA DEVICE DATA/STATUS/COMMANDS
14. DISKETTE DRIVE DATA/STATUS/COMMANDS

INTELLEC® MDS BLOCK DIAGRAM

HARDWARE SPECIFICATIONS

WORD SIZE
Host Processor (Intel 8080)
- Data: 8 bits
- Instruction, 8, 16, or 24 bits

MEMORY SIZE
RAM: 16K bytes expandable to 64K bytes using optional modules.

ROM: 2K bytes expandable to 14K bytes in 256 byte increments using optional PROM modules.

PROM: 256 bytes expandable to 12K bytes using optional modules.

Total: RAM, ROM and PROM may be combined in user defined configurations up to a maximum of 64K bytes.

MACHINE CYCLE TIME
Host Processor (Intel 8080): 2.0 μS

BUS TRANSFER RATE
Maximum bus transfer rate of 5 MHz.

SYSTEM CLOCKS
Host Processor (Intel 8080) Clock: Crystal controlled at 2 MHz ±0.1%.

Bus Clock: Crystal controlled at 9.8304 MHz ±0.1%.

I/O INTERFACES
CRT:
- Baud Rates: 110/300/600/1200/2400/4800/9600 (selectable).
- Code Format: 7–12 level code (programmable).
- Parity: Odd/even (programmable).
- Interface: TTL/RS232C (selectable).

TTY:
- Baud Rate: 110
- Code Format:
  - Input: 10 level or greater.
  - Output: 11 level.
  - Parity: Odd.
  - Interface: 20 mA current loop.

High Speed Paper Tape Reader:
- Transfer Rate: 200 cps.
- Control: 2-bit output. 1-bit input.
- Data: 8-bit byte
- Interface: TTL

Punch:
- Transfer Rate: 75 cps
- Control: 2-bit output 1-bit input
- Data: 8-bit byte
- Interface: TTL

Printer:
- Transfer Rate: 165 cps
- Control: 2-bit status input 1-bit output
- Data: ASCII
- Interface: TTL

PROM Programmer:
- Control: 3 strobes for multiplexed output data.
- Data: 8-bit bidirectional
- Interface: TTL

GENERAL PURPOSE I/O (OPTIONAL)
Input Ports: 8-bit TTL compatible (latched or unlatched); expandable in 4 port increments to 44 input ports.

Output Ports: 8-bit TTL compatible (latched); expandable in 4 port increments to 44.

Interrupts: 8 TTL compatible interrupt lines.

INTERRUPT
8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

DIRECT MEMORY ACCESS
Standard capability on Intellec bus; implemented for user selected DMA devices through optional DMA module – maximum transfer rate of 2 MHz.

MEMORY ACCESS TIME
RAM: 450 ns
PROM: 1.3 μs using Intel 8708A PROM.

PHYSICAL CHARACTERISTICS
Dimensions: 8.5" X 19" X 17"
21.6 cm X 48.3 cm X 43.2 cm
Weight: 65 lb (29.5 kg)

ELECTRICAL CHARACTERISTICS

DC POWER SUPPLY (Volts)	POWER SUPPLY CURRENT (Amps)	BASIC SYSTEM CURRENT REQUIREMENTS (Amps)	
		Maximum	Typical
+ 5 ±5%	35.0	9.0	6.6
+12 ±5%	3.0	0.7	0.4
–10 ±5%	3.0	0.2	0.2
–12 ±5%	0.5	––	––

AC POWER REQUIREMENTS
50–60 Hz; 115/230 VAC; 150 Watts

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0 to 55°C

SOFTWARE SPECIFICATIONS

CAPABILITIES

System Monitor:

Devices supported include:

- ASR 33 teletype
- Intel high speed paper tape reader
- Paper tape punch
- CRT
- Printer
- Universal PROM programmer
- 4 logical devices recognized
- 16 physical devices maximum allowed

Macro Assembler:

800 symbols in standard system; automatically expandable with additional RAM memory to 6500 symbols maximum.

Assembles all seventy-eight 8080 machine instructions plus 10 pseudo-operators.

Text Editor:

12K bytes of workspace in standard system; automatically expandable with additional RAM memory to 58K bytes.

OPERATIONAL ENVIRONMENTAL

System Monitor:

Required hardware:

- Intellec MDS
- 331 bytes RAM memory
- 2K bytes ROM memory
- System console

Macro Assembler:

Required hardware:

- Intellec MDS
- 12K bytes RAM memory
- System console
- Reader device
- Punch device
- List device

Required software:

- System monitor

Text Editor:

Required hardware:

- Intellec MDS
- 8K bytes RAM memory
- System console
- Reader device
- Punch device

Required software:

- System monitor

Tape Format:

Hexadecimal object format.

MDS OPTIONS

MDS-016	16K Dynamic RAM
MDS-406	6K PROM (sockets and logic)
MDS-501	DMA Channel Controller
MDS-504	General Purpose I/O Module
MDS-600	Prototype Module
MDS-610	Extender Module
MDS-620	Rack Mounting Kit

MDS EMULATORS/SIMULATOR

MDS-ICE-30	3001 In-Circuit Emulator
MDS-ICE-80	8080 In-Circuit Emulator
MDS-SIM-100	Bipolar ROM Simulator

MDS PERIPHERALS

MDS-UPP	Universal PROM Programmer
MDS-PTR	High Speed Paper Tape Reader
MDS-DOS	Diskette Operating System

MDS INTERFACE CABLES/CONNECTORS

MDS-900	CRT Interface Cable
MDS-910	Line Printer Interface Cable
MDS-915	High Speed Reader Interface Cable
MDS-920	High Speed Punch Interface Cable
MDS-930	Peripheral Extension Cable
MDS-940	DMA Cable
MDS-950	General Purpose I/O Cable
MDS-960	25-pin Connector Pair
MDS-970	37-pin Connector Pair
MDS-980	60-pin Motherboard Auxiliary Connector
MDS-985	86-pin Motherboard Main Connector
MDS-990	100-pin Connector Hood

EQUIPMENT SUPPLIED

Central Processor Module
RAM Memory Module
Monitor Module (System I/O)
Front Panel Control Module
Chassis with Motherboard
Power Supplies
Finished Cabinet
Front Panel
ROM Resident System Monitor
RAM Resident Macro Assembler
RAM Resident Text Editor
Hardware Reference Manual
Reference Schematics
Operator's Manual
8080 Assembly Language Programming Manual
System Monitor Source Listing
8080 Assembly Language Reference Card
TTY Cable
European AC Adapter
AC Cord

MDS-DOS DISKETTE OPERATING SYSTEM
AND MDS-DRV ADDITIONAL DRIVE UNIT

Floppy diskette operating system providing high speed Input/Output and data storage for the Intellec® MDS.

Supports all existing standard Intellec® peripherals.

Data on flexible diskette addressed using IBM soft-sectored format which allows 1/4 million byte data capacity per diskette.

Up to 200 files per diskette.

Dynamic allocation and deallocation of diskette sectors for variable length files.

Device independence realized by assignment of unique file names to each peripheral device.

Supports optional Intellec MDS ICE-80 (In-circuit Emulator) for Intel® 8080 Microprocessor.

Diskette system macro assembler used to assemble all 8080 machine instructions with full macro and conditional assembly capabilities.

Diskette system text editor with string search, substitution, insertion, and deletion commands.

Listing produced by macro assembler can be directed to diskette allowing interrogation from high speed console device.

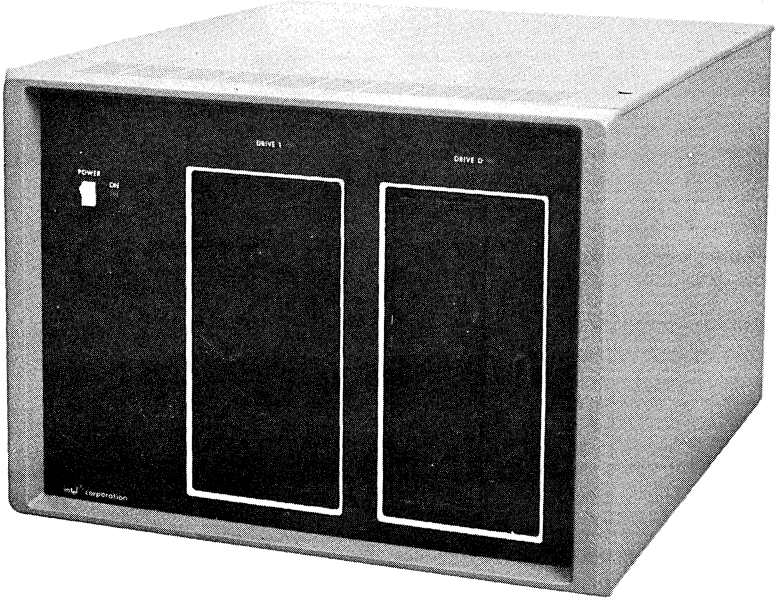
Diskette operating system software products loaded into Intellec MDS RAM in seconds.

Access to all Intellec MDS Monitor facilities.

Programs created, edited, assembled, executed and debugged without paper tape handling.

Diskette operating system functions callable from user programs.

The Intellec MDS Diskette Operating System is a general purpose, high speed data handler and file manipulation system for use with the Intellec MDS and its peripherals. The use of a single or dual drive Diskette Operating System significantly reduces program development time. The software system known as ISIS (Intel Systems Implementation Supervisor), provides the ability to edit, assemble, execute and debug programs, and performs all file management tasks for the user.

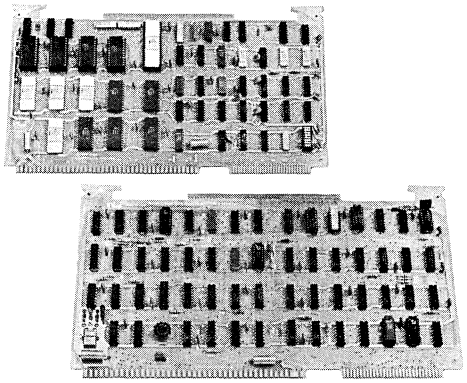


MDS-DOS Diskette Drive and Optional MDS-DRV

HARDWARE

The INTELLEC® MDS diskette system provides direct access bulk storage, intelligent controller, and up to two diskette drives. Each drive provides 1/4 million bytes of storage with a data transfer rate of 250,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the INTELLEC MDS bus, as well as supporting the two diskette drives. The MDS diskette system records all data in the IBM-compatible soft sector format.

The MDS diskette controller consists of two boards, the Channel Board and the Interface Board. These two printed circuit boards reside in the INTELLEC MDS chassis and constitute the diskette controller. Each of the systems components is shown in the photograph, and are described in more detail in the following paragraphs.



DOS Channel and Interface Controller Boards

CHANNEL BOARD

The *Channel Board* is the primary control module within the diskette system. The Channel Board receives, decodes, and responds to channel commands from the 8080 Central Processor Unit (CPU) in the INTELLEC MDS system. The Channel Board can access a block of INTELLEC MDS system memory to determine the particular diskette operations to be performed and fetch the parameters required for the successful completion of the specified operation.

The control functions of the Channel Board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 Central Processing Elements (2-bit slice per CPE), a 3001 Microprogram Control Unit, and 512 X 32 bits of 3604 programmable-read-only-memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the Channel Board.

INTERFACE BOARD

The *Interface Board* provides the diskette controller with a means of communication with the diskette drives, as well as with the INTELLEC MDS system bus. Under control of the microprogram being executed on the Channel Board, the Interface Board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), cause the head to move to the proper track and verify successful operation. The Interface Board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the Channel Board.

During write operations, the Interface Board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

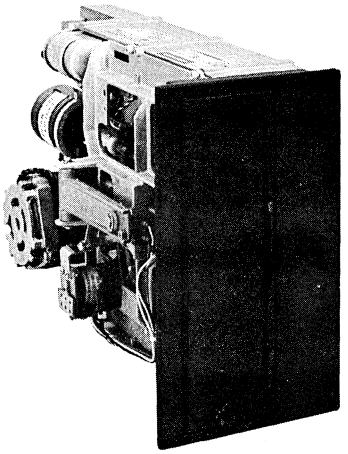
When the diskette controller requires access to INTELLEC MDS system memory, the Interface Board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The Interface Board also acknowledges I/O commands as required by the INTELLEC MDS bus.

The Diskette System is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

DISKETTE DRIVE MODULES

Each diskette drive consists of read/write and control electronics, drive mechanisms, read/write head, track positioning mechanism, and the removable floppy diskette platter. These components interact to perform the following functions:

- Interpret and generate control signals.
- Move read/write head to selected track.
- Read and write data.



Additional Drive Unit MDS-DRV

SOFTWARE – INTEL SYSTEM IMPLEMENTATION SUPERVISOR (ISIS)

The ISIS programs and subroutines reside on the system diskette and provide a broad range of user-oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS 8080 Macro Assembler can be loaded in seconds, from the diskette, and all passes executed without the need for user interaction. Object code and list files may be directed to any output device, or stored as diskette files. A special ISIS utility is provided which converts files from hexadecimal to absolute binary for high-speed retrieval and execution. Powerful system console commands are provided in an easy to use English context. Debugging is initiated by a special prefix to any system command or program call which causes Monitor mode to be entered directly from the program call along with its calling parameters.

A file is a user-defined collection of information of variable length. ISIS also treats each of the standard INTELLEC® MDS supported peripherals as files through preassignment of unique file names to each device. In this manner data can be copied from one device to another (i.e., tape reader to tape punch) using the same command required to copy one diskette data file to another. ISIS provides automatic implementation of random access disk files. Each file is identified by a user-chosen name unique on its diskette. Up to 200 files may be stored on each 1/4 million byte diskette.

SYSTEM COMMANDS

The user is provided with a wide range of system commands that offer powerful file and program manipulation features:

- The DIR command lists the names, sizes and attributes of files resident on the specified disk directory.
- The RENAME command allows users to change the identifying names of files.
- The COPY command allows users to create new copies of existing files or to transfer files from one device to another.
- The ATTRIB command allows the user to set or reset write-protection and other characteristics of a disk file.
- The DELETE command removes a file from a diskette, thereby freeing space for allocation for other files.
- The HEXBIN command coverts an Intel standard hexadecimal format file into absolute binary format for a reduction in load time and space.
- The FORMAT command formats a diskette on a second disk drive so that it may be used by ISIS.
- The DEBUG command loads the name program and parameters, and gives control to the INTELLEC MDS monitor for execution and/or debugging in the event of an error.
- Programs may be loaded and executed by typing the program name as a command. Users may therefore name their own programs with descriptive verbs and extend their command repertoire.

ISIS 8080 MACRO ASSEMBLER

The ISIS 8080 Macro Assembler translates symbolic 8080 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits the assembler to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

The ISIS Assembler accepts diskette file input and produces an object file with corresponding symbol table and assembly listing file with any errors. The list file may then be interrogated from the system console or copied to the appropriate list device. The object file may be kept on diskette in its hexadecimal format for loading under ISIS supported software packages such as the optional 8080 In-Circuit Emulator (ICE-80). For loading directly under control of ISIS, the object file may be converted from hexadecimal to absolute binary format using the HEXBIN command.

The ISIS 8080 Macro Assembler is written in PL/M™-80, Intel's high level systems programming language. It occupies 12K bytes of RAM memory allowing space for over 1000 symbols when used with ISIS in a 32K INTELLEC MDS system. The symbol table size may be expanded by adding additional RAM memory.

ISIS TEXT EDITOR

The ISIS Text Editor is a comprehensive tool for the entry and correction of assembly language programs for the Intel 8080 microcomputer. Its command set allows manipulation of either entire lines of text or individual characters within a line.

Programs may be entered from the console keyboard or may be loaded directly. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

To facilitate the use of these editing commands, utility commands are used to change positions in the workspace, These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

The contents of the workspace are stored on the diskette and can be immediately accessed by ISIS commands or other programs such as the ISIS 8080 Macro Assembler.

The ISIS Text Editor is written in PL/M™-80. It occupies 8K bytes of RAM memory allowing approximately 12K bytes of workspace in a 32K INTELLEC MDS system.

SOFTWARE SPECIFICATIONS

ISIS CAPABILITIES

ISIS commands (User entries at console input device)

File commands:

DIR	List diskette directory.
COPY	Make a copy of a file.
DELETE	Remove a file from diskette.
RENAME	Change the name of a diskette file.
ATTRIB	Change the attributes of a diskette file.

Diskette initialization:

FORMAT	Initialize a new diskette.

Program debug and conversion:

DEBUG	Execute a program in debug mode.
HEXBIN	Convert program from hexadecimal format to absolute binary.

Program execution:

file name	An executable program in a diskette file can be executed by entering the file name as a command.

ISIS System Calls (System services called by user programs)

Input/output operations:

OPEN	Initialize file for input/output operations
READ	Transfer data from file to memory
WRITE	Transfer data from memory to file
SEEK	Position diskette file pointer at any byte in the file
RESCAN	Position pointer to beginning of current line
CLOSE	Terminate input/output operations on file

Diskette directory maintenance

DELETE	Delete a file from the diskette directory
RENAME	Change diskette file name
ATTRIB	Change diskette file attributes

Console Reassignment and error message output

CONSOLE	Change console device
WHOCON	Determine currently assigned system console
ERROR	Output error message on system console

Program loading and execution

LOAD	Load a file of executable code and transfer control to loaded program
EXIT	Terminate program and return to ISIS control

ISIS 8080 Macro Assembler:

1000 symbols in 32K system; automatically expandable with additional RAM memory.

Assembles all seventy-eight 8080 machine instructions plus 10 pseudo-operators.

ISIS Text Editor:

12K bytes of workspace in 32K system; automatcially expandable with additional RAM memory.

ISIS OPERATIONAL ENVIRONMENTAL

ISIS:

Required hardware:
- Intellec MDS
- 32K bytes RAM memory
- System console
- MDS-DOS Diskette Operating System

Required software:
- System monitor

Macro Assembler:

Required hardware:
- Intellec MDS
- MDS-DOS Diskette Operating System
- 32K bytes RAM memory
- System console

Text Editor:

Required hardware:
- Intellec MDS
- MDS-DOS Diskette Operating System
- 32K bytes RAM memory
- System console

Required software:
- ISIS
- System monitor

Required software:
- ISIS
- System monitor

ICE-80 (Optional)

Required hardware:
- Intellec MDS
- MDS-80 ICE
- 32K bytes RAM memory
- MDS-DOS Diskette Operating System

Required software:
- ISIS
- System monitor

HARDWARE SPECIFICATIONS

MEDIA

Flexible Diskette
One Recording Surface
IBM Soft Sector Format
77 Tracks/Diskette
26 Sectors/Track
128 Bytes/Sector

PHYSICAL CHARACTERISTICS

(Chassis and Drives)

Mounting:	Table-Top or Standard 19" Retma Cabinet
Height:	12.08" (30.68 cm)
Width:	16.88" (42.88 cm)
Depth:	19.0" (48.26 cm)
Weight:	1 Drive 51 lb (23 kg)
	2 Drives 64 lb (29 kg)

ELECTRICAL CHARACTERISTICS

Chassis
DC Power Supplies

Voltage	Current
5V	3A ±5%
−5V	600 mA ±5%
24V	4A ±5%

AC Power Requirements
3-wire input with center conductor (earth ground) tied to chassis
Single-phase, 115/230 VAC; 50–60 Hz; 160 watts

INTELLEC® MDS-DOS Controller
DC Power Requirements
Channel Board: 5V @ 3.75A (typ), 5A (max)
Interface Board: 5V @ 1.5A (typ), 2.5A (max)

DISKETTE DRIVE PERFORMANCE SPECIFICATION

Capacity (Unformatted):
Per Disk . . . . . 3.1 megabits
Per Track . . . . . 41 kilobits
Capacity (Formatted):
Per Disk . . . . . 2.05 M Bits
Per Track . . . . . 26.6 K Bits
Data Transfer Rate . . . . . 250 Kilobits/sec.
Access Time:
Track-to-Track . . . . . .10 ms
Head Settling Time . . . . . .10 ms
Average Random Positioning Time . . . . . .260 ms
Rotational Speed . . . . . .360 rpm
Average Latency . . . . . .83 ms
Recording Mode . . . . . Frequency Modulation

ENVIRONMENTAL CHARACTERISTICS

MEDIA

Temperature:	
Operating	15.6°C to 51.7°C
Non-Operating:	5°C to 55%
Humidity:	
Operating:	8 to 80% (Wet bulb 29.4°C)
Non-Operating:	8 to 90%

DRIVES AND CHASSIS

Temperature:	
Operating:	10°C to 38°C
Non-Operating:	−35°C to 65°C
Humidity:	
Operating:	20% to 80% (Wet bulb 26.7°C)
Non-Operating:	5% to 95%

MDS-DOS CONTROLLER BOARDS

Temperature:	
Operating:	0 to 70°C
Non-Operating:	−55°C to 85°C
Humidity:	
Operating:	Up to 90% relative humidity without condensation.
Non-Operating:	All conditions without condensation of water or frost.

EQUIPMENT SUPPLIED

Cabinet, Power Supplies, Line Cord, Single Drive
FDC Channel Board
FDC Interface Board
Dual Auxiliary Board Connector
Floppy Disk Controller Cable
Floppy Disk Peripheral Cable
Hardware Reference Manual
Reference Schematics
ISIS System Diskette
ISIS Operators Manual
ISIS/MDS Monitor Bootstrap PROM

OPTIONAL EQUIPMENT

Rack Mount Kit
MDS-DRV Additional Drive Unit
Blank Diskettes
ISIS System Diskettes

MDS-UPP UNIVERSAL PROM PROGRAMMER

Intellec® MDS peripheral capable of programming the following Intel PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704, 8708.

Personality cards used for specific Intel PROM programming requirements.

Zero insertion force sockets for both 16-pin and 24-pin PROMs.

Flexible power source for system logic and programming pulse generation.

PROM programming verification facility.

Stand alone or rack mountable.

The Universal PROM Programmer is an Intellec MDS peripheral capable of programming and verifying the following Intel PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704, and 8708. Programming and verification operations are initiated from the Intellec MDS system console and are controlled by programs resident in the Intellec MDS and Universal PROM Programmer.

SPECIFICATIONS

INTERFACE
Data: Two 8-bit unidirectional buses
Commands: 3 Write Commands
2 Read Commands
Initiate Command

AVERAGE PROGRAMMING TIME
1702A/8702A: 40 seconds
2708/8708: 5 minutes
3601: 2 seconds
3604: 10 seconds
3624: 10 seconds
2704/8704: 2.5 minutes

PHYSICAL CHARACTERISTICS
Dimensions: 6" X 7" X 17"
14.7 cm X 17.2 cm X 41.7 cm
Weight: 18 lb (8.2 kg)

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0° to 70°C.

OPTIONS
Personality Cards:
MDS-UPP-361:3601 Personality Card
MDS-UPP-864:8604/3604/3624 Personality Card
MDS-UPP-872:8702A/1702A Personality Card
MDS-UPP-878:8708/8704/2708/2704 Personality Card

PROM Programming Sockets:
MDS-UPP-501: 16-pin/24-pin pair
MDS-UPP-502: 24-pin/24-pin pair

EQUIPMENT SUPPLIED
Cabinet
Power Supplies
4040 Intelligent Controller Module
Specified Zero Insertion Force Socket Pair
Intellec MDS Interface Cable
Hardware Reference Manual
Reference Schematics

MDS-PTR HIGH SPEED PAPER TAPE READER

Intellec® MDS high speed paper tape reader peripheral

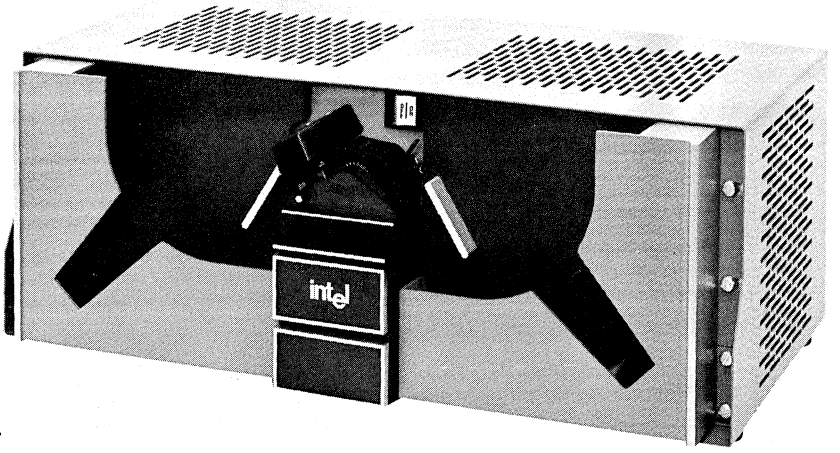
20 times faster than standard ASR-33 Teletype reader

Loads 16K Intellec MDS program memory in less than three minutes.

Data transfer at asynchronous rates in excess of 200 characters per second

Rack mountable or stand-alone

The MDS-PTR high speed paper tape reader is an Intellec MDS peripheral that reads paper tape over twenty times faster than the standard ASR-33 Teletype reader. This translates into a significantly faster development cycle due to a marked reduction in the time required for repetitive program loading, assembly, and editing operations.



SPECIFICATIONS

TAPE MOVEMENT

Tape Reader Speed:
0 to 200 characters per second asynchronous

Tape Stopping:
Stops "On Character"

TAPE CHARACTERISTICS

Tape must be prepared to ANSI X 3.18 or EMCA 10 Standards for base materials and perforations.

Reads tape of any material with thickness between 0.0027" and 0.0045" with transmissivity less than or equal to 57% (oiled buff paper tape).

Tape loading: in line

Tape width: 1 inch

PHYSICAL CHARACTERISTICS

Height: 7.75 in. (19.69 cm)
Width: 19.25 in. (48.90 cm)
Depth: 11.62 in. (29.52 cm)
Weight: 13 lb (5.9 kg)

ELECTRICAL CHARACTERISTICS

AC Power Requirements:
3-wire input with center conductor (earth ground) tied to chassis. 100, 115, or 127 VAC, single phase at 3.0 amps or 220 or 240 VAC and 1.5 amps; 47 to 63 Hz.

ENVIRONMENTAL CHARACTERISTICS

Temperature:
Operating: 0 to 55°C (free air)
Non-operating: −55°C to +85°C

Humidity:
Operating: Up to 90% relative humidity without condensation.
Storage: All conditions without condensation of water or frost.

EQUIPMENT SUPPLIED

Paper Tape Reader
Reader Cable
Fanfold Tape Guide
Fanfold Paper Tape
Hardware Manual
Installation and Operations Guide
Fanfold Guide Installation Instructions

MDS-ICE-80 8080 IN-CIRCUIT EMULATOR

Extends powerful Intellec® MDS diagnostic capabilities into user configured system allowing real time (2 MHz) emulation of the user system 8080.

User configured system can share Intellec MDS RAM, ROM, and PROM memory.

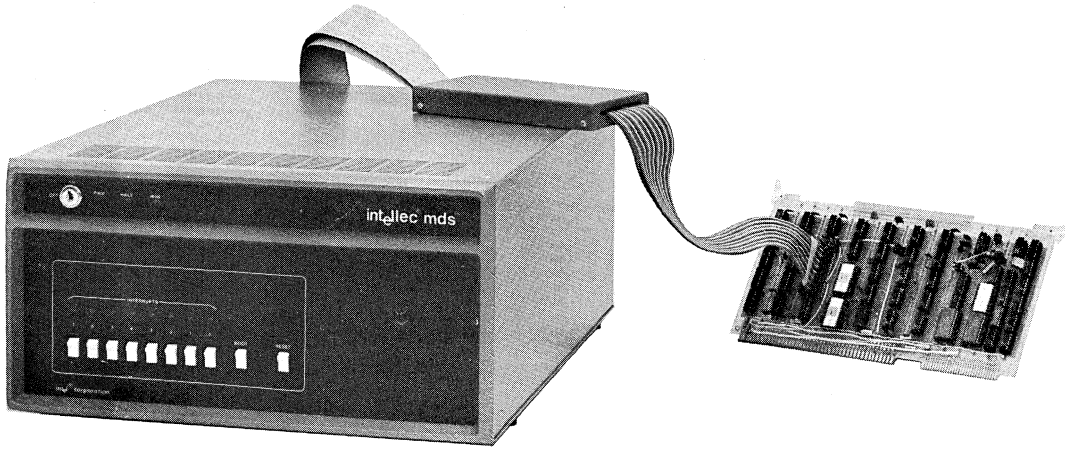
I/O translation allows user configured systems to share Intellec MDS input/output facilities.

Capability to display previously executed instructions with corresponding address, data, and 8080 status information.

Capability to examine and alter CPU registers and main memory.

Direct Intellec MDS connection to user configured system via an external cable and 40-pin plug.

ICE-80 is an Intellec MDS resident module that interfaces to any user configured 8080 system and allows the designer to emulate the user 8080 in real time, single step the user system's 8080, substitute Intellec MDS memory and I/O for user system equivalents, and extend powerful debug functions into the user system.



SPECIFICATIONS

WORD SIZE
Instruction: 8, 16 or 24 bits
Data: 8 bits

CENTRAL PROCESSOR
8080 CPU, 2 μS cycle time, 8-bit accumulator, six 8-bit registers, subroutine nesting to any level, multiple level interrupt capability.

INSTRUCTION SET
78 instructions including conditional branching, binary arithmetic, logical operations, register-to-register transfers, and I/O.

CONNECTORS
Edge Connector: CDC VPB01E43A00A1

PHYSICAL CHARACTERISTICS
Width: 12.00 in.
Height: 6.75 in.
Depth: 0.50 in.

ELECTRICAL CHARACTERISTICS
DC Power:
V_{CC} = +5 ±5%
I_{CC} = 9.81A max.; 6.90A typ.
V_{DD} = +12 ±5%
I_{DD} = 79 ma max.; 45 ma typ.
V_{BB} = −9V ±5%
I_{BB} = 1 ma max.; 1 μa typ.

DEVELOPMENT SYSTEMS

SPECIFICATIONS

MEMORY ADDRESSING
Intellec MDS RAM, ROM and PROM may be combined with user system ROM, PROM, and RAM combinations in 4K segments up to a maximum of 65, 536 bytes.

I/O ADDRESSING
Intellec MDS I/O ports may be combined with user system I/O ports in 16 port groups, up to a maximum of 256 8-bit input and 256 8-bit output ports.

USER SYSTEM INTERFACE
Cable carrying all 8080 address, data, and control signals terminated in a 40-pin plug.

SYSTEM CLOCK
Crystal controlled 2 MHz ±0.01%.
Removable by jumper selection when replaced by user clock.

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0 to 70°C

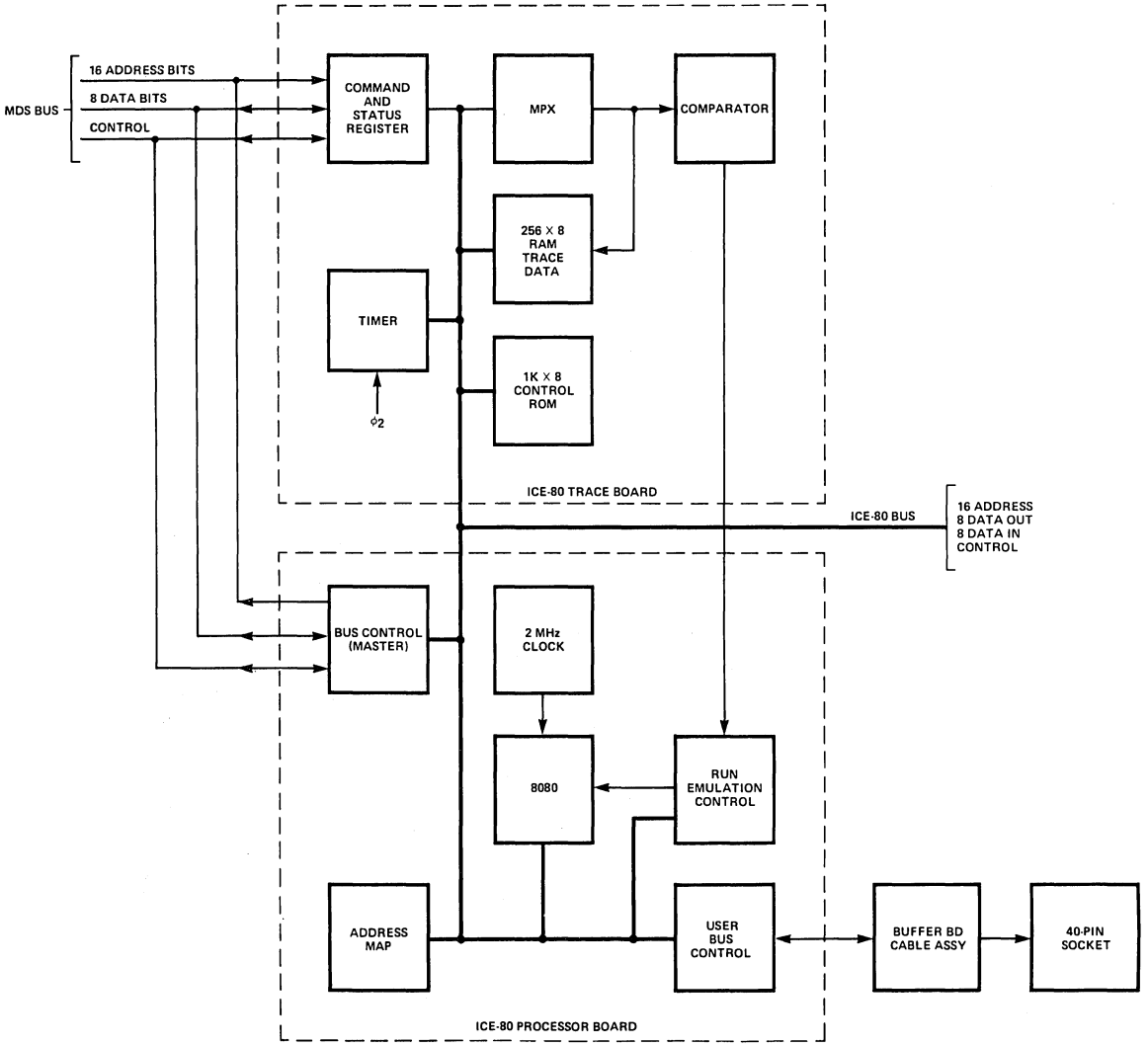
EQUIPMENT SUPPLIED
Printed Circuit Modules (2)
Interface Cables and Buffer Board
Reference Manual
Schematic Diagram

ICE-80 allows the user to assign Intellec® MDS resident memory and I/O to the user system. Once assigned, the MDS memory or I/O becomes a part of the user system. The user system may operate with all MDS resident memory and I/O, all user provided memory and I/O, or a combination of both.

ICE-80 debug features include the setting of breakpoints in two hardware comparitors which can trap on any memory read, memory write, I/O read or I/O write operation. Breakpoint extensions, which can be logically ANDED with basic breakpoint parameters, include stack operation, M1 fetch state, or a user defined logic signal. When a breakpoint is encountered in the emulation mode, ICE-80 automatically reverts to the interrogation mode. At this time the memory address, data bus contents, and 8080 status byte from the last 44 machine cycles can be displayed along with the actual number of clock cycles which elapsed since program initiation. In the single-step mode, the user may select single-step or multiple single-step operation. In single-step operation a single instruction is executed, and upon completion, all relevant system status may be displayed. In multiple single-step mode, status information is stored at the end of each machine cycle and the next instruction is executed. When multiple single-step operation is terminated upon a software breakpoint or user command, historical information may be retrieved for display or off line analysis.

The heart of ICE-80 is a microcomputer system utilizing Intel's 8080 microprocessor as its nucleus. This system communicates with the Intellec MDS host processor via I/O commands. Host processor commands and ICE-80 status are interchanged through registers on the ICE module. ICE-80 and the MDS also communicate through a control block resident in Intellec MDS main memory which contains detailed configuration and status information.

The ICE-80 microcomputer system consists of an Intel 8080 CPU, control memory and data storage memory. The system may be driven with either an internal 2 MHz clock or a user supplied clock. The basic ICE-80 system is augmented by several peripheral devices. An 8-bit command register receives Intellec MDS commands and an 8-bit status register provides ICE-80 systems status information to the Intellec MDS. Bus control logic allows the ICE-80 processor to assume control of the Intellec MDS bus as a bus master, when required. A comparitor contains two 24-bit hardware breakpoint registers which provide address and control information associated with breakpoint functions. Finally, buffer/driver circuitry, located in circuit board in the ICE-80 cable, insures that data transmission between the ICE-80 and user system meets the capacitive loading and input current requirements for the 8080.



ICE-80 BLOCK DIAGRAM

MDS-ICE-30 3000 SERIES IN-CIRCUIT EMULATOR

Extends the Intellec® MDS diagnostic capabilities into user configured systems allowing in-circuit emulation of the user system's 3001 MCU

Direct Intellec MDS connection to the user configured system is achieved via an external cable with 3001 compatible 40-pin connector

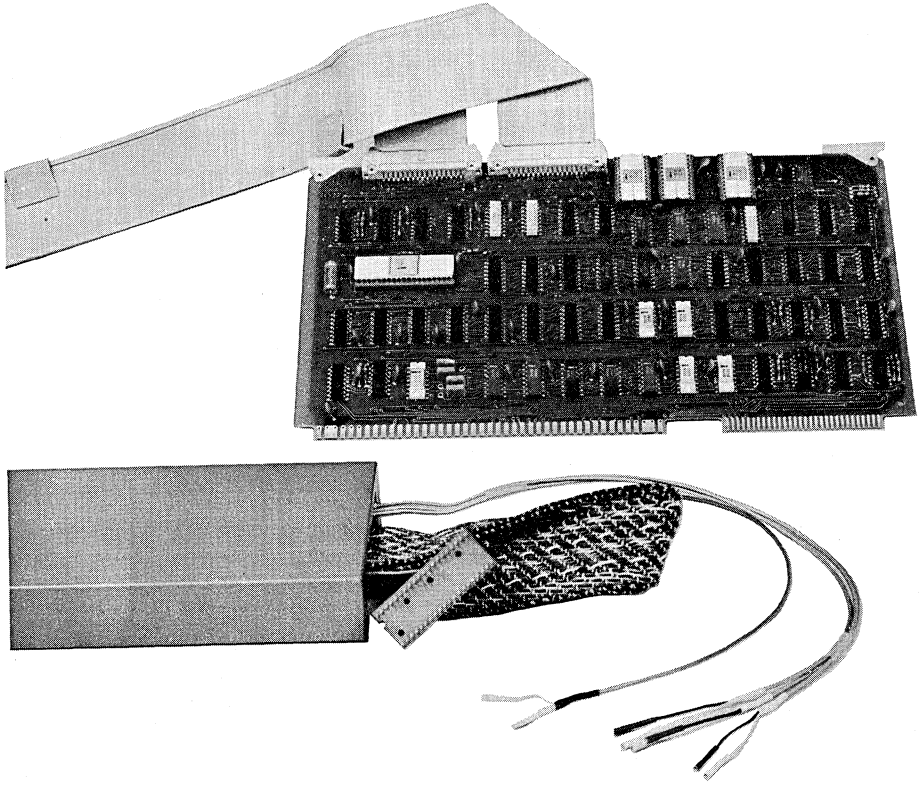
Provides for the display of all 3001 address, status, and control lines for the current micro-instruction executed

Allows for single step microprogram execution

Presets the 9-bit 3001 Microprogram Address Register and set two independent breakpoints on micro-instruction addresses generated by 3001

Allows two independent breakpoints to be set on the logical combination of any three TTL compatible signals in the user system via three logic probes

ICE-30 is an Intellec® MDS resident module that provides the user with direct in-circuit emulation of the 3001 Microprogram Control Unit (MCU) and complete control over the execution of user developed microprograms. Through in-circuit emulation, the designer is able to set micro-program address breakpoints, single step micro-program execution and monitor all of the address, status, and control lines of the 3001.



ICE-30 Module Board with External Cable and 40 Pin Connector

A.C. CHARACTERISTICS $T_A = 0°C$ to $55°C$, $V_{CC} = 5.0V \pm 5\%$

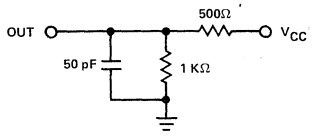
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY} (2)	Cycle Time	185	120		ns
t_{WP}	Clock Pulse Width	35	20		ns
t_{CS}	Clock Pulse Separation	150			
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC_0–AC_6	13			ns
t_{SK}	FC_0, FC_1	13			ns
t_{SX}	SX_0–SX_3, PX_4–PX_7	13			ns
t_{SI}	FI	13			ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC_0–AC_6	15			ns
t_{HK}	FC_0, FC_1	15			ns
t_{HX}	SX_0–SX_3, PX_4–PX_7	15			ns
t_{HI}	FI	15			ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA_0–MA_8, FO)		90	137	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		78	130	ns
t_{FO}	Propagation Delay from Control Inputs AC_0–AC_6 to Latch Outputs (PR_0–PR_2)		98	150	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA_0–MA_8, FO, PR_0–PR_2)			50	ns
t_{FI}	Propagation Delay from Control Inputs AC_0–$AC_6$to Interrupt Strobe Enable Output (ISE)		86	140	ns
t_{MH}	Propagation Delay from Clock Input (CLK) to Breakpoint Match $\overline{MATCH}$			158	ns

NOTES:
(1) Typical values are for $T_A = 25°C$ and nominal supply voltage.
(2) $t_{CY} = t_{CO} + t_{SF} + t_{WP}$

TEST CONDITIONS:

Input rise and fall times of 10 ns between 0.8 volt and 2.4 volts.
Output load of 10 mA and 50 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT



CAPACITANCE $T_A = 25°C$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:			50	pF
C_{OUT}	Output Capacitance			50	pF

D.C. AND OPERATING CHARACTERISTICS $T_A = 0°$ to $55°C$, $V_{CC} = 5.0V \pm 5\%$

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 55°C

Storage Temperature. . . . . −20°C to +75°C

All Output and Supply Voltages . . . . . −0.5V to +7V

All Input Voltages . . . . . −1.0V to +5.5V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		−0.8	−1.5	V	$I_C = -12mA$
I_F	Input Load Current: CLK Input Logic Probe inputs All other inputs			 −2.0 −3.0 −0.4	 mA mA mA	$V_F = 0.45V$
V_{IL}	Input Low Voltage			0.8	V	$V_{CC} = 5.0V$
V_{IH}	Input High Voltage	2.0			V	$V_{CC} = 5.0V$
I_{CC}	Power Supply Current			0.0	mA	
V_{OL}	Output Low Voltage PR_0–PR_2 All other outputs		 0.35 0.35	 0.45 0.45	 V V	 $I_{OL} = 16mA$ $I_{OL} = 40mA$
V_{OH}	Output High Voltage MA_0–MA_8, ISE, FO	2.4	3.0		V	$I_{OH} = -2mA$
I_{OS}	Output Short Circuit Current MA_0–MA_8, ISE, FO	−40		−120	mA	$V_{CC} = 5.0V$(2)
$I_{O(OFF)}$	Off-State Output Current MA_0–MA_8, FO MA_0–MA_8, FO, PR_0–PR_2			 −100 100	 μA μA	 $V_0 = 0.45V$ $V_0 = 5.25V$

NOTES:
(1) Typical values are for $T_A = 25°C$ and nominal supply voltage.
(2) Not more than one output should be shorted at one time.

SIM-101/SIM-102/SIM-104 ROM SIMULATORS

Extends the powerful Intellec® MDS diagnostic capabilities into user-configured systems, allowing simulation of the user system's bipolar ROM/PROM memory

Direct Intellec MDS connection to the user-configured system via external cables and Intel's ROM/PROM compatible dual-in-line connectors

Simulates Intel's standard bipolar ROMs and PROMs

Modular design allows the user to configure simulation modules to particular memory space requirements

Directly load the ROM Simulator modules from the output of the Intel® Cross Microassembler, CROMIS

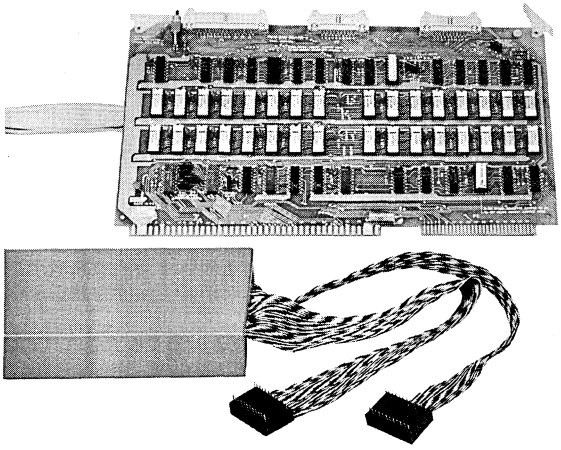
Access the configured memory space from the console keyboard using simulated ROM addresses

Examine an entire word regardless of length; i.e., 8 bits, 10 bits, 32 bits etc.

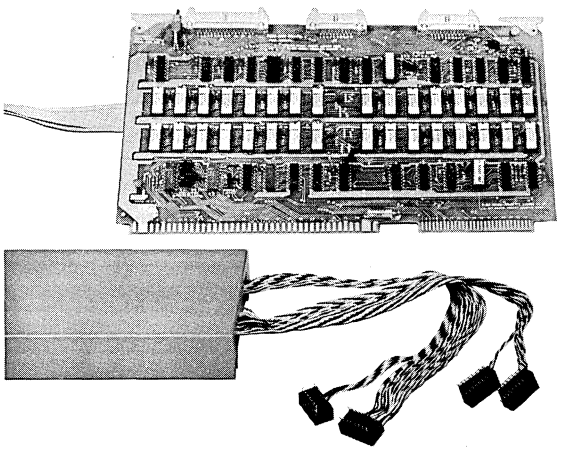
Modify an entire word in a single operation regardless of length

Read access time is 130 ns, maximum

Each ROM-SIM module consists of a high-speed, 130-nanosecond 8K bit RAM board, buffer assembly, external cables, and an interactive software program. The ROM-SIM software is a PL/M™-80 program that operates in the Intellec MDS to provide the user interface for the ROM-SIM hardware. The software loads BNPF or hexadecimal files such as those generated by the Cross Microassembler System, CROMIS. The ROM-SIM software has the capability to compare and verify microcode, load, display and modify simulated control store contents, and output new BNPF or hexadecimal files from the simulated ROM memory for ROM/PROM programming.



SIM-101, 102



SIM-104

SPECIFICATIONS

DC CHARACTERISTICS

T_A = 0°C to 55°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	LIMITS			TEST CONDITION
		MIN	MAX	UNIT	
I_I	Input Load Current Low Order Addr A0-A8 High Order Addr A9-AB Chip Selects		 −1.6 −2.1 −0.75	 mA	 V_{CC} = 5.25V V_{IN} = 0.45V
V_{OL}	Output Low Voltage		0.45	V	V_{CC} = 4.75V, I_{OL} = 16 mA
I_{CC}	User Power Supply Sensing		6	mA	User V_{CC} = 5.25V
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0		V	V_{CC} = 5.0V
V_{OH}	Output High Voltage		2.4	V	V_{CC} = 4.75V
I_{SC}	Output Short Circuit Current at Single Output	−40	−100	mA	V_O = 0V, V_{CC} = 5V
I_{CEX}	Output Leakage Current		±50 250	μA μA	For High Impedance State For Open Collector V_{CC} = 5.25V

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to 55°C
Storage Temperature ..... −20°C to 75°C
All Outputs or Supply ..... −0.5V to 7.0V
All Inputs ..... −1.0V to 5.5V

CAPACITANCE LOAD

C_{IN}	Low Order Address, Chip Selects High Order Address (Coaxial)	45 pF max. 50 pF max.
C_{OUT}	Data Outputs	50 pF max.

INTELLEC® 8/MOD 8
MICROCOMPUTER DEVELOPMENT SYSTEM

Complete Hardware/Software Development System for the design and implementation of 8008 CPU based microcomputer systems

Front panel designer's console provides complete system control and monitoring functions

8K bytes of random access memory (RAM) expandable to 16K bytes

2K bytes of erasable and field programmable read only memory (PROM) expandable to 16K bytes

Self contained PROM programming facility with zero insertion force PROM socket

Four 8-bit input and four 8-bit output ports

Integral asynchronous serial data communications capability at 110, 1200, or 2400 baud

Discrete teletype interface (20mA) current loop)

Standard system software includes a PROM resident system monitor, RAM resident Macro-Assembler and RAM resident text editor

Expansion capability provided for up to 16 standard or custom designed microcomputer modules

The Intellec® 8/MOD 8 (imm 8-80A) is a complete, self-contained microcomputer development system designed specifically to support the development and implementation of 8008 CPU based microcomputer systems. Its modular design facilitates the development of both large and small MCS-8 system.

The basic Intellec 8/MOD 8 consists of seven standard microcomputer modules (CPU, RAM, PROM, I/O, PROM Programmer, Front Panel Control) and power supplies enclosed in a finished table top cabinet. The heart of the system is the imm 8-82 central processor module built around Intel's 8008 p-channel 8-bit CPU on a single chip.

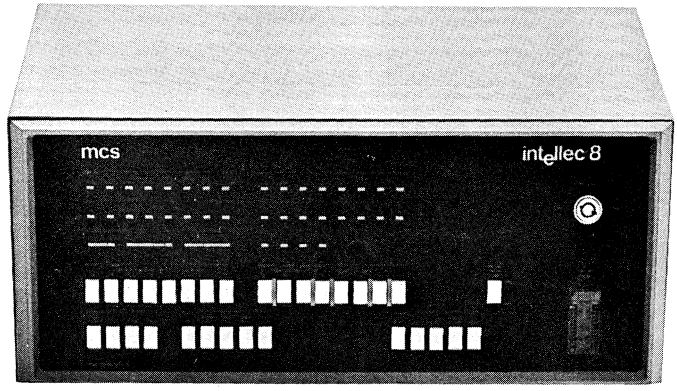
The Intellec Development System directly supports up to 16K of memory, eight input ports, twenty-four output ports, and provides expansion capability for custom designed micrcomputer modules within the system chassis.

The front panel designer's console provides an easy means of monitoring and controlling system operation, manually moving data to and from memory and input/output devices, setting hardware breakpoints, and executing or debugging programs.

The Intellec 8/MOD 8 has 10K bytes of memory in its basic configuration which can be expanded to 16K bytes within the system chassis. Of the basic 10K bytes of memory, 8K bytes are random access read/write memory located on two imm 6-28 RAM memory modules. This memory can be used for both data and program storage. The remaining 2K bytes of memory are located on the imm 6-26 PROM memory module and contain the Intellec 8/MOD 8 system monitor in eight Intel® 1702A erasable and field programmable read only memory chips. Eight additional sockets (2K bytes) are available on the imm 6-26 for expansion.

The PROM and RAM memory modules may be used in any combination to make up the 16K of directly addressable memory housed in the system chassis. Facilities are built into these modules so that combinations of RAM, ROM or PROM may be mixed in 256 byte increments.

The self-contained PROM programming module allows Intel 1602A or 1702A PROMs to be programmed and verified directly from RAM or PROM memory.



INTELLEC® 8
HIGH SPEED PAPER TAPE READER

Directly compatible with all Intellec® 8 Microcomputer Development Systems

20 times faster than standard ASR-33 teletype reader

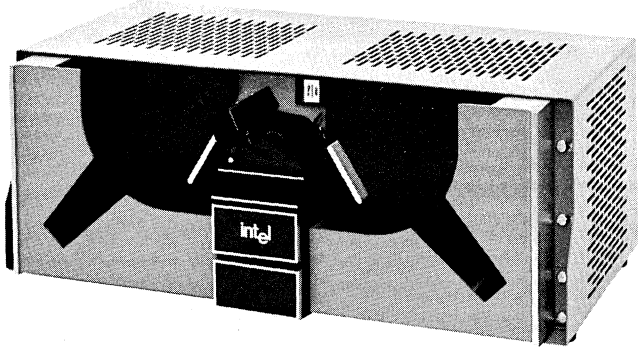
Loads any 8K Intellec® 8 program memory in less than 90 seconds

Data transfer at asynchronous rates in excess of 200 characters per second

Rack mountable or stand-alone

The imm8-90 high speed paper tape reader provides all Intellec 8 Microcomputer Development Systems with a high speed paper tape input that is over twenty times faster than the standard ASR-33 teletype reader. This translates into a significantly faster development cycle due to a marked reduction in the time required for repetitive program loading, assembly, and editing operations.

The Intellec 8 monitor software provides two key capabilities which significantly enhance the systems performance of the imm8-90. A general purpose paper tape reader driver is included in the Intellec 8 Monitor. It enables all systems software to utilize the high speed reader features and is caliable by user written application programs. The monitor also provides dynamic I/O reconfiguration permitting instantaneous reassignment of physical devices to logical devices.



SPECIFICATIONS

TAPE MOVEMENT:

Tape Reading Speed
0 to 200 characters per second asynchronous

Tape Stopping
Stops "On Character"

TAPE CHARACTERISTICS:

Tapes must be prepared to ANSI X 3.18 or EMCA 10 Standards for base materials and perforations.

Reads tape of any material with thickness between 0.0027" and 0.0045" with transmissivity less than or equal to 5% (oiled buff paper tape).

Tape loading: in line

Tape width: 1 inch

ELECTRICAL CHARACTERISTICS:

AC Power Requirement
3 wire input with center conductor (earth ground) tied to chassis. 100, 115, or 127 VAC, single phase at 3.0 amps or 220 or 240 VAC and 1.5 amps; 47 to 63 Hz.

EQUIPMENT SUPPLIED

Paper Tape Reader
Reader Cable
Reader Flat Cable
Fanfold Tape Guide
Fanfold Paper Tape
Hardware Manual
Installation and Operations Guide
Fanfold Guide Installation Instructions

BAREBONES 80
MICROCOMPUTER SUBSYSTEM

Complete 8080 CPU based microcomputer subsystem composed of Intel microcomputer modules housed in a card cage and interconnected by a printed circuit motherboard containing module sockets

78 instructions including data transfer; decimal, binary, and double precision arithmetic; logical, branch, stack, and I/O

Vectored interrupt capability

DMA capability

4K 8-bit bytes of RAM expandable to 16K bytes in standard system and 64K bytes in user modified system

Sockets for 4K 8-bit bytes of PROM expandable to 16K bytes in standard system and 64K bytes in user modified system

Four 8-bit input ports expandable to 16 input ports; four 8-bit output ports expandable to 28 output ports. Expansion to 256 input and 256 output ports in user modified system. All ports are TTL compatible

Integral asynchronous serial data communications capability at 110, 1200, or 2400 baud

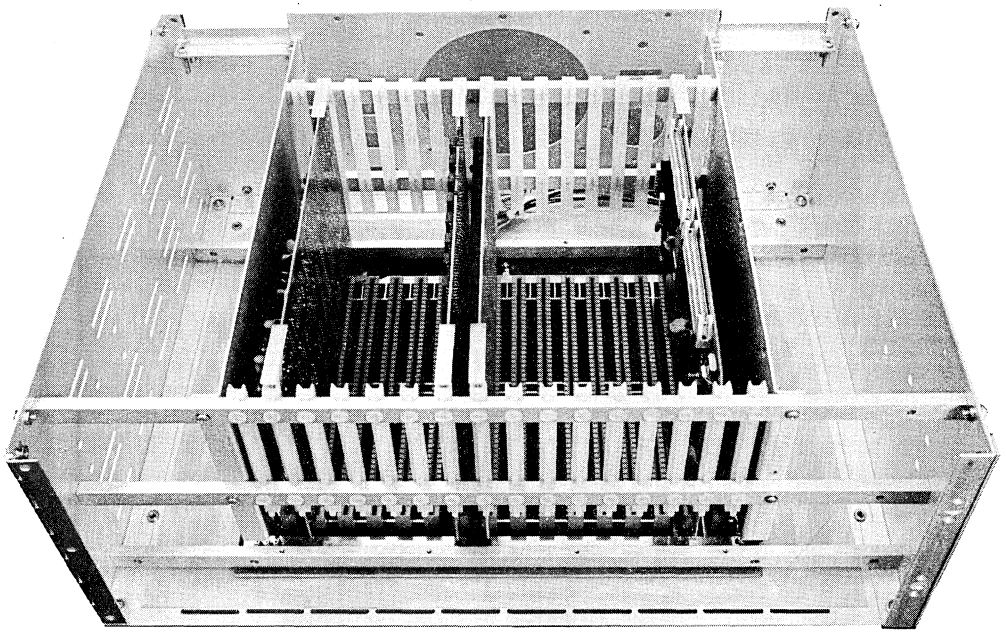
Discrete teletype interface (20 mA current loop)

Expansion capability provided for additional 12 Intel or custom microcomputer modules

Rack mountable.

The Barebones 80 (imm8-85) is a complete microcomputer system intended for OEM applications. The subsystem is composed of Intel microcomputer modules which are housed in a card cage and interconnected by a printed circuit motherboard. The chassis has space allocated for OEM power supplies, fan, and front panel.

Four modules are supplied with the basic system and expansion capability exists for 12 additional Intel-supplied or custom modules. Control signals, data and address lines are present at the 12 expansion connectors.



BAREBONES 80

SPECIFICATIONS

WORD SIZE
Data: 8 bits
Instruction: 8, 16, or 24 bits

MEMORY SIZE
6K bytes expandable to 16K bytes with standard modules, 64K bytes using custom memory modules.

INSTRUCTION SET
78, including conditional branching, binary arithmetic, logical, register-to-register, input/output, and memory reference.

MACHINE CYCLE TIME
2.5 μs. (Reduction to 2.0 μs possible by using faster memory and appropriate bus control signals.)

SYSTEM CLOCK
Crystal controlled at 2 MHz ±0.01%.

I/O CHANNELS
Maximum Input/Output configuration available with I/O or Output Modules

	Input Ports	Output Ports
imm8-61	16	16
imm8-63 (with one imm8-61)	4	28

INTERRUPT
User-designed multiple level interrupt capability.

DIRECT MEMORY ACCESS
User-designed DMA capability.

MEMORY ACCESS TIME
RAM: 1 μs with standard RAM module. Faster access time available with user-designed memory systems.
PROM: 1.3 μs with 8702A PROMs. Faster access time available with higher speed PROMs.

PHYSICAL CHARACTERISTICS
6¾" X 17" X 12" (suitable for mounting in standard RETMA 7" X 19" panel space).
Weight: 11 lb (4.9 kg).

ELECTRICAL CHARACTERISTICS
DC Power Requirement:
V_{CC} = 5V ±5%,
I_{CC} = 6A max., 3.5A typ.
V_{DD} = -9V ±5%,
I_{DD} = 1.2A max., 0.8A typ.
V_{CC} = +12V ±5%,
I_{GG} = 0.06A max., 0.04A typ.

*Requirement based on basic Barebones 80 system.

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0°C to 70°C

OPTIONAL MODULES
Available for Barebones 80:
- imm8-61 I/O Module
- imm8-63 Output Module
- imm6-28 RAM Memory Module
- imm6-70 Universal Prototype Module
- imm6-72 Module Extender

EQUIPMENT SUPPLIED
Central Processor Module
Input/Output Module
PROM Memory Module
RAM Memory Module
Chassis with Mother Board
PROM Resident System Monitor
Complete Hardware and Software Documentation including schematics and assembly drawings
Rack Slides

INTELLEC® 4/MOD 40
MICROCOMPUTER DEVELOPMENT SYSTEM

Complete Hardware/Software Development System for the design and implementation of 4040 and 4004 CPU based microcomputer systems

TTY interface, front panel designer's console, and high speed paper tape reader interface, in conjunction with PROM resident system monitor provide complete program loading, punching, monitoring, interrogation, and alteration capabilities

Program RAM (4K 8-bit bytes) provides a program development medium which lends itself to rapid and facile program monitoring and alteration

Data RAM (320 4-bit bytes expandable to 2560 bytes) provides data storage capacity

Program PROM (expandable to 4K 8-bit bytes) in conjunction with the resident PROM programmer provide capability of simulating final ROM resident program

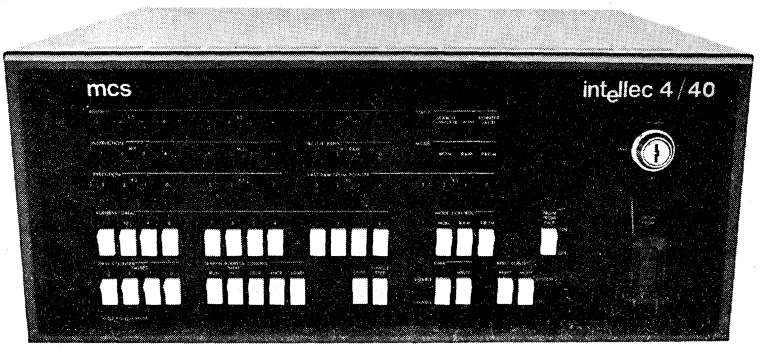
PROM resident system monitor, RAM resident assembler with edit feature included in standard systems software

Includes such standard program development features as program single step, address search (and pass count), next instruction indication, program flow verification

I/O expandable to 16 4-bit input ports and 48 4-bit output ports (all TTL compatible) allowing "hands-on" simulation of entire user system (processor and peripheral devices)

RESET, STOP, INTERRUPT control signals available to user via back panel

Modular design with expansion capability provided for up to eleven optional or user designed modules



The Intellec® 4/MOD 40 (imm 4-44A) is a complete, self-contained microcomputer development system designed specifically to support the development and implementation of 4040 and 4004 CPU based mirocomputer systems. Its modular design provides the flexibility to adapt to any size user system and the resident software facilitates program development.

The basic Intellec 4/MOD 40 Microcomputer Development System consists of 4 microcomputer modules (CPU, RAM, MEMORY CONTROL, and PROM PROGRAMMER), power supplies, I/O connectors, console, and displays. The heart of the system is the imm 4-43 central processor module built around Intel's high performance 4-bit 4040 CPU. The imm 4-43 is a complete microcomputer system containing the system clock, 1K 8-bit bytes of PROM memory, 320 4-bit bytes of data RAM memory, 3 4-bit input ports and 8 4-bit output ports. The imm 6-28 program RAM memory module contains a 4K x 8 memory array composed of Intel 2102 static random access memory elements. The imm 4-72 control module contains the circuitry required to interface the central processor module to the program RAM module. The imm 6-76 PROM programmer module provides the capability of programming Intel 1702A PROMs in conjunction with the front panel PROM socket and system monitor. All I/O ports are TTL compatible and accessible from the back panel 37-pin connectors. The front panel designer's console provides a means of monitoring and controlling system operation.

The Intellec modular design allows great design system flexibility. Program PROM can be expanded to 4K 8-bit bytes using imm 6-26 or imm 4-22 optional modules. Data RAM can be expanded to 2560 4-bit bytes using imm 4-24 modules. I/O capability can be expanded to 16 4-bit input and 48 4-bit output ports using optional imm 4-60 and 4-24 modules. The universal prototype card (imm 6-70) in conjunction with the eleven optional card sockets (which contain all essential system signals) provide the capability for interfacing custom designed modules.

The user RESET IN/OUT, STOP/STOP ACKNOWLEDGE, and INTERRUPT/INTERRUPT ACKNOWLEDGE control signals are all available at the back panel. Hence, the user can interrupt, halt, and reset the resident CPU via his own interface.

INTELLEC®4
HIGH SPEED PAPER TAPE READER

Directly compatible with all Intellec® 4 Microcomputer Development Systems

20 times faster than standard ASR-33 teletype reader

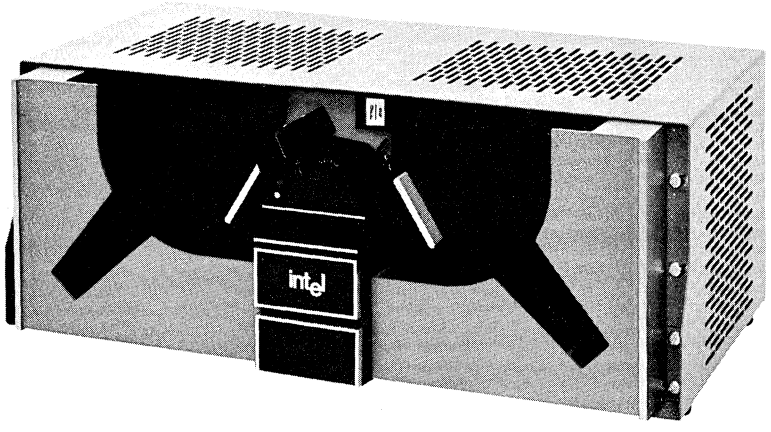
Data transfer at asynchronous rates in excess of 200 characters per second

Rack mountable or stand-alone

The imm4-90 high speed paper tape reader provides all Intellec® 4 Microcomputer Development Systems with a high speed paper tape input that is twenty times faster than the standard ASR-33 teletype reader. This translates into a significantly faster development cycle due to a marked reduction in the time required for repetitive program loading, assembly, and editing operations.

The Intellec 4 monitor provides the capability of assigning the imm4-90 as an input device and contains the reader driver software. Tapes may be read in BNPF or hexadecimal format.

At least one optional imm4-60 Input/Output Module must be included in the Intellec system to provide the required reader input and output ports.



SPECIFICATIONS

TAPE MOVEMENT:
Tape Reading Speed
0 to 200 characters per second asynchronous
Tape Stopping
Stops "On Character"

TAPE CHARACTERISTICS:
Tapes must be prepared to ANSI X 3.18 or EMCA 10 Standards for base materials and perforations.

Reads tape of any material with thickness between 0.0027" and 0.0045" with transmissivity less than or equal to 5% (oiled buff paper tape).

Tape loading: in line

Tape width: 1 inch

ELECTRICAL CHARACTERISTICS:
AC Power Requirement
3 wire input with center conductor (earth ground) tied to chassis. 100, 115, or 127 VAC, single phase at 3.0 amps or 220 or 240 VAC and 1.5 amps; 47 to 63 Hz.

EQUIPMENT SUPPLIED:
Paper Tape Reader
Reader Cable
Reader Flat Cable
Fanfold Tape Guide
Fanfold Paper Tape
Hardware Manual
Installation and Operations Guide
Fanfold Guide Installation Instructions

NOTE: Operation of the imm4-90 in conjunction with the Intellec 4/MOD 4 and Intellec 4/MOD 40 requires Version 2.0 software.

8080 SYSTEM DESIGN KIT SDK-80

Complete single board microcomputer system including CPU, memory and I/O

Easy to assemble kit-form

High-performance (2 μs instruction cycle)

Interfaces directly with most terminals (75-4800 baud)

Large wire-wrap area for custom interfaces

Extensive system monitor software in ROM

PC board format and power, compatible with Intellec®MDS

The 8080 System Design Kit (SDK-80) is a complete, single board, microcomputer system in kit form. It contains all necessary components, including resistors, caps, crystal and miscellaneous hardware to complete construction. Included is a pre-programmed ROM that contains the system monitor for general software utilities and system diagnostics.

All that is required for operation are power supplies and a suitable terminal; TTY, CRT, etc., (level conversions and baud rate generation included on board).

The SDK-80 is an inexpensive, high-performance prototype system that has designed-in flexibility for simple interface to the users application.

DEVELOPMENT SYSTEMS

SPECIFICATIONS

CENTRAL PROCESSOR
CPU: 8080A
Instruction Cycle: 1.95 microsecond
Tcy: 488 ns

MEMORY
ROM: 2K bytes (expandable to 4K bytes) 8708/8308
RAM: 256 bytes (expandable to 1K bytes) 8111
Addressing: ROM 0000-0FFF
RAM 1000-13FF

INPUT/OUTPUT
Parallel: One 8255 for 24 lines (expandable to 48 lines).
Serial: One 8251 USART.
On-board baud rate generator (jumper selectable).
Baud Rates: 75, 110, 300, 600, 1200, 2400, 4800

INTERFACES
Bus: All signals TTL compatible.
Parallel I/O: All signals TTL compatible.
Serial I/O: RS232C/EIA
20 mA current loop TTY
TTL (one TTL load)

INTERRUPTS
Single level: Generates RST7 vector.
TTL compatible input.

DMA
Hold Request: Jumper selectable.

SOFTWARE
System Monitor: Pre-programmed 8708 or 8308 ROM
Addresses; 0000-03FF.
Features:

Display Memory Contents	(D)
Move blocks of memory	(M)
Substitute memory locations	(S)
Insert hex code	(I)
Examine Registers	(X)
Program Control	(G)
Break Point Capability	
Power-up start or system reset start.	

I/O: Console Device (serial I/O)

LITERATURE
Design Library:
8080 Users Manual
8080 Assembly Language Manual
PL/M Programming Manual
MDS Brochure
Reference Card (Programmers)
SDK-80 User's Guide

CONNECTORS
I/O: 25 pin female (RS232C)
PCB: MDS format

PHYSICAL CHARACTERISTICS (MDS MECHANICAL FORMAT)
Width: 12.0 in.
Height: 6.75 in.
Depth: 0.50 in.
Weight: approx. 12 oz.

ELECTRICAL CHARACTERISTICS (DC POWER)

V_{CC} 5V ±5%	1.3 Amps
V_{DD} 12V ±5%	0.35 Amps
V_{BB} −10V ±5%	0.20 Amps
or −12V ±5%	

MICROCOMPUTER MODULES

MCS-4/40™

Modules may be ordered individually. All modules are 8" wide, 6.18" high and use standard 100-pin connectors.

imm4-42 Central Processor Module

- This is a complete microcomputer system with the processor, program storage, data storage, and I/O in a single module.
- The heart of this module is Intel's 4004 single chip four-bit parallel processor — p-channel silicon gate MOS.
- Accumulator and sixteen working registers (4-bit).
- Subroutine nesting up to 3 levels.
- For development work, the CPU interfaces to standard semiconductor memory elements (provided by Intel's standard memory and I/O interface set 4008/4009).
- Sockets for 1K bytes of PROM (Intel 1702A PROM) are provided.
- 320 words (4-bit) of data storage (Intel 4002) are provided.
- Four 4-bit input ports and eight 4-bit output ports (includes TTY interface).
- Bus-oriented expansion of memory and I/O.
- Two phase crystal clock.

imm4-43 Central Processor Module

- Complete microcomputer system with Intel's high performance 4040 4-bit processor, program storage, data storage, I/O and system clock in a single module.
- 60 instructions including decimal arithmetic, register-to-register transfers, conditional branching, logical operations and I/O.
- Interrupt capability.
- Single step capability.
- 24 index registers.
- Subroutine nesting to 7 levels.
- Direct interface capability to all standard memories (i.e., TTL, NMOS, PMOS, CMOS) through Intel's 4289 Standard Memory Interface chip.
- Sockets for 1K x 8 bytes of program memory (Intel 4702A PROM) expandable to 4K x 8 using optional imm6-26 or imm4-24 modules.
- 320 4-bit bytes of data storage (Intel 4002) expandable to 2560 x 4 using optional imm4-22 or imm4-24 modules.
- Four 4-line input ports and eight 4-line output ports expandable to 16 input and 48 output ports using optional imm4-60, imm4-22 or imm4-24 modules.
- Two phase crystal clock.

imm4-22 Instruction/Data Storage Module

- This microcomputer module has memory capacity identical to the Central Processor Module and is used for expanding memory and I/O.
- Sockets for 1K bytes of PROM program storage are provided.
- 320 words (4-bit) of data storage are provided.
- Four 4-bit input ports and eight 4-bit output ports.

imm4-24 Data Storage Module

- This microcomputer module has capacity for sixteen Intel 4002 RAMS — 1280 words (4-bit) of data storage.
- 320 words (4-bit) of data storage are provided.
- A maximum Intellec 4 system may contain up to 2560 words of storage — decoding for this expansion is provided.
- A 4-bit output port is associated with each RAM on this microcomputer module providing sixteen 4-bit output ports on each module.
- All output ports are TTL compatible.

imm4-60 Input/Output Module

- This module provides input and output port expansion without additional memory.
- Eight 4-bit input ports and eight 4-bit output ports are provided.
- Ports on this module are TTL compatible.

MCS-8™

imm8-82 Central Processor Module

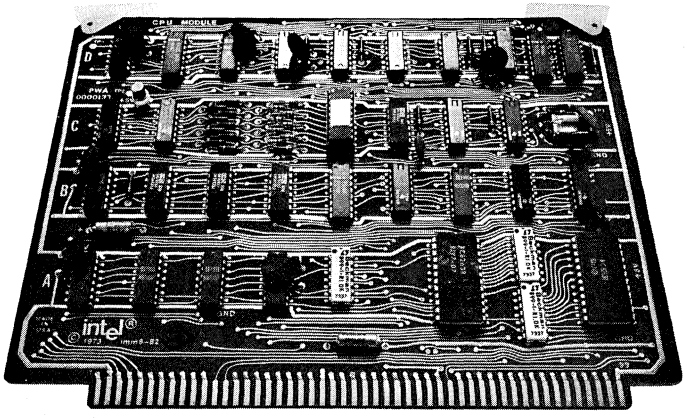
- Intel's 8008 eight-bit parallel single chip CPU — p-channel silicon gate MOS.
- Accumulator and six 8-bit working registers.
- Subroutine nesting up to seven levels.
- Interface to 16K 8-bit bytes of PROM, ROM, or RAM via the PROM Memory Module and RAM Memory Module.
- Interface for expansion to eight 8-bit input ports and twenty-four 8-bit output ports, via the I/O and Output Modules.
- Interrupt capability.
- Two phase crystal clock.
- All module interfaces are TTL compatible.

imm8-60 Input/Output Module

- Four 8-bit input ports (32 lines).
- Four 8-bit data latching output ports (32 lines).
- One pair of ports for TTY communication.
- All input and output ports are TTL compatible.

imm8-62 Output Module

- Eight 8-bit data latching output ports (64 lines).
- All output ports are TTL compatible.



imm8-82 Central Processor Module

MCS-80™

imm8-83 CPU Module

- Complete 8-bit parallel central processor module with system clocks, interface and control for memory, I/O ports, and real time interrupt.
- Utilizes Intel's high performance 8080 single chip n-channel microcomputer.
- 2.5 μsecond instruction execution time.
- 78 basic instructions including the entire 8008 instruction set.
- Direct addressing of up to 64K bytes of any speed ROM, PROM, or RAM memory.
- Unlimited subroutine nesting.
- Seven working registers — six 8-bit general purpose registers and an 8-bit accumulator.
- Separate 16-bit address bus, 8-bit output bus and 3 multiplexed 8-bit input busses for I/O input, memory input and interrupt data.
- Direct addressing of 256 input and 256 output ports.
- Multiple level real time interrupt capability.
- Direct memory access capability.
- All buses TTL compatible.

imm8-61 I/O Module

- Four 8-bit input and four 8-bit latching output ports.
- Directly compatible with imm8-83 central processor module.
- Integral asynchronous serial data communications capability and teletype interface.
- Jumper selectable transmission rates of 110, 1200 or 2400 baud.
- Crystal controlled clock.
- Capable of high speed serial communications to 9600 baud.
- TTL compatible.

imm8-63 Output Module

- Eight 8-bit latching output ports.
- Directly compatible with imm8-83 central processor module.
- Decoding provided for the selection of up to 256 individual output ports.
- TTL compatible.

COMMON SYSTEM MODULES

imm6-26 PROM Memory Module

- Provides sockets for up to sixteen 1702A electrically programmable and erasable PROMs for a system's fixed program memory (maximum 4K bytes/module).
- For volume requirements, Intel 2048-bit mask programmed MOS ROMs (1302) may be substituted in the same module.

imm6-28 RAM Memory Module

- A 4K x 8 n-channel MOS memory system using Intel's 1024-bit Static RAM (2102).
- Address latching, data latching, and module select decoding are provided on the card.
- Provides program storage for up to 4K instructions.

imm6-70 Universal Prototype Module

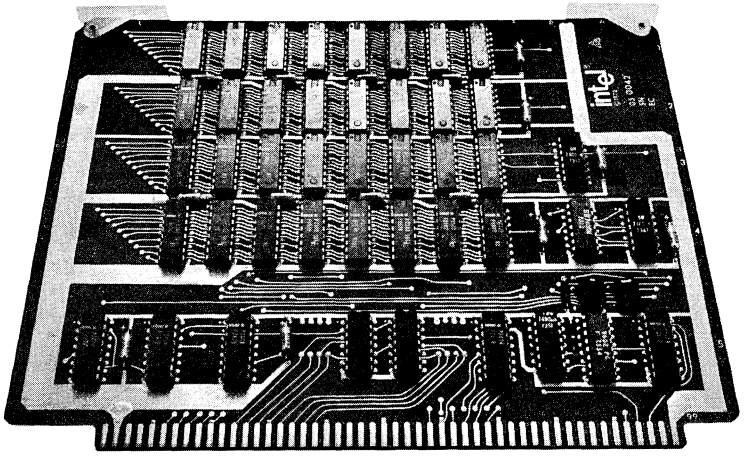
- Accommodates 14, 16, 24, or 40 pin wire wrap sockets (maximum of 52 16-pin sockets).
- Provides breadboard capability for developing custom and specialized interface circuits.

imm6-72 Module Extender

- Extends Intellec modules out of card chassis for ease in test and system debugging.

imm6-76 PROM Programmer Module

- Provides all timing and level shifting circuitry for programming Intel's programmable and erasable 1702A PROMs.



IMM 6-28 RAM MEMORY MODULE

CONVERSION KITS

imm4-88

The imm4-88 conversion kit provides an upgrade path for Intellec®4/MOD 4 microcomputer development systems. It includes all the hardware and software required to fully support 4040 CPU based microcomputer system development.

The conversion kit contains an imm4-43 CPU module, new memory controller, new front panel, and any software required.

NOTE: Due to necessary wiring changes, these conversions are done at the Intel factory. Contact local Intel salesmen or representatives for instructions.

imm8-88

The imm8-88 conversion kit provides an upgrade path for Intellec®8/MOD 8 microcomputer development systems. It includes all the hardware and software products required to fully support 8080 CPU based microcomputer system development. With the imm8-88 conversion kit installed in an Intellec 8/MOD 8, complete 8080 CPU hardware and software development capability is provided.

The conversion kit is installed by simply plugging in the three new hardware modules in the appropriate Intellec 8/MOD 8 chassis connectors and installing the new system monitor. The system can be quickly reconfigured to support 8080 CPU chip development by replacing the original boards and system monitor.

SBC 80/10 SINGLE BOARD COMPUTER

8080A Central Processing Unit

1 K bytes of read/write memory

Sockets for 4K bytes of programmable or masked read-only memory

48 Programmable I/O lines with sockets for interchangeable line drivers and terminators

Programmable Synchronous/Asynchronous communications interface with selectable teletype or RS232C compatibility.

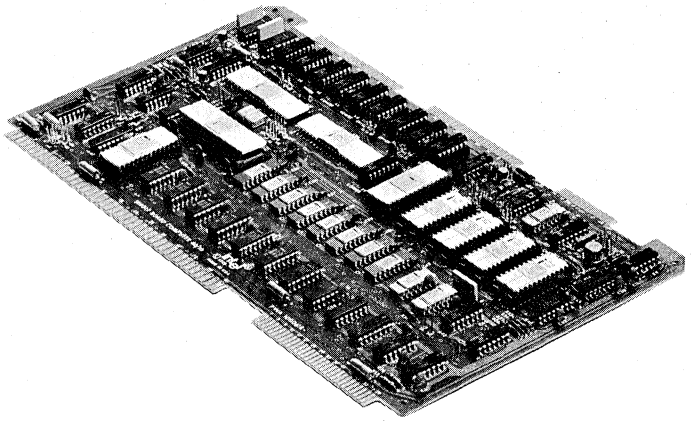
Six interrupt request lines.

Bus drivers for memory and I/O expansion

Compatable with optional memory and I/O boards.

The SBC-80/10 is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer based solutions for OEM applications. The SBC-80/10 is a complete computer system on a single 6.75-by-12 inch printed circuit card. The CPU, system clock, read/write memory, non-volatile read-only-memory, I/O ports and drivers, serial communications interface, bus control logic and drivers all reside on the board.

Memory and I/O expansion may be achieved using standard Intel boards. Memory may be expanded to 65,536 bytes by adding user specified combinations of SBC-016 16K byte RAM boards, SBC-406 6K byte PROM boards, and SBC-416 16K PROM boards. Input/output capacity may be expanded to 63 8-bit input ports and 63 8-bit output ports using SBC-508 Input/Output boards. Each I/O board contains four 8-bit input ports and four 8-bit output ports. Memory and I/O may be expanded simultaneously (i.e. 4K bytes of RAM, 4K bytes of PROM, and 48 programmable I/O lines, and a USART) by using the SBC-104 Combination board. Expandable backplanes and card-cages are available to support multi-board systems.



SPECIFICATIONS

WORD SIZE

Instruction: 8, 16, or 24 bits
Data: 8 bits

CYCLE TIME

Basic Instruction Cycle: 1.95 μsec
Note: Basic instruction cycle is defined as the fastest instruction (i.e. four clock cycles)

MEMORY ADDRESSING

On-Board ROM/PROM: 0-0FFF
On-Board RAM: 3C00-3FFF

I/O CAPACITY

Parallel: 48 programmable lines

Note: Expansion to 504 input and 504 output lines can be accomplished using optional I/O boards.

Serial: (USART)

Frequency (KHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷16	÷64
307.2	–	19200	4800
153.6	–	9600	2400
76.8	–	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	–	110

SPECIFICATIONS

MEMORY CAPACITY

On-Board ROM/PROM: 4K bytes (sockets only)
On-Board RAM: 1K bytes
Off-Board Expansion: Up to 65,536 bytes using user specified combinations of RAM, ROM, and PROM
NOTE: ROM/PROM may be added in 1K byte increments.

I/O ADDRESSING

On-Board Programmable I/O

Port	1	2	3	4	5	6	8255 #1 Control	8255 #2 Control	USART Data	USART Control
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

Synchronous:
5-8 bit characters
Internal or external character synchronization
Automatic Sync Insertion
Asynchronous:
5-8 bit characters
Break characters generation
1, 1-1/2, or 2 stop bits
False start bit detectors
Full duplex, double buffered transmitter and receiver
Parity, overrun, and framing error detection

INTERRUPTS

Single-level with on-board logic that automatically vectors processor to location 38_{16} using RESTART 7 instruction. Interrupt requests may originate from user specified I/O (2) the programmable peripheral interface (2), or USART (2)

INTERFACES

Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Serial I/O: RS232C or 20 mil current loop TTY interface (jumper selectable)
Interrupt Requests: All TTL compatible

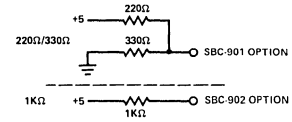
LINE DRIVERS AND TERMINATORS

I/O Drivers:
The following line drivers and terminators are all compatible with the I/O driver sockets on the SBC-80/10.

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note: I = inverting N.I. = non-inverting OC = open collector

I/O Terminators:
Terminators: 220Ω/330Ω divider or 1 kΩ*



*Must be ordered separately.

Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	Tri-State	25
Address	Tri-State	25
Commands	Tri-State	25

SYSTEM CLOCK

2.048 MHz ± 0.1%

CONNECTORS

Bus:
86 pin double-sided PC edge connector
0.156 inch centers
Mating Connector: Control Data Corp. VPB01E43A00A1
Parallel I/O:
Two 50 pin double-sided PC edge connectors
0.1 inch centers
Mating Connector: 3M 3415-000 or TI H312125
Serial I/O:
26 pin double-sided PC edge connector
0.1 inch centers
Mating Connector: 3M 3462-000 or TI H312113

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.14 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz. (0.48 Kg)

ELECTRICAL CHARACTERISTICS

DC Power:

V_{CC} = +5 ± 5%	I_{CC} = 2.9 A max
V_{DD} = +12 ± 5%	I_{DD} = 150 mA max
V_{BB} = −5V ± 5%	I_{BB} = 2 mA max
V_{SS} = −12V ± 5%	I_{SS} = 150 mA max

Note: Does not include power required for options PROM, I/O drivers, and I/O terminators.

MICROCOMPUTER SOFTWARE PRODUCTS

The following section contains information on Intel's Cross Software Products and User's Library. These cross products are all written in FORTRAN IV and are designed to run on a large computer system while generating code for or simulating one of Intel's microcomputers. All these products are also available on several computer timesharing services worldwide.

Included among these products are the PL/M™ compilers. The PL/M™ high level programming language was developed by Intel for the 8008 and 8080 microcomputers. Use of this language can significantly reduce programming time and costs.

A partial list of programs in the Intel microcomputer User's Library is also included. New programs are constantly being added to the library in a continuing effort to increase the size of the largest commercially available library of microcomputer programs in the world. You are encouraged to become a member to reap the benefits of the knowledge and experience of hundreds of users. Contributed programs are gratefully accepted.

DEVELOPMENT SYSTEMS

MCS-40 CROSS ASSEMBLER

Accepts all 4004 and 4040 instructions

Conditional assembly capability

Full macro facility

Hexadecimal or BNPF object code formats

Written in ANSI standard FORTRAN IV

Comprehensive user documentation

Instantly available on worldwide timesharing services

The MCS-40 Cross Assembler, MAC40, is a powerful program development tool for Intel's® 4-bit microcomputers, the 4004 and the new 4040. MAC40 provides extensive capabilities which reduce the time and effort involved in program development, debug and documentation. The cross assembler allows usage of the high speed I/O and text editing capability of a large computer system to further shorten the programming task.

MAC40 translates 4004/4040 machine assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions, or to move the program to another memory location. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits MAC40 to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

Output from MAC40 may be punched to paper tape in hex format for loading into an Intellec® 4 Development System or may be punched in BNPF format to program ROMs.

MAC40 is written in ANSI standard FORTRAN IV and is designed to run on most large scale computing systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

SPECIFICATIONS

CAPABILITIES:

Accepts all 66 instruction mnemonics plus 10 pseudo-operators.

Allows up to 499 labels in standard configuration; easily expandable.

Allows a total of up to 9 levels of nested conditional assembly and nested macro-calls.

User definable I/O formats.

Batch or interactive mode.

OPERATIONAL ENVIRONMENT:

Hardware required

32-bit or larger word size

12–16K words depending on machine

Software required

ANSI standard FORTRAN IV compiler

SHIPPING MEDIA:

Magnetic tape

TAPE FORMAT:

9 Track	80 Byte unblocked records
EBCDIC	
800 BPI	Unlabeled

TAPE CONTENTS:

MCS-40™ Cross Assembler (FORTRAN IV Source)

MERGE Source File Editing Program (FORTRAN IV Source)

XCNV4 Conversion Program (FORTRAN IV Source)

DOCUMENTATION PACKAGE INCLUDES:

4004/4040 Assembly Language Programming Manual

MAC4 External Reference Specification

Pocket Reference Card

MCS-8™ CROSS ASSEMBLER

Accepts all 8008 instructions

Conditional assembly capability

Full macro facility

Hexadecimal or BNPF object code formats

Written in ANSI standard FORTRAN IV

Comprehensive user documentation

Instantly available on worldwide timesharing services

The MCS-8™ Cross Assembler, MAC8, is a powerful program development tool for Intel's® 8008 microcomputer. MAC8 provides extensive capabilities which reduce the time and effort involved in program development, debug and documentation. The cross assembler allows usage of the high speed I/O and text editing capability of a large computer system to further shorten the programming task.

MAC8 translates symbolic 8008 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions, or to move the program to another memory location. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits MAC8 to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

Output from MAC8 may be loaded directly to the 8008 Simulator (INTERP/8) for interactive, symbolic debugging or may be punched to paper tape in hex format for loading into an Intellec® 8/Mod 8 Development System. It may also be punched in BNPF format to program ROMs.

MAC8 is written in ANSI standard FORTRAN IV and is designed to run on most large scale computing systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

MCS-8™ ASSEMBLY LANGUAGE PROGRAMMING EXAMPLE:

```
                                ; UMUL – UNSIGNED INTEGER MULTIPLY
                                ; CALL:  ARGUMENTS IN C & D
                                ; EXIT:  HI ORDER PRODUCT IN B
                                ;        LO ORDER PRODUCT IN C
                                ; REGS:  A,B,E AND FLAGS EXCEPT CARRY ALTERED
001E                            UMUL:
001E  0E00                              MVI B,0
0020  2609                              MVI E,9
0022                            UMUL0:
0022  C2                               MOV A,C         ; ROTATE CARRY INTO
0023  1A                               RAR             ; PRODUCT – MULTIPLIER
0024  D0                               MOV C,A         ;  SHARED REGUSTER
0025  21                               DCR E           ;   FORCING NEXT LSB
0026  2B                               RZ              ;    INTO CARRY
0027  C1                               MOV A,B         ; EXIT IF 8TH ITERATION
0028  402C00                           JNC UMUL1       ; IF CARRY SET
002B  83                               ADD D           ; ADD MULTIPLICAND TO '
002C                            UMUL1:                  ; PRODUCT
002C  1A                               RAR
002D  C8                               MOV B,A         ; ROTATE MOST SIGNIFICANT
002E  442200                           JMP UMUL0       ;  PRODUCT AND REPEAT LOOP
```

SPECIFICATIONS

CAPABILITIES:

Accepts all 48 instruction mnemonics plus 10 pseudo-operators.

Allows up to 499 labels in standard configuration; easily expandable.

Allows total of up to 9 levels of nested conditional assembly and nested macro-calls.

User definable I/O formats.

Batch or interactive mode.

OPERATIONAL ENVIRONMENT:

Hardware required

32-bit or larger word size

12—16K words depending on machine

Software required

ANSI standard FORTRAN IV compiler

SHIPPING MEDIA:

Magnetic tape

TAPE FORMAT:

9 Track	80 Byte unblocked
EBCDIC	records
800 BPI	Unlabeled

TAPE CONTENTS:

MCS-8™ Cross Assembler (FORTRAN IV Source)

MERGE Source File Editing Program (FORTRAN IV Source)

CONV8 Conversion Program (FORTRAN IV Source)

DOCUMENTATION PACKAGE INCLUDES:

8008 Assembly Language Programming Manual

MAC8 External Reference Specification

Pocket Reference Card

DEVELOPMENT SYSTEMS

4004/4040 SIMULATOR

Simulates all 4004/4040 machine instructions

Accepts output from MAC40, the Intel® 4004/4040 Cross Assembler

Contains extensive symbolic debugging capabilities

Written in ANSI standard FORTRAN IV

Instantly available on worldwide timesharing services

COMMAND CAPABILITIES:

Set breakpoints

Trace program execution

Dump and modify memory

Examine and modify registers

Examine and set I/O ports

Simulate the 4040 hardware interrupt

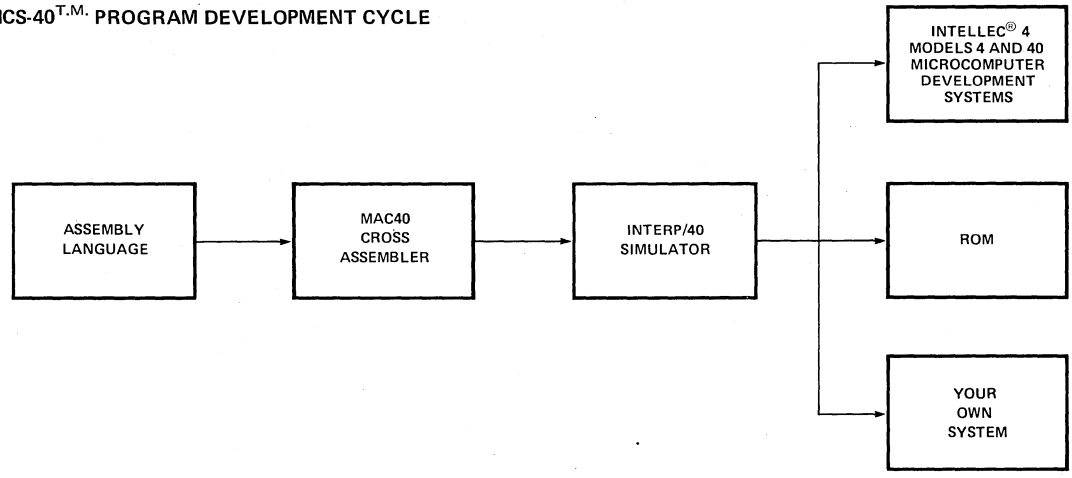
Measure program execution time

The 4004/4040 Simulator, INTERP/40, is a complete simulation and debug program for the Intel® 4004 and 4040 microcomputers. Programs can be run, displayed, stopped, and altered allowing step by step refinement without continuous reassembly of the source program. INTERP/40 provides powerful commands to control the execution of 4004 and 4040 programs. Extensive debug features are built in to help reduce the time and cost involved in program checkout.

INTERP/40 also provides symbolic reference to storage locations and operation codes as well as numeric reference in various number bases.

INTERP/40 is written in FORTRAN IV and is designed to run on most large scale computer systems with a 32-bit or larger integer format (word size). It is also available for immediate use on major timesharing services throughout the world.

MCS-40™ PROGRAM DEVELOPMENT CYCLE



SPECIFICATIONS

CAPABILITIES:
Provides total software simulation of the Intel® 4004 and 4040 CPU's.

Can be run in batch or interactive mode.

OPERATIONAL ENVIRONMENT:
Hardware required
- 32-bit or larger word size
- 12-15K words of memory, depending on machine

Software required
- FORTRAN IV compiler

SHIPPING MEDIA:
Magnetic tape

TAPE FORMAT:

9-track	80-byte unblocked
EBCDIC	records
800BPI	Unlabeled

TAPE CONTENTS:
4004/4040 Simulator
(FORTRAN IV Source)
MERGE Source File Editing Program
(FORTRAN IV Source)

DOCUMENTATION PACKAGE:
INTERP/40 External Reference Specification

DEVELOPMENT SYSTEMS

8008 SIMULATOR

Simulates all 8008 machine instructions

Accepts output from PL/M[T.M.] compiler or MAC8 cross assembler

Comprehensive debug features

Written in FORTRAN IV

Instantly available on worldwide timesharing services

Comprehensive user documentation

The 8008 Simulator, INTERP/8, is a complete simulation and debug program for the Intel® 8008 microcomputer. INTERP/8 provides powerful commands to control the execution of 8008 programs. Extensive debug features are built-in to help reduce the time and cost involved in program checkout.

INTERP/8 simulates execution of all 8008 machine instructions. Programs either compiled on the PL/M[T.M.] compiler or assembled on the MAC8 Cross Assembler may be loaded directly into INTERP/8 for simulation and checkout.

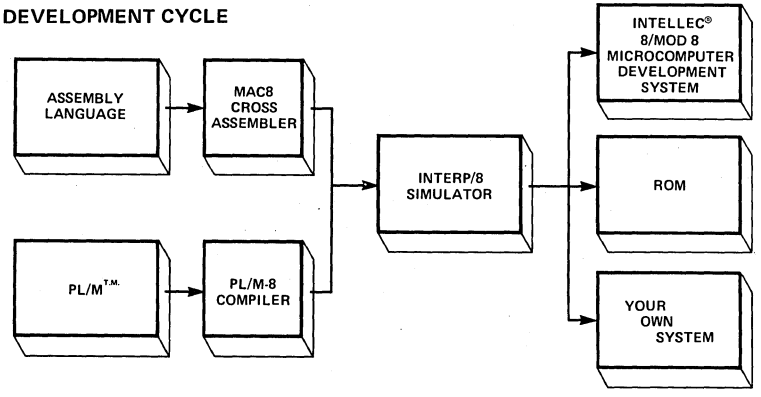
INTERP/8 provides commands to:

- Set Breakpoints
- Trace Program Execution
- Dump and Modify Memory
- Examine and Modify Registers
- Measure Program Timing
- Examine and Set I/O Ports
- Perform Interrupts and Stack Manipulations
- Perform Address Arithmetic

INTERP/8 also provides symbolic debugging capability. Memory locations may be referenced by their symbolic names, either through labels or variable names. This eliminates the need to know the specific absolute address of each variable or label.

INTERP/8 is written in FORTRAN IV and is designed to run on most large-scale computer systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

MCS-8[T.M.] PROGRAM DEVELOPMENT CYCLE



SPECIFICATIONS

CAPABILITIES:
Simulates all 48 machine instructions

Allows full 16K program

Can be run in batch or interactive mode

OPERATIONAL ENVIRONMENT:
Hardware required
32-bit or larger word size
15—20K words of memory, depending on machine
Software required
FORTRAN IV compiler

SHIPPING MEDIA:
Magnetic tape

TAPE FORMAT:

9-track	80-byte unblocked
EBCDIC	records
800 BPI	Unlabeled

TAPE CONTENTS:
8008 Simulator
(FORTRAN IV Source)
MERGE Source File Editing Program
(FORTRAN IV Source)

DOCUMENTATION PACKAGE:
INTERP/8 User's Manual
INTERP/8 Installation Guide

MCS-80™ CROSS ASSEMBLER

Accepts all 8080 instructions

Conditional assembly capability

Full macro facility

Hexadecimal or BNPF object code formats

Written in ANSI standard FORTRAN IV

Comprehensive user documentation

Instantly available on worldwide timesharing services

The MCS-80 Cross Assembler, MAC80, is a powerful program development tool for Intel's® 8080 microcomputer. MAC80 provides extensive capabilities which reduce the time and effort involved in program development, debug and documentation. The cross assembler allows usage of the high speed I/O and text editing capability of a large computer system to further shorten the programming task.

MAC80 translates symbolic 8080 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions, or to move the program to another memory location. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits MAC80 to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

Output from MAC80 may be loaded directly to the 8080 Simulator (INTERP/80) for interactive, symbolic debugging or may be punched to paper tape in hex format for loading into an Intellec® MDS Microcomputer Development System. It may also be punched in BNPF format to program ROMs.

MAC80 is written in ANSI standard FORTRAN IV and is designed to run on most large scale computing systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

MCS-80™ ASSEMBLY LANGUAGE PROGRAMMING EXAMPLE:

```
                        ;       THIS SUBROUTINE PERFORMS DECIMAL ADDITION
                        ;       FOR 16 DECIMAL DIGITS ON THE INTEL 8080
                        ;       MICROCOMPUTER.
                        ;
                        ;       THE ADDRESS OF THE FIRST OPERAND IS EXPECTED TO BE IN THE
                        ;       D AND E REGISTERS AND THE ADDRESS OF THE
                        ;       SECOND OPERAND SHOULD BE IN THE H AND L
                        ;       REGISTERS.  THE RESULT IS STORED OVER THE
                        ;       FIRST OPERAND.  THE ADDITION IS DONE TWO DIGITS
                        ;       AT A TIME.
                        ;
0000                    DECAD:
0000  0E08                      MVI C,8         ; INITIALIZE DIGIT COUNTER (HALF)
0002  AF                        XRA A           ; CLEAR CARRY BIT
0003                    LOOP:
0003  1A                        LDAX D          ; LOAD TWO DIGITS FROM FIRST OPERAND
0004  8E                        ADC M           ; ADD TWO DIGITS FROM SECOND OPERAND WITH CARRY
0005  27                        DAA             ; DECIMAL ADJUST RESULT
0006  12                        STAX D          ; STORE TWO DIGITS OF RESULTS OVER FIRST OPERAND
0007  23                        INX H           ; INCREMENT ADDRESS OF SECOND OPERAND
0008  13                        INX D           ; INCREMENT ADDRESS OF FIRST OPERAND
0009  0D                        DCR C           ; DECREMENT DIGIT COUNT
000A  C20300                    JNZ LOOP        ; CONTINUE IF MORE DIGITS LEFT
000D  C9                        RET
```

8080 SIMULATOR

Simulates all 8080 machine instructions

Accepts output from PL/M[T.M.] compiler or MAC80 Cross Assembler

Comprehensive debug features

Written in FORTRAN IV

Instantly available on worldwide timesharing services

Comprehensive user documentation

The 8080 Simulator, INTERP/80[T.M.], is a complete simulation and debug program for the Intel® 8080 microcomputer. INTERP/80 provides powerful commands to control the execution of 8080 programs. Extensive debug features are built in to help reduce the time and cost involved in program checkout.

INTERP/80 simulates execution of all 8080 machine instructions. Programs either compiled on the PL/M[T.M.] compiler or assembled on the MAC80 Cross Assembler may be loaded directly into INTERP/80 for simulation and checkout.

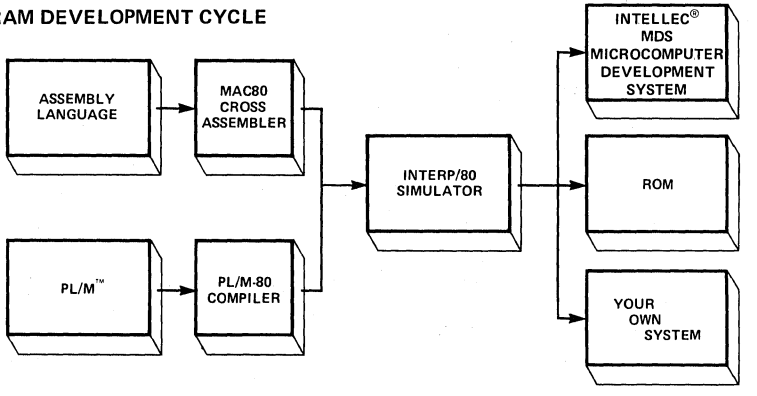
INTERP/80 provides commands to:

- Set Breakpoints
- Trace Program Execution
- Dump and Modify Memory
- Examine and Modify Registers
- Measure Program Timing
- Examine and Set I/O Ports
- Perform Interrupts and Stack Manipulations
- Perform Address Arithmetic

INTERP/80 also provides symbolic debugging capability. Memory locations may be referenced by their symbolic names, either through labels or variable names. This eliminates the need to know the specific absolute address of each variable or label.

INTERP/80 is written in FORTRAN IV and is designed to run on most large-scale computer systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

MCS-80[T.M.] PROGRAM DEVELOPMENT CYCLE



SPECIFICATIONS

CAPABILITIES:
Simulates all 78 machine instructions

Allows 16K program, easily expandable

Can be run in batch or interactive mode

OPERATIONAL ENVIRONMENT:
Hardware required
32-bit or larger word size
15–20K words of memory, depending on machine
Software required
FORTRAN IV compiler

SHIPPING MEDIA:
Magnetic tape

TAPE FORMAT:

9-track	80-byte unblocked
EBCDIC	records
800 BPI	Unlabeled

TAPE CONTENTS:
8080 Simulator
(FORTRAN IV Source)
MERGE Source File Editing Program
(FORTRAN IV Source)

DOCUMENTATION PACKAGE:
INTERP/80 User's Manual
INTERP/80 Installation Guide

intel®

PL/M™ HIGH LEVEL PROGRAMMING LANGUAGE MCS-8™ AND MCS-80™ CROSS COMPILERS

Reduces program development time and cost

Improves product reliability and eases maintenance

Available for 8008 and 8080

Comprehensive user documentation

Hexadecimal or BNPF object code formats

Written in ANSI standard FORTRAN IV

Instantly available on worldwise timesharing services

PL/M is a high-level system programming language, specifically designed to ease the programming task for INTEL's 8-bit microcomputers, the 8008 and the 8080. PL/M is a powerful tool, well suited to the requirements of the microcomputer system designer and implementor. The language has been designed to facilitate the use of modern techniques in structured programming. These techniques can lead to rapid system development and checkout, straightforward maintenance and modification, and high product reliability.

The PL/M compilers convert a free-form symbolic PL/M program into an equivalent 8008 or 8080 object program. The compilers themselves take care of all the details of machine or assembly language programming, which permits the programmer to concentrate entirely on effective software design, and the logical requirements of his system.

Output from the PL/M compiler may be loaded directly into the 8008 or 8080 simulator programs for interactive, symbolic debugging or may be punched to paper tape in hex format for loading into an Intellec® Microcomputer Development System. It may also be punched in BNPF format to program ROMs.

The PL/M compilers are written in ANSI standard FORTRAN IV and are designed to run on any large-scale computer system with a minimum 32-bit integer format (word size). They are also available for immediate use on several worldwide timesharing systems.

PL/M PROGRAMMING EXAMPLE:

```
                                    /*  BUBBLE SORT DECLARATION  */
SORT: PROCEDURE (N) ADDRESS;
    /*    N = LENGTH OF A
          COUNT = NR. OF SWITCHES PERFORMED TO-DATE
          SWITCHED = (BOOLEAN) HAVE WE DONE ANY SWITCHING YET ON THIS SCAN?  */
    DECLARE (N, I, SWITCHED) BYTE,
          (TEMP, COUNT) ADDRESS;
    SWITCHED = 1;              /*  SWITCHED = TRUE MEANS NOT DONE YET  */
    COUNT = 0;
    DO WHILE SWITCHED;
          SWITCHED = 0;        /*  BEGIN NEXT SCAN OF A  */
          DO I = 0 TO N-2;
                IF A(I) > A(I+1) THEN
                      DO;                  /*  FOUND A PAIR OUT OF ORDER  */
                      COUNT = COUNT + 1;
                      SWITCHED = 1;        /*  SET SWITCHED = TRUE  */
                      TEMP = A(I);         /*  SWITCH THEM INTO ORDER  */
                      A(I) = A(I+1);
                      A(I+1) = TEMP;
                      END;
          END;
          /*  HAVE NOW COMPLETED A SCAN  */
    END  /*  WHILE  */;
    /*  HAVE NOW COMPLETED A SCAN WITH NO SWITCHING  */
    RETURN COUNT;
END SORT;
```

SPECIFICATIONS

OPERATING ENVIRONMENT:
Required hardware
32-bit or larger word size
20–25K words of memory, depending on machine
Required software
ANSI standard FORTRAN IV compiler

SHIPPING MEDIA:
Magnetic tape

TAPE FORMAT:
9-track EBCDIC
800 BPI 80-byte unblocked records
Unlabeled

DOCUMENTATION PACKAGE:
8008 and 8080 PL/M Programming Manual
8008 (or 8080) PL/M Compiler Operator's Manual

TAPE CONTENTS:
PLM Pass 1 (FORTRAN IV Source)
PLM Pass 2 (FORTRAN IV Source)
MERGE Source File Editing Program (FORTRAN IV Source)
Sample Test Program (PL/M Source)

SERIES 3000 CROSS MICROPROGRAMMING SYSTEM

Built-in series 3000 fields and mnemonics
User definable fields and mnemonics
Hierarchical field defaults
Free field statement format
String macro capability
Extended address generation
Graphical microprogram memory display
Symbolic label reference directory
MCU jump address validation
RAM/ROM/PROM programming file generation

The Intel® Series 3000 Cross Microprogramming System, CROMIS, is an advanced software system that supports the generation of microprograms for custom Series 3000 processor and controller micro-architectures. It provides extensive programming facilities that greatly reduce the time and effort required to develop, debug, and document a microprogram.

CROMIS consists of two major software subsystems, XMAS and XMAP, XMAS is a symbolic microassembler which is dynamically user extensible in the size and structure of the target microinstruction format. XMAP is a complementary subsystem which maps the microinstruction bit patterns produced by XMAS into the desired physical microprogram memory locations.

In addition to providing four built-in microinstruction fields and corresponding mnemonic sets for the basic 3001 MCU and 3002 CPE functions, XMAS accepts user definitions for extended microinstruction fields and their associated mnemonics. Graphic debugging aids, string macro capability, definable defaults, and extended address generation further simplify the microprogramming of Series 3000 computing elements.

XMAP accepts the microinstruction file produced by XMAS and generates under user specifications one or more programming files for use with standard memory components. It enables the user to specify the mapping of the field into the physical bit positions of the microprogram memory components.

CROMIS is designed for use on almost any modern computing system with high speed I/O and on-line file facilities. It is available in ANSI (standard) FORTRAN IV source form for user installation or may be immediately accessed on any of several major timesharing services throughout the world. To insure the long term reliability and maintainability of CROMIS, all component programs are written in a highly modular, structured programming style with extensive operational documentation.

SPECIFICATIONS

XMAS CAPABILITIES

Translates all 3001 MCU and 3002 CPE mnemonics.

Dynamically allocates storage for labels, values and strings in a user expandable data area.

Accepts microinstruction format definitions of up to 64 total bits.

Provides extended address generation for up to 16K microinstructions.

Includes a four-level user definable field default mechanism.

XMAP CAPABILITIES

Provides direct or inverted mapping for any bit in any microinstruction field.

Permits explicit 1's or 0's to be specified for unused bit locations.

Generates standard BNPF or hexadecimal programming files.

Accepts memory configuration definitions from 1 X 1 bits to 16K X 16 bits.

OPERATIONAL ENVIRONMENT

Required hardware:
- 16-bit or larger word size
- 5 rewindable data files (disc or tapes)

Required software:
- ANSI standard FORTRAN IV compiler

TAPE CONTENTS

TAPE 1
- Part 1 of XMAS FORTRAN IV Source

TAPE 2
- Part 2 of XMAS FORTRAN IV Source
- XMAS Sample Program
- XMAP FORTRAN IV Source
- XMAP Sample Program
- MERGE File Editing Program

SHIPPING MEDIA

Two 2400' magnetic tapes

TAPE FORMAT

9-track	800 bpi
80 byte	unblocked
EBCDIC	unlabeled

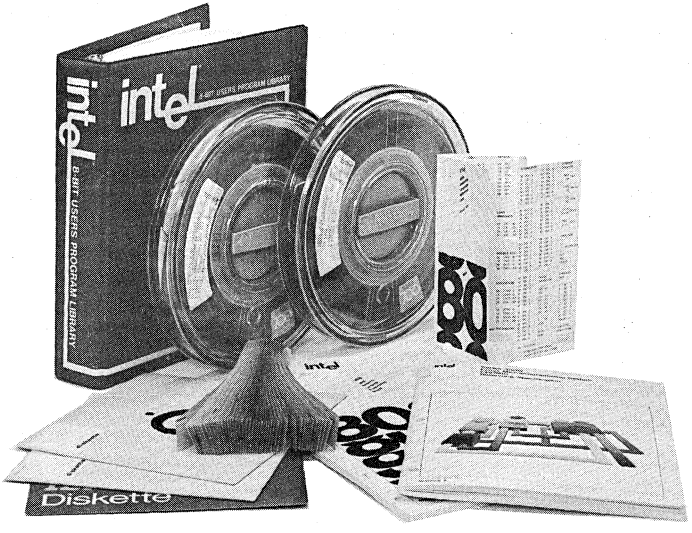
DOCUMENTATION

Microprogramming the Series 3000
XMAS/XMAP Message Summary
XMAS Installation Guide
(preamble to XMAS FORTRAN source)
XMAP Installation Guide
(preamble to XMAP FORTRAN source)

MICROCOMPUTER SOFTWARE LIBRARY
USER'S PROGRAM LIBRARY

The Intel Microcomputer User's Library is a collection of programs, subroutines, procedures and macros written by users of Intel's 4004, 4040, 8008 or 8080 microcomputers. Thanks to customer contributions to the User's Library, Intel is now able to make these programs available to all users of Intel microcomputers. By taking advantage of the availability of these general purpose routines, the microcomputer design engineer and programmer can save many hours of programming and debugging.

A complete, documented listing of each program, procedure or macro in the user's library is sent to each member. This includes information on the program environment, required hardware and software, subroutine calling sequences and memory requirements. As new programs are submitted to the User's Library, they will be sent to all members. Strict documentation standards will be maintained to assure the usability of each library program by every interested member. Several of the available programs are listed in this brochure.



There are two user's libraries, one each containing programs for the Intel 4-bit and 8-bit microcomputer systems, respectively. Membership in each user's library is available to any interested person or organization. A yearly membership fee of $100 is charged, for which the member receives a manual of all programs in that library and all updates during the year. For those prospective members who submit a program to the library, a free one-year membership will be awarded. A submittal form for program donation is included in this catalog. More forms may be obtained from any Intel representative.

DEVELOPMENT SYSTEMS

Ordering Information

To become a member, send a program, purchase order, or check to:

User's Library
Microcomputer Systems
Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051

MICROCOMPUTER SOFTWARE LIBRARY
PARTIAL PROGRAM INDEX-4-BIT USERS LIBRARY

TITLE	FUNCTION
Cross Assembler on PDP-8	Performs symbolic assembly for 4004 assembly language programs. The assembler runs on a DEC PDP-8 minicomputer.
Cross Assembler for NOVA Computer	Assemble MCS-4 programs and program PROMs.
BNPF Tape Generator for PDP-8	Produces a BNPF object tape from the output of the PDP-8 assembler modified to assemble MCS-4 programs.
MCS-4 Simulator for PDP-8	Simulates operation of MCS-4 system; allows breakpoints, dumps, modification of RAM or ROM, I/O under user control, provides cycle counter for timing. Accepts output of PAL8 assembler in binary form.
MCS-40 Cross Assembler	Program to perform assembly of 4040 programs on an Intellec 8/Mod 80.
Intel MCS-40 Cross Assembler and Text Editor	Edit and assemble MCS-40 source language using a Computer Automation Alpha-16/Alpha-LSI producing program listings, error diagnostics, source and object tapes.

All programs listed below will execute on the 4004 or 4040 CPU.

A Chebyshev Approximation Package	The package contains approximation routines for sine, cosine, arctangent, natural logrithm ($\log_e$), and exponential functions (e^x). It also contains routines for performing addition, complement, multiplication, and division on 64-bit binary numbers.
Parity Checker/Generator	Routine to check or generate parity for 8-bit byte. Utilizes modulo-2 counting technique.
Parity Generator, ASCII Character	Routine to add even parity bits to 7-bit ASCII character. Utilized modulo-2 counting technique.
Code Conversion: ASCII to EBCDIC	Table and routine to perform 7-bit ASCII to 8-bit EBCDIC code conversion. Full table with 128 entries provided.
Delay Subroutines	To conditionally generate a selectable time delay of: 1. 1 through 256 ms in one ms increments 2. 1 through 256 quarter seconds in one quartersecond increments 3. 1 through 15 minutes in one minute increments
Bit Manipulation Routine	AND, OR, XOR, COMPARE, set unselected bits, clear selected bits, test ones.
Universal Logic Subroutines	Forms logical AND, OR, XOR, $\overline{\text{XOR}}$ functions functions between the contents of Registers 0 and 1.
8-bit Parity Check Annex	Compute parity of 8-bit word without affecting any registers or carry.
Binary to BCD Converter	Converts 16-bit binary value into BCD.
Data Compare	Compares two 8-digit numbers and returns a pointer to the greater value in the carry.
Paper Tape Edit	Add, correct, or delete lines in generating a new paper tape without manually controlling tape reader.
IOMEC SERIES THREE (S-3) Cartritape to Intel MCS-4	Routines which allow full control of the IOMEC S-3 by the MCS-4.

TITLE	FUNCTION
I/O Test	To exercise all I/O lines to allow for troubleshooting of system design, wiring errors, and chip malfunctions.
Bowmar TP 3100 Printer Routine	This program is to run a Bowmar model 3100 thermal printer.
8-Digit Register Dispaly	Program to display 8 digits of data.
Intellec 4/Mod 40 — Silent 700 Interface	Program to interface Intellec 4/Mod 40 to TI Silent 700 terminal.
PROM Dump Utility Program	This is a program to dump the contents of a PROM in the front panel socket onto the teletype printer. The first address and first word is always printed out in the form "00-00" as address-contents. All subsequent address contents-listings are printed out only if the contents of the respective location are different from the contents of the previous location.
PRO FORMA	This program assists in the compiling of source code tapes by eliminating errors and typing mistakes. In the keyboard mode it will only transmit characters to the paper tape punch that are valid in the context of the system assembly language, and automatically formats individual lines and pages to suit.
Peripheral Interface Routine for a Thermal Strip Printer	This subroutine controls the printing of data (numbers and selected characters) on thermal print paper using a 4x5 dot matrix thermal printhead. The software provides character generation and controls the timing of the print cycle.
MCS-4/40 Dissembler	To convert MCS-4 or MCS-40 machine code programs back into mnemonic or assembly code to assist in the modification of programs.
Right Justified HEX Data Shifter	Shifts HEX digit (four binary bits) into RAM right justified.
Floating Point Arithmetic Subroutine Package	Performs decimal arithmetic on 16-digit floating point operands (hexadecimal arithmetic is possible with minor changes). Numbers may range from 10^{-130} to 10^{125}. Functions include Addition, Subtraction, Multiplication, Division and a normalization routine.
HEXBCD	Convert 2 digit HEX value to decimal range.
Fast Binary Multiply: Selectable Bit Precision and Constant Execute Time	The user loads the input variables to CPU registers and specifies one of five multiply precisions (12x12, 12x8, 8x8, 8x4, 4x4) via a code character in register E.
Fast Decimal Multiplication Routine	This subroutine computes the product (16 digit maximum) of two fixed point decimal numbers (each 8 digits maximum).
Automatic Digital Integration	Program will detect and integrate peaks from an amino acide analyzer and type out the area under the peak on the teletype. Program will detect saddle peaks and do simple baseline correction.
Multiply/Divide 8 Decimal Numbers	The multiply/divide subroutine calculates the product/quotient by repeated shifted additions or subtractions and by incrementing/decrementing the multiplier/quotient.
Binary to BCD Converter	Converts an 8-bit binary number to a BCD number.

PARTIAL PROGRAM INDEX-8-BIT USERS LIBRARY
8-BIT MICROCOMPUTER SOFTWARE LIBRARY

TITLE	FUNCTION
Save/Restore CPU State on an Interrupt	Saves the CPU registers and flags to memory at the start of interrupt processing and restores the CPU registers and flags after the interrupt has been processed.
RAM TEST PROGRAM	Performs write and read of all zeros and ones, checkerboard test and unique address test. The RAM to be tested is successively initialized to a value and then tested.
TTY Binary Load Routine	Will load memory from a paper tape which is formatted into blocks of 256 or less binary bytes and tests each block against a checksum frame for any read errors. The tape format requires a rubout to indicate start of blocks followed by the starting page address, the starting byte address, the word count up to 256 bytes of data and a checksum in that order. A block of data may overlap pages but may not exceed 256 bytes in length. The last block of data should be followed by two consecutive rubouts to indicate end of data. Program will then branch to page 000 byte 000.
TTY Binary Dump Routine	Program will punch the contents of memory to paper tape which is formatted into blocks of 256 or less binary bytes with checksum. Tape format begins with a rubout to indicate start of block followed by the starting page address, starting byte address, word count, up to 256 bytes of data and checksum in that order. Start and end memory locations are entered from TTY keyboard.
Memory Dump	Lists memory in octal: start and stop point user definable.
PROM Programmer for Intellec 8 Microcomputer Development System	Changes programmer from fixed timing to PROM dependent timing. Program 50% more than minimum required, ensuring permanency.
Data Transfer Routine	Transfer a block of data from any location in memory to another.
Move Routine	Moves a string with a specified length to a specified location in RAM.
Morse Code	Program receives message text typed on an ASR33 teletype and sends morse code equivalent to output port 10 bit 0. It contains a 256 character buffer so that text can be typed in faster than it is sent.
Binary Search Routine	Uses a binary search method to find a character in a table of characters.
Floating Point Math Package	Package contains subroutines for Addition, Subtraction, Multiplication, Division, Negate, Absolute Value, and Test of Floating Point Numbers.
Floating Point Format Conversion Package	Provides subroutines for conversion between floating point format and ASCII or BCD. Functions are: 1. Floating point to BCD conversion 2. BCD to floating point conversion 3. Floating point to fixed point (integer) conversion 4. Fixed point to floating point conversion
16-Bit Multiply	Multiplication of two 16-bit positive numbers giving a 32-bit result.
DECHL	Macro for decrementing the 16-bit binary contents of the H and L registers.
16-Bit Multiply	Performs 16-bit X 16-bit multiplication giving a 16-bit result.
SIMPY16	16-bit 2's complement signed multiply.
LOG2A	To calculate the Base 2 log of a number between 1 and 256.

TITLE	FUNCTION
Single Precision (8-bit) Multiply/Divide Subroutine	Five subroutines are provided: 1. 8-bit by 8-bit multiply for signed integers giving a 16-bit result 2. 8-bit by 8-bit multiply for unsigned integers giving a 16-bit result 3. 16-bit by 8-bit divide for signed integers giving an 8-bit result 4. 16-bit by 8-bit divide for unsigned integers giving an 8-bit result 5. 16-bit negate (2's complement)
DIV16	Performs a 16-bit X 16-bit division giving a 16-bit quotient and a 16-bit remainder.
BCD To/From Binary Conversion	Subroutines are provided for: 1. BCD to binary conversion 2. Binary to BCD conversion
Binary Multiplication	Multiplies two binary numbers: 1. Multiplicand: 24-bits 2. Multiplier: 1- to 24-bits
8080 I/O System Status Display	Display current I/O assignment information when invoked by the INTELLEC 8/MOD 80 MONITOR (Version 1.0).
Binary to BCD Routine	Converts binary value (1- to 24-bits) to its BCD value (1 to 8 digits).
BCD to Binary Routine	Converts BCD value (1 to 8 digits) to binary value (maximum 24 bits).
Match Game	A game to match a player against the processor in a test of logic.
Bit Masking Subroutine	Subroutines for changing 1 to 16 bits of a command word in RAM.
High Speed List	Permits use of a high speed printer with the Intellec 8 monitor (Version 1.0).
Read and Interrupt Modification	Allows printing of headings or operator instructions at the beginning of a Read Operation.
MPY16	Performs a 16-bit X 16-bit multiply giving a 16-bit result.
Binary to ASCII Digit Converter	Converts binary numbers to ASCII characters.
Gray to Binary Conversion	Converts up to 16 bits of cyclic Gray into binary data.
I/O Simulation Macros	I/O simulation macros for INTELLEC 8/MOD 80 systems allows simulation of input and output instruction based on an assembly time variable.
Tape Duplication	Duplicates a tape read in from the high speed tape reader by punching a copy on the TTY terminal with a leader added at both ends.
CRC GEN	Generate a 16 bit cyclic redundancy check (CRC) for a data string of up to 2^{16} bytes. The generator polynomial and initial conditions are defined by the user.
16 Bit CRC for polynomial X16+X12+X5+1 (polynomial for SDLC)	Produces a 16 bit CRC with 8 bit input bytes. Care should be taken with Most/Least bit feeding of the data byte and CRC residue. Does not require a table or contain any loops. Requires 24H memory locations and executes in 72.5 μsec.
CRC16	This macro calculates a CRC16 check word using the generation polynomial X**16+X**15+X**2+1. It can be used to generate a check word for a record that doesn't include one or to check that a record including a check word is correct.
CRECH	Computes CRC characters for IBM compatible floppy disk. Also works for Synchronous Data Link Control (SDLC).

TITLE	FUNCTION
Legible Paper Tape	The program punches legible characters on paper tape, useful for tape labeling.
Banner Print and Punch	Create, on a listing device or tape perforator, a graphic representation of certain ASCII characters.
Large Character Paper Tape Punch Program	The program will convert an inputted TTY ASCII character to a symbolic representation of that character on the paper tape. The program can also be called to output the ASCII character in the accumulator so the punch feature can be used by other programs such as monitors to print leaders, etc.
Page Listing Program	Provide facility for listing information in a paginated, numbered format. This is accomplished thru the system software with the console printer.
Source Paper Tape to Magnetic Cassette	Will copy a source paper tape onto a magnetic cassette. End statement must be followed by a carriage return. Program will ignore leading blanks.
I Command	This program loads HEX code into sequential RAM locations beginning at the address specified. It is useful for loading HEX machine code directly into RAM for corrections, debugging, execution, or PROM programming.
8080 RAM Memory Test	Memory test for Intellec 8/Mod 80 system
Memory Diagnostic Program	Writes test bytes in any range of memory and compares the written bit combination with what is read. Upon detection of a defective memory location, an error message is printed specifying the address, reference and actual values.
Compare Object Code Tape with Memory	This program extends the Intellec 8 system monitor's "Compare" command to check the data from a HEX format tape against the current information stored in memory.
K, Program Trap	This program provides tow traps (search/wait) for debugging other programs which use RAM memory. Displays the contents of five registers and the trap address when the trap occurs.
DEBUG	A two PROM debugging package to be used in minimum 8080 systems to inspect, dump, move and find data in memory.
Punch Test or TTY Reader/Punch Test	(1) Tests paper tape (using high speed or TTY reader), (2) complete TTY reader/punch test.
Reader Test	Test high speed paper tape reader or TTY reader.
TALLEY R2050 HSPTR Driver	Extension to the Intel 8080 monitor to handle a TALLY model R2050 photoelectric tape reader at 200 cps.
TALLY	Allows Tally 2200 line printer to be used in the assembly stage of programming with Intellec 8/Mod 80.
Model 101 Centronics Printer Handler	Accepts character output for Model 101 Centronics printer from assembler or other source. Buffers print characters in RAM performing TTY compatible operations with control characters. Causes line to be printed upon receipt of line feed. Counts lines and keeps track of pagination. Inserts title at top of each page.
High Speed Paper Tape Reader with Stepper Motor Control	This circuit and program allow paper tape to be read at approximately 150 characters per second. The reader is assigned by monitor command "AR=1". The program uses electronic damping, under software control, of a stepper motor to increase stepping speed and precision.
Terminal Editor	Procedure for controlling an ASR733 Texas Instruments terminal equipped with RDC (remote control device) option. Search a line in a file contained in cassette 1 with or without copying on cassette 2. The procedure is linked to the Intellec monitor.

TITLE	FUNCTION
Intellec 8/Mod 80-Silent 700 Interface	Interface TI Silent 700 to Mod 80.
Interrupt Service Routine	Handles multiple-level interrupts, saving all registers and flags and outputting the status of the current interrupt to an external status latch.
Interrupt Handler Re-entrant	On processor receipt of an interrupt instruction (RST 0–7), this program saves the machine state and previous interrupt level on the stack, transmits the new service level to the interrupt control unit (ICU), executes a subroutine corresponding to the level interrupt received, then restores the machine and ICU to their pre-interrupt state before resuming executing the interrupted program.
8008 Disassembler	This program is used to obtain an assembly language listing of a machine coded program in memory.
8080 Dis-Assembler	This program inputs a HEX tape and generates a symbolic assembly language program suitable for modifications and/or assembling.
DISASM (8080 Disassembler)	DISASM is intended as a software development and debugging aid. Operating on resident object code, it produces an assembly language equivalent which is printed on a TTY terminal. In its present form, the program starts at a given memory address and steps sequentially through memory until manually halted.
BINLB – 8080 System Loader	Loads HEX format paper tape produced by macro assembler on GE Timesharing into 8080 system. Also provides TTY input and output subroutines. BINLD can also produce a binary dump of itself for bootstrap loading.
Boot	To allow for bootstrap loading of program and for patching of programs or data in memory via the teletype. The program uses less than 200 bytes of memory and may be placed in ROM or entered manually.
Octal PROM Programming	This program accepts sets of 3 octal numbers. The fourth character (unless it is a rubout) will cause the BYTES to be placed in memory starting at 100H. Any invalid octal character input in the first 3 positions will cause a carriage return and line feed to be output to the teletype and the line to be ignored. Any number of sets may be input (up to the practical limit of 100H). Whenever a "bell" is typed, the address of the last valid byte on Page 1 will be displayed on the register/flag lights and control will pass to the system monitor. To program the PROM, type P100, 1NN, 0 where NN is the HEX number displayed on the lights.
8080 IDLE Analyzer for Approximating CPU Utilization	Displays amount of time 8080 would have spent in an idle loop. When RUN time is compared with idle time, the percent of CPU utilization can be calculated. Time display is in memory, in ASCII.
Real Time Executive	Performs processor initialization, period and demand scheduling, routine termination, and waits during idle time.
Read/write Routines for Interchange Tapes	Subroutines read and write blocks and characters for any common audio cassette recorder. Variable redundancy allows high-speed or highly reliable operation.
Proportional Power Control Image Builder	This program builds an "ON-OFF" image in RAM to allow proportional power control using zero crossing solid state relays.
Flag Processing Routine	A routine for contact closure debounding and processing.
Software Stack Routines for 8008	Subroutines provided for PUSH, POP and EXCHange A with top of stack, and to save processor state on stack in case of an interrupt, and to restore it again.
Symbol Table List Routine	This program will print the user's symbols in alphabetical order followed by the address the 8008 Macro Assembler has assigned to each symbol.

TITLE	FUNCTION
Digital to Analog Conversion for Eight Outputs	The program processes a list of eight 16 bit values to generate eight pulse width modulated voltages which can be filtered to provide inexpensive digital to analog conversion useful for process control or other low speed requirements.
Binary to HEX Routine	To read a paper tape in binary (EBCDIC) format from the Intel high speed paper tape reader to the MCS-80 system.
Binary to BCD Subroutine	Converts unsigned binary number in D, E to 5 BCD digits.
HEX to decimal conversion	Converts any HEX number between 0 and FFFFH to the decimal equivalent.
"VALUE" ASCII to HEX check and convert routine	Using routines already available in the Intellec 8/Mod 80 monitor, "VALUE", when called will get an ASCII character from the assigned console device, check it for a valid hex digit and convert it to a four bit memory value which is returned in the ACCumulator.
BCD input and direct conversion to binary routine	Fast and efficient BCD to binary conversion code. Presented in pseudo subroutine form for implementation in ROM to allow reading of BCD input value, conversion to binary representation and branching based on loading H & L registers to PC.
BINDECBIN	Converts hex numbers input on TTY to decimal numbers and vice versa. Decimal numbers must be ended with D, hexadecimals with H. Conversion begins with space. If first character input is CR, control is given back to monitor. Largest number handled is two bytes binary.
MATH	Includes routines for fixed and floating point arithmetic together with a demonstration program that performs algebraic evaluation and allows unlimited parentheses nesting. An expression within parentheses can be evaluated and displayed by "=" and is preserved as a subtotal, etc.
Elementary Function Package	Calculates floating point: square root logarithm exponential function sine cosine arc tangent hyperbolic sine hyperbolic cosine
8080 Foating Point Package with BCD Conversion Routine	Performs floating addition, subtraction, multiplication, division, fixing, floating, negation, and conversion from floating point to BCD with exponent.
8080 Least Squares Quadratic Fitting Routine	Performs summations and matrix manipulation for fitting up to 256 floating point X-Y pairs to a function of the form: $aX^2 + bX + c = Y$
Floating point procedures	Dummy PL/M interface procedures.
PL/M floating point interface	Interfaces PL/M conventions with floating point assembler format.
Floating point decimal & HEX format conversion	The program converts a number of 27 characters maximum to standard 13 digit decimal format and to floating point accumulator form in HEX format on the teletype.
N-byte Binary Multiplication and leading zero blanking	The program performs binary multiplication on two numbers and returns a result that may be up to 255 bytes in length.
Subroutine DEMULT	To multiply M decimal digits by N decimal digits and store the product (7 digits x 3 digits as written, but easy to expand as required.)

TITLE	FUNCTION
BCD Multiplication	Multiplies up to a 6 digit BCD number by a 4 digit BCD number, providing a 10 digit BCD result. All numbers are unsigned.
MUL/DIV multi-precision pack for 8080	Signed fixed-point binary fraction multiply and divide. Double-precision inputs, double-precision output for divide and 4-byte output for multiply.
Double precision multiply	To multiply two 16-bit numbers, returning the most significant 16 bits (in address form) thru the appropriate registers to the calling program.
16 Bit Square Root Routine	Return 16 bit square root (8 bit whole number joined with 8 bit fraction) of a 16 bit argument. The result conforms to standard signed number convention; therefore, its highest order bit will always be zero. The argument must have zeros in its two highest order bits, for its square root to lie in the valid range of the signed result.
Floating Point Square Root	Math & numerical Manipulation Programs. Operations performed are: test for negative argument (overflow set and return) computation of the square root for positive arguments
SQRTF	Generates 8 bit root of 16 bit number.
Subroutine SQRT	This subroutine takes the square root of a number in floating point notation.
Fast Floating Point Square Root Routine	Calculate square root of a floating point number by Heron's method. Execution time less than 50 ms for any number.
Natural logarithm	Computes the natural logarithm of a number between 1 and 65535.
Subroutine LOG	This subroutine takes the log to any integer base of any positive floating point number.
Approximating Routine	To solve functions such as the log, the antilog, the sine and the tangent function. The program given is set up to solve the antilog (base 2) function.
Sin X, Cos X Subroutines	Generates sine or cosine accurate to 8 bits of an input angle that is accurate to 8 bits. Uses a Chebyshev Economization of Taylor Series for Cosine X. Sine X is generated by complementing the angle X with respect to 90° ($x' = 90^{\circ} - X$) and then taking Cosine X.
RMSTF	To calculate the integration "T" of any continuous function "F(x)" between two limits "a" and "b".
Binary search	Program searches a table of up to 128 entries. Each entry is composed of a 1 byte argument (Search Key) and an associated result. The result field may be up to 255 bytes for each argument. Result fields must all be the same length.
Random Number Generator Subroutine	Subroutine to generate a random number between 0 and 177_8 (125^{10}).
8-bit Pseudo Random Number Generator	The program reads data from page 0, address FF and generates a random number. The new number is written back in the same location. All numbers except zero are generated. Zero is a disallowed state and is corrected in the program.
16-bit Random Number Generator	The subroutine implements a linear congruential sequence which generates 16-bit random numbers. The random numbers produced range from 0000 to FFFF with a period less than or equivalent to 2 ** 16. An 8-bit random number is available as the upper byte of the 16-bit random number. X(N+1) = (2053*X(N) + 13849)mod 2**16

TITLE	FUNCTION
PL/M Histogram Procedure and Random Number Generator	Main program generates an 8-bit shift register sequence by XORing the first and last bits and shifting the result into the next random numbers bottom bit. 1000 numbers are generated and then histogramed. Histogram procedure sets up an output histogram array and then prints the histogram on the TTY when commanded after printing. The array is not zeroed so that intermediate results may be displayed without effect on the final histogram.
RANDOM$BITS	A Non-multiplicative pseudo-random number generator.
Clock Subroutine	Maintains a current time of day, decimal adjusted in BCD, of hours, minutes, and seconds. Must be invoked once each second, usually by an external interrupt. Time is stored in three bytes of memory, in the 24-hour system or optically in the 12-hour system.
Interrupt Driven Clock Routine	Updating of clock located in RAM based on 100 ms time intervals. Pulses arriving on interrupt line. Four storage locations reserved for 100 ms counter, secs counter, mins counter and hour counter. One location for interval counter one for preset interval and one for flag indicating interval has elapsed. Updating of clock takes about 70 microsecs.
Calendar Subroutine	Uses three bytes of RAM to store the current date arranged as two BCD digits per byte. The date is adjusted for months with 28, 29, 30 or 31 days and February is adjusted for leap years 1976, 1980 and 1984.
PASS	Program PASS transfers addresses of parameters between a calling program and subroutine.
Address	Subroutines for dynamic memory allocation and addressing.
Data Array Move	A contiguous array of data may be relocated in memory, regardless of the magnitude and direction of the move. The source and destination array locations may overlap. The maximum array size is 2^{16} bytes.
Shellsort	Sorts arrays in place using Shell's method of diminishing increment.
Text Storage Program	Allows text to be stored in memory using a letter of the alphabet as a pointer. After the message is stored, it can be retrieved by depressing a single key on the TTY. Up to 32 messages may be stored and retrieved independently.
Time Sharing Communications	To communicate with medium to large scale computer systems as an external time-share user.
A Generalized Stepper Motor Driver Program	Operations performed by the program are: using entry variables of number of steps, clockwise or counterclockwise direction and speed of steps — several programs are illustrated for moving a stepper motor in either direction then stopping, moving N steps forward then return N steps, moving motor continuously in either direction until interrupted by a TTY keyboard entry, also programs using an LED-photodetector sensor for absolute motor position.

8-BIT

CROSS PRODUCTS

Cross Assembler for HP2100
Cross Assembler for PDP-11
Macro Assembler for PDP-11
Absolute Loader for PDP-11 LDA Tape Format
8008 Macro Definition Set for Assembly on PDP-11
8080 Macro Definition Set for Assembly on PDP-11
8080 Cross Compiler on PDP-11
Cross Assembler for PDP-11
Cross Assembler for Nova 1200
Cross Assembler for Nova 1220, IBM 360/40 and CDC3300
Nova Cross Assembler for Intel 8080
Cross Assembler for Nova
Intel 8008 Cross Inverse Assembler for HP 2100
8080 Cross Assembler for HP 2100 DOS
8008 Cross Assembler for HP 3000
8080 Cross Assembler for HP 3000
PL/M 80 Pass 3

GAMES

NIM
NIM
Blackjack
The Word Game
Gambol
Mastermind
Maze
Game of Life
Numbers
Kalah
An Adaptive Game Program
Match Game

MICROCOMPUTER USER'S LIBRARY SUBMITTAL FORM

☐ 4004 ☐ 4040 ☐ 8008 ☐ 8080 ☐ 3000 (use additional sheets if necessary)

Program Title

Function

Required Hardware

Required Software

Input Parameters

Output Results

Registers Modified:	**Assembler/Compiler Used:**
RAM Required:	**Programmer:**
ROM Required:	**Company:**
Maximum Subroutine Nesting Level:	**Address:**

INSTRUCTIONS FOR PROGRAM SUBMITTAL TO MCS USER'S LIBRARY

1. Complete Submittal Form as follows: (Please print or type)
   a. Processor (check appropriate box)
   b. Program title: Name or brief description of program function
   c. Function: Detailed description of operations performed by the program
   d. Required hardware:
      For example: TTY on port 0 and 1
      Interrupt circuitry
      I/O Interface
      Machine line and configuration for cross products
   e. Required software:
      For example: TTY routine
      Floating point package
      Support software required for cross products
   f. Input parameters: Description of register values, memory areas or values accepted from input ports
   g. Output results: Values to be expected in registers, memory areas or on output ports
   h. Program details (for resident products only)
      1. Registers modified
      2. RAM required (bytes)
      3. ROM required (bytes)
      4. Maximum subroutine nesting level
   i. Assembler/Compiler Used:
      For example: PL/M
      Intellec 8 Macro Assembler
      IBM 370 Fortran IV
   j. Programmer, company and address

2. A source listing of the program must be included. This should be the output listing of a compile or assembly, Extra information such as symbol table or code dumps is not necessary.

3. A test program which assures the validity of the contributed program must be included. This is for the user's verification after he has transcribed and assembled the program in question.

4. A source paper tape of the contributed program is required. This insures that a clear, original copy of the program is available to photo-copy for publication in a User's Library update publication.

Send completed documentation to:

Intel Corporation
User's Library
Microcomputer Systems
3065 Bowers Avenue
Santa Clara, California 95051

intel

MICROCOMPUTER TRAINING
MICROCOMPUTER WORKSHOPS

Microcomputers are being used in hundreds of applications from simple controllers to complex data processing systems. To enable users to bring microcomputers into their applications, Intel is offering a selection of 3 and 4 day workshops that are designed to provide you with the "tools" for making optimum use of Intel microcomputers in system development.

PREREQUISITES: To attain benefit from course presentation, some background in logic design and a basic knowledge of programming is necessary.

ATTENDANCE: Attendance is limited to (15) enrollees.

TUITION: The fee for each workshop is $350, which includes course materials, computer time, and luncheons.

SCHEDULE: These workshops are scheduled to be held at Intel Corporation Training Centers in Santa Clara, CA and Boston, MA.

REGISTRATION: Contact your Intel Sales Office for details.

MCS-80/ICE-80 WORKSHOP

COURSE OBJECTIVE: This workshop will prepare the student to design and develop a system using the Intel® 8080 microprocessor through the use of lecture, demonstration, and laboratory "hands-on" experience with the Intellec MDS development system and ICE-80.

COURSE OUTLINE:

DAY 1

Introduction
- a. Microprocessor System Fundamentals Function/Organization/ Programming
- b. Introduction to the 8080
  1. Basic System
     - a) CPU
     - b) Memory
     - c) Input/Output: (Programmed/Interrupt/DMA)
  2. Programming Model
- c. Languages
  1. Machine Code
  2. Assembly Language
  3. PL/M

Instructions
- a. Input/Output
- b. Register/Memory Reference
- c. Control/Arithmetic

The Intellec MDS
- a. Function/Operation
- b. System Monitor

The Text Editor
- a. Structure/Commands
- b. Operation

Laboratory
- a. Using the System Monitor
- b. Using the Text Editor

DAY 2

The Macro Assembler
- a. Syntax/Pseudo-Instructions
- b. Operation

System Timing
- a. Instruction
- b. Clock
- c. Address/Data

Input/Output Programming

Subroutines
- a. Invocation
- b. Stack Memory
- c. Parameter Passing

Teletype Programming Requirements

The Interrupt System
- a. Definition
- b. RST Instruction
- c. Service Subroutines

Laboratory
- a. Using the Assembler
- b. Program Assembly and Execution

DAY 3

Branch Table
- a. Application
- b. Construction

Direct Load/Store Instructions

System Monitor Debugging Function

System Design Process
- a. Memory and I/O Requirements
- b. Bus Control
- c. Clocks
- d. Hardware/Software Trade-offs

Additional Development Aids

Laboratory
- a. Program Assembly and Execution
- b. PROM Programming

DAY 4

What is "In Circuit Emulation"

ICE-80 Description
- a. Functional Block Diagram
- b. Theory of Operation

ICE-80 Laboratory
- a. Operating the ICE-80
- b. Emulating an 8080 Based System

PL/M LANGUAGE WORKSHOP

COURSE OBJECTIVE: This workshop will prepare the student for writing and debugging PL/M programs using lecture, demonstration, and laboratory "hands-on" experience in operating PL/M interactively from a high-speed, time-shared computer terminal.

COURSE OUTLINE:

DAY 1

Introduction
a. Overview of PL/M
b. Preview of Course

Definitions
a. Symbols
b. Identifiers
c. Reserved Words
d. Comments
e. Data Elements
f. Expressions
g. Statements
h. Declarations

Data Elements
a. Variables
b. Subscripted Variables
c. Data Type
d. Constants

Operators, Operations and Priorities
a. Arithmetic
b. Boolean

Evaluating Expressions Statements
a. Redefine
b. Basic
c. Conditional

Blocks
a. Concept and Use
b. Scope of Declarations
   1. Global and Local
   2. Nested and Parallel Blocks

Laboratory
a. Introduction to Data Terminal and Timesharing
b. Compiling a PL/M Program

Assignment
Sample Problem to Flowchart and Program Outside Class

DAY 2

Review
Procedures
a. Declaration
b. Invocation
c. Program Construction

Data References
Statement Labels
Unconditional Transfers
Compile-Time Macro Processing
Input/Output Processing
Simulating an 8080 System
Laboratory
a. Compile Programs
b. Execute Programs

DAY 3

Review
Memory Mapping
Assembly Language Interface
Interrupt Processing
Predeclared Variables and Procedures
a. LENGTH and LAST
b. Condition Code
c. Memory Vector
d. TIME Procedure
e. Type Transfer
f. Decimal Arithmetic
g. Shifts and Rotates

Laboratory
a. Compile Programs
b. Execute Programs

SERIES 3000 WORKSHOP

COURSE OBJECTIVE: This workshop will provide the student with an in-depth understanding of the Series 3000 family through the use of lecture and demonstration. Microprogramming and design examples are presented.

COURSE OUTLINE:

DAY 1

Introduction
a. Introduction to Microprogramming
b. The Series 3000 Component Family
c. Series 3000 System Overview

CPU Design Example
a. CPU System Requirements
b. Architecture of a CPU
c. Developing a Macro-instruction Set
d. Interrupt Handling
e. Microprogram Mapping

DAY 2

Design Techniques
a. Conditional Clocking
b. K-Bus
c. Micro-instruction Field Extension
d. Micro-subroutines
e. Pipelining
f. Timing Analysis

Controller Design Example
a. Disc Controller System Requirements
b. Architecture of a Disc Controller
c. Microprogram Implementation

DAY 3

Development Support
a. Introduction to CROMIS, the Series 3000 Cross Micro-Assembler
b. MDS-800 Microcomputer Development System
c. ICE-30 In-Circuit Emulator
d. ROM Simulator
e. Demonstration

MCS-4/40 WORKSHOP

COURSE OBJECTIVE: This workshop will prepare the student to design and develop systems using the Intel® 4040 and 4004 through the use of lecture, demonstration, and laboratory "hands-on" experience with the Intellec 4 MOD 40 development system.

COURSE OUTLINE:

DAY 1

Introduction
a. Basic Microcomputer Block Diagram
   1. Function
   2. Uses
b. MCS-40 Block Diagram
   1. CPU – 4004/4040
   2. Memory – 4001, 4002, 4308, 4289
   3. I/O – 4207, 4209, 4211, 4003

Basic System Timing
Description of Major Elements of CPU
MCS-40 Instructions
a. Basic Machine Instructions
b. Accumulator Group Instructions
c. I/O and RAM Instructions
d. 4040 Group Instructions

MCS-40 Assembler
a. Syntax
b. I/O Formats
c. Coding Examples

Laboratory – Intellec 40 Operation
a. Control Console Use
b. TTY Input
c. High-Speed Reader Operation

Homework Utilizing Assembler Language to Code Sample Programs

DAY 2

Review Sample Programs
The Interrupt System
a. Definition
b. Instructions
c. Service Subroutines

System Monitor Description
System Development Aids
a. Intellec 4 MOD 40
b. Cross Assemblers
c. User's Library

System Interrelation
a. Connections
   1. Hardware
   2. Software
b. ROM/RAM Configurations
c. Interface Design
d. MCS-40 Family Components

Sample System Design
Laboratory
a. Using the Assembler
b. Debug Using System Monitor and Console

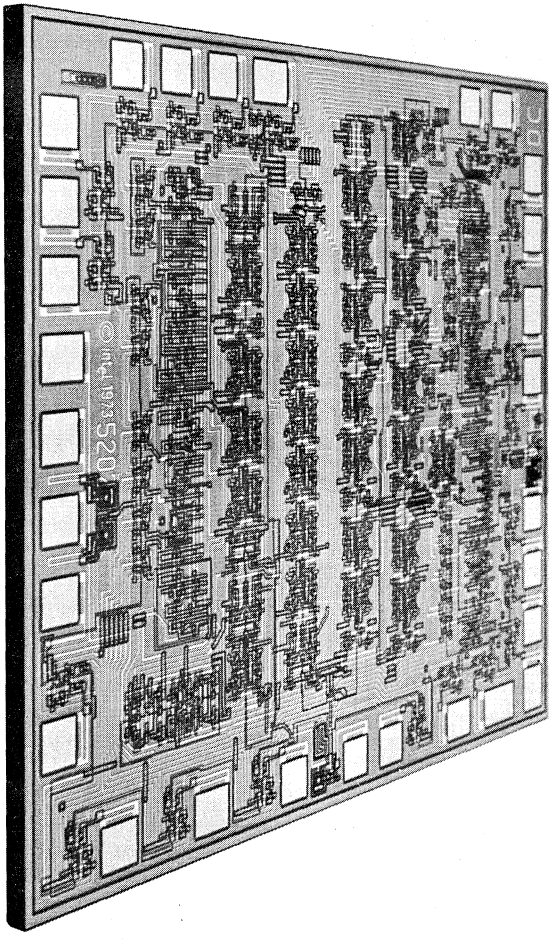
DAY 3

Review System Design
Hardware/Software Trade-offs
Laboratory
a. Hands-On Programming Time
b. PROM Programming

Summary and Course Review

11

TIMEKEEPING CIRCUITS



SINGLE CHIP LCD TIME/SECONDS/DATE WATCH CIRCUIT

- **On Chip Voltage Multiplier Provides 4.5V For Driving 3½ Digit Field Effect Display**
- **Only Two Switches Required For Complete Operation Of The Watch**
- **Operates With 32.768 kHz Quartz Crystal**
- **Anti-Bounce Protection On Switch Inputs**
- **AM/PM Indication When Setting Time**

The 5810A is a low power timekeeping circuit intended for use with 7 segment, 3-1/2 digit field effect liquid crystal displays. All of the circuitry required in a Time/Seconds/Date watch is contained on this single chip.

An on-chip voltage multiplier is incorporated on the 5810A. The multiplier derives a 4 to 4.8 volt display drive supply from the 1.5 volt battery. This multiplier requires only three external capacitors.

The 5810A, in conjunction with an external quartz crystal and trimmer capacitor, oscillates at 32.768 kHz, divides down and decodes Seconds, Minutes, Hours, and Date of Month.

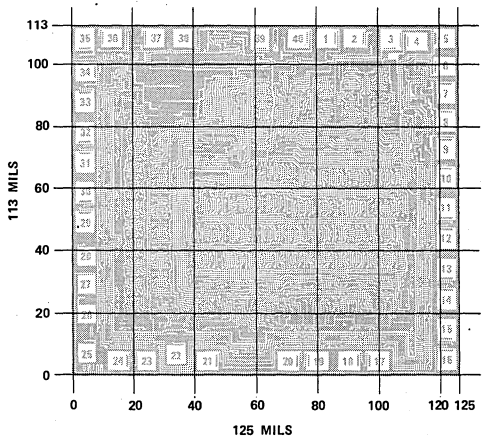
The 5810A will normally display Hours and Minutes. Closure of the D/C command switch will cause Seconds to be displayed in the Minutes position and the Hours will be blanked. A second closure of the D/C command switch will cause the Date to be displayed in the Minutes position and Hours to be blanked. A third closure of the D/C command switch will cause a return to the normal mode displaying Hours and Minutes. Switch S is used in conjunction with switch D/C for timesetting operations (see page 11-4 for description of operation). Thus only two switches are required for complete operation of the watch.

The colon is flashed at a 1Hz rate in all three display modes.

To facilitate testing and calibration a fast test input, reset and oscillator calibrate output are provided. These functions are described on page 11-4.

The 5810A is manufactured with complementary silicon gate MOS. This extremely low power technology is ideally suited for the manufacture of devices designed to operate on small batteries for long periods of time.

CHIP TOPOGRAPHY



PAD ASSIGNMENT

1. D/C	21. B3
2. S	22. Fast Test
3. VDD	23. C3
4. GND	24. D3
5. Cap 1	25. E3
6. Cap 1	26. C2
7. Cap 2	27. A2 + D2
8. Cap 2	28. E2
9. VTT	29. L
10. G1	30. C1
11. F1	31. D1
12. A1	32. E1
13. B1	33. K
14. G2	34. Common
15. F2	35. Calibrate Out
16. A2 + D2	36. Oscillator Cap 1
17. B2	37. Oscillator Cap 2
18. G3	38. Oscillator Out
19. F3	39. Oscillator In
20. A3	40. Reset

Absolute Maximum Ratings*

Temperature Under Bias ..... −20°C to +70°C
Storage Temperature ..... −40°C to +125°C
Supply Voltage V_{DD} with respect to GND ..... -8.0V to +0.3V
Voltage on all Inputs or Outputs with respect to GND ..... V_{DD} -0.3V to +0.3V
Power Dissipation 100mW

COMMENT:

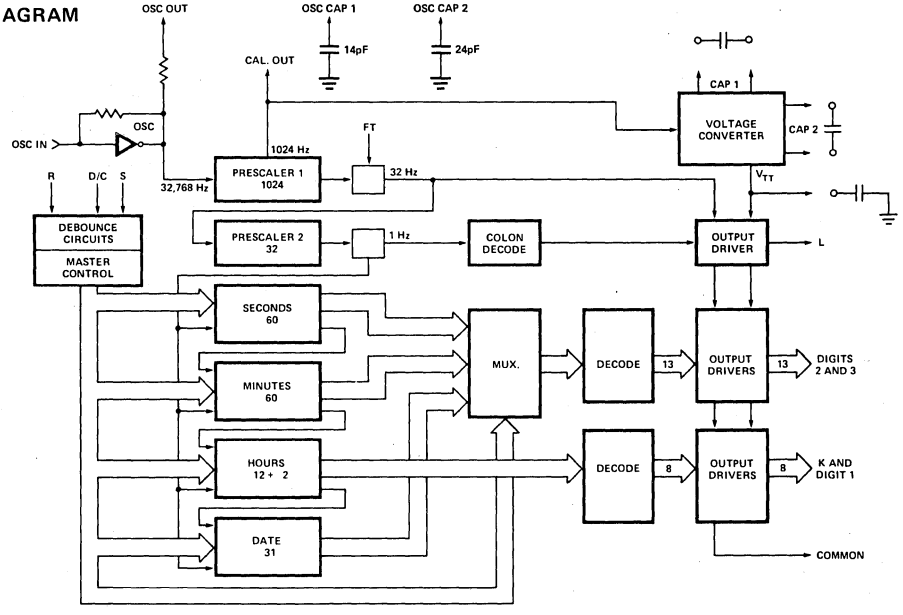
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

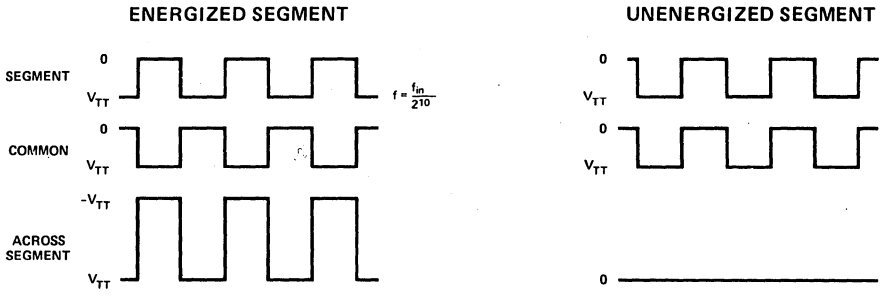
T_A = 25°C; V_{DD} = -1.6V; f_{OSC} = 32.768 kHz, Unless Otherwise Specified.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
I_{DD}	Total Average Internal Current		5	μA	No Output Load
			10	μA	1μA Output Load
V_{TT}	Multiplier Output Voltage		-4.8	V	I_{OUT} = 0.0μA
		-4.0		V	V_{DD} = 1.5V, I_{OUT} = 1.0μA
I_{IHS}	Switch Input High Current (D/C, S)		4	μA	V_{IN} = 0V
V_{IL}	Input Low Voltage	V_{DD}-0.3	V_{DD}+0.4	V	
V_{IH}	Input High Voltage	-0.3	0.3	V	
V_{DD} START	Minimum Oscillator Start Voltage	-1.4		V	
V_{DD} SUST	Minimum Oscillator Sustaining Voltage	-1.3		V	
V_{OLC}	Output Low Voltage Common		V_{TT}+0.1	V	V_{TT}=-4.0V; I_{OLC}=1.0μA
V_{OHC}	Output High Voltage Common	-0.1V		V	V_{TT}=-4.0V; I_{OHC}=-1.0μA
V_{OLS}	Output Low Voltage Segment		V_{TT}+0.1	V	V_{TT}=-4.0V; I_{OLS}=50nA
V_{OHS}	Output High Voltage Segment	-0.1V		V	V_{TT}=-4.0V; I_{OHS}=-50nA

BLOCK DIAGRAM

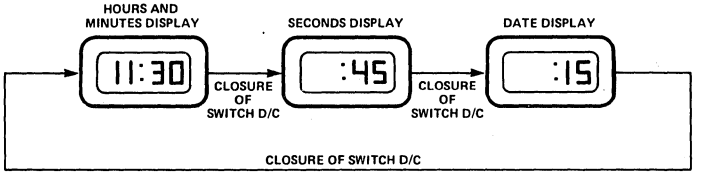


Output Waveforms



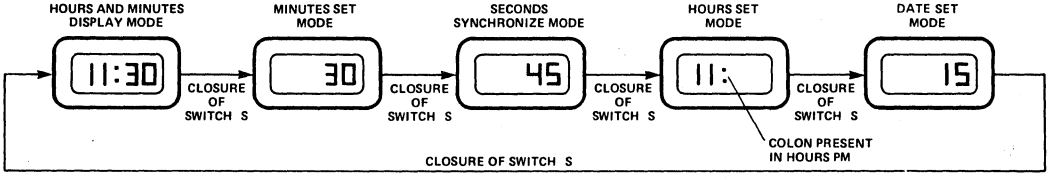
Time Display

Switch input D/C controls the time display modes. Each closure of switch D/C (D/C input = high) causes a change in the display mode in the sequence Hours and Minutes→Seconds→Date→Hours and Minutes. The following diagram illustrates this:



Time Setting

Switch input S controls the time setting modes. This switch input is active only when the circuit is in the Hours and Minutes display mode. Each closure of switch S (S input = high) causes a change in the time set modes in the sequence Hours and Minutes→Minutes→Seconds →Hours→Date→Hours and Minutes. *Closure of switch D/C when in the Minutes, Hours, or Date time set modes will cause that mode to be advanced at a 1 Hz rate. Closure of switch D/C in the Seconds synchronize mode will cause the Minutes to be advanced by one and the Seconds to be reset to zero and held until the D/C input is returned high.* The colon is displayed only in the Hours PM state in the time set mode. The following diagram illustrates this:



Reset

The reset input may be used to initialize all time counters to the zero state. All time counters are automatically reset to zero when voltage is initially applied to the circuit. The zero state is 12:00 AM, 00 Seconds, 0 Date.

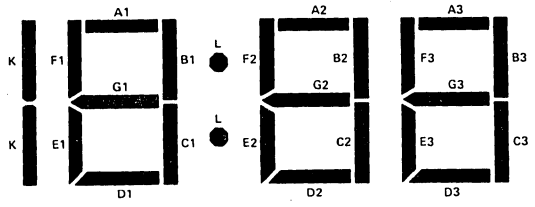
Fast Test

This input by-passes the oscillator stage and prescaler 1, allowing cycling of the counters at rates faster than real time.

Calibration Output

This output brings out the oscillator frequency divided by 32 and may be used for calibration of the oscillator.

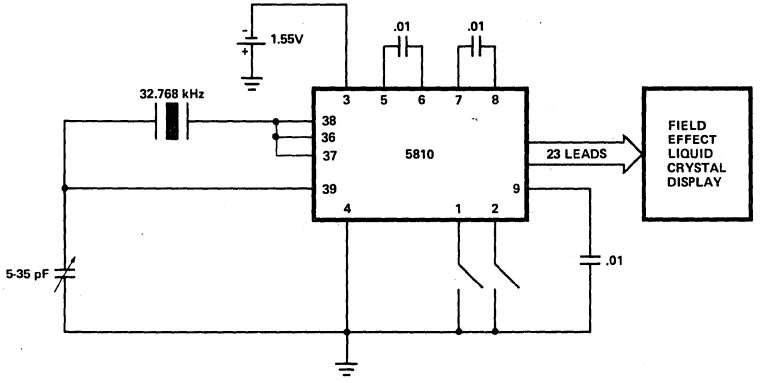
Display Segment Format



DIGITS D1, D2 AND D3 TRUTH TABLE

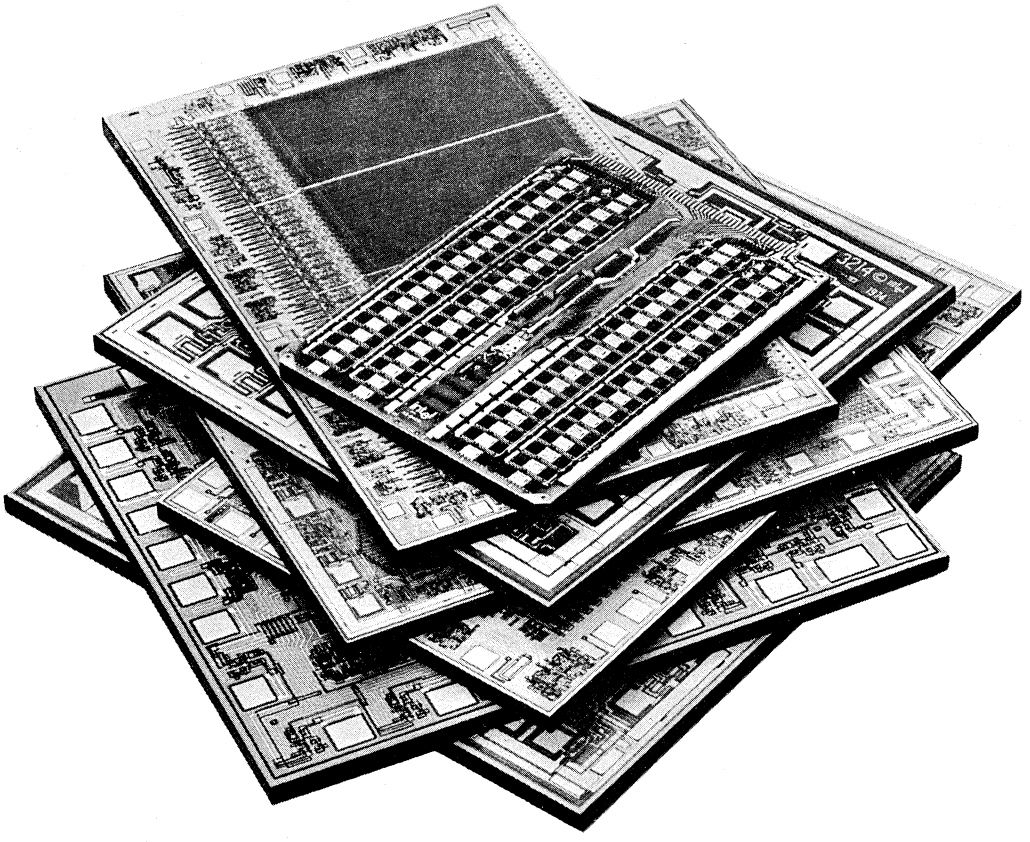
NUMBER	SEGMENTS						
	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Typical Application



12

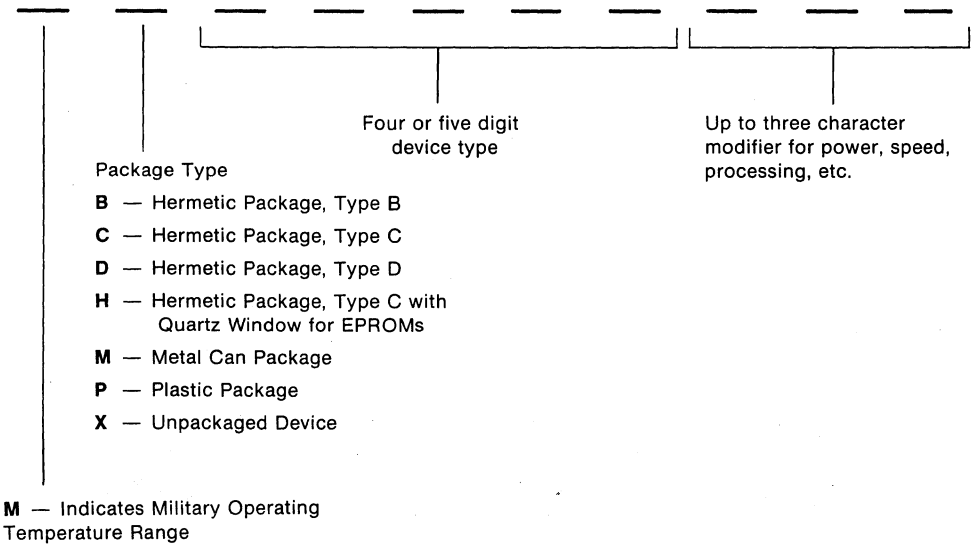
GENERAL INFORMATION



GENERAL INFORMATION

ORDERING INFORMATION

Semiconductor components are ordered as follows:



Examples

P5101L	CMOS 256 x 4 RAM, low power selection, plastic package, commercial temperature range
C8080A2	8080A Microprocessor with 1.5 μs cycle time, hermetic package Type C, commercial temperature range
MD3601/C	256 x 4 PROM, hermetic package Type D, military temperature range, MIL-STD-883 Level C processing*
MC8080A/B	8080A Microprocessor, hermetic package Type C, military temperature range, MIL-STD-883 Level B processing*

**On military temperature devices, the /B suffix indicates MIL-STD-883 Level B processing, suffix /C indicates MIL-STD-883 Level C processing.*

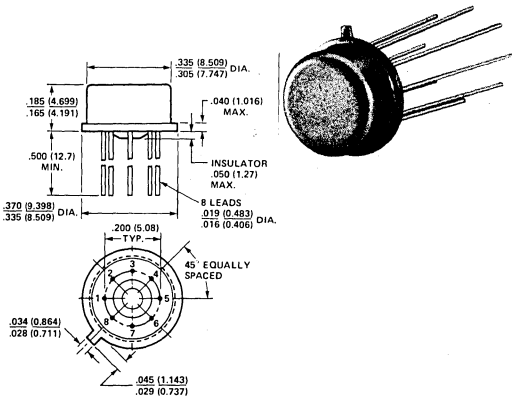
Systems boards, kits and software are ordered using designated part numbers as shown in this catalog.

The latest Intel price book should be consulted for availability of various options.

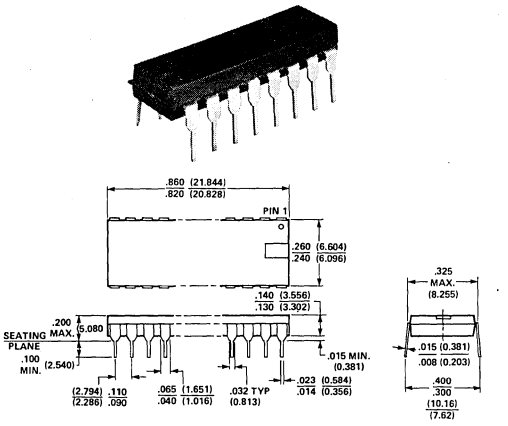
PACKAGING INFORMATION

Dimensions in inches
and (millimeters)

8-LEAD METAL CAN PACKAGE TYPE M



16-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



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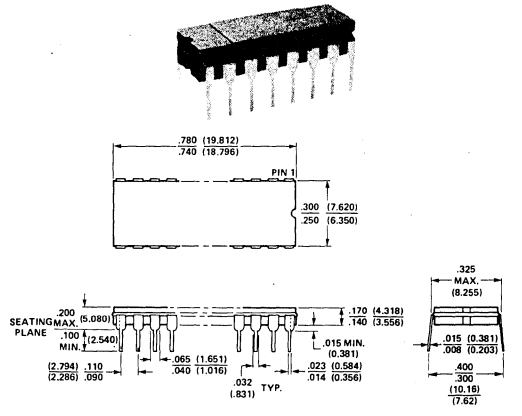

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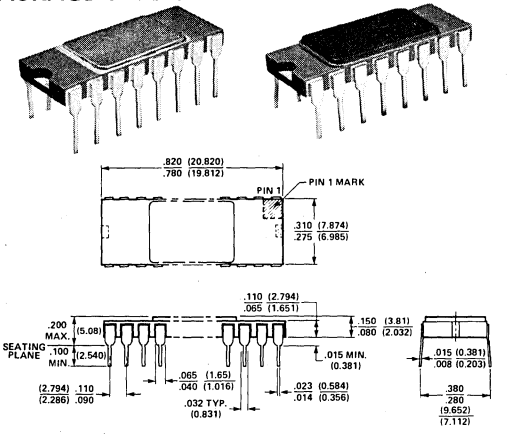

GENERAL INFORMATION

PACKAGING INFORMATION

Dimensions in inches
and (millimeters)

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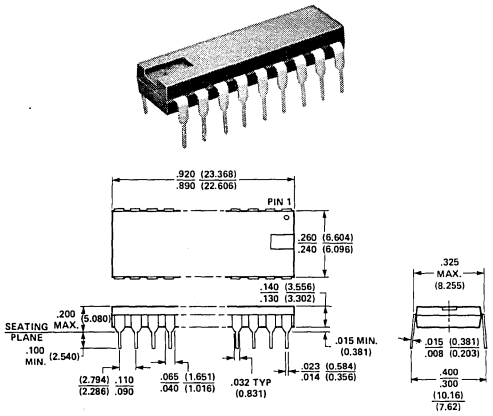

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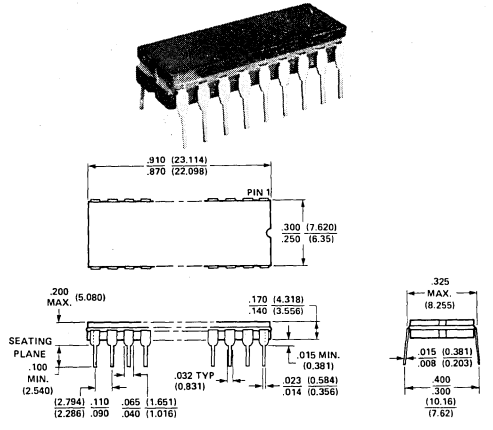

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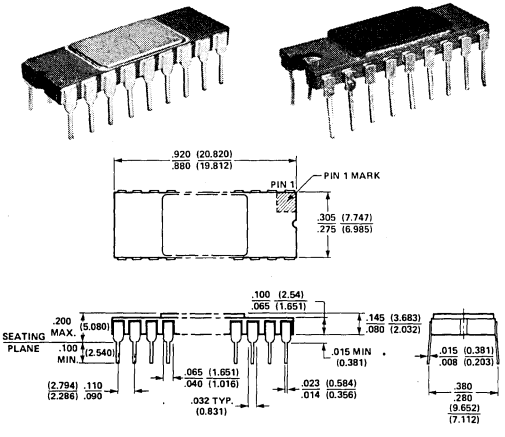

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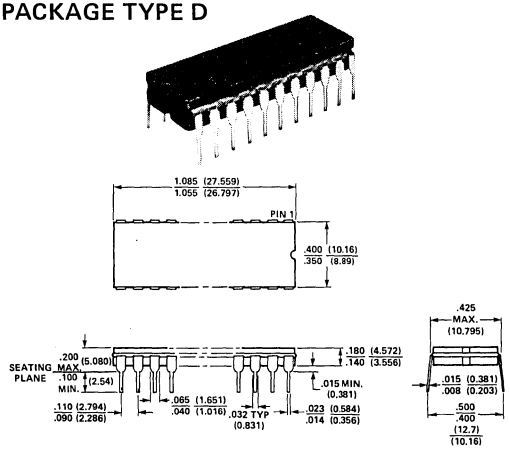

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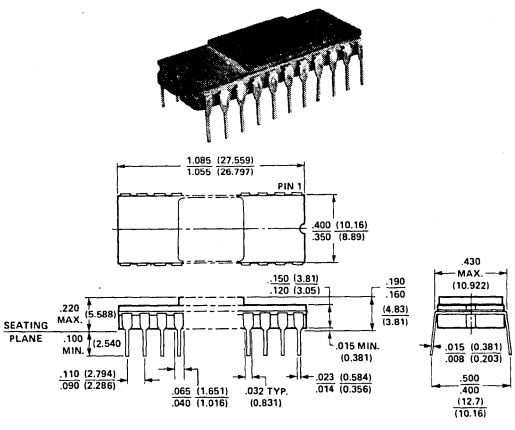

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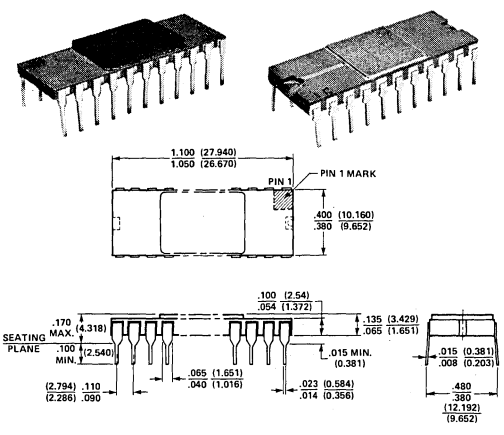

GENERAL INFORMATION

PACKAGING INFORMATION

Dimensions in inches
and (millimeters)

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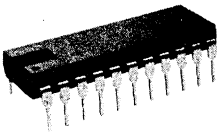

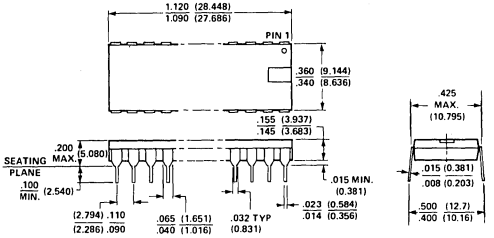

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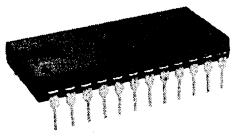

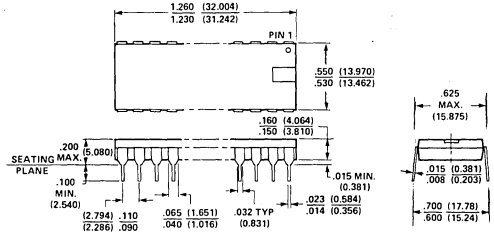

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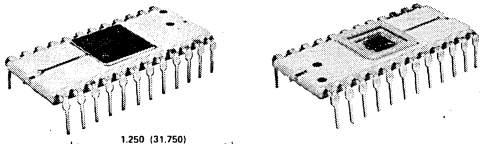
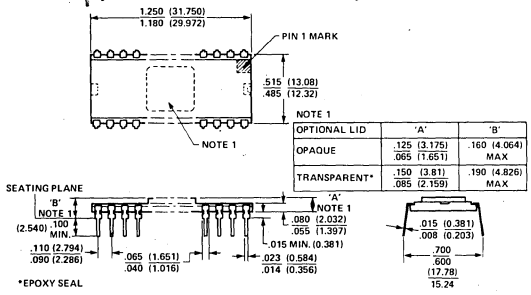
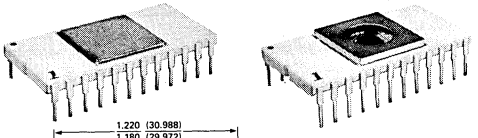
TYPE C

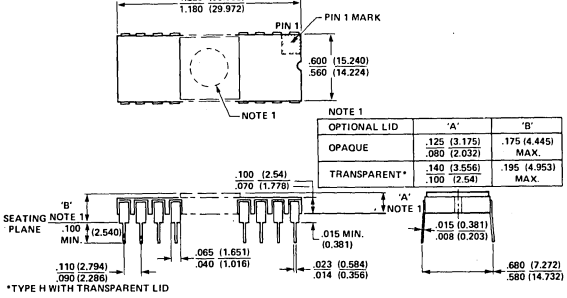




OPTIONAL LID	'A'	'B'
OPAQUE	.125 (3.175) / .065 (1.651)	.160 (4.064) MAX
TRANSPARENT*	.150 (3.81) / .085 (2.159)	.190 (4.826) MAX

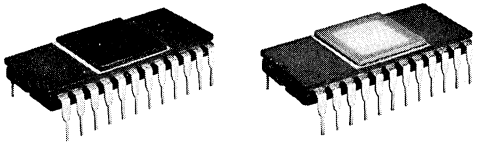
TYPE C OR H*

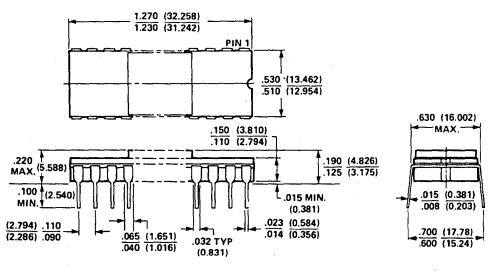




OPTIONAL LID	'A'	'B'
OPAQUE	.125 (3.175) / .080 (2.032)	.175 (4.445) MAX.
TRANSPARENT*	.140 (3.556) / .100 (2.54)	.195 (4.953) MAX.

24-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE B





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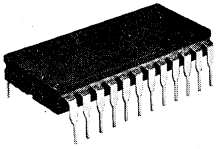
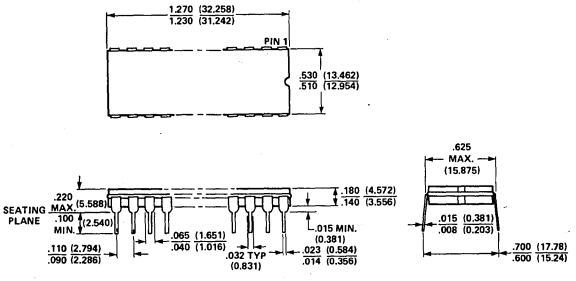


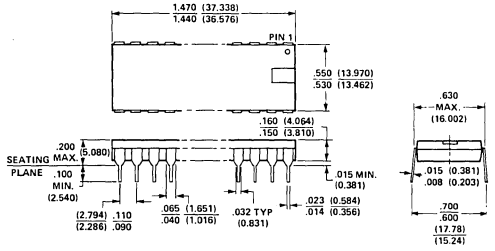


GENERAL INFORMATION

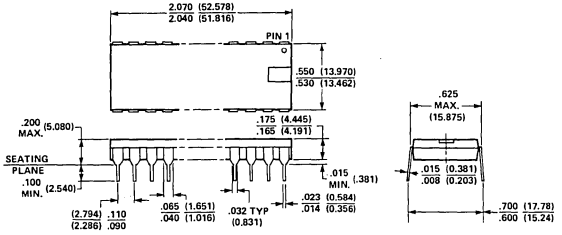
PACKAGING INFORMATION

Dimensions in inches
and (millimeters)

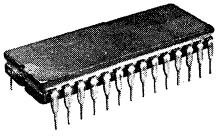
28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

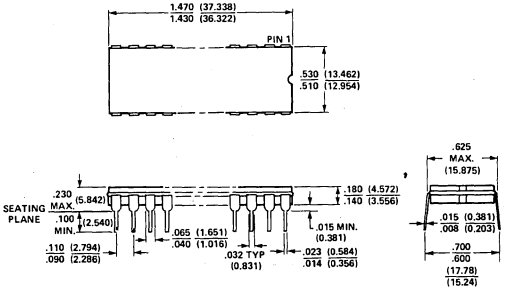


40-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

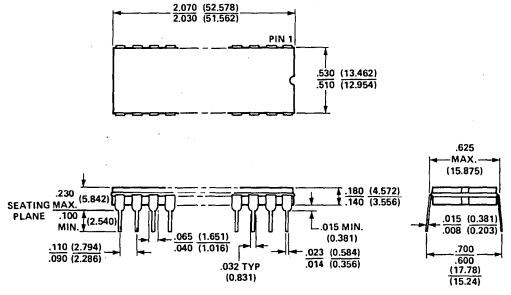


28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D





40-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



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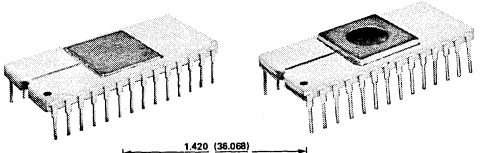
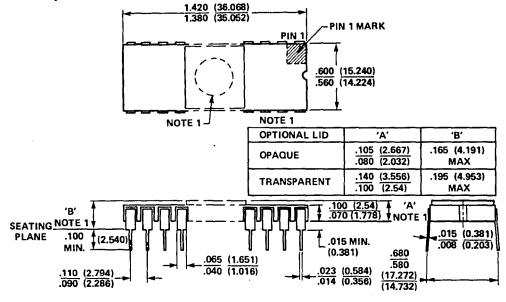
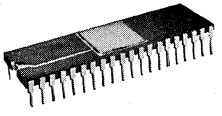
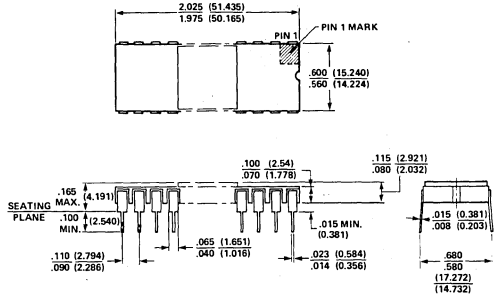




OPTIONAL LID	'A'	'B'
OPAQUE	.105 (2.667) .080 (2.032)	.165 (4.191) MAX
TRANSPARENT	.140 (3.556) .100 (2.54)	.195 (4.953) MAX

40-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE C

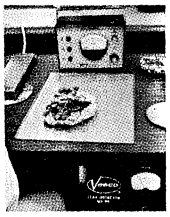




GENERAL INFORMATION

STANDARD PRODUCT PROCESSING AND 100% SCREENING —

Optical inspection criteria based on MIL-STD-883 Method 2010.1B to insure that all devices are free from internal defects which could lead to failure in normal applications. (Monitored by QA)

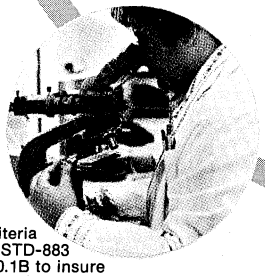


Hermeticity Testing to eliminate devices which show insufficient hermeticity. (Monitored by QA)
Fine leak C DIPs,CERDIPs,and Metal cans (MIL-STD-883 Method 1014A)* **Gross Leak** C DIPs and Cerdips only (Method 1014C; vacuum omitted and 2 hour pressurization).

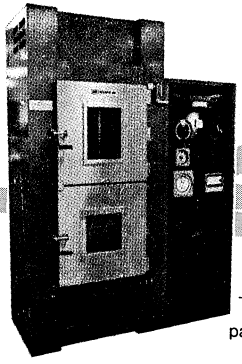
Die Attach
(Monitored by QA)

Lead Bonding (Monitored by QA per MIL-STD-883 Method 2011 Test Condition D.)

Metal Can
Pneupactor for constant acceleration and mechanical shock (15,000G for 0.5 msec) to insure that all devices are adequately die attached, bonded and free from package defects. (Not 100% screened. Monitored by QA)



Precap Visual Inspection criteria based on MIL-STD-883 Method 2010.1B to insure that after assembly all devices are free from defects which could lead to failure in normal applications. (Each lot must pass a QA acceptance.)



Temperature Cycling per MIL-STD-883 Method 1010 Test Condition C (10 Cy(−65°C to +150°C) to insure that all de\ are free from metalization, bonding or packaging defects. (Monitored by QA)

MIL-STD-883 100% screens for class B devices which are performed on a "Customer Special" basis are:

Stabilization Bake	(Method 1008)
Burn-in	(Method 1015, conditions A, B, or C)

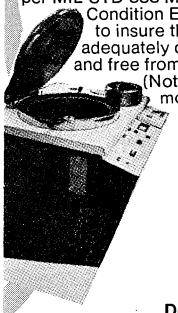
MIL-STD-883 Group A Electrical Tests of Method 5005 at maximum and minimum operating temperatures are performed on a "Customer Special" basis.

MIL-STD-883 Group B and C tests are performed periodically to provide generic data. Reprints of the reports on these tests are available from:

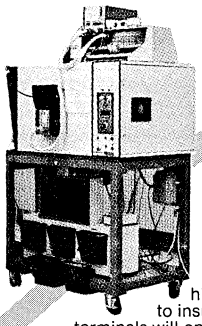
Product Marketing
Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051

COMPUTER GRADE PRODUCTS*

***Fine leak limits:** All devices: 5 x 10^{-7} cc/sec. Quartz lid devices are not tested.



Ceramic DIP and Cerdip Centrifuge for constant acceleration per MIL-STD-883 Method 2001 Test Condition E (30,000G Y1 plane) to insure that all devices are adequately die attached, bonded and free from package defects. (Not 100% screened; monitored by QA)



Continuity at high temperature to insure that no terminals will open or short at high temperatures. (Monitored by QA)

Plastic Deflash, trim and form leads. Back fill. (Monitored by QA)

Electrical Testing at 25°C to test conditions and limits which guarantee AC, DC and functional performance over full specified temperature range.

Final QA Acceptance per MIL-STD-883 Method 2009 External Visual, and Electrical AC, DC, Functional Tests at 25°C with correlated limits to guarantee performance over full specified temperature range (AQL 1%)

*Consumer Grade Products receive similar processing as applicable.

Intel provides a variety of brochures, users' manuals, and other literature. The list below includes the most popular publications available at the time of publication. If you wish to receive one of the listed documents or have specific requirements for more detailed information, contact your local distributor, sales office, or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051, Attention: Literature Department.

International locations also provide selected literature in Japanese, French or German.

Complimentary Information

BROCHURES

MCS-80™ Brochure
MCS-40™ Brochure
Intellec® MDS Brochure
MCS Users' Library Brochure
OEM Single Board Computer Brochure
Selection of best approach with 4K RAMs: 16, 18 or 22 pin.

REFERENCE CARDS

8080 Assembly Language reference card
8008 Assembly Language reference card
MCS-40 Assembly Language reference card

RELIABILITY REPORTS

RR-6 1702A Silicon Gate MOS 2K PROM
RR-7 2107A/2107B N-Channel Silicon Gate MOS 4K RAMs
RR-8 Polysilicon Fuse Bipolar PROMs
RR-9 Static MOS RAMs

Manuals and Handbooks

(Please enclose check or money order payable to Intel Corporation with your order)

	Price
Memory Design Handbook: The complete source of application information on RAMs, ROMs, Serial Memory and Support Circuits	$5.00
8080 Microcomputer Systems User's Manual	5.00
MCS-8 User's Manual	2.50
8080 Assembly Language Programming Manual	5.00
8008 Assembly Language Programming Manual	5.00
8008 and 8080 PL/M Programming Manual	5.00
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