Networking

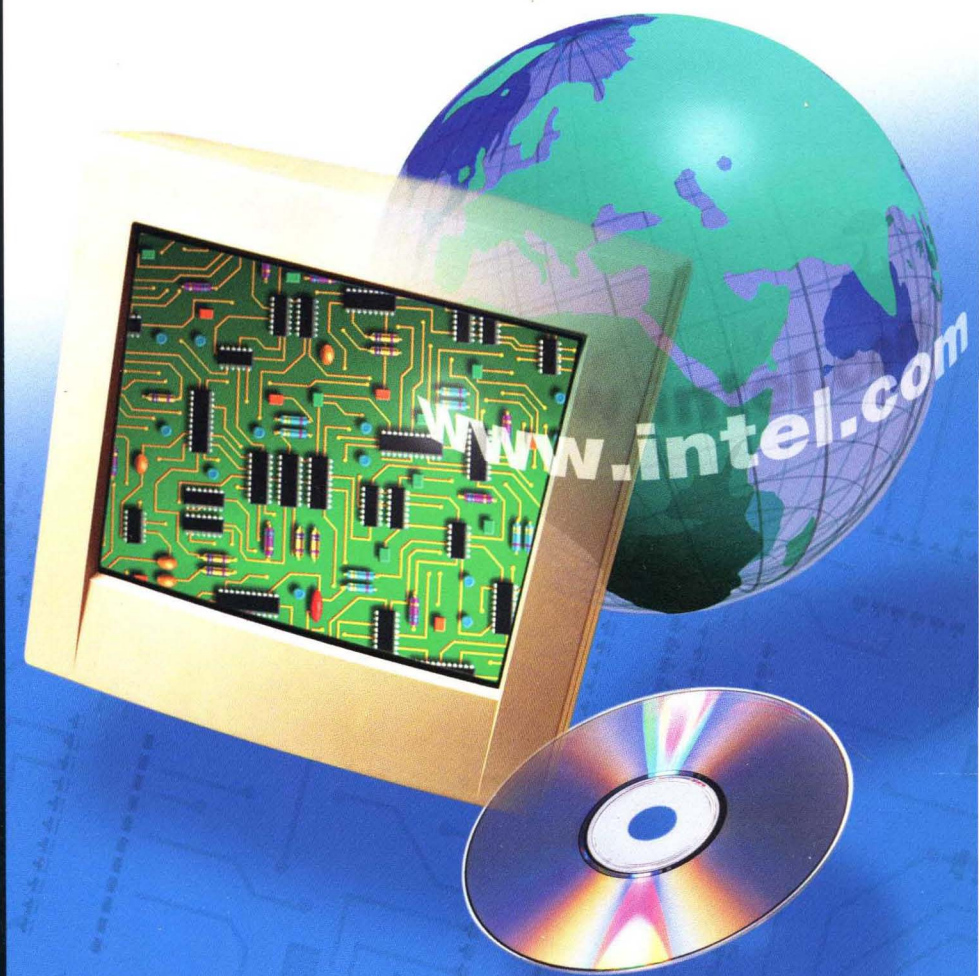
82557 Fast Ethernet Controller

82596 Ethernet Coprocessor

82595FX Ethernet Controller

Telecommunications Components

Communication/ Interface Controllers



intel®

LITERATURE

For additional information on Intel products in the U.S. or Canada, call Intel's Literature Center at (800) 548-4725 or write to:

INTEL LITERATURE SALES
P. O. Box 7641
Mt. Prospect, IL 60056-7641

To order literature outside of the U.S. and Canada contact your local sales office.

Additional information about Intel products is available on Intel's web site: http://www.intel.com.

CURRENT DATABOOKS

Product line databooks contain datasheets, application notes, article reprints, and other design information. All databooks can be ordered individually, and most are available in a pre-packaged set in the U.S. and Canada. Databooks can be ordered in the U.S. and Canada by calling TAB/McGraw-Hill at 1-800-822-8158; outside of the U.S. and Canada contact your local sales office.

Title	Intel Order Number	ISBN
SET OF NINE DATABOOKS (Available in U.S. and Canada)	**231003**	**N/A**
CONTENTS LISTED BELOW FOR INDIVIDUAL ORDERING:		
EMBEDDED MICROCONTROLLERS	270646	1-55512-248-5
EMBEDDED MICROPROCESSORS	272396	1-55512-249-3
FLASH MEMORY (2 volume set)	210830	1-55512-250-7
i960® PROCESSORS AND RELATED PRODUCTS	272084	1-55512-252-3
NETWORKING	297360	1-55512-256-6
OEM BOARDS, SYSTEMS AND SOFTWARE	280407	1-55512-253-1
PACKAGING	240800	1-55512-254-X
PENTIUM® AND PENTIUM PRO PROCESSORS AND RELATED PRODUCTS	241732	1-55512-251-5
PERIPHERAL COMPONENTS	296467	1-55512-255-8
ADDITIONAL LITERATURE: (Not included in handbook set)		
AUTOMOTIVE PRODUCTS	231792	1-55512-257-4
COMPONENTS QUALITY/RELIABILITY	210997	1-55512-258-2
EMBEDDED APPLICATIONS (1995/96)	270648	1-55512-179-9
MILITARY	210461	N/A
SYSTEMS QUALITY/RELIABILITY	231762	1-55512-046-6

A complete set of this information is available on CD-ROM through Intel's Data on Demand program, order number 240897. For information about Intel's Data on Demand ask for item number 240952.

December 1995
Order Number: 000900-001

Intel Application Support Services

World Wide Web [URL: http://www.intel.com/]

Intel's Web site now contains technical and product information that is available 24-hours a day! Also visit Intel's site for financials, history, current news and events, job opportunities, educational news and much, much more!

FaxBack*

Technical and product information are available 24-hours a day! Order documents containing:

- Product Announcements
- Product Literature
- Intel Device Characteristics
- Design/Application Recommendations
- Stepping/Change Notifications
- Quality and Reliability Information

Information on the following subjects are available:

- Microcontroller and Flash
- OEM Branded Systems
- Multibus and iRMX Software/BBS listing
- Multimedia
- Development Tools
- Quality and Reliability/Change Notification
- Microprocessor/PCI/Peripheral
- Intel Architecture Labs

To use FaxBack (for Intel components and systems), dial **(800) 628-2283** or 916-356-3105 (U.S./Canada/APAC/Japan) *or +44{0} 1793-496646 (Europe)* and follow the automated voice-prompt. Document orders will be faxed to the fax number you specify. For information on how the Intel Application Support team can help you, order our Customer Service Agreement, document #1201. Catalogs are updated as needed, so call for the latest information!

Bulletin Board System (BBS)

To use the Intel Application BBS (components and systems), dial **(503) 264-7999** or **(916) 356-3600** (U.S./Canada/APAC/Japan) *or +44{0} 1793-432955 (Europe).* The BBS will support 1200-19200 baud rate modem. *Typical modem configuration: 14.4K baud rate, No Parity, 8 Data Bits, 1 Stop Bit.*

CompuServe *Just type* 'Go Intel'

Intel maintains several forums where people come together to meet their peers, gather information, share discoveries and debate issues. For more information about service fees and access, call CompuServe at 1-800-848-8199 or 614-529-1340 (outside the U.S.). The INTELC forum is setup to support designers using various Intel components.

General Information Help Desk

Dial 1-800-628-8686 or 916-356-7599 (U.S. and Canada) between 5 a.m. and 5 p.m. PST for help with Intel products. For customers not in the U.S. or Canada, please contact your local distributor.

Intel Literature Centers

U.S.	+1-800-548-4725	France	+44{0} 1793 421777
U.S. (from overseas)	+1-708-296-9333	Germany	+44{0} 1793 421333
England	+44{0} 1793 431 155	Japan (fax only)	+81{0} 120 47 88 32

Intel Distributors

Check the back of an Intel data book or request one of the following distributor listing FaxBack documents: #4083 (U.S. Eastern Time Zone), #4084 (U.S. Central Time Zone), #4085 (Mountain Time Zone), #4086 (U.S. Alaska/Pacific Time Zone), #4209 (Europe) or #4403 (Canada).

* Other brands and names are the property of their respective owners.

December 1995
Order Number: 000901-001

intel®

Networking

Networking Components (Ethernet Controllers, Ethernet Coprocessors); Telecommunication Components; Communication/Interface Controllers*

1996

Information in this document is provided in connection with Intel products. Intel assumes no liability whatsoever, including infringement of any patent or copyright, for sale and use of Intel products except as provided in Intel's Terms and Conditions of Sale for such products.

Intel retains the right to make changes to these specifications at any time, without notice. Microcomputer Products may have minor variations to this specification known as errata.

*Other brands and names are the property of their respective owners.

†Since publication of documents referenced in this document, registration of the Pentium, OverDrive and iCOMP trademarks has been issued to Intel Corporation.

Contact your local Intel sales office or your distributor to obtain the latest specifications before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call 1-800-879-4683

COPYRIGHT © INTEL CORPORATION, 1996

DATASHEET DESIGNATIONS

Intel uses various datasheet markings to designate each phase of the document as it relates to the product. The markings appear in the lower inside corner of each datasheet page. Following are the definitions of each marking:

Datasheet Marking	Description
Product Preview	Contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available.
Advanced Information	Contains information on products being sampled or in the initial production phase of development.*
Preliminary	Contains preliminary information on new products in production.*
No Marking	Contains information on products in full production.*

* Specifications within these datasheets are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

November 1995
Order Number: 000902-001

intel®

Table of Contents

Alphanumeric Index

intel®

1

Local Area Network Components

82595TX
ISA/PCMCIA HIGH INTEGRATION ETHERNET CONTROLLER

- **Optimal Integration for Lowest Cost Solution**
  - Glueless 8-Bit/16-Bit ISA/PCMCIA 2.0 Bus Interface
  - Provides Fully 802.3 Compliant AUI and TPE Serial Interface
  - Local DRAM Support up to 64 Kbytes
  - FLASH/EPROM Boot Support up to 1 Mbyte for Diskless Workstations
  - Hardware and Software Portable between Motherboard, Adapter, and PCMCIA LAN Card Solution
- **High Performance Networking Functions**
  - Concurrent Processing Functionality for Enhanced Performance
  - 16-Bit/32-Bit IO Accesses to Local DRAM with Zero Added Wait-States
  - Ring Buffer Structure for Continuous Frame Reception and Transmit Chaining
  - Automatic Retransmission on Collision
  - Automatically Corrects TPE Polarity Switching Problems
- **Low Power CHMOS IV Technology**
- **Ease of Use**
  - Integrated Plug N' Play™ Hardware Functionality
  - EEPROM Interface to Support Jumperless Designs
  - Software Structures Optimized to Reduce Processing Steps
  - Automatically Maps into Unused PC IO Locations to Help Eliminate LAN Setup Problems
  - All Software Structures Contained in One 16-Byte IO Space
  - JTAG Port for Reduced Board Testing Times
  - Automatic or Manual Switching between TPE and AUI Ports
- **Power Management**
  - SL Compatible SMOUT Power Down Input
  - Software Power Down Command for Non-SL Systems
- **144-Lead tQFP Package Provides Smallest Available Form Factor**
- **100% Backwards Hardware/Software Compatible to 82595**

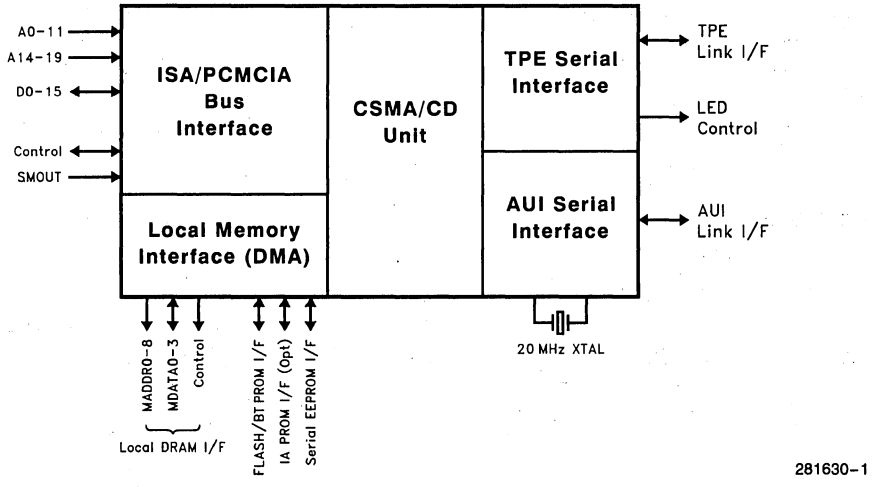


Figure 1. 82595TX Block Diagram

82595TX
ISA/PCMCIA High Integration ETHERNET Controller

CONTENTS

CONTENTS

CONTENTS

CONTENTS

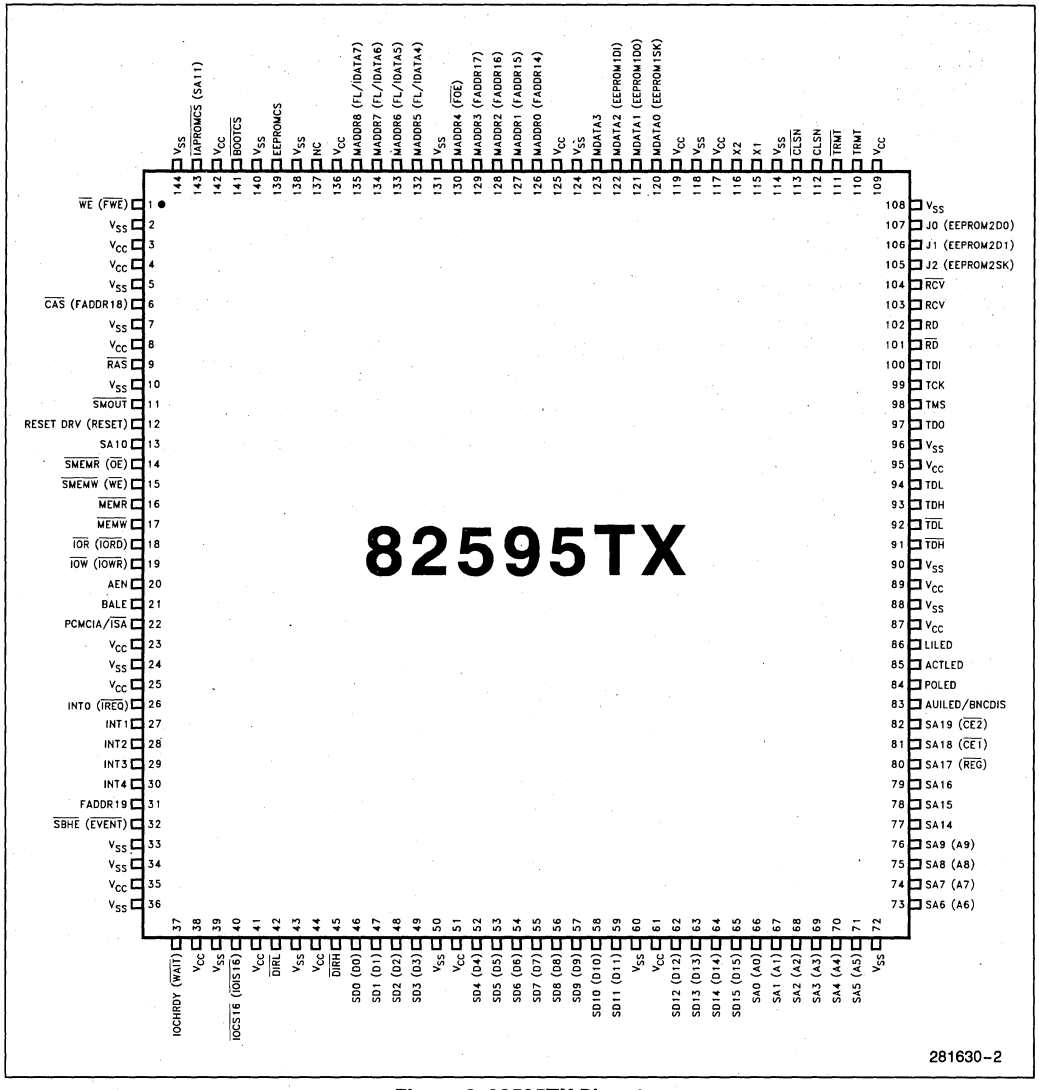


Figure 2. 82595TX Pinout

1.0 INTRODUCTION

1.1 82595TX Overview

The 82595TX is a highly integrated, high performance LAN controller which provides a cost effective LAN solution for ISA compatible Personal Computer (PC) motherboards (both desktop and portable), add-on ISA adapter boards, and PCMCIA cards. The 82595TX integrates all of the major functions of a buffered LAN solution into one chip with the exception of the local buffer memory, which is implemented by adding one DRAM component to the LAN solution. The 82595TX's new Concurrent Processing feature significantly enhances throughput performance. Both system bus and serial link activities occur concurrently, allowing the 82595TX to maximize network bandwidth by minimizing delays associated with transmit or receiving frames. The 82595TX's bus interface is a glueless attachment to either an ISA or PCMCIA version 2.0 bus. Its serial interface provides a Twisted Pair Ethernet (TPE) and an Attachment Unit Interface (AUI) connection. By integrating the majority of the LAN solution functions into one cost effective component, production cost saving can be achieved as well as significantly decreasing the design time for a solution. This level of integration also allows an 82595TX solution to be ported between different applications (PC motherboards, adapters, and PCMCIA IO cards), while maintaining a compatible hardware and software base. This results in further savings in both hardware and software development costs for manufacturers expanding into different applications i.e., an ISA adapter vendor producing PCMCIA IO cards, etc.

The 82595TX's software interface is optimized to reduce the number of processing steps that are required to interface to the 82595TX solution. The 82595TX's initialization and control registers are directly addressable within one 16-byte IO address block. The 82595TX can automatically resolve any conflicts to an IO block by moving its IO offset to an unused location in the case that a conflict occurs. The 82595TX's local memory is arranged in a simple ring buffer structure for efficient transfer of transmit and receive packets. The local memory, up to 64 Kbytes of DRAM, resides as either a 16-bit or 32-bit IO port in the host systems IO map programmable through configuration. The 82595TX provides direct control over the local DRAM, including refresh. The 82595TX performs a prefetch to the DRAM memory allowing CPU IO cycles to this data with no added wait-states. The 82595TX also provides an interface to up to 1 Mbyte of FLASH or EPROM memory. An interface to an EEPROM, which holds solution configuration values and can also contain the Node ID, allows for the implementation of a "jumperless" design. In addition, the 82595TX contains full hardware support for the implementation of the ISA Plug N' Play specification. Plug N' Play eliminates jumpers and complicated setup utilities by allowing peripheral functions to be added to a PC automatically (such as adapter cards) without the need to individually configure each parameter (e.g. Interrupt, IO Address, etc). This allows for configuration ease-of-use, which results in minimal time associated with installation.

The 82595TX's packaging and power management features are designed to consume minimal board real estate and system power. This is required for applications such as portable PC motherboard designs and PCMCIA cards which require a solution with very low real estate and power consumption. The 82595TX package is a 144-lead tQFP (thin Quad Flat Pack). Its dimensions are 20 mm by 20 mm, and 1.7 mm in height (roughly the same area as a US Nickel, and the same height as a US Dime). The 82595TX contains two power down modes; an SL compatible power down mode which utilizes the SL SMOUT input, and a POWER DOWN command for non-SL systems.

1.2 Enhancements to the 82595

The 82595TX is fully backwards compatible to the 82595, both in pinout and software. However, the 82595TX contains several advanced functions from the 82595 which increase performance and ease of use. The following is a list of the major enhancements to the 82595TX:

Concurrent Processing Functionality

32-Bit Local Memory IO Port

Integrated Plug N' Play support

Added EEPROM Interface for Plug N' Play

Flash addressing up to 1 Mbyte (versus 256K for 82595)

> For further information on these enhancements and a description of all the differences between the 82595 and 82595TX, please consult the 82595TX User's Manual, available through your local sales representative.

1.3 Compliance to Industry Standards

The 82595TX has two interfaces; the host system interface, which is an ISA or PCMCIA bus interface, and the serial, or network interface. Both interfaces have been standardized by the IEEE.

1.3.1 BUS INTERFACE— ISA IEEE P996/PCMCIA 2.0

The 82595TX implements the full ISA bus interface. It is compatible with the IEEE spec P996. The 82595TX also interfaces to ISA bus implementations that deviate from the IEEE spec by requiring early assertion of the IOCHRDY signal and alternate host address decode timing. This alternate timing can be configured in the 82595TX after a software test which is run at initialization time. The 82595TX can also be configured for a PCMCIA bus interface depending on the state of the PCMCIA/ISA input pin. In this case the 82595TX implements the complete PCMCIA interface, compatible to the PCMCIA revision 2.0 specification.

1.3.2 ETHERNET/TWISTED PAIR ETHERNET INTERFACE—IEEE 802.3 SPECIFICATION

The 82595TX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop, providing a fully compliant IEEE 802.3 AUI interface. The TPE port provides a fully compliant IEEE 10BASE-T interface. The 82595TX can automatically switch to whichever port (TPE or AUI) is active.

2.0 82595TX PIN DEFINITIONS

2.1 ISA Bus Interface

The ISA bus interface consists of three sections: an Address Bus, a Data Bus, and a Control section.

Symbol	Pin No.	Type	Name and Function
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11	66 67 68 69 70 71 73 74 75 76 13 143	I	**ADDRESS BUS:** These pins provide address decoding for up to 1 Kbyte of address. These pins also provide 4 Kbytes of IO addressing to support the Plug N' Play Standard.
SA14 SA15 SA16 SA17 SA18 SA19	77 78 79 80 81 82	I	**ADDRESS BUS:** These pins provide address decoding between the 16 Kbyte and 1 Mbyte memory space. This allows for decoding of a Boot EPROM or a FLASH in 16K increments.

2.1 ISA Bus Interface (Continued)

Symbol	Pin No.	Type	Name and Function
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15	46 47 48 49 52 53 54 55 56 57 58 59 62 63 64 65	I/O	**DATA BUS:** This is the data interface between the 82595TX and the host system. This data is buffered by one (8-bit design) or two (16-bit design) transceivers. The 82595TX's data lines should always be connected to the B side of the data bus transceiver.
AEN	20	I	**ADDRESS ENABLE:** Active high signal indicates a DMA cycle is active.
BALE	21	I	**BUFFERED ADDRESS LATCH ENABLE:** Falling edge used to latch a valid system address.
$\overline{\text{SMEMR}}$	14	I	**MEMORY READ** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{SMEMW}}$	15	I	**MEMORY WRITE** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{MEMR}}$/ 8/16 Detect	16	I	**MEMORY READ** for system memory accesses above or below 1 Mbyte. Active low. This pin also determines if the 82595TX is operating in an 8- or 16-bit system. For 16-bit systems, it should always be connected.
$\overline{\text{MEMW}}$	17	I	**MEMORY WRITE** for system memory accesses above or below 1 Mbyte. Active low.
$\overline{\text{IOR}}$	18	I	**IO READ:** Active low.
$\overline{\text{IOW}}$	19	I	**IO WRITE:** Active low.
$\overline{\text{IOCS16}}$	40	O	**IO CHIP SELECT 16:** Active low, open drain output which indicates that an IO cycle access to the 82595TX solution is 16-bit wide. Driven for IO cycles to the local memory or to the 82595TX.
IOCHRDY	37	O	**IO CHANNEL READY:** Active high, open drain output. When driven low, it extends host cycles to the 82595TX solution.
$\overline{\text{SBHE}}$	32	I	**SYSTEM BUS HIGH ENABLE:** Active low input indicates a data transfer on the high byte (D8–D15) of the system bus (a 16-bit transfer).
INT0 INT1 INT2 INT3 INT4	26 27 28 29 30	O	**82595TX INTERRUPT 0–4:** One of these five pins is selected to be active at a time (the other four are in Hi-Z state) by configuration. These active high outputs serve as interrupts to the host system.
RESET DRV	12	I	**RESET DRIVE:** Active high reset signal.

2.2 PCMCIA Bus Interface

The PCMCIA bus interface consists of three sections: an Address Bus, a Data Bus, and a Control section.

Symbol	Pin No.	Type	Name and Function
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9	66 67 68 69 70 71 73 74 75 76	I	**ADDRESS BUS:** These pins provide IO address decoding for up to 1 Kbyte.
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	46 47 48 49 52 53 54 55 56 57 58 59 62 63 64 65	I/O	**DATA BUS:** This is the data interface between the 82595TX and the host system.

2.2 PCMCIA Bus Interface (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{OE}$	14	I	**OUTPUT ENABLE (Memory Read):** Active low.
$\overline{WE}$	15	I	**WRITE ENABLE (Memory Write):** Active low.
$\overline{IORD}$	18	I	**IO READ:** Active low.
$\overline{IOWR}$	19	I	**IO WRITE:** Active low.
$\overline{IOIS16}$	40	O	**IO IS 16:** Active low output which indicates that an IO cycle access to the 82595TX solution is 16-bit wide. $\overline{IOIS16}$ should be asserted prior to Card Enable or CMD ($\overline{IORD}$ or $\overline{IOWR}$) assertion.
$\overline{WAIT}$	37	O	**WAIT:** Active low output when driven low, extends host cycles to the 82595TX.
$\overline{IREQ}$	26	O	**82595TX INTERRUPT:** Active low output.
RESET	12	I	**RESET:** Active high reset signal.
$\overline{CE1}$ $\overline{CE2}$	81 82	I	**Card Enable 1** and **Card Enable 2:** active low signals driven by the host. These signals provide a card select based on an address decode (decode done by the host) and also byte lane enables. When both $\overline{CE1}$ and $\overline{CE2}$ are high, no host accesses are made to the card. If $\overline{CE1}$ is low (active) and CE2 is high (inactive), the device operates in byte access mode with valid data being driven on D0–D7, and A0 determines the selection of an odd or even byte. When both $\overline{CE1}$ and $\overline{CE2}$ are low, a word access is taking place. In this case A0 is ignored, and the data is transferred on D0–D15. Odd-byte-only accesses can occur when $\overline{CE1}$ is high and $\overline{CE2}$ is low. In this case the data is driven on D8–D15 and A0 is ignored. See Section 4.9 for a summary of the PCMCIA decode functions.
$\overline{REG}$	80	I	**$\overline{REG}$:** is an active low input used to determine whether a host access is to Attribute memory (the 1st 1K of FLASH or CONF Regs) or to Common memory (FLASH above 1K). If $\overline{REG}$ is low the access is to Attribute memory, if $\overline{REG}$ is high the access is to Common memory. $\overline{REG}$ is also asserted low for all accesses to the 82595TX's IO Registers (including the access to the local DRAM via the 82595TX's Local Memory IO Port). See Section 4.9 for a summary of the PCMCIA decode functions.
$\overline{EVENT}$	32	O	**$\overline{EVENT}$:** is an active low output which, when enabled, will be asserted whenever a frame has been received by the 82595TX. This allows the 82595TX to "wake up" a system which has powered down (with the exception of powering down the LAN). This output will remain asserted until the 82595TX's RCV Interrupt (for the frame which woke up the system) has been acknowledged.

2.3 Local Memory Interface

Symbol	Pin No.	Type	Name and Function
MADDR0 MADDR1 MADDR2 MADDR3 MADDR4 MADDR5 MADDR6 MADDR7 MADDR8	126 127 128 129 130 132 133 134 135	O	**LOCAL MEMORY ADDRESS (MADDR0–MADDR8):** These outputs contain the multiplexed address for the local DRAM.

2.3 Local Memory Interface (Continued)

Symbol	Pin No.	Type	Name and Function
MDATA0 MDATA1 MDATA2 MDATA3	120 121 122 123	I/O	**LOCAL DATA BUS (MDATA0–MDATA3):** The four I/O signals, comprising the local data bus, are used to read or write data to or from the 4-bit wide DRAM. These signals also provide the lower 4 bits of data for accesses to an 8-bit FLASH/EPROM or IA PROM if these components are used. A 3.3K pull-up resistor connects to MDATA3 and enables EEPROM port 2.
$\overline{RAS}$	9	O	This active low output is the **Row Address Strobe** signal to the DRAM.
$\overline{CAS}$	6	O	This active low output is the **Column Address Strobe** signal to the DRAM.
$\overline{LWE}$	1	O	This active low output is the **Write Enable** to the DRAM.
FADDR14 FADDR15 FADDR16 FADDR17 FADDR18 FADDR19	126 127 128 129 6 31	O	**FLASH ADDRESS 14–17 :** These pins control the FLASH addressing from 16K to 1M to allow paging of the FLASH in 16K spaces. These addresses are under direct control of the FLASH PAGING configuration register. **NOTE:** ISA Bus I/F Only
$\overline{FOE}$	130	O	This output provides the active low **Output Enable** control to the **FLASH.**
$\overline{FWE}$	1	O	This output provides the active low **Write Enable** control to the **FLASH.**
$\overline{BOOTCS}$	141	O	**BOOT EPROM/FLASH $\overline{CS}$**
$\overline{IAPROMCS}$	143	O	**IA PROM $\overline{CS}$**
FL/IADATA4 FL/IADATA5 FL/IADATA6 FL/IADATA7	132 133 134 135	I/O	Provides the upper 4 bits of an 8 bit data path for both the Boot EPROM/FLASH and IA PROM, for CPU accesses. A 3.3K pull-down resistor connected to FL/IADATA4 and a 3.3K pull-up resistor connected to FL/IADATA7 enables AUTOFLASH/Boot EPROM detect.
EEPROMCS	139	I/O	**EEPROM CS:** Active high signal. If no EEPROM is connected, this pin should be connected to V_{CC}. In this case it will function as an input to the 82595TX to indicate no EEPROM is connected.
EEPROMSK Port 1 (EEPROM1SK) Port 2 (EEPROM2SK)	 120 105	O	**EEPROM SHIFT CLOCK:** This output is used to shift data into and out of the serial EEPROM. **NOTE:** Port 2 must be used for Plug N' Play
EEPROMDO Port 1 (EEPROM1DO) Port 2 (EEPROM2DO)	 121 107	I	**EEPROM DATA OUT** **NOTE:** Port 2 must be used for Plug N' Play
EEPROMDI Port 1 (EEPROM1DI) Port 2 (EEPROM1DI)	 122 106	O	**EEPROM DATA IN** **NOTE:** Port 2 must be used for Plug N' Play

2.4 Miscellaneous Control

Symbol	Pin No.	Type	Name and Function
$\overline{DIRL}$	42	O	**DIRECTION LOW:** Controls the direction of the low byte data bus transceiver. The direction defaults to always point in from the ISA bus to the 82595TX ($\overline{DIRL}$ = 1). This direction is turned around (82595TX out to ISA bus, $\overline{DIRL}$ = 0) only in the case of a read access to the 82595TX based solution.
$\overline{DIRH}$	45	O	**DIRECTION HIGH:** Controls the direction of the high byte data bus transceiver. The direction defaults to always point in from the ISA bus to the 82595TX ($\overline{DIRH}$ = 1). This direction is turned around (82595TX out to ISA bus, $\overline{DIRH}$ = 0) only in the case of a read access to the 82595TX based solution. This signal is active for 16-bit accesses only.
$\overline{SMOUT}$	11	I/O	This active LOW signal, when asserted, places the 82595TX into a Power Down mode. The 82595TX will remain in power down mode until $\overline{SMOUT}$ is unasserted. If this line is unconnected to $\overline{SMOUT}$ from the system bus, it can be used as an active low output which, when a POWER DOWN command is issued to the 82595TX, can be used to power down other external components (this output function is enabled by configuration).
PCMCIA/$\overline{ISA}$	22	I	This pin, when strapped low, selects an ISA bus interface. Strapped high selects PCMCIA.
J0 J1 J2	107 106 105	I I/O I/O	**JUMPER:** input for selecting between 7 ISA IO spaces (also selects whether the IO location should be read from the EEPROM). These pins should be connected to either V_{CC} or GND. The 82595TX reads the Jumper block during its initialization sequence.

J0	J1	J2	IO Address
GND	GND	GND	Address Contained in EEPROM
V_{CC}	GND	GND	2A0h
GND	V_{CC}	GND	280h
V_{CC}	V_{CC}	GND	340h
GND	GND	V_{CC}	300h
V_{CC}	GND	V_{CC}	360h
GND	V_{CC}	V_{CC}	350h
V_{CC}	V_{CC}	V_{CC}	330h

2.5 JTAG Control

Symbol	Pin No.	Type	Name and Function
TDO	97	O	**JTAG TEST DATA OUT**
TMS	98	I	**JTAG TEST MODE SELECT**
TCK	99	I	**JTAG TEST CLOCK**
TDI	100	I	**JTAG TEST DATA IN**

2.6 Serial Interface

Symbol	Pin No.	Type	Name and Function
TRMT	110	O	Positive side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out A).
$\overline{\text{TRMT}}$	111	O	Negative side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out B).
RCV	103	I	The positive input to a differential amplifier connected to the RCV pair of the AUI cable (Data In A). It is driven with 10 Mb/s Manchester Encoded data.
$\overline{\text{RCV}}$	104	I	The negative input to a differential amplifier connected to the RCV pair of the AUI cable (Data In B). It is driven with 10 Mb/s Manchester Encoded data.
CLSN	112	I	The positive input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In A).
$\overline{\text{CLSN}}$	113	I	The negative input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In B).
TDH	93	O	**TRANSMIT DATA HIGH:** Active high Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, $\overline{\text{TDH}}$, and $\overline{\text{TDL}}$ to generate the pre-conditioned twisted pair output waveform.
TDL	94	O	**TRANSMIT DATA LOW:** Twisted Pair Output Driver. Active high Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDH, $\overline{\text{TDH}}$, and $\overline{\text{TDL}}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{\text{TDH}}$	91	O	**TRANSMIT DATA HIGH INVERT:** Twisted Pair Output Driver. Active low Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{\text{TDL}}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{\text{TDL}}$	92	O	**TRANSMIT DATA LOW INVERT:** Twisted Pair Output Driver. Active low Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{\text{TDH}}$ to generate the pre-conditioned twisted pair output waveform.
RD	102	I	Active high Manchester Encoded data received from the twisted pair.
$\overline{\text{RD}}$	101	I	Active low Manchester Encoded data received from the twisted pair.
X1	115	I	**20 MHz CRYSTAL INPUT:** This pin can be driven with an external MOS level clock when X2 is left floating. This input provides the timing for all of the 82595TX functional blocks.
X2	116	O	**20 MHz CRYSTAL OUTPUT:** If X1 is driven with an external MOS level clock, X2 should be left floating.

2.6 Serial Interface (Continued)

Symbol	Pin No.	Type	Name and Function
AUI LED/BNC DIS	83	O	**AUI LED INDICATOR:** This output, when the 82595TX is used for as a TPE/AUI solution, will turn on an LED when the 82595TX is actively interfaced to its AUI serial port. When the 82595TX is used as a BNC/AUI solution, this output becomes the **BNC DIS** output, which can be used to power down the BNC Transceiver section (the Transceiver and the DC to DC Converter) of the solution when the BNC port is unconnected.
LILED	86	O	**LINK INTEGRITY LED:** Normally on (low) ouput which indicates a good link integrity status when the 82595TX is connected to an active TPE port. This output will remain on when the Link Integrity function has been disabled. It turns off (driven high) when Link Integrity fails, or when the 82595TX is actively interfaced to an AUI port. The minimum off time is 100 ms.
ACTLED	85	O	**LINK ACTIVITY LED:** Normally off (high) output turns on to indicate activity for transmission, reception, or collision. Flashes at a rate dependent on the level of activity on the link.
POLED	84	O	**POLARITY LED:** If the 82595TX detects that the receive TPE wires are reversed, POLED will turn on (low) to indicate the fault. POLED remains on even if automatic polarity correction is enabled, and the 82595TX has automatically corrected for the reversed wires.

2.7 Power and Ground

Symbol	Pin No.	Type	Name and Function
V_{CC}	3, 4, 8, 23, 25, 35, 38, 41, 44, 51, 61, 87, 89, 95, 109, 117, 119, 125, 136, 142	I	**POWER:** +5V ±5%.
V_{SS}	2, 5, 7, 10, 24, 33, 34, 36, 39, 43, 50 60, 72, 88, 90, 96, 108, 114, 118, 124, 131, 138, 140, 144	I	**GROUND:** 0V.

2.8 82595TX Pin Summary

ISA/PCMCIA Bus Interface

ISA Pin Name	MUXed PCMCIA Pin Name	Pin Type	P-Down State
SA0–SA11 (In)	A0–A9 (In)		Inactive
SA14–16 (In)			Inactive
SA17 (In)	$\overline{REG}$ (In)		Inactive/Act(1)
SA18 (In)	$\overline{CE1}$ (In)		Inactive/Act(1)
SA19 (In)	$\overline{CE2}$ (In)		Inactive
SD0–SD15 (I/O)	D0–D15 (I/O)	TS	TS
$\overline{SMEMR}$ (In)	$\overline{OE}$ (In)		Inactive
$\overline{SMEMW}$ (In)	$\overline{WE}$ (In)		Inactive
$\overline{IOR}$ (In)	$\overline{IORD}$ (In)		Inactive
$\overline{IOW}$ (In)	$\overline{IOWR}$ (In)		Inactive/Act(1)
INT0 (Out)	$\overline{IREQ}$ (Out)	TS	TS
INT1–4 (Out)		TS	TS
RESET DRV (In)	RESET (In)		Act
$\overline{IOCS16}$ (Out)	$\overline{IOIS16}$ (Out)	OD/TS	TS
BALE (In)			Inactive
IOCHRDY (Out)	$\overline{WAIT}$ (Out)	OD/2S	TS
$\overline{SBHE}$ (In)	$\overline{EVENT}$ (Out)	2S	Inactive/TS
AEN (In)			Inactive/Act(1)
$\overline{MEMR}$ (In)			Inactive
$\overline{MEMW}$ (In)			Inactive

NOTE:
1. For hardware powerdown using $\overline{SMOUT}$, these pins will be inactive. For software powerdown, these pins remain active.

Local Memory Interface

Pin Name	MUXed Pin Name	Pin Type	P-Down State
MADDR0–3 (Out)	FADDR14–17 (Out)	2S	TS
MADDR4 (Out)	$\overline{FOE}$ (Out)	2S	TS
MADDR5–8 (Out)	FL/IADATA4–7 (In)	TS	TS
MDATA0 (I/O)	EEPROM1SK(Out)	TS	TS
MDATA1 (I/O)	EEPROM1DO(In)	TS	TS
MDATA2 (I/O)	EEPROM1DI(Out)	TS	TS
MDATA3 (I/O)		TS	TS
$\overline{WE}$ (Out)	$\overline{FWE}$ (Out)	2S	TS
$\overline{RAS}$ (Out)		2S	PU
$\overline{CAS}$ (Out)	FADDR18 (Out)	2S	PU
$\overline{BOOTCS}$ (Out)		2S	PU
$\overline{IAPROMCS}$ (Out)	SA11 (In) (Dual)	2S	PU
EEPROMCS (I/O)		TS	PD
FADDR19 (Out)		TS	TS

Miscellaneous Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State	Dual Pin Name
$\overline{DIRL}$ (Out)		2S	PU	
$\overline{DIRH}$ (Out)		2S	PU	
J0(In)			ACT	EEPROM2D0 (In)
J1 (I/O)		TS	TS	EEPROM2DI (Out)
J2 (I/O)		TS	TS	EEPROM2SK (Out)
$\overline{SMOUT}$ (I/O)		TS	ACT/TS	
PCMCIA/$\overline{ISA}$ (In)			ACT	

JTAG Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TMS (In)			In Act
TCK (In)			In Act
TDI (In)			In Act
TDO (Out)		2S	

Serial Interface

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TRMT (Out)		Ana	TS
$\overline{TRMT}$ (Out)		Ana	TS
RCV (In)		Ana	In Act
$\overline{RCV}$ (In)		Ana	In Act
CLSN (In)		Ana	In Act
$\overline{CLSN}$ (In)		Ana	In Act
TDH (Out)		Ana	TS
TDL (Out)		Ana	TS
$\overline{TDH}$ (Out)		Ana	TS
$\overline{TDL}$ (Out)		Ana	TS
RD (In)		Ana	In Act
$\overline{RD}$ (In)		Ana	In Act
X1 (In)			In Act
X2 (Out)		2S	TS
LILED (Out)		2S	TS
POLED (Out)		2S	TS
ACTLED (Out)		2S	TS
AUILED (Out)	BNC DIS (Out)	2S	TS

Legend:
TS—TriState.
OD—Open Drain.
2S—Two State, will be found in either a 1 or 0 logic level.
Ana—Analog pin (all serial interface signals).
Act—Input buffer is active during Power Down.
In Act—Input buffer is inactive during Power Down.
PU—Output in inactive state with weak internal Pull-up during Power Down.
PD—Output in inactive state with weak internal Pull-down during Power Down.
Dual—Dual function pin.

3.0 82595TX INTERNAL ARCHITECTURE OVERVIEW

Figure 1 shows a high level block diagram of the 82595TX. The 82595TX is divided into four main subsections; a system interface, a local memory sub-system interface, a CSMA/CD unit, and a serial interface.

3.1 System Interface Overview

The 82595TX's system interface subsection includes a glueless ISA or PCMCIA bus interface (selectable by strapping), and the 82595TX's IO registers (including the 82595TX's command, status, and Data In/Out registers). The system interface block also interfaces with the 82595TX's local memory interface subsystem and CSMA/CD subsystem.

The bus interface logic provides the control, address, and data interface to either an ISA compatible or PCMCIA revision 2.0 bus. The 82595TX decodes up to 1M of total memory address space. Address decoding within 16K block increments (A14–A19) are used for Flash or Boot EPROM. IO accesses are decoded throughout the 1 Kbyte PC IO address range (A10 and A11 provide up to 4K of IO addressing and are used for Plug N' Play). The 82595TX data bus interface provides either an 8- or 16-bit interface to the host system's data bus. The control interface provides complete handshaking interface with the system bus to enable transfer of data between the 82595TX solution and the host system. This logic also controls the direction of the Data Bus transceivers.

The 82595TX's IO registers provide 3 banks of directly addressable registers which are used as the control and data interface to the 82595TX. There are 16 IO registers per bank, with only one bank enabled at a time. This allows the complete 82595TX software interface to be contained in one 16-byte IO space. The base address of this IO space is selectable via either software (which can be stored in a serial EEPROM interfaced to either of two ports in the 82595TX), or by strapping the 82595TX IO Jumper block (J0–J2). The 82595TX can also detect conflicts to its base IO space, and automatically resolve these conflicts either by allowing the selection of one Plug N' Play card from multiple cards (using Plug N' Play software), or by mapping itself into an un-used IO space (Automatic IO Resolution). Included in the 82595TX IO registers are the Command Register, the Status Register, and the Local Memory IO Port register, which provides the data interface to the local DRAM buffer contained in an 82595TX solution. Functions such as IO window mapping, Interrupt enable, RCV and XMT buffer initialization, etc. are also configured and controlled through the IO registers.

3.1.1 CONCURRENT PROCESSING FUNCTIONALITY

The 82595TX's Concurrent Processing feature significantly enchances data throughput performance by performing both system bus and serial link activities concurrently. Transmission of a frame is started by the 82595TX before that frame is completely copied into local memory. During reception, a frame is processed by the host CPU before that frame is entirely copied to local memory. Transmit Concurrent Processing feature is enabled by writing to BANK 2, Register 1, Bit 0. A 1 written to this bit enables this functionality, a 0 (default) disables it. To enable Receive Concurrent Processing, BANK 1, Register 7 must be programmed to value other than 00h (00h disables RCV Concurrent Processing, and is default). (See Section 4.1 for the format of IO BANK 1 and 2.) Concurrent Processing is not recommended for 8-bit interfaces. For more information on Transmit and Receive Concurrent Processing, refer to Section 7.0 and Section 8.0.

3.2 Local Memory Interface

The 82595TX's local memory interface includes a DMA unit which controls data transfers to or from the 82595TX's local DRAM, control for access to an IA PROM and a Boot EPROM/FLASH, and two interfaces to a serial EEPROM. The local memory interface subsection also arbitrates accesses to the local memory by the host CPU and the 82595TX.

Data transfers between the 82595TX and the local DRAM are always through the 82595TX's Local Memory 16-bit/32-bit IO Port. This allows the entire DRAM memory (up to 64 Kbytes) to be mapped into one IO location in the host systems IO map. By setting a configuration bit in the 82595TX's IO Registers (32IO/HAR#), the local memory can be extended from 16 bits to a full 32 bits. During 32-bit accesses, the CPU would perform a doubleword access addressed to register 12 of BANK0. The ISA bus will break this access up into two 16-bit accesses to Registers 12/13 followed by Registers 14/15, (or 4 sequential 8-bit accesses in an 8-bit interface). The CPU always accesses the 82595TX IO Port for Receive or Transmit data transfers, while the 82595TX automatically increments the address to the DRAM after each CPU access. The DRAMs data path is a 4-bit interface (typically 64K by 4-bits wide, or 256K by 4-bits wide) to allow for the lowest possible solution cost. The 82595TX implements a prefetch mechanism to the local DRAM so that the data is always available to the CPU as either an 8- or 16-bit word. In the case of the CPU reading from the DRAM, the 82595 TX reads the next four 4-bit nibbles from the DRAM, the 82595TX between CPU cycles so that the data is always available as a word in the 82595TX's Local Memory IO Port register. In the case of the CPU writing to the DRAM, the data is

written into the 82595TX's Local Memory IO Port then transferred to the DRAM by the 82595TX between CPU cycles. This prefetch mechanism of the 82595TX allows for IO read and writes to the local memory to be performed with no additional wait-states (3 clocks per data transfer cycle).

The DMA unit provides addressing and control to move RCV or XMT data between the 82595TX and the local DRAM. For transmission, the CPU is required only to copy the data to the local memory, initialize the 82595TX's DMA Current Address Register (CAR) to point to the beginning of the frame, and issue a Transmit Command to the 82595TX. The DMA unit facilitates the transfers from the local memory to the 82595TX as transmission takes place. The DMA unit will reset upon collision during a transmission, enabling automatic re-transmission of the transmit frame. During reception, the DMA unit implements a recyclable ring buffer structure which can receive continuous back to back frames without CPU intervention on a per frame basis (see Section 8.2 for details).

The 82595TX provides address decoding and control to allow access to an external Boot EPROM/FLASH or an IA PROM if these components are utilized in an 82595TX design (an IA PROM cannot be used for Plug N' Play). The 82595TX also provides two complete interfaces to a serial EEPROM (Port1 or Port2) to replace jumper blocks used to contain configuration information. Port1 is used to store configuration information such as IO Mapping Window, Interrupt line selection, etc., and is backwards pin compatible to the 82595TX EEPROM interface. Port2 is used to store configuration information as in Port1; in addition, it is used to store Plug N' Play information as defined in the Plug N' Play Specification.

The 82595TX arbitrates accesses to the local memory sub-system by the CPU and the 82595TX. The arbitration unit will hold off an 82595TX DMA cycle to the local memory if a CPU cycle is already in progress. Likewise, it will hold off the CPU if an 82595TX cycle is already in progress. The cycle which is held off will be completed on termination of the preceding cycle.

3.3 CSMA/CD Unit

The CSMA/CD unit implements the IEEE 802.3 CSMA/CD protocol. It performs such functions as transmission deferral to link traffic, interframe spacing, exponential backoff for collision handling, address recognition, etc. The CSMA/CD unit serves as the interface between the local memory and the serial interface. It serializes data transferred from the local memory before it is passed to the serial interface unit for transmission. During frame reception, it converts the serial data received from the serial interface to a byte format before it is transferred to local memory. The CSMA/CD unit strips framing parameters such as the Preamble and SFD fields before the frame is passes to memory for reception. For transmission, the CSMA/CD unit builds the frame format before the frame is passed to the serial interface for transmission.

3.4 Serial Interface

The 82595TX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also interface to a transceiver device to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595TX automatically enables either to the AUI or TPE interface depending on which medium is connected to the chip. Software configuration can override this automatic selection.

4.0 ACCESSING THE 82595TX

All access to the 82595TX is made through one of three banks of IO registers. Each bank contains 16 registers. Each register in a bank is directly accessible via addressing. Through the use of bank switching, the 82595TX utilizes only 16 IO locations in the host system's IO map to access each of its registers. The different banks are accessed by setting the POINTER field in the 82595TX Command Register to select each bank. The Command Register is Register for each bank.

4.1 82595TX Register Map

The 82595TX registers are contained in three banks of 16 IO registers per bank. These three banks are shown in the following three pages.

4.1.1 IO BANK 0

The format for IO Bank 0 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
RCV States		EXEC States		EXEC INT	TX INT	RX INT	RX STP INT	Reg 1
ID REGISTER (Counter)		1	(Auto En)	0	1	0 RESERVED	0	Reg 2
0 Resvrd	0 Resvrd	Cur/ $\overline{\text{Base}}$	32 IO/ $\overline{\text{HAR}}$	EXEC Mask	TX Mask	RX Mask	RX STP Mask	Reg 3
RCV CAR/BAR (Low)								Reg 4
RCV CAR/BAR (High)								Reg 5
RCV STOP REG (Low)								Reg 6
RCV STOP REG (High)								Reg 7
RCV Copy Threshold REG								Reg 8
0	0	0	0	0	0	0	0	
(Reserved)								Reg 9
XMT CAR/BAR (Low)								Reg 10
XMT CAR/BAR (High)								Reg 11
Host Address Reg/32-Bit I/O (Byte 0) (Low)								Reg 12
Host Address Reg/32-Bit I/O (Byte 1) (High)								Reg 13
Local Memory/32-Bit I/O (Byte 2) IO Port (Low)								Reg 14
Local Memory/32-Bit I/O (Byte 3) IO Port (High)								Reg 15

1

4.1.2 IO BANK 1

The format for IO Bank 1 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
$\overline{\text{Tri-ST}}$ INT	Alt RDY Tm	0 Resvrd	0 Resvrd	0 Resvrd	0 Resvrd	Host Bus Wd	0 Resvrd	Reg 1
FL/$\overline{\text{BT}}$ Detect	Boot EPROM/FLASH Decode Window			0 Resvrd	INT Select			Reg 2
0	0	I/O Mapping Window						Reg 3
0	0	0	0	0	0	0	0	Reg 4
(Reserved)								
0	0	0	0	0	0	0	0	Reg 5
(Reserved)								
0	0	0	0	0	0	0	0	Reg 6
(Reserved)								
RCV BOF Threshold REG								Reg 7
RCV LOWER LIMIT REG (High Byte)								Reg 8
RCV UPPER LIMIT REG (High Byte)								Reg 9
XMT LOWER LIMIT REG (High Byte)								Reg 10
XMT UPPER LIMIT REG (High Byte)								Reg 11
FLASH PAGE SELECT HIGH		FLASH WRITE ENABLE		FLASH PAGE SELECT				Reg 12
0	0	0	0	0	$\overline{\text{SMOUT}}$ OUT EN	AL RDY TEST	AL RDY PAS/FL	Reg 13
0	0	0	0	0	0	0	0	Reg 14
(Reserved)								
0	0	0	0	0	0	0	0	Reg 15
(Reserved)								

4.1.3 IO BANK 2

The format for IO Bank 2 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
Disc Bad Fr	Tx Chn $\overline{\text{ErStp}}$	Tx Chn Int Md	PCMCIA/ $\overline{\text{ISA}}$	0	0	0	TX Con Proc En	Reg 1
LoopBack		Multi IA	No SA Ins	Length $\overline{\text{Enable}}$	RX CRC $\overline{\text{InMem}}$	BC DIS	PRMSC Mode	Reg 2
Test1	Test2	BNC/ $\overline{\text{TPE}}$	$\overline{\text{APORT}}$	Jabber Disabl	TPE/ $\overline{\text{AUI}}$	Pol $\overline{\text{Corr}}$	Lnk In Dis	Reg 3
INDIVIDUAL ADDRESS REGISTER 0								Reg 4
INDIVIDUAL ADDRESS REGISTER 1								Reg 5
INDIVIDUAL ADDRESS REGISTER 2								Reg 6
INDIVIDUAL ADDRESS REGISTER 3								Reg 7
INDIVIDUAL ADDRESS REGISTER 4								Reg 8
INDIVIDUAL ADDRESS REGISTER 5								Reg 9
STEPPING			Trnoff Enable	EEDO	EEDI	EECS	EESK	Reg 10
RCV NO RESOURCE COUNTER								Reg 11
IAPROM IO Port								Reg 12
0	0	0	0	0	0	0	0	Reg 13
(Reserved)								
0	0	0	0	0	0	0	0	Reg 14
(Reserved)								
0	0	0	0	0	0	0	0	Reg 15
(Reserved)								

4.2 Writing to the 82595TX

Writing to the 82595TX is accomplished by an IO Write instruction (such as an OUT instruction) from the host processor to one of the 82595TX registers. The 82595TX registers reside in a block of 16 contiguous addresses contained within the PC IO address space. The mapping of this address block is programmable throughout the 1 Kbyte PC IO address map.

The 82595TX registers are contained within three banks of IO registers. When writing to a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once a bank is selected, all register accesses are made in that bank until a switch to another bank is performed. Switching banks is accomplished by writing to the PTR field of Reg 0 in any bank. Reg 0 is the command register of the 82595TX and its functionality is identical in each bank. Once in the appro-

priate bank, the processor can write directly to any of the 82595TX registers by simply issuing an OUT instruction to the IO address of the register.

4.3 Reading from the 82595TX

Reading from the 82595TX is accomplished by an IO Read instruction (such as an IN instruction) from the host processor to one of the 82595TX registers. When reading from a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once in the appropriate bank, the processor can read directly from any of the 82595TX registers by simply issuing an IN instruction to the IO address of the register.

4.4 Local DRAM Accesses

IO mapping the local DRAM memory of an 82595TX solution allows it to appear as simply an IO Port to the host system. This allows an 82595TX solution to work in PCs which do not have enough space in their system memory map to accommodate the addition of LAN buffer memory (typically 16 Kbytes to 64 Kbytes) into the map. The entire local memory (up to 64 Kbytes) is mapped into one 16-bit IO Port location. For all IO-mapped accesses to the local memory of a 82595TX solution, the 82595TX performs the IO address decoding and the ISA Bus interface handshake and asserts the address and control signals to the local memory.

4.4.1 WRITING TO LOCAL MEMORY

The local memory of an 82595TX solution is written to whenever the host CPU performs a Write operation to the 82595TX Local Memory IO Port. Prior to writing a block of data to the local memory, the CPU should update the 82595TX Host Address Register with the first address to be written. The CPU then copies the data to the local memory by writing it to the 82595TX Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82595TX upon completion of each write cycle. This allows sequential accesses to the local memory, even though the IO port address accessed does not change.

4.4.2 READING FROM LOCAL MEMORY

The local memory of an 82595TX solution is read from whenever the host CPU performs a Read operation from the 82595TX Local Memory IO Port. Prior to reading a block of data from the local memory, the CPU should utilize the 82595TX Host Address Register to point to first address to be read. The CPU then reads the data from the local memory through the 82595TX Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82595TX upon completion of each read cycle.

4.5 Serial EEPROM Interface

A Serial EEPROM, a Hyundai HY93C46 or equivalent IC, stores configuration data for the 82595TX. The use of an EEPROM enables 82595TX designs to be implemented without jumpers (the use of jumpers to select IO windows is optional.) The 85295TX provides two complete interfaces to a serial EEPROM (Port1 or Port2, and only one port can be used). Port1 is used to store configuration information in the EEPROM, such as IO Base Address and Interrupt selection, and is backwards pin compatible to the 82595 EEPROM interface. Port2 stores configuration information as in Port1; in addition, it is used to store Plug N' Play information as defined in the Plug N' Play specification. Plug N' Play allows peripheral functions to be added to a PC (such as adapter cards) without the need to individually configure each parameter (e.g. Interrupt, IO Address, etc). Information describing system resources are contained within the 82595TX configuration registers. This allows Auto-configuration software, which is usually contained in the BIOS or O/S, to identify system resource usage, identify conflicts and automatically re-configure the 82595TX.

The 82595TX automatically accesses Register 0 of the EEPROM upon a RESET in ISA Bus Interface mode. Register 0 contains the information that the 82595TX must be configured to allow CPU accesses to it (IO Mapping Window, FLASH Detect Enable, Auto I/O Enable, Boot EPROM/FLASH Window, Host Bus Width, and Plug N' Play Enable) following a system boot. The format for EEPROM Register 0 is shown in Figure 4-1. Note that all 0's are assumed to be reserved. In the case where an EEPROM is either unprogrammed (each bit defaults to a 1) or completely erased (all 0's), the 82595TX will default to IO Address 300h.

For additional information regarding a Plug N' Play implementation for the 82595TX, please consult the 82595TX User Manual and LAN595TX Specification, available through your local sales representative. The latest Plug N' Play Specification is available by Microsoft.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IO Mapping Window						0	Flash	0	Auto	BT/FLSH Window			Hst	0	PnP
MSb					LSb		Det		I/O En	MSb		LSb	Wdt		En

Figure 4-1. EEPROM Register 0

4.6 Boot EPROM/FLASH Interface

The Boot EPROM/FLASH of an 82595TX solution is read from or written to (FLASH only) whenever the host CPU performs a Read or a Write operation to a memory location that is within the Boot EPROM/FLASH mapping window. This window is programmable throughout the ISA PROM address range (C8000–DFFFF) by configuring the 82595TX Boot EPROM Decode Window register (Bank 1, Register 2, bits 4–6). The 82595TX asserts the BOOTCS# signal when it decodes a valid access. Up to 1 MBytes of FLASH can be addressed by the 82595TX.

4.7 IA PROM Interface

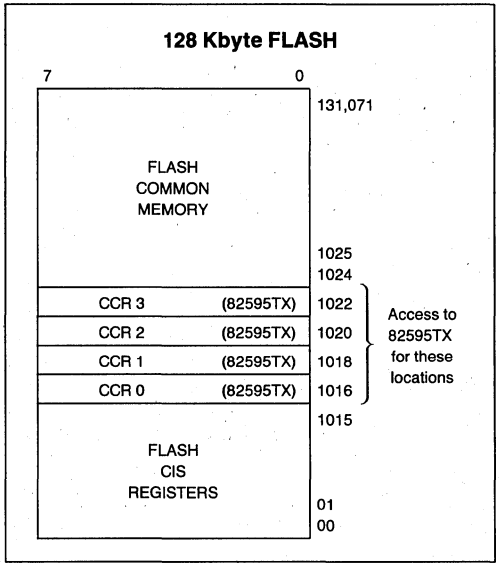
The 82595TX supports an IA PROM interface. Implementation of an IA PROM in a 82595TX solution is optional. The IA can also be stored in the serial EEPROM. In this case the IA PROM is not needed. For Plug N' Play, an IA PROM cannot be used.

4.8 PCMCIA CIS Structures

The 82595TX supports access to 1K of Attribute Memory when configured for PCMCIA support. Attribute memory is defined by the PCMCIA standard to be comprised of the Card Information Structure (FLASH memory referred to as CIS residing at memory offset 0 to 1015:decimal) and 4 8-bit Card Configuration Registers which reside at memory offset 1016 to 1022 on even boundaries only (1016, 1018, 1020, 1022). These four registers are contained in the 82595TX. They are memory mapped and are accessed when $\overline{CE1}$ and $\overline{REG}$ are asserted low along with the decode of A0–A9 and assertion of either a $\overline{OE}$ or $\overline{WE}$. The 82595TX Card Configuration Registers are shown at the bottom of this page.

4.9 PCMCIA Decode Functions

The Attribute Memory and Common Memory map for a PCMCIA card is shown below. Attribute Memory is defined as the CIS structures (residing in FLASH below 1K) and the CCR Registers (residing in the 82595TX). Common Memory is defined as the FLASH memory above 1K.



82595TX Card Configuration Registers

7	6	5	4	3	2	1	0	
RESET	0	0	0	0	0	XIP En	IO En	CCR 0 (Addr 1016)
0	0	IOIS8	EvntWk	0	0	IREQ	0	CCR 1 (Addr 1018)
0	0	0	0	0	0	0	0	CCR 2 (Addr 1020)
0	0	0	0	0	0	0	0	CCR 3 (Addr 1022)

NOTE:
All 0's in the above registers are reserved.

5.0 COMMAND AND STATUS INTERFACE

The format for the 82595TX Command Register is shown in Figure 5-1. The Command Register resides in Register 0 of each of the three IO Banks of the 82595TX, and can be accessed in any of these banks. The Command Register is accessed by writing to or reading from the IO address for Register 0.

5.1 Command OP Code Field

Bits 0 through 4 of the Command Register comprise the Command OP Code field. A command is issued to the 82595TX by writing it into the Command OP Code field. A command can be issued to the 82595TX at any time; however in certain cases the command may be ignored (for example, issuing a Transmit command while a Transmit is already in progress). In these cases the command is not performed, and no interrupt will result from it.

The Command OP Code field can also be read. In this case it will indicate an execution status event other than TRANSMIT DONE (TDR Done, DIAGNOSE Done, MC-SETUP Done, DUMP Done, INIT Done, and POWER-UP) has been completed. This field is valid only when the EXEC INT bit (Bank 0, Reg 1, Bit 3) is set.

5.2 ABORT (Bit 5)

This bit indicates if an execution command other than TRANSMIT was aborted while in progress. This bit provides status information only. It should be written to a 0 whenever the Command Register is written to.

5.3 Pointer Field (Bits 6 and 7)

The Pointer field controls which 82595TX IO register bank is currently to be accessed (Bank 0, Bank 1, or Bank 2). Writing a 00:b to the Pointer field selects Bank 0, 01:b for Bank 1, and 10:b for Bank 2. The Pointer field is valid only when the SWITCH BANK (0h) command is issued. This field will be ignored for any other command. The 82595TX will continue to operate in a current bank until a different bank is selected. Upon power up of the device or Reset, the 82595TX will default to Bank 0.

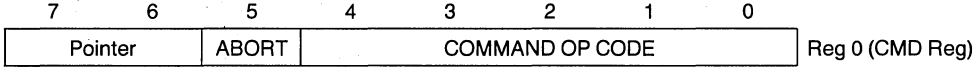


Figure 5-1. 82595TX Command Register

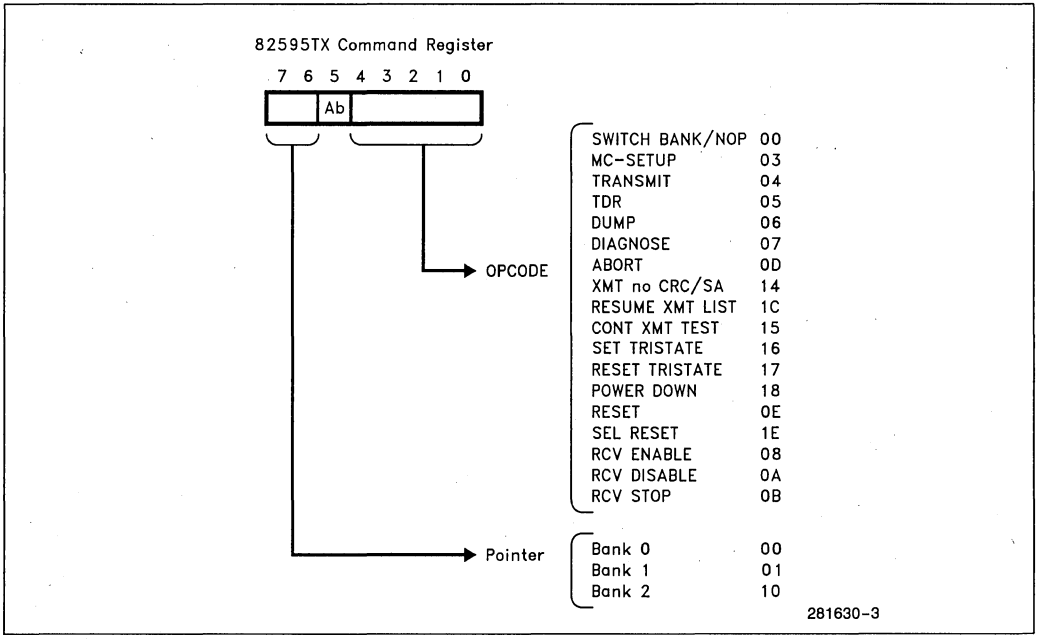


Figure 5-2. 82595TX Command Interface

5.4 82595TX Status Interface

The Status of the 82595TX can be read from Register 1 of Bank 0, with additional status information contained in Register 0 (the Command Register). Figure 5-3 shows these registers. Other information concerning the configuration and initialization of the 82595TX and its registers can be obtained by directly reading the 82595TX registers.

When read, the Command OP Code field indicates which event (MC Done, Init Done, TDR Done, or DIAG Done) has been completed. This field is valid only when the EXEC INT Bit (Bank 0, Reg 1, Bit 3) is set to a 1. Reading the Pointer field indicates which bank the 82595TX is currently operating in. Register 1 in Bank 0 contains the 82595TX interrupts status as well as the current states of the RCV and Execution units of the 82595TX. Resultant status from events such as the completion of a transmission or the reception of an incoming frame is contained in the status field of the memory structures for these particular events.

6.0 INITIALIZATION

Upon either a software or hardware RESET, the 82595TX enters into its initialization sequence. When the 82595TX is interfaced to an ISA bus, the 82595TX reads information from its EEPROM and Jumper block (if utilized) which configures critical parameters (IO Address mapping, etc.) to allow initial accesses to the 82595TX during the host system's initialization sequence and also access by the software device driver. The 82595TX can also be configured (via the EEPROM) to automatically resolve any conflicts to its IO address location either by moving its IO address offset to an unused location in the case that a conflict occurs, or by using the Plug N' Play Software to the I/O address location. This process eliminates a large majority of LAN end-user setup problems.

The 82595TX can be configured to operate with ISA systems that require early deassertion of the IOCHRDY signal to its low (not ready) state. The 82595TX, along with its software driver, can perform a test at initialization to determine if early IOCHRDY deassertion is required.

The 82595TX, when interfaced to a PCMCIA bus, simply powers up with default PCMCIA configuration values enabled. This is the only step for PCMCIA initialization, since the PCMCIA bus requires no selection of Interrupts, IO Space, etc.

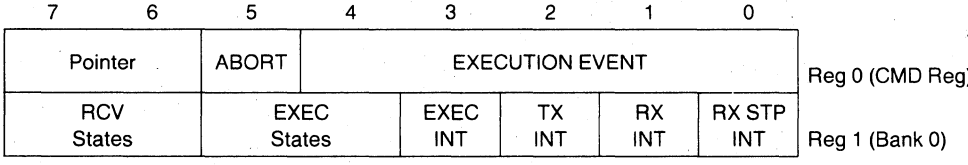


Figure 5-3. 82595TX Status Information

7.0 FRAME TRANSMISSION

The 82595TX performs all of the necessary functions needed to transmit frames from its local memory. If Transmit Concurrent Processing is enabled, the CPU must only program the Base and Host Address Register with the starting address to be transmitted, copy a portion of the frame into the 82595TX's transmit buffer located in local memory (the number of bytes for this first portion is determined by the software driver without causing an Underrun), issue a XMT command to the 82595TX, and complete the data copies for this frame to local memory. If Transmit Concurrent Processing is disabled, the CPU must copy an entire frame into the 82595TX's transmit buffer located in local memory, set up the 82595TX's Current Address Registers to point to that frame, and issue a XMT command to the 82559TX. The 82595TX performs all the link management functions, DMA operations, and statistics keeping to handle transmission onto the link and communicate the status of the transmission to the CPU. The 82595TX performs automatic retransmission on collision with no CPU interaction.

7.1 82595TX XMT Block Memory Format

The format in which a XMT block is written to memory by the CPU is shown in Figure 7-1 for a 16-bit interface. Figure 7-2 shows this structure for an 8-bit interface.

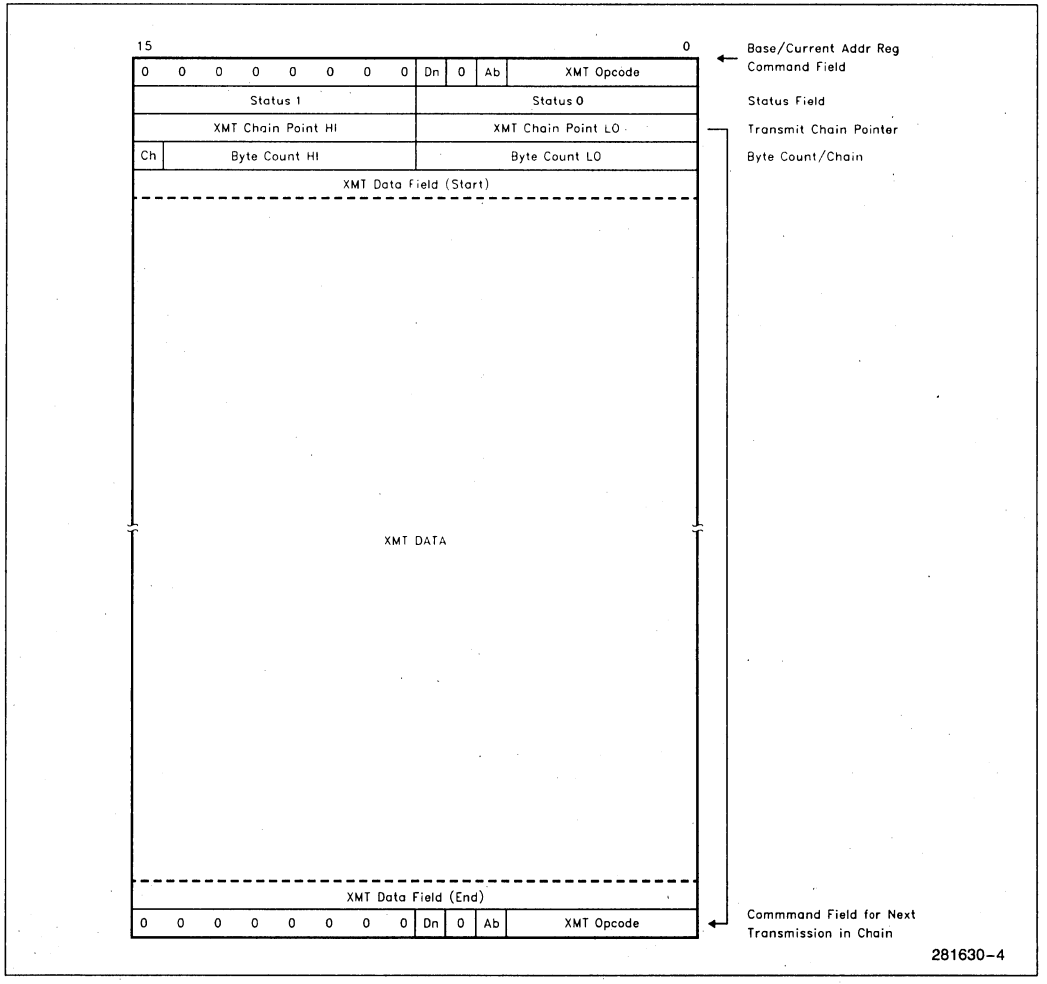


Figure 7-1. XMT Block Memory Structure (16-Bit)

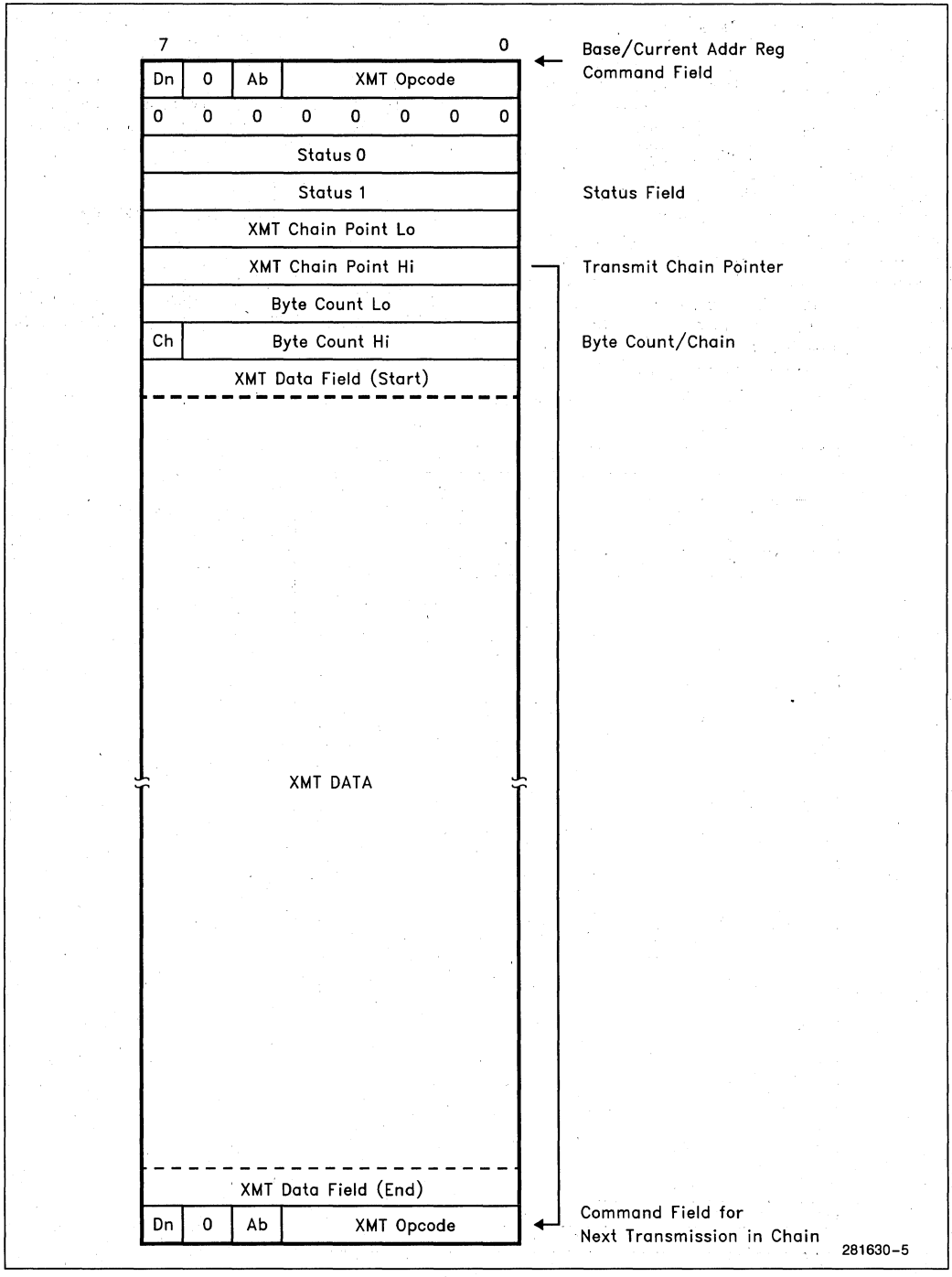


Figure 7-2. XMT Block Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 7-3. In a 16-bit wide interface, these two bytes will combine to form one word. This field is originally set to all 0's by the CPU as the XMT block is copied to memory. It is updated by the 82595TX upon completion of the transmission.

7.2 XMT Chaining

The 82595TX can transmit consecutive frames without the CPU having issued a separate Transmit command for each frame. This is called Transmit Chaining. The 82595TX Transmit Chaining memory structure for a 16-bit interface is shown in Figure 7-4, with an 8-bit interface shown in Figure 7-5. The 82595TX registers which control the memory structure are also shown. The CPU places multiple XMT blocks in the Transmit buffer. The 82595TX will transmit each frame in the chain, reporting the status for each frame in its status field. If Concurrent Processing is enabled, the copy of additional frames in a chain will take place while the first portion of the chain (one or more frames) is being transmitted by the 82595TX. This chain can be dynamically updated by the CPU to add more frames to the chain. The transmit chain can be configured to terminate upon an errored frame (maximum collisions, underrun, lost CRS, etc.) or it can continue to the next frame in the chain. The 82595TX can be configured to interrupt upon completion of each transmission or to interrupt at the end of the transmit chain only (it always interrupts upon an errored condition).

7	6	5	4	3	2	1	0	
TX DEF	HRT BET	MAX COL	X	No OF COLLISIONS				Status 0
COLL	X	TX OK	0	LTCOL	LST CRS	X	UND RUN	Status 1

Figure 7-3. Transmit Result

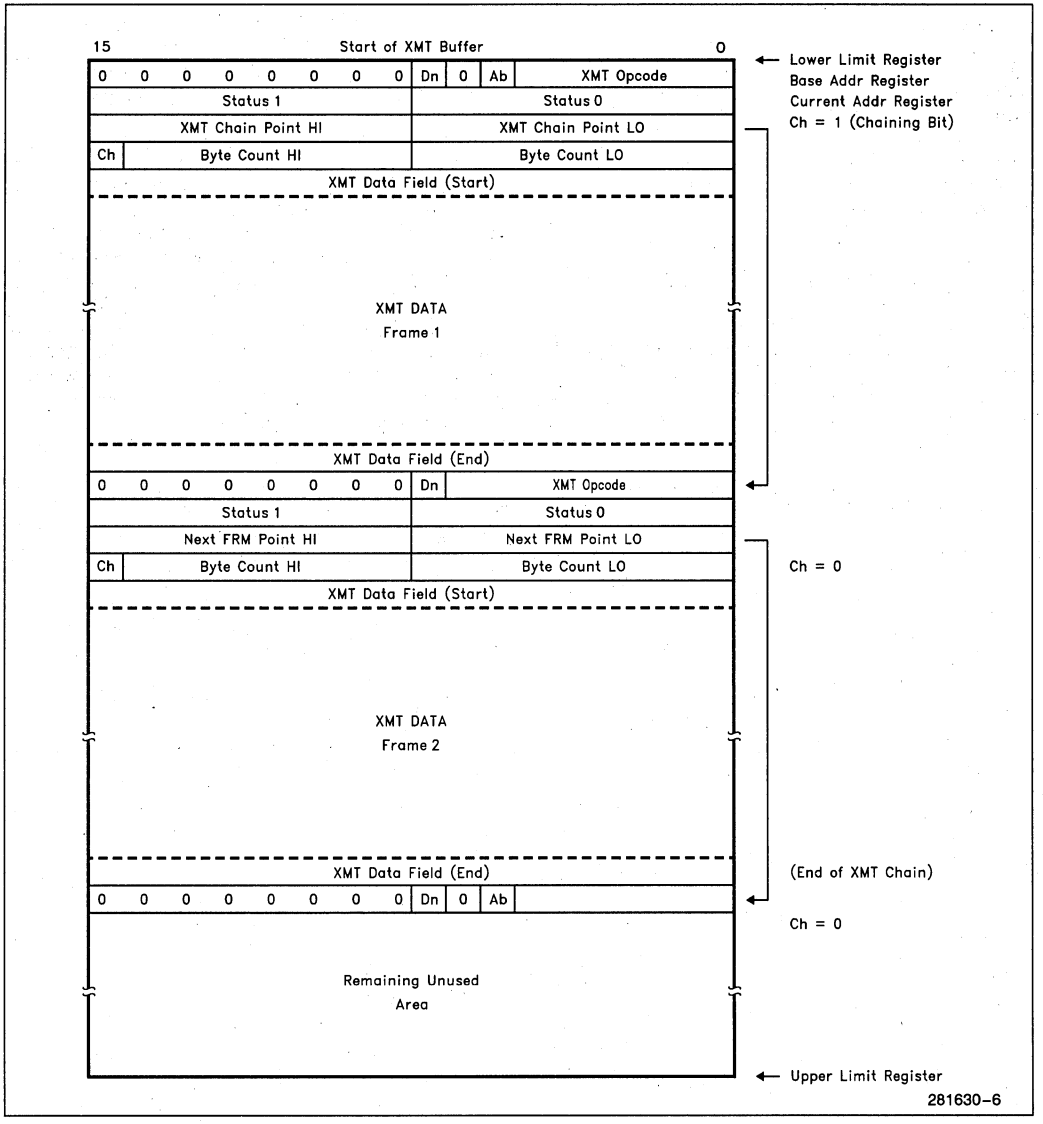


Figure 7-4. 82595TX XMT Chaining Memory Structure

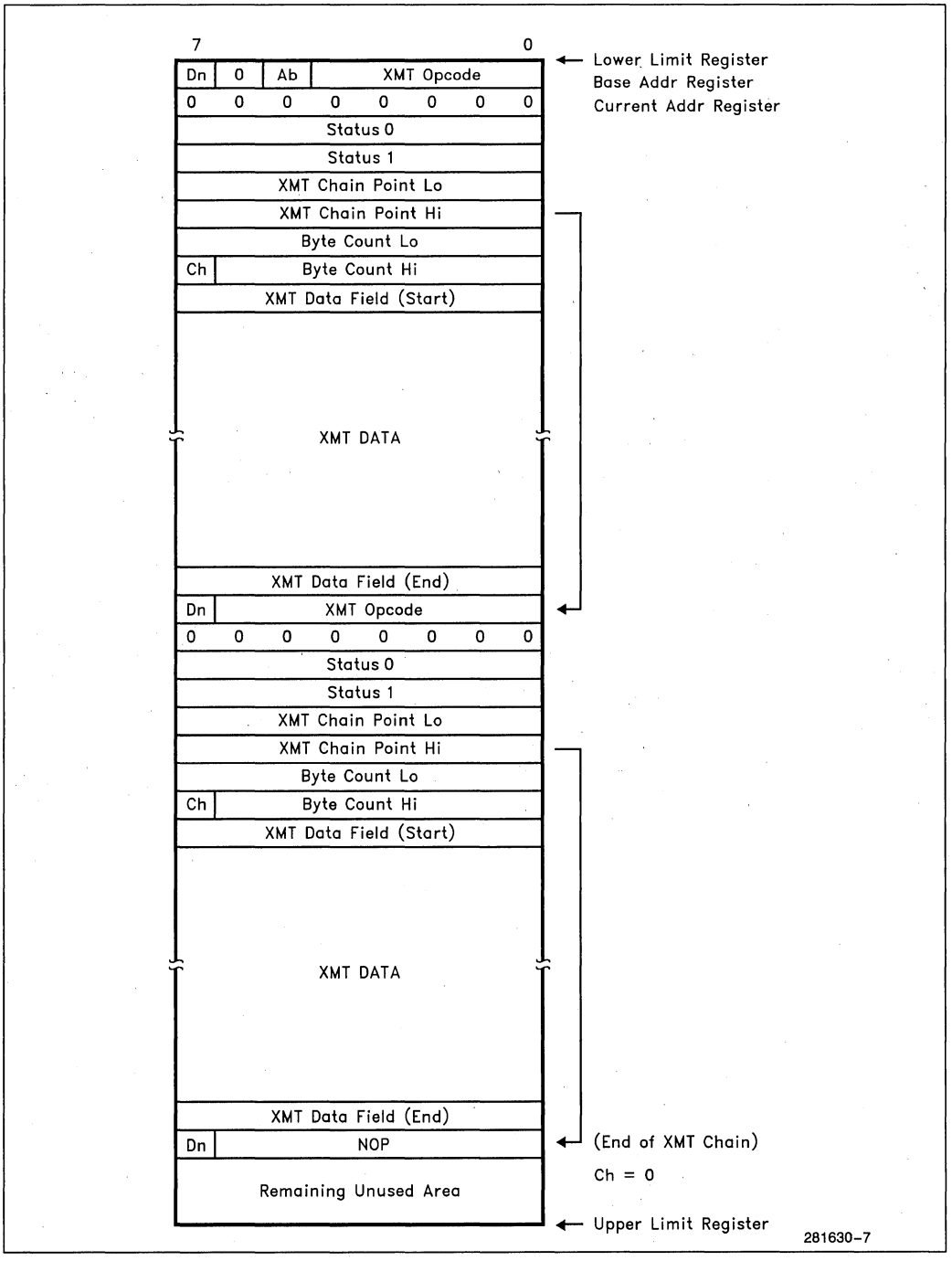


Figure 7-5. XMT Block Memory Structure (8-Bit)

7.3 Automatic Retransmission on Collision

The 82595TX performs automatic retransmission when a collision is experienced within the first slot time of the transmission with no intervention by the CPU. The 82595TX performs jamming, exponential backoff, and retransmission attempts as specified by the IEEE 802.3 spec. The 82595TX reaccesses its local memory automatically on collision. This allows the 82595TX to retransmit up to 15 times after the initial collision with no CPU interaction.

The 82595TX reaccesses the data in its transmit buffer by simply resetting the value of its Current Address Register back to the value of the Base Address Register (the beginning of the XMT block) and repeating the DMA process to access the data in the transmit buffer again. Once it regains access to the link, retransmission is attempted. When Transmit Chaining is utilized, the process for retransmission is exactly the same. Only the current frame in the chain will be retransmitted, since the Base Address Register is updated upon transmission of each frame.

8.0 FRAME RECEPTION

The 82595TX implements a recyclable ring buffer DMA structure to support the reception of back to back incoming RCV frames with minimal CPU overhead. The structure of the RCV frames in memory is optimized to allow the CPU to process each frame with as few software processing steps as possible. The frame format is arranged so that all of the required infomation for each frame (status, size, etc.) is located at the beginning of the frame.

8.1 82595TX RCV Memory Structure

The 82595TX RCV memory structure for a 16-bit interface is shown in Figure 8-1. Figure 8-2 shows this structure for the 8-bit interface. Once an incoming frame passes the 82595TX's address filtering, the 82595TX deposits the frame into the RCV Data field of the RCV Memory Structure. The fields which precede the RCV Data field, Event, Status, Byte Count, Next Frame Pointer, and the Event field of the following frame, are updated upon the end of the frame after all of the incoming data has been deposited in the RCV Data field. If Receive Concurrent Processing is enabled, the CPU processes the receive frame without the entire frame being deposited by the 82595TX to the RCV Data Field. The 85295TX, along with the software driver, determines the portion of the frame being copied to host memory before the rest of that frame is copied to local memory. An interrrupt is asserted by the 82595TX (EOF) after frame reception has been completed.

If the 82595TX is configured to Discard Bad Frames, it will discard all incoming errored frames by resetting its DMA Current Address Register back to the value of the Base Address Register and not updating any of the fields in the RCV frame structure. This area will now be reused to store the next incoming frame.

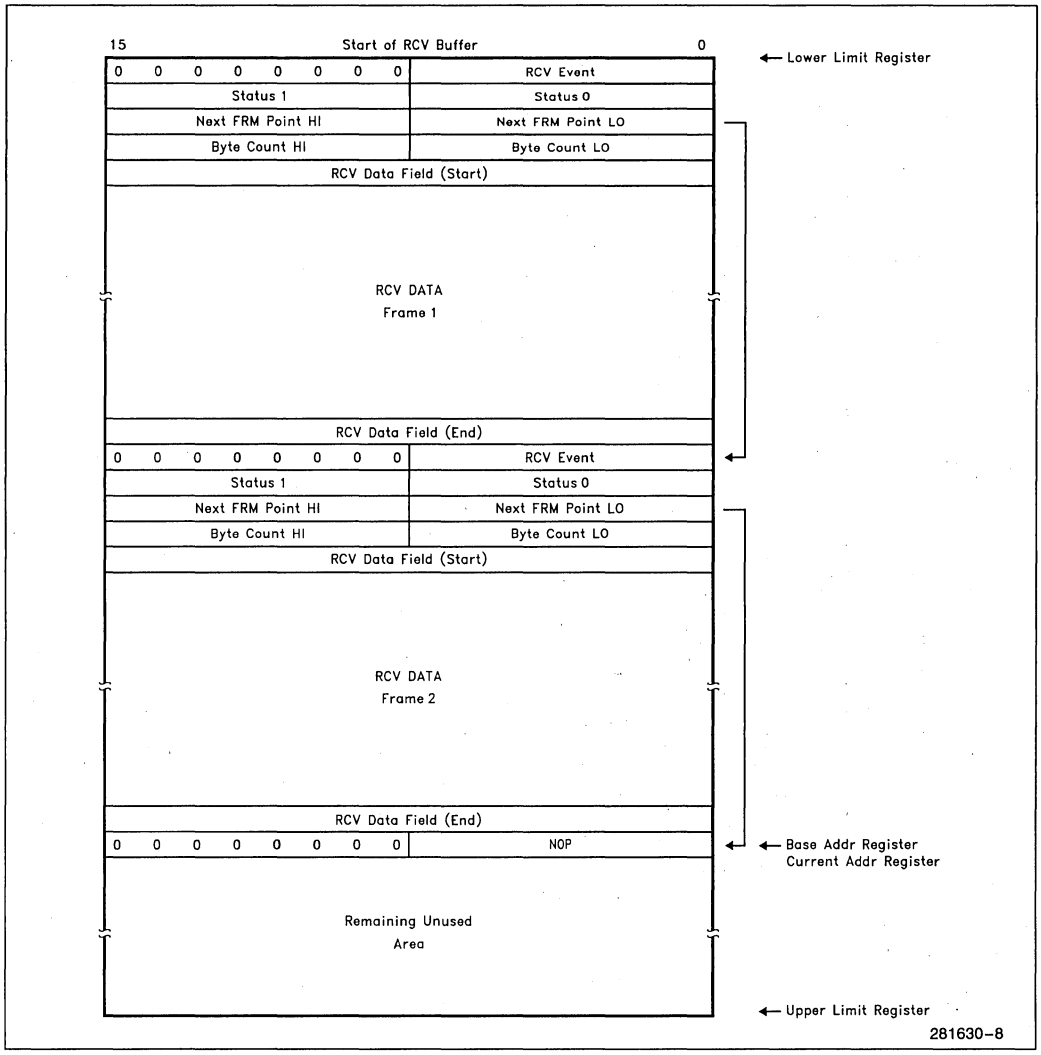


Figure 8-1. 82595TX RCV Memory Structure (16-Bit)

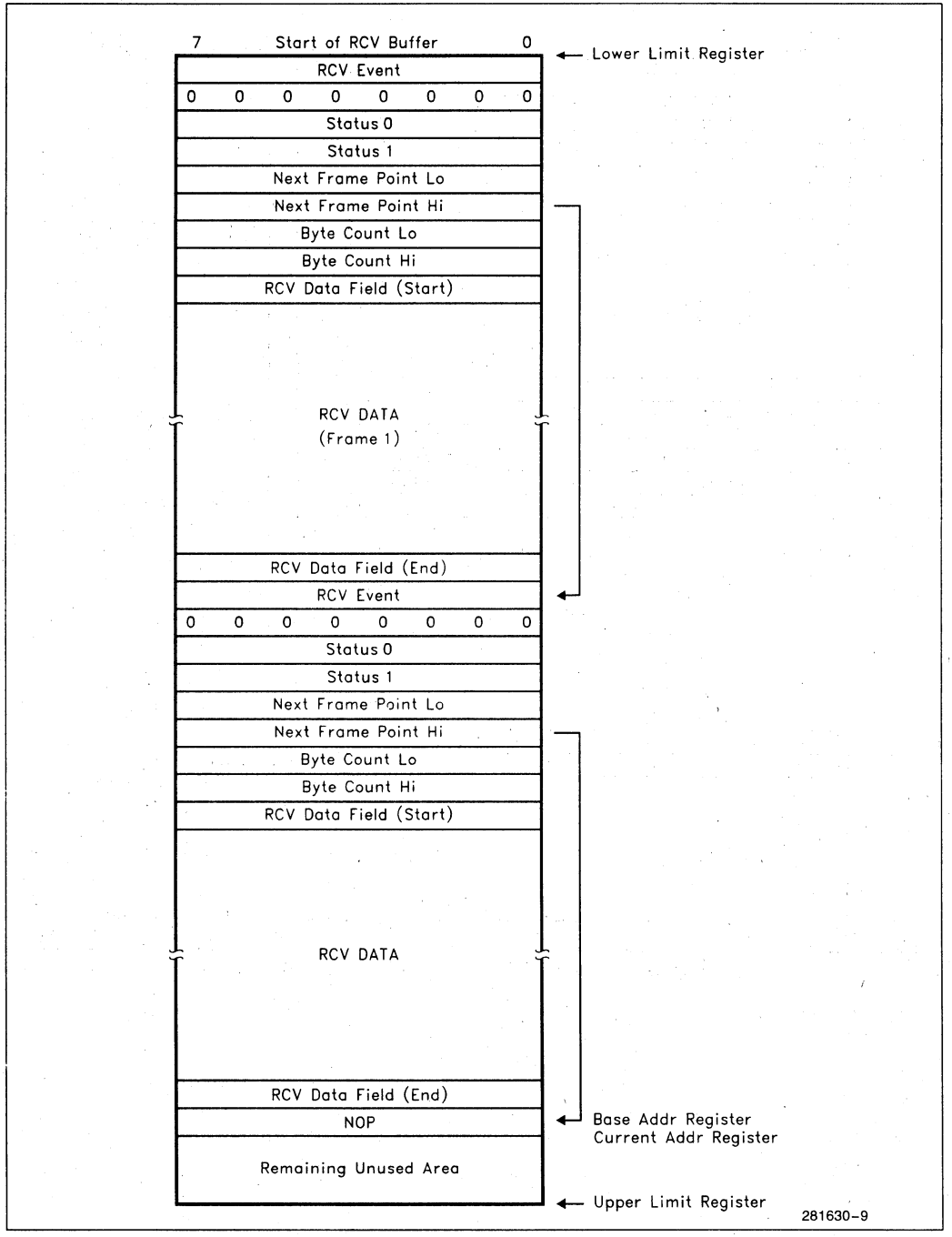


Figure 8-2. 82595TX RCV Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 8-3. In a 16-bit wide interface, these two bytes will combine to form one word. The 82595TX provides this field for each incoming frame.

8.2 RCV Ring Buffer Operation

The 82595TX RCV Ring Buffer operation is illustrated in Figure 8-4. The 82595TX copies received frames sequentially into the RCV Buffer area of the local memory. The CPU processes these frames by copying the frames from the local memory. After a frame is processed, the CPU updates the 82595TX's Stop Register to point to the last location processed. This indicates that the RCV Buffer memory which precedes the value programmed in the Stop Register is now free area (it has been processed by the CPU). When the 82595TX reaches the end of the RCV Buffer (the Upper Limit Register value) it will now wrap around back to the beginning of the buffer, and continue to copy RCV frames into the buffer, beginning at the value pointed to by the Lower Limit Register. The 82595TX will continue to copy frames into the RCV Buffer area as long as it does not reach the address pointed to by the Stop Register (if this does occur, the 82595TX stops copying the frames into memory and issues an Interrupt to the CPU). As the CPU processes additional incoming frames, the Stop Register value continues to be moved. This action allows the CPU to keep ahead of the incoming frames and allows the Ring Buffer to be continually recycled as the memory space consumed by an incoming frame is reused as that frame is processed.

7	6	5	4	3	2	1	0	
SRT FRM	X	X	1	X	X	IA MCH	RCLD	Status 0
TYP/$\overline{\text{LEN}}$	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR RN	Status 1

Figure 8-3. RCV Status Field

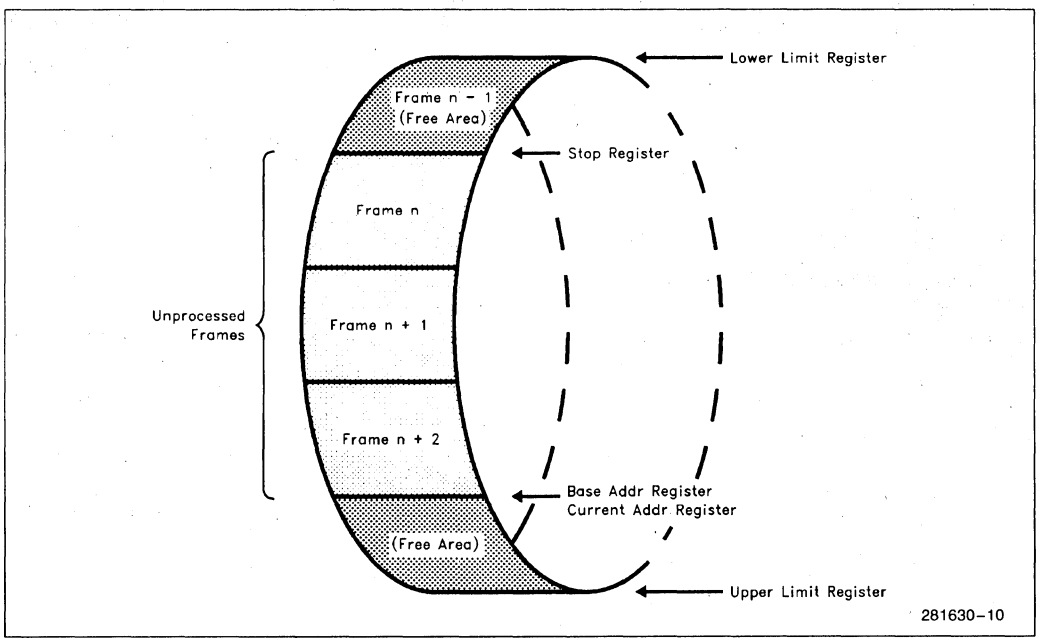


Figure 8-4. 82595TX RCV Ring Buffer Operation

9.0 SERIAL INTERFACE

The 82595TX's serial interface subsystem incorporates all the active circuitry required to interface the 82595TX to 10BASE-T networks or to the attachment unit (AUI) interface. It includes on-chip AUI and TPE drivers and receivers as well as Manchester Encoder/Decoder and Clock Recovery circuitry. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also be interfaced to a transceiver to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595TX automatically enables either the AUI or TPE interface, depending on which medium is active. This automatic selection can be overridden by software configuration. The TPE interface also features a polarity fault detection and correction circuit which will detect and correct a polarity error on the twisted pair wire, the most common wiring fault in twisted pair networks.

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ±0.01% clock required by the IEEE 802.3 specification.

We recommend that a crystal that meets the following specifications be used:

- Quartz Crystal
- 20.00 MHz ±0.002% at 25°C
- Accuracy ±0.005% over Full Operating Temperature, 0°C to +70°C
- Parallel resonant with 20 pF Load Fundamental Mode

Several vendors have such crystals; either off-the-shelf or custom-made. Two possible vendors are:

1. M-Tron Industries, Inc.
   Yankton, SD 57078
   Specifications:
   Part No. HC49 with 20 MHz, 50 PPM over 0°C to +70°C, and 20 pF fundamental load.
2. Crystek Corporation
   100 Crystal Drive
   Ft. Myers, FL 33907
   Part No. 013212

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics; therefore, it is advisable to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 pF and 35 pF.

An external 20 MHz MOS-level clock may be applied to pin X1, if pin X2 is left floating.

A summary of the 82595TX's serial interface subsections functions is shown below:

- **Manchester Encoder/Decoder and Clock Recovery**
- **Diagnostic Loopback**
- **Reset-Low-Power Mode**
- **Network Status Indicators**
- **Defeatable Jabber Timer**
- **User Test Modes**
- **Complies with IEEE 802.3 AUI Standard**
  - **— Direct Interface to AUI Transformers**
  - **— On-Chip AUI Squelch**
- **Complies with IEEE 802.3 10BASE-T for Twisted Pair Ethernet**
  - **— Selectable Polarity Detection and Correction**
  - **— Direct Interface to TPE Analog Filters**
  - **— On-Chip TPE Squelch**
  - **— Defeatable Link Integrity for Pre-Standard Networks**
  - **— Supports 4 LEDs (Link Integrity, Activity, AUI/BNC DIS and Polarity Correction)**

10.0 APPLICATION NOTES

This section is intended to provide Ethernet LAN designers with a basic understanding of how the 82595TX is used in a buffered LAN design.

10.1 Bus Interface

The 82595TX Bus Interface unit integrates the interface to both an ISA compatible bus and a PCMCIA rev 2.0 bus. Selection of the desired bus interface is done by strapping the PCMCIA/ISA pin accordingly. Two 74ALS245 transceivers are used to buffer the 82595TX's data bus, with the 82595TX providing the control over the transceivers. The data bus is not buffered in a PCMCIA design. The 82595TX also provides the complete control and address interface to the host system bus. When the ISA bus interface is selected, it implements the complete ISA bus protocol. When PCMCIA interface is selected, the complete PCMCIA bus interface protocol is implemented.

10.2 Local Memory Interface

The 82595TX's local memory interface includes a DMA unit which controls data transfers between the 82595TX and the local memory DRAM. The 82595TX can support up to 64 Kbytes of local DRAM.

The 82595TX provides address decoding and control to allow access to an external Boot EPROM or a FLASH. Addition of a Boot EPROM or FLASH to an ISA solution is optional. The FLASH is always contained as part of a PCMCIA solution. The 82595TX also supports a separate IA PROM if one is desired. For this example, the IA is assumed to be stored in the serial EEPROM for the ISA solution and in the FLASH for the PCMCIA solution.

10.3 EEPROM Interface (ISA Only)

The 82595TX provides a complete interface to a serial EEPROM for ISA adapter designs. For ISA motherboard designs and PCMCIA designs, the EEPROM is not required. The EEPROM is used to store configuration information such as Memory and IO Mapping Window, Interrupt line selection, Plug N' Play resource data local bus width, etc. The EEPROM is used to replace jumper blocks which previously contained this type of information. The 82595TX also contains an optional jumper interface (J0–J2). These jumpers can be used to select the IO mapping window of the solution. In the case of this design, the jumper block is grounded (disabled) with the IO mapping window being contained in the EEPROM.

10.4 Serial Interface

The 82595TX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 10BASE5 interface. The AUI port can also be interfaced to a transceiver device on the adapter to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595TX automatically enables either the AUI or TPE interface, depending on which medium is connected to the chip. This automatic selection can be overridden by software configuration.

10.4.1 AUI CIRCUIT

When used in conjunction with pulse transformers, the 82595TX provides a complete IEEE 802.3 AUI interface. In order to meet the 16V fault tolerance specification of IEEE 802.3, a pulse transformer is recommended. The transformer should be placed between the TRMT, RCV, and CLSN pairs of the 82595TX and the DO, DI, and CI pairs of the AUI (DB-15) connector. The pulse transformer should have the following characteristics:

- 75 μH minimum inductance (100 μH recommended)
- 2000V isolation between the primary and secondary windings
- 2000V isolation between the primaries of separate transformers
- 1:1 Turns ratio

The RCV and CLSN input pairs should each be terminated by 78.7Ω $\pm$1% resistors.

10.4.2 TPE CIRCUIT

The 82595TX provides the line drivers and receivers needed to directly interface to the TPE analog filter network. The TPE receive section requires a 100Ω termination resistor, a filter section (filter, isolation transformer, and a common mode choke) as described by the 10BASE-T 802.3i-1990 specification.

The TPE transmit section is implemented by connecting the 82595TX's four TPE outputs (TDH, $\overline{\text{TDH}}$, TDL, $\overline{\text{TDL}}$) to a resistor summing network to form the differential output signal. The parallel resistance of R5 and R6 sets the transmitters maximum output voltage, while the difference (R5 − R6)/R5 + R6), is used to reduce the amplitude of the second half of the fat bit (100 ns) to a predetermined level. This predistortion reduces line overcharging, a major source of jitter in the TPE environment. The output of the summing network is then fed into the above

mentioned filter and then to the 10BASE-T connector (RJ-45). Analog Front End solutions can be purchased in a single-chip solution from several manufacturers. The solution described in this data sheet uses the Pulse Engineering (PE65434) AFE.

10.4.3 LED CIRCUIT

The 82595TX's internal LED drivers support four LED indicators displaying node status and activity (i.e., Transmit data, receive data, collisions, link integrity, polarity correction, and port (TPE/AUI). To implement the LED indicators, connect the LED driver output to an LED in series with a 510Ω resistor tied to V_{CC}. Each driver can sink up to 10 mA of current with an output impedance of less than 50Ω.

10.5 Layout Guidelines

10.5.1 GENERAL

The analog section, as well as the entire board itself, should conform to good high-frequency practices and standards to minimize switching transients and parasitic interaction between various circuits. To achieve this, follow these guidelines:

Make power supply and ground traces as thick as possible. This will reduce high-frequency cross coupling caused by the inductance of thin traces.

Connect logic and chassis ground together.

You must connect all V_{CC} pins to the same power supply and all V_{SS} pins to the same ground plane. Use separate decoupling and noise conditions per power-supply/ground pin.

Close signal paths to ground as close as possible to their sources to avoid ground loops and noise cross coupling.

Use high-loss magnetic beads on power supply distribution lines.

10.5.2 CRYSTAL

The crystal should be adjacent to the 82595TX and trace lengths should be as short as possible. the X1 and X2 traces should be symmetrical.

10.5.3 82595TX ANALOG DIFFERENTIAL SIGNALS

The differential signals from the 82595TX to the transformers, analog front end, and the connectors should be symmetrical for each pair and as short as possible.

As a general rule, the trace widths should be one to three times the distance between the PCB layers to eliminate excessive trace inductance.

The differential signals should also be isolated from the high speed logic signals on the same layer as well as on any sublayers of the PCB.

Group each of the circuits together, but keep them separate from each other. Separate their grounds.

In layout, the circuitry from the connectors to the filter network should have the ground and power planes removed from beneath it. This will prevent ground noise from being induced into the analog front end.

All trace bends should not exceed 45 degrees.

10.5.4 DECOUPLING CONSIDERATIONS

Four 0.1 μF ceramic capacitors should be used. Place one on each side in the center of the I.C. (V_{CC} pins 23, 51, 89, 125 are recommended) adjacent to the 82595TX. Connect the capacitors directly to the V_{CC} pins on the 82595TX and then directly to the ground plane. In addition to the 0.1 μF capacitors, a 10 μF tantalum should be used near one of the 82595TX's V_{CC} pins. The proximity of this capacitor to the 82595TX is not as critical as in the case of the 0.1 μF capacitors. Placement of this capacitor within approximately one inch of the 82595TX is recommended.

11.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

11.1 Absolute Maximum Ratings

Case Temperature under Bias .....0°C to +85°C

Storage Temperature .....−65°C to +140°C

All Output and Supply Voltages .....−0.5V to +7V

All Input Voltages .....−1.0V to +6.0V(1)

Further information on the quality and reliability of the 82595TX may be found in the *Components Quality and Reliability Handbook*, Order Number 210997.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

1

Table 11-1. D.C. Characteristics (T_C = 0°C to +85°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input LOW Voltage (TTL)	−0.3	+0.8	V	
V_{IH}	Input HIGH Voltage (TTL)	2.0	V_{CC} + 0.3	V	
$V_{IH(JUMPR)}$	Input HIGH Voltage (Jumpers)	3.0	V_{CC} + 0.3	V	
V_{OL1}	Output LOW Voltage(11)		0.45	V	I_{OL} = 2 mA
V_{OL2}	Output LOW Voltage(11)		0.45	V	I_{OL} = 6 mA
V_{OL3}	Output LOW Voltage(11)		0.45	V	I_{OL} = 12 mA
V_{OL4}	Output LOW Voltage(11)		0.45	V	I_{OL} = 17 mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −1 mA
V_{OL} (LED)(2)	Output Low Voltage		0.45	V	I_{OL} = 10 mA
V_{OH} (LED)	Output High Voltage	3.9		V	I_{OH} = −500 µA
I_{LP}	Leakage Current, Low Power Mode(3)		±10	µA	$0 \le V_I \le V_{CC}$
R_{DIFF}	Input Differential-Resistance(4)	10		KΩ	DC
V_{IDF} (TPE)(5)	Input Differential Accept Input Differential Reject	±0.5	±3.1 ±0.3	V_P V_P	5 MHz ≤ f ≤ 10 MHz
R_S (TPE)(6)	Output Source Resistance	6	13	Ω	$\|I_{LOAD}\|$ = 25 mA
V_{IDF} (AUI)(7)	Input Differential Accept Input Differential Reject	±0.3	±1.5 ±0.16	V_P V_P	
V_{ICM} (AUI)	AC Input Common Mode		±0.5 ±0.1	V_P V_P	f ≤ 40 KHz 40 KHz ≤ f ≤ 10 MHz
V_{ODF} (AUI)(8)	Output Differential Voltage	±0.45	±1.2	V	
I_{OSC} (AUI)	AUI Output Short Circuit Current		±150	mA	Short Circuit to V_{CC} or GND
VU (AUI)	Output Differential Undershoot		−100	mV	
V_{ODI} (AUI)	Differential Idle Voltage(9)		40	mV	
I_{CC}	Power Supply Current		90	mA	
I_{CCPD}	Power Supply Current– Power Down Mode		1	mA	
C_{IN}(10)	Input Capacitance		10	pF	@ f = 1 MHz

NOTES:
1. The voltage levels for RCV and CLSN pairs are −0.75V to +8.5V.
2. LED Pins: ACTLED, TPE_BNC_$\overline{AUI}$, POLED, LILED.
3. Pins: ACTLED, TPE_BNC_$\overline{AUI}$, POLED, LILED.
4. Pins: RD to $\overline{RD}$, RCV to $\overline{RCV}$ and CLNS to $\overline{CLSN}$.
5. TPE input pins: RD and $\overline{RD}$.
6. TPE output pins: TDH, $\overline{TDH}$, TDL and $\overline{TDL}$, R_S measure V_{CC} or V_{SS} to pin.
7. AUI input pins: RCV and CLSN pairs.
8. AUI output pins: TPMT pair.
9. Measured 8.0 µs after last positive transition of data packet.
10. Characterized, not tested.
11. V_{OL1} is pins SD_{0-15}, $\overline{RAS}$, $\overline{CAS}$, EEPROMCS, $\overline{IAPROMCS}$, $\overline{BOOTCS}$, $\overline{DIRH}$, and $\overline{DIRL}$. V_{OL2} is pins $MDATA_{0-3}$, $MADDR_{0-8}$, TDO, $\overline{LWE}$, $\overline{SBHE}$, and $\overline{SMOUT}$. V_{OL3} is pins IOCHRDY and INT_{0-4}. V_{OL4} is $\overline{IOCS16}$.

11.1.1 PACKAGE THERMAL SPECIFICATIONS

The 82595TX is specified for operation when case temperature is within the range of 0°C to 85°C. The case temperature may be measured in any environment to determine whether the 82595TX is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from the θ_{JA} and the θ_{JC} from the following equations:

$$T_J = T_C + P^*\theta_{JC}$$
$$T_A = T_J - P^*\theta_{JA}$$
$$T_C = T_A + P^*\{\theta_{JA} - \theta_{JC}\}$$

θ_{JA} and θ_{JC} values for the 144 tQFP package are as follows:

Thermal Resistance (°C/Watt)

θ_{JC}	θ_{JA} – VS – Airflow ft/min (m/Sec)	
	0 (0)	200 (1.01)
17	48	38

11.2 A.C. Timing Characteristics

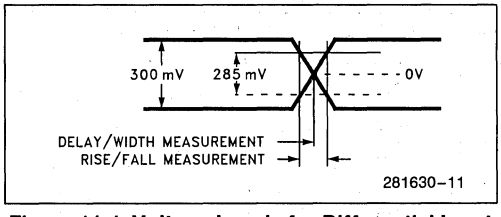


Figure 11-1. Voltage Levels for Differential Input Timing Measurements (RCV and CLSN Pairs)

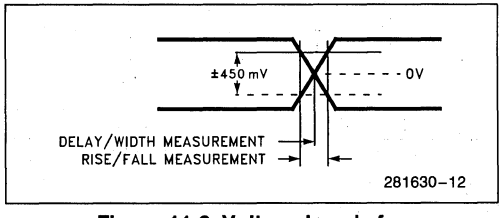


Figure 11-2. Voltage Levels for TDH, TDL, $\overline{TDH}$ and $\overline{TDL}$

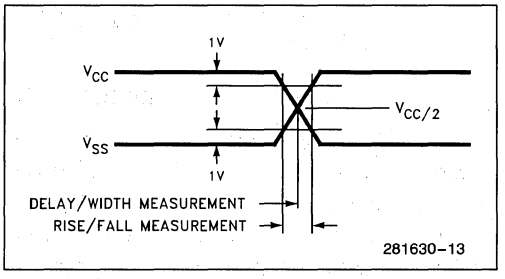


Figure 11-3. Voltage Levels for TRMT Pair Output Timing Measurements

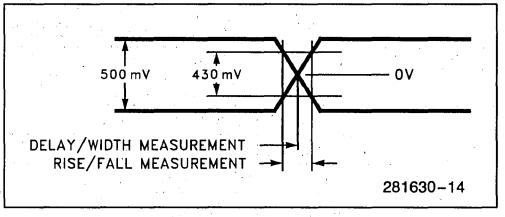


Figure 11-4. Voltage Levels for Differential Input Timing Measurements (RD Pair)

11.3 A.C. Measurement Conditions

1. T_C = 0°C to +85°C, V_{CC} = 5V ±5%
2. The signal levels are referred to in Figures 1, 2, 3 and 4.
3. A.C. Loads:
   a) AUI Differential: a 10 pF total capacitance from each terminal to ground and a load resistor of 78Ω ±1% in parallel with a 27 μH ±5% inductor between terminals.
   b) TPE: 20 pF total capacitance to ground.

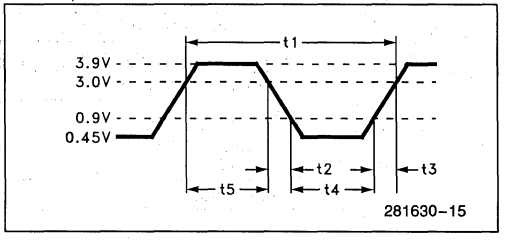


Figure 11-5. X1 Input Voltage Levels for Timing Measurements

Table 11-2. Clock Timing

Symbol	Parameter	Min	Max	Unit
t1	X1 Cycle Time	49.995	50.005	ns
t2	X1 Fall Time		5	ns
t3	X1 Rise Time		5	ns
t4	X1 Low Time	15		ns
t5	X1 High Time	15		ns

11.4 ISA Interface Timing

Table 11-3. ISA 16-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1a	BALE Active to Inactive	50		ns	
T2a	BALE Active from Command Inactive	35		ns	
T3a	AEN Valid to Falling Edge of BALE	20		ns	Applies for Early IOCHRDY
T4a	AEN Valid to I/O Command Active	100		ns	
T5a	AEN Valid from I/O Command Inactive	30		ns	
T6a	SA Valid to Falling BALE	20		ns	Applies for Early IOCHRDY
T7a	SA to CMD Active	63		ns	
T8a	SA Valid Hold from CMD Inactive	42		ns	
T9a	Valid SA to $\overline{\text{IOCS16}}$ Active		100	ns	
T10a	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T11a	CMD Active to Inactive	125		ns	
T12a	CMD Inactive to Active	92		ns	*Before* I/O Command
T13a	Active CMD to Valid IOCHRDY		18	ns	
T14a	IOCHRDY Inactive Pulse		12	μs	
T15a	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T16a	DATA Driven from READ CMD Active	0		ns	
T17a	Valid READ Data from CMD Active		54	ns	Applies to Standard Cycles Only
T18a	Valid READ Data from IOCHRDY Active		42	ns	Applies to Ready Cycles Only
T19a	READ Data Hold from CMD Inactive	0		ns	
T20a	READ CMD Inactive to Data Tristate		30	ns	
T21a	CMD to WRITE Data Active		62	ns	
T22a	WRITE Data Hold from CMD Inactive	25		ns	
T23a	WRITE CMD Inactive to Data Tristate		30	ns	
T24a	IOCHRDY Inactive to CMD Active	15		ns	Applies to Early IOCHRDY
T25a	BALE Inactive to CMD Active	55		ns	Applies to Early IOCHRDY
T26a	READ CMD Active to $\overline{\text{DIRx}}$ Active		34	ns	
T27a	READ CMD Inactive to $\overline{\text{DIRx}}$ Inactive		15	ns	

Table 11-4. ISA 8-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1b	BALE Active to Inactive	50		ns	
T2b	BALE Active from Command Inactive	35		ns	
T3b	AEN Valid to Falling Edge of BALE	20		ns	Applies to Early IOCHRDY
T4b	AEN Valid to I/O Command Active	100		ns	
T5b	AEN Valid from I/O Command Inactive	30		ns	
T6b	SA Valid to Falling BALE	20		ns	Applies to Early IOCHRDY
T7b	SA to CMD Active	63		ns	
T8b	SA Valid Hold from CMD Inactive	42		ns	
T9b	Valid SA to $\overline{\text{IOCS16}}$ Active		100	ns	
T10b	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T11b	CMD Active to Inactive	125		ns	
T12b	CMD Inactive to Active	92		ns	*Before* I/O Command
T13b	Active CMD to Valid IOCHRDY		18	ns	
T14b	IOCHRDY Inactive Pulse		12	µs	
T15b	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T16b	DATA Driven from READ CMD Active	0		ns	
T17b	Valid READ Data from CMD Active		54	ns	Applies to Standard Cycles Only
T18b	Valid READ Data from IOCHRDY Active		42	ns	Applies to Ready Cycles Only
T19b	READ Data Hold from CMD Inactive	0		ns	
T20b	READ CMD Inactive to Data Tristate		30	ns	
T21b	CMD to WRITE Data Active		62	ns	
T22b	WRITE Data Hold from CMD Inactive	15		ns	
T23b	WRITE CMD Inactive to Data Tristate		30	ns	
T24b	IOCHRDY Inactive to CMD Active	15		ns	Applies to Early IOCHRDY
T25b	BALE Inactive to CMD Active	55		ns	Applies to Early IOCHRDY
T26b	READ CMD Active to $\overline{\text{DIRx}}$ Active		34	ns	
T27b	READ CMD Inactive to $\overline{\text{DIRx}}$ Inactive		15	ns	

Table 11-5. ISA 8-Bit Memory Access

Parameter	Description	Min	Max	Units	Comments
T1c	BALE Active to Inactive	50		ns	
T2c	BALE Active from Command Inactive	35		ns	
T4c	AEN Valid to Command Active	100		ns	
T5c	AEN Valid from Command Inactive	30		ns	
T7c	SA to CMD Active	63		ns	
T8c	SA Valid Hold from CMD Inactive	42		ns	
T11c	CMD Active to Inactive	125		ns	
T12c	CMD Inactive to Active	60		ns	*Before* Memory Command
T13c	Active CMD to Valid IOCHRDY		18	ns	
T14c	IOCHRDY Inactive Pulse		12	μs	
T15c	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T16c	DATA Driven from READ CMD Active	0		ns	
T18c	Valid READ Data from IOCHRDY Active		42	ns	Applies to Ready Cycles Only
T19c	READ Data Hold from CMD Inactive	0		ns	
T20c	READ CMD Inactive to Data Tristate		30	ns	
T21c	CMD to WRITE Data Active		52	ns	
T23c	WRITE CMD Inactive to Data Tristate		30	ns	
T26c	READ CMD Active to $\overline{\text{DIRx}}$ Active		34	ns	
T27c	READ CMD Inactive to $\overline{\text{DIRx}}$ Inactive		15	ns	

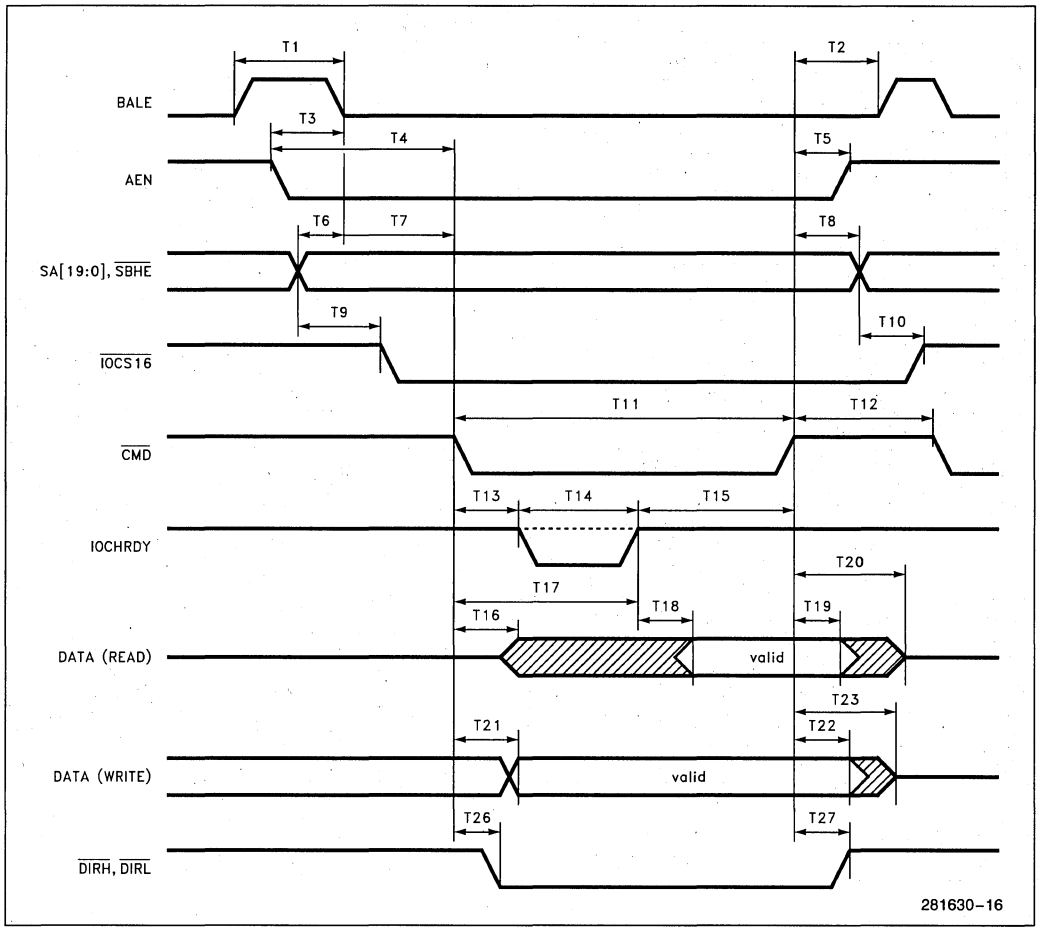


Figure 11-6. ISA-Compatible Cycle

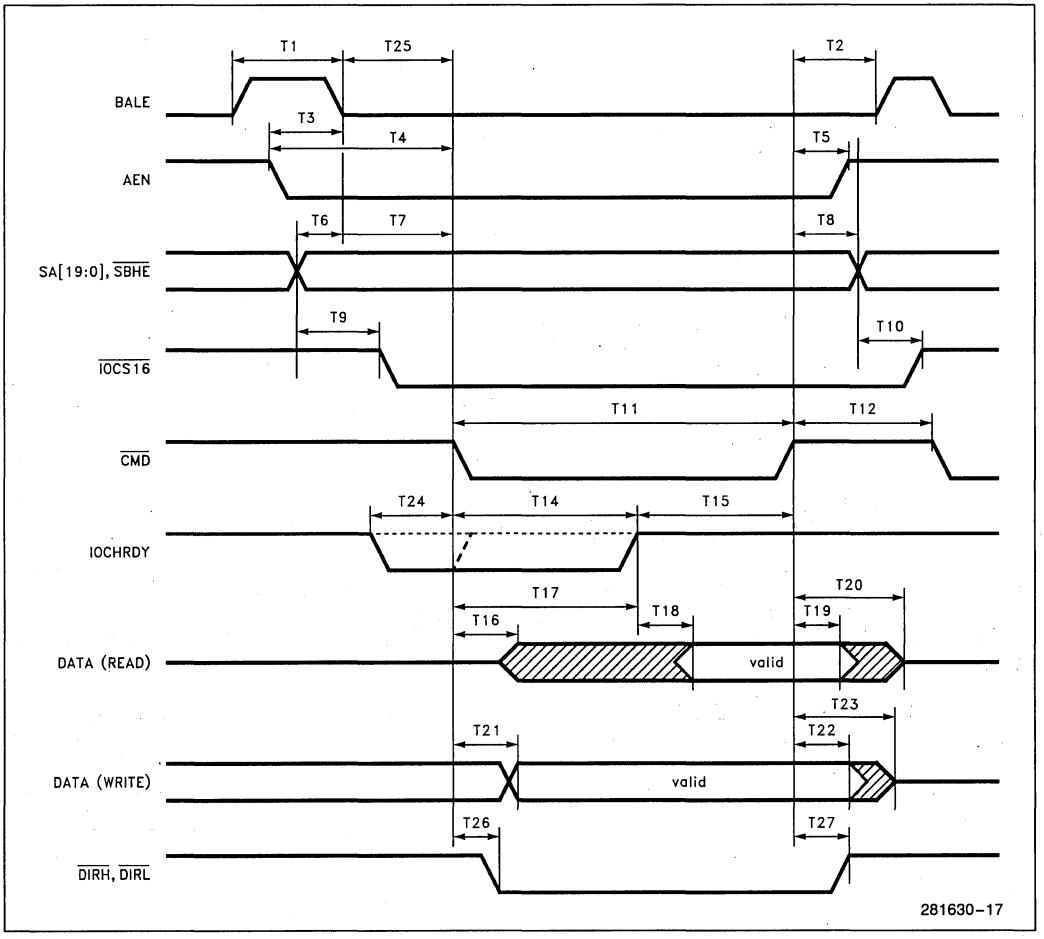


Figure 11-7. Early IOCHRDY Cycle

11.5 PCMCIA Interface Timing

Table 11-6. PCMCIA I/O Access

Parameter	Description	Min	Max	Units	Comments
T30a	ADDRESS Valid to CMD Active	70		ns	
T31a	CMD Inactive to ADDRESS Change	20		ns	
T32a	ADDRESS Valid to $\overline{IOIS16}$ Active/Inactive		35	ns	
T33a	ADDRESS Change to $\overline{IOIS16}$ Change		35	ns	
T34a	$\overline{REG}$ Active before CMD Active	5		ns	
T35a	$\overline{REG}$ Active after CMD Inactive	0		ns	
T36a	$\overline{CE}$ Active/Inactive before CMD Active	5		ns	
T37a	$\overline{CE}$ Active/Inactive after CMD Inactive	20		ns	
T38a	CMD Active to Inactive	165		ns	
T39a	$\overline{CMD}$ Active to $\overline{WAIT}$ Active/Inactive		35	ns	
T40a	$\overline{WAIT}$ Active Duration		12	µs	
T41a	$\overline{WAIT}$ Inactive to CMD Inactive	0		ns	
T42a	CMD Active to DATA READ Valid		90	ns	
T43a	$\overline{WAIT}$ Inactive to DATA READ Valid		25	ns	Applies to Extended Cycles Only
T44a	DATA READ Valid after CMD Inactive	0		ns	
T45a	DATA WRITE Valid to CMD Active	50		ns	
T46a	DATA WRITE Valid after CMD Inactive	30		ns	
T184a	Data Driven from READ CMD Active	0		ns	
T185a	READ CMD Inactive to Data Tri-State		30	ns	

Table 11-7. PCMCIA Memory Access

Parameter	Description	Min	Max	Units	Comments
T30b	ADDRESS Valid to CMD Active	30		ns	
T31b	CMD Inactive to ADDRESS Change	20		ns	
T34b	$\overline{REG}$ Inactive before CMD Active	30		ns	
T35b	$\overline{REG}$ Inactive after CMD Inactive	20		ns	
T36b	$\overline{CE}$ Active/Inactive before CMD Active	0		ns	
T37b	$\overline{CE}$ Active/Inactive after CMD Inactive	20		ns	
T38b	CMD Active to Inactive	100		ns	
T39b	$\overline{CMD}$ Active to $\overline{WAIT}$ Active/Inactive		35	ns	
T40b	$\overline{WAIT}$ Active Duration		12	µs	
T41b	$\overline{WAIT}$ Inactive to CMD Inactive	0		ns	
T43b	$\overline{WAIT}$ Inactive to DATA READ Valid		−10	ns	
T44b	DATA READ Valid after CMD Inactive	0		ns	
T45b	CMD Active to DATA WRITE Valid	125		ns	
T46b	DATA WRITE Valid after CMD Inactive	25		ns	
T184b	Data Driven from READ CMD Active	5		ns	
T185b	READ CMD Inactive to Data Tri-State		100	ns	

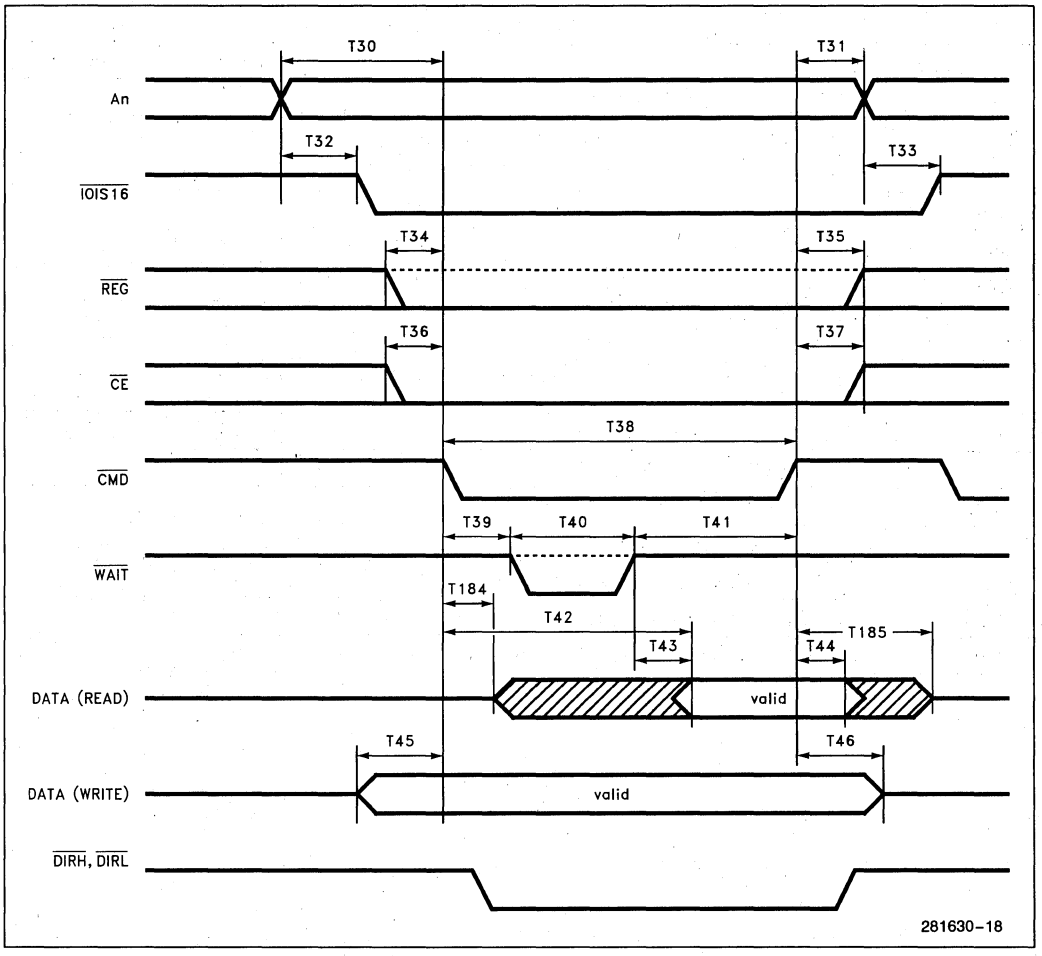


Figure 11-8. PCMCIA Cycle

11.6 Local Memory Timings

11.6.1 DRAM TIMINGS

The 82595TX supports up to 80 ns DRAM producing:

Word transfer every 400 ns.

Byte transfer every 250 ns.

Refresh cycle—200 ns.

The 82595TX supports 64K x 4 or 256K x 4 DRAM in fast page mode only. Write cycles are produced in *EARLY WRITE* mode. This eliminates using the DRAM $\overline{OE}$ signal (it must be connected to GND).

Table 11-8. DRAM—A.C. Characteristics

Symbol	Parameter	Timing		Units	Notes
		Min	Max		
T49	Access Time from $\overline{RAS}$		80	ns	
T50	Access Time from $\overline{CAS}$		30	ns	
T51	Access Time from Column Address		40	ns	
T52	$\overline{CAS}$ to Output Low Z	0		ns	
T53	Output Buffer Turn-Off Delay Time	0	40	ns	
T54	$\overline{RAS}$ Precharge Time	75		ns	
T55	$\overline{RAS}$ Pulse Width	80		ns	
T56	$\overline{RAS}$ Hold Time	30		ns	
T57	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	20		ns	
T58	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	30		ns	
T59	$\overline{CAS}$ Pulse Width	35		ns	
T60	$\overline{CAS}$ Hold Time	80		ns	
T61	Row Address Set-Up Time	0		ns	
T62	Row Address Hold Time	15		ns	
T63	Column Address Set-Up Time	0		ns	
T64	Column Address Hold Time	20		ns	
T65	Column Address Time Referenced to $\overline{RAS}$	65		ns	
T66	$\overline{RAS}$ to Column Address Delay Time	20		ns	
T67	Column Address to $\overline{RAS}$ Lead Time	40		ns	
T68	Write Command Set-Up Time	0		ns	
T69	Write Command Hold Time	15		ns	
T70	Write Command to $\overline{CAS}$ Lead Time	30		ns	
T71	D_{IN} Set-Up Time	0		ns	
T72	D_{IN} Hold Time	15		ns	
T73	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		ns	
T74	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	25		ns	
T75	Fast Page Mode Cycle Time	55		ns	
T76	Fast Page Mode $\overline{CAS}$ Precharge Time	15		ns	
T77	Random Read or Write Cycle Time	190		ns	
T78	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	100		ns	

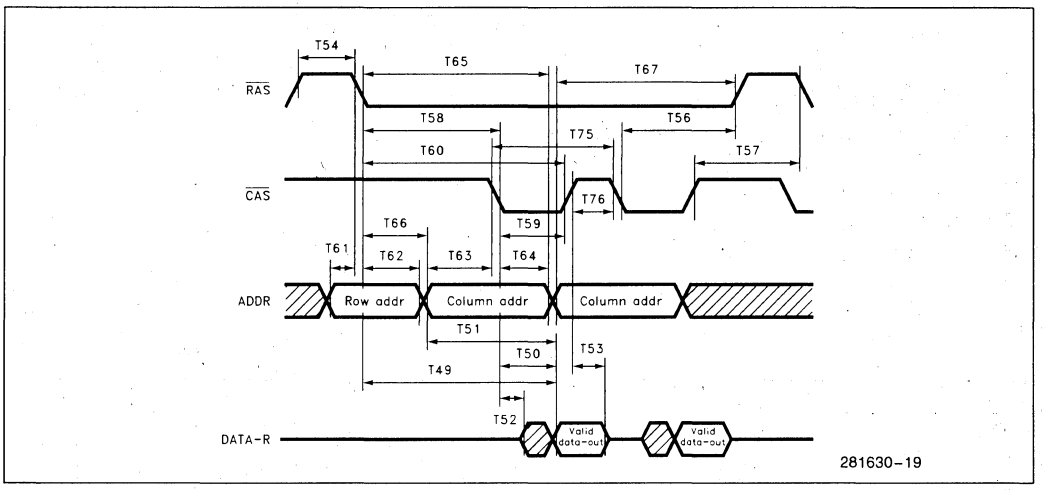


Figure 11-9. DRAM Timing Diagram: Fast Page Mode—Read Cycle

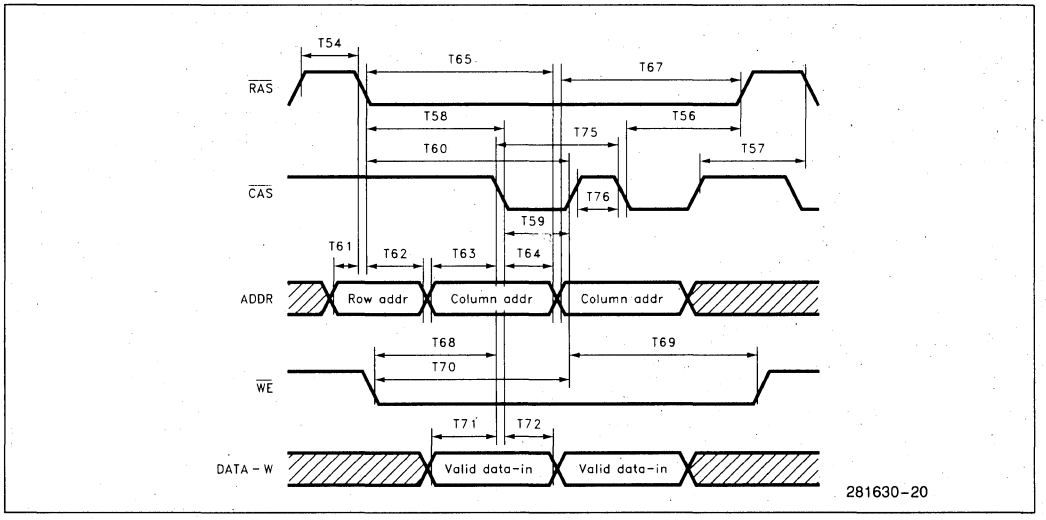


Figure 11-10. DRAM Timing Diagrams: Fast Page Mode—Write Cycle

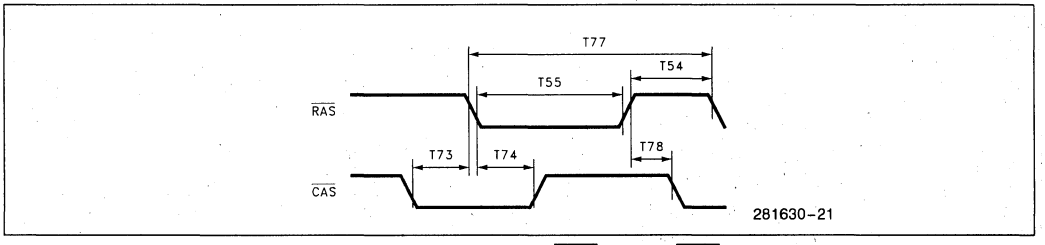


Figure 11-11. DRAM Timing Diagrams: $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

11.6.2 FLASH/EPROM TIMINGS

- The 82595TX is designed to support a FLASH or EPROM up to 200 ns access time.
- The V_{PP} signal in FLASH implementation is connected always to 12V. Thus writing to the FLASH is controlled only by the $\overline{WE}$ signal.

Table 11-9. FLASH—A.C. Characteristics

Symbol	Parameter	Min	Max	Units	Notes
T79	Address Access Time		200	ns	
T80	Chip Enable Access Time		200	ns	
T81	Output Enable Access Time		100	ns	
T82	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$	0		ns	
T84	Address Set-Up Time	0			
T85	Address Hold Time	100		ns	
T86	Chip Enable Set-Up Time before Write	15		ns	
T87	Chip Enable Hold Time	0		ns	
T88	Data Set-Up Time	60		ns	
T89	Data Hold Time	15		ns	

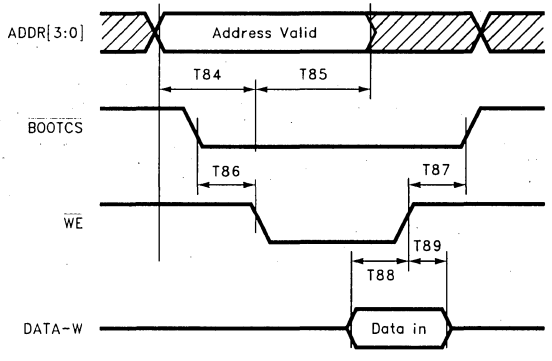


Figure 11-12. FLASH Timings—Write Cycle

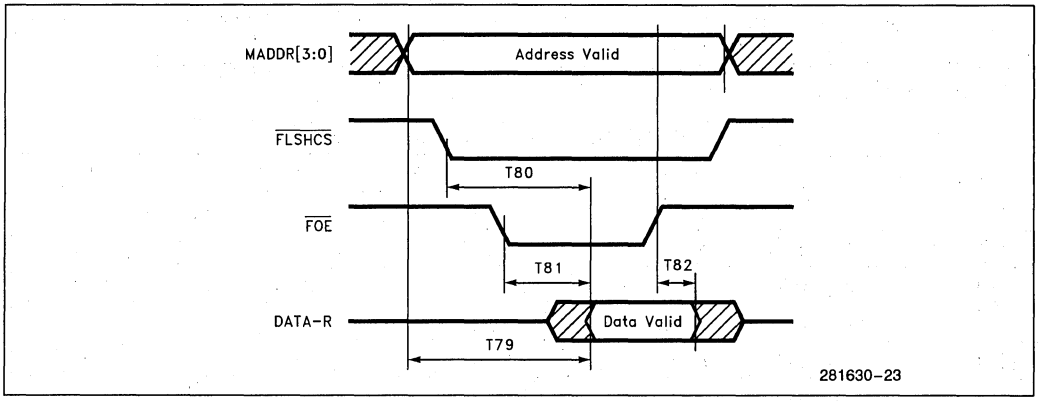


Figure 11-13. Flash Timings—Read Cycle

Table 11-10. EEPROM Timings

Symbol	Description	Min	Max	Units	Comments
T193	CS Setup Time	1.0		μs	
T194	SK High Time	3.0		μs	
T195	SK Low Time	3.0		μs	
T196	CS Hold Time	0		μs	
T197	CS Low Time	1.0		μs	
T198	DI Setup Time	0.4		μs	
T199	DI Hold Time	0.4		μs	
T200	Data Out Valid Time		0.4	μs	EEProm Restriction
T201	CS Inactive to DO Floated		0.4	μs	EEProm Restriction

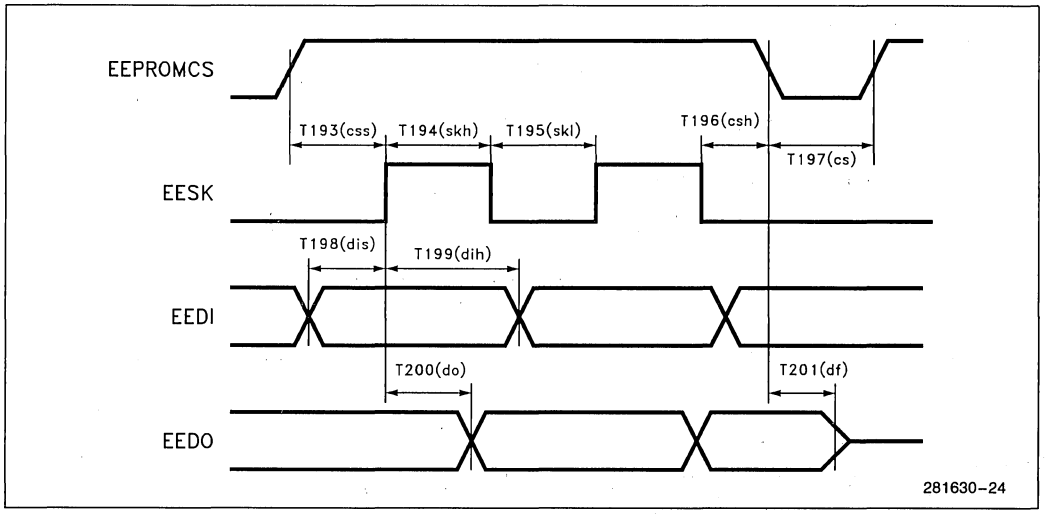


Figure 11-14. EEPROM Timings

11.6.3 IA PROM TIMINGS

*The PROM used is a TTL 32 x 8 bit.

Table 11-11. IA PROM A.C. Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
T174	Address Access Time		60	ns	
T175	Chip Enable Access Time		40	ns	

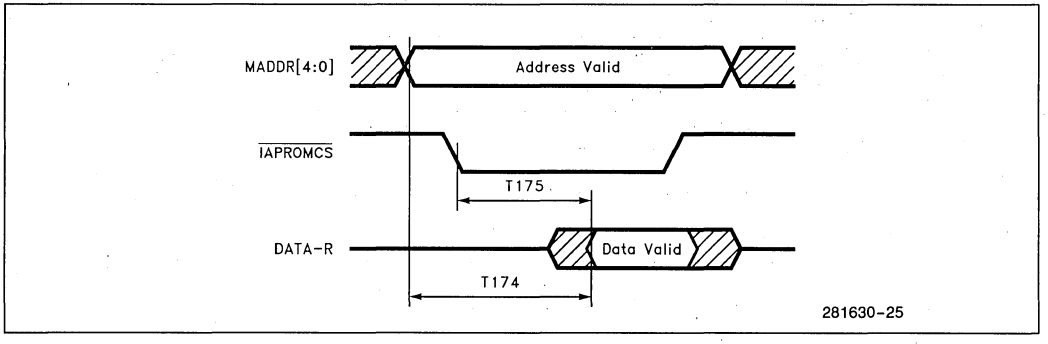
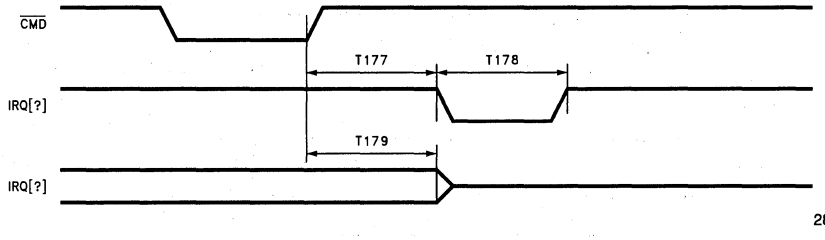


Figure 11-15. IA PROM Timings

11.7 Interrupt Timing

Table 11-12. Interrupt Timing

Parameter	Description	Min	Max	Units	Notes
T177	Interrupt Ack $\overline{CMD}$ Inactive to IRQ[4:0] Inactive		500	ns	
T178	IRQ[4:0] Inactive to IRQ[4:0] Active	100		ns	
T179	Tri-state $\overline{CMD}$ Inactive to IRQ[4:0] Tri-State		500	ns	



NOTE:
For ISA bus, IRQ is Active high.
For PCMCIA bus, IRQ is Active low.

Figure 11-16. Interrupt Timing

11.8 RESET and $\overline{SMOUT}$ Timing

General Comments

- Both signals are asynchronous signals and have minimum pulse duration specification only.
- $\overline{SMOUT}$ during Hardware power down activation.

Table 11-13. RESET and $\overline{SMOUT}$ Timing

Parameter	Description	Min	Max	Units	Notes
T180	RESET Minimum Duration	32		ms	1
T181	$\overline{SMOUT}$ Minimum Duration	100		ns	2
T182	$\overline{SMOUT}$ Activation by Power Down Command	150		ns	3
T183	$\overline{SMOUT}$ Deactivation	25		ns	3

NOTES:
1. Noise spikes of maximum TBD ns are allowed on Reset.
2. $\overline{SMOUT}$ is input.
3. $\overline{SMOUT}$ is output after configuration.

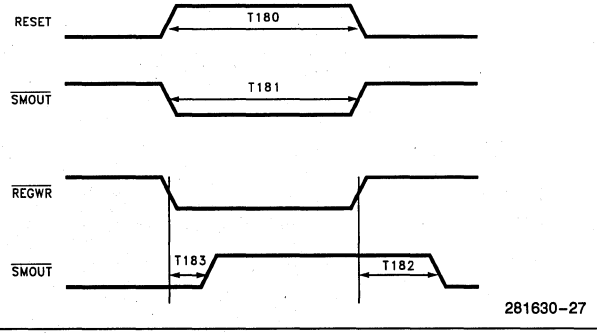


Figure 11-17. $\overline{SMOUT}$ Timing

11.9 JTAG Timing

Table 11-14. 82595TX JTAG Timing

Symbol	Parameter	Min	Max	Unit	Notes
T184	TMS Set-Up Time	15		ns	
T185	TMS Hold Time	10		ns	
T186	TDI Set-Up Time	15		ns	
T187	TDI Hold Time	10		ns	
T188	Input Signals Set-Up Time	15		ns	
T189	Input Signals Hold Time	10		ns	
T190	Outputs Valid Delay		150	ns	
T191	TDO Valid Delay		40	ns	
T192	TCK Cycle Time (Period)	100		ns	50% Duty Cycle

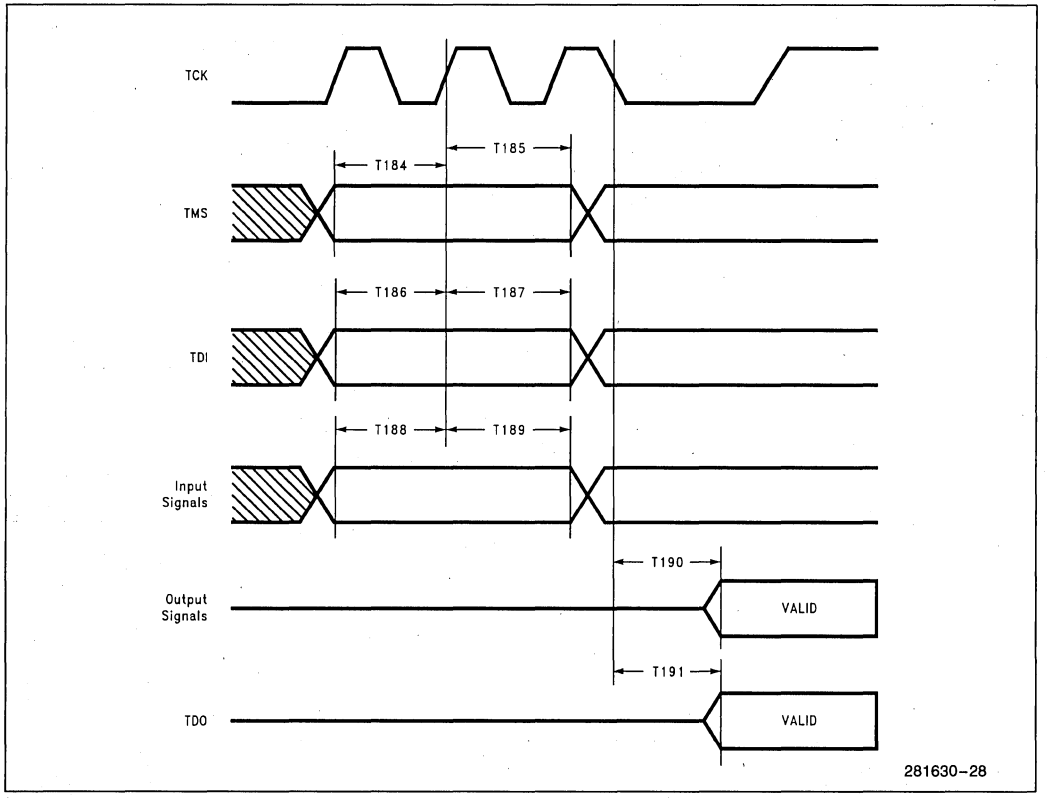
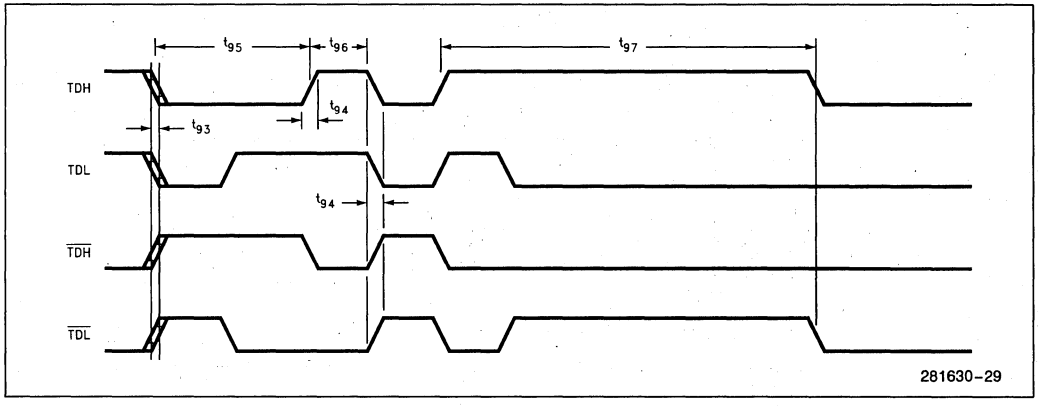


Figure 11-18. 82595TX JTAG Timing

11.10 Serial Timings

Table 11-15. TPE Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{90}	Number of TxD Bit Loss at Start of Packet			2	bits
t_{91}	Internal Steady State Propagation Delay			400	ns
t_{92}	Internal Start UP Delay			600	ns
t_{93}	TDH and TDL Pairs Edge Skew (@ $V_{CC}/2$)		1.5	3	ns
t_{94}	TDH and TDL Pairs Rise/Fall Times (@ 0.5V to V_{CC} − 0.5V)		2	5	ns
t_{95}	TDH and TDL Pairs Bit Cell Center to Center	99	100	101	ns
t_{96}	TDH and TDL Pairs Bit Cell Center to Boundary	49	50	51	ns
t_{97}	TDH and TDL Pairs Return to Zero from Last TDH	250		400	ns
t_{98}	Link Test Pulse Width	98	100	100	ns
t_{99}	Last TD Activity to Link Test Pulse	8	13	24	ms
t_{100}	Link Test Pulse to Data Separation	190	200		ns



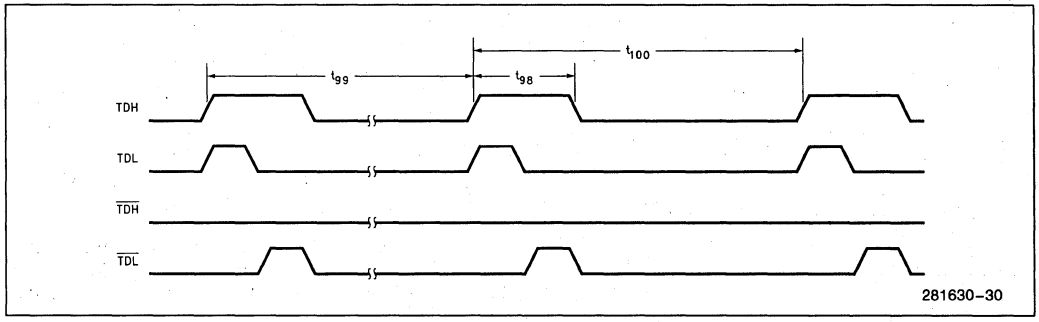


Figure 11-19. TPE Transmit Timings (Link Test Pulse)

Table 11-16. TPE Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{105}	RD to RxD Bit Loss at Start of Packet	4		19	bits
t_{106}	RD Invalid Bits Allowed at Start of Packet			1	bits
t_{107}	RD to Internal Steady State Propagation Delay			400	ns
t_{108}	RD to Internal Start Up Delay			2.4	μs
t_{109}	RD Pair Bit Cell Center Jitter			±13.5	ns
t_{110}	RD Pair Bit Cell Boundry Jitter			±13.5	ns
t_{111}	RD Pair Held High from Last Valid Position Transition	230		400	ns

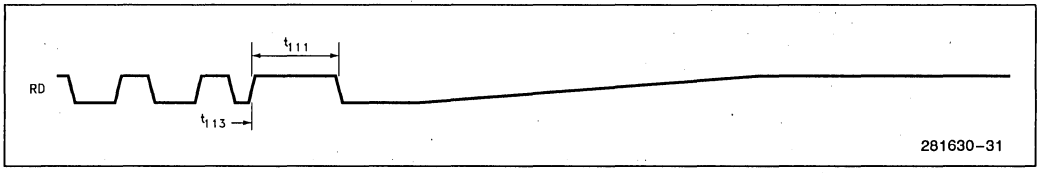


Figure 11-20. TPE Receive Timings (End of Frame)

Table 11-17. TPE Link Integrity Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{120}	Last RD Activity to Link Fault (Link Loss Timer)	50	100	150	ms
t_{121}	Minimum Received Linkbeat Separation(1)	2	5	7	ms
t_{122}	Maximum Received Linkbeat Separation(2)	25	50	150	ms

NOTES:
1. Linkbeats closer in time to this value are considered noise and rejected.
2. Linkbeats further apart in time than this value are not considered consecutive and are rejected.

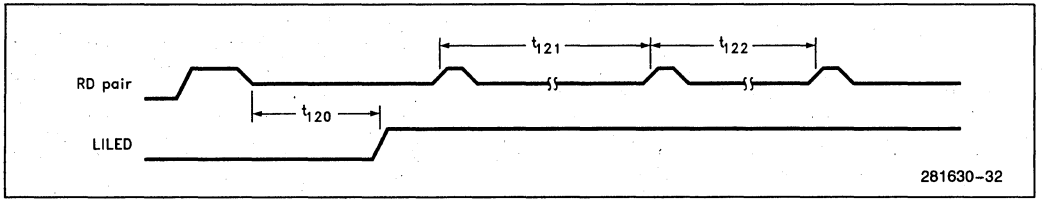


Figure 11-21. TPE Link Integrity Timings

Table 11-18. AUI Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{126}	TRMT Pair Rise/Fall Times		3	5	ns
t_{127}	Bit Cell Center to Bit Cell Center of TRMT Pair	99.5	50	100.5	ns
t_{128}	Bit Cell Center to Bit Cell Boundary of TRMT Pair	49.5	50	50.5	ns
t_{129}	TRMT Pair Held at Positive Differential at Start of Idle	200			ns
t_{130}	TRTM Pair Return to ≤40 mVp from Last Positive Transition			8.0	μs

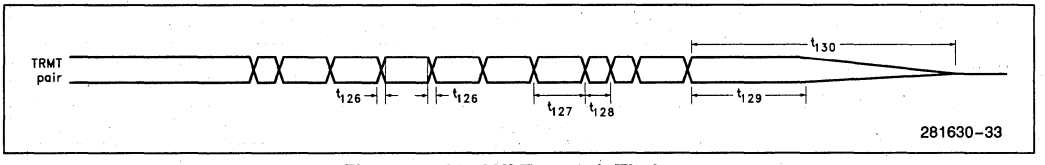


Figure 11-22. AUI Transmit Timings

Table 11-19. AUI Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{135}	RCV Pair Rise/Fall Times			10	ns
t_{136}	RCV Pair Bit Cell Center Jitter in Preamble			±12	ns
t_{137}	RCV Pair Bit Cell Center/Boundary Jitter in Data			±18	ns
t_{138}	RCV Pair Idle Time after Transmission	8			μs
t_{139}	RCV Pair Return to Zero from Last Positive Transition	160			ns

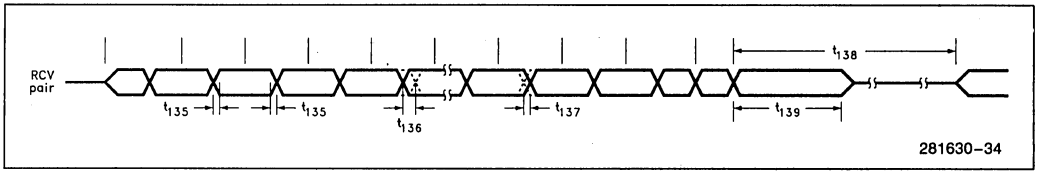


Figure 11-23. AUI Receive Timings

Table 11-20. AUI Collision Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{145}	CLSN Pair Cycle Time	80		118	ns
t_{146}	CLSN Pair Rise/Fall Times			10	ns
t_{147}	CLSN Pair Return to Zero from Last Positive Transition	160			ns
t_{148}	CLSN Pair High/Low Times	35		70	ns

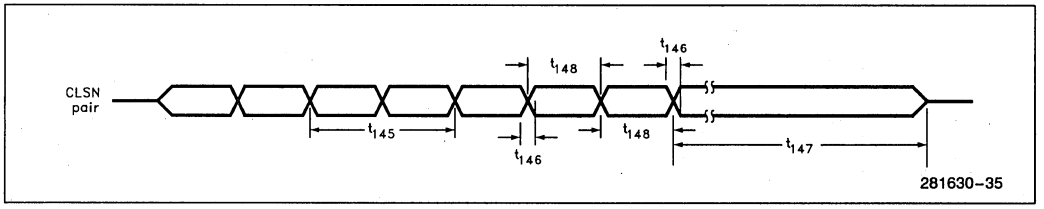


Figure 11-24. AUI Collision Timings

Table 11-21. AUI Noise Filter Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{152}	RCV Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns
t_{153}	CLSN Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns

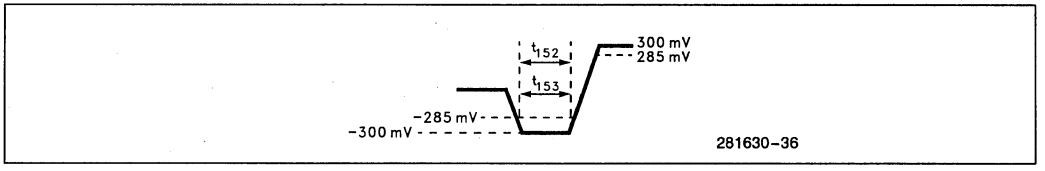


Figure 11-25. AUI Noise Filter Timings

Table 11-22. Jabber Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{165}	Maximum Length Transmission before Jabber Fault (TPE)	20	25	150	ms
t_{166}	Maximum Length Transmission before Jabber Fault (AUI)	10	13	18	ms
t_{167}	Minimum Idle Time to Clear Jabber Function	250	275	750	ms

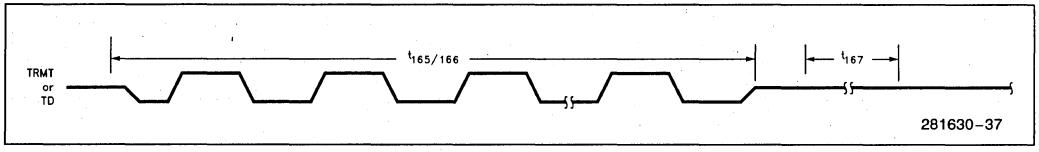


Figure 11-26. Jabber Timings

Table 11-23. LED Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{170}	ACTLED On Time	50		450	ms
t_{171}	ACTLED Off Time	50			ms
t_{172}	LILED On Time	50			ms
t_{173}	LILED Off Time	100			ms

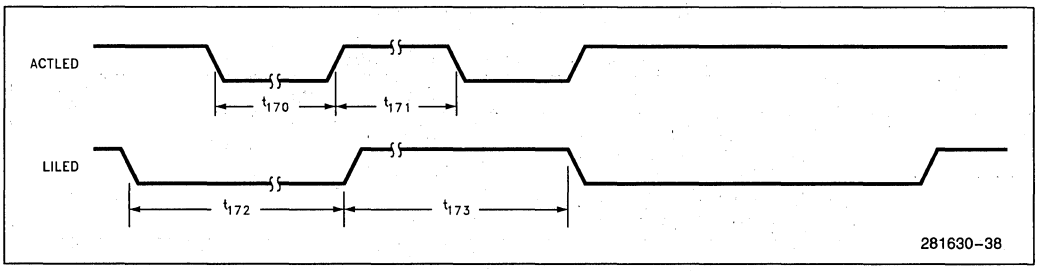


Figure 11-27. LED Timings

Additional 82595TX Documentation

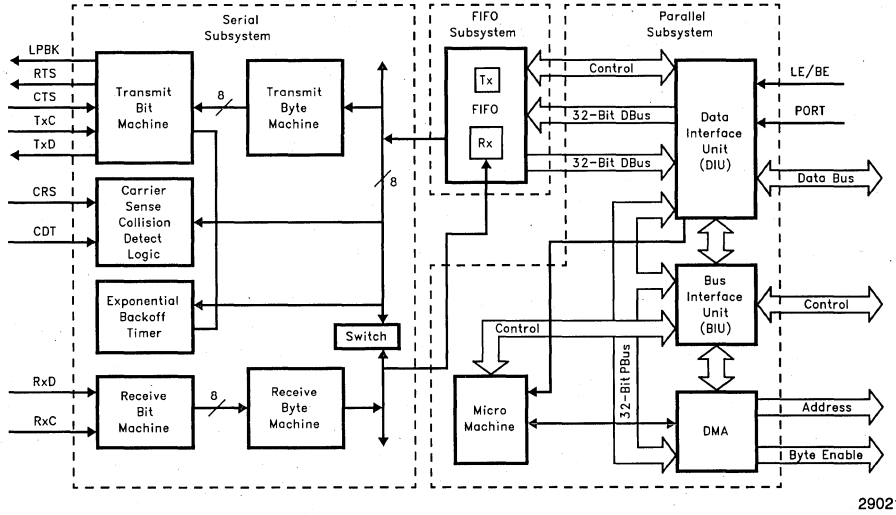
This datasheet provides complete pinout and pin definitions, and electrical specifications and timings. It also includes an overview of the various subsections listed in Figure 1. For more complete information on the 82595TX, please ask your local sales representative for the 82595TX User Manual and LAN595TX Specification. The 82595TX User Manual contains detailed information on the 82595TX feature set, including register descriptions and implementation steps for various 82595TX functions (initialization, transmission, reception). The LAN595TX Specification describes various hardware/software implementations and configuration techniques. Hardware compatible with this interface can work with software developed by Intel and other NOS vendors which conform to this specification.

82596CA
HIGH-PERFORMANCE 32-BIT LOCAL AREA NETWORK COPROCESSOR

- **Performs Complete CSMA/CD Medium Access Control (MAC) Functions—Independently of CPU**
  - **— IEEE 802.3 (EOC) Frame Delimiting**
- **Supports Industry Standard LANs**
  - **— IEEE TYPE 10BASE-T, IEEE TYPE 10BASE5 (Ethernet*), IEEE TYPE 10BASE2 (Cheapernet), IEEE TYPE 1BASE5 (StarLAN), and the Proposed Standard 10BASE-F**
  - **— Proprietary CSMA/CD Networks Up to 20 Mb/s**
- **On-Chip Memory Management**
  - **— Automatic Buffer Chaining**
  - **— Buffer Reclamation after Receipt of Bad Frames; Optional Save Bad Frames**
  - **— 32-Bit Segmented or Linear (Flat) Memory Addressing Formats**
- **Network Management and Diagnostics**
  - **— Monitor Mode**
  - **— 32-Bit Statistical Counters**
- **82586 Software Compatible**
- **Self-Test Diagnostics**
- **Optimized CPU Interface**
  - **— Optimized Bus Interface to Intel's i486™DX, i486™SX, i487™SX and 80960CA Processors**
  - **— 33 MHz, 25 MHz, 20 MHz and 16 MHz Clock Frequencies**
  - **— Supports Big Endian and Little Endian Byte Ordering**
- **32-Bit Bus Master Interface**
  - **— 106 MB/s Bus Bandwidth**
  - **— Burst Bus Transfers**
  - **— Bus Throttle Timers**
  - **— Transfers Data at 100% of Serial Bandwidth**
  - **— 128-Byte Receive FIFO, 64-Byte Transmit FIFO**
- **Configurable Initialization Root for Data Structures**
- **High-Speed, 5V, CHMOS** IV Technology**
- **132-Pin Plastic Quad Flat Pack (PQFP) and PGA Package**

(See Packaging Spec Order No. 240800-001, Package Type KU and A)

i486 is a trademark of Intel Corporation.
*Ethernet is a registered trademark of Xerox Corporation.
**CHMOS is a patented process of Intel Corporation.



290218-1

Figure 1. 82596CA Block Diagram

October 1995
Order Number: 290218-006

82596CA High-Performance 32-Bit Local Area Network Coprocessor

CONTENTS

CONTINUED

INTRODUCTION

The 82596CA is an intelligent, high-performance 32-bit Local Area Network coprocessor. The 82596CA implements the CSMA/CD access method and can be configured to support all existing IEEE 802.3 standards—TYPEs 10BASE-T, 10BASE5, 10BASE2, 1BASE5, and 10BROAD36. It can also be used to implement the proposed standard TYPE 10BASE-F. The 82596CA performs high-level commands, command chaining, and interprocessor communications via shared memory, thus relieving the host CPU of many tasks associated with network control. All time-critical functions are performed independently of the CPU, this increases network performance and efficiency. The 82596CA bus interface is optimized for Intel's i486™SX, i486™DX, i487™SX, 80960CA, and 80960KB processors.

The 82596CA implements all IEEE 802.3 Medium Access Control and channel interface functions, these include framing, preamble generation and stripping, source address generation, destination address checking, short-frame detection, and automatic length-field handling. Data rates up to 20 Mb/s are supported.

The 82596CA provides a powerful host system interface. It manages memory structures automatically, with command chaining and bidirectional data chaining. An on-chip DMA controller manages four channels, this allows autonomous transfer of data blocks (buffers and frames) and relieves the CPU of byte transfer overhead. Buffers containing errored or collided frames can be automatically recovered without CPU intervention. The 82596CA provides an upgrade path for existing 82586 software drivers by providing an 82586-software-compatible mode that supports the current 82586 memory structure. The 82586CA also has a Flexible memory structure and a Simplified memory structure. The 82596CA can address up to 4 gigabytes of memory. The 82596CA supports Little Endian and Big Endian byte ordering.

The 82596CA bus interface can achieve a burst transfer rate of 106 MB/s at 33 MHz. The bus interface employs bus throttle timers to regulate 82596CA bus use. Two large, independent FIFOs—128 bytes for Receive and 64 bytes for Transmit—tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case bus latency. The high-performance bus is capable of back-to-back transmission and reception during the IEEE 802.3 9.6-μs Interframe Spacing (IFS) period.

The 82596CA provides a wide range of diagnostics and network management functions, these include internal and external loopback, exception condition tallies, channel activity indicators, optional capture of all frames regardless of destination address (promiscuous mode), optional capture of errored or collided frames, and time domain reflectometry for locating fault points on the network cable. The statistical counters, in 32-bit segmented and linear modes, are 32-bits each and include CRC errors, alignment errors, overrun errors, resource errors, short frames, and received collisions. The 82596CA also features a monitor mode for network analysis. In this mode the 82596CA can capture status bytes, and update statistical counters, of frames monitored on the link without transferring the contents of the frames to memory. This can be done concurrently while transmitting and receiving frames destined for that station.

The 82596CA can be used in both baseband and broadband networks. It can be configured for maximum network efficiency (minimum contention overhead) with networks of any length. Its highly flexible CSMA/CD unit supports address field lengths of zero through six bytes for IEEE 802.3/Ethernet frame delimitation. It also supports 16- or 32-bit cyclic redundancy checks. The CRC can be transferred directly to memory for receive operations, or dynamically inserted for transmit operations. The CSMA/CD unit can also be configured for full duplex operation for high throughput in point-to-point connections.

The 82596 C-step incorporates several new features not found in previous steppings. The following is a summary of the 82596 C-step's new features.

- The 82596 C-step fixes Errata found in the A1 and B steppings.
- The 82596 C-step has improved AC timings over both the A and B steppings.
- The 82596 C-step has a New Enhanced Big Endian Mode where in Linear Addressing Mode, true 32-bit Big Endian functionality is achieved. New Enhanced Big Endian Mode is enabled by setting bit 7 of the SYSBUS byte. This mode is software compatible with the big endian mode of the B-step with one exception—no 32-bit addresses need to be swapped by software in the C-step. In this new mode, the 82596 C-step treats 32-bit address pointers as true 32-bit entities and the SCB absolute address and statistical counters are still treated as two 16-bit big endian entities. Not setting this mode will configure the 82596 C-step to be 100% compatible to the A1-step big endian mode.
- The 82596 C-step is hardware and software compatible to both the A1 and B steppings allowing for easy "drop-in" to current designs. Pinout and control structures remain unchanged.

The 82596CA is fabricated with Intel's reliable, 5-V, CHMOS IV (process 648.8) technology. It is available in a 132-pin PQFP or PGA package.

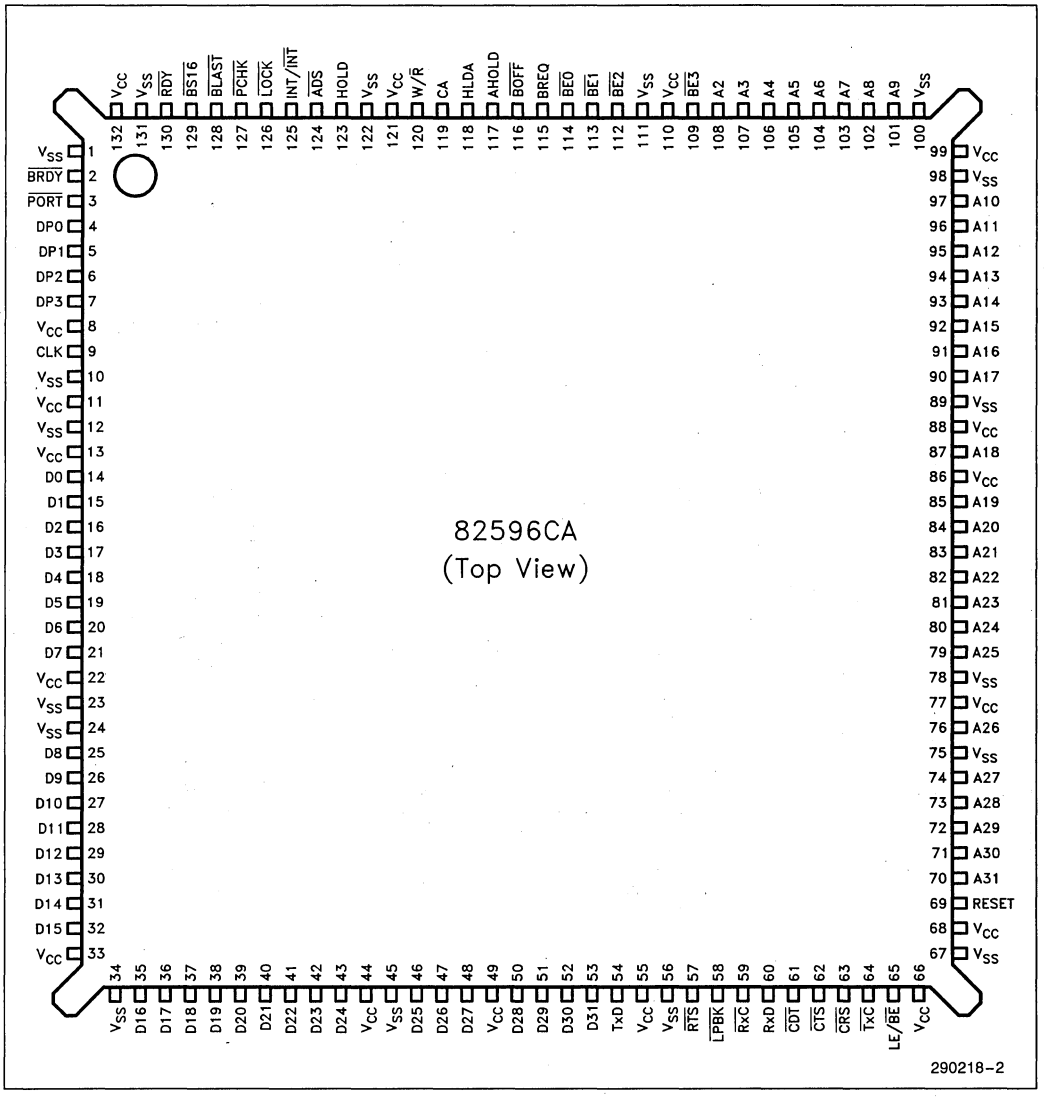


Figure 2. 82596CA PQFP Pin Configuration

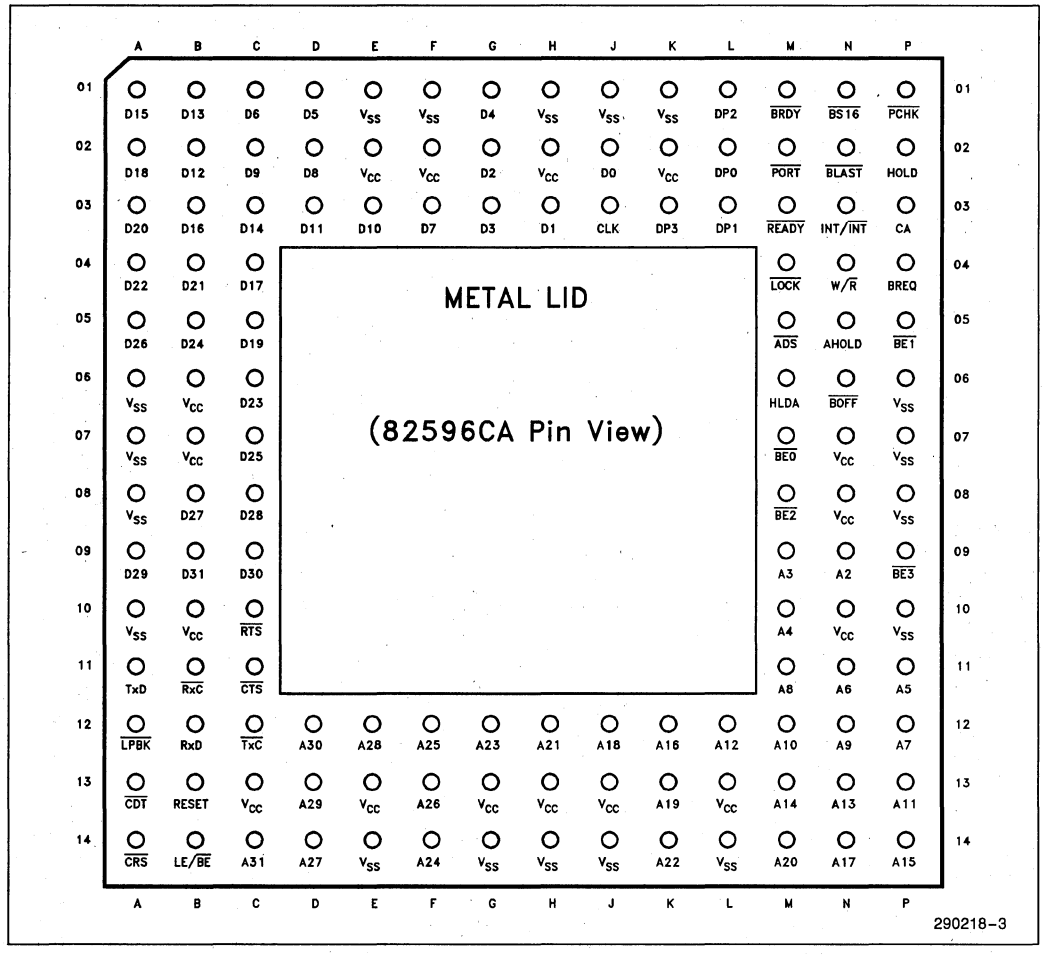


Figure 3. 82596CA PGA Pinout

82596CA PGA Cross Reference by Pin Name

Address		Data		Control		Serial Interface		V_{CC}	V_{SS}
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Pin No.	Pin No.
A2	N9	D0	J2	$\overline{ADS}$	M5	$\overline{CDT}$	A13	B6	A6
A3	M9	D1	H3	AHOLD	N5	$\overline{CRS}$	A14	B7	A7
A4	M10	D2	G2	$\overline{BE0}$	M7	$\overline{CTS}$	C11	B10	A8
A5	P11	D3	G3	$\overline{BE1}$	P5	$\overline{LPBK}$	A12	C13	A10
A6	N11	D4	G1	$\overline{BE2}$	M8	$\overline{RTS}$	C10	E2	E1
A7	P12	D5	D1	$\overline{BE3}$	P9	$\overline{RxC}$	B11	E13	E14
A8	M11	D6	C1	$\overline{BLAST}$	N2	$\overline{RxD}$	B12	F2	F1
A9	N12	D7	F3	$\overline{BOFF}$	N6	$\overline{TxC}$	C12	G13	G14
A10	M12	D8	D2	$\overline{BRDY}$	M1	TxD	A11	H2	H1
A11	P13	D9	C2	BREQ	P4			H13	H14
A12	L12	D10	E3	$\overline{BS16}$	N1			J13	J1
A13	N13	D11	D3	CA	P3			K2	J14
A14	M13	D12	B2	CLK	J3			L13	K1
A15	P14	D13	B1	DP0	L2			N7	L14
A16	K12	D14	C3	DP1	L3			N8	P6
A17	N14	D15	A1	DP2	L1			N10	P7
A18	J12	D16	B3	DP3	K3				P8
A19	K13	D17	C4	HLDA	M6				P10
A20	M14	D18	A2	HOLD	P2				
A21	H12	D19	C5	INT/$\overline{INT}$	N3				
A22	K14	D20	A3	LE/$\overline{BE}$	B14				
A23	G12	D21	B4	$\overline{LOCK}$	M4				
A24	F14	D22	A4	$\overline{PCHK}$	P1				
A25	F12	D23	C6	$\overline{PORT}$	M2				
A26	F13	D24	B5	$\overline{READY}$	M3				
A27	D14	D25	C7	RESET	B13				
A28	E12	D26	A5	W/$\overline{R}$	N4				
A29	D13	D27	B8						
A30	D12	D28	C8						
A31	C14	D29	A9						
		D30	C9						
		D31	B9						

PIN DESCRIPTIONS

<table>
<tr><th>Symbol</th><th>PQFP Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>CLK</td><td>9</td><td>I</td><td>CLOCK. The system clock input provides the fundamental timing for the 82596. It is a 1X CLK input used to generate the 82596 clock and requires TTL levels. All external timing parameters are specified in reference to the rising edge of CLK.</td></tr>
<tr><td>D0–D31</td><td>14–53</td><td>I/O</td><td>DATA BUS. The 32 Data Bus lines are bidirectional, tri-state lines that provide the general purpose data path between the 82596 and memory. With the 82596 the bus can be either 16 or 32 bits wide; this is determined by the $\overline{BS16}$ signal. The 82596 always drives all 32 data lines during Write operations, even with a 16-bit bus. D31– D0 are floated after a Reset or when the bus is not acquired.
These lines are inputs during a CPU Port access; in this mode the CPU writes the next address to the 82596 through the data lines. During $\overline{PORT}$ commands (Relocatable SCP, Self-Test, Reset and Dump) the address must be aligned to a 16-byte boundary. This frees the D_3–D_0 lines so they can be used to distinguish the commands. The following is a summary of the decoding data.
<table>
<tr><th>D0</th><th>D1</th><th>D2</th><th>D3</th><th>D31–D4</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0000</td><td>Reset</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>ADDR</td><td>Relocatable SCP</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>ADDR</td><td>Self-Test</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>ADDR</td><td>Dump Command</td></tr>
</table></td></tr>
<tr><td>DP0–DP3</td><td>4–7</td><td>I/O</td><td>DATA PARITY. These are tri-stated data parity pins. There is one parity line for each byte of the data bus. The 82596 drives them with even-parity information during write operations having the same timing as data writes. Likewise, even-parity information, with the same timing as read information, must be driven back to the 82596 over these pins to ensure that the correct parity check status is indicated by the 82596.</td></tr>
<tr><td>$\overline{PCHK}$</td><td>127</td><td>O</td><td>PARITY CHECK. This pin is driven high one clock after $\overline{RDY}$ to inform Read operations of the parity status of data sampled at the end of the previous clock cycle. When driven low it indicates that incorrect parity data has been sampled. It only checks the parity status of enabled bytes, which are indicated by the Byte Enable and Bus Size signals. $\overline{PCHK}$ is only valid for one clock time after data read is returned to the 82596; i.e., it is inactive (high) at all other times.</td></tr>
<tr><td>A31-A2</td><td>70–108</td><td>O</td><td>ADDRESS LINES. These 30 tri-stated Address lines output the address bits required for memory operation. These lines are floated after a Reset or when the bus is not acquired.</td></tr>
<tr><td>$\overline{BE3}$–$\overline{BE0}$</td><td>109–114</td><td>O</td><td>BYTE ENABLE. These tri-stated signals are used to indicate which bytes are involved with the current memory access. The number of Byte Enable signals asserted indicates the physical size of the data being transferred (1, 2, 3, or 4 bytes).
• $\overline{BE0}$ indicates D7–D0
• $\overline{BE1}$ indicates D15–D8
• $\overline{BE2}$ indicates D23–D16
• $\overline{BE3}$ indicates D31–D24
These lines are floated after a Reset or when the bus is not acquired.</td></tr>
<tr><td>W/$\overline{R}$</td><td>120</td><td>O</td><td>WRITE/READ. This dual function pin is used to distinguish Write and Read cycles. This line is floated after a Reset or when the bus is not acquired.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
$\overline{ADS}$	124	O	**ADDRESS STATUS.** The 82596 uses this tri-state pin to indicate to indicate that a valid bus cycle has begun and that A31–A2, $\overline{BE3}$–$\overline{BE0}$, and W/$\overline{R}$ are being driven. It is asserted during t1 bus states. This line is floated after a Reset or when the bus is not acquired.
$\overline{RDY}$	130	I	**READY.** Active low. This signal is the acknowledgment from addressed memory that the transfer cycle can be completed. When high, it causes wait states to be inserted. It is ignored at the end of the first clock of the bus cycle's data cycle. This active-low signal does not have an internal pull-up resistor. This signal must meet the setup and hold times to operate correctly.
$\overline{BRDY}$	2	I	**BURST READY.** Active low. Burst Ready, like $\overline{RDY}$, indicates that the external system has presented valid data on the data pins in response to a Read, or that the external system has accepted the 82596 data in response to a Write request. Also, like $\overline{RDY}$, this signal is ignored at the end of the first clock in a bus cycle. If the 82596 can still receive data from the previous cycle, ADS will not be asserted in the next clock cycle; however, Address and Byte Enable will change to reflect the next data item expected by the 82596. $\overline{BRDY}$ will be sampled during each succeeding clock and if active, the data on the pins will be strobed to the 82596 or to external memory (read/write). $\overline{BRDY}$ operates exactly like READY during the last data cycle of a burst sequence and during nonburstable cycles.
$\overline{BLAST}$	128	O	**BURST LAST.** A signal (active low) on this tri-state pin indicates that the burst cycle is finished and when $\overline{BRDY}$ is next returned it will be treated as a normal ready; i.e., another set of addresses will be driven with $\overline{ADS}$ or the bus will go idle. $\overline{BLAST}$ is not asserted if the bus is not acquired.
AHOLD	117	I	**ADDRESS HOLD.** This hold signal is active high, it allows another bus master to access the 82596 address bus. In a system where an 82596 and an i486 processor share the local bus, AHOLD allows the cache controller to make a cache invalidation cycle while the 82596 holds the address lines. In response to a signal on this pin, the 82596 immediately (i.e. during the next clock) stops driving the entire address bus (A31–A2); the rest of the bus can remain active. For example, data can be returned for a previously specified bus cycle during Address Hold. The 82596 will not begin another bus cycle while AHOLD is active.
$\overline{BOFF}$	116	I	**BACKOFF.** This signal is active low, it informs the 82596 that another bus master requires access to the bus before the 82596 bus cycle completes. The 82596 immediately (i.e. during the next clock) floats its bus. Any data returned to the 82596 while $\overline{BOFF}$ is asserted is ignored. $\overline{BOFF}$ has higher priority than $\overline{RDY}$ or $\overline{BRDY}$; if two such signals are returned in the same clock period, $\overline{BOFF}$ is given preference. The 82596 remains in Hold until $\overline{BOFF}$ goes high, then the 82596 resumes its bus cycle by driving out the address and status, and asserting $\overline{ADS}$.
$\overline{LOCK}$	126	O	**LOCK.** This tri-state pin is used to distinguish locked and unlocked bus cycles. $\overline{LOCK}$ generates a semaphore handshake to the CPU. $\overline{LOCK}$ can be active for several memory cycles, it goes active during the first locked memory cycle (t1) and goes inactive at the last locked cycle (t2). This line is floated after a Reset or when the bus is not acquired. $\overline{LOCK}$ can be disabled via the sysbus byte in software.

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
$\overline{BS16}$	129	I	**BUS SIZE.** This signal allows the 82596CA to work with either 16- or 32-bit bytes. Inserting $\overline{BS16}$ low causes the 82596 to perform two 16-bit memory accesses when transferring 32-bit data. In little endian mode the D15–D0 lines are driven when $\overline{BS16}$ is inserted, in Big Endian mode the D31–D16 lines are driven.
HOLD	123	O	**HOLD.** The HOLD signal is active high, the 82596 uses it to request local bus mastership. In normal operation HOLD goes inactive before HLDA. The 82596 can be forced off the bus by deasserting HLDA or if the bus throttle timers expire.
HLDA	118	I	**HOLD ACKNOWLEDGE.** The HLDA signal is active high, it indicates that bus mastership has been given to the 82596. HLDA is internally synchronized; after HOLD is detected low, the CPU drives HLDA low. **NOTE:** *Do not connect HLDA to V_{CC}—it will cause a deadlock.* A user wanting to give the 82596 permanent access to the bus should connect HLDA to HOLD. If HLDA goes inactive before HOLD, the 82596 will release the bus (by deasserting HOLD) within a maximum of within a specified number of bus cycles as specified in the 82596 User's Manual.
BREQ	115	I	**BUS REQUEST.** This signal, when configured to an externally activated mode, is used to trigger the bus throttle timers.
$\overline{PORT}$	3	I	**PORT.** When this signal is received, the 82596 latches the data on the data bus into an internal 32-bit register. When the CPU is asserting this signal it can write into the 82596 (via the data bus). This pin must be activated twice during all CPU Port access commands.
RESET	69	I	**RESET.** This active high, internally synchronized signal causes the 82596 to terminate current activity. The signal must be high for at least five system clock cycles. After five system clock cycles and four $\overline{TxC}$ clock cycles the 82596 will execute a Reset when it receives a high RESET signal. When RESET returns to low the 82596 waits for the first CA signal and then begins the initialization sequence.
LE/$\overline{BE}$	65	I	**LITTLE ENDIAN/BIG ENDIAN.** This dual-function pin is used to select byte ordering. When LE/$\overline{BE}$ is high, little endian byte ordering is used; when low, big endian byte ordering is used for data in frames (bytes) and for control (SCB, RFD, CBL, etc).
CA	119	I	**CHANNEL ATTENTION.** The CPU uses this pin to force the 82596 to begin executing memory resident Command blocks. The CA signal is internally synchronized. The signal must be high for at least one system clock. It is latched internally on the high to low edge and then detected by the 82596. The first CA after a Reset forces the 82596 into the initialization sequence beginning at location 00FFFFF6h or an SCP address written to the 82596 using CPU Port access. All subsequent CA signals cause the 82596 to begin executing new command sequences from the SCB.
INT/$\overline{INT}$	125	O	**INTERRUPT.** A high signal on this pin notifies the CPU that the 82596 is requesting an interrupt. This signal is an edge triggered interrupt signal, and can be configured to be active high or low.

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
V_{CC}	17 Pins		**POWER.** +5 V ±10%.
V_{SS}	17 Pins		**GROUND.** 0 V.
TxD	54	O	**TRANSMIT DATA.** This pin transmits data to the serial link. It is high when not transmitting.
$\overline{TxC}$	64	I	**TRANSMIT CLOCK.** This signal provides the fundamental timing for the serial subsystem. The clock is also used to transmit data synchronously on the TxD pin. For NRZ encoding, data is transferred to the TxD pin on the high to low clock transition. For Manchester encoding, the transmitted bit center is aligned with the low to high transition. Transmit clock must always be running for proper device operation.
$\overline{LPBK}$	58	O	**LOOPBACK.** This TTL-level control signal enables the loopback mode. In this mode serial data on the TxD input is routed through the 82C501 internal circuits and back to the RxD output without driving the transceiver cable. To enable this signal, both internal and external loopback need to be set with the Configure command.
RxD	60	I	**RECEIVE DATA.** This pin receives NRZ serial data only. It must be high when not receiving.
$\overline{RxC}$	59	I	**RECEIVE CLOCK.** This signal provides timing information to the internal shifting logic. For NRZ data the state of the RxD pin is sampled on the high to low transition of the clock.
$\overline{RTS}$	57	O	**REQUEST TO SEND.** When this signal is low the 82596 informs the external interface that it has data to transmit. It is forced high after a Reset or when transmission is stopped.
$\overline{CTS}$	62	I	**CLEAR TO SEND.** An active-low signal that enables the 82596 to send data. It is normally used as an interface handshake to $\overline{RTS}$. Asserting $\overline{CTS}$ high stops transmission. $\overline{CTS}$ is internally synchronized. If $\overline{CTS}$ goes inactive, meeting the setup time to the $\overline{TxC}$ negative edge, the transmission will stop and $\overline{RTS}$ will go inactive within, at most, two $\overline{TxC}$ cycles.
$\overline{CRS}$	63	I	**CARRIER SENSE.** This signal is active low, it is used to notify the 82596 that traffic is on the serial link. It is only used if the 82596 is configured for external Carrier Sense. In this configuration external circuitry is required for detecting traffic on the serial link. $\overline{CRS}$ is internally synchronized. To be accepted, the signal must remain active for at least two serial clock cycles (for CRSF = 0).
$\overline{CDT}$	61	I	**COLLISION DETECT.** This active-low signal informs the 82596 that a collision has occurred. It is only used if the 82596 is configured for external Collision Detect. External circuitry is required for collision detection. $\overline{CDT}$ is internally synchronized. To be accepted, the signal must remain active for at least two serial clock cycles (for CDTF = 0).

82596 AND HOST CPU INTERACTION

The 82596CA and the host CPU communicate through shared memory. Because of its on-chip DMA capability, the 82596 can make data block transfers (buffers and frames) independently of the CPU; this greatly reduces the CPU byte transfer overhead.

The 82596 is a multitasking coprocessor that comprises two independent logical units—the Command Unit (CU) and the Receive Unit (RU). The CU executes commands from shared memory. The RU handles all activities related to frame reception. The independence of the CU and RU enables the 82596 to engage in both activities simultaneously—the CU can fetch and execute commands from memory while the RU is storing received frames in memory. The CPU is only involved with this process after the CU has executed a sequence of commands or the RU has finished storing a sequence of frames.

The CPU and the 82596 use the hardware signals Interrupt (INT) and Channel Attention (CA) to initiate communication with the System Control Block (SCB), see Figure 4. The 82596 uses INT to alert the CPU of a change in the contents of the SCB, the CPU uses CA to alert the 82596.

The 82596 has a CPU Port Access state that allows the CPU to execute certain functions without accessing memory. The 82596 $\overline{\text{PORT}}$ pin and data bus pins are used to enable this feature. The CPU can directly activate four operations when the 82596 is in this state.

- Write an alternative System Configuration Pointer (SCP). This can be used when the 82596 cannot use the default SCP address space.
- Write a different Dump Command Pointer and execute Dump. This can be used for troubleshooting No Response problems.
- The CPU can reset the 82596 via software without disturbing the rest of the system.
- A self-test can be used for board testing; the 82596 will execute a self-test and write the results to memory.

82596 BUS INTERFACE

The 82596CA has bus interface timings and pin definitions that are compatible with Intel's 32-bit i486™SX and i486™DX microprocessors. This eliminates the need for additional bus interface logic. Operating at 33 MHz, the 82596's bus bandwidth can be as high as 106 MB/s. Since Ethernet only requires 1.25 MB/s, this leaves a considerable amount of bandwidth for the CPU. The 82596 also has a bus throttle to regulate its use of the bus. Two timers can be programmed through the SCB: one controls the maximum time the 82596 can remain on the bus, the other controls the time the 82596 must stay off the bus (see Figure 5). The bus throttle can be programmed to trigger internally with HLDA or externally with BREQ. These timers can restrict the 82596 HOLD activation time and improve bus utilization.

82596 MEMORY ADDRESSING

The 82596 has a 32-bit memory address range, which allows addressing up to four gigabytes of memory. The 82596 has three memory addressing modes (see Table 1).

- **82586 Mode.** The 82596 has a 24-bit memory address range. The System Control Block, Command List, Receive Descriptor List, and Buffer Descriptors must reside in one 64-KB memory segment. Transmit and Receive buffers can reside in a 24-bit address space.
- **32-Bit Segmented Mode.** The 82596 has a 32-bit memory address range. The System Control Block, Command List, Receive Descriptor List, and Buffer Descriptors must reside in one 64-KB memory segment. Transmit and Receive buffers can reside in a 32-bit address space.
- **Linear Mode.** The 82596 has a 32-bit memory address range. Any memory structure can reside anywhere within the 32-bit memory address range.

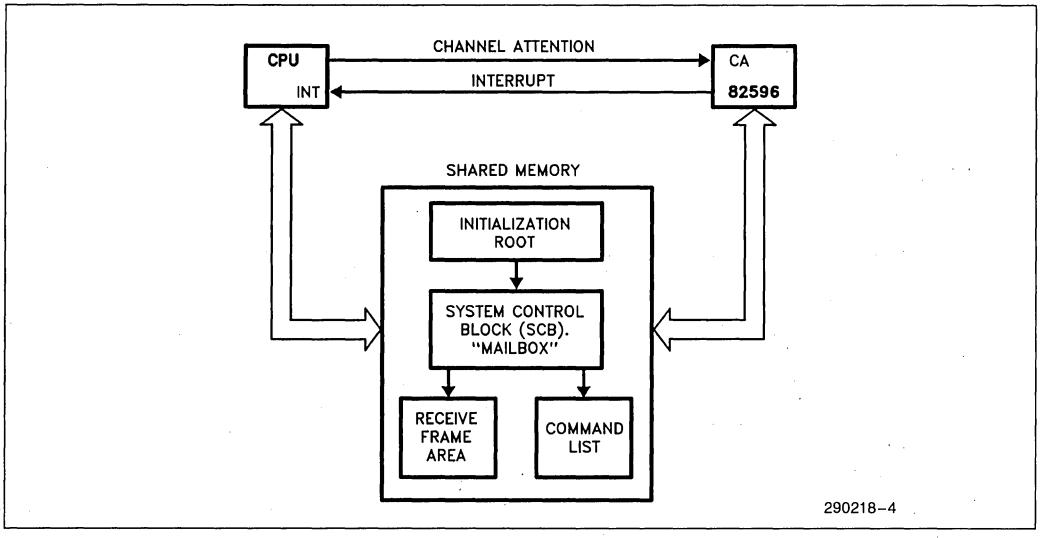


Figure 4. 82596 and Host CPU Intervention

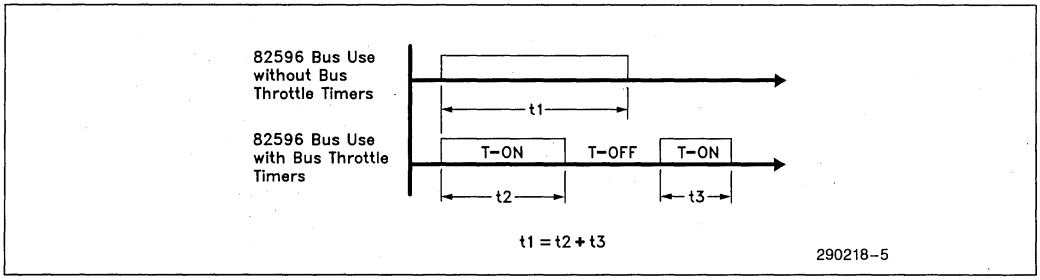


Figure 5. Bus Throttle Timers

Table 1. 82596 Memory Addressing Formats

Pointer or Offset	Operation Mode		
	82586	32-Bit Segmented	Linear
ISCP Address	24-Bit Linear	32-Bit Linear	32-Bit Linear
SCB Address	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Command Block Pointers	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Frame Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Tx Frame Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Buffer Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Tx Buffer Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Buffers	24-Bit Linear	32-Bit Linear	32-Bit Linear
Tx Buffers	24-Bit Linear	32-Bit Linear	32-Bit Linear

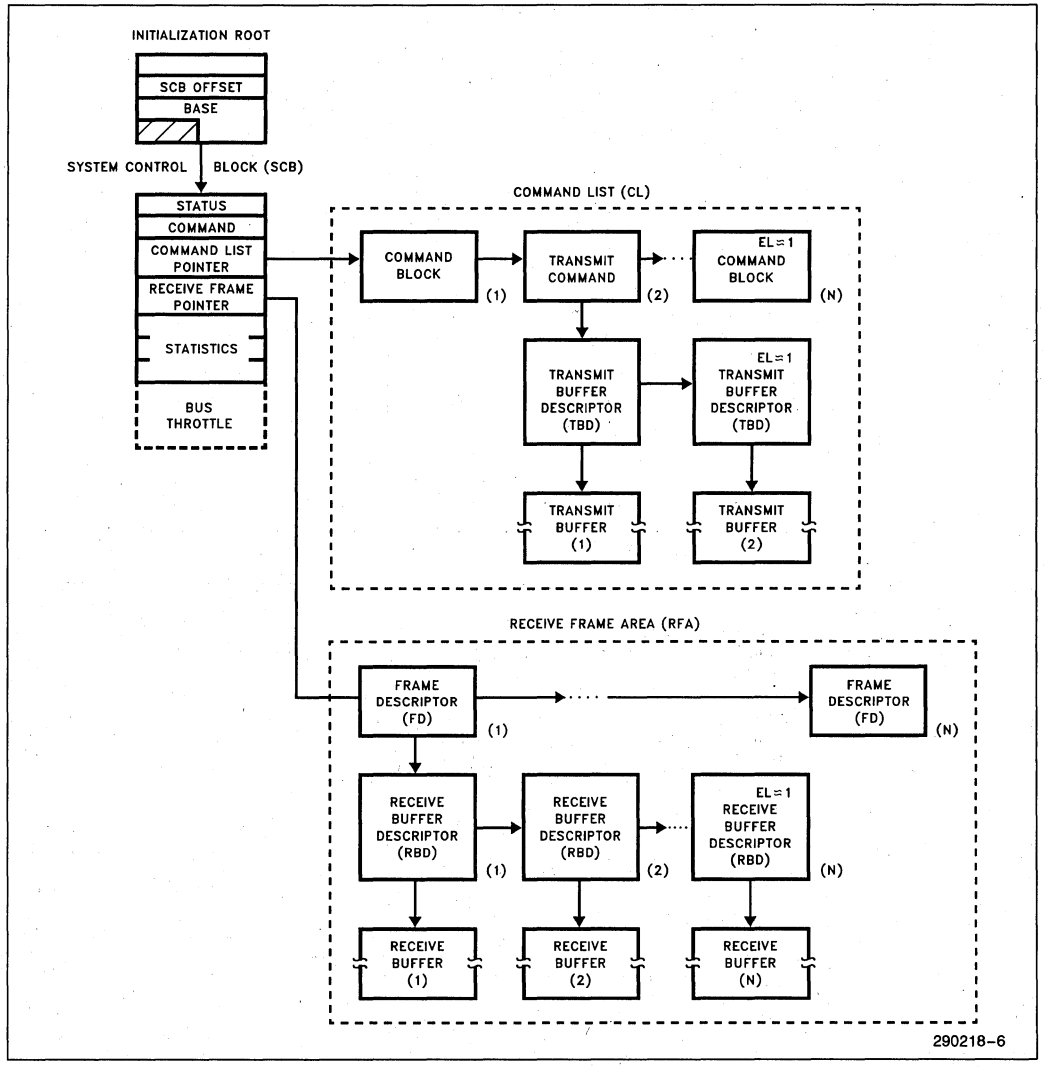


Figure 6. 82596 Shared Memory Structure

82596 SYSTEM MEMORY STRUCTURE

The Shared Memory structure consists of four parts: the Initialization Root, the System Control Block, the Command List, and the Receive Frame Area (see Figure 6).

The Initialization Root is in an established location known to the host CPU and the 82596 (00FFFFF6h). However, the CPU can establish the Initialization Root in another location by using the CPU Port access. This root is accessed during initialization, and points to the System Control Block.

The System Control Block serves as a bidirectional mail drop for the host CPU and the 82596 CU and RU. It is the central point through which the CPU and the 82596 exchange control and status information. The SCB has two areas. The first contains instructions from the CPU to the 82596. These include: control of the CU and RU (Start, Abort, Suspend, and Resume), a pointer to the list of CU commands, a pointer to the Receive Frame Area, a set of Interrupt Acknowledge bits, and the T-ON and T-OFF timers for the bus throttle. The second area contains status information the 82596 is sending to the CPU. Such as, the CU and RU states (Idle, Active

Ready, Suspended, No Receive Resources, etc.), interrupt bits (Command Completed, Frame Received, CU Not Ready, and RU Not Ready), and statistical counters.

The Command List functions as a program for the CU; individual commands are placed in memory units called Command Blocks (CBs). These CBs contain the parameters and status of specific high-level commands called Action Commands; e.g., Transmit or Configure.

Transmit causes the 82596 to transmit a frame. The Transmit CB contains the destination address, the length field, and a pointer to a list of linked buffers holding the frame that is to be constructed from several buffers scattered throughout memory. The Command Unit operates without CPU intervention; the DMA for each buffer, and the prefetching of references to new buffers, is performed in parallel. The CPU is notified only after a transmission is complete.

The Receive Frame Area is a list of Free Frame Descriptors (descriptors not yet used) and a list of user-prepared buffers. Frames arrive at the 82596 unsolicited; the 82596 must always be ready to receive and store them in the Free Frame Area. The Receive Unit fills the buffers when it receives frames, and reformats the Free Buffer List into received-frame structures. The frame structure is, for all practical purposes, identical to the format of the frame to be transmitted. The first Frame descriptor is referenced by the SCB. Unless the 82596 is configured to Save Bad Frames, the frame descriptor, and the associated buffer descriptor, which is wasted when a bad frame is received, are automatically reclaimed and returned to the Free Buffer List.

Receive buffer chaining (storing incoming frames in a linked buffer list) significantly improves memory utilization. Without buffer chaining, the user must allocate consecutive blocks of memory, each capable of containing a maximum frame (for Ethernet, 1518 bytes). Since an average frame is about 200 bytes, this is very inefficient. With buffer chaining, the user can allocate small buffers and the 82596 will only use those that are needed.

Figure 7 A–D illustrates how the 82596 uses the Receive Frame Area. Figure 7A shows an unused Receive Frame Area composed of Free Frame Descriptors and Free Receive Buffers prepared by the user. The SCB points to the first Frame Descriptor of the Frame Descriptor List. Figure 7B shows the same Receive Frame Area after receiving one frame. This first frame occupies two Receive Buffers and one Frame Descriptor—a valid received frame will only occupy one Frame Descriptor. After receiving this frame the 82596 sets the next Free Frame Descriptor RBD pointer to the next Free RBD. Figure 7C shows the RFA after receiving a second frame. In this example the second frame occupies only one Receive Buffer and one RFD. The 82596 again sets the RBD pointer. This process is repeated again in Figure 7D, showing the reception of another frame using one Receive Buffer; in this example there is an extra Frame Descriptor.

TRANSMIT AND RECEIVE MEMORY STRUCTURES

There are three memory structures for reception and transmission. The 82586 memory structure, the Flexible memory structure, and the Simplified memory structure. The 82586 mode is selected by configuring the 82596 during initialization. In this mode all the 82596 memory structures are compatible with the 82586 memory structures.

When the 82596 is not configured to the 82586 mode, the other two memory structures, Simplified and Flexible, are available for transmitting and receiving. These structures are selected by setting the S/F bit in the Transmit Command and/or the Receive Frame Descriptor (see Figures 29, 30, 41, and 42). It is recommended that any linked list of buffers be relegated to a single type—either simplified or flexible. The Simplified memory structure offers a simple structure for ease of programming (see Figure 8). All information about a frame is contained in one structure; for example, during reception the RFD and data field are contained in one structure.

The Flexible memory structure (see Figure 9) has a control field that allows the programmer to specify the amount of receive data the RFD will contain for receive operations and the amount of transmit data the Transmit Command Block will contain for transmit operations. For example, when the control field in the RFD is set to 20 bytes during a reception, the first 20 bytes of the data field are stored in the RFD (6 bytes of destination address, 6 bytes of source address, 2 bytes of length field, and 6 bytes of data) and the remainder of the data field is stored in the Receive Data Buffers. This is useful for capturing frame headers when header information is contained in the data field. The header information can then be automatically stored in the RFD partitioned from the Receive Data Buffer.

The control field can also be used for the Transmit Command when the Flexible memory structure is used. The quantity of data field bytes to be transmitted from the Transmit Command Block is specified by the variable control field.

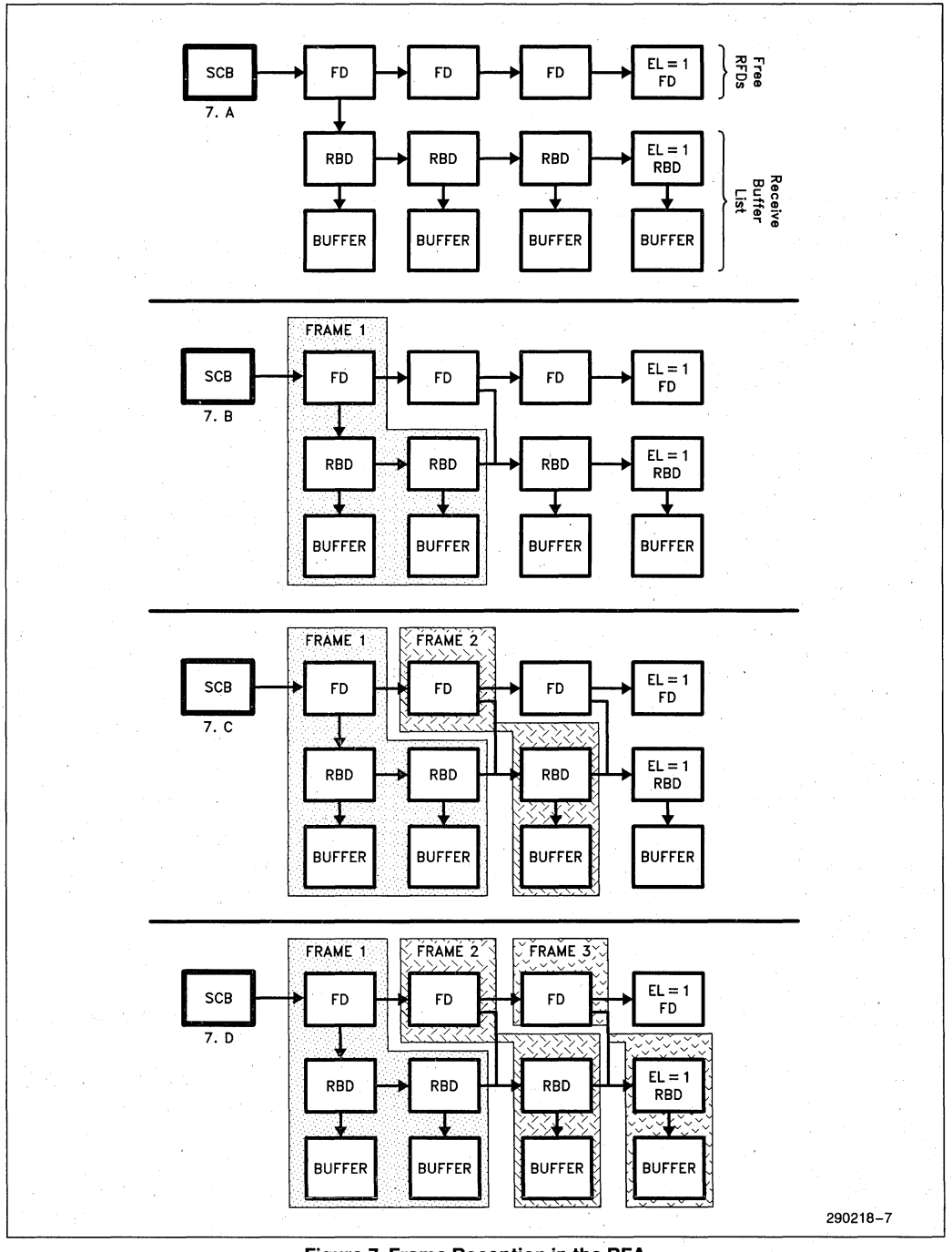


Figure 7. Frame Reception in the RFA

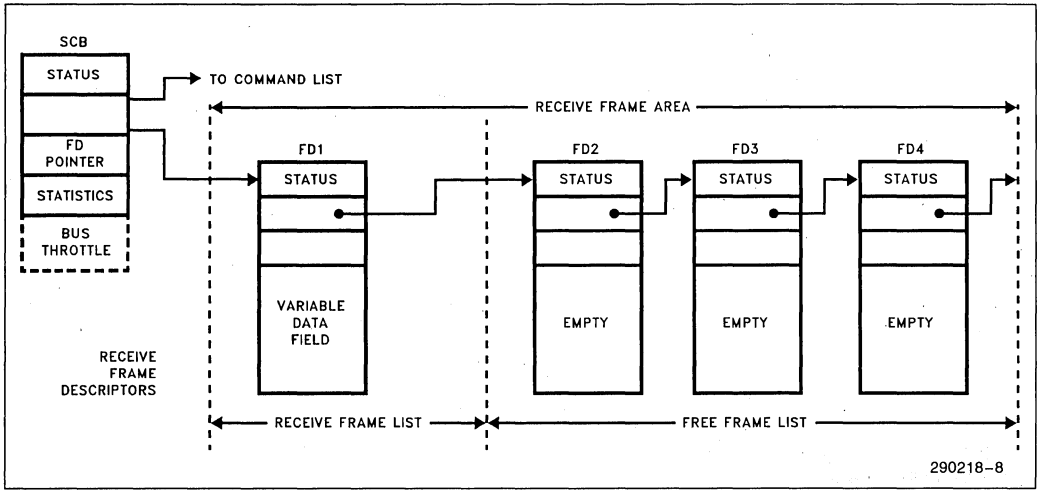


Figure 8. Simplified Memory Structure

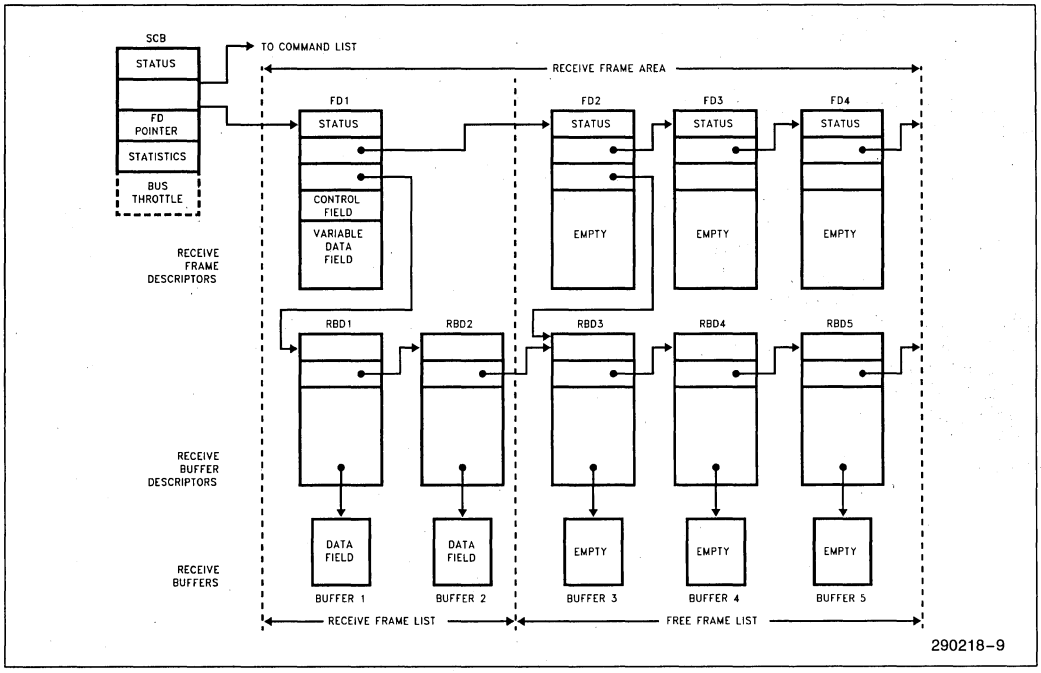


Figure 9. Flexible Memory Structure

TRANSMITTING FRAMES

The 82596 executes high-level Action Commands from the Command List in system memory. Action Commands are fetched and executed in parallel with the host CPU operation, thereby significantly improving system performance. The format of the Action Commands is shown in Figure 10. Figure 28 shows the 82586 mode, and Figures 29 and 30 show the command formats of the Linear and 32-bit Segmented modes.

A single Transmit command contains, as part of the command-specific parameters, the destination address and length field of the transmitted frame and a pointer to buffer area in memory containing the data portion of the frame. The data field is contained in a memory data structure consisting of a buffer descriptor (BD) and a data buffer—or a linked list of buffer descriptors and buffers—as shown in Figure 11.

Multiple data buffers can be chained together using the BDs. Thus, a frame with a long data field can be transmitted using several (shorter) data buffers chained together. This chaining technique allows the system designer to develop efficient buffer management.

The 82596 automatically generates the preamble (alternating 1s and 0s) and start frame delimiter, fetches the destination address and length field from the Transmit command, inserts its unique address as the source address, fetches the data field specified by the Transmit command, and computes and appends the CRC to the end of the frame (see Figure 12). In the Linear and 32-bit Segmented mode the CRC can be optionally inserted on a frame-by-frame basis by setting the NC bit in the Transmit Command Block (see Figures 29 and 30).

The 82596 generates the standard End Of Carrier (EOC) start and end frame delimiters. In EOC, the start frame delimiter is 10101011 and the end frame delimiter is indicated by the lack of a signal after the last bit of the frame check sequence field has been transmitted. In EOC, the 82596 can be configured to extend short frames by adding pad bytes (7Eh) during transmission, according to the length field.

When a collision occurs, the 82596 manages the jam, random wait, and retry processes, reinitializing DMA pointers without CPU intervention. Multiple frames can be sent by linking the appropriate number of Transmit commands together. This is particularly useful when transmitting a message larger than the maximum frame size (1518 bytes for Ethernet).

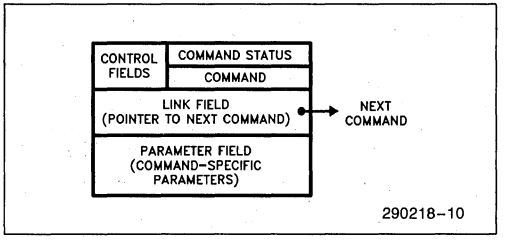


Figure 10. Action Command Format

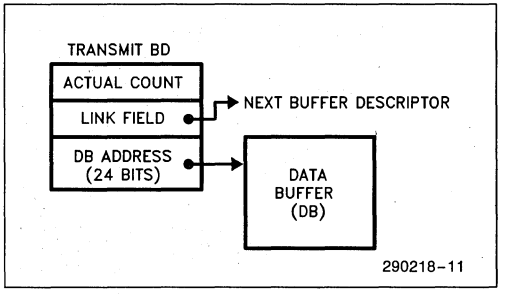


Figure 11. Data Buffer Descriptor and Data Buffer Structure

PREAMBLE	START FRAME DELIMITER	DESTINATION ADDRESS	SOURCE ADDRESS	LENGTH FIELD	DATA FIELD	FRAME CHECK SEQUENCE	END FRAME DELIMITER

Figure 12. Frame Format

RECEIVING FRAMES

To reduce CPU overhead, the 82596 is designed to receive frames without CPU supervision. The host CPU first sets aside an adequate receive buffer space and then enables the 82596 Receive Unit. Once enabled, the RU watches for arriving frames and automatically stores them in the Receive Frame Area (RFA). The RFA contains Receive Frame Descriptors, Receive Buffer Descriptors, and Data Buffers (see Figure 13). The individual Receive Frame Descriptors make up a Receive Descriptor List (RDL) used by the 82596 to store the destination and source addresses, the length field, and the status of each frame received (see Figure 14).

Once enabled, the 82596 checks each passing frame for an address match. The 82596 will recognize its own unique address, one or more multicast addresses, or the broadcast address. If a match is found the 82596 stores the destination and source addresses and the length field in the next available RFD. It then begins filling the next available Data Buffer on the FBL, which is pointed to by the current RFD, with the data portion of the incoming frame. As one Data Buffer is filled, the 82596 automatically fetches the next DB on the FBL until the entire frame is received. This buffer chaining technique is particularly memory efficient because it allows the system designer to set aside buffers to fit frames much shorter than the maximum allowable frame length. If AL-LOC = 1, or if the flexible memory structure is used, the addresses and length field can be placed in the Receive Buffer.

Once the entire frame is received without error, the 82596 does the following housekeeping tasks.

- The actual count field of the last Buffer Descriptor used to hold the frame just received is updated with the number of bytes stored in the associated Data Buffer.
- The next available Receive Frame Descriptor is fetched.
- The address of the next available Buffer Descriptor is written to the next available Receive Frame Descriptor.
- A frame received interrupt status bit is posted in the SCB.
- An interrupt is sent to the CPU.

If a frame error occurs, for example a CRC error, the 82596 automatically reinitializes its DMA pointers and reclaims any data buffers containing the bad frame. The 82596 will continue to receive frames without CPU help as long as Receive Frame Descriptors and Data Buffers are available.

82596 NETWORK MANAGEMENT AND DIAGNOSTICS

The behavior of data communication networks is normally very complex because of their distributed and asynchronous nature. It is particularly difficult to pinpoint a failure when it occurs. The 82596 has extensive diagnostic and network management functions that help improve reliability and testability. The 82596 reports on the following events after each frame is transmitted.

- Transmission successful.
- Transmission unsuccessful. Lost Carrier Sense.
- Transmission unsuccessful. Lost Clear to Send.
- Transmission unsuccessful. A DMA underrun occurred because the system bus did not keep up with the transmission.
- Transmission unsuccessful. The number of collisions exceeded the maximum allowed.
- Number of Collisions. The number of collisions experienced during transmission of the frame.
- Heartbeat Indicator. This indicates the presence of a heartbeat during the last Interframe Spacing (IFS) after transmission.

When configured to Save Bad Frames the 82596 checks each incoming frame and reports the following errors.

- CRC error. Incorrect CRC in a properly aligned frame.
- Alignment error. Incorrect CRC in a misaligned frame.
- Frame too short. The frame is shorter than the value configured for minimum frame length.
- Overrun. Part of the frame was not placed in memory because the system bus did not keep up with incoming data.
- Out of buffer. Part of the frame was discarded because of insufficient memory storage space.
- Receive collision. A collision was detected during reception and the destination address of the incoming frame matches the 82596 individual address. Collisions in the preamble are not counted.
- Length error. A frame not matching the frame length parameter was detected.

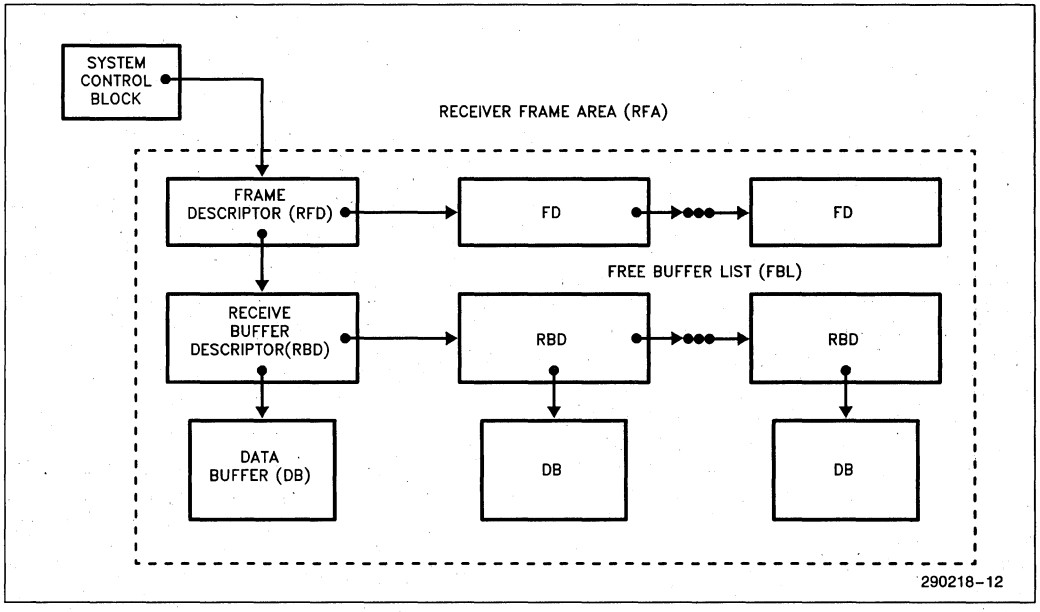


Figure 13. Receive Frame Area Diagram

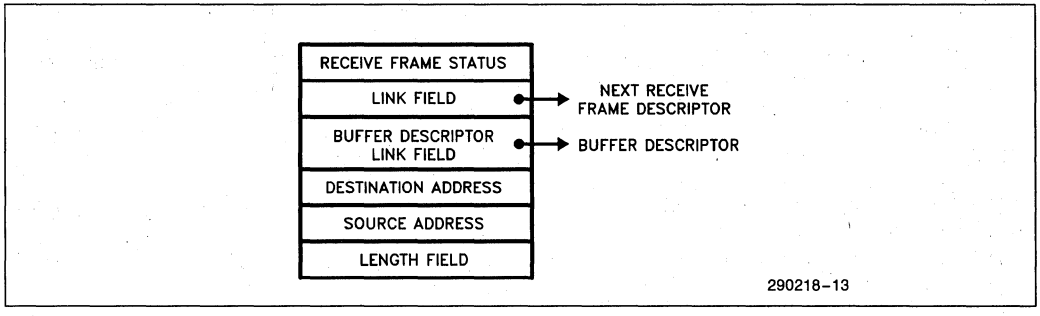


Figure 14. Receive Frame Descriptor

NETWORK PLANNING AND MAINTENANCE

To properly plan, operate, and maintain a communication network, the network management entity must accumulate information on network behavior. The 82596 provides a rich set of network-wide diagnostics that can serve as the basis for a network management entity.

Information on network activity is provided in the status of each frame transmitted. The 82596 reports the following activity indicators after each frame.

- Number of collisions. The number of collisions the 82596 experienced while attempting to transmit the frame.
- Deferred transmission. During the first transmission attempt the 82596 had to defer to traffic on the link.

The 82596 updates its 32-bit statistical counters after each received frame that both passes address filtering and is longer than the Minimum Frame Length configuration parameter. The 82596 reports the following statistics.

- CRC errors. The number of well-aligned frames that experienced a CRC error.
- Alignment errors. The number of misaligned frames that experienced a CRC error.
- No resources. The number of frames that were discarded because of insufficient resources for reception.
- Overrun errors. The number of frames that were not completely stored in memory because the system bus did not keep up with incoming data.
- Receive Collision counter. The number of collisions detected during receive. Collisions occurring before the minimum frame length will be counted as short frames. Collisions in the preamble will not be counted at all.
- Short Frame counter. The number of frames that were discarded because they were shorter than the configured minimum frame length.

Once again, these counters are not updated until the 82596 decodes a destination address match.

The 82596 can be configured to Promiscuous mode. In this mode it captures all frames transmitted on the network without checking the Destination Address. This is useful when implementing a monitoring station to capture all frames for analysis.

A useful method of capturing frame headers is to use the Simplified memory mode, configure the 82596 to Save Bad Frames, and configure the 82596 to Promiscuous mode with space in the RFD allocated for specific number of receive data bytes. The 82596 will receive all frames and put them in the RFD. Frames that exceed the available space in the RFD will be truncated, the status will be updated, and the 82596 will retrieve the next RFD. This allows the user to capture the initial data bytes of each frame (for instance, the header) and discard the remainder of the frame.

The 82596 also has a monitor mode for network analysis. During normal operation the receive function enables the 82596 to receive frames that pass address filtering. These frames must have the Start of Frame Delimiter (SFD) field and must be longer than the absolute minimum frame length of 5 bytes (6 bytes in case of Multicast address filtering). Contents and status of the received frames are transferred to memory. The monitor function enables the 82596 to simply evaluate the incoming frames. The 82596 can monitor the frames that pass or do not pass the address filtering. It can also monitor frames which do not have the SFD fields. The 82596 can be configured to only keep statistical information about monitor frames. Three options are available in the Monitor mode. These options are selected by the two monitor mode configuration bits available in the configuration command.

When the first option is selected, the 82596 receives good frames that pass address filtering and transfers them to memory while monitoring frames that do not pass address filtering or are shorter than the minimum frame size (these frames are not transferred to memory). When this option is used the 82596 updates six counters: CRC errors, alignment errors, no resource errors, overrun errors, short frames and total good frames received.

When the second option is selected, the receive function is completely disabled. The 82596 monitors only those frames that pass address filterings and meet the minimum frame length requirement. When this option is used the 82596 updates six counters: CRC errors, alignment errors, total frames (good and bad), short frames, collisions detected and total good frames.

When the third option is selected, the receive function is completely disabled. The 82596 monitors all frames, including frames that do not have a Start Frame Delimiter. When this option is used the 82596 updates six counters: CRC errors, alignment errors, total frames (good and bad), short frames, collisions detected and total good frames.

STATION DIAGNOSTICS AND SELF-TEST

The 82596 provides a large set of diagnostic and network management functions. These include internal and external loopback and time domain reflectometry for locating fault points in the network cable. The 82596 ensures software reliability by dumping the contents of the 82596 internal registers into system memory. The 82596 has a self-test mode that enables it to run an internal self-test and place the results in system memory.

82586 SOFTWARE COMPATIBILITY

The 82596 has a software-compatible state in which all its memory structures are compatible with the 82586 memory structure. This includes all the Action Commands, the Receive Frame Area (including the RFD, Buffer Descriptors, and Data Buffers), the System Control Block, and the initialization procedures. There are two minor differences between the 82596 in the 82586-Compatible memory structure and the 82586.

- When the internal and external loopback bits in the Configure command are set to 11 the 82596 is in external loopback and the $\overline{LPBK}$ pin is activated; in the 82586 this situation would produce internal loopback.
- During a Dump command both the 82596 and 82586 dump the same number of bytes; however, the data format is different.

INITIALIZING THE 82596

A Reset command is issued to the 82596 to prepare it for normal operation. The 82596 is initialized through two data structures that are addressed by two pointers, the System Configuration Pointer (SCP) and the Intermediate System Configuration Pointer (ISCP). The initialization procedure begins when a Channel Attention signal is asserted after RESET. The 82596 uses the address of the double word that contains the SCP as a default—00FFFFF4h. Before the CA signal is asserted this default address can be changed to any other available address by asserting the $\overline{PORT}$ pin and providing the desired address over the $D_{31}-D_4$ pins of the address bus. Pins D_3-D_0 must be 0010; i.e., any alternative address must be aligned to 16-byte boundaries. All addresses sent to the 82596 must be word aligned, which means that all pointers and memory structures must start on an even address (A_0 = zero).

SYSTEM CONFIGURATION POINTER (SCP)

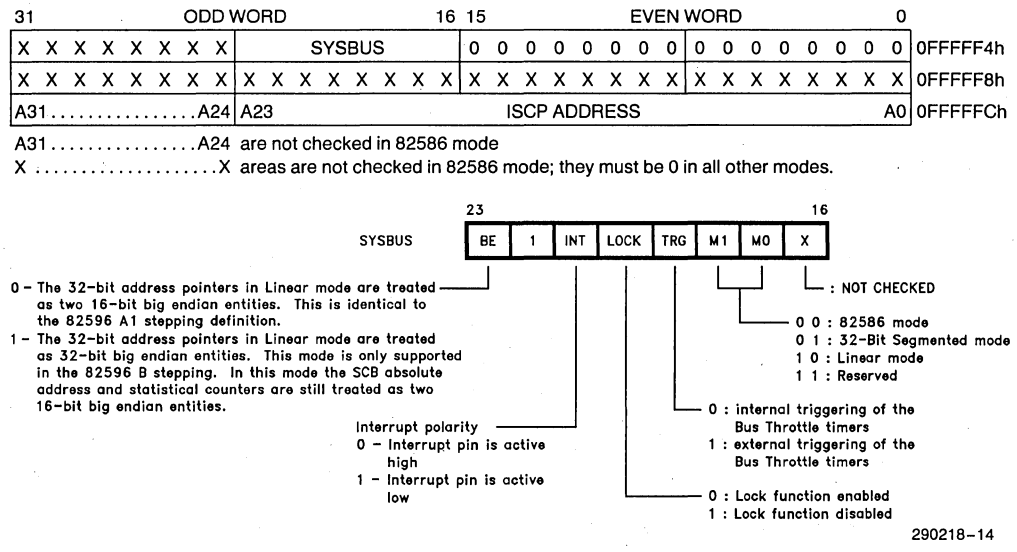
The SCP contains the sysbus byte and the location of the next structure of the initialization process, the ISCP. The following parameters are selected in the SYSBUS.

- The 82596 operation mode.
- The Bus Throttle timer triggering method.
- Lock enabled.
- Interrupt polarity.
- Big Endian 32-bit entity mode.

Byte ordering is determined by the LE/$\overline{BE}$ pin. LE/$\overline{BE}$ = 1 selects Little Endian byte ordering and LE/$\overline{BE}$ = 0 selects Big Endian byte ordering.

NOTE:
In the following, X indicates a bit not checked 82586 mode. This bit must be set to 0 in all other modes.

The following diagram illustrates the format of the SCP.



ISCP ADDRESS— The physical address of the ISCP. In the 82586 mode, bits A31–A24 are considered to be zero.

Figure 15. The System Configuration Pointer

Writing the Sysbus

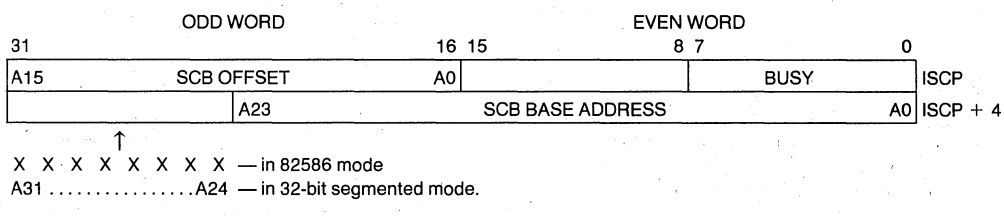
When writing the sysbus byte it is important to pay attention to the byte order.

- When a Little Endian processor is used, the sysbus byte is located at byte address 00FFFFF6h (or address $n+2$ if an alternative SCP address n was programmed).
- When a processor using Big Endian byte ordering is used, the sysbus, alternative SCP, and ISCP addresses will be different.
  - The sysbus byte is located at 00FFFFF5h.
  - If an alternative SCP address is programmed, the sysbus byte should be at byte address $n+1$.

INTERMEDIATE SYSTEM CONFIGURATION POINTER (ISCP)

The ISCP indicates the location of the System Control Block. Often the SCP is in ROM and the ISCP is in RAM. The CPU loads the SCB address (or an equivalent data structure) into the ISCP and asserts CA. This Channel Attention signal causes the 82596 to begin its initialization procedure and to get the SCB address from the ISCP and SCP. In 82586 and 32-bit Segmented modes the SCP base address is also the base address of all Command Blocks, Frame Descriptors, and Buffer Descriptors (but not buffers). All these data structures must reside in one 64-KB segment; however, in Linear mode no such limitation is imposed.

The following diagram illustrates the ISCP format.

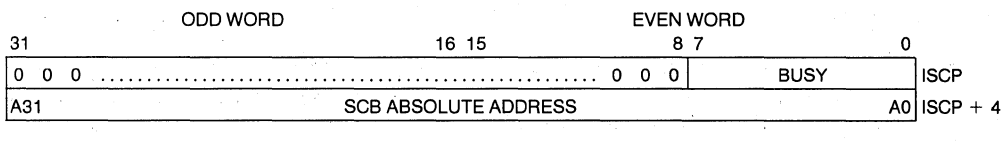


BUSY — Indicates that the 82596 is being initialized. The CPU sets the ISCP to 01h before it gives the first CA to the 82596. The ISCP is cleared by the 82596 after the SCB base and offset are read. Note that the most significant byte of the first word of the ISCP is not modified when BUSY is cleared.

SCB OFFSET— This 16-bit quantity specifies the offset portion of the address of the SCB.

SCB BASE — Specifies the base portion of the address of the SCB. The base of SCB is also the base of all 82596 Command Blocks, Frame Descriptors and Buffer Descriptors. In the 82586 mode, bits A31–A24 are considered to be zero.

Figure 16. The Intermediate System Configuration Pointer—82586 and 32-Bit Segmented Modes



BUSY — Indicates that the 82596 is being initialized. The ISCP is set to 01h by the CPU before its first CA to the 82596. It is cleared by the 82596 after the SCB address is read.

SCB ADDRESS— This 32-bit quantity specifies the physical address of the SCB.

Figure 17. The Intermediate System Configuration Pointer—Linear Mode.

INITIALIZATION PROCESS

The CPU sets up the SCP, ISCP, and the SCB structures, and, if desired, an alternative SCP address. It also sets BUSY to 01h. The 82596 is initialized when a Channel Attention signal follows a Reset signal, causing the 82596 to access the System Configuration Pointer. The sysbus byte, the operational mode, the bus throttle timer triggering method, the interrupt polarity, and the state of $\overline{\text{LOCK}}$ are read. After reset the Bus Throttle timers are essentially disabled—the T-ON value is infinite, the T-OFF value is zero. After the SCP is read, the 82596 reads the ISCP and saves the SCB address. In 82586 and 32-bit Segmented modes this address is represented as a base address plus the offset (this base address is also the base address of all the control blocks). In Linear mode the base address is also an absolute address. The 82596 clears BUSY, sets CX and CNR to equal 1 in the SCB, clears the SCB command word, sends an interrupt to the CPU, and awaits another Channel Attention signal. RESET configures the 82596 to its default state before CA is asserted.

CONTROLLING THE 82596CA

The host CPU controls the 82596 with the commands, data structures, and methods described in this section. The CPU and the 82596 communicate through shared memory structures. The 82596 contains two independent units: the Command Unit and the Receive Unit. The Command Unit executes commands from the CPU, and the Receive Unit handles frame reception. These two units are controlled and monitored by the CPU through a shared memory structure called the System Control Block (SCB). The CPU and the 82596 use the CA and INT signals to communicate with the SCB.

82596 CPU ACCESS INTERFACE ($\overline{PORT}$)

The 82596 has a CPU access interface that allows the host CPU to do four things.

- Write an alternative System Configuration Pointer address.
- Write an alternative Dump area pointer and perform Dump.
- Execute a software reset.
- Execute a self-test.

The following events initiate the CPU access state.

- Presence of an address on the $D_{31}-D_4$ data bus pins.
- The D_3-D_0 pins are used to select one of the four functions.
- The $\overline{PORT}$ input pin is asserted, as in a regular write cycle.

NOTE.
The SCP Dump and Self-Test addresses must be 16-byte aligned.

The 82596 requires two 16-bit write cycles for a port command. The first write holds the internal machines and reads the first 16 bits; the second activates the $\overline{PORT}$ command and reads the second 16 bits.

The $\overline{PORT}$ Reset is useful when only the 82596 needs to be reset. The CPU must wait for 10-system and 5-serial clocks before issuing another CA to the 82596; this new CA begins a new initialization process.

The Dump function is useful for troubleshooting No Response problems. If the chip is in a No Response state, the $\overline{PORT}$ Dump operation can be executed and a $\overline{PORT}$ Reset can be used to reinitialize the 82596 without disturbing the rest of the system.

The Self-Test function can be used for board testing; the 82596 will execute a self-test and write the results to memory.

Table 2. $\overline{PORT}$ Function Selection

	D31 ..... D4						D0
Function	**Addresses and Results**			**D3**	**D2**	**D1**	**D0**
Reset	A31	Don't Care	A4	0	0	0	0
Self-Test	A31	Self-Test Results Address	A4	0	0	0	1
SCP	A31	Alternative SCP Address	A4	0	0	1	0
Dump	A31	Dump Area Pointer	A4	0	0	1	1

MEMORY ADDRESSING FORMATS

The 82596 accesses memory by 32-bit addresses. There are two types of 32-bit addresses: linear and segmented. The type of address used depends on the 82596 operating mode and the type of memory structure it is addressing. The 82596 has three operating modes.

- 82586 Mode
  - A Linear address is a single 24-bit entity. Address pins $A_{31}-A_{24}$ are always zero.
  - A Segmented address uses a 24-bit base and a 16-bit offset.
- 32-bit Segmented Mode
  - A Linear address is a single 32-bit entity.
  - A Segmented address uses a 32-bit base and a 16-bit offset.

NOTE:
In the previous two memory addressing modes, each command header (CB, TBD, RFD, RBD, and SCB) must wholly reside within one segment. If the 82596 encounters a memory structure that does not follow this restriction, the 82596 will fetch the next contiguous location in memory (beyond the segment).

- Linear Mode
  - A Linear address is a single 32-bit entity.
  - There are no Segmented addresses.

Linear addresses are primarily used to address transmit and receive data buffers. In the 82586 and 32-bit Segmented modes, segmented addresses (base plus offset) are used for all Command Blocks, Buffer Descriptors, Frame Descriptors, and System Control Blocks. When using Segmented addresses, only the offset portion of the entity being addressed is specified in the block. The base for all offsets is the same—that of the SCB. See Table 1.

LITTLE ENDIAN AND BIG ENDIAN BYTE ORDERING

The 82596 supports both Little Endian and Big Endian byte ordering for its memory structures.

The 82596 A1 stepping supports Big Endian byte ordering for word and byte entities. Dword entities are not supported with 82596 A1 Big Endian byte ordering. This results in slightly different 82596A1 memory structures for Big Endian operation. These structures are defined in the *32-Bit LAN Components User's Manual.*

The 82596 B stepping supports Big Endian byte ordering for Linear mode only. All 82596 B 32-bit address pointers are treated as 32-bit Big Endian entities, however, the SCB absolute address and statistical counters are treated as two 16-bit Big Endian entities. This 32-bit Big Endian entity support is configured through bit 7 in the SYSBUS byte.

The 82596 C-step has a New Enhanced Big Endian Mode where in Linear Addressing mode, true 32-bit Big Endian functionality is achieved. New Enhanced Big Endian Mode is enabled exactly the same as the B-step, by setting bit 7 of the SYSBUS byte. This mode is software compatible with the big endian mode of the B-step with one exception—no 32-bit addresses need to be swapped by software in the C-step. In this new mode, the 82596 C-step treats 32-bit address pointers as true 32-bit entities and the SCB absolute address and statistical counters are still treated as two 16-bit big endian entities. Not setting this mode will configure the 82596 C-step to be 100% compatible to the A1-step big endian mode.

NOTE:
All 82596 memory entities must be word or dword aligned, except the transmit buffers can be byte aligned for the 82596 B or C-steppings.

An example of a dword entity is a frame descriptor command/status dword, whereas the raw data of the frame are byte entities. Both 32- and 16-bit buses are supported. When a 16-bit bus is used with Big Endian memory organization, data lines $D_{15}-D_0$ are used. The 82596 has an internal crossover that handles these swap operations.

COMMAND UNIT (CU)

The Command Unit is the logical unit that executes Action Commands from a list of commands very similar to a CPU program. A Command Block is associated with each Action Command. The CU is modeled as a logical machine that takes, at any given time, one of the following states.

- **Idle.** The CU is not executing a command and is not associated with a CB on the list. This is the initial state.
- **Suspended.** The CU is not executing a command; however, it is associated with a CB on the list.
- **Active.** The CU is executing an Action Command and pointing to its CB.

The CPU can affect CU operation in two ways: by issuing a CU Control Command or by setting bits in the Command word of the Action Command.

When programming the 82596 CU, it is important to consider the asynchronous way the 82596 processes commands. If a command is issued to the 82596 CU, it may be busy processing other commands. In order to avoid asynchronous race conditions, the following guidelines are recommended to the 82596 programmer:

- If the CU is already in the Active state, and another command needs to be executed, it is unwise to immediately issue another CU Start command. If a new command (or list of commands) needs to be started, first issue a CU Suspend command, wait for the CU to become Suspended, then issue the new CU Start. This will insure that all commands are processed correctly.
- In general, it is a good idea to make sure any CU command has been accepted and executed before issuing a new control command to the CU.

RECEIVE UNIT (RU)

The Receive Unit is the logical unit that receives frames and stores them in memory. The RU is modeled as a logical machine that takes, at any given time, one of the following states.

- **Idle.** The RU has no memory resources and is discarding incoming frames. This is the initial state.
- **No Resources.** The RU has no memory resources and is discarding incoming frames. This state differs from Idle in that the RU accumulates statistics on the number of discarded frames.
- **Suspended.** The RU has memory available for storing frames, but is discarding them. The suspend state can only be reached if the CPU forces this through the SCB or sets the suspend bit in the RFD.
- **Ready.** The RU has memory available and is storing incoming frames.

The CPU can affect RU operation in three ways: by issuing an RU Control Command, by setting bits in the Frame Descriptor Command word of the frame being received, or by setting the EL bit of the current buffer's Buffer Descriptor.

When programming the 82596 RU, it is important to consider the asynchronous way the 82596 processes receive frames. If an RU Start is issued to the 82596 RU, it may be busy processing other incoming packets. In order to avoid asynchronous race conditions, the following guidelines are recommended to the 82596 programmer:

- If the RU is already in the Ready state, and a new RFA is required to be started, it is unwise to immediately issue another RU Start command. If the new RFA needs to be started, first issue an RU Suspend command, wait for the RU to become Suspended, then issue the new RU Start. This will insure that all incoming frames are received correctly.
- In general, it is a good idea to make sure any RU command has been accepted and executed before issuing a new control command to the RU.

SYSTEM CONTROL BLOCK (SCB)

The SCB is a memory block that plays a major role in communications between the CPU and the 82596. Such communications include the following.

- Commands issued by the CPU
- Status reported by the 82596

Control commands are sent to the 82596 by writing them into the SCB and then asserting CA. The 82596 examines the command, performs the required action, and then clears the SCB command word. Control commands perform the following types of tasks.

- Operation of the Command Unit (CU). The SCB controls the CU by specifying the address of the Command Block List (CBL) and by starting, suspending, resuming, or aborting execution of CBL commands.
- Operation of the Bus Throttle. The SCB controls the Bus Throttle timers by providing them with new values and sending the Load and Start timer commands. The timers can be operated in both the 32-bit Segmented and Linear modes.
- Reception of frames by the Receive Unit (RU). The SCB controls the RU by specifying the address of the Receive Frame Area and by starting, suspending, resuming, or aborting frame reception.
- Acknowledgment of events that cause interrupts.
- Resetting the chip.

The 82596 sends status reports to the CPU via the System Control Block. The SCB contains four types of status reports.

- The cause of the current interrupts. These interrupts are caused by one or more of the following 82596 events.
  - The Command Unit completes an Action Command that has its I bit set.
  - The Receive Unit receives a frame.
  - The Command Unit becomes inactive.
  - The Receive Unit becomes not ready.
- The status of the Command Unit.
- The status of the Receive Unit.
- Status reports from the 82596 regarding reception of corrupted frames.

Events can be cleared only by CPU acknowledgment. If some events are not acknowledged by the ACK field the Interrupt signal (INT) will be reissued after Channel Attention (CA) is processed. Furthermore, if a new event occurs while an interrupt is set, the interrupt is temporarily cleared to trigger edge-triggered interrupt controllers.

The CPU uses the Channel Attention line to cause the 82596 to examine the SCB. This signal is trailing-edge triggered—the 82596 latches CA on the trailing edge. The latch is cleared by the 82596 before the SCB control command is read.

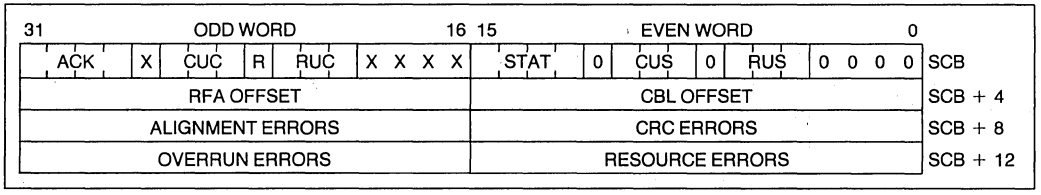


Figure 18. SCB—82586 Mode

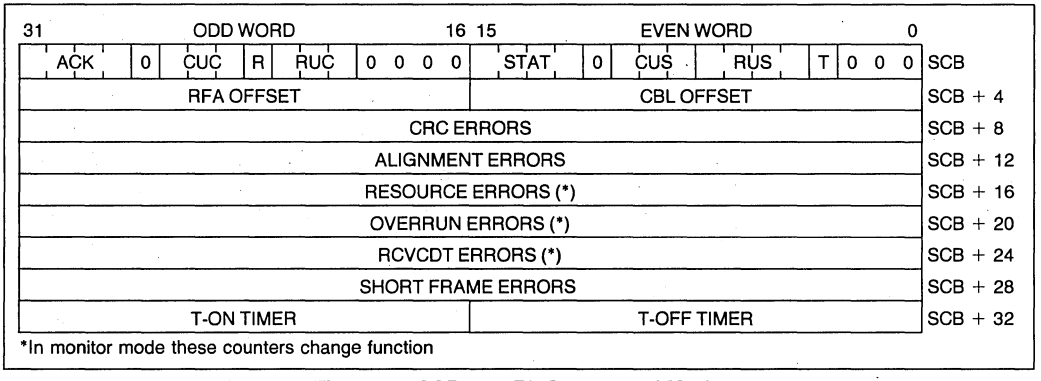


Figure 19. SCB—32-Bit Segmented Mode

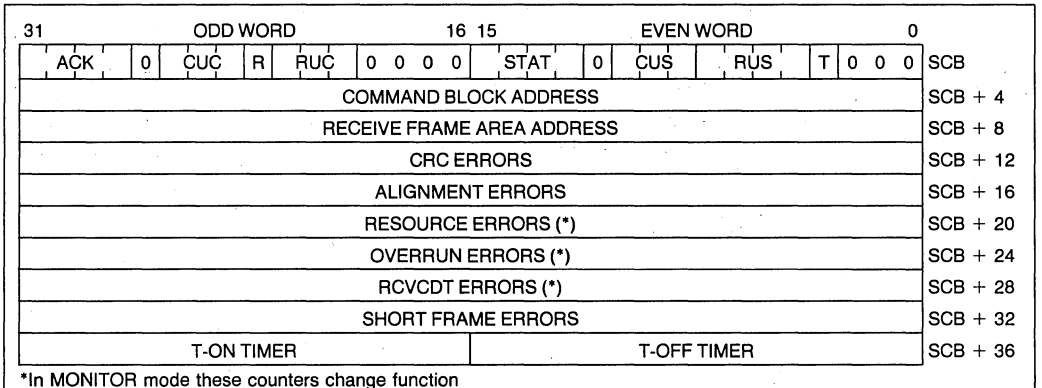
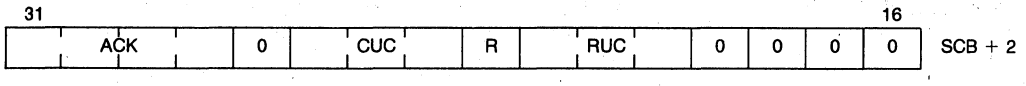


Figure 20. SCB—Linear Mode

Command Word



These bits specify the action to be performed as a result of a CA. This word is set by the CPU and cleared by the 82596. Defined bits are:

Bit 31 ACK-CX — Acknowledges that the CU completed an Action Command.

Bit 30 ACK-FR — Acknowledges that the RU received a frame.

Bit 29 ACK-CNA — Acknowledges that the Command Unit became not active.

Bit 28 ACK-RNR — Acknowledges that the Receive Unit became not ready.

Bits 24–26 CUC — (3 bits) This field contains the command to the Command Unit. Valid values are:

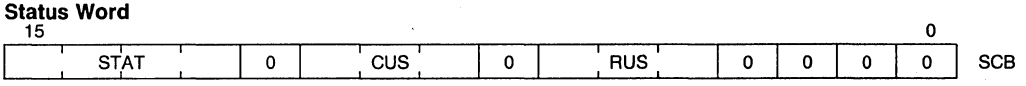
- 0 — NOP (does not affect current state of the unit).
- 1 — Start execution of the first command on the CBL. If a command is executing, complete it before starting the new CBL. The beginning of the CBL is in CBL OFFSET (address).
- 2 — Resume the operation of the Command Unit by executing the next command. This operation assumes that the Command Unit has been previously suspended.
- 3 — Suspend execution of commands on CBL after current command is complete.
- 4 — Abort current command immediately.
- 5 — Loads the Bus Throttle timers so they will be initialized with their new values after the active timer (T-ON or T-OFF) reaches Terminal Count. If no timer is active new values will be loaded immediately. This command is not valid in 82586 mode.
- 6 — Loads and immediately restarts the Bus Throttle timers with their new values. This command is not valid in 82586 mode.
- 7 — Reserved.

Bit 23 RESET — Reset chip (logically the same as hardware RESET).

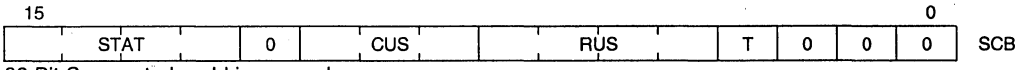
Bits 20–22 RUC — (3 bits) This field contains the command to the Receive Unit. Valid values are:

- 0 — NOP (does not alter current state of unit).
- 1 — Start reception of frames. The beginning of the RFA is contained in the RFA OFFSET (address). If a frame is being received complete reception before starting.
- 2 — Resume frame reception (only when in suspended state).
- 3 — Suspend frame reception. If a frame is being received complete its reception before suspending.
- 4 — Abort receiver operation immediately.
- 5–7 — Reserved.

Status Word



82586 mode



32-Bit Segmented and Linear mode.

Indicates the status of the 82596. This word is modified only by the 82596. Defined bits are:

Bit 15 CX — The CU finished executing a command with its I (interrupt) bit set.

Bit 14 FR — The RU finished receiving a frame.

Bit 13 CNA — The Command Unit left the Active state.

Bit 12 RNR — The Receive Unit left the Ready state.

Bits 8–10 CUS — (3 bits) This field contains the status of the command unit. Valid values are:

0 — Idle

1 — Suspended

2 — Active

3–7 — Not used

Bits 4–7 RUS — This field contains the status of the receive unit. Valid values are:

0h (0000) — Idle

1h (0001) — Suspended

2h (0010) — No Resources. This bit indicates both no resources due to lack of RFDs in the RDL and no resources due to lack of RBDs in the FBL.

4h (0100) — Ready

Ah (1010) — No resources due to no more RBDs (not in the 82586 mode).

Ch (1100) — No more RBDs (not in 82586 mode)

No other combinations are allowed

Bit 3 T — Bus Throttle timers loaded (not in 82586 mode).

SCB OFFSET ADDRESSES

CBL Offset (Address)

In 82586 and 32-bit Segmented modes this 16-bit quantity indicates the offset portion of the address for the first Command Block on the CBL. In Linear mode it is a 32-bit linear address for the first Command Block on the CBL. It is accessed only if CUC equals Start.

RFA Offset (Address)

In 82586 and 32-bit Segmented modes this 16-bit quantity indicates the offset portion of the address for the Receive Frame Area. In Linear mode it is a 32-bit linear address for the Receive Frame Area. It is accessed only if RUC equals Start.

SCB STATISTICAL COUNTERS

Statistical Counter Operation

- The CPU is responsible for clearing all error counters before initializing the 82596. The 82596 updates these counters by reading them, adding 1, and then writing them back to the SCB.
- The counters are wraparound counters. After reaching FFFFFFFFh the counters wrap around to zero.
- The 82596 updates the required counters for each frame. It is possible for more than one counter to be updated; multiple errors will result in all affected counters being updated.
- The 82596 executes the read-counter/increment/write-counter operation without relinquishing the bus (locked operation). This is to ensure that no logical contention exists between the 82596 and the CPU due to both attempting to write to the counters simultaneously. In the dual-port memory configuration the CPU should not execute any write operation to a counter if $\overline{LOCK}$ is asserted.
- The counters are 32-bits wide and their behavior is fully compatible with the IEEE 802.3 standard. The 82596 supports all relevant statistics (mandatory, optional, and desired) through the status of the transmit and receive header and directly through SCB statistics.

CRCERRS

This 32-bit quantity contains the number of aligned frames discarded because of a CRC error. This counter is updated, if needed, regardless of the RU state.

ALNERRS

This 32-bit quantity contains the number of frames that both are misaligned (i.e., where $\overline{CRS}$ deasserts on a nonoctet boundary) and contain a CRC error. The counter is updated, if needed, regardless of the RU state.

SHRTFRM

This 32-bit quantity contains the number of received frames shorter than the minimum frame length.

The last three counters change function in monitor mode.

RSCERRS

This 32-bit quantity contains the number of good frames discarded because there were no resources to contain them. Frames intended for a host whose RU is in the No Receive Resources state, fall into this category. This counter is updated only if the RU is in the No Resources state. When in Monitor mode this counter counts the total number of frames—good and bad.

OVRNERRS

This 32-bit quantity contains the number of frames known to be lost because the local system bus was not available. If the traffic problem lasts longer than the duration of one frame, the frames that follow the first are lost without an indicator, and they are not counted. This counter is updated, if needed, regardless of the RU state.

This 32-bit counter contains the number of collisions detected during frame reception. This counter will only be updated if at least 64 bytes of data are received before the collision occurs. If a collision occurs before 64 bytes of data are received, the frame is counted as a short frame. If the collision occurs in the preamble, no counters are incremented.

ACTION COMMANDS AND OPERATING MODES

This section lists all the Action Commands of the Command Unit Command Block List (CBL). Each command contains the Command field, the Status and Control fields, the link to the next Action Command, and any command-specific parameters. There are three basic types of action commands: 82596 Configuration and Setup, Transmission, and Diagnostics. The following is a list of the actual commands.

- NOP
- Individual Address Setup
- Configure
- MC Setup
- Transmit
- TDR
- Dump
- Diagnose

The 82596 has three addressing modes. In the 82586 mode all the Action Commands look exactly like those of the 82586.

- **82586 Mode.** The 82596 software and memory structure is compatible with the 82586.
- **32-Bit Segmented Mode.** The 82596 can access the entire system memory and use the two new memory structures—Simplified and Flexible—while still using the segmented approach. This does not require any significant changes to existing software.
- **Linear Mode.** The 82596 operates in a flat, linear, 4 gigabyte memory space without segmentation. It can also use the two new memory structures.

In the 32-bit Segmented mode there are some differences between the 82596 and 82586 action commands, mainly in programming and activating new 82596 features. Those bits marked "don't care" in the compatible mode are not checked; however, we strongly recommend that those bits all be zeroes; this will allow future enchancements and extensions.

In the Linear mode all of the address offsets become 32-bit address pointers. All new 82596 features are accessible in this mode, and all bits previously marked "don't care" must be zeroes.

The Action Commands, and all other 82596 memory structures, must begin on even byte boundaries, i.e., they must be word aligned.

NOP

This command results in no action by the 82596 except for those performed in the normal command processing. It is used to manipulate the CBL manipulation. The format of the NOP command is shown in Figure 21.

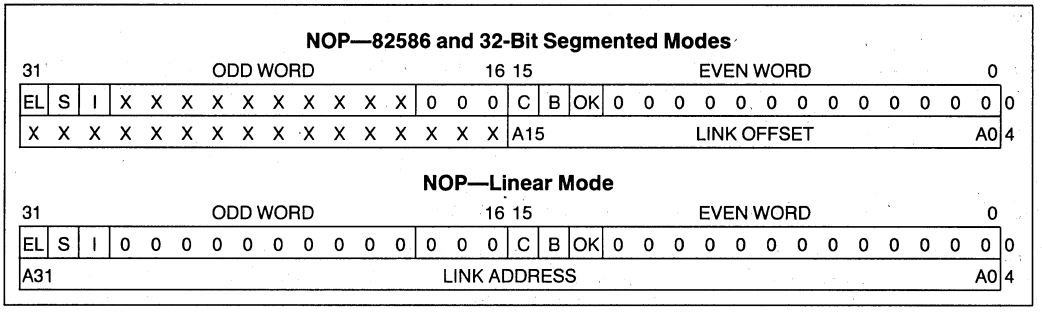


Figure 21

where:

LINK POINTER — In the 82586 or 32-bit Segmented modes this is a 16-bit offset to the next Command Block. In the Linear mode this is the 32-bit address of the next Command Block.

EL — If set, this bit indicates that this command block is the last on the CBL.

S — If set to one, suspend the CU upon completion of this CB.

I — If set to one, the 82596 will generate an interrupt after execution of the command is complete. If I is not set to one, the CX bit will not be set.

CMD (bits 16–18) — The NOP command. Value: 0h.

Bits 19–28 — Reserved (zero in the 32-bit Segmented and Linear modes).

C — This bit indicates the execution status of the command. The CPU initially resets it to zero when the Command Block is placed on the CBL. Following a command Completion, the 82596 will set it to one.

B — This bit indicates that the 82596 is currently executing the NOP command. It is initially reset to zero by the CPU. The 82596 sets it to one when execution begins and to zero when execution is completed. This bit is also set when the 82596 prefetches the command.

NOTE:

The C and B bits are modified in one operation.

OK — Indicates that the command was executed without error. If set to one no error occurred (command executed OK). If zero an error occured.

Individual Address Setup

This command is used to load the 82596 with the Individual Address. This address is used by the 82596 for inserting the Source Address during transmission and recognizing the Destination Address during reception. After RESET, and prior to Individual Address Setup Command execution, the 82596 assumes the Broadcast Address is the Individual Address in all aspects, i.e.:

- This will be the Individual Address Match reference.
- This will be the Source Address of a transmitted frame (for AL-LOC=0 mode only).

The format of the Individual Address Setup command is shown in Figure 22.

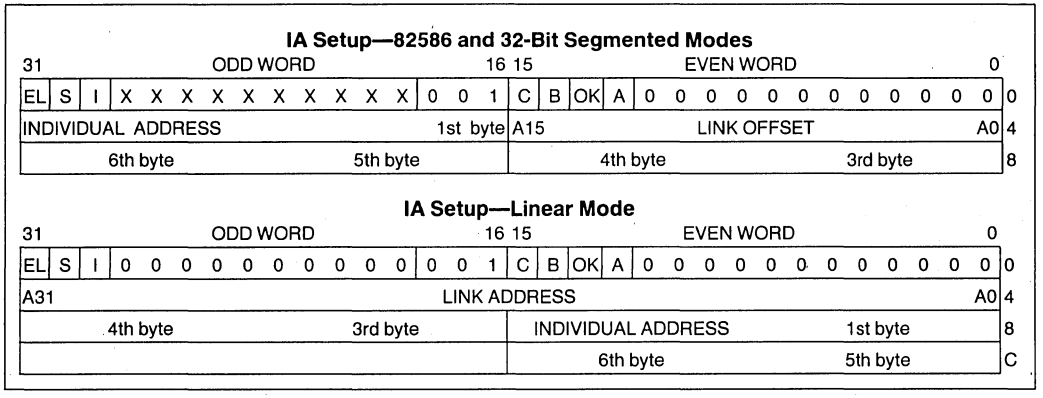


Figure 22

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted, and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (zero in the 32-bit Segmented and Linear modes).

CMD (bits 16–18) — The Address Setup command. Value: 1h.

INDIVIDUAL ADDRESS — The individual address of the node, 0 to 6 bytes long.

The least significant bit of the Individual Address must be zero for Ethernet (see the Command Structure). However, no enforcement of 0 is provided by the 82596. Thus, an Individual Address with 1 as its least significant bit is a valid Individual Address in all aspects.

The default address length is 6 bytes long, as in 802.3. If a different length is used the IA Setup command should be executed after the Configure command.

Configure

The Configure command loads the 82596 with its operating parameters. It allows changing some of the parameters by specifying a byte count less than the maximum number of configuration bytes (11 in the 82586 mode, 14 in the 32-Bit Segmented and Linear modes). The 82596 configuration depends on its mode of operation. When configuring the 12th byte (Byte 11 undefined) in 82586 mode this byte should be all ones.

- In the 82586 mode the maximum number of configuration bytes is 12. Any number larger than 12 will be reduced to 12 and any number less than 4 will be increased to 4.
- The additional features of the serial side are disabled in the 82586 mode.
- In both the 32-Bit Segmented and Linear modes there are four additional configuration bytes, which hold parameters for additional 82596 features. If these parameters are not accessed, the 82596 will follow their default values.
- For more detailed information refer to the 32-Bit LAN Components User's Manual.

The format of the Configure command is shown in Figure 23, 24 and 25.

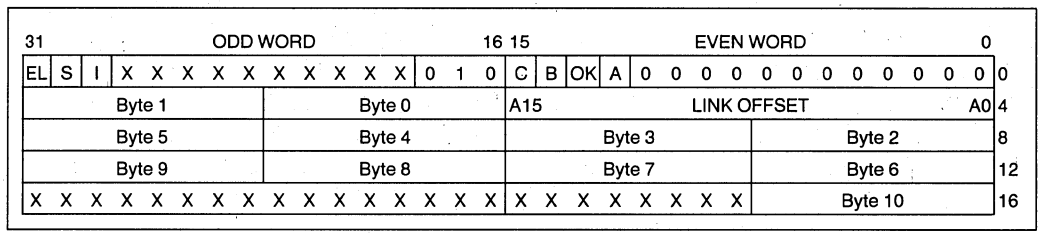


Figure 23. CONFIGURE—82586 Mode

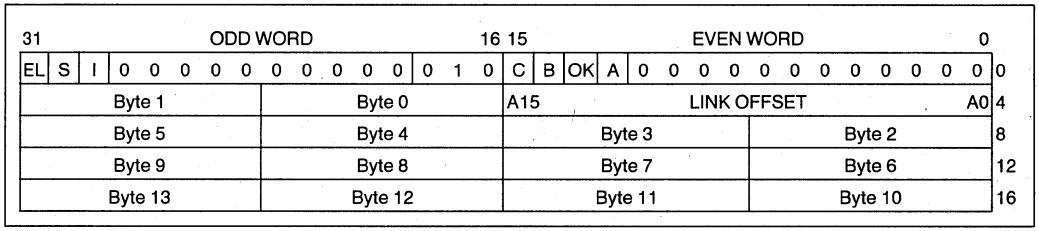


Figure 24. CONFIGURE—32-Bit Segmented Mode

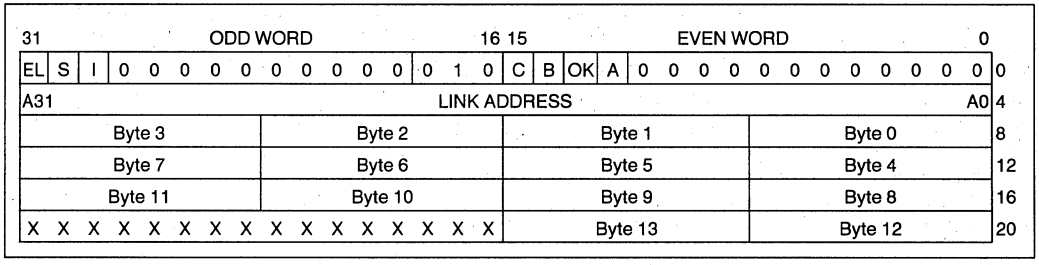


Figure 25. CONFIGURE—Linear Mode

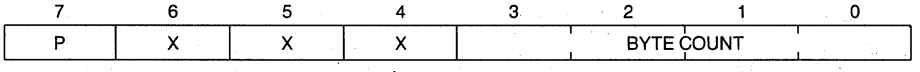
LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to a CU Abort control command. If 1, then the command was aborted and if necessary it should be repeated. If this bit is 0, the command was not aborted.

Bits 19–28 — Reserved (zero in the 32-Bit Segmented and Linear Modes)

CMD (bits 16–18) — The CONFIGURE command. Value: 2h.

The interpretation of the fields follows:

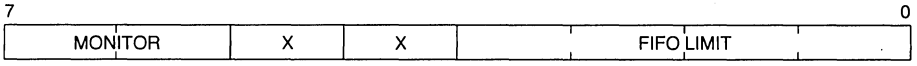


BYTE 0

BYTE CNT (Bits 0–3) — Byte Count. Number of bytes, including this one, that hold parameters to be configured.

PREFETCHED (Bit 7) — Enable the 82596 to write the prefetched bit in all prefetch RBDs.

NOTE:
The P bit is valid only in the new memory structure modes. In 82586 mode this bit is disabled (i.e., no prefetched mark).

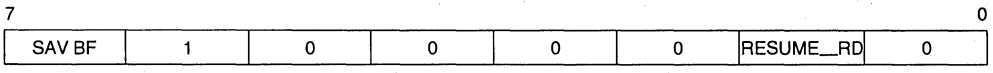


BYTE 1

FIFO Limit (Bits 0–3) — FIFO limit.

MONITOR# (Bits 6–7) — Receive monitor options. If the Byte Count of the configure command is less than 12 bytes then these Monitor bits are ignored.

DEFAULT: C8h

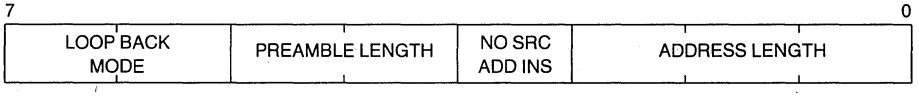


BYTE 2

SAV BF (Bit 7) — 0—Received bad frames are not saved in the memory.
1—Received bad frames are saved in the memory.

DEFAULT: 40h

RESUME_RD (Bit 1) — 0 — The 82596 does not reread the next CB on the list when a CU Resume Control Command is issued.
1 — The 82596 will reread the next CB on the list when a CU Resume Control Command is issued. This is available only on the 82596B stepping.



BYTE 3

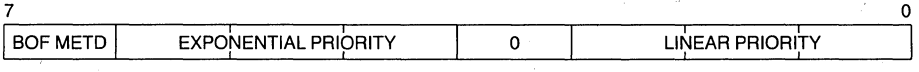
ADR LEN (Bits 0–2) — Address length (any kind).

NO SCR ADD INS (Bit 3) — No Source Address Insertion.
In the 82586 this bit is called AL LOC.

PREAM LEN (Bits 4–5) — Preamble length.

LP BCK MODE (Bits 6–7) — Loopback mode.

DEFAULT: 26h



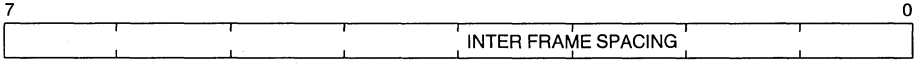
BYTE 4

LIN PRIO (Bits 0–2) — Linear Priority.

EXP PRIO (Bits 4–6) — Exponential Priority.

BOF METD (Bit 7) — Exponential Backoff method.

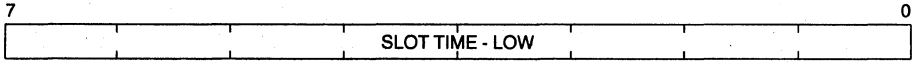
DEFAULT: 00h



BYTE 5

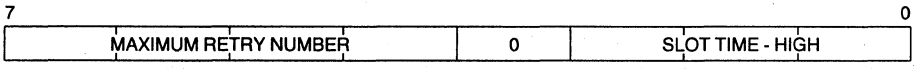
INTERFRAME SPACING — Interframe spacing.

DEFAULT: 60h



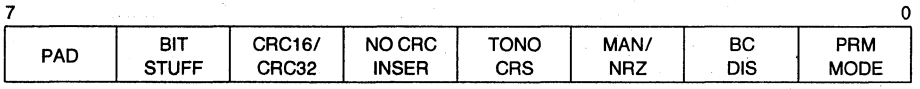
BYTE 6

SLOT TIME (L)	Slot time, low byte.
DEFAULT: 00h	



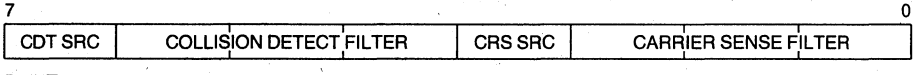
BYTE 7

SLOT TIME (H) (Bits 0–2)	Slot time, high part.
RETRY NUM (Bits 4–7)	Number of transmission retries on collision.
DEFAULT: F2h	



BYTE 8

PRM (Bit 0)	Promiscuous mode.
BC DIS (Bit 1)	Broadcast disable.
MANCH/NRZ (Bit 2)	Manchester or NRZ encoding. See specific timing requirements for TXC in Manchester mode.
TONO CRS (Bit 3)	Transmit on no CRS.
NOCRC INS (Bit 4)	No CRC insertion.
CRC-16/CRC-32 (Bit 5)	CRC type.
BIT STF (Bit 6)	Bit stuffing.
PAD (Bit 7)	Padding.
DEFAULT: 00h	



BYTE 9

CRSF (Bits 0–2)	Carrier Sense filter (length).
CRS SRC (Bit 3)	Carrier Sense source.
CDTF (Bits 4–6)	Collision Detect filter (length).
CDT SRC (Bit 7)	Collision Detect source.
DEFAULT: 00h	

7							0
MINIMUM FRAME LENGTH							

BYTE 10

MIN FRAME LEN — Minimum frame length.

DEFAULT: 40h

7							0
MONITOR		MC__ALL	CDBSAC	AUTOTX	CRCINM	LNGFLD	PRECRS

BYTE 11

PRECRS (Bit 0) — Preamble until Carrier Sense

LNGFLD (Bit 1) — Length field. Enables padding at the End-of-Carrier framing (802.3).

CRCINM (Bit 2) — Rx CRC appended to the frame in memory.

AUTOTX (Bit 3) — Auto retransmit when a collision occurs during the preamble.

CDBSAC (Bit 4) — Collision Detect by source address recognition.

MC__ALL (Bit 5) — Enable to receive all MC frames.

MONITOR (Bits 6–7) — Receive monitor options.

DEFAULT: FFH

7							0
0	FDX	0	0	0	0	0	0

BYTE 12

FDX (Bit 6) — Enables Full Duplex operation.

DEFAULT: 00h

7							0
DIS__BOF	MULT__IA	1	1	1	1	1	1

BYTE 13

MULT__IA (Bit 6) — Multiple individual address.

DIS__BOF (Bit 7) — Disable the backoff algorithm.

DEFAULT: 3Fh

A reset (hardware or software) configures the 82596 according to the following defaults.

Table 4. Configuration Defaults

	Parameter	Default Value	Units/Meaning
	ADDRESS LENGTH	**6	Bytes
	A/L FIELD LOCATION	0	Located in FD
*	AUTO RETRANSMIT	1	Auto Retransmit Enable
	BITSTUFFING/EOC	0	EOC
	BROADCAST DISABLE	0	Broadcast Reception Enabled
*	CDBSAC	1	Disabled
	CDT FILTER	0	Bit Times
	CDT SRC	0	External Collision Detection
*	CRC IN MEMORY	1	CRC Not Transferred to Memory
	CRC-16/CRC-32	**0	CRC-32
	CRS FILTER	0	0 Bit Times
	CRS SRC	0	External CRS
*	DISBOF	0	Backoff Enabled
	EXT LOOPBACK	0	Disabled
	EXPONENTIAL PRIORITY	**0	802.3 Algorithm
	EXPONENTIAL BACKOFF METHOD	**0	802.3 Algorithm
*	FULL DUPLEX (FDX)	0	CSMA/CD Protocol (No FDX)
	FIFO THRESHOLD	8	TX: 32 Bytes, RX: 64 Bytes
	INT LOOPBACK	0	Disabled
	INTERFRAME SPACING	**96	Bit Times
	LINEAR PRIORITY	**0	802.3 Algorithm
*	LENGTH FIELD	1	Padding Disabled
	MIN FRAME LENGTH	**64	Bytes
*	MC ALL	1	Disabled
*	MONITOR	11	Disabled
	MANCHESTER/NRZ	0	NRZ
*	MULTI IA	0	Disabled
	NUMBER OF RETRIES	**15	Maximum Number of Retries
	NO CRC INSERTION	0	CRC Appended to Frame
	PREFETCH BIT IN RBD	0	Disabled (Valid Only in New Modes)
	PREAMBLE LENGTH	**7	Bytes
*	Preamble Until CRS	1	Disabled
	PROMISCUOUS MODE	0	Address Filter On
	PADDING	0	No Padding
	SLOT TIME	**512	Bit Times
	SAVE BAD FRAME	0	Discards Bad Frames
	TRANSMIT ON NO CRS	0	Disabled

NOTES:
1. This configuration setup is compatible with the IEEE 802.3 specification.
2. The Asterisk "*" signifies a new configuration parameter not available in the 82586.
3. The default value of the Auto retransmit configuration parameter is enabled(1).
4. Double Asterisk "**" signifies IEEE 802.3 requirements.

Multicast-Setup

This command is used to load the 82596 with the Multicast-IDs that should be accepted. As noted previously, the filtering done on the Multicast-IDs is not perfect and some unwanted frames may be accepted. This command resets the current filter and reloads it with the specified Multicast-IDs. The format of the Multicast-addresses setup command is:

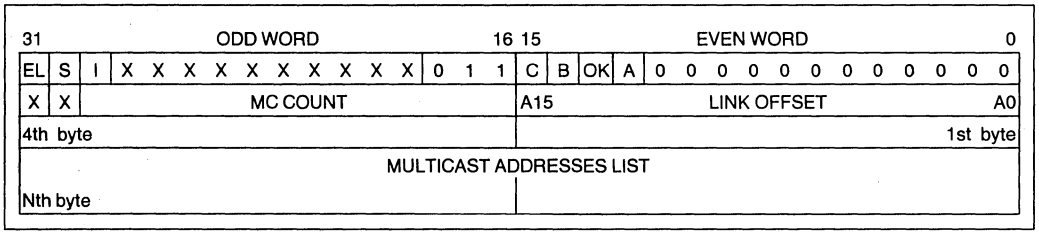


Figure 26. MC Setup—82586 and 32-Bit Segmented Modes

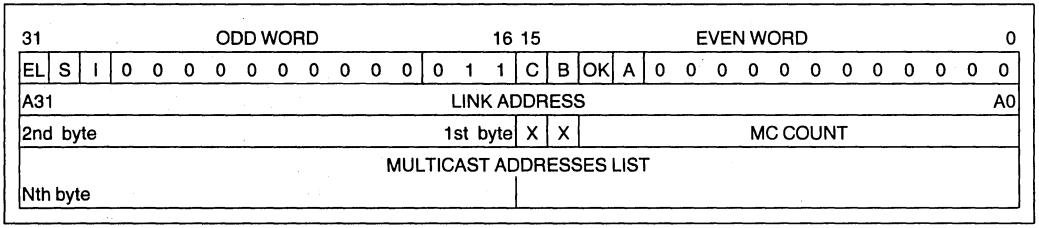


Figure 27. MC Setup—Linear Mode

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to a CU Abort control command. If one, then the command was aborted and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (0 in both the 32-Bit Segmented and Linear Modes).

CMD (bits 16–18) — The MC SETUP command value: 3h.

MC-CNT — This 14-bit field indicates the number of bytes in the MC LIST field. The MC CNT must be a multiple of the ADDR LEN; otherwise, the 82596 reduces the MC CNT to the nearest ADDR LEN multiple. MC CNT = 0 implies resetting the Hash table which is equivalent to disabling the Multicast filtering mechanism.

MC LIST — A list of Multicast Addresses to be accepted by the 82596. The least significant bit of each MC address must be 1.

NOTE:

The list is sequential; i.e., the most significant byte of an address is immediately followed by the least significant byte of the next address.

— When the 82596 is configured to recognize multiple Individual Address (Multi-IA), the MC-Setup command is also used to set up the Hash table for the individual address.

The least significant bit in the first byte of each IA address must be 0.

Transmit

This command is used to transmit a frame of user data onto the serial link. The format of a Transmit command is as follows.

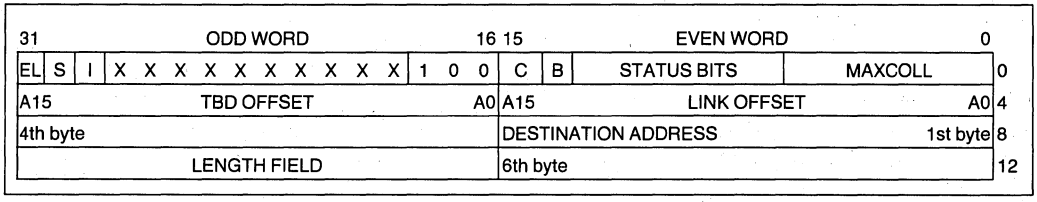


Figure 28. TRANSMIT—82586 Mode

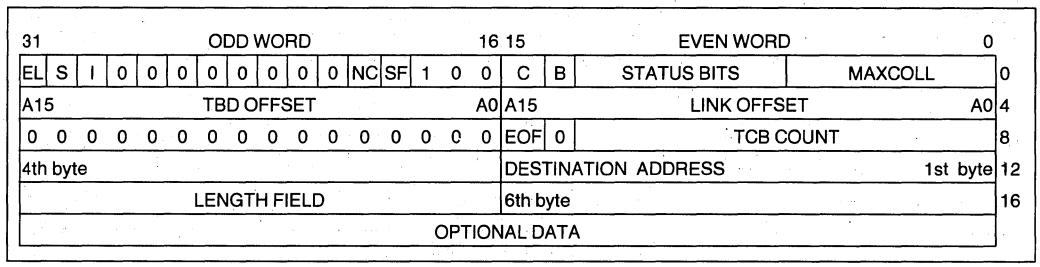


Figure 29. TRANSMIT—32-Bit Segmented Mode

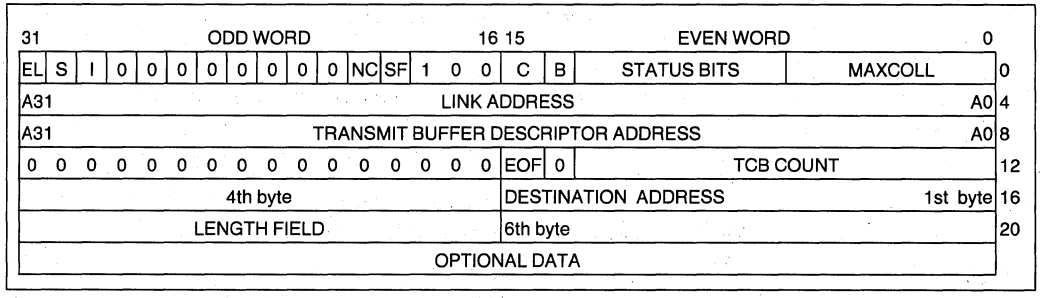
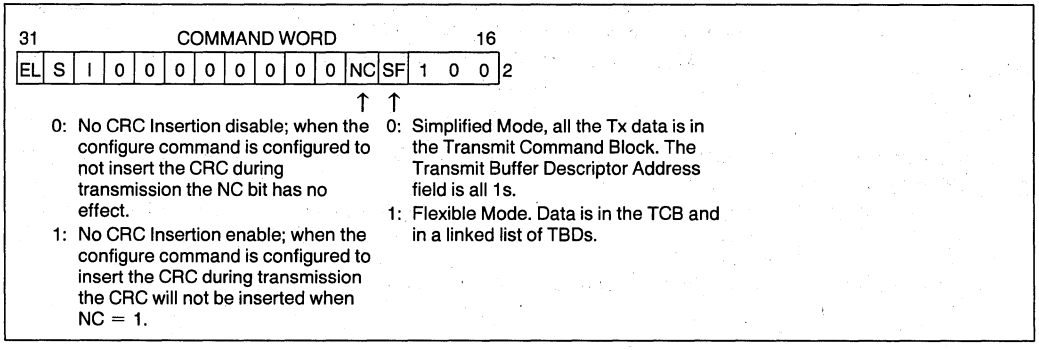


Figure 30. TRANSMIT—Linear Mode



where:

EL, B, C, I, S	— As per standard Command Block (see the NOP command for details).
OK (Bit 13)	— Error free completion.
A (Bit 12)	— Indicates that the command was abnormally terminated due to CU Abort control command. If 1, then the command was aborted, and if necessary it should be repeated. If this bit is 0, the command was not aborted.
Bits 19–28	— Reserved (0 in the 32-bit Segmented and Linear modes).
CMD (Bits 16–18)	— The transmit command: 4h.
Status Bit 11	— Late collision. A late collision (a collision after the slot time is elapsed) is detected.
Status Bit 10	— No Carrier Sense signal during transmission. Carrier Sense signal is monitored from the end of Preamble transmission until the end of the Frame Check Sequence for TONOCRS = 1 (Transmit On No Carrier Sense mode) it indicates that transmission has been executed despite a lack of CRS. For TONOCRS = 0 (Ethernet mode), this bit also indicates unsuccessful transmission (transmission stopped when lack of Carrier Sense has been detected).
Status Bit 9	— Transmission unsuccessful (stopped) due to Loss of $\overline{\text{CTS}}$.
Status Bit 8	— Transmission unsuccessful (stopped) due to DMA Underrun; i.e., the system did not supply data for transmission.
Status Bit 7	— Transmission Deferred, i.e., transmission was not immediate due to previous link activity.
Status Bit 6	— Heartbeat Indicator, Indicates that after a previously performed transmission, and before the most recently performed transmission, (Interframe Spacing) the CDT signal was monitored as active. This indicates that the Ethernet Transceiver Collision Detect logic is performing properly. The Heartbeat is monitored during the Interframe Spacing period.
Status Bit 5	— Transmission attempt was stopped because the number of collisions exceeded the maximum allowable number of retries.
Status Bit 4	— 0 (Reserved).
MAX-COL (Bits 3–0)	— The number of Collisions experienced during this frame. Max Col = 0 plus S5 = 1 indicates 16 collisions.
LINK OFFSET	— As per standard Command Block (see the NOP Command for details)
TBD POINTER	— In the 82586 and 32-bit Segmented modes this is the offset of the first Tx Buffer Descriptor containing the data to be transmitted. In the Linear mode this is the 32-bit address of the first Tx Buffer Descriptor on the list. If the TBD POINTER is all 1s it indicates that no TBD is used.
DEST ADDRESS	— Contains the Destination Address of the frame. The least significant bit (MC) indicates the address type. MC = 0: Individual Address. MC = 1: Multicast or Broadcast Address. If the Destination Address bits are all 1s this is a Broadcast Address.
LENGTH FIELD	— The contents of this 2-byte field are user defined. In 802.3 it contains the length of the data field. It is placed in memory in the same order it is transmitted; i.e., most significant byte first, least significant byte second.
TCB COUNT	— This 14-bit counter indicates the number of bytes that will be transmitted from the Transmit Command Block, starting from the third byte after the TCB COUNT field (address $n+12$ in the 32-bit Segmented mode, $N+16$ in the Linear mode). The TCB COUNT field can be any number of bytes (including an odd byte), this allows the user to transmit a frame with a header having an odd number of bytes. The TCB COUNT field is not used in the 82586 mode.
EOF Bit	— Indicates that the whole frame is kept in the Transmit Command Block. In the Simplified memory model it must be always asserted.

The interpretation of what is transmitted depends on the No Source Address insertion configuration bit and the memory model being used.

NOTES:

1. The Destination Address and the Length Field are sequential. The Length Field immediately follows the most significant byte of the Destination Address.
2. In case the 82596 is configured with No Source Address insertion bit equal to 0, the 82596 inserts its configured Source Address in the transmitted frame.
   - In the 82586 mode, or when the Simplified memory model is used, the Destination and Length fields of the transmitted frame are taken from the Transmit Command Block.
   - If the FLEXIBLE memory model is used, the Destination and Length fields of the transmitted frame can be found either in the TCB or TBD, depending on the TCB COUNT.
3. If the 82596 is configured with the Address/Length Field Location equal to 1, the 82596 does not insert its configured Source Address in the transmitted frame. The first (2 × Address Length) + 2 bytes of the transmitted frame are interpreted as Destination Address, Source Address, and Length fields respectively. The location of the first transmitted byte depends on the operational mode of the 82596:
   - In the 82586 mode, it is always the first byte of the first Tx Buffer.
   - In both the 32-bit Segmented and Linear modes it depends on the SF bit and TCB COUNT:
     - — In the Simplified memory mode the first transmitted byte is always the third byte after the TCB COUNT field.
     - — In the Flexible mode, if the TCB COUNT is greater than 0 then it is the third byte after the TCB COUNT field. If TCB COUNT equals 0 then it is first byte of the first Tx Buffer.
   - Transmit frames shorter than six bytes are invalid. The transmission will be aborted (only in 82586 mode) because of a DMA Underrun.
4. Frames which are aborted during transmission are jammed. Such an interruption of transmission can be caused by any reason indicated by any of the status bits 8, 9, 10 and 12.

Jamming Rules

1. Jamming will not start before completion of preamble transmission.
2. Collisions detected during transmission of the last 11 bits will not result in jamming.

The format of a Transmit Buffer Descriptor is:

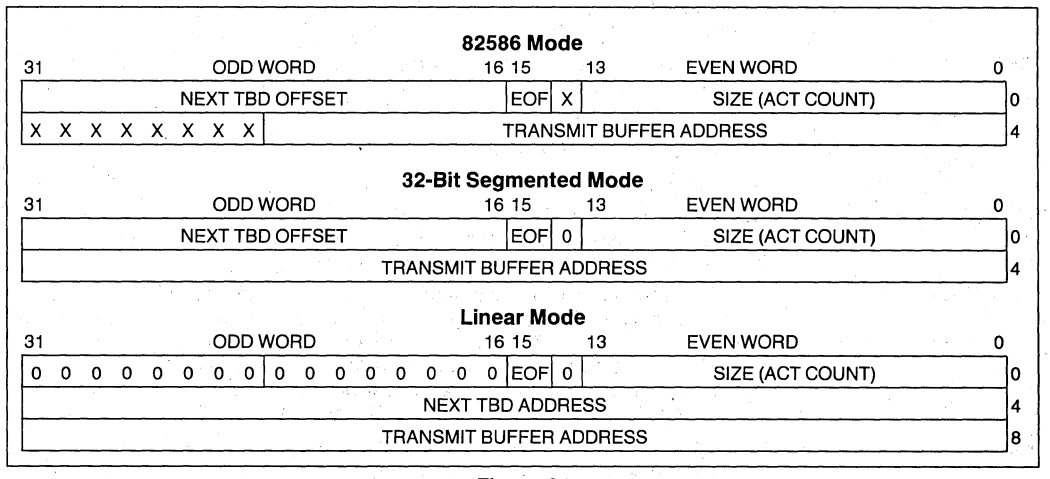


Figure 31

where:

EOF — This bit indicates that this TBD is the last one associated with the frame being transmitted. It is set by the CPU before transmit.

SIZE (ACT COUNT) — This 14-bit quantity specifies the number of bytes that hold information for the current buffer. It is set by the CPU before transmission.

NEXT TBD ADDRESS — In the 82586 and 32-bit Segmented modes, it is the offset of the next TBD on the list. In the Linear mode this is the 32-bit address of the next TBD on the list. It is meaningless if EOF = 1.

BUFFER ADDRESS — The starting address of the memory area that contains the data to be sent. In the 82586 mode, this is a 24-bit address (A31–A24 are considered to be zero). In the 32-bit Segmented and Linear modes this is a 32-bit address. This buffer can be byte aligned for the 82596 B step.

TDR

This operation activates Time Domain Reflectomet, which is a mechanism to detect open or short circuits on the link and their distance from the diagnosing station. The TDR command has no parameters. The TDR transmit sequence was changed, compared to the 82586, to form a regular transmission. The TDR command is designed to be used statically. Make sure that both the CU and RU are idle before attempting a TDR command. The TDR bit stream is as follows.

— Preamble

— Source address

— Another Source address (the TDR frame is transmitted back to the sending station, so DEST ADR = SRC ADR).

— Data field containing 7Eh patterns.

— Jam Pattern, which is the inverse CRC of the transmitted frame.

Maximum length of the TDR frame is 2048 bits. If the 82596 senses collision while transmitting the TDR frame it transmits the jam pattern and stops the transmission. The 82596 then triggers an internal timer (STC); the timer is reset at the beginning of transmission and reset if CRS is returned. The timer measures the time elapsed from the start of transmission until an echo is returned. The echo is indicated by Collision Detect going active or a drop in the Carrier Sense signal. The following table lists the possible cases that the 82596 is able to analyze.

Conditions of TDR as Interpreted by the 82596

Transceiver Type / Condition	Ethernet	Non Ethernet
Carrier Sense was inactive for 2048-bit-time periods	Short or Open on the Transceiver Cable	NA
Carrier Sense signal dropped	Short on the Ethernet cable	NA
Collision Detect went active	Open on the Ethernet cable	Open on the Serial Link
The Carrier Sense Signal did not drop or the Collision Detect did not go active within 2048-bit time period	No Problem	No Problem

An Ethernet transceiver is defined as one that returns transmitted data on the receive pair and activates the Carrier Sense Signal while transmitting. A Non-Ethernet Transceiver is defined as one that does not do so.

The format of the Time Domain Reflectometer command is:

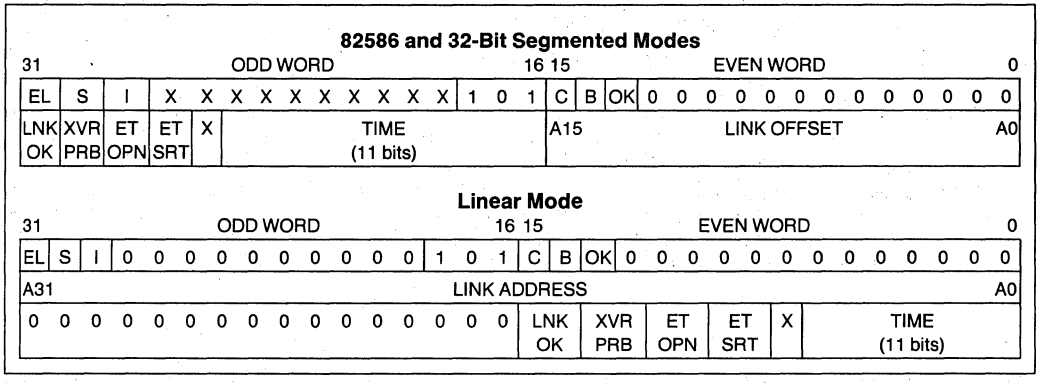


Figure 32. TDR

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details).

A — Indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted, and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (0 in the 32-bit Segmented and Linear Modes).

CMD (Bits 16–18) — The TDR command. Value: 5h.

TIME — An 11-bit field that specifies the number of TxC cycles that elapsed before an echo was observed. No echo is indicated by a reception consisting of "1s" only. Because the network contains various elements such as transceiver links, transceivers, Ethernet, repeaters etc., the TIME is not exactly proportional to the problems distance.

LNK OK (Bit 15) — No link problem identified. TIME = 7FFh.

XCVR PRB (Bit 14) — Indicates a Transceiver problem. Carrier Sense was inactive for 2048-bit time period. LNK OK = 0. TIME = 7FFh.

ET OPN (Bit 13) — The transmission line is not properly terminated. Collision Detect went active and LNK OK = 0.

ET SRT (Bit 12) — There is a short circuit on the transmission line. Carrier Sense Signal dropped and LNK OK = 0.

DUMP

This command causes the contents of various 82596 registers to be placed in a memory area specified by the user. It is supplied as a 82596 self-diagnostic tool, and to provide registers of interest to the user. The format of the DUMP command is:

82586 and 32-Bit Segmented Modes

31			ODD WORD									16	15					EVEN WORD											0
EL	S	I	X	X	X	X	X	X	X	X	X	1	1	0	C	B	OK	0	0	0	0	0	0	0	0	0	0	0	0
A15			BUFFER OFFSET								A0	A15			LINK OFFSET													A0	

Linear Mode

31			ODD WORD									16	15					EVEN WORD											0
EL	S	I	X	X	X	X	X	X	X	X	X	1	1	0	C	B	OK	0	0	0	0	0	0	0	0	0	0	0	0
A31			LINK ADDRESS																										A0
A31			BUFFER ADDRESS																										A0

Figure 33. Dump

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details).

OK — Indicates error free completion.

Bits 19–28 — Reserved (0 in the 32-bit Segmented and Linear Modes).

CMD (Bits 16–18) — The Dump command. Value: 6h.

BUFFER POINTER — In the 82586 and 32-bit Segmented modes this is the 16-bit-offset portion of the dump area address. In the Linear mode this is the 32-bit linear address of the dump area.

Dump Area Information Format

- The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586. The compatible data will be marked with an asterisk.
- In 82586 mode the dump area is 170 bytes.
- The DUMP area format of the 32-bit Segmented and Linear modes is described in Figure 35.
- The size of the dump area of the 32-bit Segmented and Linear modes is 304 bytes.
- When the Dump is executed by the Port command an extra word will be appended to the Dump Area. The extra word is a copy of the Dump Area status word (containing the C, B, and OK Bits). The C and OK Bits are set when the 82596 has completed the Port Dump command.

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
DMA CONTROL REGISTER	00
CONFIGURE BYTES* 3, 2	02
CONFIGURE BYTES* 5, 4	04
CONFIGURE BYTES* 7, 6	06
CONFIGURE BYTES* 9, 8	08
CONFIGURE BYTES* 10	0A
I.A. BYTES 1, 0*	0C
I.A. BYTES 3, 2*	0E
I.A. BYTES 5, 4*	10
LAST T.X. STATUS*	12
T.X. CRC BYTES 1, 0*	14
T.X. CRC BYTES 3, 2*	16
R.X. CRC BYTES 1, 0*	18
R.X. CRC BYTES 3, 2*	1A
R.X. TEMP MEMORY 1, 0*	1C
R.X. TEMP MEMORY 3, 2*	1E
R.X. TEMP MEMORY 5, 4*	20
LAST RECEIVED STATUS*	22
HASH REGISTER BYTES 1, 0*	24
HASH REGISTER BYTES 3, 2*	26
HASH REGISTER BYTES 5, 4*	28
HASH REGISTER BYTES 7, 6*	2A
SLOT TIME COUNTER*	2C
WAIT TIME COUNTER*	2E
MICRO MACHINE**	30
REGISTER FILE	.
60 BYTES	6A
MICRO MACHINE LFSR**	6C
MICRO MACHINE**	6E
FLAG ARRAY	.
14 BYTES	7A
QUEUE MEMORY**	7C
CU PORT	.
8 BYTES	82
MICRO MACHINE ALU**	84
RESERVED**	86
M.M. TEMP A ROTATE R**	88
M.M. TEMP A**	8A
T.X. DMA BYTE COUNT**	8C
M.M. INPUT PORT ADDRESS**	8E
T.X. DMA ADDRESS	90
M.M. OUTPUT PORT**	92
R.X. DMA BYTE COUNT**	94
M.M. OUTPUT PORT ADDRESS REGISTER**	96
R. DMA ADDRESS**	98
RESERVED**	9A
BUS THROTTLE TIMERS	9C
DIU CONTROL REGISTER**	9E
RESERVED**	A0
DMA CONTROL REGISTER**	A2
BIU CONTROL REGISTER**	A4
M.M. DISPATCHER REG.**	A6
M.M. STATUS REGISTER**	A8

*The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586.

**These bytes are not user defined, results may vary from Dump command to Dump command.

Figure 34. Dump Area Format—82586 Mode

31	0	
CONFIGURE BYTES 5, 4, 3, 2		00
CONFIGURE BYTES 9, 8, 7, 6		04
CONFIGURE BYTES 13, 12, 11, 10		08
I.A. BYTES 1, 0	X X X X X X X X	0C
I.A. BYTES 5, 2		10
TX CRC BYTES 0, 1	LAST T.X. STATUS	14
RX CRC BYTES 0, 1	TX CRC BYTES 3, 2	18
RX TEMP MEMORY 1, 0	RX CRC BYTES 3, 2	1C
R.X. TEMP MEMORY 5, 2		20
HASH REGISTERS 1, 0	LAST R.X. STATUS	24
HASH REGISTER BYTES 5, 2		28
SLOT TIME COUNTER	HASH REGISTERS 7, 6	2C
RECEIVE FRAME LENGTH	WAIT-TIME COUNTER	30
MICRO MACHINE** REGISTER FILE 128 BYTES		34 . . . B0
MICRO MACHINE LFSR**		B4
MICRO MACHINE** FLAG ARRAY 28 BYTES		B8 . . . D0
M.M. INPUT PORT** 16 BYTES		D4 . E0
MICRO MACHINE ALU**		E4
RESERVED**		E8
M.M. TEMP A ROTATE R.**		EC
M.M. TEMP A**		F0
T.X. DMA BYTE COUNT**		F4
M.M. INPUT PORT ADDRESS REGISTER**		F8
T.X. DMA ADDRESS**		FC
M.M. OUTPUT PORT REGISTER**		100
R.X. DMA BYTE COUNT**		104
M.M. OUTPUT PORT ADDRESS REGISTER**		108
R.X. DMA ADDRESS REGISTER**		10C
RESERVED**		110
BUS THROTTLE TIMERS		114
DIU CONTROL REGISTER**		118
RESERVED**		11C
DMA CONTROL REGISTER**		120
BIU CONTROL REGISTER**		124
M.M. DISPATCHER REG.**		128
M.M. STATUS REGISTER**		12C

The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586.
**These bytes are not user defined, results may vary from Dump command to Dump command.

Figure 35. Dump Area Format—Linear and 32-Bit Segmented Mode

Diagnose

The Diagnose Command triggers an internal self-test procedure that checks internal 82596 hardware, which includes:

- Exponential Backoff Random Number Generator (Linear Feedback Shift Register).
- Exponential Backoff Timeout Counter.
- Slot Time Period Counter.
- Collision Number Counter.
- Exponential Backoff Shift Register.
- Exponential Backoff Mask Logic.
- Timer Trigger Logic.

This procedure checks the operation of the Backoff block, which resides in the serial side and is not easily controlled. The Diagnose command is performed in two phases.

The format of the 82596 Diagnose command is:

82586 and 32-Bit Segmented Modes

31												16	15															0
			ODD WORD												EVEN WORD													
EL	S	I	X	X	X	X	X	X	X	X	X	1	1	1	C	B	OK	0	F	0	0	0	0	0	0	0	0	0	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A15														A0
																				LINK OFFSET								

Linear Mode

31												16	15															0
			ODD WORD												EVEN WORD													
EL	S	I	0	0	0	0	0	0	0	0	0	1	1	1	C	B	OK	0	F	0	0	0	0	0	0	0	0	0	0
A31																				LINK ADDRESS									A0

Figure 36. Diagnose

where:

LINK ADDRESS, EL, B, C, I, S	— As per standard Command Block (see the NOP command for details).
Bits 19–28	— Reserved (0 in the 32-bit Segmented and Linear Modes).
CMD (bits 16–18)	— The Diagnose command. Value: 7h.
OK (bit 13)	— Indicates error free completion.
F (bit 11)	— Indicates that the self-test procedure has failed.

RECEIVE FRAME DESCRIPTOR

Each received frame is described by one Receive Frame Descriptor (see Figure 37). Two new memory structures are available for the received frames. The structures are available only in the Linear and 32-bit Segmented modes.

Simplified Memory Structure

The first is the Simplified memory structure, the data section of the received frame is part of the RFD and is located immediately after the Length Field. Receive Buffer Descriptors are not used with the Simplified structure, it is primarily used to make programming easier. If the length of the data area described in the Size Field is smaller than the incoming frame, the following happens.

1. The received frame is truncated.
2. The No Resource error counter is updated.
3. If the 82596 is configured to Save Bad Frames the RFD is not reused; otherwise, the same RFD is used to hold the next received frame, and the only action taken regarding the truncated frame is to update the counter.
4. The 82596 continues to receive the next frame in the next RFD.

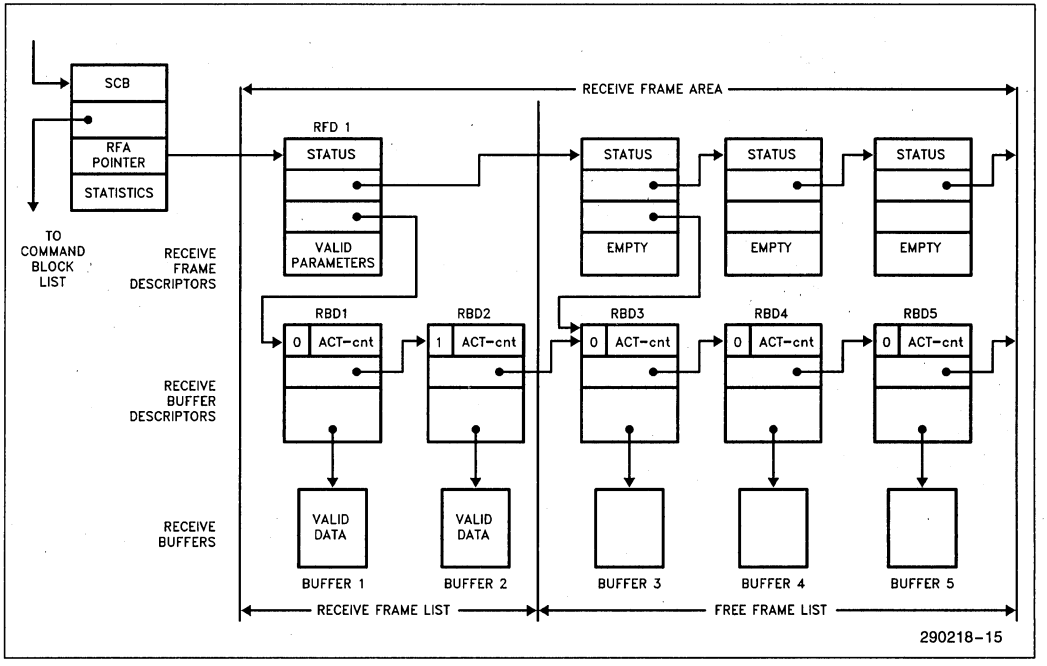


Figure 37. The Receive Frame Area

Note that this sequence is very useful for monitoring. If the 82596 is configured to Save Bad Frames, to receive in Promiscuous mode, and to use the Simplified memory structure, any programmed length of received data can be saved in memory.

The Simplified memory structure is shown in Figure 38.

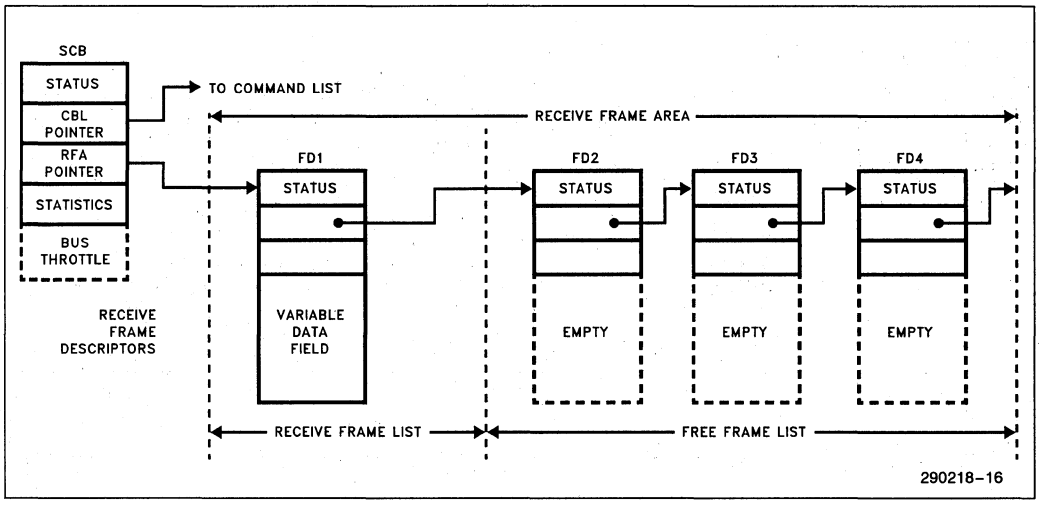


Figure 38. RFA Simplified Memory Structure

Flexible Memory Structure

The second structure is the Flexible memory structure, the data structure of the received frame is stored in both the RFD and in a linked list of Receive Buffers—Receive Buffer Descriptors. The received frame is placed in the RFD as configured in the Size field. Any remaining data is placed in a linked list of RBDs.

The Flexible memory structure is shown in Figure 39.

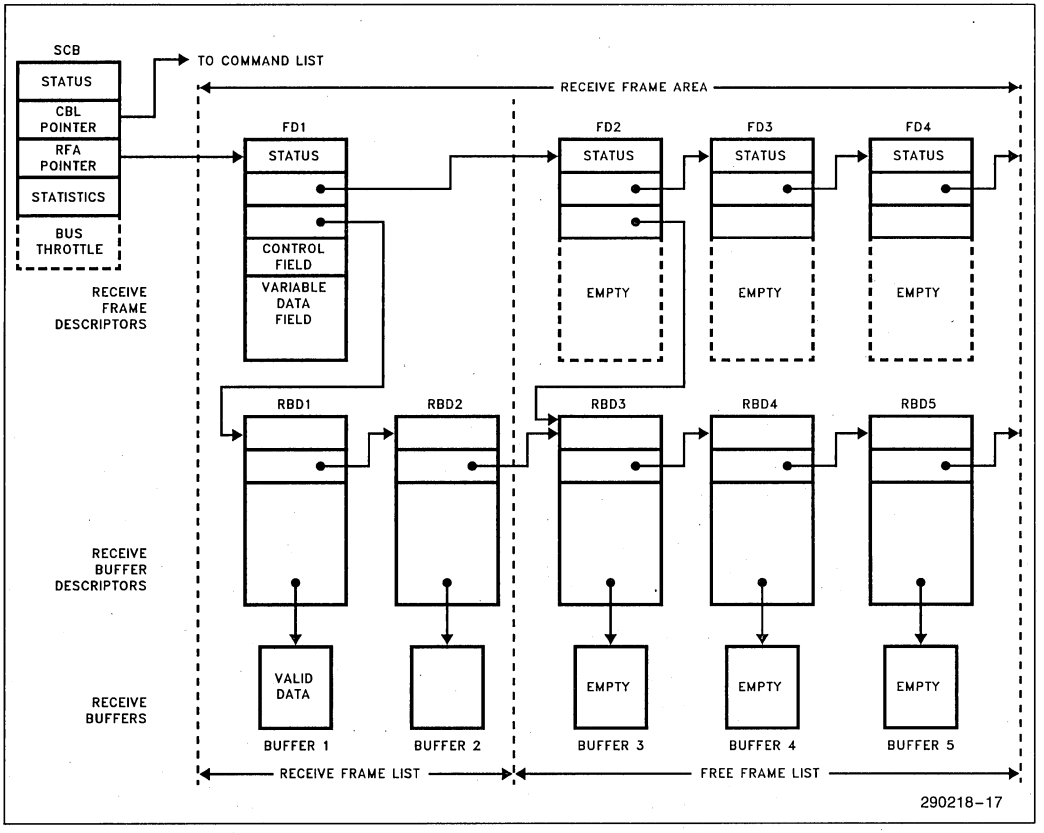


Figure 39. RFA Flexible Memory Structure

Buffers on the receive side can be different lengths. The 82596 will not place more bytes into a buffer than indicated in the associated RBD. The 82596 will fetch the next RBD before it is needed. The 82596 will attempt to receive frames as long as the FBL is not exhausted. If there are no more buffers, the 82596 Receive Unit will enter the No Resources state. Before starting the RU, the CPU must place the FBL pointer in the RBD pointer field of the first RFD. All remaining RBD pointer fields for subsequent RFDs should be "1s." If the Receive Frame Descriptor and the associated Receive Buffers are not reused (e.g., the frame is properly received or the 82596 is configured to Save Bad Frames), the 82596 writes the address of the next free RBD to the RBD pointer field of the next RFD.

Receive Buffer Descriptor (RBD)

The RBDs are used to store received data in a flexible set of linked buffers. The portion of the frame's data field that is outside the RFD is placed in a set of buffers chained by a sequence of RBDs. The RFD points to the first RBD, and the last RBD is flagged with an EOF bit set to 1. Each buffer in the linked list of buffers related to a particular frame can be any size up to 2^{14} bytes but must be word aligned (begin on an even numbered byte). This ensures optimum use of the memory resources while maintaining low overhead. All buffers in a frame are filled with the received data except for the last, in which the actual count can be smaller than the allocated buffer space.

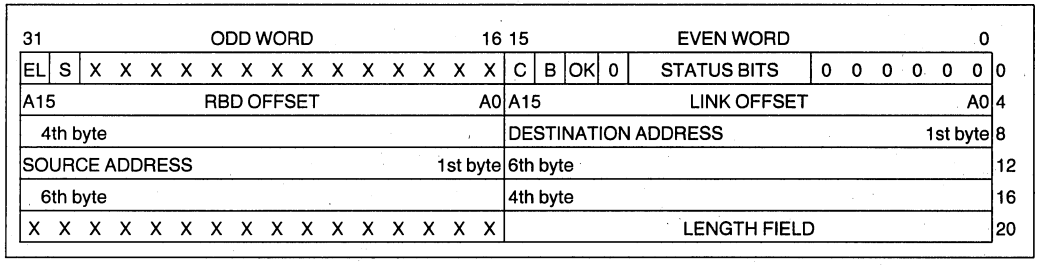


Figure 40. Receive Frame Descriptor—82586 Mode

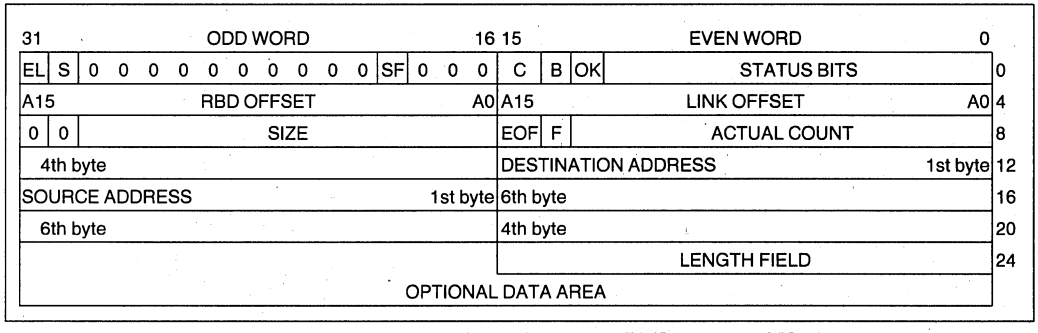


Figure 41. Receive Frame Descriptor—32-Bit Segmented Mode

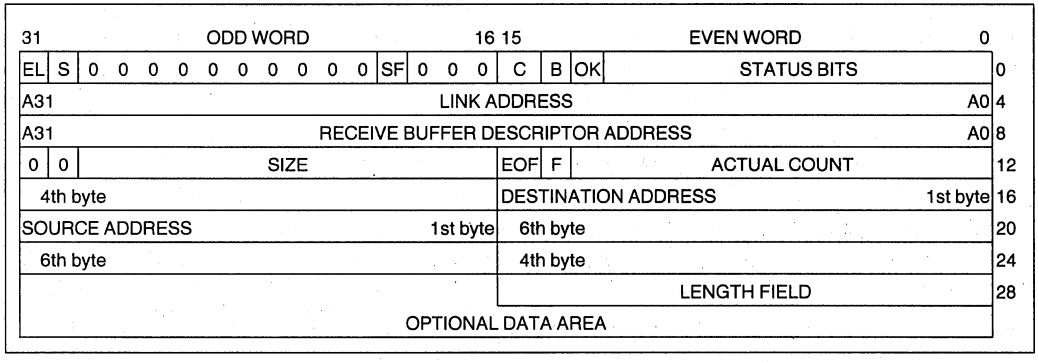


Figure 42. Receive Frame Descriptor—Linear Mode

where:

EL — When set, this bit indicates that this RFD is the last one on the RDL.

S — When set, this bit suspends the RU after receiving the frame.

SF — This bit selects between the Simplified or the Flexible mode.

0 — Simplified mode, all the RX data is in the RFD. RBD ADDRESS field is all "1s."

1 — Flexible mode. Data is in the RFD and in a linked list of Receive Buffer Descriptors.

C — This bit indicates the completion of frame reception. It is set by the 82596.

B — This bit indicates that the 82596 is currently receiving this frame, or that the 82596 is ready to receive the frame. It is initially set to 0 by the CPU. The 82596 sets it to 1 when reception set up begins, and to 0 upon completion. The C and B bits are set during the same operation.

OK (bit 13) — Frame received successfully, without errors. RFDs with bit 13 equal to 0 are possible only if the save bad frames, configuration option is selected. Otherwise all frames with errors will be discarded, although statistics will be collected on them.

STATUS — The results of the Receive operation. Defined bits are,

Bit 12: Length error if configured to check length

Bit 11: CRC error in an aligned frame

Bit 10: Alignment error (CRC error in misaligned frame)

Bit 9: Ran out of buffer space—no resources

Bit 8: DMA Overrun failure to acquire the system bus.

Bit 7: Frame too short.

Bit 6: No EOP flag (for Bit stuffing only)

Bit 5: When the SF bit equals zero, and the 82596 is configured to save bad frames, this bit signals that the receive frame was truncated. Otherwise it is zero.

Bits 2–4: Zeros

Bit 1: When it is zero, the destination address of the received frame matches the IA address. When it is a 1, the destination address of the received frame did not match the individual address. For example, a multicast address or broadcast address will set this bit to a 1.

Bit 0: Receive collision. A collision is detected during reception and the collision occurred after the destination address was received.

LINK ADDRESS — A 16-bit offset (32-bit address in the Linear mode) to the next Receive Frame Descriptor. The Link Address of the last frame can be used to form a cyclical list.

RBD POINTER — The offset (address in the Linear mode) of the first RBD containing the received frame data. An RBD pointer of all ones indicates no RBD.

EOF
F
SIZE
ACT COUNT — These fields are for the Simplified and Flexible memory models. They are exactly the same as the respective fields in the Receive Buffer Descriptor. See the next section for detailed explanation of their functions.

MC — Multicast bit.

DESTINATION ADDRESS — The contents of the destination address of the receive frame. The field is 0 to 6 bytes long.

SOURCE ADDRESS — The contents of the Source Address field of the received frame. It is 0 to 6 bytes long.

LENGTH FIELD — The contents of this 2-byte field are user defined. In 802.3 it contains the length of the data field. It is placed in memory in the same order it is received, i.e., most significant byte first, least significant byte second.

NOTES

1. The Destination address, Source address and Length fields are packed, i.e., one field immediately follows the next.
2. The affect of Address/Length Location (No Source Address Insertion) configuration parameter while receiving is as follows:

— 82586 Mode: The Destination address, Source address and Length field are not used, they are placed in the RX data buffers.

— 32-Bit Segmented and Linear Modes: when the Simplified memory model is used, the Destination address, Source address and Length fields reside in their respective fields in the RFD. When the Flexible memory strucrture is used the Destination address, Source address, and Length field locations depend on the SIZE field of the RFD. They can be placed in the RFD, in the RX data buffers, or partially in the RFD and the rest in the RX data buffers, depending on the SIZE field value.

82586 Mode

31 ODD WORD 16	15 EVEN WORD 0	
A15 NEXT RBD OFFSET A0	EOF F ACTUAL COUNT	0
X X X X X X X X A23 RECEIVE BUFFER ADDRESS A0		4
X X X X X X X X X X X X X X X X	EL X SIZE	8

32-Bit Segmented Mode

31 ODD WORD 16	15 EVEN WORD 0	
A15 NEXT RBD OFFSET A0	EOF F ACTUAL COUNT	0
A31 RECEIVE BUFFER ADDRESS A0		4
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	EL P SIZE	8

Linear Mode

31 ODD WORD 16	15 EVEN WORD 0	
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	EOF F ACTUAL COUNT	0
A31 NEXT RBD ADDRESS A0		4
A31 RECEIVE BUFFER ADDRESS A0		8
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	EL P SIZE	

Figure 43. Receive Buffer Descriptor

where:

EOF — Indicates that this is the last buffer related to the frame. It is cleared by the CPU before starting the RU, and is written by the 82596 at the end of reception of the frame.

F — Indicates that this buffer has already been used. The Actual Count has no meaning unless the F bit equals one. This bit is cleared by the CPU before starting the RU, and is set by the 82596 after the associated buffer has been. This bit has the same meaning as the Complete bit in the RFD and CB.

ACT COUNT — This 14-bit quantity indicates the number of meaningful bytes in the buffer. It is cleared by the CPU before starting the RU, and is written by the 82596 after the associated buffer has already been used. In general, after the buffer is full, the Actual Count value equals the size field of the same buffer. For the last buffer of the frame, Actual Count can be less than the buffer size.

NEXT BD ADDRESS — The offset (absolute address in the Linear mode) of the next RBD on the list. It is meaningless if EL = 1.

BUFFER ADDRESS — The starting address of the memory area that contains the received data. In the 82586 mode, this is a 24-bit address (with pins A24–A31 = 0). In the 32-bit Segmented and Linear modes this is a 32-bit address.

EL — Indicates that the buffer associated with this RBD is last in the FBL.

P — This bit indicates that the 82596 has already prefetched the RBDs and any change in the RBD data will be ignored. This bit is valid only in the new 82596 memory modes, and if this feature has been enabled during configure command. The 82596 Prefetches the RBDs in locked cycles; after prefetching the RBD the 82596 performs a write cycle where the P bit is set to one and the rest of the data remains unchanged. The CPU is responsible for resetting it in all RBDs. The 82596 will not check this bit before setting it.

SIZE — This 14-bit quantity indicates the size, in bytes, of the associated buffer. This quantity must be an even number.

PGA PACKAGE THERMAL SPECIFICATION

Parameter	Thermal Resistance
θ_{JC}	3°C/W
θ_{JA}	24°C/W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

ELECTRICAL AND TIMING CHARACTERISTICS

Absolute Maximum Ratings

- Storage Temperature ..... −65°C to +150°C
- Case Temperature under Bias −65°C to +110°C
- Supply Voltage with Respect to V_{SS} ..... −0.5V to +6.5V
- Voltage on Other Pins .... −0.5V to V_{CC} + 0.5V

DC Characteristics

T_C = 0°C–85°C, V_{CC} = 5V ±10% LE/$\overline{BE}$ have MOS levels (see V_{MIL}, V_{MIH}).
All other signals have TTL levels (see V_{IL}, V_{IH}, V_{OL}, V_{OH}).

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage (TTL)	−0.3	+0.8	V	
V_{IH}	Input High Voltage (TTL)	2.0	V_{CC} + 0.3	V	
V_{MIL}	Input Low Voltage (MOS)	−0.3	+0.8	V	
V_{MIH}	Input High Voltage (MOS)	3.7	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage (TTL)		0.45	V	I_{OL} = 4.0 mA
V_{CIL}	$\overline{RXC}$, $\overline{TXC}$ Input Low Voltage	−0.5	0.6	V	
V_{CIH}	$\overline{RXC}$, $\overline{TXC}$ Input High Voltage	3.3	V_{CC}+0.5	V	
V_{OH}	Output High Voltage (TTL)	2.4		V	I_{OH} = 0.9 mA–1 mA
I_{LI}	Input Leakage Current		±15	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±15	μA	$0.45 < V_{OUT} < V_{CC}$
C_{IN}	Capacitance of Input Buffer		10	pF	FC = 1 MHz
C_{OUT}	Capacitance of Input/Output Buffer		12	pF	FC = 1 MHz
C_{CLK}	CLK Capacitance		20	pF	FC = 1 MHz
I_{CC}	Power Supply		200	mA	At 25 MHz I_{CC} Typical = 100 mA
I_{CC}	Power Supply		300	mA	At 33 MHz I_{CC} Typical = 150 mA

AC Characteristics

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C–+85°C, V_{CC} = 5V ±10%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	16 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	16 MHz	1X CLK Input
T1	CLK Period	62.5	80	
T1a	CLK Period Stability		0.1%	Adjacent CLK Δ
T2	CLK High	20		2.0V
T3	CLK Low	20		0.8V
T4	CLK Rise Time		8	0.8V to 2.0V
T5	CLK Fall Time		8	2.0V to 0.8V
T6	$\overline{BEn}$, $\overline{LOCK}$, and A2–A31 Valid Delay	3	23	
T6a	$\overline{BLAST}$, $\overline{PCHK}$ Valid Delay	3	32	
T7	$\overline{BEn}$, $\overline{LOCK}$, $\overline{BLAST}$, A2–A31 Float Delay	3	39	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	23	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	3	39	
T10	D0–D31, DPn Write Data Valid Delay	3	27	
T11	D0–D31, DPn Write Data Float Delay	3	39	
T12	HOLD Valid Delay	2	30	
T13	CA and BREQ Setup Time	11		1, 2
T14	CA and BREQ Hold Time	6		1, 2
T15	$\overline{BS16}$ Setup Time	12		2
T16	$\overline{BS16}$ Hold Time	5		2
T17	$\overline{BRDY}$, $\overline{RDY}$ Setup Time	12		2
T18	$\overline{BRDY}$, $\overline{RDY}$ Hold Time	5		2
T19	D0–D31, DPn READ Setup Time	10		2
T20	D0–D31, DPn READ Hold Time	6		2
T21	AHOLD and HLDA Setup Time	15		1, 2
T22	AHOLD Hold Time	5		1, 2
T22a	HLDA Hold Time	5		1, 2
T23	RESET Setup Time	14		1, 2
T24	RESET Hold Time	5		1, 2
T25	INT/$\overline{INT}$ Valid Delay	1	23	
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	2 T1		1, 2, 3
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	10		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	6		2
T29	$\overline{PORT}$ Setup Time	11		2
T30	$\overline{PORT}$ Hold Time	5		2
T31	$\overline{BOFF}$ Setup Time	12		2
T32	$\overline{BOFF}$ Hold Time	5		2

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C–+85°C, V_{CC} = 5V ±10%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	20 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	20 MHz	1X CLK Input
T1	CLK Period	50	80	
T1a	CLK Period Stability		0.1%	Adjacent CLK Δ
T2	CLK High	16		2.0V
T3	CLK Low	16		0.8V
T4	CLK Rise Time		6	0.8V to 2.0V
T5	CLK Fall Time		6	2.0V to 0.8V
T6	$\overline{BE}$n, $\overline{LOCK}$, and A2–A31 Valid Delay	3	20	
T6a	$\overline{BLAST}$, $\overline{PCHK}$ Valid Delay	3	25	
T7	$\overline{BE}$n, $\overline{LOCK}$, $\overline{BLAST}$, A2–A31 Float Delay	3	34	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	20	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	3	34	
T10	D0–D31, DPn Write Data Valid Delay	3	23	
T11	D0–D31, DPn Write Data Float Delay	3	34	
T12	HOLD Valid Delay	2	25	
T13	CA and BREQ Setup Time	10		1, 2
T14	CA and BREQ Hold Time	6		1, 2
T15	$\overline{BS16}$ Setup Time	12		2
T16	$\overline{BS16}$ Hold Time	4		2
T17	$\overline{BRDY}$, $\overline{RDY}$ Setup Time	12		2
T18	$\overline{BRDY}$, $\overline{RDY}$ Hold Time	4		2
T19	D0–D31, DPn READ Setup Time	6		2
T20	D0–D31, DPn READ Hold Time	5		2
T21	AHOLD and HLDA Setup Time	15		1, 2
T22	AHOLD Hold Time	4		1, 2
T22a	HLDA Hold Time	5		1, 2
T23	RESET Setup Time	12		1, 2
T24	RESET Hold Time	4		1, 2
T25	INT/$\overline{INT}$ Valid Delay	1	23	
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	2 T1		1, 2, 3
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	6		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	5		2
T29	$\overline{PORT}$ Setup Time	10		2
T30	$\overline{PORT}$ Hold Time	5		2
T31	$\overline{BOFF}$ Setup Time	12		2
T32	$\overline{BOFF}$ Hold Time	4		2

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C–+85°C, V_{CC} = 5V ±10%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	25 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	25 MHz	1X CLK Input
T1	CLK Period	40	80	
T1a	CLK Period Stability		0.1%	Adjacent CLK Δ
T2	CLK High	14		2.0V
T3	CLK Low	14		0.8V
T4	CLK Rise Time		4	0.8V to 2.0V
T5	CLK Fall Time		4	2.0V to 0.8V
T6	$\overline{BEn}$ Valid Delay	3	17	
T6a	$\overline{BLAST}$ Valid Delay	3	20	
T6b	$\overline{LOCK}$ Valid Delay	3	18	
T6c	A2–A31 Valid Delay	3	18	
T6d	$\overline{PCHK}$ Valid Delay	3	24	
T7	$\overline{BEn}$, $\overline{LOCK}$, $\overline{BLAST}$, A2–A31 Float Delay	3	30	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	19	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	3	30	
T10	D0–D31, DPn Write Data Valid Delay	3	20	
T11	D0–D31, DPn Write Data Float Delay	3	30	
T12	HOLD Valid Delay	3	19	
T13	CA and BREQ Setup Time	7		1, 2
T14	CA and BREQ Hold Time	3		1, 2
T15	$\overline{BS16}$ Setup Time	8		2
T16	$\overline{BS16}$ Hold Time	3		2
T17	$\overline{BRDY}$ Setup Time	9		2
T17a	$\overline{RDY}$ Setup Time	8		2
T18	$\overline{BRDY}$, $\overline{RDY}$ Hold Time	3		2
T19	D0–D31, DPn READ Setup Time	6		2
T20	D0–D31, DPn READ Hold Time	4.5		2
T21	AHOLD and HLDA Setup Time	10		1, 2
T22	AHOLD Hold Time	3		1, 2
T22a	HLDA Hold Time	3		1, 2
T23	RESET Setup Time	10		1, 2
T24	RESET Hold Time	3		1, 2
T25	INT/$\overline{INT}$ Valid Delay	1	20	

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C–+85°C, V_{CC} = 5V ±10%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	25 MHz		Notes
		Min	Max	
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	2 T1		1, 2, 3
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	6		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	4.5		2
T29	$\overline{PORT}$ Setup Time	7		2
T30	$\overline{PORT}$ Hold Time	3		2
T31	$\overline{BOFF}$ Setup Time	10		2
T32	$\overline{BOFF}$ Hold Time	3		2

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C to +85°C, V_{CC} = 5V ±5%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	33 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	33 MHz	1X CLK Input
T1	CLK Period	30	80	
T1a	CLK Period Stability		0.1%	Adjacent CLK Δ
T2	CLK High	11		2.0V
T3	CLK Low	11		0.8V
T4	CLK Rise Time		3	0.8V to 2.0V
T5	CLK Fall Time		3	2.0V to 0.8V
T6	$\overline{BEn}$ Valid Delay	3	17	
T6a	$\overline{BLAST}$ Valid Delay	3	20	
T6b	$\overline{LOCK}$ Valid Delay	3	16	
T6c	A2–A31 Valid Delay	3	18	
T6d	$\overline{PCHK}$ Valid Delay	3	23	
T7	$\overline{BEn}$, $\overline{LOCK}$, $\overline{BLAST}$, A2–A31 Float Delay	3	20	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	16	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	3	20	
T10	D0–D31, DPn Write Data Valid Delay	3	19	
T11	D0–D31, DPn Write Data Float Delay	3	20	
T12	HOLD Valid Delay	3	19	
T13	CA and BREQ Setup Time	7		1, 2
T14	CA and BREQ Hold Time	3		1, 2
T15	$\overline{BS16}$ Setup Time	7		2
T16	$\overline{BS16}$ Hold Time	3		2
T17	$\overline{BRDY}$ Setup Time	9		2
T17a	$\overline{RDY}$ Setup Time	8		2
T18	$\overline{BRDY}$, $\overline{RDY}$ Hold Time	3		2
T19	D0–D31, DPn READ Setup Time	6		2
T20	D0–D31, DPn READ Hold Time	4.5		2
T21	AHOLD Setup Time	10		1, 2
T21a	HLDA Setup Time	8		1, 2
T22	AHOLD Hold Time	3		1, 2

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

C_L on all outputs is 50 pF unless otherwise specified.
All timing requirements are given in nanoseconds.

Symbol	Parameter	33 MHz		Notes
		Min	Max	
T22a	HLDA Hold Time	3		1, 2
T23	RESET Setup Time	9		1, 2
T24	RESET Hold Time	3		1, 2
T25	INT/$\overline{\text{INT}}$ Valid Delay	1	20	
T26	CA and BREQ, $\overline{\text{PORT}}$ Pulse Width	2T1		1, 2, 3
T27	D0–D31 CPU $\overline{\text{PORT}}$ Access Setup Time	6		2
T28	D0–D31 CPU $\overline{\text{PORT}}$ Access Hold Time	4.5		2
T29	$\overline{\text{PORT}}$ Setup Time	7		2
T30	$\overline{\text{PORT}}$ Hold Time	3		2
T31	$\overline{\text{BOFF}}$ Setup Time	10		2
T32	$\overline{\text{BOFF}}$ Hold Time	3		2

NOTES:
*Timings shown are for the 82596CA C-stepping. For information regarding timings for the 82596CA A1 or B-step, contact your local Intel representative.
1. RESET, HLDA, and CA are internally synchronized. This timing is to guarantee recognition at next clock for RESET, HLDA and CA.
2. All set-up, hold and delay timings are at maximum frequency specification Fmax, and must be derated according to the following equation for operation at lower frequencies:
   Tderated = (Fmax/Fopr) × T
   where:
   Tderate = Specifies the value to derate the specification.
   Fmax = Maximum operating frequency.
   Fopr = Actual operating frequency.
   T = Specification at maximum frequency.
   This calculation only provides a rough estimate for derating the frequency. For more detailed information, contact your Intel Sales Office for the data sheet supplement.
3. CA pulse width need only be 1 T1 wide if the set up and hold times are met; BREQ must meet setup and hold times and need only be 1 T1 wide.

TRANSMIT/RECEIVE CLOCK PARAMETERS

Symbol	Parameter	20 MHz		Notes
		Min	Max	
T36	$\overline{\text{TxC}}$ Cycle	50		1, 3
T38	$\overline{\text{TxC}}$ Rise Time		5	1
T39	$\overline{\text{TxC}}$ Fall Time		5	1
T40	$\overline{\text{TxC}}$ High Time	19		1, 3
T41	$\overline{\text{TxC}}$ Low Time	18		1, 3
T42	TxD Rise Time		10	4
T43	TxD Fall Time		10	4
T44	TxD Transition	20		2, 4
T45	$\overline{\text{TxC}}$ Low to TxD Valid		25	4, 6
T46	$\overline{\text{TxC}}$ Low to TxD Transition		25	2, 4
T47	$\overline{\text{TxC}}$ High to TxD Transition		25	2, 4
T48	$\overline{\text{TxC}}$ Low to TxD High (At End of Transition)		25	4

TRANSMIT/RECEIVE CLOCK PARAMETERS (Continued)

Symbol	Parameter	20 MHz		Notes
		Min	Max	
$\overline{\text{RTS}}$ AND $\overline{\text{CTS}}$ PARAMETERS				
T49	$\overline{\text{TxC}}$ Low to $\overline{\text{RTS}}$ Low, Time to Activate $\overline{\text{RTS}}$		25	5
T50	$\overline{\text{CTS}}$ Low to $\overline{\text{TxC}}$ Low, $\overline{\text{CTS}}$ Setup Time		20	
T51	$\overline{\text{TxC}}$ Low to $\overline{\text{CTS}}$ Invalid, $\overline{\text{CTS}}$ Hold Time	10		7
T52	$\overline{\text{TxC}}$ Low to $\overline{\text{RTS}}$ High		25	5
RECEIVE CLOCK PARAMETERS				
T53	$\overline{\text{RXC}}$ Cycle	50		1, 3
T54	$\overline{\text{RXC}}$ Rise Time		5	1
T55	$\overline{\text{RXC}}$ Fall Time		5	1
T56	$\overline{\text{RXC}}$ High Time	19		1
T57	$\overline{\text{RXC}}$ Low Time	18		1
RECEIVED DATA PARAMETERS				
T58	RXD Setup Time	20		6
T59	RXD Hold Time	10		6
T60	RXD Rise Time		10	
T61	RXD Fall Time		10	
$\overline{\text{CRS}}$ AND $\overline{\text{CDT}}$ PARAMETERS				
T62	$\overline{\text{CDT}}$ Low to $\overline{\text{TXC}}$ HIGH External Collision Detect Setup Time	20		
T63	$\overline{\text{TXC}}$ High to $\overline{\text{CDT}}$ Inactive, $\overline{\text{CDT}}$ Hold Time	10		
T64	$\overline{\text{CDT}}$ Low to Jam Start			10
T65	$\overline{\text{CRS}}$ Low to $\overline{\text{TXC}}$ High, Carrier Sense Setup Time	20		
T66	$\overline{\text{TXC}}$ High to $\overline{\text{CRS}}$ Inactive, $\overline{\text{CRS}}$ Hold Time (Internal Collision Detect)	10		
T67	$\overline{\text{CRS}}$ High to Jamming Start,			12
T68	Jamming Period			11
T69	$\overline{\text{CRS}}$ High to $\overline{\text{RXC}}$ High, $\overline{\text{CRS}}$ Inactive Setup Time	30		
T70	$\overline{\text{RXC}}$ High to $\overline{\text{CRS}}$ High, $\overline{\text{CRS}}$ Inactive Hold Time	10		

TRANSMIT/RECEIVE CLOCK PARAMETERS (Continued)

Symbol	Parameter	20 MHz		Notes
		Min	Max	
INTERFRAME SPACING PARAMETERS				
T71	Interframe Delay			9
EXTERNAL LOOPBACK-PIN PARAMETERS				
T72	$\overline{TXC}$ Low to $\overline{LPBK}$ Low		T36	4
T73	$\overline{TXC}$ Low to $\overline{LPBK}$ High		T36	4

NOTES:
1. Special MOS levels. V_{CIL} = 0.9V and V_{CIH} = 3.0V.
2. Manchester only.
3. Manchester. Needs 50% duty cycle.
4. 1 TTL load + 50 pF.
5. 1 TTL load + 100 pF.
6. NRZ only.
7. Abnormal end of transmission—CTS expires before RTS.
8. Normal end to transmission.
9. Programmable value:
   T71 = N_{IFS} • T36
   where: N_{IFS} = the IFS configuration value
   (if N_{IFS} is less than 12 then N_{IFS} is forced to 12).
10. Programmable value:
    T64 = (N_{CDF} • T36) + x • T36
    (If the collision occurs after the preamble)
    where:
    N_{CDF} = the collision detect filter configuration value, and
    x = 12, 13, 14, or 15
11. T68 = 32 • T36
12. Programmable value:
    T67 = (N_{CSF} • T36) + x • T36
    where: N_{CSF} = the Carrier Sense Filter configuration value, and
    x = 12, 13, 14, or 15
13. To guarantee recognition on the next clock.

82596CA BUS OPERATION

The following figures show the 82596CA basic bus cycle and basic burst cycle.

Please refer to the *32-Bit LAN Component User's Manual.*

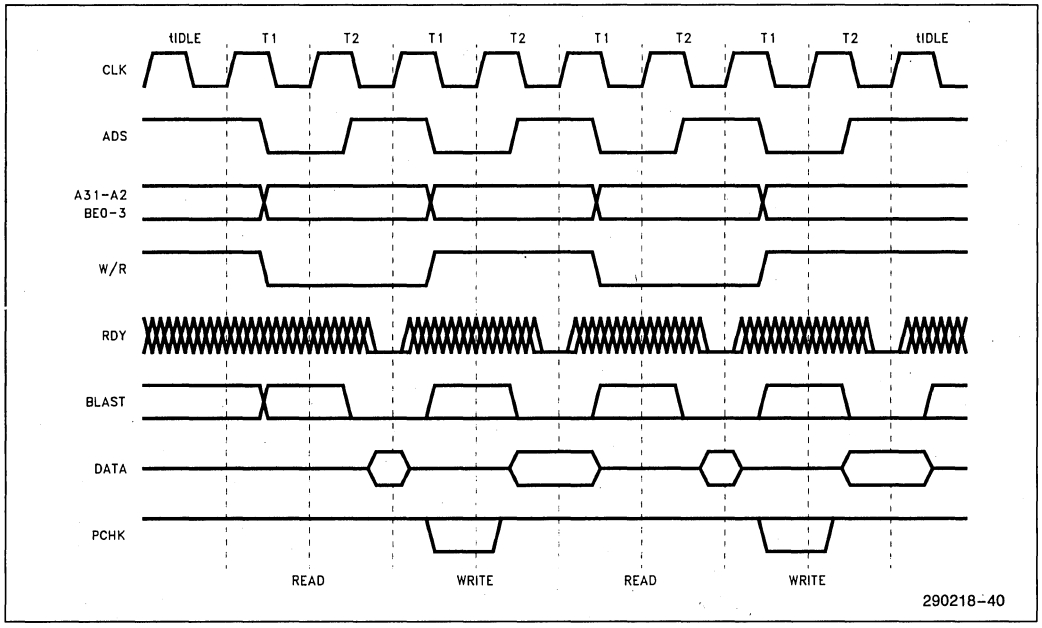


Figure 44. Basic 82596CA Bus Cycle

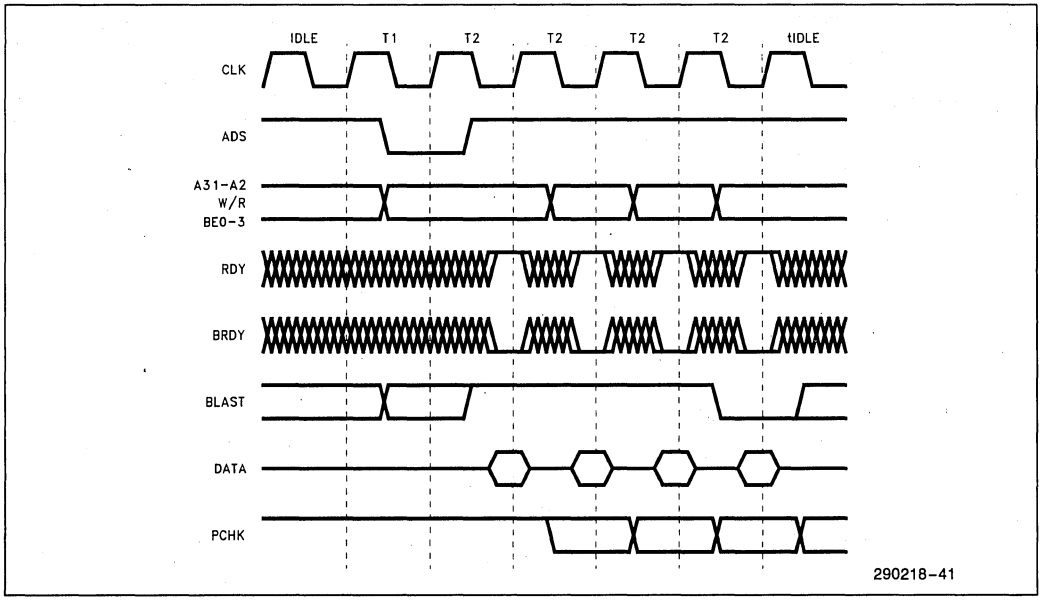


Figure 45. Basic 82596CA Burst Cycle

SYSTEM INTERFACE A.C. TIMING CHARACTERISTICS

The measurements should be done at:

- T_C = 0°C to +85°C, V_{CC} = 5V ±10%, C = 50 pF unless otherwise specified.
- A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
- Timing measurements are made at 1.5V for both logic "1" and "0".
- Rise and Fall time of inputs and outputs signals are measured between 0.8V and 2.0V respectively unless otherwise specified.
- All timings are relative to CLK crossing the 1.5V level.
- All A.C. parameters are valid only after 100 μs from power up.

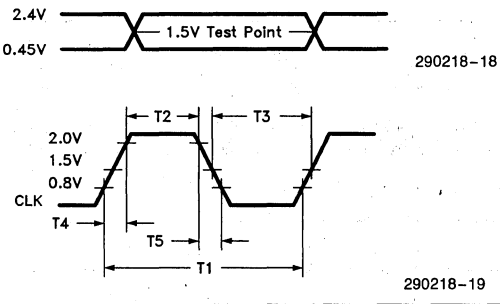
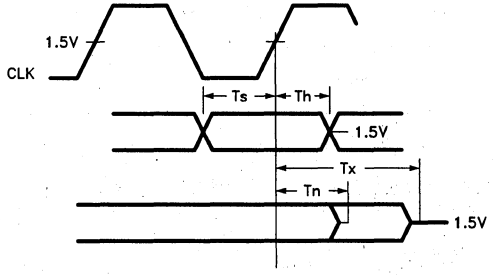


Figure 46. CLK Timings

Two types of timing specifications are presented below:

1. Input Timing—minimum setup and hold times.
2. Output Timings—output delays and float times from CLK rising edge.

Figure 47 defines how the measurements should be done:



LEGEND:
Ts = Input Setup Time
Th = Input Hold Time
Tn = Minimum output delay or Mininum float delay
Tx = Maximum output delay or Maximum float delay

Figure 47. Drive Levels and Measurements Points for A.C. Specifications

Ts = T13, T15, T17, T19, T21, T23, T27, T29, T31
Th = T14, T16, T18, T20, T22, T22a, T24, T28, T30, T32
Tn = T6, T6a, T7, T8, T9, T10, T11, T12, T25
Tx = T6, T6a, T7, T8, T9, T10, T11, T12, T25

INPUT WAVEFORMS

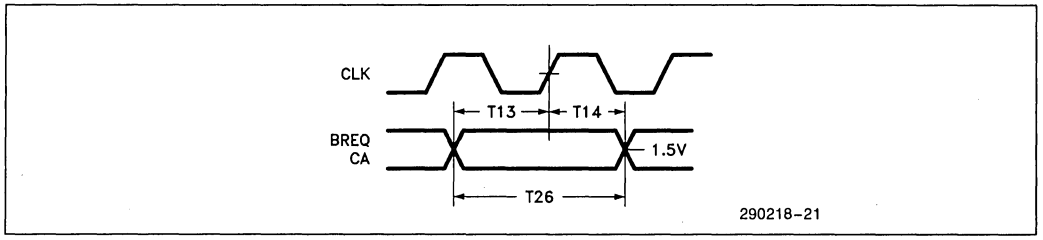


Figure 48. CA and BREQ Input Timing

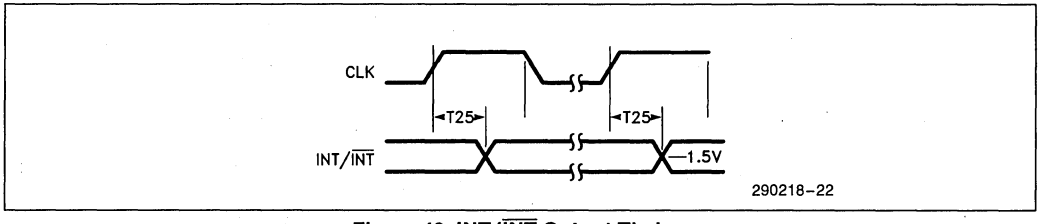


Figure 49. INT/$\overline{INT}$ Output Timing

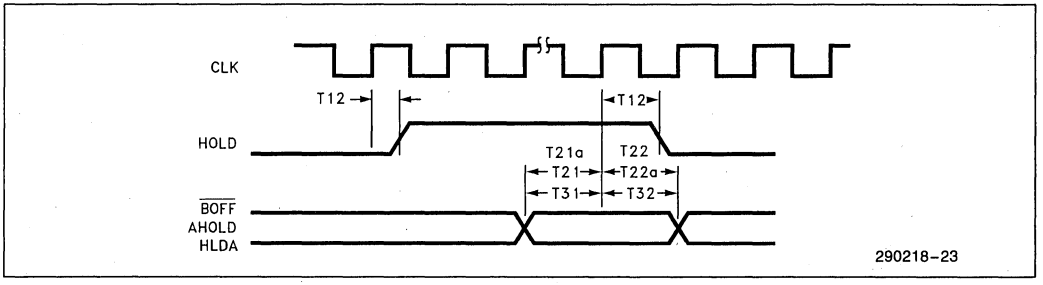


Figure 50. HOLD/HLDA Timings

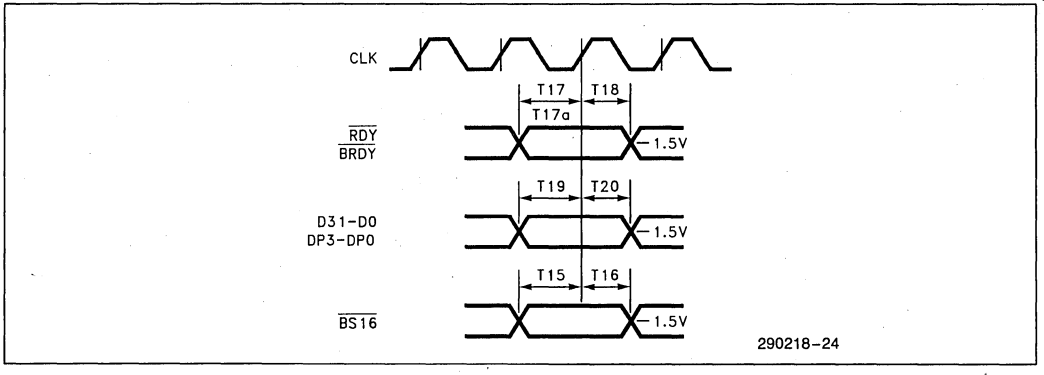


Figure 51. Input Setup and Hold Time

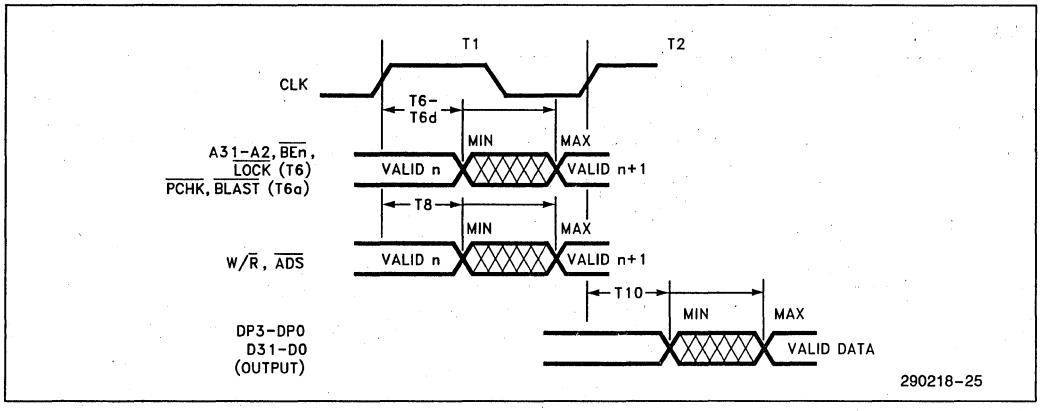


Figure 52. Output Valid Delay Timing

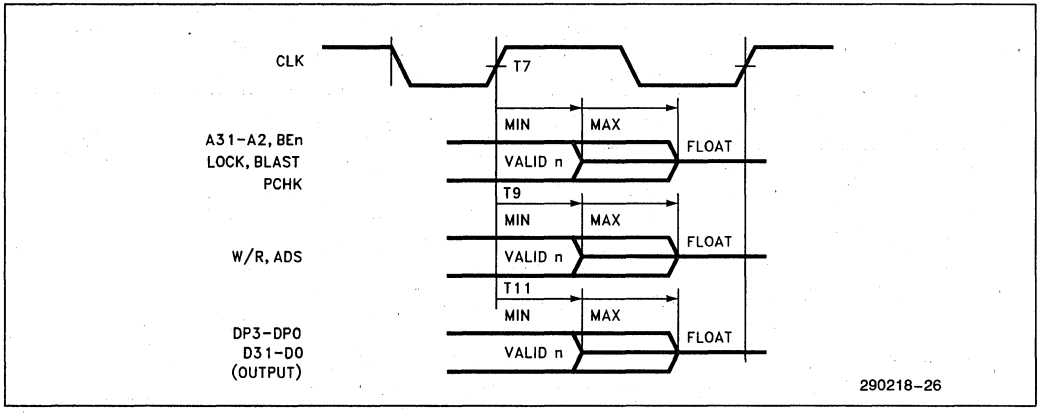


Figure 53. Output Float Delay Timing

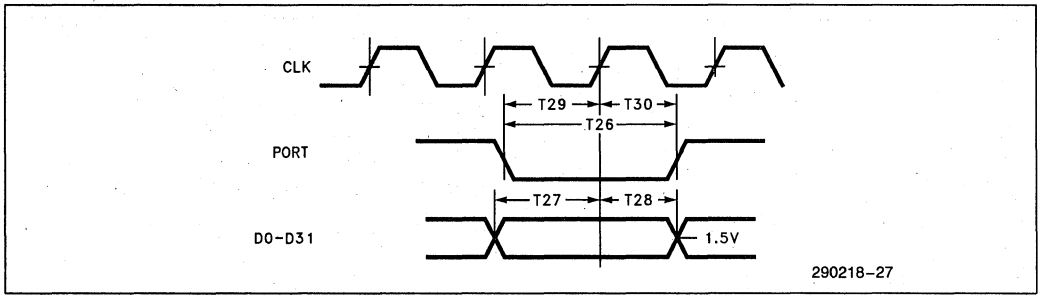


Figure 54. $\overline{\text{PORT}}$ Setup and Hold Time

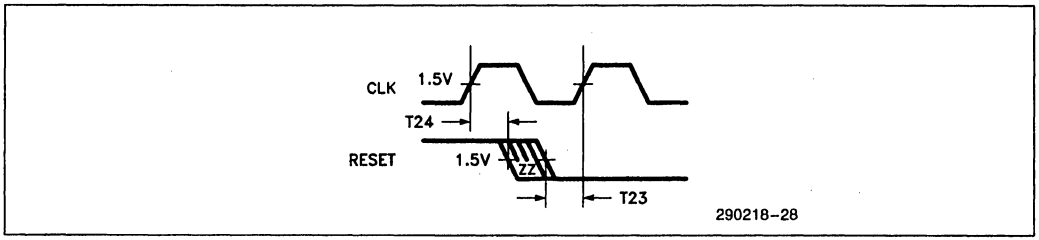


Figure 55. RESET Input Timing

SERIAL AC TIMING CHARACTERISTICS

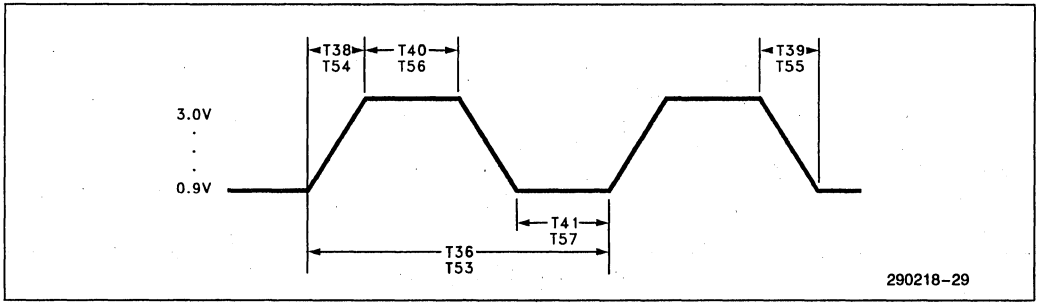


Figure 56. Serial Input Clock Timing

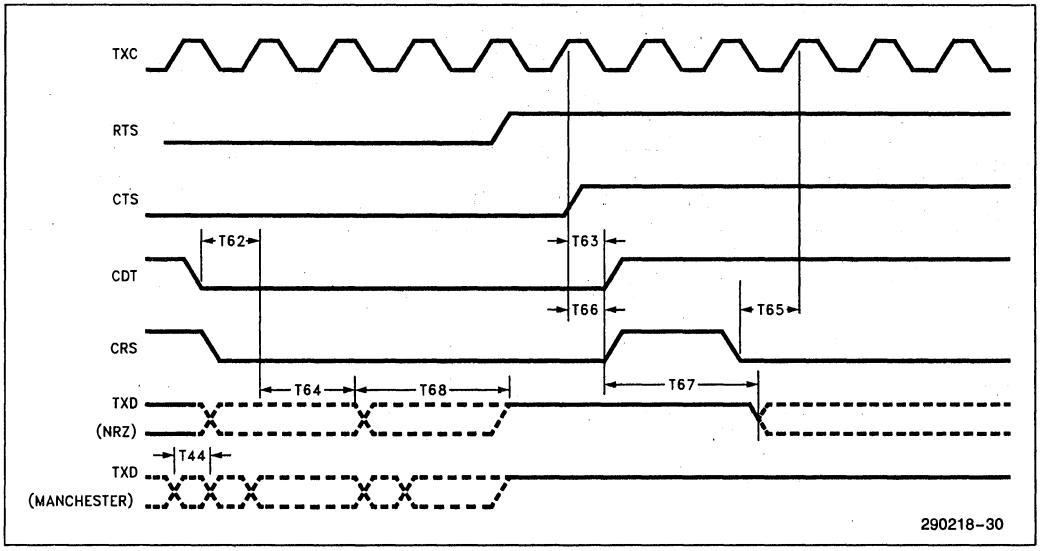


Figure 57. Transmit Data Waveforms

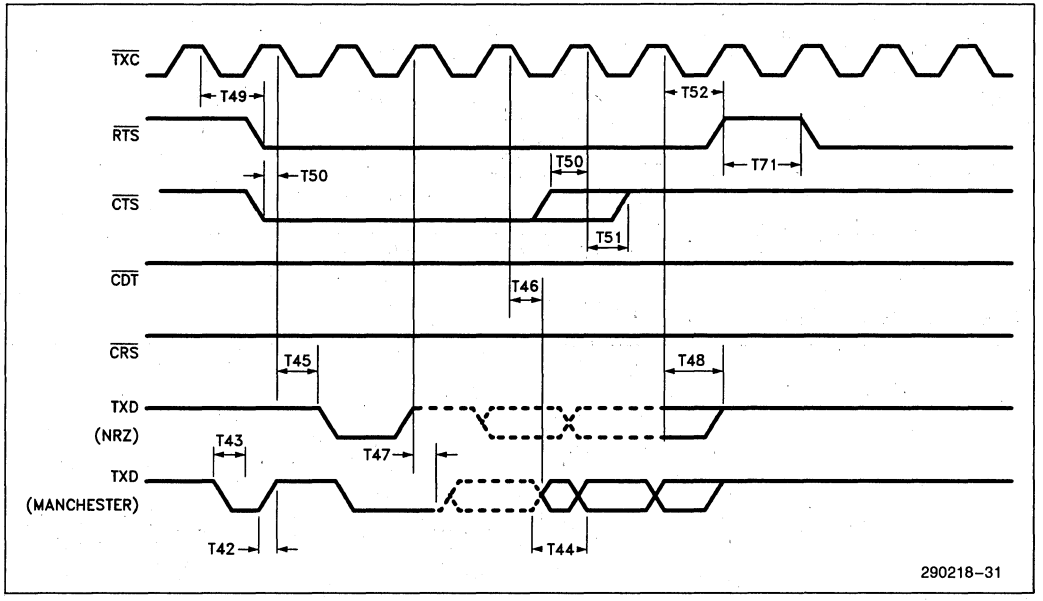


Figure 58. Transmit Data Waveforms

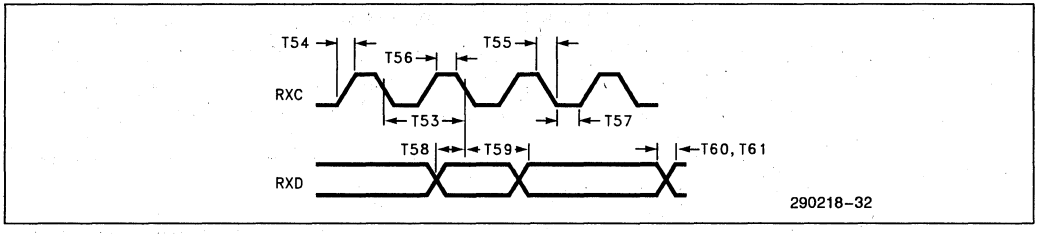


Figure 59. Receive Data Waveforms (NRZ)

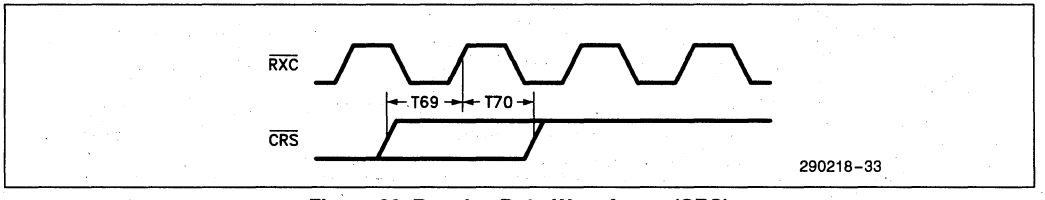
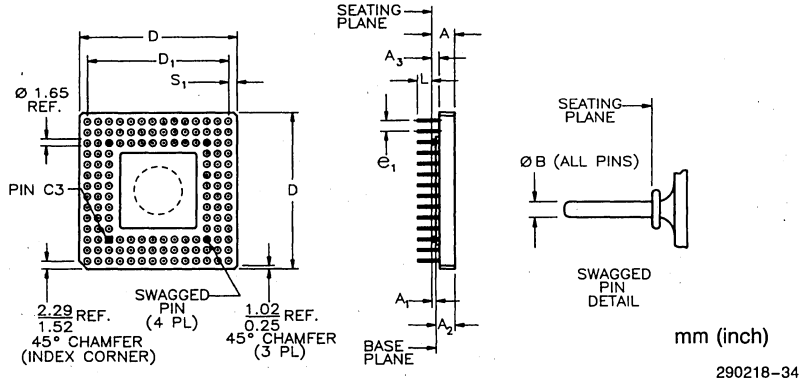


Figure 60. Receive Data Waveforms (CRS)

OUTLINE DIAGRAMS

132 LEAD CERAMIC PIN GRID ARRAY PACKAGE INTEL TYPE A



Family: Ceramic Pin Grid Array Package						
Symbol	**Millimeters**			**Inches**		
	Min	**Max**	**Notes**	**Min**	**Max**	**Notes**
A	3.56	4.57		0.140	0.180	
A_1	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A_2	2.67	3.43	Solid Lid	0.105	0.135	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	36.45	37.21		1.435	1.465	
D_1	32.89	33.15		1.295	1.305	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	132			132		
S_1	1.27	2.54		0.050	0.100	
ISSUE	IWS 10/12/88					

Intel Case Outline Drawings
Plastic Quad Flat Pack (PQFP)
0.025 Inch (0.635mm) Pitch

Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170
A1	Standoff	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
D, E	Terminal Dimension	0.675	0.685	0.775	0.785	0.875	0.885	1.075	1.085	1.275	1.285	1.475	1.485
D1, E1	Package Body	0.547	0.553	0.647	0.653	0.747	0.753	0.947	0.953	1.147	1.153	1.347	1.353
D2, E2	Bumper Distance	0.697	0.703	0.797	0.803	0.897	0.903	1.097	1.103	1.297	1.303	1.497	1.503
D3, E3	Lead Dimension	0.400 REF		0.500 REF		0.600 REF		0.800 REF		1.000 REF		1.200 REF	
D4, E4	Foot Radius Location	0.623	0.637	0.723	0.737	0.823	0.837	1.023	1.037	1.223	1.237	1.423	1.437
L1	Foot Length	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
Issue	IWS Preliminary 12/12/88												INCH

Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32
A1	Standoff	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
D, E	Terminal Dimension	17.15	17.40	19.69	19.94	22.23	22.48	27.31	27.56	32.39	32.64	37.47	37.72
D1, E1	Package Body	13.89	14.05	16.43	16.59	18.97	19.13	24.05	24.21	29.13	29.29	34.21	34.37
D2, E2	Bumper Distance	17.70	17.85	20.24	20.39	22.78	22.93	27.86	28.01	32.94	33.09	38.02	38.18
D3, E3	Lead Dimension	10.16 REF		12.70 REF		15.24 REF		20.32 REF		25.40 REF		30.48 REF	
D4, E4	Foot Radius Location	15.82	16.17	18.36	18.71	21.25	21.25	25.89	26.33	31.06	31.41	36.14	36.49
L1	Foot Length	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
Issue	IWS Preliminary 12/12/88												mm

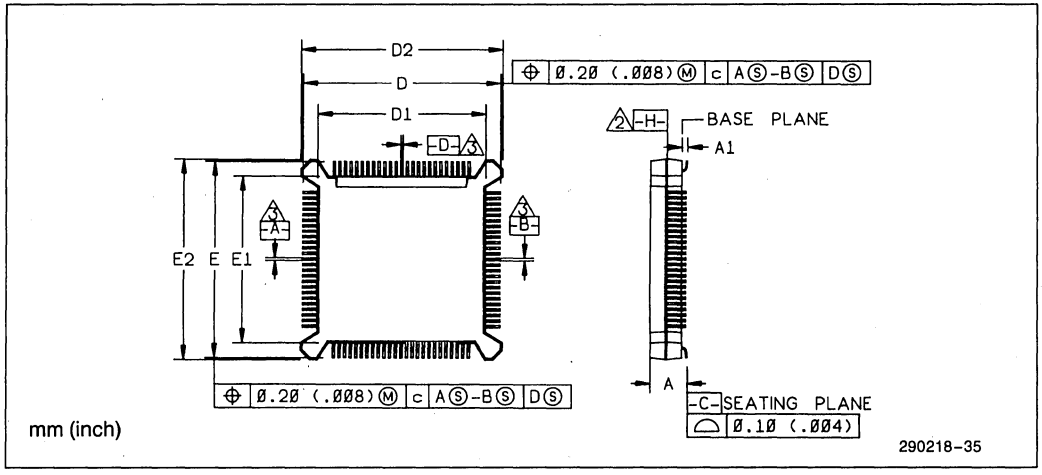


Figure 61. Principal Dimensions and Datums

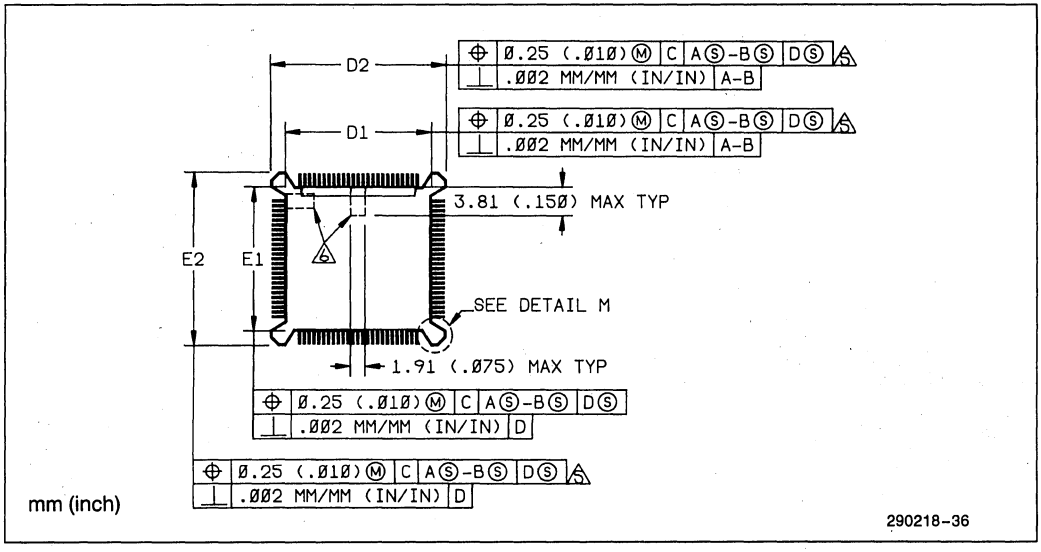


Figure 62. Molded Details

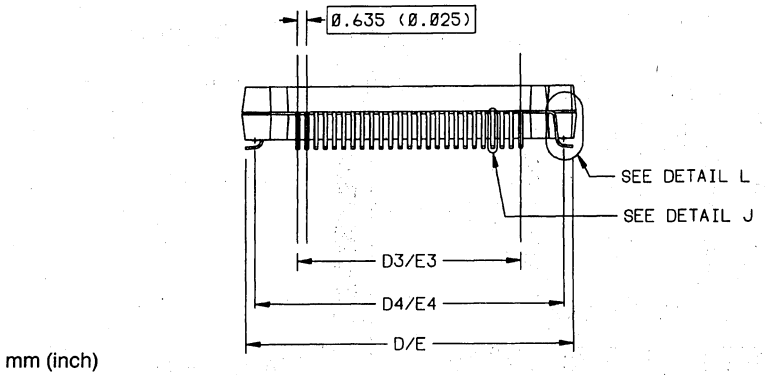


Figure 63. Terminal Details

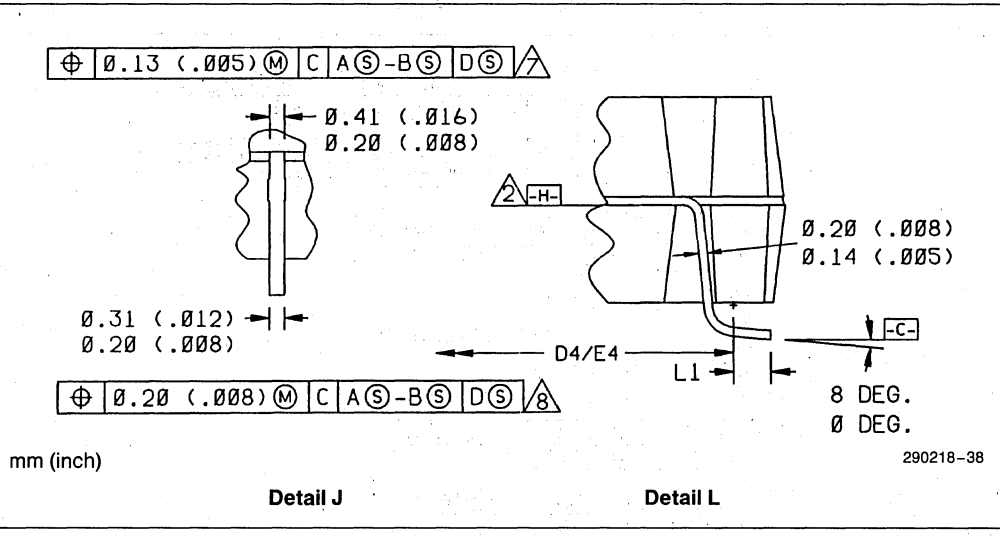
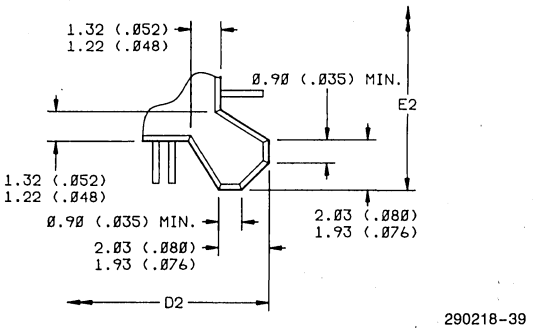


Figure 64. Typical Lead



mm (inch)

Figure 65. Detail M

REVISION SUMMARY

The following represents the key differences between version 004 and version 005 of the 82596CA Data Sheet.

1. Timings added for -16 MHz and -20 MHz specfications.

The following represents the key differences between version 005 and version 006 of the 82596CA Data Sheet.

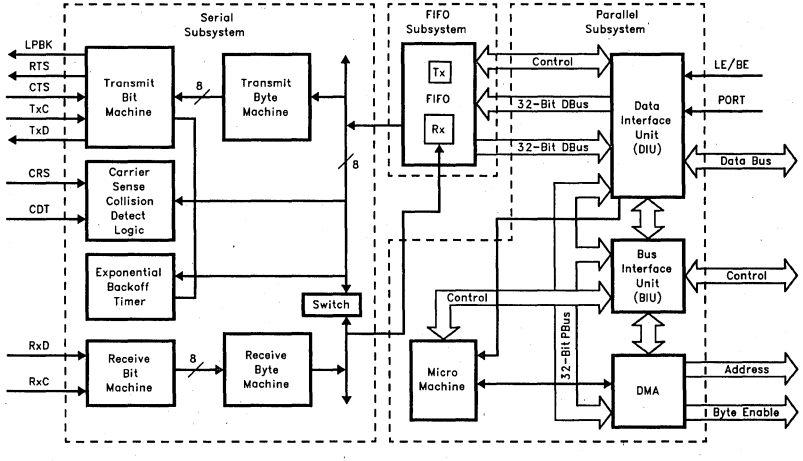
1. A description of the 82596CA C-stepping enhancements was added and the 82596CA B-step information was removed.
2. Description of BOFF pin changed. BOFF may be asserted in T1 in the 82596 C-step.
3. Recommendation to use only one type of buffer (either Simplified or Flexible) in any given linked list.
4. Added detailed description regarding operation or RCVCDT counter.
5. Added New Enhanced Big Endian Mode section. The New Enhanced Big Endian Mode applies only to the 82596 C-stepping.
6. Added programming recommendations regarding RU and CU Start commands. These warn against Starting the CU while it is Active and Starting the RU while it is Ready.
7. Emphasized that the TDR command is a static command and should not be used in an active network.
8. Improved 82596CA C-step timings were added for all speeds.

82596DX AND 82596SX HIGH-PERFORMANCE 32-BIT LOCAL AREA NETWORK COPROCESSOR

- **Performs Complete CSMA/CD Medium Access Control (MAC) Functions—Independently of CPU**
  - **— IEEE 802.3 (EOC) Frame Delimiting**
- **Supports Industry Standard LANs**
  - **— IEEE TYPE 10BASE-T (TPE), IEEE TYPE 10BASE5 (Ethernet*), IEEE TYPE 10BASE2 (Cheapernet), IEEE TYPE 1BASE5 (StarLAN), and the Proposed Standard TYPE 10BASE-F**
  - **— Proprietary CSMA/CD Networks Up to 20 Mb/s**
- **On-Chip Memory Management**
  - **— Automatic Buffer Chaining**
  - **— Buffer Reclamation after Receipt of Bad Frames; Optional Save Bad Frames**
  - **— 32-Bit Segmented or Linear (Flat) Memory Addressing Formats**
- **82586 Software Compatible**
- **Optimized CPU Interface**
  - **— 82596DX Bus Interface Optimized to Intel's 32-Bit i386™DX**
  - **— 82596SX Bus Interface Optimized to Intel's 16-Bit i386™SX**
  - **— Supports Big Endian and Little Endian Byte Ordering**
- **High-Performance 16-/32-Bit Bus Master Interface**
  - **— 66-MB/s Bus Bandwidth**
  - **— 33-MHz Clock, Two Clocks Per Transfer**
  - **— Bus Throttle Timers**
  - **— Transfers Data at 100% of Serial Bandwidth**
  - **— 128-Byte Receive FIFO, 64-Byte Transmit FIFO**
- **Network Management and Diagnostics**
  - **— Monitor Mode**
  - **— 32-Bit Statistical Counters**
- **Self-Test Diagnostics**
- **Configurable Initialization Root for Data Structures**
- **High-Speed, 5-V, CHMOS** IV Technology**
- **132-Pin Plastic Quad Flat Pack (PQFP) and PGA Package**

  (See Packaging Specifications Order Number: 240800-001, Package Type KU and A)

i386™ is a trademark of Intel Corporation
*Ethernet is a registered trademark of Xerox Corporation.
**CHMOS is a patented process of Intel Corporation.



290219-1

Figure 1. 82596DX/SX Block Diagram

October 1995
Order Number: 290219-006

82596DX and 82596SX High-Performance 32-Bit Local Area Network Coprocessor

CONTENTS

CONTENTS

INTRODUCTION

The 82596DX/SX is an intelligent, high-performance 32-bit Local Area Network coprocessor. The 82596DX/SX implements the CSMA/CD access method and can be configured to support all existing IEEE 802.3 standards—TYPEs 10BASE-T, 10BASE5, 10BASE2, 1BASE5, and 10BROAD36. It can also be used to implement the proposed standard TYPE 10BASE-F. The 82596DX/SX performs high-level commands, command chaining, and interprocessor communications via shared memory, thus relieving the host CPU of many tasks associated with network control. All time-critical functions are performed independently of the CPU, this increases network performance and efficiency. The 82596DX/SX bus interface is optimized for Intel's i386™ DX and i386™ SX microprocessors.

The 82596DX/SX implements all IEEE 802.3 Medium Access Control and channel interface functions, these include framing, preamble generation and stripping, source address generation, destination address checking, short-frame detection, and automatic length-field handling. Data rates up to 20 Mb/s are supported.

The 82596DX/SX provides a powerful host system interface. It manages memory structures automatically, with command chaining and bidirectional data chaining. An on-chip DMA controller manages four channels, this allows autonomous transfer of data blocks (buffers and frames) and relieves the CPU of byte transfer overhead. Buffers containing errored or collided frames can be automatically recovered without CPU intervention. The 82596DX/SX provides an upgrade path for existing 82586 software drivers by providing an 82586-software-compatible mode that supports the current 82586 memory structure. The 82596DX/SX also has a Flexible memory structure and a Simplified memory structure. The 82596DX/SX can address up to 4 gigabytes of memory. The 82596DX/SX supports Little Endian and Big Endian byte ordering.

The 82596DX/SX bus interface is optimized to Intel's i386™ DX and i386 SX microprocessors, providing a bus transfer rate of up to 66 MB/s at 33 MHz. The bus interface employs bus throttle timers to regulate 82596DX/SX bus use. Two large, independent FIFOs—128 bytes for Receive and 64 bytes for Transmit—tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case bus latency.

The 82596DX/SX provides a wide range of diagnostics and network management functions, these include internal and external loopback, exception condition tallies, channel activity indicators, optional capture of all frames regardless of destination address (promiscuous mode), optional capture of errored or collided frames, and time domain reflectometry for locating fault points on the network cable. The statistical counters, in 32-bit segmented and linear modes, are 32-bits each and include CRC errors, alignment errors, overrun errors, resource errors, short frames, and received collisions. The 82596DX/SX also features a monitor mode for network analysis. In this mode the 82596DX/SX can capture status bytes, and update statistical counters, of frames monitored on the link without transferring the contents of the frames to memory. This can be done concurrently while transmitting and receiving frames destined for that station.

The 82596DX/SX can be used in both baseband and broadband networks. It can be configured for maximum network efficiency (minimum contention overhead) with networks of any length. Its highly flexible CSMA/CD unit supports address field lengths of zero through six bytes for IEEE 802.3/Ethernet frame delimitation. It also supports 16- or 32-bit cyclic redundancy checks. The CRC can be transferred directly to memory for receive, operations or dynamically inserted for transmit operations. The CSMA/CD unit can also be configured for full duplex operation for high throughput in point-to-point connections.

The 82596 C-Step incorporates several new features not found in previous steppings. The following is a summary of the 82596 C-step's new features.

- The 82596 C-step fixes Errata found in the A1 and B steppings.
- The 82596 C-step has improved AC timings over both the A and B steppings.
- The 82596 C-step has a New Enhanced Big Endian Mode where in Linear Addressing mode, true 32-bit Big Endian functionality is achieved. New Enhanced Big Endian Mode is enabled by setting bit 7 of the SYSBUS byte. This mode is software compatible with the big endian mode of the B-step with one exception—no 32-bit addresses need to be swapped by software in the C-step. In this new mode, the 82596 C-step treats 32-bit address pointers as true 32-bit entities and the SCB absolute address and statistical counters are still treated as two 16-bit big endian entities. Not setting this mode will configure the 82596 C-step to be 100% compatible to the A1-step bit endian mode.
- The 82596 C-step is hardware and software compatible to both the A1 and B steppings allowing for easy "drop-in" to current designs. Pinout and control structures remain unchanged.

The 82596DX/SX is fabricated with Intel's reliable, 5-V, CHMOS IV (Process 648.8) technology. It is available in a 132-pin PQFP or PGA package.

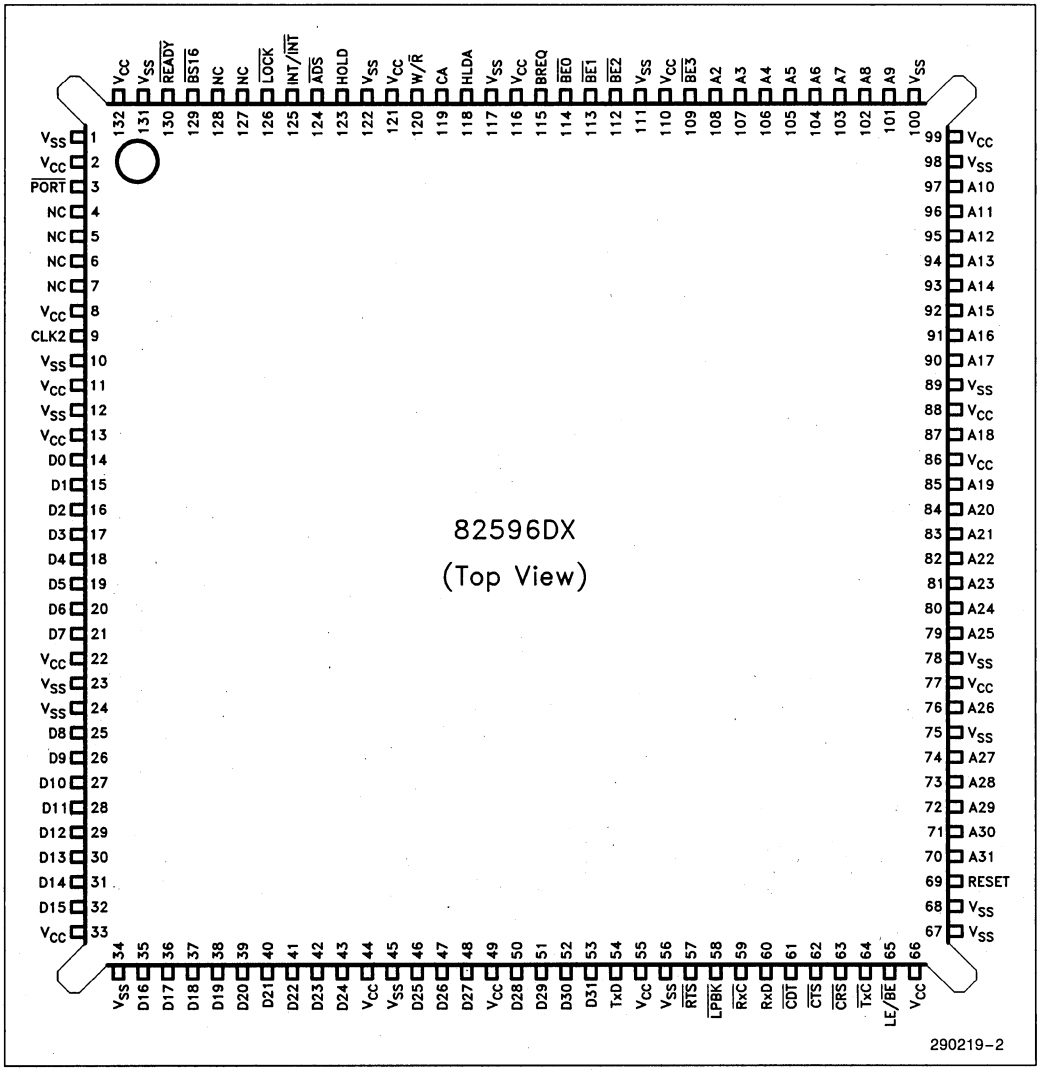


Figure 2a. 82596DX PQFP Pin Configuration

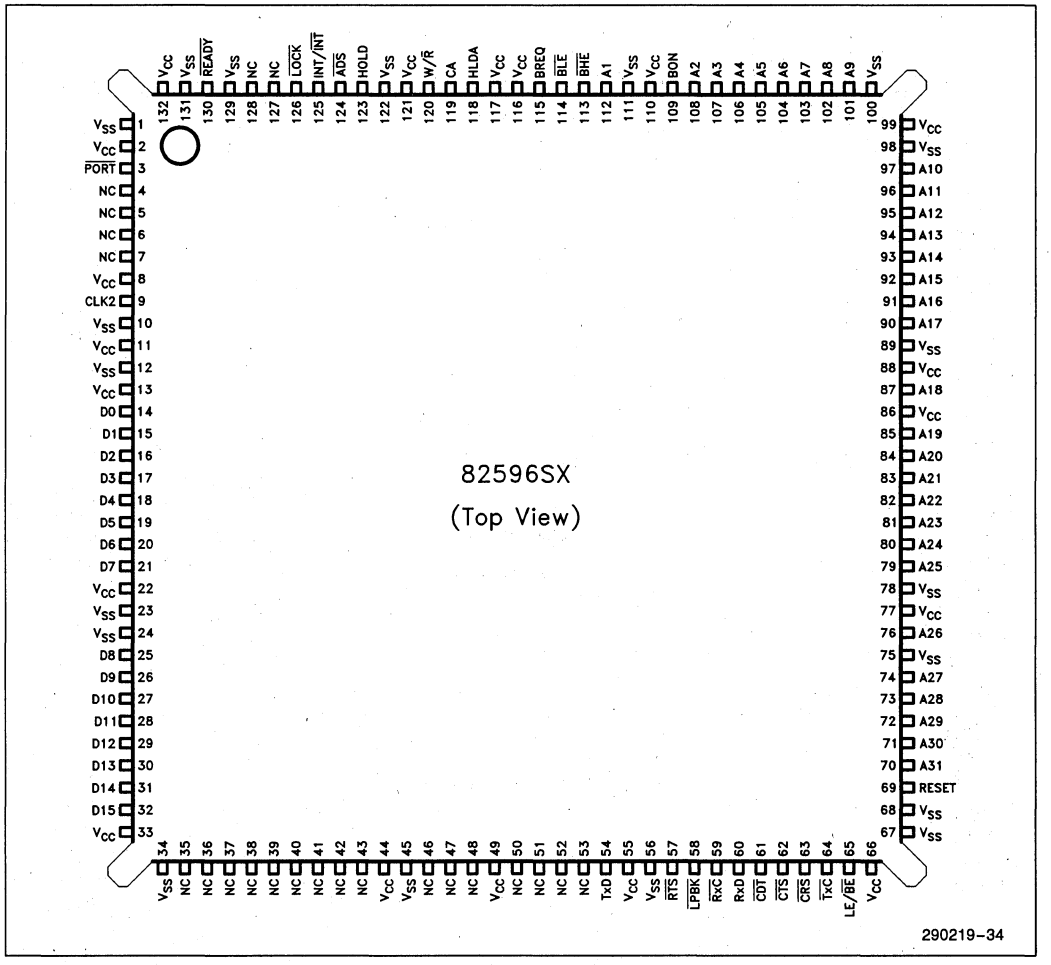


Figure 2b. 82596SX PQFP Pin Configuration

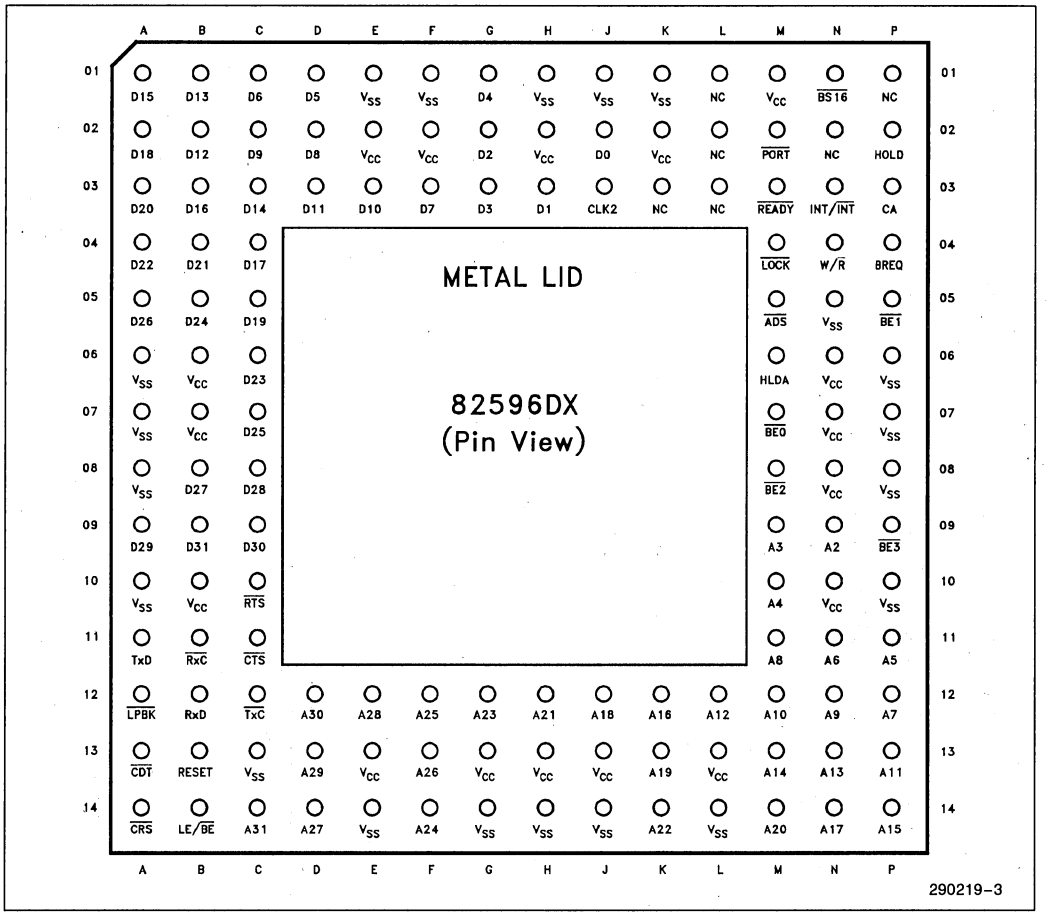


Figure 3a. 82596DX PGA Pin View Side

82596DX PGA Cross Reference by Pin Name

Address		Data		Control		Serial Interface		N/C	V_{CC}	V_{SS}
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Pin No.	Pin No.	Pin No.
A_2	N9	D_0	J2	$\overline{ADS}$	M5	$\overline{CDT}$	A13	K3	B6	A6
A_3	M9	D_1	H3	$\overline{BE0}$	M7	$\overline{CRS}$	A14	L1	B7	A7
A_4	M10	D_2	G2	$\overline{BE1}$	P5	$\overline{CTS}$	C11	L2	B10	A8
A_5	P11	D_3	G3	$\overline{BE2}$	M8	$\overline{LPBK}$	A12	L3	E2	A10
A_6	N11	D_4	G1	$\overline{BE3}$	P9	$\overline{RTS}$	C10	N2	E13	C13
A_7	P12	D_5	D1	BREQ	P4	$\overline{RxC}$	B11	P1	F2	E1
A_8	M11	D_6	C1	$\overline{BS16}$	N1	$\overline{RxD}$	B12		G13	E14
A_9	N12	D_7	F3	CA	P3	$\overline{TxC}$	C12		H2	F1
A_{10}	M12	D_8	D2	CLK2	J3	TxD	A11		H13	G14
A_{11}	P13	D_9	C2	HLDA	M6				J13	H1
A_{12}	L12	D_{10}	E3	HOLD	P2				K2	H14
A_{13}	N13	D_{11}	D3	INT/$\overline{INT}$	N3				L13	J1
A_{14}	M13	D_{12}	B2	LE/$\overline{BE}$	B14				M1	J14
A_{15}	P14	D_{13}	B1	$\overline{LOCK}$	M4				N6	K1
A_{16}	K12	D_{14}	C3	$\overline{PORT}$	M2				N7	L14
A_{17}	N14	D_{15}	A1	$\overline{READY}$	M3				N8	N5
A_{18}	J12	D_{16}	B3	RESET	B13				N10	P6
A_{19}	K13	D_{17}	C4	W/$\overline{R}$	N4					P7
A_{20}	M14	D_{18}	A2							P8
A_{21}	H12	D_{19}	C5							P10
A_{22}	K14	D_{20}	A3							
A_{23}	G12	D_{21}	B4							
A_{24}	F14	D_{22}	A4							
A_{25}	F12	D_{23}	C6							
A_{26}	F13	D_{24}	B5							
A_{27}	D14	D_{25}	C7							
A_{28}	E12	D_{26}	A5							
A_{29}	D13	D_{27}	B8							
A_{30}	D12	D_{28}	C8							
A_{31}	C14	D_{29}	A9							
		D_{30}	C9							
		D_{31}	B9							

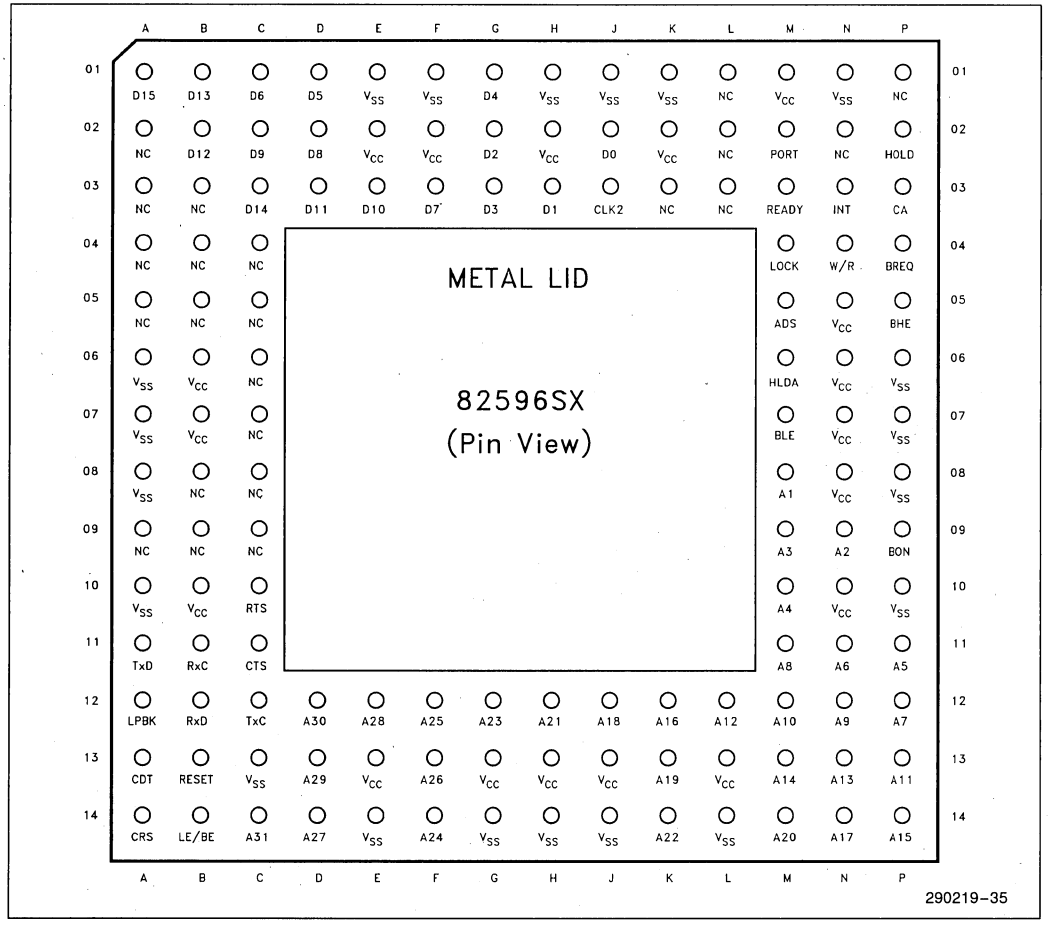


Figure 3b. 82596SX PGA Pin View Side

82596SX PGA Cross Reference by Pin Name

Address		Data		Control		Serial Interface		N/C	V_{CC}	V_{SS}
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Pin No.	Pin No.	Pin No.
A_2	N9	D_0	J2	$\overline{ADS}$	M5	$\overline{CDT}$	A13	A2	B6	A6
A_3	M9	D_1	H3	$\overline{BLE}$	M7	$\overline{CRS}$	A14	A3	B7	A7
A_4	M10	D_2	G2	$\overline{BHE}$	P5	$\overline{CTS}$	C11	A4	B10	A8
A_5	P11	D_3	G3	BON	P9	$\overline{LPBK}$	A12	A5	E2	A10
A_6	N11	D_4	G1	BREQ	P4	$\overline{RTS}$	C10	A9	E13	C13
A_7	P12	D_5	D1	CA	P3	$\overline{RxC}$	B11	B3	F2	E1
A_8	M11	D_6	C1	CLK2	J3	$\overline{RxD}$	B12	B4	G13	E14
A_9	N12	D_7	F3	HLDA	M6	$\overline{TxC}$	C12	B5	H2	F1
A_{10}	M12	D_8	D2	HOLD	P2	TxD	A11	B8	H13	G14
A_{11}	P13	D_9	C2	INT/$\overline{INT}$	N3			B9	J13	H1
A_{12}	L12	D_{10}	E3	LE/$\overline{BE}$	B14			C4	K2	H14
A_{13}	N13	D_{11}	D3	$\overline{LOCK}$	M4			C5	L13	J1
A_{14}	M13	D_{12}	B2	$\overline{PORT}$	M2			C6	M1	J14
A_{15}	P14	D_{13}	B1	$\overline{RDY}$	M3			C7	N5	K1
A_{16}	K12	D_{14}	C3	RESET	B13			C8	N6	L14
A_{17}	N14	D_{15}	A1	W/$\overline{R}$	N04			C9	N7	N1
A_{18}	J12							K3	N8	P6
A_{19}	K13							L1	N10	P7
A_{20}	M14							L2		P8
A_{21}	H12							L3		P10
A_{22}	K14							N2		
A_{23}	G12							P1		
A_{24}	F14									
A_{25}	F12									
A_{26}	F13									
A_{27}	D14									
A_{28}	E12									
A_{29}	D13									
A_{30}	D12									
A_{31}	C14									

PIN DESCRIPTIONS

<table>
<tr><th>Symbol</th><th>PQFP Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>CLK2</td><td>9</td><td>I</td><td>CLOCK. The system clock input provides the fundamental timing for the 82596. It is internally divided by two to generate the 82596 clock. All external timing parameters are specified in reference to the rising edge of CLK2. For clock levels see D.C. Characteristics.</td></tr>
<tr><td>D31–D0</td><td>14–53</td><td>I/O</td><td>DATA BUS. The 32 Data Bus lines are bidirectional, tri-state lines that provide the general purpose data path between the 82596 and memory. With the 82596DX the bus can be either 16 or 32 bits wide; this is determined by the $\overline{BS16}$ signal which is static. The 82596 always drives all 32 data lines during Write operations, even with a 16-bit bus. D0–D31 are floated after a Reset or when the bus is not acquired.
These lines are inputs during a CPU Port access; in this mode the CPU writes the next address to the 82596 through the Data lines. During $\overline{PORT}$ commands (Relocatable SCP, Self-Test, and Dump) the address must be aligned to a 16 byte boundary. This frees the D_3–D_0 lines so they can be used to distinguish the commands. The following is a summary of the decoding data.
<table>
<tr><th>D0</th><th>D1</th><th>D2</th><th>D3</th><th>D4–D31</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0000</td><td>Reset</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>ADDR</td><td>Relocatable SCP</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>ADDR</td><td>Self-Test</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>ADDR</td><td>Dump Command</td></tr>
</table></td></tr>
<tr><td>(D15–D0)</td><td>14–32</td><td>I/O</td><td>These 16 Data Bus lines are bidirectional, tri-state lines that provide the entire data path for the 82596SX. In the 82596SX D16–D31 are not connected (NC).</td></tr>
<tr><td>A31–A2</td><td>70–108</td><td>O</td><td>ADDRESS LINES. These 30 tri-stated Address lines output the address bits required for memory operation. These lines are floated after a Reset or when the bus is not acquired.</td></tr>
<tr><td>A1</td><td>112</td><td>O</td><td>The 82596SX requires this additional address line to output the address bits required for memory operation.</td></tr>
<tr><td>$\overline{BE3}$–$\overline{BE0}$</td><td>109–114</td><td>O</td><td>BYTE ENABLE. (82596DX only.) These tri-stated signals are used to indicate which bytes are involved with the current memory access. The number of Byte Enable signals asserted indicates the physical size of the data being transferred (1, 2, 3, or 4 bytes).
• $\overline{BE0}$ indicates D0–D7
• $\overline{BE1}$ indicates D8–D15
• $\overline{BE2}$ indicates D16–D23
• $\overline{BE3}$ indicates D24–D31
These lines are floated after a Reset or when the bus is not acquired.</td></tr>
<tr><td>$\overline{BHE}$, $\overline{BLE}$</td><td>113–114</td><td>O</td><td>(82596SX only.) These signals are the Byte High Enable and Byte Low Enable signals for the 82596SX.</td></tr>
<tr><td>BON</td><td>109</td><td>O</td><td>BUS ON. (82596SX only.) This signal is driven high when the 82596 is holding the bus. This signal is tri-stated when the bus is relinquished. BON has the same timing as the Byte Enables.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
W/$\overline{R}$	120	O	**WRITE/READ.** This dual-function pin is used to distinguish Write and Read cycles. This line is floated after a Reset or when the bus is not acquired.
$\overline{ADS}$	124	O	**ADDRESS STATUS.** This tri-state pin is used by the 82596 to indicate that a valid bus cycle has begun and that A31–A2, $\overline{BE3}$–$\overline{BE0}$, and W/$\overline{R}$ are being driven. It is asserted during t1 bus states. This line is floated after a Reset or when the bus is not acquired.
$\overline{RDY}$	130	I	**READY.** Active low. This signal is the acknowledgment from addressed memory that the transfer cycle can be completed. When high, it causes wait states to be inserted. It is ignored at the end of the first clock of the bus cycle's data cycle. This active-low signal does not have an internal pull-up resistor. This signal must meet the setup and hold times to operate correctly.
$\overline{LOCK}$	126	O	**LOCK.** This tri-state pin is used to distinguish locked and unlocked bus cycles. $\overline{LOCK}$ generates a semaphore handshake to the CPU. $\overline{LOCK}$ can be active for several memory cycles, it goes active during the first locked memory cycle (t1) and goes inactive at the last locked cycle (t2). This line is floated after a Reset or when the bus is not acquired. $\overline{LOCK}$ can be disabled via the sysbus byte in software.
$\overline{BS16}$	129	I	**BUS SIZE.** This signal allows the 82596DX to work with either 16- or 32-bit bytes. This signal is static and should be tied high for 32-bit operation or low for 16-bit operation. In Little Endian mode the D0–D15 lines are driven when $\overline{BS16}$ is inserted, in Big Endian mode the D16–D31 lines are driven.
HOLD	123	O	**HOLD.** The HOLD signal is active high, the 82596 uses it to request local bus mastership. In normal operation HOLD goes inactive before HLDA. The 82596 can be forced off the bus by deasserting HLDA or if the bus throttle timers expire.
HLDA	118	I	**HOLD ACKNOWLEDGE.** The HLDA signal is active high, it indicates that bus mastership has been given to the 82596. HLDA is internally synchronized; after HOLD is detected low, the CPU drives HLDA low. **NOTE** *Do not connect HLDA to V_{CC}—it will cause a deadlock.* A user wanting to give the 82596 permanent access to the bus should connect HLDA to HOLD. If HLDA goes inactive before HOLD, the 82596 will release the bus (by deasserting HOLD) within a specified number of system clocks.
BREQ	115	I	**BUS REQUEST.** This signal, when configured to an externally activated mode, is used to trigger the bus throttle timers.

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
$\overline{PORT}$	3	I	**PORT.** When this signal is received, the 82596 latches the data on the data bus into an internal 32-bit register. When the CPU is asserting this signal it can write into the 82596 (via the data bus). This pin must be activated twice during all CPU Port access commands.
RESET	69	I	**RESET.** This active high, internally synchronized signal causes the 82596 to terminate current activity. The signal must be high for at least five system clock cycles. After five system clock cycles and four TxC clock cycles the 82596 will execute a Reset when it receives a high RESET signal. When RESET returns to low, the 82596 waits for the first CA signal and then begins the initialization sequence.
LE/$\overline{BE}$	65	I	**LITTLE ENDIAN/BIG ENDIAN.** This dual-function pin is used to select byte ordering. When LE/$\overline{BE}$ is high, little endian byte ordering is used; when low, big endian byte ordering is used for data in frames (bytes) and for control (SCB, RFD, CBL, etc.).
CA	119	I	**CHANNEL ATTENTION.** The CPU uses this pin to force the 82596 to begin executing memory resident Command blocks. The CA signal is internally synchronized. The signal must be high for at least one system clock. It is latched internally on the high to low edge and then detected by the 82596. The first CA after a Reset forces the 82596 into the initialization sequence beginning at location 00FFFFF6h or an SCP address written to the 82596 using CPU Port access. All subsequent CA signals cause the 82596 to begin executing new command sequences from the SCB.
INT/$\overline{INT}$	125	O	**INTERRUPT.** A high signal on this pin notifies the CPU that the 82596 is requesting an interrupt. This signal is an edge triggered interrupt signal, and can be configured to be active high or low.
V_{CC}	18 Pins (DX) 19 Pins (SX)		**POWER.** +5V ±10%.
V_{SS}	19 Pins (DX and SX)		**GROUND.** 0V.
TxD	54	O	**TRANSMIT DATA.** This pin transmits data to the serial link. It is high when not transmitting.
$\overline{TxC}$	64	I	**TRANSMIT CLOCK.** This signal provides the fundamental timing for the serial subsystem. The clock is also used to transmit data synchronously on the TxD pin. For NRZ encoding, data is transferred to the TxD pin on the high to low clock transition. For Manchester encoding, the transmitted bit center is aligned with the low to high transition. Transmit clock should always be running for proper device operation.

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
$\overline{\text{LPBK}}$	58	O	**LOOPBACK.** This TTL-level control signal enables the loopback mode. In this mode serial data on the TxD input is routed through the 82C501 internal circuits and back to the RxD output without driving the transceiver cable. To enable this signal, both internal and external loopback need to be set with the Configure command.
RxD	60	I	**RECEIVE DATA.** This pin receives NRZ serial data only. It must be high when not receiving.
$\overline{\text{RxC}}$	59	I	**RECEIVE CLOCK.** This signal provides timing information to the internal shifting logic. For NRZ data the state of the RxD pin is sampled on the high to low transition of the clock.
$\overline{\text{RTS}}$	57	O	**REQUEST TO SEND.** When this signal is low the 82596 informs the external interface that it has data to transmit. It is forced high after a Reset or when transmission is stopped.
$\overline{\text{CTS}}$	62	I	**CLEAR TO SEND.** An active-low signal that enables the 82596 to send data. It is normally used as an interface handshake to $\overline{\text{RTS}}$. Asserting $\overline{\text{CTS}}$ high stops transmission. $\overline{\text{CTS}}$ is internally synchronized. If $\overline{\text{CTS}}$ goes inactive, meeting the setup time to the $\overline{\text{TxC}}$ negative edge, the transmission will stop and $\overline{\text{RTS}}$ will go inactive within, at most, two $\overline{\text{TxC}}$ cycles.
$\overline{\text{CRS}}$	63	I	**CARRIER SENSE.** This signal is active low, it is used to notify the 82596 that traffic is on the serial link. It is only used if the 82596 is configured for external Carrier Sense. In this configuration external circuitry is required for detecting traffic on the serial link. $\overline{\text{CRS}}$ is internally synchronized. To be accepted, the signal must remain active for at least two serial clock cycles (for CRSF = 0).
$\overline{\text{CDT}}$	61	I	**COLLISION DETECT.** This active-low signal informs the 82596 that a collision has occurred. It is only used if the 82596 is configured for external Collision Detect. External circuitry is required for collision detection. $\overline{\text{CDT}}$ is internally synchronized. To be accepted, the signal must remain active for at least two serial clock cycles (for CDTF = 0).

82596 AND HOST CPU INTERACTION

The 82596DX/SX and the host CPU communicate through shared memory. Because of its on-chip DMA capability, the 82596 can make data block transfers (buffers and frames) independently of the CPU; this greatly reduces the CPU byte transfer overhead.

NOTE:
The 82596DX and 82596SX differ in their address pin definitions and their data bus sizes. Information in this data sheet applies to both versions unless otherwise stated.

The 82596 is a multitasking coprocessor that comprises two independent logical units—the Command Unit (CU) and the Receive Unit (RU). The CU executes commands from shared memory. The RU handles all activities related to frame reception. The independence of the CU and RU enables the 82596 to engage in both activities simultaneously—the CU can fetch and execute commands from memory while the RU is storing received frames in memory. The CPU is only involved with this process after the CU has executed a sequence of commands or the RU has finished storing a sequence of frames.

The CPU and the 82596 use the hardware signals Interrupt (INT) and Channel Attention (CA) to initiate communication with the System Control Block (SCB), see Figure 4. The 82596 uses INT to alert the CPU of a change in the contents of the SCB, the CPU uses CA to alert the 82596.

The 82596 has a CPU Port Access state that allows the CPU to execute certain functions without accessing memory. The 82596 $\overline{\text{PORT}}$ pin and data bus pins are used to enable this feature. The CPU can directly activate four operations when the 82596 is in this state.

- Write an alternative System Configuration Pointer (SCP). This can be used when the 82596 cannot use the default SCP address space.
- Write a different Dump Command Pointer and execute Dump. This can be used for troubleshooting No Response problems.
- The CPU can reset the 82596 via software without disturbing the rest of the system.
- A self-test can be used for board testing; the 82596 will execute a self-test and write the results to memory.

82596 BUS INTERFACE

The 82596DX/SX has bus interface timings and pin definitions that are compatible with Intel's 32-bit i386 DX and i386 SX microprocessors. This eliminates the need for additional bus interface logic. Operating at 33 MHz, the 82596's bus bandwidth can be as high as 66 MB/s. Since Ethernet only requires 1.25 MB/s, this leaves a considerable amount of bandwidth for the CPU. The 82596 also has a bus throttle to regulate its use of the bus. Two timers can be programmed through the SCB: one controls the maximum time the 82596 can remain on the bus, the other controls the time the 82596 must stay off the bus (see Figure 5). The bus throttle can be programmed to trigger internally with HLDA or externally with BREQ. These timers can restrict the 82596 HOLD activation time and improve bus utilization.

82596 MEMORY ADDRESSING

The 82596 has a 32-bit memory address range, which allows addressing up to four gigabytes of memory. The 82596 has three memory addressing modes (see Table 1).

- **82586 Mode.** The 82596 has a 24-bit memory address range. The System Control Block, Command List, Receive Descriptor List, and Buffer Descriptors must reside in one 64-kB memory segment. Transmit and Receive buffers can reside in a 24-bit address space.
- **32-Bit Segmented Mode.** The 82596 has a 32-bit memory address range. The System Control Block, Command List, Receive Descriptor List, and Buffer Descriptors must reside in one 64-kB memory segment. Transmit and Receive buffers can reside in a 32-bit address space.
- **Linear Mode.** The 82596 has a 32-bit memory address range. Any memory structure can reside anywhere within the 32-bit memory address range.

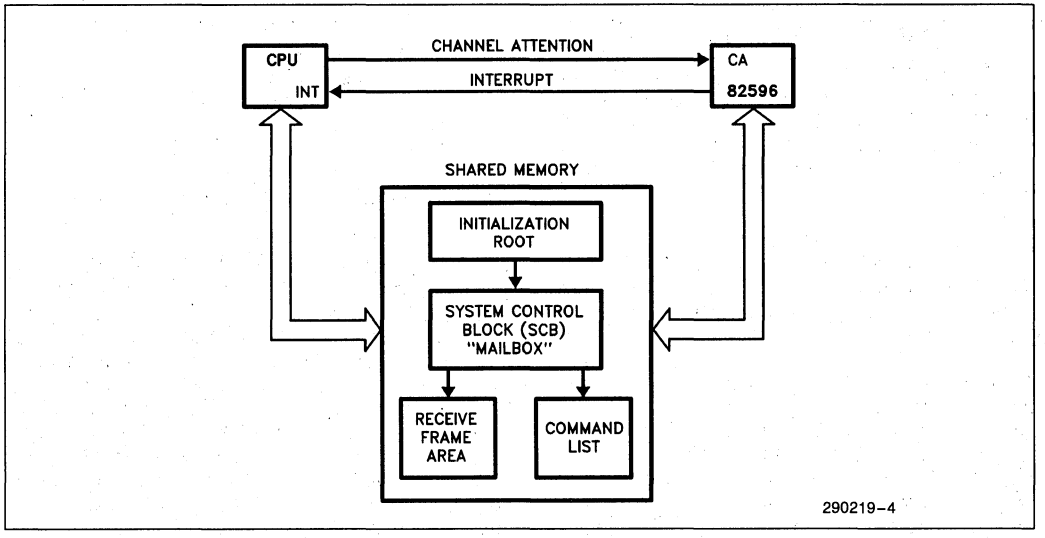


Figure 4. 82596 and Host CPU Intervention

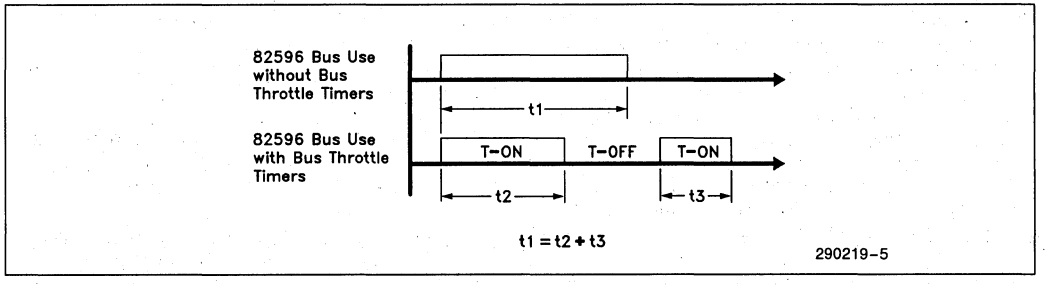


Figure 5. Bus Throttle Timers

Table 1. 82596 Memory Addressing Formats

Pointer or Offset	Operation Mode		
	82586	32-Bit Segmented	Linear
ISCP ADDRESS	24-Bit Linear	32-Bit Linear	32-Bit Linear
SCB ADDRESS	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Command Block Pointers	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Frame Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Tx Frame Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Buffer Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Tx Buffer Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Buffers	24-Bit Linear	32-Bit Linear	32-Bit Linear
Tx Buffers	24-Bit Linear	32-Bit Linear	32-Bit Linear

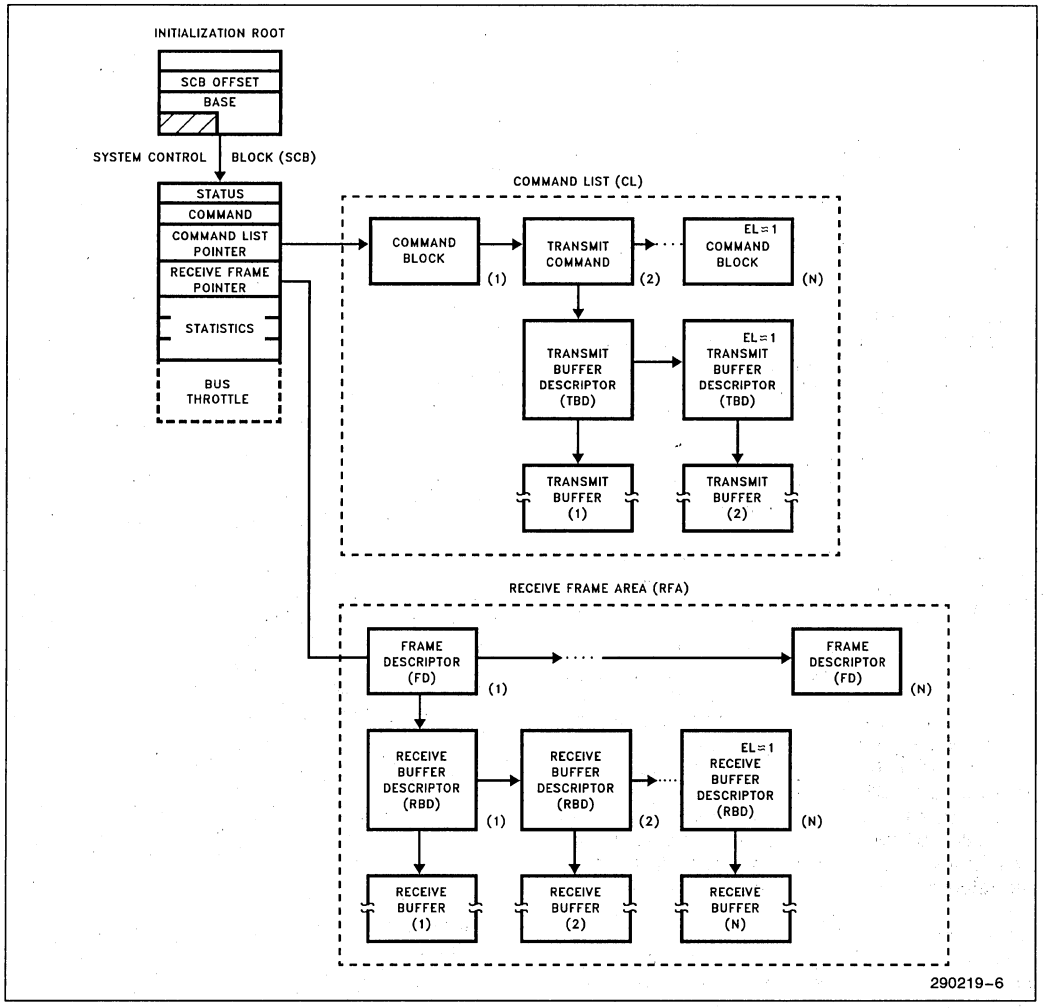


Figure 6. 82596 Shared Memory Structure

82596 SYSTEM MEMORY STRUCTURE

The Shared Memory structure consists of four parts: the Initialization Root, the System Control Block, the Command List, and the Receive Frame Area (see Figure 6).

The Initialization Root is in an established location known to the host CPU and the 82596 (00FFFFF6h). However, the CPU can establish the Initialization Root in another location by using the CPU Port access. This root is accessed during initialization, and points to the System Control Block.

The System Control Block serves as a bidirectional mail drop for the host CPU and the 82596 CU and RU. It is the central point through which the CPU and the 82596 exchange control and status information. The SCB has two areas. The first contains instructions from the CPU to the 82596. These include: control of the CU and RU (Start, Abort, Suspend, and Resume), a pointer to the list of CU commands, a pointer to the Receive Frame Area, a set of Interrupt Acknowledge bits, and the T-ON and T-OFF timers for the bus throttle. The second area contains status information the 82596 is sending to the CPU. Such as, the CU and RU states (Idle, Active

Ready, Suspended, No Receive Resources, etc.), interrupt bits (Command Completed, Frame Received, CU Not Ready, and RU Not Ready), and statistical counters.

The Command List functions as a program for the CU; individual commands are placed in memory units called Command Blocks (CBs). These CBs contain the parameters and status of specific high-level commands called Action Commands; e.g., Transmit or Configure.

Transmit causes the 82596 to transmit a frame. The Transmit CB contains the destination address, the length field, and a pointer to a list of linked buffers holding the frame that is to be constructed from several buffers scattered throughout memory. The Command Unit operates without CPU intervention; the DMA for each buffer, and the prefetching of references to new buffers, is performed in parallel. The CPU is notified only after a transmission is complete.

The Receive Frame Area is a list of Free Frame Descriptors (descriptors not yet used) and a list of user-prepared buffers. Frames arrive at the 82596 unsolicited; the 82596 must always be ready to receive and store them in the Free Frame Area. The Receive Unit fills the buffers when it receives frames, and reformats the Free Buffer List into received-frame structures. The frame structure is, for all practical purposes, identical to the format of the frame to be transmitted. The first Frame descriptor is referenced by the SCB. Unless the 82596 is configured to Save Bad Frames, the frame descriptor, and the associated buffer descriptor, which is wasted when a bad frame is received, are automatically reclaimed and returned to the Free Buffer List.

Receive buffer chaining (storing incoming frames in a linked buffer list) significantly improves memory utilization. Without buffer chaining, the user must allocate consecutive blocks of memory, each capable of containing a maximum frame (for Ethernet, 1518 bytes). Since an average frame is about 200 bytes, this is very inefficient. With buffer chaining, the user can allocate small buffers and the 82596 will only use those that are needed.

Figure 7 A–D illustrates how the 82596 uses the Receive Frame Area. Figure 7A shows an unused Receive Frame Area composed of Free Frame Descriptors and Free Receive Buffers prepared by the user. The SCB points to the first Frame Descriptor of the Frame Descriptor List. Figure 7B shows the same Receive Frame Area after receiving one frame. This first frame occupies two Receive Buffers and one Frame Descriptor—a valid received frame will only occupy one Frame Descriptor. After receiving this frame the 82596 sets the next Free Frame Descriptor RBD pointer to the next Free RBD. Figure 7C shows the RFA after receiving a second frame. In this example the second frame occupies only one Receive Buffer and one RFD. The 82596 again sets the RBD pointer. This process is repeated again in Figure 7D, showing the reception of another frame using one Receive Buffer; in this example there is an extra Frame Descriptor.

TRANSMIT AND RECEIVE MEMORY STRUCTURES

There are three memory structures for reception and transmission. The 82586 memory structure, the Flexible memory structure, and the Simplified memory structure. The 82586 mode is selected by configuring the 82596 during initialization. In this mode all the 82596 memory structures are compatible with the 82586 memory structures.

When the 82596 is not configured to the 82586 mode, the other two memory structures, Simplified and Flexible, are available for transmitting and receiving. These structures are selected by setting the S/F bit in the Transmit Command and/or the Receive Frame Descriptor (see Figures 29, 30, 41, and 42). It is recommended that any linked list of buffers be relegated to a single type—either simplified or flexible. The Simplified memory structure offers a simple structure for ease of programming (see Figure 8). All information about a frame is contained in one structure; for example, during reception the RFD and data field are contained in one structure.

The Flexible memory structure (see Figure 9) has a control field that allows the programmer to specify the amount of receive data the RFD will contain for receive operations and the amount of transmit data the Transmit Command Block will contain for transmit operations. For example, when the control field in the RFD is set to 20 bytes during a reception, the first 20 bytes of the data field are stored in the RFD (6 Bytes of Destination Address, 6 Bytes of Source Address, 2 Bytes of Length Field, and 6 Bytes of Data), and the remainder of the data field is stored in the Receive Data Buffers. This is useful for capturing frame headers when header information is contained in the data field. The header information can then be automatically stored in the RFD partitioned from the Receive Data Buffer.

The control field can also be used for the Transmit Command when the Flexible memory structure is used. The quantity of data field bytes to be transmitted from the Transmit Command Block is specified by the variable control field.

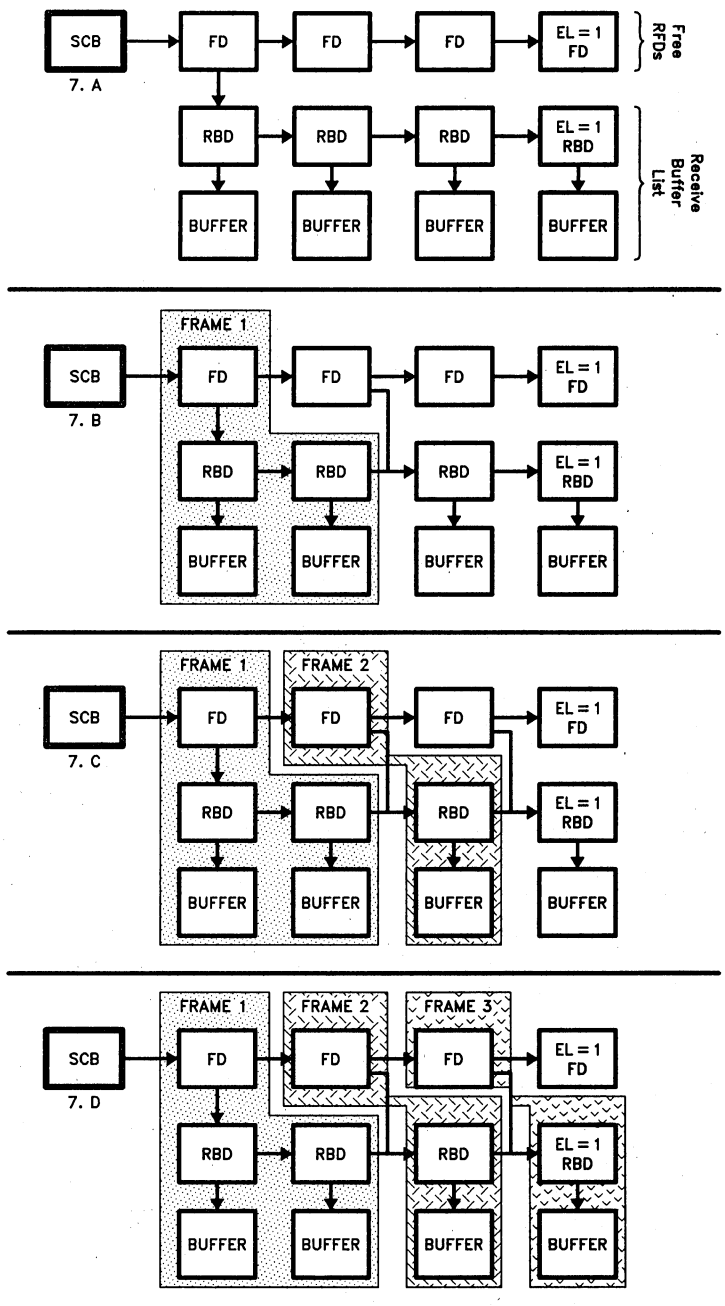


Figure 7. Frame Reception in the RFA

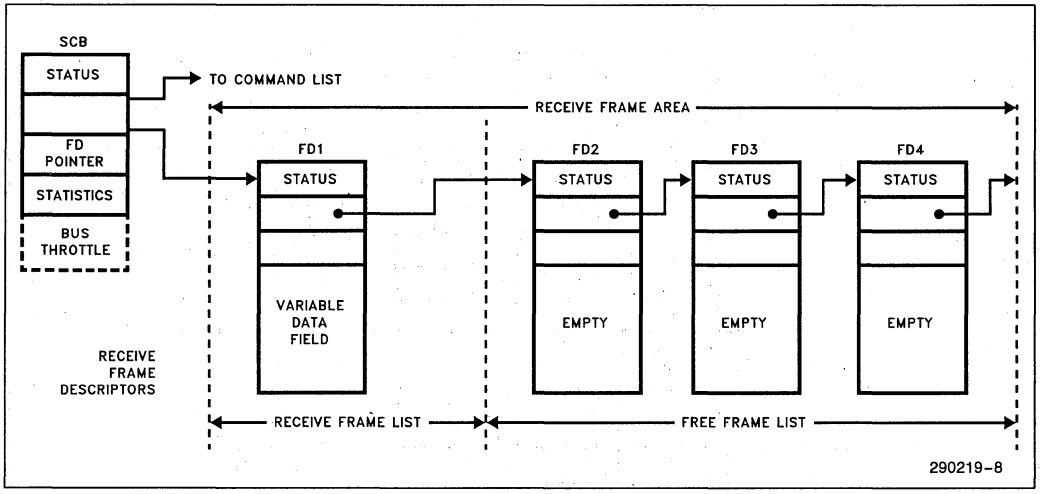


Figure 8. Simplified Memory Structure

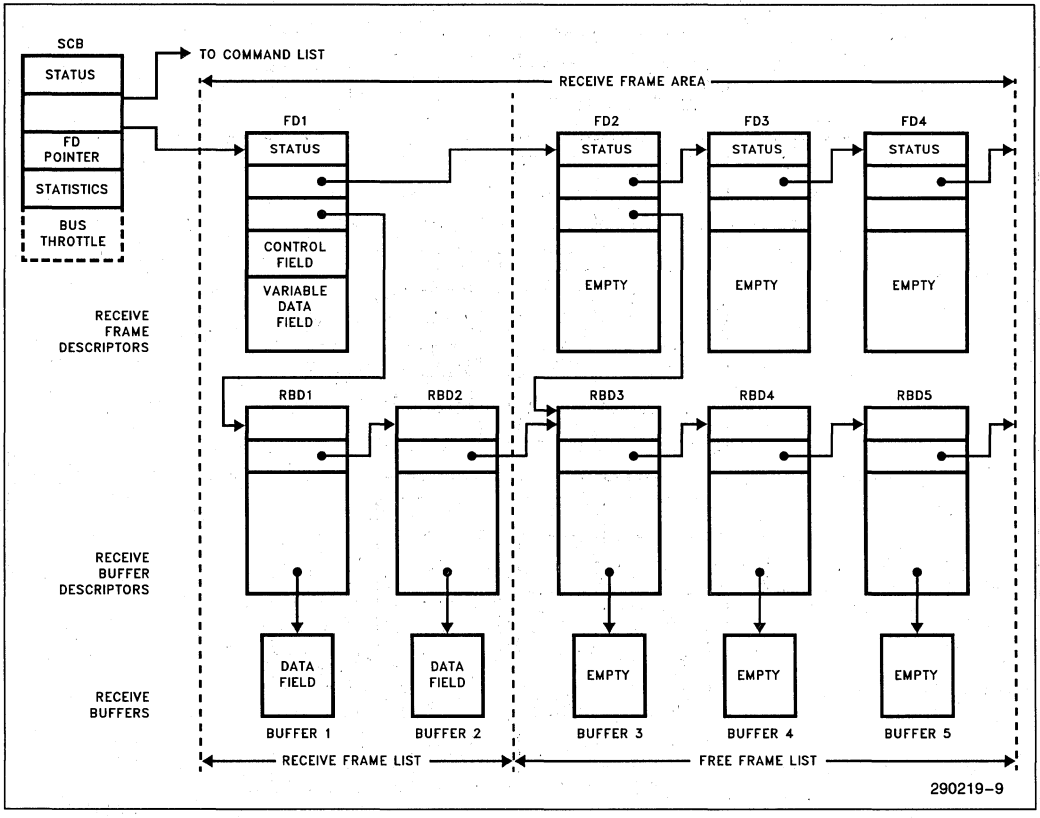


Figure 9. Flexible Memory Structure

TRANSMITTING FRAMES

The 82596 executes high-level Action Commands from the Command List in system memory. Action Commands are fetched and executed in parallel with the host CPU operation, thereby significantly improving system performance. The format of the Action Commands is shown in Figure 10. Figure 28 shows the 82586 mode, and Figures 29 and 30 shows the command formats of the Linear and 32-bit Segmented modes.

A single Transmit command contains, as part of the command-specific parameters, the destination address and length field of the transmitted frame and a pointer to buffer area in memory containing the data portion of the frame. The data field is contained in a memory data structure consisting of a buffer descriptor (BD) and a data buffer—or a linked list of buffer descriptors and buffers—as shown in Figure 11.

Multiple data buffers can be chained together using the BDs. Thus, a frame with a long data field can be transmitted using several (shorter) data buffers chained together. This chaining technique allows the system designer to develop efficient buffer management.

The 82596 automatically generates the preamble (alternating 1s and 0s) and start frame delimiter, fetches the destination address and length field from the Transmit command, inserts its unique address as the source address, fetches the data field specified by the Transmit command, and computes and appends the CRC to the end of the frame (see Figure 12). In the Linear and 32-bit Segmented mode the CRC can be optionally inserted on a frame-by-frame basis by setting the NC bit in the Transmit Command Block (see Figures 29 and 30).

The 82596 generates the standard End Of Carrier (EOC) start and end frame delimiters. In EOC, the start frame delimiter is 10101011 and the end frame delimiter is indicated by the lack of a signal after the last bit of the frame check sequence field has been transmitted. In EOC, the 82596 can be configured to extend short frames by adding pad bytes (7Eh) during transmission, according to the length field.

When a collision occurs, the 82596 manages the jam, random wait, and retry processes, reinitializing DMA pointers without CPU intervention. Multiple frames can be sent by linking the appropriate number of Transmit commands together. This is particularly useful when transmitting a message larger than the maximum frame size (1518 bytes for Ethernet).

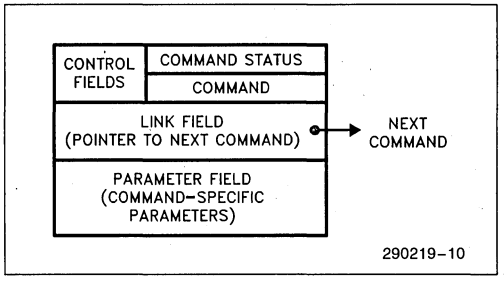


Figure 10. Action Command Format

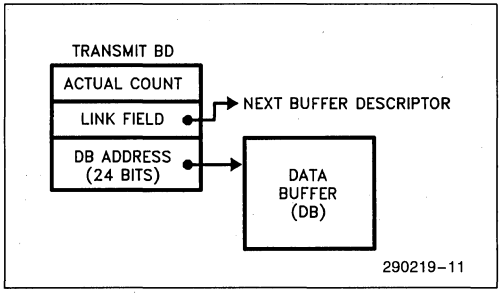


Figure 11. Data Buffer Descriptor and Data Buffer Structure

PREAMBLE	START FRAME DELIMITER	DESTINATION ADDRESS	SOURCE ADDRESS	LENGTH FIELD	DATA FIELD	FRAME CHECK SEQUENCE	END FRAME DELIMITER

Figure 12. Frame Format

RECEIVING FRAMES

To reduce CPU overhead, the 82596 is designed to receive frames without CPU supervision. The host CPU first sets aside an adequate receive buffer space and then enables the 82596 Receive Unit. Once enabled, the RU watches for arriving frames and automatically stores them in the Receive Frame Area (RFA). The RFA contains Receive Frame Descriptors, Receive Buffer Descriptors, and Data Buffers (see Figure 13). The individual Receive Frame Descriptors make up a Receive Descriptor List (RDL) used by the 82596 to store the destination and source addresses, the length field, and the status of each frame received (see Figure 14).

Once enabled, the 82596 checks each passing frame for an address match. The 82596 will recognize its own unique address, one or more multicast addresses, or the broadcast address. If a match is found the 82596 stores the destination and source addresses and the length field in the next available RFD. It then begins filling the next available Data Buffer on the FBL, which is pointed to by the current RFD, with the data portion of the incoming frame. As one Data Buffer is filled, the 82596 automatically fetches the next DB on the FBL until the entire frame is received. This buffer chaining technique is particularly memory efficient because it allows the system designer to set aside buffers to fit frames much shorter than the maximum allowable frame length. If AL-LOC = 1, or if the flexible memory structure is used, the addresses and length field can be placed in the receive buffer.

Once the entire frame is received without error, the 82596 does the following housekeeping tasks.

- The actual count field of the last Buffer Descriptor used to hold the frame just received is updated with the number of bytes stored in the associated Data Buffer.
- The next available Receive Frame Descriptor is fetched.
- The address of the next available Buffer Descriptor is written to the next available Receive Frame Descriptor.
- A frame received interrupt status bit is posted in the SCB.
- An interrupt is sent to the CPU.

If a frame error occurs, for example a CRC error, the 82596 automatically reinitializes its DMA pointers and reclaims any data buffers containing the bad frame. The 82596 will continue to receive frames without CPU help as long as Receive Frame Descriptors and Data Buffers are available.

82596 NETWORK MANAGEMENT AND DIAGNOSTICS

The behavior of data communication networks is normally very complex because of their distributed and asynchronous nature. It is particularly difficult to pinpoint a failure when it occurs. The 82596 has extensive diagnostic and network management functions that help improve reliability and testability. The 82596 reports on the following events after each frame is transmitted.

- Transmission successful.
- Transmission unsuccessful. Lost Carrier Sense.
- Transmission unsuccessful. Lost Clear to Send.
- Transmission unsuccessful. A DMA underrun occurred because the system bus did not keep up with the transmission.
- Transmission unsuccessful. The number of collisions exceeded the maximum allowed.
- Number of Collisions. The number of collisions experienced during transmission of the frame.
- Heartbeat Indicator. This indicates the presence of a heartbeat during the last Interframe Spacing (IFS) after transmission.

When configured to Save Bad Frames the 82596 checks each incoming frame and reports the following errors.

- CRC error. Incorrect CRC in a properly aligned frame.
- Alignment error. Incorrect CRC in a misaligned frame.
- Frame too short. The frame is shorter than the value configured for minimum frame length.
- Overrun. Part of the frame was not placed in memory because the system bus did not keep up with incoming data.
- Out of buffer. Part of the frame was discarded because of insufficient memory storage space.
- Receive collision. A collision was detected during reception and the destination address of the incoming frame passes 82596 address filtering. Collisions in the preamble are not counted.
- Length error. A frame not matching the frame length parameter was detected.

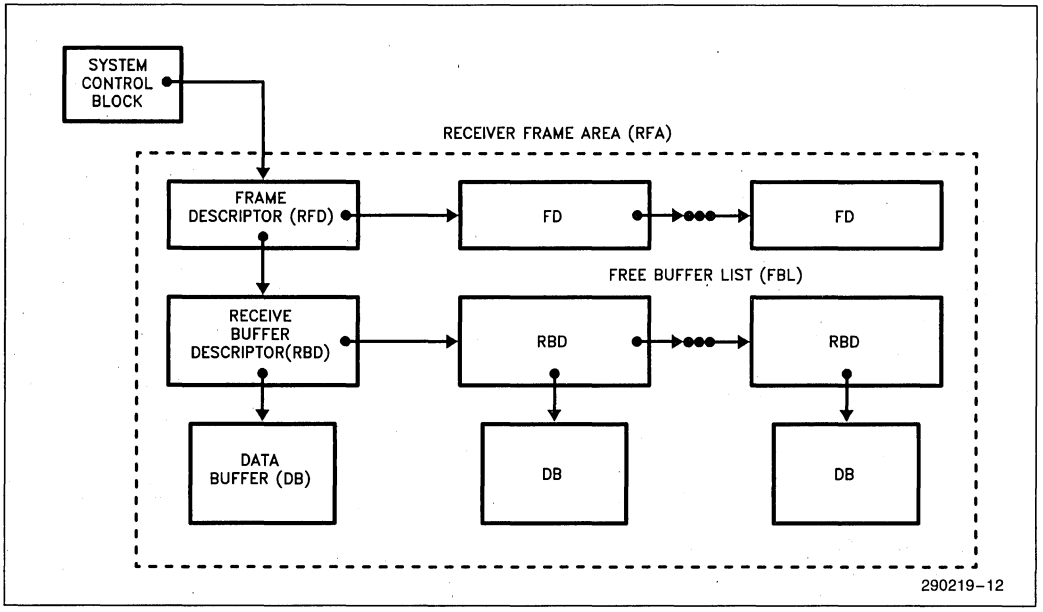


Figure 13. Receive Frame Area Diagram

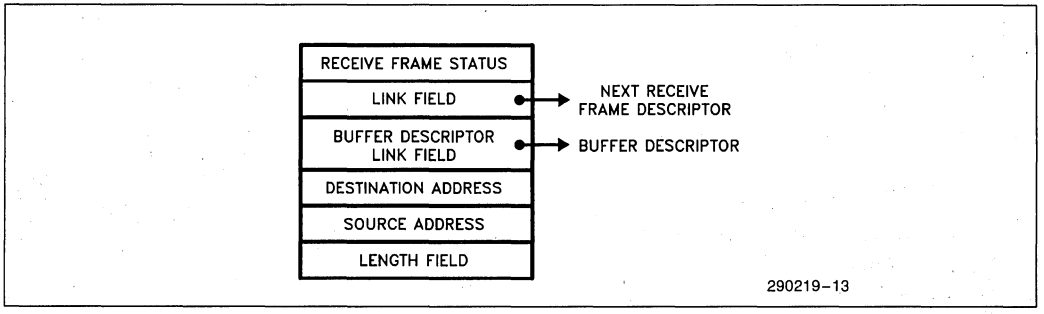


Figure 14. Receive Frame Descriptor

NETWORK PLANNING AND MAINTENANCE

To properly plan, operate, and maintain a communication network, the network management entity must accumulate information on network behavior. The 82596 provides a rich set of network-wide diagnostics that can serve as the basis for a network management entity.

Information on network activity is provided in the status of each frame transmitted. The 82596 reports the following activity indicators after each frame.

- Number of collisions. The number of collisions the 82596 experienced while attempting to transmit the frame.
- Deferred transmission. During the first transmission attempt the 82596 had to defer to traffic on the link.

The 82596 updates its 32-bit statistical counters after each received frame that both passes address filtering and is longer than the Minimum Frame Length configuration parameter. The 82596 reports the following statistics.

- CRC errors. The number of well-aligned frames that experienced a CRC error.
- Alignment errors. The number of misaligned frames that experienced a CRC error.
- No resources. The number of frames that were discarded because of insufficient resources for reception.
- Overrun errors. The number of frames that were not completely stored in memory because the system bus did not keep up with incoming data.
- Receive Collision counter. The number of collisions detected during receive. Collisions occurring before the minimum frame length will be counted as short frames. Collisions in the preamble will not be counted at all.
- Short Frame counter. The number of frames that were discarded because they were shorter than the configured minimum frame length.

Once again, these counters are not updated until the 82596 decodes a destination address match.

The 82596 can be configured to Promiscuous mode. In this mode it captures all frames transmitted on the network without checking the Destination Address. This is useful when implementing a monitoring station to capture all frames for analysis.

A useful method of capturing frame headers is to use the Simplified memory mode, configure the 82596 to Save Bad Frames, and configure the 82596 to Promiscuous mode with space in the RFD allocated for specific number of receive data bytes. The 82596 will receive all frames and put them in the RFD. Frames that exceed the available space in the RFD will be truncated, the status will be updated, and the 82596 will retrieve the next RFD. This allows the user to capture the initial data bytes of each frame (for instance, the header) and discard the remainder of the frame.

The 82596 also has a monitor mode for network analysis. During normal operation the receive function enables the 82596 to receive frames which pass address filtering. These frames must have the Start of Frame Delimiter (SFD) field and must be longer than the absolute minimum frame length of 5 bytes (6 bytes in case of Multicast address filtering). Contents and status of the received frames are transferred to memory. The monitor function enables the 82596 to simply evaluate the incoming frames. The 82596 can monitor the frames that pass or do not pass the address filtering. It can also monitor frames which do not have the SFD fields. The 82596 can be configured to only keep statistical information about monitor frames. Three options are available in the Monitor mode. These modes are selectable by the two monitor mode configuration bits available in the configuration command.

When the first option is selected, the 82596 receives good frames that pass address filtering and transfers them to memory while monitoring frames that do not pass address filtering or are shorter than the minimum frame size (these frames are not transferred to memory). When this option is used the 82596 updates six counters: CRC errors, alignment errors, no resource errors, overrun errors, short frames, and total good frames received.

When the second option is selected, the receive function is completely disabled. The 82596 monitors only those frames that pass address filterings and meet the minimum frame length requirement. When this option is used the 82596 updates six counters: CRC errors, alignment errors, total frames (good and bad), short frames, collisions detected, and total good frames.

When the third option is selected, the receive function is completely disabled. The 82596 monitors all frames, including frames that do not have a Start Frame Delimiter. When this option is used the 82596 updates six counter (CRC errors, alignment errors, total frames (good and bad), short frames, collisions detected, and total good frames.

STATION DIAGNOSTICS AND SELF-TEST

The 82596 provides a large set of diagnostic and network management functions. These include internal and external loopback and time domain reflectometry for locating fault points in the network cable. The 82596 ensures software reliability by dumping the contents of the 82596 internal registers into system memory. The 82596 has a self-test mode that enables it to run an internal self-test and place the results in system memory.

82586 SOFTWARE COMPATIBILITY

The 82596 has a software-compatible state in which all its memory structures are compatible with the 82586 memory structure. This includes all the Action Commands, the Receive Frame Area (including the RFD, Buffer Descriptors, and Data Buffers), the System Control Block, and the initialization procedures. There are two minor differences between the 82596 in the 82586-Compatible memory structure and the 82586.

- When the internal and external loopback bits in the Configure command are set to 11 the 82596 is in external loopback and the $\overline{\text{LPBK}}$ pin is activated; in the 82586 this situation would produce internal loopback.
- During a Dump command both the 82596 and 82586 dump the same number of bytes; however, the data format is different.

INITIALIZING THE 82596

A Reset command is issued to the 82596 to prepare it for normal operation. The 82596 is initialized through two data structures that are addressed by two pointers, the System Configuration Pointer (SCP) and the Intermediate System Configuration Pointer (ISCP). The initialization procedure begins when a Channel Attention signal is asserted after RESET. The 82596 uses the address of the double word that contains the SCP as a default—00FFFFF4h. Before the CA signal is asserted this default address can be changed to any other available address by asserting the $\overline{\text{PORT}}$ pin and providing the desired address over the $D_{31}-D_4$ pins of the address bus. Pins D_3-D_0 must be 0010; i.e., any alternative address must be aligned to 16 byte boundaries. All addresses sent to the 82596 must be word aligned, which means that all pointers and memory structures must start on an even address (A_0 = zero).

SYSTEM CONFIGURATION POINTER (SCP)

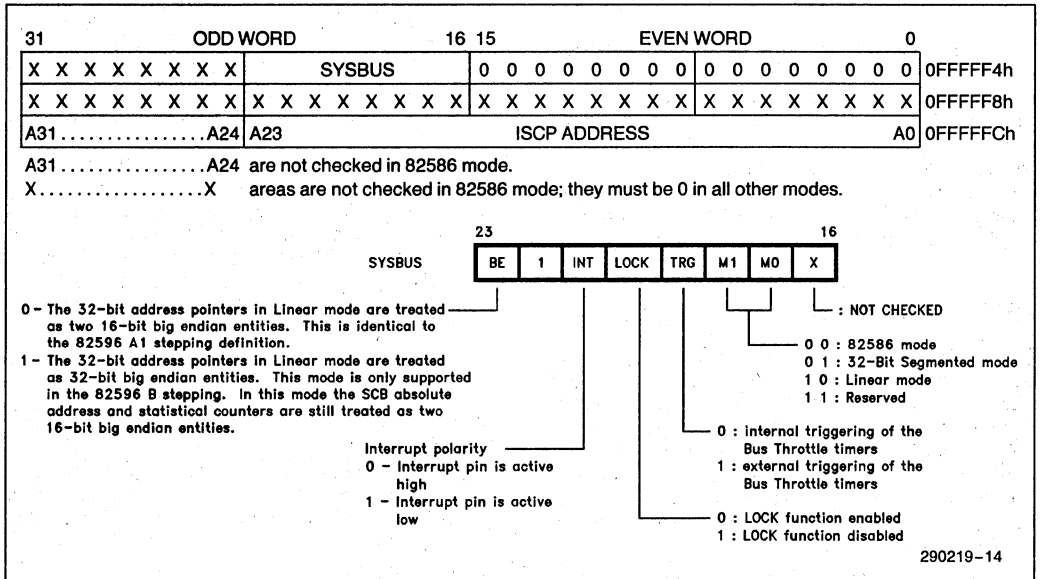
The SCP contains the SYSBUS byte and the location of the next structure of the initialization process, the ISCP. The following parameters are selected in the SYSBUS.

- The 82596 operation mode.
- The Bus Throttle timer triggering method.
- Lock enabled.
- Interrupt polarity.
- Big Endian 32-bit entity mode.

Byte ordering is determined by the LE/$\overline{\text{BE}}$ pin. LE/$\overline{\text{BE}}$ = 1 selects little endian byte ordering and LE/$\overline{\text{BE}}$ = 0 selects big endian byte ordering.

NOTE:
In the following, X indicates a bit not checked in 82586 mode. This bit must be set to 0 in all other modes.

The following diagram illustrates the format of the SCP.



ISCP ADDRESS— The physical address of the ISCP. In the 82586 mode, bits A31–A24 are considered to be zero.

Figure 15. The System Configuration Pointer

Writing the Sysbus

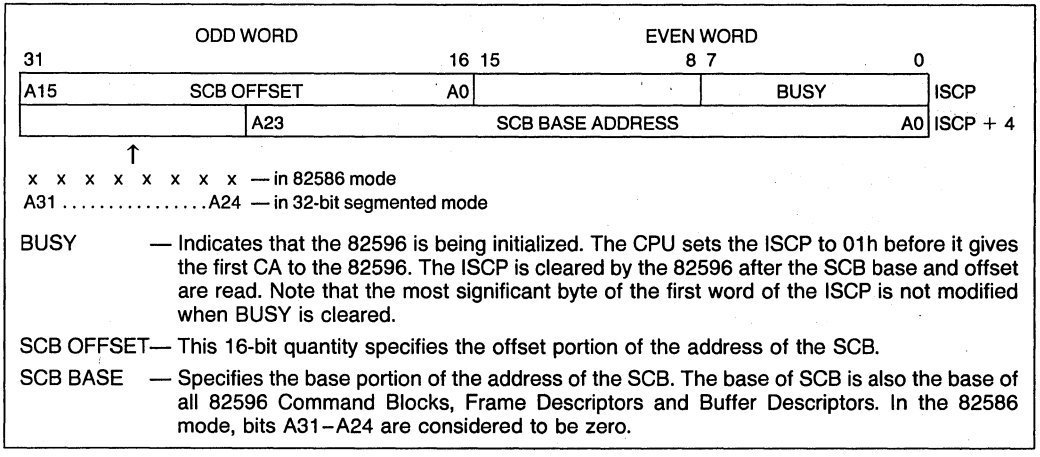
When writing the Sysbus byte it is important to pay attention to the byte order.

- When a Little Endian processor is used, the Sysbus byte is located at byte address 00FFFFF6h (or address $n+2$ if an alternative SCP address n was programmed).
- When a processor using Big Endian byte ordering is used, the SYSBUS, alternative SCP, and ISCP addresses will be different.
  - The Sysbus byte is located at 00FFFFF7h.
  - If an alternative SCP address is programmed, the SYSBUS byte should be at byte address $n+1$.

INTERMEDIATE SYSTEM CONFIGURATION POINTER (ISCP)

The ISCP indicates the location of the System Control Block. Often the SCP is in ROM and the ISCP is in RAM. The CPU loads the SCB address (or an equivalent data structure) into the ISCP and asserts CA. This Channel Attention signal causes the 82596 to begin its initialization procedure and to get the SCB address from the ISCP and SCP. In 82586 and 32-bit Segmented modes the SCP base address is also the base address of all Command Blocks, Frame Descriptors, and Buffer Descriptors (but not buffers). All these data structures must reside in one 64-kB segment; however, in Linear mode no such limitation is imposed.

The following diagram illustrates the ISCP format.

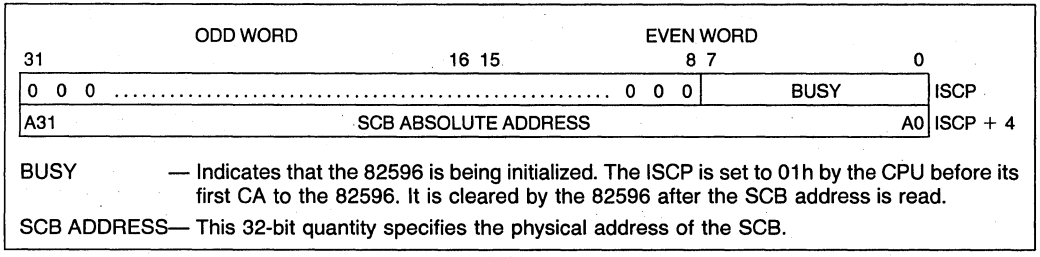


BUSY — Indicates that the 82596 is being initialized. The CPU sets the ISCP to 01h before it gives the first CA to the 82596. The ISCP is cleared by the 82596 after the SCB base and offset are read. Note that the most significant byte of the first word of the ISCP is not modified when BUSY is cleared.

SCB OFFSET— This 16-bit quantity specifies the offset portion of the address of the SCB.

SCB BASE — Specifies the base portion of the address of the SCB. The base of SCB is also the base of all 82596 Command Blocks, Frame Descriptors and Buffer Descriptors. In the 82586 mode, bits A31–A24 are considered to be zero.

Figure 16. The Intermediate System Configuration Pointer—82586 and 32-Bit Segmented Modes



BUSY — Indicates that the 82596 is being initialized. The ISCP is set to 01h by the CPU before its first CA to the 82596. It is cleared by the 82596 after the SCB address is read.

SCB ADDRESS— This 32-bit quantity specifies the physical address of the SCB.

Figure 17. The Intermediate System Configuration Pointer—Linear Mode.

INITIALIZATION PROCESS

The CPU sets up the SCP, ISCP, and the SCB structures, and, if desired, an alternative SCP address. It also sets BUSY to 01h. The 82596 is initialized when a Channel Attention signal follows a Reset signal, causing the 82596 to access the System Configuration Pointer. The sysbus byte, the operational mode, the bus throttle timer triggering method, the interrupt polarity, and the state of $\overline{LOCK}$ are read. After reset the bus throttle

timers are essentially disabled—the T-ON value is infinite, the T-OFF value is zero. After the SCP is read, the 82596 reads the ISCP and saves the SCB address. In 82586 and 32-bit Segmented modes this address is represented as a base address plus the offset (this base address is also the base address of all the control blocks). In Linear mode the base address is also an absolute address. The 82596 clears BUSY, sets CX and CNR to equal 1 in the SCB, clears the SCB command word, sends an interrupt to the CPU, and awaits another Channel Attention signal. RESET configures the 82596 to its default state before CA is asserted.

CONTROLLING THE 82596DX/SX

The host CPU controls the 82596 with the commands, data structures, and methods described in this section. The CPU and the 82596 communicate through shared memory structures. The 82596 contains two independent units: the Command Unit and the Receive Unit. The Command Unit executes commands from the CPU, and the Receive Unit handles frame reception. These two units are controlled and monitored by the CPU through a shared memory structure called the System Control Block (SCB). The CPU and the 82596 use the CA and INT signals to communicate with the SCB.

82596 CPU ACCESS INTERFACE ($\overline{PORT}$)

The 82596 has a CPU access interface that allows the host CPU to do four things.

- Write an alternative System Configuration Pointer address.
- Write an alternative Dump area pointer and perform Dump.
- Execute a software reset.
- Execute a self-test.

The following events initiate the CPU access state.

- Presence of an address on the $D_{31}-D_4$ data bus pins.
- The D_3-D_0 pins are used to select one of the four functions.
- The $\overline{PORT}$ input pin is asserted, as in a regular write cycle.

NOTE

The SCP Dump and Self-Test addresses must be 16-byte aligned.

The 82596 requires two 16-bit write cycles for a port command. The first write holds the internal machines and reads the first 16 bits, the second activates the $\overline{PORT}$ command and reads the second 16 bits.

The $\overline{PORT}$ Reset is useful when only the 82596 needs to be reset. The CPU must wait for 10-system and 5-serial clocks before issuing another CA to the 82596; this new CA begins a new initialization process.

The Dump function is useful for troubleshooting No Response problems. If the chip is in a No Response state, the $\overline{PORT}$ Dump operation can be executed and a $\overline{PORT}$ Reset can be used to reinitialize the 82596 without disturbing the rest of the system.

The Self-Test function can be used for board testing; the 82596 will execute a self-test and write the results to memory.

Table 2. $\overline{PORT}$ Function Selection

	D_{31} ..... D_4						..... D_0
Function	**Addresses and Results**			D_3	D_2	D_1	D_0
Reset	A31	Don't Care	A4	0	0	0	0
Self-Test	A31	Self-Test Results Address	A4	0	0	0	1
SCP	A31	Alternative SCP Address	A4	0	0	1	0
Dump	A31	Dump Area Pointer	A4	0	0	1	1

MEMORY ADDRESSING FORMATS

The 82596 accesses memory by 32-bit addresses. There are two types of 32-bit addresses: linear and segmented. The type of address used depends on the 82596 operating mode and the type of memory structure it is addressing. The 82596 has three operating modes.

- 82586 Mode
  - A Linear address is a single 24-bit entity. Address pins $A_{31}-A_{24}$ are always zero.
  - A Segmented address uses a 24-bit base and a 16-bit offset.
- 32-bit Segmented Mode
  - A Linear address is a single 32-bit entity.
  - A Segmented address uses a 32-bit base and a 16-bit offset.

NOTE:
In the previous two memory addressing modes, each command header (CB, TBD, RFD, RBD, and SCB) must wholly reside within one segment. If the 82596 encounters a memory structure that does not follow this restriction, the 82596 will fetch the next contiguous location in memory (beyond the segment).

- Linear Mode
  - A Linear address is a single 32-bit entity.
  - There are no Segmented addresses.

Linear addresses are primarily used to address transmit and receive data buffers. In the 82586 and 32-bit Segmented modes, segmented addresses (base plus offset) are used for all Command Blocks, Buffer Descriptors, Frame Descriptors, and System Control Blocks. When using Segmented addresses, only the offset portion of the entity being addressed is specified in the block. The base for all offsets is the same—that of the SCB. See Table A.

LITTLE ENDIAN AND BIG ENDIAN BYTE ORDERING

The 82596 supports both Little Endian and Big Endian byte ordering for its memory structures.

The 82596A1 stepping supports Big Endian byte ordering for word and byte entities. Dword entities are not supported with 82596A1 Big Endian byte ordering. This results in slightly different 82596 memory structures for Big Endian operation. These structures are defined in the *32-Bit LAN Components A1 Manual.*

The 82596 B stepping supports Big Endian byte ordering for dword, word, and byte entities in Linear mode only. All 82596 B 32-bit address pointers are treated as 32-bit Big Endian entities, however, the SCB absolute address and statistical counters are treated as two 16-bit Big Endian entities. This 32-bit Big Endian entity support is configured via bit 7 in the SYSBUS byte.

The 82596 C-step has a New Enhanced Big Endian Mode where in Linear Addressing mode, true 32-bit Big Endian functionality is achieved. New Enhanced Big Endian Mode is enabled exactly the same as the B-step, by setting bit 7 of the SYSBUS byte. This mode is software compatible with the big endian mode of the B-step with one exception—no 32-bit addresses need to be swapped by software in the C-step. In this new mode, the 82596 C-step treats 32-bit address pointers as true 32-bit entities and the SCB absolute address and statistical counters are still treated as two 16-bit big endian entities. Not setting this mode will configure the 82596 C-step to be 100% compatible to the A1-step big endian mode.

NOTE:
All 82596 memory entities must be word or dword aligned, except the transmit buffers can be byte aligned for the 82596 B or C steppings.

An example of a double word entity is a frame descriptor command/status dword, whereas the raw data of the frame are byte entities. Both 32- and 16-bit buses are supported. When a 16-bit bus is used with Big Endian memory organization, data lines D_{15}–D_0 are used. The 82596 has an internal crossover that handles these swap operations.

COMMAND UNIT (CU)

The Command Unit is the logical unit that executes Action Commands from a list of commands very similar to a CPU program. A Command Block is associated with each Action Command. The CU is modeled as a logical machine that takes, at any given time, one of the following states.

- **Idle.** The CU is not executing a command and is not associated with a CB on the list. This is the initial state.
- **Suspended.** The CU is not executing a command; however, it is associated with a CB on the list. The suspend state can only be reached if the CPU forces it through the SCB or sets the suspend bit in the RFD.
- **Active.** The CU is executing an Action Command and pointing to its CB.

The CPU can affect CU operation in two ways: by issuing a CU Control Command or by setting bits in the Command word of the Action Command.

When programming the 82596 CU, it is important to consider the asynchronous way the 82596 processes commands. If a command is issued to the 82596 CU, it may be busy processing other commands. In order to avoid asynchronous race conditions, the following guidelines are recommended to the 82596 programmer:

- If the CU is already in the Active state, and another command needs to be executed, it is unwise to immediately issue another CU Start command. If a new command (or list of commands) needs to be started, first issue a CU Suspend command, wait for the CU to become Suspended, then issue the new CU Start. This will insure that all commands are processed correctly.
- In general, it is a good idea to make sure any CU command has been accepted and executed before issuing a new control command to the CU.

RECEIVE UNIT (RU)

The Receive Unit is the logical unit that receives frames and stores them in memory. The RU is modeled as a logical machine that takes, at any given time, one of the following states.

- **Idle.** The RU has no memory resources and is discarding incoming frames. This is the initial state.
- **No Resources.** The RU has no memory resources and is discarding incoming frames. This state differs from Idle in that the RU accumulates statistics on the number of discarded frames.
- **Suspended.** The RU has memory available for storing frames, but is discarding them. The suspend state can only be reached if the CPU forces it through the SCB or sets the suspend bit in the RFD.
- **Ready.** The RU has memory available and is storing incoming frames.

The CPU can affect RU operation in three ways: by issuing a RU Control Command, by setting bits in the Frame Descriptor Command word of the frame being received, or by setting the EL bit of the current buffer's Buffer Descriptor.

When programming the 82596 RU, it is important to consider the asynchronous way the 82596 processes receive frames. If an RU Start is issued to the 82596 RU, it may be busy processing other incoming packets. In order to avoid asynchronous race conditions, the following guidelines are recommended to the 82596 programmer:

- If the RU is already in the Ready state, and a new RFA is required to be started, it is unwise to immediately issue another RU Start command. If the new RFA needs to be started, first issue an RU Suspend command, wait for the RU to become Suspended, then issue the new RU Start. This will insure that all incoming frames are received correctly.
- In general, it is a good idea to make sure any RU command has been accepted and executed before issuing a new control command to the RU.

SYSTEM CONTROL BLOCK (SCB)

The SCB is a memory block that plays a major role in communications between the CPU and the 82596. Such communications include the following.

- Commands issued by the CPU
- Status reported by the 82596

Control commands are sent to the 82596 by writing them into the SCB and then asserting CA. The 82596 examines the command, performs the required action, and then clears the SCB command word. Control commands perform the following types of tasks.

- Operation of the Command Unit (CU). The SCB controls the CU by specifying the address of the Command Block List (CBL) and by starting, suspending, resuming, or aborting execution of CBL commands.

- Operation of the Bus Throttle. The SCB controls the Bus Throttle timers by providing them with new values and sending the Load and Start timer commands. The timers can be operated in both the 32-bit Segmented and Linear modes.
- Reception of frames by the Receive Unit (RU). The SCB controls the RU by specifying the address of the Receive Frame Area and by starting, suspending, resuming, or aborting frame reception.
- Acknowledgment of events that cause interrupts.
- Resetting the chip.

The 82596 sends status reports to the CPU via the System Control Block. The SCB contains four types of status reports.

- The cause of the current interrupts. These interrupts are caused by one or more of the following 82596 events.
  - The Command Unit completes an Action Command that has its I bit set.
  - The Receive Unit receives a frame.
  - The Command Unit becomes inactive.
  - The Receive Unit becomes not ready.
- The status of the Command Unit.
- The status of the Receive Unit.
- Status reports from the 82596 regarding reception of corrupted frames.

Events can be cleared only by CPU acknowledgment. If some events are not acknowledged by the ACK field the Interrupt signal (INT) will be reissued after Channel Attention (CA) is processed. Furthermore, if a new event occurs while an interrupt is set, the interrupt is temporarily cleared to trigger edge-triggered interrupt controllers.

The CPU uses the Channel Attention line to cause the 82596 to examine the SCB. This signal is trailing-edge triggered—the 82596 latches CA on the trailing edge. The latch is cleared by the 82596 before the SCB control command is read.

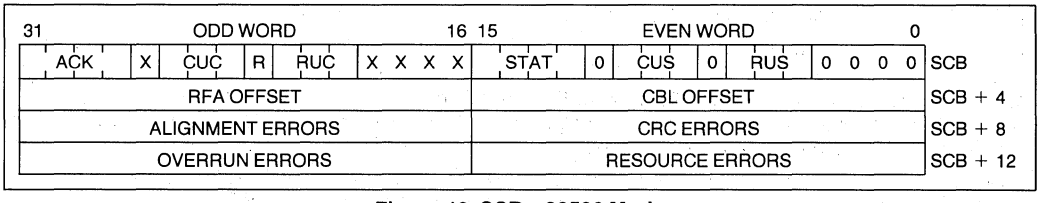


Figure 18. SCB—82586 Mode

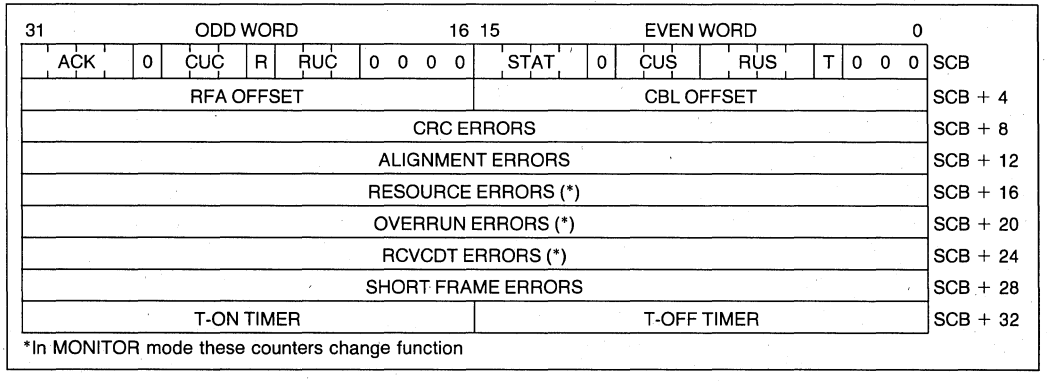


Figure 19. SCB—32-Bit Segmented Mode

31 ODD WORD 16	15 EVEN WORD 0	
ACK | 0 | CUC | R | RUC | 0 0 0 0 | STAT | 0 | CUS | RUS | T | 0 0 0		SCB
COMMAND BLOCK ADDRESS		SCB + 4
RECEIVE FRAME AREA ADDRESS		SCB + 8
CRC ERRORS		SCB + 12
ALIGNMENT ERRORS		SCB + 16
RESOURCE ERRORS (*)		SCB + 20
OVERRUN ERRORS (*)		SCB + 24
RCVCDT ERRORS (*)		SCB + 28
SHORT FRAME ERRORS		SCB + 32
T-ON TIMER	T-OFF TIMER	SCB + 36

*In MONITOR mode these counters change function

Figure 20. SCB—Linear Mode

Command Word

31	16	
ACK | 0 | CUC | R | RUC | 0 0 0 0		SCB + 2

These bits specifiy the action to be performed as a result of a CA. This word is set by the CPU and cleared by the 82596. Defined bits are:

Bit 31 ACK-CX — Acknowledges that the CU completed an Action Command.

Bit 30 ACK-FR — Acknowledges that the RU received a frame.

Bit 29 ACK-CNA — Acknowledges that the Command Unit became not active.

Bit 28 ACK-RNR — Acknowledges that the Receive Unit became not ready.

Bits 24–26 CUC — (3 bits) This field contains the command to the Command Unit. Valid values are:

0 — NOP (does not affect current state of the unit).

1 — Start execution of the first command on the CBL. If a command is executing, complete it before starting the new CBL. The beginning of the CBL is in CBL OFFSET (address).

2 — Resume the operation of the Command Unit by executing the next command. This operation assumes that the Command Unit has been previously suspended.

3 — Suspend execution of commands on CBL after current command is complete.

4 — Abort current command immediately.

5 — Loads the Bus Throttle timers so they will be initialized with their new values after the active timer (T-ON or T-OFF) reaches Terminal Count. If no timer is active new values will be loaded immediately. This command is not valid in 82586 mode.

6 — Loads and immediately restarts the Bus Throttle timers with their new values. This command is not valid in 82586 mode.

7 — Reserved.

Bits 20–22 RUC — (3 bits) This field contains the command to the Receive Unit. Valid values are:

0 — NOP (does not alter current state of unit).

1 — Start reception of frames. The beginning of the RFA is contained in the RFA OFFSET (address). If a frame is being received complete reception before starting.

2 — Resume frame reception (only when in suspended state).

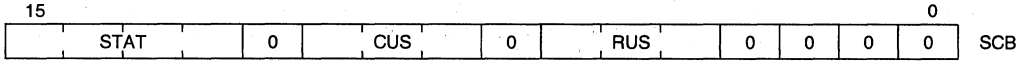
3 — Suspend frame reception. If a frame is being received complete its reception before suspending.

4 — Abort receiver operation immediately.

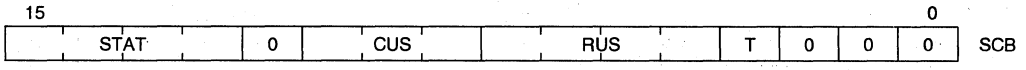
5–7 — Reserved.

Bit 23 RESET — Reset chip (logically the same as hardware RESET).

Status Word



82586 Mode



32-Bit Segmented and Linear Modes

Indicates the status of the 82596. This word is modified only by the 82596. Defined bits are:

Bit 15 CX — The CU finished executing a command with its I (interrupt) bit set.

Bit 14 FR — The RU finished receiving a frame.

Bit 13 CNA — The Command Unit left the Active state.

Bit 12 RNR — The Receive Unit left the Ready state.

Bits 8–10 CUS — (3 bits) This field contains the status of the command unit. Valid values are:

0 — Idle

1 — Suspended

2 — Active

3–7 — Not used

Bits 4–7 RUS — This field contains the status of the receive unit. Valid values are:

0h (0000) — Idle

1h (0001) — Suspended

2h (0010) — No resources. This bit indicates both no resources due to lack of RFDs in the RDL and no resources due to lack of RBDs in the FBL.

4h (0100) — Ready

Ah (1010) — No resources due to no more RBDs. (Not in the 82586 mode.)

Ch (1100) — No more RBDs (not in the 82586 mode).

No other combinations are allowed.

Bit 3 T — Bus Throttle timers loaded (not in 82586 mode).

SCB OFFSET ADDRESSES

CBL Offset (Address)

In 82586 and 32-bit Segmented modes this 16-bit quantity indicates the offset portion of the address for the first Command Block on the CBL. In Linear mode it is a 32-bit linear address for the first Command Block on the CBL. It is accessed only if CUC equals Start.

RFA Offset (Address)

In 82586 and 32-bit Segmented modes this 16-bit quantity indicates the offset portion of the address for the Receive Frame Area. In Linear mode it is a 32-bit linear address for the Receive Frame Area. It is accessed only if RUC equals Start.

SCB STATISTICAL COUNTERS

Statistical Counter Operation

- The CPU is responsible for clearing all error counters before initializing the 82596. The 82596 updates these counters by reading them, adding 1, and then writing them back to the SCB.
- The counters are wraparound counters. After reaching FFFFFFFFh the counters wrap around to zero.
- The 82596 updates the required counters for each frame. It is possible for more than one counter to be updated; multiple errors will result in all affected counters being updated.
- The 82596 executes the read-counter/increment/write-counter operation without relinquishing the bus (locked operation). This is to ensure that no logical contention exists between the 82596 and the CPU due to both attempting to write to the counters simultaneously. In the dual-port memory configuration the CPU should not execute any write operation to a counter if $\overline{LOCK}$ is asserted.
- The counters are 32-bits wide and their behavior is fully compatible with the IEEE 802.3 standard. The 82596 supports all relevant statistics (mandatory, optional, and desired) through the status of the transmit and receive header and directly through SCB statistics.

CRCERRS

This 32-bit quantity contains the number of aligned frames discarded because of a CRC error. This counter is updated, if needed, regardless of the RU state.

ALNERRS

This 32-bit quantity contains the number of frames that both are misaligned (i.e., where $\overline{CRS}$ deasserts on a nonoctet boundary) and contain a CRC error. The counter is updated, if needed, regardless of the RU state.

SHRTFRM

This 32-bit quantity contains the number of received frames shorter than the minimum frame length.

The last three counters change function in monitor mode.

RSCERRS

This 32-bit quantity contains the number of good frames discarded because there were no resources to contain them. Frames intended for a host whose RU is in the No Receive Resources state, fall into this category. This counter is updated only if the RU is in the No Resources state. When in Moniitor mode, this counter counts the total number of frames.

OVRNERRS

This 32-bit quantity contains the number of frames known to be lost because the local system bus was not available. If the traffic problem lasts longer than the duration of one frame, the frames that follow the first are lost without an indicator, and they are not counted. This counter is updated, if needed, regardless of the RU state.

RCVCDT

This 32-bit counter contains the number of collisions detected during frame reception. This counter will only be updated if at least 64 bytes of data are received before the collision occurs. If a collision occurs before 64 bytes of data are received, the frame is counted as a short frame. If the collisions occurs in the preamble, no counters are incremented.

ACTION COMMANDS AND OPERATING MODES

This section lists all the Action Commands of the Command Unit Command Block List (CBL). Each command contains the Command field, the Status and Control fields, the link to the next Action Command, and any command-specific parameters. There are three basic types of action commands: 82596 Configuration and Setup, Transmission, and Diagnostics. The following is a list of the actual commands.

- NOP
- Individual Address Setup
- Configure
- MC Setup
- Transmit
- TDR
- Dump
- Diagnose

The 82596 has three addressing modes. In the 82586 mode all the Action Commands look exactly like those of the 82586.

- **82586 Mode.** The 82596 software and memory structure is compatible with the 82586.
- **32-Bit Segmented Mode.** The 82596 can access the entire system memory and use the two new memory structures—Simplified and Flexible—while still using the segmented approach. This does not require any significant changes to existing software.
- **Linear Mode.** The 82596 operates in a flat, linear, 4 gigabyte memory space without segmentation. It can also use the two new memory structures.

In the 32-bit Segmented mode there are some differences between the 82596 and 82586 action commands, mainly in programming and activating new 82596 features. Those bits marked "don't care" in the compatible mode are not checked; however, we strongly recommend that those bits all be zeroes; this will allow future enchancements and extensions.

In the Linear mode all of the address offsets become 32-bit address pointers. All new 82596 features are accessible in this mode, and all bits previously marked "don't care" must be zeroes.

The Action Commands, and all other 82596 memory structures, must begin on even byte boundaries, i.e., they must be word aligned.

NOP

This command results in no action by the 82596 except for those performed in the normal command processing. It is used to manipulate the CBL manipulation. The format of the NOP command is shown in Figure 21.

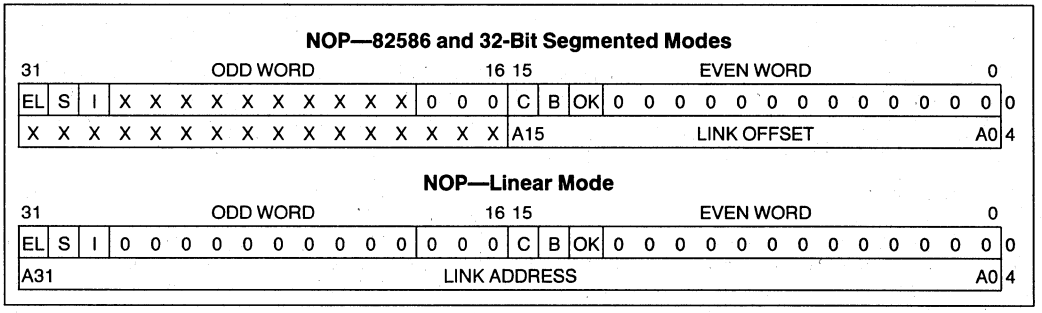


Figure 21

where:

LINK POINTER — In the 82586 or 32-bit Segmented modes this is a 16-bit offset to the next Command Block. In the Linear mode this is the 32-bit address of the next Command Block.

EL — If set, this bit indicates that this command block is the last on the CBL.

S — If set to one, suspend the CU upon completion of this CB.

I — If set to one, the 82596 will generate an interrupt after execution of the command is complete. If I is not set to one, the CX bit will not be set.

CMD (bits 16–18) — The NOP command. Value: 0h.

Bits 19–28 — Reserved (zero in the 32-bit Segmented and Linear modes).

C — This bit indicates the execution status of the command. The CPU initially resets it to zero when the Command Block is placed on the CBL. Following a command Completion, the 82596 will set it to one.

B — This bit indicates that the 82596 is currently executing the NOP command. It is initially reset to zero by the CPU. The 82596 sets it to one when execution begins and to zero when execution is completed. This bit is also set when the 82596 prefetches the command.

NOTE:

The C and B bits are modified in one operation.

OK — Indicates that the command was executed without error. If set to one no error occurred (command executed OK). If zero an error occur.

INDIVIDUAL ADDRESS SETUP

This command is used to load the 82596 with the Individual Address. This address is used by the 82596 for inserting the Source Address during transmission and recognizing the Destination Address during reception. After RESET, and prior to Individual Address Setup Command execution, the 82596 assumes the Broadcast Address is the Individual Address in all aspects, i.e.:

- This will be the Individual Address Match reference.
- This will be the Source Address of a transmitted frame (for AL-LOC = 0 mode only).

The format of the Individual Address Setup command is shown in Figure 22.

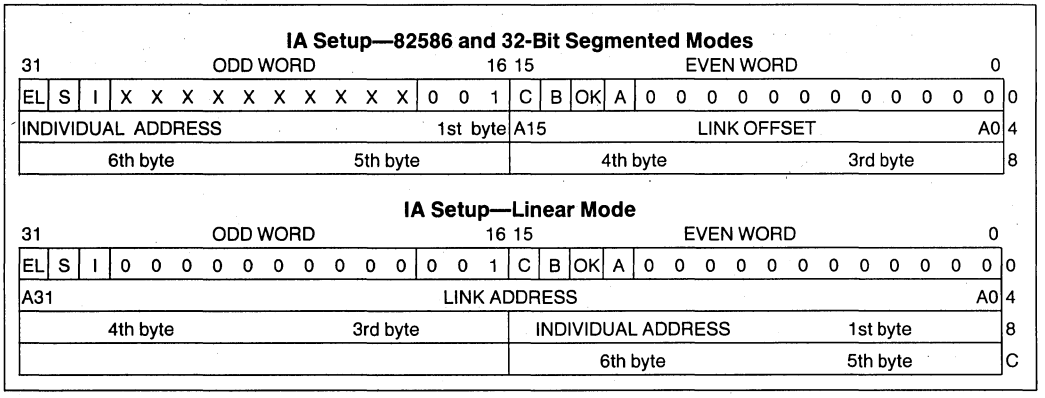


Figure 22

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted, and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (zero in the 32-bit Segmented and Linear modes).

CMD (bits 16–18) — The Address Setup command. Value: 1h.

INDIVIDUAL ADDRESS — The individual address of the node, 0 to 6 bytes long.

The least significant bit of the Individual Address must be zero for Ethernet (see the Command Structure). However, no enforcement of 0 is provided by the 82596. Thus, an Individual Address with 1 as its least significant bit is a valid Individual Address in all aspects.

The default address length is 6 bytes long, as in 802.3. If a different length is used the IA Setup command should be executed after the Configure command.

CONFIGURE

The Configure command loads the 82596 with its operating parameters. It allows changing some of the parameters by specifying a byte count less than the maximum number of configuration bytes (11 in the 82586 mode, 14 in the 32-Bit Segmented and Linear modes). The 82596 configuration depends on its mode of operation.

- In the 82586 mode the maximum number of configuration bytes is 12. Any number larger than 12 will be reduced to 12 and any number less than 4 will be increased to 4. When configuring the 12th byte (Byte 11 undefined) in 82586 mode this byte should be all ones.
- The additional features of the serial side are disabled in the 82586 mode.
- In both the 32-Bit Segmented and Linear modes there are four additional configuration bytes, which hold parameters for additional 82596 features. If these parameters are not accessed, the 82596 will follow their default values.
- For more detailed information refer to the *32-Bit LAN Components User's Manual.*

The format of the Configure command is shown in Figures 23, 24, and 25.

31 ODD WORD 16	15 EVEN WORD 0	
EL S I X X X X X X X X X X 0 1 0	C B OK A 0 0 0 0 0 0 0 0 0 0 0 0	0
Byte 1	Byte 0	4
A15 LINK OFFSET A0		4
Byte 5	Byte 4	8
Byte 3	Byte 2	8
Byte 9	Byte 8	12
Byte 7	Byte 6	12
X X X X X X X X X X X X X X X X	X X X X X X X X	16
	Byte 10	16

Figure 23. CONFIGURE—82586 Mode

31 ODD WORD 16	15 EVEN WORD 0	
EL S I 0 0 0 0 0 0 0 0 0 0 0 1 0	C B OK A 0 0 0 0 0 0 0 0 0 0 0 0	0
Byte 1	Byte 0	4
A15 LINK OFFSET A0		4
Byte 5	Byte 4	8
Byte 3	Byte 2	8
Byte 9	Byte 8	12
Byte 7	Byte 6	12
Byte 13	Byte 12	16
Byte 11	Byte10	16

Figure 24. CONFIGURE—32-Bit Segmented Mode

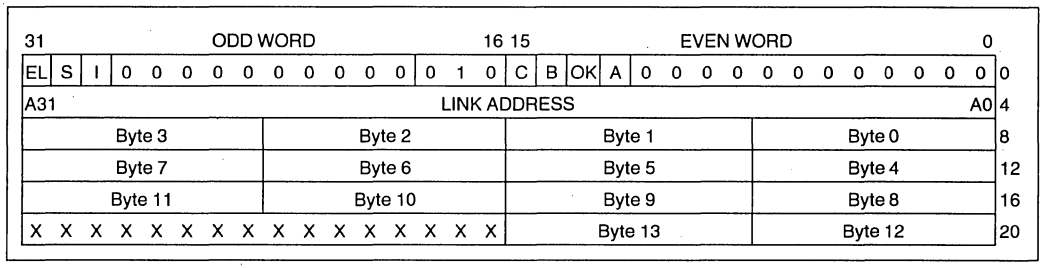


Figure 25. CONFIGURE—Linear Mode

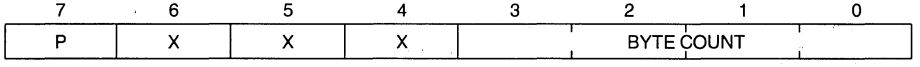
LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to a CU Abort control command. If 1, then the command was aborted and if necessary it should be repeated. If this bit is 0, the command was not aborted.

Bits 19–28 — Reserved (zero in the 32-Bit Segmented and Linear Modes)

CMD (bits 16–18) — The CONFIGURE command. Value: 2h.

The interpretation of the fields follows:

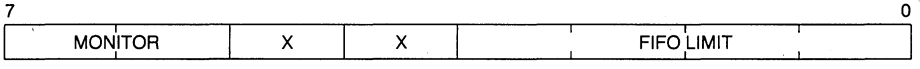


BYTE 0

BYTE CNT (Bits 0–3) — Byte Count. Number of bytes, including this one, that hold parameters to be configured.

PREFETCHED (Bit 7) — Enable the 82596 to write the prefetched bit in all prefetch RBDs.

NOTE:
The P bit is valid only in the new memory structure modes. In 82586 mode this bit is disabled (i.e., no prefetched mark).

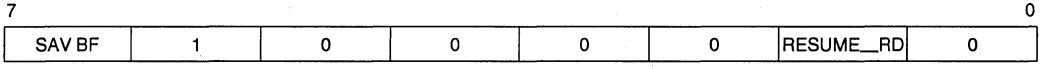


BYTE 1

FIFO Limit (Bits 0–3) — FIFO limit.

MONITOR# (Bits 6–7) — Receive monitor options. If the Byte Count of the configure command is less than 12 bytes then these Monitor bits are ignored.

DEFAULT: C8h



BYTE 2

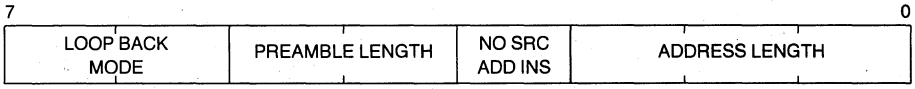
RESUME_RD (Bit 1) — 0— The 82596 does not reread the next CB on the list when a CU RESUME Control Command is issued.

1— The 82596 will reread the next CB on the list when a CU RESUME Control Command is issued. This is available only on the 82596B stepping.

SAV BF (Bit 7) — 0— Received bad frames are not saved in the memory.

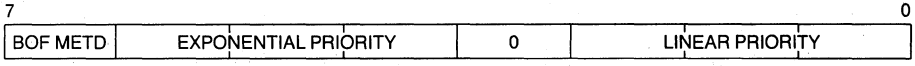
1— Received bad frames are saved in the memory.

DEFAULT: 40h



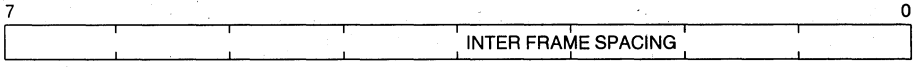
BYTE 3

ADR LEN (Bits 0–2)	Address length (any kind).
NO SCR ADD INS (Bit 3)	No Source Address Insertion. In the 82586 this bit is called AL LOC.
PREAM LEN (Bits 4–5)	Preamble length.
LP BCK MODE (Bits 6–7)	Loopback mode.
DEFAULT: 26h	



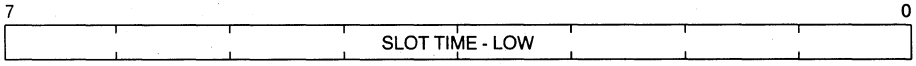
BYTE 4

LIN PRIO (Bits 0–2)	Linear Priority.
EXP PRIO (Bits 4–6)	Exponential Priority.
BOF METD (Bit 7)	Exponential Backoff method.
DEFAULT: 00h	



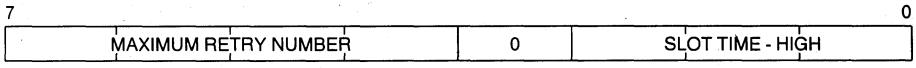
BYTE 5

INTERFRAME SPACING	Interframe spacing.
DEFAULT: 60h	



BYTE 6

SLOT TIME (L)	Slot time, low byte.
DEFAULT: 00h	



BYTE 7

SLOT TIME (H) (Bits 0–2)	Slot time, high part.
RETRY NUM (Bits 4–7)	Number of transmission retries on collision.
DEFAULT: F2h	

7							0
PAD	BIT STUFF	CRC16/ CRC32	NO CRC INSER	Tx ON NO CRS	MAN/ NRZ	BC DIS	PRM MODE

BYTE 8

PRM (Bit 0)	Promiscuous mode.
BC DIS (Bit 1)	Broadcast disable.
MANCH/NRZ (Bit 2)	Manchester or NRZ encoding. See specific timing requirements for TxC in Manchester mode.
TONO CRS (Bit 3)	Transmit on no CRS.
NOCRC INS (Bit 4)	No CRC insertion.
CRC-16/CRC-32 (Bit 5)	CRC type.
BIT STF (Bit 6)	Bit stuffing.
PAD (Bit 7)	Padding.
DEFAULT: 00h	

7			0
CDT SRC	COLLISION DETECT FILTER	CRS SRC	CARRIER SENSE FILTER

BYTE 9

CRSF (Bits 0–2)	Carrier Sense filter (length).
CRS SRC (Bit 3)	Carrier Sense source.
CDTF (Bits 4–6)	Collision Detect filter (length).
CDT SRC (Bit 7)	Collision Detect source.
DEFAULT: 00h	

7		0
MINIMUM FRAME LENGTH		

BYTE 10

MIN FRAME LEN	Minimum frame length.
DEFAULT: 40h	

7							0
MONITOR	MC_ALL	CDBSAC	AUTOTX	CRCINM	LNGFLD	PRECRS	

BYTE 11

PRECRS (Bit 0)	Preamble until Carrier Sense
LNGFLD (Bit 1)	Length field. Enables padding at the End-of-Carrier framing (802.3).
CRCINM (Bit 2)	Rx CRC appended to the frame in memory.
AUTOTX (Bit 3)	Auto retransmit.
CDBSAC (Bit 4)	Collision Detect by source address recognition.
MC_ALL (Bit 5)	Enable to receive all MC frames.
MONITOR (Bits 6–7)	Receive monitor options.
DEFAULT: FFH	

7							0
0	FDX	0	0	0	0	0	0

BYTE 12

FDX (Bit 6) Enables Full Duplex operation.

DEFAULT: 00h

7							0
DIS_BOF	MULT_IA	1	1	1	1	1	1

BYTE 13

MULT_IA (Bit 6) Multiple individual address.

DIS_BOF (Bit 7) Disable the backoff algorithm.

DEFAULT: 3Fh

A reset (hardware or software) configures the 82596 according to the following defaults.

Table 4. Configuration Defaults

	Parameter	Default Value	Units/Meaning
	ADDRESS LENGTH	**6	Bytes
	A/L FIELD LOCATION	0	Located in FD
*	AUTO RETRANSMIT	1	Auto Retransmit Enable
	BITSTUFFING/EOC	0	EOC
	BROADCAST DISABLE	0	Broadcast Reception Enabled
*	CDBSAC	1	Disabled
	CDT FILTER	0	Bit Times
	CDT SRC	0	External Collision Detection
*	CRC IN MEMORY	1	CRC Not Transferred to Memory
	CRC-16/CRC-32	**0	CRC-32
	CRS FILTER	0	0 Bit Times
	CRS SRC	0	External CRS
*	DISBOF	0	Backoff Enabled
	EXT LOOPBACK	0	Disabled
	EXPONENTIAL PRIORITY	**0	802.3 Algorithm
	EXPONENTIAL BACKOFF METHOD	**0	802.3 Algorithm
*	FULL DUPLEX (FDX)	0	CSMA/CD Protocol (No FDX)
	FIFO THRESHOLD	8	TX: 32 Bytes, RX: 64 Bytes
	INT LOOPBACK	0	Disabled
	INTERFRAME SPACING	**96	Bit Times
	LINEAR PRIORITY	**0	802.3 Algorithm
*	LENGTH FIELD	1	Padding Disabled
	MIN FRAME LENGTH	**64	Bytes
*	MC ALL	1	Disabled
*	MONITOR	11	Disabled
	MANCHESTER/NRZ	0	NRZ
*	MULTI IA	0	Disabled
	NUMBER OF RETRIES	**15	Maximum Number of Retries
	NO CRC INSERTION	0	CRC Appended to Frame
	PREFETCH BIT IN RBD	0	Disabled (Valid Only in New Modes)
	PREAMBLE LENGTH	**7	Bytes
*	Preamble Until CRS	1	Disabled
	PROMISCUOUS MODE	0	Address Filter On
	PADDING	0	No Padding
	SLOT TIME	**512	Bit Times
	SAVE BAD FRAME	0	Discards Bad Frames
	TRANSMIT ON NO CRS	0	Disabled

NOTES:
1. This configuration setup is compatible with the IEEE 802.3 specification.
2. The Asterisk "*" signifies a new configuration parameter not available in the 82586.
3. The default value of the Auto retransmit configuration parameter is enabled (1).
4. Double Asterisk "**" signifies IEEE 802.3 requirements.

MULTICAST-SETUP

This command is used to load the 82596 with the Multicast-IDs that should be accepted. As noted previously, the filtering done on the Multicast-IDs is not perfect and some unwanted frames may be accepted. This command resets the current filter and reloads it with the specified Multicast-IDs. The format of the Multicast-addresses setup command is:

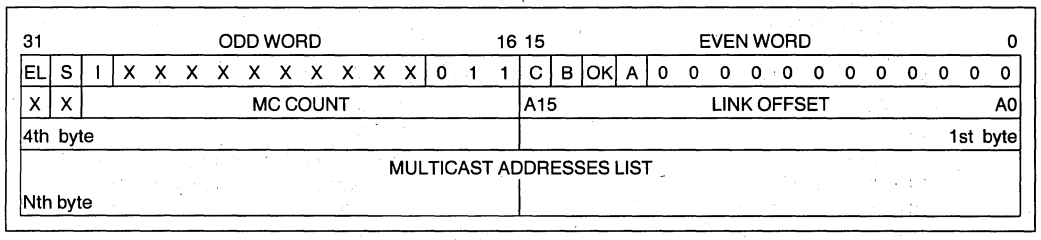


Figure 26. MC Setup—82586 and 32-Bit Segmented Modes

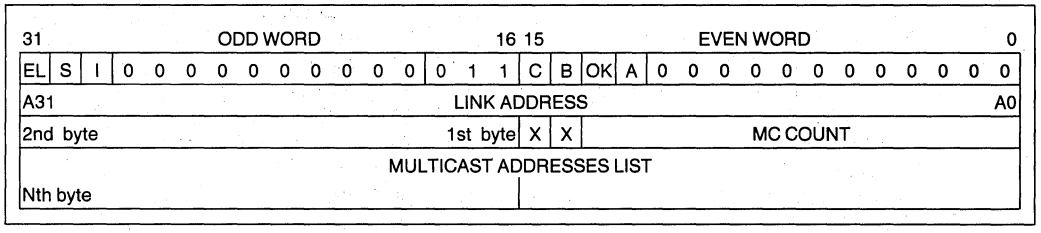


Figure 27. MC Setup—Linear Mode

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to a CU Abort control command. If one, then the command was aborted and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (0 in both the 32-Bit Segmented and Linear Modes).

CMD (bits 16–18) — The MC SETUP command value: 3h.

MC-CNT — This 14-bit field indicates the number of bytes in the MC LIST field. The MC CNT must be a multiple of the ADDR LEN; otherwise, the 82596 reduces the MC CNT to the nearest ADDR LEN multiple. MC CNT = 0 implies resetting the Hash table which is equivalent to disabling the Multicast filtering mechanism.

MC LIST — A list of Multicast Addresses to be accepted by the 82596. The least significant bit of each MC address must be 1.

NOTE:

The list is sequential; i.e., the most significant byte of an address is immediately followed by the least significant byte of the next address.

— When the 82596 is configured to recognize multiple Individual Address (Multi-IA), the MC-Setup command is also used to set up the Hash table for the individual address.

The least significant bit in the first byte of each IA address must be 0.

TRANSMIT

This command is used to transmit a frame of user data onto the serial link. The format of a Transmit command is as follows.

31 ODD WORD 16	15 EVEN WORD 0	
EL S I X X X X X X X X X X 1 0 0	C B STATUS BITS MAXCOLL	0
A15 TBD OFFSET A0	A15 LINK OFFSET A0	4
4th byte	DESTINATION ADDRESS 1st byte	8
LENGTH FIELD	6th byte	12

Figure 28. TRANSMIT—82586 Mode

31 ODD WORD 16	15 EVEN WORD 0	
EL S I 0 0 0 0 0 0 0 0 NC SF 1 0 0	C B STATUS BITS MAXCOLL	0
A15 TBD OFFSET A0	A15 LINK OFFSET A0	4
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	EOF 0 TCB COUNT	8
4th byte	DESTINATION ADDRESS 1st byte	12
LENGTH FIELD	6th byte	16
OPTIONAL DATA		

Figure 29. TRANSMIT—32-Bit Segmented Mode

31 ODD WORD 16	15 EVEN WORD 0	
EL S I 0 0 0 0 0 0 0 0 NC SF 1 0 0	C B STATUS BITS MAXCOLL	0
A31 LINK ADDRESS A0		4
A31 TRANSMIT BUFFER DESCRIPTOR ADDRESS A0		8
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	EOF 0 TCB COUNT	12
4th byte	DESTINATION ADDRESS 1st byte	16
20 LENGTH FIELD	6th byte	
OPTIONAL DATA		

Figure 30. TRANSMIT—Linear Mode

31 COMMAND WORD 16	
EL S I 0 0 0 0 0 0 0 0 NC SF 1 0 0	2

NC:
- 0: No CRC Insertion disable; when the configure command is configured to not insert the CRC during transmission the NC has no effect.
- 1: No CRC Insertion enable; when the configure command is configured to insert the CRC during transmission the CRC will not be inserted when NC = 1.

SF:
- 0: Simplified Mode, all the Tx data is in the Transmit Command Block. The Transmit Buffer Descriptor Address field is all 1s.
- 1: Flexible Mode. Data is in the TCB and in a linked list of TBDs.

where:

EL, B, C, I, S	— As per standard Command Block (see the NOP command for details).
OK (Bit 13)	— Error free completion.
A (Bit 12)	— Indicates that the command was abnormally terminated due to CU Abort control command. If 1, then the command was aborted, and if necessary it should be repeated. If this bit is 0, the command was not aborted.
Bits 19–28	— Reserved (0 in the 32-bit Segmented and Linear modes).
CMD (Bits 16–18)	— The transmit command: 4h.
Status Bit 11	— Late collision. A late collision (a collision after the slot time is elapsed) is detected.
Status Bit 10	— No Carrier Sense signal during transmission. Carrier Sense signal is monitored from the end of Preamble transmission until the end of the Frame Check Sequence for TONOCRS = 1 (Transmit On No Carrier Sense mode) it indicates that transmission has been executed despite a lack of CRS. For TONOCRS = 0 (Ethernet mode), this bit also indicates unsuccessful transmission (transmission stopped when lack of Carrier Sense has been detected).
Status Bit 9	— Transmission unsuccessful (stopped) due to Loss of $\overline{\text{CTS}}$.
Status Bit 8	— Transmission unsuccessful (stopped) due to DMA Underrun; i.e., the system did not supply data for transmission.
Status Bit 7	— Transmission Deferred, i.e., transmission was not immediate due to previous link activity.
Status Bit 6	— Heartbeat Indicator, Indicates that after a previously performed transmission, and before the most recently performed transmission, (Interframe Spacing) the CDT signal was monitored as active. This indicates that the Ethernet Transceiver Collision Detect logic is performing properly. The Heartbeat is monitored during the Interframe Spacing period.
Status Bit 5	— Transmission attempt was stopped because the number of collisions exceeded the maximum allowable number of retries.
Status Bit 4	— 0 (Reserved).
MAX-COL (Bits 3–0)	— The number of Collisions experienced during this frame. Max Col = 0 plus S5 = 1 indicates 16 collisions.
LINK OFFSET	— As per standard Command Block (see the NOP for details).
TBD POINTER	— In the 82586 and 32-bit Segmented modes this is the offset of the first Tx Buffer Descriptor containing the data to be transmitted. In the Linear mode this is the 32-bit address of the first Tx Buffer Descriptor on the list. If the TBD POINTER is all 1s it indicates that no TBD is used.
DEST ADDRESS	— Contains the Destination Address of the frame. The least significant bit (MC) indicates the address type. MC = 0: Individual Address. MC = 1: Multicast or Broadcast Address. If the Destination Address bits are all 1s this is a Broadcast Address.
LENGTH FIELD	— The contents of this 2-byte field are user defined. In 802.3 it contains the length of the data field. It is placed in memory in the same order it is transmitted; i.e., most significant byte first, least significant byte second.
TCB COUNT	— This 14-bit counter indicates the number of bytes that will be transmitted from the Transmit Command Block, starting from the third byte after the TCB COUNT field (address $n+12$ in the 32-bit Segmented mode, $N+16$ in the Linear mode). The TCB COUNT field can be any number of bytes (including an odd byte), this allows the user to transmit a frame with a header having an odd number of bytes. The TCB COUNT field is not used in the 82586 mode.
EOF Bit	— Indicates that the whole frame is kept in the Transmit Command Block. In the Simplified memory model it must be always asserted.

The interpretation of what is transmitted depends on the No Source Address insertion configuration bit and the memory model being used.

NOTES

1. The Destination Address and the Length Field are sequential of the Length Field immediately follows the most significant byte of the Destination Address.
2. In case the 82596 is configured with No Source Address insertion bit equal to 0, the 82596 inserts its configured Source Address in the transmitted frame.

- In the 82586 mode, or when the Simplified memory model is used, the Destination and Length fields of the transmitted frame are taken from the Transmit Command Block.
- If the FLEXIBLE memory model is used, the Destination and Length fields of the transmitted frame can be found either in the TCB or TBD, depending on the TCB COUNT.

3. If the 82596 is configured with the Address/Length Field Location equal to 1, the 82596 does not insert its configured Source Address in the transmitted frame. The first (2 × Address Length) + 2 bytes of the transmitted frame are interpreted as Destination Address, Source Address, and Length fields respectively. The location of the first transmitted byte depends on the operational mode of the 82596:

- In the 82586 mode, it is always the first byte of the first Tx Buffer.
- In both the 32-bit Segmented and Linear modes it depends on the SF bit and TCB COUNT:
  - — In the Simplified memory mode the first transmitted byte is always the third byte after the TCB COUNT field.
  - — In the Flexible mode, if the TCB COUNT is greater than 0 then it is the third byte after the TCB COUNT field. If TCB COUNT equals 0 then it is first byte of the first Tx Buffer.
- Transmit frames shorter than six bytes are invalid. The transmission will be aborted (only in 82586 mode) because of a DMA Underrun.

4. Frames which are aborted during transmission are jammed. Such an interruption of transmission can be caused by any reason indicated by any of the status bits 8, 9, 10 and 12.

JAMMING RULES

1. Jamming will not start before completion of preamble transmission.
2. Collisions detected during transmission of the last 11 bits will not result in jamming.

The format of a Transmit Buffer Descriptor is:

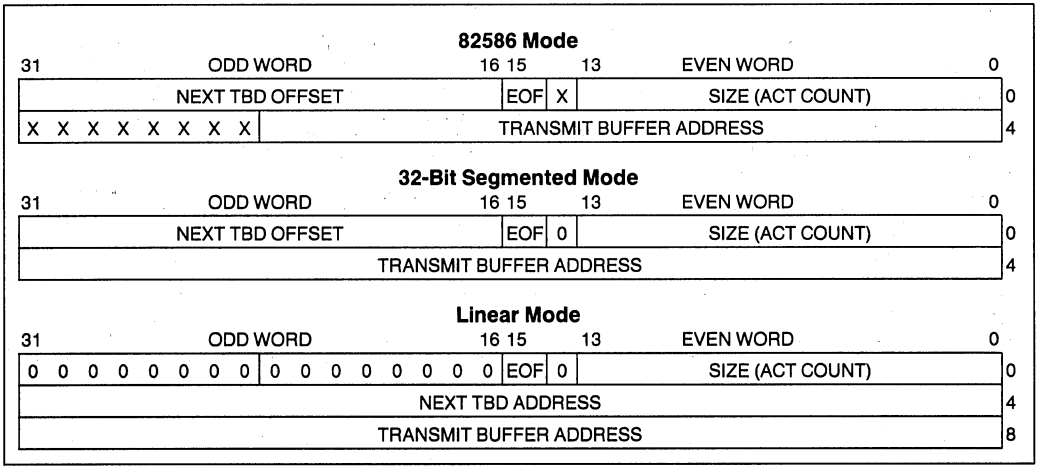


Figure 31

where:

EOF — This bit indicates that this TBD is the last one associated with the frame being transmitted. It is set by the CPU before transmit.

SIZE (ACT COUNT) — This 14-bit quantity specifies the number of bytes that hold information for the current buffer. It is set by the CPU before transmission.

NEXT TBD ADDRESS — In the 82586 and 32-bit Segmented modes, it is the offset of the next TBD on the list. In the Linear mode this is the 32-bit address of the next TBD on the list. It is meaningless if EOF = 1.

BUFFER ADDRESS — The starting address of the memory area that contains the data to be sent. In the 82586 mode, this is a 24-bit address (A31–A24 are considered to be zero). In the 32-bit Segmented and Linear modes this is a 32-bit address. This buffer can be byte aligned for the 82596 B-step.

TDR

This operation activates Time Domain Reflectometry, which is a mechanism to detect open or short circuits on the link and their distance from the diagnosing station. The TDR command has no parameters. The TDR transmit sequence was changed, compared to the 82586, to form a regular transmission. The TDR command is designed to be used statically. Make sure that both the CU and RU are idle before attempting a TDR command. The TDR bit stream is as follows.

— Preamble
— Source address
— Another Source address (the TDR frame is transmitted back to the sending station, so DEST ADR = SRC ADR).
— Data field containing 7Eh patterns.
— Jam Pattern, which is the inverse CRC of the transmitted frame.

Maximum length of the TDR frame is 2048 bits. If the 82596 senses collision while transmitting the TDR frame it transmits the jam pattern and stops the transmission. The 82596 then triggers an internal timer (STC); the timer is reset at the beginning of transmission and reset if CRS is returned. The timer measures the time elapsed from the start of transmission until an echo is returned. The echo is indicated by Collision Detect going active or a drop in the Carrier Sense signal. The following table lists the possible cases that the 82596 is able to analyze.

Conditions of TDR as Interpreted by the 82596

Transceiver Type / Condition	Ethernet	Non Ethernet
Carrier Sense was inactive for 2048-bit-time periods	Short or Open on the Transceiver Cable	NA
Carrier Sense signal dropped	Short on the Ethernet cable	NA
Collision Detect went active	Open on the Ethernet cable	Open on the Serial Link
The Carrier Sense Signal did not drop or the Collision Detect did not go active within 2048-bit time period	No Problem	No Problem

An Ethernet transceiver is defined as one that returns transmitted data on the receive pair and activates the Carrier Sense Signal while transmitting. A Non-Ethernet Transceiver is defined as one that does not do so.

The format of the Time Domain Reflectometer command is:

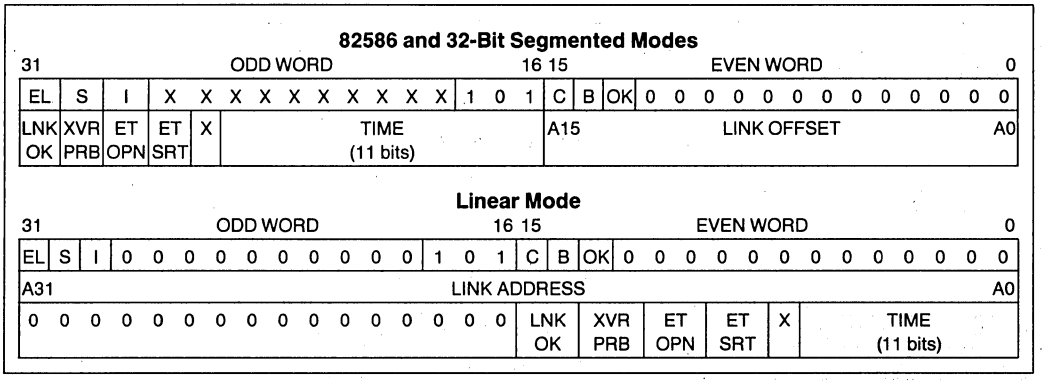


Figure 32. TDR

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details).

A — Indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted, and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (0 in the 32-bit Segmented and Linear Modes).

CMD (Bits 16–18) — The TDR command. Value: 5h.

TIME — An 11-bit field that specifies the number of TxC cycles that elapsed before an echo was observed. No echo is indicated by a reception consisting of "1s" only. Because the network contains various elements such as transceiver links, transceivers, Ethernet, repeaters etc., the TIME is not exactly proportional to the problems distance.

LNK OK (Bit 15) — No link problem identified. TIME = 7FFh.

XCVR PRB (Bit 14) — Indicates a Transceiver problem. Carrier Sense was inactive for 2048-bit time period. LNK OK = 0. TIME = 7FFh.

ET OPN (Bit 13) — The transmission line is not properly terminated. Collision Detect went active and LNK OK = 0.

ET SRT (Bit 12) — There is a short circuit on the transmission line. Carrier Sense Signal dropped and LNK OK = 0.

DUMP

This command causes the contents of various 82596 registers to be placed in a memory area specified by the user. It is supplied as a 82596 self-diagnostic tool, and to provide registers of interest to the user. The format of the DUMP command is:

82586 and 32-Bit Segmented Modes

31			ODD WORD									16	15				EVEN WORD										0
EL	S	I	X	X	X	X	X	X	X	X	X	1	1	0	C	B	OK	0	0	0	0	0	0	0	0	0	0	0
A15			BUFFER OFFSET											A0	A15			LINK OFFSET										A0

Linear Mode

31			ODD WORD									16	15				EVEN WORD										0
EL	S	I	X	X	X	X	X	X	X	X	X	1	1	0	C	B	OK	0	0	0	0	0	0	0	0	0	0	0
A31			LINK ADDRESS																								A0
A31			BUFFER ADDRESS																								A0

Figure 33. Dump

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details).

OK — Indicates error free completion.

Bits 19–28 — Reserved (0 in the 32-bit Segmented and Linear Modes).

CMD (Bits 16–18) — The Dump command. Value: 6h.

BUFFER POINTER — In the 82586 and 32-bit Segmented modes this is the 16-bit-offset portion of the dump area address. In the Linear mode this is the 32-bit linear address of the dump area.

Dump Area Information Format

- The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586. The compatible data will be marked with an asterisk.
- In 82586 mode the dump area is 170 bytes.
- The dump area format of the 32-bit Segmented and Linear modes is described in Figure 35.
- The size of the dump area of the 32-bit Segmented and Linear modes is 304 bytes.
- When the dump is executed by the Port command an extra word will be appended to the Dump Area. The extra word is a copy of the Dump Area status word (containing the *C, B,* and *OK* bits). The *C* and *OK* bits are set when the 82596 has completed the Port Dump command.

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
DMA CONTROL REGISTER*	00
CONFIGURE BYTES 3, 2	02
CONFIGURE BYTES 5, 4	04
CONFIGURE BYTES 7, 6	06
CONFIGURE BYTES 9, 8	08
CONFIGURE BYTES 10	0A
I.A. BYTES 1, 0*	0C
I.A. BYTES 3, 2*	0E
I.A. BYTES 5, 4*	10
LAST T.X. STATUS*	12
T.X. CRC BYTES 1, 0*	14
T.X. CRC BYTES 3, 2*	16
R.X. CRC BYTES 1, 0*	18
R.X. CRC BYTES 3, 2*	1A
R.X. TEMP MEMORY 1, 0*	1C
R.X. TEMP MEMORY 3, 2*	1E
R.X. TEMP MEMORY 5, 4*	20
LAST RECEIVED STATUS*	22
HASH REGISTER BYTES 1, 0*	24
HASH REGISTER BYTES 3, 2*	26
HASH REGISTER BYTES 5, 4*	28
HASH REGISTER BYTES 7, 6*	2A
SLOT TIME COUNTER*	2C
WAIT TIME COUNTER*	2E
MICRO MACHINE**	30
REGISTER FILE	.
60 BYTES	6A
MICRO MACHINE LFSR**	6C
MICRO MACHINE	6E
FLAG ARRAY	.
14 BYTES	7A
QUEUE MEMORY**	7C
CU PORT	.
8 BYTES	82
MICRO MACHINE ALU**	84
RESERVED**	86
M.M. TEMP A ROTATE R**	88
M.M. TEMP A**	8A
T.X. DMA BYTE COUNT**	8C
M.M. INPUT PORT ADDRESS**	8E
T.X. DMA ADDRESS**	90
M.M. OUTPUT PORT**	92
R.X. DMA BYTE COUNT**	94
M.M. OUTPUT PORT ADDRESS REGISTER**	96
R.X. DMA ADDRESS**	98
RESERVED**	9A
BUS THROTTLE TIMERS	9C
DIU CONTROL REGISTER**	9E
RESERVED**	A0
DMA CONTROL REGISTER**	A2
BIU CONTROL REGISTER**	A4
M.M. DISPATCHER REGISTER**	A6
M.M. STATUS REGISTER**	A8

NOTE:
*The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586. The compatible data will be marked with an asterisk.
**These bytes are not user defined, results may vary from Dump command to Dump command.

Figure 34. Dump Area Format—82586 Mode

31	0	
CONFIGURE BYTES 5, 4, 3, 2		00
CONFIGURE BYTES 9, 8, 7, 6		04
CONFIGURE BYTES 13, 12, 11, 10		08
I.A. BYTES 1, 0	X X X X X X X X	0C
I.A. BYTES 5, 2		10
TX CRC BYTES 0, 1	LAST T.X. STATUS	14
RX CRC BYTES 0, 1	TX CRC BYTES 3, 2	18
RX TEMP MEMORY 1, 0	RX CRC BYTES 3, 2	1C
R.X. TEMP MEMORY 5, 2		20
HASH REGISTERS 1, 0	LAST R.X. STATUS	24
HASH REGISTER BYTES 5, 2		28
SLOT TIME COUNTER	HASH REGISTERS 7, 6	2C
RECEIVE FRAME LENGTH	WAIT-TIME COUNTER	30
MICRO MACHINE** REGISTER FILE 128 BYTES		34 . . . B0
MICRO MACHINE LFSR**		B4
MICRO MACHINE** FLAG ARRAY 28 BYTES		B8 . . . D0
M.M. INPUT PORT** 16 BYTES		D4 E0
MICRO MACHINE ALU**		E4
RESERVED**		E8
M.M. TEMP A ROTATE R.**		EC
M.M. TEMP A**		F0
T.X. DMA BYTE COUNT**		F4
M.M. INPUT PORT ADDRESS REGISTER**		F8
T.X. DMA ADDRESS**		FC
M.M. OUTPUT PORT REGISTER**		100
R.X. DMA BYTE COUNT**		104
M.M. OUTPUT PORT ADDRESS REGISTER**		108
R.X. DMA ADDRESS REGISTER**		10C
RESERVED**		110
BUS THROTTLE TIMERS		114
DIU CONTROL REGISTER**		118
RESERVED**		11C
DMA CONTROL REGISTER**		120
BIU CONTROL REGISTER**		124
M.M. DISPATCHER REG.**		128
M.M. STATUS REGISTER**		12C

NOTE:
The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586. The compatible data will be marked with an asterisk.
**These bytes are not user defined, results may vary from Dump command to Dump command.

Figure 35. Dump Area Format—Linear and 32-Bit Segmented Mode

DIAGNOSE

The Diagnose Command triggers an internal self-test procedure that checks internal 82596 hardware, which includes:

- Exponential Backoff Random Number Generator (Linear Feedback Shift Register).
- Exponential Backoff Timeout Counter.
- Slot Time Period Counter.
- Collision Number Counter.
- Exponential Backoff Shift Register.
- Exponential Backoff Mask Logic.
- Timer Trigger Logic.

This procedure checks the operation of the Backoff block, which resides in the serial side and is not easily controlled. The Diagnose command is performed in two phases.

The format of the 82596 Diagnose command is:

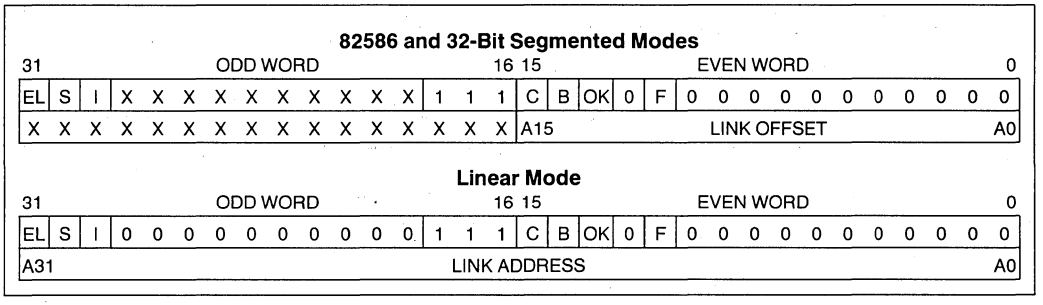


Figure 36. Diagnose

where:

LINK ADDRESS, EL, B, C, I, S	— As per standard Command Block (see the NOP command for details).
Bits 19–28	— Reserved (0 in the 32-bit Segmented and Linear Modes).
CMD (bits 16–18)	— The Diagnose command. Value: 7h.
OK (bit 13)	— Indicates error free completion.
F (bit 11)	— Indicates that the self-test procedure has failed.

RECEIVE FRAME DESCRIPTOR

Each received frame is described by one Receive Frame Descriptor (see Figure 37). Two new memory structures are available for the received frames. The structures are available only in the Linear and 32-bit Segmented modes.

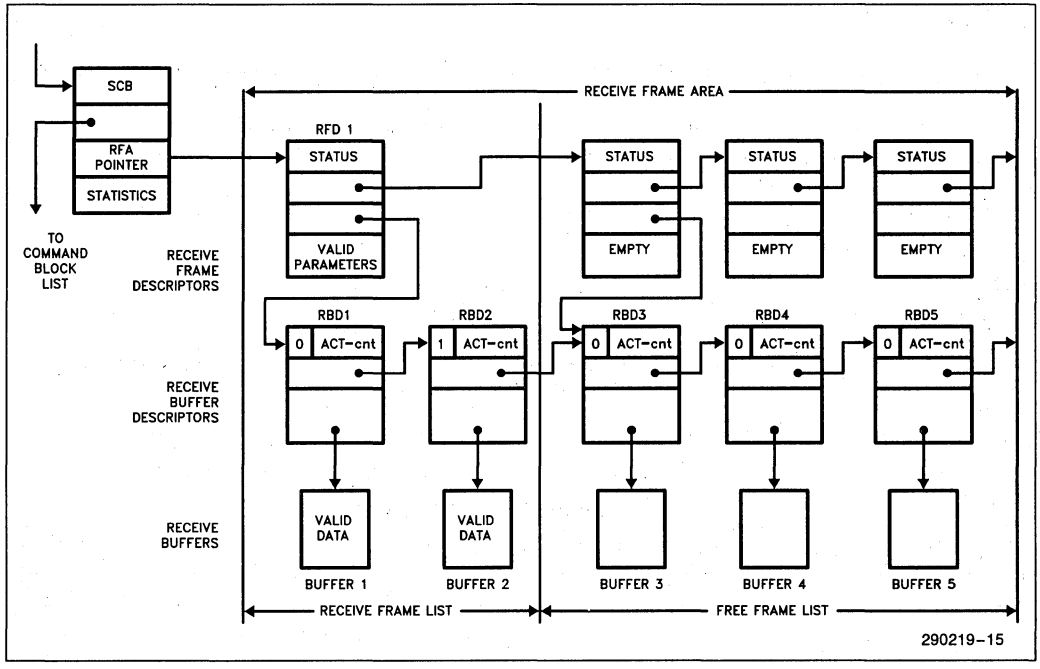


Figure 37. The Receive Frame Area

Simplified Memory Structure

The first is the Simplified memory structure, the data section of the received frame is part of the RFD and is located immediately after the Length Field. Receive Buffer Descriptors are not used with the Simplified structure, it is primarily used to make programming easier. If the length of the data area described in the Size Field is smaller than the incoming frame, the following happens.

1. The received frame is truncated.
2. The No Resource error counter is updated.
3. If the 82596 is configured to Save Bad Frames the RFD is not reused; otherwise, the same RFD is used to hold the next received frame, and the only action taken regarding the truncated frame is to update the counter.
4. The 82596 continues to receive the next frame in the next RFD.

Note that this sequence is very useful for monitoring. If the 82596 is configured to Save Bad Frames, to receive in Promiscuous mode, and to use the Simplified memory structure, any programmed length of received data can be saved in memory.

The Simplified memory structure is shown in Figure 38.

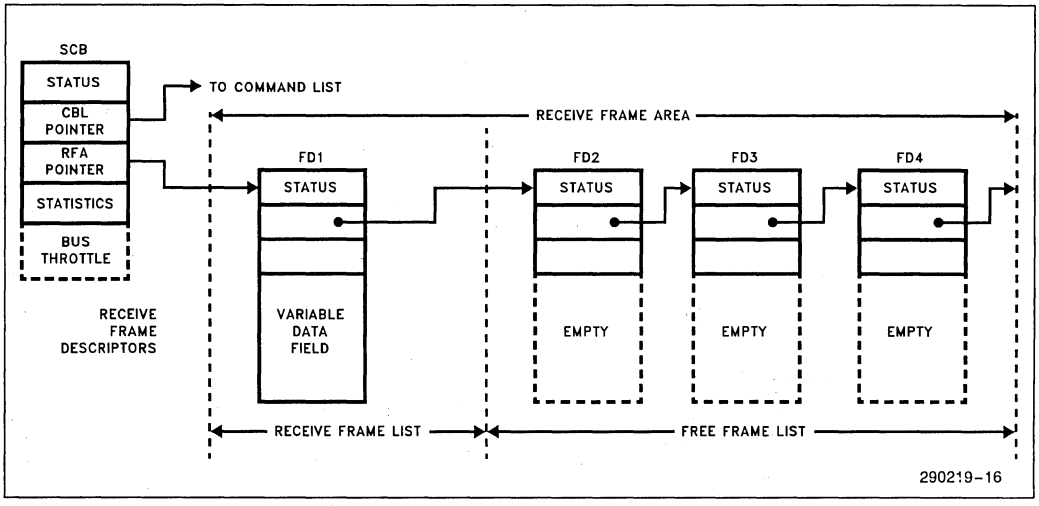


Figure 38. RFA Simplified Memory Structure

Flexible Memory Structure

The second structure is the Flexible memory structure, the data structure of the received frame is stored in both the RFD and in a linked list of Receive Buffers—Receive Buffer Descriptors. The received frame is placed in the RFD as configured in the Size field. Any remaining data is placed in a linked list of RBDs.

The Flexible memory structure is shown in Figure 39.

Buffers on the receive side can be different lengths. The 82596 will not place more bytes into a buffer than indicated in the associated RBD. The 82596 will fetch the next RBD before it is needed. The 82596 will attempt to receive frames as long as the FBL is not exhausted. If there are no more buffers, the 82596 Receive Unit will enter the No Resources state. Before starting the RU, the CPU must place the FBL pointer in the RBD pointer field of the first RFD. All remaining RBD pointer fields for subsequent RFDs should be "1s." If the Receive Frame Descriptor and the associated Receive Buffers are not reused (e.g., the frame is properly received or the 82596 is configured to Save Bad Frames), the 82596 writes the address of the next free RBD to the RBD pointer field of the next RFD.

RECEIVE BUFFER DESCRIPTOR (RBD)

The RBDs are used to store received data in a flexible set of linked buffers. The portion of the frame's data field that is outside the RFD is placed in a set of buffers chained by a sequence of RBDs. The RFD points to the first RBD, and the last RBD is flagged with an EOF bit set to 1. Each buffer in the linked list of buffers related to a particular frame can be any size up to 2^{14} bytes but must be word aligned (begin on an even numbered byte). This ensures optimum use of the memory resources while maintaining low overhead. All buffers in a frame are filled with the received data except for the last, in which the actual count can be smaller than the allocated buffer space.

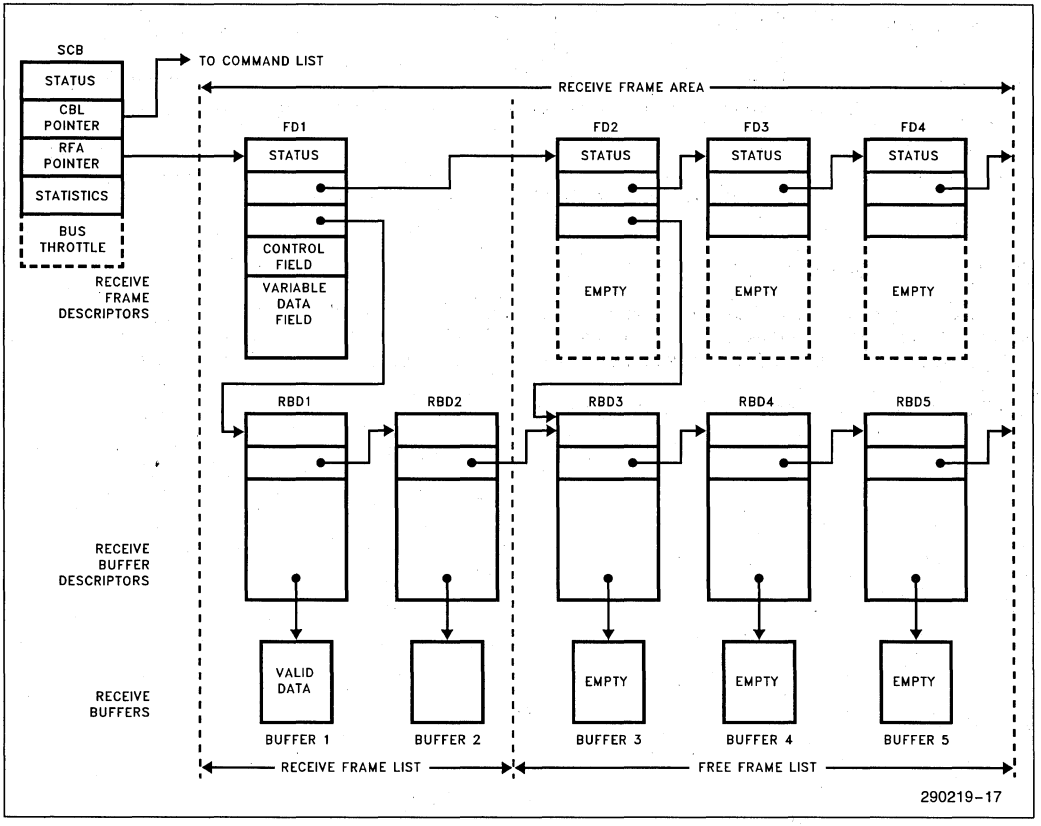


Figure 39. RFA Flexible Memory Structure

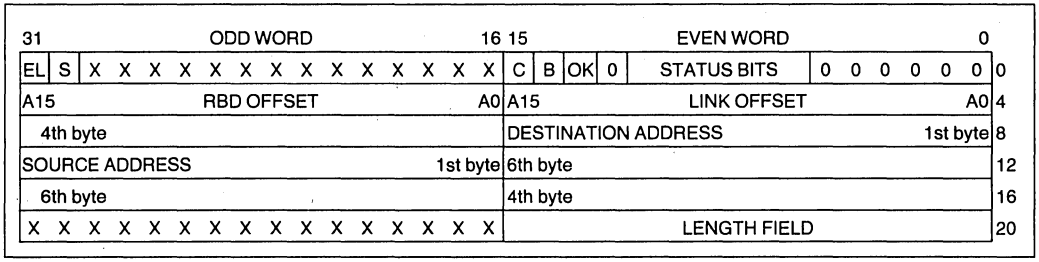


Figure 40. Receive Frame Descriptor—82586 Mode

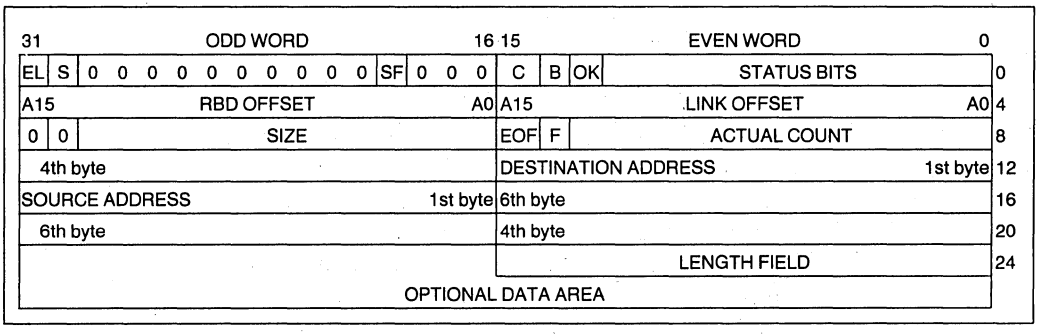


Figure 41. Receive Frame Descriptor—32-Bit Segmented Mode

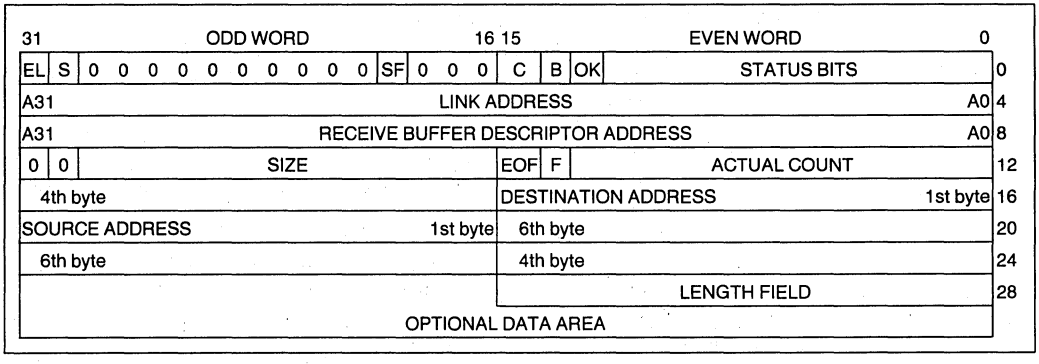


Figure 42. Receive Frame Descriptor—Linear Mode

where:

EL — When set, this bit indicates that this RFD is the last one on the RDL.

S — When set, this bit suspends the RU after receiving the frame.

SF — This bit selects between the Simplified or the Flexible mode.

0 — Simplified mode, all the RX data is in the RFD. RBD ADDRESS field is all "1s."

1 — Flexible mode. Data is in the RFD and in a linked list of Receive Buffer Descriptors.

C — This bit indicates the completion of frame reception. It is set by the 82596.

B — This bit indicates that the 82596 is currently receiving this frame, or that the 82596 is ready to receive the frame. It is initially set to 0 by the CPU. The 82596 sets it to 1 when reception set up begins, and to 0 upon completion. The C and B bits are set during the same operation.

OK (bit 13) — Frame received successfully, without errors. RFDs with bit 13 equal to 0 are possible only if the save bad frames configuration option is selected. Otherwise all frames with errors will be discarded, although statistics will be collected on them.

STATUS — The results of the Receive operation. Defined bits are,

Bit 12: Length error if configured to check length

Bit 11: CRC error in an aligned frame

Bit 10: Alignment error (CRC error in misaligned frame)

Bit 9: Ran out of buffer space—no resources

Bit 8: DMA Overrun failure to acquire the system bus.

Bit 7: Frame too short.

Bit 6: No EOP flag (for Bit stuffing only)

Bit 5: When the SF bit equals zero, and the 82596 is configured to save bad frames, this bit signals that the received frame was truncated. Otherwise it is zero.

Bits 2–4: Zeros

Bit 1: When it is zero, the destination address of the received frame matches the IA address. When it is 1, the destination address of the received frame does not match the individual address. For example, a multicast address or broadcast address will set this bit to a 1.

Bit 0: Receive collision. A collision is detected during reception, and the collision occurred after the destination address was received.

LINK ADDRESS — A 16-bit offset (32-bit address in the Linear mode) to the next Receive Frame Descriptor. The Link Address of the last frame can be used to form a cyclical list.

RBD POINTER — The offset (address in the Linear mode) of the first RBD containing the received frame data. An RBD pointer of all ones indicates no RBD.

EOF
F
SIZE
ACT COUNT — These fields are for the Simplified and Flexible memory models. They are exactly the same as the respective fields in the Receive Buffer Descriptor. See the next section for detailed explanation of their functions.

MC — Multicast bit.

DESTINATION ADDRESS — The contents of the destination address of the receive frame. The field is 0 to 6 bytes long.

SOURCE ADDRESS — The contents of the Source Address field of the received frame. It is 0 to 6 bytes long.

LENGTH FIELD — The contents of this 2-byte field are user defined. In 802.3 it contains the length of the data field. It is placed in memory in the same order it is received, i.e., most significant byte first, least significant byte second.

NOTES

1. The Destination address, Source address and Length fields are packed, i.e., one field immediately follows the next.
2. The affect of Address/Length Location (No Source Address Insertion) configuration parameter while receiving is as follows:

— 82586 Mode: The Destination address, Source address and Length field are not used, they are placed in the RX data buffers.

— 32-Bit Segmented and Linear Modes: when the Simplified memory model is used, the Destination address, Source address and Length fields reside in their respective fields in the RFD. When the Flexible memory strucrture is used the Destination address, Source address, and Length field locations depend on the SIZE field of the RFD. They can be placed in the RFD, in the RX data buffers, or partially in the RFD and the rest in the RX data buffers, depending on the SIZE field value.

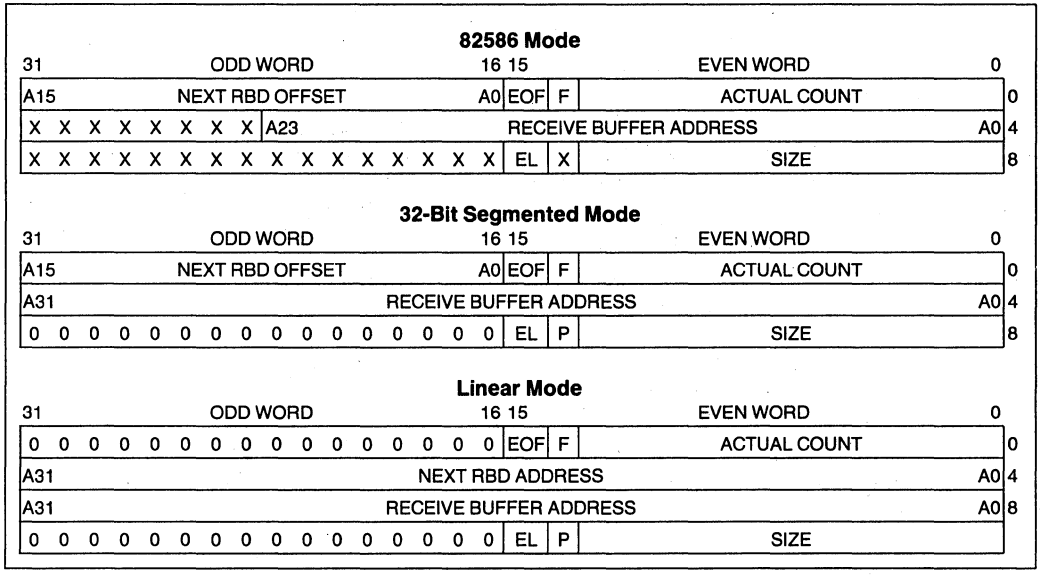


Figure 43. Receive Buffer Descriptor

where:

EOF — Indicates that this is the last buffer related to the frame. It is cleared by the CPU before starting the RU, and is written by the 82596 at the end of reception of the frame.

F — Indicates that this buffer has already been used. The Actual Count has no meaning unless the F bit equals one. This bit is cleared by the CPU before starting the RU, and is set by the 82596 after the associated buffer has been. This bit has the same meaning as the Complete bit in the RFD and CB.

ACT COUNT — This 14-bit quantity indicates the number of meaningful bytes in the buffer. It is cleared by the CPU before starting the RU, and is written by the 82596 after the associated buffer has already been used. In general, after the buffer is full, the Actual Count value equals the size field of the same buffer. For the last buffer of the frame, Actual Count can be less than the buffer size.

NEXT BD ADDRESS — The offset (absolute address in the Linear mode) of the next RBD on the list. It is meaningless if EL = 1.

BUFFER ADDRESS — The starting address of the memory area that contains the received data. In the 82586 mode, this is a 24-bit address (with pins A24–A31 = 0). In the 32-bit Segmented and Linear modes this is a 32-bit address.

EL — Indicates that the buffer associated with this RBD is last in the FBL.

P — This bit indicates that the 82596 has already prefetched the RBDs and any change in the RBD data will be ignored. This bit is valid only in the new 82596 memory modes, and if this feature has been enabled during configure command. The 82596 Prefetches the RBDs in locked cycles; after prefetching the RBD the 82596 performs a write cycle where the P bit is set to one and the rest of the data remains unchanged. The CPU is responsible for resetting it in all RBDs. The 82596 will not check this bit before setting it.

SIZE — This 14-bit quantity indicates the size, in bytes, of the associated buffer. This quantity must be an even number.

PGA PACKAGE THERMAL SPECIFICATION

Parameter	Thermal Resistance
θ_{JC}	3°C/W
θ_{JA}	24°C/W

ELECTRICAL AND TIMING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Case Temperature under Bias ... −65°C to +110°C
Supply Voltage
with Respect to V_{SS} ..... −0.5V to +6.5V
Voltage on Other Pins ..... −0.5V to V_{CC} + 0.5V

D.C. CHARACTERISTICS

T_C = 0°C to +85°C, V_{CC} = 5V ±10% CLK2 and LE/$\overline{BE}$ have MOS levels (see V_{MIL}, V_{MIH}).
All other signals have TTL levels (see V_{IL}, V_{IH}, V_{OL}, V_{OH}).

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage (TTL)	−0.3	+0.8	V	
V_{IH}	Input High Voltage (TTL)	2.0	V_{CC} + 0.3	V	
V_{MIL}	Input Low Voltage (MOS)	−0.3	+0.8	V	
V_{MIH}	Input High Voltage (MOS)	3.7	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage (TTL)		0.45	V	I_{OL} = 4.0 mA
V_{CIL}	$\overline{RxC}$, $\overline{TxC}$ Input Low Voltage	−0.5	0.6	V	
V_{CIH}	$\overline{RxC}$, $\overline{TxC}$ Input High Voltage	3.3	V_{CC} + 0.5	V	
V_{OH}	Output High Voltage (TTL)	2.4		V	I_{OH} = 0.9mA−1 mA
I_{LI}	Input Leakage Current		±15	μA	$0 \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current		±15	μA	$0.45 < V_{OUT} < V_{CC}$
C_{IN}	Capacitance of Input Buffer		10	pF	FC = 1 MHz
C_{OUT}	Capacitance of Input/Output Buffer		12	pF	FC = 1 MHz
C_{CLK}	CLK Capacitance		20	pF	FC = 1 MHz
I_{CC}	Power Supply		150	mA	At 20 MHz for the 82596SX I_{CC} Typical = 90 mA
I_{CC}	Power Supply		200	mA	At 25 MHz I_{CC} Typical = 100 mA
I_{CC}	Power Supply		300	mA	At 33 MHz I_{CC} Typical = 150 mA

A.C. CHARACTERISTICS

82596DX C-STEP INPUT/OUTPUT SYSTEM TIMINGS T_C = 0°C to +85°, V_{CC} = 5V ±10%

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	25 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	25 MHz	CLK2/2
T1	CLK2 Period	20	40	
T2	CLK2 High	4		3.7V
T3	CLK2 Low	5		0.8V
T4	CLK2 Rise Time	—	7	0.8V to 3.7V
T5	CLK2 Fall Time	—	7	3.7V to 0.8V
T13	CA and BREQ Setup Time	7		1, 2, 3
T14	BREQ Hold Time	3		1, 2, 3
T14a	CA Hold Time	5		1, 2, 3
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	4 T1		3
T25	INT Valid Delay	1	26	
T6	$\overline{BEx}$ Valid Delay	3	17	
T6b	$\overline{LOCK}$ Valid Delay	3	21	
T6c	A2–A31 Valid Delay	3	18	
T7	$\overline{BEx}$, $\overline{LOCK}$, and A2–A31 Float Delay	4	30	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	21	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	4	30	
T10	D0–D31 Write Data Valid Delay	3	19	
T11	D0–D31 Write Data Float Delay	4	22	
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	7		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	5		2
T29	$\overline{PORT}$ Setup Time	7		2
T30	$\overline{PORT}$ Hold Time	3		2
T17	$\overline{RDY}$ Setup Time	9		2
T18	$\overline{RDY}$ Hold Time	3		2
T19	D0–D31 READ Setup Time	7		2
T20	D0–D31 READ Hold Time	5		2
T12	HOLD Valid Delay	3	22	
T21	HLDA Setup Time	10		1, 2
T22a	HLDA Hold Time	3		1, 2
T23	RESET Setup Time	10		2
T24	RESET Hold Time	3		2

NOTE:
Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

A.C. CHARACTERISTICS (Continued)

82596DX C-STEP INPUT/OUTPUT SYSTEM TIMINGS $T_C = 0°C$ to $+85°C$, $V_{CC} = 5V \pm 5\%$

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	33 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	33 MHz	CLK2/2
T1	CLK2 Period	15	40	
T2	CLK2 High	4.5		3.7V
T3	CLK2 Low	4.5		0.8V
T4	CLK2 Rise Time	—	4	3.7V to 0.8V
T5	CLK2 Fall Time	—	4	0.8V to 3.7V
T13	CA and BREQ Setup Time	7		1, 2, 3
T14	BREQ Hold Time	3		1, 2, 3
T14a	CA Hold Time	5		1, 2, 3
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	4 T1		3
T25	INT Valid Delay	1	20	
T6	$\overline{BEx}$ Valid Delay	3	17	
T6b	$\overline{LOCK}$ Valid Delay	3	16	
T6c	A2–A31 Valid Delay	3	18	
T7	$\overline{BEx}$, $\overline{LOCK}$, and A2–A31 Float Delay	4	20	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	16	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	4	20	
T10	D0–D31 Write Data Valid Delay	3	19	
T11	D0–D31 Write Data Float Delay	4	17	
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	5		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	3		2
T29	$\overline{PORT}$ Setup Time	7		2
T30	$\overline{PORT}$ Hold Time	3		2
T17	$\overline{RDY}$ Setup Time	8		2
T18	$\overline{RDY}$ Hold Time	3		2
T19	D0–D31 READ Setup Time	5.5		2
T20	D0–D31 READ Hold Time	4		2
T12	HOLD Valid Delay	3	19	
T21	HLDA Setup Time	8		1, 2
T22a	HLDA Hold Time	3		1, 2
T23	RESET Setup Time	9		2
T24	RESET Hold Time	3		2

NOTE:
Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

A.C. CHARACTERISTICS (Continued)

82596SX C-STEP INPUT/OUTPUT SYSTEM TIMINGS $T_C = 0°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	20 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	20 MHz	CLK2/2
T1	CLK2 Period	25	40	
T2	CLK2 High	8		at 2.0V
T3	CLK2 Low	8		at 2.0V
T4	CLK2 Rise Time	—	8	0.8V to 3.7V
T5	CLK2 Fall Time	—	8	3.7V to 0.8V
T13	CA and BREQ Setup Time	10		1, 2, 3
T14	BREQ Hold Time	7		1, 2, 3
T14a	CA Hold Time	8		1, 2, 3
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	4 T1		3
T25	INT Valid Delay	1	35	
T6	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$, BON, and A1–A31 Valid Delay	3	30	
T7	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$, BON, and A1–A31 Float Delay	4	30	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	26	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	4	30	
T10	D0–D15 Write Data Valid Delay	3	38	
T11	D0–D15 Write Data Float Delay	4	27	
T27	D0–D15 CPU $\overline{PORT}$ Access Setup Time	9		2
T28	D0–D15 CPU $\overline{PORT}$ Access Hold Time	6		2
T29	$\overline{PORT}$ Setup Time	10		2
T30	$\overline{PORT}$ Hold Time	7		2
T17	$\overline{RDY}$ Setup Time	12		2
T18	$\overline{RDY}$ Hold Time	4		2
T19	D0–D15 READ Setup Time	9		2
T20	D0–D15 READ Hold Time	5		2
T12	HOLD Valid Delay	3	28	
T21	HLDA Setup Time	15		1, 2
T22a	HLDA Hold Time	7		1, 2
T23	RESET Setup Time	12		1, 2
T24	RESET Hold Time	4		1, 2

NOTE:
Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

A.C. CHARACTERISTICS (Continued)

82596SX C-STEP INPUT/OUTPUT SYSTEM TIMINGS T_C = 0°C to +85°C, V_{CC} = 5V ±10%

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	16 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	16 MHz	CLK2/2
T1	CLK2 Period	31	40	
T2	CLK2 High	9		2.0V
T3	CLK2 Low	9		2.0V
T4	CLK2 Rise Time	—	8	0.8V to 3.7V
T5	CLK2 Fall Time	—	8	3.7V to 0.8V
T13	CA and BREQ Setup Time	11		1, 2, 3
T14	CA and BREQ Hold Time	8		1, 2, 3
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	4 T1		3
T25	INT Valid Delay	1	40	
T6	$\overline{BHE}$, $\overline{BLE}$, BON, and A1–A31 Valid Delay	3	36	
T6b	LOCK# Valid Delay	1	33	
T7	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$, BON, and A1–A31 Float Delay	4	40	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	1	33	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	4	35	
T10	D0–D15 Write Data Valid Delay	3	40	
T11	D0–D15 Write Data Float Delay	4	35	
T27	D0–D15 CPU $\overline{PORT}$ Access Setup Time	9		2
T28	D0–D15 CPU $\overline{PORT}$ Access Hold Time	6		2
T29	$\overline{PORT}$ Setup Time	11		2
T30	$\overline{PORT}$ Hold Time	8		2
T17	$\overline{RDY}$ Setup Time	19		2
T18	$\overline{RDY}$ Hold Time	6		2
T19	D0–D15 READ Setup Time	9		2
T20	D0–D15 READ Hold Time	6		2
T12	HOLD Valid Delay	2	33	

A.C. CHARACTERISTICS (Continued)

82596SX C-STEP INPUT/OUTPUT SYSTEM TIMINGS T_C = 0°C to +85°C, V_{CC} = 5V ±10% (Continued)

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	16 MHz		Notes
		Min	Max	
T21	HLDA Setup Time	15		1, 2
T22a	HLDA Hold Time	7		1, 2
T23	RESET Setup Time	13		1, 2
T24	RESET Hold Time	4		1, 2

NOTES:
Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.
1. RESET, HLDA, and CA are internally synchronized. This timing is to guarantee recognition at next clock for RESET, HLDA, and CA.
2. All set-up, hold, and delay timings are at the maximum frequency specification Fmax, and must be derated according to the following equation for operation at lower frequencies:
   Tderated = (Fmax/Fopr) × T
   where:
   Tderated = Specifies the value to derate the specification.
   Fmax = Maximum operating frequency.
   Fopr = Actual operating frequency.
   T = Specification at maximum frequency.
This calculation only provides a rough estimate for derating the frequency. For more detailed information contact your Intel sales office for the data sheet supplement.
3. CA is internally synchronized; if the setup and hold times are met then CA needs to be only 2 T1. BREQ and $\overline{\text{PORT}}$ are not internally synchronized. BREQ must meet setup and hold times and need only be 2 T1 wide.

TRANSMIT/RECEIVE CLOCK PARAMETERS

Symbol	Parameter	20 MHz		Notes
		Min	Max	
T36	$\overline{TxC}$ Cycle	50		1, 3
T38	$\overline{TxC}$ Rise Time		5	1
T39	$\overline{TxC}$ Fall Time		5	1
T40	$\overline{TxC}$ High Time	19		1, 3
T41	$\overline{TxC}$ Low Time	18		1, 3
T42	TxD Rise Time		10	4
T43	TxD Fall Time		10	4
T44	TxD Transition	20		2, 4
T45	$\overline{TxC}$ Low to TxD Valid		25	4, 6
T46	$\overline{TxC}$ Low to TxD Transition		25	2, 4
T47	$\overline{TxC}$ High to TxD Transition		25	2, 4
T48	$\overline{TxC}$ Low to TxD High (At End of Transition)		25	4
$\overline{RTS}$ AND $\overline{CTS}$ PARAMETERS				
T49	$\overline{TxC}$ Low to $\overline{RTS}$ Low, Time to Activate $\overline{RTS}$		25	5
T50	$\overline{CTS}$ Low to $\overline{TxC}$ Low, $\overline{CTS}$ Setup Time		20	
T51	$\overline{TxC}$ Low to $\overline{CTS}$ Invalid, $\overline{CTS}$ Hold Time	10		7
T52	$\overline{TxC}$ Low to $\overline{RTS}$ High		25	5
RECEIVE CLOCK PARAMETERS				
T53	$\overline{RxC}$ Cycle	50		1, 3
T54	$\overline{RxC}$ Rise Time		5	1
T55	$\overline{RxC}$ Fall Time		5	1
T56	$\overline{RxC}$ High Time	19		1
T57	$\overline{RxC}$ Low Time	18		1
RECEIVED DATA PARAMETERS				
T58	RxD Setup Time	20		6
T59	RxD Hold Time	10		6

TRANSMIT/RECEIVE CLOCK PARAMETERS (Continued)

Symbol	Parameter	20 MHz		Notes
		Min	Max	
RECEIVED DATA PARAMETERS (Continued)				
T60	RxD Rise Time		10	
T61	RxD Fall Time		10	
$\overline{CRS}$ AND $\overline{CDT}$ PARAMETERS				
T62	$\overline{CDT}$ Low to $\overline{TxC}$ HIGH External Collision Detect Setup Time	20		
T63	$\overline{TxC}$ High to $\overline{CDT}$ Inactive, $\overline{CDT}$ Hold Time	10		
T64	$\overline{CDT}$ Low to Jam Start			10
T65	$\overline{CRS}$ Low to $\overline{TxC}$ High, Carrier Sense Setup Time	20		
T66	$\overline{TxC}$ High to $\overline{CRS}$ Inactive, $\overline{CRS}$ Hold Time	10		
T67	$\overline{CRS}$ High to Jamming Start, (Internal Collision Detect)			12
T68	Jamming Period			11
T69	$\overline{CRS}$ High to $\overline{RxC}$ High, $\overline{CRS}$ Inactive Setup Time	30		
T70	$\overline{RxC}$ High to $\overline{CRS}$ High, $\overline{CRS}$ Inactive Hold Time	10		
INTERFRAME SPACING PARAMETERS				
T71	Interframe Delay			9
EXTERNAL LOOPBACK-PIN PARAMETERS				
T72	$\overline{TxC}$ Low to $\overline{LPBK}$ Low		T36	4
T73	$\overline{TxC}$ Low to $\overline{LPBK}$ High		T36	4

NOTES:
1. Special MOS levels, V_{CIL} = 0.9V and V_{CIH} = 3.0V.
2. Manchester only.
3. Manchester. Needs 50% duty cycle.
4. 1 TTL load + 50 pF.
5. 1 TTL load + 100 pF.
6. NRZ only.
7. Abnormal end of transmission—CTS expires before RTS.
8. Normal end to transmission.
9. Programmable value:
   T71 = N_{IFS} • T36
   where: N_{IFS} = the IFS configuration value
   (if N_{IFS} is less than 12 then N_{IFS} is forced to 12).
10. Programmable value:
    T64 = (N_{CDF} • T36) + x • T36
    (If the collision occurs after the preamble)
    where:
    N_{CDF} = the collision detect filter configuration value, and
    x = 12, 13, 14, or 15
11. T68 = 32 • T36
12. Programmable value:
    T67 = (N_{CSF} • T36) + x • T36
    where: N_{CSF} = the Carrier Sense Filter configuration value, and
    x = 12, 13, 14, or 15
13. To guarantee recognition on the next clock.

82596DX/SX BUS OPERATION

The following figures show thae basic bus cycles for the 82596DX and 82596SX.

For more details refer to the *32-Bit LAN Components Manual.*

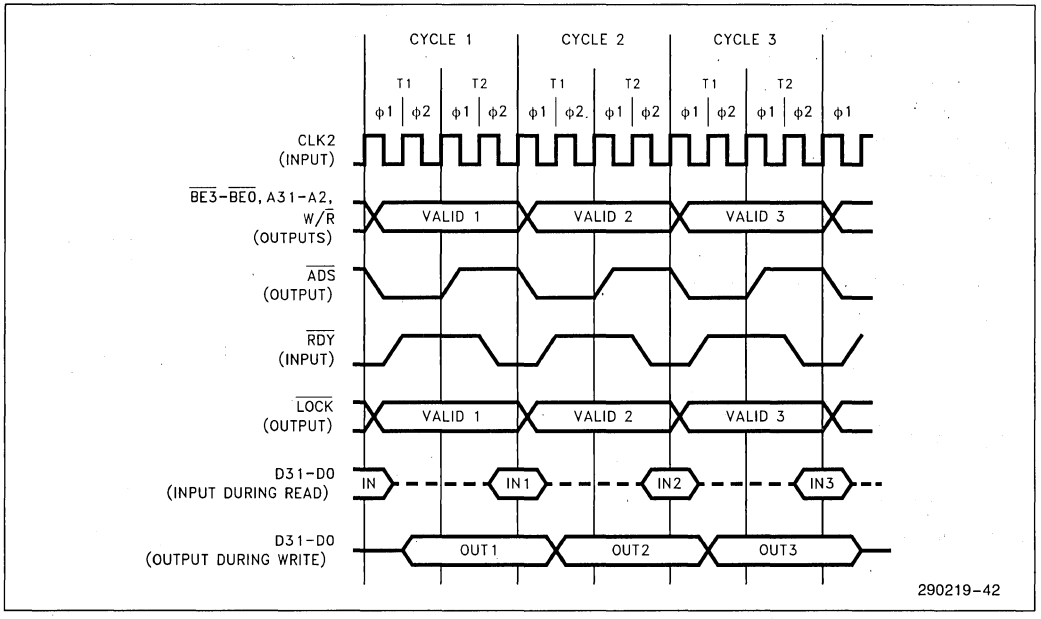


Figure 44. Basic 82596DX Bus Cycles

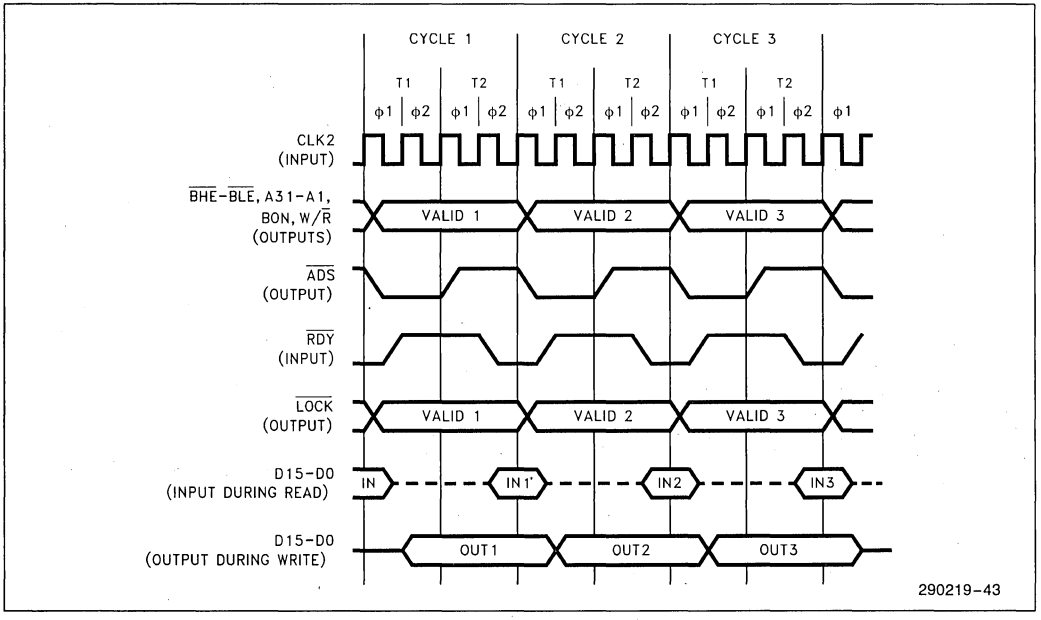


Figure 45. Basic 82596SX Bus Cycles

SYSTEM INTERFACE A.C. TIMING CHARACTERISTICS

The measurements should be done at:

- T_C = 0°C–85°C, V_{CC} = 5V ±10%, C = 50 pF unless otherwise specified.
- A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
- Timing measurements are made at 1.5V for both logic "1" and "0".
- Rise and Fall time of inputs and outputs signals are measured between 0.8V and 2.0V respectively unless otherwise specified.
- All timings are relative to CLK2 crossing the 1.5V level.
- All A.C. parameters are valid only after 100 μs from power up.

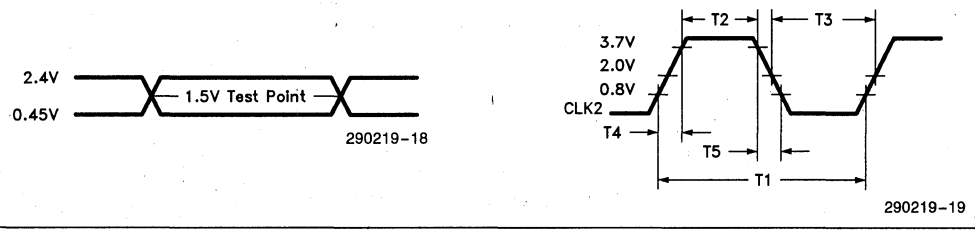
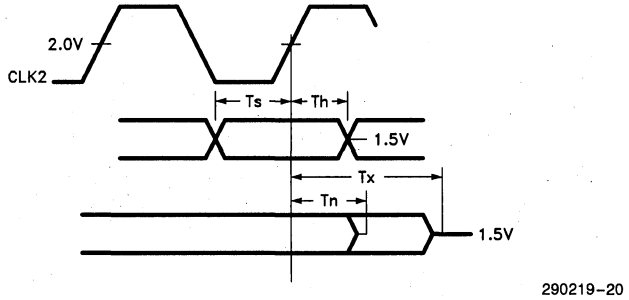


Figure 46. CLK2 Timings

Two types of timing specifications are presented below:

1. Input Timing—minimum setup and hold times.
2. Output Timings—output delays and float times from CLK2 rising edge.

Figure 45 defines how the measurements should be done:



LEGEND:
Ts = Input Setup Time
Th = Input Hold Time
Tn = Minimum output delay or Mininum float delay
Tx = Maximum output delay or Maximum float delay

Figure 47. Drive Levels and Measurements Points for A.C. Specifications

INPUT WAVEFORMS

Ts = T13, T15, T17, T19, T21, T23, T27, T29, T31
Th = T14, T16, T18, T20, T22, T22a, T24, T28, T30, T32

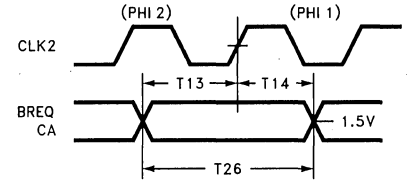


Figure 48. CA and BREQ Input Timing

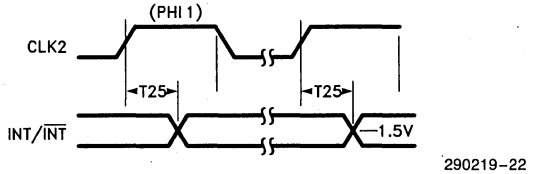


Figure 49. INT/$\overline{INT}$ Output Timing

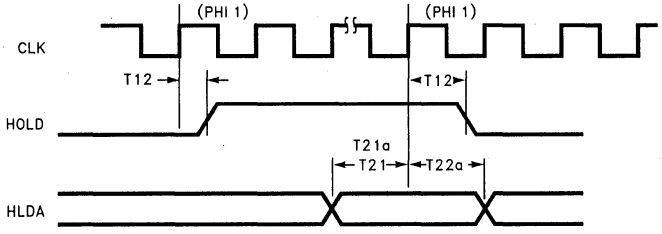


Figure 50. HOLD/HLDA Timings

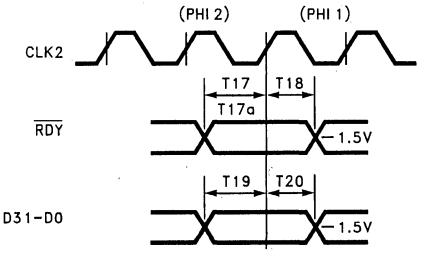


Figure 51. Input Setup and Hold Time

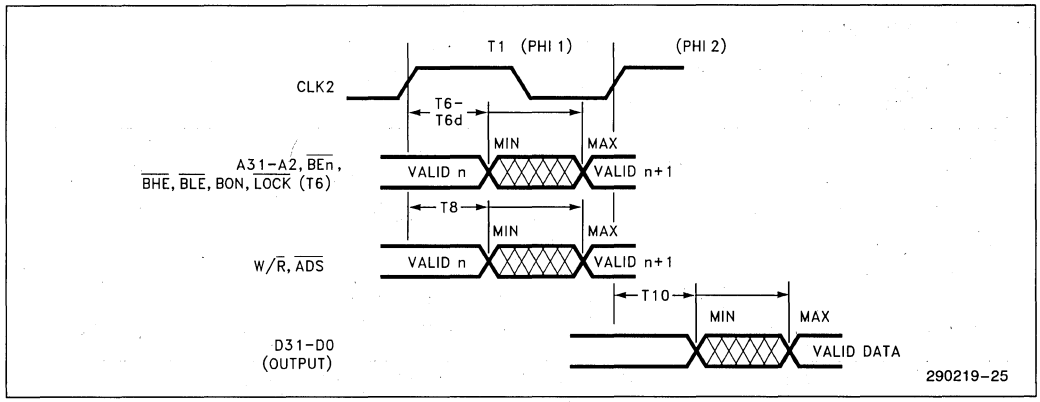


Figure 52. Output Valid Delay Timing

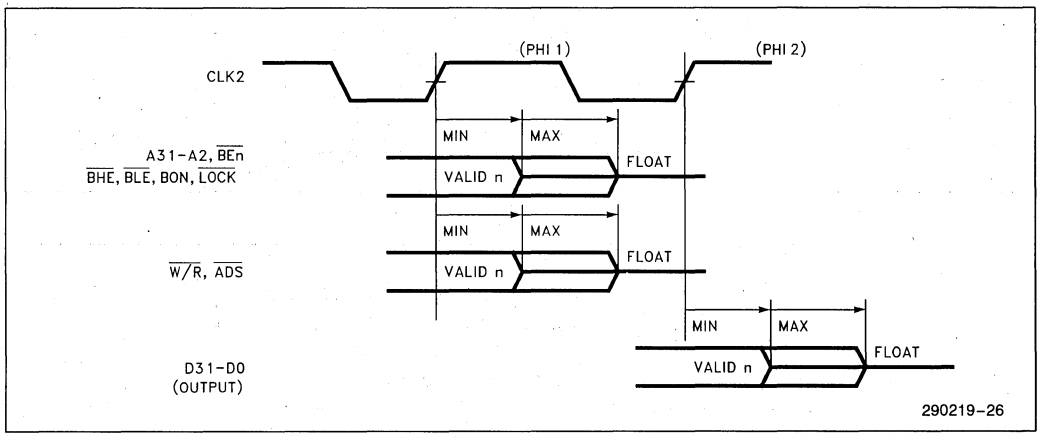


Figure 53. Output Float Delay Timing

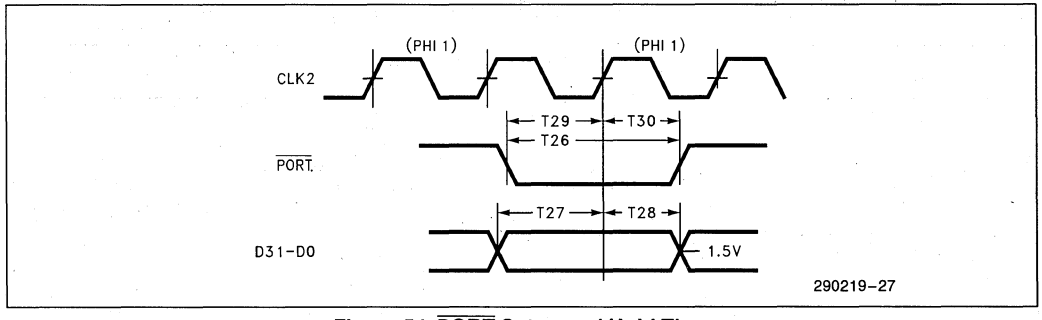


Figure 54. PORT Setup and Hold Time

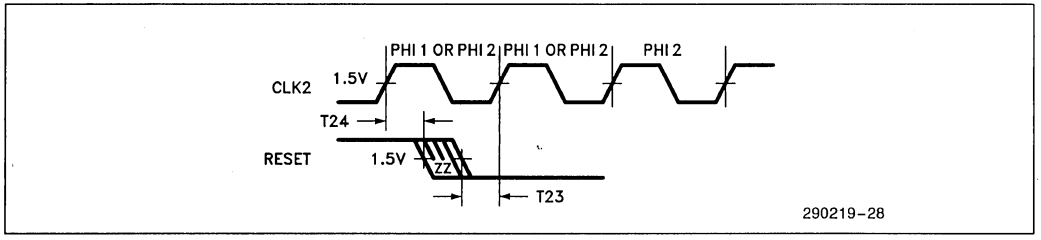


Figure 55. RESET Input Timing

SERIAL A.C. TIMING CHARACTERISTICS

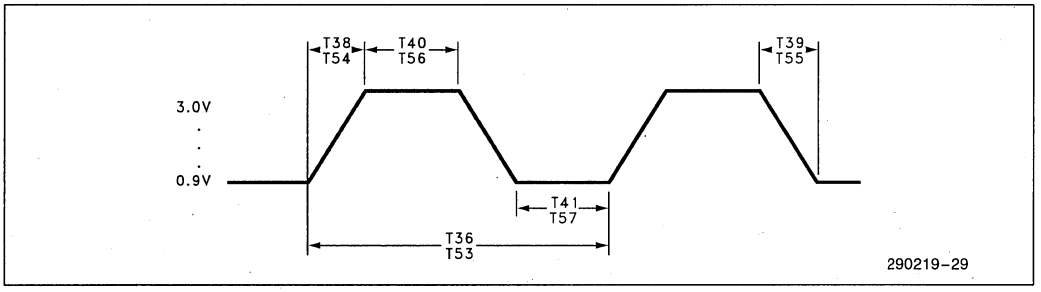


Figure 56. Serial Input Clock Timing

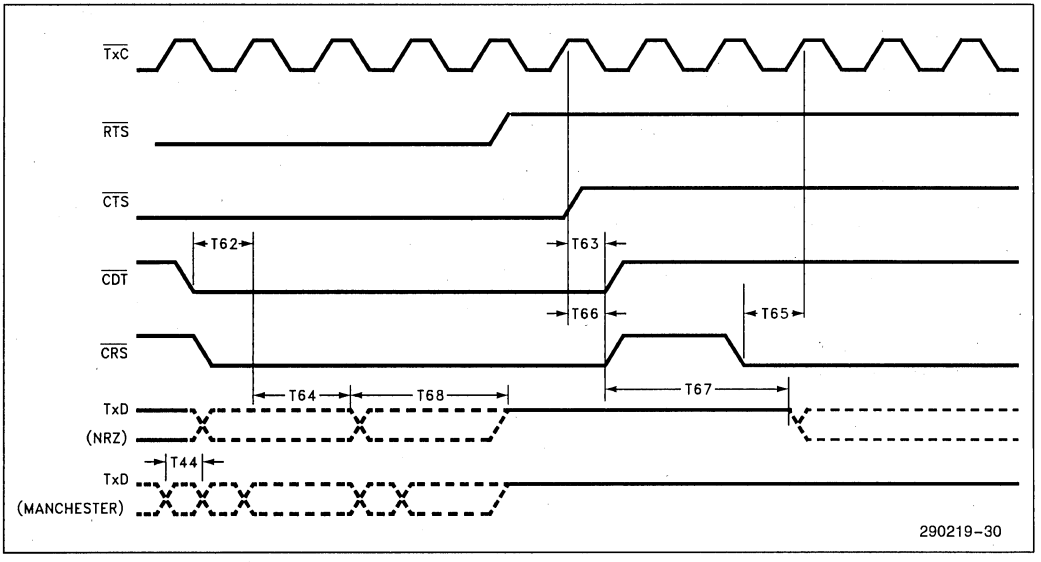


Figure 57. Transmit Data Waveforms

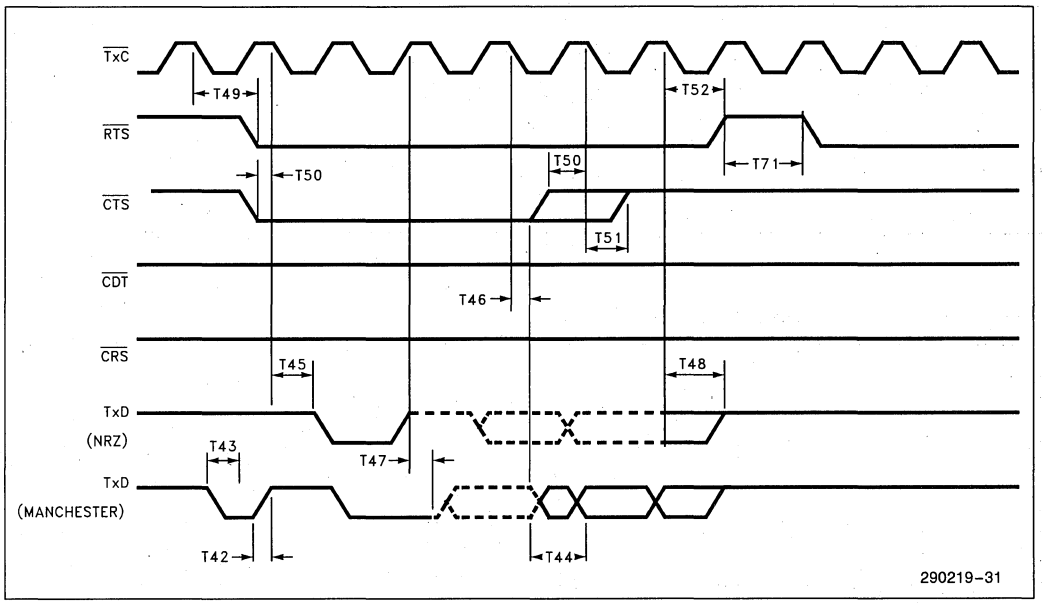


Figure 58. Transmit Data Waveforms

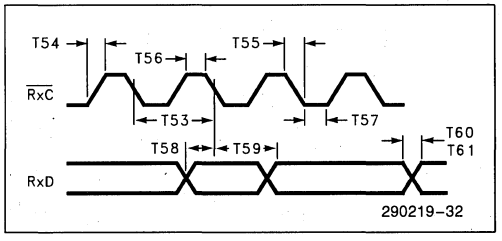


Figure 59. Receive Data Waveforms (NRZ)

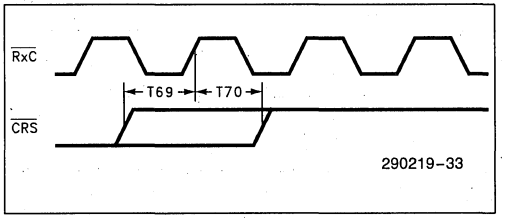
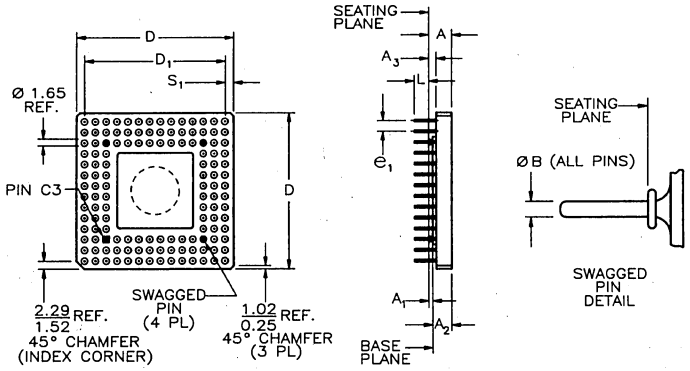


Figure 60. Receive Data Waveforms (CRS)

OUTLINE DIAGRAMS

132 LEAD CERAMIC PIN GRID ARRAY PACKAGE INTEL TYPE A



290219-36

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A_2	2.67	3.43	Solid Lid	0.105	0.135	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	36.45	37.21		1.435	1.465	
D_1	32.89	33.15		1.295	1.305	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	132			132		
S_1	1.27	2.54		0.050	0.100	
ISSUE	IWS 10/12/88					

Intel Case Outline Drawings
Plastic Quad Flat Pack (PQFP)
0.025 Inch (0.635mm) Pitch

Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170
A1	Standoff	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
D, E	Terminal Dimension	0.675	0.685	0.775	0.785	0.875	0.885	1.075	1.085	1.275	1.285	1.475	1.485
D1, E1	Package Body	0.547	0.553	0.647	0.653	0.747	0.753	0.947	0.953	1.147	1.153	1.347	1.353
D2, E2	Bumper Distance	0.697	0.703	0.797	0.803	0.897	0.903	1.097	1.103	1.297	1.303	1.497	1.503
D3, E3	Lead Dimension	0.400 REF		0.500 REF		0.600 REF		0.800 REF		1.000 REF		1.200 REF	
D4, E4	Foot Radius Location	0.623	0.637	0.723	0.737	0.823	0.837	1.023	1.037	1.223	1.237	1.423	1.437
L1	Foot Length	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
Issue	IWS Preliminary 12/12/88												INCH

Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32
A1	Standoff	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
D, E	Terminal Dimension	17.15	17.40	19.69	19.94	22.23	22.48	27.31	27.56	32.39	32.64	37.47	37.72
D1, E1	Package Body	13.89	14.05	16.43	16.59	18.97	19.13	24.05	24.21	29.13	29.29	34.21	34.37
D2, E2	Bumper Distance	17.70	17.85	20.24	20.39	22.78	22.93	27.86	28.01	32.94	33.09	38.02	38.18
D3, E3	Lead Dimension	10.16 REF		12.70 REF		15.24 REF		20.32 REF		25.40 REF		30.48 REF	
D4, E4	Foot Radius Location	15.82	16.17	18.36	18.71	21.25	21.25	25.89	26.33	31.06	31.41	36.14	36.49
L1	Foot Length	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
Issue	IWS Preliminary 12/12/88												mm

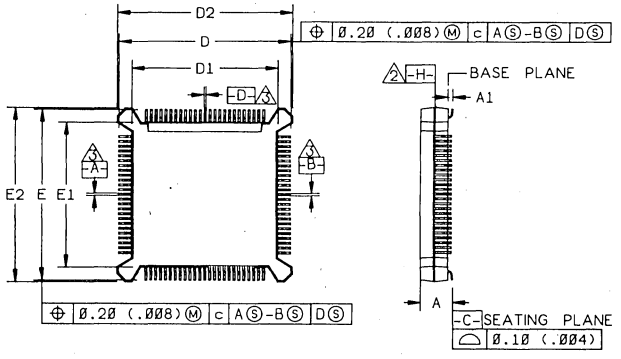


Figure 61. Principal Dimensions and Datums

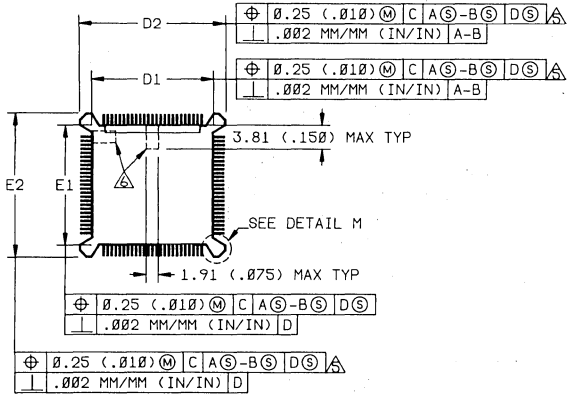


Figure 62. Molded Details

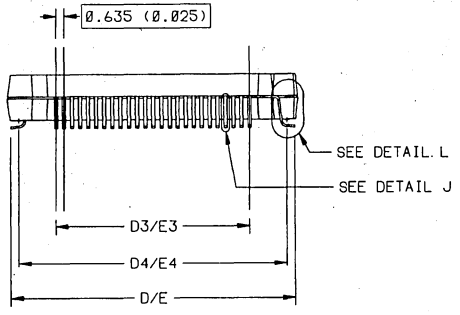
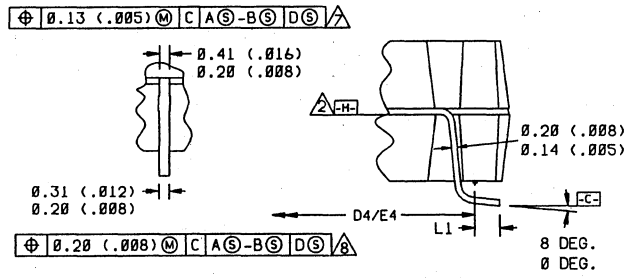


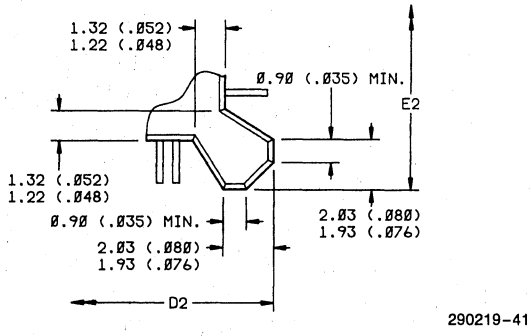
Figure 63. Terminal Details



mm (inch)

Detail J **Detail L**

Figure 64. Typical Lead



mm (inch)

Figure 65. Detail M

REVISION SUMMARY

The following represents the key differences between version -005 and version -006 of the 82596CA Data Sheet.

1. A description of the 82596DX/SX C-stepping enhancements was added and the 82596DX/SX B-step information was removed.
2. Recommendation to use only one type of buffer (either Simplified or Flexible) in any given linked list.
3. Added detailed description regarding operation of RCVCDT counter.
4. Added New Enhanced Big Endian Mode section. The New Enhanced Big Endian Mode applies only to the 82596 C-stepping.
5. Added programming recommendations regarding RU and CU Start commands. These warn against Starting the CU while it is Active and Starting the RU while it is Ready.
6. Emphasized that the TDR command is a static command and should not be used in an active network.
7. Improved 82596DX/SX C-step timings were added for all speeds.

82503
DUAL SERIAL TRANSCEIVER (DST)

82503 PRODUCT FEATURE SET OVERVIEW

- Single Component Ethernet* Interface to Both 802.3 10BASE-T and AUI
- Automatic or Manual Port Selection
- Manchester Encoder/Decoder and Clock Recovery
- No Glue Interface to Industry-Standard LAN Controllers
  - — Intel 82586, 82590, 82593 and 82596
  - — AMD 7990 (LANCE*)
  - — National Semiconductor 8390 and 83932 (SONIC*)
  - — Western Digital 83C690
  - — Fujitsu 86950 (Etherstar*)
- Diagnostic Loopback
- Reset, Low Power Modes
- Network Status Indicators
- Defeatable Jabber Timer
- User Test Modes
- 10 MHz Transmit Clock Generator
- One Micron CHMOS** IV (Px48) Technology
- Single 5-V Supply

1

INTERFACE FEATURES

TPE

- Complies with 10BASE-T, IEEE Std. 802.3i-1990 for Twisted Pair Ethernet
- Selectable Polarity Switching
- Direct Interface to TPE Analog Filters
- On-Chip TPE Squelch
- Defeatable Link Integrity (LI)
- Support of Cable Lengths $>$ 100m

AUI

- Complies with IEEE 802.3 AUI Standard
- Direct Interface to AUI Transformers
- On-Chip AUI Squelch

A block diagram of a typical application is shown in Figure 1. The 82503 Dual Serial Transceiver is a high-integration CMOS device designed to simplify interfacing industry standard Ethernet LAN Controllers to IEEE 802.3 local area network applications (10BASE5, 10BASE2, and 10BASE-T). The component supports both an attachment unit interface (AUI) and a Twisted Pair Ethernet interface (TPE). It allows OEMs to design a state-of-the-art media interface that is jumperless and fully automatic. The 82503 includes on-chip AUI and TPE drivers and receivers; it offers designers a cost-effective, integrated solution for interfacing LAN controllers to the wire medium.

**CHMOS is a patented process of Intel Corporation.
*Ethernet is a registered trademark of Xerox Corporation.
LANCE is a registered trademark of Advanced Micro Devices.
Etherstar is a registered trademark of Fujitsu Electronics.
Sonic is a registered trademark of National Semiconductor Corporation.

October 1995
Order Number: 290421-004

82503 Dual Serial Transceiver (DST)

CONTENTS

CONTENTS

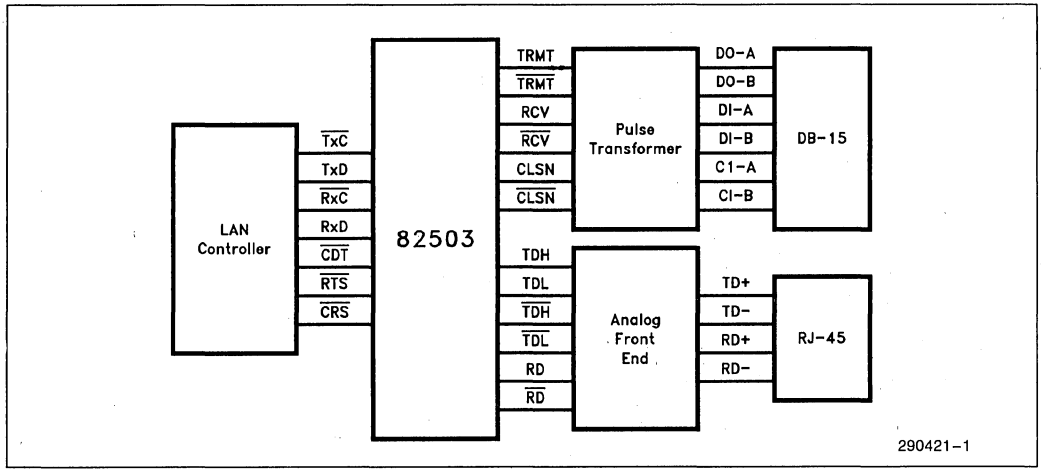


Figure 1. Application Block Diagram

1.0 82503 PRODUCT FEATURES

The 82503 incorporates all the active circuitry required to interface Ethernet controllers to 10BASE-T networks or the attachment unit interface (AUI). It supports a direct no-glue interface to Intel's family of high-performance LAN controllers (82586, 82590, 82593, and 82596). The 82503 also provides a direct no-glue interface to the National Semiconductor 8390 and 83932 (SONIC), the Western Digital 83C690, the Advanced Micro Devices 7990 (LANCE) and 79C900 (ILACC), and the Fujitsu 86950 (Etherstar) controllers.

This component includes three advanced features: jumperless two-port design capability, automatic port selection, and polarity switching. The jumperless TPE or AUI port selection capability allows designers maximum ease-of-use and network flexibility. Automatic port selection ensures complete software compatibility with existing 10BASE2 and 10BASE5 software drivers. The 82503's polarity switching feature will detect and correct polarity errors on the twisted pair—the most common wiring fault in twisted pair networks.

The 82503 contains all the circuitry needed to meet the 10BASE-T specification, including link integrity, a jabber timer and internal predistortion. Deselecting link integrity allows the component to be used in some prestandard networks. The 82503's jabber timer prevents the station from continuously transmitting and is defeatable for simple design characterization. The predistortion circuitry eliminates line overcharge and reduces jitter on 10BASE-T links.

The 82503 can also support twisted pair cable lengths of up to 200m when placed in TPE Extended Squelch Mode (XSQ).

This component incorporates six LED drivers to display transmit data, receive data, collision, link integrity, polarity faults and port selections, allowing for complete network monitoring by the user. The transmit, receive and collision LEDs indicate the rate of activity by the frequency of flashing. The 82503 also has a low power mode. During low power, many of the 82503's pins are in a high-impedance state to facilitate board-level testing.

The 82503's diagnostic loopback control enables it to route a transmission signal from the LAN controller through its Manchester encoder-decoder circuitry and back to the LAN controller. This provides effective network node fault detection and isolation capabilities. In addition, the 82503 supports diagnostic test modes that generate continuous tranmission of data through the twisted pair port, allowing designers to measure the analog performance of their design.

The 82503 is available in 44-lead PLCC and 44-lead QFP packages and is fabricated with Intel's low-power, high-speed, CHMOS IV technology using a single 5-V supply.

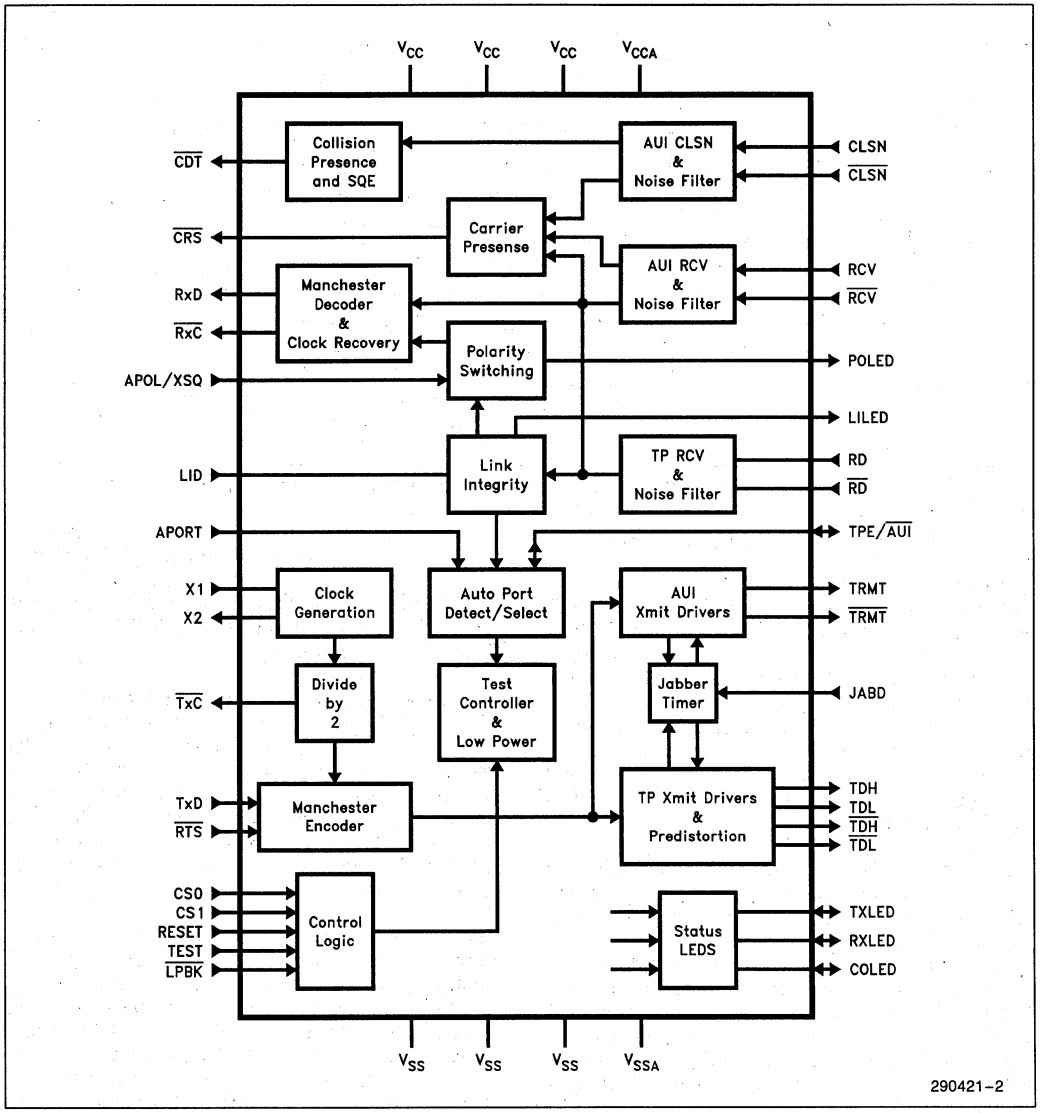


Figure 2. 82503 Functional Block Diagram

2.0 PIN DEFINITION

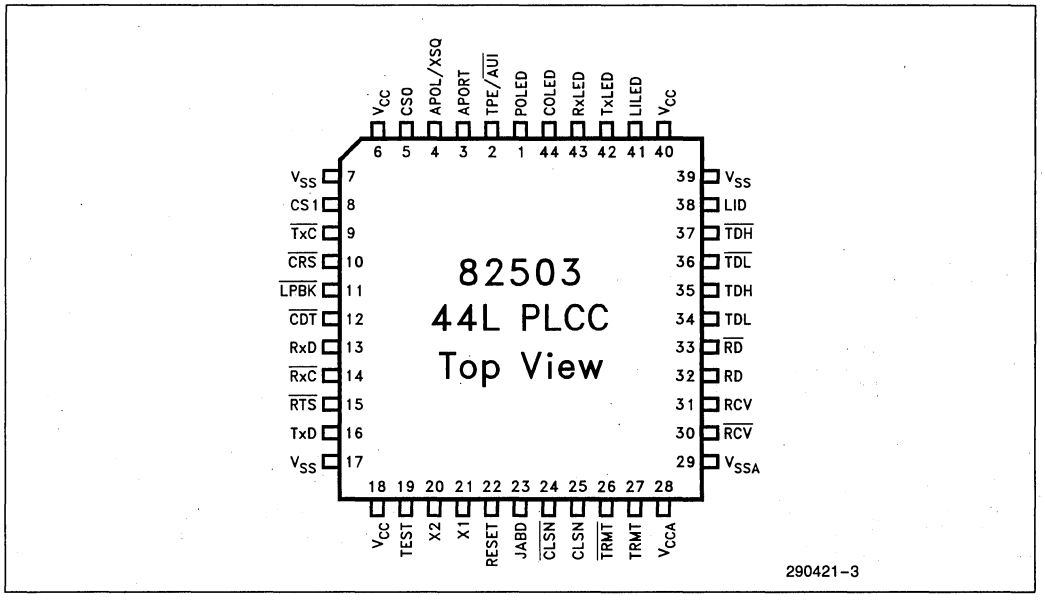


Figure 3. 44-Lead PLCC Pin Configuration

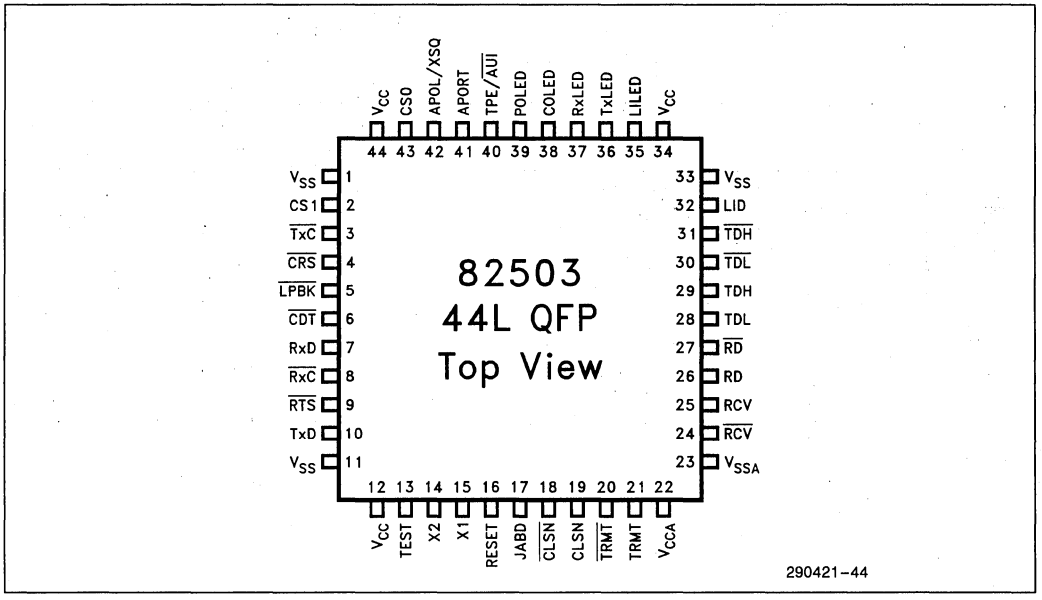


Figure 4. 44-Lead QFP Pin Configuration

2.1 Power Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
V_{SS}(1)	7, 17, 39	1, 11, 33	Supply	**Digital Ground.**
V_{CC}(1)	6, 18, 40	44, 12, 34	Supply	**Digital V_{CC}.** A 5-V ± 5% Power Supply.
V_{CCA}(1)	28	22	Supply	**Analog V_{CC}.** A 5-V ± 5% Power Supply.
V_{SSA}(1)	29	23	Supply	**Analog Ground.**

NOTE:
1. V_{CC} and V_{CCA} must be connected to the same power supply. V_{SS} and V_{SSA} must be connected to the same ground. Separate decoupling and noise conditioning (e.g., ferrite beads) should be used.

2.2 Clock Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
X1	21	15	I	**CLOCK CRYSTAL.** A 20 MHz crystal input. This pin can be driven with an external MOS level clock when X2 is left floating.
X2	20	14	O	**CLOCK CRYSTAL.** A 20 MHz crystal output. X1 can be driven with an external MOS level clock when this pin is left floating.

2.3 AUI Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TRMT $\overline{\text{TRMT}}$	27 26	21 20	O O	**TRANSMIT PAIR.** A differential output driver pair that drives the transmit pair of the transceiver cable. The output bit stream is Manchester encoded. Following the last transition, which is positive at TRMT, the differential voltage is reduced to zero volts.
RCV $\overline{\text{RCV}}$	31 30	25 24	I I	**RECEIVE PAIR.** A differentially driven input pair which is tied to the receive pair of the Ethernet transceiver cable. The first transition on RCV is negative-going to indicate the beginning of the frame. The last transition is positive-going to indicate the end of the frame. The received bit stream is assumed to be Manchester encoded.
CLSN $\overline{\text{CLSN}}$	25 24	19 18	I I	**COLLISION PAIR.** A differentially driven input pair tied to the collision presence pair of the Ethernet transceiver cable. The collision presence signal is a 10 MHz square wave. The first transition at CLSN is negative-going to indicate the beginning of the signal; the last transition is positive-going to indicate the end of the signal.

2.4 TPE Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TDH $\overline{TDH}$ TDL $\overline{TDL}$	35 37 34 36	29 31 28 30	O O O O	**TP TRANSMIT PAIR DRIVERS.** These four outputs constitute the twisted-pair drivers, which have predistortion capabilities. The TDH/$\overline{TDH}$ outputs generate the 10 Mb/s Manchester Encoded data. The TDL/$\overline{TDL}$ outputs mirror the TDH/$\overline{TDH}$ outputs except for fat bit occurrences (100 ns pulses). During the second half of a fat bit (either high or low), the TDL/$\overline{TDL}$ outputs are inverted with respect to TDH/$\overline{TDH}$ outputs. This signal behavior reduces the amount of jitter by preventing overcharge on the twisted pair medium.
RD $\overline{RD}$	32 33	26 27	I I	**TP RECEIVE PAIR.** The differential twisted pair receiver. The receiver pair is connected to the twisted pair medium and is driven with 10 Mb/s Manchester encoded data.

1

2.5 Controller Interface Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
$\overline{TxC}$	9	3	O	**TRANSMIT CLOCK.** A 10 MHz clock output tied directly to the transmit clock pin of the Ethernet controller. Changes sense depending on controller selected. Active low for Intel and Fujitsu controller interfaces, active high for National and AMD interfaces. Can drive one TTL load.
TxD	16	10	I	**TRANSMIT DATA.** TTL input. NRZ serial data is clocked in on TxD from the Ethernet controller. Connects directly to the transmit data pin of the Ethernet controller.
$\overline{RTS}$	15	9	I	**REQUEST TO SEND.** TTL input. An active low input signal synchronous to $\overline{TxC}$ which enables data transmission on the active port. Changes sense depending on controller selected. Active low for the Intel controller interface, active high for National, AMD, and Fujitsu interfaces.
$\overline{RxC}$	14	8	O	**RECEIVE CLOCK.** A 10 MHz clock output tied directly to the receive clock pin of the Ethernet controller. This clock is the recovered clock from incoming data on the active port. Changes sense depending on controller selected. Active low for Intel and Fujitsu controller interfaces, active high for National and AMD interfaces. Can drive one TTL load.
RxD	13	7	O	**RECEIVE DATA.** Received NRZ data (synchronous to $\overline{RxC}$) passed to the Ethernet controller. Connect directly to the receive data pin of the controller. Can drive one TTL load.
$\overline{CRS}$	10	4	O	**CARRIER SENSE.** Output that alerts the Ethernet controller that data is present on the active port. Connects directly to the carrier sense pin of the Ethernet controller. Changes sense depending on controller mode selected. Active low for Intel controller interface, active high for National, AMD, and Fujitsu interfaces. Can drive one TTL load.
$\overline{CDT}$	12	6	O	**COLLISION DETECT.** Output that indicates presence of a collision. Connects directly to the collision detect pin of the Ethernet controller. Changes sense depending on controller selected. Active low for Intel and Fujitsu controller interfaces, active high for National and AMD interfaces. Can drive one TTL load.

2.6 Mode Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TPE/$\overline{\text{AUI}}$	2	40	I/O	**PORT SELECT.** TTL input/LED output. If APORT is low, TPE/$\overline{\text{AUI}}$ is an input and selects either the TPE port (TPE/$\overline{\text{AUI}}$ high) or AUI port (TPE/$\overline{\text{AUI}}$ low). If APORT is high, the 82503 will indicate the port selected by driving TPE/$\overline{\text{AUI}}$ high (TPE) or low (AUI). TPE/$\overline{\text{AUI}}$ can drive an LED pull-up.
APORT	3	41	I	**AUTOMATIC PORT SELECTION.** TTL input. When high, 82503 will automatically select TPE or AUI port based on presence of valid link beats or frames on the TPE receive input. Mode selected will be indicated on TPE/$\overline{\text{AUI}}$.
APOL/XSQ	4	42	I	**AUTOMATIC POLARITY CORRECTION/EXTENDED SQUELCH ENABLE.** TTL input. When high, the extended squelch mode is disabled and automatic polarity correction is enabled. Both junctions (APOL and XSQ) are enabled when this pin is at a high impedance state. When low, both functions become disabled. The presence of a polarity fault on the TPE receive pair is indicated on POLED regardless of the state of APOL.
LID	38	32	I	**LINK INTEGRITY DISABLE.** TTL input. If high, link integrity function is disabled. If low, link integrity function is enabled.
CS0 CS1	5 8	43 2	I I	**CONTROLLER SELECT.** Selects the appropriate interface for the desired Ethernet controller. When CS0/1 = 0/0, supports Intel controllers. When CS0/1 = 0/1, supports Fujitsu controllers. When CS0/1 = 1/0, supports Western Digital and National controllers. When CS0/1 = 1/1, supports AMD controllers. (See Table 2.)
$\overline{\text{LPBK}}$	11	5	I	**LOOPBACK.** TTL input. An active low input signal that causes the 82503 to enter diagnostic loopback mode. The twisted pair or AUI medium will be removed from the circuit, thus isolating the node from the network. When not connected, this pin assumes the inactive (high) state. Diagnostic loopback does not disable the operation of the link integrity processor, link beat generator, or automatic port selection.
JABD	23	17	I	**JABBER DISABLE.** TTL input. When high, this pin disables the jabber function. When low, the jabber function is enabled and the device performs AUI or TP jabber protection for the active port. If this pin and TEST are asserted during a falling edge of RESET, the 82503 enters its low power mode; when either this pin or TEST deasserts, then the 82503 transitions to its normal operating mode.
TEST	19	13	I	**TEST MODE ENABLE.** TTL input. When TEST is high and RESET is deasserted, a customer test mode is directly accessed. When driven low, test mode is disabled. If this pin and JABD are asserted during a falling edge of RESET, the 82503 enters its low power mode; when either this pin or JABD deasserts, then the 82503 transitions to its normal operating mode.
RESET	22	16	I	**RESET.** TTL input. When high, resets internal circuitry. On the falling edge of RESET, either test mode or low power mode can be entered depending on the state of JABD and TEST.

2.7 LED Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TxLED	42	36	I/O	**TRANSMIT LED.** LED output. Indicates transmit status of the AUI or TPE port. Normally off (high) output. Turns on to indicate transmission. Flashes at a rate dependent on the level of transmit activity. Upon entering a customer test mode, this pin must be driven high either through an LED, or a resistor.
RxLED	43	37	I/O	**RECEIVE LED.** LED output. Indicates receive status of the AUI or TPE port. Normally off (high) output. Turns on to indicate reception. Flashes at a rate dependent on the level of receive activity. Upon entering a customer test mode, this pin must be driven high either through an LED, or a resistor.
COLED	44	38	I/O	**COLLISION LED.** LED output. Indicates collision status of the AUI or TPE port. Normally off (high) output. Turns on to indicate collision. Flashes at a rate dependent on the level of collision activity. This pin is also used to determine which customer test modes are entered.
LILED	41	35	O	**LINK INTEGRITY LED.** LED output. Normally on (low) output which indicates good link integrity on the TPE port during TPE mode. Remains on when link integrity function has been disabled. Turns off during AUI mode or when link integrity fails in TPE mode. Minimum off time is 100 ms, minimum on time is set by the link integrity function.
POLED	1	39	O	**POLARITY INDICATION.** LED output. If the 82503 detects that the receive TPE wires are reversed, POLED will turn on (low) to indicate the fault. POLED remains on even if APOL/XSQ is high and the 82503 has automatically corrected for the reversed wires.

NOTE:
1. The LED outputs have a weak pull-up capable of sourcing 500 μA. They can sink 10 mA while still meeting TTL levels. All LEDs can be used as indication pins if no LED is needed. Some of these outputs include pulse width conditioning, which should be accounted for in software.

3.0 82503 ARCHITECTURE

3.1 Clock Generation

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ±0.01% clock required by the IEEE 802.3 specification.

We recommend a crystal that meets the following specifications be used.

- Quartz Crystal
- 20 MHz ± 0.002% at 25°C
- Accuracy ± 0.005% over full operating temperature, 0°C to +70°C
- Parallel resonant with 20 pF Load Fundamental Mode
- Maximum Series Resistance: $R_{SERIES} = 30\Omega$

Several vendors have such crystals; either-off-the shelf or custom made. Two possible vendors are:

1. M-Tron Industries, Inc.
   Yankton, SD 57078
   Specifications;
   Part No. HC49 with 20 MHz, 50 PPM over 0°C to +70°C, and 20 pF fundamental load.
2. Crystek Corporation
   100 Crystal Drive
   Ft. Myers, FL 33907
   Part No. 013212

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics, therefore it is advisable to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 pF and 35 pF.

An external 20 MHz MOS-level clock may be applied to pin X1, if pin X2 is left floating.

3.2 Transmit Blocks

3.2.1 MANCHESTER ENCODER

The 20 MHz clock is used to Manchester-encode data on the TxD input. This clock is also divided by two to produce the 10 MHz clock the LAN controller needs for synchronizing its $\overline{RTS}$ and TxD signals.

Data encoding and transmission begins with $\overline{RTS}$ asserting. Since the first bit of a transmission is a 1, the first transition is always negative on the transmit outputs (TRMT or TD pins). Transmission ends when $\overline{RTS}$ deasserts. The last transition is always positive at the transmit outputs (TRMT or TD pins) and may occur at the center of the bit cell if the last data bit to be transmitted is a 1, or at the boundary of the bit cell if the last data bit to be sent is a 0.

Immediately after the end of a transmission, all signals on the RCV pair (when AUI mode is selected) are inhibited for 4 to 5 μs. This dead time is necessary for proper operation of the SQE (heartbeat) test.

3.2.2 AUI CABLE DRIVER

The AUI cable driver (TRMT pair) is a differential circuit, which interfaces to the AUI cable through a pulse transformer.

High voltage protection is achieved by using a transformer to isolate the transmit pins (TRMT pair) from the transceiver cable. The total transmit circuit inductance, including the 802.3 transceiver transformers, should be a minimum of 27 μH for Ethernet applications.

3.2.3 TWISTED PAIR CABLE DRIVER

The twisted pair line drivers (TD pairs) begin transmitting the serial Manchester bit stream 3 bit times after $\overline{RTS}$ is asserted. The line drivers use a predistortion algorithm to improve jitter performance for up to 100 meters of twisted pair cable. The line drivers reduce their drive level during the second half of "fat" (100 ns) Manchester pulses and maintain a full drive level during all "thin" (50 ns) pulses and during the first half of the "fat" pulses. This reduces line overcharging during "fat" pulses, a major source of jitter.

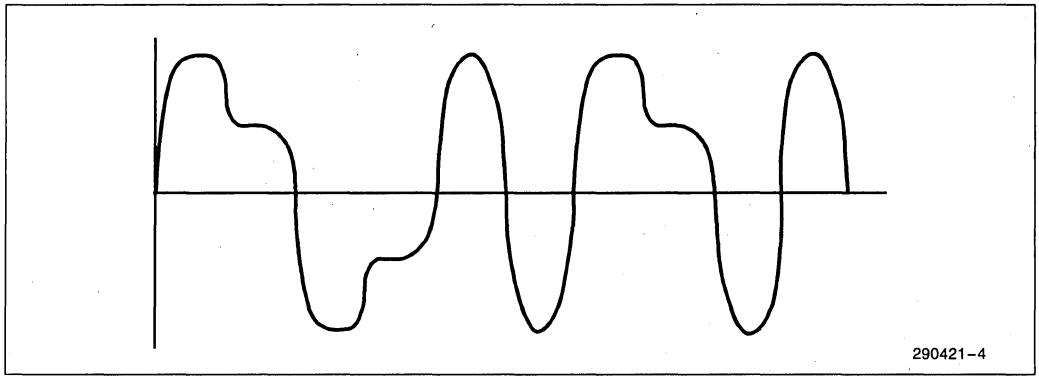


Figure 5. TPE Predistortion

3.3 Receive Blocks

3.3.1 MANCHESTER DECODER AND CLOCK RECOVERY

The 82503 performs Manchester decoding and timing recovery of the incoming data in AUI and TPE modes.

The Manchester-encoded data stream is decoded to separate the Receive Clock ($\overline{RxC}$) and the Receive Data (RxD) from the differential signal. The 82503 uses an advanced digital technique to perform the decoding function. The use of digital circuitry instead of analog circuitry (e.g., a phase-lock loop) to perform the decoding ensures that the decoding function is less sensitive to variations in operating conditions.

A high-resolution phase reference is used to digitize the phase of the incoming data bit-center transition. The digitizer has a phase resolution of 1/32 of a bit time.

The digitized phase is filtered by a digital low-pass filter to remove rapid phase variations, i.e., phase jitter. Slow phase variations, such as those caused by small differences between the data frequency and the clock frequency, are not filtered by the low-pass filter.

The $\overline{RxC}$ generator digitally sets the phases of the two $\overline{RxC}$ transitions to respectively lead and lag the bit-center transition by ¼ bit time. $\overline{RxC}$ is used to recover RxD by sampling the incoming data with an edge-triggered flip-flop.

Lock is achieved by reducing the time constant of the digital filter to zero at the start of a new frame. Any uncertainty in the bit-center phase of the first transition that is caused by jitter is subsequently removed by gradually increasing the filter time constant during the following preamble. By that time, the phase of the bit center is output by the filter, and lock is achieved. Lock is achieved within the first 14 bit times as seen by the AUI inputs. The maximum bit-cell timing distortion (jitter) tolerated by the Manchester decoder circuitry is ±12 ns (preamble), ±18 ns (data) for AUI, and ±13.5 ns for TPE (data and preamble).

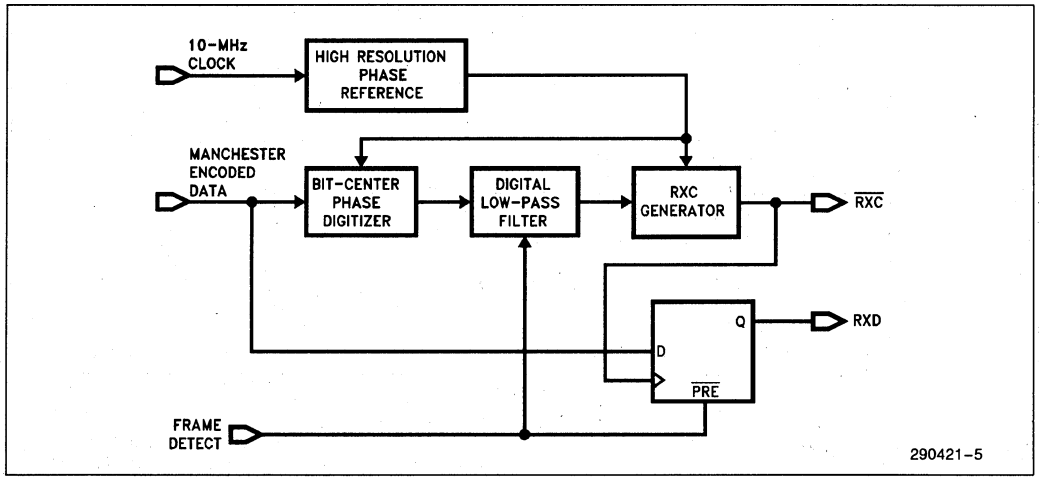


Figure 6. Manchester Decoder and Clock Recovery

3.3.2 AUI RECEIVE AND COLLISION BUFFERS

The AUI receive and collision inputs are driven through isolation transformers to provide high voltage protection and DC common mode voltage rejection. The incoming signals are converted to digital levels and passed to the Manchester decoder and collision detection circuitry.

3.3.3 AUI RECEIVE AND COLLISION SQUELCH CIRCUITS

Both the receive (RCV) and collision (CLSN) pairs have the following squelch characteristics.

- The squelch circuits are turned on at idle.
- A pulse is rejected if the peak differential voltage is more positive than −160 mV regardless of pulse width.
- A pulse is considered valid if its peak differential voltage is more negative than −300 mV and its width, measured at −285 mV, is greater than 25 ns.
- The squelch circuits are disabled by the first valid negative differential pulse on either the AUI receive (RCV) or the AUI collision (CLSN) pair.
- If a positive differential pulse occurs on either the AUI receive or collision pairs for greater than 160 ns, End of Frame (EOF) is assumed and the squelch circuitry is turned on.

3.3.4 TPE RECEIVE BUFFER

The TPE receive pins (RD and $\overline{RD}$) are connected to the twisted pair medium through an analog front end. The analog front end contains the line coupling devices and EMI filters necessary to conform to the 10BASE-T standards and local RF regulations. The input differential voltage range for the TPE receiver is greater than 500 mV and less than 3.1V differential.

3.3.5 TPE RECEIVE SQUELCH CIRCUITS

The TPE receive buffer distinguishes valid receive differential data, link test pulses, and the idle condition according to the requirements of the 10BASE-T standard. Signals at the output of the EMI filter (thus at the RD and $\overline{RD}$ pair) are rejected as follows:

- All differential pulses of peak magnitude less than 300 mV are rejected.
- All continuous sinusoids with a differential amplitude less than 6.2 V_{PP} and a frequency less than 2 MHz are rejected.
- All sine waves of single cycle duration starting with phase 0° or 180° that have an amplitude less than 6.2 V_{PP}, and a frequency of 2 MHz to 16 MHz are rejected, if the single cycle is preceeded and followed by 4 bit times of silence (i.e., a signal less than 300 mV).

3.3.6 TPE Extended Squelch Mode

By placing the 82503 into TPE extended squelch mode, the 82503 can support cable lengths greater than the 100m specified in the 10Base-T IEEE standard (802.3i-1990). The squelch thresholds for the signals at the RD/$\overline{RD}$ pair are typically reduced by 4.5 dB. This allows Grade 5 twisted-pair cable to be used to overcome attenuation and multipair crosstalk for cable lengths up to 200 meters.

TPE extended squelch mode is enabled by presenting a high-impedance (>100 KΩ) at the APOL/XSQ pin. This can be done by floating the APOL/XSQ pin, tying APOL/XSQ low through a 100 KΩ resistor, or driving APOL/XSQ with a three-state buffer. When driven high or low using a TTL driver or a low impedance pull-up or pull-down (<2 KΩ) extended squelch is disabled and the driven level at the APOL/XSQ pin determines the state of the polarity-correction function (APOL/XSQ = 1 enables polarity correction, APOL/XSQ = 0 disables polarity correction). The TPE extended squelch feature is transparent to previous steppings of the 82503. Polarity correction is always enabled when the TPE extended-squelch feature is enabled (APOL/XSQ = Z).

The APOL/XSQ pin senses a high-impedance state by an active-polling circuit implemented at the pin. Two small polling devices attempt to pull the APOL/XSQ pin up to V_{CC} and down to V_{SS}. If the pin is in a high-impedance state, the devices will be successful in pulling the APOL/XSQ pin high and low. If the pin is driven high or low, the polling devices will not be able to successfully pull the pin in the opposite direction. In this way, an internal state machine can correctly determine one of three states of the APOL/XSQ pin. The pin is polled every 25.6 μs.

3.4 Collision Detection

3.4.1 AUI COLLISION DETECTION

Collision detection in the AUI mode is performed by the attached transceiver, and signalled to the 82503 on the CLSN pair. A 10 MHz +25%, or −15%, square wave with transition times between 35 ns and 70 ns indicates the collision. The 82503 reports this to the LAN controller on the $\overline{CDT}$ pin.

3.4.2 TPE COLLISION DETECTION

Collision detection in the TPE mode is indicated by simultaneous transmission and reception on the twisted pair link segment. The $\overline{CDT}$ signal is asserted for the duration of both $\overline{RTS}$ and the presence of received data; $\overline{CRS}$ is asserted for the duration of either $\overline{RTS}$ or the presence of received data. During a collision, the source of RxD will be the received data. If the received data stream ends before the transmit data stream, the RxD source will be changed to transmit data stream until it ends.

3.5 Link Integrity

The 82503 supports the link integrity function as defined by 10BASE-T. During long periods of idle on the transmitter, link test pulses will be transmitted on to the twisted pair medium as an indication to the remote MAU that the link is good. These pulses will be transmitted 8 ms to 24 ms after the end of the last transmission or link test pulse.

The link integrity function continuously monitors activity on the receive circuit. If neither valid data nor link test pulses are received, the link integrity processor declares the link bad, and disables transmission and reception on the media, loopback, and the SQE test function. Transmission of link test pulses and monitoring receive activity are not affected. The idle time required for the link integrity processor to determine the link is bad is 50 ms to 150 ms.

Once a frame or a sequence of 2 to 10 valid consecutive link test pulses are detected, the Link Integrity Processor declares the link is good, and reconnects the transmitter and receiver.

The link integrity function can be disabled by driving the LID pin high or by disabling automatic port selection (APORT = 0) and selecting the AUI port. This option is intended primarily for use with pre-10BASE-T networks.

3.6 Jabber Function

The 82503 contains a jabber timer to implement the jabber function. If a transmission continues beyond the limits specified, the jabber function inhibits further transmission and asserts the collision indicator, $\overline{CDT}$. The limits for jabber transmission are 20 ms to 150 ms in TPE Mode, and 8 ms to 16 ms in AUI mode. For both AUI and TPE mode, the transmission inhibit period extends until the 82503 detects sufficient idle time (between 250 ms and 750 ns) on the $\overline{RTS}$ signal. The jabber function can be disabled by driving the JABD high.

In TPE mode the link integrity function continues to operate even if the jabber function is inhibiting transmission. Link test pulses continue to be sent and the receive circuit continues to be monitored. Additionally, the link integrity function reconnects to a restored link without waiting for the transmit input to go idle when the jabber function is inhibiting transmission.

3.7 TPE Loopback

In TPE mode the 82503 implements the transmit to receive loopback (DO to DI) mode specified in the 10BASE-T standard. This mode loops back transmitted data through the receive path.

This function is required to maintain full compatibility with coax MAUs where the data loopback is a natural result of the architecture.

The transmit to receive loopback function is disabled when the jabber function or link integrity function is inhibiting transmission.

3.8 SQE Test Function

The 82503 supports the SQE test function when in TPE mode or in Diagnostic Loopback mode. The 82503 will assert its $\overline{CDT}$ pin within 0.6 μs to 1.6 μs after the end of a transmission, and it will remain asserted for 5- to 15-bit times. If the 82503 is in the TPE mode and is not in diagnostic loopback mode, the link integrity function will disable the SQE test function when it detects a bad link.

3.9 Port Selection

The 82503 features both manual and automatic port selection. To enable automatic port selection, connect APORT to V_{CC}. The 82503 then starts in TPE mode and monitors link integrity. If the link is good, the 82503 stays in TPE mode and pulls TPE/$\overline{AUI}$ high to indicate that the TPE port was selected. If link integrity fails, the 82503 switches to AUI mode and pulls TPE/$\overline{AUI}$ low to indicate that the AUI port is now active. TPE/$\overline{AUI}$ can drive an LED to indicate port selection (on for AUI, off for TPE mode). Note that LILED will be on if TPE mode is selected and off if AUI mode is selected. If link integrity is disabled while automatic port selection is enabled, the 82503 defaults to TPE mode. If the 82503 changes ports while $\overline{RTS}$ is active, transmission is terminated with an End of Frame marker on the old port. Transmission of the remaining packet fragment is not allowed on the new port. Transmissions will begin with a complete data packet.

The port can be manually selected by driving APORT low. TPE/$\overline{AUI}$ = 0 selects AUI mode, and TPE/$\overline{AUI}$ = 1 TPE mode. When the port is manually selected, the circuitry for the unused port is powered down. Changing ports requires 100 μs to allow the circuitry for the new port to resume normal operation.

Table 1. Port Selection

Configuration			State
LID	APORT	TPE/$\overline{AUI}$	
X	0	0	AUI (TPE Port Powered Down)
X	0	1	TPE (AUI Port Powered Down)
0	1	X*	Automatic Port Selection
1	1	X*	TPE

NOTE:
*TPE/$\overline{AUI}$ is an output pin when APORT = 1.

3.10 LED Description

The 82503 supports six LED pins to indicate the status of important states; TPE/$\overline{AUI}$, TxLED, POLED, LILED, RxLED, COLED. Each pin is capable of directly driving an LED.

3.10.1 TPE/$\overline{AUI}$

When automatic port selection is enabled (APORT is high), TPE/$\overline{AUI}$ becomes an LED output and turns off if TPE mode is selected and on if AUI mode is selected.

3.10.2 TxLED

Transmit status. This LED is normally off and flashes at 2.5 Hz, 5 Hz, and 10 Hz to indicate respectively a low, medium, and high rate of transmit activity.

3.10.3 RxLED

Receive LED. This LED is normally off and flashes at 2.5 Hz, 5 Hz, and 10 Hz to indicate respectively a low, medium, and high rate of receive activity.

3.10.4 COLED

Collision LED. This LED is normally off and flashes at 2.5 Hz, 5 Hz, and 10 Hz to indicate respectively a low, medium, and high rate of collision activity.

3.10.5 POLED

Polarity Fault. This LED is normally off and turns on to indicate a polarity fault in the receive pair of the 10BASE-T link. Operation of this pin is not affected by the state of the polarity correction function (APOL/XSQ = X).

3.10.6 LILED

Link Integrity status. When Aport is enabled (APORT = 1), this LED is normally on (driven low) to indicate the presence of a valid 10BASE-T link when the TPE port is active. The LED will turn off (driven high) when the link fails. When link integrity is disabled (LID = 1) while APORT is enabled (APORT = 1) this LED is turned on (driven low). If APORT is disabled (APORT = 0) and the AUI port is manually selected (TPE/$\overline{AUI}$ = 0) the LED output is tristated.

3.11 Polarity Switching

In TPE mode, the 82503 monitors receive link beats and end-of-frame delimiters for a possible receiver

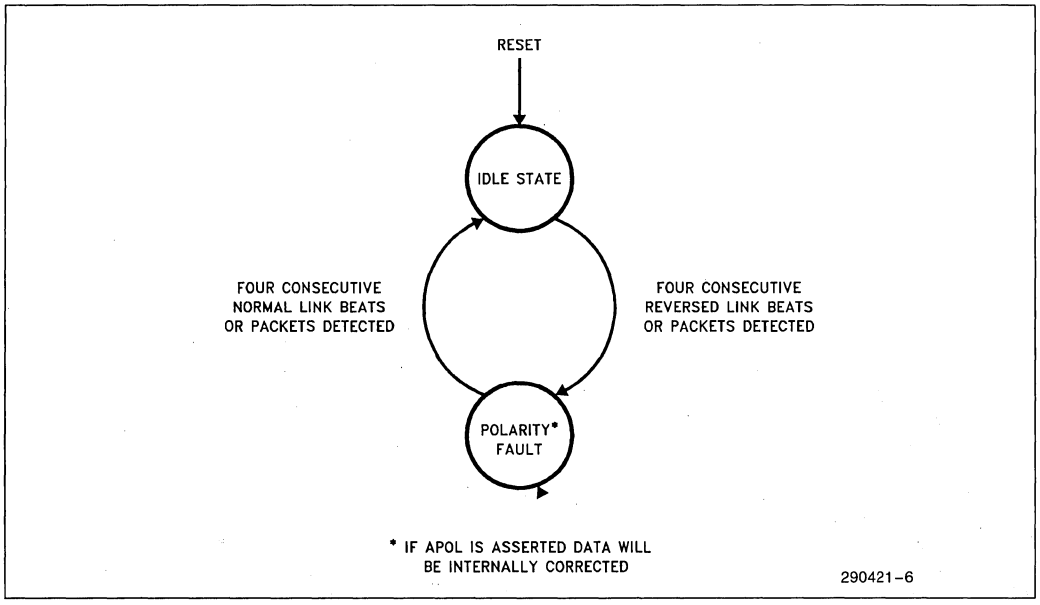


Figure 7. Polarity Fault State Diagram

polarity error due to crossed wires. If Pin 4 of the 82503 is high and the TPE receive pins are reversed, the 82503 will correct the error by reversing the signals internally, and turn POLED on (low) to indicate that the fault has been detected and corrected. The polarity correction function is defeatable by driving the APOL/XSQ input low. However, the polarity fault will continue to be indicated on the POLED.

3.12 Controller Interface

Connecting the 82503 to one of the Intel Ethernet controllers (82586, 82590, 82593, 82596) requires no additional components. Simply drive CS0 and CS1 both low, and connect $\overline{\text{TxC}}$, TxD, $\overline{\text{RTS}}$, $\overline{\text{RxC}}$, RxD, $\overline{\text{CRS}}$, $\overline{\text{CDT}}$, and $\overline{\text{LPBK}}$ to the corresponding controller pins.

The 82503 also works with other Ethernet controllers without additional components, including the National Semiconductor 8390 and 83932 (SONIC), Western Digital 83C690, Fujitsu 86950 (Etherstar), depending on the state of and CS0 and CS1 inputs.

The interface of the 82503 to the AMD 7990 (LANCE) requires external logic to control the $\overline{\text{LPBK}}$ pin of the 82503. Note that when an AMD LAN controller is used to interface to the 82503, the $\overline{\text{LPBK}}$ pin of the 82503 becomes active high. That is, the 82503 enters diagnostic loopback mode when $\overline{\text{LPBK}}$ pin is high and is in normal operation mode when $\overline{\text{LPBK}}$ pin is low.

The logic sense of the 82503 controller pins will change and should be connected to the controller pins according to the following table.

Table 2. Controller Interface Selection

82503 Pin	Intel Controller 825XX		National, WD Controllers 8390, 83C690, 83832 (SONIC)		AMD Controller 7990 (LANCE), 79C900 (ILACC)		Fujitsu Controllers 86950 (Etherstar)	
CS0(1)	0		1		1		0	
CS1	0		0		1		1	
Pin	**Pin**	**Sense**	**Pin**	**Sense**	**Pin**	**Sense**	**Pin**	**Sense**
$\overline{TxC}$	$\overline{TxC}$	Low	TXC	High	TCLK	High	TCKN	Low
TxD	TxD	High	TXD	High	TX	High	TXD	High
$\overline{RTS}$	$\overline{RTS}$	Low	TXE	High	TENA	High	TEN	High
$\overline{RxC}$	$\overline{RxC}$	Low	RXC	High	RCLK	High	RCKN	Low
RxD	RxD	High	RXD	High	RX	High	RXD	High
$\overline{CRS}$	$\overline{CRS}$	Low	CRS	High	RENA	High	XCD	High
$\overline{CDT}$	$\overline{CDT}$	Low	COL	High	CLSN	High	XCOL	Low
$\overline{LPBK}$	$\overline{LPBK}$	Low	LPBK	High	(Note 2)		LPBK	High

NOTES:
1. CS0 and CS1 are intended to be static pins only. Switching CS0 and CS1 during network reception or transmission will produce unpredictable results.
2. Refer to Section 3.12.

4.0 RESET, LOW-POWER AND TEST MODES

4.1 Reset

When RESET is asserted the device resets its internal circuits. RESET is required after power up, and before data can be transmitted or received. It is allowed any time thereafter, but any existing receive or transmit activity will be lost, and all state machines (Link integrity, Jabber, and Polarity Correction) return to their initial states. TEST must be held low for a device reset to prevent entering a test for low power mode. During RESET, $\overline{TxC}$ continues without interruption (in Fujitsu mode both $\overline{TxC}$ and $\overline{RxC}$ run continuously).

4.2 Low Power and High Impedance Modes

When RESET is deasserted while both TEST and JABD are held high, the 82503 enters its low power and high impedance modes. The majority of internal circuitry is powered down, and many inputs and outputs are three-stated. These pins are: APORT, APOL/XSQ, LID, TPE/$\overline{AUI}$, POLED, LILED, $\overline{RTS}$, $\overline{LPBK}$, RxD, TxD, $\overline{CRS}$ and $\overline{CDT}$. When either JABD or TEST is deasserted, the device begins a power on cycle which lasts less than 1 ms. During this cycle, all inputs are ignored and all transmissions are disabled. If $\overline{RTS}$ is active when the device returns to normal operation, the remainder of that packet fragment is not transmitted. Normal transmissions are resumed at the start of the first complete data packet.

4.3 Diagnostic Loopback

This is a diagnostic test mode to help in fault isolation and detection. Serial NRZ data input on TxD is Manchester encoded and then looped back through the Manchester decoder (TMD) appearing at the RxD output. Collision detect is asserted following each transmission to simulate the SQE test. Output cable drivers and input amplifiers are disconnected from the controller interface pins while in this mode. The link integrity and polarity fault detection functions are not inhibited by diagnostic loopback mode. If otherwise enabled, they continue to function.

4.4 Customer Test Mode (Continuous AUI/TPE Transmit)

In this mode, the 82503 continuously transmits data without the intervention of a LAN controller. Transmission is at 10 MHz (11-bit pattern), and can occur on either the TPE or AUI port. The jabber timer is disabled in this mode, allowing users to easily test the 10BASE-T harmonic content specification and the quality of their analog front end design without complex software exercisers.

Customer Test Mode—and Low Power Mode are selected at the deassertion of RESET as shown in the following table. (Note that the 82503 must be in non-loopback mode before it can enter the customer test mode.)

Table 3. Test and Low Power Mode Selection

RESET	TEST	JABD	TxLED(1)	RxLED(1)	COLED(1)	Mode Selected
↓	0	X	X	X	X	Normal Mode
↓	1	0	1	1	1	Cont Tx 10 MHz
↓	1	1	X	X	X	Low Power

NOTE:
1. A standard LED connection to these pins is sufficient to pull them to a logic 1.

The port on which the continuous transmit appears is determined by the APORT and TPE/$\overline{AUI}$ pins. If automatic port selection is enabled (APORT = 1) then the TPE port broadcasts the continuous transmit. If manual port selection is enabled (APORT = 0), then TPE/$\overline{AUI}$ selects the port (1 for TPE, 0 for AUI). Test mode is disabled when TEST is deasserted and the device is reset.

5.0 APPLICATION EXAMPLE

5.1 Introduction

The 82503 is designed to work directly with the Intel LAN controllers (82586, 82590, 82593, and 82596), as well as AMD's Am7990, National Semiconductor's 8390, Western Digital's 82C690, and Fujitsu's 86950. The serial interface signals connect directly between one of the aforementioned LAN controllers and the 82503 without the need for external logic.

This example is targeted toward interfacing the 82503 to the Intel 82596 in a two-port (TPE/AUI) application.

5.2 Design Guidelines

AUI Pulse Transformer

In order to meet the 16V fault tolerance specification of 802.3 a pulse transformer is recommended for the transmit, receive and collision pairs. The transformer should be placed between the TRMT, RCV, and CLSN pairs of the 503, and the DO, DI, and CI pairs respectively, of the AUI (DB-15 connector). The pulse transformer should have a parallel inductance of 75 μH minimum (100 μH recommended).

Several vendors stock such transformers. Two possible vendors are:

1. Pulse Engineering (P/N PE-64103)
2. Valor Electronics (P/N LT6003)

Terminating Resistors

The terminating resistors used across the receive and collision pairs are recommended to be 78.7 Ω ±1%.

Analog Front-End

The 82503 provides six TPE pins (TDH, $\overline{TDH}$, TDL, $\overline{TDL}$, RD, and $\overline{RD}$) that connect to the Analog Front End through a resistor summing network (Figure 7). AFE solutions can be made discretely or purchased from several manufacturers. Two different solutions are described in Application Note 356. The example shown here uses a Pulse Engineering AFE package PE65434 which includes EMI filter, isolation transformer, and common mode choke. The output of the AFE connects directly to the 10BASE-T connector (RJ-45).

Decoupling

It is recommended that 0.01 μF X7R and 0.001 μF NPO decoupling capacitors be placed between the V_{CCA} and V_{CCD} of the 82503 to V_{SSA} and V_{SSD}.

Clock Generation

The clock input to the 82503 can be from a clock oscillator or a crystal. If a clock oscillator is used, X1 should be driven, and X2 left floating. If a crystal oscillator is used, refer to Section 3.1 for crystal specifications.

A complete 82596/82503 TPE/AUI Ethernet Solution is shown at the end of this section.

5.3 Layout Guidelines

General

The analog section, as well as, the entire board itself should conform to good high-frequency practices and standards to minimize switching transients and parasitic interaction between various circuits. To achieve this, the following guidelines are presented.

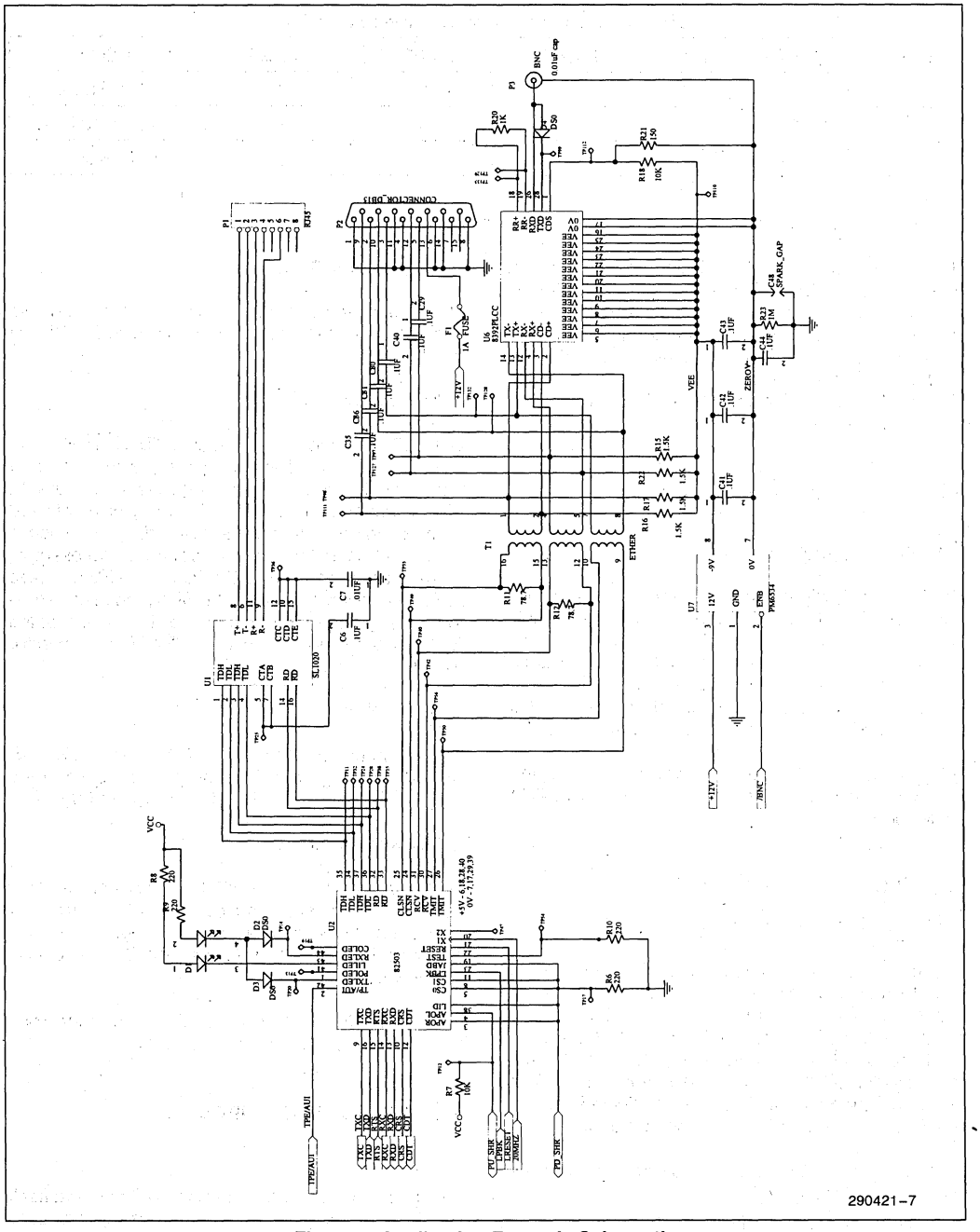


Figure 8. Application Example Schematic

Make power supply and ground traces as thick as possible. This will reduce high-frequency cross coupling caused by the inductance of thin traces.

Connect logic and chassis ground together.

Separate and decouple all of the analog and digital power supply lines.

Close signal paths to ground as close as possible to their sources to avoid ground loops and noise cross coupling.

Use high-loss magnetic beads on power supply distribution lines.

Crystal

The crystal should be adjacent to the 82503 and trace lengths should be as short as possible. The X1 and X2 traces should be symmetrical.

82503 Analog Differential Signals

The differential signals from the 82503 to the transformers, analog front end, and the connectors should be symmetrical for each pair and as short as possible. Differential signal layout should be performed to a characteristic impedance of 78Ω (for AUI) or 100Ω (for TPE).

As a general rule, the trace widths should be one to three times the distance between the PCB layers to eliminate excessive trace inductance.

The differential signals should also be isolated from the high speed logic signals on the same layer as well as on any sublayers of the PCB.

Group each of the circuits together, but keep them separate from each other. Separate their grounds.

In layout, the circuitry from the connectors to the filter network, should have the ground plane removed from beneath it. This will prevent ground noise from being induced into the analog front end.

All trace bends should not exceed 45 degrees.

6.0 PACKAGE THERMAL SPECIFICATIONS

The 82503 Dual Serial Transceiver is specified for operation when case temperature (T_C) is within the range of 0°C to +85°C. The case temperature can be measured in any environment, to determine if the 82503 is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The acceptable operating ambient temperature (T_A) is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from the θ_{ja} and θ_{jc} from the following equations:

$$T_J = T_C + P \times \theta_{jc}$$
$$T_J = T_A + P \times \theta_{ja}$$
$$T_A = T_C - P \times (\theta_{ja} - \theta_{jc})$$

Values for θ_{ja} and θ_{jc} are given in Table 4 for the 44-lead PLCC and 44-lead QFP packages. Various values for θ_{ja} at different airflows. Table 5 shows the maximum T_A allowable (without exceeding T_C) at various airflows.

Table 4. Thermal Resistance (°C/Watt) θ_{jc} and θ_{ja}

Package	θ_{jc}	θ_{ja} vs Airflow—ft/min (m/s)					
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
44-Lead PLCC	19	57	48	43	41	39	37
44-Lead QFP	26	98	94	78	70	66	64

Table 5. Maximum T_A at Various Airflows

Package	θ_{ja} vs Airflow—ft/min (m/s)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
44-Lead PLCC	66	71	73	74	75	76
44-Lead QFP	49	51	59	63	65	66

7.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Case Temperature Under Bias . . . . . 0°C to +85°C
Storage Temperature . . . . . −65°C to +140°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +6.0V(1)

DC CHARACTERISTICS (T_C = 0°C to +85°C, V_{CC} = 5V ±5%, V_{CCA} = 5V ±5%)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}(TTL)(2)	Input Low Voltage	−0.3	0.8	V	
V_{IH}(TTL)(2)	Input High Voltage	2.0	V_{CC}	V	
I_{LI}(2)	Input Leakage Current		±10	μA	0.0V ≤ V_I ≤ V_{CC}, RESET = 1
V_{OL}(MOS)(3)	Output Low Voltage		0.45	V	I_{OL} = 4 mA
V_{OH}(MOS)	Output High Voltage	3.9		V	I_{OH} = −500 μA
V_{OL}(LED)(4)	Output Low Voltage		0.45	V	I_{OL} = 10 mA
V_{OH}(LED)	Output High Voltage	3.9		V	I_{OH} = −500 μA
I_{LP}	Leakage Current, Low Power Mode(5)		±10	μA	0.0V ≤ V_I ≤ V_{CC}
R_{DIFF}	Input Differential Resistance(6)	10		kΩ	dc
V_{IDF}(TPE)(7)	Input Differential Accept Input Differential Reject Input Differential Accept (XSQ) Input Differential Reject (XSQ)	±0.500 (Note 8)	±3.1 ±0.300 ±3.1 ±0.180	V_P V_P V_P V_P	5 MHz ≤ f ≤ 10 MHz
R_S(TPE)(8)	Output Source Resistance	6	13	Ω	$\|I_{LOAD}\|$ = 25 mA
V_{IDF}(AUI)(9)	Input Differential Accept Input Differential Reject	±0.300	±1.5 ±0.160	V_P V_P	
V_{ODF}(AUI)(10)	Output Differential Voltage	±0.450	±1.20	V	

NOTES:
1. The voltage levels for RCV, CLSN, and RD pairs are −0.75V to +8.5V.
2. TTL Input Pins: TxD, $\overline{RTS}$, TPE/$\overline{AUI}$, APORT, APOL/XSQ, LID, CS0, CS1, $\overline{LPBK}$, JABD, TEST, RESET.
3. MOS Output Pins: $\overline{TxC}$, RxD, $\overline{RxC}$, $\overline{CRS}$, $\overline{CDT}$.
4. LED Pins: TPE/$\overline{AUI}$, TxLED, RxLED, COLED, POLED, LILED. V_{OL} measured 10 ns after falling edge of $\overline{TxC}$.
5. Pins: APORT, APOL/XSQ, LID, TPE/$\overline{AUI}$, POLED, LILED, $\overline{RTS}$, $\overline{LPBK}$, RxD, TxD, $\overline{CRS}$, $\overline{CDT}$, CS0, CS1, JABD, TEST, and RESET.
6. Pins: RD to $\overline{RD}$, RCV to $\overline{RCV}$, and CLSN to $\overline{CLSN}$.
7. TPE Input Pins: RD, and $\overline{RD}$. See Section 3.3.4 and Section 3.3.5.
8. Typically it is −4.5 dB below normal squelch level.
9. TPE Output Pins: TDH, $\overline{TDH}$, TDL, and $\overline{TDL}$. R_S measures V_{CC} or V_{SS} to Pin.
10. AUI Input Pins: RCV, and CLSN pairs.
11. AUI Output Pins: TRMT pair.

DC CHARACTERISTICS (T_C = 0°C to +85°C, V_{CC} = 5V ±5%, V_{CCA} = 5V ±5%) (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{OSC}(AUI)	AUI Output Short Circuit Current		±150	mA	Short Circuit to V_{CC} or GND
V_U(AUI)	Output Differential Undershoot		−100	mV	
V_{ODI}(AUI)	Differential Idle Voltage(11)		±40	mV	
I_{CC}(HOT)	Power Supply Current(12)		65	mA	APORT = 1
I_{CC}	Power Supply Current		75	mA	APORT = 1
I_{CC}	Power Supply Current		60	mA	APORT = 0
I_{CCSB}	Standby Supply Current(13)		1	mA	Low Power Mode, 20 μA Typical
PD (HOT)	Power Dissipation(12)		0.38	W	APORT = 1, Continuous Transmission on AUI
PD	Power Dissipation		0.40	W	APORT = 1, Continuous Transmission on AUI
PD_{SB}	Standby Power Dissipation(13)		5.25	mW	Low Power Mode, 105 μW Typical
C_{IN}(14)	Input Capacitance		10	pF	at f = 1 MHz

1

NOTES:
11. Measured 8.0 μs after last positive transition of data packet.
12. I_{CC} HOT measurements made at T_C = +85°C. Additionally, TRMT, $\overline{\text{TRMT}}$, TDH, $\overline{\text{TDH}}$, TDL, $\overline{\text{TDL}}$ are loaded with 20 pF and load resistors removed.
13. Pins CS0 and CS1 connected to V_{CC} or V_{SS} through a 2.5 kΩ (or less) resistor. I_{CCSB} is typically at 20 μA after 30s from power down assertion—not tested.
14. Characterized, not tested. (Controller interface and mode pins only.)

AC TIMING CHARACTERISTICS

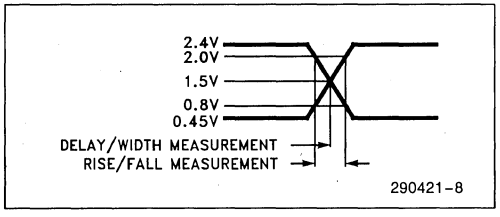


Figure 9. MOS Input Voltage Levels (TTL Compatible) for Timing Measurements (TxD, $\overline{\text{RTS}}$, TPE/$\overline{\text{AUI}}$, APORT, APOL/XSQ, LID, $\overline{\text{LPBK}}$, JABD, TEST, and RESET).

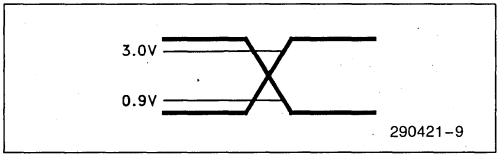


Figure 10. Voltage Levels for MOS Level Output Timing Measurements ($\overline{\text{TxC}}$, RxD, $\overline{\text{RxC}}$, $\overline{\text{CRS}}$, and $\overline{\text{CDT}}$).

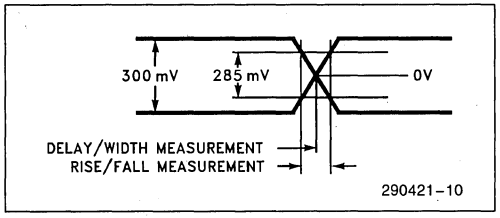


Figure 11. Voltage Levels for Differential Input Timing Measurements (RCV and CLSN Pairs).

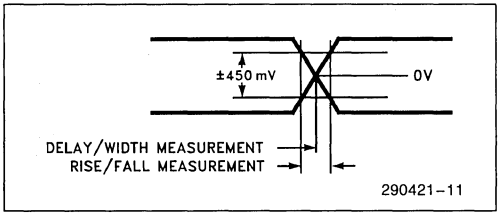


Figure 12. Voltage Levels for TRMT Pair Output Timing Measurements.

AC TIMING CHARACTERISTICS (Continued)

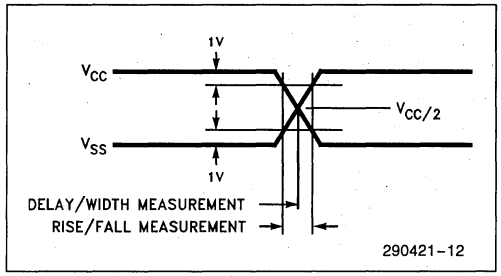


Figure 13. Voltage Levels for TDH, TDL, $\overline{TDH}$, and $\overline{TDL}$.

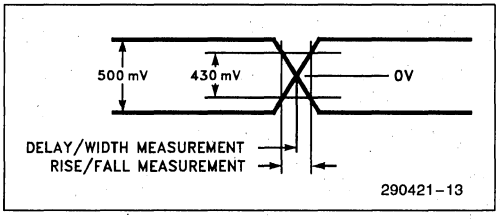


Figure 14. Voltage Levels for Differential Input Timing Measurements (RD Pair).

AC MEASUREMENT CONDITIONS

1. T_C = 0°C to +85°C, V_{CC} = 5V ±5%.
2. The AC MOS, TTL and differential signals are referred to in Figures, 8, 9, 10, 11, 12, and 13.
3. AC loads
   a. MOS: 20 pF total capacitance to ground.
   b. AUI Differential: a 10 pF total capacitance from each terminal to ground and a load resistor of 78Ω ±1% in parallel with a 27 μH ±1% inductor between terminals.
   c. TPE: 20 pF total capacitance to ground.
4. All parameters become valid 200 μs after the supply voltage and input clock has stabilized, or after RESET deasserts.

CLOCK TIMING (15)

Symbol	Parameter	Min	Typ	Max	Units
t_1	X1 Cycle Time	49.995		50.005	ns
t_2	X1 Fall Time			5	ns
t_3	X1 Rise Time			5	ns
t_4	X1 Low Time	15			ns
t_5	X1 High Time	15			ns

NOTE:
15. Refers to External Clock Input.

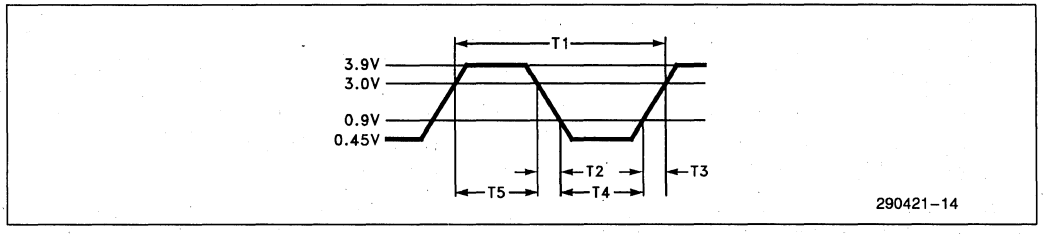


Figure 15. X1 Input Voltage Levels for Timing Measurements

Controller Interface Timings (Intel Mode)

TRANSMIT TIMINGS (Intel)

Symbol	Parameter	Min	Typ	Max	Units
t_{10}	$\overline{TxC}$ Cycle Time	99.99		100.01	ns
t_{11}	$\overline{TxC}$ High/Low Time	40			ns
t_{12}	$\overline{TxC}$ Rise/Fall Time			5	ns
t_{13}	TxD and $\overline{RTS}$ Rise/Fall Time			10	ns
t_{14}	TxD Setup Time to $\overline{TxC}\downarrow$	45			ns
t_{15}	TxD Hold Time from $\overline{TxC}\downarrow$	0			ns
t_{16}	$\overline{RTS}$ Setup Time to $\overline{TxC}\downarrow$	45			ns
t_{17}	$\overline{RTS}$ Hold Time from $\overline{TxC}\downarrow$	0			ns

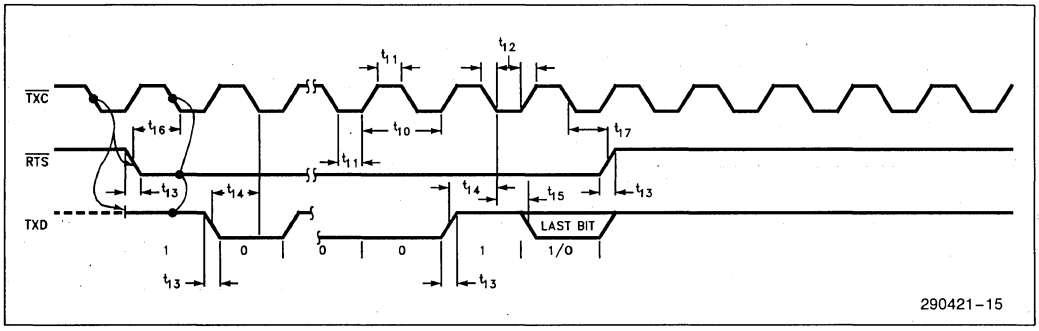


Figure 16. Transmit Timing (Intel)

RECEIVE TIMING (Intel)

Symbol	Parameter	Min	Typ	Max	Units
t_{20}	$\overline{RxC}$ Cycle Time	96	100		ns
t_{21}	$\overline{RxC}$ High Time	36			ns
t_{22}	$\overline{RxC}$ Low Time	40			ns
t_{23}	$\overline{RxC}$ Rise/Fall Time			5	ns
t_{24}	$\overline{RxC}$ Delay from $\overline{CRS}$ ↓		1100	1400	ns
t_{25}	RxD Rise/Fall Time			5	ns
t_{26}	RxD Setup from $\overline{RxC}$ ↓	30			ns
t_{27}	RxD Hold from $\overline{RxC}$ ↓	30			ns
t_{28}	$\overline{CRS}$ Deassertion Hold Time from $\overline{RxC}$ High	10		40	ns

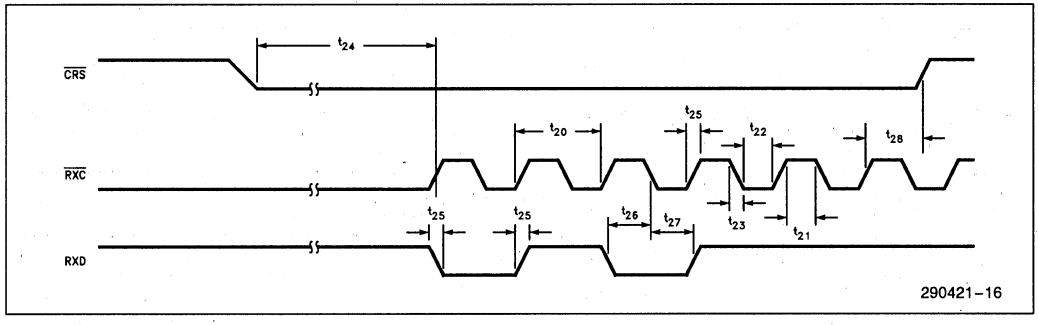


Figure 17. Receive Timing (Intel)

Controller Interface Timings (National Mode)

TRANSMIT TIMINGS (National)

Symbol	Parameter	Min	Typ	Max	Units
t_{30}	TXC Cycle Time(16)	99.99		100.01	ns
t_{31}	TXC High/Low Time	40	50		ns
t_{32}	TXC Rise/Fall Time at 20% to 80%			5	ns
t_{33}	TXD Setup Time to TXC ↑	20			ns
t_{34}	TXD Hold Time from TXC ↑	0			ns
t_{35}	TXE Setup Time to TXC ↑	20			ns
t_{36}	TXE Hold Time from TXC ↑	0			ns

NOTE:
16. All delay and width measurements on TxC are made at 1.5V.

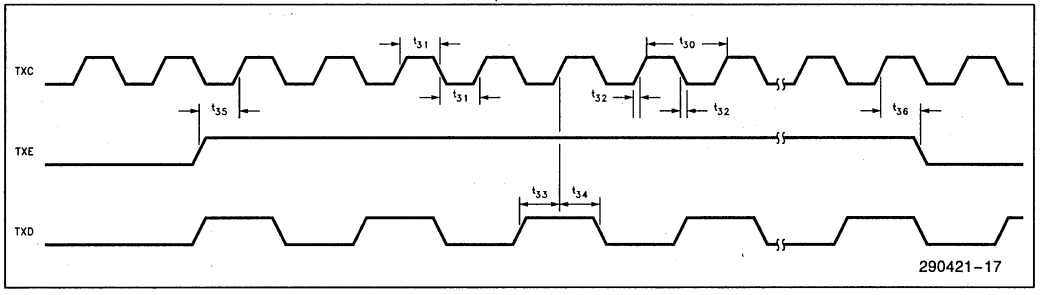


Figure 18. Transmit Timing (National)

RECEIVE TIMINGS (National)

Symbol	Parameter	Min	Typ	Max	Units
t_{40}	RxC Cycle Time	96	100		ns
t_{41}	RxC High/Low Time(17)	40	50	60	ns
t_{42}	RxC Rise/Fall Time at 20% to 80%			5	ns
t_{43}	RXD Rise/Fall Time at 20% to 80%			5	ns
t_{44}	RXD Setup Time to RxC ↑	30			ns
t_{45}	RXD Hold Time from RxC ↑	20			ns
t_{46}	RxC Delay from CRS ↑			1400	ns
t_{47}	RxC Continuing Beyond CRS ↓			5	cycles

NOTE:
17. All delay and width measurements on RXC are made at 1.5V.

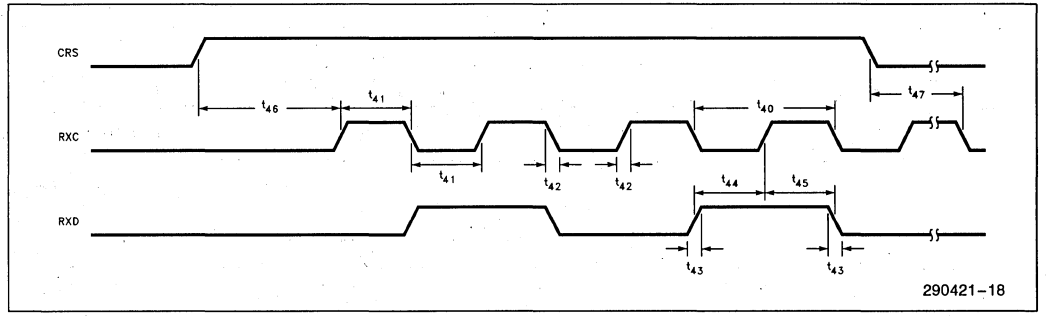


Figure 19. Receiving Timings (National)

Controller Interface Timing (AMD Mode)

TRANSMIT TIMINGS[18] (AMD)

Symbol	Parameter	Min	Typ	Max	Units
t_{50}	TCLK Cycle Time	99.99		100.01	ns
t_{51}	TCLK High Time (@ 0.8V to 2.0V)	45	50	58	ns
t_{52}	TCLK Low Time (@ 2.0V to 0.8V)	45	50	58	ns
t_{53}	TCLK Rise/Fall Time (@ 0.8V to 2.0V)		2.5	5	ns
t_{54}	TX Setup Time to TCLK ↑	20			ns
t_{55}	TX Hold Time from TCLK ↑	5			ns
t_{56}	TENA Setup Time to TCLK ↑	20			ns
t_{57}	TENA Hold Time from TCLK ↑	5			ns

NOTE:
18. Delay times for TX, TENA, and TCLK are measured from 0.8V for falling edges, and 2.0V for rising edges.

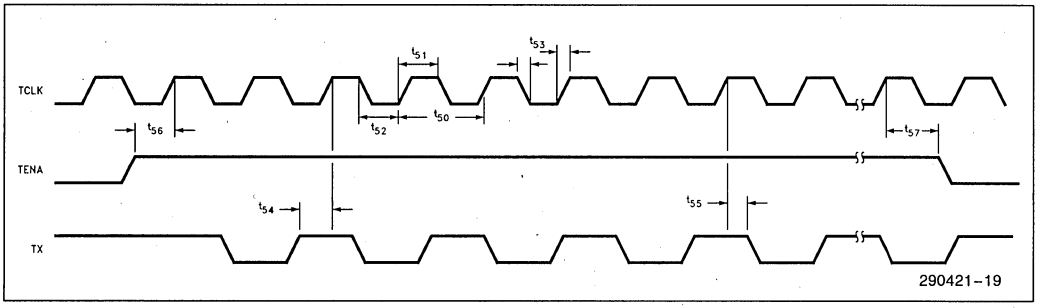


Figure 20. Transmit Timings (AMD)

RECEIVE TIMINGS[19] (AMD)

Symbol	Parameter	Min	Typ	Max	Units
t_{60}	RCLK Cycle Time	96	100		ns
t_{61}	RCLK High Time (@ 0.8V to 2.0V)	38	50		ns
t_{62}	RCLK Low Time (@ 2.0V to 0.8V)	38	50		ns
t_{63}	RCLK Rise/Fall Time (@ 0.8V to 2.0V)		2.5	5	ns
t_{64}	RX Rise/Fall Time (@ 0.8V to 2.0V)		2.5	5	ns
t_{65}	RX Hold time from RCLK ↑	10			ns
t_{66}	RX Setup Time to RCLK ↑	45			ns
t_{67}	RENA Deassertion Hold Time from RCLK ↑	40	50	80	ns
t_{68}	RCLK Delay from RENA ↑			450	ns

NOTE:
19. Delay times for RX, RENA, and RCLK are measured from 0.8V for falling edges and 2.0V for rising edges.

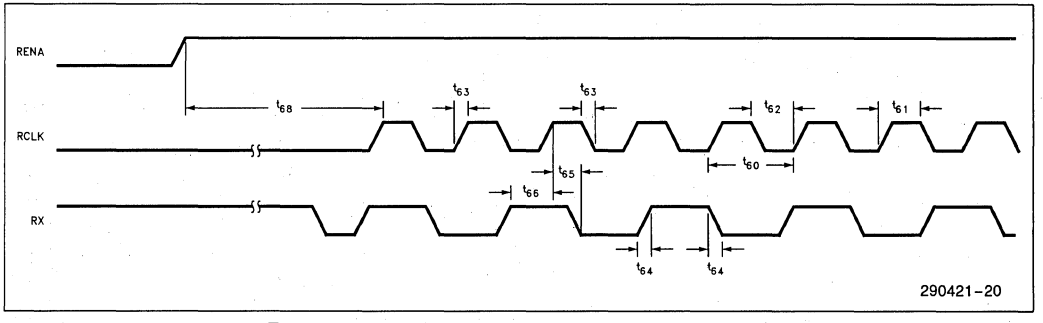


Figure 21. Receive Timings (AMD—Start of Frame)

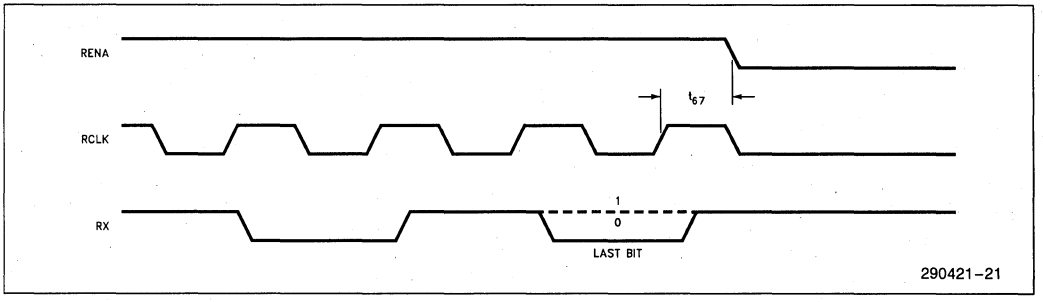


Figure 22. Receive Timings (AMD—End of Frame)

Controller Interface Timings (Fujitsu Mode)

TRANSMIT TIMINGS (Fujitsu)

Symbol	Parameter	Min	Typ	Max	Units
t_{70}	TCKN Cycle Time	99.99		100.01	ns
t_{71}	TCKN High/Low Time(20)	40	50		ns
t_{72}	TCKN Rise/Fall Time at 20% to 80%			5	ns
t_{73}	TXD Setup Time to TCKN ↓ (20)	20			ns
t_{74}	TXD Hold Time from TCKN ↓ (20)	0			ns
t_{75}	TEN Setup Time to TCKN ↓ (20)	20			ns
t_{76}	TEN Hold Time from TCKN ↓ (20)	0			ns

NOTE:
20. Timing measurements are referenced at 1.5V level.

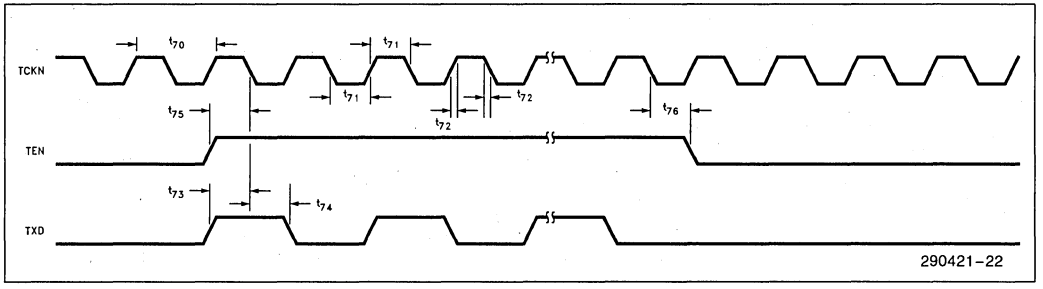


Figure 23. Transmit Timings (Fujitsu)

RECEIVE TIMINGS (Fujitsu)

Symbol	Parameter	Min	Typ	Max	Units
t_{80}	RCKN Cycle Time	96	100		ns
t_{81}	RCKN High/Low Time(21)	35	50	60	ns
t_{82}	RCKN Rise/Fall Time at 20% to 80%			5	ns
t_{83}	RXD Setup Time from RCKN ↓ (21)	20			ns
t_{84}	RXD Hold Time from RCKN ↓ (21)	10			ns
t_{85}	XCD Assertion Hold Time from RCKN ↓ (21)	0	10		ns
t_{86}	XCD Deassertion Hold Time from RCKN ↓ (21)		120		ns
t_{87}	XCD Deassertion Setup Time from RCKN ↓ (21)		80	130	ns
t_{88}	RCKN Delay from XCD ↑ (21)			1400	ns

NOTE:
21. Timing measurements are referenced at 1.5V.

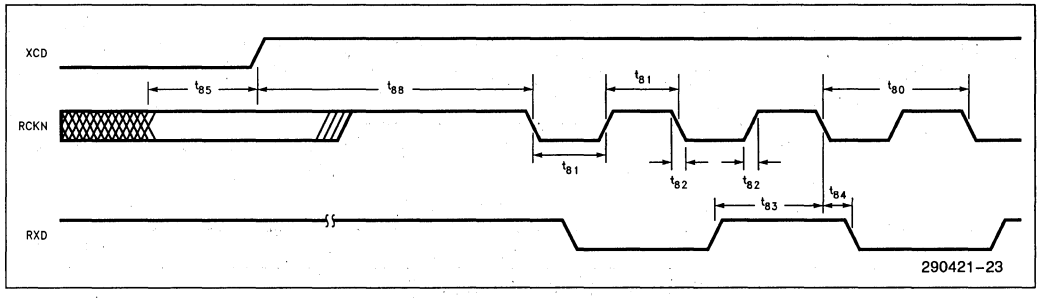


Figure 24. Receive Timings (Fujitsu—Start of Frame)

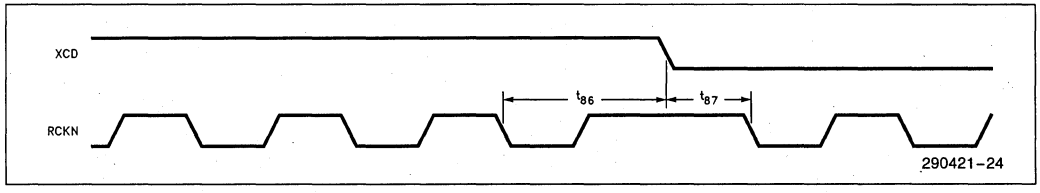


Figure 25. Receive Timings (Fujitsu—End of Frame)

TPE Timings

TPE TRANSMIT TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{90}	TxD to TD Bit Loss at Start of Packet			2	bits
t_{91}	TxD to TD Steady State Propagation Delay			400	ns
t_{92}	TxD to TD Startup Delay			600	ns
t_{93}	TDH and TDL Pairs Edge Skew (@ $V_{CC}/2$)		1.5	3	ns
t_{94}	TDH and TDL Pairs Rise/Fall Times (@ 0.5V to V_{CC} − 0.5V)		2	5	ns
t_{95}	TDH and TDL Pairs Bit Cell Center to Center	99	100	101	ns
t_{96}	TDH and TDL Pairs Bit Cell Center to Boundary	49	50	51	ns
t_{97}	TDH and TDL Pairs Return to Zero from Last TDH ↑	250		400	ns
t_{98}	Link Test Pulse Width	98	100	102	ns
t_{99}	Last TD Activity to Link Test Pulse	8	13	24	ms
t_{100}	Link Test Pulse to Data Separation	190	200		ns

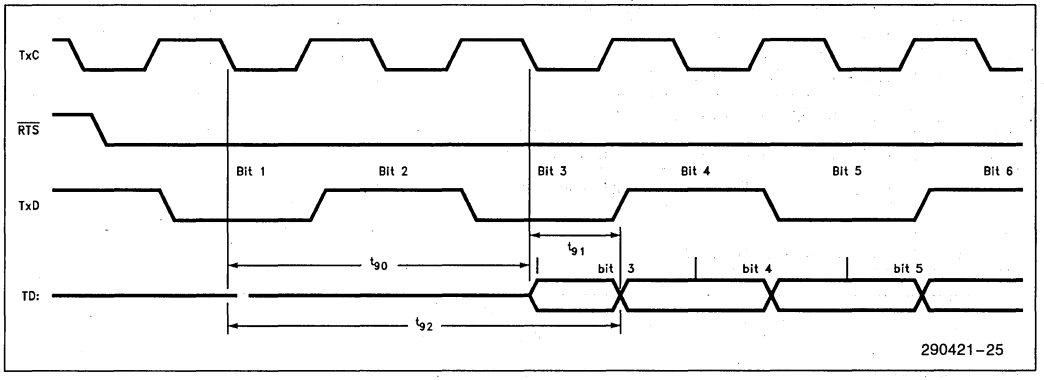


Figure 26. TPE Transmit Timings (Start of Frame)

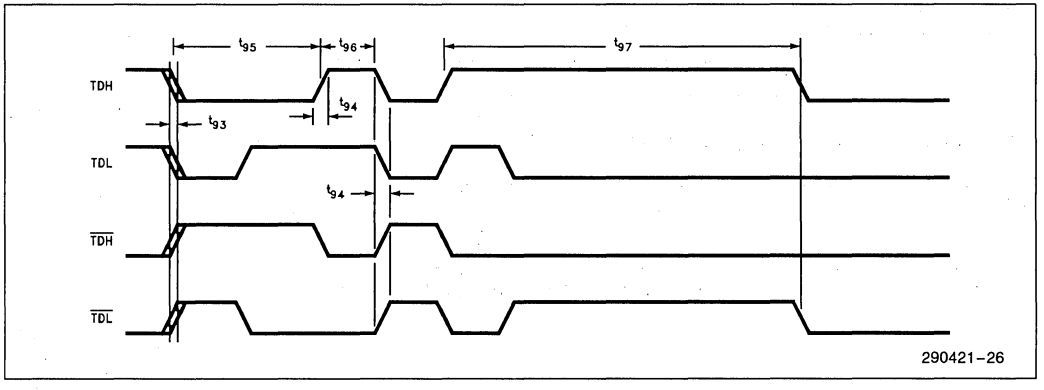


Figure 27. TPE Transmit Timings (End of Frame)

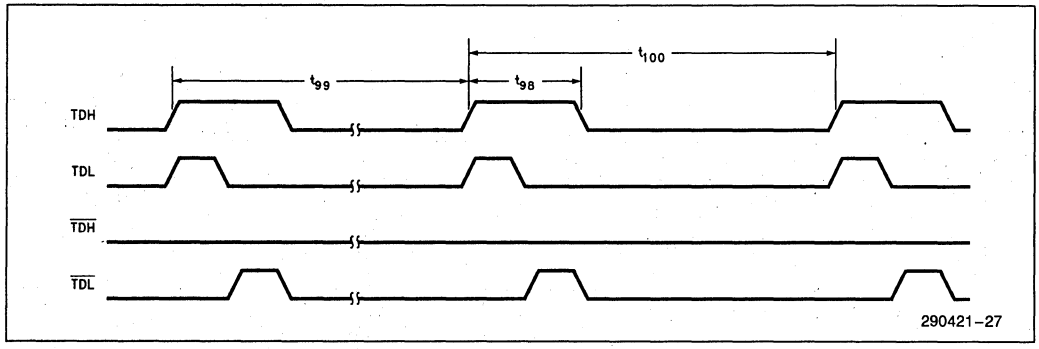


Figure 28. TPE Transmit Timings (Link Test Pulse)

TPE RECEIVE TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{105}	RD to RxD Bit Loss at Start of Packet	4		19	bits
t_{106}	RD to RxD Invalid Bits Allowed at Start of Packet			1	bits
t_{107}	RD to RxD Steady State Propagation Delay			400	ns
t_{108}	RD to RxD Start UP Delay			2.4	μs
t_{109}	RD Pair Bit Cell Center Jitter			±13.5	ns
t_{110}	RD Pair Bit Cell Boundary Jitter			±13.5	ns
t_{111}	RD Pair Held High from Last Valid Positive Transition	230		400	ns
t_{112}	$\overline{CRS}$ Assertion Delay (Intel, NS, and Fuji Mode) (AMD Mode)			700 1500	ns ns
t_{113}	$\overline{CRS}$ Deassertion Delay			450	ns

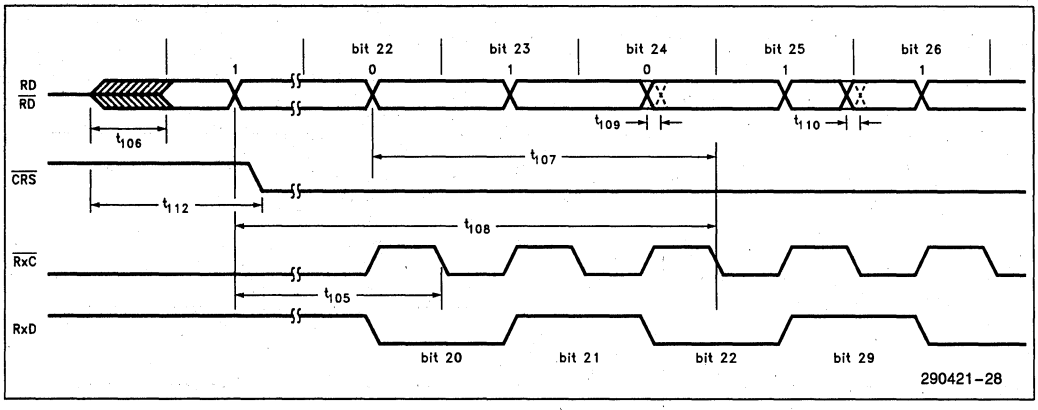


Figure 29. TPE Receive Timings (Start of Frame)

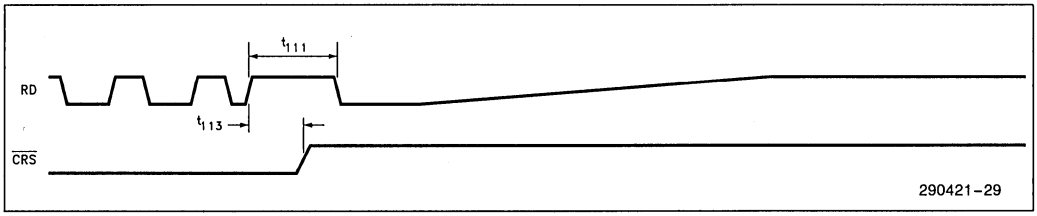


Figure 30. TPE Receive Timings (End of Frame)

TPE COLLISION TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{115}	Onset of Collision (RD Pair and $\overline{RTS}$ Active) to $\overline{CDT}$ Assert			900	ns
t_{116}	End of Collision (RD Pair or $\overline{RTS}$ Inactive) to $\overline{CDT}$ Deassert			900	ns
t_{117}	$\overline{CDT}$ Assert to RxD Sourced from RD Pair			900	ns
t_{118}	$\overline{CDT}$ Deassert (RD Pair Inactive) to RxD Sourced from TxD			900	ns

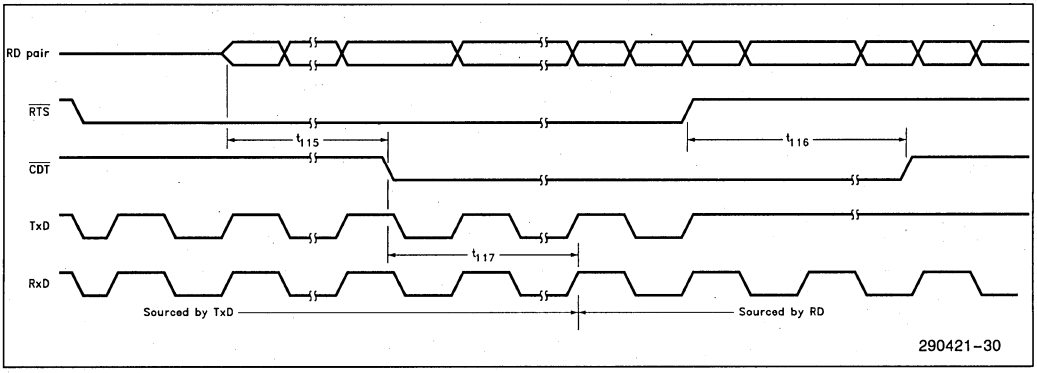


Figure 31. TPE Collision Timings (Start of Collision)

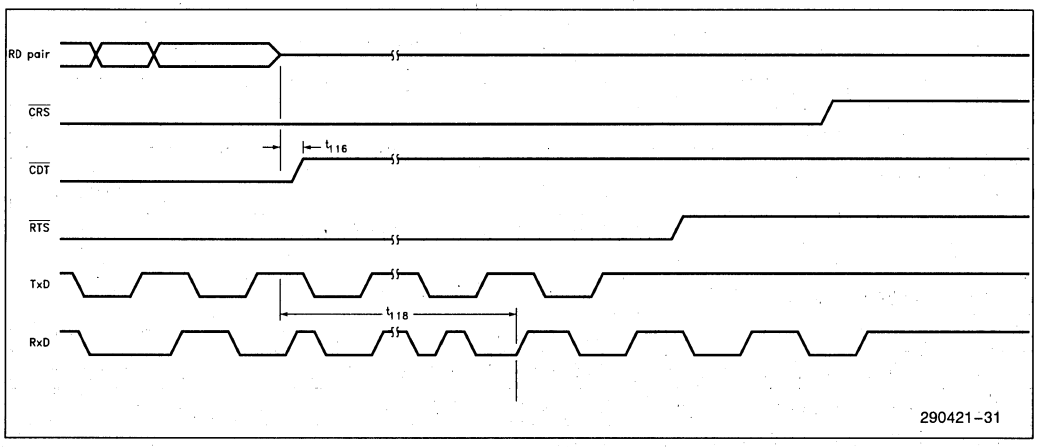


Figure 32. TPE Collision Timings (End of Collision)

TPE LINK INTEGRITY TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{120}	Last RD Activity to Link Fault (Link Loss Timer)	50	100	150	ms
t_{121}	Minimum Received Linkbeat Separation(20)	2	5	7	ms
t_{122}	Maximum Received Linkbeat Separation(21)	25	50	150	ms

NOTES:
20. Linkbeats closer in time to this value are considered noise, and are rejected.
21. Linkbeats further apart in time than this value are not considered consecutive, and are rejected.

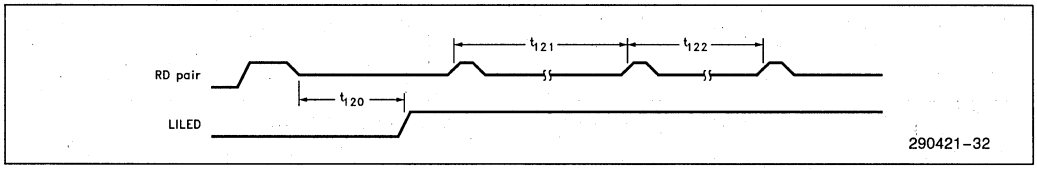


Figure 33. TPE Link Integrity Timings

AUI Timings

AUI TRANSMIT TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{125}	TxD to TRMT Pair Steady State Propagation Delay			200	ns
t_{126}	TRMT Pair Rise/Fall Times		3	5	ns
t_{127}	Bit Cell Center to Bit Cell Center of TRMT Pair	99.5	100	100.5	ns
t_{128}	Bit Cell Center to Bit Cell Boundary of TRMT Pair	49.5	50	50.5	ns
t_{129}	TRMT Pair Held at Positive Differential at Start of Idle	200			ns
t_{130}	TRMT Pair Return to ≤ 40 mV from Last Positive Transition			8.0	μs

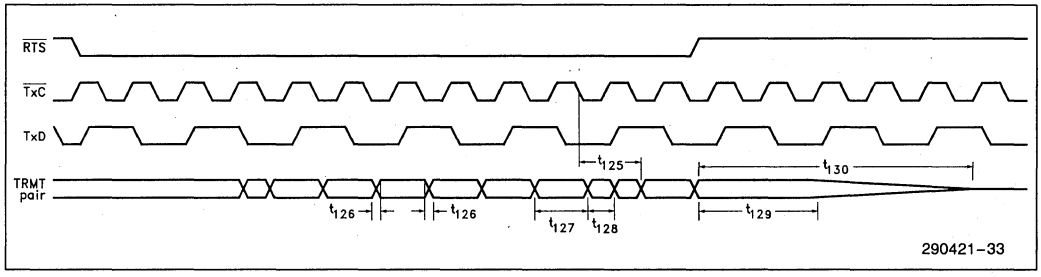


Figure 34. AUI Transmit Timings

AUI RECEIVE TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{135}	RCV Pair Rise/Fall Times			10	ns
t_{136}	RCV Pair Bit Cell Center Jitter in Preamble			±12	ns
t_{137}	RCV Pair Bit Cell Center/Boundary Jitter in Data			±18	ns
t_{138}	RCV Pair Idle Time after Transmission	8			μs
t_{139}	RCV Pair Return to Zero from Last Positive Transition	160			ns
t_{140}	$\overline{CRS}$ Assertion Delay (Intel, National, Fujitsu Modes) (AMD Mode)			100 1050	ns ns
t_{141}	$\overline{CRS}$ Deassertion Delay			350	ns
t_{142}	$\overline{CRS}$ Inhibited after Frame Transmission	4	4.3	5	μs

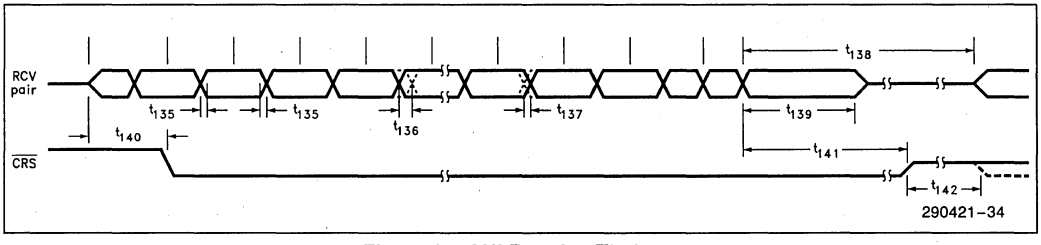


Figure 35. AUI Receive Timings

AUI COLLISION TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{145}	CLSN Pair Cycle Time	80		118	ns
t_{146}	CLSN Pair Rise/Fall Times			10	ns
t_{147}	CLSN Pair Return to Zero from Last Positive Transition	160			ns
t_{148}	CLSN Pair High/Low Times	35		70	ns
t_{149}	$\overline{CDT}$ Assertion Time			75	ns
t_{150}	$\overline{CDT}$ Deassertion Time			300	ns
t_{151}	$\overline{CRS}$ Deassertion Time (Intel Mode Only, RCV Pair Idle)			450	ns

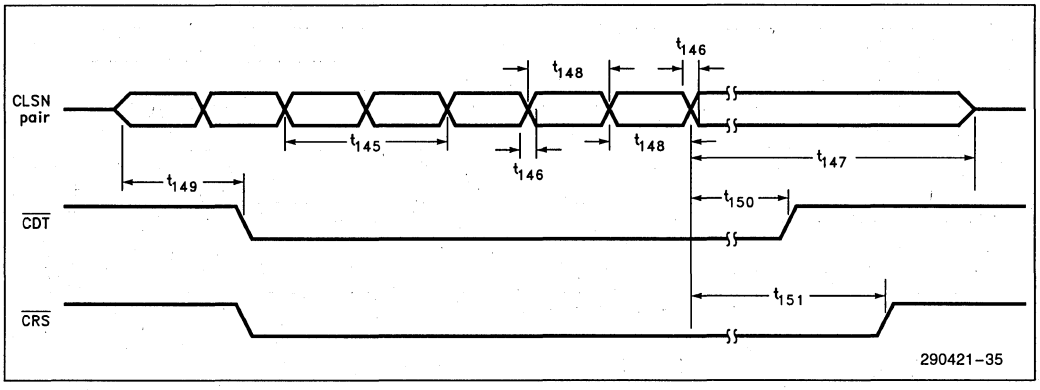


Figure 36. AUI Collision Timings

AUI NOISE FILTER TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{152}	RCV Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns
t_{153}	CLSN Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns

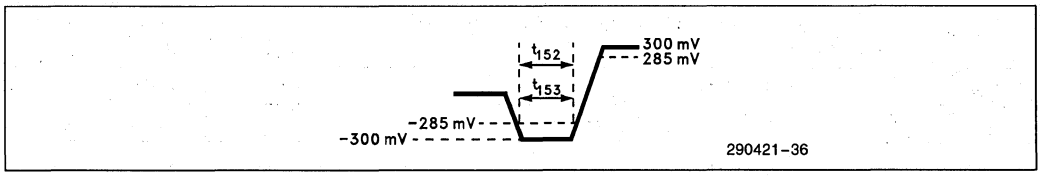


Figure 37. AUI Noise Filter Timings

LOOPBACK TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{155}	TxD to RxD Bit Loss at Start of Packet			16	bits
t_{156}	TxD to RxD Steady State Propagation Delay			600	ns
t_{157}	TxD to RxD Startup Delay			2.2	μs
t_{158}	SQE Test Wait Time	0.6	1.2	1.6	μs
t_{159}	SQE Test Duration	0.5	0.8	1.5	μs
t_{160}	$\overline{LPBK}$ Setup/Hold Times to $\overline{RTS}$(22)	1.0			μs

NOTE:
22. Guarantees proper processing of transmitted packets. Violation of this specification will not result in spurious data transmission. Incoming data packets occuring during transitions on $\overline{LPBK}$ will not be accepted.

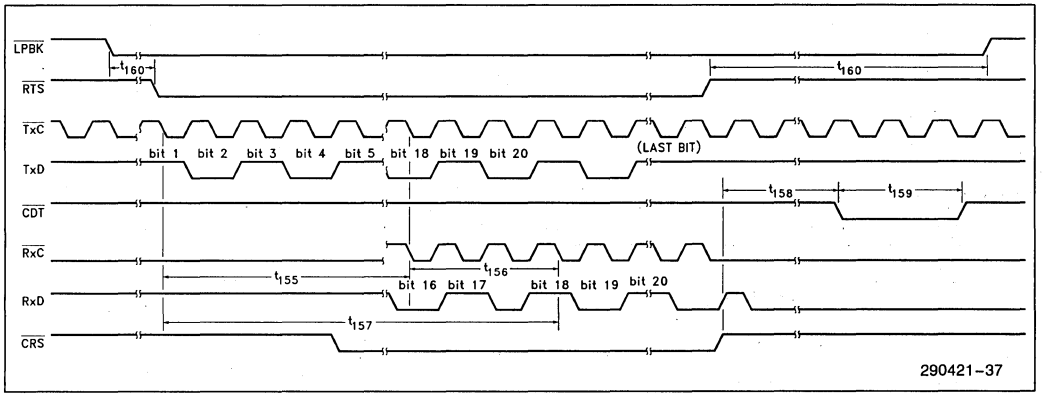


Figure 38. Loopback Timings

JABBER TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{165}	Maximum Length Transmission before Jabber Fault (TPE)	20	25	150	ms
t_{166}	Maximum Length Transmission before Jabber Fault (AUI)	10	13	18	ms
t_{167}	Minimum Idle Time to Clear Jabber Function	250	420	750	ms

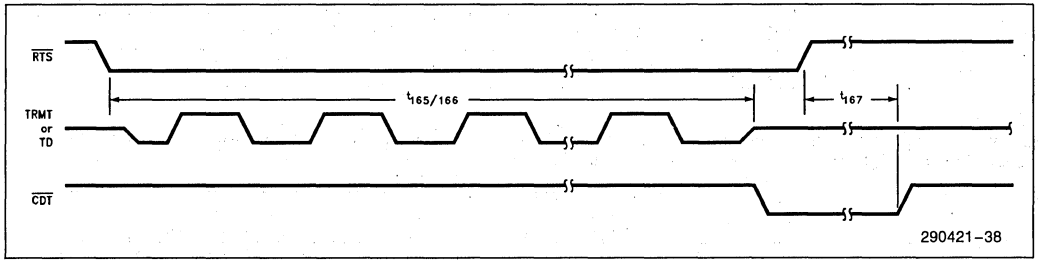


Figure 39. Jabber Timings

LED TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{170}	TxLED, RxLED, COLED On Time	50		450	ms
t_{171}	TxLED, RxLED, COLED Off Time	50			ms
t_{172}	LILED On Time	50			ms
t_{173}	LILED Off Time	100			ms

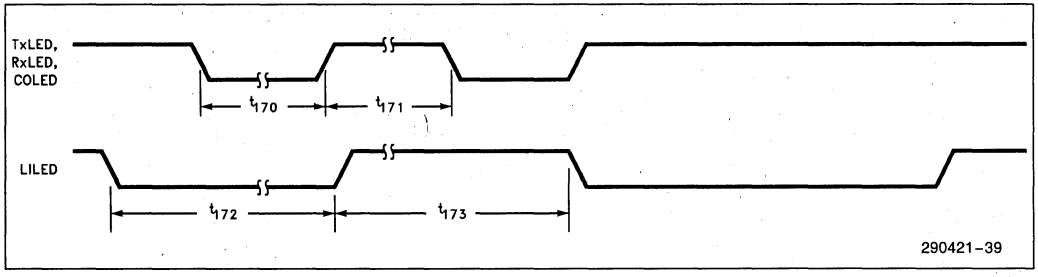


Figure 40. LED Timings

MODE TIMINGS(23, 24)

Symbol	Parameter	Min	Typ	Max	Units
t_{175}	Mode Pins Setup to $\overline{RTS}$ ↓	100			ms
t_{176}	Mode Pins Hold from $\overline{RTS}$ ↑	100			ms
t_{177}	Mode Pins Setup to RD Active(25)	100			ms
t_{178}	Mode Pins Hold from RD Active(25)	100			ms

NOTES:
23. Guarantees Proper processing of data packets. Violation of these specifications will not affect the integrity of the network.
24. Mode pins are: APORT, APOL/XSQ, LID, JABD, and TPE/$\overline{AUI}$.
25. Any data received within 100 ms of a mode transmission will be considered invalid.

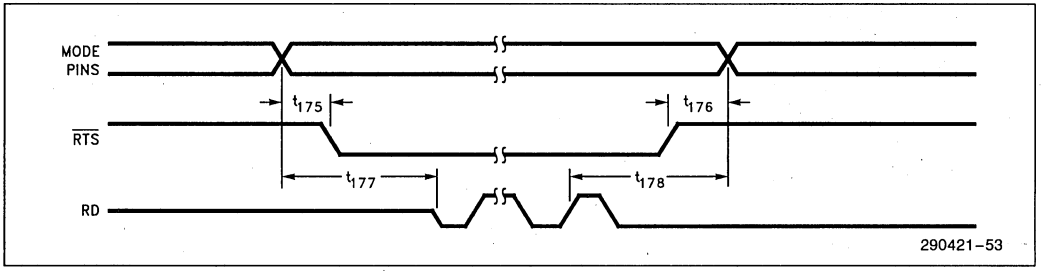


Figure 41. Mode Timings

RESET, TEST, AND LOW POWER MODE TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{180}	TEST and JABD Setup Time to RESET ↓	50			ns
t_{181}	RESET Pulse Width	300			ns
t_{182}	Low Power Mode Deactivation from TEST and JABD ↓			1	ms

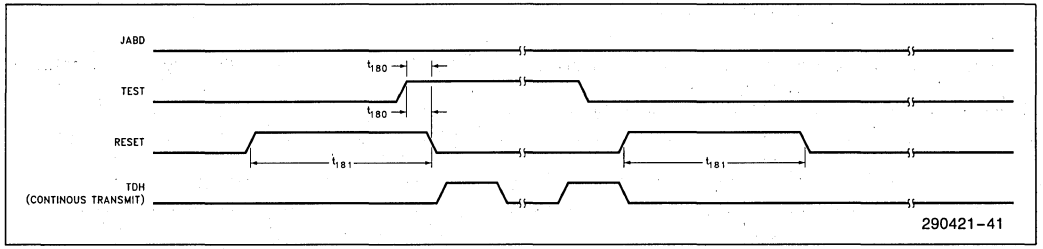


Figure 42. Reset Timings (Test Mode)

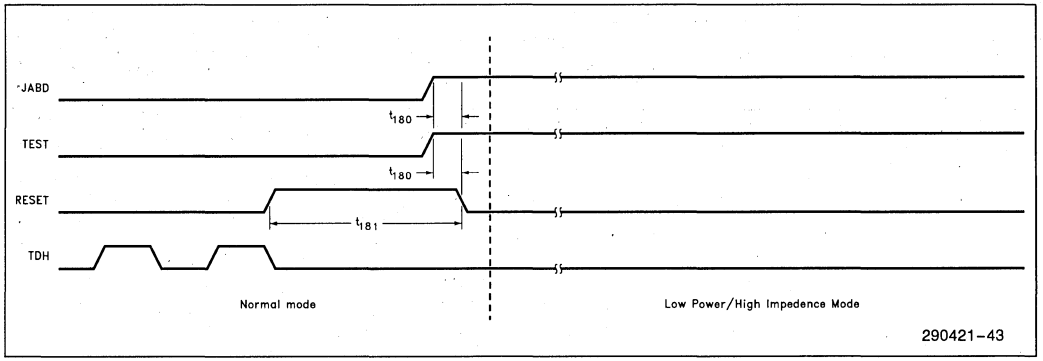


Figure 43. Reset Timings (Start of Low Power Mode)

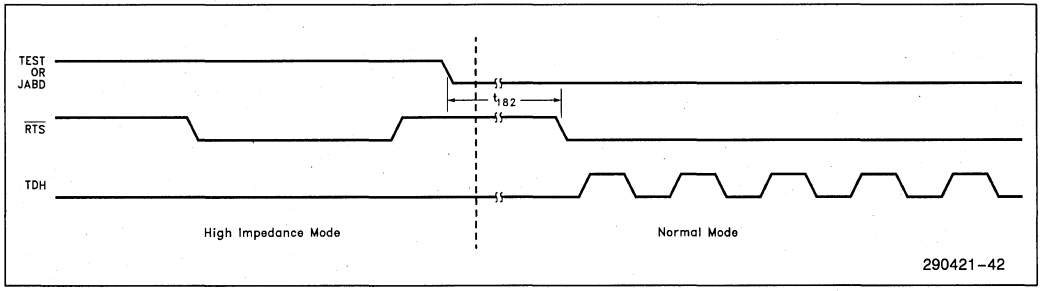


Figure 44. Reset Timings (End of Low Power Mode)

PACKAGE DIMENSIONS

PLASTIC LEADED CHIP CARRIER

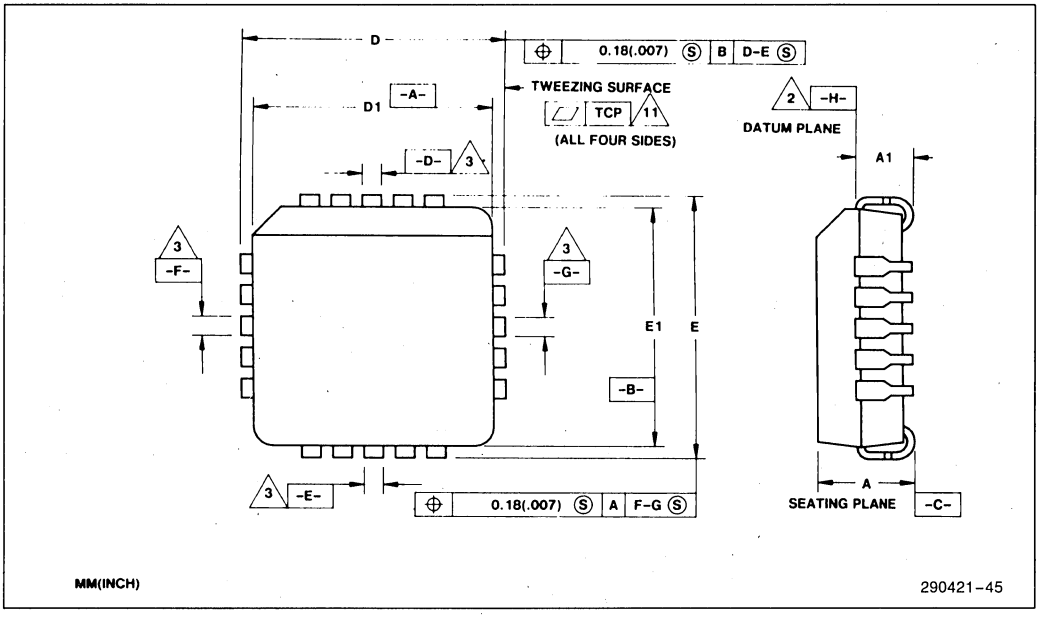


Figure 45. Principle Dimensions and Data

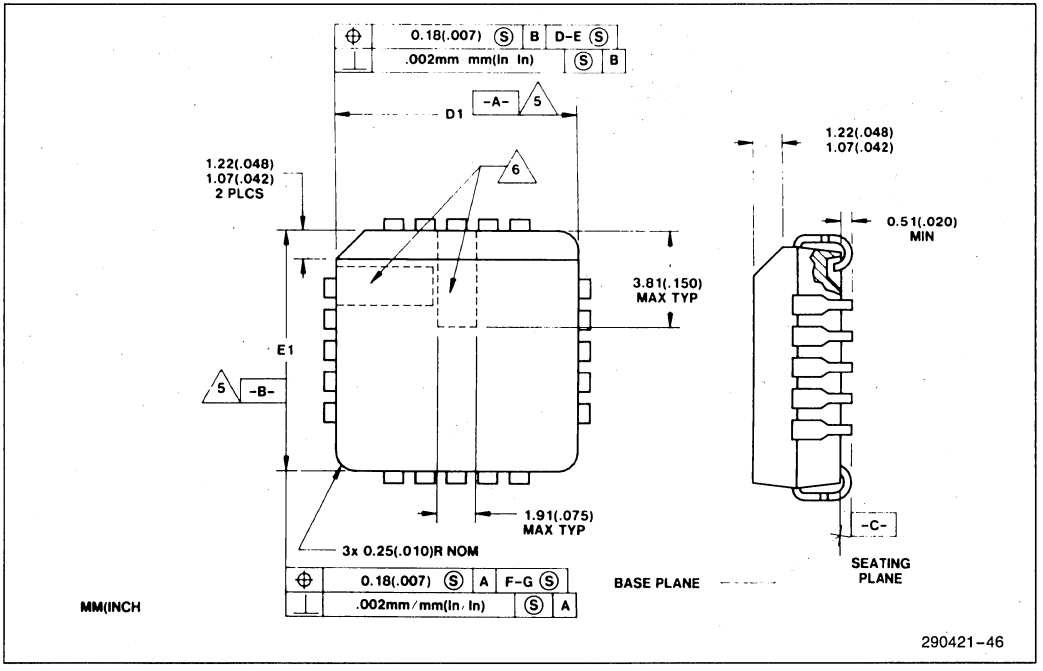


Figure 46. Molded Details

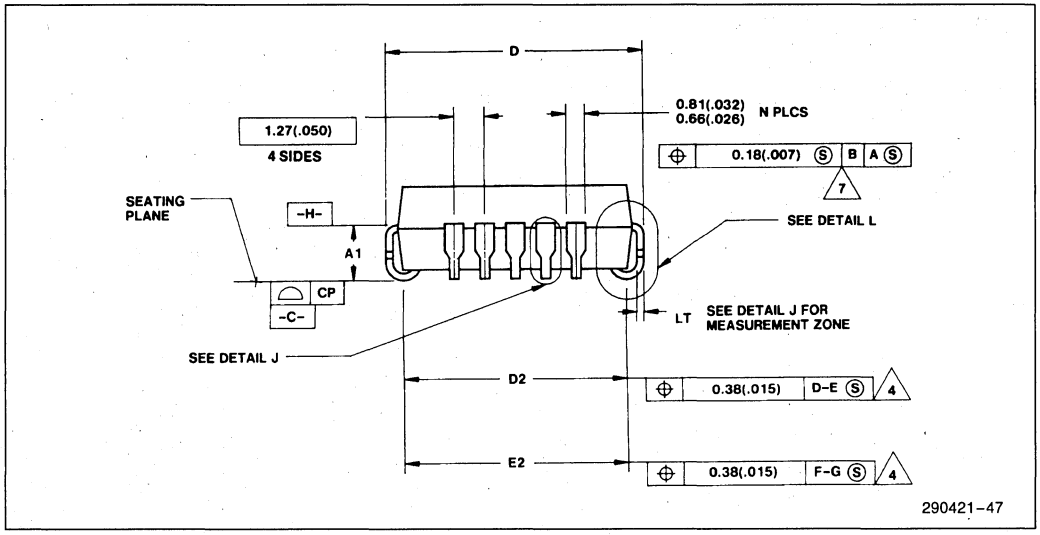


Figure 47. Terminal Details

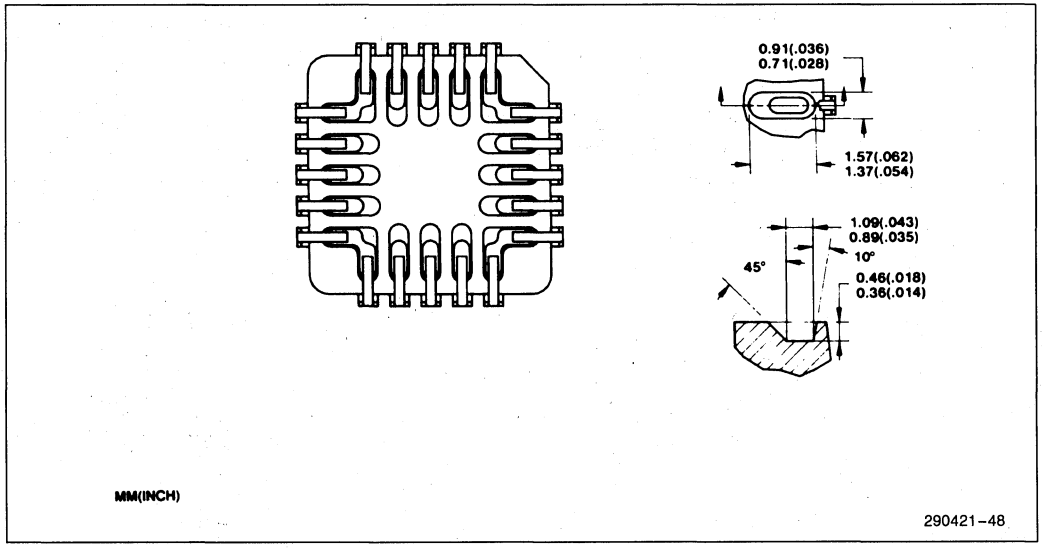
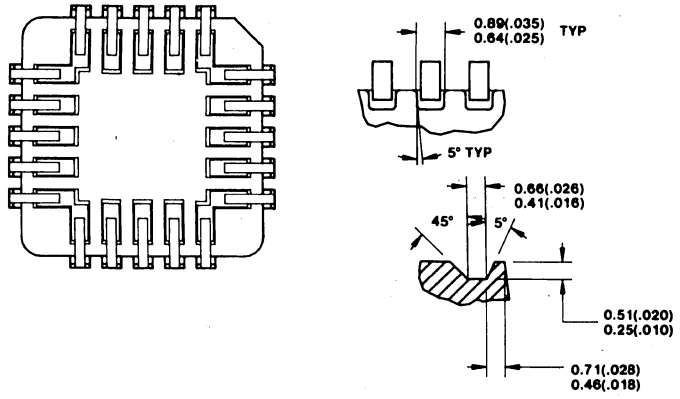


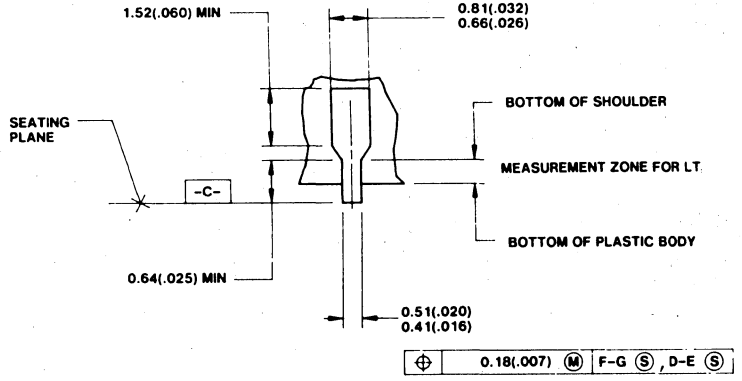
Figure 48. Standard Package Bottom View (Tooling Option 1)



MM(INCH)

290421-49

Figure 49. Standard Package Bottom View (Tooling Option II)



DETAIL J

MM(INCH)

290421-50

Figure 50. Detail J. Terminal Detail

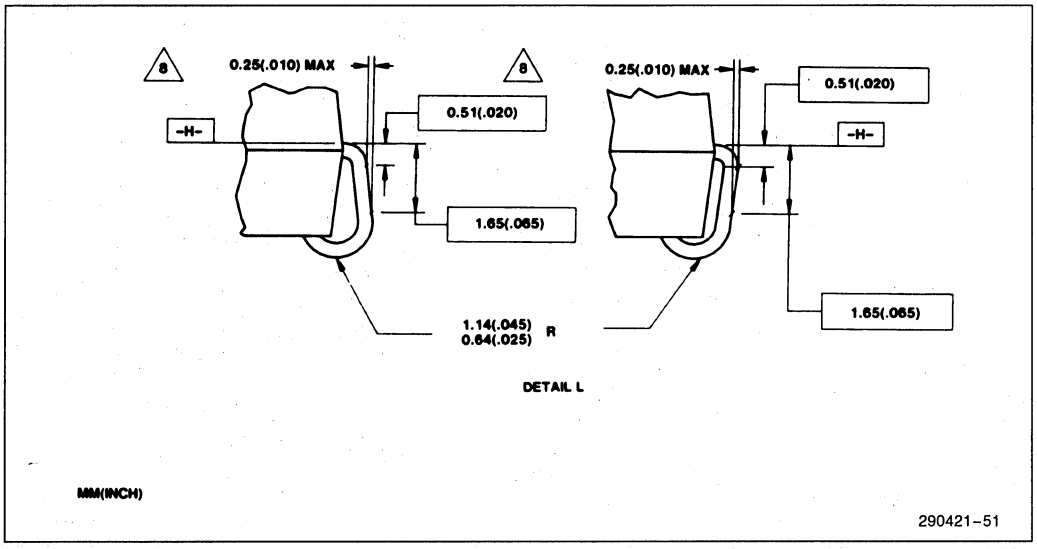


Figure 51. Detail L. Terminal Details

NOTES:
The above diagrams use a 20-lead PLCC package to show symbols for package dimensions. The table below indicates dimensions in mm that are specific to the 44-lead PLCC package.
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **—H—** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Datums **D–E** and **F–G** to be determined where center leads exit plastic body at datum plane **—H—**.
4. To be determined at seating plane **—C—**.
5. Dimensions D_1 and E_1 do not include mold protrusion.
6. Pin 1 identifier is located within one of the two defined zones.
7. Locations to datum **—A—** and **—B—** to be determined at plane **—H—**.
8. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
9. Controlling dimension, inch.
10. All dimensions and tolerances include lead trim offset and lead plating finish.
11. Tweezing surface planarity is defined as the furthest any lead on a side may be from the datum. The datum is established by touching the outermost lead on that side and parallel to **D–E** or **F–G**.

Symbol	Description	Min	Max
A	Overall Height	4.19	4.57
A_1	Distance from Lead Shoulder to Seating Plane	2.29	3.05
D	Overall Package Dimension	17.4	17.7
D_1	Plastic Body Dimension	16.5	16.7
D_2	Foot Print	15.0	16.0
E	Overall Package Dimension	17.4	17.7
E_1	Plastic Body Dimension	16.5	16.7
E_2	Foot Print	15.0	16.0
CP	Seating Plans Coplanarity	0.00	0.10
TCP	Tweezing Coplanarity	0.00	0.10
LT	Lead Thickness	0.23	0.38

44-LEAD QUAD FLATPACK PACKAGE

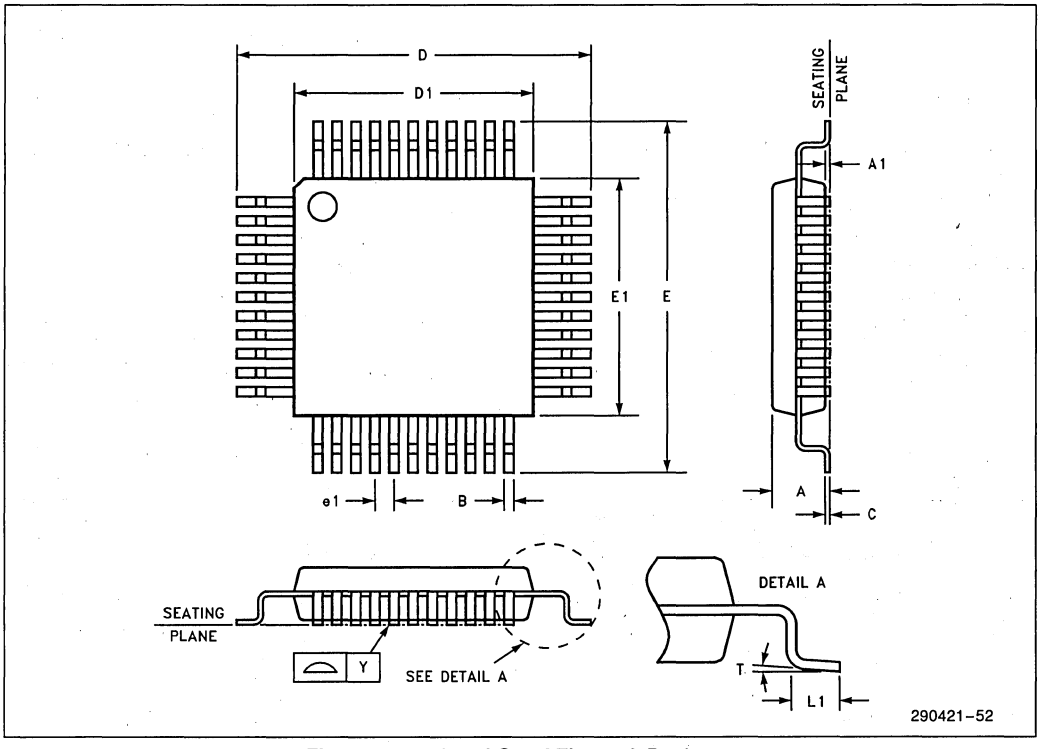


Figure 52. 44-Lead Quad Flatpack Package

Symbol	Description	Min	Nom	Max
A	Package Height			2.35
A1	Stand Off	0		0.60
B	Lead Width	0.2	0.3	0.4
C	Lead Thickness	0.1	0.15	0.2
D_1	Package Body		10	
E_1	Package Body		10	
e_1	Lead Pitch	0.65	0.8	0.95
D	Terminal Dimension	12.0	12.4	12.8
E	Terminal Dimension	12	12.4	12.8
L_1	Foot Length	0.38	0.58	0.78
Y	Coplanarity			0.1
T	Lead Angle	0		10°

NOTE:
Unless otherwise specified, all units are in millimeters.

82557
FAST ETHERNET PCI BUS LAN CONTROLLER

- **Optimum Integration for Lowest Cost Solution**
  - **IEEE 802.3 10BASE-T and 100BASE-T Compatible**
  - **Glueless 32-bit PCI Bus Master Interface**
  - **Flash Support up to 1 Mbyte**
- **High Performance Networking Functions**
  - **Chained Memory Structure Similar to the 82596 Controller**
  - **Improved Dynamic Transmit Chaining**
  - **Programmable Transmit Threshold**
  - **Early Receive Interrupt**
  - **Large Internal Receive and Transmit FIFOs**
  - **Back-to-Back Transmit at 100 Mbps, within minimum IFS**
- **Ease of Use**
  - **Built-in Interface to MII Compliant Serial Devices**
  - **Full or Half Duplex Capable at 10 Mbps or 100 Mbps**
  - **Standard 7-Pin ENDEC Interface to Serial Device Such as the Intel 82503 for 10 Mbps Only Designs**
  - **EEPROM Support**
  - **Internal Counters for Network Management**

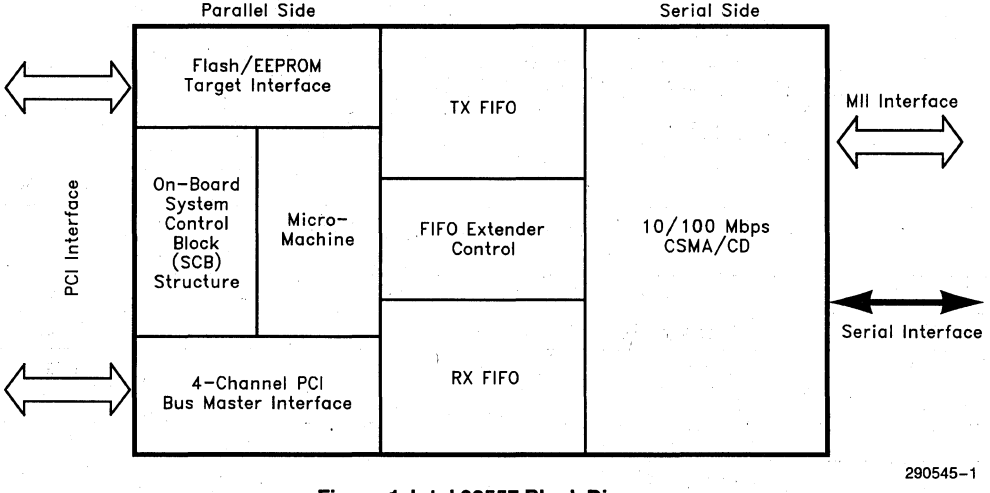


Figure 1. Intel 82557 Block Diagram

*Other brands and names are the property of their respective owners.

October 1995
Order Number: 290545-001

82557
FAST ETHERNET* PCI BUS CONTROLLER

CONTENTS

CONTENTS

CONTENTS

CONTENTS

CONTENTS

PAGE

FIGURES

CONTENTS

PAGE

TABLES

1.0 INTRODUCTION

1.1 82557 Overview

The 82557 is Intel's first highly integrated 32-bit PCI LAN controller for 10 Mbps or 100 Mbps Fast Ethernet networks. The 82557 offers a high performance LAN solution while maintaining low-cost through its high-integration. It contains a 32-bit PCI Bus Master interface to fully utilize the high bandwidth available (up to 132 Mbytes per second) to masters on the PCI bus. The bus master interface can eliminate the intermediate copy step in Receive (RCV) and Transmit (XMT) frame copies, resulting in faster processing of these frames. It maintains a similar memory structure to the Intel 82596 LAN Coprocessor, however, these memory structures have been streamlined for better network operating system (NOS) interaction and improved performance.

The 82557 contains two large receive and transmit FIFOs which prevent data overruns or underruns while waiting for access to the PCI bus, as well as enabling back to back frame transmission within the minimum 960 ns inter frame spacing. Full support for up to 1 Mbyte of FLASH enables network management support via Intel FlashWorks utilities as well as remote boot capability (a BIOS extension stored in the FLASH which could allow a node to boot itself off of a network drive). For 100 Mbps applications, the 82557 contains an IEEE MII compliant interface to the Intel 82553 serial interface device (or other MII compliant PHYs) which will allow connection to 100 Mbps/10 Mbps networks. For 10 Mbps networks, the 82557 can be interfaced to a standard ENDEC device (such as the Intel 82503 Serial Interface), while maintaining software compatibility with 100 Mbps solutions.

The 82557 is designed to implement cost effective, high performance PCI add-in adapters, PC motherboards, or other interconnect devices such as a hubs or bridges. Its combination of high integration and low cost make it ideal for these applications.

1.2 Features and Enhancements

The following list summarizes the main features of the Intel 82557 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with PCI Bus Specification, revision 2.1
- 82596-like Chained Memory Structure
- Improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- FLASH support up to 1 Mbyte
- Large on-chip receive and transmit FIFOs
- On-chip counters for network management
- Back-to-back transmit at 100 Mbps
- EEPROM support
- Support for both 10 Mbps and 100 Mbps Networks
- Interface to MII compliant PHY devices, including Intel 82553 Physical Interface component for 10 Mbps/100 Mbps designs
- IEEE 802.3 100BASE-T, TX, and T4 compatible
- Interface to Intel 82503 or other serial device for 10 Mbps designs: IEEE 802.3 10BASE-T compatible
- Autodetect and autoswitching for 10 Mbps or 100 Mbps network speeds
- Full or half duplex-capable at 10 Mbps and 100 Mbps
- 160-Lead QFP package

1.3 Compliance to Industry Standards

The 82557 has two interfaces. The host system PCI bus interface and the serial or network interface. The network interface complies to the IEEE standard for 10Base-T, TX, and T4 Ethernet interfaces. The 82557 also complies to the PCI Bus Specification, Revision 2.1.

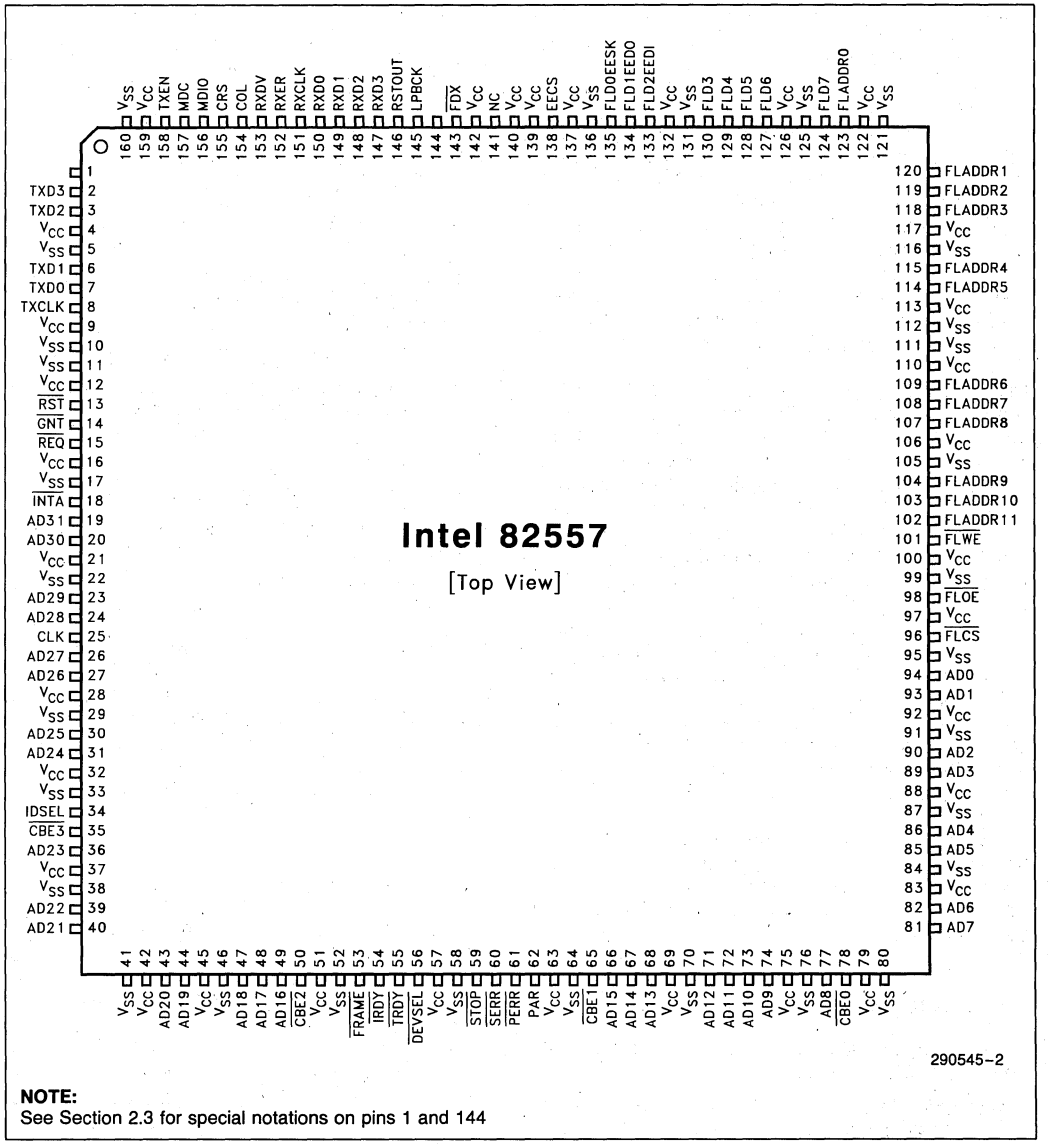
1.4 Other Literature

This data sheet provides complete pin identification, definitions and electrical specifications. It also provides an overview of each main subsystem within the component. Most of this information is aimed at hardware design engineers.

Software engineers and others who are designing interfaces or writing device drivers for this component, should refer to the *82557 User's Guide*. This document provides more detailed information on feature sets, register descriptions and implementation steps for various functions.

2.0 PIN DEFINITIONS

Figure 2 shows pin numbering and signal identification for the 82557. Sections 2.1 through 2.4 describe the signals.



NOTE:
See Section 2.3 for special notations on pins 1 and 144

Figure 2. Device Pinout, Top View

2.1 PCI Bus Interface Signals

The following sections describe the 82557 pins and signals by function.

2.1.1 SIGNAL TYPE DEFINITION

IN	Input is a standard input-only signal.
OUT	Totem Pole Output is a standard active driver.
TS	Tri-State is a bi-directional, tri-state input/output pin.
STS	Sustained Tri-State is an active low tri-state signal owned and driven by the 82557. When the 82557 drives this pin low, it must drive it high for at least one clock before letting it float.
OD	Open Drain allows multiple devices to share as a wire-OR.

2.1.2 ADDRESS AND DATA PINS

Symbol	Pin	Type	Name and Function
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31	94 93 90 89 86 85 82 81 77 74 73 72 71 68 67 66 49 48 47 44 43 40 39 36 31 30 27 26 24 23 20 19	TS	Address and Data are multiplexed on the same PCI pins by the 82557. A bus transaction consists of an address phase followed by one or more data phases.The address phase is the clock cycle in which $\overline{\text{FRAME}}$ is asserted. During the address phase AD0–31 contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory it is a DWORD address. The 82557 used "Little Endian" byte ordering. During data phases AD0–7 contain the least significant byte (LSB) and AD24–31 contain the most significant byte (MSB).
$\overline{\text{CBE0}}$ $\overline{\text{CBE1}}$ $\overline{\text{CBE2}}$ $\overline{\text{CBE3}}$	78 65 50 35	TS	Bus Command and Byte Enables are multiplexed on the same PCI pins by the 82557. During the address phase of a transaction, C/$\overline{\text{BE0–3}}$ define the bus command. During the data phase C/$\overline{\text{BE0–3}}$ are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/$\overline{\text{BE0}}$ applies to byte 0 (LSB) and C/$\overline{\text{BE3}}$ applies to byte 3 (MSB).
PAR	62	TS	Parity is even parity across AD0–31 and C/$\overline{\text{BE0–3}}$. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either $\overline{\text{IRDY}}$ is asserted on a write transaction or $\overline{\text{TRDY}}$ is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82557 is a bus master, it drives PAR for address and write data phases. As a slave, it drives PAR for read data phases.

2.1.3 INTERFACE CONTROL PINS

Symbol	Pin	Type	Name and Function
FRAME	53	STS	FRAME is driven by the 82557 to indicate the beginning and duration of an access. FRAME is asserted to indicate a bus transaction is beginning. While FRAME is asserted, data transfers continue. When FRAME is deasserted, the transaction is in the final data phase.
IRDY	54	STS	INITIATOR READY indicates the ability of the 82557 (as a bus mastering device) to complete the current data phase of the transaction. IRDY is used in conjunction with TRDY. A data phase is completed on any clock in which both IRDY and TRDY are sampled asserted. During a write, IRDY indicates that valid data is present on AD0–31. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are asserted together. The 82557 drives IRDY when acting as a master, and samples it when acting as a slave.
TRDY	55	STS	TARGET READY indicates the ability of the 82557 (as a selected device) to complete the current data phase of the transaction. TRDY is used in conjunction with IRDY. A data phase is completed on any clock in which both TRDY and IRDY are sampled asserted. During a read, TRDY indicates that valid data is present on AD0–31. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are asserted together. The 82557 drives TRDY when acting as a slave, and samples it when acting as a master.
STOP	59	STS	STOP indicates the current target is requesting the master to stop the current transaction. As a slave, the 82557 drives STOP to inform the bus master to stop the current transaction. As a bus master, the 82557 receives STOP from the slave and stops the current transaction.
IDSEL	34	IN	Initialization Device Select is used by the 82557 as a chip select during configuration read and write transactions.
DEVSEL	56	STS	DEVICE SELECT, when actively driven by the 82557 as a slave, indicates to the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL indicates whether any device on the bus has been selected.

2.1.4 ERROR REPORTING PINS

Symbol	Pin	Type	Name and Function
SERR	60	OD	SYSTEM ERROR is used by the 82557 to report address parity errors. SERR is open drain and is actively driven for a single PCI clock when reporting the error.
PERR	61	STS	PARITY ERROR is used by the 82557 for reporting data parity errors during all PCI transactions except a Special Cycle. The PERR pin is sustained tri-state and must be driven active by the 82557 receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR is one clock for each data phase that a data parity error is detected.

2.1.5 INTERRUPT PIN

Symbol	Pin	Type	Name and Function
$\overline{INTA}$	18	OD	$\overline{INTERRUPT\ A}$ is used to request an interrupt by the 82557. This is an active low, level-triggered interrupt signal.

2.1.6 ARBITRATION PINS

Symbol	Pin	Type	Name and Function
$\overline{REQ}$	15	TS	$\overline{REQUEST}$ indicates to the arbiter that the 82557 desires use of the bus. This is a point to point signal. Every master has its own $\overline{REQ}$.
$\overline{GNT}$	14	IN	$\overline{GRANT}$ indicates to the 82557 that access to the bus has been granted. This is a point to point signal.

2.1.7 SYSTEM PINS

Symbol	Pin	Type	Name and Function
CLK	25	IN	Clock provides timing for all transactions on the PCI bus and is an input to the 82557. All other PCI signals, except $\overline{RST}$ and the $\overline{INT}$ lines are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge.
$\overline{RST}$	13	IN	$\overline{RESET}$ is used to bring PCI-specific registers, sequencers and signals to a consistent state. Anytime $\overline{RST}$ is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be tri-stated. $\overline{SERR}$ (open drain) is floated. To prevent AD, C/$\overline{BE}$ and PAR signals from floating during reset, the central device may drive these lines during reset (bus parking) but only to a logic low level—they may not be driven high.

2.2 Local Memory Interface

Symbol	Pin	Type	Name and Function
EECS	138	OUT	EEPROM Chip Select: Active high signal used to assert Chip Select to the serial EEPROM.
FLD0EESK	135	TS	Multiplexed pin. During flash access acts as FLASH Data 0 input/output. During EEPROM access acts as EEPROM SHIFT CLOCK output to shift data into and out of the serial EEPROM.
FLD1EEDO	134	TS	Multiplexed pin. During flash access acts as FLASH Data 1 input/output. During EEPROM access, this pin acts as the input EEPROM DATA OUT.
FLD2EEDI	133	TS	Multiplexed pin. During flash access acts as FLASH Data 2 input/output. During EEPROM access, this pin acts as the output EEPROM DATA IN.
FLD3 FLD4 FLD5 FLD6 FLD7	130 129 128 127 124	TS	FLASH Data 7 to 3 input/outputs.
FLADDR0 FLADDR1 FLADDR2 FLADDR3 FLADDR4 FLADDR5 FLADDR6 FLADDR7 FLADDR8 FLADDR9 FLADDR10 FLADDR11	123 120 119 118 115 114 109 108 107 104 103 102	OUT	FLASH Address 11 to 0. These 12 pins work in conjunction with an external 8-bit Address Latch to control the FLASH addressing up to 1 Mbyte. The 8 most significant FLASH address pins (FLADDR11 to 4) should be connected to both the Address Latch and to Address Pins 11 to 4 of the FLASH. The Address Latch provides the upper 8 bits, 19 to 12, of address to the FLASH and is loaded by assertion of the $\overline{\text{FLCS}}$ pin.
$\overline{\text{FLCS}}$	96	OUT	FLASH CS will normally be high to disable access to the FLASH. Whenever a FLASH high address is to be latched, $\overline{\text{FLCS}}$ will go low, thus latching the data in the latch and enabling the FLASH. $\overline{\text{FLCS}}$ should be connected to both the ENABLE pin on the external address latch and the $\overline{\text{CE}}$ pin on the FLASH.
$\overline{\text{FLOE}}$	98	OUT	This output provides the active low Output Enable control to the FLASH.
$\overline{\text{FLWE}}$	101	OUT	This output provides the active low Write Enable control to the FLASH.

2.3 MII/Serial Interface Pins

Symbol	Pin	Type	Name and Function
RXCLK	151	IN	Receive Clock input operates at either 25 MHz, 2.5 MHz (MII Mode), or 10 MHz (10 Mbps-only mode).
RXD0 RXD1 RXD2 RXD3	150 149 148 147	IN	Receive Data. In MII mode: nibble wide receive data inputs. In 10 Mbps only mode, RXD0 is the serial receive data input.
RXDV	153	IN	Receive Data Valid indicates that valid data is present on the RXD lines. Used for MII mode only. When this pin is inactive (low), receive data is not sampled by the 82557.
RXER	152	IN	Receive Data Error. Indicates that an invalid symbol has been detected inside a receive packet. MII mode only.
Reserved	1	—	No connection.
CRS	155	IN	Carrier Sense. Indicates traffic on the wire
TXCLK	8	IN	Transmit Clock input operates at either 25 MHz, 2.5 MHz (MII Mode), or 10 MHz (10 Mbps-only mode).
TXD0 TXD1 TXD2 TXD3	7 6 3 2	OUT	Transmit Data. In MII mode: nibble wide transmit data outputs. In 10 Mbps only mode: TXD0 is the serial transmit data output.
RTS/TXEN	158	OUT	Request To Send. Indicates that the 82557 has a frame pending for transmission (10 Mbps-only mode) Transmit Enable. Indicates that the 82557 is transferring data to the PHY (MII mode).
COL	154	IN	Collision Detect. Indicates a collision has been detected on the wire. In Full Duplex mode, assertion of COL indicates a Congestion condition has occurred.
Reserved	144	IN	Tie high with a 3.3 KΩ pull-up resistor.
RSTOUT	146	OUT	Reset Out signal to the PHY, driven high during H/W reset of the 82557.
LPBCK	145	OUT	Loopback controls the PHY into loopback mode.
$\overline{\text{FDX}}$	143	IN	Full Duplex is an input from the physical layer component indicating if it has switched into or out of full duplex mode. $\overline{\text{FDX}}$ is active low.
FULHAL	6	OUT	When active, indicates 82557 is in full duplex mode. This pin is multiplexed with the TXD1 pin and operates only when in 10 Mbps-only mode.
MDIO	156	TS	Management Data Input/Output. Bidirectional signal between the 82557 and an MII-compatible PHY. It is used to transfer control information and status between the 82557 and the PHY. Control information is driven by the 82557 on the MDIO synchronously to MDC and sampled synchronously by PHY. Status information is driven synchronously by PHY and sampled synchronously by 82557.
MDC	157	OUT	Management Data Clock. Timing reference for transfer of control information and status on the MDIO signal. The frequency of this clock is up to 2.5 MHz.

2.4 Power and Ground

Symbol	Pin	Type	Name and Function
V_{CC}	4, 9, 12, 16, 21, 28, 32, 37, 42, 45, 51, 57, 63, 69, 75, 79, 83, 88, 92, 97, 100, 106, 110, 113, 117, 122, 126, 132, 137, 159	IN	Power: +5V ±5%.
V_{SS}	5, 10, 11, 17, 22, 29, 33, 38, 41, 46, 52, 58, 64, 70, 76, 80, 84, 87, 91, 95, 99, 105, 111, 112, 116, 121, 125, 131, 136, 160	IN	Ground: 0V.

3.0 82557 ARCHITECTURE OVERVIEW

Figure 1 (on the cover) shows a high level block diagram of the 82557 part. It is divided into three main subsystems: a parallel subsystem, a FIFO subsystem and the 10 Mbps/100 Mbps CSMA/CD unit.

3.1 Parallel Subsystem Overview

The parallel subsystem is broken down into several functional blocks: a PCI Bus Master Interface, a Micro Machine processing unit and its corresponding microcode ROM and a PCI Target Control/FLASH/EEPROM interface. The parallel subsystem also interfaces to the FIFO subsystem, passing data (XMT, RCV and Configuration), command and status parameters between these two blocks.

The PCI Bus Master Interface provides a complete interface to a PCI bus and is compliant with revision 2.1 of the PCI Bus Specification. No external logic is required to interface the 82557 to a PCI bus. The 82557 provides 32 bits of addressing and data, as well as the complete control interface to operate on a PCI bus. As a PCI Target, it follows the PCI Configuration format which allows all accesses to the 82557 (control register, FLASH accesses, boot, etc.) to be automatically mapped into free memory and I/O space upon initialization of a PCI system. For processing of XMT and RCV frames, the 82557 operates as a master on the PCI bus, initiating zero wait state transfers for accessing these data parameters.

The PCI Bus Master Interface consists of three units. The Bus Interface Unit (BIU) controls the access to the PCI bus according to the bus protocol. The BIU controls such actions as initiating when to request or relinquish the external PCI bus and handles internal DMA (XMT, RCV, or Control) channel arbitration. The Data Interface Unit (DIU) routs data into and out of the 82557 at high speed data transfers. The DMA unit controls the addressing for four separate DMA channels.

The 82557 Control/Status Register Block is contained as part of the PCI Target element. The Control/Status Register Block consists of the following 82557 internal control registers: SCB, PORT, FLASH control register, EEPROM control register and MDI Control register. Refer to the 82557 User's Guide for more information on the Control/Status Register Block.

The Micro Machine is an embedded processing unit contained in the 82557. The Micro Machine accesses the 82557 microcode ROM working its way through the op-codes (or instructions) contained in the ROM to perform its functions. Parameters accessed from memory such as Transmit Buffer Descriptor fields or pointers to data buffers are also used by the Micro Machine during processing of RCV or XMT frames by the 82557. A typical function of the Micro Machine would be to take a data buffer pointer field and load it into the 82557 DMA unit for direct access to the data buffer. The Micro Machine is divided into two units, a Receive Unit and a Command Unit (including XMT functions). These two units operate independently and concurrently. Control is switched between the two units according to the microcode instruction flow. The independence of the Receive and Command units of the Micro Machine allows the 82557 to execute commands and receive incoming frames simultaneously, with no real-time CPU intervention.

The 82557 contains an interface to both an external FLASH memory and an external serial EEPROM. The FLASH interface, which could also be used to connect to any standard 8-bit EPROM device, provides up to 1 MByte of addressing to the FLASH. It utilizes a multiplexed address scheme that works in conjunction with an LS373 or compatible latch to demultiplex the address. Both Read and Write accesses are supported. Without the latch, up to 16 Kbytes can be addressed. The FLASH may be used for remote boot functions, network statistical and diagnostics functions, etc. The FLASH is mapped into host system memory (anywhere within the 32-bit memory address space) for software accesses. It is also mapped into an available boot expansion ROM location during boot time of the system. For more information on the FLASH interface, see Section 4.1.3. The EEPROM is used to store relevant information for a LAN connection such as Node Individual Address, as well as board manufacturing and configuration information. Both Read and Write accesses to the EEPROM are supported by the 82557. For more information on the EEPROM interface, see Section 4.1.3.

3.2 FIFO Subsystem Overview

The 82557 FIFO subsystem consists of a large transmit FIFO and large receive FIFO. Each FIFO is unidirectional and independent of the other. The FIFO subsystem serves as the interface between the 82557 parallel side and the serial CSMA/CD unit. It provides a temporary buffer storage area for frames as they are either being received or transmitted by the 82557. This allows for several important features in the 82557:

- Transmit frames can be queued within the XMT FIFO, allowing back to back transmission within the minimum inter-frame spacing (IFS).
- The storage area in the FIFO area allows the 82557 to withstand long PCI Bus latencies without losing incoming data or corrupting outgoing data.
- The 82557 XMT FIFO Threshold allows the transmit start threshold to be tuned to eliminate underruns while concurrent transmits are being performed.
- The FIFO subsection allows extended PCI 0 Wait State burst accesses to or from the 82557 for both RCV and XMT frames, since the transfer is to the FIFO storage area as opposed to directly to the serial link.
- Transmissions resulting in errors (CDT, Underrun) are retransmitted directly from the 82557 FIFO, increasing performance and eliminating the need to reaccess this data from the host system.
- Incoming Runt RCV Frames (less than the legal minimum frame size) can be discarded automatically by the 82557 without transferring this faulty data to the host system.

3.3 10 Mbps/100 Mbps Serial CSMA/CD Unit Overview

The CSMA/CD unit of the 82557 allows it to be connected to either a 10 Mbps or 100 Mbps Ethernet network. The 82557 interfaces to either an IEEE 802.3 10 Mbps/100 Mbps MII compatible PHY device or a 10 Mbps-only IEEE 802.3 PHY. In the case of the MII compatible PHY, the 82557 can switch automatically between 10 Mbps or 100 Mbps operation depending on the speed of the network. The CSMA/CD unit performs all of the functions of the 802.3 protocol such as frame formatting, frame stripping, collision handling, deferral to link traffic, etc. The CSMA/CD unit can also be placed in a Full Duplex mode which allows for simultaneous transmission and reception of frames. The CSMA/CD unit accepts data from the 82557 XMT FIFO and converts it to either serial or nibble-wide (MII Compatible mode) data for transmission on the link. During reception, the CSMA/CD unit converts data from either serial or nibble-wide data to a byte-wide format and transfers it to the RCV FIFO of the 82557. The CSMA/CD unit contains a Management Data Interface (MDI) to an MII compliant PHY. This allows control and status parameters to be passed between the 82557 and the PHY (parameters specified by software) by one serial pin and a clocking pin, reducing the number of control pins needed for PHY mode control.

4.0 THE 82557 HARDWARE INTERFACE

4.1 PCI Bus Interface

The PCI bus interface enables the 82557 to interact with the host system via the PCI bus. It provides the control, address and data interface to implement a

PCI compliant interface. The 82557 operates as both a master and slave on the PCI bus. As a master, the 82557 interacts with the system main memory to access data for transmission or deposit received data.

As a slave, some 82557 control structures are accessed by the host CPU which reads or writes to these on-chip registers. The CPU provides the 82557 with the necessary action commands, control commands and pointers which enable the 82557 to process RCV and XMT data. The PCI bus interface also provides the means for configuring PCI parameters in the 82557. Refer to the *PCI Bus Interface Specification* for more details specific to the PCI bus.

4.1.1 PCI CONFIGURATION

The configuration process in a PCI system starts before anything else. The 82557 is actually disconnected from the PCI bus until it is configured. At this stage it responds to configuration cycles only. This subsection provides a detailed description of the PCI configuration process from S/W and H/W point of view. Specifically, it defines the programming model and usage rules for the configuration register space of the 82557.

The 82557 supports all mandatory required registers along with specific registers that are needed for its operation. Mainly, it implements several Base Address registers. These registers and their purpose will be described in details later on. For more concise information refer to the *PCI System Design Guide*.

4.1.1.1 PCI Configuration Space Organization

The organization of configuration space registers as defined in the PCI specification is shown in Figure 3. This region consists of fields that uniquely identify the 82557 and allow it to be generically controlled. The 82557 treats configuration space write operations to reserved registers as no-ops (the data written is ignored). Read accesses to reserved or undefined registers will always return a data value of all zeros. For all accesses to the PCI Configuration Registers, the 82557 will disconnect from the bus following each access. In other words, no burst accesses may be made to these registers.

Figure 3 shows the layout of the 64-byte predefined header portion of the 256-byte configuration space that every PCI device must support. These registers are known as the PCI Configuration Registers in the 82557. Devices must place any necessary device specific registers only in locations 64 through 255. Currently, the 82557 does not implement any register beyond the 64-byte predefined header portion. All multibyte numeric fields follow little-endian ordering. That is, lower addresses contain the least significant parts of the field. Software must take care to deal correctly with bit-encoded fields that have some bits reserved for future use.

On reads, software must use appropriate masks to extract the defined bits, and may not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and the data then written back. Section 4.1.2 describes the registers in the predefined header portion of the configuration space. It also specifies which registers are reserved and which ones are implemented.

The predefined header portion of the configuration space is divided into two parts. The first 16 bytes are defined the same for all types of PCI compliant devices. The 82557, as a PCI compliant device, supports the Vendor ID, Device ID, Command and Status fields in the header. Implementation of the other registers is optional (i.e., they can be treated as reserved registers). The specific implementation of these resisters in the 82557 is described in Section 4.1.2.

4.1.1.2 PCI Configuration Registers

This section lists and describes all PCI registers defined in the predefined header portion of the configuration space that are supported and implemented in the 82557. All reserved registers are also specified.

Configuration space is intended for configuration, initialization, and catastrophic error handling functions. Its use should be restricted to initialization software and error handling software. All operational software must continue to use I/O and/or memory space accesses to manipulate device registers. The PCI configuration registers are described while partitioned into several groups according to their functionality.

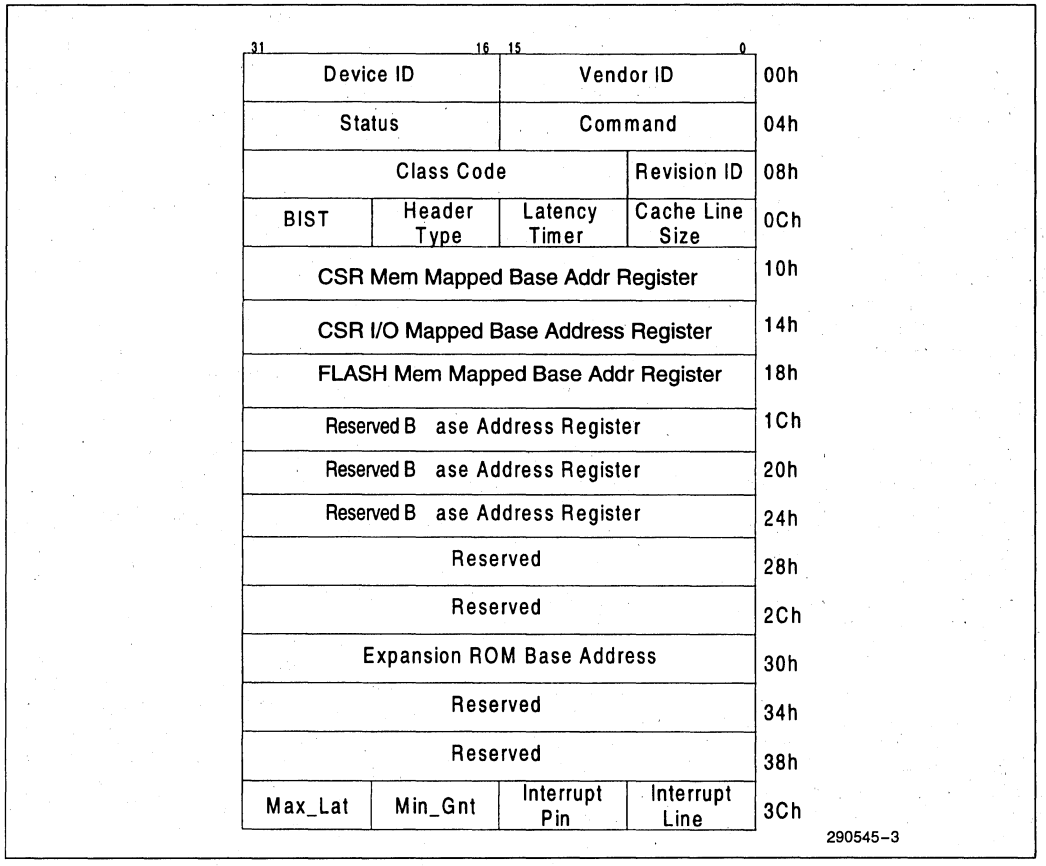


Figure 3. PCI Configuration Registers

4.1.1.2.1 DEVICE IDENTIFICATION REGISTERS

Five fields in the predefined header deal with device identification. The 82557, as a PCI compliant device, implements them as required. These registers (fields) enable generic configuration software to easily determine what devices are available on the system's PCI bus(ses). All of these registers are read-only. The description of their functionality and their assigned value in the 82557 is given in Table 1. Their location (offset) in the PCI configuration space in given in Figure 3.

4.1.1.2.2 PCI COMMAND REGISTER

The PCI Command Register provides control over the 82557's ability to generate and respond to PCI cycles. When a 0 is written to this register, the 82557 is logically disconnected from the PCI bus for all accesses except configuration accesses. Figure 4 shows the layout of the register and Table 2 explains the meanings of the different bits in the Command register. Table 2 also gives the default value of this register upon power up and the specific implementation of individual bits in the 82557 (i.e., R/O or R/W).

Table 1. Device Identification Registers

Register	Description
Vendor ID	This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. The vendor ID value for the 82557 is always 8086 and is read-only.
Device ID	This field identifies the particular device. This identifier is allocated by the vendor. The device ID for the 82557 is 1229 and is read-only.
Revision ID	This read-only register specifies the 82557 stepping.
Header Type	This byte identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. The 82557 Header Type of 00h specifies the layout shown in Figure 3 and indicates a single function device. This field is read-only.
Class Code	The Class Code register is read-only and is used to identify the generic function of the device and (in some cases) a specific register-level programming interface. The register is broken into three byte-size fields. The upper byte, 02h is a base class code and specifies the 82557 as a Network Controller. The middle byte is a sub-class code, 00h which specifies Ethernet Controller. The lower byte identifies a specific register-level programming interface and the 82557 always returns 00h in this field.

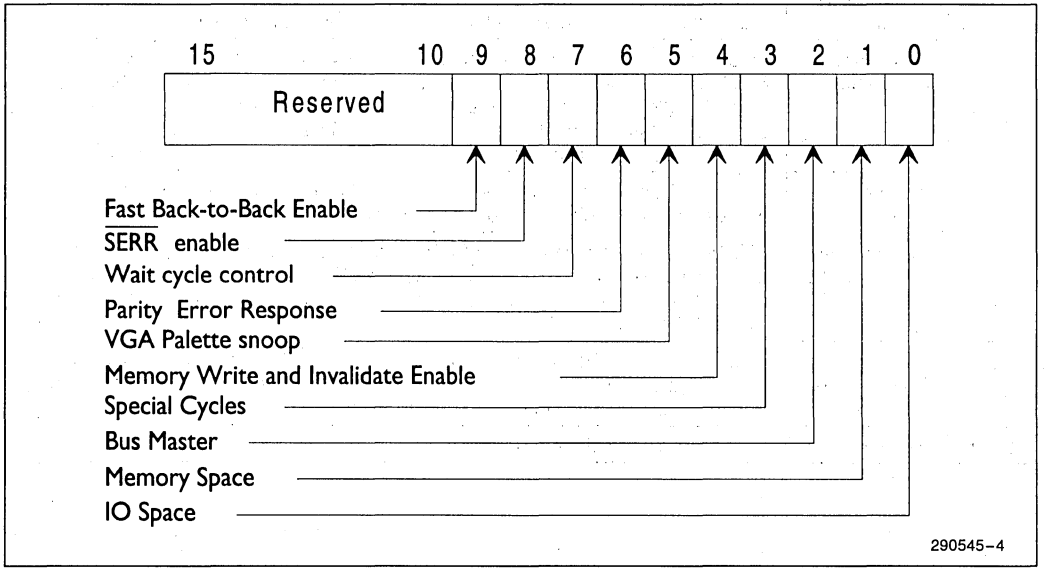


Figure 4. PCI Command Register Layout

Table 2. PCI Command Register Bits

Bit #	Bit Name	Description
0	IO Space	Controls a device's response to I/O space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O space accesses. The specific implementation of this bit in the 82557 is configurable with default value 0.
1	Mem Space	Controls a device's response to memory space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory space accesses. This bit is configurable in the 82557 with a default value 0.
2	Bus Master	Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. This bit is configurable in the 82557 with a default value 0.
3	Special Cycle	Controls a device's action on Special Cycle operations. A value of 0 causes the device to ignore all Special Cycle operations. This bit is always set to 0 in the 82557.
4	Mem WR & Invalidate En	This is an enable bit for using the Memory Write and Invalidate command. This bit is always set to 0 in the 82557 (disabled).
5	VGA Palette Snoop	This bit controls how VGA compatible devices handle accesses to their palette registers. This bit is always set to a 0 in the 82557 (disabled).
6	Parity Error Response	This bit controls the 82557's response to parity errors. When the bit is set, the 82557 takes its normal action when a parity error is detected. When the bit is reset, the 82557 ignores any parity errors that it detects and continues normal operation. This bit must be set to 0 after $\overline{RST}$. This bit is configurable in the 82557 with a default value 0.
7	Wait Cycle Control	This bit, when set to a 1, is used to control whether or not a device does address/data stepping. This bit is always set to 0 in the 82557 (disabled).
8	Serr Enable	This bit is an enable bit for the $\overline{SERR}$ driver. A value of 0 disables the $\overline{SERR}$ driver. A value of 1 enables the $\overline{SERR}$ driver. This bit (and bit 6, $\overline{Perr}$ Enable) must be on to report address parity errors. This bit is configurable in the 82557 with a default value of 0.
9	Fast Back-to-Back Enable	This bit controls whether or not a master can do fast back-to-back transactions to different devices. This bit is set to a 0 in the 82557, fast back-to-back transactions are only allowed to the same agent.
10–15	Reserved	Reserved. These bits are hardwired to 0 in the 82557.

4.1.1.2.3 PCI STATUS REGISTER

The PCI Status Register is used to record status information for PCI bus related events. The definition of each of the bits is given in Table 3 and the layout of the register is shown in Figure 5. The specific implementation of each bit in the 82557 is also given in Table 4. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

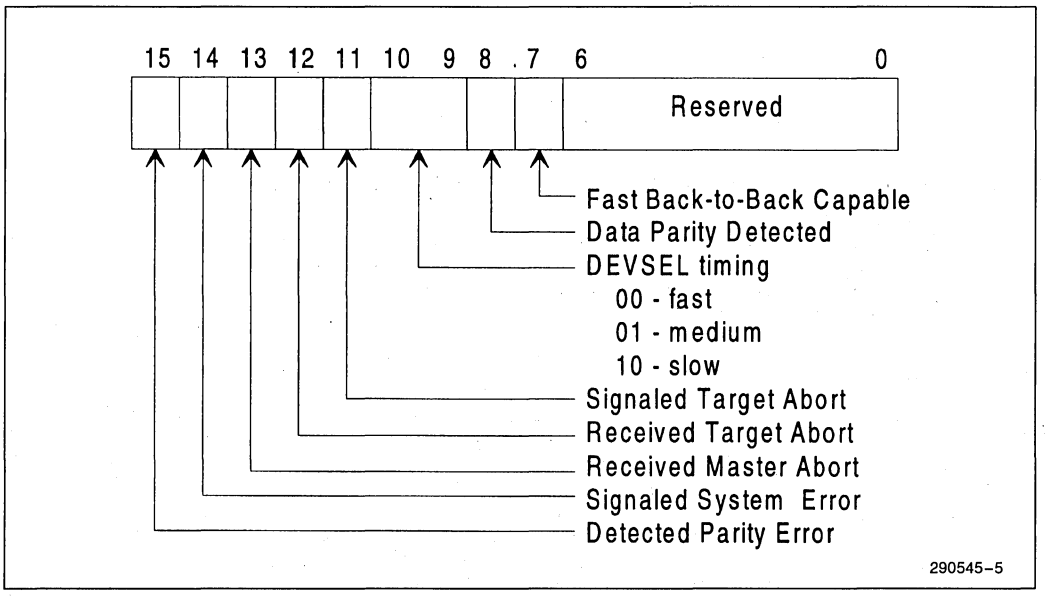


Figure 5. PCI Status Register Layout

Table 3. PCI Status Register Bits

Bit #	Bit Location	Description
0–6	Reserved	Reserved. These bits are hardwired to 0 in the 82557.
7	Fast Back-to-Back Capable	This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. The value of this bit in the 82557 is 1 (Fast Back-to-Back Capable).
8	Data Parity Detected	This bit is set when three conditions are met: 1) the bus agent asserted $\overline{\text{PERR}}$ itself or observed $\overline{\text{PERR}}$ asserted; 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; 3) the Parity Error Response bit (Command Register) is set. The initial value of this bit in the 82557 is 0.
9–10	$\overline{\text{DEVSEL}}$ Timing	These bits encode the timing of $\overline{\text{DEVSEL}}$. There are three allowable timings for assertion of $\overline{\text{DEVSEL}}$. These are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). The value of these bits are always set to 01 (medium).
11	Signaled Target Abort	This bit must be set by a target device whenever it terminates a transaction with target-abort. The value of this bit is always 0.
12	Received Target Abort	This bit must be set by a master device whenever its transaction is terminated with target-abort. The initial value of this bit in the 82557 is 0.
13	Received MasterAbort	This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with master-abort. The initial value of this bit in the 82557 is 0.
14	Signalled System Error	This bit must be set whenever the device asserts $\overline{\text{SERR}}$. The initial value of this bit in the 82557 is 0.
15	Detected Parity Error	This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register). The initial value of this bit in the 82557 is 0.

4.1.1.2.4 MISCELLANEOUS PCI CONFIGURATION REGISTERS

This section describes the registers that are device independent and only need to be implemented by devices that provide the described function. The specific implementation of each register for the 82557 is also provided.

4.1.1.2.5 BASE ADDRESS REGISTERS

One of the most important functions for enabling superior configurability and ease of use is the ability to relocate PCI devices in the address spaces. At system power-up device independent software must be able to determine what devices are present, build a consistent address map, and determine if a device has an expansion ROM.

The 82557 contains three Base Address registers, two requesting memory mapped resources, and one requesting I/O mapping. Each register is 32 bits wide. The least significant bit in each base address register determines whether it represents an I/O or memory space. Figures 6 and 7 show the layout of a Base Address register for both I/O and memory mapping. After determining this information, power-up software can map the I/O and memory controllers into available locations and proceed with system boot. In order to do this mapping in a device independent manner, the base registers for this mapping are placed in the predefined header portion of configuration space. Device drivers can then access this configuration space to determine the mapping of a particular device.

Bit 0 in all base registers is read-only and used to determine whether the register maps into Memory or I/O space. Base registers that map to Memory space must return a 0 in bit 0. Base registers that map to I/O space must return a 1 in bit 0.

Base registers that map into I/O space are always 32 bits with bit 0 hardwired to a 1, bit 1 is reserved and must return 0 on reads, and the other bits are used to map the device into I/O space.

Table 4. Miscellaneous PCI Configuration Bits

Register	Description
Cache Line Size	This register is not implemented in the 82557. The value of this field is fixed to 0.
Latency Timer	The 82557, as a master device, implements this register to limit the size of very long burst cycles. The initial value is 0 and is then programmed by system BIOS at initialization time.
Built-In Self Test (BIST)	This optional register is used for control and status of BIST. The 82557 will not provide PCI BIST and the value of this field is always set to 0.
Interrupt Line	The Interrupt Line register is an 8-bit register used to communicate interrupt line routing information. This register is configurable in the 82557. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. Device drivers and operating systems can then use this information to determine priority and vector information.
Interrupt Pin	The Interrupt Pin register tells which interrupt pin the device (or device function) uses. This eight bit register is always set to a 1 in the 82557, indicating $\overline{INTA}$ is used.
MIN_GNT/ MAX_LAT	These read-only byte registers are used to specify the devices desired settings for Latency Timer values. For both registers, the value specifies a period of time in units of microsecond. MIN_GNT is used for specifying how long a burst period the device needs assuming a clock rate of 33 MHz. MAX_LAT is used for specifying how often the device needs to gain access to the PCI bus. The values of these registers are 8h (2 μs) for MIN_GNT and 38h (14 μs) for MAX_LAT.

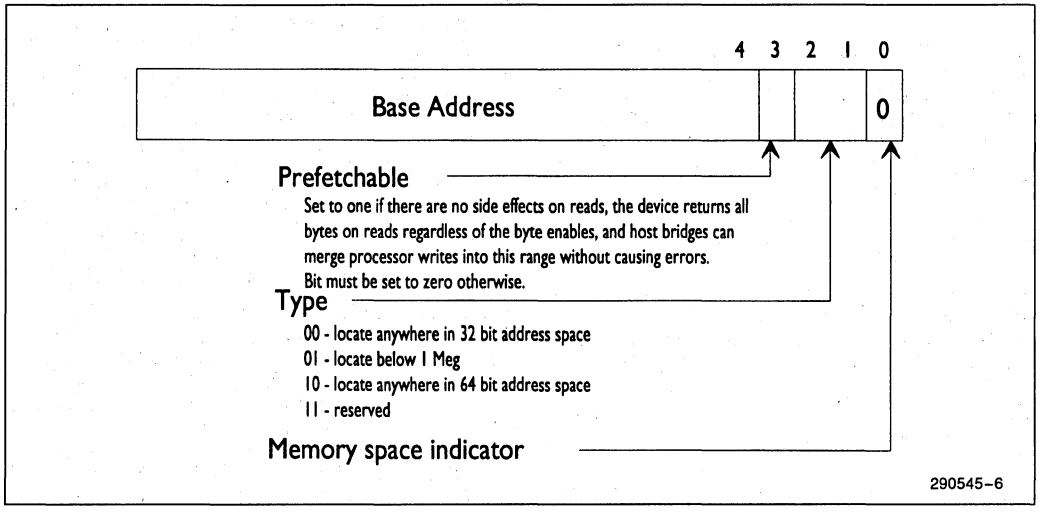


Figure 6. Base Address Register for Memory Mapping

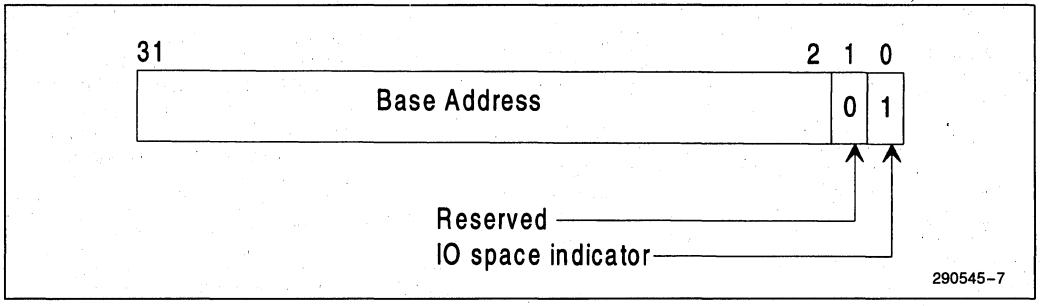


Figure 7. Base Address Register for I/O

The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. A device that wants a 1 MB memory address space would set the most significant 12 bits of the base address register to be configurable, setting the other bits to 0.

For its Control/Status Registers (CSR), the 82557 requires one Base Address Register to I/O Map these registers, and one Base Address Register to Memory Map these registers anywhere within the 32-bit memory address space. It is up to the software driver to determine which Base Address Register (I/O or Memory) to use to access the 82557 Control/Status registers. Both are always requested by the 82557. The 82557 requires one Base Address Register to map the accesses to an optional FLASH memory. The size of the space requested is 1 MB, and it is always mapped anywhere in the 32-bit memory address space. Table 5 describes the implementation of the Base Address Registers in the 82557.

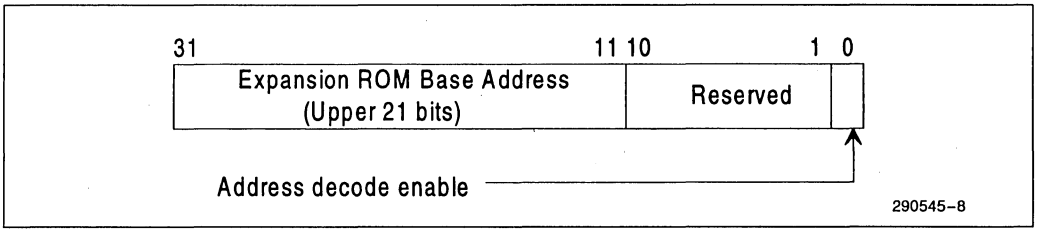


Figure 8. Expansion ROM Base Address Register Layout

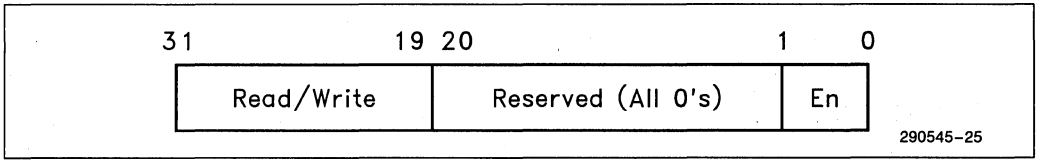


Figure 9. 82557 Expansion ROM Base Address Register Format

Table 5. 82557 Base Address Registers

Register Location	Description
10h	Memory space for the 82557 Control/Status Registers. The size of this space is 4 Kbytes. It will be marked as a prefetchable space and is mapped anywhere in the 32-bit memory address space.
14h	I/O space for 82557 Control/Status Registers. The size of this space is 32 bytes.
18h	Memory space for the 82557 flash buffer for accesses above 1 MB. The size of this space is 1 MB. It will be marked as a non-prefetchable space and is mapped anywhere in the 32-bit address space.
1C–27h	Reserved. 82557 returns 0.

4.1.1.2.6 EXPANSION ROM BASE ADDRESS REGISTER

The 82557 provides an interface to a local FLASH (or EPROM) which can be used as an expansion ROM. A 32-bit Expansion ROM Base Address Register at offset 30h in the configuration space is defined to handle the address and size information for boot-time access to the FLASH. Figure 8 shows how this register is organized. The register functions exactly like a 32-bit Base Address register except that the encoding (and usage) of the bottom bits is different. The upper 21 bits correspond to the upper 21 bits of the Expansion ROM base address. The 82557 allows its Expansion ROM to be mapped on any 1 MB boundary. The most significant 12 bits are configurable to indicate the 1 MB size requirement.

Bit 0 in the register is used to control whether or not the device accepts accesses to its expansion ROM. When this bit is reset, the device's Expansion ROM address space is disabled. This bit is programmed at initialization time by the system BIOS. The Memory Space bit in the Command register has precedence over the Expansion ROM enable bit. A device responds to accesses to its expansion ROM only if both the Memory Space bit and the Expansion ROM Base Address Enable bit are set to 1 (it is reset to 0 on Reset).

4.1.1.3 PCI Configuration Cycles

As already mentioned, the PCI definition provides for totally software driven initialization and configuration via a separate configuration address space. This section provides a description of the PCI commands for accessing the PCI configuration space. For more concise information please refer to the latest revision of the PCI Local Bus Specification.

For normal accesses (i.e., memory or I/O), each device decodes its own addresses. In configuration accesses, the device selection decoding is done externally, and signaled to the PCI device via the IDSEL pin. The 82557 becomes the target of a configuration command (RD or WR) only if its IDSEL is asserted and AD0–1 are 00 during the address phase of the command. The addressed register in the configuration space is determined by AD2–7 and $\overline{BE0–3}$ lines. The 82557 will support non-burst configuration accesses of a BYTE, WORD, or DWORD. Read and Write configuration cycles are shown in Figures 10 and 11.

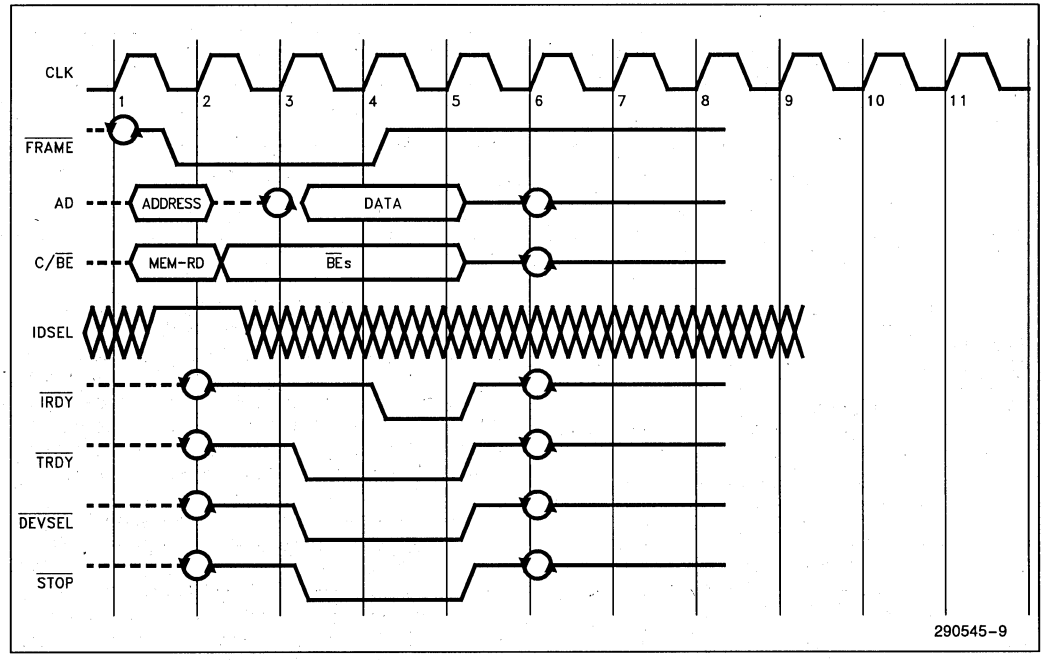


Figure 10. Configuration Read Cycle

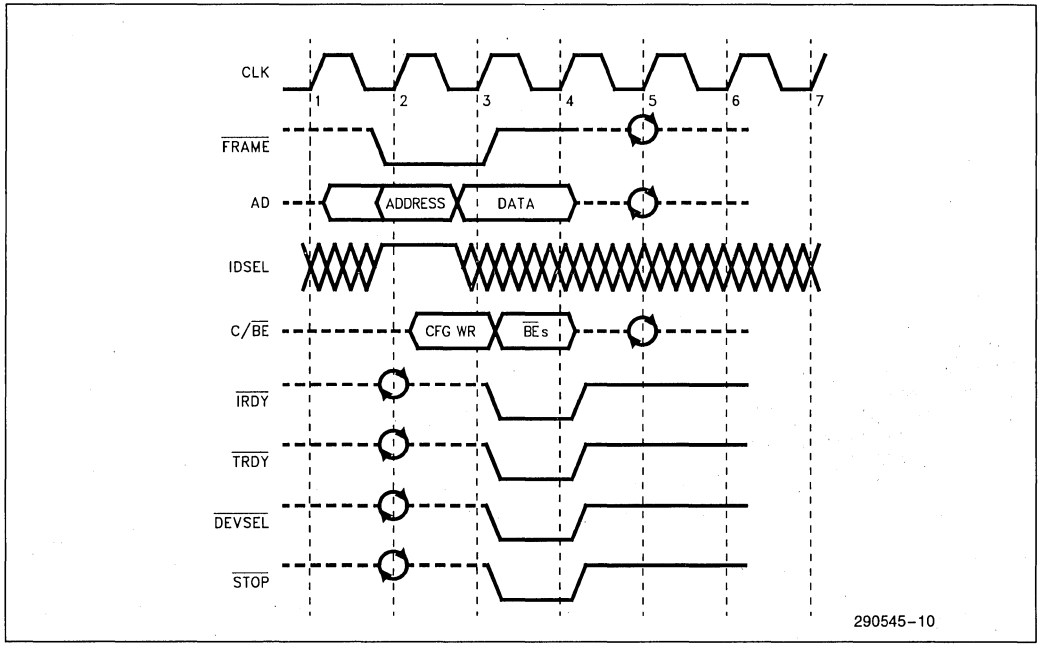


Figure 11. Configuration Write Cycle

4.1.2 82557 BUS OPERATIONS

4.1.2.1 General Overview

After configuration, the 82557 is ready for its normal operation. As a Fast Ethernet Controller, the role of the 82557 is to access transmitted data or deposit received data. In both cases the 82557, as a bus master device, will initiate memory cycles via the PCI bus to fetch/deposit the required data.

In order to perform these actions, the 82557 is controlled and examined by the CPU via its control and status structures and registers. Some of these control and status structures reside on chip and some reside in system memory. For access to its Control/Status Registers (CSR), the 82557 serves as a slave (target). The 82557 serves as a slave also while the CPU accesses its 1 MB Flash buffer or its EEPROM. The next subsection describes the 82557 slave operation. It is followed by a description of the 82557 operation as a bus master (initiator).

4.1.2.1.1 82557 SLAVE BUS OPERATION

The 82557 serves as a Slave in one of the following cases:

- CPU accesses to the 82557 SCB control and status structures (CSR).
- CPU accesses to the EEPROM through its control register (CSR).
- CPU accesses to the 82557 PORT address (CSR).
- CPU accesses to the MDI control register (CSR).
- CPU accesses to the FLASH control register (CSR).
- CPU accesses to the 1 MB FLASH.

The CSR and the 1 MB Flash buffer are considered by the 82557 as two totally separated memory spaces. The 82557 provides separate Base Address Registers in the configuration space to distinguish between them. The size of the control and status registers memory space is 32 bytes in the I/O space and 4 Kbytes in the memory space. The 82557 treats accesses to these memory spaces differently. For more information, refer to the *82557 User's Guide*.

4.1.2.1.2 CONTROL/STATUS REGISTERS (CSR) ACCESSES

The 82557 supports zero wait state single cycle I/O, or memory mapped accesses to its CSR space. Separate base address registers request 32 bytes of both memory and I/O space to accomplish this. Based on its needs, the software driver will use either I/O or memory mapping to access these registers. The 82557 provides 32 valid bytes of CSR, which include the following elements:

1. SCB.
2. PORT.
3. FLASH control register.
4. EEPROM control register.
5. MDI Control register.

Figures 12 and 13 show CSR read and write cycles. They show general zero wait state I/O read and write cycles. In case of accessing the Control and Status structures, the CPU is the initiator and the 82557 is the target of the transaction.

Read Accesses: The CPU, as the initiator, drives the address lines AD0–31, the command and byte enable lines C/$\overline{BE0-3}$ and the control lines $\overline{IRDY}$ and $\overline{FRAME}$. As a slave, the 82557 controls the $\overline{TRDY}$ signal and provides valid data on each data access. The 82557 allows the CPU to issue only one read cycle when it accesses the Control and Status registers, generating a Disconnect by asserting the $\overline{STOP}$ signal. The CPU can insert wait states by deasserting $\overline{IRDY}$ when it is not ready.

Write Accesses: The CPU, as the initiator, drives the address lines AD0–31, the command and byte enable lines C/$\overline{BE0-3}$ and the control lines $\overline{IRDY}$ and $\overline{FRAME}$. It also provides the 82557 with valid data on each data access immediately after asserting $\overline{IRDY}$. The 82557 controls the $\overline{TRDY}$ signal and asserts it from the data access. As for read cycles, the 82557 allows the CPU to issue only one I/O write cycle to the Control and Status registers, generating a Disconnect by asserting the $\overline{STOP}$ signal. This is true for both memory mapped and I/O mapped accesses.

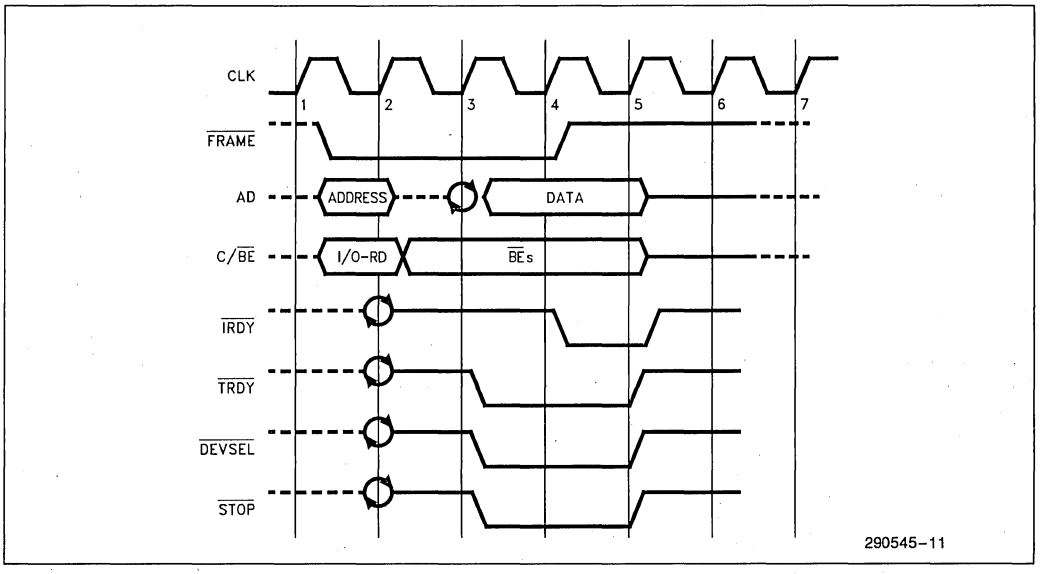


Figure 12. CSR Read Cycles

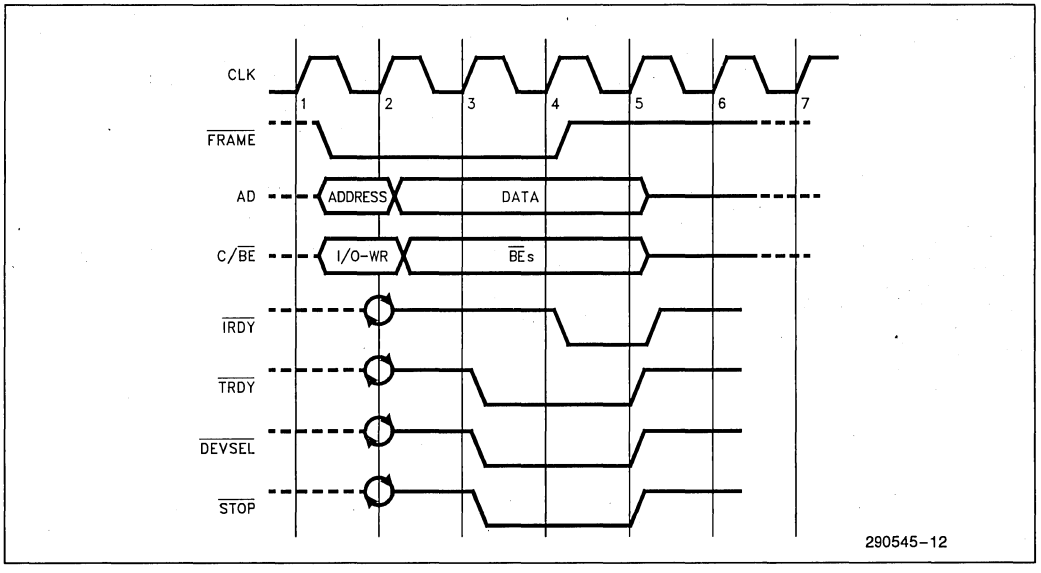


Figure 13. CSR Write Cycle

4.1.2.1.3 FLASH BUFFER ACCESSES

The CPU accesses to the Flash Buffer are very slow. For this reason the 82557 issues a *target-disconnect* at the first data access. The 82557 asserts the $\overline{STOP}$ signal to indicate a *target-disconnect*. Figures 14 and 15 show memory CPU read and write accesses to the 1 MB Flash Buffer. The longest Burst cycle to the Flash Buffer contains one data access only.

Read Accesses: The CPU, as the initiator, drives the address lines AD0–31, the command and byte enable lines C/$\overline{BE0-3}$ and the control lines $\overline{IRDY}$ and $\overline{FRAME}$. The 82557 controls the $\overline{TRDY}$ signal and deasserts it for a certain number of clocks until valid data can be read from the Flash Buffer. When $\overline{TRDY}$ is asserted, the 82557 drives valid data on the AD0–31 lines. The CPU can also insert wait states by deasserting $\overline{IRDY}$ until it is ready. Flash buffer read accesses can be byte or word length. See NOTE in Section 4.2 for additional information.

Write Accesses: The CPU, as the initiator, drives the address lines AD0–31, the command and byte enable lines C/$\overline{BE0-3}$ and the control lines $\overline{IRDY}$ and $\overline{FRAME}$. It also provides the 82557 with valid data immediately after asserting $\overline{IRDY}$. The 82557 controls the $\overline{TRDY}$ signal and deasserts it for a certain number of clocks until valid data is written to the Flash Buffer. By asserting $\overline{TRDY}$, the 82557 signals the CPU that the current data access is completed. Flash buffer write accesses can be byte length only. See NOTE in Section 4.2 for additional information.

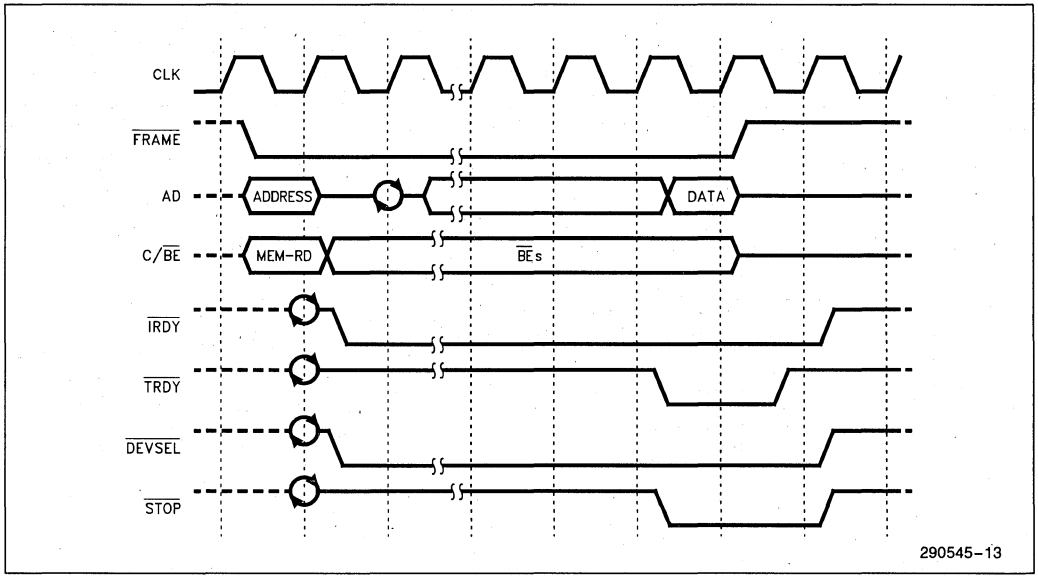


Figure 14. Flash Buffer Read Cycles

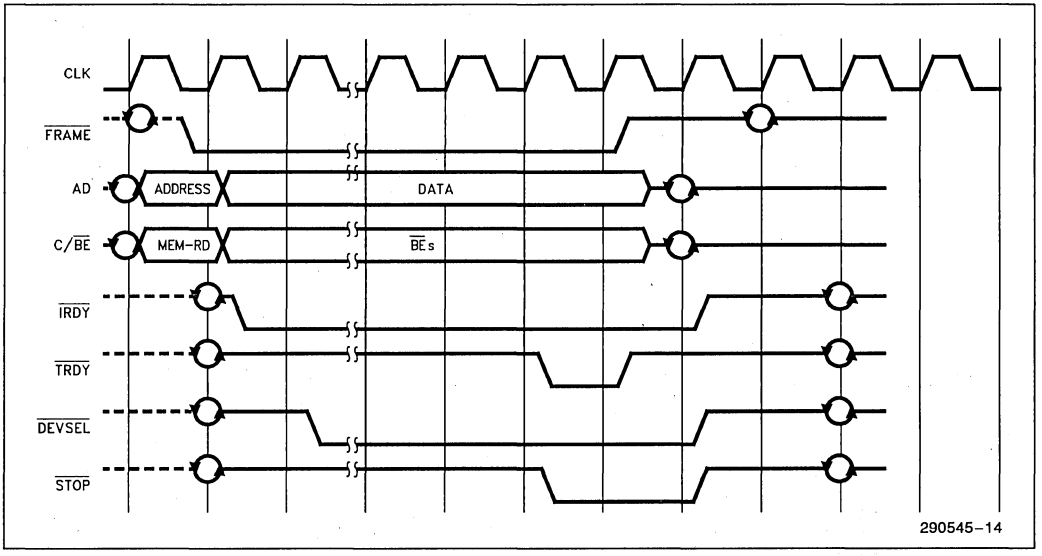


Figure 15. Flash Buffer Write Cycle

4.1.2.1.4 ERROR HANDLING

Data Parity Errors: The 82557 checks for data parity errors while it is the target of the transaction. If an error was detected, the 82557 always sets the Detected Parity Error bit (PCI Status Register, bit 15). The 82557 also asserts PERR, if the Parity Error Response bit is set (PCI Command Register, bit 6). The 82557 does not attempt to terminate a cycle in which a parity error was detected. This gives the initiator of the access, at each H/W or S/W level, the option of recovery.

Target-Disconnect: The 82557 will use premature termination in the following cases:

- After accesses to the 1 MB Flash buffer.
- After accesses to its CSR.
- After accesses to the configuration space.

System Error: The 82557 reports parity error on address phase using the SERR pin. If the SERR Enable bit (in the PCI-configuration command register) or the Parity Error Response bit are not set, the 82557 only sets the Detected Parity Error bit (PCI Status Register, bit 15). If SERR Enable and Parity Error Response bits are both set, the 82557 sets the Signaled System Error bit (PCI Status Register, bit 14) as well as the Detected Parity Error bit and asserts SERR for one clock.

The 82557, when detecting system error, will claim the cycle if it was the target of the transaction and continue the transaction as though the address was correct.

NOTE:
The 82557 will report a system error for any parity error on address phase, whether or not it is involved in the current transaction.

4.1.2.1.5 82557 BUS MASTER OPERATION

As a PCI Bus Master, the 82557 initiates memory cycles to fetch data for transmission or deposit received data, as well as for accessing the memory resident control structures. The 82557 performs zero wait state burst read and write cycles to the host main memory. Figures 16 and 17 depict memory read and write burst cycles. For Bus Master cycles, the 82557 is the initiator and the host main memory (or the PCI Host Bridge depending on the configuration of the systems) is the target.

The CPU provides the 82557 with action commands and pointers to the data buffers that reside in host main memory. The 82557 independently manages these structures and initiates burst memory cycles to transfer data to and from them. The 82557 uses MEM-RD Multiple for burst accesses to data buffers and MEM-RD LINE for burst accesses to control structures (commands, pointers, etc.). For all write burst accesses to either data or control, the 82557 uses the MEM-WR command. The 82557 does not use the MEM-WR and Invalidate command.

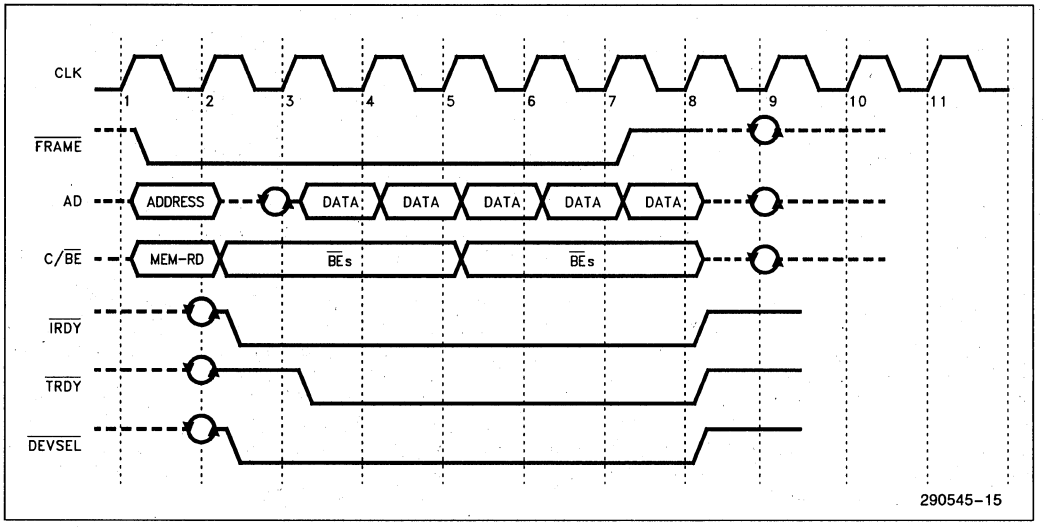


Figure 16. Memory Read Burst Cycles

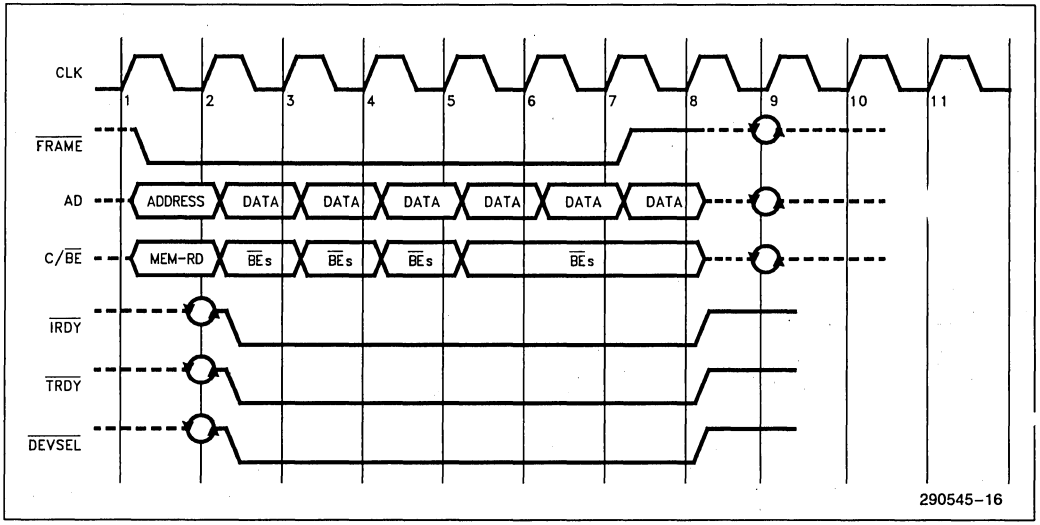


Figure 17. Memory Write Burst Cycle

Read Accesses: The 82557 performs block transfers from host system memory in order to perform frame transmission on the serial link. In this case, the 82557 initiates zero wait state memory read burst cycles for these accesses. The length of a burst is bounded by the system and also by the 82557 internal FIFO. The length of a read burst may also be bounded by the TX DMA MAXIMUM BYTE COUNT in the Configuration command.

The 82557, as the initiator, drives the address lines AD0–31, the command and byte enable lines C/$\overline{BE0-3}$ and the control lines $\overline{IRDY}$ and $\overline{FRAME}$. The 82557 asserts $\overline{IRDY}$ to support zero wait state burst cycles. The target signals the 82557 that valid data is ready to be read by asserting the $\overline{TRDY}$ signal.

Write Accesses: The 82557 performs block transfers to host system memory during frame reception. In this case, the 82557 initiates memory write burst cycles to deposit the data, usually without wait states. The length of a burst is bounded by the system and also by the 82557 internal FIFO threshold. The length of a write burst may also be bounded by the RX DMA MAXIMUM BYTE COUNT in the Configuration command.

The 82557, as the initiator, drives the address lines AD0–31, the command and byte enable lines C/$\overline{BE0-3}$ and the control lines $\overline{IRDY}$ and $\overline{FRAME}$. The 82557 asserts $\overline{IRDY}$ to support zero wait state burst cycles. The 82557 also drives valid data on AD0–31 lines during each data phase (from the first clock and on). The target controls the length and signals completion of a data phase by deassertion and assertion of $\overline{TRDY}$.

Cycle Completion: The 82557 completes (terminates) its initiated memory burst cycles in the following cases:

- Normal Completion: all data involved in the transaction has been transferred to or from the target (i.e., host main memory).
- Backoff: the Latency Timer has expired and the arbiter has removed the 82557 bus grant signal ($\overline{GNT}$), indicating that the 82557 has been preempted by another bus master.
- TX or RX DMA MAXIMUM BYTE COUNT: the 82557 burst has reached the length specified in the TX or RX DMA MAXIMUM BYTE COUNT field in the configuration block. Refer to the *82557 User's Guide* for more detailed information.
- Target Termination: the target may request to terminate the transaction with target-disconnect, target-retry, or target-abort. In the first two cases, the 82557 initiates the cycle again. In the case of a Target Abort, the 82557 sets the Received Target Abort bit in the PCI Status field (PCI Status Register, bit 12) and does not reinitiate the cycle.
- Master Abort: The target of the transaction has not responded to the address initiated by the 82557 ($\overline{DEVSEL}$ has not been asserted). The 82557 simply deasserts $\overline{FRAME}$ and $\overline{IRDY}$ as in the case of normal completion.
- Error Condition: In the event of parity or any other system error detection, the 82557 completes its current initiated transaction. Any further action taken by the 82557 depends on the type of error and other conditions.

Data Parity Errors: As an initiator, the 82557 checks and detects data parity errors that occur during a transaction. If the Parity Error Response bit is set (PCI Command Register, bit 6), the 82557 also asserts $\overline{PERR}$ and sets the Data Parity Detected bit (PCI Status Register, bit 8). In addition, if the error was detected by the 82557 during read cycles, it sets the Detected Parity Error bit (PCI Status Register, bit 15).

4.2 FLASH/EEPROM Interface

The local memory interface consists of an interface to a FLASH (or EPROM) and an interface to a serial EEPROM. The 82557 provides address decoding and control to allow access to up to 1 MB (megabyte) of FLASH. The EEPROM is used to store information such as Node Individual Address and board configuration.

4.2.1.1 Flash Interface Operation

The FLASH (or Boot EPROM) is read from or written to whenever the host CPU performs a read or a write operation to a memory location that is within the FLASH mapping window. All accesses to the FLASH, except read accesses, require the appropriate command sequence for the device used. Refer to the specific FLASH data sheet for more details on reading from or writing to FLASH. The accesses to the FLASH are based on a direct decode of CPU accesses to a memory window defined in either the 82557 FLASH Base Address Register (PCI Control Register at offset 18h) or the Expansion ROM Base Address Register (PCI Control Register at offset 30h). The 82557 asserts control to the FLASH when it decodes a valid access.

NOTE:
FLASH accesses must always be assembled or disassembled by the 82557 to or from the FLASH whenever the access is greater than a byte-wide access. Due to slow access times to a typical FLASH and in order to avoid violating PCI bus holding specifications (no more than 16 Wait States inserted for any cycles which are not system-initiation cycles), write commands should be byte accesses, and read commands should be byte or word accesses for any cycles that occur after system initialization. Boot ROM shadowing is an exception to the 16 clock rule.

Flash registers are described in the *82557 User's Guide*.

4.2.1.2 Serial EEPROM Interface

The Serial EEPROM, a Hyundai HY93C46 or equivalent IC, stores configuration data for the 82557. The EEPROM is a serial in/serial out device. Serial EEPROMs range in size from 16 to 256 registers of 16 bits per register. All accesses, either read or write, are preceded by a command instruction to the device. The command instructions, begin with a logical 1 as a start bit, two op code bits (indicating RD, WR, Erase, etc.) and n-bits of address. The address field varies with the size of the EEPROM, for example 6 bits for a 64 register EEPROM, or 8 bits for a 256 register device, etc. The end of the address field is indicated by a dummy 0 bit from the EEPROM which indicates the entire address field has been transferred to the device. A command is issued by asserting the CS signal and clocking the data into the EEPROM on its DI input relative to the SK (Shift Clock) input. The CS signal is deasserted after completion of the EEPROM cycle (Command, Address and Data). Figure 18 shows the EEPROM timing diagram.

The *82557 User's Guide* describes EEPROM access port and instruction sets.

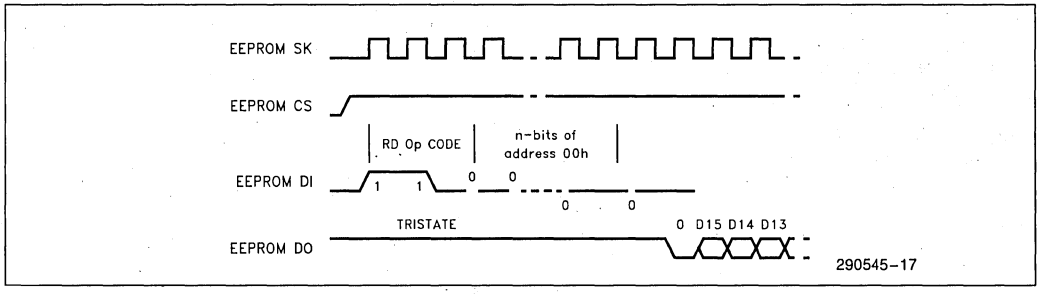


Figure 18. 82557 EEPROM Timing Diagram (Example Read from Address 0)

4.3 10 Mbps/100 Mbps CSMA/CD UNIT

The 82557 CSMA/CD unit implements both the IEEE802.3 10 Mbps and IEEE802.3u Fast Ethernet 100 Mbps standards. It performs all the CSMA/CD protocol functions such as transmission, reception, collision handling, etc. The 82557 CSMA/CD unit operates in two modes of operation; a 10 Mbps/100 Mbps MII compatible mode, in which the data stream is nibble-wide and the serial clocks run at either 25 MHz or 2.5 MHz, or a 10 Mbps-only mode, in which the data stream is bit-wide and the clocking is at 10 MHz. Selection of either MII compatible mode or 10 Mbps-only mode is by configuration.

The MII compatible mode, along with an MII-compatible 10/100 Serial PHY (physical interface such as the Intel 82553) switches automatically between either 10 Mbps or 100 Mbps operation depending on the speed of the network to which it is attached. During frame transmission, byte wide data is accepted from the 82557 internal FIFO block. The CSMA/CD unit builds the IEEE 802.3 frame format and depending on the mode, the frame is either transmitted as a bit stream (10 Mbps-only mode) or as a nibble stream (10 Mbps/100 Mbps MII mode). During frame reception the CSMA/CD unit converts the bit stream (10 Mbps-only mode) or nibble stream (10 Mbps/100 Mbps MII mode) to a byte wide format, strips off the frame delimiters as the preamble and SFD and then passes the data to the 82557 internal FIFO block from where it is deposited into host system memory via the 82557 PCI Bus Master interface.

4.3.1 10 Mbps/100 Mbps MII COMPATIBLE INTERFACE

The CSMA/CD unit provides the functional interface to any MII compatible serial PHY. The data path consists of a separate nibble-wide stream for both transmit and receive activities. Data transfers are clocked by the 25 MHz transmit and receive clocks in 100 Mbps operation, or by 2.5 MHz clocks in 10 Mbps operation. These clock inputs are driven by the PHY.

4.3.1.1 10 Mbps/100 Mbps MII Transmission

When the 82557 has a frame ready for transmission, it samples the link for activity. If the CRS signal is inactive (no activity on the link), frame transmission begins. The data is transmitted via pins TXD0–3, clocked on the rising edge of TXC. The signal TXEN is asserted at this same time. The CRS signal is expected to be asserted before one slot time has elapsed, however the transmission will complete successfully even if CRS is not asserted (the absence of CRS will be reported in a status bit). In the case of a collision, the PHY asserts the COL signal on the 82557 which will then stop transmitting the frame within four clock times and append a JAM sequence onto the link.

After the end of a collided transmission, the 82557 will back off and attempt to retransmit once the backoff timer expires. Note that the retransmission is done from the data stored internally in the 82557 FIFO block, so no reaccess to the data in host memory is performed. In the case of a successful transmission, the 82557 is ready to transmit any other frames queued in its FIFO block within the minimum inter frame spacing (IFS) of the link.

4.3.1.2 10 Mbps/100 Mbps MII Reception

Frame reception starts with the assertion of CRS (while the 82557 is not transmitting) by the PHY. Once RXDV is asserted, 82557 will begin sampling incoming data on pins RXD0–3 on the rising edge of RXC. There is a minimum of four RXC clock periods from assertion of CRS until the 82557 samples the first RCV data nibble from the PHY. The 82557 accepts frames which pass its address filtering mechanism, passing the frame in a byte-wide format to its internal FIFO block. Reception ends when CRS is deasserted by the PHY. The last nibble sampled by the 82557 is the nibble present on RXD0–3 on the RXCLK rising edge in which RXDV deassertion is detected and CRS is still asserted.

During reception the RXDV (Receive Data Valid) signal is asserted to the 82557. If, while RXDV is asserted, the 82557 detects the assertion of RXER, it will designate this frame as a corrupted frame by setting an error bit in the status field of the frame. The 82557 will continue to receive the incoming frame regardless of the RXER signal. While no reception is taking place, RXDV should remain deasserted.

4.3.2 10 Mbps/100 MII Mbps FULL DUPLEX OPERATION

When operating in Full Duplex mode the 82557 can transmit and receive frames simultaneously. In Full

Duplex mode the CRS signal is associated with received frames only and has no affect on transmitted frames. Similarly, COL is associated with transmission only and does not affect received frames.

Transmission starts when TXEN goes active. Transmission starts regardless of the state of CRS. Reception starts when the CRS signal is asserted indicating traffic on the RCV pair of the PHY.

4.3.3 10 Mbps-ONLY INTERFACE

The 10 Mbps mode is fully compliant with the IEEE 802.3 CSMA/CD standard. It interfaces to 10 Mbps-only PHY devices such as the Intel 82503. The 10 Mbps serial interface is bit wide. Transmission is performed on the TXD0 pin and reception on RXD0. Serial data is clocked on the rising edge of the clock; TXCLK for transmission and RXCLK for reception. These clocks operate at 10 MHz and are both driven by the PHY.

4.3.3.1 10 Mbps Transmission

When the 82557 has a frame ready for transmission it samples the link for activity. If the CRS signal is inactive (no activity on the link), frame transmission begins. The data is transmitted via TXD0 and is clocked on the rising edge of TXC. The RTS signal is asserted at this time. The CRS signal is expected to be asserted before one slot time has elapsed, however the transmission will complete successfully even if CRS is not asserted (the absence of CRS will be reported in a lost CRS status bit). In the case of a collision, the PHY asserts the COL signal to the 82557 which will then stop transmitting the frame within four clock times and append a JAM sequence onto the link. After the end of a collided transmission the 82557 will back off and attempt to transmit once again when the back off timer expires. Note that the retransmission is done from the data stored internally in the 82557 FIFO block, so no re-access to the data in host memory is performed. In the case of a successful transmission, the 82557 is ready to transmit any other frames queued in its FIFO block within the minimum inter frame spacing (IFS) of the link.

4.3.3.2 10 Mbps Reception

Frame reception starts with the assertion of CRS by the PHY. The 82557 will then start sampling incoming data on RXD0 on the rising edge of RXC. There is a PHY-dependant delay of two or more clock cycles between the assertion of CRS and the first data bit the 82557 samples. The 82557 accepts frames which pass its address filtering mechanism, passing the frame in a byte-wide format to its internal FIFO block. Reception ends when CRS is deasserted by the PHY. The last bit sampled by the 82557 is the bit present on RXD0 on the RXCLK rising edge in which CRS deassertion is detected.

4.3.3.3 10 Mbps Full Duplex Operation

In 10 Mbps-only mode, when the 82557 is placed in Full Duplex mode transmission will begin regardless of the state of CRS or the 82557 receive unit. The 82557 receiver accepts incoming frames regardless of the transmitters operation. The 82557 does not accept the COL input in this mode. Frame delineation is by CRS deassertion.

4.4 MII Management Interface

The MII management interface allows the CPU to have direct control over an MII-compatible PHY device via a control register in the 82557. This allows the driver software to place the PHY in specific modes such as Full Duplex, Loopback, Power Down, etc., without the need for specific hardware pins to select the desired mode. This structure allows the 82557 to query a PHY device for status of the link. This register, called the MDI Control Register, resides at offset 10h in the 82557 CSR. The CPU writes commands to this register and the 82557 reads or writes control/status parameters to the PHY device via a serial, bi-directional data pin called MDIO. These serial data transfers are clocked by the MDC clock output from the 82557.

The *82557 User's Guide* describes the structure of the MDI control register and the MDI read and write cycle bit streams.

4.4.1 MDI CYCLES

The MDI protocol consists of a bit stream that is driven or sampled by the 82557 on each rising edge of the MDC pin. The bit stream consists of the following elements:

<PREAMBLE> <ST> <OP> <PHYAD> <REGAD> <TA>
< DATA> <IDLE>

where:

PREAMBLE At the beginning of each transaction, the 82557 sends a sequence of 32 contiguous logic one bits on the MDIO pin with corresponding cycles on the MDC clock pin for synchronization by the PHY.

ST A Start of Frame pattern of 01.

OP An Operation Code which can assume one of two values:

10 Read

01 Write

PHYAD A 5-bit address of the PHY device which provides support for 32 unique PHY addresses. The 82557 will drive the value written into the PHYAD portion of the MDI register in this field.

REGAD A 5-bit address of the specific register within the PHY device. Provides support for 32 unique registers. The desired register address is specified by the value written to the MDI register.

TA A two-bit turnaround time during which no device actively drives the MDIO signal on a Read cycle. During a Read transaction the PHY should not drive MDIO in the first bit time and drive a 0 in the second bit time. During a Write transaction the 82557 will drive a 10 pattern to fill this time.

DATA 16 bits of data driven by the PHY on Read transactions or by the 82557 on Write transactions. This data is either control or status parameters passed between the 82557 and the PHY.

IDLE The IDLE condition on MDIO is a high impedance state. The MDIO driver is disabled, and the PHY should pull-up the MDIO line to a logic one.

5.0 82557 SOFTWARE INTERFACE

5.1 The Shared Memory Communication Architecture

The 82557 establishes a shared memory communication system with the host CPU. This shared memory is divided into three parts: the Control/Status Registers (CSR), the Command Block List (CBL), and the Receive Frame Area (RFA). The CSR resides on-chip and can be accessed by either I/O or memory cycles, while the rest of the 82557 memory structures reside in system (host) memory. The first 8 bytes of the CSR is called the System Control Block (SCB). The SCB serves as a central communication point for exchanging control and status information between the host CPU and the 82557.

The host software controls the state of the 82557 Command Unit (CU) and Receive Unit (RU) (e.g. Active, Suspended or Idle) by writing commands to the SCB. The 82557 posts the status of the CU and RU in the SCB Status word and indicates status changes with an interrupt. The SCB also holds pointers to a linked list of action commands called the CBL and a linked list of receive resources called the RFA. Figure 19 shows this type of structure.

The CBL consists of a linked list of individual action commands in structures called Command Blocks (CBs). The CBs contain command parameters and status of the action commands. Action commands are categorized as follows:

- Non-Tx commands: This category includes commands such as NOP, Configure, IA Setup, Multicast Setup, Dump and Diagnose.
- Tx command: This includes Transmit Command Blocks (TxCB).

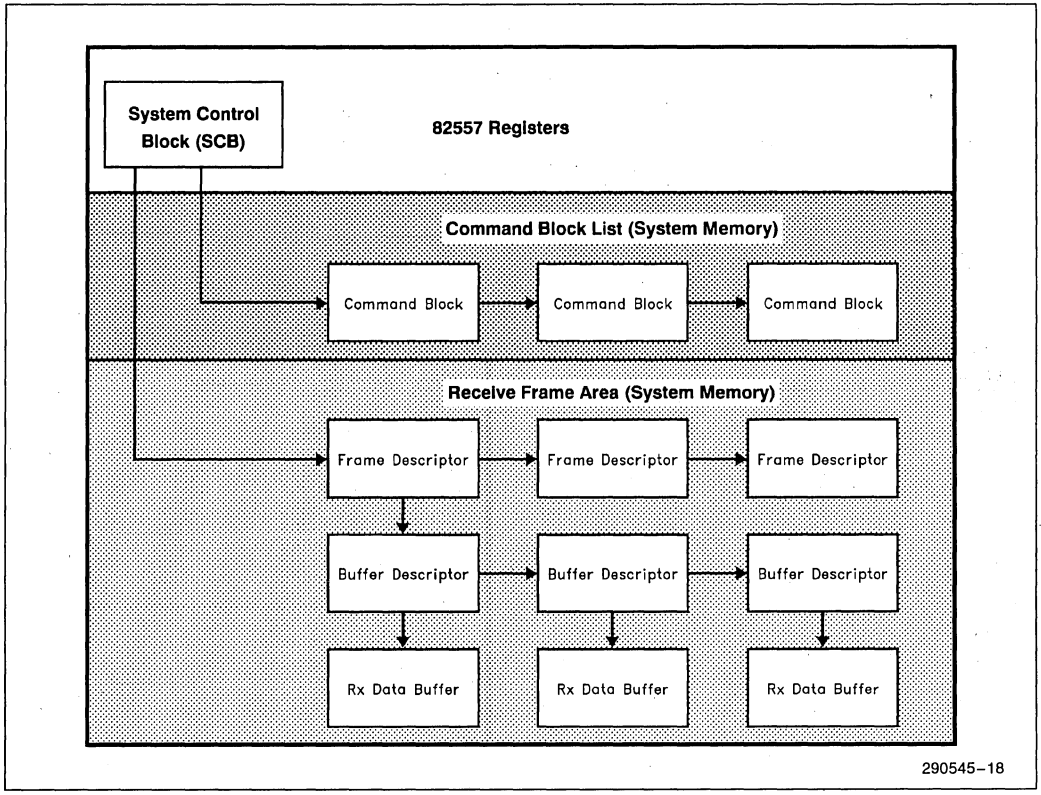


Figure 19. 82557 Shared Memory Structure

Transmit commands can be programmed in Simplified or Flexible memory modes. In the Simplified memory model, the TxCB contains the full transmit frame, immediately following the header information. In the Flexible memory model, each TxCB can be associated with an array of 0 or more Transmit Buffer Descriptors (TBD). Each TBD points to a data buffer fragment. All the data fragments associated with a TxCB (including data in the optional data area of the TxCB) comprise the full transmit frame.

The RFA consists of a list of Receive Frame Descriptors (RFD) and a list of user-prepared or NOS provided buffers. Two memory models are supported. In the Simplified memory model, the data buffer immediately follows the RFD. In the Flexible memory model, each RFD can be associated with a list of zero or more Receive Buffer Descriptors (RBD). Each RBD points to a data buffer fragment. The 82557 RU fills the buffers when it receives frames and updates the status in the RFD (and RBDs if applicable).

The 82557 also provides read/write access to external EEPROM, Flash memory and MDI (Management Data Interface) registers. This is achieved through the EEPROM Control Register, Flash Control Register, and the MDI Control Register respectively. These three registers make up the last eight bytes of the CSR.

Refer to the *82557 User's Guide* for additional information.

5.2 Initializing the 82557

A power-on or software reset prepares the 82557 for normal operation. Because the PCI specification already provides for auto-configuration of many critical parameters such as I/O, memory mapping and interrupt assignment, the 82557 is set to an operational default state after reset. However, the 82557 cannot transmit or receive frames until a Configure command is issued. Refer to the *82557 User's Guide* for additional information. Table 6 lists the different reset options.

Table 6. Summary of Reset Commands

RESET Operation	Effect on 82557
Hardware Reset	Resets all internal registers. A full initialization sequence is needed to make the 82557 operational.
Software Reset* (issued as PORT RESET** command)	Resets all internal registers. A full initialization sequence is needed to make the 82557 operational.
Selective Reset (issued as PORT SELECTIVE RESET** command)	Maintains configuration information. All other setup information is lost.
Self Test (issued as a PORT SELF TEST** Command) or PORT DUMP Command	Resets all internal registers. A Selective Reset is issued internally before the command is executed. A Software Reset is issued internally after the command is completed. A full initialization sequence is needed to make the 82557 operational.

NOTES:
* Software reset will be used throughout this manual to indicate a complete reset using the PORT reset command.
** PORT commands are discussed in detail in the *82557 User's Guide*.

5.3 Controlling the 82557

The CPU issues control commands to the Command Unit (CU) and Receive Unit (RU) through the SCB, which is part of the CSR (described below). The CPU instructs the 82557 to Activate, Suspend, Resume or Idle the CU or RU by placing the appropriate control command in the CU or RU control field. A CPU write access to the SCB causes the 82557 to read the SCB, including the Status word, Command word, CU and RU Control fields, and the SCB General Pointer. Activating the CU causes the 82557 to begin executing the CBL. When execution is completed the 82557 updates the SCB with the CU status then interrupts the CPU, if configured to do so. Activating the RU causes the 82557 to access the RFA and go into the READY state for frame reception. When a frame is received the RU updates the SCB with the RU status and interrupts the CPU. It also automatically advances to the next free RFD in the RFA. This interaction between the CPU and 82557 can continue until a software reset is issued to the 82557, at which point the initialization process must be executed again. The CPU can also perform certain 82557 functions directly through a CPU PORT interface.

5.3.1 THE 82557 CONTROL/STATUS REGISTER (CSR)

The 82557 has seven Control/Status registers which make up the CSR space. These are the SCB Command word, SCB Status word, SCB General Pointer, PORT interface, EEPROM Control register, Flash Control register, and MDI Control register. The CSR space is five DWORDs in length and is shown in Figure 20. The 82557 CSR can be accessed as either an I/O mapped or memory mapped PCI slave.

31 Upper Word 16	15 Lower Word 0	Offset
SCB Command Word	SCB Status Word	Base + 0h
SCB General Pointer		Base + 4h
PORT		Base + 8h
EEPROM Control Register	Flash Control Register	Base + Ch
MDI Control Register		Base + 10h

Figure 20. Control/Status Register

SCB Command Word: The CPU places commands for the CU and RU and acknowledges interrupts in this register.

SCB Status Word: The 82557 places the status of its CU and RU and interrupt indications in this register, for the CPU to read.

SCB General Pointer: This points to various data structures in main memory depending on the current SCB Command word.

PORT Interface: This special interface allows the CPU to reset the 82557, force the 82557 to dump information to main memory, or perform an internal Self-Test.

EEPROM Control Register: This register allows the CPU to read and write to an external EEPROM.

Flash Control Register: This register allows the CPU to enable writes to an external Flash.

MDI Control Register: This register allows the CPU to read and write information from Physical Layer components via the Management Data Interface.

5.3.1.1 Statistical Counters

The 82557 provides information for network management statistics by providing on-chip statistical counters that count a variety of events associated with both transmit and receive. The counters are updated by the 82557 when it completes the processing of a frame, i.e., when it has completed transmitting a frame on the link or when it completed receiving a frame. The Statistical Counters are reported to the software on demand by issuing the *Dump Statistical Counters* command in the SCB CUC field.

Table 7. Error Counters

Counter	Description
Transmit Good Frames	This counter contains the number of frames that were transmitted properly on the link. It is updated only after the actual transmission on the link is completed, and not when the frame was read from memory as is done for the TxCB status.
Transmit Maximum Collisions (Maxcol) Errors	This counter contains the number of frames that were not transmitted since they encountered the configured maximum number of collisions.
Transmit Late Collisions (Latecol) Errors	This counter contains the number of frames that were not transmitted since they encountered a collision later than the configured slot time.
Transmit Underrun Errors	A DMA underrun occured because the system bus did not keep up with the transmission. This counter contains the number of frames that were either not transmitted or retransmitted due to a TxDMA underrun. If the 82557 is configured to retransmit on underrun, this counter may be updated multiple times for a single frame.
Transmit Lost Carrier Sense (CRS)	Transmission was not successful due to lost Carrier Sense. This counter contains the number of frames that were transmitted by the 82557 despite the fact that it detected the deassertion of CRS during the transmission.
Transmit Deferred	During the transmission attempt the 82557 had to defer to traffic on the link. This counter contains the number of frames that were deferred before transmission due to activity on the link.

Table 7. Error Counters (Continued)

Counter	Description
Transmit Single Collisions	This counter contains the number of transmitted frames that encountered one collision.
Transmit Multiple Collisions	This counter contains the number of transmitted frames that encountered more than one collision.
Transmit Total Collisions	This counter contains the total number of collisions that were encountered while attempting to transmit. This count includes late collisions and frames that encountered MAXCOL.
Receive Good Frames	This counter contains the number of frames that were received properly from the link. It is updated only after the actual reception from the link is completed, and all the data bytes are stored in memory.
Receive CRC Errors	This counter contains the number of aligned frames discarded because of a CRC error. This counter is updated, if needed, regardless of the RU state. If the RX__ER pin is asserted during a receive frame, the CRCERRS counter will increment (only once per receive frame). The CRCERRS counter is mutually exclusive to the ALNERRS and SHRTFRM counters.
Receive Alignment Errors	This counter contains the number of frames that are both misaligned (i.e., where CRS deasserts on a nonoctal boundary) and contain a CRC error. The counter is updated, if needed, regardless of the RU state. The ALNERRS counter is mutually exclusive to the CRCERRS and SHRTFRM counters.
Receive Resource Errors	This counter contains the number of good frames discarded because there were no resources available. Frames intended for a host whose RU is in the No Resources state fall into this category. If the 82557 is configured to Save Bad Frames and the status of the received frame indicates that it is a bad frame, the RSCERRS counter is not updated.
Receive Overrun Errors	This counter contains the number of frames known to be lost because the local system bus was not available. If the traffic problem persists for more than one frame, the frames that follow the first are also lost; however, because there is no lost frame indicator, they are not counted.
Receive Collision Detect (CDT) Errors	This counter contains the number of frames that encountered collisions during frame reception.
Receive Short Frame Errors	This counter contains the number of received frames that are shorter than the minimum frame length. The SHRTFRM counter is mutually exclusive to the ALNERRS and CRCERRS counters and has a higher priority (i.e., a short frame will always increment only the SHRTFRM counter).

The Statistical Counters are initially set to zero by the 82557 after reset. They cannot be preset to anything other than zero. The 82557 increments the counters by internally reading them, incrementing them and writing them back. This process is invisible to the CPU and PCI bus. Refer to the *82557 User's Guide* for additional information.

6.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

6.1 Absolute Maximum Ratings

Case Temperature under Bias .....0°C to +85°C
Storage Temperature .....−65°C to +140°C
All Output and Supply Voltages .....−0.5V to +7V
All Input Voltages.....−1.0V to 6.0V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

More information on the quality and reliability of the 82557, refer to the *Components Quality and Reliability Handbook,* order number 210997.

6.2 DC Specifications

Table 8. General DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage		4.75		5.25	V	
I_{CC}	Power Supply			300		mA	

Table 9. PCI Interface DC Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V	
V_{IL}	Input Low Voltage		−0.5	0.8	V	
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	μA	1
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		−70	μA	1
V_{OH}	Output High Voltage	I_{OUT} = −2 mA	2.4		V	
V_{OL}	Output Low Voltage	I_{OUT} = 3 mA, 6 mA		0.55	V	2
C_{IN}	Input Pin Capacitance			10	pF	3
C_{CLK}	CLK Pin Capacitance		5	12	pF	3
C_{IDSEL}	IDSEL Pin Capacitance			8	pF	3
L_{PIN}	Pin Inductance			20	nH	3

NOTES:
1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. Signals without pullup resistors have 3 mA low output current. Signals requiring pull up have 6 mA; the latter include, **FRAME**, **TRDY**, **IRDY**, **DEVSEL**, **STOP**, **SERR** and **PERR**.
3. Characterized, not tested.

Table 10. MII and 10 Mbps PHY Interface DC Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V	
V_{IL}	Input Low Voltage		−0.5	0.8	V	
I_{IL}	Input Low Leakage Current	$0 < V_{IN} < V_{CC}$		±20	μA	
V_{OH}	Output High Voltage	I_{OUT} = −4 mA	2.4		V	
V_{OL}	Output Low Voltage	I_{OUT} = 4 mA		0.4	V	3
C_{IN}	Input Pin Capacitance			8	pF	1

NOTES:
1. Characterized, not tested.
2. To drive an MII cable (Z_o = 68Ω ±15%, Length = 0.5m) a 40Ω ±10% resistor should be connected in series to each MII output.
3. For pins LPBCK and RSTOUT I_{OL} = 1 mA.

Table 11. FLASH/EEPROM Interface DC Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V	
V_{IL}	Input Low Voltage		−0.5	0.8	V	
I_{IL}	Input Low Leakage Current	$0 < V_{IN} < V_{CC}$		±20	μA	
V_{OH}	Output High Voltage	I_{OUT} = −1 mA	2.4		V	
V_{OL}	Output Low Voltage	I_{OUT} = 1 mA		0.4	V	
C_{IN}	Input Pin Capacitance			10	pF	1

NOTE:
1. Characterized, not tested.

6.3 AC Specifications

6.3.1 PCI Interface

Table 12. AC Specifications for PCI Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$	-44		mA	1, 2
		$1.4 < V_{OUT} < 2.4$	$-44 + (V_{OUT} - 1.4)/0.024$	Eqt'n A	mA	1, 2
	(Test Point)	$V_{OUT} = 3.1$		-142	mA	1, 2
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$	95		mA	2
		$2.2 > V_{OUT} > 0.55$	$V_{OUT}/0.023$	Eqt'n B	mA	2
	(Test Point)	$V_{OUT} = 0.71$		206	mA	2
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA	2
t_r	Unloaded Output Rise Time	0.4V to 2.4V	1	5	V/ns	1, 2
t_f	Unloaded Output Fall Time	2.4V to 0.4V	1	5	V/ns	2

NOTES:
1. Not relevant to **SERR** or **INTA** which are open drain outputs.
2. Characterized, not tested.

6.4 Timing Specification

6.4.1 CLOCK SPECIFICATIONS

6.4.1.1 PCI Interface Clock

The 82557 uses the PCI clock. Figure 21 shows the clock waveform and required measurement points for the PCI clock signal. Table 13 summarizes the PCI clock specifications. This clock waveform should be treated as minimum requirement of the 82557.

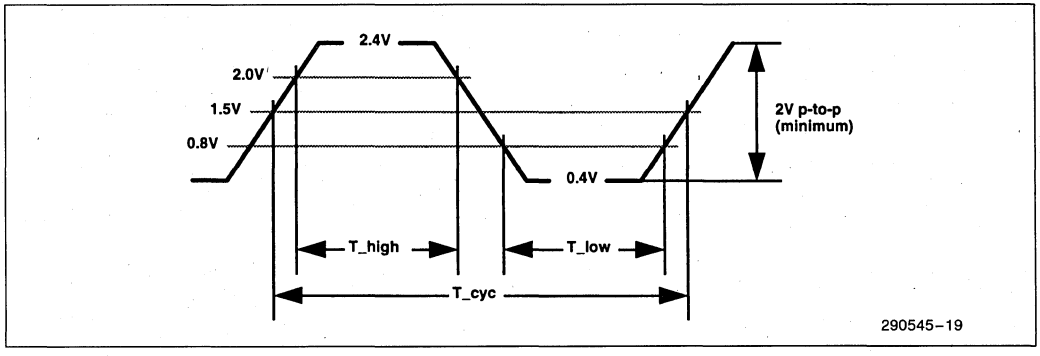


Figure 21. Clock Waveform

Table 13. PCI Clock Specifications

	Symbol	Parameter	Min	Max	Units	Notes
T1	t_{CYC}	CLK Cycle Time	30		ns	1
T2	t_{HIGH}	CLK High Time	11		ns	
T3	t_{LOW}	CLK Low Time	11		ns	
T4	—	CLK Slew Rate	1	4	V/ns	2

NOTES:
1. The 82557 will work with any PCI clock frequency up to 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate should be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 21.

6.4.1.2 MII Interface Clock

The 82557 uses two clocks on the MII interface: transmit clock (TXCLK) and receive clock (RXCLK). Table 14 shows timings for each clock.

Table 14. MII Clock Specifications

	Symbol	Parameter	Min	Typ	Max	Units	Notes
T5	t_{CYC100}	TXCLK/RXCLK Cycle Time @ 100 Mbps Operation		40		ns	1, 2, 3
T6	t_{CYC10}	TXCLK/RXCLK Cycle Time @ 10 Mbps Operation		400		ns	1, 2, 3
T7	DC	TXCLK/RXCLK Duty Cycle	35		65	%	1, 2, 3

NOTES:
1. Either high or low times of **RXCLK** may be extended at the event of switching it from recovered clock to **TXCLK**, or vice versa.
2. No specific phase relationship is assumed between **TXCLK** and **RXCLK**.
3. When RXDV is active, the frequency difference between TXCLK and RXCLK should not exceed ±200 ppm.

6.4.1.3 10 Mbps Serial Interface Clock

The 82557 uses two clocks on the serial interface: transmit clock TXCLK and receive clock RXCLK. Table 15 shows timings for both clocks.

Table 15. Serial interface Clock Specifications

	Symbol	Parameter	Min	Typ	Max	Units	Notes
T8	$t_{cycTXCLK}$	TXCLK Cycle Time	99.99		100.01	ns	
T9	$t_{hi\_loTXCLK}$	TXCLK Duty Cycle	35	50	65	%	
T10	t_{r_fTXCLK}	TXCLK Rise/Fall Time			5	ns	
T11	$t_{cycRXCLK}$	RXCLK Cycle Time		100		ns	
T12	$t_{hi\_loRXCLK}$	RXCLK Duty Cycle	35		65	%	
T13	t_{r_fRXCLK}	RXCLK Rise/Fall Time			5	ns	

NOTE:
1. No specific phase relationship is assumed between **TXCLK** and **RXCLK.**

6.4.2 TIMING PARAMETERS

6.4.2.1 PCI Timings

Table 16 provides the timing parameters of the 82557 for its PCI interface.

Table 16. PCI Timing Parameters

	Symbol	Parameter	Min	Max	Units	Notes
T14	t_{val}	CLK to Signal Valid Delay: Bussed Signals	2	11	ns	1, 2, 3
T15	$t_{val(ptp)}$	CLK to Signal Valid Delay: Point to Point	2	12	ns	1, 2, 3
T16	t_{ON}	Float to Active Delay	2		ns	1
T17	t_{OFF}	Active to Float Delay		28	ns	1
T18	t_{su}	Input Set Up Time to CLK: Bussed Signals	7		ns	3, 4
T19	$t_{su(ptp)}$	Input Set Up Time to CLK: Point to Point	10		ns	3, 4
T20	t_{H}	Input Hold Time from CLK	0		ns	4
T22	$t_{rst-clk}$	Reset Active Time after CLK Stable	100		µs	5
T23	$t_{rst-off}$	Reset Active to Output Float Delay		40	ns	5, 6

NOTES:
1. See timing measurement conditions diagram in this section.
2. Minimum times are specified with 0 pF equivalent load; maximum times are specified with 50 pF equivalent load. Actual test capacitance may vary, but results are correlated to these specifications.
3. **$\overline{\text{REQ}}$** and **$\overline{\text{GNT}}$** are point-to-point signals, and have different output valid delay and input setup times than do bussed signals. All other signals are bussed.
4. See timing measurement conditions in this section.
5. **$\overline{\text{RST}}$** is asserted and deasserted asynchronously with respect to **CLK**.
6. All PCI I/F output drivers are floated when **$\overline{\text{RST}}$** is active.

6.4.2.2 MII and 10 Mbps Interface Timings

Table 17 provides the timing parameters for MII and serial interface signals.

Table 17. MII and Serial Interface Timing Parameters

	Symbol	Parameter	Min	Max	Units	Notes
T24	t_{valTX}	TX Synchronous Signals Valid Time	0	15	ns	1, 3
T25	t_{suRX}	RX Synchronous Signals Setup Time	10		ns	2, 3
T26	t_{hRX}	RX Synchronous Signals Hold Time	10		ns	2, 3
T27	$t_{hiloMDC}$	MDC High/Low Time	200		ns	5, 7
			310		ns	5, 8
T28	t_{valMD}	MDC to MDIO Valid Delay	50	440	ns	6, 7
			50	580	ns	6, 8
T29	T_{suMDIO}	MDIO Setup Time	120		ns	6, 7
			120		ns	6, 8
T30	t_{hMDIO}	MDIO Hold Time	0		ns	6

NOTES:
1. TX Synchronous Signals are: **TXD0–3** and **TXEN** (**RTS** in serial interface).
2. RX Synchronous Signals are: **RXD0–3, RXDV** and **RXER.**
3. The timing reference is the rising edge of **TXCLK,** for transmit, or **RXCLK,** for receive.
4. To drive an MII cable (Z_o = 68Ω ±15%, Length = 0.5m) a 40Ω ±10% resistor should be connected in series with each MII output (**TXD0–3, TXEN, MDC** and **MDIO**).
5. **MDC** is an aperiodic signal.
6. Referenced to rising edge of **MDC.**
7. These timings apply when the **PCI** clock rate is 33 MHz. As the **PCI** clock rate references the **MDC/MDIO** I/F these timings scale accordingly.
8. These timings apply when the **PCI** clock rate is 25 MHz. As the PCI clock rate references the **MDC/MDIO** I/F these timings scale accordingly.
9. The **MDC/MDIO** timings are specified as measured at the **82557,** and as required or supplied by the **82557.**
10. **CRS** and **COL** (**CLD** in serial interface) are asynchronous with regard to either **RXCLK** or **TXCLK.**

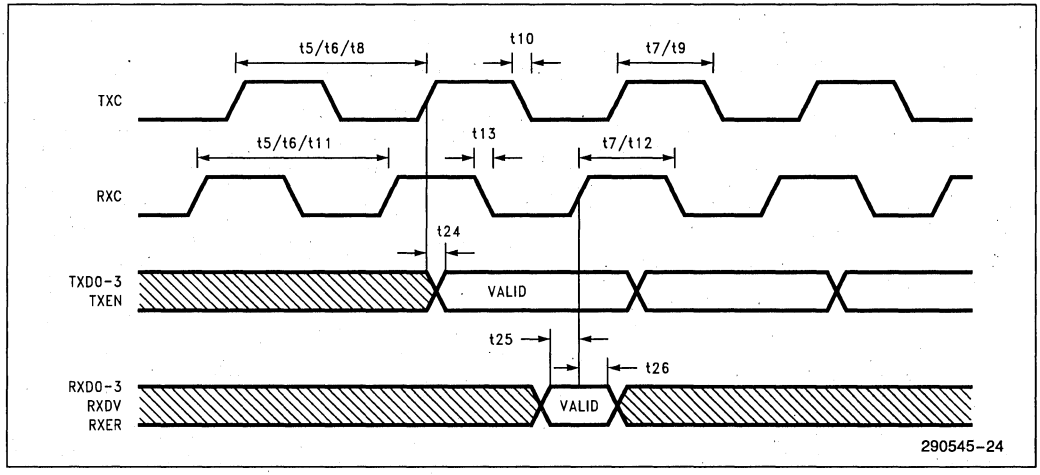


Figure 22. Transmit Timings

6.4.2.3 Collision Parameters

Symbol	Parameter	Typ	Units
T_{COL}	Collision Active to Jam Start	4	TXCLK Periods

6.4.2.4 FLASH Interface Timings

- The 82557 is designed to support FLASH of up to 150 ns access time.
- The V_{PP} signal in FLASH implementation should be connected permanently to 12V. Thus, writing to the FLASH is controlled only by the **WE**ρ signal.

Table 18 provides the timing parameters for FLASH interface signals. The timing parameters are illustrated in Figures 23 and 24.

Table 18. FLASH Interface Timing Parameters

	Symbol	Parameter	Min	Max	Units	Notes
T31	t_{flrwc}	Read/Write Cycle Time	150		ns	1, flash t_{AVAV} = 150 ns
T32	t_{flacc}	FLADDR to Read FLD Setup Time	150		ns	1, flash t_{AVQV} = 150 ns
T33	t_{flce}	$\overline{FLCS}$ to Read FLD Setup Time	150		ns	1, flash t_{ELQV} = 150 ns
T34	t_{floe}	$\overline{FLOE}$ Active to Read FLD Setup Time	120		ns	1, flash t_{GLQV} = 55 ns
T35	t_{fldf}	$\overline{FLOE}$ Inactive to FLD Driven Delay Time		50	ns	1, flash t_{GHQZ} = 35 ns
T36	t_{flas}	$\overline{FLWE}$ Active Delay after FLADDR Stable	5		ns	2, flash t_{AVWL} = 0 ns
T37	t_{flah}	FLADDR Stable after $\overline{FLWE}$ Active	100		ns	2, flash t_{WLAX} = 60 ns
T38	t_{flcs}	$\overline{FLWE}$ Active Delay after $\overline{FLCS}$ Active	20		ns	2, flash t_{ELWL} = 20 ns
T39	t_{flch}	$\overline{FLCS}$ Inactive Delay after $\overline{FLWE}$ Inactive	0		ns	2, flash t_{WHEH} = 0 ns
T40	t_{flds}	$\overline{FLWE}$ Inactive Delay after FLD Stable		50	ns	2, flash t_{DVWH} = 50 ns
T41	t_{fldh}	FLD Delay after $\overline{FLWE}$ Inactive	10		ns	2, flash t_{WHDX} = 10 ns
T42	t_{flwp}	Write Pulse Width	120		ns	2, flash t_{WLWH} = 60 ns
T43	t_{flwph}	Write Pulse Width High	25		ns	2, flash t_{WHWL} = 20 ns
T44	t_{lasu}	FLADDR Setup Time before $\overline{FLCS}$	4		ns	3, latch t_{SU} = 2 ns
T45	t_{lah}	FLADDR Hold Time after $\overline{FLCS}$	4		ns	3, latch t_H = 1.5 ns

NOTES:
1. These timing specifications apply to FLASH read cycles. The flash timings referenced are 28F020-150 timings.
2. These timing specifications apply to FLASH write cycles. The flash timings referenced are 28F020-150 timings.
3. These timing specifications apply to all FLASH cycles. The latch timings referenced are '373 timings.

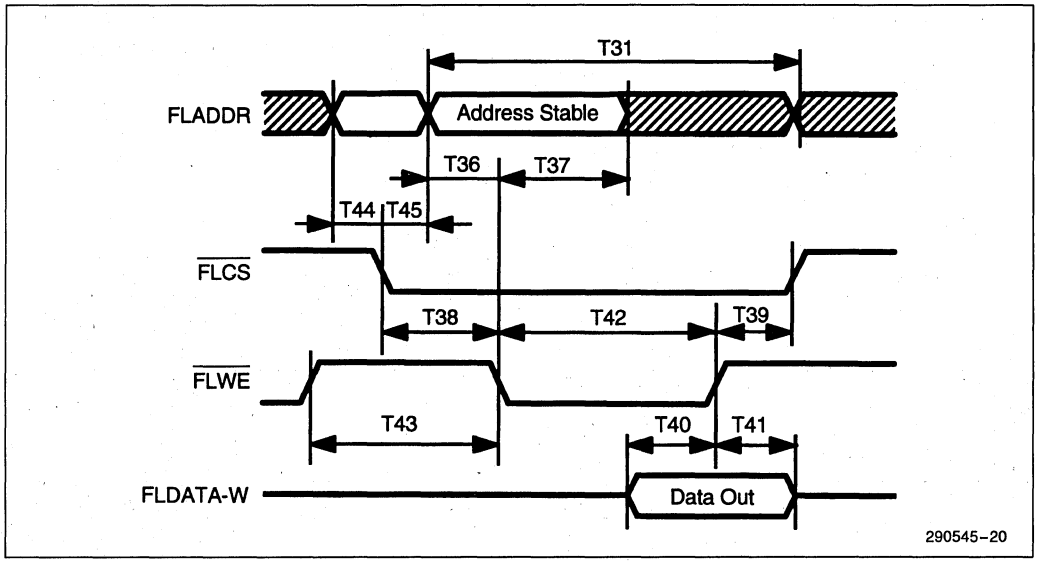


Figure 23. FLASH Timings: Write Cycle

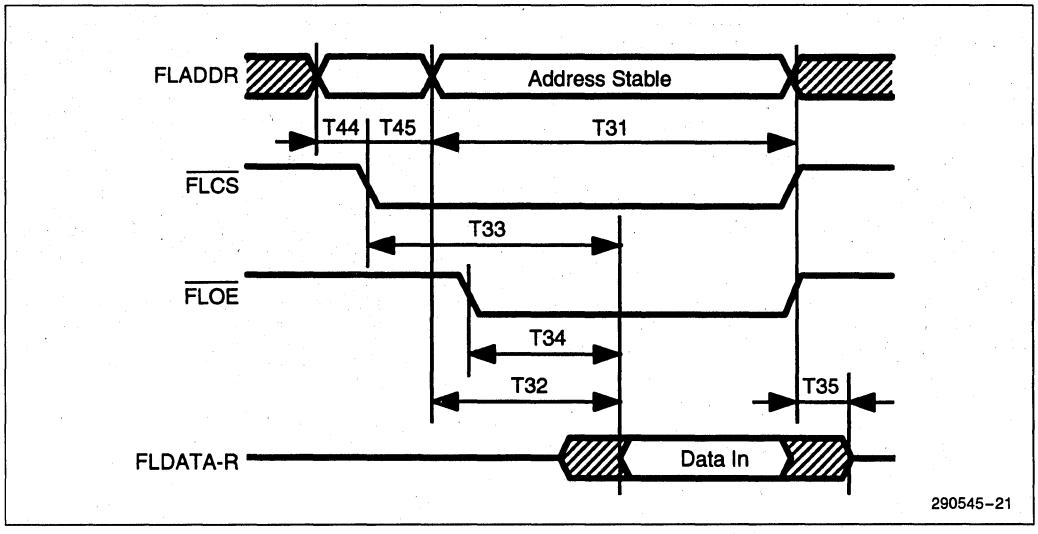


Figure 24. FLASH Timings: Read Cycle

7.0 PHYSICAL ATTRIBUTES and DIMENSIONS

This section provides the physical packaging information for the 82557. The 82557 is a 160-lead plastic quad flatpack (PQFP) device. Package attributes are provided in Table 19 and dimensions are shown in Figures 25 and 26. Table 20 shows the dimensions for the figures. For more information on Intel device package, refer to the *Intel Packaging Handbook,* available from Intel Literature or your local sales office.

Table 19. Intel 82557 Package Attributes

Attribute	Value
Lead Count	160
Square or Rectangle?	Square
Pitch (mm)	0.65
Package Thickness (mm)	3.65
Shipping Media	Trays
Desiccant Pack	Yes
Comments	Gull wing lead configuration, non-bumpered

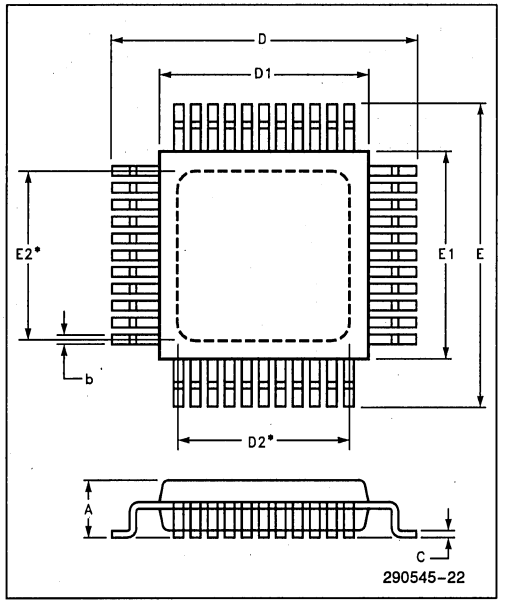


Figure 25. Dimensions Diagram for Table 20

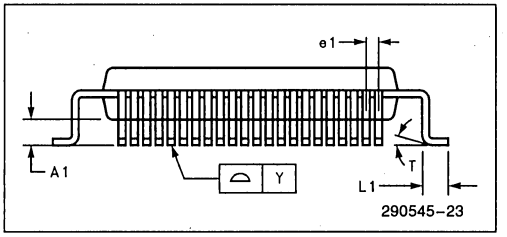


Figure 26. Terminal Dimensions for Table 20

Table 20. Quad Flatpack Dimensions in Figures 25 and 26

Symbol	Description	Min	Max
A	Overall Height	3.25	3.75
A1	Standoff	0	0.30
b	Lead Width	0.20	0.40
c	Lead Thickness	0.150	0.188
D	Terminal Dimension	30.2	31.0
D1	Package Body	27.9	28.1
E	Terminal Dimension	30.2	31.0
E1	Package Body	27.9	28.1
e1	Lead Pitch	0.55	0.75
L1	Foot Length	0.60	1.0
T	Lead Angle	0°	10°
Y	Coplanarity	0.1	

NOTE:
Dimensions are in millimeters.

1

82595FX
ISA BUS HIGH INTEGRATION ETHERNET CONTROLLER

- **Optimal Integration for Lowest Cost Solution**
  - Glueless 8-Bit/16-Bit ISA Bus Interface
  - Provides Fully 802.3 Compliant AUI and TPE Serial Interface
  - Local SRAM Support up to 64 Kbytes
  - Integrated ISA Bus Data Transceivers
  - FLASH/EPROM Boot Support up to 1 Mbyte for Diskless Workstations
  - Hardware and Software Portable between Motherboard and Adapter Card Solutions
- **High Performance Networking Functions**
  - Advanced Concurrent Processing of Receive and Transmit Functions
  - 16-Bit/32-Bit IO Accesses to Local SRAM with Zero Added Wait-States
  - Ring Buffer Structure for Continuous Frame Reception and Transmit Chaining
  - Automatic Retransmission on Collision
  - Automatically Corrects TPE Polarity Switching Problems
  - Auto Negotiation/Manual Full Duplex Support
- **Low Power CHMOS IV Technology**
- **Ease of Use**
  - Auto-Negotiation of Full Duplex Functionality
  - Fully Compatible with ISA Plug and Play Specification
  - EEPROM Interface to Support Jumperless Designs
  - Software Structures Optimized to Reduce Processing Steps
  - Automatically Maps into Unused PC IO Locations to Help Eliminate LAN Setup Problems
  - All Software Structures Contained in One 16-Byte IO Space
  - JTAG Port for Reduced Board Testing Times
  - Automatic or Manual Switching between TPE and AUI Ports
  - Supports Eight IRQs
- **Power Management**
  - Advanced Power Management Support by Power Down and Sleep Mode
  - Both SL Compatible SMOUT Input and Non-SL Software Parameter for Power Down Mode
- **160-Lead QFP Package Provides Smallest Available Form Factor**
- **100% Backwards Software Compatible to 82595TX**

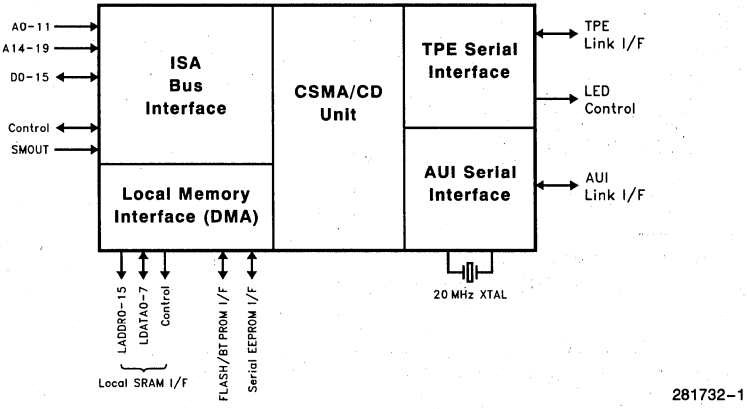


Figure 1. 82595FX Block Diagram

September 1995
Order Number: 281732-001

82595FX
ISA Bus High Integration ETHERNET Controller

CONTENTS

CONTENTS

CONTENTS

CONTENTS

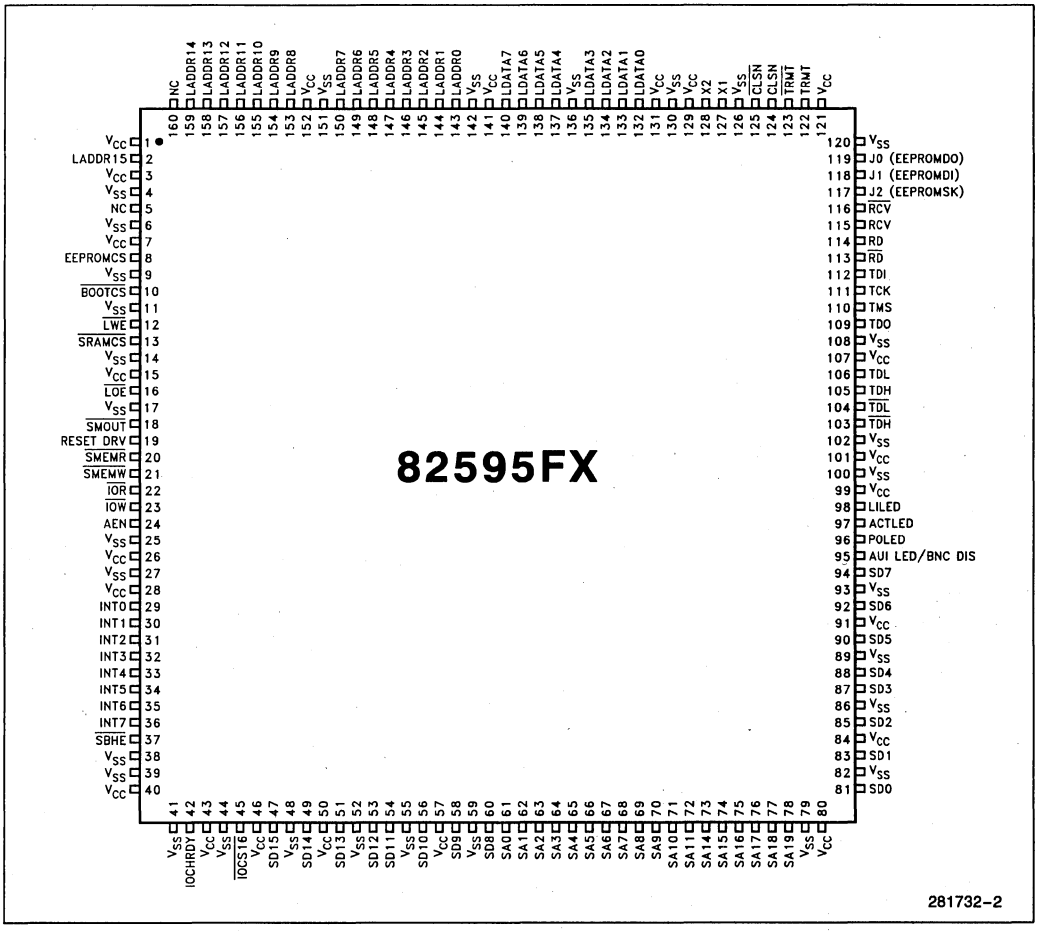


Figure 2. 82595FX Pinout

1.0 INTRODUCTION

1.1 82595FX Overview

The 82595FX is a highly integrated, high performance LAN controller which provides a cost effective LAN solution for ISA compatible Personal Computer (PC) motherboards (both desktop and portable), and add-on ISA adapter boards. The 82595FX integrates all of the major functions of a buffered LAN solution into one chip with the exception of the local buffer memory, which is implemented by adding one SRAM component to the LAN solution. The 82595FX's Concurrent Processing feature significantly enhances throughput performance. Both system bus and serial link activities occur concurrently, allowing the 82595FX to maximize network bandwidth by minimizing delays associated with transmit or receiving frames. The 82595FX's bus interface is a glueless attachment to an ISA bus. Its serial interface provides a Twisted Pair Ethernet (TPE) and an Attachment Unit Interface (AUI) connection. By integrating the majority of the LAN solution functions into one cost effective component, production cost saving can be achieved as well as significantly decreasing the design time for a solution. This level of integration also allows an 82595FX solution to be ported between different applications (PC motherboards, and adapters, while maintaining a compatible hardware and software base.

The 82595FX's software interface is optimized to reduce the number of processing steps that are required to interface to the 82595FX solution. The 82595FX's initialization and control registers are directly addressable within one 16-byte IO address block. The 82595FX can automatically resolve any conflicts to an IO block by moving its IO offset to an unused location in the case that a conflict occurs. The 82595FX's local memory is arranged in a simple ring buffer structure for efficient transfer of transmit and receive packets. The local memory, up to 64 Kbytes of SRAM, resides as either a 16-bit or 32-bit IO port in the host systems IO map programmable through configuration. The 82595FX provides direct control over the local SRAM. The 82595FX performs a prefetch to the SRAM memory allowing CPU IO cycles to this data with no added wait-states. The 82595FX also provides an interface to up to 1 Mbyte of FLASH or EPROM memory. An interface to an EEPROM, which holds solution configuration values and can also contain the Node ID, allows for the implementation of a "jumperless" design. In addition, the 82595FX contains full hardware support for the implementation of the ISA Plug N' Play specification. Plug N' Play eliminates jumpers and complicated setup utilities by allowing peripheral functions to be added to a PC automatically (such as adapter cards) without the need to individually configure each parameter (e.g. Interrupt, IO Address, etc). This allows for configuration ease-of-use, which results in minimal time associated with installation.

The 82595FX's packaging and power management features are designed to consume minimal board real estate and system power. This is required for applications such as portable PC motherboard designs which require a solution with very low real estate and power consumption. The 82595FX package is a 160-lead PQFP (Plastic Quad Flat Pack). Its dimensions are 28 mm by 28 mm, and 3.5 mm in height. The 82595FX contains two power down modes; an SL compatible power down mode which utilizes the SL SMOUT input, and a POWER DOWN command for non-SL systems.

1.2 Power Management

Power management and low power consumption are two items that will allow any design using the 82595FX to be suitable for green PC use. Low power operation is initiated when software issues a SLEEP command to the device. After a short wait, it will shut off the system clock, some parts of the Backoff Randomizer, several input buffers and the two LED drivers. The 82595FX will subsequently wake up from sleep mode when software initiates an ISA cycle in the application, as well as when it receives a frame addressed to it. The total power consumption when in sleep mode can be as low as approximately 175 mW. Normal idle power consumption is 300 mW.

The software POWER DOWN command, along with its companion hardware implementation—the SMOUT I/O pin, provide additional power management capabilities. This feature allows the 82595FX to be powered down, and then at some time in the future be selectively reset without having lost the current configuration. See the 82595FX User's Guide for further details on these features.

1.3 Auto-Negotiation

Auto-negotiation functionality is a method of automatically determining the highest common operating mode (i.e., 10BaseT half duplex, 10BaseT full duplex, etc.) between two network devices. Using this functionality, two stations, each having a varying number of different operating modes, negotiate the highest possible common operating mode between them. During the power up sequence, the auto-negotiation functionality will automatically establish a link with which it can take advantage of any auto-negotiation-capable device it is connected to. An auto-negotiation capable hub can detect and automatically configure its ports to take maximum advantage of

common modes of operation without any user intervention or prior knowledge by connected stations. See the 82595FX User's Guide for details on this function.

For further information on these enhancements and a description of all the differences between the 82595TX and 82595FX, please consult the 82595FX User's Manual, available through your local sales representative.

1.4 Compliance to Industry Standards

The 82595FX has two interfaces; the host system interface, which is an ISA bus interface, and the serial, or network interface. This interface has been standardized by the IEEE.

1.4.1 BUS INTERFACE—ISA IEEE P996

The 82595FX implements the full ISA bus interface. It is compatible with the IEEE spec P996.

1.4.2 ETHERNET/TWISTED PAIR ETHERNET INTERFACE—IEEE 802.3 SPECIFICATION

The 82595FX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop, providing a fully compliant IEEE 802.3 AUI interface. The TPE port provides a fully compliant IEEE 10BASE-T interface. The 82595FX can automatically switch to whichever port (TPE or AUI) is active.

2.0 82595FX PIN DEFINITIONS

2.1 ISA Bus Interface

Symbol	Pin No.	Type	Name and Function
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11	61 62 63 64 65 66 67 68 69 70 71 72	I	**ADDRESS BUS:** These pins provide address decoding for up to 1 Kbyte of address. These pins also provide 4 Kbytes of IO addressing to support the Plug N' Play Standard.
SA14 SA15 SA16 SA17 SA18 SA19	73 74 75 76 77 78	I	**ADDRESS BUS:** These pins provide address decoding between the 16 Kbyte and 1 Mbyte memory space. This allows for decoding of a Boot EPROM or a FLASH in 16K increments.

2.1 ISA Bus Interface (Continued)

Symbol	Pin No.	Type	Name and Function
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15	81 83 85 87 88 90 92 94 60 58 56 54 53 51 49 47	I/O	**DATA BUS:** This is the data interface between the 82595FX and the host system. This data is buffered by one (8-bit design) or two (16-bit design) internal transceivers.
AEN	24	I	**ADDRESS ENABLE:** Active high signal indicates a DMA cycle is active.
$\overline{\text{SMEMR}}$	20	I	**MEMORY READ** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{SMEMW}}$	21	I	**MEMORY WRITE** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{IOR}}$	22	I	**IO READ:** Active low.
$\overline{\text{IOW}}$	23	I	**IO WRITE:** Active low.
$\overline{\text{IOCS16}}$	45	O	**IO CHIP SELECT 16:** Active low, open drain output which indicates that an IO cycle access to the 82595FX solution is 16-bit wide. Driven for IO cycles to the local memory or to the 82595FX.
IOCHRDY	42	O	**IO CHANNEL READY:** Active high, open drain output. When driven low, it extends host cycles to the 82595FX solution.
$\overline{\text{SBHE}}$	37	I	**SYSTEM BUS HIGH ENABLE:** Active low input indicates a data transfer on the high-byte (D8–D15) of the system bus (a 16-bit transfer). This pin also determines if the 82595FX is operating in an 8- or 16-bit system upon initialization.
INT0 INT1 INT2 INT3 INT4 INT5 INT6 INT7	29 30 31 32 33 34 35 36	O	**82595FX INTERRUPT 0–7:** One of these 8 pins is selected to be active one at a time (the other seven are in Hi-Z state) by configuration. These active high outputs serve as interrupts to the host system.
RESET DRV	19	I	**RESET DRIVE:** Active high reset signal.

2.2 Local Memory Interface

Symbol	Pin No.	Type	Name and Function
LADDR0 LADDR1 LADDR2 LADDR3 LADDR4 LADDR5 LADDR6 LADDR7 LADDR8 LADDR9 LADDR10 LADDR11 LADDR12 LADDR13 LADDR14 LADDR15	143 144 145 146 147 148 149 150 153 154 155 156 157 158 159 2	O	**LOCAL MEMORY ADDRESS (LADDR0–LADDR15):** These outputs contain the multiplexed address for the local SRAM. **FLASH ADDRESS 14–17 (LADDR0–LADDR5):** These pins control the FLASH addressing from 16K to 1M to allow paging of the FLASH in 16K spaces. These addresses are under direct control of the FLASH PAGING configuration register.
LDATA0 LDATA1 LDATA2 LDATA3 LDATA4 LDATA5 LDATA6 LDATA7	132 133 134 135 137 138 139 140	I/O	**LOCAL MEMORY DATA BUS (LDATA0–LDATA7):** The eight I/O signals, comprising the local data bus, are used to read or write data to or from the 8-bit wide SRAM. **FLASH MEMORY DATA BUS (LDATA0–LDATA7):** These signals also provide eight bits of data for accesses to an 8-bit FLASH/EPROM if these components are used.
$\overline{\text{SRAMCS}}$	13	O	**SRAM CHIP SELECT:** This active low output is the chip select to the SRAM.
$\overline{\text{LWE}}$	12	O	This active low output is the **Write Enable** to the SRAM. This pin also provides the active low **Write Enable** to the **FLASH.**
$\overline{\text{LOE}}$	16	O	This active low output is the **Output Enable** to the SRAM. This pin also provides the active low **Output Enable** control to the **FLASH.**
$\overline{\text{BOOTCS}}$	10	O	**BOOT EPROM/FLASH CHIP SELECT:** Active low output.
EEPROMCS	8	I/O	**EEPROM CS:** Active high signal. If no EEPROM is connected, this pin should be connected to V_{CC}. In this case it will function as an input to the 82595FX to indicate no EEPROM is connected.
EEPROMSK	117	O	**EEPROM SHIFT CLOCK:** This output is used to shift data into and out of the serial EEPROM.
EEPROMDO	119	O	**EEPROM DATA OUT**
EEPROMDI	118	O	**EEPROM DATA IN**

2.4 Miscellaneous Control

Symbol	Pin No.	Type	Name and Function
$\overline{\text{SMOUT}}$	18	I/O	This active LOW signal, when asserted, places the 82595FX into a Power Down mode. The 82595FX will remain in power down mode until $\overline{\text{SMOUT}}$ is unasserted. If this line is unconnected to $\overline{\text{SMOUT}}$ from the system bus, it can be used as an active low output which, when a POWER DOWN command is issued to the 82595FX, can be used to power down other external components (this output function is enabled by configuration).
J0 J1 J2	119 118 117	I I I	**JUMPER:** Input for selecting between 7 ISA IO spaces. These pins should be connected to either V_{CC} or GND or the EEPROM. The 82595FX reads the Jumper block during its initialization sequence.

J0	J1	J2	IO Address
Connected to EEPROM			Configuration contained in EEPROM
GND	GND	GND	I/O Window Disabled
V_{CC}	GND	GND	2A0h
GND	V_{CC}	GND	280h
V_{CC}	V_{CC}	GND	340h
GND	GND	V_{CC}	300h
V_{CC}	GND	V_{CC}	360h
GND	V_{CC}	V_{CC}	350h
V_{CC}	V_{CC}	V_{CC}	330h

2.4 JTAG Control

Symbol	Pin No.	Type	Name and Function
TDO	109	O	**JTAG TEST DATA OUT**
TMS	110	I	**JTAG TEST MODE SELECT**
TCK	111	I	**JTAG TEST CLOCK**
TDI	112	I	**JTAG TEST DATA IN**

2.5 Serial Interface

Symbol	Pin No.	Type	Name and Function
TRMT	122	O	Positive side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out A).
$\overline{\text{TRMT}}$	123	O	Negative side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out B).
RCV	115	I	The positive input to a differential amplifier connected to the RCV pair of the AUI cable (Data In A). It is driven with 10 Mb/s Manchester Encoded data.

2.5 Serial Interface (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RCV}$	116	I	The negative input to a differential amplifier connected to the RCV pair of the AUI cable (Data In B). It is driven with 10 Mb/s Manchester Encoded data.
CLSN	124	I	The positive input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In A).
$\overline{CLSN}$	125	I	The negative input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In B).
TDH	105	O	**TRANSMIT DATA HIGH:** Active high Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, $\overline{TDH}$, and $\overline{TDL}$ to generate the pre-conditioned twisted pair output waveform.
TDL	106	O	**TRANSMIT DATA LOW:** Twisted Pair Output Driver. Active high Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDH, $\overline{TDH}$, and $\overline{TDL}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{TDH}$	103	O	**TRANSMIT DATA HIGH INVERT:** Active low Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{TDL}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{TDL}$	104	O	**TRANSMIT DATA LOW INVERT:** Twisted Pair Output Driver. Active low Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{TDH}$ to generate the pre-conditioned twisted pair output waveform.
RD	114	I	Active high Manchester Encoded data received from the twisted pair.
$\overline{RD}$	113	I	Active low Manchester Encoded data received from the twisted pair.
X1	127	I	**20 MHz CRYSTAL INPUT:** This pin can be driven with an external MOS level clock when X2 is left floating. This input provides the timing for all of the 82595FX functional blocks.
X2	128	O	**20 MHz CRYSTAL OUTPUT:** If X1 is driven with an external MOS level clock, X2 should be left floating.

2.6 Serial Interface LEDs

Symbol	Pin No.	Type	Name and Function
AUI LED/BNC DIS	95	O	**AUI LED INDICATOR:** This output, when the 82595FX is used as a TPE/AUI solution, will turn on an LED when the 82595FX is actively interfaced to its AUI serial port. When the 82595FX is used as a BNC/AUI solution, this output becomes the **BNC DIS** output, which can be used to power down the BNC Transceiver section (the Transceiver and the DC to DC Converter) of the solution when the BNC port is unconnected.
LILED	98	O	**LINK INTEGRITY LED:** Normally on (low) ouput which indicates a good link integrity status when the 82595FX is connected to an active TPE port. This output will remain on when the Link Integrity function has been disabled. It turns off (driven high) when Link Integrity fails, or when the 82595FX is actively interfaced to an AUI port. The minimum off time is 100 ms.

2.6 Serial Interface LEDs (Continued)

Symbol	Pin No.	Type	Name and Function
ACTLED	97	O	**LINK ACTIVITY LED:** Normally off (high) output turns on to indicate activity for transmission, reception, or collision. Flashes at a rate dependent on the level of activity on the link.
POLED	96	O	**POLARITY LED:** If the 82595FX detects that the receive TPE wires are reversed, the POLED will turn on (low) to indicate the fault. POLED remains on even if automatic polarity correction is enabled, and the 82595FX has automatically corrected for the reversed wires.

2.7 Power and Ground

Symbol	Pin No.	Type	Name and Function
V_{CC}	1, 3, 7, 15, 26, 28, 40, 43, 46, 50, 57, 80, 84, 91, 99, 101, 107, 121, 129, 131, 141, 152	I	**POWER:** +5V ±5%.
V_{SS}	4, 6, 9, 11, 14, 17, 25, 27, 38, 39, 41, 44, 48, 52, 55, 59, 79, 82, 86, 89, 93, 100, 102, 108, 120, 126, 130, 136, 142, 151	I	**GROUND:** 0V.

2.8 Reserved Pins

Symbol	Pin No.	Type	Name and Function
N/C	5, 160		Reserved. Do not connect.

2.9 82595FX Pin Summary

ISA Bus Interface

ISA Pin Name	Pin Type	P-Down State
SA0–SA3 (In)		Inactive
SA4–SA11		Inactive/Act(1)
SA14–19 (In)		Inactive
SD0–SD15 (I/O)	TS	TS
$\overline{\text{SMEMR}}$ (In)		Inactive
$\overline{\text{SMEMW}}$ (In)		Inactive
$\overline{\text{IOR}}$ (In)		Inactive
$\overline{\text{IOW}}$ (In)		Inactive/Act(1)
INT0–7 (Out)	TS	TS
RESET DRV (In)		Act
$\overline{\text{IOCS16}}$ (Out)	OD	TS
IOCHRDY (Out)	OD	TS
$\overline{\text{SBHE}}$ (In)		Inactive
AEN (In)		Inactive/Act(1)

NOTE:
1. For hardware powerdown using $\overline{\text{SMOUT}}$, these pins will be inactive. For software powerdown, these pins remain active.

Local Memory Interface

Pin Name	MUXed Name	Pin Type	P-Down
LADDR[5:0] (Out)	FADDR[14:19]	2S	TS
LADDR[6:15] (Out)		2S	TS
LDATA[0:7] (I/O)		TS	TS
$\overline{\text{LWE}}$ (Out)		2S	TS
$\overline{\text{LOE}}$ (Out)		2S	TS
$\overline{\text{BOOTCS}}$ (Out)		2S	PU
$\overline{\text{SRAMCS}}$ (Out)		2S	PU
EEPROMCS (I/O)		TS	PD

Miscellaneous Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State	Dual Pin Name
J0(In)			ACT	EEPROM2D0 (In)
J1 (I/O)		TS	TS	EEPROM2DI (Out)
J2 (I/O)		TS	TS	EEPROM2SK (Out)
$\overline{\text{SMOUT}}$ (I/O)		TS	ACT/TS	

JTAG Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TMS (In)			In Act
TCK (In)			In Act
TDI (In)			In Act
TDO (Out)		TS	

Serial Interface

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TRMT (Out)		Ana	TS
$\overline{\text{TRMT}}$ (Out)		Ana	TS
RCV (In)		Ana	In Act
$\overline{\text{RCV}}$ (In)		Ana	In Act
CLSN (In)		Ana	In Act
$\overline{\text{CLSN}}$ (In)		Ana	In Act
TDH (Out)		Ana	TS
TDL (Out)		Ana	TS
$\overline{\text{TDH}}$ (Out)		Ana	TS
$\overline{\text{TDL}}$ (Out)		Ana	TS
RD (In)		Ana	In Act
$\overline{\text{RD}}$ (In)		Ana	In Act
X1 (In)			In Act
X2 (Out)		2S	TS
LILED (Out)		2S	TS*
POLED (Out)		2S	TS*
ACTLED (Out)		2S	TS*
AUILED (Out)	BNC DIS (Out)	2S	TS*

*Assuming auto-negotiation disabled.

Legend:
TS—TriState.
OD—Open Drain.
2S—Two State, will be found in either a 1 or 0 logic level.
Ana—Analog pin (all serial interface signals).
Act—Input buffer is active during Power Down.
In Act—Input buffer is inactive during Power Down.
PU—Output in inactive state with weak internal Pull-up during Power Down.
PD—Output in inactive state with weak internal Pull-down during Power Down.
Dual—Dual function pin.

3.0 82595FX INTERNAL ARCHITECTURE OVERVIEW

Figure 1 shows a high level block diagram of the 82595FX. The 82595FX is divided into four main subsections; a system interface, a local memory sub-system interface, a CSMA/CD unit, and a serial interface.

3.1 System Interface Overview

The 82595FX's system interface subsection includes a glueless ISA bus interface, and the 82595FX's IO registers (including the 82595FX's command, status, and Data In/Out registers). The system interface block also interfaces with the 82595FX's local memory interface subsystem and CSMA/CD subsystem.

The bus interface logic provides the control, address, and data interface to an ISA compatible bus. The 82595FX decodes up to 1M of total memory address space. Address decoding within 16K block increments (A14–A19) are used for Flash or Boot EPROM. IO accesses are decoded throughout the 1 Kbyte PC IO address range (A10 and A11 provide up to 4K of IO addressing and are used for Plug N' Play). The 82595FX data bus interface provides either an 8- or 16-bit interface to the host system's data bus. The control interface provides complete handshaking interface with the system bus to enable transfer of data between the 82595FX solution and the host system.

The 82595FX's IO registers provide 3 banks of directly addressable registers which are used as the control and data interface to the 82595FX. There are 16 IO registers per bank, with only one bank enabled at a time. This allows the complete 82595FX software interface to be contained in one 16-byte IO space. The base address of this IO space is selectable via either software (which can be stored in a serial EEPROM), or by strapping the 82595FX IO Jumper block (J0–J2). The 82595FX can also detect conflicts to its base IO space, and automatically resolve these conflicts either by allowing the selection of one Plug N' Play card from multiple cards (using Plug N' Play software), or by mapping itself into an un-used IO space (Automatic IO Resolution). Included in the 82595FX IO registers are the Command Register, the Status Register, and the Local Memory IO Port register, which provides the data interface to the local SRAM buffer contained in an 82595FX solution. Functions such as IO window mapping, Interrupt enable, RCV and XMT buffer initialization, etc. are also configured and controlled through the IO registers.

3.1.1 CONCURRENT PROCESSING FUNCTIONALITY

The 82595FX's Concurrent Processing feature significantly enchances data throughput performance by performing both system bus and serial link activities concurrently. Transmission of a frame is started by the 82595FX before that frame is completely copied into local memory. During reception, a frame is processed by the host CPU before that frame is entirely copied to local memory. Transmit Concurrent Processing feature is enabled by writing to BANK 2, Register 1, Bit 0. A 1 written to this bit enables this functionality, a 0 (default) disables it. To enable Receive Concurrent Processing, BANK 1, Register 7 must be programmed to value other than 00h (00h disables RCV Concurrent Processing, and is default). (See Section 4.1 for the format of IO BANK 1 and 2.) Improvements in concurrent processing functionality have allowed the 82595FX to include enhancements to the throughput efficiency of the 82595TX. For details, refer to the 82595FX User's Guide. Concurrent Processing is not recommended for 8-bit interfaces. For more information on Transmit and Receive Concurrent Processing, refer to Section 7.0 and Section 8.0.

3.2 Local Memory Interface

The 82595FX's local memory interface includes a DMA unit which controls data transfers to or from the 82595FX's local SRAM, control for access to a Boot EPROM/FLASH, and two interfaces to a serial EEPROM. The local memory interface subsection also arbitrates accesses to the local memory by the host CPU and the 82595FX.

Data transfers between the 82595FX and the local SRAM are always through the 82595FX's Local Memory 16-bit/32-bit IO Port. This allows the entire SRAM memory (up to 64 Kbytes) to be mapped into one IO location in the host systems IO map. By setting a configuration bit in the 82595FX's IO Registers (32IO/HAR#), the local memory can be extended from 16 bits to a full 32 bits. During 32-bit accesses, the CPU would perform a doubleword access addressed to register 12 of BANK0. The ISA bus will break this access up into two 16-bit accesses to Registers 12/13 followed by Registers 14/15, (or 4 sequential 8-bit accesses in an 8-bit interface). The CPU always accesses the 82595FX IO Port for Receive or Transmit data transfers, while the 82595FX automatically increments the address to the SRAM after each CPU access. The SRAMs data path is an 8-bit interface (typically 64K by 8-bits wide, or 256K by 8-bits wide) to allow for the lowest possible solution cost. The 82595FX implements a

prefetch mechanism to the local SRAM so that the data is always available to the CPU as either an 8- or 16-bit word. In the case of the CPU reading from the SRAM, the 82595FX reads the next two bytes from the SRAM, the 82595FX between CPU cycles so that the data is always available as a word in the 82595FX's Local Memory IO Port register. In the case of the CPU writing to the SRAM, the data is written into the 82595FX's Local Memory IO Port then transferred to the SRAM by the 82595FX between CPU cycles. This prefetch mechanism of the 82595FX allows for IO read and writes to the local memory to be performed with no additional wait-states (3 clocks per data transfer cycle).

The DMA unit provides addressing and control to move RCV or XMT data between the 82595FX and the local SRAM. For transmission, the CPU is required only to copy the data to the local memory, initialize the 82595FX's DMA Current Address Register (CAR) to point to the beginning of the frame, and issue a Transmit Command to the 82595FX. The DMA unit facilitates the transfers from the local memory to the 82595FX as transmission takes place. The DMA unit will reset upon collision during a transmission, enabling automatic re-transmission of the transmit frame. During reception, the DMA unit implements a recyclable ring buffer structure which can receive continuous back to back frames without CPU intervention on a per frame basis (see Section 8.2 for details).

The 82595FX provides address decoding and control to allow access to an external Boot EPROM/FLASH if these components are utilized in an 82595FX design. The 82595FX also provides an interface to a serial EEPROM to replace jumper blocks used to contain configuration information. This port is used to store configuration information and in addition, it is used to store Plug N' Play information as defined in the Plug N' Play Specification.

The 82595FX arbitrates accesses to the local memory sub-system by the CPU and the 82595FX. The arbitration unit will hold off an 82595FX DMA cycle to the local memory if a CPU cycle is already in progress. Likewise, it will hold off the CPU if an 82595FX cycle is already in progress. The cycle which is held off will be completed on termination of the preceding cycle.

3.3 CSMA/CD Unit

The CSMA/CD unit implements the IEEE 802.3 CSMA/CD protocol. It performs such functions as transmission deferral to link traffic, interframe spacing, exponential backoff for collision handling, address recognition, etc. The CSMA/CD unit serves as the interface between the local memory and the serial interface. It serializes data transferred from the local memory before it is passed to the serial interface unit for transmission. During frame reception, it converts the serial data received from the serial interface to a byte format before it is transferred to local memory. The CSMA/CD unit strips framing parameters such as the Preamble and SFD fields before the frame is passes to memory for reception. For transmission, the CSMA/CD unit builds the frame format before the frame is passed to the serial interface for transmission.

3.4 Serial Interface

The 82595FX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also interface to a transceiver device to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595FX automatically enables either to the AUI or TPE interface depending on which medium is connected to the chip. Software configuration can override this automatic selection.

4.0 ACCESSING THE 82595FX

All access to the 82595FX is made through one of three banks of IO registers. Each bank contains 16 registers. Each register in a bank is directly accessible via addressing. Through the use of bank switching, the 82595FX utilizes only 16 IO locations in the host system's IO map to access each of its registers. The different banks are accessed by setting the POINTER field in the 82595FX Command Register to select each bank. The Command Register is Register for each bank.

4.1 82595FX Register Map

The 82595FX registers are contained in three banks of 16 IO registers per bank. These three banks are shown in the following three pages.

4.1.1 IO BANK 0

The format for IO Bank 0 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
RCV States		EXEC States		EXEC INT	TX INT	RX INT	RX STP INT	Reg 1
ID REGISTER (Counter)		1	(Auto En)	0	1	0 RESERVED		Reg 2
0 Resvrd	0 Resvrd	Cur/$\overline{\text{Base}}$	32 IO/$\overline{\text{HAR}}$	EXEC Mask	TX Mask	RX Mask	RX STP Mask	Reg 3
RCV CAR/BAR (Low)								Reg 4
RCV CAR/BAR (High)								Reg 5
RCV STOP REG (Low)								Reg 6
RCV STOP REG (High)								Reg 7
RCV Copy Threshold REG								Reg 8
EARLY XMT THRESHOLD REGISTER (XTR)								Reg 9
XMT CAR/BAR (Low)								Reg 10
XMT CAR/BAR (High)								Reg 11
Host Address Reg (Low) /32-Bit I/O (Byte 0)								Reg 12
Host Address Reg (High) /32-Bit I/O (Byte 1)								Reg 13
Local Memory I/O Port (Low) /32-Bit I/O (Byte 2)								Reg 14
Local Memory I/O Port (High) /32-Bit I/O (Byte 3)								Reg 15

4.1.2 IO BANK 1

The format for IO Bank 1 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
$\overline{\text{Tri-ST}}$ INT	0 Resvrd	0 Resvrd	0 Resvrd	0 Resvrd	0 Resvrd	Host Bus Wd	0 Resvrd	Reg 1
FL/$\overline{\text{BT}}$ $\overline{\text{Present}}$	Boot EPROM/FLASH Decode Window			Bad IRQ	INT Select			Reg 2
0	0	I/O Mapping Window						Reg 3
0	0	0	0	0	0	0	0	Reg 4
(Reserved)								
0	0	0	0	0	0	0	0	Reg 5
(Reserved)								
BACK TO BACK TRANSMIT IFS								Reg 6
RCV BOF Threshold REG								Reg 7
RCV LOWER LIMIT REG (High Byte)								Reg 8
RCV UPPER LIMIT REG (High Byte)								Reg 9
XMT LOWER LIMIT REG (High Byte)								Reg 10
XMT UPPER LIMIT REG (High Byte)								Reg 11
FLASH SELECT	PAGE HIGH	FLASH WRITE ENABLE		FLASH PAGE SELECT				Reg 12
0	0	0	0	0	$\overline{\text{SMOUT}}$ OUT EN	0 Resvrd	0 Resvrd	Reg 13
(Reserved)								
0	0	0	0	0	0	0	0	Reg 14
(Reserved)								
0	0	0	0	0	0	0	0	Reg 15
(Reserved)								

4.1.3 IO BANK 2

The format for IO Bank 2 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
Disc Bad Fr	Tx Chn $\overline{\text{ErStp}}$	Tx Chn Int Md	Res 0	0	0 (Reserved)	0	TX Con Proc En	Reg 1
LoopBack		Multi IA	No SA Ins	Length $\overline{\text{Enable}}$	RX CRC In MEM	BC DIS	PRMSC Mode	Reg 2
Test 1	Test 2	BNC/ $\overline{\text{TPE}}$	$\overline{\text{APORT}}$	Jabber Disable	TPE/ $\overline{\text{AUI}}$	Pol $\overline{\text{Corr}}$	Link In Dis	Reg 3
INDIVIDUAL ADDRESS REGISTER 0								Reg 4
INDIVIDUAL ADDRESS REGISTER 1								Reg 5
INDIVIDUAL ADDRESS REGISTER 2								Reg 6
INDIVIDUAL ADDRESS REGISTER 3								Reg 7
INDIVIDUAL ADDRESS REGISTER 4								Reg 8
INDIVIDUAL ADDRESS REGISTER 5								Reg 9
STEPPING			Turnoff Enable	EEDO	EEDI	EECS	EESK	Reg 10
RCV NO RESOURCE COUNTER								Reg 11
Reserved 0								Reg 12
Polarity $\overline{\text{LED}}$	Link $\overline{\text{LED}}$	Activity $\overline{\text{LED}}$	0 (Resvrd)	Auto-Negotiation Status		A-N Enable	FDX/ $\overline{\text{HDX}}$	Reg 13
0	0	0	0	0	0	0	0	Reg 14
			(Reserved)					
0	0	0	0	0	0	0	0	Reg 15
			(Reserved)					

4.2 Writing to the 82595FX

Writing to the 82595FX is accomplished by an IO Write instruction (such as an OUT instruction) from the host processor to one of the 82595FX registers. The 82595FX registers reside in a block of 16 contiguous addresses contained within the PC IO address space. The mapping of this address block is programmable throughout the 1 Kbyte PC IO address map.

The 82595FX registers are contained within three banks of IO registers. When writing to a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once a bank is selected, all register accesses are made in that bank until a switch to another bank is performed. Switching banks is accomplished by writing to the PTR field of Reg 0 in any bank. Reg 0 is the command register of the 82595FX and its functionality is identical in each bank. Once in the appro-

priate bank, the processor can write directly to any of the 82595FX registers by simply issuing an OUT instruction to the IO address of the register.

4.3 Reading from the 82595FX

Reading from the 82595FX is accomplished by an IO Read instruction (such as an IN instruction) from the host processor to one of the 82595FX registers. When reading from a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once in the appropriate bank, the processor can read directly from any of the 82595FX registers by simply issuing an IN instruction to the IO address of the register.

4.4 Local SRAM Accesses

IO mapping the local SRAM memory of an 82595FX solution allows it to appear as simply an IO Port to the host system. This allows an 82595FX solution to work in PCs which do not have enough space in their system memory map to accommodate the addition of LAN buffer memory (typically 16 Kbytes to 64 Kbytes) into the map. The entire local memory (up to 64 Kbytes) is mapped into one 16-bit IO Port location. For all IO-mapped accesses to the local memory of a 82595FX solution, the 82595FX performs the IO address decoding and the ISA Bus interface handshake and asserts the address and control signals to the local memory.

4.4.1 WRITING TO LOCAL MEMORY

The local memory of an 82595FX solution is written to whenever the host CPU performs a Write operation to the 82595FX Local Memory IO Port. Prior to writing a block of data to the local memory, the CPU should update the 82595FX Host Address Register with the first address to be written. The CPU then copies the data to the local memory by writing it to the 82595FX Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82595FX upon completion of each write cycle. This allows sequential accesses to the local memory, even though the IO port address accessed does not change.

4.4.2 READING FROM LOCAL MEMORY

The local memory of an 82595FX solution is read from whenever the host CPU performs a Read operation from the 82595FX Local Memory IO Port. Prior to reading a block of data from the local memory, the CPU should utilize the 82595FX Host Address Register to point to first address to be read. The CPU then reads the data from the local memory through the 82595FX Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82595FX upon completion of each read cycle.

4.5 Serial EEPROM Interface

A Serial EEPROM, a Hyundai HY93C46 or equivalent IC, stores configuration data for the 82595FX. The use of an EEPROM enables 82595FX designs to be implemented without jumpers (the use of jumpers to select IO windows is optional.) The port interface to the serial EEPROM provides both configuration and Plug N' Play information access. Plug N' Play allows peripheral functions to be added to a PC (such as adapter cards) without the need to individually configure each parameter (e.g. Interrupt, IO Address, etc). Information describing system resources are contained within the 82595FX configuration registers. This allows Auto-configuration software, which is usually contained in the BIOS or O/S, to identify system resource usage, identify conflicts and automatically re-configure the 82595FX.

The 82595FX automatically accesses Register 0 of the EEPROM upon a RESET in ISA Bus Interface mode. Register 0 contains the information that the 82595FX must be configured to allow CPU accesses to it (IO Mapping Window, FLASH Detect Enable, Auto I/O Enable, Boot EPROM/FLASH Window, Host Bus Width, and Plug N' Play Enable) following a system boot. The format for EEPROM Register 0 is shown in Figure 4-1. Note that all 0's are assumed to be reserved. In the case where an EEPROM is either unprogrammed (each bit defaults to a 1) or completely erased (all 0's), the 82595FX will default to IO Address 300h.

Word0, Bit 1, the Word 1 Enable bit, is asserted to enable the read of EEPROM Word 1 during reset. This bit is active high.

NOTE:
If Word 1 of the EEPROM is not to be read during a reset, software must wait 200 μs after the reset is issued before accessing the 82595FX, as was the case on all versions of the 82595. If Word 1 is to be read during a reset, software must wait 400 μs after reset before accessing the part. During this "blackout" period, the part will not respond to accesses on the ISA bus.

Word 0, Bit 8, is the Flash Present bit. This bit is active low to indicate the presence of flash memory, as in the 82595FX B-3. The functionality of the bit is changed from the 82595FX B-2 and prior versions. Word 0, Bit 9 is the Auto-Negotiation, or A-N, Enable bit for the negotiation process at boot time. The bit is active high.

Word 1 of the EEPROM is used to store the INT Select value to which the part will default on reset. The mapping from INT Select to IRQ is explained later in this document. The value stored in bits 0 through 2 of word 1 of the EEPROM is loaded into the INT Select register of the 82595FX, bank 1, register 2, bits 0 through 2 on any hardware or software reset. The reading of Word 1 on reset is enabled when bit 1 of word 0 of the EEPROM is set. If this bit is not set on reset, word 1 will not be read and the INT select register and Bad IRQ bit in bank 1 will be initialized to zero.

For additional information regarding a Plug N' Play implementation for the 82595FX, please consult the 82595FX User's Guide and LAN595TX Specification, available through your local sales representative. The latest Plug N' Play Specification is available by Microsoft.

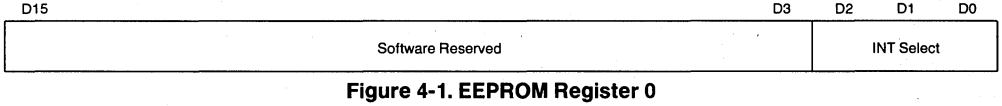


Figure 4-1. EEPROM Register 0

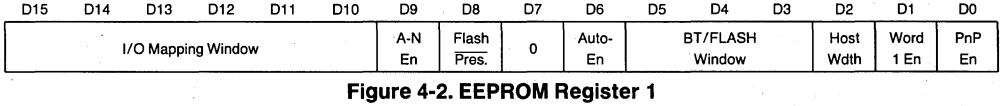


Figure 4-2. EEPROM Register 1

4.6 Boot EPROM/FLASH Interface

The Boot EPROM/FLASH of an 82595FX solution is read from or written to (FLASH only) whenever the host CPU performs a Read or a Write operation to a memory location that is within the Boot EPROM/FLASH mapping window. This window is programmable throughout the ISA PROM address range (C8000–DFFFF) by configuring the 82595FX Boot EPROM Decode Window register (Bank 1, Register 2, bits 4–6). The 82595FX asserts the BOOTCS# signal when it decodes a valid access. Up to 1 MBytes of FLASH can be addressed by the 82595FX.

5.0 COMMAND AND STATUS INTERFACE

The format for the 82595FX Command Register is shown in Figure 5-1. The Command Register resides in Register 0 of each of the three IO Banks of the 82595FX, and can be accessed in any of these banks. The Command Register is accessed by writing to or reading from the IO address for Register 0.

5.1 Command OP Code Field

Bits 0 through 4 of the Command Register comprise the Command OP Code field. A command is issued to the 82595FX by writing it into the Command OP Code field. A command can be issued to the 82595FX at any time; however in certain cases the command may be ignored (for example, issuing a Transmit command while a Transmit is already in progress). In these cases the command is not performed, and no interrupt will result from it.

The Command OP Code field can also be read. In this case it will indicate an execution status event other than TRANSMIT DONE (TDR Done, DIAGNOSE Done, MC-SETUP Done, DUMP Done, INIT Done, and POWER-UP) has been completed. This field is valid only when the EXEC INT bit (Bank 0, Reg 1, Bit 3) is set.

5.2 ABORT (Bit 5)

This bit indicates if an execution command other than TRANSMIT was aborted while in progress. This bit provides status information only. It should be written to a 0 whenever the Command Register is written to.

5.3 Pointer Field (Bits 6 and 7)

The Pointer field controls which 82595FX IO register bank is currently to be accessed (Bank 0, Bank 1, or Bank 2). Writing a 00:b to the Pointer field selects Bank 0, 01:b for Bank 1, and 10:b for Bank 2. The Pointer field is valid only when the SWITCH BANK (0h) command is issued. This field will be ignored for any other command. The 82595FX will continue to operate in a current bank until a different bank is selected. Upon power up of the device or Reset, the 82595FX will default to Bank 0.

7	6	5	4	3	2	1	0	
Pointer		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)

Figure 5-1. 82595FX Command Register

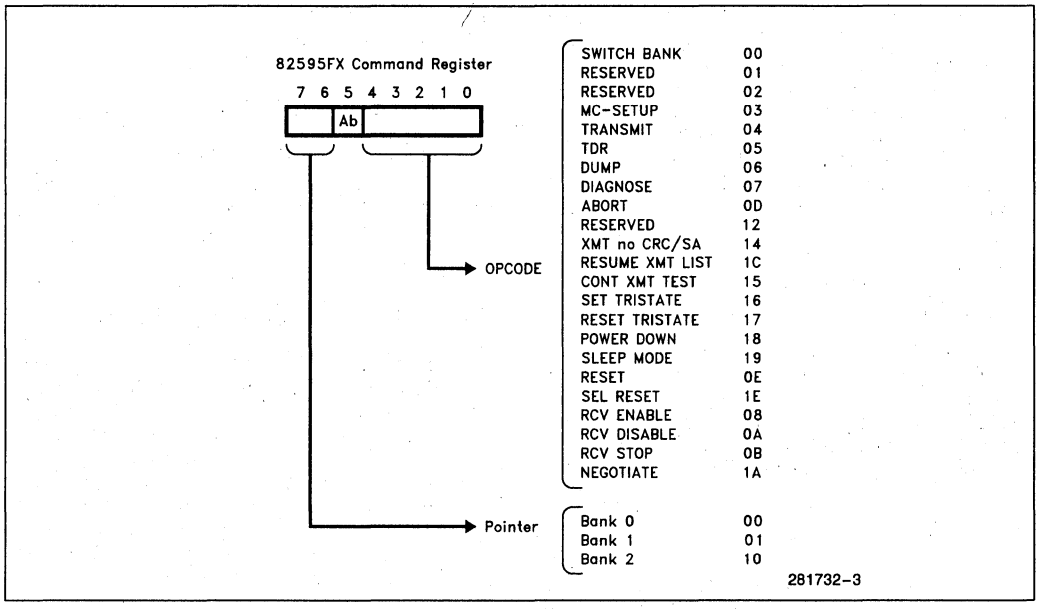


Figure 5-2. 82595FX Command Interface

5.4 82595FX Status Interface

The Status of the 82595FX can be read from Register 1 of Bank 0, with additional status information contained in Register 0 (the Command Register). Figure 5-3 shows these registers. Other information concerning the configuration and initialization of the 82595FX and its registers can be obtained by directly reading the 82595FX registers.

When read, the Command OP Code field indicates which event (MC Done, Init Done, TDR Done, or DIAG Done) has been completed. This field is valid only when the EXEC INT Bit (Bank 0, Reg 1, Bit 3) is set to a 1. Reading the Pointer field indicates which bank the 82595FX is currently operating in. Register 1 in Bank 0 contains the 82595FX interrupts status as well as the current states of the RCV and Execution units of the 82595FX. Resultant status from events such as the completion of a transmission or the reception of an incoming frame is contained in the status field of the memory structures for these particular events.

6.0 INITIALIZATION

Upon either a software or hardware RESET, the 82595FX enters into its initialization sequence. When the 82595FX is interfaced to an ISA bus, the 82595FX reads information from its EEPROM and Jumper block (if utilized) which configures critical parameters (IO Address mapping, etc.) to allow initial accesses to the 82595FX during the host system's initialization sequence and also access by the software device driver. The 82595FX can also be configured (via the EEPROM) to automatically resolve any conflicts to its IO address location either by moving its IO address offset to an unused location in the case that a conflict occurs, or by using the Plug N' Play Software to the I/O address location. This process eliminates a large majority of LAN end-user setup problems.

The 82595FX can be configured to operate with ISA systems that require early deassertion of the IOCHRDY signal to its low (not ready) state. The 82595FX, along with its software driver, can perform a test at initialization to determine if early IOCHRDY deassertion is required.

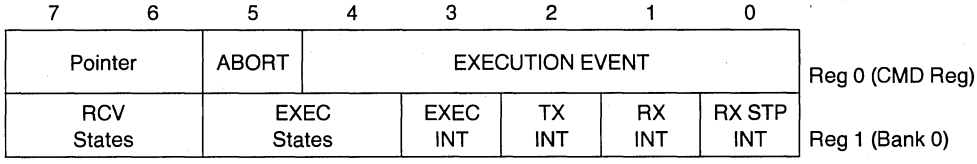


Figure 5-3. 82595FX Status Information

7.0 FRAME TRANSMISSION

The 82595FX performs all of the necessary functions needed to transmit frames from its local memory. If Transmit Concurrent Processing is enabled, the CPU must only program the Base and Host Address Register with the starting address to be transmitted, copy a portion of the frame into the 82595FX's transmit buffer located in local memory (the number of bytes for this first portion is determined by the software driver without causing an Underrun), issue a XMT command to the 82595FX, and complete the data copies for this frame to local memory. If Transmit Concurrent Processing is disabled, the CPU must copy an entire frame into the 82595FX's transmit buffer located in local memory, set up the 82595FX's Current Address Registers to point to that frame, and issue a XMT command to the 82559TX. The 82595FX performs all the link management functions, DMA operations, and statistics keeping to handle transmission onto the link and communicate the status of the transmission to the CPU. The 82595FX performs automatic retransmission on collision with no CPU interaction.

7.1 82595FX XMT Block Memory Format

The format in which a XMT block is written to memory by the CPU is shown in Figure 7-1 for a 16-bit interface. Figure 7-2 shows this structure for an 8-bit interface.

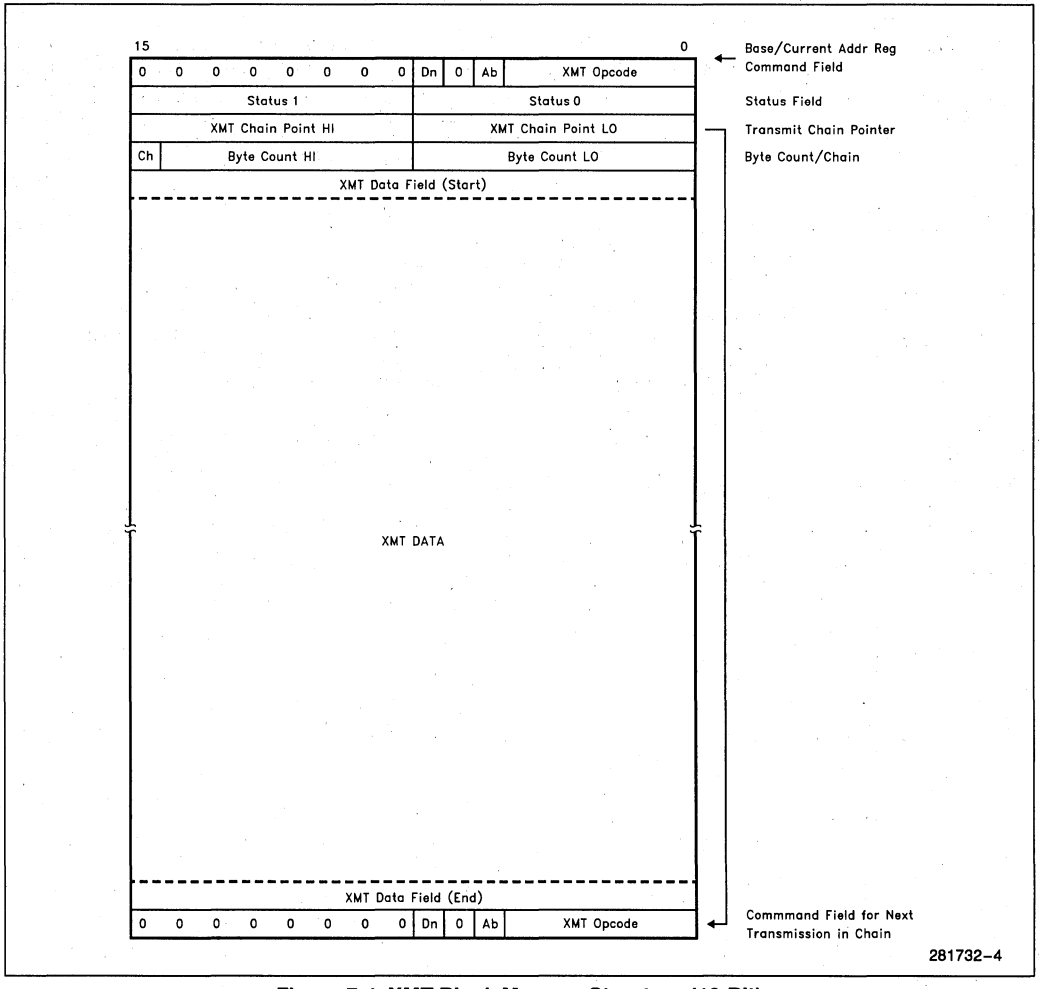


Figure 7-1. XMT Block Memory Structure (16-Bit)

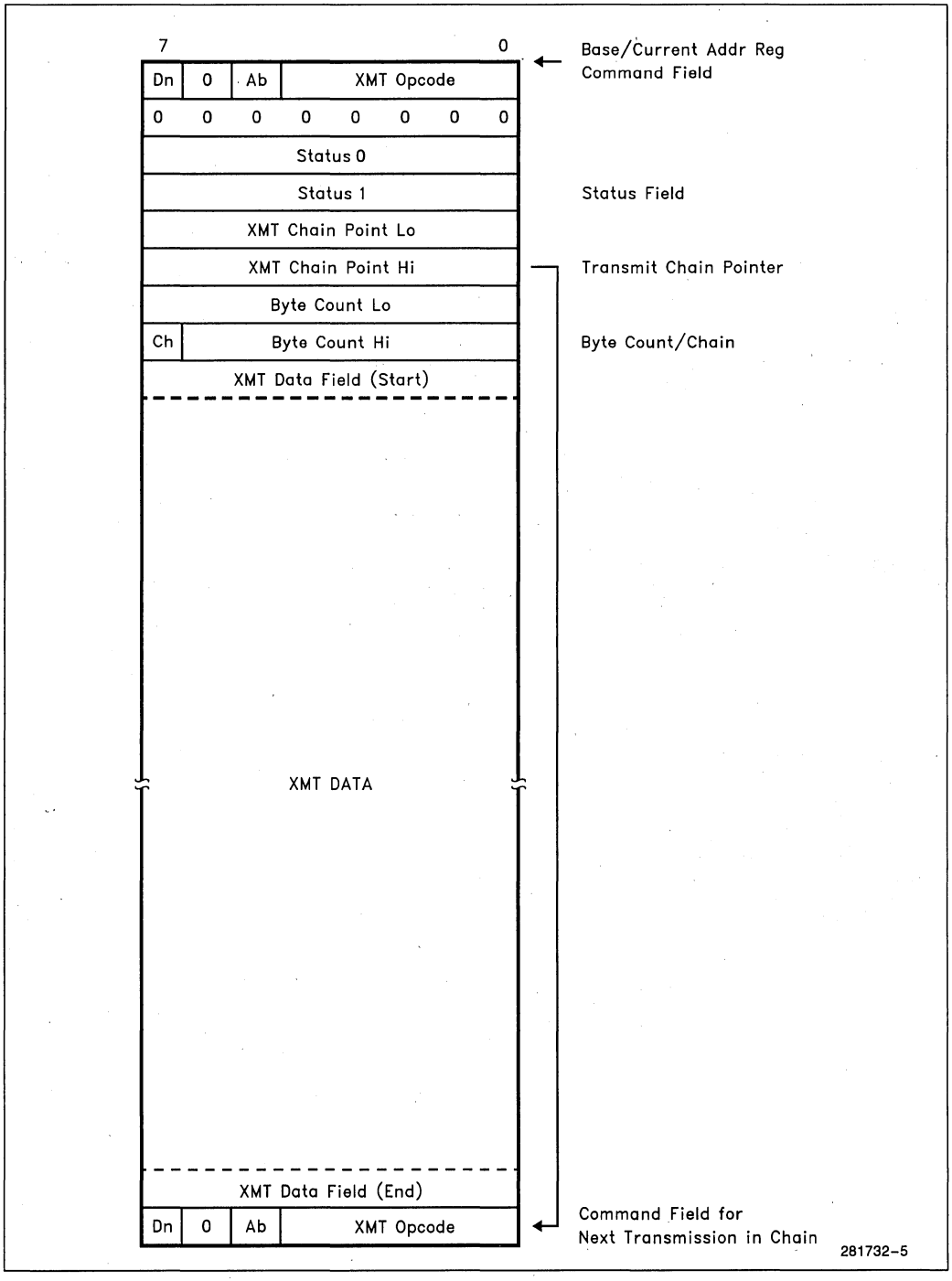


Figure 7-2. XMT Block Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 7-3. In a 16-bit wide interface, these two bytes will combine to form one word. This field is originally set to all 0's by the CPU as the XMT block is copied to memory. It is updated by the 82595FX upon completion of the transmission.

7.2 XMT Chaining

The 82595FX can transmit consecutive frames without the CPU having issued a separate Transmit command for each frame. This is called Transmit Chaining. The 82595FX Transmit Chaining memory structure for a 16-bit interface is shown in Figure 7-4, with an 8-bit interface shown in Figure 7-5. The 82595FX registers which control the memory structure are also shown. The CPU places multiple XMT blocks in the Transmit buffer. The 82595FX will transmit each frame in the chain, reporting the status for each frame in its status field. If Concurrent Processing is enabled, the copy of additional frames in a chain will take place while the first portion of the chain (one or more frames) is being transmitted by the 82595FX. This chain can be dynamically updated by the CPU to add more frames to the chain. The transmit chain can be configured to terminate upon an errored frame (maximum collisions, underrun, lost CRS, etc.) or it can continue to the next frame in the chain. The 82595FX can be configured to interrupt upon completion of each transmission or to interrupt at the end of the transmit chain only (it always interrupts upon an errored condition).

7	6	5	4	3	2	1	0	
TX DEF	HRT BET	MAX COL	X	No OF COLLISIONS				Status 0
COLL	X	TX OK	0	LTCOL	LST CRS	X/JERR(1)	UND RUN	Status 1

NOTE:
1. Only functional in full duplex operations.

Figure 7-3. Transmit Result

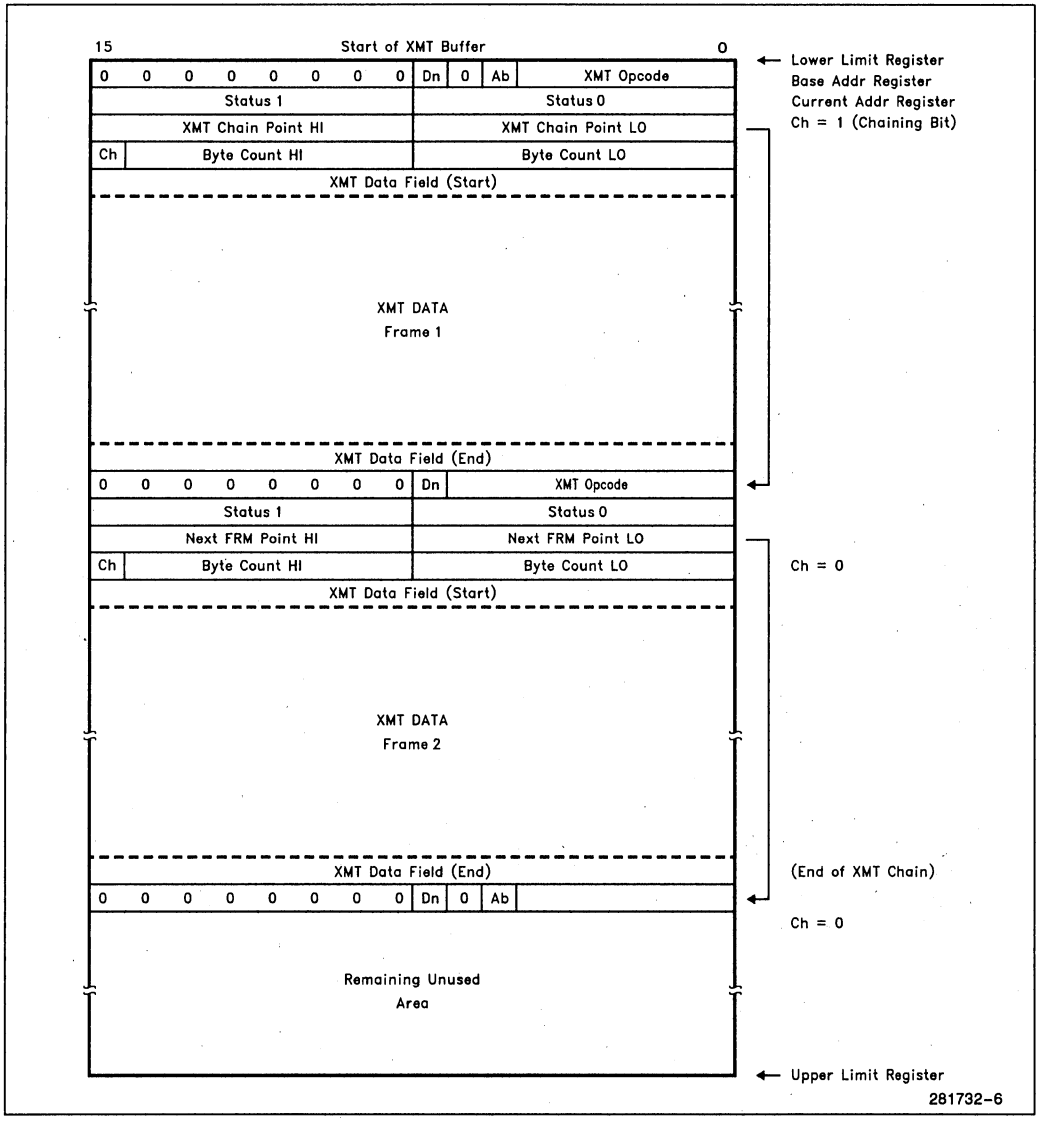


Figure 7-4. 82595FX XMT Chaining Memory Structure

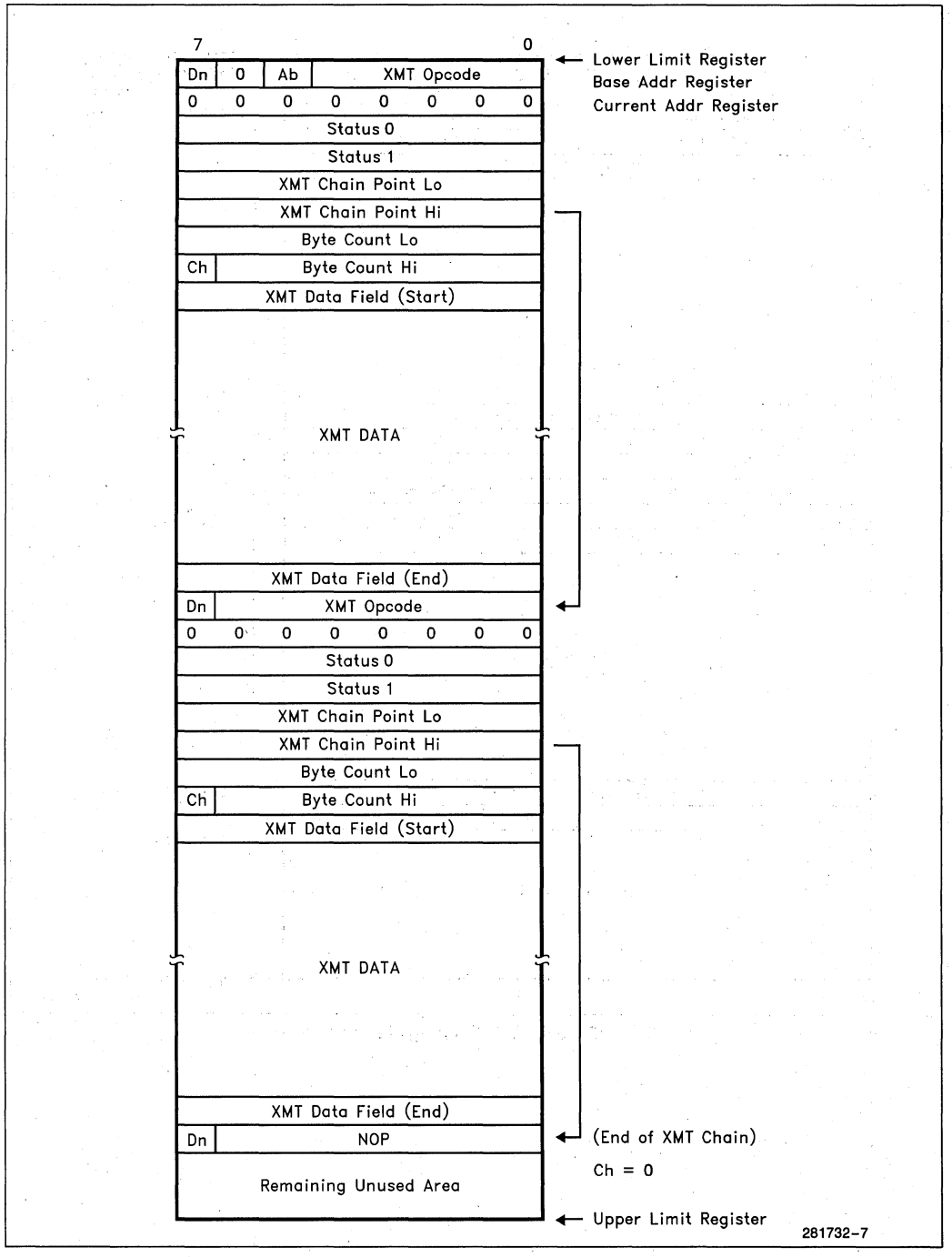


Figure 7-5. XMT Block Memory Structure (8-Bit)

7.3 Automatic Retransmission on Collision

The 82595FX performs automatic retransmission when a collision is experienced within the first slot time of the transmission with no intervention by the CPU. The 82595FX performs jamming, exponential backoff, and retransmission attempts as specified by the IEEE 802.3 spec. The 82595FX reaccesses its local memory automatically on collision. This allows the 82595FX to retransmit up to 15 times after the initial collision with no CPU interaction.

The 82595FX reaccesses the data in its transmit buffer by simply resetting the value of its Current Address Register back to the value of the Base Address Register (the beginning of the XMT block) and repeating the DMA process to access the data in the transmit buffer again. Once it regains access to the link, retransmission is attempted. When Transmit Chaining is utilized, the process for retransmission is exactly the same. Only the current frame in the chain will be retransmitted, since the Base Address Register is updated upon transmission of each frame.

8.0 FRAME RECEPTION

The 82595FX implements a recyclable ring buffer DMA structure to support the reception of back to back incoming RCV frames with minimal CPU overhead. The structure of the RCV frames in memory is optimized to allow the CPU to process each frame with as few software processing steps as possible. The frame format is arranged so that all of the required infomation for each frame (status, size, etc.) is located at the beginning of the frame.

8.1 82595FX RCV Memory Structure

The 82595FX RCV memory structure for a 16-bit interface is shown in Figure 8-1. Figure 8-2 shows this structure for the 8-bit interface. Once an incoming frame passes the 82595FX's address filtering, the 82595FX deposits the frame into the RCV Data field of the RCV Memory Structure. The fields which precede the RCV Data field, Event, Status, Byte Count, Next Frame Pointer, and the Event field of the following frame, are updated upon the end of the frame after all of the incoming data has been deposited in the RCV Data field. If Receive Concurrent Processing is enabled, the CPU processes the receive frame without the entire frame being deposited by the 82595FX to the RCV Data Field. The 85295FX, along with the software driver, determines the portion of the frame being copied to host memory before the rest of that frame is copied to local memory. An interrrupt is asserted by the 82595FX (EOF) after frame reception has been completed.

If the 82595FX is configured to Discard Bad Frames, it will discard all incoming errored frames by resetting its DMA Current Address Register back to the value of the Base Address Register and not updating any of the fields in the RCV frame structure. This area will now be reused to store the next incoming frame.

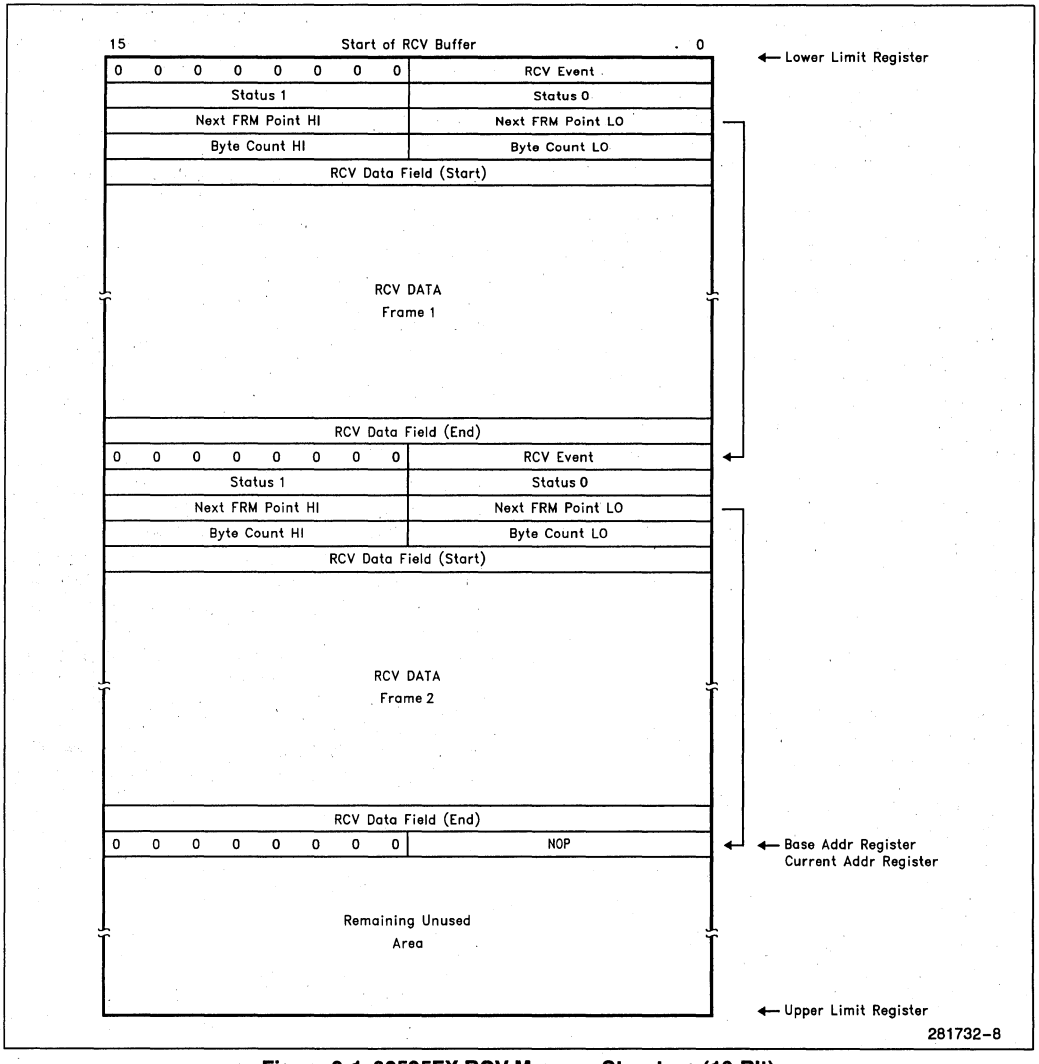


Figure 8-1. 82595FX RCV Memory Structure (16-Bit)

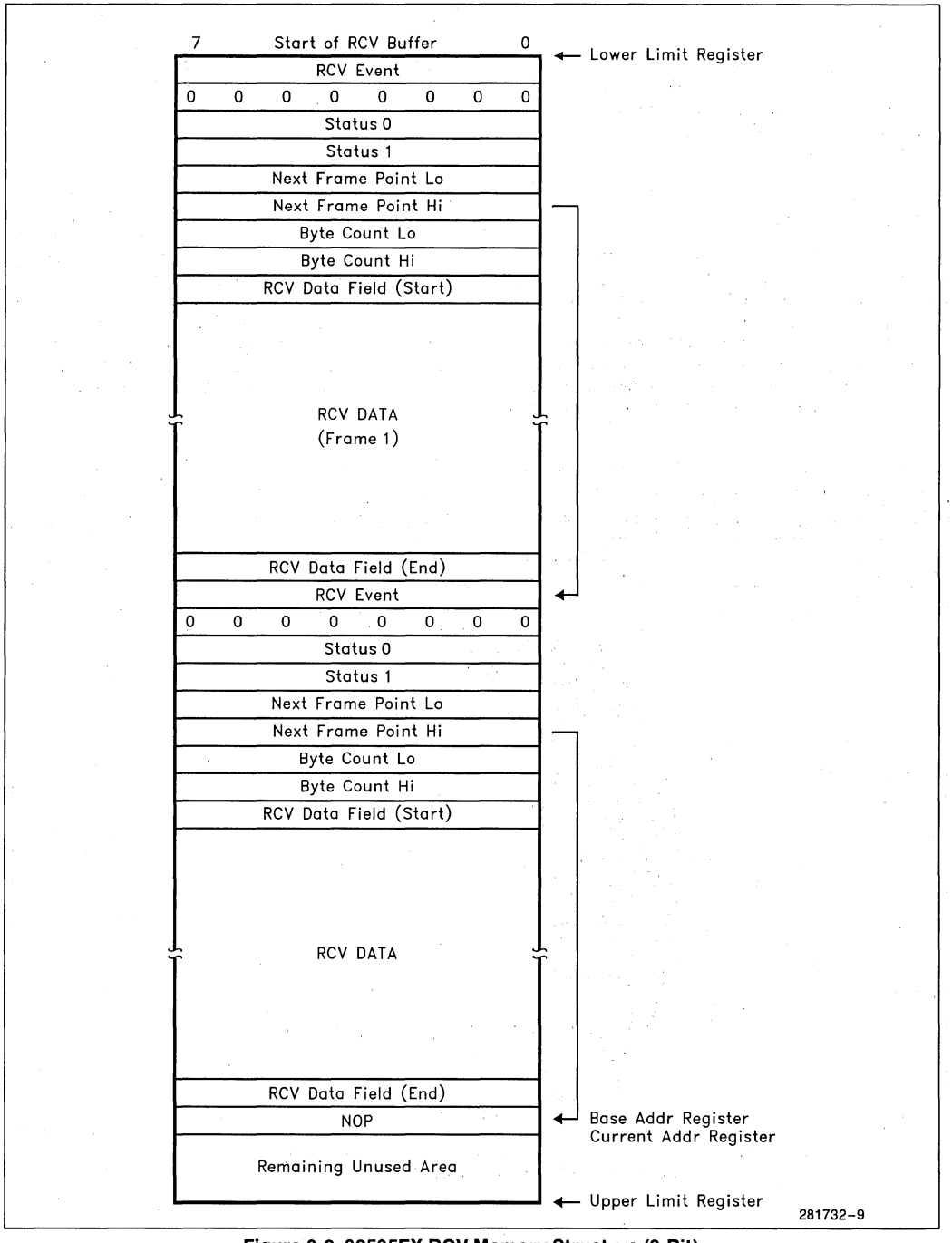


Figure 8-2. 82595FX RCV Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 8-3. In a 16-bit wide interface, these two bytes will combine to form one word. The 82595FX provides this field for each incoming frame.

8.2 RCV Ring Buffer Operation

The 82595FX RCV Ring Buffer operation is illustrated in Figure 8-4. The 82595FX copies received frames sequentially into the RCV Buffer area of the local memory. The CPU processes these frames by copying the frames from the local memory. After a frame is processed, the CPU updates the 82595FX's Stop Register to point to the last location processed. This indicates that the RCV Buffer memory which precedes the value programmed in the Stop Register is now free area (it has been processed by the CPU). When the 82595FX reaches the end of the RCV Buffer (the Upper Limit Register value) it will now wrap around back to the beginning of the buffer, and continue to copy RCV frames into the buffer, beginning at the value pointed to by the Lower Limit Register. The 82595FX will continue to copy frames into the RCV Buffer area as long as it does not reach the address pointed to by the Stop Register (if this does occur, the 82595FX stops copying the frames into memory and issues an Interrupt to the CPU). As the CPU processes additional incoming frames, the Stop Register value continues to be moved. This action allows the CPU to keep ahead of the incoming frames and allows the Ring Buffer to be continually recycled as the memory space consumed by an incoming frame is reused as that frame is processed.

7	6	5	4	3	2	1	0	
SRT FRM	X	X	1	X	X	IA MCH	RCLD	Status 0
TYP/$\overline{\text{LEN}}$	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR RN	Status 1

Figure 8-3. RCV Status Field

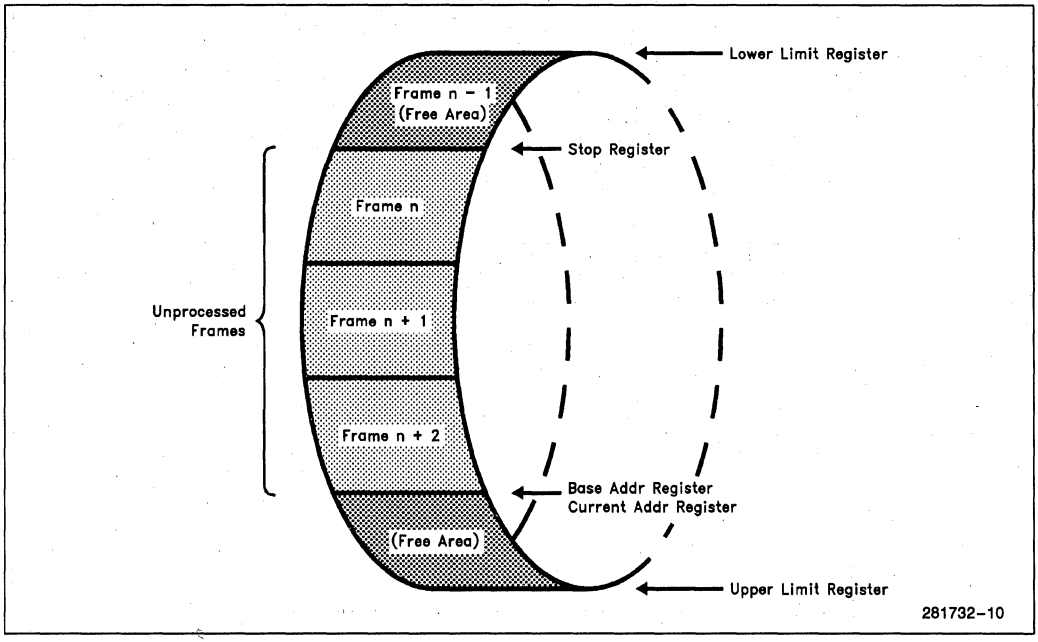


Figure 8-4. 82595FX RCV Ring Buffer Operation

9.0 SERIAL INTERFACE

The 82595FX's serial interface subsystem incorporates all the active circuitry required to interface the 82595FX to 10BASE-T networks or to the attachment unit (AUI) interface. It includes on-chip AUI and TPE drivers and receivers as well as Manchester Encoder/Decoder and Clock Recovery circuitry. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also be interfaced to a transceiver to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595FX automatically enables either the AUI or TPE interface, depending on which medium is active. This automatic selection can be overridden by software configuration. The TPE interface also features a polarity fault detection and correction circuit which will detect and correct a polarity error on the twisted pair wire, the most common wiring fault in twisted pair networks.

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ±0.01% clock required by the IEEE 802.3 specification.

The 82595FX supports 802.3 Half Duplex Ethernet functionality, as did previous versions of the 82595. It also supports a Full Duplex Ethernet mode that complies with *Specifications for Full Duplex Ethernet*, Rev. 1.0, Sept. 9th, 1993, from Kalpana, when connected to a Full Duplex hub through the TPE port. Full-duplex provides increased network throughput (using full duplex network components) by providing dedicated channels for both Transmit and Receive data at the same time. Full Duplex operation is transparent to existing software drivers. More details on Full Duplex functionality can be found in the 82595FX User's Guide.

Auto-Negotiation (or N-Way) is a method of maximizing network operational efficiency. Auto-Negotiation works by interrogating Auto-Negotiation compliant equipment to determine the highest common mode of operation shared by all connected devices. When Auto-Negotiation is enabled, the 82595FX will negotiate the Highest Common Denominator (HCD) transmission mode with the hub to which it is attached, on a hardware reset. If the hub does not support Auto-Negotiation and Auto-Negotiation is enabled on the 82595FX, the 82595FX will revert to Half Duplex.

The 82595FX is in Auto-Negotiation mode only when the A-N Enable bit, bit 1 in register 13 of bank 2, is set. On hardware reset, the state of this bit is copied from the EEPROM A-N Enable bit, bit 9 of Word 0 of the EEPROM.

We recommend that a crystal that meets the following specifications be used:

- Quartz Crystal
- 20.00 MHz ±0.002% at 25°C
- Accuracy ±0.005% over Full Operating Temperature, 0°C to +70°C
- Parallel resonant with 20 pF Load Fundamental Mode

Several vendors have such crystals; either off-the-shelf or custom-made. Two possible vendors are:

1. M-Tron Industries, Inc.
   Yankton, SD 57078
   Specifications:
   Part No. HC49 with 20 MHz, 50 PPM over 0°C to +70°C, and 20 pF fundamental load.
2. Crystek Corporation
   100 Crystal Drive
   Ft. Myers, FL 33907
   Part No. 013212

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics; therefore, it is advisable to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 pF and 35 pF.

An external 20 MHz MOS-level clock may be applied to pin X1, if pin X2 is left floating.

A summary of the 82595FX's serial interface subsections functions is shown below:

- **Manchester Encoder/Decoder and Clock Recovery**
- **Diagnostic Loopback**
- **Reset-Low-Power Mode**
- **Network Status Indicators**
- **Defeatable Jabber Timer**
- **User Test Modes**

- **Complies with IEEE 802.3 AUI Standard**
  - **Direct Interface to AUI Transformers**
  - **On-Chip AUI Squelch**
- **Complies with IEEE 802.3 10BASE-T for Twisted Pair Ethernet**
  - **Selectable Polarity Detection and Correction**
  - **Direct Interface to TPE Analog Filters**
  - **On-Chip TPE Squelch**
  - **Defeatable Link Integrity for Pre-Standard Networks**
  - **Supports 4 LEDs (Link Integrity, Activity, AUI/BNC DIS and Polarity Correction)**
  - **Auto-Negotiation of Full Duplex Functionality**

10.0 APPLICATION NOTES

This section is intended to provide Ethernet LAN designers with a basic understanding of how the 82595FX is used in a buffered LAN design.

10.1 Bus Interface

The 82595FX Bus Interface unit integrates ISA Bus data transceivers, providing an even more cost efficient and seamless integration than that of the 82595TX. The 82595FX provides the complete control and address interface to the host system bus—implementing a complete ISA bus protocol.

10.2 Local Memory Interface

The 82595FX's local memory interface includes a DMA unit which controls data transfers between the 82595FX and the local memory SRAM. The 82595FX can support up to 64 Kbytes of local SRAM.

The 82595FX provides address decoding and control to allow access to an external Boot EPROM or a FLASH. Addition of a Boot EPROM or FLASH to an ISA solution is optional. The IA is assumed to be stored in the serial EEPROM for the ISA solution.

10.3 EEPROM Interface

The 82595FX provides a complete interface to a serial EEPROM for ISA adapter designs. For ISA motherboard designs, the EEPROM is not required. The EEPROM is used to store configuration information such as Memory and IO Mapping Window, Interrupt line selection, Plug N' Play resource data local bus width, etc. The EEPROM is used to replace jumper blocks which previously contained this type of information.

10.4 Serial Interface

The 82595FX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 10BASE5 interface. The AUI port can also be interfaced to a transceiver device on the adapter to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595FX automatically enables either the AUI or TPE interface, depending on which medium is connected to the chip. This automatic selection can be overridden by software configuration.

10.4.1 AUI CIRCUIT

When used in conjunction with pulse transformers, the 82595FX provides a complete IEEE 802.3 AUI interface. In order to meet the 16V fault tolerance specification of IEEE 802.3, a pulse transformer is recommended. The transformer should be placed between the TRMT, RCV, and CLSN pairs of the 82595FX and the DO, DI, and CI pairs of the AUI (DB-15) connector. The pulse transformer should have the following characteristics:

- 75 μH minimum inductance (100 μH recommended)
- 2000V isolation between the primary and secondary windings
- 2000V isolation between the primaries of separate transformers
- 1:1 Turns ratio

The RCV and CLSN input pairs should each be terminated by 78.7Ω $\pm$1% resistors.

10.4.2 TPE CIRCUIT

The 82595FX provides the line drivers and receivers needed to directly Fabinterface to the TPE analog filter network. The TPE receive section requires a 100Ω termination resistor, a filter section (filter, isolation transformer, and a common mode choke) as described by the 10BASE-T 802.3i-1990 specification.

The TPE transmit section is implemented by connecting the 82595FX's four TPE outputs (TDH, $\overline{\text{TDH}}$, TDL, $\overline{\text{TDL}}$) to a resistor summing network to form the differential output signal. The parallel resistance of R5 and R6 sets the transmitters maximum output voltage, while the difference (R5 − R6)/R5 + R6), is used to reduce the amplitude of the second half of the fat bit (100 ns) to a predetermined level. This predistortion reduces line overcharging, a major source of jitter in the TPE environment. The output of the summing network is then fed into the above mentioned filter and then to the 10BASE-T connector (RJ-45). Analog Front End solutions can be purchased in a single-chip solution from several manufacturers. The solution described in this data sheet uses the Pulse Engineering (PE65434) AFE.

10.4.3 LED CIRCUIT

The 82595FX's internal LED drivers support four LED indicators displaying node status and activity (i.e., Transmit data, receive data, collisions, link integrity, polarity correction, and port (TPE/AUI). To implement the LED indicators, connect the LED driver output to an LED in series with a 510Ω resistor tied to V_{CC}. Each driver can sink up to 10 mA of current with an output impedance of less than 50Ω.

10.5 Layout Guidelines

10.5.1 GENERAL

The analog section, as well as the entire board itself, should conform to good high-frequency practices and standards to minimize switching transients and parasitic interaction between various circuits. To achieve this, follow these guidelines:

Make power supply and ground traces as thick and as short as possible. This will reduce high-frequency cross coupling caused by the inductance of thin traces.

Connect logic and chassis ground together, only at one point on the fab—near the connection to system ground.

You must connect all V_{CC} pins to the same power supply and all V_{SS} pins to the same ground plane. Use separate decoupling per power-supply/ground pin.

Close signal paths to ground as close as possible to their sources to avoid ground loops and noise cross coupling.

10.5.2 CRYSTAL

The crystal should be adjacent to the 82595FX and trace lengths should be as short as possible. the X1 and X2 traces should be as symmetrical as possible.

10.5.3 82595FX ANALOG DIFFERENTIAL SIGNALS

The differential signals from the 82595FX to the transformers, analog front end, and the connectors should be symmetrical for each pair and as short as possible.

The differential signals should also be isolated from the high speed logic signals on the same layer as well as on any sublayers of the PCB.

Group each of the circuits together, but keep them separate from each other. Separate their grounds.

In layout, the circuitry from the connectors to the filter network should have the ground and power planes removed from beneath it. This will prevent ground noise from being induced into the analog front end.

All trace bends should not exceed 45 degrees.

10.5.4 DECOUPLING CONSIDERATIONS

Four 0.1 μF ceramic capacitors should be used. Place one on each side in the center of the I.C. adjacent to the 82595FX. Connect the capacitors directly to the V_{CC} pins and ground planes of the 82595FX.

11.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

11.1 Absolute Maximum Ratings

Case Temperature under Bias .....0°C to +85°C

Storage Temperature .....−65°C to +140°C

All Output and Supply Voltages .....−0.5V to +7V

All Input Voltages .....−1.0V to +6.0V(1)

Further information on the quality and reliability of the 82595FX may be found in the *Components Quality and Reliability Handbook*, Order Number 210997.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 11-1. DC Characteristics (T_C = 0°C to +85°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input LOW Voltage (TTL)	−0.3	+0.8	V	
V_{IH}	Input HIGH Voltage (TTL)	2.0	V_{CC} + 0.3	V	
$V_{IH(JUMPR)}$	Input HIGH Voltage (Jumpers)	3.0	V_{CC} + 0.3	V	
V_{OL1}(2)	Output LOW Voltage		0.45	V	I_{OL} = 17 mA
V_{OL2}(3)	Output LOW Voltage		0.45	V	I_{OL} = 12 mA
V_{OL4}(4)	Output LOW Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −1 mA
V_{OL} (LED)(5)	Output Low Voltage		0.45	V	I_{OL} = 10 mA
V_{OH} (LED)	Output High Voltage	3.9		V	I_{OH} = −500 µA
I_{LP}(6)	Leakage Current		±10	µA	$0 \le V_I \le V_{CC}$
R_{DIFF}(7)	Input Differential-Resistance	10		KΩ	DC
V_{IDF} (TPE)(8)	Input Differential Accept Input Differential Reject	±0.5	±3.1 ±0.3	V_P V_P	5 MHz ≤ f ≤ 10 MHz
R_S (TPE)(9)	Output Source Resistance	5	13	Ω	$\|I_{LOAD}\|$ = 25 mA
V_{IDF} (AUI)(10)	Input Differential Accept Input Differential Reject	±0.3	±1.5 ±0.16	V_P V_P	
V_{ICM} (AUI)(11)	AC Input Common Mode		±0.5 ±0.1	V_P V_P	f ≤ 40 KHz 40 KHz ≤ f ≤ 10 MHz
V_{ODF} (AUI)	Output Differential Voltage	±0.45	±1.2	V	
I_{OSC} (AUI)	AUI Output Short Circuit Current		±150	mA	Short Circuit to V_{CC} or GND
VU (AUI)	Output Differential Undershoot		−100	mV	
V_{ODI} (AUI)(12)	Differential Idle Voltage		40	mV	
I_{CC}	Power Supply Current		90	mA	
I_{CCHWPD} I_{CCSWPD} $I_{CCSLEEP}$	Hardware Power Down Software Power Down Sleep Mode		400 2 35	µA mA mA	
C_{IN}(13)	Input Capacitance		10	pF	@ f = 1 MHz

NOTES:
1. The voltage level for RCV and CLSN pairs are −0.75V to +8.5V.
2. SDx, $\overline{IOCS16}$.
3. IOCHRDY, IRQx.
4. LDATAx, LADDRx, $\overline{LOE}$, $\overline{LWE}$, $\overline{BOOTCS}$, $\overline{SRAMCS}$, EEPROMCS, $\overline{SMOUT}$, TSTCLK, TDO, J1, J2.
5. LILED, ACTLED, POLED and TPE_BNC_$\overline{AUI}$.
6. Pins: ACTLED, LILED, POLED, TPE_BNC_$\overline{AUI}$.
7. RD to $\overline{RD}$, RCV to $\overline{RCV}$ and CLSN to $\overline{CLSN}$.
8. TPE input pins: RD and $\overline{RD}$.
9. TPE output pins: TDH, $\overline{TDH}$, TDL and $\overline{TDL}$, R_S measure V_{CC} or V_{SS} to pin.
10. AUI input pins: RCV and CLSN pairs.
11. AUI output pins: TPMT pair.
12. Measured 8.0 µs after last positive transition of data packet.
13. Characterized, not tested.

11.1.1 PACKAGE THERMAL SPECIFICATIONS

The 82595FX is specified for operation when case temperature is within the range of 0°C to 85°C. The case temperature may be measured in any environment to determine whether the 82595FX is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from the θ_{JA} and the θ_{JC} from the following equations:

$$T_J = T_C + P*\theta_{JC}$$
$$T_A = T_J - P*\theta_{JA}$$
$$T_C = T_A + P*(\theta_{JA} - \theta_{JC})$$

θ_{JA} and θ_{JC} values for the 160 QFP package are as follows:

Thermal Resistance (°C/Watt)

θ_{JC}	θ_{JA} – VS – Airflow ft/min (m/Sec)
	0 (0)
4.9	34.4

11.2 AC Timing Characteristics

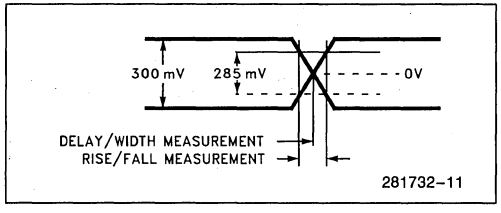


Figure 11-1. Voltage Levels for Differential Input Timing Measurements (RCV and CLSN Pairs)

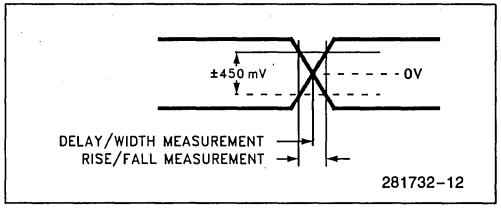


Figure 11-2. Voltage Levels for TDH, TDL, $\overline{TDH}$ and $\overline{TDL}$

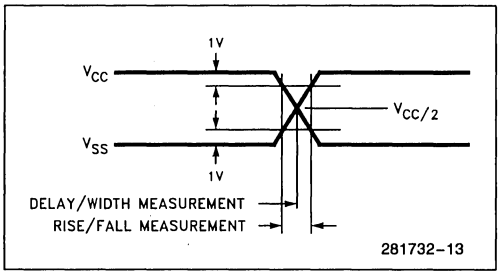


Figure 11-3. Voltage Levels for TRMT Pair Output Timing Measurements

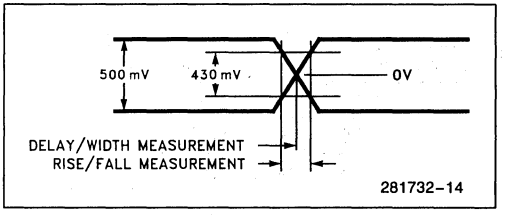


Figure 11-4. Voltage Levels for Differential Input Timing Measurements (RD Pair)

11.3 AC Measurement Conditions

1. T_C = 0°C to +85°C, V_{CC} = 5V ±5%
2. The signal levels are referred to in Figures 1, 2, 3 and 4.
3. AC Loads:
   a) AUI Differential: a 10 pF total capacitance from each terminal to ground and a load resistor of 78Ω ±1% in parallel with a 27 μH ±5% inductor between terminals.
   b) TPE: 20 pF total capacitance to ground.

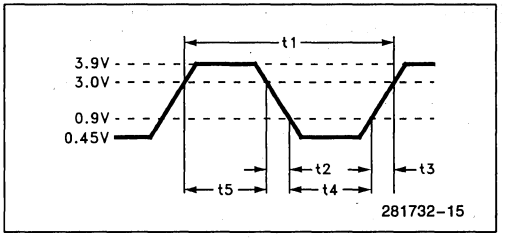


Figure 11-5. X1 Input Voltage Levels for Timing Measurements

Table 11-2. Clock Timing

Symbol	Parameter	Min	Max	Unit
t1	X1 Cycle Time	49.995	50.005	ns
t2	X1 Fall Time		5	ns
t3	X1 Rise Time		5	ns
t4	X1 Low Time	15		ns
t5	X1 High Time	15		ns

11.4 ISA Interface Timing

Table 11-3. 16-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1a	AEN Valid to I/O Command Active	100		ns	
T2a	AEN Valid from I/O Command Inactive	30		ns	
T3a	SA to CMD Active	63		ns	
T4a	SA Valid Hold from CMD Inactive	42		ns	
T5a	Valid SA to $\overline{\text{IOCS16}}$ Active		100	ns	
T6a	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T7a	CMD Active to Inactive	125		ns	
T8a	CMD Inactive to Active	92		ns	*Before* I/O Command
T9a	Active CMD to Valid IOCHRDY		30	ns	Applies to Ready Cycles
T10a	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T11a	DATA Driven from READ CMD Active	0		ns	
T12a	Valid READ Data from CMD Active		64	ns	Applies to Standard Cycles Only
T13a	Valid READ Data from IOCHRDY Active		52	ns	Applies to Ready Cycles Only
T14a	READ Data Hold from CMD Inactive	0		ns	
T15a	READ CMD Inactive to Data Tristate		30	ns	
T16a	CMD to WRITE Data Active		62	ns	
T17a	WRITE Data Hold from CMD Inactive	15		ns	
T18a	WRITE CMD Inactive to Data Tristate		30	ns	

Table 11-4. 8-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1b	AEN Valid to I/O Command Active	100		ns	
T2b	AEN Valid from I/O Command Inactive	30		ns	
T3b	SA to CMD Active	63		ns	
T4b	SA Valid Hold from CMD Inactive	42		ns	
T5b	Valid SA to $\overline{\text{IOCS16}}$ Inactive		100	ns	
T6b	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T7b	CMD Active to Inactive	125		ns	
T8b	CMD Inactive to Active	92		ns	*Before* I/O Command
T9b	Active CMD to Valid IOCHRDY		226	ns	Applies to Ready Cycles
T10b	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T11b	DATA Driven from READ CMD Active	0		ns	
T12b	Valid READ Data from CMD Active		64	ns	Applies to Standard Cycles
T13b	Valid READ Data from IOCHRDY Active		52	ns	Applies to Ready Cycles Only
T14b	READ Data Hold from CMD Inactive	0		ns	
T15b	READ CMD Inactive to Data Tristate		30	ns	
T16b	CMD to WRITE Data Active		62	ns	
T17b	WRITE Data Hold from CMD Inactive	15		ns	
T18b	WRITE CMD Inactive to Data Tristate			ns	

Table 11-5. 8-Bit Memory Access

Parameter	Description	Min	Max	Units	Comments
T1c	AEN Valid to Command Active	100		ns	
T2c	AEN Valid from Command Inactive	30		ns	
T3c	SA to CMD Active	63		ns	
T4c	SA Valid Hold from CMD Inactive	42		ns	
T5c	CMD Active to Inactive	125		ns	
T6c	CMD Inactive to Active	60		ns	*Before* Memory Command
T7c	Active CMD to Valid IOCHRDY		226	ns	Applies to Ready Cycles
T8c	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T9c	DATA Driven from READ CMD Active	0		ns	
T10c	Valid READ Data from IOCHRDY Active		52	ns	
T11c	READ Data Hold from CMD Inactive	0		ns	
T12c	READ CMD Inactive to Data Tristate		30	ns	
T13c	CMD to WRITE Data Active		62	ns	
T14c	WRITE CMD Inactive to Data Tristate		30	ns	

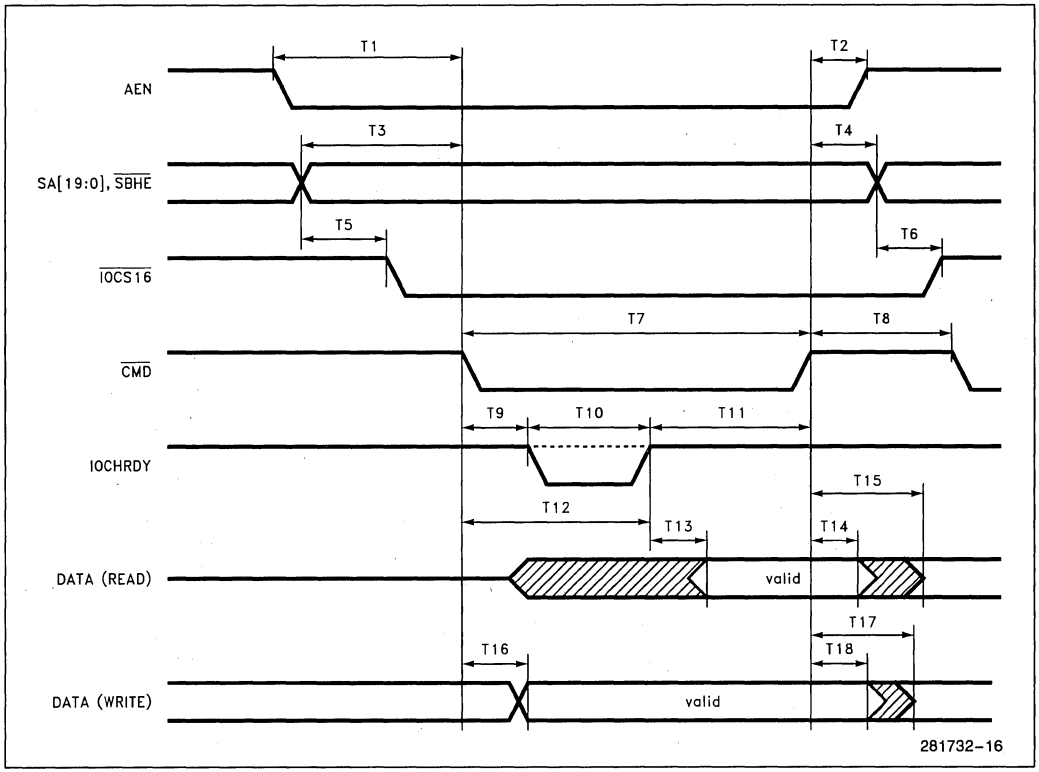


Figure 11-6. ISA Read/Write Cycle

11.6 Local Memory Timings

11.6.1 SRAM TIMINGS

- The 82595FX any SRAM up to 25 ns access time.
- SRAM type supported are 4K, 8K, 16K, 32K, 64K x 8.

Table 11-6. 82595FX SRAM—AC Characteristics

Parameter	Description	Min	Max	Units	Comments
T1w	LADDR Valid to $\overline{\text{SRAMCS}}$ Active	0		ns	
T2w	LADDR Valid to $\overline{\text{LWE}}$ Active	0		ns	
T3w	$\overline{\text{SRAMCS}}$ Active Time	25		ns	
T4w	$\overline{\text{LWE}}$ Active Time	25		ns	
T5w	Data Valid to $\overline{\text{SRAMCS}}$ Inactive	15		ns	
T6w	Data Valid to $\overline{\text{LWE}}$ Inactive	15		ns	
T7w	$\overline{\text{SRAMCS}}$ Inactive to Data Invalid	0		ns	
T8w	$\overline{\text{LWE}}$ Inactive to Data Invalid	0		ns	
T9w	$\overline{\text{SRAMCS}}$ Inactive to LADDR Invalid	0		ns	
T10w	$\overline{\text{LWE}}$ Inactive to $\overline{\text{LADDR}}$ Invalid	0		ns	
T1r	LADDR Valid to $\overline{\text{SRAMCS}}$ Active	0		ns	
T2r	LADDR Valid to $\overline{\text{LOE}}$ Active	0		ns	
T3r	$\overline{\text{SRAMCS}}$ Active Time	25		ns	
T4r	$\overline{\text{LOE}}$ Active Time	25		ns	
T5r	Data Valid to $\overline{\text{SRAMCS}}$ Active		25	ns	
T6r	Data Valid to $\overline{\text{LOE}}$ Inactive		25	ns	
T7r	Data Read Hold Time from $\overline{\text{SRAMCS}}$ Inactive	0	25	ns	
T8r	Read Data Hold Time from $\overline{\text{LOE}}$ Inactive	0	25	ns	

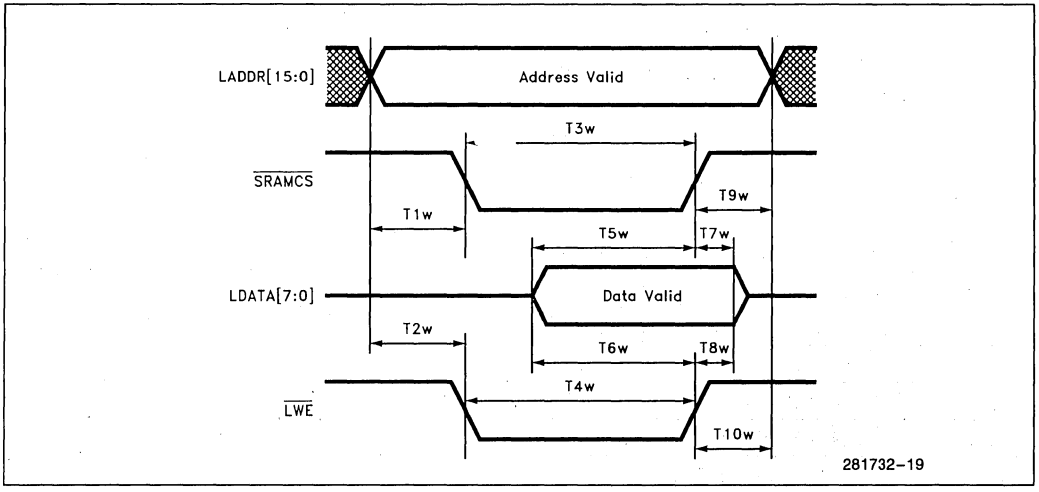


Figure 11-7. SRAM Timings—Write Cycle

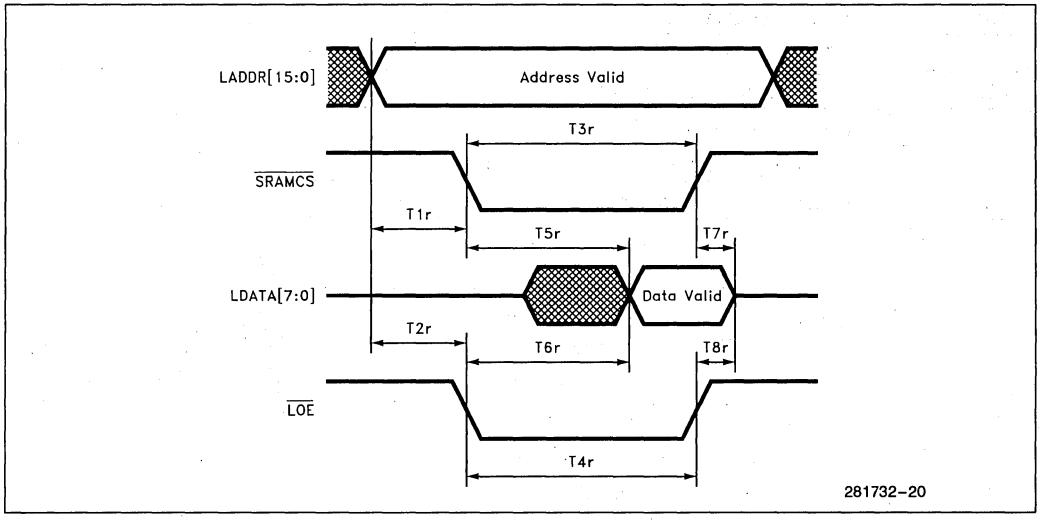


Figure 11-8. SRAM Timings—Read Cycle

11.6.2 FLASH/EPROM TIMINGS

- The 82595FX is designed to support a FLASH or EPROM up to 200 ns access time.
- Flash/EPROM types supported are 16K, 32K, 64K, 128K, 256K, 512K, 1024K x 8.

Table 11-7. FLASH—AC Characteristics

Parameter	Description	Min	Max	Units	Comments
T1w	LADDR Setup Time to $\overline{LWE}$ Active	0		ns	
T2w	LADDR Hold Time from $\overline{LWE}$ Active	75		ns	
T3w	$\overline{LWE}$ Active Time	60		ns	
T4w	$\overline{BOOTCS}$ Setup Time before $\overline{LWE}$ Active	20		ns	
T5w	$\overline{BOOTCS}$ Hold Time from $\overline{LWE}$ Inactive	0		ns	
T6w	Data Setup Time before $\overline{LWE}$ Inactive	50		ns	
T7w	Data Hold Time from $\overline{LWE}$ Inactive	10		ns	
T1r	LADDR Setup Time to $\overline{BOOTCS}$ Active	0		ns	
T2r	LADDR Setup Time to $\overline{LOE}$	0		ns	
T3r	$\overline{BOOTCS}$ Active Time	225		ns	
T4r	$\overline{LOE}$ Active Time	225		ns	
T5r	$\overline{BOOTCS}$ Active to Data Valid		200	ns	
T6r	$\overline{LOE}$ Active to Data Valid		200	ns	
T7r	Data Hold Time from $\overline{BOOTCS}$ Inactive	0	40	ns	
T8r	Data Hold Time from $\overline{LOE}$ Inactive	0	40	ns	

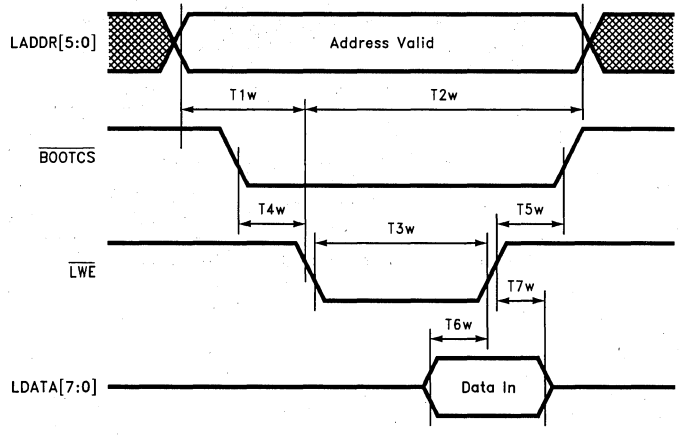


Figure 11-10. FLASH Timings—Write Cycle

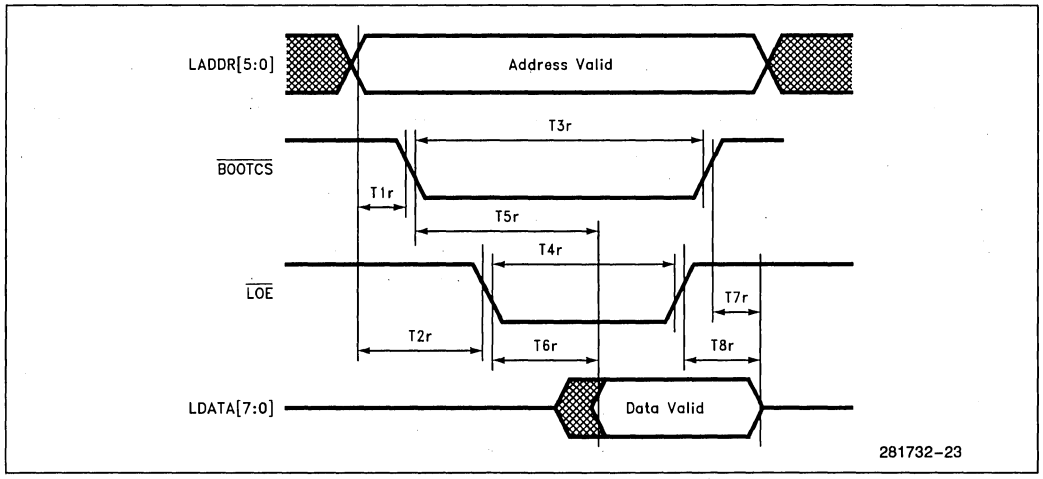


Figure 11-11. Flash Timings—Read Cycle

Table 11-8. EEPROM AC Characteristics

Parameter	Description	Min	Max	Units	Comments
T1(css)	CS Setup Time	1.0		μs	
T2(skh)	SK High Time	3.0		μs	
T3(skl)	SK Low Time	3.0		μs	
T4(csh)	CS Hold Time	0		μs	
T5(cs)	CS Low Time	1.0		μs	
T6(dis)	DI Setup Time	0.4		μs	
T7(dih)	DI Hold Time	0.4		μs	
T8(do)	DO Valid Time		0.4	μs	EEPROM Restriction
T9(df)	CS Inactive to DO Floating		0.4	μs	EEPROM Restriction

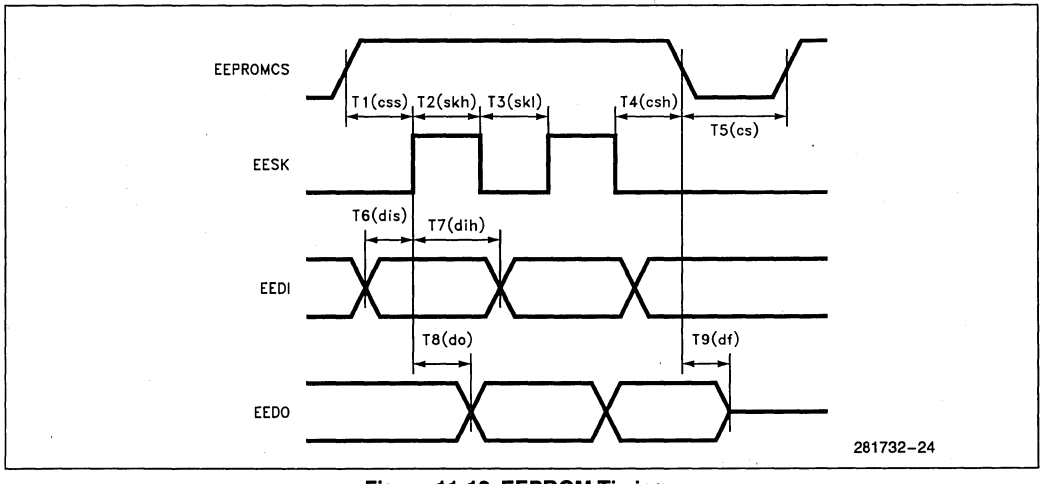


Figure 11-12. EEPROM Timings

11.7 Interrupt Timing

Table 11-9. Interrupt Timing

Parameter	Description	Min	Max	Units	Notes
T177	Interrupt Ack $\overline{CMD}$ Inactive to IRQ[0–7] Inactive		500	ns	
T178	IRQ[0–7] Inactive to IRQ[0–7] Active	100		ns	
T179	Tri-state $\overline{CMD}$ Inactive to IRQ[0–7] Tri-State		500	ns	

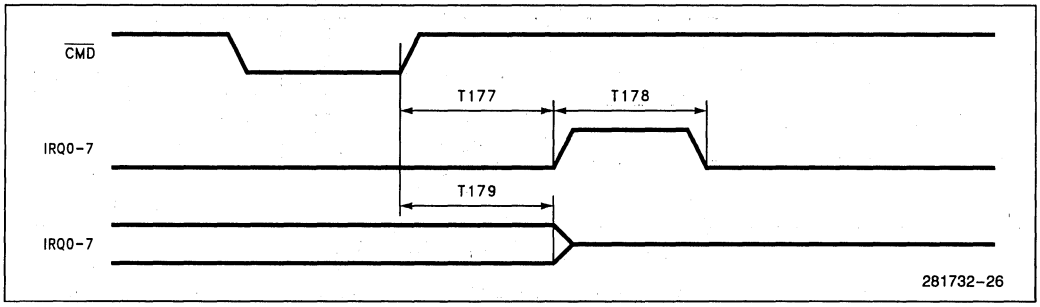


Figure 11-13. Interrupt Timing

11.8 RESET and $\overline{\text{SMOUT}}$ Timing

General Comments

- Both signals are asynchronous signals and have minimum pulse duration specification only.
- $\overline{\text{SMOUT}}$ during Hardware power down activation.

Table 11-10. RESET and $\overline{\text{SMOUT}}$ Timing

Parameter	Description	Min	Max	Units	Notes
T180	RESET Minimum Duration	32		ms	1
T181	$\overline{\text{SMOUT}}$ Minimum Duration	100		ns	2
T182	$\overline{\text{SMOUT}}$ Activation by Power Down Command	150		ns	3
T183	$\overline{\text{SMOUT}}$ Deactivation	25		ns	3

NOTES:
1. Noise spikes of maximum TBD ns are allowed on Reset.
2. $\overline{\text{SMOUT}}$ is input.
3. $\overline{\text{SMOUT}}$ is output after configuration.

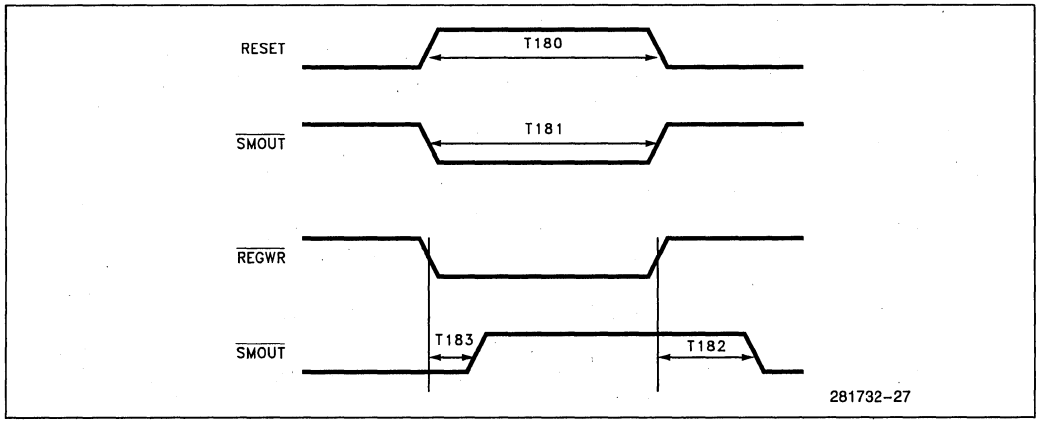


Figure 11-14. $\overline{\text{SMOUT}}$ Timing

11.9 JTAG Timing

Table 11-11. 82595FX JTAG Timing

Symbol	Parameter	Min	Max	Unit	Notes
T184	TMS Set-Up Time	30		ns	
T185	TMS Hold Time	30		ns	
T186	TDI Set-Up Time	30		ns	
T187	TDI Hold Time	30		ns	
T188	Input Signals Set-Up Time	30		ns	
T189	Input Signals Hold Time	30		ns	
T190	Outputs Valid Delay		200	ns	
T191	TDO Valid Delay		40	ns	
T192	TCK Cycle Time (Period)	100		ns	50% Duty Cycle

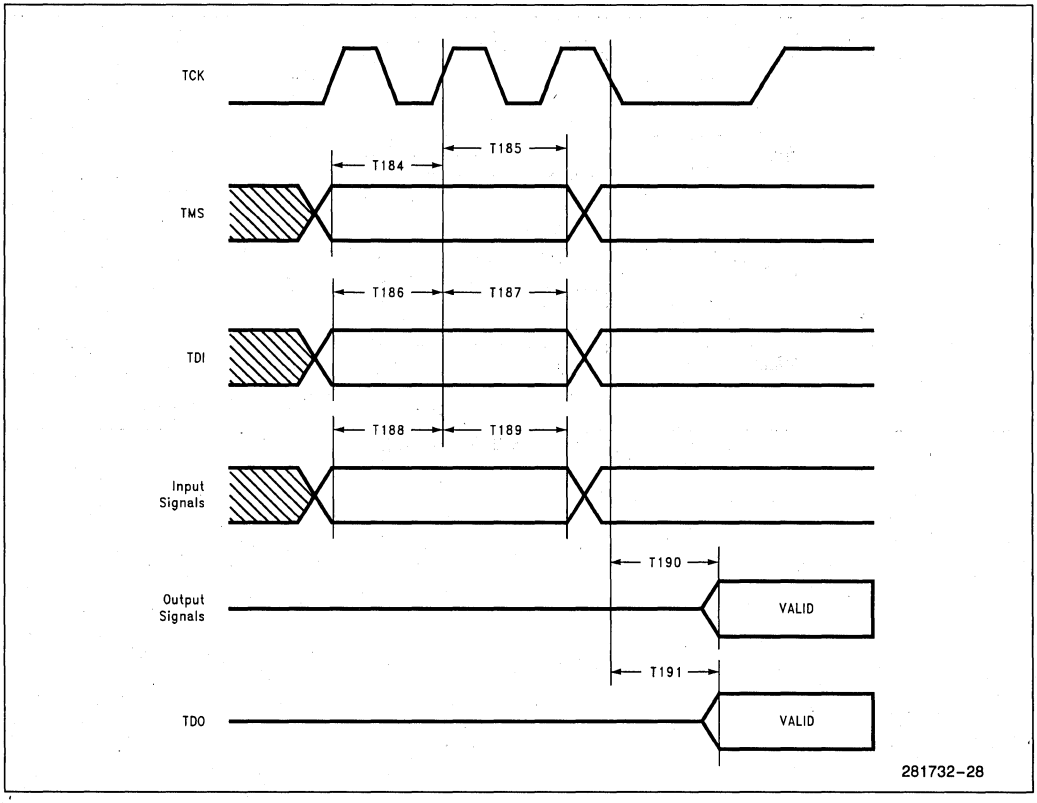
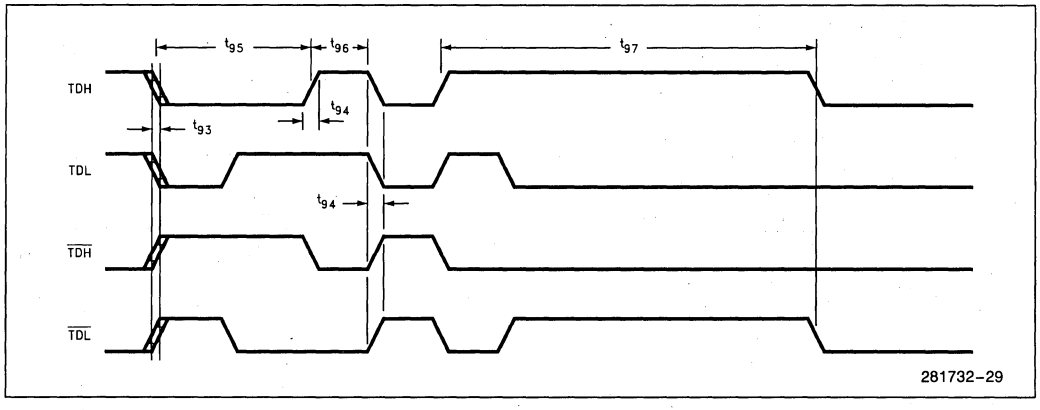


Figure 11-15. 82595FX JTAG Timing

11.10 Serial Timings

Table 11-12. TPE Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{90}	Number of TxD Bit Loss at Start of Packet			2	bits
t_{91}	Internal Steady State Propagation Delay			400	ns
t_{92}	Internal Start UP Delay			600	ns
t_{93}	TDH and TDL Pairs Edge Skew (@ $V_{CC}/2$)		1.5	3	ns
t_{94}	TDH and TDL Pairs Rise/Fall Times (@ 0.5V to V_{CC} − 0.5V)		2	5	ns
t_{95}	TDH and TDL Pairs Bit Cell Center to Center	99	100	101	ns
t_{96}	TDH and TDL Pairs Bit Cell Center to Boundary	49	50	51	ns
t_{97}	TDH and TDL Pairs Return to Zero from Last TDH	250		400	ns
t_{98}	Link Test Pulse Width	98	100	100	ns
t_{99}	Last TD Activity to Link Test Pulse	8	13	24	ms
t_{100}	Link Test Pulse to Data Separation	190	200		ns



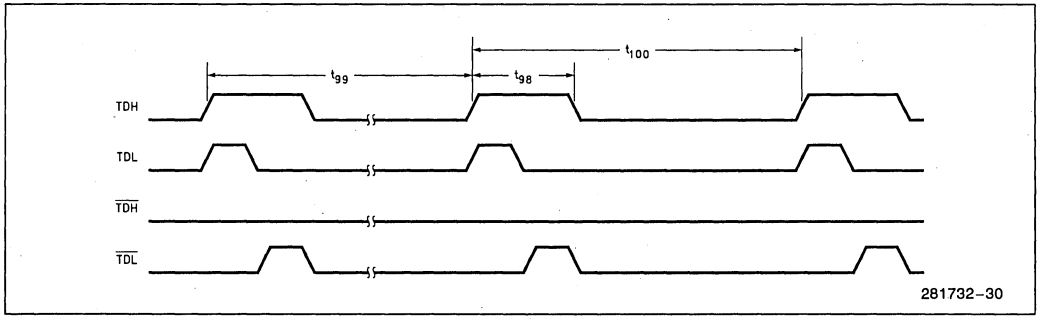


Figure 11-16. TPE Transmit Timings (Link Test Pulse)

Table 11-13. TPE Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{105}	RD to RxD Bit Loss at Start of Packet	4		19	bits
t_{106}	RD Invalid Bits Allowed at Start of Packet			1	bits
t_{107}	RD to Internal Steady State Propagation Delay			400	ns
t_{108}	RD to Internal Start Up Delay			2.4	μs
t_{109}	RD Pair Bit Cell Center Jitter			±13.5	ns
t_{110}	RD Pair Bit Cell Boundry Jitter			±13.5	ns
t_{111}	RD Pair Held High from Last Valid Position Transition	230		400	ns

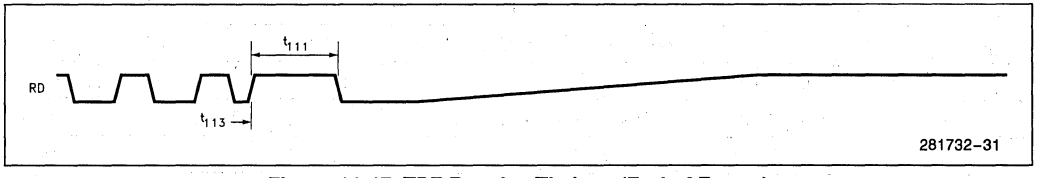


Figure 11-17. TPE Receive Timings (End of Frame)

Table 11-14. TPE Link Integrity Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{120}	Last RD Activity to Link Fault (Link Loss Timer)	50	100	150	ms
t_{121}	Minimum Received Linkbeat Separation(1)	2	5	7	ms
t_{122}	Maximum Received Linkbeat Separation(2)	25	50	150	ms

NOTES:
1. Linkbeats closer in time to this value are considered noise and rejected.
2. Linkbeats further apart in time than this value are not considered consecutive and are rejected.

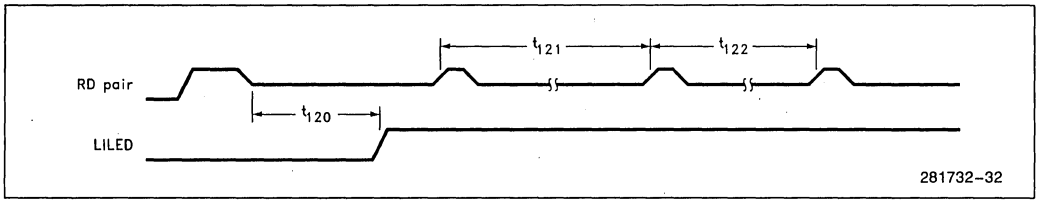


Figure 11-18. TPE Link Integrity Timings

Table 11-15. AUI Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{126}	TRMT Pair Rise/Fall Times		3	5	ns
t_{127}	Bit Cell Center to Bit Cell Center of TRMT Pair	99.5	50	100.5	ns
t_{128}	Bit Cell Center to Bit Cell Boundary of TRMT Pair	49.5	50	50.5	ns
t_{129}	TRMT Pair Held at Positive Differential at Start of Idle	200			ns
t_{130}	TRTM Pair Return to ≤40 mVp from Last Positive Transition			8.0	μs

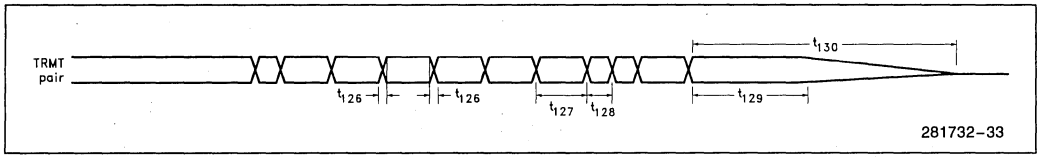


Figure 11-19. AUI Transmit Timings

Table 11-16. AUI Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{135}	RCV Pair Rise/Fall Times			10	ns
t_{136}	RCV Pair Bit Cell Center Jitter in Preamble			±12	ns
t_{137}	RCV Pair Bit Cell Center/Boundary Jitter in Data			±18	ns
t_{138}	RCV Pair Idle Time after Transmission	8			μs
t_{139}	RCV Pair Return to Zero from Last Positive Transition	160			ns

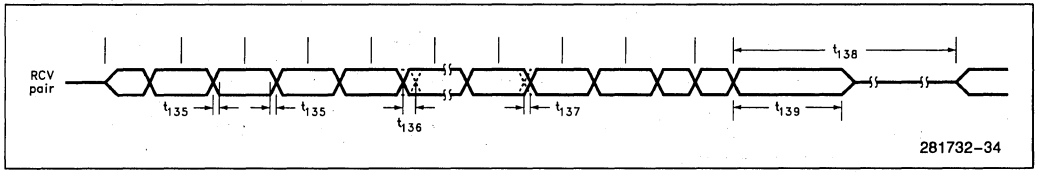


Figure 11-20. AUI Receive Timings

Table 11-17. AUI Collision Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{145}	CLSN Pair Cycle Time	80		118	ns
t_{146}	CLSN Pair Rise/Fall Times			10	ns
t_{147}	CLSN Pair Return to Zero from Last Positive Transition	160			ns
t_{148}	CLSN Pair High/Low Times	35		70	ns

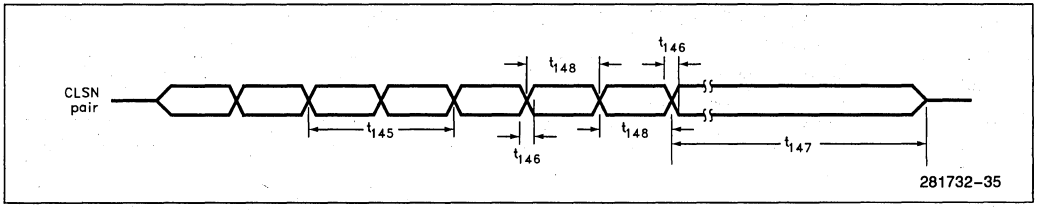


Figure 11-21. AUI Collision Timings

Table 11-18. AUI Noise Filter Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{152}	RCV Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns
t_{153}	CLSN Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns

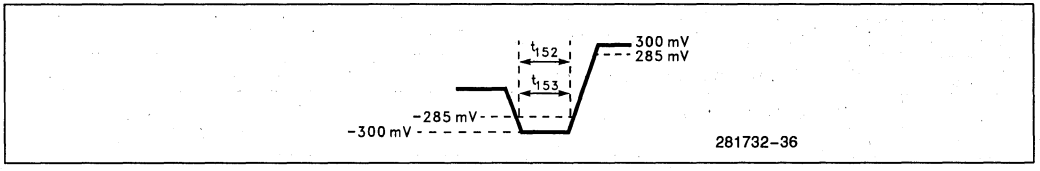


Figure 11-22. AUI Noise Filter Timings

Table 11-19. Jabber Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{165}	Maximum Length Transmission before Jabber Fault (TPE)	20	25	150	ms
t_{166}	Maximum Length Transmission before Jabber Fault (AUI)	10	13	18	ms
t_{167}	Minimum Idle Time to Clear Jabber Function	250	275	750	ms

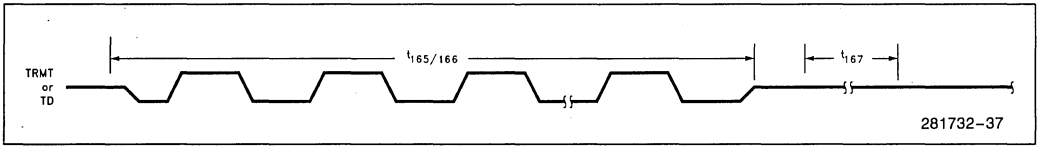


Figure 11-23. Jabber Timings

Table 11-20. LED Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{170}	ACTLED On Time	50		450	ms
t_{171}	ACTLED Off Time	50			ms
t_{172}	LILED On Time	50			ms
t_{173}	LILED Off Time	100			ms

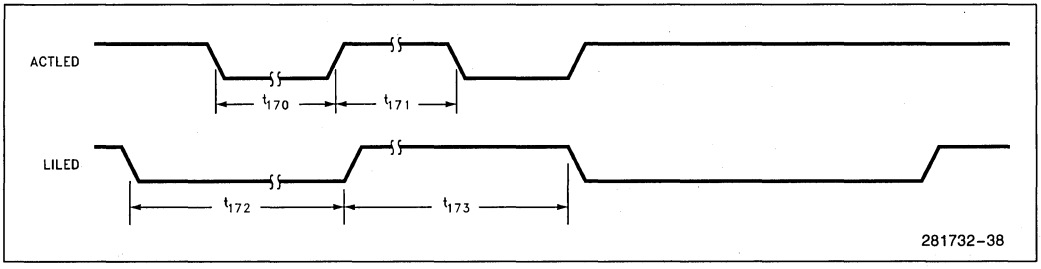


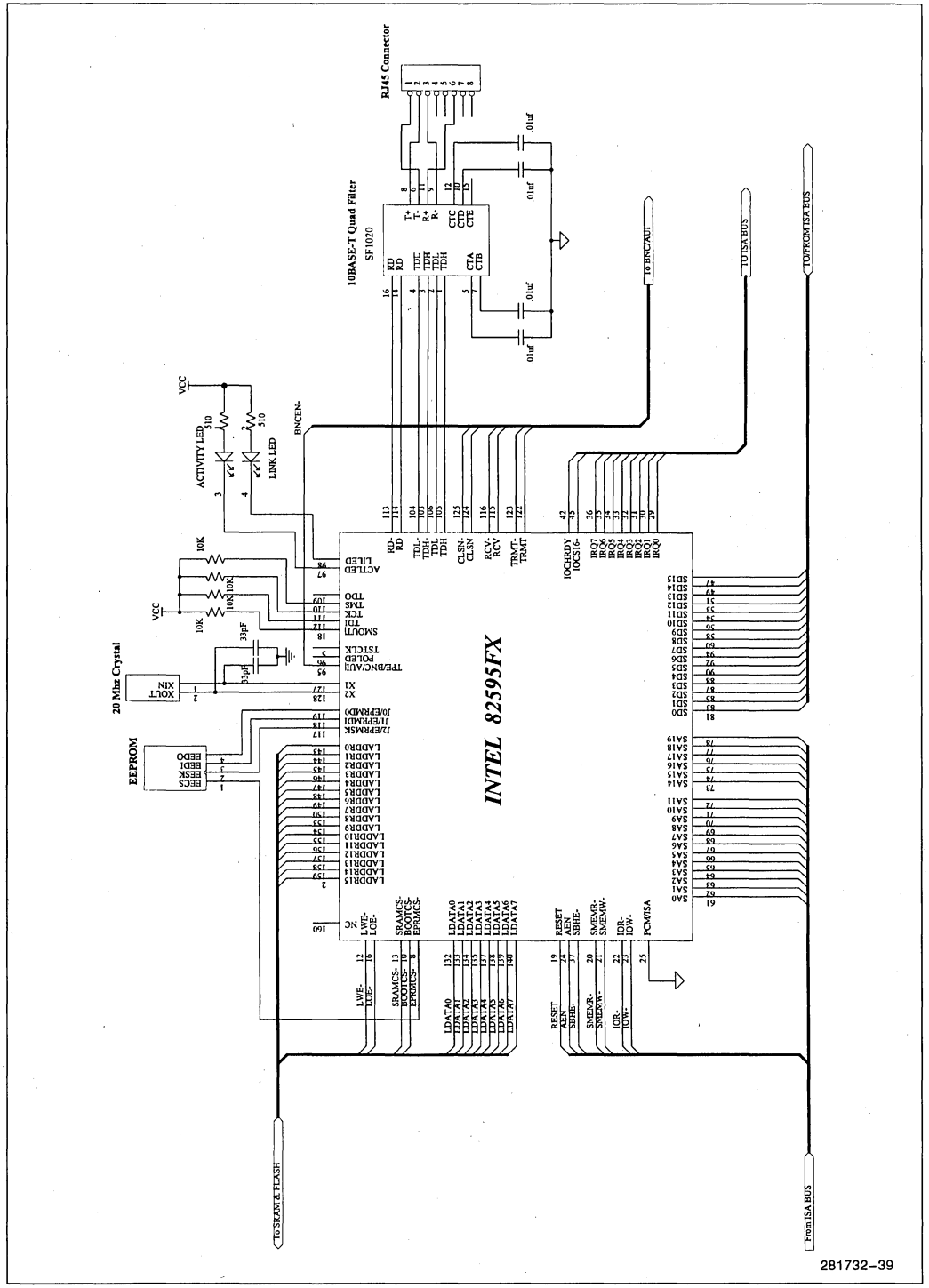
Figure 11-24. LED Timings

Additional 82595FX Documentation

This datasheet provides complete pinout and pin definitions, and electrical specifications and timings. It also includes an overview of the various subsections listed in Figure 1. For more complete information on the 82595FX, please ask your local sales representative for the 82595FX User's Guide. The 82595FX User's Guide contains detailed information on the 82595FX feature set, including register descriptions and implementation steps for various 82595FX functions (initialization, transmission, reception).

Design Example

The schematic on the next page shows a typical 82595FX design.


INTEL 82595FX
RJ45 Connector
10BASE-T Quad Filter
SF1020
20 Mhz Crystal
EEPROM
ACTIVITY LED
LINK LED
VCC
BNCEN-
TO BNC/AUI
TO ISA BUS
TO/FROM ISA BUS
To SRAM & FLASH
From ISA BUS
281732-39

intel®

AP-368

APPLICATION NOTE

82557 10/100 Mbps PCI LAN Controller A Guide to 82596 Compatibility

Technical Marketing
Network Products Division

November 1995

PRELIMINARY

Order Number: 644126-001

82557 10/100 Mbps PCI LAN CONTROLLER
A GUIDE TO 82596 COMPATIBILITY

CONTENTS

CONTENTS

1.0 INTRODUCTION

Over the last few years, the networking environment has evolved to account for the needs of high-bandwidth. Fast Ethernet,* otherwise known as IEEE 100BASE-T, is a technology derived from 10BASE-T Ethernet and was designed to address many of the performance bottlenecks associated with classic 10 Mbit Ethernet networks. Intel's Fast Ethernet component product solution includes the 82557 and 82553 components.

This application note provides information on the differences between the Intel 82596 and the Intel 82557 next generation family of LAN controllers. It explains 82596 to 82557 compatibility for Ethernet designers. The application note can help designers transition from an existing 82596 LAN solution to an 82557 solution.

For further information on the 82557, refer to the *82557 Data Sheet* and the *82557 User's Manual,* available from an Intel Sales Representative.

2.0 THE 82557 LAN CONTROLLER

The 82557 is Intel's first highly-integrated 32-bit PCI LAN controller for 10 or 100 Mbps Fast Ethernet networks. The 82557 offers a high performance LAN solution while maintaining low-cost through its high-integration. It contains a high-performance 32-bit PCI Bus Master interface to fully use the high bandwidth available (up to 132 Mbytes per second) to masters on the PCI bus. The 82557 is optimized to support twisted pair Ethernet, the required wiring media for 100BASE-T.

The 82557 contains a number of high-performance networking features that off-load time-critical tasks from the CPU. Its bus master architecture can eliminate the "intermediate copy" step in Receive (RCV) and Transmit (XMT) frame copies, resulting in faster processing of these frames. It maintains a similar memory structure to the Intel 82596 LAN Coprocessor, however, these memory structures have been streamlined for better Network Operating System (NOS) interaction and improved performance.

The 82557 contains two separate RCV and XMT FIFOs, preventing data overruns or underruns while waiting for access to the PCI bus. The FIFOs also enable back to back frame transmission within the minimum inter-frame spacing. Full support for up to 1 Mbyte of FLASH provides remote Boot capability (a BIOS extension stored in the FLASH which could allow a node to boot itself off of a network drive). For 100 Mbps applications the 82557 contains an IEEE MII compliant interface to the Intel 82553 physical interface device (or other MII compliant PHY) which provides a complete LAN solution for 100/10 Mbps networks. For 10 Mbps networks, the 82557 can be interfaced to a standard ENDEC interface (such as the Intel 82503 Serial Interface component), while maintaining software compatibility to 100 Mbps solutions.

The 82557 was designed to implement cost-effective, high-performance PCI add-in adapters, or it can also be used directly on a PC motherboard designs. Its combination of high integration and low cost make it ideal for either application.

82557 Feature Summary

- Glueless 32-bit PCI bus master interface (direct drive of bus)—compatible to PCI spec Rev 2.1
- 82596-like chained memory structure
- Improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- Built-in FLASH interface with addressing up to 1 MByte
- On-chip receive and transmit FIFOs
- On-chip counters for network management
- Support for back to back transmit interframe spacing (IFS)
- Built in EEPROM interface
- Support for both 10 Mbps and 100 Mbps networks
- Interface to MII-compliant physical interface such as the Intel 82553 Serial Component for 10/100 Mbps designs—IEEE 802.3 100BASE-T compatible
- Interface to Intel 82503 for 10 Mbps designs—IEEE 802.3 10BASE-T compatible
- Autodetect and autoswitching for 10 or 100 Mbps network speeds
- Full duplex capable at 10 and 100 Mbps
- 160 Lead QFP package

3.0 FEATURE CHANGES IN THE 82557

The 82557 is a follow-on to the 82596 LAN controller. Intel made a number of changes and enhancements in the 82557 to increase performance while being cost sensitive. The following table highlights key functional and physical changes between the 82557 and 82596:

Feature	82557	82596
Maximum Serial Speed	10 or 100 Mbps	10 Mbps
MII	Yes	No
Bus Interface	32-Bit PCI	32-Bit Local Bus
Bus Bandwidth	132 Mbytes/ Sec. @33 MHz	106 Mbytes/ Sec. @33 MHz
Architecture	Master	Master
Shared Memory Structures	CSR, CBL, RFA	Initialization Root, SCB, CBL, RFA
Transmit/ Receive Structures	Simplified, Flexible	82586, Simplified, Flexible
Memory Addressing	32-Bit Enhanced Linear	82586, 32-Bit Segmented, Linear
FIFO	3K RX, 3K TX	128 Byte RX, 64 Byte TX
Byte Ordering	Little Endian	Little, Big Endian
FLASH Interface	Yes (1 M)	No
Package	160-Pin PQFP	132-Pin PQFP, PGA
Pin Compatible	No	No
Bursting	256 Dword	4 Dword

4.0 FUNCTIONAL CHANGES BETWEEN THE 82557 AND 82596

This section lists primary functional changes between the 82557 and the 82596. Some are functional enhancements, others are deletions of the 82596 functionality.

4.1 New Enhancements in the 82557

- FIFO size: the 82557 includes independent on-chip Transmit and Receive FIFOs (3 Kbytes each); the 82596 includes 64 byte transmit and 128 byte receive on-chip FIFOs.
- General chip control structure changes: in the 82557, an on-chip CSR structure incorporates SCB, Flash/EEPROM and MDI registers. In the 82596, the shared memory SCB, ISCP, and SCP structures were used for general chip control.
- Operational speed flexibility: the 82557 supports either 10 or 100 Mbit operation. The 82596 supports a 10 Mbit operation only (ignoring full duplex functionality in both).
- Reset functionality: the 82557 includes a selective reset command which specifically resets CU and RU without affecting the overall device configuration. The 82596 includes the CU_ABORT command which terminates the current CU activity and returns the CU to a known (Idle) state.
- DMA resource tuning: in the 82557, Tx and Rx DMA preempt counts allow direct manipulation of DMA resources to reflect design biases towards either transmit or receive functions. The 82596 has a fixed priority scheme for managing DMA resources.
- Statistical counters: the 82557 contains 16 on-chip statistical counters that are automatically updated with each transmit/receive command. The 82596 TCB stores statistical data which must be compiled by the driver for each TCB before continuing to the next command.
- MII: the 82557 supports MII interface compatibility (includes MII specific control and data signals and MDI register). The 82596 includes a generic ENDEC serial interface.
- PCI: the 82557 includes a full 32-bit PCI standard interface. The 82596 includes a 32-bit local bus interface.
- Bus throughput: the 82557 allows a 132 Mbyte maximum parallel (PCI) bandwidth at 33 MHz. The 82596 allows a 106 Mbyte maximum parallel bandwidth at 33 MHz.
- Flash capable: the 82557 allows for a flash memory interface (control and addressing up to 1 Mbyte). The 82596 does not allow for designs requiring flash memory devices.
- Full duplex: the 82557 is truly Full duplex capable using FDX and FULHAL pins for controlling full duplex functionality. The 82596 implements a limited full duplex capability.

- Adaptive IFS: the 82557 supports an adaptive IFS algorithm which maximizes network throughput. The 82596 includes a tunable IFS parameter for manually adjusting IFS.
- Bursting: the 82557 allows bursting of 256 Dword lengths. The 82596 allows bursting of 4 Dword length.
- Early Transmit Completion Status: the 82557 reports a completion of a transmit command as soon as the frame is copied from memory so that the driver can reuse resources to prepare a new transmit command.
- Transmit threshold: the 82557 incorporates a transmit threshold parameter which allows adjustment to the FIFO level at which the Transmit process begins. The 82596 begins the Transmit process as soon as the first Dword reaches the bottom of the transmit FIFO.
- Addressing modes: the 82557 uses an enhanced linear addressing mode for all operations. The 82596 uses either linear or 32-bit segmented (82586) addressing modes.

4.2 Functions in the 82596 not Supported by the 82557

- Byte Ordering: the 82557 supports Little Endian mode only (no Big Endian mode).
- Addressing: the 82557 has no 82586 compatible addressing modes.
- Adjustable frame length: the 82557 has no Minimum Frame Length variable (82557 has a default minimum frame length of 64 bytes).
- Monitor mode: the 82557 has no monitoring mode for evaluating incoming frames.
- Adjustable slot time: the 82557 has no support for an adjustable slot time parameter.
- Control structures: the 82557 does not include SCP, SCB or ISCP shared memory structures (on-chip CSR replaces SCB).
- CRC: CRC flexibility is not supported in the 82557 (No CRC and CRC-16/CRC-32 options are not present).

5.0 SOFTWARE INTERFACE COMPARISONS

Both the 82557 and 82596 use a shared memory communication system with the CPU. However, the 82557 uses only three parts that comprise the shared memory structure: *Control/Status Registers (CSR), Command Block List (CBL),* and the *Receive Frame Area (RFA).* The 82596 memory structure is divided into four parts: the *Initialization Root,* the *System Control Block,* the *Command Block List,* and the *Receive Frame Area.*

One of the main differences in the 82557 and 82596 memory structures is the 82557 System Control block (SCB) residing on-chip (accessed by either I/O or memory cycles) as part of the Control Status Register (CSR). In the 82596, the channel attention signal is used by the 82596 to access the System Configuration Pointer (SCP) and the Intermediate System Configuration Pointer (ISCP). The ISCP then points to the SCB (see Figure 2). However, the SCB serves the same purpose in both the 82596 and 82557. It is a central communication point for exchanging control and status information between the CPU and the 82557. The CPU controls the state of the Command Unit (CU) and Receive Unit (RU) (e.g. Active, Suspended or Idle) by writing commands to the SCB. The 82557 and 82596 updates the SCB Status Word to provide status.

5.1 The 82557 Control Status Register (CSR)

The 82557 CSR registers, MDI, Flash, PORT, MDI Control, and General Pointer allow the CPU to read to and from an EEPROM, FLASH, Management Data Interface (in the case of MDI, Flash, and MDI Control). They also point to various data structures in memory, reset the 82557, etc. (for General Pointer and PORT, respectively). In contrast, the 82596 does not include FLASH or MDI in its SCB; it uses RFA Offset/CBL Offset, as opposed to the 82557 General Pointer. The 82596 also uses T-ON and T-OFF parameters in its SCB, which the 82557 does not use. Additionally, the 82596 uses the PORT# pin to allow the CPU to directly access it for certain function, as opposed to the 82557, which has a PORT register within its SCB.

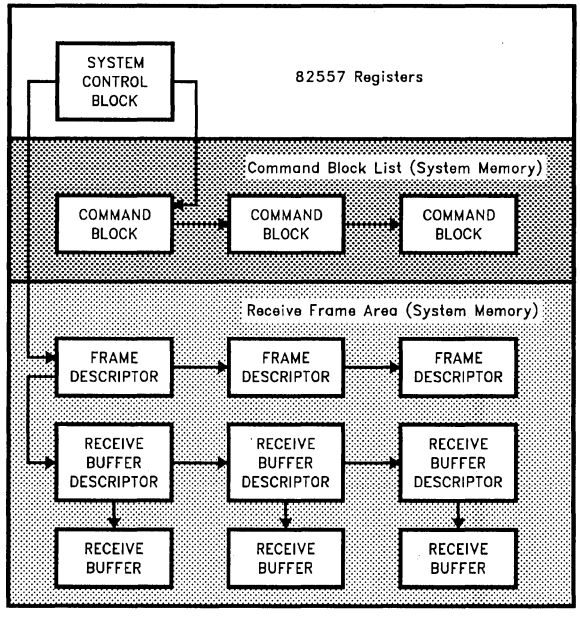


Figure 1. 82557 Shared Memory Structure

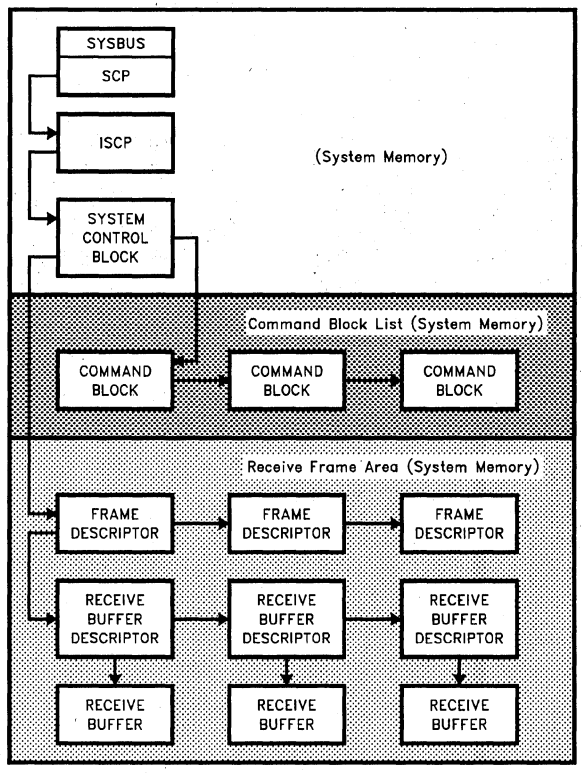


Figure 2. 82596 Shared Memory Structure

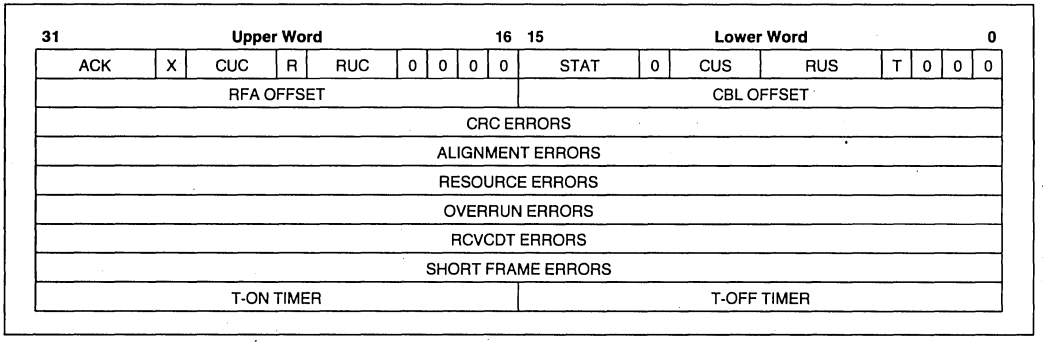


Figure 3. 82596 System Control Block

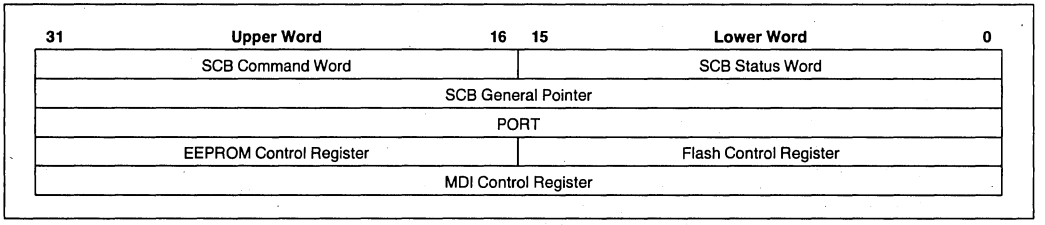


Figure 4. 82557 Control Status Register

The 82557 Command Block List (linked list of individual action commands) and Receive Frame Area (list of free frame descriptors and data buffers) are very similar to those of the 82596. Transmit commands can be programmed in either Simplified or Flexible memory modes. The Receive Frame Area consists of Receive Frame Descriptors (RFDs) and Receive Buffer Descriptors (RBDs). The 82596 RFD can be one two types: Simplified or Flexible. For the 82557, its RFD can be one of three types: Simplified, Flexible, or Header.

Detailed memory structure differences are highlighted in Sections 5.2 through 5.7.

5.2 SCB Command Comparisons

Type of Command	82557		82596	
	Op Code	Parameter	Op Code	Parameter
CPU Acknowledge Events	N/A	Acknowledge events are located in SCB Status word	N/A	CX: CU completed action command
			N/A	FR: RU received a frame
			N/A	CNA: Command Unit became not active
			N/A	RNR: Receive Unit became not ready
Interrupt Control	1	Software Generated Interrupt	N/A	N/A (Need external latch)
	1	Interrupt Mask bit		
CU Commands	000	NOP	000	NOP
	001	CU Start	001	CU Start
	010	CU Resume	010	CU Resume
	011	Reserved	011	CU Suspend
	100	Load Dump Counters Address	100	CU Abort
	101	Dump Statistical Counters	101	Load Bus Throttle Timers
	110	Load CU Base		Load & restart Bus Throttle Timers
	111	Dump and Reset Statistical Counters	111	Reserved
RU Commands	000	NOP	000	NOP
	001	RU Start	001	RU Start
	010	RU Resume	010	RU Resume
	011	Reserved	011	RU Suspend
	100	RU Abort	100	RU Abort
	101	Load Header Data Size	101	Reserved
	110	Load RU Base	110	Reserved
	111	RBD Resume	111	Reserved
Other	N/A	Must use PORT reset	N/A	Reset (logically same as hardware RESET)

5.3 SCB Status/Acknowledge Comparisons

Type of Status	82557	82596
Interrupt Acknowledgment	CX/TNO: CU finished executing a command with "I" bit set, or indicates transmit command ended NOT OK. (configurable)	CX: CU finished executing a command with its "I" bit set.
	FR: RU finished receiving the frame, or header part of frame.	FR: RU finished receiving a frame.
	CNA: Command unit left the Active state and entered the idle state. (configurable)	CNA: Command unit left the active state.
	RNR: Receive unit left the Ready state.	RNR: Receive unit left the Ready state.
	MDI: MDI read or write cycle is completed. (configurable)	N/A
	SWI : Software generated interrupt.	N/A
CU Status	Idle	Idle
	Suspended	Suspended
	Active	Active
RU Status	Idle	Idle
	Suspended	Suspended
	No Resources	No Resources
	Ready	Ready
	Suspended with no more RBDs	N/A
	No resources due to no more RBDs	No resources due to no more RBDs
	Ready with no RBDs present	Ready with no RBDs present

5.4 Action Command Comparisons

Type of Command	Op Code	82557	Op Code	82596
Action Commands	000	NOP	000	NOP
	001	Individual Address Setup	001	Individual Address Setup
	010	Configure	010	Configure
	011	Multicast Address Setup	011	Multicast Address Setup
	100	Transmit	100	Transmit
	101	Reserved	101	TDR
	110	Dump	110	Dump
	111	Diagnose	111	Diagnose

5.5 Configure Parameter Differences

Parameters	Op Code	82557	Op Code	82596
Configure Command Parameters	010		010	
FIFO/DMA Parameters		RX FIFO Limit		FIFO Limit
		TX FIFO Limit		FIFO Limit
		RX DMA Max. Byte Count		N/A
		TX DMA Max. Byte Count		N/A
		DMA Max. Byte Count Enable		N/A
Statistical/Error Parameters		Save Bad Frames		Save Bad Frames
		Discard Short Receive Frames		N/A (use Min. Frame length)
		RCV CRC Transfer		N/A
		N/A		No CRC Insertion
		N/A		CRC-16/CRC-32
		N/A		CRC in Memory
		N/A		Monitor Bits
		N/A		Monitor
IEEE Parameters		Linear Priority		Linear Priority
		Interframe Spacing		Interface Spacing
		Broadcast Disable		Broadcast Disable
		Promiscuous Mode		Promiscuous Mode
		Linear Priority Mode		N/A
		No Source Address Insertion		No Source Address Insertion
		N/A		Backoff Method
		N/A		Slot Time
		N/A		Maximum Retry Number
		N/A		Disable Backoff
		N/A		Exponential Priority

5.5 Configure Parameter Differences (Continued)

Parameters	Op Code	82557	Op Code	82596
Collision Parameters		CRS or CDT		N/A
		N/A		Carrier Sense Filter
		N/A		Carrier Sense Source
		N/A		Collision Detect Filter
		N/A		Collision Detect Source
		N/A		Transmit on no CRS
		N/A		Collision Detect by Source Address Comparison
Header Parameters		N/A		Address Length
		N/A (use discard short frames)		Minimum Frame Length
		Multicast ALL		Multicast ALL
		Multiple Individual Address		Multiple Individual Address
		N/A		Preamble Until Carrier Sense
		Preamble Length		Preamble Length
Other		Adaptive IFS		N/A
		Late SCB Update		N/A
		Transmit Not OK Interrupt		N/A
		CU Idle Interrupt		N/A
		Underrun Retry		N/A
		503/MII		N/A
		Loopback		Loopback
		N/A		Manchester/NRZ
		Stripping Enable		N/A
		Padding Enable		N/A
		N/A		Bit Stuffing
		N/A		Padding (for Bit Stuffing)
		N/A		Auto Retransmit
		Byte Count		Byte Count
		Force Full Duplex		Full Duplex Operation
		Full Duplex Pin Enable		Full Duplex Operation

5.6 PORT Interface Comparisons

82557	82596
Software Reset	Software Reset
Self-Test	Self-Test
Selective Reset	N/A (must use CU/RU Abort)
Dump	Dump
N/A	SCP

5.7 Statistical/Error Information Comparisons

82557		82596	
Statistical/Error	**Location in Memory/On-Chip**	**Statistical/Error**	**Location in Memory/On-Chip**
Transmit Good Frames	on chip counter	N/A	N/A
Transmit Maximum Collisions Errors	on chip counter	Transmit Maximum Collisions (number of collisions experience per frame; used with Transmit Attempt Stopped)	in TCB (per frame)
N/A	N/A	Transmit Attempt Stopped (stopped because number of collisions exceeded max. number of retries)	in TCB (per frame)
Transmit Late Collisions Errors	on chip counter/in TCB	Transmit Late Collision	in TCB (per frame)
Transmit Underrun Errors	on chip counter	Transmit Underrun	in TCB (per frame)
Transmit Lost Carrier Sense	on chip counter	Transmit Lost Carrier Sense	in TCB (per frame)
Transmit Deferred	on chip counter	Transmit Deferred	in TCB (per frame)
Transmit Single Collisions	on chip counter	Use Transmit Max. Collisions	
Transmit Multiple Collisions	on chip counter		
Transmit Total Collisions	on chip counter		
Receive Good Frames	on chip counter	N/A	N/A
Receive CRC Errors	on chip counter	Receive CRC Errors	in SCB
Receive Alignment Errors	on chip counter	Receive Alignment Errors	in SCB
Receive Resource Errors	on chip counter	Receive Resource Errors	in SCB
Receive Overrun Errors	on chip counter	Receive Overrun Errors	in SCB
Receive Collision Detect Errors	on chip counter	Receive Collision Detect Errors	in SCB
Receive Short Frame Errors	on chip counter	Receive Short Frame Errors	in SCB
N/A	N/A	Heartbeat Indicator	in TCB (per frame)
N/A	N/A	Transmit lost Clear to Send	in TCB (per frame)

6.0 ADDITIONAL INFORMATION

For additional literature contact your local Intel sales office or contact the Intel Literature Center by calling 1-800-548-4725. If you need design information, contact your local Intel Field Applications Engineer.

intel®

2

Telecommunication Products

2910A
PCM CODEC - μLAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G712 Compatible, ATT T1 Compatible with 8th Bit Signaling**
- **Microcomputer Interface with On-Chip Timeslot Computation**
- **Simple Direct Mode Interface When Fixed Timeslots are Used**
- **±5% Power Supplies: +12V, +5V, −5V**
- **78dB Dynamic Range, with Resolution Equivalent to 12-Bit Linear Conversion Around Zero**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption 230 mW Typ. Standby Power 33mW Typ.**
- **Fabricated with Reliable N-Channel MOS Process**

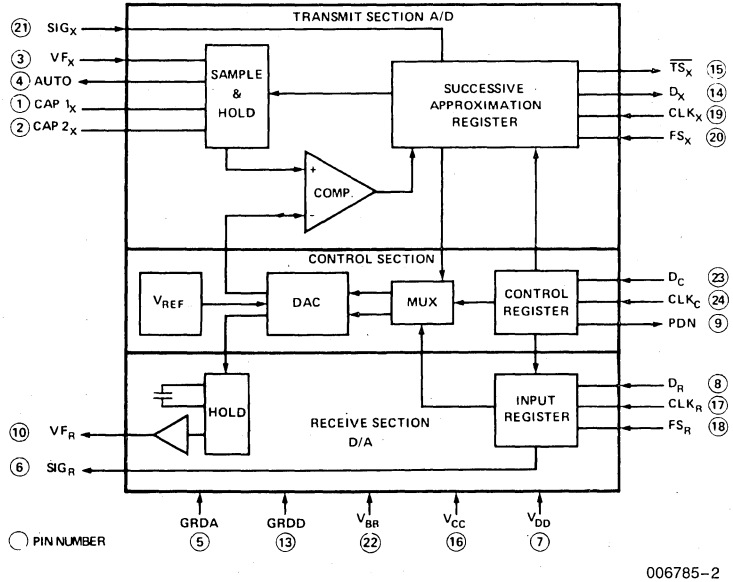
The Intel 2910A is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link and provide in-band signaling.

The primary applications are in telephone systems:

- Transmission —T1 Carrier
- Switching —Digital PBX's and Central Office Switching Systems
- Concentration —Subscriber Carrier/Concentrators

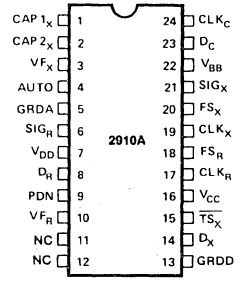
The wide dynamic range of the 2910A (78dB) and the minimal conversion time (80μsec minimum) make it an ideal product for other applications, like:

• Date Acquisition • Telemetry • Secure Communications Systems • Signal Processing Systems



006785-2

Figure 1. Block Diagram



006785-1

Figure 2. Pin Configuration

CAP 1_X, CAP 2_X	Holding Capacitor
VF_X	Analog Input
VF_R	Analog Output
D_R, D_C, SIG_X	Digital Input
SIG_R, D_X, $\overline{TS}_X$	Digital Output
CLK_C, CLK_X, CLK_R	Clock Input
FS_X, FS_R	Frame Sync Input
AUTO	Auto Zero Output
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
PDN	Power Down
GRDA	Analog Ground
GRDD	Digital Ground
NC	No Connect

Figure 3. Pin Names

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

November 1986
Order Number: 006785-002

2911A-1
PCM CODEC—A LAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G732 Compatible, Even Order Bits Inversion Included**
- **Microcomputer Interface with On-Chip Time-Slot Computation**
- **Simple Direct Mode Interface When Fixed Timeslots Are Used**
- **±5% Power Supplies: +12V, +5V, −5V**
- **66 dB Dynamic Range, with Resolution Equivalent to 11-Bit Linear Conversion Around Zero**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption 230 mW Typ. Standby Power 33 mW Typ.**
- **Fabricated with Reliable N-Channel MOS Process**

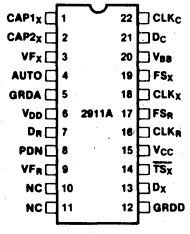
The Intel 2911A is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link.

The primary applications are in telephone systems:

- Transmission — 30/32 Channel Systems at 2.048 Mbps
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

The wide dynamic range of the 2911A (66 dB) and the minimal conversion time (80 μs minimum) make it an ideal product for other applications, like:

- Data Acquisition
- Telemetry
- Secure Communications Systems
- Signal Processing Systems

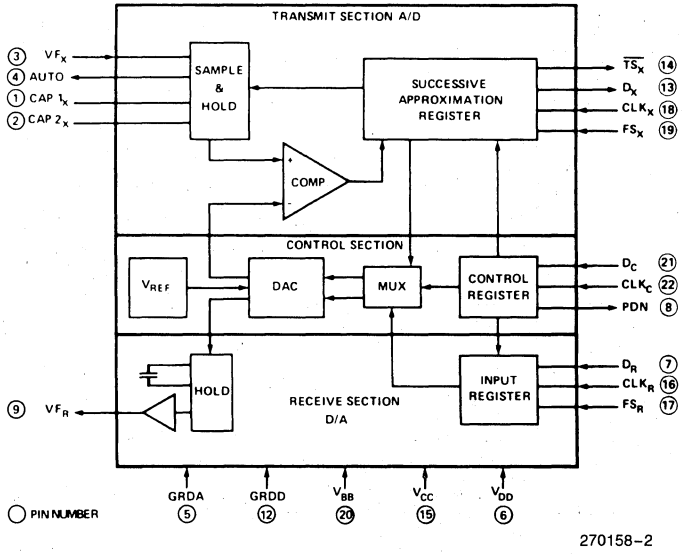


270158-1

Figure 1. Pin Configuration

CAP 1_X, CAP 2_X	Holding Capacitor
VF_X	Analog Input
VF_R	Analog Output
D_R, D_C	Digital Input
D_X, $\overline{TS_X}$	Digital Output
CLK_C, CLK_X, CLK_R	Clock Input
FS_X, FS_R	Frame Sync Input
AUTO	Auto Zero Output
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
PDN	Power Down
GRDA	Analog Ground
GRDD	Digital Ground
NC	No Connect

Figure 2. Pin Names



270158-2

Figure 3. Block Diagram

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

November 1986
Order Number: 270158-001

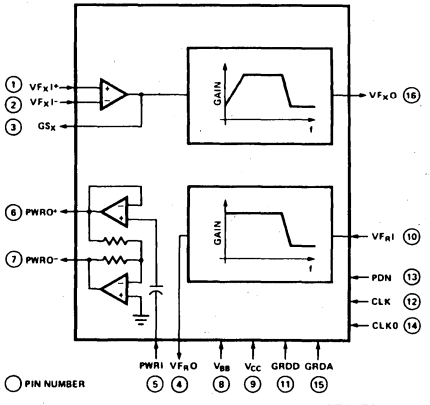
2912A
PCM TRANSMIT/RECEIVE FILTER

- **Low Power Consumption:**
  60 mW Typical without Power Amplifiers
  80 mW Typical with Power Amplifiers
  0.5 mW Typical Standby
- **Low Idle Channel Noise:**
  2 dBrnc0 Typical, Receive
  6 dBrnc0 Typical, Transmit
- **Excellent Power Supply Rejection:**
  40 dB Typical on V_{CC} @ 50 KHz
  30 dB Typical on V_{BB} @ 50 KHz
- **Transmit Filter Rejects Low Frequency Noise:**
  23 dB @ 60 Hz
  25 dB @ 50 Hz
  50 dB @ 16-2/3 Hz
- **Adjustable Gain in Both Directions**
- **Fully Compatible with the Industry Standard Intel 2912**
- **D3/D4 and CCITT G712 Compatible**
- **Common Mode Op Amp Input Rejection 75 dB Typical**
- **Direct Interface to the Intel 2910A/2911A PCM Codecs Including Stand-By Power Down Mode**
- **Direct Interface with Transformer or Electronic Hybrids**
- **Fabricated with Reliable N-Channel MOS Process**

2

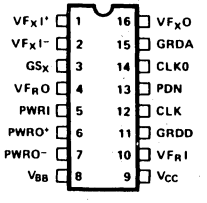
The Intel 2912A 2nd generation PCM line filter is a fully integrated monolithic device containing the two filters of a PCM line or trunk termination. It has improved key parameters of power consumption, idle channel noise, and power supply rejection. A single part exceeds both AT&T* D3/D4 and CCITT transmission specs, exceeds digital Class 5 central office switching system stringent specifications, and is fully compatible with the 2912. The primary application for the 2912A is in telephone systems for transmission, switching, or remote concentration.

An advanced version of the switched capacitor technique used for the 2912 is used to implement the transmit and receive passband filter sections of the 2912A. The device is fabricated using Intel's reliable two layer polysilicon gate NMOS technology. (See Intel Reliability Report RR-24 on the 2910A, 2911A, and 2912.) The combination of advances in the switched capacitor techniques first used on the 2912 and the NMOS technology results in a monolithic 2912A filter which is packaged in a standard 16-pin DIP.



270159-1

Figure 1. Block Diagram



270159-2

Pin Names

VF_XI^+, VF_XI^-	Analog Inputs
GS_X	Gain Control
VF_XO	Analog Output
VF_RI	Analog Input
VF_RO	Analog Output
PWRI	Driver Input
$PWRO^+$, $PWRO^-$	Driver Output
CLK	Clock Input
CLK0	Clock Selection
PDN	Power Down
V_{CC}	Power (+5V)
V_{BB}	Power (−5V)
GRDD	Digital Ground
GRDA	Analog Ground

Figure 2. Pin Configuration

*AT&T is a registered trademark of American Telephone and Telegraph Corporation.

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1988
Order Number: 270159-002

2913 AND 2914
COMBINED SINGLE-CHIP PCM CODEC AND FILTER

- **2913 Synchronous Clocks Only, 300 Mil Package**
- **2914 Asynchronous Clocks, 8th Bit Signaling, Loop Back Test Capability**
- **AT&T D3/D4 and CCITT Compatible for Synchronous Operation**
- **Pin Selectable μ-Law or A-Law Operation**
- **Two Timing Modes:**
  - **— Fixed Data Rate Mode 1.536, 1.544, or 2.048 MHz**
  - **— Variable Data Rate Mode 64 KHz 2.048 MHz**
- **Exceptional Analog Performance**
- **28-Pin Plastic Leaded Chip Carrier (PLCC) for Higher Integration**
- **Low Power HMOS-E Technology:**
  - **— 5 mW Typical Power Down**
  - **— 140 mW Typical Operating**
- **Fully Differential Architecture Enhances Noise Immunity**
- **On-Chip Auto Zero, Sample and Hold, and Precision Voltage References**
- **Direct Interface with Transformer or Electronic Hybrids**

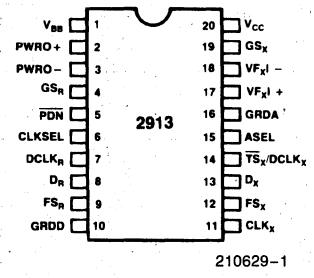
The Intel 2913 and 2914 are fully integrated PCM codecs with transmit/receive filters fabricated in a highly reliable and proven N-channel HMOS silicon gate technology (HMOS-E). These devices provide the functions that were formerly provided by two complex chips (2910A or 2911A and 2912A). Besides the higher level of integration, the performance of the 2913 and 2914 is superior to that of the separate devices.

The primary applications for the 2913 and 2914 are in telephone systems:

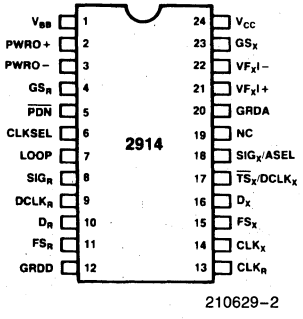
- Switching—Digital PBX's and Central Office Switching Systems
- Transmission—D3/D4 Type Channel Banks and Subscriber Carrier Systems
- Subscriber Instruments—Digital Handsets and Office Workstations

The wide dynamic range of the 2913 and 2914 (78 dB) and the minimal conversion time make them ideal products for other applications such as:

- Voice Store and Forward
- Digital Echo Cancellers
- Secure Communications Systems
- Satellite Earth Stations

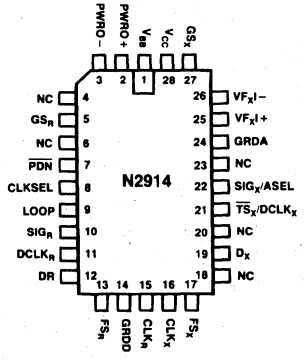


210629-1



210629-2

PLCC 28-Lead Rectangular



210629-3

Figure 1. Pin Configurations

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 210629-004

iATC 29C48
FEATURE CONTROL COMBO

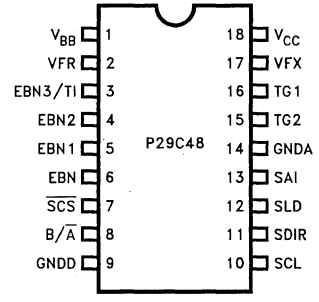
- **External and User Programmable Transmit and Receive Gain**
- **Programmable External Hybrid Balance Network Select**
- **Programmable Analog, Digital and Subscriber Loopback**
- **Programmable μ/A-Law Select**
- **Secondary Analog Input Channel**
- **Low Power Consumption**
- **External Tone Injection to Receive Path**
- **SLD A/B Channel Select (for 16 Channel Line Cards)**

The Intel iATC 29C48 Feature Control Combo is a low cost, user-programmable, fully integrated PCM Codec with transmit/receive filters fabricated in a CMOS technology. This technology is built on CHMOS and will allow the 29C48 to realize the same excellent transmission performance as in the Intel 2913/2914 combo while achieving the low power consumption typical of CMOS circuits.

The 29C48 supports the analog subscriber with a variety of added per-line features to the normal BORSCHT functions associated with the analog line circuit. Some of these features include secondary analog input channel, programmable transmit and receive gain, custom hybrid balancing network selection, and programmable μ or A-law conversions. Additionally, the 29C48 can operate on either the A or B channel of the SLD interface, allowing two combos to be connected to one SLD link. In order to facilitate the SLIC interface in this configuration, the 29C48 generates SLIC chip select signals for the proper routing of signaling information.

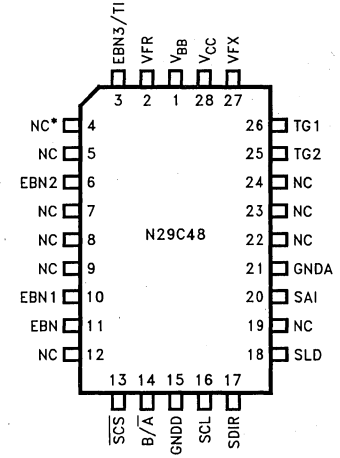
A unique feature of the 29C48 is programmable tone injection. This feature and its SLD interface makes it particularly easy to use in conjunction with Intel's advanced transceivers, such as the iATC 29C53AA, in subscriber equipment environments. The 29C53AA handles transfer of voice and feature control information to the 29C48.

18-Lead Plastic Dual-In-Line Package



270153-1

28-Lead Rectangular Plastic Leaded Chip Carrier



*Not connected

270153-2

Figure 1. Pin Configurations

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 270153-008

intel®

3

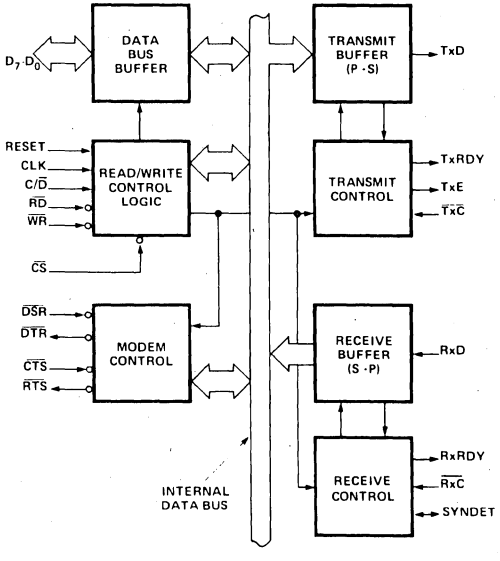
Communication / Interface Controllers

8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
- **Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous 5-8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling**
- **Synchronous Baud Rate—DC to 64K Baud**
- **Asynchronous Baud Rate—DC to 19.2K Baud**
- **Full-Duplex, Double-Buffered Transmitter and Receiver**
- **Error Detection—Parity, Overrun and Framing**
- **Compatible with an Extended Range of Intel Microprocessors**
- **28-Pin DIP Package**
- **All Inputs and Outputs are TTL Compatible**
- **Available in EXPRESS and Military Versions**

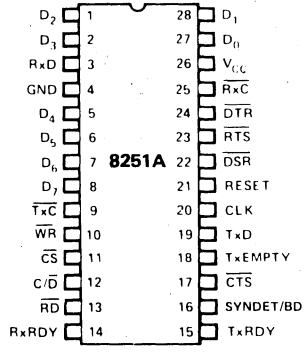
3

The Intel 8251A is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's microprocessor families such as MCS-48, 80, 85, and iAPX-86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using Intel's high performance HMOS technology.



205222-1

Figure 1. Block Diagram



205222-2

Figure 2. Pin Configuration

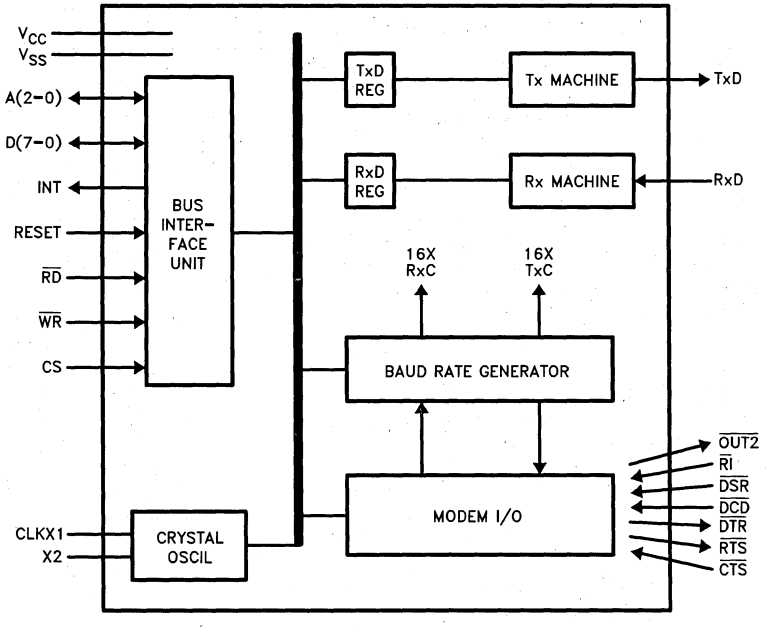
The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 205222-003

82050
ASYNCHRONOUS COMMUNICATIONS CONTROLLER

- **Asynchronous Operation**
  - **— 5- to 8-Bit Character Format**
  - **— Odd-, Even-, or No-Parity Generation and Detection**
  - **— Serial Bit Rate: DC to 56 Kb/s**
- **Programmable, 16-Bit Baud Rate Generator**
- **System Clock**
  - **— On-Chip Crystal Oscillator**
  - **— Externally Generated Clock**
- **28-Lead DIP and PLCC Packages**
- **IBM PC (INS 16450/8250A) Software Compatible**
- **Seven I/O Pins**
  - **— Dedicated Modem I/O**
  - **— General Purpose I/O**
- **No-TTL Interface to Most Intel Processors**
- **Internal Diagnostics with Local Loopback**
- **Complete Interrupt and Status Reporting**
- **CHMOS III Technology Provides Increased Reliability and Reduced Power Consumption**
- **Line Break Generation and Detection**

The Intel CHMOS 82050 Asynchronous Communications Controller is a low cost, higher performance alternative to the INS 16450—it emulates the INS 16450 and provides 100% compatibility with IBM PC software. Its 28-lead package provides all the functionality necessary for an IBM PC environment while substantially decreasing board space requirements. The 82050's simpler system interface reduces TTL glue—especially for higher frequency PC bus designs. The 82050 provides a low cost, high-performance integrated modem solution when combined with Intel's 89024 modem chip set. The compact 28-pin 82050 is fabricated using CHMOS III technology for decreased power consumption and increased reliability.



290137-1

Figure 1. Block Diagram

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

October 1994
Order Number: 290137-006

82510
ASYNCHRONOUS SERIAL CONTROLLER

- **Asynchronous Operation**
  - **— 5- to 9-Bit Character Format**
  - **— Baud Rate DC to 288k**
  - **— Complete Error Detection**
- **Multiple Sampling Windows**
- **Two, Independent, Four-Byte Transmit and Receive FIFOs with Programmable Threshold**
- **Two, 16-Bit Baud Rate Generators/ Timers**
- **System Clock Options**
  - **— On-Chip Crystal Oscillator**
  - **— External Clocks, Low/High Speed**
- **MCS-51 9-Bit Protocol Support**
- **IBM PC AT* (INS 8250A/16450) Software Compatible**
- **Control Character Recognition**
- **CHMOS III with Power Down Mode**
- **Interrupts Maskable at Two Levels**
- **Auto Echo and Loopback Modes**
- **Seven I/O Pins, Dedicated and General Purpose**
- **28-Lead DIP and PLCC Packages**
  (See Packaging Spec., Order #: 231369)

The Intel CHMOS 82510 is designed to increase system efficiency in asynchronous environments such as modems or serial ports—including expanding performance areas: MCS-51 9-bit format and high speed async. The functional support provided in the 82510 is unparalleled—two baud rate generators/timers provide independent data rates or protocol timeouts; a crystal oscillator and smart modem I/O simplify system logic. New features, dual FIFOs and Control Character Recognition (CCR), dramatically reduce CPU interrupts and increase software efficiency. The 82510's software versatility allows emulation of the INS8250A/16450 for IBM PC AT* compatibility or a high-performance mode, configured by 35 control registers. All interrupts are maskable at two levels. The multipersonality I/O pins are configurable as desired. A DPLL and multiple sampling of serial data improve data reliability for high-speed, asynchronous communication. The compact 28-pin 82510 is fabricated with CHMOS III technology and includes a software powerdown option.

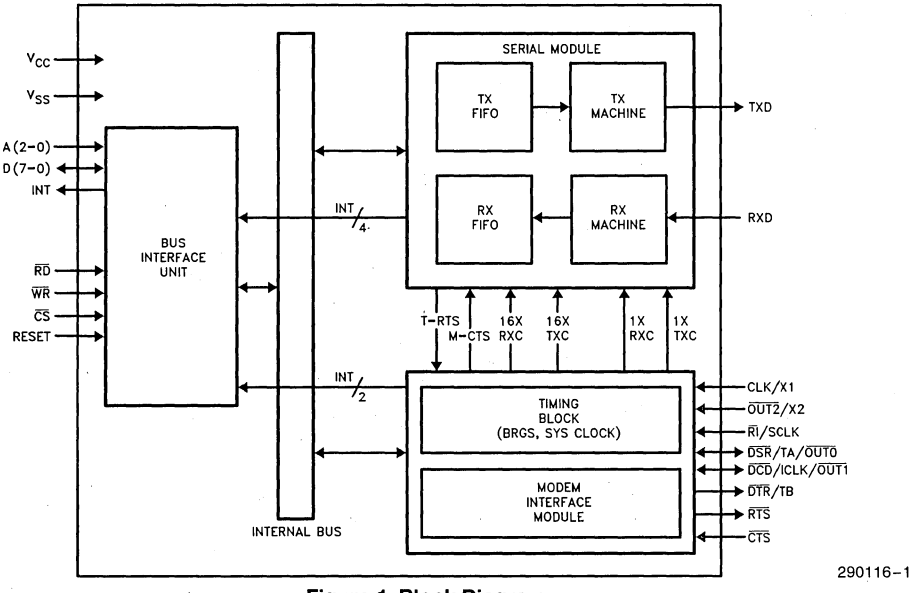


Figure 1. Block Diagram

*IBM and PC AT are trademarks of International Business Machines.

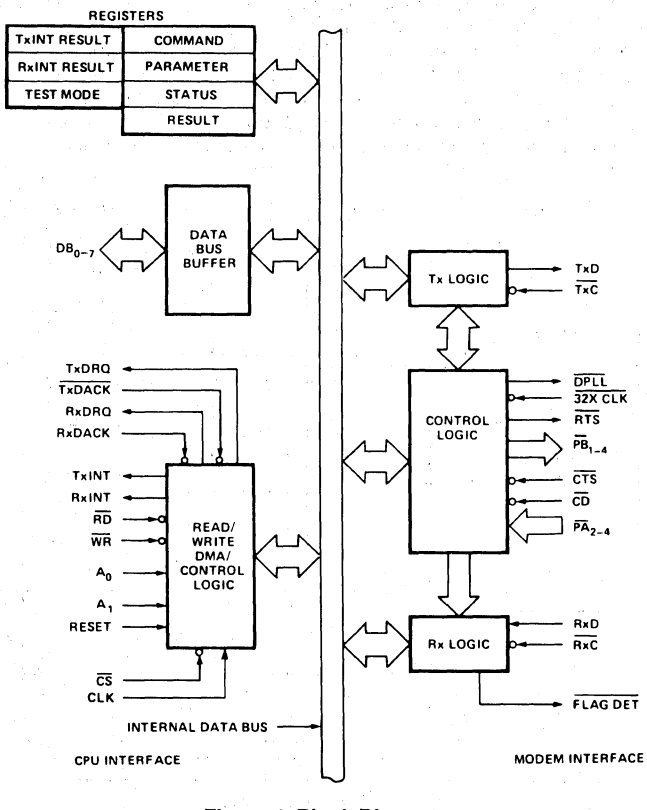
The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

October 1994
Order Number: 290116-006

8273
PROGRAMMABLE HDLC/SDLC PROTOCOL CONTROLLER

- **CCITT X.25 Compatible**
- **HDLC/SDLC Compatible**
- **Full Duplex, Half Duplex, or Loop SDLC Operation**
- **Up to 64K Baud Synchronous Transfers**
- **Automatic FCS (CRC) Generation and Checking**
- **Up to 9.6K Baud with On-Board Phase Locked Loop**
- **Programmable NRZI Encode/Decode**
- **Two Programmable Modem Control Ports**
- **Digital Phase Locked Loop Clock Recovery**
- **Minimum CPU Overhead**
- **Fully Compatible with 8048/8080/ 8085/8088/8086/80188/80186 CPUs**
- **Single +5V Supply**

The Intel 8273 Programmable HDLC/SDLC Protocol Controller is a dedicated device designed to support the ISO/CCITT's HDLC and IBM's SDLC communication line protocols. It is fully compatible with Intel's new high performance microcomputer systems such as the MCS 188/186. A frame level command set is achieved by a unique microprogrammed dual processor chip architecture. The processing capability supported by the 8273 relieves the system CPU of the low level real-time tasks normally associated with controllers.



210479-1

Figure 1. Block Diagram

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

December 1992
Order Number: 210479-004

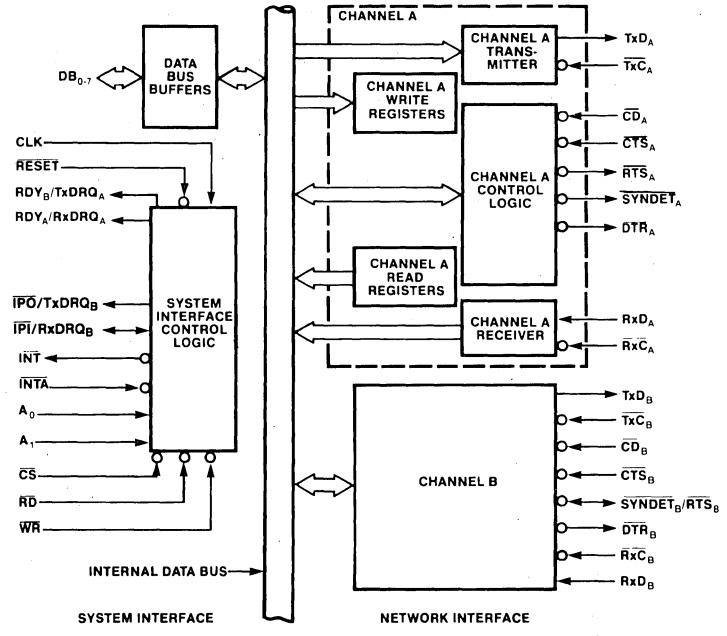
8274
MULTI-PROTOCOL SERIAL CONTROLLER (MPSC)

- **Asynchronous, Byte Synchronous and Bit Synchronous Operation**
- **Two Independent Full Duplex Transmitters and Receivers**
- **Fully Compatible with 8048, 8051, 8085, 8088, 8086, 80188 and 80186 CPU's; 8257 and 8237 DMA Controllers; and 8089 I/O Proc.**
- **4 Independent DMA Channels**
- **Baud Rate: DC to 880K Baud**
- **Asynchronous:**
  - **5–8 Bit Character; Odd, Even, or No Parity; 1, 1.5 or 2 Stop Bits**
  - **Error Detection: Framing, Overrun, and Parity**
- **Byte Synchronous:**
  - **Character Synchronization, Int. or Ext.**
  - **One or Two Sync Characters**
  - **Automatic CRC Generation and Checking (CRC-16)**
  - **IBM Bisync Compatible**
- **Bit Synchronous:**
  - **SDLC/HDLC Flag Generation and Recognition**
  - **8 Bit Address Recognition**
  - **Automatic Zero Bit Insertion and Deletion**
  - **Automatic CRC Generation and Checking (CCITT-16)**
  - **CCITT X.25 Compatible**
- **Available in EXPRESS and Military**

3

The Intel 8274 Multi-Protocol Series Controller (MPSC) is designed to interface High Speed Communications Lines using Asynchronous, IBM Bisync, and SDLC/HDLC protocol to Intel microcomputer systems. It can be interfaced with Intel's MCS-48, -85, -51; iAPX-86, -88, -186 and -188 families, the 8237 DMA Controller, or the 8089 I/O Processor in polled, interrupt driven, or DMA driven modes of operation.

The MPSC is a 40 pin device fabricated using Intel's High Performance HMOS Technology.



170102-1

Figure 1. Block Diagram

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

April 1995
Order Number: 170102-005

82530/82530-6
SERIAL COMMUNICATIONS CONTROLLER (SCC)

- **Two Independent Full Duplex Serial Channels**
- **On Chip Crystal Oscillator, Baud-Rate Generator and Digital Phase Locked Loop for Each Channel**
- **Programmable for NRZ, NRZI or FM Data Encoding/Decoding**
- **Diagnostic Local Loopback and Automatic Echo for Fault Detection and Isolation**
- **System Clock Rates:**
  - **— 4 MHz for 82530**
  - **— 6 MHz for 82530-6**
- **Max Bit Rate (6 MHz)**
  - **— Externally Clocked: 1.5 Mbps**
  - **Self-Clocked:**
  - **375 Kbps FM CODING**
  - **187 Kbps NRZI CODING**
  - **93 Kbps Asynchronous**
- **Interfaces with Any INTEL CPU, DMA or I/O Processor**
- **Available in 40 Pin DIP and 44 Lead PLCC**
- **Available in Express Version**
- **Asynchronous Modes**
  - **— 5–8 bit Character; Odd, Even or No Parity; 1, 1.5 or 2 Stop Bits**
  - **— Independent Transmit and Receive Clocks. 1X, 16X, 32X or 64X Programmable Sampling Rate**
  - **— Error Detection: Framing, Overrun and Parity**
  - **— Break Detection and Generation**
- **Bit Synchronous Modes**
  - **— SDLC Loop/Non-Loop Operation**
  - **— CRC-16 or CCITT Generation Detection**
  - **— Abort Generation and Detection**
  - **— I-field Residue Handling**
  - **— CCITT X.25 Compatible**
- **Byte Synchronous Modes**
  - **— Internal or External Character Synchronization (1 or 2 Characters)**
  - **— Automatic CRC Generation and Checking (CRC 16 or CCITT)**
  - **— IBM Bisync Compatible**

The INTEL 82530 Serial Communications Controller (SCC) is a dual-channel, multi-protocol data communications peripheral. It is designed to interface high speed communications lines using Asynchronous, Byte synchronous and Bit synchronous protocols to INTEL's microprocessors based systems. It can be interfaced with Intel's MCS51/96, iAPX86/88/186 and 188 in polled, interrupt driven or DMA driven modes of operation.

The SCC is a 40-pin device manufactured using INTEL's high-performance HMOS* II technology.

---

* HMOS is a patented process of Intel Corporation.

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

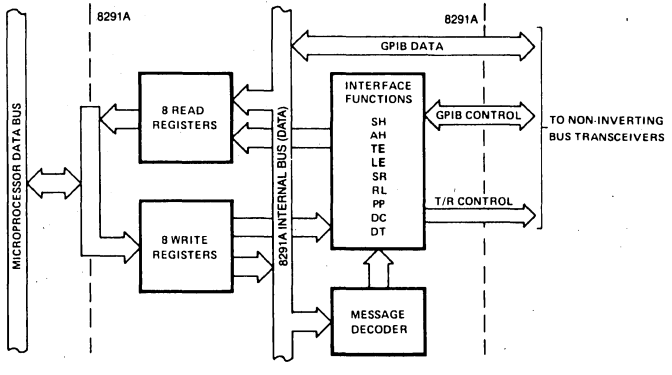
October 1987
Order Number: 230834-003

8291A
GPIB TALKER/LISTENER

- Designed to Interface Microprocessors (e.g., 8048/49, 8051, 8080/85, 8086/88) to an IEEE Standard 488 Digital Interface Bus
- Programmable Data Transfer Rate
- Complete Source and Acceptor Handshake
- Complete Talker and Listener Functions with Extended Addressing
- Service Request, Parallel Poll, Device Clear, Device Trigger, Remote/Local Functions
- Selectable Interrupts
- On-Chip Primary and Secondary Address Recognition
- Automatic Handling of Addressing and Handshake Protocol
- Provision for Software Implementation of Additional Features
- 1–8 MHz Clock Range
- 16 Registers (8 Read, 8 Write), 2 for Data Transfer, the Rest for Interface Function Control, Status, etc.
- Directly Interfaces to External Non-Inverting Tranceivers for Connection to the GPIB
- Provides Three Addressing Modes, Allowing the Chip to be Addressed Either as a Major or a Minor Talker/Listener with Primary or Secondary Addressing
- DMA Handshake Provision Allows for Bus Transfers without CPU Intervention
- Trigger Output Pin
- On-Chip EOS (End of Sequence) Message Recognition Facilitates Handling of Multi-Byte Transfers

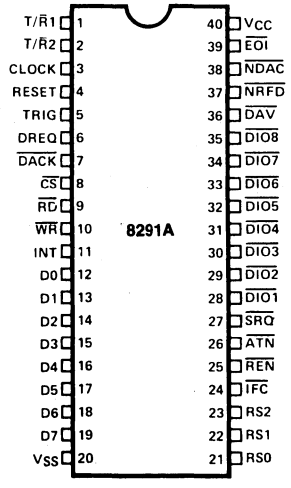
3

The 8291A is an enhanced version of the 8291 GPIB Talker/Listener designed to interface microprocessors to an IEEE Standard 488 Instrumentation Interface Bus. It implements all of the Standard's interface functions except for the controller. The controller function can be added with the 8292 GPIB Controller.



205248-1

Figure 1. Block Diagram



205248-2

Figure 2. Pin Configuration

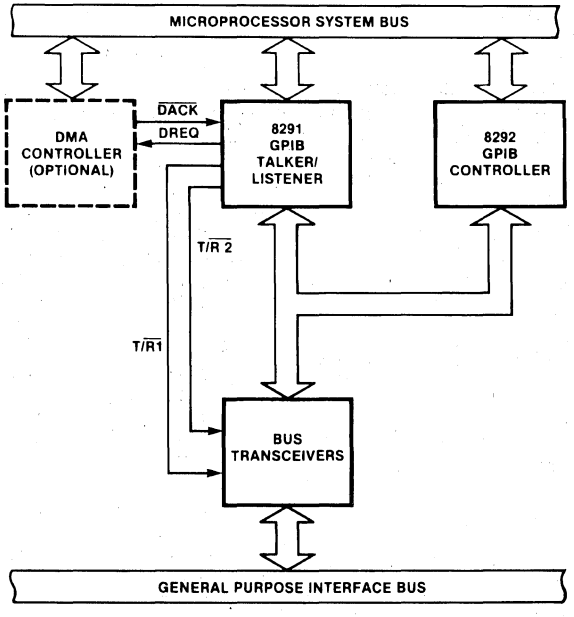
The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 205248-003

8292
GPIB CONTROLLER

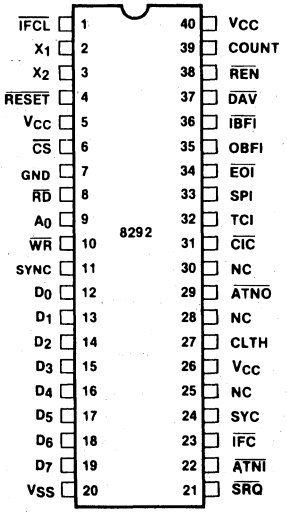
- **Complete IEEE Standard 488 Controller Function**
- **Interface Clear (IFC) Sending Capability Allows Seizure of Bus Control and/or Initialization of the Bus**
- **Responds to Service Requests (SRQ)**
- **Sends Remote Enable (REN), Allowing Instruments to Switch to Remote Control**
- **Complete Implementation of Transfer Control Protocol**
- **Synchronous Control Seizure Prevents the Destruction of Any Data Transmission in Progress**
- **Connects with the 8291 to Form a Complete IEEE Standard 488 Interface Talker/Listener/Controller**

The 8292 GPIB Controller is a microprocessor-controlled chip designed to function with the 8291 GPIB Talker/Listener to implement the full IEEE Standard 488 controller function, including transfer control protocol. The 8292 is a preprogrammed Intel 8041A.



205250-1

Figure 1. 8291, 8292 Block Diagram



205250-2

Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 205250-003

8294A
DATA ENCRYPTION/DECRYPTION UNIT

- **Certified by National Bureau of Standards**
- **400 Byte/Sec Data Conversion Rate**
- **64-Bit Data Encryption Using 56-Bit Key**
- **DMA Interface**
- **3 Interrupt Outputs to Aid in Loading and Unloading Data**
- **7-Bit User Output Port**
- **Single 5V ± 10% Power Supply**
- **Fully Compatible with iAPX-86, 88, MCS-85, MCS-80, MCS-51, and MCS-48 Processors**
- **Implements Federal Information Processing Data Encryption Standard**
- **Encrypt and Decrypt Modes Available**

The Intel 8294A Data Encryption Unit (DEU) is a microprocessor peripheral device designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard. The DEU operates on 64-bit text words using a 56-bit user-specified key to produce 64-bit cipher words. The operation is reversible: if the cipher word is operated upon, the original text word is produced. The algorithm itself is permanently contained in the 8294A; however, the 56-bit key is user-defined and may be changed at any time.

The 56-bit key and 64-bit message data are transferred to and from the 8294A in 8-bit bytes by way of the system data bus. A DMA interface and three interrupt outputs are available to minimize software overhead associated with data transfer. Also, by using the DMA interface two or more DEUs may be operated in parallel to achieve effective system conversion rates which are virtually any multiple of 400 bytes/second. The 8294A also has a 7-bit TTL compatible output port for user-specified functions.

Because the 8294A implements the NBS encryption algorithm it can be used in a variety of Electronic Funds Transfer applications as well as other electronic banking and data handling applications where data must be encrypted.

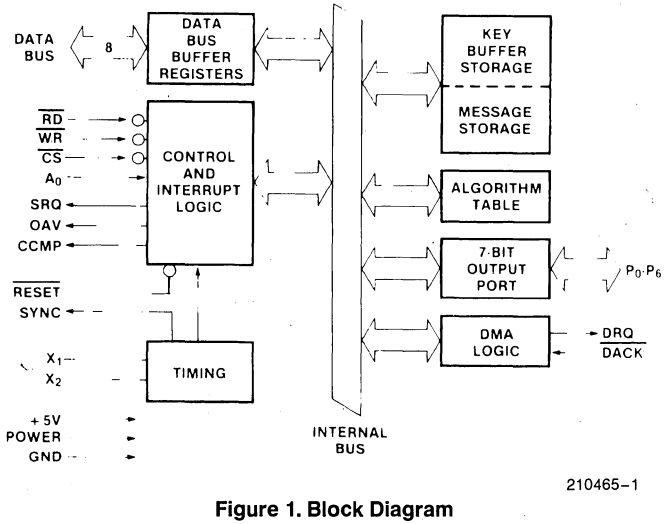


Figure 1. Block Diagram

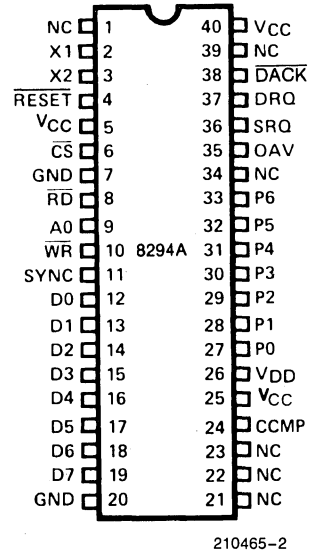


Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 210465-005

NORTH AMERICAN SALES OFFICES

ARIZONA

Intel Corp.
410 North 44th Street
Suite 470
Phoenix 85008
Tel: (800) 628-8686
FAX: (602) 244-0446

CALIFORNIA

Intel Corp.
26707 W. Agoura Road
Suite 203
Calabasas, CA 91302
Tel: (800) 628-8686
FAX: (818)-880-1820

Intel Corp.
3550 Watt Avenue
Suite 140
Sacramento 95821
Tel: (800) 628-8686
FAX: (916) 979-7011

Intel Corp.
9655 Granite Ridge Drive
3rd Floor
Suite 4A
San Diego 92123
Tel: (800) 628-8686
FAX: (619) 467-2460

Intel Corp.
1781 Fox Drive
San Jose 95131
Tel: (800) 628-8686
FAX: (408) 441-9540

Intel Corp.
1551 North Tustin Avenue
Suite 800
Santa Ana 92701
Tel: (800) 628-8686
TWX: (910) 595-1114
FAX: (714) 541-9157

Intel Corp.
514 Via de la Valle
Suite 208-RCO
Solana Beach 92075

Intel Corp.
1960 E. Grand Avenue
Suite 150
El Segundo, CA 90245
Tel: (800) 628-8686
FAX: (310) 640-7133

COLORADO

Intel Corp.
600 South Cherry Street
Suite 700
Denver 80222
Tel: (800) 628-8686
TWX: 910-931-2289
FAX: (303) 322-8670

CONNECTICUT

Intel Corp.
40 Old Ridgebury Road
Suite 311
Danbury 06811
Tel: (800) 628-8686
FAX: (203) 778-2168

FLORIDA

Intel Corp.
600 West Hillsboro Blvd.
Suite 348
Deerfield Beach 33441
Tel: (800) 628-8686
FAX: (305) 421-2444

Intel Corp.
2250 Lucien Way
Suite 100
Suite 8
Maitland 32751
Tel: (800) 628-8686
FAX: (407) 660-1283

GEORGIA

Intel Corp.
20 Technology Park
Suite 150
Norcross 30092
Tel: (800) 628-8686
FAX: (404) 448-0875

IDAHO

Intel Corp.
910 W. Main Street
Suite 236
Boise 83702
Tel: (800) 628-8686
FAX: (208) 331-2295

ILLINOIS

Intel Corp.
300 North Martingale Road
Suite 400
Schaumburg 60173
Tell: (800) 628-8686
FAX: (708) 605-9762

INDIANA

Intel Corp.
8041 Knue Road
Indianapolis 46250
Tel: (800) 628-8686
FAX: (317) 577-4939

MARYLAND

Intel Corp.
131 National Bus. Pkwy
Suite 200
Annapolis Junction 20701
Tel: (800) 628-8686
FAX: (301) 206-3678

MASSACHUSETTS

Intel Corp.
Nagog Park
125 Nagog Park
Acton 01720
Tel: (800) 628-8686
FAX: (508) 266-3867

MICHIGAN

Intel Corp.
32255 North Western Hwy.
Suite 212, Tri Atria
Farmington Hills 48334
Tel: (800) 628-8686
FAX: (313) 851-8770

MINNESOTA

Intel Corp.
3500 West 80th Street
Suite 360
Bloomington 55431
Tel: (800) 628-8686
TWX: 910-576-2867
FAX: (612) 831-6497

NEW JERSEY

Intel Corp.
2001 Route 46
Suite 310
Parsippany 07054
Tel: (800) 628-8686
FAX: (201) 402-4893

Intel Corp.
Lincroft Center
125 Half Mile Road
Red Bank 07701
Tel: (800) 628-8686
FAX: (908) 747-0983

NEW YORK

Intel Corp.
850 Cross Keys Office Pk
Fairport 14450
Tel: (800) 628-8686
TWX: 510-253-7391
FAX: (716) 223-2561

Intel Corp.
2950 Expressway Drive
Islandia 11722
Tel: (800) 628-8686
TWX: 510-227-6236
FAX: (516) 348-7939

OHIO

Intel Corp.
56 Milford Drive
Suite 205
Hudson 44236
Tel: (800) 628-8686
FAX: (216) 528-1026

***†Intel Corp.**
3401 Park Center Drive
Suite 220
Dayton 45414
Tel: (800) 628-8686
TWX: 810-450-2528
FAX: (513) 890-8658

OKLAHOMA

Intel Corp.
6801 North Broadway
Suite 115
Oklahoma City 73162
Tel: (800) 628-8686
FAX: (405) 840-9819

OREGON

Intel Corp.
15254 NW Greenbrier
Pkwy
Building B
Beaverton 97006
Tel: (800) 628-8686
TWX: 910-467-8741
FAX: (503) 645-8181

PENNSYLVANIA

Intel Corp.
925 Harvest Drive
Suite 200
Blue Bell 19422
Tel: (800) 628-8686
FAX: (215) 641-0785

SOUTH CAROLINA

Intel Corp.
7403 Parklane Road
Suite 4
Columbia 29223
Tel: (800) 628-8686
FAX: (803) 788-7999

Intel Corp.
100 Executive Center Dr
Suite 109, B183
Greenville 29615
Tel: (800) 628-8686
FAX: (803) 297-3401

TEXAS

Intel Corp.
8911 Capital of Texas Hwy
Suite 4230
Austin 78759
Tel: (800) 628-8686
FAX: (512) 338-9335

Intel Corp.
5000 Quorum Drive
Suite 750
Dallas 75240
Tel: (800) 628-8686
FAX: (214) 233-1325

Intel Corp.
20405 State Hwy 249
Suite 880
Houston 77070
Tel: (800) 628-8686
TWX: 910-881-2490
FAX: (713) 376-2891

UTAH

Intel Corp.
428 East 6400 South
Suite 135
Murray 84107
Tel: (800) 628-8686
FAX: (801) 268-1457

WASHINGTON

Intel Corp.
2800 156th Avenue SE
Suite 105
Bellevue 98007
Tel: (800) 628-8686
FAX: (206) 746-4495

WISCONSIN

Intel Corp.
400 North Executive Drive
Suite 401
Brookfield 53005
Tel: (800) 628-8686
FAX: (414) 789-2746

CANADA

BRITISH COLUMBIA

Intel of Canada, Ltd.
999 Canada Place
Suite 404
Suite 11
Vancouver V6C 3E2
Tel: (800) 628-8686
FAX: (604) 844-2813

ONTARIO

Intel of Canada, Ltd.
2650 Queensview Drive
Suite 250
Ottawa K2B 8H6
Tel: (800) 628-8686
FAX: (613) 820-5936

Intel of Canada, Ltd.
190 Attwell Drive
Suite 500
Rexdale M9W 6H8
Tel: (800) 628-8686
FAX: (416) 675-2438

QUEBEC

Intel of Canada, Ltd.
1 Rue Holiday, Tour West
Suite 320
Pt. Claire H9R 5N3
Tel: (800) 628-8686
FAX: 514-694-0064

NORTH AMERICAN DISTRIBUTORS

ALABAMA

Anthem Electronics
600 Boulevard South
Suite 104F & H
Huntsville 35802
Tel: (205) 890-0302

Arrow/Schweber Electronics
1015 Henderson Road
Huntsville 35805
Tel: (205) 837-6955
FAX: (205) 721-1581

Hall-Mark Computer
4890 University Square
Huntsville 35816
Tel: (800) 409-1483

Hamilton Hallmark
4890 University Square
Suite 1
Huntsville 35816
Tel: (205) 837-8706
FAX: (205) 830-2565

MTI Systems Sales
4950 Corporate Drive
Suite 120
Huntsville 35805
Tel: (205) 830-9526
FAX: (205) 830-9557

Pioneer Technologies Group
4835 University Square
Suite 5
Huntsville 35805
Tel: (205) 837-9300
FAX: (205) 837-9358

Wyle Electronics
7800 Governers Dr., W.
Tower Building, 2nd Floor
Huntsville 35807
Tel: (205) 830-1119
FAX: (205) 830-1520

ARIZONA

Alliance Electronics
7550 East Redfield Rd
Scottsdale 85260
Tel: (602) 261-7988

Anthem Electronics
1555 West 10th Place
Suite 101
Tempe 85281
Tel: (602) 966-6600
FAX: (602) 966-4826

Arrow/Schweber Electronics
2415 West Erie Drive
Tempe 85282
Tel: (602) 431-0030
FAX: (602) 431-9555

Avnet Computer
1626 South Edwards Dr
Tempe 85281
Tel: (800) 426-7999

Hall-Mark Computer
4637 South 37th Place
Phoenix 85040
Tel: (800) 409-1483

Pioneer Standard
1438 West Broadway
Suite B-140
Tempe 85282
Tel: (602) 350-9335

Hamilton Hallmark
4637 South 36th Place
Phoenix 85040
Tel: (602) 437-1200
FAX: (602) 437-2348

Wyle Electronics
4141 East Raymond
Phoenix 85040
Tel: (602) 437-2088
FAX: (602) 437-2124

CALIFORNIA

Anthem Electronics
9131 Oakdale Avenue
Chatsworth 91311
Tel: (818) 775-1333
FAX: (818) 775-1302

Anthem Electronics
1 Oldfield Drive
Irvine 92718-2809
Tel: (714) 768-4444
FAX: (714) 768-6456

Anthem Electronics
580 Menlo Drive
Suite 8
Rocklin 95677
Tel: (916) 624-9744
FAX: (916) 624-9750

Anthem Electronics
9369 Carroll Park Drive
San Diego 92121
Tel: (619) 453-9005
FAX: (619) 546-7893

Anthem Electronics
1160 Ridder Park Drive
San Jose 95131
Tel: (408) 453-1200
FAX: (408) 441-4504

Arrow/Schweber Electronics
26707 West Agoura Road
Calabasas 91302
Tel: (818) 880-9686
FAX: (818) 772-8930

Arrow/Schweber Electronics
48834 Kato Road
Suite 103
Fremont 94538
Tel: (510) 490-9477
FAX: (510) 490-1084

Arrow/Schweber Electronics
6 Cromwell
Suite 100
Irvine 92718
Tel: (714) 581-4622
FAX: (714) 454-4206

Arrow/Schweber Electronics
9511 Ridgehaven Court
San Diego 92123
Tel: (619) 565-4800
FAX: (619) 279-8062

Arrow/Schweber Electronics
1180 Murphy Avenue
San Jose 95131
Tel: (408) 441-9700
FAX: (408) 453-4810

Avnet Computer
1 Mauchley
Irvine 92718
Tel: (800) 426-7999

Avnet Computer
371 Van Ness Way
Torrance 90501
Tel: (800) 426-7999

Avnet Computer
15950 Bernardo Ctr Dr
Suite 6
San Diego 92127
Tel: (800) 426-7999

Avnet Computer
1175 Bordeaux Drive
Suite A
Sunnyvale 94089
Tel: (800) 426-7999

Hall-Mark Computer
21150 Califa Street
Woodland Hills 91367
Tel: (800) 409-1483

Hall-Mark Computer
15950 Bernardo Ctr Dr
Suite C
San Diego 92127
Tel: (800) 409-1483

Hall-Mark Computer
1175 Bordeaux Drive
Sunnyvale 94089
Tel: (800) 409-1483

Hall-Mark Computer
1 Mauchly
Irvine 92718
Tel: (800) 409-1483

Hall-Mark Computer
580 Menlo Drive
Suite 2
Rocklin 95765
Tel: (800) 409-1483

Hamilton Hallmark
3170 Pullman Street
Costa Mesa 92626
Tel: (714) 641-4100
FAX: (714) 641-4122

Hamilton Hallmark
2105 Lundy Avenue
San Jose 95131
Tel: (408) 435-3500
FAX: (408) 435-3720

Hamilton Hallmark
4545 Viewridge Avenue
San Diego 92123
Tel: (619) 571-7540
FAX: (619) 277-6136

Hamilton Hallmark
21150 Califa Street
Woodland Hills 91367
Tel: (818) 594-0404
FAX: (818) 594-8234

Hamilton Hallmark
580 Menlo Drive
Suite 2
Rocklin 95762
Tel: (916) 624-9781
FAX: (916) 961-0922

Pioneer Standard
5126 Clareton Drive
Suite 106
Agoura Hills 91301
Tel: (818) 865-5800

Pioneer Standard
217 Technology Drive
Suite 110
Irvine 92718
Tel: (714) 753-5090

Pioneer Technologies Group
134 Rio Robles
San Jose 95134
Tel: (408) 954-9100
FAX: (408) 954-9113

Pioneer Standard
4370 La Jolla Village Drive
San Diego 92122
Tel: (619) 546-4906

Wyle Electronics
15370 Barranca Pkwy
Irvine 92713
Tel: (714) 753-9953
FAX: (714) 753-9877

Wyle Electronics
15360 Barranca Pkwy
Suite 200
Irvine 92713
Tel: (714) 753-9953
FAX: (714) 753-9877

Wyle Electronics
2951 Sunrise Blvd.
Suite 175
Rancho Cordova 95742
Tel: (916) 638-5282
FAX: (916) 638-1491

Wyle Electronics
9525 Chesapeake Dr.
San Diego 92123
Tel: (619) 565-9171
FAX: (619) 365-0512

Wyle Electronics
3000 Bowers Avenue
Santa Clara 95051
Tel: (408) 727-2500
FAX: (408) 727-5896

Wyle Electronics
17872 Cowan Avenue
Irvine 92714
Tel: (714) 863-9953
FAX: (714) 263-0473

Wyle Electronics
26010 Mureau Road
Suite 150
Calabasas 91302
Tel: (818) 880-9000
FAX: (818) 880-5510

Zeus Arrow Electronics
6276 San Ignacio Avenue
Suite E
San Jose 95119
Tel: (408) 629-4689
FAX: (408) 629-4792

Zeus Arrow Electronics
6 Cromwell Street
Suite 100
Irvine 92718
Tel: (714) 581-4622
FAX: (714) 454-4355

COLORADO

Anthem Electronics
373 Inverness Dr. S.
Englewood 80112
Tel: (303) 790-4500
FAX: (303) 790-4532

Arrow/Schweber Electronics
61 Inverness Dr East
Suite 105
Englewood 80112
Tel: (303) 799-0258
FAX: (303) 799-0730

Avnet Computer
9605 Maroon Circle
Englewood 80111
Tel: (800) 426-7999

Hall-Mark Computer
9605 Maroon Circle
Englewood 80111
Tel: (800) 409-1483

Hamilton Hallmark
12503 East Euclid Dr
Suite 20
Englewood 80111
Tel: (303) 790-1662
FAX: (303) 790-4991

Hamilton Hallmark
710 Wooten Road
Suite 28
Colorado Springs 80915
Tel: (719) 637-0055
FAX: (719) 637-0088

Pioneer Technologies
5600 Greenwood Plaza Blvd.
Suite 201
Englewood 80111
Tel: (303) 773-8090

Wyle Electronics
451 East 124th Avenue
Thornton 80241
Tel: (303) 457-9953
FAX: (303) 457-4831

CONNECTICUT

Anthem Electronics
61 Mattatuck Heights Road
Waterburg 06705
Tel: (203) 575-1575
FAX: (203) 596-3232

Arrow/Schweber Electronics
860 N. Main St. Ext.
Wallingford 06492
Tel: (203) 265-7741
FAX: (203) 265-7988

Hall-Mark Computer
Still River Corporate Ctr
55 Federal Road
Danbury 06810
Tel: (800) 409-1483

Hamilton Hallmark
125 Commerce Court, Unit 6
Cheshire 06410
Tel: (203) 271-2844
FAX: (203) 272-1704

Pioneer Standard
2 Trap Falls Road
Shelton 06484
Tel: (203) 929-5600

FLORIDA

Anthem Electronics
5200 NW 3rd Avenue
Suite 206
Ft. Lauderdale 33309
Tel: (305) 484-0990

Anthem Electronics
598 S. Northlake Blvd.
Suite 1024
Altamonte Sprgs 32701
Tel: (813) 797-2900
FAX: (813) 796-4880

Arrow/Schweber Electronics
400 Fairway Drive
Suite 102
Deerfield Beach 33441
Tel: (305) 429-8200
FAX: (305) 428-3991

Arrow/Schweber Electronics
37 Skyline Drive
Suite 3101
Lake Mary 32746
Tel: (407) 333-9300
FAX: (407) 333-9320

Arrow/Schweber Electronics
4010 Boy Scout Dr.
Suite 295
Tampa 33607
Tel: (813) 873-1030
FAX: (813) 873-0077

Avnet Computer
541 S. Orlando Ave.
Suite 203
Maitland 32751
Tel: (800) 426-7999

Hall-Mark Computer
10491 72nd St. North
Largo 34647
Tel: (800) 409-1483

Hall-Mark Computer
13700 58th St. North
Suite 206
Clearwater 34620
Tel: (800) 409-1483

Hamilton Hallmark
3350 N.W. 53rd Street
Suite 105-107
Ft. Lauderdale 33309
Tel: (305) 484-5482
FAX: (305) 484-2995

NORTH AMERICAN DISTRIBUTORS (Cont'd)

Hamilton Hallmark
10491 72nd St. North
Largo 34647
Tel: (813) 541-7440
FAX: (813) 544-4394

Hamilton Hallmark
7079 University Blvd.
Winter Park 32792
Tel: (407) 657-3300
FAX: (407) 678-4414

Pioneer Technologies Group
337 Northlake Blvd
Suite 1000
Alta Monte Spgs 32701
Tel: (407) 834-9090
FAX: (407) 834-0865

Pioneer Technologies Group
674 South Military Trail
Deerfield Beach 33442
Tel: (305) 428-8877
FAX: (305) 481-2950

Wyle Electronics
1000 112th Circle North
St. Petersburg 33716
Suite 800
Tel: (813) 579-1518
FAX: (813) 579-1518

Zeus Arrow Electronics
37 Skyline Drive
Bldg D., Suite 3101
Lake Mary 32746
Suite 800
Tel: (407) 333-3055
FAX: (407) 333-9681

GEORGIA

Anthem Electronics
2400 Pleasant Hill Rd
Suites 9 & 10
Duluth 30136
Tel: (404) 931-3900
FAX: (404) 931-3902

Arrow/Schweber Electronics
4250 E Riyergreen Pkwy
Suite E
Duluth 30136
Tel: (404) 497-1300
FAX: (404) 476-1493

Avnet Computer
3425 Corporate Way
Suite G
Duluth 30136
Tel: (800) 426-7999

Hall-Mark Computer
3425 Corporate Way
Suite G
Duluth 30136
Tel: (800) 409-1483

Hamilton Hallmark
3425 Corporate Way
Suite G & A
Duluth 30136
Tel: (404) 623-5475
FAX: (404) 623-5490

Pioneer Technologies Group
4250C Rivergreen Pkwy
Duluth 30136
Tel: (404) 623-1003
FAX: (404) 623-0665

Wyle Electronics
6025 The Corners Pkwy
Suite 111
Norcross 30092
Tel: (404) 441-9045
FAX: (404) 441-9086

ILLINOIS

Anthem Electronics
1300 Remington Road
Suite A
Schaumberg 60173
Tel: (708) 884-0200
FAX: (708) 885-0480

Arrow/Schweber Electronics
1140 W Thorndale Rd
Itasca 60143
Tel: (708) 250-0500

Avnet Computer
1124 Thorndale Ave
Bensenville 60106
Tel: (800) 426-7999

Hall-Mark Computer
1124 Thorndale Ave
Bensenville 60106
Tel: (800) 409-1483

Hamilton Hallmark
1130 Thorndale Ave
Bensenville 60106
Tel: (800) 426-7999

MTI Systems Sales
1140 West Thorndale Avenue
Itasca 60143
Tel: (708) 250-8222
FAX: (708) 250-8275

Pioneer Standard
2171 Executive Drive
Suite 200
Addison 60101
Tel: (708) 495-9680
FAX: (708) 495-9831

Wyle Electronics
2055 Army Trail Road
Suite 140
Addison 60101
Tel: (800) 853-9953

Zeus Arrow Electronics
1140 W Thorndale Ave
Itasca 60143
Tel: (708) 250-0500

INDIANA

Arrow/Schweber Electronics
7108 Lakeview
Parkway West Drive
Indianapolis 46268
Tel: (317) 299-2071
FAX: (317) 299-2379

Avnet Computer
655 West Carmel Drive
Suite 160
Carmel 46032
Tel: (800) 426-7999

Hall-Mark Computer
655 West Carmel Drive
Carmel 46032
Tel: (800) 409-1483

Hamilton Hallmark
655 West Carmel Drive
Suite 160
Carmel 46032
Tel: (317) 575-3500
FAX: (317) 575-3535

Pioneer Standard
9350 Priority Way W Dr
Indianapolis 46250
Tel: (317) 573-0880
FAX: (317) 573-0979

KANSAS

Arrow/Schweber Electronics
9801 Legler Road
Lenexa 66219
Tel: (913) 541-9542
FAX: (913) 541-0328

Hall-Mark Computer
10809 Lakeview Ave
Lenexa 66219
Tel: (800) 409-1483

Hamilton Hallmark
10809 Lakeview
Avenue
Lenexa 66215
Tel: (913) 888-4747
FAX: (913) 888-0523

MARYLAND

Anthem Electronics
7168A Columbia
Gateway Drive
Columbia 21046
Tel: (800) 239-6039

Arrow/Schweber Electronics
9800J Patuxent Woods
Drive
Columbia 21046
Tel: (301) 596-7800
FAX: (301) 596-7821

Avnet Computer
7172 Columbia
Gateway Drive
Suite G
Columbia 21045
Tel: (800) 426-7999

Hall-Mark Computer
7172 Columbia
Gateway Drive
Suite G
Columbia 21046
Tel: (800) 409-1483

Hamilton Hallmark
10240 Old Columbia
Road
Columbia 21046
Tel: (410) 988-9800
FAX: (410) 381-2036

North Atlantic Industries
Systems Division
7125 River Wood Drive
Columbia 21046
Tel: (301) 312-5800
FAX: (301) 312-5850

Pioneer Technologies Group
15810 Gaither Road
Gaithersburg 20877
Tel: (301) 921-0660
FAX: (301) 670-6746

Wyle Electronics
9101 Guilford Road
Suite 120
Columbia 21046
Tel: (301) 490-2170
FAX: (301) 490-2190

MASSACHUSETTS

Anthem Electronics
200 Research Drive
Wilmington 01887
Tel: (508) 657-5170
FAX: (508) 657-6008

Arrow/Schweber Electronics
25 Upton Drive
Wilmington 01887
Tel: (508) 658-0900
FAX: (508) 694-1754

Avnet Computer
10 D Centennial Drive
Peabody 01960
Tel: (800) 426-7999

Hall-Mark Computer
10 D Centennial Drive
Peabody 01960
Tel: (800) 409-1483

Hamilton Hallmark
10 D Centennial Drive
Peabody 01960
Tel: (508) 531-7430
FAX: (508) 532-9802

Pioneer Standard
44 Hartwell Avenue
Lexington 02173
Tel: (617) 861-9200
FAX: (617) 863-1547

Wyle Electronics
5 Oak Park Drive
Bedford 01803
Tel: (617) 271-9953
FAX: (617) 275-3809

Zeus Arrow Electronics
25 Upton Drive
Wilmington 01887
Tel: (508) 658-4776
FAX: (508) 694-2199

MICHIGAN

Arrow/Schweber Electronics
44720 Helm Street
Plymouth 48170
Tel: (313) 462-2290
FAX: (313) 462-2686

Avnet Computer
41650 Garden Brk Rd
Suite 120
Novi 48375
Tel: (800) 426-7999

Hall-Mark Computer
41650 Garden Brk Rd
Suite 120
Novi 48375
Tel: (800) 409-1483

Hamilton Hallmark
44191 Plymouth Oaks
Blvd.
Suite 1300
Plymouth 48170
Tel: (313) 416-5806
FAX: (313) 416-5811

Hamilton Hallmark
41650 Garden Brk Rd
Suite 100
Novi 49418
Tel: (313) 347-4271
FAX: (313) 347-4021

Pioneer Standard
4505 Broadmoor S.E.
Grand Rapids 49512
Tel: (616) 698-1800
FAX: (616) 698-1831

Pioneer Standard
44190 Plymouth Oaks
Blvd.
Plymouth 48170
Tel: (313) 525-1800
FAX: (313) 427-3720

MINNESOTA

Anthem Electronics
7646 Golden Triangle
Drive
Eden Prairie 55344
Tel: (612) 944-5454
FAX: (612) 944-3045

Arrow/Schweber Electronics
10100 Viking Drive
Suite 100
Eden Prairie 55344
Tel: (612) 941-5280
FAX: (612) 942-7803

Avnet Computer
9800 Bren Roaqd East
Suite 410
Minnetonka 55343
Tel: (800) 426-7999

Hall-Mark Computer
9800 Bren Road East
Suite 410
Minnetonka 55343
Tel: (800) 409-1483

Hamilton Hallmark
9401 James Ave South
Suite 140
Bloomington 55431
Tel: (612) 881-2600
FAX: (612) 881-9461

Pioneer Standard
7625 Golden Triangle
Drive
Suite G
Eden Prairie 55344
Tel: (612) 944-3355
FAX: (612) 944-3794

Wyle Electronics
1325 East 79th Street
Suite 1
Bloomington 55425
Tel: (612) 853-2280
FAX: (612) 853-2298

MISSOURI

Arrow/Schweber Electronics
2380 Schuetz Road
St. Louis 63141
Tel: (314) 567-6888
FAX: (314) 567-1164

Avnet Computer
3783 Rider Train South
Earth City 63045
Tel: (800) 426-7999

Hall-Mark Computer
3783 Rider Trail South
Earth City 63045
Tel: (800) 409-1483

Hamilton Hallmark
3783 Rider Trail South
Earth City 63045
Tel: (314) 291-5350
FAX: (314) 291-0362

NEW HAMPSHIRE

Avnet Computer
2 Executive Park Drive
Bedford 03102
Tel: (800) 426-7999

NEW JERSEY

Anthem Electronics
26 Chapin Road, Unit K
Pine Brook 07058
Tel: (201) 227-7960
FAX: (201) 227-9246

Arrow/Schweber Electronics
4 East Stow Road
Unit 11
Marlton 08053
Tel: (609) 596-8000
FAX: (609) 596-9632

Arrow/Schweber Electronics
43 Route 46 East
Pine Brook 07058
Tel: (201) 227-7880
FAX: (201) 227-2064

Avnet Computer
1-B Keystone Avenue
Building 36
Cherry Hill 08003
Tel: (800) 426-7999

Hall-Mark Computer
1-B Keystone Avenue
Building 36
Cherry Hill 08003
Tel: (800) 409-1483

Hall-Mark Computer
10 Lanidex Plaza West
Parsippany 07054
Tel: (800) 409-1483

Hamilton Hallmark
1 Keystone Avenue
Building 36
Cherry Hill 08003
Tel: (609) 424-0110
FAX: (609) 751-2552

Hamilton Hallmark
10 Lanidex Plaza West
Parsippany 07054
Tel: (201) 515-5300
FAX: (201) 515-1601

MTI Systems Sales
43 Route 46 East
Pinebrook 07058
Tel: (201) 882-8780
FAX: (201) 539-6430

NORTH AMERICAN DISTRIBUTORS (Cont'd)

PioneerStandard
14-A Madison Road
Fairfield 07006
Tel: (201) 575-3510
FAX: (201) 575-3454

Wyle Electronics
115 Route 46, Bldg F
Mountain Lakes 07046
Tel: (201) 402-4970

NEW MEXICO

Alliance Electronics, Inc.
3411 Bryn Mawr N.E.
Albuquerque 87101
Tel: (505) 292-3360
FAX: (505) 275-6392

Avnet Computer
7801 Academy Road
Building 1, Suite 204
Albuquerque 87109
Tel: (800) 426-7999

NEW YORK

Anthem Electronics
47 Mall Drive
Commack 11725
Tel: (516) 864-6600
FAX: (516) 493-2244

Arrow/Schweber Electronics
3375 Brighton Henrietta Townline Road
Rochester 14623
Tel: (716) 427-0300
FAX: (716) 427-0735

Arrow/Schweber Electronics
20 Oser Avenue
Hauppauge 11788
Tel: (516) 231-1000
FAX: (516) 231-1072

Avnet Computer
2 Penn Plaza
Suite 1245
New York 10121
Tel: (800) 426-7999

Avnet Computer
1057 E. Henrietta Road
Rochester 14623
Tel: (800) 426-7999

Hall-Mark Computer
2 Penn Plaza
New York 10121
Tel: (800) 409-1483

Hall-Mark Computer
1057 E Henrietta Road
Rochester 14623
Tel: (800) 409-1483

Hamilton Hallmark
933 Motor Parkway
Hauppauge 11788
Tel: (516) 434-7470
FAX: (516) 434-7491

Hamilton Hallmark
1057 E Henrietta Road
Rochester 14623
Tel: (716) 475-9130
FAX: (716) 475-9119

Hamilton Hallmark
3075 Veterans Memorial Hwy.
Ronkonkoma 11779
Tel: (516) 737-0600
FAX: (516) 737-0838

MTI Systems Sales
1 Penn Plaza
250 West 34th Street
New York 10119
Tel: (212) 643-1280
FAX: (212) 643-1288

Pioneer Standard
68 Corporate Drive
Binghamton 13904
Tel: (607) 722-9300
FAX: (607) 722-9562

Pioneer Standard
60 Crossway Pk West
Woodbury, Long Island 11797
Tel: (516) 921-8700
FAX: (516) 921-2143

Pioneer Standard
840 Fairport Park
Fairport 14450
Tel: (716) 381-7070
FAX: (716) 381-5955

Zeus Arrow Electronics
100 Midland Avenue
Port Chester 10573
Tel: (914) 937-7400
FAX: (914) 937-2553

NORTH CAROLINA

Anthem Electronics
4805 Greenwood
Suite 100
Raleigh 27604
Tel: (919) 782-3550

Arrow/Schweber Electronics
5240 Greensdairy Road
Raleigh 27604
Tel: (919) 876-3132
FAX: (919) 878-9517

Avnet Computer
4421 Stuart Andrew Boulevard
Suite 600
Charlotte 28217
Tel: (800) 426-7999

Hall-Mark Computer
3510 Spring Forest Rd
Suite B
Raleigh 27604
Tel: (800) 409-1483

Hamilton Hallmark
3510 Spring Forest Rd
Suite B
Raleigh 27604
Tel: (800) 409-1483

Hamilton Hallmark
5234 Greens Dairy Rd
Raleigh 27604
Tel: (919) 878-0819

Pioneer Technologies Group
2200 Gateway Ctr. Blvd
Suite 215
Morrisville 27560
Tel: (919) 460-1530

OHIO

Arrow/Schweber Electronics
6573 Cochran Road
Suite E
Solon 44139
Tel: (216) 248-3990
FAX: (216) 248-1106

Arrow/Schweber Electronics
8200 Washington Village Drive
Centerville 45458
Tel: (513) 435-5563
FAX: (513) 435-2049

Avnet Computer
7764 Washington Village Drive
Dayton 45459
Tel: (800) 426-7999

Avnet Computer
2 Summit Park Drive
Suite 520
Independence 44131
Tel: (800) 426-7999

Hall-Mark Computer
5821 Harper Road
Solon 44139
Tel: (800) 409-1483

Hall-Mark Computer
777 Dearborn Pk Lane
Suite L
Worthington 43085
Tel: (800) 409-1483

Hamilton Hallmark
5821 Harper Road
Solon 44139
Tel: (216) 498-1100
FAX: (216) 248-4803

Hamilton Hallmark
777 Dearborn Pk Lane
Suite L
Worthington 43085
Tel: (614) 888-3313
FAX: (614) 888-0767

MTI Systems Sales
23404 Commerce Pk Road
Beachwood 44122
Tel: (216) 464-6688
FAX: (216) 464-3564

Pioneer Standard
4433 Interpoint Blvd
Dayton 45424
Tel: (513) 236-9900
FAX: (513) 236-8133

Pioneer Standard
4800 East 131st Street
Cleveland 44105
Tel: (216) 587-3600
FAX: (216) 663-1004

Wyle Electronics
6835 Cochran Rd.
Solon 44139
Tel: (216) 248-9996

OKLAHOMA

Arrow/Schweber Electronics
12101 East 51st Street
Suite 106
Tulsa 74146
Tel: (918) 252-7537
FAX: (918) 254-0917

Hamilton Hallmark
5411 S. 125th E. Ave
Suite 305
Tulsa 74146
Tel: (918) 254-6110
FAX: (918) 254-6207

Pioneer Standard
9717 East 42nd Street
Suite 105
Tulsa 74146
Tel: (918) 665-7840
FAX: (918) 665-1891

OREGON

Almac Arrow Electronics
9500 S.W. Nimbus Ave
Suite E
Beaverton 97008
Tel: (503) 629-8090
FAX: (503) 645-0611

Anthem Electronics
9090 SW Gemini Drive
Beaverton 97005
Tel: (503) 643-1114
FAX: (503) 626-7928

Avnet Computer
9750 SW Nimbus Ave.
Beaverton 97005
Tel: (800) 426-7999

Hall-Mark Computer
9750 SW Nimbus Ave.
Beaverton 97005
Tel: (800) 409-1483

Hamilton Hallmark
9750 SW Nimbus Ave.
Beaverton 97005
Tel: (503) 526-6200
FAX: (503) 641-5939

Pioneer Technologies
8905 Southwest Nimbus Ave.
Suite 160
Beaverton 97005
Tel: (503) 626-7300
FAX: (503) 626-5300

Wyle Electronics
9640 Sunshine Court
Building G
Suite 200
Beaverton 97005
Tel: (503) 643-7900
FAX: (503) 646-5466

PENNSYLVANIA

Anthem Electronics
355 Business Ctr Drive
Horsham 19044
Tel: (215) 443-5150
FAX: (215) 675-9875

Avnet Computer
213 Executive Drive
Suite 320
Mars 16046
Tel: (800) 426-7999

Arrow/Schweber Electronics
2681 Mosside Blvd
Suite 204
Monroeville 15146
Tel: (412) 856-9490

Pioneer Technologies Group
259 Kappa Drive
Pittsburgh 15238
Tel: (412) 782-2300
FAX: (412) 963-8255

Pioneer Technologies Group
500 Enterprise Road
Keith Valley Bus.Ctr
Horsham 19044
Tel: (215) 674-4000

Wyle Electronics
1 Eves Drive
Suite 111
Marlton 08053-3185
Tel: (609) 985-7953
FAX: (609) 985-8757

TEXAS

Anthem Electronics
651 N. Plano Road
Suite 401
Richardson 75081
Tel: (214) 238-7100
FAX: (214) 238-0237

Anthem Electronics
14050 Summit Drive
Suite 119
Tel: (512) 388-0049
FAX: (512) 388-0271

Arrow/Schweber Electronics
Brake Ctr III, Bldg M1
11500 Metric Boulevard
Suite 160
Austin 78758
Tel: (512) 835-4180
FAX: (512) 832-5921

Arrow/Schweber Electronics
3220 Commander Drive
Carrollton 75006
Tel: (214) 380-6464
FAX: (214) 248-7208

Arrow/Schweber Electronics
19416 Park Row
Suite 190
Houston 77084
Tel: (713) 647-6868
FAX: (713) 492-8722

Avnet Computer
4004 Beltline
Suite 200
Dallas 75244
Tel: (800) 426-799

Avnet Computer
1235 North Loop West
Suite 525
Houston 77008
Tel: (800) 426-7999

Hall-Mark Computer
12211 Technology Blvd
Austin 78727
Tel: (800) 409-1483

Hall-Mark Computer
4004 Beltline Road
Suite 200
Dallas 75244
Tel: (800) 409-1483

Hall-Mark Computer
1235 North Loop West
Houston 77008
Tel: (800) 409-1483

Hamilton Hallmark
12211 Technology Boulevard
Austin 78727
Tel: (512) 258-8848
FAX: (512) 258-3777

Hamilton Hallmark
11420 Page Mill Road
Dallas 75243
Tel: (214) 553-4300
FAX: (214) 553-4395

Hamilton Hallmark
8000 Westglen
Houston 77063
Tel: (713) 781-6100
FAX: (713) 953-8420

Pioneer Standard
1826D Kramer Lane
Austin 78758
Tel: (512) 835-4000
FAX: (512) 835-9829

Pioneer Standard
13765 Beta Road
Dallas 75244
Tel: (214) 263-3168
FAX: (214) 490-6419

Pioneer Standard
10530 Rockley Road
Suite 100
Houston 77099
Tel: (713) 495-4700
FAX: (713) 495-5642

Wyle Electronics
1810 Greenville Ave
Richardson 75081
Tel: (214) 235-9953
FAX: (214) 644-5064

Wyle Electronics
9208 Waterford Center Blvd
Suite 150
Austin 78750
Tel: (512) 345-8853
FAX: (512) 345-9330

Wyle Electronics
2901 Wilcrest
Suite 120
Houston 77099
Tel: (713) 879-9953
FAX: (713) 879-9953

Zeus Arrow Electronics
3220 Commander Dr
Carrollton 75006
Tel: (214) 380-4330
FAX: (214) 447-2222

UTAH

Anthem Electronics
1279 West 2200 South
Salt Lake City 84119
Tel: (801) 973-8555
FAX: (801) 973-8909

Arrow/Schweber Electronics
1946 West Parkway Boulevard
Salt Lake City 84119
Tel: (801) 973-6913
FAX: (801) 972-0200

NORTH AMERICAN DISTRIBUTORS (Cont'd)

Avnet Computer
1100 East 6600 South
Suite 150
Salt Lake City 84121
Tel: (800) 426-7999

Hall-Mark Computer
1100 East 6600 South
Suite 150
Salt Lake City
Tel: (800) 409-1483

Hamilton Hallmark
1100 East 6600 South
Suite 120
Salt Lake City 84121
Tel: (801) 266-2022
FAX: (801) 263-0104

Wyle Electronics
1325 West 2200 South
Suite E
West Valley 84119
Tel: (801) 974-9953
FAX: (801) 972-2524

WASHINGTON

Almac Arrow Electronics
14360 S.E. Eastgate Way
Bellevue 98007
Tel: (206) 643-9992
FAX: (206) 643-9709

Anthem Electronics
19017 120th Ave N.E.
Suite 102
Bothell 98011
Tel: (206) 483-1700
FAX: (206) 486-0571

Avnet Computer
8630 154th Ave, NE
Redmond 98052
Tel: (800) 426-7999

Hamilton Hallmark
8630 154th Avenue
Redmond 98052
Tel: (206) 881-6697
FAX: (206) 867-0159

Pioneer Technologies
2800 156th Ave S.E.
Suite 100
Bellevue 98007
Tel: (206) 644-7500

Wyle Electronics
15385 NE 90th St
Redmond 98052
Tel: (206) 881-1150
FAX: (206) 881-1567

WISCONSIN

Arrow/Schweber Electronics
200 N. Patrick
Suite 100
Brookfield 53045
Tel: (414) 792-0150
FAX: (414) 792-0156

Avnet Computer
2440 South 179th St
New Berlin 53416
Tel: (800) 426-7999

Hall-Mark Computer
2440 South 179th St
New Berlin 53146
Tel: (800) 409-1483

Hamilton Hallmark
2440 South 179th St
New Berlin 53146
Tel: (414) 797-7844
FAX: (414) 797-9259

Pioneer Standard
120 Bishops Way
Suite 163
Brookfield 53005
Tel: (414) 780-3600
FAX: (414) 780-3613

Wyle Electronics
150 North Patrick
Building 7, Suite 150
Brookfield 53045
Tel: (414) 879-0434
FAX: (414) 879-0474

ALASKA

Avnet Computer
1400 W Benson Blvd
Suite 400
Anchorage 99503
Tel: (800) 426-7999

CANADA

ALBERTA

Avnet Computer
1144 29th Avenue NE
Suite 108
Calgary T2E 7P1
Tel: (800) 387-3406

Pioneer/Pioneer
560, 1212-31 Ave. NE
Calgary T2E 7S8
Tel: (403) 291-1988
FAX: (403) 295-8714

BRITISH COLUMBIA

Almac Arrow Electronics
8544 Baxter Place
Burnaby V5A 4T8
Tel: (604) 421-2333
FAX: (604) 421-5030

Hamilton Hallmark
8610 Commerce Court
Burnaby V5A 4N6
Tel: (604) 420-4101
FAX: (604) 420-5376

Pioneer/Pioneer
4455 North 6 Road
Rochmond V6V 1P6
Tel: (604) 273-5575
FAX: (604) 273-2413

MANITOBA

Pioneer/Pioneer
540 Marjorie Street
Winnipeg R3H 0S9

ONTARIO

Arrow/Schweber Electronics
36 Antares Drive
Unit 100
Nepean K2E 7W5
Tel: (613) 226-6903
FAX: (613) 723-2018

Arrow/Schweber Electronics
1093 Meyerside, Unit 2
Mississauga L5T 1M4
Tel: (416) 670-2010
FAX: (416) 670-5863

Avnet Computer
Canada System Engineering Group
151 Superior Blvd.
Mississuaga L5T 2L1
Tel: (800) 387-3406

Avnet Computer
190 Colonade Road
Nepean K2E 7J5
Tel: (800) 387-3406

Canada System Engineering Group
151 Superior Boulevard
Mississuaga L5T 2L1
Tel: (800) 387-3406

Hamilton Hallmark
151 Superior Blvd.,
Unit 1-6
Mississauga L5T 2L1
Tel: (416) 564-6060
FAX: (416) 564-6033

Hamilton Hallmark
190 Colonade Road
Nepean K2E 7J5
Tel: (613) 226-1700
FAX: (613) 226-1184

Pioneer/Pioneer
3415 American Drive
Mississauga L4V 1T6
Tel: (416) 507-2600
FAX: (416) 507-2831

Pioneer/Pioneer
155 Colonnade Rd., S.
Suite 17
Nepean K2E 7K3
Tel: (613) 226-8840
FAX: (613) 226-6352

QUEBEC

Arrow/Schweber Electronics
1100 Street Regis Blvd
Dorval H9P 2T5
Tel: (514) 421-7411
FAX: (514) 421-7430

Gates Arrow Electronics
500 Boul.
St-Jean-Baptiste Ave
Quebec H2E 5R9
Tel: (418) 871-7500
FAX: (418) 871-6816

Avnet Computer
7575 Trans Canada
Suite 601
St. Laurent H4T 1V6
Tel: (800) 265-1135

Hamilton Hallmark
7575 Transcanada Hwy
Suite 600
Street Laurent H4T 2V6
Tel: (514) 335-1000
FAX: (514) 335-2481

Pioneer/Pioneer
520 McCaffrey
Street Laurent H4T 1N1
Tel: (514) 737-9700
FAX: (514) 737-5212

NORTH AMERICAN SERVICE OFFICES

Computervision

Intel Corporation's North American Preferred Service Provider

Central Dispatch: 1-800-876-SERV (1-800-876-7378)

ALABAMA
- Birmingham
- Huntsville

ALASKA
- Anchorage

ARIZONA
- Phoenix
- Tucson

ARKANSAS
- North Little Rock

CALIFORNIA
- Concord
- Los Angeles
- Ontario
- Orange
- Redwood City
- Sacramento
- San Diego
- San Francisco
- Van Nuys

COLORADO
- Colorado Springs
- Denver

CONNECTICUT
- E. Windsor
- Middlebury

FLORIDA
- Ft. Lauderdale
- Jacksonville
- Miami
- Orlando
- Pensacola
- Tampa

GEORGIA
- Atlanta

HAWAII
- Honolulu

ILLINOIS
- Chicago
- Wood Dale

INDIANA
- Carmel
- Evansville
- Ft. Wayne
- South Bend

IOWA
- Cedar Rapids
- Davenport
- West Des Moines

KANSAS
- Kansas City
- Wichita

KENTUCKY
- Louisville
- Madisonville

LOUISIANA
- Baton Rouge
- New Orleans

MAINE
- Auburn

MARYLAND
- Baltimore

MASSACHUSETTS
- Bedfoird
- S. Easton

MICHIGAN
- Detroit
- Flint
- Grand Rapids
- Lansing
- Troy

MINNESOTA
- Minneapolis

MISSOURI
- Springfield
- Street Louis

MISSISSIPPI
- Jackson

NEW HAMPSHIRE
- Manchester*

MONTANA
- Butte

NEBRASKA
- Omaha

NEW JERSEY
- Cherry Hill
- Hamilton Township
- Westfield

NEW MEXICO
- Albuquerque

NEW YORK
- Albany
- Binghampton
- Buffalo
- Farmingdale
- New York City
- Rochester
- Dryden

NORTH CAROLINA
- Ashville
- Charlotte
- Greensboro
- Raleigh
- Wilmington

OHIO
- Cincinnati
- Cleveland
- Columbus
- Dayton

OKLAHOMA
- Oklahoma City
- Tulsa

OREGON
- Beaverton

PENNSYLVANIA
- Camp Hill
- Erie
- Pittsburgh
- Wayne

SOUTH CAROLINA
- Charleston
- Columbia
- Greenville

TENNESSEE
- Chattanooga
- Knoxville
- Memphis
- Nashville

TEXAS
- Austin
- Houston
- Dallas
- Tyler

UTAH
- Salt Lake City

VERMONT
- White River Junction

VIRGINIA
- Charlottesville
- Richmond
- Roanoke
- Virginia Beach

WASHINGTON
- Renton
- Richland

WASHINGTON D.C.*

WEST VIRGINIA
- Charleston

WISCONSIN
- Milwaukee

CANADA
- Calgary
- Edmonton
- Fredericton
- Halifax
- Mississauga
- Montreal
- Ottawa
- Toronto
- Vancouver, BC*
- Winnipeg
- Quebec City
- Regina
- St.John's

Networking

As an established leader in the networking market, Intel provides a wide range of component solutions for workstations, servers, desktop and portable computer solutions. Intel offers a complete line of Ethernet* components featuring our new Fast Ethernet 10/100 Mbps 82557 controller. Intel also offers a range of products for telecommunications applications.

This databook features product datasheets and application information for Intel's networking and telecommunications product lines. The databook highlights the 82557, a highly integrated PCI Fast Ethernet controller, the 82595FX for cost-effective 10 Mbps ISA designs and the 82596, a high-performance LAN coprocessor for high-performance 10 Mbps applications. Charts and diagrams are included to show parameter and test conditions, layout principles and much more.

*Ethernet is a registered trademark of Xerox Corp.

ISBN 1-55512-256-6

Order Number 297360-003
Printed in USA/0196/18k/RRD/TS
iPG - Networking Products

Printed on Recycled Material