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Introduction to Intel Cell-Based Design

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Introduction to Intel Cell-Based Design

CELL BASED PRODUCTS

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PREFACE

A growing number of system designers are turning to Application Specific Integrated Circuits (ASICs) for the solution to their system design needs. ASIC design methodologies bridge the gap between standard ICs and fully-customized devices. Using sophisticated software design tools and a collection of predefined circuit elements, system designers realize the benefits of custom ICs without incurring the high cost and long development times associated with full custom designs.

The Intel Design Environment provides a flexible system for designing and manufacturing Intel ASIC products. ASIC designers may now choose from a broad range of products and services under the umbrella of Intel's proven leadership in semiconductor technology, including cell-based ICs, gate arrays, and Electrical Programmable Logic Devices (EPLDs). The design environment includes a comprehensive set of CAE/CAD tools, design libraries running on the Daisy and Mentor engineering workstations, and design and manufacturing services. Intel cell-based designs are backed by a proven manufacturing capability and the same strict adherence to quality and reliability applied to Intel standard products.

This manual introduces the Intel 1.5 Micron CHMOS III Cell Library. It provides cell data specifications and describes Intel design services as they relate to cell-based designs executed at Intel design centers or at the customer site. This is the second edition of the manual, superceding those manuals dated 1986.

RELATED PUBLICATIONS

• *Cell-Based Design—Daisy Environment*	Order # 83002
• *Cell-Based Design — Mentor Environment*	Order # 830000
• *Introduction to Intel Gate Array Design*	Order # 231811
• *Programmable Logic Handbook*	Order # 296083
• *Microprocessor and Peripheral Handbook*	Order # 230843
• *Embedded Controller Handbook*	Order # 210918
• *Components Quality/Reliability Handbook*	Order # 210997

MANUAL ORGANIZATION

The Introduction to Intel Cell-Based Design manual is organized into the following chapters and appendixes:

- Chapter 1, "Introduction to the Intel 1.5 Micron CHMOS III Cell Library," provides an overview of the Intel 1.5 Micron CHMOS III Cell Library, including descriptions of the different types of cells in the library.
- Chapter 2, "Introduction to the Intel Design Environment," describes the Intel cell-based ASIC design flow, available Computer Aided Engineering (CAE) workstation tools and libraries, and Intel provided design support and services.
- Chapter 3, "The Intel 1.5 Micron CHMOS III Cell Library," provides data sheets for all fixed height, variable width cells in the Intel 1.5 Micron CHMOS III Cell Library, including SSI/MSI functions, telescoping cells, and I/O cells. System specifications for the cell library are also presented.
- Chapter 4, "VLSiCEL Elements and LSI Functions," provides data sheets for VLSiCEL elements and LSI function cells in the Intel 1.5 Micron CHMOS III Cell Library, including the 80C51BH Microcontroller Core cells, Microprocessor Support Peripheral Family cells, and memory cells.
- Appendix A, "Packaging," presents a matrix of standard package types available for use with Intel cell-based ASICs.
- Appendix B, "Terms and Definitions," contains definitions of cell specification parameters which appear in the Intel 1.5 Micron CHMOS III Cell Library data sheets.
- Appendix C, "Cell Reference Guide," provides an index of cells in the Intel 1.5 Micron CHMOS III Cell Library. These cells are listed alphabetically and include the cell description, grid count, and page number of the cell data sheet.

TABLE OF CONTENTS

Page

APPENDIX C
CELL REFERENCE GUIDE

Figures

Tables

Introduction to the Intel 1.5 Micron CHMOS III Cell Library

1

CHAPTER 1
INTRODUCTION TO THE INTEL 1.5 MICRON CHMOS III CELL LIBRARY

The Intel 1.5 Micron CHMOS III Cell Library provides customers with the building blocks necessary to design complex semicustom integrated circuits. The 1.5 Micron CHMOS III Cell Library is composed of pre-designed, fully characterized equivalents of common circuit elements and Intel standard products. The library includes SSI, MSI, and LSI circuit elements commonly used in system design. In addition, the library contains VLSiCEL elements, functional equivalents of Intel standard microcontroller, microprocessor, and microprocessor support peripheral products.

FEATURES/BENEFITS

- Over 150 SSI/MSI/LSI logic functions.
- A comprehensive cell library provides a wide range of cell-based ASIC solutions. The library is highlighted by VLSiCEL elements, cell versions of popular Intel standard microprocessors, microcontrollers, and microprocessor support peripherals. VLSiCEL elements offer the highest level of microcomputer-based system integration. Intel's cell-based design methodology offers customers the ability to use predefined circuit elements as building blocks to design complex circuits. The current library includes:

80C51BH	8-Bit Microcontroller
82C37A	Programmable DMA Controller
82C54	Programmable Interval Timer
82C59A	Programmable Interrupt Controller
82C84A	8086 Clock Generator
82C284	80286 Clock Generator
82C88	8086 Bus Controller
82288	80286 Bus Controller

  A complete set of test vectors is provided for each VLSiCEL building block, providing a guaranteed 0.1% AQL (Acceptable Quality-Level) or better.
- The UC51 Emulator Design Kit facilitates hardware and software debug of 80C51BH core plus ASIC designs.
- User-configurable n-bit counters, registers, multipliers, and magnitude comparators built from "telescoping" cells achieve high performance for repetitive functions.
- CHMOS III—An advanced 1.5 micron, double-layer metal CMOS process technology providing high performance, high density, and low power semicustom integrated circuits with proven manufacturability. The CHMOS III process is also used to produce Intel's 80386 and 80C51BH high volume standard products.
- 0.7 ns typical gate delay for a 2-input NAND, fanout of 2.
- 65 MHz typical D flip-flop toggle frequency.
- CMOS, TTL, and Schmitt Trigger compatible I/O cells available with a variety of drive levels and ESD protection to 2000V.

- A complete set of packaging options with lead counts up to 208 pins. Special packaging configurations and higher pin count packages are available upon request.
- The Intel Design Environment provides a comprehensive set of CAE/CAD tools, logic libraries, and customer support and design services that enable users without IC design expertise to design their own cell-based ASICs.
- Intel's 1.5 Micron CHMOS III Cell Library is fully supported on Mentor and Daisy compatible engineering workstations. Mainframe simulation capability is supported through Intel technology centers and direct dial-up to Intel factory mainframes.

CELL-BASED DESIGN

Why Cell-Based ASICs?

Semicustom integrated circuits are designed from a variety of functional building blocks ranging in complexity from individual logic gates to LSI and VLSI functions. Cell-based ASICs offer the highest level of semicustom integration and are capable of implementing complex VLSI functions (microprocessors and microcontrollers). They also offer high performance, increased functionality and better silicon utilization because the individual cells have been hand-packed to the highest possible densities. Better silicon utilization means lower-cost production in high volume. Full custom ICs can provide the same benefits as cell-based ICs. However, while full custom designs often require years to develop, semicustom chips can be developed in weeks or months. Well-characterized, easy-to-use automated design methodologies also typlify semicustom chip development, making ASIC design accessible to system engineers without specialized IC design experience. System manufacturers realize a faster time to market, thus giving more time to concentrate on system rather than IC issues.

Why Intel?

Intel believes that to successfully serve its ASIC customers, it must provide customers with a comprehensive product offering, advanced manufacturing capabilities, a complete CAE tool set, and design services to support the entire ASIC design process.

- Product offering. Intel's ASIC product offering includes programmable logic devices, gate arrays and cell-based ICs, and libraries which contain ASIC versions of Intel standard products.
- Manufacturing expertise. Intel ASIC manufacturing draws on the recognized strengths of Intel CMOS technology, advanced packaging, and a demonstrated expertise in assembly and test.
- Design tools. Customers may access the Intel libraries on a variety of platforms, including the Daisy Systems and Mentor Graphics compatible workstations. Simulations for complex designs are supported on mainframes through Intel Technology Centers and direct dial-up to the Intel factory. The UC51-EDK provides emulation capability for UC51-based designs.
- Design services. Intel provides complete documentation for ASIC product lines. Technology centers offer comprehensive hands-on training courses. And both the gate array and cell-based product lines are fully second sourced.

What is a Standard Cell?

A standard cell can be thought of as a well characterized module containing an individual, independent, logic circuit. It is a complete functional block with predesigned and precharacterized logic. Intel has designed these cells for optimum electrical performance and silicon utilization. The standard SSI/MSI cells in the library have been designed with a fixed-height and variable-width configuration. These cells are arranged horizontally in rows with routing channels on either side. The height of these routing channels is variable, and is determined by required metalization interconnect between the cells.

Customers who design with standard cells need only look at a "black box" view of the functions. Knowledge of or training on gate/transistor level functionality is not necessary, making the cell-based approach similar to designing with commodity logic or standard products.

Figure 1-1 is an example of a standard cell.

Large scale functions including the VLSiCEL elements and Intel's special function cells are designed as "both" variable-width and variable-height cell structures.

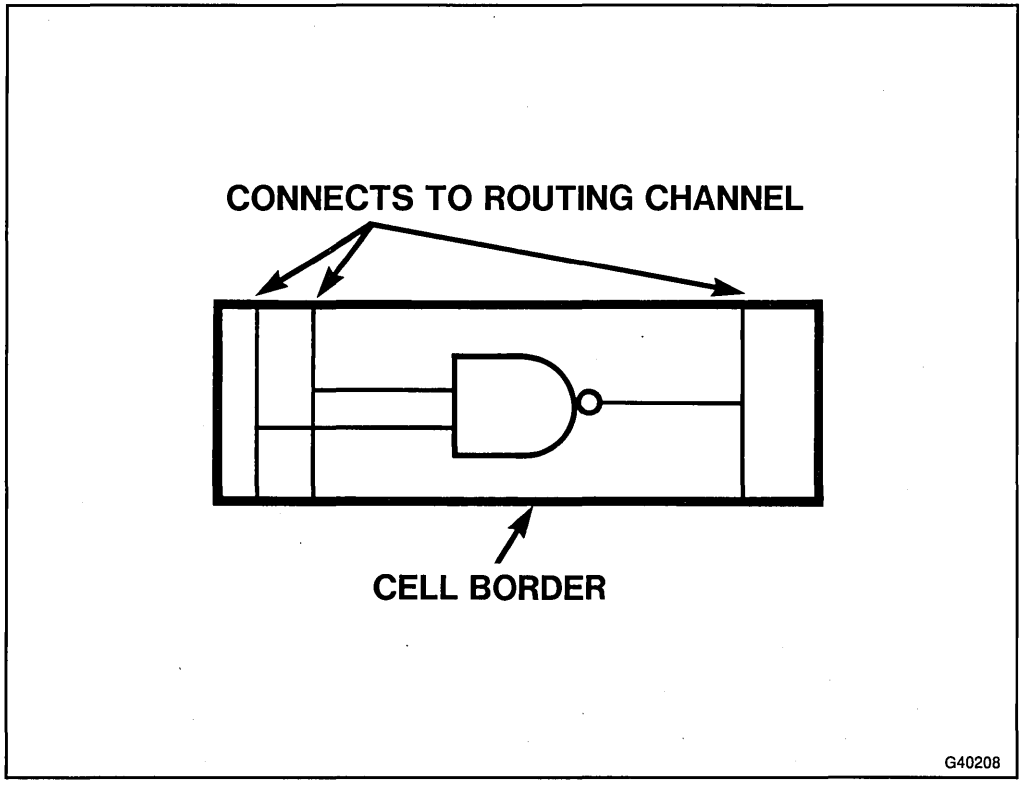

Figure 1-1. Example Standard Cell

An Example of a Cell-Based Design

Figure 1-2 depicts a 25,000 "gate" cell-based design where a gate is defined as equal to 4 transistors (the typical equivalent complexity of a 2-input NAND function). When VLSiCEL and special function cells are used in a cell-based ASIC, higher densities are achieved via the large, custom-designed cells. Intel cell-based ASICs often have 100,000 or more transistors.

CELL TYPES

Standard Cells

The 1.5 Micron CHMOS III Cell Library is composed of over 150 hard-wired basic logic building blocks. These standard cells represent SSI and MSI cells, and are as easy to use as their commodity logic counterparts.

The cell library offers an extensive variety of random logic cells. Included in this category are AND, OR, NAND, NOR, AND-OR, AND-OR-INVERT, EXCLUSIVE OR and EXCLUSIVE NOR gates. Inverters and buffers are available with normal drive, high drive, or 3-state outputs.

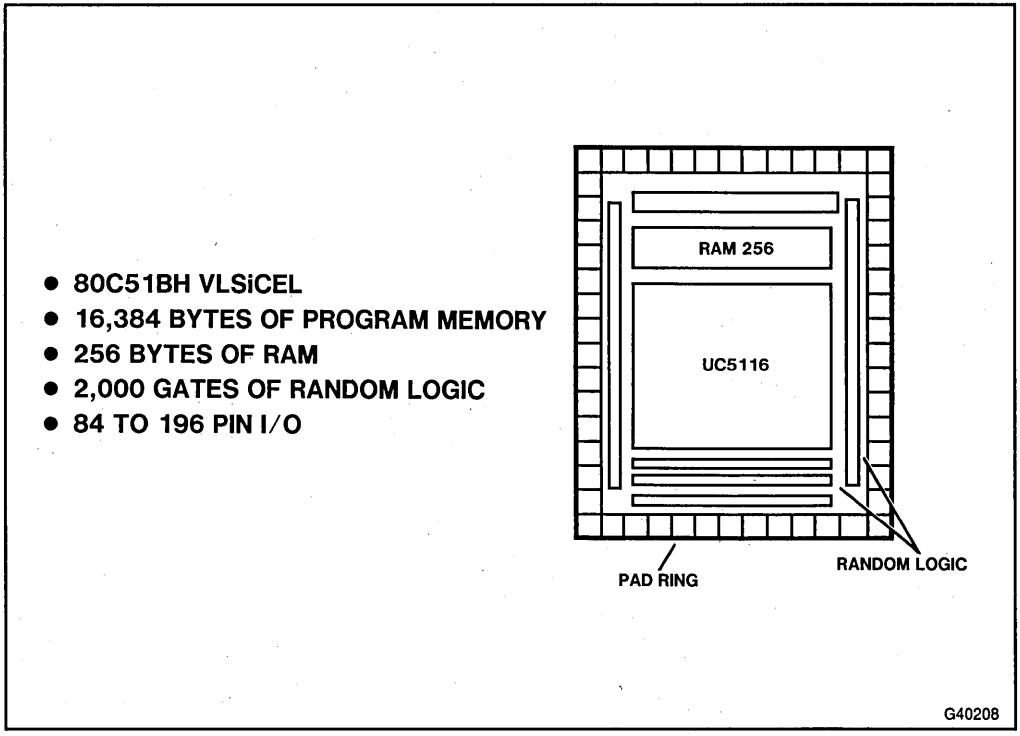

Figure 1-2. Example Cell-Based Design

The Intel cell library contains a broad range of flip-flops and latches. Flip-flops include D, JK, and Toggle; latches include transparent, SR, and $\overline{SR}$. All bistable devices in the Intel 1.5 Micron CHMOS III Cell Library contain an asynchronous master reset input to aid in system design. Flip-flop and latch configurations provide enable, 3-state, scan input, and set functionality. Other standard cell functions in the Intel 1.5 Micron CHMOS III Cell Library include multiplexers, decoders/demultiplexers and a parity generator/checker.

Telescoping Cells

Registers, shift registers, counters, adders, and magnitude comparators are all available in the Intel 1.5 Micron CHMOS III Cell Library as "telescoping" cells. Telescoping cells provide silicon-efficient, user-configurable implementation of repetitive logic functions.

A telescoping cell is designed with all input pins and output pins on opposite sides of the cell. Because the outputs from one telescoping cell align with the inputs of another, multistage devices can be defined by the designer without the need for routing channels. Thus, telescoping cells enhance cell-to-cell continuity in a design, improve the performance of the circuit, and greatly decrease the area of silicon required to implement a function.

Designing a telescoping multistage device may require three types of telescoping cells: body cells, control cells, and cap cells. Body cells provide the basic function required by a telescoping component. Control cells provide an interface between a body cell and an external network. Cap cells are used as a driver for any final output (such as carry-out) related to the overall operation of the device. The use of cap cells is optional.

In Figure 1-3, a 4-bit counter designed without the use of telescoping cells is compared to an implementation which uses telescoping cells. In the example without telescoping cells the design requires the use of 4 routing channels. The 4-bit counter which has been designed using Intel's telescoping cells requires no routing channels. The silicon area savings is approximately equal to the area required to route an additional 20 gates of logic. Also, the elimination of interconnect delays due to routing significantly improves the performance of the counter circuit.

Cluster Macros

Intel provides customers with the capability to group cells which when placed together perform a higher level function. During the layout phase of the design, these cells are physically placed together on-chip—minimizing delays due to interconnect. These cell groups, or cluster macros, are particularly useful for controlling critical path timing.

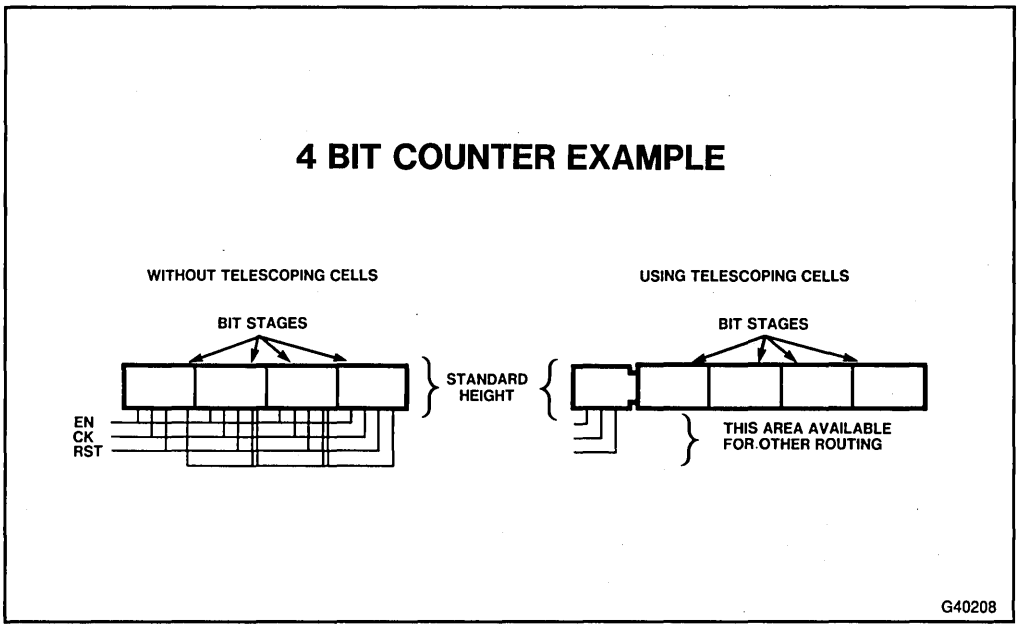

Figure 1-3. Example 4-Bit Counter

I/O Cells

The Intel cell library contains over 30 types of I/O buffer cells. Input, output, and I/O cells are available in TTL or CMOS compatible configurations. Input cells are available in both inverting or non-inverting configurations, and with Schmitt Trigger inputs. Each type of input cell contains bonding pads as well as input static protection networks. Output cells are also available in both inverting or non-inverting configurations and with open drain and 3-state outputs. Output cells include bonding pads and output static protection networks. ESD protection to 2000V is provided.

Table 1-1 shows the available I/O cells and the associated options.

Memory Cells

The most popular Static RAM sizes are available as standard blocks in the cell library. All RAM cells feature byte-wide organization, with densities ranging from 512 to 8K bits.

VLSiCEL Elements

VLSiCEL building blocks provide the customer with the ability to use Intel standard products in their design. The VLSiCEL elements are captured and simulated as complete functions with fully supported simulation models. Intel has addressed the long-standing test issues that have prevented the incorporation of embedded microprocessors and complex functions into

Table 1-1. Available I/O Cells and Associated Options

I/O Cell Types	Options
Input	TTL and CMOS compatible Inverting/non-inverting buffers Schmitt Trigger inputs Pull-up resistors Normal and high drive
Output	TTL and CMOS compatible Inverting/non-inverting buffers 3-state, open drain, push-pull Multiple output drive levels
Bidirectional	TTL and CMOS compatible 3-state outputs, latched inputs Multiple output drive levels

semicustom ICs by building in elements of design for testability. All VLSiCEL building blocks come with a pre-defined set of test vectors, assuring circuit validation and eliminating test "bottlenecks." Complex chips can be designed in a fraction of the time required for gate-level implementations. Complete cell descriptions are available for each function (see Chapter 4, "VLSiCEL Elements and LSI Functions").

CELL SIZE

The standard cells (SSI, MSI) in the 1.5 Micron CHMOS III Cell Library are fixed-height, variable-width cells. Intel expresses the size of these cells in terms of grids. Grid counts provide a relative measure of the physical size of these cells. The grid count for each cell, indicated on the cell data sheet, can be used to determine with circuit configuration that yields the optimum silicon area for a given design.

Introduction to the Intel Design Environment

2

CHAPTER 2
INTRODUCTION TO THE INTEL DESIGN ENVIRONMENT

Intel's design environment provides the customer with a comprehensive set of CAE/CAD tools, logic libraries, customer support and design services. The design environment enables users without IC design expertise to design their own Application Specific Integrated Circuits (ASICs). The libraries support Intel's three ASIC product lines: Cell-Based, Gate Array, and EPLD. This chapter will focus on the design interface for Intel cell-based ASICs.

AN OVERVIEW OF THE INTEL DESIGN ENVIRONMENT

Intel's design environment includes all the design tools and services required to design cell-based ASICs.

The cell-based ASIC design sequence begins with the entering of the design schematic followed by the generation of a netlist (a netlist defines the interconnections between the cells used in the design). Once a netlist has been specified, simulation tools allow the engineer to evaluate the functionality of the design, including timing verification. The design engineer defines the stimulus to exercise the design and verify performance during the simulation phase. After a successful simulation, automatic place and route tools are used to lay out the design. The design is then re-simulated using the delay times that are computed from the layout database. After a successful resimulation, prototypes are manufactured, tested, and delivered.

During all phases of the design process, Intel provides a wide range of support services. Dedicated regional ASIC specialists provide local design analysis and consultation. Technology centers offer comprehensive customer training and technical support, along with access to the software tools running on a variety of hardware platforms. Extensive documentation is available for all software tools and libraries.

AN OVERVIEW OF THE CELL-BASED DESIGN SEQUENCE

Cell-based ASIC designs can be separated into three major phases: design, layout and verification, and manufacturing.

DESIGN PHASE

The design phase includes device specification, logic design, schematic capture, and simulation of the ASIC device. Figure 2-1 shows the typical flow of events that occur during the design phase of a cell-based ASIC design.

After becoming familiar with the CAE tools and the Intel 1.5 Micron CHMOS III Cell Library, the engineer begins the design process by creating a chip specification. This includes functionality, logic partitioning, and physical requirements (i.e., I/O limitations, packaging,

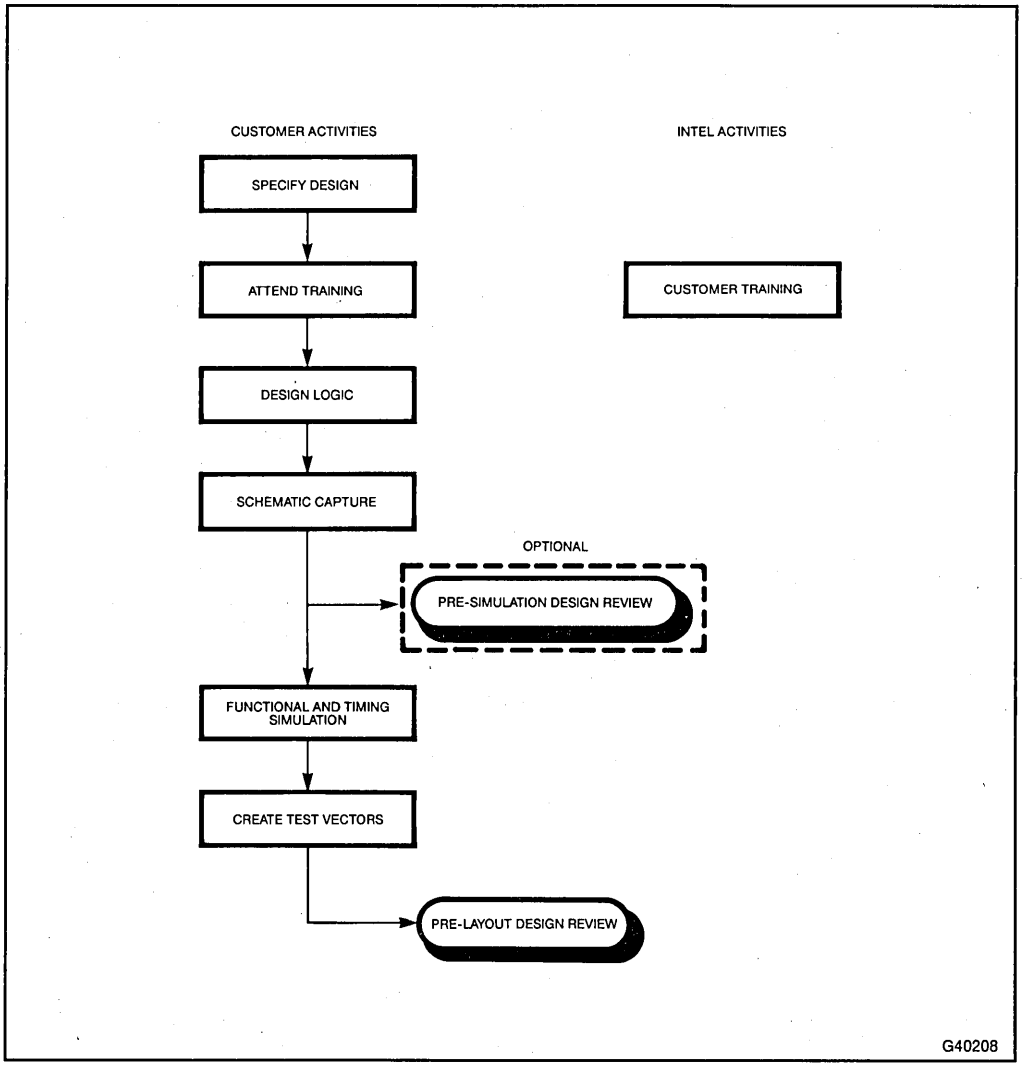

Figure 2-1. Design Phase Flowchart (Technology Center)

power requirements, die size limitations, operating conditions, and performance requirements). Intel recommends that the engineer adhere to several cell-based design guidelines and design for testability considerations, which are covered in the *Introduction to Cell-Based Design Course* (see the end of this chapter). During this phase, customers may also develop functional and timing delay simulation vectors and identify critical paths.

Once the preliminary design is complete, an optional pre-design review can be held. The engineer will then begin selecting cells from the Intel 1.5 Micron CHMOS III Cell Library. Cells are organized into three general categories within the library: VLSiCEL elements,

special function cells, and standard cells, as described earlier in this manual. Data specification sheets can be used to select functions the same way a component catalog is used to evaluate standard components for board level design.

Upon completion of the chip specification and cell selection, the engineer enters the schematic on a CAE workstation. Schematic capture can be done at an Intel technology center or on an Intel-supported workstation at the customer site. Customers may wish to hold an optional pre-simulation design review with Intel at this time.

A functional simulation and a full timing analysis are required to verify that the design will meet performance requirements. Simulation may be done using workstation simulation or Intel-supported mainframe simulators, depending on the complexity of the design. Designs greater than the approximately 10K gates in complexity often require the computational power of a mainframe for efficient simulation. This mainframe capability gives designers maximum flexibility for simulating large designs such as those including VLSiCEL elements. This phase may require several iterations.

During the design and simulation phase, it is important to consider the testability requirements for the circuit. Intel requires customers to produce designs with 100% observability when performing an industry standard node toggle test. Fault grading is an available option.

After the design is successfully simulated, a pre-layout design review must occur before layout can begin. Once approved by both Intel and the customer, the design progresses to the layout and verification phase.

LAYOUT AND VERIFICATION

Figure 2-2 shows the sequence of events in the layout and verification phase. Placement and routing of the ASIC design is performed using automatic place and route software. As a final check Intel factors in the actual delay times as determined from the layout database (this is called back annotation). The design is then resimulated and post- and pre-layout simulation results are compared for consistency. When requirements are met, and both Intel and the customer are satisfied with the results, a final design specification is approved. The design specification becomes the governing document against which prototype and production components are evaluated. The design then enters the manufacturing phase.

MANUFACTURING PHASE

Figure 2-3 shows the sequence of events in the manufacturing phase. After the layout and verification phase has been completed, Intel will produce prototypes. These prototypes will be submitted to the customer for a final review and production approval.

Intel offers rapid turnaround times for its ASIC products. The ASIC circuits are fabricated, tested, sorted, assembled into packages, and tested again as finished devices. Customer-defined test patterns are used to verify the device, and standard parametric tests are used to confirm performance over temperature and supply voltage extremes.

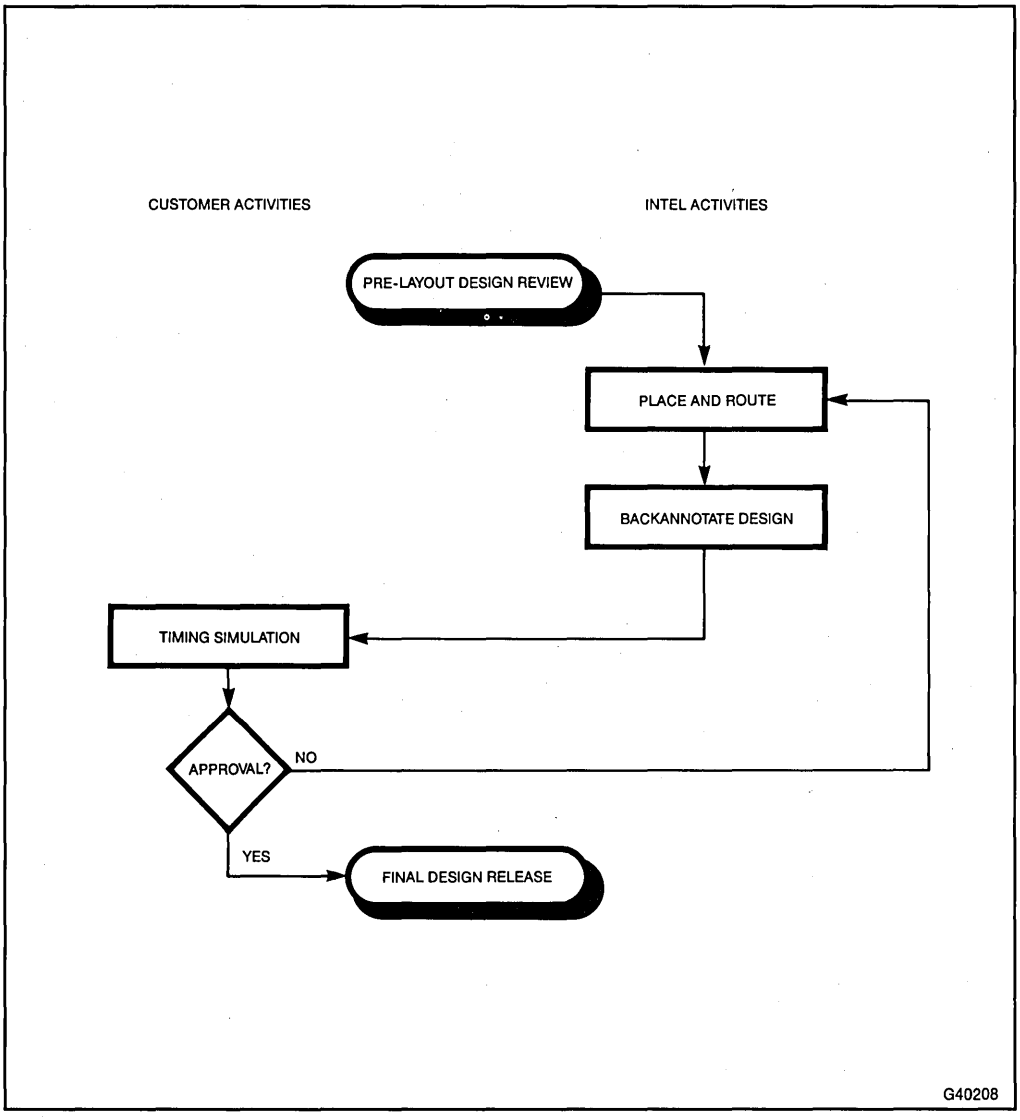

Figure 2-2. Layout and Verification Phase Flowchart

PACKAGING

Intel provides a variety of standard IC packages for use with cell-based ASIC designs. Among the available packaging options are ceramic and plastic Dual In-Line Packages (DIP) with up to 48 pins, Plastic Leaded Chip Carriers (PLCC) with up to 84 pins, ceramic and plastic Pin Grid Arrays (PGA) with up to 180 pins, and ceramic and plastic quad flatpacks for up to 208 pin configurations. Special packages are available upon request. Refer to Appendix A for more information.

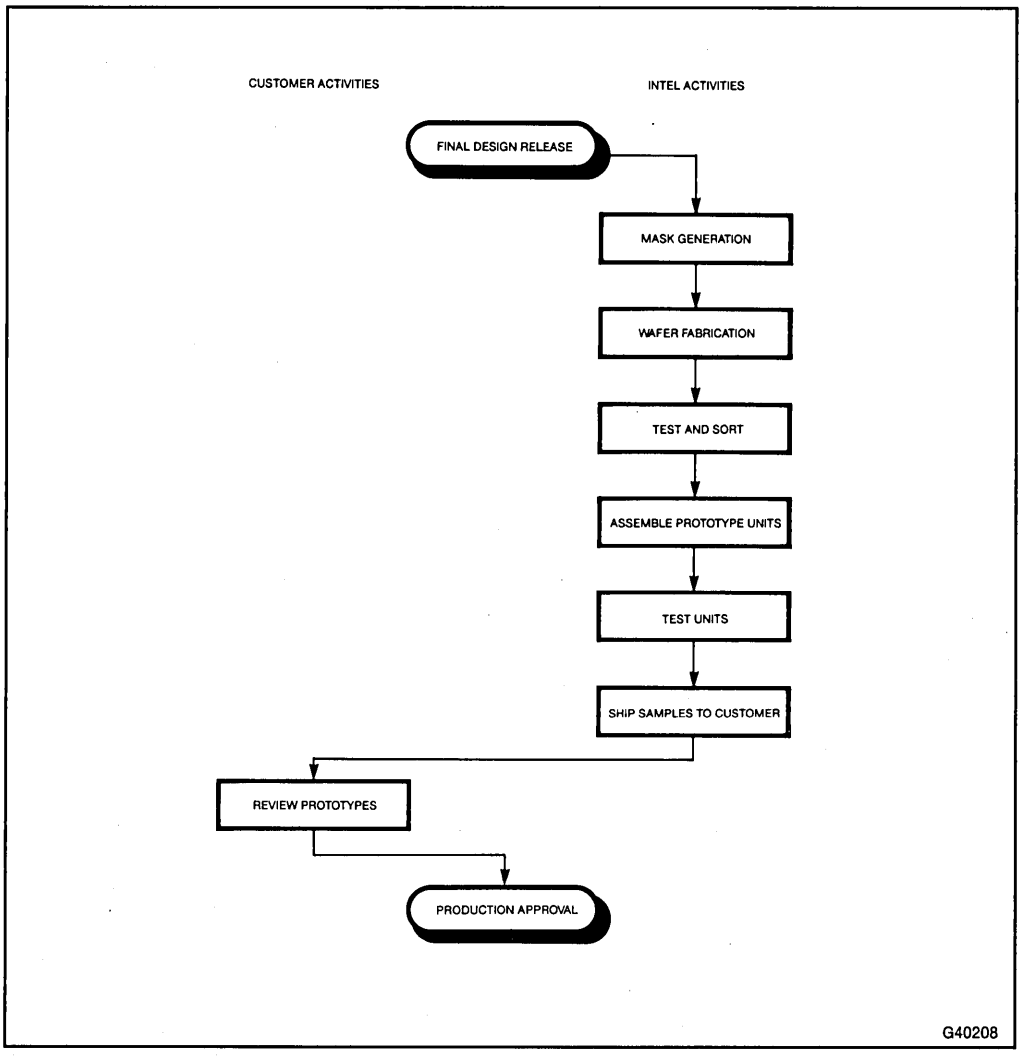

Figure 2-3. Manufacturing Phase Flowchart

QUALITY AND RELIABILITY

Intel is committed to the highest possible standards of quality, reliability and customer satisfaction in its products. All ASIC products must meet the same quality and reliability standards as Intel standard products. Intel insists on building-in quality and reliability for every product from the very beginning of a technology and product development cycle. Strict controls and monitors are applied in the manufacturing process to ensure high quality and reliability. All processes are audited regularly to ensure that they meet specifications. For additional details on Intel's quality and reliability programs, refer to the *Components Quality/Reliability Handbook*, Order Number 210997.

Intel's cell-based products are shipped to a .1% AQL level and less than 200 FITs (Failures In Time).

DESIGN SUPPORT

Intel customers have the option to specify as much or as little design support as needed to complete their ASIC. Table 2-1 describes the two preferred ASIC design interfaces: design tasks performed at the customer's site or at an Intel technology center. Customers may also opt for full service design support.

Intel's design environment provides the necessary design tools and services for all these design interface alternatives. Customers who choose to develop their ASIC on-site port Intel libraries onto their own CAE systems and design the device within their own development environment. Customers who decide to use Intel technology centers for ASIC development take advantage of Intel's on-site CAE systems, libraries, and applications support to assist them during their design effort.

Table 2-1 lists the major steps required to execute a design and specifies the responsibilities for each party.

Table 2-1. Design Sequence Responsibilities

Activity	Technology Center	Customer Site
Pre-design Start Design Review	Intel/Customer	Intel/Customer
Cell Selection	Intel/Customer	Customer
Schematic Capture	Intel/Customer	Customer
Simulation (Functional)	Intel/Customer	Customer
Simulation (Timing)	Intel/Customer	Customer
Pre-Layout Design Review	Intel/Customer	Intel/Customer
Test Vector Generation	Intel/Customer	Intel/Customer
Autolayout	Intel	Intel
Post-Layout Simulation	Intel/Customer	Intel/Customer
Post-Layout Approval	Intel/Customer	Intel/Customer
Mask Generation	Intel	Intel
Wafer Fab	Intel	Intel
Assembly/Test	Intel	Intel
Prototype Approval	Customer	Customer

COMPUTER AIDED ENGINEERING (CAE) TOOLS

The 1.5 Micron CHMOS III Cell Library runs on all engineering workstations from Daisy Systems and Mentor Graphics. This wide range of compatibility gives designers the flexibility to execute cell-based designs using a variety of CAE hardware.

MAINFRAME-BASED SIMULATION

Simulation requirements for complex designs are often best served by mainframe computational power. Using an Intel mainframe simulator, customers can run simulations that are too time consuming or not possible to do using a desktop workstation environment. An integrated design database allows for portability between the mainframe environment and the workstation environment.

Intel's mainframe computers may be accessed through dial-up from the customer site or via an Intel technology center.

INTEL TECHNOLOGY CENTERS

Intel technology centers offer training classes, design consultation and technical workstation support for semicustom chip design, cell-based design libraries, and CAE workstations as well as access to workstations for schematic capture and simulation. Customers may use the technology centers to take advantage of Intel's on-site systems, libraries and services. Each center is equipped with IBM PC-ATs, and Daisy Systems and Mentor Graphics workstations. Direct access to the Intel mainframe is also available for efficient simulation of complex designs.

Training classes and technical support are available from Intel's technology center ASIC specialists. The *Introduction to Intel Cell-Based Design Course* consists of both lecture and labs emphasizing "hands-on" experience. Lectures address Intel-specific design practices; labs offer hands-on training in the Intel design environment. Contact the Intel technology center nearest you or your local Intel field sales office for scheduling.

INTEL TECHNOLOGY CENTERS

CALIFORNIA
Intel Technology Center
3065 Bowers Avenue
Santa Clara, CA 95051
Tel: (408) 765-2252

MASSACHUSETTS
Intel Technology Center
3 Carlisle Rd.
Westford, MA 01886
Tel: (617) 692-3222

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Intel Technology Center
Piper's Way
Swindon SN3IRJ
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The Intel 1.5 Micron CHMOS III Cell Library

3

ADVANCE INFORMATION

CHAPTER 3
THE INTEL 1.5 MICRON CHMOS III CELL LIBRARY

This chapter provides data sheets for all fixed height, variable width cells in the Intel 1.5 Micron CHMOS III Cell Library, including SSI/MSI functions, telescoping cells, and I/O cells. The data sheets are preceded by system specifications for the cell library. Information provided includes Absolute Maximum Ratings and Recommended Operating Conditions, and Measurement Conditions. A guide to interpreting the cell data sheets is also provided. Data sheets for VLSiCEL elements and LSI functions are provided in Chapter 4.

CELL LIBRARY SYSTEM SPECIFICATIONS

Table 3-1. Absolute Maximum Ratings

Case Temperature Under Bias	
Plastic	−40°C to +85°C
Ceramic	−55°C to +125°C
Storage Temperature	−65°C to +150°C
DC Supply Voltage (VDD)	0 V to 7.0 V
Voltage to Any Pin with Respect to Ground	−0.5 V to VDD + 0.5 V
Power Dissipation	1.0 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3-2. Recommended Operating Conditions

DC Supply Voltage (VDD)	+4.5 V to +5.5 V
Case Temperature	0°C to +70°C

NOTICE: Cell performance as noted on the cell data sheets are guaranteed when the device is operated within these parameters.

MEASUREMENT CONDITIONS

Measurement conditions for propagation delay times and 3-state enable and disable times for I/O buffer cells are provided in this section. Voltage waveforms are used to illustrate the data points at which the parameters were determined. Data points were established at

the following conditions over the recommended operating supply voltage and temperature ranges:

1. Input rise and fall times = 1 ns.
2. For open drain output buffers, all propagation delays were measured with a 2 KΩ pull-up resistor to VDD on the output.
3. For 3-state output and bi-directional I/O buffers, enable and disable times to and from the logic low-level were measured with a 1 KΩ resistance tied to VDD at the output. Enable and disable delays to and from the logic high-level were measured with a 1 KΩ resistance tied to VSS at the output.

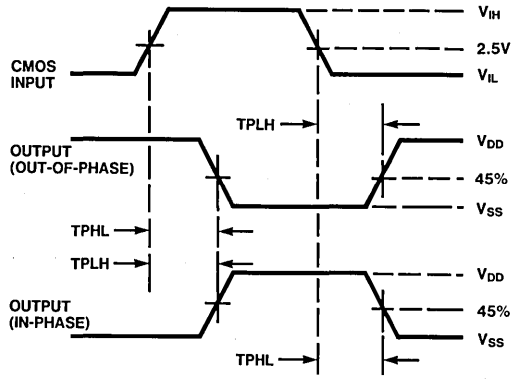

Figure 3-1. CMOS Input and Bi-Directional I/O Cell Input Propagation Delay Times

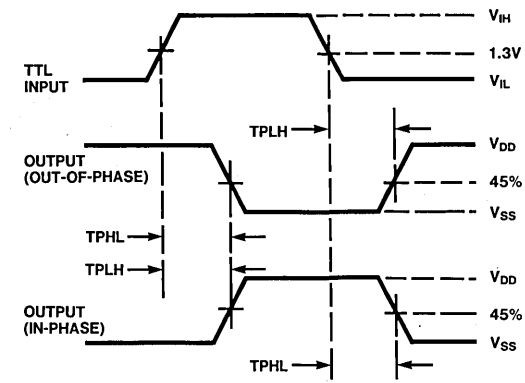

Figure 3-2. TTL Input and Bi-Directional I/O Cell Input Propagation Delay Times

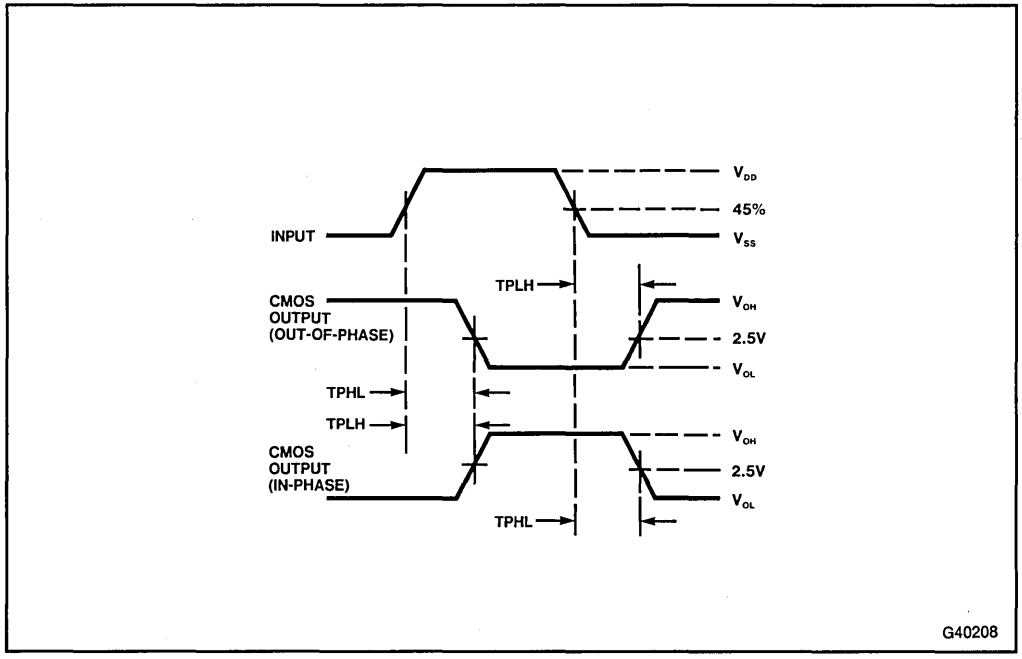

Figure 3-3. CMOS Output and Bi-Directional I/O Cell Output Propagation Delay Times

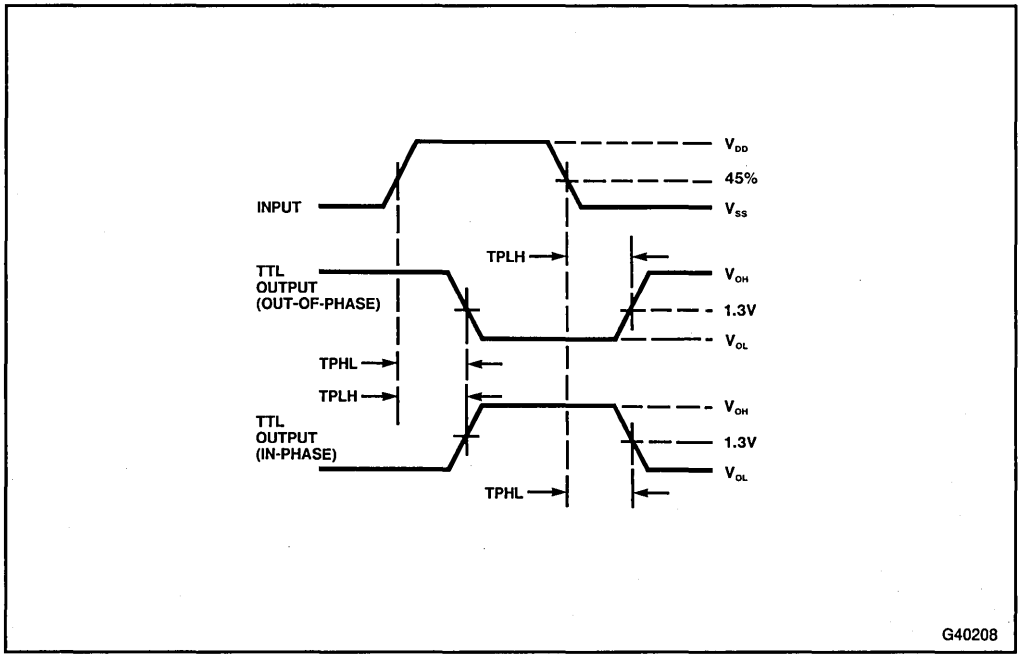

Figure 3-4. TTL Output and Bi-Directional I/O Cell Output Propagation Delay Times

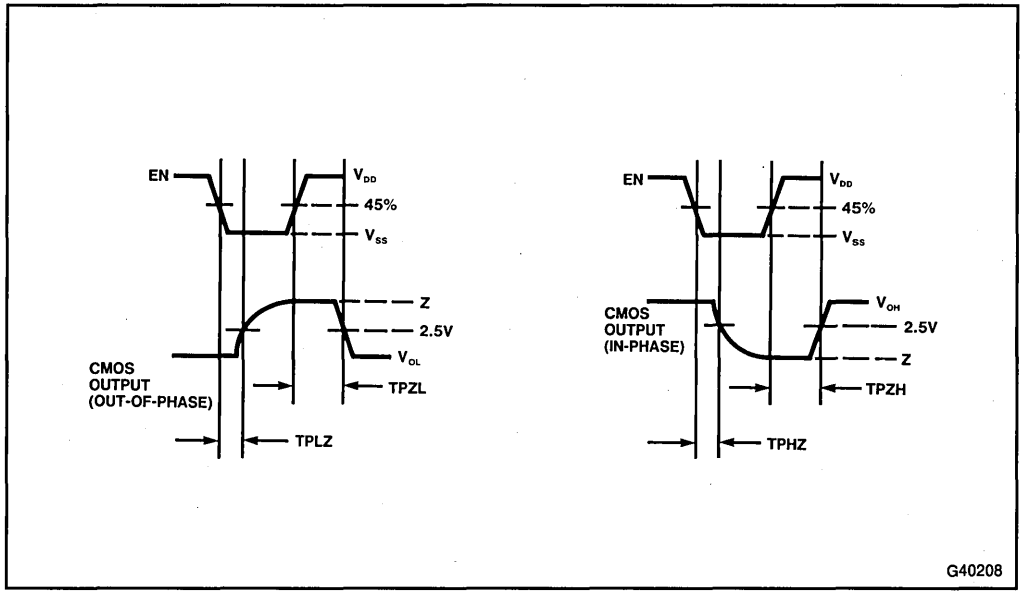

Figure 3-5. CMOS 3-State Output and Bi-Directional I/O Cell Enable and Disable Times

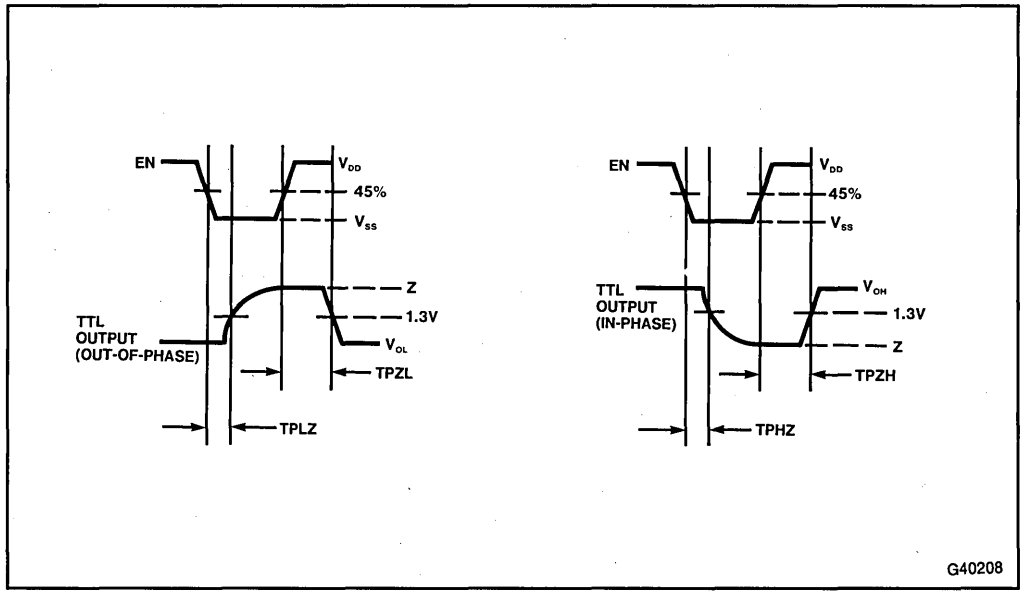

Figure 3-6. TTL 3-State Output and Bi-Directional I/O Cell Enable and Disable Times

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INTERPRETING CELL DATA SHEETS

This section explains how to interpret the individual cell data sheets given in this chapter. Cell types CULB (Figure 3-7) and PCIO (Figure 3-8) are used to illustrate the various components of the data sheets.

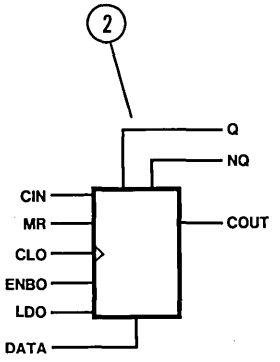
1. Data Sheet Heading—gives the cell name and a general functional categorization of the cell.
2. Logic Symbol—a symbolic representation of the cell. Where possible, the symbols given will match those presented by Intel's engineering workstation models.
3. Functional Description—a complete textual description of the cell's functionality.
4. Grid Count—Intel expresses the size of its cells in terms of grids. A cell's grid count provides a relative measure of its physical size. Grid counts can be used to determine optimum silicon utilization of a given design.
5. Logic Table—provides a tabulation relating all output logic states to all necessary possible combinations of input logic states to completely characterize the functionality of the cell. The following symbols are used in cell logic tables:

   LEGEND

   0 — low-level (steady state)
   1 — high-level (steady state)
   X — don't care state
   Z — high impedance (off) state of a 3-state output
   ↑ — transition from low-to-high level
   ↓ — transition from high-to-low level
   Q_0 — previous level of Q before the most recent transition state
   a — the steady state level at input a
   na — complement state of input a

   Where necessary, a descriptive representation of logic functionality is used.
6. Pin Description Table—a functional description of the cell's pins; cell pins are illustrated on the logic symbol. For telescoping cells, two categories of pins are given, external pins and telescoping interconnect pins. External pins provide the functional connection to and from the telescoping function. Telescoping interconnect pins are used for connecting together the various telescoping cell building blocks. These pins cannot be used outside of a telescoping function.

CULB — TELESCOPING UP COUNTER BODY (1)



5 Logic Table

Inputs						Outputs		
CLO	CIN	DATA	LDO	ENBO	MR	Q	NQ	COUT
1	X	X	X	X	1	0	1	0
0	0	X	X	X	0	Q_0	NQ_0	0
0	1	X	X	X	0	Q_0	NQ_0	Q_0
↑	X	0	1	X	0	0	1	0
↑	0	1	1	X	0	1	0	0
↑	1	1	1	X	0	1	0	1
↑	0	X	0	0	0	Q_0	NQ_0	0
↑	1	X	0	0	0	Q_0	NQ_0	Q_0
↑	0	X	0	1	0	Q_0	NQ_0	0
↑	1	X	0	1	0	NQ_0	Q_0	NQ_0
1	0	X	X	X	0	Q_0	NQ_0	0
1	1	X	X	X	0	Q_0	NQ_0	Q_0

NOTES: — A CLO signal transition to 1 when MR is 1 will be transparent to the user when the control cell is attached to a group of body cells.

— COUT = CIN • Q; a cap cell (CULP) must be used if COUT is to be connected to circuitry external to a telescoping block.

CULB Description

3

Function: Telescoping Up Counter Body
Grid Count: 338

4

6 Pin Description

External Pins	
DATA	Data Input
Q	Output
NQ	Complemented Output
Telescoping Interconnect Pins	
CLO	Clock Input
CIN	Carry Input
ENBO	Enable Input
LDO	Load Input
MR	Master Reset Input (Asynchronous, Active High)
COUT	Carry Output

G30176

Figure 3-7. CULB Data Sheet

7. D.C. Characteristics Table—provides all applicable voltage, current, and pull-up resistance specifications for Input/Output cells over the stated operating conditions. These specifications are given to ensure proper system integration of cell-based ASICs.
8. Input Capacitance Table—provides the load capacitance value for all input signals of the cell. This parameter is used when calculating the propagation delay of a given signal path.
9. 3-State Output Capacitance Table—provides the off state load capacitance value for all applicable outputs of 3-state and open drain cells. This parameter is used when calculating the propagation delay of a bused signal path.
10. A.C. Characteristics Heading—gives the operating conditions over which setup and hold times and propagation delay specifications are valid. In order to make the cell-based design process as accurate and simple as possible, A.C. Characteristic parameters are specified at three data points: minimum, typical, and maximum.
11. Setup and Hold Times Table—provides applicable setup and hold parameters for edge-triggered and latching cells.

D.C. Characteristics at 0–70°C, 5V+/−10% (7)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	3.5			V	
VIL			1.2	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS
VOH	4.0			V	IOH = −2.4 mA
VOL			0.4	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF
EN	0.30	pF
PAD	2.40	pF

(8)

3-State Output Capacitance

Input Name	Max.	Units
PAD(z)	2.40	pF

(9)

(10)

A.C. Characteristics at 0–70°C, 5V+/−10% (11)

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
PAD to EN	2.0	3.0	5.5	1.2	2.6	6.0	ns

G40208

Figure 3-8. PCIO Data Sheet

12. Propagation Delay Tables—two tables are given for cell propagation delay, intrinsic propagation delay and load dependent delay. The intrinsic propagation delay is the delay through the cell logic, independent of external loading effects. The load dependent delay is the delay associated with external capacitive loading and is specified in terms of ns/pF. Together with the summation of input capacitance values for all cells connected to a given cell output, these tables are used to calculate path delays for that output. A formula is given below:

    Propagation Delay = Intrinsic Propagation Delay + Σ Input Capacitance • Load Dependent Delay

Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	1.0	1.8	4.1	ns
Tphl	IN to PAD	0.9	2.0	4.8	ns
Tplh	PAD to OUT	1.4	2.6	5.0	ns
Tphl	PAD to OUT	1.2	2.5	5.7	ns
Tpzh	EN to PAD	0.8	1.9	5.1	ns
Tpzl	EN to PAD	0.6	1.3	3.0	ns
Tphz	EN to PAD	1.2	2.2	4.5	ns
Tplz	EN to PAD	0.9	1.5	3.0	ns

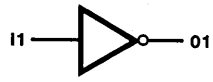
Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PAD	0.10	0.10	0.20	0.10	0.10	0.20	ns/pF
OUT	0.40	0.80	2.10	0.40	0.70	1.20	ns/pF

G40208

Figure 3-8. PCIO Data Sheet (Cont'd.)

INVN, INVNH — INVERTERS



Logic Table

Inputs	Outputs
I1	O1
0 1	1 0

INVN Description

Function: Inverter, Normal Drive
Grid Count: 26

INVNH Description

Function: Inverter, High Drive
Grid Count: 39

Pin Description

I1 O1	Data Input Output

Input Capacitance

Input Name	Max.	Units
I1 INVN	0.30	pF
I1 INVNH	0.60	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

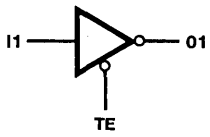
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
INVN I1 to O1	0.1	0.2	0.3	0.2	0.2	0.3	ns
INVNH I1 to O1	0.1	0.2	0.3	0.2	0.2	0.3	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
O1 INVN	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF
O1 INVNH	0.16	0.35	0.93	0.22	0.32	0.55	ns/pF

INVTE — 3-STATE INVERTER



Logic Table

Inputs		Outputs
I1	TE	O1
0	0	1
1	0	0
X	1	Z

INVTE Description

Function: 3-State Inverter with Active Low Output Enable, Normal Drive
Grid Count: 52

Pin Description

I1	Data Input
TE	3-State Enable Input
O1	Output

Input Capacitance

Input Name	Max.	Units
I1	0.50	pF
TE	0.40	pF

3-State Output Capacitance

Output Name	Max.	Units
O1(z)	0.25	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

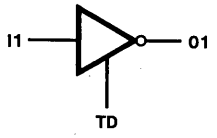
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	I1 to O1	0.2	0.4	1.1	ns
Tphl	I1 to O1	0.4	0.6	1.2	ns
Tpzh	TE to O1	0.6	1.0	2.4	ns
Tpzl	TE to O1	0.6	1.2	3.1	ns
Tphz	TE to O1	0.6	1.2	3.1	ns
Tplz	TE to O1	0.6	1.0	2.4	ns

Load Dependent Delay

Parameter	Output Name	Min.	Typ.	Max.	Units
Tplh	O1	0.32	0.75	2.06	ns/pF
Tphl	O1	0.44	0.72	1.38	ns/pF
Tpzh	O1	0.32	0.75	2.06	ns/pF
Tpzl	O1	0.44	0.72	1.38	ns/pF

INVTD — 3-STATE INVERTER



Logic Table

Inputs		Outputs
I1	TD	O1
0	1	1
1	1	0
X	0	Z

INVTD Description

Function: 3-State Inverter with Active High Output Enable, Normal Drive
Grid Count: 52

Pin Description

I1	Data Input
TD	3-State Enable Input
O1	Output

Input Capacitance

Input Name	Max.	Units
I1	0.50	pF
TD	0.25	pF

3-State Output Capacitance

Output Name	Max.	Units
O1(z)	0.25	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

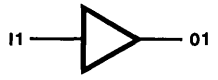
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	I1 to O1	0.2	0.4	1.3	ns
Tphl	I1 to O1	0.3	0.5	1.0	ns
Tpzh	TD to O1	0.6	1.0	2.4	ns
Tpzl	TD to O1	0.6	1.2	3.1	ns
Tphz	TD to O1	0.6	1.2	3.1	ns
Tplz	TD to O1	0.6	1.0	2.4	ns

Load Dependent Delay

Parameter	Output Name	Min.	Typ.	Max.	Units
Tplh	O1	0.32	0.75	2.06	ns/pF
Tphl	O1	0.44	0.72	1.37	ns/pF
Tpzh	O1	0.32	0.75	2.06	ns/pF
Tpzl	O1	0.44	0.72	1.38	ns/pF

BUF, BUFH — BUFFERS



Logic Table

Inputs	Outputs
I1	O1
0 1	0 1

BUF Description

Function: Buffer, Normal Drive
Grid Count: 39

BUFH Description

Function: Buffer, High Drive
Grid Count: 52

Pin Description

I1 O1	Data Input Output

Input Capacitance

Input Name	Max.	Units
I1 BUF	0.10	pF
I1 BUFH	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

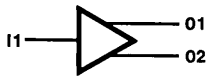
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
BUF I1 to O1	0.4	0.6	1.2	0.3	0.7	1.8	ns
BUFH I1 to O1	0.4	0.5	1.0	0.3	0.6	1.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
O1 BUF	0.33	0.73	1.95	0.46	0.68	1.17	ns/pF
O1 BUFH	0.15	0.35	0.93	0.22	0.32	0.57	ns/pF

BUF2 — BUFFER WITH DUAL OUTPUT



Logic Table

Inputs	Outputs
I1	O1 O2
0 1	0 0 1 1

BUF2 Description

Function: Buffer with Dual Output, Normal Drive
Grid Count: 52

Pin Description

I1 O1, O2	Data Input Outputs

Input Capacitance

Input Name	Max.	Units
I1	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

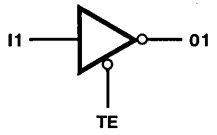
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
I1 to O1, O2	0.3	0.5	1.0	0.3	0.6	1.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
O1, O2	0.33	0.74	1.95	0.46	0.68	1.17	ns/pF

BUFTE — 3-STATE BUFFER



Logic Table

Inputs		Outputs
I1	TE	O1
0	0	0
1	0	1
X	1	Z

BUFTE Description

Function: 3-State Buffer with Active Low Output Enable, Normal Drive
Grid Count: 65

Pin Description

I1	Data Input
TE	3-State Enable Input
O1	Output

Input Capacitance

Input Name	Max.	Units
I1	0.10	pF
TE	0.40	pF

3-State Output Capacitance

Output Name	Max.	Units
O1(z)	0.25	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

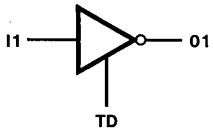
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	I1 to O1	0.6	1.0	2.4	ns
Tphl	I1 to O1	0.6	1.2	3.1	ns
Tpzh	TE to O1	0.6	1.0	2.4	ns
Tpzl	TE to O1	0.6	1.2	3.1	ns
Tphz	TE to O1	0.6	1.2	3.1	ns
Tplz	TE to O1	0.6	1.0	2.4	ns

Load Dependent Delay

Parameter	Output Name	Min.	Typ.	Max.	Units
Tplh	O1	0.32	0.75	2.06	ns/pF
Tphl	O1	0.44	0.72	1.38	ns/pF
Tpzh	O1	0.32	0.75	2.06	ns/pF
Tpzl	O1	0.44	0.72	1.38	ns/pF

BUFTD — 3-STATE BUFFER



Logic Table

Inputs		Outputs
I1	TD	O1
0	1	0
1	1	1
X	0	Z

BUFTD Description

Function: 3-State Buffer with Active High Output Enable, Normal Drive
Grid Count: 65

Pin Description

I1	Data Input
TD	3-State Enable Input
O1	Output

Input Capacitance

Input Name	Max.	Units
I1	0.10	pF
TD	0.25	pF

3-State Output Capacitance

Output Name	Max.	Units
O1(z)	0.25	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	I1 to O1	0.6	1.1	2.5	ns
Tphl	I1 to O1	0.6	1.2	3.0	ns
Tpzh	TD to O1	0.6	1.0	2.4	ns
Tpzl	TD to O1	0.6	1.2	3.1	ns
Tphz	TD to O1	0.6	1.2	3.1	ns
Tplz	TD to O1	0.6	1.0	2.4	ns

Load Dependent Delay

Parameter	Output Name	Min.	Typ.	Max.	Units
Tplh	O1	0.32	0.75	2.06	ns/pF
Tphl	O1	0.44	0.72	1.38	ns/pF
Tpzh	O1	0.32	0.75	2.06	ns/pF
Tpzl	O1	0.44	0.72	1.38	ns/pF

NAN2 — 2 INPUT NAND GATE

Logic Table

Inputs		Outputs
I1	I2	O1
0	X	1
X	0	1
1	1	0

NAN2 Description

Function: 2 Input NAND, Normal Drive
Grid Count: 39

Pin Description

I1, I2	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1, I2	0.35	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1, I2 to O1	0.2	0.3	0.6	0.2	0.2	0.4	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.73	1.95	0.44	0.72	1.35	ns/pF

NAN3 — 3 INPUT NAND GATE

Logic Table

Inputs			Outputs
I1	I2	I3	O1
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

NAN3 Description

Function: 3 Input NAND, Normal Drive
Grid Count: 65

Pin Description

I1-I3	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I3	0.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

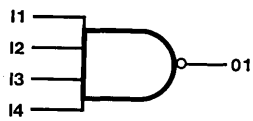
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I3 to O1	0.2	0.4	1.0	0.2	0.3	0.6	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.73	1.96	0.43	0.73	1.42	ns/pF

NAN4 — 4 INPUT NAND GATE



Logic Table

Inputs				Outputs
I1	I2	I3	I4	O1
0	X	X	X	1
X	0	X	X	1
X	X	0	X	1
X	X	X	0	1
1	1	1	1	0

NAN4 Description

Function: 4 Input NAND, Normal Drive
Grid Count: 78

Pin Description

I1-I4	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I4	0.45	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

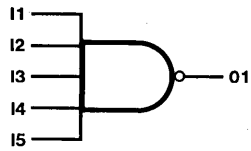
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I4 to O1	0.3	0.6	1.6	0.2	0.3	0.7	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.97	0.40	0.70	1.38	ns/pF

NAN5 — 5 INPUT NAND GATE



Logic Table

Inputs					Outputs
I1	I2	I3	I4	I5	O1
0	X	X	X	X	1
X	0	X	X	X	1
X	X	0	X	X	1
X	X	X	0	X	1
X	X	X	X	0	1
1	1	1	1	1	0

NAN5 Description

Function: 5 Input NAND, Normal Drive
Grid Count: 104

Pin Description

I1-I5	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I5	0.55	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

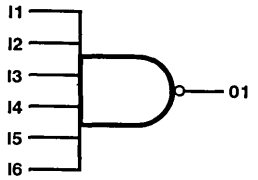
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I5 to O1	0.4	0.9	2.4	0.2	0.5	1.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.75	2.00	0.39	0.70	1.39	ns/pF

NAN6 — 6 INPUT NAND GATE



Logic Table

Inputs						Outputs
I1	I2	I3	I4	I5	I6	O1
0	X	X	X	X	X	1
X	0	X	X	X	X	1
X	X	0	X	X	X	1
X	X	X	0	X	X	1
X	X	X	X	0	X	1
X	X	X	X	X	0	1
1	1	1	1	1	1	0

NAN6 Description

Function: 6 Input NAND, Normal Drive
Grid Count: 117

Pin Description

I1-I6	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I6	0.60	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

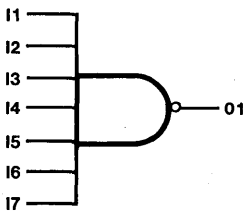
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I6 to O1	0.5	1.2	3.3	0.3	0.6	1.3	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.34	0.76	2.03	0.37	0.68	1.36	ns/pF

NAN7 — 7 INPUT NAND GATE



Logic Table

Inputs							Outputs
I1	I2	I3	I4	I5	I6	I7	O1
0	X	X	X	X	X	X	1
X	0	X	X	X	X	X	1
X	X	0	X	X	X	X	1
X	X	X	0	X	X	X	1
X	X	X	X	0	X	X	1
X	X	X	X	X	0	X	1
X	X	X	X	X	X	0	1
1	1	1	1	1	1	1	0

NAN7 Description

Function: 7 Input NAND, Normal Drive
Grid Count: 169

Pin Description

I1-I7	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I7	0.11	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

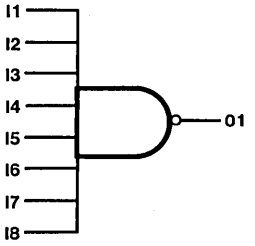
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I7 to O1	0.9	1.7	3.9	0.5	1.1	3.1	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.73	1.96	0.45	0.73	1.39	ns/pF

NAN8 — 8 INPUT NAND GATE



Logic Table

Inputs								Outputs
I1	I2	I3	I4	I5	I6	I7	I8	O1
0	X	X	X	X	X	X	X	1
X	0	X	X	X	X	X	X	1
X	X	0	X	X	X	X	X	1
X	X	X	0	X	X	X	X	1
X	X	X	X	0	X	X	X	1
X	X	X	X	X	0	X	X	1
X	X	X	X	X	X	0	X	1
X	X	X	X	X	X	X	0	1
1	1	1	1	1	1	0	1	0

NAN8 Description

Function: 8 Input NAND, Normal Drive
Grid Count: 182

Pin Description

I1-I8	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I8	0.11	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I8 to O1	0.9	1.7	3.9	0.5	1.2	3.1	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.73	1.96	0.45	0.73	1.39	ns/pF

NOR2 — 2 INPUT NOR GATE

Logic Table

Inputs		Outputs
I1	I2	O1
0	0	1
1	X	0
X	1	0

NOR2 Description

Function: 2 Input NOR, Normal Drive
Grid Count: 52

Pin Description

I1, I2	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1, I2	0.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

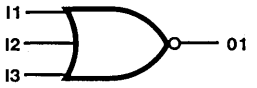
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1, I2 to O1	0.1	0.3	0.9	0.4	0.6	0.9	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.32	0.75	2.06	0.46	0.68	1.19	ns/pF

NOR3 — 3 INPUT NOR GATE



Logic Table

Inputs			Outputs
I1	I2	I3	O1
0	0	0	1
1	X	X	0
X	1	X	0
X	X	1	0

NOR3 Description

Function: 3 Input NOR, Normal Drive
Grid Count: 78

Pin Description

I1-I3	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I3	0.60	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

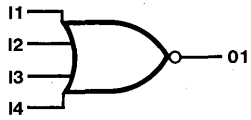
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I3 to O1	0.2	0.6	1.8	0.7	1.1	1.7	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.30	0.72	2.01	0.47	0.70	1.25	ns/pF

NOR4 — 4 INPUT NOR GATE



Logic Table

Inputs				Outputs
I1	I2	I3	I4	O1
0	0	0	0	1
1	X	X	X	0
X	1	X	X	0
X	X	1	X	0
X	X	X	1	0

NOR4 Description

Function: 4 Input NOR, Normal Drive
Grid Count: 104

Pin Description

I1-I4	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I4	0.75	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

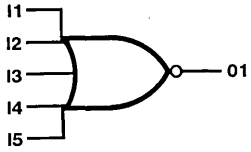
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I4 to O1	0.4	1.0	2.9	1.2	1.6	2.5	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.30	0.73	2.05	0.49	0.74	1.34	ns/pF

NOR5 — 5 INPUT NOR GATE



Logic Table

Inputs					Outputs
I1	I2	I3	I4	I5	O1
0	0	0	0	0	1
1	X	X	X	X	0
X	1	X	X	X	0
X	X	1	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0

NOR5 Description

Function: 5 Input NOR, Normal Drive
Grid Count: 130

Pin Description

I1-I5	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I5	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

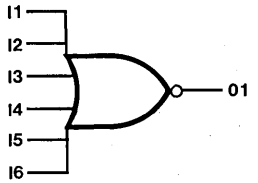
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I5 to O1	0.4	1.0	2.5	0.8	1.5	3.6	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.46	0.68	1.18	ns/pF

NOR6 — 6 INPUT NOR GATE



Logic Table

Inputs						Outputs
I1	I2	I3	I4	I5	I6	O1
0	0	0	0	0	0	1
1	X	X	X	X	X	0
X	1	X	X	X	X	0
X	X	1	X	X	X	0
X	X	X	1	X	X	0
X	X	X	X	1	X	0
X	X	X	X	X	1	0

NOR6 Description

Function: 6 Input NOR, Normal Drive
Grid Count: 143

Pin Description

I1-I6	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I6	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

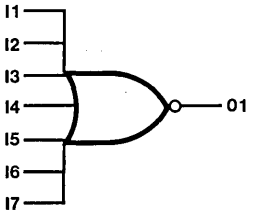
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I6 to O1	0.5	1.1	2.9	1.0	1.9	4.5	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.46	0.68	1.19	ns/pF

NOR7 — 7 INPUT NOR GATE



Logic Table

Inputs							Outputs
I1	I2	I3	I4	I5	I6	I7	O1
0	0	0	0	0	0	0	1
1	X	X	X	X	X	X	0
X	1	X	X	X	X	X	0
X	X	1	X	X	X	X	0
X	X	X	1	X	X	X	0
X	X	X	X	1	X	X	0
X	X	X	X	X	1	X	0
X	X	X	X	X	X	1	0

NOR7 Description

Function: 7 Input NOR, Normal Drive
Grid Count: 169

Pin Description

I1-I7	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I7	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

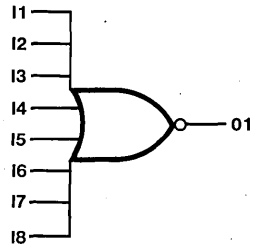
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I7 to O1	0.5	1.3	3.6	1.1	2.1	5.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.32	0.75	2.07	0.46	0.68	1.18	ns/pF

NOR8 — 8 INPUT NOR GATE



Logic Table

Inputs								Outputs
I1	I2	I3	I4	I5	I6	I7	I8	O1
0	0	0	0	0	0	0	0	1
1	X	X	X	X	X	X	X	0
X	1	X	X	X	X	X	X	0
X	X	1	X	X	X	X	X	0
X	X	X	1	X	X	X	X	0
X	X	X	X	1	X	X	X	0
X	X	X	X	X	1	X	X	0
X	X	X	X	X	X	1	X	0
X	X	X	X	X	X	X	1	0

NOR8 Description

Function: 8 Input NOR, Normal Drive
Grid Count: 182

Pin Description

I1-I8	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I8	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I8 to O1	0.5	1.3	3.6	1.1	2.1	5.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.32	0.75	2.07	0.46	0.68	1.18	ns/pF

AND2 — 2 INPUT AND GATE

Logic Table

Inputs		Outputs
I1	I2	O1
0	X	0
X	0	0
1	1	1

AND2 Description

Function: 2 Input AND, Normal Drive
Grid Count: 52

Pin Description

I1, I2	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1, I2	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1, I2 to O1	0.3	0.6	1.3	0.4	0.9	2.3	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.46	0.68	1.19	ns/pF

AND3 — 3 INPUT AND GATE

Logic Table

Inputs			Outputs
I1	I2	I3	O1
0	X	X	0
X	0	X	0
X	X	0	0
1	1	1	1

AND3 Description

Function: 3 Input AND, Normal Drive
Grid Count: 65

Pin Description

I1-I3	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I3	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

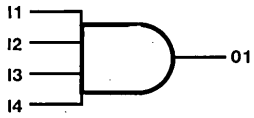
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I3 to O1	0.3	0.7	1.6	0.5	1.1	3.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.46	0.68	1.20	ns/pF

AND4 — 4 INPUT AND GATE



Logic Table

Inputs				Outputs
I1	I2	I3	I4	O1
0	X	X	X	0
X	0	X	X	0
X	X	0	X	0
X	X	X	0	0
1	1	1	1	1

AND4 Description

Function: 4 Input AND, Normal Drive
Grid Count: 78

Pin Description

I1-I4	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I4	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

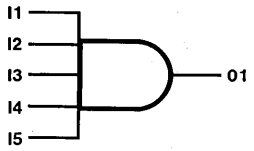
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I4 to O1	0.4	0.8	1.9	0.6	1.4	3.9	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.46	0.69	1.23	ns/pF

AND5 — 5 INPUT AND GATE



Logic Table

Inputs					Outputs
I1	I2	I3	I4	I5	O1
0	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0
1	1	1	1	1	1

AND5 Description

Function: 5 Input AND, Normal Drive
Grid Count: 104

Pin Description

I1-I5	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I5	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

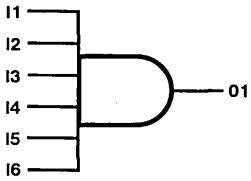
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I5 to O1	0.5	0.9	2.3	0.7	1.4	3.6	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.32	0.75	2.07	0.46	0.68	1.20	ns/pF

AND6 — 6 INPUT AND GATE



Logic Table

Inputs						Outputs
I1	I2	I3	I4	I5	I6	O1
0	X	X	X	X	X	0
X	0	X	X	X	X	0
X	X	0	X	X	X	0
X	X	X	0	X	X	0
X	X	X	X	0	X	0
X	X	X	X	X	0	0
1	1	1	1	1	1	1

AND6 Description

Function: 6 Input AND, Normal Drive
Grid Count: 130

Pin Description

I1-I6	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I6	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

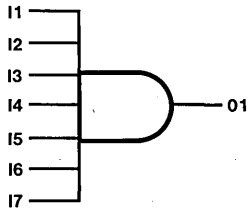
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I6 to O1	0.5	1.0	2.5	0.8	1.6	4.3	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.32	0.75	2.07	0.46	0.68	1.21	ns/pF

AND7 — 7 INPUT AND GATE



Logic Table

Inputs							Outputs
I1	I2	I3	I4	I5	I6	I7	O1
0	X	X	X	X	X	X	0
X	0	X	X	X	X	X	0
X	X	0	X	X	X	X	0
X	X	X	0	X	X	X	0
X	X	X	X	0	X	X	0
X	X	X	X	X	0	X	0
X	X	X	X	X	X	0	0
1	1	1	1	1	1	1	1

AND7 Description

Function: 7 Input AND, Normal Drive
Grid Count: 169

Pin Description

I1-I7	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I7	0.11	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

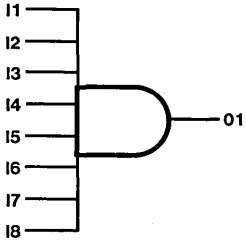
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
I1-I7 to O1	0.6	1.3	3.3	1.0	2.0	5.0	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
O1	0.33	0.74	1.95	0.46	0.68	1.18	ns/pF

AND8 — 8 INPUT AND GATE



Logic Table

Inputs								Outputs
I1	I2	I3	I4	I5	I6	I7	I8	O1
0	X	X	X	X	X	X	X	0
X	0	X	X	X	X	X	X	0
X	X	0	X	X	X	X	X	0
X	X	X	0	X	X	X	X	0
X	X	X	X	0	X	X	X	0
X	X	X	X	X	0	X	X	0
X	X	X	X	X	X	0	X	0
X	X	X	X	X	X	X	0	0
1	1	1	1	1	1	1	1	1

AND8 Description

Function: 8 Input AND, Normal Drive
Grid Count: 182

Pin Description

I1-I8	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I8	0.11	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I8 to O1	0.6	1.3	3.3	1.0	2.0	5.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.95	0.46	0.68	1.18	ns/pF

OR2 — 2 INPUT OR GATE

Logic Table

Inputs		Outputs
I1	I2	O1
0	0	0
1	X	1
X	1	1

OR2 Description

Function: 2 Input OR, Normal Drive
Grid Count: 52

Pin Description

I1, I2	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1, I2	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1, I2 to O1	0.7	1.1	2.2	0.3	0.9	2.5	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.46	0.68	1.22	ns/pF

OR3 — 3 INPUT OR GATE

Logic Table

Inputs			Outputs
I1	I2	I3	O1
0	0	0	0
1	X	X	1
X	1	X	1
X	X	1	1

OR3 Description

Function: 3 Input OR, Normal Drive
Grid Count: 78

Pin Description

I1-I3	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I3	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

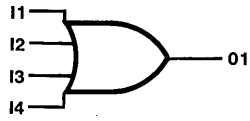
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I3 to O1	0.7	1.2	2.5	0.3	0.9	2.6	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.44	0.73	1.40	ns/pF

OR4 — 4 INPUT OR GATE



Logic Table

Inputs				Outputs
I1	I2	I3	I4	O1
0	0	0	0	0
1	X	X	X	1
X	1	X	X	1
X	X	1	X	1
X	X	X	1	1

OR4 Description

Function: 4 Input OR, Normal Drive
Grid Count: 91

Pin Description

I1-I4	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I4	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

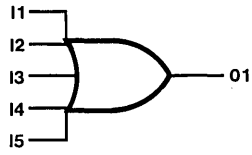
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I4 to O1	0.8	1.3	2.7	0.3	0.9	2.5	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.45	0.73	1.39	ns/pF

OR5 — 5 INPUT OR GATE



Logic Table

Inputs					Outputs
I1	I2	I3	I4	I5	O1
0	0	0	0	0	0
1	X	X	X	X	1
X	1	X	X	X	1
X	X	1	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1

OR5 Description

Function: 5 Input OR, Normal Drive
Grid Count: 143

Pin Description

I1-I5	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I5	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

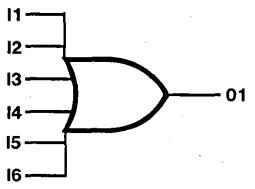
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I5 to O1	0.8	1.3	2.8	0.4	0.9	2.4	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.73	1.96	0.35	0.59	1.20	ns/pF

OR6 — 6 INPUT OR GATE



Logic Table

Inputs						Outputs
I1	I2	I3	I4	I5	I6	O1
0	0	0	0	0	0	0
1	X	X	X	X	X	1
X	1	X	X	X	X	1
X	X	1	X	X	X	1
X	X	X	1	X	X	1
X	X	X	X	1	X	1
X	X	X	X	X	1	1

OR6 Description

Function: 6 Input OR, Normal Drive
Grid Count: 156

Pin Description

I1-I6	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I6	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

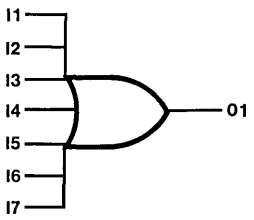
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I6 to O1	0.9	1.6	3.6	0.4	1.0	2.7	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.73	1.97	0.35	0.59	1.21	ns/pF

OR7 — 7 INPUT OR GATE



Logic Table

Inputs							Outputs
I1	I2	I3	I4	I5	I6	I7	O1
0	0	0	0	0	0	0	0
1	X	X	X	X	X	X	1
X	1	X	X	X	X	X	1
X	X	1	X	X	X	X	1
X	X	X	1	X	X	X	1
X	X	X	X	1	X	X	1
X	X	X	X	X	1	X	1
X	X	X	X	X	X	1	1

OR7 Description

Function: 7 Input OR, Normal Drive
Grid Count: 182

Pin Description

I1-I7	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I7	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

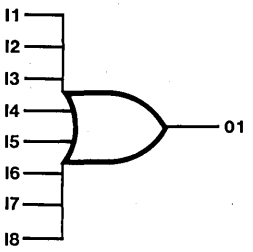
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I7 to O1	1.3	2.3	5.0	0.6	1.5	4.4	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.73	1.96	0.47	0.68	1.23	ns/pF

OR8 — 8 INPUT OR GATE



Logic Table

Inputs								Outputs
I1	I2	I3	I4	I5	I6	I7	I8	O1
0	0	0	0	0	0	0	0	0
1	X	X	X	X	X	X	X	1
X	1	X	X	X	X	X	X	1
X	X	1	X	X	X	X	X	1
X	X	X	1	X	X	X	X	1
X	X	X	X	1	X	X	X	1
X	X	X	X	X	1	X	X	1
X	X	X	X	X	X	1	X	1
X	X	X	X	X	X	X	1	1

OR8 Description

Function: 8 Input OR, Normal Drive
Grid Count: 195

Pin Description

I1-I8	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1-I8	0.15	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

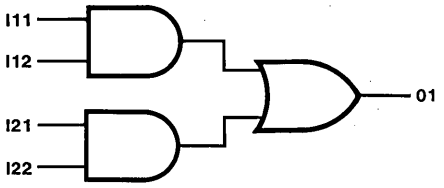
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1-I8 to O1	1.3	2.3	5.0	0.6	1.5	4.4	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.73	1.96	0.47	0.68	1.23	ns/pF

AOR22 — AND-OR GATE



Logic Table

Inputs				Outputs
I11	I12	I21	I22	O1
1	1	X	X	1
X	X	1	1	1
Any other combination				0

AOR22 Description

Function: 2 AND2 into OR2, Normal Drive
Grid Count: 78

Pin Description

I11, I12, I21, I22	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I11, I12, I21, I22	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

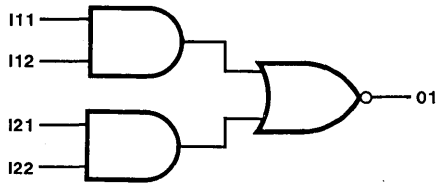
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I11, I12, I21, I22 to O1	0.7	1.2	2.5	0.6	1.3	3.8	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.47	0.70	1.29	ns/pF

AOI22 — AND-OR INVERT GATE



Logic Table

Inputs				Outputs
I11	I12	I21	I22	O1
1	1	X	X	0
X	X	1	1	0
Any other combination				1

AOI22 Description

Function: 2 AND2 into NOR2, Normal Drive
Grid Count: 78

Pin Description

I11, I12, I21, I22	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I11, I12, I21, I22	0.50	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

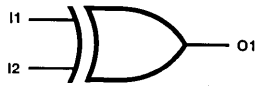
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I11, I12, I21, I22 to O1	0.3	0.6	1.7	0.5	0.9	1.7	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.32	0.75	2.05	0.44	0.72	1.38	ns/pF

EXR2 — EXCLUSIVE OR GATE



Logic Table

Inputs		Outputs
I1	I2	O1
0	0	0
0	1	1
1	0	1
1	1	0

EXR2 Description

Function: 2 Input EXCLUSIVE OR, Normal Drive
Grid Count: 78

Pin Description

I1, I2	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1, I2	0.30	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1, I2 to O1	0.6	1.2	2.8	0.5	1.1	3.1	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.46	0.68	1.21	ns/pF

EXN2 — EXCLUSIVE NOR GATE

Logic Table

Inputs		Outputs
I1	I2	O1
0	0	1
0	1	0
1	0	0
1	1	1

EXN2 Description

Function: 2 Input EXCLUSIVE NOR, Normal Drive
Grid Count: 65

Pin Description

I1, I2	Data Inputs
O1	Output

Input Capacitance

Input Name	Max.	Units
I1, I2	0.60	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

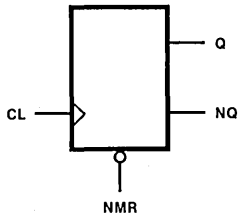
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I1, I2 to O1	0.4	0.8	1.8	0.5	1.0	2.6	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.73	1.95	0.44	0.72	1.37	ns/pF

FFT — TOGGLE FLIP-FLOP WITH RESET



Logic Table

Inputs		Outputs	
CL	NMR	Q	NQ
X	0	0	1
0	1	Q_0	NQ_0
↑	1	NQ_0	Q_0
1	1	Q_0	NQ_0

FFT Description

Function: Toggle Flip-Flop with Master Reset
Grid Count: 195

Pin Description

CL	Clock Input
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time			Hold Time			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
NMR (Inactive) to CL	2.0	3.0	4.0	0.6	1.6	4.0	ns

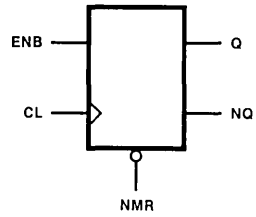
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to Q	0.9	1.7	3.9	1.0	1.9	4.6	ns
NMR to Q	—	—	—	1.1	2.4	6.1	ns
CL to NQ	1.2	2.4	5.7	1.2	2.3	5.8	ns
NMR to NQ	1.4	2.9	7.2	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.73	1.96	0.46	0.68	1.20	ns/pF
NQ	0.33	0.73	1.94	0.46	0.68	1.19	ns/pF

FFTE — TOGGLE FLIP-FLOP WITH ENABLE AND RESET



Logic Table

Inputs			Outputs	
CL	ENB	NMR	Q	NQ
X	X	0	0	1
0	X	1	Q_0	NQ_0
↑	0	1	Q_0	NQ_0
↑	1	1	NQ_0	Q_0
1	X	1	Q_0	NQ_0

FFTE Description

Function: Toggle Flip-Flop with Enable and Master Reset
Grid Count: 247

Pin Description

CL	Clock Input
ENB	Gate Enable Input
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
ENB	0.20	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
ENB to CL	2.0	3.0	4.5	0.6	1.2	2.8	ns
NMR (Inactive) to CL	2.0	3.0	4.0	0.6	1.2	2.8	ns

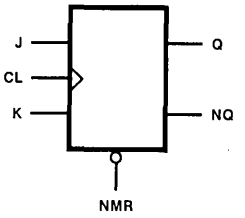
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to Q	0.9	1.7	3.9	1.0	1.9	4.6	ns
NMR to Q	—	—	—	1.1	2.4	6.1	ns
CL to NQ	1.3	2.5	6.0	1.2	2.5	6.4	ns
NMR to NQ	1.4	3.0	7.6	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.74	1.96	0.46	0.68	1.20	ns/pF
NQ	0.33	0.73	1.94	0.46	0.68	1.21	ns/pF

FFJK — JK FLIP-FLOP WITH RESET



Logic Table

Inputs				Outputs	
CL	J	K	NMR	Q	NQ
X	X	X	0	0	1
0	X	X	1	Q_0	NQ_0
↑	0	0	1	Q_0	NQ_0
↑	0	1	1	0	1
↑	1	0	1	1	0
↑	1	1	1	NQ_0	Q_0
1	X	X	1	Q_0	NQ_0

FFJK Description

Function: JK Flip-Flop with Master Reset
Grid Count: 247

Pin Description

CL	Clock Input
J	Data Input
K	Data Input
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
J	0.20	pF
K	0.15	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Typ.	Max.	Hold Time Min.	Typ.	Max.	Units
J to CL	2.0	3.0	4.5	0.5	1.2	2.7	ns
K to CL	2.0	3.0	4.5	0.5	1.2	2.7	ns
NMR (Inactive) to CL	2.0	3.0	4.0	0.5	1.2	2.7	ns

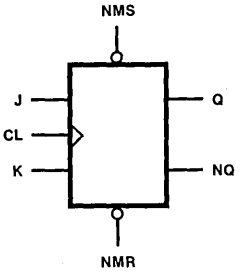
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
CL to Q	0.9	1.7	3.9	1.0	1.9	4.6	ns
NMR to Q	—	—	—	1.1	2.4	6.1	ns
CL to NQ	1.3	2.5	6.0	1.2	2.5	6.3	ns
NMR to NQ	1.4	3.0	7.6	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
Q	0.33	0.74	1.96	0.46	0.68	1.20	ns/pF
NQ	0.33	0.73	1.94	0.46	0.68	1.20	ns/pF

FLJK — JK FLIP-FLOP WITH SET AND RESET



Logic Table

Inputs					Outputs	
CL	J	K	NMS	NMR	Q	NQ
X	X	X	0	0	0*	0*
X	X	X	0	1	1	0
X	X	X	1	0	0	1
0	X	X	1	1	Q_0	NQ_0
↑	0	0	1	1	Q_0	NQ_0
↑	0	1	1	1	0	1
↑	1	0	1	1	1	0
↑	1	1	1	1	NQ_0	Q_0
1	X	X	1	1	Q_0	NQ_0

NOTE: *Nonstable state (if NMS and NMR are changed from 0 to 1 at the same time the results are unpredictable).

FLJK Description

Function: JK Flip-Flop with Master Set and Master Reset
Grid Count: 260

Pin Description

CL	Clock Input
J	Data Input
K	Data Input
NMS	Master Set Input (Asynchronous)
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.10	pF
J	0.15	pF
K	0.10	pF
NMS	0.30	pF
NMR	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
J to CL	2.0	3.0	7.0	0	0	0	ns
K to CL	2.0	3.0	7.0	0	0	0	ns
NMS (Inactive) to CL	2.0	3.0	4.0	1.3	3.0	6.7	ns
NMR (Inactive) to CL	2.0	3.0	4.0	1.3	3.0	6.7	ns

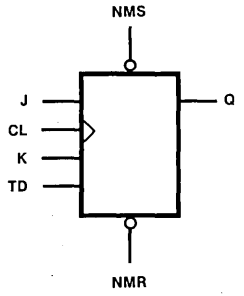
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to Q	0.9	1.7	4.2	1.0	2.0	5.3	ns
NMS to Q	0.9	1.8	4.9	—	—	—	ns
NMR to Q	—	—	—	0.5	1.1	2.9	ns
CL to NQ	1.2	2.4	6.1	1.1	2.3	6.0	ns
NMS to NQ	—	—	—	0.4	0.9	2.4	ns
NMR to NQ	0.8	1.7	4.3	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.74	1.97	0.46	0.68	1.23	ns/pF
NQ	0.33	0.73	1.94	0.46	0.67	1.18	ns/pF

FLJKT — 3-STATE JK FLIP-FLOP WITH SET AND RESET



Logic Table

Inputs						Outputs
CL	J	K	NMS	NMR	TD	Q
X	X	X	X	X	0	Z
X	X	X	0	0	1	0*
X	X	X	0	1	1	1
X	X	X	1	0	1	0
0	X	X	1	1	1	Q_0
↑	0	0	1	1	1	Q_0
↑	0	1	1	1	1	0
↑	1	0	1	1	1	1
↑	1	1	1	1	1	NQ_0
1	X	X	1	1	1	Q_0

NOTE: — *Nonstable state (if NMS and NMR are changed from 0 to 1 at the same time the results are unpredictable).
— The internal operation of FLJKT is not affected when TDO is 0.

FLJKT Description

Function: 3-State JK Flip-Flop with Master Set and Master Reset
Grid Count: 247

Pin Description

CL	Clock Input
J	Data Input
K	Data Input
NMS	Master Set Input (Asynchronous)
NMR	Master Reset Input (Asynchronous)
TD	3-State Enable Input (Asynchronous)
Q	Output

Input Capacitance

Input Name	Max.	Units
CL	0.10	pF
J	0.15	pF
K	0.10	pF
NMS	0.30	pF
NMR	0.20	pF
TD	0.25	pF

3-State Output Capacitance

Output Name	Max.	Units
Q(z)	0.25	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time			Hold Time			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
J to CL	2.0	3.0	7.0	0	0	0	ns
K to CL	2.0	3.0	7.0	0	0	0	ns
NMS (Inactive) to CL	2.0	3.0	4.0	1.3	2.9	6.5	ns
NMR (Inactive) to CL	2.0	3.0	4.0	1.3	2.9	6.5	ns

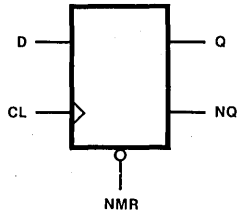
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	CL to Q	1.0	2.1	5.5	ns
Tphl	CL to Q	1.2	2.5	6.4	ns
Tplh	NMS to Q	1.0	2.3	6.2	ns
Tphl	NMR to Q	0.7	1.5	4.0	ns
Tpzh	TD to Q	0.6	1.0	2.4	ns
Tpzl	TD to Q	0.6	1.2	3.1	ns
Tphz	TD to Q	0.6	1.2	3.1	ns
Tplz	TD to Q	0.6	1.0	2.4	ns

Load Dependent Delay

Parameter	Output Name	Min.	Typ.	Max.	Units
Tplh	Q	0.32	0.75	2.07	ns/pF
Tphl	Q	0.44	0.72	1.39	ns/pF
Tpzh	Q	0.32	0.75	2.06	ns/pF
Tpzl	Q	0.44	0.72	1.38	ns/pF

FFD — D FLIP-FLOP WITH RESET



Logic Table

Inputs			Outputs	
CL	D	NMR	Q	NQ
X	X	0	0	1
0	X	1	Q_0	NQ_0
↑	0	1	0	1
↑	1	1	1	0
1	X	1	Q_0	NQ_0

FFD Description

Function: D Flip-Flop with Master Reset
Grid Count: 208

Pin Description

CL	Clock Input
D	Data Input
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
D	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time			Hold Time			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
D to CL	2.0	3.0	4.0	0.7	1.5	3.4	ns
NMR (Inactive) to CL	2.0	3.0	4.0	0.7	1.5	3.4	ns

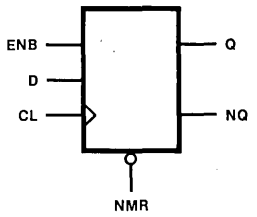
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to Q	1.1	1.9	4.4	1.1	2.1	5.0	ns
NMR to Q	—	—	—	1.1	2.4	6.0	ns
CL to NQ	1.3	2.4	5.7	1.2	2.4	5.8	ns
NMR to NQ	1.3	2.7	6.7	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.73	1.96	0.46	0.68	1.20	ns/pF
NQ	0.33	0.73	1.94	0.46	0.67	1.18	ns/pF

FFDE — D FLIP-FLOP WITH ENABLE AND RESET



Logic Table

Inputs				Outputs	
CL	D	ENB	NMR	Q	NQ
X	X	X	0	0	1
0	X	X	1	Q_0	NQ_0
↑	X	0	1	Q_0	NQ_0
↑	0	1	1	0	1
↑	1	1	1	1	0
1	X	X	1	Q_0	NQ_0

FFDE Description

Function: D Flip-Flop with Enable and Master Reset
Grid Count: 273

Pin Description

CL	Clock Input
D	Data Input
ENB	Gate Enable Input
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
D	0.20	pF
ENB	0.30	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
D to CL	2.0	3.0	6.0	0.3	0.7	1.5	ns
ENB to CL	2.0	3.0	6.0	0.3	0.7	1.5	ns
NMR (Inactive) to CL	2.0	3.0	4.0	0.3	0.7	1.5	ns

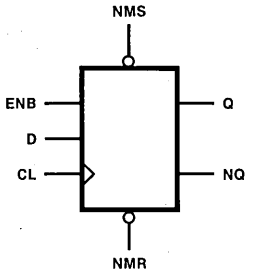
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to Q	1.1	1.9	4.3	1.1	2.1	5.0	ns
NMR to Q	—	—	—	1.1	2.4	6.0	ns
CL to NQ	1.5	2.9	7.1	1.5	3.0	7.7	ns
NMR to NQ	1.6	3.2	8.1	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.74	1.96	0.46	0.68	1.20	ns/pF
NQ	0.33	0.73	1.93	0.46	0.68	1.25	ns/pF

FLDE — D FLIP-FLOP WITH ENABLE, SET, AND RESET



Logic Table

Inputs					Outputs	
CL	D	ENB	NMS	NMR	Q	NQ
X	X	X	0	0	0*	0*
X	X	X	0	1	1	0
X	X	X	1	0	0	1
0	X	X	1	1	Q_0	NQ_0
↑	X	0	1	1	Q_0	NQ_0
↑	0	1	1	1	0	1
↑	1	1	1	1	1	0
1	X	X	1	1	Q_0	NQ_0

NOTE: *Nonstable state (if NMS and NMR are changed from 0 to 1 at the same time the results are unpredictable).

FLDE Description

Function: D Flip-Flop with Enable, Master Set, and Master Reset
Grid Count: 260

Pin Description

CL	Clock Input
D	Data Input
ENB	Gate Enable Input
NMS	Master Set Input (Asynchronous)
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.10	pF
D	0.20	pF
ENB	0.30	pF
NMS	0.30	pF
NMR	0.30	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Typ.	Max.	Hold Time Min.	Typ.	Max.	Units
D to CL	2.0	3.0	6.0	0	0	0	ns
ENB to CL	2.0	3.0	6.0	0	0	0	ns
NMS (Inactive) to CL	2.0	3.0	4.0	1.4	3.0	6.8	ns
NMR (Inactive) to CL	2.0	3.0	4.0	1.4	3.0	6.8	ns

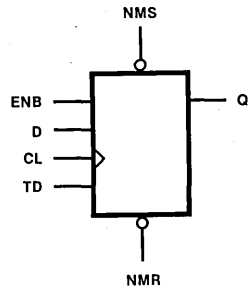
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
CL to Q	0.9	1.7	4.2	1.0	2.0	5.3	ns
NMS to Q	0.8	1.8	4.8	—	—	—	ns
NMR to Q	—	—	—	0.5	1.1	2.9	ns
CL to NQ	1.1	2.4	6.0	1.1	2.2	5.8	ns
NMS to NQ	—	—	—	0.5	1.1	2.8	ns
NMR to NQ	0.8	1.6	4.2	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
Q	0.33	0.74	1.96	0.46	0.68	1.23	ns/pF
NQ	0.33	0.73	1.94	0.46	0.67	1.18	ns/pF

FLDET — 3-STATE D FLIP-FLOP WITH ENABLE, SET, AND RESET



Logic Table

Inputs						Outputs
CL	D	ENB	NMS	NMR	TD	Q
X	X	X	X	X	0	Z
X	X	X	0	0	1	0*
X	X	X	0	1	1	1
X	X	X	1	0	1	0
0	X	X	1	1	1	Q_0
↑	X	0	1	1	1	Q_0
↑	0	1	1	1	1	0
↑	1	1	1	1	1	1
1	X	X	1	1	1	Q_0

NOTES: — *Nonstable state (if NMS and NMR are changed from 0 to 1 at the same time the results are unpredictable).
— The internal operation of FLDET is not affected when TD is 0.

FLDET Description

Function: 3-State D Flip-Flop with Enable, Master Set, and Master Reset
Grid Count: 260

Pin Description

CL	Clock Input
D	Data Input
ENB	Gate Enable Input
NMS	Master Set Input (Asynchronous)
NMR	Master Reset Input (Asynchronous)
TD	3-State Enable Input (Asynchronous)
Q	Output

Input Capacitance

Input Name	Max.	Units
CL	0.10	pF
D	0.20	pF
ENB	0.30	pF
NMS	0.30	pF
NMR	0.20	pF
TD	0.25	pF

3-State Output Capacitance

Output Name	Max.	Units
Q(z)	0.25	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time			Hold Time			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
D to CL	2.0	3.0	6.0	0	0	0	ns
ENB to CL	2.0	3.0	6.0	0	0	0	ns
NMS (Inactive) to CL	2.0	3.0	4.0	1.3	2.9	6.5	ns
NMR (Inactive) to CL	2.0	3.0	4.0	1.3	2.9	6.5	ns

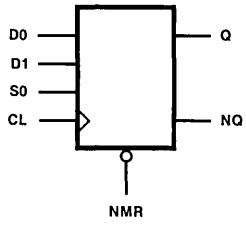
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	CL to Q	1.0	2.1	5.5	ns
Tphl	CL to Q	1.2	2.5	6.4	ns
Tplh	NMS to Q	1.0	2.3	6.2	ns
Tphl	NMR to Q	0.7	1.5	4.0	ns
Tpzh	TD to Q	0.6	1.0	2.4	ns
Tpzl	TD to Q	0.6	1.2	3.1	ns
Tphz	TD to Q	0.6	1.2	3.1	ns
Tplz	TD to Q	0.6	1.0	2.4	ns

Load Dependent Delay

Parameter	Output Name	Min.	Typ.	Max.	Units
Tplh	Q	0.32	0.75	2.06	ns/pF
Tphl	Q	0.44	0.72	1.38	ns/pF
Tpzh	Q	0.32	0.75	2.06	ns/pF
Tpzl	Q	0.44	0.72	1.38	ns/pF

FFDM2 — D FLIP-FLOP WITH 2 TO 1 DATA MULTIPLEXER AND RESET



Logic Table

Inputs					Outputs	
CL	D0	D1	S0	NMR	Q	NQ
X	X	X	X	0	0	1
0	X	X	X	1	Q_0	NQ_0
↑	0	X	0	1	0	1
↑	1	X	0	1	1	0
↑	X	0	1	1	0	1
↑	X	1	1	1	1	0
1	X	X	X	1	Q_0	NQ_0

FFDM2 Description

Function: D Flip-Flop with 2 to 1 Data Multiplexer and Master Reset
Grid Count: 260

Pin Description

CL	Clock Input
D0, D1	Data Inputs
S0	Select Input
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
D0, D1	0.20	pF
S0	0.30	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
D0, D1 to CL	2.0	3.0	6.0	0.4	0.8	1.8	ns
S0 to CL	2.0	3.0	6.0	0.4	0.8	1.8	ns
NMR (Inactive) to CL	2.0	3.0	4.0	0.4	0.8	1.8	ns

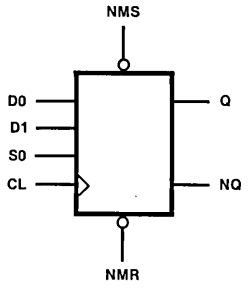
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to Q	1.1	1.9	4.4	1.1	2.1	5.0	ns
NMR to Q	—	—	—	1.1	2.4	6.0	ns
CL to NQ	1.3	2.4	5.7	1.2	2.4	5.8	ns
NMR to NQ	1.3	2.7	6.8	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.73	1.96	0.46	0.68	1.20	ns/pF
NQ	0.33	0.73	1.94	0.46	0.67	1.18	ns/pF

FLDM2 — D FLIP-FLOP WITH 2 TO 1 DATA MULTIPLEXER, SET, AND RESET



Logic Table

Inputs						Outputs	
CL	D0	D1	S0	NMS	NMR	Q	NQ
X	X	X	X	0	0	0*	0*
X	X	X	X	0	1	1	0
X	X	X	X	1	0	0	1
0	X	X	X	1	1	Q_0	NQ_0
↑	0	X	0	1	1	0	1
↑	1	X	0	1	1	1	0
↑	X	0	1	1	1	0	1
↑	X	1	1	1	1	1	0
1	X	X	X	1	1	Q_0	NQ_0

NOTE: *Nonstable state (if NMS and NMR are changed from 0 to 1 at the same time the results are unpredictable).

FLDM2 Description

Function: D Flip-Flop with 2:1 Data Multiplexer, Master Set, and Master Reset
Grid Count: 260

Pin Description

CL	Clock Input
D0, D1	Data Inputs
S0	Select Input
NMS	Master Set Input (Asynchronous)
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.10	pF
D0, D1	0.20	pF
S0	0.30	pF
NMS	0.30	pF
NMR	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Typ.	Max.	Hold Time Min.	Typ.	Max.	Units
D0, D1 to CL	2.0	3.0	6.0	0	0	0	ns
S0 to CL	2.0	3.0	6.0	0	0	0	ns
NMS (Inactive) to CL	2.0	3.0	4.0	1.4	3.0	6.8	ns
NMR (Inactive) to CL	2.0	3.0	4.0	1.4	3.0	6.8	ns

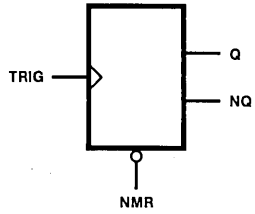
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
CL to Q	0.9	1.7	4.3	1.0	2.0	5.3	ns
NMS to Q	0.8	1.7	4.5	—	—	—	ns
NMR to Q	—	—	—	0.5	1.1	2.9	ns
CL to NQ	1.1	2.2	5.7	1.0	2.1	5.4	ns
NMS to NQ	—	—	—	0.5	1.0	2.5	ns
NMR to NQ	0.7	1.5	3.9	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
Q	0.33	0.74	1.96	0.46	0.68	1.22	ns/pF
NQ	0.33	0.73	1.94	0.46	0.67	1.17	ns/pF

FFDHI — POSITIVE EDGE EVENT TRIGGER WITH RESET



Logic Table

Inputs		Outputs	
TRIG	NMR	Q	NQ
X	0	0	1
0	1	Q_0	NQ_0
↑	1	1	0
1	1	Q_0	NQ_0

FFDHI Description

Function: Positive Edge Event Trigger with Master Reset
Grid Count: 195

Pin Description

TRIG	Trigger Input
NMR	Master Reset Input (Asynchronous)
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
TRIG	0.15	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
NMR (Inactive) to TRIG	2.0	3.0	4.0	0.3	0.7	1.7	ns

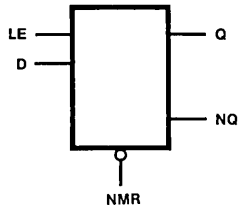
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
TRIG to Q	1.1	1.9	4.4	—	—	—	ns
NMR to Q	—	—	—	1.1	2.4	6.0	ns
TRIG to NQ	—	—	—	1.2	2.4	5.8	ns
NMR to NQ	1.3	2.7	6.7	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.73	1.96	0.46	0.68	1.20	ns/pF
NQ	0.33	0.73	1.94	0.46	0.67	1.18	ns/pF

LAD — TRANSPARENT D LATCH WITH RESET



Logic Table

Inputs			Outputs	
LE	D	NMR	Q	NQ
X	X	0	0	1
0	X	1	Q_0	NQ_0
1	0	1	0	1
1	1	1	1	0

LAD Description

Function: Transparent D Latch with Master Reset
Grid Count: 143

Pin Description

LE	Latch Enable Input
D	Data Input
NMR	Master Reset Input
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
LE	0.10	pF
D	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
D to LE	2.0	3.5	7.5	0	0	0	ns
NMR (Inactive) to LE	2.0	3.0	6.0	0	0	0	ns

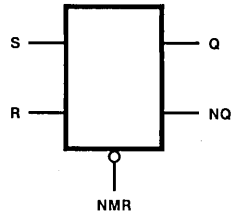
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
LE to Q	1.1	2.4	6.1	1.4	2.8	7.2	ns
D to Q	1.2	2.3	5.8	1.3	2.8	7.3	ns
NMR to Q	—	—	—	0.8	1.8	5.0	ns
LE to NQ	1.1	2.2	5.3	0.9	1.9	5.0	ns
D to NQ	1.1	2.2	5.4	0.9	1.8	4.7	ns
NMR to NQ	0.6	1.2	2.8	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.73	1.94	0.46	0.67	1.20	ns/pF
NQ	0.33	0.73	1.96	0.47	0.69	1.25	ns/pF

LSR — S-R LATCH WITH RESET



Logic Table

Inputs			Outputs	
S	R	NMR	Q	NQ
X	X	0	0	1
0	0	1	Q_0	NQ_0
0	1	1	0	1
1	0	1	1	0
1	1	1	0*	1*

NOTE: *Pseudo stable state (if S and R are changed from 1 to 0 at the same time the results are unpredictable).

LSR Description

Function: S-R Latch with Master Reset
Grid Count: 104

Pin Description

S	Latch Set Input
R	Latch Reset Input
NMR	Master Reset Input
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
S	0.15	pF
R	0.21	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

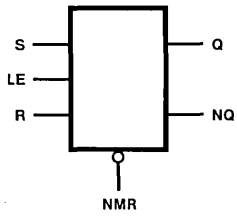
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
S to Q	1.2	2.5	6.3	—	—	—	ns
R to Q	0.5	1.1	3.1	0.9	1.7	4.1	ns
NMR to Q	0.9	1.8	4.9	1.3	2.7	6.4	ns
S to NQ	—	—	—	1.1	2.2	5.6	ns
R to NQ	0.8	1.3	2.6	0.4	0.9	2.7	ns
NMR to NQ	1.2	2.2	5.0	0.7	1.5	4.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.73	1.91	0.46	0.67	1.18	ns/pF
NQ	0.33	0.73	1.96	0.47	0.71	0.94	ns/pF

LASR — S-R LATCH WITH ENABLE AND RESET



Logic Table

Inputs				Outputs	
LE	S	R	NMR	Q	NQ
X	X	X	0	0	1
0	X	X	1	Q_0	NQ_0
1	0	0	1	Q_0	NQ_0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1*	0*

NOTE: *Pseudo stable state (if S and R are changed from 1 to 0 at the same time the results are unpredictable).

LASR Description

Function: S-R Latch with Enable and Master Reset
Grid Count: 182

Pin Description

LE	Latch Enable Input
S	Latch Set Input
R	Latch Reset Input
NMR	Master Reset Input
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
LE	0.10	pF
S	0.15	pF
R	0.15	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Typ.	Max.	Hold Time Min.	Typ.	Max.	Units
S to LE	2.0	4.0	9.0	0	0	0	ns
R to LE	2.5	5.5	12.0	0	0	0	ns
NMR (Inactive) to LE	2.0	3.0	6.0	0	0	0	ns

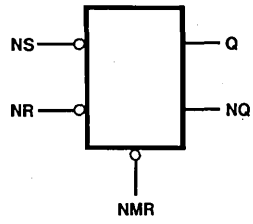
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
LE to Q	1.2	2.5	6.5	1.4	2.8	7.3	ns
S to Q	1.4	2.7	6.7	1.3	3.0	8.3	ns
R to Q	—	—	—	1.9	3.8	9.7	ns
NMR to Q	0.8	1.7	4.3	1.1	2.4	6.2	ns
LE to NQ	1.1	2.1	5.1	0.9	1.9	5.0	ns
S to NQ	1.1	2.2	5.8	1.1	2.1	5.2	ns
R to NQ	1.6	3.1	7.5	—	—	—	ns
NMR to NQ	0.6	1.2	2.7	0.5	1.1	3.3	ns

Load Dependent Delay

Output Name	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
Q	0.33	0.73	1.95	0.46	0.68	1.21	ns/pF
NQ	0.33	0.73	1.96	0.47	0.69	1.25	ns/pF

LNSR — $\overline{S}$-$\overline{R}$ LATCH WITH RESET



Logic Table

Inputs			Outputs	
NS	NR	NMR	Q	NQ
X	X	0	0	1
0	0	1	0*	1*
0	1	1	1	0
1	0	1	0	1
1	1	1	Q_0	NQ_0

NOTES: *Pseudo stable state (if NS and NR are changed from 0 to 1 at the same time the results are unpredictable).

LNSR Description

Function: $\overline{S}$-$\overline{R}$ Latch with Master Reset
Grid Count: 104

Pin Description

NS	Latch Set Input
NR	Latch Reset Input
NMR	Master Reset Input
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
NS	0.11	pF
NR	0.12	pF
NMR	0.12	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

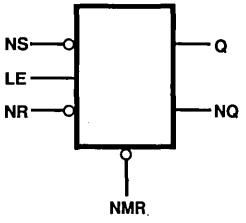
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
NS to Q	0.5	1.0	2.5	—	—	—	ns
NR to Q	0.4	0.9	2.1	0.6	1.2	3.4	ns
NMR to Q	0.4	0.9	2.0	0.5	1.1	3.1	ns
NS to NQ	—	—	—	0.7	1.5	3.9	ns
NR to NQ	0.8	1.6	4.2	0.6	1.3	3.9	ns
NMR to NQ	0.7	1.5	3.9	0.6	1.3	3.8	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.74	1.94	0.46	0.67	1.17	ns/pF
NQ	0.33	0.73	1.94	0.46	0.67	0.79	ns/pF

LANSR — $\overline{S}$-$\overline{R}$ LATCH WITH ENABLE AND RESET



Logic Table

Inputs				Outputs	
NS	NR	LE	NMR	Q	NQ
X	X	X	0	0	1
X	X	0	1	Q_0	NQ_0
1	1	1	1	Q_0	NQ_0
1	0	1	1	0	1
0	1	1	1	1	0
0	0	1	1	0*	1*

NOTE: *Pseudo stable state (if NS and NR are changed from 0 to 1 at the same time the results are unpredictable).

LANSR Description

Function: $\overline{S}$-$\overline{R}$ Latch with Enable and Master Reset
Grid Count: 182

Pin Description

LE	Latch Enable Input
NS	Latch Set Input
NR	Latch Reset Input
NMR	Master Reset Input
Q	Output
NQ	Complemented Output

Input Capacitance

Input Name	Max.	Units
LE	0.10	pF
NS	0.11	pF
NR	0.11	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Typ.	Max.	Hold Time Min.	Typ.	Max.	Units
NS to LE	2.5	5.0	10.5	0	0	0	ns
NR to LE	2.0	4.0	8.5	0	0	0	ns
NMR (Inactive) to LE	2.0	3.0	6.0	0	0	0	ns

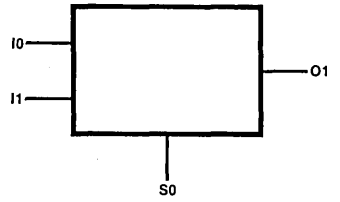
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
LE to Q	1.2	2.5	6.4	1.4	2.9	7.6	ns
NS to Q	1.2	2.6	6.8	—	—	—	ns
NR to Q	1.1	2.4	6.2	1.4	3.1	8.2	ns
NMR to Q	0.8	1.7	4.3	1.1	2.3	6.1	ns
LE to NQ	1.1	2.2	5.3	0.9	1.9	5.0	ns
NS to NQ	—	—	—	0.9	2.0	5.4	ns
NR to NQ	1.1	2.3	5.9	0.8	1.8	4.8	ns
NMR to NQ	0.6	1.2	2.7	0.5	1.1	3.3	ns

Load Dependent Delay

Output Name	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
Q	0.33	0.73	1.94	0.46	0.68	1.21	ns/pF
NQ	0.33	0.73	1.96	0.46	0.69	1.25	ns/pF

MUX21 — 2-LINE TO 1-LINE MULTIPLEXER



Logic Table

Inputs			Outputs
I0	I1	S0	O1
0	X	0	0
1	X	0	1
X	0	1	0
X	1	1	1

MUX21 Description

Function: 2-Line to 1-Line Multiplexer
Grid Count: 104

Pin Description

I0, I1	Data Inputs
S0	Select Input
O1	Output

Input Capacitance

Input Name	Max.	Units
I0, I1	0.20	pF
S0	0.30	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

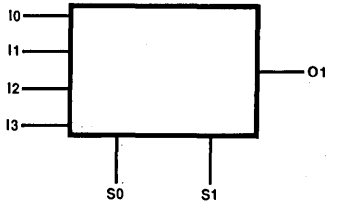
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
I0, I1 to O1	0.7	1.2	2.4	0.5	1.1	2.9	ns
S0 to O1	0.6	1.1	2.3	0.5	1.3	3.7	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.95	0.46	0.69	1.22	ns/pF

MUX41 — 4-LINE TO 1-LINE MULTIPLEXER



Logic Table

Inputs						Outputs
I0	I1	I2	I3	S1	S0	O1
0	X	X	X	0	0	0
1	X	X	X	0	0	1
X	0	X	X	0	1	0
X	1	X	X	0	1	1
X	X	0	X	1	0	0
X	X	1	X	1	0	1
X	X	X	0	1	1	0
X	X	X	1	1	1	1

MUX41 Description

Function: 4-Line to 1-Line Multiplexer
Grid Count: 182

Pin Description

I0-I3	Data Inputs
S0	Select Input (LSB)
S1	Select Input (MSB)
O1	Output

Input Capacitance

Input Name	Max.	Units
I0-I3	0.20	pF
S0	0.35	pF
S1	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

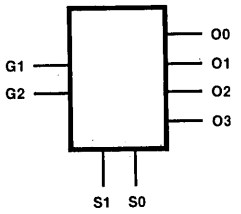
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
I0-I3 to O1	1.0	1.8	4.0	0.7	1.6	4.7	ns
S0 to O1	0.9	1.7	3.9	0.8	1.9	5.6	ns
S1 to O1	0.9	1.7	3.9	0.8	1.9	5.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
O1	0.33	0.74	1.97	0.47	0.72	1.35	ns

DMX2 — 2-LINE TO 4-LINE DEMULTIPLEXER/DECODER



Logic Table

Inputs				Outputs			
G1	G2	S1	S0	O0	O1	O2	O3
0	X	X	X	0	0	0	0
X	0	X	X	0	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	0	1	0	0
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

DMX2 Description

Function: 2-Line to 4-Line Demultiplexer/Decoder with 2 Enables
Grid Count: 299

Pin Description

G1	Enable Input
G2	Enable Input
S0	Select Input (LSB)
S1	Select Input (MSB)
O0-O3	Outputs

Input Capacitance

Input Name	Max.	Units
G1	0.11	pF
G2	0.11	pF
S0	0.10	pF
S1	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

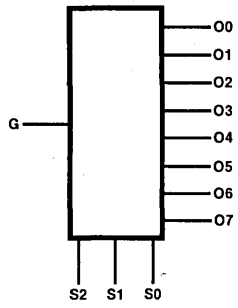
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
G1 to O0-O3	0.7	1.4	3.2	0.9	1.9	5.0	ns
G2 to O0-O3	0.7	1.4	3.2	0.9	1.9	5.0	ns
S0 to O0-O3	0.7	1.3	3.0	0.6	1.4	3.9	ns
S1 to O0-O3	0.7	1.5	3.4	0.8	1.7	4.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
O0-O3	0.33	0.74	1.96	0.46	0.68	1.19	ns/pF

DMX3 — 3-LINE TO 8-LINE DEMULTIPLEXER/DECODER



Logic Table

Inputs				Outputs							
G	S2	S1	S0	O0	O1	O2	O3	O4	O5	O6	O7
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

DMX3 Description

Function: 3-Line to 8-Line Demultiplexer/Decoder
Grid Count: 559

Pin Description

G	Enable Input
S0	Select Input (LSB)
S1	Select Input
S2	Select Input (MSB)
O0-O7	Outputs

Input Capacitance

Input Name	Max.	Units
G	0.21	pF
S0	0.10	pF
S1	0.10	pF
S2	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

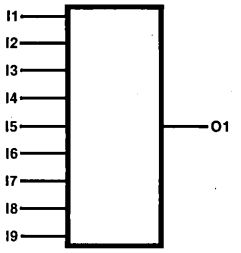
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
G to O0-O7	0.7	1.3	3.2	0.8	1.7	4.6	ns
S0 to O0-O7	0.5	1.1	3.0	0.7	1.3	3.5	ns
S1 to O0-O7	0.6	1.2	3.2	0.8	1.5	3.8	ns
S2 to O0-O7	0.7	1.5	3.7	0.9	2.0	5.4	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
O0-O7	0.33	0.74	1.96	0.46	0.68	1.19	ns/pF

CPR — 8/9-BIT PARITY CHECKER/GENERATOR



Logic Table

Inputs	Outputs
Number of Inputs I1 thru I9 that are 1	O1
1, 3, 5, 7, 9	0
0, 2, 4, 6, 8	1

CPR Description

Function: 8/9-Bit Parity Checker/Generator
Grid Count: 429

Pin Description

I1-I8	Data Inputs
I9	Data Input/Parity Input
O1	Even/$\overline{\text{Odd}}$ Parity Output

Input Capacitance

Input Name	Max.	Units
I1-I8	0.20	pF
I9	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
I1-I8 to O1	1.5	3.3	8.8	1.8	3.7	9.4	ns
I9 to O1	0.6	1.1	2.5	0.5	1.1	3.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
O1	0.33	0.74	1.96	0.46	0.69	1.24	ns/pF

INTRODUCTION TO TELESCOPING CELLS

Telescoping cells are building blocks from which certain multi-stage logic functions can be implemented. They are the preferred method of construction for multi-stage logic functions because they are designed with all input and output pins on opposite sides. Assembled telescoping devices are silicon efficient because the outputs from one telescoping cell align with the inputs of the adjacent cell, eliminating the need for routing channels. Performance of the device is optimized because interconnect parasitics between cells is reduced.

Construction of telescoping devices requires two types of cells: body cells and control cells. Body cells perform the basic function of a telescoping device. Each body cell equates to one functional bit, hence the number of body cells implemented determines the size of the completed telescoping device. Control cells provide the interface between external circuitry and the body cells. A third type of telescoping cells, the cap cell, is available where applicable as a driver for any final output related to the overall operation of the telescoping device. Cap cells are used when two or more telescoping devices are cascaded together to form a larger device, or when the final output signal is to be connected to circuitry external to the telescoping device.

Telescoping devices can be 1-12 bits in length. The 12 bit limit is due to loading limitations on the control cells. For optimum performance, it is recommended that the length of telescoping devices be kept to a minimum. This can be achieved by splitting large telescoping devices into multiple blocks.

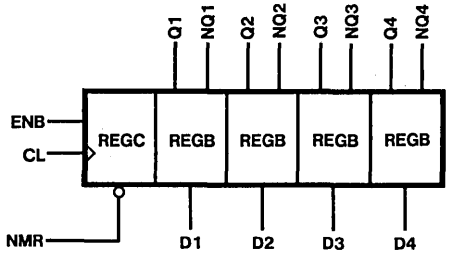
The following multi-stage functions are implemented with telescoping cells:

- Register—Synchronous Register (1-12 bits) with Enable and Master Reset.
- 3-State Register—3-State Synchronous Register (1-12 bits) with Enable and Master Reset.
- Shift Register—Synchronous Shift Register (1-12 bits), Serial Input, Parallel Output with Enable and Master Reset.
- Shift Register with Load—Synchronous Shift Register (1-12 bits), Serial Input, Parallel Input, Parallel Output with Load, Enable, and Master Reset.
- Up Counter—Synchronous, Cascadable Binary Up Counter (1-12 bits) with Load, Enable, and Master Reset.
- Up/Down Counter—Synchronous, Cascadable Binary Up/Down Counter (1-12 bits) with Load, Enable, and Master Reset.
- Adder— Cascadable Binary Ripple Adder (1-12 bits).
- Magnitude Comparator—Cascadable Binary Magnitude Comparator (1-12 bits).

Data sheets for telescoping functions are presented in two ways: first for an assembled telescoping device, then for the associated individual telescoping cells. The data sheets for assembled telescoping devices should prove to be the most useful. They include logic tables and equations for all potential device configurations for easy functional and performance evaluation.

TELESCOPING REGISTER (REGC, REGB)

Example: 4-bit register



Logic Table

Inputs				Outputs	
CL	Dn	ENB	NMR	Qn	NQn
X	X	X	0	0	1
0	X	X	1	Qno	NQno
↑	X	0	1	Qno	NQno
↑	0	1	1	0	1
↑	1	1	1	1	0
1	X	X	1	Qno	NQno

Telescoping Register Description

Function: Synchronous Register ($1 \leq n \leq 12$ bits) with Enable and Master Reset
Grid Count: $117 + n$ (221)

Pin Description

CL	Clock Input
Dn	Data Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous)
Qn	Output
NQn	Complemented Output

Input Capacitance

Input Name	Max.	Units
CL	0.14	pF
Dn	0.17	pF
ENB	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Parameter	Signal Path	Min.	Typ.	Max.	Units
Setup	Dn to CL	1.3 − n(0.035)	2.3 − n(0.078)	5.0 − n(0.21)	ns
Hold	Dn to CL	0	0	0	ns
Setup	ENB to CL	1.7 + n(0.025)	3.5 + n(0.057)	8.0 + n(0.15)	ns
Hold	ENB to CL	0	0	0	ns
Setup	NMR (Inactive) to CL	1.8 + n(0.013)	2.8 − n(0.010)	3.9 − n(0.089)	ns
Hold	NMR (Inactive) to CL	0	0	0	ns

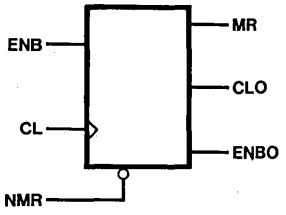
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	CL to Qn	1.3 + n(0.035)	2.3 + n(0.078)	5.1 + n(0.21)	ns
Tphl	CL to Qn	1.2 + n(0.035)	2.3 + n(0.078)	5.3 + n(0.21)	ns
Tplh	CL to NQn	1.4 + n(0.035)	2.7 + n(0.078)	6.0 + n(0.21)	ns
Tphl	CL to NQn	1.5 + n(0.035)	2.7 + n(0.078)	6.3 + n(0.21)	ns
Tphl	NMR to Qn	1.4 + n(0.033)	2.7 + n(0.073)	6.2 + n(0.20)	ns
Tplh	NMR to NQn	1.6 + n(0.033)	3.0 + n(0.073)	6.9 + n(0.20)	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Qn	0.33	0.74	1.96	0.46	0.68	1.19	ns/pF
NQn	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF

REGC — TELESCOPING REGISTER CONTROL



Logic Table

Inputs			Outputs		
CL	ENB	NMR	CLO	ENBO	MR
X	X	0	1	X	1
0	X	1	0	X	0
↑	X	1	↑	X	0
1	X	1	1	X	0
X	0	X	X	0	X
X	1	X	X	1	X

REGC Description

Function: Telescoping Register Control
Grid Count: 117

Pin Description

External Pins	
CL	Clock Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous, Active Low)
Telescoping Interconnect Pins	
CLO	Clock Output
ENBO	Enable Output
MR	Master Reset Output (Asynchronous, Active High)

Input Capacitance

Input Name	Max.	Units
CL	0.14	pF
ENB	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

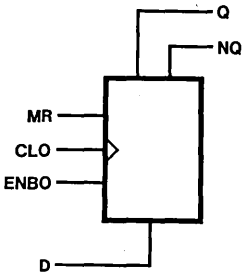
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to CLO	0.7	1.2	2.5	0.4	1.0	2.8	ns
NMR to CLO	0.7	1.3	3.2	0.6	1.2	3.1	ns
ENB to ENBO	0.4	0.7	1.5	0.4	0.8	2.2	ns
NMR to MR	0.4	0.9	2.2	0.5	1.0	2.4	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CLO	0.23	0.52	1.38	0.34	0.51	0.94	ns/pF
ENBO	0.23	0.52	1.37	0.34	0.50	0.88	ns/pF
MR	0.33	0.73	1.95	0.47	0.68	1.18	ns/pF

REGB — TELESCOPING REGISTER BODY



Logic Table

Inputs				Outputs	
CLO	D	ENBO	MR	Q	NQ
1	X	X	1	0	1
0	X	X	0	Q_0	NQ_0
↑	X	0	0	Q_0	NQ_0
↑	0	1	0	0	1
↑	1	1	0	1	0
1	X	X	0	Q_0	NQ_0

NOTE: A CLO signal transition to 1 when MR is 1 will be transparent to the user when the control cell is attached to a group of body cells.

REGB Description

Function: Telescoping Register Body
Grid Count: 221

Pin Description

External Pins	
D Q NQ	Data Input Output Complemented Output
Telescoping Interconnect Pins	
CLO ENBO MR	Clock Input Enable Input Master Reset Input (Asynchronous, Active High)

Input Capacitance

Input Name	Max.	Units
CLO	0.15	pF
D	0.17	pF
ENBO	0.26	pF
MR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Typ.	Max.	Hold Time Min.	Typ.	Max.	Units
D to CLO	2.0	3.5	7.5	0	0	0	ns
ENBO to CLO	2.0	4.0	9.0	0	0	0	ns
MR (Inactive) to CLO	2.0	3.0	4.0	0	0	0	ns

Intrinsic Propagation Delay

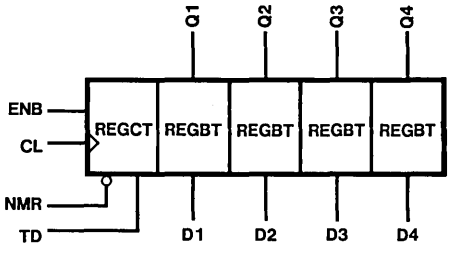
Signal Path	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
CLO to Q	0.6	1.1	2.6	0.5	1.1	2.8	ns
MR to Q	—	—	—	1.0	1.8	4.0	ns
CLO to NQ	0.7	1.5	3.5	0.8	1.5	3.8	ns
MR to NQ	1.2	2.1	4.7	—	—	—	ns

Load Dependent Delay

Output Name	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
Q	0.33	0.74	1.96	0.46	0.68	1.19	ns/pF
NQ	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF

TELESCOPING 3-STATE REGISTER (REGCT, REGBT)

Example: 4-bit 3-state register



Logic Table

Inputs					Outputs
CL	Dn	ENB	NMR	TD	Qn
X	X	X	X	0	Z
X	X	X	0	1	0
0	X	X	1	1	Qno
↑	X	0	1	1	Qno
↑	0	1	1	1	0
↑	1	1	1	1	1
1	X	X	1	1	Qno

NOTE: The internal operation of the register is not affected when TD is 0.

Telescoping 3-State Register Description

Function: 3-State Synchronous Register ($1 \leq n \leq 12$ bits) with Enable and Master Reset

Grid Count: $156 + n$ (234)

Pin Description

CL	Clock Input
Dn	Data Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous)
TD	3-State Enable Input (Asynchronous)
Qn	Output

Input Capacitance

Input Name	Max.	Units
CL	0.14	pF
Dn	0.17	pF
ENB	0.10	pF
NMR	0.10	pF
TD	0.10	pF

3-State Output Capacitance

Output Name	Max.	Units
Qn(z)	0.25	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Parameter	Signal Path	Min.	Typ.	Max.	Units
Setup	Dn to CL	1.3 − n(0.035)	2.3 − n(0.078)	5.0 − n(0.21)	ns
Hold	Dn to CL	0	0	0	ns
Setup	ENB to CL	1.7 + n(0.025)	3.5 + n(0.057)	8.0 + n(0.15)	ns
Hold	ENB to CL	0	0	0	ns
Setup	NMR (Inactive) to CL	1.8 + n(0.013)	2.8 − n(0.010)	3.9 − n(0.089)	ns
Hold	NMR (Inactive) to CL	0	0	0	ns

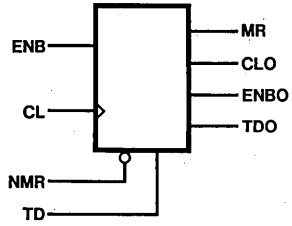
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	CL to Qn	1.5 + n(0.035)	2.7 + n(0.078)	6.3 + n(0.21)	ns
Tphl	CL to Qn	1.5 + n(0.035)	2.8 + n(0.078)	6.3 + n(0.21)	ns
Tphl	NMR to Qn	1.6 + n(0.033)	3.1 + n(0.073)	7.1 + n(0.20)	ns
Tpzh	TD to Qn	1.0 + n(0.092)	1.8 + n(0.21)	4.0 + n(0.55)	ns
Tpzl	TD to Qn	1.0 + n(0.092)	1.9 + n(0.21)	4.5 + n(0.55)	ns
Tphz	TD to Qn	1.0 + n(0.14)	2.0 + n(0.20)	5.2 + n(0.35)	ns
Tplz	TD to Qn	1.0 + n(0.14)	1.9 + n(0.20)	4.7 + n(0.35)	ns

Load Dependent Delay

Parameter	Output Name	Min.	Typ.	Max.	Units
Tplh	Qn	0.32	0.75	2.06	ns/pF
Tphl	Qn	0.44	0.72	1.37	ns/pF
Tpzh	Qn	0.32	0.75	2.06	ns/pF
Tpzl	Qn	0.44	0.72	1.38	ns/pF

REGCT — TELESCOPING 3-STATE REGISTER CONTROL



Logic Table

Inputs				Outputs			
CL	ENB	NMR	TD	CLO	ENBO	MR	TDO
X	X	0	X	1	X	1	X
0	X	1	X	0	X	0	X
↑	X	1	X	↑	X	0	X
1	X	1	X	1	X	0	X
X	0	X	X	X	0	X	X
X	1	X	X	X	1	X	X
X	X	X	0	X	X	X	0
X	X	X	1	X	X	X	1

REGCT Description

Function: Telescoping 3-State Register Control
Grid Count: 156

Pin Description

External Pins	
CL	Clock Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous, Active Low)
TD	3-State Enable Input (Asynchronous)
Telescoping Interconnect Pins	
CLO	Clock Output
ENBO	Enable Output
MR	Master Reset Output (Asynchronous, Active High)
TDO	3-State Enable Output (Asynchronous)

Input Capacitance

Input Name	Max.	Units
CL	0.14	pF
ENB	0.10	pF
NMR	0.10	pF
TD	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

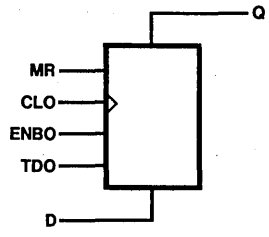
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to CLO	0.7	1.2	2.5	0.4	1.0	2.8	ns
NMR to CLO	0.7	1.3	3.2	0.6	1.2	3.1	ns
ENB to ENBO	0.4	0.7	1.5	0.4	0.8	2.2	ns
NMR to MR	0.4	0.9	2.2	0.5	1.0	2.4	ns
TD to TDO	0.4	0.7	1.5	0.4	0.8	2.2	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CLO	0.23	0.52	1.38	0.34	0.51	0.94	ns/pF
ENBO	0.23	0.52	1.37	0.34	0.50	0.88	ns/pF
MR	0.33	0.73	1.95	0.47	0.68	1.18	ns/pF
TDO	0.23	0.52	1.37	0.34	0.50	0.88	ns/pF

REGBT — TELESCOPING 3-STATE REGISTER BODY



Logic Table

Inputs					Outputs
CLO	D	ENBO	MR	TDO	Q
X	X	X	X	0	Z
1	X	X	1	1	0
0	X	X	0	1	Q_0
↑	X	0	0	1	Q_0
↑	0	1	0	1	0
↑	1	1	0	1	1
1	X	X	0	1	Q_0

NOTES: — A CLO signal transition to 1 when MR is 1 will be transparent to the user when the control cell is attached to a group of body cells.

— The internal operation of REGBT is not affected when TDO is 0.

REGBT Description

Function: Telescoping 3-State Register Body
Grid Count: 234

Pin Description

External Pins	
D	Data Input
Q	Output
Telescoping Interconnect Pins	
CLO	Clock Input
ENBO	Enable Input
MR	Master Reset Input (Asynchronous, Active High)
TDO	3-State Enable Input (Asynchronous)

Input Capacitance

Input Name	Max.	Units
CLO	0.15	pF
D	0.17	pF
ENBO	0.26	pF
MR	0.10	pF
TDO	0.40	pF

3-State Output Capacitance

Output Name	Max.	Units
Q(z)	0.25	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time			Hold Time			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
D to CLO	2.0	3.5	7.5	0	0	0	ns
ENBO to CLO	2.0	4.0	9.0	0	0	0	ns
MR (Inactive) to CLO	2.0	3.0	4.0	0	0	0	ns

Intrinsic Propagation Delay

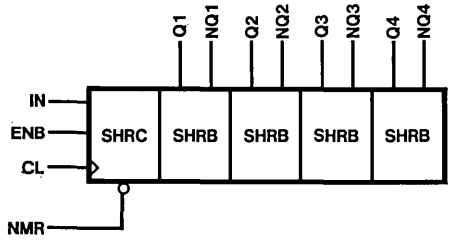
Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	CLO to Q	0.8	1.5	3.8	ns
Tphl	CLO to Q	0.8	1.6	3.8	ns
Tphl	MR to Q	1.2	2.2	4.9	ns
Tpzh	TDO to Q	0.6	1.1	2.5	ns
Tpzl	TDO to Q	0.6	1.2	3.0	ns
Tphz	TDO to Q	0.6	1.2	3.0	ns
Tplz	TDO to Q	0.6	1.1	2.5	ns

Load Dependent Delay

Parameter	Output Name	Min.	Typ.	Max.	Units
Tplh	Q	0.32	0.75	2.06	ns/pF
Tphl	Q	0.44	0.72	1.37	ns/pF
Tpzh	Q	0.32	0.75	2.06	ns/pF
Tpzl	Q	0.44	0.72	1.38	ns/pF

TELESCOPING SHIFT REGISTER (SHRC, SHRB)

Example: 4-bit shift register



Telescoping Shift Register Description

Function: Synchronous Shift Register ($1 \leq n \leq 12$ bits), Serial Input, Parallel Output with Enable and Master Reset

Grid Count: $130 + n$ (221)

Pin Description

CL	Clock Input
IN	Serial Data Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous)
Qn	Output
NQn	Complemented Output

Logic Table

Inputs				Outputs						
CL	IN	ENB	NMR	Q1	NQ1	Q2	NQ2	Q3	NQ3	...
X	X	X	0	0	1	0	1	0	1	
0	X	X	1	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	$Q3_0$	$NQ3_0$	
↑	X	0	1	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	$Q3_0$	$NQ3_0$	
↑	0	1	1	0	1	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	
↑	1	1	1	1	0	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	
1	X	X	1	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	$Q3_0$	$NQ3_0$	

Input Capacitance

Input Name	Max.	Units
CL	0.14	pF
IN	0.18	pF
ENB	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Parameter	Signal Path	Min.	Typ.	Max.	Units
Setup	IN to CL	1.3 − n(0.035)	2.3 − n(0.078)	5.0 − n(0.21)	ns
Hold	IN to CL	0	0	0	ns
Setup	ENB to CL	1.7 + n(0.025)	3.5 + n(0.057)	8.0 + n(0.15)	ns
Hold	ENB to CL	0	0	0	ns
Setup	NMR (Inactive) to CL	1.8 + n(0.013)	2.8 − n(0.010)	3.9 − n(0.089)	ns
Hold	NMR (Inactive) to CL	0	0	0	ns

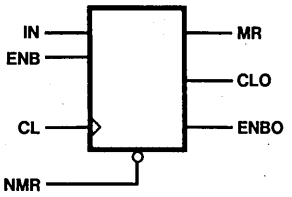
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	CL to Qn	1.3 + n(0.035)	2.3 + n(0.078)	5.1 + n(0.21)	ns
Tphl	CL to Qn	1.2 + n(0.035)	2.3 + n(0.078)	5.3 + n(0.21)	ns
Tplh	CL to NQn	1.7 + n(0.035)	3.1 + n(0.078)	6.9 + n(0.21)	ns
Tphl	CL to NQn	1.7 + n(0.035)	3.2 + n(0.078)	7.7 + n(0.21)	ns
Tphl	NMR to Qn	1.4 + n(0.033)	2.7 + n(0.073)	6.1 + n(0.20)	ns
Tplh	NMR to NQn	1.8 + n(0.033)	3.4 + n(0.073)	7.8 + n(0.20)	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Qn	0.33	0.74	1.96	0.47	0.68	1.19	ns/pF
NQn	0.33	0.73	1.94	0.46	0.68	1.23	ns/pF

SHRC — TELESCOPING SHIFT REGISTER CONTROL



Logic Table

Inputs				Outputs		
CL	IN	ENB	NMR	CLO	ENBO	MR
X	X	X	0	1	X	1
0	X	X	1	0	X	0
↑	X	X	1	↑	X	0
1	X	X	1	1	X	0
X	X	0	X	X	0	X
X	X	1	X	X	1	X

SHRC Description

Function: Telescoping Shift Register Control
Grid Count: 130

Pin Description

External Pins	
CL	Clock Input
IN	Serial Data Input Feedthrough
ENB	Enable Input
NMR	Master Reset Input (Asynchronous, Active Low)
Telescoping Interconnect Pins	
CLO	Clock Output
ENBO	Enable Output
MR	Master Reset Output (Asynchronous, Active High)

NOTE: IN is routed directly through SHRC without buffering to the Serial Data Input signal (IN) of the least significant (shift left configuration) or most significant (shift right configuration) SHRB cell.

Input Capacitance

Input Name	Max.	Units
CL	0.14	pF
IN	0.01	pF
ENB	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

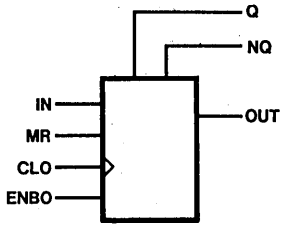
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to CLO	0.7	1.2	2.5	0.4	1.0	2.8	ns
NMR to CLO	0.7	1.3	3.2	0.6	1.2	3.1	ns
ENB to ENBO	0.4	0.7	1.5	0.4	0.8	2.2	ns
NMR to MR	0.4	0.9	2.2	0.5	1.0	2.4	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CLO	0.23	0.52	1.38	0.34	0.51	0.94	ns/pF
ENBO	0.23	0.52	1.37	0.34	0.50	0.88	ns/pF
MR	0.33	0.73	1.95	0.47	0.68	1.18	ns/pF

SHRB — TELESCOPING SHIFT REGISTER BODY



Logic Table

Inputs				Outputs		
CLO	IN	ENBO	MR	Q	NQ	OUT
1	X	X	1	0	1	0
0	X	X	0	Q_0	NQ_0	OUT_0
↑	X	0	0	Q_0	NQ_0	OUT_0
↑	0	1	0	0	1	0
↑	1	1	0	1	0	1
1	X	X	0	Q_0	NQ_0	OUT_0

NOTE: A CLO signal transition to 1 when MR is 1 will be transparent to the user when the control cell is attached to a group of body cells.

SHRB Description

Function: Telescoping Shift Register Body
Grid Count: 221

Pin Description

External Pins	
Q	Output
NQ	Complemented Output
Telescoping Interconnect Pins	
CLO	Clock Input
IN	Serial Data Input
ENBO	Enable Input
MR	Master Reset Input (Asynchronous, Active High)
OUT	Serial Output

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Typ.	Max.	Hold Time Min.	Typ.	Max.	Units
IN to CLO	2.0	3.5	7.5	0	0	0	ns
ENBO to CLO	2.0	4.0	9.0	0	0	0	ns
MR (Inactive) to CLO	2.0	3.0	4.0	0	0	0	ns

Intrinsic Propagation Delay

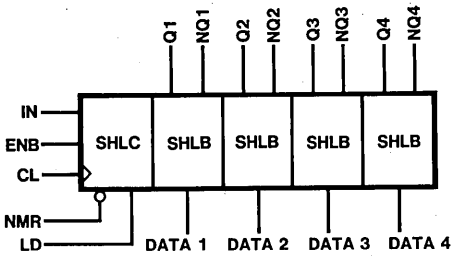
Signal Path	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
CLO to Q	0.6	1.1	2.6	0.5	1.1	2.8	ns
MR to Q	—	—	—	1.0	1.8	3.9	ns
CLO to NQ	1.0	1.9	4.4	1.0	2.0	5.2	ns
MR to NQ	1.4	2.5	5.6	—	—	—	ns
CLO to OUT	0.6	1.1	2.6	0.5	1.1	2.8	ns

Load Dependent Delay

Output Name	Tplh Min.	Typ.	Max.	Tphl Min.	Typ.	Max.	Units
Q	0.33	0.74	1.96	0.47	0.68	1.19	ns/pF
NQ	0.33	0.73	1.94	0.46	0.68	1.23	ns/pF
OUT	0.33	0.74	1.96	0.47	0.68	1.19	ns/pF

TELESCOPING SHIFT REGISTER WITH LOAD (SHLC, SHLB)

Example: 4-bit shift register with parallel load



Telescoping Shift Register with Load Description

Function: Synchronous Shift Register ($1 \leq n \leq 12$ bits), Serial Input, Parallel Input, Parallel Output with Load, Enable, and Master Reset

Grid Count: 156 + n (312)

Pin Description

CL	Clock Input
IN	Serial Data Input
DATAn	Parallel Data Input
LD	Load Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous)
Qn	Output
NQn	Complemented Output

Logic Table

Inputs									Outputs						
CL	IN	DATA1	DATA2	DATA3	···	LD	ENB	NMR	Q1	NQ1	Q2	NQ2	Q3	NQ3	···
X	X	X	X	X		X	X	0	0	1	0	1	0	1	
0	X	X	X	X		X	X	1	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	$Q3_0$	$NQ3_0$	
↑	X	X	X	X		X	0	1	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	$Q3_0$	$NQ3_0$	
↑	X	a	b	c		1	1	1	a	na	b	nb	c	nc	
↑	0	X	X	X		0	1	1	0	1	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	
↑	1	X	X	X		0	1	1	1	0	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	
1	X	X	X	X		X	X	1	$Q1_0$	$NQ1_0$	$Q2_0$	$NQ2_0$	$Q3_0$	$NQ3_0$	

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
IN	0.22	pF
DATAn	0.17	pF
LD	0.10	pF
ENB	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Parameter	Signal Path	Min.	Typ.	Max.	Units
Setup	IN to CL	2.3 − n(0.035)	4.8 − n(0.078)	10.5 − n(0.21)	ns
Hold	IN to CL	0	0	0	ns
Setup	DATAn to CL	2.3 − n(0.035)	4.8 − n(0.078)	10.5 − n(0.21)	ns
Hold	DATAn to CL	0	0	0	ns
Setup	LD to CL	2.7 + n(0.025)	6.0 + n(0.057)	13.5 + n(0.15)	ns
Hold	LD to CL	0	0	0	ns
Setup	ENB to CL	1.7 + n(0.025)	3.5 + n(0.057)	8.0 + n(0.15)	ns
Hold	ENB to CL	0	0	0	ns
Setup	NMR (Inactive) to CL	1.8 + n(0.013)	2.8 − n(0.010)	3.9 − n(0.088)	ns
Hold	NMR (Inactive) to CL	0	0	0	ns

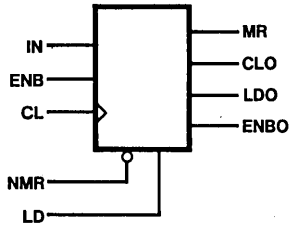
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	CL to Qn	1.4 + n(0.035)	2.5 + n(0.078)	5.5 + n(0.21)	ns
Tphl	CL to Qn	1.3 + n(0.035)	2.5 + n(0.078)	5.6 + n(0.21)	ns
Tplh	CL to NQn	1.9 + n(0.035)	3.6 + n(0.078)	8.0 + n(0.21)	ns
Tphl	CL to NQn	2.0 + n(0.035)	3.8 + n(0.078)	8.0 + n(0.21)	ns
Tphl	NMR to Qn	1.4 + n(0.033)	2.7 + n(0.073)	6.3 + n(0.20)	ns
Tplh	NMR to NQn	2.1 + n(0.033)	3.9 + n(0.073)	8.7 + n(0.20)	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Qn	0.33	0.74	1.96	0.46	0.68	1.19	ns/pF
NQn	0.33	0.73	1.94	0.46	0.70	1.30	ns/pF

SHLC — TELESCOPING SHIFT REGISTER WITH LOAD, CONTROL



Logic Table

Inputs					Outputs			
CL	IN	LD	ENB	NMR	CLO	LDO	ENBO	MR
X	X	X	X	0	1	X	X	1
0	X	X	X	1	0	X	X	0
↑	X	X	X	1	↑	X	X	0
1	X	X	X	1	1	X	X	0
X	X	0	X	X	X	0	X	X
X	X	1	X	X	X	1	X	X
X	X	X	0	X	X	X	0	X
X	X	X	1	X	X	X	1	X

SHLC Description

Function: Telescoping Shift Register with Load, Control
Grid Count: 156

Pin Description

External Pins	
CL	Clock Input
IN	Serial Data Input Feedthrough
LD	Load Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous, Active Low)
Telescoping Interconnect Pins	
CLO	Clock Output
LDO	Load Output
ENBO	Enable Output
MR	Master Reset Output (Asynchronous, Active High)

NOTE: IN is routed directly through SHLC without buffering to the Serial Data Input signal (IN) of the least significant (shift left configuration) or most significant (shift right configuration) SHLB cell.

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
IN	0.05	pF
LD	0.10	pF
ENB	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

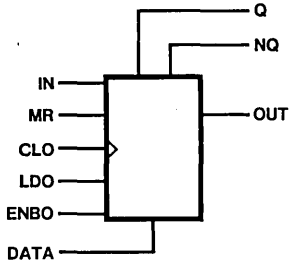
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to CLO	0.7	1.2	2.5	0.4	1.0	2.8	ns
NMR to CLO	0.7	1.3	3.2	0.6	1.2	3.1	ns
LD to LDO	0.4	0.7	1.5	0.4	0.8	2.2	ns
ENB to ENBO	0.4	0.7	1.5	0.4	0.8	2.2	ns
NMR to MR	0.4	0.9	2.2	0.5	1.0	2.4	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CLO	0.23	0.52	1.38	0.34	0.51	0.94	ns/pF
LDO	0.23	0.52	1.37	0.34	0.50	0.88	ns/pF
ENBO	0.23	0.52	1.37	0.34	0.50	0.88	ns/pF
MR	0.33	0.73	1.95	0.47	0.68	1.17	ns/pF

SHLB — SHIFT REGISTER WITH LOAD, BODY



Logic Table

Inputs						Outputs		
CLO	IN	DATA	LDO	ENBO	MR	Q	NQ	OUT
1	X	X	X	X	1	0	1	0
0	X	X	X	X	0	Q_0	NQ_0	OUT_0
↑	X	X	X	0	0	Q_0	NQ_0	OUT_0
↑	X	0	1	1	0	0	1	0
↑	X	1	1	1	0	1	0	1
↑	0	X	0	1	0	0	1	0
↑	1	X	0	1	0	1	0	1
1	X	X	X	X	0	Q_0	NQ_0	OUT_0

NOTE: A CLO signal transition to 1 when MR is 1 will be transparent to the user when the control cell is attached to a group of body cells.

SHLB Description

Function: Telescoping Shift Register with Load, Body
Grid Count: 312

Pin Description

External Pins	
DATA	Parallel Data Input
Q	Output
NQ	Complemented Output
Telescoping Interconnect Pins	
CLO	Clock Input
IN	Serial Data Input
ENBO	Enable Input
LDO	Load Input
MR	Master Reset Input (Asynchronous, Active High)
OUT	Serial Output

Input Capacitance

Input Name	Max.	Units
CLO	0.15	pF
IN	0.17	pF
DATA	0.17	pF
LDO	0.26	pF
ENBO	0.26	pF
MR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
IN to CLO	3.0	6.0	13.0	0	0	0	ns
DATA to CLO	3.0	6.0	13.0	0	0	0	ns
LDO to CLO	3.0	6.5	14.5	0	0	0	ns
ENBO to CLO	2.0	4.0	9.0	0	0	0	ns
MR (Inactive) to CLO	2.0	3.0	4.0	0	0	0	ns

Intrinsic Propagation Delay

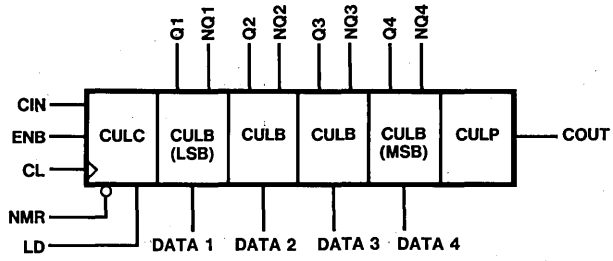
Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CLO to Q	0.7	1.3	3.0	0.6	1.3	3.1	ns
MR to Q	—	—	—	1.0	1.8	4.1	ns
CLO to NQ	1.2	2.4	5.5	1.3	2.6	6.5	ns
MR to NQ	1.7	3.0	6.5	—	—	—	ns
CLO to OUT	1.0	2.0	5.0	1.1	2.0	4.4	ns
MR to OUT	—	—	—	1.5	2.5	5.4	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Q	0.33	0.74	1.96	0.46	0.68	1.19	ns/pF
NQ	0.33	0.73	1.94	0.46	0.70	1.30	ns/pF
OUT	0.33	0.73	1.94	0.46	0.70	1.30	ns/pF

TELESCOPING UP COUNTER (CULC, CULB, CULP)

Example: 4-bit up counter



Telescoping Up Counter Description

Function: Synchronous, Cascadable Binary Up Counter ($1 \leq n \leq 12$ bits) with Load, Enable, and Master Reset

Grid Count: With CULP — 208 + n (338)
Without CULP — 169 + n (338)

Pin Description

CL	Clock Input
CIN	Carry Input
DATAn	Data Input
LD	Load Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous)
Qn	Output
NQn	Complemented Output
COUT	Carry Output

Logic Table

Inputs									Outputs						
CL	CIN	···	DATA3	DATA2	DATA1	LD	ENB	NMR	···	Q3	NQ3	Q2	NQ2	Q1	NQ1
X	X		X	X	X	X	X	0		0	1	0	1	0	1
0	X		X	X	X	X	X	1		$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$
↑	X		X	X	X	0	0	1		$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$
↑	X		c	b	a	1	X	1		c	nc	b	nb	a	na
↑	0		X	X	X	0	1	1		$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$
↑	1		X	X	X	0	1	1		See Table A					
1	X		X	X	X	X	X	1		$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$

Table A

Previous State							Next State					
···	$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$	···	Q3	NQ3	Q2	NQ2	Q1	NQ1
	0	1	0	1	0	1		0	1	0	1	1	0
	0	1	0	1	1	0		0	1	1	0	0	1
	0	1	1	0	0	1		0	1	1	0	1	0
	0	1	1	0	1	0		1	0	0	1	0	1
	1	0	0	1	0	1		1	0	0	1	1	0
	1	0	0	1	1	0		1	0	1	0	0	1
	1	0	1	0	0	1		1	0	1	0	1	0
	1	0	1	0	1	0		0	1	0	1	0	1

NOTES: COUT = CIN • Q1 • Q2 • Q3...; COUT is generated with combinatorial logic, thus under certain conditions a short pulse will occur. Therefore, COUT should not be used as a clock signal or for any other edge triggered signal. A cap cell (CULP) must be used if COUT is to be connected to circuitry external to a telescoping block.

Input Capacitance

Input Name	Max.	Units
CL	0.14	pF
CIN	0.23	pF
DATAn	0.17	pF
LD	0.10	pF
ENB	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Parameter	Signal Path	Min.	Typ.	Max.	Units
Setup	CIN to CL	1.8 + n(0.44)	3.8 + n(0.95)	7.9 + n(2.42)	ns
Hold	CIN to CL	0	0	0	ns
Setup	DATAn to CL	1.3 − n(0.035)	2.3 − n(0.078)	5.0 − n(0.21)	ns
Hold	DATAn to CL	0	0	0	ns
Setup	LD to CL	1.7 + n(0.025)	3.5 + n(0.057)	8.0 + n(0.15)	ns
Hold	LD to CL	0	0	0	ns
Setup	ENB to CL	2.7 − n(0.002)	5.4 − n(0.005)	11.7 − n(0.012)	ns
Hold	ENB to CL	0	0	0	ns
Setup	NMR (Inactive) to CL	1.8 + n(0.013)	2.8 − n(0.010)	3.9 − n(0.088)	ns
Hold	NMR (Inactive) to CL	0	0	0	ns

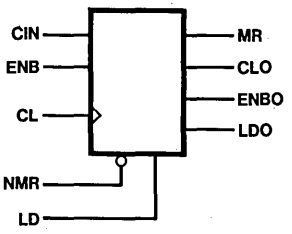
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	CL to Qn	1.3 + n(0.035)	2.3 + n(0.078)	5.1 + n(0.21)	ns
Tphl	CL to Qn	1.2 + n(0.035)	2.3 + n(0.078)	5.3 + n(0.21)	ns
Tplh	CL to NQn	1.5 + n(0.035)	2.7 + n(0.078)	6.2 + n(0.21)	ns
Tphl	CL to NQn	1.5 + n(0.035)	2.8 + n(0.078)	6.6 + n(0.21)	ns
Tphl	NMR to Qn	1.5 + n(0.033)	2.7 + n(0.073)	6.1 + n(0.20)	ns
Tplh	NMR to NQn	1.6 + n(0.033)	3.1 + n(0.073)	7.0 + n(0.20)	ns
Tplh (n=1)	CL to COUT	2.1	3.9	9.0	ns
Tplh (2≤n≤12)	CL to COUT	1.7 + n(0.51)	2.8 + n(1.10)	6.2 + n(2.83)	ns
Tphl	CL to COUT	1.9 + n(0.035)	4.0 + n(0.078)	9.1 + n(0.21)	ns
Tphl	NMR to COUT	2.1 + n(0.033)	4.3 + n(0.073)	9.9 + n(0.20)	ns
Tplh	CIN to COUT	0.3 + n(0.47)	0.3 + n(1.02)	0.3 + n(2.62)	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
Qn	0.33	0.74	1.97	0.46	0.68	1.20	ns/pF
NQn	0.33	0.74	1.96	0.46	0.68	1.21	ns/pF
COUT	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF

CULC — TELESCOPING UP COUNTER CONTROL



Logic Table

Inputs					Outputs			
CL	CIN	LD	ENB	NMR	CLO	LDO	ENBO	MR
X	X	X	X	0	1	X	X	1
0	X	X	X	1	0	X	X	0
↑	X	X	X	1	↑	X	X	0
1	X	X	X	1	1	X	X	0
X	X	0	X	X	X	0	X	X
X	X	1	X	X	X	1	X	X
X	X	X	0	X	X	X	0	X
X	X	X	1	X	X	X	1	X

CULC Description

Function: Telescoping Up Counter Control
Grid Count: 169

Pin Description

External Pins	
CL	Clock Input
CIN	Carry In Feedthrough
LD	Load Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous, Active Low)
Telescoping Interconnect Pins	
CLO	Clock Output
LDO	Load Output
ENBO	Enable Output
MR	Master Reset Output (Asynchronous, Active High)

NOTE: CIN is routed directly through CULC without buffering to the Carry Input signal (CIN) of the least significant CULB cell. This signal must be tied high into the least significant counter block.

Input Capacitance

Input Name	Max.	Units
CL	0.14	pF
CIN	0.01	pF
LD	0.10	pF
ENB	0.10	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

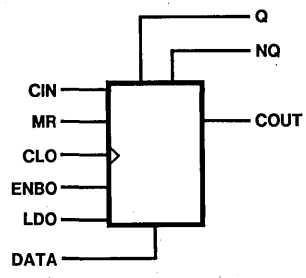
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
CL to CLO	0.7	1.2	2.5	0.4	1.0	2.8	ns
NMR to CLO	0.7	1.3	3.2	0.6	1.2	3.1	ns
LD to LDO	0.4	0.7	1.5	0.4	0.8	2.2	ns
ENB to ENBO	0.4	0.6	1.2	0.3	0.7	1.8	ns
NMR to MR	0.4	0.9	2.2	0.5	1.0	2.4	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLO	0.23	0.52	1.38	0.34	0.51	0.94	ns/pF
LDO	0.23	0.52	1.37	0.34	0.50	0.88	ns/pF
ENBO	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF
MR	0.33	0.73	1.95	0.47	0.68	1.18	ns/pF

CULB — TELESCOPING UP COUNTER BODY



Logic Table

Inputs						Outputs		
CLO	CIN	DATA	LDO	ENBO	MR	Q	NQ	COUT
1	X	X	X	X	1	0	1	0
0	0	X	X	X	0	Q_0	NQ_0	0
0	1	X	X	X	0	Q_0	NQ_0	Q_0
↑	X	0	1	X	0	0	1	0
↑	0	1	1	X	0	1	0	0
↑	1	1	1	X	0	1	0	1
↑	0	X	0	0	0	Q_0	NQ_0	0
↑	1	X	0	0	0	Q_0	NQ_0	Q_0
↑	0	X	0	1	0	Q_0	NQ_0	0
↑	1	X	0	1	0	NQ_0	Q_0	NQ_0
1	0	X	X	X	0	Q_0	NQ_0	0
1	1	X	X	X	0	Q_0	NQ_0	Q_0

NOTES: — A CLO signal transition to 1 when MR is 1 will be transparent to the user when the control cell is attached to a group of body cells.

— COUT = CIN • Q; a cap cell (CULP) must be used if COUT is to be connected to circuitry external to a telescoping block.

CULB Description

Function: Telescoping Up Counter Body
Grid Count: 338

Pin Description

External Pins	
DATA	Data Input
Q	Output
NQ	Complemented Output
Telescoping Interconnect Pins	
CLO	Clock Input
CIN	Carry Input
ENBO	Enable Input
LDO	Load Input
MR	Master Reset Input (Asynchronous, Active High)
COUT	Carry Output

Input Capacitance

Input Name	Max.	Units
CLO	0.15	pF
CIN	0.22	pF
DATA	0.17	pF
LDO	0.26	pF
ENBO	0.10	pF
MR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time			Hold Time			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
CIN to CLO	3.0	6.0	13.0	0	0	0	ns
DATA to CLO	2.0	3.5	7.5	0	0	0	ns
LDO to CLO	2.0	4.0	9.0	0	0	0	ns
ENBO to CLO	3.0	6.0	13.0	0	0	0	ns
MR (Inactive) to CLO	2.0	3.0	4.0	0	0	0	ns

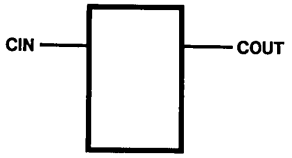
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLO to Q	0.6	1.1	2.6	0.5	1.1	2.8	ns
MR to Q	—	—	—	1.0	1.8	3.9	ns
CLO to NQ	0.8	1.5	3.7	0.8	1.6	4.1	ns
MR to NQ	1.2	2.2	4.8	—	—	—	ns
CIN to COUT	0.2	0.4	0.9	0.3	0.6	1.4	ns
CLO to COUT	0.9	1.7	4.3	0.8	1.8	4.3	ns
MR to COUT	—	—	—	1.3	2.4	5.4	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Q	0.33	0.74	1.97	0.46	0.68	1.20	ns/pF
NQ	0.33	0.74	1.96	0.46	0.68	1.21	ns
COUT	1.24	2.84	7.84	1.70	2.63	4.94	ns/pF

CULP — TELESCOPING UP COUNTER CAP



Logic Table

Inputs	Outputs
CIN	COUT
0 1	0 1

NOTES:
— COUT is generated with combinational logic, thus under certain conditions a short pulse will occur. Therefore, the carry out signal should not be used as a clock signal or for any other edge triggered signal.
— CUPL must be used if COUT is to be connected to circuitry external to a telescoping block.

CULP Description

Function: Telescoping Up Counter Carry Out Driver
Grid Count: 39

Pin Description

External Pins	
COUT	Carry Output
Telescoping Interconnect Pins	
CIN	Carry Input

Input Capacitance

Input Name	Max.	Units
CIN	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

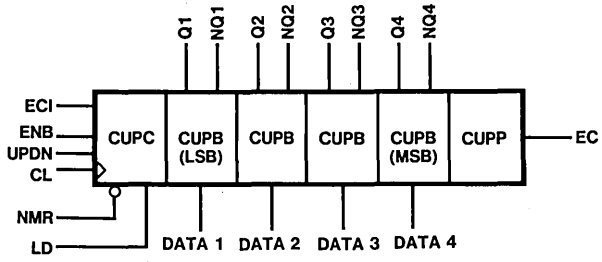
Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CIN to COUT	0.4	0.6	1.2	0.3	0.7	1.8	ns

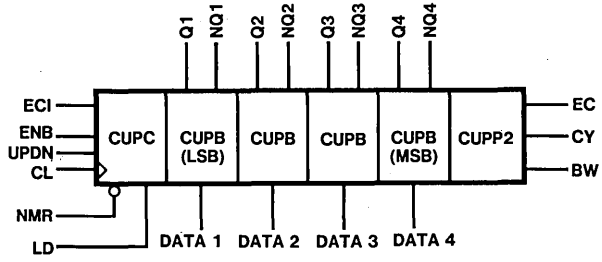
Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
COUT	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF

TELESCOPING UP/DOWN COUNTER (CUPC, CUPB, CUPP, CUPP2)

Example: 4-bit up/down counter





Telescoping Up Counter Description

Function: Synchronous, Cascadable Binary Up/Down Counter ($1 \leq n \leq 12$ bits) with Load, Enable, and Master Reset

Grid Count: With CUPP — 221 + n (429)
With CUPP2 — 338 + n (429)
Without CUPP or CUPP2 — 195 + n(429)

Pin Description

CL	Clock Input
ECI	End Count Input
DATAn	Data Input
UPDN	Count Up/Down Input (Up—Active High)
LD	Load Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous)
Qn	Output
NQn	Complemented Output
EC	End Count Output (CUPP, CUPP2)
CY	Carry Output (CUPP2)
BW	Borrow Output (CUPP2)

Logic Table

Inputs										Outputs					
CL	ECI	···	DATA3	DATA2	DATA1	UPDN	LD	ENB	NMR	···	Q3	NQ3	Q2	NQ2	Q1	NQ1
X	X		X	X	X	X	X	X	0		0	1	0	1	0	1
0	X		X	X	X	X	X	X	1		$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$
↑	X		X	X	X	X	X	0	1		$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$
↑	X		c	b	a	X	1	1	1		c	nc	b	nb	a	na
↑	0		X	X	X	X	0	1	1		$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$
↑	1		X	X	X	0	0	1	1		See Table A					
↑	1		x	x	x	1	0	1	1		See Table B					
1	X		X	X	X	X	X	X	1		$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$

Table A (Count Down)

Previous State							Next State					
···	$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$	···	Q3	NQ3	Q2	NQ2	Q1	NQ1
	0	1	0	1	0	1		1	0	1	0	1	0
	0	1	0	1	1	0		0	1	0	1	0	1
	0	1	1	0	0	1		0	1	0	1	1	0
	0	1	1	0	1	0		0	1	1	0	0	1
	1	0	0	1	0	1		0	1	1	0	1	0
	1	0	0	1	1	0		1	0	0	1	0	1
	1	0	1	0	0	1		1	0	0	1	1	0
	1	0	1	0	1	0		1	0	1	0	0	1

Table B (Count Up)

Previous State							Next State					
···	$Q3_0$	$NQ3_0$	$Q2_0$	$NQ2_0$	$Q1_0$	$NQ1_0$	···	Q3	NQ3	Q2	NQ2	Q1	NQ1
	0	1	0	1	0	1		0	1	0	1	1	0
	0	1	0	1	1	0		0	1	1	0	0	1
	0	1	1	0	0	1		0	1	1	0	1	0
	0	1	1	0	1	0		1	0	0	1	0	1
	1	0	0	1	0	1		1	0	0	1	1	0
	1	0	0	1	1	0		1	0	1	0	0	1
	1	0	1	0	0	1		1	0	1	0	1	0
	1	0	1	0	1	0		0	1	0	1	0	1

NOTES: — EC = ECI • ((UPDN • $\overline{LD}$)+LD) • ENB • Q1 • Q2 • Q3...
+ ECI • ((UPDN • $\overline{LD}$ • ENB)+$\overline{ENB}$) • NQ1 • NQ2 • NQ3...
— CY = ECI • UPDN • $\overline{LD}$ • ENB • Q1 • Q2 • Q3...
— BW = ECI • $\overline{UPDN}$ • $\overline{LD}$ • ENB • NQ1 • NQ2 • NQ3...
— The various end count signals are generated with combinatorial logic, thus under certain conditions a short pulse will occur. Therefore, these signals should not be used as a clock signal or for any other edge triggered signal.

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
ECI	0.22	pF
DATAn	0.20	pF
UPDN	0.20	pF
LD	0.31	pF
ENB	0.20	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Parameter	Signal Path	Min.	Typ.	Max.	Units
Setup	ECI to CL	2.3 + n(0.42)	4.9 + n(0.77)	10.4 + n(2.17)	ns
Hold	ECI to CL	0	0	0	ns
Setup	DATAn to CL	1.3 − n(0.035)	2.3 − n(0.078)	5.0 − n(0.21)	ns
Hold	DATAn to CL	0	0	0	ns
Setup	UPDN to CL	2.3 + n(0.034)	4.8 + n(0.024)	11.7 − n(0.13)	ns
Hold	UPDN to CL	0	0	0	ns
Setup	LD to CL	2.9 + n(0.012)	7.5 + n(0.026)	14.0 + n(0.069)	ns
Hold	LD to CL	0	0	0	ns
Setup	ENB to CL	3.1 + n(0.001)	6.8 + n(0.026)	15.2 + n(0.069)	ns
Hold	ENB to CL	0	0	0	ns
Setup	NMR (Inactive) to CL	1.8 + n(0.013)	2.9 − n(0.010)	3.9 − n(0.088)	ns
Hold	NMR (Inactive) to CL	0	0	0	ns

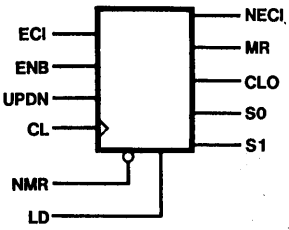
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	CL to Qn	1.3 + n(0.035)	2.3 + n(0.078)	5.1 + n(0.21)	ns
Tphl	CL to Qn	1.2 + n(0.035)	2.3 + n(0.078)	5.3 + n(0.21)	ns
Tplh	CL to NQn	1.5 + n(0.035)	2.8 + n(0.078)	6.4 + n(0.21)	ns
Tphl	CL to NQn	1.5 + n(0.035)	2.9 + n(0.078)	6.8 + n(0.21)	ns
Tphl	NMR to Qn	1.4 + n(0.033)	2.7 + n(0.073)	6.2 + n(0.20)	ns
Tplh	NMR to NQn	1.6 + n(0.033)	3.1 + n(0.073)	7.2 + n(0.20)	ns
Tplh (n=1)	CL to EC CUPP EC CUPP2 CY BW	2.3 2.4 2.7 2.7	4.7 4.9 5.6 5.7	11.2 11.6 13.6 14.2	ns
Tplh (2≤n≤12)	CL to EC CUPP EC CUPP2 CY BW	1.9 + n(0.49) 2.0 + n(0.49) 2.3 + n(0.49) 2.3 + n(0.49)	3.8 + n(0.93) 4.0 + n(0.93) 4.7 + n(0.93) 4.8 + n(0.93)	8.7 + n(2.58) 9.0 + n(2.58) 10.8 + n(2.58) 11.4 + n(2.58)	ns
Tphl	CL to EC CUPP EC CUPP2 CY BW	2.5 + n(0.035) 2.6 + n(0.035) 3.0 + n(0.035) 2.9 + n(0.035)	4.8 + n(0.078) 5.0 + n(0.078) 5.9 + n(0.078) 5.9 + n(0.078)	11.4 + n(0.21) 12.0 + n(0.21) 14.6 + n(0.21) 14.3 + n(0.21)	ns
Tplh	ECI to EC CUPP EC CUPP2 CY BW	0.7 + n(0.45) 0.9 + n(0.45) 1.2 + n(0.45) 1.2 + n(0.45)	1.1 + n(0.85) 1.3 + n(0.85) 2.0 + n(0.85) 2.1 + n(0.85)	2.0 + n(2.38) 2.3 + n(2.38) 4.1 + n(2.38) 4.7 + n(2.38)	ns
Tplh (n=1)	NMR to EC CUPP EC CUPP2 CY BW	2.6 2.7 3.0 3.0	5.0 5.2 5.9 6.0	12.3 12.7 14.5 15.1	ns
Tplh (2≤n≤12)	NMR to EC CUPP EC CUPP2 CY BW	2.1 + n(0.45) 2.2 + n(0.45) 2.5 + n(0.45) 2.5 + n(0.45)	4.1 + n(0.85) 4.3 + n(0.85) 5.0 + n(0.85) 5.1 + n(0.85)	8.8 + n(2.38) 9.1 + n(2.38) 10.9 + n(2.38) 11.5 + n(2.38)	ns
Tphl	NMR to EC CUPP EC CUPP2 CY BW	2.6 + n(0.033) 2.7 + n(0.033) 3.1 + n(0.033) 2.9 + n(0.033)	4.7 + n(0.073) 4.9 + n(0.073) 5.8 + n(0.073) 5.8 + n(0.073)	11.1 + n(0.20) 11.7 + n(0.20) 14.3 + n(0.20) 14.0 + n(0.20)	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Qn	0.33	0.74	1.96	0.47	0.68	1.19	ns/pF
NQn	0.33	0.74	1.96	0.46	0.68	1.20	ns/pF
EC CUPP	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF
EC CUPP2	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF
CY	0.33	0.74	1.95	0.46	0.68	1.18	ns/pF
BW	0.33	0.74	1.95	0.46	0.68	1.19	ns/pF

CUPC — TELESCOPING UP/DOWN COUNTER CONTROL



Logic Table

Inputs						Outputs				
CL	ECI	UPDN	LD	ENB	NMR	CLO	NECI	S0	S1	MR
X	X	X	X	X	0	1	X	X	X	1
↑	X	X	X	X	1	↑	X	X	X	0
0	X	X	X	X	1	0	X	X	X	0
1	X	X	X	X	1	1	X	X	X	0
X	X	0	0	1	X	X	X	0	0	X
X	X	1	0	1	X	X	X	0	1	X
X	X	X	X	0	X	X	X	1	0	X
X	X	X	1	1	X	X	X	1	1	X
X	0	X	X	X	X	X	1	X	X	X
X	1	X	X	X	X	X	0	X	X	X

CUPC Description

Function: Telescoping Up/Down Counter Control
Grid Count: 195

Pin Description

External Pins	
CL	Clock Input
ECI	End Count Input
UPDN	Count Up/Down Input (Up—Active High)
LD	Load Input
ENB	Enable Input
NMR	Master Reset Input (Asynchronous, Active Low)
Telescoping Interconnect Pins	
CLO	Clock Output
NECI	End Count Output
S0	Control Output (LSB)
S1	Control Output (MSB)
MR	Master Reset Output (Asynchronous, Active High)

NOTE: ECI must be tied high into the least significant counter block.

Input Capacitance

Input Name	Max.	Units
CL	0.15	pF
ECI	0.10	pF
UPDN	0.20	pF
LD	0.31	pF
ENB	0.20	pF
NMR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

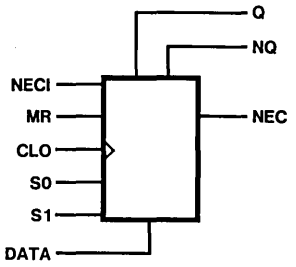
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CL to CLO	0.7	1.2	2.5	0.4	1.0	2.8	ns
NMR to CLO	0.7	1.3	3.2	0.6	1.2	3.1	ns
ECI to NECI	0.1	0.2	0.4	0.2	0.2	0.3	ns
LD to S0	0.6	1.0	2.0	0.4	0.9	2.5	ns
ENB to S0	0.8	1.5	3.2	0.6	1.2	3.3	ns
UPDN to S1	0.5	0.8	1.7	0.5	1.0	2.7	ns
LD to S1	0.6	1.0	2.0	0.4	1.1	3.0	ns
ENB to S1	0.4	0.8	1.7	0.6	1.4	3.7	ns
NMR to MR	0.4	0.9	2.2	0.5	1.0	2.4	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLO	0.23	0.52	1.38	0.34	0.51	0.94	ns/pF
NECI	1.24	2.84	7.82	1.70	2.63	4.94	ns/pF
S0	0.23	0.52	1.38	0.34	0.51	0.94	ns/pF
S1	0.23	0.52	1.37	0.34	0.51	0.97	ns/pF
MR	0.33	0.73	1.95	0.47	0.68	1.19	ns/pF

CUPB — TELESCOPING UP/DOWN COUNTER BODY



Logic Table

Inputs						Outputs		
CLO	NECI	DATA	S0	S1	MR	Q	NQ	NEC
1	1	X	X	X	1	0	1	1
1	0	X	X	0	1	0	1	0
1	0	X	X	1	1	0	1	1
0	1	X	X	X	0	Q_0	NQ_0	1
0	0	X	X	0	0	Q_0	NQ_0	Q_0
0	0	X	X	1	0	Q_0	NQ_0	NQ_0
↑	0	X	0	0	0	NQ_0	Q_0	NQ_0
↑	1	X	0	0	0	Q_0	NQ_0	1
↑	0	X	0	1	0	NQ_0	Q_0	Q_0
↑	1	X	0	1	0	Q_0	NQ_0	1
↑	0	X	1	0	0	Q_0	NQ_0	Q_0
↑	1	X	1	0	0	Q_0	NQ_0	1
↑	x	0	1	1	0	0	1	1
↑	0	1	1	1	0	1	0	0
↑	1	1	1	1	0	1	0	1
1	1	X	X	X	0	Q_0	NQ_0	1
1	0	X	X	0	0	Q_0	NQ_0	Q_0
1	0	X	X	1	0	Q_0	NQ_0	NQ_0

NOTES: — A CLO signal transition to 1 when MR is 1 will be transparent to the user when the control cell is attached to a group of body cells.

— $\overline{NEC} = \overline{NECI} \cdot ((UPDN \cdot LD) + \overline{LD}) \cdot ENB \cdot Q + \overline{NECI} \cdot ((\overline{UPDN} \cdot \overline{LD} \cdot ENB) + \overline{ENB}) \cdot NQ$.

— NEC cannot be used as a final end count output signal; a cap cell (CUPP or CUPP2) must be used if external circuitry is to be connected to an end count signal.

CUPB Description

Function: Telescoping Up/Down Counter Body
Grid Count: 429

Pin Description

External Pins	
DATA	Data Input
Q	Output
NQ	Complemented Output
Telescoping Interconnect Pins	
CLO	Clock Input
NECI	End Count Input
S0	Control Input (LSB)
S1	Control Input (MSB)
MR	Master Reset Input (Asynchronous, Active High)
NEC	End Count Output

Input Capacitance

Input Name	Max.	Units
CLO	0.15	pF
NECI	0.10	pF
DATA	0.20	pF
S0	0.20	pF
S1	0.20	pF
MR	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
NECI to CLO	3.0	6.5	14.5	0	0	0	ns
DATA to CLO	2.0	3.5	7.5	0	0	0	ns
S0 to CLO	3.0	6.5	14.5	0	0	0	ns
S1 to CLO	2.5	3.0	11.5	0	0	0	ns
MR (Inactive) to CLO	2.0	3.0	4.0	0	0	0	ns

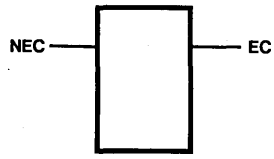
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CLO to Q	0.6	1.1	2.6	0.5	1.1	2.8	ns
MR to Q	—	—	—	1.0	1.8	4.0	ns
CLO to NQ	0.8	1.6	3.9	0.8	1.7	4.3	ns
MR to NQ	1.2	2.2	5.0	—	—	—	ns
NECI to NEC	0.4	0.6	1.4	0.3	0.6	1.9	ns
CLO to NEC	1.3	2.6	6.4	1.1	2.5	6.9	ns
S1 to NEC	0.4	0.8	1.8	0.4	0.9	3.0	ns
MR to NEC	1.7	3.1	7.2	1.6	3.1	8.3	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Q	0.33	0.74	1.96	0.47	0.68	1.19	ns/pF
NQ	0.33	0.74	1.96	0.46	0.68	1.20	ns/pF
NEC	1.24	2.84	7.83	1.51	2.52	4.76	ns/pF

CUPP — TELESCOPING UP/DOWN COUNTER CAP



Logic Table

Inputs	Outputs
NEC	EC
0	1
1	0

NOTE: EC is generated with combinatorial logic, thus under certain conditions a short pulse will occur. Therefore, EC should not be used as a clock signal or for any other edge triggered signal.

CUPP Description

Function: Telescoping Up/Down Counter End Count Driver
Grid Count: 26

Pin Description

External Pins	
EC	End Count Output
Telescoping Interconnect Pins	
NEC	End Count Input

Input Capacitance

Input Name	Max.	Units
NEC	0.28	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

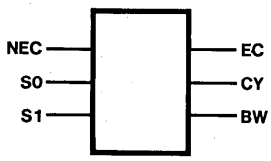
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
NEC to EC	0.1	0.2	0.3	0.2	0.2	0.3	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
EC	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF

CUPP2 — TELESCOPING UP/DOWN COUNTER CAP



Logic Table

Inputs			Outputs		
S0	S1	NEC	EC	CY	BW
X	X	1	0	0	0
0	0	0	1	0	1
0	1	0	1	1	0
1	0	0	1	0	0
1	1	0	1	0	0

NOTE: EC, CY, and BW are generated with combinatorial logic, thus under certain conditions a short pulse will occur. Therefore, these signals should not be used as a clock signal or for any other edge triggered signal.

CUPP2 Description

Function: Telescoping Up/Down Counter End Count/Carry/Borrow Driver
Grid Count: 143

Pin Description

External Pins	
EC CY BW	End Count Output Carry Output Borrow Output
Telescoping Interconnect Pins	
NEC S0 S1	End Count Input Control Input (LSB) Control Input (MSB)

Input Capacitance

Input Name	Max.	Units
NEC	0.36	pF
S0	0.28	pF
S1	0.23	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

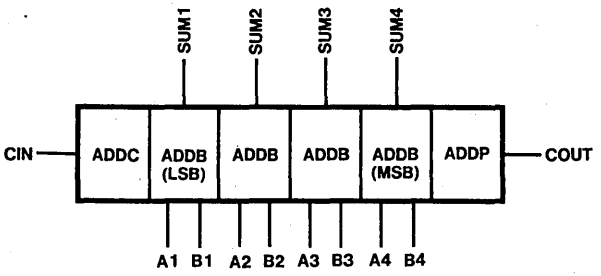
Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
NEC to EC	0.1	0.2	0.3	0.2	0.2	0.3	ns
NEC to CY	0.4	0.9	2.1	0.6	1.1	2.9	ns
S0 to CY	0.4	1.0	2.7	0.8	1.4	3.7	ns
S1 to CY	0.6	1.1	2.8	0.7	1.4	3.7	ns
NEC to BW	0.4	0.9	2.2	0.5	1.0	2.6	ns
S0 to BW	0.4	0.9	2.3	0.7	1.4	3.3	ns
S1 to BW	0.4	1.0	2.6	0.9	1.6	3.7	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
EC	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF
CY	0.33	0.74	1.95	0.46	0.68	1.18	ns/pF
BW	0.33	0.74	1.95	0.46	0.68	1.19	ns/pF

TELESCOPING ADDER (ADDC, ADDB, ADDP)

Example: 4-bit adder



Logic Table

Inputs			Outputs	
CINn	An	Bn	SUMn	COUTn
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

NOTES: — COUT = COUTn(msb)
— CINn(lsb) = CIN, CINn = COUTn−1
— A cap cell (ADDP) must be used if COUT is to be connected to circuitry external to a telescoping block.

Telescoping Adder Description

Function: Cascadable Binary Ripple Adder ($1 \leq n \leq 12$ bits)
Grid Count: With ADDP — $52 + n(169)$
Without ADDP — $13 + n(169)$

Pin Description

CIN	Carry Input
An	Data Input
Bn	Data Input
SUMn	Output
COUT	Carry Output

Input Capacitance

Input Name	Max.	Units
CIN	0.31	pF
An	0.26	pF
Bn	0.26	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

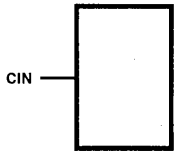
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	An, Bn to SUMn	1.3	2.4	5.6	ns
Tphl	An, Bn to SUMn	0.9	2.2	6.0	ns
Tplh (2≤n≤12)	A1, B1 to SUMn	−0.2 + n(0.62)	−0.3 + n(1.24)	−1.6 + n(3.34)	ns
Tphl (2≤n≤12)	A1, B1 to SUMn	−0.3 + n(0.62)	−0.3 + n(1.24)	−0.9 + n(3.34)	ns
Tplh	CIN to SUMn	−0.1 + n(0.62)	−0.3 + n(1.24)	−1.3 + n(3.34)	ns
Tphl	CIN to SUMn	−0.2 + n(0.62)	−0.3 + n(1.24)	−0.6 + n(3.34)	ns
Tplh (n=1)	A1, B1 to COUT	1.0	2.1	5.0	ns
Tplh (2≤n≤12)	A1, B1 to COUT	0.1 + n(0.62)	0.1 + n(1.24)	−0.4 + n(3.34)	ns
Tphl (n=msb)	An, Bn to COUT	0.8	1.6	3.8	ns
Tplh	CIN to COUT	0.2 + n(0.62)	0.1 + n(1.24)	−0.1 + n(3.34)	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
SUMn	0.33	0.73	1.93	0.47	0.67	1.23	ns/pF
COUT	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF

ADDC — TELESCOPING ADDER CONTROL



ADDC Description

Function: Telescoping Adder Control
Grid Count: 13

Pin Description

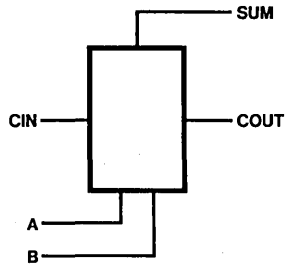
External Pins	
CIN	Carry Input Feedthrough

NOTE: CIN is routed directly through ADDC without buffering to the Carry Input signal (CIN) of the least significant ADDB cell.

Input Capacitance

Input Name	Max.	Units
CIN	0.05	pF

ADDB — TELESCOPING ADDER BODY



Logic Table

Inputs			Outputs	
CIN	A	B	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

NOTE: A cap cell (ADDP) must be used if COUT is to be connected to circuitry external to a telescoping block.

ADDB Description

Function: Telescoping Adder Body
Grid Count: 169

Pin Description

External Pins	
A	Data Input
B	Data Input
SUM	Output
Telescoping Interconnect Pins	
CIN	Carry Input
COUT	Carry Output

Input Capacitance

Input Name	Max.	Units
CIN	0.26	pF
A	0.26	pF
B	0.26	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

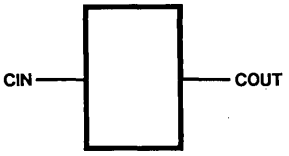
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
A to SUM	1.3	2.4	5.6	0.9	2.2	6.0	ns
B to SUM	1.3	2.4	5.6	0.9	2.2	6.0	ns
CIN to SUM	0.5	0.9	2.0	0.4	0.9	2.7	ns
A to COUT	0.2	0.5	1.0	0.3	0.6	1.5	ns
B to COUT	0.2	0.5	1.0	0.3	0.6	1.5	ns
CIN to COUT	0.3	0.5	1.3	0.3	0.6	1.5	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
SUM	0.33	0.73	1.93	0.47	0.67	1.23	ns/pF
COUT	1.24	2.84	7.84	1.51	2.52	4.90	ns/pF

ADDP — TELESCOPING ADDER CAP



Logic Table

Inputs	Outputs
CIN	COUT
0 1	0 1

NOTE: ADDP must be used if COUT is to be connected to circuitry external to a telescoping block.

ADDP Description

Function: Telescoping Adder Carry Out Driver
Grid Count: 39

Pin Description

External Pins	
COUT	Carry Output
Telescoping Interconnect Pins	
CIN	Carry Input

Input Capacitance

Input Name	Max.	Units
CIN	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

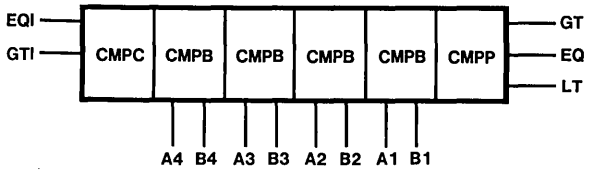
Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
CIN to COUT	0.4	0.6	1.2	0.3	0.7	1.8	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
COUT	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF

TELESCOPING MAGNITUDE COMPARATOR (CMPC, CMPB, CMPP)

Example: 4-bit magnitude comparator



Telescoping Magnitude Comparator Description

Function: Cadcadable Binary Magnitude Comparator ($1 \leq n \leq 12$ bits)
Grid Count: With CMPP $-130 + n(182)$
Without CMPP $-26 + n\ (182)$

Pin Description

EQI	Equal Input
GTI	Greater Than Input
An	Data Input
Bn	Data Input
EQ	Equal Output
GT	Greater Than Output
LT	Less Than Output

Logic Table

Inputs						Outputs		
EQI	GTI	An,Bn	···	A2,B2	A1,B1	EQ	GT	LT
0	0	X	···	X	X	0	0	1
0	1	X	···	X	X	0	1	0
1	0	An>Bn	···	X	X	0	1	0
1	0	An<Bn	···	X	X	0	0	1
1	0	An=Bn	···	A2>B2	X	0	1	0
1	0	An=Bn	···	A2<B2	X	0	0	1
1	0	An=Bn	···	A2=B2	A1<B1	0	1	0
1	0	An=Bn	···	A2=B2	A1>B1	0	0	1
1	0	An=Bn	···	A2=B2	A1=B1	1	0	0

Input Capacitance

Input Name	Max.	Units
EQI	0.27	pF
GTI	0.15	pF
An	0.21	pF
Bn	0.27	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh (n=1)	A1, B1 to EQ	1.4	2.9	7.5	ns
Tphl (n=1)	A1, B1 to EQ	1.8	3.1	6.8	ns
Tplh (2≤n≤12)	A1, B1 to EQ	0.9 + n(0.47)	1.9 + n(1.02)	4.9 + n(2.62)	ns
Tphl (2≤n≤12)	A1, B1 to EQ	1.1 + n(0.67)	1.9 + n(1.18)	4.1 + n(2.69)	ns
Tplh (n=1)	A1, B1 to GT	1.3	2.5	6.4	ns
Tphl (n=1)	A1, B1 to GT	1.4	2.7	6.1	ns
Tplh (2≤n≤12)	A1, B1 to GT	1.0 + n(0.47)	2.1 + n(1.02)	5.3 + n(2.62)	ns
Tphl (2≤n≤12)	A1, B1 to GT	1.2 + n(0.47)	2.2 + n(1.02)	6.5 + n(2.62)	ns
Tplh (n=1)	A1, B1 to LT	1.6	3.1	6.8	ns
Tphl (n=1)	A1, B1 to LT	1.4	2.9	7.2	ns
Tplh (2≤n≤12)	A1, B1 to LT	1.0 + n(0.47)	1.8 + n(1.02)	5.6 + n(2.62)	ns
Tphl (2≤n≤12)	A1, B1 to LT	1.0 + n(0.47)	2.1 + n(1.02)	5.0 + n(2.62)	ns

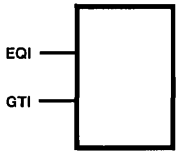
Intrinsic Propagation Delay (Cont'd.)

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	EQI to EQ	0.7 + n(0.47)	1.4 + n(1.02)	3.4 + n(2.62)	ns
Tphl	EQI to EQ	0.8 + n(0.67)	1.4 + n(1.18)	3.2 + n(2.69)	ns
Tplh	EQI to GT	0.8 + n(0.47)	1.6 + n(1.02)	3.8 + n(2.62)	ns
Tphl	EQI to GT	0.7 + n(0.47)	1.4 + n(1.02)	3.4 + n(2.62)	ns
Tplh	EQI to LT	0.7 + n(0.47)	1.4 + n(1.02)	3.1 + n(2.62)	ns
Tphl	EQI to LT	0.7 + n(0.47)	1.4 + n(1.02)	3.4 + n(2.62)	ns
Tplh	GTI to GT	0.9 + n(0.42)	1.7 + n(0.78)	4.3 + n(1.98)	ns
Tphl	GTI to GT	0.9 + n(0.35)	1.7 + n(0.65)	3.7 + n(1.68)	ns
Tplh	GTI to LT	0.7 + n(0.35)	1.3 + n(0.65)	2.8 + n(1.68)	ns
Tphl	GTI to LT	0.9 + n(0.42)	1.7 + n(0.78)	4.0 + n(1.98)	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
EQ	0.33	0.73	1.95	0.46	0.68	1.17	ns/pF
GT	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF
LT	0.32	0.75	2.06	0.46	0.68	1.19	ns/pF

CMPC — TELESCOPING MAGNITUDE COMPARATOR CONTROL



CMPC Description

Function: Telescoping Magnitude Comparator Control
Grid Count: 26

Pin Description

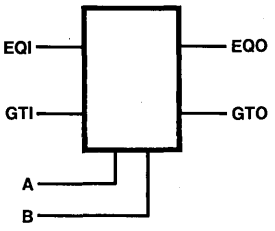
External Pins	
EQI	Equal Input Feedthrough
GTI	Greater Than Input Feedthrough

NOTE: EQI and GTI are routed directly through CMPC without buffering to the Equal Input (EQI) and Greater Than Input (GTI) signals respectively of the most significant CMPB cell. EQI must be tied high and GTI must be tied low into the most significant magnitude comparator block.

Input Capacitance

Input Name	Max.	Units
EQI	0.05	pF
GTI	0.05	pF

CMPB — TELESCOPING MAGNITUDE COMPARATOR BODY



Logic Table

Inputs				Outputs	
EQI	GTI	A	B	EQO	GTO
0	0	X	X	0	0
0	1	X	X	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0

NOTE: EQO and GTO cannot be used as final output signals; a cap cell (CMPP) must be used if external circuitry is to be connected to a final output signal.

CMPB Description

Function: Telescoping Magnitude Comparator Body
Grid Count: 182

Pin Description

External Pins	
A	Data Input
B	Data Input
Telescoping Interconnect Pins	
EQI	Equal Input
GTI	Greater Than Input
EQO	Equal Output
GTO	Greater Than Output

Input Capacitance

Input Name	Max.	Units
EQI	0.22	pF
GTI	0.10	pF
A	0.21	pF
B	0.22	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

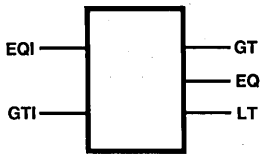
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
A to EQO	0.4	0.9	2.4	0.6	1.1	2.5	ns
B to EQO	0.4	0.9	2.4	0.6	1.1	2.5	ns
EQI to EQO	0.2	0.4	0.9	0.3	0.6	1.6	ns
A to GTO	0.3	0.5	1.3	0.3	0.7	1.9	ns
B to GTO	0.3	0.5	1.3	0.3	0.7	1.9	ns
EQI to GTO	0.3	0.6	1.3	0.4	0.8	3.4	ns
GTI to GTO	0.3	0.5	1.2	0.2	0.4	1.2	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
EQO	1.24	2.84	7.84	1.70	2.63	4.94	ns/pF
GTO	1.24	2.84	7.84	1.51	2.52	4.75	ns/pF

CMPP — TELESCOPING MAGNITUDE COMPARATOR CAP



Logic Table

Inputs		Outputs		
EQI	GTI	EQ	GT	LT
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	1	1	0

CMPP Description

Function: Telescoping Magnitude Comparator Equal/Greater Than/Less Than Driver
Grid Count: 104

Pin Description

External Pins	
EQ GT LT	Equal Output Greater Than Output Less Than Output
Telescoping Interconnect Pins	
EQI GTI	Equal Input Greater Than Input

Input Capacitance

Input Name	Max.	Units
EQI	0.50	pF
GTI	0.50	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
EQI to EQ	0.4	0.6	1.2	0.3	0.7	1.8	ns
GTI to GT	0.4	0.6	1.2	0.3	0.7	1.8	ns
EQI to LT	0.1	0.3	0.9	0.4	0.6	0.9	ns
GTI to LT	0.1	0.3	0.9	0.4	0.6	0.9	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
EQ	0.33	0.73	1.95	0.46	0.68	1.17	ns/pF
GT	0.33	0.73	1.95	0.46	0.68	1.18	ns/pF
LT	0.32	0.75	2.06	0.46	0.68	1.19	ns/pF

PCI, PCIH — NON-INVERTING CMOS INPUT BUFFERS

Logic Table

Inputs	Outputs
PAD	OUT
0 1	0 1

PCI Description

Function: Non-Inverting CMOS Input Buffer, Normal Drive

PCIH Description

Function: Non-Inverting CMOS Input Buffer, High Drive

Pin Description

PAD OUT	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	3.5			V	
VIL			1.2	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS

Input Capacitance

Input Name	Max.	Units
PAD (PCI)	0.31	pF
PAD (PCIH)	0.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

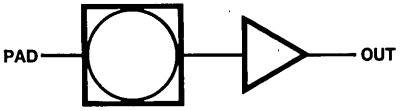
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PCI PAD to OUT	0.5	0.4	0.6	0.4	0.8	1.6	ns
PCIH PAD to OUT	0.7	0.6	0.9	0.5	1.0	2.1	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
OUT (PCI)	0.39	0.78	1.96	0.47	0.69	1.19	ns/pF
OUT (PCIH)	0.13	0.25	0.63	0.13	0.20	0.37	ns/pF

PTI, PTIH — NON-INVERTING TTL INPUT BUFFERS



Logic Table

Inputs	Outputs
PAD	OUT
0 1	0 1

PTI Description

Function: Non-Inverting TTL Input Buffer, Normal Drive

PTIH Description

Function: Non-Inverting TTL Input Buffer, High Drive

Pin Description

PAD OUT	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	2.0			V	
VIL			0.8	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS

Input Capacitance

Input Name	Max.	Units
PAD (PTI)	0.40	pF
PAD (PTIH)	0.50	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

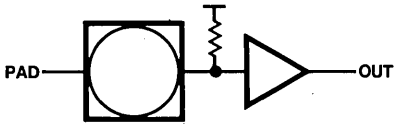
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PTI PAD to OUT	0.6	0.8	1.2	0.6	1.3	3.6	ns
PTIH PAD to OUT	0.8	1.1	1.9	0.8	1.9	5.5	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
OUT (PTI)	0.35	0.76	1.99	0.52	0.77	1.32	ns/pF
OUT (PTIH)	0.11	0.24	0.63	0.16	0.27	0.58	ns/pF

PTIRH — NON-INVERTING TTL INPUT BUFFER WITH PULL-UP RESISTOR



Logic Table

Inputs	Outputs
PAD	OUT
0 1	0 1

PTIRH Description

Function: Non-Inverting TTL Input Buffer with Pull-Up Resistor, High Drive

Pin Description

PAD OUT	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
Pull-Up Resistance	2.1	4.1	9.4	kOhm	
VIH	2.0			V	
VIL			0.8	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS

Input Capacitance

Input Name	Max.	Units
PAD	0.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

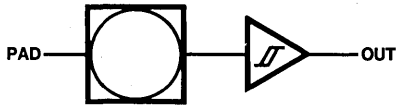
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD to OUT	0.8	1.1	1.9	0.8	1.9	5.5	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
OUT	0.11	0.24	0.63	0.16	0.27	0.58	ns/pF

PISH — NON-INVERTING TTL SCHMITT TRIGGER INPUT BUFFER



Logic Table

Inputs	Outputs
PAD	OUT
0	0
1	1

PISH Description

Function: Non-Inverting TTL Schmitt Trigger Input Buffer, High Drive

Pin Description

PAD	Data Input
OUT	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VT+	2.4	2.0	2.0	V	
VT−	0.8	0.9	1.0	V	
Vhys	0.4	0.6	0.65	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS

Input Capacitance

Input Name	Max.	Units
PAD	0.50	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

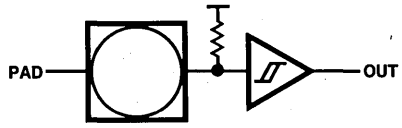
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD to OUT	2.6	3.1	5.0	1.3	3.3	11.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
OUT	0.16	0.35	0.94	0.22	0.38	0.82	ns/pF

PISRH — NON-INVERTING TTL SCHMITT TRIGGER INPUT BUFFER WITH PULL-UP RESISTOR



Logic Table

Inputs	Outputs
PAD	OUT
0 1	0 1

PISRH Description

Function: Non-Inverting TTL Schmitt Trigger Input Buffer with Pull-Up Resistor, High Drive

Pin Description

PAD OUT	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
Pull-Up Resistance	2.1	4.1	9.4	kOhm	
VT+	2.4	2.0	2.0	V	
VT−	0.8	0.9	1.0	V	
Vhys	0.4	0.6	0.65	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS

Input Capacitance

Input Name	Max.	Units
PAD	0.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

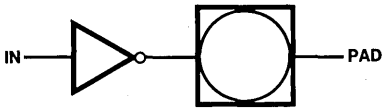
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD to OUT	2.6	3.1	5.0	1.3	3.3	11.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
OUT	0.16	0.35	0.94	0.22	0.38	0.82	ns/pF

PCO — INVERTING CMOS OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0	1
1	0

PCO Description

Function: Inverting CMOS Output Buffer, 3.2 mA

Pin Description

IN	Data Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	4.0			V	IOH = −2.4 mA
VOL			0.4	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

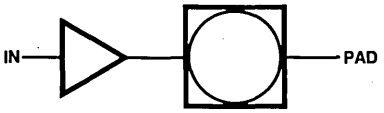
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	0.6	1.2	3.0	0.7	1.3	3.0	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.043	0.095	0.28	0.054	0.084	0.16	ns/pF

PCNO — NON-INVERTING CMOS OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0	0
1	1

PCNO Description

Function: Non-Inverting CMOS Output Buffer, 3.2 mA

Pin Description

IN	Data Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	4.0			V	IOH = −2.4 mA
VOL			0.4	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

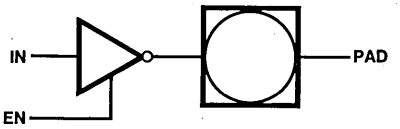
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	0.8	1.5	3.6	0.8	1.6	3.9	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.043	0.096	0.28	0.051	0.084	0.16	ns/pF

PCOT — 3-STATE INVERTING CMOS OUTPUT BUFFER



Logic Table

Inputs		Outputs
IN	EN	PAD
X	0	Z
0	1	1
1	1	0

PCOT Description

Function: 3-State Inverting CMOS Output Buffer, 3.2 mA

Pin Description

IN	Data Input
EN	3-State Enable Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	4.0			V	IOH = −2.4 mA
VOL			0.4	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF
EN	0.30	pF

3-State Output Capacitance

Output Name	Max.	Units
PAD(z)	2.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

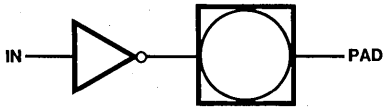
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	0.8	1.6	3.9	ns
Tphl	IN to PAD	0.8	1.6	4.0	ns
Tpzh	EN to PAD	0.8	1.7	4.6	ns
Tpzl	EN to PAD	0.5	1.2	2.5	ns
Tphz	EN to PAD	1.2	2.0	3.8	ns
Tplz	EN to PAD	0.8	1.2	2.1	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PAD	0.055	0.13	0.35	0.064	0.11	0.23	ns/pF

PTO — INVERTING TTL OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0	1
1	0

PTO Description

Function: Inverting TTL Output Buffer, 3.2 mA Sink

Pin Description

IN	Data Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	2.4			V	IOH = −6.5 mA
VOL			0.45	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

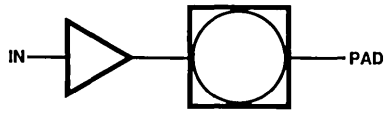
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	0.6	1.2	2.8	0.7	1.4	3.2	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.026	0.058	0.16	0.072	0.12	0.23	ns/pF

PTNO — NON-INVERTING TTL OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0	0
1	1

PTNO Description

Function: Non-Inverting TTL Output Buffer, 3.2 mA Sink

Pin Description

IN	Data Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	2.4			V	IOH = −6.5 mA
VOL			0.45	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

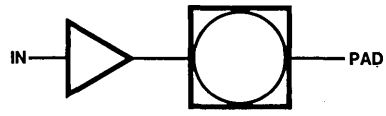
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	0.7	1.4	3.4	0.8	1.7	4.1	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.029	0.059	0.16	0.068	0.11	0.23	ns/pF

PTNO3 — NON-INVERTING TTL OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0 1	0 1

PTNO3 Description

Function: Non-Inverting TTL Output Buffer, 9.6 mA Sink

Pin Description

IN PAD	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	2.4			V	IOH = −2.7 mA
VOL			0.45	V	IOL = 9.6 mA

Input Capacitance

Input Name	Max.	Units
IN	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

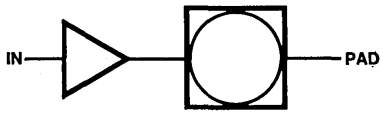
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	0.9	1.6	3.8	0.6	1.3	3.3	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.056	0.13	0.39	0.052	0.087	0.17	ns/pF

PTNO5 — NON-INVERTING TTL OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0 1	0 1

PTNO5 Description

Function: Non-Inverting TTL Output Buffer, 16 mA Sink

Pin Description

IN PAD	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	2.4			V	IOH = −2.7 mA
VOL			0.45	V	IOL = 16.0 mA

Input Capacitance

Input Name	Max.	Units
IN	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

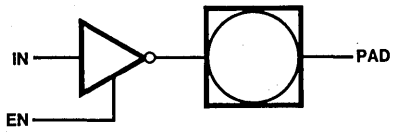
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	1.1	2.0	4.6	0.7	1.4	3.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.055	0.13	0.38	0.044	0.073	0.16	ns/pF

PTOT — 3-STATE INVERTING TTL OUTPUT BUFFER



Logic Table

Inputs		Outputs
IN	EN	PAD
X	0	Z
0	1	1
1	1	0

PTOT Description

Function: 3-State Inverting TTL Output Buffer, 3.2 mA Sink

Pin Description

IN	Data Input
EN	3-State Enable Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	2.4			V	IOH = −6.5 mA
VOL			0.45	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF
EN	0.30	pF

3-State Output Capacitance

Output Name	Max.	Units
PAD(z)	2.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

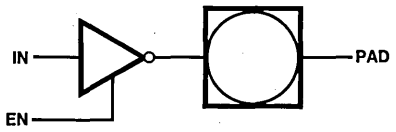
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	0.7	1.5	3.6	ns
Tphl	IN to PAD	0.9	1.7	4.3	ns
Tpzh	EN to PAD	0.5	1.5	3.9	ns
Tpzl	EN to PAD	0.6	1.3	3.1	ns
Tphz	EN to PAD	1.2	2.0	3.8	ns
Tplz	EN to PAD	0.8	1.2	2.1	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PAD	0.037	0.087	0.23	0.083	0.15	0.32	ns/pF

PTOT3 — 3-STATE INVERTING TTL OUTPUT BUFFER



Logic Table

Inputs		Outputs
IN	EN	PAD
X	0	Z
0	1	1
1	1	0

PTOT3 Description

Function: 3-State Inverting TTL Output Buffer, 9.6 mA Sink

Pin Description

IN	Data Input
EN	3-State Enable Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	2.4			V	IOH = −2.7 mA
VOL			0.45	V	IOL = 9.6 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF
EN	0.30	pF

3-State Output Capacitance

Output Name	Max.	Units
PAD(z)	2.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

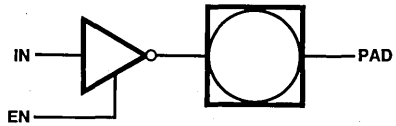
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	0.9	1.7	4.0	ns
Tphl	IN to PAD	0.7	1.3	3.3	ns
Tpzh	EN to PAD	0.6	1.7	4.1	ns
Tpzl	EN to PAD	0.5	1.2	3.1	ns
Tphz	EN to PAD	1.1	1.6	3.4	ns
Tplz	EN to PAD	1.1	1.8	3.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PAD	0.060	0.15	0.42	0.063	0.12	0.26	ns/pF

PTOT5 — 3-STATE INVERTING TTL OUTPUT BUFFER



Logic Table

Inputs		Outputs
IN	EN	PAD
X	0	Z
0	1	1
1	1	0

PTOT5 Description

Function: 3-State Inverting TTL Output Buffer, 16 mA Sink

Pin Description

IN	Data Input
EN	3-State Enable Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	2.4			V	IOH = −2.7 mA
VOL			0.45	V	IOL = 16.0 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF
EN	0.30	pF

3-State Output Capacitance

Output Name	Max.	Units
PAD(z)	2.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

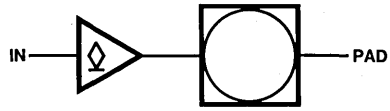
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	1.2	2.1	4.8	ns
Tphl	IN to PAD	0.7	1.4	3.6	ns
Tpzh	EN to PAD	0.7	1.7	4.4	ns
Tpzl	EN to PAD	0.5	1.3	3.3	ns
Tphz	EN to PAD	1.1	1.7	3.2	ns
Tplz	EN to PAD	1.5	2.2	3.9	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PAD	0.056	0.14	0.41	0.055	0.099	0.23	ns/pF

PTND — NON-INVERTING TTL OPEN-DRAIN OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0 1	0 1

PTND Description

Function: Non-Inverting TTL Open-Drain Output Buffer, 3.2 mA Sink

Pin Description

IN PAD	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOL			0.45	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

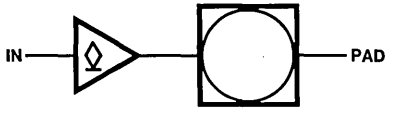
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	0.9	1.4	2.7	0.5	1.1	2.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.50	0.55	0.63	0.11	0.15	0.26	ns/pF

PTND3 — NON-INVERTING TTL OPEN-DRAIN OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0 1	0 1

PTND3 Description

Function: Non-Inverting TTL Open-Drain Output Buffer, 9.6 mA Sink

Pin Description

IN PAD	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOL			0.45	V	IOL = 9.6 mA

Input Capacitance

Input Name	Max.	Units
IN	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

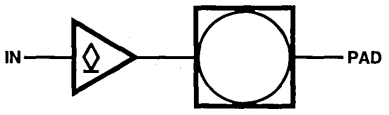
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	1.1	1.9	3.6	0.5	1.2	2.9	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.54	0.61	0.70	0.051	0.079	0.15	ns/pF

PTND5 — NON-INVERTING TTL OPEN-DRAIN OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0 1	0 1

PTND5 Description

Function: Non-Inverting TTL Open-Drain Output Buffer, 16 mA Sink

Pin Description

IN PAD	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOL			0.45	V	IOL = 16.0 mA

Input Capacitance

Input Name	Max.	Units
IN	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

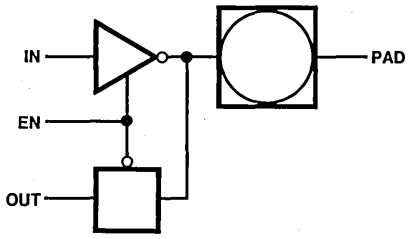
Intrinsic Propagation Delay

Signal Path	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
IN to PAD	1.5	2.4	4.5	0.6	1.3	3.3	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PAD	0.53	0.61	0.71	0.039	0.068	0.14	ns/pF

PCIO — CMOS I/O BUFFER



Logic Table

Inputs			Outputs	
IN	EN	PAD	PAD	OUT
0	1	1	1	OUT_0
1	1	0	0	OUT_0
X	0	0	Z	0
X	0	1	Z	1

PCIO Description

Function: CMOS I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, 3.2 mA

Pin Description

IN	Internal Data Input
EN	Enable Input
PAD	Bi-Directional Pin; External Output, External Data Input
OUT	Internal Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	3.5			V	
VIL			1.2	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS
VOH	4.0			V	IOH = −2.4 mA
VOL			0.4	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF
EN	0.30	pF
PAD	2.40	pF

3-State Output Capacitance

Input Name	Max.	Units
PAD(z)	2.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time Min.	Setup Time Typ.	Setup Time Max.	Hold Time Min.	Hold Time Typ.	Hold Time Max.	Units
PAD to EN	2.0	3.0	5.5	1.2	2.6	6.0	ns

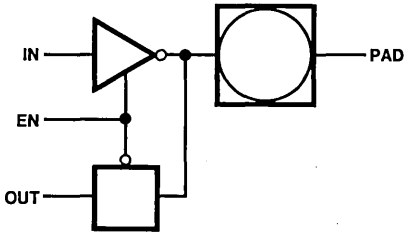
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	1.0	1.8	4.1	ns
Tphl	IN to PAD	0.9	2.0	4.8	ns
Tplh	PAD to OUT	1.4	2.6	5.0	ns
Tphl	PAD to OUT	1.2	2.5	5.7	ns
Tpzh	EN to PAD	0.8	1.9	5.1	ns
Tpzl	EN to PAD	0.6	1.3	3.0	ns
Tphz	EN to PAD	1.2	2.2	4.5	ns
Tplz	EN to PAD	0.9	1.5	3.0	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.10	0.10	0.20	0.10	0.10	0.20	ns/pF
OUT	0.40	0.80	2.10	0.40	0.70	1.20	ns/pF

PTIO — TTL I/O BUFFER



Logic Table

Inputs			Outputs	
IN	EN	PAD	PAD	OUT
0	1	1	1	OUT_0
1	1	0	0	OUT_0
X	0	0	Z	0
X	0	1	Z	1

PTIO Description

Function: TTL I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, 3.2 mA Sink

Pin Description

IN	Internal Data Input
EN	Enable Input
PAD	Bi-Directional Pin; External Output, External Data Input
OUT	Internal Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	2.0			V	
VIL			0.8	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS
VOH	2.4			V	IOH = −6.5 mA
VOL			0.45	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF
EN	0.30	pF
PAD	2.40	pF

3-State Output Capacitance

Output Name	Max.	Units
PAD(z)	2.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time			Hold Time			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PAD to EN	2.0	3.0	5.5	1.2	2.6	6.0	ns

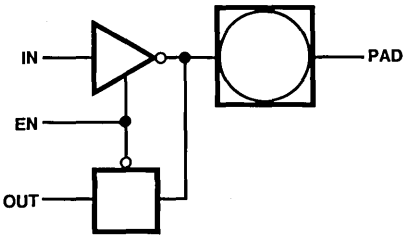
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	0.8	1.6	3.8	ns
Tphl	IN to PAD	1.1	2.2	5.3	ns
Tplh	PAD to OUT	1.3	2.4	5.2	ns
Tphl	PAD to OUT	1.5	3.2	8.0	ns
Tpzh	EN to PAD	0.6	1.7	4.0	ns
Tpzl	EN to PAD	0.7	1.5	3.5	ns
Tphz	EN to PAD	1.2	2.2	4.5	ns
Tplz	EN to PAD	0.9	1.5	3.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PAD	0.10	0.10	0.20	0.10	0.10	0.20	ns/pF
OUT	0.40	0.70	2.00	0.50	0.70	1.10	ns/pF

PTIO3 — TTL I/O BUFFER



Logic Table

Inputs			Outputs	
IN	EN	PAD	PAD	OUT
0	1	1	1	OUT_0
1	1	0	0	OUT_0
X	0	0	Z	0
X	0	1	Z	1

PTIO3 Description

Function: TTL I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, 9.6 mA Sink

Pin Description

IN	Internal Data Input
EN	Enable Input
PAD	Bi-Directional Pin; External Data Input
OUT	Internal Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	2.0			V	
VIL			0.8	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS
VOH	2.4			V	IOH = −6.5 mA
VOL			0.45	V	IOL = 9.6 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF
EN	0.30	pF
PAD	2.40	pF

3-State Output Capacitance

Output Name	Max.	Units
PAD(z)	2.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD to EN	2.0	3.0	5.5	1.0	2.1	4.8	ns

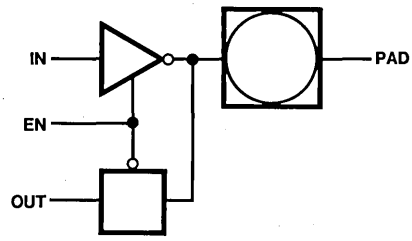
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	0.9	1.8	4.1	ns
Tphl	IN to PAD	0.7	1.4	3.4	ns
Tplh	PAD to OUT	1.2	2.0	4.4	ns
Tphl	PAD to OUT	1.4	3.0	7.1	ns
Tpzh	EN to PAD	0.7	1.8	4.5	ns
Tpzl	EN to PAD	0.6	1.4	3.5	ns
Tphz	EN to PAD	1.1	2.0	3.8	ns
Tplz	EN to PAD	1.3	2.1	4.1	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.059	0.14	0.42	0.063	0.11	0.24	ns/pF
OUT	0.30	0.70	2.00	0.50	0.70	1.10	ns/pF

PTIO5 — TTL I/O BUFFER



Logic Table

Inputs			Outputs	
IN	EN	PAD	PAD	OUT
0	1	1	1	OUT_0
1	1	0	0	OUT_0
X	0	0	Z	0
X	0	1	Z	1

PTIO5 Description

Function: TTL I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, 16 mA Sink

Pin Description

IN	Internal Data Input
EN	Enable Input
PAD	Bi-Directional Pin; External Output, External Data Input
OUT	Internal Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	2.0			V	
VIL			0.8	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS
VOH	2.4			V	IOH = − 6.5 mA
VOL			0.45	V	IOL = 16.0 mA

Input Capacitance

Input Name	Max.	Units
IN	0.20	pF
EN	0.30	pF
PAD	2.40	pF

Input Capacitance

Output Name	Max.	Units
PAD(z)	2.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD to EN	2.0	3.0	5.5	1.0	2.1	4.8	ns

Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	1.2	2.2	4.9	ns
Tphl	IN to PAD	0.7	1.5	3.7	ns
Tplh	PAD to OUT	1.2	2.0	4.4	ns
Tphl	PAD to OUT	1.4	3.0	7.1	ns
Tpzh	EN to PAD	0.8	1.8	4.7	ns
Tpzl	EN to PAD	0.6	1.5	3.7	ns
Tphz	EN to PAD	1.2	2.0	3.8	ns
Tplz	EN to PAD	1.6	2.6	5.0	ns

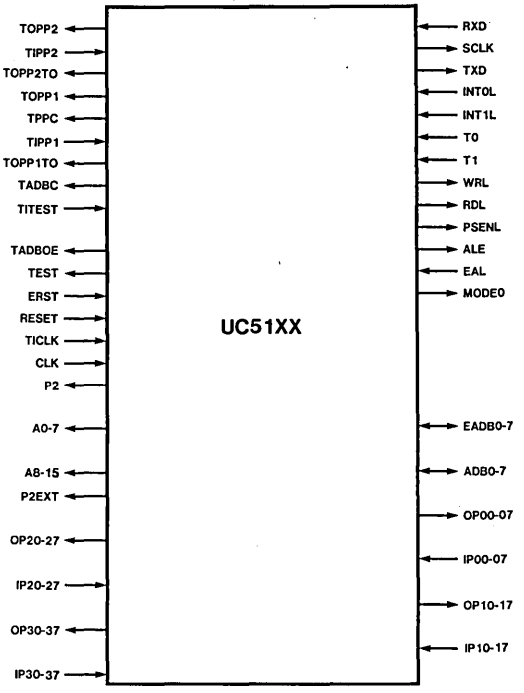
Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.056	0.41	0.14	0.055	0.095	0.22	ns/pF
OUT	0.30	0.70	2.00	0.50	0.70	1.10	ns/pF

VLSiCEL Elements and LSI Functions 4

CHAPTER 4
VLSiCEL ELEMENTS AND LSI FUNCTIONS

UC51 — 80C51BH MICROCONTROLLER CORE



Functional Pin Diagram G40208

- Cell Version of the 80C51BH Microcontroller; Code and Functional Compatibility with the Standard Product Assured.
- 12 MHz Operation.
- On-Chip ROM Expandable to 16K Bytes:

  UC5100 — No ROM
  UC5104 — 4K Bytes ROM
  UC5108 — 8K Bytes ROM
  UC5116 — 16K Bytes ROM
- UC52xx Cores Expand the On-Chip RAM from 128 Bytes to 256 Bytes
- Demultiplexed I/O Ports Make Available all Functional Signals of the 80C51BH.
- Tested and Verified Against Standard Product Test Programs, Providing a Guaranteed 0.1% AQL or Better.
- Code Development Supported with the Configurable UC51 Emulator Design Kit.

UC51 DESCRIPTION

The UC51 core is the cell version of Intel's industry standard 80C51BH Microcontroller. The UC51 can be used in conjunction with the Intel 1.5 Micron CHMOS III Cell Library, allowing the designer to implement a semi-custom integrated circuit that includes an 80C51BH core and design specific support logic.

The UC51 has on-chip Read Only Memory (ROM), available in 4K, 8K, and 16K byte configurations. The use of additional ROM expands the code space of the UC51 core beyond the 4K bytes available with the 80C51BH standard product, in most cases alleviating the need for external program memory. A ROM-less version of the UC51 is also available, providing the user an 80C31BH compatible VLSiCEL core.

All UC51xx cores contain 128 bytes of on-chip Static RAM. This RAM can be expanded to 256 bytes via the UC52xx cores. These cores provide the additional RAM while maintaining the exact functionality of their UC51xx counterparts.

In partitioning the 80C51BH into a cell compatible format, the standard product's I/O drivers and pin multiplexers were eliminated. As a result, all functional pins of the 80C51BH are available to the UC51 user as "raw" I/O. This expanded I/O capability, totalling 117 user available signals, allows design flexibility not previously available to MCS-51 designers. Intel has also assured compatibility with a cell library of over 150 logic elements while maintaining code and functional compatibility with the standard product. Designers can, however, take advantage of the UC51's demultiplexed I/O ports to optimize their application code.

For a complete functional description of the MCS-51 architecture, including a description of the instruction set and a programmer's reference guide, refer to Chapters 5-7, the "80C31BH/80C51BH 8-Bit Microcontrollers" data sheet in Chapter 8, and AP-252 "Designing with the 80C51BH" in Chapter 9 of the Intel *Embedded Controller Handbook.*

Pin Description

80C51BH Pin #	80C51BH Name	UC51 Pin Name	UC51 Pin Description
Port 1			
1-8	P1.0 to 1.7	IP10-17	(Input Port 1, Address = 90H) An 8-bit input port. Port 1 is not used for the address input during ROM verify or any other test modes. Unused inputs must be connected to VSS. This port is equivalent to the Port 1 input function of the 80C51BH.
		OP10-17	(Output Port 1, Address = 90H) An 8-bit output port. This port is equivalent to the Port 1 output function of the 80C51BH.

Pin Description (Cont'd.)

80C51BH Pin #	80C51BH Name	UC51 Pin Name	UC51 Pin Description
9	RST	RESET	(Internal Reset) A logic 1 on this pin applied for 12 oscillator periods resets the UC51. It is provided to give the user the ability to reset the core using on-chip logic. If only off-chip reset is desired, tie RESET to VSS.
		ERST	(External Reset) MANDATORY PACKAGE PIN. This pin must be brought off-chip and serves as the external reset signal. A logic 1 on this pin resets the entire chip both in normal user operation mode and in test modes. No internal user logic should drive this line.
Port 3			
10-17	RXD/P3.0- *RD/P3.7	IP30-37	(Input Port 3, Address = B0H) An 8-bit input port. Unused inputs must be connected to VSS. This port is equivalent to the Port 3 input function of the 80C51BH.
		OP30-37	(Output Port 3, Address = B0H) An 8-bit output port. This port is equivalent to the Port 3 output function of the 80C51BH.
10	RXD/P3.0	RXD	(Serial Input Port) Serial port input pin for all 4 serial port modes.
11	TXD/P3.1	TXD	(Serial Output Port) Serial port output pin for all 4 serial port modes.
		SCLK	(Serial Clock) Serial port shift clock (same as Mode 0 TXD output on the 80C51BH). SCLK is fixed at one-sixth of the input clock (CLK or TICLK). SCLK is output only during Serial Mode 0.
		MODE0	(Serial Port MODE0 Control Pin) Active when Mode 0 serial port configuration is selected. MODE0 is used to recombine Port 3 with RXD, TXD, and SCLK to create an 80C51BH-type Serial Mode 0. If MODE0 is not used to recreate the 80C51BH type function then, in Mode 0, the serial data will enter through RXD, exit through TXD, and SCLK will output the shift clock.
12	*INT0/P3.2	INT0L	(Interrupt 0) External Interrupt 0.
13	*INT1/P3.3	INT1L	(Interrupt 1) External Interrupt 1.
14	T0/P3.4	T0	(Timer/Counter 0) Timer/Counter 0 external input pin.

Pin Description (Cont'd.)

80C51BH Pin #	80C51BH Name	UC51 Pin Name	UC51 Pin Description
Port 3 (Cont'd.)			
15	T1/P3.5	T1	(Timer/Counter 1) Timer/Counter 1 external input pin.
16	*WR/P3.6	WRL	(Write Strobe) Write strobe for external data memory.
17	*RD/P3.7	RDL	(Read Strobe) Read strobe for external data memory.
18	XTAL2		
19	XTAL1	CLK	(Input Clock) During normal user operation, CLK is the input clock to the UC51. The CLK signal must be supplied. If an on-chip oscillator is required in the design, CLK should be connected to the output of the oscillator companion cell, POSC. Otherwise, CLK can be driven by an input pad, or by on-chip user logic.
		TICLK	(Tester Input Clock) MANDATORY PACKAGE PIN. TICLK is selected as the input clock during test. TICLK must be driven from off-chip, allowing the tester to control the UC51 frequency.
20	VSS		
Port 2			
21-28	P2.0-2.7/ A8-A15	IP20-27	(Input Port 2, Address = A0H) An 8-bit input port. Unused inputs must be connected to VSS. This port is equivalent to the Port 2 input function of the 80C51BH.
		P2EXT	(Port 2/A8-15 Select Signal) P2EXT is an active high output signal. During internal program execution (EAL high), P2EXT is active if a MOVX @ DPTR instruction is executed. During external program execution (EAL low or when the addressing limit of the internal ROM has been exceeded), P2EXT is always active except during a MOVX @ Ri or a Port 2 instruction. P2EXT can be used to reconstruct the 80C51BH Port 2 output function.
		OP20-27	(Output Port 2, Address = A0H) An 8-bit output port. This port is equivalent to the Port 2 output function of the 80C51BH. Unlike the 80C51BH Port 2, OP2 is not used to output the high-order address during fetches to internal program memory (see P2EXT).
		A8-15	(High Address Bus) A8-15 are the 8 most significant bits of the 16-bit address bus for external program and data memory. This address bus is completely separate from Port 2 and can be latched (see P2EXT).

Pin Description (Cont'd.)

80C51BH Pin #	80C51BH Name	UC51 Pin Name	UC51 Pin Description
29	*PSEN	PSENL	(Program Store Enable) PSENL is an output and may be used to enable the output drivers of external program memory.
30	ALE	ALE	(Address Latch Enable) In conjunction with PSENL, ALE is used for external program memory expansion. In conjunction with WRL or RDL, ALE is used for external data memory expansion. When ALE is a logic 1, the memory address is available on EADB0-7 and ADB0-7. The entire latched address is available on A0-15.
31	*EA	EAL	(External Access Control) EAL is an input. The state of this pin defines the location of program memory (0 = external, 1 = internal). Regardless of what state EAL is, the core will fetch instructions from the external memory if the address is pointing to a location outside of the internal ROM boundary. EAL is not present on the UC5100 core.
Port 0			
32-39	P0.0-0.7	IP00-07	(Input Port 0, Address = 80H) An 8-bit input port completely separate from the address/data bus; consequently, any use of ADB and EADB has no effect on IP00-07. Unused inputs must be connected to VSS.
		OP00-07	(Output Port 0, Address = 80H) An 8-bit output port completely separate from the address/data bus; consequently any use of ADB or EADB has no effect on OP00-07.
		A0-7	(Low Address Bus) A0-A7 are the 8 least significant bits of the 16-bit address bus for external program and data memory. This address bus can be latched on ALE.
		ADB0-7	(Address/Data Bus) Bidirectional address/data bus for on-chip connection to user logic. During normal user operation, ADB0-7 acts as the data bus and lower 8 bits of address for program and data memory (see TADBOE).
		EADB0-7	(External Address/Data Bus) MANDATORY PACKAGE PINS. Bidirectional address/data bus to be brought off-chip for testing and for off-chip program and data memory accesses. No on-chip logic may be connected to EADB0-7. The EADB and ADB busses are electrically connected during normal user operation (see TADBOE).
		TADBOE	(Test Address/Data Bus Output Enable Control) TADBOE controls the direction of the PADB companion cells which are connected to EADB. A low level TADBOE 3-states the PADB cells. TADBOE must be combined with user logic to control PADB if user logic is driving ADB0-7.

Pin Description (Cont'd.)

80C51BH Pin #	80C51BH Name	UC51 Pin Name	UC51 Pin Description
40	VCC		
Additional UC51 Signals			
		P2	(Phase 2 Clock Output) Signal frequency ½ of CLK or TICLK.
		TEST	Test is active high during all UC51 test modes.
		TPPC	(Test Programmable Pin Control) Control signal for TOPP/UOS selection to the PRGPIN1 and PRGPIN2 companion cells. TPPC is a logic 1 during test and selects the test programmable pin outputs (TOPP) from TOPP1/UOS and TOPP2/UOS. TPPC remains low during normal user operation and selects the user output signals (UOS) from TOPP1/UOS and TOPP2/UOS.
		TIPP1	(Test Programmable Pin 1 Input) MANDATORY PACKAGE PIN — MULTIPLEXED WITH TOPP1. Functions as the path for programmable pin 1 inputs during test. TIPP1 is input to the UC51 from the PRGPIN1 companion cell.
		TOPP1	(Test Programmable Pin 1 Output) MANDATORY PACKAGE PIN — MULTIPLEXED WITH TIPP1. Functions as the path for programmable pin 1 outputs during test. TOPP1 is output from the UC51 to the PRGPIN1 companion cell.
		TOPP1TO	(Test Programmable Pin 1 Output Enable Control) TOPP1TO controls the direction of the PRGPIN1 companion cell during test. TOPP1TO is low during normal user operation, configuring TPP1 as an output.
		TIPP2	(Test Programmable Pin 2 Input) MANDATORY PACKAGE PIN — MULTIPLEXED WITH TOPP2. Functions as the path for programmable pin 2 inputs during test. TIPP2 is input to the UC51 from the PRGPIN2 companion cell.
		TOPP2	(Test Programmable Pin 2 Output) MANDATORY PACKAGE PIN — MULTIPLEXED WITH TIPP2. Functions as the path for programmable pin 2 outputs during test. TOPP2 is output from the UC51 to the PRGPIN2 companion cell.
		TOPP2TO	(Test Programmable Pin 2 Output Enable Control) TOPP2TO controls the direction of the PRGPIN2 companion cell during test. TOPP2TO is low during normal user operation, configuring TPP2 as an output.

Pin Description (Cont'd.)

80C51BH Pin #	80C51BH Name	UC51 Pin Name	UC51 Pin Description
Additional UC51 Signals (Cont'd.)			
		TADBC	(Test Enable Control) Control signal for ALE/UOS selection to the PRGPINALE companion cell. TADBC is a logic 1 during test and selects Address Latch Enable from ALE/UOS. TADBC remains low during normal user operation and selects the user output signal (UOS) from ALE/UOS.
		TITEST	(Test Enable Input) MANDATORY PACKAGE PIN — MULTIPLEXED WITH ALE. The state of this pin during reset (RESET or ERST high) is one of the variables for defining the operating mode of the chip. TITEST is input to the UC51 from the PRGPINALE companion cell.

MANDATORY UC51 SIGNALS AND UC51 COMPANION CELLS

In partitioning the 80C51BH into a cell compatible format, the I/O drivers were removed. This allows the UC51 core to be integrated with a cell library of over 150 logic functions into a user defined ASIC. Because of this, those UC51 signals which are required external to the ASIC device must be buffered off-chip as package pins. Mandatory UC51 signals are signals which require package pins for every UC51 based design.

There are thirteen mandatory UC51 signals, most of which are used for production testing of the UC51 core and which only nominally affect the design of the user specific application logic. Ten of these required signals are normally used in any design. The other three (TPP1, TPP2, and TALE) may be reconfigured by the designer as output signals during normal user operation.

There are two types of mandatory UC51 signals: non-multiplexed and multiplexed. Most of the mandatory signals are routed off-chip using UC51 companion cells. The major task of the companion cells is to multiplex the applicable UC51 signals between test and normal user operation modes and/or to act as buffers for the signals. Companion cells can also be used to reconfigure the demultiplexed I/O ports of the UC51 into their 80C51BH standard product equivalents. Refer to the individual data sheets of the various companion cells for more information on their operation. Refer to the "Designing with the UC51 Microcontroller Core" module in the Intel cell-based design, engineering workstation environment documentation for more information on designing the UC51 for test and the application of UC51 companion cells.

Non-Multiplexed Signals

These two pins keep the same function whether the device is executing in test mode or normal user operation mode.

ERST (External Reset Input)

The ERST pin is required in all UC51 designs to allow the tester to initialize the UC51 and is brought on-chip through the PRESET companion cell.

TICLK (Tester Input Clock)

For testing purposes, the UC51 frequency source must be externally controlled. If the signal CLK is to be generated externally by either a crystal or any other clock source, TICLK and CLK should be connected to the same package pin.

Multiplexed Signals

The function of these eleven pins depends on whether the device is executing in test mode or normal user operation mode.

EADB0-7 (External Address/Data Bus)

EADB0-7 is accessed during production test to fully check out the UC51 core and the application logic. EADB0-7 is brought off-chip through the PADB companion cell. EADB0-7 is also available for those applications requiring an off-chip address/data bus for external program and data memory.

TPP1 (TIPP1/TOPP1/UOS)

TPP1 interfaces between the UC51 and the package pins through the PRGPIN1 companion cell. During test, TPP1 functions as an I/O path through TIPP1 and TOPP1. During normal user operation, TPP1 can be configured as a user output signal (UOS).

TPP2 (TIPP2/TOPP2/UOS)

TPP2 interfaces between the UC51 and the package pins through the PRGPIN2 companion cell. During test, TPP2 functions as an I/O path through TIPP2 and TOPP2. During normal user operation, TPP2 can be configured as a user output signal (UOS).

TALE (TITEST/ALE/UOS)

TALE interfaces between the UC51 and the package pins through the PRGPINALE companion cell. TITEST is input to the UC51 during reset to enable the UC51 to enter a test mode. ALE is output from the UC51 when the UC51 is configured in any test mode requiring external memory access. During normal user operation, TALE can be configured as a user output signal (UOS).

Input Capacitance

Input Name	UC5100 Max.	UC5104 Max.	UC5108 Max.	UC5116 Max.	Units
ADB0-7	1.3	1.5	1.6	1.8	pF
CLK	1.1	1.3	1.4	1.6	pF
EADB0-7	1.3	1.5	1.6	1.8	pF
EAL	—	1.3	1.4	1.6	pF
ERST	1.2	1.4	1.5	1.7	pF
INT0L	1.1	1.3	1.4	1.6	pF
INT1L	1.1	1.3	1.4	1.6	pF
IP00-07	0.1	0.1	0.1	0.1	pF
IP10-17	0.1	0.1	0.1	0.1	pF
IP20-27	0.1	0.1	0.1	0.1	pF
IP30-37	0.1	0.1	0.1	0.1	pF
RESET	1.5	1.7	1.8	2.0	pF
RXD	1.1	1.3	1.4	1.6	pF
T0	1.1	1.3	1.4	1.6	pF
T1	1.1	1.3	1.4	1.6	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

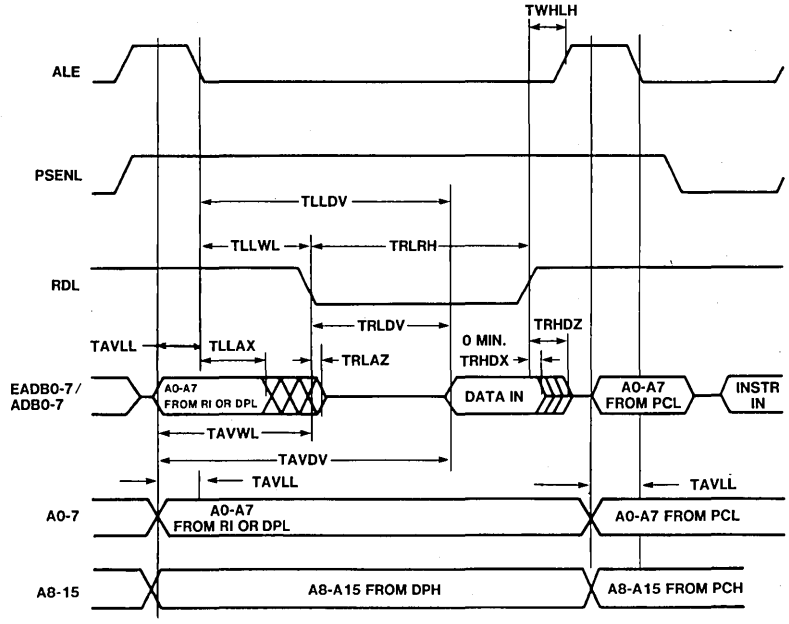
NOTE: A.C. Characteristics are given to the edge of the UC51 core. Additional delays will apply in connecting UC51 signals to package pins through selected I/O buffer cells.

External Program and Data Memory Characteristics

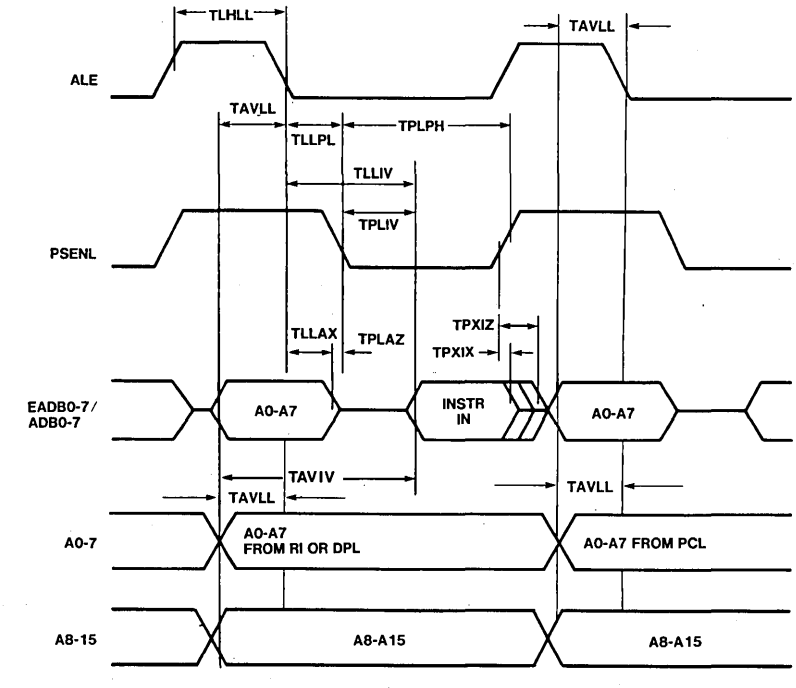
Symbol	Parameter	12 MHz OSC		Variable Oscillator		Units
		Min.	Max.	Min.	Max.	
1/TCLCL	OSCILLATOR FREQUENCY			3.5	12	MHz
TLHLL	ALE PULSE WIDTH	166		2TCLCL −0.3		ns
TAVLL	ADDRESS VALID to ALE LOW	83		TCLCL −0.6		ns
TLLAX	ADDRESS HOLD AFTER ALE LOW	84		TCLCL +0.2		ns
TLLIV	ALE LOW to VALID INSTR. IN		325		4TCLCL −8.1	ns
TLLPL	ALE LOW to PSENL LOW	85		TCLCL +1.2		ns
TPLPH	PSENL PULSE WIDTH	250		3TCLCL		ns
TPLIV	PSENL LOW to VALID INSTR. IN		237		3TCLCL −12.8	ns
TPXIX	INPUT INSTR. HOLD AFTER PSENL	0		0		ns
TPXIZ	INPUT INSTR. FLOAT AFTER PSENL		78		TLCLC −5.0	ns
TAVIV	ADDRESS to VALID INSTR. IN		406		5TCLCL −10.2	ns
TPLAZ	PSENL LOW to ADDRESS FLOAT		2.6		2.6	ns
TRLRH	RDL PULSE WIDTH	500		6TCLCL +0.5		ns
TWLWH	WRL PULSE WIDTH	500		6TCLCL +0.5		ns
TRLDV	RDL LOW to VALID DATA IN		410		5TCLCL −7.0	ns
TRHDX	DATA HOLD AFTER RDL	0		0		ns
TRHDZ	DATA FLOAT AFTER RDL		165		2TCLCL −2.0	ns
TLLDV	ALE LOW to VALID DATA IN		658		8TCLCL −8.1	ns
TAVDV	ADDRESS to VALID DATA IN		740		9TCLCL −10.2	ns
TLLWL	ALE LOW to RDL or WRL LOW	230	270	3TCLCL −20.0	3TCLCL +20.0	ns
TAVWL	ADDRESS VALID to RDL or WRL LOW	332		4TCLCL −0.8		ns
TQVWX	DATA VALID to WRL TRANSITION	83		TCLCL −0.8		ns
TWHQX	DATA HOLD AFTER WRL	84		TCLCL +0.3		ns
TRLAZ	RDL LOW to ADDRESS FLOAT		0		0	ns
TWHLH	RDL or WRL HIGH to ALE HIGH	68	98	TCLCL −15.0	TCLCL +15.0	ns

Load Dependent Delay

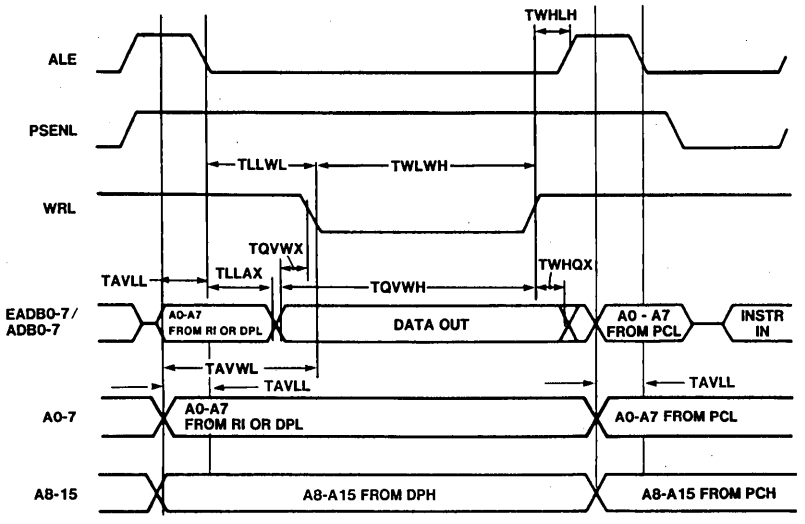
Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
A0-7	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
A8-15	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
ADB0-7	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
ALE	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
EADB0-7	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
MODE0	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
OP00-07	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
OP10-17	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
OP20-27	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
OP30-37	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
P2	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
P2EXT	1.8	1.9	2.2	1.7	1.8	1.8	ns/pF
PSENL	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
RDL	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
SCLK	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
TADBC	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
TADBOE	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
TPPC	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
TXD	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF
WRL	0.2	0.3	0.9	0.2	0.3	0.6	ns/pF



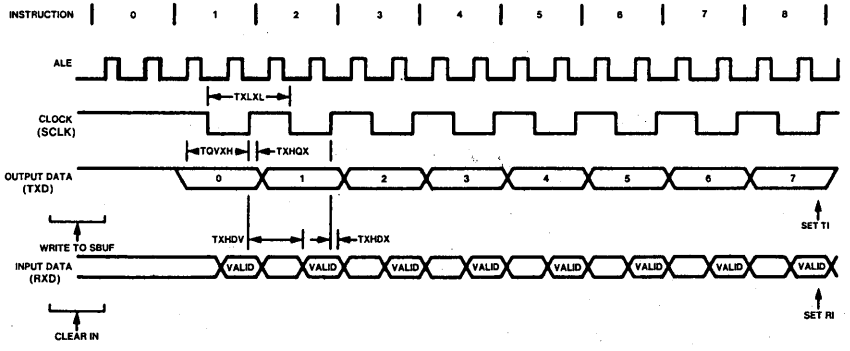
External Data Memory Read Cycle G40208



External Program Memory Read Cycle G40208

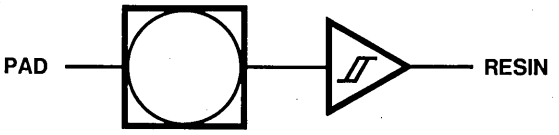


External Data Memory Write Cycle G40208



Shift Register Mode Timing Waveforms G40208

PRESET — RESET INPUT BUFFER



Logic Table

Inputs	Outputs
PAD	RESIN
0 1	0 1

PRESET Description

Function: Reset Input Buffer; Non-Inverting, Schmitt Trigger. This cell is used to buffer the off-chip reset signal (ERST) into a UC51 core.

Pin Description

PAD RESIN	External Reset Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	3.5			V	VDD = 5 V
VIL			0.9	V	VSS = 0 V
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS

Input Capacitance

Input Name	Max.	Units
PAD	4.00	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

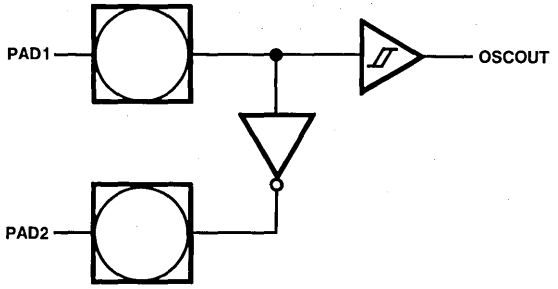
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD to RESIN	1.0	1.6	3.5	1.2	2.5	6.6	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
RESIN	0.16	0.35	0.93	0.22	0.32	0.56	ns/pF

POSC — OSCILLATOR



Logic Table

Inputs	Outputs	
PAD1	PAD2	OSCOUT
0	1	0
1	0	1

POSC Description

Function: Oscillator, Frequency Range to 16 MHz. This cell is used to provide the clock input to a UC51 core (CLK) from an external crystal. In test mode, the external tester clock is connected directly to PAD1, with PAD2 left unconnected. Refer to the 80C51BH data sheet in the Intel *Embedded Controller Handbook* for the recommended implementation of an external crystal. POSC is designed to function over the full range of operating frequencies of the UC51.

Pin Description

PAD1	Oscillator Input
PAD2	Oscillator Feedback Output
OSCOUT	Clock Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	2.0			V	
VIL			0.8	V	
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS

Input Capacitance

Input Name	Max.	Units
PAD1	4.77	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

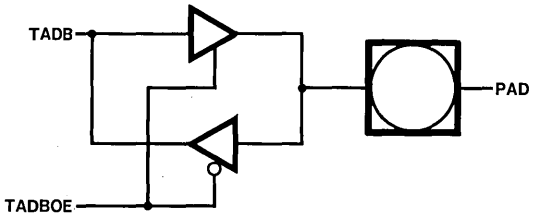
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD1 to OSCOUT	1.4	2.6	6.2	1.2	2.4	5.7	ns
PAD1 to PAD2	0.4	0.7	1.5	0.7	0.9	1.5	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
OSCOUT	0.16	0.35	0.93	0.22	0.32	0.56	ns/pF
PAD2	0.11	0.24	0.57	0.17	0.26	0.48	ns/pF

PADB — ADDRESS/DATA BUS I/O BUFFER



Logic Table

Inputs			Outputs	
TADB	TADBOE	PAD	TADB	PAD
0	1	0	Z	0
1	1	1	Z	1
0	0	0	0	Z
1	0	1	1	Z

PADB Description

Function: Address/Data Bus I/O Buffer; 3-State Non-Inverting Input, 3-State Non-Inverting TTL Output, 3.2 mA sink. This cell is used to bring the external address/data bus of the UC51 (EADB0-7) off-chip.

Pin Description

TADBOE	Enable Input
TADB	Bi-Directional Pin; Internal Address/Data Bit
PAD	Bi-Directional Pin; External Address/Data Bit

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	1.9			V	VDD = 5 V
VIL			0.9	V	VSS = 0 V
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS
VOH	2.4			V	IOH = −0.08 mA
VOL			0.45	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
TADBOE	0.20	pF
TADB	0.60	pF
PAD	2.85	pF

3-State Output Capacitance

Output Name	Max.	Units
TADB(z)	0.60	pF
PAD(z)	2.85	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

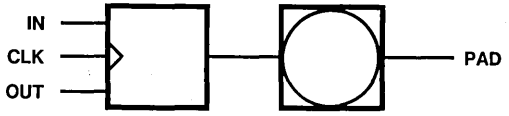
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
TADB to PAD	1.5	2.6	6.6	1.5	3.5	8.0	ns
PAD to TADB	3.0	5.0	9.0	1.5	3.1	8.7	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
TADB	0.30	0.40	0.80	0.20	0.40	0.80	ns/pF
PAD	0.10	0.10	0.20	0.10	0.10	0.20	ns/pF

PTNQB — QUASI-BIDIRECTIONAL I/O BUFFER



Logic Table

Inputs			Outputs	
CLK	IN	PAD	PAD	OUT
X	0	0	0	0
X	1[a]	1	1	1
↓	1	1*	1*	1*
X[b]	1	1*	1*	1*
X[b]	1	0	0	0
X[b]	1	1	1	1

NOTE: * — Weak high state; after a falling edge of CLK with IN = 1, a weak high state will occur internal to the cell on PAD and OUT in the absence of an external input signal on PAD. This state will be overdriven by an external input signal on PAD.

a — This condition is valid only after a state change at IN from 0 to 1 and prior to a falling edge of CLK.

b — Any state or transition of CLK after a falling edge of CLK with IN = 1 where IN remains equal to one.

PTNQB Description

Function: Quasi-Bidirectional I/O Buffer; Non-Inverting TTL Output, 3.2 mA Sink. This cell is used to reconfigure UC51 input and output ports to their equivalent 80C51BH bidirectional port structures.

Pin Description

CLK	P2 Clock Input
IN	Internal Data Input
PAD	Bi-Directional Pin; External Output, External Data Input
OUT	Internal Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VIH	1.9			V	VDD = 5 V
VIL			0.9	V	VSS = 0 V
IIH			10.0	uA	VIH = VDD
IIL			−10.0	uA	VIL = VSS
VOH	2.4			V	IOH = −6.5 mA
VOL			0.45	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
CLK	0.10	pF
IN	0.10	pF
PAD	2.30	pF

Output Capacitance

Output Name	Max.	Units
PAD	2.30	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

Setup and Hold Times

Signal Path	Setup Time			Hold Time			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
IN to CLK	14.0	30.0	67.5	0	0	0	ns

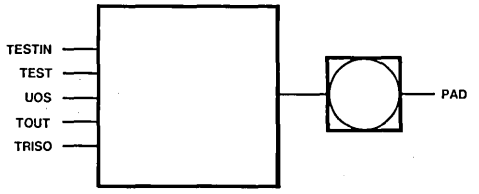
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	1.3	2.5	6.7	1.3	3.0	7.4	ns
PAD to OUT	3.9	5.2	6.9	0.5	4.9	12.4	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.023	0.055	0.16	0.068	0.091	0.15	ns/pF
OUT	0.40	0.77	1.93	0.77	0.83	1.63	ns/pF

PRGPIN — PROGRAMMABLE I/O BUFFER



Logic Table

Inputs					Outputs	
UOS	TESTIN	TEST	TRISO	PAD	PAD	TOUT
0	X	0	0	0	0	0
1	X	0	0	1	1	1
X	0	1	0	0	0	0
X	1	1	0	1	1	1
X	X	X	1	0*	Z	0*
X	X	X	1	0	Z	0
X	X	X	1	1	Z	1

NOTE: * — Weak low state; with TRISO = 1, a weak low state will occur internal to the cell on PAD and TOUT in the absence of an external input signal on PAD. This state will be overdriven by an external input signal on PAD.

PRGPIN Description

Function: Programmable I/O Buffer; 3-State Non-Inverting TTL Output, 3.2 mA Sink. This cell is used to multiplex a UC51 input and output test signal pair with a user definable output signal.

Pin Description

TESTIN	Test Signal Input (From UC51)
UOS	User Output Signal Input
TEST	Select Input (TESTIN or UOS)
TRISO	Enable Input
PAD	Bi-Directional Pin; External Output, External Data Input
TOUT	Test Signal Output (To UC51)

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	2.4			V	IOH = −0.08 mA
VOL			0.45	V	IOL = 3.2 mA

Input Capacitance

Input Name	Max.	Units
TESTIN	0.10	pF
UOS	0.10	pF
TEST	0.10	pF
TRISO	0.10	pF
PAD	2.85	pF

3-State Output Capacitance

Output Name	Max.	Units
PAD(z)	2.85	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

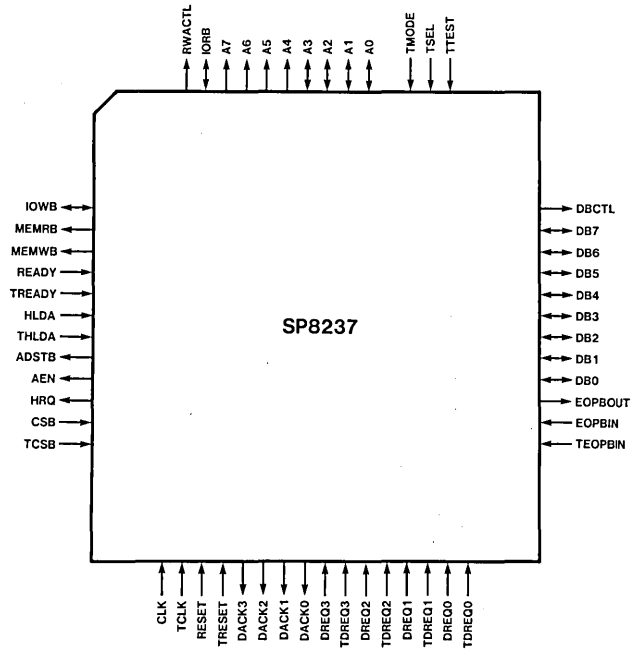
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
UOS to PAD	1.7	3.2	7.6	1.7	3.6	8.8	ns
TESTIN to PAD	1.7	3.2	7.6	1.7	3.6	8.8	ns
PAD to TOUT	2.9	3.4	4.3	0.7	1.5	5.0	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.10	0.10	0.20	0.10	0.10	0.20	ns/pF
TOUT	0.50	0.70	2.00	0.50	0.70	1.10	ns/pF

SP8237 — PROGRAMMABLE DMA CONTROLLER



Functional Pin Diagram G40208

- Cell Version of the 82C37A Programmable DMA Controller; Functional Compatibility with the Standard Product Assured.
- 12.5 MHz Operation.
- Tested and Verified Against Standard Product Test Programs, Providing a Guaranteed 0.1% AQL or Better.
- Enable/Disable Control of Individual DMA Requests.
- Four Independent DMA Channels.
- Independent Auto-Initialization of all Channels.
- Memory-to-Memory Transfers.
- Memory Block Initialization.
- Address Increment or Decrement.
- Directly Expandable to any Number of Channels.
- End of Process Input for Terminating Transfers.
- Software DMA Requests.
- Independent Polarity Control for DREQ and DACK Signals.

SP8237 DESCRIPTION

The Intel SP8237 is a high performance, CHMOS cell version of the industry standard 82C37A Programmable Direct Memory Access (DMA) Controller and is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The SP8237 offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The SP8237 is designed to be used in conjunction with an external 8-bit address register. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to auto-initialize to its original condition following an End of Process.

Each channel has a full 64K address and word count capability.

The SP8237 can be used in conjunction with the Intel 1.5 Micron CHMOS III Cell Library, allowing the designer to implement a semi-custom integrated circuit that includes the SP8237 and design specific support logic.

For a complete functional description of the 82C37 architecture, refer to the "82C37A-5 CHMOS High Performance Programmable DMA Controller" data sheet in the Intel *Microprocessor and Peripheral Handbook.*

Pin Description

Pin Name	Pin Type	Function
CLK TCLK	I	CLOCK INPUT: Clock Input controls the internal operations of the SP8237 and its rate of data transfers.
CSB TCSB	I	CHIP SELECT: Chip Select is an active low input used to select the SP8237 as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
RESET TRESET	I	RESET: Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip-flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY TREADY	I	READY: Ready is an input used to extend the memory read and write pulses from the SP8237 to accomodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.

Pin Description (Cont'd.)

Pin Name	Pin Type	Function
HLDA THLDA	I	HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that is has relinquished control of the system busses.
DREQ0-3 TDREQ0-3	I	DMA REQUEST: The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.
DB0-7	I/O	DATA BUS: The Data Bus lines are bidirectional 3-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the SP8237 control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the SP8237 on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.
IORB	I/O	I/O READ: I/O Read is a bidirectional active low 3-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the SP8237 to access data from a peripheral during a DMA Write transfer.
IOWB	I/O	I/O WRITE: I/O Write is a bidirectional active low 3-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the SP8237. In the Active cycle, it is an output control signal used by the SP8237 to load data to the peripheral during a DMA Read transfer.
EOPBIN TEOPBIN	I	END OF PROCESS INPUT: End of Process Input is an active low input signal used to terminate an active DMA service. The reception of an active EOPBIN signal will cause the SP8237 to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by an active EOPBIN signal unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. EOPBIN should be tied high if it is not used to prevent erroneous end of process inputs.

Pin Description (Cont'd.)

Pin Name	Pin Type	Function
EOPBOUT	0	EOPBOUT: End of Process Output is an active low output signal that indicates the completion of an active DMA service. An active EOPBOUT signal is generated by the SP8237 when the terminal count (TC) for any channel is reached. This causes the SP8237 to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by an active EOPBOUT signal unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, an active EOPBOUT signal will be output when the TC for channel 1 occurs.
A0-3	I/O	ADDRESS: The four least significant address lines are bidirectional 3-state signals. In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.
A4-7	0	ADDRESS: The four most significant address lines are 3-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	0	HOLD REQUEST: HRQ is an active high output signal and is the Hold Request to the CPU. HRQ is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes the SP8237 to issue the HRQ. After HRQ goes active at least one clock (TCY) must occur before HLDA goes active.
DACK0-3	0	DMA ACKNOWLEDGE: DMA Acknowledge outputs are used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines if programmable. Reset initializes them to active low.
AEN	0	ADDRESS ENABLE: Address Enable is an active high output used to enable an external 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers.
ADSTB	0	ADDRESS STROBE: Address Strobe is an active high output used to strobe the upper address byte into an external latch.
MEMRB	0	MEMORY READ: Memory Read is an active low 3-state output used to access data from the selected memory location during a DMA Read or memory-to-memory transfer.
MEMWB	0	MEMORY WRITE: Memory Write is an active low 3-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

Pin Description (Cont'd.)

Pin Name	Pin Type	Function
DBCTL	0	DATA BUS CONTROL: The Data Bus Control signal is used for data bus transceiver control. When this signal is high, DB0-7 are being driven by the SP8237.
RWACTL	0	READ, WRITE, ADDRESS CONTROL: The Read, Write, Address Control Signal is used for Read, Write and Address Bus transceiver control. When this signal is high IORB, MEMRB, IOWB, MEMWB, and A0-7 are being driven by the SP8237.
TMODE, TSEL	I	TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the SP8237 (see table below). The SP8237 can operate in one of three modes: user mode, active test mode, or inactive test mode.

TMODE	TSEL	Function
0	0	User Mode (Normal operation)
0	1	User Mode (Normal operation)
1	0	Inactive Test Mode
1	1	Active Test Mode

TTEST	I	TTEST is an input signal used only in test mode. It has no corresponding user mode signal. TTEST is a mandatory package pin.

NOTE: All signals Txxx are test related input signals. All test related signals except for TTEST, TMODE, and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
A0	1.6	pF
A1	1.8	pF
A2	1.6	pF
A3	1.5	pF
CLK	0.8	pF
CSB	0.2	pF

Input Capacitance (Cont'd.)

Input Name	Max.	Units
DB0	1.2	pF
DB1	1.1	pF
DB2	1.1	pF
DB3	1.5	pF
DB4	1.3	pF
DB5	1.1	pF
DB6	1.4	pF
DB7	1.1	pF
DREQ0	0.4	pF
DREQ1	0.2	pF
DREQ2	0.2	pF
DREQ3	0.2	pF
EOPBIN	0.2	pF
HLDA	0.3	pF
IORB	0.7	pF
IOWB	0.6	pF
READY	0.2	pF
TMODE	1.0	pF
TSEL	1.0	pF

3-State Output Capacitance

Output Name	Max.	Units
A0 (z)	1.6	pF
A1 (z)	1.8	pF
A2 (z)	1.6	pF
A3 (z)	1.5	pF
A4 (z)	1.5	pF
A5 (z)	1.5	pF
A6 (z)	1.4	pF
A7 (z)	1.4	pF
DB0 (z)	1.2	pF
DB1 (z)	1.1	pF
DB2 (z)	1.1	pF
DB3 (z)	1.5	pF
DB4 (z)	1.3	pF
DB5 (z)	1.1	pF
DB6 (z)	1.4	pF
DB7 (z)	1.1	pF
IORB (z)	0.7	pF
IOWB (z)	0.6	pF
MEMRB (z)	0.4	pF
MEMWB (z)	0.4	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

NOTE: A.C. Characteristics are given to the edge of the SP8237 core. Additional delays will apply in connecting SP8237 signals to package pins through selected I/O buffer cells.

DMA (MASTER) MODE

Symbol	Parameter	Min.	Max.	Units
TAEL	AEN HIGH from CLK LOW (SI) Delay Time		41.9	ns
TAET	AEN LOW from CLK HIGH (SI) Delay Time		43.9	ns
TAFAB	Address Active to Float Delay from CLK HIGH		58.4	ns
TAFC	IORB/MEMRB or IOWB/MEMWB Float from CLK HIGH		55.6	ns
TAFDB	DB Active to Float Delay from CLK HIGH		66.8	ns
TAHR	Address from IORB/MEMRB HIGH Hold Time	61.7		ns
TAHS	DB from ADSTB LOW Hold Time	15.6		ns
TAHW	Address from IOWB/MEMWB HIGH Hold Time	74.0		ns
TAK	DACK Valid from CLK LOW Delay Time (Note 2)		54.7	ns
	EOPBOUT HIGH from CLK HIGH Delay Time		41.5	ns
	EOPBOUT LOW from CLK HIGH Delay Time		45.5	ns
TASM	Address Stable from CLK HIGH		45.4	ns
TASS	DB to ADSTB LOW Setup Time	58.7		ns
TCH	Clock HIGH Time (Transitions ≤5 ns)	35.0		ns
TCL	Clock LOW Time (Transitions ≤5 ns)	35.0		ns
TCY	CLK Cycle Time	80.0		ns

DMA (MASTER) MODE (Cont'd.)

Symbol	Parameter	Min.	Max.	Units
TDCL	CLK HIGH to IORB LOW Delay		27.2	ns
	CLK HIGH to IOWB LOW Delay		31.5	ns
	CLK HIGH to MEMRB LOW Delay		23.7	ns
	CLK HIGH to MEMWB LOW Delay		30.6	ns
TDCTR	IORB HIGH from CLK HIGH (S4) Delay Time		58.3	ns
	MEMRB HIGH from CLK HIGH (S4) Delay Time		57.9	ns
TDCTW	IOWB HIGH from CLK HIGH (S4) Delay Time		45.6	ns
	MEMWB HIGH from CLK HIGH (S4) Delay Time		46.0	ns
TDQ	HRQ Valid from CLK HIGH Delay Time		40.2	ns
TEPS	EOPBOUT LOW from CLK LOW Setup Time	0		ns
TEPW	EOPBIN Pulse Width	20.0		ns
TFAAB	Address Float to Active Delay from CLK HIGH		60.0	ns
TFAC	IORB/MEMRB or IOWB/MEMWB Active from CLK HIGH		56.0	ns
TFADB	DB Float to Active Delay from CLK HIGH		73.3	ns
THS	HLDA valid to CLK HIGH Setup Time	0		ns
TIDH	Input Data from MEMRB HIGH Hold Time	3.0		ns
TIDS	Input Data to MEMRB HIGH Setup Time	10.0		ns
TODH	Output Data from MEMWB HIGH Hold Time	2.7		ns
TODV	Output Data Valid to MEMWB HIGH	60.2		ns

DMA (MASTER) MODE (Cont'd.)

Symbol	Parameter	Min.	Max.	Units
TQS	DREQ to CLK LOW (SI,S4) Setup Time (Note 2)	0		ns
TRH	CLK to READY LOW Hold Time	11.0		ns
TRS	READY to CLK LOW Setup Time	11.0		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		52.7	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		50.3	ns
TDEL	DBCTL LOW from CLK HIGH Delay Time		63.1	ns
TDEH	DBCTL HIGH from CLK HIGH Delay Time		63.1	ns
TRWEL	RWACTL LOW from CLK HIGH Delay Time		49.8	ns
TRWEH	RWACTL HIGH from CLK HIGH Delay Time		50.8	ns
TWR	End of IOWB/MEMWB to End of IORB/MEMRB in DMA Transfer	0		ns

PERIPHERAL (SLAVE) MODE

Symbol	Parameter	Min.	Max.	Units
TAR	Address Valid or CSB LOW to IORB LOW	0		ns
TAW	Address Valid to IOWB HIGH Setup Time	8.0		ns
TCW	CSB LOW to IOWB HIGH Setup Time	23.0		ns
TDW	Data Valid to IOWB HIGH Setup Time	8.0		ns
TRA	Address or CSB Hold from IORB HIGH	0		ns
TRDE	Data Access from IORB LOW		79.5	ns

PERIPHERAL (SLAVE) MODE (Cont'd.)

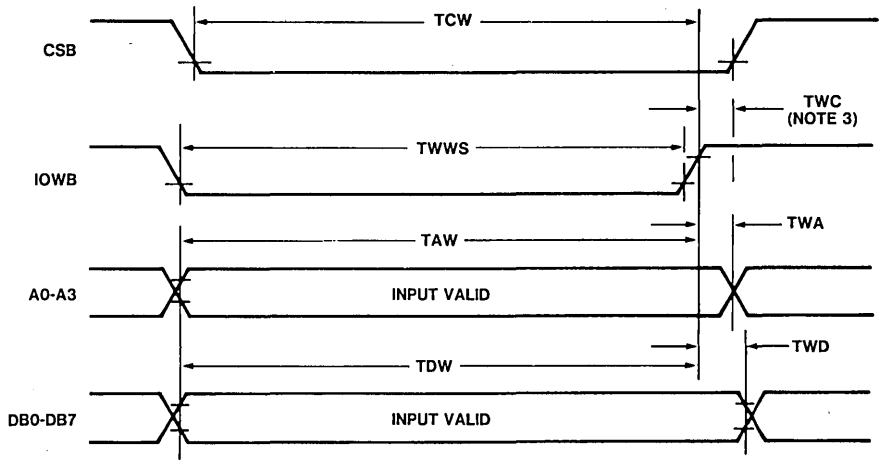
Symbol	Parameter	Min.	Max.	Units
TRDF	DB Float Delay from IORB HIGH	7.2	29.2	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500.0		ns
TRSTS	RESET to First IORB or IOWB	2TCY		ns
TRSTW	RESET Pulse Width (Note 4)	160.0		ns
TRW	IORB Width	75.0		ns
TWA	Address from IOWB HIGH Hold Time	13.0		ns
TWC	CSB HIGH from IOWB HIGH Hold Time	15.0		ns
TWD	Data from IOWB HIGH Hold Time	43.0		ns
TWWS	IOWB Width	30.0		ns
TRDEL	DBCTL LOW from IORB HIGH Delay Time		25.5	ns
TRDEH	DBCTL HIGH from IORB LOW Delay Time		30.1	ns
TCDEL	DBCTL LOW from CSB HIGH Delay Time		37.8	ns

NOTES:

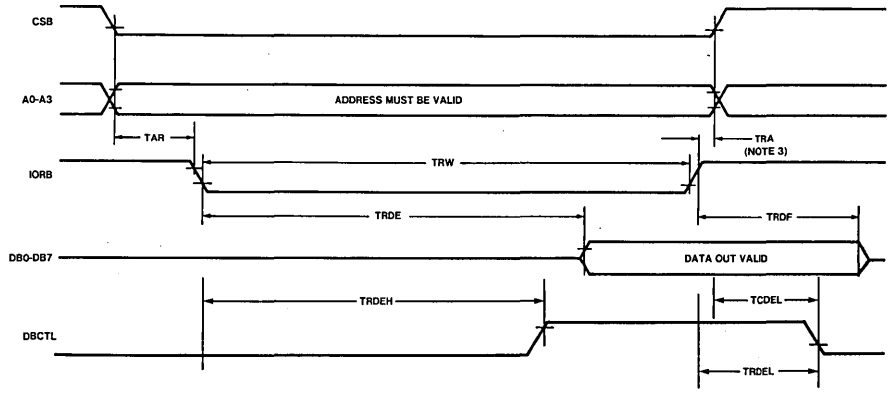
1. DREQ should be held active until DACK is returned.
2. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
3. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 160 ns for the SP8237 as recovery time between active read or write pulses. The same recovery time is needed between an active read or write pulse followed by a DMA transfer.
4. In order to properly reset the SP8237, the clock signal (CLK) should be driven low during reset or should be allowed to run during reset and at least one clock cycle after reset.

Load Dependent Delay

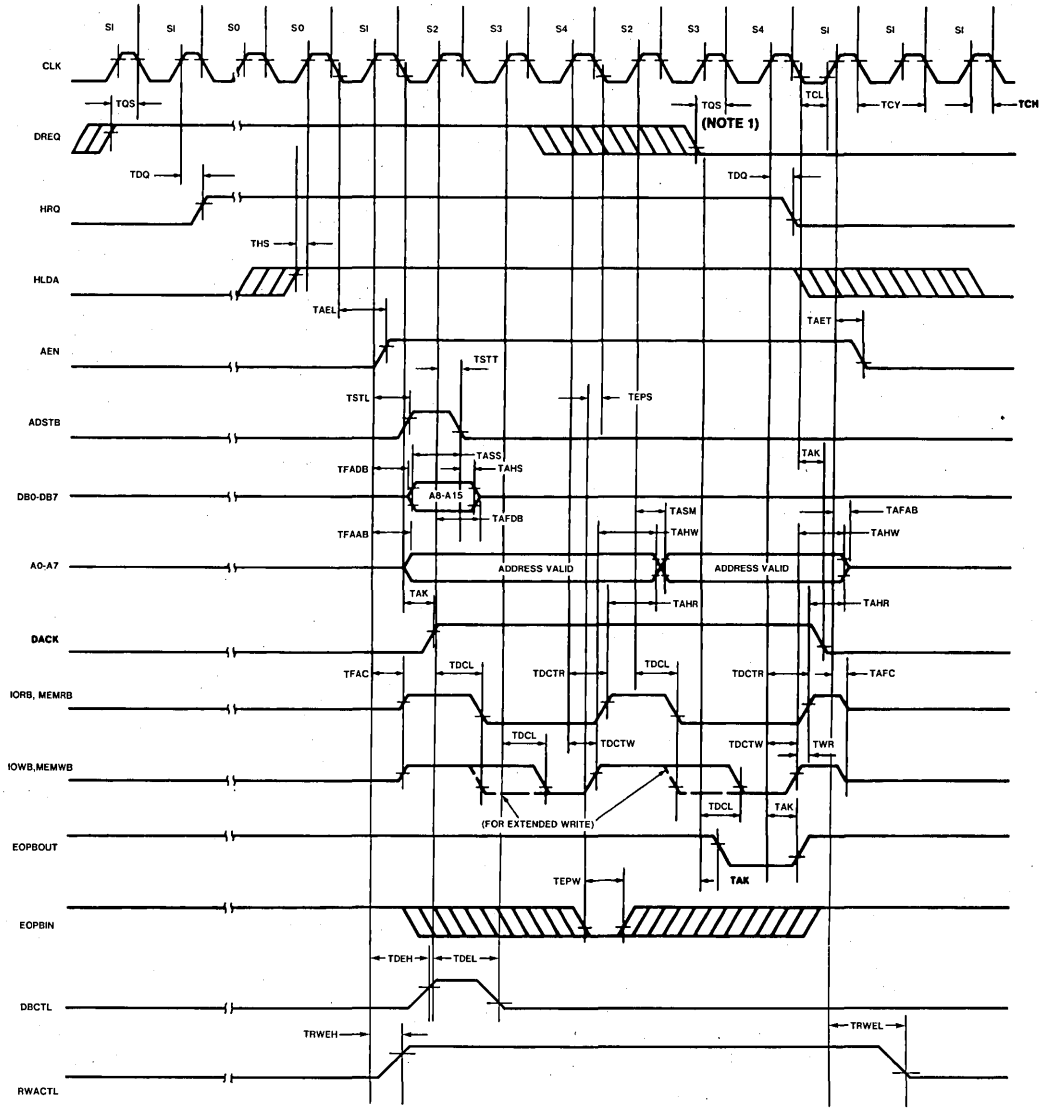
Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
A0-7	0.2	0.4	1.2	0.3	0.4	0.8	ns/pF
ADSTB	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
AEN	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
DACK0-3	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
DB0-7	0.2	0.4	1.2	0.3	0.4	0.8	ns/pF
DBCTL	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
EOPBOUT	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
HRQ	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF
IORB	0.2	0.4	1.2	0.3	0.4	0.8	ns/pF
IOWB	0.2	0.4	1.2	0.3	0.4	0.8	ns/pF
MEMRB	0.2	0.4	1.2	0.3	0.4	0.8	ns/pF
MEMWB	0.2	0.4	1.2	0.3	0.4	0.8	ns/pF
RWACTL	0.3	0.7	2.0	0.5	0.7	1.2	ns/pF



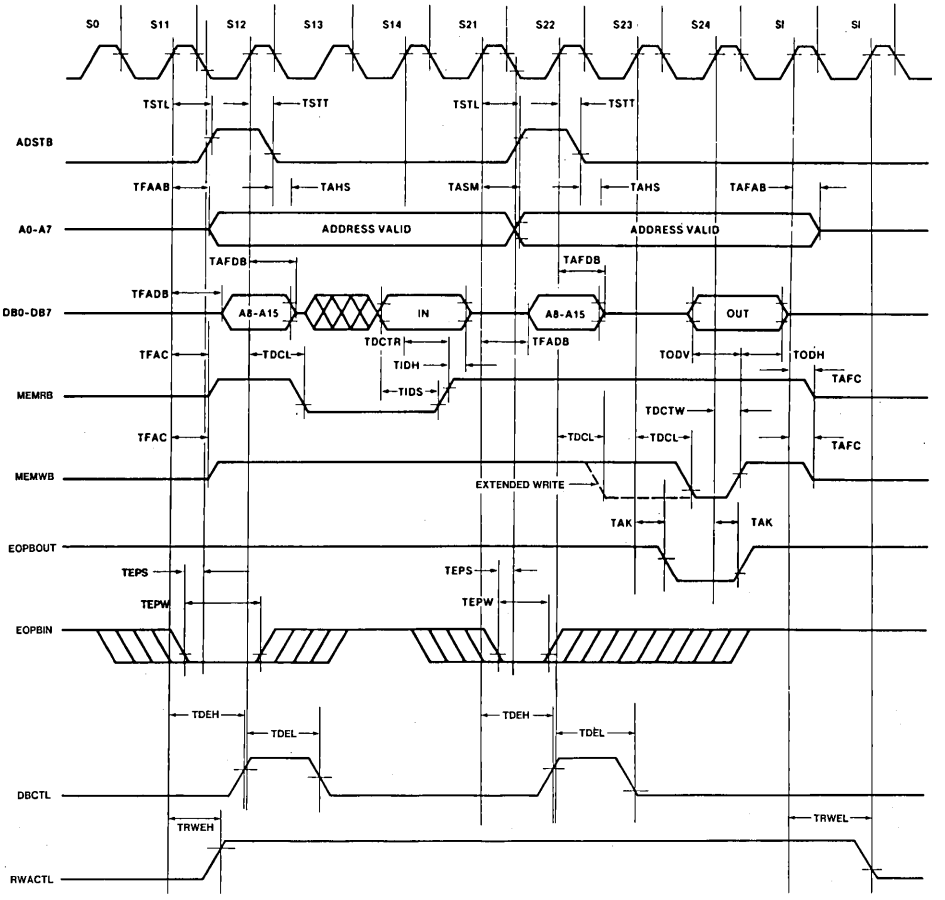
Slave Mode Write Timing G40208



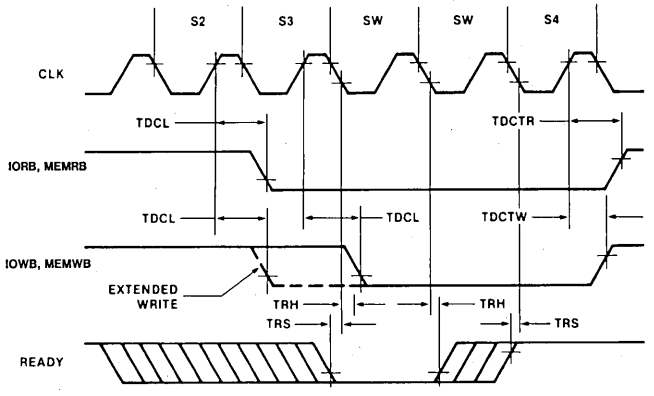
Slave Mode Read Timing G40208



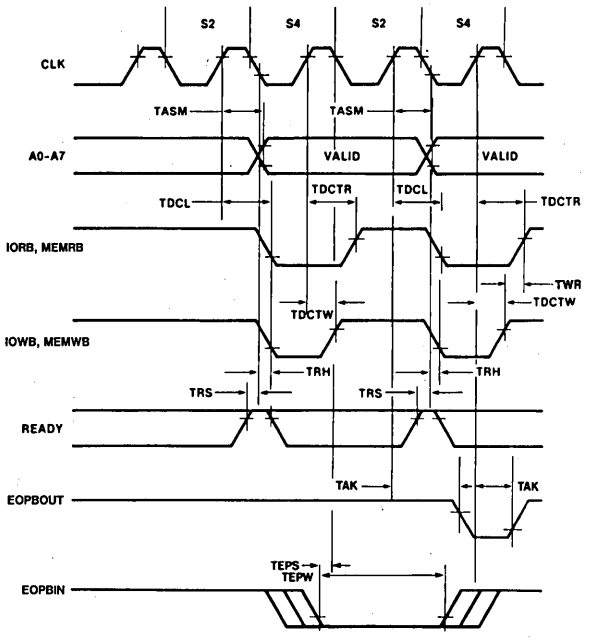
DMA Transfer Timing G40208



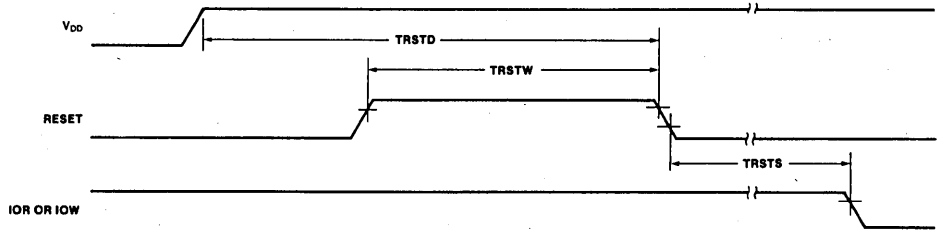
Memory-to-Memory Transfer Timing G40208



Ready Timing G40208

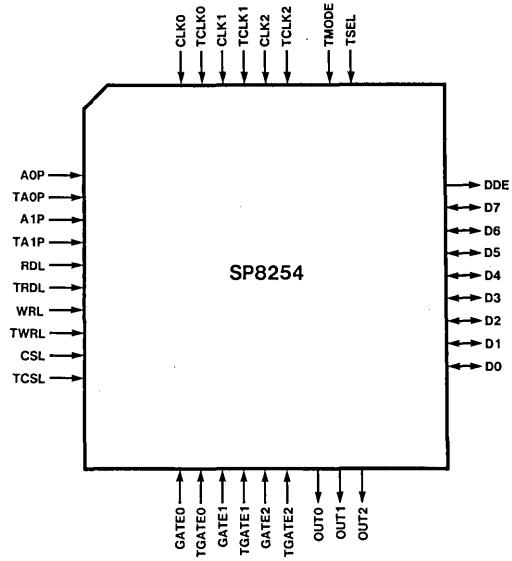


Compressed Transfer Timing G40208



Reset Timing G40208

SP8254 — PROGRAMMABLE INTERVAL TIMER



Functional Pin Diagram G40208

- Cell Version of the 82C54 Programmable Interval Timer; Functional Compatibility with the Standard Product Assured.
- 12.5 MHz Operation.
- Tested and Verified Against Standard Product Test Programs, Providing a Guaranteed 0.1% AQL or Better.
- Handles Inputs from DC to 12.5 MHz.
- Three Independent 16 Bit Counters.
- Six Programmable Counter Modes.
- Binary or BCD Counting.

SP8254 DESCRIPTION

The Intel SP8254 is a high performance, CHMOS cell version of the industry standard 82C54 Programmable Interval Timer designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 12.5 MHz. All modes are software programmable.

Six programmable timer modes allow the SP8254 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications.

The SP8254 can be used in conjunction with the Intel 1.5 Micron CHMOS III Cell Library, allowing the designer to implement a semi-custom integrated circuit that includes the SP8254 and design specific support logic.

For a complete functional description of the 82C54 architecture, refer to the "82C54 CHMOS Programmable Interval Timer" data sheet in the Intel *Microprocessor and Peripheral Handbook.*

Pin Description

Pin Name	Pin Type	Function
D0-7	I/O	DATA: Bidirectional 3-state data bus lines, connected to system data bus through a transceiver.
CLK0 TCLK0	I	CLOCK 0: Clock input of Counter 0.
OUT0	0	OUTPUT 0: Output of Counter 0.
GATE0 TGATE0	I	GATE 0: Gate input of Counter 0.
CLK1 TCLK1	I	CLOCK 1: Clock input of Counter 1.
OUT1	0	OUTPUT 1: Output of Counter 1.
GATE1 TGATE1	I	GATE 1: Gate input of Counter 1.
CLK2 TCLK2	I	CLOCK 2: Clock input of Counter 2.
OUT2	0	OUTPUT 2: Output of Counter 2.
GATE2 TGATE2	I	GATE 2: Gate input of Counter 2.

Pin Description (Cont'd.)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Function</th></tr>
<tr><td>A0P, A1P
TA0P, TA1P</td><td>I</td><td>ADDRESS: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.
<table>
<tr><th>A1P</th><th>A0P</th><th>Selects</th></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td>Counter 0
Counter 1
Counter 2
Control Word Register</td></tr>
</table></td></tr>
<tr><td>CSL
TCSL</td><td>I</td><td>CHIP SELECT: A low on this input enables the SP8254 to respond to RDL and WRL signals. RDL and WRL are ignored otherwise.</td></tr>
<tr><td>RDL
TRDL</td><td>I</td><td>READ CONTROL: This input is low during CPU read operations.</td></tr>
<tr><td>WRL
TWRL</td><td>I</td><td>WRITE CONTROL: This input is low during CPU write operations.</td></tr>
<tr><td>DDE</td><td>0</td><td>DATA DRIVE ENABLE: Used for data bus transceiver control. When this signal is high, D0-7 are being driven by the SP8254.</td></tr>
<tr><td>TMODE,
TSEL</td><td>I</td><td>TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the SP8254 (see table below). The SP8254 can operate in one of three modes: user mode, active test mode, or inactive test mode.
<table>
<tr><th>TMODE</th><th>TSEL</th><th>Function</th></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td>User Mode (Normal operation)
User Mode (Normal operation)
Inactive Test Mode
Active Test Mode</td></tr>
</table></td></tr>
</table>

NOTE: All signals Txxx are test related input signals. All test related signals except for TMODE and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
A0P, A1P	0.3	pF
CLK0	0.3	pF
CLK1	0.3	pF
CLK2	0.3	pF
CSL	0.3	pF
D0-7	0.6	pF
GATE0	0.3	pF
GATE1	0.3	pF
GATE2	0.3	pF
RDL	0.3	pF
TMODE	0.3	pF
TSEL	0.3	pF
WRL	0.3	pF

3-State Output Capacitance

Output Name	Max.	Units
D0-7 (z)	0.6	pF

A.C. Characteristics at 0-70°C, 5V+/−10%

NOTE: A.C. Chracteristics are given to the edge of the SP8254 core. Additional delays will apply in connecting SP8254 signals to package pins through selected I/O buffer cells.

BUS PARAMETERS (NOTE 1)

READ CYCLE

Symbol	Parameter	Min.	Max.	Units
tAR	Address Stable Before RDL ↓	5.0		ns
tSR	CSL Stable Before RDL ↓	0		ns
tRA	Address Hold Time After RDL ↑	0		ns
tRR	RDL Pulse Width	22.0		ns
tRD	Data Delay from RDL ↓		33.0	ns
tDF	RDL ↑ to Data Floating	4.0	19.0	ns
tRV	Command Recovery Time	122.0		ns
tRE	DDE Active After RDL ↓		17.0	ns
tEE	DDE Pulse Width	22.0		ns

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Units
tAW	Address Stable Before WRL ↓	0		ns
tSW	CSL Stable Before WRL ↓	0		ns
tWA	Address Hold Time After WRL ↑	0		ns
tWW	WRL Pulse Width	63.0		ns
tDW	Data Setup Time Before WRL ↑	44.0		ns
tWD	Data Hold Time After WRL ↑	0		ns
tRV	Command Recovery Time	122.0		ns

CLOCK AND GATE

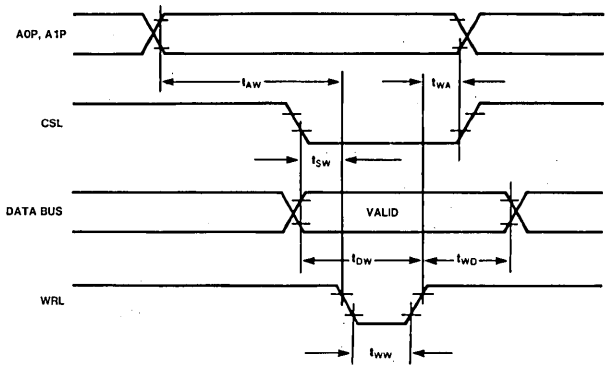
Symbol	Parameter	Min.	Max.	Units
tCLK	Clock Period	80.0		ns
tPWH	Clock High Pulse Width (Note 3)	26.0		ns
tPWL	Clock Low Pulse Width (Note 3)	40.0		ns
tGW	Gate Width High	40.0		ns
tGL	Gate Width Low	40.0		ns
tGS	Gate Setup Time to CLK ↑	8.0		ns
tGH	Gate Hold Time After CLK ↑ (Note 2)	9.0		ns
tOD	Output Delay from CLK ↓		31.0	ns
tODG	Output Delay from Gate ↓		30.0	ns
tWC	CLK Delay for Loading	0	51.0	ns
tWG	Gate Delay for Sampling	1.0	17.0	ns
tWO	OUT Delay from Mode Write		73.0	ns
tCL	CLK Setup for Count Latch	−10.0	5.0	ns

NOTES:

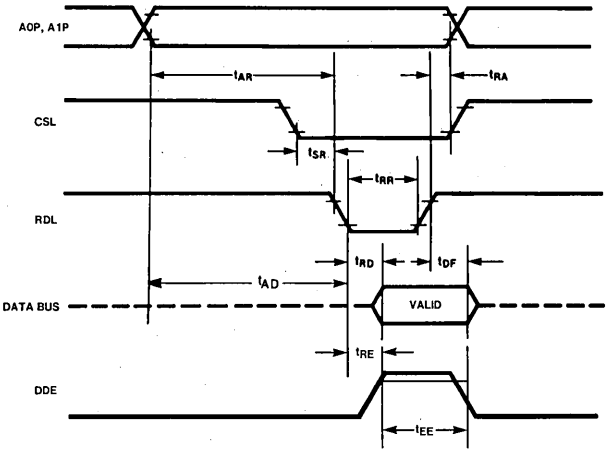
1. A.C. timings measured at Vth (crosspoint threshold voltage) = 2.25V.
2. In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 56 ns of the rising clock edge may not be detected.
3. Low-going glitches that violate tPWH, tPWL may cause errors requiring counter reprogramming.

Load Dependent Delay

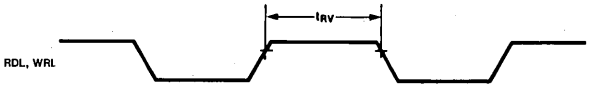
Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
D0-7	0.2	0.3	0.9	0.2	0.3	0.5	ns/pF
DDE	0.3	0.6	1.6	0.5	0.7	1.2	ns/pF
OUT0	0.3	0.6	1.6	0.5	0.7	1.2	ns/pF
OUT1	0.3	0.6	1.6	0.5	0.7	1.2	ns/pF
OUT2	0.3	0.6	1.6	0.5	0.7	1.2	ns/pF



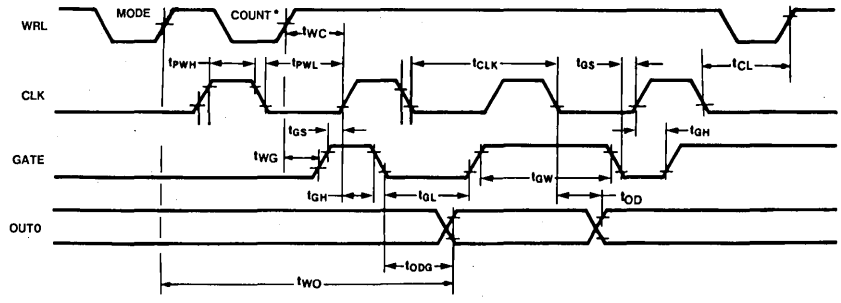
Write G40208



Read G40208



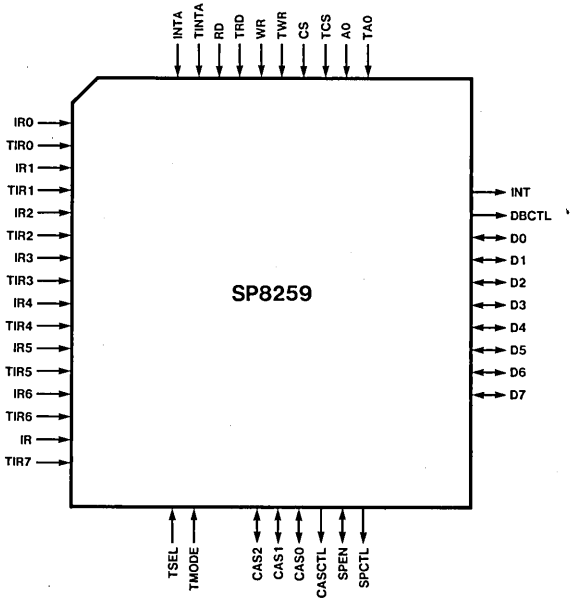
Recovery G40208



* Last byte of count being written

Clock and Gate G40208

SP8259 — PROGRAMMABLE INTERRUPT CONTROLLER



Functional Pin Diagram G40208

- Cell Version of the 82C59A Programmable Interrupt Controller; Functional Compatibility with the Standard Product Assured.
- 12.5 MHz Operation.
- Tested and Verified Against Standard Product Test Programs, Providing a Guaranteed 0.1% AQL or Better.
- Eight-Level Priority Interrupt Controller.
- Expandable to 64 Levels.
- Programmable Interrupt Modes.
- Individual Request Mask Capability.
- Fully Static Design.

SP8259 DESCRIPTION

The Intel SP8259 is a high performance, CHMOS cell version of the industry standard 82C59A Programmable Interrupt Controller. The SP8259 is designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system.

The SP8259 can handle up to 8 vectored priority interrupts for the CPU and is cascadable to 64 without additional circuitry. It is designed to minimize the software and real time overhead in handling multi-level priority interrupts. Two modes of operation make the SP8259 optimal for a variety of system requirements.

The SP8259 can be used in conjunction with the Intel 1.5 Micron CHMOS III Cell Library, allowing the designer to implement a semi-custom integrated circuit that includes the SP8259 and design specific support logic.

For a complete functional description of the 82C59A architecture, refer to the "82C59A-2 CHMOS Programmable Interrupt Controller" data sheet in the Intel *Microprocessor and Peripheral Handbook.*

Pin Description

Pin Name	Pin Type	Function
CS TCS	I	CHIP SELECT: A low on this pin enables RD and WR communication between the CPU and the SP8259. INTA functions are independent of CS.
WR TWR	I	WRITE: A low on this pin when CS is low enables the SP8259 to accept command words from the CPU.
RD TRD	I	READ: A low on this pin when CS is low enables the SP8259 to release status onto the Data Bus for the CPU.
INTA TINTA	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable SP8259 interrupt vector data onto the Data Bus by a sequence of interrupt acknowledge pulses issued by the CPU. INTA is active low.
A0 TA0	I	A0 ADDRESS LINE: This pin acts in conjunction with the CS, WR, and RD pins. It is used by the SP8259 to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 80C86, 80C88).
IR0-7 TIR0-7	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high) and holding it high until it is acknowledged (Edge Triggered Mode), or just by holding a high level on the IR input (Level Triggered Mode).

Pin Description (Cont'd.)

Pin Name	Pin Type	Function
INT	0	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
D0-7	I/O	DATA BUS: Bidirectional 3-state data bus lines, connected to system data bus through a transceiver. Control, status and interrupt vector information is transferred via this bus.
DBCTL	0	DATA BUS CONTROL: Used for data bus transceiver control. When this signal is high, D0-7 are being driven by the SP8259.
CAS0-2	I/O	CASCADE LINES: The CAS lines form a private bus to control a multiple SP8259 structure. These pins are outputs for a Master SP8259 and inputs for a Slave SP8259.
CASCTL	0	CASCADE CONTROL: Used for cascade lines transceiver control. When this signal is high, CAS0-2 are being driven by the SP8259.
SPEN	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. When in the Buffered Mode, it can be used as an output to control buffer transceivers (EN). When not in the Buffered Mode, it is used as an input to designate a Master (SP=1) or a Slave (SP=0).
SPCTL	0	SPEN CONTROL: Used for SPEN transceiver control. When this signal is high, SPEN is being driven by the SP8259.
TMODE, TSEL	I	TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the SP8259 (see table below). The SP8259 can operate in one of three modes: user mode, active test mode, or inactive test mode.

TMODE	TSEL	Function
0	0	User Mode (Normal operation)
0	1	User Mode (Normal operation)
1	0	Inactive Test Mode
1	1	Active Test Mode

NOTE: All signals Txxx are test related input signals. All test related signals except for TMODE and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
A0	0.3	pF
CAS0-2	0.6	pF
CS	0.3	pF
D0-7	0.6	pF
INTA	0.3	pF
IR0-7	0.3	pF
RD	0.3	pF
SPEN	0.6	pF
TMODE	0.3	pF
TSEL	0.3	pF
WR	0.3	pF

3-State Output Capacitance

Output Name	Max.	Units
D0-7 (z)	0.6	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

NOTE: A.C. Characteristics are given to the edge of the SP8259 core. Additional delays will apply in connecting SP8259 signals to package pins through selected I/O buffer cells.

BUS PARAMETERS (NOTE 1)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units
TAHRL	A0/CS Setup to RD/INTA ↓	0		ns
TRHAX	A0/CS Hold after RD/INTA ↑	0		ns
TRLRH	RD/INTA Pulse Width	75.0		ns
TAHWL	A0/CS Setup to WR ↓	0		ns
TWHAX	A0/CS Hold after WR ↑	0		ns

TIMING REQUIREMENTS (Cont'd.)

Symbol	Parameter	Min.	Max.	Units
TWLWH	WR Pulse Width	75.0		ns
TDVWH	Data Setup to WR ↑	40.0		ns
TWHDX	Data Hold after WR ↑	0		ns
TJLJH	Interrupt Request Width (Low)	15.0		ns
TCVIAL	Cascade Setup to Second or Third INTA ↓ (Slave Only)	20.0		ns
TRHRL	End of RD to next RD, End of INTA to next INTA within an INTA sequence only	75.0		ns
TWHWL	End of WR to next WR	75.0		ns
TCHCL	End of Command to Next Command (Not Same Command Type)	75.0		ns

TIMING RESPONSES

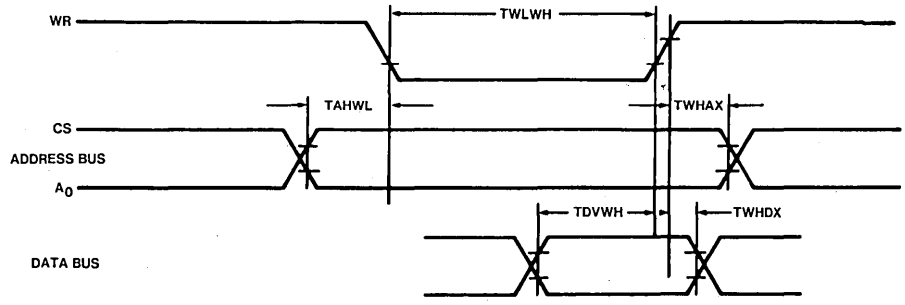
Symbol	Parameter	Min.	Max.	Units
TRLDV	Data Valid from RD/INTA ↓		75.0	ns
TRHDZ	Data Float after RD/INTA ↑	10.0	40.0	ns
TJHIH	Interrupt Output Delay		40.0	ns
TIALCV	Cascade Valid from First INTA ↓ (Master Only)		40.0	ns
TRLEL	Enable Active from RD/INTA ↓		50.0	ns
TRHEH	Enable Inactive from RD/INTA ↑		30.0	ns

NOTES:

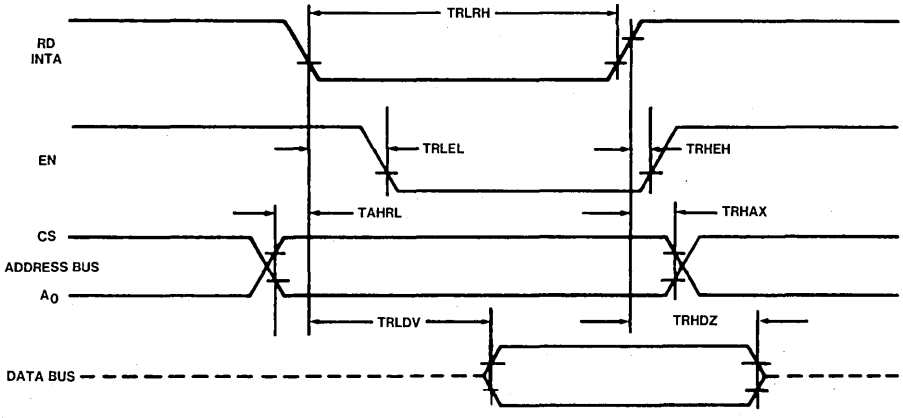
1. A.C. timings measured at Vth (crosspoint threshold voltage) = 2.25V.

Load Dependent Delay

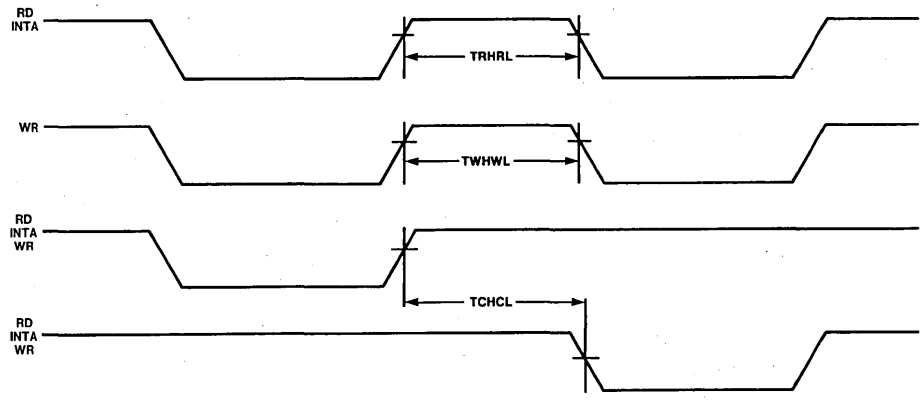
Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
CAS0-2	0.2	0.3	0.9	0.2	0.3	0.5	ns/pF
CASCTL	0.3	0.6	1.6	0.5	0.7	1.2	ns/pF
D0-7	0.2	0.3	0.9	0.2	0.3	0.5	ns/pF
DBCTL	0.3	0.6	1.6	0.5	0.7	1.2	ns/pF
INT	0.3	0.6	1.6	0.5	0.7	1.2	ns/pF
SPCTL	0.3	0.6	1.6	0.5	0.7	1.2	ns/pF
SPEN	0.2	0.3	0.9	0.2	0.3	0.5	ns/pF



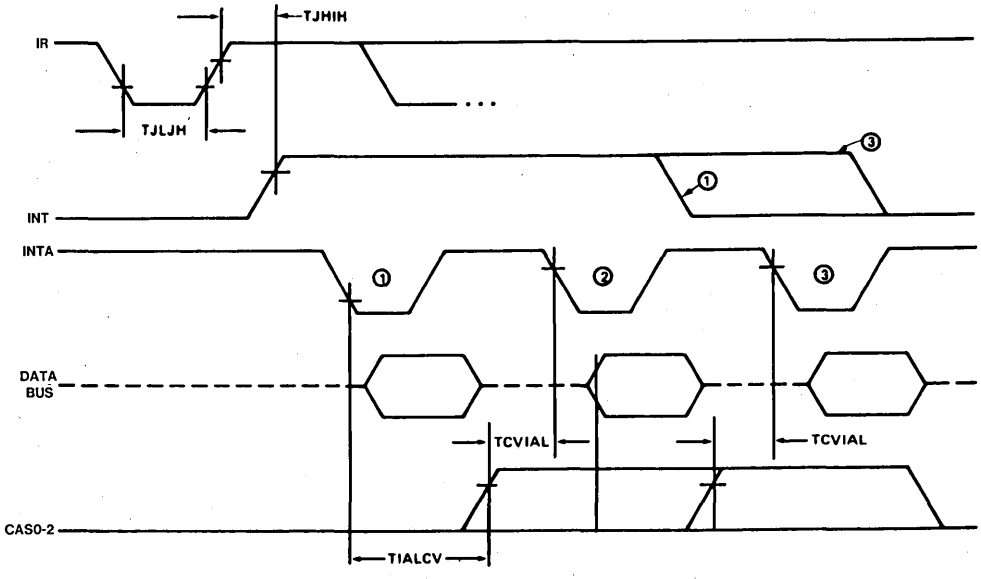
Write G40208



Read/INTA G40208

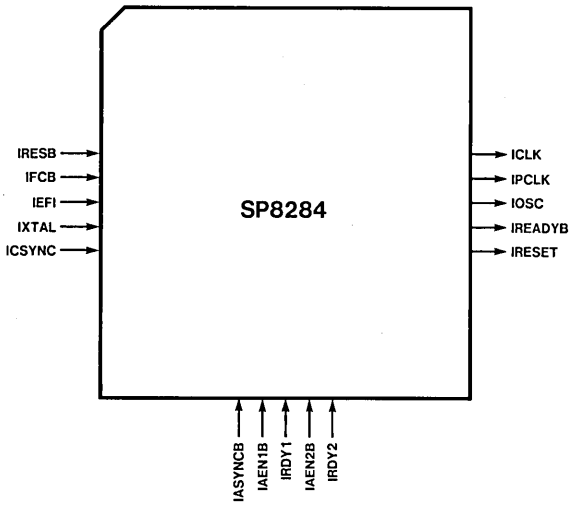


Other Timing G40208



INTA Sequence G40208

SP8284 — 8086/8088 CLOCK GENERATOR AND DRIVER



Functional Pin Diagram G40208

- Cell Version of the 82C84A 8086/8088 Clock Generator and Driver; Functional Compatibility with the Standard Product Assured.
- 12.5 MHz Operation.
- Tested and Verified Against Standard Product Test Programs, Providing a Guaranteed 0.1% AQL or Better.
- Generates the System Clock for the 8086 and 8088 Microprocessor Families.
- Uses a Crystal or an External Frequency Source.
- Provides Local READY Synchronization.
- Generates System Reset Output.
- Capable of Clock Synchronization with other SP8284 Cells.

SP8284 DESCRIPTION

The Intel SP8284 is a high performance, CHMOS cell version of the industry standard 82C84A Clock Generator and Driver designed to service the requirements of the 80C86/88 and 8086/88. The chip contains a divide-by-three counter and complete READY synchronization and reset logic. A specially designed oscillator cell (POSC2) used in conjunction with the SP8284 provides for operation from an external crystal. An external frequency source may also be used.

The SP8284 can be used in conjunction with the Intel 1.5 Micron CHMOS III Cell Library, allowing the designer to implement a semi-custom integrated circuit that includes the SP8284 and design specific support logic.

For a complete functional description of the 82C84A architecture, refer to the "82C84A/82C84A-5 CHMOS Clock Generator and Driver for 80C86, 80C88 Processors" data sheet in the Intel *Microprocessor and Peripheral Handbook.*

Pin Description

Pin Name	Pin Type	Function
ICLK	O	PROCESSOR CLOCK: ICLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. ICLK has an output frequency which is one third of the IXTAL or IEFI input frequency and one third duty cycle.
IFCB	I	FREQUENCY/CRYSTAL SELECT: When LOW, IFCB permits the processor's clock to be generated from the IXTAL input. When IFCB is HIGH, ICLK is generated from the IEFI input.
IEFI	I	EXTERNAL FREQUENCY: When IFCB is high, ICLK is generated from the frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired ICLK output.
IXTAL	I	EXTERNAL CRYSTAL IN: IXTAL is the pin to which the output of the SP8284 oscillator companion cell POSC2 is attached. The crystal frequency is 3 times the desired processor clock frequency.
IPCLK	O	PERIPHERAL CLOCK: IPCLK is a peripheral clock signal whose output frequency is one-half that of ICLK and has a 50% duty cycle.
IOSC	O	OSCILLATOR OUTPUT: IOSC is the oscillator output equal in frequency to that of IXTAL.

Pin Description (Cont'd.)

Pin Name	Pin Type	Function
IAEN1B IAEN2B	I	ADDRESS ENABLES: Active LOW signals which qualify their respective Bus Ready Signals (IRDY1, IRDY2). Two IAEN signals are useful in system configurations which permit the processor to access two Multi-Master system busses. In non Multi-Master configurations the IAEN signals are tied true (low).
IRDY1 IRDY2	I	BUS READY (Transfer Complete): IRDY is an active HIGH signal which is an indication from a device located on the system data bus that the data has been received, or is available. IRDY1 and IRDY2 are qualified by IAEN1 and IAEN2 respectively.
IASYNCB	I	READY SYNCHRONIZATION SELECT: IASYNCB is an input which defines the synchronization mode of the READY logic. When IASYNCB is LOW, two stages of READY synchronization are provided. When IASYNCB is HIGH, a single stage of ready synchronization is provided.
IREADYB	0	READY: IREADYB is an active LOW signal which is the synchronized IRDY input signal. IREADYB is cleared after the guaranteed hold time to the processor has been met.
ICSYNC	I	CLOCK SYNCHRONIZATION: ICSYNC is an active HIGH signal which allows multiple SP8284s to be synchronized to provide clocks that are in phase. When ICSYNC is HIGH the internal counters are reset. When ICSYNC goes LOW the internal counters are allowed to resume counting. ICSYNC needs to be externally synchronized to IEFI. When using the crystal oscillator ICSYNC should be connected to ground.
IRESB	I	RESET IN: IRESB is an active LOW signal which is used to generate IRESET.
IRESET	0	RESET: IRESET is an active HIGH signal which is used to reset the processor. Its timing characteristics are determined by IRESB.

Input Capacitance

Input Name	Max.	Units
IAEN1B, IAEN2B	0.05	pF
IASYNCB	0.05	pF
ICSYNC	0.19	pF
IEFI	0.05	pF
IFCB	0.10	pF
IRDY1, IRDY2	0.10	pF
IRESB	0.06	pF
IXTAL	0.10	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

NOTE: A.C. Characteristics are given to the edge of the SP8284 core. Additional delays will apply in connecting SP8284 signals to package pins through selected I/O buffer cells.

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units
tEHEL	External Frequency HIGH Time	13.0		ns
tELEH	External Frequency LOW Time	13.0		ns
tELEL	IEFI/IXTAL Period	26.0		ns
tR1VCL	IRDY1/IRDY2 Active/Inactive Setup to ICLK	12.0		ns
tR1VCH	IRDY1/IRDY2 Active Setup to ICLK	5.0		ns
tCLR1X	IRDY1/IRDY2 Hold to ICLK	− 6.0		ns
tAYVCL	IASYNCB Setup to ICLK	12.0		ns
tCLAYX	IASYNCB Hold to ICLK	− 6.0		ns
tA1VR1V	IAEN1B/IAEN2B Setup to IRDY1/IRDY2	1.0		ns
tCLA1X	IAEN1B/IAEN2B Hold to ICLK	− 6.0		ns

TIMING REQUIREMENTS (Cont'd.)

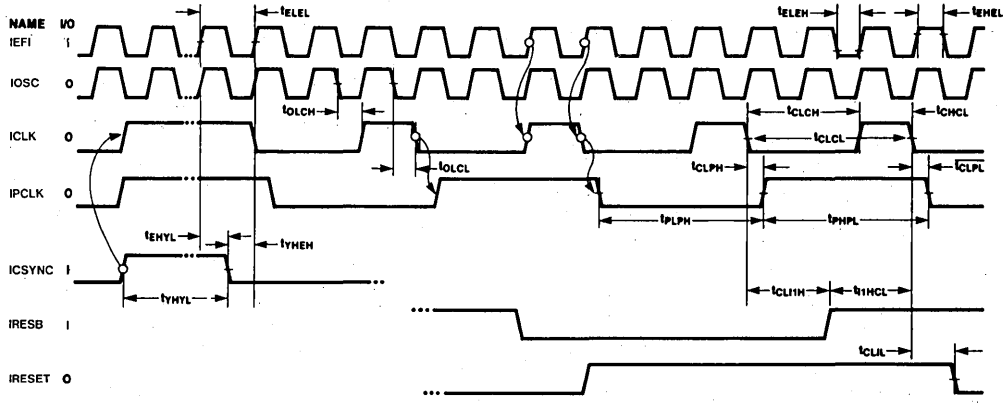
Symbol	Parameter	Min.	Max.	Units
tYHEH	ICSYNC Setup to IEFI	4.0		ns
tEHYL	ICSYNC Hold to IEFI	6.0		ns
tYHYL	ICSYNC Width	9.0		ns
tI1HCL	IRESB Setup to ICLK	4.0		ns
tCLI1H	IRESB Hold to ICLK	2.0		ns

TIMING RESPONSES

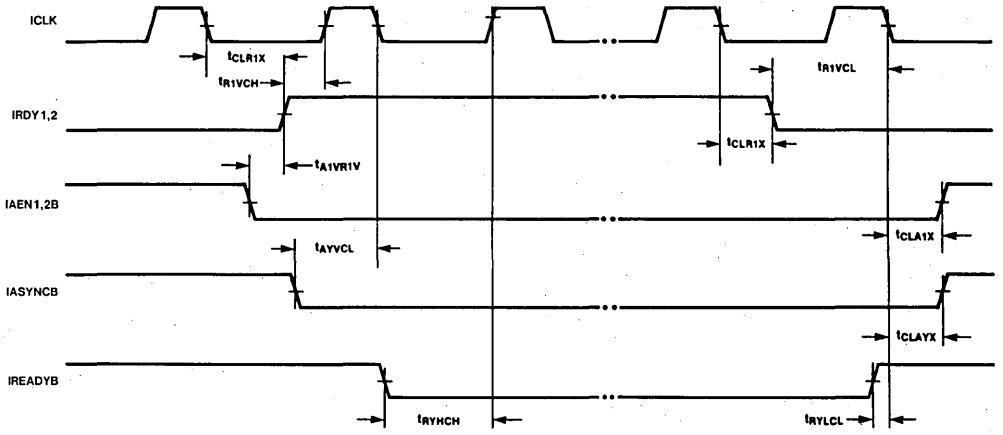
Symbol	Parameter	Min.	Max.	Units
tCLCL	ICLK Cycle Period	80.0		ns
tCHCL	ICLK HIGH Time	(⅓ tCLCL) +5.8		ns
tCLCH	ICLK LOW Time	(⅔ tCLCL) −7.1		ns
tPHPL	IPCLK HIGH Time	tCLCL −0.1		ns
tPLPH	IPCLK LOW Time	tCLCL +0.1		ns
tRYLCL	IREADYB Inactive to ICLK	3.5		ns
tRYHCH	IREADYB Active to ICLK	(⅔ tCLCL) −13.4		ns
tCLIL	ICLK to IRESET Delay		8.5	ns
tCLPH	ICLK to IPCLK HIGH Delay		12.7	ns
tCLPL	ICLK to IPCLK LOW Delay		12.6	ns
tOLCH	IOSC to ICLK HIGH Delay	−3.0	9.2	ns
tOLCL	IOSC to ICLK LOW Delay	−8.8	16.3	ns

Load Dependent Delay

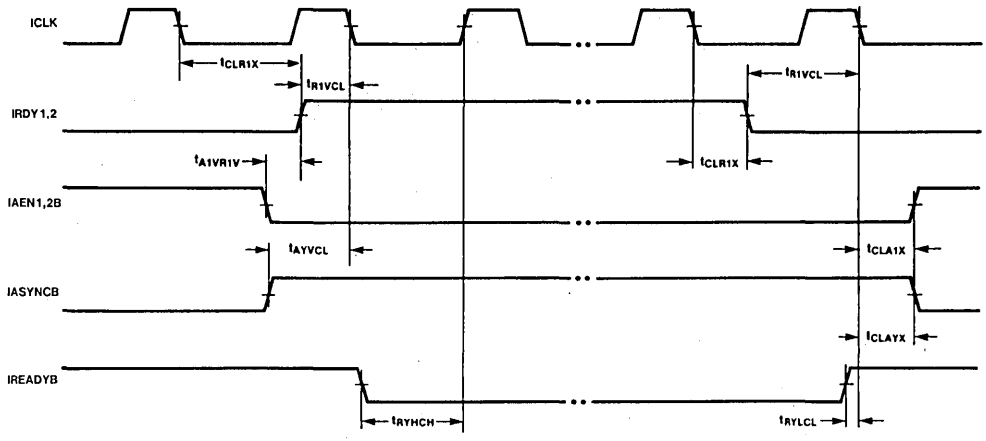
Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
ICLK	0.25	0.57	1.53	0.45	0.67	1.19	ns/pF
IOSC	0.33	0.74	1.96	0.46	0.67	1.19	ns/pF
IPCLK	0.33	0.73	1.96	0.46	0.67	1.19	ns/pF
IREADYB	0.08	0.16	0.42	0.13	0.20	0.38	ns/pF
IRESET	0.32	0.73	1.95	0.45	0.67	1.17	ns/pF



Clocks and Reset Signals G40208

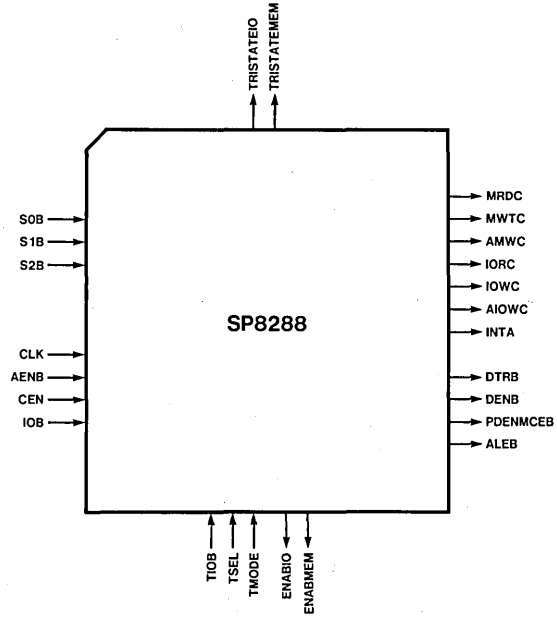


Ready Signals (for Asynchronous Devices) G40208



Ready Signals (for Synchronous Devices) G40208

SP8288 — 8086/8088 BUS CONTROLLER



Functional Pin Diagram G40208

- Cell Version of the 82C88 8086/8088 Bus Controller; Functional Compatibility with the Standard Product Assured.
- 12.5 MHz Operation.
- Tested and Verified Against Standard Product Test Programs, Providing a Guaranteed 0.1% AQL or Better.
- Provides Support for 8086/88, 80186/188 Microprocessor Families.
- Provides Advanced Commands for Multi-Master Busses.
- 3-State Command Output Drivers.
- Configurable for Use with an I/O Bus.

SP8288 DESCRIPTION

The Intel SP8288 is a high performance, CHMOS cell version of the industry standard 82C88 Bus Controller. The SP8288 provides command and control timing generation for 8086/88, 80186/188 architecture systems. Specially designed SP8288 high drive output buffer companion cells eliminate the need for additional bus drivers when used in conjunction with the SP8288.

The SP8288 can be used in conjunction with the Intel 1.5 Micron CHMOS III Cell Library, allowing the designer to implement a semi-custom integrated circuit that includes the SP8288 and design specific support logic.

For a complete functional description of the 82C88 architecture, refer to the "82C88 CHMOS Bus Controller" data sheet in the Intel *Microprocessor and Peripheral Handbook.*

Pin Description

Pin Name	Pin Type	Function
S0B S1B S2B	I	STATUS INPUT PINS: These pins are the status input pins from the processor. The SP8288 decodes these inputs to generate command and control signals at the appropriate time. When these pins are not in use (passive) they are all HIGH.
CLK	I	CLOCK: This is a clock signal from the SP8284 clock generator and serves to establish when command and control signals are generated.
ALEB	0	ADDRESS LATCH ENABLE: This signal serves to strobe an address into the address latches. This signal is active LOW and latching occurs on the rising (LOW to HIGH) transition.
DENB	0	DATA ENABLE: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active LOW.
DTRB	0	DATA TRANSMIT/RECEIVE: This signal establishes the direction of data flow through the transceivers. A LOW on this line indicates Transmit (write to I/O or memory) and a HIGH indicates Receive (Read).
AENB	I	ADDRESS ENABLE: AENB enables command outputs of the SP8288 at least 145 ns after it becomes active (LOW) via the ENABIO and ENABMEM signals. AENB going inactive immediately 3-states the command output drivers via the TRISTATEIO (I/O Bus Mode) and TRISTATEMEM signals.

Pin Description (Cont'd.)

Pin Name	Pin Type	Function
CEN	I	COMMAND ENABLE: When this signal is LOW all SP8288 command outputs and the DENB and PDENMCEB control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled. The command outputs are controlled by the ENABIO and ENABMEM signals.
IOB TIOB	I	INPUT/OUTPUT BUS MODE: When IOB is HIGH the SP8288 functions in the I/O Bus mode. When LOW, the SP8288 functions in the System Bus mode.
AIOWC	0	ADVANCED I/O WRITE COMMAND: This command line issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. AIOWC is active HIGH.
IOWC	0	I/O WRITE COMMAND: This command line instructs an I/O device to read the data on the data bus. IOWC is active HIGH.
IORC	0	I/O READ COMMAND: This command line instructs an I/O device to drive its data onto the data bus. IORC is active HIGH.
AMWC	0	ADVANCED MEMORY WRITE COMMAND: This command line issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. AMWC is active HIGH.
MWTC	0	MEMORY WRITE COMMAND: This command line instructs the memory to record the data present on the data bus. MWTC is active HIGH.
MRDC	0	MEMORY READ COMMAND: This command line instructs the memory to drive its data onto the data bus. MRDC is active HIGH.
INTA	0	INTERRUPT ACKNOWLEDGE: This signal tells an interrupting device that its interrupt has been acknowledged and that it should drive the vectoring information onto the data bus. INTA is active HIGH.
PDENMCEB	0	This is a dual function pin. MCEB (IOB LOW): MASTER CASCADE ENABLE, occurs during an interrupt sequence and serves to read a Cascade Address from a master PIC (Priority Interrupt Controller) onto the data bus. MCEB is active LOW. PDEN (IOB HIGH): PERIPHERAL DATA ENABLE, enables the data bus transceiver for the I/O bus that DENB performs for the system bus. PDEN is active HIGH.

Pin Description (Cont'd.)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Function</th></tr>
<tr><td>TRISTATEIO</td><td>0</td><td>3-STATE I/O: This signal is used as a 3-state control signal for the I/O command signals (INTA, IORC, AIOWC, IOWC). TRISTATEIO is active HIGH.</td></tr>
<tr><td>TRISTATEMEM</td><td>0</td><td>3-STATE MEMORY: This signal is used as a 3-state control signal for the memory command signals (MRDC, AMWC, MWTC). TRISTATEMEM is active HIGH.</td></tr>
<tr><td>ENABIO</td><td>0</td><td>ENABLE I/O: This signal is used as an enable control signal for the I/O command signals (INTA, IORC, AIOWC, IOWC). ENABIO is active HIGH.</td></tr>
<tr><td>ENABMEM</td><td>0</td><td>ENABLE MEMORY: This signal is used as an enable control signal for the memory command signals (MRDC, AMWC MWTC). ENABMEM is active HIGH.</td></tr>
<tr><td>TMODE,
TSEL</td><td>I</td><td>TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the SP8288 (see table below). The SP8288 can operate in one of three modes: user mode, active test mode, or inactive test mode.
<table>
<tr><th>TMODE</th><th>TSEL</th><th>Function</th></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td>User Mode (Normal operation)
User Mode (Normal operation)
Inactive Test Mode
Active Test Mode</td></tr>
</table>
</td></tr>
</table>

NOTE: All signals Txxx are test related input signals. All test related signals except for TMODE and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
AENB	0.41	pF
CEN	0.30	pF
CLK	2.41	pF
IOB	0.06	pF
S0B, S1B, S2B	0.33	pF
TMODE	0.19	pF
TSEL	0.08	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

NOTE: A.C. Characteristics are given to the edge of the SP8288 core. Additional delays will apply in connecting SP8288 signals to package pins through selected I/O buffer cells.

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units
fc	CLK Frequency		12.5	MHz
TCLCL	CLK Cycle Period	80.0		ns
TCLCH	CLK Low Time	46.0		ns
TCHCL	CLK High Time	26.0		ns
TSVCH	Status Active Setup Time	7.2	14.8	ns
TCHSV	Status Inactive Hold Time	0	0	ns
TSHCL	Status Inactive Setup Time	2.8	9.5	ns
TCLSH	Status Active Hold Time	−8.8	−1.2	ns

TIMING RESPONSES

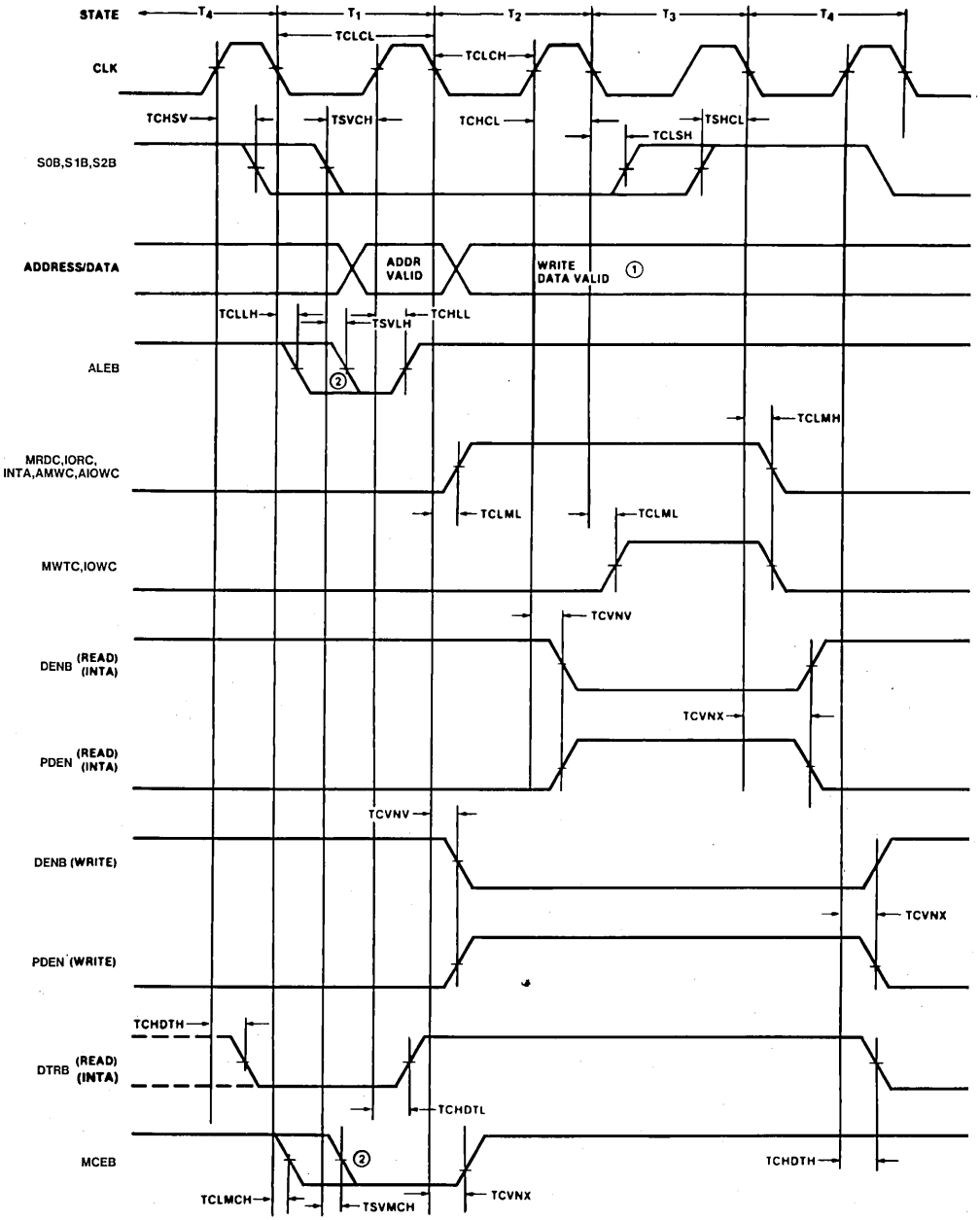
Symbol	Parameter	Min.	Max.	Units
TCVNV	Control Active Delay — DENB Read	2.1	8.7	ns
	Control Active Delay — DENB Write	2.3	9.8	ns
	Control Active Delay — PDEN Read	1.6	6.6	ns
	Control Active Delay — PDEN Write	1.9	7.6	ns
TCVNX	Control Inactive Delay — DENB Read	2.4	8.1	ns
	Control Inactive Delay — DENB Write	2.4	7.6	ns
	Control Inactive Delay — PDEN Read	2.4	9.2	ns
	Control Inactive Delay — PDEN Write	2.4	8.7	ns
	Control Inactive Delay — MCEB	1.1	5.4	ns
TCLLH	ALEB Active Delay (from CLK)	0.7	3.8	ns
TCLMCH	MCEB Active Delay (from CLK)	1.3	5.5	ns
TSVLH	ALEB Active Delay (from Status)	0.7	3.8	ns
TSVMCH	MCEB Active Delay (from Status)	1.5	6.6	ns
TCHLL	ALEB Inactive Delay	1.2	3.7	ns
TCLML	Command Active Delay	1.0	3.9	ns
TCLMH	Command Inactive Delay	1.4	5.7	ns
TCHDTL	Direction Control Active Delay	1.4	4.7	ns
TCHDTH	Direction Control Inactive Delay	0.9	3.3	ns
TAELCH	Command Enable Time (Memory)	0.5	1.5	ns
	Command Enable Time (I/O)	0.8	3.5	ns
TAEHCZ	Command Disable Time (Memory)	0.6	1.3	ns
	Command Disable Time (I/O)	0.9	2.5	ns
TAELCV	Enable Delay Time (Memory)	148.0	175.0	ns
	Enable Delay Time (I/O)	148.0	176.0	ns
TAEVNV	AENB to DENB	0.6	3.2	ns

TIMING RESPONSES (Cont'd.)

Symbol	Parameter	Min.	Max.	Units
TCEVNV	CEN to DENB	1.1	4.2	ns
	CEN to PDEN	0.7	2.6	ns
TCELRH	CEN to Command Enable Active (Memory)	0.9	2.5	ns
	CEN to Command Enable Active (I/O)	1.2	3.2	ns
TCELRL	CEN to Command Enable Inactive (Memory)	0.8	3.5	ns
	CEN to Command Enable Inactive (I/O)	0.8	3.9	ns

Load Dependent Delay

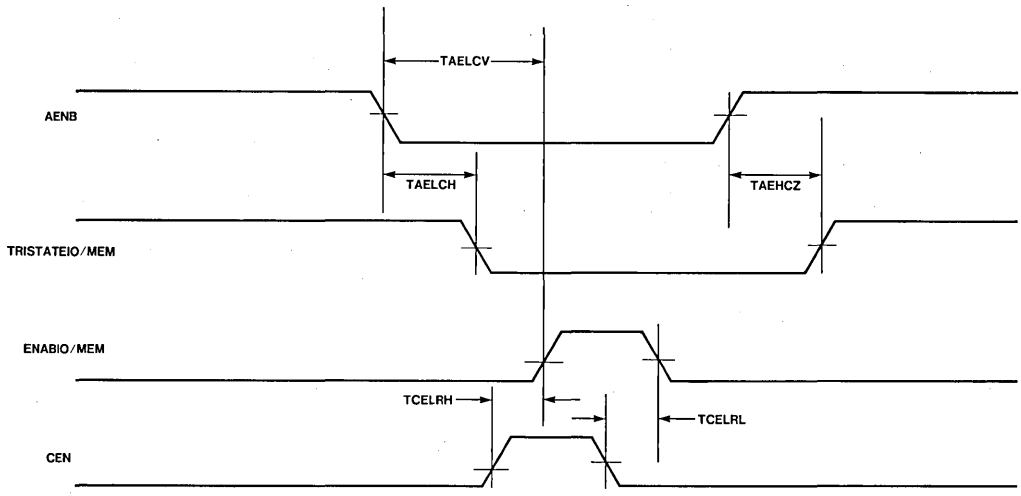
Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
AIOWC	0.37	0.82	2.20	0.42	0.72	1.38	ns/pF
ALEB	0.32	0.78	2.03	0.65	0.82	1.54	ns/pF
AMWC	0.37	0.82	2.20	0.42	0.72	1.38	ns/pF
DENB	0.32	0.78	2.03	0.65	0.82	1.54	ns/pF
DTRB	0.32	0.78	2.03	0.65	0.82	1.54	ns/pF
ENABIO	0.08	0.19	0.51	0.14	0.22	0.38	ns/pF
ENABMEM	0.08	0.19	0.51	0.14	0.22	0.38	ns/pF
INTA	0.37	0.82	2.20	0.42	0.72	1.38	ns/pF
IORC	0.37	0.82	2.20	0.42	0.72	1.38	ns/pF
IOWC	0.37	0.82	2.20	0.42	0.72	1.38	ns/pF
MRDC	0.37	0.82	2.20	0.42	0.72	1.38	ns/pF
MWTC	0.37	0.82	2.20	0.42	0.72	1.38	ns/pF
PDENMCEB	0.75	1.64	4.41	0.84	1.44	2.76	ns/pF
TRISTATEIO	0.08	0.19	0.51	0.14	0.22	0.38	ns/pF
TRISTATEMEM	0.08	0.19	0.51	0.14	0.22	0.38	ns/pF



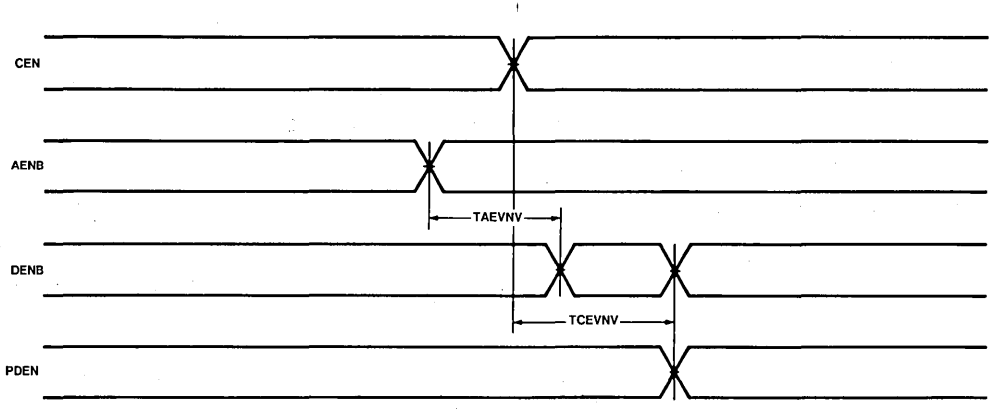
NOTES:
1. Address/Data Bus is shown only for reference purposes.
2. Leading edge of ALEB and MCEB is determined by the falling edge of CLK or Status going active, whichever occurs last.

G40208

ADDRESS ENABLE (AENB) TIMING (3-STATE ENABLE/DISABLE).

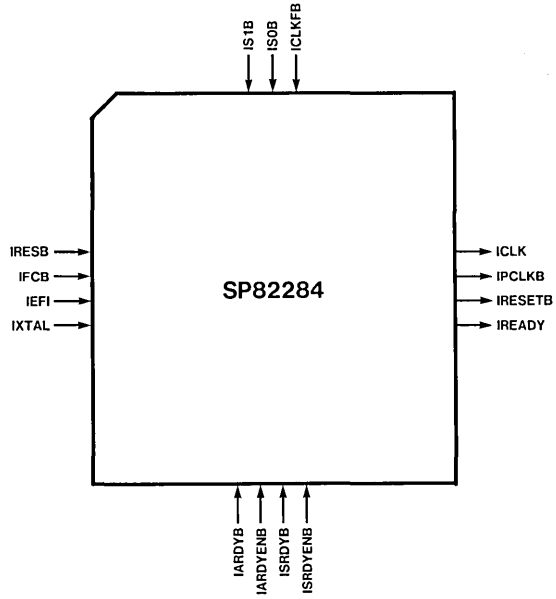


DENB, PDEN Qualification Timing G40208



Address Enable (AENB) Timing (3-State Enable/Disable) G40208

SP82284 — 80286 CLOCK GENERATOR AND READY INTERFACE



Functional Pin Diagram G40208

- Cell Version of the 82C284 80286 Clock Generator and Ready Interface; Functional Compatibility with the Standard Product Assured.
- 12.5 MHz Operation.
- Tested and Verified Against Standard Product Test Programs, Providing a Guaranteed 0.1% AQL or Better.
- Generates System Clock for 80286 Family Microprocessors.
- Uses a Crystal or an External Frequency Source.
- Provides Local READY Synchronization.
- Generates System Reset Output.

SP82284 DESCRIPTION

The Intel SP82284 is a high performance, CHMOS cell version of the industry standard 82C84 80286 Clock Generator and Ready Interface. The SP82284 is a clock generator/driver which provides clock signals for 80286 family microprocessors and support components. It also contains logic to supply READY to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input. A specially designed oscillator cell (POSC2) used in conjunction with the SP82284 provides for operation from an external crystal. An external frequency source may also be used.

The SP82284 can be used in conjunction with the Intel 1.5 Micron CHMOS III Cell Library, allowing the designer to implement a semi-custom integrated circuit that includes the SP82284 and design specific support logic.

For a complete functional description of the 82C284 architecture, refer to the "82C284 Clock Generator and Ready Interface for 80286 Processors" data sheet in the Intel *Microprocessor and Peripheral Handbook.*

Pin Description

Pin Name	Pin Type	Function
ICLK	O	SYSTEM CLOCK: The clock signal used by the processor and support devices which must be synchronous with the processor. The frequency of the ICLK output is twice the desired internal processor clock frequency.
ICLKFB	I	INTERNAL CLOCK: ICLKFB is the ICLK signal used internal to the SP82284. This signal is equivalent to the off-chip system clock (ICLK) and must be connected to the output of the ICLK SP82284 I/O buffer companion cell (PCNO4). This signal is filtered in the SP82284 to eliminate any noise or ringing which may be present on the clock output.
IFCB	I	FREQUENCY/CRYSTAL SELECT: Selects the source for the ICLK output. When IFCB is low, the IXTAL input drives ICLK. When IFCB is HIGH, the EFI input drives the ICLK output.
IEFI	I	EXTERNAL FREQUENCY IN: Drives ICLK when IFCB is HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
IXTAL	I	EXTERNAL CRYSTAL IN: IXTAL is the pin to which the output of the SP82284 oscillator companion cell POSC2 is attached. The crystal frequency must be twice the desired internal processor clock frequency.
IPCLKB	O	PERIPHERAL CLOCK: An output which provides a 50% duty cycle clock with one-half the frequency of ICLKFB. IPCLKB will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.

Pin Description (Cont'd.)

Pin Name	Pin Type	Function
IARDYENB	I	ASYNCHRONOUS READY ENABLE: An active LOW input which qualifies the IARDYB input. IARDYENB selects IARDYB as the source of ready for the current bus cycle. Inputs to IARDYENB may be applied asynchronously to ICLKFB. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
IARDYB	I	ASYNCHRONOUS READY: An active LOW input used to terminate the current bus cycle. The IARDYB input is qualified by IARDYENB. Inputs to IARDYB may be applied asynchronously to ICLKFB. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
ISRDYENB	I	SYNCHRONOUS READY ENABLE: An active LOW input which qualifies ISRDYB. ISRDYENB selects ISRDYB as the source for IREADY to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
ISRDYB	I	SYNCHRONOUS READY: An active LOW input used to terminate the current bus cycle. The ISRDYB input is qualified by the ISRDYENB input. Setup and hold times must be satisfied for proper operation.
IREADY	0	READY: An active HIGH output which signals the current bus cycle is to be completed. The ISRDY, ISRDYENB, IARDYB, IARDYENB, IS0B, IS1B, and IRESB inputs control IREADY.
IS0B IS1B	I	STATUS: Inputs which prepare the SP82284 for a subsequent bus cycle. IS0B and IS1B synchronize IPCLK to the internal processor clock and control IREADY. Setup and hold times must be satisfied for proper operation.
IRESETB	0	RESET: An active LOW output which is derived from the IRESB input. IRESETB is used to force the system into an initial state. When IRESETB is active, IREADY will be active (HIGH).
IRESB	I	RESET IN: An active LOW input which generates the system reset signal, IRESETB. Signals to IRESB may be applied asynchronously to ICLKFB. Setup and hold times are given to assure a guaranteed response to synchronous inputs.

Input Capacitance

Input Name	Max.	Units
IARDYB	0.08	pF
IARDYENB	0.08	pF
ICLKFB	1.03	pF
IEFI	0.15	pF
IFCB	0.15	pF
IRESB	0.05	pF
IS0B, IS1B	0.06	pF
ISRDYB	0.08	pF
ISRDYENB	0.08	pF
IXTAL	0.12	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

NOTE: A.C. Characteristics are given to the edge of the SP82284 core. Additional delays will apply in connecting SP82284 signals to package pins through selected I/O buffer cells.

TIMING PARAMETERS

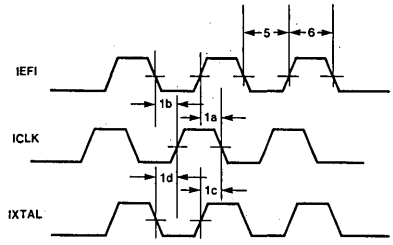
Symbol	Parameter	Min.	Max.	Units
1a	IEFI HIGH to ICLK LOW	0.6	1.5	ns
1b	IEFI LOW to ICLK HIGH	0.2	0.9	ns
1c	IXTAL HIGH to ICLK LOW	4.4	8.3	ns
1d	IXTAL LOW to ICLK HIGH	0.8	4.0	ns
4	ICLKFB Period	31.0		ns
5	ICLKFB LOW Time	10.0		ns
6	ICLKFB HIGH Time	10.0		ns
9	Status Setup Time	6.0		ns
10	Status Hold Time	1.0		ns

TIMING PARAMETERS (Cont'd.)

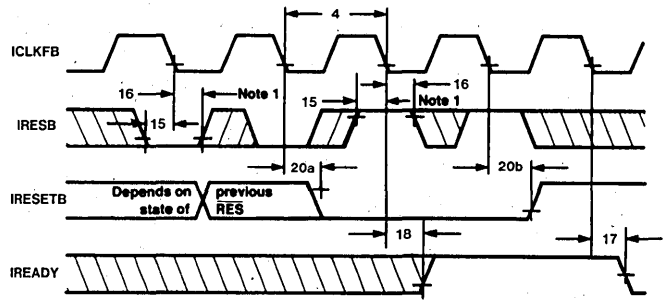
Symbol	Parameter	Min.	Max.	Units
11a	ISRDYB or ISRDYENB Active Setup Time	7.0		ns
11b	ISRDYB or ISRDYENB Inactive Setup Time	10.0		ns
12	ISRDYB or ISRDYENB Hold Time	1.0		ns
13	IARDYB or IARDYENB Setup Time	1.0		ns
14	IARDYB or IARDYENB Hold Time	11.0		ns
15	IRESB Setup Time	0		ns
16	IRESB Hold Time	7.0		ns
17	IREADY Inactive Delay	6.4	16.4	ns
18	IREADY Active Delay	2.6	10.0	ns
19a	IPCLKB Delay LOW	2.3	7.8	ns
19b	IPCLKB Delay HIGH	2.4	9.5	ns
20a	IRESETB Delay LOW	7.2	11.3	ns
20b	IRESETB Delay HIGH	7.6	11.5	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
ICLK	0.31	0.71	1.92	0.52	0.82	1.54	ns/pF
IPCLKB	0.08	0.13	0.31	0.10	0.13	0.21	ns/pF
IREADY	0.08	0.16	0.42	0.10	0.11	0.19	ns/pF
IRESETB	0.09	0.15	0.39	0.12	0.16	0.26	ns/pF

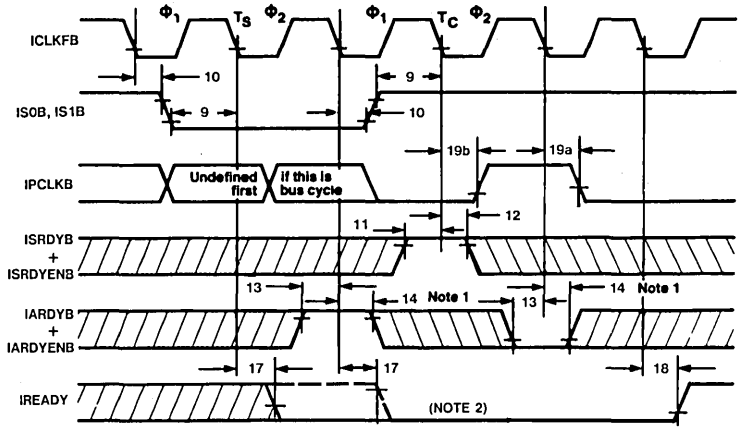


ICLK as a Function of IEFI and IXTAL G40208



NOTE:
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

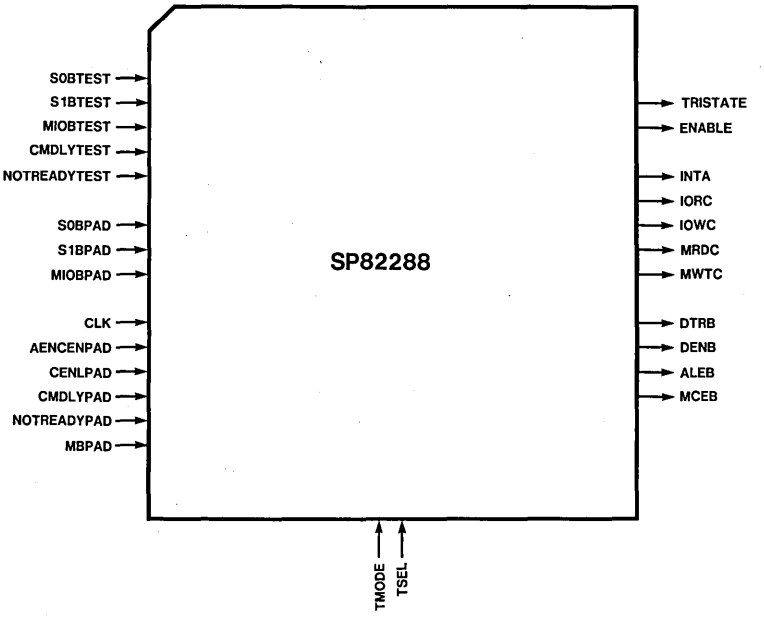
IRESETB and IREADY Timing as a Function of IRESB with IS0B, IS1B, IARDYB + IARDYENB, and ISRDYB + ISRDYENB High G40208



NOTES:
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. If ISRDYB + ISRDYENB or IARDYB + IARDYENB are active before and/or during the first bus cycle after IRESETB. IREADY may not be deasserted until after the falling edge of 02 of Ts.

IREADY and IPCLKB Timing with IRESB High G40208

SP82288 — 80286 BUS CONTROLLER



Functional Pin Diagram G40208

- Cell Version of the 82288 80286 Bus Controller; Functional Compatibility with the Standard Product Assured.
- 12.5 MHz Operation.
- Tested and Verified Against Standard Product Test Programs, Providing a Guaranteed 0.1% AQL or Better.
- Provides Support for 80286 Family Microprocessors.
- Provides Commands and Control for Local and System Buses.
- Offers Wide Flexibility in System Configurations.
- Flexible Command Timing.
- Optional MULTIBUS Compatible Timing.

SP82288 DESCRIPTION

The Intel SP82288 is a high performance, CHMOS cell version of the industry standard 82288 80286 Bus Controller designed for use in 80286 microsystems. The SP82288 provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals.

The SP82288 can be used in conjunction with the Intel 1.5 Micron CHMOS III Cell Library, allowing the designer to implement a semi-custom integrated circuit that includes the SP82288 and design specific support logic.

For a complete functional description of the 82288 architecture, refer to the "82288 Bus Controller for 80286 Processors" data sheet in the Intel *Microprocessor and Peripheral Handbook.*

Pin Description

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th colspan="4">Function</th></tr>
<tr><td>CLK</td><td>I</td><td colspan="4">SYSTEM CLOCK: This signal provides the basic timing control for the SP82288 in an 80286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and command and control outputs change.</td></tr>
<tr><td rowspan="11">S0BPAD,
S1BPAD,
S0BTEST,
S1BTEST</td><td rowspan="11">I</td><td colspan="4">BUS CYCLE STATUS: These signals start a bus cycle and, along with MIOBPAD, defines the type of bus cycle. These inputs are active LOW. A bus cycle is started when either S0BPAD or S1BPAD is sampled LOW at the falling edge CLK. Setup and hold times must be met for proper operation.</td></tr>
<tr><td colspan="4">80286 Bus Cycle Status Definition</td></tr>
<tr><td>MIOBPAD</td><td>S1BPAD</td><td>S0BPAD</td><td>Type of Bus Cycle</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>I/O Read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O Write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>None; Idle</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Halt or Shutdown</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Memory Read</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory Write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None; Idle</td></tr>
<tr><td>MIOBPAD
MIOBTEST</td><td>I</td><td colspan="4">MEMORY OR I/O SELECT: This signal determines whether the current bus cycle is in the memory or I/O space. When LOW, the current bus cycle is in the I/O space. Setup and hold times must be met for proper operation.</td></tr>
</table>

Pin Description (Cont'd.)

Pin Name	Pin Type	Function
MBPAD	I	MULTIBUS MODE SELECT: This signal determines timing of the command and control outputs. When HIGH, the bus controller operates with MULTIBUS compatible timings. When LOW, the bus controller optimizes the control and command output timing for short bus cycles. The function of the AENCENPAD input is selected by this signal.
CENLPAD	I	COMMAND ENABLED LATCHED: This is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENLPAD is an active HIGH input latched internally at the end of each TS cycle. CENLPAD is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be tied HIGH to select this SP82288 for all transfers. No control inputs affect CENLPAD. Setup and hold times must be met for proper operation.
CMDLYPAD, CMDLYTEST	I	COMMAND DELAY: This signal allows delaying the start of a command. CMDLYPAD is an active HIGH input. If sampled HIGH, the command output is not activated and CMDLYPAD is again sampled at the next clock cycle. When sampled LOW the selected command is enabled. If NOTREADYPAD is detected LOW before the command output is activated, the SP82288 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be tied LOW if no delays are required before starting a command. This input has no effect on SP82288 control outputs.
NOTREADYPAD NOTREADYTEST	I	READY: Indicates the end of the current bus cycle. NOTREADYPAD is an active LOW input. MULTIBUS mode requires at least one wait state to allow the command outputs to become active. NOTREADYPAD must be LOW during reset, to force the SP82288 into the idle state. Setup and hold times must be met for proper operation.
AENCENPAD	I	COMMAND ENABLE/ADDRESS ENABLE: This signal controls the command and DENB outputs of the bus controller. AENCENPAD inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. When MBPAD is HIGH this pin has the AENB function. AENB is an active LOW input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit 3-state OFF and become inactive. AENB HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into 3-state OFF and DENB inactive (LOW). AENB would normally be controlled by an 82289 bus arbiter which activates AENB when that arbiter owns the bus to which the bus controller is attached. When MBPAD is LOW this pin has the CEN function. CEN is an unlatched active HIGH input which allows the bus controller to activate its command and DENB outputs. With MBPAD LOW, CEN LOW forces the command and DENB outputs inactive.

Pin Description (Cont'd.)

Pin Name	Pin Type	Function
ALEB	0	ADDRESS LATCH ENABLE: This signal controls the address latches used to hold an address stable during a bus cycle. This output is active LOW. ALEB will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MCEB	0	MASTER CASCADE ENABLE: This signals that a cascade address from a master SP8259 interrupt controller may be placed onto the CPU address bus for latching by the address latches ALEB control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active LOW. MCEB is only active during interrupt acknowledge cycles and is not affected by any control input.
DENB	0	DATA ENABLE: This signal controls when data transceivers connected to the local data bus should be enabled. DENB is an active LOW control output. DENB is delayed for write cycles in the MULTIBUS mode.
DTRB	0	DATA TRANSMIT/RECEIVE: This signal establishes the direction of data flow to or from the local data bus. When LOW, this control output indicates that a write bus cycle is being performed. A HIGH indicates a read bus cycle. DENB is always inactive when DTRB changes state. DTRB is not affected by any of the control inputs.
IOWC	0	I/O WRITE COMMAND: This signal instructs an I/O device to read the data on the data bus. IOWC is an active HIGH command output. The MBPAD and CMDLYPAD inputs control when this output becomes active. NOTREADYPAD controls when it becomes inactive.
IORC	0	I/O READ COMMAND: This signal instructs an I/O device to place data onto the data bus. IORC is an active HIGH command output. The MBPAD and CMDLYPAD inputs control when this output becomes active. NOTREADYPAD controls when it becomes inactive.
MWTC	0	MEMORY WRITE COMMAND: This signal instructs a memory device to read the data on the data bus. MWTC is an active HIGH command output. The MBPAD and CMDLYPAD inputs control when this output becomes active. NOTREADYPAD controls when it becomes inactive.

Pin Description (Cont'd.)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Function</th></tr>
<tr><td>MRDC</td><td>0</td><td>MEMORY READ COMMAND: This signal instructs a memory device to place data onto the data bus. MRDC is an active HIGH command output. The MBPAD and CMDLYPAD inputs control when this output becomes active. NOTREADYPAD controls when it becomes inactive.</td></tr>
<tr><td>INTA</td><td>0</td><td>INTERRUPT ACKNOWLEDGE: This signal tells an interrupting device that its interrupt request is being acknowledged. INTA is an active HIGH command output. The MBPAD and CMDLYPAD inputs control when this output becomes active. NOTREADYPAD controls when it becomes inactive.</td></tr>
<tr><td>ENABLE</td><td>0</td><td>ENABLE: This signal is used to enable the command output signals. ENABLE is active HIGH.</td></tr>
<tr><td>TRISTATE</td><td>0</td><td>TRISTATE: This signal is used to 3-state the command output signals. TRISTATE is active HIGH (when active, command outputs enter a 3-state OFF state).</td></tr>
<tr><td>TMODE, TSEL</td><td>I</td><td>TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the SP82288 (see table below). The SP82288 can operate in one of three modes: user mode, active test mode, or inactive test mode.
<table>
<tr><th>TMODE</th><th>TSEL</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>User Mode (Normal operation)</td></tr>
<tr><td>0</td><td>1</td><td>User Mode (Normal operation)</td></tr>
<tr><td>1</td><td>0</td><td>Inactive Test Mode</td></tr>
<tr><td>1</td><td>1</td><td>Active Test Mode</td></tr>
</table></td></tr>
</table>

NOTE: All signals xxxTEST and Txxx are test related input signals. All test related signals except for TMODE and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
AENCENPAD	0.18	pF
CENLPAD	0.22	pF
CLK	2.42	pF
CMDLYPAD	0.11	pF
MBPAD	0.49	pF
MIOBPAD	0.11	pF
NOTREADYPAD	0.11	pF
S0BPAD, S1BPAD	0.11	pF
TMODE	0.14	pF
TSEL	0.08	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

NOTE: A.C. Characteristics are given to the edge of the SP82288 core. Additional delays will apply in connecting SP82288 signals to package pins through selected I/O buffer cells.

Symbol	Parameter	Min.	Max.	Units
1	CLK Period	50.0		ns
2	CLK HIGH Time	16.0		ns
3	CLK LOW Time	12.0		ns
6	MIOBPAD and Status Setup Time	9.0		ns
7	MIOBPAD and Status Hold Time	0		ns
8	CENLPAD Setup Time	15.0		ns
9	CENLPAD Hold Time	1.0		ns
10	NOTREADYPAD Setup Time	15.0		ns
11	NOTREADYPAD Hold Time	0		ns
12	CMDLYPAD Setup Time	15.0		ns
13	CMDLYPAD Hold Time	0		ns

A.C. Characteristics at 0–70°C, 5V+/−10% (Cont'd.)

Symbol	Parameter	Min.	Max.	Units
14	AENB Setup Time	10.0		ns
15	AENB Hold Time	1.0		ns
16	ALEB, MCEB Active Delay from CLK	0.9	4.4	ns
17	ALEB, MCEB Inactive Delay from CLK	0.6	3.7	ns
18	DENB (Write) Inactive from CENLPAD	2.8	10.5	ns
19	DTRB LOW from CLK	1.8	8.1	ns
20	DENB (Read) Active Delay from DTRB (Note 1)	1.0	6.2	ns
21	DENB (Read) Inactive Delay from CLK	2.8	10.5	ns
22	DTRB HIGH from DENB Inactive (Note 1)	1.5	6.6	ns
23	DENB (Write) Active Delay from CLK	2.3	9.7	ns
24	DENB (Write) Inactive Delay from CLK	2.8	10.5	ns
25	DENB Inactive from CEN	2.1	6.7	ns
26	DENB Active from CEN	1.7	7.3	ns
27	DTRB HIGH from CLK (when CEN = LOW)	1.9	7.4	ns
28	DENB Active from AENB	2.1	6.7	ns
29	Command Output Active Delay from CLK	0.6	3.7	ns
30	Command Output Inactive Delay from CLK	0.9	4.4	ns
31	ENABLE LOW from CEN	0.8	3.7	ns
32	ENABLE HIGH from CEN	1.5	4.3	ns
33	TRISTATE LOW from AENB	0.8	4.1	ns

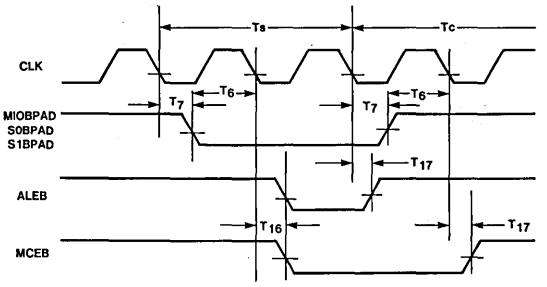
A.C. Characteristics at 0–70°C, 5V+/−10% (Cont'd.)

Symbol	Parameter	Min.	Max.	Units
34	TRISTATE HIGH from AENB	1.7	4.7	ns
35	MBPAD Setup Time	13.0		ns
36	MBPAD Hold Time	1.0		ns
37	TRISTATE LOW from MBPAD ↓	0.8	4.1	ns
38	TRISTATE HIGH from MBPAD ↑	1.7	4.7	ns
39	DENB Inactive from MBPAD ↑	2.1	6.7	ns
40	DEN Active from MBPAD ↑	1.7	7.3	ns

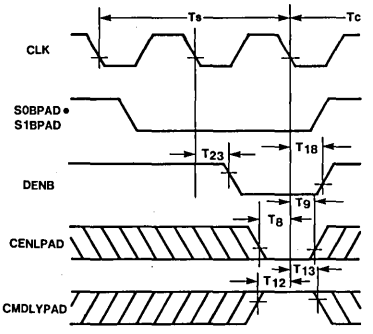
NOTES:
1. This specification does not conform to the corresponding standard product specification for overlap between DTRB and DENB. This may, depending on the system design, cause bus contention.

Load Dependent Delay

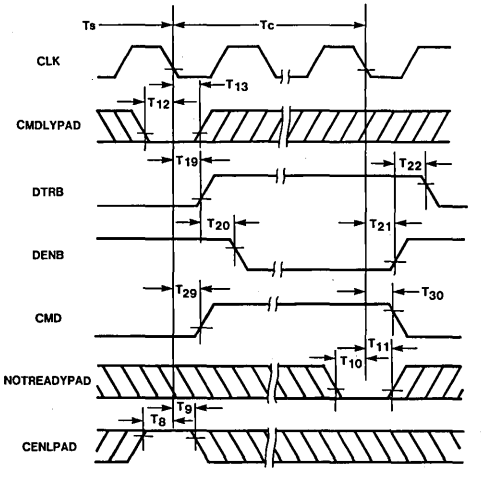
Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
ALEB	0.39	0.73	2.02	0.51	0.86	1.54	ns/pF
DENB	0.32	0.78	2.03	0.65	0.82	1.54	ns/pF
DTRB	0.32	0.78	2.03	0.65	0.82	1.54	ns/pF
ENABLE	0.08	0.19	0.51	0.14	0.22	0.38	ns/pF
INTA	0.39	0.73	2.02	0.51	0.86	1.54	ns/pF
IORC	0.39	0.73	2.02	0.51	0.86	1.54	ns/pF
IOWC	0.39	0.73	2.02	0.51	0.86	1.54	ns/pF
MCEB	0.39	0.73	2.02	0.51	0.86	1.54	ns/pF
MRDC	0.39	0.73	2.02	0.51	0.86	1.54	ns/pF
MWTC	0.39	0.73	2.02	0.51	0.86	1.54	ns/pF
TRISTATE	0.08	0.19	0.51	0.14	0.22	0.38	ns/pF



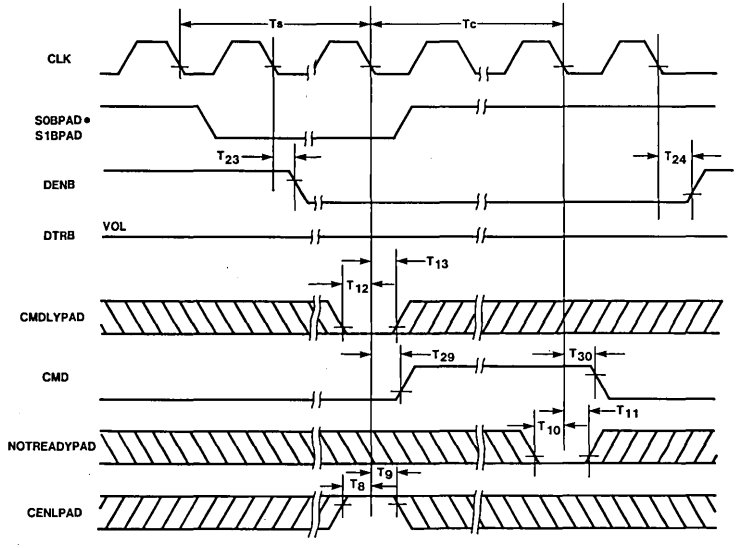
STATUS, ALEB, MCEB Characteristics G40208



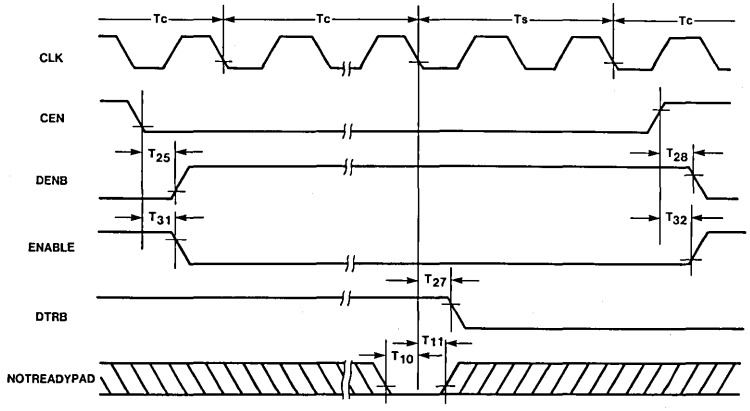
CENLPAD, CMDLYPAD, DENB Characteristics with MBPAD = 0 and CEN = 1 during Write Cycle G40208



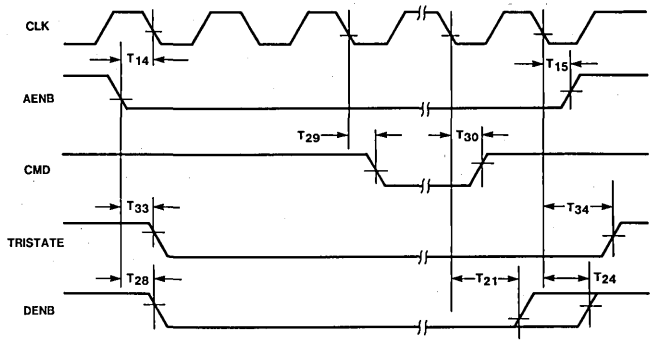
Read Cycle Characteristics with MBPAD = 0 and CEN = 1 G40208



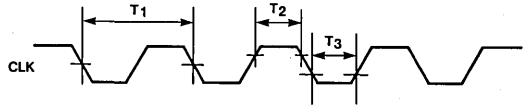
Write Cycle Characteristics with MBPAD = 0 and CEN = 1 G40208



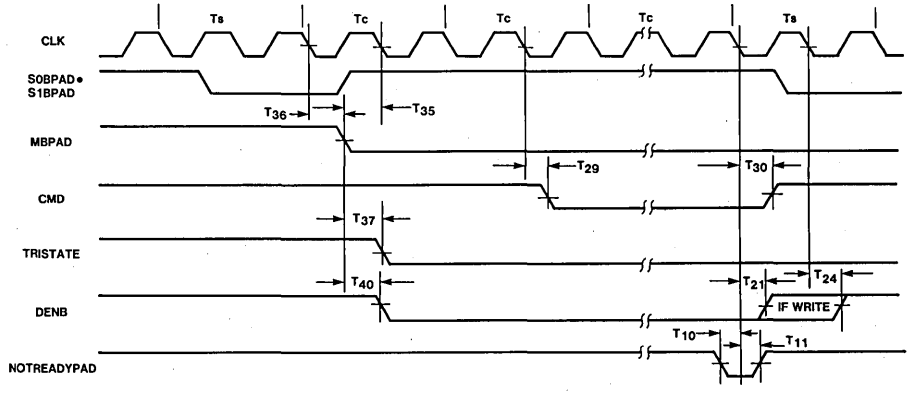
CEN Characteristics with MBPAD = 0 G40208



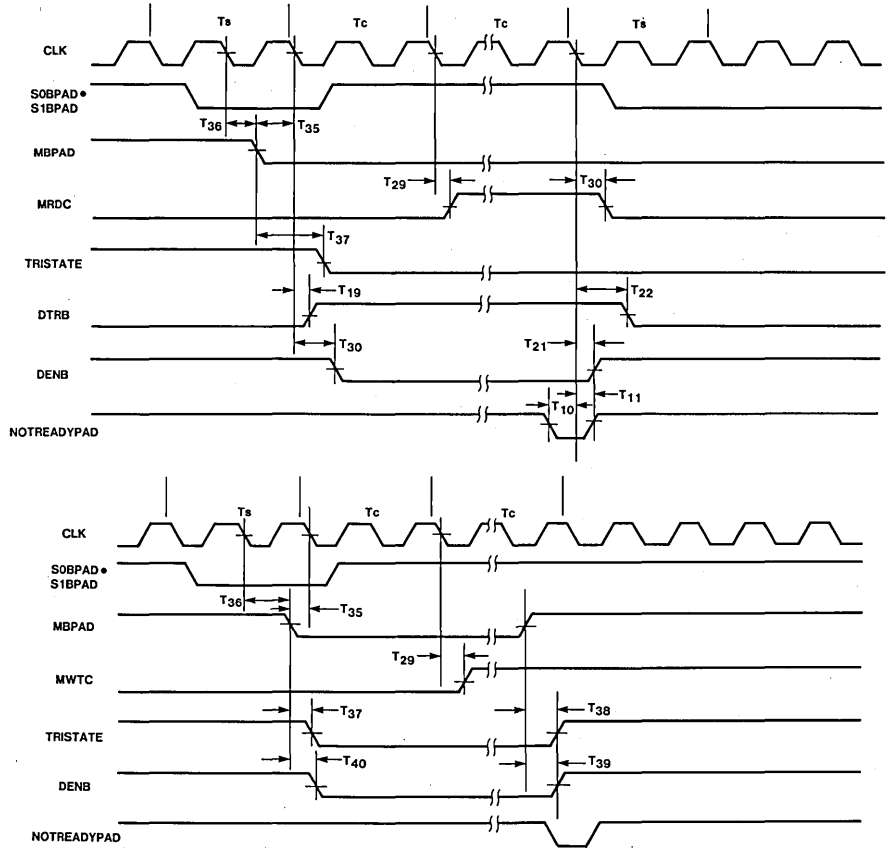
AENB Characteristics with MBPAD = 1 G40208



CLK Characteristics G40208



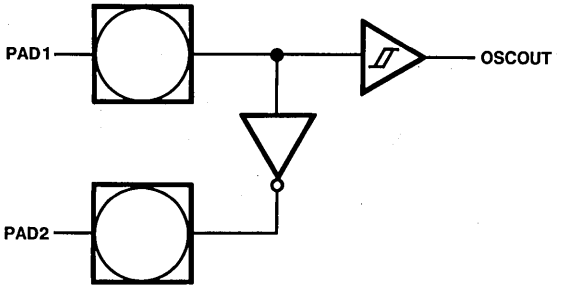
MBPAD Characteristics with AENCENPAD = 1 G40208



NOTES:
1. MPBAD is an asynchronous input. MBPAD setup and hold times specified to guarantee the response shown.
2. If the setup time, T35, is met two clock cycles will occur before CMD becomes active after the falling edge of MBPAD.

MBPAD Characteristics with AENCENPAD = 1 (Cont'd.) G40208

POSC2 — OSCILLATOR



Logic Table

Inputs	Outputs	
PAD1	PAD2	OSCOUT
0	1	0
1	0	1

POSC2 Description

Oscillator, Frequency Range to 37.5 MHz. This cell is used to provide the clock input to the SP8284 and the SP82284 clock generator cells (ICLK) from an external crystal. In test mode, the external tester clock is connected directly to PAD1, with PAD2 left unconnected. POSC2 is designed to function over the full range of operating frequencies of the SP8284 and SP82284.

Pin Description

PAD1	Oscillator Input
PAD2	Oscillator Feedback Output
OSCOUT	Clock Output

Input Capacitance

Input Name	Max.	Units
PAD1	4.11	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

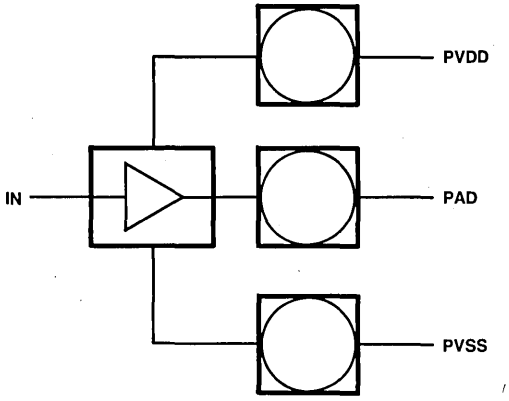
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD1 to OSCOUT	1.2	1.8	3.4	1.4	1.9	3.5	ns
PAD1 to PAD2	0.6	0.8	1.3	0.9	1.1	1.5	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
OSCOUT	0.30	0.70	1.80	0.60	0.80	1.40	ns/pF
PAD2	0.06	0.10	0.20	0.08	0.10	0.20	ns/pF

PCNO4 — NON-INVERTING CMOS OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0 1	0 1

PCNO4 Description

Function: Non-Inverting CMOS Output Buffer, 15 mA. This cell is used in conjunction with the SP8284 and SP82284 clock generator cells as a clock output driver/buffer. The output signal PAD is also used as a feedback to the SP82284 to provide the internal clock signal ICLKFB.

Pin Description

IN PAD	Data Input Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	4.0			V	IOH = −6.6 mA
VOL			0.4	V	IOL = 15.0 mA

Input Capacitance

Input Name	Max.	Units
IN	0.21	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

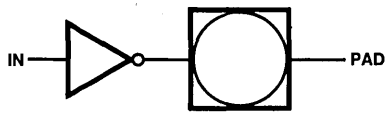
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	2.5	3.5	6.1	2.2	3.2	6.0	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.03	0.04	0.07	0.03	0.03	0.05	ns/pF

PCO2 — INVERTING CMOS OUTPUT BUFFER



Logic Table

Inputs	Outputs
IN	PAD
0	1
1	0

PCO2 Description

Function: Inverting CMOS Output Buffer, 16 mA. This cell is used in conjunction with the SP8288 and SP82288 bus controller cells as a high drive CMOS output buffer.

Pin Description

IN	Data Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	4.0			V	IOH = −2.8 mA
VOL			0.4	V	IOL = 16.0 mA

Input Capacitance

Input Name	Max.	Units
IN	0.22	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

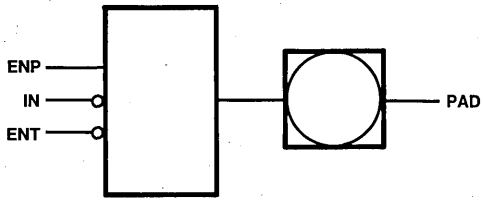
Intrinsic Propagation Delay

Signal Path	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
IN to PAD	2.5	3.4	6.5	3.3	4.7	7.8	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
PAD	0.03	0.04	0.10	0.07	0.06	0.07	ns/pF

PCOT6 — 3-STATE INVERTING CMOS OUTPUT BUFFER



Logic Table

Inputs			Outputs
IN	ENP	ENT	PAD
X	X	1	Z
X	0	0	1
0	1	0	1
1	1	0	0

PCOT6 Description

Function: 3-State Inverting CMOS Output Buffer with Enable, 42 mA. This cell is used in conjunction with the SP8288 and SP82288 bus controller cells as a command output driver/buffer.

Pin Description

IN	Data Input
ENP	Gate Enable Input
ENT	3-State Enable Input
PAD	Output

D.C. Characteristics at 0–70°C, 5V+/−10%

Parameter	Min.	Typ.	Max.	Units	Test Conditions
VOH	4.0			V	IOH = −8.0 mA
VOL			0.4	V	IOL = 42.0 mA

Input Capacitance

Input Name	Max.	Units
IN	0.35	pF
ENP	0.13	pF
ENT	0.38	pF

3-State Output Capacitance

Output Name	Max.	Units
PAD(z)	12.7	pF

A.C. Characteristics at 0-70°C, 5V+/−10%

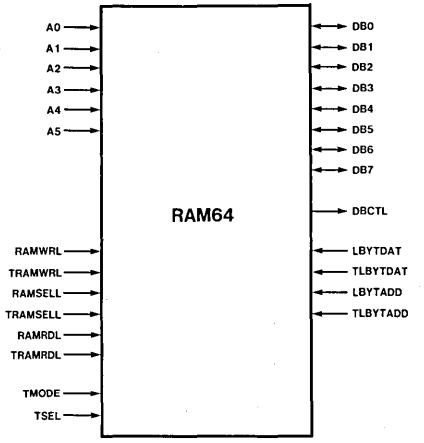
Intrinsic Propagation Delay

Parameter	Signal Path	Min.	Typ.	Max.	Units
Tplh	IN to PAD	4.6	6.0	10.7	ns
Tphl	IN to PAD	6.3	7.5	11.7	ns
Tplh	ENP to PAD	5.3	7.6	14.6	ns
Tphl	ENP to PAD	6.7	8.5	14.5	ns
Tpzh	ENT to PAD	4.6	6.0	10.7	ns
Tpzl	ENT to PAD	6.3	7.5	11.7	ns
Tphz	ENT to PAD	6.3	7.5	11.7	ns
Tplz	ENT to PAD	4.6	6.0	10.7	ns

Load Dependent Delay

Parameter	Output Name	Min.	Typ.	Max.	Units
Tplh	PAD	0.01	0.02	0.04	ns/pF
Tphl	PAD	0.02	0.02	0.03	ns/pF

RAM64 — 64 × 8 STATIC RANDOM ACCESS MEMORY



RAM64 Description

Function: 64 × 8 Static Random Access Memory (SRAM).

Pin Description

Pin Name	Pin Type	Function
A0-5	I	A0-5 are address inputs to the RAM cell. A0-5 can be configured as either latched or unlatched address inputs via the LBYTADD input signal (see LBYTADD, LBYTDAT description). These lines are not used when the RAM is configured with common, multiplexed address/data lines.
RAMWRL, TRAMWRL	I	WRITE: RAMWRL is an active LOW write enable input. When the RAM cell is selected (RAMSELL LOW) and RAMRDL is HIGH, a LOW on RAMWRL will enable the data inputs. The data present on DB0-7 will be written into the addressed RAM location.
RAMRDL, TRAMRDL	I	READ: RAMRDL is an active LOW read enable input. When the RAM cell is selected (RAMSELL LOW) and RAMWRL is HIGH, a LOW on RAMRDL will enable the data outputs. The contents of the addressed RAM location will be presented on DB0-7.
RAMSELL, TRAMSELL	I	RAM SELECT: RAMSELL is an active LOW RAM cell select input. RAMSELL must be active during all RAM operations. When RAMSELL is HIGH, DB0-7 will be in a high impedance state.
DB0-7	I/O	DATA: DB0-7 are bidirectional, 3-state data lines. During a write operation, DB0-7 are data inputs to the RAM. During a read operation, DB0-7 are data outputs from the RAM. DB0-7 outputs will remain in a high impedance state except during a read operation (RAMSELL, RAMRDL LOW). DB0-7 can also serve as a multiplexed address/data bus. In this configuration, the DB0-7 lines first present the valid address inputs to the RAM. After the address is latched internally (see LBYTADD, LBYTDAT description), DB0-7 acts as the RAM data bus operating as described above.

Pin Description (Cont'd.)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Function</th></tr>
<tr><td>LBYTADD,
LBYTDAT,
TLBYTADD,
TLBYTDAT</td><td>I</td><td>ADDRESS BUS CONTROL: LBYTADD and LBYTDAT are inputs which together determine the source of RAM address inputs and control the internal latching of the address lines (see table below). A0-5 will drive the internal address lines if LBYTDAT is tied LOW. In this configuration, the internal address lines will match A0-5 when LBYTADD is HIGH. Latching of the address inputs is accomplished by toggling LBYTADD LOW. DB0-5 will drive the internal address lines if LBYTADD is tied LOW. In this configuration, the internal address lines will match DB0-5 when LBYTDAT is HIGH. When LBYTDAT is taken LOW, the address inputs are latched and valid data may be presented on DB0-7.
<table>
<tr><th>LBYTADD</th><th>LBYTDAT</th><th>Internal Address Lines</th></tr>
<tr><td>0</td><td>0</td><td>Address Latched</td></tr>
<tr><td>0</td><td>1</td><td>Driven by DB0-5</td></tr>
<tr><td>1</td><td>0</td><td>Driven by A0-5</td></tr>
<tr><td>1</td><td>1</td><td>Invalid State</td></tr>
</table></td></tr>
<tr><td>DBCTL</td><td>0</td><td>DATA BUS CONTROL: The Data Bus Control signal is used for data bus transceiver control. When this signal is high, DB0-7 are being driven by the RAM cell.</td></tr>
<tr><td>TMODE,
TSEL</td><td>I</td><td>TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the RAM cell (see table below). The RAM cell can operate in one of three modes: user mode, active test mode, or inactive test mode.
<table>
<tr><th>TMODE</th><th>TSEL</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>User Mode (Normal operation)</td></tr>
<tr><td>0</td><td>1</td><td>User Mode (Normal operation)</td></tr>
<tr><td>1</td><td>0</td><td>Inactive Test Mode</td></tr>
<tr><td>1</td><td>1</td><td>Active Test Mode</td></tr>
</table></td></tr>
</table>

NOTE: All signals Txxx are test related input signals. All test related signals except for TMODE and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
A0-5	0.15	pF
DB0-7	1.30	pF
LBYTADD	0.10	pF
LBYTDAT	0.10	pF
RAMRDL	0.15	pF
RAMSELL	0.15	pF
RAMWRL	0.15	pF

3-State Output Capacitance

Output Name	Max.	Units
DB0-7(z)	1.30	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

WRITE CYCLE

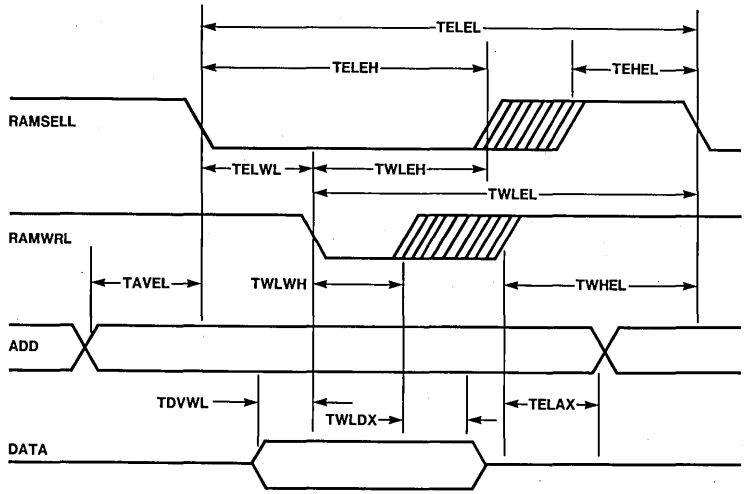
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Write Cycle Time	20.0	33.0	72.0	ns
TELEH	RAMSELL Pulse Width	12.0	20.0	43.0	ns
TEHEL	RAMSELL HIGH Time	8.0	13.0	29.0	ns
TAVEL	Address Setup Time	0	0	0	ns
TELAX	Address Hold after RAMWRL HIGH	3.0	4.0	6.0	ns
TWLEL	RAMWRL LOW to Next RAMSELL LOW	20.0	33.0	72.0	ns
TWLWH	RAMWRL Pulse Width	12.0	20.0	43.0	ns
TDVWL	Data Setup to RAMWRL LOW	0	0	0	ns
TWLDX	Data Hold after RAMWRL HIGH	5.0	7.0	12.0	ns
TELWL	RAMSELL LOW to RAMWRL LOW	0	0	0	ns
TWLEH	RAMWRL LOW to RAMSELL HIGH	12.0	20.0	43.0	ns
TWHEL	RAMWRL HIGH to Next RAMSELL LOW	8.0	13.0	29.0	ns

READ CYCLE

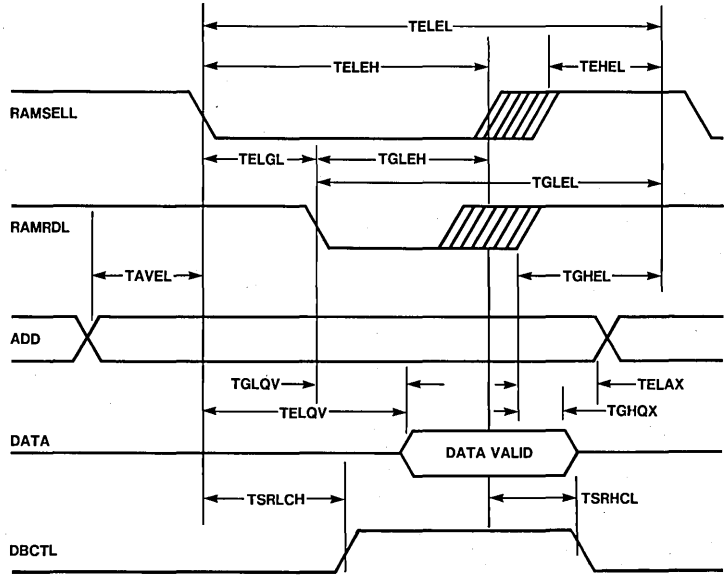
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Read Cycle Time	19.0	34.0	74.0	ns
TELQV	Access Time From RAMSELL	12.0	21.0	45.0	ns
TGLQV	Access Time From RAMRDL	12.0	21.0	45.0	ns
TELEH	RAMSELL Pulse Width	12.0	21.0	45.0	ns
TEHEL	RAMSELL HIGH Time	8.0	13.0	30.0	ns
TAVEL	Address Setup Time	5.0	6.0	10.0	ns
TELAX	Address Hold after RAMWRL HIGH	0	0	0	ns
TGLEL	RAMRDL LOW to Next RAMSELL LOW	19.0	34.0	74.0	ns
TGHEL	RAMRDL HIGH to Next RAMSELL LOW	8.0	13.0	29.0	ns
TGHQX	RAMRDL/RAMSELL HIGH to Data Float	5.0	8.0	15.0	ns
TELGL	RAMSELL LOW to RAMRDL LOW	0	0	0	ns
TGLEH	RAMRDL LOW to RAMSELL HIGH	12.0	21.0	45.0	ns
TSRLCH	RAMRDL/RAMSELL LOW to DBCTL HIGH	5.0	8.0	16.0	ns
TSRHCL	RAMRDL/RAMSELL HIGH to DBCTL LOW	5.0	8.0	16.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
DB0-7	0.75	1.50	3.20	0.75	0.90	1.50	ns/pF

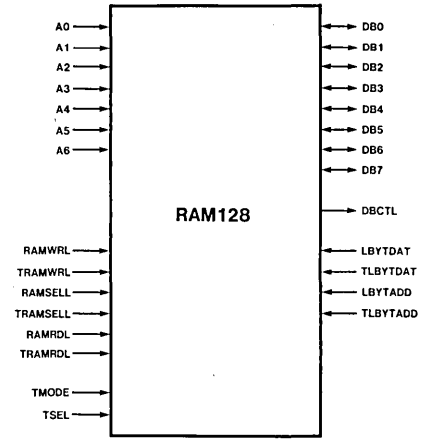


Write Cycle G40208



Read Cycle G40208

RAM128 — 128 × 8 STATIC RANDOM ACCESS MEMORY



RAM128 Description

Function: 128 × 8 Static Random Access Memory (SRAM).

Pin Description

Pin Name	Pin Type	Function
A0-6	I	ADDRESS: A0-6 are address inputs to the RAM cell. A0-6 can be configured as either latched or unlatched address inputs via the LBYTADD input signal (see LBYTADD, LBYTDAT description). These lines are not used when the RAM is configured with common, multiplexed address/data lines.
RAMWRL, TRAMWRL	I	WRITE: RAMWRL is an active LOW write enable input. When the RAM cell is selected (RAMSELL LOW) and RAMRDL is HIGH, a LOW on RAMWRL will enable the data inputs. The data present on DB0-7 will be written into the addressed RAM location.
RAMRDL, TRAMRDL	I	READ: RAMRDL is an active LOW read enable input. When the RAM cell is selected (RAMSELL LOW) and RAMWRL is HIGH, a LOW on RAMRDL will enable the data outputs. The contents of the addressed RAM location will be presented on DB0-7.
RAMSELL, TRAMSELL	I	RAM SELECT: RAMSELL is an active LOW RAM cell select input. RAMSELL must be active during all RAM operations. When RAMSELL is HIGH, DB0-7 will be in a high impedance state.
DB0-7	I/O	DATA: DB0-7 are bidirectional, 3-state data lines. During a write operation, DB0-7 are data inputs to the RAM. During a read operation, DB0-7 are data outputs from the RAM. DB0-7 will remain in a high impedance state except during a read operation (RAMSELL, RAMRDL LOW). DB0-7 can also serve as a multiplexed address/data bus. In this configuration, the DB0-7 lines first present the valid address inputs to the RAM. After the address is latched internally (see LBYTADD, LBYTDAT description), DB0-7 acts as the RAM data bus operating as described above.

Pin Description (Cont'd.)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Function</th></tr>
<tr><td>LBYTADD,
LBYTDAT,
TLBYTADD,
TLBYTDAT</td><td>I</td><td>ADDRESS BUS CONTROL: LBYTADD and LBYTDAT are inputs which together determine the source of RAM address inputs and control the internal latching of the address lines (see table below). A0-6 will drive the internal address lines if LBYTDAT is tied LOW. In this configuration, the internal address lines will match A0-6 when LYTADD is HIGH. Latching of the address inputs is accomplished by toggling LBYTADD LOW. DB0-6 will drive the internal address lines if LBYTADD is tied LOW. In this configuration, the internal address lines will match DB0-6 when LBYTDAT is HIGH. When LBYTDAT is taken LOW, the address inputs are latched and valid data may be presented on DB0-7.
<table>
<tr><th>LBYTADD</th><th>LBYTDAT</th><th>Internal Address Lines</th></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td>Address Latched
Driven by DB0-6
Driven by A0-6
Invalid State</td></tr>
</table></td></tr>
<tr><td>DBCTL</td><td>O</td><td>DATA BUS CONTROL: The Data Bus Control signal is used for data bus transceiver control. When this signal is high, DB0-7 are being driven by the RAM cell.</td></tr>
<tr><td>TMODE,
TSEL</td><td>I</td><td>TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the RAM cell (see table below). The RAM cell can operate in one of three modes: user mode, active test mode, or inactive test mode.
<table>
<tr><th>TMODE</th><th>TSEL</th><th>Function</th></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td>User Mode (Normal operation)
User Mode (Normal operation)
Inactive Test Mode
Active Test Mode</td></tr>
</table></td></tr>
</table>

NOTE: All signals Txxx are test related input signals. All test related signals except for TMODE and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
A0-6	0.30	pF
DB0-7	1.40	pF
LBYTADD	0.10	pF
LBYTDAT	0.10	pF
RAMRDL	0.30	pF
RAMSELL	0.30	pF
RAMWRL	0.30	pF

3-State Output Capacitance

Output Name	Max.	Units
DB0-7(z)	1.40	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

WRITE CYCLE

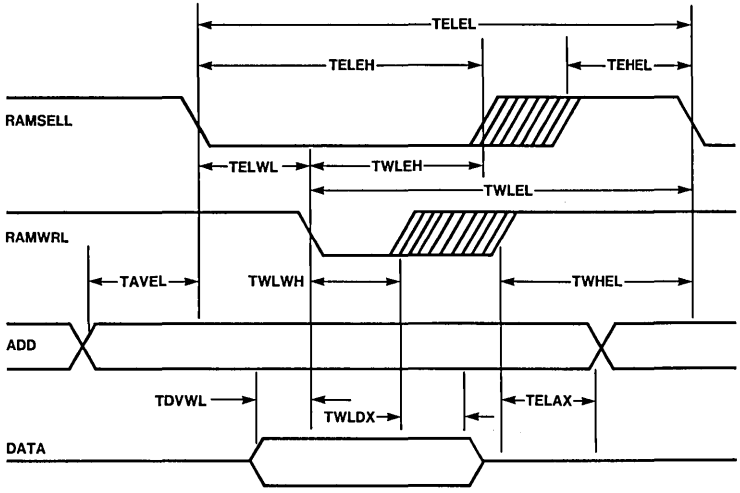
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Write Cycle Time	20.0	33.0	73.0	ns
TELEH	RAMSELL Pulse Width	12.0	20.0	43.0	ns
TEHEL	RAMSELL HIGH Time	8.0	13.0	30.0	ns
TAVEL	Address Setup Time	0	0	0	ns
TELAX	Address Hold after RAMWRL HIGH	3.0	4.0	6.0	ns
TWLEL	RAMWRL LOW to Next RAMSELL LOW	20.0	33.0	73.0	ns
TWLWH	RAMWRL Pulse Width	12.0	20.0	43.0	ns
TDVWL	Data Setup to RAMWRL LOW	0	0	0	ns
TWLDX	Data Hold after RAMWRL HIGH	5.0	7.0	12.0	ns
TELWL	RAMSELL LOW to RAMWRL LOW	0	0	0	ns
TWLEH	RAMWRL LOW to RAMSELL HIGH	12.0	20.0	43.0	ns
TWHEL	RAMWRL HIGH to Next RAMSELL LOW	8.0	13.0	30.0	ns

READ CYCLE

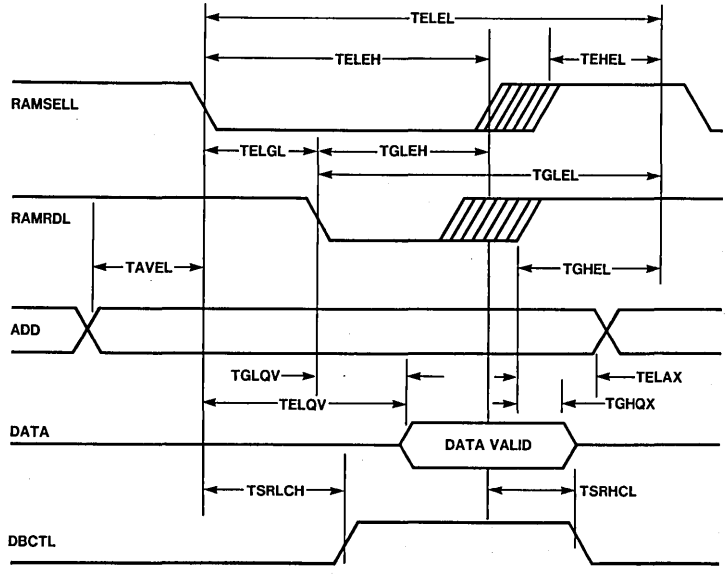
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Read Cycle Time	20.0	35.0	76.0	ns
TELQV	Access Time From RAMSELL	12.0	22.0	46.0	ns
TGLQV	Access Time From RAMRDL	12.0	22.0	46.0	ns
TELEH	RAMSELL Pulse Width	12.0	22.0	46.0	ns
TEHEL	RAMSELL HIGH Time	8.0	13.0	30.0	ns
TAVEL	Address Setup Time	5.0	6.0	10.0	ns
TELAX	Address Hold after RAMWRL HIGH	0	0	0	ns
TGLEL	RAMRDL LOW to Next RAMSELL LOW	20.0	35.0	76.0	ns
TGHEL	RAMRDL HIGH to Next RAMSELL LOW	8.0	13.0	30.0	ns
TGHQX	RAMRDL/RAMSELL HIGH to Data Float	5.0	8.0	15.0	ns
TELGL	RAMSELL LOW to RAMRDL LOW	0	0	0	ns
TGLEH	RAMRDL LOW to RAMSELL HIGH	12.0	22.0	46.0	ns
TSRLCH	RAMRDL/RAMSELL LOW to DBCTL HIGH	5.0	8.0	16.0	ns
TSRHCL	RAMRDL/RAMSELL HIGH to DBCTL LOW	5.0	8.0	16.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
DB0-7	0.75	1.50	3.20	0.75	0.90	1.50	ns/pF

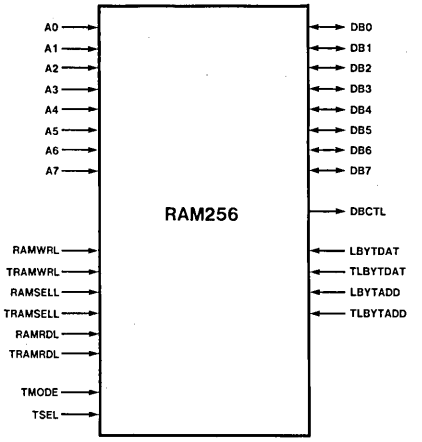


Write Cycle G40208



Read Cycle G40208

RAM256 — 256 × 8 STATIC RANDOM ACCESS MEMORY



RAM256 Description

Function: 256 × 8 Static Random Access Memory (SRAM).

Pin Description

Pin Name	Pin Type	Function
A0-7	I	ADDRESS: A0-7 are address inputs to the RAM cell. A0-7 can be configured as either latched or unlatched address inputs via the LBYTADD input signal (see LBYTADD, LBYTDAT description). These lines are not used when the RAM is configured with common, multiplexed address/data lines.
RAMWRL, TRAMWRL	I	WRITE: RAMWRL is an active LOW write enable input. When the RAM cell is selected (RAMSELL LOW) and RAMRDL is HIGH, a LOW on RAMWRL will enable the data inputs. The data present on DB0-7 will be written into the addressed RAM location.
RAMRDL, TRAMRDL	I	READ: RAMRDL is an active LOW read enable input. When the RAM cell is selected (RAMSELL LOW) and RAMWRL is HIGH, a LOW on RAMRDL will enable the data outputs. The contents of the addressed RAM location will be presented on DB0-7.
RAMSELL, TRAMSELL	I	RAM SELECT: RAMSELL is an active LOW RAM cell select input. RAMSELL must be active during all RAM operations. When RAMSELL is HIGH, DB0-7 will be in a high impedance state.
DB0-7	I/O	DATA: DB0-7 are bidirectional, 3-state data lines. During a write operation, DB0-7 are data inputs to the RAM. During a read operation, DB0-7 are data outputs from the RAM. DB0-7 will remain in a high impedance state except during a read operation (RAMSELL, RAMRDL LOW). DB0-7 can also serve as a multiplexed address/data bus. In this configuration, the DB0-7 lines first present the valid address inputs to the RAM. After the address is latched internally (see LBYTADD, LBYTDAT description), DB0-7 acts as the RAM data bus operating as described above.

Pin Description (Cont'd.)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Function</th></tr>
<tr><td>LBYTADD,
LBYTDAT
TLBYTADD,
TLBYTDAT</td><td>I</td><td>ADDRESS BUS CONTROL: LBYTADD and LBYTDAT are inputs which together determine the source of RAM address inputs and control the internal latching of the address lines (see table below). A0-7 will drive the internal address lines if LBYTDAT is tied LOW. In this configuration, the internal address lines will match A0-7 when LBYTADD is HIGH. Latching of the address inputs is accompllished by toggling LBYTADD LOW. DB0-7 will drive the internal address lines if LBYTADD is tied LOW. In this configuration, the internal address lines will match DB0-7 when LBYTDAT is HIGH. When LBYTDAT is taken LOW, the address inputs are latched and valild data may be presented on DB0-7.
<table>
<tr><th>LBYTADD</th><th>LBYTDAT</th><th>Internal Address Lines</th></tr>
<tr><td>0</td><td>0</td><td>Address Latched</td></tr>
<tr><td>0</td><td>1</td><td>Driven by DB0-7</td></tr>
<tr><td>1</td><td>0</td><td>Driven by A0-7</td></tr>
<tr><td>1</td><td>1</td><td>Invalid State</td></tr>
</table></td></tr>
<tr><td>DBCTL</td><td>O</td><td>DATA BUS CONTROL: The Data Bus Control signal is used for data bus transceiver control. When this signal is high, DB0-7 are being driven by the RAM cell.</td></tr>
<tr><td>TMODE,
TSEL</td><td>I</td><td>TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the RAM cell (see table below). The RAM cell can operate in one of three modes: user mode, active test mode, or inactive test mode.
<table>
<tr><th>TMODE</th><th>TSEL</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>User Mode (Normal operation)</td></tr>
<tr><td>0</td><td>1</td><td>User Mode (Normal operation)</td></tr>
<tr><td>1</td><td>0</td><td>Inactive Test Mode</td></tr>
<tr><td>1</td><td>1</td><td>Active Test Mode</td></tr>
</table></td></tr>
</table>

NOTE: All signals Txxx are test related input signals. All test related signals except for TMODE and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
A0-7	0.45	pF
DB0-7	1.50	pF
LBYTADD	0.10	pF
LBYTDAT	0.10	pF
RAMRDL	0.45	pF
RAMSELL	0.45	pF
RAMWRL	0.45	pF

3-State Output Capacitance

Output Name	Max.	Units
DB0-7(z)	1.50	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

WRITE CYCLE

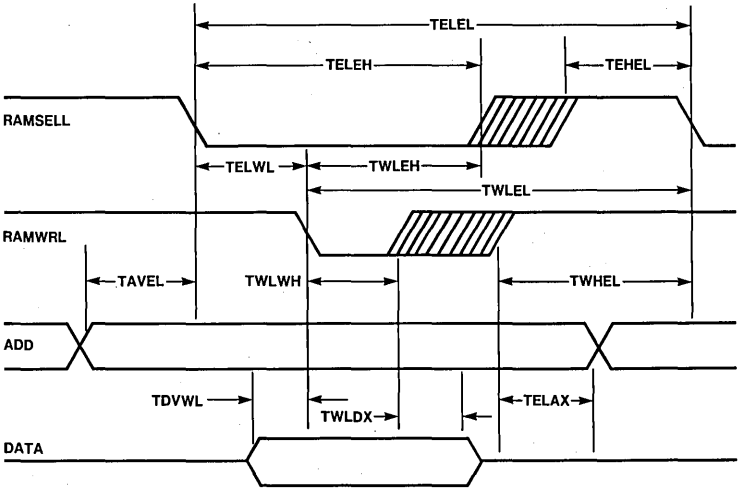
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Write Cycle Time	21.0	35.0	77.0	ns
TELEH	RAMSELL Pulse Width	12.0	19.0	43.0	ns
TEHEL	RAMSELL HIGH Time	9.0	16.0	34.0	ns
TAVEL	Address Setup Time	0	0	0	ns
TELAX	Address Hold after RAMWRL HIGH	3.0	4.0	6.0	ns
TWLEL	RAMWRL LOW to Next RAMSELL LOW	21.0	35.0	77.0	ns
TWLWH	RAMWRL Pulse Width	12.0	19.0	43.0	ns
TDVWL	Data Setup to RAMWRL LOW	0	0	0	ns
TWLDX	Data Hold after RAMWRL HIGH	5.0	7.0	12.0	ns
TELWL	RAMSELL LOW to RAMWRL LOW	0	0	0	ns
TWLEH	RAMWRL LOW to RAMSELL HIGH	12.0	19.0	43.0	ns
TWHEL	RAMWRL HIGH to Next RAMSELL LOW	9.0	16.0	34.0	ns

READ CYCLE

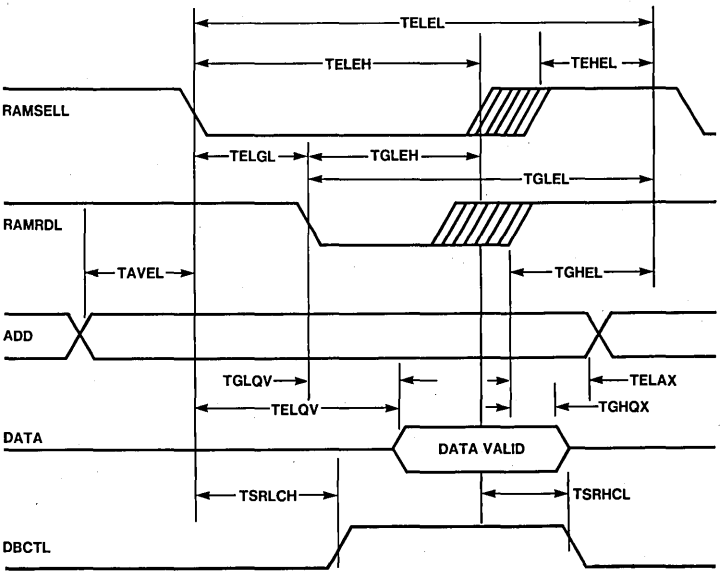
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Read Cycle Time	23.0	42.0	86.0	ns
TELQV	Access Time From RAMSELL	14.0	26.0	52.0	ns
TGLQV	Access Time From RAMRDL	14.0	26.0	52.0	ns
TELEH	RAMSELL Pulse Width	14.0	26.0	52.0	ns
TEHEL	RAMSELL HIGH Time	9.0	16.0	34.0	ns
TAVEL	Address Setup Time	5.0	6.0	11.0	ns
TELAX	Address Hold after RAMWRL HIGH	0	0	0	ns
TGLEL	RAMRDL LOW to Next RAMSELL LOW	23.0	42.0	86.0	ns
TGHEL	RAMRDL HIGH to Next RAMSELL LOW	9.0	16.0	34.0	ns
TGHQX	RAMRDL/RAMSELL HIGH to Data Float	5.0	8.0	15.0	ns
TELGL	RAMSELL LOW to RAMRDL LOW	0	0	0	ns
TGLEH	RAMRDL LOW to RAMSELL HIGH	14.0	26.0	52.0	ns
TSRLCH	RAMRDL/RAMSELL LOW to DBCTL HIGH	5.0	8.0	16.0	ns
TSRHCL	RAMRDL/RAMSELL HIGH to DBCTL LOW	5.0	8.0	16.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
DB0-7	0.75	1.50	3.20	0.75	0.90	1.50	ns/pF

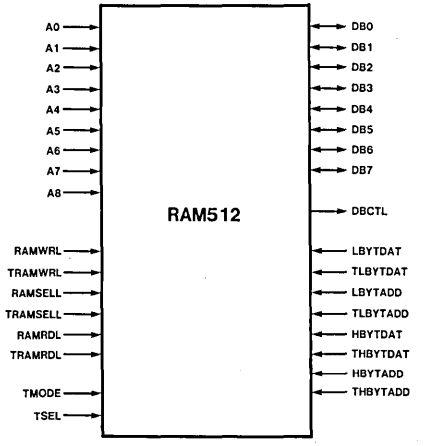


Write Cycle G40208



Read Cycle G40208

RAM512 — 512 × 8 STATIC RANDOM ACCESS MEMORY



RAM512 Description

Function: 512 × 8 Static Random Access Memory (SRAM).

Pin Description

Pin Name	Pin Type	Function
A0-8	I	ADDRESS: A0-8 are address inputs to the RAM cell. A0-8 can be configured as either latched or unlatched address inputs via the LBYTADD and HBYTADD input signals (see LBYTADD, LBYTDAT, HBYTADD, HBYTDAT description). These lines are not used when the RAM is configured with common, multiplexed address/data lines.
RAMWRL, TRAMWRL	I	WRITE: RAMWRL is an active LOW write enable input. When the RAM cell is selected (RAMSELL LOW) and RAMRDL is HIGH, a LOW on RAMWRL will enable the data inputs. The data present on DB0-7 will be written into the addressed RAM location.
RAMRDL, TRAMRDL	I	READ: RAMRDL is an active LOW read enable input. When the RAM cell is selected (RAMSELL LOW) and RAMWRL is HIGH, a LOW on RAMRDL will enable the data outputs. The contents of the addressed RAM location will be presented on DB0-7.
RAMSELL, TRAMSELL	I	RAM SELECT: RAMSELL is an active LOW RAM cell select input. RAMSELL must be active during all RAM operations. When RAMSELL is HIGH, DB0-7 will be in a high impedance state.

Pin Description (Cont'd.)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Function</th></tr>
<tr><td>DB0-7</td><td>I/O</td><td>DATA: DB0-7 are bidirectional, 3-state data lines. During a write operation, DB0-7 are data inputs to the RAM. During a read operation, DB0-7 are data outputs from the RAM. DB0-7 will remain in a high impedance state except during a read operation (RAMSELL, RAMRDL LOW). DB0-7 can also serve as a multiplexed address/data bus. In this configuration, the DB0-7 lines first present the valid address inputs to the RAM. After the address is latched internally (see LBYTADD, LBYTDAT, HBYTADD, HBYTDAT description), DB0-7 acts as the RAM data bus operating as described above.</td></tr>
<tr><td>LBYTADD,
LBYTDAT,
HBYTADD,
HBYTDAT,
TLBYTADD,
TLBYTDAT,
THBYTADD,
THBYTDAT</td><td>I</td><td>ADDRESS BUS CONTROL: LBYTADD, LBYTDAT, HBYTADD, and HBYTDAT are inputs which together determine the source of RAM address inputs and control the internal latching of the address lines (see table below). A0-8 will drive the internal address lines if LBYTDAT and HBYTDAT are tied LOW. In this configuration, the internal address lines will match A0-8 when LBYTADD and HBYTADD are HIGH. Latching of the address inputs is accomplished by toggling LBYTADD and HBYTADD LOW. DB0-7 will drive the internal address lines if LBYTADD and HBYTADD are tied LOW. In this configuration, the internal address lines A0-8 are latched from DB0-7 in two stages. First, A0-7 is driven by DB0-7 when LBYTDAT is HIGH and HBYTDAT is LOW and is latched by toggling LBYTDAT LOW. Next, HBYTDAT is taken high to allow the data on DB0 to appear on address bit A8. These address bits are latched by toggling HBYTDAT LOW. When LBYTDAT and HBYTDAT are LOW and the valid address has been latched in, valid data may be presented on DB0-7.
<table>
<tr><th>LBYTADD</th><th>LBYTDAT</th><th>Internal Address Lines</th></tr>
<tr><td>0</td><td>0</td><td>Address Latched</td></tr>
<tr><td>0</td><td>1</td><td>Driven by DB0-7 (A0-7)</td></tr>
<tr><td>1</td><td>0</td><td>Driven by A0-8</td></tr>
<tr><td>1</td><td>1</td><td>Invalid State</td></tr>
<tr><th>HBYTADD</th><th>HBYTDAT</th><th>Internal Address Lines</th></tr>
<tr><td>0</td><td>0</td><td>Address Latched</td></tr>
<tr><td>0</td><td>1</td><td>Driven by DB0 (A8)</td></tr>
<tr><td>1</td><td>0</td><td>Driven by A0-8</td></tr>
<tr><td>1</td><td>1</td><td>Invalid State</td></tr>
</table></td></tr>
<tr><td>DBCTL</td><td>O</td><td>DATA BUS CONTROL: The Data Bus Control signal is used for data bus transceiver control. When this signal is high, DB0-7 are being driven by the RAM cell.</td></tr>
</table>

Pin Description (Cont'd.)

Pin Name	Pin Type	Function		
TMODE, TSEL	I	TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the RAM cell (see table below). The RAM cell can operate in one of three modes: user mode, active test mode, or inactive test mode.		
		TMODE	TSEL	Function
		0	0	User Mode (Normal operation)
		0	1	User Mode (Normal operation)
		1	0	Inactive Test Mode
		1	1	Active Test Mode

NOTE: All signals Txxx are test related input signals. All test related signals except for TMODE and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
A0-8	0.60	pF
DB0-7	1.60	pF
HBYTADD	0.10	pF
HBYTDAT	0.10	pF
LBYTADD	0.10	pF
LBYTDAT	0.10	pF
RAMRDL	0.60	pF
RAMSELL	0.60	pF
RAMWRL	0.60	pF

3-State Output Capacitance

Output Name	Max.	Units
DB0-7(z)	1.60	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

WRITE CYCLE

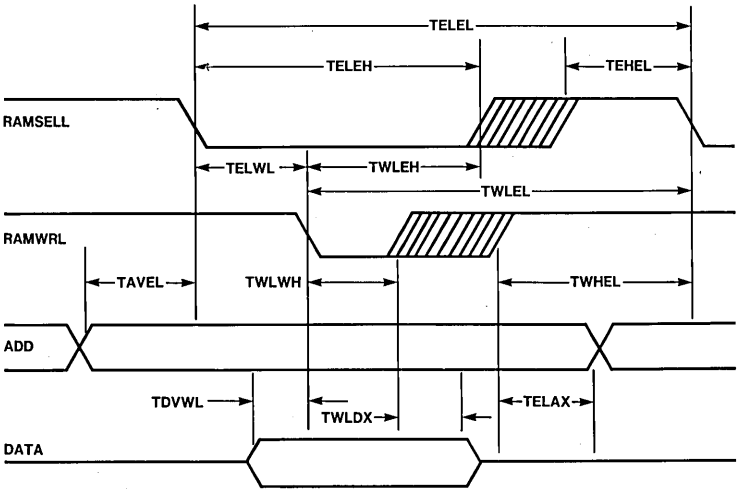
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Write Cycle Time	23.0	37.0	81.0	ns
TELEH	RAMSELL Pulse Width	12.0	20.0	43.0	ns
TEHEL	RAMSELL HIGH Time	11.0	17.0	38.0	ns
TAVEL	Address Setup Time	0	0	0	ns
TELAX	Address Hold after RAMWRL HIGH	3.0	4.0	6.0	ns
TWLEL	RAMWRL LOW to Next RAMSELL LOW	23.0	37.0	81.0	ns
TWLWH	RAMWRL Pulse Width	12.0	20.0	43.0	ns
TDVWL	Data Setup to RAMWRL LOW	0	0	0	ns
TWLDX	Data Hold after RAMWRL HIGH	5.0	7.0	12.0	ns
TELWL	RAMSELL LOW to RAMWRL LOW	0	0	0	ns
TWLEH	RAMWRL LOW to RAMSELL HIGH	12.0	20.0	43.0	ns
TWHEL	RAMWRL HIGH to Next RAMSELL LOW	11.0	17.0	38.0	ns

READ CYCLE

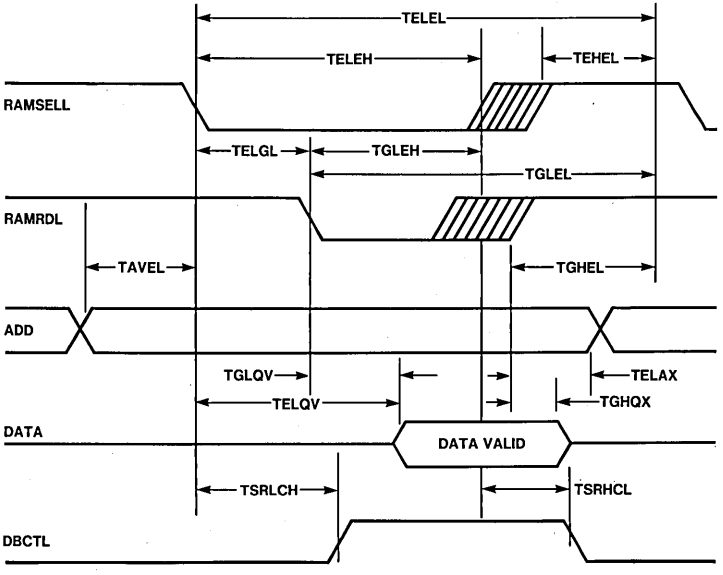
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Read Cycle Time	26.0	47.0	95.0	ns
TELQV	Access Time From RAMSELL	15.0	30.0	57.0	ns
TGLQV	Access Time From RAMRDL	15.0	30.0	57.0	ns
TELEH	RAMSELL Pulse Width	15.0	30.0	57.0	ns
TEHEL	RAMSELL HIGH Time	11.0	17.0	38.0	ns
TAVEL	Address Setup Time	5.0	7.0	11.0	ns
TELAX	Address Hold after RAMWRL HIGH	0	0	0	ns
TGLEL	RAMRDL LOW to Next RAMSELL LOW	26.0	47.0	95.0	ns
TGHEL	RAMRDL HIGH to Next RAMSELL LOW	11.0	17.0	38.0	ns
TGHQX	RAMRDL/RAMSELL HIGH to Data Float	5.0	8.0	15.0	ns
TELGL	RAMSELL LOW to RAMRDL LOW	0	0	0	ns
TGLEH	RAMRDL LOW to RAMSELL HIGH	15.0	30.0	57.0	ns
TSRLCH	RAMRDL/RAMSELL LOW to DBCTL HIGH	5.0	8.0	16.0	ns
TSRHCL	RAMRDL/RAMSELL HIGH to DBCTL LOW	5.0	8.0	16.0	ns

Load Dependent Delay

Output Name	Tplh			Tphl			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
DB0-7	0.75	1.50	3.20	0.75	0.90	1.50	ns/pF

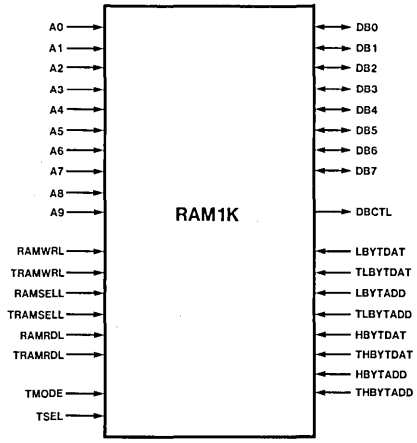


Write Cycle G40208



Read Cycle G40208

RAM1K — 1024 × 8 STATIC RANDOM ACCESS MEMORY



RAM1K Description

Function: 1024 × 8 Static Random Access Memory (SRAM).

Pin Description

Pin Name	Pin Type	Function
A0-9	I	ADDRESS: A0-9 are address inputs to the RAM cell. A0-9 can be configured as either latched or unlatched address inputs via the LBYTADD and HBYTADD input signals (see LBYTADD, LBYTDAT, HBYTADD, HBYTDAT description). These lines are not used when the RAM is configured with common, multiplexed address/data lines.
RAMWRL, TRAMWRL	I	WRITE: RAMWRL is an active LOW write enable input. When the RAM cell is selected (RAMSELL LOW) and RAMRDL is HIGH, a LOW on RAMWRL will enable the data inputs. The data present on DB0-7 will be written into the addressed RAM location.
RAMRDL, TRAMRDL	I	READ: RAMRDL is an active LOW read enable input. When the RAM cell is selected (RAMSELL LOW) and RAMWRL is HIGH, a LOW on RAMRDL will enable the data outputs. The contents of the addressed RAM location will be presented on DB0-7.
RAMSELL, TRAMSELL	I	RAM SELECT: RAMSELL is an active LOW RAM cell select input. RAMSELL must be active during all RAM operations. When RAMSELL is HIGH, DB0-7 will be in a high impedance state.

Pin Description (Cont'd.)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Function</th></tr>
<tr><td>DB0-7</td><td>I/O</td><td>DATA: DB0-7 are bidirectional, 3-state data lines. During a write operation, DB0-7 are data inputs to the RAM. During a read operation, DB0-7 are data outputs from the RAM. DB0-7 will remain in a high impedance state except during a read operation (RAMSELL, RAMRDL LOW). DB0-7 can also serve as a multiplexed address/data bus. In this configuration, the DB0-7 lines first present the valid address inputs to the RAM. After the address is latched internally (see LBYTADD, LBYTDAT, HBYTADD, HBYTDAT description), DB0-7 acts as the RAM data bus operating as described above.</td></tr>
<tr><td>LBYTADD,
LBYTDAT
HBYTADD,
HBYTDAT
TLBYTADD,
TLBYTDAT,
THBYTADD,
THBYTDAT</td><td>I</td><td>ADDRESS BUS CONTROL: LBYTADD, LBYTDAT, HBYTADD, and HBYTDAT are inputs which together determine the source of RAM address inputs and control the internal latching of the address lines (see table below). A0-9 will drive the internal address lines if LBYTDAT and HBYTDAT are tied LOW. In this configuration, the internal address lines will match A0-9 when LBYTADD and HBYTADD are HIGH. Latching of the address inputs is accomplished by toggling LBYTADD and HBYTADD LOW. DB0-7 will drive the internal address lines if LBYTADD and HBYTADD are tied LOW. In this configuration, the internal address lines A0-9 are latched from DB0-7 in two stages. First, A0-7 is driven by DB0-7 when LBYTDAT is HIGH and HBYTDAT is LOW and is latched by toggling LBYTDAT LOW. Next, HBYTDAT is taken high to allow the data on DB0-1 to appear on address bits A8-9. These address bits are latched by toggling HBYTDAT LOW. When LBYTDAT and HBYTDAT are LOW and the valid address has been latched in, valid data may be presented on DB0-7.
<table>
<tr><th>LBYTADD</th><th>LBYTDAT</th><th>Internal Address Lines</th></tr>
<tr><td>0</td><td>0</td><td>Address Latched</td></tr>
<tr><td>0</td><td>1</td><td>Driven by DB0-7 (A0-7)</td></tr>
<tr><td>1</td><td>0</td><td>Driven by A0-9</td></tr>
<tr><td>1</td><td>1</td><td>Invalid State</td></tr>
<tr><th>HBYTADD</th><th>HBYTDAT</th><th>Internal Address Lines</th></tr>
<tr><td>0</td><td>0</td><td>Address Latched</td></tr>
<tr><td>0</td><td>1</td><td>Driven by DB0-1 (A8-9)</td></tr>
<tr><td>1</td><td>0</td><td>Driven by A0-9</td></tr>
<tr><td>1</td><td>1</td><td>Invalid State</td></tr>
</table></td></tr>
<tr><td>DBCTL</td><td>O</td><td>DATA BUS CONTROL: The Data Bus Control signal is used for data bus transceiver control. When this signal is high, DB0-7 are being driven by the RAM cell.</td></tr>
</table>

Pin Description (Cont'd.)

Pin Name	Pin Type	Function		
TMODE, TSEL	I	TEST CONTROL LINES: TMODE and TSEL are inputs which together determine the operating mode of the RAM cell (see table below). The RAM cell can operate in one of three modes: user mode, active test mode, or inactive test mode.		
		TMODE	TSEL	Function
		0	0	User Mode (Normal operation)
		0	1	User Mode (Normal operation)
		1	0	Inactive Test Mode
		1	1	Active Test Mode

NOTE: All signals Txxx are test related input signals. All test related signals except for TMODE and TSEL have a user signal equivalent and are listed with their non-test counterpart. These test signals have the identical functionality as their user signal equivalents, but are not used during normal user operation. All test signals must be accessible through a package pin. This can be accomplished by tying the test signal to its user signal equivalent if it is directly connected to a package pin, or to any other user input signal that is directly connected to a package pin. One package pin for TMODE and TSEL is required per device, regardless of the number of cells implemented which require these inputs. Additional test logic will be necessary for TSEL generation to multiple cells.

Input Capacitance

Input Name	Max.	Units
A0-9	0.90	pF
DB0-7	2.00	pF
HBYTADD	0.10	pF
HBYTDAT	0.10	pF
LBYTADD	0.10	pF
LBYTDAT	0.10	pF
RAMRDL	0.90	pF
RAMSELL	0.90	pF
RAMWRL	0.90	pF

3-State Output Capacitance

Output Name	Max.	Units
DB0-7(z)	2.00	pF

A.C. Characteristics at 0–70°C, 5V+/−10%

WRITE CYCLE

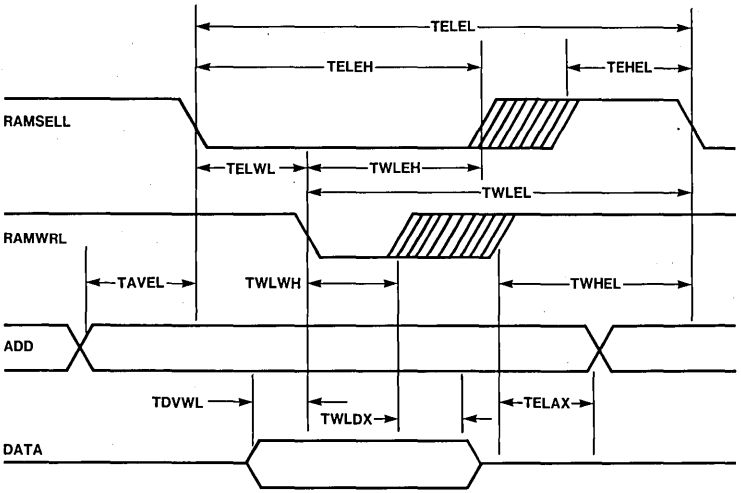
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Write Cycle Time	23.0	40.0	88.0	ns
TELEH	RAMSELL Pulse Width	12.0	20.0	43.0	ns
TEHEL	RAMSELL HIGH Time	11.0	20.0	45.0	ns
TAVEL	Address Setup Time	0	0	0	ns
TELAX	Address Hold after RAMWRL HIGH	2.0	3.0	6.0	ns
TWLEL	RAMWRL LOW to Next RAMSELL LOW	23.0	40.0	88.0	ns
TWLWH	RAMWRL Pulse Width	12.0	20.0	43.0	ns
TDVWL	Data Setup to RAMWRL LOW	0	0	0	ns
TWLDX	Data Hold after RAMWRL HIGH	5.0	7.0	12.0	ns
TELWL	RAMSELL LOW to RAMWRL LOW	0	0	0	ns
TWLEH	RAMWRL LOW to RAMSELL HIGH	12.0	20.0	43.0	ns
TWHEL	RAMWRL HIGH to Next RAMSELL LOW	11.0	20.0	45.0	ns

READ CYCLE

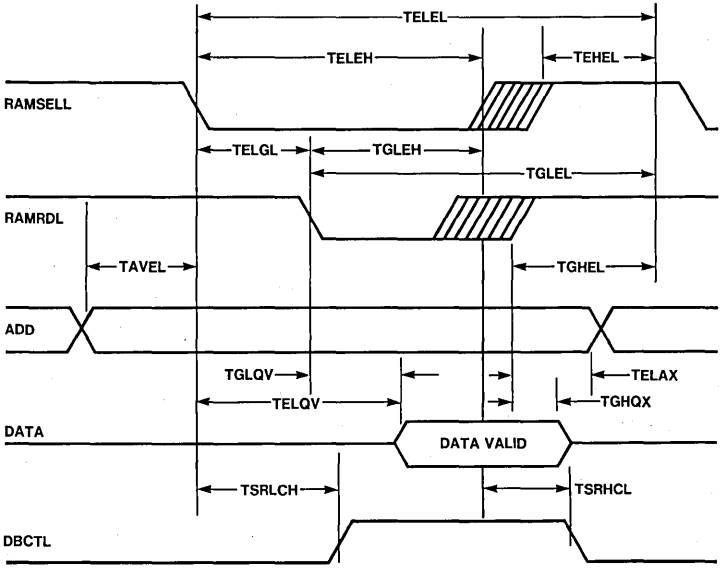
Symbol	Parameter	Min.	Typ.	Max.	Units
TELEL	Read Cycle Time	28.0	55.0	112.0	ns
TELQV	Access Time From RAMSELL	17.0	35.0	67.0	ns
TGLQV	Access Time From RAMRDL	17.0	35.0	67.0	ns
TELEH	RAMSELL Pulse Width	17.0	35.0	67.0	ns
TEHEL	RAMSELL HIGH Time	11.0	20.0	45.0	ns
TAVEL	Address Setup Time	5.0	7.0	11.0	ns
TELAX	Address Hold after RAMWRL HIGH	0	0	0	ns
TGLEL	RAMRDL LOW to Next RAMSELL LOW	28.0	55.0	112.0	ns
TGHEL	RAMRDL HIGH to Next RAMSELL LOW	11.0	20.0	45.0	ns
TGHQX	RAMRDL/RAMSELL HIGH to Data Float	5.0	8.0	15.0	ns
TELGL	RAMSELL LOW to RAMRDL LOW	0	0	0	ns
TGLEH	RAMRDL LOW to RAMSELL HIGH	17.0	35.0	67.0	ns
TSRLCH	RAMRDL/RAMSELL LOW to DBCTL HIGH	5.0	8.0	16.0	ns
TSRHCL	RAMRDL/RAMSELL HIGH to DBCTL LOW	5.0	8.0	16.0	ns

Load Dependent Delay

Output Name	Tplh Min.	Tplh Typ.	Tplh Max.	Tphl Min.	Tphl Typ.	Tphl Max.	Units
DB0-7	0.75	1.50	3.20	0.75	0.90	1.50	ns/pF



Write Cycle G40208



Read Cycle G40208

Appendix A
Packaging

APPENDIX A
PACKAGING

Intel offers a wide array of standard package types for use with cell-based ASICs. Refer to Table A-1 below for a chart of standard package types currently available. Additional package types are available upon request.

Table A-1 lists the available packages categorically by type and by lead count. In addition, the pin spacing for each package type is given. Please consult with your Intel Sales Representative if you have any questions regarding a given package type.

Table A-1. Packages for Cell-Based ASICs

Package Type	Lead Count	Pin Spacing (Mils)
Plastic Dual-In-Line:		
PDIP	16	100
PDIP	18	100
PDIP	20	100
PDIP	24	100
PDIP	28	100
PDIP	40	100
PDIP	48	100
Ceramic Dual-In-Line:		
CDIP	20	100
CDIP	24	100
CDIP	28	100
CDIP	40	100
CDIP	48	100
Side Brazed Ceramic Dual-In-Line:		
S/B DIP	28	100
S/B DIP	40	100
S/B DIP	48	100
Plastic Leaded Chip Carrier:		
PLCC	20	50
PLCC	28	50
PLCC	32	50
PLCC	44	50
PLCC	52	50
PLCC	68	50
PLCC	84	50
Ceramic Leaded Chip Carrier:		
CLCC	44	50
CLCC	68	50
CLCC	84	50

Table A-1. Packages for Cell-Based ASICs (Cont'd.)

Package Type	Lead Count	Pin Spacing (Mils)
Ceramic Leadless Chip Carrier:		
LCC	68	50
LCC	84	50
Plastic Quad Flat Pack:		
PQFP	84	25
PQFP	100	25
PQFP	132	25
PQFP	164	25
PQFP	196	25
Ceramic Quad Flat Pack:		
CQFP	84	25
CQFP	100	25
CQFP	132	25
CQFP	164	25
CQFP	196	25
Pressed Ceramic Quadpack:		
CERQUAD	28	50
CERQUAD	44	50
CERQUAD	68	50
Plastic Pin Grid Array:		
PPGA	68	100
PPGA	72	100
PPGA	88	100
PPGA	100	100
PPGA	132	100
PPGA	144	100
Ceramic Pin Grid Array:		
CPGA	68	100
CPGA	72	100
CPGA	84	100
CPGA	88	100
CPGA	100	100
CPGA	132	100
CPGA	144	100
CPGA	180	100
CPGA	208	100
EIAJ Quad Flat Pack*:		
EIAJQFP	80	25.6
EIAJQFP	100	25.6
EIAJQFP	124	25.6
EIAJQFP	144	25.6
EIAJQFP	160	25.6

*Contact your Intel Sales Representative

Appendix B
Terms and Definitions

APPENDIX B
TERMS AND DEFINITIONS

The following terms and definitions are for cell specification parameters which appear in the Intel 1.5 Micron CHMOS III Cell Library data sheets. These terms and definitions are in accordance with current JEDEC standards.

IIH: High-Level Input Current

The current into* an input when a specified high-level voltage is applied to that input.

IIL: Low-Level Input Current

The current into* an input when a specified low-level voltage is applied to that input.

IOH: High-Level Output Current

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

IOL: Low-Level Output Current

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

Tphl: Propagation Delay Time, High-to-Low Level Output

The time interval between the specified reference points on the input and output voltage waveforms with the specified output changing from the defined high level to the defined low level.

Tphz: Disable Time from the High Level (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms with the specified output changing from the defined high level to a high-impedance (off) state.

Tplh: Propagation Delay Time, Low-to-High Level Output

The time interval between the specified reference points on the input and output voltage waveforms with the specified output changing from the defined low level to the defined high level.

Tplz: Disable Time from the Low Level (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms with the specified output changing from the defined low level to a high-impedance (off) state.

*Current out of a terminal is given as a negative quantity.

Tpzh: Enable Time to the High Level (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms with the specified output changing from a high-impedance (off) state to the defined high level.

Tpzl: Enable Time to the Low Level (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms with the specified output changing from a high-impedance (off) state to the defined low level.

Th: Hold time

The time interval during which a signal is retained at a specified input after an active transition occurs at another specified input.

Note: The hold time is the actual time between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which operation of the digital circuit is guaranteed.

Tsu: Setup Time

The time interval between the application of a signal at a specified input and a subsequent active transition at another specified input.

Note: The setup time is the actual time between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

Vhys: Hysteresis

The difference between the positive-going and negative-going input threshold voltages.

VIH (min): Minimum High-Level Input Voltage

The least positive (most negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

VIL (max): Maximum Low-Level Input Voltage

The most positive (least negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

VOH: High-Level Output Voltage

The voltage level at an output with input conditions applied that, according to the product specification, will establish a high level at the output.

VOL: Low-Level Output Voltage

The voltage level at an output with input conditions applied that, according to the product specification, will establish a low level at the output.

VT+: Positive-Going Input Threshold Voltage

The input voltage level that, when crossed as the input voltage is rising, enables an output to change its logic state.

VT−: Negative-Going Input Threshold Voltage

The input voltage level that, when crossed as the input voltage is falling, enables an output to change its logic state.

Appendix C
Cell Reference Guide

APPENDIX C
CELL REFERENCE GUIDE

Cell	Description	Grid Count	Page
ADDB	Telescoping Adder Body	169	3-161
ADDC	Telescoping Adder Control	13	3-160
ADDP	Telescoping Adder Carry Out Driver	39	3-163
AND2	2 Input AND, Normal Drive	52	3-39
AND3	3 Input AND, Normal Drive	65	3-40
AND4	4 Input AND, Normal Drive	78	3-41
AND5	5 Input AND, Normal Drive	104	3-42
AND6	6 Input AND, Normal Drive	130	3-43
AND7	7 Input AND, Normal Drive	169	3-44
AND8	8 Input AND, Normal Drive	182	3-45
AOI22	2 AND2 into NOR2, Normal Drive	78	3-54
AOR22	2 AND2 into OR2, Normal Drive	78	3-53
BUF	Buffer, Normal Drive	39	3-18
BUFH	Buffer, High Drive	52	3-18
BUFTD	3-State Buffer with Active High Output Enable, Normal Drive	65	3-23
BUFTE	3-State Buffer with Active Low Output Enable, Normal Drive	65	3-21
BUF2	Buffer with Dual Output, Normal Drive	52	3-30
CMPB	Telescoping Magnitude Comparator Body	182	3-168
CMPC	Telescoping Magnitude Comparator Control	26	3-167
CMPP	Telescoping Magnitude Comparator Equal/ Greater Than/Less Than Driver	104	3-170
CPR	8/9-bit Parity Checker/Generator	429	3-100
CULB	Telescoping Up Counter Body	338	3-138
CULC	Telescoping Up Counter Control	169	3-136
CULP	Telescoping Up Counter Carry Out Driver	39	3-141
CUPB	Telescoping Up/Down Counter Body	429	3-151
CUPC	Telescoping Up/Down Counter Control	195	3-148
CUPP	Telescoping Up/Down Counter End Count Driver	26	3-154
CUPP2	Telescoping Up/Down Counter End Count/Carry/ Borrow Driver	143	3-156
DMX2	2-Line to 4-Line Demultiplexer/Decoder with 2 Enables	299	3-96
DMX3	3-Line to 8-Line Demultiplexer/Decoder	559	3-98
EXN2	2 Input EXCLUSIVE NOR, Normal Drive	65	3-56
EXR2	2 Input EXCLUSIVE OR, Normal Drive	78	3-55
FFD	D Flip-Flop with Master Reset	208	3-68
FFDE	D Flip-Flop with Enable and Master Reset	273	3-70
FFDHI	Positive Edge Event Trigger with Master Reset	195	3-81
FFDM2	D Flip-Flop with 2 to 1 Data Multiplexer and Master Reset	260	3-77
FFJK	JK Flip-Flop with Master Reset	247	3-61
FFT	Toggle Flip-Flop with Master Reset	195	3-57
FFTE	Toggle Flip-Flop with Enable and Master Reset	247	3-59
FLDE	D Flip-Flop with Enable, Master Set, and Master Reset	260	3-72
FLDET	3-State D Flip-Flop with Enable, Master Set, and Master Reset	260	3-74

Cell	Description	Grid Count	Page
FLDM2	D Flip-Flop with 2 to 1 Data Multiplexer, Master Set and Master Reset	260	3-79
FLJK	JK Flip-Flop with Master Set and Master Reset	260	3-63
FLJKT	3-State JK Flip-Flop with Master Set and Master Reset	247	3-65
INVN	Inverter, Normal Drive	26	3-12
INVNH	Inverter, High Drive	39	3-12
INVTD	3-State Inverter with Active High Output Enable, Normal Drive	52	3-16
INVTE	3-State Inverter with Active Low Output Enable, Normal Drive	52	3-14
LAD	Transparent D Latch with Master Reset	143	3-83
LANSR	$\overline{S}$-$\overline{R}$ Latch with Enable and Master Reset	182	3-91
LASR	S-$\overline{R}$ Latch with Enable and Master Reset	182	3-87
LNSR	$\overline{S}$-$\overline{R}$ Latch with Master Reset	104	3-89
LSR	S-R Latch with Master Reset	104	3-85
MUX21	2-Line to 1-Line Multiplexer	104	3-93
MUX41	4-Line to 1-Line Multiplexer	182	3-94
NAN2	2 Input NAND, Normal Drive	39	3-25
NAN3	3 Input NAND, Normal Drive	65	3-26
NAN4	4 Input NAND, Normal Drive	78	3-27
NAN5	5 Input NAND, Normal Drive	104	3-28
NAN6	6 Input NAND, Normal Drive	117	3-29
NAN7	7 Input NAND, Normal Drive	169	3-30
NAN8	8 Input NAND, Normal Drive	182	3-31
NOR2	2 Input NOR, Normal Drive	52	3-32
NOR3	3 Input NOR, Normal Drive	78	3-33
NOR4	4 Input NOR, Normal Drive	104	3-34
NOR5	5 Input NOR, Normal Drive	130	3-35
NOR6	6 Input NOR, Normal Drive	143	3-36
NOR7	7 Input NOR, Normal Drive	169	3-37
NOR8	8 Input NOR, Normal Drive	182	3-38
OR2	2 Input OR, Normal Drive	52	3-46
OR3	3 Input OR, Normal Drive	78	3-47
OR4	4 Input OR, Normal Drive	91	3-48
OR5	5 Input OR, Normal Drive	143	3-49
OR6	6 Input OR, Normal Drive	156	3-50
OR7	7 Input OR, Normal Drive	182	3-51
OR8	8 Input OR, Normal Drive	195	3-52
PADB	Address/Data Bus I/O Buffer		4-18
PCI	Non-Inverting CMOS Input Buffer, Normal Drive		3-172
PCIH	Non-Inverting CMOS Input Buffer, High Drive		3-172
PCIO	CMOS I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, 3.2 mA		3-201
PCNO	Non-Inverting CMOS Output Buffer, 3.2 mA		3-183
PCNO4	Non-Inverting CMOS Output Buffer, 15 mA		4-94
PCO	Inverting CMOS Output Buffer, 3.2 mA		3-182
PCOT	3-State Inverting CMOS Output Buffer, 3.2 mA		3-184
PCO2	Inverting CMOS Output Buffer, 16 mA		4-96
PCOT6	3-State Inverting CMOS Output Buffer with Enable, 42 mA		4-98
PISH	Non-Inverting TTL Schmitt Trigger Input Buffer, High Drive		3-178
PISRH	Non-Inverting TTL Schmitt Trigger Input Buffer with Pull-up Resistor, High Drive		3-180

Cell	Description	Grid Count	Page
POSC	Oscillator, Frequency Range to 16 MHz		4-16
POSC2	Oscillator, Frequency Range to 37.5 MHz		4-92
PRESET	Reset Input Buffer		4-14
PRGPIN	Programmable I/O Buffer		4-23
PTI	Non-Inverting TTL Input Buffer, Normal Drive		3-174
PTIH	Non-Inverting TTL Input Buffer, High Drive		3-174
PTIO	TTL I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, 3.2 mA Sink		3-203
PTIO3	TTL I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, 9.6 mA Sink		3-205
PTIO5	TTL I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, 16 mA Sink		3-207
PTIRH	Non-Inverting TTL Input Buffer with Pull-up Resistor, High Drive		3-176
PTND	Non-Inverting TTL Open-Drain Output Buffer, 3.2 mA Sink		3-198
PTND3	Non-Inverting TTL Open-Drain Output Buffer, 9.6 mA Sink		3-199
PTND5	Non-Inverting TTL Open-Drain Output Buffer, 16 mA Sink		3-200
PTNO	Non-Inverting TTL Output Buffer, 3.2 mA Sink		3-187
PTNO3	Non-Inverting TTL Output Buffer, 9.6 mA Sink		3-188
PTNO5	Non-Inverting TTL Output Buffer, 16 mA Sink		3-190
PTNQB	Quasi-Bidirectional I/O Buffer		4-20
PTO	Inverting TTL Output Buffer, 3.2 mA Sink		3-186
PTOT	3-State Inverting TTL Output Buffer, 3.2 mA Sink		3-192
PTOT3	3-State Inverting TTL Output Buffer, 9.6 mA Sink		3-194
PTOT5	3-State Inverting TTL Output Buffer, 16 mA Sink		3-196
RAM64	64 × 8 Static Random Access Memory		4-100
RAM128	128 × 8 Static Random Access Memory		4-105
RAM256	256 × 8 Static Random Access Memory		4-110
RAM512	512 × 8 Static Random Access Memory		4-115
RAM1K	1024 × 8 Static Random Access Memory		4-121
REGB	Telescoping Register Body	221	3-107
REGBT	Telescoping 3-State Register Body	234	3-114
REGC	Telescoping Register Control	117	3-105
REGCT	Telescoping 3-State Register Control	156	3-112
SHLB	Telescoping Shift Register with Load, Body	312	3-129
SHLC	Telescoping Shift Register with Load, Control	156	3-127
SHRB	Telescoping Shift Register Body	221	3-122
SHRC	Telescoping Shift Register Control	130	3-120
SP82284	80286 Clock Generator and Ready Interface		4-73
SP82288	80286 Bus Controller		4-80
SP8237	Programmable DMA Controller		4-25
SP8254	Programmable Interval Timer		4-41
SP8259	Programmable Interrupt Controller		4-49
SP8284	8086/8088 Clock Generator and Driver		4-57
SP8288	8086/8088 Bus Controller		4-64
UC5100	80C51BH Microcontroller Core with No ROM		4-1
UC5104	80C51BH Microcontroller Core with 4K Bytes ROM		4-1
UC5108	80C51BH Microcontroller Core with 8K Bytes ROM		4-1
UC5116	80C51BH Microcontroller Core with 16K Bytes ROM		4-1

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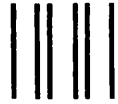

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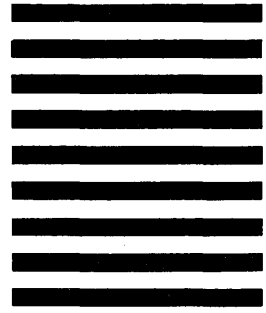

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Suite 340
Orlando 32822
Tel: (305) 240-8000
FAX: 305-240-8097

†Intel Corp.
11300 4th Street North
Suite 170
St. Petersburg 33716
Tel: (813) 577-2413
FAX: 813-578-1607

GEORGIA

†Intel Corp.
3280 Pointe Parkway
Suite 200
Norcross 30092
Tel: (404) 449-0541

ILLINOIS

Intel Corp.*
300 N. Martingale Road, Suite 400
Schaumburg 60173
Tel: (312) 310-8031

INDIANA

†Intel Corp.
8777 Purdue Road
Suite 125
Indianapolis 46268
Tel: (317) 875-0623

IOWA

Intel Corp.
1930 St. Andrews Drive N.E.
2nd Floor
Cedar Rapids 52402
Tel: (319) 393-5510

KANSAS

†Intel Corp.
8400 W. 110th Street
Suite 170
Overland Park 66210
Tel: (913) 345-2727

MARYLAND

Intel Corp.*
7321 Parkway Drive South
Suite C
Hanover 21076
Tel: (301) 796-7500
TWX: 710-862-1944

Intel Corp.
7833 Walker Drive
Suite 550
Greenbelt 20770
Tel: (301) 441-1020

MASSACHUSETTS

†Intel Corp.*
Westford Corp. Center
3 Carlisle Road
2nd Floor
Westford 01886
Tel: (617) 692-3222
TWX: 710-343-6333

MICHIGAN

†Intel Corp.
7071 Orchard Lake Road
Suite 100
West Bloomfield 48033
Tel: (313) 851-8096

MINNESOTA

Intel Corp.
3500 W. 80th St., Suite 360
Bloomington 55431
Tel: (612) 835-6722
TWX: 910-576-2867

MISSOURI

Intel Corp.
4203 Earth City Expressway
Suite 131
Earth City 63045
Tel: (314) 291-1990

NEW JERSEY

†Intel Corp.*
Parkway 109 Office Center
328 Newman Springs Road
Red Bank 07701
Tel: (201) 747-2233

†Intel Corp.
280 Corporate Center
75 Livingston Avenue
First Floor
Roseland 07068
Tel: (201) 740-0111
FAX: 201-740-0626

NEW MEXICO

†Intel Corp.
8500 Menaul Boulevard N.E.
Suite B 295
Albuquerque 87112
Tel: (505) 292-8086

NEW YORK

Intel Corp.
127 Main Street
Binghamton 13905
Tel: (607) 773-0337
FAX: 607-723-2677

†Intel Corp.*
850 Cross Keys Office Park
Fairport 14450
Tel: (716) 425-2750
TWX: 510-253-7391

†Intel Corp.*
300 Motor Parkway
Hauppauge 11787
Tel: (516) 231-3300
TWX: 510-227-6236

†Intel Corp.
15 Myers Corner Road
Suite 28
Hollowbrook Park
Wappinger Falls 12590
Tel: (914) 297-6161
TWX: 510-248-0060

NORTH CAROLINA

Intel Corp.
5700 Executive Drive
Suite 213
Charlotte 28212
Tel: (704) 568-8966

†Intel Corp.
2700 Wycliff Road
Suite 102
Raleigh 27607
Tel: (919) 781-8022

OHIO

Intel Corp.*
3401 Park Center Drive
Suite 220
Dayton 45414
Tel: (513) 890-5350
TWX: 810-450-2528

Intel Corp.*
25700 Science Park Dr., Suite 100
Beachwood 44122
Tel: (216) 464-2736
TWX: 810-427-9298

OKLAHOMA

Intel Corp.
6801 N. Broadway
Suite 115
Oklahoma City 73162
Tel: (405) 848-8086

OREGON

†Intel Corp.
15254 N.W. Greenbrier Parkway, Bldg. B
Beaverton 97006
Tel: (503) 645-8051
TWX: 910-467-8741

PENNSYLVANIA

Intel Corp.*
455 Pennsylvania Avenue
Suite 230
Fort Washington 19034
Tel: (215) 641-1000
TWX: 510-661-2077

Intel Corp.*
400 Penn Center Blvd., Suite 610
Pittsburgh 15235
Tel: (412) 823-4970

PUERTO RICO

Intel Microprocessor Corp.
South Industrial Park
P.O. Box 910
Las Piedras 00671
Tel: (809) 733-8616

TEXAS

†Intel Corp.
313 E. Anderson Lane
Suite 314
Austin 78752
Tel: (512) 454-3628

†Intel Corp.*
12000 Ford Road
Suite 400
Dallas 75234
Tel: (214) 241-8087
FAX: 214-484-1180

Intel Corp.*
7322 S.W. Freeway
Suite 1490
Houston 77074
Tel: (713) 988-8086
TWX: 910-881-2490

UTAH

Intel Corp.
5201 Green Street
Suite 290
Murray 84123
Tel: (801) 263-8051

VIRGINIA

†Intel Corp.
1504 Santa Rosa Road
Suite 108
Richmond 23288
Tel: (804) 282-5668

WASHINGTON

Intel Corp.
155 108th Avenue N.E.
Suite 386
Bellevue 98004
Tel: (206) 453-8086
TWX: 910-443-3002

Intel Corp.
408 N. Mullan Road
Suite 102
Spokane 99206
Tel: (509) 928-8086

WISCONSIN

†Intel Corp.
330 S. Executive Dr.
Suite 102
Brookfield 53005
Tel: (414) 784-8087
FAX: (414) 796-2115

CANADA

BRITISH COLUMBIA

Intel Semiconductor of Canada, Ltd.
4585 Canada Way, Suite 202
Burnaby V5G 4L6
Tel: (604) 298-0387
FAX: (604) 298-8234

ONTARIO

†Intel Semiconductor of Canada, Ltd.
2650 Queensview Drive
Suite 250
Ottawa K2B 8H6
Tel: (613) 829-9714
TLX: 053-4115

†Intel Semiconductor of Canada, Ltd.
190 Attwell Drive
Suite 500
Rexdale M9W 6H8
Tel: (416) 675-2105
TLX: 06983574
FAX: (416) 675-2438

QUEBEC

†Intel Semiconductor of Canada, Ltd.
620 St. John Boulevard
Pointe Claire H9R 3K2
Tel: (514) 694-9130
TWX: 514-694-9134

†Sales and Service Office
*Field Application Location

DOMESTIC DISTRIBUTORS

ALABAMA

Arrow Electronics, Inc.
1015 Henderson Road
Huntsville 35816
Tel: (205) 837-6955

†Hamilton/Avnet Electronics
4940 Research Drive
Huntsville 35805
Tel: (205) 837-7210
TWX: 810-726-2162

Pioneer/Technologies Group Inc.
4825 University Square
Huntsville 35816
Tel: (205) 837-9300
TWX: 810-726-2197

ARIZONA

†Hamilton/Avnet Electronics
505 S. Madison Drive
Tempe 85281
Tel: (602) 968-1461
TWX: 910-950-0077

Kierulff Electronics, Inc.
4134 E. Wood Street
Phoenix 85040
Tel: (602) 437-0750
FAX: 602-252-9109

Wyle Distribution Group
17855 N. Black Canyon Highway
Phoenix 85023
Tel: (602) 866-2888
FAX: 602-866-6937

CALIFORNIA

Arrow Electronics, Inc.
19748 Dearborn Street
Chatsworth 91311
Tel: (818) 701-7500
FAX: 818-772-8930

Arrow Electronics, Inc.
9511 Ridgehaven Court
San Diego 92123
Tel: (619) 565-4800
FAX: 619-279-0862

†Arrow Electronics, Inc.
521 Weddell Drive
Sunnyvale 94089
Tel: (408) 745-6600
FAX: 408-743-4770

Arrow Electronics, Inc.
2961 Dow Avenue
Tustin 92680
Tel: (714) 838-5422
FAX: 714-838-4151

†Avnet Electronics
350 McCormick Avenue
Costa Mesa 92626
Tel: (714) 754-6051
FAX: 714-754-6007

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale 94089
Tel: (408) 743-3300
FAX: 408-745-6679

†Hamilton/Avnet Electronics
4545 Viewridge Avenue
San Diego 92123
Tel: (619) 571-7500
FAX: 619-277-6136

†Hamilton/Avnet Electronics
9650 Desoto Ave.
Chatsworth 91311
Tel: (818) 700-1222, 6500
FAX: 818-700-6553

†Hamilton/Avnet Electronics
4103 Northgate Boulevard
Sacramento 95834
Tel: (916) 920-3150
FAX: 916-925-3478

†Hamilton/Avnet Electronics
3002 G Street
Ontario 91311
Tel: (714) 989-9411
FAX: 714-980-7129

†Hamilton/Avnet Electronics
10950 W. Washington Blvd.
Culver City 90230
Tel: (213) 558-2458
FAX: 213-558-2248

†Hamilton Electro Sales
3170 Pullman Street
Costa Mesa 92626
Tel: (714) 641-4150
FAX: 714-641-4122

CALIFORNIA (Cont'd.)

Kierulff Electronics, Inc.
10824 Hope Street
Cypress 90430
Tel: (714) 220-6300
FAX: 714-821-8420

†Kierulff Electronics, Inc.
1180 Murphy Avenue
San Jose 95131
Tel: (408) 971-2600
FAX: 408-947-3432

†Kierulff Electronics, Inc.
14242 Chamber Rd.
Tustin 92680
Tel: (714) 731-5711
FAX: 714-669-4235

†Kierulff Electronics, Inc.
9800 Variel St.
Chattsworth 91311
Tel: (213) 725-0325
FAX: 818-407-0803

Wyle Distribution Group
26677 W. Agoura Rd.
Calabasas 91302
Tel: (818) 880-9000
FAX: 818-880-5510

†Wyle Distribution Group
17872 Cowan Avenue
Irvine 92714
Tel: (714) 863-9953
FAX: 714-863-0473

Wyle Distribution Group
11151 Sun Center Drive
Rancho Cordova 95670
Tel: (916) 638-5282
FAX: 916-638-1491

†Wyle Distribution Group
9525 Chesapeake Drive
San Diego 92123
Tel: (619) 565-9171
TWX: 910-371-9592
FAX: 619-565-9171 ext. 274

†Wyle Distribution Group
3000 Bowers Avenue
Santa Clara 95051
Tel: (408) 727-2500
FAX: 408-727-5896

Wyle Military
18910 Teller Avenue
Irvine 92715
Tel: (714) 851-9958
TWX: 910-371-9127
FAX: 714-851-8366

Wyle Systems
7382 Lampson Avenue
Garden Grove 92641
Tel: (714) 891-1717
FAX: 714-895-9038

COLORADO

Arrow Electronics, Inc.
1390 S. Potomac Street
Suite 136
Aurora 80012
Tel: (303) 696-1111

†Hamilton/Avnet Electronics
8765 E. Orchard Road
Suite 708
Englewood 80111
Tel: (303) 740-1017
TWX: 910-935-0787

†Wyle Distribution Group
451 E. 124th Avenue
Thornton 80241
Tel: (303) 457-9953
TWX: 910-936-0770

CONNECTICUT

†Arrow Electronics, Inc.
12 Beaumont Road
Wallingford 06492
Tel: (203) 265-7741
TWX: 710-476-0162

Hamilton/Avnet Electronics
Commerce Industrial Park
Commerce Drive
Danbury 06810
Tel: (203) 797-2800
FAX: 203-797-2866

†Pioneer Northeast Electronics
112 Main Street
Norwalk 06851
Tel: (203) 853-1515
TWX: 710-468-3373

FLORIDA

†Arrow Electronics, Inc.
350 Fairway Drive
Deerfield Beach 33441
Tel: (305) 429-8200
TWX: 510-955-9456

Arrow Electronics, Inc.
1001 N.W. 62nd St., Ste. 108
Ft. Lauderdale 33309
Tel: (305) 475-4297
TWX: 510-955-9456

†Arrow Electronics, Inc.
1530 Bottlebrush N.E.
Palm Bay 32905
Tel: (305) 725-1480

†Hamilton/Avnet Electronics
6801 N.W. 15th Way
Ft. Lauderdale 33309
Tel: (305) 971-2900
TLX: 510-956-3097

Hamilton/Avnet Electronics
3245 Tech Drive North
St. Petersburg 33702
Tel: (813) 576-3930
TWX: 810-863-0374

Hamilton/Avnet Electronics
6947 University Boulevard
Winterpark 32792
Tel: (305) 628-3888
FAX: 305-628-3888 ext. 40

†Pioneer Electronics
337 N. Lake Blvd., Ste. 1000
Alta Monte Springs 32701
Tel: (305) 834-9090
TWX: 810-853-0284

Pioneer Electronics
674 S. Military Trail
Deerfield Beach 33442
Tel: (305) 428-8877
TWX: 510-955-9653

GEORGIA

†Arrow Electronics, Inc.
3155 Northwoods Parkway
Suite A
Norcross 30071
Tel: (404) 449-8252
FAX: 404-242-6827

Hamilton/Avnet Electronics
5825 D. Peachtree Corners East
Norcross 30092
Tel: (404) 447-7500
TWX: 810-766-0432

Pioneer Electronics
3100 F. Northwoods Place
Norcross 30071
Tel: (404) 448-1711
FAX: 404-446-8270

ILLINOIS

†Arrow Electronics, Inc.
2000 E. Alonquin Street
Schaumberg 60173
Tel: (312) 397-3440
FAX: 312-397-3550

†Hamilton/Avnet Electronics
1130 Thorndale Avenue
Bensenville 60106
Tel: (312) 860-7780
TWX: 910-227-0060

Kierulff Electronics, Inc.
1140 W. Thorndale
Itasca 60143
Tel: (312) 250-0500
FAX: 312-250-0916

MTI Systems Sales
1100 West Thorndale
Itasca 60143
Tel: (312) 773-2300

†Pioneer Electronics
1551 Carmen Drive
Elk Grove Village 60007
Tel: (312) 437-9680
TWX: 910-222-1834

INDIANA

†Arrow Electronics, Inc.
2495 Directors Row, Suite H
Indianapolis 46241
Tel: (317) 243-9353
TWX: 810-341-3119

INDIANA (Cont'd.)

Hamilton/Avnet Electronics
485 Gradle Drive
Carmel 46032
Tel: (317) 844-9333
FAX: 317-844-5921

†Pioneer Electronics
6408 Castleplace Drive
Indianapolis 46250
Tel: (317) 849-7300
TWX: 810-260-1794

KANSAS

†Hamilton/Avnet Electronics
9219 Quivera Road
Overland Park 66215
Tel: (913) 888-8900
FAX: 913-541-7951

Pioneer Electronics
10551 Lackman Rd.
Lenexa 66215
Tel: (913) 492-0500
FAX: 913-492-7832

KENTUCKY

Hamilton/Avnet Electronics
805-A Newtown Circle
Lexington 40511
Tel: (606) 259-1475
FAX: 606-252-3238

MARYLAND

Arrow Electronics, Inc.
8300 Guilford Road, Ste. H
Rivers Center
Columbia 21046
Tel: (301) 995-6002
TWX: 710-236-9005
FAX: 301-381-3854

†Hamilton/Avnet Electronics
6822 Oak Hall Lane
Columbia 21045
Tel: (301) 995-3500
FAX: 301-995-3593

†Mesa Technology Corp.
9720 Patuxent Woods Dr.
Columbia 21046
Tel: (301) 720-5020
TWX: 710-828-9702

†Pioneer Electronics
9100 Gaither Road
Gaithersburg 20877
Tel: (301) 921-0660
TWX: 710-828-0545

MASSACHUSETTS

†Arrow Electronics, Inc.
1 Arrow Drive
Woburn 01801
Tel: (617) 933-8130
TWX: 710-393-6770

†Hamilton/Avnet Electronics
10D Centennial Drive
Peabody 01960
Tel: (617) 532-3701
TWX: 710-393-0382

Kierulff Electronics, Inc.
13 Fortune Dr.
Billerica 01821
Tel: (617) 667-8331
TWX: 710-390-1449
FAX: 617-663-1754

Pioneer Northeast Electronics
44 Hartwell Avenue
Lexington 02173
Tel: (617) 861-9200
FAX: 617-863-1547

MICHIGAN

Arrow Electronics, Inc.
755 Phoenix Drive
Ann Arbor 48108
Tel: (313) 971-8220
FAX: 313-971-2633

†Hamilton/Avnet Electronics
32487 Schoolcraft Road
Livonia 48150
Tel: (313) 522-4700
TWX: 810-242-8775
FAX: 313-522-2624

Hamilton/Avnet Electronics
2215 29th Street S.E.
Space A5
Grand Rapids 49508
Tel: (616) 243-8805
TWX: 810-273-6921
FAX: 616-243-0028

MICHIGAN (Cont'd.)

Pioneer Electronics
4505 Broadmoor Ave. S.E.
Grand Rapids 49508
Tel: (616) 698-1800
FAX: 616-698-1831

†Pioneer Electronics
13485 Stamford
Livonia 48150
Tel: (313) 525-1800
TWX: 810-242-3271

MINNESOTA

†Arrow Electronics, Inc.
5230 W. 73rd Street
Edina 55435
Tel: (612) 830-1800
FAX: 612-830-1856

Hamilton/Avnet Electronics
12400 White Water Drive
Minnetonka 55343
Tel: (612) 932-0600
FAX: 612-932-0613

†Pioneer Electronics
10203 Bren Road East
Minnetonka 55343
Tel: (612) 935-5444
FAX: 612-935-1921

MISSOURI

†Arrow Electronics, Inc.
2380 Schuetz
St. Louis 63146
Tel: (314) 567-6888
FAX: 314-567-1164

†Hamilton/Avnet Electronics
13743 Shoreline Court East
Earth City 63045
Tel: (314) 344-1200
FAX: 314-291-8889

Kierulff Electronics, Inc.
11804 Borman Dr.
St. Louis 63146
Tel: (314) 997-4956
FAX: 314-567-0860

NEW HAMPSHIRE

†Arrow Electronics, Inc.
3 Perimeter Road
Manchester 03103
Tel: (603) 668-6968
FAX: 603-668-3484

Hamilton/Avnet Electronics
444 E. Industrial Drive
Manchester 03103
Tel: (603) 624-9400
FAX: 603-624-2402

NEW JERSEY

†Arrow Electronics, Inc.
6000 Lincoln Drive East
Marlton 08053
Tel: (609) 596-8000
FAX: 609-596-5632

†Arrow Electronics, Inc.
6 Century Drive
Parsipanny 07054
Tel: (201) 538-0900
FAX: 201-538-4962

†Hamilton/Avnet Electronics
1 Keystone Ave., Bldg. 36
Cherry Hill 08003
Tel: (609) 424-0110
TWX: 710-940-0262
FAX: 609-751-8624

†Hamilton/Avnet Electronics
10 Industrial
Fairfield 07006
Tel: (201) 575-3390
FAX: 201-575-5839

†Pioneer Northeast Electronics
45 Route 46
Pinebrook 07058
Tel: (201) 575-3510
FAX: 201-575-3454

†MTI Systems Sales
37 Kulick Rd.
Fairfield 07006
Tel: (201) 227-5552
FAX: 201-575-6336

†Microcomputer System Technical Distributor Centers

DOMESTIC DISTRIBUTORS

NEW MEXICO

Alliance Electronics Inc.
11030 Cochiti S.E.
Albuquerque 87123
Tel: (505) 292-3360
FAX: 505-292-6537

Hamilton/Avnet Electronics
2524 Baylor Drive S.E.
Albuquerque 87106
Tel: (505) 765-1500
FAX: 505-243-1395

NEW YORK

Arrow Electronics, Inc.
25 Hub Drive
Melville 11747
Tel: (516) 694-6800
TWX: 510-224-6126
FAX: 516-391-1401

†Arrow Electronics, Inc.
3375 Brighton-Henrietta Townline Rd.
Rochester 14623
Tel: (716) 427-0300
FAX: 716-427-0735

Arrow Electronics, Inc.
20 Oser Avenue
Hauppauge 11788
Tel: (516) 231-1000
FAX: 516-231-1072

Hamilton/Avnet Electronics
2060 Townline Rd.
Rochester 14623
Tel: (716) 475-9130
FAX: 716-475-9119

†Hamilton/Avnet Electronics
103 Twin Oaks Drive
Syracuse 13206
Tel: (315) 437-2641
FAX: 315-432-0740

†Hamilton/Avnet Electronics
933 Motor Parkway
Hauppauge 11788
Tel: (516) 231-9800
FAX: 516-434-7426

†MTI Systems Sales
38 Harbor Park Drive
P.O. Box 271
Port Washington 11050
Tel: (516) 621-6200
FAX: 516-625-3039

†Pioneer Northeast Electronics
68 Corporate Dr.
Binghamton 13904
Tel: (607) 722-9300
FAX: 607-722-9562

†Pioneer Northeast Electronics
60 Crossway Park West
Woodbury, Long Island 11797
Tel: (516) 921-8700
TWX: 510-221-2184
FAX: 516-921-2143

†Pioneer Northeast Electronics
840 Fairport Park
Fairport 14450
Tel: (716) 381-7070
FAX: 716-381-5955

NORTH CAROLINA

†Arrow Electronics, Inc.
5240 Greens Dairy Road
Raleigh 27604
Tel: (919) 876-3132
FAX: 919-876-3132, ext. 200

†Hamilton/Avnet Electronics
3510 Spring Forest Drive
Raleigh 27609
Tel: (919) 878-0819
TWX: 510-928-1836

NORTH CAROLINA (Cont'd.)

Pioneer Electronics
9801 A-Southern Pine Blvd.
Charlotte 28217
Tel: (704) 527-8188
TWX: 810-621-0366

OHIO

Arrow Electronics, Inc.
7620 McEwen Road
Centerville 45459
Tel: (513) 435-5563
FAX: 513-435-2049

†Arrow Electronics, Inc.
6238 Cochran Road
Solon 44139
Tel: (216) 248-3990
FAX: 216-248-1106

Hamilton/Avnet Electronics
777 Brooksedge Blvd.
Westerville 43081
Tel: (614) 882-7004
FAX: 614-882-8650

†Hamilton/Avnet Electronics
954 Senate Drive
Dayton 45459
Tel: (513) 439-6700
FAX: 513-439-6711

†Hamilton/Avnet Electronics
30325 Bainbridge Rd., Bldg. A
Solon 44139
Tel: (216) 349-5100
FAX: 216-349-1894

†Pioneer Electronics
4433 Interpoint Blvd.
Dayton 45424
Tel: (513) 236-9900
FAX: 513-236-8133

†Pioneer Electronics
4800 E. 131st Street
Cleveland 44105
Tel: (216) 587-3600
TWX: 810-422-2211
FAX: 216-587-3906

OKLAHOMA

Arrow Electronics, Inc.
3158 S. 108 East Ave., Ste. 210
Tulsa 74146
Tel: (918) 665-7700
FAX: 918-665-7700

OREGON

†Almac Electronics Corp.
1885 N.W. 169th Place
Beaverton 97006
Tel: (503) 629-8090
FAX: 503-645-0611

†Hamilton/Avnet Electronics
6024 S.W. Jean Road
Bldg. C, Suite 10
Lake Oswego 97034
Tel: (503) 635-7848
FAX: 503-636-1327

Wyle Distribution Group
5250 N.E. Elam Young Parkway
Suite 600
Hillsboro 97124
Tel: (503) 640-6000
FAX: 503-640-5846

PENNSYLVANIA

Arrow Electronics, Inc.
650 Seco Road
Monroeville 15146
Tel: (412) 856-7000
FAX: 412-856-5777

Hamilton/Avnet Electronics
2800 Liberty Ave., Bldg. E
Pittsburgh 15222
Tel: (412) 281-4150
FAX: 412-281-8662

PENNSYLVANIA (Cont'd.)

Pioneer Electronics
259 Kappa Drive
Pittsburgh 15238
Tel: (412) 782-2300
TWX: 710-795-3122
FAX: 412-963-8255

†Pioneer Electronics
261 Gibralter Road
Horsham 19044
Tel: (215) 674-4000
TWX: 510-665-6778
FAX: 215-674-3107

TEXAS

†Arrow Electronics, Inc.
3220 Commander Drive
Carrollton 75006
Tel: (214) 380-6464
FAX: 214-248-7208

†Arrow Electronics, Inc.
10899 Kinghurst Dr.
Suite 100
Houston 77099
Tel: (713) 530-4700
FAX: 713-568-8518

†Arrow Electronics, Inc.
2227 W. Braker Lane
Austin 78758
Tel: (512) 835-4180
FAX: 512-832-9875

†Hamilton/Avnet Electronics
1807A W. Braker Lane
Austin 78758
Tel: (512) 837-8911
FAX: 512-339-6232

†Hamilton/Avnet Electronics
2111 W. Walnut Hill Lane
Irving 75038
Tel: (214) 550-6111
FAX: 214-550-8172

†Hamilton/Avnet Electronics
4850 Wright Road, Ste. 190
Stafford 77477
Tel: (713) 240-7733
FAX: 713-240-0582

Kierulff Electronics, Inc.
2010 Merritt Dr.
Garland 75040
Tel: (214) 840-0110
FAX: 214-278-0928

†Pioneer Electronics
1826-D Kramer Lane
Austin 78758
Tel: (512) 835-4000
FAX: 512-835-9829

†Pioneer Electronics
13710 Omega Road
Dallas 75244
Tel: (214) 386-7300
FAX: 214-490-6419

†Pioneer Electronics
5853 Point West Drive
Houston 77036
Tel: (713) 988-5555
FAX: 713-988-1732

UTAH

†Hamilton/Avnet Electronics
1585 West 2100 South
Salt Lake City 84119
Tel: (801) 972-2800
FAX: 801-974-9675

Kierulff Electronics, Inc.
1946 W. Parkway Blvd.
Salt Lake City 84119
Tel: (801) 973-6913
FAX: 801-972-0200

Wyle Distribution Group
1325 West 2200 South
Suite E
Salt Lake City 84119
Tel: (801) 974-9953
FAX: 801-972-2524

WASHINGTON

†Almac Electronics Corp.
14360 S.E. Eastgate Way
Bellevue 98007
Tel: (206) 643-9992
FAX: 206-643-9709

Arrow Electronics, Inc.
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Bellevue 98007
Tel: (206) 643-4800
FAX: 206-746-3740

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CANADA

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2816 21st Street N.E.
Calgary T2E 6Z2
Tel: (403) 250-9380
FAX: 403-250-1591

Zentronics
6815 8th Street, N.E., Ste. 100
Calgary T2E 7H7
Tel: (403) 295-8838
FAX: 403-295-8714

BRITISH COLUMBIA

Hamilton/Avnet Electronics
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MANITOBA

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FAX: 416-677-0627

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Tel: (418) 687-4231
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St. Laurent H4S 1P8
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Tel: +46 8 734 01 00
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1120 Brussel
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Tel: 45 (0) 2 45 66 45
TLX: 33 355

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Tel: (1) 47 90 62 40
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Tel: (1) 45 34 75 35
TLX: 204552

WEST GERMANY

Electronic 2000 Vertriebs-AG
Stahlgruberring 12
8000 Muenchen 82
Tel: (089) 42 00 10
TLX: 522551

ITT Multikomponent GmbH
Bahnhofstrasse 44
7141 Moeglingen
Tel: (071) 41 48 79
TLX: 7264399

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6250 Limburg
Tel: (064) 31 50 80
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Viale Fulvio Testi 126
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Milano
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2627 AP Delft
Tel: (015) 60 99 06
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NORWAY

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P.O. Box 122
Smedsvingen 4
1364 Hvalstad
Tel: (2) 84 62 10
TLX: 77546

PORTUGAL

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TLX: 14182

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ATD Electronica S.A.
Plaza Ciudad de Viena no. 6
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Tel: (1) 234 40 00
TLX: 42477

ITT-SESA
Calle Miguel Angel no. 21-3
28010 Madrid
Tel: (1) 419 09 57
TLX: 27461

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Nordisk Elektronik A.B.
Huvudstagatan 1
P.O. Box 1409
17127 Solna
Tel: (8) 734 97 70
TLX: 10547

SWITZERLAND

Industrade A.G.
Hertistrasse 31
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Tel: (01) 8 30 50 40
TLX: 56788

UNITED KINGDOM

Accent Electronic Components Ltd.
Jubilee House, Jubilee Way
Letchworth, Herts SG6 1QH
Tel: (0462) 68 66 66
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Bytech Comway Ltd.
Unit 2 The Western Centre
Western Road
Bracknell
Berks RG12 1RW
Tel: (0344) 48 22 11
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Rapid Silicon
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Denmark St.
High Wycombe
Bucks HP11 2ER
Tel: (0494) 44 22 66
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Rapid Systems
Rapid House
Denmark St.
High Wycombe
Bucks HP11 2ER
Tel: (0494) 45 02 44
TLX: 837931

YUGOSLAVIA

H.R. Microelectronics Corp.
2005 de la Cruz Blvd., Ste. 223
Santa Clara, CA 95050
U.S.A.
Tel: (408) 988-0286
TLX: 387452

*Field Application Location

CG-1/18/88

INTERNATIONAL SALES OFFICES

AUSTRALIA

Intel Australia Pty. Ltd.*
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Crows Nest, NSW, 2065
Tel: (2) 957-2744
TLX: 20097
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Intel PRC Corporation
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FAX: 250-9256

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Arun Complex
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TLX: 0845-8332 MD BG IN

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*Field Application Location

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Suite 340
Orlando 32822
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3280 Pointe Parkway
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Norcross 30092
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Tel: (201) 225-3000

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Tel: (919) 294-1541

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28001 Chagrin Boulevard
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Tel: (216) 464-6915
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Dayton 45414
Tel: (513) 890-5350

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Tel: (503) 645-8051
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Hillsboro 97123
Tel: (503) 681-8080

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Intel Corp.
201 Penn Center Boulevard
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Tel: (313) 354-1540

TEXAS

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Suite 314
Austin 78752
Tel: (512) 454-3628
TWX: 910-874-1347

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12000 Ford Road
Suite 400
Dallas 75234
Tel: (214) 241-8087
FAX: 214-484-1180

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El Paso 79904
Tel: (915) 751-0186

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Suite 108
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Tel: (804) 282-5668

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Suite 510
Bellevue 98004
Tel: 1-800-468-3548
TWX: 910-443-3002

WISCONSIN

Intel Corp.
330 S. Executive Dr.
Suite 102
Brookfield 53005
Tel: (414) 784-8087

CANADA

Intel Semiconductor of Canada, Ltd.
190 Attwell Drive, Suite 500
Rexdale, Ontario
Canada M9W 6H8
Tel: (416) 675-2105

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620 St. John Blvd.
Pointe Claire, Quebec
Canada H9R 3K2
Tel: (514) 694-9130

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Ottawa, Ontario
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Intel Semiconductor GmbH
Seidlstrasse 27
D-8000 Muenchen 2

HONG KONG
Intel Semiconductor Ltd.
1701-3 Connaught Centre
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Printed in USA/0188/A7-415/10K/RRD RM
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