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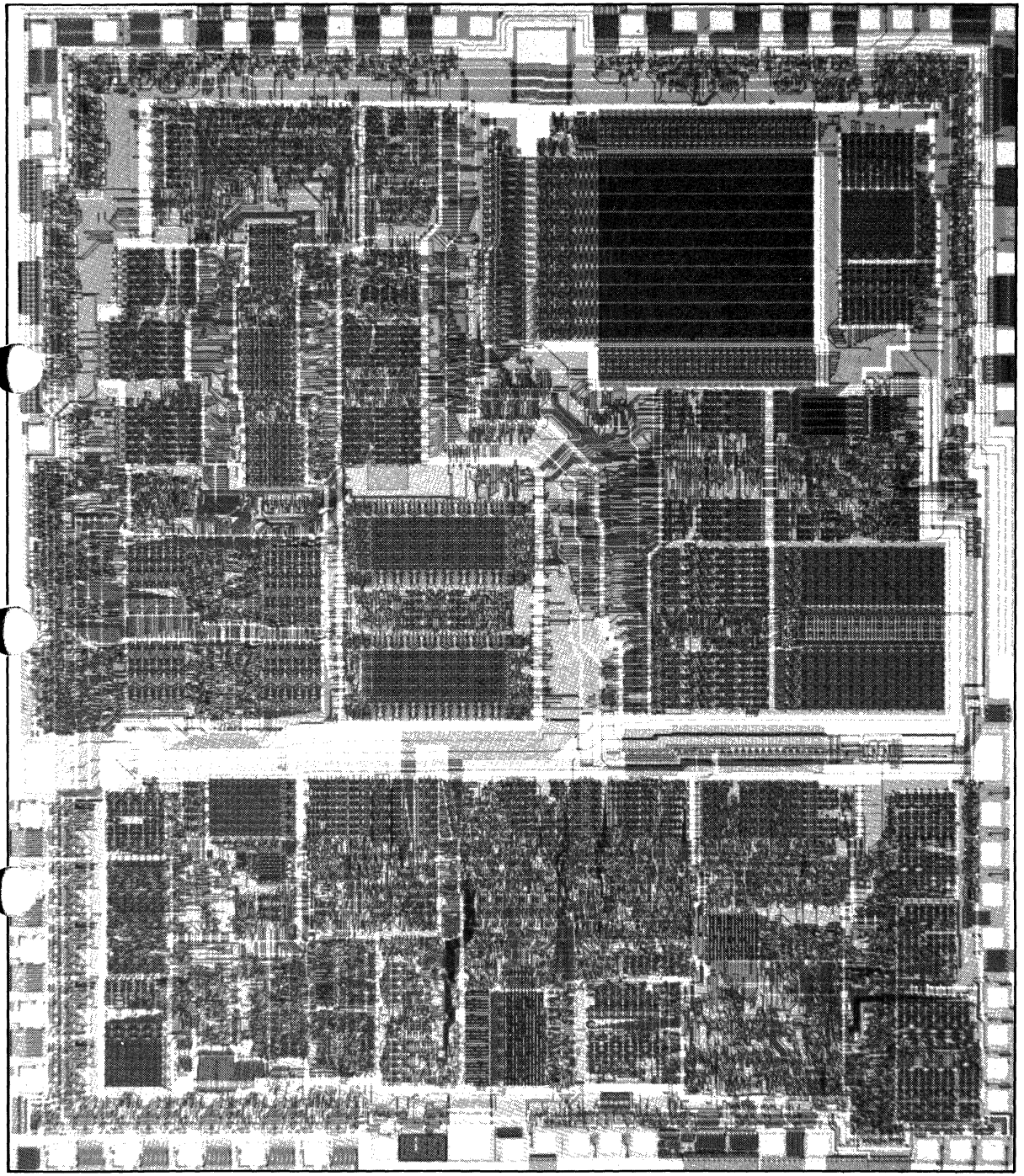
82586 Reference Manual

ADVANCE INFORMATION



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82586 REFERENCE MANUAL

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INTRODUCTION

The 82586 is an intelligent, high performance Local Communications Controller (LCC). It is designed to relieve a host CPU of many of the tasks associated with controlling local networks and serial backplanes. Because the 82586 integrates many of the functions required to implement a local network into a single LSI component, the cost and complexity of the communication interface is dramatically reduced.

The 82586 provides most of the functions normally associatd with the data link and physical link layers of a local network architecture. In particular, it performs framing (frame boundary delineation, addressing, and bit error detection), link management, and data modulation It also supports a network management interface.

The framing functions on the 82586 are very flexible and permit a variety of different techniques to be specified in addition to Ethernet. The boundaries of a frame may be specified by either flags/bitstuffing or an end-of-carrier techniques. Addressing features include support of a very large address space with single node, multicast, and broadcast capability. Bit error detection is performed by use of either the CCITT V.41 CRC polynomial or the Autodin-II 32 bit polynomial.

The 82586 has a memory based architecture in that the 82586 and CPU communicate entirely through a shared memory space. Transmit and receive data are located in data buffers of programmable length that can be chained together. Chaining of data buffers results in efficient use of system memory.

The 82586 features a high level diagnostic or maintenance, capability. The 82586 automatically gathers statistics on CRC errors, frame alignment errors, overrun errors, and frames lost because there was no resource to recieve them. In addition, the user can output the status of all internal registers to facilitate system design. An on-chip time domain reflectometer can be used to help locate cable faults.

This document provides the system designer with a detailed description of the 82586. It is assumed that the reader has familiarized himself with fundamental 82586/CPU system operation as described in the 82586 Data Sheet, "System-Level Functions Enhance Controller IC", Electronics, October 6, 1982 (Intel article reprint AR-237), and "2-Chip Controller Set Drives Ethernet Hookup Costs", Data Communications, October 1982 (Intel article reprint AR-244).

2.0 CONTROLLING THE 82586

2.1 OVERVIEW

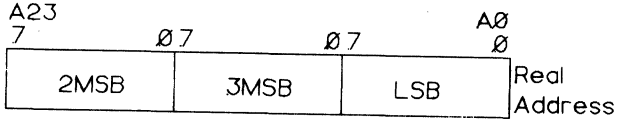
This section describes the commands, data structures, and techniques by which a host CPU controls and uses the 82586. The emphasis here is not on any particular action command (e.g. Transmit), but rather on how the 82586 is controlled. The 82586 consists of two major internal processors: the Command Unit (CU) and the Receive Unit (RU). The control that the CPU exercises over them is indirect. Each unit accepts CPU commands during a ready state, although they are almost always ready, there may be a delay if the unit is busy responding to another request (internally generated). Both units can be viewed as multitasked units with nonpreemptive scheduling (although buffer switching tasks preempt the RU and CU).

All control structures are memory resident and thus, all communication between the CPU and the 82586 takes place via shared memory structures. There is no I/O port access to the 82586. Please refer to the 82586 data sheet for a general description of 82586/CPU shared memory structure.

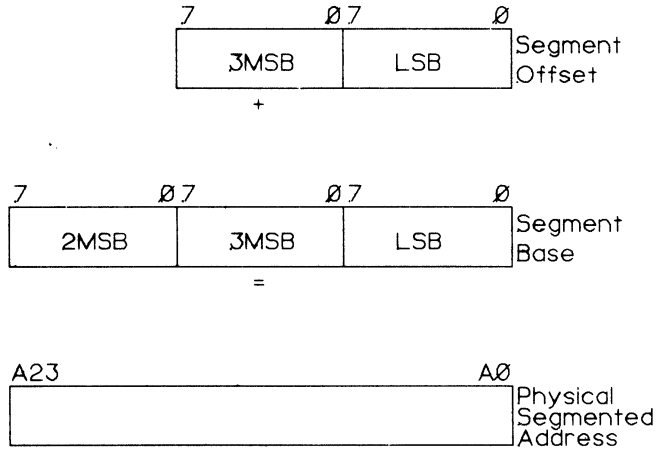
2.2 MEMORY ADDRESSING FORMATS

The 82586 accesses memory by 24-bit addresses. There are two types of 24-bit address: real addresses and segmented addresses. A real address is a single 24-bit entity. It is used primarily to address transmit and receive data buffers. The other form is a segmented address that uses a 24-bit base and a 16-bit offset. The segmented address form is used for all Command Blocks, Buffer Descriptors, Frame Descriptors and System Control Blocks. In general, only the offset portion of the addressed entity is specified in the block. The base for all offsets is the same (that of the SCB). The diagrams below detail the memory formats used. The 'LSB' is the least significant byte of the address, '3MSB' is the next most significant byte, '2MSB', if present, is the next most significant byte.

Physical (Real) data buffer addressing:



Command structure addressing:



2.3 THE SYSTEM CONTROL BLOCK (SCB)

The SCB is a memory block that is shared by the CPU and 82586, and thereby forms the communication link between the CPU and the 82586. Such communication involves:

* Issuing commands by the CPU.
* Reporting status by the 82586.

The CPU delivers Control commands to the 82586 by writing the commands into the SCB and asserting Channel Attention (CA). The 82586 will examine the command, perform whatever action is required, and clear the command. Control commands perform the following types of tasks:

* Controlling the operation of the Command Unit (CU).
* Controlling the reception of frames by the Receive Unit (RU).
* Acknowledging events that caused an interrupt.
* Resetting the chip.

The SCB controls the Command Unit by specifying the address of the Command Block List (CBL) and by starting, suspending, resuming or aborting execution of commands of the CBL. The SCB controls the Receive Unit by specifying the address of the Receive Frame Area (RFA), and by enabling, suspending, resuming or halting reception of frames.

The SCB is also used for reporting status to the host CPU. There are four types of status information contained in the SCB. The first describes the cause(s) of the currently pending interrupt (events). The second indicates the status of the Command Unit. The third indicates the status of the Receive Unit. The fourth contains statistics collected by the 82586 related to receive frames, found to be corrupted.

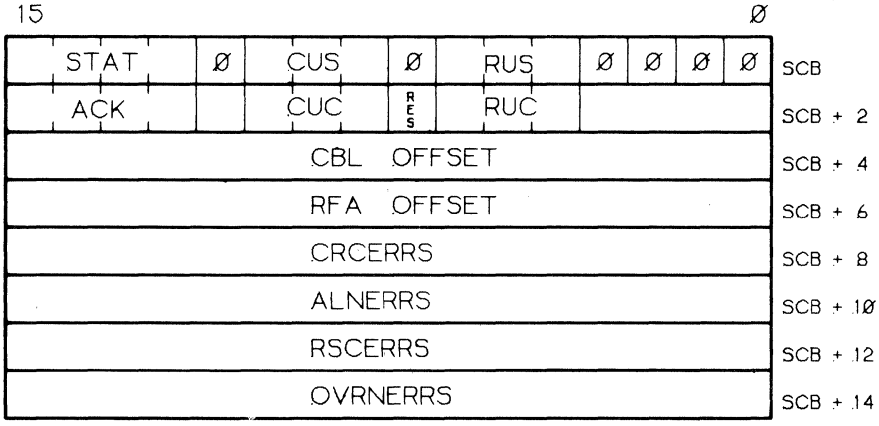
The status of four events saved by the 82586:

* The completion of an action command by the CU.
* The reception of a frame by the RU.
* The Command Unit becoming not ready.
* The Receive Unit becoming not ready.

The acknowledgement of events by the CPU is the only means by which they are cleared. Note that if not all events are acknowledged by the Channel Attention (CA), then the Interrupt (INT) signal will be re-issued after processing the CA. Also, if a new event occurs while the interrupt is set, the interrupt is momentarily cleared in order to trigger edge triggered interrupt controllers.

The CPU commands the 82586 to examine the SCB via the Channel Attention line. This signal is trailing edge triggered and is latched by the 82586. The latch is cleared by the 82586 as part of the SCB examination process, prior to reading the SCB.

The format of the SCB is:



STATUS -

Indicates the status of the 82586. This word is modified only by the 82586. Defined bits are:

Bit 15 CX - A command in the CBL having its 'I' (interrupt) bit set has been executed.

Bit 14 FR - A frame has been received.

Bit 13 CNR - The command unit became not ready.

Bit 12 RNR - The receive unit became not ready.

Bits 8-10 CUS - (3 bits) this field contains the status of the Command Unit.
Valid values are:

0 - Idle
1 - Suspended
2 - Ready
3-7 - Not used

Bits 4-6 RUS - (3 bits) this field contains the status of the Receive Unit. Valid values are:

0 - Idle
1 - Suspended
2 - No Resources
3 - Not used
4 - Ready
5-7 - Not used

COMMAND -

Specifies the action to be performed as a result of the CA. This word is set by the CPU and cleared by the 82586. Defined bits are :

Bit 15 ACK-CX - Acknowledges the command executed event.

Bit 14 ACK-FR - Acknowledges the frame received event.

Bit 13 ACK-CNR - Acknowledges that the Command Unit became not ready.

Bit 12 ACK-RNR - Acknowledges that the Receive Unit became not ready.

Bits 8-10 CUC - (3 bits) this field contains the command to the Command Unit. Valid values are:

0 - NOP (doesn't affect current state of the unit)
1 - Start execution of the first command on the CBL. If a command is in execution, then complete it before starting the new CBL. The beginning of the CBL is in CBL OFFSET.

2 - Resume the operation of the command unit by executing the next command. This operation assumes that the command unit has been previously suspended.
3 - Suspend execution of commands on CBL after current command is complete.
4 - Abort current command immediately.
5-7 - Illegal for use. The effect will be exactly as NOP.

Bits 4-6 RUC - (3 bits) This field contains the command to the receive unit. Valid values are :

0	-	NOP (does not alter current state of unit).
1	-	Start reception of frames. If a frame is being received, then complete reception before starting. The beginning of the RFA is contained in the RFA OFFSET.
2	-	Resume frame receiving (only when in suspended state).
3	-	Suspend frame receiving. If a frame is being received, then complete its reception before suspending.
4	-	Abort receiver operation immediately.
5-7	-	Illegal for use. The effect will be exactly as NOP.

Bit 7 RESET - Reset chip (logically the same as hardware RESET).

CBL OFFSET -

This 16-bit quantity specifies the offset portion of the address for the first command block on the CBL. It is accessed only if CUC = START.

RFA OFFSET -

This 16 bit quantity specifies the offset portion of the address for the Receive Frame Area (RFA). It is accessed only if RUC = START.

CRCERRS - Counter

This 16 bit quantity contains the number of aligned frames discarded because of a CRC error (see Sec. 7.2.2). This counter is updated, if needed, no matter what the state of the RU is.

ALNERRS -Counter

This 16 bit quantity contains the number of misaligned frames discarded because of a CRC error. This counter is updated if needed in all RU states.

RSCERRS - Counter

This 16 bit quantity contains the number of good frames discarded because there were no resources to receive them. Frames intended for a host whose RU is in the No Receive Resources state, fall into this category. This counter is updated only if the RU is in the No Resources state.

OVRNERRS - Counter

This 16 bit quantity contains the number of frames that are known to be lost because of a lack of due to local system bus availability. If the traffic problem period lasts for more than the duration of one frame, the frames that follow the first one are lost without any indicator, and are not counted. This counter is updated, if needed, in all RU states.

2.3.1 Notes on Error Counters Operation

1. The CPUs clears all error counters, prior to initiating the 82586. The 82586 updates these counters by reading them, adding one and writing back to their SCB positions. Multiple errors will result in all the relevant counters update.

2. The counters are sticky; after reaching the value of FFFFH, the counters do not wrap around to zero. They will stay at this value, unless modified by the CPU.

3. The 82586 will update all the statistical counters after every frame. It may happen that more than one counter is to be updated. The 82586 will update all of them.

4. The 82586 performs the read counter/increment/write counter operation without relinquishing the bus. This is done to ensure that no logical contention exists between the 82586 and the CPU. In a dual port memory configuration, the CPU should not perform any write operation to any counter unless the counter is in FFFFH state. Otherwise, it is possible that the write operation will be overwritten by the 82586 that has recently read 'old' information from the counter. Since the 82586 does not write to the counter when FFFFH state is reached, the CPU may safely reset the counter.

2.3.2 Software Reset Operation

Upon reading a Reset bit set in the SCB command word, the 82586 will:

* Terminate the Transmit and Receive processes.

* Ignore the remaining SCB command field.

* Clear the SCB command word.

* Reset the chip.

After the 82586 has cleared the SCB command word, the reset effectively starts. Note that INT is not raised. The CPU must wait at least 10 system clocks before issuing the CA to the 82586, to trigger the initialization procedure.

2.3.3. Semantics of Control Commands

Control Commands are submitted independently to the RU and CU. The explanation below applies for both RU and CU control commands.

The commands are treated by the 82586 in two phases. The first phase is named CONTROL COMMAND ACCEPTANCE. Its termination is indicated by the 82586 clearing the SCB command word. Acceptance is complete after the 82586 responded to the CPU's request, read the command from SCB command word and performed the required activities, which depend on the state of the CU or RU.

The second phase is named CONTROL COMMAND EXECUTION, and is performed as soon as the current CU or RU activity (at CB or FD level) is finished. For the CU, it happens when the Command Block currently in execution, is completed. For the RU, it happens when the frame currently in reception has ended.

Both the CU and RU have a pointer to the next CB (for CU) or RFD (for RU). NEXT CB points to the Command Block to be executed after the current CB is completed. NEXT RFD points to the RFD to be set up after the present frame is received.

The Effect of the Control Commands

The effect of the Control Command is explained below:

* START - This command specifies the list of CBs or RFDs. NEXT CB or NEXT RFD pointer is always updated. If the unit is not active during acceptance (i.e., the CU is not executing CBs or the RU is not receiving a frame), the next CB or RFD will immediately be set up. In this case, the acceptance and execution phases overlap. If the unit is active during acceptance, the next CB or RFD will be set up at the end of the current activity (execution phase). In all cases, the next state of the units is READY.
* ABORT - At acceptance time, this command causes the immediate termination of the CU or RU activities.
End of execution is signalled by the CU or RU entering their idle states.
* SUSPEND - This command is ignored if the unit is not READY, at acceptance time. If the unit is READY, the present activity is completed (CB execution for CU and frame reception for RU) and the unit becomes SUSPENDED.
* RESUME - This command is ignored if the unit is not SUSPENDED. If during acceptance, the unit is not active (CB execution for CU, frame reception for RU), then NEXT CB or NEXT RFD are set up. Otherwise, the NEXT CB or NEXT RFD are set up at the end of the current activity. In any case, after execution, the new state of CU or RU is READY.

At the end of the activity (CB completion or reception of a frame completed), the CU or RU assesses its situation based upon 'EL' and 'S' bit status. If 'EL'is set, the last CB or RFD was exhausted. The CU becomes IDLE or the RU enters its No Resources state, regardless of any other factor. If 'S' is set, the unit becomes SUSPENDED.

* 'REQUESTS' REMEMBERED FROM ACCEPTANCE TIME

  - If a Suspend is requested, the unit becomes SUSPENDED.
  - If a Start is requested, the unit enters its READY state and CB or RFD setup follows.
  - If no request is pending, CB or RFD set up follows per Command Block List or Receive Frame List.

2.3.4 Rules for Using Control Commands

2.3.4.1 Handshake

- The CPU writes the control command to SCB command word and causes a falling edge of CA input.

- The 82586, after a finite but undefined number of clocks, recognizes the CA transition and performs its control command acceptance procedure, as described in Section 2.4.4 (for the CU) and 2.5.4 (for the RU). At the end of the sequence, the 82586 clears the whole SCB command word and places current CU and RU status into the SCB.

- At this time, the CPU is allowed to issue the next control command to the 82586.

- A new accepted control command cancels a previous control command that was accepted and awaits execution. (Note: A NOP control command does not cancel previous commands. This is provided to allow acknowledging interrupts without disturbing the CU and RU operation).

2.3.4.2 Normal Operation

- The CPU is notified that the control command was accepted by the 82586. This notification is signalled by the 82586 clearing the SCB command word.

- The execution of control commands may be deferred because of the CU or RU being active (CB execution or frame reception) at command acceptance time.

- When the control command execution is completed the new status of the CU and RU is reported.

- The only state transitions that are specifically signalled, with interrupt to the CPU, are RU and CU becoming not READY. Interrupt also happens at the completion of a CB (with I bit set) and after completing reception of a frame.

2.4 THE COMMAND UNIT

2.4.1 Overview

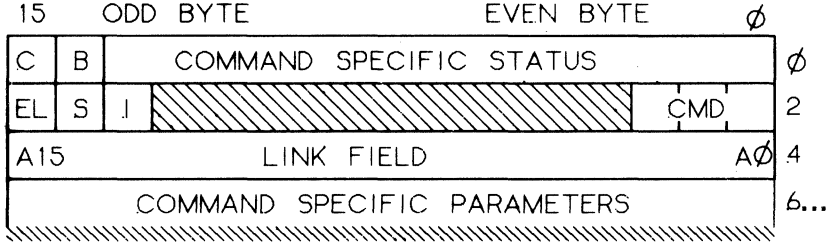
The CU is responsible for handling commands from the CPU. These commands fall into two categories: control and action. This section is concerned primarily with control commands and the generic class of action commands. Action commands are discussed in detail in Chapter 4.

Control commands are the means by which the CPU controls the CU's execution of action commands. Action commands are located in Command Blocks (CB) which are then linked together to form the Command Block List (CBL). The CBL may contain one or more CBs. The last CB is indicated by the End List (EL) bit in the CB being a one. The CU starts at the beginning of the CBL and executes the commands, one at a time, until the CB where EL = 1.

2.4.2 Command Blocks

Action commands are organized in blocks (CB's). The beginning of the CBL is defined by the CBL OFFSET in the SCB and its end is indicated by the EL bit in the last CB.

The generalized form of command block is:



where:

STATUS - This 14-bit field contains the command results. It is set at the same time as the C bit. It is not valid until C=1.

Most of the contents of this field are command dependent. There are two bits that are standard for all commands. They are :

Bit 13 - Indicates that the command was executed without error. If one, then no error occured (command executed OK). If zero, then an error did occur and the remaining bits should be consulted to discover what the problem was.

Bit 12 - Indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted and if necessary, it should be repeated. Refer to Section 2.6 for a detailed description of CU Abort control command. If bit 12 is zero, the command was not aborted.

LINK FIELD - A 16 bit pointer to the next Command Block.

EL - If set, this bit indicates that this command block is the last on the CBL.

S - If set to one, suspend the CU upon completion of this CB.

I - If set to one, the 82586 will generate an interrupt after execution of the command is completed. If I is not set to one, the CX bit will not be set.

CMD - A 3-bit field that specifies the command opcode. See Chapter 4.

Bits 4-12 - Reserved

C - This bit indicates the execution status of the command. The CPU initially sets it to zero when the Command Block is placed on the CBL. Following a command execution, the 82586 will set it to one.

B - This bit indicates that the 82586 is currently executing this command. It is initially set to zero by the CPU. The 82586 sets it to one when execution begins, and to zero when execution is completed.
Note: The C and B bits are modified in one operation.

For more information see Chapter 4.

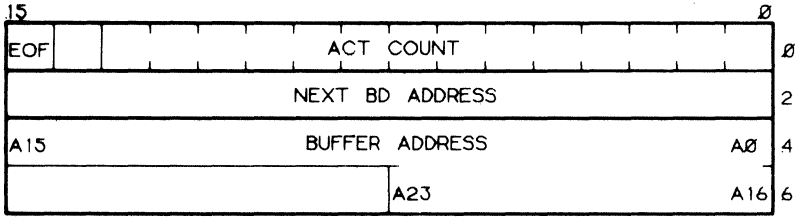
COMMAND SPECIFIC PARAMETERS - This is a variable length field that contains parameters for and/or results from the command. Its length and contents are command dependent. For further details see Chapter 4.

Command Blocks are chained together to form the CBL. When searching the CBL after an interrupt, the CPU can remove any block with C=1, since execution of it is complete. Manipulation of the CBL is described in Section 2.4.5. The forward link in the last CB may be used to form a cyclic list.

2.4.3 Transmit Buffer Descriptor

The transmit command accesses user data contained in buffers for Transmit operations. Each buffer is described by a Transmit Buffer Descriptor (TBD). TBDs are used with Transmit commands to contain user data that is to be sent. Each command may contain zero or more TBDs. The TBDs are linked together to form a frame. They are automatically prefetched by the CU as required.

The TBD has the following format:



where :

EOF - This bit indicates that this TBD is the last associated with the frame being transmitted. Set by the CPU before transmitting.

ACT-COUNT - This 14 bit quantity specifies the number of bytes that hold information for the current buffer. It is set by the CPU before transmit.

NEXT BD ADDRESS - The offset portion of the address of the next TBD on the list. It is meaningless if EOF = 1.

BUFFER ADDRESS - The starting address of the memory area that contains the data to be sent. This is a 24-bit physical address. In WORD mode the buffer address must be even.

2.4.4 Command Unit Control

The CU may be in one of three major states during normal operation. These states are:

a. IDLE - In this state the CU has no action commands to execute. It will still respond to control commands. The CU is initialized to IDLE state.

b. SUSPENDED - This state is similiar to IDLE, except that the CU may become READY by a RESUME command. It remembers the state of the CBL list. It comes to this state only via a SUSPEND control command or executing a CB with S = 1.

c. READY - In this state, the CU has commands on the CBL and is executing them.

The following three events may cause the CU to change state:

a. All control commands:

NOP - This command is ignored by the CU.

SUSPEND - This command suspends operation of the CU after the currently executing command is complete.

RESUME - This command returns the CU to the READY state from the SUSPENDED state.

START - This command gives the CU a new CBL to work on.

ABORT - This command stops the CU immediately. Execution of commands is stopped.

b. Action command (whose CB has S = 1) executed.

c. The end of the CBL is reached.

Multiple events may occur concurrently.

SET UP CB means: start processing the next command in the queue.

REQUEST SUSPEND means: the suspend will be executed as soon as the command, presently in execution, is done.

Most of the transitions do not cause interrupts. In actual operation, CX interrupts will be the most common. When the CPU receive an interrupt it examines the CBL and removes all CBs where C = 1. There may be more than one. The CPU should always keep a pointer to the first unexecuted CB.

CU not ready interrupts are due to the CU leaving the READY state. This may result from a control command, a CB with S = 1, or the end of the CBL. The CPU should maintain the context and so be able to determine the significance.

After initialization process is complete (see Sec. 3.1), the CU will issue both a CX and CU not ready interrupt. The CPU should expect such interrupts at the end of the initialization process.

Table 2.1 shows the CU activities at the end of the control command execution time:

TABLE 2.1: CU ACTIVITIES PERFORMED AT END OF EXECUTION

EL BIT	S BIT	REQUEST	NEXT STATE	ACTION
Ø	Ø	NONE	READY	SET UP CB
Ø	Ø	SUSPEND	SUSPENDED	CNR INTERRUPT
Ø	1	NONE	SUSPENDED	CNR INTERRUPT
Ø	1	SUSPEND	SUSPENDED	CNR INTERRUPT
1	Ø	NONE	IDLE	CNR,CX INTERRUPTS
1	Ø	SUSPEND	IDLE	CNR,CX INTERRUPTS
1	1	NONE	IDLE	CNR,CX INTERRUPTS
1	1	SUSPEND	IDLE	CNR,CX INTERRUPTS

NOTES:
1. After a CB with 'I' bit set is completed, CX interrupt is generated.
2. Since the transition READY to READY STATE via the START Command is smoothly performed, no interrupt, related to state transition, is generated and no action is required at the end of Action Command Execution.

2.5 THE RECEIVE UNIT

2.5.1 Overview

The Receive Unit (RU) handles all activities related to frame reception. It operates independently of the CU although it does use the CU to communicate with the CPU. It manages a pool of free memory space, the Receive Frame Area (RFA) that consists of two lists: Received Frame List (RFL) and Free Frame List (FFL). The SCB points to the RFL, and the last frame in the RFL points to the FFL.

The Free Frame List (FFL) consists of two lists: The first is a list of free Receive Frame Descriptors (RFD), called the Receive Descriptor List (RDL). The second is a list of free buffers, called the Free Buffer List (FBL), with each described by a Receive Buffer Descriptor (RBD). The root of the FBL is the first RFD on the RDL (Figure 2.1).

The address of the RFA (the first RFD on the RDL) is given to the RU by the CPU using the SCB with a start control command. One RFD is used for each received frame and as many RBDs (actually the buffers associated with each) as are required to contain the frame.

When either list is exhausted the RU notifies the CPU and enters the No Resources state.

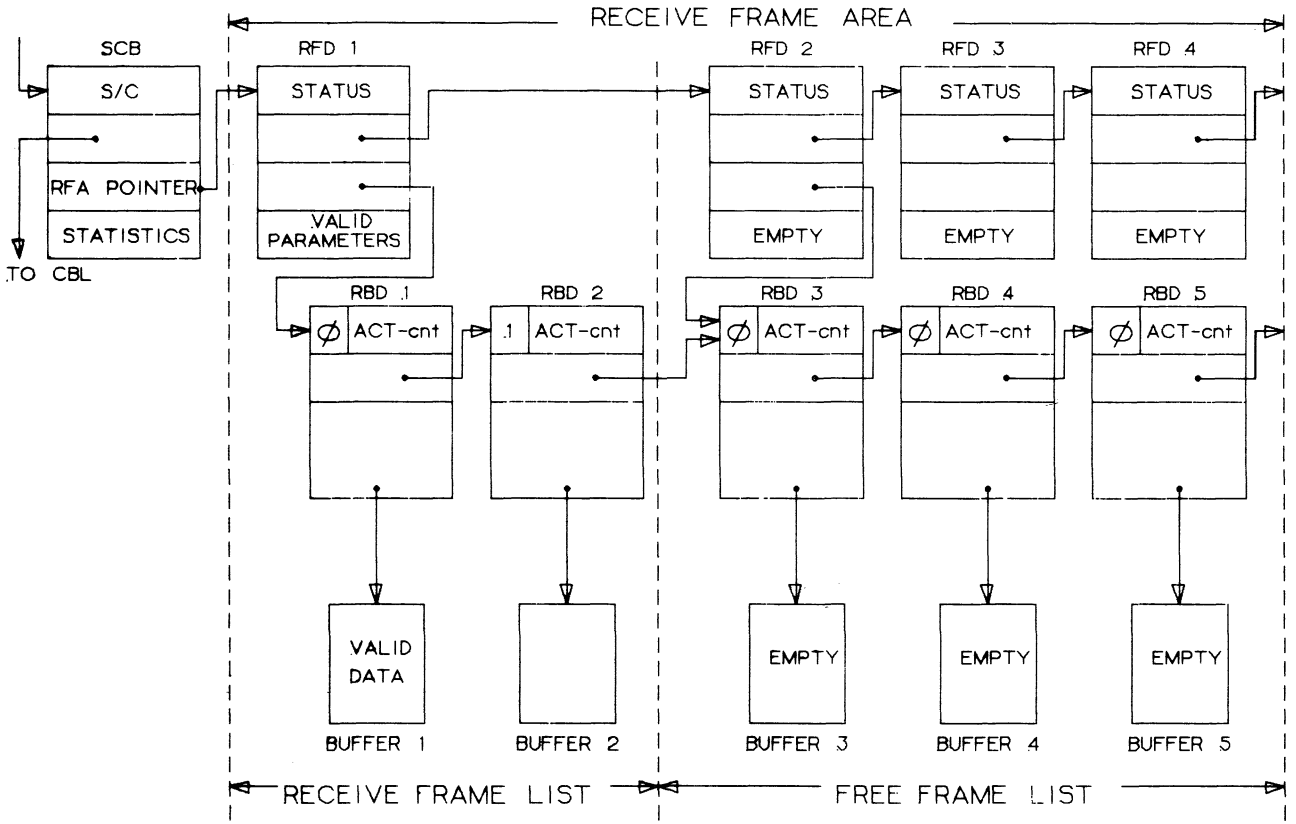
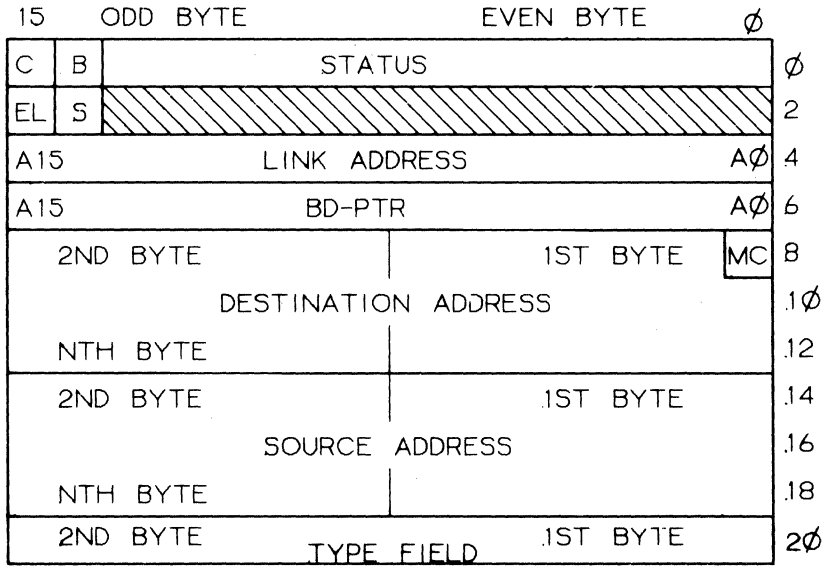


FIGURE 2.1: RECEIVE FRAME AREA

2.5.2 THE RECEIVE FRAME DESCRIPTOR

Each received frame is described by one Receive Frame Descriptor. The RFD used is the one at the head of the RDL.

The format of the receive frame descriptor is:



where:

STATUS - The results of the receive frame descriptor operation. Defined bits are:

Bit 13: Frame received without errors
Bit 12: Reserved - not used
Bit 11: CRC error in an aligned frame
Bit 10: Alignment error (CRC error in misaligned frame)
Bit 9: Ran out of buffer space
Bit 8: DMA Overrun
Bit 7: Frame Too Short
Bit 6: No EOF flag (for Bitstuffing only)
Bits 0-5: Not used (reserved)

RFD's with bit 13 not equal 1 will occur only if the SAVE BAD FRAME configuration option is selected. Otherwise all frames with errors will be discarded, although statistics will be kept on them.

LINK-ADDRESS - A 16-bit pointer to the next Receive Frame Descriptor. The Link Address of the last frame can be used to form a cyclic list.

EL - If set, this bit indicates that this RFD is the last one on the RDL.

S - If set, suspend the RU after receiving thisframe.

C - This bit indicates the completion of frame reception. It is set by the 82586.

B - This bit indicates that the 82586 is currently receiving this frame, or that the 82586 is ready to receive the frame. It is initially set to zero by the CPU. The 82586 sets it to one when reception set up begins, and to zero upon completion. The C and B bits are set in one operation.

BD-PTR - The offset portion of the address of the first RBD containing frame data. BD-PTR = OFFFFH indicates no RBD at all.

MC - Multicast bit.

DESTINATION ADDRESS - The contents of the destination address of the receive frame. The field is 0 to 6 bytes long.

SOURCE ADDRESS - The contents of the Source Address field of the received frame. It is 0 to 6 bytes long.

TYPE-FIELD - The contents of the type field of the received frame. It is 2 bytes long.

NOTES:

1. The last 4 fields will not be used when the 82586 is configured to locate address/control in the data buffers (AC-LOC=1 - see Sec. 4.3).

2. The last four fields are packed, i.e. one field immediately follows the next.

The receive buffers can be of different lengths. The 82586 will place no more bytes into a buffer than is indicated in the associated RBD. The 82586 will prefetch the next RBD in-time to use it.

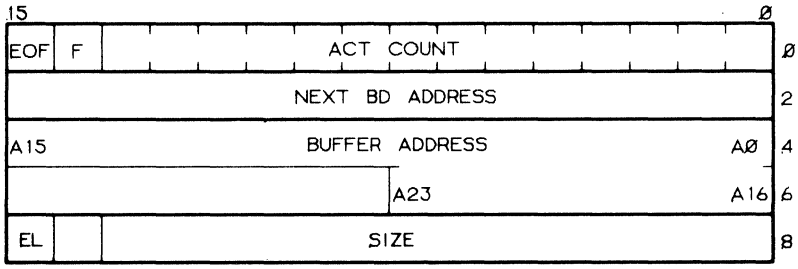
The 82586 will attempt to receive frames as long as the FBL is not exhausted. If it becomes exhausted, the 82586 Receive Unit will enter the No Resources state.

Before starting the RU, the CPU must place the pointer to the FBL in BD-PTR field of the first RFD. All remaining BD-PTR fields for the subsequent RFDs should be FFFFH.

If the Receive Frame Descriptor and the associated receive buffers are not reused (frame is well received or the 82586 works in a mode where it saves bad frames), the 82586 writes to the BD-PTR field of the next RFD, the address pointer of the next free RBD.

2.5.3 Receive Buffer Descriptor (RBD)

The information field of a frame is not a part of the RFD, but is accessed with a special pointer to a separate block in order to provide the flexibility of separating control from information. The information field of a frame is placed in a set of buffers that are chained by a sequence of Receive Buffer Descriptors. The RFD points to the first RBD, and the last RBD is flagged with an EOF bit set to one. The format of the Receive Buffer Descriptor is as follows:



where :

EOF - Indicates that this is the last buffer related to the frame. It is cleared by the CPU before starting the RU and written by the 82586 at the end of reception of the frame.

F - Indicates that this buffer has already been used. The Actual Count has no meaning unless the F bit equals one. This bit is cleared by the CPU before starting the RU, and set by the 82586 after the associated buffer has already been used.

ACT COUNT - This 14 bit quantity indicates the number of meaningful bytes in the buffer. It is cleared by the CPU before starting the RU and written by the 82586 after the associated buffer has already been used. In general, after the buffer is full, Actual Count value equals the size field of the same buffer. For the last buffer of the frame, Actual Count maybe less than the buffer size. NOTE: If Actual Count is odd (in word mode), garbage will be written by the 82586 into the high byte of the last word.

NEXT BD ADDRESS - The offset portion of the address of the next RBD on the list . It is meaningless if EL = 1.

BUFFER ADDRESS - The starting address of the memory area that contains the data tnat was received. This is a 24 bit physical address. In word mode, the buffer address must be even.

EL - Indicates that the associated buffer to this RBD is last in the FBL.

SIZE - This 14 bit quantity indicates the size, in bytes, of the associated buffer. In word mode the quantity must be even.

2.5.4 RECEIVE UNIT CONTROL

The RU may be in one of four basic states.

These states are :

a. IDLE - In this state the RU does not respond to frames on the serial link and does not modify any data structures. The RU is initialized to this state.

b. SUSPENDED- This state is similiar to IDLE, except that the RU may become READY by a RESUME command. It remembers the state of the RFA lists. It transfers to this state via a SUSPEND control command or after a RFD with S = 1.

c. NO RESOURCES - In this state the RU is looking for frames on the serial link, but has no buffers or no descriptors to store them in. It will keep statistics on how many frames were lost.

d. READY - In this state, the RU is looking for frames and has buffers to store them in.

In each of these states, the RU may or may not be receiving a frame. If a frame is being received, the situation is named 'RU Actively Receiving'. If the RU is READY and Actively Receiving, the frame is being stored in RFA buffers. If the RU is not READY (IDLE, SUSPENDED or NO RESOURCES), the frame is 'discarded'. The RU still maintains statistics on CRC, Alignment or Overrun errors for discarded frames, although the frames themselves are lost.

The following three events that may cause the RU to change state:

a. All control commands:

NOP - This command is ignored by the RU.

SUSPEND - This command suspends operation of the RU when frame reception is completed.

RESUME - This command causes RU transition from SUSPENDED state to READY state.

START - This command gives the RU a new RFA to work on. The RU is exited to READY state.

ABORT - This command stops the RU immediately. Reception of any frame is stopped, and the CU goes into the IDLE state.

b. A frame is received using a RFD with S = 1.

c. The end of the RDL or FBL is reached.

SET UP RFD means: Prepare the next RFD for frame reception.

Most transitions do not cause interrupts. Most interrupts are caused by frames being received. When the CPU gets a FR interrupt, it should scan down the RDL, removing all RFDs where C = 1. There may be more than one RFD. The CPU should keep a pointer to the head of the RDL.

RU Not Ready interrupt, might be caused a control command issued by the CPU to the RU, reception of a frame using a RFD with S = 1, or to the exhaustion of either (or both) the RDL or FBL.

The reason for RNR interrupt may be identified by CPU, knowing it has issued a control command and by testing the S and EL bits of the last used RFD.

Table 2.2 shows the RU activities at control command execution time.

TABLE 2.2: RU ACTIVITIES PERFORMED AT END OF EXECUTION

EL BIT	S BIT	REQUEST	NEXT STATE	ACTION
Ø	Ø	NONE	READY	SET UP RPD
Ø	Ø	SUSPEND	SUSPENDED	RNR INTERRUPT
Ø	Ø	START	READY	SET UP RPD
Ø	1	NONE	SUSPENDED	RNR INTERRUPT
Ø	1	SUSPEND	SUSPENDED	RNR INTERRUPT
Ø	1	START	SUSPENDED	RNR INTERRUPT
1	Ø	NONE	NO RESOURCES	RNR INTERRUPT
1	Ø	SUSPEND	NO RESOURCES	RNR INTERRUPT
1	Ø	START	READY	SET UP RPD
1	1	NONE	NO RESOURCES	RNR INTERRUPT
1	1	SUSPEND	NO RESOURCES	RNR INTERRUPT
1	1	START	READY	SET UP RPD

Note: After a frame is received, FR interrupt is generated.

Regardless of its state, the RU looks for start requests at the end of a receive frame. This guarantees that frames are either housed in the old RFA or entirely in the new RFA. There is a sharp transition from the old RFA to the new RFA, that takes place at the end of the receive frame.

Note, the process of starting the RU takes time. During this time, receive frames may be lost due to a temporary lack of memory resources. This situation may arise, even if the previous RFA has enough resources to contain the incoming frame.

Depending on the 82586 internal state, the RSCERR or OVRNERR counters in SCB will be updated. CRCERR and ALNERR counters will be updated as usual.

2.6 INTERRUPT OPERATION

The INT pin is used to notify the CPU about one or more of the following events:

* a command in CB with its 'I' bit set was executed (CX interrupt).
* a frame was received (FR interrupt).
* the CU became Not Ready (CNR interrupt).
* the RU became Not Ready (RNR interrupt).

2.6.1. Interrupt Request Sequence

Once an event requiring an interrupt has occured, the following sequence is performed by the 82586 :

1. INT pin is set to its low level (inactive).

2. The status word in SCB is written, denoting the source of the interrupt (CX, FR, CNR or RNR interrupt), together with the states of the CU and RU.

3. INT pin is raised (set to active).

2.6.2 Interrupt Servicing by the CPU

Upon detecting a rising edge on the INT pin, the CPU may perform its interrupt service routine, as follows :

1. Save registers
2. Wait until the SCB command word is 'All Zero'
3. Read SCB STATUS field
4. Determine the cause(s) of the interrupt and the states of the CU and RU
5. Process each interrupt cause and determine the next control commands for the CU and RU
6. Write Interrupt Acknowledge bits to the processed interrupt requests together with the next control commands for CU and RU
7. Issue a CA falling edge to the 82586
8. Restore registers and exit interrupt routine

2.6.3. 82586 Response to CA

Upon detecting a falling edge on its CA input, the 82586 performs the CA acceptance sequence, as follows :

1. Determine which interrupt requests were acknowledged by the CPU. For each of them clear the corresponding interrupt request bit in SCB status word.

2. Perform the control command acceptance procedure, as described in Sections 2.4.4 (for the CU) and 2.5.4 (for the RU).

3. The INT pin is set LOW.

4. Write the SCB status word indicating the unacknowledged interrupt requests, and newly generated interrupt requests, together with CU and RU states.

5. If any interrupt request bit is active, set the INT pin to HIGH.

2.6.4 Initialization Procedure

2.6.4.1. 82586 Actions

* After Reset (either hardware or software reset), INT pin is set to its low level (inactive).
* The 82586 waits for a CA high to low transition.
* When this happens, the initialization procedure described in Section 2.1 is performed. Upon completion, CX (Command Executed) and CNR (CU became Not Ready), interrupts are written to SCB status word, together with the status of CU and RU (both are idle).
* The INT pin is then set to HIGH.

2.6.4.2 CPU Actions

* CPU should expect interrupts as part of the 82586 initialization procedure.
* It writes the control commands for the CU and RU (typically STARTing both) and acknowledges the CX and CNR interrupts.
* It issues a CA to the 82586 and the INT/CA handshake mechanism keeps rolling on by itself.

2.7 INTERACTION BETWEEN CONTROL & ACTION COMMANDS

2.7.1 82586 Channel Attention (CA) Timing

The CU is responsible for control command acceptance, following the trailing edge on CA input. The CU will first finish all its higher priority activities and only then accept the control commands.

Higher priority CU activities that delay CA acceptance are :
a. Transmit BD prefetch
b. Transmit buffer switching
c. Current CB command completion

The 82586 will accept a CA prior to the set up of the next CB in the CBL.

The CU recognizes an RU control command and notifies the RU. The RU will first finish all its higher priority activities, and only then accept the control command.

Higher priority RU activites that delay CA acceptance are :
a. Receive BD prefetch
b. Receive buffer switching
c. Receive end of frame processing

Only after the CU and RU have accepted the control command, the SCB command word is cleared. At that time the CPU may issue the next CA to the 82586.

Internally to the 82586, the CA trailing edge is detected and latched. Prior to reading the SCB control command, the 82586 clears the latch. A new CA, given to the 82586 before the SCB command word is cleared, may be lost due to its being cleared before serviced. The user must refrain from such violations.

The 82586 does not wait until for reception or transmission to end in order to process a CA. The SCB related operations will be carried out on an interleaved basis with the transmission or reception process.

2.7.2 Critical Regions In The Interface To The CPU

2.7.2.1. Common Bus Operation

When the 82586 and the CPU reside on the same system bus, the bus aquisition and release is governed by the HOLD/HLDA protocol. This scheme ensures that only one bus master owns the bus at a time.

The 82586 performs its bus accesses to a descriptor in memory without relinquishing the bus. This results in a certain number of system clocks where the system bus is owned by the 82586, but no bus activity happens.

The only way for the CPU to enforce the 82586 off the bus during descriptor processing, is by dropping HLDA. In this case, the CPU and any other master peripheral must refrain from modifying 82586 memory control structure.
The affected descriptors are :

* Command Blocks
* Receive Frame Descriptors
* Transmit Buffer Descriptors
* Receive Buffer Descriptors
* System Control Block

2.7.2.2 Dual Ported RAM Configuration

In a system where the 82586 communicates with the CPU via Dual Ported RAM, the same memory location can be accessed in principle simultaneously from both sides.

To avoid system divergence to unknown state, the CPU can modify the control structure for command or receive, only if the corresponding 82586 unit is in an inactive state (IDLE, SUSPENDED, or NO RESOURCES for RU only).

Note: The 8207 (Dual Port Dynamic RAM Controller) does not fall into this category. The 8207 has a LOCK capability, that enables the 82586 to lock out the CPU accesses till the 82586 finishes its descriptors process. In this way, the limitations noted in this section do not apply to the 8207 interface.

3.0 INITIALIZATION AND CONFIGURATION

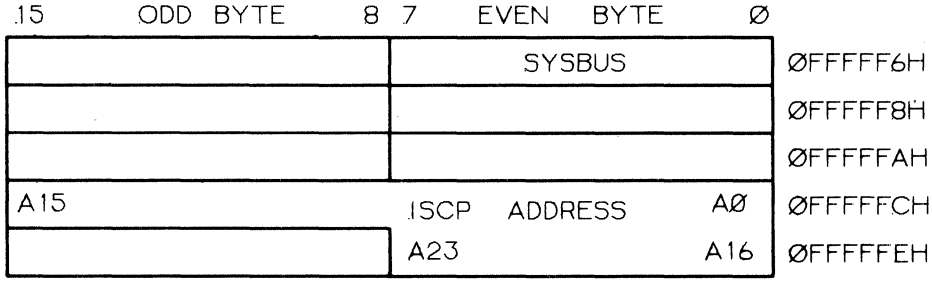
3.1 INTIALIZATION

The 82586 accesses the "Initialization Root" as part of the initialization sequence, begun after CA is asserted for the first time following a RESET. The Initialization Root consists of two data structures addressed via two pointers: the System Configuration Pointer (SCP) and the Intermediate System Configuration Pointer (ISCP).

The primary purpose of this process, in addition to bringing the 82586 into a stable state, is to locate the SCB and that in turn defines the 64k byte page in which all command/control structures are located.

3.1.1 THE SYSTEM CONFIGURATION POINTER (SCP)

The SCP begins at location OFFFFF6H and is the only fixed address data structure in an 82586 system. It's purpose is to specify the width of the data bus used by the 82586 (8 or 16 bits), as well as the location of the ISCP. The SCP for the 82586 shares the location OFFFFF6H with the SCPs of all other Master peripherals. The format of the SCP is:



where:

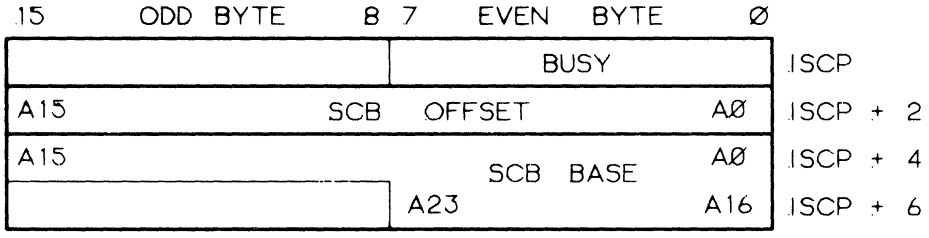
SYSBUS - Specifies whether the system data bus available to the 82586 is 8-bits or 16-bits wide. A "1" indicates 8-bits, and a "0" indicates 16-bits. During the first read operation from the SCP, the 82586 assumes a byte wide bus, reading the SYSBUS byte. The bus width goes into effect immediately after SYSBUS is read.

ISCP ADDRESS - A 24-bit quantity that is the physical address of the ISCP.

3.1.2 THE INTERMEDIATE SYSTEM CONTROL POINTER (ISCP)

The ISCP specifies the location of the SCB. Usually, all Master peripherals in a system will share the same ISCP address. The SCP will often be in ROM with the ISCP in RAM. The CPU will load the address of the SCB (or an equivalent data structure) for each Master peripheral into the ISCP and assert the peripheral's CA. The 82586 now begins initialization procedure to fetch the address of the SCB via the SCP and ISCP.

The base address of the SCB is also the base address of all Command Blocks, Frame Descriptors and Buffer Descriptors (but not buffers) in the system. All such data structures must exist in a 64K byte segment. The format of the ISCP is:



where:

BUSY - Indicates that the 82586 is being initialized. It is set to 01H by the CPU before its first CA to the 82586. It is cleared by the 82586 after the SCB base and offset are read. Note that the most significant byte of the first word of the ISCP is not modified when BUSY is cleared.

SCB OFFSET - This 16-bit quantity specifies the offset portion of the address of the SCB.

SCB BASE - This 24-bit quantity specifies the base portion of the address of the SCB. The base of SCB is also the base of all 82586 Command Blocks, Frame Descriptors and Buffer Descriptors.

Note: All descriptors (segment addresses) must start at even addresses in word mode.

3.1.3 INITIALIZATION PROCEDURE

The CPU sets up the SCP, ISCP, and the SCB structures. It also sets BUSY to 01H. The initialization procedure is started by the CA signal following a RESET. This CA causes the 82586 to access the SCP at locations OFFFFF6H (see Figure 3.1). The SYSBUS byte is fetched in byte mode. Once the bus width is determined, all further memory transfers will be at the specified bus width. After the SCP is accessed, the 82586 fetches the ISCP. The 82586 saves the base of the SCB (that is, the base of all the control blocks), as well as the SCB address. It clears busy, sets CX=1 and CNR=1 in the SCB (see Section 2.3), clears the SCB Command word, signals an interrupt to the CPU, and waits for a CA.

The RESET configures the 82586, prior to CA, to an operational mode compatible with the Ethernet standard. Only Broadcast Address is accepted by the 82586 until an Individual Address is set up. If there is a need to change some parameters, this can be done with a CONFIGURE command.

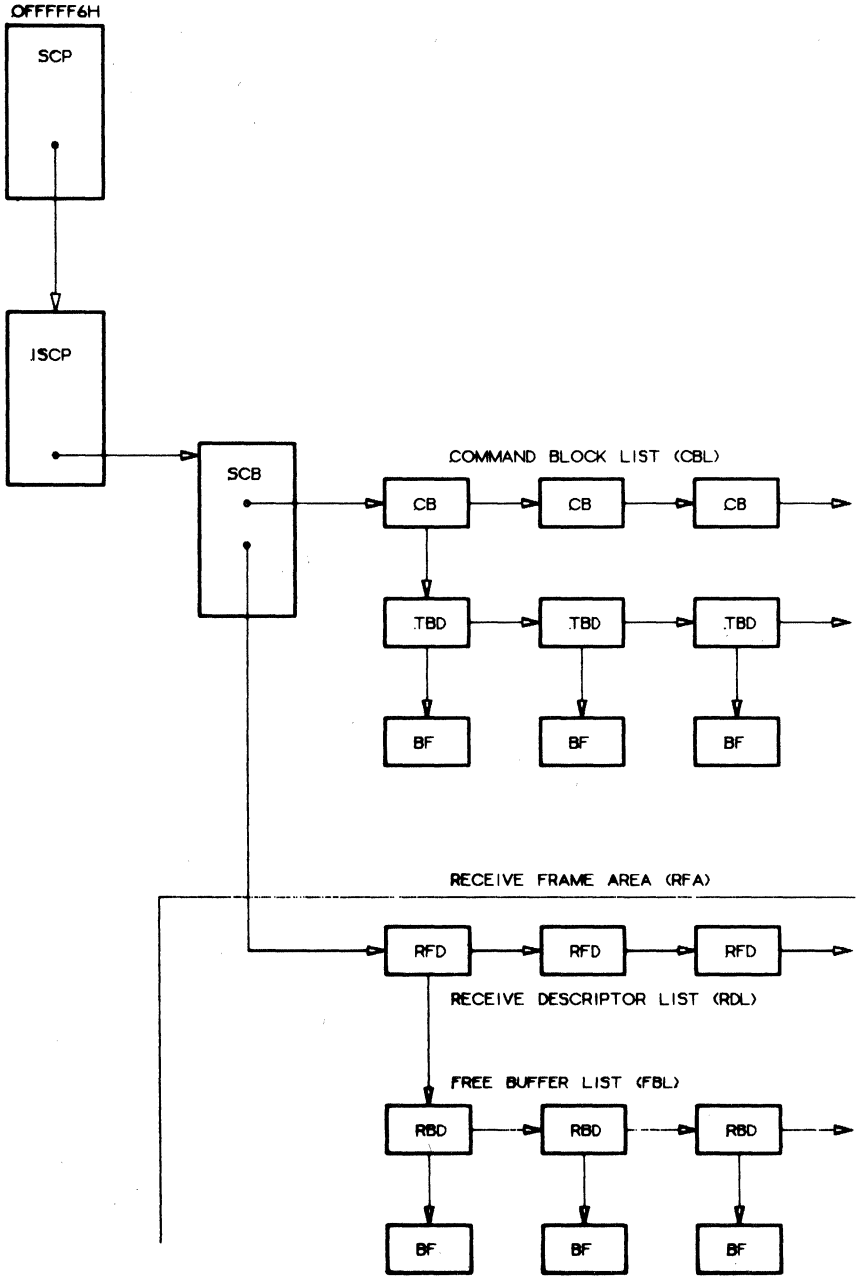


FIGURE 3.1: THE SHARED 82856/CPU MEMORY STRUCTURE

3.2 CONFIGURATION

Operation parameters are loaded into the 82586 via the configure command (see Section 4.3). Configuration parameters are:

FIFO-LIMIT

Specifies the point in the FIFO at which the 82586 requests the bus in order to transfer data to/from its internal FIFO from/to memory.

SRDY/$\overline{\text{ARDY}}$

Selects between synchronous ready function and asynchronous ready function of the SRDY/ARDY pin.

0 - ARDY - Asynchronous Ready i.e. The Ready signal is internally synchronized by the 82586. This adds one wait state to the 82586 bus cycle.

1 - SRDY - Synchronous Ready i.e. 82586 assumes that the Ready signal is externally synchronized.

Save-Bad Frame

Specifies whether errored frames (CRC error, Alignment error, etc.) are to be discarded or saved. 0 - discard, 1 - save. In Save Bad-Frame mode, the Receive Frame Descriptor, as well as the Receive Buffer Descriptors and Receive Buffers are NOT reused for the next frame. In the complementary mode, all the descriptors and buffers used for bad frames, will be reused thus, not leaving any information about the lost frame except for statistical tallies update.

Address Length

Determines the length, in bytes, of the address that the 82586 refers to. This includes Source, Destination, Multicast, or Broadcast Addresses.

Address/Control Field Location

0 - Address and Type Fields are located in consecutive bytes in the descriptor.

1 - The whole frame is located in the data buffers. Source Address insertion by the transmitting 82586, is disabled.

INT-Loopback

When set, the 82586 disconnects itself from the serial wire and logically connects TxD to RxD and TxC to RxC. TxC must still be supplied by the user. Internally, TxC is divided by 4. This slows down the serial bit rate sufficiently to enable 82586 operation in full duplex. This will alter the effective values of all configure command parameters that are defined in terms of TxC. Note that this is purely Internal Loopback capability. Note, the INT-Loopback bit overrides the EXT-Loopback, i.e. having an INT-Loopback bit set, at the same time with EXT-Loopback, causes the 82586 to operate in Internal Loopback Mode.

EXT-Loopback

The 82586 will receive and transmit simultaneously, at full rate, a frame limited to 18 bytes (including the Frame Check Sequence). This allows checking of external hardware as well as the serial link to the transceiver. For Ethernet transceivers, since the transmitted data is fed back via the receive pair, practically nothing has to be done to perform External Loopback. For other transceiver types, the user is responsible for external transmit-receive interconnection.

Note: Internal Loopback bit overrides External Loopback bit.

Linear Priority

These bits define the amount of delay (expressed in Slot Time period units) that a station will withold itself from transmission after the Interframe Spacing.

For Linear Priority greater than zero, the 82586 will check the Carrier Sense at the timeout completion. If the station senses carrier, it assumes that higher priority station (with lower Linear Priority number) grabbed the link and will withold itself from transmission.

All stations being configured to zero Linear Priority is equivalent to Ethernet.

Exponential Priority

This number provides priority by affecting the average Exponential Backoff delay. If:
EP - is the exponential priority number
N - the number of collisons
r - the random number multiplicant of the Slot Time

then, r is chosen randomly according to the following :

$$0 \leqslant r < 2^{\text{MIN}\,[N+EP,\ 10]}$$

Thus, for EP = 0, we simply get the Ethernet Exponential Backoff Delay.

Exponential Backoff Method

Determines when to start the backoff timeout :

0 - According to 3-company standard, immediately after the jamming, concurrently with Interframe Spacing.
1 - After the deferring period expires. This method prevents inefficiency and throughput loss at short topologies and low bit rates where Interframe Spacing may be longer than the Slot Time.

Interframe Spacing

Specifies the time period, in TxC units, that the 82586 must wait after detecting loss of Carrier Sense before it can begin transmission or reception of a frame. The minimum value is 32 and any value less than that will default to 32. However, during DUMP STATUS command execution, the original configuration number will be read out.

Slot Time

The network Slot Time number or number of TxC cycles in the Slot Time. This value is the basis for backoff delay generation. Zero Slot Time number will be interpreted by the 82586 as 2048.

Promiscuous Mode

If configured to Promiscuous Mode, the 82586 will accept frames independently of their Destination Address.

Broadcast Disable

Disables reception of frames with Broadcast Address even via the Multicast mechanism. Promiscuous Mode bit overwrites the Broadcast Disable Mode.

Manchester/NRZ

Specifies whether NRZ or Manchester encoding/decoding is to be performed.

0 - NRZ.
1 - Manchester.

Note, in Manchester mode there is a need for external receive clock recovery logic from the receive data.

Transmit On No CRS

If set, allows transmission even if there is no CRS back from the transceiver. Important for transceivers (non-Ethernet) that do not feed back the transmitted signals via the receive pair.

No CRC Insertion

0 - CRC is inserted at the end of the frame.
1 - No CRC insertion - (allows higher level CRC generation).

CRC-16/CRC-32

0 - 32-bit Autodin-II CRC.
1 - 16-bit CCITT CRC.

Bitstuffing/EOC

0 - End of Carrier Framing.
1 - Bitstuffing Framing, with HDLC type start of frame/end of frame delimiters.

Padding

Only valid if Bitstuffing is set. If set to padding mode, the 82586 will append automatically flags to frames, shorter than a Slot Time period. Thus, the activity on the link will be for at least one Slot Time period.

CRS-Filter

Specifies the required minimal width of CRS, in TxC cycle units, before it will be recognized as a being Carrier Sense. The Carrier Sense Expired state is recognized immediately.

Internal CRS

Specifies whether Carrier Sense is to be generated internally or externally (via CRS pin).

0 - External.
1 - Internal.

CDT-Filter

Specifies for externally generated Collison Detect, the required width of CDT, in TxC cycle units, before Collison Detect will be treated as a collision.

Internal CDT

Specifies whether Collision Detect is to be generated internally or externally (via CDT pin).
0 - External, 1 - Internal.
Operates only with transceivers that do not feed back transmitted data on the receive pair, but can sense some other station data.

Min-Frame-Length

The minimum frame size, in bytes. No frame that is shorter than the minimum will be accepted by the 82586. NOTE: Apart from this mechanism, there are some other limitations on the minimum frame length:

First, frames which are shorter than 6 bytes (even in Save Bad Frame Mode, Promiscuous Mode, Address Length of Zero) are discarded. No status is reported on such received frames.

Second, for AC - LOC =0 (when Address Control Location implies data separated from control), also frames shorter than 2 x ADDR-LEN + 2 (not including the Frame Check Sequence) are discarded.

Preamble Length

Selects the length of the preamble including BOF.

00 - 2 bytes
01 - 4 bytes
10 - 8 bytes
11 -16 bytes

Number of Retries

The number of retries after collision the 82586 will perform before the transmit attempt is aborted.

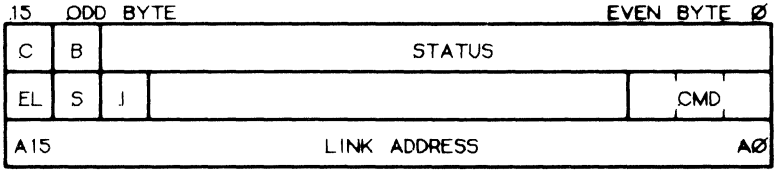
4.0 ACTION COMMANDS

The action commands reside in the CBL. The general action command structure is described in Sec. 2.4. There are three types of action commands :

a. 82586 Configuration and Setup
b. Transmission
c. Diagnostics oriented

4.1 NOP

This command results in no action by the 82586, except for that performed in normal command process. It is present as an aid to CBL manipulation. The format of the NOP command is:



where:

LINK ADDRESS, EL, B, C, I, S, OK - As per standard CB's (see Sec. 2.4.2)

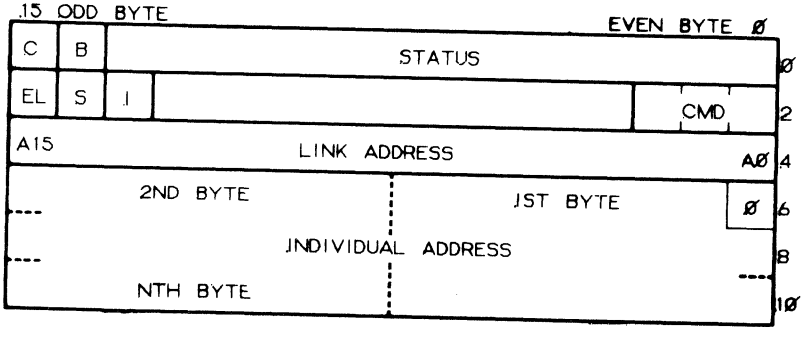
CMD - The NOP command. Value: OH.

STATUS - Bits 12,13 as per standard CB's (See Sec. 2.4.2)

4.2 INDIVIDUAL ADDRESS SET UP

This command is used to load the 82586 with the Individual Address. This address will be used by the 82586 for recognition of Destination Address and insertion of Source Address.

The format is as follows :



where:

LINK ADDRESS, EL, B, C, I, S - As per standard CB's (See Section 2.4.2)

CMD - The ADDRESS SETUP command. Value: 1H.

STATUS - Bits 12,13 as per standard CB's (See Sec. 2.4.2.).

Note: After RESET, and prior to Individual Address Setup Command execution, the 82586 assumes the Broadcast Address as the Individual Address in all aspects: i.e.:

* This will be the Individual Address Match reference.
* This will be the Source Address of a transmitted frame (for AC-LOC=0 mode only).

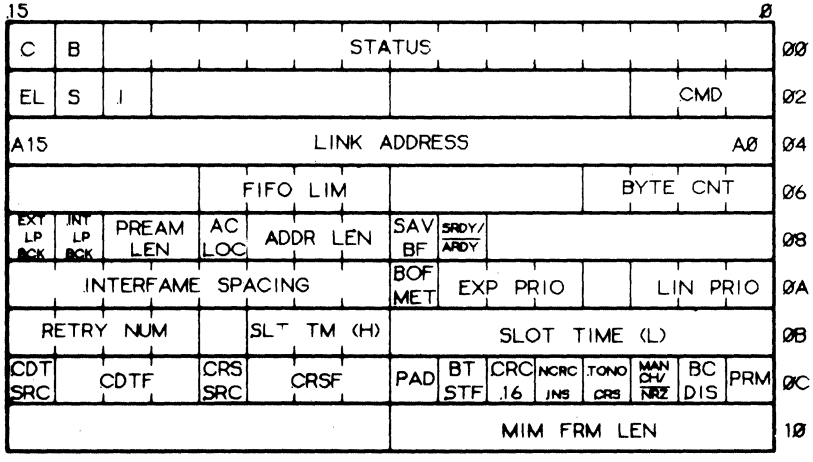
The Individual Address least significant bit must be zero for Ethernet (see the Command Structure). However, no enforcement of 0 is provided by the 82586. Thus, Individual Address with least significant bit 1, is a valid Individual Address in all aspects.

INDIVIDUAL ADDRESS - The individual address of the node.

4.3 CONFIGURE

The Configure command is used to load the 82586 with its operating parameters. (See Section 3.2). The Configure command allows changing only part of the parameters by specifying a byte count of less than 12. Any number larger than 12 will be truncated to 12. Any number less than 4 will be rounded to 4.

The format of the Configure command is :



The interpretation of the fields is as follows (parameters are defined in Section 3.2):

LINK ADDRESS, EL, B, C, I, S - As per standard CB's (see Sec. 2.4.2)

STATUS - Bits 12,13 as per standard CB's.

CMD - The Configure command value: 2H.

Byte 1: BYTE-CNT (Bits 0-3) - Byte Count. Number of bytes including this one, that hold parameters to be configured.

NOTES:
1. In word mode,if programmed to odd number, the last byte is truncated.
2. Number smaller than 4 is interpreted as 4.
3. Number greater than 12 is interpreted as 12.

Byte 2: FIFO-LIM (Bits 0-3) - FIFO LIMIT value

Byte 3: SRDY/$\overline{\text{ARDY}}$(Bit 6):0 - SRDY/ARDY pin operates as ARDY (internal synchronization)

1 - SRDY/ARDY pin operates as SRDY (external synchronization)

SAV-BF (Bit 7) 0 - Received bad frames are not saved in the memory.

1 - Received bad frames are saved in the memory.

Byte 4: ADDR-LEN (Bits 0-2) - Number of address bytes.
NOTE: 7 is interpreted as 0.

AC-LOC (Bit 3) 0 - Address and Type Fields are separated from data and are associated with Transmit Command Block or Receive Frame Descriptor. For transmitted frame, the Source Address is generated by the 82586.

1 - Address and Type Fields are part of the transmit/receive data buffers, including the Source Address.

PREAM-LEN (Bits 4-5)- Preamble Length including Beginning Of Frame indicator.

00 - 2 bytes
01 - 4 bytes
10 - 8 bytes
11 - 16 bytes

INT-LPBCK (Bit 6) Internal Loopback.

EXT-LPBCK (Bit 7) External Loopback.

NOTE: Bits 6 and 7 configured to 1, cause Internal Loopback.

Byte 5: LIN-PRIO (Bits 0-2) Linear Priority

EXP-PRIO (Bits 4-6) Exponential Priority

BOF-MET (Bit 7) Exponential Backoff Method

0 - Ethernet
1 - Short Topology and/or Low Bit Rate (Interframe Spacing shorter than the Slot Time).

Byte 6: INTERFRAME-SPACING Number that indicates the Interframe Spacing in TxC period units.
NOTE: Number smaller than 32 is interpreted as 32.

Byte 7: SLOT-TIME (L) Slot Time number, low byte.

Byte 8: SLT-TM (H) (Bits 0 -2) Slot Time, number,high byte.

NOTES:
1. Slot Time is the Slot Time number of TxC period units.
2. Slot Time Number of zero is interpreted as 2048 (2^{11}).

RETRY-NUM (Bits 4-7) Number of transmission retries on collisions.

Byte 9: PRM (Bit 0) Promiscous mode
0 - Non Promiscuous address filtering mode.
1 - Promiscuous Mode.

BC-DIS (Bit 1) Broadcast Disable.
0 - Broadcasted frames accepted.
1 - Broadcasted frames rejected.

MANCH/NRZ (Bit 2) Manchester or NRZ encoding/decoding.
0 - NRZ
1 - Manchester

TONO-CRS (Bit 3) Transmit On No Carrier Sense
0 - Cease transmission if CRS goes inactive during frame transmission (after preamble is sent).
1 - Continue transmission even if there is no Carrier Sense.

NCRC-INS (Bit 4) No CRC Insertion
0 - 82586 generates and appends FCS to transmitted frames.
1 - Disable the internal logic that generates CRC.

CRC-16 (Bit 5) CRC Type
0 - 32 bit Autodin II CRC polynomial.
1 - 16 bit CCITT CRC polynomial.

BT-STF (Bit 6) Bitstuffing
0 - End Of Carrier mode (Ethernet)
1 - HDLC like Bitstuffing mode.

PAD (Bit 7) Padding

0- No Padding

1 - Perform padding by transmitting flags for the rest of the Slot Time.

NOTE: PAD has meaning only for Bitstuffing. In EOC mode, PAD value is internally enforced to zero.

Byte 10: CRSF (Bits 0-2) Carrier Sense Filter bits

CRS-SRC (Bit 3) Carrier Sense Source.
0 - Carrier Sense Signal externally generated.
1 - Carrier Sense Signal internally generated.

CDTF (Bits 4-6) Collision Detect Filter bits

CDT-SRC (Bit 7) Collision Detect Source
0 - Collison Detect signal externally generated.
1 - Collision Detect signal internally generated.

(Works for a transceiver that does not feed back the transmitted signal on the receive pair).

Byte 11: MIN-FRM-LEN Minimum number of bytes in a frame. Frames shorter than the MIN FRM LEN will be treated as bad frames.

4.3.1 CONFIGURATION DEFAULTS

The reset configures the 82586 to be compatible with the Ethernet specifications:

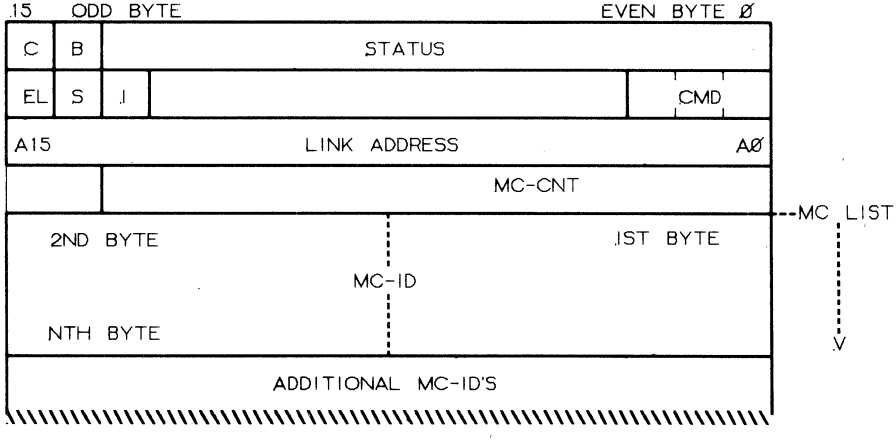
FIFO LIMIT	=8
SRDY/ARDY	=0
SAVE BAD FRAME	=0
ADDRESS LENGTH	=6
ADDRESS/CONTROL	=0
FIELD LOCATION	=0
INT LOOPBACK	=0
EXT LOOPBACK	=0
LINEAR PRIORITY	=0
EXPONENTIAL PRIORITY	=0
EXPONENTIAL BACKOFF METHOD	=0
INTERFRAME SPACING	=96

SLOT TIME	=512
PROMISCUOUS MODE	=0
BROADCAST DISABLE	=0
MANCHESTER/NRZ	=0
TRANSMIT ON NO CRS	=0
NO CRC INSERTION	=0
CRC-16/CRC-32	=0
BITSTUFFING/EOC	=0
PADDING	=0
CRS FILTER	=0
INTERNAL CRS	=0
INTERNAL CDT	=0
CDT FILTER	=0
MIN FRAME LENGTH	=64
PREAMBLE LENGTH	=2
NUMBER OF RETRIES	=15

4.4 MULTICAST ADDRESS SET UP

This command is used to load the 82586 with the Multicast-ID's that should be accepted. This command resets the current filter and reloads it with the specified Multicast-ID's.

The format of the Multicast Address Set Up command is:



where:

LINK ADDRESS, EL, B, C, I, S - As per standard CB's (see Sec. 2.4.2)

STATUS - Bits 12, 13 as per standard CB's (See Sec. 2.4.2).

CMD - The MULTICAST ADDRESS SET UP command value: 3H.

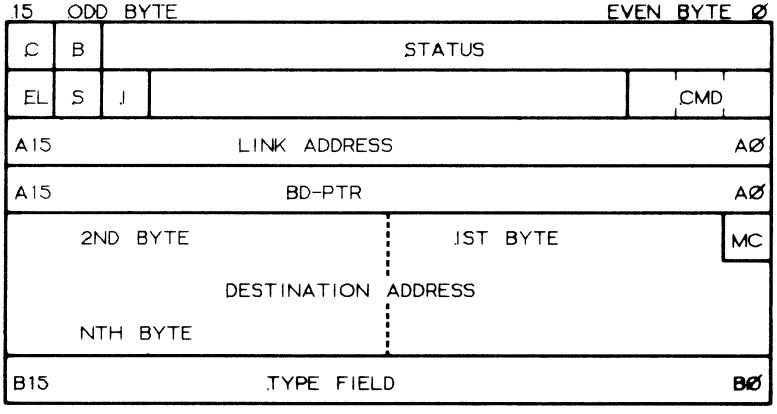
MC-CNT - This 14 bit field indicates the number of bytes in the MC LIST field. The MC-CNT used, must be a multiple of the ADDR-LEN, otherwise, the 82586 truncates the MC-CNT to the nearest ADDR-LEN multiple. MC-CNT = 0 implies reset of the HASH TABLE which is equivalent to disabling of the Multicast filtering mechanism.

MC LIST - A list of Multicast Addresses to be accepted by the 82586. The least significant bit of each MC address must be '1'. Note, the list is compacted, i.e. the most significant byte of an address is immediately followed by the least significant byte of the next address.

4.5 TRANSMIT

This command is used to transmit a frame of user data onto the serial link.

The format of a transmit command is:



where:

LINK ADDRESS, EL, C, B, S, I - As per standard CB's (see Sec. 3.4.2)

STATUS - Defined bits are:
Bits 12, 13 as per standard CB's (See Sec. 2.4.2).

Bit 10: No Carrier Sense signal during transmission. Carrier Sense signal is monitored from the end of Preamble transmission until the end of Frame Check Sequence for TONO-CRS =1 (Transmit On No Carrier Sense Mode) it indicates that transmission has been executed despite CRS non-existance. For TONO-CRS=0 (Ethernet) mode, this bit also indicates unsuccessful transmission (transmission stopped when lack of Carrier Sense has been detected).

Bit 9: Transmission unsuccessful (stopped) due to Lost of Clear To Send signal.

Bit 8: Transmission unsuccessful (stopped) due to DMA Underrun, i.e. data not supplied from the system for transmission.

Bit 7: Transmission Deferred, i.e. transmission was not immediate due to 82586 deferring transmission as a result of previous link activity.

Bit 6: Heart-Beat Indicates, that after previously performed transmission, and before the recently performed transmission, (Interframe Spacing) CDT signal was monitored being active. This indicates that the Ethernet Transceiver Collision Detect Logic performs well.

The Heartbeat is monitored during the Interframe Spacing Period.

Bit 5: Transmission attempt stopped due Too Many Collisions. This happens if the number of retries is exhausted.

Bits 3-0 Number of Collisions experienced by recently transmitted frame.

CMD - The TRANSMIT command: 4H.

BD-PTR - The offset portion of the address of the first TBD containing transmit data. BD-PTR = OFFFFH indicates no TBD is used.

DESTINATION-ADDRESS - Contains the Destination Address for the frame. The least significant bit (MC) indicates the address type:
MC = 0: Individual Address
MC = 1: Multicast or Broadcast Address.
If the Destination Address bits are 'ALL Ones', this is a Broadcast Address.

TYPE-FIELD - The contents of this field are user defined.

NOTES:

1. The DESTINATION-ADDRESS and the TYPE-FIELD are packed i.e. the TYPE-FIELD's least significant byte follows immediately the DESTINATION-ADDRESS's most significant byte.

2. The DESTINATION-ADDRESS and TYPE-FIELD are not used when the 82586 is configured to AC-LOC=0.

3. For AC-LOC=1 transmit buffers shorter than ADDR-LEN are invalid. The transmission will be aborted by DMA Underrun.

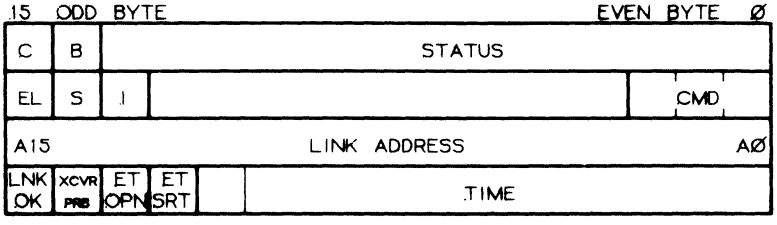
4. Frames which are aborted in the middle of transmission (can result from any reason indicated by any of the STATUS bits 8,9,10, and 12) are jammed.

5. JAMMING RULES:
   a. Jamming will not start before completion of preamble transmission.
   b. Collision detected during transmission of the last 11 bits will not result in jamming.
      If the collision is detected during the transmisson of the last bit or later, the collision will not be reported and retransmission will not take place. This may happen for invalid frame which is shorter in length than the Slot Time.

4.6 TDR

This command performs a Time Domain Reflectometer test on the serial link. By performing the command, the user is able to identify shorts or opens and their location. Along with transmission of 'All Ones', the 82586 triggers an internal timer. The timer measures the time elapsed from transmission start until 'echo' is obtained. 'Echo' is indicated by Collision Detect going active or Carrier Sense signal drop.

The TDR command format is :



where:

LINK ADDRESS, EL, B, C, I, S - As per standard CB's (see Sec. 2.4.2)

STATUS - Bits 12, 13 as per standard CB's (See Sec. 2.4.2)

CMD - The TDR command. Value: 5H.

TIME - An 11 bit field that specifies the number of TxC cycles that elapsed before 'echo' was observed. 'All Ones' indicates no echo.

Note, due to the network consisting of various elements as transceiver links, transceivers, Ethernet, repeaters etc, the TIME is not exactly proportional to problem distance.

The accuracy of problem location is 0.5Vs/fs where :

Vs - the wave propogation speed on the link
fs - the serial clock frequency

LNK-OK (Bit 15) - No link problem identified.
TIME = 7FF H.

XCVR-PRB (Bit 14) - Transceiver Link Problem identified.
LNK-OK =0. TIME = 7FF H.

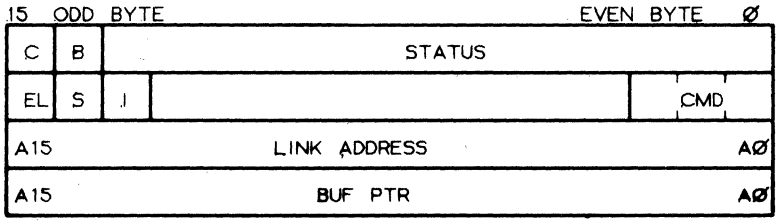
ET-OPN (Bit 13) - Open on the 'Ethernet' link identified LNK_OK = 0.

ET-SRT (Bit 12) - Short on the 'Ethernet' Link identified.
LNK-OK = 0.

4.7 DUMP STATUS

This command causes the contents of various 82586 registers to be placed in memory. It is supplied as an 82586 self diagnostic means plus access to registers of interest to the user.

The DUMP-STATUS command format is:



where:

LINK ADDRESS, EL, B, C, I, S - As per standard CB's (see Sec. 2.4.2)

CMD - The DUMP-STATUS command. Value: 6H.

STATUS - Bits 12, 13 as per standard CB's (See Sec. 2.4.2).

BUF-PTR - This 16-bit quantity specifies the offset portion of the memory address which points to the top of buffer allocated for the dumped registers content.

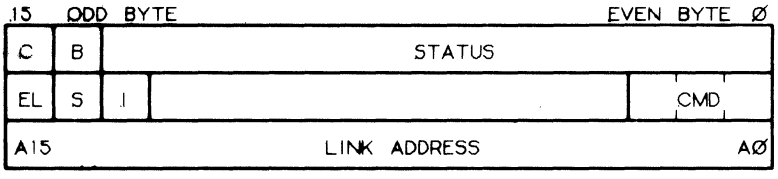
Note: The user of the DUMP-STATUS command, must allocate a 170 byte buffer for this purpose.

4.8 DIAGNOSE

The Diagnose Command checks the internal to the 82586 timer hardware which includes:

* Exponential Backoff Random Number Generator (Free Run Counter).
* Exponential Backoff Timeout Counter.
* Slot Time Period Counter.
* Collision Number Counter.
* Exponential Backoff Shift Register.
* Exponential Backoff Mask Logic.
* Timer Trigger Logic.

The DIAGNOSE Command format is :



where:

LINK ADDRESS, EL, B, C, I, S, - As per standard CB's (see Sec. 2.4.2)

STATUS - Bits 12 and 13 as per standard CB's (See Sec. 2.4.2)

CMD - The DIAGNOSE command. Value: 7H.

The DIAGNOSE is performed in two phases.

PHASE 1

Counters Test

The Free Run, Exponential Backoff Timeout, Slot Time and Collision Counters are checked. Misinterpretation of stuck in state counter as a positive result is avoided by checking the counters when performing transition.

The test is performed in the following steps :

1. All counters are RESET at once.
2. Count.
3. Stop counting when the Free Run Counter (10 bits), Exponential Backoff Counter (10 bits), wrap from 'All Ones' to 'All Zeros'. Simultaneously Slot Time counter switches from 01111111111 to 10000000000 and the collision counter (4 bits) wraps from 'All Ones' to 'All Zeros'.

   Note: Counting is stopped if any of the 3 longer counters wrap, as described above.

4. The 10 least significant bits (if they exist) are checked for being 'All Zeros'.

   If the PHASE 1 passes successfully, this means all the counters count properly, including the Free Run Counter.

PHASE 2

Trigger Logic Test

1. Reset the Exponential Backoff Shift Register, and all the counters.
2. Configure internally the Exponential Backoff logic according to the following :

   SLOT-TIME = 8H
   LIN-PRIO = 2H
   EXP-PRIO = 1H
   BOF-MET = 0H

3. Emulate internally transmission and collision.
4. Is the most significant bit of Exponential Backoff Shift Register '1'? If not, go to Step 3. If yes, continue.
5. Check the Mask Logic output for being 'All Ones' (the Free Run Counter is 'All Ones' at this point and the Exponential Backoff Shift Register is also 'All Ones').

If Step 5's result is positive, 'Passed' status is issued, otherwise, 'Failed' status is issued.

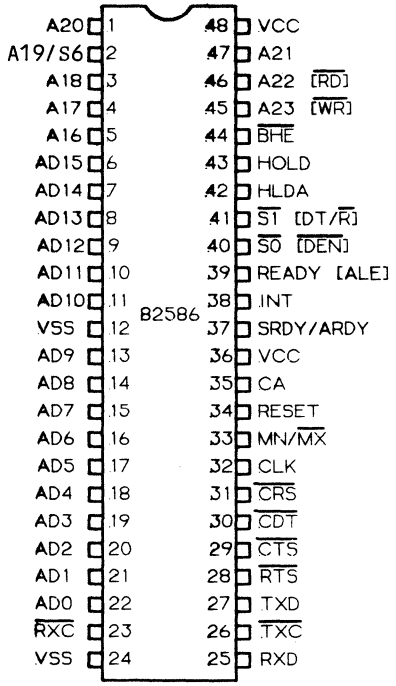
5.0 PIN FUNCTIONS

The 82586 is packaged in a 48 pin DIP. 48 unique pins alone are insufficient to handle the diversity of system configurations and CPU environments that the 82586 will be placed. To facilitate flexibility for the user, the 82586 is equipped in run in a "Maximum Mode" or "Minimum Mode", as controlled by the MN/$\overline{MX}$ pin.

5.1 PINOUT LIST

The 82586 is packaged in Dual In Line (DIP) 48 pin package. The pin description is given in Figure 5.1.

V_{CC}, V_{SS}	-	POWER
MN/$\overline{MX}$	-	STRAPPING
AD_0- AD_{15}	-	ADDRESS/DATA
A_{16}-A_{18}, A_{20}, A_{21}	-	ADDRESS
A_{19}/S_6	-	ADDRESS/STATUS
A_{22} ($\overline{RD}$) *	-	ADDRESS OR READ
A_{23} ($\overline{WR}$) *	-	ADDRESS OR WRITE
$\overline{BHE}$	-	BYTE HIGH ENABLE
READY (ALE) *	-	READY OR ALE
$\overline{S}_0$ ($\overline{DEN}$) *	-	STATUS OR DEN
S_1 (DT/$\overline{R}$) *	-	STATUS OR DT/$\overline{R}$
SRDY/ARDY **	-	SYNCHRONOUS OR ASYNCHORNOUS READY
CLK	-	SYSTEM CLOCK
HOLD, HLDA	-	BUS ARBITRATION
CA, INT	-	HANDSHAKE
RESET	-	RESET
TxC, RxC	-	TRANSMIT AND RECEIVE CLOCKS
TxD, RxD	-	TRANSMIT AND RECEIVE DATA
$\overline{CRS}$	-	CARRIER SENSE
$\overline{CDT}$	-	COLLISION DETECT
$\overline{RTS}$, $\overline{CTS}$	-	SERIAL HANDSHAKE



* STRAPPED OPTION FOR MINIMUM MODE (MN/$\overline{MX}$ 1) THE PIN IS DEFINED AS THE VALUE STATED IN BRACKETS

** PROGRAMMABLE

FIGURE 5.1 82586 (LCC) PINOUT AND THEIR DESCRIPTION

5.2 PIN DEFINITIONS

MN/$\overline{MX}$ (Input)

When HIGH, MN selects $\overline{RD}$, $\overline{WR}$, ALE, $\overline{DEN}$, DT/$\overline{R}$ (Minimum Mode). When LOW, MN selects A22, A23, READY, S0, S1 (Maximum Mode). Note: The pin should be static during 82586 operation.

AD0 - AD15 (Input/Output, 3-State)

These lines constitute the time multiplexed memory address (t_1) and data (t_2, t_3, t_W, t_4) bus. In BYTE MODE the high byte will output the address during the entire cycle. AD0-AD15 are floated after a Reset or when the bus is not acquired.

A16-A18,A20-A23 (Output, 3-State; A22, A23 - Maximum Mode only)

These lines constitute 7 out of 8 most significant address bits for memory operation. They switch during t_1 and stay valid during the entire memory cycle. These lines are floated after RESET or when the bus is not acquired.

A19/S6 (Output 3-State)

During t_1 this pin constitutes line 19 of the memory address. During t_2 thru t_4 the pin is used as a status that indicates that this is a Master peripheral cycle, and is HIGH. Its timing is identical to that of AD0 - AD15 during write operation.

$\overline{BHE}$ (Output, 3-State)

The Bus High Enable signal is used to enable data onto the most significant half of the data bus. Its timing is identical to that of A16-A23. In word mode it is LOW and in byte mode HIGH. Note: After RESET, the 82586 is configured to byte mode. Thus, during the first memory access (to SCP block, SYSBUS byte) BHE = 1.

HOLD (Output)

An active HIGH signal used by the 82586 to request local bus mastership at the end of the current CPU bus transfer cycle, or at the end of the current DMA burst transfer cycle. In normal operation, HOLD drops before HLDA. The 82586 can be forced off the bus by dropping HLDA. In that case HOLD will drop at most three bus cycles after HLDA drop.

HLDA (Input)

An active HIGH Hold Acknowledge signal indicates that the CPU has received the HOLD request and that bus control has been relinquished to the 82586. It is internally synchronized. After HOLD is detected as being LOW, the processor will drive HLDA LOW. Note, IT IS NOT ALLOWED TO CONNECT THE HLDA TO V_{CC}, because it will cause a deadlock. User that wants to give a permanent access to the bus, to the 82586, should connect the HLDA with HOLD. If the HLDA drops before HOLD, then the 82586 will release the bus (by dropping HOLD) at most for three bus cycles. For further details see Sec. 5.3.1.

RESET (Input)

This active HIGH, internally synchronized signal, causes the 82586 to immediately terminate present activity. The signal must be HIGH for at least four clock cycles. 82586 will execute RESET within ten system clock cycles starting from RESET HIGH. When RESET returns LOW, the 82586 waits for the first CA to begin the initialization sequence.

CA (Input)

The CA pin is a Channel Attention input which is used by the higher level intelligence to initiate execution by the 82586 of memory resident Command Blocks. The CA signal is internally synchronized. The signal must be HIGH for at least one system clock period. It is latched internally on HIGH to LOW edge and then detected by the 82586.

The first CA after a RESET will force the 82586 into the initialization sequence beginning at location OFFFFF6H. All subsequent CA's cause the 82586 to begin execution of new command sequences from the relocatable memory address defined during the initialization sequence (the SCB).

INT (Output)

Active HIGH interrupt request signal. For further details see Sec. 5.3.2.

CLK (Input)

The system clock input from the 80186 or another symmetric clock generator. It requires special voltage levels and wave shape as shown in Chapter 8.

READY (Input; Max Mode only)

This active HIGH signal is the acknowledgement from the addressed memory that the transfer cycle can be completed. While LOW, it causes wait states to be inserted. This signal must be externally synchronized with the system clock. The internal to 82586 Ready is a logical OR between READY and SRDY/ARDY.

SRDY/ARDY (Input)

This active HIGH signal performs the same function as READY. If it is programmed at configure time to SRDY, it is identical to READY. If it is programmed to ARDY, the positive edge of the Ready signal is internally synchronized. Note, the negative edge must still meet setup and hold time specifications, when in ARDY mode. The ARDY signal must be active for at least signal system clock HIGH periods for proper strobing. The internal to 82586 Ready is a logical OR between READY (in Maximum Mode only) and SRDY/ARDY. Note: Following the RESET this pin assumes ARDY mode.

$\overline{S0}$, $\overline{ST}$ (Output, 3-State; Max Mode only)

These are the status pins which define the type of DMA transfer during the current memory cycle. They are encoded as follows:

$\overline{ST}$	$\overline{S0}$
0	0 - Not Used
0	1 - Read Memory
1	0 - Write Memory
1	1 - Passive

Status is active from the middle of t_4 to the end of t_2. They return to the passive state (1,1) during t_3 or during t_W when READY or ARDY is HIGH. These signals can be used by the 8288 Bus Controller to generate all memory control and timing signals. Any change from the passive state signals the 8288 to begin the next t_1 to t_4 bus cycle. These pins are pulled HIGH and floated after a system RESET and when the bus is not acquired.

$\overline{RD}$ (Output, 3-State; Min Mode only)

The read strobe indicates that the 82586 is performing a memory read cycle. RD is active LOW during t_2, t_3 and t_W of any read cycle. This signal is pulled HIGH and floated after a RESET and when the bus is not acquired.

$\overline{WR}$ (Output, 3-State; Min Mode only)

The write strobe indicates that the 82586 is performing a write memory cycle. WR is active LOW during t_2, t_3 and TW of any write cycle. It is pulled HIGH and floats after RESET and when the bus is not acquired.

ALE (Output; Min Mode only)

Address Latch Enable is provided by the 82586 to latch the address into the 8282/8283 address latch. It is a HIGH pulse, during the t_1 - 'clock low' time of any bus cycle (see Chapter 8). Note that ALE is never floated.

$\overline{DEN}$ (Output, 3-State; Min Mode only)

Data ENable is provided as an output enable for the 8286/8287 transceivers in a stand-alone (no 8288) system. DEN is active LOW during each memory access. For a read cycle, it is active from the middle of t_2 until the beginning of t_4, while for a write cycle, it is active from the beginning of t_2 until the middle of t_4. It is pulled HIGH and floats after a system RESET or when the bus is not acquired.

DT/$\overline{R}$ (Output, 3-State; Min Mode only)

Data Transmit/$\overline{Receive}$ is used in non-8288 systems that use an 8286/8287 data bus transceiver. It controls the direction of data flow through the transceiver. Logically, DT/R is equivalent to S1. It becomes valid in the t_4 preceding a bus cycle and remains valid until the final t_4 of the cycle. This signal is pulled HIGH and floated after a RESET or when the bus is not acquired.

SERIAL CHANNEL SIGNALS:

TxD (Output)

Transmitted Serial Data output signal will be HIGH (marking) when not transmitting.

$\overline{\text{TxC}}$ (Input)

Transmit data clock provides timing information to the internal serial logic depending upon the mode of data transfer. For NRZ mode of operation, data is transferred to the TxD pin on the HIGH to LOW transition of the clock. This signal input has special voltage levels and waveshape characteristics (see Chapter 8).

RxD (Input)

Received data input signal input has special voltage levels and waveshape characteristics (see Chapter 7).

$\overline{\text{RxC}}$ (Input)

Received data clock signal provides timing information to the internal shifting logic depending upon the mode of data transfer. For NRZ data, the state of the RxD pin is sampled on the HIGH to LOW transition of the clock. This signal input has special voltage levels and waveshape characteristics (see Chapter 8).

$\overline{\text{RTS}}$ (Output)

A Request To Send signal when LOW, notifies an external interface that the 82586 has data to transmit. It is forced HIGH after a Reset and when the Transmit Serial Unit is not sending data.

$\overline{\text{CTS}}$ (Input)

The active LOW Clear To Send input enables the 82586 transmitter to actually send data. It is normally used as an interface handshake to RTS. Dropping this signal stops the transmission. It is internally synchronized. If the CTS goes inactive, meeting the setup time to TxC negative edge, the transmission will be stopped and the RTS will drop within, at most, two TxC cycles.

$\overline{\text{CRS}}$ (Input)

The active LOW Carrier Sense input is used to notify the 82586 that there is traffic on the serial link. It is used only if the 82586 is configured for external Carrier Sense. When so configured, external circuitry is required for detecting serial link traffic. It is internally synchronized. In order to be accepted, the signal must stay active for at least two serial clock cycles (for CRSF =0).

$\overline{\text{CDT}}$ (Input)

The active LOW Collision Detect input is used to notify the 82586 that a collision has occurred. It is used only if the 82586 is configured for external Collision Detect. External circuitry is required for detecting the collision. It is internally synchronized. In order to be accepted, the signal must stay active for at least two serial clock cycles (for CDTF = 0).

5.3 82586/CPU BUS ARBITRATION & HANDSHAKE CONVENTIONS

5.3.1 HOLD/HLDA BUS ARBITRATION

Figure 5.2 describes the 82586 HOLD pin behavior as driven by internal and external events.

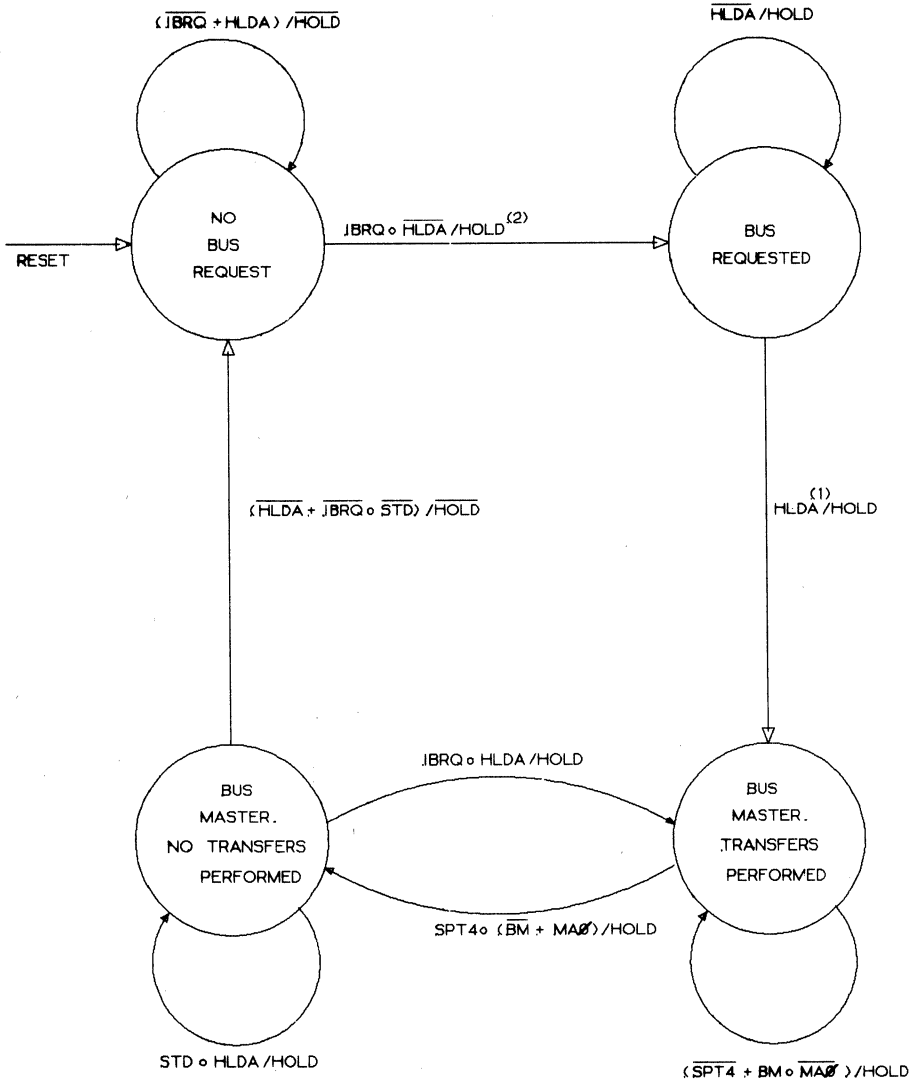


FIGURE 5.2

The following defines the states and exitations of the state diagram :

STATES:

NO BUS REQUEST:	The 82586 is not requesting the bus via HOLD, because Internal Bus Request (IBRQ) is not pending, or when the IBRQ arrived the HLDA level was HIGH.
BUS REQUESTED:	The 82586 has issued HOLD HIGH (bus request). HLDA is LOW i.e. bus was not yet granted.
BUS MASTER/TRANSFERS PERFORMED:	The 82586 owns the bus and performs transfers.
BUS MASTER/NO TRANSFERS PERFORMED:	The 82586 owns the bus, but not uses it for transfers. This is used by the 82586 to lock the bus for few system clock cycles for READ/MODIFY/WRITE operations, or when the 82586 knows that it will need the bus soon (e.g. when buffer switching occurs).

EXITATIONS

RESET:	Software or hardware Reset.
IBRQ:	Internal Bus Request. Any internal demand to perform bus transfers on the bus- e.g. Receive or Transmit DMA, CU or RU issued requests.
STD:	Special state different from t_1, t_2, t_3, t_W and t_4, for which the 82586 masters the bus, but no transfers are performed (ALE, $\overline{RD}$, $\overline{WR}$, are inactive in Minimum Mode or $\overline{S_0}$, S_1 are passive in Maximum Mode).
SPT4:	State prior to t_4. May be t_3 for zero wait states or the last TW for any number of wait states.
BM:	Byte Mode (SYSBUS = 01H).
MAO:	Memorized AO. AO was true during the last t_1 (Even-Address bus cycle).

NOTES:

1. HLDA should be at least HIGH for one system clock period in the case where HOLD/HLDA are synchronous to the 82586 system clock.

2. The HOLD signal will stay LOW for at least two system clock periods after it drops.

5.3.2 CA/INT HANDSHAKE

The 82586/CPU handshake is performed by the Channel Attention and Interrupt pair and a set of bits in the SCB.

Thus, the STAT bits in the SCB Status word:
CX, FR, CNR and RNR (See Sec. 2.3) define the interrupt cause. Similarly, the ACK bits in the SCB command word : ACK-CX, ACK-FR, ACK-CNR and ACK-RNR define which interrupt cause has been given the CPU's attention.

The 82586/CPU handshake is a combination of hardware signalling and setting/resetting the STAT and ACK bits:

1. The 82586 sets the STAT field, the bit/s which describe the interrupt cause.

2. The 82586 issues an INT HIGH. The INT stays HIGH until the 82586 notifies CA.

3. INT HIGH grabs CPU's attention. The CPU reads the STAT field.

4. After handling one or more interrupt reasons, CPU sets the appropriate bit/s in the ACK field.

5. CPU issues a CA signal.

6. Upon sensing the CA, the 82586 reads the ACK field.

7. The INT drops to LOW.

8. New STAT is prepared based on clearing the serviced interrupts (since it is possible that not all were serviced, therefore, it is possible that not all are cleared) and ORing them with new requests.

9. The new STAT field is written in the SCB and the ACK field is cleared.

10. INT is reissued (HIGH) if one of the STAT bits is one.

Note, since the INT signal drops LOW, every CA is later reissued if necessary. The INT is suitable for triggering dc level interrupt controllers and edge triggered controllers as well.

6.0 82586 - BASED SYSTEMS

6.1 PHYSICAL CONFIGURATION

The 82586 can operate on the local bus of the host CPU as an alternate bus master with common status lines. Because the status lines are common, all local bus resources can be shared (Clock Generator, 8288 Bus Controller, Address Latches and Data Transceivers). The interface is optimized for use with an 80186. The 82586 can be used with an 80286 in dual-ported memory configurations using the 8207 Dynamic RAM Controller. The 82586 can also be used with an 8086/88, or 8085 using the Multibus.

All bus timing and loading specifications are consistent with those of the 80186 system, and are provided in Section 8.

The 82586 CLK signal input must receive MOS level inputs. The 82586 can work with an 80186 or a 10 MHz 8086 using an 8 MHz 50% duty cycle clock (full performance), or with a 5 MHz 8086 using a 5 MHz 30% duty cycle clock (reduced performance).

System examples are provided in Section 6.4.

6.2 MEMORY ADDRESSING AND ORGANIZATION

The 82586 addresses memory as a linear sequence of 16Mbytes. It automatically establishes transfers as high-byte-only or double-byte when used with an 8086/80186/80286 or as single-byte-only for use with an 8088 or other 8-bit processors.

As a Master Peripheral with the 8088, the 82586 treats memory as a single bank (D7-D0) of 1M 8-bit words addressed by address lines A19-A0. Address lines A23-A20 and $\overline{BHE}$ are not used.

When operating with the 8086/80186, the 82586 treats memory as a high bank (D15-D8) and a low bank (D7-D0) of 512K 8-bit words addressed in parallel by A19-A1. The 82586 provides two enable signals, $\overline{BHE}$ and A0, to selectively allow reading/writing to either an odd byte location or a full word location. Byte transfers with even addresses (A0=LOW, $\overline{BHE}$=HIGH) on D7-D0 are not allowed to occur. Odd addressed byte transfers (A0=HIGH, $\overline{BHE}$=LOW) occur on D15-D8. Word transfers (A0=LOW, $\overline{BHE}$=LOW) are restricted to even addressing. Thus, for maximum performance, operands are constrained to be arranged with the least significant byte located at an even address.

The following table summarizes the operation of $\overline{BHE}$ and A0:

$\overline{BHE}$	A0	
0	- 0	Whole word
0	- 1	Upper byte from/to odd address
1	- 0	Not applicable
1	- 1	Not applicable

When operating with the 80286, the full 16M byte address space is available. It has the same characteristics and restrictions as for the 8086/80186.

6.3 BUS OPERATION

Each memory transfer cycle consists of at least four CLK cycles. These are referred to as t_1, t_2, t_3 and t_4. The address is generated by the 82586 beginning at t_1, and data transfer occurs on the bus during t_2 through t_3. In the event that a 'READY' indication is not received from the addressed memory, 'WAIT' states (t_W) are inserted between t_3 and t_4. Each inserted 'WAIT' state is of the same duration as a CLK cycle.

The 82586 outputs status ($\overline{ST}$ and $\overline{SO}$) to provide type-of-memory-cycle information to the 8288 Bus Controller in Maximum Mode or in Multibus Configuration. The 8288 generates the memory read and write commands, and issues control signals to the address buffers and data transceivers. The 82586 provides $\overline{RD}$, $\overline{WR}$ and ALE signals for memory transfers in Minimum Mode. A multi-master system bus can be constructed with the use of the 8289 Bus Arbiter. The key arbiter inputs are the same as those for the 8288: local status lines S1 and S0.

The operation of the 82586 is structured so that all command, status and data flow is via memory. Therefore, the S2 status line is not required and is not provided by the 82586. No provision is made for transfer to any fixed address system resource (I/O or memory). Addresses always increment sequentially.

6.3.1 READ

The read cycle begins at t_1 with the generation of the address. The memory read command signal (MRDC from the 8288) is asserted. This read command causes the addressed device to enable its data bus drivers onto the system bus. Some time later valid data will drive the READY line HIGH. When the read command returns to the HIGH level, the addressed device will again tri-state its data bus drivers. If a transceiver (8286/8287) is required to buffer the local bus, the direction (DT/$\overline{R}$) and enable ($\overline{DEN}$) controls are provided by the 8288 Bus Controller (or from the 82586).

6.3.2 WRITE

A write cycle begins with the generation of the address during t_1. At t_2 the processor generates the data to be written. This data remains valid until the middle of t_4. During t_2, t_3 and t_W, the advanced memory write command from the 8288 (AMWTC) is asserted, while the normal memory write command ($\overline{MWTC}$) is asserted during t_3 and t_W only. The latter command is used by older memories that require valid data prior to the write command.

6.4 SYSTEM CONFIGURATIONS

6.4.1 80186 ELEMENTARY MAXIMUM MODE SYSTEM

SYSTEM INTERFACE

This is a highly recommended communication system configuration (See Figure 6.1). Since the 82586 pinout has been optimized for a 80186 microprocessor bus; there is only one additional TTL package to integrate the 82586 in an 80186 system. The 82586 is configured to Maximum Mode by strapping the MN/$\overline{MX}$ pin to ground. In this mode the 82586 generates status signals that will be used for bus control signal generation.

The 82586 is clocked by the CLKOUT signal generated by 80186. Thus, the already existing address latches, data transceivers and bus controller can be shared by the CPU and the 82586.

The 80186, 82586, S0, S1, are wired together, driving the 8288 bus controller. Since the 8288, $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ inputs sustain at HIGH, the S0, S1 and S2 lines whenever the 80186 and the 82586 corresponding outputs are tristated, therefore, there is no need for external pull up resistors on these lines. NOTE: S2 8288 input is driven only from the 80186. This status is not generated by the 82586 because it accesses memory only (no I/O). The S0, S1 and S2 are used by the 8288 to generate a full set of standard bus control signals.

The shared data bus of the 80186 and the 82586 is sixteen bits wide. The system memory can be accessed either by the 80186 or by the 82586 at once. Bus arbitration is resolved by the HOLD/$\overline{HLDA}$ signal pair. The CPU grants the bus to the 82586 by issuing the HLDA HIGH as a response to bus request from the 82586 (HOLD HIGH). The CPU is able to withdraw its bus grant by dropping HLDA low. In this case the 82586 will release the bus within a maximum three memory cycles (see 5.3.1).

It is not recommended that the CPU take away HLDA during transmission or reception because there will be a high chance of frame abortion by underrun or overrun respectively.

Communication on the task level between the CPU and the 82586 is accomplished by a shared system memory mailbox and the CA/INT handshake. For details See 5.3.2.

It is possible to create a multimaster system by using the 8289 bus arbiter . It is suggested, that in these systems, the 82586 communication node is assigned the highest priority. This will ensure a minimum bus latency for the 82586 whenever it needs the bus, thus avoiding waste of bus bandwidth by underrun or overrun frames.

To support Ethernet, 10Mbps rate and 9.6 microseconds Interframe Spacing, it is sufficient to operate at 8MHz system clock and zero wait state bus cycles.

Also lower rates and slower memories (that introduce wait state) are possible in Ethernet systems.

SERIAL INTERFACE

Figure 6.1 displays an Ethernet Serial Interface.

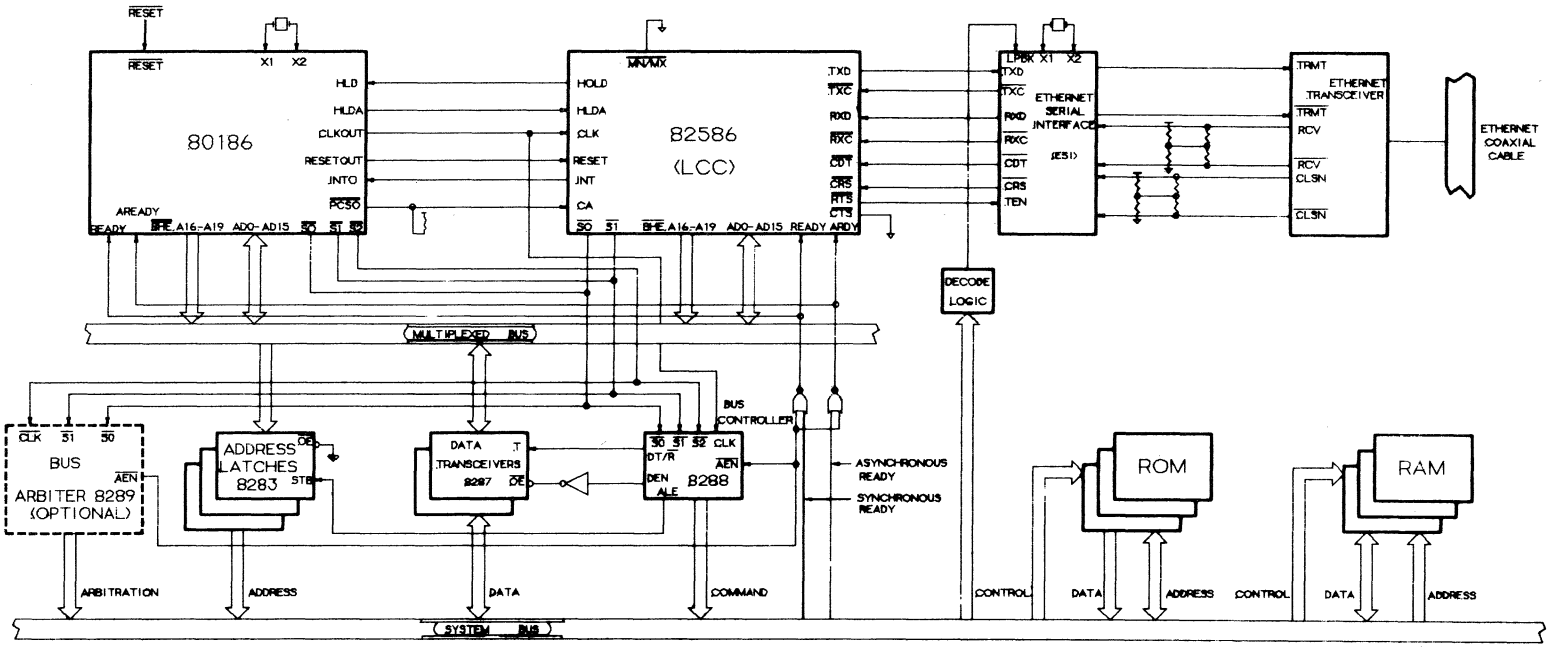


FIGURE 6.1: 80186 ELEMENTARY MAXIMUM MODE SYSTEM

6.4.2 8086 ELEMENTARY MAXIMUM MODE SYSTEM

SYSTEM INTERFACE

This system (Figure 6.2) is similar in performance to the 80186 Elementary Maximum Mode System. However, some extra TTL logic must be externally added. There is a need for :

* HOLD/HLDA - RQ/$\overline{GT}$ converter: This logic bridges over the incompatible 8086 and 82586 bus arbitration protocols. A complete TTL based design that performs this function is given in Figure 6.3. A Local Bus Arbiter (LBA) device will be available from Intel, integrating of this logic into a single 20 pin DIP device.

* 8259A Programmable Interrupt Controller (PIC): This device generates the interrupt vector for the 8086 which initiates the 8086 execution of 82586 interrupt service routine.

* 82285 Clock Generator: This device generates an 8MHz Symmetric Clock for the 8086-1 as well as for the 82586. NOTE: the 10MHz 8086-1 is absolutely necessary, since the 8086 has been optimized for 33% duty cycle clock. Therefore, only 10MHz 8086 can run on 8MHz 50% duty cycle clock. The 82285 Clock Generator also generates RESET and READY signals for the 8086-1/82586 system.

* Channel Attention Decode Logic: This simple logic generates the CA signal based on 8086-1 delivered address and control signal.

The Maximum Mode configuration is achieved by strapping to ground the MN/$\overline{MX}$ pins of the 8086-1 and the 82586. In all other aspects, the system interface is similar to the one described in Section 6.2.1.

Similar but lower performance system is possible by using a 5MHz 8086. The system configuration is the same as the one in Figure 6.2, except for the 8284A clock generator that replaces the 8285 clock generator. This system runs on a 5MHz/33% duty cycle clock. Thus, an 8MHz 82586 must be used to be able to run on a 5MHz non-symmetrical clock.

SERIAL INTERFACE

For Ethernet the serial interface is described in Sec. 6.3.

6.4.3 STANDALONE MULTIBUS® SYSTEM

SYSTEM INTERFACE

It is possible for an 82586 CPU system to share a memory interface via the Multibus (see Figure 6.4). The Multibus is the Intel's standard bus structure which allows Intel's board products to communicate. Standard address latches, data transceivers and a bus controller are needed in order to interface to a demultiplexed Multibus.

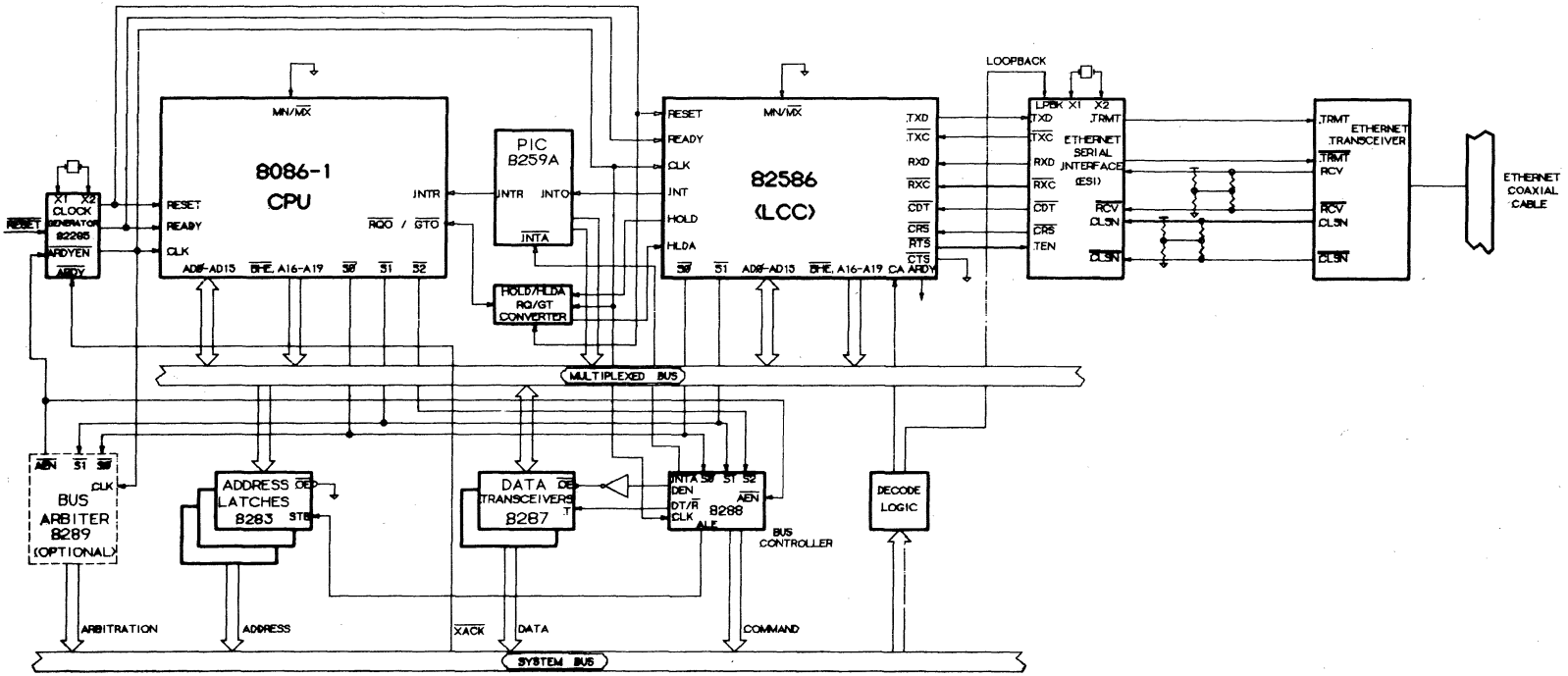


FIGURE 6.2: 8086 MAXIMUM SYSTEM

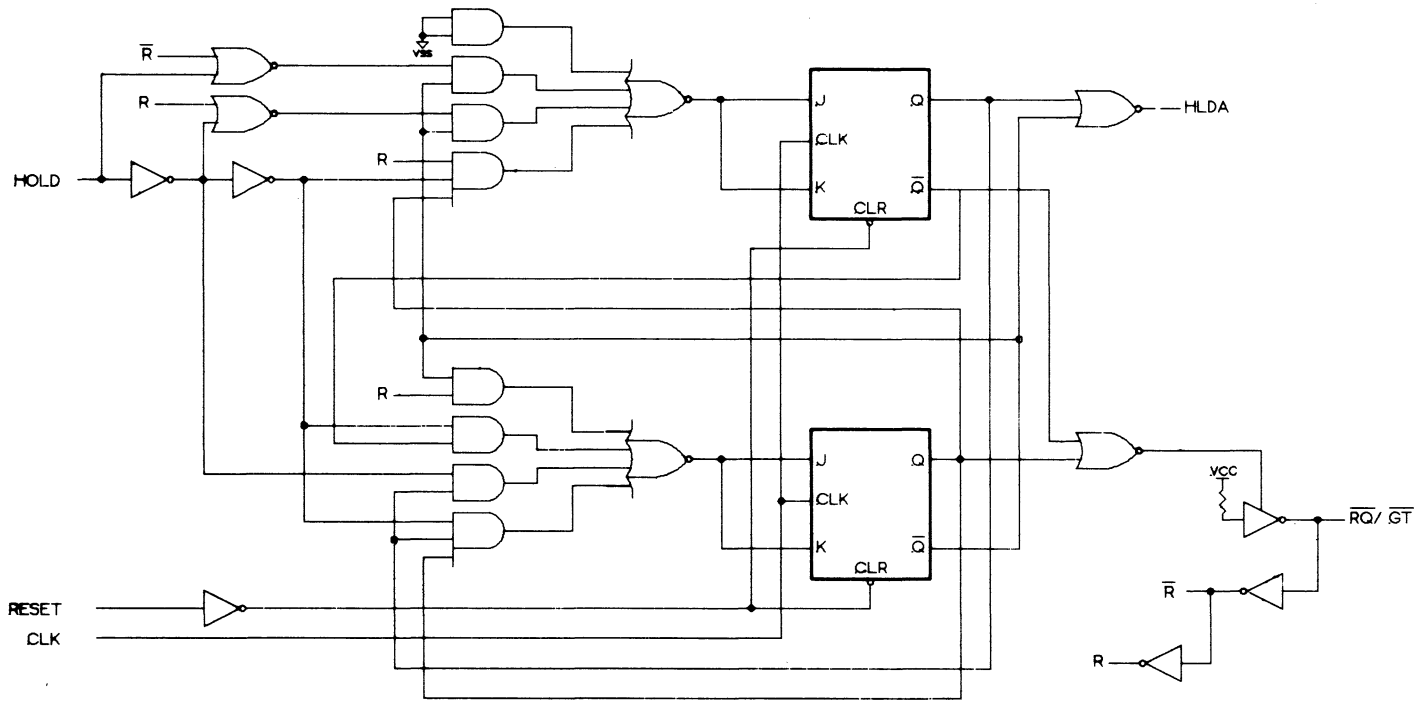


FIGURE 6.3: THE TTL HOLD/HLDA RQ/GT CONVERSION LOGIC

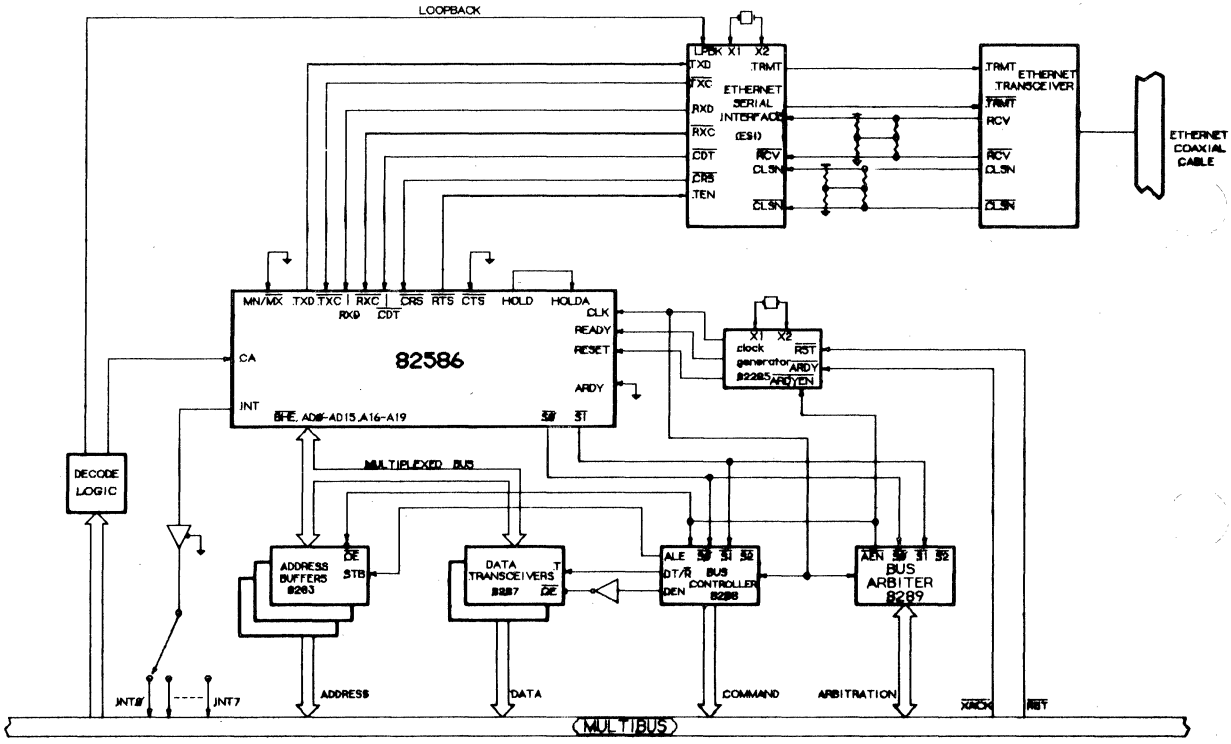


FIGURE 6.4 82586 STAND ALONE MULTIBUS® INTERFACE

Bus Arbiter 8289 is needed, in order to resolve Multibus arbitration. It is recommended to assign the 82586 system the highest priority in order to handle efficiently the Ethernet communication tasks. INTO - the highest priority interrupt request on the Multibus, is used in order to grab remote CPU's attention to a completed communications task.

6.4.4 DUAL PORTED RAM-BASED SYSTEM

SYSTEM INTERFACE

When operating at 10Mbps serial bit rate, the 82586 may utilize a significant percentage of bus bandwidth, thus leaving insufficent bus bandwidth for other than data communication purposes. When the 82586 bus bandwidth utilization is intolerable, use of a dual ported memory system, with one port dedicated to the 82586, is recommended. Since the 82586 is separated from the CPU, both can perform their tasks concurrently i.e. when the 82586 accesses the dual ported memory on one port, the CPU can access any other peripheral on the other.

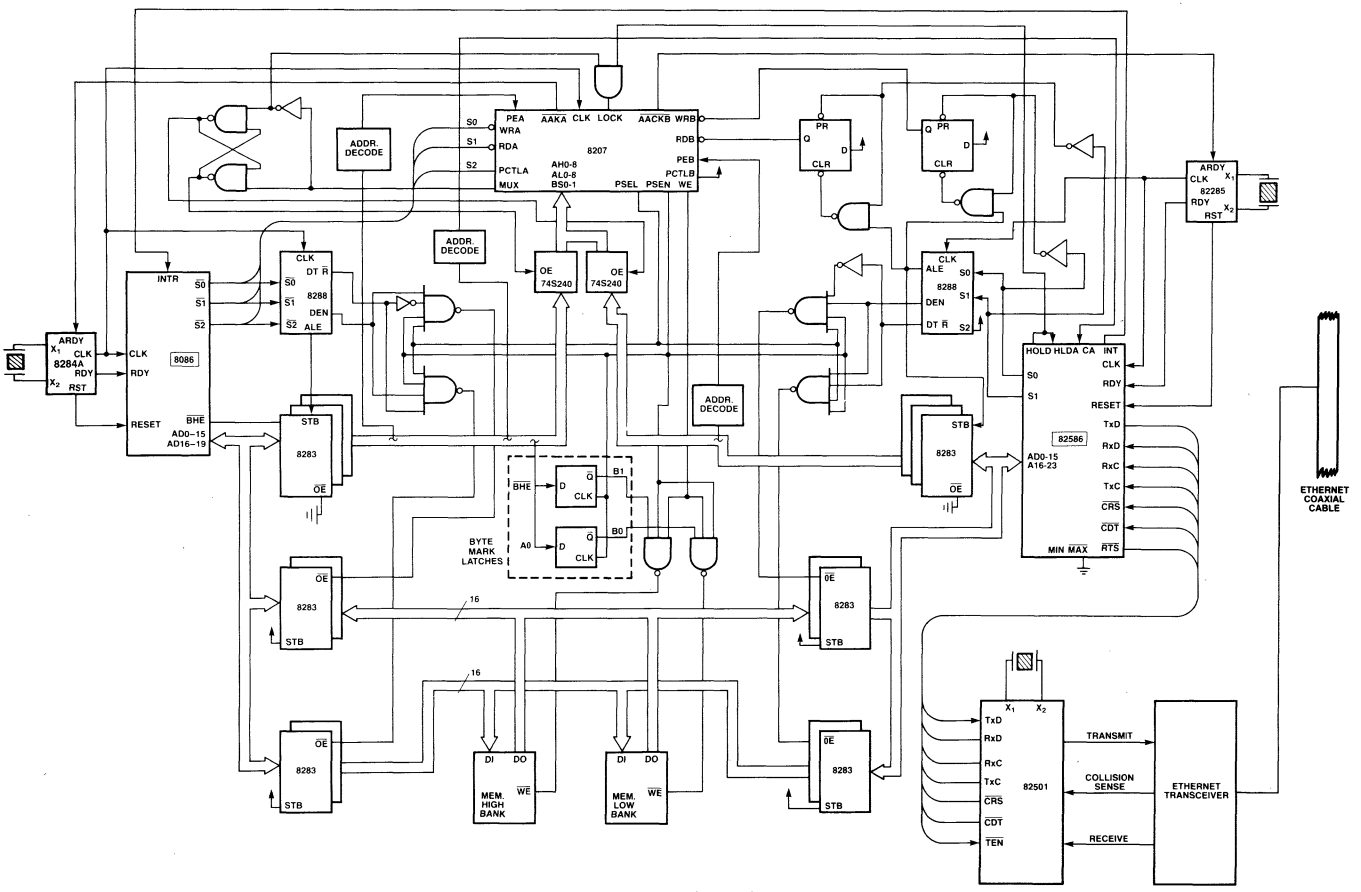
Figure 6.5 displays a typical dual ported memory based system.

Standard dynamic RAMs and the 8207 DRAM CONTROLLER are the dual ported RAM basic building blocks. The 8207 provides not only dynamic RAM refresh ($\overline{RAS}$ and $\overline{CAS}$), but also arbitrates between each of the process requests and directs data to or from the appropriate port.

The dual ported RAM consists of two memory banks (LOW and HIGH), eight 8283 latches, their steering logic (four NAND gates plus two inverters), 8207, a MUX, and a memory read/write control logic (BYTE MARK LATCHes plus two NAND gates. The port is selected to read/write from/to the memory via PSEL, PSEN 8207 generated signals and $\overline{DEN}$ signals generated by both ports systems. The LOW or HIGH bank is selected by the BYTE MARK LATCH (driven by AO, $\overline{BHE}$ and PSEN). The transfer direction (read or write) is selected via the WE signal from the 8207 and DT/R signals generated by both port systems. The port arbitration is provided by the 8207, that is strobing-in both port addresses via a MUX and outputs the presently selected port address.

The strobed-in address is chosen by the 8207 generated MUX signal. Once the processor commanded transfer is executed, an $\overline{XACK}$ signal is issued by the 8207 to acknowledge transfer completion. As shown in Figure 6.5 configuration, the 82586 has absolute control of the dual ported memory, immediately after issuing the HOLD signal. This is accomplished by the 8207 LOCK signal driven by the 82586 HOLD.

The 82586 port system shown in Figure 6.5 is similar to the MULTIBUS standalone configuration. Thus, a dedicated 82285 Clock Generator is needed on the 82586 port. NOTE: If a 22 bit address space is sufficient, the 82586 can be configured to Minimum Mode (strapping the MN/$\overline{MX}$ pin to VCC). In this mode, the 82586 generates directly the DEN and DT/R signals, thus saving the 8288 Bus Controller.



8256–8086 DUAL PORT CONFIGURATION

SN11–22

The CPU port system is represented by a block which drives demultiplexed address, data and command buses, plus two I/O ports that generate the $\overline{CS}$ and LPBK signals. It is the user's responsibility to build around a microprocessor a CPU system that matches with this CPU definition.

6.4.5 8088 ELEMENTARY MAXIMUM MODE SYSTEM

SYSTEM CONFIGURATION

This system is similar to the 8086 system shown in Figure 6.2. There are a few differences:

* The data bus is 8 bit wide (82586 must be configured to byte mode).
* The 8086-1 is replaced by the 8088.
* The 82285 Clock Generator is replaced by the 8284A Clock Generator.

The whole system runs on 5MHz 8088 non-symmetrical clock. However, on 8MHz 82586 must be used.

SERIAL INTERFACE

Since the system byte transfer rate is only around 30% of the maximum performance systems, this configuration is not recommended for Ethernet. This configuration is practically applicable for CSMA/CD networks that operate at less than 3Mbps serial bit rate, having no restrictions on the 82586 memory structure. With some restrictions on the 82586 memory structure (e.g. buffers large enough to contain a full frame) higher bit rates but not 10Mbps can be supported.

6.4.6 8085-BASED ELEMENTARY MINIMUM SYSTEM

SYSTEM INTERFACE

This is a highly recommended non-Ethernet lower serial bit rate configuration. With four devices (8085, 82586, 8185-2 and 8355-2) plus some buffers and discrete components, one can build a low cost system as in Figure 6.6 containing:

* 256 Bytes of RAM
* 2K Bytes of ROM
* 38 I/O pins
* 4 Interrupt Levels
* 1 Timer
* 1 CSMA/CD serial channel
* 1 Low-rate asynchronous serial channel
* 1 General purpose CPU.

This system is very efficient for low-end applications, e.g.: a supermarket cash register network. The 82586 is configured to minimum mode by strapping the MN/$\overline{MX}$ pin to VCC and to byte mode (SYSBUS = 01H). In this mode, the 82586 can be wired with the appropriate 8085 address, data and control signals.

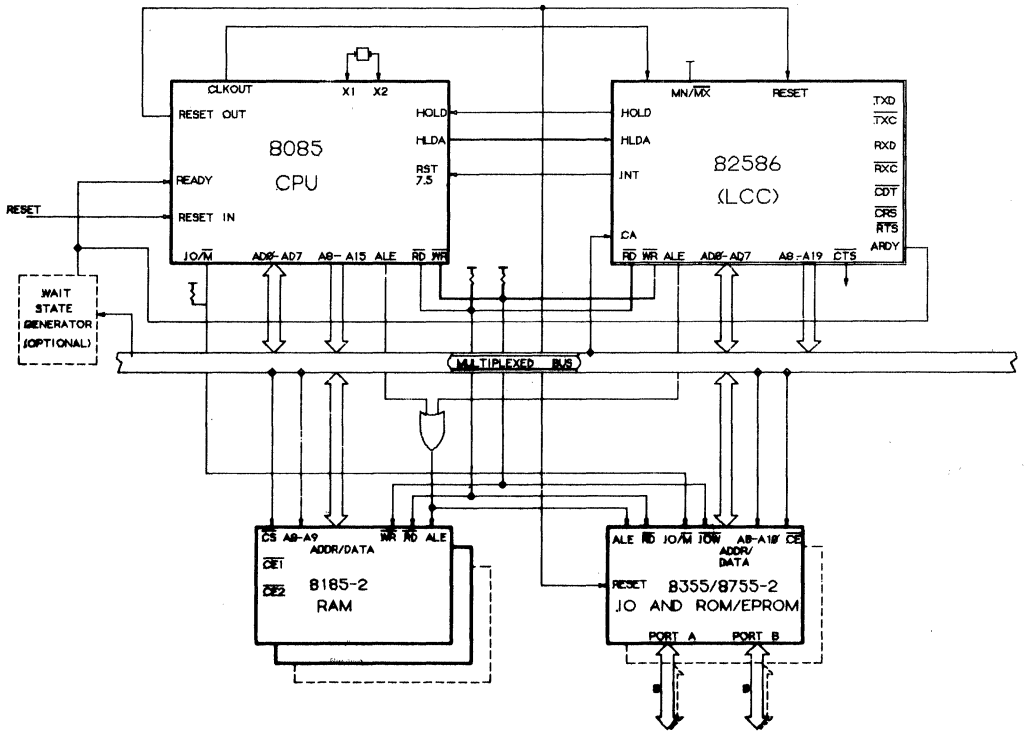


FIGURE 6.6: 8085 BASED ELEMENTARY MINIMUM SYSTEM

Since the 8185-2 and the 8355-2 (or 8755-2) internally demultiplex address and data, no external data external data latches and transceivers are needed. The whole system bus is clocked by a 5MHz clock generated by the 8085. Since this clock is symmetrical, a 5MHz 82586 (lower cost) may be used.

SERIAL INTERFACE

The restrictions on this system serial interface are similar to Sec. 6.4.5 system.

7.0 SERIAL INTERFACE

7.1 DATA ENCODING SUPPORT

The 82586 implements NRZ encoding. Manchester encoding is also supported because it has significant advantages over NRZ when considering DC levels, maximum data rate, and the elimination of the need for clock busing.

The encoding technique is specified by NRZ/MANCH in the CONFIGURE COMMAND parameter table.

7.1.1 NRZ

7.1.1.1 TRANSMISSION

Internally the 82586 shifts the data out from an 8-bit parallel input shift register. The data is shifted out at a 1x baud rate synchronous to $\overline{TxC}$. Data is shifted out on the falling edge of the $\overline{TxC}$, as shown in Figure 7.1.

The encoding methods chosen for the 82586 allow some tradeoffs between hardware cost and speed. Other types of user defined encoding methods can be employed using the NRZ mode of operation with $\overline{TxC}$ and $\overline{RxC}$ being presented to the 82586 by some external encoding logic.

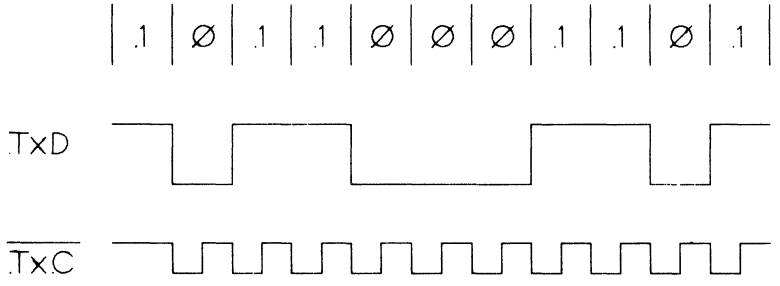


FIGURE 7.1 NRZ WAVEFORM RELATIVE TO $\overline{TxC}$

7.1.1.2 RECEPTION

Received data is synchronously sampled and shifted into the 82586 on the falling edge of $\overline{RxC}$. The data is sampled exactly in the second half of the bit cell (for a 50% duty cycle clock) (Figure 7.2). The $\overline{RxC}$ line must be clean from glitches, otherwise unpredictable actions may result.

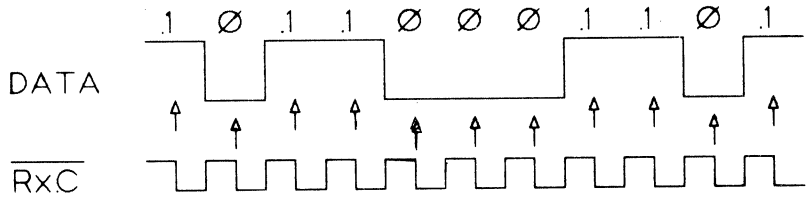


FIGURE 7.2: NRZ RELATIVE TO $\overline{RxC}$

7.1.2 MANCHESTER

Manchester encoding is a binary signaling mechanism that combines data and clock into 'bit-symbols'. Each bit-symbol is split into two halves with the second half containing the binary inverse of the first half a transition always occurs in the middle of each bit-symbol.

During the first half of the bit-symbol, the encoded signal is the logical complement of the bit value being encoded. During the second half of the bit symbol, the encoded signal is the uncomplemented value of the bit being encoded. An example of Manchester waveform is shown in Figure 7.3.

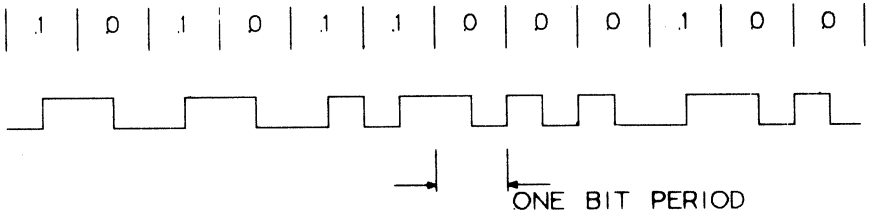


FIGURE 7.3: AN EXAMPLE OF MANCHESTER ENCODED DATA

When configured to Manchester (via CONFIGURE), the 82586 is capable of transmitting a Manchester encoded data. However, it still receives NRZ encoded data. At lower than 10Mbps bit rates a simple external hardware is required to support Manchester data reception.

7.1.2.1 TRANSMISSION

Figure 7.4 shows an example of Manchester encoded data as transmitted by the 82586 relative to the TxC pin.

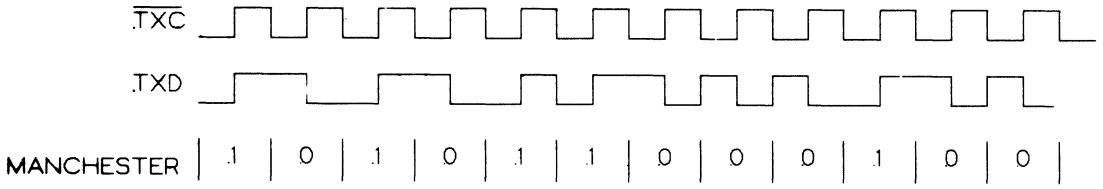


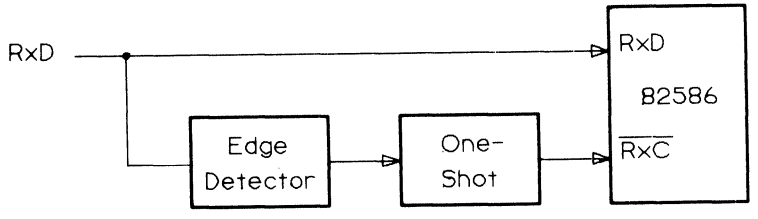
FIGURE 7.4: 82586 MANCHESTER TRANSMITTED DATA RELATIVE TO TxC

The transmitted bit center is aligned with the TxC LOW to HIGH transition.

7.1.2.2 RECEPTION

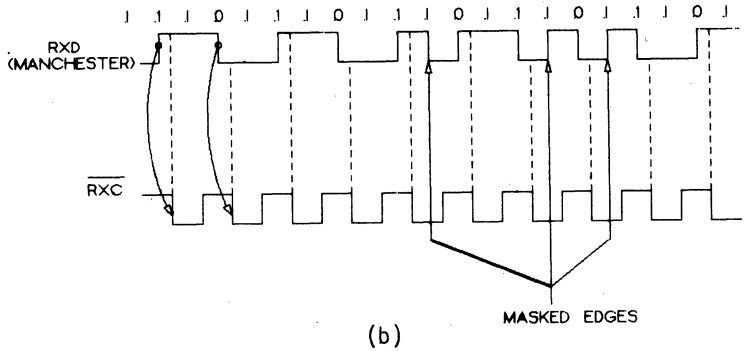
The 82586 is capable of receiving NRZ encoded data even if configured to Manchester. Thus, RECEIVED NRZ DATA TIMING RESTRICTIONS MUST BE MET (See Sec. 8.3.2). At lower bit rates simple external hardware can be used to meet the required specifications and is shown in Figure 7.5 (a) and (b).

The hardware consists of positive/negative edge detector triggering a one-shot. The one-shot non-triggerable during its non-steady state, is triggered some time after the data bit center but before the data bit end. The nonsteady period of time must be long enough to mask a potential data bit period boundary transition. Figure 8.5 timing parameters must be met by the recovered receive clock, relative to the receive 'NRZ' (really Manchester) data.



(a)

FIGURE 7.5a: RECEIVE CLOCK RECOVERY FROM MANCHESTER DATA CIRCUIT



(b)

FIGURE 7.5b RECOVERED RxC TIMING RELATIVE TO RxD (b)

7.1.3 TREATMENT OF THE LAST BIT TRANSMITTED

Following the last bit transmission cell, the $\overline{TxC}$ pin will be pulled up towards VCC. Therefore, independent of the encoding scheme, there may be one more transition at the end of the transmission if the TxD is at low voltage at the end of the last bit cell. In this way the TxD pin will be in a known state when not transmitting.

7.2 LINK MANAGEMENT CONSIDERATIONS

This section describes the link management protocol in terms of how it affects the serial interface operation. It is intended as a users guide and not as the definitive specification

7.2.1 TRANSMISSION

A host with a frame to transmit gives it to the 82586 via the action command 'TRANSMIT.' The CU accepts the command and determines if it can transmit the frame onto the serial link. The 82586 always monitors the serial link to determine such information as well as when it can look for frames to receive.

The frame can be transmitted onto the serial link if the station does not currently sense traffic on the link and has not for an Interframe Spacing (IFS) time.

If Carrier Sense is high when the CU is given a frame to send, the CU will wait until it falls and the IFS timer expires. At that point transmission is started.

Once transmission has begun, it will continue until the frame is completely transmitted or until a collision (or some other error) occurs. In the case of a collision, the 82586 will continue to transmit the remainder of the data byte in progress and then transmit four bytes of all ones. It will then stop transmission, drop $\overline{RTS}$, and calculate the backoff delay. The actual backoff delay timer will not start until the transmitter is quiet. Once the backoff timer has expired, the transmitter will start transmitting if the link has been quiet for the IFS time.

NOTE: any abnormal situation during transmission as frame abortion, underrun, drop of $\overline{CTS}$ or drop of $\overline{CRS}$ (if configured to TONOCRS = 0), will cause jamming.

7.2.2 RECEPTION

Frame reception begins by the 82586 detecting a carrier on the serial link. The detection is filtered so as to prevent noise spikes from starting the RU. Once the start of frame is found, the counting of bytes begins for the minimum frame size check. As each byte is received, the counter is incremented. A frame that does not meet minimum length is discarded.

The first N=ADDR-LEN bytes are checked to be the node's Individual Address, a Broadcast Address or a Multicast Address. If the address is valid, (or Promiscuous Mode is set) the reception of the frame is continued. Otherwise the frame is discarded without notifying the higher level using the bus. The end of the frame is determined by the framing technique specified. If Bitstuffing framing is used, then detection of the flag ('01111110') will signal end of frame. Any bits after the flag will be ignored. The search for the next frame will not begin until IFS time, after the carrier drops. If the number of bits after zero bit deletion is not equal to an eight multiple, then the residue will be discarded. The Frame Check Sequence is checked on the truncated data. Having a residue and a bad FCS will be reported as an Alignment Error.

For the End Of Carrier framing technique, the loss of Carrier Sense indicates the end of the frame. This simply means that no more bits are on the wire. The end of frame is indicated by the first Carrier Sense drop. Should it reappear shortly (a few bit times), no additional bits will be received. If Carrier-sense is lost on a non-byte boundary, a similar treatment to Bitstuffing Mode will occur.

The receiver will be blocked for IFS period after carrier goes away, thus, being incapable of any reception during this time period.

8.0 ELECTRICAL AND TIMING CHARACTERISTICS

The specifications following are preliminary values and are subject to change without notice.

8.1 D.C. CHARACTERISTICS

TA = 0 - 70 deg. C, VCC = 5V+/-10% CLK, TxD, TxC, RxD, RxC have MOS levels (see VMIL,VMIH,VMOL,VMOH). All other signals have TTL levels (see VIL, VIH, VOL, VOH).

NOTE: Industrial and military standard range 82586 devices (at lower performace) will be specified after product sampling.

TABLE 8.1: DC CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
VIL	Input Low Voltage (TTL)	-0.5	+0.8	V	
VIH	Input high Voltage (TTL)	2.0	VCC+ 0.5	V	
VOL	Output Low Voltage (TTL)		0.45	V	IOL=2.5mA
VOH	Output High Voltage (TTL)	2.4		V	IOH=-400uA
VMIL	Input Low Voltage (MOS)	-0.5	0.6	V	
VMIH	Input High Voltage (MOS)	3.9	VCC+ 0.5	V	
VMOL	Output Low Voltage (MOS)		0.45	V	IOL=2.5mA
VMOH	Output High Voltage	VCC- 0.5		V	IOH=-400uA
ILI	Input Leakage Current		+10	uA	0 VIN VCC
ILO	Output Leakage Current		+/-10	uA	0.45 VOUT VCC

TABLE 8.1 continued...

Symbol	Parameter	Min.	Max.	Units	Test Conditions
CIN	Capacitance of Input Buffer		10	pF	FC=1MHz
COUT	Capacitance of Output Buffer		20	pF	FC=1MHz
ICC	Power Supply		450	mA	TA=25deg.C

8.2 SYSTEM INTERFACE A.C. TIMING CHARACTERISTICS

TA = 0 - 70 Deg. C, VCC 5V+/-10%

Figure 8.1 and Figure 8.2 define how the measurements should be done:

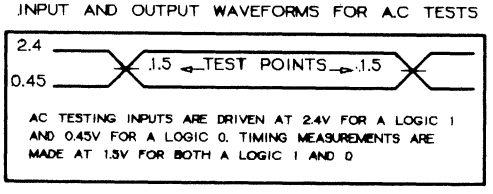


FIGURE 8.1: TTL INPUT/OUTPUT VOLTAGE LEVELS FOR TIMING MEASUREMENTS

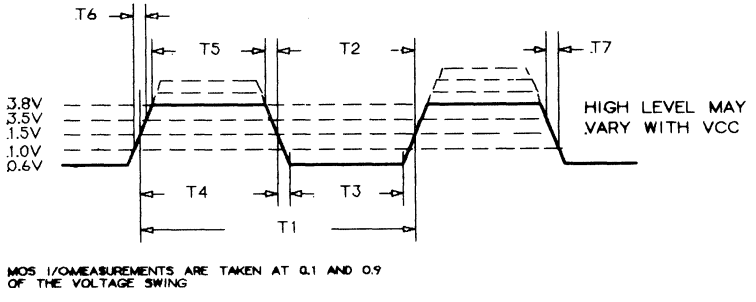


FIGURE 8.2: SYSTEM CLOCK MOS INPUT VOLTAGE LEVELS FOR TIMING MEASUREMENTS

Figure 8.3, Figure 8.4 and Figure 8.5 show the INT, CA and RESET timings, respectively.

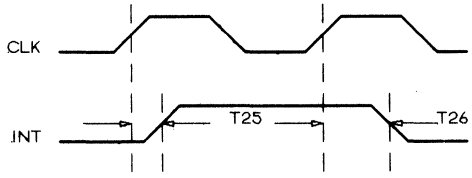


FIGURE 8.3 : INT OUTPUT TIMING

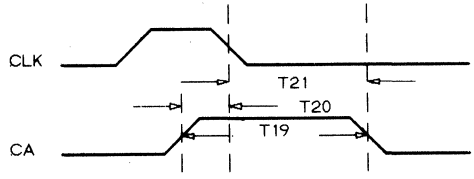


FIGURE 8.4: CA INPUT TIMING

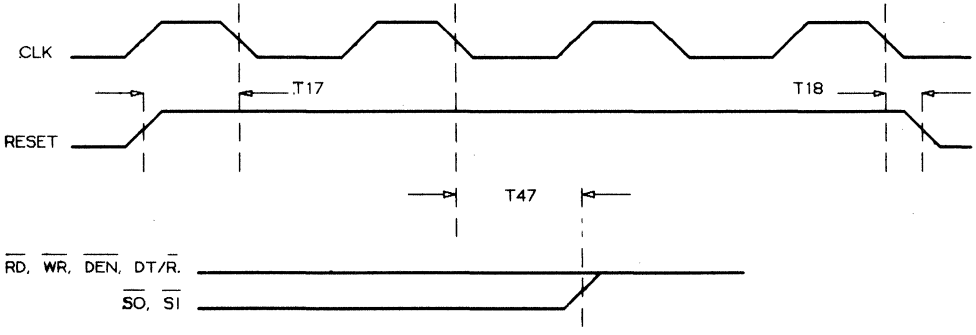


FIGURE 8.5: RESET TIMING

The 82586 SREADY and ARDY timings are shown in Figure 8.6.

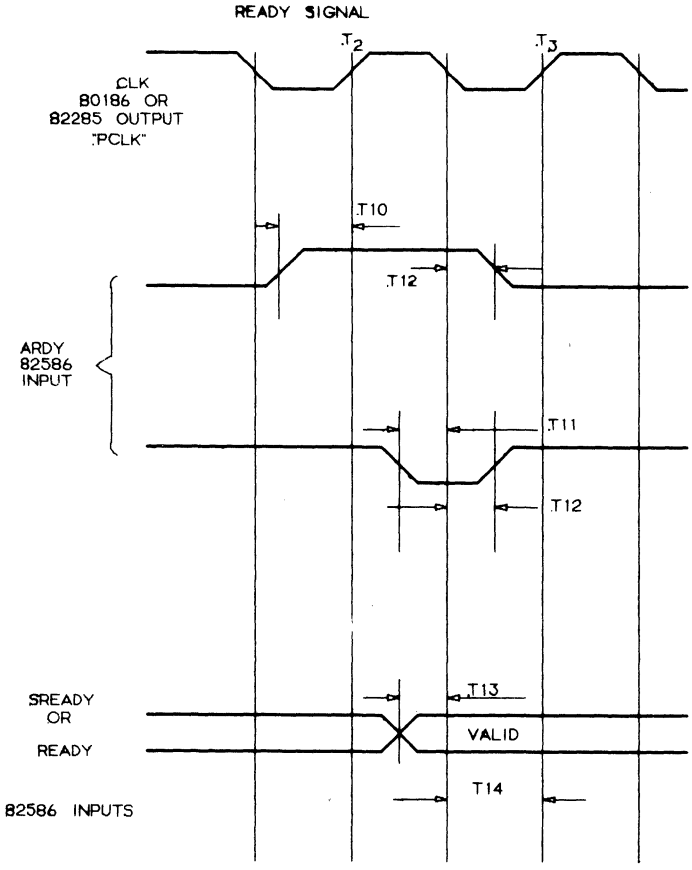
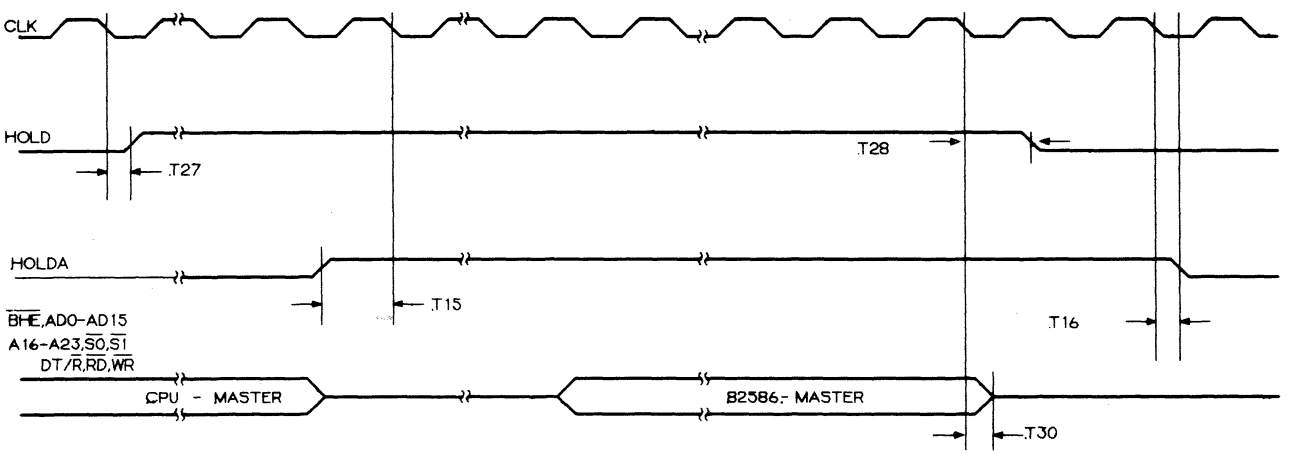


FIGURE 8.6: ARDY & SRDY TIMINGS RELATIVE TO CLK

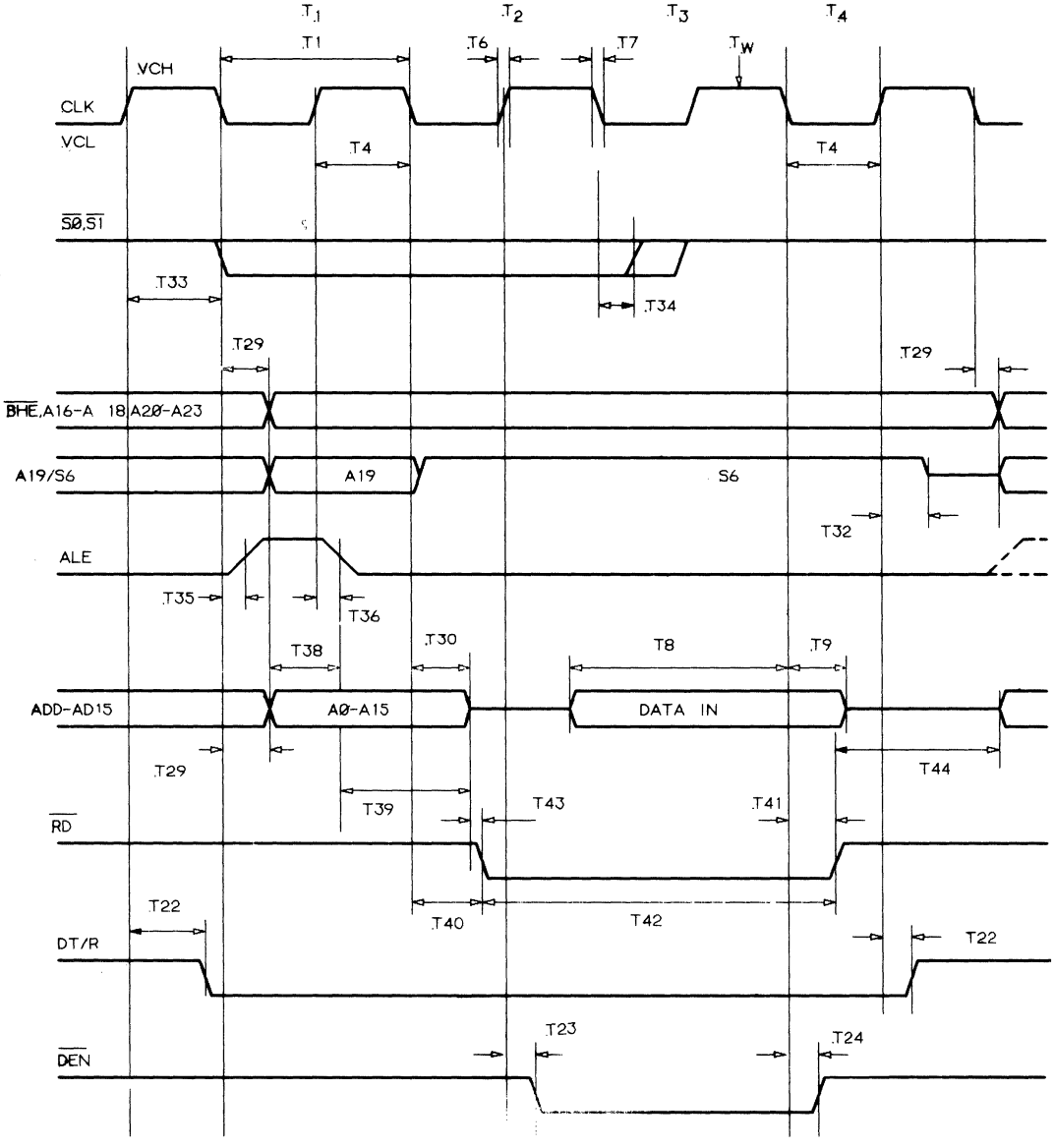
Figure 8.7 shows the HOLD and HLDA timings:



HOLD/HLDA TIMING

FIGURE 8.7 HOLD/HLDA TIMING RELATIVE TO CLK

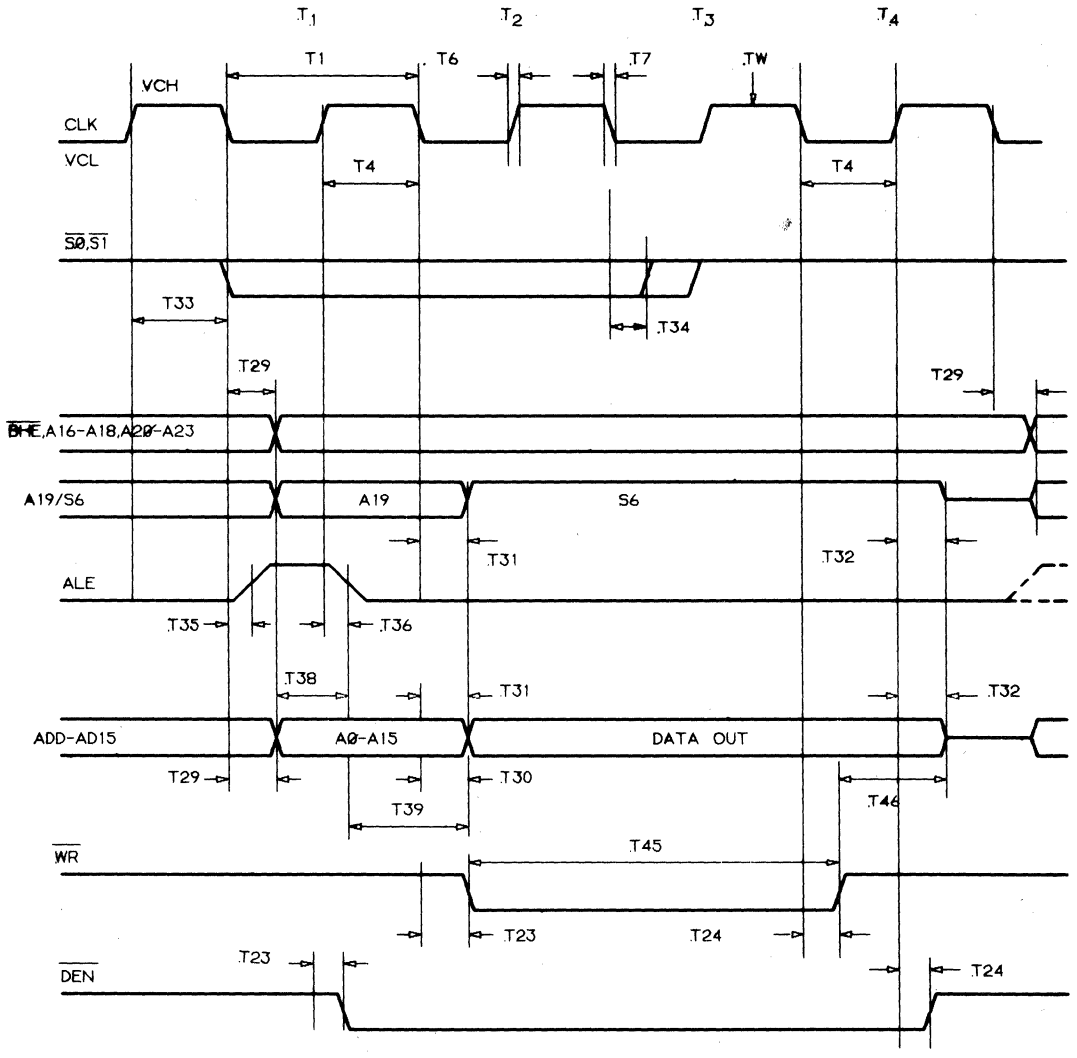
Figure 8.8 shows the Read Cycle timings.



READ CYCLE

FIGURE 8.8: READ CYCLE TIMINGS

Figure 8.9 shows the Write Cycle timings:



WRITE CYCLE

FIGURE 8.9: WRITE CYCLE TIMING

Table 8.2 gives all the 82586 system input requirements and Table 8.3 - the system output delays.

TABLE 8.2: 82586 INPUT TIMING REQUIREMENTS

TIMING REQUIREMENTS — all units are in nSec
8MHz

Symbol	Parameter	Min.	Max.	Comments
T1	CLK cycle period	125	2000	
T2	CLK low time at 1.5V	53	1000	
T3	CLK low time at 0.6V	42.5	1000	
T4	CLK high time at 1.5V	53		
T5	CLK high time at 3.8V	42.5		
T6	CLK rise time		15	*1
T7	CLK fall time		15	*2
T8	Data in setup time	20		
T9	Data in hold time	10		
T10	Async RDY active setup time	20		*3
T11	Async RDY inactive setup time	35		*3
T12	Async RDY hold time	15		*3
T13	Synchronous ready/active setup	35		
T14	Synchronous ready hold time	0		

Table 8.2 contd..

TIMING REQUIREMENTS 8MHz

Symbol	Parameter	Min.	Max.	Comments
T15	HLDA setup time	20		*3
T16	HLDA hold time	10		*3
T17	Reset setup time	20		*3
T18	Reset hold time	10		*3
T19	CA pulse width	1 T1		
T20	CA setup time	20	15	*3
T21	CA hold time	10		*3

TABLE 8.3: 82586 OUTPUT TIMINGS

all units are in nSec

CL ON ALL OUTPUTS IS 20-200$_p$F UNLESS OTHERWISE SPECIFIED

Symbol	Parameter	Min.	Max.	Comments
T22	DT/R valid delay	0	60	
T23	WR, DEN active delay	0	70	
T24	WR, DEN inactive delay	0	65	

Table 8.3 contd...

TIMING REQUIREMENTS 8MHz

Symbol	Parameter	Min.	Max.	Comments
T25	Int. active delay	0	85	*4
T26	Int. inactive delay	0	85	*4
T27	Hold active delay	0	85	*4
T28	Hold inactive delay	0	85	*4
T29	Address valid delay	0	60	
T30	Address float delay	0	50	
T31	Data valid delay	0	60	
T32	Data hold Time	0		
T33	Status active delay	0	60	
T34	Status inactive delay	0	70	
T35	ALE active delay	0	45	*5
T36	ALE inactive delay	0	45	*5
T37	ALE width	T_2-10		*5
T38	Address valid to ALE low	T_2-30		
T39	Address hold to ALE inactive	T_7-10		

Table 8.3 contd...

TIMING REQUIREMENTS 8MHz

Symbol	Parameter	Min.	Max.	Comments
T40	RD active delay	0	95	
T41	RD inactive delay	0	70	
T42	RD width	2T1-50		
T43	Address float to RD active	0		
T44	RD inactive to Address active	T1-40		
T45	WR width	2T4-40		
T46	Data hold after WR	T2-25		
T47	Control inactive after reset	0	60	*6

NOTE LIST:

*1 - 1.0V to 3.5V
*2 - 3.5V to 1.0V
*3 - to guarantee recognition at next clock
*4 - CL = 50_pF
*5 - CL = 100_pF
*6 - Affects:

MIN MODE : RD, WR, DT/R, DEN
MAX MODE : S0, S1

8.3 SERIAL INTERFACE A.C. TIMING CHARACTERISTICS

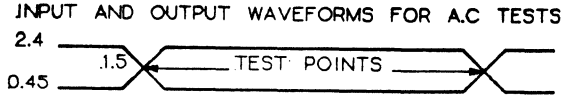
8.3.1 CLOCK SPECIFICATION

Applies for $\overline{TxC}$, $\overline{RxC}$
f min = 1MHz +/-100ppm
f max = 10MHz +/-100ppm
for Manchester, symmetry is needed:

$$T51, T52 = \frac{1}{2f} \text{ +/-5\%}$$

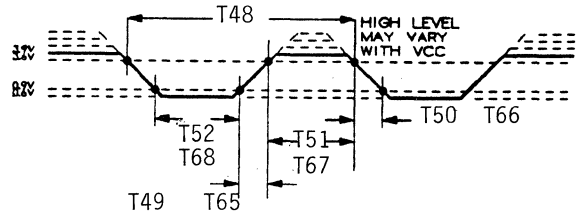
8.3.2 A.C. TIMING CHARACTERISTICS

Figure 8.10 and 8.11 define how the measurement should be done.



AC TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 AND 0.45V FOR A LOGIC 0. TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC 1 AND 0

FIGURE 8.10: TTL INPUT/OUTPUT VOLTAGE LEVELS FOR TIMING MEASUREMENTS



MOS I/O MEASUREMENTS ARE TAKEN AT 0.1 AND 0.9 OF THE VOLTAGE SWING

FIGURE 8.11: SERIAL CLOCK INPUT VOLTAGE LEVELS FOR TIMING MEASUREMENTS

Figure 8.12 and 8.13 show the transmit control and data waveforms

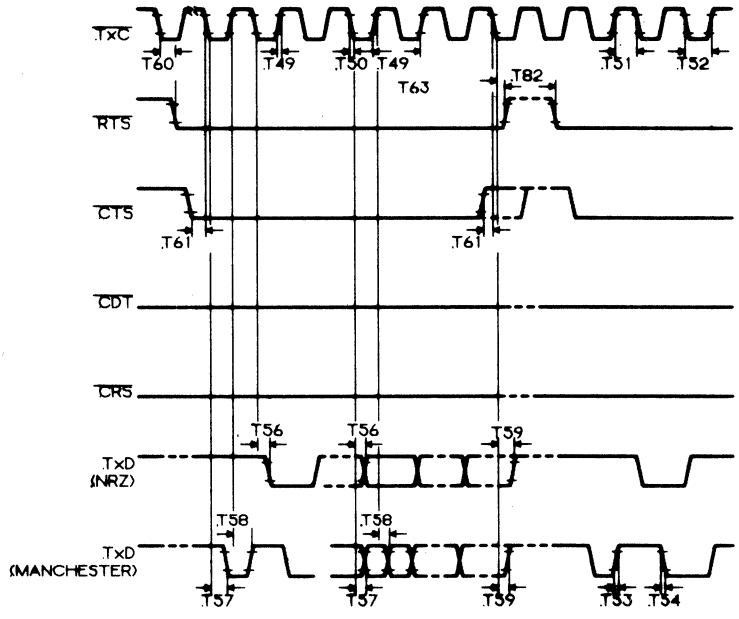


FIGURE 8.12: TRANSMIT AND CONTROL AND DATA TIMING

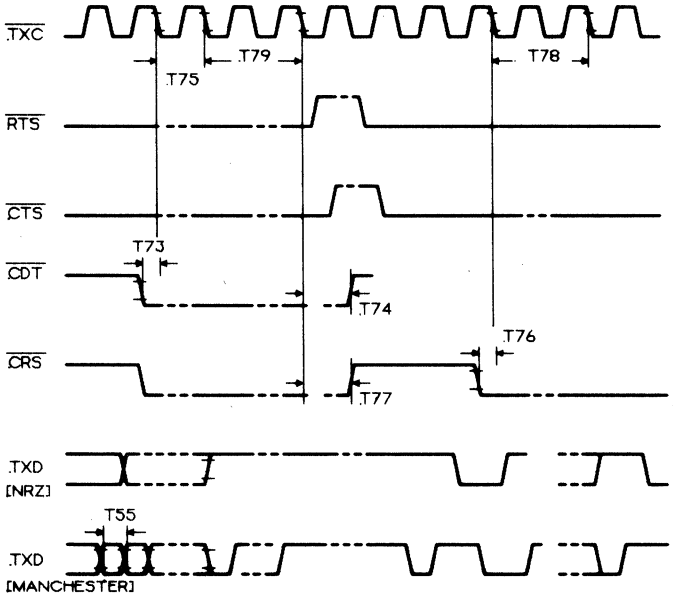


FIGURE 8.13: TRANSMIT CONTROL & DATA TIMING (CONTINUED...)

Figure 8.14 shows the Received Data timing requirements (NRZ) relative to the Receive Clock:

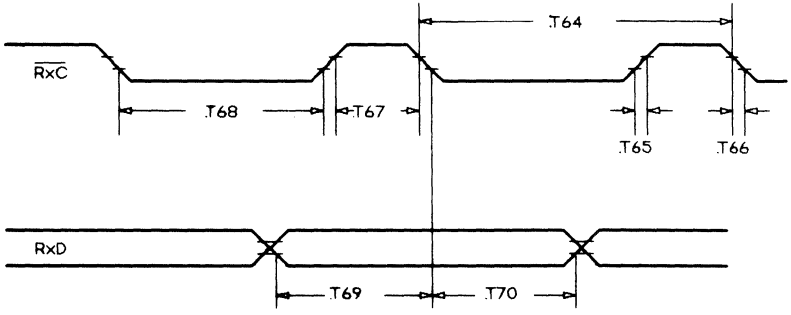


FIGURE 8.14: RxD TIMING RELATIVE TO RxC

Figure 8.15 shows the Carrier Sense signal timing requirements relative to the Receive Clock:

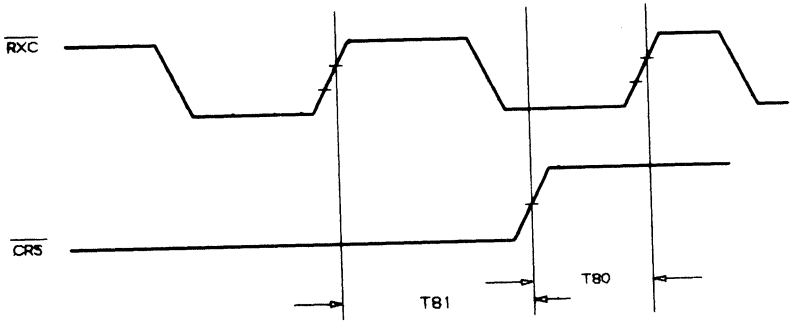


FIGURE 8.15: CRS TIMING RELATIVE TO RxC

Table 8.4 specifies the serial side timing requirements:

TABLE 8.4: TRANSMIT & RECEIVE TIMING PARAMETER SPECIFICATION

All units are nSec.

Symbol	Parameter	Min.	Max.	Comments
TRANSMIT CLOCK PARAMETERS				
T48	$\overline{TxC}$ Cycle	100	1000	*1, 2
T48	$\overline{TxC}$ Cycle	100		*1, 3
T49	$\overline{TxC}$ Rise Time		5	*1
T50	$\overline{TxC}$ Fall Time		5	*1
T51	$\overline{TxC}$ High Time	40	1000	*1
T52	$\overline{TxC}$ Low Time	40		*1, 4
TRANSMIT DATA PARAMETERS				
T53	TxD Rise Time		10	*1, 5
T54	TxD Fall Time		10	*1, 5
T55	TxD Transition - Transition	35		*1,2,5
T56	$\overline{TxC}$ Low to TxD Valid		40	*1,3,5
T57	$\overline{TxC}$ Low to TxD Transition		40	*1,2,5
T58	$\overline{TxC}$ High to TxD Transition		40	*1,2,5
T59	$\overline{TxC}$ Low to TxD High at the Transmission end		40	*1, 5

Symbol	Parameter	Min.	Max.	Comments
REQUEST TO SEND/CLEAR TO SEND PARAMETERS				
T60	$\overline{TxC}$ Low to $\overline{RTS}$ Low Time to Activate RTS		40	*6
T61	$\overline{CTS}$ Valid to $\overline{TxC}$ Low $\overline{CTS}$ Set-up Time	45		*6
T62	$\overline{TxC}$ Low to $\overline{CTS}$ Invalid. CTS Hold Time	20		*6,7
T63	$\overline{TxC}$ Low to $\overline{RTS}$ High. Time to deactivate RTS		40	*6
RECEIVE CLOCK PARAMETERS				
T64	$\overline{RxC}$ Clock Cycle	100		*1,3
T65	$\overline{RxC}$ Rise Time		5	*1
T66	$\overline{RxC}$ Fall Time		5	*1
T67	RxC High Time	40	1000	*1
T68	$\overline{RxC}$ Low Time	40		*1
RECEIVE DATA PARAMETERS				
T69	RxD Setup Time	30		*1
T70	RxD Hold Time	30		*1
T71	RxD Rise Time		10	*1
T72	RxD Fall Time		10	*1

Table 8.4 Cont...

Symbol	Parameter	Min.	Max.	Comments
CARRIER SENSE/COLLISION DETECT PARAMETERS				
T73	$\overline{CDT}$ Valid to $\overline{TxC}$ Low Ext. Collision Detect Setup Time	30		*12
T74	$\overline{TxC}$ Low to $\overline{CDT}$ Inactive. CDT Hold Time	20		*12
T75	CDT Low to Jamming Start		*8	
T76	$\overline{CRS}$ Valid to $\overline{TxC}$ Low Ext. Carrier Sense Setup Time	30		*12
T77	$\overline{TxC}$ Low to $\overline{CRS}$ Inactive CRS Hold Time	20		*12
T78	$\overline{CRS}$ Low to Jamming Start		*9	
T79	Jamming Period	*10		
T80	$\overline{CRS}$ Inactive Setup Time to RxC High. End of Receive Pkt	60		
T81	$\overline{CRS}$ Inactive Hold Time to RxC High. End of Receive Pkt	10		
INTERFRAME SPACING PARAMETER				
T82	Inter Frame Delay	*11		

NOTES:

*1 - MOS levels.
*2 - Manchester only.
*3 - NRZ only
*4 - Manchester requires 50% Duty Cycle
*5 - 1TTL Load + 50_{p}F.
*6 - 1TTL Load + 100_{p}F.
*7 - Abnormal End of Transmission. CTS Expires Before RTS.
*8 - Programmable value:
T81 = NCDF x T54 +(12.5 to 23.5) x T54 if collision occurs after preamble
NCDF - The Collision Detect Filter Configuration Value.
*9 - Programmable Value:
T84 = NCSF x T54 +(12.5 to 23.5) x T54
NCSF - The Carrier Sense Filter Configuration Value.
TBD is a function of Internal/External Carrier Sense Bit
* 10 T85 = 32 x T54
* 11 Programmable value:
T88 = NIFS x T48
NIFS - The IFS Configuration Value.
If NIFS 31 then NIFS is enforced to 32.
*12 To guarantee recognition on the next clock.

9.0 RELEVANT DOCUMENTS

1. Ethernet: Distributed Packet Switching for Local Computer Networks, R.M. Metcalfe et al, Communications of ACM, July 1976.

2. Performance of an Ethernet Local Network- A Preliminary Report. J.F. Shoch et al, LACN Symposium, Boston, May 1979.
3. Message-Based priority functions in Multiaccess/Broadcast Communication Systems with carrier sense capability, F.A. TOBAGI Stanford Electronic Labs, Technical Report No.181 October 1979.

4. The Ethernet Specification Version 1.0, September 30 1980 Digital, Intel, Xerox.

5. ISO "Reference Model for Open Systems Architecture", ISO/TC97/SC16 N117.

6. ISO 3309, Data Communication, High Level Data Link Control procedures, Frame Structure, 1976.

7. "Data Communications - HDLC Frame Structure", ISO/TC97 UCD 681.3 : 621.391.

8. 82586 Data Sheet

9. 82501 Data Sheet

10. "System-Level Functions Enhance Controller" Electronics, October 6, 1982, Intel Article Reprint AR 237, order number 210788-001.

11. "2-Chip Controller Set Drives Ethernet Hookup, Costs" Data Communications, October 1982, Intel Article Reprint AR-244, order number 210832-001.

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