iSBC 016A/032A/064A/028A/056A™ RAM BOARD HARDWARE REFERENCE MANUAL

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This manual provides general information, preparation for use, principles of operation, and service information for the iSBC 016A/032A/064A/028A/056A RAM Board. Supplementary information is provided in the following documents.

- *Peripheral Design Handbook,* Order No. 9800676.
- *Intel Multibus Specification,* Order No. 9800683.

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ILLUSTRATIONS

1-1. INTRODUCTION

The iSBC 016A/032A/064A/028A/056A Random Access Memory (RAM) Boards provide a dynamic memory storage capacity of 16k, 32k, 64k, 128k, and 256k bytes, respectively, for use with all Intel iSBC 80/86 Series Single Board Computers and Intel 80/86 Series Microcomputer Systems. These RAM boards interface directly with the bus master via the Multibus interface and differ only in memory capacity and memory array configuration. This manual provides a general introduction, preparations for use, principles of operation, and service requirements for each of the configurations of the RAM board.

The iSBC 016A/032A/064A/028A/056A RAM boards are designed to allow quick, easy, and inexpensive expansion of RAM storage facilities within an Intel Multibus-compatible System. On-board refresh circuitry initiates periodic RAM refresh cycles to maintain the integrity of the RAM data. An optional auxiliary bus connector may provide battery back-up power for the RAM and the refresh circuits. The RAM boards are direct replacement products for the iSBC 016/032/064 RAM Boards. Figure 1-1 shows a typical example of the iSBC 016A/032A/064A/028A/056A RAM Boards.

1-2. DESCRIPTION

The RAM boards consist of components that are mounted onto a single printed circuit board (as shown in figure 1-1) that is physically and electrically compatible with the Multibus standards as outlined in the *Intel Multibus Specification*. The capacity of the RAM boards varies depending on the type of memory devices installed on the boards; Intel 2110 (8,192 by 1 bit), Intel 2118 (16,384 by 1 bit), Intel 2132 (32,768 by 1 bit), or Intel 2164 (65,536 by 1 bit) RAM chips. The capacity of each version of the RAM board is as follows:

Type of RAM Board	Quantity of Chips	Type of Chips	Memory Capacity
iSBC 016A RAM Board	16	2110	16k bytes
iSBC 032A RAM Board	36	2110	32k bytes
iSBC 064A RAM Board	36	2118	64k bytes
iSBC 028A RAM Board	36	2132	128k bytes
iSBC 056A RAM Board	36	2164	256k bytes
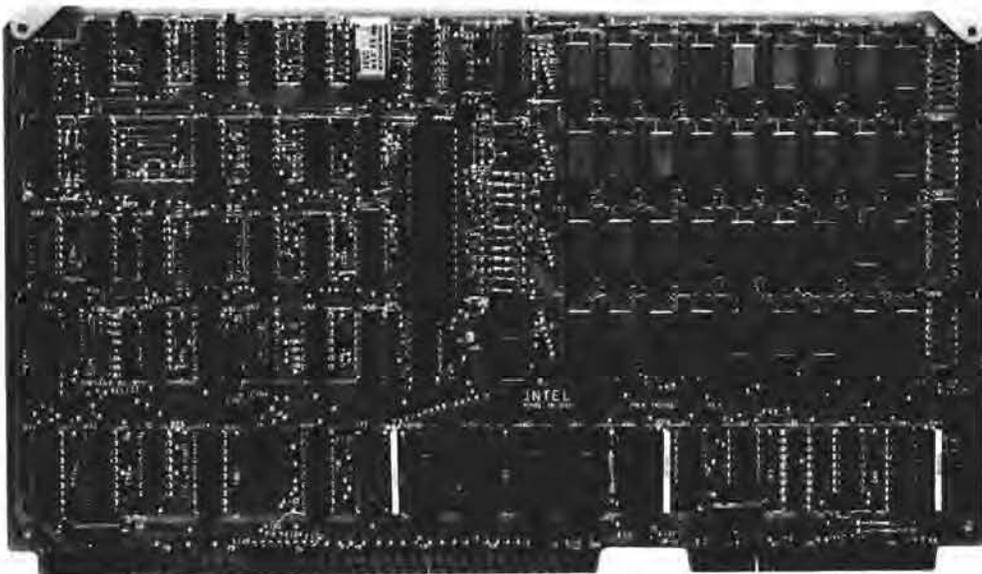
Figure 1-1. iSBC 016A/032A/064A/028A/056A™ RAM Boards

The design of the RAM boards allows operation within either an 8-bit or a 16-bit system. On-board jumpers are used to establish a RAM base address and to define page address boundaries. The RAM base address serves as a select address for the board. More information on jumper configurations is presented in Chapter 2 of this manual.

All of the RAM boards (except for the iSBC 016A RAM board) are equipped with a parity generating and checking feature that provides data handling and storage integrity verification for the RAM boards. The result of the parity check performed on a READ operation is stored within an internal I/O register on the RAM boards and accessible to the Multibus interface via an I/O READ operation. The RAM boards are equipped with an LED that provides a visual indication if a parity error does occur.

All electrical connections to and from the RAM boards are implemented via edge connectors P1 and P2. Connector P1 (86-pin) provides the interface to the Multibus structure and accommodates the power and signal lines including the address and data busses. The P2 connector (60-pin) accommodates the auxiliary power lines and upper address lines.

1-3. MODES OF OPERATION

The iSBC 016A/032A/064A/028A/056A RAM boards are capable of operation with any 8- or 16-bit iSBC board operating as the Multibus master. Board modifications are not required to convert a RAM board from 8- to 16-bit system operation. More details of the data transfer sequence are contained in Chapter 4 of this manual.

1-4. EQUIPMENT SUPPLIED

The RAM boards are shipped with a current revision of the schematic drawing that should be placed into this manual.

1-5. SPECIFICATIONS

Table 1-1 lists the specifications and requirements for the iSBC 016A/032A/064A/028A/056A RAM boards.

Table 1-1. Specifications

BOARD CAPACITY:	
iSBC 016A RAM Board:	16,384 bytes or 8,192 words
iSBC 032A RAM Board:	32,768 bytes or 16,384 words
iSBC 064A RAM Board:	65,536 bytes or 32,768 words
iSBC 028A RAM Board:	131,072 bytes or 65,536 words
iSBC 056A RAM Board:	262,144 bytes or 131,072 words
MULTIBUS INTERFACE:	All versions of the RAM board are fully compatible with the *Multibus Specification.*
	ADDRESS SELECTION:
Page Address:	User configured jumpers allow assignment of memory into one of 16 possible megabyte pages of memory address space.
4k Boundary Address:	User configured jumpers allow assignment of the starting address of memory to one of 256 possible 4k boundaries.
ACCESS TIME:	
Read:	406 nanoseconds (maximum for 016A, 032A, 064A)
Write:	343 nanoseconds (maximum for 016A, 032A, 064A, 028A) See table 2-7
CYCLE TIMES:	
Read:	608 nanoseconds (maximum for 016A, 032A, 064A, 028A)
Write:	608 nanoseconds (maximum for 016A, 032A, 064A, 028A)
Refresh:	608 nanoseconds (maximum for 016A, 032A, 064A, 028A) See table 2-7
PHYSICAL CHARACTERISTICS:	
Width:	30.48 cm (12.00 inches)
Length:	17.15 cm (6.75 inches)
Thickness:	1.27 cm (0.50 inch)
Weight:	400 gm (14.0 ounces)
POWER REQUIREMENTS:	
Power Consumption:	24 Watts maximum (see table 2-1) 10 Watts typical
Power Supply Voltage:	+5 volts at 4.0 amps (maximum) 2.0 amps (typical)
ENVIRONMENTAL SPECIFICATIONS:	
Operating Temperature:	0 to 55°C (32 to 130°F)
Operating Humidity:	To 90% (without condensation)

2-1. INTRODUCTION

This chapter provides instructions for preparing the iSBC 016A/032A/064A/028A/056A RAM Boards for use in a user-defined environment. Included in this chapter are instructions on unpacking and inspection, installation considerations, jumper configurations, battery back-up configuration, and board installation information. It is advisable that the contents of Chapter 4 be fully read and understood before beginning the configuration and installation procedures contained in this chapter.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and the packing material for the agent's inspection.

For repair to a product damaged in shipment, contact the Intel Technical Support Center to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that the salvageable shipping cartons and packing material be saved for future use in the event that the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

Installation considerations such as power, cooling, physical size requirements, and interfacing requirements are outlined in the following paragraphs.

2-4. POWER REQUIREMENTS

The power requirements for the RAM boards depend on the type and quantity of RAM chips installed onto the RAM boards. Table 2-1 lists the various current requirements for each configuration of the RAM boards.

![CAUTION]

In all cases, the "A" versions of the RAM boards require more +5 volt current than their earlier-model counterparts. Ensure that the current requirements of the RAM boards are within the limits of your system's capability. Failure to do so could result in damage to the power supply.

2-5. COOLING REQUIREMENTS

The heat dissipation for the RAM boards varies with the configuration of the board; table 2-1 shows the maximum power dissipation for each configuration. Adequate circulation of air must be provided to prevent a temperature rise above 55°C (130°F). The system chassis units available from Intel include fans that provide adequate intake and exhaust of ventilating air.

Table 2-1. Power Consumption/
Heat Dissipation (maximum)

Configuration	Power Requirements	Heat Dissipation
iSBC 016A board	16.5 W	247 gc/m (1.00 BTU)
iSBC 032A board	17.3 W	299 gc/m (1.21 BTU)
iSBC 064A board	17.3 W	299 gc/m (1.21 BTU)
iSBC 028A board	24.0 W	341 gc/m (1.38 BTU)
iSBC 056A board	24.0 W	341 gc/m (1.38 BTU)

2-6. INTERFACING REQUIREMENTS

The iSBC 016A/032A/064A/028A/056A RAM Boards are designed for installation into a standard Intel iSBC cardcage or into an Intel Microcomputer Development System chassis. As shown in figure 1-1, the 43/86-pin edge connector (P1) on the RAM boards provides interfacing to the Multibus structure. Table 2-2 lists the pin assignments for the P1 connector and table 2-3 lists a description of the function of each signal.

Edge connector P2 on the RAM boards is an optional 30/60-pin connector providing the external RAM refresh signal, the upper memory address bits, parity bits for each byte of a data word, battery back-up signals, and memory protection signals for the RAM boards. Table 2-4 lists the pin assignments for connector P2 and table 2-5 lists a description of each signal function on the P2 interface. Notice that the RAM boards require the use of a P2 connector if the memory is to reside anywhere other than on mega-byte page 0; the upper address lines must be made available to the RAM boards.

The ac and dc characteristics of the RAM boards are listed in tables 2-6 and 2-7, respectively. The ac characteristics listed in table 2-6 are further defined by figure 2-1 which shows the system timing requirements for a Memory WRITE and Memory READ operation, and by figure 2-2 which shows the system timing requirements for an I/O WRITE and I/O READ operation.

Table 2-2. P1 Connector Pin Assignment

	PIN	(COMPONENT SIDE)		PIN	(CIRCUIT SIDE)	
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Sig GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7			8		
	9		Reserved	10		Reserved
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13		Reserved	14	INIT/	Reset
	15		Reserved	16		Reserved
	17		Reserved	18		Reserved
	19	MRDC/	Mem Red Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 Disable RAM
BUS CONTROLS AND ADDRESS	25		Reserved	26		Reserved
	27	BHEN/	Byte High Enable	28	AD10/	
	29		Reserved	30	AD11/	Address
	31		Reserved	32	AD12/	Bus
	33		Reserved	34	AD13/	
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79		Reserved	80		Reserved
	81	+5V	+5Vdc	82	+5	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

Table 2-8 contains a list of compatible connectors that a user may install into a standard Intel iSBC cardcage for interface to the P2 connector on the RAM boards. If the system does not require any of the signals provided on the P2 connector, the compatible P2 connector need not be installed.

Table 2-3. P1 Connector Signal Description

Signal	Functional Description
ADR0/ ADRF/ ADR10/-ADR13/	*Address.* These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR0/ (when active) enables the even byte bank (DAT0/-DAT7/) on the Multibus; i.e., ADR0/ is active for all even addresses. ADR13/ is the most significant address bit.
BHEN/	*Byte High Enable.* When active low, enables the odd byte bank (DAT8/-DATF/) onto the Multibus.
DAT0/-DATF/	*Data.* These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most signficant bit. For data byte operations, DAT0/ - DAT7/ is the even byte and DAT8/-DATF/ is the odd byte.
INH1/	*Inhibit RAM.* For system applications, allows iSBC dual port RAM addresses to be overlayed by ROM/PROM or memory mapped I/O devices. This signal has no effect on local CPU access of its dual port RAM.
INT0/-INT7/	*Interrupt Request.* These eight lines transmit interrupt Requests to the appropriate interrupt handler. INT0 has the highest priority.
IORC/	*I/O Read Command.* Indicates that the address of an I/O port is on the Multibus address lines and that the output of that port is to be read (placed) into the Multibus data lines.
IOWC/	*I/O Write Command.* Indicates that the address of an I/O port is on the Multibus address lines and that the contents on the Multibus data lines are to be accepted by the addressed port.
MRDC/	*Memory Read Command.* Indicates that the address of a memory location is on the Multibus address lines and that the contents of that location are to be read (placed) on the Multibus data lines.
MWTC/	*Memory Write Command.* Indicates that the address of a memory location is on the Multibus address lines and that the contents on the Multibus data lines are to be written into that location.
XACK/	*Transfer Acknowledge.* Indicates that the address memory location has completed the specified read or write operation. That is, data has been placed onto or accepted from the Multibus data lines.

Table 2-4. P2 Connector Pin Assignment

PIN	(COMPONENT SIDE) MNEMONIC	(COMPONENT SIDE) DESCRIPTION	PIN	(CIRCUIT SIDE) MNEMONIC	(CIRCUIT SIDE) DESCRIPTION
1	GND	Signal GND	2	GND	Signal GND
3	GVB	+5V Battery	4	GBV	+5V Battery
5		Reserved	6		
7			8		
9		Reserved	10	Reserved	
11			12		
13			14	Reserved	
15			16		
17			18		
19			20	MPRO/	Memory Protect
21	GND	Signal GND	22	GND	Signal GND
23			24		
25			26		
27			28		
29			30		
31			32	PO0	Parity Bit (Byte 0)
33			34	PO1	Parity Bit (Byte 1)
35			36		
37			38		
39			40		
41	RFQST/	REFRESH REQUEST	42		
43			44		
45			46	Reserved	
47			48		
49			50		
51			52		
53			54		
55	ADR17/	ADDRESS	56	ADR16/	ADDRESS
57	ADR16/	BUS	58	ADR14/	BUS
59			60		

Table 2-5. P2 Connector Signal Description

Signal	Functional Description
ADR14/-ADR17/	*Address.* These address lines select one of 16 megabytes of memory space to be accessed.
MPRO/	*Memory Protect.* This externally generated signal prevents the the memory and I/O on the RAM boards from recognizing and responding to a subsequent command from the Multibus interface.
PO0/,PO1/	*Parity Bits.* These parity bits are generated by the RAM boards for each data word when enabled; PO0/ for the even byte and PO1/ for the odd byte of data.
RFQST/	*Refresh Request.* This signal provides the Dynamic RAM Controller with an externally generated timing signal for generation of RAM refresh.

Table 2-6. DC Signal Characteristics for P1 Connector

Signal	Parameter	Test Conditions	Minimum	Maximum	Units
MRDC/	VIL VIH IIL IIH CL	 VIN=0.45V VIN=2.4V	 2.0	0.8 -0.4 50 7	V V mA μA pF
MWTC/	VIL VIH IIL IIH CL	 VIN=0.5V VIN=2.4V	 2.0	0.8 -0.4 50 7	V V mA μA pF
IORC/ IOWC/	VIL VIH IIL IIH CL	 VIN=0.4V VIN=2.7V	 2.0	0.8 -1.6 40 7	V V mA μA pF
INIT/	VIL VIH IIL IIH CL	 VIN=0.4V VIN=2.4V	 2.0	0.8 -1.6 40 7	V V mA μA pF
AACK/ XACK/	VOL VOH CO	IOL=64mA IOH=-3mA	 2.4 300	0.55	V V pF
INHI/	VIL VIH IIL IIH CL	 VIN=0.4V VIN=2.4V	 2.0	0.8 -0.2 20 7	V V mA μA pF
ADR0/ ADR17/ BHEN/	VIL VIH IIL IIH CL	 VIN=0.45V VIN=2.4V	 2.0	0.8 -0.4 50 7	V V mA μA pF
DAT0/ DATF/	VIL VIH IIL IIH CL VOL VOH	 VIN=0.45V VIN=2.4V IOL=32mA IOH=-5mA	 2.0 2.4	0.8 -0.4 100 24 0.45	V V mA μA pF V V

Table 2-6. DC Signal Characteristics for P1 Connector (Continued)

Signal	Parameter	Test Conditions	Minimum	Maximum	Units
MPRO/	VIL VIH IIL IIH CL	 VIN=0.4V VIN=2.4V	 2.0	0.8 -2 50 7	V V mA μA pF
INT0/	VOL VOH CL	IOL=16mA	 Open Collector	0.4 18	V pF

Table 2-7. AC Signal Characteristics for P1 Connector

Parameter	Description	Minimum All	Maximum		
			016A-064A	028A	056A
tAS	Address Set-up Time	50			
tDS	Write Data Set-up Time Memory Write Data Set-up Time I/O	-100 0			
tAH	Address Hold Time	0			
tDHW	Write Data Hold Time	0			
tDXL	Read Data Set-up Time to XACK	0			
tDHR	Read Data Hold Time	0		60	
tAXAH	Acknowledge Hold Time	0		55	
tXACK	Acknowledge Time: Memory Read Cycle Acknowledge Time: Memory Write Cycle		406 343	500 343	570 363
	Acknowledge Time: I/O Read Cycle Acknowledge Time: I/O Write Cycle		238	330 185	370
tID	Inhibit Delay From Address			150	
tCS	Command Separation	50			
tIS	Inhibit Set-up Time to CMD			-100	
tACC	Command to Data Valid		357	402	447
tIH	Inhibit Hold Time after CMD	850			
tCY	Cycle Time Memory Cycle Time I/O Read Cycle Time I/O Write		608 268	608 340 235	653 360
tINIT	INIT Pulse Width	50			
tCYD	Cycle Time of Non-Qualified Write		1200	1200	1200
tRD	Refresh Delay Time		480	480	540
tRI	Refresh Interval	10.56μs		14.4μs	
tNQDS	Write Data Delay from Command (Non qualified write cycle)		600		

Note:
All units are in nanoseconds.
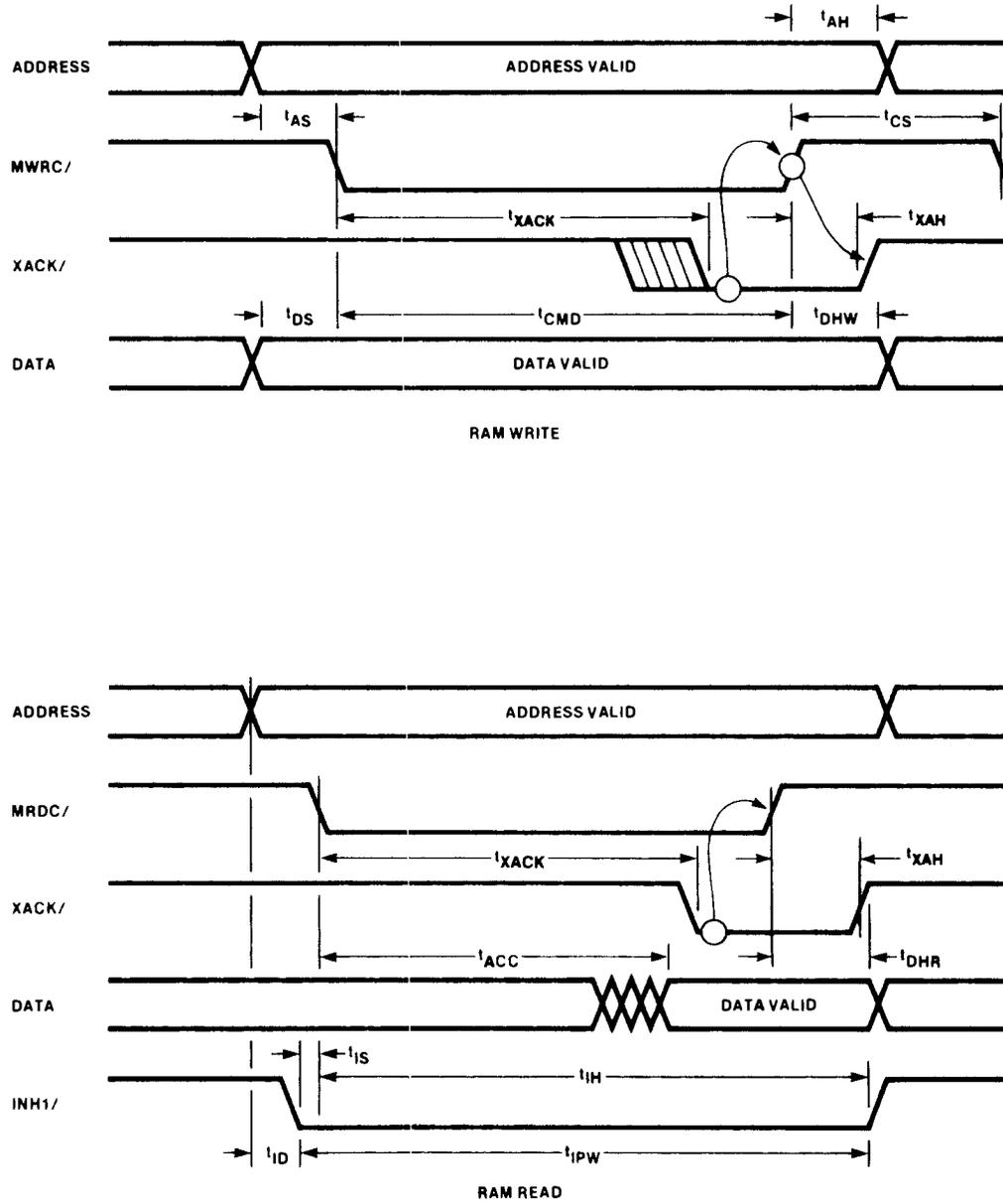
Figure 2-1. Multibus Timing For Memory READ and Memory WRITE operations
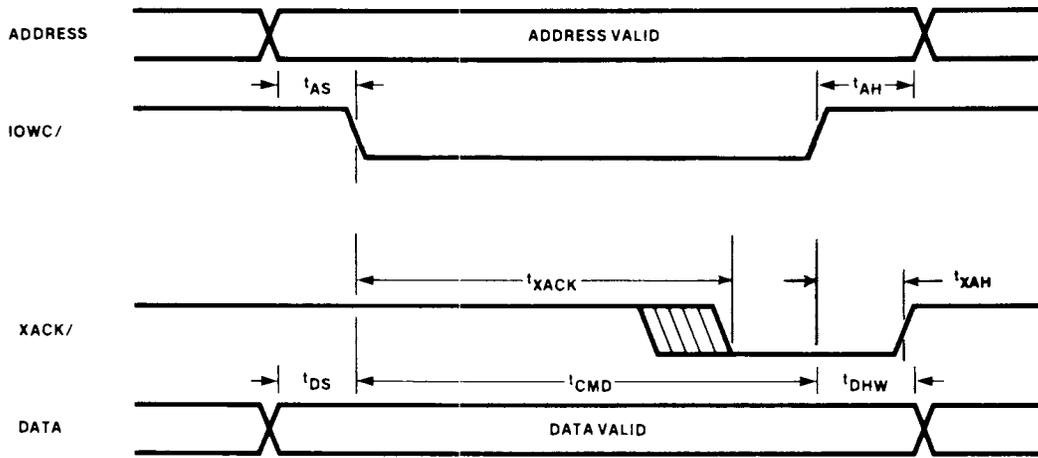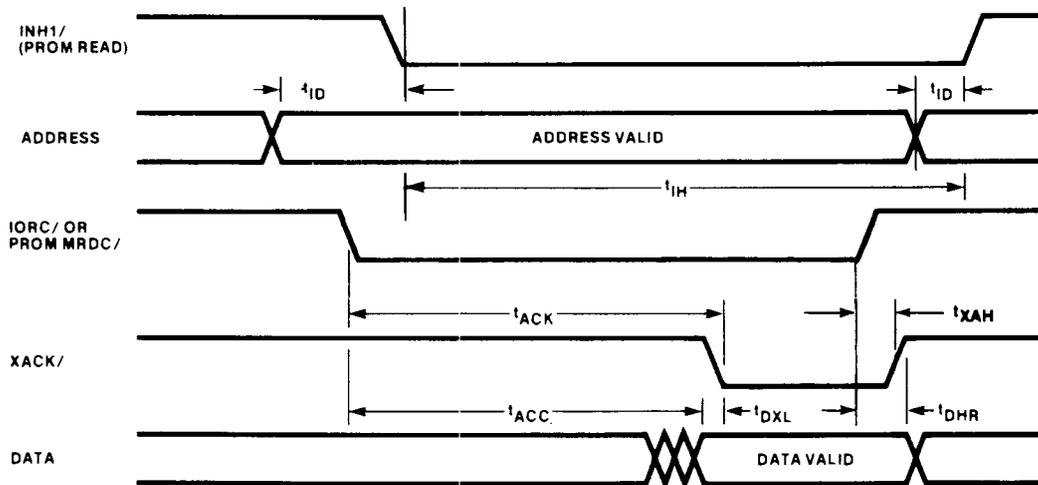
Figure 2-2. Multibus Timing For I/O READ and I/O WRITE operations

Table 2-8. Compatible User-provided P1 and P2 Connectors

Function	Pins	Centers (Inches)	Connector Type	Vendor	Part Number
Multibus Connector P1	43/86	0.156	Solder PCB	ELFAB VIKING	BS1562043PBB 2KH43/9AMK12
			Wire Wrap (no ears)	EDAC ELFAB	337-086-0540-201 BW1562D-43PBB
			Wire Wrap (with 0.128 mounting holes)	EDAC ELFAB	337-086-540-202 BW1562A-43PBB
Auxiliary Connector P2	30/60	0.100	Wire Wrap	EDAC ELFAB	345-060-524-802 BS1020A-30PBB
			With 0.128 mounting holes	TI VIKING	H421121-30 3KH30/9JNK
			No Ears	EDAC ELFAB	345-060-540-201 BW1020D-30PBB

Notes:
1. Connector heights are not guaranteed to conform to OEM equipment.
2. Wire wrap pin lengths are not guaranteed to conform to OEM equipment.
3. Connector numbering convention may not agree with board connector.

2-7. JUMPER CONFIGURATIONS

Jumper selection options available to a user of the RAM boards include megabyte page address selection, 4k boundary selection, parity enable/disable, external refresh request enable, interrupt level selection, and non-qualified memory write selection.

The instructions for configuring each of these jumpers are provided in the following paragraphs; table 2-9 contains a list of the functions performed by each jumper and table 2-10 contains a list of the default jumper connections for each version of the RAM boards, as shipped.

Table 2-9. Jumper Functions

Jumper Number	Version Used On	Function
E1,E2,E3	Used only in 064A version	ADVANCED/DELAYED WRITE SELECT. Connecting E2-E3 (the as-shipped configuration) enables operation in a DELAYED (normal) WRITE mode. Connecting E1-E2 enables the ADVANCED (NON-QUALIFIED) WRITE mode; the ADVANCED WRITE mode is required only for use with MDS 800 Development Systems and ICE 80 Emulators.
E4,E5	All versions except 016A	PARITY FLAG REGISTER OUTPUT ENABLE. When installed (the as-shipped condition), the jumper enables the Parity Flag Register to output the parity error location information onto the Multibus interface.
E26,E27,E28	All versions except 016A	INPUT PARITY SELECT (BANK 1). Jumper E26-E27 (installed as-shipped) enables on-board generation of a parity bit for a WRITE to memory bank 1 operation. Installation of jumper E27-E28 enables external generation of a parity bit via the P2 connector.
E31,E32,E33	All versions except 016A	INPUT PARITY SELECT (BANK 0). Jumper E31-E32 (installed-as-shipped) enables on-board generation of a parity bit for a WRITE to memory bank 0 operation. Installation of jumper E32-E33 enables external generation of a parity bit via the P2 connector.
E76,E77,E78, E103,E104, E105,E106, E107,E108,E109, E110 through E114	All versions	ENABLES FOR ON-BOARD I/O PORT ADDRESS SELECT. These jumpers allow user selection of the I/O port address at which the Parity Flag Register is accessed via the Multibus interface. As shipped, E103-E104, E105-E106, E107-E108, and E76-E77 are connected. Refer to tables 2-14 and 2-15 to verify proper configuration.

Table 2-9. Jumper Functions (Continued)

Jumper Number	Version Used On	Function
E139 through E143	All versions	MEGABYTE PAGE SELECT. As shipped, all page select jumpers are removed, selecting megabyte page address 0XXXXXH; more information on configuration of the megabyte page address is contained in table 2-11.
E79 through E87	All versions	4k MEMORY ADDRESS BOUNDARY SELECT. As shipped, the starting 4K boundary for the board is 000000 (no jumpers installed) on all RAM boards (except the iSBC 032A RAM Board which starts at 08000H). User configuration of the jumpers is outlined in table 2-12.
E116,E117,E120, E121,E146,E47, E118,E119	All versions	BATTERY BACK-UP ENABLE. As shipped, the jumpers ARE connected. Removal of E146- E 47, E116-E117, E118-E120, and E119-E121 fully enables the battery back-up option.
E144,E145	All versions	EXTERNAL REFRESH REQUEST ENABLE. This jumper is not installed at the factory, but may be added by a user requiring a refresh cycle that is generated from an external source.
E123 through E132	All versions	INTERRUPT REQUEST ENABLE. Jumper E123-E127 is factory installed to provide an interrupt request on INT5/ if a parity error is detected. Reconfiguration of the jumper will generate one of the Multibus interrupt request lines as follows: E123-E132 Generate INT0/ E123-E131 Generate INT1/ E123-E130 Generate INT2/ E123-E129 Generate INT3/ E123-E128 Generate INT4/ E123-E127 Generate INT5/ E123-E126 Generate INT6/ E123-E125 Generate INT7/

Table 2-10. Jumper Configuration (as shipped)

Board Version	Default Jumper Configuration
iSBC 016A board with 2110-4AOL RAM chips	Connect E2-E3, E6-E7, E15-E22, E21-E22, E29-E30, E34-E35, E37-E38, E39-E45, E42-E46, E64-E65, E74-E75, E91-E92, E94-E96, E97-E99, E100-E101, E109-E108.
iSBC 016A board with 2110-4AOH RAM chips	Connect E2-E3, E6-E7, E15-E22, E21-E22, E29-E30, E34-E35, E37-E38, E39-E45, E43-E46, E64-E65, E74-E75, E91-E92, E94-E96, E97-E99, E100-E101, E109-E108, E123-E127.
iSBC 032A board with 2110-4AOL RAM chips	Connect E2-E3, E4-E5, E6-E7, E15-E22, E17-E22, E26-E27, E31-E32, E34-E35, E37-E38, E39-E45, E42-E46, E64-E65, E66-E67, E74-E75, E76-E77, E91-E92, E94-E96, E97-E99, E102-E101, E103-E104, E105-E106, E107-E108, E123-E127.
iSBC 032A board with 2110-4AOH RAM chips	Connect E2-E3, E4-E5, E6-E7, E15-E22, E17-E22, E26-E27, E31-E32, E34-E35, E37-E38, E39-E45, E43-E46, E64-E65, E66-E67, E74-E75, E76-E77, E91-E92, E94-E96, E97-E99, E102-E101, E103-E104, E105-E106, E107-E108, E123-E127.
iSBC 064A board with 2118-4 RAM chips	Connect E2-E3, E4-E5, E6-E7, E15-E22, E16-E22, E26-E27, E31-E32, E34-E35, E37-E38, E39-E45, E44-E46, E64-E65, E66-E67, E74-E75, E76-E77, E91-E92, E94-E96, E97-E98, E101-E102, E103-E104, E105-E106, E107-E108, E123-E127.
iSBC 028A board with 2132A-20T RAM chips	Connect E2-E3, E4-E5, E6-E7, E15-E22, E20-E22, E26-E27, E31-E32, E34-E35, E37-E38, E40-E45, E44-E46, E61-E65, E66-E67, E76-E77, E91-E92, E94-E95, E97-E98, E101-E102, E103-E104, E105-E106, E107-E108, E123-E127, E9-E12.
iSBC 028A board with 2132A-20B RAM chips	Connect E2-E3, E4-E5, E6-E7, E15-E22, E20-E22, E26-E27, E31-E32, E34-E35, E37-E38, E41-E45, E44-E46, E61-E65, E66-E67, E76-E77, E91-E92, E94-E95, E97-E98, E101-E102, E103-E104, E105-E106, E107-E108, E123-E127, E9-E12.

Table 2-10. Jumper Configuration (as shipped) (Continued)

Board Version	Default Jumper Configuration, as shipped
iSBC 028A board with 2132A-20L RAM chips	Connect E2-E3, E4-E5, E6-E7, E15-E22, E20-E22, E26-E27, E31-E32, E34-E35, E37-E38, E39-E45, E44-E46, E61-E65, E66-E67, E76-E77, E91-E92, E94-E95, E97-E98, E101-E102, E103-E104, E105-E106, E107-E108, E123-E127, E9-E11.
iSBC 028A board with 2132A-20R RAM chips	Connect E2-E3, E4-E5, E6-E7, E15-E22, E20-E22, E26-E27, E31-E32, E34-E35, E37-E38, E39-E45, E44-E46, E61-E65, E66-E67, E76-E77, E91-E92, E94-E95, E97-E98, E101-E102, E103-E104, E105-E106, E107-E108, E123-E127, E9-E14.
iSBC 056A board with 2164A-25 RAM chips	Connect E2-E3, E4-E5, E6-E7, E15-E22, E18-E22, E26-E27, E31-E32, E34-E35, E37-E38, E39-E45, E44-E46, E59-E65, E66-E67, E76-E77, E92-E93, E94-E95, E97-E98, E101-E102, E103-E104, E105-E106, E107-E108, E123-E127, E9-E13.

2-8. MEMORY ADDRESS JUMPER CONFIGURATION

Configuration of the memory address jumpers is performed by placing the binary equivalent of the desired memory address into jumper matrices E79 through E87 and E139 through E143. Figure 2-3 shows the approximate location of the jumper matrices on the RAM boards. The starting memory address for the RAM boards is assigned in two steps:

- The first step in configuring the memory addresses for the RAM boards is to select one of 16 possible 1 megabyte pages in which the address space of the RAM boards will reside.

- The second step is to select a 4k boundary address (within the selected 1 megabyte page) to be the starting address of the on-board memory space.
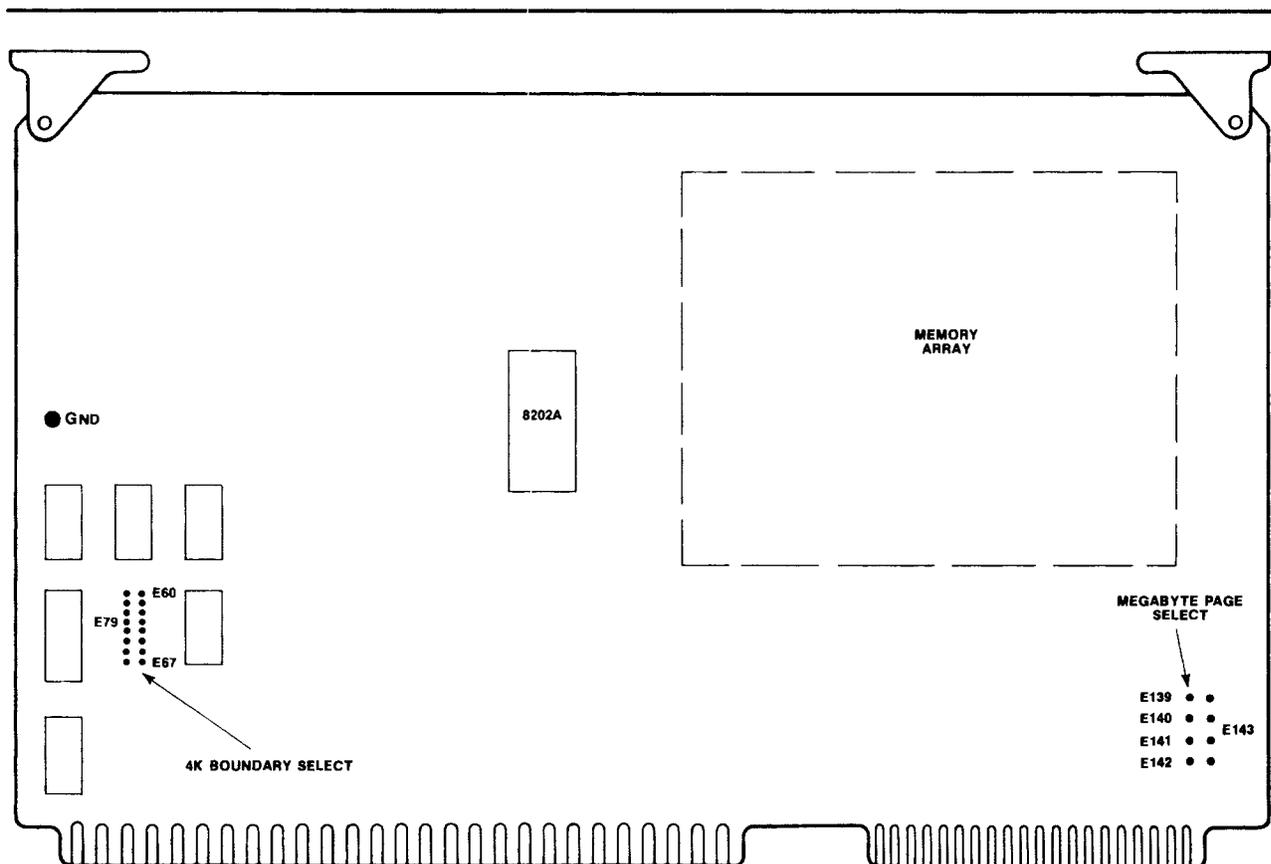
Figure 2-3. Memory Address Jumper Location Diagram

In general terms, if the desired megabyte page address is "X" and the desired starting 4k boundary is "YY", then the starting address of the boards memory space is:

"X" (megabyte) + "YY" (4k bytes) = Starting Memory Address.

where "X" and "YY" are direct decodes of the jumpers present in the respective jumper matrices. (See Figure 2-5 for example.)

The formula contains the required megabyte page address (X) and the 4k boundary select address (YY). The combination of the 3 hexadecimal digits X and YY, when assembled into one number, provides the highest 12 bits of the memory address. Since the memory can be segmented only on 4k boundaries, the lowest 3 digits of each starting memory address must be 000. Each step for configuring the address select jumpers on the RAM boards is detailed further in the following paragraphs.

2-9. MEGABYTE PAGE ADDRESS SELECT JUMPERS. The iSBC 016A/032A/064A/028A/056A RAM Boards contain four user-configured jumpers that allow user selection of the megabyte page of memory in which the on-board memory

resides; one of 16 possible 1 megabyte pages of the system memory address space. (Figure 2-4 shows the page address select jumpers (E139, E140, E141, E142, and E143) and the memory address lines (ADR14/, ADR15/, ADR16/, and ADR17) to which they are compared.

The page address select jumpers are configured as described in table 2-11. The jumper matrix decodes as a true binary representation of the actual megabyte page that is selected; E139 provides the most significant bit and E142 provides the least significant bit of the address. The presence of a jumper can be interpreted as a "1"; the absence of a jumper can be interpreted as a "0". As shipped from the factory, all RAM boards are configured to reside in megabyte page 0; i.e., all jumpers are removed.

NOTE

The RAM boards cannot increment a memory address across a megabyte page boundary. The proper megabyte page boundary must be configured in the megabyte page address select jumpers.
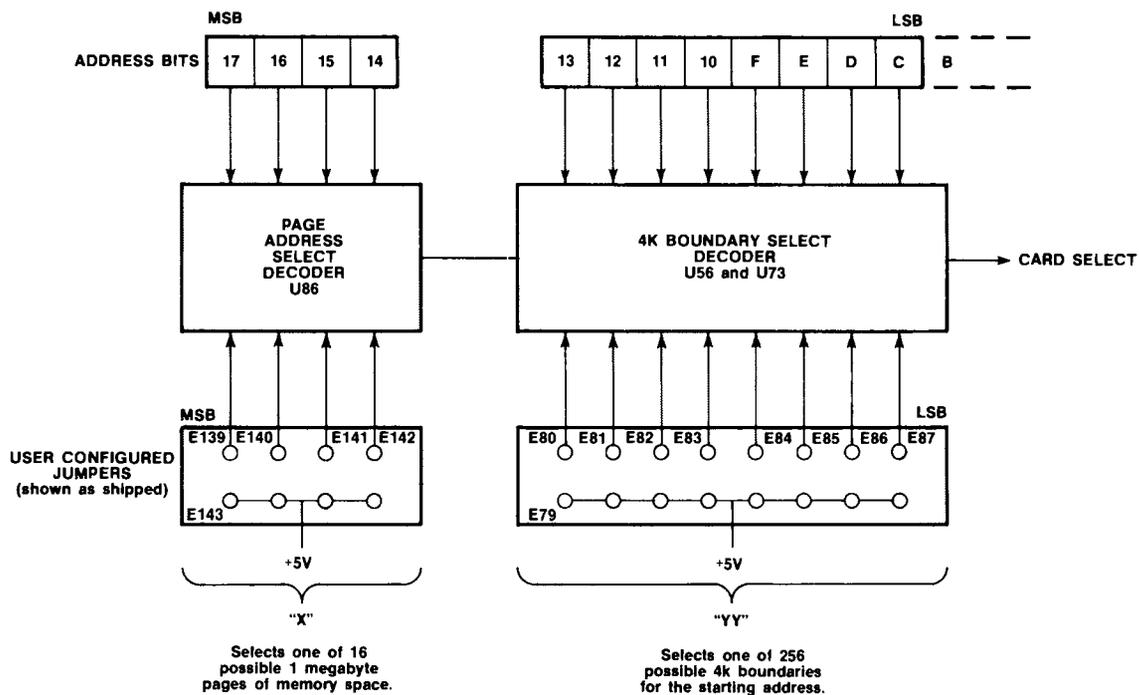
Figure 2-4. Address Selection Jumper Configuration

Table 2-11. Megabyte Page Select Jumpers

Address Space of the Board	Jumpers Required To Configure		
0 to 1Mb-1	None		
1Mb to 2Mb-1	E142-E143		
2Mb to 3Mb-1	E141-E143		
3Mb to 4Mb-1	E141-E143, E142-E143		
4Mb to 5Mb-1	E140-E143		
5Mb to 6Mb-1	E140-E143, E142-E143		
6Mb to 7Mb-1	E140-E143, E141-E143		
7Mb to 8Mb-1	E140-E143, E141-E143, E142-E143		
8Mb to 9Mb-1	E139-E143		
9Mb to 10Mb-1	E139-E143, E142-E143		
10Mb to 11Mb-1	E139-E143, E141-E143		
11Mb to 12Mb-1	E139-E143, E141-E143, E142-E143		
12Mb to 13Mb-1	E139-E143, E140-E143		
13Mb to 14Mb-1	E139-E143, E140-E143, E142-E143		
14Mb to 15Mb-1	E139-E143, E140-E143, E141-E143		
15Mb to 16Mb-1	E139-E143, E140-E143, E141-E143, E142-E143		

2-10. 4k BOUNDARY SELECT JUMPERS.

The iSBC 016A/032A/064A/028A/056A RAM Boards contain eight user-configured jumpers that assign the starting location for the memory space to any 4k address boundary (see note) within the 1 megabyte page. Figure 2-4 shows the 4k boundary select jumpers (E79 through E87) and the memory address lines (ADR13/ through ADRC/) to which the jumpers are compared.

The 4k boundary select jumper configurations are shown in table 2-12. The jumper matrix is decoded as a true binary representation of the actual 4k boundary that is selected; E80 through E83 provide the most significant bit and E84 through E87 provide the least significant bit of the address. The presence of a jumper can be interpreted as a "1"; the absence of a jumper can be interpreted as a "0". As shipped from the factory, all versions except the iSBC 032A RAM Board are configured to 4k boundary X00000H, i.e., all jumpers are removed. The iSBC 032A RAM Board, as shipped, contains a jumper at E79-E83 to configure the 4k boundary select to 32k (address X08000H).

Table 2-12. 4k Boundary Jumper Configuration Examples

Starting 4k Boundary[6]	Jumpers Required To Configure
X00000H of the megabyte page	None
X01000H of the megabyte page	E87-E79
X02000H of the megabyte page	E86-E79
X03000H of the megabyte page	E87-E79,E86-E79
X04000H of the megabyte page	E85-E79
X05000H of the megabyte page	E85-E79,E87-E79
X06000H of the megabyte page	E85-E79,E86-E79
X07000H of the megabyte page	E85-E79,E86-E79,E87-E79
[7]	
XC0000H of the megabyte page[5]	E80-E79,E81-E79
XE0000H of the megabyte page[4]	E80-E79,E81-E79,E82-E79
XF0000H of the megabyte page[3]	E80-E79,E81-E79,E82-E79,E83-E79
XF8000H of the megabyte page[2]	E80-E79,E81-E79,E82-E79,E83-E79,E84-E79
XFC000H of the megabyte page[1]	E80-E79,E81-E79,E82-E79,E83-E79,E84-E79,E85-E79

Notes:
1. The highest possible 4k boundary that does not cross a megabyte page boundary for an iSBC 016A board.
2. The highest possible 4k boundary that does not cross a megabyte page boundary for an iSBC 032A board.
3. The highest possible 4k boundary that does not cross a megabyte page boundary for an iSBC 064A board.
4. The highest possible 4k boundary that does not cross a megabyte page boundary for an iSBC 028A board.
5. The highest possible 4k boundary that does not cross a megabyte page boundary for an iSBC 056A board.
6. The upper digit (X) of each address is the megabyte page select; refer to table 2-11 for actual values.
7. The table continues in a hexadecimal decode of 256 possible configurations.

By modifying the 4k boundary select jumpers, the user may assign the memory space to start from any 4k byte boundary between 0 and 256.

NOTE

The 4k boundary for the starting memory address should be selected such that the entire memory space of the RAM board fits onto the same 1 megabyte page of memory. Failure to do so will cause the off-page portion of memory to be inaccessible.

NOTE

The memory on one RAM board must be assigned contiguously within a 1 megabyte page starting at a selected 4k boundary.

2-11. RAM BOARD ADDRESS CONFIGURATION EXAMPLE.
The iSBC 016A/032A/064A/028A/056A RAM Boards must be assigned to the memory space so that all memory locations are accessible within the megabyte of memory space. This requires that the starting address for the lowest 4k byte segment be less than or equal to the addresses listed in table 2-13. To assign the memory segments to address space within the megabyte of on-board memory space, use the formula:

"X" (megabyte) + "YY" (4k bytes) = Starting Memory Address.

NOTE

Banks 0 and 1 always operate as a pair; for a word operation, bank 0 holds the odd byte and bank 1 holds the even byte.

Table 2-13. Maximum Starting 4k Boundary

RAM Board	Maximum 4k Boundary Selected
iSBC 016A RAM Board	XFC000H
iSBC 032A RAM Board	XF8000H
iSBC 064A RAM Board	XF0000H
iSBC 028A RAM Board	XE0000H
iSBC 056A RAM Board	XC0000H
Note: "X" is the megabyte page address.	

a. Determine which megabyte page address to use, and convert it to hexadecimal. Then place the hexadecimal equivalent of the number (listed as "X" in the formula and in figure 2-5) into the jumper matrix; E139 is the MSB and E142 is the LSB (presence of a jumper equals a "1").

b. Determine which starting 4k boundary to use, and convert it to hexadecimal. Then place the hexadecimal equivalent of the number (listed as "YY" in the formula and in figure 2-5) into the jumper matrix; E80 is the MSB and E87 is the LSB (presence of a jumper equals a "1").
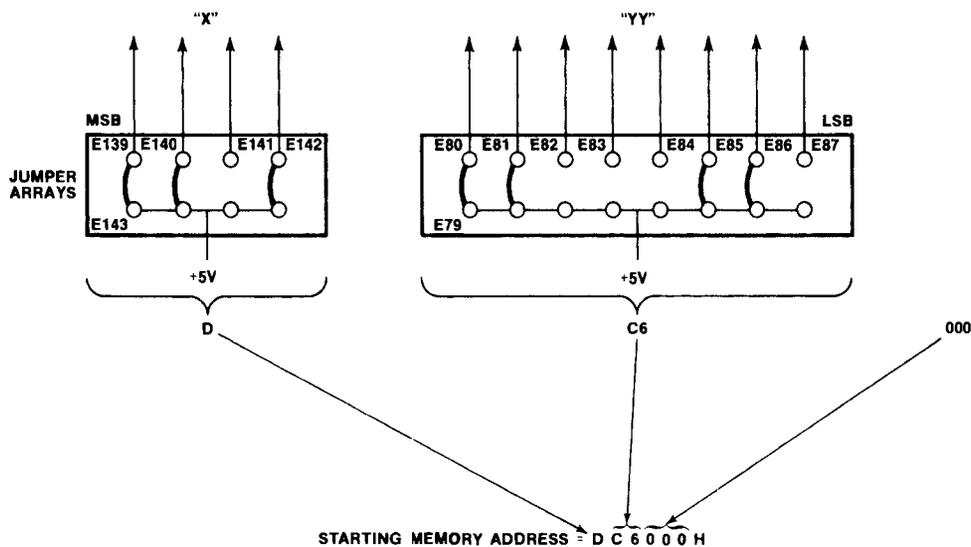
Figure 2-5. Address Jumper Configuration Example

2-12. DELAYED/ADVANCED WRITE JUMPER CONFIGURATION

Most systems operate in a Delayed (normal) WRITE mode. That is, the Memory WRITE Command is issued to the RAM board a minimum of 50 nanoseconds after the write data and memory address are placed on the Multibus interface. This is the normal mode of operation for the iSBC 016A/032A/064A/028A/056A RAM Boards. As shipped, each version of the RAM board contains a jumper connecting E2-E3 to enable the Delayed WRITE mode operation on the board.

For the iSBC 064A RAM Board, the Delayed WRITE mode operation can be eliminated and the Advanced WRITE (or non-qualified WRITE) mode can be enabled by removing the jumper E2-E3 and installing one at E1-E2. Systems requiring an Advanced WRITE mode are those that must receive a Memory WRITE Command from the bus master a maximum of 500 nanoseconds before the write data is placed onto the Multibus interface. The Advanced WRITE mode is required for operation with an MDS 800 Development System or an ICE 80 Emulator.

2-13. PARITY FLAG REGISTER ADDRESS JUMPER CONFIGURATION

The configuration of jumpers E76, E77, E78, E103 through E108, and E110 through E114 determines the Multibus I/O port address at which the bus master can access the Parity Flag Register within the RAM boards. As shipped, the RAM boards contain jumpers to configure the Parity Flag Register I/O port address to 000FH. The jumpers allow the user a two part selection of the I/O port address:

* Jumpers E103 through E108 allow user selection of the number of bits of Multibus address to be considered in decoding the I/O port address required to access the Parity Flag Register; either 8-bits, 12-bits, or 16-bits. Refer to table 2-14 for the jumper connections.

* Jumpers E76, E77, E78, and E110 through E114 allow user selection of the state (active or inactive) of Multibus address lines ADR0/, ADR1/, ADR2/, ADR3/, and ADR6/ to generate the IOCS/ signal required to access the Parity Flag Register. Refer to table 2-15 for jumper connections.

Table 2-14. I/O Address Line Enables for Parity Flag Register

Jumper Connection	Description
E103-E104*	Enable address lines ADRC/, ADRD/, ADRE/, and ADRF/ into the I/O port address decode logic when jumper installed.
E105-E106*	Enable address lines ADR8/, ADR9/, ADRA/, and ADRB/ into the I/O port address decode logic when jumper installed.
E107-E108*	Enable address lines ADR0/, ADR1/, ADR2/, ADR3/, ADR4/, ADR5/, ADR6/, and ADR7/ into the address decode logic when jumper installed.
E108-E109	Disables the operation of the Parity Error Flag. (016A version only.)
NOTE: *indicates that the jumpers are installed at the factory before shipping.	

Table 2-15. I/O Port Address Selection

Jumper	Function
E76-E77 Installed*	Enables the I/O port address decode when Multibus address line 6 (ADR6) is LOW. Jumper E107-E108 must be installed.
E77-E78 Installed	Enables the I/O port address decode when Multibus address line 6 (ADR6) is HIGH. Jumper E107-E108 must be installed.
E110-E111 Installed	Enables Multibus address line 3 (ADR3) into the I/O port address decode when LOW.
E110-E111 Removed*	Enables Multibus address line 3 (ADR3) into the I/O port address decode when HIGH.
E110-E112 Installed	Enables Multibus address line 2 (ADR2) into the I/O port address decode when LOW.
E110-E112 Removed*	Enables Multibus address line 2 (ADR2) into the I/O port address decode when HIGH.
E110-E113 Installed	Enables Multibus address line 1 (ADR1) into the I/O port address decode when LOW.
E110-E113 Removed*	Enables Multibus address line 1 (ADR1) into the I/O port address decode when HIGH.
E110-E114 Installed	Enables Multibus address line 0 (ADR0) into the I/O port address decode when LOW.
E110-E114 Removed*	Enables Multibus address line 0 (ADR0) into the I/O port address decode when HIGH.
NOTE: * indicates that the jumpers are installed at the factory before shipment.	

2-14. BATTERY BACK-UP/MEMORY PROTECT JUMPER CONFIGURATION

In systems employing a battery back-up memory protect feature, the user must provide and install a P2 connector for the Intel iSBC cardcage. Compatible connectors listed in table 2-8 include both soldered and wirewrapped types of connectors. Procure the required connector at a local electronic parts supplier.

When the P2 connector is secured into place, solder the battery back-up, memory protect, and address lines to the appropriate pins of the connector, as listed in table 2-4.

When battery back-up power is to be installed for use with the RAM boards, disconnect the system power from the RAM boards. Then remove the jumpers E146-E47, E116-E117, E118-E120, and E119-E120 to separate the +5 volt battery bus on connector P2 pins 3 and 4 from the Multibus +5 volt bus.

CAUTION

Always remove both battery back-up and system power from the RAM boards before installing or removing the boards from a system cardcage. Failure to do so could result in damage to the boards.

2-15. BOARD INSTALLATION

The iSBC 016A/032A/064A/028A/056A RAM Boards are compatible with the Intel iSBC 604/614 Cardcage. In a single board computer based system, install the RAM board into any cardcage slot that is not wired for a dedicated function. Ensure that the auxiliary connector P2 (if used) is mated properly with the user installed connector.

3-1. INTRODUCTION

Data is written to and read from the RAM boards through normal Memory READ and Memory WRITE operations. However, the contents of the Parity Flag Register is accessed through I/O READ and I/O WRITE operations. The following paragraphs provide a description of the Parity Flag Register.

3-2. PORT ADDRESS

The Parity Flag Register is addressed as though it were an I/O device on the RAM boards. An I/O port address is selected by the user through configuration of jumpers E77, E78, E104 through E108, and E110 through E114 as described in paragraph 2-17 and shown in tables 2-14 and 2-15. The jumpers allow user selection of the quantity of Multibus address lines to be used in performing the selection and the state of address lines ADR0/, ADR1/, ADR2/, ADR3/, and ADR6/ that is required for the selection; the remaining Multibus address lines must be inactive.

3-3. PARITY FLAG REGISTER FORMAT

The Parity Flag Register, in the event of a parity error, provides the location of the parity error. Figure 3-1 shows the format of the parity Flag Register on the RAM boards.

The I/O port address serves two functions, 1) on an I/O READ, the Multibus master can access the contents of the Parity Flag Register, and 2) on an I/O WRITE, the Multibus master can reset the Parity Flag Register contents and, if desired, change the type of parity generated by the RAM boards.
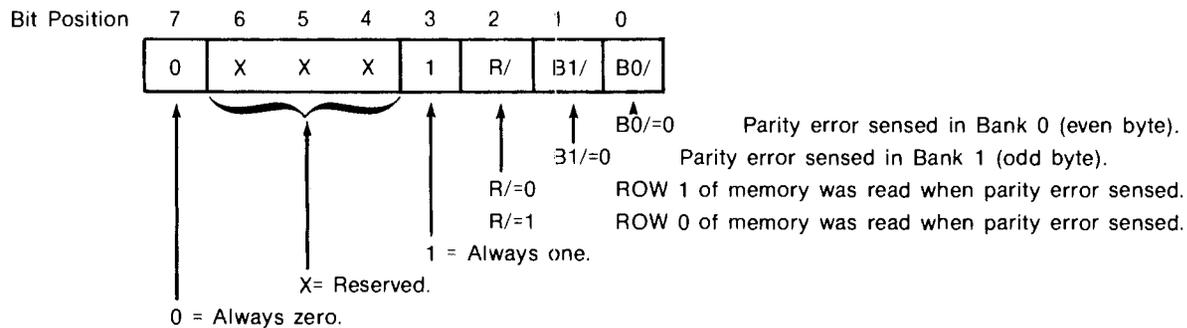

Figure 3-1. Parity Flag Register Format

4-1. INTRODUCTION

This chapter provides a functional description and a detailed circuit analysis of the operation of the iSBC 016A/032A/064A/028A/056A RAM Boards. Figure 4-1 is a block diagram of the major logic functions of the RAM boards. The following paragraphs contain a functional description of each of the major areas of the RAM boards and, beginning at paragraph 4-11, a detailed circuit analysis of the RAM boards.

4-2. FUNCTIONAL DESCRIPTION

The iSBC 016A/032A/064A/028A/056A RAM Boards (figure 4-1) are divided into six functional areas: memory address buffers, RAM array, Dynamic RAM Controller, memory I/O buffers, control logic, and parity generate/check logic (on all but the iSBC 016A RAM Board). Upon receiving a command from the Multibus interface, the RAM boards read data from or writes data into the RAM storage area. Except for the data flow, both operations require that the same sequence occur.

All data transferred between the iSBC 016A/032A/064A/028A/056A RAM Boards and the bus master is performed via the Multibus interface. Data is channelled between the Multibus interface and the on-board RAM chips via bidirectional data buffers that maintain signal compatibility between the board and the bus. The Dynamic RAM Controller generates timing and control signals required to synchronize the data transfer operations.

A typical operation on the iSBC 016A/032A/064A/028A/056A RAM Boards is initiated when the bus master issues a memory address to all devices on the Multibus interface. The address is decoded by the select logic on the RAM boards to prepare the boards for the command that is following. After sending the address to or from which data is to be transferred, the bus master may issue the READ or WRITE command to start the operation. The command is placed onto the Multibus interface a minimum of 50 nanoseconds after the address.

If a READ command is sensed from the Multibus interface, the RAM boards perform a sequence of operations to READ data from the addressed memory location and place its contents onto the Multibus interface data bus (DAT0/ through DATF/). When the data has stabilized on the bus, the RAM boards issue a Transfer Acknowledge signal (XACK/) to the bus master indicating that the data is available on the Multibus interface. In response to the Transfer Acknowledge signal, the bus master accepts the data from the Multibus interface and removes the READ command (MRDC/) and the RAM address from the Multibus control and address lines.

If a WRITE command is sensed from the Multibus interface, the RAM boards perform a sequence of operations to WRITE a data byte into the memory at the address provided by the bus master via the Multibus interface address lines (ADR0/ through ADR17/). The bus master places the write data onto the Multibus interface coincident with issuing an address. The bus master then issues a WRITE command to the RAM boards after the data stablizes on the Multibus interface. On receiving the command, the RAM board performs the WRITE operation; a sequence of events to write the data byte from the Multibus interface into the addressed RAM memory location. On completion of the WRITE operation, the control logic for the RAM boards send a Transfer Acknowledge signal (XACK/) to the bus master indicating that the operation is completed. In response to the XACK/ signal, the bus master removes the WRITE command (MWTC/) from the Multibus interface. A minimum of 50 nanoseconds later, the bus master deactivates the data lines and the address lines on the Multibus interface.

The refresh logic required by the dynamic RAM chips is internal to the Dynamic RAM Controller. The refresh logic is capable of providing refresh for one row of memory cells each 15 microseconds. An off-board RAM refresh request is sensed by the Dynamic RAM Controller when the RFQST/ line on the P2 connector goes LOW. The RAM refresh logic will allow the off-board request to speed up the RAM refresh rate, however, it will not allow refresh generation at a rate slower than that of the internal refresh logic. After a refresh cycle is requested, the actual execution may be delayed, but never longer than one READ or WRITE cycle.

The RAM board includes a feature by which auxiliary power may be supplied through the P2 connector. This allows the RAM board to maintain the integrity of the RAM data in the event of a power failure.

For each word of data read from or written to the memory array, two parity bits are generated; one for each byte. The parity bits provide even parity, are stored in the parity storage RAMs, and are made available to the bus master via the P2 connector.
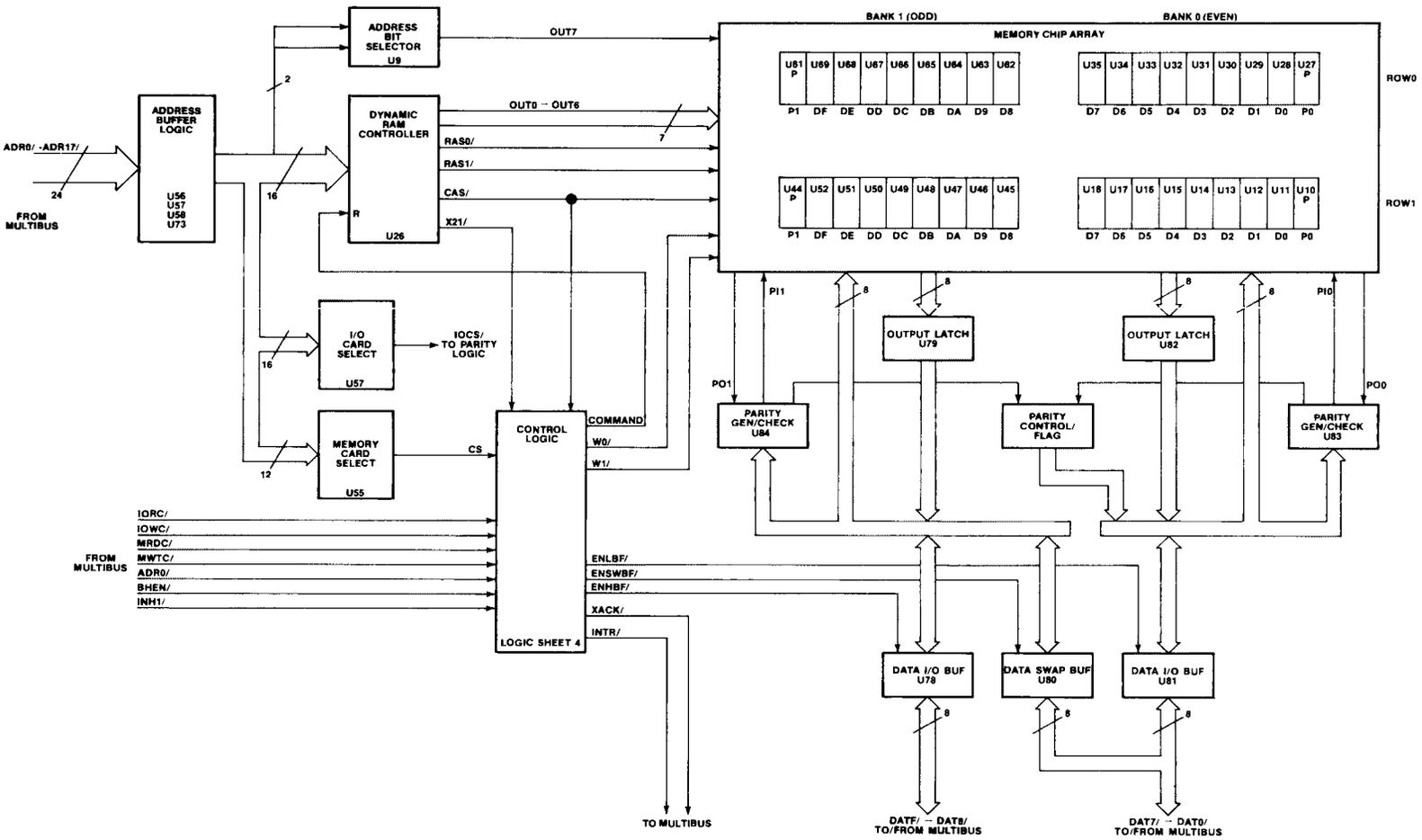
Figure 4-1. iSBC 016A/032A/064A/028A/056A™ RAM Boards Block Diagram

The P2 connector also includes the memory protect line (MPRO/) from the bus master. When asserted, the MPRO/ signal denies all access to the RAM memory and provides protection for the RAM contents during a power failure.

4-3. DYNAMIC RAM CONTROLLER

The RAM board contains a Dynamic RAM Controller that provides multiplexed addresses, address strobes, and refresh/access arbitration. The Dynamic RAM Controller is directly addressed and contributes to the RAM boards control of up to 256k bytes of RAM memory and is fully compatible with the Intel 8080A, 8085A, 8086, 8088, and 8089 microprocessors. Memory refresh cycles may be internally or externally requested and internally or externally clocked. The Dynamic RAM Controller generates the ROW address select signals (RAS0/, RAS1/, RAS2/, and RAS3/) and the COLUMN address select signal (CAS/) required to enable the memory array during READ, WRITE, and REFRESH operations. More information on the operation of the Dynamic RAM Controller is available in the *Intel Peripheral Design Handbook*.

At any given instant, the Dynamic RAM Controller on the RAM boards may be found in one of the following states: IDLE, WRITE cycle, READ cycle, or REFRESH cycle. In IDLE, the Dynamic RAM Controller monitors internal and external cycle requests and counts toward generation of an internal refresh cycle for the RAM chips.

A WRITE cycle is generated on the RAM board when the READ input to the Dynamic RAM Controller (RD/ on pin-32) is held LOW. During the WRITE cycle, an address is input from the Multibus interface to generate the ROW, COLUMN, and BANK addresses for the memory array. The Dynamic RAM Controller generates ROW and COLUMN address strobe signals (RAS/ and CAS/) when the ROW and COLUMN addresses are valid and the RAM board generates the write enable signals (W0/ and W1/) to the memory array. With the RAS/, CAS/, W0/, and W1/ signals, the RAM board begins the data storage operation. Shortly thereafter, the Dynamic RAM Controller generates X2/ to indicate that the data storage operation is completed and enable the next. If a REFRESH cycle request is received during a write operation, the REFRESH cycle is generated immediately following the WRITE cycle.

The READ cycle within the Dynamic RAM Controller is identical to that of the WRITE cycle except that the write enable signals (W0/ and W1/) on the RAM board are not generated, implying a READ operation. If a REFRESH cycle request is received during a READ operation, a REFRESH cycle will occur immediately following the READ cycle.

A REFRESH cycle on the RAM board begins within the Dynamic RAM Controller and may be generated from one of two sources; 1) the Dynamic RAM Controller contains an internal Refresh Timer that performs the REFRESH cycle automatically, and 2) an external REFRESH cycle can be requested of the Dynamic RAM Controller via the REFRQ/ signal from the bus master (REFRQ/ is active LOW on pin 40 of the P2 Connector). When an external REFRESH cycle is requested, the Dynamic RAM Controller resets the internal Refresh Timer to zero and places the internally generated Refresh Address (ROW and COLUMN addresses) onto the OUT0/ through OUT6/ address lines. In doing so, the Dynamic RAM Controller also activates the RAS/ signals to enable access to the memory array. The timing required for an internally and an externally requested REFRESH cycle is identical.

4-4. DYNAMIC RAM CONTROLLER INTERFACE. The signals input to the Dynamic RAM Controller include the memory COLUMN (AH0-AH6), memory ROW (AL0-AL6), and memory BANK (B0 and B1) address lines. The signals output from the Dynamic RAM Controller include the address output for the RAM array (OUT0/-OUT6/), the COLUMN Address Strobe (CAS/), the ROW Address Strobe (RAS0/-RAS3/), and the Transfer Acknowledge (XACK/) signal. The functions performed by each of these is described in the following paragraphs.

AL0 THROUGH AL7 (LOW ORDER ADDRESS). The Low Order Address input lines generate the ROW address for the memory array as OUT0/ through OUT6/ from pins 7, 9, 11, 13, 15, 17, and 19 of the Dynamic RAM Controller. When made available from the Dynamic RAM Controller, the address is latched into the memory array by the RAS0/ through RAS3/ signals.

AH0 THROUGH AH7 (HIGH ORDER ADDRESS). The High Order Address input lines generate the COLUMN ADDRESS for the memory array as OUT0/ through OUT6/ from pins 7, 9, 11, 13, 15, 17, and 19 of the Dynamic RAM Controller. When made available from the Dynamic RAM Controller, the address is latched into the memory array by the CAS/ signal.

B0 AND B1 (BANK ADDRESS SELECT). The BANK Address Select inputs are user selectable to generate a select signal from RAS0/ through RAS3/ that selects one of four BANKs of RAM.

CAS/ (COLUMN ADDRESS SELECT). This active LOW output signal from the Dynamic RAM Controller is used as an enable for all RAM chips in the RAM array.

RAS0/-RAS3/ (ROW ADDRESS SELECT).
This active LOW output from the Dynamic RAM
Controller that is a decode of the B0 line input to the
Dynamic RAM Controller from the Multibus inter-
face. The RAS/ lines are used to select the row of
RAM chips in the RAM array that is to be accessed.

OUT0/-OUT7/ (DATA OUTPUT LINES). These
active LOW output signals from the Dynamic RAM
Controller provide the RAM chip that is selected by
the CAS/ and RAS/ signals with an address to
which data is read or written.

X2/ (TRANSFER ACKNOWLEDGE). The Trans-
fer Acknowledge signal from the Dynamic RAM
Controller is an active LOW output to the command
sensing logic on the RAM board. For a READ or
WRITE operation, the X2/ signal resets the Memory
READ/Memory WRITE command sensing logic
(U4/U57 on 4ZD6) after completion of the command
execution cycle within the Dynamic RAM Controller
so that the next command from the Multibus
interface can be sensed and executed.

4-5. ADDRESS BUFFERS

The address lines from the Multibus interface are
buffered on the RAM board by U74, U76, and U77,
three high impedance, octal, line driver/receiver
buffers. All addresses from the Multibus interface
are buffered in the address buffers. The outputs from
the buffers are used as inputs to the Dynamic RAM
Controller and the address decode logic.

4-6. ADDRESS DECODE LOGIC

The address decode logic is shown on sheet 2 of the
schematic drawings and consists of two 74S85 4-bit
comparator chips (U86 and U59 on schematic sheet
2) and two 74S283 4-bit Binary Full Adder chips
(U73 and U56). User configured jumper arrays are
input to the comparator and adder chips and
compared with the memory address lines presented
by the bus master on ADR0/ through ADR17/. The
Multibus address lines are decoded into board select
signals for the memory array (CS/ on 2ZB2) and the
on-board I/O device (IOCS/ on 2ZC2). The CS/ and
IOCS/ signals generate memory enable and com-
mand decode signals.

4-7. MEMORY ARRAY

The configuration of the memory array depends on
the type of memory chips installed onto the RAM
boards. The RAM boards accept 2110, 2118, 2132A,

and 2164A Dynamic RAM chips; however, they can-
not accept a mixture of the various types of chips.
Figure 4-2 shows the typical layout of the memory
array on the iSBC 032A/064A/028A/056A RAM
Boards, including the odd/even byte and the ROW0/
ROW1 memory arrangement. The iSBC 016A RAM
Board layout is similar, however, it includes only the
memory chips labeled as ROW 0; ROW 1 is not avail-
able. The memory array is configured at the factory
before shipment, is defined by the quantity and type
of memory chips installed onto the RAM boards, and
is not intended to be modified by the user.

4-8. DATA I/O BUFFERS

Two 74S373 output buffers (U79 and U82) and three
8286 bidirectional 8-bit buffers provide the interface
to the Multibus data lines. As figure 4-1 shows, the
high and low bytes of data may be multiplexed
directly onto the Multibus interface if the system is
capable of handling 16-bit data transfers.

4-9. PARITY GENERATION/CHECKING
LOGIC

Parity generating, checking, and storing logic is not
available on the iSBC 016A RAM Board and is
provided as a standard feature on the iSBC 032A/
064A/028A/056A RAM Boards when configured as
shipped. The following discussion describes the
operation of the parity generating and checking
circuitry that is shipped with the iSBC 032A/064A/
028A/056A RAM Boards.

The parity circuitry on the RAM boards consists of
Parity Storage RAMs (U10, U27, U44, and U61; one
for the high byte and one for the low byte of each
BANK of memory), two parity generator/checker
devices (U83 and U84; one for each byte), a four bit
Parity Flag Register (U8), an Error Test Latch (U41
pin-6), an Error Interrupt Request Latch (U41 pin-8),
and several logic gates (U5, U23, U54, and U60).
These components ensure that each byte of data
read from or written to the RAM array conforms to
the even parity requirement configured on the RAM
boards.

When a byte of data is read from the RAM array, a
parity bit is also read and input with the data byte
into the Parity Generator/Checker devices (U83 and
U84 on 5ZC7). When a byte of data is written to the
RAM array, the on-board Parity Generator/Checker
senses the data (via DI0 through DIF from the
Multibus interface) and generates an even parity bit
for each byte of data. Upon sensing a parity error,
the RAM boards store the memory ROW and BANK
number in the Parity Flag Register, illuminate the
Parity Error indicator, and generate INTR5/ to the

bus master to request an interrupt. In response to the Interrupt Request, the bus master must perform one of three functions to service the request:

1) The bus master could issue a Multibus RESET signal (INIT/) to reset the Parity Flag Register and remove the Interrupt Request,

2) The bus master could issue an I/O READ command to the RAM boards to read the contents of the Parity Flag Register and remove the Interrupt Request, or

3) The bus master could issue an I/O WRITE command to the RAM boards to write a value into flipflop U41 (schematic sheet 5ZC3), reset the Parity Flag Register, and remove the Interrupt Request.

As the Interrupt Request signal is removed, the Parity Error indicator on the RAM boards is extinguished.

4-10. CONTROL LOGIC

The control logic (schematic sheet 4) consists of the on-board circuitry for generating and decoding the Multibus control signals that are required by the RAM board and the bus master. The input signals operating the control logic are MRDC/, MWTC/, INH1/ (generated by the bus master), BHEN/, and ADR0/. These signals control the logical generation of the Write Enable signals for BANKs 0 and 1 (W0/ and W1/), the I/O buffer enable signals (ENHBF/, ENSWBF/, and ENLBF/), and the Transfer Acknowledge signal (XACK/) which, in turn, control the execution of a command.

4-11. DETAILED CIRCUIT ANALYSIS

The following paragraphs describe detailed logic circuit operations on the RAM boards. Included are operational descriptions for the board addressing, memory partitioning, command operation descriptions, data transfer modes, memory protect operation, parity generator/checker operation, parity test operation, and interrupt generation.
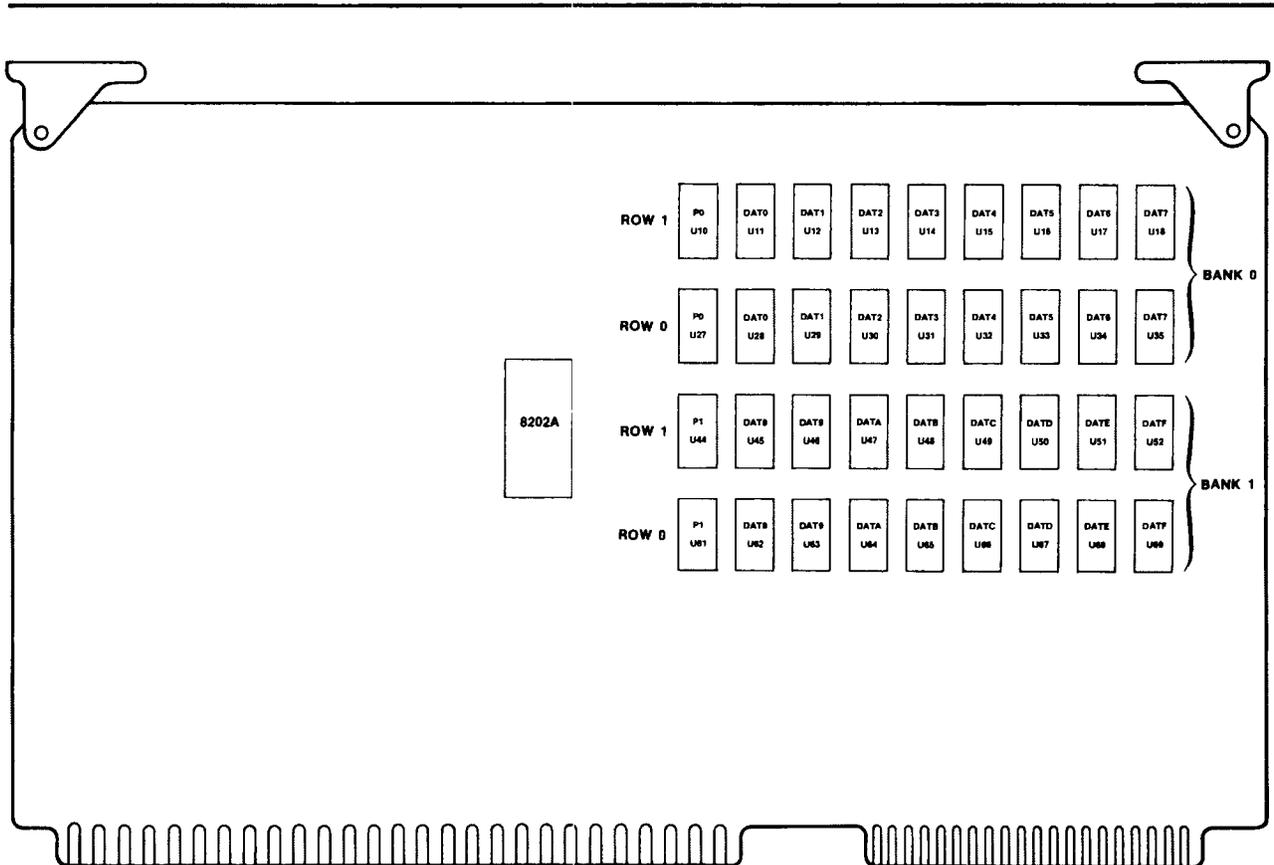

Figure 4-2. Memory Array Layout

4-12. ADDRESS AND DATA ROUTING

The address and data routing is similar for each version of the RAM boards. During a READ operation, the MRDC/ command from the Multibus interface generates a READ cycle within the Dynamic RAM Controller that accesses the memory location defined by the state of the Multibus address lines (ADR0/ through ADR17/). The Dynamic RAM Controller generates RAS/, CAS/, and OUT0/-OUT6/ to the memory array which responds with a data word on data output lines DO0/ through DOF/. When the Dynamic RAM Controller generates its internal Transfer Acknowledge signal (X21/ from pin-29 of U26), the READ buffers (U80 and U78 on 5ZC6) are enabled to latch the data and the command execution within the Dynamic RAM Controller is completed. However, in an effort to speed up the data transfer operation, the logic on the RAM boards generates an earlier Transfer Acknowledge signal (XACK/) that is made available to the Multibus interface approximately 100 nanoseconds before X2/. By providing XACK/, the RAM boards allow the bus master to accept the READ data earlier from the Multibus interface.

When the MRDC/ signal from the Multibus is decoded with ADR0 and BHEN/, the Control logic generates one or more of the I/O buffer enable terms (ENHBF/, ENSWBF/, and ENLBF/ on schematic sheet 4), and the other enable term required (END-LTCH). With the generation of the required enable terms, the data from memory is gated into the READ buffers (U80 and U78 on 5ZC6) and into the bidirectional Multibus interface buffer/drivers (U78, U80, and U81). After the data is placed onto the Multibus interface, the Transfer Acknowledge signal (X2/) is generated from the Dynamic RAM Controller to indicate to RAM board logic that the cycle is completed. That valid data is available on DAT0/ through DATF/ (for a 16-bit operation).

4-13. MEMORY PARTITIONING

A maximum of 24-bits of address from the Multibus interface provides board selection for the RAM boards and divides the memory address into a 4-bit

megabyte page select (ADR14/ through ADR17/), an 8-bit 4k boundary select for starting memory address (ADRC/ through ADR13/), and a ROW/COLUMN/BANK address select required for the Dynamic RAM Controller to access the memory array.

The memory on the RAM boards is organized in two ROWs (one ROW for the iSBC 016A RAM Board). Each ROW is divided into two 8-bit BANKs. A full 16-bit WRITE operation places 16 bits of data into the RAM, one byte into BANK 1 (the odd bytes) and one byte into BANK 0 (the even bytes) of a ROW. Table 4-1 shows the logical organization of the memory array, including the most and least significant bits of each byte and the RAM chips in which the bits are stored.

The 4 high order memory address lines from the Multibus interface (ADR14/, ADR15/, ADR16/, and ADR17/) are compared, via a 4-bit comparator U48, with the user-selected address range to determine if the memory address from the Multibus interface is within the RAM board's memory address space. The 4-bit Full Adder devices (U73 and U56) decode address bits ADRD/ through ADR13/ to select a 4k address boundary from which the on-board memory space is assigned. The Adder devices compare the user-selected 4k byte address boundary with that of the address on the Multibus interface and either enable or disable the memory devices via U55 pin-5. The memory address lines for all versions of the RAM board are decoded as shown in figure 2-4. The jumper configuration required for each version of the RAM boards is shown in tables 2-11 and 2-12.

NOTE

The memory addressing options available for the "A" version of the RAM boards are not compatible with that of the "non-A" version. The "A" version does not allow division of the memory address space into 16k blocks that are moveable independent of each other; rather the memory address space must remain a contiguous block.

Table 4-1. Memory ARRAY Organization

	High Byte (odd) BANK 1 (MSB)								Low Byte (even) BANK 0 (LSB)							
Data Bits	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
RAM IC Numbers ROW 0	A70	A69	A68	A67	A66	A65	A64	A63	A35	A34	A33	A32	A31	A30	A29	A28
RAM IC Numbers ROW 1	A52	A51	A50	A49	A48	A47	A46	A45	A17	A16	A15	A14	A13	A12	A11	A10

4-14. MEMORY READ COMMAND

When a memory READ command (MRDC/) is received from the Multibus interface, the latch (comprised of U4 pins 4, 5, and 6, and U57 pins 1, 2, 12, and 13 on schematic sheet 4ZD6) sets to provide an indication that a command is sensed. The indication is passed to the Dynamic RAM Controller in the form of a LOW on pin 32 of U26 which starts the operation.

The Dynamic RAM Controller initiates a READ operation when the RD/ input (pin-32) is activated (LOW) and begins generation of the RAS/ and CAS/ signals (schematic sheet 3ZB6) to the memory array. The RAS/ signals select the ROW address and provide a decode of the condition of the B0 and B1 inputs (the BANK address of the RAM). The CAS/ signal selects the COLUMN address for the BANK of the RAM memory array. The CAS/ signal also

clocks flipflop U3 (schematic sheet 4ZA6) to the set condition. This flipflop performs two functions;

1) The set output from the flipflop triggers the delay logic if INH1/ is inactive. The delay logic generates a 100ns delay between generation of the COLUMN Address Select signal (CAS/) and the Transfer Acknowledge signal (XACK).

2) The output from U3 also generates through U39 pin-8 (4ZC5) a pulse that resets the U4/U57 latch output after the Multibus READ command (MRDC/) is removed by the bus master. The pin-12 output from U57 drops LOW to remove the READ operation request from the Dynamic RAM Controller.

Figure 4-3 shows the timing for a READ operation in which the bus master issues a READ command to the RAM board and the RAM board responds by placing data and parity onto the Multibus interface.
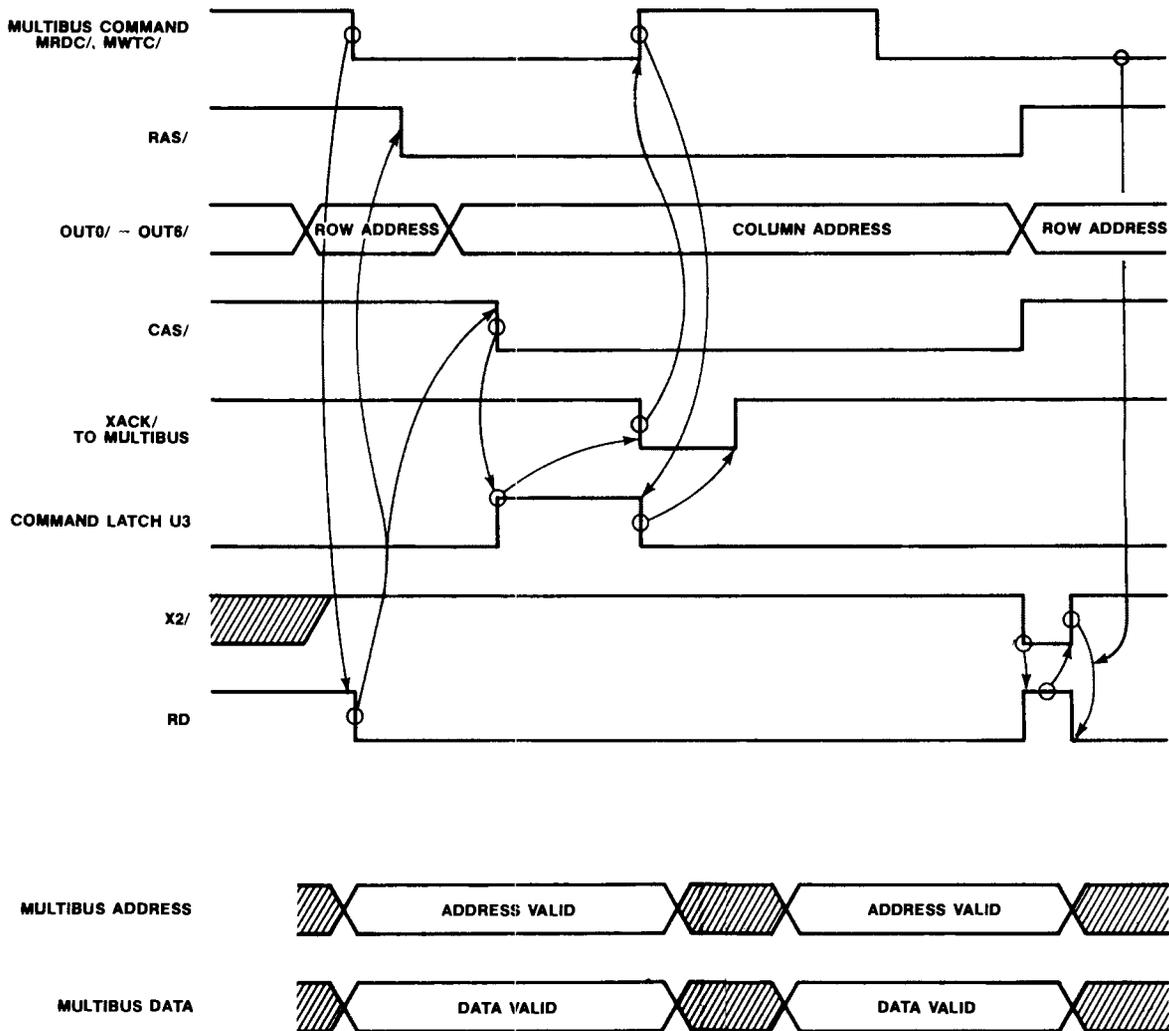

Figure 4-3. READ and WRITE Command Timing

When a Multibus command is sensed, the U4/U57 flipflop sets and generates a LOW input to RD/ (the pin-32 input to the Dynamic RAM Controller). RD/ causes the Dynamic RAM Controller to generate the required CAS/ and RAS/ signals for the command. CAS/ in turn sets U3 to partially disable the resetting of U4/U57 until completion of the Multibus cycle. When the Dynamic RAM Controller generates its transfer acknowledge signal (X2/) and the Multibus cycle is completed, the flipflop U4/U57 is reset and the RAM board can begin execution of the next Multibus command.

Another Multibus command could follow the previous one by as little as 100 nanoseconds. The actual execution of the next Multibus command will not begin until after the Dynamic RAM Controller has provided a Transfer Acknowledge signal (X2/) to the RAM board indicating that the previous command execution is completed successfully. As X2/ is generated LOW, it resets the U4/U57 flipflop which removes the RD/ input to the Dynamic RAM Controller that was generated by the previous command. Removal of the RD/ input enables the Dynamic RAM Controller to drop the X2/ signal to an inactive state. Removal of the X2/ signal, in turn, allows the RAM board to sense the next command waiting on the Multibus interface.

4-15. MEMORY WRITE COMMAND

A WRITE command is initiated on the RAM board when the memory write command from the Multibus interface is LOW (MWTC/ = 0). The command is decoded similar to the sequence used for the READ operation; the RD/ input to the Dynamic RAM Controller is pulled LOW. The U4/U57 latch sets as for a READ operation, however, MWTC/ generates a LOW from U4 pin-3 (4ZC7) and a HIGH from U38 pin-4 (4ZB7) to enable generation of the Write Enable signals (W0/ an W1/ from U25 on schematic sheet 4ZC3). Figure 4-3 shows the timing for a typical WRITE command on the RAM boards.

The Dynamic RAM Controller initiates a WRITE operation in the same manner as a READ operation, the RD/ input (pin-32) to the Dynamic RAM Controller is activated to generate the RAS/ and CAS/ signals (schematic sheet 3ZB6) to the memory array. The RAS/ signals select the ROW address and provide a decode of the condition of the B0 and B1 inputs (the BANK address of the RAM). The CAS/ signal selects the COLUMN address for the BANK of the RAM memory array. The CAS/ signal also clocks flipflop U3 (schematic sheet 4ZA6) to the set condition. This flipflop performs three functions as described for the READ operation.

4-16. REFRESH COMMAND

As shipped, the Dynamic RAM Controller is configured to internally generate REFRESH cycles for the RAM devices. A Refresh Timer and a Refresh Counter operate internal to the Dynamic RAM Controller in generating a RAM REFRESH signal at a regular interval; once each 15 microseconds (maximum). The RAM boards also accept via pin-40 of the P2 connector a special input for an external REFRESH request signal (REFRQ/). A LOW on pin-40 indicates to the Dynamic RAM Controller that an external REFRESH signal is requested.

When the either REFRESH request is sensed, the Dynamic RAM Controller generates a REFRESH address on OUT0/ through OUT6/ to the memory chips. The REFRESH address is sent to the memory array and the REFRESH cycle is performed when the Dynamic RAM Controller generates the RAS/ signals. The use of the external REFRESH signal can only increase the rate of refresh; it cannot decrease the rate of refresh to a speed less than that of the internal refresh rate. Figure 4-4 shows the timing requirements of the internally and externally requested REFRESH cycle.
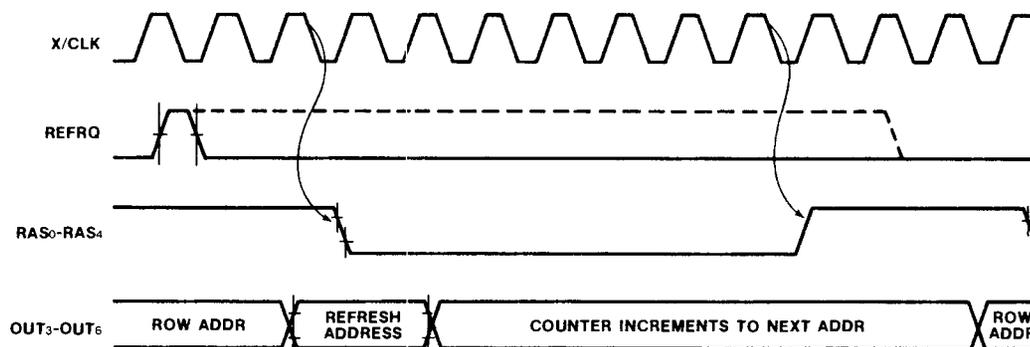

Figure 4-4. External REFRESH Command Timing

4-17. DATA TRANSFER MODES

Each version of RAM board contains three 8286 Bidirectional Octal Bus Transceiver devices at chip locations U78, U80, and U81 to buffer the input and output data for the boards. As table 4-2 shows, the transceiver devices provide the interface between the Multibus structure and the board and a buffer for performing a data swap operation; i.e., placing the HIGH order data byte from memory onto the LOW order Multibus interface lines during an output operation, and placing the LOW order data byte from the Multibus interface onto the HIGH order memory during an input operation. When not in use, the interface buffers are held in a high impedance state to minimize the loading effects on the Multibus structure.

The bidirectional transceiver devices are enabled via the ENLBF/ (for U81), ENHBF/ (for U78), and ENSWBF/ (for U80) input signals provided on pin-9 to each device. When the enable pin is LOW, the transceiver device is enabled to perform an operation as defined by the T/R (transmit/receive) input on pin-11. When the enable pin is HIGH, the transceiver devices are held in a high impedance state; all I/O lines from the devices are disabled. The pin-11 input to each transceiver device controls the direction in which the device passes data. When pin-11 (T/R) is LOW, the transceiver devices are enabled to receive data from the Multibus interface. When pin-11 (T/R) is HIGH, the transceiver devices are enabled to transmit data onto the Multibus structure.

The RAM board is designed to operate in any of three types of data transfer mode; even byte transfer, odd byte transfer, or 16-bit transfer.

4-18. EVEN BYTE TRANSFER OPERATION.

An even byte transfer is required when a byte of data is read from or written into an even memory location. To initiate an even byte transfer, the RAM board must receive ADR0/=1 (ADR0 is always false for an even byte) and BHEN/=1 from the Multibus interface (for 8-bit operations, BHEN/ is always false).

In performing an even byte READ or WRITE operation, the RAM board uses the low order data buffer (U81 on 5ZD5) to transfer the even data byte via Multibus data lines DAT0/ through DAT7/.

Table 4-2. Data Transfer Modes

RAM BOARD	MULTIBUS	BHEN/	ADR0/	USES
LOW, EVEN BYTES ← DAT0/DAT7/ HIGH, ODD BYTES — DAT8/ -DATF/		H	H	8 BIT LOW BYTE
LOW, EVEN BYTES — DAT0/ -DAT7/ HIGH, ODD BYTES ← DAT8/ - DATF/		H	L	8 BIT HIGH BYTE (SWAP BYTE)
LOW, EVEN BYTES ← DAT0/ - DAT7/ HIGH, ODD BYTES ← DAT8/ - DATF/		L	H	16 BIT

4-19. ODD BYTE TRANSFER OPERATION.
An odd byte transfer is required when a byte of data
is read from or written into an odd memory location.
To initiate an odd byte transfer, the RAM board
must receive ADR0/ = 0 and BHEN/ = 1 from the
Multibus interface. In performing an odd byte
READ operation, the RAM board uses either 1) the
high order dat buffer (U78 on 5ZD5) to transfer the
odd data byte to Multibus data lines DAT8/ through
DATF/ or 2) the swap buffer (U80 on 5ZC5) to trans-
fer the odd data byte to Multibus data lines DAT0/
through DAT7/. In performing an odd byte WRITE
operation, the RAM board uses the swap buffer (U80
on 5ZC5) to transfer the odd data byte from the
Multibus data lines (DAT0/) through DAT7/ when
BHEN/ = 1).

4-20. 16-BIT TRANSFER OPERATION. The
16-bit word transfer is controlled by the ADR0/ and
BHEN/ signals from the Multibus interface. When
BHEN/ is active (LOW) and ADR0/ is inactive
(HIGH), the odd byte of data is transferred from/to
an odd BANK of memory via the DAT8/ through
DATF/ data lines and the even byte of data is
transferred from/to an even BANK of memory via
DAT0/ through DAT7/.

In performing a 16-bit READ operation, the RAM
board uses both 1) the high order data buffer (U78 on
5ZD5) to transfer the odd data byte to Multibus data
lines DAT8/ through DATF/ and 2) the low order
buffer (U81 on 5ZC5) to transfer the even data byte
to Multibus data lines DAT0/ through DAT7/. For a
16-bit WRITE operation, the RAM board uses both 1)
the high order data buffer (U78 on 5ZD5) to transfer
the odd data byte from the Multibus data lines
(DAT8/ through DATF/) into the memory and 2) the
low order buffer (U81 on 5ZC5) to transfer the even
data byte from the Multibus data lines (DAT0/
through DAT7/) into the memory location. Table 4-2
shows the configurations available and the enable
signals generated for board operation with a 16-bit
Multibus interface.

**4-21. TRANSFER ACKNOWLEDGE
OPERATION**

The Transfer Acknowledge (XACK/) signal informs
the bus master that the READ or WRITE command
is completed.

NOTE

It is strongly recommended that the Ad-
vanced Acknowledge signal (AACK/) no
longer be used in lieu of its slower counter-
part, the XACK/ signal. The AACK/ signal
is no longer supported as a standard Multi-
bus interface signal on the P1 Connector.

During a command cycle, the lack of an inhibit from
the Multibus interface (INH1/=1) coincident with the
decode of a command and the generation of CAS/
during command execution enables U25 pin-11 to
output a LOW into the Delay Timer (U40). The
falling edge of the input generates a rippled output
from U40, one of which is enabled via jumpers to
become the XACK/ signal from the RAM boards.

The delay timer (U40 on 4ZB4) provides 9 trigger
pulses at timed intervals for use in generating the
XACK/ signal. When the input signal is held HIGH,
the pin-3 output activates 25 nanoseconds later and
stays HIGH. As long as the input remains HIGH, a
sequence of rising edge signals is output from U40 at
25 nanosecond intervals. Then, if the input remains
HIGH for 250 nanoseconds, the pin-13 output goes
HIGH and at that point, all outputs from U40 are
HIGH. When the input returns to the inactive state,
the outputs will follow at a 25 nanosecond interval in
the sequence in which they were activated.

The XACK/ signal is jumper selectable to occur
between 100 and 250 nanoseconds after the CAS/
signal from the Dynamic RAM Controller. The
required trigger pulse is connected to the XACK/
line via the jumpers E58 through E65. The connected
clock pulse determines the time at which the XACK/
signal is generated in relation to: (1) the issuance of
a command to the RAM board from the bus master
and (2) the length of time that data is available on
the Multibus interface during a READ operation.

The XACK/ signal is deactivated shortly after the
command is removed from one Multibus interface.
As the bus command is removed, the flipflop U3
resets to generate a HIGH into pin-2 of U40 the
Delay Timer. The trailing edge of the Multibus
command disable the XACK signal.

4-22. INHIBIT OPERATION

The inhibit signal from the Multibus interface
(INH1/) essentially disconnects an iSBC 016A/
032A/064A/028A/056A RAM Board from the system
by disabling the on-board memory buffers, and the
XACK/ signal from operating. Consequently, a
higher priority device that is asserting INH1/ will
function normally and a lower priority device will
not respond to bus commands.

There are instances where the latter situation can be
used advantageously. For example, when a PROM
board equipped with a RAM inhibit signal (such as
the iSBC 416 PROM board) is assigned to occupy
part or all of the system memory space assigned to
the iSBC 016A/032A/064A/028A/056A RAM Boards
and is installed into the system, the PROM board
can provide maintenance functions without memory

or jumper alterations. Then, on completion of a maintenance function, the removal of the PROM board from the system restores the function of the iSBC 016A/032A/064A/028A/056A RAM Boards to their original state.

The inhibit line from the Multibus interface (INH1/) is generated whenever the bus master issues a RAM address during a RED operation for which two separate memory devices in the system could respond. In such a case, the higher priority memory device generates the XACK/ signal and an inhibit signal (INH1/ = 0) that disables the lower priority memory devices from generating the same signals. The inhibit signal is functional during a READ or WRITE operation. The iSBC 016A/032A/064A/028A/056A RAM Boards do not drive the INH1/ line on the Multibus interface; they merely sense the condition of the line as generated by another interface memory device.

When a Multibus command is received by the RAM board, the INH1/ signal from the higher priority memory device disables the execution of the command by the on-board logic. The INH1/ signal is inverted through gate U54 (4ZB7) on the RAM board. When active, the INH1/ signal from the Multibus interface generates a LOW from U38 pin-4 (4ZB7) to disable generation of the write enable signals W0/ and W1/ (4ZC3). The INH1/ signal also disables output from U25 pin-11 (4ZB6), thereby disabling generation of the AACK/ and XACK/ signals to the Multibus interface. The timing for the inhibited READ operation is shown in figure 4-3.

4-23. MEMORY PROTECT OPERATION

The optional memory protection feature for the iSBC 016A/032A/064A/028A/056A RAM Boards makes it possible for the user to prevent the boards from responding to a READ or WRITE command from the Multibus interface. The memory protection feature is activated by the system bus master when the MPRO/ signal on the Multibus interface is held LOW. The MPRO/ signal from the Multibus interface is inverted by U43 (2ZB5) to generate the signal PCS/ input to the Dynamic RAM Controller. When HIGH, PCS/ causes the Dynamic RAM Controller to disregard a subsequent READ or WRITE command request on pin-32. If MPRO/ from the bus master goes LOW while a memory cycle is in progress on the RAM board, the Dynamic RAM Controller finishes the cycle in progress before being disabled by the bus master.

4-24. PARITY CIRCUITRY OPERATION

The parity circuitry on the RAM boards consists of Parity Storage RAMs (U10, U27, U44, and U61; one for the high byte and one for the low byte of each BANK of memory), two parity generator/checker devices (U83 and U84; one for each byte), a four bit Parity Flag Register (U8), an Error Test Latch (U41 pin-6), an Error Interrupt Request Latch (U41 pin-8), and several logic gates (U5, U23, U54, and U60). These components operate together to ensure that each byte of data read from or written into the RAM array conforms to the even parity requirements of the RAM boards.

PARITY GENERATION ON DATA WRITE. When a byte of data is written to the RAM array, the Parity Generator/Checker senses the data (via DI0 through DIF from the Multibus interface) and generates an even parity bit for each byte of data. The parity bits (PI0 and PI1) are then provided as input data to the Parity Storage RAMs in the memory array (U10, U27, U44, and U61 on schematic sheet 3). Each byte of data written into the RAM includes a parity bit that is stored in the parity RAM chips. Notice that the output from U23 pin-3 and pin-11 is used on the READ operation to sense and report a parity error. During a WRITE operation, parity bits are gated through U23 pin-3 and pin-11, however, the parity error reporting circuitry (U41 and U8) is disabled from recording the error and requesting an interrupt by the LOW output from U60 pin-8 (5ZB7).

PARITY CHECKING ON DATA READ. A READ from the RAM array provides the stored parity bit as an input with the data byte into the Parity Generator/ Checker devices (U83 and U84 on 5ZC7). The combination of the data byte and the even parity bit from the Parity Storage RAMs should always generate a LOW from pin-5 of U83 and U84, the Parity Generator/Checker devices. The outputs from U83 and U84 are then input to an "XOR" gate (U23 on 5ZC4) that compares the generated parity bit with a one (selecting even parity) from flipflop U41. A parity error is indicated when the output of either half of U23 is HIGH (the pin-11 output provides an indicator for the byte from memory BANK 0 and the pin-3 output is for memory BANK 1).

PARITY ERROR DETECTING AND RECORDING. Parity errors are detected only during a READ operation. Data is READ from the memory array by words and is output onto an internal bus by bytes; each byte is accompanied by an even parity bit. The parity bits for the low byte and high byte are input to U5 pin-1 and pin-10 (5ZB4), and controlled by the byte enable terms (LBEN and HBEN) placed onto input pin-9 and pin-13 of U5. When one or the other of the data bytes is enabled to the Multibus interface (i.e., either LBEN or HBEN is HIGH), the parity bit is sensed through U5 (LOW on pin-8 indicates that a

parity error is sensed on the data byte; HIGH on pin-8 indicates that no parity error is sensed). When the pin-8 output from U5 is LOW, flipflop U41 (5ZB3) resets, generating a HIGH from U41 pin-8 to perform three functions for the parity logic: 1) the Parity Flag Register is clocked to save the location of the parity error (including the memory BANK and ROW), 2) the interrupt request (INTR5/=0) is generated from U37 pin-10, and 3) the error is shown visually via U37 pin-12 output to the Parity Error LED

Once a parity error is detected and indicated, U41 remains reset (effectively, holding the error) until either a power-on reset is sensed, an I/O READ is issued to the RAM board from the bus master (retrieving the Parity Flag Register contents), or an I/O WRITE operation is issued to the RAM board to change from an even to odd parity check. If a parity error should occur on both bytes of a 16-bit READ operation, the first byte enabled to the Multibus interface is the one for which a parity error is indicated. The second error is lost.

ERROR RETRIEVING. When a parity error is sensed and an Interrupt Request is generated, the bus master must issue an I/O READ command to the RAM boards to access the contents of the Parity Flag Register and determine the origin of the error. To perform the access, the bus master activates IORC/, the I/O READ command signal. IORC/ (5ZA8) enables generation of the XACK/ signal and generates a pulse from U39 pin-11 (2ZB3) to enable generation of IOCS/, the signal required to access the Parity Flag Register contents. The IOCS/ signal enables U42 pin-3 (4ZB3) to output a LOW, providing an enable (ENLBF/) to U81 (5ZC5), the output buffer through which the contents of the Parity Flag Register are gated to the Multibus interface. The IORC/ signal holds the output of U4 pin-8 HIGH (5ZA6), thereby generating an output enable to pin-1 of U8 (5ZB3), the Parity Flag Register. The enable places the contents of the register onto DI0 through DI7, which is inverted and output onto the Multibus interface as DAT0/ through DAT7/. At the same time a LOW pulse is generated from U5 pin-6 (5ZB6) that virtually sets U41 (5ZB3), the Interrupt Request flipflop, and deactivates the Interrupt Request signal on the Multibus interface. As the Interrupt Request is removed, the Parity Error indicator on the RAM boards is extinguished.

NOTE

Notice that the Dynamic RAM Controller is not allowed to operate during a Parity Flag Register read operation.

4-25. PARITY TEST CIRCUITRY OPERATION

Once data (and even parity) is written into memory, the RAM board can be enabled to test for odd parity on each byte read from memory, thereby generating parity errors on any subsequent READ operations. The parity errors generated in this manner can test the parity storage, checking, and generating circuitry.

The entry into a parity test operation is triggered when an I/O WRITE command is issued to the RAM boards to change the parity mask bit. When the bus master issues an I/O WRITE command, it generates the IOWC/ signal on the Multibus interface. The IOWC/ signal from the Multibus interface enables a user to switch the pin-13 and pin-2 inputs to U23 (5ZC4) to a constant LOW; effectively, changing the test performed by U26 from an even parity check to an odd parity check. The IOWC/ command produces an IOCS/ signal (2ZC2), which generates the ENLBF/ signal (4ZC1) to enable the low order I/O data buffer U81 (5ZC5). The IOWC/ signal also generates a HIGH from U4 pin-11 (5ZA6) to clock the flipflop U41 (5ZC3) either set or reset, depending on the condition of the DAT0/ line multiplexed from the Multibus to the flipflop.

To test the parity generation circuitry of the board, the user must program the board into a Parity Test Mode by placing a 1 onto DAT0 on the Multibus interface and performing an I/O WRITE to the address of the Parity Error Flag. In this mode, the RAM board tests for odd parity on data previously written with even parity and thus generates a parity error indication for each READ operation. The board exits from Parity Test Mode either by receiving an initialization signal (INIT/) or by execution of a program that writes a 1 into the parity mask bit.

NOTE

The iSBC 016A RAM Board will not perform the parity test because parity is not available on the board.

The RAM boards can be configured via the Parity Test Circuitry to generate odd parity. This is performed by changing the parity test mask from "1" to "0" before writing data into the RAM chips. The data must be placed onto DAT0 (the Multibus data line) before issuing an I/O WRITE command to the I/O Port address for the Parity Flag Register. Effectively, the RAM board generates and stores even parity, reads data and even parity from memory, and inverts the parity bits through U23 (5ZC4) to provide odd parity outputs on pin-32 and pin-34 of the P2 connector.

4-26. INTERRUPT REQUEST LOGIC

The interrupt request logic is activated only by sensing a parity error. When the interrupt request logic is enabled on the RAM boards, the boards activate one of the Multibus Interrupt Request signals (INTR0/ through INTR7/) to the bus master on detection of a parity error. The interrupt request is generated as a result of the operation of logic devices U5, U37, and U41 (schematic sheet 5).

Once an interrupt request is generated from the RAM boards, the request can be terminated in one of three methods; 1) by generation of the Multibus RESET signal (INIT/ on pin-14 of P1), 2) by performing an I/O READ of the Parity Flag Register contents on the RAM boards, or 3) by performing an I/O WRITE to flipflop U41 used in the test for the parity check.

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, and service and repair assistance instructions for the iSBC 016A/032A/064A/023A/056A RAM Boards.

5-2. SERVICE AND REPAIR ASSISTANCE

United States Customers can obtain service and repair assistance by contacing the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). This number is usually silk-screened onto the board.

c. Serial number of product. This number is usually stamped on the board.

d. Shipping and billing addresses.

e. Purchase order number for billing purposes if your warranty has expired.

f. Information on extended warranty agreements, if applicable.

Use the following telephone numbers for contacting the Intel Product Service Hotline:

All U.S. locations, except Alaska, Arizona & Hawaii:

(800) 528 - 0595

All other locations: (602) 869 - 4600

TWX Number: (910) 951 - 1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH - 240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclosed in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5-3. REPLACEABLE PARTS

Table 5-1 provides a list of replaceable parts for the RAM boards. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column of table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML". Every effort should be made to procure these parts from a local (commercial) distributor.

5-4. SERVICE DIAGRAMS

The parts location diagram and schematic diagram for the RAM boards are provided in figures 5-1, 5-2 and 5-3, respectively. The parts location diagram is useful in locating the parts listed in table 5-1.

The schematic diagram (figure 5-3) consists of six sheets of logic drawings that are current when the manual is printed. However, minor revisions and changes may have occurred since the manual was printed, so Intel provides with each product a current copy of the schematic diagram that should be inserted into this manual. In some instances, the schematic shipped with the product will be identical to that in the manual.

The signals on the schematic diagrams that traverse from one sheet of the drawing to another are labeled with a boxed letter reference (e.g., A or AB) to make the signal tracing operation easier. Each signal is listed with the same boxed letter reference on each sheet of figure 5-3 to which it is routed.

The signal mnemonic and the source/destination sheet number are shown adjacent to the boxed letter reference. Signal mnemonics listed on the left side of a sheet are entering the diagram; signal mnemonics listed on the right side of a sheet are leaving the diagram. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., BHEN/) is active LOW. Conversely, a signal mnemonic without the slash (e.g., ADR0) is active HIGH.

Table 5-1. Replaceable Parts

Reference Designator	Mfr. Description	Mfr. Part No.	Code	Qty
U28-U35, U62-U69	IC, 2110 Dynamic RAM iSBC 016A RAM Board	2110-4A0L	Intel	16
U28-U35, U62-U69	IC, 2110 Dynamic RAM iSBC 016A RAM Board	2110-4A0H	Intel	16
U11-U18, U28-U35, U45-U52, U62-U69	IC, 2110 Dynamic RAM iSBC 032A RAM Board	2110-4A0L	Intel	36
U11-U18, U28-U35, U45-U52, U62-U69	IC, 2110 Dynamic RAM* iSBC 032A RAM Board	2110-4A0H	Intel	36
U11-U18, U28-U35, U45-U52, U62-U69	IC, 2118 Dynamic RAM iSBC 064A RAM Board	2118-4	Intel	36
U10-U18, U27-U35, U44-U52, U61 U69	IC, 2132 Dynamic RAM iSBC 028A RAM Board	2132A-20T	Intel	36
U10-U18, U27-U35, U44-U52, U61 U69	IC, 2132 Dynamic RAM iSBC 028A RAM Board	2132A-20B	Intel	36
U10-U18, U27-U35, U44-U52, U61 U69	IC, 2132 Dynamic RAM iSBC 028A RAM Board	2132A-20L	Intel	36
U10-U18, U27-U35, U44-U52, U61 U69	IC, 2132 Dynamic RAM iSBC 028A RAM Board	2132A-20R	Intel	36
U10-U18, U27-U35, U44-U52, U61 U69	IC, 2164 Dynamic RAM iSBC 056A RAM Board	2164A-25	Intel	36
U78,U80,U81	IC, 8286 Octal Transceiver	8286	Intel	3
U1	IC, Serial Shift Register	74LS164	TI	1
U2, U24	IC, Quad 2 input Positive-OR gate	74S32	TI	2
U3,U21,U41	IC, Dual D-type Flipflop	74S74	TI	3
U4,U6 U39,U42	IC, Quad 2 input Positive-NAND gate	74S00	TI	4
U5	IC, Dual AND-OR-Invert gate	74S51	TI	1
U38	IC, Quad 2-input Positive-NOR gate	74S02	TI	1
U8	IC, 4-bit D-Type Register	747LS173	TI	1
U9	IC, Quad 2-to-1 Data Multiplexer	74S158	TI	1
U20,U22,U43	IC, Hex Inverters	74S04	TI	3
U23	IC, Quad 2-input XOR gates	74S86	TI	1
U25	IC, Quad 2-input Positive-NAND gates	74S37	TI	1
U37	IC, Hex Inverters, Open Collector	7405	TI	1
U54,U76, U77,U87	IC, Octal 3-state buffers	74S240	TI	4
U55	IC, 4-input AND-OR-Invert gate	74S260	TI	1
U56,U73	IC, 4-bit Binary Full Adder	74S283	TI	2
U57	IC, Triple 3-input Positive-NAND gates	74S10	TI	1
U58	IC, 4-input AND-OR-Invert gate	74LS260	TI	1
U59,U86	IC, 4-bit Magnitude Comparator	74S85	TI	2
U60	IC, Quad 2-input Positive-AND gate	74S08	TI	1
U71,U72,U74	IC, Octal 3-state buffers	74LS240	TI	3
U79,U82	IC, Octal D-Type Latches	74S373	TI	2
U83,U84	IC, Odd/even Parity Generator/Checker	74S280	TI	2
R1,R2,R4, R8,R10-13, R29,R30	Resistor, 1K ohm,1/4 W,5%	OBD	COML	10
R6,R7	Resistor, 330 ohm,1/4W,5%	OBD	COML	2
R27	Resistor, 180 ohm,1/4W,5%	OBD	COML	1
R26	Resistor, 360 ohm,1/4W,5%	OBD	COML	1
RP1,RP3-RP6	Resistor pack, 1K ohm, 8-pin	4308R-101-102	BOU	5
RP7-RP9	Resistor pack, 1K ohm, 10-pin	4310R-101-102	BOU	3
R5,R14-16,R18 R19,R20-23	Resistor, 39 ohm,1/4W,5%	OBD	COML	10
R17,R20, R24,R29	Resistor, 22 ohm,1/4W,5%	OBD	COML	4

Table 5-1. Replaceable Parts (Continued)

Reference Designator	Mfr. Description	Mfr. Part No.	Code	Qty
C1,C3-6,C9-17 C19,C21-43, C45-57,C59-62, C65,C66,C71	Capacitor, .01F,50V,+80 -20%	OBD	COML	1
C58,C63,C64	Capacitor, 47F,10V,10%	OBD	COML	5
C8	Capacitor, 200pF,10V,5%	OBD	COML	1
C18	Capacitor, 10pF,100V,5%	OBD	COML	1
C2	Capacitor, .001F,100V,5%	OBD	COML	1
C44	Capacitor, 270pF,100V,5%	OBD	COML	1
C7	Capacitor, .01F,50V,+80 -20%	OBD	COML	1
XJ2	Socket, 20-pin	520-AG11D	AUG	1
XU79,XU82	Socket, 20-pin	520-AG11D	AUG	2
XU10,XU27, XU44,XU61	Socket, 16-pin	516-AG11D	AUG	4
U40	Delay Line, 250 nanosecond	PE9825-002	PUL	1
Y1	Crystal, 12.000 MHz	CY12B	CCI	1
DS1	Light Emitting Diode, red	550-2406	DLC	1
E1-5,E26-28, E31-38,E51-56 E76-90,E103-114 E123-132,E139-145	Wirewrap posts, interconnect	87623-1	AMP	78
	Shorting Plug	8136-475G1	AUG	22
	Receptacle, 2-pin	530153-2	AMP	2
	Terminal Turret	2010B	USC	3

Note:
* marks the components that are not present on the iSBC 016A RAM Board when configured as shipped.

Table 5-2. Manufacturer Codes

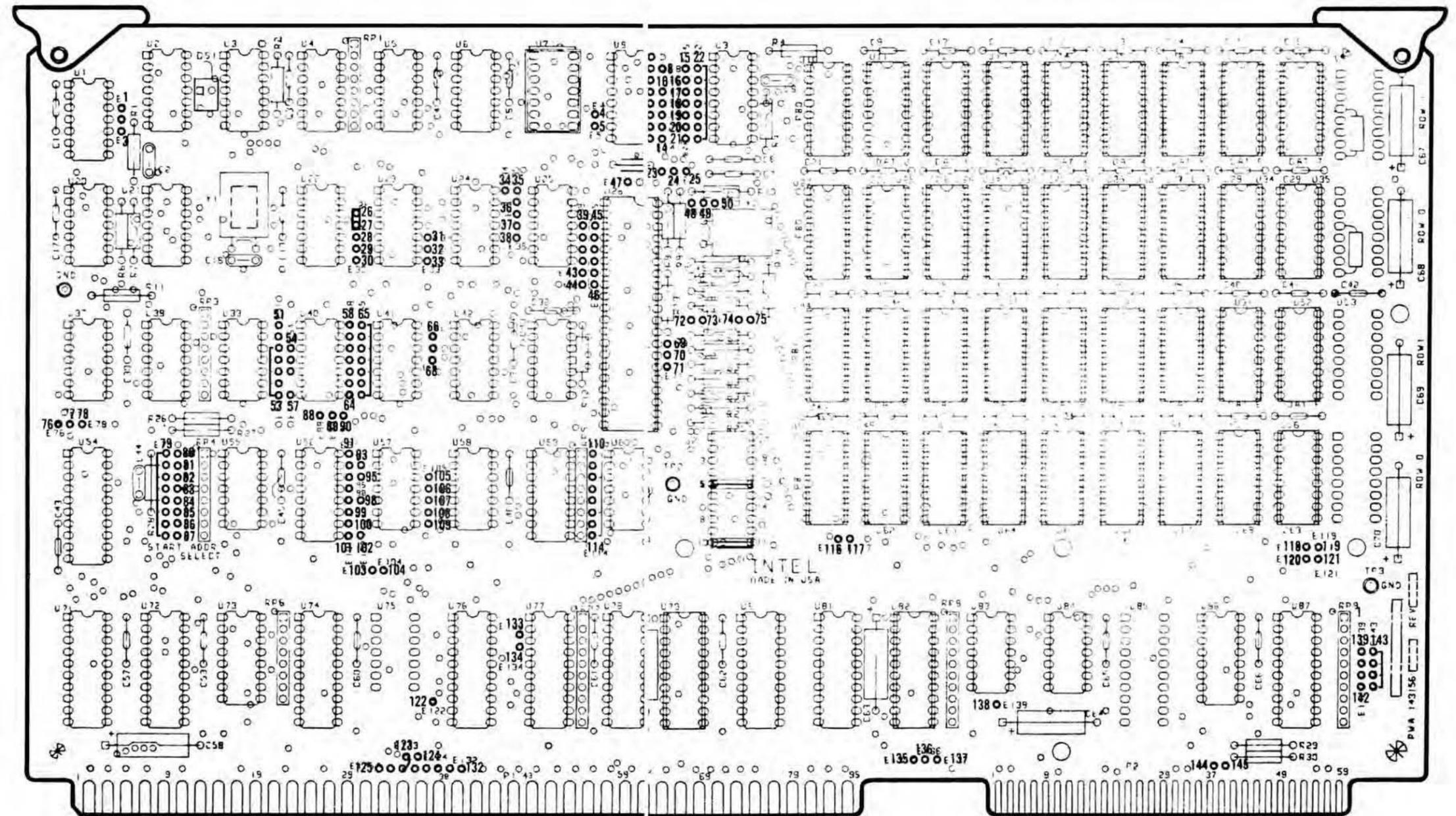| Mfr. Code	Manufacturer	Address
AMP	AMP, Inc.	Harrisburg, PA
AUG	Augat, Inc.	Attelboro, MA
BOU	Bourns	Riverside, CA
CCI	Crystek Crystals, Inc.	Ft. Myers, FL
DLC	Dialight Corp.	Brooklyn, NY
INTEL	Intel Corp.	Santa Clara, CA
PUL	Pulse Engineering, Inc.	San Diego, CA
TI	Texas Instruments, Inc.	Dallas, TX
USC	Useco	Van Nuys, CA
OBD	Order by description, any commercial (COML) source	

Figure 5-1. Jumper Location Diagram

Figure 5-2. iSBC 016A/032A/064A/028A/056A™ RAM Boards Parts Location Diagram

Figure 5-3. iSBC 016A/032A/064A/028A/056A™ RAM Boards Schematic Diagram (Sheet 1 of 5)

RAM Board Jumpers	Grid Location	Function
E139 through E143	2-C7	Selects Megabyte Page Address.
E79 through E87	2-C5	Selects Starting 4k Boundary Address.
E110 through E114, E103 through E109, and E76 through E78	2-B5	Selects I/O Port Address

Figure 5-3. iSBC 016A/032A/064A/028A/056A™ RAM Boards Schematic Diagram (Sheet 2 of 5)
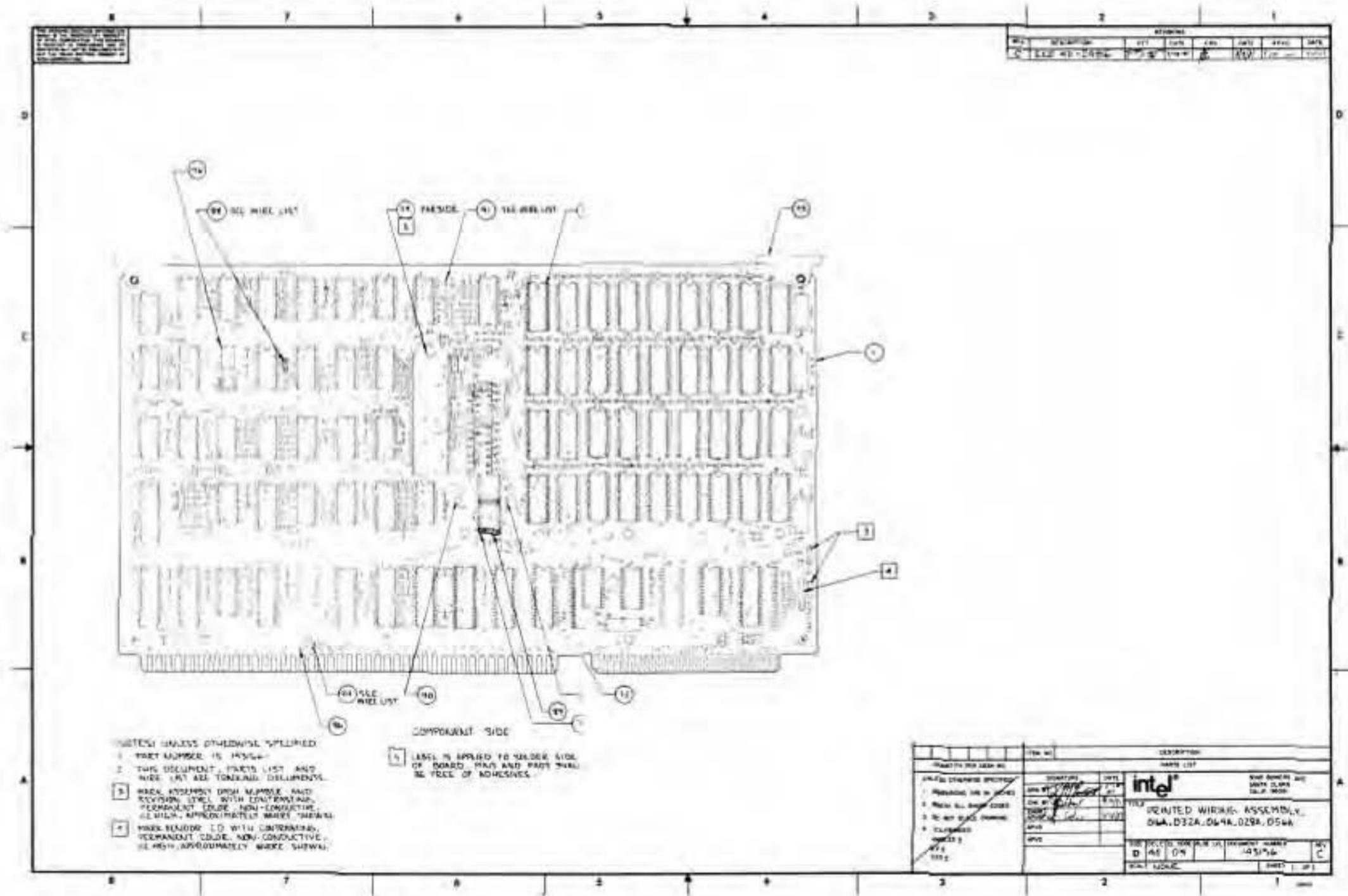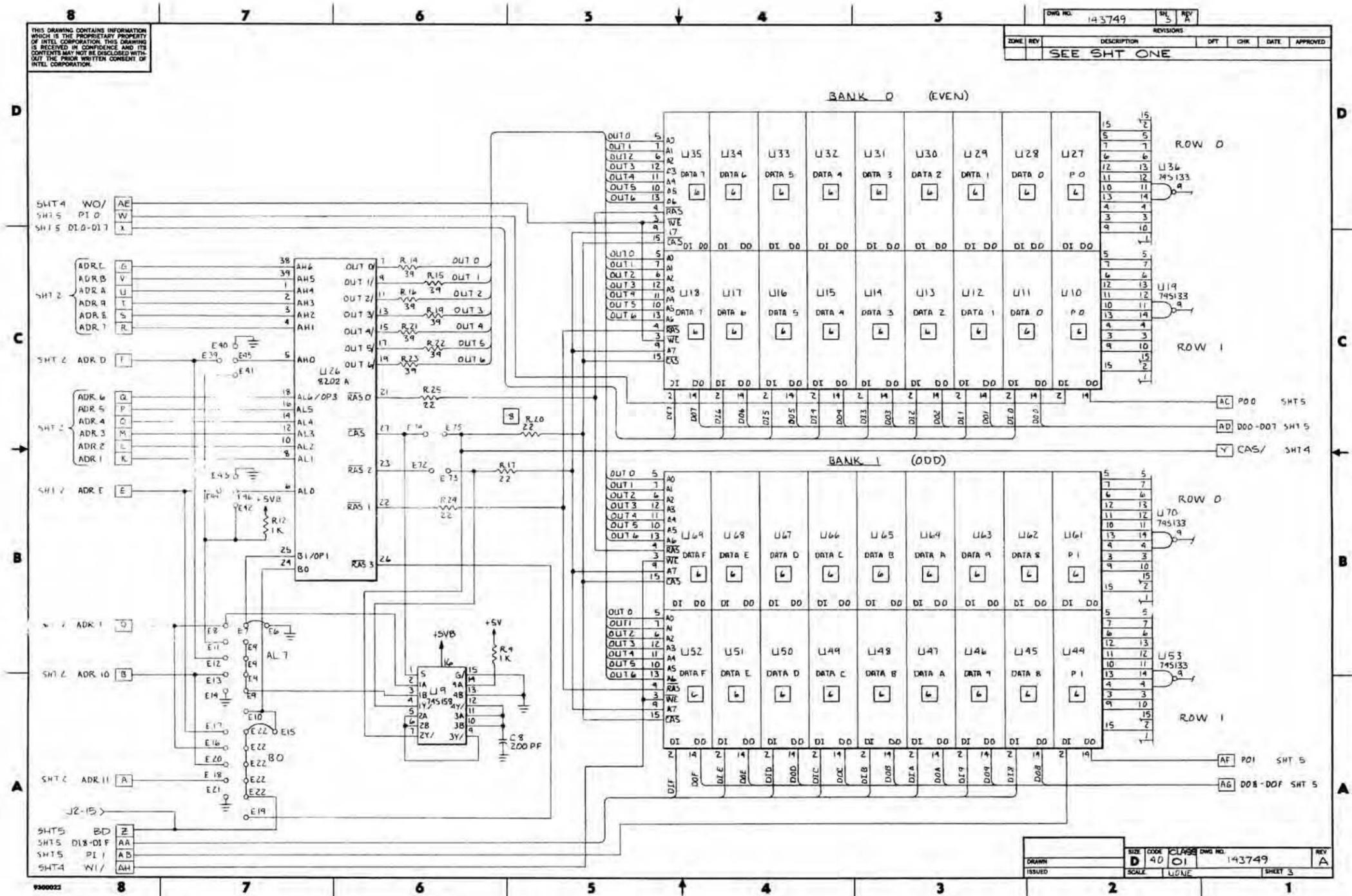
Figure 5-3. iSBC 016A/032A/064A/028A/056A™ RAM Boards Schematic Diagram (Sheet 3 of 5)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

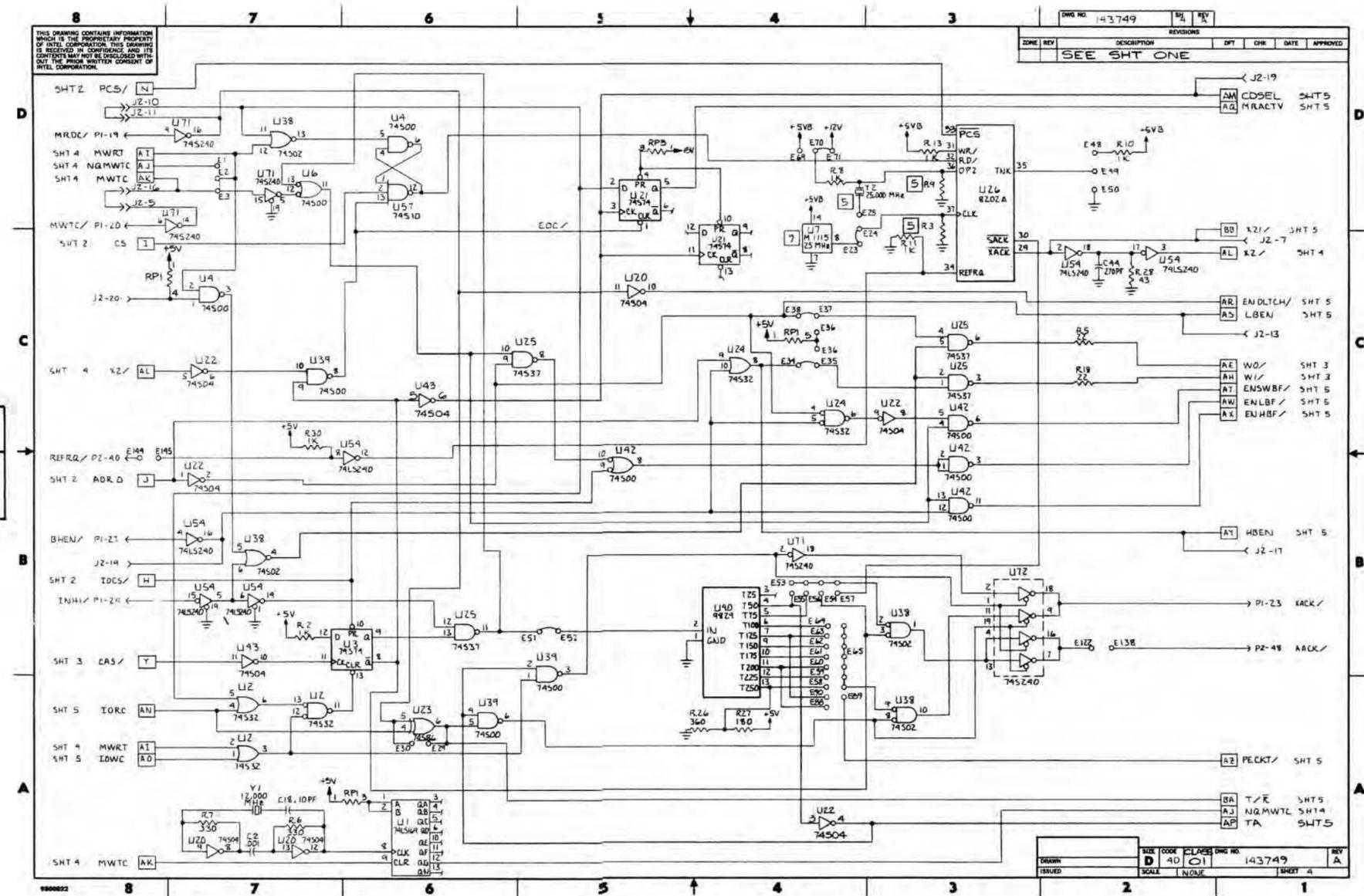| RAM Board Jumpers	Grid Location	Function
E2-E3	4-D7	Selects Advanced Write Mode.
E1-E2	4-D7	Selects Advanced Write Mode
E144-E145	4-8C	Enables External Refresh Timing

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-3. iSBC 016A/032A/064A/028A/056A™ RAM Boards Schematic Diagram (Sheet 4 of 5)

RAM Board Jumpers	Grid Location	Function
E26-E27	5-C3	Enables Internal Parity Generation for Bank 1.
E27-E28	5-C3	Enables External Parity Generation for Bank 1.
E31-E32	5-C3	Enables Internal Parity Generation for Bank 0.
E32-E33	5-C3	Enables External Parity Generation for Bank 0.
E123 through E132	5-B1	Selects Interrupt Request Level.
E4-E5	5-B2	Enables Parity Flag Register Output.

Figure 5-3. iSBC 016A/032A/064A/028A/056A™ RAM Boards Schematic Diagram (Sheet 5 of 5)