iSBC® 286/10A
SINGLE BOARD COMPUTER
HARDWARE REFERENCE MANUAL

Order Number: 147532-001

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INTENDED AUDIENCE AND PURPOSE

This manual provides sufficient information for a user to successfully

- Configure the jumpers and interfaces on the board for a specific application.
- Install the board into a standard MULTIBUS system environment.
- Program the board for operation in its system environment.

This manual is written for software and hardware engineers and requires a medium to high level of technical expertise in both the software and hardware operation of the iAPX 286 CPU chip and its family of peripheral support chips.

RELATED PUBLICATIONS

To avoid redundancy, this manual references technical information contained in these technical publications:

- iAPX 286 Hardware Reference Manual, Order Number: 21Ø76Ø.
- iAPX 286 Programmer's Reference Manual, Order Number: 21Ø498.
- Intel Microsystem Components Handbook, Order Number: 23Ø843.
- Intel Memory Components Handbook, Order Number: 21Ø83Ø.
- Intel MULTIBUS® Specification, Order Number: 98ØØ683.
- Intel iLBX™ Bus Specification, Order Number: 145695.
- Intel iSBX™ Bus Specification, Order Number: 142686.
- EIA Standard for RS232C Interfacing, EIA-RS-232C.
- EIA Standard for RS422A Interfacing, EIA-RS-422A.
- EIA Standard for RS449 Interfacing, EIA-RS-499.

Other Intel publications you may find helpful are

- Introduction to the iAPX 286, Order Number: 21Ø3Ø8.
- Intel iAPX 286 Data Sheet, Order Number: 21Ø253.
- Intel Application Note AP-134, Asynchronous Communications with the 8274 Multiple Protocol Serial Controller.
- Intel Application Note AP-145, Synchronous Communications with the 8274 Multiple Protocol Serial Controller.
- iSBC® Ø12EX/Ø1ØEX/Ø2ØEX/Ø4ØEX RAM Boards Hardware Reference Manual, Order Number: 147783.

The previous and other Intel publications are listed in Intel's Literature Guide, Order Number: 21Ø621. See page ii for the ordering address.

NOTATIONAL CONVENTIONS

This manual uses two special characters, the asterisk (*) and the section symbol (§):

- * Used after a signal mnemonic to indicate that the signal is active-low. Signal mnemonics without a trailing asterisk are active-high. The asterisk replaces the slash (/) previously used to indicate the active state of a signal; the slash is still used on the schematic diagrams.

- § Used after a jumper connection to indicate a factory-installed jumper (default configuration).

You will encounter **NOTES**, **CAUTIONS**, and **WARNINGS** throughout this manual. Notes emphasize information for special consideration. Cautions indicate possible errors that could result in software or hardware damage. Most importantly, warnings indicate there is a possibility of personal injury.

ORGANIZATION OF THIS MANUAL

This section provides a short abstract of each chapter.

CHAPTER 1. GENERAL INFORMATION

This chapter provides a brief overview of the features of the iAPX 286 CPU and the iSBC 286/10A Single Board Computer. The chapter also contains the specifications that the user needs to use the board in a system.

CHAPTER 2. BOARD OPERATION

This chapter provides a functional description based on the board's block diagram. The chapter also supplies the default configuration of each block.

CHAPTER 3. INSTALLATION

This chapter supplies information to help you prepare for board installation and provides a preview of user-supplied components/equipment that may be needed. The board's operating requirements are also supplied.

CHAPTER 4. CONFIGURATION

This chapter contains jumper, addressing, interface, and programming information for configuring each function on the board.

CHAPTER 5. SERVICE INFORMATION

This chapter provides service and repair assistance instructions and schematic diagrams for the board.

APPENDIX A. JUMPER INFORMATION

This appendix consolidates all the jumper information and can be used as a quick reference. The appendix shows the jumper locations, explains jumper functions, and provides a jumper index for the schematic.

APPENDIX B. MULTIDROP CONSIDERATIONS

This appendix provides a functional multidrop example, which includes calculations for determining bias and terminator resistor values.

APPENDIX C. PAL EQUATIONS

This appendix supplies the pin-out description and equations for PAL U74 and a summary of the primary decode memory maps that define local and iLBX memory.

APPENDIX D. WAIT-STATE REQUIREMENTS

This appendix provides information on wait-state requirements for local and dual-port memory.

APPENDIX E. MEMORY SOCKET MATRIX CONFIGURATIONS

This appendix provides information for configuring the local and dual-port memory socket's matrices for different device sizes and types.

APPENDIX F. iSBC® 341 MEMORY BOARD INSTALLATION

This appendix provides information for installing the iSBC 341 memory board for four more local or dual-port sockets.

APPENDIX G. I/O PORT ADDRESS LIST

This appendix consolidates all the I/O addresses and can be used as a quick reference.

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FIGURES (continued)

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1.1 INTRODUCTION

The iSBC® 286/1ØA Single Board Computer (Figure 1-1) is a board-level solution for high-speed, multiuser, multitasking, real-time, multiprocessor system applications.

This manual provides all information necessary to use the iSBC 286/1ØA board. This chapter provides a brief overview of the features and the specifications of the iSBC 286/1ØA processor board.

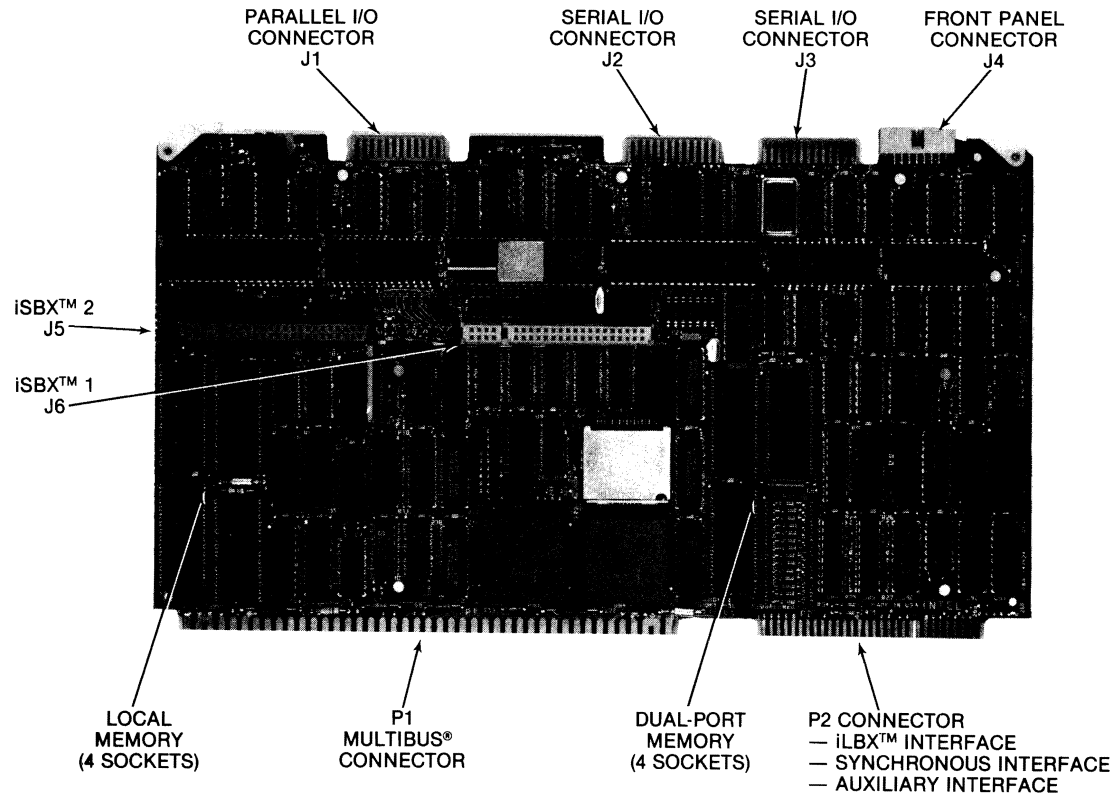

Figure 1-1. iSBC® 286/1ØA Single Board Computer

The board contains the standard MULTIBUS® connector (P1), an iLBX™ Bus connector (P2), and three I/O edge connectors (J1, J2, and J3). Connector J4 provides the signals for operating a system front panel, and connectors J5 and J6 provide two iSBX™ bus interfaces.

1.2 iAPX 286 CPU FEATURES

The design of the iAPX 286 CPU provides the iSBC 286/1ØA board with several features:

- Two modes of operation: Protected Virtual Address Mode (PVAM) and Real Address Mode
- Concurrent instruction decoding within the CPU
- Bus cycle pipelining on the local bus
- Extended iAPX 86, 88 instruction set
- Large address space –

PVAM	Real Mode
16 megabytes physical 1 gigabyte virtual	1 megabyte

- Four levels of process protection (PVAM)
- Automatic memory access verification (PVAM)

For detailed information, refer to Intel's iAPX 286 PROGRAMMER'S REFERENCE MANUAL.

1.3 BOARD FEATURES

In addition to the iAPX 286 features, the iSBC 286/1ØA board contains several other features:

- An iLBX (Local Bus Extension) interface for high-speed memory expansion
- A synchronous interface for high-speed memory expansion
- A front panel interface
- 8 JEDEC sockets for optional memory components
  4 sockets for local memory (expandable to 8)
  4 sockets for dual-port memory (expandable to 8)
- Configurable memory capacity - up to 128K bytes of dual-port
  - up to 256K bytes of local
- Two programmable serial I/O interfaces
- Accepts the 8Ø287 Numeric Processor Extension
- Two 8- or 16-bit iSBX bus interface connectors for I/O expansion
- Centronics-compatible parallel I/O printer interface
- 15 levels of vectored interrupt control

Refer to Chapter 2 for a general description of these features and Chapter 4 for configuring and programming information.

1.4 BOARD SPECIFICATIONS

Table 1-1 contains the specifications for the iSBC 286/1ØA board.

Table 1-1. Specifications

CPU	Intel iAPX 286 CPU
WORD SIZE	
Instruction:	8, 16, 24, 32, 4Ø, or 48 bits
Data:	8 to 8Ø bits
Physical Addressing:	2Ø bits (1 Mbyte) - Real Address mode 24 bits (16 Mbyte) - PVAM
Virtual Addressing:	1 gigabyte - PVAM
SYSTEM CLOCK SPEED:	or 4.9 MHz 8.Ø MHz (default)
INSTRUCTION EXECUTION TIME	375 nsec 25Ø nsec, instruction in queue
MEMORY	
On-board Memory:	Eight 28-pin JEDEC-compatible chip sockets hold user-provided memory devices in 2Kx8, 8Kx8, 16Kx8, 32Kx8, or 64Kx8 capacity. Four sockets are dedicated to dual-port memory; four sockets are dedicated to local memory. The iSBC 341 memory expansion board adds four sockets to both local and dual-port memory.
MAXIMUM LOCAL MEMORY	256K bytes (maximum in 4 or 8 sockets)
MAXIMUM DUAL-PORT MEMORY	128K bytes (maximum in 4 or 8 sockets)
PHYSICAL CHARACTERISTICS	
Width:	3Ø.48 cm (12.ØØ in)
Height:	17.15 cm (6.75 in)
Depth:	1.42 cm (Ø.56 in) with no MULTIMODULE boards 1.82 cm (Ø.718 in) with iSBC 341 MULTIMODULE board 2.95 cm (1.16 inches) with an iSBX MULTIMODULE board
Weight:	534 gm (19 oz)

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Table 1-1. Specifications (continued)

ENVIRONMENTAL REQUIREMENTS	
Operating Temperature:	Ø°C to 55°C
Relative Humidity:	to 9Ø%, noncondensing
Air Velocity:	2ØØ linear feet/minute minimum
INTERFACE COMPLIANCE LEVELS:	
MULTIBUS® Compliance:	Master D16 M24 I16 VØ2 E L
iSBX™ Bus Compliance:	D16/16 I
iLBX™ Bus Compliance:	PM D16 A24
I/O CAPABILITY	
Parallel:	24 programmable I/O lines using one 8255A PPI device; 18 of the lines are configurable. Default configured for on-board functions and direct operation with a printer using the Centronics interface standard.
Serial:	2 serial interfaces using the 8274 MPSC device. Connector J2 is configurable for either RS232C or RS422A/449 operation; Connector J3 is configured for only RS232C (DCE) operation.
I/O Expansion:	2 iSBX bus connectors providing expansion via addition of 8-bit or 16-bit iSBX MUlTIMODULE boards, in increments as follows: • one single-wide MULTIMODULE board, or • two single-wide MULTIMODULE boards, or • one double-wide MULTIMODULE board, or • one single- and one double-wide MULTIMODULE board
SERIAL COMMUNICATIONS CHARACTERISTICS	Supports the following modes of the 8274 MPSC:
Protocols:	Bit-synchronous Byte-synchronous Asynchronous
Synchronous:	5- to 8-bit characters; internal character or HDLC/SDLC synchronization; automatic sync bit insertion, even or odd parity.
Asynchronous:	5- to 8-bit characters; break character generation; 1, 1-1/2, or 2 stop bits; false start-bit detection, even or odd parity.

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Table 1-1. Specifications (continued)

8274 Baud Rates:

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)				
	Synchronous	Asynchronous			
Reference: 1.23 MHz	÷1	÷1	÷16	÷32	÷64
615.	615,000	615,000	38,400	19,200	9,600
307.	307,000	307,000	19,200	9,600	4,800
154.	154,000	154,000	9,600	4,800	2,400
76.8	76,800	76,800	4,800	2,400	1,200
38.4	38,400	38,400	2,400	1,200	600
19.2	19,200	19,200	1,200	600	300
9.6	9,600	9,600	600	300	150
4.8	4,800	4,800	300	150	75
2.4	2,400	2,400	150	75	—
1.2	1,200	1,200	75	—	—
0.6	600	600	—	—	—

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ELECTRICAL CHARACTERISTICS

DC Power Requirements:

Supply Voltage	Current Required (typical)	(max.)
+5V ±5%	5.6 A	7.1 A
+12V ±5% (note 1)	5Ø mA	5Ø mA
-12V ±5% (note 1)	5Ø mA	5Ø mA

Notes:
1. ±12 volts is required for RS232C interface.
2. Values do not include power for memory devices or iSBX MULTIMODULE boards. If you add either, add their power requirements to the data in this table.

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Table 1-1. Specifications (continued)

VISUAL INDICATORS	
2 Red LEDs	User-programmable after the 8255 PPI is initialized. On after a reset.
1 Yellow LED	Time-out indicator. On when no acknowledge signal is found after an iLBX, synchronous, or MULTIBUS access has been requested. Turned off by program control.
1 Green LED	On when a cycle is in progress (between ALE and READY).

***

2.1 INTRODUCTION

This chapter provides an overview of the operation of the board and of the functional devices. Each functional area of the board is shown in the block diagram and its default configuration will be explained. Refer to Chapter 4 for more detailed information.

2.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the iSBC 286/10A board is shown in Figure 2-1. The following sections describe each of the functional units of the block diagram.

2.2.1 CLOCK GENERATION CIRCUITS

The iSBC 286/10A board contains three clock generator devices, the 82284, 8284A, and G1. These devices operate independently and provide these jumper-selectable clock rate options:

1. Operate the 80286 CPU at 4.9 MHz or 8 MHz (default).
2. Operate the 80287 synchronously with the 80286 CPU:
   - 80287 at 3.28 MHz with 80286 CPU at 4.9 MHz.
   - 80287 at 5.33 MHz with 80286 CPU at 8.0 MHz (default).

   Operate the 80287 asynchronously with the 80286 CPU:
   - 80287 at 8.0 MHz independent of 80286 clock.

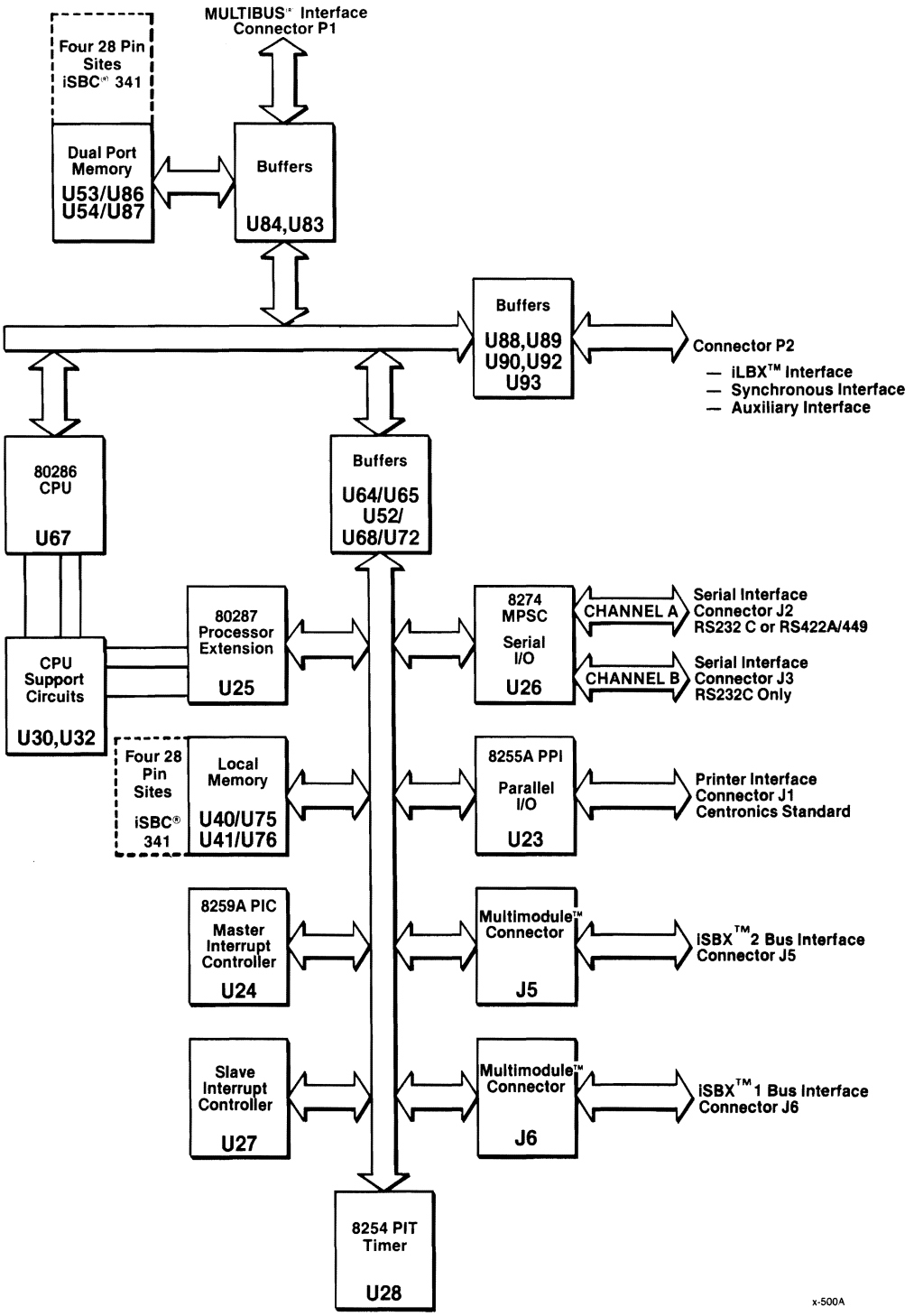


Figure 2-1. Block Diagram

2.2.2 CENTRAL PROCESSOR

The 8Ø286 CPU operates in one of two modes: Real Address mode or Protected Virtual Address Mode (PVAM). The CPU automatically operates in Real Address mode after power-up or reset. Issuing one software command, which changes the contents of the Machine Status Word Register, switches the 8Ø286 CPU from Real Address mode to PVAM. A word-write to the parallel port switches the iSBC 286/1ØA board from 2Ø-bit to 24-bit addressing.

NOTE

After switching the 8Ø286 CPU from Real Address mode to PVAM, you cannot switch back to Real Address mode without a hardware RESET.

The differences between the two modes are quite significant and are listed in the following sections. For more information, refer to Intel's iAPX 286 PROGRAMMER'S REFERENCE MANUAL.

REAL ADDRESS MODE

- The 8Ø286 executes a superset of the 8Ø86 instruction set.
- The 8Ø286 can access up to one megabyte of address space.
- The 8Ø286 can access up to 64K 8-bit I/O addresses or up to 32K 16-bit I/O addresses.
- The memory protection hardware features of the 8Ø286 are disabled.
- The 8Ø286 begins program execution at memory location FFFFØH in the Real Address mode.

PROTECTED VIRTUAL ADDRESS MODE

- The 8Ø286 executes a superset of the Real Address mode instruction set with additional instructions specifically for use with PVAM.

- The 8Ø286 can access up to 16 megabytes of physical address space and up to one gigabyte of virtual address space.

- The 8Ø286 can access the same number of I/O ports as in Real Address mode.

- The 8Ø286 performs automatic memory access verification. Each memory segment is assigned a Read only, Read/Write, Execute/Read, or Execute access right. On every memory access, the iAPX 286 CPU automatically verifies that the access rights are not being violated.

- The 8Ø286 provides four privilege levels. An error flag indicates when any privilege level restriction is violated. The hardware enforces a strict protection algorithm that

  -- allows tasks to access data in only those segments with an equal or lower privilege level

  -- allows tasks to call only those segments with an equal or higher privilege level

  -- allows only those tasks executing at the highest privilege level to execute instructions that alter the CPU state (for example, the HALT instruction)

In both modes of operation, the 8Ø286 allows space for up to 256 interrupt vectors. Interrupt vectors Ø through 31 are used by internally generated interrupts and are reserved. Vectors 32 through 256 share the hardware interrupt request pin (INTR) and are identified by their interrupt vector during an interrupt acknowledge cycle. All are available through software interrupts.

2.2.3 SERIAL I/O INTERFACES

The serial I/O on the iSBC 286/1ØA board consists of an 8274 Multiple Protocol Serial Controller (MPSC) device controlling two 26-pin connectors, J2 and J3. Channel A of the 8274 MPSC operates the serial interface at Connector J2; Channel B operates Connector J3. Because the two channels are independent, they can operate simultaneously.

In the default configuration, the iSBC 286/1ØA board provides a specific interface standard on each of the serial I/O connectors:

- Connector J2 is configured as an RS232C DCE (Data Communications Equipment) interface via Channel A. Connector J2 may also be altered for RS232C DTE (Data Terminal Equipment) mode or as an RS422/449 (DTE or DCE mode) interface.

- Connector J3 is configured as an RS232C DCE interface via Channel B and cannot be altered.

Depending on how the 8274 MPSC is programmed, the interfaces are in either an interrupt-driven mode or a polled-interrupt mode.

In the default configuration, the 8274 MPSC operates in an interrupt-driven mode; that is, an interrupt request signal (SER INTR) is activated whenever either channel needs service. By activating the SER INTR signal, the 8274 MPSC provides an interrupt acknowledge signal at interrupt level 6 to the master 8259A PIC. With the interrupt request, the 8274 MPSC also provides an 8-bit interrupt vector address on the local data bus.

Connector J2

The iSBC 286/1ØA board provides configuration control on Channel A (Connector J2). In the default configuration, the iSBC 286/1ØA board operates Channel A as an RS232C DCE interface. By altering the DIP header configuration, Channel A is reconfigured as an RS232C DTE interface. By changing the orientation of a socketed resistor pack, adding a socketed IC, and moving a DIP header, Channel A can be reconfigured as an RS422A/449 interface. The interface is also compatible with CCITT X.25, a European serial interfacing standard, when configured as an RS422A/449 interface.

Connector J3

Channel B (Connector J3) is not reconfigurable. Channel B must operate as an RS232C interface in DCE mode.

2.2.4 PARALLEL I/O INTERFACE

The parallel I/O on the iSBC 286/1ØA board consists of an 8255A PPI device controlling J1, the 26-pin parallel I/O port. Chapter 4 supplies detailed information for the interface.

The iSBC 286/1ØA board provides jumpers for configuring the printer interface as interrupt-driven. The interface logic can generate an interrupt request to the on-board 8259A PIC via the LPT ACK/INT signal.

In the default configuration, the iSBC 286/1ØA board provides signals at Connector J1 that are plug-compatible with the Centronics standard interface. The iSBC 286/1ØA board also provides interface drivers and receivers for the printer interface. To use the Centronics printer interface, an initialization routine must initialize the 8255A PPI device for operation in Mode Ø with Port B as input, Port A as output, and Port C as output. The printer interface is complete and ready to use when the iSBC 286/1ØA board is received.

The direction of operation of Port A can be reconfigured. However, undefined board operation may result if Ports B and C are also reconfigured.

2.2.5 ON-BOARD MEMORY

The on-board memory space on the iSBC 286/1ØA board consists of three separate memory areas: local memory one, local memory two, and dual-port memory space. Each area is configurable and independent of the others. The local memory is accessible only to the on-board CPU, while the dual-port memory is accessible by both the on-board CPU and another MULTIBUS board.

Local memory consists of chip sockets U4Ø/U75 (local memory one) and U41/U76 (local memory two). In the default configuration, each local memory socket pair is prepared for immediate installation of 27128 (16Kx8) EPROM devices. You can reconfigure the board to accept a maximum of 256K bytes of memory at the local memory chip sockets. Local memory supports only EPROM devices.

Dual-port memory consists of chip sockets U53/U86 and U54/U87 and will accept immediate installation of four 2Kx8 Static RAM devices. You can reconfigure the dual-port memory to accept a different device type, consuming up to 128K of memory space. The dual-port locations support EPROM, EEPROM (only those with 5V programming signals), Static RAM, and iRAM.

In addition to the socketed memory, both local and dual-port memory can be expanded by installing an iSBC 341 Memory Expansion MULTIMODULE board. The iSBC 341 board connects (piggyback) onto the iSBC 286/1ØA board and allows installation of four more memory devices into the address space. The iSBC 341 board does not increase the maximum capacity, which is 256K bytes for local memory and 128K bytes for dual-port memory.

When choosing which memory space to use (dual-port or local), consider these issues:

1) Memory device access time

2) Whether other MULTIBUS boards in the system require access to the data

Typically, the access time for the dual-port memory is higher than the access time for local memory, because of the added time for the MULTIBUS arbitration logic.

In the default configuration, the CPU circuitry inserts two wait-states when accessing the dual-port memory sockets and one wait-state when accessing the local memory sockets. The number of wait-states is reconfigurable for local memory.

2.2.5.1 Local Memory

The local memory array is subdivided into two independent parts of memory address space: socket pair U4Ø/U75 and socket pair U41/U76. Socket pair U4Ø/U75 is intended to hold EPROM containing the bootstrap routine for the board and, as such, must ALWAYS be top-justified (contain the highest addresses) in the local memory address space. Socket pair U41/U76 is for user-configuration. One iSBC 341 board can be installed into chip sockets U41/U76 on the iSBC 286/1ØA board, but the total memory cannot exceed 256K bytes.

2.2.5.2 Dual-Port Memory

Other bus masters and the on-board CPU may access the dual-port memory on the iSBC 286/1ØA board. The dual-port memory on the iSBC 286/1ØA board appears to the on-board CPU and other bus masters to be an independent byte-wide memory resource on the MULTIBUS interface. The on-board CPU, however, has priority in a simultaneous access to the dual-port memory. Other MULTIBUS masters must arbitrate for control before accessing the dual-port memory. One iSBC 341 Memory Expansion MULTIMODULE Board can be installed into chip sockets U54/U87 on the iSBC 286/1ØA board, but the total memory cannot exceed 128K bytes.

2.2.6 iSBX™ INTERFACES

The iSBC 286/1ØA board provides two iSBX bus interfaces at connectors J5 and J6. Each interface can perform either 8-bit or 16-bit operations, depending on the capabilities of the iSBX MULTIMODULE board installed.

All I/O operations with the iSBX bus interface require a minimum 2 wait-state delay. Each iSBX bus interface has the option of inserting additional wait-states at the 8Ø286 CPU, by controlling its MWAIT* signal.

The iSBC 286/1ØA board assigns I/O port addresses ØØ8ØH through ØØBFH to the iSBX bus connectors if at least one iSBX MULTIMODULE board is installed. If no iSBX MULTIMODULE board is installed, the iSBC 286/1ØA board performs MULTIBUS I/O operations rather than iSBX bus interface operations for port addresses ØØ8ØH through ØØBFH.

2.2.7 iLBX™, Synchronous, and Auxiliary Interfaces

The iSBC 286/1ØA board has Connector P2 default configured as an iLBX interface. By connecting a memory board to the iSBC 286/1ØA board via the iLBX bus interface, the local memory space can be expanded to a full 14 megabytes physically located off-board.

You can also configure Connector P2 for use as a synchronous interface. The synchronous interface is also an off-board local memory extension that performs at 8.Ø MHz with Ø wait-states, using Intel's EX line of RAM boards.

Although the iSBC 286/1ØA board contains a special connector (J4) for front panel signals, some applications may require signals on the iLBX (P2) connector that operate compatibly with the auxiliary connector on other Intel single board computers. You can disable the iLBX bus interface and reconfigure the P2 connector for bussing these auxiliary signals.

2.2.8 MULTIBUS® INTERFACE

The iSBC 286/1ØA board provides some control over the MULTIBUS interface signals, including the bus lock (LOCK*), bus priority output (BPRO*), common bus request (CBRQ*), bus clock (BCLK* and CCLK*), and interrupt (INTRx*) signals.

The iSBC 286/1ØA board provides for either a serial or parallel bus priority resolution scheme. Each scheme has advantages and disadvantages. The serial scheme requires no additional backplane hardware but limits the system to three or less masters. The parallel scheme allows up to 16 masters in the system but requires additional hardware on the backplane. Refer to the INTEL MULTIBUS SPECIFICATION for more details.

The 82289 MULTIBUS Arbiter provides all the needed signals for controlling MULTIBUS arbitration.

2.2.9 PROGRAMMABLE INTERVAL TIMERS

The iSBC 286/1ØA board contains an 8254 Programmable Interval Timer (PIT). The 8254 PIT contains three independent, 16-bit programmable counters (Counters Ø, 1, and 2).

In the default configuration, all of the counters provide dedicated functions on-board:

- Counter Ø provides a programmable real-time interrupt.
- Counter 1 provides the clock for Channel B of the 8274 MPSC.
- Counter 2 provides a transmit clock for Channel A of the 8274 MPSC.

Because the counters are dedicated, the iSBC 286/1ØA board expects a specific power-on initialization for the PIT. The initialization firmware should initialize all three counters for operation, as specified in Chapter 4.

The default jumper configuration of the iSBC 286/1ØA board routes the TCLK clock signal (1.23 MHz clock) into the CLK input for all three counters within the 8254 PIT. The iSBC 286/1ØA board also provides a jumper-selectable 4 MHz clock signal (SYS CLK).

2.2.10 PROGRAMMABLE INTERRUPT CONTROLLERS

The iSBC 286/1ØA board contains two 8259A Programmable Interrupt Controller (PIC) devices. Each 8259A PIC provides eight independent levels of interrupt priority.

The iSBC 286/1ØA board can monitor or generate the MULTIBUS interrupt signals (INTØ* through INT7*). In the default configuration, the board monitors all interrupt signals from the MULTIBUS interface.

The iSBC 286/1ØA board expects the initialization routine to configure the master PIC and the slave PIC, cascaded through interrupt level IR7 on the master PIC. This configuration provides 15 levels of on-board interrupt priority plus Non-Maskable Interrupt (NMI).

As shipped, the iSBC 286/1ØA board contains jumpers connecting two interrupt levels (IR6 and IR7) on the master PIC to the on-board direct-vectored interrupt devices. A direct-vectored interrupt device can generate an interrupt signal to the master PIC and an interrupt vector to the CPU. The devices on the iSBC 286/1ØA board that can operate as direct-vectored devices are the slave PIC (on IR7) and the 8274 MPSC (on IR6), if programmed for operation in direct-vectored mode.

The iSBC 286/1ØA board can form a non-direct-vectored interrupt scheme; however, both PIC devices and the 8274 MPSC device must be programmed for non-direct-vectored mode operation. In this type of operation, the slave device gives an interrupt to the master PIC, which passes it on to the CPU. The CPU polls the slave device to determine the interrupt requirements. Neither the slave PIC nor the master PIC provides a vector.

You can define specific interrupt levels on the master PIC as bus-vectored interrupts. The master PIC receives an interrupt indication from a slave device on one of the MULTIBUS interrupt lines and passes it on to the CPU, then the MULTIBUS device provides the vector on the bus.

The iSBC 286/1ØA board provides jumpers for configuring interrupt levels Ø through 7 of the master PIC. Levels Ø through 2 are configurable on the slave PIC, but interrupt levels 3 through 7 are fixed.

NOTE

Interrupt IR6 on the master PIC is used as an on-board interrupt. The hardware does not allow the use of IR6 to service a bus-vectored interrupt.

2.2.11 NUMERIC PROCESSOR EXTENSION

The iSBC 286/1ØA board reserves a 4Ø-pin socket at chip location U25 for installing an 8Ø287 Numeric Processor Extension. The 8Ø287 Numeric Processor Extension provides a high-speed math processing device that supports the specifications in the IEEE Microcomputer Floating Point Standard P754.

Programming the 8Ø287 is done exactly as for the 8Ø87, with escape sequences into the instruction execution sequence. When the 8Ø286 executes an escape sequence, it starts program execution in the 8Ø287. At that point, the 8Ø286 and 8Ø287 devices execute instructions in parallel until the 8Ø286 executes a WAIT instruction to wait for completion of the 8Ø287 operation.

CAUTION

Before installing the 80287 chip, remove jumper E280 - E281. Failure to do so will damage the 80287 device.

***

CHAPTER 3
INSTALLATION

3.1 INTRODUCTION

This chapter provides a preview of equipment and components that you may need for your application. This chapter includes information on preparing the board's environmental conditions and also lists the equipment and components that are user-supplied. Programming and configuration information is located in Chapter 4.

3.2 UNPACKING AND INSPECTING THE BOARD

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection. Refer to Chapter 5 for repair and servicing information.

3.3 PREPARING THE BOARD ENVIRONMENT

The iSBC 286/1ØA board has several specific power, cooling, and physical space requirements. These requirements are explained in the following sections and are summarized in Table 1-1.

3.3.1 POWER REQUIREMENTS

Power is provided for the iSBC 286/1ØA board through the MULTIBUS interface. At most, the board will require three voltage levels and ground:

- +5 volt power source for all configurations
- ±12 volt power source for configurations requiring an RS232C interface or possibly a MULTIMODULE board
- Ground for all configurations

The iSBC 286/1ØA board requires a specific minimum amount of current at each power source, depending on four factors:

1) The type of user-supplied memory devices on the board
2) The quantity of user-supplied memory devices on the board
3) The types of user-supplied memory expansion MULTIMODULE boards on the board
4) The type of serial interface at Connector J2 on the board (either RS422A/449 or RS232C)

Table 1-1 lists the current requirements for each supply voltage required to operate the board in its default configuration (with an RS232C interface, but no memory chips). To calculate the total current, add the extra currents for your application to the currents in the table.

3.3.2 COOLING REQUIREMENTS

The iSBC 286/1ØA board dissipates a maximum of 527.Ø gram-calories of heat per minute (2.Ø BTU per minute). To dissipate this heat and prevent possible heat damage to the board, provide adequate air circulation to prevent the ambient air around the board from rising above 55°C (131°F). Typically, a minimum air flow of 2ØØ linear feet per minute across the board provides enough air circulation.

3.3.3 PHYSICAL DIMENSIONS

The physical dimensions of the iSBC 286/1ØA board are

Width: 3Ø.48 cm (12.ØØ inches)
Length: 17.15 cm (6.75 inches)
Depth: 1.42 cm (Ø.56 inches) with no MULTIMODULE boards
1.82 cm (Ø.718 inches) with an iSBC 341 MULTIMODULE board
2.95 cm (1.16 inches) with an iSBX MULTIMODULE board
Weight: 534 gm (19 ounces)

3.4 COMPATIBLE EQUIPMENT

The iSBC 286/1ØA board is designed to operate as either a master or an intelligent slave with other single board computers on the MULTIBUS interface. For more information on the MULTIBUS architecture, refer to the MULTIBUS HANDBOOK.

The memory configuration on the iSBC 286/1ØA board allows an iSBC 341 Memory Expansion MULTIMODULE Board to be added at these chip sockets:

- U41/U76 for local memory
- U54/U87 for dual-port memory

The iSBX bus interfaces are electrically and mechanically compatible with either 8-bit or 16-bit iSBX MULTIMODULE boards.

CAUTION

If a MULTIMODULE board is installed onto iSBX bus connector J5, ensure that the LEDs are not damaged during the connection.

The iSBC 286/1ØA board does not accept an iSBC 337A Numeric Data Processor MULTIMODULE board. Instead, use the 4Ø-pin chip socket provided for the 8Ø287 Numeric Processor Extension.

CAUTION

Before installing the 80287 chip, remove jumper E280-E281. Failure to do so may damage the 80287 device.

The iLBX bus interface on the iSBC 286/1ØA board operates compatibly with the iLBX specification. The synchronous interface on Connector P2 supports Intel's line of high-speed, high-density EX memory boards.

3.5 COMPONENTS REQUIRED

Figure 3-1 shows the location for the user-supplied parts. Table 3-1 lists all of the components that could be required for the iSBC 286/1ØA board. Install only those components required to satisfy your application.

Table 3-1. User-Supplied Components

Item No.	Part	Description
1	Memory	The local memory sockets will accept only EPROM memory devices. The dual-port sockets will accept EPROM, iRAM, or Static RAM devices. The dual-port sockets will only accept those EEPROM devices using 5V programming signals.
2	Termination Resistor Pack (RP4)	Provide a termination resistor pack at RP4 whenever the iSBC 286/1ØA board is used in a point-to-piont RS422A/449 application. Refer to Appendix B for more information.
3	Bias Resistor Pack (RP5,RP6)	Remove or change bias resistor packs at RP5 and RP6 whenever the iSBC 286/1ØA board is used in a Multidrop RS422A/449 application. Refer to Appendix B for more information.
4	3487 (U15)	Provide an IC (3487) device at socket U15 when using the J2 connector as an RS422A/449 interface.
5	Programmable Array Logic Chip (U74)	Change the PAL whenever a memory configuration is required beyond those provided by PAL U74. The PAL is a 16L8A device by Monolithic Memories, Inc., or an equivalent.
6	8Ø287	Insert an 8Ø287 in socket U25 to achieve high performance floating-point instruction. To prevent possible damage, remove jumper E28Ø-E281 before 8Ø287 insertion.

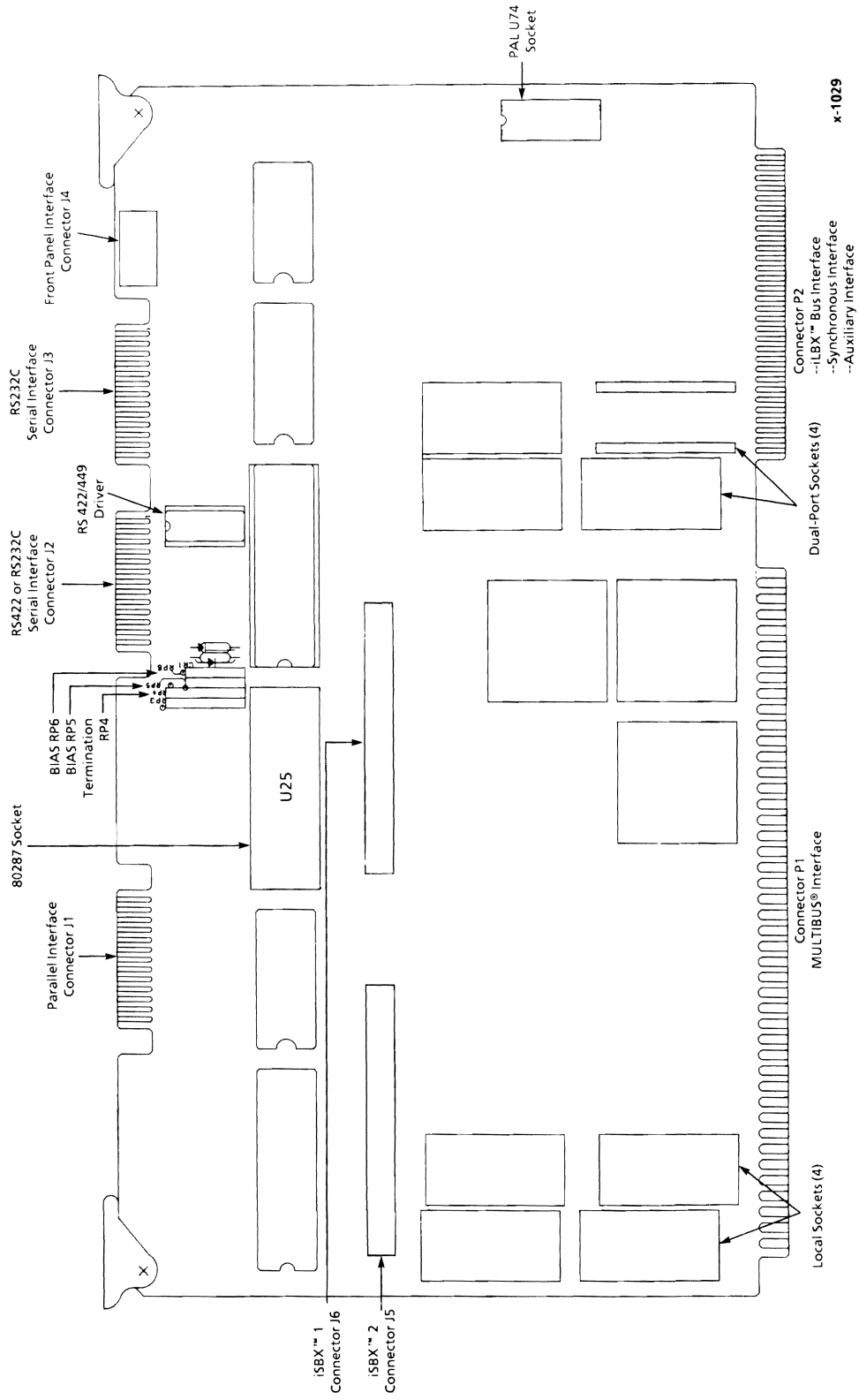


Figure 3-1. User-Supplied Components Location Diagram

3.6 COMPONENT INSTALLATION

The following sections provide instructions for installing the user-supplied memory devices and bias/termination resistors. Figure 3-1 shows an approximate location for each component. Table 3-1 gives a description of each type of component. Any electrically and mechanically equivalent components may be substituted.

When installing the integrated circuit packages into the sockets on the iSBC 286/1ØA board, ensure that pin 1 of the chip is inserted into pin 1 of the chip socket. This orientation places pin 1 of the chip closest to the silk-screened dot (which indicates pin 1 of the socket).

3.6.1 MEMORY COMPONENTS

The iSBC 286/1ØA board contains no memory components when shipped from the factory. One of several different types of memory components can be installed into the memory sockets, including EPROM, iRAM, and Static RAM devices. Figure 3-2 shows how to install either 24-pin or 28-pin memory chips into the JEDEC-compatible sockets. Refer to Chapter 4 for instructions on configuring the memory addresses at each socket.

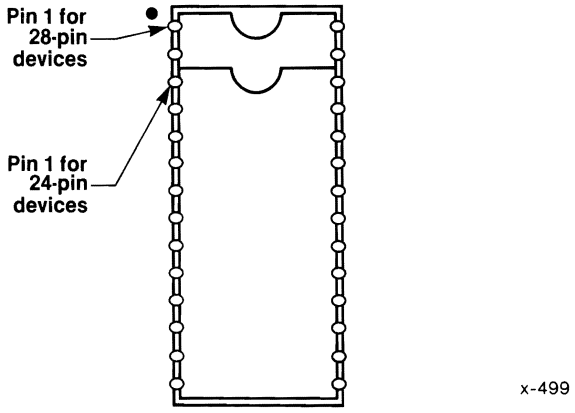


Figure 3-2. Memory Chip Installation

CAUTION

Never insert components into a board when power is applied. Doing so could damage the components.

CAUTION

All MOS components such as ROM, EPROM, and RAM devices are highly susceptible to damage from static electricity. Use extreme caution when installing MOS components in a low-humidity environment. Always ground yourself before handling MOS components; this ensures that a static charge build-up is not dissipated through the MOS devices.

User-supplied memory devices can be installed into the eight 28-pin JEDEC-compatible chip sockets on the iSBC 286/1ØA board. Table 3-2 lists these types of memory devices. In selecting memory components, you can substitute any electrically and mechanically equivalent devices.

Table 3-2. Compatible Memory Devices

Memory Type	Memory Capacity	Chip Example	Chip Location	
			Local	Dual-Port
Static RAM	2Kx8	---	no	yes
	8Kx8	---	no	yes
	16Kx8	---	no	yes
iRAM	8Kx8	2186	no	yes
	16Kx8	---	no	yes
EPROM	4Kx8	2732	yes	yes
	8Kx8	2764	yes	yes
	16Kx8	27128	yes	yes
	32Kx8	27256	yes	yes
	64Kx8	27512	yes	yes

NOTE

The iSBC 286/1ØA board is designed to accept most byte-wide components in the memory sockets. Typically, system operation requires EPROM devices in sockets U4Ø/U75 to hold the bootstrap program.

NOTE

The iSBC 286/1ØA board can accommodate both 24- and 28-pin memory chips in the same socket. The 24-pin integrated circuits must be installed, as shown in Figure 3-2, with pin 1 of the integrated circuit in pin 3 of the socket.

3.6.2 LINE DRIVER DEVICES

When shipped from the factory, the iSBC 286/1ØA board contains the line driver and line receiver chips required for RS232C interfaces at Connectors J2 and J3. Connector J2 can be modified for RS422A/449 operation, while Connector J3 cannot be modified.

3.6.3 RESISTOR PACKS

The iSBC 286/1ØA board contains two resistor packs (RP5 and RP6) that perform biasing and one empty socket for a termination resistor pack (RP4). Figure 3-3 shows the bias and terminator resistor types.

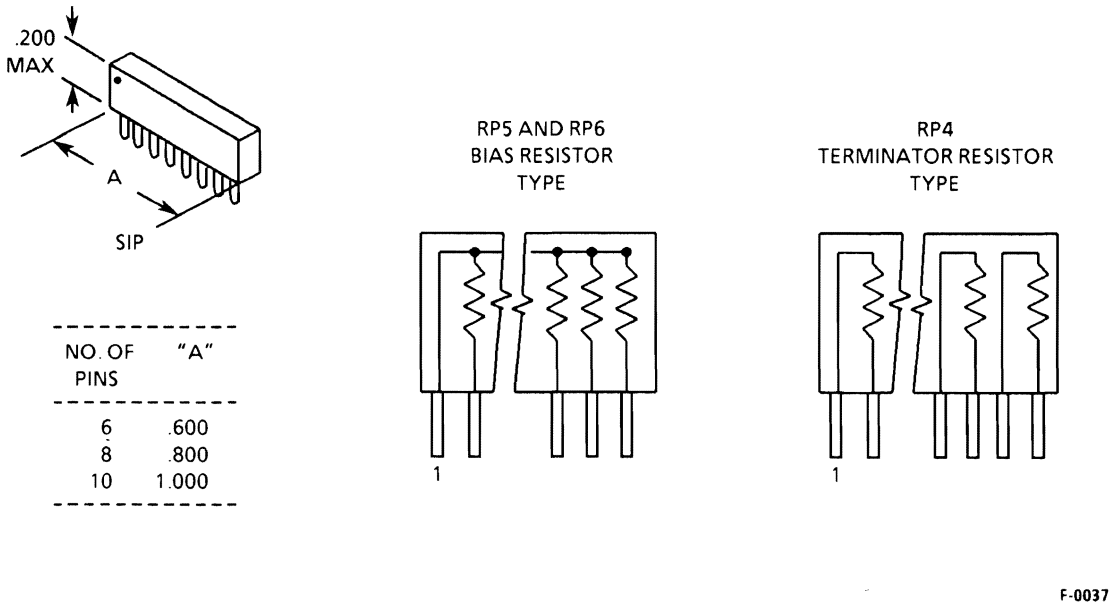


Figure 3-3. Bias and Terminator Resistor Types

The functions of each resistor pack depend on the operating mode of the interface at Connector J2, as follows:

RP4 TERMINATION - For an RS422A/449 multidrop network, if the board is the farthest slave from the master in the network, install a resistor pack at RP4 to properly terminate the signal lines. Refer to Appendix B for instructions on calculating the value for RP4.

For an RS232C interface application, do not install a resistor pack at RP4.

RP5 BIAS - For an RS422A/449 master interface (either a multidrop or point-to-point network), install the resistor pack at RP5 with pin 1 closest to connector J2 (18Ø-degree rotation from the default configuration). RP5 maintains voltage levels on the signal lines.

For an RS422A/449 slave interface in a multidrop network, remove the resistor pack at RP5.

For an RS232C interface, install the resistor pack at RP5 with pin-1 closest to the MULTIBUS connector (the default configuration).

RP6 BIAS - For an RS422A/449 master interface in a multidrop network, install the resistor pack at RP6 (the default configuration). RP6 maintains voltage levels on the signal lines.

For an RS422A/449 slave interface in a multidrop network, remove the resistor pack at RP6.

For an RS232C application, install the resistor pack at RP6 (the default configuration) to maintain voltage levels on the signal lines.

The following sections provide more information on the default configuration of each R-pack.

3.6.3.1 Bias Resistors

When shipped from the factory, the iSBC 286/1ØA board contains two six-pin sockets with 2.2K ohm bias resistor packs (RP5 and RP6). These resistor packs provide bias for a four-drop RS422A/449 interface at Connector J2. At shipment, the SIP devices are installed so that pin 1 of RP5 is in pin 6 of its socket, and pin 1 of RP6 is in pin 1 of its socket.

By removing RP5, rotating it 18Ø degrees, and reinstalling it so that pin 1 is farthest from the MULTIBUS connector (so that pin 1 of the pack is in pin 1 of the socket), the board is configured to hold the four noninverting inputs to U11 at an inactive voltage level. This is required because the RS232C interface does not implement those lines.

By changing the value of the resistor pack, the bias at the serial interface receivers can be changed. Appendix B shows how to calculate the bias resistor values for an application.

3.6.3.2 Termination Resistors

When shipped from the factory, the iSBC 286/1ØA board provides an empty socket at RP4 for a single in-line resistor pack (SIP) RP4.

Termination resistors are required only for RS422A/449 interface applications on Connector J2. They provide a means of reducing the amount of signal noise between the lines of a differential pair. If the iSBC 286/1ØA board is the unit farthest from the primary master in a multidrop network, install an eight-pin termination SIP into socket RP4.

Determine the resistor value to terminate a multidrop or point-to-point network by performing a series of calculations as listed in Appendix B.

3.7 CONNECTOR AND CABLE PARTS

Some connector parts are required for the iSBC 286/1ØA board when it is used in certain applications. Figure 3-1 shows the approximate location of the five connector types:

- Three 26-pin edge connectors (J1, J2, and J3)
- A 14-pin front panel interface connector (J4)
- Two 36- or 44-pin iSBX bus connectors (J5 and J6)
- An 86-pin MULTIBUS interface connector (P1)
- A 6Ø-pin iLBX bus interface connector (P2)

Table 3-3 provides a list of connector parts that are ready-made to interface to the board connectors. The table also provides the manufacturers' names and part numbers to order the connectors. Any electrically and mechanically equivalent parts may be substituted.

Table 3-4 provides information on cables compatible with the connector parts in Table 3-3 for the serial I/O interfaces at Connectors J2 and J3.

Table 3-3. User-Supplied Connector Information

Function	# of Pins	Centers (inches)	Connector Type	Vendor	Vendor Part Number
MULTIBUS connector (P1)	86	Ø.156	Soldered[1] PC board mount	VIKING ELFAB	2KH43/9AMK12 BS1562D43PBB
			Wirewrap Without ears	EDAC ELFAB	337Ø8654Ø2Ø1 BW1562D43PBB
			Wirewrap (.128 dia.) Mounting holes	EDAC ELFAB	337Ø8654Ø2Ø2 BW1562A43PBB
iLBX bus connector (P2)	6Ø	Ø.1	Solder Solder Solder	KELAM KELAM T&B Ansley	RF3Ø-28Ø3-5 11Ø-1Ø-ØØ1-37 A3Ø2Ø
		Ø.1	Soldered	ELFAB EDAC	97169ØØ1 34Ø6Ø5243ØØ
			Wirewrap No ears	ELFAB EDAC	BW1Ø2ØD3ØPBB 345Ø6Ø54Ø2Ø1
			Wirewrap	ELFAB EDAC	BS1Ø2ØA3ØPBB 345Ø6Ø5248Ø2
			Wirewrap (.128 dia.)	TI Viking	H421121-3Ø 3KH3Ø/9JNK
iSBX bus connector male 16-bit female (J5, J6)	36	Ø.1	Soldered	Viking Viking	ØØØ292-ØØØ1 ØØØ291-ØØØ1

----------(continued)----------

Table 3-3. User-Supplied Connector Information (continued)

Function	# of Pins	Centers (inches)	Connector Type	Vendor	Vendor Part Number
iSBX bus connector 16-bit (J5, J6)	44	Ø.1	Soldered	Viking Viking	ØØØ293-ØØØ1 male ØØØ294-ØØØ1 female
Parallel connector (J1)	26	Ø.1	Wirewrap Soldered Flat crimp Flat crimp	EDAC EDAC 3M AMP	345Ø2654Ø2Ø1 345Ø265ØØ2Ø1 3462-ØØØ1 88373-5
Serial I/O connector (J2,J3)	26	Ø.1	Wirewrap Soldered Flat crimp Flat crimp	EDAC EDAC 3M AMP	345Ø2654Ø2Ø1 345Ø265ØØ2Ø1 3462-ØØØ1 88373-5
Front panel connector (J4)	14	Ø.5	Soldered	BERG	65Ø43-Ø3Ø

Notes: 1. Connector heights are not guaranteed to conform to Intel packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to Intel packaging equipment.

Table 3-4. Cable Information

Interface Type	Mode[1]	MULTIMODULE™ Edge Connector	Cable	Interface Connector
RS232C	DTE	26-pin[2], 3M-3462-ØØØ1	3M[3]-3349/25	25-pin[4], 3M-3482-1ØØØ
RS232C	DCE	26-pin, 3M-3462-ØØØ1	3M-3349/25	25-pin, 3M-3483-1ØØØ
RS449	DCE	26-pin, 3M-3462-ØØØ1	3M-3349/25	37-pin[5], 3M-35Ø3-1ØØØ

Notes:
1. DTE=Data Terminal Equipment mode (male connector). DCE=Data Communication Equipment mode (female connector).
2. Pin 26 of the edge connector is not connected to the flat cable.
3. Cable is tapered at one end to fit the 3M-3462 connector.
4. May be used with the cable housing 3M-3485-1ØØØ.
5. Cable housing 3M-3485-4ØØØ may be used with the connector.

3.8 iSBC® 286/10A BOARD INSTALLATION

This installation procedure assumes you have already configured the board for your system and you have all the necessary connectors and cables ready for installation.

1. Ensure that power to your system/cardcage is OFF.
2. Slide the board into its cardslot in the cardcage and firmly seat it in the P1 and P2 connectors. Ensure the cardslot is properly configured for bus priority.
3. Connect all required I/O cables to the board.

This completes the installation for the iSBC 286/1ØA board.

***

CHAPTER 4
CONFIGURATION

4.1 INTRODUCTION

This chapter describes the configuration of each independent function on the board and includes jumper, addressing, interface, and programming information, covered in the following sections:

4.2	CPU and CPU Support Circuitry
4.3	8Ø287 Math Coprocessor
4.4	Interrupt Handling (with the PIC devices)
4.5	Programmable Interval Timers (with the PIT device)
4.6	iSBX Interfaces - J5 & J6
4.7	MULTIBUS Interface - P1
4.8	Parallel I/O Interface (with the PPI device) - J1
4.9	Serial I/O Interfaces (with the MPSC device) - J2 & J3
4.1Ø	Front Panel Interface - J4
4.11	iLBX, Synchronous, and Auxiliary Interfaces - P2
4.12	Memory

Appendix A consolidates the jumper information into a jumper location diagram, jumper description list, and schematic jumper index list.

Figure 2-1 shows a detailed block diagram of the functions on the board. The following sections describe the configurations available for each functional area.

4.2 CPU AND CPU SUPPORT CIRCUITRY CONFIGURATIONS

The iSBC 286/1ØA board has several configuration options for directly configuring the operation of the CPU and its support circuits:

- CPU operating mode selection, either in Real Address or Protected Virtual Address Mode
- CPU wait-state selection for local memory, either 1, 2, or 3 wait-state operation
- CPU clock, either 8 MHz or 4.9 MHz

Each is described in more detail in the following sections.

4.2.1 CPU MODE SELECTION

You must configure the 8Ø286 CPU for operation in one of two software-selectable modes: Real Address Mode or Protected Virtual Address Mode (PVAM).

In Real Address mode, the 8Ø286 CPU operates similarly to an 8Ø86 or 8Ø88 CPU, but with higher performance. As such, the 8Ø286 CPU can access up to one megabyte of real memory.

PVAM operation of the 8Ø286 CPU provides two features in addition to those available in Real Address mode operation:

1) It allows the 8Ø286 CPU to access up to 16 megabytes of real memory and one gigabyte of virtual memory.

2) It provides a series of hierarchical priority levels and the extended instruction set required to control them. Effectively using the priority structure requires certain software features not available from all operating systems.

You must use the 8Ø286 CPU in PVAM if you intend to address more than 1 megabyte of memory or to use an operating system compatible with its memory protection features.

After power-up, the 8Ø286 CPU on the iSBC 286/1ØA board begins operation in Real Address mode. You have the choice, at that point, to either use the CPU in Real Address mode or further initialize the CPU into PVAM.

The architecture of the CPU is such that you can switch from Real Address to PVAM, but not from PVAM to Real Address mode. The only way you can force the 8Ø286 CPU to re-enter Real Address mode (after going to PVAM) is by performing a reset.

Switching from Real Mode to PVAM requires two steps:

1. Switch the CPU to PVAM by setting bit Ø within the Machine Status Word register in the 8Ø286 CPU using the LMSW instruction.

2. Switch the iSBC 286/1ØA board by performing a word write operation to Port B of the 8255A PPI device, port address ØØCAH. The data value written to the parallel port is not significant. This enables the 24-bit addressing mode.

NOTE

The 8Ø286 CPU must be switched to PVAM before the iSBC 286/1ØA board. Switching the board first will cause the system to hang, because the memory map is relocated.

4.2.2 CPU WAIT-STATE SELECTION

You can configure the number of wait-states for local memory; you can select either 1, 2, or 3. You cannot configure the wait-states for I/O, dual-port memory, or iLBX memory accesses. An I/O operation requires two wait-states, a dual-port operation requires two wait-states, and an iLBX bus operation requires a minimum of one wait-state delay (or Ø wait-states for the synchronous interface) in the CPU. For more information on wait-state configuration for local memory, refer to Section 4.12.3.2.4 and Appendix D.

4.2.3 CPU CLOCK SELECTION

You can configure the 8Ø286 CPU for 8 MHz or 4.9 MHz. The jumper configuration is listed in Table 4-1.

4.3 80287 MATH PROCESSOR EXTENSION CONFIGURATION

You can add high-speed floating-point numeric processing to the board. In the default configuration, the iSBC 286/1ØA board does not contain an 8Ø287 device. However, if you require the capability, you can easily install an 8Ø287 at chip socket U25 on the board. The following sections describe how to install the 8Ø287, configure the clock jumpers, and program the device.

4.3.1 80287 INSTALLATION

Figure 3-1 shows the location of chip socket U25. You can insert the 8Ø287 chip directly into this socket. When installing the chip, ensure that pin 1 of the chip aligns with pin 1 of the socket.

CAUTION

Before installing the 80287 chip, remove jumper E280 - E281. Failure to do so will damage the 80287 device.

4.3.2 80287 JUMPER CONFIGURATIONS

The clock rate to the 8Ø287 device is configurable. You have three choices in configuring the clock rate; two are synchronous with the 8Ø286 CPU clock and one is asynchronous. The asynchronous option operates the 8Ø287 and the 8Ø286 CPU from two independent clock sources.

The default configuration provides a 16.Ø MHz clock input to both the 8Ø287 and the 8Ø286 CPU, from the 82284 Clock Generator. The 8Ø286 performs an internal divide by two, resulting in 8.Ø MHz processing. The 8Ø287 has an internal divide by three, resulting in 5.33 MHz numeric processing.

Jumpers E149 through E153 provide the clock select options. Table 4-1 lists the jumper options available for selecting a clock rate for the 8Ø287.

Table 4-1. CPU and Numeric Processor Clock Options

Type of Operation	Jumper Connections Required
8Ø286 CPU Configuration	
Select 8Ø286 operation at 8.Ø MHz. Default configuration.	E216-E217 § installed
Select 8Ø286 operation at 4.9 MHz.	E216-E217 removed
8Ø287 Numeric Processor Extension Configuration	
Select 8Ø287 operation at 3.28 MHz. 8Ø286 CPU at 4.9 MHz.	E216-E217 removed E151-E152 removed E152-E153 installed E149-E15Ø installed
Select 8Ø287 operation at 5.33 MHz. Default configuration. 8Ø286 CPU at 8.Ø MHz.	E216-E217 § installed E151-E152 § removed E152-E153 § installed E149-E15Ø § installed
Select independent 8Ø287 operation at 8.Ø MHz. Independent of 8Ø286 CPU clock.	E216-E217 not significant E151-E152 installed E149, E15Ø, E153 not connected

Note: Failure to remove jumper E28Ø - E281, before inserting the 8Ø287 Math Processor, will damage the 8Ø287 device.
§ identifies default configuration.

4.3.3 80287 PROGRAMMING

The 8Ø286 CPU communicates with the 8Ø287 via four word-wide I/O port addresses: ØØF8H through ØØFFH. You must ensure that your application code does not attempt to access or use these addresses; treat them as reserved. Their programming is performed automatically by the hardware within the 8Ø286 CPU whenever it decodes an instruction for the 8Ø287.

NOTE

To avoid corrupting operation of the 8Ø287, you should ensure that your software never attempts to access I/O ports in the range ØØF8H-ØØFFH.

You initiate an 8Ø287 operation by placing an 8Ø287 instruction into the execution code for the 8Ø286 CPU. When the 8Ø286 decodes an 8Ø287 instruction, the 8Ø286 CPU generates an I/O sequence that starts instruction execution in the 8Ø287. Meanwhile, the 8Ø286 CPU continues to execute its code.

If the operation in the 8Ø287 requires that the 8Ø287 eventually store data in memory, the 8Ø286 will monitor the operation status of the 8Ø287 and perform the operation with memory.

After placing an 8Ø287 instruction into the 8Ø286 instruction stream, you can allow the 8Ø286 CPU to execute several 8Ø287 nonreferencing instructions. This allows the 8Ø287 time to complete the instruction before it receives the next one. Failure to do so causes the 8Ø286 CPU to wait for a "done" status from the 8Ø287 (for the previous operation).

4.4 INTERRUPT HANDLING (WITH THE PIC DEVICES)

The iSBC 286/1ØA board contains two 8259A Programmable Interrupt Controller (PIC) devices that supply most of the interrupt logic on the board. You can configure the board for several types of interrupt operation depending on how you program the interrupt sensing and generating devices.

The iSBC 286/1ØA board provides an interrupt vector table for up to 256 interrupt vectors, some of which are reserved. Refer to Intel's HIGH PERFORMANCE MICROPROCESSOR WITH MEMORY MANAGEMENT & PROTECTION DATA SHEET for a map of this interrupt vector table.

Four basic operating modes service the interrupts. The differences in the modes are described in the following sections, as well as how to use the time-out circuitry.

4.4.1 INTERRUPT MODES

The iSBC 286/1ØA board can operate in one of four interrupt modes:

- Polled
- Polled and vectored
- Direct-vectored
- Bus-vectored

In a polled mode environment, the 8Ø286 CPU does not receive an interrupt request but polls each device that it operates. By doing so, the CPU provides service on regular intervals. If using polled mode, ensure that both the 8274 MPSC and the 8259A PIC devices are initialized for polled mode operation.

Vectored and polled mode is similar to polled mode. However, in this mode, the master PIC provides a vector and an interrupt request to the 8Ø286 CPU. Then, the CPU follows the interrupt request with a poll of the device to get information that further defines the request. The iSBC 286/1ØA board provides three devices that you can operate in vectored and polled mode: the two 8259A PICs and the 8274 MPSC.

Direct-vectored mode uses the automatic vectoring capabilities of the 8274 MPSC and the 8259A PIC devices. In direct-vectored mode, a slave device provides an interrupt signal to the master 8259A PIC, which in turn passes the interrupt request to the 8Ø286 CPU. The master PIC, however, does not provide the interrupt vector; it allows the slave (that requested the interrupt) to give the vector to the 8Ø286 CPU. Only those slave devices that are on-board, that are capable of generating an interrupt vector, and that are monitored by the master 8259A PIC can operate in direct-vectored mode.

Bus-vectored mode is similar to direct-vectored mode. However, in this mode, the 8Ø286 CPU does not know where the vector originates; it could come from either on-board or off-board. As a result, the iSBC 286/1ØA board must gain control of the MULTIBUS interface for each interrupt request.

In bus-vectored mode, a slave device (that may be off-board) provides an interrupt signal to the master 8259A PIC, which in turn passes the interrupt request signal to the 8Ø286 CPU. The master PIC, however, does not provide the interrupt vector; it allows the requesting slave to give the vector to the 8Ø286 CPU. Only those devices that can generate an interrupt vector and operate through the master 8259A PIC can operate in bus-vectored mode.

You select one of the interrupt servicing modes by initializing the 8259A PIC devices and the 8274 MPSC device, and by configuring jumpers on the iSBC 286/1ØA board. Each is discussed in greater detail in the following sections.

4.4.2 MODE SELECTION

When shipped from the factory, the iSBC 286/1ØA board contains two devices that are cascaded through the master PIC and that are capable of providing a vector: the 8274 MPSC and the slave 8259A PIC. You should initialize these devices for vectored operations, as shown later in this section.

Although it is default configured for bus-vectored operation (across the MULTIBUS interface), you can reconfigure the iSBC 286/1ØA board for either direct-vectored, vectored and polled, or polled mode operation by removing jumpers and re-initializing the programmable chips (the 8274 MPSC and the 8259A PIC devices).

To configure for bus-vectored mode operation, you must:

- Install jumper E231-E232§ The iSBC 286/1ØA board can now gain control of the MULTIBUS interface for each interrupt request.
- Install jumper E92-E1Ø6§ (Slave PIC INT to IR7 on master PIC)
- Install jumper E1ØØ-E98§ (8274 INT to IR6 on master PIC)
- Program the slave PIC for vectored mode operation
- Program the master PIC for vectored mode operation
- Program the 8274 MPSC for vectored mode operation

To configure for direct-vectored mode operation (if bus-vectored mode is never used), you must:

- Remove jumper E231-E232
- Install jumper E92-E1Ø6§
- Install jumper E1ØØ-E98§
- Program the master PIC for non-single mode (cascade mode)
- Program the slave PIC for direct vectoring
- Program the 8274 MPSC for direct vectoring

To configure for vectored and polled mode operation, you must:

- Remove jumper E231-E232
- Install jumper E92-E1Ø6§ (Slave PIC INT to IR7 on master PIC)
- Install jumper E1ØØ-E98§ (8274 INT to IR6 on master PIC)
- Program each PIC for polled mode (non-cascade mode)
- Program the 8274 MPSC for non-vectored mode operation

To configure for polled mode operation, you must:

- Configuration of jumper E231-E232 is not important
- Configuration of jumper E92-E1Ø6 is not important
- Configuration of jumper E1ØØ-E98 is not important
- Program each PIC for polled mode (non-cascade mode)
- Program the 8274 MPSC for non-vectored mode operation

4.4.3 INTERRUPT JUMPER MATRIX CONFIGURATION

The iSBC 286/1ØA board contains an array of 56 stake pins to configure the interrupt functions. Figure 4-1 shows the interrupt stake pins in the default configuration.

As shipped from the factory, the iSBC 286/1ØA board contains 11 interrupt jumpers in the interrupt jumper matrix, as follows:

E94-E131	§	Provides a timer interrupt from Counter Ø of the 8254 PIT to the master PIC Level Ø
E98-E1ØØ	§	Provides a serial interrupt from the 8274 MPSC to the master PIC Level 6
E92-E1Ø6	§	Provides an interrupt signal from the slave PIC (U27)
E122-E147	§	Connects INTØ* (MULTIBUS) to NMI
E126-E141	§	Connects INT1* (MULTIBUS) to IR1 on master PIC
E121-E135	§	Connects INT2* (MULTIBUS) to IR2 on master PIC
E116-E13Ø	§	Connects INT3* (MULTIBUS) to IR3 on master PIC
E11Ø-E125	§	Connects INT4* (MULTIBUS) to IR4 on master PIC
E1Ø4-E12Ø	§	Connects INT5* (MULTIBUS) to IR5 on master PIC
E114-E143	§	Connects INT6* (MULTIBUS) to SINTØ (slave PIC IRØ)
E1Ø8-E144	§	Connects INT7* (MULTIBUS) to SINT1 (slave PIC IR1)

§ identifies the default configuration.

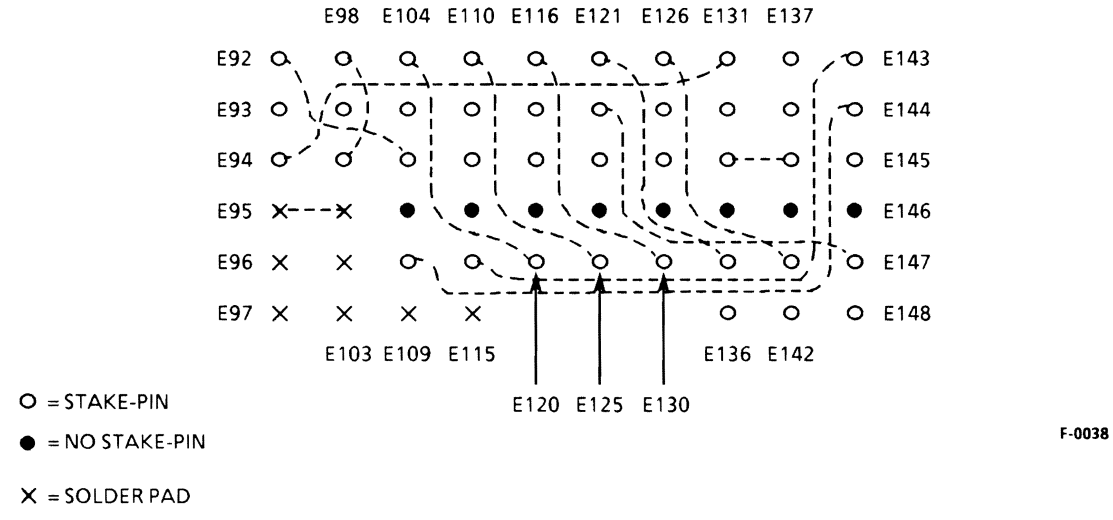


Figure 4-1. Interrupt Jumper Matrix

With this jumper configuration, the iSBC 286/1ØA board operates U24 as a master PIC and U27 as a slave PIC. As such, both PIC devices operate in bus-vectored mode; any interrupt sensed by either PIC device causes the master PIC to expect an interrupt vector on the bus.

Tables 4-2 and 4-3 list the interrupt sources and destinations available at the interrupt jumper matrix on the iSBC 286/1ØA board. Table 4-4 lists the default jumper configuration for the interrupt levels of each PIC device on the board.

NOTE

Whenever the iSBC 286/1ØA board services a bus-vectored interrupt, it must have control of the MULTIBUS interface.

Attempting to service a bus-vectored interrupt without jumper E231-E232 installed or without initializing the PIC devices and the 8274 MPSC device in bus-vectored mode can halt board operation. Ensure proper set up before using vectored interrupts.

Table 4-2. Interrupt Source Jumper Matrix Options

Jumper Numbers	Interrupt Sources	
E93	Counter 1 Output (CNTR1)	
E94	Counter Ø Output (CNTRØ)	
E1ØØ	Serial Channel Interrupt Request	
E1Ø6	Slave PIC U27 Interrupt Request	
E111	Edge-sense Latch Output	
E112	Timeout Interrupt	
E117	Inverter U4 Output	
E118	Bus Request Error (Active Low)	
E123	Interrupt signal from PC5 of PPI device (Active Low)	
E127	Ground (for NMI)	
E128	Front Panel Interrupt (Active Low)	
E132	Power Fail Interrupt (Active Low)	
E187	OR-gate U42 Output	
E147	MULTIBUS Interrupt Level Ø (INTØ*)	Input
E141	MULTIBUS Interrupt Level 1 (INT1*)	Input
E135	MULTIBUS Interrupt Level 2 (INT2*)	Input
E13Ø	MULTIBUS Interrupt Level 3 (INT3*)	Input
E125	MULTIBUS Interrupt Level 4 (INT4*)	Input
E12Ø	MULTIBUS Interrupt Level 5 (INT5*)	Input
E114	MULTIBUS Interrupt Level 6 (INT6*)	Input
E1Ø8	MULTIBUS Interrupt Level 7 (INT7*)	Input

Table 4-3. Interrupt Destination Jumper Matrix Options

Jumper Numbers	Interrupt Destinations
E92	Master PIC U24 Interrupt Level 7 (IR7)
E98	Master PIC U24 Interrupt Level 6 (IR6)
E1Ø4	Master PIC U24 Interrupt Level 5 (IR5)
E11Ø	Master PIC U24 Interrupt Level 4 (IR4)
E116	Master PIC U24 Interrupt Level 3 (IR3)
E121	Master PIC U24 Interrupt Level 2 (IR2)
E126	Master PIC U24 Interrupt Level 1 (IR1)
E131	Master PIC U24 Interrupt Level Ø (IRØ)
E99	Inverter U4 Input
E1Ø5	Edge-sense Latch Input (Active Low)
E122	NMI Input to CPU (NMI)
E185	OR-gate U42 Input
E186	OR-gate U42 Input
E143	Slave PIC U27 Interrupt Level Ø (SINTØ)
E144	Slave PIC U27 Interrupt Level 1 (SINT1)
E145	Slave PIC U27 Interrupt Level 2 (SINT2)
E238	MULTIBUS Interrupt Line Ø (INTØ*) Output
E239	MULTIBUS Interrupt Line 1 (INT1*) Output
E24Ø	MULTIBUS Interrupt Line 2 (INT2*) Output
E241	MULTIBUS Interrupt Line 3 (INT3*) Output
E242	MULTIBUS Interrupt Line 4 (INT4*) Output
E243	MULTIBUS Interrupt Line 5 (INT5*) Output
E244	MULTIBUS Interrupt Line 6 (INT6*) Output
E245	MULTIBUS Interrupt Line 7 (INT7*) Output

Table 4-4. Default 8259A Interrupt Level Configuration

Level	PIC	Jumper	Location	Function
IRØ		E94-E131	Interrupt Matrix	Output from Counter Ø of the 8254 PIT
IR1	M	E126-E141	Interrupt Matrix	MB INT1 to PIC U24, IR1
IR2	A S	E121-E135	Interrupt Matrix	MULTIBUS Interrupt signal line INT2*
IR3	T	E116-E13Ø	Interrupt Matrix	MB INT3* to PIC U24, IR3
IR4	E	E11Ø-E125	Interrupt Matrix	MB INT4* to PIC U24, IR4
IR5	R	E1Ø4-E12Ø	Interrupt Matrix	MB INT5* to PIC U24, IR5
IR6		E98-E1ØØ	Interrupt Matrix	Interrupt signal from the 8274 MPSC
IR7		E92-E1Ø6	Interrupt Matrix	Interrupt signal from the slave PIC

(continued)

Table 4-4. Default 8259A Interrupt Level Configuration (continued)

Level	PIC	Jumper	Location	Function
IRØ		E143-E114	Interrupt Matrix	MB INT6* to PIC U27, IRØ
IR1		E144-E1Ø8	Interrupt Matrix	MB INT7* to PIC U27, IR1
IR2	S	E145	Interrupt Matrix	Not connected
IR3	L A	None	Permanent connection	MINTRØ from iSBX bus Connector J6
IR4	V E	None	Permanent connection	MINTR1 from iSBX bus Connector J6
IR5		None	Permanent connection	MINTRØ from iSBX bus Connector J5
IR6		None	Permanent connection	MINTR1 from iSBX bus Connector J5
IR7		None	Permanent connection	Interrupt signal from the Line Printer Interface

The interrupt facilities also include some logic components that you can apply to your interrupt scheme, if necessary. These logic components are a 74LSØ4 inverter (U4), a 74LS279 latch (U3) that is pulse-triggered, and a 74S32 OR-gate (U42).

4.4.4 INTERRUPT SUPPORT LOGIC

This section explains how to configure the time-out protocol as well as how to convert an edge-triggered signal to a latched active-high signal.

4.4.4.1 Time-Out Configuration

For MULTIBUS requests, there are two ways to receive the time-out signal:

1. When the bus is not acquired 1Ø ms after the 82289 Bus Arbiter requests it,

   or if the bus is acquired,

2. by not getting the MULTIBUS XACK signal within 1Ø ms of acquiring the bus.

The first condition activates BUS REQ ERR*, a falling edge-triggered signal.

For iLBX bus or synchronous interface requests, time-out is triggered when no iLBX XACK is acquired after 1Ø ms of request.

The yellow LED comes on when time-out occurs. You can turn off the LED and reset the flip-flop by programming bit PC3 of the PPI device to go low and then high.

The time-out signal is available at the interrupt matrix at pin E112, which may be connected to a PIC for an interrupt (for example, IR2 on the slave PIC, pin E145). The program can then recognize this interrupt as a time-out error and run a service interrupt routine, part of which would reset the time-out flip-flop. If connected, the time-out interrupt will stay active (latched active high) until it is reset. The time-out flip-flop is also reset by programming bit PC3 of the PPI device low.

4.4.4.2 Changing Signals from Edge-Triggered to Level-Active

Any edge-triggered signal may be converted to a latched active-high signal, typically for use as an interrupt. Connect a falling edge-triggered signal (for example, BUS REQ ERR* at pin E118) to stake pin E1Ø5. The latched active-high output is then available at stake pin E111. Connect a rising edge-triggered signal (for example, CNTR1 at pin E94) to E99, to invert the signal. Then connect the inverted signal (now falling edge-triggered) at pin E117 to E1Ø5, to create a latched active-high output at E111.

The latched active-high output (pin E111) can now be connected to a PIC (for example, IR2 on the slave PIC, pin E145). The latched output is cleared by programming PC4 of the PPI to go low and then high, which may be accomplished in the interrupt service routine.

4.4.5 PIC PROGRAMMING

This section presents the port addresses and the parameter sequences required for the PIC devices on the iSBC 286/1ØA board.

4.4.5.1 PIC Port Addressing

You can use four I/O port addresses to program the operation of the PIC devices on the iSBC 286/1ØA board. Table 4-5 lists these addresses and the functions performed by each.

4.4.5.2 PIC Initialization Sequence

You must initialize both PIC devices on the iSBC 286/1ØA board for operation. If you cannot use the PIC devices when configured as-shipped, you can change the jumper configurations and power-up initialization routine so that it sends different initialization command words to the PIC devices.

Each PIC requires that you issue parameters to it in this order:

```
ICW1              -- Interrupt Control Word One
ICW2              -- Interrupt Control Word Two
ICW3 (if needed)  -- Interrupt Control Word Three
ICW4              -- Interrupt Control Word Four
OCW1 (if needed)  -- Output Control Word One
```

Table 4-5. Port Addresses for the 8259A PIC Devices

I/O Address	Device	Operation	Function Performed
ØØCØH	Master PIC	Byte Read: Byte Write: Word:	Status and Poll Registers ICW1, OCW2, and OCW3 Parameters N/A
ØØC2H	Master PIC	Byte Read: Byte Write: Word:	Mask Register or OCW1 Parameter Mask Register or ICW2, ICW3, ICW4, and OCW1 Parameters N/A
ØØC4H	Slave PIC	Byte Read: Byte Write: Word:	Status and Poll Registers ICW1, OCW2, and OCW3 Parameters N/A
ØØC6H	Slave PIC	Byte Read: Byte Write: Word:	Mask Register or OCW1 Parameter Mask Register or ICW2, ICW3, ICW4, and OCW1 Parameters N/A

Table 4-6 lists a programming sequence that initializes the PIC for the default configuration. As such, each PIC requires initialization to the cascaded mode of operation, CALL address interval of 4, 8Ø86 mode, and buffered mode. For additional details on parameters for the 8259A PIC, refer to Intel's MICROSYSTEM COMPONENTS HANDBOOK.

To avoid unexpected interrupts, you should either mask or ground all unused inputs to the PIC devices during initialization.

Table 4-6. Parameter Sequence for PIC Initialization

Sequence	Port/ Data	Functions Performed in 8259A PIC
1.	ØCØH Ø19H	Port Number for master PIC Data; ICW1. This parameter specifies level-triggered operation, cascaded operation, and ICW4 parameter required.
2.	ØC2H Ø2ØH	Port Number for master PIC Data; ICW2. This parameter provides T3 through T7 of the interrupt vector (to be multiplied by 4).
3.	ØC2H ØCØH	Port Number for master PIC Data; ICW3 (define slave PICs). On the iSBC 286/1ØA board, this parameter identifies levels 6 and 7 (IR6 and IR7) of the master PIC as being connected to interrupt sources supplying a vector.
4.	ØCØH ØØDH	Port Number for master PIC Data; ICW4. On the iSBC 286/1ØA board, this parameter selects not-special fully-nested mode, buffered mode (master), normal end of interrupt, and 8Ø86 mode.
5.	ØC2H ØFFH	Port Number for master PIC Data; OCW1. This parameter is the MASK Register format; it masks off all interrupts.
6.	ØC4H Ø19H	Port Number for slave PIC Data; ICW1. This parameter specifies level-triggered operation, cascaded operation, and ICW4 parameter required.
7.	ØC6H Ø28H	Port Number for slave PIC Data; ICW2. This parameter provides T3 through T7 of the interrupt vector (to be multiplied by 4).
8.	ØC6H ØØ7H	Port Number for slave PIC Data; ICW3 (cascade address). On the iSBC 286/1ØA board, this parameter locates the slave PIC (as being for IR7) on the master PIC input lines. Note that the 8274 does not require an ICW3 parameter to identify its location on the master PIC input lines; this is handled in hardware.

(continued)

Table 4-6. Parameter Sequence for PIC Initialization (continued)

Sequence	Port/ Data	Functions Performed in 8259A PIC
9.	ØC6H ØØ9H	Port Number for slave PIC Data; ICW4. On the iSBC 286/1ØA board, this parameter selects not-special fully-nested mode, buffered mode (slave), normal end of interrupt, and 8Ø86 mode for the slave PIC.
1Ø.	ØC6H ØFFH	Port Number for slave PIC Data; OCW1. This parameter is the MASK Register format; it masks off all interrupts.

4.5 PROGRAMMABLE INTERVAL TIMERS (WITH THE PIT DEVICE)

An 8254 Programmable Interval Timer (PIT) provides three 16-bit interval timers used to generate real-time interrupts and baud rates on the iSBC 286/1ØA board. Your options in configuring the PIT consist of changing jumpers and programming sequences. Each of these topics is discussed in greater detail in the following sections.

4.5.1 PIT JUMPER CONFIGURATIONS

When you receive your iSBC 286/1ØA board from the factory, the PIT counters are configured as follows:

- Counter Ø: regular-interval pulse generator clocked at 1.23 MHz.
- Counter 1: baud-rate generator providing a Transmit/Receive clock (TxC) for Channel B of the 8274 MPSC; clocked at 1.23 MHz.
- Counter 2: baud-rate generator providing a Transmit/Receive Clock (TxC) for Channel A of the 8274 MPSC; clocked at 1.23 MHz.

You can form most common baud rates with the board in its default configuration. If you need more baud rate flexibility, you can also use the 4.Ø MHz (SYS CLK) clock.

You can use Counter Ø as either a frequency generator (mode Ø) or as a rate generator (mode 2), and Counters 1 and 2 as square wave generators (mode 3).

To derive a specific output frequency (modes 2 and 3) or time interval (modes 1, 4, and 5), use the following formula:

$$\text{Output Frequency} = \frac{F}{N}$$

Where: F is the basic clock frequency on the PIT clock input
N is the count value needed for the output frequency

You can use Counter Ø as a frequency generator (mode Ø). In doing so, you must derive a specific output frequency. Derive your count value for Counter Ø by using the following formula:

$$\text{Count Value} = T \text{ times } F$$

Where: T is the desired interrupt time interval in seconds
F is the basic clock frequency on the PIT clock input

By programming the PIT for the longest possible count, you can create a maximum delay of 53.3 ms on Counter Ø. If this is not a long enough delay, you can reconfigure the jumpers to cascade the output from Counter Ø into the input of Counter 1. This provides a maximum delay of 28.41 seconds. However, if you choose to use Counter 1 as a cascaded timer rather than a source of Transmit clock for Channel B of the 8274 MPSC, you must ensure that you provide another clock source for the 8274 MPSC.

Table 4-7 lists the jumper functions for the PIT. Figure 4-2 shows the default configuration.

Table 4-7. PIT Jumper Connections

Jumper Connections	Functions Performed
E24,E25	Access to the SYS CLK signal, a 4.Ø MHz clock rate (with CLK at 8.Ø MHz)
E29	Clock input (CLKØ) pin for Counter Ø
E3Ø	Clock input (CLK2) pin for Counter 2
E31	Clock input (CLK1) pin for Counter 1
E34,E35,E36	1.23 MHz clock source for PIT
E26	Output signal from Counter Ø (CNTRØ)
E27	Output signal from Counter 2 (CNTR2)
E4Ø	Output signal from Counter 1 (CNTR1)
E39	Not used

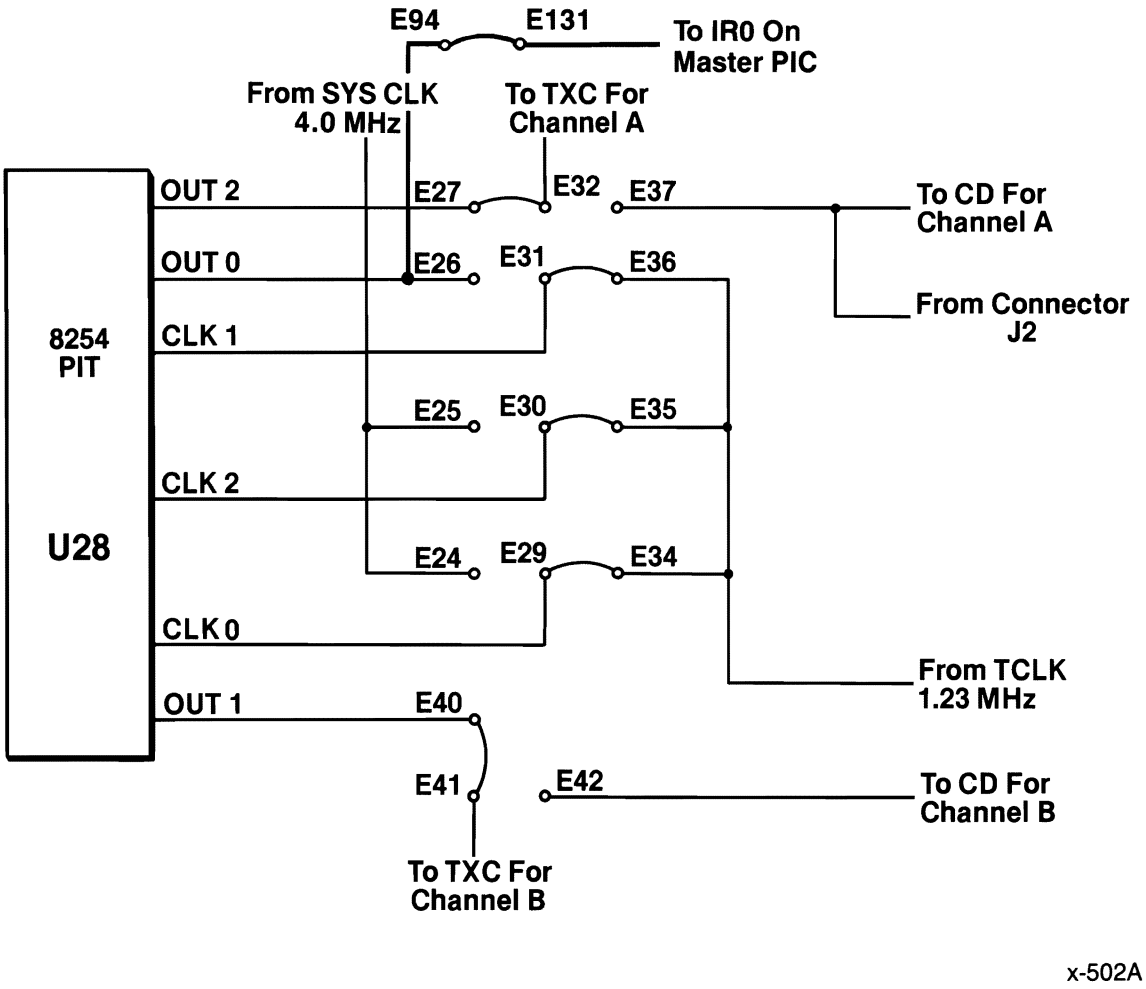


Figure 4-2. PIT Default Jumper Configuration

4.5.2 PIT PROGRAMMING

In the default configuration, the iSBC 286/1ØA board expects initialization for Counter Ø to Mode Ø, Counter 1 to Mode 3, and Counter 2 to Mode 3. You can reprogram Counter Ø for Mode 2 operation without changing the jumper configuration on the board.

You program the 8254 PIT by using the even I/O port addresses between ØØDØH and ØØD6H as listed in Table 4-8.

The 8254 PIT is very flexible about the order in which you issue the sequence of parameters. You can issue parameters in any sequence so long as you adhere to two conventions:

1. Always write a Control Word parameter to a counter before writing the count value parameter(s) to the counter.

2. The byte(s) of the count value parameter must comply with the byte sequence specified in the Control Word parameter (for example, LSB only, MSB only, or LSB followed by MSB).

NOTE

After you load the Control Word for a specific counter, you can load and reload count values without issuing another Control Word.

Typical PIT-generated baud rates for the 8274 MPSC device are shown in Table 1-1.

Table 4-8. Port Addresses for the 8254 PIT Device

I/O Address	Device	Operation	Function Performed
ØØDØH	PIT Counter Ø	Byte Read: Byte Write: Word:	LSB or MSB of count value LSB or MSB of count value N/A
ØØD2H	PIT Counter 1	Byte Read: Byte Write: Word:	LSB or MSB of count value LSB or MSB of count value N/A
ØØD4H	PIT Counter 2	Byte Read: Byte Write: Word:	LSB or MSB of count value LSB or MSB of count value N/A
ØØD6H	PIT Control Word Register	Byte Read: Byte Write: Word:	N/A Control Word Register Parameter N/A

4.5.3 PIT PROGRAMMING EXAMPLE

Table 4-9 contains a programming sequence that issues the required parameter to initialize the PIT device.

Counter Ø can be initialized for operation in any mode. Initialize it for operation in Mode 2 (time-tick generator) by writing a value of 34H into the Control Word Register, or initialize for Mode Ø (interrupt on terminal count) by writing a value of 36H into the Control Word Register.

Table 4-9. PIT Programming Sequence

Sequence	Port/ Data	Functions Performed in 8254 PIT
1.	ØDØH	Port Number for Counter Ø
	Ø3ØH	Command: select Counter Ø, Read/Write LSB then MSB, Mode Ø, 16-bit binary counter
	ØFFH	LSB of count value
	ØFFH	MSB of count value
2.	ØD2H	Port Number for Counter 1
	Ø76H	Command: select Counter 1, Read/Write LSB then MSB, Mode 3, 16-bit binary counter
	ØFFH	LSB of count value
	ØFFH	MSB of count value
3.	ØD4H	Port Number for Counter 2
	ØB6H	Command: select Counter 2, Read/Write LSB then MSB, Mode 3, 16-bit binary counter
	ØFFH	LSB of count value
	ØFFH	MSB of count value

Note: The count value of FFFF is intended only as an example.

4.6 iSBX™ INTERFACES – J5 & J6

The iSBC 286/1ØA board contains two 36/44-pin iSBX bus connectors for 8- or 16-bit I/O expansion. The connectors are labeled J5 (iSBX 2) and J6 (iSBX 1). The following sections provide a description of the interfaces, programming information, and configuring information.

4.6.1 iSBX™ BUS DESCRIPTION

The iSBX bus interfaces comply with the INTEL iSBX BUS SPECIFICATION as follows:

D16/16 I

- The "D16/16" means support for either an 8- or 16-bit expansion module.
- The lack of a "D" means that the board does not support DMA operations to iSBX bus connectors.
- The "I" means support of interlocked read and write operations (using MWAIT*).

Refer to the INTEL iSBX BUS SPECIFICATION for a description of the pin assignments and AC/DC characteristics of the J5 and J6 Connectors.

4.6.2 iSBX™ INTERFACE CONFIGURATIONS

You can configure the iSBX bus interfaces via programming and jumper configurations:

- Select either 8- or 16-bit interface operation for each iSBX bus interface. You do this when you select a type of device to interface to the iSBX connectors (whether an 8- or 16-bit device).

- If required, configure the four jumper pins that provide access to the option signal lines (OPTØ and OPT1) that can be used for passing interrupt and clock signals between the MULTIMODULE boards and the iSBC 286/1ØA board. The jumpers are described further in Section 4.6.2.2

4.6.2.1 Interface Addressing

If you attach a MULTIMODULE board to either connector, the iSBC 286/1ØA board reserves all I/O port addresses in the range of ØØ8ØH through ØØBFH as on-board addresses for the iSBX bus connectors.

If you do not install a MULTIMODULE board, the I/O address space is not reserved as on-board. In this case, you can use the addresses as MULTIBUS I/O address space.

Table 4-1Ø lists all of the I/O port addresses for the board. Notice that the port addresses are listed for two configurations: an iSBC 286/1ØA board with an 8-bit MULTIMODULE board, and an iSBC 286/1ØA board with a 16-bit MULTIMODULE board. You can find details on the functions available at each I/O port address by referring to the manual for the specific MULTIMODULE board that you are using.

Suppose, for example, the 8-bit iSBX 351 Serial MULTIMODULE board is installed in J5 (iSBX 2). To program the MULTIMODULE's PIT Counter Ø requires the address ZØ or Z8 (Z designates the base address activating MCS1* - ØØB in this case), as found in the MULTIMODULE's Hardware Reference Manual. Either address, ØØBØ (or ØØB1) or ØØB8 (or ØØB9), would be correct.

Table 4-1Ø. I/O Port Addresses for iSBX™ Connectors

Port addresses for 286/1ØA board with an 8-bit MULTIMODULE board

On Connector J6 (SBX1)		On Connector J5 (SBX2)
ØØ9F or ØØ9E		ØØBF or ØØBE
ØØ9D or ØØ9C		ØØBD or ØØBC
ØØ9B or ØØ9A		ØØBB or ØØBA
ØØ99 or ØØ98	MCS1* Active	ØØB9 or ØØB8
ØØ97 or ØØ96		ØØB7 or ØØB6
ØØ95 or ØØ94		ØØB5 or ØØB4
ØØ93 or ØØ92		ØØB3 or ØØB2
ØØ91 or ØØ9Ø		ØØB1 or ØØBØ
ØØ8F or ØØ8E		ØØAF or ØØAE
ØØ8D or ØØ8C		ØØAD or ØØAC
ØØ8B or ØØ8A		ØØAB or ØØAA
ØØ89 or ØØ88	MCSØ* Active	ØØA9 or ØØA8
ØØ87 or ØØ86		ØØA7 or ØØA6
ØØ85 or ØØ84		ØØA5 or ØØA4
ØØ83 or ØØ82		ØØA3 or ØØA2
ØØ81 or ØØ8Ø		ØØA1 or ØØAØ

Port addresses for 286/1ØA board with a 16-bit MULTIMODULE board

On Connector J6 (SBX1)		On Connector J5 (SBX2)	
ØØ8F	ØØ8E	ØØAF	ØØAE
ØØ8D	ØØ8C	ØØAD	ØØAC
ØØ8B	ØØ8A	ØØAB	ØØAA
ØØ89	ØØ88	ØØA9	ØØA8
ØØ87	ØØ86	ØØA7	ØØA6
ØØ85	ØØ84	ØØA5	ØØA4
ØØ83	ØØ82	ØØA3	ØØA2
ØØ81	ØØ8Ø	ØØA1	ØØAØ
MCS1* Active	MCSØ* Active	MCS1* Active	MCSØ* Active

4.6.2.2 Jumper Configurations

The iSBC 286/1ØA board contains four jumper pins (E142, E148, E188, and E189) that provide access to the two option signals (OPTØ and OPT1) for each iSBX connector, as listed in Table 4-11.

Table 4-11. iSBX™ Jumper Options

Jumper Number	Connector Number	Signal Names and Functions
E142	J6 (SBX1)	Option Line Ø (OPTØ)
E148	J6 (SBX1)	Option Line 1 (OPT1)
E188	J5 (SBX2)	Option Line Ø (OPTØ)
E189	J5 (SBX2)	Option Line 1 (OPT1)

4.7 MULTIBUS® INTERFACE - P1

The iSBC 286/1ØA board contains an 86-pin MULTIBUS connector (P1) for interfacing to other system's functions. Memory accessed off-board via the MULTIBUS interface is explained in Section 4.12.8. The following sections describe the interface and how you can change its operation.

Refer to the INTEL MULTIBUS SPECIFICATION for a description of the pin assignments and the AC/DC characteristics of the P1 Connector interface.

4.7.1 MULTIBUS® INTERFACE DESCRIPTION

The MULTIBUS interface on the iSBC 286/1ØA board complies with the IEEE 796 Microcomputer Systems Bus Standard, as follows:

MASTER D16 M24 I16 VØ2 E L

- The "MASTER" means that the board supports either master or slave operation on the MULTIBUS interface.
- The "D16" means either an 8- or 16-bit data path.
- The "M24" means a 24-bit memory address path.
- The "I16" means either an 8- or 16-bit I/O address path.
- The "VØ2" means that the board supports two cycle bus-vectored interrupt requests.
- The "E" means that the board supports edge-level triggered interrupt sensing.
- The "L" means that the board supports level triggered interrupt sensing.

4.7.2 MULTIBUS® INTERFACE CONFIGURATIONS

By installing or removing the jumpers listed in Table 4-12, you can control four features of the MULTIBUS interface: the MULTIBUS lock, the bus clock, the bus priority resolution, and the bus release signals.

Table 4-12. MULTIBUS® Interface Jumpers

Jumper	Signal Name	Description
E253-E254§	BCLK* Bus clock	Provides a common Bus Clock from the iSBC 286/1ØA board to all MULTIBUS boards.
E246-E247§	CCLK* Constant clock	Provides a common Constant Clock from the iSBC 286/1ØA board to all MULTIBUS boards (CCLK is 18Ø degrees out of phase with BCLK).
E255-E256§	LOCK* Bus Lock	Allows the iSBC 286/1ØA board to generate a LOCK* signal to the MULTIBUS interface. LOCK* prevents another master from gaining control of the MULTIBUS interface.
E271-E272§	BPRO* Bus Priority Out	Active only when the iSBC 286/1ØA board is passing control of the MULTIBUS interface to another board (useful only in serial priority resolution schemes and removed in parallel priority schemes).
E235 E236-E237§	CBRQ* Common Bus Request	Input or output depending on the Arbiter's release mode. As input, indicates another arbiter is requesting MULTIBUS. As output, indicates this Arbiter is requesting MULTIBUS.
E233-E234	ALWAYS*/CBQLCK* Always Release or Common Bus Request Lock	This pin is read at reset to be either the ALWAYS* (if tied low) strapping option or the CBQLCK* (if tied high) control input.

Note: § identifies the default jumper configuration.

The bus clock jumpers allow the iSBC 286/1ØA board to provide two clocks that provide timing for the bus contention and synchronization logic on other master boards on the MULTIBUS interface. By removing jumpers E246-E247, and E253-E254, you can allow another master board to provide the system timing (BCLK* and CCLK*) signals on the MULTIBUS interface. Ensure, however, that you have only one device driving each MULTIBUS interface clock signal.

The bus priority resolution jumpers allow you to select the priority level that your iSBC 286/1ØA board uses when it arbitrates for use of the MULTIBUS interface. By reconfiguring the jumpers, you can change the priority level for the iSBC 286/1ØA board in acquiring control of the MULTIBUS interface.

The bus release jumpers allow you to define the conditions under which the iSBC 286/1ØA board releases control of the MULTIBUS interface to another bus master. Table 4-13 lists the three release modes of the arbiter and their jumper configurations.

Table 4-13. MULTIBUS® Release Modes

Release Mode	Jumper Connect	Description
1	E233-E234§	The Bus Arbiter releases the bus at the end of each transfer cycle
2	E233-nc	The Bus Arbiter retains the bus until: • a higher-priority Arbiter requests the bus (BPRN* high) • a lower priority Arbiter requests the bus (CBRQ* low)
3	E233†	The Bus Arbiter retains the bus until: • a higher-priority Arbiter requests the bus, driving BPRN* high (CBRQ* low ignored)

Note: † Pin E233 must be dynamically controlled to be high during RESET then low for the required duration. Reference Intel's MICROSYSTEM COMPONENTS HANDBOOK for detailed information.
§ Identifies the default jumper configuration.
nc = no connection.

In mode 1 (the default configuration), the arbiter releases the bus at the end of each transfer cycle. For multiple transfers, this requires the arbiter to acquire and release the bus for each transfer, even if another arbiter is not requesting the bus.

In mode 2, the arbiter releases the bus when another arbiter of higher or lower priority requests it. The major difference between modes 1 and 2 is mode 2 does not waste time acquiring and releasing the bus for multiple transfers.

In mode 3, the arbiter releases the bus only to an arbiter with higher priority. The 82289 Arbiter has the capability of switching between mode 2 and 3 during operation.

4.8 PARALLEL I/O INTERFACE (WITH THE PPI DEVICE) - J1

The parallel I/O interface on the iSBC 286/1ØA board (connector J1) provides a Centronics-compatible printer interface in its default configuration. You can change the jumper configuration, the I/O cabling, and the operation of the 8255A Programmable Peripheral Interface (PPI) device to redefine the interface to suit your needs.

The parallel I/O port reconfiguration involves jumper configurations and initialization parameters that define the

- Direction of the Port A transceiver
- Function of the general-purpose inputs on Port B
- Use of the interrupt indication from Port C

Each of these topics is discussed in greater detail in the following sections.

4.8.1 PARALLEL INTERFACE DESCRIPTION

The 8255A PPI device controls the operation of the J1 Connector interface. The PPI device provides a total of 24 configurable I/O bits, although the design of the iSBC 286/1ØA board restricts usage on some of the bits. Refer to Intel's MICROSYSTEM COMPONENTS HANDBOOK for more information on the 8255A PPI device.

4.8.1.1 Interface Pin Assignments

Table 4-14 lists the pin assignments for the Connector J1 interface and shows how the pin assignments compare to the Centronics interface standard for line printers.

Table 4-14. Connector J1 Pin Assignments

Pin Number		Signal Function	Pin Number		Signal Function
J1	Centronics Std.		J1	Centronics Std.	
1	19	Ground	2	1	Data Strobe
3	2Ø	Ground	4	2	Data Bit Ø
5	21	Ground	6	3	Data Bit 1
7	22	Ground	8	4	Data Bit 2
9	23	Ground	1Ø	5	Data Bit 3
11	24	Ground	12	6	Data Bit 4
13	25	Ground	14	7	Data Bit 5
15	26	Ground	16	8	Data Bit 6
17	27	Ground	18	9	Data Bit 7
19	28	Ground	2Ø	1Ø	Acknowledge
21	29	Ground	22	11	Busy
23	3Ø	No Connect	24	12	Error
25	31	No Connect	26	13	No Connect

4.8.1.2 Interface Drive Characteristics

Table 4-15 presents the DC current driving and sinking limits for the parallel interface at Connector J1.

Table 4-15. Connector J1 Interface DC Characteristics

Parameter	Conditions	Minimum	Maximum	Units
V_{IL}		-	Ø.8	V
V_{IH}		2.Ø	-	V
I_{IL}	V_{IN}=Ø.4V	-	-5.Ø	mA
I_{IH}	V_{IN}=2.4V	-	-1.Ø	mA
V_{OL}	I_{OL}=16mA	-	.45	V
V_{OH}	I_{OH}=-4ØØuA	2.4	-	V

4.8.1.3 Interface Cabling

The iSBC 286/1ØA board line printer interface meets the pinout and DC characteristics of the Centronics interface standard, so you can use a 26-conductor flat cable with a standard Centronics interface connector (Amp #552931-1 or equivalent) to connect directly to the J1 edge connector.

NOTE

When installing the cable onto the edge connector, ensure that pin 2 of the edge connector aligns with the pin 1 marking on the connector housing. As a result, pin 2 of the housing should align with pin 1 of the edge connector.

4.8.2 PPI JUMPER CONFIGURATIONS

The default configuration contains jumper connections that assume PPI device operation in Mode Ø, with Ports A and C as outputs and Port B as an input. Figure 4-3 shows this default configuration.

Table 4-16 lists the available jumper options. Seven jumper options control the general-purpose input signals to Port B. Four jumper options control the direction of the transceiver on Port A: tie the direction control high, tie the direction control low, control the direction through bit PC4, or control the direction through pin J1-22.

4.8.3 PPI DEVICE PROGRAMMING

You can use the PPI device for a function other than the default Centronics-compatible line printer configuration by redefining the operation of the PPI device. However, you cannot change operation of Port C; some of the bits of Port C are dedicated to performing special on-board functions such as NMI mask control, bus control override, edge interrupt sense reset, and line printer data strobe control.

4.8.3.1 PPI Port Addresses

You can use four I/O port addresses to program the operation of the PPI device. Table 4-17 lists the port addresses and the functions performed by each.

Table 4-16. Parallel I/O Jumper Options

Jumper Number	Description
E53 E54 E55 E56 E45,46,47	General Purpose Input Ø General Purpose Input 1 General Purpose Input 2 General Purpose Input 3 Ground for GP input lines User-defined input signals to the PPI device.
E48	Line printer interrupt request signal to the interrupt matrix: 1 = interrupt active Ø = interrupt inactive
E2 E2-E1 E2-E3 E2-nc§ E2-E4	Direction control for the transceiver on Port A of the PPI device, as follows: Use an external signal from J1-22 to control the direction of Port A Operate Port A as an input port Operate Port A as an output port Control direction of Port A through bit 4 of Port C: Bit 4 = 1 for output Bit 4 = Ø for input

Notes: § identifies the default jumper configuration.
nc means not connected.

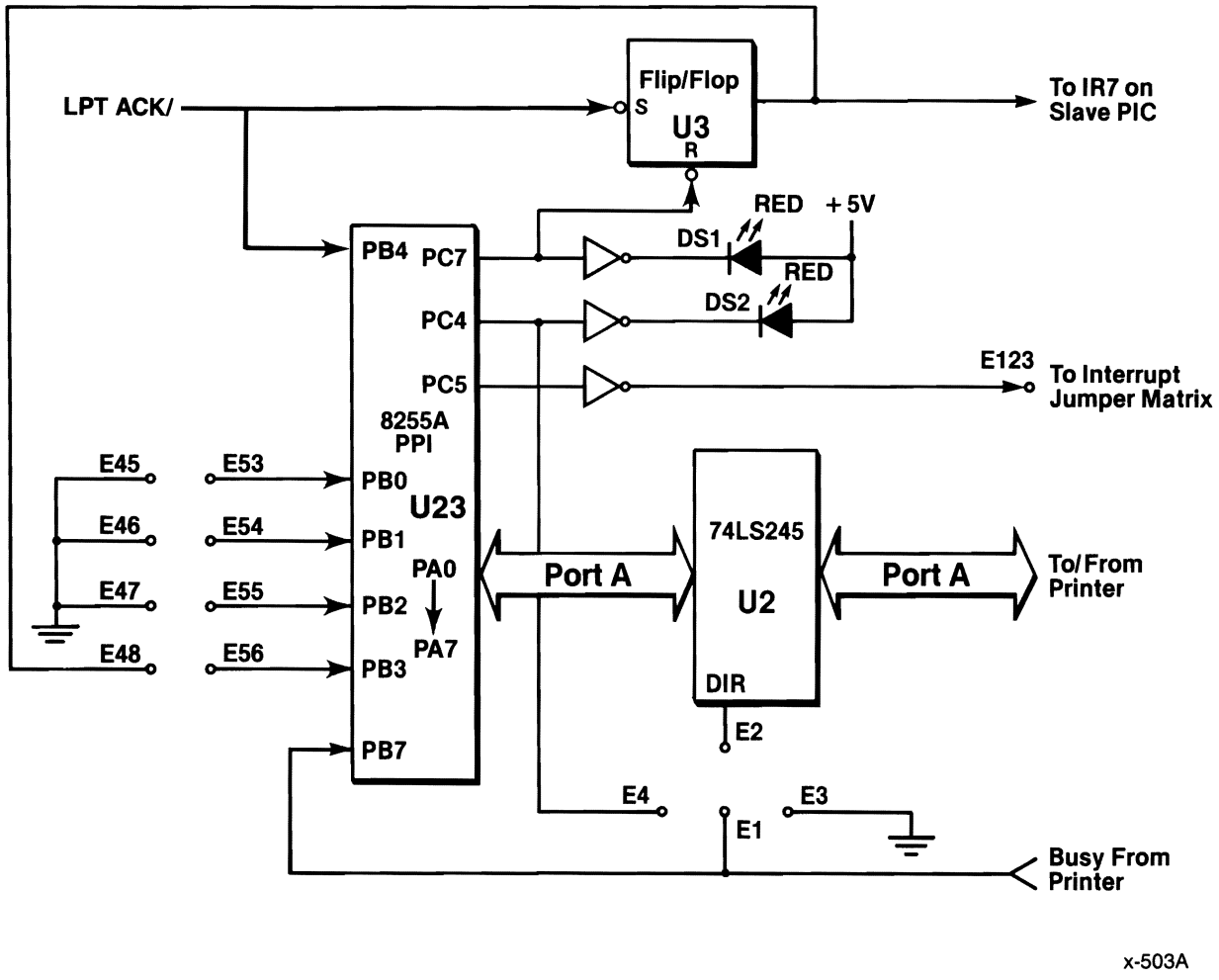


Figure 4-3. PPI Default Jumper Configuration

4.8.3.2 PPI Initialization

As shipped, the board requires a power-up initialization routine that configures the PPI device for Mode Ø operation; that is, Ports A and C are output ports and Port B is an input port. This type of configuration requires a Mode Word definition format of 82H.

Table 4-17. PPI Port Addresses

I/O Address	Device	Operation	Function Performed
ØØC8H	PPI Port A	Byte Read: Byte Write: Word Write:	Read back output data Port A Special function (see following note)
ØØCAH	PPI Port B	Byte Read: Byte Write: Word Write:	Port B N/A (default) Special
ØØCCH	PPI Port C	Byte Read: Byte Write: Word Write:	Read back output data Port C Special
ØØCEH	PPI Control	Byte Read: Byte Write: Word Write:	N/A Control Special

NOTE

Table 4-17 lists a word write operation to port addresses ØØC8H to ØØCEH as "special." Whenever you issue a word write operation to those addresses, you switch the iSBC 286/1ØA board from 2Ø- to 24-bit addressing.

It is risky to write to an output port or to the control port in an attempt to switch modes. The port will accept the signal also as data. We recommend writing to Port B, defined as input, for the mode switch.

You can change the direction of data transfer of the transceiver on Port A by reconfiguring the jumpers. However, you must also reinitialize the PPI device with a different Mode Word; a Mode Word of 92H makes the port operate as an input port.

Table 4-18 contains the sequence of parameters required to initialize the 8255A PPI device for operation in the default board configuration.

Table 4-18. Parameter Sequence for PPI Device Initialization

Sequence	Port/ Data	Functions Performed in 8255A PPI
1.	ØCEH Ø82H	Port Number for control of PPI Data; PPI configuration (Port A out, Port B in, Port C out)
2.	ØCCH ØØAH	Port Number for Port C of PPI Data; Port C default configuration

4.8.4 BIT ASSIGNMENTS FOR PPI SIGNALS

In the default configuration, the iSBC 286/1ØA board uses each bit position of each I/O port for specific functions. Table 4-19 lists the bit assignment for each bit of the three I/O ports and describes the functions.

Bit positions accessible via jumper posts may be reprogrammed. However, use caution in changing the operation of Port C of the PPI device; it performs some dedicated functions that you may need:

- Port C, Bit 1 - Bus Control Override provides programmable control of the MULTIBUS LOCK feature. By programming a Ø into Port C bit 1, you can place a permanent LOCK condition into the 82289 Bus Arbiter. Once the iSBC 286/1ØA board obtains control of the MULTIBUS interface, it then retains exclusive access until Port C, bit 1 goes high.

- Port C, Bit 3 - NVRAM Enable provides a special signal on jumper pins E172 (dual-port sockets), E66 (local U4Ø/U75), and E81 (local U41/U76) that is required to operate NVRAM devices.

- Port C, Bit 5 - Bus Drive provides a signal that you can use to drive an interrupt signal (INTØ* through INT7*) to the MULTIBUS interface.

Table 4-19. PPI Bit Assignments (Default Configuration)

Port	Direction	Bit	Assigned Function	Signal On Pin
Port A	Output	Ø	Line Printer Data Bit Ø	LPT DØ on J1-4
		1	Line Printer Data Bit 1	LPT D1 on J1-6
		2	Line Printer Data Bit 2	LPT D2 on J1-8
		3	Line Printer Data Bit 3	LPT D3 on J1-1Ø
		4	Line Printer Data Bit 4	LPT D4 on J1-12
		5	Line Printer Data Bit 5	LPT D5 on J1-14
		6	Line Printer Data Bit 6	LPT D6 on J1-16
		7	Line Printer Data Bit 7	LPT D7 on J1-18
Port B	Input	Ø	General Purpose Input Ø	E53
		1	General Purpose Input 1	E54
		2	General Purpose Input 2	E55
		3	General Purpose Input 3	E56
		4	Line Printer Acknowledge	LPT ACK* on J1-2Ø
		5	Power Fail Sense	PFSN* on J4-13
		6	Line Printer Error	LPT ERROR* on J1-24
		7	Line Printer Busy	LPT BUSY* on J1-22
Port C	Output	Ø	Line Printer Data Strobe (Active Low)	LPT DSTB* on J1-2
		1	Bus Control Override Ø = Hold MULTIBUS Interface 1 = Release MULTIBUS Interface	OVERRIDE
		2	NMI Mask 1 = NMI Disabled Ø = NMI Enabled	NMI MASK
		3	Dual Function 1 = Non-Volatile RAM Enable Ø = Clear Timeout Interrupt	
		4	Dual Function 1 = Red LED DS2 On Ø = Red LED DS2 Off and Clear Edge Sense Flip-flop	CLR EDGE1*
		5	Bus Drive Ø = Drive MULTIBUS Interrupt	BUS DRIVE* to E123
		6	Serial Channel Operation 1 = Channel A Loopback Ø = Channel A On-line	SER LB
		7	Dual Function 1 = Red LED DS1 On Ø = Red LED DS1 Off and Clear Line Printer Acknowledge flip-flop	LPT ACK* on E48

4.9 SERIAL I/O INTERFACES (WITH THE MPSC DEVICE) – J2 & J3

The iSBC 286/1ØA board provides two 26-pin serial I/O interfaces, one at Connector J2 and one at Connector J3. The board provides several configuration options on each interface. The following sections present information for configuring the serial interfaces.

Baud rate information for the serial ports is located in Section 4.5 and Table 1-1.

NOTE

After a power-up reset, you must provide a software reset to both Channels A and B of the 8274 MPSC.

4.9.1 SERIAL JUMPER INFORMATION

Table 4-2Ø lists the jumper options that you can use with the serial interfaces at Connectors J2 and J3. Channel A of the 8274 MPSC operates Connector J2 and Channel B operates Connector J3.

Table 4-2Ø. Serial I/O Jumper Options

Jumpers	Descriptions
E4Ø-E41 §	Transmit Clock to Channel B of the 8274 from PIT Counter 1
E41-E42	Transmit Clock to Channel B of the 8274 from an external source using the DTR signal line
E39-E41	Test purposes only
E28-E33 §	Use the Transmit Clock to Channel B of the 8274 as the source for the Receive Clock for Channel B
E33-E38	Receive Clock to Channel B of the 8274 from an external source using the TxC signal line
E27-E32 §	Transmit Clock to Channel A of the 8274 from PIT Counter 2
E32-E37	Transmit Clock to Channel A of the 8274 from an external source using DTR (RS232C) or TR (RS422A)
E15-E16 §	Receive Clock for Channel A of the 8274 sourced from Transmit clock from Channel A
E14-E15	Receive clock for Channel A of the 8274 from an external source using TxC (RS232C) or TT (RS422A)
E2Ø-E21	Enable use of the Channel A interface in a multidrop application
E18-E19	Frame ground or shield on pin 2 of Connector J2

Note: § identifies the default jumper configuration.

4.9.2 8274 MPSC CHANNEL A – CONNECTOR J2

Figure 4-4 shows the serial interface options on the iSBC 286/1ØA board. Connector J2 is configured to operate as a Data Communications Equipment (DCE) device with an RS232C interface, but can be reconfigured for RS422 operation.

4.9.2.1 Connector J2 Description

Table 4-21 lists the pin assignments and signals on each pin of Connector J2, if reconfigured for an RS422A/449 interface. Table 4-23 lists the pin assignments and signals for the connector in the default RS232C interface configuration.

Refer to the EIA Standard RS232C, the EIA Standard RS422A and the component data sheets for the 1488, 3486, and 3487 line drivers for more information.

4.9.2.2 Connector J2 Configurations

Connector J2 operates as a DCE device with an RS232C interface in the default configuration. As such, socket U13 contains the DIP header (DCE mode configuration), U15 is empty, and RP5 is placed with pin 1 closest to the MULTIBUS interface connector. You can convert the interface to one of four other operating modes:

- RS422A/449 DCE (Data Communications Equipment) mode operation
- RS232C DTE (Data Terminal Equipment) mode operation
- Multidrop application, RS422A/449 DCE (Appendix B)
- Internal loopback operation

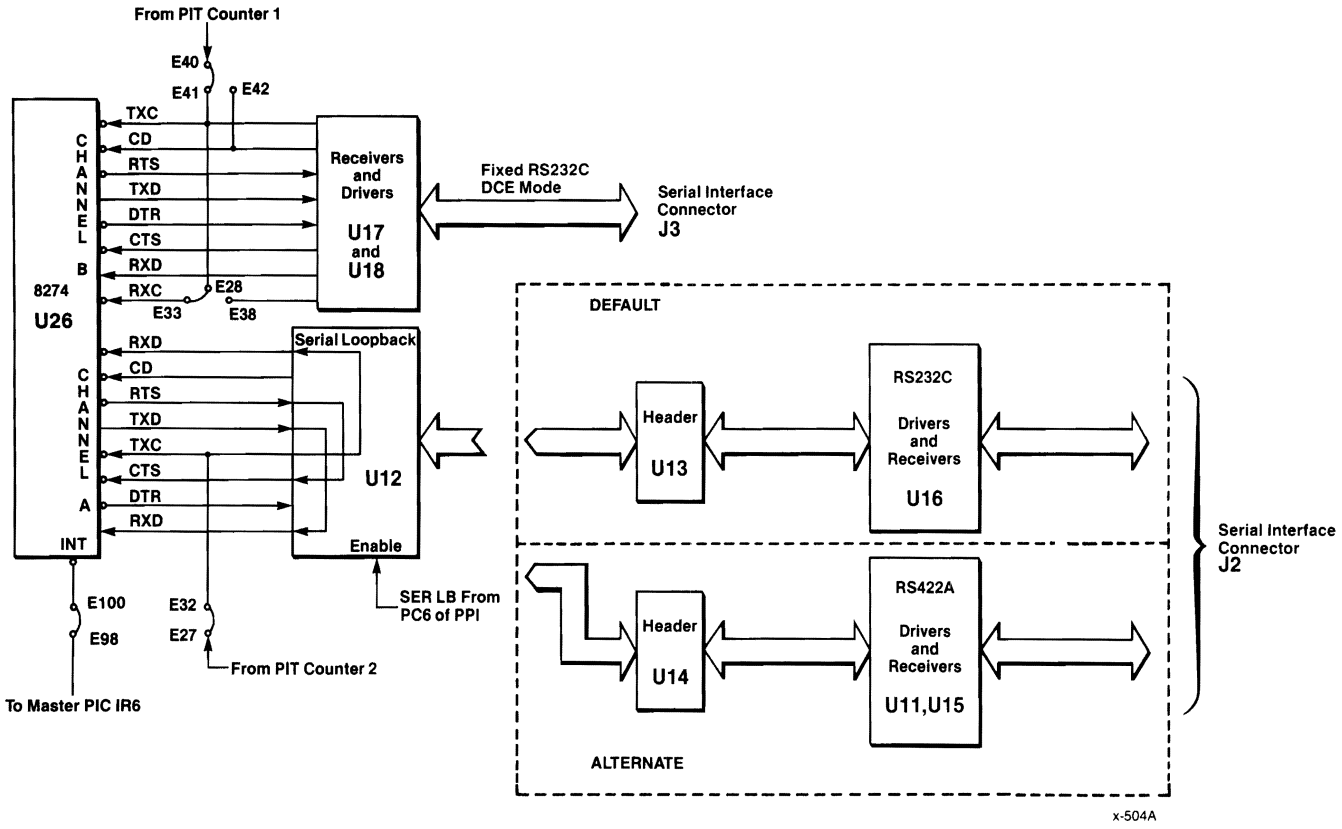


Figure 4-4. Serial I/O Interface Options

Table 4-21. Pin Assignment for Connector J2 - RS422A/449 Interface

J2 Pin Number	RS422A Pin Number	RS449 Signal Name	RS449 Signal Function
1	2Ø	RC	Receive Common
2	1	Shield	Shield
3	21	TT (B)	Terminal Timing (TT)
4	2	---	---
5	22	SD (B)	Send Data
6	3	TT (A)	Terminal Timing (TT)
7	23	---	---
8	4	SD (A)	Send Data
9	24	RD (B)	Receive Data
1Ø	5	---	---
11	25	RS (B)	Request To Send
12	6	RD (A)	Receive Data
13	26	RT (B)	Receive Timing
14	7	RS (A)	Request To Send
15	27	CS (B)	Clear To Send
16	8	RT (A)	Receive Timing
17	28	---	---
18	9	CS (A)	Clear To Send
19	29	DM (B)	Data Mode
2Ø	1Ø	---	---
21	3Ø	TR (B)	Terminal Ready
22	11	DM (A)	Data Mode
23	31	---	---
24	12	TR (A)	Terminal Ready
25	32	---	---
26	13	---	---

Note: All unlisted signals are not supported by the board in the default configuration.

Later sections provide a configuration sequence for each of these operating modes. In making a choice in the type of operation, you must make some tradeoffs in cost, performance, or ease of use.

Table 4-22 provides a comparison of the RS232C and the RS422A/449 interfaces.

Consider your application requirements when deciding on either Data Terminal Equipment (DTE) or Data Communications Equipment (DCE) mode operation for Connector J2. Figure 4-5 is a block diagram showing the differences between the two; DTE typically feeds a DCE-type modem.

Select DTE mode if the board operates as a terminal device; select DCE mode if the board operates as a processor device. The DCE device transmits data to and receives data from the DTE device.

Table 4-22. Serial I/O Interface Configuration Comparison

Feature Description	Comparison	
	RS232C	RS422/449
Number of signal lines required to enact the interface protocol	x	2x
Communication cable lengths	5Ø feet (max.)	Up to 4ØØØ feet
Voltages required to operate the interface	+12 volts -12 volts ground	+5 volts ground

4.9.2.2.1 RS422A/449 DCE CONFIGURATION SEQUENCE. To reconfigure the J2 interface to RS422A/449 DCE operation, do the following steps:

1) Move the DIP header from socket U13 to U14. Socket U13 should now be empty.

2) Ensure that the DIP header is configured for DCE operation, as shown in Figure 4-6.

3) Install a 3487 device at IC socket U15.

4) Remove RP5, turn it 18Ø degrees, and reinstall it in the same SIP socket. The location of RP5 is shown in Figure 4-7. At this point, you should have RP5 installed onto the board so that pin 1 is closest to the J2 connector on the board.

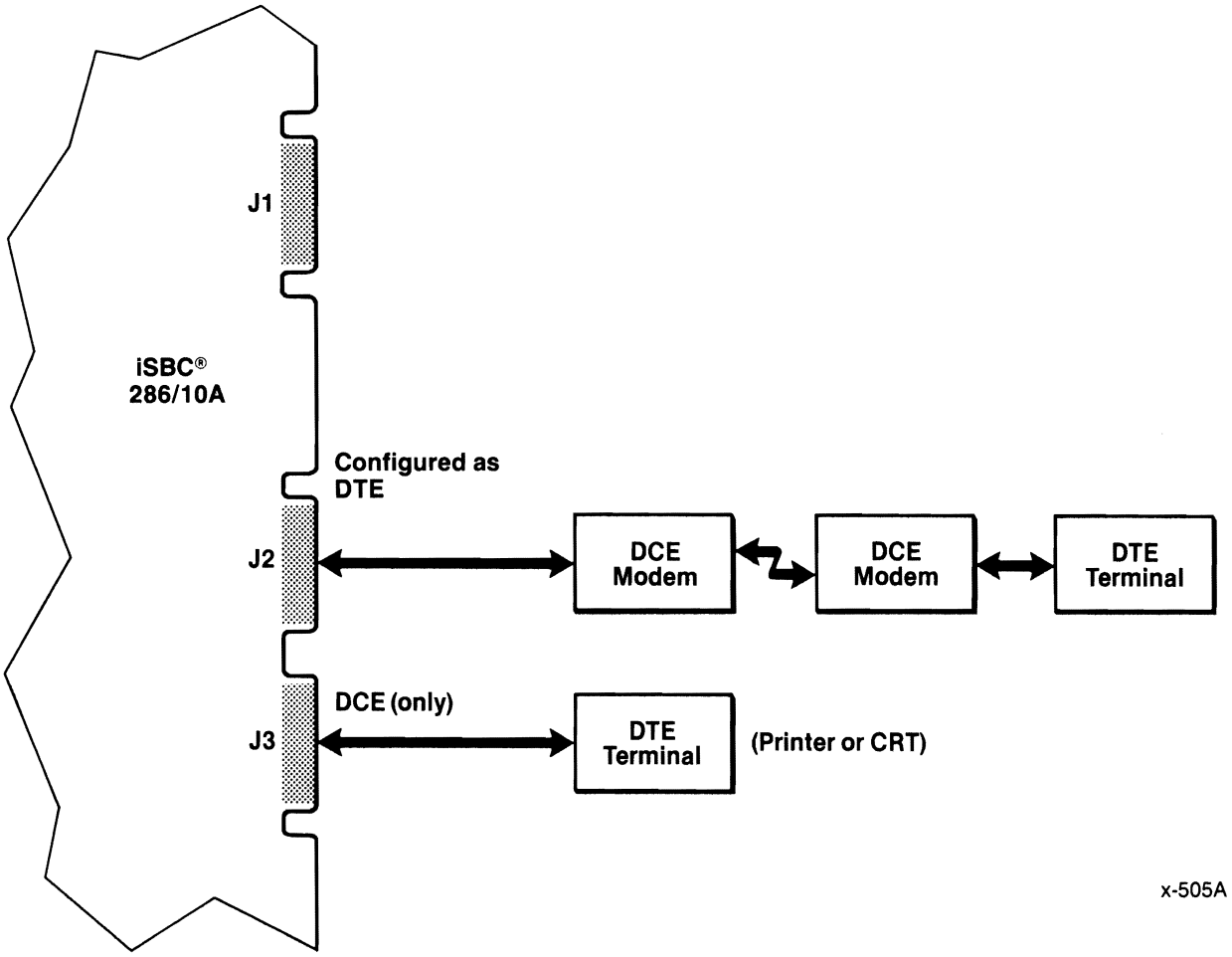


Figure 4-5. DCE and DTE Interface Block Diagram

4.9.2.2.2 RS232C DTE CONFIGURATION SEQUENCE. To reconfigure the J2 interface from the default DCE mode to DTE, do the following steps:

1) Remove the DIP header from socket U13 and discard it. Socket U13 should now be empty.

2) Provide another DIP header configured for RS232C DTE operation, as shown in Figure 4-6. Install it into U13.

3) Ensure that socket U15 is empty; there may be a 3487 device in it if the interface was used for an RS422A/449 interface.

4) Remove RP5, turn it 18Ø degrees, and reinstall it in the same SIP socket. The location of RP5 is shown in Figure 4-7. Install RP5 so that pin 1 is closest to the P1 MULTIBUS connector on the board. The effect of rotating RP5 is shown in Figure 4-8.

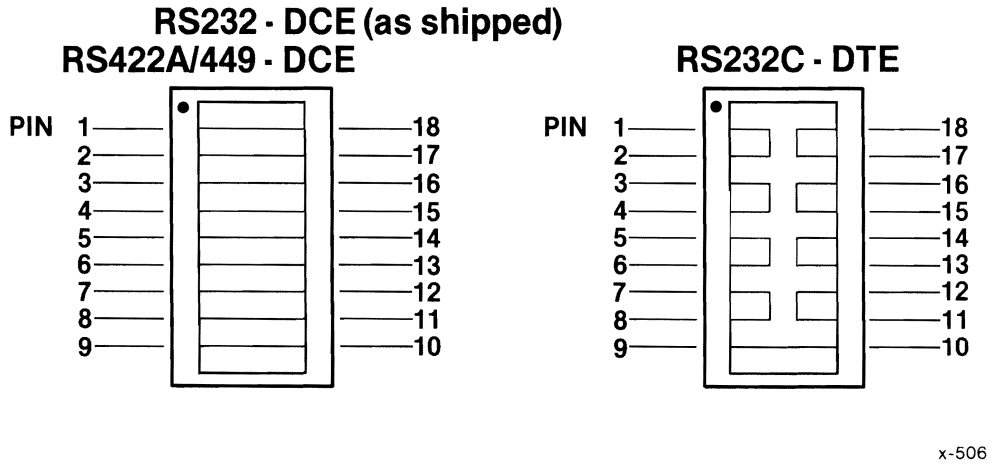


Figure 4-6. DIP Header for DCE and DTE Operation

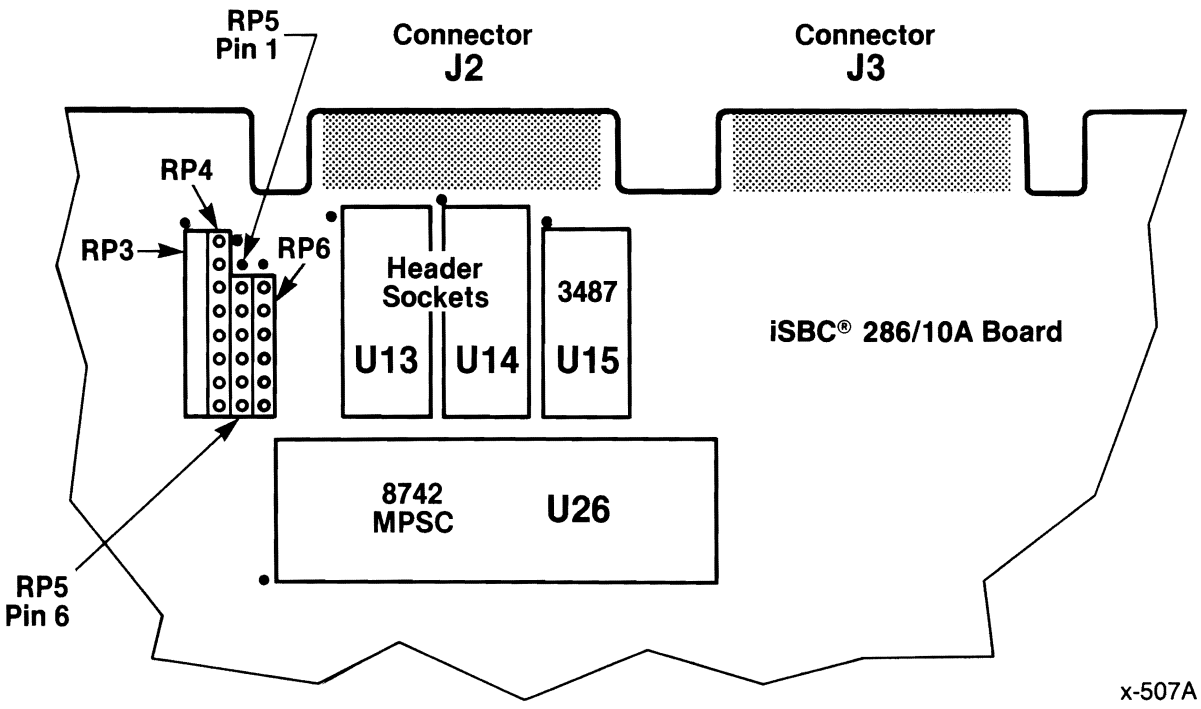


Figure 4-7. RP5 Location

4.9.2.2.3 LOOPBACK CONFIGURATION SEQUENCE. The iSBC 286/1ØA board contains a loopback feature that functions as a programmable diagnostic tool to use in isolating application problems in the serial interface at Connector J2.

In loopback operation, the board takes three TTL-level signals from Channel A of the 8274, routes them through a multiplexer, and returns them to the 8274 MPSC as different signals. The input and output signals from the 8274 are as follows:

8274 Output		8274 Input
RTS	becomes	CTS
TxC	becomes	RxC
TxD	becomes	RxD

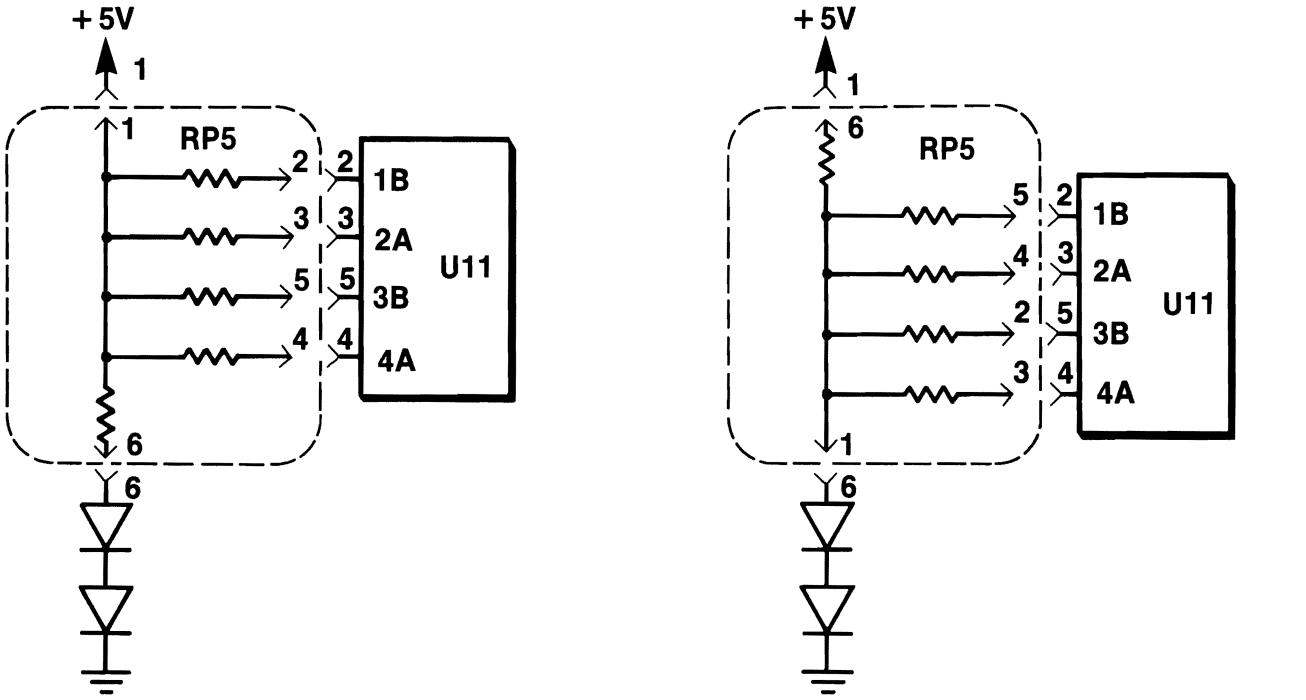


Figure 4-8. RP5 Configurations

After a power-up or system reset, the iSBC 286/1ØA board automatically places Channel A into loopback mode operation and writes a 1 into bit 6 of Port C of the 8255A PPI device. You disable operation of the loopback by writing a Ø into bit 6 of Port C after initializing the 8255A PPI device. This makes the 8255A PPI deactivate a signal (SER LB) that controls operation of the loopback multiplexer.

Do not activate the loopback while using the interface for transferring data.

4.9.3 8274 MPSC CHANNEL B - RS232C INTERFACE - CONNECTOR J3

Connector J3 is default configured as a DCE device with an RS232C interface.

4.9.3.1 Connector J3 Description

Table 4-23 lists the pin assignments and RS232C signals for Connector J3.

Refer to EIA standard RS232C for the specific AC/DC specifications for the serial interface at Connector J3.

4.9.3.2 Connector J3 Configuration

Connector J3 allows no configuration options.

4.9.4 SERIAL INTERFACE PROGRAMMING INFORMATION

You program either Connector J2 or J3 by programming Channel A or B of the 8274 MPSC device. The following sections present programming information for the 8274 MPSC, including port addresses, initialization sequences, and examples. For more information, refer to Intel's MICROSYSTEM COMPONENTS HANDBOOK or to these Intel Application Notes: ASYNCHRONOUS COMMUNICATIONS WITH THE 8274 MULTIPLE PROTOCOL SERIAL CONTROLLER, AP-134; SYNCHRONOUS COMMUNICATIONS WITH THE 8274 MULTIPLE PROTOCOL SERIAL CONTROLLER, AP-145.

Table 4-23. RS232C Pin Assignment

J2 Pin Number	RS232C Pin Number	RS232C Signal Name	RS232C Signal Function
1	14	---	---
2	1	---	---
3	15	---	---
4	2	TxD	Transmit Data
5	16	---	---
6	3	RxD	Receive Data
7	17	RxC	Receive Clock
8	4	RTS	Request To Send
9	18	---	---
1Ø	5	CTS	Clear To Send
11	19	---	---
12	6	DSR	Data Set Ready
13	2Ø	DTR	Data Terminal Ready
14	7	SG	Signal Ground
15	21	---	---
16	8	---	---
17	22	---	---
18	9	---	---
19	3	---	---
2Ø	1Ø	---	---
21	24	DTE TxC	Transmit Clock
22	11	---	---
23	25	---	---
24	12	---	---
25	nc	---	---
26	13	---	---

Note: All unlisted signals are not required by the board in the default configuration.
nc = no connection.

4.9.4.1 8274 MPSC Addressing

You program the serial interfaces by using four I/O port addresses. These port addresses, listed in Table 4-24, provide access to both channels of the 8274 MPSC device.

Table 4-24. Serial I/O Port Addresses

Port Address	Resource Accessed	Type Of Operations Available
ØØD8H	Channel A, Connector J2	Byte: Data Word: N/A
ØØDAH	Channel B, Connector J3	Byte: Data Word: N/A
ØØDCH	Channel A, Connector J2	Byte: Control/Status Word: N/A
ØØDEH	Channel B, Connector J3	Byte: Control/Status Word: N/A

4.9.4.2 8274 MPSC Initialization

Table 4-25 lists a sequence to initialize the operation of the 8274 MPSC and the interfaces at Connectors J2 and J3 for operation in the default configuration. The board supports most modes of operation of the 8274; it does not allow the use of the DMA and external synchronous detect features of the chip.

4.10 FRONT PANEL INTERFACE – J4

The front panel interface, Connector J4, provides a 14-pin connector that contains the signals that provide battery backup for memory and operate a front panel.

Three options are available for the interface at Connector J4:

- Use it as it is to provide a front panel interface, consistent with the iLBX specification.
- Use it as it is to provide battery backup for some of the memory devices on the board.
- Modify some jumpers on the board to move certain signals back to the iLBX P2 Connector, providing an auxiliary interface at connector P2 (details in Section 4.11.3).

Each of these topics is discussed following the description of the interface.

Table 4-25. 8274 Parameter Sequence for Initialization

Sequence	Port/ Data	Functions Performed in 8274 MPSC
1.	ØDEH ØØ4H	Port Number for Channel B Control Data; point to WR4B.
2.	ØDEH Ø4CH	Port Number for Channel B Control Data; 16X clock, 8-bit sync, 2 stop bits, odd parity, parity disabled.
3.	ØDEH ØØ1H	Port Number for Channel B Control Data; point to WR1B.
4.	ØDEH Ø1CH	Port Number for Channel B Control Data; disable wait, wait on transmit, interrupt on all receive, parity does not affect vector, status affects vector, no transmit interrupt, no external interrupt.
5.	ØDCH ØØ2H	Port Number for Channel A Control Data; point to WR2A.
6.	ØDCH Ø34H	Port Number for Channel A Control Data; pin-1Ø is RTS, vectored interrupt, 8Ø86 mode, receive priority, both channels interrupt mode.
7.	ØDEH ØØ2H	Port Number for Channel B Control Data; point to WR2B.
8.	ØDEH Ø3ØH	Port Number for Channel B Control Data; vector base address.
9.	ØDEH ØØ3H	Port Number for Channel B Control Data; point to WR3B.
1Ø.	ØDEH ØC1H	Port Number for Channel B Control Data; receive 8 bits/char, no auto enables, no halt mode, no receive CRC, no address search, no sync, enable receiver.
11.	ØDEH ØØ5H	Port Number for Channel B Control Data; point to WR5B.
12.	ØDEH ØFAH	Port Number for Channel B Control Data; DTR on, transmit 8 bits/char, no break, enable transmitter, no SDLC CRC, RTS on, no transmit CRC.

4.10.1 FRONT PANEL INTERFACE DESCRIPTION

Table 4-26 lists the pin assignments for Connector J4. Table 4-27 presents the DC current driving and sinking limits for the six signals on the connector.

You can use a 14-pin connector such as the Berg # 65Ø43-Ø3Ø for interfacing to Connector J4. When installing the connector, ensure that pin 1 of each connector aligns.

Table 4-26. Connector J4 Pin Assignments

Pin Number	Signal	Pin Number	Signal
1	+5 Volt Battery	2	Ground
3	+5 Volt Battery	4	Ground
5	MPRO*	6	Reserved
7	ALE	8	Ground
9	AUX RESET*	1Ø	Ground
11	EXT INTR*	12	Reserved
13	PFSN*	14	PFINT*

Note: Pin 1 is located in the lower left-hand corner, pin 2 is above it, and pin 3 is on the right side of it (looking straight at the pins, component side up).

CAUTION

When you provide a source for +5 volt (battery) power on pin 1 and pin 3 of Connector J4, remember to also provide ground on pin 2 and pin 4 from the same battery source. Failure to do so could cause ground-shifts.

4.10.2 FRONT PANEL CONFIGURATIONS

Connector J4 is configured for a Front Panel Interface in the default condition. Section 4.11.3 explains how to configure connector P2 as an auxiliary connector interface.

You can provide battery backup power for the dual-port memory chip sockets on the board. By removing jumper E261-E262, you can isolate part of the +5 volt power that provides power to the dual-port memory devices. This allows the +5 volt battery to power the dual-port memory devices.

Table 4-27. Connector J4 Interface DC Characteristics

Signal	Parameter/Conditions	Minimum	Maximum	Units
MPRO*	Vih	2.Ø	---	V
	Vil	---	Ø.8	V
	Iih @ 2.4V	---	+Ø.2	mA
	Iil @ Ø.4V	---	-1.Ø	mA
PFSN*	Vih	2.Ø	---	V
	Vil	---	Ø.8	V
	Iih @ 2.4V	---	+2.Ø	mA
	Iil @ Ø.4V	---	-5.Ø	mA
PFINT*	Vih	2.Ø	---	V
	Vil	Ø.8	Ø.8	V
	Iih @ 2.4V	-2.Ø	---	mA
	Iil @ Ø.4V	---	-1.6	mA
AUX RESET*	Vih	(note 1)	---	
	Vil	---	Ø.8	V
	Iih	(note 1)	---	
	Iil @ Ø.4V	---	-1.6	mA
EXT INTR*	Vih	2.4	---	V
	Vil	---	Ø.8	V
	Iih @ 2.4V	---	+2.Ø	mA
	Iil @ Ø.4V	---	-5.5	mA
ALE	Voh @ Ioh = -2ØØuA	2.4	-	V
	Vol @ Iol = 8mA	-	Ø.4	V

Note 1: Must be pulled to ground with an open-collector device.

4.11 iLBX™, SYNCHRONOUS, AND AUXILIARY INTERFACES - P2

The P2 Connector provides three choices for its use:

- iLBX bus (asynchronous) interface (default configuration)
- Synchronous interface (requires four jumper changes)
- Auxiliary interface (requires three jumper changes)

These configurations are listed and described in Table 4-28.

Table 4-28. Connector P2 Interface Options

Jumper Configuration	Function Performed
	Auxiliary Configuration
E263-E264	Connects the ALE signal to P2-32; requires removal of E267-E268; do not install when using iLBX memory.
E265-E266	Connects the AUX RESET signal to P2-38; requires removal of E267-E268; do not install when using iLBX memory.
	iLBX Bus and Synchronous Interface Configuration
E267-E268 §	Installed: enables iLBX/synchronous interface address drivers for driving the address lines on the P2 Connector. Removed: disables the iLBX/synchronous interface address drives at the P2 Connector; removed when placing the ALE and AUX RESET signals on the P2 Connector.
E269-E27Ø §	Enables iLBX/synchronous interface memory accesses when installed.
	iLBX Bus/Synchronous Interface Mode Select †
E278-E279 § E283-E284 § E286-E287 §	Enables iLBX mode. Must also remove E275-E276.
E277-E278 E282-E283 E275-E276 E285-E286 E275-E276	Enables synchronous interface mode.

Note: † The Mode Select jumpers are arranged for a visual check, refer to Section 4.11.2.
§ identifies the default jumper configuration.

4.11.1 iLBX™ INTERFACE DESCRIPTION

When shipped, the iSBC 286/1ØA board is configured for a high-speed local memory expansion interface at the P2 Connector, called the iLBX bus interface. The interface expands local memory on the iSBC 286/1ØA board by linking iLBX memory boards directly to the iSBC 286/1ØA board via an iLBX cable and connectors. The interface complies with the iLBX BUS SPECIFICATION as follows:

iLBX compliance: PM D16 A24

- The "PM" means the board operates as a primary master on the iLBX interface.
- The "D16" means the board can communicate with 16-bit data path devices.
- The "A24" means a 24-bit memory address path.

Refer to the iLBX BUS SPECIFICATION for the pin assignments and the AC/DC operating characteristics.

4.11.1.1 iLBX™ Interface Configurations

As Table 4-28 shows, you can disable the iLBX memory space by removing jumper E269-E27Ø. If you do not install iLBX memory, the iSBC 286/1ØA board allows the memory space normally assigned to iLBX memory to be used by the dual-port or MULTIBUS memory.

4.11.1.2 iLBX™ Bus Connector Installation Instructions

You expand the local memory on the iSBC 286/1ØA board by cabling it to iLBX memory boards via iLBX bus connectors. Most system backplanes do not include iLBX bus connectors and cables, so you must install the iLBX bus connectors and cable into the backplane.

Install the connectors into the cardcage as shown in the iLBX BUS SPECIFICATION. Pin 1 of the connectors (identified by the colored band on the cable) should be closest to the MULTIBUS connector and inside the cardcage.

Install the iSBC 286/1ØA board into the cardcage, ensuring that the P1 Connector seats into the MULTIBUS connector and that the P2 Connector seats into an iLBX bus connector.

Install your iLBX bus memory boards into the other cardslots containing iLBX bus connectors.

CAUTION

Do not install any board into an iLBX bus connector unless it has an iLBX interface.

Do not install or remove iLBX boards while power is applied to the system.

Failure to follow either of these precautions will damage the boards.

4.11.1.3 iLBX™ Bus Timing Specifications

The iSBC 286/1ØA board contains some board-specific timing requirements that affect its operation on the iLBX bus interface.

The iSBC 286/1ØA board allows you to use from zero to four wait-states when accessing the iLBX bus interface. Table 4-29 lists the timing specifications for the board in each wait-state.

Table 4-29. Timing for the iLBX™ Interface

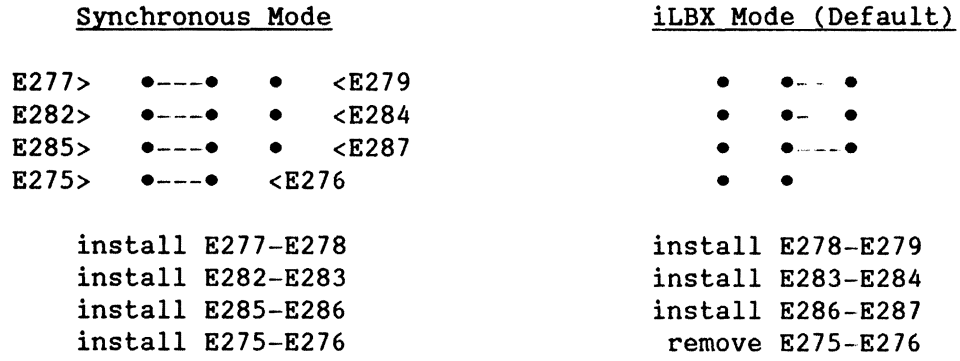
Entry Number	Parameter	Number of Wait-States				
		Ø	1	2	3	4
1	Address Strobe to Data Valid	13Ø	255	39Ø	515	64Ø
2	Address Strobe to Acknowledge (minimum)	4	129	254	379	5Ø4
3	Address Strobe to Acknowledge (maximum)	62	187	312	437	562
4	Acknowledge to Valid Data (minimum)	1Ø2	1Ø2	1Ø2	1Ø2	1Ø2
5	Data Strobe to Acknowledge (minimum)	-36	9Ø	215	34Ø	465
6	Data Strobe to Acknowledge (maximum)	6	131	256	381	5Ø6
7	Cycle Time on iLBX Bus (minimum)	25Ø	375	5ØØ	625	75Ø

Note: Address Strobe = ASTB* Acknowledge = ACK*
Data Strobe = DSTB*

4.11.2 SYNCHRONOUS INTERFACE DESCRIPTION

The P2 connector has a special option that allows synchronous data transfers with the EX-series RAM boards. This option allows access of up to 14 megabytes (limited by primary decode) of memory with no wait-states at 8 MHz.

With the iSBC 286/1ØA board in the default configuration, the P2 connector is configured for iLBX bus operation (refer to Table 4-28). The stake pins are organized on the iSBC 286/1ØA board so that a visual check can determine if the board is configured for synchronous interface or iLBX mode operation. To reconfigure the iSBC 286/1ØA for synchronous interface operation over the P2 connector, make the following jumper changes:



Both configurations, iLBX and synchronous, require jumpers E267-E268 and E269-E27Ø to be installed.

The synchronous interface uses the same cabling and pin assignments as the iLBX bus interface, except two signal lines, pins 59 and 6Ø, are redefined as follows:

Pin	Signal	Description
59	CGND	Clock Ground
6Ø	SEXCLK*	Inverted processor clock

For more information, refer to the synchronous EX-series RAM board's hardware reference manual.

CAUTION

A synchronous EX-series RAM board is required when the iSBC 286/10A board is configured for synchronous interface operation. In synchronous mode, iLBX memory boards (CX-series, for example) are not compatible.

The memory map for synchronous interface operation is the same as for iLBX memory.

4.11.3 AUXILIARY INTERFACE DESCRIPTION

As an auxiliary interface, the P2 Connector operates compatibly with the P2 Connector on boards without the iLBX bus interface, which provides both the ALE and AUX RESET signals.

To reconfigure Connector P2 for operation as an auxiliary interface, refer to Table 4-28 and make these changes:

```
 remove E267-E268 (disable the iLBX bus transceivers)
install E265-E266 (place AUX RESET onto P2 (pin 38))
install E263-E264 (place ALE onto P2 (pin 32))
```

Note that the ALE and AUX RESET signals are still available on the front panel interface (Connector J4) after the reconfiguration.

When operating as an auxiliary connector, the P2 interface provides DC characteristics for the AUX RESET and ALE signals as follows:

Signal Names	Parameter/Conditions	Maximum	Minimum	Units
ALE	Voh @ Ioh = -2ØØuA	2.4	-	V
AUX RESET	Vol @ Iol = 8mA	Ø.4	-	V

4.12 MEMORY CONFIGURATION

Before using the iSBC 286/1ØA board, you must first configure the on- and off-board memory. This section presents this information, divided into four major sections (as is the memory space): local memory, dual-port memory, iLBX bus memory, and MULTIBUS memory.

Local memory is the memory resource accessible to only the local processor and resides on-board. The iLBX and synchronous interface memory is an off-board resource that is bussed to the iSBC 286/1ØA board. The dual-port memory is on-board memory that is merely a portion of a system-wide memory resource accessible to both the MULTIBUS devices and the local CPU. The MULTIBUS memory is off-board memory accessible to the CPU through the MULTIBUS interface.

The following sections provide configuration information for the memory space in the following sequence:

4.12.1 MEMORY MAP (Default Configuration)

You must install EPROM chips (containing a boot load program) into local sockets U4Ø/U75 before you can use the board. No memory is shipped with the iSBC 286/1ØA board.

You can install four 16Kx8 devices into the local memory sockets (U4Ø, U41, U75, and U76) and four 2Kx8 devices into the dual-port RAM sockets (U53, U54, U86, and U87) without reconfiguring the jumpers on the board. This default configuration provides a memory map as shown in Figure 4-9 depending on the operating mode of the CPU (PVAM or Real Address mode).

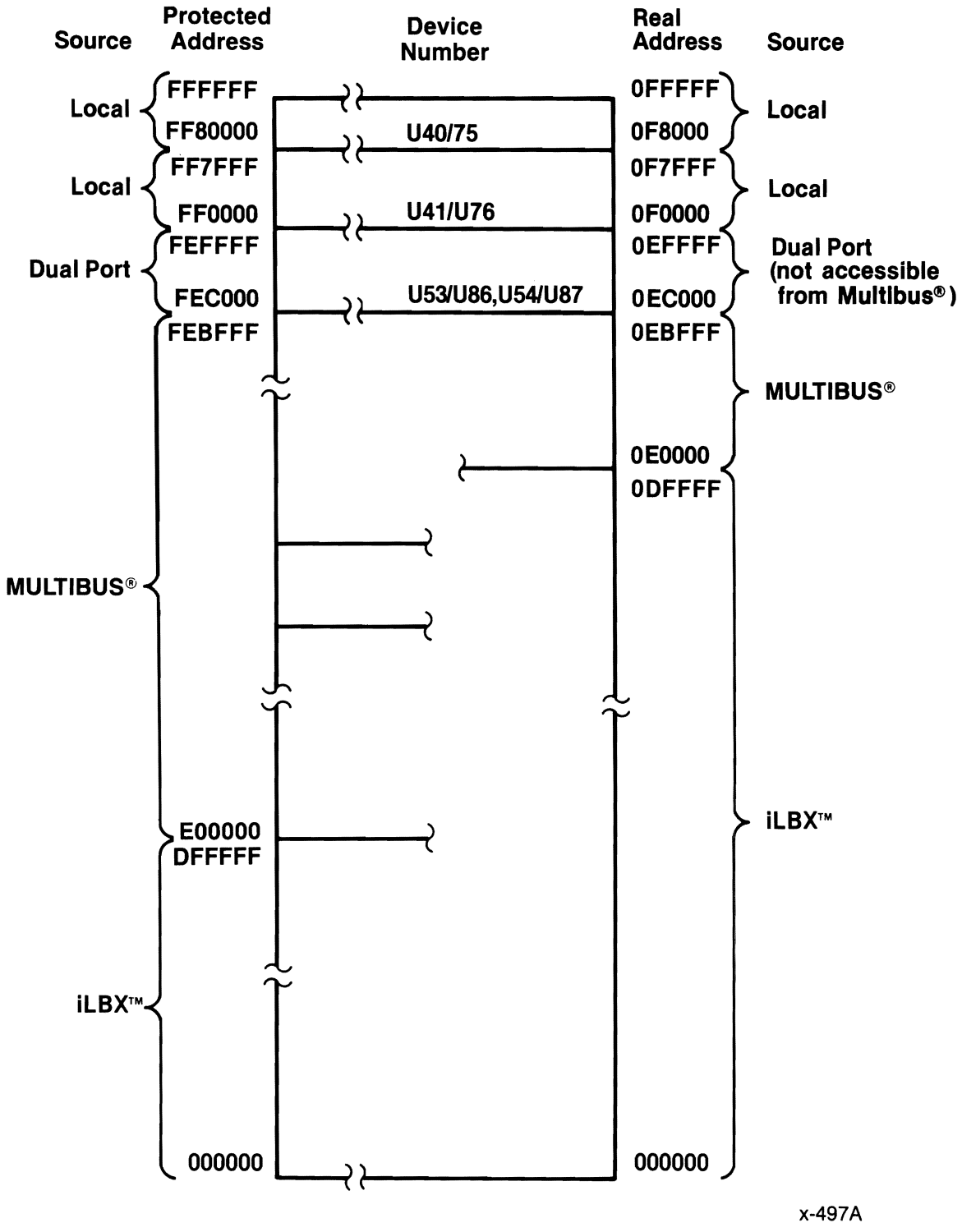


Figure 4-9. Default Memory Map (as seen by on-board CPU)

Real Address Mode (default)

iLBX Bus Address Space:	ØØØØØØH-ØDFFFFH
MULTIBUS Address Space:	ØEØØØØH-ØEBFFFH
Dual-Port Address Space (U53/U86,U54/U87):	ØECØØØH-ØEFFFFH
Local Memory Address Space at U41/U76:	ØFØØØØH-ØF7FFFH
Local Memory Address Space at U4Ø/U75:	ØF8ØØØH-ØFFFFFH

Operating Parameters for Local Memory
- Starting memory address at ØFØØØØH
- 1 wait-state for U4Ø/U75
- 1 wait-state for U41/U76
- 16Kx8 devices

Operating Parameters for Dual-Port Memory
- Starting memory address at ØECØØØH for the on-board CPU
- Starting memory address at FECØØØH from the MULTIBUS interface
- 16K byte on-board block size
- 2Kx8 devices (8K bytes without 341 or 16K bytes with 341)
- 2 wait-states (minimum from on-board)

Protected Virtual Address Mode (default)

iLBX Bus Interface Address Space:	ØØØØØØH-DFFFFFH
MULTIBUS Address Space:	EØØØØØH-FEBFFFH
Dual-Port Address Space:	FECØØØH-FEFFFFH
Local Memory Address Space at U41/U76:	FFØØØØH-FF7FFFH
Local Memory Address Space at U4Ø/U75:	FF8ØØØH-FFFFFFH

Operating Parameters for Local Memory
- Starting memory address at FFØØØØH
- 1 wait-state for U4Ø/U75
- 1 wait-state for U41/U76
- 16Kx8 devices

Operating Parameters for Dual-Port Memory
- Starting memory address at FECØØØH
- 2 wait-states (minimum from on-board)
- 16K byte on-board block size
- 16K byte off-board block size
- 2Kx8 devices (8K bytes without 341 or 16K with 341))

NOTE

The above addresses are for the on-board CPU, in Real Mode and PVAM. Other MULTIBUS masters use only the PVAM addresses for accessing dual-port memory. For example, a MULTIBUS master addresses dual-port memory from addresses FECØØØ to FEFFFF, regardless of which mode the on-board CPU is in.

4.12.2 OVERVIEW OF THE MEMORY CONFIGURATION OPTIONS

The iSBC 286/1ØA board provides configuration control features for both local and dual-port memory space. You can configure the local memory socket pairs as two independent pieces of memory address space, depending on how you configure the jumper matrices for the sockets. However, you must configure the dual-port memory as one consecutive piece of memory address space. The iLBX memory configuration depends on the operation of the iLBX bus memory boards.

Before you reconfigure memory, draw a diagram of the total memory space, showing exactly what you want. Then configure your local memory space, next your iLBX or synchronous interface memory space, and finally your dual-port memory space.

The similarities between the local and dual-port memory configuration sequences are

- A standard jumper matrix format for selecting a chip type
- 28-pin JEDEC sockets for the 24- or 28-pin memory chips
- Supports the iSBC 341 board

The differences between the local and dual-port memory configuration sequences are

- iRAM, Static RAM, and EEPROM (those requiring a 5V programming signal) devices allowed only in dual-port sockets, local sockets accept only EPROM
- Block size select for dual-port; none for local
- Battery back-up for dual-port; none for local
- Two wait-states (nonselectable) for dual-port sockets; selectable (from 1 to 3) wait-states for local
- Continuous one-part memory space in dual-port sockets; optional two-part (noncontinuous) memory space for local

When determining iLBX and local memory address ranges for each configuration, you must consider the operating mode of the CPU. When the CPU operates in Real Address mode, the board works with 2Ø-bit addresses. If you switch it to PVAM, the CPU operates with 24-bit addresses. The significance of the address mode switch is shown more clearly in the discussion of the starting address selection for the local memory space.

Both the local and dual-port sockets accept the iSBC 341 Memory Expansion MULTIMODULE board. Refer to Section 4.12.5 for more information and Appendix F for installation.

Refer to Appendix E for configuring the memory sockets for specific memory device types: EPROM, iRAM, and Static RAM.

4.12.3 LOCAL MEMORY CONFIGURATION

This section describes configuration options for the local memory resources. The following sections present information on the local memory configuration in this order:

- Description of the sockets
- Overview of the configuration sequence
- Details of the configuration sequence

4.12.3.1 Local Memory Socket Pair Descriptions

The iSBC 286/1ØA board contains no local memory when shipped from the factory. The default configuration accepts four 16Kx8 EPROM devices in the 28-pin JEDEC-compatible chip sockets: U4Ø, U41, U75, and U76. This arrangement provides 64K bytes of local memory (in PVAM, addresses FFØØØØH to FFFFFFH).

The design allows you to partition the local memory into two pieces and configure each piece independently. Sockets U4Ø and U75 are a socket set, referred to as pair U4Ø/U75; sockets U41 and U76 are a set, referred to as pair U41/U76.

The chip sockets allow you to install up to 256K bytes (maximum) of local memory on the board. Figure 4-1Ø shows the local memory sockets and the jumper matrices for the sockets.

Local memory socket pair U4Ø/U75 must always be top-justified (able to address the highest addresses) in your local memory map. The sockets are intended for EPROM that contains the boot-up program for a power-up sequence.

Socket pair U41/U76 can be moved within the memory map; you can either top-justify it behind U4Ø/U75 to provide more EPROM space for the boot-up program (continuous memory), or you can separate it to create a separate local memory space from that of U4Ø/U75.

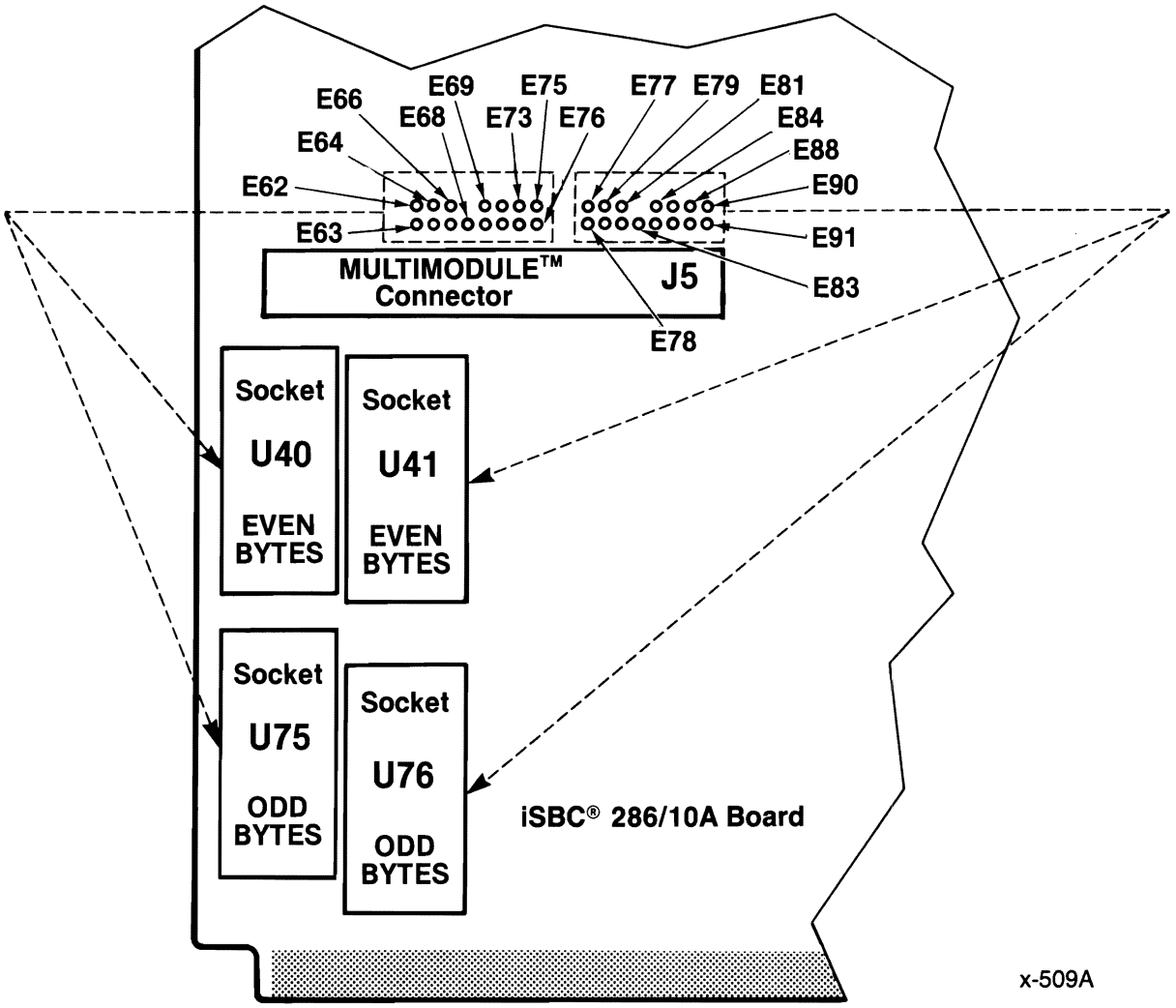


Figure 4-1Ø. Local Memory Socket Pairs and Jumper Matrices

4.12.3.2 Local Memory Configuration Sequence Overview

You can logically step through the entire local memory configuration sequence by performing four steps, as follows:

1. Select a device type for each socket pair.

   Configure the board for operation with a specific type of memory device by installing or removing jumpers at jumper matrix E62 through E76 for socket pair U4Ø/U75 and at E77 through E91 for socket pair U41/U76.

2. Select a starting address and size for local memory.

   This selection is determined by PAL U74, the primary decode PAL. Make the selection by configuring jumper inputs E218 through E221 for the PAL; you must select one of four memory map configurations for all of the local memory (including the iLBX memory). If one of the four options does not provide a suitable solution, you can custom-program a replacement PAL for socket U74 to create your own solution.

3. Select size/justification for local memory.

   This is another combination selection coordinated by PAL U6Ø and U61, the secondary decode PAL. Make the selection by configuring jumpers E49, E5Ø, E51, E57, E58, and E59 for the PAL devices, thus changing the size of the memory space and the justification of each socket pair.

NOTE

You must configure the memory size using a two-level decode in step 2 and step 3 of this sequence. Step 2 provides a primary level of decode and step 3 provides a secondary decode. Step 2 also defines the iLBX/synchronous interface memory map.

The iSBC 286/1ØA board always manipulates local memory in 16K-byte blocks. You cannot change the block size.

4. Select wait-state timing for local memory.

   Select the number of CPU wait-states by configuring jumpers E178 through E181. The jumpers provide nine options that provide from one to three wait-states at each socket pair.

The following sections provide details for each step of the configuration sequence.

4.12.3.2.1 STEP 1 – SELECT A DEVICE TYPE FOR EACH SOCKET PAIR.

You can use only EPROM device types in the local memory sockets.

The socket pair jumper matrix consists of 15 stake pins arranged in two rows. The pin arrangement is a standard format, as shown in Figure 4-11; the missing pin serves as a key to the orientation of the matrix. Figure 4-11 also lists the signals assigned to each pin of the matrix.

Figure 4-1Ø shows the approximate location of the jumper matrices on the board. You will find three of these jumper matrices on the iSBC 286/1ØA board: two for local memory and one for dual-port memory. You can configure each matrix independently for a different type of memory device, if required.

You can install a different type of memory chip into each pair of local memory sockets; however, you cannot mix types within a socket pair. For example, if you install a 32Kx8 EPROM device at U4Ø, then you must install a 32Kx8 EPROM device at U75; meanwhile, you could install 16Kx8 EPROM devices in the other pair of sockets, U41 and U76.

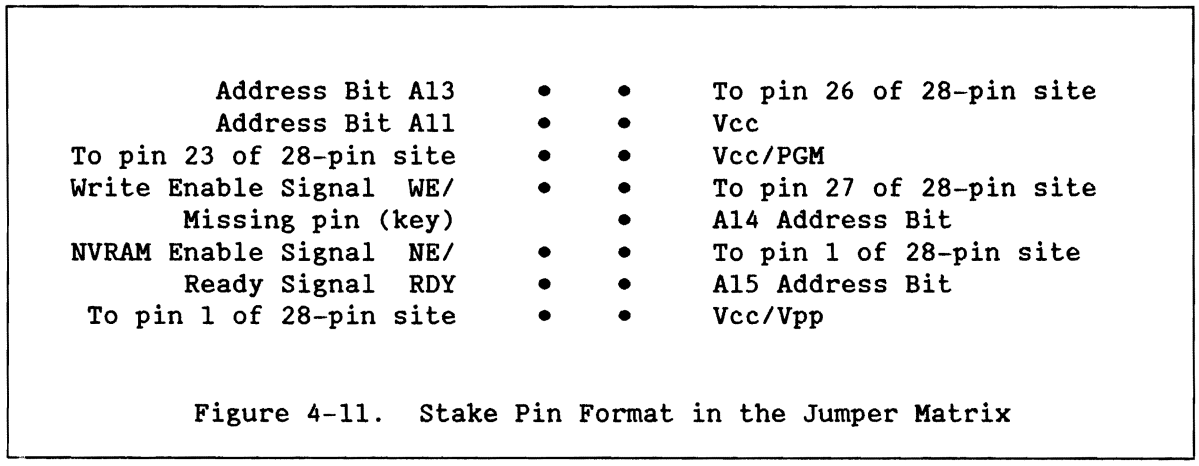


Figure 4-11. Stake Pin Format in the Jumper Matrix

JUMPER MATRIX CONFIGURATION

Each matrix is configured in a similar fashion; you install jumpers as required to place signals onto the proper pins of the memory devices.

Figure 4-11 shows the stake pins in a generic fashion. To make the figure specific to a particular socket pair, list the Exxx number for each stake pin in the matrix for that pair. Jumpers E62 through E76 configure socket pair U4Ø/U75, and jumpers E77 through E9Ø configure pair U41/U76.

The types of memory devices and the jumper matrix configurations for each socket are explained in further detail in Appendix E.

The six options for each of the local memory socket pairs are as follows:

Matrix Conf. Numbers	Type of Memory Device in the Socket Pair	Reference
6 through 11	For applications using EPROM devices	Figure E-4

Some of the figures list a specific part number in addition to the more generic part number. You can use any electrical and mechanical equivalent.

4.12.3.2.2 STEP 2 – SELECT A STARTING ADDRESS AND SIZE FOR LOCAL MEMORY. In this step, you provide a partial selection of the memory size. Step 3 completes the memory size configuration.

You select a starting address and size for local memory by configuring jumpers E218 through E221 for PAL U74. As you do, you select one of four memory map configurations for all of the local memory (including the iLBX memory). Figure 4-12 shows the approximate location and orientation of jumpers E218 through E221.

Table 4-3Ø lists the four memory map options through primary decode that are available through jumper configuration. Tables 4-31 through 4-34 show details of each of the four memory map options and list the changes that occur when the CPU switches from Real Address mode to PVAM operation.

If none of the four options provides a suitable solution, you can custom-program a replacement PAL for socket U74 to create your own solution. Appendix C presents the PAL equations for designing your own version of the PAL. Appendix C is also designed as a quick reference to the primary memory decode options.

Table 4-3Ø. Memory Map (Primary Decode) Options

Option Number	Jumpers Required	Function Performed
Ø	E218-E219 removed E22Ø-E221 removed	Primary Decode Option Ø.
1 §	E218-E219 installed E22Ø-E221 removed	Primary Decode Option 1.
2	E218-E219 removed E22Ø-E221 installed	Primary Decode Option 2.
3	E218-E219 installed E22Ø-E221 installed	Primary Decode Option 3.
Note: § indicates default configuration.		

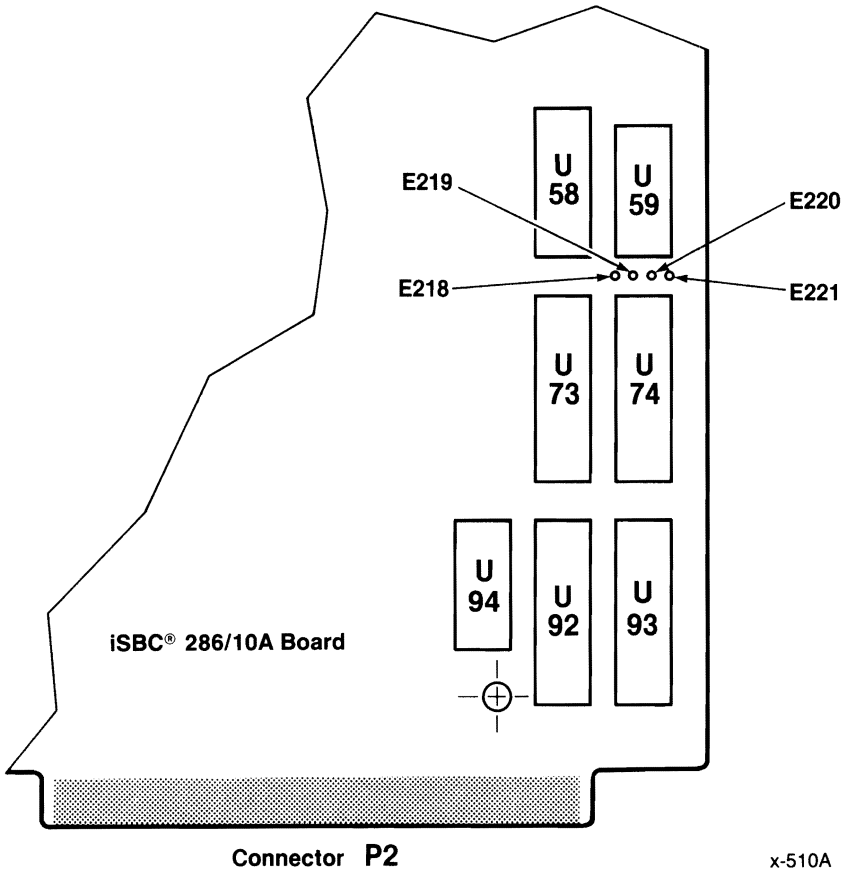


Figure 4-12. Local Memory Jumper Location

Table 4-31. Local Memory Map - Primary Decode Option Ø

E218-219 removed, E22Ø-221 removed			
Local Memory At U4Ø/U75:			Capacity:
PVAM	=	FFCØØØ-FFFFFF	16K bytes
Real Address Mode	=	ØFCØØØ-ØFFFFF	16K bytes
Local Memory At U41/U76:			
PVAM	=	FFØØØØ-FFBFFF	48K bytes
Real Address Mode	=	ØFØØØØ-ØFBFFF	48K bytes
iLBX Bus Memory:			
PVAM	=	ØØØØØØ-DFFFFF	14M bytes
Real Address Mode	=	ØØØØØØ-ØDFFFF	896K bytes

Note: This option requires use of Secondary Decode Option Ø.

Table 4-32. Local Memory Map - Primary Decode Option 1 (Default Configuration)

E218-219 installed, E22Ø-221 removed (default configuration)			
Local Memory At U4Ø/U75:			Capacity:
PVAM	=	FF8ØØØ-FFFFFF	32K bytes
Real Address Mode	=	ØF8ØØØ-ØFFFFF	32K bytes
Local Memory At U41/U76:			
PVAM	=	FFØØØØ-FF7FFF	32K bytes
Real Address Mode	=	ØFØØØØ-ØF7FFF	32K bytes
iLBX Bus Memory:			
PVAM	=	ØØØØØØ-DFFFFF	14M bytes
Real Address Mode	=	ØØØØØØ-ØDFFFF	896K bytes

Note: This option requires use of Secondary Decode Option 1.

Table 4-33. Local Memory Map - Primary Decode Option 2

E218-219 removed, E22Ø-221 installed			
Local Memory At U4Ø/U75:			Capacity:
PVAM	=	FFØØØØ-FFFFFF	64K bytes
Real Address Mode	=	ØFØØØØ-ØFFFFF	64K bytes
Local Memory At U41/U76:			
PVAM	=	FCØØØØ-FEFFFF	192K bytes
Real Address Mode	=	ØCØØØØ-ØEFFFF	192K bytes
iLBX Bus Memory:			
PVAM	=	ØØØØØØ-DFFFFF	14M bytes
Real Address Mode	=	ØØØØØØ-Ø9FFFF	64ØK bytes

Note: This option requires use of Secondary Decode Option 2.

Table 4-34. Local Memory Map - Primary Decode Option 3

E218-219 installed, E22Ø-221 installed			
Local Memory At U4Ø/U75:			Capacity:
PVAM	=	FEØØØØ-FFFFFF	128K bytes
Real Address Mode	=	ØFØØØØ-ØFFFFF	64K bytes
Local Memory At U41/U76:			
PVAM	=	FCØØØØ-FDFFFF	128K bytes
Real Address Mode	=	ØCØØØØ-ØEFFFF	192K bytes
iLBX:			
PVAM	=	ØØØØØØ-DFFFFF	14M bytes
Real Address Mode	=	ØØØØØØ-Ø9FFFF	64ØK bytes

Note: This Primary Option can use Secondary Decode Option 3, 4, 5, 6, or 7.

4.12.3.2.3 STEP 3 - SELECT SIZE/JUSTIFICATION FOR LOCAL MEMORY.

Complete the memory size selection (begun in step 2) by configuring jumper pairs E49-E57, E5Ø-E58, and E51-E59, the input signals for PAL devices U6Ø and U61. This changes the size of the memory space available at each socket pair and the justification of the memory within socket pair U41/U76. PAL U61 performs a secondary decode of the memory size. Figure 4-13 shows the jumpers that perform the selection.

You can move the memory in the U41/U76 socket pair to some extent. Jumpers pairs (49 to 57, 5Ø to 58, 51 to 59) disjoin the memory space within socket pair U41/U76 from the memory space within socket pair U4Ø/U75. The memory within socket pair U4Ø/U75 must always be top-justified.

Table 4-35 lists the jumpers required to select each of the eight options available and shows the restrictions that those configurations place onto the primary decode options (configured in step 2).

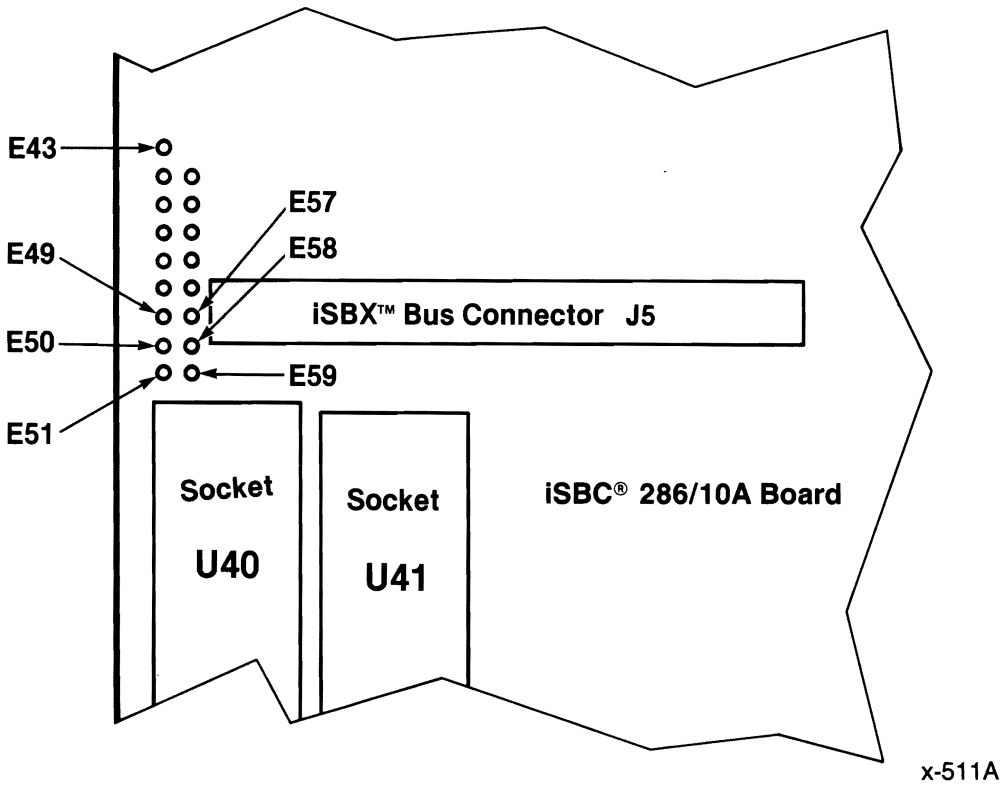


Figure 4-13. Size/Justification Jumper Locations on the Board

Table 4-36 lists the memory size that each of the options allowed at each socket and lists the address ranges for each socket pair. Notice, from the address ranges, that Secondary Decode Options 4 through 7 allow discontinuity of memory addresses between the two socket pairs.

Sockets U4Ø and U41 always hold even-byte addresses, and U75 and U76 hold odd-byte addresses.

Table 4-35. Jumper Configurations for Secondary Decode Options

Secondary Option Number	Jumper Configuration			Primary Option Number Required (from step 2)
	E51-59	E5Ø-58	E49-57	
Ø	NO	NO	NO	Ø
1 §	NO	NO	YES	1
2	NO	YES	NO	2
3	NO	YES	YES	3
4	YES	NO	NO	3
5	YES	NO	YES	3
6	YES	YES	NO	3
7	YES	YES	YES	3

Note: § indicates default configuration.

Table 4-36. Local Memory Configurations Allowed By Each Secondary Option

Primary/ Secondary Option Number	Number of Bytes of Storage At Each Socket (note 1)				Addresses Ranges Available At Each Socket Pair (note 3)	
	U4Ø	U75	U41	U76	U4Ø/U75	U41/U76
Real Address Mode						
Ø/Ø	8Kx8	8Kx8	8Kx8	8Kx8	FCØØØ-FFFFF	F8ØØØ-FBFFF
1/1 §	16Kx8	16Kx8	16Kx8	16Kx8	F8ØØØ-FFFFF	FØØØØ-F7FFF
2/2	32Kx8	32Kx8	32Kx8	32Kx8	FØØØØ-FFFFF	EØØØØ-EFFFF
3/3 (note 2)	64Kx8	64Kx8	64Kx8	64Kx8	EØØØØ-FFFFF	CØØØØ-DFFFF
3/4	64Kx8	64Kx8	2Kx8	2Kx8	EØØØØ-FFFFF	CØØØØ-CØFFF
3/5	64Kx8	64Kx8	8Kx8	8Kx8	EØØØØ-FFFFF	CØØØØ-C3FFF
3/6	64Kx8	64Kx8	16Kx8	16Kx8	EØØØØ-FFFFF	CØØØØ-C7FFF
3/7	64Kx8	64Kx8	32Kx8	32Kx8	EØØØØ-FFFFF	CØØØØ-CFFFF
Protected Virtual Address Mode						
Ø/Ø	8Kx8	8Kx8	8Kx8	8Kx8	FFCØØØ-FFFFFF	FF8ØØØ-FFBFFF
1/1 §	16Kx8	16Kx8	16Kx8	16Kx8	FF8ØØØ-FFFFFF	FFØØØØ-FF7FFF
2/2	32Kx8	32Kx8	32Kx8	32Kx8	FFØØØØ-FFFFFF	FEØØØØ-FEFFFF
3/3 (note 2)	64Kx8	64Kx8	64Kx8	64Kx8	FEØØØØ-FFFFFF	FCØØØØ-FDFFFF
3/4	64Kx8	64Kx8	2Kx8	2Kx8	FEØØØØ-FFFFFF	FCØØØØ-FCØFFF
3/5	64Kx8	64Kx8	8Kx8	8Kx8	FEØØØØ-FFFFFF	FCØØØØ-FC3FFF
3/6	64Kx8	64Kx8	16Kx8	16Kx8	FEØØØØ-FFFFFF	FCØØØØ-FC7FFF
3/7	64Kx8	64Kx8	32Kx8	32Kx8	FEØØØØ-FFFFFF	FCØØØØ-FCFFFF

Notes:
1. Options 4 to 7 list maximum memory sizes. You can install smaller capacity chips onto the board, but the memory may appear more than once in the listed address space.
2. U41/U76 is contiguous with U4Ø/U75 for options Ø to 3 and not contiguous for options 4 to 7.
3. Addresses within socket pair U4Ø/U75 are always top-justified.
4. Option 4 mixes 64Kx8 EPROM devices and 2Kx8 EPROM devices.
5. Option 5 mixes 64Kx8 EPROM devices and 8Kx8 EPROM devices.
6. Option 6 mixes 64Kx8 EPROM devices and 16Kx8 EPROM devices.
7. Option 7 mixes 64Kx8 EPROM devices and 32Kx8 EPROM devices.
8. Local memory sockets accept only EPROM devices.

§ Identifies the default configuration.

4.12.3.2.4 STEP 4 – SELECT WAIT-STATE TIMING FOR LOCAL MEMORY.

You can configure the number of wait-states that your CPU executes whenever it performs a memory operation with each local memory socket pair. This ensures that the CPU waits long enough for a response from a slower type of memory device.

You perform the configuration for both local socket pairs in a sequence of three steps, as follows:

1. Using the data sheet for the memory device, determine the various parameter times required by the memory devices that you wish to install. These parameters can vary for each socket pair since you can install different types of memory devices into each pair.

2. Turn to Appendix D of this manual. Compare the timing requirements for your memory devices with the timing requirements for the iSBC 286/1ØA board, listed for an 8.Ø MHz clock. Choose the configuration that ensures board operation with your memory devices. After locating a table whose parameters work with your memory device, you can convert those parameters into wait-states by using the wait-state numbers in the table titles.

3. Now that you have the number of wait-states, you can configure operation by installing or removing jumpers E177 through E181, as listed in Table 4-37. You can configure each local socket pair for a different type of operation if required.

Table 4-37. Local Memory Wait-State Jumpers

Local Pair U4Ø/U75 Wait-states	Local Pair U41/U76 Wait-states	Jumper Connections
1 §	1 §	None §
1	2	E177-E18Ø
1	3	E177-E178
2	1	E179-E18Ø
2	2	E18Ø-E181
2	3	E179-E18Ø, E177-E178
3	1	E178-E179
3	2	E178-E179, E177-E18Ø
3	3	E178-E181

Notes: § indicates default configuration.

4.12.4 DUAL-PORT MEMORY CONFIGURATION

This section describes options that are available to you in configuring the dual-port memory resources. The following sections present information on the dual-port memory configuration in this order:

- Description of the dual-port memory sockets
- Overview of the configuration sequence
- Details of the configuration sequence

4.12.4.1 Dual-Port Memory Socket Pair Description

The iSBC 286/1ØA board contains four 28-pin chip sockets for JEDEC-compatible memory devices. These sockets provide up to 128K bytes (maximum) of dual-port memory. Figure 4-14 shows the dual-port memory sockets and the jumper matrix for the sockets.

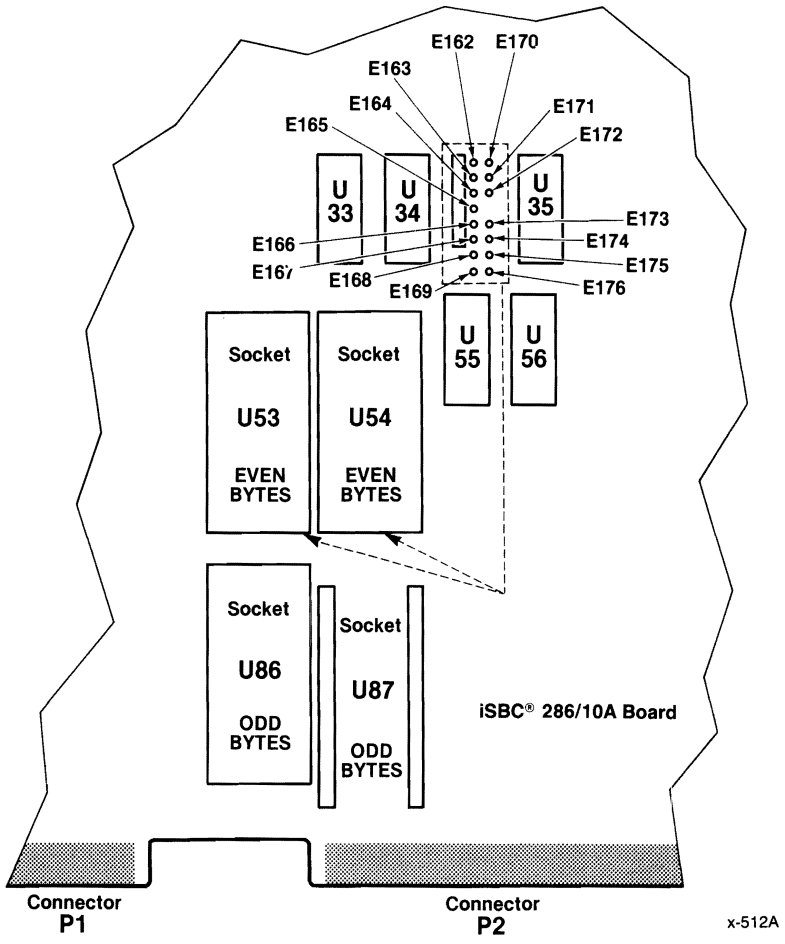


Figure 4-14. Dual-Port Memory Socket Pairs and Jumper Matrix

The default configured iSBC 286/1ØA board contains no dual-port memory. However, the board accepts four 2Kx8 Static RAM devices in chip sockets U53, U54, U86, and U87 and an iSBC 341 Memory Expansion MULTIMODULE Board. This arrangement provides 16K bytes of dual-port memory (in PVAM, addresses FECØØØH to FEDFFFH on-board and addresses FEEØØØH to FEFFFFH on the iSBC 341 board).

4.12.4.2 Dual-Port Memory Configuration Sequence Overview

If you cannot use the iSBC 286/1ØA board with a dual-port memory arrangement as shipped, you can reconfigure the memory arrangement by changing some or all of the parameters that define the memory address space.

The parameters are listed in the following sections. If you change one of the parameters, be sure to check its effect on other parameters. The parameters and their accesses are as follows:

1. Select a memory device type.

2. Select a memory device size.

3. Configure a starting memory address:

   - Megabyte page select.
     For all device sizes.
   - 64K-byte page select within the chosen Megabyte page.
     For 2Kx8 and 8Kx8 device sizes.
     For 16Kx8 and 32Kx8 device sizes, select only even 64Kx8 byte pages.
   - 16K-byte boundary select within the chosen 64K-byte page.
     Only for 2Kx8 device sizes.

4. Select the amount of dual-port memory that is accessible to the on-board CPU.

5. Select the amount of dual-port memory that is accessible to other MULTIBUS masters.

6. Configure the other attributes of the dual-port operation, if required:

   - Locking the dual-port memory whenever the local CPU requests a MULTIBUS resource.

   - Providing battery back-up for the dual-port memory on the board.

The following sections provide detailed information on the six categories of parameters for the dual-port memory.

4.12.4.2.1 STEP 1 – SELECT A DUAL-PORT MEMORY DEVICE TYPE.

You can choose from among five types of memory device for your dual-port memory. The dual-port memory sockets are compatible with EPROM, static RAM, and iRAM devices; you can easily adapt the sockets for operation with almost any byte-wide memory device. However, one restriction exists in selecting memory devices:

- You must install the same type of device into all four dual-port sockets on the board.

You can add one iSBC 341 Memory Expansion MULTIMODULE Board onto the dual-port memory. The iSBC 341 board contains jumpers that allow you to install a second type of memory device into its additional four sockets.

You perform the selection by installing or removing jumpers at the jumper matrix for the dual-port memory. The methods and options are exactly as described for the local memory configurations. The jumper matrix consists of 15 stake pins arranged in two rows as shown in Figure 4-11. You will find three of these jumper matrices on the iSBC 286/1ØA board: only one is for the dual-port memory sockets; the other two are for the local memory socket pairs. To make the figure specific to a particular socket pair, you can assign jumper numbers E162 through E176 to the stake pins in the matrix.

You can install three types of memory devices onto the dual-port memory sockets on the board (refer to Figures E-2, E-3, and E-4 of Appendix E). Within each type category, you have one or more sizes of device; each is assigned a configuration number from Ø to 11. The 12 options are as follows:

Matrix Conf. Numbers	Type of Memory Device in the Socket Pair	Reference
Ø through 3	For applications using Static RAM	Figure E-2
4 and 5	For applications using iRAM	Figure E-3
6 through 11	For applications using EPROM devices	Figure E-4

Some of the figures list specific part numbers of memory devices. As an example, Figure E-2 shows the matrix configuration for 2Kx8 Static RAM devices (configuration Ø).

4.12.4.2.2 STEP 2 - SELECT A DUAL-PORT MEMORY DEVICE SIZE.

The iSBC 286/1ØA board is default configured for operation with 2Kx8 devices. You can reconfigure the board for one of three other memory device sizes by installing jumper pairs E257-E258 and E259-E26Ø. Figure 4-15 shows the location of the jumpers on the board. As Table 4-38 lists, you can configure for 2Kx8, 8Kx8, 16Kx8 or 32Kx8 memory device sizes. Notice from Table 4-38 that some devices pose starting address restrictions.

Table 4-38. Memory Device Size Selection - Dual-Port

Jumpers Installed		Memory Device Size (per socket)	Total Memory Capacity for the Dual-Port
E257-E258	E259-E26Ø		
NO §	NO §	2Kx8 device	16K bytes (1)
NO	YES	8Kx8 device	64K bytes (1)(3)
YES	NO	16Kx8 device	128K bytes (1)(4)
YES	YES	32Kx8 device	128K bytes (2)(4)

Notes:
(1) Total assumes that you install and fill an iSBC 341 board.
(2) No iSBC 341 board; the iSBC 286/1ØA board allows a maximum of 128K bytes of memory in the dual-port memory sockets.
(3) For this device size, the lowest Page Select is a 64K Page Select (starting address must be on a 64K boundary).
(4) For this device size, the lowest Page Select is an even 64K Page Select (starting address must be on a 128K boundary).
§ Indicates default configuration.

As Table 4-38 shows, dual-port memory expects the iSBC 341 Memory Expansion MULTIMODULE to be installed when using 2Kx8, 8Kx8, or 16Kx8 size memory devices. This means the lower half of the total capacity of memory will be on-board, and the upper half will be on the iSBC 341 board. If the On-Board Block Size or MULTIBUS Block Size is configured for reading the full capacity (on-board plus iSBC 341 board) and no memory is installed on the iSBC 341 board, then invalid data will be accepted as valid data when the upper 8K bytes are addressed.

For example, suppose the board remains configured at default for 2Kx8 memory devices (total capacity of dual-port = 16K bytes). The lower 8K bytes of memory reside on-board and the upper 8K bytes reside on the iSBC 341 board. Assign the on-board block size as 16K bytes (choices are Ø or 16K bytes, for 2Kx8 devices). If the iSBC 341 board is not installed, but the upper 8K bytes are addressed, bad data will be read.

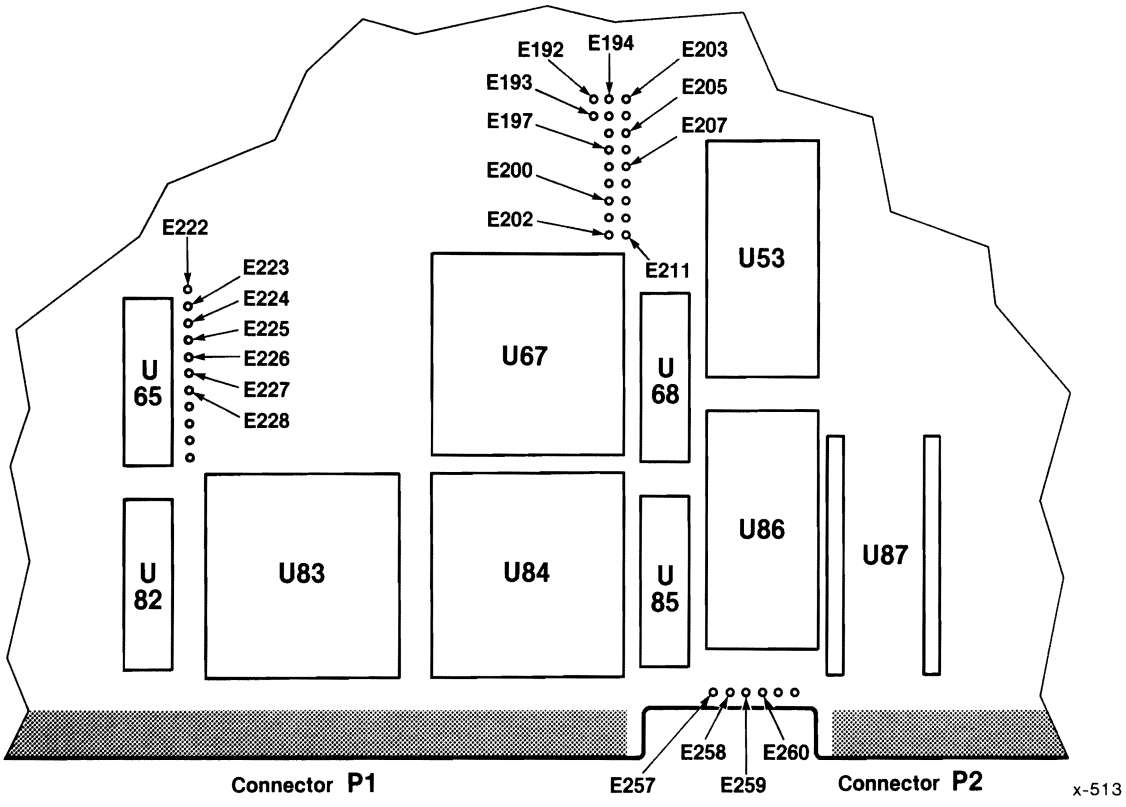


Figure 4-15. Dual-Port Jumper Locations

4.12.4.2.3 STEP 3 – SELECT THE DUAL-PORT MEMORY STARTING ADDRESS.

By configuring the starting memory address, you define a common starting memory address for both a local access and a MULTIBUS access to the dual-port memory.

In the default configuration, the board has this starting address:

- Megabyte page F (for PVAM)
- 64K byte page E
- 16K boundary CØØØ

This places the lowest byte (starting address) of the dual-port memory at address FECØØØH.

You can change the starting memory address by installing or removing jumpers E192 through E211. Figure 4-15 shows the location of the jumpers on the board. The jumpers partition the address selection process into three parts, as follows:

- Select one of 16 megabyte pages via jumpers E192, E199, E2Ø2, and E197.

  No restrictions from the device size.

  Refer to Table 4-39 for a list of the pages and their jumper configurations.

- Select a 64K-byte page within the megabyte page via jumpers E196, E2ØØ, E2Ø1, and E198.

  If a 2Kx8 or 8Kx8 device size is used, select any of the 16 64K-byte pages. If a 16Kx8 or 32Kx8 device size is used, select one of the eight even 64K-byte pages (for example, xØxxxxH or x2xxxxH).

  Refer to Table 4-4Ø for a list of the pages and their jumper configurations.

- Select a 16K-byte boundary within the 64K page via jumpers E194 and E195.

  If a 2Kx8 device size is used, select any of the four 16K-byte pages. If an 8Kx8, 16Kx8, or 32Kx8 device size is used, this boundary is not selectable (actually, xxØØØØH is used).

  Refer to Table 4-41 for a list of the boundaries and their jumper configurations.

NOTE

The following tables contain PVAM starting addresses. The Real Mode addresses are the same, except the first hexadecimal (upper four bits) is not recognized. For example, address FF8ØØØH in PVAM is the same as address ØF8ØØØH in Real Mode.

Table 4-39. Megabyte Starting Page Configuration

Jumpers Installed				Megabyte Page Selected	Megabyte Addresses
E192-E193	E199-E2Ø8	E2Ø2-E211	E197-E2Ø6		
NO	NO	NO	NO	Ø	ØxxxxxH
NO	NO	NO	YES	1	1xxxxxH
NO	NO	YES	NO	2	2xxxxxH
NO	NO	YES	YES	3	3xxxxxH
NO	YES	NO	NO	4	4xxxxxH
NO	YES	NO	YES	5	5xxxxxH
NO	YES	YES	NO	6	6xxxxxH
NO	YES	YES	YES	7	7xxxxxH
YES	NO	NO	NO	8	8xxxxxH
YES	NO	NO	YES	9	9xxxxxH
YES	NO	YES	NO	1Ø	AxxxxxH
YES	NO	YES	YES	11	BxxxxxH
YES	YES	NO	NO	12	CxxxxxH
YES	YES	NO	YES	13	DxxxxxH
YES	YES	YES	NO	14	ExxxxxH
YES§	YES§	YES§	YES§	15§	FxxxxxH

Note: No restrictions due to memory device size.
§ identifies default configuration.

Table 4-4Ø. 64K Starting Page Configuration

Jumpers Installed				64K Page Selected	Page Address
E196-E2Ø5	E2ØØ-E2Ø9	E2Ø1-E21Ø	E198-E2Ø7		
NO	NO	NO	NO	Ø	xØxxxxH †
NO	NO	NO	YES	1	x1xxxxH
NO	NO	YES	NO	2	x2xxxxH †
NO	NO	YES	YES	3	x3xxxxH
NO	YES	NO	NO	4	x4xxxxH †
NO	YES	NO	YES	5	x5xxxxH
NO	YES	YES	NO	6	x6xxxxH †
NO	YES	YES	YES	7	x7xxxxH
YES	NO	NO	NO	8	x8xxxxH †
YES	NO	NO	YES	9	x9xxxxH
YES	NO	YES	NO	1Ø	xAxxxxH †
YES	NO	YES	YES	11	xBxxxxH
YES	YES	NO	NO	12	xCxxxxH †
YES	YES	NO	YES	13	xDxxxxH
YES§	YES§	YES§	NO§	14§	xExxxxH †§
YES	YES	YES	YES	15	xFxxxxH

Note: No restrictions for 2Kx8 or 8Kx8 memory devices.
† 16Kx8 and 32Kx8 memory devices require an even 64K page.
§ identifies default configuration.

Table 4-41. 16K Starting Boundary Configuration

Jumpers Installed		16K Boundary Selected	Address Range
E194-E2Ø3	E195-E2Ø4		
NO	NO	Ø	xxØØØØH †
NO	YES	1	xx4ØØØH
YES	NO	2	xx8ØØØH
YES§	YES§	3	xxCØØØH

Note: 16x8 boundary select is only for 2Kx8 devices.
† 8Kx8, 16Kx8, and 32Kx8 devices require this boundary.
§ identifies the default configuration.

NOTE

The dual-port memory is always contiguous and bottom-justified within the address space; that is, it always starts from a 16K boundary. Specifically, for 8, 16, or 32Kx8 devices, dual-port memory always starts at xxØØØØH.

Remember that primary decode has defined the local and iLBX memory ranges. If dual-port addresses are now defined to overlap any primary decode addresses, the dual-port addresses will not be recognized. The reserved iLBX addresses may be used for dual-port memory if the iLBX bus is disabled.

4.12.4.2.4 STEP 4 - SELECT THE ON-BOARD BLOCK SIZE.

This attribute is referred to as the on-board block size. In selecting an on-board block size, you determine how much of the address space of the dual-port memory on the board is accessible to the on-board CPU. You make the selection by configuring jumpers E222 through E228. Refer to Figure 4-15 for the location of the jumpers on the board.

Table 4-42 lists the four configurations of the jumpers and the on-board block sizes that they allow. You have a choice of Ø, 16K, 32K, 64K, and 128K byte block sizes.

NOTE

If the configured block size (on-board or MULTIBUS) is greater than four times the actual block size (eight times if an iSBC 341 board is installed), then the memory will repeat within the defined memory address space. For example, do not define the block size as greater than 16K bytes when 2Kx8 size devices are used (2Kx8's yield a maximum of 16K bytes).

Table 4-42. On-Board Block Size Configuration

Jumper Configuration	On-Board Block Size Selected
E222-E223 In § E224-E225 In § E226-E227 In § E288-E289 Out §	16K bytes of on-board dual-port memory addresses. Dual-port Memory address range for the on-board CPU is the selected starting address plus 16K.
E222-E223 In E224-E225 In E226-E227 Out E288-E289 Out	32K bytes of on-board dual-port memory addresses. Dual-port Memory address range for the on-board CPU is the selected starting address plus 32K.
E222-E223 In E224-E225 Out E226-E227 Out E288-E289 Out	64K bytes of on-board dual-port memory addresses. Dual-port Memory address range for the on-board CPU is the selected starting address plus 64K.
E222-E223 Out E224-E225 Out E226-E227 Out E288-E289 Out	128K bytes of on-board dual-port memory addresses. Dual-port Memory address range for the on-board CPU is the selected starting address plus 128K.
E227-E228 In E288-E289 In	Disable all dual-port memory availability to the on-board CPU. You should also disable all dual-port memory availability to the MULTIBUS interface, per Table 4-43 (install E154-E16Ø).

Note: § identifies default configuration.

NOTE

If you disable dual-port memory space on-board (i.e., if you install jumper E227-E228), ensure that you also disable the space from the MULTIBUS interface (i.e., you must install jumper E154-E16Ø). This configuration will completely disable dual-port memory.

Remove E288-E289 when using dual-port memory. Install E288-E289 when not using dual-port memory. When installed, one wait-state is removed for MULTIBUS accesses.

4.12.4.2.5 STEP 5 – SELECT THE MULTIBUS® BLOCK SIZE.

This attribute is referred to as the MULTIBUS block size. In selecting a MULTIBUS block size, you determine how much of the address space in the dual-port memory on the board is accessible to other MULTIBUS masters. You make the selection by configuring jumpers E154 through E16Ø. Table 4-43 lists the four configurations of the jumpers and the on-board block sizes that they support: Ø, 16K, 32K, 64K, and 128K.

NOTE

By installing E154-E16Ø, you can disable accesses to the dual-port memory by all MULTIBUS devices and yet allow accesses to the dual-port memory via the on-board CPU.

Table 4-43. MULTIBUS® Block Size Configuration

Jumper Configuration	MULTIBUS® Block Size Selected
E155-E156 In § E157-E158 In § E159-E16Ø In §	16K bytes of on-board dual-port memory addresses. Dual-port Memory address range from MULTIBUS interface is selected starting address plus 16K.
E155-E156 In E157-E158 In E159-E16Ø Out	32K bytes of on-board dual-port memory addresses. Dual-port Memory address range from MULTIBUS interface is selected starting address plus 32K.
E155-E156 In E157-E158 Out E159-E16Ø Out	64K bytes of on-board dual-port memory addresses. Dual-port Memory address range from MULTIBUS interface is selected starting address plus 64K.
E155-E156 Out E157-E158 Out E159-E16Ø Out	128K bytes of on-board dual-port memory addresses. Dual-port Memory address range from MULTIBUS interface is selected starting address plus 128K.
E154-E16Ø In	Disable all dual-port memory availability to the MULTIBUS interface. To totally disable dual-port memory, refer to Table 4-42.
Note: § identifies default configuration.	

4.12.4.2.6 STEP 6 - SELECT OTHER ATTRIBUTES OF DUAL-PORT MEMORY.

The remaining attributes of the dual-port operation are the dual-port LOCK operation and the battery back-up for the dual-port memory.

LOCK CONTROL

You lock the dual-port memory by issuing an instruction containing the LOCK prefix to the CPU or by asserting the OVERRIDE signal through programming the 8255A PPI device (see Section 4.8).

Either the local CPU or a MULTIBUS master can lock the dual-port memory. Either device excludes the other from access to the dual-port memory when it asserts the LOCK* signal.

When the local CPU locks the dual-port memory, you use a jumper to control the hardware release or non-release of the locked condition.

The default configured board contains jumper E19Ø-E191, allowing the hardware to remove the LOCK* signal whenever the local CPU has the on-board dual-port memory locked and makes a MULTIBUS access request. In releasing the lock, the hardware eliminates a possible dead-lock condition: a MULTIBUS master waits for access to the locked on-board dual-port memory while the local CPU waits for access to a busy MULTIBUS interface.

By removing jumper E19Ø-E191, you prevent the local CPU from releasing the lock on the dual-port memory when it makes a MULTIBUS access request. This may be desirable for an application that cannot tolerate MULTIBUS access to the on-board dual-port memory. However, a dead-lock condition can occur as a result of holding the lock signal active.

BATTERY BACK-UP

You can enable or disable battery back-up for the dual-port memory (and an iSBC 341 board, if installed), depending on the configuration of jumper E261-E262.

You configure the board for battery back-up power by removing jumper E261-E262. This removes the dual-port sockets from the +5 volt power bus on the board. You also need to connect the user-provided +5 volt battery positive lead to pins 1 and 3 of Connector J4 and the negative lead to pins 2, 4, 8, and 1Ø of Connector J4.

4.12.5 iSBC® 341 MEMORY EXPANSION MULTIMODULE™ BOARD

With certain configurations of the iSBC 286/1ØA board, you can double the capacity of memory by adding an iSBC 341 board. The determining factor in adding the board is this: the dual-port sockets on the iSBC 286/1ØA board cannot contain more than 128K bytes of dual-port memory or more than 256K bytes of local memory.

The design of the iSBC 286/1ØA board requires you to install only one type of memory device into four dual-port sockets. However, when you add an iSBC 341 board, you gain the option of installing a second type of memory device onto the iSBC 341 board, although those memory devices must be the same size as the ones on the iSBC 286/1ØA board.

Appendix F provides installation instructions and describes the configuration options.

4.12.6 iLBX™ MEMORY CONFIGURATION

Through the iLBX bus interface, you can expand the local memory on the iSBC 286/1ØA board to a maximum of 14 megabytes (16 megabytes if PAL U74 is changed; refer to Appendix C). The speed between the 8Ø286 CPU and the iLBX bus memory is comparable to the speed between the 8Ø286 CPU and the on-board local memory.

When you add iLBX bus memory, the factory-programmed Programmable Array Logic (PAL) device at U74 assigns certain portions of the memory address space to the iLBX bus interface. To configure your iLBX memory, refer to Section 4.12.3.2.

The iSBC 286/1ØA board provides four options for your iLBX memory space:

1. Disable the use of iLBX memory by removing jumper E269-E27Ø. The previous iLBX memory locations are now available for dual-port access. If not used by dual-port, the memory locations can be configured for MULTIBUS access.

2. Use the default iLBX memory configuration, Primary Decode Option One:

   Place iLBX memory at address range ØØØØØH through ØDFFFFH by operating the CPU in Real Address mode (896K bytes).
   Place iLBX memory at address range ØØØØØØH through DFFFFFH by operating the CPU in PVAM (14M bytes).

3. Reconfigure the default iLBX memory configuration, to Primary Decode Option Two or Three (local memory also changes):

   Place iLBX memory at address range ØØØØØH through Ø9FFFFH by operating the CPU in Real Address mode (64ØK bytes).
   Place iLBX memory at address range ØØØØØØH through DFFFFFH by operating the CPU in PVAM (14M bytes).

4. Program your own PAL device for socket U74 to place the PVAM or Real Address mode address ranges where you want them.

The default configured board contains jumper E269-E27Ø, configuring the iLBX memory for option two, as previously listed. Appendix C provides information on programming another PAL. You may have to use it if you find that option one, two, or three does not fit into your application.

4.12.7 SYNCHRONOUS INTERFACE MEMORY CONFIGURATION

The iSBC 286/1ØA board also contains an option for the P2 connector, allowing synchronous data transfers. In synchronous mode, the P2 connector supports the family of EX RAM expansion boards, allowing access of up to 14 megabytes of memory with no wait-states at 8 MHz.

To use the synchronous interface, switch the mode from iLBX to synchronous configuration (see Section 4.11.2). The addressing is the same as iLBX addressing; the mode configuration determines which interface is in operation. Remember, the iLBX cabling is not compatible with synchronous interface cabling.

4.12.8 MULTIBUS® MEMORY CONFIGURATION

Accessible I/O and memory through the MULTIBUS interface, with the board in the default configuration, is as follows:

- MULTIBUS memory (Real Address mode) — ØEØØØØH-ØEBFFFH
- MULTIBUS memory (PVAM) — EØØØØØH-FEBFFFH
- MULTIBUS I/O space (with no iSBX MULTIMODULE board) — ØØØØ to ØØBFH and Ø1ØØH to FFFFH
- MULTIBUS I/O space (with an iSBX MULTIMODULE board) — ØØØØ to ØØ7FH and Ø1ØØH to FFFFH

When the iLBX or dual-port memory sockets are disabled, the memory addresses are assigned to use the MULTIBUS interface.

To disable iLBX (or synchronous interface) memory:
Remove jumper E269-E27Ø. The addresses are now available for use to dual-port memory.

To disable dual-port memory:
Install jumpers E227-E228 (disables dual-port from on-board accesses).
Install E154-E16Ø (disables dual-port from MULTIBUS accesses).

4.13 MEMORY CONFIGURATION EXAMPLES

Tables 4-44 through 4-46 provide three examples of memory configurations for the iSBC 286/1ØA board. Two of the three examples operate the iSBC 286/1ØA board in the Real Address mode. Each shows a memory map of the configuration and lists all of the jumper connections required for the configuration.

Table 4-44. Memory Configuration Example 1

Parameters:

Local Memory:	Four 8Kx8 EPROM devices
Dual-Port Memory:	Four 8Kx8 Static RAM devices on board
	Four 8Kx8 Static RAM devices for iSBC 341 board
CPU Mode:	The CPU operates in Real Address mode

Local Memory Configurations

1) Memory Type Select - four 8Kx8 EPROMs
   E71-E73 Installed
   E7Ø-E72 Installed U4Ø/U75
   E62-E63 Installed

   E77-E78 Installed
   E85-E87 Installed U41/U76
   E86-E88 Installed
   Refer to section 4.12.3.2.1

2) Starting Memory Address - Primary Decode Option # Ø
   E218-E219 Removed
   E22Ø-E221 Removed
   Refer to Section 4.12.3.2.2

3) Memory Size/Justification - Secondary Decode Option # Ø
   E51-E59 Removed
   E5Ø-E58 Removed
   E49-E57 Removed
   Refer to Section 4.12.3.2.3

4) Wait-states - U4Ø/U75 = 1 wait-state
   - U41/U76 = 1 wait-state
   No jumpers on E177 through E181
   Refer to Section 4.12.3.2.4

----------(continued)----------

Table 4-44. Memory Configuration Example 1 (continued)

Dual-Port Memory Configurations

1) Memory Type Select - eight 8Kx8 Static RAMs (4 on the iSBC 286/1ØA board, 4 on the iSBC 341 board)
  E166-E173 Installed
  E168-E169 Installed
  E174-E175 Installed
  Refer to Section 4.12.4.2.1

2) Memory Device Size - 8Kx8 devices (64K bytes total)
  E259-E26Ø Installed
  E257-E258 Removed
  Refer to Section 4.12.4.2.2

3) Starting Address - ØEØØØØH to ØEFFFFH
  E192-E193 Removed
  E199-E2Ø8 Removed
  E2Ø2-E211 Removed
  E197-E2Ø6 Removed Select ØxxxxxH

  E196-E2Ø5 Installed
  E2ØØ-E2Ø9 Installed
  E2Ø1-E21Ø Installed
  E198-E2Ø7 Removed Select xExxxxH

  E194-E2Ø3 Removed
  E195-E2Ø4 Removed Select xxØØØØH

  Refer to Section 4.12.4.2.3

4) On-Board Block Size - 64K bytes
  E222-E223 Installed
  E224-E225 Removed
  E226-E227 Removed
  E288-E289 Removed
  Refer to Section 4.12.4.2.4

5) MULTIBUS Block Size - 64K bytes
  E155-E156 Installed
  E157-E158 Removed
  E159-E16Ø Removed
  Refer to Section 4.12.4.2.5

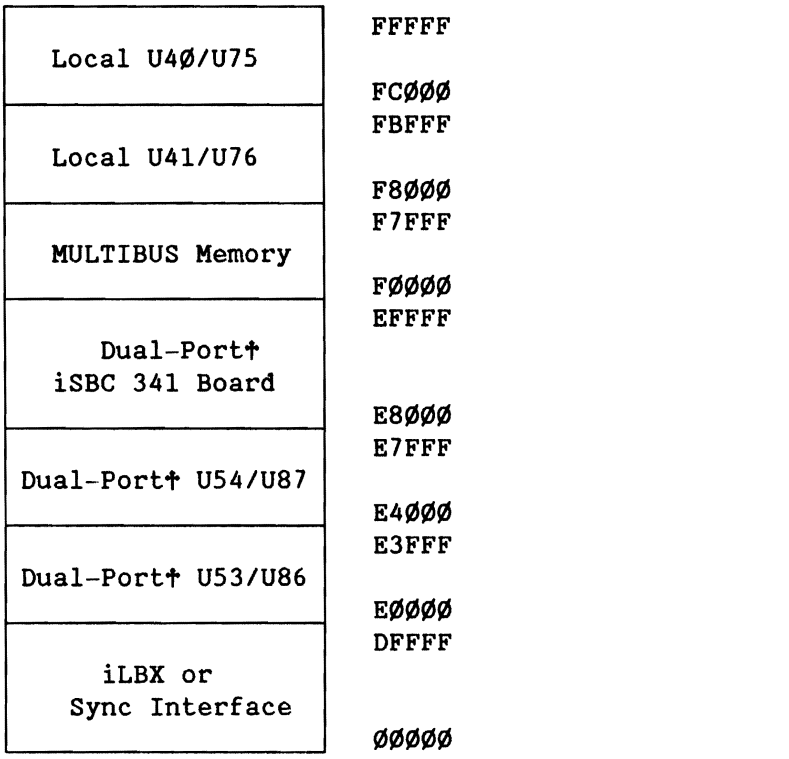
6) iSBC 341 Board Configuration - 32K bytes
  Addresses as listed in Memory Map
  See Appendix F for MULTIMODULE board jumpers
  Refer to Section 4.12.4.2.2

----------(continued)----------

Table 4-44. Memory Configuration Example 1 (continued)

7) Other Configurations
E19Ø-E191 Removed - No LOCK release
E261-E262 Installed - No battery back-up
Refer to Section 4.12.4.2.6

MEMORY MAP



Note: † Other MULTIBUS masters address dual-port memory from FEØØØØ to FEFFFF, regardless of the on-board CPU's mode.

Table 4-45. Memory Configuration Example 2

Parameters:

Local Memory:	Four 8Kx8 EPROM devices
Dual-Port Memory:	Four 8Kx8 Static RAM devices on board No devices for iSBC 341 board (board not installed)
CPU Mode:	The CPU operates in Real Address mode

(Same parameters as example 1, except not using iSBC 341 board.)

Local Memory Configurations

1) Memory Type Select - four 8Kx8 EPROMs
   E71-E73 Installed
   E7Ø-E72 Installed U4Ø/U75
   E62-E63 Installed

   E77-E78 Installed
   E85-E87 Installed U41/U76
   E86-E88 Installed
   Refer to Section 4.12.3.2.1

2) Starting Memory Address - Primary Decode Option # Ø
   E218-E219 Removed
   E22Ø-E221 Removed
   Refer to Section 4.12.3.2.2

3) Memory Size/Justification - Secondary Decode Option # Ø
   E51-E59 Removed
   E5Ø-E58 Removed
   E49-E57 Removed
   Refer to Section 4.12.3.2.3

4) Wait-states - U4Ø/U75 = 1 wait-state
   - U41/U76 = 1 wait-state
   No jumpers on E177 through E181
   Refer to Section 4.12.3.2.4

----------(continued)----------

Table 4-45. Memory Configuration Example 2 (continued)

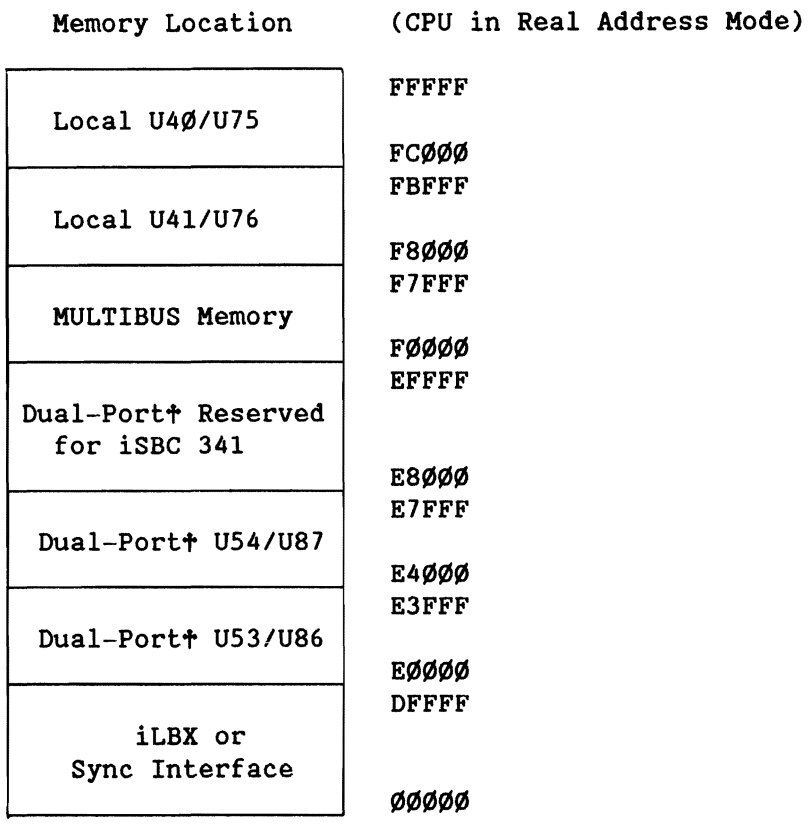
```
Dual-Port Memory Configurations

1) Memory Type Select - four 8Kx8 Static RAMs (no iSBC 341 board)
    E166-E173 Installed
    E168-E169 Installed
    E174-E175 Installed
    Refer to Section 4.12.4.2.1

2) Memory Device Size - 8Kx8 devices
    E259-E26Ø Installed
    E257-E258 Removed
    Refer to Section 4.12.4.2.2

3) Starting Address - EØØØØ to E7FFF
    E192-E193 Removed
    E199-E2Ø8 Removed
    E2Ø2-E211 Removed
    E197-E2Ø6 Removed   Select ØxxxxxH

    E196-E2Ø5 Installed
    E2ØØ-E2Ø9 Installed
    E2Ø1-E21Ø Installed
    E198-E2Ø7 Removed   Select xExxxxH

    E194-E2Ø3 Removed
    E195-E2Ø4 Removed   Select xxØØØØH

    Refer to Section 4.12.4.2.3

4) On-Board Block Size - 32K bytes (all)
    E222-E223 Installed
    E224-E225 Installed
    E226-E227 Removed
    E288-E289 Removed
    Refer to Section 4.12.4.2.4

5) MULTIBUS Block Size - 32K bytes (all)
    E155-E156 Installed
    E157-E158 Installed
    E159-E16Ø Removed
    Refer to Section 4.12.4.2.5

6) iSBC 341 Board Configuration - none
    Not required for this example
```

----------(continued)----------

Table 4-45. Memory Configuration Example 2 (continued)

7) Other Configurations
   E19Ø-E191 Removed - No LOCK release
   E261-E262 Installed - No battery back-up
   Refer to Section 4.12.4.2.6

MEMORY MAP



Note: † Other MULTIBUS masters address dual-port memory from FEØØØØ to FE7FFF, regardless of the on-board CPU's mode.

Table 4-46. Memory Configuration Example 3

Parameters:

Local Memory:	Four 8Kx8 EPROM devices
Dual-Port Memory:	Four 16Kx8 EPROM devices on board
	Four 16Kx8 EPROM devices on the iSBC 341 board
CPU Mode:	The CPU operates in PVAM

Local Memory Configurations

1) Memory Type Select - four 8Kx8 EPROMs

   E71-E73 Installed
   E7Ø-E72 Installed U4Ø/U75
   E62-E63 Installed

   E77-E78 Installed
   E85-E87 Installed U41/U76
   E86-E88 Installed
   Refer to Section 4.12.3.2.1

2) Starting Memory Address - Primary Decode Option # Ø
   E218-E219 Removed
   E22Ø-E221 Removed
   Refer to Section 4.12.3.2.2

3) Memory Size/Justification - Secondary Decode Option # Ø
   E51-E59 Removed
   E5Ø-E58 Removed
   E49-E57 Removed
   Refer to Section 4.12.3.2.3

4) Wait-states - U4Ø/U75 = 1 wait-state
   - U41/U76 = 1 wait-state
   No jumpers on E177 through E181
   Refer to Section 4.12.3.2.4

----------(continued)----------

Table 4-46. Memory Configuration Example 3 (continued)

Dual-Port Memory Configurations

1) Memory Type Select - eight 16Kx8 EPROMs (4 on the iSBC 286/10A board and 4 on the iSBC 341 board)
   E166-E167 Installed
   E174-E175 Installed
   E162-E17Ø Installed
   E169-E176 Installed
   E168-E169 Removed
   E173-E174 Removed
   Refer to Section 4.12.4.2.1

2) Memory Device Size - 16Kx8 devices plus 341 (128K bytes total)
   E259-E26Ø Removed
   E257-E258 Installed
   Refer to Section 4.12.4.2.2

3) Starting Address - FØØØØØ to F1FFFF
   E192-E193 Installed
   E199-E2Ø8 Installed
   E2Ø2-E211 Installed
   E197-E2Ø6 Installed Select FxxxxxH

   E196-E2Ø5 Removed
   E2ØØ-E2Ø9 Removed
   E2Ø1-E21Ø Removed
   E198-E2Ø7 Removed Select xØxxxxH

   E194-E2Ø3 Removed
   E195-E2Ø4 Removed Select xxØØØØH

   Refer to Section 4.12.4.2.3

4) On-Board Block Size - 128K bytes
   E222-E223 Removed
   E224-E225 Removed
   E226-E227 Removed
   E288-E289 Removed
   Refer to Section 4.12.4.2.4

5) MULTIBUS Block Size - 128K bytes
   E155-E156 Removed
   E157-E158 Removed
   E159-E16Ø Removed
   Refer to Section 4.12.4.2.5

----------(continued)----------

Table 4-46. Memory Configuration Example 3 (continued)

6) iSBC 341 Board Configuration - 64K bytes
   Addresses as listed in Memory Map
   Refer to Appendix F for MULTIMODULE board jumpers
   Refer to Section 4.12.4.2.2

7) Other Configurations
   E19Ø-E191 Removed - No LOCK release
   E261-E262 Installed - No battery back-up
   Refer to Section 4.12.4.2.6

MEMORY MAP

Memory Location	(CPU in PVAM)
Local U4Ø/U75	FFFFFF
	FFCØØØ
Local U41/U76	FFBFFF
	FF8ØØØ
MULTIBUS Memory	FF7FFF
	F2ØØØØ
Dual-Port† iSBC 341 Board	F1FFFF
	F1ØØØØ
Dual-Port† U54/U86	FØFFFF
	FØ8ØØØ
Dual-Port† U53/U86	FØ7FFF
	FØØØØØ
MULTIBUS Memory	EFFFFF
	EØØØØØ
iLBX or Sync Interface	DFFFFF
	ØØØØØØ

Note: † Other MULTIBUS masters address dual-port memory from FØØØØØ to F1FFFF, regardless of the on-board CPU's mode.

***

5.1 INTRODUCTION

This chapter provides a list of service diagrams, and service and repair assistance instructions for the iSBC 286/1ØA Single Board Computer.

5.2 SERVICE DIAGRAMS

The parts location diagram and schematic diagram for the iSBC 286/1ØA board are shown in Figures 5-2 and 5-3. Figures 5-4 and 5-5 show a parts location diagram and a schematic for the 82289 Emulator Board at chip location U77/U78 on the iSBC 286/1ØA board. Table 5-1 provides a schematic mini-index.

On the schematic diagram, a signal mnemonic that ends with an asterisk (e.g., ALE*) is active low. Conversely, a signal mnemonic without an asterisk (e.g., ALE) is active high.

5.3 SERVICE AND REPAIR ASSISTANCE

Customer Support Service Engineering provides both a Return Replacement Authorization (RRA) and Direct Return Authorization (DRA) service.

The RRA service replaces a defective product. Return the defective product to Intel, freight prepaid. Intel will replace the product, bearing a new serial number. This service is not offered on all products and is subject to availability. Typically, Intel ships the replacement product within 48 hours of receiving the defective product.

The DRA service provides repair work. Return the defective product to Intel, freight prepaid. Intel will repair, test, and update the product with Engineering Change Orders. The serial number will not change. Normal turnaround time is four to six weeks from receipt of the defective product.

Determine which service you need, RRA or DRA. Before calling Customer Support Service, have the necessary information ready (see Figure 5-1 for the telephone number for your area):

a. Part and serial number of the product.

b. Purchase order number, for repair and shipping charges.

c. If it is a warranty repair, the proof of purchase showing the product was received within 9Ø days of the service request date. Without proof, services will be billed at the current rate.

d. Your shipping and billing addresses.

e. Your telephone number.

In correspondence with Customer Support Service, reference the authorization number on the packing slip, the purchase order, and any other related documents.

Before shipping, remove all user modifications. Protect the equipment from damage in transit:

a. Place boards in antistatic bags and then in padded shipping bags. Wrap power supplies and other large items in antistatic material.

b. Protect the product with protective padding such as flow pack or foam.

c. Write the return authorization number on the outside of the box and label it "FRAGILE."

NOTE

Damage due to lack of compliance with safe return packaging could result in extra repair charges.

d. Forward the product and all correspondence to this address:

Intel Corporation
Customer Support Marketing Administration
Billing Department - DV-1-7Ø4
24Ø2 W. Beardsley Road
Phoenix, Arizona 85Ø27
Authorization # _____

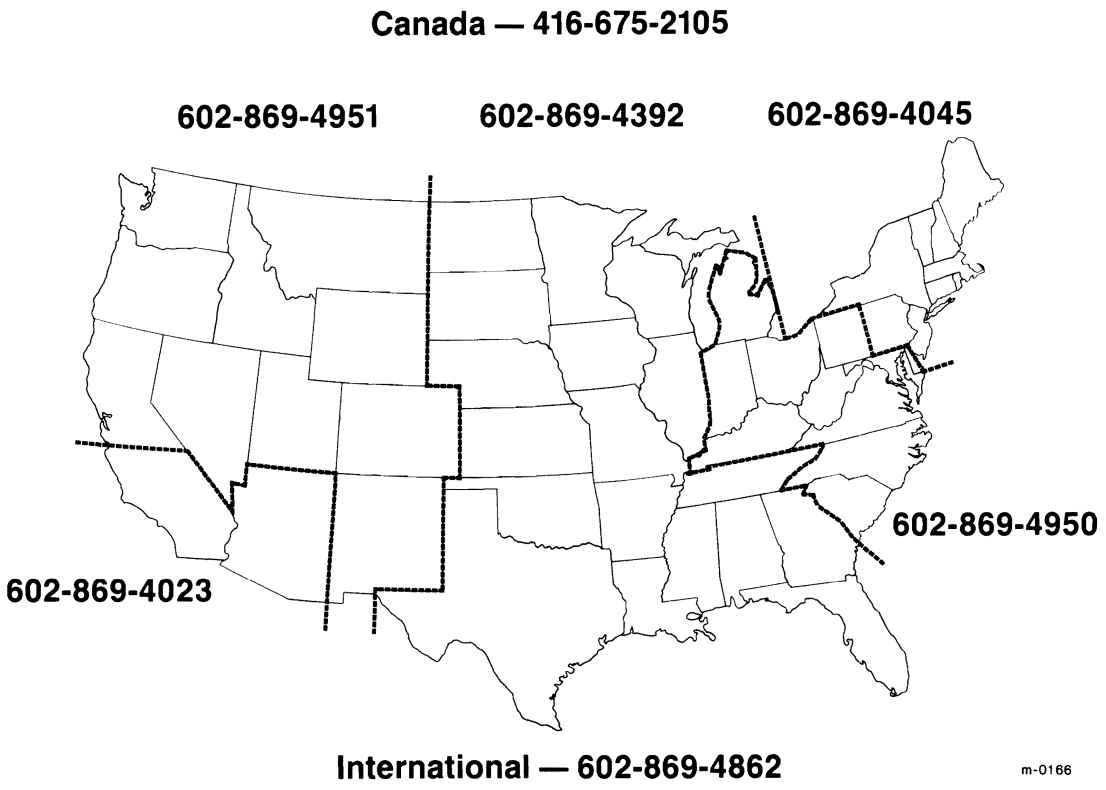


Figure 5-1. Territorial Service Telephone Numbers

Table 5-1. Schematic Index

Item	Schematic Sheet Number
CPU AND SUPPORT	
CPU (8Ø286)	2
Clock Generators (82284 and 8284A)	2
Numeric Processor Extension (8Ø287)	2
PROGRAMMABLE COMPONENTS	
PIT (8254)	9
PPI (8255A)	12
PSC (8274)	9
PIC -- Master (8259A)	7
PIC -- Slave (8259A)	9
Interrupt Jumper Matrix	7
MEMORY	
Local Memory	11
Dual-Port Memory	5
Primary Decode PAL U74	3
Secondary Decode PAL's U6Ø & U61	11
CONNECTORS	
P1 MULTIBUS Connector	5
P2 iLBX, Synchronous, or Aux. Interface	3
J1 Parallel Port	12
J2 Channel A Serial Port	1Ø
J3 Channel B Serial Port	9
J5 iSBX2	8
J6 iSBX1	8

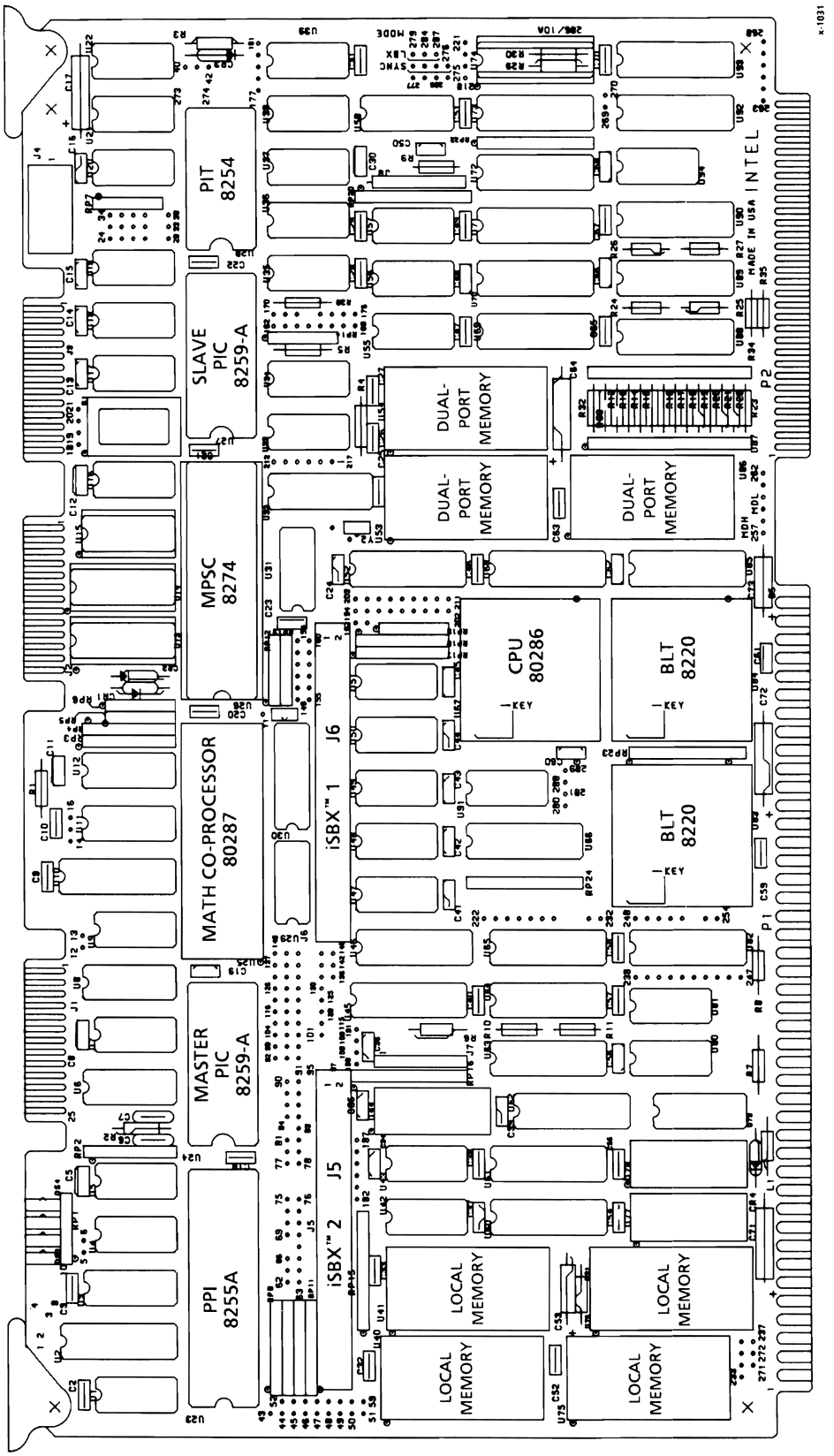


Figure 5-2. iSBC® 286/1ØA Single Board Computer Parts Location Diagram

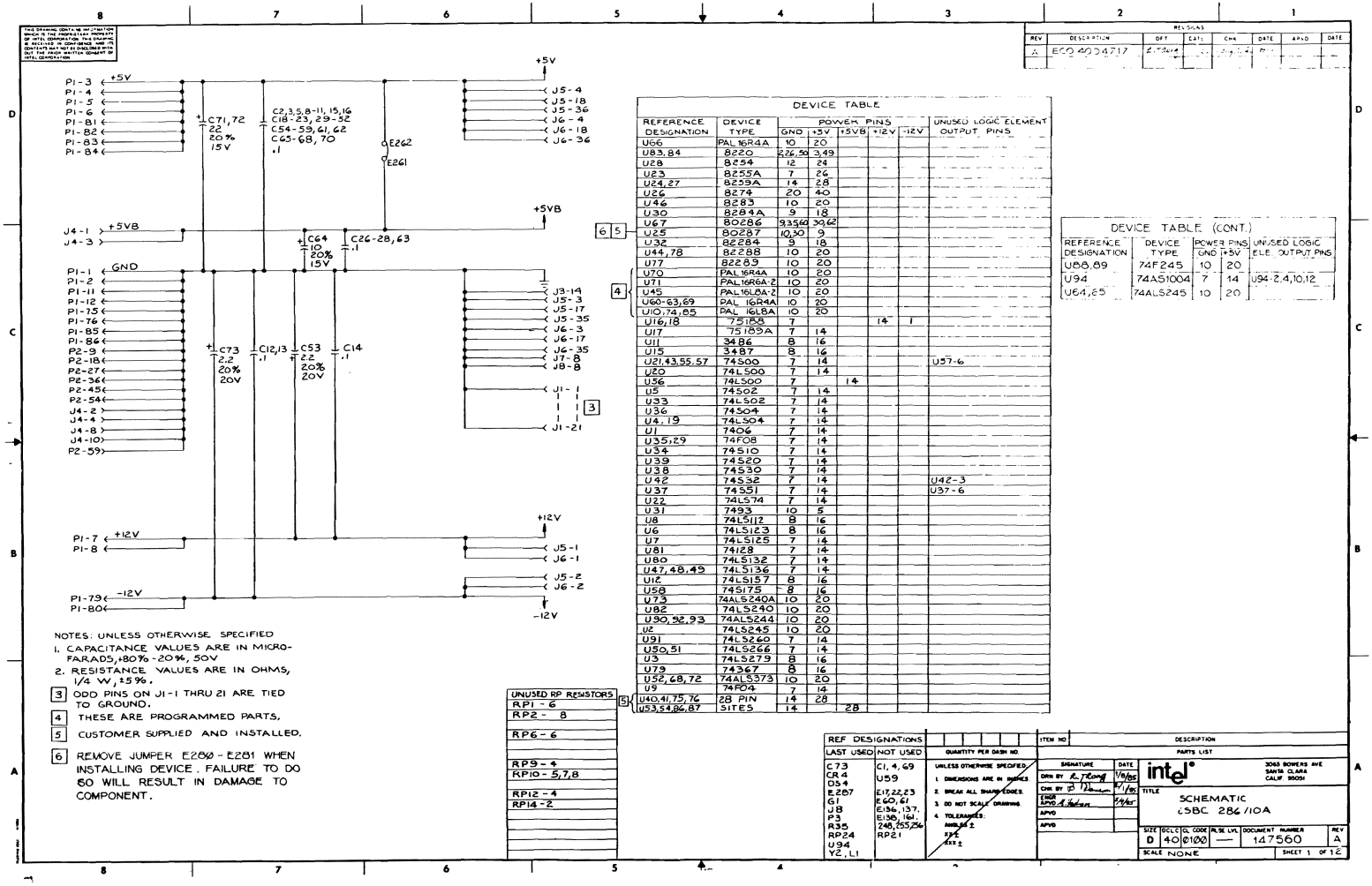


Figure 5-3. iSBC® 286/10A Single Board Computer Schematic Diagram (Sheet 1 of 12)

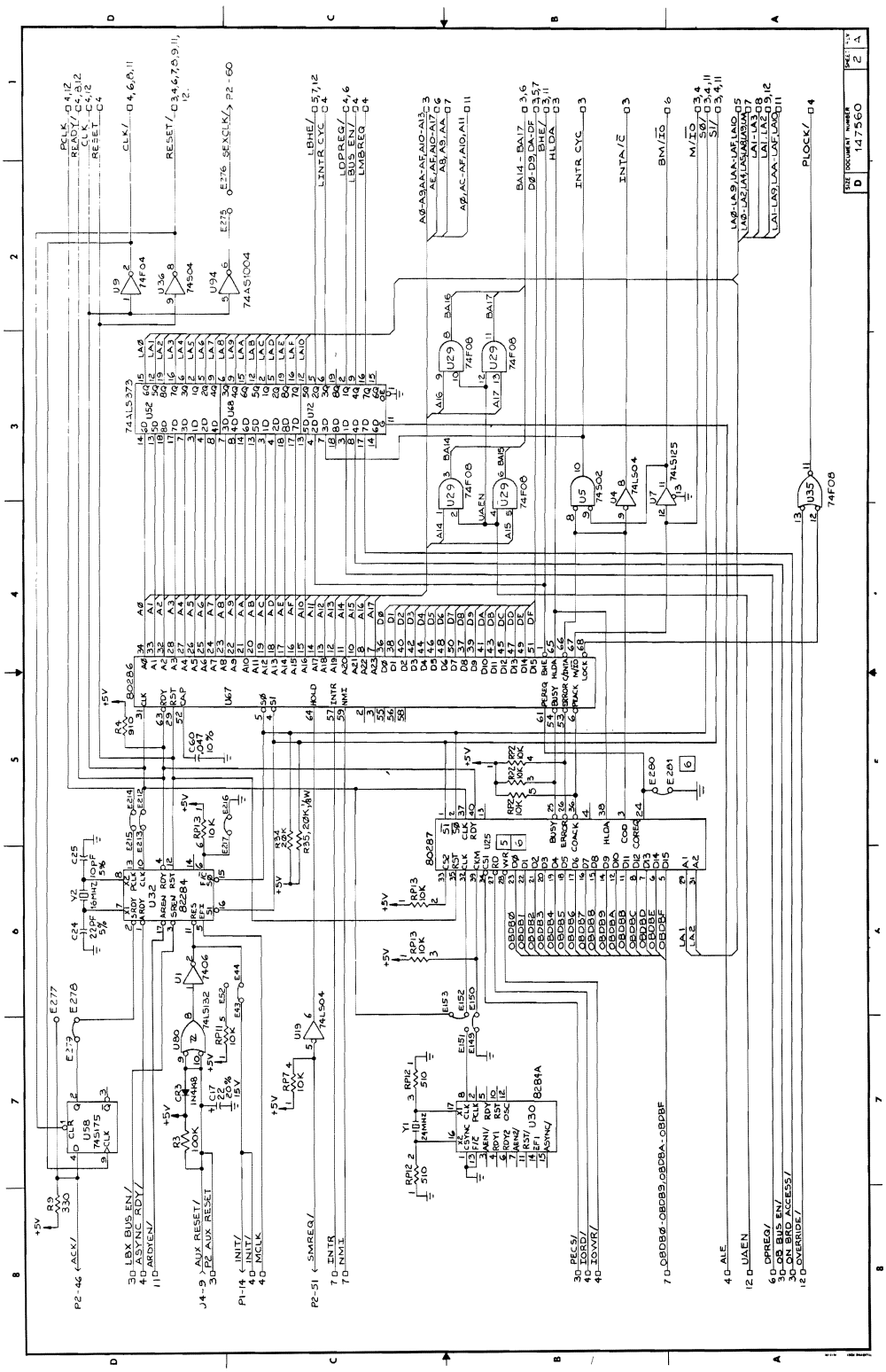


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 2 of 12)

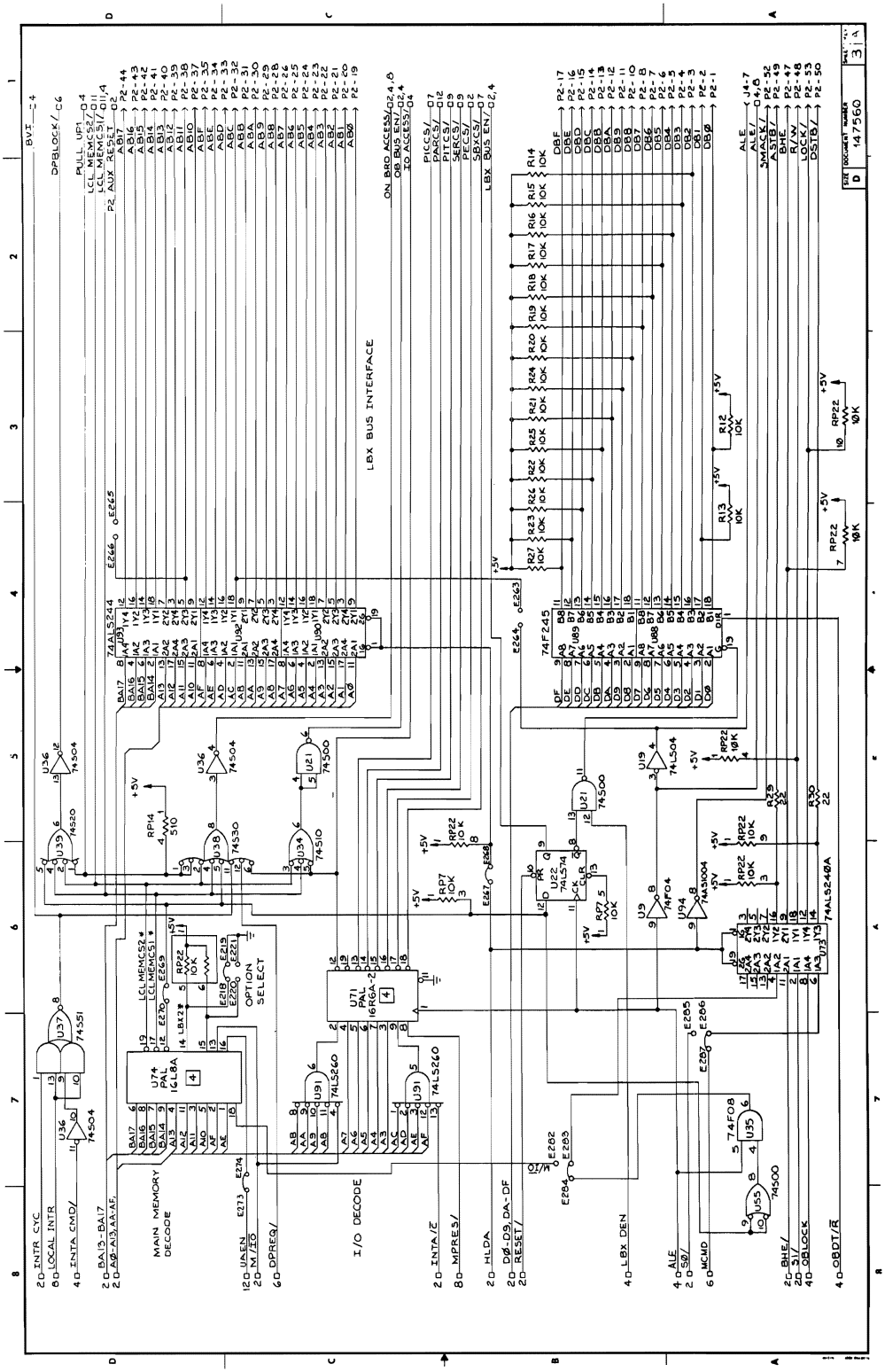


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 3 of 12)

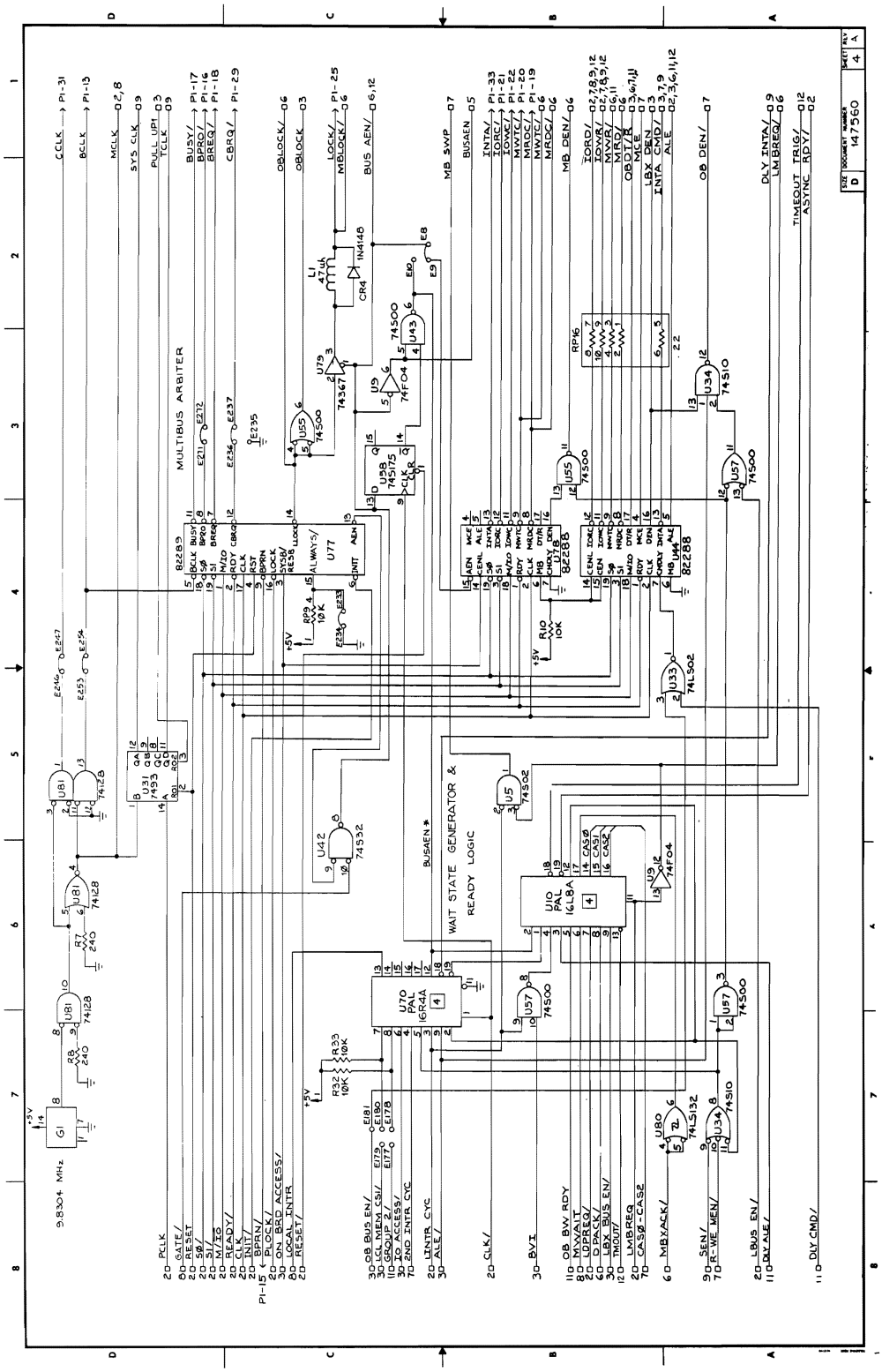


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 4 of 12)

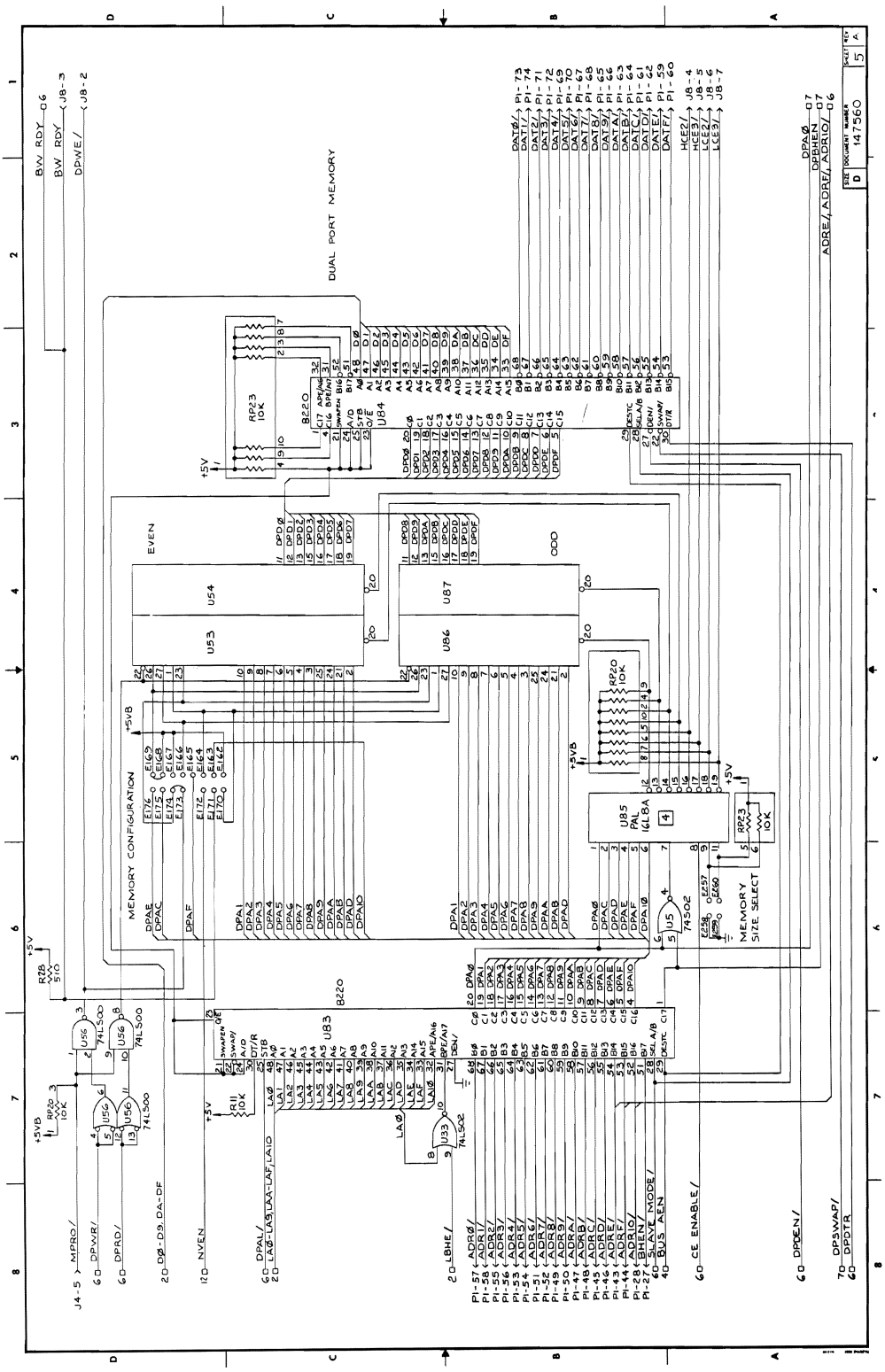


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 5 of 12)

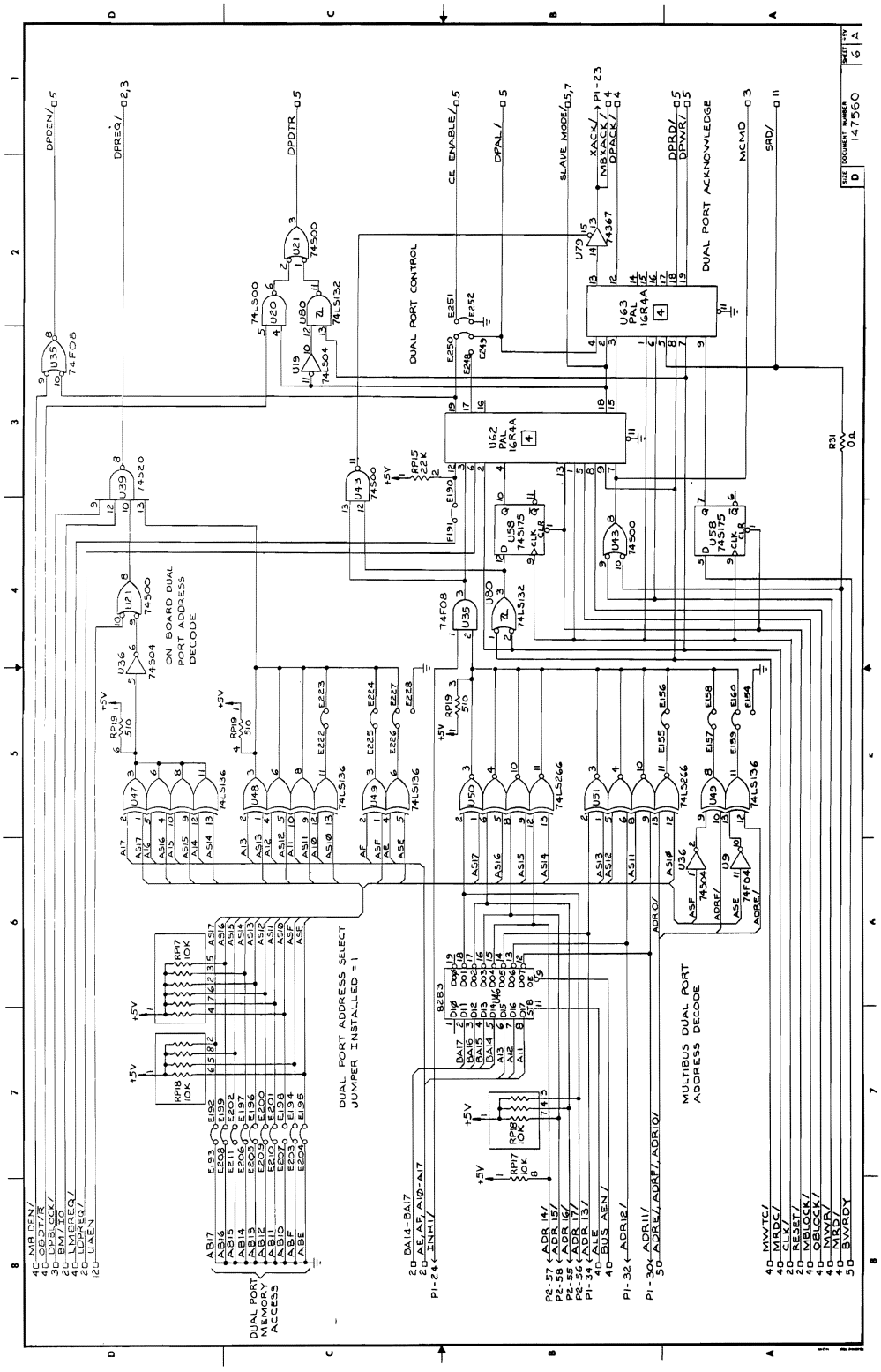


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 6 of 12)

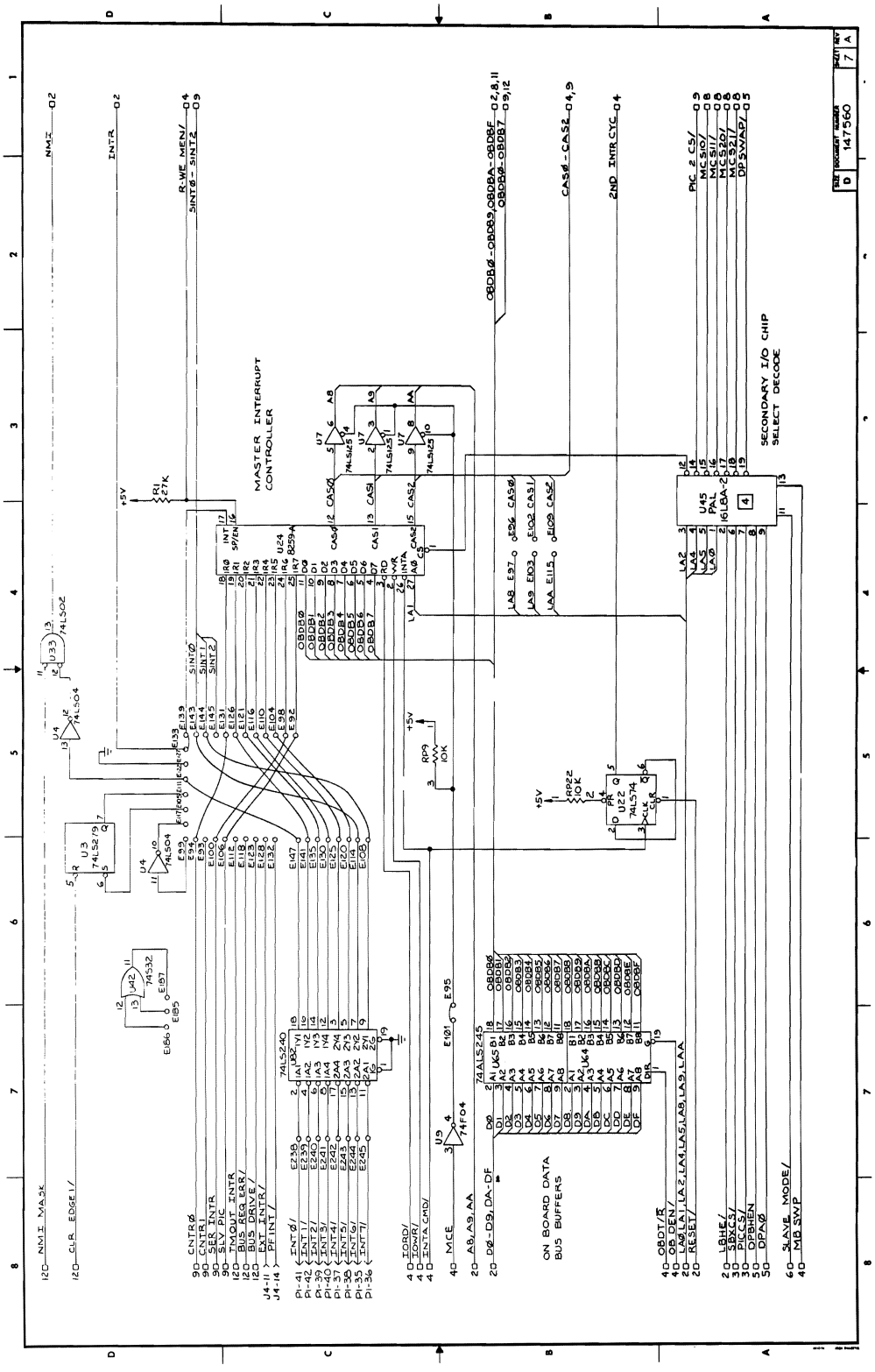


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 7 of 12)

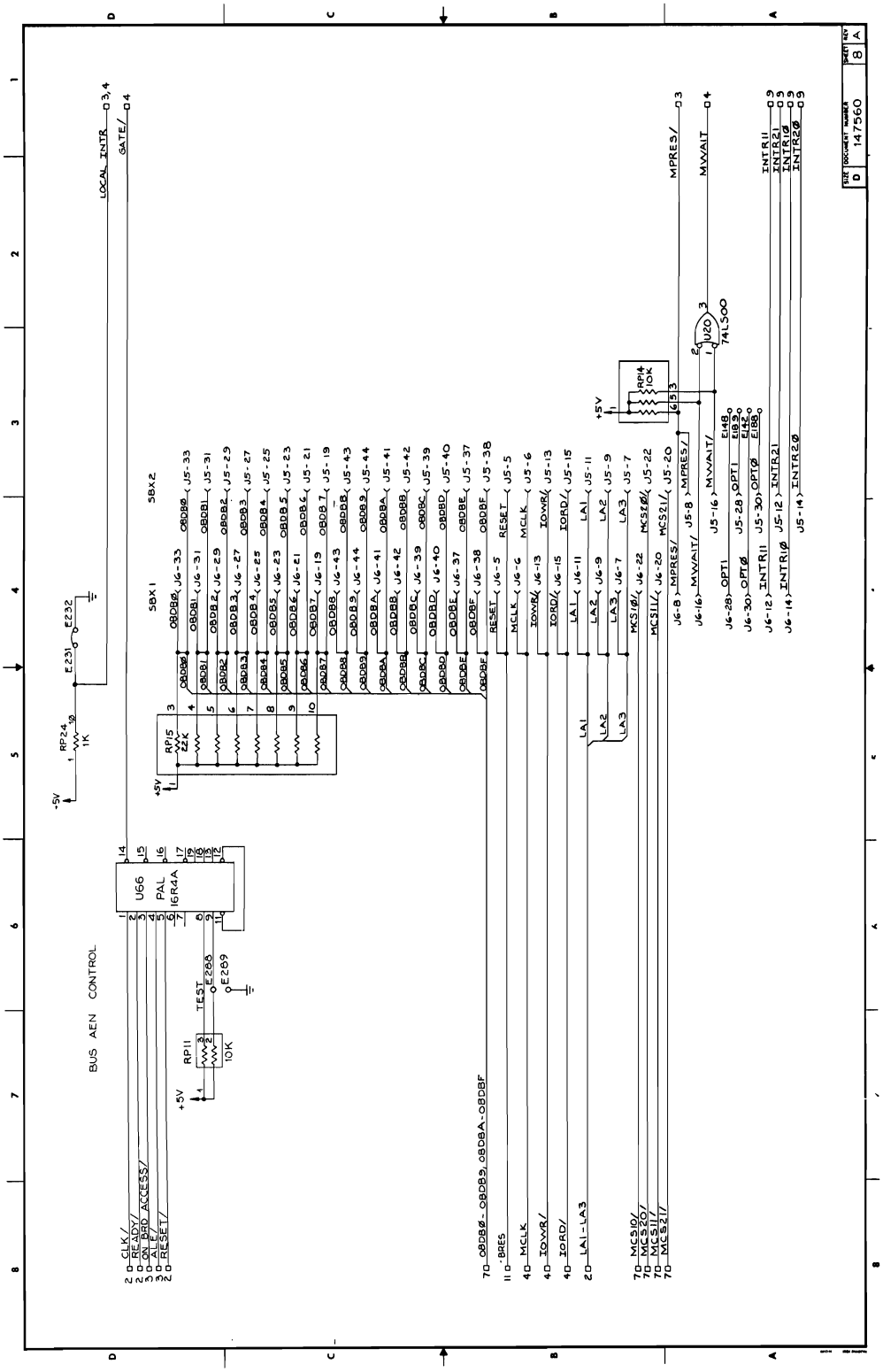


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 8 of 12)

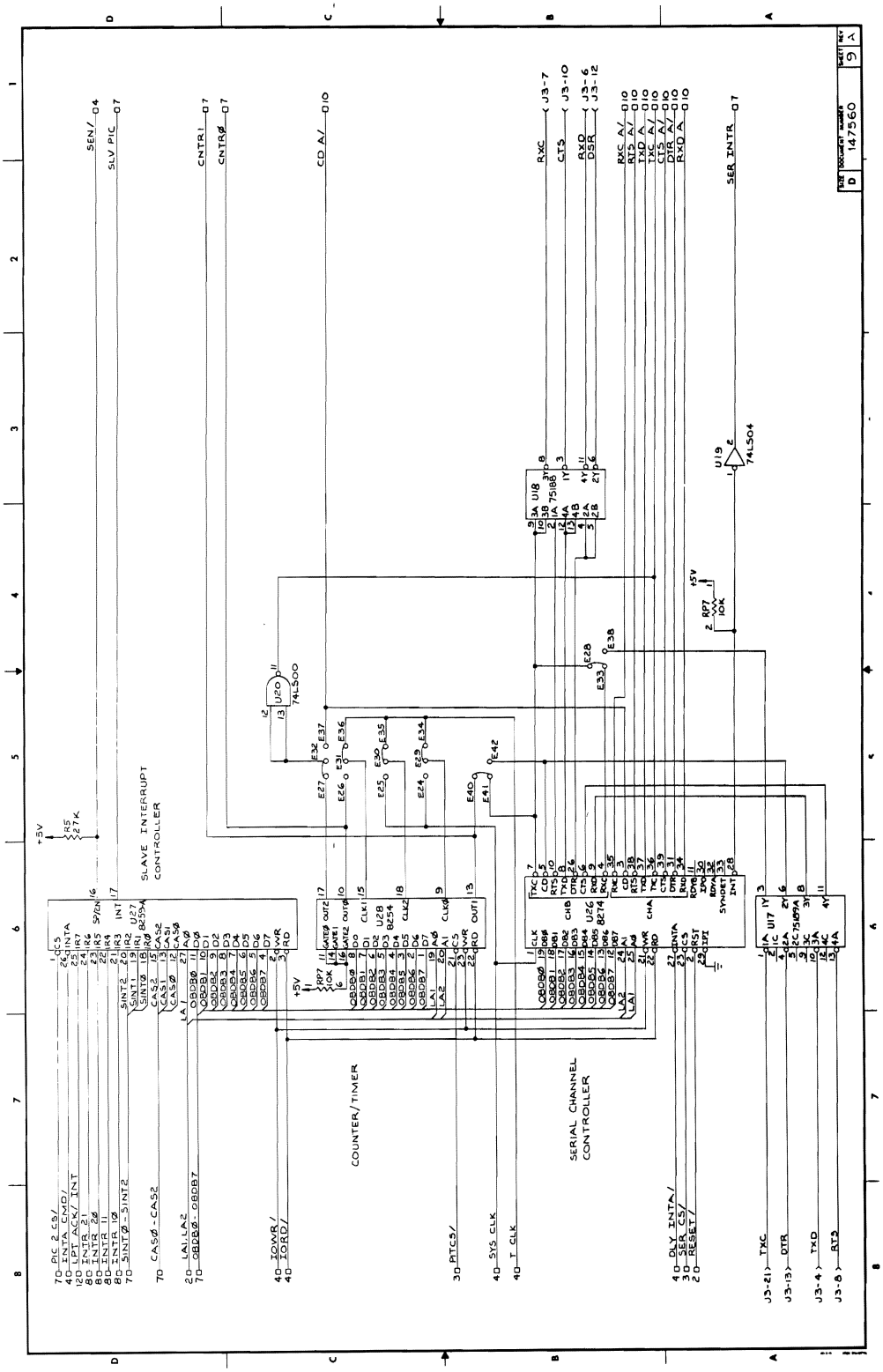


Figure 5-3. iSBC® 286/10A Single Board Computer Schematic Diagram (Sheet 9 of 12)

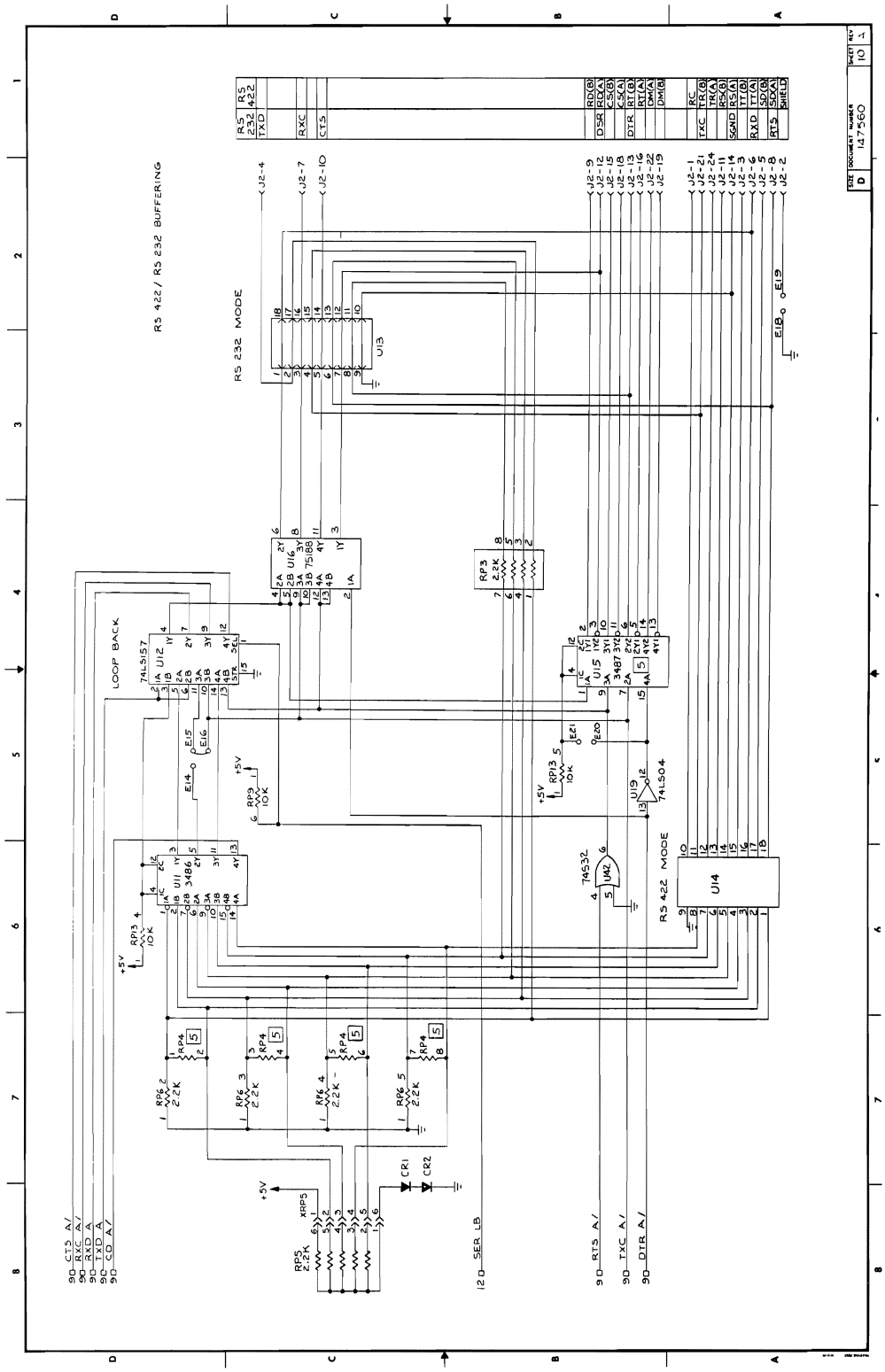


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 1Ø of 12)

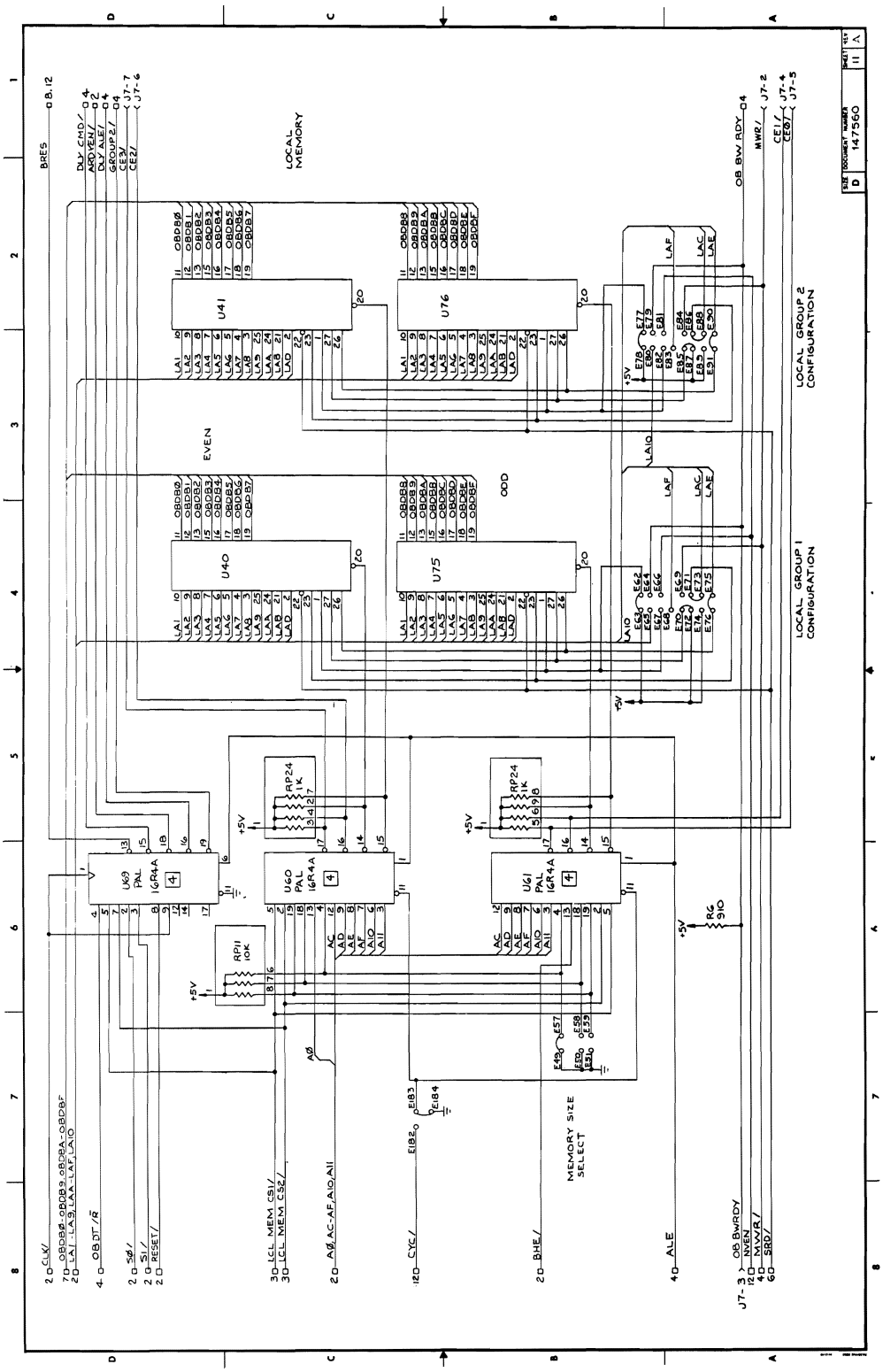


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 11 of 12)

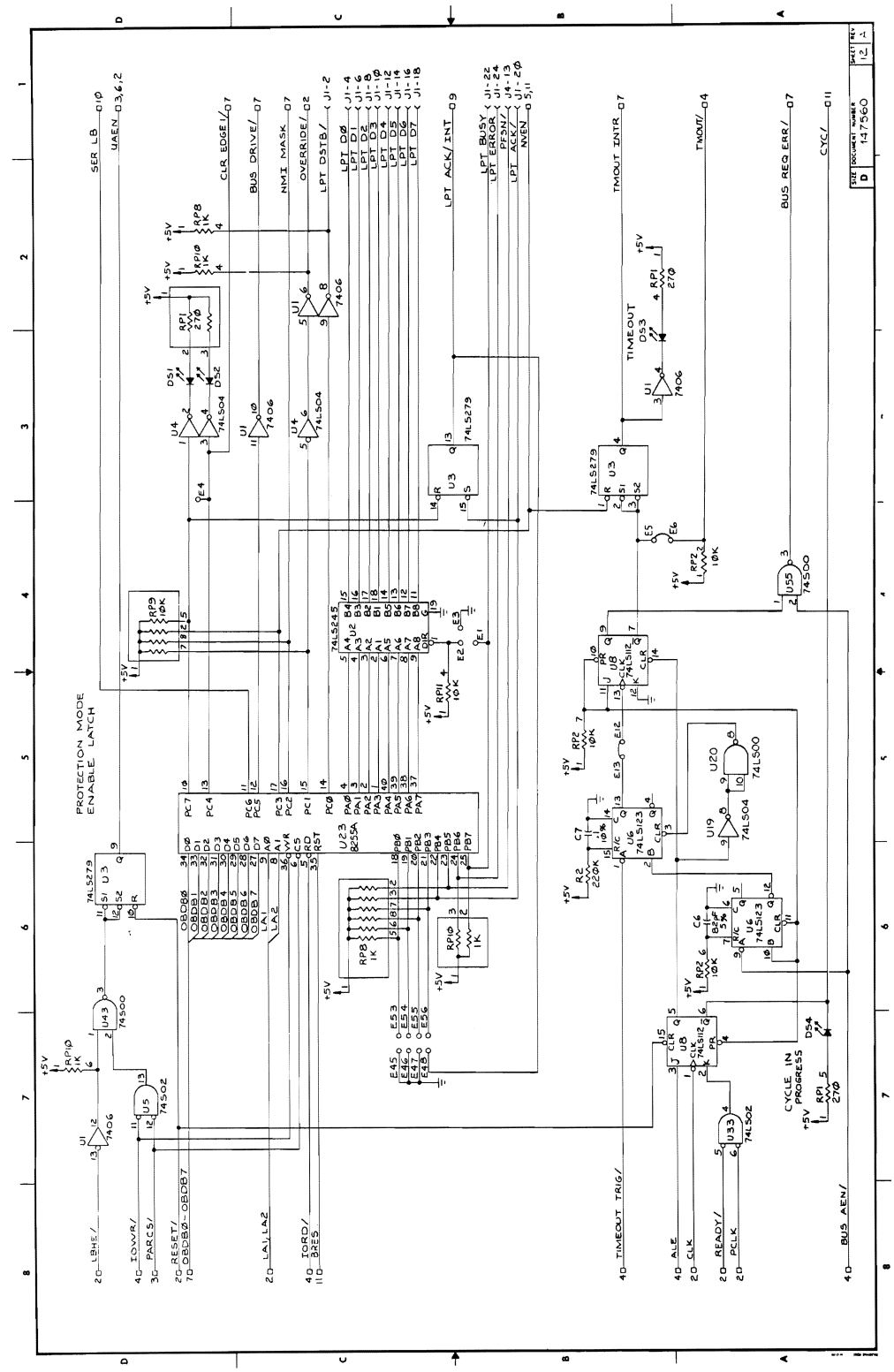


Figure 5-3. iSBC® 286/1ØA Single Board Computer Schematic Diagram (Sheet 12 of 12)

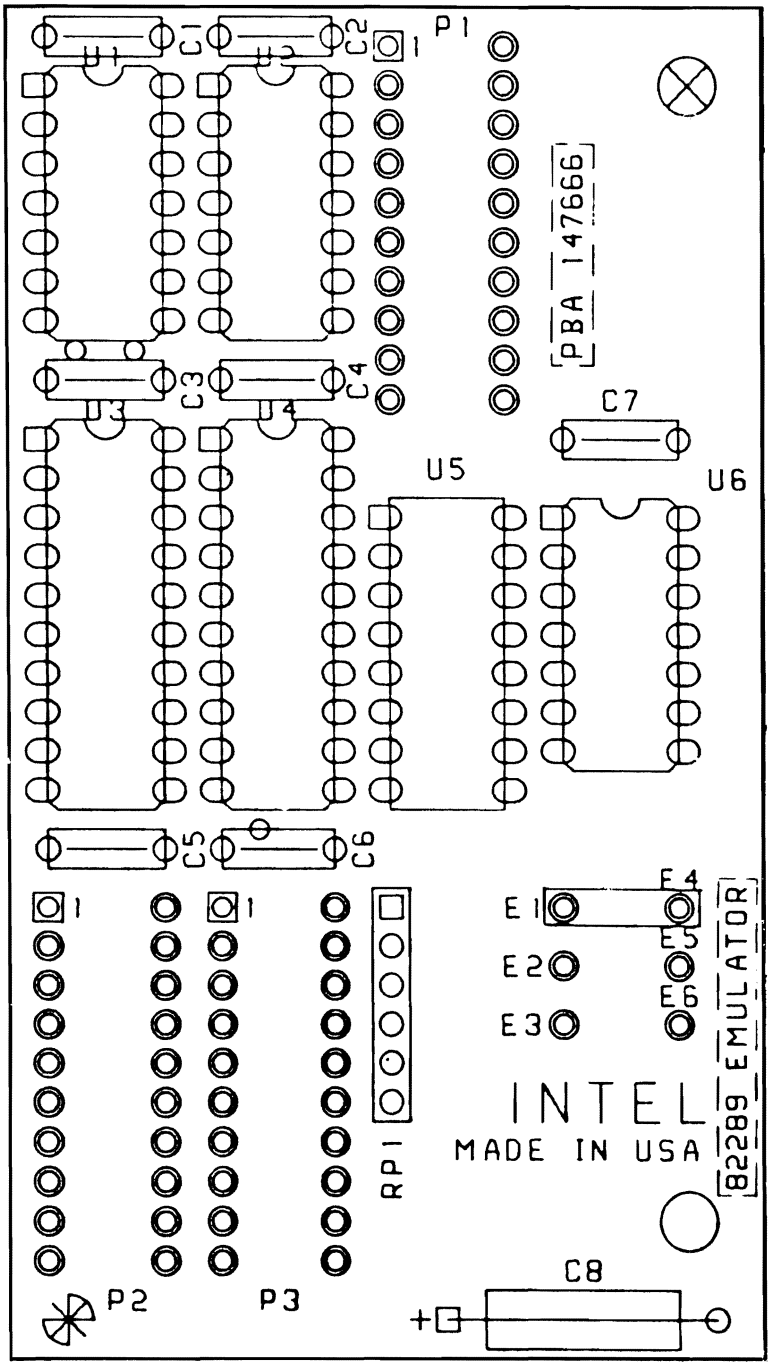
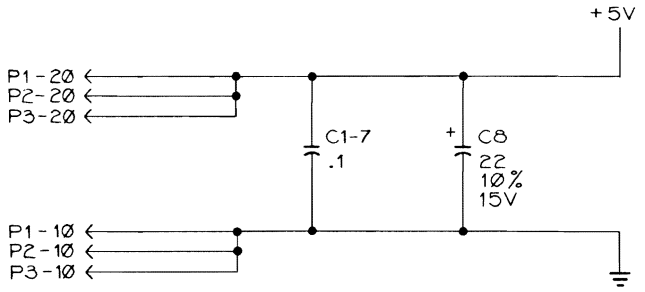


Figure 5-4. 82289 Emulator Parts Location Diagram



DEVICE TABLE				
REFERENCE DESIGNATION	DEVICE TYPE	POWER PINS		UNUSED LOGIC ELEMENT OUTPUT PINS
		GND	+5V	
U4	PAL16R6A	10	20	12,13,16
U3	8289	10	20	
U2	74F00	7	14	
U6	74F08	7	14	
U1	74F74	7	14	6,8
U5	DELAY LINE	8	16	

NOTES; UNLESS OTHERWISE SPECIFIED:
1. CAPACITOR VALUES ARE IN MICROFARADS, +80%, -20%, 50V.
2. RESISTOR VALUES ARE IN OHMS, 1/4 W, ± 1%.
[3] PROGRAMMED DEVICE.

Figure 5-5. 82289 Emulator Schematic Diagram (Sheet 1 of 2)

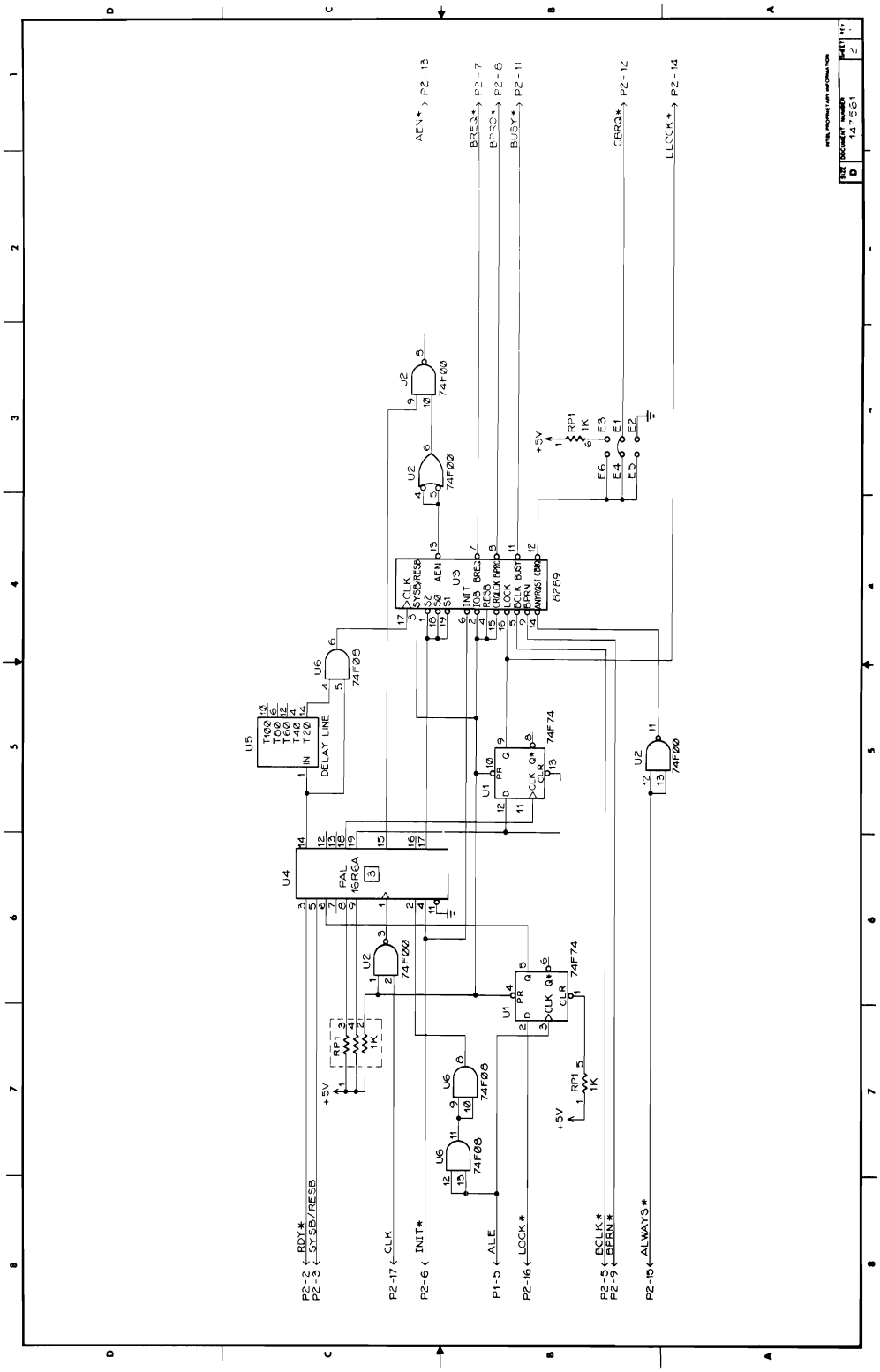


Figure 5-5. 82289 Emulator Schematic Diagram (Sheet 2 of 2)

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APPENDIX A
JUMPER INFORMATION

A.1 INTRODUCTION

This appendix provides an overview of the jumpers on the iSBC 286/1ØA board. The appendix is designed as a quick reference; refer to Chapter 4 for functional explanations. Figure A-1 shows the location of the jumpers on the iSBC 286/1ØA board. Table A-1 lists all jumpers and their functions, Table A-2 lists the stake-pin schematic index, and Table A-3 lists the default jumper schematic index.

Table A-1. Numerical List of Jumpers and their Functions

Jumper Number	Functions
E1	Access to the LPT BUSY signal from Connector J1
E2	Direction control input to printer interface
E3	Ground
E4	Access to bit 4 of Port C output
E5-E6§	Enable bus time-out when installed
E7	Not used
E8-E9§	AEN input to 82288 from 82289
E1Ø	Synchronized BUS AEN* signal
E11	Not used
E12-E13§	Test only
E14	Access to the TT signal for loopback
E15-E16§	Channel A loopback of TxC to RxC on the 8274 MPSC
E18-E19	Place a board ground onto J2 pin 2 for RS422A interfaces
E2Ø-E21	Allows using Connector J2 in an RS422A/449 interface in a multidrop application
E24	4 MHz clock SYS CLK
E25	4 MHz clock SYS CLK
E26	Output signal from Counter Ø of the PIT
E27-E32§	Connects the output from Counter 2 to the Transmit clock (TxC) input for Channel A of the 8274 MPSC
E28-E33§	Common RxC and TxC for Channel B, Connector J3 interface.
E29-E34§	Provides a 1.23 MHz clock signal (T CLK) for Counter Ø
E3Ø-E35§	Provides a 1.23 MHz clock signal (T CLK) for Counter 2
E31-E36§	Provides a 1.23 MHz clock signal (T CLK) for Counter 1
E37	Carrier Detect input to 8274 Channel A
E38	Transmit Clock input for Channel B of the 8274 MPSC
E39	Not used
E4Ø-E41§	Connects the output from Counter 1 to the Transmit clock (TxC) input for Channel B of the 8274 MPSC
E42	Carrier Detect input for Channel B of the 8274 MPSC
E43-E44§	MULTIBUS reset enable (INT*)
E45,E46,E47	Ground
E48	Access to the LPT ACK/INT signal to the printer interface
E49-E57§	Memory size select - secondary decode option select
E5Ø-E58	Memory size select - secondary decode option select
E51-E59	Memory size select - secondary decode option select
E53	Access to the Bit Ø input to Port B
E54	Access to the Bit 1 input to Port B
E55	Access to the Bit 2 input to Port B
E56	Access to the Bit 3 input to Port B

----------(continued)----------

Table A-1. Numerical List of Jumpers and their Functions (continued)

Jumper Number	Functions
E62 thru E76	Local Memory Socket Configuration - U4Ø/U75
E62-E63§	+5V to pin 1, 16Kx8 EPROM (27128)
E7Ø-E72§	+5V to pin 27, 16Kx8 EPROM (27128)
E71-E73§	LAC to pin 23, 16Kx8 EPROM (27128)
E75-E76§	LAE to pin 26, 16Kx8 EPROM (27128)
E77 thru E91	Local Memory Socket Configuration - U41/U76
E77-E78§	+5V to pin 1, 16Kx8 EPROM (27128)
E85-E87§	+5V to pin 27, 16Kx8 EPROM (27128)
E86-E88§	LAC to pin 23, 16Kx8 EPROM (27128)
E9Ø-E91§	LAE to pin 26, 16Kx8 EPROM (27128)
E92-E1Ø6§	Slave PIC INT to master PIC IR7
E93	Output from Counter 1 of the PIT
E94-E131§	Counter Ø Output (8254 PIT) to PIC U24, Level Ø
E95-E1Ø1§	Enables MCE to drive A8, A9, and AA.
E96	Test only
E97	Test only
E98-E1ØØ§	MPSC INT to Master PIC IR6
E99	Input to inverter U4
E1Ø2	Test only
E1Ø3	Test only
E1Ø4-E12Ø§	INT5* (MULTIBUS) to Master PIC IR5
E1Ø5	Input to edge-sense flip-flop U3
E1Ø7	Not used
E1Ø8-E144§	INT7* (MULTIBUS) to slave PIC IR1
E1Ø9	Test only
E11Ø-E125§	INT4* (MULTIBUS) to master PIC IR4
E111	Output from edge-sense flip-flop U3
E112	Time-out interrupt signal
E113	Not used
E114-E143§	INT6* (MULTIBUS) to slave PIC IRØ
E115	Test only
E116-E13Ø§	INT3* (MULTIBUS) to master PIC IR3
E117	Output from inverter U4
E118	Buss Request error sense indication
E119	Not used
E121-E135§	INT2* (MULTIBUS) to master PIC IR2
E122-E147§	INTØ* (MULTIBUS) to NMI
E123	Bus driver for reset or interrupt signal onto MULTIBUS interface
E124	Not used

----------(continued)----------

Table A-1. Numerical List of Jumpers and their Functions (continued)

Jumper Number	Functions
E126-E141§	INT1* (MULTIBUS) to master PIC IR1
E128	EXT INTR* signal from J4
E129	Not used
E132	PFINT* signal (power fail interrupt) from J4
E133-E139§	Master PIC INTR to 8Ø286 INTR
E134	Not used
E136	Not used
E137	Not used
E138	Not used
E14Ø	Not used
E142	OPTØ signal on iSBX Bus Connector J6
E145	SINT2 output from slave PIC
E146	Not used
E148	OPT1 signal on iSBX Bus Connector J6
E149 thru E153	Clock select for 8Ø287 math co-processor
E149-E15Ø§	Selects divide by 3 clock mode for 8Ø287
E151	8.Ø MHz clock for 8Ø287 CPU
E152-E153	Provides 16 MHz clock input into 8Ø287 (internal divide by 3 creates 5.33 MHz clock rate)
E154 thru E16Ø	Select a dual-port block size for the MULTIBUS interface E155-E156§ Part of binary decode for 16K block size E157-E158§ Part of binary decode for 16K block size E159-E16Ø§ Part of binary decode for 16K block size
E162 thru E176	Dual-Port Memory Socket Configuration - U53/U86 & U54/U87
E173-E174§	Dual-Port write enable (DPWE*) to pin 23, 2Kx8 SRAM
E168-E169§	+5V to pin 26, 2Kx8 SRAM
E177 thru E181	Wait-state select inputs for PAL U7Ø
E182	Access to cycle-in-progress monitoring logic
E183-E184§	Chip enable
E185	Input to OR-gate U42
E186	Input to OR-gate U42

----------(continued)----------

Table A-1. Numerical List of Jumpers and their Functions (continued)

Jumper Number	Functions
E187	Output from OR-gate U42
E188	OPTØ signal on iSBX Bus Connector J5
E189	OPT1 signal on iSBX Bus Connector J5
E19Ø-E191§	Allows CPU to remove on-board LOCK signal
E192 thru E21Ø	Starting Address for Dual-Port Memory
E192-E183§	Megabyte page select
E194-E2Ø3§	16K boundary select, XXCØØØH
E195-E2Ø4§	16K boundary select, XXCØØØH
E196-E2Ø5§	64K page select
E197-E2Ø6§	Megabyte page select
E199-E2Ø8§	Megabyte page select
E2ØØ-E2Ø9§	64K page select
E2Ø1-E21Ø§	64K page select
E2Ø2-E211§	Megabyte page select
E212-E213§	16 MHz clock to CPU (internal divide by 2 for 8 MHz)
E214-E215§	Enable PCLK to MULTIBUS interface
E216-E217§	CPU clock select; out = 9.83 MHz from EFI, in = 16.Ø MHz from crystal
E218-E219§	SELØ for U74 main memory decode
E22Ø-E221	SEL1 for U74 main memory decode
E222 thru E228	Dual-Port Block Size for the On-Board CPU
E222-E223§	Dual-Port 64K Decode
E224-E225§	Dual-Port 32K Decode
E226-E227§	Dual-Port 16K Decode
E229	Not used
E23Ø	Not used
E231-E232§	
E233-E234§	ALWAYS* tied to ground
E235	Ground connection
E236-E237§	Enable CBRQ* signal to MULTIBUS interface
E238	Interrupt input INTØ* from MULTIBUS interface
E239	Interrupt input INT1* from MULTIBUS interface
E24Ø	Interrupt input INT2* from MULTIBUS interface
E241	Interrupt input INT3* from MULTIBUS interface
E242	Interrupt input INT4* from MULTIBUS interface
E243	Interrupt input INT5* from MULTIBUS interface
E244	Interrupt input INT6* from MULTIBUS interface
E245	Interrupt input INT7* from MULTIBUS interface
E246-E247§	Enable CCLK signal to MULTIBUS interface

----------(continued)----------

Table A-1. Numerical List of Jumpers and their Functions (continued)

Jumper Number	Functions
E248 thru E252	Select iRAM Devices for Dual-Port Memory
E249-E25Ø§	DPAL*, dual-port control
E251-E252§	Chip Enable
E253-E254§	Enable BCLK* signal to MULTIBUS interface
E257-E258	Memory size input to PAL U85
E259-E26Ø	Memory size input to PAL U85
E261-E262§	+5VB (battery back-up) to +5V
E263-E264	Place the ALE signal onto P2 pin 32
E265-E266	Place the P2 AUX RESET signal on P2 pin 38
E267-E268§	Enables iLBX bus drivers and receivers
E269-E27Ø§	Enables iLBX bus memory addresses
E271-E272§	Enable BPRO* signal to MULTIBUS interface
E273-E274§	Enables UAEN (upper address enable -- upper 4 bits)
	Synchronous Interface Mode
E275-E276	Processor Clock for synchronous interface
E277-E278	ACK* directly to 82284
E282-E283	M/IO to P2-49
E285-E286	SØ* to P2-5Ø
	iLBX Interface Mode
E278-E279§	Synchronized ACK* to 82284
E283-E284§	ASTB* to P2-49
E286-E287§	DSTB* to P2-5Ø
E275-E276	Removed
E28Ø-E281§	Disables 8Ø287 interface (remove before installing 8Ø287)
E288-E289	Remove if using dual-port memory Install if not using dual-port memory (removes a wait-state for MULTIBUS accesses)

Note: § identifies default configuration.

Table A-2. Stake Pin Schematic Index

E1–E6 /12	E7 /np	E8–E1Ø /4	E11 /np
E12–E13 /12	E14–E16 /1Ø	E17 /np	E18–E21 /1Ø
E22–E23 /np	E24–E38 /9	E39 /np	E4Ø–E42 /9
E43–E44 /2	E45–E48 /12	E49–E51 /11	E52 /2
E53–E56 /12	E57–E59 /11	E6Ø–E61 /np	E62–E91 /11
E92–E1Ø6 /7	E1Ø7 /np	E1Ø8–E112 /7	E113 /np
E114–E118 /7	E119 /np	E12Ø–E123 /7	E124 /np
E125–E128 /7	E129 /np	E13Ø–E133 /7	E134 /np
E135 /7	E136–E138 /np	E139 /7	E14Ø /np
E141 /7	E142 /8	E143–E145 /7	E146 /np
E147 /7	E148 /8	E149–E153 /2	E154–E16Ø /6
E161 /np	E162–E176 /5	E177–E181 /4	E182–E184 /11
E185–E187 /7	E188–E189 /8	E19Ø–E211 /6	E212–E217 /2
E218–E221 /3	E222–E228 /6	E229–E23Ø /np	E231–E232 /8
E233–E237 /4	E238–E245 /7	E246–E247 /4	E248–E252 /6
E253–E254 /4	E255–E256 /np	E257–E26Ø /5	E261–E262 /1
E263–E27Ø /3	E271–E272 /4	E273–E274 /3	E275–E281 /2
E282–E287 /3	E288–E289 /8		

Note: The table format: stake pin(s)/schematic sheet number
np means no stake pin on the board.

Table A-3. Default Jumper Listing and Schematic Index

E5–E6 /12	E8–E9 /4	E12–E13 /12	E15–E16 /1Ø
E27–E32 /9	E28–E33 /9	E29–E34 /9	E3Ø–E35 /9
E31–E36 /9	E4Ø–E41 /9	E43–E44 /2	E49–E57 /11
E62–E63 /11	E7Ø–E72 /11	E71–E73 /11	E75–E76 /11
E77–E78 /11	E85–E87 /11	E86–E88 /11	E9Ø–E91 /11
E92–E1Ø6 /7	E94–E131 /7	E95–E1Ø1 /7	E98–E1ØØ /7
E1Ø4–E12Ø /7	E1Ø8–E144 /7	E11Ø–E125 /7	E114–E143 /7
E116–E13Ø /7	E121–E135 /7	E122–E147 /7	E126–E141 /7
E133–E139 /7	E149–E15Ø /2	E152–E153 /2	E155–E156 /6
E157–E158 /6	E159–E16Ø /6	E168–E169 /5	E173–E174 /5
E183–E184 /11	E19Ø–E191 /6	E192–E193 /6	E194–E2Ø3 /6
E195–E2Ø4 /6	E196–E2Ø5 /6	E197–E2Ø6 /6	E199–E2Ø8 /6
E2ØØ–E2Ø9 /6	E2Ø1–E21Ø /6	E2Ø2–E211 /6	E212–E213 /2
E214–E215 /2	E216–E217 /2	E218–E219 /3	E222–E223 /6
E224–E225 /6	E226–E227 /6	E231–E232 /8	E233–E234 /4
E236–E237 /4	E246–E247 /4	E249–E25Ø /6	E251–E252 /6
E253–E254 /4	E261–E262 /1	E267–E268 /3	E269–E27Ø /3
E271–E272 /4	E273–E274 /3	E278–E279 /2	E28Ø–E281 /2
E283–E284 /3	E286–E287 /3		

Note: The table format: jumper/schematic sheet number

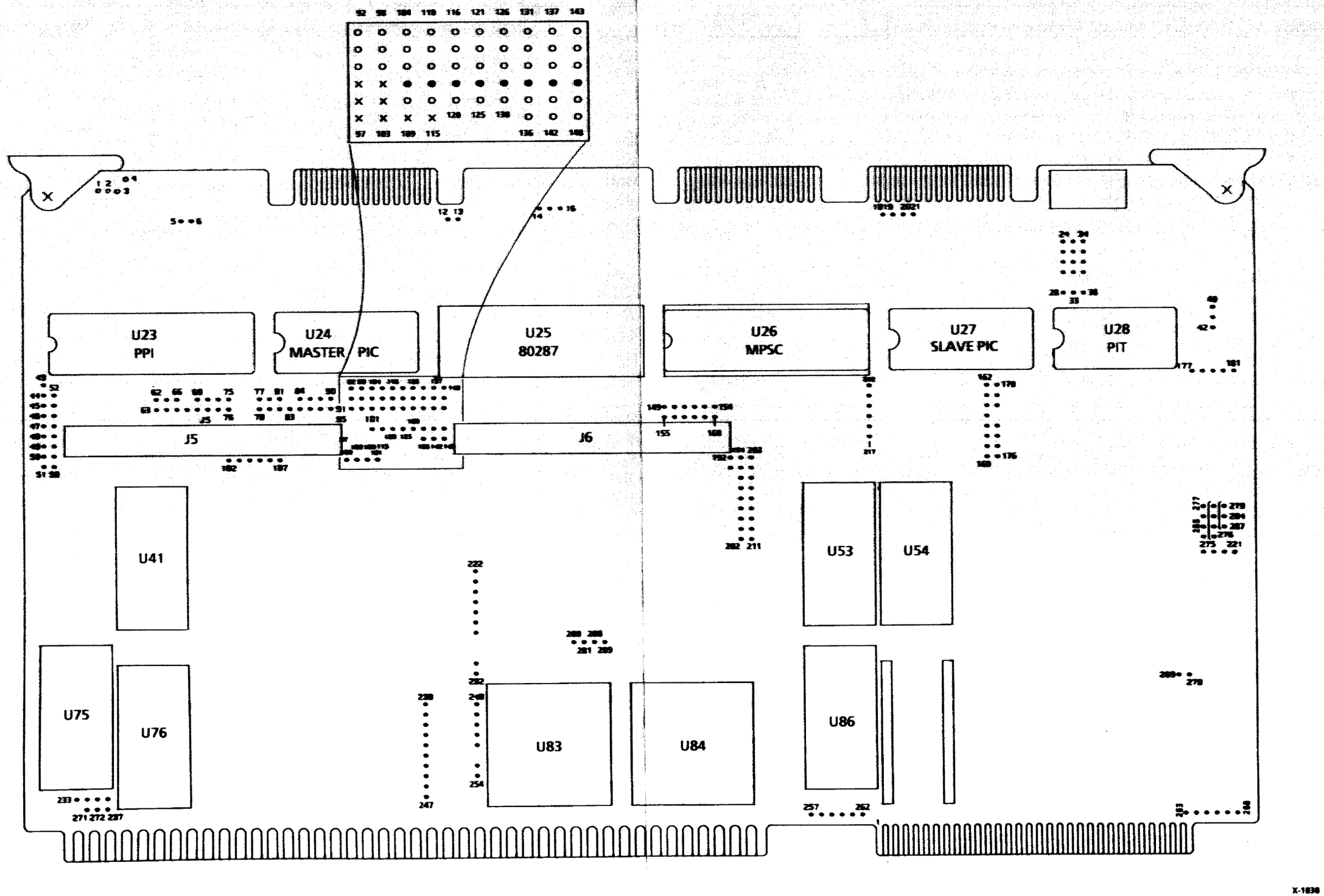

Figure A-1. iSBC 286/1ØA® Board Jumper Post Location Diagram

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APPENDIX B
MULTIDROP CONSIDERATIONS

B.1 INTRODUCTION

The iSBC 286/1ØA Single Board Computer lends itself readily to configuration for a multidrop application. This appendix shows an example for configuring Connector J2 for operation in a full-duplex RS422A/449 multidrop application. Some of the line conditioning considerations you must make in configuring the board for a multidrop application are as follows:

- You must calculate the value of the bias resistors for installation at the master unit in the system.

- You must calculate the value of the termination resistors for installation at the farthest slave unit in the system.

Figure B-1 shows a typical RS422A/449 full-duplex multidrop configuration that assumes only one master station is attached to the system and always drives the output lines. A full-duplex system allows a slave to listen to the data line and to perform some task in parallel with a task performed on another slave, but only the selected slave may transmit to the master. This example is for a system with four stations; however, the slaves are under strict program control to output only on command from the master. If more than four stations are connected in a system, you must refigure the resistance value.

You can configure a simpler RS422A/449 multidrop system for half-duplex operation; however, the protocol is more strict. A half-duplex configuration requires two data lines (to carry a differential signal) and a ground line (return) between the master and all slaves in the system. Recall, however, that a major restriction of a half-duplex system is its limitation to communicate in only one direction at a time.

For all practical purposes, the half-duplex system allows no priority for masters and slaves; all units may listen to whomever is using the data line. This presents a programming constraint in that the system software protocol for half-duplex operation must be designed to allow only one unit to transmit at any given instant.

B.2 JUMPER CONFIGURATION

The default configured board is not configured for operation in a multidrop application: jumper E2Ø-E21 is not installed. By connecting E2Ø-E21, the 8274 MPSC can enable the output drivers on the iSBC 286/1ØA board whenever the DTR signal is active. You tri-state the drivers by deactivating DTR. You must install E2Ø-E21 on each master if your system uses multiple iSBC 286/1ØA boards. If your system uses multiple iSBC 286/1ØA boards as slave devices, you must install E2Ø-E21 on each slave board.

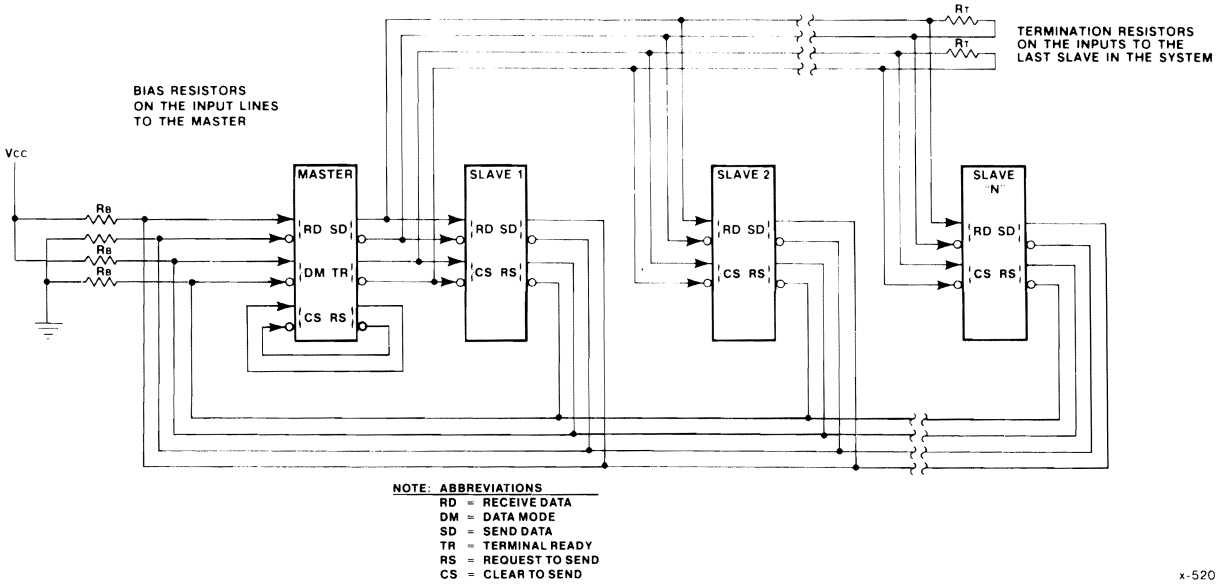

Figure B-1. Full-Duplex RS422A/449 Multidrop Configuration Example

B.3 MULTIDROP BIAS RESISTOR REQUIREMENT

In an RS422A/449 multidrop application, it is strongly recommended that the open or floating data lines in the system be biased by means of user-supplied bias resistors, as shown in Figure B-2. The default configured board contains 2.2K ohm bias resistors (RP5 and RP6). Without the bias resistors, the state of a floating line cannot be guaranteed. You must install RP5/RP6 on the master and remove RP5/RP6 from all slaves.

The exact value of the bias resistors may be calculated only on an individual application basis since the controlling parameters will vary from one application to another. The following procedure steps through an example for calculating the bias resistance required to dissipate the leakage currents encountered in a typical full-duplex RS422A/449 multidrop application. The procedure determines both the best case and the worst case resistor values; any resistor value that satisfies both cases may be installed onto the iSBC 286/1ØA board as a bias resistor.

Using the configuration shown in Figure B-2, the value of the bias resistors must be calculated for two conditions:

1. When the lines are tri-stated

2. When the lines are driven to the marking (off) state

When the lines are tri-stated, assume the following conditions:

1. $V_A - V_B \geq Ø.3V$ to guarantee differential voltage for a "spacing" (on) condition.

2. All drivers are tri-stated.

3. Driver leakage current (I_{LEAK}) is $\pm$ 1ØØ mA for each driver (reference RS422 specification).

4. The general equation for the input current to the receiver is

$$\text{for Iin = positive (into device)} \qquad I = \frac{V + 3 \text{ volts}}{4K \text{ ohms}}$$

$$\text{for Iin = negative} \qquad I = \frac{V - 3 \text{ volts}}{4K \text{ ohms}}$$

(reference RS422 Specification).

5. No common mode voltage occurs between drivers and receivers.

6. Assume $V_A \geq 2.6V$ and $V_B \leq 2.3V$.

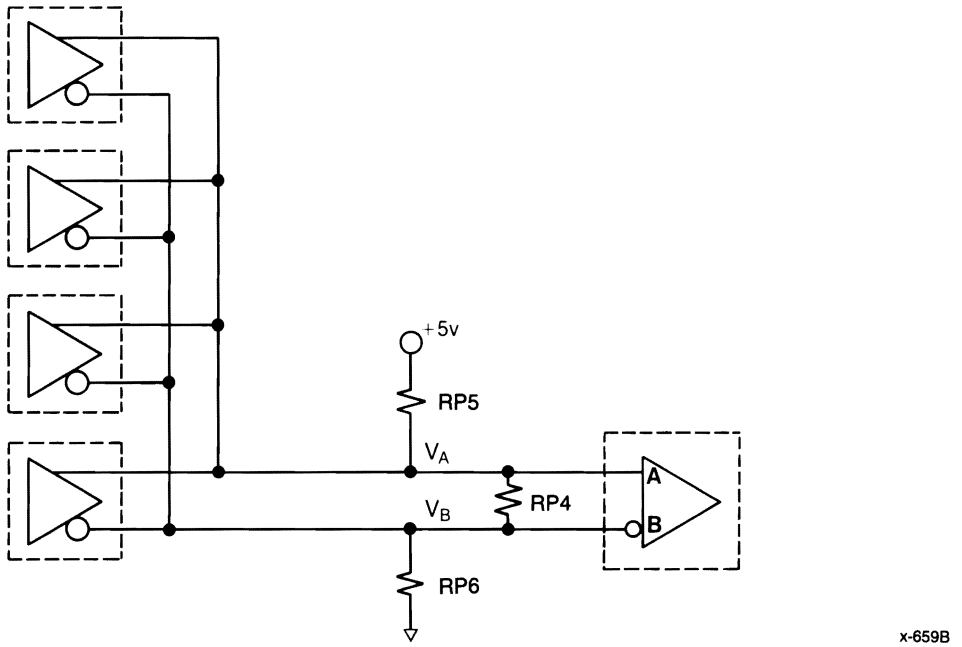

Figure B-2. System Example - Bias and Terminator Resistor Placement

B.4 CASE 1: LINES FLOATING

To calculate the maximum value of RP5 and RP6, we must calculate the resistance required to guarantee at least a Ø.3 volt differential between the lines when they are tri-stated.

Referring to the previous general receiver input current equation:

$$Iin(A) = \frac{V_A + 3V}{4K\ ohms} = \frac{(2.6 + 3)V}{4K\ ohms} = + 1.4mA$$

$$Iin(B) = \frac{V_B - 3V}{4K\ ohms} = \frac{(2.2 - 3)V}{4K\ ohms} = - .18mA$$

Referring to Figure B-3:

$$I_T = \frac{V_A - V_B}{RP4} = \frac{(2.6 - 2.3)V}{RP4} = \frac{.3V}{RP4}$$

with the termination resistance RP4 = 1ØØ ohms, I_T = 3mA.

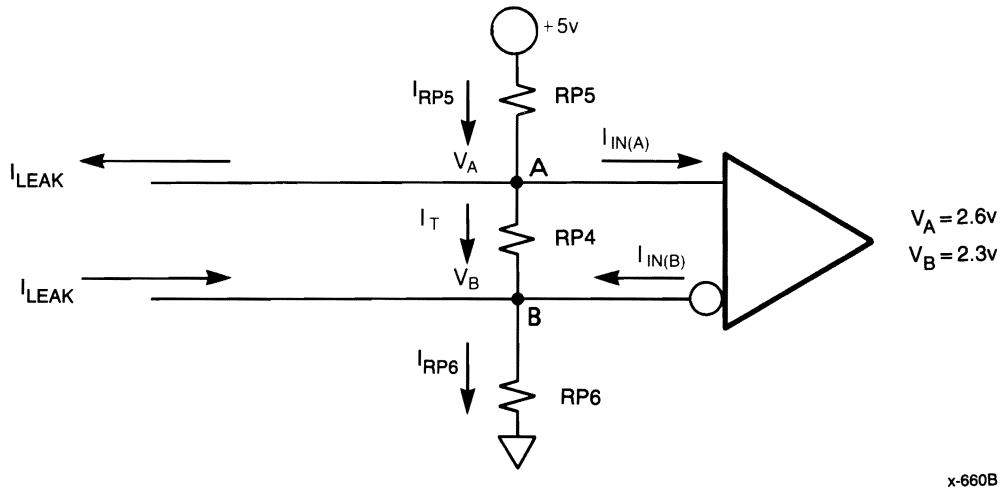

Figure B-3. Case 1 Example (Lines Floating)

Writing the node equation for Node A:

$$I_{RP5} = I_{in}(A) + I_{LEAK} + I_T$$

$$= 1.4mA + (1ØØmA \times 4 \text{ devices}) + 3mA$$

$$I_{RP5} = 4.8mA$$

$$\text{To keep } V_A \geq 2.6V, \quad RP5 \leq \frac{5 - V_A}{I_{RP5}} = \frac{(5 - 2.6)V}{4.8mA}$$

$$RP5 \leq 5ØØ \text{ ohms}$$

Writing the node equation for Node B:

$$I_{RP6} = I_{in}(B) + I_{LEAK} + I_T$$

$$= .18mA + 4ØØmA + 3mA = 3.58mA$$

$$\text{To keep } V_B \leq 2.3V,\ RP6 \leq \frac{V_B}{I_{RP6}} = \frac{2.3V}{3.58mA},\quad RP6 \leq 642 \text{ ohms}$$

B.5 CASE 2: LINES DRIVEN

The driver will control the lines to either a marking (off) or a spacing (on) state. The resistor values needed for the spacing state were previously calculated in Case 1. For the resistor values needed in the marking state, $V_B - V_A \geq Ø.3$ volts must be guaranteed as well as the following assumptions:

1. Assume $V_A \leq 2.3$ volts, $V_B \geq 2.6$ volts.
2. The general receiver input current equations are the same as in Case 1.
3. Driver output current is +2ØmA (I_{OL}) and -2ØmA (I_{OH}).
4. Driver leakage currents are negligible in relation to the drive current of the enabled driver.
5. No common mode voltage occurs between the driver and receiver.

Referring to the general receiver input current equation:

$$I_{in(A)} = \frac{V_A - 3V}{4K} = \frac{(2.3 - 3)V}{4K} = -.18mA$$

$$I_{in(B)} = \frac{V_B + 3V}{4K} = \frac{(2.6 + 3)V}{4K} = 1.4mA$$

Referring to Figure B-4:

$$I_T = \frac{V_B - V_A}{RP4} = \frac{(2.6 - 2.3)V}{1ØØ \text{ ohms}} = 3 \text{ mA}$$

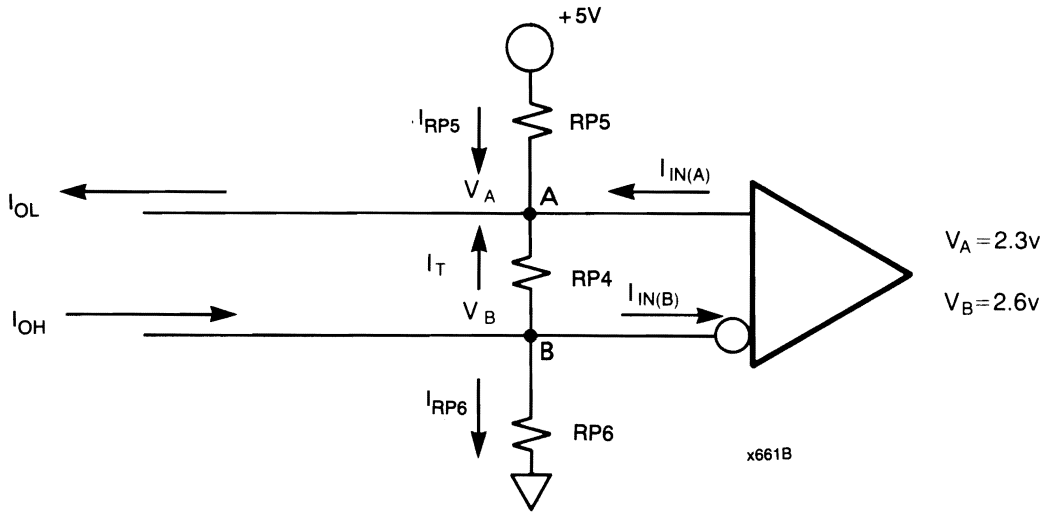

Figure B-4. Case 2 Example (Lines Driven)

Writing the node equation for Node A and referring to Figure B-4 we have:

$$I_{RP5} + I_{in}(A) + I_T \leq I_{OL}$$

$$I_{RP5} \leq I_{OL} - I_T - I_{in}(A)$$

$$I_{RP5} \leq 2\text{Ø}mA - 3mA - .18mA$$

$$I_{RP5} \leq 16.8mA$$

and,

$$\frac{5V - V_A}{RP5} \leq I_{RP5} \quad \text{so that RP5} \geq \frac{5V - V_A}{16.8\ mA}, \quad \text{RP5} \geq 161 \text{ ohms}$$

Writing the node equation for Node B:

$$I_{RP6} + I_T + I_{in}(B) \leq I_{OH}$$

$$I_{RP6} \leq I_{OH} - I_T - I_{in}(B)$$

$$I_{RP6} \leq 20mA - 3mA - 1.4mA$$

$$I_{RP6} \leq 15.6mA$$

$$I_{RP6} = \frac{V_B}{RP6} \leq 15.6mA$$

$$RP6 \geq \frac{V_B}{I_{RP6}} \geq \frac{2.6V}{15.6mA}$$

$$RP6 \geq 167 \text{ ohms}$$

Combining these results we find:

$$167 \text{ ohms} \leq RP6 \leq 638 \text{ ohms}$$

$$161 \text{ ohms} \leq RP5 \leq 500 \text{ ohms}$$

The values for RP5 and RP6 should be equal and near the top of the resistor range to reduce the current through the driver. Choosing a resistor value of 450 ohms $\pm$ 10% will satisfy this requirement.

B.6 MULTIDROP TERMINATION REQUIREMENT

For applications with long transmission lines, a termination resistor (RP4) should be added at the receiver farthest from the driver to reduce the line signal reflection. This termination resistance value should be as close as possible to the characteristic impedance of the serial cable, approximately 100 ohms, but not less than 90 ohms.

For applications with long cable stubs or drivers driving in multiple directions on the cable, the termination may need to be placed at several end-point locations on the cable. Because the RS422 drivers do not have enough output current to drive multiple 100-ohm terminators, the resistor value for each terminator must be increased such that the total load resistance is no less than 90 ohms between the differential lines (refer to the EIA RS422 specification).

***

C.1 INTRODUCTION

PAL device U74 on the iSBC 286/1ØA board is considered user-replaceable. This appendix lists the contents of PAL U74. This appendix can also be used as a quick reference for the memory decode options.

PAL U74 on the iSBC 286/1ØA board defines your memory address space for local and iLBX bus memory. You can change the factory-default memory configuration by programming another PAL device that defines a specific memory configuration for your application.

Table C-1 lists the pinout for the primary decode PAL on the iSBC 286/1ØA board. Table C-2 lists the PAL equations for the default version of PAL U74. Table C-3 lists the memory configurations that PAL U74 provides in the default configuration.

NOTE

We recommend altering only the LBX and QMIO equations. QMIO must be active (true) when LBX is inactive (false), and QMIO must be inactive when LBX is active.

Intel provides technical support and repair service for only those boards modified by jumpers or replacement of socketed components. The original socketed component must be reinstalled before the board is sent to the repair center. There is no guarantee customer modified parts will be returned after the board's repair.

Table C-1. Primary Decode PAL U74 Device Description

Pin #	I/O	Name	Description
1	input	AE	Address Bits
2	input	AF	
3	input	A11	
4	input	A13	
5	input	A1Ø	
6	input	A17	
7	input	A15	
8	input	A16	
9	input	A14	
1Ø	input	GND	Ground
11	input	A12	Address bit
12	output	/LBX	LBX transfer selected, active low
13	input	MIO	Memory or I/O transfer
14	input	SELØ	Decode option select Ø (E218-E219)
15	input	SEL1	Decode option select 1 (E22Ø-E221)
16	input	UAEN	Upper address enable (PVAM)
17	output	/LCL1	Local memory group 1 (U4Ø/U75), active low
18	output	/QMIO	Qualified M/IO (for sync interface) active low
19	output	/LCL2	Local memory group 2 (U41/U76), active low
2Ø	input	VCC	+5 Volts

Note: UAEN determines operation mode of the iSBC 286/1ØA board:
UAEN low = 2Ø-bit board addressing
high = 24-bit board addressing

QMIO is used to protect the synchronous interface from false cycles when accessing on-board memory.

Table C-2. PAL Equations for U74

PAL Output	Signal Names and Relationships to Activate Output
IF (VCC) LBX	= MIO * /UAEN * /A13 + MIO * /UAEN * /A12 * /A11 + MIO * /UAEN * SEL1 * /A12 + MIO * /UAEN * SEL1 * /A11 + MIO * UAEN * /A17 + MIO * UAEN * /A16 + MIO * UAEN * /A15
IF (VCC) QMIO	= /MIO + /UAEN * /SEL1 * A13 * /A12 * A11 + /UAEN * /SEL1 * A13 * A12 + /UAEN * SEL1 * A13 * A12 * A11 + UAEN * A17 * A16 * A15
IF (VCC) LCL1	= MIO * /UAEN * SEL1 * SELØ * A13 * A12 * A11 * A1Ø * AF * AE + MIO * /UAEN * SEL1 * /SELØ * A13 * A12 * A11 * A1Ø * AF + MIO * /UAEN * /SEL1 * A13 * A12 * A11 * A1Ø + MIO * UAEN * SEL1 * SELØ * A17 * A16 * A15 * A14 * A13 * A12 * A11 * A1Ø * AF * AE + MIO * UAEN * SEL1 * /SELØ * A17 * A16 * A15 * A14 * A13 * A12 * A11 * A1Ø * AF + MIO * UAEN * /SEL1 * SELØ * A17 * A16 * A15 * A14 * A13 * A12 * A11 * A1Ø + MIO * UAEN * /SEL1 * /SELØ * A17 * A16 * A15 * A14 * A13 * A12 * A11
IF (VCC) LCL2	= MIO * /UAEN * SEL1 * A13 * A12 * A11 * A1Ø + MIO * /UAEN * /SEL1 * A13 * A12 + MIO * UAEN * SEL1 * A17 * A16 * A15 * A14 * A13 * A12 * A11 * A1Ø + MIO * UAEN * /SEL1 * A17 * A16 * A15 * A14 * A13 * A12

Note: LBX activates the iLBX and synchronous interfaces. The mode configuration determines which one will be used.

Table C-3. PAL U74 Memory Map (Compatibility Mode - UAEN Low)

Option Number	SEL1	SELØ	Local UØ/U75	Local U41/U76	iLBX™ Bus
Ø	1	1	FCØØØ-FFFFF (16K bytes)	FØØØØ-FBFFF (48K bytes)	ØØØØØ-DFFFF (896K bytes)
1	1	Ø	F8ØØØ-FFFFF (32K bytes)	FØØØØ-F7FFF (32K bytes)	ØØØØØ-DFFFF (896K bytes)
2	Ø	1	FØØØØ-FFFFF (64K bytes)	CØØØØ-EFFFF (192K bytes)	ØØØØØ-9FFFF (64ØK bytes)
3	Ø	Ø	FØØØØ-FFFFF (64K bytes)	CØØØØ-EFFFF (192K bytes)	ØØØØØ-9FFFF (64ØK bytes)

Table C-4. PAL U74 Memory Map (PVAM - UAEN High)

Option Number	SEL1	SELØ	Local UØ/U75	Local U41/U76	iLBX™ Bus
Ø	1	1	FFCØØØ-FFFFFF (16K bytes)	FFØØØØ-FFBFFF (48K bytes)	ØØØØØØ-DFFFFF (14 megabytes)
1	1	Ø	FF8ØØØ-FFFFFF (32K bytes)	FFØØØØ-FF7FFF (32K bytes)	ØØØØØØ-DFFFFF (14 megabytes)
2	Ø	1	FFØØØØ-FFFFFF (64K bytes)	FCØØØØ-FEFFFF (192K bytes)	ØØØØØØ-DFFFFF (14 megabytes)
3	Ø	Ø	FEØØØØ-FFFFFF (128K bytes)	FCØØØØ-FDFFFF (128K bytes)	ØØØØØØ-DFFFFF (14 megabytes)

Note: jumper E218-E219 = SELØ
SELØ and SEL1 = Ø
with their jumpers installed

jumper E22Ø-E221 = SEL1
SELØ and SEL1 = 1
with their jumpers removed

The PAL decodes up to the next power of two boundary (for example, 48K is actually a 64K block), causing an overlap between LCL1 and LCL2 in some cases. The secondary decode PAL handles the situation.

***

APPENDIX D
WAIT-STATE REQUIREMENTS

D.1 INTRODUCTION

This appendix helps you decide how many wait-states you must configure for local memory and shows time requirements for dual-port memory (fixed at two wait-states). By comparing the operating specifications from your memory devices with those listed in the following four tables, you can select one of the solutions that best satisfies your system requirements.

You have the option in the local memory sockets of placing a different type of device into each socket pair. As such, you can configure the wait-states independently for each socket pair. By configuring each socket pair to its optimum speed, you can make your system operation as efficient as possible.

Figures D-1 and D-2 show the parameters that are listed in Tables D-1 through D-4. You select a wait-state number for local memory by comparing the specifications for your memory devices with those listed in Tables D-1 through D-3. If any one of the memory device specifications listed in the table is violated by the chip specifications when you do your comparison, you cannot reliably use the memory chip with that number of wait-states; try another.

If you find that your memory chips do not meet the specifications for up to three wait-states for local memory or two wait-states for dual-port memory, you must use another type of memory chip.

Table D-1. Local Memory Requirements for 1 Wait-State at 8.Ø MHz

Symbol In Figure D-1	Parameter Description	Minimum	Maximum
t1	Read or Write Cycle Time	375	
t2	Address Access Time		254
t3	Chip Select Access Time		262
t4	Output Enable to Output Valid		147
t5	Output Disable to Output in High Z		121
t6	Chip Deselect to Output in High Z		N/A
t7	Chip Select to End of Write	286	
t8	Address Valid to End of Write	278	
t9	Address Set Up	153	
t1Ø	Write Pulse Width	125	
t11	Address Hold Time	56	
t12	Data Set Up Time	2Ø6	
t13	Data Hold Time	56	

Table D-2. Local Memory Requirements for 2 Wait-States at 8.Ø MHz

Symbol In Figure D-1	Parameter Description	Minimum	Maximum
t1	Read or Write Cycle Time	5ØØ	
t2	Address Access Time		379
t3	Chip Select Access Time		387
t4	Output Enable to Output Valid		272
t5	Output Disable to Output in High Z		121
t6	Chip Deselect to Output in High Z		N/A
t7	Chip Select to End of Write	411	
t8	Address Valid to End of Write	4Ø3	
t9	Address Set Up	153	
t1Ø	Write Pulse Width	25Ø	
t11	Address Hold Time	56	
t12	Data Set Up Time	331	
t13	Data Hold Time	56	

Table D-3. Local Memory Requirements for 3 Wait-States at 8.Ø MHz

Symbol In Figure D-1	Parameter Description	Minimum	Maximum
t1	Read or Write Cycle Time	625	
t2	Address Access Time		5Ø4
t3	Chip Select Access Time		512
t4	Output Enable to Output Valid		397
t5	Output Disable to Output in High Z		121
t6	Chip Deselect to Output in High Z		N/A
t7	Chip Select to End of Write	536	
t8	Address Valid to End of Write	528	
t9	Address Set Up	153	
t1Ø	Write Pulse Width	375	
t11	Address Hold Time	56	
t12	Data Set Up Time	456	
t13	Data Hold Time	56	

Table D-4. Dual-Port Memory Requirements
2 Wait-States at 8.Ø MHz (Nonconfigurable)

Symbol In Figure D-1	Parameter Description	Minimum	Maximum
t1	Read or Write Cycle Time	438	
t2	Address Access Time		254
t3	Chip Select Access Time		222
t4	Output Enable to Output Valid		1Ø9
t5	Output Disable to Output in High Z		145
t6	Chip Deselect to Output in High Z		N/A
t7	Chip Select to End of Write	226	
t8	Address Valid to End of Write	258	
t9	Address Set Up	6Ø	
t1Ø	Write Pulse Width	163	
t11	Address Hold Time	29	
t12	Data Set Up Time	193	
t13	Data Hold Time	28	

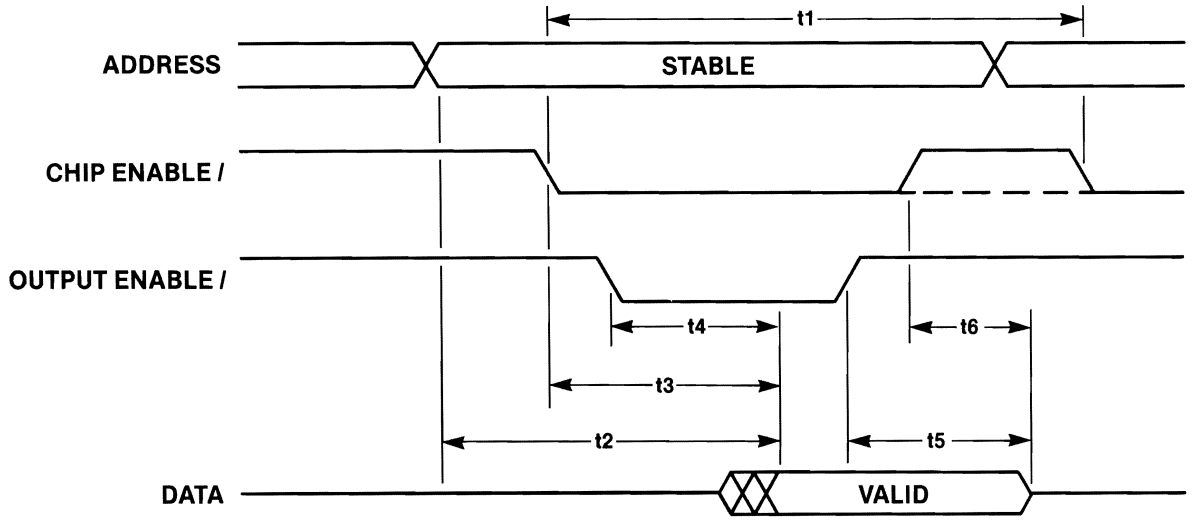

Figure D-1. Read Cycle

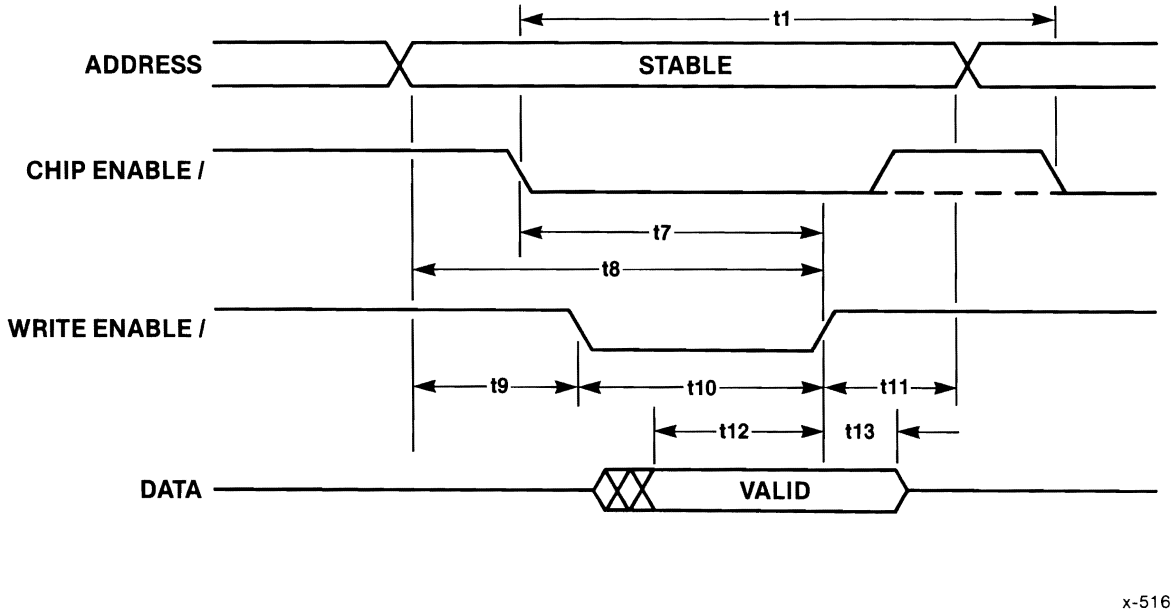

Figure D-2. Write Cycle

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APPENDIX E
MEMORY SOCKET MATRIX CONFIGURATIONS

E.1 INTRODUCTION

This appendix provides information for selecting memory components for the iSBC 286/1ØA board. The two important considerations in selecting a memory component for the board are

- Ensure that the memory component is compatible with the AC and DC specifications required by the chip socket.
- Ensure that your jumper configuration on the jumper matrix selects the required type of memory component.

E.2 SOCKET INTERFACE CHARACTERISTICS

The byte-wide sockets have certain AC and DC interface requirements. Any device installed into the byte-wide sockets (whether into dual-port or local sockets) must conform to the AC and DC specifications for byte-wide devices (listed in Table E-1).

Table E-1. Byte-Wide Socket AC and DC Specifications

Parameter	Conditions	Minimum	Maximum	Units
DC Characteristics				
V_{IL}			Ø.8	V
V_{IH}		2.Ø		V
I_{IL}	V_{IN}=Ø.4V		± 1Ø	uA
I_{IH}	V_{IN}=2.4V		± 1Ø	uA
V_{OL}	I_{OL}=2.ØmA		Ø.4	V
V_{OH}	I_{OH}=-2ØØuA	2.4		V
AC Characteristics				
C_{IO}	I/O Capacitance		12	pf

E.3 JUMPER MATRIX CONFIGURATION

You will find three jumper matrices on the iSBC 286/1ØA board: one for local memory socket pair U4Ø/U75, one for local memory socket pair U41/U76, and one for the dual-port memory sockets. You can configure each matrix independently for a different type of memory device.

The default configuration expects 16Kx8 EPROM devices to be installed into the local memory sites, and 2Kx8 EPROM, iRAM, or Static RAM to be installed in the dual-port memory sites.

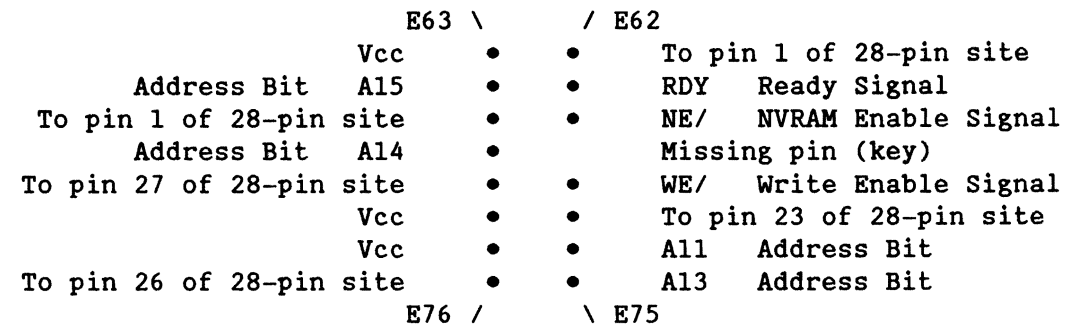
Each matrix consists of 15 stake pins arranged in two rows. One missing pin in each matrix serves as a key to the orientation. The pin assignments are shown in Figure E-1.

You configure each matrix by installing jumpers as required to place signals onto the proper pins of the memory devices. The jumper matrix provides 13 modes of operation for each respective socket pair. Figures E-2 through E-4 show diagrams of each of the 13 modes, assigned a configuration number from Ø to 12. The functions provided by each configuration are as follows:

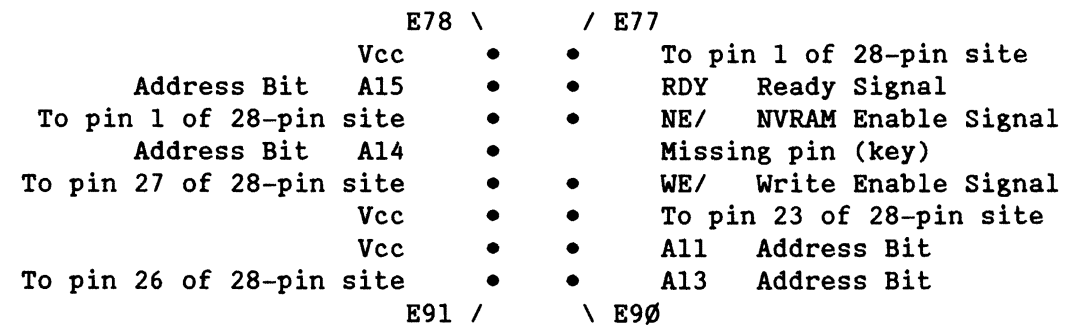
Reference	Configuration	Type of Memory Device in the Socket Pair
Figure E-2	Ø,1,2,3,4	For applications using Static RAM (for dual-port sockets only)
Figure E-3	5,6	For applications using iRAM devices (for dual-port sockets only)
Figure E-4	7,8,9,1Ø,11,12	For applications using EPROM devices (for local or dual-port sockets)

NOTE

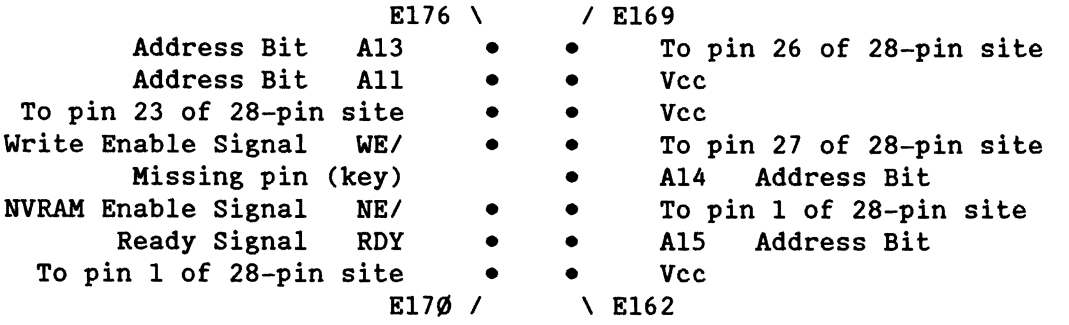
Verify the manufacturer's component pinout to nc. Some nc are required to be tied high or low.



Local Memory Socket Pinout, Pair U4Ø/U75



Local Memory Socket Pinout, Pair U41/U76



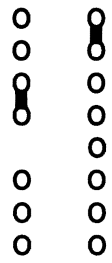
Dual-Port Memory Socket Pinout

Figure E-1. Memory Sockets' Pinout

2k x 8 Static RAM

Pin 1	n/c
Pin 27	n/c
Pin 26	Vcc
Pin 23	WE/

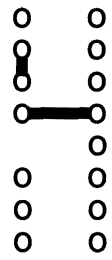
Jumper Matrix Configuration 0



4k x 8 Static RAM

Pin 1	n/c
Pin 27	WE/
Pin 26	n/c
Pin 23	A11

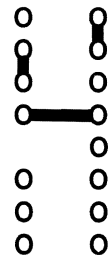
Jumper Matrix Configuration 1



8k x 8 Static RAM

Pin 1	n/c
Pin 27	WE/
Pin 26	Vcc
Pin 23	A11

Jumper Matrix Configuration 2



16k x 8 Static RAM

Pin 1	n/c
Pin 27	WE/
Pin 26	A13
Pin 23	A11

Jumper Matrix Configuration 3

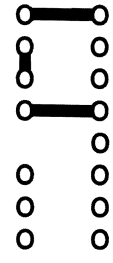


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Figure E-2. Jumper Matrix Configurations for Static RAM Devices

----------(continued)----------

32k x 8 Static RAM

Pin 1	A14
Pin 27	WE/
Pin 26	A13
Pin 23	A11

Jumper Matrix Configuration 3

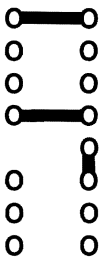

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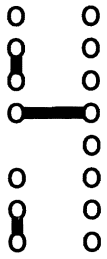
Figure E-2. Jumper Matrix Configurations for Static RAM Devices (continued)

8k x 8 iRAM (example 2168)

Pin 1	RDY
Pin 27	WE/
Pin 26	n/c
Pin 23	A11

Jumper Matrix Configuration 4



16k x 8 iRAM

Pin 1	RDY
Pin 27	WE/
Pin 26	A13
Pin 23	A11

Jumper Matrix Configuration 5

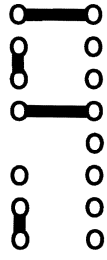


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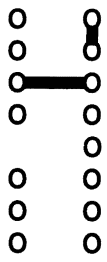
Figure E-3. Jumper Matrix Configurations for iRAM Devices

2k x 8 EPROM
(example 2716)

Pin 1	n/c
Pin 27	n/c
Pin 26	Vcc
Pin 23	Vcc/Vpp

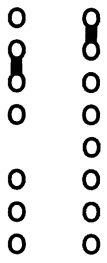
Jumper Matrix Configuration 6



4k x 8 EPROM
(example 2732A)

Pin 1	n/c
Pin 27	n/c
Pin 26	Vcc
Pin 23	A11

Jumper Matrix Configuration 7



8k x 8 EPROM
(example 2764)

Pin 1	Vcc/Vpp
Pin 27	Vcc/PGM
Pin 26	n/c
Pin 23	A11

Jumper Matrix Configuration 8

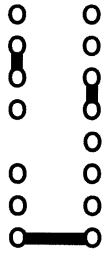


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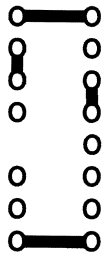
Figure E-4. Jumper Matrix Configurations for EPROM Devices

----------(continued)----------

16k x 8 EPROM (example 27128)

Pin 1	Vcc/Vpp
Pin 27	Vcc/PGM
Pin 26	A13
Pin 23	A11

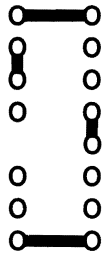
Jumper Matrix Configuration 9



32k x 8 EPROM (example 27256)

Pin 1	Vcc/Vpp
Pin 27	A14
Pin 26	A13
Pin 23	A11

Jumper Matrix Configuration 10



64k x 8 EPROM (example 27512)

Pin 1	A15
Pin 27	A14
Pin 26	A13
Pin 23	A11

Jumper Matrix Configuration 11

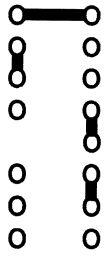


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Figure E-4. Jumper Matrix Configurations for EPROM Devices (continued)

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F.1 INTRODUCTION

This appendix provides information for installing the iSBC 341 Memory Expansion MULTIMODULE Board onto the iSBC 286/1ØA Single Board Computer. This expansion board expands the number of 28-pin memory chip sockets from four to eight for local or dual-port memory.

Local memory accepts only EPROM device types. However, dual-port memory accepts EPROM, EEPROM (only those requiring 5V programming signals), Static RAM, and iRAM device types.

F.2 iSBC® 341 BOARD INSTALLATION

Installing the iSBC 341 board adds four memory chip locations, labeled U2, U3, U5, and U6. As an example, the following sequence outlines the procedure for installing the iSBC 341 board onto the dual-port memory sites:

1. Unpack the board.
2. Inspect the board for damage. If damage exists, follow the instructions for servicing in Chapter 5 of this manual.
3. Modify the jumpers on the board to provide the required operation; refer to Section F.3 for jumper configurations.
4. Install the user-supplied memory devices onto the board.

CAUTION

The iSBC 286/10A board accommodates both 24- and 28-pin memory chips in the same socket. Ensure that pin 1 of the device is in the proper location.

5. Trim the leads of the memory devices (installed in step 4) at the end of the connectors.

6. Ensure that system power is off.

7. Remove the iSBC 286/1ØA board from the backplane and place it on a soft surface (preferably a piece of nonconducting foam), component side up.

8. Remove the memory devices from these locations:
   U41/U76 for local memory expansion
   U54/U87 for dual-port expansion

9. Hold the iSBC 286/1ØA board on edge and install the three screws (reference Figure F-1) from the solder side.

1Ø. Place a spacer on each of the screws.

11. Install the iSBC 341 board on the iSBC 286/1ØA board in the location shown in Figure F-1.

12. Press the iSBC 341 board into place by pressing at locations U1 and U4.

13. Install the three nuts and tighten them finger tight.

14. Tighten the three nuts with a nut driver.

CAUTION

Do not overtighten the nuts. Damage to the board could result.

15. Reinstall the memory devices, removed from the iSBC 286/1ØA board in step 8, into locations U1 and U4 on the iSBC 341 board.

CAUTION

Ensure that the memory devices are properly oriented in their sockets or they could be damaged when power is applied.

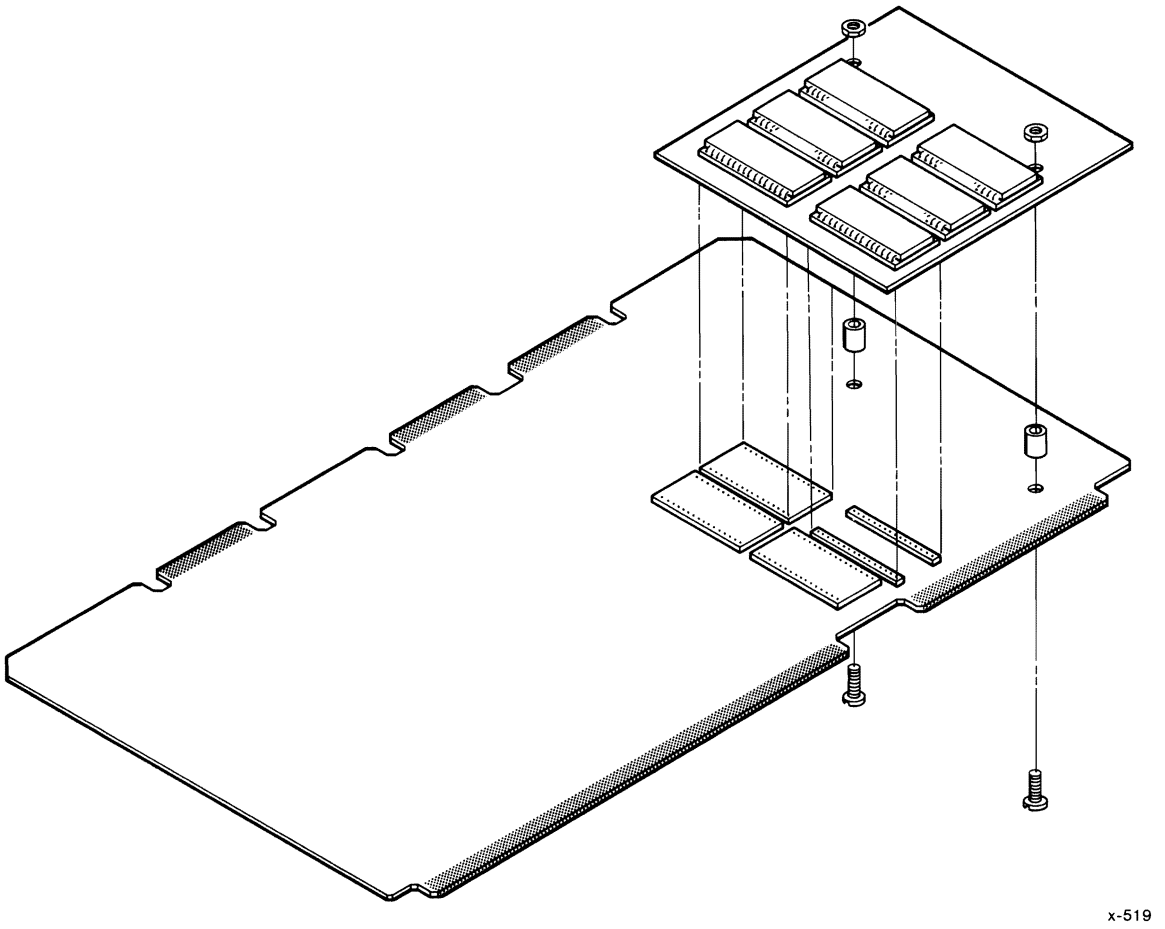

Figure F-1. iSBC® 341 Board Orientation (for dual-port memory)

F.3 CONFIGURATION INFORMATION

The iSBC 341 Memory Expansion MULTIMODULE board is shipped from the factory with the following jumpers installed (refer to the schematic diagram, Figure F-3):

E9-E1Ø	E39-E43	E13-E14	E47-E5Ø
E17-E18	E3Ø-E31	E53-E57	E37-E41
E25-E26	E1-E2	E21-E22	E35-E36

This configuration matches the iSBC 341 board to the configuration of the iSBC 286/1ØA board. For example, if the iSBC 286/1ØA board is configured to accept a particular capacity of memory devices, this jumper configuration allows the iSBC 341 board to accept the same capacity of memory device.

Jumper modifications are required for installation of Static RAM, iRAM, and EEPROM devices as shown in Table F-1.

Table F-1. Jumper Configurations for Types of Memory Devices

In iSBC® 341 Sockets Remove:	Install:	
STATIC RAM REQUIREMENTS		
U2 and U5 U3 and U6	E39 - E43 E37 - E41	E4Ø - E44 E38 - E42
iRAM REQUIREMENTS		
U2 and U5 E39 - E43 U3 and U6 E37 - E41	E9 - E1Ø E4Ø - E44 E1 - E2 E38 - E42	E7 - E15 E4 - E11
EEPROM REQUIREMENTS		
U2 and U5	E39 - E43 E53 - E57 E3Ø - E31 E9 - E1Ø	E6 - E7 E54 - E58 E27 - E28 E4Ø - E44
U3 and U6	E37 - E41 E47 - E5Ø E35 - E36 E1 - E2	E3 - E4 E45 - E48 E32 - E33 E38 - E42

NOTE

The iSBC 286/1ØA board does not support EEPROM devices that require a 21-volt programming signal but does support those requiring a 5-volt signal.

F.4 SERVICE DIAGRAMS

The iSBC 341 board parts location diagram and schematic diagram are provided in Figures F-2 and F-3.

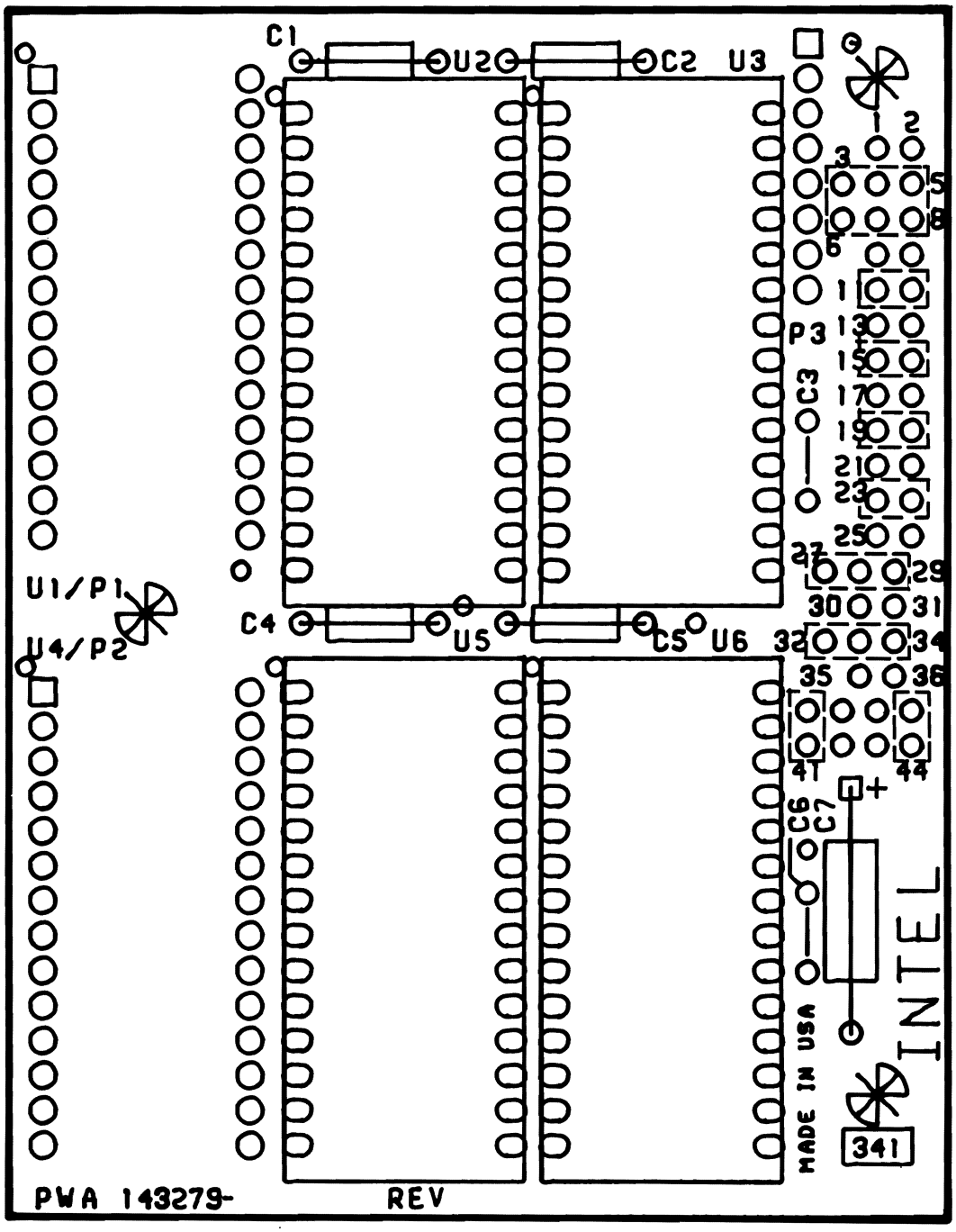

Figure F-2. iSBC® 341 Board Parts Location Diagram

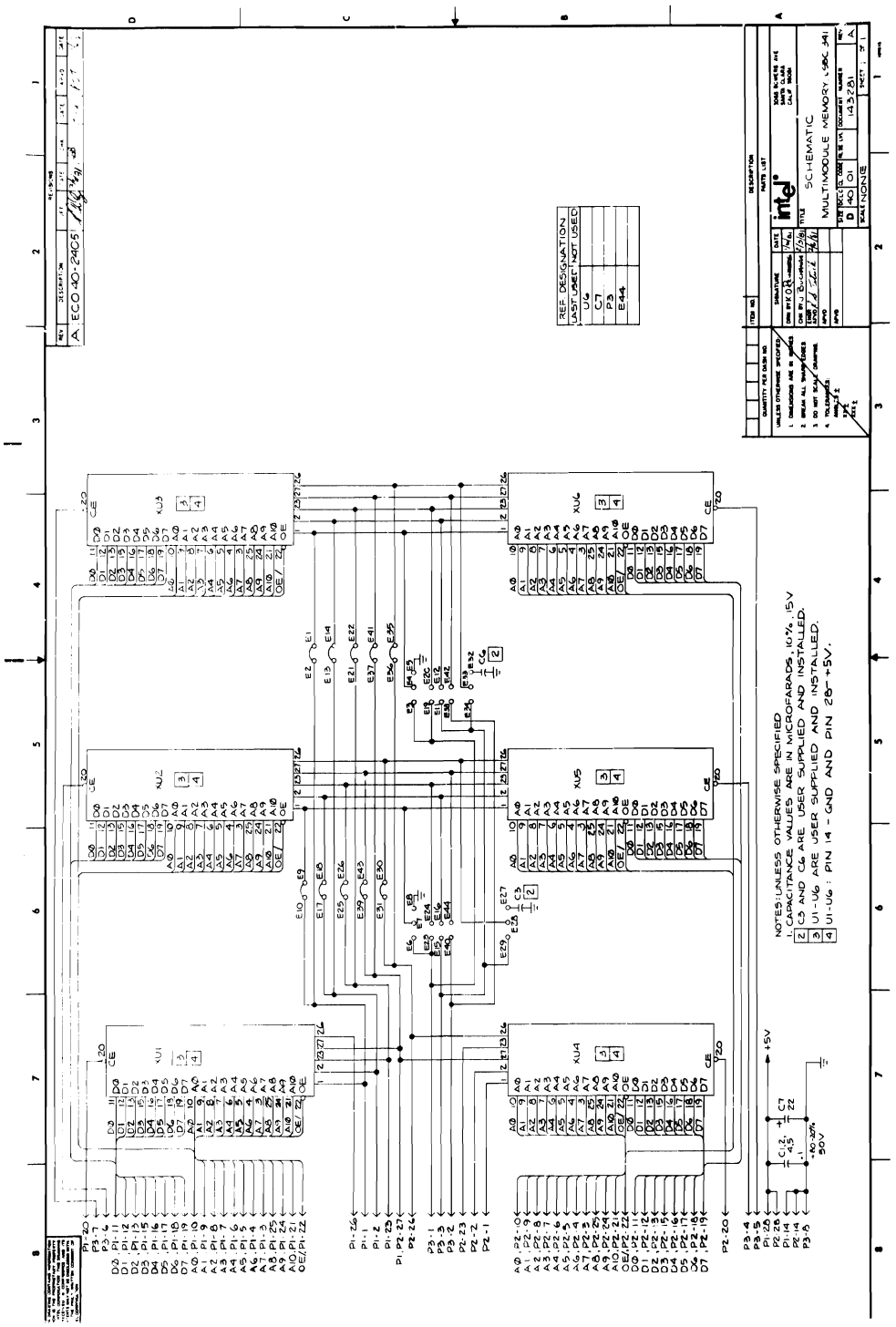

Figure F-3. iSBC® 341 Board Schematic Diagram

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G.1 INTRODUCTION

This appendix provides a list of all I/O port addresses for the iSBC 286/10A board and is to be used as a quick reference. See Chapter 4 for specific information. Table G-1 lists the port addresses for the two iSBX bus interfaces, and Table G-2 lists the port addresses for the other I/O devices on the board.

Table G-1. I/O Port Addresses for iSBX™ Bus Connectors

Port Addresses for 286/10A board with an 8-bit MULTIMODULE board

on Connector J6 (SBX1)		on Connector J5 (SBX2)
009F or 009E		00BF or 00BE
009D or 009C		00BD or 00BC
009B or 009A		00BB or 00BA
0099 or 0098	MCS1* Active	00B9 or 00B8
0097 or 0096		00B7 or 00B6
0095 or 0094		00B5 or 00B4
0093 or 0092		00B3 or 00B2
0091 or 0090		00B1 or 00B0
008F or 008E		00AF or 00AE
008D or 008C		00AD or 00AC
008B or 008A		00AB or 00AA
0089 or 0088	MCS0* Active	00A9 or 00A8
0087 or 0086		00A7 or 00A6
0085 or 0084		00A5 or 00A4
0083 or 0082		00A3 or 00A2
0081 or 0080		00A1 or 00A0

Port Addresses for 286/10A board with a 16-bit MULTIMODULE board

on Connector J6 (SBX1)			on Connector J5 (SBX2)	
008F	008E		00AF	00AE
008D	008C		00AD	00AC
008B	008A		00AB	00AA
0089	0088		00A9	00A8
0087	0086		00A7	00A6
0085	0084		00A5	00A4
0083	0082		00A3	00A2
0081	0080		00A1	00A0
MCS1* Active	MCS0* Active		MCS1* Active	MCS0* Active

Table G-2. I/O Port Addresses for iSBC® 286/1ØA Board

Port Addresses (Hex)	Device	Functions Available
ØØCØ	Master PIC	Byte: Status, ICW1 Word: N/A
ØØC2	Master PIC	Byte: MASK Word: N/A
ØØC4	Slave PIC	Byte: Status, ICW1 Word: N/A
ØØC6	Slave PIC	Byte: MASK Word: N/A
ØØC8	Parallel I/O	Byte: Port A Out Word: note 2
ØØCA	Parallel I/O	Byte: Port B In Word: note 2
ØØCC	Parallel I/O	Byte: Port C Out Word: note 2
ØØCE	Parallel I/O	Byte: Control Word: note 2
ØØDØ	Timer	Byte: Counter Ø Word: N/A
ØØD2	Timer	Byte: Counter 1 Word: N/A
ØØD4	Timer	Byte: Counter 2 Word: N/A
ØØD6	Timer	Byte: Control Word: N/A
ØØD8	Serial I/O	Byte: CH A Data Word: N/A
ØØDA	Serial I/O	Byte: CH B Data Word: N/A
ØØDC	Serial I/O	Byte: CH A Control Word: N/A
ØØDE	Serial I/O	Byte: CH B Control Word: N/A
ØØEØ-ØØEE	RESERVED	
ØØF8	8Ø287 CPU	Byte: N/A Word: RD Status, WR Opcode
ØØFA	8Ø287 CPU	Byte: N/A Word: Data
ØØFC	8Ø287 CPU	Byte: N/A Word: Address

Notes: 1. All ports in the range ØØCØ-ØØFF which are not listed are on-board and reserved. If any iSBX board is installed, all I/O ports in the range ØØ8Ø-ØØBF become an on-board resource and may be considered as reserved.

2. A word-write to this port switches the board from Real Address Mode to PVAM.

Primary references are underlined.

■ I ■

■ J ■

■ L ■

■ M ■

■ N ■

■ P ■

■ R ■

■ S ■

■ U ■

■ W ■

***

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