

SBC 519 PROGRAMMABLE I/O EXPANSION BOARD HARDWARE REFERENCE MANUAL

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Revision B includes technical corrections (Figure 2-3, Table 4-1, and Table 7-2) and new schematics.

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CHAPTER 1

INTRODUCTION

The SBC-519 TTL Programmable General Purpose I/O (TTL PGPI/O) board is a member of Intel's complete line of SBC 80 I/O expansion boards. The SBC-519 provides expanded parallel I/O capacity to any SBC 80 Single Board Computer via the system bus. It also provides a vectored polled interrupt scheme that is capable of resolving up to eight interrupts according to a program-controlled priority structure. An interval timer is included on the SBC-519 board to provide a time-based interrupt source for real-time processing applications.

The parallel I/O expansion feature uses three Intel 8255A Programmable Peripheral Interfaces. Together, these devices provide 72 I/O lines, which can be configured by the system software to meet a wide variety of peripheral interface requirements. These 72 lines can be implemented in various combinations of unidirectional input/output and bi-directional ports, which the user can program to operate in any of three modes.

So that full advantage can be taken of the large number of possible I/O configurations, sockets are provided for interchangeable quad I/O line drivers and terminators. This provision allows the user to select sink currents, polarities and other characteristics appropriate to the application.

The SBC-519 includes an Intel 8259 Programmable Interrupt Controller, which gathers up to eight interrupt sources and generates

a single priority interrupt. The 8259 supplies the CPU with a three-bit vector (highest priority) for each interrupt request.

There are 10 potential interrupt sources available to the 8259 device: six from the 8255A's, three from external sources and one from the interval timer. Jumper pads on the SBC-519 allows any combination of up to eight interrupt sources to be selected from this set of 10.

The 8259 resolves priority among the eight interrupt inputs according to a program-selected algorithm. A variety of priority algorithms is available to the programmer so that the manner in which the 8259 handles interrupt requests can be adapted to different system characteristics. Because they are program-controlled, these algorithms can be changed dynamically to accommodate changing system requirements. The 8259 can be programmed to operate in the following non-exclusive modes.

- . Rotating Priority Mode
- . Special Mask Mode
- . Polled Mode (Note: This mode is always used for submitting interrupt requests to CPU.)

The user also has the option of by-passing the 8259 and driving the SBC bus interrupt lines directly.

The 8255A and 8259 port registers are addressed as I/O ports. Address assignments are made by on-board jumper selection. The selected base I/O address must be on a 16-byte boundary. No other address assignment constraint is imposed by the SBC-519.

The user can also jumper-select the Interval Timer period from four possibilities, whose values are determined by the CCLK frequency in the following relationships: $4608 \times 1/\text{CCLK}$; $9216 \times 1/\text{CCLK}$; $18,432 \times 1/\text{CCLK}$ and $36,864 \times 1/\text{CCLK}$. If CCLK is supplied by an SBC 80/10 or 80/20, the four possible Interval Timer periods are 0.5 ms, 1 ms, 2 ms and 4 ms.

All SBC-519 circuit elements reside on a single 6.75×12 inch printed circuit card and are physically and electrically compatible with the SBC 80 system bus. The SBC-519 is also compatible with the Intellec Microcomputer Development System bus, as defined in Chapter 6.0.

CHAPTER 2

FUNCTIONAL/PROGRAMMING CHARACTERISTICS

This chapter briefly describes the organization of the SBC-519 from two points of view. The principal functions performed by the hardware are identified and the general data flow is illustrated in Section 2.1. This section is intended as an introduction to the detailed information provided in Chapter 3, Theory of Operations. Section 2.2 summarizes the information needed by the programmer to initialize and access the I/O and interrupt facilities on the SBC-519.

2.1 FUNCTIONAL DESCRIPTION

To facilitate the following description, the SBC-519 is divided into functional blocks, as shown in Figure 2-1.

- 1) Bus Interface
- 2) Parallel I/O Interface
- 3) Interrupt Controller
- 4) Interval Timer

The Bus Interface logic consists of those circuit elements most directly involved with communication between the bus master and the SBC-519. These include bus address/control line receiver, bidirectional data buffer, I/O port select decode logic and transfer acknowledge generation and line driver circuits.

The Parallel I/O Interface consists of three Intel 8255A Programmable Peripheral Interface devices, and twenty-four 14-pin sockets

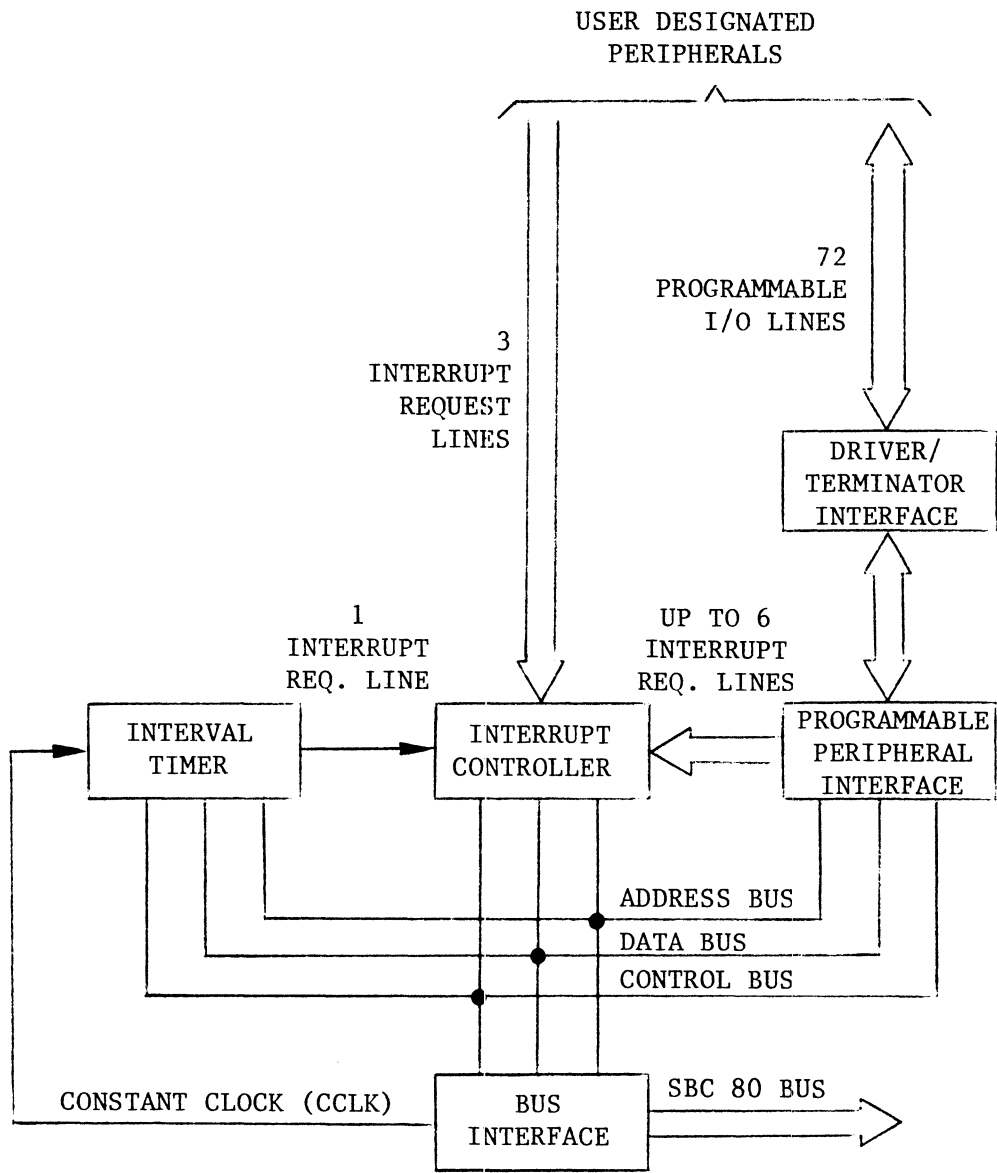


FIGURE 2-1. SBC-519 FUNCTIONAL BLOCK DIAGRAM

for installing quad line driver and/or terminator packages as required to satisfy the particular I/O interface requirements. The input/output configuration of each 8255A device is programmed independently, with the three ports (A, B and C) of each device treated as a separate group. Wire wrap jumper pins allow the user to implement up to six I/O lines (two per group) to be implemented as interrupt request lines.

The Intel 8259 Interrupt Controller resolves interrupt requests from up to eight different sources according to a program-selected priority scheme. Interrupt request (IR) inputs to the 8259 are determined by on-board jumper selection. Priority assignments for the eight IR inputs can be changed under program control using the rotating priority mode. Individual IR inputs can also be masked or unmasked under program control. When polled by the CPU, the 8259 issues a three-bit vector that identifies the current interrupt request having the highest priority.

The Interval Timer is formed by a cascaded set of four binary counters; a D-type flip-flop latches the timer output. This timer circuit is driven by the system's CCLK (9.216 MHz for SBC 80/10 or 80/20). A jumper pad in the circuit provides the means for selecting one of four possible interrupt periods. If CCLK is provided by an SBC 80/10 or 80/20, the available periods are: 0.5 ms, 1 ms, 2 ms or 4 ms. A second jumper pad allows the Interval Timer output to be applied to IR input 0 (normally highest priority) or to disable that input. The Interval Timer output can also be read directly by the CPU whether the IRO input to the 8259 is enabled or disabled.

2.2 PROGRAMMING CHARACTERISTICS

This section summarizes the SBC-519 addressing characteristics.

The module's base I/O address is assigned through the use of wire wrap jumper pins on the board. These two jumpers are part of the board's address decode circuit for system address bits 4-7. They allow the selection of a base address for the SBC-519 on a 16-bit boundary. Address bits 0-3 are decoded by other logic to select 1 of 16 data, status or control ports on the board.

Program access to SBC-519 module's 16 ports is discussed in the following subsections.

2.2.1 PARALLEL I/O INTERFACE ADDRESSES

The parallel I/O interface consists of three identical groups of parallel I/O ports, with three eight-bit ports in each group. Each port is separately addressable. In addition, each group includes a control register, which has its own address. These control registers are written into in order to specify certain operating characteristics for their respective ports.

These various ports and registers are accessed at the addresses shown in Table 2-1.

2.2.2 PROGRAMMABLE INTERRUPT CONTROLLER

There are two port addresses associated with the 8259. These are used for outputting command words to the 8259 and for reading various 8259 registers. The 8259 port addresses are shown in Table 2-2.

TABLE 2-1. PARALLEL I/O PORT ADDRESSES

Group 1 (A19)		Group 2 (A22)		Group 3 (A23)	
Port	Address	Port	Address	Port	Address
1	X0	4	X4	7	X8
2	X1	5	X5	8	X9
3	X2	6	X6	9	XA
Control Register	X3	Control Register	X7	Control Register	XB

X = Any hex digit; assigned by jumper selection;
X is the same for all SBC-519 ports.

TABLE 2-2. INTERRUPT CONTROLLER PORT ADDRESSES

Port Addr	Read	Write	Function
XC	1	0	Read interrupt vector, interrupt request register (IRR) or in-service register (ISR).
XC	0	1	Write initialization command word (ICW) or operation command word (OCW).
XD	1	0	Read interrupt mask register (IMW).
XD	0	1	Write ICW or OCW.

X = Any hex digit; assigned by jumper selection;
X is the same for all SBC-519 ports.

ICW's (Input Command Word) are used to prepare the 8259 for normal operation. A two-byte ICW sequence (ICW1 and ICW2) is output to the 8259 in order to reset the edge sense circuit, special mask mode flip-flop and status read flip-flop. This sequence also clears the interrupt mask register (IMR) and assigns priority 7 (lowest priority) to the Interrupt Request 7 (IR7) input.

Figure 2-2 shows the 8259 initialization sequence.

The OCW's (Output Command Word) are used to command the 8259 to operate in various interrupt modes: rotating priority mode, special mask mode or polled mode.

Table 2-3 lists the instruction set used for programming the 8259. Those instructions that are not available to the SBC-519's Interrupt Controller are shaded in the table.

Further details regarding 8259 operation are provided in Chapter 3.

2.2.3 INTERVAL TIMER

The same port addresses are used to sample the Interval Timer output as to reset the Interval Timer output latch. The output is sampled by executing an input (read) to port address XE or XF. The state of the Interval Timer is represented on data line 0. The Interval Timer is reset by executing a write to port XE or XF with a 00 in the accumulator. The timer interval is set by hardware jumper. The timer will cause the timer flag to interrupt the bus master once a cycle (one time interval). The bus master must service the interrupt by resetting the timer flag. If the bus master does not reset the timer flag before the next time interval was expired, the timer flag will not generate a new interrupt.

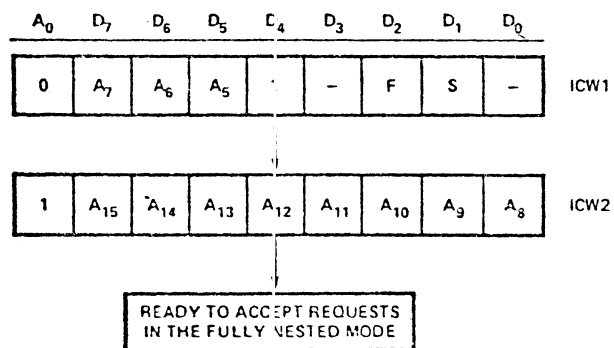


FIGURE 2-2. 8259 INITIALIZATION SEQUENCE

PORT	WRITE	READ	FUNCTION
XE or XF	1		RESET INTERRUPT FLAG ACC = 00
XE or XF		1	READ INTERRUPT FLAG D0 = 0 INTERRUPT OCCURRED = 1 NO INTERRUPT D1-D7 = UNDEFINED

FIGURE 2-3. INTERVAL TIMER PORTS

TABLE 2-3. 8259 INSTRUCTION SET

INST. No.	MNEMONIC	A0	D7	D6	D5	D4	D3	D2	D1	D0	OPERATION DESCRIPTION
1	ICW1 A	0	A7	A6	A5	1	-	1	1	-	Byte 1 initialization, format = 4, single.
2	ICW1 B	0	A7	A6	A5	1	-	1	0	-	Byte 1 initialization, format = 4, not single.
3	ICW1 C	0	A7	A6	A5	1	-	0	1	-	Byte 1 initialization, format = 8, single.
4	ICW1 D	0	A7	A6	A5	1	-	0	0	-	Byte 1 initialization, format = 8, not single
5	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization (Address No. 2)
6	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization - master.
7	ICW3 S	1	-	-	-	-	-	S2	S1	S0	Byte 3 initialization - slave.
8	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask reg. read mask reg.
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non specific EO1.
10	OCW2 SE	0	0	1	1	0	0	L2	L1	L0	Specific EO1, L2, L1, L0 code of ISFF to be reset.
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EO1 (Auto Mode).
12	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate at EO1 (Specific Mode). L2, L1, L0, code of line to be reset and selected as bottom priority.
13	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	L2, L1, L0 code of bottom priority line.
14	OCW3 P	0	-	0	0	0	1	1	0	0	Poll mode.
15	OCW3 RIS	0	-	0	0	0	1	0	1	1	Read IS register.
16	OCW3 RR	0	-	0	0	0	1	0	1	0	Read requests register.
17	OCW3 SM	0	-	1	1	0	1	0	0	0	Set special mask mode.
18	OCW3 RSM	0	-	1	0	0	1	0	0	0	Reset special mask mode.

Notes:

1. In the master mode \overline{SP} pin = 1, in slave mode \overline{SP} = 0.
2. (-) = do not care.

NOTE: All mnemonics copyright 1976 Intel Corporation.

CHAPTER 3

THEORY OF OPERATION

In the preceding chapter, each of the SBC-519 functional blocks was identified and briefly defined. This chapter explains how these functions are implemented. For detailed circuit information, refer to the SBC-519 schematics, which are provided in Appendix A.

Note: Both active-high (positive true) and active-low (negative true) signals appear in the SBC-519 schematics. To avoid confusion when referring to these signals in this chapter, the following convention is used. The mnemonic (signal label) for each active-low signal is terminated by a slash; e.g., IOW/ means that the signal level on that line will be low when the I/O write command is true (active). A mnemonic without the slash refers to an active-high signal; e.g., the line labeled EXT INTR 0 is at the high logic level when the external interrupt 0 signal is true.

3.1 BUS INTERFACE

The Bus Interface refers to those logic elements that participate directly in the following types of system bus activity.

- 1) System address, control and data buffering
- 2) System address decoding
- 3) System control signal propagation
- 4) Transfer acknowledge generation.

The four groups of Bus Interface logic responsible for these tasks are described in the following paragraphs.

3.1.1 BUS ADDRESS, CONTROL, DATA BUFFERS

The bus address and control signal buffer circuit consists of inverting line receivers of the 74LS04 (address) and 74S00 (control) types. These circuits restore the signals on the system bus lines to their proper logic levels with very high switching speed.

The data buffers are formed by two Intel 8226 inverting bi-directional driver/receiver chips (A9 and A10). The system data bus is connected to the devices' DB pins. The D0 and DI pins of each chip are connected, via printed wires, to the 8259 outputs and to the data/control pins of the three 8255A devices.

Directional control (RD/) for A9 and A10 is exercised by the I/O read command (IORC/). If the read command is asserted by the bus master, and the matching base I/O address is present, the data buffer's driver mode is selected. At all other times, the data buffer's receiver circuits are enabled.

The chip select (CS/) for the data buffer is enabled when a command is gated into the board.

3.1.2 SYSTEM ADDRESS DECODE LOGIC

This logic decodes the appropriate system bus address bits into a chip select for one of the 8255A devices, the 8259 device, or for the Interval Timer. It also produces an enable for the read/write command decode logic.

The base I/O address is decoded by an Intel 3205 one out of eight binary decoder, A20. This device is enabled by either ADR7/ or ADR7, as determined by the jumper selection at jumper pins 36, 37, 38. When enabled, A20 decodes address bits ADR4/, ADR5/ and ADR6/ into one of eight outputs.

Jumper pad S1 allows the base I/O address enable to be taken

from any one of the eight A20 outputs.

When the ADR4/ through ADR7/ bits correspond to the selected base I/O address, an enable is provided to a chip select generator and to the read/write command gates.

The chip select generator consists of an Intel 3205 device (A7) that is enabled by the decoded base I/O address. When enabled, A7 decodes address bits ADR2/ and ADR3/ into one of four chip select outputs. One of the four outputs is further decoded with ADR1 and ADR1/ to provide an enable for the Interval Timer read/write logic.

Table 3-1 identifies the address bit combinations required to produce these chip selects and enables.

TABLE 3-1. CHIP SELECT DECODE COMBINATIONS

Address Bits			Select
3	2	1	
0	0	x	55CS0/; selects 8255A at A19
0	1	x	55CS1/; selects 8255A at A22
1	0	x	55CS2/; selects 8255A at A23
1	1	0	Selects 8259
1	1	1	Enables Interval Timer read/write gates
(x) = Used to decode port select in 8255A 0 = ADR bit is high (false) 1 = ADR bit is low (true)			

3.1.3 COMMAND DECODE

A pair of 74S00 NAND gates buffer the IORC/ (I/O Read Command) and IOWC/ (I/O Write Command) inputs from the system bus.

These gates are permanently enabled so that any I/O read or I/O

write command appearing on the system bus is passed on to the Advance/Transfer Acknowledge Generator via OR gate A2. The output of A2 is designated CMD.

CMD is inverted and then enabled by the decoded base I/O address at gate A2 to produce the board enable. This signal, BD ENABLE/ controls the 3-state gates that drive AACK/ and XACK/ on the system bus.

The output of the IOWC/ receiver (A1-8) is inverted and forwarded to the Interrupt Controller (A8), the Interval Timer write gate (A11-4) and the three Peripheral I/O Interface chips (A19, A22, A23). This internal write enable, designated WRT/, is qualified at each of these destinations by the appropriate chip select.

The output of the IORC/ receiver (A1-11) is enabled by the decoded base I/O address at A2-8. The resulting internal read enable, RD/, is applied to the Interrupt Controller (A8), the Interval Timer read gate (A11-9) and to the bidirectional bus driver chips (A9, A10).

3.1.4 ADVANCE/TRANSFER ACKNOWLEDGE GENERATION

This logic provides a transfer acknowledge response, XACK, to notify the bus master that data has either been accepted from the system bus (during a WRITE operation) or placed on the system bus (during a READ operation). An advance acknowledge response, AACK, is also provided for use in certain 8080-based systems, where it can decrease by one the number of wait states needed to complete a READ or WRITE operation.

AACK is used in certain I/O applications where an early acknowledgment to the 8080 is needed to allow it to proceed to the T3 state following the current T2 or wait state. Such applications have the following

characteristics--XACK is generated too late for the 8080 to detect it in the current state, but

- 1) valid read data will be placed on the system bus by the time the 8080 needs it in the current state, or
- 2) write data will be accepted from the system bus by the time the 8080 has completed its WRITE operation.

In either case, AACK is sent to the 8080 early enough in the current state (T2 or wait) to prevent the bus master from entering a subsequent wait state. The I/O transaction is completed during the current T2 or wait state and the bus master moves on to T3.

NOTE: All SBC boards connected to the system bus must have AACK compatibility for any one of them to use the feature unless the incompatible board can jumper off AACK.

Both acknowledge responses are generated by A18, an eight-bit serial in, parallel out shift register. When enabled by CMD, A18 shifts CCLK/ pulses. These produce a sequence of high-true pulses at A18's Q outputs. The outputs occur at approximately 100 ns intervals.

The appropriate Q outputs are selected by hardwire connections to the inputs of a pair of 3-state gates (A4-12, A4-14). These gates allow the AACK/ and XACK/ outputs onto the system bus when enabled by BD ENABLE/.

3.2 PARALLEL I/O INTERFACE

The Parallel I/O Interface logic on the SBC-519 provides 72 signal lines for the transfer and control of data to or from peripheral devices. Sockets are provided for the installation of appropriate line driver and/or termination networks for all 72 lines. The optional drivers and terminators are installed in groups of four lines by insertion into the 14-pin sockets or 16-pin sockets for Intel's 8216 or 8226 bidirectional drivers. Bidirectional bus driver chips (e.g., 8216 or 8226) can be used in certain socket positions. These are identified in Chapter 4.

All 72 signal lines emanate from the I/O ports on three Intel 8255A Programmable Peripheral Interface devices, as shown on sheets 2 and 3 of the SBC-519 schematic. These 8255A devices, A19, A22 and A23, allow for a wide

variety of I/O configurations. Before describing the possible configurations, however, we will summarize the general operational characteristics of the 8255A device.

3.2.1 8255A OPERATIONAL SUMMARY

The 8255A contains three 8-bit ports (A,B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B.

The bus master dictates the operating characteristics of the ports by outputting two different types of control words to the 8255A:

- 1) mode definition control word (bit 7 = 1)
- 2) port C bit set/reset control word (bit 7 = 0)

Bit 7 of each control word specifies its format, as shown in Figures 3-2 and 3-3, respectively.

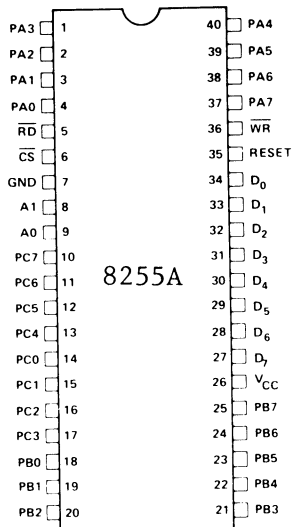
Mode Selection

There are three basic modes of operation that can be selected by the system software:

- Mode 0 - Basic Input/Output
- Mode 1 - Strobed Input/Output
- Mode 2 - Bidirectional Bus

When the RESET input goes "high" all ports will be set to the Input Mode 0 (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255A can remain in the Input mode with no additional initialization required. During the execution of the

PIN CONFIGURATION



PIN NAMES

D ₇ -D ₀	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V _{cc}	+5 VOLTS
GND	0 VOLTS

FIGURE 3-1. 8255A PIN ASSIGNMENTS

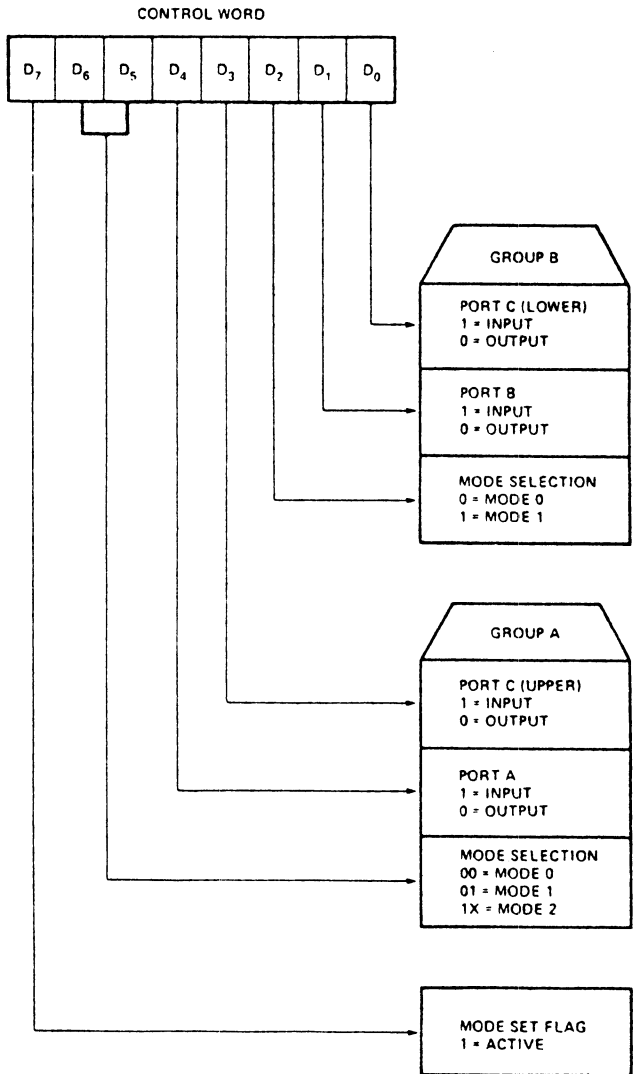


FIGURE 3-2. MODE DEFINITION CONTROL WORD FORMAT

system program, the other modes may be selected using a single OUT instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed except for $\overline{\text{OBF}}$ in modes 1 and 2. Modes may be combined so that their functional definition can be tailored to almost any I/O structure. For instance, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUT instruction (see Figure 3-3). This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using a Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the bus master. The interrupt request signals, generated from Port C can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit set/reset function of Port C.

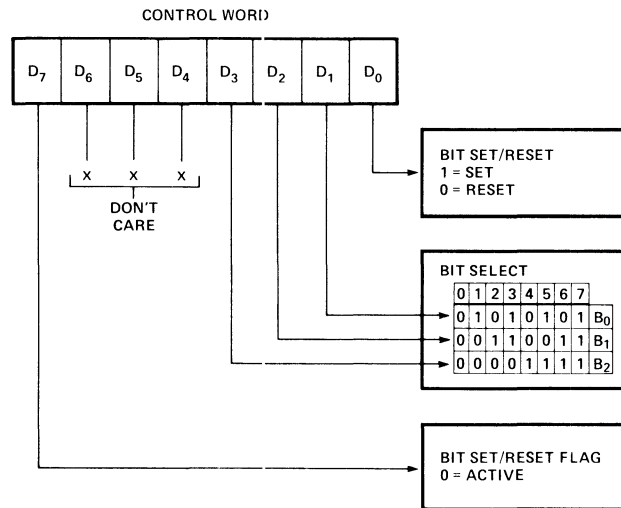


FIGURE 3-3. BIT SET/RESET CONTROL WORD FORMAT

This function allows the Programmer to disallow or allow specific I/O devices to interrupt the bus master without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) - INTE is SET - Interrupt enable

(BIT-RESET) - INTE is RESET - Interrupt disable

NOTE: All mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output):

This functional configuration provides simple Input and Output operations for each of the three ports. No "hand-shaking" is required, data is simply written to or read from a specified port. Mode 0 timing is illustrated in Figure 3-4.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.

Sixteen different Input/Output configurations are possible in this Mode. Figure 3-5 shows two possible configurations.

Mode 1 (Strobed Input/Output):

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two transfer ports (A and B).
- Each transfer port contains one 8-bit data port and 4 bits from one half of the control/data port (Port C).
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.

Input Control Signal Definition for Mode 1

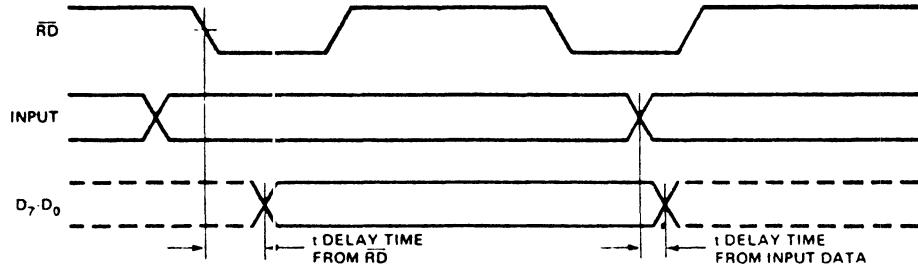
$\overline{\text{STB}}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by the falling edge of the STB input and is reset by the rising edge of the $\overline{\text{RD}}$ input.

BASIC INPUT
TIMING (D₇-D₀
FOLLOWS INPUT,
NO LATCHING)



BASIC OUTPUT
TIMING (OUTPUTS
LATCHED)

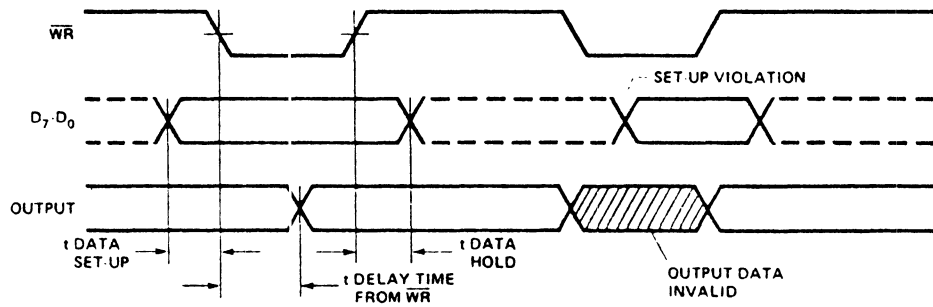


FIGURE 3-4. 8255A MODE 0 TIMING

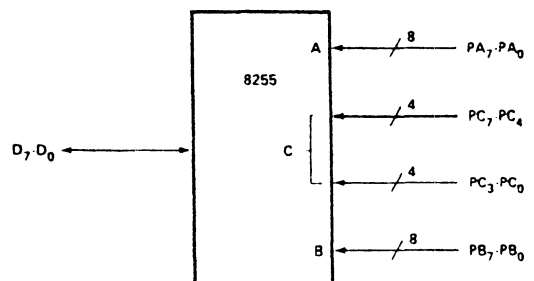
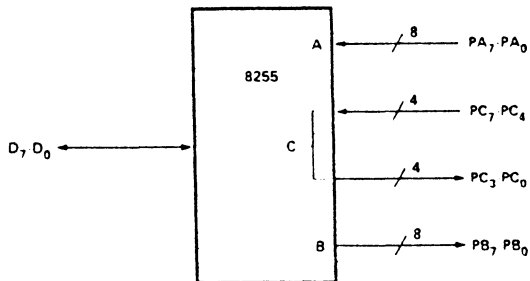
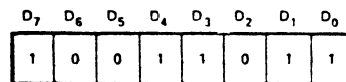
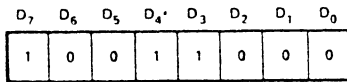


FIGURE 3-5. EXAMPLES OF MODE 0 CONFIGURATION

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the bus master when an input device is requesting service. INTR is set by the rising edge of \overline{STB} if IBF is a 1 and INTE is a 1. It is reset by the falling edge of \overline{RD} . This procedure allows an input device to request service from the bus master by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Figure 3-6 illustrates the Mode 1 input configuration, while Figure 3-7 shows the basic timing for Mode 1 input.

Output Control Signal Definition for Mode 1

\overline{OBF} (Output Buffer Full F/F)

The \overline{OBF} output will go low to indicate that the bus master has written data out to the specified port. The OBF F/F will be set by the rising edge of the \overline{WR} input and reset by the falling edge of the \overline{ACK} input signal.

\overline{ACK} (Acknowledge Input)

A low on this input informs the 8255A that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the bus master.

INTR (Interrupt Request)

A high on this output can be used to interrupt the bus master

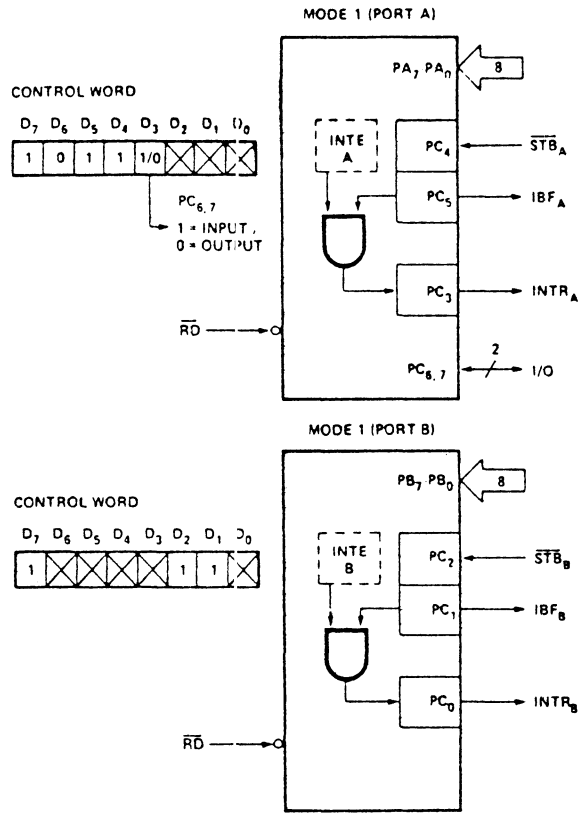


FIGURE 3-6. MODE 1 INPUT CONFIGURATION

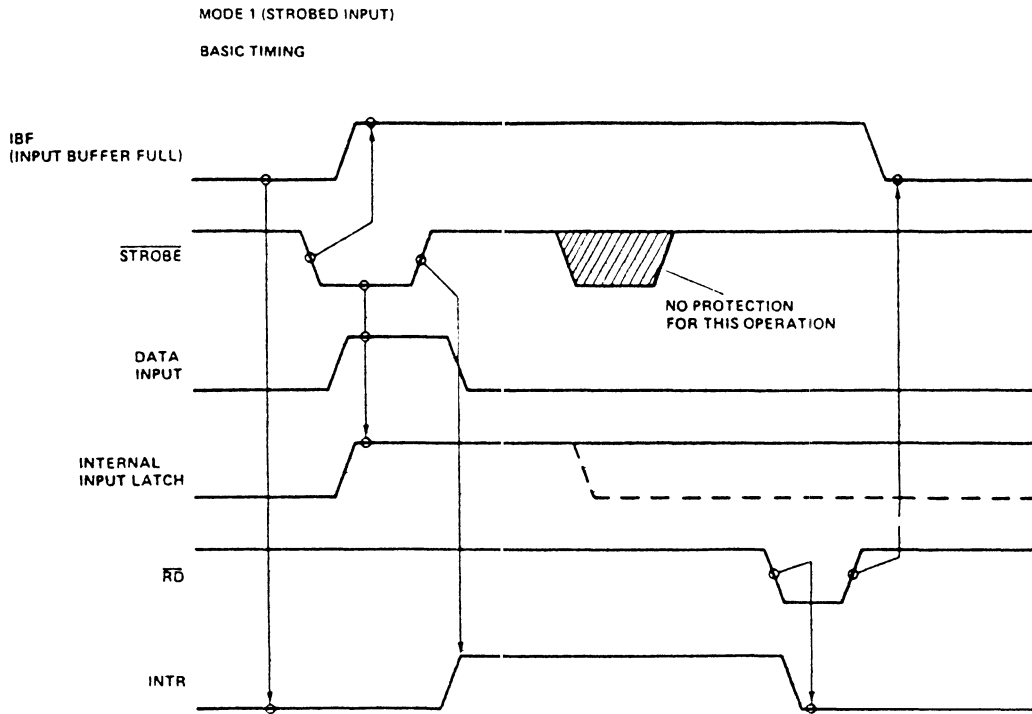


FIGURE 3-7. 8255A MODE 1 INPUT TIMING

when an output device has accepted data transmitted by the bus master. INTR is set by the rising edge of $\overline{\text{ACK}}$ if $\overline{\text{OBF}}$ is a 1 and INTE is a 1. It is reset by the falling edge of $\overline{\text{WR}}$.

INTE A

Controlled by bit set/reset of PC6.

INTE B

Controlled by bit set/reset of PC2.

Figure 3-8 illustrates the Mode 1 output configuration, while Figure 3-9 shows basic Mode 1 output timing.

Mode 2 (Strobed Bidirectional Bus I/O):

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Port A only.
- One 8-bit, bidirectional data Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control Port (Port C) is used for control and status for the 8-bit, bidirectional data Port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the bus master for both input or output operations.

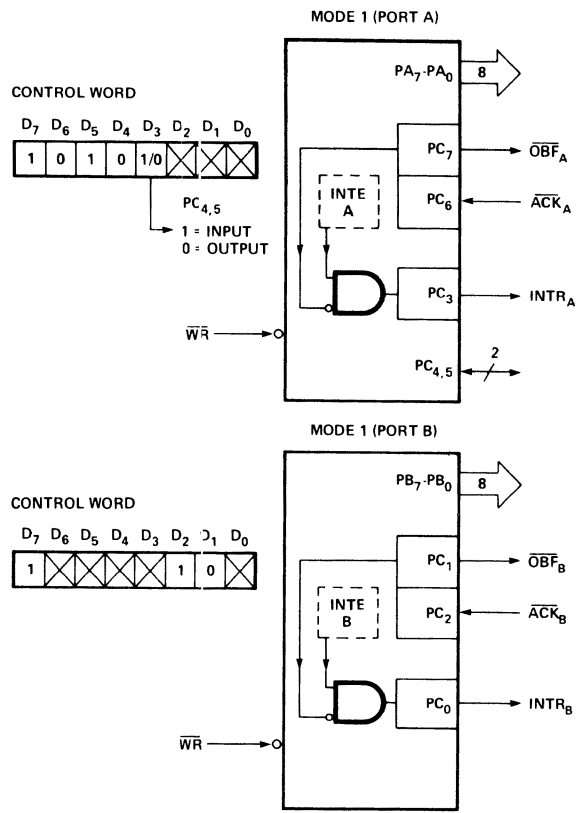


FIGURE 3-8. MODE 1 OUTPUT CONFIGURATION

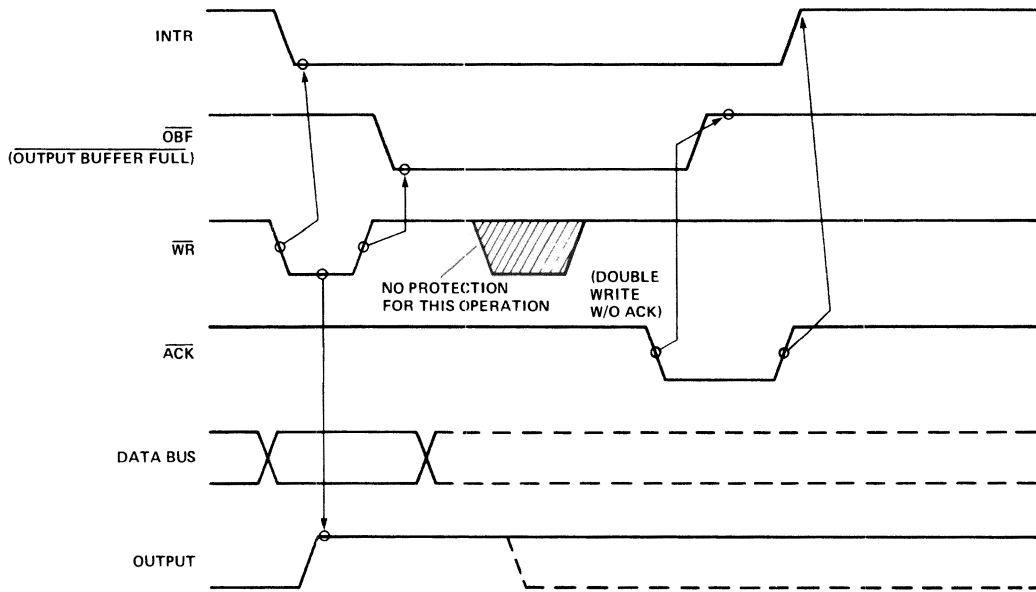


FIGURE 3-9. MODE 1 BASIC OUTPUT TIMING

Output Operation Control Signals

$\overline{\text{OBF}}$ (Output Buffer Full)

The $\overline{\text{OBF}}$ output will go low to indicate that the bus master has written data out to Port A.

$\overline{\text{ACK}}$ (Acknowledge)

A low on this input enables the 3-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTR A and B (The INTE flip-flop associated with $\overline{\text{OBF}}$)

Controlled by bit set/reset of PC6 (INTE 1)

Input Operation Control Signals

$\overline{\text{STB}}$ (Strobed Input)

A low on this input indicates that data has been loaded into the input latch.

IBF (Input Buffer Full F/F)

A high on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE flip-flop associated with IBF)

Controlled by bit set/reset PC4 (INTE 2)

$$\text{INTR}_A = \text{PC6} \cdot \overline{\text{OBF}}_A + \text{PC4} \cdot \text{IBF}_A$$

Figure 3-10 illustrates the port configuration for Mode 2, Figure 3-11 shows Mode 2 timing, and Table 3-2 summarizes 8255A Mode definition.

3.2.2 PARALLEL I/O CONFIGURATIONS

As shown on sheets 2 and 3 of the schematic, there are three 8255A devices, one located at A19, A22 and A23. For convenience the following device designations will be used: The device at A19 is called the "group 1" device, the device at A22 is referred to as the "group 2" device and

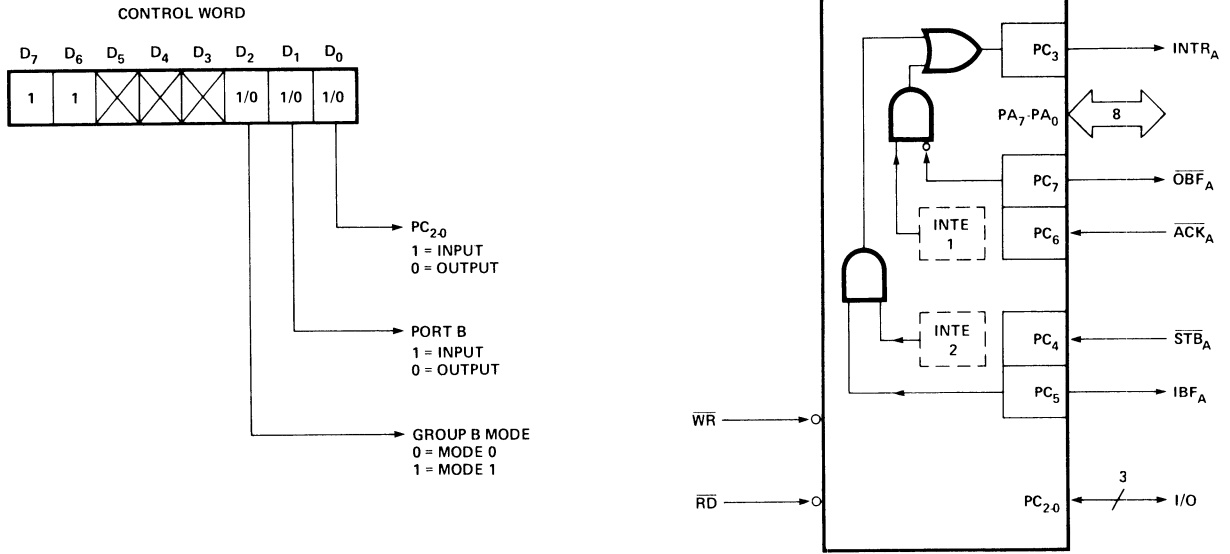


FIGURE 3-10. MODE 2 PORT CONFIGURATION

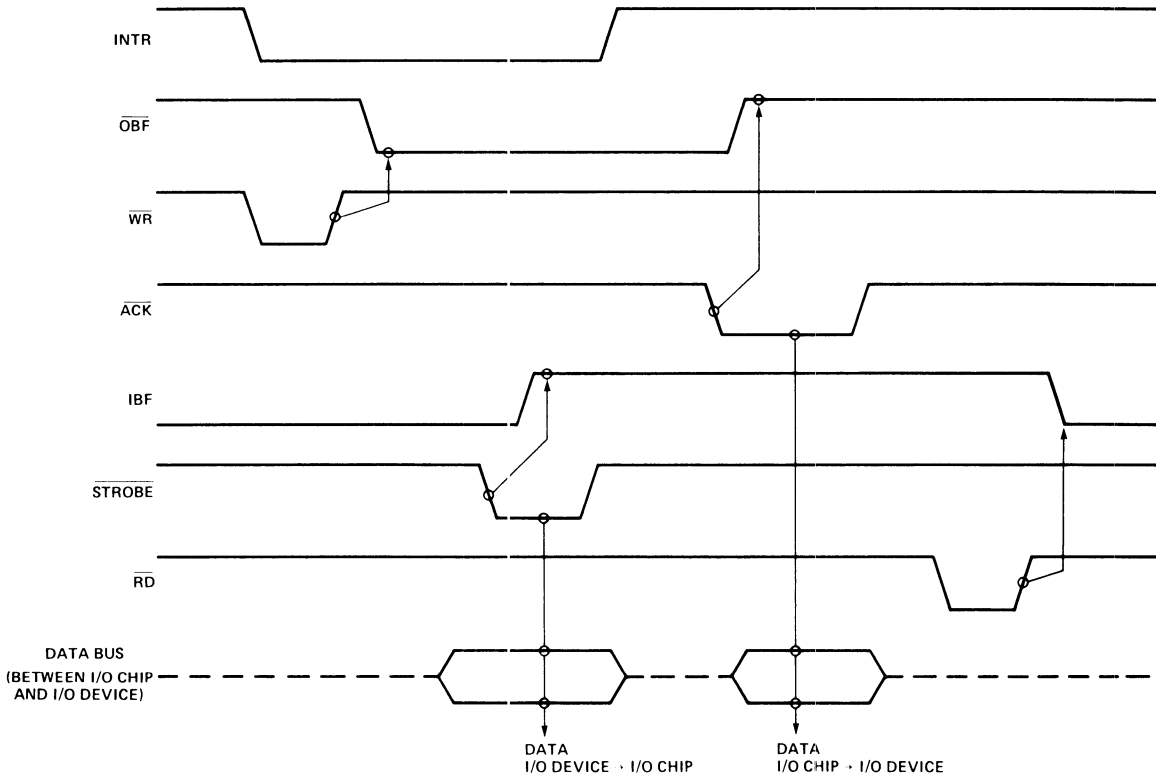


FIGURE 3-11. MODE 2 TIMING

MODE DEFINITION SUMMARY TABLE

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA ₀	IN	OUT	IN	OUT	↔
PA ₁	IN	OUT	IN	OUT	↔
PA ₂	IN	OUT	IN	OUT	↔
PA ₃	IN	OUT	IN	OUT	↔
PA ₄	IN	OUT	IN	OUT	↔
PA ₅	IN	OUT	IN	OUT	↔
PA ₆	IN	OUT	IN	OUT	↔
PA ₇	IN	OUT	IN	OUT	↔
PB ₀	IN	OUT	IN	OUT	—
PB ₁	IN	OUT	IN	OUT	—
PB ₂	IN	OUT	IN	OUT	—
PB ₃	IN	OUT	IN	OUT	—
PB ₄	IN	OUT	IN	OUT	—
PB ₅	IN	OUT	IN	OUT	—
PB ₆	IN	OUT	IN	OUT	—
PB ₇	IN	OUT	IN	OUT	—
PC ₀	IN	OUT	INTR _B	INTR _B	I/O
PC ₁	IN	OUT	IBF _B	OBFB	I/O
PC ₂	IN	OUT	STB _B	ACK _B	I/O
PC ₃	IN	OUT	INTR _A	INTR _A	INTR _A
PC ₄	IN	OUT	STB _A	I/O	STB _A
PC ₅	IN	OUT	IBF _A	I/O	IBF _A
PC ₆	IN	OUT	I/O	ACK _A	ACK _A
PC ₇	IN	OUT	I/O	OBFA	OBFA

MODE 0
OR MODE 1
ONLY

TABLE 3-2. 8255A MODE DEFINITION SUMMARY

the device at A23 is referred to as the "group 3" device. Each device has three eight-bit ports. The "group 1" ports are designated Ports 1, 2 and 3; the "group 2" ports are designated Ports 4, 5 and 6 and the "group 3" ports are designated Ports 7, 8 and 9.

All three groups communicate with the bus master via the bi-directional bus drivers A9 and A10. Except for their separate chip select lines, they all use the same signal lines: the 8-bit data bus (DB0-DB7) and five control/address lines (IOR/, IOW/, RESET, ADRO and ADR1). The three select lines are labeled 55 CS0/ (A19), 55 CS1/ (A22) and 55 CS2/ (A23). The data lines bring control bytes or data bytes to an 8255A or deliver data from an 8255A to the bidirectional data buffer at the interface. The chip select control signals, 55 CS0/, 55 CS1/ and 55 CS2/, select the group 1, 2 and 3 devices, respectively, when the proper I/O address appears on the system address bus. 55 CS0/, 55CS1/ or 55 CS2/ results from decoding address bits 2 through 7 (ADR2-7), as shown on sheet 1 of the schematic. The two least significant address bits (ADRO and ADR1) select the control register (when programming an 8255A) or one of the three I/O ports (when reading or writing data). IOR/ (8255A → bus master) and IOW/ (bus master → 8255A) indicate the direction of data flow, as summarized in Table 3-3. Specific I/O addresses for the nine ports and three 8255A control registers on the SBC-519 are listed in Table 3-4.

A high on the RESET line clears all internal 8255A registers including the control register; all ports (A, B and C) are set for input.

All three groups have the same interface characteristics with respect to the system bus. They are also both capable of the same range of configurations with respect to their peripheral interfaces.

TABLE 3-3. BASIC 8255A OPERATION FOR GROUP 1, 2 OR 3

<u>A1</u>	<u>A0</u>	<u>IOR/</u>	<u>IOW/</u>	<u>CS/</u>	<u>Input Operation (Read)</u>
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
					<u>Output Operation (Write)</u>
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					<u>Disable Function</u>
x	x	x	x	1	Data Bus → High-Impedance
1	1	0	1	0	Illegal

TABLE 3-4. PARALLEL I/O PORT ADDRESSES

<u>Port</u>	<u>8255 Device Location</u>	<u>*Eight-Bit Address (Hexadecimal)</u>
Group 1		
1	A19 Port (A)	X0
2	A19 Port (B)	X1
3	A19 Port (C)	X2
-	A19 Control	X3 For I/O write only.
Group 2		
4	A22 Port (A)	X4
5	A22 Port (B)	X5
6	A22 Port (C)	X6
-	A22 Control	X7 For I/O write only.
Group 3		
7	A23 Port (A)	X8
8	A23 Port (B)	X9
9	A23 Port (C)	XA
-	A23 Control	XB For I/O write only.

*Notes: X is any hex digit assigned by jumper selection

The operating characteristics of each port are determined by the mode and direction control information supplied by the bus master in its control word. In addition, certain mode/port relationships impose restrictions on the use of other ports in the group. These mode-related characteristics and restrictions are discussed briefly below. Details regarding mode implementation and the associated inter-port restrictions are presented in Chapter 4, User Selectable Options.

Since the three groups are functionally identical, only one group (group 1) will be referred to in the following discussion. Statements made about group 1 ports apply equally to group 2 and 3 ports. The reader should keep in mind, however, that the peripheral interface consists of three sets of equally versatile ports, which are independently programmed.

The allowable port configurations for each group are summarized below:

Port 1 (Group 1 Port A)

Mode 0 Input
Mode 0 Output (Latched)
Mode 1 Input (Strobed)
Mode 1 Output (Latched)
Mode 2 Bidirectional

Port 2 (Group 1 Port B)

Mode 0 Input
Mode 0 Output (Latched)
Mode 1 Input (Strobed)
Mode 1 Output (Latched)

Port 3 (Group 1 Port C)

Mode 0 8 Bit Input
Mode 0 8 Bit Output (Latched)
Mode 0 Split 4 bit input and 4 bit output

NOTE: Control mode dependent upon Port A and B mode.

Port 1 is the most versatile of the three group 1 ports. It can be programmed to function in any one of the three 8255A operating modes. The first port is the only port in the group that can communicate with its peripheral devices via bidirectional bus driver circuits (two 8226/16 bus driver devices at A40 and A41).

Before Port 1 is programmed for input or output in any one of three operating modes (as described in Section 3.2.1), certain jumper connections must be made to allow the port to function properly in the chosen mode. The 52-53-54-55 jumper pad specifies the direction of data flow for the two 8226/16 bidirectional bus drivers. If input in mode 0 or mode 1 is to be programmed for Port 1, jumper pair 52-55 should be connected. If output in mode 0 or mode 1 is to be used jumper pair 54-55 should be connected. If Port 1 is to be programmed for bidirectional mode 2, then a wire must be run from jumper pin 53 to pin 55. This connection allows the Port 3 acknowledge output ACK/, which is available at bit 6 of Port 3, to dynamically dictate direction for the two 8226/16 devices.

NOTE: *Indicates a default connection, which is the factory-selected connection. If some path other than the one provided by a default connection is selected (e.g., pins 52-55), the default wire must be removed (e.g., delete 53-55*)

When Port 1 is programmed for mode 1 or mode 2, an interrupt can be added to the Port 1 bit array by connecting jumper pins 74 and 77 (delete 75-77*). This allows the INTR output from bit 3 of Port 3 to activate the peripheral I/O interrupt request INTR PORT XØ. Refer back to Section 3.2.1 for details regarding INTR.

INTR PORT X0 is forwarded to the interrupt logic shown on sheet 1 of the schematic.

When Port 1 is in mode 0, which has no provision for interrupts, the default connections 64-73* and 75-77* must remain to allow the use of bit 3 of Port 3 and to inhibit Port 1 interrupts.

Because the 8226 bus drivers are inverting devices, all data input to or output from Port 1 is considered to be negative true with respect to the levels at the J1 edge connector. If 8216 bus drivers are used all data is positive true with respect to levels at the J1 edge connector.

Port 2 can be programmed for input or output in either mode 0 or mode 1 (see Section 3.2.1). If Port 2 is to be used for input (in either mode), terminator networks must be installed in the sockets at A43 and A29. Because of the passive nature of termination networks, data that is input to Port 2 must be positive true. If Port 2 is to be used for output (in either mode), driver networks must be installed in the sockets at A43 and A29. Assuming that the drivers are inverting devices, then the data being output will be negative true at the J1 edge connector.

When Port 2 is programmed for mode 1, a Port 2 interrupt can be implemented by connecting jumper pins 61-60 (delete 69-60*) . This allows the INTR output from bit 0 of Port 3 to activate the peripheral I/O interrupt request INTR PORT X1. This interrupt is forwarded to the interrupt logic shown on sheet 1 of the schematic.

When Port 2 is in mode 0, the default connections 61-70* and 69-60* must remain to allow the use of bit 0 of Port 3 and to inhibit Port 2 interrupts.

As was described in Section 3.2.1, the use of Port 3 depends on

the modes programmed for Ports 1 and 2. If Port 1 is in mode 1 or mode 2, bits 3, 4, 5, 6 and 7 of Port 3 can have the following dedicated control functions.

Port 3 bit 3	→ INTR (interrupt request)	- input or output	
Port 3 bit 4	← STB/ (input strobe)		} mode 1 input or mode 2
Port 3 bit 5	→ IBF (input buffer full flag)		
Port 3 bit 6	← ACK/ (output acknowledge)		} mode 1 output or mode 2
Port 3 bit 7	→ OBF/ (output buffer full flag)		

If Port 2 is in mode 1, bits 0, 1 and 2 of Port 3 have these dedicated control functions:

Port 3 bit 0	→ INTR (interrupt request)	- input or output	
Port 3 bit 1	→ IBF (input buffer full)		} input only
Port 3 bit 2	← STB/ (input strobe)		
Port 3 bit 1	→ OBF/ (output buffer full)		} output only
Port 3 bit 2	← ACK/ (output acknowledge)		

While certain Port 3 bits are available if Port 1 is in mode 1 or if Port 2 is in mode 0, the use of Port 3 as an eight-bit data path is restricted to those configurations that have both Port 1 and Port 2 programmed for mode 0. In this case all 8 bits of Port 3 can be programmed for mode 0 input (termination networks must be installed in the sockets at A28 and A42) or output (driver networks must be installed at A28 and A42) or split 4 bits input and 4 bits output.

NOTE: If Port 1 and 2 are not both in mode 0, then a driver network must be installed in the sockets at A42 and a termination network must be installed at A28, so that the Port 3 control lines can function properly.

3.3 INTERRUPT CONTROLLER

The Interrupt Controller logic consists of Intel's powerful 8259 Interrupt Controller device and various sets of jumper pins that allow the user to select up to eight interrupt sources out of 10 possible sources for connection to the 8259's eight interrupt request inputs.

The 8259 resolves priority among the eight levels according to an algorithm that is program-selected by the user. The Interrupt Controller is shown on sheet 1 of the SBC-519 schematic (Appendix A).

Section 3.3.1 provides a basic functional description of the 8259 and Section 3.3.2 summarizes the operational characteristics of the 8259.

3.3.1 8259 BASIC FUNCTIONAL DESCRIPTION

The 8259 is a device specifically designed for use in real time interrupt driven, microcomputer systems. It manages eight levels of requests. It is programmed by the system's software as an I/O peripheral. A selection of priority algorithms is available to the programmer so that the manner in which the requests are processed by the 8259 can be configured to match the user's system requirements. The priority assignments and algorithms can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

A functional block diagram of the 8259 is shown in Figure 3-12.

The various functional blocks are described below:

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels that

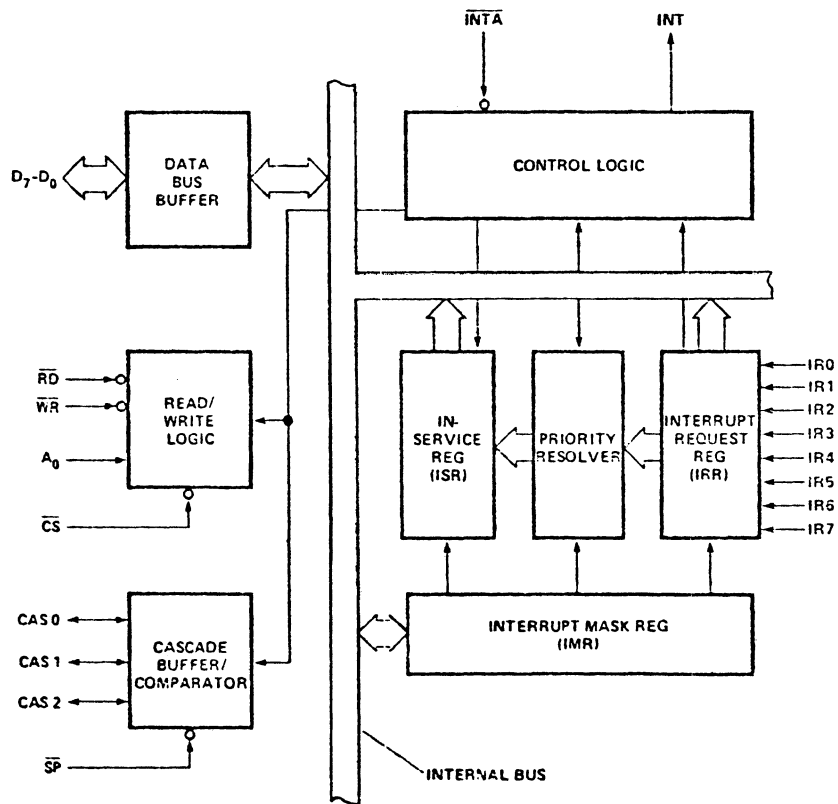


FIGURE 3-12. 8259 INTERRUPT CONTROLLER

are requesting service; and the ISR is used to store all the interrupt levels that are being serviced.

Whenever there is a positive transition at an IR input, the corresponding IRR bit is set and the INT line is raised high. Since IRR bits are set independently of one another, more than one IRR bit can be set at the same time so long as they are not masked. Masked IRR bits are held reset regardless of any transitions at their IR inputs.

The bus master responds to the interrupt request (INT) by placing the 8259 in the polled mode and then reading the 8259 port. The resulting RD/ pulse sets the ISR bit that corresponds to the highest priority active (set) IRR bit and then resets that IRR bit. The ISR bit remains set during the service routine until an EOI (End of Interrupt) or SEOI (Specific End of Interrupt) command is received by the 8259.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during RD/ pulse.

INT (Interrupt)

This output goes to the bus master.

INTA/(Interrupt Acknowledge)

This input is not used in the SBC-519's 8259.

Interrupt Mask Register (IMR)

The IMR stores the bits of the interrupt lines to be masked. The IMR operates on both the IRR and the ISR. Masking of a higher priority

bit will not affect the interrupt request lines of lower priority.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8259 to the SBC-519's internal data bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept commands from the bus master. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers, which store the various control formats for device operation. This function block also allows the status of the 8259 to be transferred onto the SBC-519 internal data bus.

CS/(Chip Select)

A "low" on this input enables the 8259. No reading or writing of the chip will occur unless the device is selected.

WR/(Write)

A "low" on this input enables the bus master to write control words (ICWs and OCWs) to the 8259.

RD/(Read)

A "low" on this input enables the 8259 to send the status of the interrupt Request Register (IRR). In Service Register (ISR), the Interrupt Mask Register (IMR) or the BCD of the interrupt level on to the data bus.

A0

This input signal is used in conjunction with WR/ and RD/ signals to write commands into the various command registers as well as reading the various status registers of the chip. In the SBC-519, this line is tied directly to system address bit 0.

SP/(Slave Program)

Not used in SBC-519.

3.3.2 8259 DETAILED OPERATIONAL SUMMARY

The powerful features of the 8259, as implemented in the SBC-519, are its programmability and its utilization of an interrupt vector response to a poll from the bus master. The normal sequence of events that the 8259 interacts with the Bus Master is as follows:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high signaling the 8259 that the corresponding peripheral equipment(s) is demanding service.
2. The 8259 accepts these requests, resolves the priorities and sends an INT to the bus master.
3. The Bus Master acknowledges the INT by outputting an OCW3 word to the 8259 with the P bit set. This places the 8259 in the polled mode.
4. Following this OCW3, the bus master issues a RD/pulse to the 8259.
5. The RD/pulse causes the 8259 to set the appropriate IS flip-flop and gates the BCD code of the highest priority level requesting service out to the Bidirectional Data Buffer (A9, A10). The BCD code occupies bits 0-2 of the 8259 output byte. Bit 7 is an interrupt flag and is set. See Figure 3-13.
6. The same RD/pulse enables the bus driver elements of the Bidirectional Data Buffer, which drive the BCD code and interrupt flag onto the system data bus.

7. The bus master shifts the BCD code two places to the left and adds it to the base address of the jump table. The resulting vector points to the location in the jump table that contains the base address of the appropriate interrupt service routine. The bus master jumps to that location and begins servicing the interrupt.
8. At the conclusion of the service routine, the bus master outputs an OCW2 with the EOI or SEOI bit set. If the EOI bit is set, the highest level active ISR bit is reset. If the SEOI bit is set, the BCD code of the appropriate priority level is also supplied in the OCW2 to specify the ISR bit that is to be reset. In either case, the EOI or SEOI bit resets the IS flip-flop that corresponds to the interrupt service routine just completed.

D7	D6	D5	D4	D3	D2	D1	D0
1					W2	W1	W0

W0-2: BCD code of the highest priority level requesting service.

I: Interrupt flag = 1

(): Undefined

FIGURE 3-13. PRIORITY LEVEL BCD CODE

Programming the 8259

The 8259 accepts two types of command words generated by the bus master.

1. Initialization Command Words (ICWs): Before normal operation can begin, the 8259 must be brought to a starting point--by a two-byte ICW sequence, timed by WR/pulses. This sequence is shown in Figure 2.2.

NOTE: Bit D0 through D3 and A5 through A15 are ignored by the SBC-519's 8259. They can assume any value without affecting operation of this 8259. However, they do have significance in other 8259 applications.

2. Operation Command Words (OCWs): These are the command words that command the 8259 to operate in various modes, including:
 - Rotating priority mode
 - Special mask mode

- Polled mode (This mode is always in effect during interrupt servicing.)

The OCWs can be written into the 8259 at anytime during operation.

Initialization Command Words 1 and 2: (ICW1 and ICW2)

Whenever a command is issued with A0 = 0 and D4 = 1 this is interpreted as Initialization Command Word 1 (ICW1), and initiates the initialization sequence. During this sequence, the following occur automatically:

- a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low to high transition to generate an interrupt.
- b. The interrupt Mask Register is cleared.
- c. IR 7 input is assigned priority 7.
- d. Special Mask Mode Flip-flop and status Read Flip-flop are reset.

Initialization Command Word 2 (ICW2) is received by the 8259 right after ICW1. ICW1 provides two psuedo control bits and 2 or 3 psuedo interrupt CALL address bits. ICW2 provides 8 additional psuedo CALL address bits. These are referred to here as psuedo control and CALL address bits because the SBC-519 8259 does not use them. While they have no significance in the SBC-519, the Initialization Command Words are required by the 8259 and, so, are a necessary part of the 8259 programming architecture.

Operation Command Words (OCWs)

After the ICWs are programmed into the 8259, the chip is ready to accept interrupt requests at its input lines. At any time following initialization sequence, a selection of algorithms can command the 8259 to operate in various modes through the Operation Command Words (OCWs).

One of these modes, the polled mode, is invoked each time the 8259 issues an INTR/ to the bus master. The other modes are optional and can be implemented as needed to change priority relationships (rotating priority mode) or disable selected interrupt levels (mask mode).

These modes and their associated OCWs are summarized in Table 3-5 and Figure 3-14 and are described below.

Polled Mode

The 8259 enters the polled mode when it receives an OCW3 command with the P bit set. This occurs in response to the INTR/ signal that the 8259 issues to the bus master. The 8259 issues INTR/ whenever its highest priority interrupt request is not currently being serviced. INTR/ may occur during the service routine for a lower priority interrupt. How such events are managed is entirely a function of program structure. For example, the current service routine can be allowed to run to completion before servicing the new, higher priority request. In this case, the bus master INT input would remain disabled until completion of the service routine. Or, a routine nesting procedure can be used to process the higher priority request immediately. This technique requires that the bus master's INT input be enabled (via the EI instruction) while each service routine is being executed.

When in the polled mode, the 8259 treats the subsequent RD/ pulse as an interrupt acknowledge. It resets the appropriate IR flip-flop, sets the corresponding IS flip-flop and enables the BCD code representing the interrupting level onto the data bus. This BCD code is used by the CPU as a pointer to a jump table. The designated jump table location contains the base address of the appropriate interrupt service routine. When the service routine is completed, it removes the 8259 from the polled mode. See Appendix C for additional service routine design information.

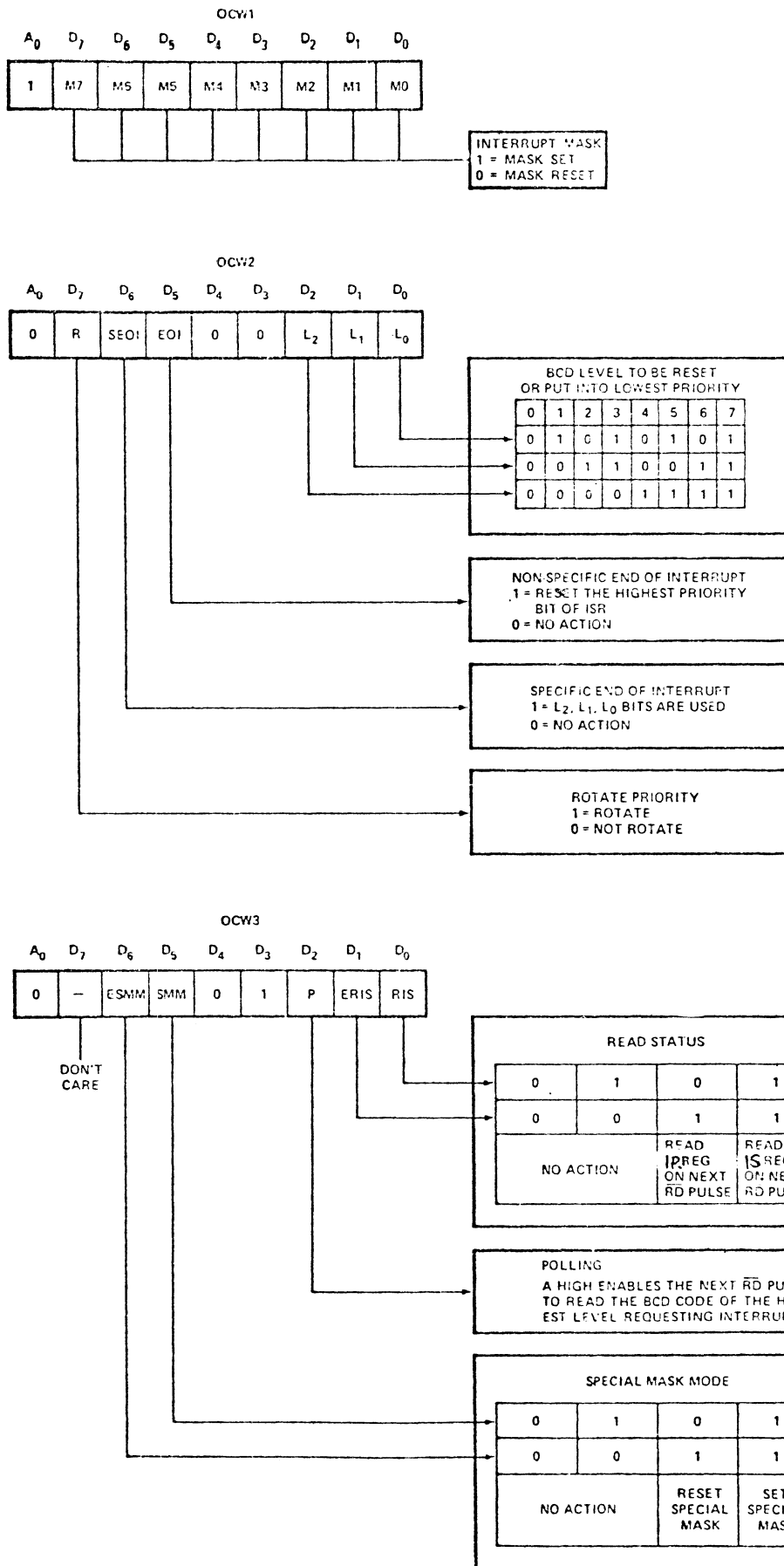


FIGURE 3-14. OPERATION COMMAND WORD FORMATS

TABLE 3-5. SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

	A0	D4	D3																																		
OCW1	1			M7-M0	IMR (Interrupt Mask Register). \overline{WR} will load it while status can be read with \overline{RD} .																																
OCW2	0	0	0	<table border="0"> <tr> <td>R</td> <td>SEOI</td> <td>EOI</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </table>	R	SEOI	EOI	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	1	1	0	1	1	1	<p>No Action.</p> <p>Non-specific End of Interrupt.</p> <p>No Action.</p> <p>Specific End of Interrupt: L2, L1, L0 is the BCD level to be reset.</p> <p>No Action.</p> <p>Rotate priority at EOI. (Auto Mode)</p> <p>Rotate priority, L2, L1, L0 becomes bottom priority without Ending of Interrupt.</p> <p>Rotate priority at EOI (Specific Mode), L2, L1, L0 becomes bottom priority, and its corresponding IS FF is reset.</p>					
R	SEOI	EOI																																			
0	0	0																																			
0	0	1																																			
0	1	0																																			
0	1	1																																			
1	0	0																																			
1	0	1																																			
1	1	0																																			
1	1	1																																			
OCW3	0	1	0	<table border="0"> <tr> <td>ESMM</td> <td>SMM</td> </tr> <tr> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>ERIS</td> <td>RIS</td> </tr> <tr> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </table>	ESMM	SMM	0	0	0	1	1	0	1	1	ERIS	RIS	0	0	0	1	1	0	1	1	<table border="0"> <tr> <td style="font-size: 2em;">}</td> <td>Special Mask not Affected.</td> </tr> <tr> <td></td> <td>Reset Special Mask.</td> </tr> <tr> <td></td> <td>Set Special Mask.</td> </tr> <tr> <td style="font-size: 2em;">}</td> <td>No Action.</td> </tr> <tr> <td></td> <td>Read IR Register Status.</td> </tr> <tr> <td></td> <td>Read IS Register Status.</td> </tr> </table>	}	Special Mask not Affected.		Reset Special Mask.		Set Special Mask.	}	No Action.		Read IR Register Status.		Read IS Register Status.
ESMM	SMM																																				
0	0																																				
0	1																																				
1	0																																				
1	1																																				
ERIS	RIS																																				
0	0																																				
0	1																																				
1	0																																				
1	1																																				
}	Special Mask not Affected.																																				
	Reset Special Mask.																																				
	Set Special Mask.																																				
}	No Action.																																				
	Read IR Register Status.																																				
	Read IS Register Status.																																				

* Note: The 8080 INT input must be disabled during:

1. Initialization sequence for all the 8259 in the system.
2. Any control command execution.

Interrupt Masks

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. The IMR will operate on both the Interrupt Request Register and the In-Service Register.

CAUTION

When interrupt sources are asynchronous with respect to the main program, it is possible for an ISR bit to be set between the time the program reads the IR status and the time it masks that IR level with an OCW1. If this happens, the IR level, although masked, will still inhibit the lower priorities. If desired, the lower priority interrupts can be enabled in either of two ways: (1) Write an End of Interrupt (EOI) command (OCW2) to reset the masked ISR bit or (2) Set the Special Mask Mode (SMM) using OCW3; the SMM technique is discussed later in the Special Mask Mode description.

Rotating Priority Mode

The Rotating Priority Mode of the 8259 serves an application of interrupting devices of equal priority such as communication channels. There are two variations of the rotating priority mode:

1. Auto Mode -- In this mode, a device after being serviced receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case, until 7 other devices are serviced at most once each, i.e., if the priority and "in service" status is:

<u>BEFORE ROTATE</u>	<u>IS7</u>	<u>IS6</u>	<u>IS5</u>	<u>IS4</u>	<u>IS3</u>	<u>IS2</u>	<u>IS1</u>	<u>IS0</u>
"IS" STATUS	0	1	0	1	0	0	0	0
		<u>LOWEST PRIORITY</u>				<u>HIGHEST PRIORITY</u>		
PRIORITY STATUS	7	6	5	4	3	2	1	0
<u>AFTER ROTATE</u>	<u>IS7</u>	<u>IS6</u>	<u>IS5</u>	<u>IS4</u>	<u>IS3</u>	<u>IS2</u>	<u>IS1</u>	<u>IS0</u>
"IS" STATUS	0	1	0	0	0	0	0	0
		<u>LOWEST PRIORITY</u>				<u>HIGHEST PRIORITY</u>		
PRIORITY STATUS	4	3	2	1	0	7	6	5

In this example, the In-Service FF corresponding to line 4 (the highest priority FF set) was reset and line 4 became the lowest priority, while all the other priorities rotated correspondingly. The Rotate command is issued in OCW2, where: R = 1, EOI = 1, SEOI = 0.

2. Specific Mode -- The programmer can change priorities by programming the bottom priority, and by doing this, to fix the highest priority: i.e., if IR5 is programmed as the bottom priority device, the IR6 will have the highest one.

The Rotate command is issued in OCW2 where: R = 1, SEOI = 1, L2, L1, L0 are the BCD priority level code of the bottom priority device.

Observe that this mode is independent of the End of Interrupt Command and priority changes can be executed during EOI command or independently from the EOI command.

End of Interrupt (EOI) and Specific End of Interrupt (SEOI)

An End of Interrupt command word must be issued to the 8259 before returning from a service routine, to reset the appropriate IS bit.

There are two forms of EOI command: Specific and non-Specific. When the 8259 is operated in modes which preserve the fully nested structure, it can determine which IS bit is to be reset on EOI. When a non-Specific EOI command is issued the 8259 will automatically reset the highest IS bit of those that are set, since in the nested mode, the highest IS level was necessarily the last level acknowledged and will necessarily be the next routine level returned from.

However, when a mode is used which may disturb the fully nested

structure, such as in the rotating priority case, the 8259 may no longer be able to determine the last level acknowledged. In this case, a specific EOI (SEOI) must be issued which includes the IS level to be reset as part of the command. The End of the Interrupt is issued whenever EOI = "1" in OCW2. For specific EOI, SEOI = "1", and EOI = 1, L2, L1, L0 is then the BCD level to be reset. As explained in the Rotate Mode earlier, this can also be the bottom priority code. Note that although the Rotate command can be issued during an EOI = 1, it is not necessarily tied to it.

Special Mask Mode (SMM)

This mode is useful when some bit(s) are set (masked) by the Interrupt Mask Register (IMR) through OCW1. If, for some reason, we are currently in a subroutine which is masked (this could happen in two manners. (1) RD from bus master acknowledges the IR just before it is masked; (2) the subroutine intentionally masks itself off) it is still possible to enable the lower priority lines by setting the Special Mask mode. In this mode, the lower priority lines are enabled until the SMM is reset. The higher priorities are not affected.

The special mask mode FF is set by OCW3 where ESMM = 1, SMM = 1, and reset where: ESMM = 1 and SMM = 0.

Reading 8259 Status

The input status of several internal registers can be read to update the user information on the system. The following registers can be read by issuing a suitable OCW and reading with RD/ for the data bus lines:

Interrupt Requests Register (IRR): 8-bit register which contains the priority levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged.

In Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when prior to the RD/ pulse, an WR/ pulse is issued with OCW3, and ERIS = 1, RIS = 0.

The ISR can be read in a similar mode, when ERIS = 1, RIS = 1.

There is no need to write an OCW3 before every status read operation as long as the status read corresponds with the previous one, i.e., the 8259 "remembers" whether the IRR or ISR has been previously selected by the OCW3. On the other hand, for polling operation, an OCW3 must be written before every read.

For reading the IMR, a WR/ pulse need not precede the RD/ pulse. The output data bus will contain the IMR whenever RD/ is active and A0 = 1.

Polling overrides status read when P = 1, ERIS = 1 in OCW3.

Appendix C is a sample of an Interrupt Service Routine using the 8259. This program shows the initialization sequence, and the software required to communicate with it.

3.4 INTERVAL TIMER

The Interval Timer is formed by a cascaded set of four binary counters (A14, A15, A16 and A17), with a D-type flip-flop (A24-5/6) at the timer output.

The timer circuit is driven by the system's CCLK/ (Constant Clock). When supplied by an SBC 80/10 or 80/20, CCLK/ has a frequency of 9.216 MHz (108.5 ns). A jumper pad in the timer circuit provides the means for

selecting one of four possible real time interrupt periods (e.g., 0.5 ms, 1* ms, 2 ms or 4 ms for SBC 80/10 or 80/20).

The flip-flop (A24-5/6) is set by the timer output at regular intervals, as determined by the jumper selection. The latch output, RTI/, can be connected by jumper (pins 49-50) to the 8259's IRO input (normally highest priority). If desired, the IRO input can be disabled by connecting pins 50-51.

In either case, RTI/ can also be sampled by the bus master on system data line 0 by issuing an I/O read command to address XE or XF. The rest of the data lines (D1-D7) are undefined during this operation. The high-order hex digit (X) must match the SBC-519's selected base I/O address.

* Default selection.

CHAPTER 4

USER SELECTABLE OPTIONS

The SBC-519 provides the user with a powerful and flexible parallel I/O capability as well as a versatile vectored priority interrupt scheme.

The parallel I/O interface, using three Intel 8255A Programmable Peripheral Interface devices, provides 72 signal lines for the transfer and control of data to or from peripheral devices. Sockets are provided for the installation of active driver networks or passive termination networks, as required to meet the needs of the user system. Bidirectional bus driver chips (Intel 8216 or 8226) can be installed in the sockets assigned to port A of any of the 8255A device.

The vectored priority interrupt structure, using Intel's 8259 Interrupt Controller, allows up to eight interrupt sources to request service in a controlled-priority environment. These eight interrupt sources can be selected by jumper from 10 potential sources.

In this chapter, each of the options available to the user will be reviewed and the specific information required to implement the desired characteristic will be summarized.

NOTE: Where jumper-selected options are listed, an asterisk (*) is used to identify the factory-installed default connection.

4.1 BASE I/O ADDRESS SELECTION

The SBC-519's base address is selected using jumper wires at pin set 36, 37, 38 and at jumper pad S1. Table 4-1 identifies the base address that is implemented for each jumper combination.

TABLE 4-1. BASE I/O ADDRESS SELECTION

Pin Set 36,37,38	S1	Base Addr	Pin Set 36,37,38	S1	Base Addr
37-38*	48-46*	00	37-36	48-46*	80
	48-45	10		48-45	90
	48-44	20		48-44	40
	48-43	30		48-43	B0
	48-42	40		48-42	CO
	48-41	50		48-41	DO
	48-40	60		48-40	EO
37-38*	48-39	70	37-36	48-39	FO

4.2 ADVANCE/TRANSFER ACKNOWLEDGE TIMING

The SBC-519's Advance Acknowledge and Transfer Acknowledge response timing is selected in approximately 100 ns increments by hardwire connections at the outputs of A18. Table 4-2 shows the range of response timing for each possible connection in terms of CCLK periods. This range occurs because of the skew introduced into the acknowledge circuit by the use of CCLK to drive A18. Actual time values for these periods depend, of course, on the frequency of CCLK. For SBC 80/10 or 80/20, CCLK is 9.216 MHz, which provides a clock period of approximately 100 ns.

TABLE 4-2. ADVANCE/TRANSFER ACKNOWLEDGE TIMING

Pin Connections		Delay from Receipt of CMD to ACK Generation
AACK	XACK	
34-24*		Immediate
34-25		0 to 1 CCLK Period
34-26		1 to 2
34-27		2 to 3
34-28		3 to 4
34-29	35-29*	4 to 5
34-30	35-30	5 to 6
34-31	35-31	6 to 7
34-32	35-32	7 to 8 CCLK Periods

NOTE: For XACK, connect pins 35-29* for either SBC 80/10 or 80/20. For AACK, connect pins 34-24* for SBC 80/10 and connect pins 34-33 for SBC 80/20.

4.3 INTERVAL TIMER PERIOD SELECTION

Four different intervals are available for use as the real time interrupt. The desired interval is selected by connecting the appropriate jumper pins in pin set 19, 20, 21, 22, 23. Table 4-3 identifies the interrupt interval that is selected for each possible jumper connection if CCLK is 9.216 MHz. The method for calculating the interval values for other CCLK frequencies is also shown.

TABLE 4-3. INTERVAL TIMER PERIOD SELECTION

Pin Connection	Interrupt Interval	
	For CCLK Equal to 9.216 MHz	For Other CCLK Frequencies
23-19	0.5 ms	$4068 \times 1/\text{CCLK}$
23-20*	1 ms	$9216 \times 1/\text{CCLK}$
23-21	2 ms	$18,432 \times 1/\text{CCLK}$
23-22	4 ms	$36,864 \times 1/\text{CCLK}$

4.4 PARALLEL I/O OPTIONS

The Parallel I/O Interface consists of nine 8-bit I/O ports implemented with three Intel 8255A Programmable Peripheral Interface devices. The primary user considerations in determining how to use each of the nine I/O ports are:

- 1) choice of operating mode (as defined in Section 3.2.1),
- 2) direction of data flow (input, output or bidirectional),
- 3) choice of driver/termination networks for port's data path.

In the following paragraphs, we will define the capabilities of each port and summarize, in tables, that information which is necessary to use the port in each of its potential configurations. Each table will list the port I/O address, the control register address and the format for the control word that is output to the 8255A by the bus master and that specifies the particular configuration to be used. Each table will also summarize all of the relevant information concerning the choice and use of driver/termination networks, the data polarity, the connecting of jumpers and what they enable, and any restrictions on the use of the other two ports in each group. Examples of suitable driver/termination networks are listed in Section 5.1.

The configuration tables for group 2 and 3 ports are identical to those for group 1 ports except for I/O address, port numbers, component location numbers and jumper pin numbers. For this reason the tables are organized as three sets: Ports 1, 4 and 7, Ports 2, 5 and 8 and Ports 3, 6 and 9.

At the beginning of each set, the general characteristics of

that port are reviewed. Where port numbers are used in the text, the group 1 number is presented first and the corresponding group 2 and 3 numbers follow in parentheses. For example, when referring to B ports, the reference will appear as Port 2(5,8).

The introductory text is followed by a series of tables that cover all of the configurations that are possible for the ports under discussion. To simplify the search for specific tables, each table is presented on a separate page.

Table 4-4 summarizes the various mode combinations that are possible with Ports A and B and indicates how each Port C bit can or cannot be used for each mode combination. This table can serve as a useful starting point for selecting an I/O configuration for any group of ports. Once the desired mode combination is selected and the Port C bit assignments are made, the appropriate configuration tables (Tables 4-5 through 4-46) can be referred to for implementation details.

4.4.1 PORTS 1,4 AND 7 (8255A PORT A)

Port 1(4,7) is the only port that can use a bidirectional driver/termination network (two 8226 or 8216 Bidirectional Bus Drivers). Port 1(4,7) is also the only port that can be programmed to function in any one of the three 8255A operation modes, which were defined in Section 3.2.1. Before Port 1(4,7) is programmed for input or output in any one of the three modes, certain jumper connections must be made to allow the port to function properly in the chosen mode. In all, there are five potential configurations for Port 1(4,7). All of the necessary information for

TABLE 4-4. PARALLEL I/O INTERFACE CONFIGURATIONS

CONFIGURATION NUMBER	8255 PORT A	8255 PORT B	8255 PORT C Lower				8255 PORT C Upper			
			C ₀	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇
1	MODE \emptyset -I	MODE \emptyset -I/O	---	I/O	---	---	I/O	---		
2	MODE \emptyset -O	MODE \emptyset -I/O	---	I/O	---	---	I/O	---		
3	MODE \emptyset -I	MODE 1-I/O	R	R	R	I	O	O	O	
4	MODE \emptyset -I	MODE 1-I/O	R	R	R	O	I	I	I	
5	MODE \emptyset -O	MODE 1-I/O	R	R	R	I	O	O	O	
6	MODE \emptyset -O	MODE 1-I/O	R	R	R	O	I	I	I	
7	MODE 1-I	MODE \emptyset -I/O	I	I	I	R	R	R	O	
8	MODE 1-I	MODE \emptyset -I/O	O	O	O	R	R	R	I	
9	MODE 1-O	MODE \emptyset -I/O	I	I	I	R	O	O	R	
10	MODE 1-O	MODE \emptyset -I/O	O	O	O	R	I	I	R	
11	MODE 1-I	MODE 1-I/O	R	R	R	R	R	R	I	
12	MODE 1-I	MODE 1-I/O	R	R	R	R	R	R	O	
13	MODE 1-O	MODE 1-I/O	R	R	R	R	I	I	R	
14	MODE 1-O	MODE 1-I/O	R	R	R	R	O	O	R	
15	MODE 2-B	MODE \emptyset -I/O	U	I	I	R	R	R	R	
16	MODE 2-B	MODE \emptyset -I/O	U	O	O	R	R	R	R	
17	MODE 2-B	MODE 1-I/O	R	R	R	R	R	R	R	

I = INPUT
O = OUTPUT
I/O = INPUT OR OUTPUT
B = BIDIRECTIONAL

R = Reserved
U = No unused drivers/terminators available. These bits may be used, however, to connect to the serial I/O interface or the Interval Timer.

implementing each configuration has been summarized in the following tables:

PORT 1(4,7) CONFIGURATIONS		TABLES		
<u>Mode</u>	<u>Direction</u>	<u>Group 1</u>	<u>Group 2</u>	<u>Group 3</u>
1. Mode 0	Input	4-5	4-6	4-7
2. Mode 0	Output (Latched)	4-8	4-9	4-10
3. Mode 1	Input (Strobed)	4-11	4-12	4-13
4. Mode 1	Output (Latched)	4-14	4-15	4-16
5. Mode 2	Bidirectional	4-17	4-18	4-19

TABLE 4-5. PORT 1, MODE 0 INPUT CONFIGURATION

<u>PORT 1 ADDRESS:</u> X0,		<u>CONTROL REGISTER ADDRESS:</u> X3						
<u>CONTROL WORD FORMAT:</u>	7	6	5	4	3	2	1	0
	1	0	0	1				
<u>DRIVER/TERMINATION NETWORKS:</u>	Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A40 and A41. If mode 2 will not be used, TTL termination networks can be used instead at A26 and A27.							
<u>DATA POLARITY AT J1:</u>	Negative for bidirectional drivers; positive for termination networks.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>					
* = Default connection	53-55*	52-55	Enable input at 8226's					
<u>PORT RESTRICTIONS</u> -	<p>PORT 2: None; Port 2 can be programmed for mode 0 or mode 1, input or output.</p> <p>PORT 3: None; Port 3 can be programmed for mode 0, 8-bit input or output, unless Port 2 is in mode 1.</p>							

TABLE 4-6. PORT 4, MODE 0 INPUT CONFIGURATION

<u>PORT 4 ADDRESS:</u> X4,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0	1				
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A45 and A46. If mode 2 will not be used, TTL termination networks can be used instead at A26 and A27.							
<u>DATA POLARITY AT J2:</u>		Negative true for bidirectional drivers; positive true for termination networks.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default Connection	83-85*	82-85	Enable input at 8226's						
<u>PORT RESTRICTIONS</u> - PORT 5:		None; Port 5 can be programmed for mode 0 or mode 1, input or output.							
PORT 6:		None; Port 6 can be programmed for mode 0, 8-bit input or output, unless Port 5 is in mode 1.							

TABLE 4-7. PORT 7, MODE 0 INPUT CONFIGURATION

<u>PORT 1 ADDRESS:</u> X8,		<u>CONTROL REGISTER ADDRESS:</u> XB							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0	1				
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A50 and A51. If mode 2 will not be used, TTL termination networks can be used instead at A26 and A27.							
<u>DATA POLARITY AT J1:</u>		Negative for bidirectional drivers; positive for termination networks.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	109-111*	108-111	Enable input at 8226's						
<u>PORT RESTRICTIONS - PORT 8:</u>		None; Port 8 can be programmed for mode 0 or mode 1, input or output.							
		PORT 9: None; Port 9 can be programmed for mode 0, 8-bit input or output, unless Port 8 is in mode 1.							

TABLE 4-8. PORT 1, MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 1 ADDRESS:</u> X0, <u>CONTROL REGISTER ADDRESS:</u> X3									
<u>CONTROL WORD FORMAT:</u>	7 6 5 4 3 2 1 0								
	<table border="1"> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td></td> <td></td> <td></td> <td></td> </tr> </table>	1	0	0	0				
1	0	0	0						
<u>DRIVER/TERMINATION NETWORKS:</u>	Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A40 and A41. If mode 2 will not be used, a TTL driver network can be used instead at A26 and A27.								
<u>DATA POLARITY AT J1:</u>	Negative true								
<u>JUMPER ACTION:</u>	<u>DELETE</u> <u>ADD</u> <u>EFFECT</u>								
* = Default connection	53-55* 54-55 Enable output at 8226's								
	75-77* Disables INTR PORT X0								
<u>PORT RESTRICTIONS</u> - PORT 2:	None; Port 2 can be in mode 0 or mode 1, input or output.								
	PORT 3: None; Port 3 can be in mode 0, 8-bit input or output, unless Port 2 is in mode 1.								

TABLE 4-9. PORT 4, MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 4 ADDRESS:</u> X4,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0	0				
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A45 and A46. If mode 2 will not be used, TTL driver networks can be used instead at A26 and A27.							
<u>DATA POLARITY AT J2:</u>		Negative true							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	83-85*	84-85	Enable output at 8226's						
		78-80*	Disable INTR PORT X4						
<u>PORT RESTRICTIONS:</u>		- PORT 5: None; Port 5 can be in mode 0 or mode 1, input or output.							
		PORT 6: None; Port 6 can be in mode 0, 8-bit input or output, unless Port 5 is in mode 1.							

TABLE 4-10. PORT 7, MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 1 ADDRESS:</u> X8,		<u>CONTROL REGISTER ADDRESS:</u> XB							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0	0				
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A50 and A51. If mode 2 will not be used, a TTL driver network can be used instead at A26 and A27.							
<u>DATA POLARITY AT J1:</u>		Negative true.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	109-111*	110-111	Enable output at 8226's						
		104-103*	Disables INTR PORT X8						
<u>PORT RESTRICTIONS</u> - PORT 8:		None; Port 8 can be in mode 0 or mode 1, input or output.							
	PORT 9:	None; Port 9 can be in mode 0, 8-bit input or output, unless Port 8 is in mode 1.							

TABLE 4-11. PORT 1, MODE 1 INPUT STROBED

<u>PORT 1 ADDRESS:</u> X0,		<u>CONTROL REGISTER ADDRESS:</u> X3							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	1	1				
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A40 and A41. A terminator network must be installed at A42 and a driver network must be installed at A28. If mode 2 will not be used TTL termination networks can be used at A26 and A27.							
<u>DATA POLARITY AT J1:</u>		Negative true. Polarity of Port 3 control outputs depends on whether driver at A28 is inverting or non-inverting.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	53-55*	52-55	Enable input at 8226's.						
	75-77* and 64-73*	74-77	Connects Port 3, bit 3 to 55 INTRO.						
		58-69*	Connects STB _A / input (J1-26) to bit 4 of Port 3.						
	58-67*	58-73	Connects bit 5 of Port 3 (IBF _A) to J1-18.						
<u>PORT RESTRICTIONS - PORT 2:</u>		None; Port 2 can be in mode 0 or mode 1, input or output.							
<u>PORT 3:</u>		Port 3 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bits 0,1 and 2 - provide control for Port 2 if Port 2 is in mode 1 . Bit 3 - 55 INTRO (interrupt request output for Port 1) . Bit 4 - STB) (strobe) input for Port 1 . Bit 5 - IBF (input buffer full) output for Port 1 . Bits 6 and 7 - Can be used for input or output; both have same direction. 							

TABLE 4-12. PORT 4, MODE 1 INPUT STROBED

<u>PORT 4 ADDRESS:</u> X4,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	1	1				
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A45 and A46. A terminator network must be installed at A33 and a driver network must be installed at A47. If mode 2 will not be used, TTL terminator networks can be used at A31 and A32.							
<u>DATA POLARITY AT J2:</u>		Negative true. Polarity of Port 6 control outputs depends on whether driver at A47 is inverting or non-inverting.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	83-85*	82-85	Enable input at 8226's						
	78-80* and 94-103*	79-80	Connects Port 6, bit 3 to 55 INTR 2.						
		89-98*	Connects STB _A / input (J2-26) to bit 4 of Port 6.						
	88-97*	88-103	Connects bit 5 of Port 6 (IBF) to J2-18.						
<u>PORT RESTRICTIONS</u> - PORT 5:		None; Port 5 can be in mode 0 or mode 1, input or output.							
PORT 6:		Port 6 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bits 0, 1 and 2 - provide control for Port 5 if Port 5 is in mode 1. . Bit 3 - 55 INTR 2 (interrupt request) output for Port 4. . Bit 4 - STB/ (strobe) input for Port 5. . Bit 5 - IBF (input buffer full) output for Port 4. . Bits 6 and 7 - can be used for input or output; both have same direction. 							

TABLE 4-13. PORT 7, MODE 1 INPUT STROBED

PORT 1 ADDRESS: X8, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT: 7 6 5 4 3 2 1 0

1	0	1	1				
---	---	---	---	--	--	--	--

DRIVER/TERMINATION NETWORKS: Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A50 and A51. A terminator network must be installed at A52 and a driver network must be installed at A37. If mode 2 will not be used TTL termination networks can be used at A35 and A36.

DATA POLARITY AT J1: Negative true. Polarity of Port 3 control outputs depends on whether driver at A37 is inverting or non-inverting.

<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>
* = Default connection	109-111*	108-111	Enable input at 8226's.
	124-129* and 104-106*	105-106	Connects Port 3, bit 3 to 55 INTR 4.
		115-119*	Connects STB _A / input (J1-26) to bit 4 of Port A.
	114-118*	114-129	Connects bit 5 of Port A (IBF _A) to J1-18.

PORT RESTRICTIONS - PORT 8: None; Port 8 can be in mode 0 or mode 1, input or output.

PORT 9: Port 9 bits perform the following dedicated functions:

- . Bits 0,1 and 2 - provide control for Port 8 if Port 8 is in mode 1.
- . Bit 3 - INTR (interrupt request output for Port 7).
- . Bit 4 - STB/ (strobe) input for Port 7.
- . Bit 5 - IBF (input buffer full) output for Port 7.
- . Bits 6 and 7 - Can be used for input or output; both have same direction.

TABLE 4-14. PORT 1, MODE 1 LATCHED OUTPUT CONFIGURATION

<u>PORT 1 ADDRESS:</u> X0,		<u>CONTROL REGISTER ADDRESS:</u> X3							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	1	0				
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A40 and A41. A terminator network must be installed at A42 and a driver network must be installed at A28. If mode 2 will not be used, TTL driver networks can be used at A26 and A27.							
<u>DATA POLARITY AT J1:</u>		Negative true. The polarity of Port 3 control outputs depends on the type of driver installed at A28.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	53-55*	54-55	Enable output at 8226's						
	75-77* and 64-73*	74-77	Connects Port 3, bit 3 to 55 INTRO.						
		58-67*	Connects ACK _A / input (J1-30) to bit 6 of Port 3.						
	56-65*	56-73	Connects bit 7 of Port 3 (OBF _A /) to J1-18.						
<u>PORT RESTRICTIONS</u> - PORT 2:		None; Port 2 can be in mode 0 or mode 1, input or output.							
PORT 3:		Port 3 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bits 0, 1 and 2 - Dedicated to the control of Port 2 if Port 2 is in mode 1. . Bit 3 - 55 INTRO (interrupt request) output for Port 1. . Bits 4 and 5 - Can be used as input or output; both have same direction. . Bit 6 - ACK/ (acknowledge) input for Port 1. . Bit 7 - OBF/ (output buffer full) output for Port 1. 							

TABLE 4-15. PORT 4, MODE 1 LATCHED OUTPUT CONFIGURATION

<u>PORT 4 ADDRESS:</u> X4,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	1	0				
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers can be installed at A45 and A46. A terminator network must be installed at A33 and a driver network must be installed at A47. If mode 2 will not be used at A31 and A32.							
<u>DATA POLARITY AT J2:</u>		Negative true. The polarity of Port 6 control outputs depends on the type of driver installed at A47.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	83-85*	84-85	Enable outputs at 8226's						
	78-80* and 94-103*	79-80	Connects Port 6, bit 3 to 55 INTR 2.						
		87-96*	Connects ACK _A / input (J2-30) to bit 6 of Port 6.						
	86-95*	86-103	Connects bit 7 of Port 6 (OBF _A /) to J2-18.						
<u>PORT RESTRICTIONS</u> - PORT 5:		None; Port 5 can be in mode 0 or mode 1, input or output.							
PORT 6:		Port 6 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bits 0, 1 and 2 - Dedicated to the control of Port 5 if Port 5 is in mode 1. . Bit 3 - 55 INTR 2 (interrupt request) output for Port 4. . Bits 4 and 5 - Can be used as input or output; both have same direction. . Bit 6 - ACK/ (acknowledge) input for Port 4. . Bit 7 - OBF/(output buffer full) output for Port 4. 							

TABLE 4-16. PORT 7, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 1 ADDRESS: X8, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT: 7 6 5 4 3 2 1 0

1	0	1	0				
---	---	---	---	--	--	--	--

DRIVER/TERMINATION NETWORKS: Two Intel 8226/16 Bidirectional Bus drivers can be installed at A50 and A51. A terminator network must be installed at A52 and a driver network must be installed at A37. If mode 2 will not be used, TTL driver networks can be used at A35 and A36.

DATA POLARITY AT J1: Negative true. The polarity of Port 3 control outputs depends on the type of driver installed at A37.

<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>
* = Default connection	109-111*	110-111	Enable output at 8226's
	124-129* and 104-106*	105-103	Connects Port 3, bit 3 to 55 INTR 0.
		113-117*	Connects ACK _A / input (J1-30) to bit 6 of Port A.
	112-116*	112-129	Connects bit 7 of Port A (OBF _A /) to J1-18.

PORT RESTRICTIONS - PORT 9: None; Port 9 can be in mode 0 or mode 1, input or output.

PORT A: Port A bits perform the following dedicated functions:

- . Bits 0, 1 and 2 - Dedicated to the control of Port 9 if Port 9 is in mode 1.
- . Bit 3 - 55 INTRO (interrupt request) output for Port 8.
- . Bits 4 and 5 - Can be used as input or output; both have same direction.
- . Bit 6 - ACK/ (acknowledge) input for Port 8.
- . Bit 7 - OBF/ (output buffer full) output for Port 8.

TABLE 4-17. PORT 1, MODE 2 BIDIRECTIONAL CONFIGURATION

<u>PORT 1 ADDRESS:</u> X0,		<u>CONTROL REGISTER ADDRESS:</u> X3							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	1	X	X				
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers must be installed at A40 and A41. A terminator network must be installed at A42 and a driver network must be installed at A28.							
<u>DATA POLARITY AT J1:</u>		Negative true. The polarity of Port 3 control output depends on the type of driver installed at A28.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		53-55*	Allows ACK _A / input of Port 3 to control 8226 direction mode.						
	64-73* and 75-77*	74-77	Connects Port 3, bit 3 to 55 INTRO.						
		59-68*	Connects STB _A / input (J1-26) to bit 4 of Port 3.						
	58-67* and 61-70*	58-70	Connects bit 5 of Port 3 (IBF _A) to J1-24.						
		57-66*	Connects ACK _A / input (J1-30) to bit 6 of Port 3.						
	56-65*	56-73	Connects bit 7 of Port 3 (OBF _A /) to J1-18.						
<u>PORT RESTRICTIONS</u> - PORT 2:		None.							
PORT 3:		Port 3 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bit 0 - Cannot be used. . Bits 1 and 2 - Can both be used in either input or output if Port 2 is in mode 0. . Bit 3 - 55 INTRO (interrupt request) output for Port 1. . Bit 4 - STB/ (strobe) input for Port 1. . Bit 5 - IBF (input buffer full) output for port 1. . Bit 6 - ACK/ (acknowledge) input for Port 1. . Bit 7 - OBF/ (output buffer full) output for Port 1. 							

TABLE 4-18. PORT 4, MODE 2 BIDIRECTIONAL CONFIGURATION

PORT 4 ADDRESS: X4, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT: 7 6 5 4 3 2 1 0

1	1	X	X				
---	---	---	---	--	--	--	--

DRIVER/TERMINATION NETWORKS: Two Intel 8226/16 Bidirectional Bus Drivers must be installed at A45 and A46. A terminator network must be installed at A33 and a driver network must be installed at A47.

DATA POLARITY AT J2: Negative true. The polarity of Port 6 control outputs depends on the type of driver used at A47.

<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>
* = Default connection		83-85*	Allows ACK _A / output of Port 6 to control 8226 direction mode.
	94-103* and 78-80*	79-80	Connects Port 6, bit 3 to 55 INTR 2.
		89-98*	Connects STB _A / input (J2-26) to bit 4 of Port 6.
	88-97* and 91-100*	88-100	Connects bit 5 of Port 6 (IBF _A) to J2-24.
		87-96*	Connects ACK _A / input (J2-30) to bit 6 of Port 6.
	86-95*	86-103	Connects bit 7 of Port 6 (OBF _A /) to J2-18.

PORT RESTRICTIONS - PORT 5: None.

PORT 6: Port 6 performs the following dedicated functions:

- . Bit 0 - Can be used to control bits on Serial I/O Interface; cannot be used otherwise.
- . Bits 1 and 2 - Can both be used as either input or output if Port 5 is in mode 0.
- . Bit 3 - 55 INTR 2 (interrupt request) output for Port 4.
- . Bit 4 - STB/ (strobe) input for Port 4.
- . Bit 4 - IBF (input buffer full) output for Port 4.
- . Bit 6 - ACK/ (acknowledge) input for Port 4.
- . Bit 7 - OBF/ (output buffer full) output for Port 4.

TABLE 4-19. PORT 7, MODE 2 BIDIRECTIONAL CONFIGURATION

<u>PORT 7 ADDRESS:</u> X8,		<u>CONTROL REGISTER ADDRESS:</u> XB	
<u>CONTROL WORD FORMAT:</u>		7	6 5 4 3 2 1 0
<u>DRIVER/TERMINATION NETWORKS:</u>		Two Intel 8226/16 Bidirectional Bus Drivers must be installed at A50 and A51. A terminator network must be installed at A52 and a driver network must be installed at A37.	
<u>DATA POLARITY AT J3:</u>		Negative true. The polarity of Port 3 control output depends on the type of driver installed at A37.	
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>
* = Default connection		109-111*	Allows ACK _A / input of Port 3 to control 8226 direction mode.
	124-129* and 104-103*	105-106	Connects Port A, bit 3 to 55 INTR 4.
		115-119*	Connects STB _A / input (J1-26) to bit 4 of Port 3.
	114-118* and 121-126*	114-126	Connects bit 5 of Port A (IBF _A) to J1-24.
		113-117*	Connects ACK _A / input (J1-30) to bit 6 of Port A.
	112-116*	112-129	Connects bit 7 of Port A (OBF _A /) to J1-18.
<u>PORT RESTRICTIONS</u> - PORT 9: None.			
Port A: Port 3 bits perform the following dedicated functions:			
<ul style="list-style-type: none"> • Bit 0 - Cannot be used. • Bits 1 and 2 - Can both be used in either input or output if Port 9 is in mode 0. • Bit 3 - INTR (interrupt request) output for Port 8. • Bit 4 - STB/ (strobe) input for Port 8. • Bit 5 - IBF (input buffer full) output for Port 8. • Bit 6 - ACK/ (acknowledge) input for Port 8. • Bit 7 - OBF/ (output buffer full) output for Port 8. 			

4.4.2 PORTS 2,5 AND 8 (8255A PORT B)

Ports 2(5,8) can be programmed for input or output in either mode 0 or mode 1. If Port 2(5,8) is to be used for input, in either mode, terminator networks must be installed in the sockets at A43(34,53) and A29(48,38). If Port 2(5,8) is to be used for output, in either mode, driver networks must be installed in the sockets at A43(34,53) and A29(48,38). The four potential configurations for Port 2(5,8) are summarized in the following tables:

PORT 2(5) CONFIGURATIONS			TABLES		
<u>Mode</u>	<u>Direction</u>	<u>Group 1</u>	<u>Group 2</u>	<u>Group 3</u>	
1. Mode 0	Input	4-20	4-21	4-22	
2. Mode 0	Output (Latched)	4-23	4-24	4-25	
3. Mode 1	Input (Strobed)	4-26	4-27	4-28	
4. Mode 1	Output (Latched)	4-29	4-30	4-31	

TABLE 4-20. PORT 2, MODE 0 INPUT CONFIGURATION

<u>PORT 2 ADDRESS:</u> X1,		<u>CONTROL REGISTER ADDRESS:</u> X3							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1					0	1	
<u>DRIVER/TERMINATION NETWORKS:</u>		Termination networks must be installed at A43 and A29.							
<u>DATA POLARITY AT J1:</u>		Positive true							
<u>JUMPER ACTION:</u>		None, other than to connect the data path between Ports 2 and the termination networks at A43 and A29.							
<u>PORT RESTRICTIONS - PORT 1:</u>		None							
		PORT 2: None; Port 3 can be in mode 0, input or output unless Port 1 is in mode 1 or mode 2.							

TABLE 4-21. PORT 5, MODE 0 INPUT CONFIGURATION

<u>PORT 5 ADDRESS:</u> X5,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1					0	1	
<u>DRIVER/TERMINATION NETWORKS:</u>		Termination networks must be installed at A34 and A48.							
<u>DATA POLARITY AT J2:</u>		Positive true							
<u>JUMPER ACTION:</u>		None, other than to connect the data path between Port 5 and the termination networks at A34 and A48.							
<u>PORT RESTRICTIONS - PORT 4:</u>		None							
		PORT 6: None; Port 6 can be in mode 0, input or output unless Port 4 is in mode 1 or mode 2.							

TABLE 4-22. PORT 8, MODE 0 INPUT CONFIGURATION

<u>PORT 8 ADDRESS:</u> X9,		<u>CONTROL REGISTER ADDRESS:</u> XB							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
1						0	1		
<u>DRIVER/TERMINATION NETWORKS:</u>		Termination networks must be installed at A53 and A38.							
<u>DATA POLARITY AT J3:</u>		Positive true.							
<u>JUMPER ACTION:</u>		None, other than to connect the data path between Port 8 and the termination networks at A53 and A38.							
<u>PORT RESTRICTIONS - PORT 7:</u>		None							
		PORT 9: None; Port 9 can be in mode 0, input or output unless Port 7 is in mode 1 or mode 2.							

TABLE 4-23. PORT 2, MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 2 ADDRESS:</u> X1,	<u>CONTROL REGISTER ADDRESS:</u> X3								
<u>CONTROL WORD FORMAT:</u>	7 6 5 4 3 2 1 0								
	<table border="1"><tr><td>1</td><td></td><td></td><td></td><td></td><td>0</td><td>0</td><td></td></tr></table>	1					0	0	
1					0	0			
<u>DRIVER/TERMINATION NETWORKS:</u>	Driver networks must be installed at A43 and A29.								
<u>JUMPER ACTION:</u>	None, other than to connect the data path between Port 2 and the drivers at A43 and A29.								
<u>PORT RESTRICTIONS</u> - PORT 1:	None								
	Port 2: None, Port 3 can be in mode 0 input or output, unless Port 1 is in mode 1 or mode 2.								

TABLE 4-24. PORT 5, MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 5 ADDRESS:</u> X5,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1					0	0	
<u>DRIVER/TERMINATION NETWORKS:</u>		Driver networks must be installed at A34 and A48.							
<u>DATA POLARITY AT J2:</u>		Negative true, assuming inverting drivers are used at A34 and A48.							
<u>JUMPER ACTION:</u>		None, other than to connect the data path between Port 5 and the drivers at A34 and A48.							
<u>PORT RESTRICTIONS</u> - PORT 4:		None							
		PORT 6:		None; Port 6 can be in mode 0, input or output, unless Port 4 is in mode 1 or mode 2.					

TABLE 4-25. PORT 8, MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 8 ADDRESS:</u> X9,		<u>CONTROL REGISTER ADDRESS:</u> XB							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1					0	0	
<u>DRIVER/TERMINATION NETWORKS:</u>		Driver networks must be installed at A53 and A38.							
<u>JUMPER ACTION:</u>		None, other than to connect the data path between Port 8 and the drivers at A53 and A38.							
<u>PORT RESTRICTIONS - PORT 7:</u>		None							
		PORT 9: None, Port 9 can be in mode 0 input or output, unless Port 7 is in mode 1 or mode 2.							

TABLE 4-26. PORT 2, MODE 1 STROBED INPUT CONFIGURATION

<u>PORT 2 ADDRESS:</u> X1,		<u>CONTROL REGISTER ADDRESS:</u> X3							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1					1	1	
<u>DRIVER/TERMINATION NETWORKS:</u>		Terminator networks must be installed at A42, A43 and A29. A driver network must be installed at A28.							
<u>DATA POLARITY AT J1:</u>		Positive true. The polarity of Port 3 control outputs depends on the type of driver at A28.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	69-60* and 61-70	60-61	Connects Port 3, bit 0 to 55 INTR 1.						
		32-71*	Connects bit 1 of Port 3 (IBF _B) to J1-22.						
	63-72* and 56-65*	63-65	Connects STB _B / input (J1-32) to bit 2 of Port 3.						
<u>PORT RESTRICTIONS - PORT 1:</u>		None							
	<u>PORT 2:</u>	Port 3 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bit 0 - INTR (interrupt request) output for Port 2. . Bit 1 - IBF (input buffer full) output for Port 2. . Bit 2 - STB/ (strobe) input for Port 2. . Bit 3 - If Port 1 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved. . Bits 4 to 7 - Can be input or output if Port 1 is in mode 0 or in some mode combinations where Port 1 is in mode 1. These bits are always reserved when Port 1 is in mode 2. 							

TABLE 4-27. PORT 5, MODE 1 STROBED INPUT CONFIGURATION

<u>PORT 5 ADDRESS:</u> X5,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1					1	1	
<u>DRIVER/TERMINATION NETWORKS:</u>		Termination networks must be installed at A33, A34 and A48. A driver network must be installed at A47.							
<u>DATA POLARITY AT J2:</u>		Positive true. The polarity of Port 3 control outputs depends on the type of driver at A47.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	99-90* and 91-100*	91-90	Connects bit 0 of Port 6 to 55 INTR 3.						
		92-101*	Connects bit 1 of Port 6 (IBF _B) to J2-22.						
	93-102* and 86-95*	93-95	Connects STB _B / input (J2-32) to bit 2 of Port 6.						
<u>PORT RESTRICTIONS - PORT 4:</u>		None							
	<u>PORT 6:</u>	Port 6 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bit 0 - INTR (interrupt request) output for Port 5. . Bit 1 - IBF (input buffer full) output for Port 5. . Bit 2 - STB/ (strobe) input for Port 5. . Bit 3 - If Port 4 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved. . Bits 4 to 7 - Can be input or output if Port 4 is in mode 0 or in some mode combinations where Port 4 is in mode 1. These bits are always reserved when Port 4 is in mode 2. 							

TABLE 4-28. PORT 8, MODE 1 STROBED INPUT CONFIGURATION

<u>PORT 8 ADDRESS:</u> X9,		<u>CONTROL REGISTER ADDRESS:</u> XB							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1					1	1	
<u>DRIVER/TERMINATION NETWORKS:</u>		Terminator networks must be installed at A52, A53 and A38. A driver network must be installed at A37.							
<u>DATA POLARITY AT J3:</u>		Positive true. The polarity of Port 9 control outputs depends on the type of driver at A37.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	120-125* and 121-126*	121-120	Connects Port 9, bit 0 to 55 INTR 5.						
		122-127*	Connects bit 1 of Port 9 (IBF _B) to J3-22.						
	123-128* and 112-116*	123-116	Connects STB _B / input (J3-32) to bit 2 of Port 9.						
<u>PORT RESTRICTIONS - PORT 7:</u>		None							
<u>PORT 9:</u>		Port 9 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bit 0 - INTR (interrupt request) output for Port 8. . Bit 1 - IBF (input buffer full) output for Port 8. . Bit 2 - STB/ (strobe) input for Port 8. . Bit 3 - If Port 7 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved. . Bits 4 to 7 - Can be input or output if Port 7 is in mode 0 or in some mode combinations where Port 1 is in mode 1. These bits are always reserved when Port 7 is in mode 2. 							

TABLE 4-29. PORT 2, MODE 1 LATCHED OUTPUT CONFIGURATION

<u>PORT 2 ADDRESS:</u> X1,		<u>CONTROL REGISTER ADDRESS:</u> X3							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1					1	0	
<u>DRIVER/TERMINATION NETWORKS:</u>		Driver networks must be installed at A28, A43 and A29. A terminator network must be installed at A42.							
<u>DATA POLARITY AT J1:</u>		Negative true, assuming that inverting drivers are used at A28, A43 and A29.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	69-60* and 61-70*	60-61	Connects bit 0 of Port 3 to 55 INTR 1.						
		62-71*	Connects bit 1 of Port 3 (OBF _B) to J1-22.						
	63-72* and 55-55*	63-65	Connects ACK _B / input (J1-32) to bit 2 of Port 3						
<u>PORT RESTRICTIONS - PORT 1:</u>		None							
<u>PORT 2:</u>		Port 3 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bit 0 - INTR (interrupt request) input for Port 2. . Bit 1 - OBF/ (output buffer full) output for Port 2. . Bit 2 - ACK/ (acknowledge) input for Port 2. . Bit 3 - If Port 1 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved. . Bits 4 to 7 - Can be input or output if Port 1 is in mode 0 or in some combinations where Port 1 is in mode 1. These bits are always reserved when Port 1 is in mode 2. 							

TABLE 4-30. PORT 5, MODE 1 LATCHED OUTPUT CONFIGURATION

<u>PORT 5 ADDRESS:</u> X5,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1					1	0	
<u>DRIVER/TERMINATION NETWORKS:</u>		Driver networks must be installed at A47, A34 and A48. A terminator network must be installed at A33.							
<u>DATA POLARITY AT J2:</u>		Negative true, assuming that inverting drivers are used at A47, A34 and A48.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection	90-99* and 91-100*	91-90	Connects bit 0 of Port 6 to 55 INTR 3.						
		92-101*	Connects bit 1 of Port 6 (OBF _B) to J2-22.						
	93-102* and 86-85*	93-95	Connects ACK _B / input (J2-32) to bit 2 of Port 6.						
<u>PORT RESTRICTIONS</u> - PORT 4:		None							
PORT 6:		Port 6 bits perform the following dedicated functions:							
		<ul style="list-style-type: none"> . Bit 0 - INTR (interrupt request) output for Port 5. . Bit 1 - OBF/ (output buffer full) output for Port 5. . Bit 2 - ACK/ (acknowledge) input for Port 5. . Bit 3 - If Port 4 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved. . Bits 4 to 7 - Can be input or output if Port 4 is in mode 0 or in some combinations where Port 4 is in mode 1. These bits are always reserved when Port 4 is in mode 2. 							

TABLE 4-31. PORT 8, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 8 ADDRESS: X9, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT: 7 6 5 4 3 2 1 0

1						1	0	
---	--	--	--	--	--	---	---	--

DRIVER/TERMINATION NETWORKS: Driver networks must be installed at A37, A53 and A38. A terminator network must be installed at A52.

DATA POLARITY AT J3: Negative true, assuming that inverting drivers are used at A37, A53 and A38.

<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>
* = Default connection	120-125* and 121-126*	120-121	Connects bit 0 of Port 9 to 55 INTR 5.
		122-127*	Connects bit 1 of Port 9 (OBF _B) to J3-22.
	112-116* and 123-128*	116-123	Connects ACK _B / input (J3-32) to bit 2 of Port 9.

PORT RESTRICTIONS - PORT 7: None

- PORT 9: Port 9 bits perform the following dedicated functions:
- . Bit 0 - INTR (interrupt request input for Port 8).
 - . Bit 1 - OBF/ (output buffer full) output for Port 8.
 - . Bit 2 - ACK/ (acknowledge) input for Port 8.
 - . Bit 3 - If Port 7 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved.
 - . Bits 4 to 7 - Can be input or output if Port 7 is in mode 0 or in some combinations where Port 7 is in mode 1. These bits are always reserved when Port 7 is in mode 2.

4.4.3 PORTS 3, 6 AND 9 (8255A PORT C)

The use of Port 3(6,9) depends on the modes programmed for Ports 1(4,7) and 2(5,8). It can be implemented as an 8-bit input or output data path or as two 4-bit I/O paths only if both Port 1(4,7) and Port 2(5,8) are programmed for mode 0. If Port 1(4,7) is in either mode 1 or mode 2 or if Port 2(5,8) is in mode 1, various individual Port 3(6,9) bits are available while the other Port 3(6,9) bits are either dedicated to control functions or are unavailable for any purpose.

Tables 4-32 through 4-43 specify the use of Port 3(6,9) bits as separate pairs of 4-bit I/O ports. As such, the two halves of Port 3(6,9) can both operate as input or output ports or they can have separate direction characteristics. The two halves are referred to as lower (bits 0 to 3) and upper (bits 4 to 7).

When Port 1(4,7) is in mode 1, it uses bit 3 of Port 3(6,9) and two upper bits of Port 3(6,9) for control functions. When Port 1(4,7) is in mode 2, it uses bit 3 of Port 3(6,9) and all four upper bits of Port 3(6,9) for control functions. Similarly, when Port 2(5,8) is in mode 1, it uses bit 0 of Port 3(6,9) and two lower bits from Port 3(6,9) for control.

Table 4-44 summarizes the use of Port 3 bits for control by Ports 1 and 2. Tables 4-45 and 4-46 serve the same purpose for Ports 6 and 9. These tables can be used as final check lists to verify the correct wiring of Port 3, Port 6 and Port 9 control bits.

TABLE 4-32. PORT 3 (LOWER) MODE 0 INPUT CONFIGURATION

<u>PORT 3 ADDRESS:</u> X2,		<u>CONTROL REGISTER ADDRESS:</u> X3							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0			0		1
<u>DRIVER/TERMINATION NETWORKS:</u>		A termination network must be installed at A28.							
<u>DATA POLARITY AT J1:</u>		Positive true.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		61-70*	Connects bit 0 to J1-24.						
		62-71*	Connects bit 1 to J1-22.						
		63-72*	Connects bit 2 to J1-20.						
		64-73*	Connects bit 3 to J1-18.						
<u>PORT RESTRICTIONS</u> - PORT 1:		Port 1 must be in mode 0 for all four bits to be available.							
	PORT 2:	Port 2 must be in mode 0 for all four bits to be available.							

TABLE 4-33. PORT 6 (LOWER) MODE 0 INPUT CONFIGURATION

<u>PORT 6 ADDRESS:</u> X6,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0			0		1
<u>DRIVER/TERMINATION NETWORKS:</u>		A termination network must be installed at A47.							
<u>DATA POLARITY AT J2:</u>		Positive true.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		91-100*	Connects bit 0 to J2-24.						
		92-101*	Connects bit 1 to J2-22.						
		93-102*	Connects bit 2 to J2-20.						
		94-103*	Connects bit 3 to J2-18.						
<u>PORT RESTRICTION</u> - PORT 4:		Port 4 must be in mode 0 for all four bits to be available.							
	PORT 5:	Port 5 must be in mode 0 for all four bits to be available.							

TABLE 4-34. PORT 9 (LOWER) MODE 0 INPUT CONFIGURATION

<u>PORT 9 ADDRESS:</u> XA,		<u>CONTROL REGISTER ADDRESS:</u> XB						
<u>CONTROL WORD FORMAT:</u>	7	6	5	4	3	2	1	0
	1	0	0			0		1
<u>DRIVER/TERMINATION NETWORKS:</u>		A termination network must be installed at A37.						
<u>DATA POLARITY AT J3:</u>		Positive true.						
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>					
* = Default connection		121-126*	Connects bit 0 to J3-24.					
		122-127*	Connects bit 1 to J3-22.					
		123-128*	Connects bit 2 to J3-20.					
		124-129*	Connects bit 3 to J3-18.					
<u>PORT RESTRICTIONS</u> - PORT 7:		Port 7 must be in mode 0 for all four bits to be available.						
	PORT 9:	Port 9 must be in mode 0 for all four bits to be available.						

TABLE 4-35. PORT 3 (UPPER) MODE 0 INPUT CONFIGURATION

<u>PORT 3 ADDRESS:</u> X2,		<u>CONTROL REGISTER ADDRESS:</u> X3							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0		1	0		
<u>DRIVER/TERMINATION NETWORKS:</u>		A termination network must be installed at A42.							
<u>DATA POLARITY AT J1:</u>		Positive true.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default		59-68*	Connects bit 4 to J1-26.						
		58-67*	Connects bit 5 to J-28.						
		57-66*	Connects bit 5 to J-30.						
		56-65*	Connects bit 7 to J1-32.						
<u>PORT RESTRICTIONS - PORT 1:</u>		Port 1 must be in mode 0 for all four bits to be available.							
	<u>PORT 2:</u>	Port 2 must be in mode 0 for all four bits to be available.							

TABLE 4-36. PORT 6 (UPPER) MODE 0 INPUT CONFIGURATION

<u>PORT 6 ADDRESS:</u> X6,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0		1	0		
<u>DRIVER/TERMINATION NETWORKS:</u>		A termination network must be installed at A33.							
<u>DATA POLARITY AT J2:</u>		Positive true							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		115-119*	Connects bit 4 to J2-26.						
		114-118*	Connects bit 5 to J2-28.						
		113-117*	Connects bit 6 to J2-30.						
		112-116*	Connects bit 7 to J2-32.						
<u>PORT RESTRICTION - PORT 4:</u>		Port 4 must be in mode 0 for all four bits to be available.							
	<u>PORT 5:</u>	Port 5 must be in mode 0 for all four bits to be available.							

TABLE 4-37. PORT 9 (UPPER) MODE 0 INPUT CONFIGURATION

<u>PORT 9 ADDRESS:</u> XA,		<u>CONTROL REGISTER ADDRESS:</u> XB							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0		1	0		
<u>DRIVER/TERMINATION NETWORKS:</u>		A termination network must be installed at A52.							
<u>DATA POLARITY AT J3:</u>		Positive true.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		89-98*	Connects bit 4 to J3-26.						
		88-97*	Connects bit 5 to J3-28.						
		87-96*	Connects bit 5 to J3-30.						
		86-95*	Connects bit 7 to J3-32.						
<u>PORT RESTRICTIONS - PORT 7:</u>		Port 7 must be in mode 0 for all four bits to be available.							
	<u>PORT 8:</u>	Port 8 must be in mode 0 for all four bits to be available.							

TABLE 4-38. PORT 3 (LOWER) MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 3 ADDRESS:</u> X2,		<u>CONTROL REGISTER ADDRESS:</u> X3							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0			0		0
<u>DRIVER/TERMINATION NETWORKS:</u>		A driver network must be installed at A28.							
<u>DATA POLARITY AT J1:</u>		Negative true, assuming inverting drivers are used at A28.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		61-70*	Connects bit 0 to J1-24.						
		62-71*	Connects bit 1 to J1-22.						
		63-72*	Connects bit 2 to J1-20.						
		64-73*	Connects bit 3 to J1-18.						
<u>PORT RESTRICTIONS</u> - PORT 1:		Port 1 must be in mode 0 for all four bits to be available.							
	PORT 2:	PORT 2 must be in mode 0 for all four bits to be available.							

TABLE 4-39. PORT 6 (LOWER) MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 6 ADDRESS:</u> X6,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0			0		0
<u>DRIVER/TERMINATION NETWORKS:</u>		A driver network must be installed at A47.							
<u>DATA POLARITY AT J2:</u>		Negative true, assuming inverting drivers are used at A47.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		91-100*	Connects bit 0 to J2-24.						
		92-101*	Connects bit 1 to J2-22.						
		93-102*	Connects bit 2 to J2-20.						
		94-103*	Connects bit 3 to J2-18.						
<u>PORT RESTRICTIONS - PORT 4:</u>		Port 4 must be in mode 0 for all four bits to be available.							
	<u>PORT 5:</u>	Port 5 must be in mode 0 for all four bits to be available.							

TABLE 4-40. PORT 9 (LOWER) MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 9 ADDRESS:</u> XA,		<u>CONTROL REGISTER ADDRESS:</u> XB							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0			0		0
<u>DRIVER/TERMINATION NETWORKS:</u>		A driver network must be installed at A37.							
<u>DATA POLARITY AT J1:</u>		Negative true, assuming inverting drivers are used at A37.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		121-126*	Connects bit 0 to J3-24.						
		122-127*	Connects bit 1 to J3-22.						
		123-128*	Connects bit 2 to J3-20.						
		124-129*	Connects bit 3 to J3-18.						
<u>PORT RESTRICTION</u> - PORT 7:		Port 7 must be in mode 0 for all four bits to be available.							
	PORT 8:	Port 8 must be in mode 0 for all four bits to be available.							

TABLE 4-41. PORT 3 (UPPER) MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 3 ADDRESS:</u> X2,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0		0	0		
<u>DRIVER/TERMINATION NETWORKS:</u>		A driver network must be installed at A42.							
<u>DATA POLARITY AT J1:</u>		Negative true, assuming inverting drivers are used at A42.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		59-68*	Connects bit 4 to J1-26.						
		58-67*	Connects bit 5 to J1-28.						
		57-66*	Connects bit 6 to J1-30.						
		56-65*	Connects bit 7 to J1-32.						
<u>PORT RESTRICTIONS</u> - PORT 1:		Port 1 must be in mode 0 for all four bits to be available.							
	PORT 2:	Port 2 must be in mode 0 for all four bits to be available.							

TABLE 4-42. PORT 6 (UPPER) MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 6 ADDRESS:</u> X6,		<u>CONTROL REGISTER ADDRESS:</u> X7							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0		0	0		
<u>DRIVER/TERMINATION NETWORKS:</u>		A driver network must be installed at A33.							
<u>DATA POLARITY AT J2:</u>		Negative true, assuming inverting drivers are used at A33.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		89-98*	Connects bit 4 to J2-26.						
		88-97*	Connects bit 5 to J2-28.						
		87-96*	Connects bit 6 to J2-30.						
		86-95*	Connects bit 7 to J2-32.						
<u>PORT RESTRICTIONS</u> - PORT 4:		Port 4 must be in mode 0 for all four bits to be available.							
	PORT 5:	Port 5 must be in mode 0 for all four bits to be available.							

TABLE 4-43. PORT 9 (UPPER) MODE 0 LATCHED OUTPUT CONFIGURATION

<u>PORT 9 ADDRESS:</u> XA,		<u>CONTROL REGISTER ADDRESS:</u> XB							
<u>CONTROL WORD FORMAT:</u>		7	6	5	4	3	2	1	0
		1	0	0		0	0		
<u>DRIVER/TERMINATION NETWORKS:</u>		A driver network must be installed at A52.							
<u>DATA POLARITY AT J3:</u>		Negative true, assuming inverting drivers are used at A52.							
<u>JUMPER ACTION:</u>	<u>DELETE</u>	<u>ADD</u>	<u>EFFECT</u>						
* = Default connection		115-119*	Connects bit 4 to J3-26.						
		114-118*	Connects bit 5 to J3-28.						
		113-117*	Connects bit 6 to J3-30.						
		112-116*	Connects bit 7 to J3-32.						
<u>PORT RESTRICTIONS</u> - PORT 7:		Port 7 must be in mode 0 for all four bits to be available.							
	PORT 8:	Port 8 must be in mode 0 for all four bits to be available.							

TABLE 4-44. PORT 3 RESTRICTION SUMMARY
(PORT 1/PORT 2 CONTROL FUNCTIONS)

<u>PORT 3 BIT #</u>	<u>PORT 1 MODE</u>	<u>PORT 2 MODE</u>	<u>FUNCTION</u>	<u>JUMPER ACTION</u>
0	-	1-I/O	Provides INTR _B to 55 INTR 1	Delete 60-69* Delete 61-70* Add 60-61
0	2-B	0-I/O	Cannot be used; no drivers/terminators available	Delete 61-70*
1	-	1-I	Provides IBF _B output to J1-22	Add 62-71*
1	-	1-0	Provides OBF _B output to J1-22	Add 62-71*
2	-	1-I	Provides STB _B input from J1-32	Delete 63-72* Delete 56-65* Add 63-65
2	-	1-0	Provides ACK _B / input from J1-32	Delete 63-72* Delete 56-65* Add 63-65
3	1-I/O	-	Provides INTR _A to 55 INTRO	Delete 64-73* Delete 75-77* Add 74-77
3	2-B	-	Provides INTR _A to 55 INTRO	Delete 64-73* Delete 75-77* Add 74-77
4	1-I	-	Provides STB _A / input from J1-26	Add 59-68*
4	2-B	-	Provides STB _A / input from J1-26	Add 59-68*
5	1-I	--	Provides IBF _A / output to J1-18	Delete 64-73* Delete 58-67* Add 58-73
5	2-B	-	Provides IBF _A output to J1-24	Delete 61-70* Delete 58-67* Add 58-70
6	1-0	-	Provides ACK _A / input from J1-30	Add 57-66*

(Table continued on next page)

TABLE 4-44. PORT 3 RESTRICTION SUMMARY
(Continued)

<u>PORT 3 BIT #</u>	<u>PORT 1 MODE</u>	<u>PORT 2 MODE</u>	<u>FUNCTION</u>	<u>JUMPER ACTION</u>
6	2-B	-	Provides ACK _A / input from J1-30	Add 57-66*
7	0-I/O	1-I/O	Cannot be used: no drivers/ter- minators available	Delete 56-65*
7	1-0	-	Provides OBF _A output to J1-18	Delete 56-65* Delete 64-73* Add 56-73

NOTE 1: If a Port 3 pin is not shown in this table as having a prescribed function for certain Port 1/Port 2 modes and if a spare driver or termination network is available, that pin can be used as an input or output, as determined by the driver/terminator availability.

NOTE 2: I = Input
O = Output
I/O = Input or Output
B = Bidirectional
*Denotes default connection

TABLE 4-45. PORT 6 RESTRICTION SUMMARY
(PORT 4/PORT 5 CONTROL FUNCTIONS)

<u>PORT 6 BIT #</u>	<u>PORT 4 MODE</u>	<u>PORT 5 MODE</u>	<u>FUNCTION</u>	<u>JUMPER ACTION</u>
0	-	1-I/O	Provides INTR _B to 55 INTR 3	Delete 91-100* Delete 90-99* Add 90-91
0	2-B	0-I/O	Cannot be used; no drivers/terminators available	Delete 91-100*
1	-	1-I	Provides IBF _B output to J2-22	Add 92-101*
1	-	1-0	Provides OBF _B output to J2-22	Add 92-101*
2	-	1-I	Provides STB _B input from J2-32	Delete 93-102* Delete 86-95* Add 93-95
2	-	1-0	Provides ACK _B / input from J2-32	Delete 93-102* Delete 86-95* Add 93-95
3	1-I/O	-	Provides INTR _A to 55 INTR 2	Delete 94-103* Delete 78-80* Add 79-80
3	2-B	-	Provides INTR _A to 55 INTR 2	Delete 94-103* Delete 78-80* Add 79-80
4	1-I	-	Provides STB _A / input from J2-26	Add 89-98*
4	2-B	-	Provides STB _A / input from J2-26	Add 89-98*
5	1-I	-	Provides IBF _A output to J2-18	Delete 94-103* and 88-97* Add 88-103
5	2-B	-	Provides IBF _A output to J2-24	Delete 91-100* and 88-97* Add 88-100

(Table continued on next page)

TABLE 4-45. PORT 6 RESTRICTION SUMMARY
(Continued)

<u>PORT 6 BIT #</u>	<u>PORT 4 MODE</u>	<u>PORT 5 MODE</u>	<u>FUNCTION</u>	<u>JUMPER ACTION</u>
6	1-0	-	Provides ACK _A / input from J2-30	Add 87-93*
6	2-B	-	Provides ACK _A / input from J2-30	Add 87-96*
7	0-I/O	1-I/O	Cannot be used; no drivers/ter- minators available	Delete 86-95*
7	1-0	-	Provides OBF _A output to J2-18	Delete 86-95* and 94-103* Add 85-103

NOTE 1: If a Port 6 pin is not shown in this table as having a prescribed function for certain Port 4/Port 5 modes and if a spare driver or termination network is available, that pin can be used as an input or output, as determined by the driver/terminator availability.

NOTE 2: I = Input
O = Output
I/O = Input or Output
B = Bidirectional
*Denotes default connection.

TABLE 4-46. PORT 9 RESTRICTION SUMMARY
(PORT 1/PORT 2 CONTROL FUNCTIONS)

<u>PORT 9 BIT #</u>	<u>PORT 7 MODE</u>	<u>PORT 8 MODE</u>	<u>FUNCTION</u>	<u>JUMPER ACTION</u>
0	-	1-I/O	Provides INTR _B to 55 INTR 5	Delete 120-125* Delete 121-126* Add 120-121
0	2-B	0-I/O	Cannot be used; no drivers/terminators available	Delete 121-126*
1	-	1-I	Provides IBF _B output to J3-22	Add 122-127*
1	-	1-0	Provides OBF _B output to J3-22	Add 122-127*
2	-	1-I	Provides STB _B input from J3-32	Delete 123-128* Delete 112-116* Add 123-116
2	-	1-0	Provides ACK _B / input from J3-32	Delete 123-128* Delete 112-116* Add 123-116
3	1-I/O	-	Provides INTR _A to 55 INTR 4	Delete 124-129* Delete 104-106* Add 105-106
3	2-B	-	Provides INTR _A to 55 INTR 4	Delete 124-129* Delete 104-106* Add 105-106
4	1-I	-	Provides STB _A / input from J3-26	Add 115-119*
4	2-B	-	Provides STB _A / input from J3-26	Add 115-119*
5	1-I	-	Provides IBF _A / output to J3-18	Delete 124-129* Delete 114-118* Add 114-129
5	2-B	-	Provides IBF _A output to J3-24	Delete 121-126* Delete 114-118* Add 114-126
6	1-0	-	Provides ACK _A / input from J3-30	Add 113-117*

(Table Continued on Next Page)

TABLE 4-46. PORT 9 RESTRICTION SUMMARY
(Continued)

<u>PORT 9 BIT #</u>	<u>PORT 7 MODE</u>	<u>PORT 8 MODE</u>	<u>FUNCTION</u>	<u>JUMPER ACTION</u>
6	2-B	-	Provides ACK _A / input from J3-30	Add 113-117*
7	0-I/O	1-I/O	Cannot be used; no drivers/ter- minators available	Delete 112-116*
7	1-0	-	Provides OBF _A output to J3-18	Delete 124-129* Delete 112-116* Add 112-129

NOTE 1: If a Port 9 pin is not shown in this table as having a prescribed function for certain Port 7/Port 8 modes and if a spare driver or termination network is available, that pin can be used as an input or output, as determined by the driver/terminator availability.

NOTE 2: I = Input
O = Output
I/O = Input or Output
B = Bidirectional
*Denotes default connection

4.5 INTERRUPT PRIORITY OPTIONS

There are two major considerations in configuring a custom interrupt structure on the SBC-519:

- 1) The connection of external and on-board interrupt requests to the eight interrupt priority level inputs (IR0-IR7) on the 8259,
- 2) The selection of a priority resolution algorithm.

The priority resolution algorithm is selected by programming the 8259 as described in Section 3.3 . The selection of interrupt sources for use as interrupt request inputs is made by connecting the appropriate jumper pins as summarized in Table 4-47.

TABLE 4-47. INTERRUPT SOURCE SELECTION

CONNECT JUMPER PINS:	INTERRUPT REQ. LEVEL (IR-)								INTERRUPT SOURCE
	0	1	2	3	4	5	6	7	
49-50	X								RTI/
74-77		X							INTR PORT X0
No Action Required			X						EXT INTRO/
61-60			X						INTR PORT X1
79-80				X					INTR PORT X4
81-80					X				EXT INTR 1/
91-90					X				INTR PORT X5
105-106						X			INTR PORT X8
107-106							X		EXT INTR 2 /
121-120							X		INTR PORT X9
No Action Required								X	EXT INTR 0/

CHAPTER 5

SYSTEM INTERFACING

This chapter identifies each of the SBC-519's external connections and defines all signals on the external system bus.

5.1 ELECTRICAL CONNECTIONS

The SBC-519 electronics are mounted on a 12.00 × 6.75 inch printed circuit board that requires maximum average DC current at the following levels:

$$\begin{array}{ccc} \triangle 1 & & \triangle 2 \\ V_{CC} = +5V \pm 5\% & I_{CC} = 3.5A & I_{CC} = 1.5A \end{array}$$

- NOTES: $\triangle 1$ The values assume that optional 220/330 Ω termination networks being driven low have been installed in the Parallel I/O Interface.
- $\triangle 2$ These values assume that the optional termination networks are not present.

The SBC-519 has five edge connectors, as shown in Figure 5-1. Edge connectors at the top of the module are designed for compatibility with both flat cable and round cable hardware. All parallel I/O functions are paired with an independent signal ground pin (odd pins are ground). This allows flat cable implementation to utilize an alternate signal/ground scheme for reduction of cross talk. Round cables may easily be implemented as twisted pair with an individual ground pin for every return wire.

The Parallel I/O Interface communicates with external I/O devices via three 50-pin double-sided PC edge connectors (J1, J2 and J3), 0.1 inch centers. External devices can be attached to J1, J2 or J3 using any of the following connectors.

NOTE: All pin numbers listed in the following tables refer to numbers printed on the board, not to mating connector pin positions. When specifying pin numbers for cable harnesses, use caution since SBC-519 pin numbering is not necessarily the same as the connector pin number scheme.

TABLE 5-1. SBC BOARDS COMPATIBLE CONNECTOR HARDWARE

FUNCTION	# OF PINS	CENTERS (inches)	CONNECTOR TYPE	VENDOR	VENDOR PART #	INTEL PART #
PARALLEL I/O	25/50	0.1	FLAT CRIMP ↓	3M 3M AMP ANSLEY SAE	3415-0000 WITH EARS 3415-0001 W/O EARS 88083-1 609-5015 SD6750 SERIES	SBC-955 (CABLE ASSY.)
SERIAL I/O	13/26	0.1	FLAT CRIMP ↓	3M AMP ANSLEY SAE	3462-0001 CRIMP 88106-1 609-2615 SD6726 SERIES	SBC-956 (CABLE ASSY.)
PARALLEL I/O	25/50	0.1	SOLDERED ↓	AMP VIKING TI	2-583485-6 3VH25/1JV5 H312125	N/A
SERIAL I/O	13/26	0.1	SOLDERED ↓	TI AMP	H312113 1-583485-5	N/A
AUXILIARY ▽	30/60	0.1	SOLDERED ↓	VIKING TI	3VH30/1JN5 H312130	N/A
BUS ▽	43/86	0.156	SOLDERED ↓	CDC MICRO PLASTICS ARCO VIKING	VPB01E43D00A1 ▽ MP-0156-43-BW-4 AE443WP1 LESS EARS 2VH43/1AV5	N/A
PARALLEL I/O ▽	25/50	0.1	WIREWRAP ↓	TI VIKING CDC ITT CANNON	H311125 3VH25/1JND5 VPB01B25D00A1 ▽ EC4A050A1A	N/A
SERIAL I/O ▽	13/26	0.1	WIREWRAP	TI	H311113	N/A
AUXILIARY ▽	30/60	0.1	WIREWRAP ↓	CDC TI	VPB01B30A00A2 ▽ H311130	MDS-980
BUS ▽	43/86	0.156	WIREWRAP ↓	CDC CDC VIKING	VFB01E43D00A1 or ▽ VPB01E43A00A1 2VH43/1AND5	MDS-985
SBC 201 SBC 501 SBC 508 SBC 905, etc.	50/100	0.1	SOLDER TAIL	VIKING	3VH50/1JN5	MDS-990
			SOLDER PAK (RAYCHEM)	CDC	VPB04B50E00A1E ▽	N/A

▽ Connector heights are not guaranteed to conform to OEM packaging equipment. Intel OEM and Inteltec® Development System motherboards offer complete mechanical compatibility.

▽ Wirewrap pin lengths are not guaranteed to conform to OEM packaging equipment. Intel connectors and OEM and Inteltec® Development System motherboards offer complete mechanical compatibility.

▽ CDC VPB01 ..., VPB02 ..., VPB04 ..., etc. are identical connectors with different electroplating thicknesses or metal surfaces.

NOTE: See next page for vendor addresses, telephone numbers and TWX numbers.

VENDORS ADDRESSES

The following information is for our customers' convenience only. Intel does not represent these vendors, guarantee availability nor continued quality of their products.

CDC CONNECTOR DIVISION
31829 W. LaTienda Drive
Westlake Village, CA 91361
213-889-3535
TWX 910-494-1224

T & B/ANSLEY
Subsidiary of Thomas & Betts Corporation
3208 Humbolt Street
Los Angeles, CA 90031
213-223-2331
TWX 910-321-3938

VIKING INDUSTRIES, INC.
21001 Nordhoff Street
Chatsworth, CA 91311
213-341-4330
TWX 910-494-2094

STANFORD APPLIED ENGINEERING, INC. (SAE)
340 Martin Avenue
Santa Clara, CA 95050
408-243-9200
TWX 910-338-0132

Connector Systems
TEXAS INSTRUMENTS, INC.
34 Forest Street
Attleboro, MA 02703
617-222-2800

3M Connectors
Electronic Products Division, Bldg. 223-4E
3M COMPANY
3M Center
St. Paul, MN 55101
612-733-1110

AMP Incorporated
P.O. Box 3608
Harrisburg, PA 17105
717-564-0100
TWX 510-657-4110

ITT CANNON ELECTRIC
666 East Dyer Road
Santa Ana, CA 92702
800-854-3573
800-432-7063 (in California)

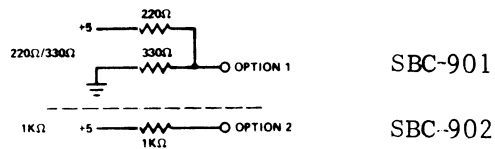
Tables 5-2, 5-3 and 5-4 provide pin lists for the J1, J2 and J3 connectors, respectively. The following TTL line drivers and Intel terminators are all compatible with the I/O driver sockets in the Parallel I/O Interface:

Driver	Characteristic	Sink Current (ma)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note: I = inverting; N.I. = non-inverting
OC = open collector

I/O Terminators:

TTL Terminators: 220Ω/330Ω divider or 1 kΩ pull up



See Appendix B for schematics

The bidirectional driver circuit consists of a bidirectional driver and a termination network. The bidirectional drivers compatible with this product are Intel's 8216 (non-inverting) and 8226 (inverting). The termination network is a 14-pin resistor pack made by many different vendors. The following list is some of the vendors and part numbers which are compatible with this product.

<u>Company</u>	<u>Series</u>
CTS	760-1
DALE	LDPI4-02
BECKMAN	899-1
SPRAGUE	914C-PE

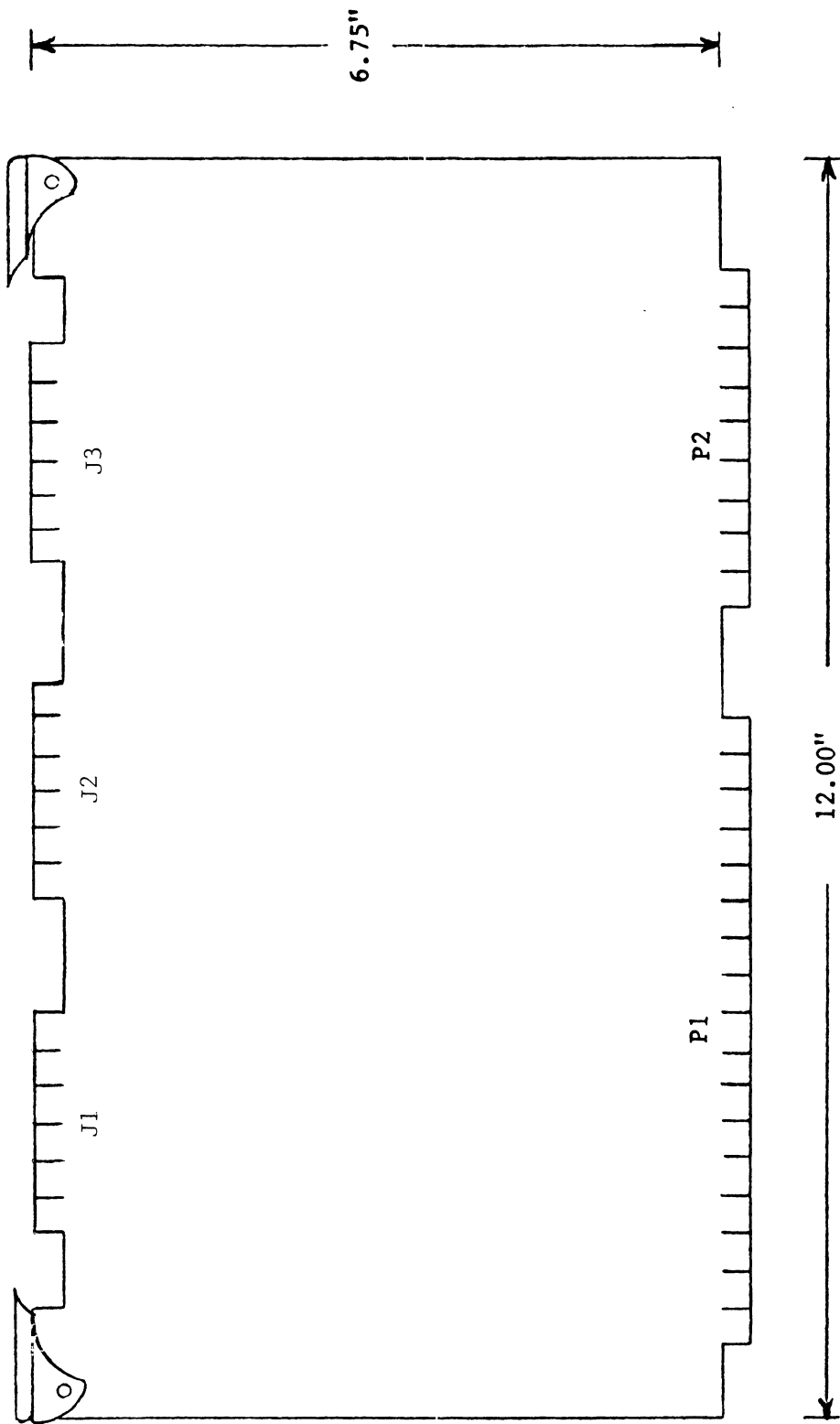




FIGURE 5-1. SBC-519 EDGE CONNECTORS

TABLE 5-2. PIN ASSIGNMENTS FOR CONNECTOR J1
(Parallel I/O Interface - Group 1)

PIN *	SIGNAL	PIN *	SIGNAL
1		2	PORT 2 - BIT 7
3		4	PORT 2 - BIT 6
5		6	PORT 2 - BIT 5
7		8	PORT 2 - BIT 4
9		10	PORT 2 - BIT 3
11		12	PORT 2 - BIT 2
13		14	PORT 2 - BIT 1
15		16	PORT 2 - BIT 0
17		18	PORT 3 - BIT 3
19		20	PORT 3 - BIT 2
21		22	PORT 3 - BIT 1
23		24	PORT 3 - BIT 0
25		26	PORT 3 - BIT 4
27		28	PORT 3 - BIT 5
29		30	PORT 3 - BIT 6
31		32	PORT 3 - BIT 7
33		34	PORT 1 - BIT 7
35		36	PORT 1 - BIT 6
37		38	PORT 1 - BIT 5
39		40	PORT 1 - BIT 4
41		42	PORT 1 - BIT 3
43		44	PORT 1 - BIT 2
45		46	PORT 1 - BIT 1
47		48	PORT 1 - BIT 0
49		50	EXT INTR 1/

* Pin Numbers refer to board connector pins only, they are not necessarily the same on the mating connector.


TABLE 5-3. PIN ASSIGNMENTS FOR CONNECTOR J2
(Parallel I/O Interface - Group 2)

PIN*	SIGNAL	PIN*	SIGNAL
1		2	PORT 5 - BIT 7
3		4	PORT 5 - BIT 6
5		6	PORT 5 - BIT 5
7		8	PORT 5 - BIT 4
9		10	PORT 5 - BIT 3
11		12	PORT 5 - BIT 2
13		14	PORT 5 - BIT 1
15		16	PORT 5 - BIT 0
17		18	PORT 5 - BIT 3
19		20	PORT 6 - BIT 2
21		22	PORT 6 - BIT 1
23		24	PORT 6 - BIT 0
25		26	PORT 6 - BIT 4
27		28	PORT 6 - BIT 5
29		30	PORT 6 - BIT 6
31		32	PORT 6 - BIT 7
33		34	PORT 6 - BIT 7
35		36	PORT 4 - BIT 6
37		38	PORT 4 - BIT 5
39		40	PORT 4 - BIT 4
41		42	PORT 4 - BIT 3
43		44	PORT 4 - BIT 2
45		46	PORT 4 - BIT 1
47		48	PORT 4 - BIT 0
49		50	EXT INTR 1/

* Pin numbers refer to board connector pins only, they are not necessarily the same on the mating connector.

The SBC-519 connects to the system bus via an 86-pin double-sided edge connector (P1), 0.156 inch centers. This edge connector will accept any of the following mating connectors: CDC VPB01E43A000A1, Micro Plastics MP-0156-43-BW-4 or ARCO AE 443WP1. Section 5.2 defines each of the external system bus signals and includes a pin list for P1 (Table 5-5).

TABLE 5-4. PIN ASSIGNMENTS FOR CONNECTOR J3
(Parallel I/O Interface - Group 3)

PIN*	SIGNAL	PIN*	SIGNAL	
1	 GND	2	PORT 8 - BIT 7	
3		4	PORT 8 - BIT 6	
5		6	PORT 8 - BIT 5	
7		8	PORT 8 - BIT 4	
9		10	PORT 8 - BIT 3	
11		12	PORT 8 - BIT 2	
13		14	PORT 8 - BIT 1	
15		16	PORT 8 - BIT 0	
17		18	PORT 9 - BIT 3	
19		20	PORT 9 - BIT 1	
21		22	PORT 9 - BIT 1	
23		24	PORT 9 - BIT 0	
25		26	PORT 9 - BIT 4	
27		28	PORT 9 - BIT 5	
29		30	PORT 9 - BIT 6	
31		32	PORT 9 - BIT 7	
33		34	PORT 9 - BIT 7	
35		36	PORT 7 - BIT 6	
37		38	PORT 7 - BIT 5	
39		40	PORT 7 - BIT 4	
41		42	PORT 7 - BIT 3	
43		44	PORT 7 - BIT 2	
45		46	PORT 7 - BIT 1	
47		48	PORT 7 - BIT 0	
49		GND	50	EXT INTR 2/

*
Pin numbers refer to board connector pins only, they are not necessarily the same on the mating connectors.

5.2 SYSTEM BUS SIGNAL DEFINITIONS

A summary definition of each system bus signal that is used by the SBC-519 is provided below.

INIT/ Initialization signal: reset the entire system to a known internal state.

CCLK/ Constant clock; provides a clock signal of constant frequency (10 MHz maximum) for use by option memory and I/O expansion boards. CCLK coincides with BCLK/

(Bus Clock - not used by SBC-519) and has a period of 100.00 nanoseconds, with a 30% - 70% duty cycle.

IORC/ I/O read command; indicates that the address of an input port has been placed on the system address bus and that the data at that input port is to be read and placed on the system data bus.

IOWC/ I/O write command; indicates that the address of an output port has been placed on the system address bus and that the contents of the system data bus are to be output to the addressed port.

XACK/ Transfer acknowledge signal; the required response of an external memory location or I/O port which indicates that the specified read/write operation has been completed. That is, data has been placed on, or accepted from, the system data bus lines.

AACK/ Advance acknowledge signal; used with 8080 CPU-based systems. AACK/ is an advance acknowledge, in response to memory or I/O access commands, that allows the CPU to proceed with the current instruction cycle.














ADRO/-ADRF/ 16 Address lines; used to transmit the address of the memory location or I/O port to be accessed ADRF/ is the most significant bit. Only ADRO/-ADR7/ are used by SBC-519.


DATO/-DAT7/ Bidirectional data lines; used to transmit/receive information to/from a memory location or I/O port. DAT7/ is the most significant bit.

INTO/-INT7/ Parallel Interrupt request lines; any one or more of the eight selected interrupt requests can be connected to these eight bus lines via on-board jumpers. These jumpers also allow any desired bit organization among the lines. These lines are independent of the data bus and bus interface logic and can be sampled without requiring an address or strobe.

INTR/ Direct Interrupt signal; signal line provided to support coded interrupt requests in special applications of system interrupt structure.

TABLE 5-5. PIN ASSIGNMENTS FOR CONNECTOR P1
(External System Bus)

(COMPONENT SIDE)			(CIRCUIT SIDE)		
PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
1	GND	Signal GND	2	GND	Signal GND
3	VCC	+ 5VDC	4	VCC	+ 5VDC
5	VCC	+ 5VDC	6	VCC	+ 5VDC
7	VDD	+12VDC	8	VDD	+12VDC
9	VBB	- 5VDC	10	VBB	- 5VDC
11	GND	Signal GND	12	GND	Signal GND
13			14	INIT/ 	Initialize
15			16		
17			18		
19			20		
21	IORC/ XACK/	I/O Read Cmd XFER Acknow	22	IOWC/	I/O Write Cmd
23			24		
25	AACK/	Advanced Acknowledge	26		
27			28		
29			30		
31	CCLK/ INTR/	Constant Clock Direct Interrupt	32		
33			34		
35	INT6/ INT4/ INT2/ INT0/	Parallel Interrupt Requests	36	INT7/ INT5/ INT3/ INT1/	Parallel Interrupt Requests
37			38		
39			40		
41			42		
43	ADRE/ ADRC/ ADRA/ ADR8/ ADR6/ ADR4/ ADR2/ ADRO/	Address Bus	44	ADRF/ ADRD/ ADRB/ ADR9/ ADR7/ ADR5/ ADR3/ ADR1/	Address Bus
45			46		
47			48		
49			50		
51			52		
53			54		
55			56		
57			58		
59			60		
61			62		
63			64		
65			66		
67	DAT6/		68	DAT7/	
69	DAT4/	Data Bus	70	DAT5/	Data Bus
71	DAT2/		72	DAT3/	
73	DAT0/		74	DAT1/	
75	GND	Signal GND	76	GND	Signal GND
77			78		
79	VAA	-12VDC	80	VAA	-12VDC
81	VCC	+ 5VDC	82	VCC	+ 5VDC
83	VCC	+ 5VDC	84	VCC	+ 5VDC
85	GND	Signal GND	86	GND	Signal GND

 Used by Intellec Microcomputer Development System bus.

Note: All mnemonics copyright 1976 Intel Corporation.



CHAPTER 6

COMPATIBLE EQUIPMENT

The SBC-519 is designed to interface directly with any SBC-80 single board computer via the system bus. It is mechanically compatible with both Intellec Microcomputer Development System chassis requirements and SBC-604 and SBC-614 4 modular cardcage, designed specifically for OEM applications. Details are presented in the following section.

6.1 SBC-80/10 AND SBC-80/20

The SBC-80/10 and SBC-80/20 are completely compatible with the SBC-519 TTL Programmable General Purpose I/O module. The SBC-80/10 or 80/20 can be interfaced with up to 9 combination modules. Table 6-1 summarizes access characteristics of the SBC-519.

6.2 MASTER MODULES

The SBC-519 can operate in systems containing more than one master module.

6.3 MODULAR BACKPLANE CARDCAGE

The SBC-604/614 Modular Backplane and Cardcage is designed specifically for OEM modules such as the SBC-519. Each card holder supports up to 4 modules. The modules may be electrically and mechanically "ganged" together for expanded capability. Provisions for power supply distribution, air circulation and bus exchange functions are featured on the OEM card holders.

TABLE 6-1. SBC-519 ACCESS CHARACTERISTICS WHEN USED WITH THE SBC-80/10

MODULE	INSTRUCTION	CPU CYCLES		CPU WAIT STATES		CYCLE TIME (μ sec)
		MIN	MAX	MIN	MAX	MIN
80/10	IOR	11	11	1	1	5.4
	IOW	12	12	2	2	5.9

REFERENCE:

IOR I/O READ: IN Addr 10 CYCLES
 IOW I/O WRITE: OUT Addr 10 CYCLES

6.4 INTELLEC MICROCOMPUTER DEVELOPMENT SYSTEM CARDCAGE

The SBC-519 is physically and electrically compatible with the Intellec Microcomputer Development System bus. The interface signals required by the SBC-519 (Table 5-5) are a subset of the Intellec Microcomputer Development System bus signal requirements.

CHAPTER 7

SBC-519 SPECIFICATIONS

7.1 DC POWER REQUIREMENTS

DC Power Requirements are given in Table 7-1.

7.2 AC CHARACTERISTICS

AC Characteristics are given in Table 7-2 and Figures 7-1 and 7-2.

7.3 DC CHARACTERISTICS

DC Characteristics are given in Table 7-3.

7.4 ENVIRONMENT

Temperature extremes can cause instability, or result in permanent damage to the circuits on the module. Ambient temperature must, therefore, be maintained within the limits of 0°C to 55°C. Exercise caution in locating the module, giving particular attention to radiant and conductive sources of heat. Remember that the module itself, when installed, will contribute some heat to the environment. Maintain an adequate clearance to permit the convective dissipation of heat from the elements on the card.

Relative humidity should not exceed 90%, non-condensing.

7.5 SBC-519 BOARD OUTLINE

See Figure 7-2.

TABLE 7-1. SBC-519 DC POWER REQUIREMENTS

VCC	5V ± 5%	ICC	1.5A WITH NO I/O DRIVER OR TERMINATOR
-----	---------	-----	---------------------------------------

TABLE 7-2. SBC-519 AC CHARACTERISTICS

I/O READ OR WRITE				
PARAMETER	MIN ns	MAX ns	DESCRIPTION	REMARKS
t_{AS}	50		Address Setup to Command	
t_{DS}	50		Write Data Setup to Command	
t_{AAK}	10	100	Command to Advanced Acknowledge Time	Jumper 34-24
t_{ACK}	$4 \cdot CCLK + 20$	$5 \cdot CCLK + 50$	Command to Transfer Acknowledge Time	Jumper 29-35, CCLK = 9.216 MHz
t_{WCMD}	410		Write Command Pulse Width	
t_{AH}	50		Address Hold Time	
t_{DH}	50		Write Data Hold Time	
t_{DHR}	0		Read Data Hold Time	
t_{TO}		65	Acknowledge Turn Off Delay	
t_{ACC}		300	Access Time to Read Data	
t_{RCMD}	410		Read Command Pulse Width	
CCLK	100	-		

INTERVAL TIMER INTERRUPT

The interval timer interrupt is generated from CCLK, thus interval timer interrupt timing accuracy depends on CCLK accuracy.

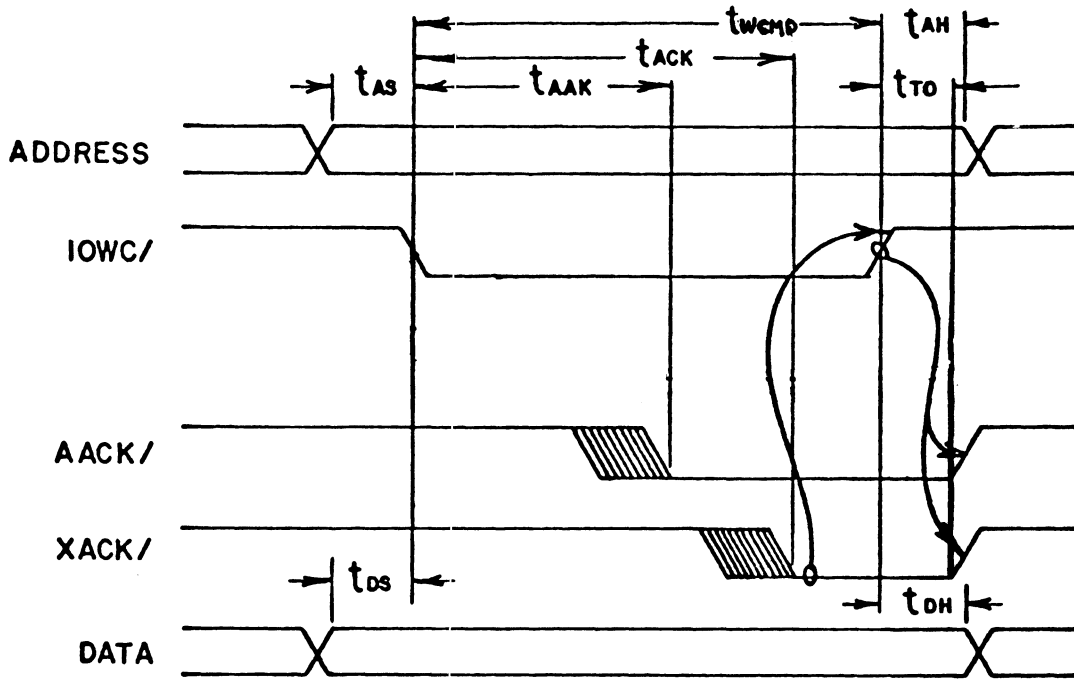
TABLE 7-3. SBC-519 DC CHARACTERISTICS

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
ADR ₀ /-ADR1/ ADDRESS INIT/	V _{IL}	Input Low Voltage			0.8	V
	V _{IH}	Input High Voltage		2.0		V
	I _{IL}	Input Current at Low V	V _{IN} = 0.4		-0.36	mA
	I _{IH}	Input Current at High V	V _{IN} = 2.7V		20	μA
	*C _L	Capacitive Load			18	pF
ADR2/-ADR6/ ADDRESS	V _{IL}	Input Low Voltage			0.85	V
	V _{IH}	Input High Voltage		2.0		V
	I _{IL}	Input Current at Low V	V _{IN} = 0.4V		.25	mA
	I _{IH}	Input Current at High V	V _{IN} = 5.25V		.01	mA
	*C _L	Capacitive Load			18	pF
AD7/	V _{IL}	Input Low Voltage			.8	V
	V _{IH}	Input High Voltage		2.0		V
	I _{IL}	Input Current at Low V	V _{IN} = 0.4		0.65	mA
	I _{IH}	Input Current at High V	V _{IN} = 5.25V		.03	mA
	*C _L	Capacitive Load			36	pF
AACK/ XACK/	V _{OL}	Output Low Voltage	I _{OL} = 32 mA		0.4	V
	V _{OH}	Output High Voltage	I _{OH} = -5.2 mA	2.4		V
	I _{LH}	Output Leakage High	V _O = 2.4		40	μA
	I _{LL}	Output Leakage Low	V _O = 0.4		-40	μA
	*C _L	Capacitive Load			15	pF
DAT ₀ /-DAT7/	V _{OL}	Output Low Voltage	I _{OL} = 50 mA		0.6	V
	V _{OH}	Output High Voltage	I _{OH} = -10 mA	2.4		V

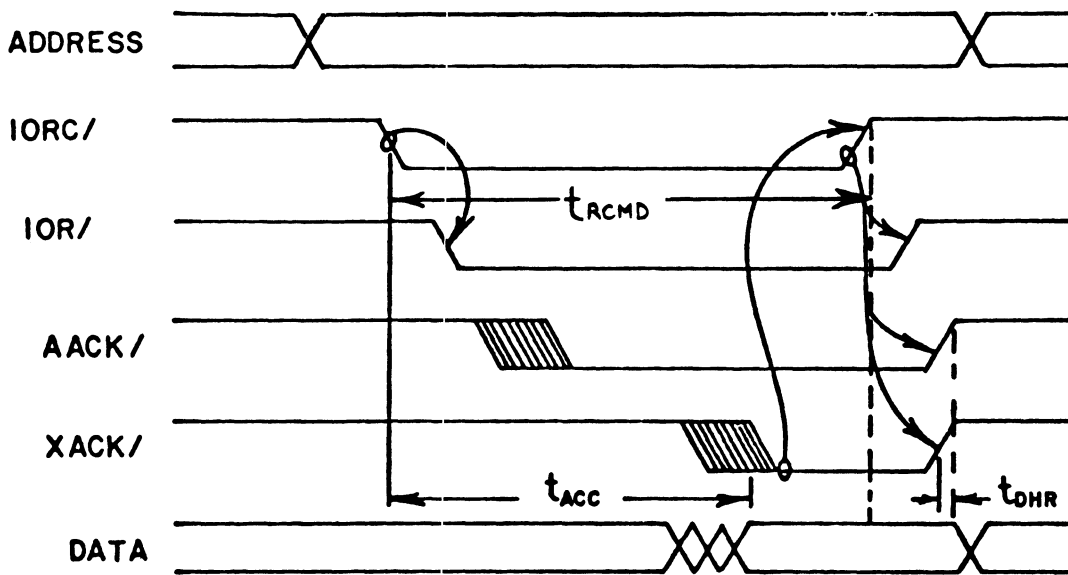
TABLE 7-3. SBC-519 DC CHARACTERISTICS (Continued)

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.45$		-0.25	mA
	I_{LH}	Output Leakage High	$V_0 = 5.25$		100	μ A
	* C_L	Capacitive Load			18	pF
INTR/ INTO/-INIT/	V_{OL}	Output Low Voltage	$I_{OL} = 16$ mA		0.4	V
	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	* C_L	Capacitive Load			18	pF
EXT INT 1/ EXT INT 2/ EXT INT 3/ (1K P.U.)	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.4V$		-6.0	mA
	I_{IH}	Input Current at High V	$V_{IN} = 0.7V$		3.0	mA
	* C_L	Capacitive Load			18	pF
BIDIRECTIONAL DRIVERS (8226) (1K P.U.)	V_{OL}	Output Low Voltage	$I_{OL} = 20$ mA		.45	V
	V_{OH}	Output High Voltage	$I_{OH} = -12$ mA	2.4		V
	V_{IL}	Input Low Voltage			.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.45$		-5.05	mA
	I_{IH}	Input Current at High V	$V_{IN} = 5.25V$.60	mA
	* C_L	Capacitive Load			18	pF
8255 DRIVER/ RECEIVER	V_{OL}	Output Low Voltage	$I_{OL} = 1.6$ mA		.4	V
	V_{OH}	Output High Voltage	$I_{OH} = -100$ μ A	2.4		V
	V_{IL}	Input Low Voltage			.8	V
	V_{IH}	Input High Voltage		2.0		V
	* C_L	Capacitive Load			18	pF

*Capacitance values are approximations only.

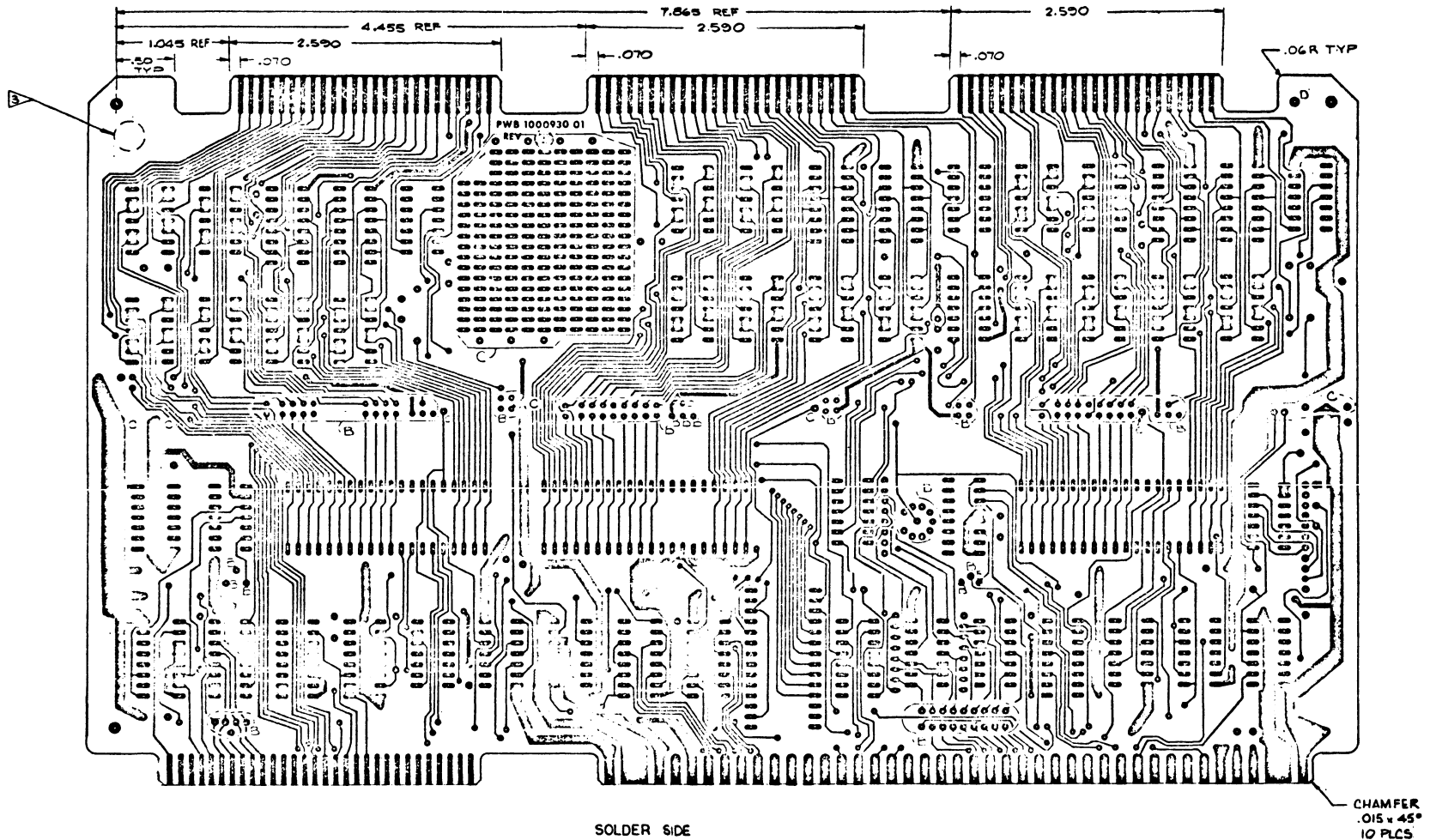


A. WRITE TO I/O PORT



B. READ I/O PORT

FIGURE 7-1. I/O READ AND WRITE PORT TIMING



NOTE: UNLESS OTHERWISE SPECIFIED

1. PART NO. IS 1000930-01
2. FABRICATE PER DRAWING NO. 4000282-02
3. MARK VENDOR IDENTIFICATION CODE.
4. HOLES ARE CODE SYMBOL "A".

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intel		3065 BOWERS AVE. SANTA CLARA CALIF. 95051	
		PRINTED WIRING BOARD TTL PGPI/O	
REV	DATE	DRAWN BY	REV
D	1410	1000930	A

FIGURE 7-2. SBC-519 BOARD OUTLINE (1 of 2)

7-7

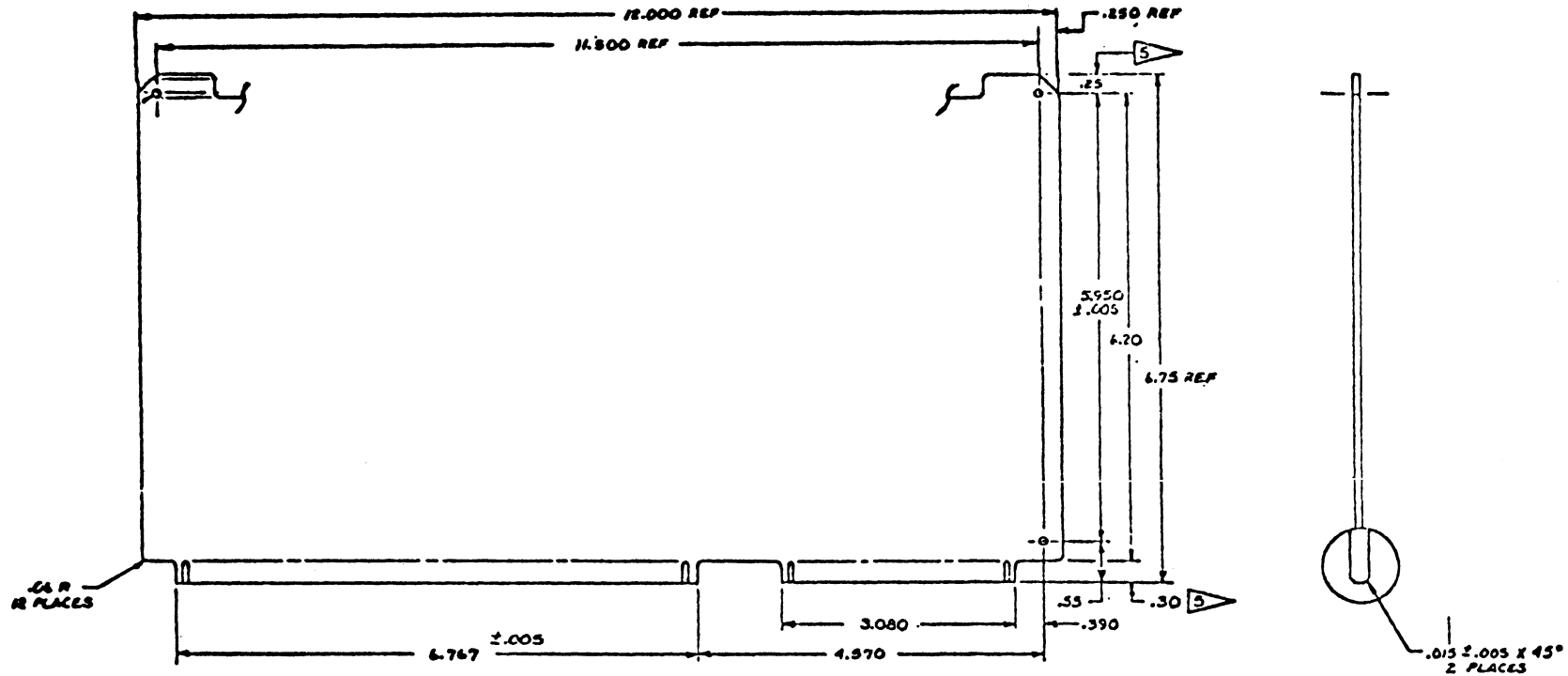


FIGURE 7-2. SBC-519 BOARD OUTLINE (2 of 2)

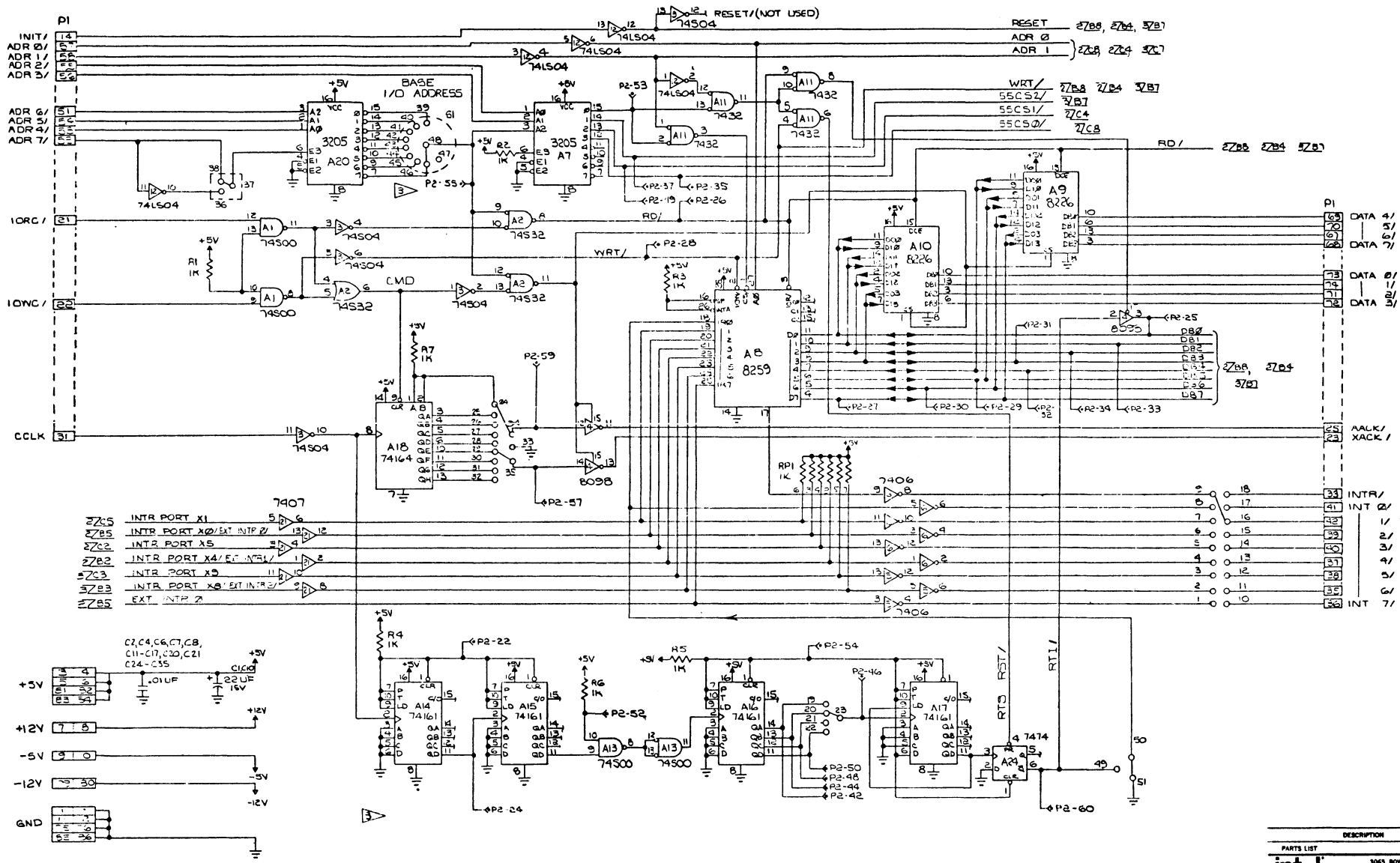
NOTES:

1. MATERIAL : .062 THK, 1 OZ COPPER CLAD, NATURAL EPOXY GLASS, TYPE 510 (202 AFTER PLATING THRU)
2. BOARD EDGES ARE LOCATED FROM INDEX HOLES. INDEX HOLES ARE ON .050 GRID INTERSECTION AND ARE USED FOR ARTWORK REGISTRATION AND MAY BE USED AS TOOLING HOLES, PLATING OPTIONAL.
3. HOLES ARE PLATED THRU WITH COPPER WALL THICKNESS OF .0007 MINIMUM.
4. HOLE SIZES SPECIFIED ARE AFTER PLATING; $\pm .003$ TOLERANCE
5. CONTACT FINGERS ARE OVERPLATED WITH A MINIMUM OF 50 MILLIONTHS GOLD OVER NICKEL TO DIMENSION SHOWN.
6. APPLY SOLDER MASK OVER SOLDER PLATE USING MATERIAL; MECUMASK GREEN
- 7.
8. DRILL FROM CIRCUIT SIDE.
9. TRACE WIDTHS MUST BE WITHIN .004 OF ARTWORK NEGATIVES.
10. APPLY SILKSCREEN ON COMPONENT SIDE, AFTER SOLDER MASK IS APPLIED, USING WHITE EPOXY INK.

APPENDIX A

SBC-519 SCHEMATICS

Schematic drawings for the SBC-519 are provided in this appendix. Information and diagrams in this section are subject to change without notice. References should be made to schematics shipped with this module.

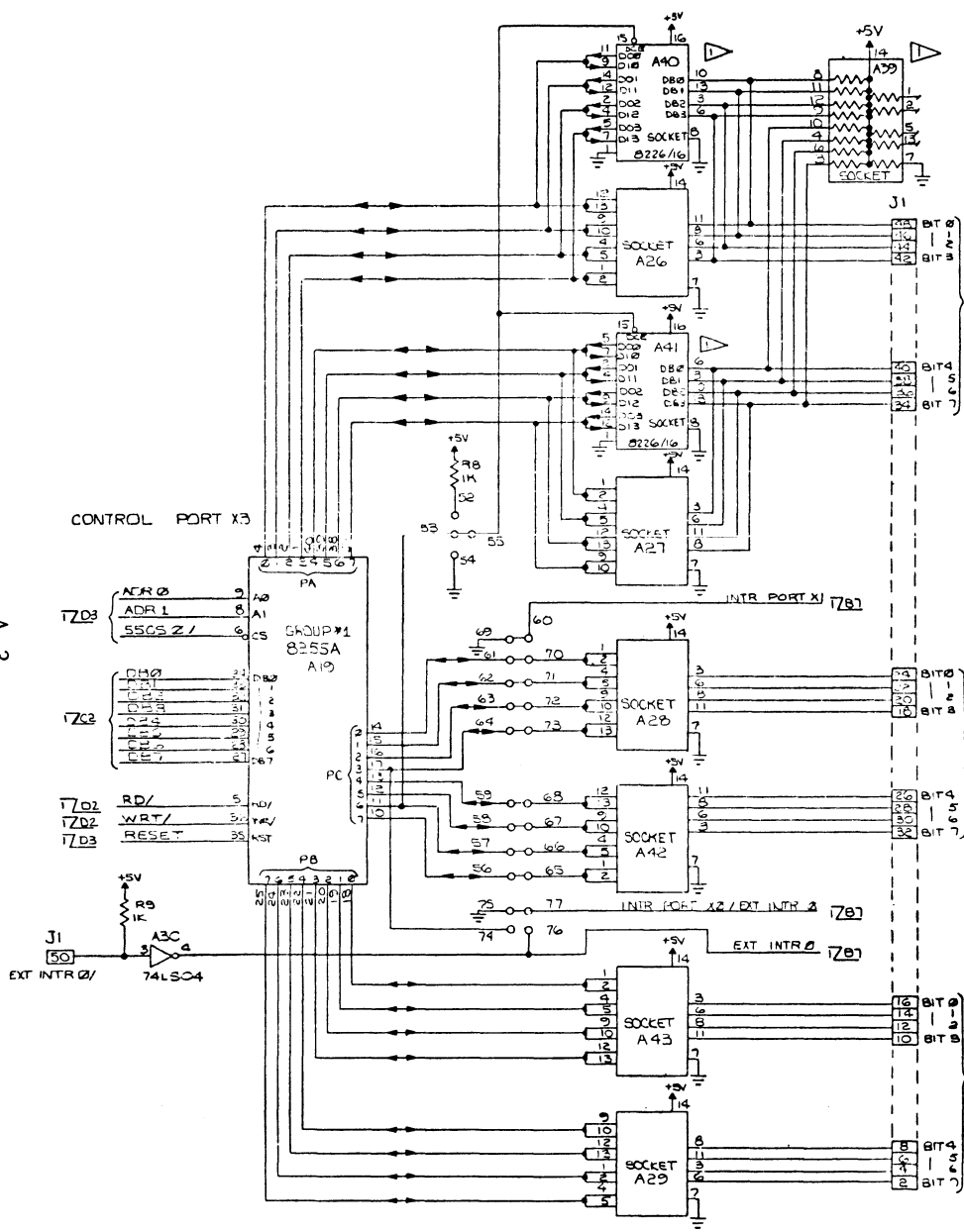


2705 INTR PORT X1
 2706 INTR PORT X0/EXT INTR Z
 2702 INTR PORT X5
 2702 INTR PORT X4/EXT INTR
 2703 INTR PORT X3
 2703 INTR PORT X0/EXT INTR
 2705 EXT INTR Z

NOTES UNLESS OTHERWISE SPECIFIED,
 ▷ SOCKETS SUPPLIED - USER FURNISHES ACTUAL PARTS.
 2. RESISTOR VALUES ARE IN OHMS, KΩ, ±5%.
 ▷ X=ANY HEX DIGIT SELECTED BY S1 AND JUMPER 2, 37, AND 38.

PARTS LIST		DESCRIPTION	
intel		3065 BOWERS AVE. SANTA CLARA CALIF. 95051	
TITLE SCHEMATIC			
TTL PDP11/0			
SIZE D	DEPT 110	DRAWING NO. 2000931	REV A

A-3

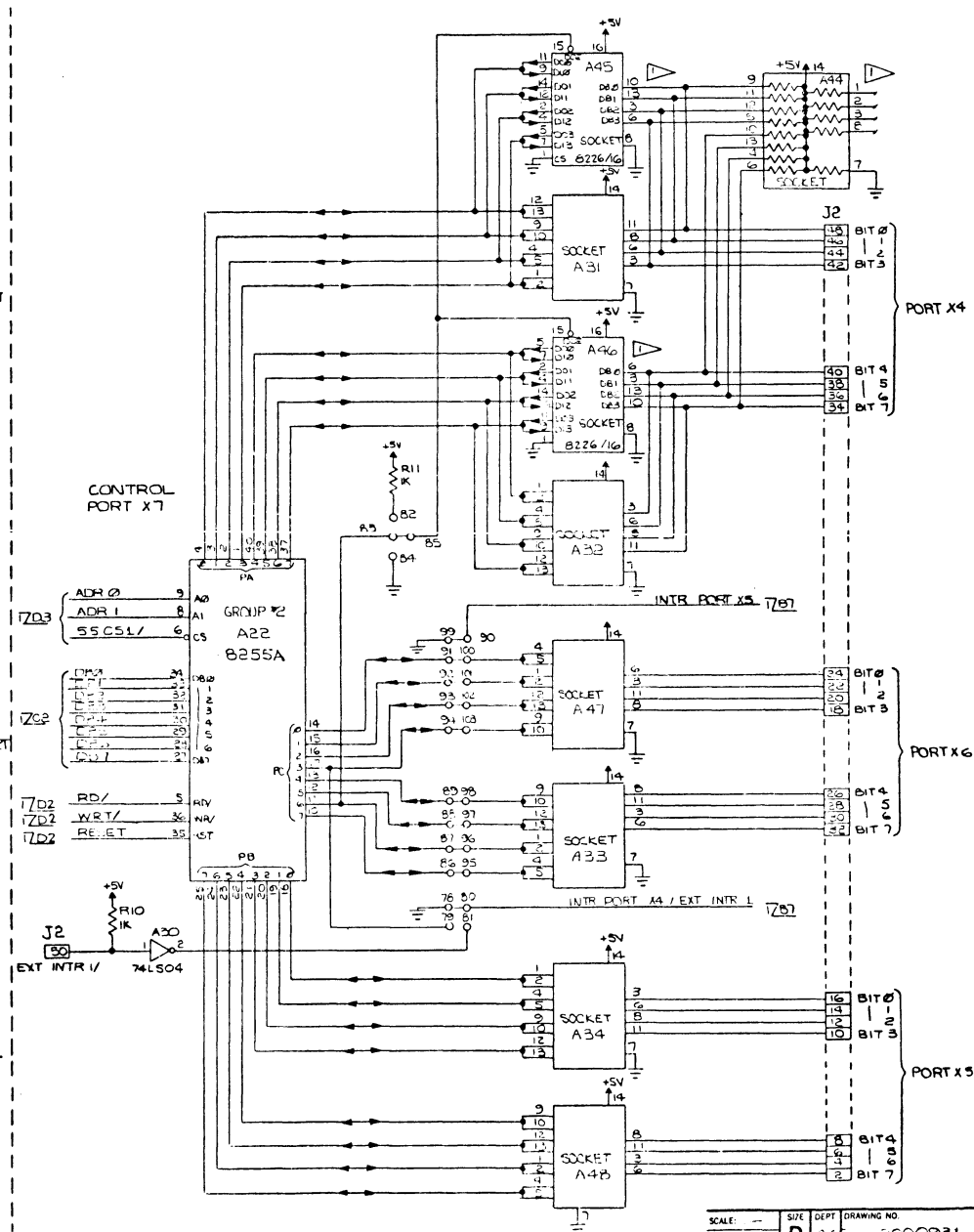


PORT X0

PORT X2

PORT X1

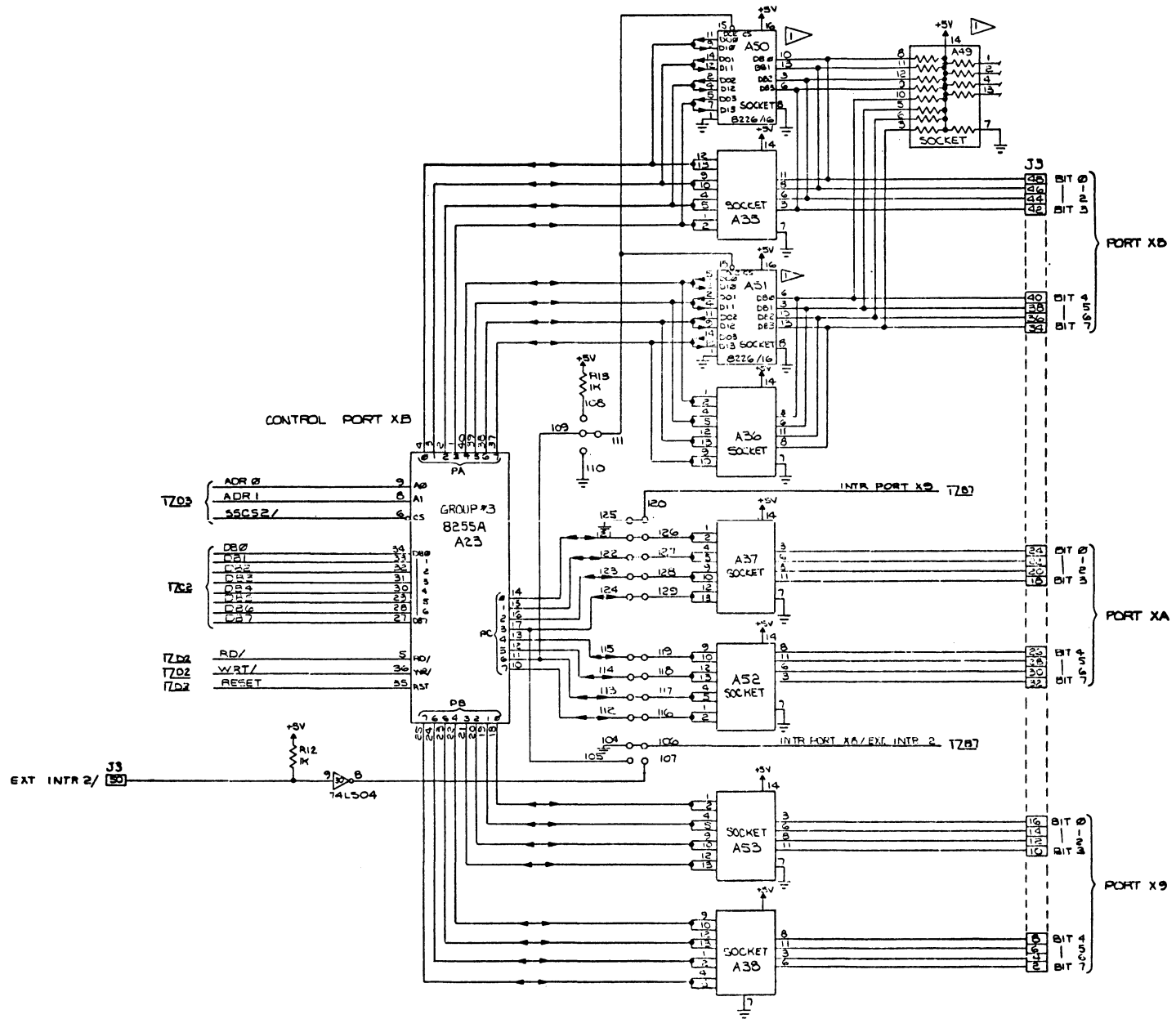
CONTROL PORT X7



PORT X4

PORT X6

PORT X5



APPENDIX B

SBC-901, SBC-902 SCHEMATICS

Schematic drawings for the SBC-901 and SBC-902 are provided in this appendix. Information and diagrams in this section are subject to change without notice.

RESISTOR NETWORK SPECIFICATIONS:

RESISTANCE VALUES:
±2% (MAX)

OPERATING TEMPERATURE:
0°C TO +70°C

TEMPERATURE COEFFICIENT:
±200 PPM/°C OVER TEMPERATURE
RANGE OF 0°C TO +70°C

OPERATING VOLTAGE:
5.0 VDC (MAX)

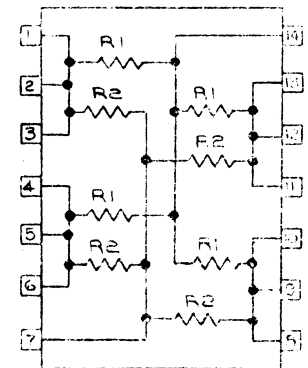
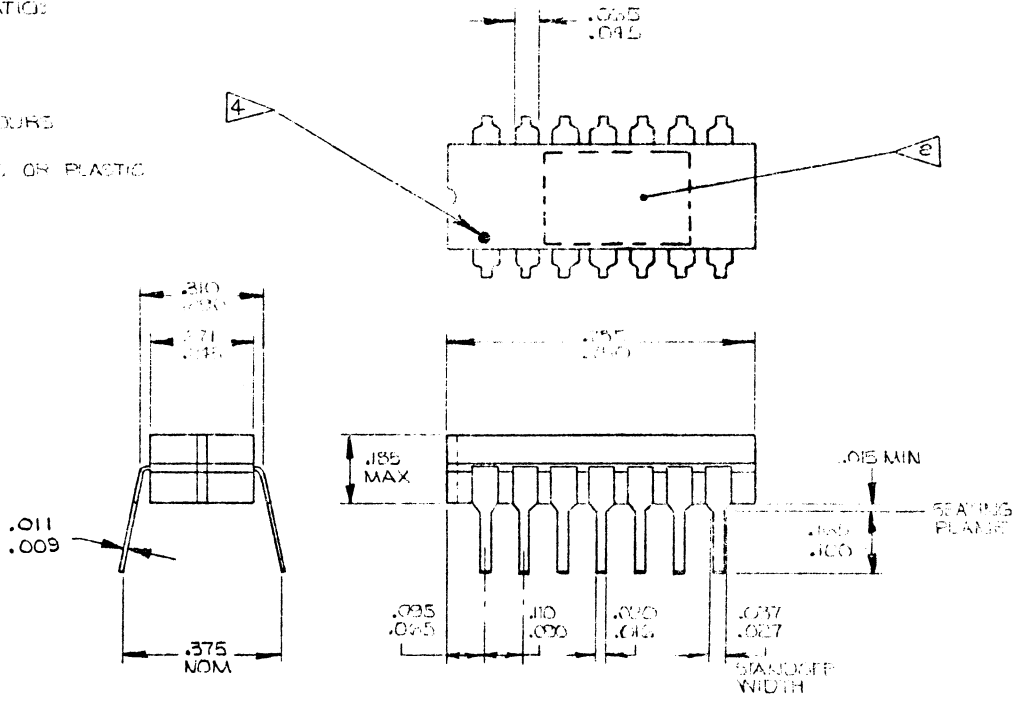
POWER RATING:
AT 70°C, 0.7 WATT PER PACK

TRACKING RESISTANCE RATIO:
±1.0% (MAX)

STABILITY:
±1% YEAR (MAX)

LOAD LIFE:
±1% (ΔR) OVER 1000 HOURS

PACKAGE:
DUAL IN LINE - CERAMIC OR PLASTIC



NOTES:

UNLESS OTHERWISE SPECIFIED,

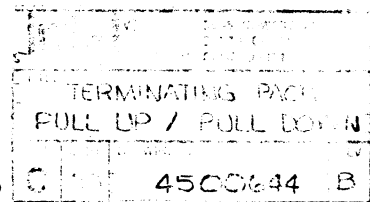
1. PART NO IS 4500644-01.

2. INK STAMP PRODUCT CODE, RESIST R VALUE, PART NO, AND DASH NUMBER WITH CONTRASTING COLOR INK USING MIN .05 HIGH CHARACTERS. NO OTHER MARKINGS PERMITTED EXCEPT MANUF BATCH NO.

E.G.) SBC-901
R220 / 330
4500644-01

3. FOR PROCUREMENT SEE LV 4500644-01.

4. IDENTIFY PIN ONE CLEARLY ON TOP OF PACKAGE.



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RESISTOR NETWORK SPECIFICATIONS:

RESISTANCE VALUES:
±2% (MAX)

OPERATING TEMPERATURE:
0°C TO +70°C

TEMPERATURE COEFFICIENT:
±200 PPM/°C OVER TEMPERATURE
RANGE OF 0°C TO +70°C

OPERATING VOLTAGE:
6.0 VDC (MAX)

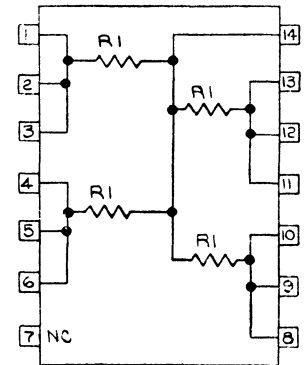
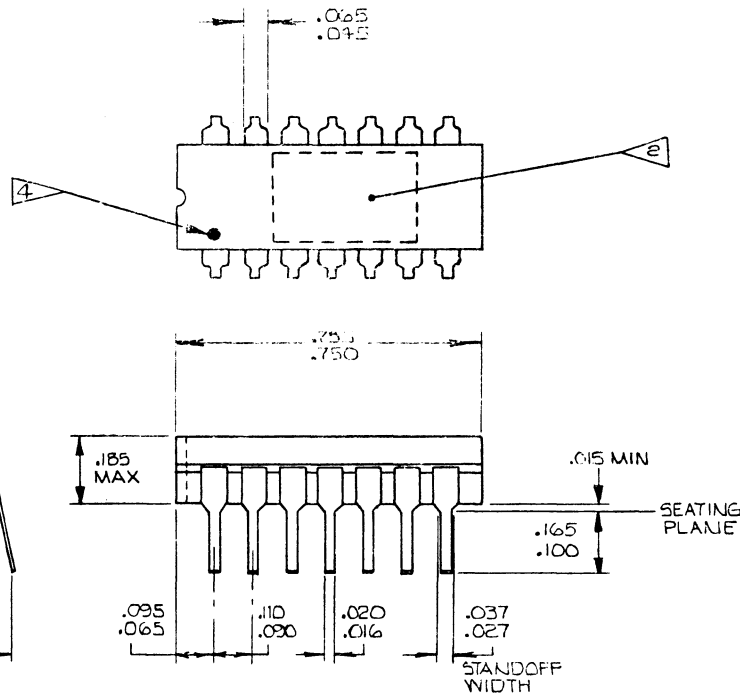
POWER RATING:
AT 70°C, 0.7 WATT PER PACK

TRACKING RESISTANCE RATIO:
±1.0% (MAX)

STABILITY:
±1% YEAR (MAX)

LOAD LIFE:
±1% (ΔR) OVER 1000 HOURS

PACKAGE:
DUAL IN LINE - CERAMIC OR PLASTIC



B-3

NOTES:

UNLESS OTHERWISE SPECIFIED,

1. PART NO IS 4500645-01.

2. INK STAMP PRODUCT CODE, RESISTOR VALUE, PART NO AND DASH NUMBER WITH CONTRASTING COLOR AND MIN .12 HIGH CHARACTERS. NO OTHER MARKINGS ARE PERMITTED EXCEPT FOR MANUF BATCH NO.

E.G.) SBC-902
R1K
4500645-01

3. FOR PROCUREMENT SEE LV4500645

4. IDENTIFY PIN ONE CLEARLY ON TOP OF PACKAGE.

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intel		3065 BOWERS AVE. SANTA CLARA CALIF. 95051	
TITLE TERMINATING PACK PULL UP			
SIZE C	DEPT 410	DRAWING NO. 4500645	REV E

APPENDIX C

INTERRUPT SERVICE ROUTINE PROGRAMMING NOTES

This appendix summarizes the basic programming tasks involved in handling interrupt requests from the SBC-519. Although these notes are very general and apply primarily to the polled mode, they also define the basic requirements for a nested service routine scheme.

INITIAL CONDITIONS: 8080 INT input has been enabled via EI instruction; INT input goes high.

	<u>STEP</u>	<u>COMMENT</u>
	JMP TO INTR	Interrupt vector location Program jumps to location labeled INTR
INTR:	PUSH PSW PUSH B PUSH D PUSH H	Save machine status
	MVI A, POLMOD OUT P59CT	Put 8259 in polled mode
	IN P59CT	Read 8259 INTR level; this is an octal code appearing on data lines 0-2 that identifies which level is interrupting
	ANI 07H	
	RAL RAL	Shift the 3-bit interrupt code two places to provide 4-byte addressing intervals
	LXI H, INTBL ADD L MOV L, A	Form the service routine jump address by adding the 3-bit interrupt level code to the base address of a jump table. This table contains addresses of service routines for all eight interrupt levels.
	PCHL	Jump to service routine specified by H,L. This address will be equal to the jump table base address plus:

	<u>STEP</u>	<u>COMMENT</u>
INTBL:		Interrupt routine jump table Must not cross page (XXFF) boundary
	JMP INTR0 NOP	Jump to service routine for interrupt level 0
	JMP INTR1 NOP	Jump to service routine for interrupt level 1
	JMP INTR2 NOP	Jump to service routine for interrupt level 2
	JMP INTR3 NOP	Jump to service routine for interrupt level 3
	JMP INTR4 NOP	Jump to service routine for interrupt level 4
	JMP INTR5 NOP	Jump to service routine for interrupt level 5
	JMP INTR6 NOP	Jump to service routine for interrupt level 6
	JMP INTR7 NOP	Jump to service routine for interrupt level 7
INTR0:		
		Level 0 Service Routine
	JMP INTEND	
INTR1:		
		Level 1 Service Routine
	JMP INTEND	
INTR2:		
		Level 2 Service Routine
	JMP INTEND	
INTR3:		
		Level 3 Service Routine
	JMP INTEND	

	<u>STEP</u>	<u>COMMENT</u>
INTR4:		
	Level 4 Service Routine	
	JMP INTEND	
INTR5:		
	Level 5 Service Routine	
	JMP INTEND	
INTR6:		
	Level 6 Service Routine	
	JMP INTEND	
INTR7:		
	Level 7 Service Routine	
INTEND:		
	MVI A, EOI	Send end of interrupt to 8259.
	OUT P59CT	(OCW2)
	POP H	Restore machine status
	POP D	
	POP B	
	POP PSW	
	EI	Enable 8080 interrupt
	RET	Return to main program
EOI	EQU 20H	
POLMOD	EQU 0CH	
P59CT	EQU XCH	Where X = 0 through F ₁₆ (I/O base address)

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