SBC 104/108

COMBINATION MEMORY AND I/O EXPANSION BOARDS

HARDWARE REFERENCE MANUAL

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SBC 104/108

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

RELATED INTEL PUBLICATIONS

Publication Number	Title
98-230	SBC 80/10 HARDWARE REFERENCE MANUAL
98-132	INTELLEC®MDS HARDWARE REFERENCE MANUAL
98-153	INTEL®8080 MICROCOMPUTER SYSTEMS USER'S MANUAL
AP-15	8255 PROGRAMMABLE PERIPHERAL INTERFACE APPLICATIONS NOTE
AP-16	8251 USART APPLICATIONS NOTE

CHAPTER 1

INTRODUCTION

The SBC 104/108 Combination Memory and I/O Expansion Boards are members of Intel's complete line of SBC 80 memory and I/O expansion boards. They interface directly (via the system bus) with any SBC 80 Single Board Computer to expand system interrupt levels, RAM and ROM memory capacity, and serial and parallel I/O lines. The SBC 108 is functionally identical to the SBC 104 except in RAM memory capacity. The SBC 104 has 4K of RAM implemented with INTEL® 2104s while the SBC 108 has 8K of RAM implemented with INTEL® 2108s. This manual presents a complete functional and physical description of the SBC 104. Except where otherwise noted, or reference is made to RAM capacity, this description is also true of the SBC 108.

The RAM memory expansion feature consists of eight Intel dynamic RAM memory components, providing 4K/8K bytes of read/write memory. Refresh control is provided onboard using an Intel® 3222 refresh controller. Refresh cycles are initiated asynchronously with respect to system memory (read/write) cycles. Any resulting competition between refresh and system

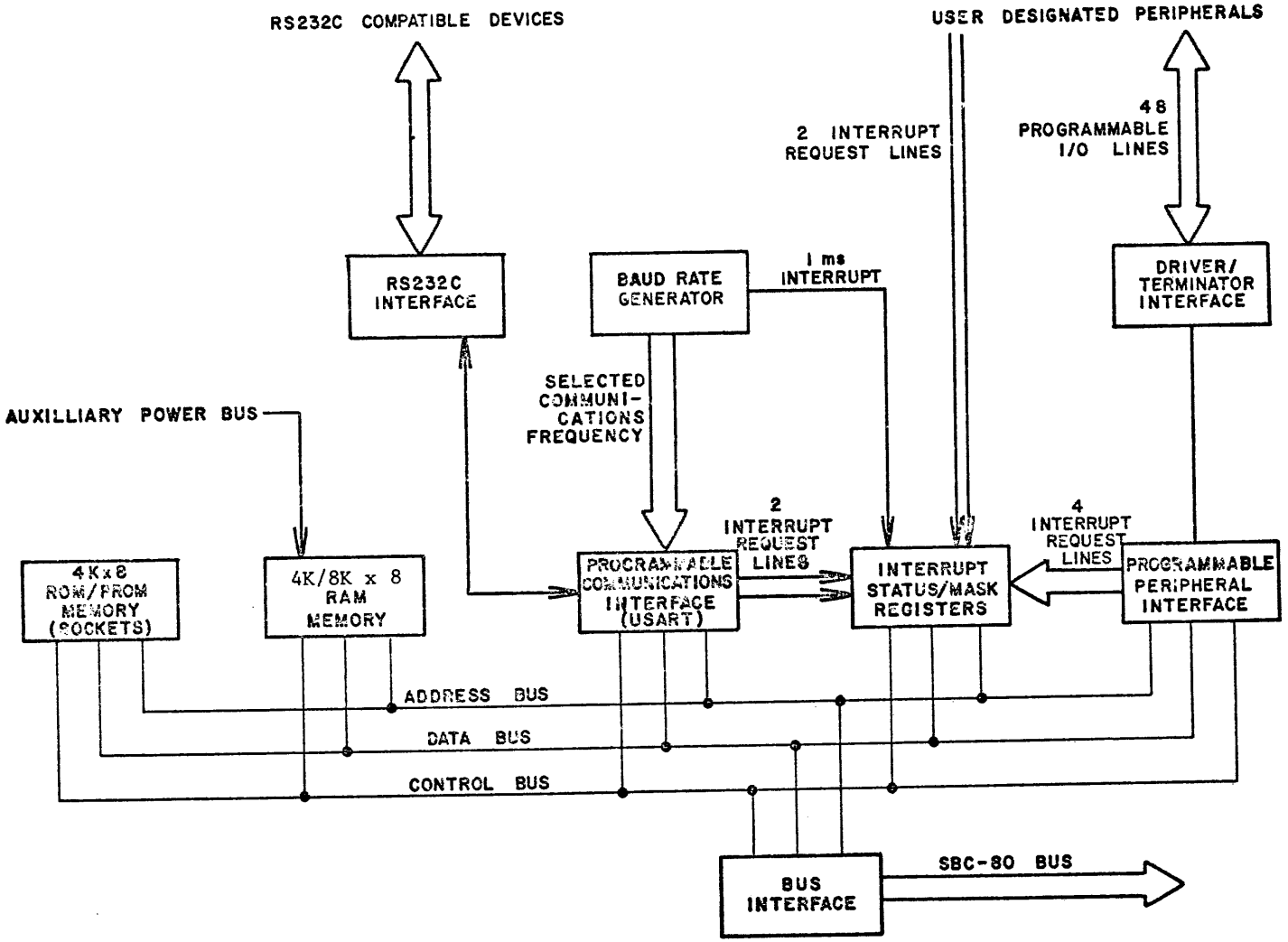


FIGURE 2-1. SBC 104/108 FUNCTIONAL BLOCK DIAGRAM

is the memory and I/O address assignment hardware, consisting of two rocker switch packages and various sets of wire wrap jumper pins.

The Random Access Memory (RAM) section provides 4096 × 8 bits of read/write storage. Eight Intel® 2104 dynamic memory chips (4096 × 1 bits each) are used for the memory elements. The other circuit functions directly related to RAM functions include the following.

- Intel®8222 refresh controller, which coordinates RAM cycle requests from the system bus with internally generated refresh requests. Sixty-four refresh cycles are required to refresh all memory cells in the array.
- Address multiplexer, which multiplexes the six or seven low-order address bits (row) with the six or seven high-order address bits (column). During refresh cycles, only the row address bits are used.
- Intel®8212 latched buffer, which stores the read data that is present at the RAM array's data out pins.
- Various flip-flops, shift registers and combinatorial logic elements that, together, control access to the RAM and its output buffer. These elements also control the generation of RAM access acknowledge signals.
- Intel®8224 crystal-stabilized clock generator, which provides the fundamental timing reference for the RAM access control logic. It also supplies TTL-level clocks to the USART.

The Read Only Memory (ROM/PROM) section provides sockets for installing up to 4096 × 8 bits of ROM or PROM. There are four 24-pin sockets that can accept either Intel's 8708 Erasable and Electrically Programmable Read Only Memory chips or Intel's 8308 Static MOS Read Only Memory chips. Each of these chips contains 1024 × 8 bits.

The Parallel I/O Interface consists of two Intel®8255 Programmable Peripheral Interface devices, four Intel 8226 Four-Bit Parallel Bidirectional Bus Driver chips and eight 14-pin sockets for installing quad

line driver and/or terminator packages as required to satisfy the particular I/O interface requirements. The input/output configuration of each 8255 device is programmed independently, with the three ports (A, B and C) of one device treated as one group and the three ports of the other device as a separate group. Wire wrap jumper pins allow the factory-installed 8226 devices to be conditioned for input, output or bidirectional operation. Other jumper pins allow the user to implement up to four I/O lines (two per group) to be implemented as interrupt request lines.

The Serial I/O Interface provides a bi-directional serial data communications channel that can be programmed to conform to most current serial data transmission protocols. It consists of an Intel 8251 Programmable Communication Interface chip, three binary counters, a baud rate select switch and two sets of level translators. One set of level translators converts TTL levels to RS232C-compatible levels. The other set converts signals received from the RS232C lines to TTL levels. Various wire wrap jumper connections are also provided to permit the user to configure the Serial I/O Interface as a data set or as a data processing terminal.

The Interrupt Status/Mask section consists of an Intel 8212 Eight-Bit Input/Output Port, a set of interrupt mask gates, an interrupt status/mask multiplexer, an 8-into-1 OR function, a set of line drivers and an interval timer interrupt circuit. The 8212 serves as the mask register providing appropriate enables for the interrupt status gates. The multiplexer holds either the current mask word or interrupt status for interrogation by the bus master. Multiplex control is exercised by the

bus master. The OR function combines the eight masked interrupt requests into a single interrupt flag. The interval timer interrupt circuit consists of a latch that is set approximately every 1 ms and is cleared by the bus master. This feature is incorporated by wire wrap connection at the factory. If both external interrupts are to be used, the interval timer interrupt jumper must be replaced by an external interrupt jumper. Jumper connections are also required to connect each of the interrupt requests outputs to the P1 connector. This feature provides maximum flexibility in making interrupt request line assignments.

2.2 PROGRAMMING CHARACTERISTICS

This section summarizes the SBC-104 memory and I/O addressing characteristics.

Separate base address assignments are made for the RAM, PROM and I/O facilities through the use of wire wrap jumpers and switch selections. A single base address is used for all I/O elements (i.e., parallel I/O interface, serial I/O interface and interrupt mask/status registers).

This base address selectability feature affords great flexibility in fitting the SBC-104 into the system addressing scheme. However, when assigning address space to the SBC-104 memory and I/O elements, the user must be careful not to violate any dedicated or previously assigned address space (e.g., the CPU module's on-board memory).

2.2.1 RAM ADDRESS ASSIGNMENT

Memory space is assigned to the SBC-104 RAM in 4K segments, with

data, which had been received by the USART in serial form, can be read from the I/O port via the SBC 104 data bus. The control register is used to program the USART. Details regarding the control word used for USART programming are provided in Section 3.5.

The USART I/O data port and control registers have the following addresses.

USART DATA	XC	READ/WRITE
USART CONTROL	XD	READ/WRITE

X = any hex digit; assigned by jumper selection;
X is the same for all I/O ports and registers.

2.2.6 INTERRUPT MASK/STATUS REGISTER ADDRESSES

The interrupt mask and interrupt status registers have separate addresses. If the interval timer interrupt option is used, the function must be initialized after each timed interrupt. This is done at a third interrupt address.

The three interrupt addresses are as follows.

Interrupt Status	XO	READ ONLY
Interrupt Mask Register	X1	READ*/WRITE
Interval Timer Interrupt	X2**	WRITE ONLY

*Note: Read to mask register yields the mask in complement form.

**Note: The interval timer can be reset at the same time the mask register is loaded by using X3.

Chapter 3

THEORY OF OPERATION

In the preceding chapter, each of the SBC 104 functional blocks was identified and briefly defined. This chapter explains how these functions are implemented.

Summarized schematics of the relevant logic elements are included for clarification. However, these diagrams are intended as supplements to the text only. Although they are derived from the engineering logic drawings, they may differ from the controlled drawings in non-functional specifics. For detailed circuit information, refer to the SBC 104 schematics, which are provided in Appendix A.

Note: Both active-high (positive true) and active-low (negative true) signals appear in the SBC 104 schematics. To avoid confusion when referring to these signals in this chapter, the following convention is used. The mnemonic (signal label) for each active-low signal is terminated by a slash; e.g., IOW/ means that the signal level on that line will be low when the I/O write command is true (active). A mnemonic without the slash refers to an active-high signal; e.g., the line labeled MEM W is at the high logic level when the memory write signal is true.

3.1 BUS INTERFACE

The Bus Interface refers to those logic elements that participate directly in the following types of system bus activity.

1) System address, control and data buffering

2) System address decoding

3) System control signal propagation

4) Transfer acknowledge generation.

The four groups of Bus Interface logic responsible for these tasks are described in the following paragraphs.

3.1.1 BUS ADDRESS, CONTROL, DATA BUFFERS

The bus address and control signal buffer circuits consist of inverting line receivers of the 74LS04 (address) and 74S04 (control) types. These circuits restore the signals on the system bus lines to their proper logic levels with very high switching speed.

The data buffers are formed by two Intel 8226 inverting bidirectional driver/receiver chips (A74 and A75). The system data bus is connected to the devices' DB pins. The DO and DI pins of each chip are connected, via printed wires, to the interrupt mask register, RAM data inputs and outputs, PROM data inputs, parallel I/O interface ports and serial I/O interface USART chip.

Directional control (DIEN/) for A74 and A75 is excercised by the memory read and I/O read commands (MRDC/ and IORC/) through NOR gate A41-1. If either read command is asserted by the bus master, the data buffer's driver mode is selected. At all other times, the data buffer's receiver circuits are enabled.

Control of chip select (CS/) for the data buffer is exercised through a set of combinatorial logic, whose final stage is NOR gate A41-4. The data buffer is selected if any one of the following sets of conditions is decoded.

1) RAMAD · INH 1/(NOT) · (MWTC/ + MRDC/) -
   If a RAM address is decoded AND the memory space is not shared by the PROM AND either a memory write or memory read command is received, a chip select is generated for A74 and A75.

2) PMAD/ · INH 2/(NOT) · MRDC/ -
If a PROM address is decoded (PMAD/) AND INHIBIT 2 is not present AND a memory read command is received, a chip select is generated for A74 and A75.

3) IOAD/ · (IOWC/ + IORC/) -
If an I/O address is decoded AND either an I/O write or I/O read command is received, a chip select is generated for A74 and A75.

3.1.2 SYSTEM ADDRESS DECODE LOGIC

This logic decodes the appropriate system bus address bits into a RAM request, PROM request or an I/O select. Associated with the decode logic are switches and jumper connections that permit field-modification of base address assignments.

Note: Row and column address decoding for memory accessing is a separate function, which is performed in the selected memory chips.

Memory address decoding is carried out by a pair of 74S151 devices, designated A56 (RAM address decoder) and A57 (PROM address decoder). These are 8-into-1 multiplexers, with true and complementary outputs.

Device A56 tests bus address lines ABC, ABD and ABE for the base address assigned to the RAM expansion memory. This base address is assigned by opening the appropriate switch on S3, which applies a high (true) logic level at the corresponding data input of the address decoder.

Note: The address decoder's data inputs are high-true, so that an OPEN switch is required to activate an input.

Address bit F is applied to the RAM address decoder's strobe input in either its true or complementary form (ABF or ABF/). This selection

determines the bit significance of the S3 switches. If ABF is used, the switch values range from 0 to 7. ABF/ increases the switch values to the range 8 to F.

Jumper pins 90, 89 and 91 are provided for this selection (90 - 89 selects ABF; 90-91 selects ABF/).

The three-bit address (ABC, ABD, ABE) enables one of the switch controlled data inputs through to the RAM address decoder's Y (true) output. When that address value corresponds to the switch-selected base address, the address decoder's output will go high (true).

This output, designated RAMAD, is ANDed with various other logic conditions to provide a chip select to the bidirectional data buffer (A74, A75) and to produce the RAM logic enable RAM REQ. The conditions required to generate RAM REQ are:

$$\text{RAMAD} \cdot \overline{\text{INH 1/}} \cdot (\text{MWRC/} + \text{MRDC/})$$

INH 1/ is a RAM inhibit that is part of the system bus. It is used to prevent RAM devices in the system from responding whenever system memory space used by a PROM is addressed. On the SBC-104, it is used to prevent the generation of RAM REQ. INH 1/ must be false for RAM REQ and the bidirectional data buffer chip select to be generated.

RAM REQ is used to enable various elements of the RAM control logic for operation. Details regarding its implementation are provided in Section 3.2, Random Access Memory (RAM).

Additional address space can be assigned to the SBC-104 RAM elements by opening (selecting) more than one S3 switch. Each open switch specifies a base address for a separate 4K block of RAM.

A PROM REQ/ is generated in a manner similar to RAM REQ generation.

Base address assignments for the PROM are made through switch package S4. Decoder A57 tests address bits ABC, ABD and ABE as specified by the S4 selection. A57 is enabled by either ABF or ABF/ through jumper connections 93-92 or 93-94. This selection controls the bit significance of the S4 switches. If ABF is used (pins 93-92), the S4 switches are assigned the values 0 to 7. ABF/ (pins 93-94) increases the switch values to the range 8 to F.

If A57 is enabled and the ABC, ABD and ABE bits contain the base address specified by S4, the W (complementary) output of A57 goes low (true).

This output, designated PMAD/ , is combined with the INH 2 and MEM R conditions to provide a chip select to the bidirectional data buffer (A74, A75) and to produce the PROM logic enable PROM REQ. The conditions required for PROM REQ are:

$$\text{PMAD/} \cdot \overline{\text{INH 2/}} \cdot \text{MEM R}$$

INH 2 is a system-wide PROM inhibit. It is asserted when a segment of memory space that is shared by more than one PROM is preempted by one of the PROM's for some special function such as bootstrap initialization.

PROM chip select generation is performed by one half of A43, which is a dual one out of four binary decoder (74S 139). This device decodes address bits ABA and ABB to generate one of four PROM chip selects, PCS0/ through PCS3/. Provision is made for future memory enhance-

ment in which the ABA input will be deleted and the ABC input added.

The other half of A43 is used by the I/O address decode logic to generate one of four I/O port selects. This general function is described next.

I/O address decoding is carried out in two stages, represented by A42 and A43.

The first stage, A42, is an Intel 8205 one out of eight binary decoder. It decodes address bits AB4, AB5 and AB6 into the I/O select level labeled IOAD/.

Jumper pad S2 allows IOAD/ to be taken from any of the eight decode outputs of A42. This means that any of the eight possible address combinations provided by AB4-6 can be assigned to IOAD/.

Furthermore, jumper pins 87, 88 and 86 permit the selection of either AB7 or AB7/ as the enable for A42. If AB7/ is used (connect 87 - 86), the eight address decoder outputs are given the relative values 0 to 7. If AB7 is used (connect 87 - 88), the decoder outputs take the values 8 to F.

When the AB4 through AB7 bits correspond to the I/O address that is specified by S2 and pins 87, 88 and 86, IOAD/ goes low (true). This level enables the I/O port select decode stage, which consists of one half of A43.

A43 decodes address bits AB2 and AB3 into one of four I/O port selects:

ADDRESS BITS		I/O SELECT
3	2	Output
0	0	SINT/ - Enables interrupt logic; see Section 3.6
0	1	SPO1/ - Enables group 1 parallel interface ports (8255 device A20); see Section 3.4
1	0	SPO2/ - Enables group 2 parallel interface ports (8255 device A21); see Section 3.4
1	1	SS01/ - Enables serial interface chip; see Section 3.5

3.1.3 System Control Signal Propagation

These are the circuits that forward the I/O and memory read/write commands to their respective destinations.

The memory write command, MWTC/, is received by the high speed hex inverter A69-6 to become MEM W. MEM W is sent to the RAM control logic where it is used with timing control circuits to provide a write enable to the RAM. It is also combined with various conditions at the interface to produce a chip select for the bidirectional data buffer (A74 and A75) and to generate the signal RAM REQ. See Sections 3.1.1 and 3.1.2 for details.

The memory read command, MRDC/, is received by the high speed hex inverter A69-4 to become MEM R. MEM R is forwarded to the RAM output buffer via a second hex inverter. There, it gates the contents of the buffer onto the internal (SBC-104) data bus. MEM R is also combined with other interface conditions to generate either a PROM REQ/ or a chip select for A74, A75 and a RAM REQ. See Sections 3.1.1 and 3.1.2 for details.

The I/O write command, IOWC/, and I/O read command, IORC/, are received by high speed hex inverters A69-10 and A69-12. The read command is sent to the interrupt logic, parallel interface and serial interface as IOR/, following a second inversion by A68-8. The write command is latched into D-type flip-flop A19-9/8 to allow data setup time for the serial and parallel I/O interfaces. The $\overline{Q}$ side of A19-9/8 is applied to the interrupt logic, parallel interface and serial interface as IOW/.

The IOW and IOR signals are also ORed with the PROM REQ/ signal to remove a disable from the transfer acknowledge control circuit, A28. This circuit is discussed in the next section.

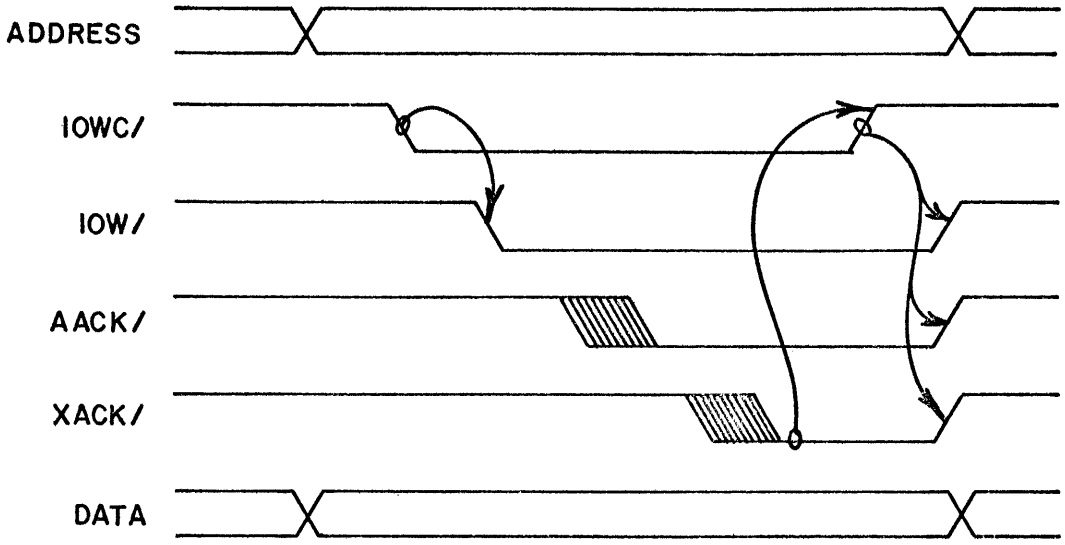
3.1.4 Transfer Acknowledge Generation

This logic provides a transfer acknowledge response, XACK/, to notify the bus master that write data provided by the bus master has been accepted or that read data it has requested is available on the system bus. XACK/ allows the bus master to conclude the current input or output instruction cycle.

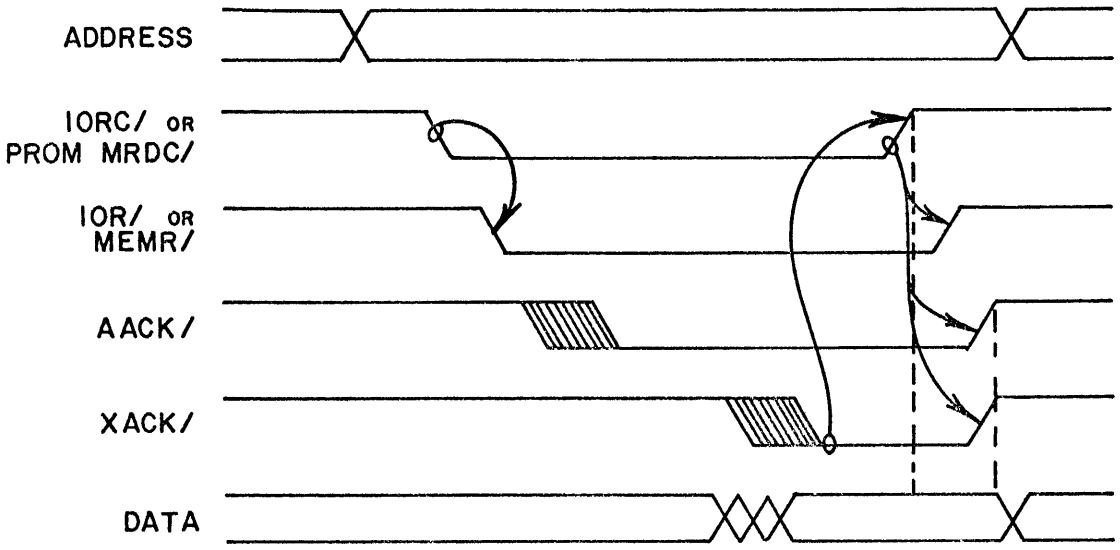
All of the logic involved in generating XACK/, except that related to RAM requests, is shown on sheet 1 of the schematics. Timing for the PROM and I/O related XACK generation is illustrated in Figure 3-1. Control logic for generating RAM transfer acknowledge signals is discussed in Section 3.2. Timing for RAM transfer acknowledge is shown in Figure 3-2.

The principal XACK control elements shown on sheet 1 consist of the timing control circuit A28 and A30-4, the XACK latch A39-9/8, NOR gate A53-10 and a set of combinational logic that enables/disables the timing control circuit and clears the XACK latch.

The final stage of the combinational logic is A52-6. A high level

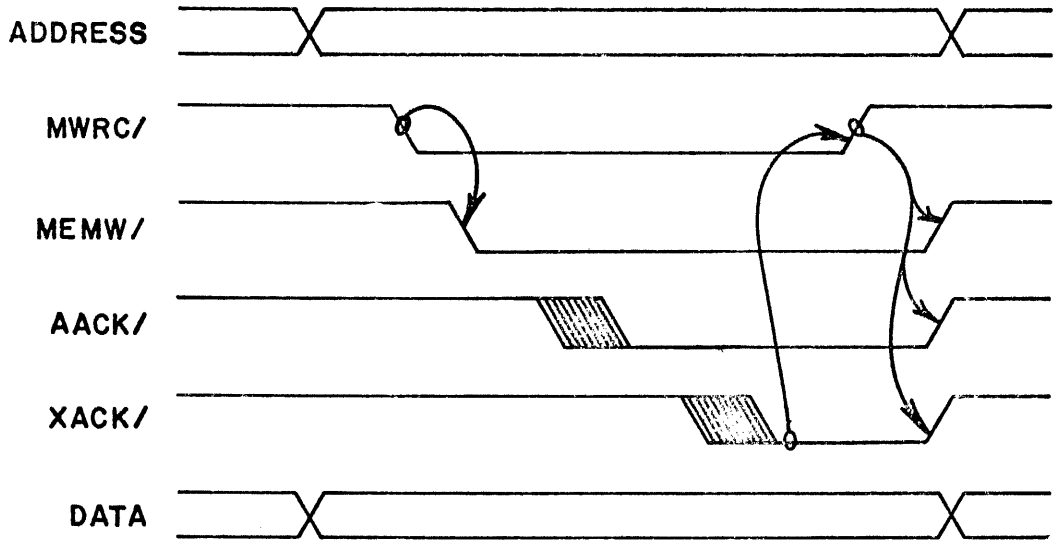


A. WRITE TO I/O PORT

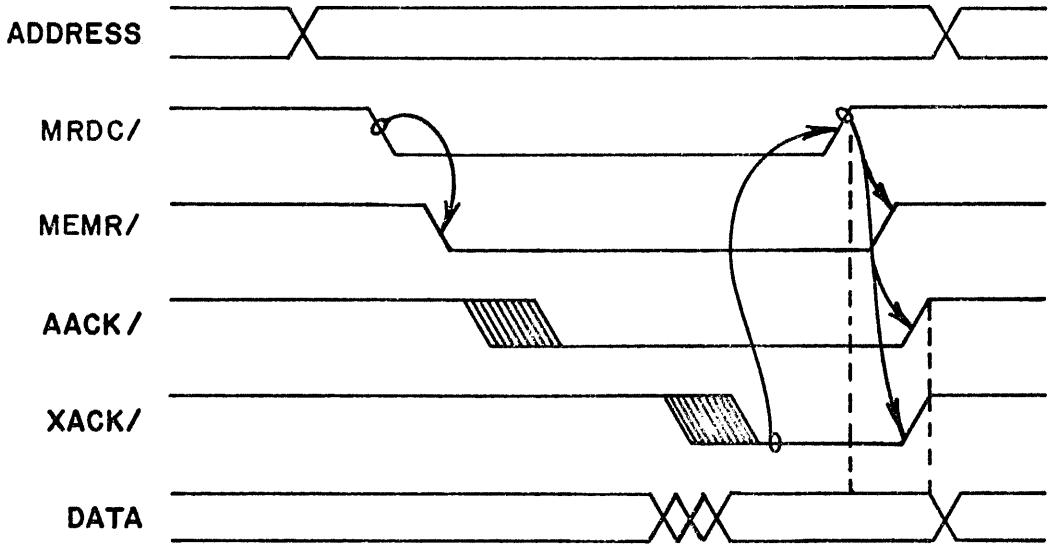


B. READ PROM OR I/O PORT

FIGURE 3-1. XACK GENERATION TIMING FOR PROM AND I/O REQUESTS



RAM WRITE



RAM READ

FIGURE 3-2. RAM TRANSFER ACKNOWLEDGE TIMING

at this point removes the clear (disable) from A28 and A39-9/8. There are three sets of conditions that produce this high level.

PROM REQ/ + (IOAD/ · IOWC/) + (IOAD/ · IORC/)

A28 is a high speed hex D flip-flop (74S174) that is wired to function as a shift register. Its purpose is to provide a delay in the generation of XACK/ to allow sufficient time for PROM or I/O port accessing. When the clear is removed, A28 is driven by the OSC/ output of the SBC-104 clock generator (described in Section 3.2). OSC/ is a 22.1184 MHz (approximately 45 ns period) square wave.

The positive edges of OSC/ cause A28 to first shift through a series of 1's and then a series of 0's. The shift register outputs are decoded in such a manner that A30-4 goes low approximately 90 ns after the first OSC/ edge following the enable. This low level arms the clock input of A39-9/8. Then, approximately 360 ns later (T + 450 ns), A30-4 goes high again, clocking the XACK latch set. Timing for this sequence is shown in Figure 3-1.

The Q side of A39-9/8 is inverted by A53-10 and driven out onto the system bus by the tri-state driver A54-11. This driver is enabled by the same gate that provides a chip select to the bidirectional data buffer A74, A75.

A39-9/8 remains set until the CPU removes MRDC/, IOWC/ or IORC/. At that point, A52-6 goes low, which resets A39-9/8 and disables A28.

Since PROM and I/O requests are not synchronous with the OSC/ clock, leading edge timing of XACK/ includes a +45 ns tolerance with respect to the read or write command.

The other input to A53-10 is supplied by RAM XAK. Its timing and

control are discussed in Section 3.2.

A28 also provides timing control for an earlier acknowledge signal, labeled AACK/ (advanced acknowledge). AACK/ can be used in some 8080-based systems, but not by the SBC-80/10, as advance notification that requested data will be valid when the bus master is ready to use it. This early acknowledge avoids a carry-over into another WAIT state, as would be required if XACK/ were used. Provision is also made for generating AACK/ in response to RAM requests. Timing for this path is determined by the RAM control logic.

3.2 RANDOM ACCESS MEMORY (RAM)

The RAM section of the SBC-104 is illustrated on sheet 3 of the schematics. It consists of eight Intel 2104 dynamic RAM memory chips, a pair of 74157 devices for multiplexing row and column address bits, an Intel 8222 refresh controller chip, an Intel 8212 chips for read data buffering, an Intel 8224 clock generator and a pair of 74S195 shift registers for timing control and various gates and flip-flops for general sequence control.

RAM transfer acknowledge (RAM XACK) circuits are included as part of the general RAM control logic.

A battery backup circuit is also provided to assure full refresh services to the RAM in the event of primary power loss. This circuit supplies auxiliary +5V, -5V and +12V power to critical circuits in the RAM section and prevents any access to the RAM except for refresh cycles.

There are three types of operations associated with the dynamic RAM elements.

1) Memory Write - In this operation, the contents of the internal data bus are written into an addressed location in the RAM array (one bit per 2104 chip) and a RAM transfer acknowledge signal is forwarded to the XACK/ circuits at the interface. Row and column address information is taken from address bits AB0 to AB5 and AB6 to ABB, respectively. These are applied to the 2104 address inputs in multiplexed fashion via devices A65 and A81. RAM control logic provides multiplex control of the row and column addresses, timing control of the 2104 chip select, write enable and address strobe inputs and timing control of the RAM transfer acknowledge signal RAM XAK.

2) Memory Read - In this operation, the contents of an addressed RAM location are loaded into the 8212 data buffer and then transferred to the bidirectional data buffer at the interface. RAM XAK is also forwarded to the XACK/ circuits at the interface. As with memory write operations, all sequences are coordinated by the RAM control logic.

3) Refresh Cycle - For this cycle, an SBC 104 performs a normal read operation (with all chips deselected) while the SBC 108 performs a "CAS before RAS" operation at a row address specified by the 8222 refresh controller. For each new refresh cycle, the row address is increased by one; 64 such cycles refresh the entire memory array. RAM control logic coordinates read/write requests with refresh requests so that competing requests are honored on a first received, first serviced basis. A timing control circuit that is part of the 8222 assures that the frequency of refresh requests is sufficient to maintain full data retention in the array.

Two of these memory operations, memory read and memory write, are initiated by the system and are referred to as system memory cycles. Details regarding these operations are presented in Section 3.2.2. Refresh cycles are discussed further in Section 3.2.3. Section 3.2.1 provides general information.

3.2.1 GENERAL RAM CONTROL

This logic coordinates memory read/write requests with refresh requests. It also provides sequence and timing control of the row/column

address multiplexing, of the 2104 control inputs (RAS, CAS, CS and WE) and of the RAM transfer acknowledge circuits.

Requests for access to the RAM array are made through the Intel 8222 refresh controller A48.

The two types of system requests, memory read and memory write, are consolidated into a single request input to the 8222. This low-true input is designated C REQ/. Requests for a refresh cycle, which are designated R REQ/, are generated by a refresh timing circuit within A48.

A third input, BUSY/, informs the refresh controller whether or not a memory cycle (system or refresh) is in progress. If BUSY/ is low (memory is busy), neither C REQ/ nor R REQ/ will be accepted.

When BUSY/ is high, the refresh controller honors the next memory request it receives. If a request is received while BUSY/ is low, the controller services that pending request after BUSY/ goes high.

The refresh controller initiates a memory control sequence in the RAM control circuits by bringing its SC/ (start cycle) output low. A second refresh controller output RO/ (refresh on) determines the nature of the memory control sequence. If RO/ is low when SC/ goes low, a refresh control sequence is executed. A high level at RO/ causes a memory read or memory write control sequence.

When a system memory cycle is specified (SC/ without RO/), two inputs from the interface logic, MEM R and MEM W, determine which type of system memory cycle is performed.

The RAM control sequence for system memory cycles is described further in the next section. Refer to Figure 3-3 for timing control information.

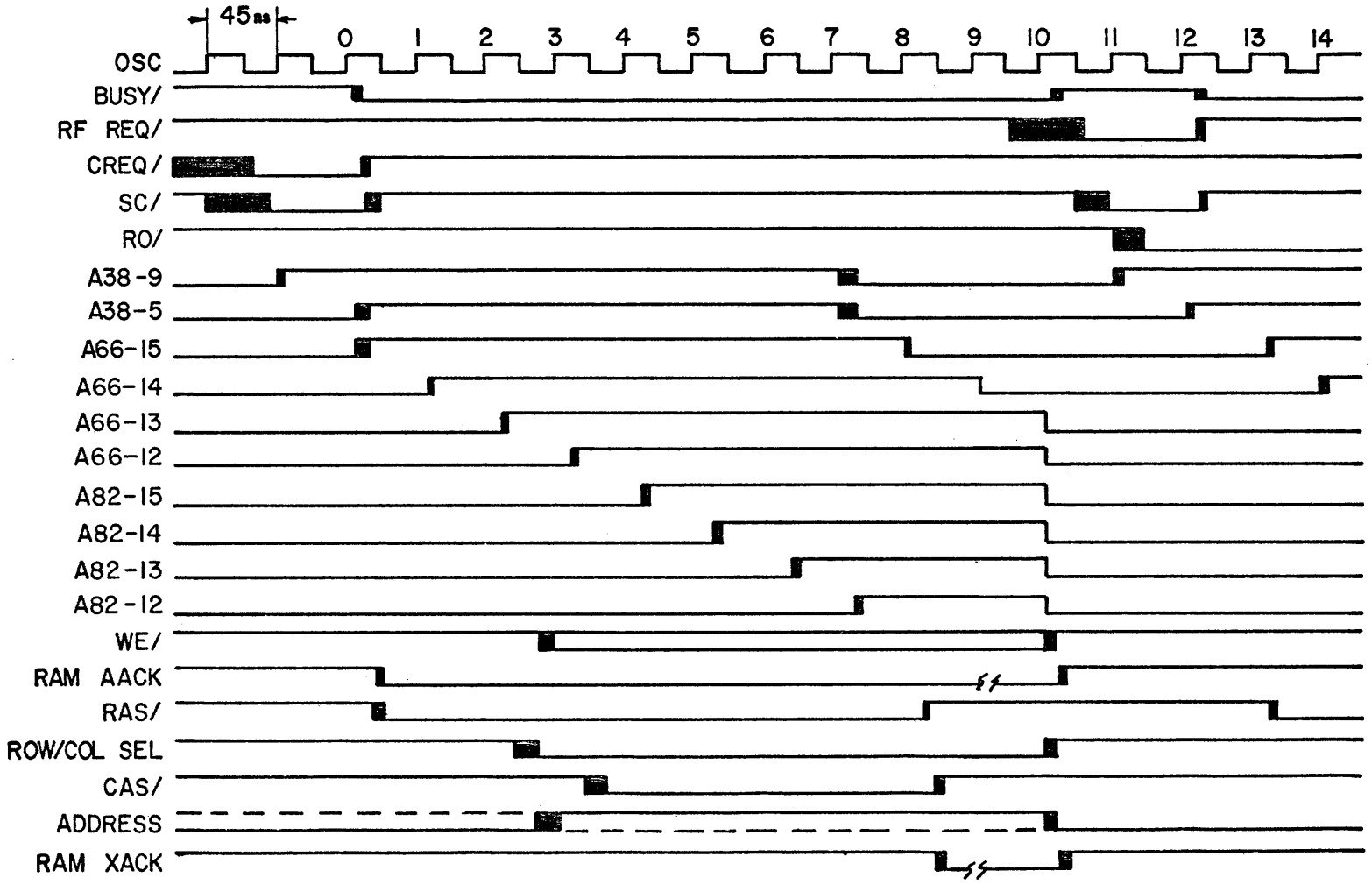


FIGURE 3-3. RAM CONTROL TIMING SUMMARY

3.2.2 SYSTEM MEMORY CYCLES (C REQ/)

A single request is made to the refresh controller for either a memory read or memory write cycle. This request, C REQ/, is made by NAND gate A51-12 as a result of successfully decoding the following three general conditions

1) The RAM REQ line from the Bus Interface must be high (true).

2) Flip-flop A67-9/8 must be reset. This condition indicates that the current RAM REQ is a new request. When it sets later in the cycle, it disables C REQ/, thereby preventing the 8222 from responding to the same RAM REQ twice.

3) The memory protect latch, A25-9/8 is in the reset state. This circuit is described in Section 3.2.4.

When these three conditions are satisfied, A51-12 applies a cycle request to the refresh controller A48. If neither the R REQ/ (refresh request) nor BUSY/ input to the refresh controller is active (low), the cycle request will be accepted and a start cycle (SC/) signal will be applied to FF1 (A38-9/8) of the RAM control logic.

FF1 will be clocked set by the next rising edge of the OSC clock. This 22.1184 MHz square wave is generated by the Intel 8224 clock generator circuit. It serves as the primary reference clock for synchronizing the various RAM control functions as well as the XACK control circuits in the interface. Other clock generator outputs are the baud clock (BD CLK) and Ø2 TTL clock, which are forwarded to the serial interface. Their uses are discussed in Section 3.5.

Since a refresh operation is not in progress at this point, the refresh controller's refresh on (RO/) output is high (false). This level allows the set state of FF1 to be propagated through gates A50-11 and A51-8 to the J and K inputs of shift register A66.

With the J and $\overline{K}$ inputs of A66 both set to 1, that device begins shifting 1's through, starting with the next positive edge of OSC. The A66 outputs then provide a sequence of transitions that are used to synchronously step the various RAM control functions through a read or write operation. One A66 output is also applied to a second shift register, A82, to extend the transition sequence. The full set of shift register outputs are referred to as OA through OH. OA corresponds to the QO output of A66 and OH corresponds to the Q3 output of A82. See Figure 3-3.

The next OSC edge after FF1 sets causes FF2 (A38-5/6) to set. FF2 brings the refresh controller's BUSY/ input low (true) via NOR gate A83-4. This in turn disables the refresh controller's SC/ (start cycle) output.

At the same time BUSY/ goes true, the OA output of A66 goes high, with the following consequences.

- The RAM array's RAS/ input goes true, which loads the row address (ABO-AB5) into the chip's internal address register. These address bits are propagated through the 8222 refresh controller because a refresh cycle is not in effect and through the row/column multiplexer (A65, A81) because the multiplexer's SEL input is high. SEL does not go low until later in the control sequence, just before CAS/ is asserted.

- The RAM AAK (Advance acknowledge) latch A67-9/8 is clocked set. Since the advanced acknowledge signal is not used in SBC-80/10 systems, this flip-flop's chief function in this case is to disable the cycle request gate, A51-12.

- One input to the CAS control gate A50-3 is satisfied. However, this gate will not provide CAS/ to the RAM array until the OD output of A66 goes high.

The OA output of A66 is also tied to a jumper set, W7, to allow its use as an alternative clock for the RAM AAK latch. It has no significance

in this application.

The OC output causes the row/column address multiplexer's SEL input to go low. This level selects the column address bits (AB6-ABB).

If the RAM REQ is for a write cycle (MEM W input is high), OC also activates the RAM array's WE (write enable) input. This strobes the contents of the SBC-104 data bus into the RAM's data in register.

Next, the OD output of A66 enables gate A50-3. As a result, the RAM array's CAS/ input goes low, which strobes the column address into the internal address register.

The OD output also provides 1's to the J and $\overline{K}$ inputs of the second shift register, A82. This causes A82 to begin contributing sequence control outputs to the operation.

If a memory read cycle has been requested, the RAM array's WE/ input will be high (false) during CAS/. This combination causes the array's data out pins to go to their high impedance states during cell access time. At the end of the period, valid data is presented at the 8212 data in pins. This timing is controlled within the 2104 .

So long as the RAM XAK latch A67-5/6 remains reset, the STB (strobe) input to the 8212 will be high and the data latch in the 8212 will reflect the contents of the data in lines. This condition changes as a result of the next event described.

The fifth positive OSC edge after CAS/ goes low causes the shift register's OA output to go low, with the following consequences.

- The RAM array's RAS/ input goes high.
- A50-3 is disabled, causing the array's CAS/ input to go high.
- A50-3 also clocks the RAM XAK latch set, which causes the 8212 STB input to go low. This latches the RAM array's out-

put data into the 8212's data latch. RAM XAK is also forwarded to the XACK/ drivers at the interface.

The 8212's tri-state output buffer is enabled by the chip's DS1/ and DS2 inputs. The low-true DS1/ condition is satisfied by MEM R, inverted. DS2 is satisfied by RAM REQ. When enabled, these drivers forward the contents of the 8212's data latch to the bidirectional data buffer at the interface.

3.2.3 REFRESH CYCLE (R REQ/)

Whenever the refresh controller's BUSY/ and C REQ/ (cycle request) inputs are not active, the controller is able to honor a refresh request.

Refresh requests are made approximately every 14 μs by a timing control circuit that is part of the 8222 device. An external RC network determines the duration of the refresh request intervals.

Each request is made by bringing the 8222's R REQ/ input low.

R REQ/ is provided by a latch in the 8222 so that if the BUSY/ input is low at the time R REQ/ is asserted, the refresh request will be maintained until it is serviced.

When the 8222 accepts R REQ/, the controller's SC/ (start cycle) output goes low, followed by the RO/ (refresh on) output. As in a read/write cycle, SC/ allows OSC to clock FF1 (A38-9/8) set. However, RO/ disables the shift register until FF2 (A38-5/6) sets one OSC cycle later. Then, the shift register begins its output sequence.

When FF2 sets, the refresh controller's BUSY/ input goes low to clear SC/ and to block any cycle request that might occur during refresh.

Next, the 8222 gates the six-bit refresh address out to the row/column address multiplexer (A65, A81) in place of system address bits AB0 - AB5).

This refresh address is supplied by a six-bit counter in the 8222 device, which is incremented by one count after each refresh cycle. The counter's output is multiplexed within the 8222 with the row address bits supplied by the system (AB0-AB5). Internal address select logic selects the system address bits during read or write and the refresh address bits during refresh cycles.

NAND gate A50-8 prevents the row/column address multiplexer from selecting its column address inputs so long as RO/ is low.

The shift register's 0A output enables the RAM array's RAS/ input and then, eight OSC cycles later, it disables RAS/.

Two clocks later, BUSY/ is held up by A26-4. The trailing edge of BUSY/ causes the 8222s RO/ output to clear, which marks the end of the refresh cycle.

The refresh timer begins a new timing cycle and, after approximately 14 µs, generates a new R REQ/.

The SBC 108 performs a special "CAS before RAS" refresh cycle. When jumper W8 is removed the normal shift register sequence is modified such that the CAS input to the memory array goes low one clock cycle before RAS. This sequence informs the RAMs that a refresh cycle is being performed.

3.2.4 MEMORY PROTECT

The memory protect feature consists of a set of auxiliary power busses, which can supply power to critical RAM and RAM control circuits when main power is lost. It also includes a flip-flop, A25-9/8, which prevents new cycle requests from being initiated once the memory protect feature is invoked.

The auxiliary power supplies, +5V, -5V and +12V, are distributed

to the appropriate RAM logic elements via separate busses from the main power. The affected logic elements are listed below.

AUX PWR SUPPLY	LOGIC ELEMENTS
+5V	A25, A26, A36, A37, A38, A48, A50, A51, A61 - A67, A77 - A83
-5V	A61 - A64, A77 - A80
+12V	A36, A61- A64, A77 - A80

Ordinarily, the auxiliary supplies are connected by solder jumpers to the corresponding main power supplies: +5V uses jumper W9; -5V uses jumper W5; +12V uses jumper W6. To implement the auxiliary supplies, these jumpers are removed, which isolates the auxiliary supplies from the main supplies.

Specifications for both main and auxiliary supplies are provided in Section 7.1.

Before power is lost, a low-true signal labeled MEMORY PROTECT must be asserted at P2-20. This signal must be generated in such a fashion that it predicts imminent loss of main power. Its low level causes A25-9/8 to reset. The true-to-false transition of BUSY/ is used as the source for the A25-9/8 clock. This synchronizes the resetting of the memory protect latch with the conclusion of a memory cycle. Memory protect must thus precede loss of power by 16 µs.

When A25-9/8 resets, its Q output disables the C REQ/ generator A51-12. No new cycle requests can be issued until MEMORY PROTECT/ goes false, allowing A25-9/8 to set again. Refresh requests are not affected.

3.3 READ ONLY MEMORY (ROM/PROM)

The SBC-104 provides sockets for installing up to 4096 × 8 bits of read only memory. Four Intel 8708 Erasable and Electrically Programmable Read Only Memory (EPROM) chips or four Intel 8308 static MOS mask read only memory (ROM) chips can be installed in the four 24 pin sockets shown on sheet 6 of the SBC-104 schematic.

In addition to the four sockets, the ROM/PROM section includes an Intel 8212 I/O port. This device receives the data read from the addressed PROM location and forwards it to the bidirectional data buffer at the interface via a set of tri-state bus drivers.

Each PROM chip is enabled by a separate chip select, PSCO/ through PCS3/. These chip selects are produced by address decode logic at the interface. When a chip select goes low, the corresponding PROM chip's output stage is enabled.

Address bit ABA is made available to jumper set W3 so that it can be used for future PROM expansion. In the standard SBC-104, pin 19 is connected to +12V to maintain the read mode.

The contents of the addressed PROM location are output to the 8212 device, A35. The STRB (strobe) input to A35 is kept high so that the PROM data is not latched in the 8212 but is simply passed on through to the device's tri-state output buffer.

The output buffer is enabled by the low-true state of PROM REQ/. See Section 3.1.2 for details regarding the generation of PROM REQ/.

3.4 PARALLEL I/O INTERFACE

The Parallel I/O Interface logic on the SBC-104 provides forty-eight (48) signal lines for the transfer and control of data to or from peripheral devices. Sixteen lines have bidirectional driver and termination networks permanently installed. The remaining thirty-two lines are uncommitted. Sockets are provided for the installation of appropriate line driver and/or termination networks for these thirty-two lines. The optional drivers and terminators are installed in groups of four by insertion into the 14-pin sockets.

All forty-eight signal lines emanate from the I/O ports on two Intel 8255 Programmable Peripheral Interface devices, as shown on sheets 4 and 5 of the SBC-104 schematic. The two 8255 devices, A20 and A21, allow for a wide variety of I/O configurations. Before describing the possible configurations, however, we will summarize the general operational characteristics of the 8255 device.

3.4.1 INTEL 8255 OPERATIONAL SUMMARY

The 8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own speical features or "personality" to further enhance the power and flexibility of the 8255.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into

two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B.

The bus master dictates the operating characteristics of the ports by outputting two different types of control words to the 8255:

1) mode definition control word (bit 7 = 1)

2) port C bit set/reset control word (bit 7 = 0)

Bit 7 of each control word specifies its format, as shown in Figures 3-4 and 3-5, respectively.

Mode Selection

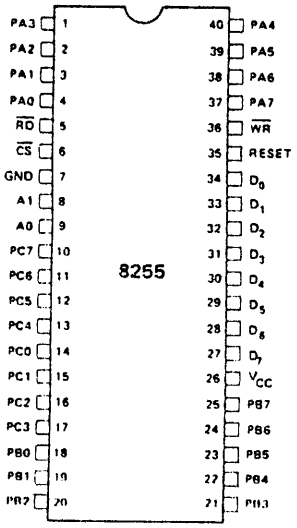
There are three basic modes of operation that can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-Directional Bus

When the RESET input goes "high" all ports will be set to the Input Mode 0 (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255 can remain in the Input mode with no additional initialization required. During the execution of the system program, the other modes may be selected using a single OUTput instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed except for $\overline{OBF}$ in

PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
Vcc	+5 VOLTS
GND	0 VOLTS

FIGURE 3-4. 8255 PIN ASSIGNMENTS:

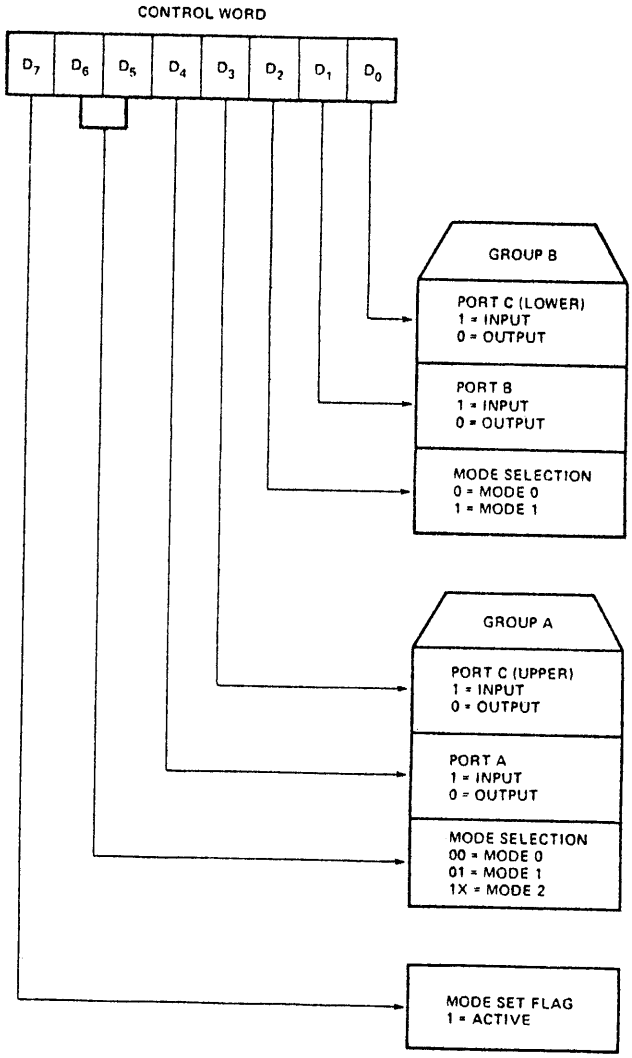


FIGURE 3-5. MODE DEFINITION CONTROL WORD FORMAT.

modes 1 and 2. Modes may be combined so that their functional definition can be tailored to almost any I/O structure. For instance, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction (see Figure 3-6). This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using a Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255 is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the bus master. The interrupt request signals, generated from Port C can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit set/reset function of Port C.

This function allows the Programmer to disallow or allow specific I/O devices to interrupt the bus master without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) - INTE is SET - Interrupt enable
(BIT-RESET) - INTE is RESET - Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

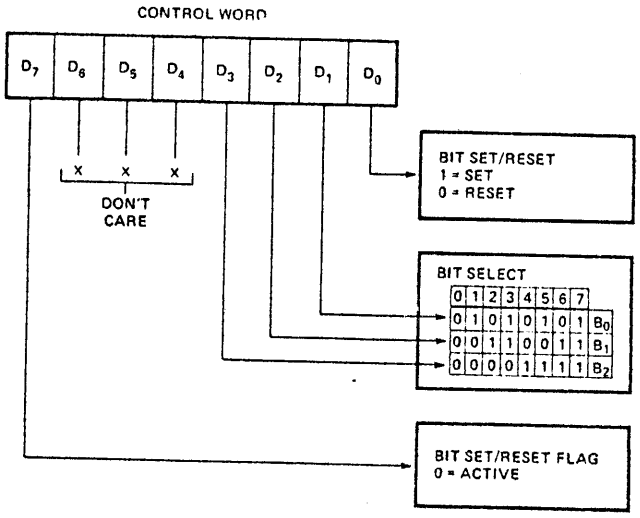


FIGURE 3-6. BIT SET/RESET CONTROL WORD FORMAT.

Operating Modes

Mode 0 (Basic Input/Output):

This functional configuration provides simple Input and Output operations for each of the three ports. No "hand-shaking" is required, data is simply written to or read from a specified port. Mode 0 timing is illustrated in Figure 3-7.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.

Sixteen different Input/Output configurations are possible in this Mode. Figure 3-8 shows two possible configurations.

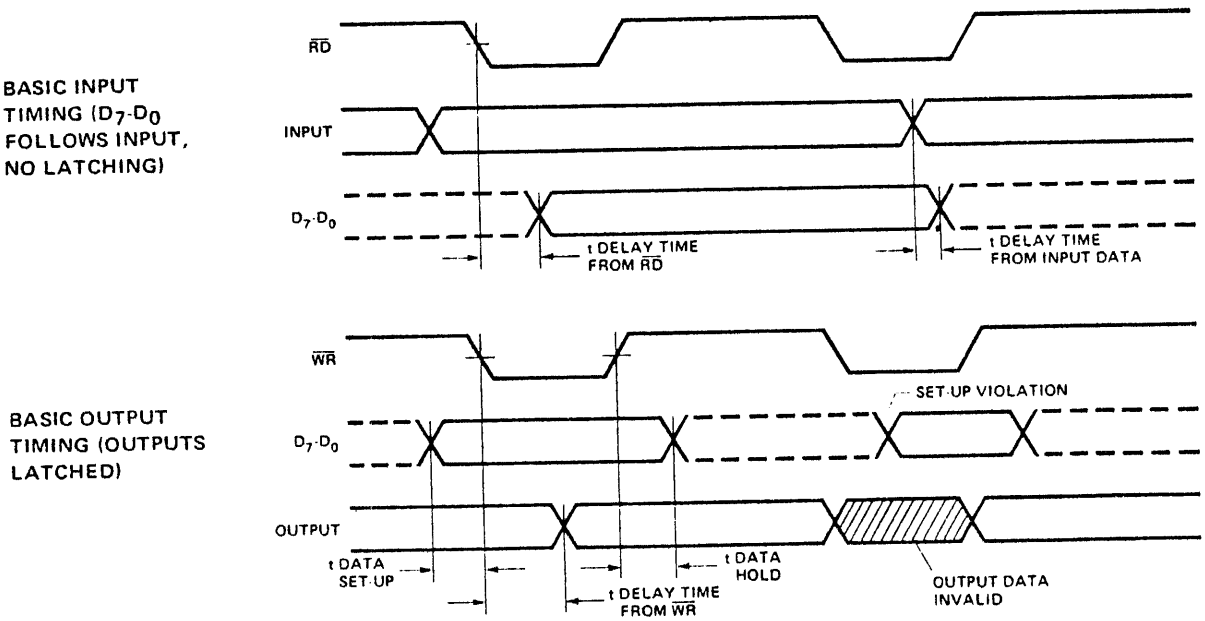


FIGURE 3-7. 8255 MODE 0 TIMING

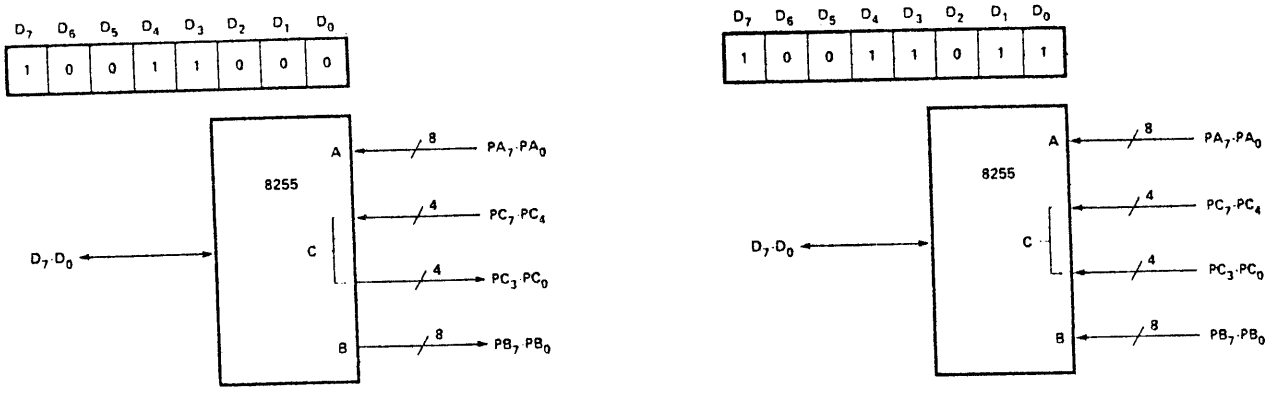


FIGURE 3-8. EXAMPLES OF MODE 0 CONFIGURATION

Mode 1 (Strobed Input/Output):

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two transfer ports (A and B).
- Each transfer port contains one 8-bit data port and 4 bits from one half of the control/data port (Port C).
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.

Input Control Signal Definition for Mode 1

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement IBF is set by the falling edge of the STB input and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the bus master when an input device is requesting service. INTR is set by the rising edge of $\overline{STB}$ if IBF is a 1 and INTE is a 1. It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the bus master by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Figure 3-9 illustrates the Mode 1 input configuration, while Figure 3-10 shows the basic timing for Mode 1 input.

Output Control Signal Definition for Mode 1

$\overline{OBF}$ (Output Buffer Full F/F)

The $\overline{OBF}$ output will go low to indicate that the bus master has written data out to the specified port. The OBF F/F will be set by the rising edge of the $\overline{WR}$ input and reset by the falling edge of the $\overline{ACK}$ input signal.

$\overline{ACK}$ (Acknowledge Input)

A low on this input informs the 8255 that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the bus master.

INTR (Interrupt Request)

A high on this output can be used to interrupt the bus master when an output device has accepted data transmitted by the bus master. INTR is set by the rising edge of $\overline{ACK}$ if $\overline{OBF}$ is a 1 and INTE is a 1. It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by bit/reset of PC6.

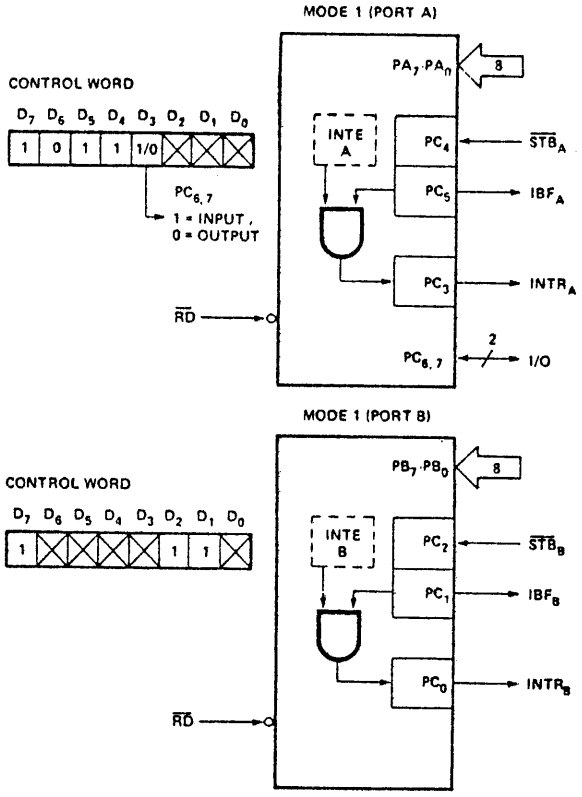


FIGURE 3-9. MODE 1 INPUT CONFIGURATION

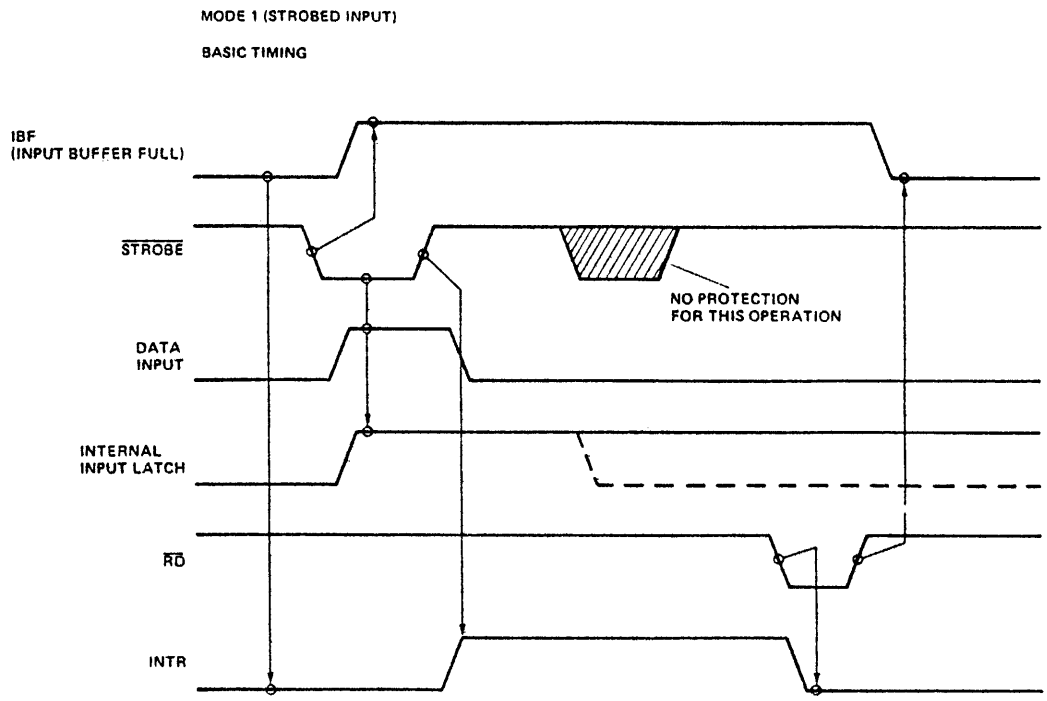


FIGURE 3-10. 8255 MODE 1 INPUT TIMING

INTE B

Controlled by bit set/reset of PC2.

Figure 3-11 illustrates the Mode 1 output configuration, while Figure 3-12 shows basic Mode 1 output timing.

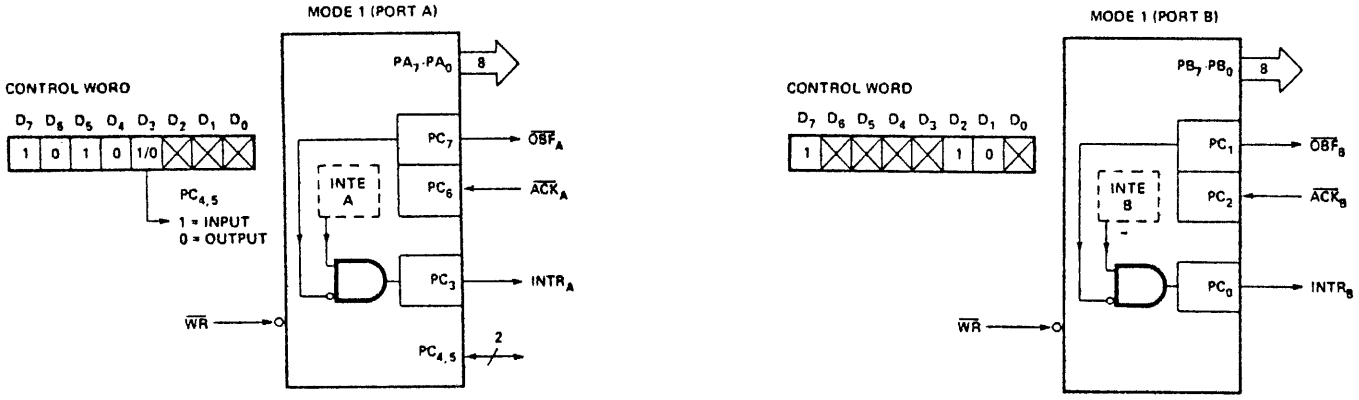


FIGURE 3-11. MODE 1 OUTPUT CONFIGURATION

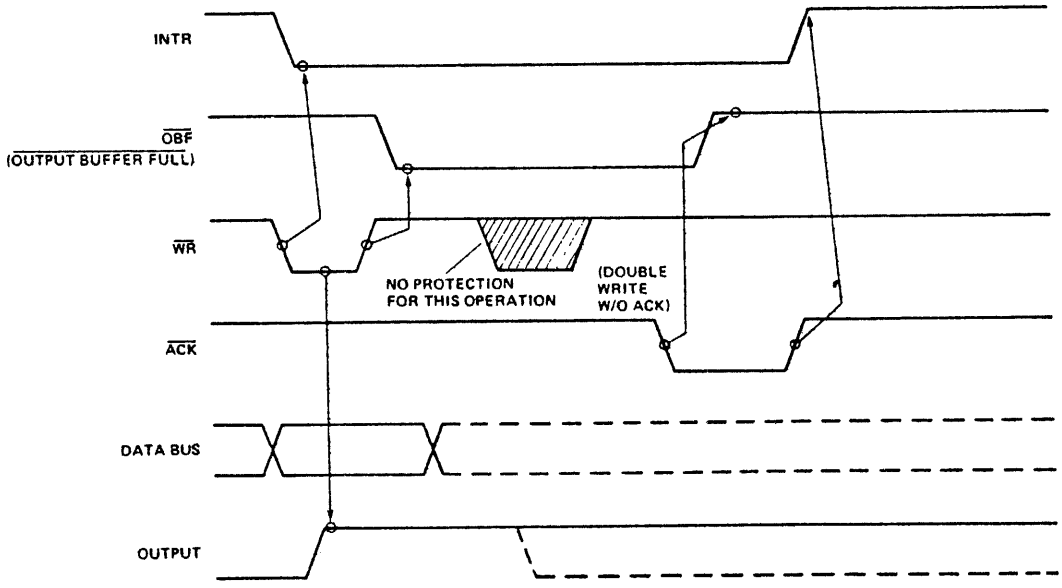


FIGURE 3-12. MODE 1 BASIC OUTPUT TIMING

Mode 2 (Strobed Bi-Directional Bus I/O):

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Port A only.
- One 8-bit, bi-directional data Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional data port (Port A).

Bi-Directional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the bus master for both input or output operations.

Output Operation Control Signals

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go low to indicate that the bus master has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A low on this input enables the tri-state output buffer of Port A to sent out the data. Otherwise, the output buffer will be in the high-impedance state.

INTR A and B (The INTE flip-flop associated with $\overline{OBF}$)

Controlled by bit set/reset of PC6 (INTE 1)

Input Operation Control Signals

$\overline{STB}$ (Strobed Input)

A low on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE flip-flop associated with IBF)

Controlled by bit set/reset PC4 (INTE 2)

$INTR_A = PC6 \cdot OBF_A + PC4 \cdot INF_A$

Figure 3-13 illustrates the port configuration for Mode 2, Figure 3-14 shows Mode 2 timing, and Table 3-1 summarizes 8255 Mode definition.

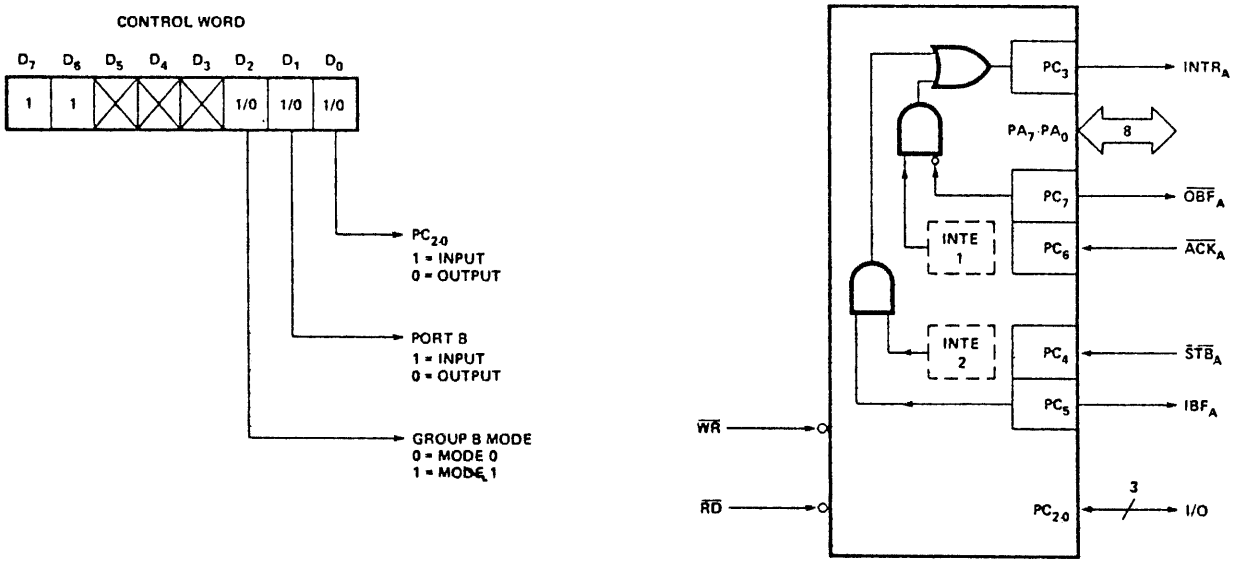


FIGURE 3-13. MODE 2 PORT CONFIGURATION

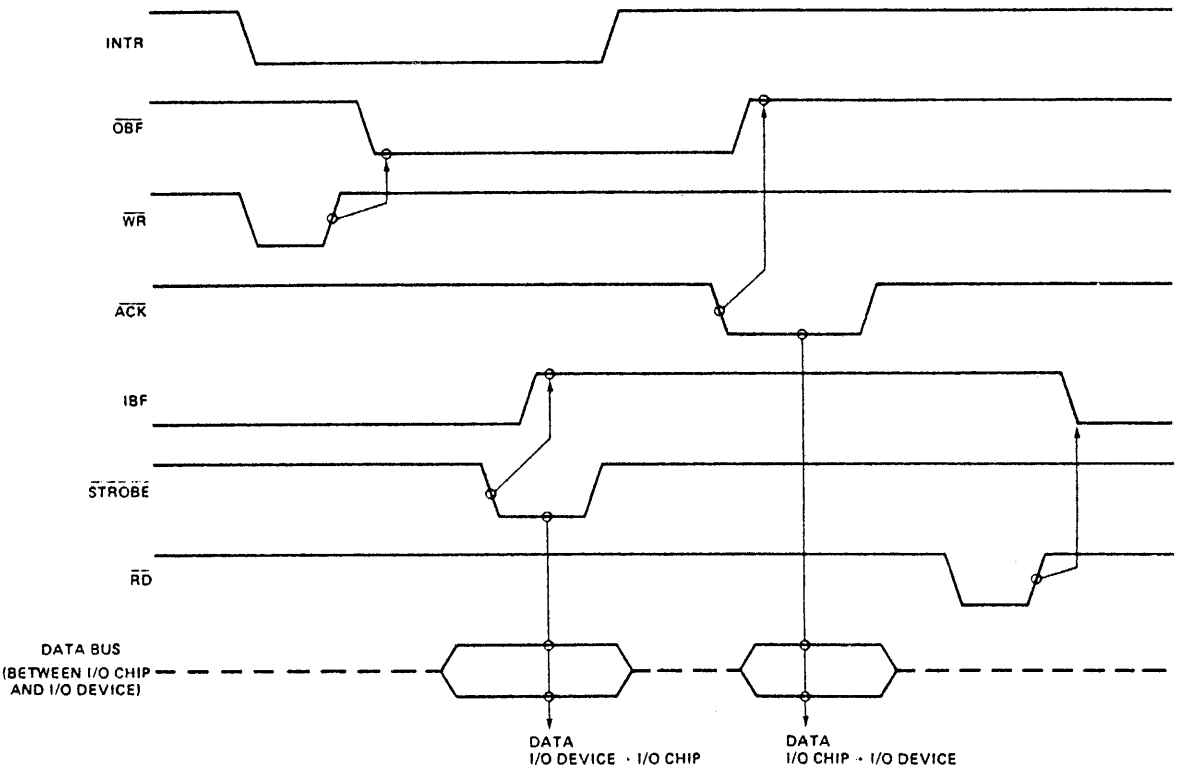


FIGURE 3-14. MODE 2 TIMING

MODE DEFINITION SUMMARY TABLE

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	⟷	
PA_1	IN	OUT	IN	OUT	⟷	
PA_2	IN	OUT	IN	OUT	⟷	
PA_3	IN	OUT	IN	OUT	⟷	
PA_4	IN	OUT	IN	OUT	⟷	
PA_5	IN	OUT	IN	OUT	⟷	
PA_6	IN	OUT	IN	OUT	⟷	
PA_7	IN	OUT	IN	OUT	⟷	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

TABLE 3-1. 8255 MODE DEFINITION SUMMARY

3.4.2 PARALLEL I/O CONFIGURATIONS

As shown on sheets 4 and 5 of the schematic, there are two 8255 devices, one loacted at A20, the other at A21. For convenience the following device designations will be used: The device at A20 is called the "group 1" device and the device at A21 is referred to as the "group 2" device. Each device has three eight-bit ports. The "group 1" ports are designated Ports 1, 2 and 3 while the "group 2" ports are designated Ports 4, 5 and 6.

The group 1 and group 2 devices both communicate with the bus master through the SBC-104 interface logic. Except for their separate select lines, they both use the same signal lines: the 8-bit data bus (DB0-DB7) and five control/address lines (IOR/, IOW/, RESET, AB0 and AB1). The two select lines are labeled SP01/ (A20) and SP02/ (A21). The data lines bring control bytes or data bytes to an 8255 or deliver data from an 8255 to the bidirectional data buffer at the interface. The chip select control signals, SP01/ and SP02/, select the group 1 and group 2 devices, respectively, when the proper I/O address appears on the system address bus. SP01/ and SP02/ are the result of decoding address bits 2 through 7 (AB2-AB7), as shown on sheet 1 of the schematic. The two least significant address bits (AB0 and AB1) select the control register (when programming an 8255) or one of the three I/O ports (when reading or writing data). IOR/ (8255 $\rightarrow$ bus master) and IOW/ (bus master $\rightarrow$ 8255) indicate the direction of data flow, as summarized in Table 3-2. Specific I/O addresses for the six ports and two 8255 control registers on the SBC-104 are listed in Table 3-3.

A high on the RESET line clears all internal 8255 registers including the control register; all ports (A, B and C) are set for input.

TABLE 3-2. BASIC 8255 OPERATION FOR EITHER GROUP 1 OR GROUP 2

A1	A0	IOR/	IOW/	CS/	Input Operation (Read)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
x	x	x	x	1	Data Bus → High-Impedance
1	1	0	1	0	Illegal

TABLE 3-3. PARALLEL I/O PORT ADDRESSES

Port	8255 Device Location	*Eight-Bit Address (Hexadecimal)	
Group 1			
1	A20 Port (A)	X4	
2	A20 Port (B)	X5	
3	A20 Port (C)	X6	
-	A20 Control	X7	For I/O write only.
Group 2			
4	A21 Port (A)	X8	
5	A21 Port (B)	X9	
6	A21 Port (C)	XA	
-	A21 Control	XB	For I/O write only.

*Notes: X is any hex digit assigned by jumper selection
Default condition = D4, D5, etc.
Group 1 select (SP01/) = xxxx01xx
Group 2 select (SP02/) = xxxx10xx

Both parallel interface groups, 1 and 2, have the same interface characteristics with respect to the system bus. They are also both capable of the same range of configurations with respect to their peripheral interfaces. The only functional difference between group 1 and group 2 is that four signal lines associated with the serial interface are made available to Port 6 (Port C of group 2) via wire wrap jumper pins. Three of the signals are RS232 inputs, which cannot be sampled by the user through the USART. They can, however, be connected by jumper to unused Port 6 bits and read through Port 6. The fourth line allows the user to drive one of the serial I/O interface output signals by setting a bit in Port 6. Details regarding the use of Port 6 by the serial interface are provided in Section 3.5, Serial I/O Interface.

The operating characteristics of each port are determined by the mode and direction control information supplied by the bus master in its control word. In addition, certain mode/port relationships impose restrictions on the use of other ports in the group. These mode-related characteristics and restrictions are discussed briefly below. Details regarding mode implementation and the associated inter-port restrictions are presented in Chapter 4, User Selectable Options.

Since the two groups are functionally identical, only one group (group 1) will be referred to in the following discussion. Statements made about group 1 ports apply equally to group 2 ports. The reader should keep in mind, however, that the peripheral interface consists of two sets of equally versatile ports, which are independently programmed.

The allowable port configurations for either group are summarized below:

Port 1 (Group 1 Port A)

Mode 0 Input
Mode 0 Output (Latched)
Mode 1 Input (Strobed)
Mode 1 Output (Latched)
Mode 2 Bidirectional

Port 2 (Group 1 Port B)

Mode 0 Input
Mode 0 Output (Latched)
Mode 1 Input (Strobed)
Mode 1 Output (Latched)

Port 3 (Group 1 Port C)

Mode 0 8 Bit Input
Mode 0 8 Bit Output (Latched)
Mode 0 Split 4 bit input and 4 bit output

Note: Control mode dependent upon Port A and B mode.

Port 1 is the most versatile of the three group 1 ports. It can be programmed to function in any one of the three 8255 operating modes. This first port is the only port in the group that already includes a permanent bidirectional driver/termination network (two 8226 bus driver devices at A1 and A2).

Before Port 1 is programmed for input or output in any one of three operating modes (as described in Section 3.4.1), certain jumper connections must be made to allow the port to function properly in the chosen mode. The 29-30-31 jumper pad specifies the direction of data flow for the two 8226 bidirectional bus drivers. If input in mode 0 or mode 1 is to be programmed for Port 1, jumper pair 29-30 should be connected. If output in mode 0 or mode 1 is to be used, jumper pair 30-31* should be connected. If Port 1 is to be programmed for bidirectional mode 2, then a wire must be run from jumper pin 37

to pin 30. This connection allows the Port 3 acknowledge output ACK/, which is available at bit 6 of Port 3, to dynamically dictate direction for the two 8226 devices.

Note: * indicates a default connection, which is the factory-selected connection. If some path other than the one provided by a default connection is selected (e.g., pins 29-30), the default wire must be removed (e.g., delete 30-31*).

When Port 1 is programmed for mode 1 or mode 2, an interrupt can be added to the Port 1 bit array by connecting jumper pins 49 and 40 (delete 40-41*). This allows the INTR output from bit 3 of Port 3 to activate the peripheral I/O interrupt request PIOA1. Refer back to Section 3.4.1 for details regarding INTR.

PIOA1 is forwarded to the interrupt logic shown on sheet 2 of the schematic.

When Port 1 is in mode 0, which has no provision for interrupts, the default connections 40-41* and 48-49* must remain to allow the use of bit 3 of Port 3 and to inhibit Port 1 interrupts.

Because the 8226 bus drivers are inverting devices, all data input to or output from Port 1 is considered to be negative true with respect to the levels at the J1 edge connector.

Port 2 can be programmed for input or output in either mode 0 or mode 1 (see Section 3.4.1). If Port 2 is to be used for input (in either mode), terminator networks must be installed in the sockets at A5 and A6. Because of the passive nature of termination networks, data that is input to Port 2 must be positive true. If Port 2 is to be used for output (in either mode), driver networks must be installed in the sockets at A5 and A6. Assuming that the drivers are inverting devices,

then the data being output will be negative true at the J1 edge connector.

When Port 2 is programmed for mode 1, a Port 2 interrupt can be implemented by connecting jumper pins 43-50 (delete 50-51*). This allows the INTR output from bit 0 of Port 3 to activate the peripheral I/O interrupt request PIOB1. PIOB1 is forwarded to the interrupt logic shown on sheet 2 of the schematic.

When Port 2 is in mode 0, the default connections 50-51* and 42-43* must remain to allow the use of bit 0 of Port 3 and to inhibit Port 2 interrupts.

As was described in Section 3.4.1, the use of Port 3 depends on the modes programmed for Ports 1 and 2. If Port 1 is in mode 1 or mode 2, bits 3, 4, 5, 6 and 7 of Port 3 can have the following dedicated control functions.

Port 3 bit 3 → INTR (interrupt request) - input or output	
Port 3 bit 4 ← STB/ (input strobe)	mode 1 input or mode 2
Port 3 bit 5 → IBF (input buffer full flag)	
Port 3 bit 6 ← ACK/ (output acknowledge)	mode 1 output or mode 2
Port 3 bit 7 → OBF/ (output buffer full flag)	

If Port 2 is in mode 1, bits 0, 1 and 2 of Port 3 have these dedicated control functions:

Port 3 bit 0 → INTR (interrupt request) - input or output	
Port 3 bit 1 → IBF (input buffer full)	input only
Port 3 bit 2 ← STB/ (input strobe)	
Port 3 bit 1 → OBF/ (output buffer full)	output only
Port 3 bit 2 ← ACK/ (output acknowledge)	

While certain Port 3 bits are available if Port 1 is in mode 1 or if Port 2 is in mode 0, the use of Port 3 as an eight-bit data path is restricted to those configurations that have both Port 1 and Port 2

programmed for mode 0. In this case all 8 bits of Port 3 can be programmed for mode 0 input (termination networks must be installed in the sockets at A3 and A4) or output (driver networks must be installed at A3 and A4) or split 4 bits input and 4 bits output.

Note: If Port 1 and 2 are not both in mode 0, then a driver network must be installed in the sockets at A3 and a termination network must be installed at A4, so that the Port 3 control lines can function properly.

3.5 SERIAL I/O INTERFACE

The Serial I/O Interface logic provides a serial data communications channel that can be programmed to operate with most of the current serial data transmission protocols, synchronous or asynchronous. Baud rate, character length, number of stop bits and even/odd parity are program selectable.

The Serial I/O Interface logic consists primarily of an Intel 8251 USART device, a counting network for baud rate selection, and RS-232C interface circuitry, as shown on sheet 6 of the schematic. Before describing the specific operation of the Serial I/O logic however, we will summarize the general operational characteristics of the 8251 USART, because it essentially defines the character of the Serial I/O Interface.

3.5.1 INTEL 8251 OPERATIONAL SUMMARY

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 8080 Micro-computer System. Like other I/O devices in the 8080 Micro-computer System its functional

configuration is programmed by the systems software for maximum flexibility. The 8251 can support virtually any serial data technique currently in use (including IBM "Bi-Sync").

Modem Control

The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{\text{DSR}}$ (Data Set Ready)

The $\overline{\text{DSR}}$ input signal is general purpose in nature. Its condition can be tested by the bus master using a Status Read operation (as described later). The $\overline{\text{DSR}}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{\text{DTR}}$ (Data Terminal Ready)

The $\overline{\text{DTR}}$ output signal is general purpose in nature. It can be set low by programming the appropriate bit in the Command Instruction word. The $\overline{\text{DTR}}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

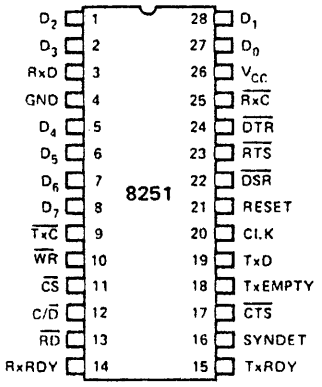
$\overline{\text{RTS}}$ (Request to Send)

The $\overline{\text{RTS}}$ output signal is general purpose in nature. It can be set low by programming the appropriate bit in the Command Instruction word. The $\overline{\text{RTS}}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A low on this input enables the 8251 to transmit data (serial) if the TxEN bit in the Command byte is set to a 1.

USART
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

FIGURE 3-15. 8251 PIN ASSIGNMENTS

$\overline{TXRDY}$ (Transmitter Ready)

This output signals the bus master that the transmitter is ready to accept a data character. It can be used as an interrupt to the system or for polled operation when the bus master can check TXRDY using a status read operation. $\overline{TXRDY}$ is active only when $\overline{CTS}$ is enabled. $\overline{TXRDY}$ is automatically reset when a character is loaded from the bus master.

TXE (Transmitter Empty)

When the 8251 has no characters to transmit, the TxE output will go high. It resets automatically upon receiving a character from the bus master. TxE can be used to indicate the end of a transmission mode, so that the bus master knows when to turn the line around in the half-duplex operational mode.

In SYNChronous mode, a high on this output indicates that a character has not been loaded and the SYNC character or characters are about to be transmitted automatically as fillers.

$\overline{\text{TXC}}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the frequency of $\overline{\text{TXC}}$ is equal to the actual Baud Rate (1X). In Asynchronous transmission mode, the frequency of $\overline{\text{TXC}}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1X, 16X, or 64X the Baud Rate.

For Example:

If Baud Rate equals 4800 Baud,

$\overline{\text{TXC}}$ equals 4800 Hz (1X)

$\overline{\text{TXC}}$ equals 76.80 kHz (16X)

$\overline{\text{TXC}}$ equals 307.2 kHz (64X).

The falling edge of $\overline{\text{TXC}}$ shifts the serial data out of the 8251.

RXRDY (Receiver Ready)

This output indicates that the 8251 contains a character that is ready to be input to the bus master. RXRDY can be connected to the interrupt structure of the bus master or for polled operation the bus master can check the condition of RXRDY using a status read operation. RXRDY is automatically reset when the character is read by the bus master.

$\overline{RXC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the frequency of $\overline{RXC}$ is equal to the actual Baud Rate (1X). In Asynchronous Mode, the frequency of $\overline{RXC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1X, 16X or 64X the Baud Rate.

For Example:

If Baud Rate equals 300 Baud,

$\overline{RXC}$ equals 300 Hx (1X)

$\overline{RXC}$ equals 4800 Hz (16X)

$\overline{RXC}$ equals 19.2 kHz (16X).

If Baud Rate equals 2400 Baud,

$\overline{RXC}$ equals 2400 Hz (1X)

$\overline{RXC}$ equals 38.4 kHz (16X)

$\overline{RXC}$ equals 153.6 kHz (64X).

Data is sampled into the 8251 on the rising edge of $\overline{RXC}$.

Note: In most communications systems, the 8251 will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the Same. Both $\overline{TXC}$ and $\overline{RXC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)

This pin is used in SYNCHronous Mode only. It is used as either input or output, programmable through the Control Word. It is reset to low upon RESET. When used as an output (internal Synch mode), the

SYNDET pin will go "high" to indicate that the 8251 has located the SYNC character in the Receive mode. If the 8251 is programmed to use double Sync characters, then SYNDET will go high in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input, (external SYNC detect mode), a positive going signal will cause the 8251 to start assembling data characters on the falling edge of the next $\overline{RXC}$. Once in SYNC, the high input signal can be removed. The duration of the high signal should be at least equal to the period of $\overline{RXC}$.

Programming the 8251

Prior to starting data transmission or reception, the 8251 must be loaded with a set of control words generated by the bus master. These control signals define the complete functional definition of the 8251 and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction,
2. Command Instruction.

Both the Mode and Command instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251 for data communication.

All control words written into the 8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251 at any time in the data block during the operation of the 8251. To return to the Mode Instruction format a

bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters (see Figure 3-16).

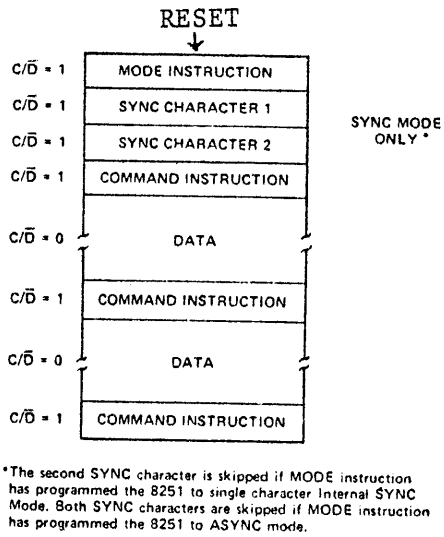


FIGURE 3-16. TYPICAL 8251 DATA BLOCK

Mode Instruction:

This format defines the general operational characteristics of the 8251. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the 8251 by the bus master, SYNC characters or Command instructions may be inserted.

The 8251 can be used for either synchronous or asynchronous data communications. The two least significant bits of the Mode Instruction control word specify synchronous or asynchronous operation. The format for the remaining bits in the control word depends on the mode chosen by bits 0 and 1. Figure 3-17 shows the control word format

for the asynchronous mode, while Figure 3-18 illustrates the control word format for the synchronous mode.

Command Instruction:

Once the functional definition of the 8251 has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode instruction has been written into the 8251 and Sync characters inserted, if necessary, then all further control writes ($C/\overline{D}$ = 1) will load the Command Instruction. A Reset operation (internal or external) will return the 8251 to the Mode Instruction Format.

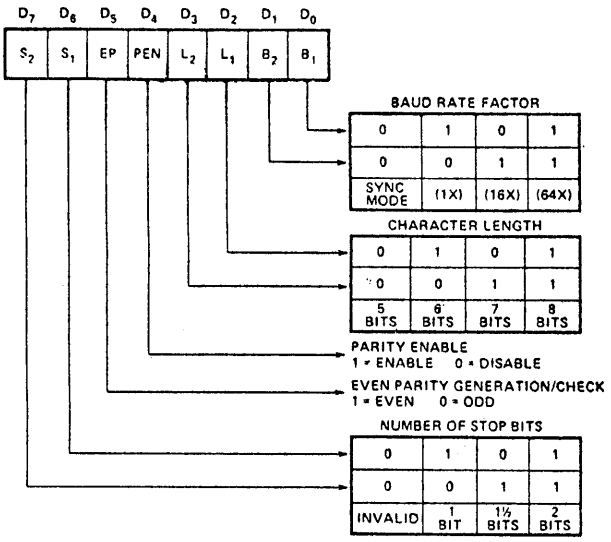
Figure 3-19 illustrates the format of a Command Instruction control word.

Status Read Definition

In data communication systems it is often necessary to examine the status of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251 has facilities that allow the programmer to read the status of the device at any time during the functional operation.

A normal read command is issued by the CPU with the $C/\overline{D}$ input at 1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings



Mode Instruction Format, Asynchronous Mode

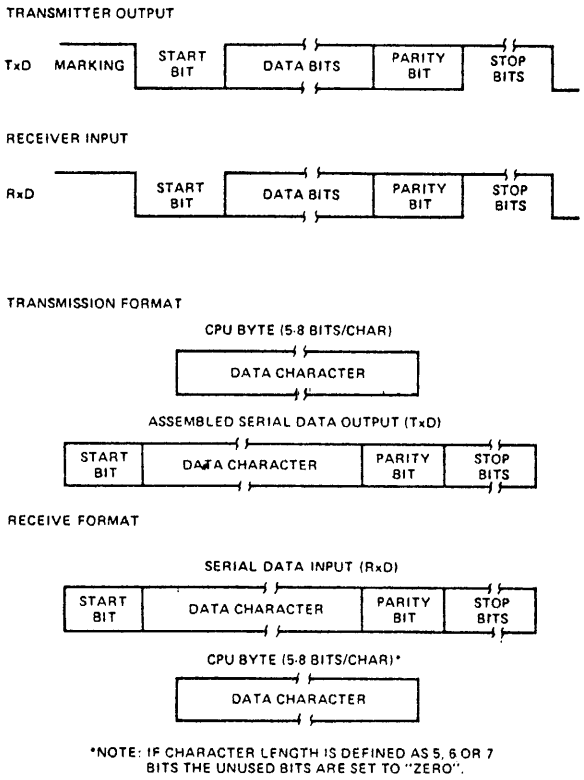
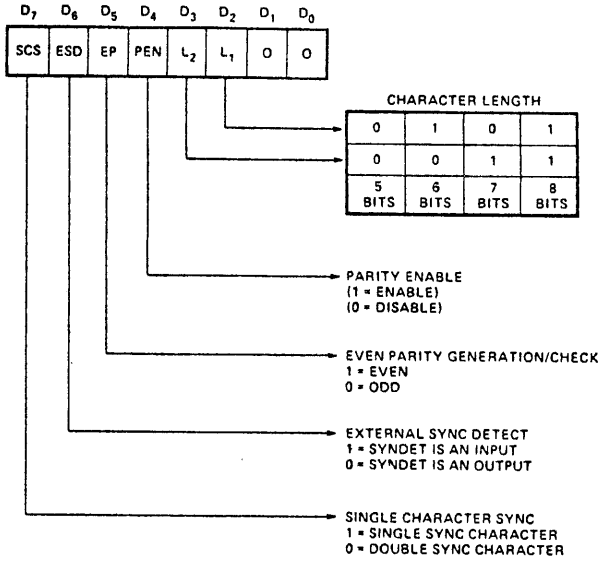


FIGURE 3-17. ASYNCHRONOUS MODE.



Mode Instruction Format, Synchronous Mode

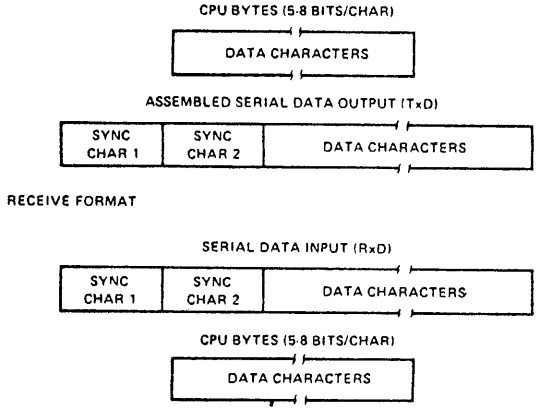


FIGURE 3-18. SYNCHRONOUS MODE.

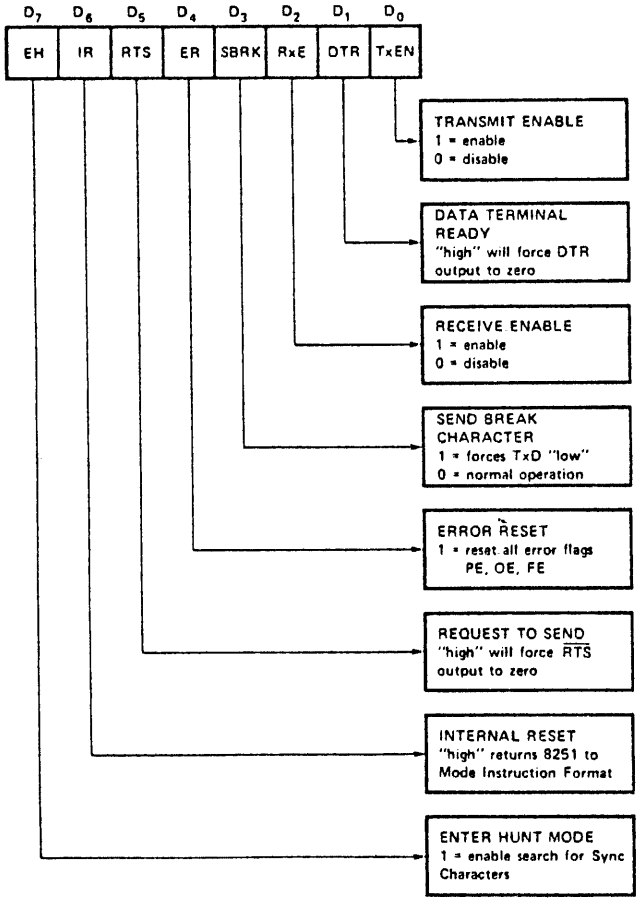


FIGURE 3-19. COMMAND INSTRUCTION FORMAT

to external output pins so that the 8251 can be used in a completely Polled environment or in an interrupt driven environment (refer to Figure 3-20).

8251 DATA TRANSFERS

Once programmed, the 8251 is ready to perform its communcation functions. The TXRDY output is raised "high" to signal the bus master that

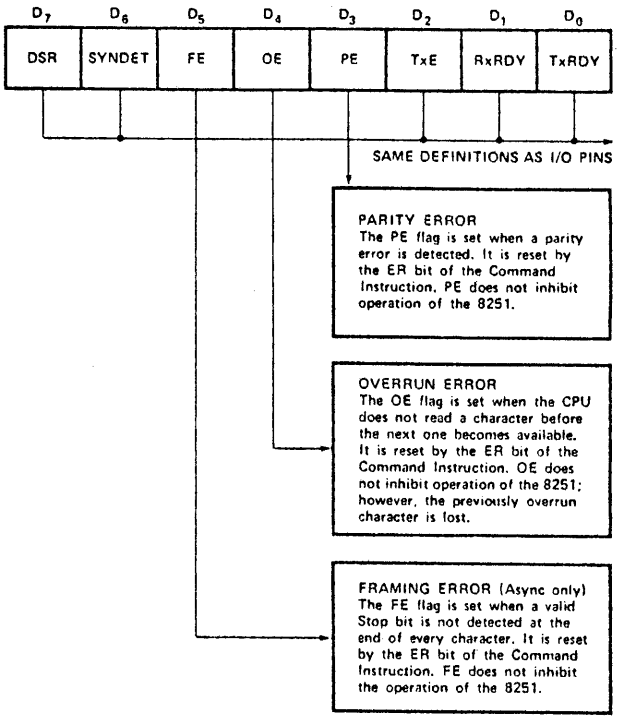


FIGURE 3-20. STATUS READ FORMAT

the 8251 is ready to receive a character. This output (TXRDY) is reset automatically when the bus master writes a character into the 8251. On the other hand, the 8251 receives serial data from the MODEM or I/O device; upon receiving an entire character the RXRDY output is raised high to signal the bus master that the 8251 has a complete character ready for the bus master to fetch. RXRDY is reset automatically upon the bus master read operation.

The 8251 cannot begin transmission until the TXEN (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send (CTS) input. The TXD output will be held in the marking state upon Reset.

Asynchronous Mode (Transmission):

Whenever a data character is sent by the bus master the 8251 automatically adds a Start bit (low level) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TXD output. The serial data is shifted out on the falling edge of $\overline{TXC}$ at a rate equal to 1/16 or 1/64 that of the $\overline{TXC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TXD if commanded to do so.

When no data characters have been loaded into the 8251 the TXD output remains high (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive):

The TXD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center. If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RXD pin with the rising edge of $\overline{RXC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. This character is then loaded into the parallel I/O buffer of the 8251. The RXRDY pin is raised to signal the CPU that a character is ready to be fetched.

If a previous character has not been fetched by the bus master, the present character replaces it in the I/O buffer, and the OVERRUN flag is raised (thus the previous character is lost). All of the error flags can be reset by a command instruction. The occurrence of any of these errors will not stop the operation of the 8251.

Synchronous Mode (Transmission):

The TXD output is continuously high until the bus master sends its first character to the 8251 which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TXC}$. Data is shifted out at the same rate as the $\overline{TXC}$.

Once transmission has started, the data stream at $\overline{TXD}$ output must continue at the $\overline{TXC}$ rate. If the bus master does not provide the 8251 with a character before the 8251 becomes empty, the SYNC characters (or character if in single SYNC word mode) will be automatically inserted in the TXC data stream. In this case, the TXEMPTY pin will momentarily go high to signal that the 8251 is empty and sync characters are being sent out. The TXEMPTY pin is internally reset by the next character being written into the 8251.

Synchronous Mode (Receive):

In this mode, character synchronization can be internally or externally achieved. If the internal SYNC mode has been programmed, the receiver starts in a HUNT mode. Data on the RXD pin is then sampled in on the rising edge of RXC. The content of the RX buffer is continuously compared with the first SYNC character until a match

occurs. If the 8251 has been programmed for two SYNC characters, the subsequent received character is also compared. When both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin. The high level can be removed after one $\overline{RXC}$ cycle. (The SBC-104 does not provide the capability to exercise this line.)

Parity error and overrun error are both checked in the same way as in the Asynchronous receive mode.

The bus master can command the receiver to enter the HUNT mode if synchronization is lost.

3.5.2 SERIAL I/O CONFIGURATIONS

The 8251 USART presents a parallel, eight-bit interface to the SBC-104 data bus (DB0-DB7) and presents a EIA RS232C interface to an external device (via edge connector J3). The 8251's interface with the data bus is enabled by a low level on its chip select (CS/) pin, which is controlled by the signal SS01/. This signal is generated by address decode logic in the SBC-104 interface as the result of the decoding system address bits 2 through 7. Bits 2 and 3 must both be active (set) to select the USART. The address value specified by bits 4 through 7 is jumper selected. The least significant bit, AB0, is applied to the 8251's C/$\overline{D}$ input to indicate a control (if set) or data (if reset) byte on the data bus. Table 3-4 summarizes the serial I/O Interface address characteristics.

TABLE 3-4. SERIAL COMMUNICATION (8251) ADDRESS ASSIGNMENTS

I/O ADDRESS (Base 16)	COMMAND	DIRECTION	FUNCTION
XD or XF	IOW/	CPU → USART	Write Control Word
XC or XE	IOW/	CPU → USART	Write Data
XD or XF	IOR/	USART → CPU	Read Status
XC or XE	IOR/	USART → CPU	Read Data

X = any hex digit; assigned by jumper selection.

An output instruction (IOW/ is true) to port XD or XF (CS/ is low and AB0 is high) causes the 8251 to accept a control byte through its data bus pins. The control byte can be either a mode instruction or a command instruction, depending on the sequence in which it is sent. The various bits in the mode control word specify the baud rate multiplexer, character length, parity and the number of stop bits as described in Section 3.5.1. Note that the actual baud rate selected is dependent on the configuration of the baud rate jumper network (refer to Section 3.5.3). The various bits in the command control word instruct the USART to enable/disable the receiver and transmitter, to reset errors, to reset internal control and return to the mode control cycle, and to set/clear the Data Terminal Ready output.

An output instruction to port XC or XE (CS/ and AB0 are low) causes the 8251 USART to accept a data byte through its data bus pins. Bit 0 is the least significant bit and bit 7 is the most significant bit. The 8251 will subsequently transmit the data byte (if the transmitter is enabled), in serial fashion, to the external device

as described in Section 3.5.1.

An input instruction (IOR/ is true) to port XD or XF (CS/ is low and AB0 is high) causes the 8251 USART to place a status byte onto the system bus. The status bits are the result of status and error checking functions performed within the USART (see Section 3.5.1).

An input instruction (IOR/ is true) to port XC or XE (CS/ and AB0 are low) causes the USART to output a data byte (previously received from the external device) from its data bus pins. Bit 0 is the least significant bit and bit 7 is the most significant bit.

Timing for the USART's internal function is provided by the ∅2 TTL signal, which is supplied by the 8224 clock generator (see sheet 3 of the schematic).

The USART is reset by the occurrence of a high level on the RESET line.

The 8251 USART transmits and receives serial data, synchronously or asynchronously, as described in Section 3.5.1.

3.5.3 BAUD RATE CLOCK GENERATION

The baud rate clock network consists of two 74161 divide-by-16 counters and a set of wire wrap jumper pins for baud rate clock selection. The two counters are driven by the 1.2288 MHz square wave labeled BD CLK. This clock is supplied by the SBC-104 clock generator's ∅2 TTL output (2.4576 MHz) via a divide-by-two circuit.

The outputs from the two 74161 counters, each providing a different clock frequency, are tied to jumper pins that can be connected

to the USART's TXC and/or RXC inputs. The available frequencies are listed in Table 4-9. When selecting the appropriate baud rate, the state of the 8251's internal frequency divider must be considered. The 8251 is capable of dividing the baud rate clock input by 1, 16 or 64.

To provide a 110 baud rate, the count cycle of the second counter, A17, must be modified. This is done by connecting jumper pins 1 and 2, which completes a path from A17's carry output to its LOAD input. This makes 110 baud available at jumper pin 9.

A third 74161 counter, A27, is included in this chain to generate the 1 ms timing required by the interval timer interrupt circuit shown on sheet 2 of the schematic.

This counter is driven by BD CLK and is enabled by the carry output of A17. It outputs high-true pulses to flip-flop A19-5/6 at approximately 1 ms intervals via the CLK INT line.

If the 110 baud rate is selected (jumper pins 1 and 2 are connected), the parallel load inputs of A27 must be changed to maintain the 1 ms periods. To do this, the existing jumper at 3-4* is deleted and jumper pins 3 and 5 are connected.

3.5.4 SERIAL I/O INTERRUPTS

The Serial I/O logic can be configured by jumper connections to provide one or two interrupts.

One interrupt, SIOR1, can be generated by the 8251's receiver ready (RXR) output. By connecting jumper pins 84-85*, SIOR1 will go high whenever the receiver enable bit of the command word has been

set and the 8251 contains a character that is ready to be input to the bus master. This interrupt line is disabled by connecting jumper pins 83-84.

The user can also elect to have either the transmitter ready (TXR) or transmitter empty (TXE) output of the 8251 activate the other interrupt, SIOT1. If jumper pair 79-81* is connected, SIOT1 will go high when the 8251 is ready to accept a character from the bus master (TXR is high). If jumper pair 79-80 is connected, SIOT1 will go high when the 8251 has no characters to transmit. In either case, the transmit enable bit of the command word must be set.

To disable the SIOT1 line, jumper pair 79-82 must be connected.

3.5.5 RS232 INTERFACE FEATURES

The input and output paths between the 8251 and the RS232 interface at J3 contain a number of selectable features that the user needs to consider when implementing the interface. Each of these features is briefly described below.

- Capacitors - Each output line and the RECEIVE DATA input line includes a provision for installing a capacitor to ground. This allows the user to modify the rise time on any of these signals by installing custom-selected capacitors, where needed.

- Handshaking Signal Jumpers - The signal paths for the four handshaking signals, DATA TERMINAL READY, DATA SET READY, REQUEST TO SEND and CLEAR TO SEND; include jumper pins so that the paths can be configured to present any one of six types of interfaces to the RS232 cable. Three of the configurations apply when the 8251 is operating in the data terminal role and the other three apply when it is operating as a data set. In general, these configurations provide for a standard interface, where each side of the

interface (terminal and data set) participates actively in the handshaking task, or an optional interface, where the handshaking response signal is produced passively by looping the initial signal back as its own response. For example, if the 8251 is operating in the data terminal role, but the RS232 circuit does not provide a DATA SET READY response to DATA TERMINAL READY, the 8251's DSR/ pin can be connected to the DATA TERMINAL READY line instead of to the DATA SET READY line. This will provide a DSR/ input automatically whenever DATA TERMINAL READY is activated. This configuration is selected by connecting jumper pins 15-16* and 16-18. The default jumper at 17-18* must be removed. All of the possible configurations for these paths and the jumper connections required to implement them are presented in Section 4.2.

- DTE TRANSMIT Clock Jumper - The selected baud rate clock (8251 TXC input) can be output on the DTE TRANSMIT CLOCK line by connecting jumper pins 13-14* and 23-24.* If this configuration is selected, the STXD option described next cannot be used.

- SEC TRANSMIT DATA Jumper - The SEC TRANSMIT DATA and SEC REQUEST TO SEND lines, which are permanently connected on board, can be controlled through one of the bits in Port 6 of the peripheral interface (A21). To implement this feature jumper pins 23-25 and 12-13 must be connected and pin 76 (shown on sheet 5 of the schematic) must be connected to the appropriate Port 6 jumper pin (56, 58, 60, 62, 64, 66, 68 or 70). The user can then activate the SEC TRANSMIT DATA line by setting the selected Port 6 bit. See Section 3.4 for details regarding the use of Port 6. If this feature is implemented, the DTE TRANSMIT CLOCK path cannot be used.

- Reading RS232 Inputs via Port 6 - Three RS232 input signals, CARRIER DETECT, RING INDICATOR and SEC CLEAR TO SEND/SEC RECEIVED DATA can be connected to otherwise unused Port 6 bits so that they can be read by the user through that port. These inputs are available to Port 6 from the following jumper pins (see Sheet 5 of the schematic)

  CARRIER DETECT - Pin 75

  RING INDICATOR - Pin 78

  SEC CLEAR TO SEND/SEC RECEIVED DATA - Pin 77

All RS232 input and output paths include on-board level translator circuits.

3.6 INTERRUPT STATUS/MASK REGISTERS

This section consists of an Intel 8212 Eight-Bit Input/Output Port (A33), a set of interrupt mask gates (A44, A45), a multiplexed status/mask input multiplexers (A58, A59), a 74148 priority encoder (A32), a set of 7407 bus drivers and an interval timer interrupt latch (A19-5/6). These functional elements are shown on sheet 2 of the schematic.

There are four types of operations that involve the interrupt circuits: write status mask into the mask register, read status mask, read masked interrupt status and reset interval timer interrupt latch. This last operation is performed as a write.

In each operation, the interrupt select line SINT/ must be true (low). This select line is generated by I/O address decode logic in the interface.

The system address assignments for each of these operations are shown below.

Function	Address AB0-AB7	R/W Command
Write Interrupt Mask	X1	IOW/
Read Mask (Inverted)	X1	IOR/
Read Masked Status	X0	IOR/
Reset Interval Timer	X2*	IOW/

*Note: Interval timer can also be reset at same time mask register is loaded by using X3.

When SINT/ and IOW/ are both low and AB1 is high, the contents of the data bus are written into the interrupt mask register A33. The output bits of A33, which always reflect the register's contents, are applied to the interrupt mask gates.

Both the inputs and outputs of A33 are high-true. A mask bit must be set to 1 to enable the corresponding interrupt status bit.

Eight interrupt lines are NANDed with the mask register outputs at gates A44 and A45. For those mask bits that are set, the corresponding interrupt path is enabled.

Seven of the interrupt lines are controlled by fixed sources. Two are from parallel I/O interface group 1 (PIOA1 and PIOB1), two are from parallel I/O interface group 2 (PIOA2 and PIOB2), two are from the serial I/O interface (SIOR1 and SIOT1) and one is provided via J2-50 by a user-selected external source (EXTERNAL INTERRUPT 2).

The eighth interrupt can be supplied by another external source (via J1-50) or by the interval timer interrupt circuit. This choice is made by the user by jumper selection. The interval timer latch is selected by a jumper at pins 27-28*, which is the default mode. The external source is selected as the source by a jumper at pins 26-27.

The interval timer latch (A19-5/6) is clocked set at 1 ms intervals. It must then be reset by a write to X2, where X is the jumper selected I/O address.

The low true output of the interrupt mask gates is routed to the following three destinations.

1) It is applied to the A inputs of the status/mask multiplexer A58, A59. These masked interrupt bits can then be read by the bus master via the bidirectional data buffer at the interface. The interrupt status bits are inverted at the multiplexer so that they are high true on the SBC-104 data bus.

2) The masked interrupt bits are logically ORed at A32. The INRQ/ output of this device is low (true) whenever any one of the interrupt bits is low (true). INRQ/ is connected to one of the interrupt pins (INT 0/ - INT 7/) at P1. This connection is made by wire wrap jumper at the user's discretion. The INRQ/ default connection is at INT 1/ (103-111*).

3) The masked interrupt bits are also made available to the P1 interrupt pins via jumper connections. This provides maximum freedom in establishing a priority handling scheme.

The interrupt mask bits are also applied to the status/mask multiplexer. They can be read in inverted form via the bidirectional data buffer at the interface.

Note: The mask bits are inverted at the multiplexer so that they are low true on the SBC-104 data bus.

The interrupt request ORing circuit (priority encoder A32) is disabled whenever the mask register is being written into or the interval timer is being reset. These two conditions are represented by SINT/ and IOW/ both being low. This causes a low to high transition of the INRQ/line to provide the edge required by edge triggered devices.

CHAPTER 4

USER SELECTABLE OPTIONS

The SBC-104 provides the user with a powerful, and flexible I/O capability for both parallel and serial transfers.

The serial I/O Interface, using Intel's 8251 USART, provides a serial data communications channel that can be programmed to operate with most of the current serial data transmission protocols. Synchronous or asynchronous mode, baud rate, character length, number of stop bits and even/odd parity are all program selectable.

The Parallel I/O Interface, using two Intel 8255 Programmable Peripheral Interface devices, provides 48 signal lines for the transfer and control of data to or from peripheral devices. Sixteen lines already have bidirectional driver and termination networks permanently installed. The remaining 32 lines, however, are uncommitted. Sockets are provided for the installation of active driver networks or passive termination networks as required to meet the specific needs of the user system.

In this chapter, each of the options available to the user will be reviewed and the specific information required to implement the desired I/O configurations will be summarized. Information required for assigning address space to the memory and I/O facilities is also provided. Section 4.1 deals with address allocation. Sections 4.2 and 4.3 cover the Serial and Parallel I/O Interface options, respectively.

4.1 MEMORY AND I/O ADDRESS ALLOCATION

The memory and I/O address decode logic in the SBC-104 interface is controlled in part by various wire wrap jumpers and switch selections. These switch/jumper connections and their use in assigning addresses to the SBC-104 memory and I/O facilities are summarized below.

RAM Address Selection

Each switch position in S3 specifies a RAM base address at a 4K byte boundary. A wire wrap jumper is used at pins 89-90-91 to select the lower or upper half of the system address space. See Table 4-1.

TABLE 4-1. RAM ADDRESS SELECTIONS

	RAM Base Address (Hex)	
Open Switch # at S3	Jumper 89-90*	Jumper 90-91
1	0000	8000
2	1000	9000
3	2000	A000
4	3000	B000
5*	4000*	C000
6	5000	D000
7	6000	E000
8	7000	F000

*Default setting - selected when shipped

PROM Address Selection

Each switch position in S4 specifies a PROM base address at a 4K byte boundary. A wire wrap jumper is used at pins 92-93-94 to select the lower or upper half of the system address space. See Table 4-2.

TABLE 4-2. PROM ADDRESS SELECTIONS

Open Switch # at S4	PROM Base Address (Hex) Jumper 92-93*	Jumper 93-94
1	0000	8000
2*	1000*	9000
3	2000	A000
4	3000	B000
5	4000	C000
6	5000	D000
7	6000	E000
8	7000	F000

*Default setting - selected at factory

Chip selects for the individual PROMs are hard wired to provide the addresses shown in Table 4-3.

TABLE 4-3. PROM Chip Select Addresses

Chip Select Mnemonic	Address Range Per Chip	Prom Device Location
PCS0/	X000 - X3FF	A34
PCS1/	X400 - X7FF	A46
PCS2/	X800 - XBFF	A60
PCS3/	XC00 - XFFF	A76

X = any hex digit; assigned by jumper selection

I/O Address Selection

The base address of the set of I/O facilities is determined jointly by wire wrap jumpers at two locations, S2 and pins 86-87-88. See Table 4-4.

Table 4-4. I/O BASE ADDRESS SELECTION

Connect Pin S2-1 To S2 Pin #	I/O Base Address (Hex) Jumper 86-87	Jumper 87-88*
9	00	80
8	10	90
7	20	A0
6	30	B0
5	40	C0
4*	50	D0*
3	60	E0
2	70	F0

*Default selection

Individual I/O port addresses are hard wired according to the address schemes shown in Table 4-5, Parallel I/O Addresses Table 4-6, Serial I/O Addresses and Table 4-7, Interrupt Addresses

Table 4-5. PARALLEL I/O ADDRESSES

	Group 1 Location A20				Group 2 Location A21			
PORT	1	2	3	CONTROL REQ	4	5	6	CONTROL REQ
ADDRESS	X4	X5	X6	X7	X8	X9	XA	XB

X = any hex digit; assigned by jumper

Table 4-6. SERIAL I/O ADDRESSES

USART DATA	XC	READ/WRITE
USART CONTROL	XD	READ/WRITE

X = any hex digit; assigned by jumper

Table 4-7. INTERRUPT ADDRESSES

INTERRUPT STATUS REGISTER	X0	READ ONLY
INTERRUPT MASK REGISTER	X1	READ/WRITE
RESET TIMER INTERRUPT	X2	WRITE ONLY

*Note: The interval timer can also be reset at the same time the mask register is loaded by using X3;
X = any hex digit; assigned by jumper

4.2 SERIAL I/O INTERFACE OPTIONS

The Serial I/O Interface includes a variety of jumper selectable features that affect how the 8251 and the RS232 interface interact, what baud rate the 8251 uses, and how serial I/O interrupts are generated. It also includes some jumper options that give the bus master access to certain RS232 signal lines via the parallel I/O interface rather than through the 8251. Implementation of each feature is summarized in the following sections.

4.2.1 USART/RS232 INTERFACE CONFIGURATIONS

The 8251 is capable of assuming the role of a data processing terminal or a data set. Whichever role it is assigned influences the source or destination connector pins for the two pairs of handshaking signals (DATA TERMINAL READY; DATA SET READY) and (REQUEST TO SEND; CLEAR TO SEND) and the serial data lines.

For example, when the 8251 operates in the data terminal role, its TXD pin is an output providing serial data to the TRANSMIT DATA line

and its RXD pin is an input for receiving serial data from the RECEIVE DATA line. When the 8251 operates in the data set role, its TXD and RXD pins exchange functions with each other. TXD becomes the RECEIVE DATA output pin and RXD becomes the TRANSMIT DATA input pin.

The same exchange of pin functions takes place at the 8251's four handshaking signal input/output pins. In the data terminal mode DTR/ and RTS/ are the DATA TERMINAL READY and REQUEST TO SEND outputs while DSR/ and CTS/ are the DATA SET READY and CLEAR TO SEND inputs. In the data set mode, DTR/ and DSR/ exchange functions and RTS/ and CTS/ exchange functions.

Jumper pins are provided on-board for connecting the RS232 handshaking signal line to the appropriate 8251 pin, according to the selected role of the 8251. However, the capability to reverse the TRANSMIT DATA and RECEIVE DATA lines must be made externally as the on-board paths for these signals do not include provisions for jumpers.

Table 4-8 identifies the necessary jumper connection to allow the 8251 to assume the role of either a data processing terminal or a data set.

4.2.2 DTE TRANSMIT CLOCK

The baud rate clock frequency, which is supplied to the 8251 TXC input, can also be connected to the RS232 output line DTE TRANSMIT CLOCK. To complete this path, the following three jumpers must be connected: 9-10*, 13-14* and 23-24*. As indicated by the asterisks, this is considered a standard configuration.

Table 4-8. USART/RS232 HANDSHAKING JUMPERS

GOAL	REQUIRED JUMPER ACTION	
	DELETE	ADD
8251 TO OPERATE AS DATA TERMINAL		
• With normal handshaking	None	Use default as is
• Loop DATA TERM RDY back to 8251 as DATA SET RDY	17-18*	16-18 use 15-16*
• Loop DATA SET RDY back to data set as DATA TERM RDY	15-16*	15-17 use 17-18*
• Loop REQ TO SEND back to 8251 as CLR TO SEND	19-20*	19-21 use 21-22*
• Loop CLR TO SEND back to data set as REQ TO SEND	21-22*	20-22 use 19-20*
8251 TO OPERATE AS DATA SET †		
• With normal handshaking	15-16* 17-18* 19-20* 21-22*	15-18 16-17 19-22 20-21
• Loop DATA SET RDY back to 8251 as DATA TERM RDY	15-16* 19-20* 21-22*	16-17 use 17-18* 19-22 21-20
• Loop DATA TERM RDY back to data term DATA SET RDY	15-16* 19-20* 21-22*	15-18 use 17-18* 19-22 20-21

Table 4-8. Continued

GOAL	REQUIRED JUMPER ACTION	
	DELETE	ADD
• Loop CLR TO SEND back to 8251 as REQ TO SEND	15-16*	15-18
	17-18*	16-17
	21-22*	20-21
		use 19-20*
• Loop REQ TO SEND back to data term as CLR TO SEND	15-16*	15-18
	17-18*	16-17
	21-22*	20-21
		use 19-20*

*Denotes default connections
†(Provision for reversing TXD and RXD must be made externally)

4.2.3 SEC TRANSMIT DATA OPTION

This optional path allows the bus master to activate the SEC TRANSMIT DATA output through Port 6 of the parallel I/O interface. To implement this option, connect the following pairs of jumper pins: 12-13, 23-25 and pin 76 to an appropriate jumper pin at Port 6. Pin 76 and the Port 6 jumper pins are shown on sheet 5 of the schematic. If this option is used, the DTE TRANSMIT CLOCK path is disabled.

Note that the pin convention for secondary transmitted data and secondary received data conforms to the RS232C specification. If reverse channel operation with Bell 202 C,D type datasets is desired, it is necessary to move the wire connected to pin 14 of the RS232C connector to pin 11 and pin 16 to pin 12.

4.2.4 SERIAL I/O INTERRUPT SELECTIONS

There are two serial I/O interrupt lines, SIOR1 and SIOT1.

To implement the SIOR1 interrupt, connect jumper pins 84-85*. SIOR1 is disabled when pins 83-84 are connected.

SIOT1 can be controlled by either the TXR or TXE output of the 8251. To generate interrupts from TXR, connect pins 79-81*. To generate interrupts from the TXE output, connect pins 79-80. A jumper at pins 79-82 will disable SIOT1.

4.2.5 BAUD RATE AND PROGRAM SELECTABLE SERIAL I/O OPTIONS

Before it can begin its serial I/O operations, the 8251 must be program-initialized to support the desired mode of operation. The bus master initializes the 8251 by outputting a set of control bytes to the USART device. These control words specify:

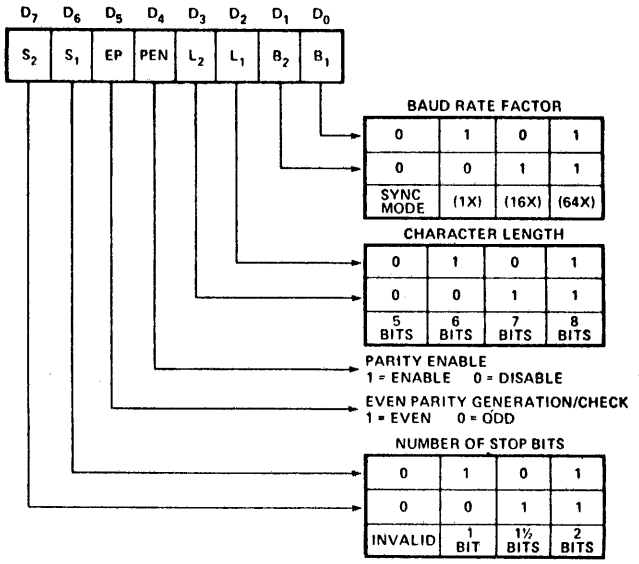
- synchronous or asynchronous operation,
- baud rate factor,
- character length,
- number of stop bits,
- even/odd parity,
- parity/no parity

As explained in Section 3.5.1, there are two types of control words: (1) Mode instruction and (2) Command instruction. The Mode instruction initializes the 8251 USART. Because the USART supports either synchronous or asynchronous operation, the Mode instruction has one format for synchronous operation and another for asynchronous. The two least significant bits of the Mode instruction byte specify the format. If DO and D1

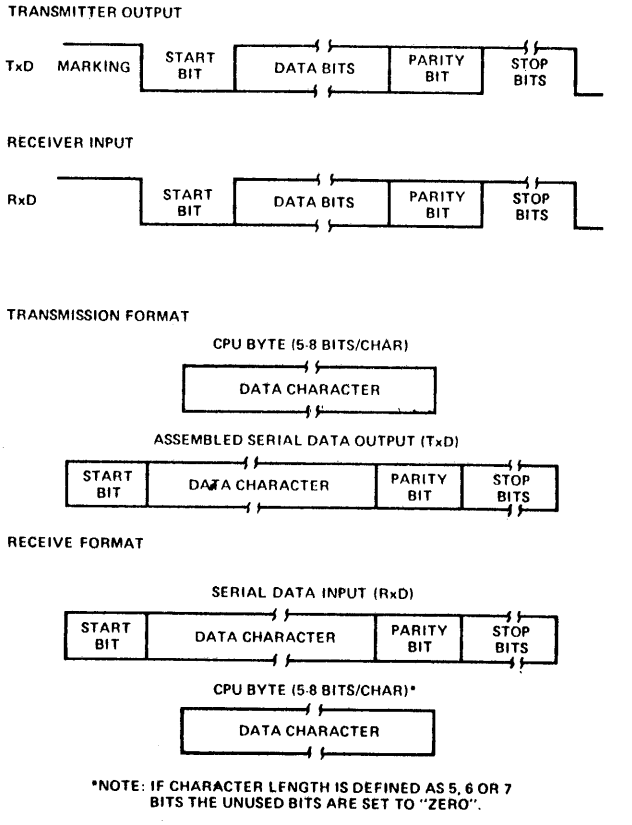
both equal 0, synchronous operation is indicated; otherwise, it is asynchronous. The Mode instruction format for asynchronous operation is illustrated in Figure 4-1. The Mode instruction for synchronous operation is shown in Figure 4-2.

Notice in Figure 4-1 that the baud rate factor is specified by the two least significant bits of the instruction byte (labeled B1 and B2). During asynchronous communications, the Baud Rate Clock frequency supplied to the 8251's TXC and RXC input pins is divided by the baud rate factor to produce the effective baud rate (i.e., the frequency at which data bits are serially transmitted by the 8251 USART). Consequently, the Baud Rate Clock, as well as the program-selected baud rate factor, must be considered in implementing the desired effective baud rate. The Baud Rate Clock frequency is selected through various jumper connections as shown on sheet 4 of the SBC-104 schematic (Appendix A). The selection of an effective baud rate is summarized in Table 4-9.

Notice from the schematic that TXC and RXC inputs can be supplied by externally supplied clocks (via connector pins J3-3 and J3-7, respectively), instead of using the Baud Rate Clock, if jumpers 10-11 and 6-7 are connected and jumpers 9-10* and 7-8* are disconnected.

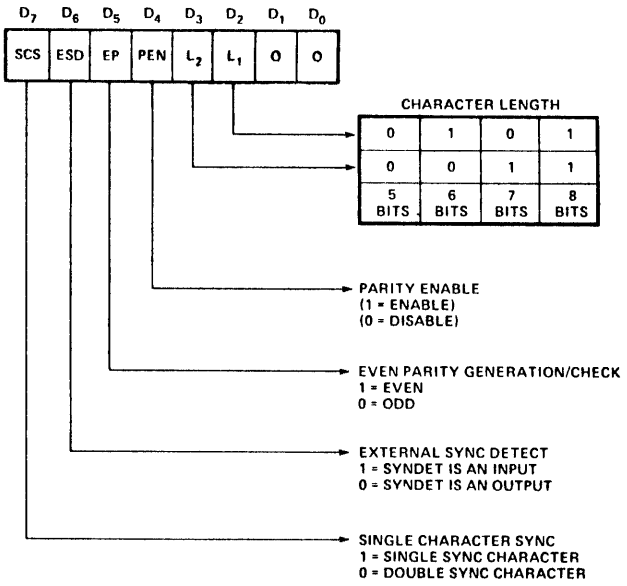


Mode Instruction Format, Asynchronous Mode

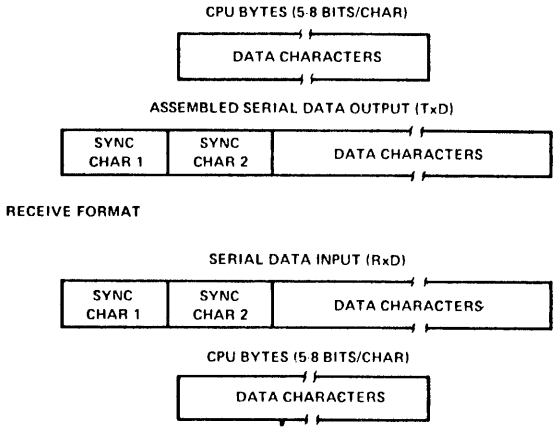


Asynchronous Mode

FIGURE 4-1. ASYNCHRONOUS OPERATION



Mode Instruction Format, Synchronous Mode



Synchronous Mode, Transmission Format

FIGURE 4-2. SYNCHRONOUS OPERATION

TABLE 4-9. BAUD RATE SELECTION

Jumper Connection	Synchronous Mode	Asynchronous Mode	
		Baud Rate Factor = 16 (2)	Baud Rate Factor = 64 (2)
3-1	-	19,200	4800
4-1	-	9600	2400
5-1	-	4800	1200
6-1	38,400	2400	600
7-1	19,200	1200	300
8-1	9600	600	150
(1) 9-1	4800	300	75
(1) 9-1, 1-2	6980	-	110 (TTY)

Effective Baud Rate (Hz)

Note: (1) If jumper pair 1-2 is not connected, the frequency at jumper pole 9 is 4.8 KHZ. If jumper 1-2 is connected, however, the frequency at jumper pole 8 is 6.98 KHZ which, with a programmed baud rate factor of 64, provides an effective baud rate of approximately 110 baud for Teletype use. If jumper pair 1-2 is connected, the jumper at 3-4 must be moved to the 3-5 position to maintain the 1 ms frequency on CLK INT.

(2) Baud rate factor is software selectable.

4.3 PARALLEL I/O OPTIONS

The Parallel I/O Interface consists of six 8-bit I/O port implemented with two Intel 8255 Programmable Peripheral Interface devices. The primary user considerations in determining how to use each of the six I/O ports are:

1) Choice of operating mode (as defined in Section 3.4.1),
2) direction of data flow (input, output or bidirectional),
3) choice of driver/termination networks for port's data path.

In the following paragraphs, we will define the capabilities of each port and summarize, in tables, that information which is necessary to use the port in each of its potential configurations. Each table will list the port I/O address, the control register address and the format for the control word which is output to the 8255 by the bus master and which specifies the particular configuration to be used. Each table will also summarize all of the relevant information concerning the choice and use of driver/termination networks, the data polarity, the connecting of jumpers and what they enable, and any restrictions on the use of the other two ports in each group. Examples of suitable driver/termination networks are listed in Section 5.1.

The configuration tables for group 2 ports are identical to those for group 1 ports except for I/O address, port numbers, component location numbers and jumper pin numbers. For this reason the tables are organized as three sets: Ports 1 and 4, Ports 2 and 5 and Ports 3 and 6.

At the beginning of each set, the general characteristics of that port are reviewed. Where port numbers are used in the text, the group 1 number is presented first and the corresponding group 2 number follows in parentheses. For example, when referring to B ports, the reference will appear as Port 2(5).

The introductory text is followed by a series of tables that cover all of the configurations that are possible for the ports under discussion. To simply the search for specific tables, each table is presented on a separate page.

Table 4-10 summarizes the various mode combinations that are possible with

TABLE 4-10. PARALLEL I/O INTERFACE CONFIGURATIONS

CONFIGURATION NUMBER	8255 PORT A	8255 PORT B	8255 PORT C Lower ($C_\emptyset$ C_1 C_2 C_3)	8255 PORT C Upper (C_4 C_5 C_6 C_7)
1	MODE $\emptyset$-I	MODE $\emptyset$-I/O	--- I/O ----	---- I/O ----
2	MODE $\emptyset$-O	MODE $\emptyset$-I/O	--- I/O ----	---- I/O ----
3	MODE $\emptyset$-I	MODE 1-I/O	R R R I	0 0 0 U
4	MODE $\emptyset$-I	MODE 1-I/O	R R R 0	I I I U
5	MODE $\emptyset$-0	MODE 1-I/O	R R R I	0 0 0 U
6	MODE $\emptyset$-0	MODE 1-I/O	R R R 0	I I I U
7	MODE 1-I	MODE $\emptyset$-I/O	I I I R	R R 0 0
8	MODE 1-I	MODE $\emptyset$-I/O	0 0 0 R	R R I I
9	MODE 1-0	MODE $\emptyset$-I/O	I I I R	0 0 R R
10	MODE 1-0	MODE $\emptyset$-I/O	0 0 0 R	I I R R
11	MODE 1-I	MODE 1-I/O	R R R R	R R I I
12	MODE 1-I	MODE 1-I/O	R R R R	R R 0 0
13	MODE 1-0	MODE 1-I/O	R R R R	I I R R
14	MODE 1-0	MODE 1-I/O	R R R R	0 0 R R
15	MODE 2-B	MODE $\emptyset$-I/O	U I I R	R R R R
16	MODE 2-B	MODE $\emptyset$-I/O	U 0 0 R	R R R R
17	MODE 2-B	MODE 1-I/O	R R R R	R R R R

I = INPUT

0 = OUTPUT

I/O = INPUT OR OUTPUT

B = BIDIRECTIONAL

R - Reserved

U - No unused drivers/terminators available. These bits may be used on 8255 #2 (A21) to connect control lines on the Serial I/O interface. (Jumpers 75-78).

Ports A and B and indicates how each Port C bit can or cannot be used for each mode combination. This table can serve as useful starting point for selecting an I/O configuration for either group 1 or group 2 ports. Once the desired mode combination is selected and the Port C bit assignments are made, the appropriate configuration tables (Tables 4-11 through 4-36) can be referred to for implementation details.

Appendix C gives an add/delete wire list for a possible implementation of each configuration. Those tables can be used to simply the generation of a wire list for a given configuration.

4.3.1 PORTS 1 and 4 (8255 PORT A)

Port 1(4) is the only port that already includes a permanent bidirectional driver/termination network (two 8226 Bidirectional Bus Drivers). Port 1(4) is also the only port which can be programmed to function in any one of the three 8255 operating modes, which were defined in Section 3.4.1. Before Port 1(4) is programmed for input or output in any one of the three modes, certain jumper connections must be made to allow the port to function properly in the chosen mode. Other jumper connections must be made to enable interrrupts when Port 1(4) is in mode 1 or mode 2. In all, there are five potential configurations for Port 1(4). All of the necessary information for implementing each configuration has been summarized in the following tables:

PORT 1(4) CONFIGURATIONS

	Mode	Direction	TABLES Group 1	Group 2
1.	Mode 0	Input	4-11	4-12
2.	Mode 0	Output (Latched)	4-13	4-14
3.	Mode 1	Input (Strobed)	4-15	4-16
4.	Mode 1	Output (Latched)	4-17	4-18
5.	Mode 2	Bidirectional	4-19	4-20

TABLE 4-11. PORT 1, MODE 0 INPUT CONFIGURATION

PORT 1 ADDRESS: X4, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0	1				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory-installed at A1 and A2.

DATA POLARITY AT J1: Negative

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	30-31*	29-30	Enable input at 8226's
		40-41*	Disables PIOA1

PORT RESTRICTIONS - PORT 2: None; Port 2 can be programmed for mode 0 or mode 1, input or output (see Section 4.3.2)

PORT 3: None; Port 3 can be programmed for mode 0, 8-bit input or output, unless Port 2 is in mode 1 (see Section 4.3.3)

TABLE 4-12. PORT 4, MODE 0 INPUT CONFIGURATION

PORT 4 ADDRESS: X8, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0	1				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory-installed at A7 and A8.

DATA POLARITY AT J2: Negative true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	52-53*	53-54	Enable input at 8226's
		71-72*	Disables PIOA2

PORT RESTRICTIONS - PORT 5: None; Port 5 can be programmed for mode 0 or mode 1, input or output (see Section 4.3.2)

PORT 6: None; Port 6 can be programmed for mode 0, 8-bit input or output, unless Port 5 is in mode 1 (see Section 4.3.3)

TABLE 4-13. PORT 1, MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 1 ADDRESS: X4, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0	0				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory-installed at A1 and A2.

DATA POLARITY AT J1: Negative true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		30-31*	Enable output at 8226's
		40-41*	Disables PIOA1

PORT RESTRICTIONS - PORT 2: None; Port 2 can be in mode 0 or mode 1, input or output (see Section 4.3.2)

PORT 3: None; Port 3 can be in mode 0, 8-bit input or output, unless Port 2 is in mode 1 (see Section 4.3.3)

TABLE 4-14. PORT 4, MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 4 ADDRESS: X8, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0	0				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory-installed at A7 and A8.

DATA POLARITY AT J2: Negative true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		52-53*	Enable output at 8226's
		71-72*	Disables PIOA2

PORT RESTRICTIONS: - PORT 5: None; Port 5 can be in mode 0 or mode 1, input or output (see Section 4.3.2)

PORT 6: None; Port 6 can be in mode 0, 8-bit input or output, unless Port 5 is in mode 1 (see Section 4.3.3)

TABLE 4-15. PORT 1, MODE 1 INPUT STROBED

PORT 1 ADDRESS: X4, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	1	1				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory installed at A1 and A2. A terminator network must be installed at A3 and a driver network must be installed at A4.

DATA POLARITY AT J1: Negative true. Polarity of Port 3 control outputs depends on whether driver at A4 is inverting or non-inverting.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	30-31*	29-30	Enable input at 8226's.
	48-49* and 40-41*	40-49	Connects Port 3, bit 3 to PIOA1.
		38-39*	Connects STB_A/ input (J1-26) to bit 4 of Port 3.
	36-37*	37-48	Connects bit 5 of Port 3 (IBF_A) to J1-18.

PORT RESTRICTIONS - PORT 2: None; Port 2 can be in mode 0 or mode 1, input or output (see Section 4.3.2)

PORT 3: Port 3 bits perform the following dedicated functions:

- Bits 0,1 and 2 - provide control for Port 2 if Port 2 is in mode 1
- Bit 3 - INTR (interrupt request) output for Port 1
- Bit 4 - STB/ (strobe) input for Port 1
- Bit 5 - IBF (input buffer full) output for Port 1
- Bits 6 and 7 - Can be used for input or output; both have same direction.

TABLE 4-16. PORT 4, MODE 1 INPUT STROBED

PORT 4 ADDRESS: X8, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	1	1				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory-installed at A7 and A8. A terminator network must be installed at A9 and a driver network must be installed at A10.

DATA POLARITY AT J2: Negative true. Polarity of Port 3 control outputs depends on whether driver at A10 is inverting or non-inverting.

JUMPER ACTION:

* = Default connection

DELETE	ADD	EFFECT
52-53*	53-54	Enable input at 8226's
71-72* and 69-70*	70-71	Connects Port 6, bit 3 to PIOA2.
	61-62*	Connects STB_A/ input (J2 - 26) to bit 4 of Port 6.
59-60*	60-69	Connects bit 5 of Port 6 to J2-18.

PORT RESTRICTIONS - PORT 5: None; Port 5 can be in mode 0 or mode 1, input or output (see Section 4.3.2)

PORT 6: Port 6 bits perform the following dedicated functions:

- Bits 0, 1 and 2 - provide control for Port 5 if Port 5 is in mode 1.
- Bit 3 - INTR (interrupt request) output for Port 4.
- Bit 4 - STB/ (strobe) input for Port 5
- Bit 5 - IBF (input buffer full) output for Port 4
- Bits 6 and 7 - Can be used for input or output; both have same direction.

TABLE 4-17. PORT 1, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 1 ADDRESS: X4, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	1	0				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory-installed at A1 and A2. A terminator network must be installed at A3 and a driver network must be installed at A4.

DATA POLARITY AT J1: Negative true. The polarity of Port 3 control outputs depends on the type of driver installed at A4.

JUMPER	DELETE	ADD	EFFECT
* = Default connection		30-31*	Enable output at 8226's
	40-41* and 48-49*	40-49	Connects Port 3, bit 3 to PIOA1.
		34-35*	Connects ACK_A/ input (J1-30) to bit 6 of Port 3.
	32-33*	33-48	Connects bit 7 of Port 3 (OBF_A/) to J1-18.

PORT RESTRICTIONS - PORT 2: None; Port 2 can be in mode 0 or mode 1, input or output.

PORT 3: Port 3 bits perform the following dedicated functions:

- Bits 0, 1 and 2 - Dedicated to the control of Port 2 if Port 2 is in mode 1.
- Bit 3 - INTR (interrupt request) output for Port 1.
- Bits 4 and 5 - Can be used as input or output; both have same direction.
- Bit 6 - ACK/ (acknowledge) input for Port 1.
- Bit 7 - OBF/(output buffer full) output for Port 1.

TABLE 4-18. PORT 4, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 4 ADDRESS: X8, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	1	0				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory-installed at A7 and A8. A terminator network must be installed at A9 and a driver network must be installed at A10.

DATA POLARITY AT J2: Negative true. The polarity of Port 6 control outputs depends on the type of driver installed at A10.

JUMPER ACTION:

* = Default connection

DELETE	ADD	
	52-53*	Enable outputs at 8226's
71-72* and 69-70*	70-71	Connects Port 6, bit 3 to PIOA2.
	57-58*	Connects ACK_A/ input (J2-30) to bit 6 of Port 6.
55-56*	56-69	Connects bit 7 of Port 6 (OBF_A/) to J2-18.

PORT RESTRICTIONS - PORT 5: None; Port 5 can be in mode 0 or mode 1, input or output.

PORT 6: Port 6 bits perform the following dedicated functions:

- Bits 0, 1 and 2 - Dedicated to the control of Port 5 if Port 5 is in mode 1.
- Bit 3 - INTR (interrupt request) output for Port 4.
- Bits 4 and 5 - Can be used as input or output; both have same direction.
- Bit 6 - ACK/ (acknowledge) input for Port 4.
- Bit 7 - OBF/(output buffer full) output for Port 4.

TABLE 4-19. PORT 1, MODE 2 BIDIRECTIONAL CONFIGURATION

PORT 1 ADDRESS: X4, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	1	X	X				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory-installed at A1 and A2. A terminator network must be installed at A3 and a driver network must be installed at A4.

DATA POLARITY AT J1: Negative true. The polarity of Port 3 control output depends on the type of driver installed at A4.

JUMPER ACTION:

* = Default connection

DELETE	ADD	EFFECT
30-31*	30-34	Allows ACK_A/ output of Port 3 to control 8226 direction mode. See NOTE below for alternatives.
40-41* and 48-49	40-49	Connects Port 3, bit 3 to POIA1.
	38-39*	Connects STB_A/ input (J1-26) to bit 4 of Port 3.
42-43* and 36-37*	37-42	Connects bit 5 of Port 3 (IBF_A) to J1-24.
	34-35*	Connects ACK_A/ input (J1-30) to bit 6 of Port 3.
32-33*	33-48	Connects bit 7 of Port 3 (OBF_A/) to J1-18.

PORT RESTRICTIONS - PORT 2: None.

PORT 3: Port 3 bits perform the following dedicated functions:

- Bit 0 - Cannot be used
- Bits 1 and 2 - Can both be used in either input or output if Port 2 is in mode 0.
- Bit 3 - INTR (interrupt request) output for Port 1.
- Bit 4 - STB/ (strobe) input for Port 1.
- Bit 5 - IBF (input buffer full) output for Port 1.
- Bit 6 - ACK/ (acknowledge) input for Port 1.
- Bit 7 - OBF/ (output buffer full) output for Port 1.

NOTE: If Port 2 is in mode 0, source for PIOA1 could be bit 0, 1 or 2 of Port 3. If external interrupt (jumper 26) is not used, an external signal could be used via J1-50.

TABLE 4-20: PORT 4, MODE 2 BIDIRECTIONAL CONFIGURATION

PORT 4 ADDRESS: X8, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	1	X	X				

DRIVER/TERMINATION NETWORKS: Two Intel 8226 Bidirectional Bus Drivers are factory-installed at A7 and A8. A terminator network must be installed at A9 and a driver network must be installed at A10.

DATA POLARITY AT J2: Negative true. The polarity of Port 6 control outputs depends on the type of driver used at A10.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	52-53*	53-57	Allows ACK_A/ output of Port 6 to control 8226 direction mode. See NOTE below for alternatives.
	71-72* and 69-70*	70-71	Connects Port 6, bit 3 to PIOA2.
		61-62*	Connects STB_A/ input (J2-26) to bit 4 of Port 6.
	63-64* and 59-60*	60-63	Connects bit 5 of Port 6 (IFB_A) to J2- 24.
		57-58*	Connects ACK_A/ input (J2-30) to bit 6 of Port 6.
	55-56*	56-69	Connects bit 7 of Port 6 (OBF_A/) to J2-18.

PORT RESTRICTIONS - PORT 5: None

PORT 6: Port 6 performs the following dedicated functions:

- Bit 0 - Can be used to control bits on Serial I/O Interface; cannot be used otherwise.
- Bits 1 and 2 - Can both be used as either input or output if Port 5 is in mode 0.
- Bit 3 - INTR (interrupt request) output for Port 4.
- Bit 4 - STB/ (strobe) input for Port 4.
- Bit 5 - IBF (input buffer full) output for Port 4.
- Bit 6 - ACK/ (acknowledge) input for Port 4.
- Bit 7 - OBF/ (output buffer full) output for Port 4.

NOTE: If Port 5 is in mode 0, source for PIOA2 could be bit 0, 1 or 2 of Port 6.

4.3.2 PORTS 2 AND 5 (8255 PORT B)

Port 2(5) can be programmed for input or output in either mode 0 or mode 1. If Port 2(5) is to be used for input, in either mode, terminator networks must be installed in the sockets at A5(11) and A6(12). If Port 2(5) is to be used for output, in either mode, driver networks must be installed in the sockets at A5(11) and A6(12). When Port 2(5) is programmed for mode 1, interrupts can be enabled by connecting jumper pair 43-50 (64-75). The four potential configurations for Port 2(5) are summarized in the following tables:

PORT 2(5) CONFIGURATIONS

Mode	Direction	TABLES Group 1	Group 2
1. Mode 0	Input	4-21	4-22
2. Mode 0	Output (Latched)	4-23	4-24
3. Mode 1	Input (Strobed)	4-25	4-26
4. Mode 1	Output (Latched)	4-27	4-28

TABLE 4-21. PORT 2, MODE 0 INPUT CONFIGURATION

PORT 2 ADDRESS: X5, _ CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					0	1	

DRIVER/TERMINATION NETWORKS: Termination networks must be installed at A5 and A6.

DATA POLARITY AT J1: Positive true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		50-51*	Disables PIOB1

PORT RESTRICTIONS - PORT 1: None

PORT 3: None; Port 3 can be in mode 0, input or output unless Port 1 is in mode 1 or mode 2.

TABLE 4-22. PORT 5, MODE 0 INPUT CONFIGURATION

PORT 5 ADDRESS: X9, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					0	1	

DRIVER/TERMINATION NETWORKS: Termination networks must be installed at A11 and A12.

DATA POLARITY AT J2: Positive true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		73-74*	Disables PIOB2

PORT RESTRICTIONS - PORT 4: None

PORT 6: None; Port 6 can be in mode 0, input or output unless Port 4 is in mode 1 or mode 2.

TABLE 4-23. PORT 2, MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 2 ADDRESS: X5, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					0	0	

DRIVER/TERMINATION NETWORKS: Driver networks must be installed at A5 and A6

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		50-51*	Disable PIOB1

PORT RESTRICTIONS - PORT 1: None

PORT 3: None, Port 3 can be in mode 0 input or output, unless Port 1 is in mode 1 or mode 2.

TABLE 4-24. PORT 5, MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 5 ADDRESS: X9, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					0	0	

DRIVER/TERMINATION NETWORKS: Driver networks must be installed at A11 and A12

DATA POLARITY AT J2: Negative true, assuming inverting drivers are used at A11 and A12.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		73-74*	Disable PIOB2

PORT RESTRICTIONS - PORT 4: None

PORT 6: None; Port 6 can be in mode 0, input or output, unless Port 4 is in mode 1 or mode 2.

TABLE 4-25. PORT 2, MODE 1 STROBED INPUT CONFIGURATION

PORT 2 ADDRESS: X5, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					1	1	

DRIVER/TERMINATION NETWORKS: Terminator networks must be installed at A3, A5 and A6. A driver network must be installed at A4.

DATA POLARITY AT J1: Positive true. The polarity of Port 3 control outputs depends on the type of driver at A4.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	50-51* and 42-43*	43-50	Connects Port 3, bit 0 to PIOB1
		44-45*	Connects bit 1 of Port 3 (IBF_B) to J1-22.
	32-33* and 46-47*	32-47	Connects STB_B/ input (J1-32) to bit 2 of Port 3.

PORT RESTRICTIONS - PORT 1: None

PORT 3: Port 3 bits perform the following dedicated functions:

- Bit 0 - INTR (interrupt request) output for Port 2.
- Bit 1 - IBF (input buffer full) output for Port 2.
- Bit 2 - STB/ (strobe) input for Port 2.
- Bit 3 - If Port 1 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved.
- Bits 4 to 7 - Can be input or output if Port 1 is in mode 0 or in some mode combinations where Port 1 is in mode 1. These bits are always reserved when Port 1 is in mode 2. See Table 4-10 for details regarding bits 4 to 7.

TABLE 4-26. PORT 5, MODE 1 STROBED INPUT CONFIGURATION

PORT 5 ADDRESS: X9, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					1	1	

DRIVER/TERMINATION NETWORKS: Termination networks must be installed at A9, A11 and A12. A driver network must be installed at A10.

DATA POLARITY AT J2: Positive true. The polarity of Port 3 control outputs depends on the type of driver at A10.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	73-74* and 63-64*	64-74	Connects bit 0 of Port 6 to PIOB2.
		65-66*	Connects bit 1 of Port 6 (IBF_B) to J2-22.
	55-56* and 67-68*	55-68	Connects STB_B/ input (J2-32) to bit 2 of Port 6

PORT RESTRICTIONS - PORT 4: None

PORT 6: Port 6 bits perform the following dedicated functions:

- Bit 0 - INTR (interrupt request) output for Port 5.
- Bit 1 - IBF (input buffer full) output for Port 5.
- Bit 2 - STB/ (strobe) input for Port 5.
- Bit 3 - If Port 4 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved.
- Bits 4 to 7 - Can be input or output if Port 4 is in mode 0 or in some mode combinations where Port 4 is in mode 1. These bits are always reserved when Port 4 is in mode 2. See Table 4-10 for details.

TABLE 4-27. PORT 2, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 2 ADDRESS: X5, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					1	0	

DRIVER/TERMINATION NETWORKS: Driver networks must be installed at A4, A5 and A6. A terminator network must be installed at A3.

DATA POLARITY AT J1: Negative true, assuming that inverting drivers are used at A4, A5 and A6.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	50-51* and 42-43*	43-50	Connects bit 0 of Port 3 to PIOB1.
		44-45*	Connects bit 1 of Port 3 (IBF_B) to J1-22.
	32-33* and 46-47*	32-47	Connects STB_B/ input (J1-32) to bit 2 of Port 3.

PORT RESTRICTIONS - PORT 1: None

PORT 3: Port 3 bits perform the following dedicated functions:

- Bit 0 - INTR (interrupt request input for Port 2.
- Bit 1 - OBF/ (output buffer full) output for Port 2.
- Bit 2 - ACK/ (acknowledge) input for Port 2.
- Bit 3 - If Port 1 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved.
- Bits 4 to 7 - Can be input or output if Port 1 is in mode 0 or in some combinations where Port 1 is in mode 1. These bits are always reserved when Port 1 is in mode 2. See Table 4-10 for details.

TABLE 4-28. PORT 5, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 5 ADDRESS: X9, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					1	0	

DRIVER/TERMINATION NETWORKS: Driver networks must be installed at A10, A11 and A12. A terminator network must be installed at A9.

DATA POLARITY AT J2: Negative true, assuming that inverting drivers are used at A10, A11 and A12.

JUMPER ACTION:

DELETE	ADD	EFFECT
73-74* and 63-64*	64-74	Connects bit 0 of Port 6 to IPOB2.
	65-66*	Connects bit 1 of Port 6 (IBF_B) to J2-22.
55-56* and 67-68*	55-68	Connects STB_B/ input (J2-32) to bit 2 of Port 6.

PORT RESTRICTIONS - PORT 4: None

PORT 6: Port 6 bits perform the following dedicated functions:

- Bit 0 - INTR (interrupt request) input for Port 5.
- Bit 1 - OBF/ (output buffer full) output for Port 5.
- Bit 2 - ACK/ (acknowledge) input for Port 5.
- Bit 3 - If Port 4 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved.
- Bits 4 to 7 - Can be input or output if Port 4 is in mode 0 or in some combinations where Port 4 is in mode 1. These bits are always reserved when Port 4 is in mode 2. See Table 4-10 for details.

4.3.3 PORTS 3 AND 6 (8255 PORT C)

The use of Port 3(6) depends on the modes programmed for Ports 1(4) and 2(5). It can be implemented as an 8-bit input or output data path or as two 4-bit I/O paths only if both Port 1(4) and Port 2(5) are programmed for mode 0. If Port 1(4) is in either mode 1 or mode 2 or if Port 2(5) is in mode 1, various individual Port 3(6) bits are available while the other Port 3(6) bits are either dedicated to control functions or are unavailable for any purpose.

Tables 4-29 through 4-36 specify the use of Port 3(6) bits as separate pairs of 4-bit I/O ports. As such, the two halves of Port 3(6) can both operate as input or output ports or they can have separate direction characteristics. The two halves are referred to as lower (bits 0 to 3) and upper (bits 4 to 7).

When Port 1(4) is in mode 1, it uses bit 3 of Port 3(6) and two upper bits of Port 3(6) for control functions. When Port 1(4) is in mode 2, it uses bit 3 of Port 3(6) and all four upper bits of Port 3(6) for control functions. Similarly, when Port 2(5) is in mode 1, it uses bit 0 of Port 3(6) and two lower bits from Port 3(6) for control.

Table 4-37 summarizes the use of Port 3 bits for control by Ports 1 and 2. Table 4-38 serves the same purpose for Port 6. These tables can be used as final check lists to verify the correct wiring of Port 3 and Port 6 control bits.

TABLE 4-29. PORT 3 (LOWER) MODE 0, INPUT CONFIGURATION

PORT 3 ADDRESS: X6, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		1	0		1

DRIVER/TERMINATION NETWORKS: A termination network must be installed at A4.

DATA POLARITY AT J1: Positive true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		42-43*	Connects bit 0 to J1-24.
		44-45*	Connects bit 1 to J1-22.
		46-47*	Connects bit 2 to J1-20.
		48-49*	Connects bit 3 to J1-18.

PORT RESTRICTIONS - PORT 1: Port 1 must be in mode 0 for all four bits to be available.
PORT 2: Port 2 must be in mode 0 for all four bits to be available.

TABLE 4-30. PORT 6, (LOWER) MODE 0, INPUT CONFIGURATION

PORT 6 ADDRESS: XA, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		1	0		1

DRIVER/TERMINATION NETWORKS: A termination network must be installed at A10.

DATA POLARITY AT J2: Positive true.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		63-64*	Connects bit 0 to J2-24.
		65-66*	Connects bit 1 to J2-22.
		67-68*	Connects bit 2 to J2-20.
		69-70*	Connects bit 3 to J2-18.

PORT RESTRICTION - PORT 4: Port 4 must be in mode 0 for all four bits to be available.

PORT 5: Port 5 must be in mode 0 for all four bits to be available.

TABLE 4-31. PORT 3 (UPPER) MODE 0, INPUT CONFIGURATION

PORT 3 ADDRESS: X6, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		1	0		1

DRIVER/TERMINATION NETWORKS: A termination network must be installed at A3.

DATA POLARITY AT J1: Positive true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		38-39*	Connects bit 4 to J1-26.
		36-37*	Connects bit 5 to J1-28.
		34-35*	Connects bit 5 to J1-30.
		32-33*	Connects bit 7 to J1-32.

PORT RESTRICTIONS - PORT 1: Port 1 must be in mode 0 for all four bits to be available.

- PORT 2: Port 2 must be in mode 0 for all four bits to be available.

TABLE 4-32. PORT 6 (UPPER) MODE 0, INPUT CONFIGURATION

PORT 6 ADDRESS: XA, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		1	0		1

DRIVER/TERMINATION NETWORKS: A termination network must be installed at A9.

DATA POLARITY AT J2: Positive true.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		61-62*	Connects bit 4 to J2-26.
		59-60*	Connects bit 5 to J2-28.
		57-58*	Connects bit 6 to J2-30.
		55-56*	Connects bit 7 to J2-32.

PORT RESTRICTION - PORT 4: Port 4 must be in mode 0 for all four bits to be available.

PORT 5: Port 5 must be in mode 0 for all four bits to be available.

TABLE 4-33. PORT 3 (LOWER) MODE 0, LATCHED OUTPUT CONFIGURATION

PORT 3 ADDRESS: X6, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		0	0		0

DRIVER/TERMINATION NETWORKS: A driver network must be installed at A4.

DATA POLARITY AT J1: Negative true, assuming inverting drivers are used at A4.

JUMPER ACTION:

* = Default connection

DELETE	ADD	EFFECT
	42-43*	Connects bit 0 to J1-24.
	44-45*	Connects bit 1 to J1-22.
	46-47*	Connects bit 2 to J1-20.
	48-49*	Connects bit 3 to J1-18.

PORT RESTRICTIONS - PORT 1: Port 1 must be in mode 0 for all four bits to be available.

PORT 2: Port 2 must be in mode 0 for all four bits to be available.

TABLE 4-34. PORT 6 (LOWER) MODE 0, LATCHED OUTPUT CONFIGURATION

PORT 6 ADDRESS: XA, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		0	0		0

DRIVER/TERMINATION NETWORKS: A driver network must be installed at A10.

DATA POLARITY AT J2: Negative true, assuming inverting drivers are used at A10.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		63-64*	Connects bit 0 to J2-24.
		65-66*	Connects bit 1 to J2-22.
		67-68*	Connects bit 2 to J2-20.
		69-70*	Connects bit 3 to J2-18.

PORT RESTRICTIONS - PORT 4: Port 4 must be in mode 0 for all four bits to be available.

PORT 5: Port 5 must be in mode 0 for all four bits to be available.

TABLE 4-35. PORT 3 (UPPER) MODE 0, LATCHED OUTPUT CONFIGURATION

PORT 3 ADDRESS: X6, CONTROL REGISTER ADDRESS: X7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		0	0		0

DRIVER/TERMINATION NETWORKS: A driver networks must be installed at A3.

DATA POLARITY AT J1: Negative true, assuming inverting drivers are used at A3.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		38-39*	Connects bit 4 to J1-26.
		36-37*	Connects bit 5 to J1-28.
		34-35*	Connects bit 6 to J1-30.
		32-33*	Connects bit 7 to J1-32.

PORT RESTRICTIONS - PORT 1: Port 1 must be in mode 0 for all four bits to be available.

PORT 2: Port 2 must be in mode 0 for all four bits to be available.

TABLE 4-36. PORT 6 (UPPER) MODE 0, LATCHED OUTPUT CONFIGURATION

PORT 6 ADDRESS: XA, CONTROL REGISTER ADDRESS: XB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		0	0		0

DRIVER/TERMINATION NETWORKS: A driver network must be installed at A9.

DATA POLARITY AT J2: Negative true, assuming inverting drivers are used at A9.

JUMPER ACTION:

* = Default connection

DELETE	ADD	EFFECT
	61-62*	Connects bit 4 to J2-26.
	59-60*	Connects bit 5 to J2-28.
	57-58*	Connects bit 6 to J2-30.
	55-56*	Connects bit 7 to J2-32.

PORT RESTRICTIONS - PORT 4: Port 4 must be in mode 0 for all four bits to be available.

PORT 5: Port 5 must be in mode 0 for all four bits to be available.

TABLE 4-37. PORT 3 RESTRICTION SUMMARY
(PORT 1/PORT 2 CONTROL FUNCTIONS)

PORT 3 BIT #	PORT 1 MODE	PORT 2 MODE	FUNCTION	JUMPER ACTION
0	-	1-I/O	Provides $INTR_B$ to PIOB1	Delete 42-43* Delete 50-51* Add 42-43
0	2-B	0-I/O	Cannot be used; no drivers/terminators available	Delete 42-43*
1	-	1-I	Provides IBF_B output to J1-22	Add 44-45*
1	-	1-0	Provides OBF_B output to J1-22	Add 44-45*
2	-	1-I	Provides STB_B input from J1-32	Delete 32-33* Delete 46-47* Add 32-47
2	-	1-0	Provides ACK_B/ input from J1-32	Delete 32-33* Delete 46-47* Add 32-47
3	1-I/O	-	Provides $INTR_A$ to PIOA1	Delete 40-41* Delete 48-49* Add 40-49
3	2-B	-	Provides $INTR_A$ to PIOA1	Delete 40-41* Delete 48-49* Add 40-49
4	1-I	-	Provides STB_A/ input from J1-26	Add 38-39*
4	2-b	-	Provides STB_A/ input from J1-26	Add 38-39*
5	1-I	-	Provides IBF_A/ output to J1-18	Delete 36-37* Add 37-48
5	2-B	-	Provides IBF_A output to J1-18	Delete 36-37* Add 37-48

(Table Continued on Next Page)

TABLE 4-37. PORT 3 RESTRICTION SUMMARY
(Continued)

PORT 3 BIT #	PORT 1 MODE	PORT 2 MODE	FUNCTION	JUMPER ACTION
6	1-0	-	Provides ACK_A/ input from J1-30	Add 34-35*
6	2-B	-	Provides ACK_A/ input from J1-30	Add 34-35*
7	0-I/O	1-I/O	Cannot be used; no drivers/terminators available	Delete 32-33*
7	1-0	-	Provides OBF_A output to J1-18	Delete 32-33* Add 33-48

NOTE 1: If Port 3 pin is not shown in this table as having a prescribed function for certain Port 1/Port 2 modes and if a spare driver or termination network is available, that pin can be used as an input or output, as determined by the driver/terminator availability.

NOTE 2: I = Input
O = Output
I/O = Input or Output
B = Bidirectional

TABLE 4-38. PORT 6 RESTRICTION SUMMARY
(PORT 4/PORT 5 CONTROL FUNCTIONS)

PORT 6 BIT #	PORT 4 MODE	PORT 5 MODE	FUNCTION	JUMPER ACTION
0	-	1-I/O	Provides $INTR_B$ to PIOB2	Delete 63-64* Delete 73-74* Add 64-74
0	2-B	0-I/O	Cannot be used; no drivers/terminators available	Delete 63-64*
1	-	1-I	Provides IBF_B output to J2-22	Add 65-66*
1	-	1-0	Provides OBF_B output to J2-22	Add 65-66*
2	-	1-I	Provides STB_B input from J2-32	Delete 55-56* Delete 67- 68 Add 55-68
2	-	1-0	Provides ACK_B/ input from J2-32	Delete 55-56* Delete 67-68* Add 55-68
3	1-I/O	-	Provides $INTR_A$ to PIOA2	Delete 69-70* Delete 71-72* Add 70-71
3	2-B	-	Provides $INTR_A$ to PIOA2	Delete 69-70* Delete 71-72* Add 70-71
4	1-I	-	Provides STB_A/ input from J2-26	Add 61-62*
4	2-B	-	Provides STB_A/ input from J2-26	Add 61-62*
5	1-I	-	Provides IBF_A output to J2-18	Delete 59-60* Add 60-69
5	2-B	-	Provides IBF_A output to J2-18	Delete 59-60* Add 60-69

(Table Continued on Next Page)

TABLE 4-38. PORT 6 RESTRICTION SUMMARY
(Continued)

PORT 6 BIT #	PORT 4 MODE	PORT 5 MODE	FUNCTION	JUMPER ACTION
6	1-0	-	Provides ACK_A/ input from J2-30	Add 57-58*
6	2-B	-	Provides ACK_A/ input from J2-30	Add 57-58*
7	0-I/O	1-I/O	Cannot be used; no drivers/terminators available	Delete 55-56*
7	1-0	-	Provides OBF_A output to J2-18	Delete 55-56* Add 56-69

NOTE 1: If a Port 6 pin is not shown in this table as having a prescribed function for certain Port 4/Port 5 modes and if a spare driver or termination network is available, that pin can be used as an input or output, as determined by the driver/terminator availability. Unused Port 6 pins can also be connected to certain control lines on the Serial I/O interface via jumper pins 75 to 78. These include pins shown in the table as unavailable because of a lack of unused drivers and terminators.

NOTE 2: I = Input
O = Output
I/O = Input or Output
B = Bidirectional

CHAPTER 5

SYSTEM INTERFACING

This chapter identifies each of the SBC-104's external connections and defines all signals on the external system bus.

5.1 ELECTRICAL CONNECTIONS

The SBC-104 electronics are mounted on a 12.00 × 6.75 inch printed circuit board that requires maximum average DC current at the following levels:

	1	2
V_{CC} = +5V ± 5%	I_{CC} = 3.6A max.	I_{CC} = 2.85A max.
V_{DD} = +12V ± 5%	I_{DD} = 700mA max.	I_{DD} = 450mA max.
V_{BB} = -5V ± 5%	I_{BB} = 180mA max.	I_{BB} = 3mA max.
V_{AA} = -12V ± 5%	I_{AA} = 60mA max.	I_{AA} = 60mA max.

Notes:
1. The values assume that four 8708 PROM's are present and that eight optional 220/330 Ω termination networks being driven low have been installed in the Parallel I/O Interface.
2. These values assume that the 8708 PROM's and optional termination networks are not present.

The SBC-104 has five edge connectors, as shown in Figure 5-1. Edge connectors at the top of the module are designed for compatibility with both flat cable and round cable hardware. All parallel I/O functions are paired with an independent signal ground pin (odd pins are ground). This allows flat cable implementation to utilize an alternate signal/ground scheme

for reduction of cross talk. Round cables may easily be implemented as twisted pair with an individual ground pin for every return wire. The serial connection hardware has similar flexibility but ground return lines are not as extensive. The connector is wired for RS232C compatibility, thus, only one signal ground is provided.

The Parallel I/O Interface communicates with external I/O devices via two 50-pin double-sided PC edge connectors (J1 and J2), 0.1 inch centers. External devices can be attached to J1 or J2 using any of the following mating connectors:

J1 and J2 Mating Connectors

Connector Type	Vendor	Part No.
Flat Cable	3M	3415-0001
	AMP	2-86792-3
Soldered	AMP	2-583715-3
	VIKING	3VH25/1JV-5
	TI	H312125
Wire-wrap	TI	H312125
	VIKING	3VH25/1JND-5
	CDC	VPB01E43A00A1
	ITT	EC4A050A1A
Crimp	AMP	1-583717-1

Tables 5-1 and 5-2 provide pin lists for the J1 and J2 connectors, respectively. The following TTL line drivers and Intel terminators are all compatible with the I/O driver sockets in the Parallel I/O Interface:

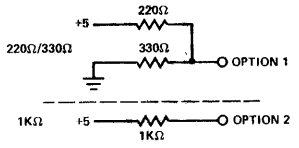
NOTE: All pin numbers listed in the following tables refer to numbers printed on the board, not to mating connector pin positions. When specifying pin numbers for cable harnesses, use caution since SBC-104 pin numbering is not necessarily the same as the connector pin numbering scheme.

Driver	Characteristic	Sink Current (ma)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note: I = inverting; N.I. = non-inverting
OC = open collector

I/O Terminators:

Terminators: 220Ω/330Ω divider or 1 kΩ pull up



SBC-901

SBC-902

See Appendix B for schematics

TABLE 5-1. PIN ASSIGNMENTS FOR CONNECTOR J1
(Parallel I/O Interface - Group 1)

PIN *	SIGNAL	PIN *	SIGNAL
1	GND	2	PORT 2 - BIT 7
3		4	PORT 2 - BIT 6
5		6	PORT 2 - BIT 5
7		8	PORT 2 - BIT 4
9		10	PORT 2 - BIT 3
11		12	PORT 2 - BIT 2
13		14	PORT 2 - BIT 1
15		16	PORT 2 - BIT 0
17		18	PORT 3 - BIT 3
19		20	PORT 3 - BIT 2
21		22	PORT 3 - BIT 1
23		24	PORT 3 - BIT 0
25		26	PORT 3 - BIT 4
27		28	PORT 3 - BIT 5
29		30	PORT 3 - BIT 6
31		32	PORT 3 - BIT 7
33		34	PORT 1 - BIT 7
35		36	PORT 1 - BIT 6
37		38	PORT 1 - BIT 5
39		40	PORT 1 - BIT 4
41		42	PORT 1 - BIT 3
43		44	PORT 1 - BIT 2
45		46	PORT 1 - BIT 1
47		48	PORT 1 - BIT 0
49	GND	50	EXT INTR 1/

* Refers to pin numbers shown on SBC-104 at J1.

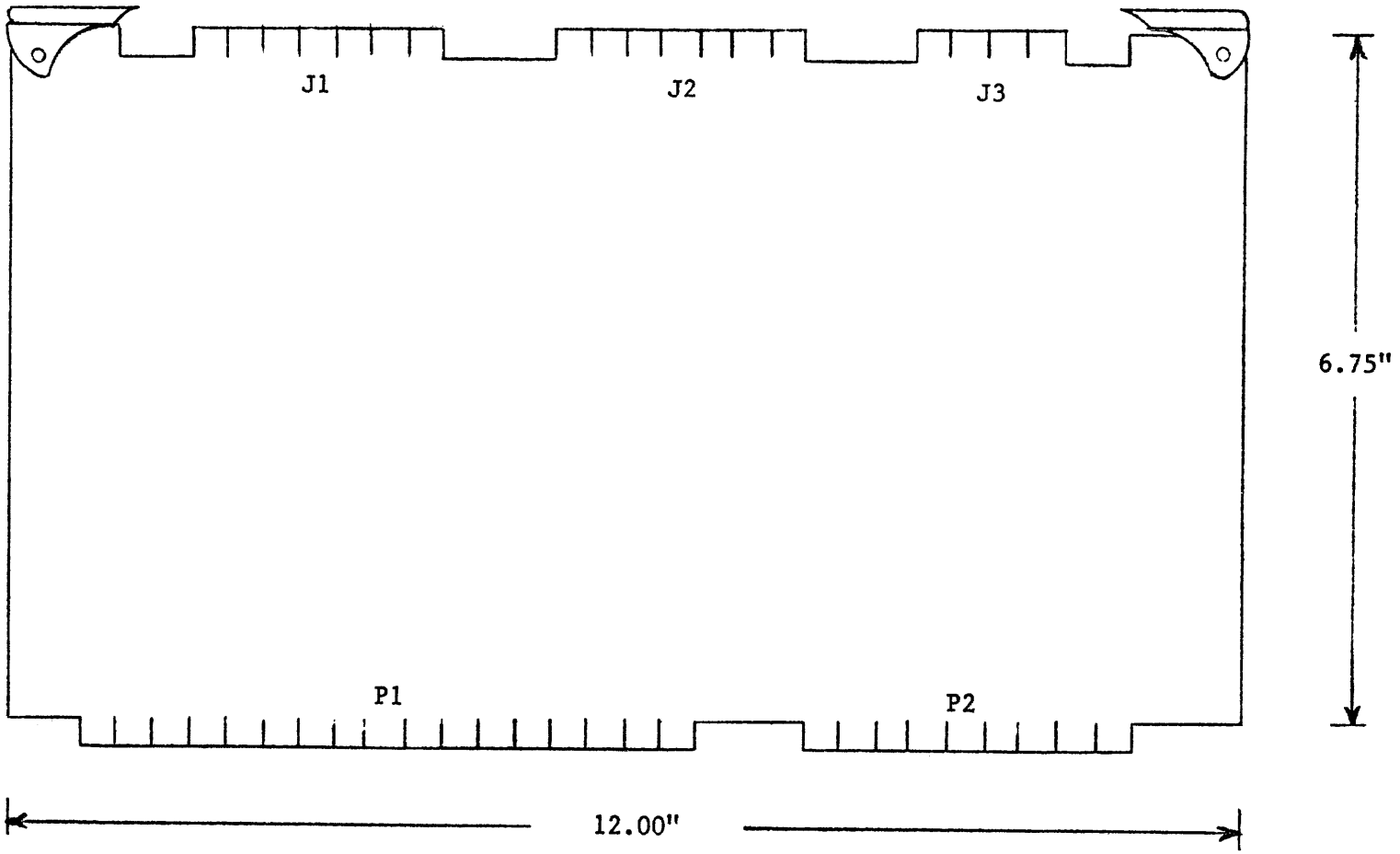


FIGURE 5-1. SBC-104/108 Edge Connectors

TABLE 5-2. PIN ASSIGNMENTS FOR CONNECTOR J2
(Parallel I/O Interface - Group 2)

PIN*	SIGNAL	PIN*	SIGNAL
1	GND	2	PORT 5 - BIT 7
3		4	PORT 5 - BIT 6
5		6	PORT 5 - BIT 5
7		8	PORT 5 - BIT 4
9		10	PORT 5 - BIT 3
11		12	PORT 5 - BIT 2
13		14	PORT 5 - BIT 1
15		16	PORT 5 - BIT 0
17		18	PORT 5 - BIT 3
19		20	PORT 6 - BIT 2
21		22	PORT 6 - BIT 1
23		24	PORT 6 - BIT 0
25		26	PORT 6 - BIT 4
27		28	PORT 6 - BIT 5
29		30	PORT 6 - BIT 6
31		32	PORT 6 - BIT 7
33		34	PORT 6 - BIT 7
35		36	PORT 4 - BIT 6
37		38	PORT 4 - BIT 5
39		40	PORT 4 - BIT 4
41		42	PORT 4 - BIT 3
43		44	PORT 4 - BIT 2
45		46	PORT 4 - BIT 1
47		48	PORT 4 - BIT 0
49	GND	50	EXT INTR 2/

*Refers to pin numbers shown on SBC-104 at J2.

The Serial I/O Interface communicates with an external I/O device via a 26-pin double-sided PC edge connector (J3), 0.1 inch centers. An external device can be connected to J3 using a 3M 3462-0001 flat cable connector or one of the following soldered connectors: TI H312113 or AMP 1-583715-1. Table 5-3 provides a pin list for connector J3.

The SBC-104 connects to the system bus via an 86-pin double-sided edge connector (P1), 0.156 inch centers. This edge connector will accept any of the following mating connectors: CDC VPB01E43A000A1,

Micro Plastics MP-0156-43-BW-4 or ARCO AE 443WP1. Section 5.2 defines each of the external system bus signals and includes a pin list for P1 (Table 5-5).

TABLE 5-3. PIN ASSIGNMENTS FOR CONNECTOR J3
(Serial I/O Interface)

PIN		PIN	
1	SEC TRANSMIT DATA	2	
3	TRANSMIT CLOCK	4	TRANSMIT DATA
5	SEC RECEIVED DATA	6	RECEIVE DATA
7	RECEIVE CLOCK	8	REQUEST TO SEND
9		10	CLEAR TO SEND
11	SEC REQUEST TO SEND	12	DATA SET READY
13	DATA TERMINAL READY	14	GND
15		16	CARRIER DETECT
17	RING INDICATOR	18	
19		20	
21	DTE TRANSMIT CLOCK	22	
23		24	
25	GND	26	SEC CLEAR TO SEND

NOTE: These pin numbers refer to pin assignments on the SBC-104 board at J3. They do not apply to any pin numbers shown on the mating connector. See Table 5-6 for a correlation between J3 pin numbers and the RS232C connector pin numbers.

The 60-pin double-sided connector labeled P2 in Figure 5-1 connects the auxiliary power supplies to RAM control circuits (see Table 5-4). These supplies may be used to supply power to the RAM memory in lieu of the main bus power. (The battery power requirements for these auxiliary supplies are shown in Table 7-1B in Section 7.1.) The mating connector for P2 is an Intel part number MDS-980. A key slot is provided on this connector between pin pairs 15-16 and 17-18 to allow protective keying of the mating connector.

TABLE 5-4. PIN ASSIGNMENTS FOR CONNECTOR P2
(Auxiliary Connector)

PIN		PIN	
1	GND	7	-5V Aux
2	GND	8	-5V Aux
3	+5V Aux	11	+12V Aux
4	+5V Aux	12	+12V Aux
		20	MEMORY PROTECT/

Note: a key slot is provided between pin pairs 15-16 and 17-18.

5.2 SYSTEM BUS SIGNAL DEFINITIONS

A summary definition of each system bus signal that is used by the SBC-104 is provided below.

INIT/ Initialization signal; resets the entire system to a known internal state.

MRDC/ Memory read command; indicates that the address of a memory location has been placed on the system address lines and specifies that the contents of the addressed location are to be read and placed on the system data bus.

MWTC/ Memory write command; indicates that the address of a memory location has been placed on the system address lines and that a data word has been placed on the system data bus. MWTC/ specifies that the data word is to be written into the addressed memory location.

TABLE 5-5. PIN ASSIGNMENTS FOR CONNECTOR P1
(External System Bus)

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	VCC	+ 5VDC	4	VCC	+ 5VDC
	5	VCC	+ 5VDC	6	VCC	+ 5VDC
	7	VDD	+12VDC	8	VDD	+12VDC
	9	VBB	- 5VDC	10	VBB	- 5VDC
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN	Bus Pri. In	16	[1]	
	17	BUSY/	Bus Busy	18	[1]	
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknow	24	INH 1/	RAM Inhibit
SPARES	25	AACK/	Advanced Acknowledge	26	INH 2/	PROM Inhibit
	27			28		
	29			30		
	31	CCLK/	Constant Clock	32		
	33	INTR/	Direct Interrupt	34		
INTERRUPTS	35	INT6/	Parallel Interrupt Requests	36	INT7/	Parallel Interrupt Requests
	37	INT4/		38	INT5/	
	39	INT2/		40	INT3/	
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/	Address Bus	44	ADRF/	Address Bus
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/		50	ADR9/	
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	[1]	Data Bus	60	[1]	Data Bus
	61	[1]		62	[1]	
	63	[1]		64	[1]	
	65	[1]		66	[1]	
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
		[1]		78	[1]	
	79	VAA	-12VDC	80	VAA	-12VDC
	81	VCC	+ 5VDC	82	VCC	+ 5VDC
	83	VCC	+ 5VDC	84	VCC	+ 5VDC
	85	GND	Signal GND	86	GND	Signal GND

[1] Used by Intellec® MDS Bus.

IORC/ — I/O read command; indicates that the address of an input port has been placed on the system address bus and that the data at that input port is to be read and placed on the system data bus.

IOWC/ — I/O write command; indicates that the address of an output port has been placed on the system address bus and that the contents of the system data bus are to be output to the addressed port.

XACK/ — Transfer acknowledge signal; the required response of an external memory location or I/O port which indicates that the specified read/write operation has been completed. That is, data has been placed on, or accepted from, the system data bus lines.

AACK/ — Advance acknowledge signal; used with 8080 CPU-based systems. AACK/ is an advance acknowledge, in response to memory or I/O access commands, that allows the CPU to proceed with the current instruction cycle.

INH 1/ — RAM Inhibit; generated when PROM memory space is addressed and is used to prevent any RAM that might share that space from responding.

INH 2/ — PROM Inhibit: generated when PROM memory space is addressed for a special function, such as bootstrap routines, and is used to prevent other PROMs from responding.

ADR0/-ADRF/	16 Address lines; used to transmit the address of the memory location or I/O port to be accessed ADRF/ is the most significant bit.
DAT0/-DAT7/	Bidirectional data lines; used to transmit/receive information to/from a memory location or I/O port. DAT7/ is the most significant bit.
INT0/-INT7/	Parallel Interrupt request lines; any one or more of the eight masked interrupt bits or the interrupt flag (INRQ/) can be connected to these eight bus lines via on-board jumpers. These jumpers also allow any desired bit organization among the lines. These lines are independent of the data bus and bus interface logic. Unless blocked by the mask, the interrupt bits can be sampled via these lines without requiring an address or strobe.
INTR/	Direct Interrupt signal; signal line provided to support coded interrupt requests in special applications of system interrupt structure.

5.3 RS232C CABLING

A 26-pin mating connector, 3M 3462-0001, should be attached to the serial I/O Interface edge connector J3 on the SBC-104 and to a 25-wire flat cable, 3M 3349/25. The flat cable is, in turn, attached to the RS232C pin-compatible connector, 3M 3483-1000. Table 5-6 equates the J3 edge connector pins with the associated RS232-compatible pins on the 3M 3483-1000 connector.

TABLE 5-6. J3/RS232C CONNECTOR PIN CORRESPONDENCE

J3 CONNECTOR PIN NO.	RS232C CONNECTOR PIN NO.
1	14
2	1
3	15
4	2
5	16
6	3
7	17
8	4
9	18
10	5
11	19
12	6
13	20
14	7
15	21
16	8
17	22
18	9
19	23
20	10
21	24
22	11
23	25
24	12
26	13

NOTE: The J3 pin numbers refer to pin assignments shown on the SBC-104 board at J3.

CHAPTER 6

COMPATIBLE EQUIPMENT

The SBC-104 is designed to interface directly with any SBC-80 single board computer via the system bus. It is mechanically compatible with both Intellec® MDS chassis requirements and SBC-604 and SBC-614 4-module card holder, designed specifically for OEM applications. Details are presented in the following section.

6.1 SBC-80/10

The SBC-80/10 is completely compatible with the SBC-104 OEM Combination Memory and I/O Board module. The SBC-80/10 can be interfaced with up to 10 combination modules. Table 6-1 summarizes access characteristics of the SBC-104.

The board includes a CPU chip set, 48 programmable I/O lines, an RS232C or TTY communications interface, 1K bytes of RAM memory, capacity for up to 4K bytes of EPROM/ROM memory, system clock, bus control logic and bus driver/receiver networks.

When using an SBC-104 with the SBC-80/10 care should be taken when assigning RAM and PROM memory addresses. The SBC-80/10 has fixed memory locations assigned to RAM (3C00-3FFF) and PROM (0000-0FFF). If the SBC-104 addresses are selected to overlap these locations, improper operation will result.

6.2 MASTER MODULES

The SBC-104 can operate in systems containing more than one master module.

TABLE 6-1. SBC-104 ACCESS CHARACTERISTICS WHEN USED WITH SBC-80/10 CPU

MODULE	INSTRUCTION	CPU CYCLES		CPU WAIT STATES		CYCLE TIME (μsec)		REFRESH DEGRADATION RAM	
		MIN	MAX	MIN	MAX	MIN	MAX*	MIN	MAX
COMBINATION	MR	8	8	1	1	3.9	4.4	0	+1
	MW	9	9	2	2	4.4	4.9	0	+1
	IOR	11	11	1	1	5.4	----		
	IOW	12	12	2	2	5.9	----		

*Includes maximum refresh degradation.

REFERENCE:

MR	MEMORY READ:	MOV A,M	7 CYCLES
MW	MEMORY WRITE:	MOV M,A	7 CYCLES
IOR . . .	I/O READ:	IN Addr	10 CYCLES
IOW . . .	I/O WRITE:	OUT Addr . . .	10 CYCLES

6.3 MODULAR BACKPLANE AND CARDCAGE

The SBC-604/614 Modular Backplane and Cardcage is designed specifically for OEM modules such as the SBC-104. Each card holder supports up to 4 modules. The modules may be electrically and mechanically "ganged" together for expanded capability. Provisions for power supply distribution, air circulation and bus exchange functions are featured on the OEM card holders.

6.4 INTELLEC®MDS CARDCAGE

The SBC 104 is physically and electrically compatible with the Intellec MDS bus except as noted below. The interface signals required by the SBC 104 (Table 5-5) are a subset of the Intellec MDS bus signal requirements.

6.4.1 POWER SUPPLIES

Intellec MDS power supplies do not support a -5V supply although a -5V bus conductor is built into the cardcage motherboard. An auxiliary power supply or converter (to convert -10V to -5V) connected to this line will suffice.

6.4.2 INHIBIT OPERATIONS

In order to minimize the access time for PROM read operations, the SBC 104 does not artificially delay the acknowledge signal to meet the Intellec MDS bus specification of 1200 ns. Therefore, in order to overlap RAM with SBC 104 PROM the setup time of INH1/ to command (t_{IS}) of the RAM board must be less than the bus master address setup time (t_{AS}) minus the inhibit delay time (t_{ID}) of the SBC 104. This would guarantee that the RAM operation would be blocked completely. Alternatively the RAM board may still be overlapped if the inhibit hold time (t_{IH}) of RAM is less than the SBC 104 inhibit hold time (t_{IHC}) or less than the minimum interval between memory commands on the bus.

CHAPTER 7

SBC-104 SPECIFICATIONS

7.1 DC POWER REQUIREMENTS

DC Power Requirements are given in Table 7-1.

7.2 AC CHARACTERISTICS

AC Characteristics are given in Table 7-2 and Figures 7-1 and 7-2.

7.3 DC CHARACTERISTICS

DC Characteristics are given in Table 7-3.

7.4 ENVIRONMENT

Temperature extremes can cause instability, or result in permanent damage to the circuits on the module. Ambient temperature must, therefore, be maintained within the limits of 0°C to 55°C. Exercise caution in locating the module, giving particular attention to radiant and conducive sources of heat. Remember that the module itself, when installed, will contribute some heat to the environment. Maintain an adequate clearance to permit the convective dissipation of heat from the elements on the card.

Relative humidity should not exceed 90%, non-condensing.

7.5 SBC-104 BOARD OUTLINE

See Figure 7-3.

TABLE 7-1. DC POWER REQUIREMENTS
(MAIN POWER AND BATTERY BACKUP)

A. MAXIMUM AVERAGE CURRENT

	[1]	[2]
V_{CC} = +5V ± 5%	I_{CC} = 3.6A max.	I_{CC} = 2.85A max.
V_{DD} = +12V ± 5%	I_{DD} = 700mA max.	I_{DD} = 450mA max.
V_{BB} = -5V ± 5%	I_{BB} = 180mA max.	I_{BB} = 3mA max.
V_{AA} = -12V ± 5%	I_{AA} = 60mA max.	I_{AA} = 60mA max.

Notes: [1] The values assume that four 8708 PROM's are present and that eight optional 220/330 Ω termination networks being driven low have been installed in the Parallel I/O Interface. These values include RAM power requirements. If the auxiliary power jumpers are removed, the bus power is reduced by the amounts shown in Table 7-1B below.

[2] These values assume that the 8708 PROM's and optional termination networks are not present.

B. BATTERY BACKUP POWER

V_{CC} = +5V ± 5%	600mA max.
V_{DD} = +12V ± 5%	400mA max.
V_{BB} = -5V ± 5%	3mA max.
V_{AA} = -12V ± 5%	-----

TABLE 7-2. SBC 104/108 AC CHARACTERISTICS

RAM READ OR WRITE

PARAM-ETER	MIN ns	MAX ns	DESCRIPTION	REMARKS
t_{AS}	50		Address Setup to Command	
t_{DS}	-145		Write Data Setup to Command	From Data to Command
*t_{AAK}	100	220	Command to Advanced Acknowledge Time	Jumper W7A → W7E
*t_{ACK}		610	Command to Transfer Acknowledge Time	
t_{AH}	0		Address Hold Time	
t_{DH}	0		Write Data Hold Time	
t_{DHR}	0		Read Data Hold Time	
t_{TO}		65	Acknowledge Turn Off Delay	
*t_{ACC}		575	Access Time to Read Data	
*t_{CY}		675	Minimum Cycle Time	$t_{ACK} + t_{TO}$
t_{RD}	0	590	Refresh Delay Time	
t_{RI}	12.4µs	15.6µ	Refresh Interval	14µs typical
t_{IS}	0		Inhibit Setup Time	To Block Cycle
t_{IH}	475		Inhibit Hold Time	To Block XACK

*Since Refresh is asynchronous, t_{RD} may be added to t_{AAK}, t_{ACK}, t_{ACC}, t_{CY}.

PROM READ

t_{AS}	50		Address Setup to Command	
t_{AAK}	95	206	Command to Advanced Acknowledge Time	
t_{ACK}	470	595	Command to Transfer Acknowledge Time	
t_{AH}	0		Address Hold Time	
t_{DHR}	0		Read Data Hold Time	
t_{TO}		90	Acknowledge Turn Off Delay	
t_{ACC}		465	Access Time to Read Data	
t_{CY}	560	685	Minimum Cycle Time	$t_{ACK} + t_{TO}$
t_{ID}		62	Address to INH1/	
t_{IHC}	495		Inhibit Hold Time	

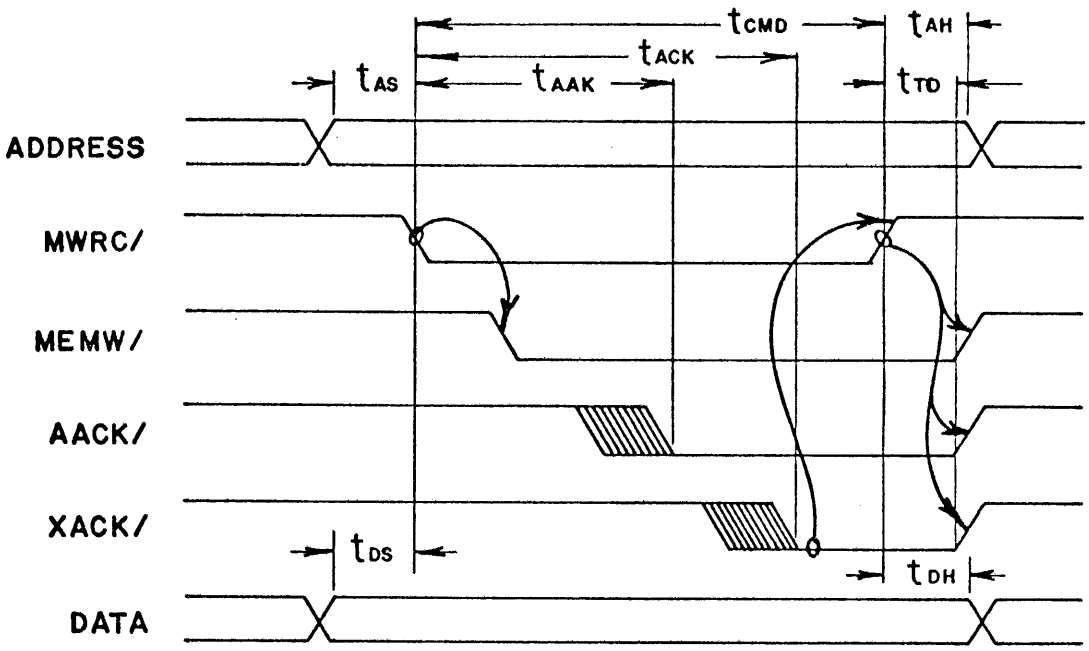
TABLE 7-2. SBC 104/108 AC CHARACTERISTICS (CONTINUED)

I/O READ OR WRITE

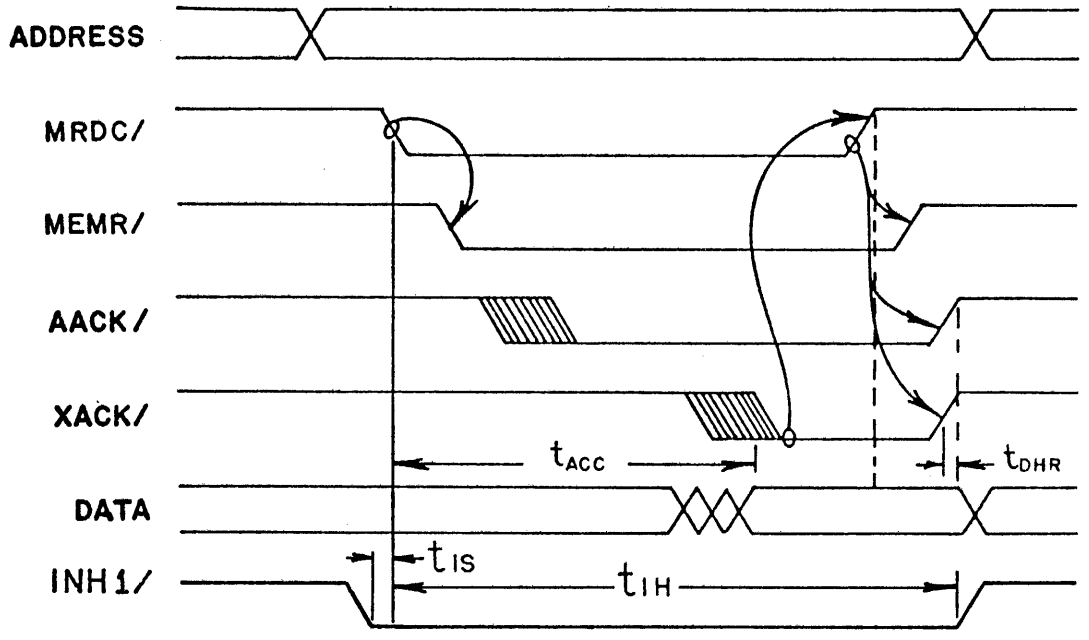
PARAM-ETER	MIN ns	MAX ns	DESCRIPTION	REMARKS
t_{AS}	50		Address Setup to Command	
t_{DS}	50		Write Data Setup to Command	
t_{AAK}	105	243	Command to Advanced Acknowledge Time	Jumper W1-H → W1-E
t_{ACK}		630	Command to Transfer Acknowledge Time	
t_{AH}	50		Address Hold Time	
t_{DH}	50		Write Data Hold Time	
t_{DHR}	0		Read Data Hold Time	
t_{TO}		130	Acknowledge Turn Off Delay	
t_{ACC}		395	Access Time to Read Data	
t_{CY}		760	Minimum Cycle Time	$t_{ACK} + t_{TO}$

INTERVAL TIMER INTERRUPT

t_{INV1}	1.002 ms	1.004 ms	Interval Timer Interrupt Period	Baud Rate = 110
t_{INV2}	1.041 ms	1.043 ms	Interval Timer Interrupt Period	Baud Rate = 110

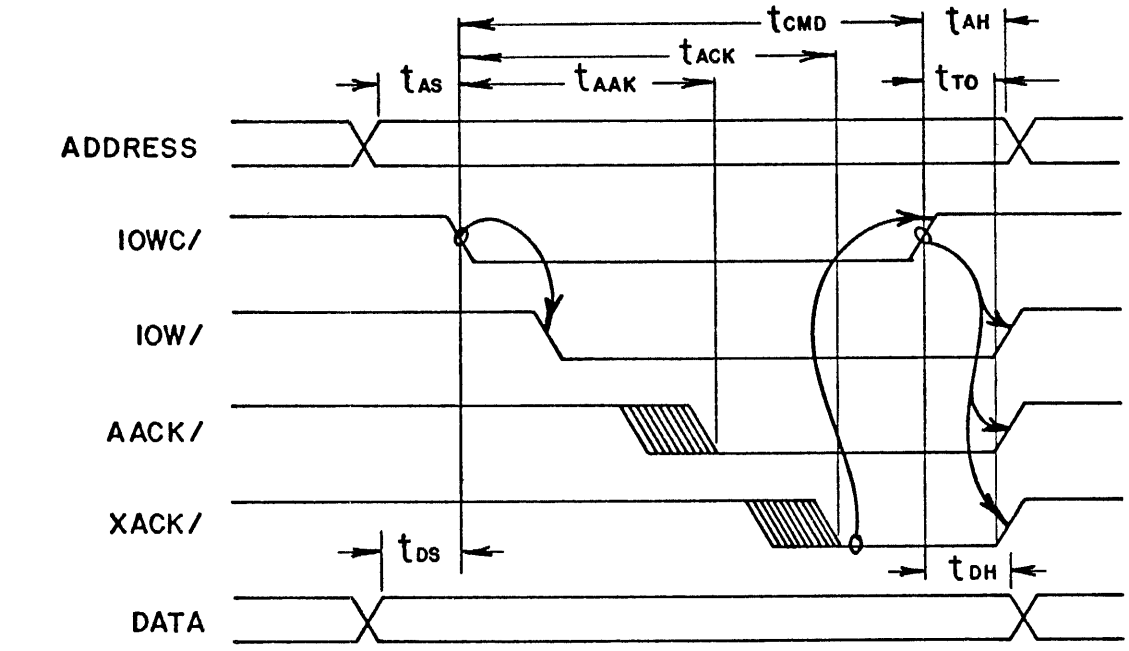


RAM WRITE

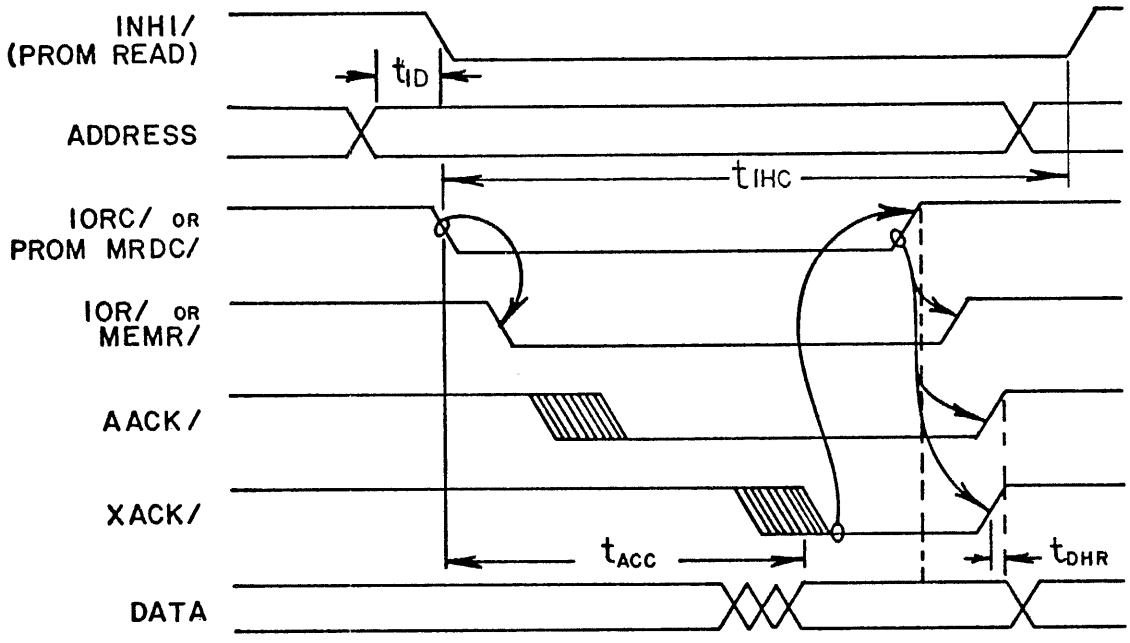


RAM READ

FIGURE 7-1



A. WRITE TO I/O PORT



B. READ PROM OR I/O PORT

FIGURE 7-2

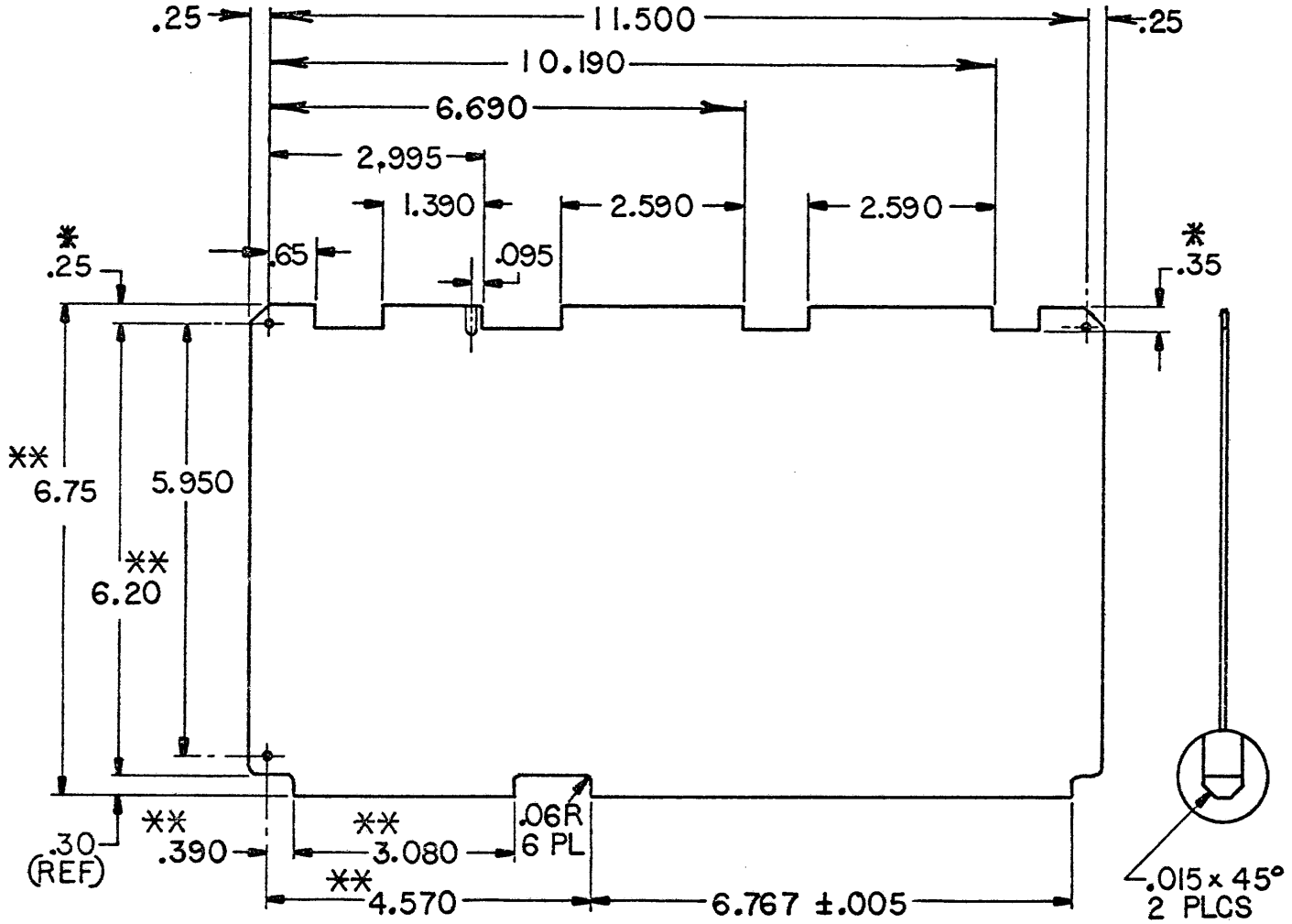
TABLE 7-3. SBC-104 DC CHARACTERISTICS

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
ADRØ/-ADRF/	V_{IL}	Input Low Voltage			0.8	V
ADDRESS	V_{IH}	Input High Voltage		2.0		V
INIT/	I_{IL}	Input Current at Low V	V_{IN} = 0.4		-0.36	mA
(74LS04)	I_{IH}	Input Current at High V	V_{IN} = 2.7V		20	µA
	*C_L	Capactive Load			18	pF
AACK/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.4	V
XACK/	V_{OH}	Output High Voltage	I_{OH} = -5.2 mA	2.4		V
(8097)	I_{LH}	Output Leakage High	V_0 = 2.4		40	µA
	I_{LL}	Output Leakage Low	V_0 = 0.4		-40	µA
	*C_L	Capacitive Load			15	pF
DATØ/-DAT7/	V_{OL}	Output Low Voltage	I_{OL} = 50 mA		0.6	V
(8226)	V_{OH}	Output High Voltage	I_{OH} = -10 mA	2.4		V
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45		-0.25	mA
	I_{LH}	Output Leakage High	V_0 = 5.25		100	µA
	*C_L	Capacitive Load			18	pF
MEMORY PROTECT/	V_{IL}	Input Low Voltage			0.8	V
(74LS74)	V_{IH}	Input High Voltage		2.0		V
10K P.U.	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-.89	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.5V		.18	mA
	*C_L	Capacitive Load			18	pF
IOWC/, IORC/	V_{IL}	Input Low Voltage			0.8	V
MWTC/, MRDC/	V_{IH}	Input High Voltage		2.0		V
INH2/	I_{IL}	Input Current at Low V	V_{IN} = 0.5		-2.0	mA
(74S04)	I_{IH}	Input Current at High V	V_{IN} = 2.7V		50	µA
	*C_L	Capacitive Load			18	pF

TABLE 7-3. SBC-104 DC CHARACTERISTICS (Continued)

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
INHI/	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
7400/7407	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = .4		-1.6	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.5		1	mA
	*C_L	Capacitive Load			22	pF
INTR/	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
INTO/-INIT/	V_{OH}	Output High Voltage	OPEN COLLECTOR			
(7407)	*C_L	Capacitive Load			18	pF
EXT INT 1/	V_{IL}	Input Low Voltage			0.8	V
EXT INT 2/	V_{IH}	Input High Voltage		2.0		V
(7404)	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-6.6	mA
(1K P.U.)	I_{IH}	Input Current at High V	V_{IN} = 5.5V		1.75	mA
	*C_L	Capacitive Load			18	pF
PORT D4,D8	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		.45	V
BIDIRECTIONAL	V_{OH}	Output High Voltage	I_{OH} = -12 mA	2.4		V
DRIVERS	V_{IL}	Input Low Voltage			.95	V
(8226)	V_{IH}	Input High Voltage		2.0		V
(1K P.U.)	I_{IL}	Input Current at Low V	V_{IN} = 0.45		-5.05	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		.60	mA
	*C_L	Capacitive Load			18	pF
8255	V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		.4	V
DRIVER/ RECEIVER	V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.4		V
	V_{IL}	Input Low Voltage			.8	V
	V_{IH}	Input High Voltage		2.0		V
	*C_L	Capacitive Load			18	pF

*Capacitance values are approximations only.



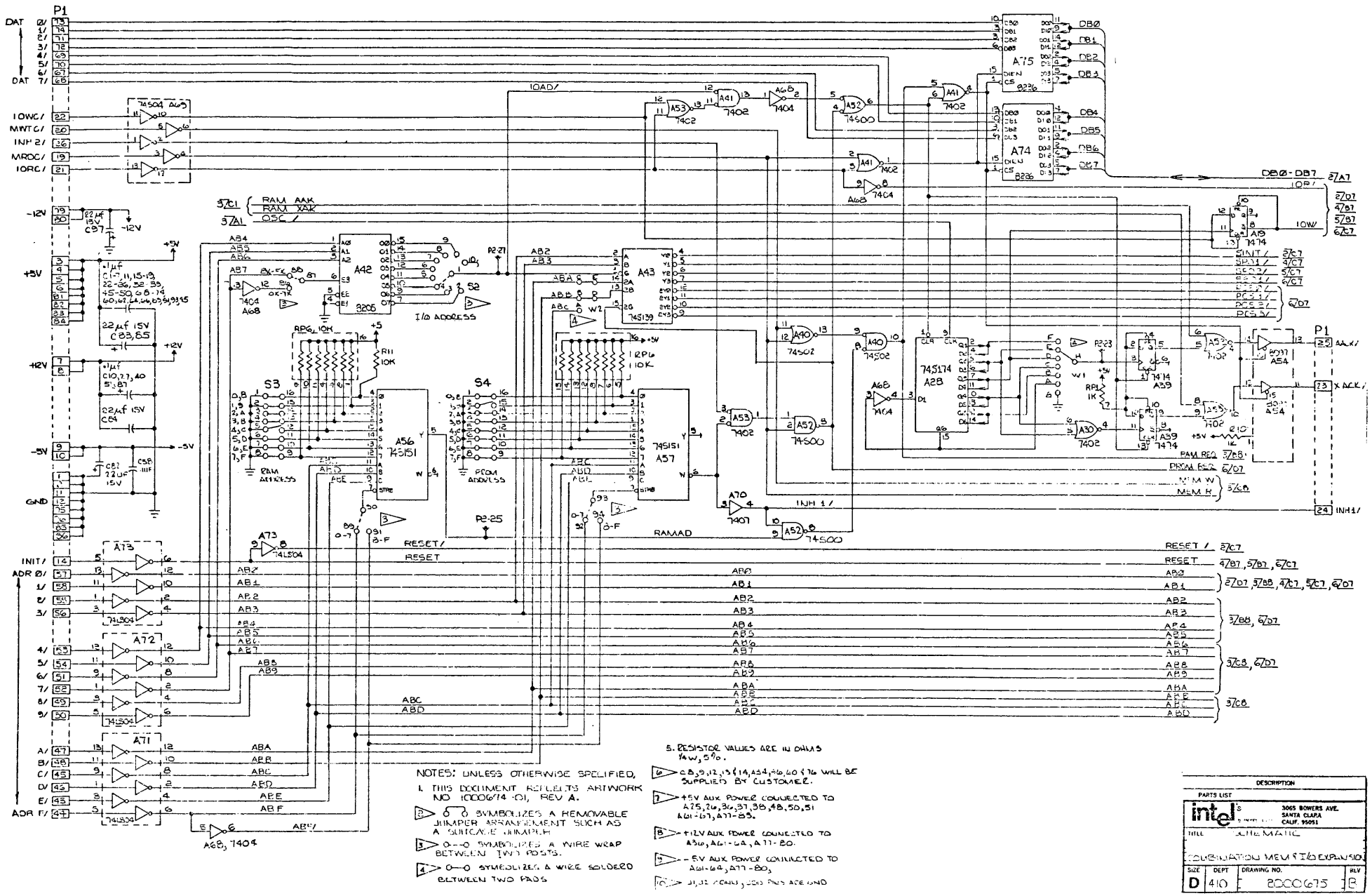
UNMARKED DIMENSIONS ARE ±.005
* THIS DIM. ±.02
** THIS DIM. ±.010
ALL DIMENSIONS ARE FOR REF ONLY AND ARE SUBJECT TO CHANGE

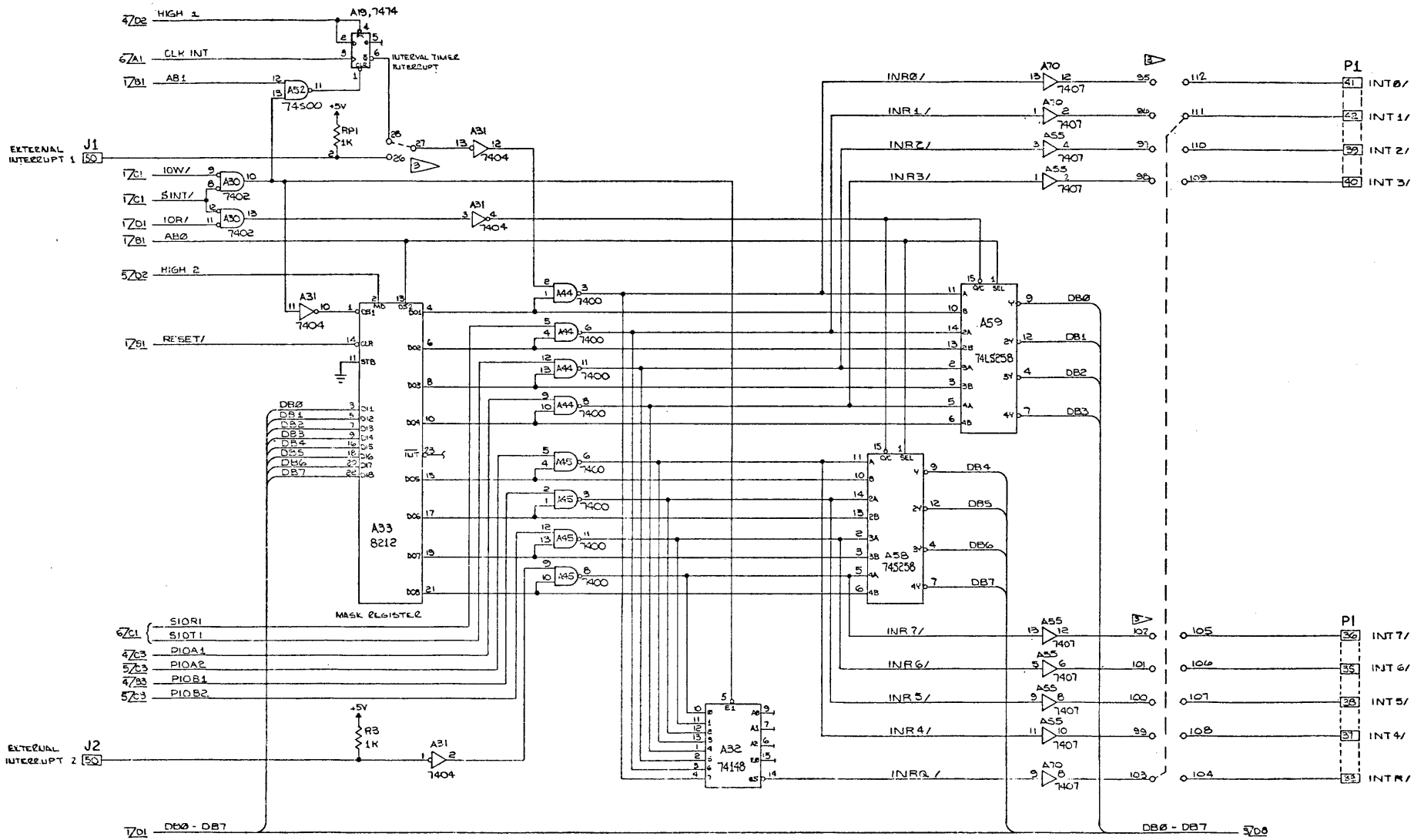
FIGURE 7-3. BOARD OUTLINE DRAWING

APPENDIX A

SBC 104/108 SCHEMATICS

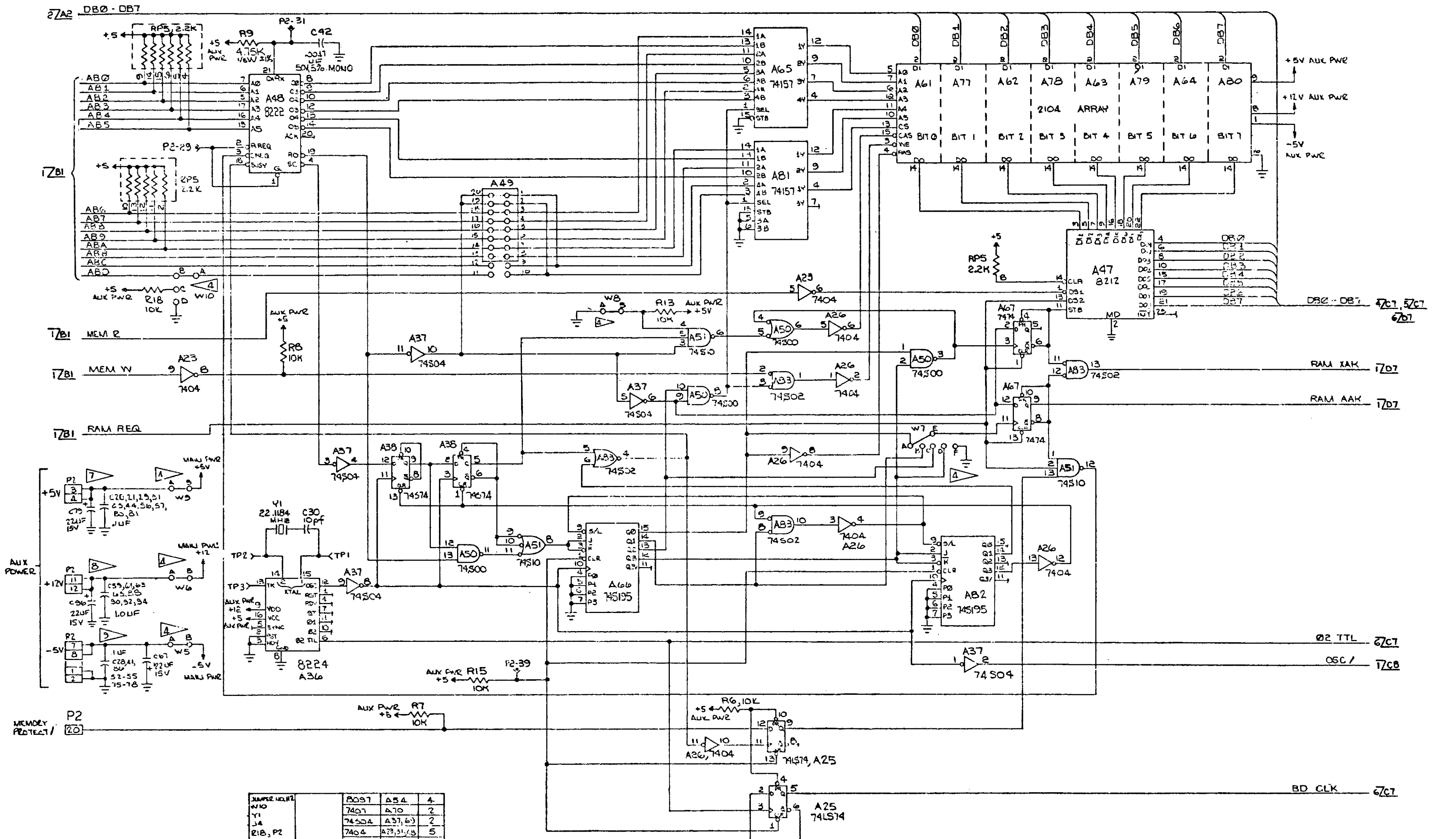
Schematic drawings for the SBC 104 and 108 are provided in this appendix. Information and diagrams in this section are subject to change without notice. References should be made to schematics shipped with this module.


P1
DAT Ø/
DAT 7/
IOWC/
MWTC/
INH 2/
MRDC/
IORC/
-12V
+5V
+12V
-5V
GND
RAM AAK
RAM XAK
OSC /
IOAD/
I/O ADDRESS
RAM ADDRESS
PROM ADDRESS
RESET/
RESET
RAMAD
INH 1/
A42
A43
A56
A57
A73
A72
A71
A75
A74
A68, 7404
DB0 - DB7
IOR/
IOW/
RAM REQ
PROM REQ
MEM W
MEM R
AAK/
XACK/
INH1/
NOTES: UNLESS OTHERWISE SPECIFIED,
1. THIS DOCUMENT REFLECTS ARTWORK NO 100006714-01, REV A.
2. SYMBOLIZES A REMOVABLE JUMPER ARRANGEMENT SUCH AS A SUNCASE JUMPER.
3. SYMBOLIZES A WIRE WRAP BETWEEN TWO POSTS.
4. SYMBOLIZES A WIRE SOLDERED BETWEEN TWO PADS
5. RESISTOR VALUES ARE IN OHMS 1/4W, 5%.
6. C8,9,12,13 & 14,A24,A36,40 & 76 WILL BE SUPPLIED BY CUSTOMER.
7. +5V AUX POWER CONNECTED TO A75,26,36,37,38,48,50,51 A61-67, A77-83.
8. +12V AUX POWER CONNECTED TO A36, A61-64, A77-80.
9. -5V AUX POWER CONNECTED TO A61-64, A77-80.
10. 21,22 (GND), 2,3,83 PINS ARE GND
DESCRIPTION
PARTS LIST
intel
3065 BOWERS AVE.
SANTA CLARA
CALIF. 95051
TITLE SCHEMATIC
COMBINATION MEM & I/O EXPANSION
SIZE D
DEPT 410
DRAWING NO. 20000675
REV B



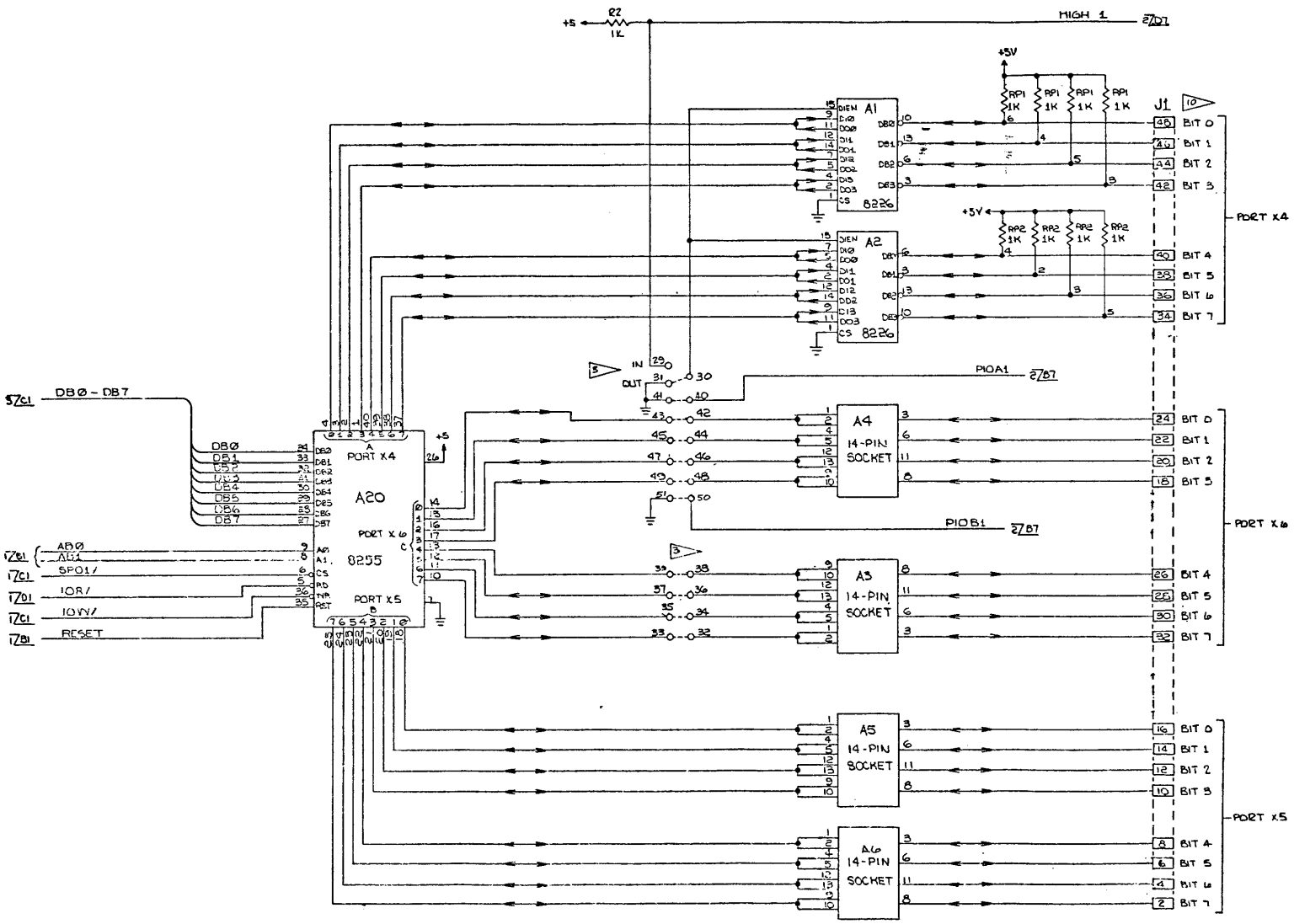
A-3

SCALE:	SIZE	DEPT	DRAWING NO.	REV
SHEET 2 OF 6	D	410	2000675	B

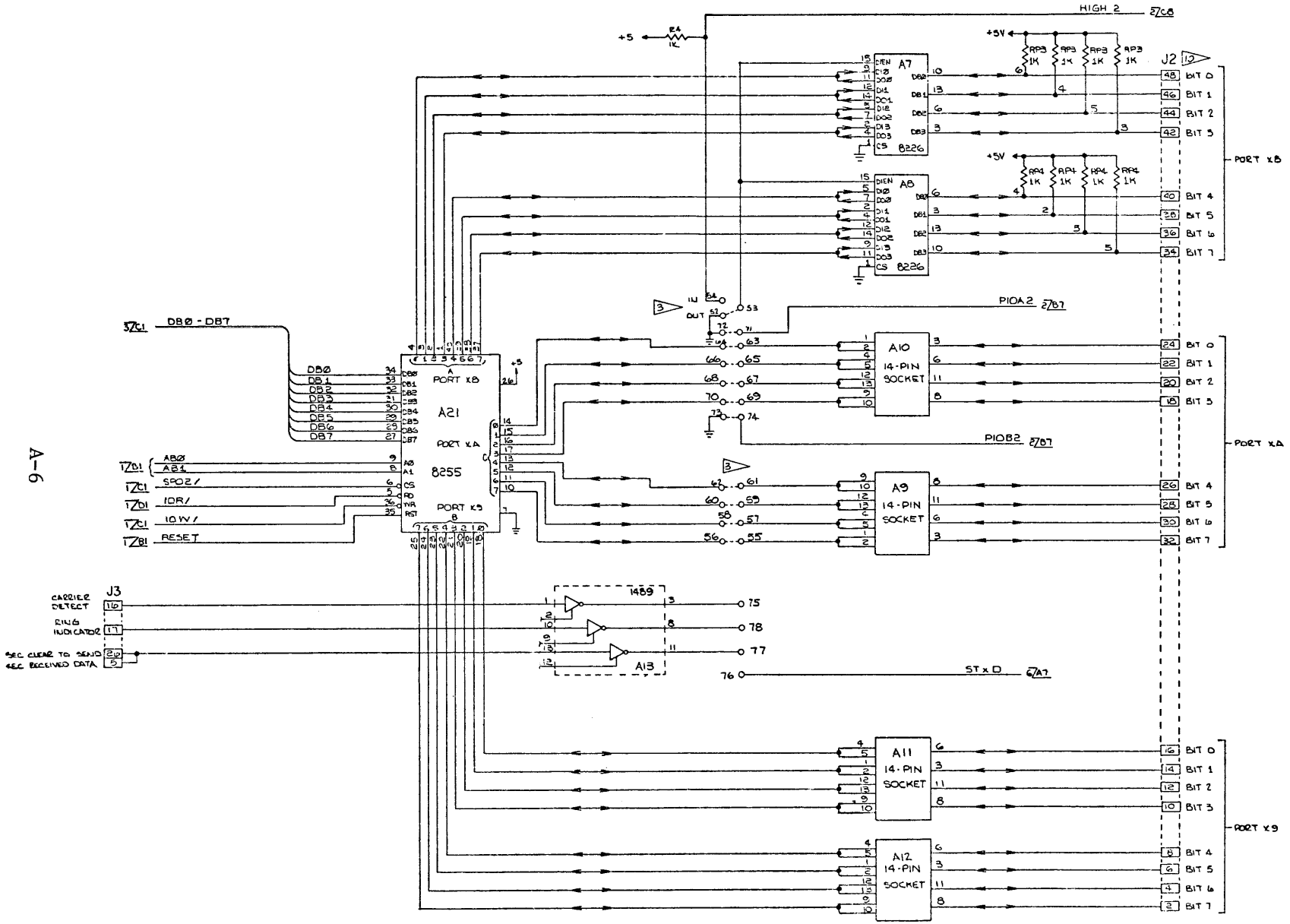


JUMPER HOLE W10 Y1 J4 R18, P2 C57, RP6 AB3, 54	A18, 24, 25	8097	A54	4
		7407	A70	2
		74S04	A37, 69	2
		7404	A23, 31, 68	5
		74S02	A40	2
		7402	A30, 41	2
LAST USED	NOT USED	TYPE	REF DESIG	QTY
REF DESIGNATION		SPEC GATES		

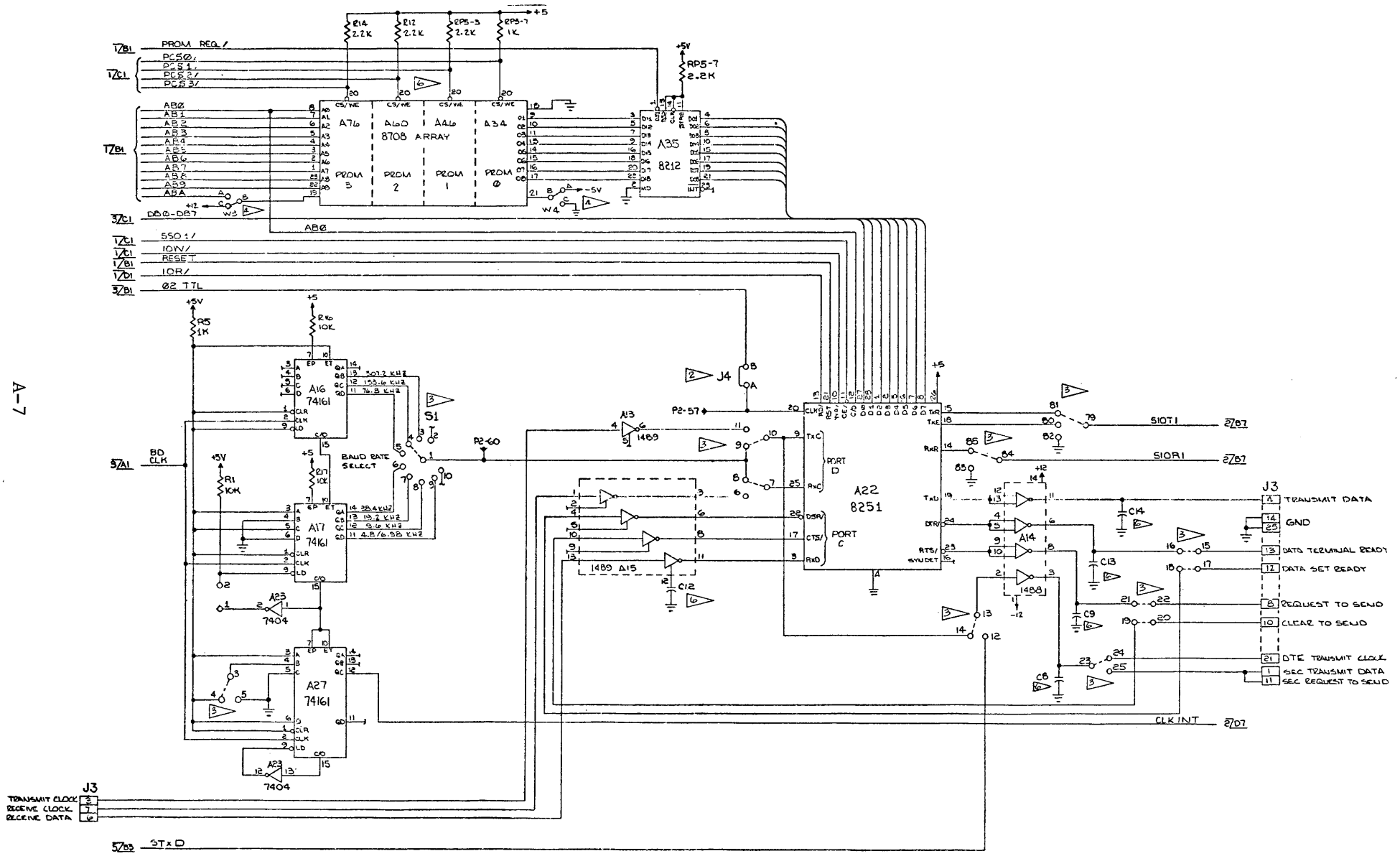
SCALE: —	SIZE	DEPT	DRAWING NO.	REV
SHEET 3 OF 6	D	410	2000675	3



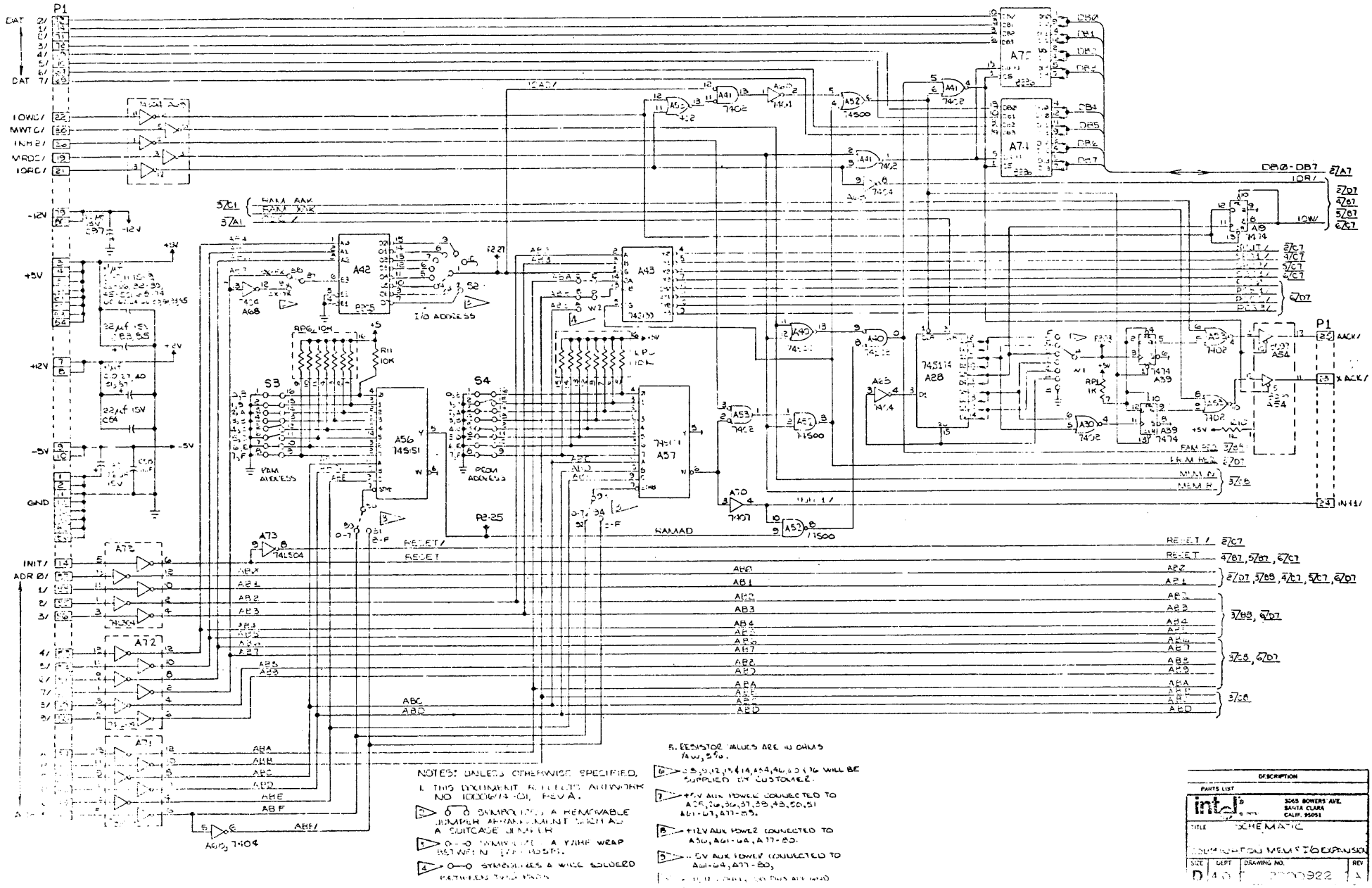
SCALE:	SIZE	DEPT	DRAWING NO.	REV
SHEET 4 OF 6	D	410	2000675	B

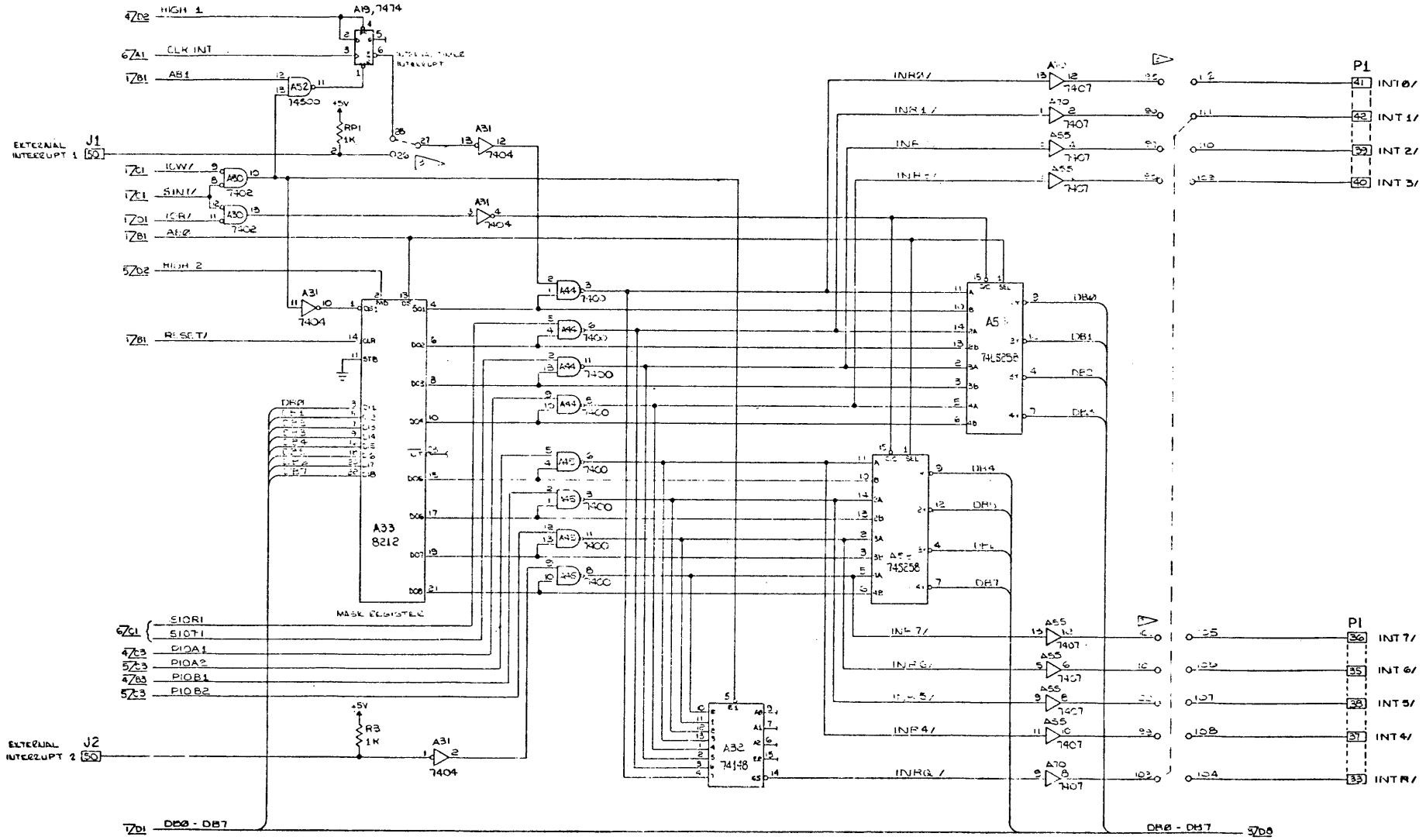


SCALE: —	SIZE	DEPT	DRAWING NO.	REV
SHEET 5 OF 6	D	410	2000675	13

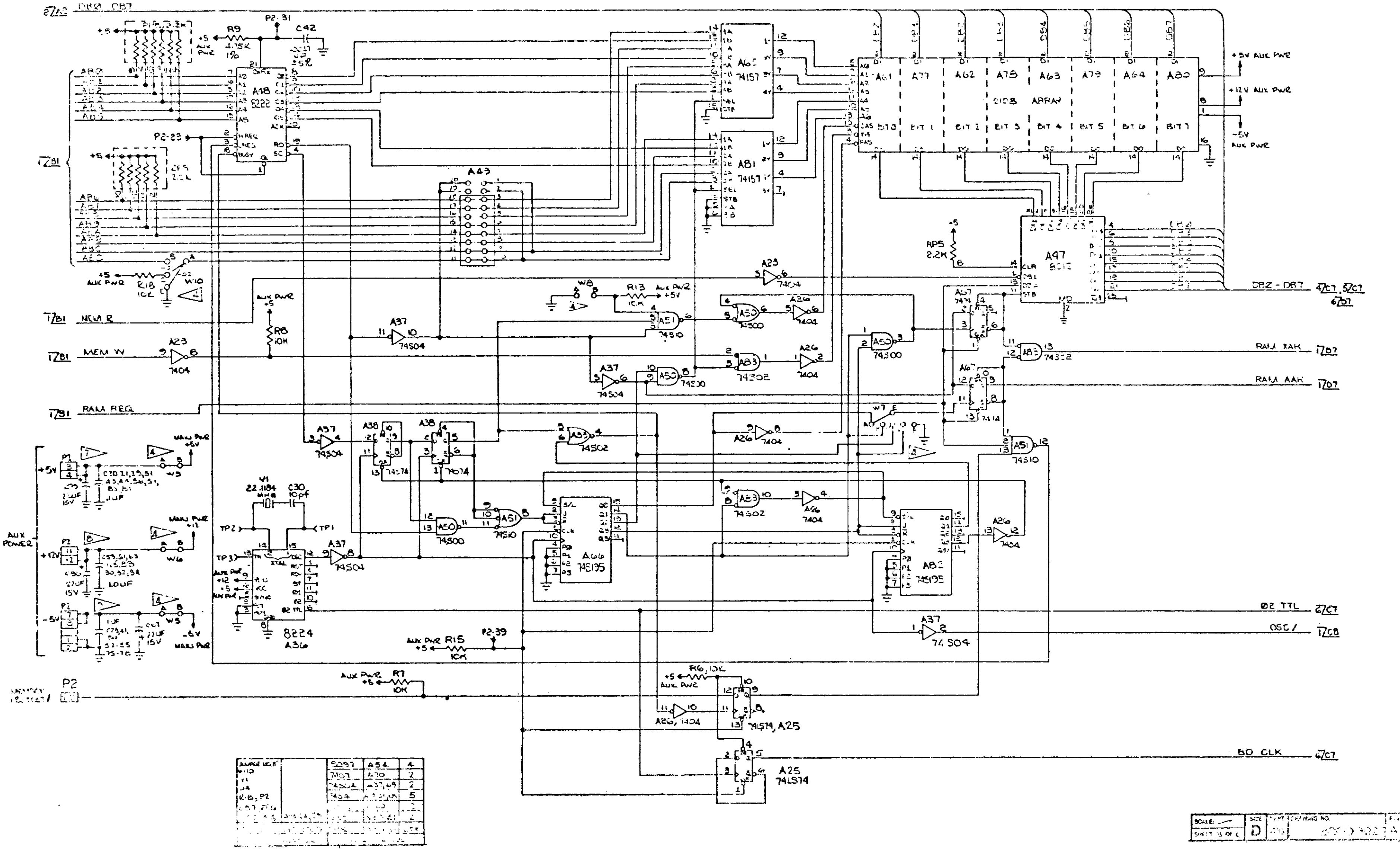


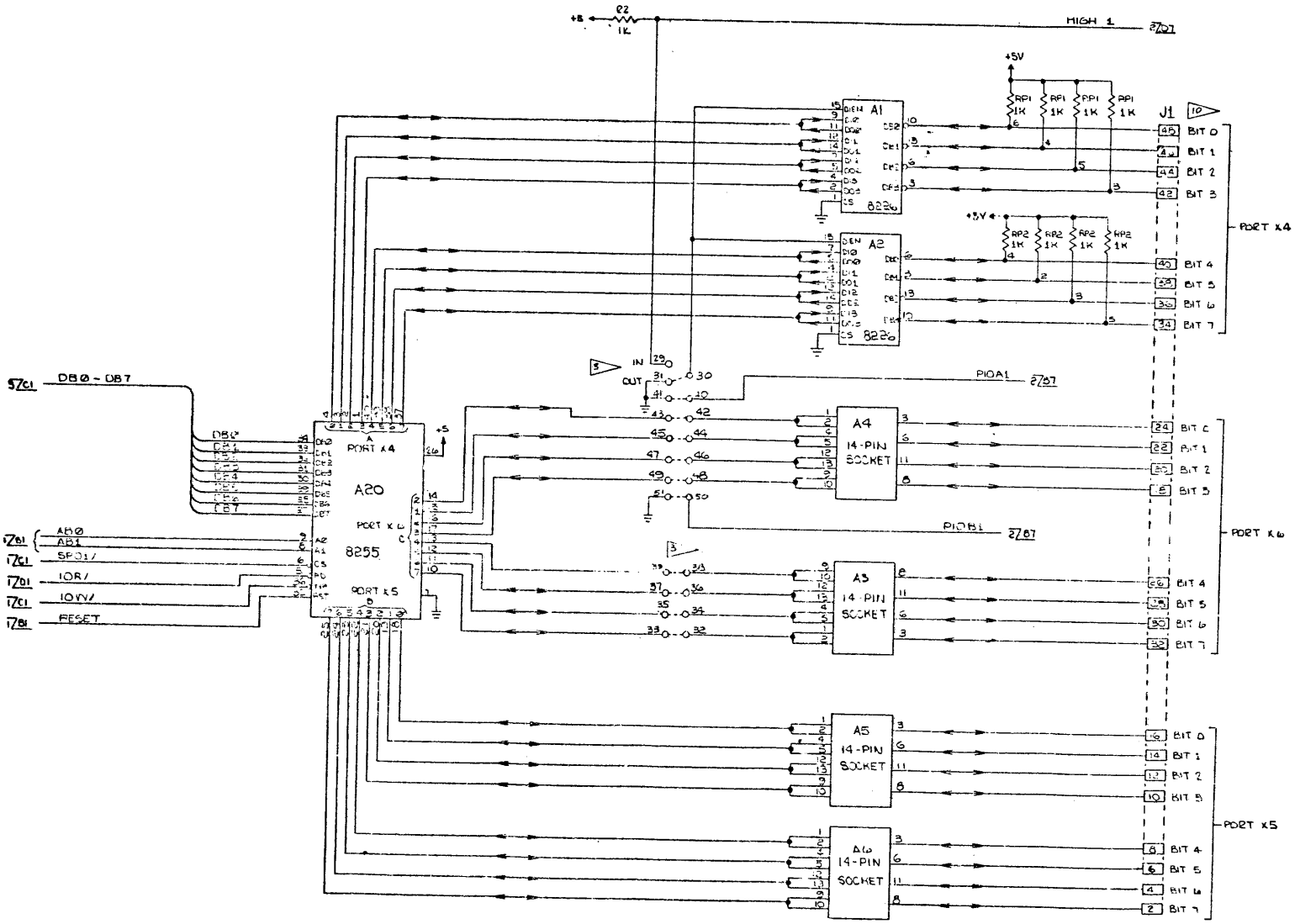
SCALE: —	SIZE	DEPT	DRAWING NO.	REV
SHEET 6 OF 6	D	110	2000675	B

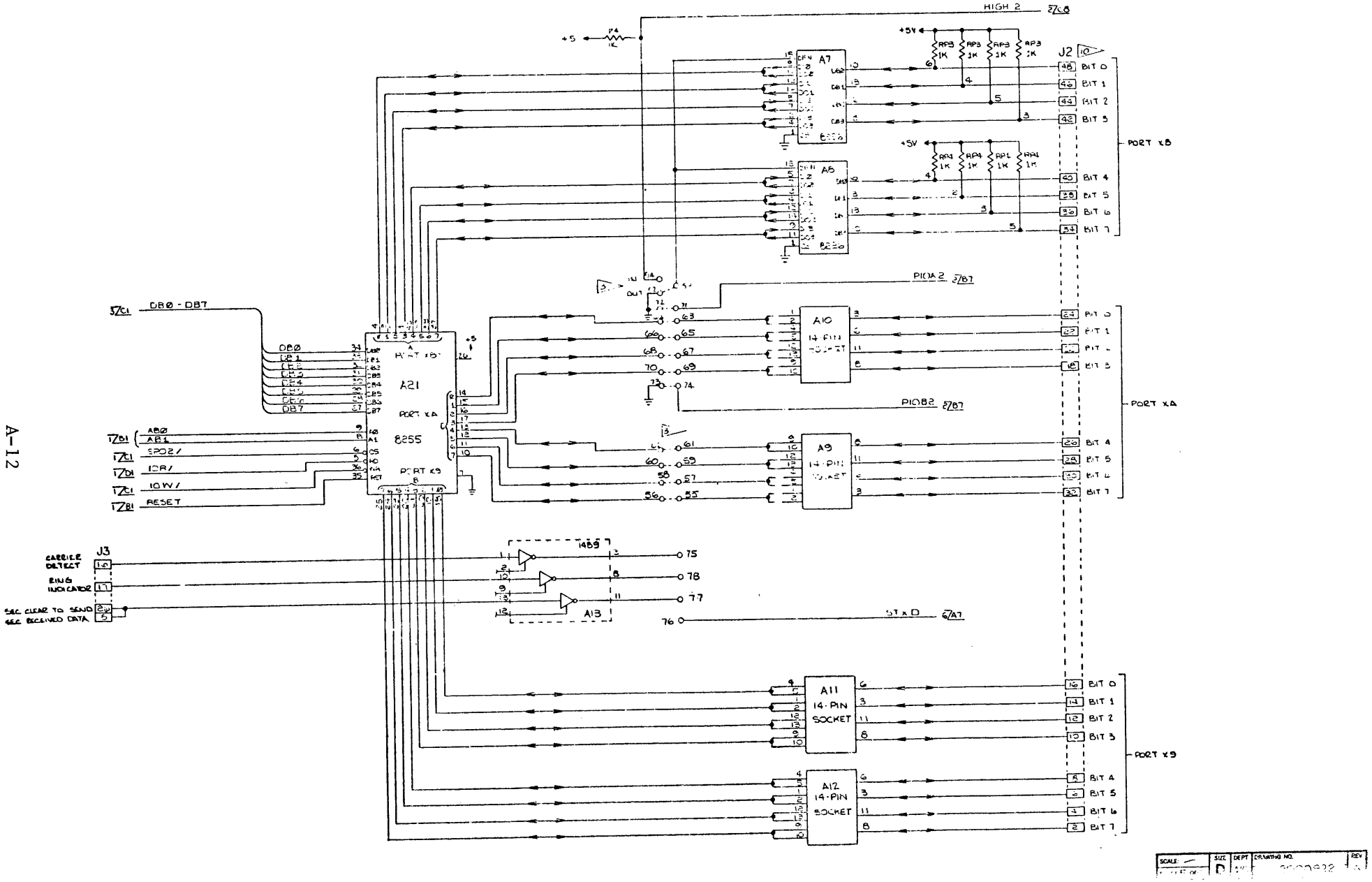

P1
DAT
IOWC/
MWTC/
INH2/
MRDC/
IORC/
-12V
+5V
+12V
-5V
GND
INIT/
ADR 0/
I/O ADDRESS
S3
S4
RAM ADDRESS
PROM ADDRESS
RESET/
RAMAD
DB0-DB7
IOR/
IOW/
MWTC/
MRDC/
INH2/
AACK/
XACK/
IN41/
ABA
ABB
ABC
ABD
ABE
ABF
NOTES: UNLESS OTHERWISE SPECIFIED,
1. THIS DOCUMENT REFLECTS ARTWORK NO. 100016/4-001, REV A.
5. RESISTOR VALUES ARE IN OHMS 1/4W, 5%.
SCHEMATIC
SBC 108 SCHEMATIC

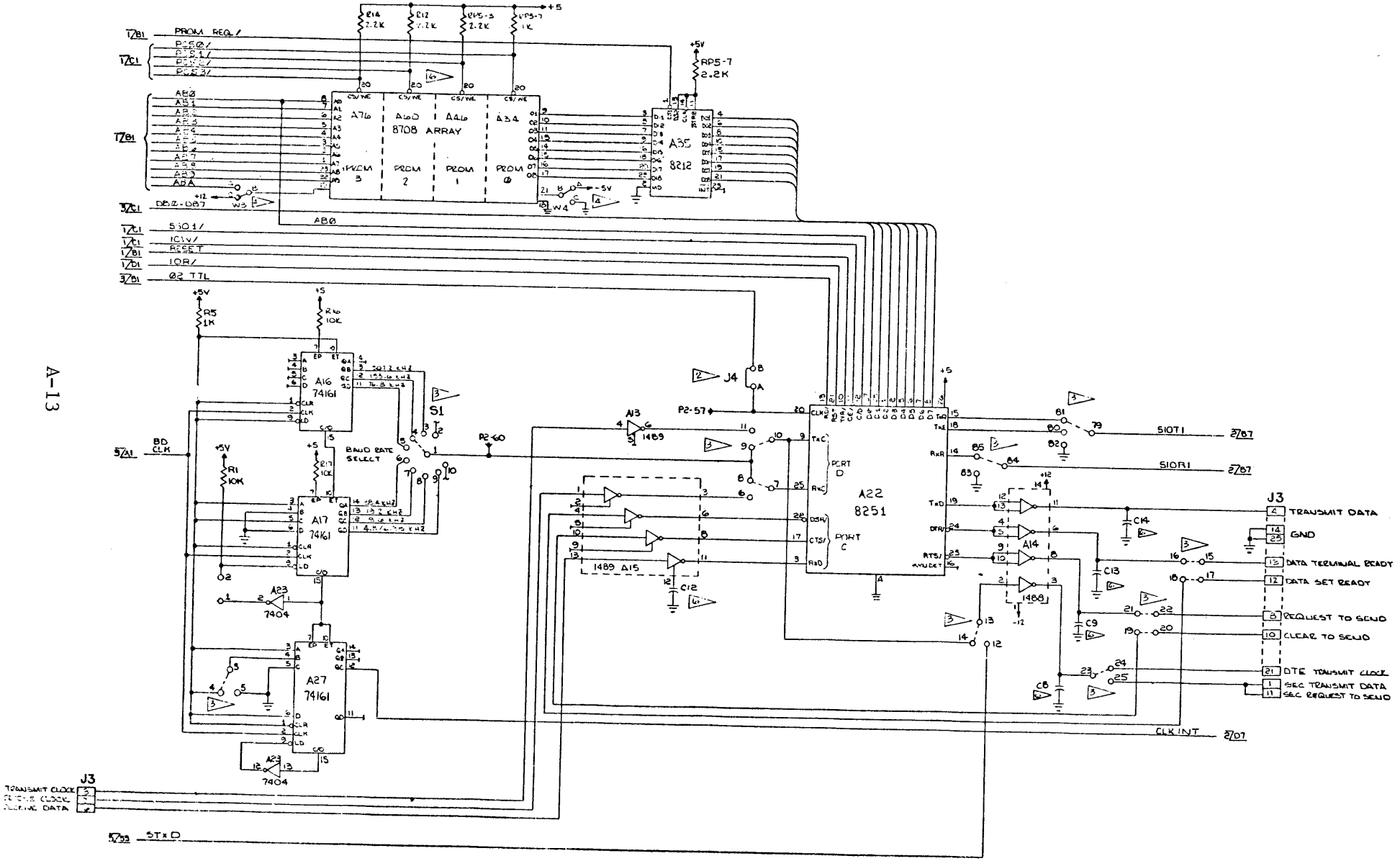


SCALE:	SIZE	DEPT	DRAWING NO.	REV
SHEET 2 OF 6	D	110	2000922	A


DB0 - DB7
A18
8222
A49
A60
74157
A81
74157
A61
A77
A62
A78
A63
A79
A64
A80
2108 ARRAY
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
+5V AUX PWR
+12V AUX PWR
-5V AUX PWR
A47
8212
RP5
2.2K
MEM R
MEM W
RAM REQ
RAM XAK
RAM AAK
A66
74S195
A82
74S195
8224
A36
22.1184 MHz
C30
10pf
AUX POWER
Ø2 TTL
OSC /
BD CLK
A25
74LS74
R15
10K
R7
10K
P2


R2
1K
+5
HIGH 1
Z07
+5V
RP1
1K
A1
8226
J1
BIT 0
BIT 1
BIT 2
BIT 3
PORT x4
RP2
A2
BIT 4
BIT 5
BIT 6
BIT 7
IN
OUT
PIOA1
Z07
DB0 - DB7
Z01
A20
PORT x4
PORT x6
PORT x5
8255
A4
14-PIN
SOCKET
PIOB1
A5
A6
AB0
AB1
SP01/
IOR/
IOW/
RESET


HIGH 2
+5
A7
A8
J2
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
PORT xB
PIOA 2
PIOB2
A10
A9
PORT xA
DB0 - DB7
A21
8255
PORT xA
PORT xB
PORT xC
RESET
CARRIER DETECT
RING INDICATOR
SEC CLEAR TO SEND
SEC RECEIVED DATA
J3
1489
A13
STxD
A11
14-PIN SOCKET
A12
14-PIN SOCKET
PORT x9



SCALE: —	SIZE D	DEPT 710	DRAWING NO 2000122	REV
SHEET 6 OF 6				

APPENDIX B

SBC-901, SBC-902 SCHEMATICS

Schematic drawings for the SBC-901 and SBC-902 are provided in this appendix. Information and diagrams in this section are subject to change without notice.

RESISTOR NETWORK SPECIFICATIONS:

RESISTANCE VALUES:
±2% (MAX)

OPERATING TEMPERATURE:
0°C TO +70°C

TEMPERATURE COEFFICIENT:
±200 PPM/°C OVER TEMPERATURE RANGE OF 0°C TO +70°C

OPERATING VOLTAGE:
6.0 VDC (MAX)

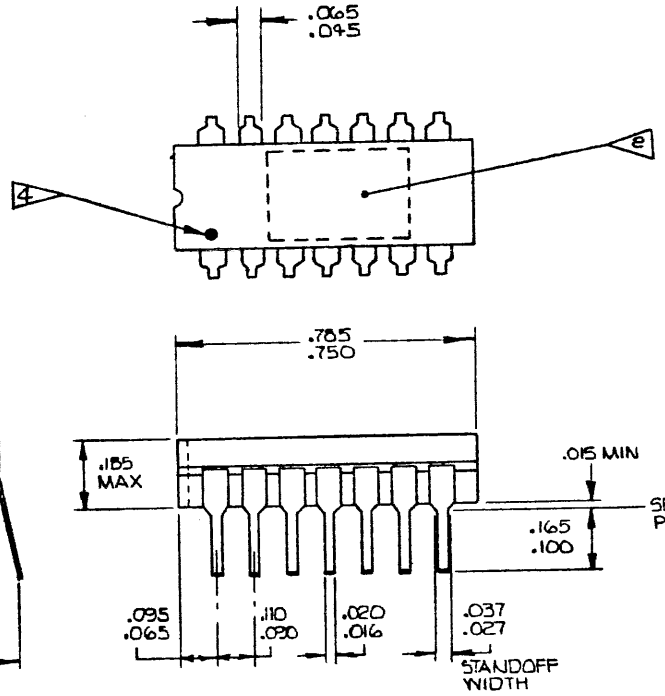
POWER RATING:
AT 70°C, 0.7 WATT PER PACK

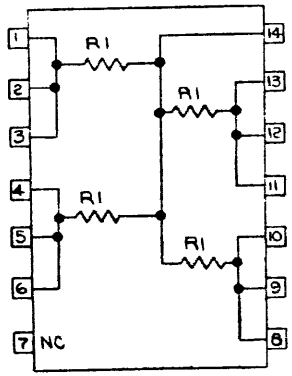
TRACKING RESISTANCE RATIO:
±1.0% (MAX)

STABILITY:
±1% YEAR (MAX)

LOAD LIFE:
±1% (ΔR) OVER 1000 HOURS

PACKAGE:
DUAL IN LINE - CERAMIC OR PLASTIC





NOTES:
UNLESS OTHERWISE SPECIFIED,

1. PART NO IS 4500645-01.

2. INK STAMP PRODUCT CODE, RESISTOR VALUE, PART NO AND DASH NUMBER WITH CONTRASTING COLOR AND MIN .12 HIGH CHARACTERS. NO OTHER MARKINGS ARE PERMITTED EXCEPT FOR MANUF BATCH NO.

E.G.) SBC-902
R 1K
4500645-01

3. FOR PROCUREMENT SEE LV4500645

4. IDENTIFY PIN ONE CLEARLY ON TOP OF PACKAGE.

DESCRIPTION			
PARTS LIST			
intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051			
TITLE: TERMINATING PACK PULL UP			
SIZE: C	DEPT: 410	DRAWING NO.: 4500645	REV: B

RESISTOR NETWORK SPECIFICATIONS:

RESISTANCE VALUES:
±2% (MAX)

OPERATING TEMPERATURE:
0°C TO +70°C

TEMPERATURE COEFFICIENT:
±200 PPM/°C OVER TEMPERATURE RANGE OF 0°C TO +70°C

OPERATING VOLTAGE:
6.0 VDC (MAX)

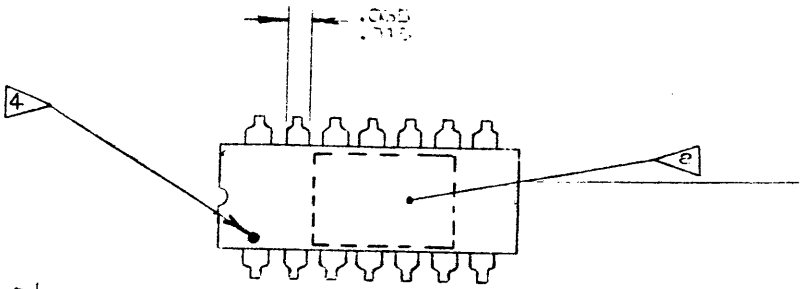
POWER RATING:
AT 70°C, 0.7 WATT PER PACK

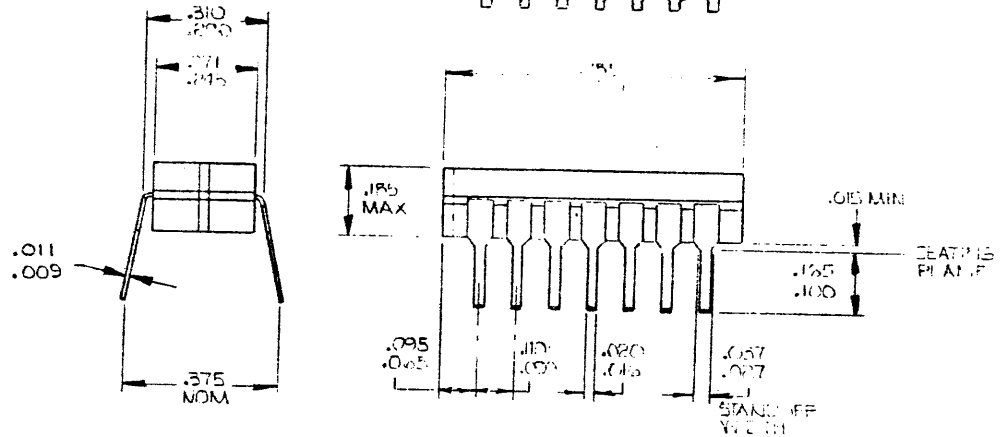
TRACKING RESISTANCE RATIO:
±1.0% (MAX)

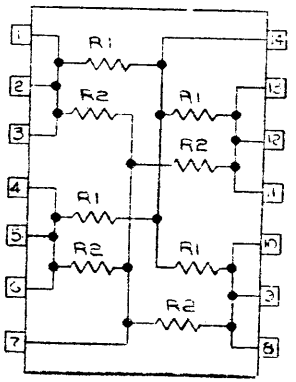
STABILITY:
±1% YEAR (MAX)

LOAD LIFE:
±1% (ΔR) OVER 1000 HOURS

PACKAGE:
DUAL IN LINE - CERAMIC OR PLASTIC







NOTES:
UNLESS OTHERWISE SPECIFIED,

1. PART NO IS 4500644-01.

2. INK STAMP PRODUCT CODE, RESIST R VALUE, PART NO, AND DASH NUMBER WITH CONTRASTING COLOR INK USING MIN .05 HIGH CHARACTERS. NO OTHER MARKING PERMITTED EXCEPT MANUF BATCH NO.
   E.G.) ABC-201
   R220/330
   4500644-01

3. FOR PROCUREMENT SEE LV 4500644-01.

4. IDENTIFY PIN ONE CLEARLY ON TOP OF PACKAGE.

DESCRIPTION			
PARTS LIST			
intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051			
TITLE: TERMINATING PACK PULL UP / PULL DOWN			
SIZE	DEPT	DRAWING NO.	REV
C	410	4500644	B

APPENDIX C

ADD/DELETE WIRE LIST

An add/delete wire list is given in this appendix for one possible implementation of each parallel I/O configuration given in Table 4-10. These tables should aid the user in preparing a wire list to implement a given configuration on the SBC-104 parallel I/O interface. The tables include information on driver/terminator installation, jumper wire adds and deletes, the final jumper configuration and the C Port I/O connection pin assignments. The pin-outs in the table have been chosen to minimize wire changes when changing configurations. The tables assume as a starting point that the I/O jumpers are wired to the default configuration (configuration 2). In some cases an alternate wire list is also given. These lists require fewer add/deletes but result in non-standard pin-outs for control lines, i.e., these lists will not correlate with the information given in Section 4.3.

8255 #1 A20 (Ports 1,2,3)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
1	AS REQUIRED	AS REQUIRED	30-31		29-30		29-30 40-41 42-43 44-45 46-47 48-49 50-51	38-39 36-37 34-35 32-33	C_0→(J1-24) C_1→(J1-22) C_2→(J1-20) C_3→(J1-18)	C_4→(J1-26) C_5→(J1-28) C_6→(J1-30) C_7→(J1-32)
2	AS REQUIRED	AS REQUIRED	---	---	---	---	30-31 40-41 42-43 44-45 46-47 48-49 50-51	38-39 36-37 34-35 32-33	SEE CONFIGURATION 1	
3	A4	A3	30-31 42-43 46-47 48-49 50-51	38-39 36-37 34-35 32-33	29-30 43-50 32-47 36-49	39-42 37-48 35-46	29-30 40-41 43-50 44-45 32-47 36-49	39-42 37-48 35-46	C_0→(PIOB1) C_1→(J1-22) C_2→(J1-32) C_3→(J1-28)	C_4→(J1-24) C_5→(J1-18) C_6→(J1-20) C_7→ OPEN
3 (Alternate Configuration)	A3	A4	30-31 42-43 44-45 50-51	32-33	29-30 43-50 32-45		29-30 40-41 43-50 32-45 46-47 48-49	38-39 36-37 34-35	C_0→(PIOB1) C_1→(J1-32) C_2→(J1-20) C_3→(J1-18)	C_4→(J1-26) C_5→(J1-28) C_6→(J1-30) C_7→ OPEN
4	A4	A3	30-31 42-43 46-47	32-33	29-30 43-50 32-47		29-30 40-41 43-50 44-45 32-47 48-49	38-39 36-37 34-35	C_0→(PIOB1) C_1→(J1-22) C_2→(J1-32) C_3→(J1-18)	C_4→(J1-26) C_5→(J1-28) C_6→(J1-30) C_7→ OPEN

8255 #2 A21 (Ports 4,5,6)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
1	AS REQUIRED	AS REQUIRED	52-53		53-54		53-54 71-72 63-64 65-66 67-68 69-70 73-74	61-62 59-60 57-58 55-56	C_0→(J2-24) C_1→(J2-22) C_2→(J2-20) C_3→(J2-18)	C_4→(J2-26) C_5→(J2-28) C_6→(J2-30) C_7→(J2-32)
2	AS REQUIRED	AS REQUIRED	---	---	---	---	52-53 71-72 63-64 65-66 67-68 69-70 73-74	61-62 59-60 57-58 55-56	SEE CONFIGURATION 1	
3	A10	A9	52-53 63-64 67-68 69-70 73-74	61-62 59-60 57-58 55-56	53-54 64-74 55-68 59-70	62-63 60-69 58-67	53-54 71-72 64-74 65-66 55-68 59-70	62-63 60-69 58-67	C_0→(PIOB2) C_1→(J2-22) C_2→(J2-32) C_3→(J2-28)	C_4→(J2-24) C_5→(J2-18) C_6→(J2-20) C_7→ OPEN
3 (Alternate Configuration)	A9	A10	52-53 63-64 65-66 73-74	55-56	53-54 64-74 55-66		53-54 71-72 64-74 55-66 67-68 69-70	61-62 59-60 57-58	C_0→(PIOB2) C_1→(J2-32) C_2→(J2-20) C_3→(J2-18)	C_4→(J2-26) C_5→(J2-28) C_6→(J2-30) C_7→ OPEN
4	A10	A9	52-53 63-64 67-68	55-56	53-54 64-74 55-68		53-54 71-72 64-74 65-66 55-68 69-70	61-62 59-60 57-58	C_0→(PIOB2) C_1→(J2-22) C_2→(J2-32) C_3→(J2-18)	C_4→(J2-26) C_5→(J2-28) C_6→(J2-30) C_7→ OPEN

8255 #1 A20 (Ports 1,2,3)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
5	A4	A3	42-43 46-47 48-49 50-51	38-39 36-37 34-35 32-33	43-50 32-47 36-49	39-42 37-48 35-46	30-31 40-41 43-50 44-45 32-47 36-49	39-42 37-48 35-46	SEE CONFIGURATION 3	
5 (Alternate Configuration)	A3	A4	42-43 44-45 50-51	32-33	43-50 32-45		30-31 40-41 43-50 32-45 46-47 48-49	38-39 36-37 34-35	SEE CONFIGURATION 3 ALTERNATE	
6	A4	A3	42-43 46-47	32-33	29-30 43-50 32-47		30-31 40-41 43-50 44-45 32-47 48-49	38-39 36-37 34-35	SEE CONFIGURATION 4	
7	A4	A3	30-31 40-41 42-43 44-45 46-47 48-49	36-37 34-35 32-33	29-30 34-43 36-45 32-47 40-49	36-48 35-46 33-42	29-30 34-43 36-45 32-47 40-49 50-51	38-39 36-48 35-46 33-42	C_0→(J1-30) C_1→(J1-28) C_2→(J1-32) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-18) C_6→(J1-20) C_7→(J1-24)
7 (Alternate Configuration)	A3	A4	30-31 40-41 48-49	38-39	29-30 40-49	39-48	29-30 42-43 44-45 46-47 40-49 50-51	39-48 36-37 34-35 32-33	C_0→(J1-24) C_1→(J1-22) C_2→(J1-20) C_3→(PIOA1)	C_4→(J1-18) C_5→(J1-28) C_6→(J1-30) C_7→(J1-32)

8255 #2 A21 (Ports 4,5,6)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
5	A10	A9	63-64 67-68 69-70 73-74	61-62 59-60 57-58 55-56	64-74 55-68 59-70	62-63 60-69 58-67	52-53 71-72 64-74 65-66 55-68 59-70	62-63 60-69 58-67	SEE CONFIGURATION 3	
5 (Alternate Configuration)	A9	A10	63-64 65-66 73-74	55-56	64-74 55-66		52-53 71-72 64-74 55-66 67-68 69-70	61-62 59-60 57-58	SEE CONFIGURATION 3 ALTERNATE	
6	A10	A9	63-64 67-68	55-56	53-54 64-74 55-68		52-53 71-72 64-74 65-66 55-68 69-70	61-62 59-60 57-58	SEE CONFIGURATION 4	
7	A10	A9	52-53 71-72 63-64 65-66 67-68 69-70	59-60 57-58 55-56	53-54 57-64 59-66 55-68 70-71	60-69 58-67 56-63	53-54 57-64 59-66 55-68 70-71 73-74	61-62 60-69 58-67 56-63	C_0→(J2-30) C_1→(J2-28) C_2→(J2-32) C_3→(PIOA2)	C_4→(J2-26) C_5→(J2-18) C_6→(J2-20) C_7→(J2-24)
7 (Alternate Configuration)	A9	A10	52-53 71-72 69-70	61-62	53-54 70-71	62-69	53-54 63-64 65-66 67-68 70-71 73-74	62-69 59-60 57-58 55-56	C_0→(J2-24) C_1→(J2-22) C_2→(J2-20) C_3→(PIOA2)	C_4→(J2-18) C_5→(J2-28) C_6→(J2-30) C_7→(J2-32)

8255 #1 A20 (Ports 1,2,3)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
8	A4	A3	30-31 40-41 48-49	36-37	29-30 40-49	37-48	29-30 42-43 44-45 46-47 40-49 50-51	38-39 37-48 34-35 32-33	C_0→(J1-24) C_1→(J1-22) C_2→(J1-20) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-18) C_6→(J1-30) C_7→(J1-32)
9	A4	A3	40-41 42-43 44-45 46-47 48-49	38-39 36-37 32-33	38-43 36-45 32-47 40-49	39-46 37-42 33-48	30-31 38-43 36-45 32-47 40-49 50-51	39-46 37-42 34-35 33-48	C_0→(J1-26) C_1→(J1-28) C_2→(J1-32) C_3→(PIOA1)	C_4→(J1-20) C_5→(J1-24) C_6→(J1-30) C_7→(J1-18)
9 (Alternate Configuration)	A3	A4	40-41 48-49	34-35	40-49	35-48	30-31 42-43 44-45 46-47 40-49 50-51	38-39 36-37 35-48 32-33	C_0→(J1-24) C_1→(J1-22) C_2→(J1-20) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-28) C_6→(J1-18) C_7→(J1-32)
10	A4	A3	40-41 48-49	32-33	40-49	33-48	30-31 42-43 44-45 46-47 40-49 50-51	38-39 36-37 34-35 33-48	C_0→(J1-24) C_1→(J1-22) C_2→(J1-20) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-28) C_6→(J1-30) C_7→(J1-18)
11	A4	A3	30-31 40-41 42-43 46-47 48-49 50-51	36-37 32-33	29-30 43-50 32-47 40-49	37-48 33-36	29-30 43-50 44-45 32-47 40-49	38-39 37-48 34-35 33-36	C_0→(PIOB1) C_1→(J1-22) C_2→(J1-32) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-18) C_6→(J1-30) C_7→(J1-28)

8255 #2 A21 (Ports 4,5,6)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
8	A10	A9	52-53 71-72 69-70	59-60	53-54 70-71	60-69	53-54 63-64 65-66 67-68 70-71 73-74	61-62 60-69 57-58 55-56	C_0→(J2-24) C_1→(J2-22) C_2→(J2-20) C_3→(PIOA2)	C_4→(J2-26) C_5→(J2-18) C_6→(J2-30) C_7→(J2-32)
9	A10	A9	71-72 63-64 65-66 67-68 69-70	61-62 59-60 55-56	61-64 59-66 55-68 70-71	62-67 60-63 56-69	52-53 61-64 59-66 55-68 70-71 73-74	62-67 60-63 57-58 56-69	C_0→(J2-26) C_1→(J2-28) C_2→(J2-32) C_3→(PIOA2)	C_4→(J2-20) C_5→(J2-24) C_6→(J2-30) C_7→(J2-18)
9 (Alternate Configuration)	A9	A10	71-72 69-70	57-58	70-71	58-69	52-53 63-64 65-66 67-68 70-71 73-74	61-62 59-60 58-69 55-56	C_0→(J2-24) C_1→(J2-22) C_2→(J2-20) C_3→(PIOA2)	C_4→(J2-26) C_5→(J2-28) C_6→(J2-18) C_7→(J2-32)
10	A10	A9	71-72 69-70	55-56	70-71	56-69	52-53 63-64 65-66 67-68 70-71 73-74	61-62 59-60 57-58 56-69	C_0→(J2-24) C_1→(J2-22) C_2→(J2-20) C_3→(PIOA2)	C_4→(J2-26) C_5→(J2-28) C_6→(J2-30) C_7→(J2-18)
11	A10	A9	52-53 71-72 63-64 67-68 69-70 73-74	59-60 55-56	53-54 64-74 55-68 70-71	60-69 56-59	53-54 64-74 65-66 55-68 70-71	61-62 60-69 57-58 56-59	C_0→(PIOB2) C_1→(J2-22) C_2→(J2-32) C_3→(PIOA2)	C_4→(J2-26) C_5→(J2-18) C_6→(J2-30) C_7→(J2-28)

8255 #1 A20 (Ports 1,2,3)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
12	A4	A3	30-31 40-41 42-43 46-47 48-49 50-51	36-37 34-35 32-33	29-30 43-50 32-47 40-49	37-48 35-46 33-42	29-30 43-50 44-45 32-47 40-49	38-39 37-48 35-46 33-42	C_0→(PIOB1) C_1→(J1-22) C_2→(J1-32) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-18) C_6→(J1-20) C_7→(J1-24)
13	A4	A3	40-41 42-43 46-47 48-49 50-51	32-33	43-50 32-47 40-49	33-48	30-31 43-50 44-45 32-47 40-49	38-39 36-37 34-35 33-48	C_0→(PIOB1) C_1→(J1-22) C_2→(J1-32) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-28) C_6→(J1-30) C_7→(J1-18)
14	A4	A3	40-41 42-43 46-47 48-49 50-51	38-39 36-37 32-33	43-50 32-47 40-49	39-46 37-42 33-48	30-31 43-50 44-45 32-47 40-49	39-46 37-42 34-35 33-48	C_0→(PIOB1) C_1→(J1-22) C_2→(J1-32) C_3→(PIOA1)	C_4→(J1-20) C_5→(J1-24) C_6→(J1-30) C_7→(J1-18)
15	A4	A3	30-31 40-41 42-43 44-45 46-47 48-49 50-51	36-37 32-33	36-45 32-47 40-49	37-42 30-35 33-48	36-45 32-47 40-49	38-39 37-42 34-35 30-35 33-48	C_0→ OPEN C_1→(J1-28) C_2→(J1-32) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-24) C_6→(J1-30) C_7→(J1-18)
16	A4	A3	30-31 40-41 42-43 48-49 50-51	36-37 32-33	40-49	37-42 30-35 33-48	44-45 46-47 40-49	38-39 37-42 34-35 30-35 33-48	C_0→ OPEN C_1→(J1-22) C_2→(J1-20) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-24) C_6→(J1-30) C_7→(J1-18)

8255 #2 A21 (Ports 4,5,6)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
12	A10	A9	52-53 71-72 63-64 67-68 69-70 73-74	59-60 57-58 55-56	53-54 64-74 55-68 70-71	60-69 58-67 56-69	53-54 64-74 65-66 55-68 70-71	61-62 60-69 58-67 56-69	C_0→(PIOB2) C_1→(J2-22) C_2→(J2-32) C_3→(PIOA2)	C_4→(J2-26) C_5→(J2-18) C_6→(J2-20) C_7→(J2-24)
13	A10	A9	71-72 63-64 67-68 69-70 73-74	55-56	64-74 55-68 70-71	56-69	52-53 64-74 65-66 55-68 70-71	61-62 59-60 57-58 56-69	C_0→(PIOB2) C_1→(J2-22) C_2→(J2-32) C_3→(PIOA2)	C_4→(J2-26) C_5→(J2-28) C_6→(J2-30) C_7→(J2-18)
14	A10	A9	71-72 63-64 67-68 69-70 73-74	61-62 59-60 55-56	64-74 55-68 70-71	62-67 60-63 56-69	52-53 64-74 65-66 55-68 70-71	62-67 60-63 57-58 56-69	C_0→(PIOB2) C_1→(J2-22) C_2→(J2-32) C_3→(PIOA2)	C_4→(J2-20) C_5→(J2-24) C_6→(J2-30) C_7→(J2-18)
15	A10	A9	52-53 71-72 63-64 65-66 67-68 69-70 73-74	59-60 55-56	59-66 55-68 70-71	60-63 53-58 56-69	59-66 55-68 70-71	61-62 60-63 57-58 53-58 56-69	C_0→ OPEN C_1→(J2-22) C_2→(J2-32) C_3→(PIOA2)	C_4→(J2-26) C_5→(J2-24) C_6→(J2-30) C_7→(J2-18)
16	A10	A9	52-53 71-72 63-64 69-70 73-74	59-60 55-56	70-71	60-63 53-58 56-69	65-66 67-68 70-71	61-62 60-63 57-58 53-58 56-69	C_0→ OPEN C_1→(J2-22) C_2→(J2-20) C_3→(PIOA2)	C_4→(J2-26) C_5→(J2-24) C_6→(J2-30) C_7→(J2-18)

8255 #1 A20 (Ports 1,2,3)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
17	A4	A3	30-31 40-41 42-43 46-47 48-49 50-51	36-37 32-33	43-50 32-47 40-49	37-42 33-48	43-50 44-45 32-47 40-49	38-39 37-42 34-35 30-35 33-48	C_0→(PIOB1) C_1→(J1-22) C_2→(J1-32) C_3→(PIOA1)	C_4→(J1-26) C_5→(J1-24) C_6→(J1-30) C_7→(J1-18)

8255 #2 A21 (Ports 4,5,6)

CONFIGURATION NUMBER	INSTALL PORT C		DELETE JUMPER		ADD JUMPER		FINAL JUMPER CONFIGURATION		C-PORTS PINOUTS	
	DRIVERS	TERM.								
17	A10	A9	52-53 71-72 63-64 67-68 69-70 73-74	59-60 55-56	64-74 55-68 70-71	60-63 56-69	64-74 65-66 55-68 70-71	61-62 60-63 57-58 53-58 56-69	$C_0 \rightarrow$(PIOB2) $C_1 \rightarrow$(J2-22) $C_2 \rightarrow$(J2-32) $C_3 \rightarrow$(PIOA2)	$C_4 \rightarrow$(J2-26) $C_5 \rightarrow$(J2-24) $C_6 \rightarrow$(J2-30) $C_7 \rightarrow$(J2-18)