THEORY OF OPERATION

iSBX 218A

FLEXIBLE DISKETTE CONTROLLER

GEORGE ARRIGOTTI

JULY 11, 1983

THEORY OF OPERATION

iSBX 218A

FLEXIBLE DISKETTE CONTROLLER

GEORGE ARRIGOTTI

JULY 11, 1983

iSBX 218/218A COMMON FEATURES

DOUBLE WIDE SBX MULTIMODULE FORM FACTOR.

CONTROLS UP TO FOUR SINGLE/DOUBLE SIDED EIGHT INCH DRIVES OR UP TO FOUR SINGLE/ DOUBLE SIDED FIVE AND ONE-QUARTER DRIVES.

SINGLE/DOUBLE DENSITY MAY BE MIXED.

IBM COMPATIBLE SOFT-SECTORED FORMAT.

DMA OR NON-DMA OPERATION OF SBX BUS.

USES INTEL 8272 FLOPPY DISK CONTROLLER.

PLAN

218A ADDITIONAL FEATURES

TWO READ/WRITE ONE BIT LATCHES USABLE FOR:

- SPINDLE MOTOR ON/OFF CONTROL
- HEAD LOAD CONTROL
- "IN USE" LED CONTROL
- TERMINAL COUNT TO 8272
- TDMA MASK

ONE WRITE-ONLY ONE BIT LATCH FOR RESET.

DMA ACKNOWLEDGE (DACK) GENERATOR TO ALLOW 8272 DMA MODE WITH 8089 AND 80186.

218A ADDITIONAL FEATURES (CONTINUED)

ON BOARD PIN SCRAMBLING FOR 5¼" DRIVES.

IMPROVED PHASE LOCKED LOOP CIRCUITRY.

CHOICE OF 125NS OR 250NS WRITE PRECOMPENSATION.

OVERCOMES SEVERAL 8272 BUGS:

- WRONG DENSITY HANGUP PROBLEM
- NON-EXISTENT DISK HANGUP PROBLEM (READY HANG)
- DRQ-TO-COMMAND DELAY SPEC
- DMA OVERRUN PROBLEM
- DACK MINIMUM PULSE WIDTH PROBLEM

FLEXIBLE DISKETTE CONTROLLER (8272)

HANDLES CONTROL/STATUS LINES TO/FROM DRIVES.

ENCODES/DECODES DATA STREAMS TO/FROM DRIVES.

INTERFACES WITH SBX BUS.

CONTROLS/COORDINATES ALL OTHER BLOCKS.

FUNCTIONAL BLOCKS

FLEXIBLE DISKETTE CONTROLLER (8272)

TIMING AND PHASE LOCKED LOOP LOGIC

READ WINDOW GENERATION LOGIC

READ DATA SHAPING LOGIC

WRITE PRECOMPENSATION LOGIC

DMA SIGNAL GENERATION LOGIC

I/O PORT OPTIONS LOGIC

ISBX BUS INTERFACE

FLEXIBLE DISKETTE DRIVE INTERFACE LOGIC

BUFFERING

MULTIPLEXING

DEMULTIPLEXING

TERMINATION

DRIVE INTERFACE OPTIONS

READY TIMEOUT CIRCUIT

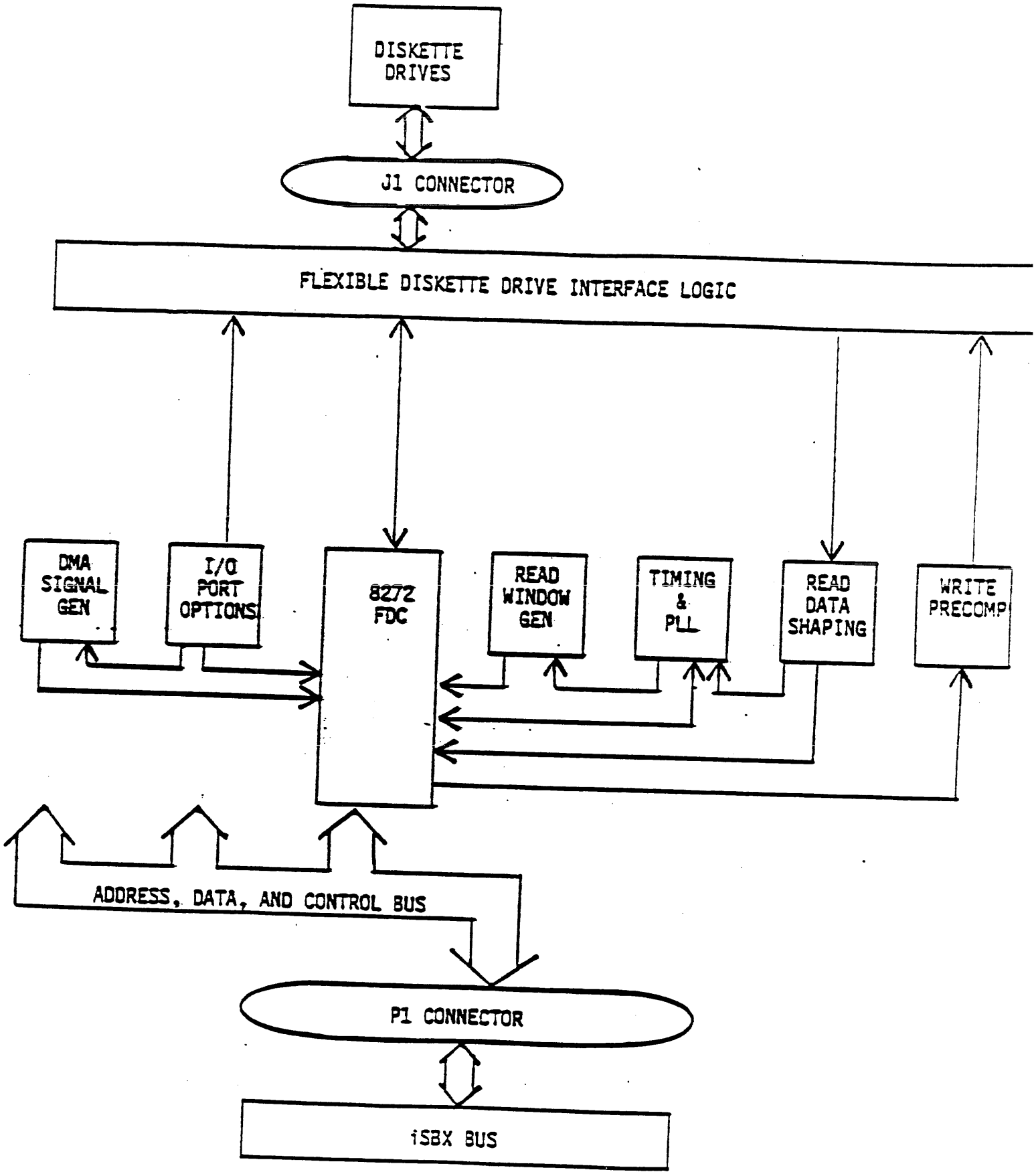


FIGURE 2. iSBX 218A FLEXIBLE DISKETTE CONTROLLER BLOCK DIAGRAM

TIMING AND PHASE LOCKED LOOP LOGIC

8 AND 4 MHz TO PRECOMPENSATION LOGIC

8 AND 4 MHz TO THE 8272.

WRITE CLOCK:
- 8" MFM 1µS PERIOD
- 8" FM 2µS PERIOD
- 5¼" MFM 2µS PERIOD
- 5¼" FM 4µS PERIOD

ALL PULSES ABOUT 250nS HIGH TIME

8272 MUST ALWAYS HAVE WRITE CLOCK.

READ WINDOW GENERATION LOGIC

CLK3 IS VCO FREQUENCY DIVIDED DOWN:

8"	MFM	2 MHz
8"	FM	1 MHz
5¼"	MFM	1 MHz
5¼"	FM	0.5 MHz

WINDOW EXTENDER ADJUSTS READ WINDOW TEMPORARILY TO CATCH ONE LATE OR EARLY BIT.

USED BY 8272 TO SEPARATE DATA FROM THE COMBINED DATA/CLOCK STREAM.

TIMING AND PHASE LOCKED LOOP LOGIC (CONTINUED)

THE VOLTAGE CONTROLLED OSCILLATOR (74S124 VCO) OUTPUT HAS THREE MODES:

1. WHEN 8272 VCO SIGNAL IS HIGH (MEANING READ), THE PHASE COMPARATOR SPEEDS UP OR SLOWS DOWN THE VCO TO MATCH THE READ DATA.
2. WHEN 8272 VCO SIGNAL IS LOW (MEANING NOT READ), THE PHASE COMPARATOR LOCKS ON TO A KNOWN FREQUENCY (WRITE CLOCK).
3. WHEN RESET BUTTON IS HELD, THERE IS NO FEEDBACK, AND C3 AFFECTS FREQUENCY.

ALL SHOULD BE ABOUT 8 MHz.

READ DATA SHAPING LOGIC

ONE SHOTS CLEAN UP READ DATA PULSES FROM DRIVE.

ARE FIRED BY WRITE CLOCK WHEN VCO SIGNAL IS LOW.

NOMINAL VALUES:

8"	MFM	550 nS	USING 4.99K	RESISTOR
8"	FM	1100 nS	USING 10.0K	RESISTOR
5¼"	MFM	1100 nS	USING 10.0K	RESISTOR
5¼"	FM	2200 nS	USING 20.0K	RESISTOR

WRITE PRECOMPENSATION LOGIC

TO COUNTER THE EFFECT OF PREDICTABLE BIT SHIFT.

EACH BIT MAY BE WRITTEN EARLY, NORMAL, OR LATE, CONTROLLED BY PSØ, PS1.

ALL TRACKS OR JUST INNER TRACKS ARE PRECOMPENSATED.

WRITE DATA TO DRIVE IS LOW WHEN WRITE ENABLE IS INACTIVE.

I/O PORT OPTIONS LOGIC

RESET LATCH - WRITING A ONE FOLLOWED BY WRITING A ZERO PRODUCES A HARDWARE RESET.

LATCH Ø - DEFAULT WIRED TO CONTROL DRIVE SPINDLE MOTOR.

LATCH 1 - DEFAULT WIRED TO CONTROL THE TDMA MASK.

DMA SIGNAL GENERATION LOGIC

DELAYS DMA REQUEST (DRQ) TO BASEBOARD TO PREVENT AN EARLY COMMAND.
MINIMUM TIMES: 8" DRIVES 800NS
5¼" DRIVES 1600NS

GENERATES MWAIT TO EXTEND DACK OR COMMAND
MINIMUM TIME: 510NS

GENERATES DACK TO 8272 WHEN BASEBOARD CONTROLLER IS 80186 OR 8089 (LIKE 215G)

SBX BUS INTERFACE

STANDARD SBX INTERFACE

IMPLEMENTED BY PALS AND THE 8272.

SOURCES OF FURTHER INFORMATION

SBX 218A EXTERNAL PRODUCT SPEC 145935

SBX 218A HARDWARE REFERENCE MANUAL (AVAILABLE LATE AUGUST)

SBX 218A INTERNAL PRODUCT SPEC (AVAILABLE LATE AUGUST)

NTEL 8272 DATA SHEET (IN COMPONENT CATALOG)

SBX 218 MANUAL, ISBC 208 MANUAL (CONTAIN THEORY OF OPERATION SECTIONS FOR VERY SIMILAR CIRCUITS)

PAL16L8
PAT NO 218AU10B
PRECOMP PAL AT U10

PAL DESIGN SPECIFICATION
GEORGE ARRIGOTTI 5-2-83

```
LCT LATE NORMAL INT PS1 PS0 DS0 DS1 ENABLE GND
EARLY WRDATA SPARE13 WE TDMA DRVSEL3 DRVSEL2 DRVSEL1 DRVSEL0 VCC

IF (VCC) /WRDATA = /WE +
                   LCT * /PS0 * /PS1 * NORMAL +
                   LCT * /PS0 * PS1 * LATE +
                   LCT * PS0 * /PS1 * EARLY +
                   /LCT * NORMAL

IF (VCC) /DRVSEL0 = /DS1 * /DS0

IF (VCC) /DRVSEL1 = /DS1 * DS0

IF (VCC) /DRVSEL2 = DS1 * /DS0

IF (VCC) /DRVSEL3 = DS1 * DS0

IF (VCC)    /TDMA = /ENABLE + /INT

IF (VCC) /SPARE13 = VCC
```

DESCRIPTION

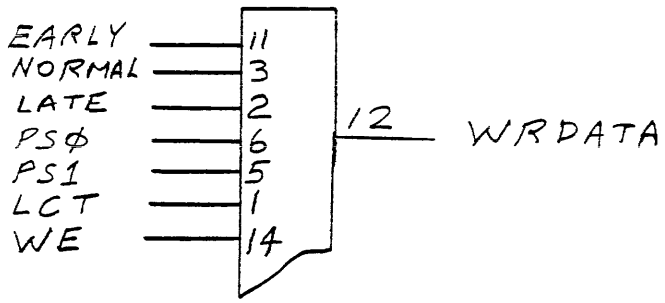
THE WRDATA OUTPUT CONTROLS THE DATA STREAM TO THE DRIVE. WHEN LCT FROM THE 8272 IS ACTIVE, IT GATES OUT THE EARLY, NORMAL, OR LATE SIGNAL DEPENDING ON THE STATE OF PS0 AND PS1 FROM THE 8272. WHEN LCT IS INACTIVE (MEANING NO PRECOMPENSATION NEEDED) IT GATES OUT THE NORMAL SIGNAL. ALL THIS ONLY HAPPENS WHEN WRITE ENABLE (WE) IS ACTIVE. OTHERWISE, WRDATA IS LOW.

THE DRVSEL OUTPUTS DECODE DS0 AND DS1 FROM THE 8272 AND ARE USED TO SELECT ONE OF THE FOUR DRIVES.

INPUTS INT, ENABLE AND OUTPUT TDMA ALLOW TDMA TO BE MASKED FROM THE SBX BUS.

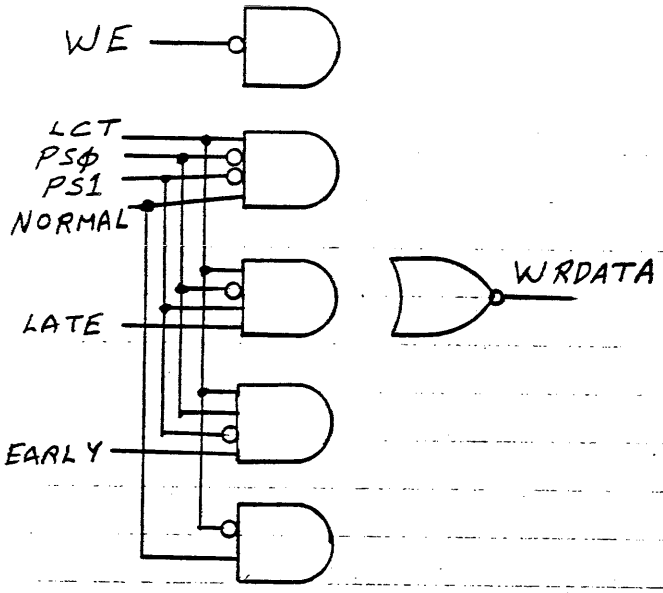
SPARE13 IS AN UNUSED INPUT/OUTPUT PIN.

PAL U10 OUTPUT PIN 12 WRDATA (WRITE DATA)



EQUATION: /WRDATA = /WE +
LCT * /PSΦ * /PS1 * NORMAL +
LCT * /PSΦ * PS1 * LATE +
LCT * PSΦ * /PS1 * EARLY +
/LCT * NORMAL

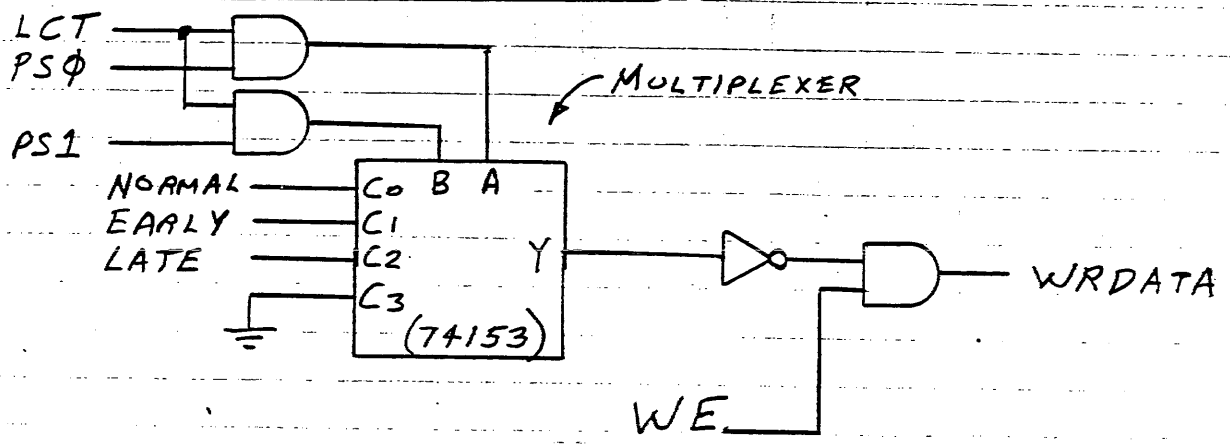
PAL CIRCUIT:



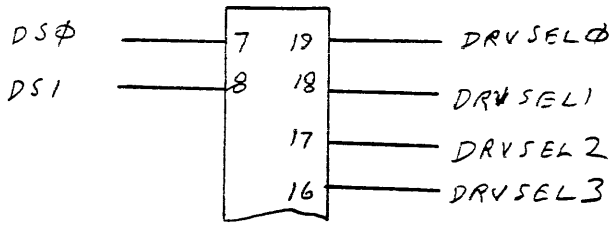
NOTES:

WHEN WE IS LOW, THE OUTPUT IS ALWAYS LOW. WHEN WE IS HIGH AND LCT IS LOW, THE NORMAL SIGNAL IS DRIVEN OUT. ONLY WHEN WE IS HIGH AND LCT IS HIGH, PSΦ AND PS1 ARE USED TO SELECT THE EARLY, NORMAL, OR LATE SIGNAL.

ALTERNATE REPRESENTATION:



PAL U10 OUTPUT PINS 16, 17, 18, 19
(DRVSEL3, DRVSEL2, DRVSEL1, DRVSEL0)



EQUATIONS:

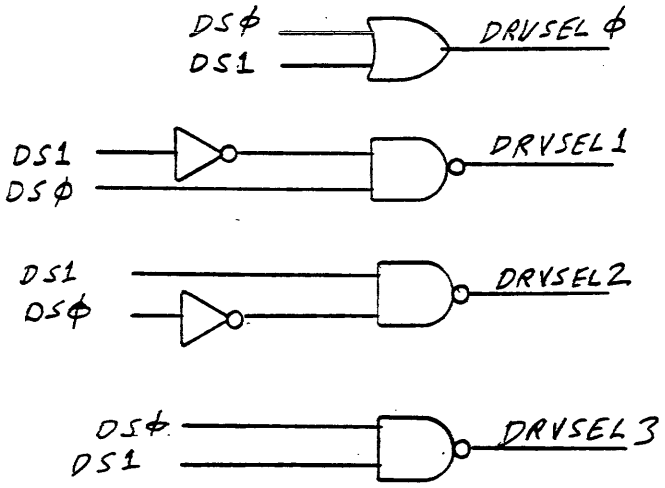
/DRVSEL0 = /DS1 * /DS0

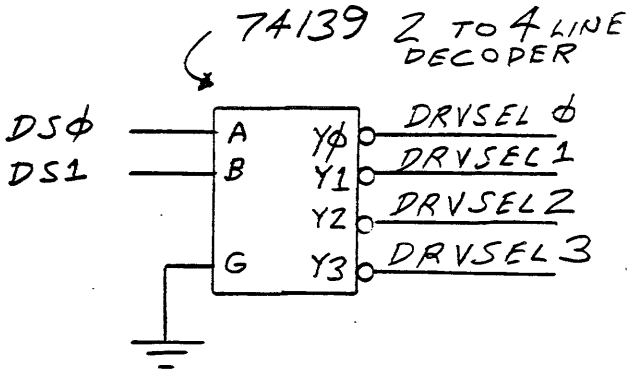
/DRVSEL1 = /DS1 * DS0

/DRVSEL2 = DS1 * /DS0

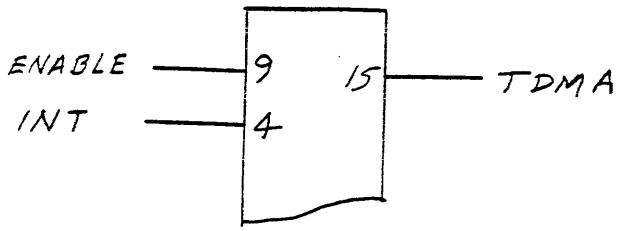
/DRVSEL3 = DS1 * DS0

ALTERNATE REPRESENTATIONS:



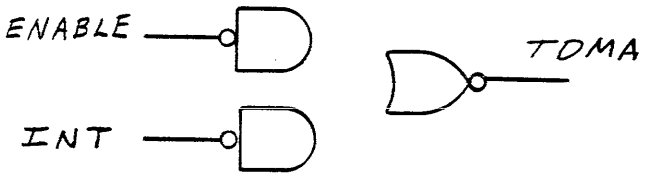


PAL U10 OUTPUT PIN 15 TDMA

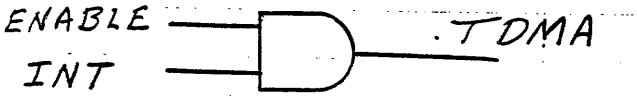


EQUATION: /TDMA = /ENABLE + /INT

PAL CIRCUIT:



ALTERNATE REPRESENTATION:



PAL16L8
PAT NO 218AU15A
DMA PAL AT U15

PAL DESIGN SPECIFICATION
GEORGE ARRIGOTTI 4-6-83

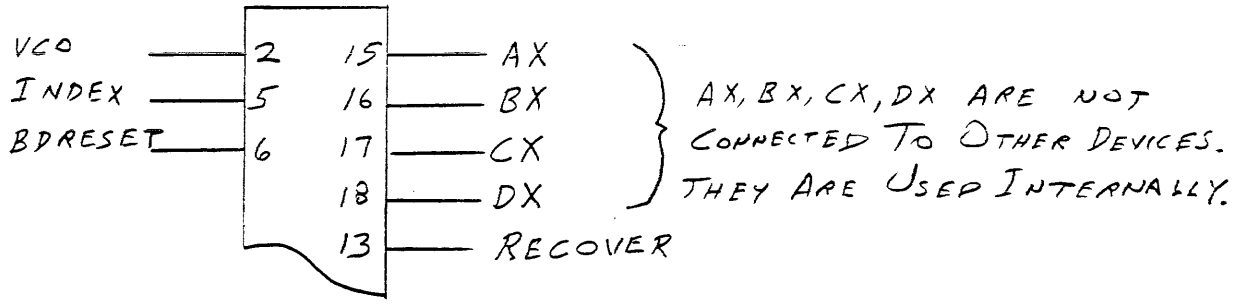
```
HDLOAD VCO DRQ DACK INDEX BDRESET SPARE7 CLK DELAY GND
INT START RECOVER MDRQT AX BX CX DX TRIGGER VCC

IF (VCC) /MDRQT = /DRQ +
                  /DACK +
                  BDRESET +
                  INT +
                  /DELAY * /MDRQT

IF (VCC)   /AX = INDEX * VCO +
                 VCO * /BDRESET * /AX

IF (VCC)   /BX = /INDEX * /AX +
                 /AX * /BDRESET * /BX

IF (VCC)   /CX = INDEX * /BX +
                 /BX * /BDRESET * /CX

IF (VCC)   /DX = /INDEX * /CX +
                 /BDRESET * VCO * /CX * /DX

IF (VCC) /RECOVER = /RECOVER * /BDRESET * VCO * /DX +
                    INDEX * /DX

IF (VCC) /START = DRQ * DACK * /BDRESET * /INT * /MDRQT

IF (VCC) /TRIGGER = INDEX * HDLOAD +
                    CLK * /HDLOAD
```

DESCRIPTION OF PINS

DACK - DMA ACKNOWLEDGE TO 8272.
DRQ - DMA REQUEST FROM 8272.
MDRQT - DMA REQUEST TO BASE BOARD.
START - SIGNAL THAT BEGINS THE RC DELAY FOR DRQ.
DELAY - INPUT FROM RC DELAY CIRCUIT.
BDRESET - BASE BOARD OR PROGRAMMED RESET.
AX,BX,CX,DX,RECOVER - STATE MACHINE USED TO OVERCOME THE
8272 FM-DISK-IN-MFM-SLOT LOCKUP BUG.
VCO - FROM 8272 - INPUT TO THE ABOVE STATE MACHINE.
INDEX - INPUT TO THE ABOVE STATE MACHINE. ALSO FOR RETRIGGER GENERATOR.
TRIGGER - OUTPUT TO KEEP RETRIGGERING THE DRIVE HANGUP ONE SHOT.
HDLOAD - FROM 8272 - INPUT TO RETRIGGER GENERATOR.
CLK - FROM WRITE CLOCK CHAIN - INPUT TO RETRIGGER GENERATOR.
SPARE7 - SPARE INPUT PIN.

PAL 415 OUTPUT PINS 13, 15, 16, 17, 18

(RECOVER, AX, BX, CX, DX)



EQUATIONS:

$$/AX = INDEX * VCO + VCO * /BDRESET * /AX$$

$$/BX = /INDEX * /AX + /AX * /BDRESET * /BX$$

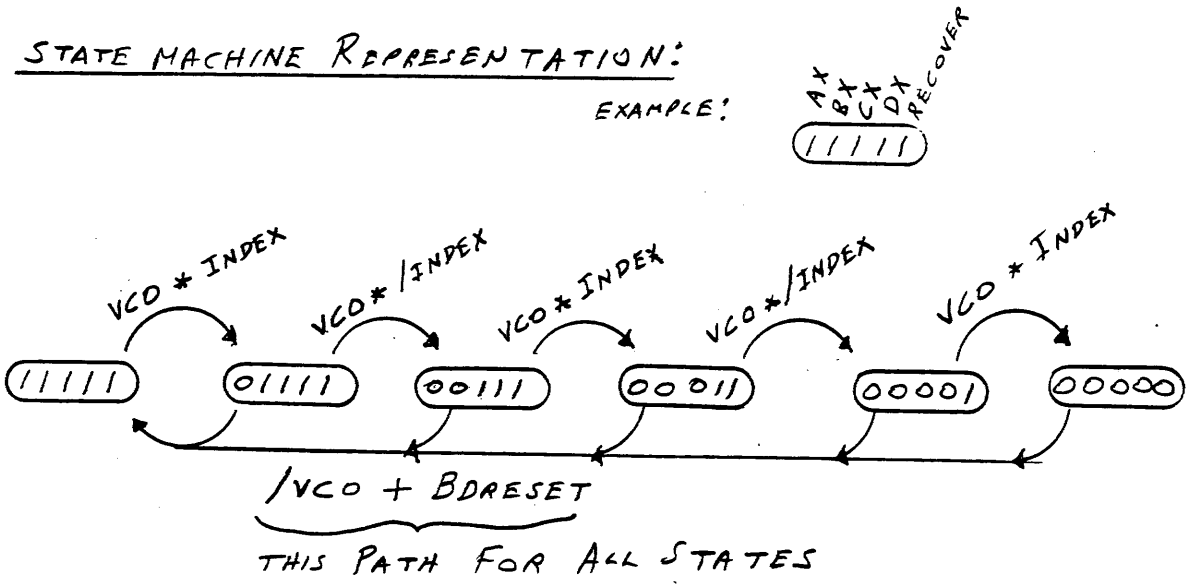
$$/CX = INDEX * /BX + /BX * /BDRESET * /CX$$

$$/DX = /INDEX * /CX + /BDRESET * VCO * /CX * /DX$$

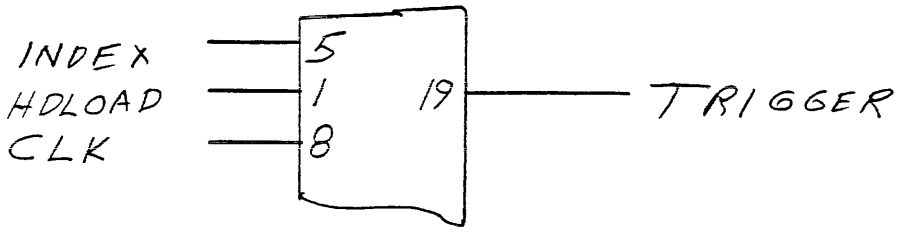
$$/RECOVER = /RECOVER * /BDRESET * VCO * /DX + INDEX * /DX$$

STATE MACHINE REPRESENTATION:

EXAMPLE:



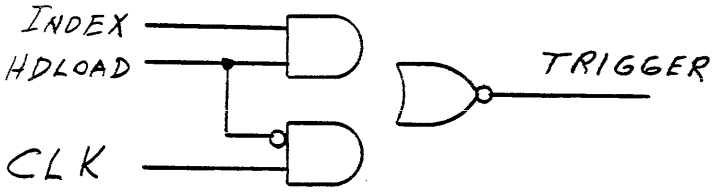
PAL U15 OUTPUT PIN 19 TRIGGER



EQUATION:

/TRIGGER = INDEX * HDLOAD +
CLK * /HDLOAD

PAL CIRCUIT:



NOTES:

TRIGGER DRIVES A FALLING-EDGE-TRIGGERRED INPUT TO A ONE SHOT. THE OUTPUT OF THE ONE SHOT DRIVES READY TO THE 8272.

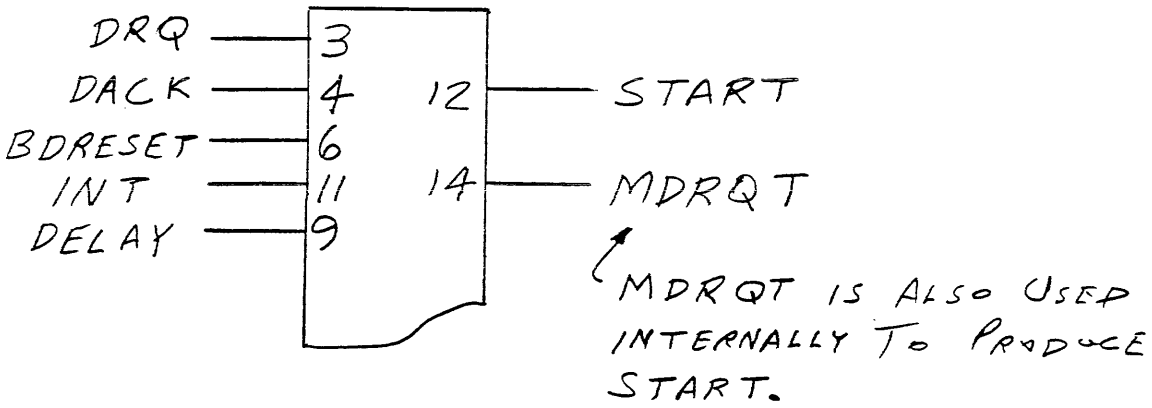
WHEN THE HEAD IS LOADED (MEANING AN ACCESS IS BEING MADE) INDEX PULSES FROM THE SELECTED DRIVE WILL KEEP RETRIGGERING THE ONE SHOT, INDICATING READY TO THE 8272.

IF THE HEAD IS LOADED AND NO DISKETTE IS INSTALLED IN THE SELECTED DRIVE, THERE WILL BE NO INDEX PULSES AND THE ONE SHOT WILL TIME OUT, INDICATING NOT READY TO THE 8272.

WHEN THE HEAD IS NOT LOADED, A CLOCK SIGNAL KEEPS RETRIGGERING THE ONE SHOT.

SO THE 8272 READY LINE IS ALWAYS TRUE EXCEPT IN THE NON-EXISTENT DISK ACCESS ATTEMPT DESCRIBED ABOVE.

PAL U15 OUTPUT PINS 12 AND 14 (START AND MDRQT)

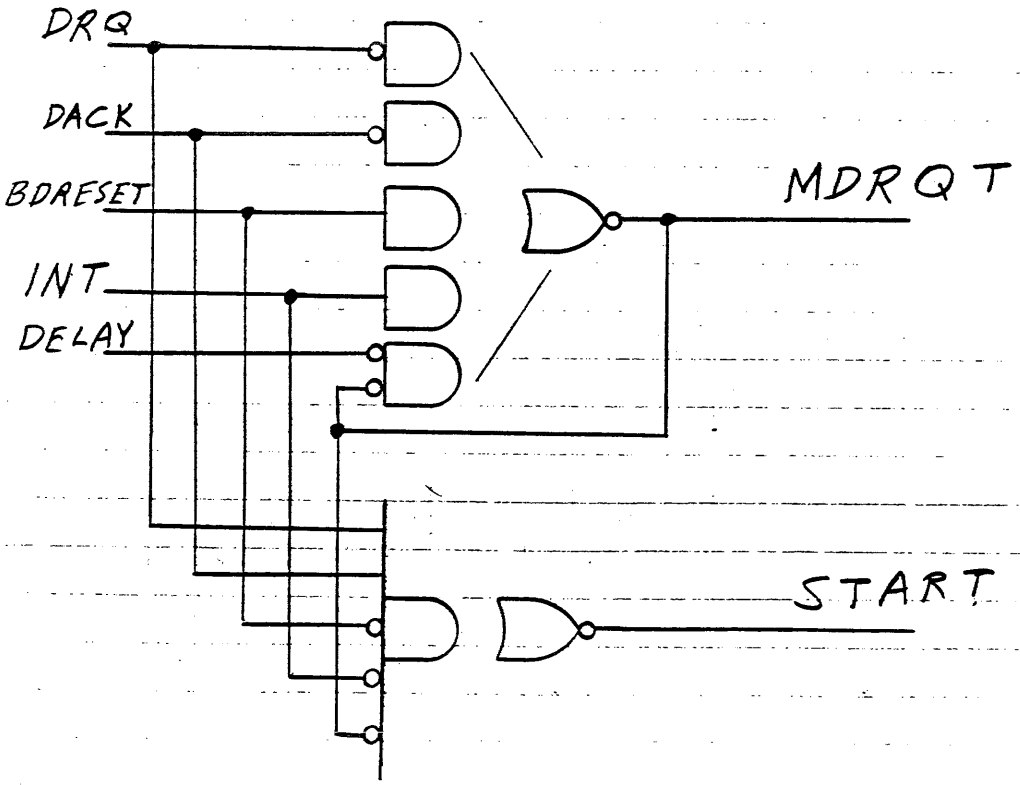


EQUATIONS:

/START = DRQ * DACK * /BDRESET * /INT * /MDRQT

/MDRQT = /DRQ +
/DACK +
BDRESET +
INT +
/DELAY * /MDRQT

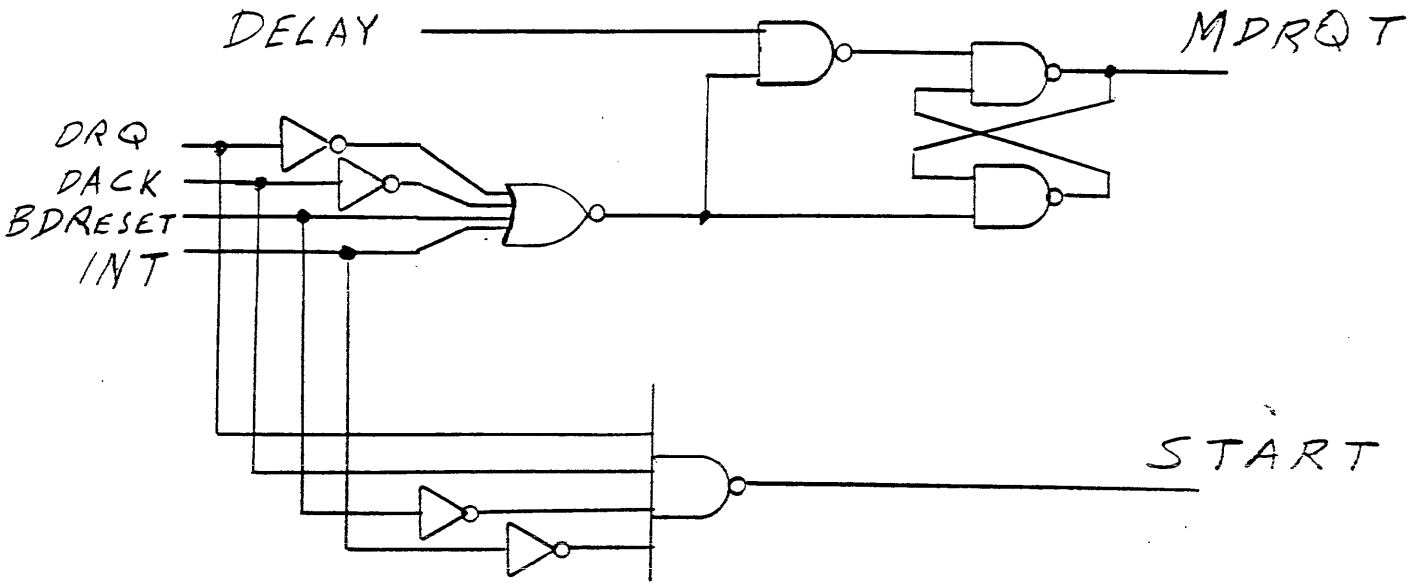
PAL CIRCUITS:



CONTINUED →

START AND MDRQT (CONTINUED)

ALTERNATE REPRESENTATION:

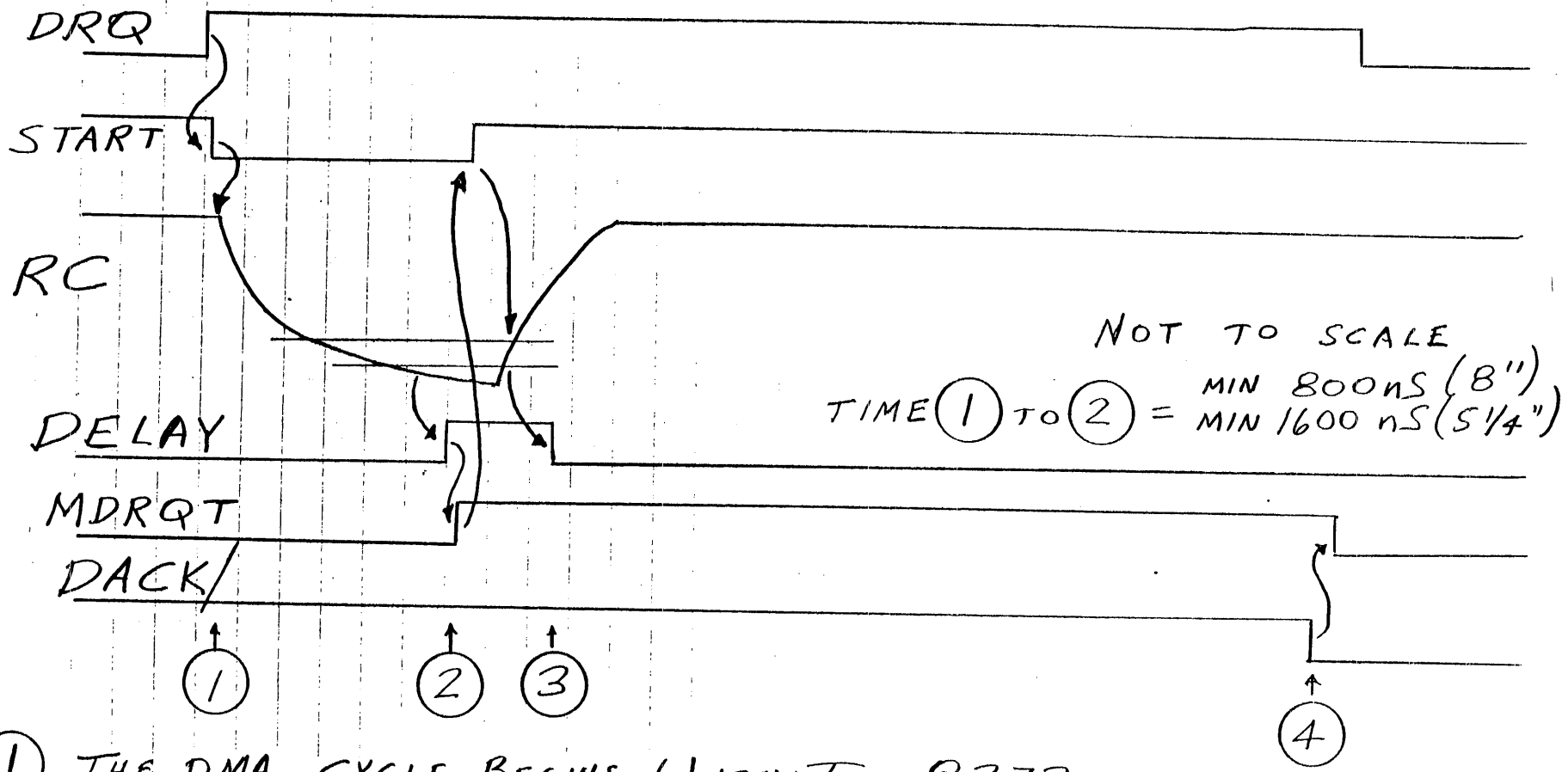


NOTES:

THE 8272 SPEC SAYS THAT AFTER IT SENDS OUT DRQ, IT MUST NOT SEE IOWRT FOR 800 nS OR IORD FOR 250 nS (DOUBLE THESE TIMES FOR 5¼" DRIVES). THE PURPOSE THE RC DELAY CIRCUIT IS TO DELAY DRQ BEFORE IT GETS TO THE BASEBOARD. BOTH READ AND WRITE DRQS ARE DELAYED AT LEAST 800 nS (1600 nS FOR 5¼" DRIVES).

A SIGNAL DIAGRAM SHOWING THE SEQUENCE OF EVENTS IS ON THE NEXT PAGE.

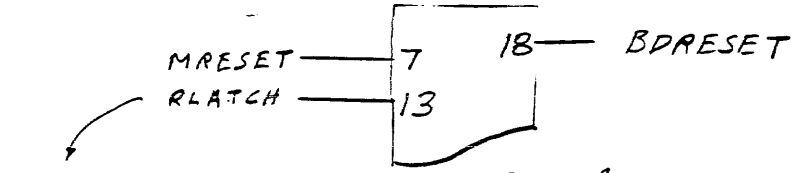
MDRQT AND START (CONTINUED)



1. THE DMA CYCLE BEGINS WHEN THE 8272 SENDS OUT DRQ, WHICH CAUSES START TO GO LOW WHICH LETS THE RC NETWORK BEGIN TO DECAY.
2. WHEN THE RC DECAYS TO LOGIC ZERO OF A SCHMITT TRIGGER, DELAY GOES HIGH, WHICH MAKES MDRQT GO ACTIVE TO THE BASEBOARD (THE REASON WE DID THIS), WHICH MAKES START GO HIGH, WHICH ALLOWS THE RC TO RECHARGE TO BE READY FOR THE NEXT CYCLE.
3. WHEN THE RC CHARGES TO LOGIC HIGH OF A SCHMITT TRIGGER, DELAY GOES LOW AGAIN.
4. WHEN DACK FROM THE BASEBOARD GOES ACTIVE, MDRQT IS REMOVED. LATER, THE 8272 REMOVES DRQ.

```
PAL16L8                          PAL DESIGN SPECIFICATION
PAT NO 218AU19A                  GEORGE ARRIGOTTI 4-6-83
IO PORTS PAL AT U19

QUAL MCS1 IORD IOWRT MA1 MA2 MRESET EXTEND MDACK GND
CLK3 DACK RLATCH RDW ALATCH MDO MLATCH BDRESET WAIT VCC

IF (VCC) /BDRESET = /MRESET * /RLATCH

IF (VCC) /MLATCH = BDRESET +
                   /IOWRT * /MCS1 * MA2 * /MA1 * /MDO +
                   /MDO * /MLATCH +
                   IOWRT * /MLATCH +
                   MCS1 * /MLATCH +
                   /MA2 * /MLATCH +
                   MA1 * /MLATCH

IF (VCC)    /RDW = EXTEND * /CLK3 +
                   /CLK3 * /RDW +
                   /EXTEND * /RDW

IF (/MCS1 * MA2 * /IORD) /MDO = /MA1 * /MLATCH +
                                MA1 * /ALATCH

IF (VCC) /ALATCH = BDRESET +
                   /MDO * /ALATCH +
                   /IOWRT * /MCS1 * MA2 * MA1 * /MDO +
                   IOWRT * /ALATCH +
                   MCS1 * /ALATCH +
                   /MA2 * /ALATCH +
                   /MA1 * /ALATCH

IF (VCC) /RLATCH = MRESET +
                   /IOWRT * /MCS1 * /MA2 * MA1 * /MDO +
                   /MDO * /RLATCH +
                   IOWRT * /RLATCH +
                   MCS1 * /RLATCH +
                   MA2 * /RLATCH +
                   /MA1 * /RLATCH

IF (VCC)   /DACK = QUAL * /MDACK * /IORD +
                   QUAL * /MDACK * /IOWRT +
                   /QUAL * /MDACK +
                   /IORD * /MA1 * /MA2 * /MCS1 +
                   /IOWRT * /MA1 * /MA2 * /MCS1

IF (VCC)   /WAIT = MDACK * MCS1 +
                   MDACK * MA1 +
                   MDACK * MA2

DESCRIPTION OF PINS

DACK - DMA ACKNOWLEDGE TO 8272.
BDRESET - RESET TO SBX BOARD.
RLATCH - PROGRAMMABLE RESET LATCH.
MLATCH - MOTOR ON/OFF LATCH.
ALATCH - AUXILIARY LATCH. MAY BE USED FOR DMA TERMINAL COUNT.
EXTEND,CLK3,RDW - READ WINDOW SIGNALS.
MCS1,IORD,IOWRT,MA1,MA2,MDO,MWAIT,MRESET,MDACK - STANDARD SBX SIGNALS.
QUAL - INPUT TO SELECT BETWEEN COMMAND-QUALIFIED DACK AND
   UNQUALIFIED DACK
WAIT - USED WITH RC DELAY CIRCUIT TO PRODUCE MWAIT TO THE SBX
   TO EXTEND DACK.
```

PAL U19 OUTPUT PIN 18 BDRESET
(BOARD RESET)

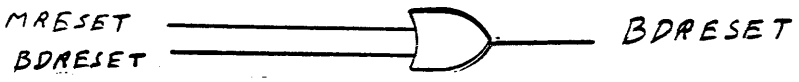


RLATCH IS AN OUTPUT OF THE PAL, BUT IS USED INTERNALLY AS AN INPUT IN THIS CIRCUIT.

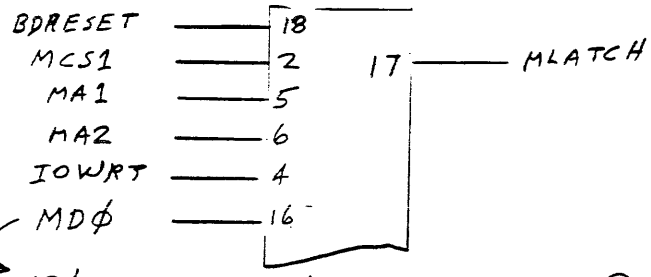
EQUATION: /BDRESET = /MRESET * /RLATCH

PAL CIRCUIT:

ALTERNATE REPRESENTATION:



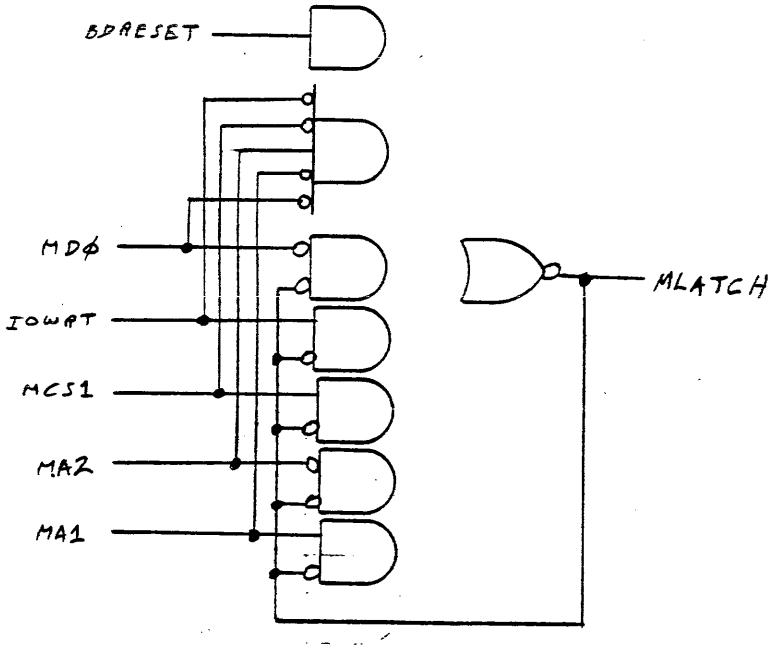
PAL U19 OUTPUT PIN 17 LATCH 0 (MOTOR LATCH)



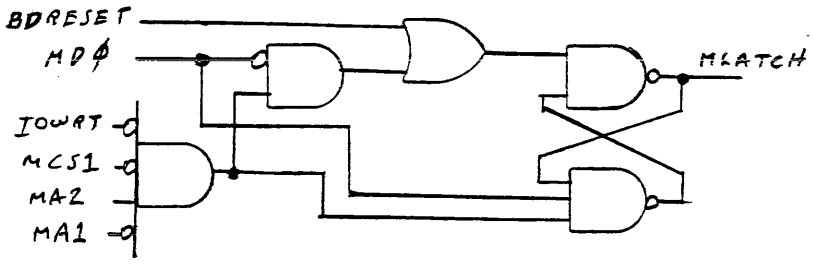
MDØ IS ALSO USED AS AN OUTPUT WHEN READING MOTOR LATCH.
BDRESET IS ALSO USED AS AN OUTPUT.

EQUATION: /MLATCH = BDRESET +
/IOWRT * /MCS1 * MA2 * /MA1 * /MDØ +
/MDØ * /MLATCH + IOWRT * /MLATCH +
MCS1 * /MLATCH + /MA2 * /MLATCH +
MA1 * /MLATCH

PAL CIRCUIT:

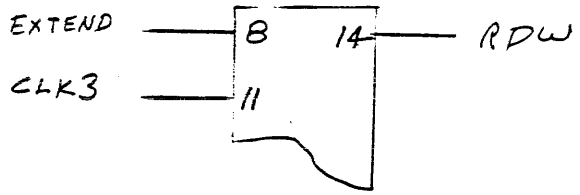


ALTERNATE REPRESENTATION



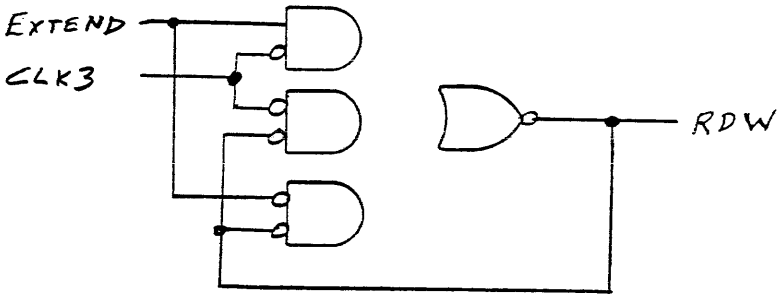
NOTES: BDRESET TURNS THE MOTOR OFF (MLATCH LOW). AN IO WRITE TO THIS ADDRESS WITH BIT 0 = 1 TURNS THE MOTOR ON; WITH BIT 0 = 0 TURNS THE MOTOR OFF. MLATCH GOES THROUGH AN INVERTING BUFFER BEFORE GOING TO THE DRIVE INTERFACE WHERE IT IS ACTIVE LOW. MLATCH CAN BE READ BY DOING AN IO READ TO THE SAME ADDRESS. SEE MDØ OUTPUT PAGE FOR DETAILS.

PAL U19 OUTPUT PIN 14 RDW
(READ WINDOW)

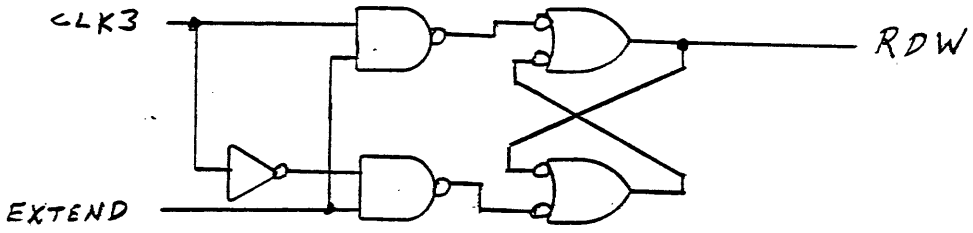


EQUATION: /RDW = EXTEND * /CLK3 +
/CLK3 * /RDW +
/EXTEND * /RDW

PAL CIRCUIT:

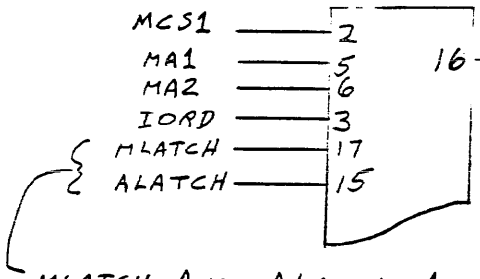


ALTERNATE REPRESENTATION:



NOTES: THIS FUNCTION USED 12 PINS OF U7 ON THE 218 NON A. SINCE IT REQUIRES ONLY 3 PINS OF THE 16L8, THE REST OF THE PAL IS AVAILABLE FOR THE NEW 218A FEATURES.

PAL U19 Output Pin 16 MDϕ

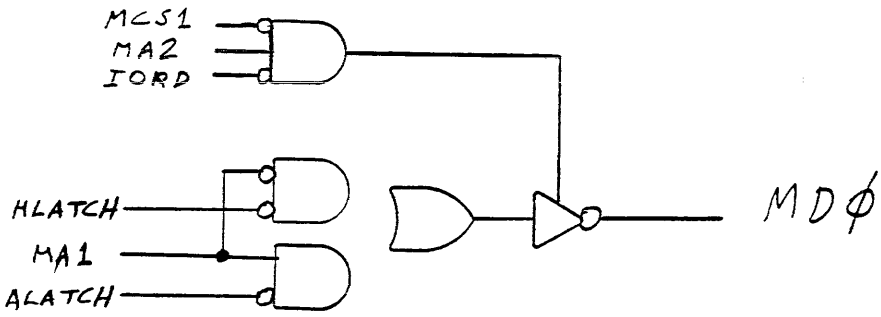


MDϕ is also used as an input for other functions in this PAL.

MLATCH and ALATCH are PAL output pins, but are used internally for this circuit.

EQUATION: IF (/MCS1 * MA2 * /IORD) /MDϕ = /MA1 * /MLATCH + MA1 * /ALATCH

PAL CIRCUIT:

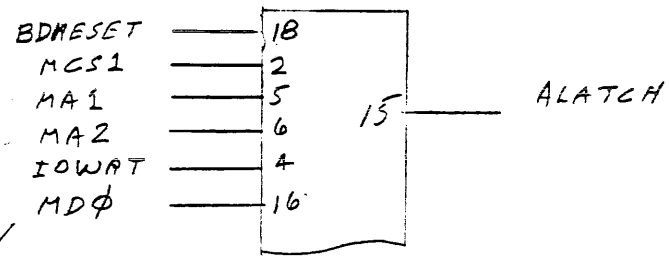


NOTES:

Usually MDϕ is strictly an input, used for writing to the motor latch, reset latch, and auxiliary latch. However, when an I O read is done to either the motor latch or the auxiliary latch, MDϕ becomes an output, driving the state of the selected latch onto the data bus. The "sense" of the data is the same as when the latches are written.
Bit 0 = 1 means latch high (motor on, or TC active).
Bit 0 = 0 means latch low (motor off, or TC inactive).

PAL U19 OUTPUT PIN 15

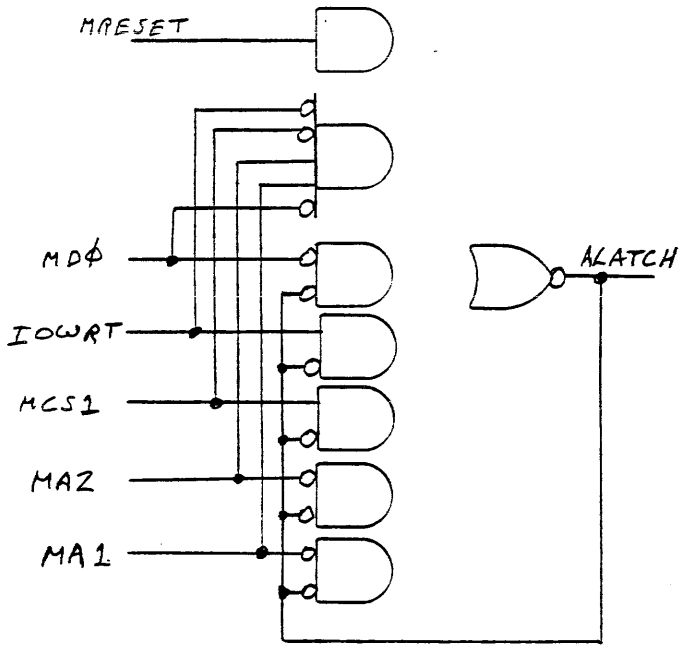
LATCH 1
(AUXILIARY LATCH)



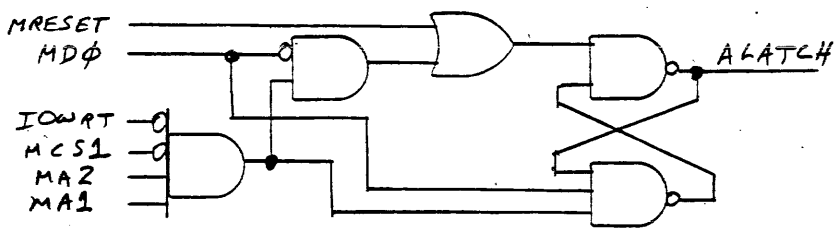
* MDØ IS ALSO USED AS AN OUTPUT WHEN READING ALATCH. BDRESET IS ALSO USED AS AN OUTPUT.

EQUATION: /ALATCH = BDRESET +
/IOWRT * /MCS1 * MA2 * MA1 * /MDØ +
/MDØ * /ALATCH + IOWRT * /ALATCH +
MCS1 * /ALATCH + /MA2 * /ALATCH +
/MA1 * /ALATCH

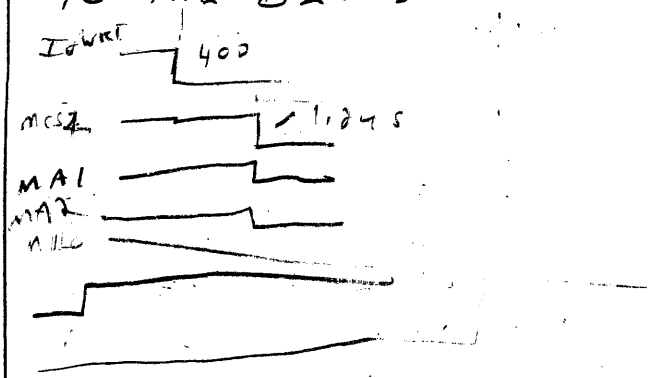
PAL CIRCUIT:



ALTERNATE REPRESENTATION:

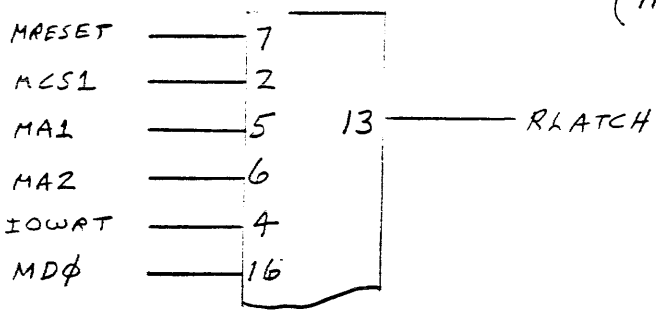


NOTES: MRESET FORCES ALATCH LOW. AN I O WRITE TO THIS ADDRESS WITH BIT 0=/ SETS ALATCH HIGH; WITH BIT 0=0 SETS ALATCH LOW. ALATCH MAY BE USED TO DRIVE TERMINAL COUNT (TC) TO THE 8272.



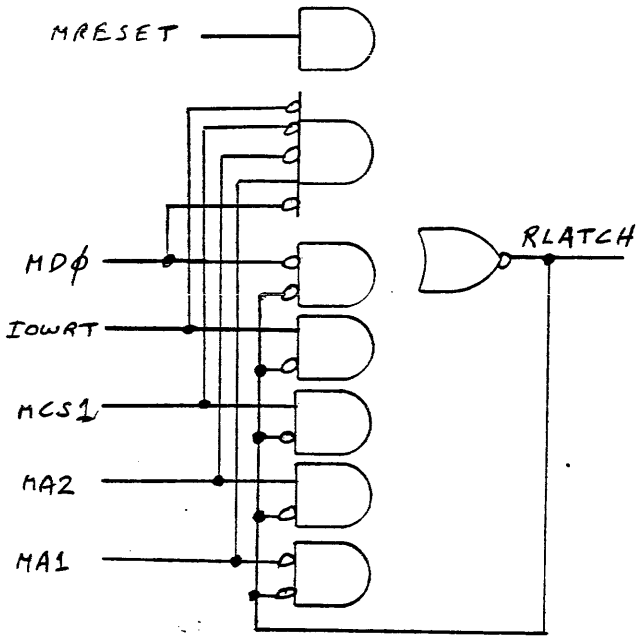
ALATCH CAN BE READ BY DOING AN I O READ TO THE SAME ADDRESS. SEE MDØ OUTPUT PAGE FOR DETAILS.

PAL U19 OUTPUT PIN 13 RLATCH (RESET LATCH)



EQUATION: /RLATCH = MRESET +
/IOWRT * /MCS1 * /MA2 * MA1 * /MDϕ +
/MDϕ * /RLATCH + IOWRT * /RLATCH +
MCS1 * /RLATCH + MA2 * /RLATCH +
/MA1 * /RLATCH

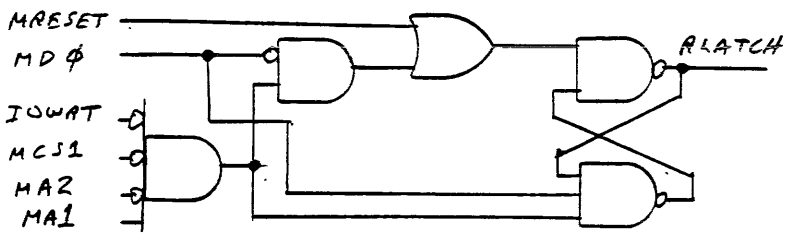
PAL CIRCUIT:



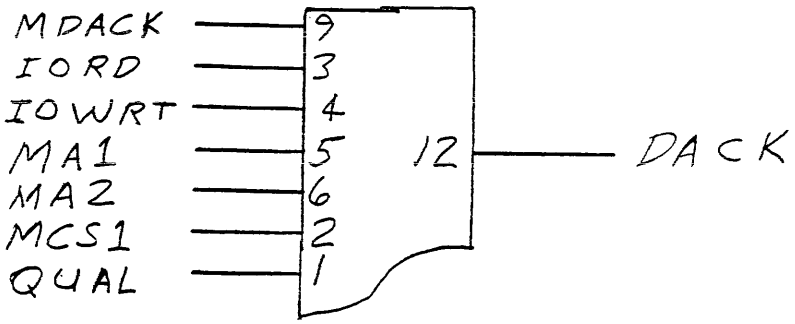
NOTES: MRESET FORCES RLATCH INACTIVE (LOW). AN IO WRITE TO THIS ADDRESS WITH BIT 0 = 1 MAKES RLATCH ACTIVE; WITH BIT 0 = 0 MAKES RLATCH INACTIVE. RLATCH CANNOT BE READ.

RLATCH IS NOT CONNECTED TO OTHER DEVICES ON THE BOARD. IT IS ONLY USED INTERNAL TO THE PAL.

ALTERNATE REPRESENTATION:



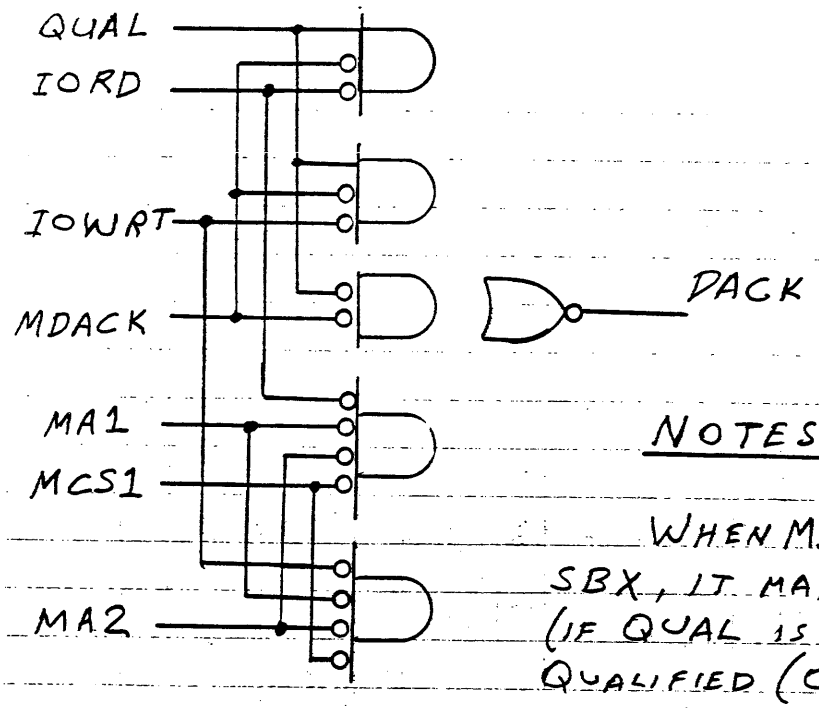
PAL U19 OUTPUT PIN 12 DACK
(DMA ACKNOWLEDGE)



EQUATION:

$$
\begin{aligned}
/DACK = {} & QUAL * /MDACK * /IORD + \\
& QUAL * /MDACK * /IOWRT + \\
& /QUAL * /MDACK + \\
& /IORD * /MA1 * /MA2 * /MCS1 + \\
& /IOWRT * /MA1 * /MA2 * /MCS1
\end{aligned}
$$

PAL CIRCUIT:

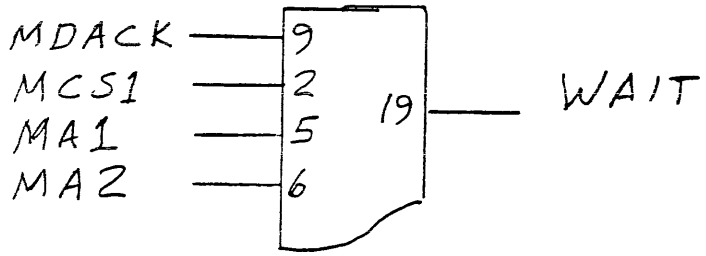


NOTES:

WHEN MDACK IS AVAILABLE ON THE SBX, IT MAY BE QUALIFIED BY COMMAND (IF QUAL IS TIED HIGH) OR NOT QUALIFIED (QUAL TIED LOW).

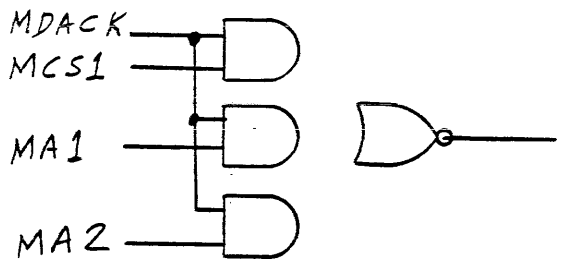
WHEN THE DACK GENERATOR OPTION IS USED, THE BASEBOARD WRITES OR READS WITH MA1, MA2 LOW, AND THE PAL SENDS DACK TO THE 8272.

PAL U19 OUTPUT PIN 19 WAIT

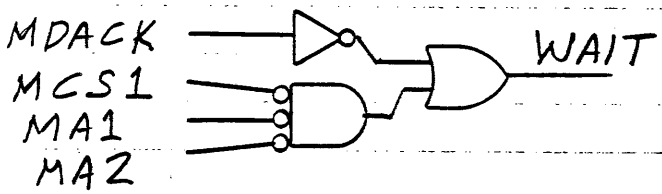


EQUATION: /WAIT = MDACK * MCS1 +
MDACK * MA1 +
MDACK * MA2

PAL CIRCUIT:



ALTERNATE REPRESENTATION:

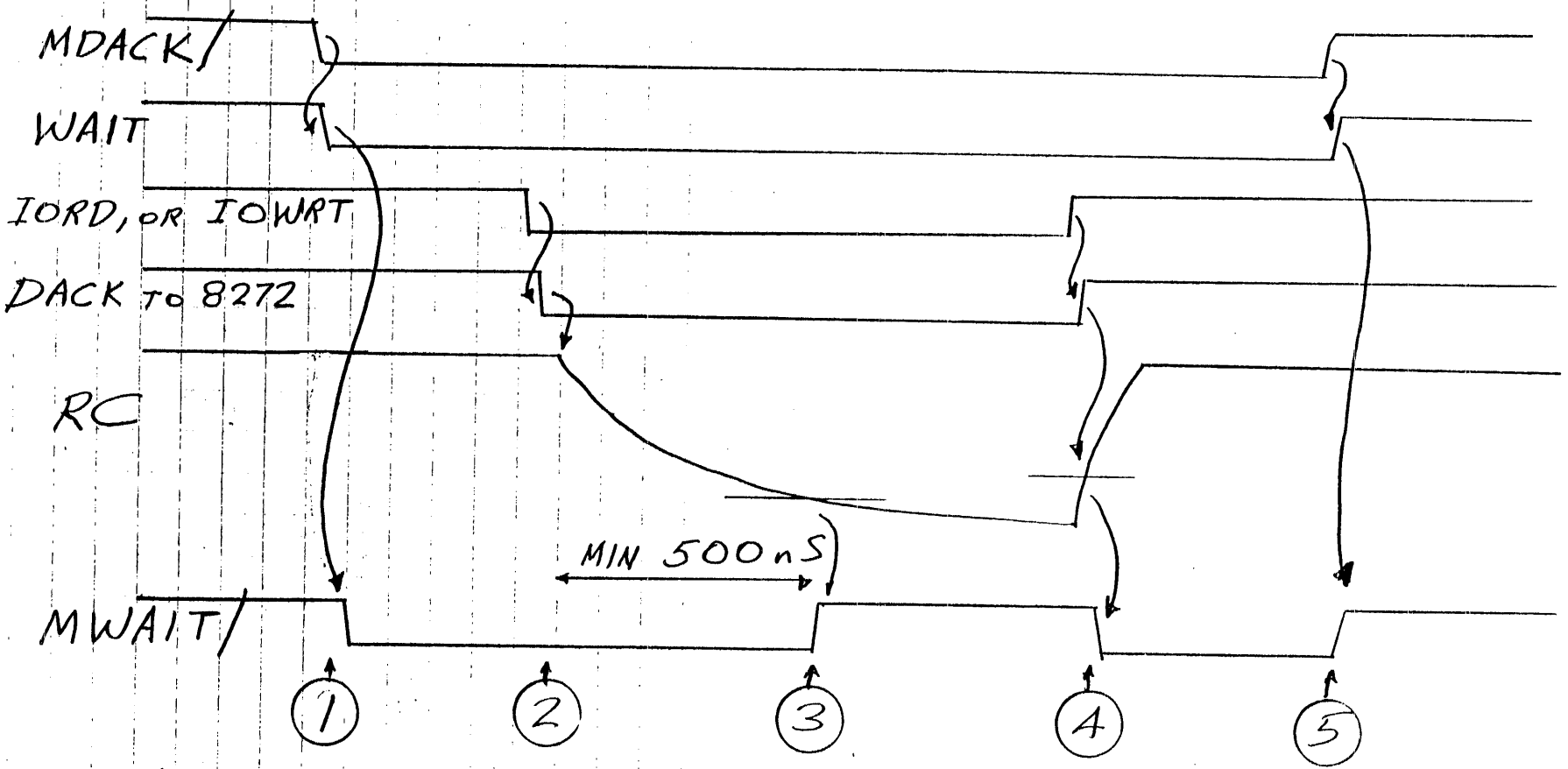


NOTES:

WAIT IS HIGH WHENEVER MDACK IS ACTIVE (LOW) OR WHEN MCS1, MA1, MA2 ARE LOW (MEANING THAT A WRITE OR READ TO THE DACK GENERATOR IS ABOUT TO OCCUR).

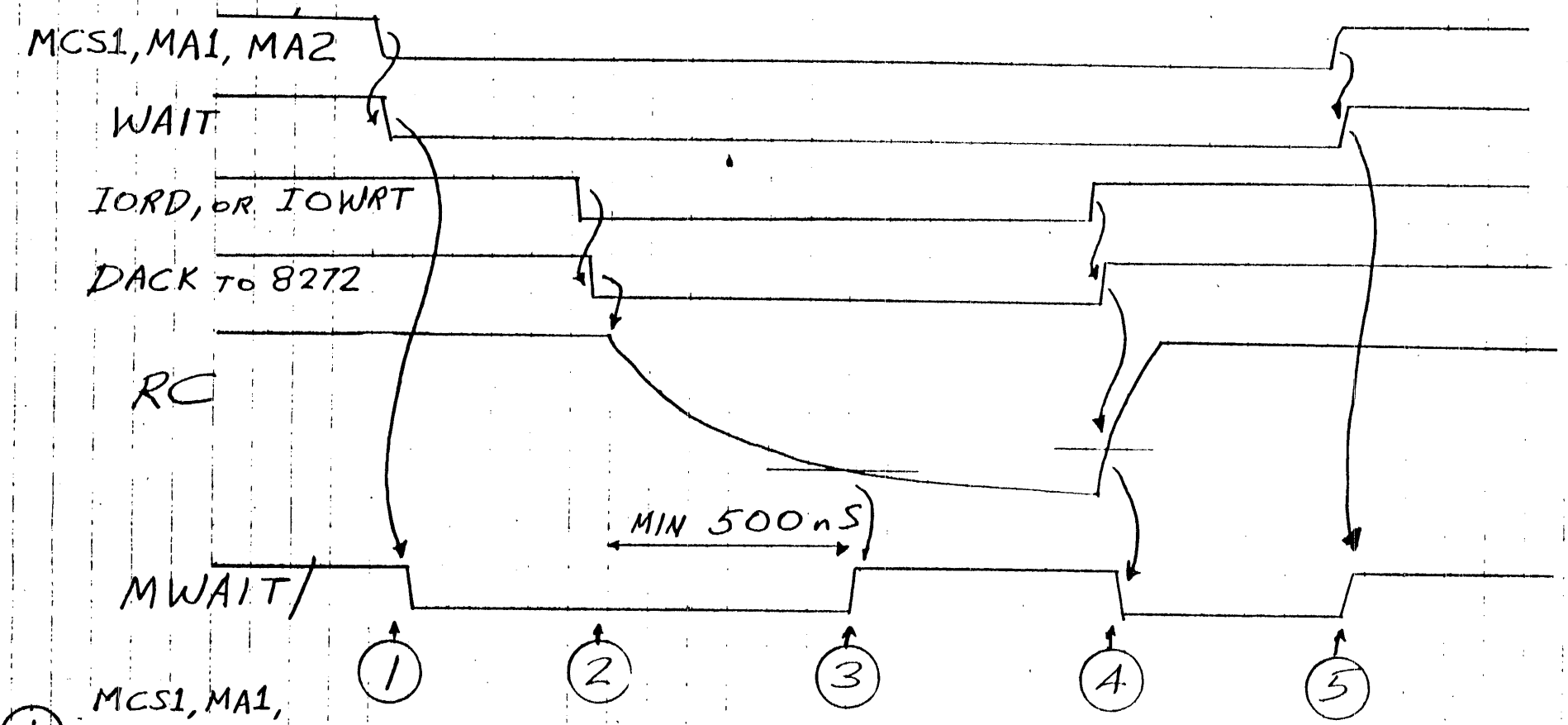
SIGNAL DIAGRAMS SHOWING THE MWAIT SEQUENCE OF EVENTS ARE ON THE NEXT TWO PAGES.

MWAIT GENERATOR WHEN SBX DACK IS USED



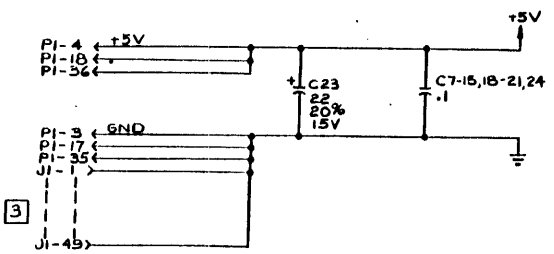
1. MDACK/ FROM THE BASEBOARD GOES ACTIVE, WHICH MAKES WAIT (PAL OUTPUT) GO LOW, WHICH MAKES MWAIT/ GO ACTIVE.
2. COMMAND ARRIVES, SO THE PAL NOW GATES DACK THROUGH TO THE 8272. (THIS ASSUMES QUALIFIED DACK WAS JUMPERED).
3. DACK GOING LOW LETS THE RC START TO DECAY. THE RC DISCHARGES DOWN TO SCHMITT TRIGGER LOGIC LOW WHICH CAUSE MWAIT TO GO HIGH, INDICATING TO THE CPU THAT NO MORE WAIT STATES BE INSERTED.
4. COMMAND ENDS, SO DACK ENDS, AND RC RECHARGES. WHEN IT REACHES SCHMITT TRIGGER HIGH, MWAIT GOES LOW AGAIN (NO EFFECT ON CPU).
5. MDACK/ ENDS, SO WAIT AND MWAIT BOTH END.

MWAIT GENERATOR WHEN DACK GENERATOR IS USED



1. MCS1, MA1, AND MA2 FROM THE BASEBOARD GO ACTIVE, WHICH MAKES WAIT (PAL OUTPUT) GO LOW, WHICH MAKES MWAIT/ GO ACTIVE.
2. COMMAND ARRIVES, SO THE PAL PRODUCES DACK AND SENDS IT TO THE 8272 (THIS IS THE DACK GENERATOR).
3. DACK GOING LOW LETS THE RC START TO DECAY. THE RC DISCHARGES DOWN TO SCHMITT TRIGGER LOGIC LOW WHICH CAUSE MWAIT TO GO HIGH, INDICATING TO THE CPU THAT NO MORE WAIT STATES BE INSERTED.
4. COMMAND ENDS, SO DACK ENDS, AND RC RECHARGES. WHEN IT REACHES SCHMITT TRIGGER HIGH, MWAIT GOES LOW AGAIN (NO EFFECT ON CPU).
5. MCS1, MA1, MA2 END, SO WAIT AND MWAIT BOTH END.

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO 40-3900	R.K.	11/7/83	KA	11/7/83	[illegible]	[illegible]



DEVICE TABLE

REFERENCE DESIGNATIONS	DEVICE TYPE	POWER PINS GND	POWER PINS +5V	UNUSED LOGIC ELEMENT OUTPUT PINS
U14	8272	20	40	
U10,15,19	PAL 16L8	10	20	
U5	74S02	7	14	
U7,12	74S74	7	14	
U6,13,16,17	74S112	8	16	
U1	74S124	9	16	
U18	74LS132	7	14	
U11	74157	8	16	
U9	74S175	8	16	
U2,8	74S240	10	20	
U4	74S241	10	20	
U20	74LS393	7	14	
U21	9602	8	16	
U3	74LS123	8	16	U3-13

DISK SIZE SELECT	
8"	5 1/4"
E42-E43	E43-E44
E55-E56	E56-E57
E59-E60	E58-E59
E62-E63	E61-E62
——	E64-E65
E69-E70	E68-E69

WRITE PRECOMPENSATION	
250nS	125nS
E25-E26	E24-E25
E30-E31	E31-E32

WRITE PRECOMPENSATION	
INNER TRACKS ONLY	ALL TRACKS
E27-E28	E28-E29

DMA MODE		
DMA WITH DACK FROM P1	DMA WITH PROGRAMMED DACK	NO DMA
E52-E53	E55-E54	E53-E54

DACK TO 8272	
QUALIFIED BY COMMANDS	NOT QUALIFIED BY COMMANDS
E36-E37	E35-E36

I/O PORT FEATURES (LATCH0, LATCH1, PROGRAMMED RESET, PROGRAMMED DACK)	
ENABLED	DISABLED
E49-E50	E50-E51

NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS, +80%,-20%, 50V.
2. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%
3. ALL ODD NUMBERED PINS OF J1 ARE CONNECTED TO GROUND.

UNUSED RP RESISTORS
RP1-2
RP2-5,8
RP3-7

REF DESIGNATIONS	
LAST USED	NOT USED
C26	
E70	
V1	
J1	
P1	
Q2	
R20	
RP9	
TP2	
U21	
CR2	

UNLESS OTHERWISE SPECIFIED
1 DIMENSIONS ARE IN INCHES
2 BREAK ALL SHARP EDGES
3 DO NOT SCALE DRAWING
4 TOLERANCES
ANGLES ±
XX ±
XXX ±

QUANTITY PER DASH NO

ITEM NO	DESCRIPTION
	PARTS LIST

	SIGNATURE	DATE
DRN BY	R. K. Chan	4/83
CHK BY	[illegible]	[illegible]
ENGR APVD	[illegible]	[illegible]
APVD		
APVD		

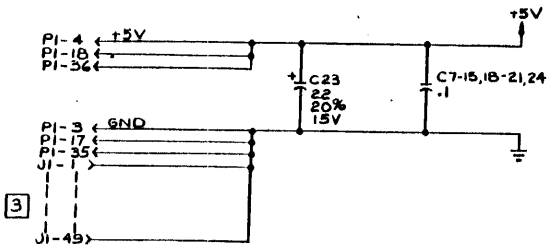
intel® 3065 BOWERS AVE SANTA CLARA CALIF 95051

TITLE: SCHEMATIC SBX 218A FLEXIBLE DISKETTE CONTROLLER

SIZE	DEPT	EC LOG	ASSY LVL	DOCUMENT NUMBER	REV
D	40	0100	——	145593	A

NEXT ASSY | SHEET 1 OF 2

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO 40-3900	R.K.	11/3/83	RA	11/3/83	[illegible]	[illegible]



DEVICE TABLE

REFERENCE DESIGNATIONS	DEVICE TYPE	POWER PINS GND	POWER PINS +5V	UNUSED LOGIC ELEMENT OUTPUT PINS
U14	8272	20	40	
U10,15,19	PAL 16L8	10	20	
U5	74S02	7	14	
U7,12	74S74	7	14	
U6,13,16,17	74S112	8	16	
U1	74S124	9	16	
U18	74LS132	7	14	
U11	74157	8	16	
U9	74S175	8	16	
U2,8	74S240	10	20	
U4	74S241	10	20	
U20	74LS393	7	14	
U21	9602	8	16	
U3	74LS123	8	16	U3-13

DISK SIZE SELECT	
8"	5 1/4"
E42-E43	E43-E44
E55-E56	E56-E57
E59-E60	E58-E59
E62-E63	E61-E62
———	E64-E65
E69-E70	E68-E69

WRITE PRECOMPENSATION	
250ns	125ns
E25-E26	E24-E25
E30-E31	E31-E32

WRITE PRECOMPENSATION	
INNER TRACKS ONLY	ALL TRACKS
E27-E28	E28-E29

DMA MODE		
DMA WITH DACK FROM P1	DMA WITH PROGRAMMED DACK	NO DMA
E52-E53	E55-E54	E53-E54

DACK TO 8272	
QUALIFIED BY COMMANDS	NOT QUALIFIED BY COMMANDS
E36-E37	E35-E36

I/O PORT FEATURES (LATCH Ø, LATCH 1, PROGRAMMED RESET, PROGRAMMED DACK)	
ENABLED	DISABLED
E49-E50	E50-E51

NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS, +80%,-20%, 50V.
2. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%
3. ALL ODD NUMBERED PINS OF J1 ARE CONNECTED TO GROUND.

UNUSED RP RESISTORS
RP1-2
RP2-5,8
RP3-7

REF DESIGNATIONS	
LAST USED	NOT USED
C26	
E70	
V1	
J1	
P1	
Q2	
R20	
RP4	
TP2	
D21	
CR2	

QUANTITY PER DASH NO

UNLESS OTHERWISE SPECIFIED
1. DIMENSIONS ARE IN INCHES
2. BREAK ALL SHARP EDGES
3. DO NOT SCALE DRAWING
4. TOLERANCES: ANGLES ± ; XX ± ; XXX ±

ITEM NO	DESCRIPTION
	PARTS LIST

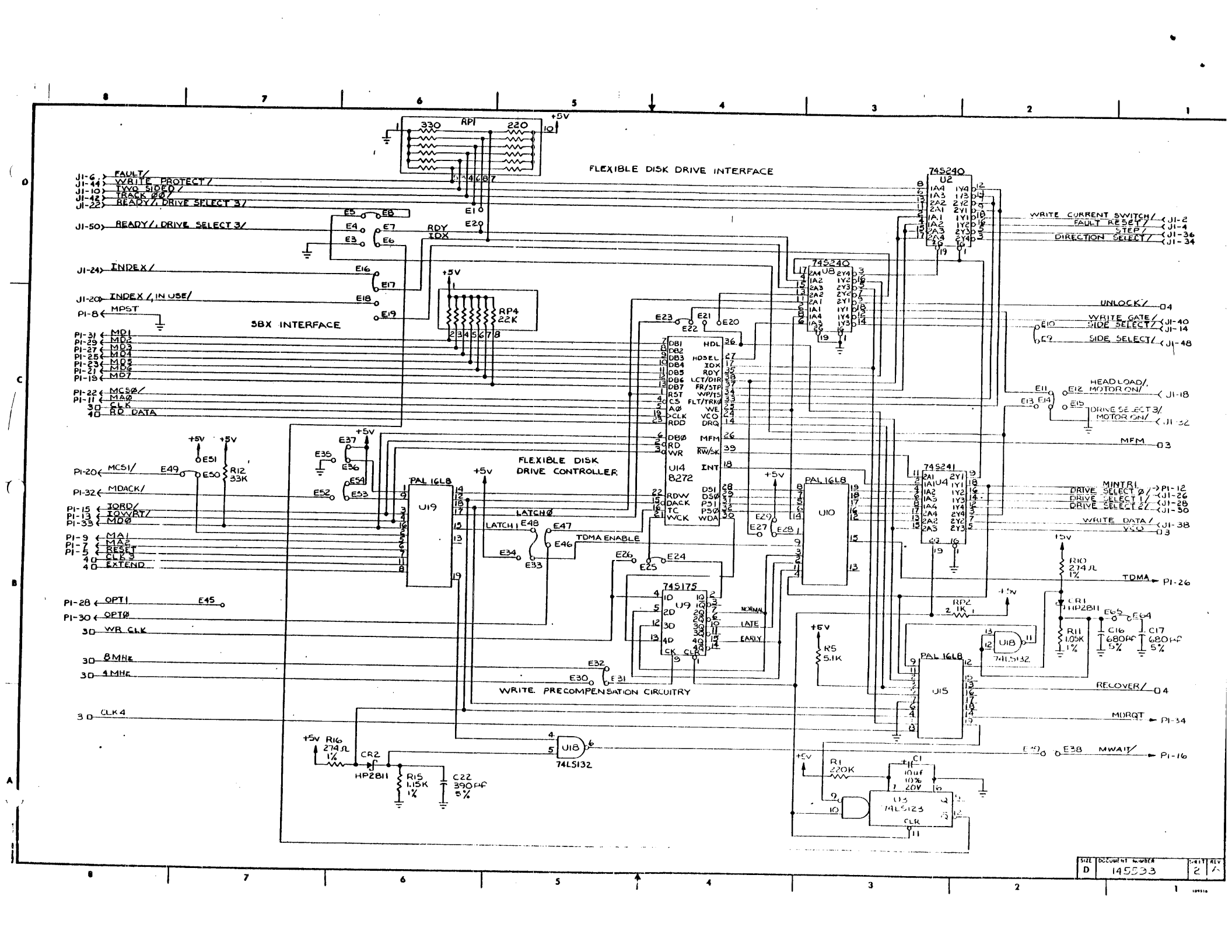
	SIGNATURE	DATE
DRN BY	[illegible]	4/84
CHK BY	[illegible]	4/84
ENGR APVD	[illegible]	4/84
APVD		
APVD		

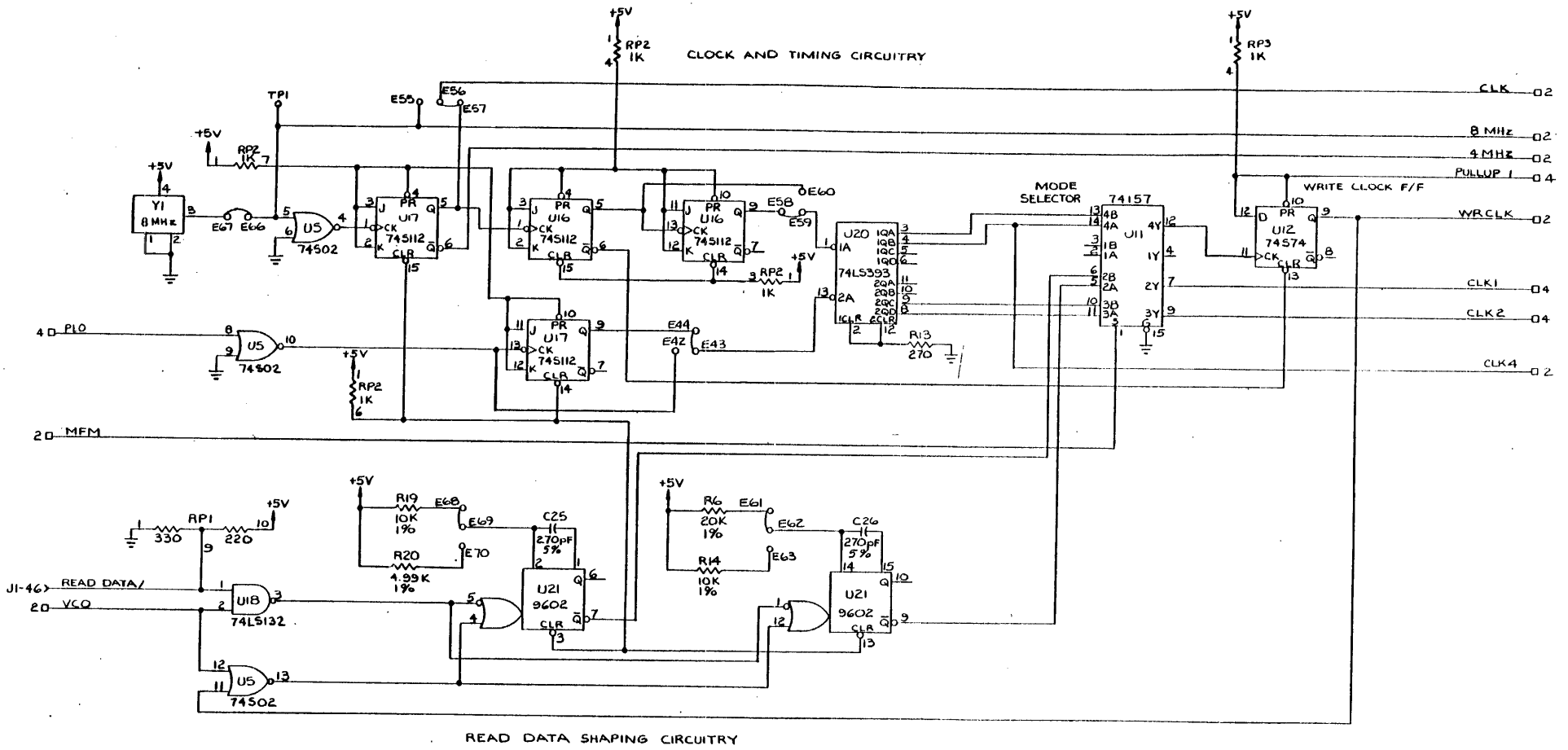
intel® 3065 BOWERS AVE SANTA CLARA CALIF 95051

TITLE: iSBC 218A FLEXIBLE DISKETTE CONTROLLER

SIZE	CODE IDENT NO	DWG NO	REV	DOCUMENT NUMBER	REV
D	04000			145593	A

SCALE: NONE SHEET 1 OF 2


FLEXIBLE DISK DRIVE INTERFACE
SBX INTERFACE
FLEXIBLE DISK DRIVE CONTROLLER
WRITE PRECOMPENSATION CIRCUITRY
RP1
330
220
RP4
22K
74S240
U2
74S240
U8
74S241
U4
8272
U14
PAL 16L8
U19
PAL 16L8
U10
PAL 16L8
U15
74S175
U9
74LS132
U18
74LS123
U3
+5V
FAULT/
WRITE PROTECT/
TWO SIDED/
TRACK Ø0/
READY/, DRIVE SELECT 3/
READY/, DRIVE SELECT 3/
INDEX/
INDEX/, IN USE/
MPST
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MCSØ/
MAØ
CLK
RD DATA
MCS1/
MDACK/
IORD/
IOWRT/
MDØ
MA1
MA2
RESET
CLK 3
EXTEND
OPT1
OPTØ
WR CLK
8 MHz
4 MHz
CLK 4
WRITE CURRENT SWITCH/
FAULT RESET/
STEP/
DIRECTION SELECT/
UNLOCK/
WRITE GATE/
SIDE SELECT1/
SIDE SELECT/
HEAD LOAD/, MOTOR ON/
DRIVE SELECT 3/, MOTOR ON/
MFM
MINTRI
DRIVE SELECT Ø/
DRIVE SELECT 1/
DRIVE SELECT 2/
WRITE DATA/
VCO
TDMA
RECOVER/
MDRQT
MWAIT/
LATCHØ
LATCH1
TDMA ENABLE
NORMAL
LATE
EARLY
HDL
HDSEL
IDX
RDY
LCT/DIR
FR/STP
WP/TS
FLT/TRKØ
WE
VCO
DRQ
MFM
RW/SK
INT
DSI
DSØ
PSI
PSØ
WDA
RDW
DACK
TC
WCK
R10 274Ω 1%
R11 1.05K 1%
C16 680pF 5%
C17 680pF 5%
R5 5.1K
RD2 2.1K
R1 220K
C1 10uf 10% 20V
R16 274Ω 1%
R15 1.15K 1%
C22 390pF 5%
CR1 HP2811
CR2 HP2811
R12 33K
SIZE D
DOCUMENT NUMBER 145533
SHEET 2
REV A



SIZE	DOCUMENT NUMBER	SHEET	REV
D	145593	3	A