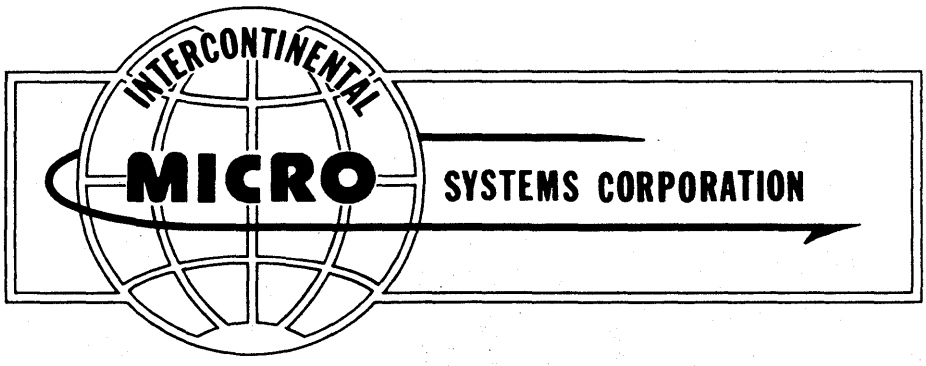
INTERCONTINENTAL MICRO SYSTEMS CORP.

CPS - MX

S-100 BUS
SINGLE BOARD SLAVE PROCESSOR



1733 South Douglas Road, Suite E • Anaheim, California • (714) 978-9758 • Telex: 678401 — TAB-IRIN

**** INTRODUCTION ****

The **Intercontinental Micro Systems Corp.** (ICM) CPS-MX single board slave processor is a Z80A (tm) or Z80B (tm) based computer complying with the IEEE 696.1/D2 S100 Bus specification. This computer incorporates all features necessary for a complete stand alone system, each to be dedicated to a user in a distributed processor system utilizing operating systems such as TurboDos (tm) and CP/NET (tm).

The CPS-MX processors together with an S100 Bus master (host) like the ICM CPZ 48000 SBCP constitute a high performance, high throughput network which can be integrated into most S100 Bus mainframes. The master/slave communications take place over the S100 Bus via slave/host bidirectional memory transfers under control of the host processor. This memory mapping technique thoroughly enhances data throughput and reduces overhead hardware resulting in a high performance, low cost slave processor, making distributed processing comparable to mainframe performance at a fraction of the cost.

FEATURES

* IEEE 696.1/D2 S100 Bus compliance.
* Z80A 4 mhz (CPS-4X) or Z80B 6 mhz (CPS-6X) operation.
* Compatible with CPZ 48000 SBCP, any Z80A based CPU with extended address compatibility or 16 bit based CPUs complying with IEEE 696.1/D2 Bus specification.
* Two synchronous (CPS-MS) or asynchronous (CPS-MA) serial I/O ports.
* Two parallel I/O ports; eight data bits and two handshake lines per port.
* TURBOdos and CP/NET compatible.
* 64 Kbytes of onboard dynamic RAM.
* Master/slave memory-to-memory transfers under DMA control at 571 Kbytes/sec transfer rate when used with CPZ-48000 SBCP.
* Master confiscation of slave memory for diagnostic purposes.
* Software selectable baud rates.
* Usable as an intelligent I/O processor in single user systems.
* Usable as a 64 Kbyte RAM by the host in either single-user or multi-user systems.

PERFORMANCE SPECIFICATIONS

Processor
  Clock Rate
    CPS-4X.....4 MHz
    CPS-6X.....6 MHz
Type
    CPS-4X.....Z80A
    CPS-6X.....Z80B

Bus Interface.....IEEE 696.1/D2 S100
Status, control, data and address. Slave I/O port address switch-selectable for address range from 00h to FFh. Slave memory address switch-selectable for address range from 010000h to FFFFFFh.

I/O CHANNELS:
  Serial I/O channels (two ports)
    CPS-4A (asynchronous).....up to 50 Kbaud
    CPS-6A (asynchronous).....up to Kbaud
    CPS-4S (synchronous).....up to 800 Kbaud
    CPS-6S (synchronous).....up to Kbaud

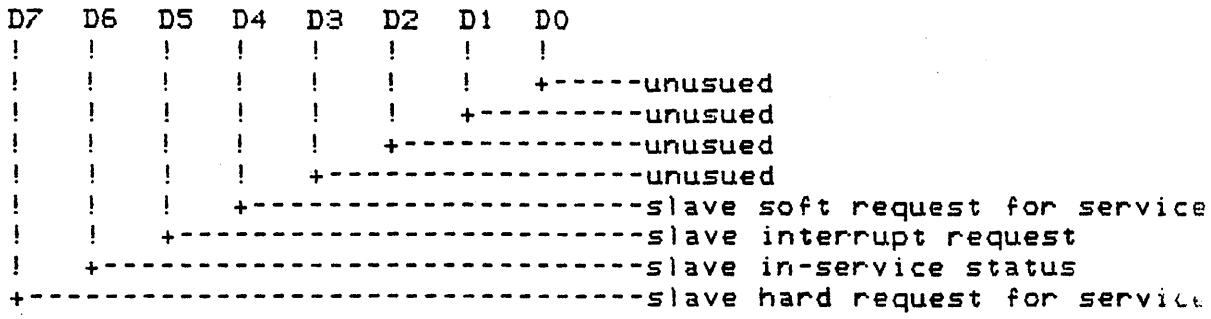
    I/O Interface.....through personality boards such as Dumb terminal, RS232 modem, and RS422 interface boards.

  Parallel I/O channels (two ports)
    Data rate.....up to 300 Kbytes/sec.
    Interface signals ..... eight data lines plus two handshaking lines per port.
    I/O interface.....through personality boards such as centronics printer, Priam and ST506 intelligent hard disk interface boards.

64 KBYTE DYNAMIC RAM:
  Wait states.....none required
  Direct memory transfers.....to/from CPZ-48000 SBCP
    Data transfer rate (non-DMA).....190 Kbytes/sec
    Data transfer rate (DMA).....571 Kbytes/sec

  Memory address.....switch selectable in the 64 Kbyte boundries for a total of 256 Kbyte pages.

STATUS PORT BIT ASSIGNMENTS:



COMMAND PORT BIT ASSIGNMENTS:

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	-----master clear slave reset
0	0	0	0	0	0	0	1	-----master confiscate slave's memory
0	0	0	0	0	0	1	0	-----master acKnowledge slave's reques
0	0	0	0	0	0	1	1	-----master release slave to run
1	0	0	0	0	0	0	0	-----master reset slave
0	1	0	0	0	0	0	0	-----master request to slave
0	0	1	0	0	0	0	0	-----master interrupt to slave

**** FUNCTIONAL DESCRIPTION ****

The CPS-MX is functionally partitioned into the following major groups:

- --CPU/64 Kbyte dynamic RAM/control
  - --64 Kbyte Ram
  - --CPU/S100 address multiplexor
  - --address multiplexor
  - --RAS/CAS generator
  - --REFRESH generator/control
- --Slave Processor Control Logic
  - --slave processor chip select/command decoder
  - --slave request logic
    - --hard request logic
    - --soft request logic
    - --interrupt request logic
- --Slave Clock Generator
- --Reset Generator
- --Input/output Structure
  - --serial I/O port control
  - --parallel I/O port control

--S100 Bus Interface
--status/control signals receivers
--data receivers/data transmitters

Each group is described below to give the user a clear undersanding of the hardware and software setup option. Prior to describing each group, a "thumbnail sketch" of the overall function of the CPS-MX is hereby described.

(1) Master/slave Action at Reset Time

At powerup, master reset or slave reset time, a slave service request flag (hard request) is raised and the slave CPU is tri-stated. During this time, the slave's 64 Kbyte RAM is addressable by the S100 Bus address lines A0-A23. Address lines A0-A15 address the 64 Kbyte RAM and A16-A23 select the page in which the 64 Kbyte section lies in the master's address range. The request flag in this case is referred to as the slave's "hard request" flag in that the slave CPU is immediately tri-stated and the memory is put into extended refresh. The master commences to poll slave request flags via I/O port status read commands. Upon determining that a slave requires service, the master issues an I/O port acknowledge command which transfers control of the slave memory to the master. The master can then "map" the slave memory into its address space. The master may then down-load the slave's operating system into the slave's memory. At the completion of this transfer, the master issues an I/O port reset command to the slave followed by a command which causes the slave's tri-state condition to be released. The slave then commences to execute program intructions deposited by the master resulting in execution of the slave's operating system. Thus, a "cold-boot" operation is executed.

(2) Master/slave Action during File Transfers

This operation is quite similar to the action described above. When a slave requires the transfer of files to or from the master, a "soft-request" flag is raised. This means that a flag is raised but without the slave's CPU going into tri-state immediately as in paragraph (1) above. The master, upon determining that slave service is required, will then issue a service acknowledge command as previously described. It is only then that the slave is tri-stated and that the slave's memory is relinquished to the master as previously described. The slave's program execution is suspended for the duration of the master's data transfer process. Files are transferred as required and at the completion, the master issues a release command so that the slave is reactivated.

The hardware is partitioned into two major groups: (1) the slave kernel and (2) the I/O structure. The I/O simply consists of the serial I/O and parallel I/O controllers and associated logic. The slave kernel consists of the slave CPU, 64 Kbytes of slave memory, slave CPU address/S100 Bus address multiplexer and the logic associated in aserting the slave CPU tri-state condition.

CPU/64 Kbyte Dynamic RAM/Control

The CPS-MX is a Z80 based CPU which can be either a 4 mhz (Z80A) or 6 mhz (Z80B) CPU. 64 Kbytes of memory is implemented in such a manner that it is accessed by either the slave CPU or by the master CPU via the S100 Bus address and control lines. Control logic is provided to issue a service request flag, switch memory control from the slave to the master and back, refresh the slave memory appropriately, switch the address lines from the slave to the S100 Bus and back and provide RAS/CAS control to the memory.

64 Kbytes RAM

The RAM consists of eight 64 Kbyte by one bit memory chips with auto refresh "pin 1" compatibility. The RAM is of 150ns access variety to provide reliable, non-wait state memory operation. It is cofigured for early-write mode to simplify internal buffering requirements. Address signals are sourced from either the slave CPU or the master CPU via the S100 Bus address lines. Data signals are transmitted in the slave's internal data bus or to/from the host processor via buffers connected to the S100 Data Bus lines.

CPU/S100 Address Multiplexer

Four Octal buffers are provided to switch address lines A0 through A15 to the slave memory from either the slave CPU or the master CPU via the S100 Bus address lines. Switching action is provided by the slave's CPU DMA acknowledge output line 'BUSAK'. When the slave CPU is successfully tri-stated, BUSAK is active and in turn, enables the S100 Bus address lines to the slave's address multiplexer.

Address Multiplexer

The slaves address multiplexer consists of two Octal buffers which multiplex address lines A0 through A15 to eight address lines which are input to 64 Kbyte memory address lines via 33 ohm series resistors. The series resistors limit voltage undershoot to less than 1.0 vdc to provide long term protection to the RAM chips.

RAS/CAS Generator

The slave's memory row address and column address strobe signals (RAS and CAS respectively) are generated by the slave CPU memory read or write cycle or by the master CPU memory read or write cycle. These signals are input to a delay line to generate precise timing signals (RAS and CAS) as required by the RAM devices. The delay line also generates a signal to switch the address multiplexer described in the previous paragraph. This section of logic also generates the write timing signal sourced by the slave CPU memory write line or the master CPU memory write line via the S100 Bus. RAS, CAS and write signals are input to the RAM via series 33 ohm resistors to provide long term damage protection to the RAM. The master CPU memory cycles are enabled by the Extended Address select logic described below.

Refresh Generator/Control

Logic is provided to generate refresh to the slave memory. Either the master or the slave generates the refresh signal appropriately. The logic is structured to generate refresh properly during the switching action from slave CPU control to master CPU control and back. Extended refresh conditions are asserted in two cases. One is during S100 Bus extended wait states and the other is during slave hard requests which have not been acKnowledged by the host processor. If the slave has entered a hard request state, the slave memory must be refreshed until the master determines that a request is present and the master acknowledges the request. This acknowledge will cause the long term refresh to go inactive and for the master to assert refresh based on its processors M1 cycles. The resultant refresh signal is input to the RAM via a series 33 ohm resistor to provide long term protection to the RAM.

Extended Address Select Logic

When the slave asserts a service request and is successfully acknowledged by the master, a comparator is enabled which compares the masters extended address lines A16(m) through A22(m) against an eight position jumper referred to as the EXTENDED ADDRESS SELECT jumper. If the master executes a memory transfer to the bus, the acknowledged slave whose comparator is enabled will cause a memory cycle to occur in the slave.

I/O Port Address Select Logic

The I/O Port Address Select Logic consists of the I/O Port Address Decoder and the Host Processor Status/Command Decoder//Logic.

I/O Port Address Decoder

The I/O Port Address Decoder consists of an eight bit comparator which compares the master's least significant address bits A0(m) through A7(m) against an eight position jumper referred to as the I/O PORT SELECT jumper. If the master executes an I/O cycles transfer to the bus, the slave whose address decoder compares, will respond to either a master's command or to the master's request for the slave's status.

Host Processor Status/Command Decoder//Logic

The master may issue one of eight commands to the slave, these commands are listed as follows:

** Clear Slave Request (00H)
The slave may issue two types of requests to the master. These are: (1) SOFTREQUEST and (2) INTERRUPT REQUEST. The master is required to acknowledge the requests which is done through an I/O command, CLEAR SLAVE REQUEST.

** Confiscate Slave's Memory (01H)
The master may asynchronously issue a memory confiscation command and cause the slave's central processor to be tri-stated. Inputs to the RAM address multiplexer are transferred from the slave to the master and the slave RAM refresh is placed in "self-refresh" mode. Further, the slave "service" status is set when the slave's central processor is successfuly tri-stated. The master must then proceed to poll the "service" status. When the "service" status is detected, the master may then proceed to issue an acknowledge command (02H), which clears the "service" status and releases the self-refresh mode. This completes the transfer of control over the slave's RAM from the slave processor to the master's processor. The master may transfer the control back to the slave by issuing a "Release Slave to Run" command (03H).

The master may maintain control indefinately thereby treating the slave as a 64Kbyte RAM appearing in the master's extended address space.

** Acknowledge Slave's Service Request (02H)
The master typically issues an acknowledge command to the slave in response to the slave's "service" status. (see "CONFISCATE SLAVE'S MEMORY" command above.)

** Release Slave to Run (03H)
The master may issue a release command to the slave following successful confiscation of the slave's memory. This command causes the RAM control to pass from the master to the slave processor. (see "CONFISCATE SLAVE'S MEMORY" command above.)

** Reset Slave (80H)
The master may reset a selected slave by issuing a RESET SLAVE command. This command causes the slave processor and other slave logic to be reset. The reset state is maintained until the master issues a "Clear Slave Request" command or the master "slave clear" line is asserted on the S100 Bus.

** Request Slave Service (40H)
A request/acknowledge handshake is implemented in the master-to-slave direction. This is done by the master issuing a Request Slave Service command. The command causes an interrupt to the slave's processor via the slave's CTC controller. The slave may then issue an acknowledge command by asserting the SOFTREQ status signal. The cycle is completed by the master issuing a "Clear Slave Request" command.

** Interrupt Slave (20H)
The master has access to a second interrupt input in the slave's interrupt structure. This interrupt is asserted by the master's issuance of the "Interrupt Slave" command.

Slave Processor Control Logic

The slave control logic consists of two subdivisions. These are: (1) the Chip Select/Command Decoder and (2) the Slave Request Logic.

** Slave Processor Chip Select/Command Decoder
This logic decodes slave commands consisting of the following control functions:

** CSSIO
CSSIO is the chip select signal for the slave processor's serial Input/Output (SIO) controller.

** CSPIO
CSPIO is the chip select signal for the slave processor's parallel Input/Output (PIO) controller.

** CSCTC
CSCTC is the chip select signal for the slave processor's counter/timer (CTC) controller.

** CSSER
CSSER is the strobe signal utilized to assert one of the following functions:
- SOFTREQUEST (I/O port address = 80H)
- HARDREQUEST (I/O port address = 40H)
- SLAVE INTERRUPT REQUEST (I/O port address = 20H)

** Slave Request Logic

- SOFTREQUEST
Softrequest is a signal asserted by the slave which may be read by the master. The slave asserts this signal when it requires service by the master but does not relinquish control to the master until the master initiates a slave memory confiscation process.

- HARDREQUEST
Hardrequest is a signal asserted by the slave processor which causes the slave processor to tri-state itself thereby suspending program execution. Note the difference between a soft and a hard request: the soft request does not cause immediate suspension of slave processor execution whereby the hard request does.

-SLAVE INTERRUPT REQUEST

The Slave Interrupt Request asserts a signal on the status part which may be polled by the master or asserts a signal via an Open collector driver which may be optionally connected to one of eight S100 Bus restored interrupt lines (VI0-VI7).

Slave Clock Generator

The Slave Clock Generator cosists of an 8 or 12 mhz oscillator, a divider and an active pull-up clock driver. An 8 mhz crystal is installed for the 4 mhz slave version and a 12 mhz crystal is installed for the 6 mhz version. A divider is used to shape the oscillator output for a 50% duty cycle. The resultant output is driven by an active pull-up which causes the clock logic to conform with the Z80 processor requirements.

Reset Generator

The slave's reset line is asserted to clear the slave's processor and internal logic. One of three reset sources cause the slave reset line to be asserted. These are:

- Master Prime
The master may issue a reset signal by asserting the I/O command "Reset Slave" (see HOST PROCESSOR STATUS/ COMMAND DECODER LOGIC section).

- Slave Clear
The master may issue a reset signal by asserting the bus reset signal "Slave Clear" (S100 Bus pin 54).

- Slave Reset
The user may issue a reset command by providing a switch closure to ground on the slave reset input. A connector input located at the top of the slave circuit board is provided (J1). The input is debounced by a one-shot.

Input/Output Structure

The I/O structure consists of two serial I/O ports with associated baud rate generator and two parallel I/O ports.

Serial I/O Port Control

The Serial I/O Port Control consists of the Serial I/O Controller and the Baud Rate Clock Generator.

Serial I/O Controller

The Serial I/O (SIO) Controller is a programmable dual channel device which provides formatting for serial data communications. The channels can handle either asynchronous (Z80 SIO) or synchronous (Z80 Dart) data transfers to/from serial peripheral devices. The SIO operates either under programmed I/O or Interrupt Control. All lines necessary to handle asynchronous, synchronous, synchronous bit oriented protocols and other serial protocols are available to the user at the interface connectors. In addition, +/- 16 volt DC and +5 volt DC power are available at these connectors.

The SIO may be interfaced to peripheral devices requiring differing protocols. This interface is tailored to the exact device requirements by use of a Personality Module. The interface is implemented through two 16-pin Ansley connectors. Refer to Appendix A for a description of the serial Personality Modules currently available.

To program the SIO, the system software issues commands to initiate the mode of operation. Seven write registers exist for that purpose. In addition, three read registers allow the programmer to read the status of each channel.

Baud Rate Clock Generator

The Baud Rate Clock Generator consists of a clock generator and a CTC Programmable Interval Timer. The CTC 2.4576 MHz is a device which, under software control, can generate variable clock periods which are a multiple of the base input clock. The device has other modes of operation; however, only the modes applicable to the CPS-MX operation will be described here.

The CTC consists of four channels, each with a signal input and all but one with a clock output. Channel 0 is tied to SIO channel A transmit and receiver clock inputs, channel 1 to SIO channel B transmit receiver clock inputs, channel 2 to interrupt 1 (master interrupt to slave) and channel 3 to interrupt 2 (master request to slave).

Channels 0 and 1 are connected to the SIO inputs via jumper options PJA and PJB. These signals are also tied to the serial interface connectors. If clock signals are originated by the interfacing devices, the jumpers are cut appropriately. The channel A jumper provides for separate transmit and receive clock inputs from the interface (connector J2) or may serve as baud rate generator outputs to the interface. This arrangement is intended to provide a clock to synchronous MODEM'S via "external" clock in accordance with the EIA RS-232C standards. The modem can then return a transmit/receive clock to the serial controller. In summary, means are provided to implement serial interfaces accommodating asynchronous, synchronous, HDLC and a great number of currently defined communications protocols.

For channels 0 and 1, the CTC generates a square wave whose period is defined by a count programmed into the respective channel's counter. The square wave will remain at a logical ZERO state for one half the count, and at logical ONE for the remaining half of the count. The counter decrements for each clock period that is received.

The CTC is programmed by the CPU specifying the mode, loading sequence and counter contents. The Baud rates that can be derived from the 2.4576 Megahertz clock are listed as follows:

Baud Rate	Theoretical Frequency (16 x clock)
50	0.8 KiloHertz
75	1.2 KiloHertz
110	1.76 KiloHertz
134.5	2.152 KiloHertz
150	2.4 KiloHertz
300	4.8 KiloHertz
600	9.6 KiloHertz
1200	19.2 KiloHertz
1800	28.8 KiloHertz
2000	32.0 KiloHertz
2400	38.4 KiloHertz
3600	57.6 KiloHertz
4800	76.8 KiloHertz
7200	115.2 KiloHertz
9600	153.6 KiloHertz
19200	307.2 KiloHertz

Parallel I/O Port Control Interface

The parallel I/O Port Control Interface consists of the Parallel I/O Controller (PIO). The Parallel I/O Controller is a programmable two-port LSI component, which interfaces peripheral devices to the Z80 microprocessor. The PIO provides data transfer to and from peripheral devices under programmed I/O or interrupt control. Handshaking data transfer control lines are provided to the interface in addition to the two eight-bit data ports. The CPU reset line and the CPU clock are also connected to this interface. The PIO is flexible and may be connected to periperal devices requiring differing protocols.

The interface is tailored to the exact device requirements by use of a "Personality Module". The Personality Module is a small external circuit board which connects to the CPS-MX to provide the hardware drivers and receivers, logic and other circuitry as required. Refer to Appendix A for a description of the parallel Personality modules currently available.

To program the PIO, the system software issues commands to initialize the mode of operation. Initialization is provided by loading the interrupt vector, mode, I/O and interrupt control registers.

S100 BUS INTERFACE

The CPS-MX S100-BUS interface consists of 71 lines. These are grouped intp sets used to transmit data, control & power.

The groups are:

Group	No. of lines
Address Bus	24
Input Data Bus	8
Output Data Bus	8
Status Bus	5
Control Input Bus	7
Vectored Interrupt Bus	8
Utility Bus	2
System Power	9

Devices connected on the bus are classified as either bus masters or bus slaves and as either permanet or temporary masters. The CPS-MX is a bus slave. It cannot take control of the bus. It can only request service by the master and once acknowledged, will be the only slave on the bus being serviced until the master releases the slave through an I/O command. File transfer to/from the slave are accomplished via memory-to-memory transfer from/to the master. Software may be configured to execute the transfers under DMA control in which case the transfer rate is approximately 571 Kbyte/second.

Each of the S-100 Bus signals utilized by the CPS-MX are described on the following pages. A summary of the S-100 Bus signals in included in Appendix B.

ADDRESS BUS

The address bus consists of 24 lines designated as A0 through A23. The address lines A0 through A15 address one of the 64 Kbytes of the slave memory whereby address lines A16 through A23 map the slave memory onto the master's address space. All address lines are sampled during master memory cycles. Address lines A0 through A7 are used by the slave during master I/O cycles to transfer I/O commands from the master and status inputs to the master.

INPUT DATA BUS

The input data bus consists of 8 lines designated as DO0 through DO7. Data inputs from the master to slave are accepted during master memory & I/O output cycles when the slave is addressed appropriately.

OUTPUT DATA BUS

The output data bus consists of 8 lines desiginated as DI0 through DI7. Data outputs from the slave to the master are accepted during master memory & I/O input cycles when the slave is addresed apprporiately.

STATUS BUS

The status bus consists of 4 master output lines which define the current master processor bus cycle. The status lines used by the slave are:

STATUS	FUNCTION
sMEMR	Master memory read cycle
sM1	Master Opcode fetch cycle
sINP	Master input cycle
sOUT	Master output cycle

**** OPERATING INSTRUCTIONS ****

Instructions are given herein to configure the CPS-MX from both the hardware and software standpoint.

Hardware Setup Instructions

The hardware is configured via jumper options and solder/trace cut areas. The solder/trace cut areas are refered to as PJX, where X is the area designator. An exception is the jumper area designated as VI0 thru VI7 where a jumper may be installed to connect to the vectored interrupt lines of the S100 Bus. The PJX and VI0-7 options are located on the "solder" side of the board. Two jumper areas are provided on the "component" side. These are implemented by header jumpers.

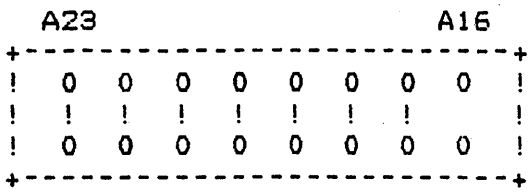
Jumper Options

Refer to figure 1 to locate the header jumper areas. These are designated as the EXT ADDR SEL and I/O PORT SEL jumpers.

EXTENDED ADDRESS SELECT (EXT ADDR SEL)

Logic is provided to map the slave's 64Kbyte memory within the master's 16 megabyte memory address space by comparing the master's extended address lines [A16 (M) through A22 (M)] against a corresponding eight position jumper. Successful comparison results in a master/slave memory transfers provided that the slave's service request was previously acknowledged by the master via a similar process for a master/slave I/O transfer. The extended address comparison jumper is designated as EXT ADDR SEL on the board's silk screen. The jumper setting designates the 64Kbyte page within the master's 16 megabyte address space that the slave's memory will reside in during the master's confiscation of the slave's memory.

EXT ADDR SEL



EXAMPLE:

To map the slave memory into the first 64Kbyte page above the master's 64Kbyte on board address space (010000H to 01FFFF), install jumpers in positions corresponding to A17 through A23 and leave A16 position open.

Note: 1. A jumper installed corresponds to a logic 0 setting and the absense of a jumper corresponds to a logic 1 setting.

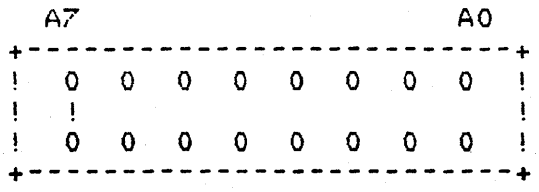
2. All slaves under the control of a common TurboDos master must be set to reside in the same 64Kbyte pages; ie: all EXT ADDR SEL jumper settings must be the same for each slave. Factory settings are provided for all slaves with EXT ADDR SEL set at 01H. TURBOdos software is configured for that setting.

3. Any other S100 Bus device installed in the bus that is memory mapped may not reside within the address space assigned to the slave(s).

I/O PORT SELECT (I/O PORT SEL)

The master transfers commands to the slaves and receives status from the slaves through I/O Bus transfers. Logic is provided to map the slave within the master's 256 byte I/O address space by comparing the master's address lines [A0 (M) through A7 (M)] against a corresponding eight position jumper. Successful comparison results in a master/slave I/O transfer. It is through I/O status and command transfers that the master determines if a slave requires service and if a slave is to be confiscated for subsequent file transfers to/from the slave's memory.

I/O PORT SEL



EXAMPLE:

To map the slave into the I/O address space 7FH, install a jumper in position A7 and none in the remaining positions.

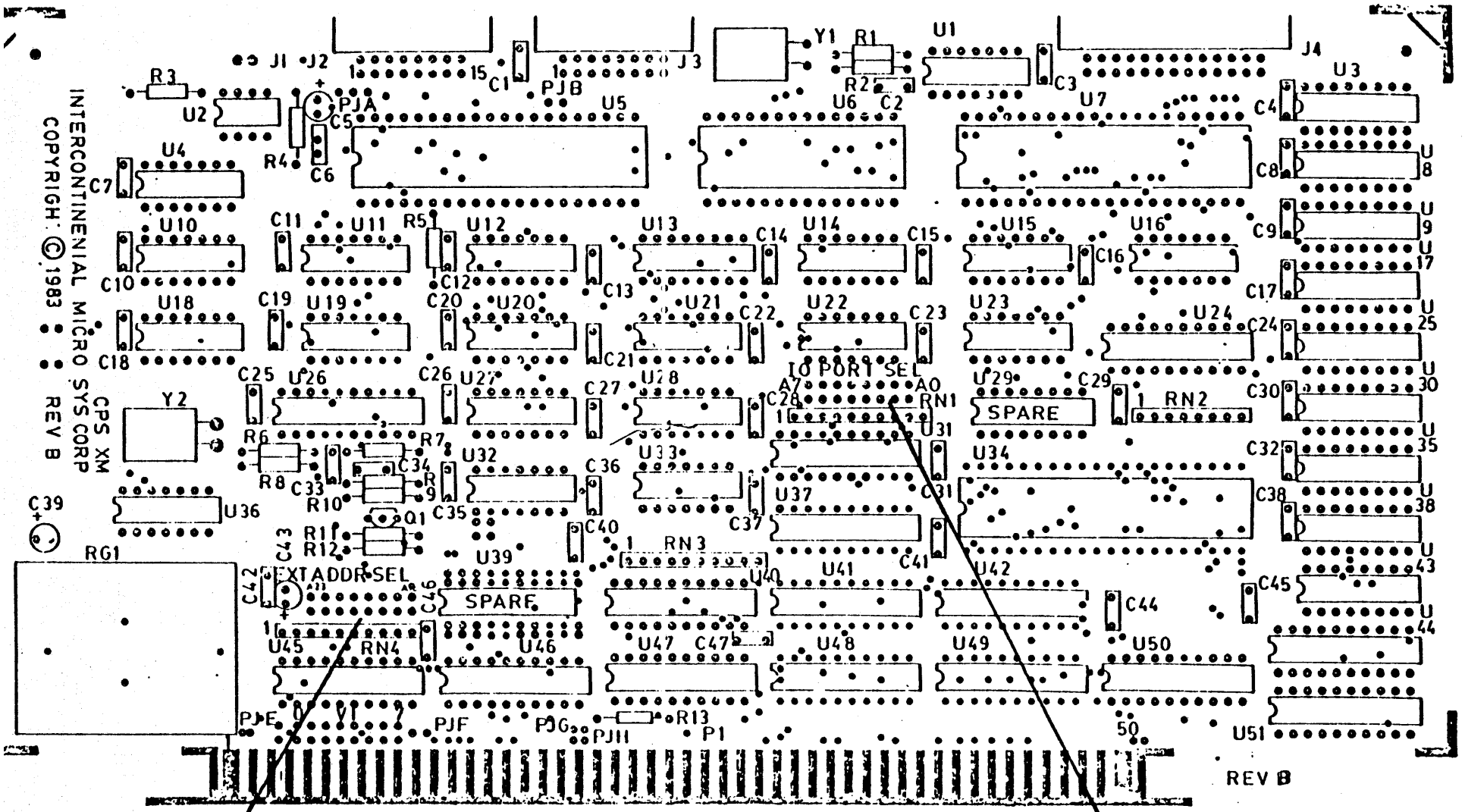
Note: 1. A jumper installed corresponds to a logic 0 setting and the absense of a jumper corresponds to a logic 1 setting.

2. Slaves under the control of a common master must be set to reside in individual I/O locations. ie: All I/O PORT SEL jumper settings are mutually exclusive. Factory setting are provided for all slaves with I/O PORT SEL set at 7fH. The customer must provide jumpers to map each slave at exclusive locations. The TURBOdos opperating system is then configured as follows:

DEFAULT I/O PORT SETTING:

Slave Number:	1	2	3	4	5	6	7	8
I/O address :	7FH	7EH	7DH	7CH	78H	7AH	79H	78H

Slave Number:	9	10	11	12	13	14	15	16
I/O address :	77H	76H	75H	74H	73H	72H	71H	70H



EXTENDED ADDRESS SELECT

FIG 1

I/O PORT SELECT

SOLDER/TRACE CUT OPTIONS

Refer to figure 2 to locate the solder/trace cut areas. These are listed as follows:

PJA - SIO Port A clock source select
PJB - SIO Port B clock source select
PJC - Master memory cycle qualified on PSYNC
PJD - Master memory cycle qualified on PSTVAL
PJE - Connect S100 Bus groung pin 53 to PCB ground plane
PJF - Pull-up SIXTN status
PJG - Connect S100 bus ground pin 20 to PCB ground plane
PJH - Connect S100 bus ground pin 70 to PCB ground plane
VIX (X=0-7) - Connect Slave interrupt request to one of eight VI lines (VI0-VI7).

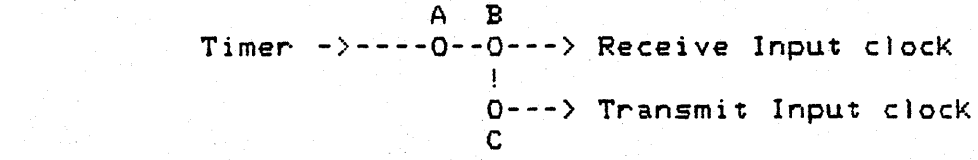
PJA

The CPZ-48000 comes configured so that the SIO ports receive their baud clocks from an on-board programmable timer. The board could be reconfigured to source the clocks from the SIO serial port connectors. Such is the case when synchronous modems connect to the serial ports. The modem provides a clock to the SIO. Furthermore, the modem may receive the clock from the on-board timer, condition the clock and return it to the input of the SIO. The transmit and receive clocks may be sourced separately on Port A. All combinations are possible through this jumper.

To source SIO PORT A inputs from the SIO connector only, cut the trace from PJA 'a' to PJA 'b'. The source can now be connected through the personality board on either PIN P2-2 or P2-3.

If the SIO PORT A inputs are to be sourced separately from the SIO connector, cut the trace from PJA b to PJA c. The receive clock is now input on P2-3 and the transmit clock is input on P2-2.

[PJA] area

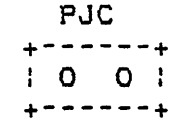


PJB

To source SIO Port B input from the SIO connector only, cut the trace at PJB. The source can now be connected through the personality board on pin P3-3.

PJC

When the host processor confiscates the slave's memory, the host processor generates memory read cycles based on the host's memory read status signal sMEMR. Option are provided to qualify the read cycle generation with pSYNC or pSTVAL or both. With the CPZ-48000 SBCP used as the host, neither pSYNC nor sSTVAL are used. PJC & PJD provide compatibility with IEEE timing signals requirements by connecting both jumper.

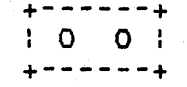


To qualify the memory read cycle with pSYNC, connect PJC.

PJD

See PJC jumper description above.

PJC

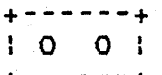


To qualify the memory read cycle with pSTVAL, connect PJD.

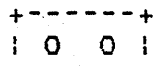
PJE	PJG	PJH

Some S100 bus boards utilize pin 20, 53 and 70 for signals other than ground. The IEEE specification requires that these be connected to ground. If a board is installed in the bus and any of these pins are used for other than ground, the corresponding jumper areas must be left open. If not used and and more ground connection is desired, solder a jumper in the respective area.

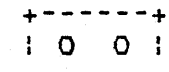
PJE



PJG



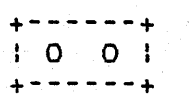
PJH



PJF

The CPS-MX is compatible with IEEE 16 data bit processors such as 8086 based Cpu's; however the CPS-MX transfers 8 bit data only. In accordance with the IEEE 696.1/D2 specification, SIXTN is interrogated by the host to determin if the data bus transfer consists of 16 or 8 data bits. If SIXTN* is found to be at a logic high, the host transfers 8 data bits. The CPS-MX must be strapped to present a logic high on the SIXTN line. This is accomplished by providing a strap on PJF.

PJF



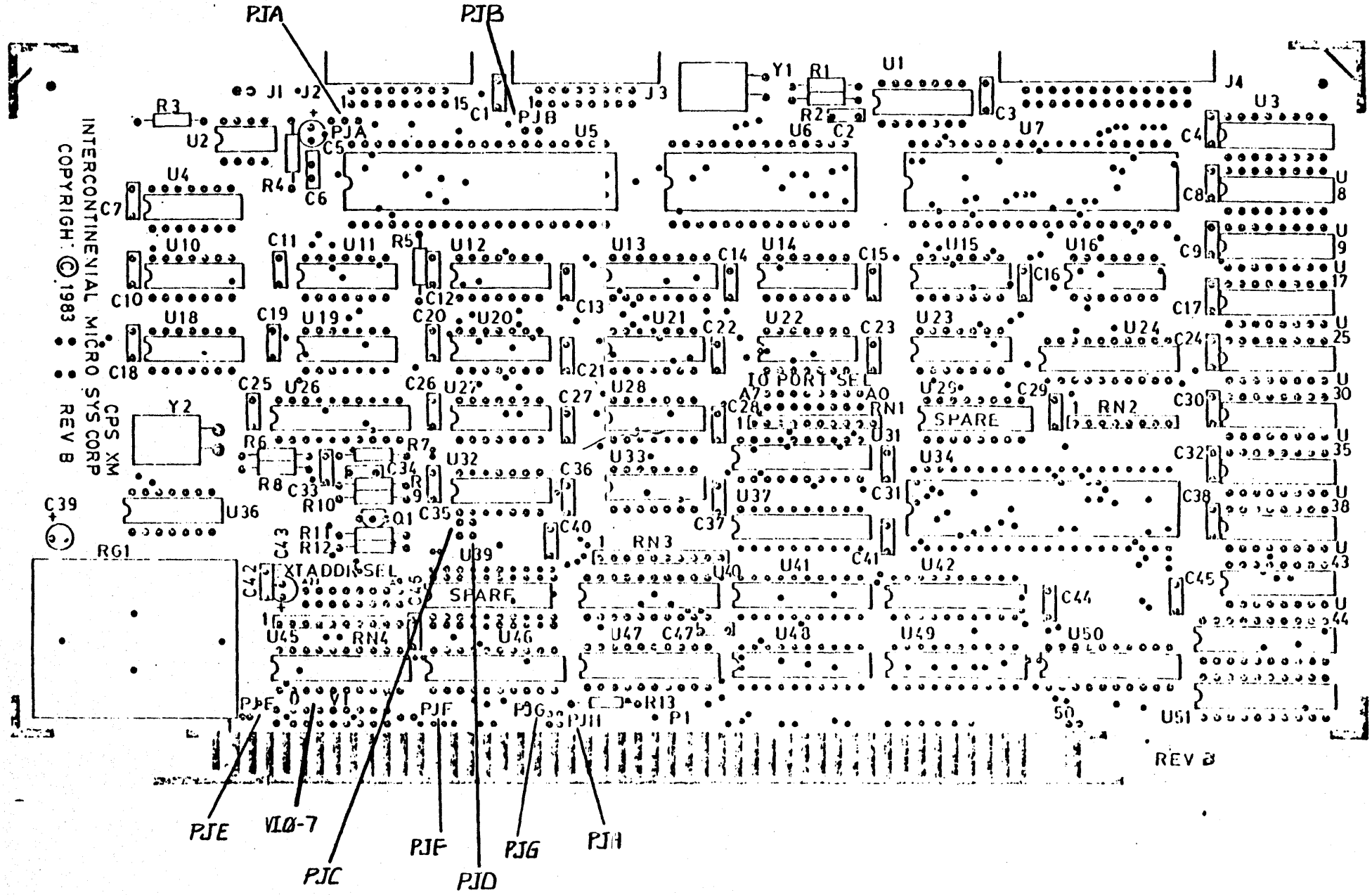
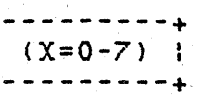
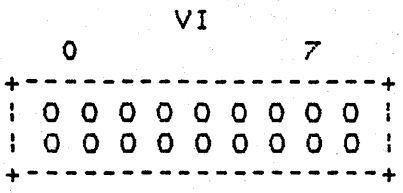

PJA
PJB
PJE
VI0-7
PJC
PJF
PJD
PJG
PJH
INTERCONTINENTIAL MICRO SYS CORP
COPYRIGHT © 1983
CPS XM
REV B
REV B
IO PORT SEL
SPARE
SHARE
XTADDR SEL

FIG 2



The CPS-MX may assert an interrupt to the host (Slave Interrupt Request). The interrupt may be connected to one of 8 VI lines of the S100 bus. This is accomplished by connecting a strap on the VI jumper area. TURBOdos does not utilize the feature.



PERSONALITY BOARD INTERCONNECTION INSTRUCTIONS

The CPS-MX has four connections at the top of the board numbered J1 through J4. These are listed below:

J1 - Slave reset connector
J2 - SIO Port A Connector
J3 - SIO Port B Connector
J4 - PIO Connector

J2,J3 & J4 are typically connected to peripheral devices through personality boards which are small printed circuit boards customizing the above listed devices to a variety of peripherals. The slave may be reset by providing a switch closure across J1. J1 may be left open without adverse effect or this input is pulled-up.

Most S-100 Bus chassis provide a jumper plate at the rear of the chassis to which peripheral connectors are installed. Typically, the connectors are of the ITT CANNON DB25 type. The personality boards provided by ICM are boards with DB25 connectors at one end and header plug at the other. The DB25 connector end is to be installed in the cutouts provided on the connector plate. Flat ribbon cable then connects the CPS-MX connector to the personality board.

At a minimum, SIO Port B (RPB100) personality board must be installed. The instructions follow:

1. - Select a DB25 connector cutout at the rear of the chassis for the RBP100 personality board.
2. - Insert and hold the RPB100 personality board in the cutout.
3. - Install #6 nuts, washers and bolts passing the bolts through the personality board's DB25 connector.
4. - Install the flat ribbon cable provided At the personality board and at the CPS-MX, connector J3.
5. - Install a cable from the chassis connector to the peripheral.