PERKIN-ELMER

M 48-080

NEW ULI

UNIVERSAL LOGIC INTERFACE (ULI)

Installation, Theory of Operation
and Programming Manual

47-056 R00

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

The Perkin-Elmer Corporation, Data Systems Group, 2 Crescent Place, Oceanport, New Jersey 07757

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PREFACE

The 35-860 universal logic interface (ULI) is an interface device designed to provide a convenient byte or halfword interface for the Perkin-Elmer Multiplexor (MUX) Bus. The ULI can be either a stand-alone interface with long distance data transmission capabilities or an interface for a custom-built user device controller, which can be located in one of the on-board wire wrap fields.

This manual provides the technician with the information necessary to install, maintain and program the ULI.

Chapter 1 contains a general description of the ULI. Chapter 2 provides a detailed description of the ULI installation and configuration. Chapter 3 describes ULI operation. Chapter 4 describes ULI equipment preparations for self-test. Chapter 5 provides the programming considerations.

For information on the contents of all Perkin-Elmer 32-bit manuals, see the 32-Bit Systems User Documentation Summary.

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The 35-860 universal logic interface (ULI) board provides the customer with the means to interface peripheral equipment to a Perkin-Elmer system. This is accomplished in one of two ways: by connecting compatible user device controllers directly to the ULI to interface user peripheral equipment, or by constructing compatible user device controllers in the two on-board wire-wrap fields to interface user peripheral equipment to the ULI.

The ULI board can be configured in the system as shown in Figure 1-1 and described as follows:

- As a direct interface to the multiplexor bus (MUX bus)
- Under a subchannel controller (SCC), which provides increased fanout capabilities for the MUX bus
- Under a selector channel (SELCH), which generates a private input/output (I/O) bus that is an extension of the MUX bus when the SELCH is idle
- Under an I/O switch, which provides the capability of sharing I/O devices between two or more processors and/or an I/O bus extension up to 50 feet

The MUX bus or SELCH I/O bus is a byte- or halfword-oriented I/O system that communicates with as many as 1,023 peripheral devices. In a typical case, a user device controller receives a 10-bit address, an 8-bit command byte and either an 8-bit data byte or a 16-bit data halfword from the processor over the 16 data lines. A user device controller sends a 10-bit address, an 8-bit status byte and either an 8-bit data byte over the least significant eight data lines (080:150) or a 16-bit data halfword over the 16 data lines (000:150) to the processor.

This chapter describes the board architecture and its interfaces to the system.

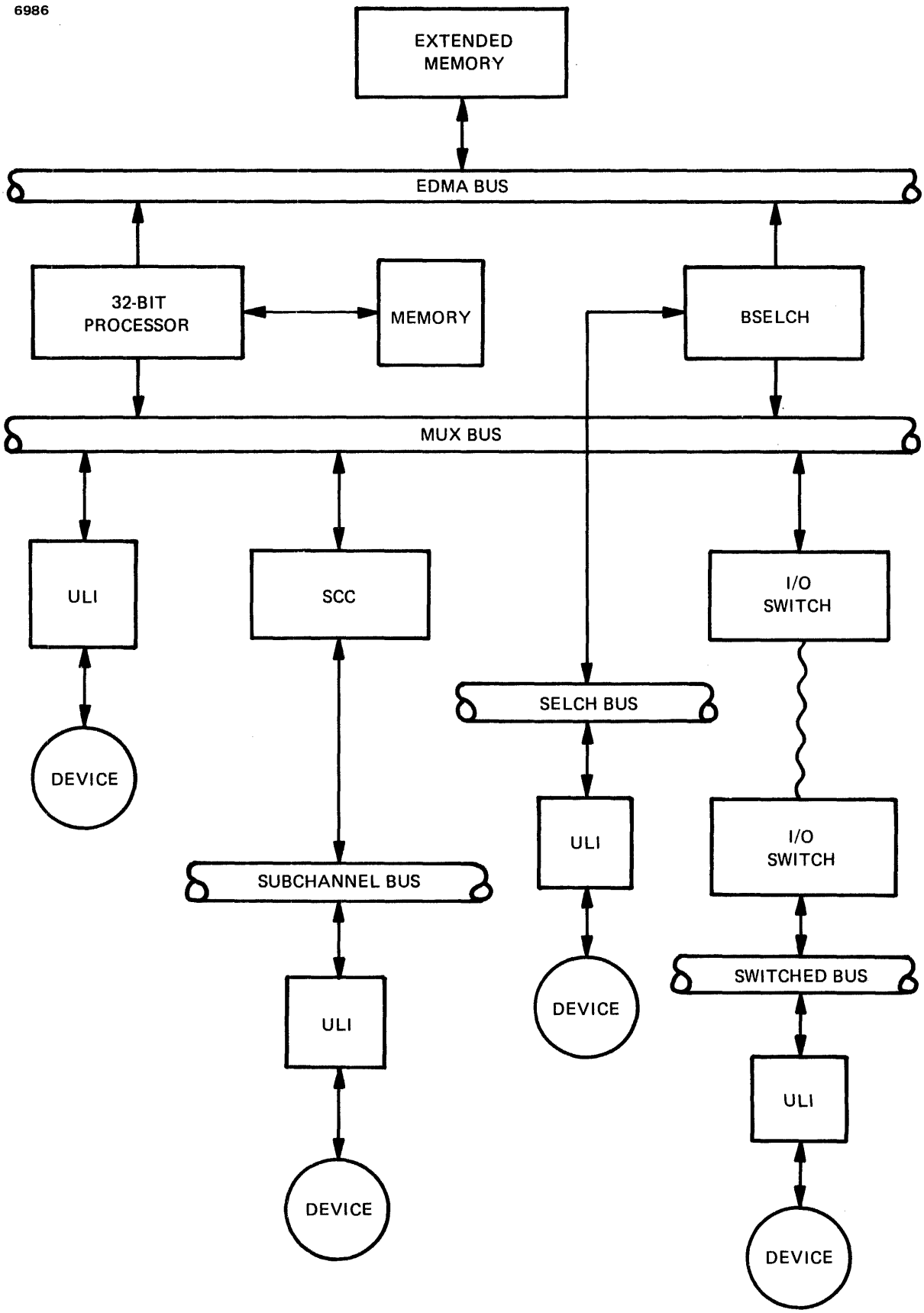

Figure 1-1 ULI/System Configuration

1.2 ARCHITECTURE

The ULI is configured on one 37.5 cm (15") board that is divided into two halfboard sections. Each section provides two ways to interface user device controllers to the ULI. One section contains general-purpose interface logic components that operate under request/response I/O control for data transfer in the byte or halfword (two bytes) mode. This enables users having device controllers compatible with the ULI I/O request/response signals to interface directly to the system. This section also contains a small wire-wrap field that allows the user to construct a device controller and connect it between an on-board connector, containing the ULI I/O request/response signals, and an off-board connector on the component side or the wire-wrap side, as required. The remaining section contains a halfboard wire-wrap field for the construction of device controllers that are too large to be constructed in the wire-wrap field located on the component side. The device controllers built on this section are also connected between the on-board connector and an off-board connector on the component side or the wire-wrap side, as required. The on-board connector can be directly strapped to the off-board connector on the wire-wrap side to make the 35-860 ULI board compatible with an M48-013 ULI board. All sections are connected in parallel to form the data link between the user's peripheral equipment and a Perkin-Elmer system.

When only the component side of the ULI is used, the board can be physically cut in half to produce halfboards. This provides the user with the option of strapping the ULI halfboard to an active halfboard, depending upon the system configuration. See Figure 1-2.

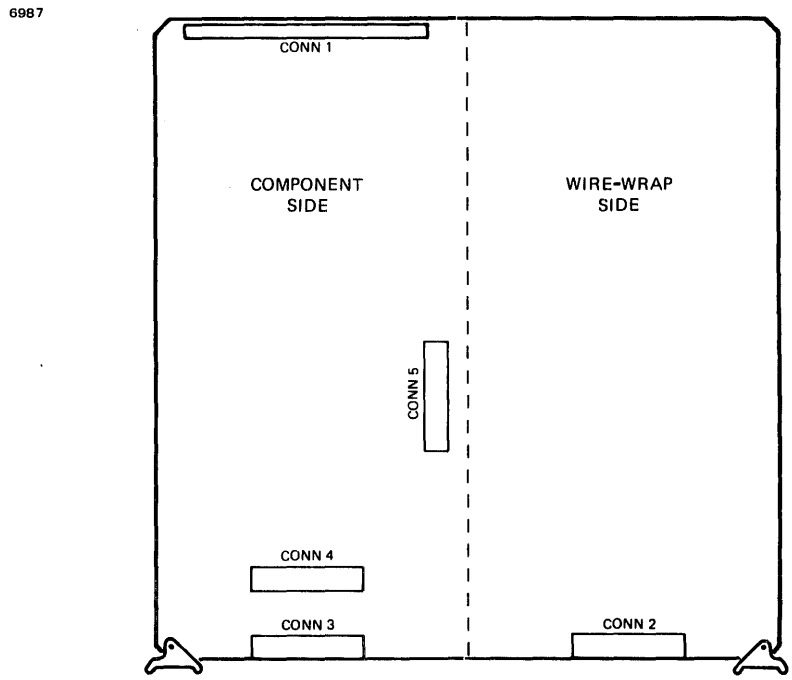

Figure 1-2 ULI Board Assembly

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

This chapter describes the unpacking procedure, power requirements, board assembly, slot location, backpanel priority wiring, cabling, connections, signal definitions and strapping information necessary for the installation of the universal logic interface (ULI) board. Also included are the wire-wrap field layout, addressing and compatibility with the M48-013 ULI board.

2.2 UNPACKING PROCEDURE

When the ULI is shipped with a system, it is installed at the factory so there is no special unpacking procedure. If the module is purchased separately, it should be inspected for damage prior to installation.

2.3 POWER REQUIREMENTS

The ULI board requires 5 VDC @ 2A.

2.4 LOCATION

The 37.5 cm (15") fullboard assembly or the ULI 17.5 cm (7") halfboard assembly and an active 17.5 cm (7") halfboard can be installed in any available input/output (I/O) slot of a standard 37.5 cm (15") chassis.

2.5 17.5 CM (7") HALFBOARD UNIVERSAL LOGIC INTERFACE (ULI)

When there is no requirement for the wire-wrap halfboard, the 37.5 cm (15") board can be cut to produce two 17.5 cm (7") halfboards. The 17.5 cm (7") ULI board is attached to an active halfboard by a 16-398 halfboard adapter kit. This generates a 37.5 cm (15") board, allowing the 17.5 cm (7") ULI board to be installed into a slot in a standard 37.5 cm (15") chassis. There is no wiring between the 17.5 cm (7") ULI board and the adapter or the active halfboard. See Figure 2-1.

2.6 BACKPANEL WIRING

To include the ULI in the receive acknowledge/transmit acknowledge (RACK0/TACK0) priority daisy chain, remove the RACK0/TACK0 strap between terminals 122 and 222 on the connector 1 (CONN 1) side of the slot occupied by the ULI. See Figure 2-2.

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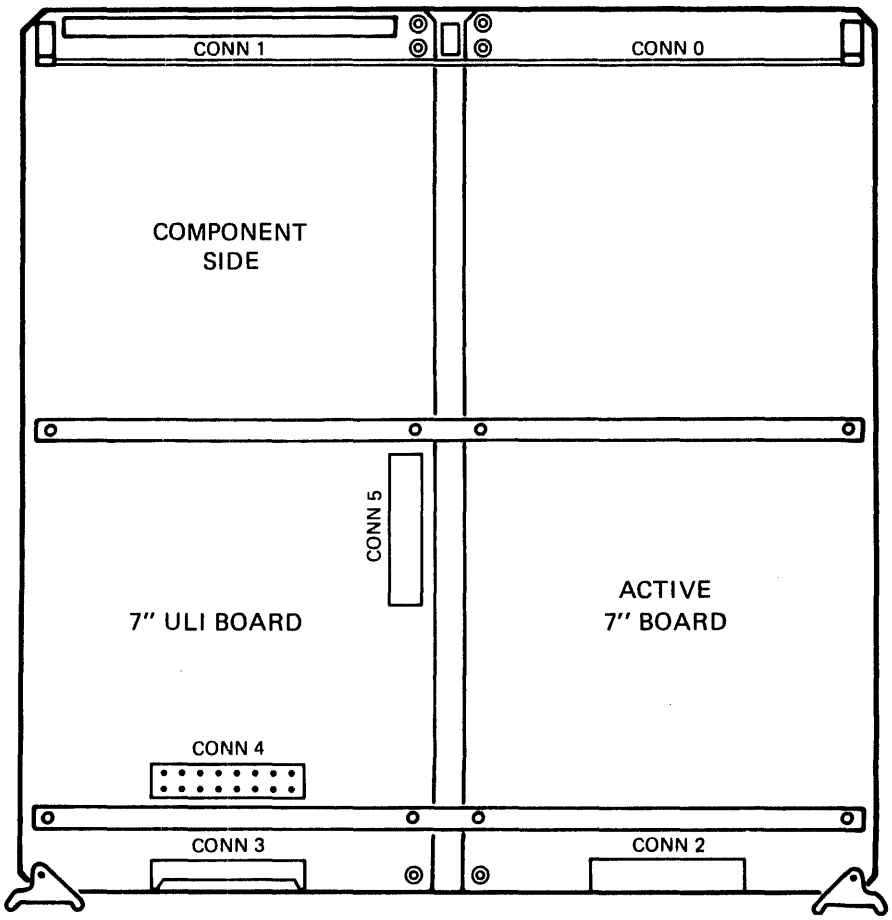

NOTE: 7" (17.5 cm) ULI BOARD CAN BE LOCATED ON EITHER SIDE.

Figure 2-1 17.5 cm (7") Halfboard Assembly

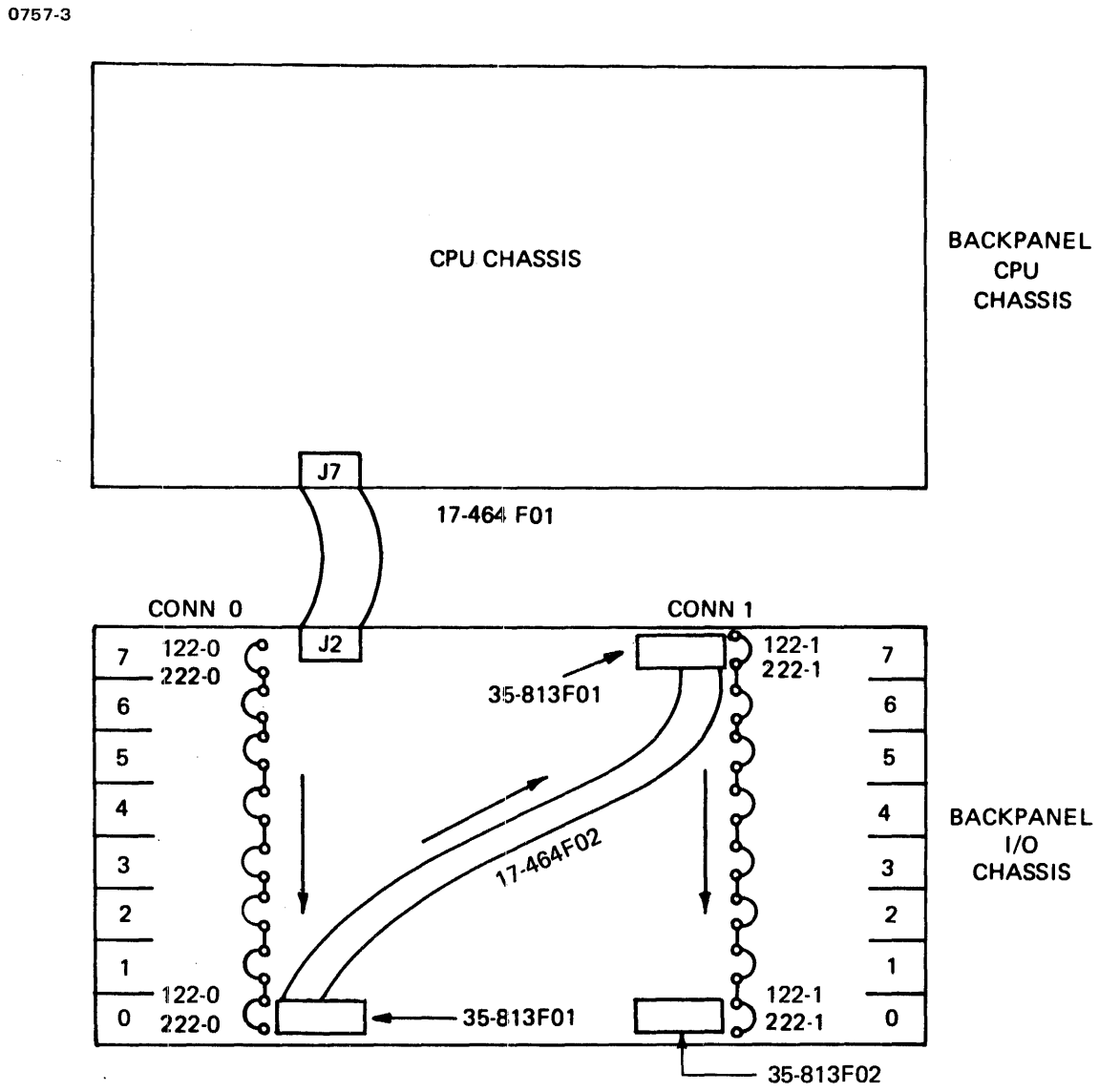

Figure 2-2 Chassis Backpanel

2.7 UNIVERSAL LOGIC INTERFACE (ULI)/WIRE-WRAP FIELD CONNECTIONS AND SIGNALS

The following sections describe the connections and signals of the ULI/wire-wrap fields' cables.

To understand Perkin-Elmer functional schematics, it must be noted that the last character in the mnemonic symbol designates the logic level when the signal is active. For example, DAT080 is data line number 8 and the last character 0 means that when DAT080 is active, the line is at a logic level zero (0).

Connector pin numbers are identified by a 4-digit number in the format:

rpp-c

Where:

r	is the row number.
pp	is the 2-digit pin number.
c	is the connector number.

2.7.1 Universal Logic Interface (ULI) Cables, Connectors and Signals for Compatible Device Controllers

The following sections describe the interconnecting cables, connectors and signal definitions for compatible device controller interfaces.

2.7.1.1 Universal Logic Interface (ULI) Cables

The two 50-pin connectors, CONN 3 and CONN 4, provide the ULI I/O request/response signals to compatible user device controllers. Two 17-651 cables are connected between CONN 3 and CONN 4 and the convenience panel, as shown in Figure 2-3. When the ULI is under test, the 17-650 test cable loops CONN 5 while running the tests and diagnostics. Figure 2-4 shows the pin map for CONN 2 and cable 17-185 connectors at the convenience panel when the ULI is used in the M48-013 compatibility mode.

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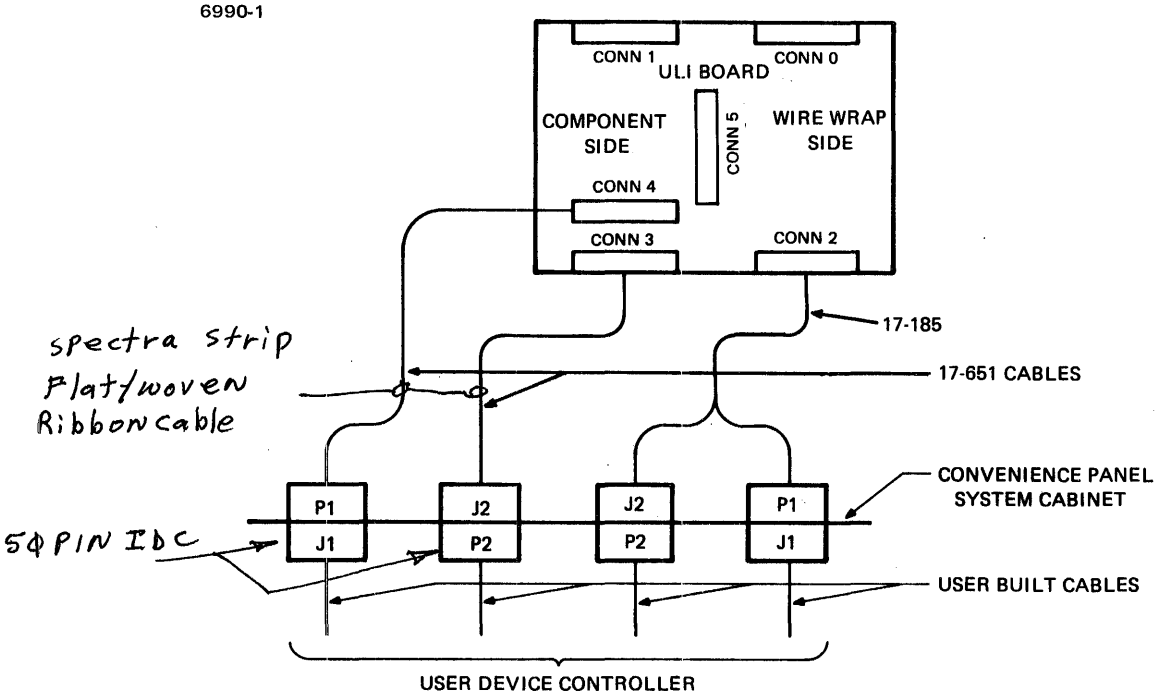

Figure 2-3 Cable Connections

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PIN MAP		
CONNECTOR 2		
ROW 1	ROW 2	PIN NO.
GND	GND	00
SIN060	SIN070	01
SIN040	SIN050	02
SIN020	SIN030	03
SIN000	SIN010	04
DIN140	DIN150	05
DIN120	DIN130	06
DIN100	DIN110	07
DIN080	DIN090	08
DIN060	DIN070	09
DIN040	DIN050	10
DIN020	DIN030	11
DIN000	DIN010	12
SATN0	SCLR0B	13
COT070	COT060	14
COT050	COT040	15
DOT150	DOT140	16
DOT130	DOT120	17
DOT110	DOT100	18
DOT090	DOT080	19
DOT070	DOT060	20
DOT050	DOT040	21
DOT030	DOT020	22
DOT010	DOT000	23
GND	GND	24

CONN 2		CONN 5
SIN	=	STATW
DIN	=	DMUXW
DOT	=	DATW
COT	=	COMW

PIN MAP		
CABLE CONNECTORS		
J2	P1	PIN NO.
DIN000	GND	01
INT0	GND	02
SCLR0B	SIN070	03
COT070	SIN060	04
COT060	SIN050	05
COT050	SIN040	06
COT040	SIN030	07
DOT150	SIN020	08
DOT140	SIN010	09
DOT130	SIN000	10
DOT120	DIN150	11
DOT110	DIN140	12
DOT100	DIN130	13
DOT090	DIN120	14
DOT080	DIN110	15
DOT070	DIN100	16
DOT060	DIN090	17
DOT050	DIN080	18
DOT040	DIN070	19
DOT030	DIN060	20
DOT020	DIN050	21
DOT010	DIN040	22
DOT000	DIN030	23
GND	DIN020	24
GND	DIN010	25

Figure 2-4 Connector 2 and 17-185 Cable Pin Map Locations

2.7.1.2 Universal Logic Interface (ULI) Connectors

Front edge connectors 3 and 4 are shown in Table 2-1 and in Figures 2-5 and 2-6.

TABLE 2-1 PIN MAP FOR CONNECTORS 3 AND 4

CONNECTOR 3			CONNECTOR 4		
ROW 1	ROW 2	PIN NO.	ROW 1	ROW 2	PIN NO.
DMUXP150	DMUXN150	00	DATP150	DATN150	00
DMUXP140	DMUXN140	01	DATP140	DATN140	01
DMUXP130	DMUXN130	02	DATP130	DATN130	02
DMUXP120	DMUXN120	03	DATP120	DATN120	03
DMUXP110	DMUXN110	04	DATP110	DATN110	04
DMUXP100	DMUXN100	05	DATP100	DATN100	05
DMUXP090	DMUXN090	06	DATP090	DATN090	06
DMUXP080	DMUXN080	07	DATP080	DATN080	07
DMUXP070	DMUXN070	08	DATP070	DATN070	08
DMUXP060	DMUXN060	09	DATP060	DATN060	09
DMUXP050	DMUXN050	10	DATP050	DATN050	10
DMUXP040	DMUXN040	11	DATP040	DATN040	11
DMUXP030	DMUXN030	12	DATP030	DATN030	12
DMUXP020	DMUXN020	13	DATP020	DATN020	13
DMUXP010	DMUXN010	14	DATP010	DATN010	14
DMUXP000	DMUXN000	15	DATP000	DATN000	15
COMP150	COMN150	16	STATP150	STATN150	16
COMP140	COMN140	17	STATP140	STATN140	17
COMP130	COMN130	18	STATP130	STATN130	18
COMP120	COMN120	19	STATP120	STATN120	19
GND	NPBUSY0	20	STATP110	STATN110	20
DRE0	DAE0	21	STATP100	STATN100	21
SRE0	CMDE0	22	STATP090	STATN090	22
SCLRE0	RSTANT0	23	STATP080	STATN080	23
SATN0	GND	24	GND	GND	24

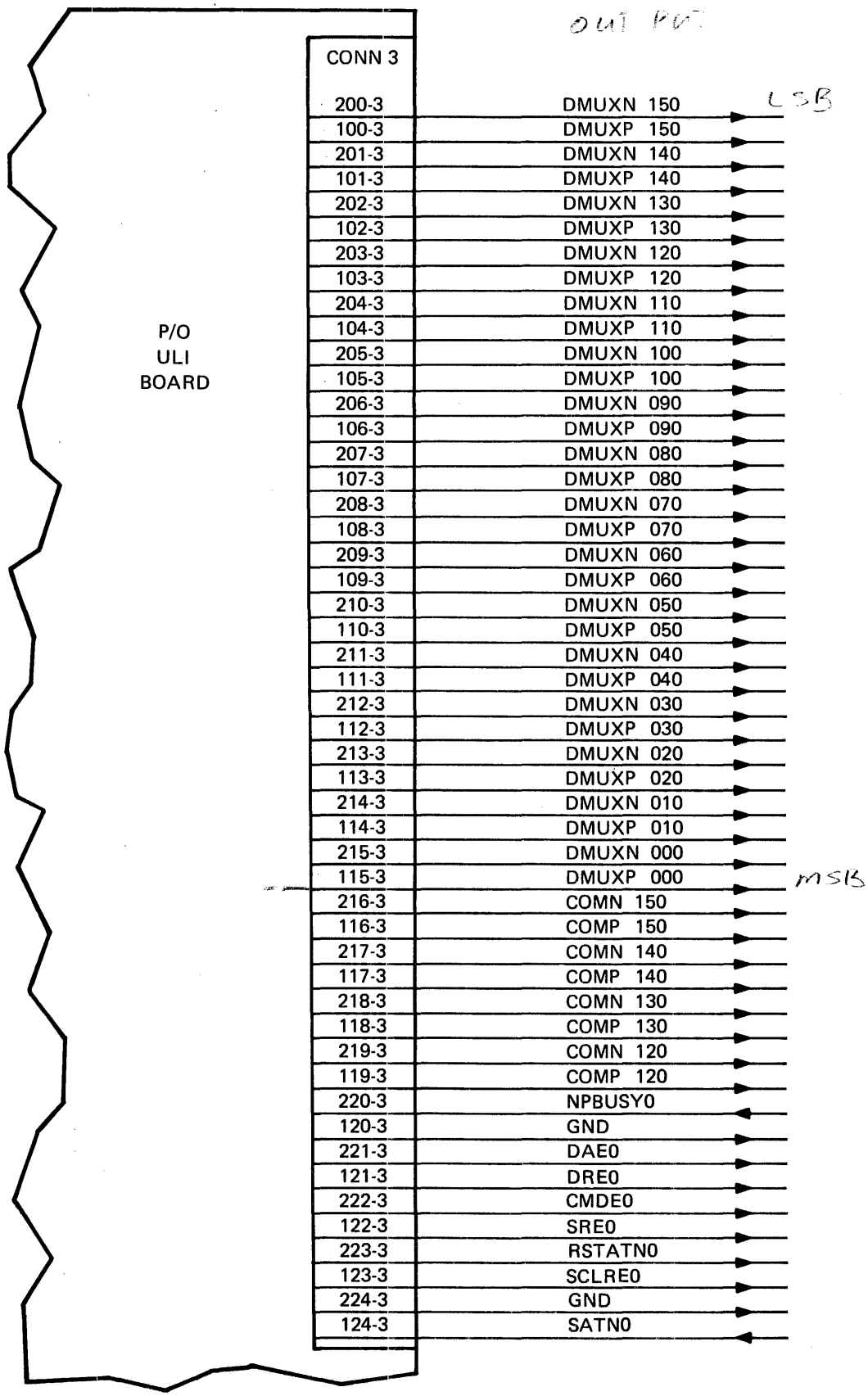

Figure 2-5 Connector 3

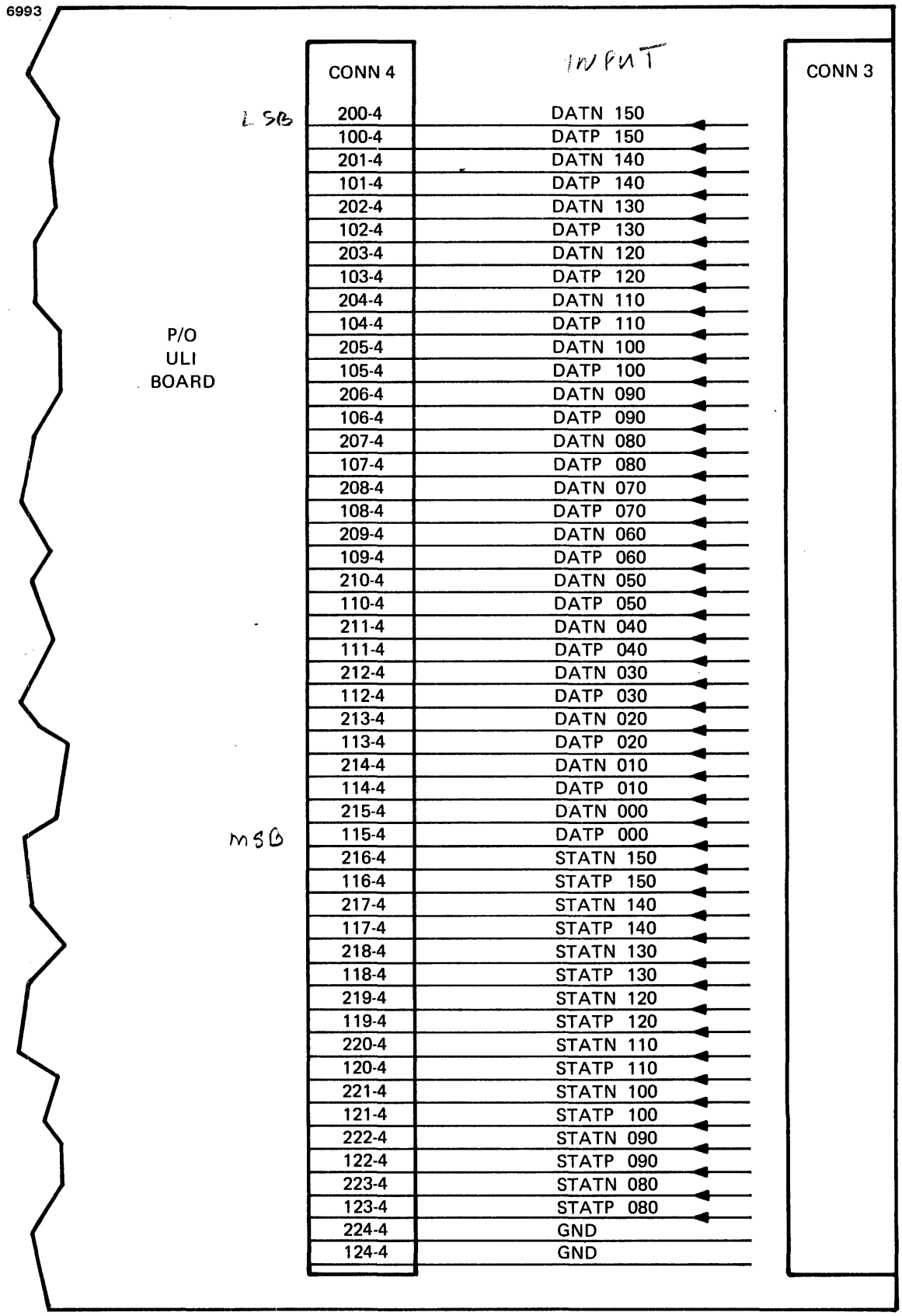

Figure 2-6 Connector 4

2.7.1.3 Universal Logic Interface (ULI) Signal Definitions

The ULI I/O signals at off-board connectors 3 and 4 are given in Table 2-2.

TABLE 2-2 ULI SIGNAL DEFINITIONS

SIGNAL LINES	ULI ⟷ USER
Data lines:	
* DMUX(N/P)000:150	→
* DAT(N/P)000:150	←
Status lines:	
* STAT(N/P)080:150	←
Command lines:	
* COM(N/P)120:150	→
Control lines:	
Status request (SRE0)	→
Command (CMDE0)	→
Data available (DAE0)	→
Data request (DRE0)	→
System clear (SCLRE0)	→
Reset attention (RSTATN0)	→
High speed SELCH protocol busy (NPBUSY)	←
Set attention (SATN0)	←

* N=negative
P=positive lines

2.7.2 Wire-Wrap Field Interconnectors, Signals and Layouts for Custom-Built Device Controllers

The following sections describe the wire-wrap field interconnectors, signal definitions and layout for custom-built device controller interfaces.

2.7.2.1 Custom-Built User Device Controller Connections

Any custom-built user device controller, on either section of the ULI board, is connected between the ULI and user peripheral equipment as described in the following paragraph.

The user device controller is wired to on-board CONN 5 for interface to the ULI, and connected to the wire-wrap stakes of CONN 4 or connector 2 (CONN 2) for off-board user peripheral equipment connection. See Figures 2-7 and 2-8 and Table 2-3.

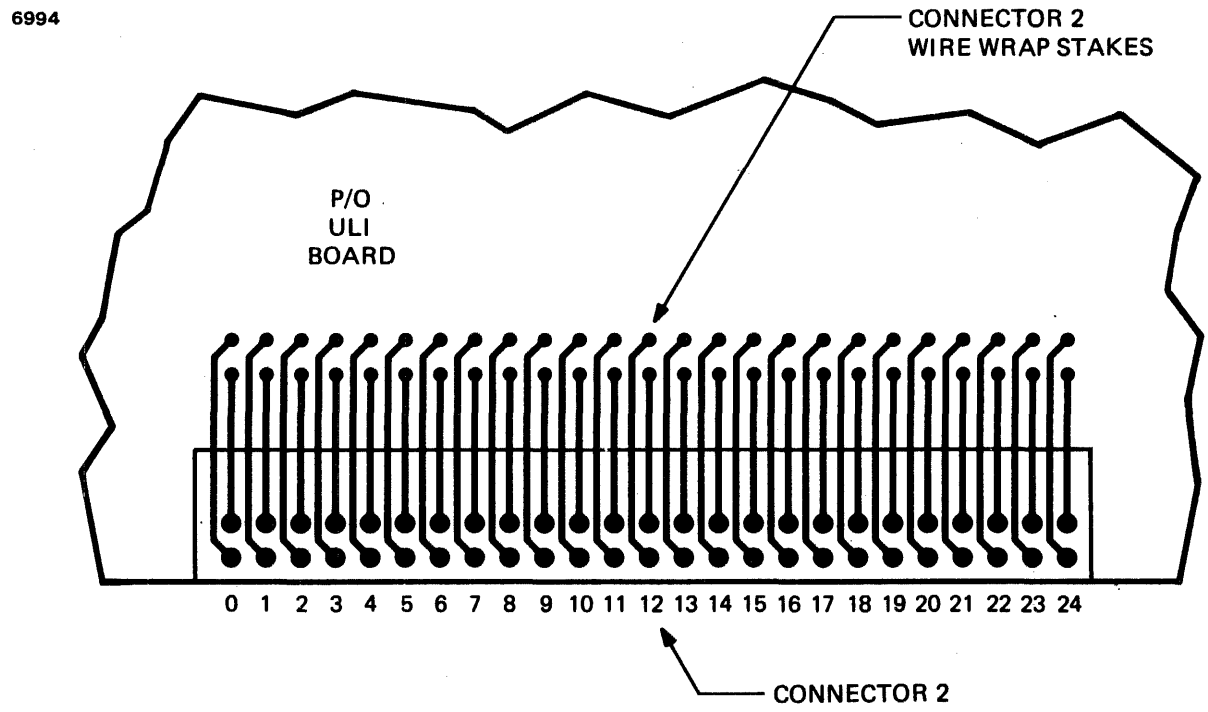

Figure 2-7 Connector 2 Wire-Wrap Stakes

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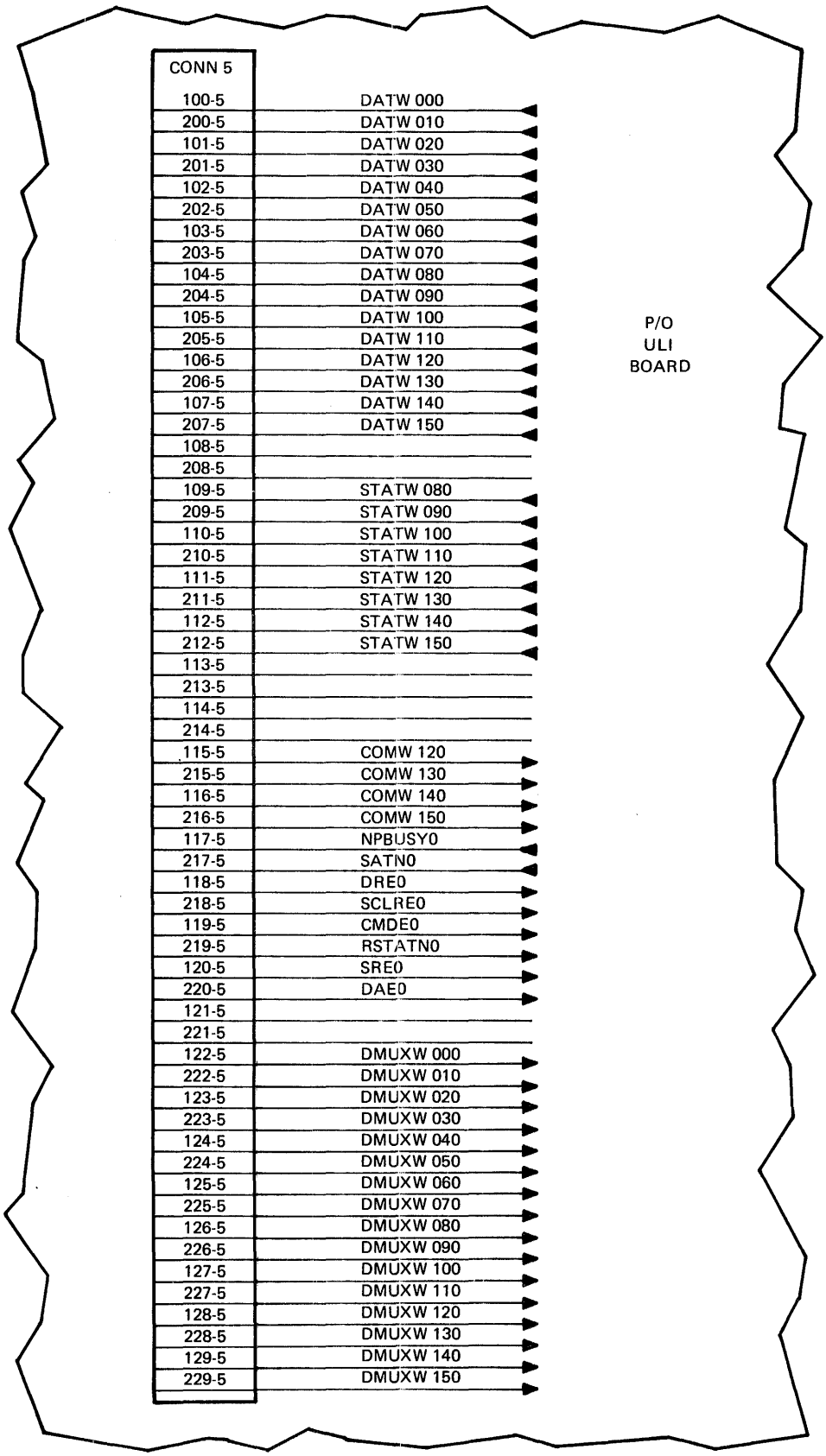


Figure 2-8 Connector 5

TABLE 2-3 PIN MAP FOR CONNECTORS 2 AND 5

CONNECTOR 2			CONNECTOR 5		
ROW 1	ROW 2	PIN NO.	ROW 1	ROW 2	PIN NO.
		24	DMUXW140	DMUXW150	29
		23	DMUXW120	DMUXW130	28
		22	DMUXW100	DMUXW110	27
		21	DMUXW080	DMUXW090	26
		20	DMUXW060	DMUXW070	25
		19	DMUXW040	DMUXW050	24
		18	DMUXW020	DMUXW030	23
		17	DMUXW000	DMUXW010	22
		16			21
		15	SRE0	DAE0	20
		14	CMDE0	RSTATN0	19
		13	DRE0	SCLRE0	18
		12	NPBUSY0	SATN0	17
		11	COMW140	COMW150	16
		10	COMW120	COMW130	15
		09			14
		08			13
		07	STATW140	STATW150	12
		06	STATW120	STATW130	11
		05	STATW100	STATW110	10
		04	STATW080	STATW090	09
		03			08
		02	DATW140	DATW150	07
		01	DATW120	DATW130	06
		00	DATW100	DATW110	05
			DATW080	DATW090	04
			DATW060	DATW070	03
			DATW040	DATW050	02
			DATW020	DATW030	01
			DATW000	DATW010	00

2.7.2.2 Wire-Wrap Signal Definitions (CONN 5)

The ULI I/O signals at on-board CONN 5 are given in Table 2-4.

TABLE 2-4 WIRE-WRAP SIGNAL DEFINITIONS

SIGNAL LINES	ULI ⇄ USER WIRE-WRAP FIELD
Data lines:	
* DMUXW000:150	→
* DATW000:150	←
Status lines:	
* STATW080:150	←
Command lines:	
* COMW120:150	→
Control lines:	
Status request extension (SREO)	→
Command extension (CMDEO)	→
Data available extension (DAEO)	→
Data request extension (DREO)	→
System clear extension (SCLREO)	→
Reset attention (RSTATNO)	→
High-speed selector channel (SELCH) protocol busy (NPBUSYO)	←
Set attention (SATNO)	←

* W indicates wire-wrap signals at CONN 5

2.7.2.3 Wire-Wrap Field Layout

The component side of the ULI contains a small universal wire-wrap field. This field can accommodate any size integrated circuit (IC) up to 48 pins or discrete components (resistors, capacitors and diodes) to build a user device controller to interface to the system. The wire-wrap field layout for the component side of the ULI is shown in Assembly Drawing 35-860 and Figure 2-9.

The wire-wrap side of the ULI board is a general-purpose wire-wrap component section. This section contains 91 positions for ICs with eight pins or less, and 12 positions for 20- to 28-pin ICs. Each position can contain one IC module or up to eight axial lead discrete components (resistors, capacitors and diodes) to build a user device controller to interface to the system. The wire-wrap field layout for the wire-wrap side of the ULI is shown in Assembly Drawing 35-860 and Figure 2-10.

The wire-wrap stakes of CONN 2 enable the 35-860 ULI to be compatible with the M48-013 ULI by wiring to CONN 5.

NOTE

When the ULI functions with a custom-built user device controller in either field, the status and data receivers on CONN 4 must be disconnected, as shown in Functional Schematic 35-860 at location 7J9.

2.8 STRAP OPTIONS

The following sections describe high-speed SELCH protocol, command bit 10, line receivers and addressing. See Figures 2-11, 2-12, 2-13 and Functional Schematic 35-860D08.

2.8.1 High-Speed Selector Channel (SELCH) Protocol

The ULI operates in two protocols: standard and high-speed SELCH. The ULI is shipped in the standard protocol, no strap between E1-1 and E1-2 (2G9). If the ULI is installed with a high-speed SELCH, connect a strap between E1-1 and E1-2 (2G9) to enable the high-speed SELCH protocol signal to check the status of the board, and ensure that a strap is installed between E16-1 and E16-2 (2C8) to enable the high-speed SELCH protocol signal to the multiplexor (MUX) bus. If the ULI is installed under a bus switch and is in the high-speed SELCH protocol mode, install straps between E1-1 and E1-2 (2G9) and between E16-1 and E16-3 (2C8) to enable the high-speed SELCH protocol signal under the bus switch to the MUX bus. See Figure 2-11.

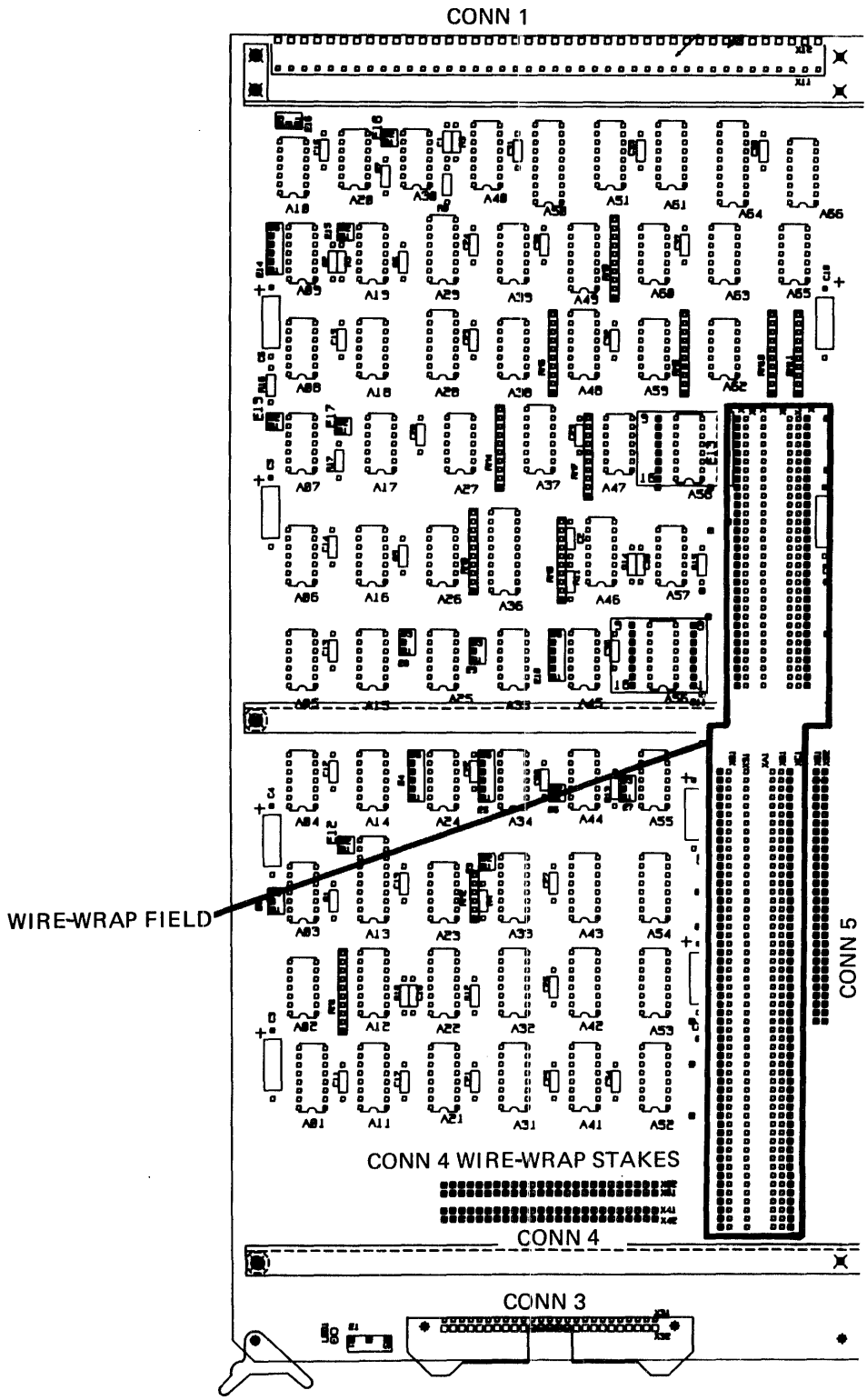


Figure 2-9 Component Side Wire-Wrap Field

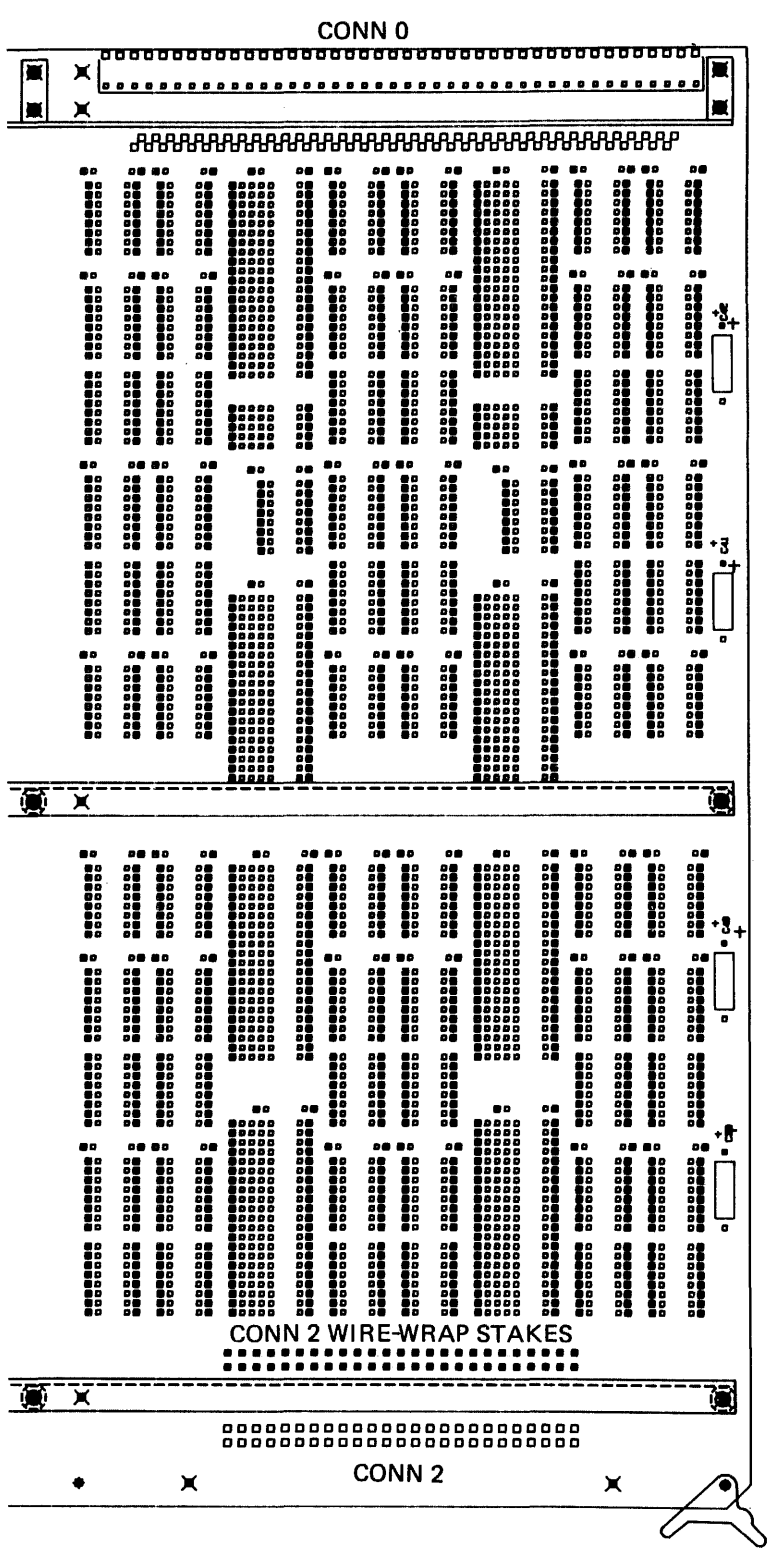


Figure 2-10 Wire-Wrap Side Wire-Wrap Field

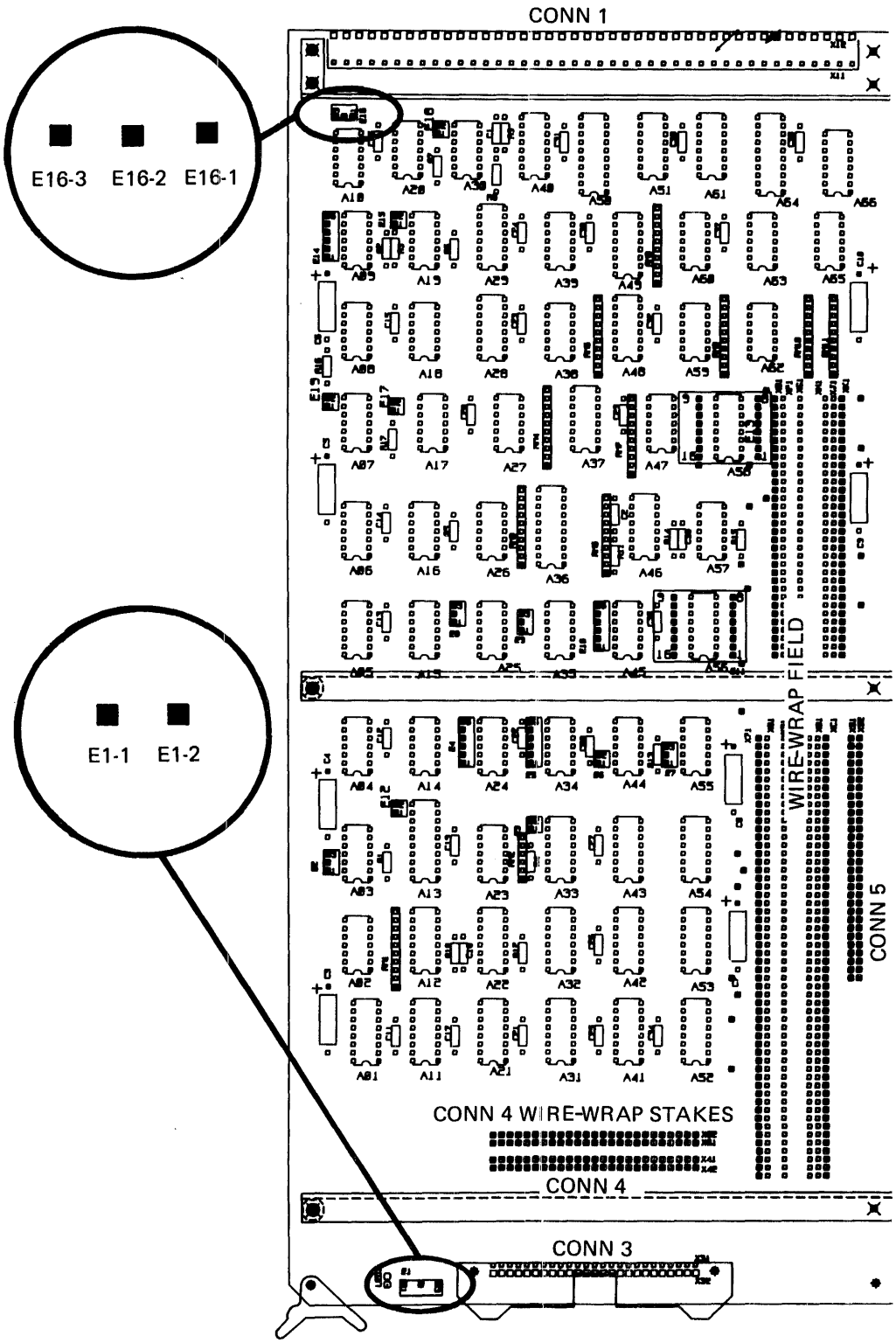


Figure 2-11 High-Speed SELCH Protocol

2.8.2 Command Bit 10

Bit 10 of the command is program controlled to determine if a byte or halfword transfer is to occur. If bit 10 is not program controlled, it can be used as an additional command bit. This is accomplished by removing the straps between E19-1 to E19-2 and E17-1 to E17-2 and connecting the system to the bit 10 line at E19-1. See Figure 2-12.

NOTE

When bit 10 is not in the programmable mode: ground E17-2 for halfword mode; ground E19-2 for byte mode.

2.8.3 Line Receivers

Prior to running the ULI self-test, the line receivers connected to CONN 4 must be disabled by connecting a strap between E3-1 and E3-2 as shown in Figure 2-13.

2.8.4 Addressing

The ULI's standard address is X'8B'. This is set on an eight switch DIP socket and can be changed by the user as required.

Bits 6 and 7 (4E6) have a strap option that enables them to be inverted for use under a subchannel controller (SCC). See the Subchannel Controller Installation and Maintenance Manual for details.

2.9 35-860 UNIVERSAL LOGIC INTERFACE (ULI)/M48-013 ULI COMPATIBILITY

To make the 35-860 ULI compatible with the M48-013 ULI, the signals from CONN 5 are wired directly to CONN 2 for peripheral interface.

2.10 TESTING

See Chapter 4 for equipment testing and the ULI diagnostic.

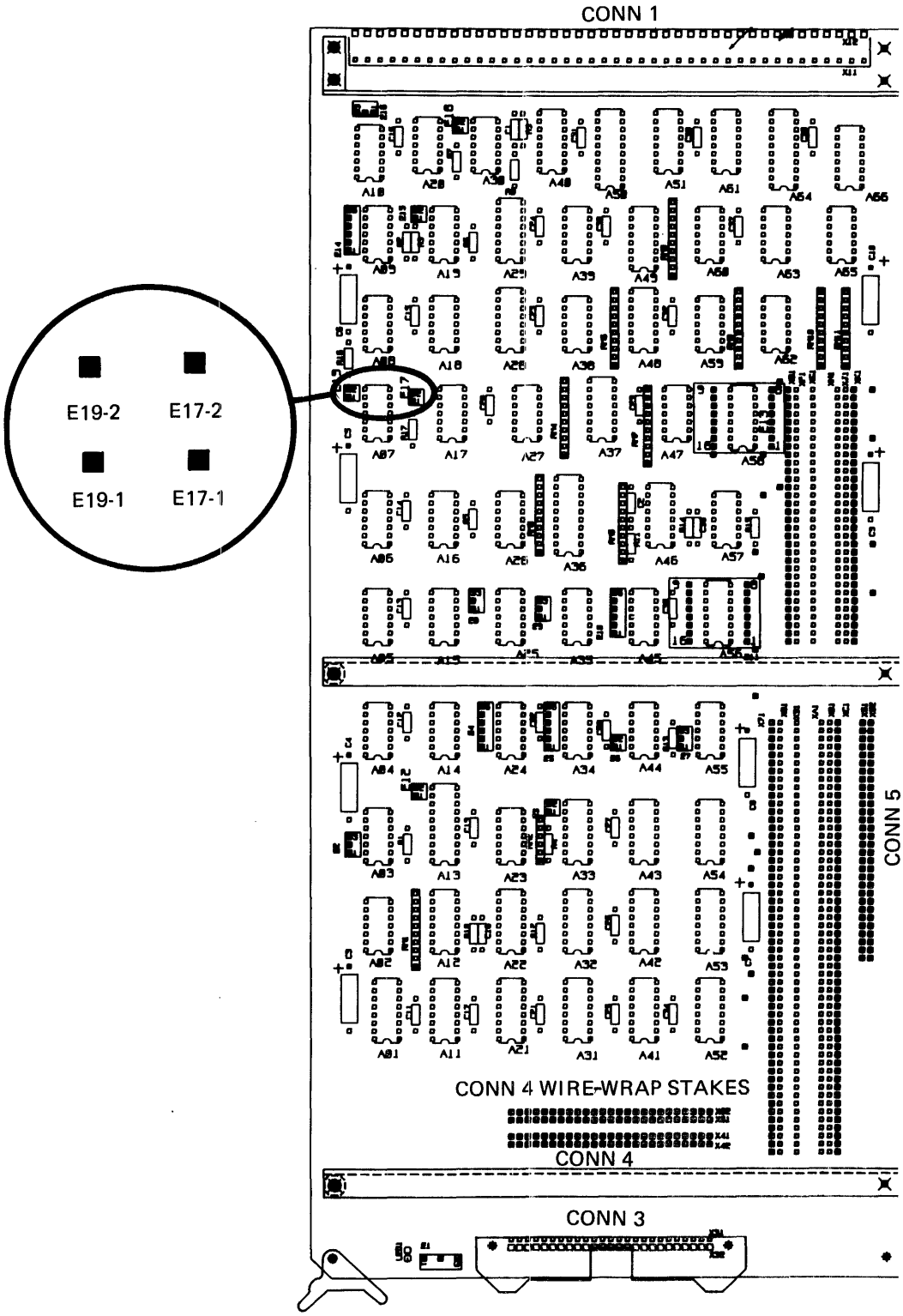


Figure 2-12 Command Bit 10 Option

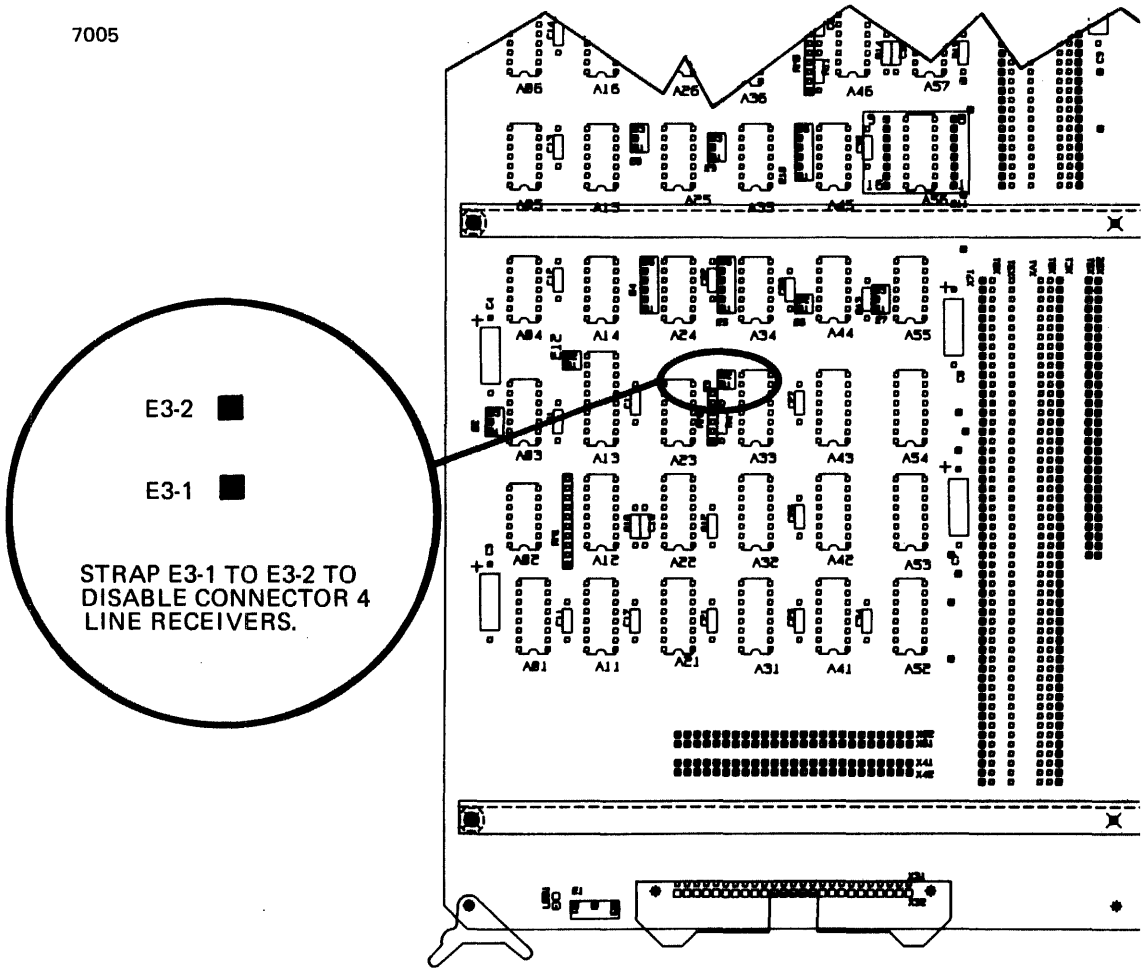


Figure 2-13 Strap to Disable Line Receivers During Self-Test

CHAPTER 3
THEORY OF OPERATION

3.1 INTRODUCTION

The universal logic interface (ULI) is an interface device designed to provide a convenient byte or halfword interface for the Perkin-Elmer Multiplexor (MUX) Bus. The ULI can be either an interface for a custom-built user device controller, which can be located in one of the on-board wire-wrap fields, or be a stand-alone interface with long distance data transmission capabilities. Data can be transferred between the ULI and the MUX bus in a byte mode or in a true 16-bit parallel halfword mode. The data transfer mode is set up under program control. The interrupt line can be disabled, enabled or disarmed within the ULI by program control. The ULI can operate with either of two protocols, the standard input/output (I/O) protocol or the high-speed selector channel (SELCH) protocol.

This chapter describes the functional operation of the ULI and its relationships with the user device controller and the processor. Also included are a block diagram analysis, a functional analysis and a mnemonics list for the ULI.

3.2 PROCESSOR BACKPANEL MULTIPLEXOR (MUX) BUS SIGNALS

An 84-pin connector (CONN 1 or CONN 0, as required) connects the ULI to the processor backpanel to provide MUX bus I/O signals to the ULI. See Figure 3-1 and Tables 3-1 and 3-2.

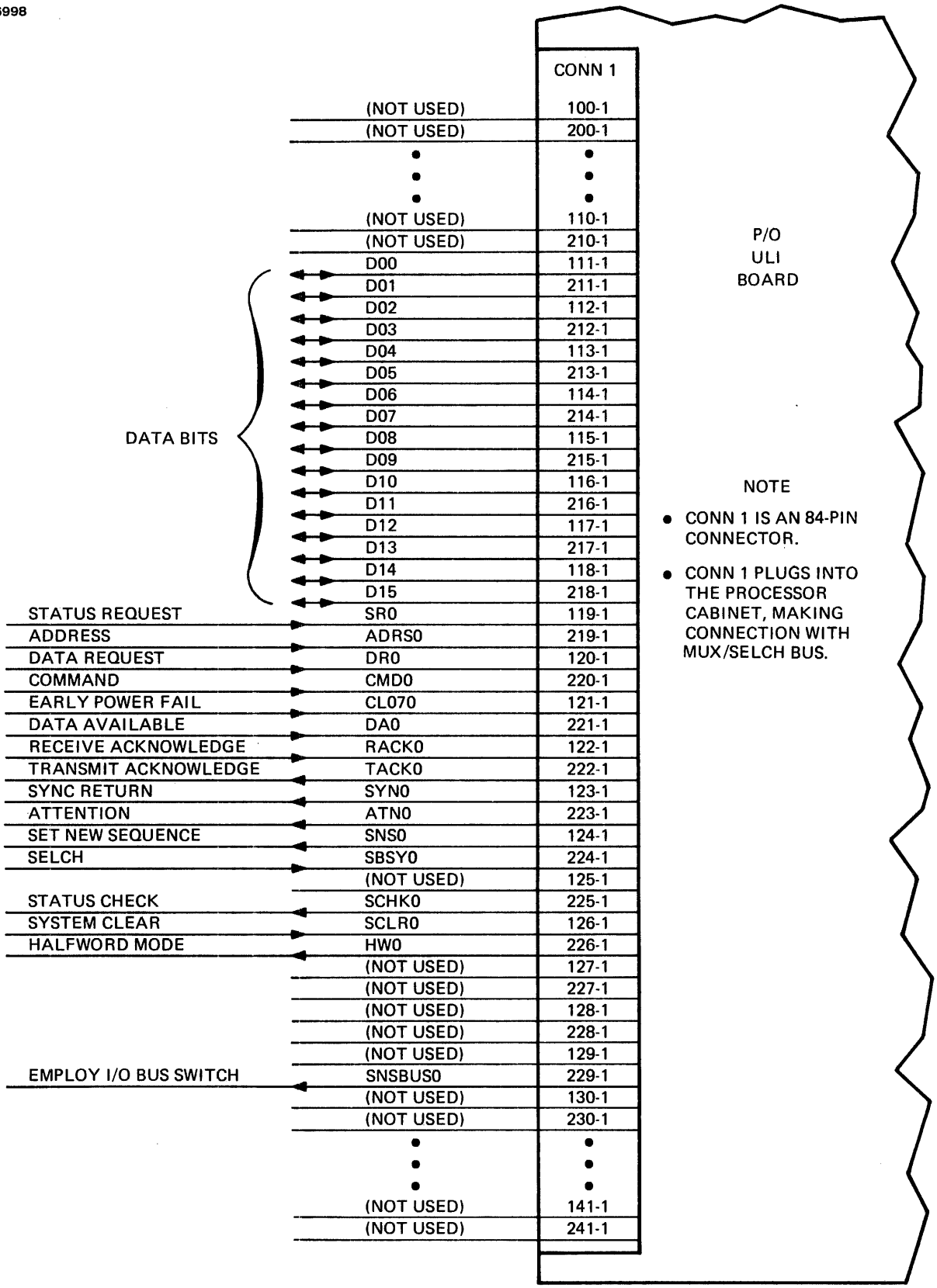


Figure 3-1 Connector 1 to MUX/SELCH Bus

TABLE 3-1 PIN MAP FOR CONNECTOR 1

CONNECTOR 1		
ROW 1	ROW 2	PIN NO.
P5	GND	41
GND	GND	40
		39
		38
		37
		36
		35
		34
		33
		32
		31
		30
	SNSBUS0	29
		28
		27
SCLR0	HW0	26
	SCHK0	25
SNS0	SBSY0	24
SYN0	ATN0	23
RACK0	TACK0	22
CL070	DA0	21
DR0	CMD0	20
SR0	ADRS0	19
DMUX140	DMUX150	18
DMUX120	DMUX130	17
DMUX100	DMUX110	16
DMUX080	DMUX090	15
DMUX060	DMUX070	14
DMUX040	DMUX050	13
DMUX020	DMUX030	12
DMUX000	DMUX010	11
		10
		09
		08
		07
		06
		05
		04
		03
		02
GND	GND	01
P5	GND	00

TABLE 3-2 MUX BUS SIGNAL LINES

TYPE	MNEMONIC	DIRECTION PROCESSOR ⟷ ULI	NUMBER
Data lines	DMUX000:150	⟷	16 lines
Control lines	ADRS0	→	1 line
	SR0	→	1 line
	DR0	→	1 line
	DA0	→	1 line
	CMD0	→	1 line
	RACK0/TACK0	—(daisy-chain)→	1 line
	CL070	→	1 line
Test lines	SYN0	←	1 line
	ATN0	←	1 line
	HW0	←	1 line
Initialize line	SCLR0	→	1 line

3.2.1 Signal Line Definitions

- Data lines

  DMUX000:150

  These 16 low-active data lines are used to transfer, in parallel, a byte or 16-bit halfword of data between the processor and the user device controller. In the byte mode, the data is transferred on the least significant data lines (080:150) on backpanel pins 115 through 218. In the halfword mode, the data is transferred on the 16 data lines (00:150) on backpanel pins 111 through 218.

- Control lines

  Address (ADRS0)

  This low-active control line is activated by the processor to all the device controllers. It is accompanied by an 8- or 10-bit device address on the data lines 060:150 to select one device controller for subsequent I/O transfers. This line uses backpanel pin 219.

Status Request (SRO)

This low-active control line is activated by the processor to the selected user device controller. The device controller gates its status byte onto the data lines 080:150. This line uses backpanel pin 119.

Data Request (DRO)

This low-active control line is activated by the processor to the selected user device controller. The user device controller gates a byte or halfword of data onto the data lines. This line uses backpanel pin 120.

Data Available (DAO)

This low-active control line is activated by the processor to the selected user device controller, accompanied by a byte or halfword of data on the data lines. This line uses backpanel pin 221.

Command (CMDO)

This low-active control line is activated by the processor to the selected user device controller, accompanied by a command byte on the data lines. This line uses backpanel pin 220.

Interrupt Acknowledge (RACKO)

This low-active control line is activated by the processor to the user device controller in a serial daisy-chain fashion. The first user device controller in the priority chain having an interrupt pending inhibits propagation of TACKO to lower priority devices and gates its device address onto the data lines. This line uses backpanel pins 122 (RACKO) and 222 (TACKO).

Early Power Fail Warning (CL070)

This low-active control line is activated by the processor to all the user device controllers when a power fail condition is detected by the processor. This control line is held active until Initialize (SCLRO) is activated. This line uses backpanel pin 121.

- Test lines

Synchronize (SYNO)

This low-active test line is activated by the user device controller to inform the processor that the device has properly recognized and responded to a control line signal.

For an address operation, SYN0 is activated only by the device controller being addressed. SYN0 is not activated by any user device controller in response to the CL070 control line. For status request, data request, command and data available operations, SYN0 is activated only by the currently selected user device controller. This line uses backpanel pin 123.

Attention (ATN0)

This low-active test line is activated by any user device controller to inform the processor that an interrupt is pending. This test line remains active until it has received an interrupt acknowledge (RACK0) control line signal. Several device controllers can activate ATN0 concurrently. This line uses backpanel pin 223.

Halfword (HW0)

This low-active test line is activated by a halfword-oriented user device controller at all times while it is addressed. A byte-oriented user device controller must not activate this test line. This line uses backpanel pin 226.

- Initialize line

System Clear (SCLR0)

This low-active line is activated during a system power up, system power down or initialization. This line uses backpanel pin 126.

With the exception of the serial RACK0/TACK0 line, all I/O signal lines are connected in parallel to all user device controllers on the MUX bus.

3.2.2 Multiplexor (MUX) Bus Input/Output (I/O) Timing

The request/response signals are used for both input and output MUX bus operations. This allows the MUX bus to run at its maximum speed whenever possible, but permits a graceful slowdown if the characteristics of a particular user device controller require signals of longer duration. User device controller designs for the wire-wrap fields of the ULI should keep I/O timing as fast as possible, consistent with practical circuit margins and the required minimum timing, as shown in the following sections. Any delays in the I/O timing that exceed the specified minimum timing result in increased I/O instruction execution time and degrade system throughput.

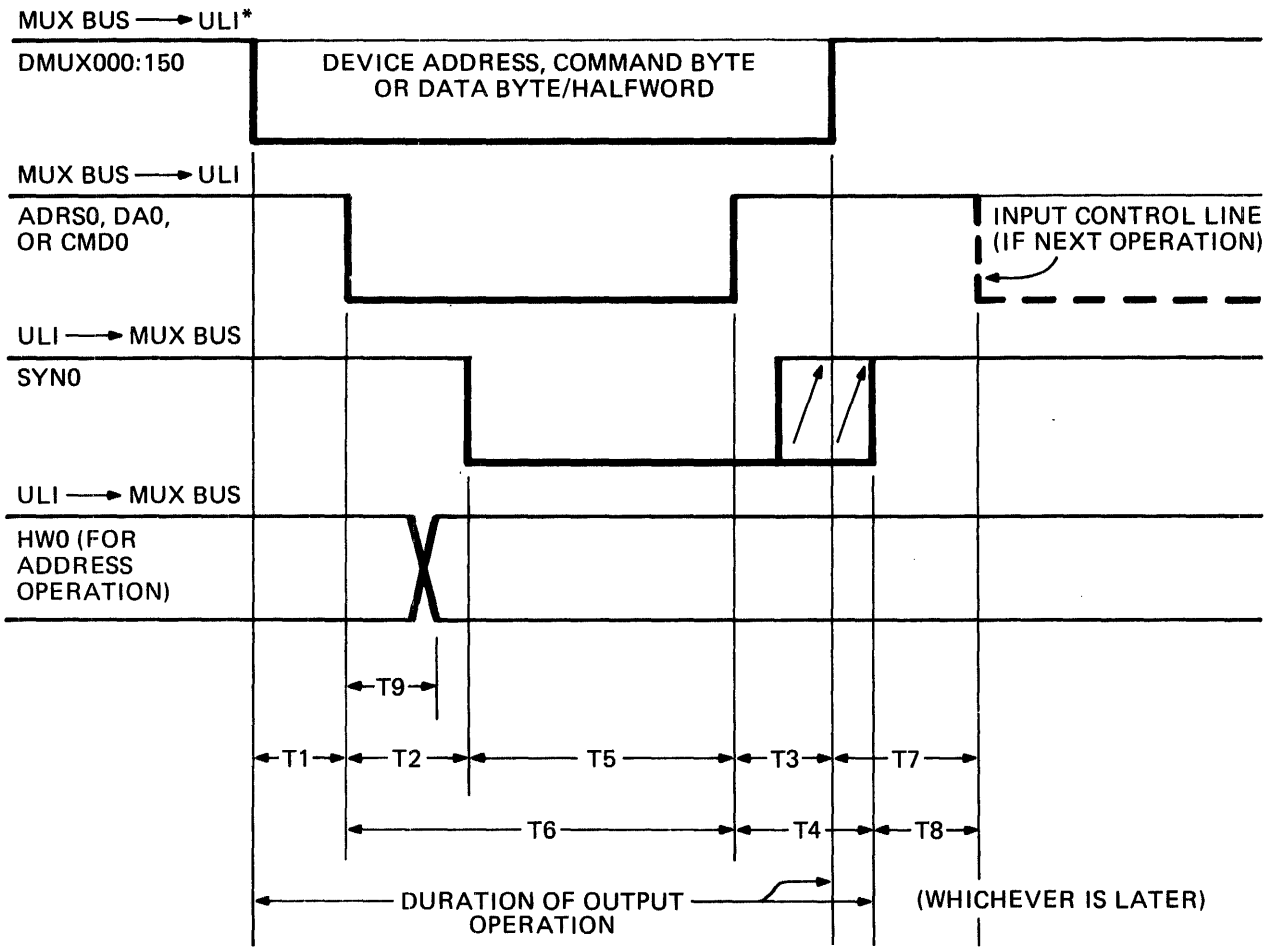
3.2.2.1 Output Timing

Figure 3-2 shows the timing for the three types of output I/O operations: Address (ADRS0), Command (CMD0) and Data Available (DA0). To start an output operation, the processor activates the MUX bus data lines with the desired data, followed by the activation of the appropriate control line (ADRS0, CMD0 or DA0). The time between the activation of the data lines and the activation of the control line at Time 1 (T1) varies, but is guaranteed to be at least 75 nanoseconds at the ULI input. This allows the ULI to recognize address match, decode or command information prior to the leading edge of the control line signal. The leading edge of the control line signal should be used where edge-triggered latches or flip-flops are used to store commands, data or address match. When the ULI has accepted the command or data or recognized an address match, it activates the Synchronize (SYN0) test line to the processor.

For command and data available operations, the processor deactivates the control line signal (after a delay of at least 100 nanoseconds) after the ULI activates SYN0. In an address operation, the processor holds the address control line active, despite the presence of SYN0, for at least 350 nanoseconds. After the control line is deactivated, the processor holds the data lines active for an additional 75 nanoseconds (minimum) at Time 3 (T3). The ULI must minimize the SYN0 deactivation time at Time 4 (T4) after the control line signal is deactivated, as the processor cannot begin another input or output operation until SYN0 deactivates. After the processor deactivates the data lines, it must wait at least 100 nanoseconds before activating any control line for an input I/O operation.

3.2.2.2 Input Timing

Figure 3-3 shows the timing for the three types of input I/O operations: Status Request (SR), Data Request (DR) and interrupt Acknowledge (ACK). To start an input operation, the processor activates one of the applicable control lines: SR, DR or Receive Acknowledge (RACK0). The ULI then gates the appropriate data onto the MUX bus data lines with minimum delay, and activates the SYN0 test line. Data must be stable on the bus before SYN0 is activated. The processor must take into account the worst case data slew of 25 nanoseconds before latching the data after SYN0 goes active. In response to SYN0, the processor accepts the contents of the data lines, and deactivates the control line with a minimum delay of 100 nanoseconds after SYN0 is activated. As the control line is deactivated, the ULI must deactivate the MUX bus data lines and deactivate SYN0 with a minimum delay. The processor considers the operation complete when SYN0 deactivates.



NOTE: TIMING SHOWN AT DEVICE CONTROLLER INPUTS

T1, T3 } 75 NS GUARANTEED MINIMUM AT CONTROLLER INPUTS

T2 – AS SHORT AS POSSIBLE AFTER DEVICE RECOGNIZES ADDRESS OR ACCEPTS DATA OR COMMAND

T4 – AS SHORT AS POSSIBLE

T5 – 100 NS MINIMUM

T6 – 350 NS MINIMUM FOR ADRS0; DA0 AND CMD0 HAVE NO MINIMUM BUT DEACTIVATE AFTER SYN0 ACTIVATES

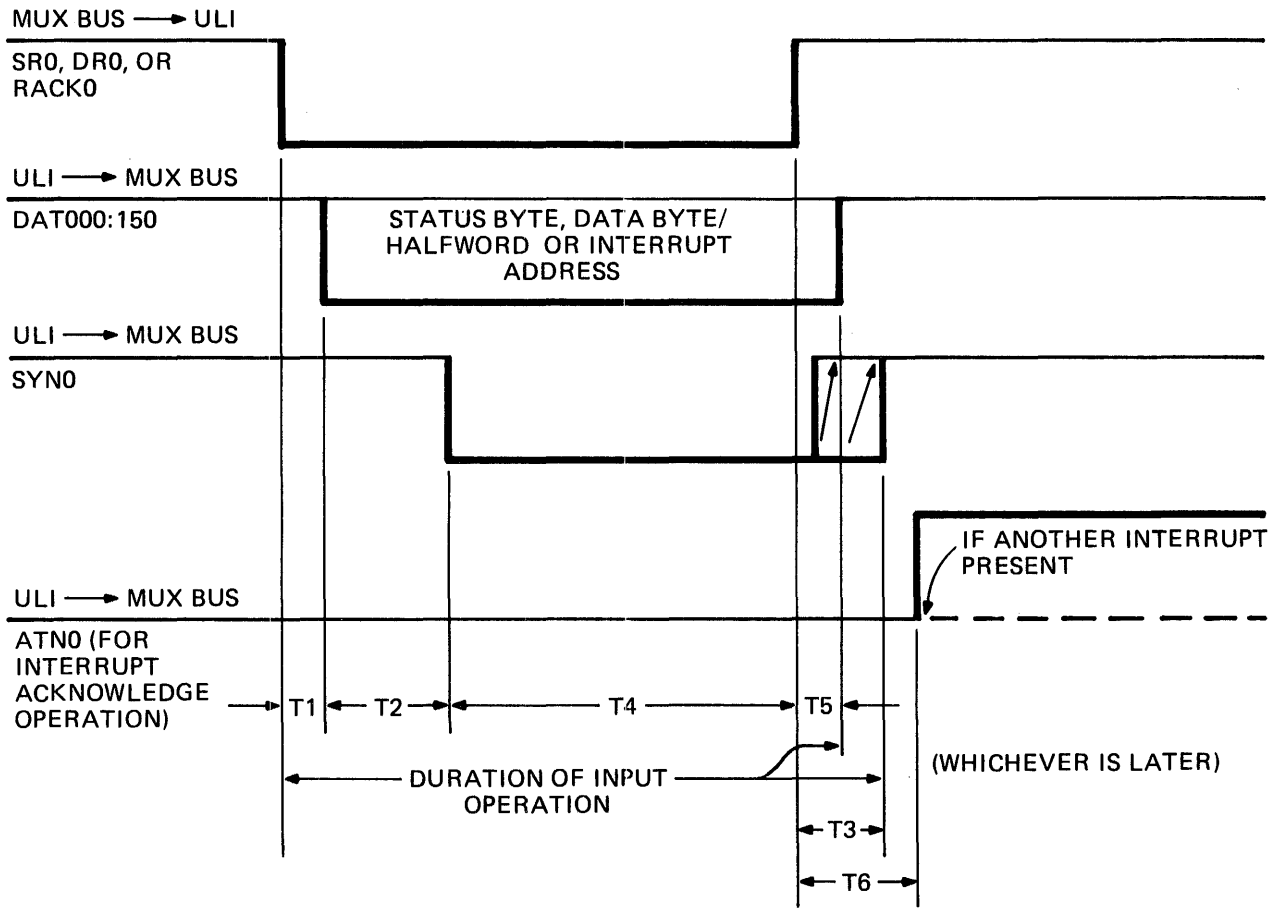
T7 – 100 NS MINIMUM

T8 – MUST BE GREATER THAN ZERO

T9 – MUST BE LESS THAN T2

*THE PROCESSOR MUST DEACTIVATE THE DATA LINES A MINIMUM OF 100 NANOSECONDS BEFORE ACTIVATING ANY CONTROL LINE FOR THE NEXT I/O OPERATION.

Figure 3-2 Output I/O Operation Timing



NOTE: TIMING SHOWN AT DEVICE CONTROLLER INPUTS

T1 – AS SHORT AS POSSIBLE
T2 – MUST BE GREATER THAN ZERO
T3 – AS SHORT AS POSSIBLE
T4 – 100 NS MINIMUM
T5 – AS SHORT AS POSSIBLE
T6 – MUST BE GREATER THAN ZERO – I.E., DEVICE MUST NOT DEACTIVATE ATN0 BEFORE RACK0 (AT DEVICE INPUT) DEACTIVATES.

Figure 3-3 Input I/O Operation Timing

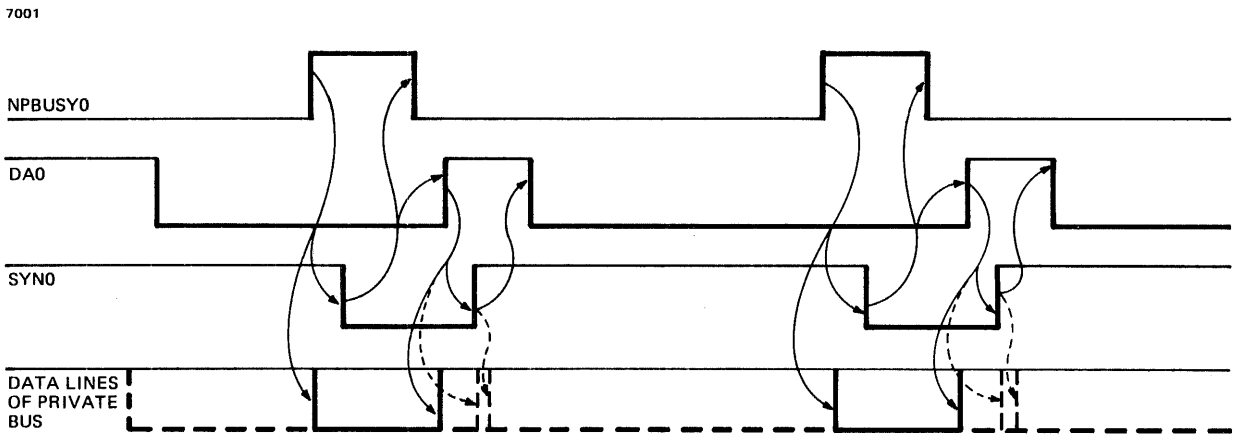
3.3 HIGH-SPEED SELECTOR CHANNEL (SELCH) PROTOCOL

The ULI operates with a byte- or halfword-oriented device. These modes are program controlled as specified in Chapter 5. The ULI operates in two I/O protocols, standard and high-speed SELCH. The high-speed SELCH protocol supports user device controllers that must sustain higher throughputs than are achieved using the standard protocol. Higher throughput is achieved by eliminating the status check operation between transfer operations and speeds up the data transfer procedure. The high-speed SELCH protocol is available on the M48-050 M01 buffered SELCH (BSELCH) (32-bit machines only). Table 3-3 shows the three additional control/test signals required for SELCH protocol. Timing for the high-speed protocol is shown in Figure 3-4.

TABLE 3-3 HIGH-SPEED SELCH SIGNAL LINES

TYPE	MNEMONIC	DIRECTION BSELCH ⇄ DEVICE	NUMBER
Control line	SBSYO	→	1 line
Test lines	SNSO	←	1 line
	SCHKO	←	1 line

(In addition to the 37 lines listed in Table 3-2.)



NOTE: DOTTED LINE INDICATES WRITE MODE

Figure 3-4 High-Speed Protocol Data Transfer Timing

3.3.1 High-Speed Buffered Selector Channel (BSELCH) Signal Line Definitions

- Control line

  SELCH busy (SBSY0)

  This low-active control line is activated by the buffered SELCH (BSELCH) to the selected user device controller, indicating that a SELCH block data transfer is in progress. This line uses backpanel pin 224-1.

- Test Lines

  Switch to New Sequence (SNS0)

  This low-active test line is activated by the selected user device controller to the BSELCH to specify that the user device controller supports the high-speed SELCH protocol. It remains active at all times while the user device controller is selected. This line uses backpanel pin 124-1.

  Status Check (SCHK0)

  This low-active test line is activated by the selected user device controller to the BSELCH to indicate the occurrence of a bad status condition (bad status = STAT130 + STAT140 + STAT150). This line can be activated only while either the Private Data Available (PDA0) control line or the Private Data Request (PDR0) control line is active and at least 50 nanoseconds before the user device controller activates Private Synchronization (PSYN0). Once activated, it must remain active until after SBSY0 (2A1) deactivates. This line uses backpanel pin 225-1.

All the listed control and test lines are connected in parallel to all devices on the SELCH bus.

3.3.2 User Interface Timing

The following sections describe the interaction of the user interface to the MUX bus via the ULI. The user interface is defined as the signals available at connectors 3, 4 and 5 (CONN 3, 4 and 5).

3.3.2.1 Interrupts

Figure 3-5 shows the sequence of signals required to interrupt the processor. The user enables Set Attention (SATN0) for a minimum of 40 nanoseconds. This creates an Attention pulse (ATN0) to the processor, indicating that an interrupt is pending. The processor returns an acknowledge signal that is propagated as Receive Acknowledge (RACK0). This allows the ULI to complete the handshaking by returning SYNC. As the Acknowledge signal (ACK0) is returned, the user receives a Reset Attention signal (RSTATN0) indicating that the attention was accepted and SATN0 can be reset.

3.3.2.2 Receive Data or Commands

Figure 3-6 shows the sequence of signals required to receive data or commands from the processor. The processor enables Command (CMD0) or Data Available (DA0). This in turn enables CMDE0 or DAE0 on the user interface at CONN 3 and 5. The user latches the command or data at the trailing edge of CMDE0 or DAE0 to guarantee that it is valid. The user enables the Busy signal at this time to allow time to process the command or data. BUSY is disabled prior to the next transmission.

3.3.2.3 Send Data or Status

Figure 3-7 shows the sequence of signals required to send data or status to the processor. The processor enables Data Request (DR0) or Status Request (SR0). This in turn enables DRE0 or SRE0 on the user interface at CONN 3 and 5. The user typically has 250 nanoseconds to place valid data or status on the bus before the ULI returns SYNC.

3.3.2.4 High-Speed Selector Channel (SELCH) Protocol

Figure 3-8 shows that when operating in high-speed SELCH protocol, NPBUSY is used to control transfers. If DAE0 or DRE0 is enabled while NPBUSY0 is active, SYNC is not returned to the processor. When the user is ready and disables NPBUSY0, SYNC is returned to the processor to complete the transfer.

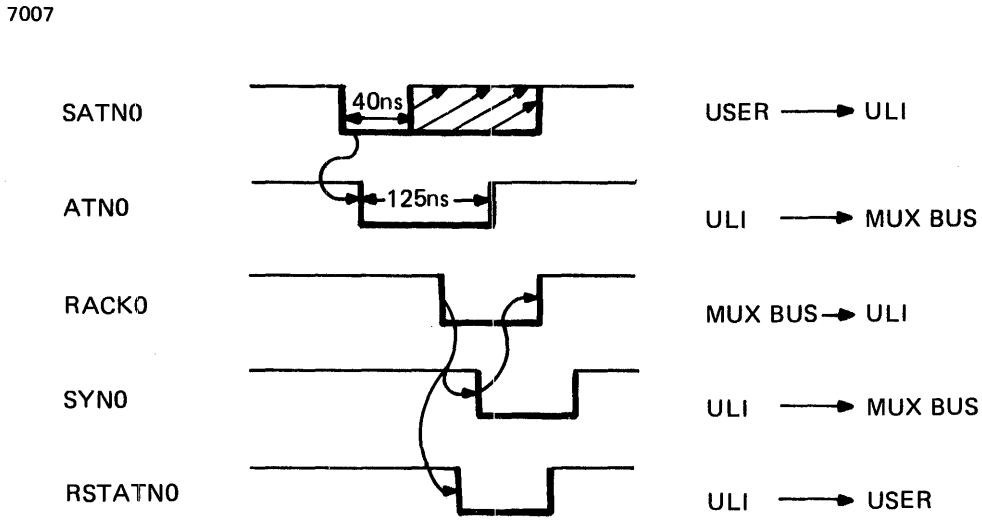


Figure 3-5 Interrupt Timing

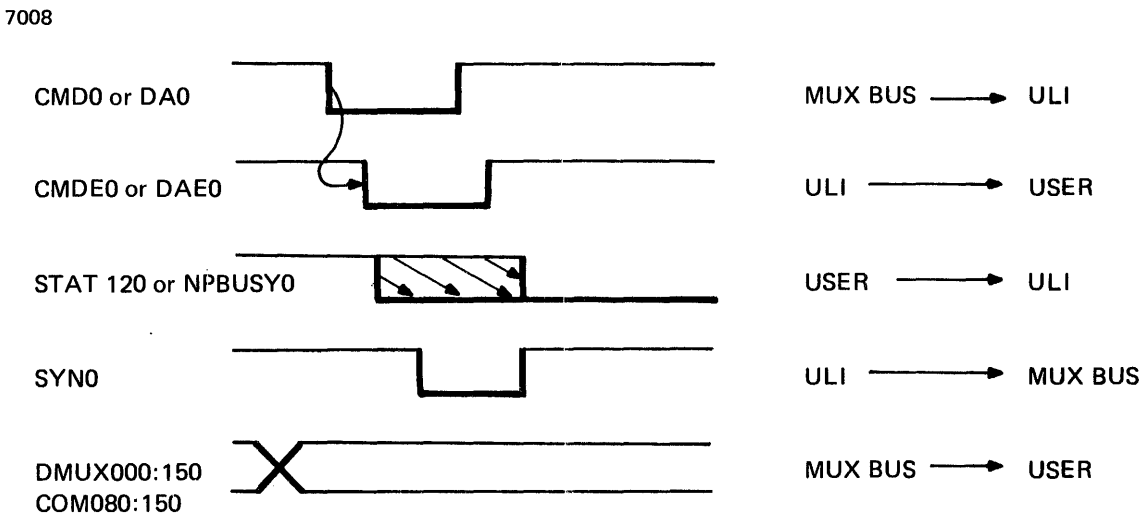


Figure 3-6 Receive Data or Command Timing

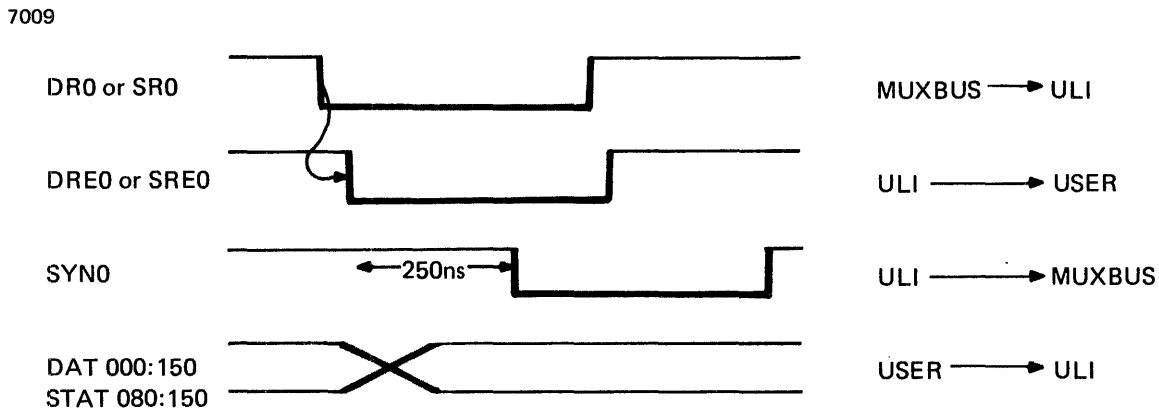


Figure 3-7 Send Data or Status Timing

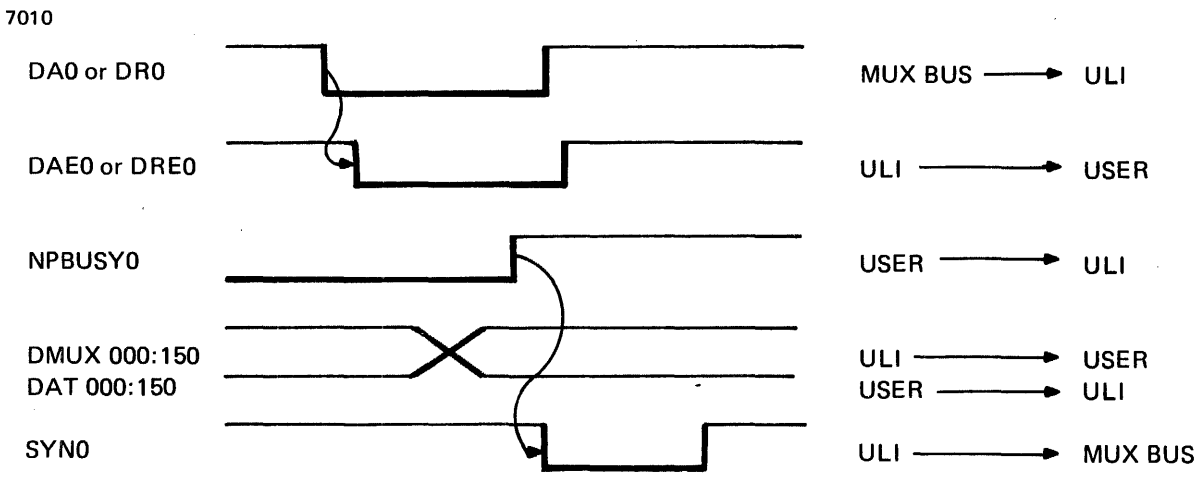


Figure 3-8 High-Speed SELCH Protocol Timing

3.4 BLOCK DIAGRAM ANALYSIS

The ULI is a communication link between the processor MUX bus and byte- or halfword-oriented peripheral equipment. See Functional Schematic 35-860D08 and Figure 3-9.

The functions that are integrated in the operation of the module are: status, command, data output and data input.

3.4.1 Status

Eight Status input lines (STAT080:150) are available to the user. The user connects the desired sense lines to eight status input lines. To read in status on the eight status lines, the program executes a sense status instruction that causes the processor to generate a Status Request pulse (SR0). The SR0 pulse enables the transfer of status from the eight Status input lines (STAT080:150) onto data lines DMUX080:150. When in high-speed SELCH protocol, this sense status is suppressed except if Status Check (SCHK0) is asserted. This only occurs when a bad status condition exists on the status lines.

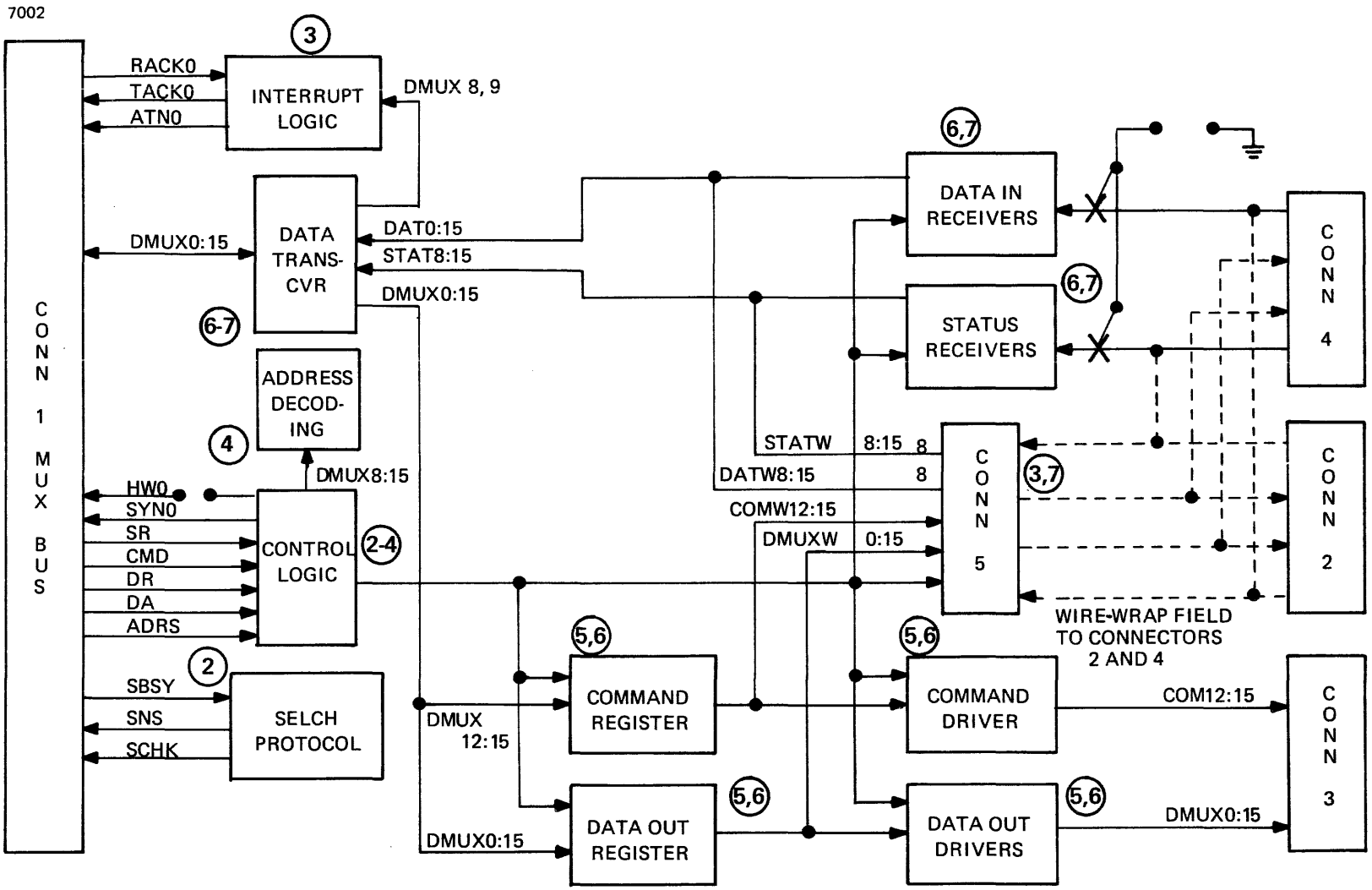
3.4.2 Command

The Command control lines (COM080:150) are generated from the data lines (DMUX080:150) and are used as follows:

- The two most significant bits of the command byte (bits 8 and 9) disable, enable or disarm the interrupt logic. See Section 5.7 for detailed information.
- The third bit of the command byte (bit 10) determines if a byte or halfword transfer is to occur. If this mode is not program controlled, command bit 10 can be used as an additional command bit. See Section 2.8.2 for strapping information.
- The fourth command bit (bit 11) can be used as an additional command bit when using a wire-wrap field.
- The four least significant bits of the command byte (bits 12:15) are user extended as COM120:150.

3.4.3 Data

Sixteen Data output lines (DMUX000:150) and sixteen Data input lines (DAT000:150) are available to the user. These data lines can be used in either byte or halfword mode and with either standard or high-speed SELCH protocol.



⊗ INDICATES SCHEMATIC SHEET
** WIRE-WRAP STAKES TO SET TO HALFWORD OR BYTE MODE WHEN USING COMMAND BIT 10 AT A USER-EXTENDED BIT.

Figure 3-9 ULI Block Diagram

3.4.3.1 Input

When the ULI is address selected and there is a data request, data is gated to the MUX bus from data lines DAT080:150 if the ULI is in the byte mode. If the ULI is in the halfword mode, data is gated from lines DAT000:150.

3.4.3.2 Output

When the ULI is address selected and Data Available (DA0) is activated, data is gated from the MUX bus to the data lines DMUX080:150 if the ULI is in the byte mode. If the ULI is in the halfword mode, data is gated from data lines DMUX000:150.

3.5 FUNCTIONAL DIAGRAM ANALYSIS

The following sections provide a functional analysis of the ULI. See Functional Schematic 35-860D08 and Figure 3-10.

3.5.1 Addressing

To communicate with the ULI, it must first be addressed. The ULI address (X'8B' preferred) is placed on data lines DMUX000:150 (Sheet 4) and the address control line is activated (ADRS0) (2A3). The eight bits of the data lines are compared to the setting of the address DIP switch. If there is a match, SYN0 is returned to the processor, and AD1 (2F4) is activated. If there is no match, AD1 is deactivated.

3.5.2 Command

An active command control line (CMD0) (2A6) is ANDed with AD1, enabling SYN0 to the processor. CMD0 also generates CMG1 (2F7), which loads command information from data lines DMUX120:150 onto the four command lines (COM120:150). The leading edge of CMG1 clocks the DISARM (3G7) and DISABLE (3H7) flip-flops to disable, enable or disarm the interrupt logic.

The CMD0 and data bit 10 (DMUX100) optionally determine the data transfer mode of operation. See Section 3.4.2. To establish the halfword mode, CMD0 and data bit 10 must be active. The CMG1 pulse sets the halfword flip-flop (2K2). The set output of the halfword flip-flop causes the halfword line (HW0) (2N2) to become active indicating to the processor that the ULI will perform halfword data transfers.

In the byte mode, CMD0 active and data bit 10 inactive, the halfword flip-flop is reset by the CMD0 pulse. The HW0 to the processor becomes inactive indicating that the ULI will perform byte data transfers.

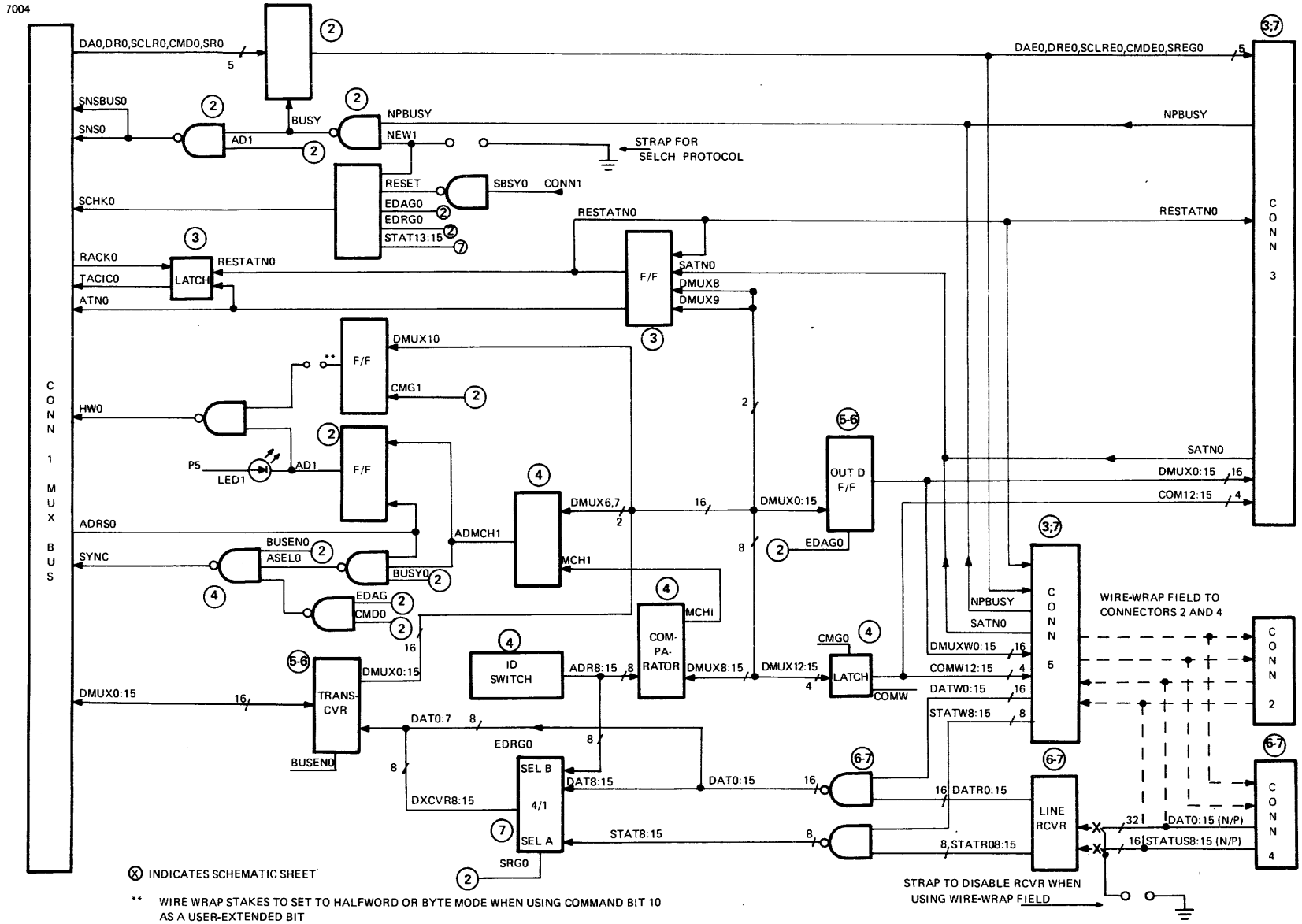


Figure 3-10 ULI Functional Diagram

3.5.3 Status Request (Sense Status Instruction)

Status Request (SR0) is ANDed with AD1, activating BUSEN0 (2N7), which enables SYN0 to the processor. A high EDRG0 and a low SRG0 are input to the four four-to-one multiplexors (7A3) to load status information on status input lines STAT080:150 onto the data lines DMUX080:150 of the MUX bus.

3.5.4 Data Available (Write Data Instruction)

In the byte mode (halfword flip-flop reset), when a write data instruction is executed, a Data Available (DA0) pulse is sent from the processor. The DA0 pulse is ANDed with AD1 and causes SYN0 to be returned to the processor. The DA0 pulse also causes EDAG0 to go active; this loads the data being sent from the processor on data lines DMUX080:150 into the output data register. Successive DA0 pulses perform the same operation.

In the halfword mode (halfword flip-flop set), SYN0 is enabled to the processor, and data from the MUX bus is gated to data output lines DMUX000:150.

3.5.5 Data Request (Read Data Instruction)

In the byte mode (halfword flip-flop reset), when a read data instruction is executed, a Data Request (DR0) pulse is sent from the processor. The DR0 pulse is ANDed with AD1, activating BUSEN0, which enables SYN0 to the processor. DR0 also causes EDR0 to go active, enabling data input lines DAT080:150 to be gated to the MUX bus. Successive DR0 pulses perform the same operation.

In the halfword mode (halfword flip-flop set), SYN0 is enabled to the processor. BUSEN0 loads the data byte from data input lines DAT000:070 onto the MUX bus. With EDRG0 high and SRG0 low, the data lines DAT080:150 are loaded onto the MUX bus by the four four-to-one multiplexors.

3.5.6 Interrupts

When an interrupt is generated, the attention flip-flop is set directly via a differentiated negative going pulse, Set Attention (SATN0). The output from the attention flip-flop generates an Attention (ATN0) signal to the processor. Command bits 8 and 9 provide control over the attention flip-flop and the ATN0 line to the processor. With bit 8 true and bit 9 false, the attention flip-flop is disabled. That is, the flip-flop can be set, but the output is held low. With bit 8 false and bit 9 true, the ATN0 signal to the processor is active, which allows new interrupts or a queued interrupt to be recognized. With bits 8 and 9 both true, the low from the disarm flip-flop direct clears the attention flip-flop. The flip-flop is now in the disarm state and cannot be set by the interrupt line.

The disarm state is cleared whenever an enable or disable command is received. Initialize (SCLR0) also disarms the attention flip-flop.

Attention is connected to the interrupt line in the processor. The processor responds with an acknowledge interrupt signal that is received by the user device controller as Receive Acknowledge (RACK0). Since the attention flip-flop was set prior to RACK0, ATN1 holds the RACK0/TACK0 latch set (3H2), and the Transmit Acknowledge (TACK0) to other devices is held high. The RACK0 signal generates Reset Attention (RSTATN0) enabling SYN0 to the processor. Upon receiving SYN0, the processor removes RACK0, causing the attention flip-flop to reset.

3.5.7 Initializing

When the system is initialized (SCLR0), the attention, address, data request, data available, halfword and disable and disarm flip-flops are reset. SCLR0 is also sent to the user.

3.6 MNEMONICS

The mnemonics found in the ULI are described as follows. The source of each signal on Functional Schematic 35-860 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AD1	Indicates the board is addressed.	2F4
ADMCH1	Indicates the address matches to the switch setting.	4G6
ADR081:151	Indicates the lines that return the user to the processor.	Sheet 4
ADRS0	Specifies the address control signal from the processor.	2A3
ASEL0	Indicates ULI's address is selected.	2E4
ATN0	Specifies the user attention signal to the processor.	3M4
BUSEN0	Specifies the signal generated by processor requests; returns SYN0.	2N7
BUSY0	Used in high-speed SELCH protocol to determine when the board is busy.	2M9

MNEMONIC	MEANING	SCHEMATIC LOCATION
CL070	Specifies the clear signal from the processor.	2A4
CMD0	Specifies the ULI command signal from the processor.	2A6
CMDE0	Specifies the command signal from the ULI to the wire-wrap field.	4F8
CMG0	Specifies the gated command signal.	2G6
COM(N/P)120:150	Specifies the ULI command output lines to the user.	Sheet 4
COMW120:150	Specifies the ULI command output lines to the user via the wire-wrap field.	Sheet 4
DAG0	Indicates gated data is available.	2F4
DA0	Indicates data is available from the processor.	2A4
DAE0	Indicates data is available from the ULI to the wire-wrap field.	4F8
DASET	Indicates data available deglitching flip-flop is set.	2M5
DAT(N/P)000:150	Specifies data lines from the user to the ULI.	Sheets 5 and 6
DATW000:150	Specifies data lines from the wire-wrap field to the ULI.	Sheets 5 and 6
DMUX(N/P)000:150	Specifies data lines from the ULI to the user.	Sheets 5 and 6
DMUXW000:150	Specifies data lines from the ULI to the wire-wrap field.	Sheets 5 and 6
DR0	Indicates a data request from the processor.	2A5
DRE0	Indicates a data request from the ULI to the wire-wrap field.	4F9
DRG0	Indicates a gated data request.	2G5
DRSET	Indicates data request deglitching flip-flop is set.	2A7

MNEMONIC	MEANING	SCHEMATIC LOCATION
DSBL0	Interrupt disable prevents interrupts but allows queuing.	3H5
DSRM0	Interrupt disarmed prevents interrupts.	3G5
DXCVR080:150	Specifies data lines from multiplexors to the transceivers.	Sheet 7
EDAG0	Indicates deglitched data is available.	2L5
EDRG0	Indicates a deglitched data request.	2N7
HW0	Is the halfword mode signal.	2M2
NEW1	Indicates a gated high-speed SELCH protocol signal.	2J9
NPBUSY0	Indicates a user signal during high-speed SELCH protocol when ULI is busy.	2K9
PSYN0	Generates SYN0 to the processor.	2N6
RACK0	Specifies receive acknowledge from the processor.	3G2
RECENB	Indicates receive enable is active when line receivers are implemented. This line is grounded when either wire-wrap field is used.	7H9
RESET0	Specifies a reset status check in high-speed SELCH protocol.	2G1
RSTATN0	Specifies a reset attention signal.	4F8
SATN0	Set attention is an interrupt signal from the user.	3A3
SBSY0	Indicates SELCH busy is used in high-speed SELCH protocol to inhibit control signals.	2A1
SCHK0	Status check is used in high-speed SELCH protocol to determine when to check the status of the board.	4M8

MNEMONIC	MEANING	SCHEMATIC LOCATION
SCLREO	Indicates system clear to the user.	4F9
SCLRO	Indicates system clear from the processor.	2A4
SCLREO	Indicates system is clear from the processor to the wire-wrap field.	4F9
SNSBUSO	Indicates a high-speed SELCH protocol signal that is asserted when the board is addressed and under a bus switch.	2A8
SNSO	Indicates a high-speed SELCH protocol asserted when the board is addressed.	2A8
SRO	Specifies a status request from the processor.	2A7
SREO	Specifies a status request from the ULI to the wire-wrap field.	4F7
SRGO	Specifies a gated status request signal.	2G7
STAT(N/P)080:150	Specifies status lines from the user.	Sheet 7
STATW080:150	Specifies status lines from the user via the wire-wrap field.	Sheet 7
SYNO	Specifies a synchronization pulse to the processor.	4M6
TACKO	Specifies transmit acknowledge to the next device.	3M3
TSTCLRO	Specifies a test point on system clear.	2A4

CHAPTER 4
TESTING

4.1 INTRODUCTION

This chapter provides information concerning the state of the hardware equipment line receivers and the test cable/connector installation prior to running the 06-129 Universal Logic Interface (ULI) Diagnostic.

The ULI diagnostic program is used to check the proper operation of the ULI. Four tests are provided for exercising halfword and byte data transfers, output commands, status requests, the interrupt mechanism and selector channel (SELCH) protocols.

The program checks the halfword and byte modes by writing a user specified data pattern that can be a fixed value, a count or a shifting or random data pattern. The data pattern is read back from the user and compared to the original pattern. The same pattern is used to test the status return and command latches. After the data transfers are complete, the interrupt mechanism is tested. Output commands are used to disarm, arm and enable the ULI and generate an interrupt. The device number on acknowledge is also checked.

4.2 REQUIREMENTS

The following is a list of the minimum hardware requirements for executing the 06-129 program.

- A Perkin-Elmer 32-bit processor
- The ULI (product #35-860)
- A SELCH, if testing SELCH protocol
- The 17-650 test cable/connector (loopback connector 5 (CONN 5))
- A console input/output (I/O) device
- A program loading device

4.3 LINE RECEIVERS, THE TEST CABLE/CONNECTOR AND THE DIAGNOSTIC

Prior to running the ULI test, the line receivers must be disabled, and the loopback test cable/connector must be installed on CONN 5.

4.3.1 Line Receivers

The two status and four data quad RS422/3 line receivers connected to CONN 4 must be disabled. See Section 2.8.3 for strapping information.

4.3.2 Test Cable/Connector

The 17-650 test cable/connector must be installed on CONN 5 to loopback the test signals. See Figure 4-1 for a CONN 5 location and loopback signal connection diagram. See Table 4-1 for test cable/connector loopback connections.

TABLE 4-1 TEST CABLE/CONNECTOR LOOPBACK CONNECTIONS

SIGNAL	ROW	PIN	TO	ROW	PIN	SIGNAL
DATW000	1	00	TO	1	22	DMUX000
DATW020	1	01	TO	1	23	DMUXW020
DATW040	1	02	TO	1	24	DMUXW040
DATW060	1	03	TO	1	25	DMUXW060
DATW080	1	04	TO	1	26	DMUXW080
DATW100	1	05	TO	1	27	DMUXW100
DATW120	1	06	TO	1	28	DMUXW120
DATW140	1	07	TO	1	29	DMUXW140
STATW080	1	09	TO	1	28	DATW120
STATW100	1	10	TO	1	29	DATW140
STATW120	1	11	TO	1	15	COMW120
STATW140	1	12	TO	1	16	COMW140
COMM120	1	15	TO	2	17	SATN0
DATW010	2	00	TO	2	22	DMUXW010
DATW030	2	01	TO	2	23	DMUXW030
DATW050	2	02	TO	2	24	DMUX050
DATW070	2	03	TO	2	25	DMUX070
DATW090	2	04	TO	2	26	DMUXW090
DATW110	2	05	TO	2	27	DMUXW110
DATW130	2	06	TO	2	28	DMUXW130
DATW150	2	07	TO	2	29	DMUXW150
STATW090	2	09	TO	2	28	DATW130
STATW110	2	10	TO	2	29	DATW150
STATW130	2	11	TO	2	15	DATW130
STATW150	2	12	TO	2	16	COMW150

4.3.3 Diagnostic

See the Perkin-Elmer ULI diagnostic program description 06-129 for ULI self-test.

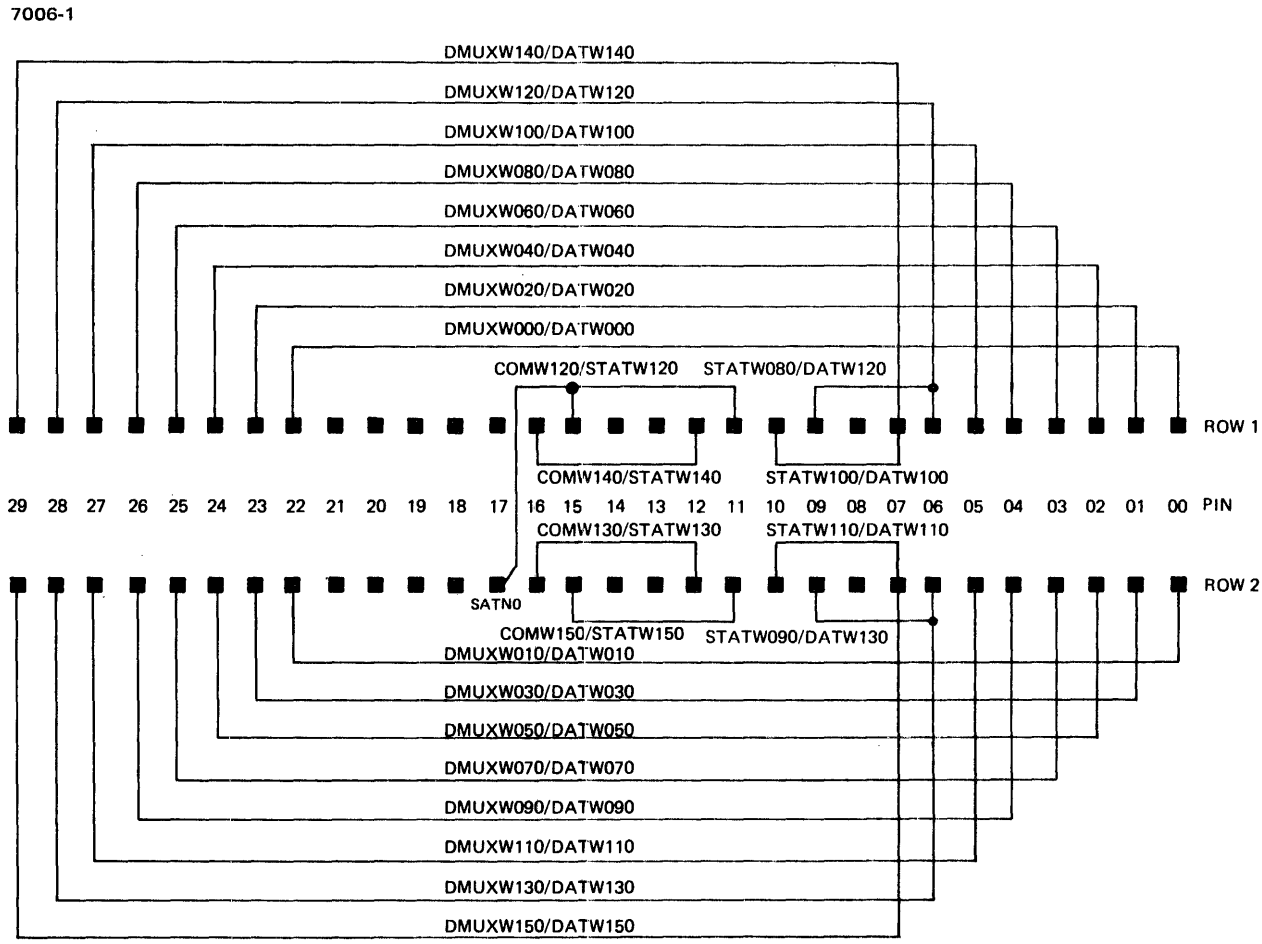


Figure 4-1 Test Cable/Connector Loopback Signal Diagram

CHAPTER 5
PROGRAMMING CONSIDERATIONS

5.1 INTRODUCTION

The universal logic interface (ULI) provides a fully buffered byte- or halfword-oriented interface module for data transfer between the processor and byte or halfword equipment provided by the user. The ULI is a transparent interface in that the function of any input/output (I/O) instruction issued depends upon the user's equipment. Data transfer rates can range from 1Mb per second, using standard protocol, to 3Mb per second, using high-speed selector channel (SELCH) protocol. This is dependent on the user's equipment and the related processor.

5.2 DATA FORMAT

The ULI can be interfaced with either a byte- or halfword-oriented device. The major functions available to the user are:

- sixteen data output lines (DMUX000:150) stored in a register that can be distributed by a halfword instruction,
- sixteen data input lines (DAT000:150) that can be read by executing a read halfword instruction,
- four command output lines (COM120:150) stored in a register that can be distributed by an output command instruction; these lines can be used as read or write commands, or for any other purpose determined by the user,
- eight status lines (STAT080:150) that can be read by executing a sense status instruction; the definition of the status lines is determined by the user,
- one priority interrupt line that can be queued and enabled by an output command,
- one initialize line that clears any pending interrupt and disarms the interrupt logic within the ULI, and

- five I/O control lines:

  - DAGO indicates data being sent by the processor.
  - DRGO indicates data being read by the processor.
  - SRGO indicates that the status bits are being read by the processor.
  - CMGO indicates that the command byte is being sent by the processor.
  - RSTATNO indicates that the interrupt that was queued has been acknowledged by the processor.

5.3 PROGRAMMING INSTRUCTIONS

Data transfer mode is selected by an output command to the device. Table 5-1 lists the output command bit assignments.

TABLE 5-1 OUTPUT COMMAND BIT ASSIGNMENT

BITS	8	9	10	11	12	13	14	15
COMMAND	DISABLE	ENABLE	HW		COMMAND OUTPUT LINES			
STATUS	STATUS INPUT LINES							

* Optional command bits

COMMAND BITS	MEANING
DISABLE	Setting this bit with enable reset prevents the device from interrupting the processor, but allows an interrupt to be queued.
ENABLE	Setting this bit with disable reset allows the ULI to interrupt the processor.
DISABLE-ENABLE	Setting both disable and enable bits places the ULI in the disarm mode. The ULI is prevented from interrupting the processor and interrupts are not queued if both these bits are reset. The priority interrupt state will not be changed.

HW	Setting this bit optionally places the ULI in the halfword mode. Resetting this bit optionally puts the ULI in the byte mode. (This bit can be used as an additional command output line by installation of the appropriate strap.)
COM120:150	The four least significant bits are available to the user and are to be defined as needed.

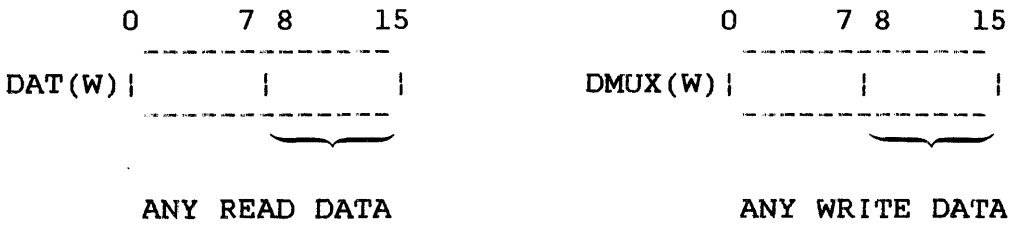
STATUS BITS	MEANING
STATUS INPUT LINES	Eight lines are extended from the user to monitor activity and to report this status when the processor requests it. Bits 12:15 are defined as busy, examine status, end of medium and device unavailable, respectively. The other four bits can be user-defined.

5.4 PROGRAMMING SEQUENCES

The ULI is structured so that it can be either byte- or halfword-oriented, depending upon whether it is programmed for byte or halfword mode. When the ULI is in the halfword mode, only read and write halfword instructions can be used for data transfers.

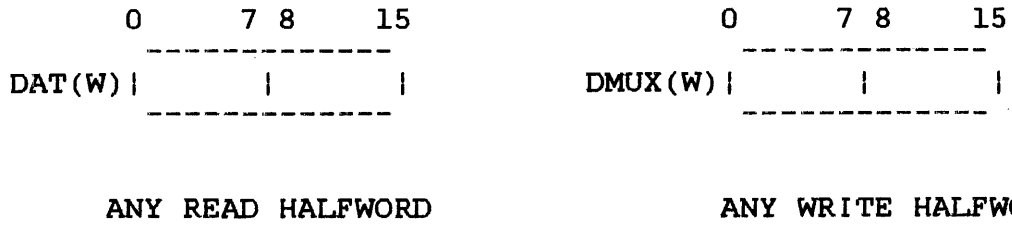
5.5 BYTE MODE

When the ULI is in the byte mode, all data is transferred between the ULI and the processor one byte at a time, over bits 8:15. Data is transferred between the ULI and the device a byte at a time, over bits 8:15.



5.6 HALFWORD MODE

When the ULI is in the halfword mode and halfword instructions are used, two parallel bytes of data are transferred between the ULI and the processor at the same time over bits 0:15.



ANY READ HALFWORD

ANY WRITE HALFWORD

5.7 INTERRUPTS

The interrupt queuing capability of the ULI can be altered by program control. Three different states can be obtained by the manipulation of command bits 8 and 9.

STATE	BIT 8	BIT 9
Enable	0	1
Disable	1	0
Disarm	1	1
No change	0	0

When the ULI interrupt logic is enabled, an interrupt can be queued in the ULI and sent to the processor.

When the ULI interrupt logic is disabled, an interrupt can be queued in the ULI but the interrupt is not sent to the processor until enabled.

When the ULI interrupt logic is disarmed, an interrupt cannot be queued or sent to the processor. Queued interrupts become reset.

5.8 INITIALIZATION

The ULI is initialized when the processor is powered up or when it is manually initialized by the INIT switch on the processor consolette. In the initialized state of the ULI, the interrupt logic is in the disarm state, the halfword mode is set and the ULI is not addressed.

5.9 DEVICE NUMBER

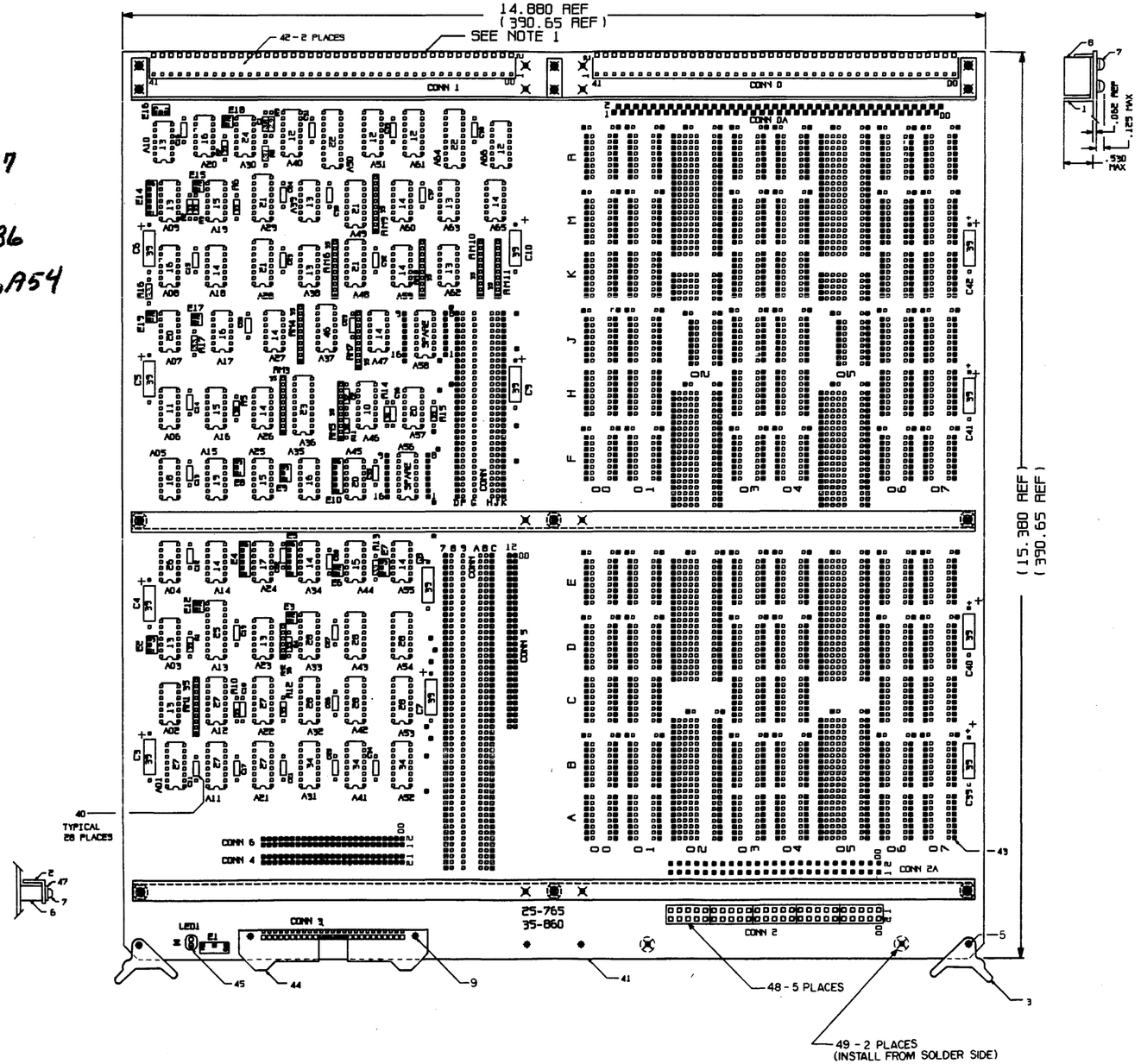
The ULI is normally assigned the device number X'8B', but this can be changed by changing the setting on the address DIP switch.

NOTES

1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
2. HEADER STIFFENER TO BE SOLDERED TO GROUND BUS AT TWO ENDS AND CENTER. (APP SIDE)
3. FOR BOARD IDENTIFICATION SEE SSP 002-OD.

19-320 = DS3487/mc3487
A1, A11, A12, A21, A22

19-321 = DS3486/mc3486
A32, A33, A42, A43, A53, A54



USED IN MANUAL 47-056

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV		
PROD	MJ	9-3-83

AREA E2, R8 WAS ITEM 29. ADDED ITEM 29 TO R9.
AREA L9,
ITEM 5 WAS ITEM 9. AREA G9, ITEM 9 WAS ITEM 5. AREA F6, IC A44 WAS ITEM 14.
ADDED ITEM NO. "3" TO RESISTORS R13, R16 & R17. ADDED ITEM NO. "38" TO CAP C1.

DB	XR	5505	M	12-9-83	R01

AREA J9 ADDED ITEM 48. 5 PLACES.
AREA L9, ADDED ITEM 49, 2 PLACES.

DB	XR	5558	M	12-9-83	R02

UNLESS OTHERWISE SPECIFIED

SCALE 1/1	TOLERANCE .XXX ± .005 .X ± .03 .XX ± .02 ANGLES 1°
DIMENSIONS IN INCHES	

NAME	TITLE	DATE
J.BIELSKIE	DES DFT	4-19-83
R.CERO	SUPV	
	CHK	
R.SCHMITT	ENG	
W.RICE	MGR	
R.BARKER	QC	

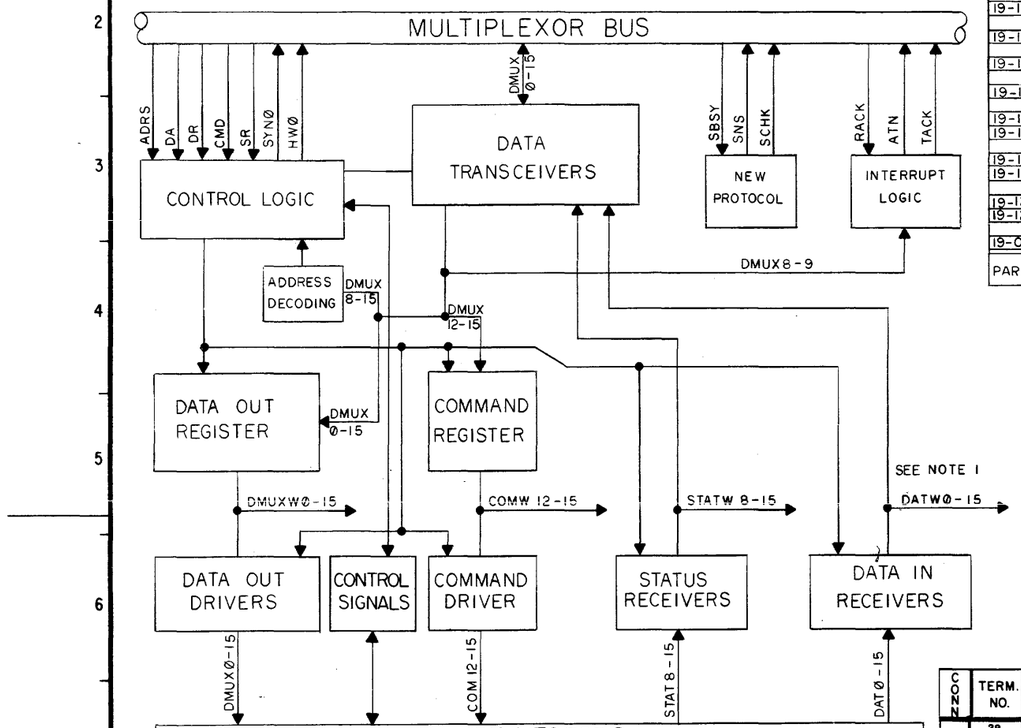
PERKIN-ELMER

OCEANPORT N.J. 07757

TITLE ASSEMBLY
UNIVERSAL LOGIC INTERFACE
(U.L.I.)

TASK 03114 SHT 1 - 1

DWG 35-860 R02 D03



ULI BLOCK DIAGRAM

PART NO.	REF DESIGNATION	SPARE OUTPUT NO.
19-160	A5	03
19-154	A16	04
19-165	A45	09
19-153	A18	03
19-159	A24	08,11
19-155	A35	06,08
19-154	A44	10
19-154	A19	08
19-153	A55	11
19-153	A34	08,11
19-125	A9	08,11
19-125	A3	11
19-042F01	A46	12

Cable

CABLE CONNECTOR MAP

CONN	TERM. NO.	ROW 2	ROW 1
MSB 4 & 6 IN	24	GND	GND
	23	STATN08Ø	STATP08Ø
	22	STATN09Ø	STATP09Ø
	21	STATN10Ø	STATP10Ø
	20	STATN11Ø	STATP11Ø
	19	STATN12Ø	STATP12Ø
	18	STATN13Ø	STATP13Ø
	17	STATN14Ø	STATP14Ø
	16	STATN15Ø	STATP15Ø
	15	DATN00Ø	DATP00Ø
	14	DATN01Ø	DATP01Ø
	13	DATN02Ø	DATP02Ø
	12	DATN03Ø	DATP03Ø
	11	DATN04Ø	DATP04Ø
	10	DATN05Ø	DATP05Ø
	09	DATN06Ø	DATP06Ø
	08	DATN07Ø	DATP07Ø
	07	DATN08Ø	DATP08Ø
	06	DATN09Ø	DATP09Ø
	05	DATN10Ø	DATP10Ø
	04	DATN11Ø	DATP11Ø
	03	DATN12Ø	DATP12Ø
	02	DATN13Ø	DATP13Ø
	01	DATN14Ø	DATP14Ø
	00	DATN15Ø	DATP15Ø
	24	GND	SATNØ
	23	RSTATNØ	SCLREØ
	22	CMDEØ	SREØ
	21	DAEØ	DREØ
	20	NPBUSYØ	GND
	19	COMN12Ø	COMP12Ø
	18	COMN13Ø	COMP13Ø
	17	COMN14Ø	COMP14Ø
	16	COMN15Ø	COMP15Ø
MSB 3 OUT	15	DMUXN000	DMUXP000
	14	DMUXN010	DMUXP010
	13	DMUXN020	DMUXP020
	12	DMUXN030	DMUXP030
	11	DMUXN040	DMUXP040
	10	DMUXN050	DMUXP050
	09	DMUXN060	DMUXP060
	08	DMUXN070	DMUXP070
	07	DMUXN080	DMUXP080
	06	DMUXN090	DMUXP090
	05	DMUXN100	DMUXP100
	04	DMUXN110	DMUXP110
	03	DMUXN120	DMUXP120
	02	DMUXN130	DMUXP130
	01	DMUXN140	DMUXP140
	00	DMUXN150	DMUXP150

MSB

CONN	TERM. NO.	ROW 1	ROW 2
5	29	DMUXW140	DMUXW150
	28	DMUXW120	DMUXW130
	27	DMUXW100	DMUXW110
	26	DMUXW080	DMUXW090
	25	DMUXW060	DMUXW070
	24	DMUXW040	DMUXW050
	23	DMUXW020	DMUXW030
	22	DMUXW000	DMUXW010
	21		
	20	SREØ	DAEØ
	19	CMDEØ	RSTATNØ
	18	DREØ	SCLREØ
	17	NPBUSYØ	SATNØ
	16	COMW14Ø	COMW15Ø
	15	COMW12Ø	COMW13Ø
	14		
	13		
2 & 2A	12	STATW14Ø	STATW15Ø
	11	STATW12Ø	STATW13Ø
	10	STATW10Ø	STATW11Ø
	09	STATW08Ø	STATW09Ø
	08		
	07	DATW14Ø	DATW15Ø (SA
	06	DATW12Ø	DATW13Ø
	05	DATW10Ø	DATW11Ø
	04	DATW08Ø	DATW09Ø
	03	DATW06Ø	DATW07Ø
	02	DATW04Ø	DATW05Ø
	01	DATW02Ø	DATW03Ø
	00	DATW000 MSB	DATW01Ø

DAT = IN
DMUX = OUT

BACK PANEL MAP

ROW 1	ROW 2	TERM. NO.	CONN
P5	GND	41	1
GND	GND	40	
		39	
		38	
		37	
		36	
		35	
		34	
		33	
		32	
		31	
		30	
	SNSBUSØ	29	
		28	
		27	
SCLRØ	HWØ	26	
	SCHKØ	25	
SNSØ	SBSYØ	24	
SYNØ	ATNØ	23	
RACKØ	TACKØ	22	
CL07Ø	DAØ	21	
DRØ	CMDØ	20	
SRØ	ADRSØ	19	
DMUX14Ø	DMUX15Ø	18	
DMUX12Ø	DMUX13Ø	17	
DMUX10Ø	DMUX11Ø	16	
DMUX06Ø	DMUX09Ø	15	
DMUX06Ø	DMUX07Ø	14	
DMUX04Ø	DMUX05Ø	13	
DMUX02Ø	DMUX03Ø	12	
DMUX000	DMUX01Ø	11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	0
GND	GND	40	
		39	
		38	
		37	
		36	
		35	
		34	
		33	
		32	
		31	
		30	
		29	
		28	
		27	
		26	
		25	
		24	
		23	
		22	
		21	
		20	
		19	
		18	
		17	
		16	
		15	
		14	
		13	
		12	
		11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
GND	GND	01	
P5	GND	00	

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

35-850 BOARD	R03 REV LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

STRAP	FROM	TO	SHEET	STRAP	FROM	TO	SHEET
				A2506	E9-3	NC	4
				A1513	E8-1	NC	4
				A2508	E8-3	NC	4
				A2509	E8-2	NC	4
				GND	E1-2	NC	2
				A1905	E1-1	NC	2
GND	E3-2	NC	7	GND	E16-3	NC	2
RECENB	E3-1	NC	7	GND	E18-2	NC	2
GND	E12-2	NC	4	CL07I	E18-1	NC	2
COM11	E12-1	NC	4	SNSØ	E16-1	E16-2	2
A1501	E9-1	NC	4	COM10I	E19-1	E19-2	2
A2505	E9-2	NC	4	HWENØ	E17-1	E17-2	2

STRAPPING TABLE

DESIGNATION	MNEMONIC	SHEET
E1-3	TSTCLRØ	2

TEST POINTS

REVISION	2	2	1	1	0	0	0
SHEET	1	2	3	4	5	6	7

USED IN MANUAL: 47-056

NOTES 1. ANY MNEMONIC ENDING WITH "W" IS A CONNECTION TO THE WIREWRAP SIDE.

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	Rdh	9/20/82

REVISED, SHTS 1, 2 & 4. AREA M9, BRD WAS R01.
DB | | 5505 | M | 12-02-83 | R01 |
SPARE GATE LIST, 19-154, A44, REMOVED PIN 12. AREA M9, BRD WAS R02. REVISED SHTS 1, 2 & 3.
DB | | 5558 | M | 12-3-83 | R02 |

19-320 = DS3487/MC3487
19-321 = DS3486/MC3486

8: 11 USER Defined STAT BITS
12: 15 Machine defined
12 - BSY
13 - EXA
14 - EOM
15 - DU

UNLESS OTHERWISE SPECIFIED

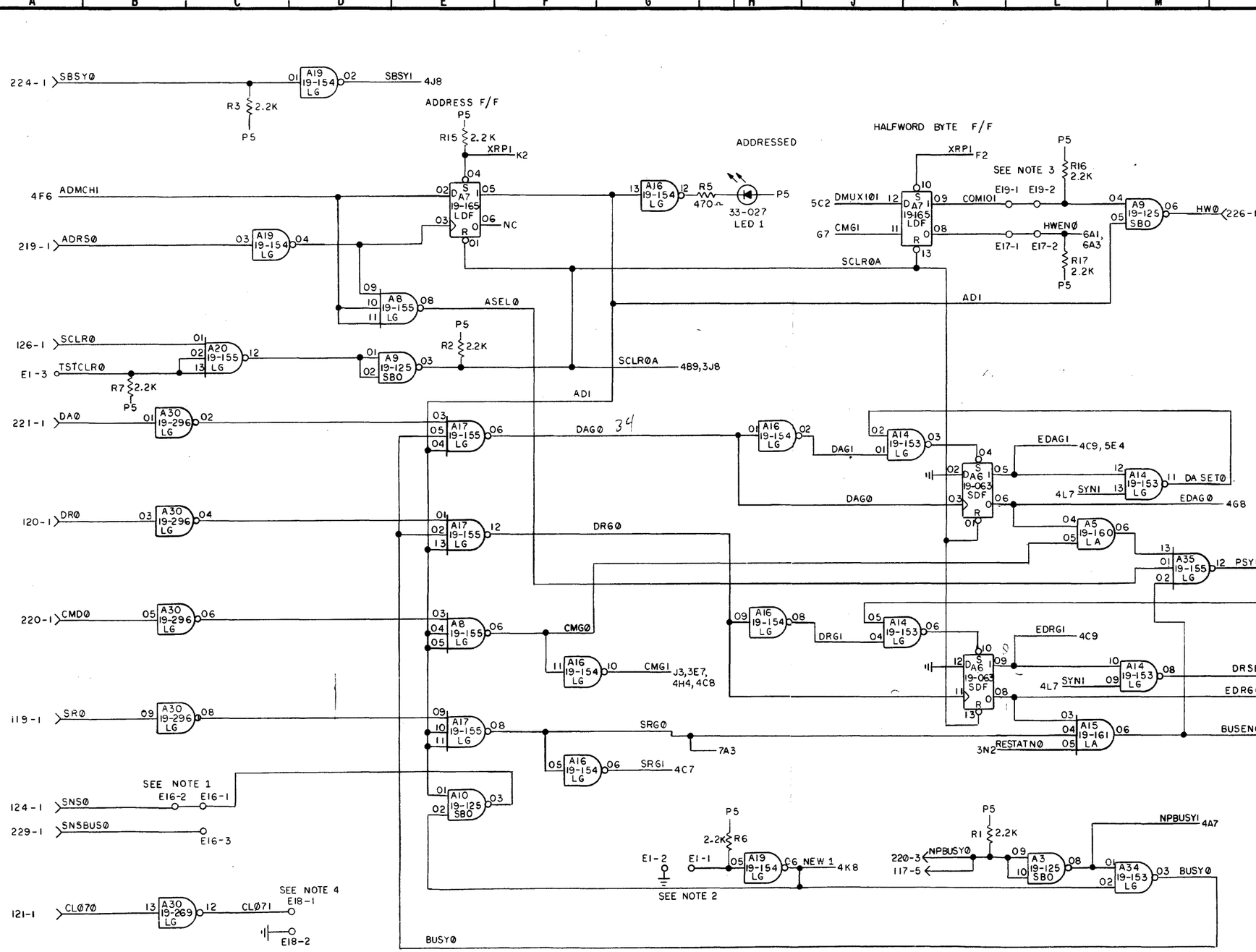
SCALE: NONE	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
J.R. BIELSKIE	E. JOHNSON	DES / DFT	6-20-83
R. CERO		SUPV	
		CHK	
R. SCHMITT		ENG	
W. RICE		MGR	
R. BARKER		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
UNIVERSAL LOGIC INTERFACE

TASK 03114
DWG 35-860 R02 D08
SHT 1-7



REVISIONS

IC'S A8-11, A17-10, A8-4 WERE CONNECTED TO A17-05 (AREA E4-E1). AREA F6, DELETED CROSS REF "4L4" FROM MNEMONIC CMG0.					
DB	AJ	5505	M	12-2-83	R01
IC A20-02 WAS CONNECTED TO IC A20-01 (AREA C4). AREA M8, ADD MNEMONIC "NPBUSY1".					
DB	AJ	5558	M	12-2-83	R02

NOTES

1. USE STRAP "E16-1 TO E16-3" IF A BUS SWITCH IS EMPLOYED AND DISCONNECT STRAP "E16-2 TO E16-1".
2. CONNECT STRAP "E1-1 TO E1-2" WHEN USING NEW PROTOCOL.
3. IF USING COMMAND BIT 10, REMOVE STRAPS "E19-1 TO E19-2" AND "E17-1 TO E17-2," GROUND PIN E17-1 IF A HALFWORD DEVICE OR GROUND PIN E19-2 IF A BYTE DEVICE.
4. OPTIONAL PIN FOR EARLY POWER FAIL.

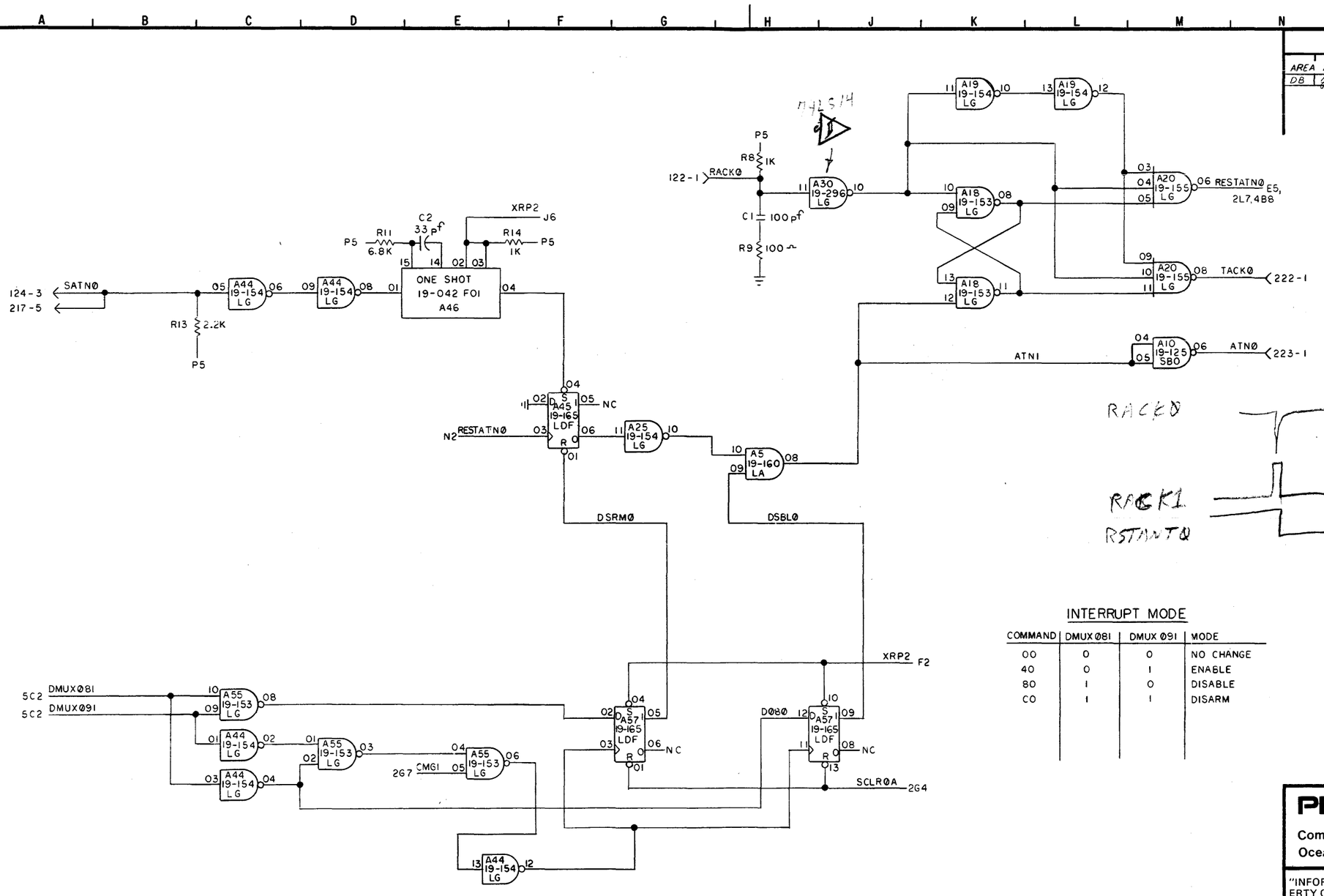
BRUNING 44-131 40579-2

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE
UNIVERSAL LOGIC INTERFACE

DRAFTER	E.JOHNSON
DATE	12-2-82
TASK	03114
DWG	35-860 R02 D08
SHT	2 - 7



INTERRUPT MODE

COMMAND	DMUX Ø81	DMUX Ø91	MODE
00	0	0	NO CHANGE
40	0	1	ENABLE
80	1	0	DISABLE
C0	1	1	DISARM

REVISIONS

AREA E8, ADDED GATE A44.					
DB	9/1	5558	M	12-3-83	R01

NOTES

DRAFTER: E. JOHNSON

DATE: 12-3-82

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE: UNIVERSAL LOGIC INTERFACE

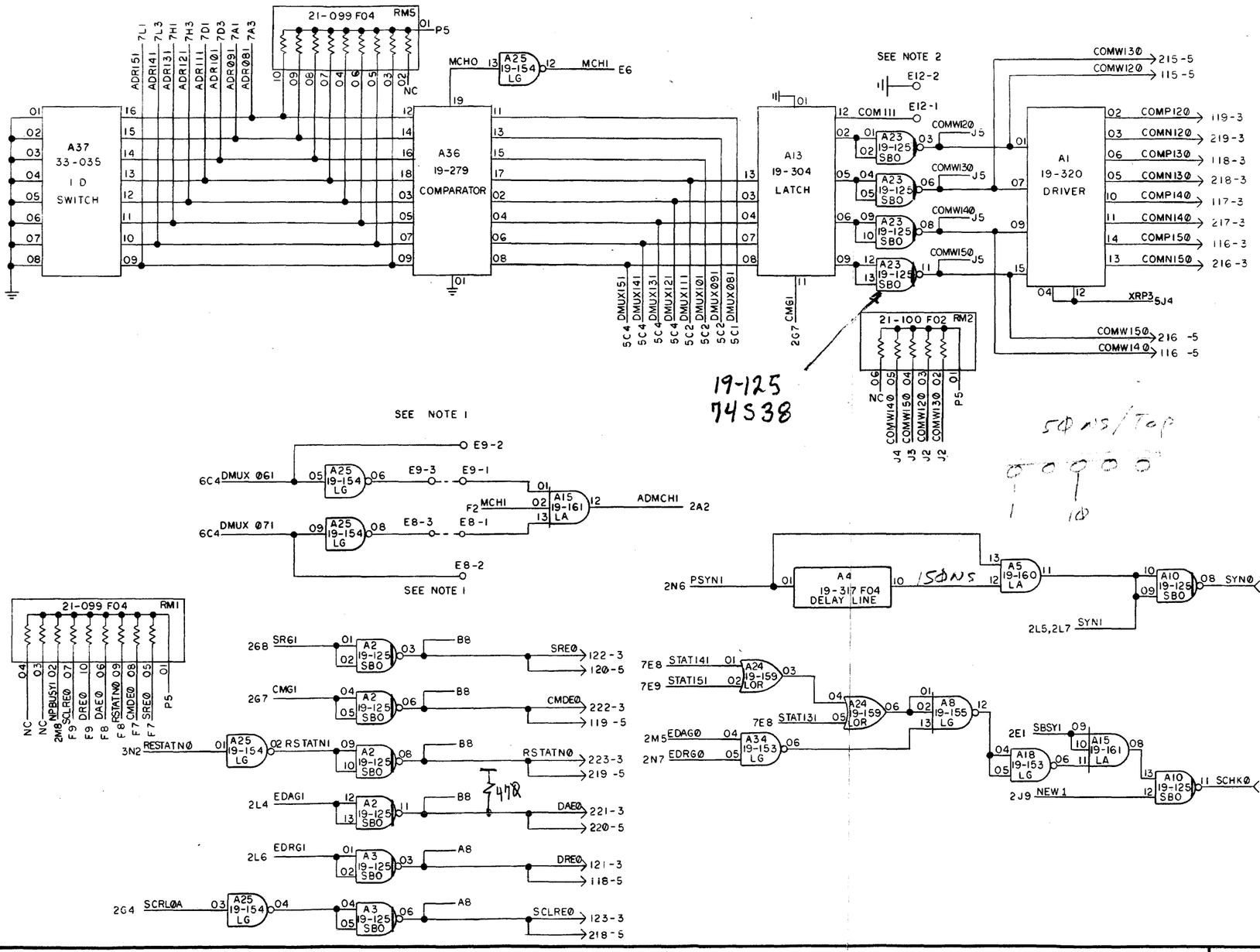
TASK 03114

DWG 35-860 R01 D08

SHT 3-7

19-125-74LS 38

REVISIONS					
AREA L4, IC A1-04, A1-12, MNEMONIC WAS "CMGØ" AND CROSS REF WAS "266". AREA H7, IC A4 WAS 19-317 F02.					
DB	JH	5505	M	12-2-83	R01



NOTES 1. DISCONNECT STRAPS "E9-1 TO E9-3" AND "E8-1 TO E8-3". CONNECT STRAPS "E8-1 TO E8-2" AND "E9-1 TO E9-2" WHEN USED UNDER A SCC.
2. EXTRA COMMAND BIT IF NEEDED.

PRINTING 44-131 40572

PERKIN-ELMER

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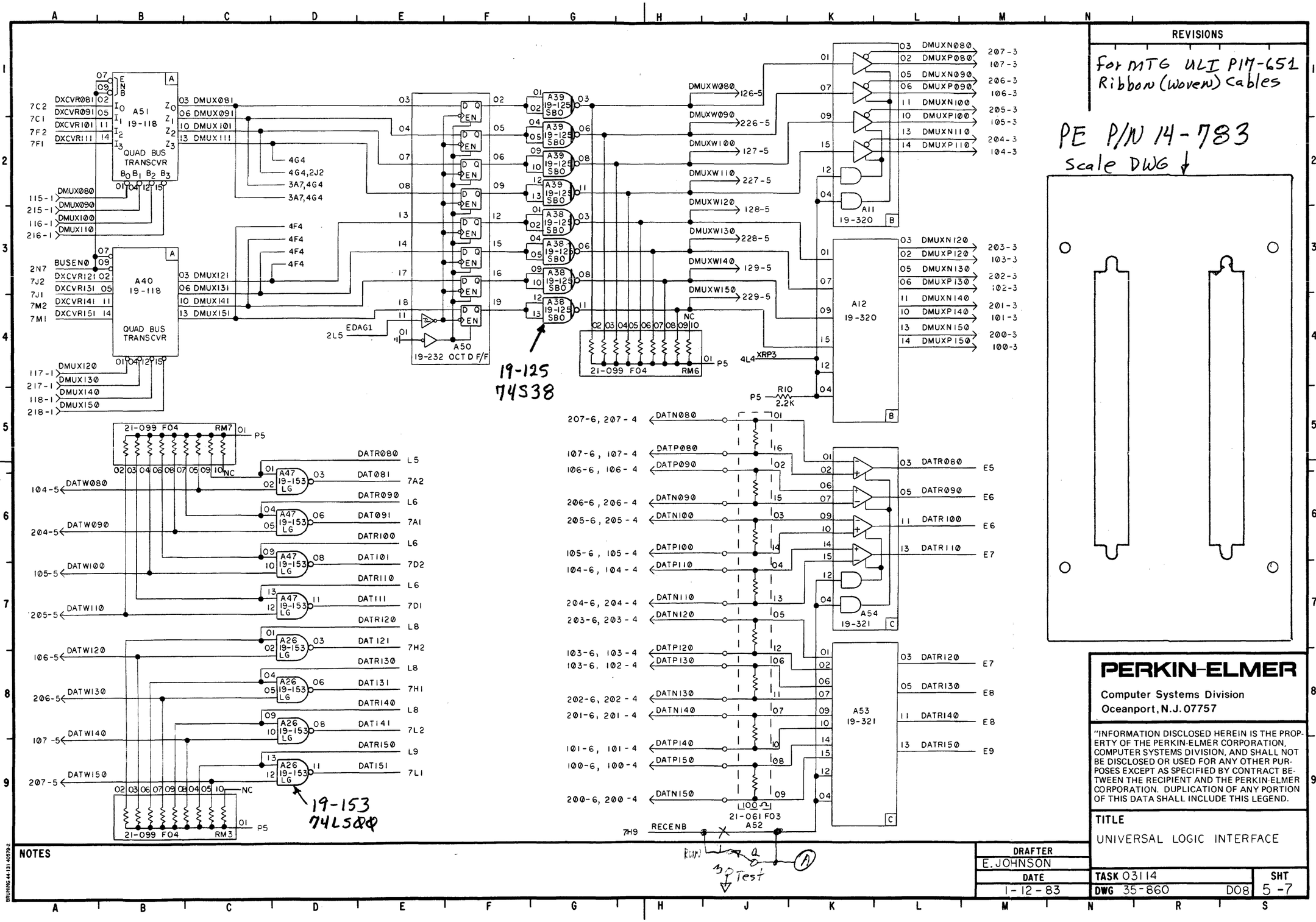
Oceanport, N.J. 07757

TITLE
UNIVERSAL LOGIC INTERFACE

DRAFTER	
E. JOHNSON	
DATE	
12-7-82	

TASK 03114
DWG 35-860R01 D08
SHT 4-7



NOTES

DRAFTER	E. JOHNSON
DATE	1-12-83
TASK	03114
DWG	35-860 D08
SHT	5-7

REVISIONS

For MTG ULI P17-651 Ribbon (woven) cables

PE P/N 14-783

Scale DWG ↓

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE

UNIVERSAL LOGIC INTERFACE

Run a 3P Test

REVISIONS

19-125
74538

2L3 HWEN0 07 09
E6 DAT001 02
E6 DAT011 05
E7 DAT021 11
E7 DAT031 14
E N B
I0 I1 I2 I3 A66 19-118 QUAD BUS TRANSCVR B0 B1 B2 B3
Z0 Z1 Z2 Z3
03 DMUX001
06 DMUX011
10 DMUX021
13 DMUX031
01 04 12 15
111-1 DMUX000
211-1 DMUX010
112-1 DMUX020
212-1 DMUX030

2L3 HWEN0 07 09
2N7 EDRG0
E7 DAT041 02
E8 DAT051 05
E8 DAT061 11
E9 DAT071 14
A61 19-118 QUAD BUS TRANSCVR
03 DMUX041
06 DMUX051
10 DMUX061
13 DMUX071
01 04 12 15
113-1 DMUX040
213-1 DMUX050
114-1 DMUX060
214-1 DMUX070

4C6
4C6
EDAG1
2L5
A64 19-232 OCT D F/F

A63 19-125 SBO
A62 19-125 SBO

DMUXW000 → 122-5
DMUXW010 → 222-5
DMUXW020 → 123-5
DMUXW030 → 223-5
DMUXW040 → 124-5
DMUXW050 → 224-5
DMUXW060 → 125-5
DMUXW070 → 225-5

02 03 04 05 06 07 08 09 10 NC
21-099 F04 RM10 01 P5

A22 19-320 B
A21 19-320 B
A42 19-321 C
A43 19-321 C

03 DMUXN000 → 215-3
02 DMUXP000 → 115-3
05 DMUXN010 → 214-3
06 DMUXP010 → 114-3
11 DMUXN020 → 213-3
10 DMUXP020 → 113-3
13 DMUXN030 → 212-3
14 DMUXP030 → 112-3
03 DMUXN040 → 211-3
02 DMUXP040 → 111-3
05 DMUXN050 → 210-3
06 DMUXP050 → 110-3
11 DMUXN060 → 209-3
10 DMUXP060 → 109-3
13 DMUXN070 → 208-3
14 DMUXP070 → 108-3

P5 R12 2.2K

215-6,215-4 DATN000
115-6,115-4 DATP000
114-6,114-4 DATP010
214-6,214-4 DATN010
213-6,213-4 DATN020
113-6,113-4 DATP020
112-6,112-4 DATP030
212-6,212-4 DATN030
211-6,211-4 DATN040
111-6,111-4 DATP040
110-6,110-4 DATP050
210-6,210-4 DATN050
209-6,209-4 DATN060
109-6,109-4 DATP060
108-6,108-4 DATP070
208-6,208-4 DATN070
100Ω 21-061 F03 A41
7H9 RECENB

03 DATR000 E5
05 DATR010 E6
11 DATR020 E6
13 DATR030 E7
03 DATR040 E7
05 DATR050 E8
13 DATR060 E8
11 DATR070 E9

21-099 F04 RM11 01 P5
02 03 04 05 06 07 08 09 10 NC

100-5 DATW000
200-5 DATW010
101-5 DATW020
201-5 DATW030
102-5 DATW040
202-5 DATW050
103-5 DATW060
203-5 DATW070

A65 19-153 LG
A60 19-153 LG

DATR000 L5 DAT001 A1
DATR010 L6 DAT011 A2
DATR020 L6 DAT021 A2
DATR030 L6 DAT031 A2
DATR040 L8 DAT041 A3
DATR050 L8 DAT051 A4
DATR060 L8 DAT061 A4
DATR070 L9 DAT071 A4

19-153
74LS00

21-099 F04 RM9 01 P5

NOTES

DRAFTER	E. JOHNSON
DATE	1-12-83

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
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TASK 03114 | SHT 6 - 7
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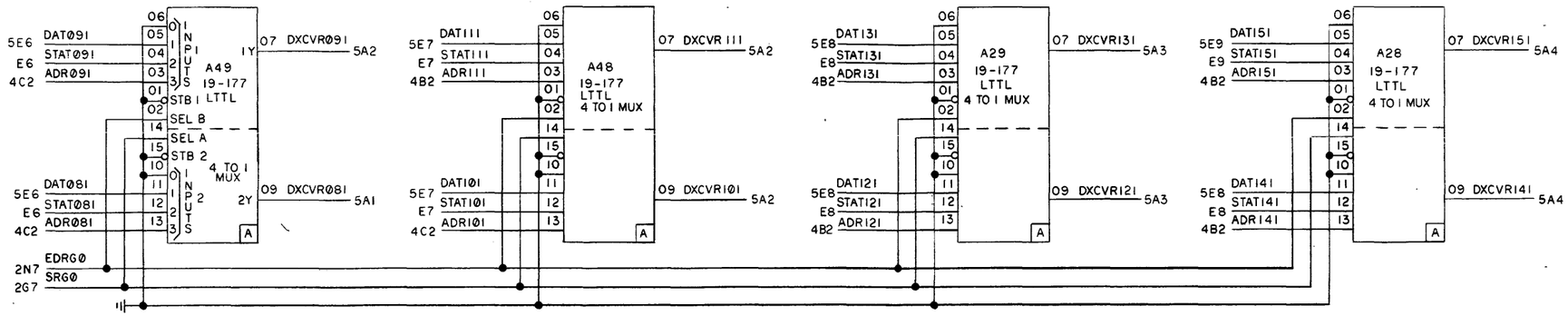
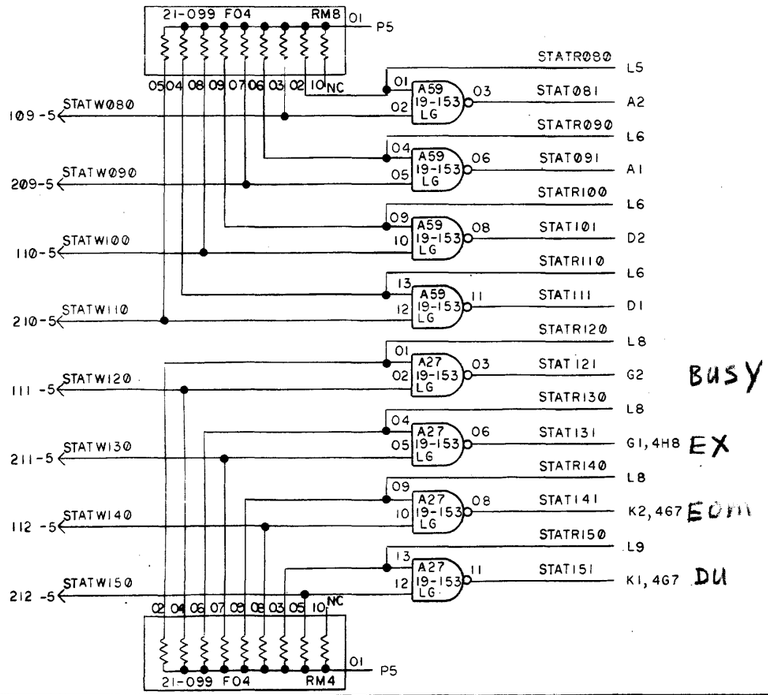
REVISIONS

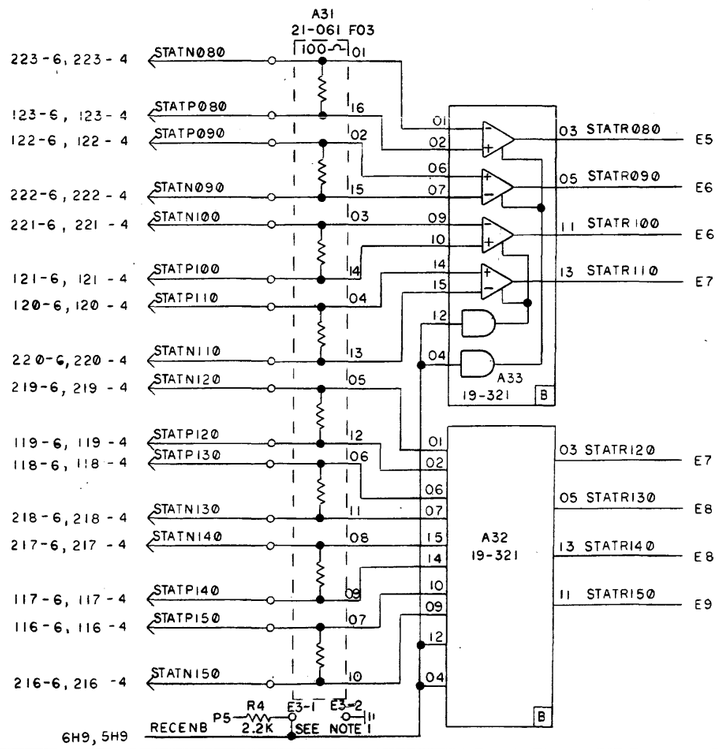


MULTIPLEXOR STATE TABLE

EDRG0	SRG0	OUT
0	0	GND
0	1	DATA
1	0	STATUS
1	1	ADDRESS



BUSY
EX
EOM
DU



NOTES 1. WHEN USING WIRE WRAP SIDE DISABLE RECEIVERS BY STRAPPING "E3-1 TO E3-2"

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