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METRIC

M47·102
PROGRAMMABLE
ASYNCHRONOUS SINGLE LINE ADAPTER
(PASLA)

MAINTENANCE MANUAL

Consists of:

Installation Specification	02-279R02A20
Maintenance Specification	02-279R02A21
Schematic	02-279R05D08
Component Locator	35-457M01R04D03

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02-279R02A20
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METRIC

M47·102 PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER (PASLA) INTERFACE · 178MM x 381MM (7"x15") INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-279 PASLA Interface (Product Number M47-102). The 35-457 halfboard must be attached to a blank halfboard (Perkin-Elmer 16-398 Halfboard Kit) or an active halfboard in order to be installed in a chassis designed for 381mm x 381mm (15" x 15") PC boards. The PASLA Interface may be in either the right or left half position, as required. See Figure 1.

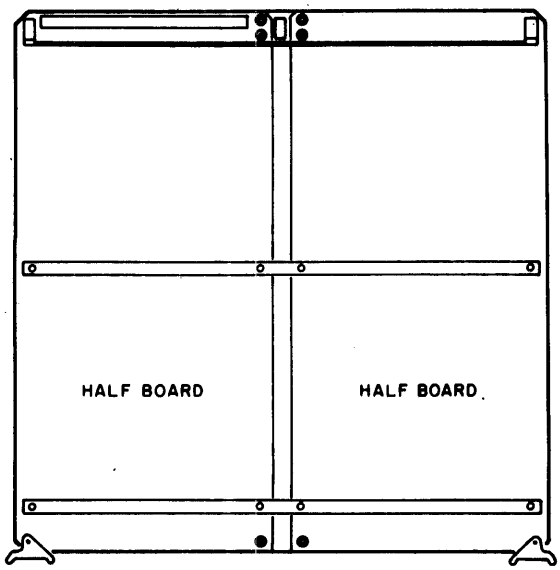


Figure 1. Halfboard Assembly

2. INSTALLATION

2.1 Unpacking

When the PASLA Interface is shipped with a system, it is installed at the factory. Therefore, no special unpacking procedure is required. It is only necessary to insure that the module is properly seated in its connector. If the module assembly is purchased separately, it should be unpacked carefully and inspected for damage prior to installation.

2.2 Location

The 35-457 PASLA Interface halfboard, strapped to a blank or active halfboard, may be installed in any I/O slot. After installing the module, remove the RACK0/TACK0 strap located on the back panel between Terminals 222 and 122 of the selected slot.

2.3 Cable Connections

The 17-197 Cable (included) is connected between the cable connector at the end of the mother board and the cable entry panel.

3. ADJUSTMENTS

The baud rate is selected by means of a potentiometer adjustment and a strap option. This procedure is described in the 02-279A21 PASLA Maintenance Specification provided in the PASLA Maintenance Manual, Publication Number 29-301. This is pre-set at the factory and should not require re-adjustment for normal installations. If, however, it becomes necessary to select a different baud rate, the user is cautioned to use a precision frequency-measuring device for the set-up. Failure to do this results in reduced receive data distortion tolerance and increased transmit data distortion. Section 6 of the 02-279A21 PASLA Maintenance Specification shows the procedure for baud rate selection and adjustments.

The PASLA is normally strapped for 300/1200 baud, HDX operation. The preferred address is X'10'.

4. STRAP OPTIONS

4.1 HDX - Strap G5 to 7 and HD to G4. FDX - Strap 7 to 8 and remove HD to G4, and G5 to 7.
4.2 BAUD RATE - See Tables 2 and 3 in 02-279A21.
4.3 Disable CARR Status - Strap CF to G0.
Disable DSRDY Status - Strap CC to G2.
Disable CL2S Status - Strap CB to G3.

02-279R02A21
February 1976

METRIC

M47·102 PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER (PASLA) MAINTENANCE SPECIFICATION

1. INTRODUCTION

The Programmable Asynchronous Single Line Adapter (PASLA) provides an interface between the Multiplexor Bus of an Perkin-Elmer Digital System and a variety of Half-Duplex (HDX) or Full-Duplex (FDX) asynchronous data sets or local terminals. The system conforms to the RS-232C interface specification and may be programmed for a variety of baud rates and character formats.

Data transfers between the data set and adapter are bit serial at a baud rate selected under program control. The adapter contains circuits to generate and detect the control signals required to set up, take down, and supervise the data communications channel, and to provide proper status and interrupt information to the Processor.

The PASLA is contained on a single 178mm x 381mm (7" x 15") PC board.

2. SCOPE

This specification covers the normal asynchronous operation of the system. It does not describe specific communication techniques since the system is transparent to valid characters passing through it.

3. BLOCK DIAGRAM ANALYSIS

The Block Diagram for the Programmable Asynchronous Single Line Adapter is shown on Sheet 0 of Functional Schematic 02-279D08.

The oscillator is adjustable and provides the baud rates for the PASLA. Two bauds are selected via a strap option and one of these two may be selected under program control.

The PASLA includes an MOS/LSI device, the Universal Asynchronous Receiver/Transmitter (UART), which provides character status and character assembly/disassembly. The Character Format Register in the UART may be programmed to provide one or two Stop Bits, odd, even, or no parity, and five through eight data bits/character.

The Clock Select Register is programmed to select one of the two baud rates which are available. The selected baud rate is an input to the UART, and is used to serialize the character to the data set when transmitting, and to de-serialize the character from the data set when receiving.

The UART is conditioned to transmit as follows: A Command is given to set up the proper character format in the UART. At this time, BUSY is zero. The BUSY Status Bit is an output from the UART and indicates to the Processor when another character can be loaded. This Command is followed by a Write Data to load the character into the UART Transmit Data Register. The UART appends the Start Bit, the programmed parity, and one or more Stop Bits, and then transmits the character. Data transmissions continue with the same character format until the Write Data instructions are terminated.

Since the UART is a Full-Duplex (FDX) device, characters may be received while simultaneously transmitting. The UART has a separate BUSY Status Bit for the Receiver. This BUSY is active until the UART has assembled a character. At this time, the BUSY drops and the character may be read into the Processor with a Read Data. The programmed character format is applicable to both the Transmitter and Receiver in the UART.

The UART has three status bits associated with the Receiver. These are Parity Fail, Overflow, and Framing Error. These are updated immediately before BUSY drops on the Receive side. The Processor may interrogate these status bits with a Sense Status instruction.

The RS-232C Transmitters/Receivers provide the logic level conversion between the DTL/TTL levels and the bipolar levels required by the data set.

The following is a sequence for establishing a connection, transferring data, and disconnecting the call in the HDX Mode over the switched network.

A call may be initiated when an operator at a remote data set dials the number of the data set connected to the local PASLA. This causes the RING lead to become active. The Processor may detect this by either acknowledging the RING interrupt from the PASLA (assuming interrupts are enabled) or by sensing status to determine when RING is active. In either case, the Processor should respond with an Output Command to set DTR in the MODEM Command Register. This causes the call to be answered (Ring terminates), and, if the local data set is in the DATA Mode, it responds with DATA SET READY to the adapter. Again, DATA SET READY status may be determined with a Sense Status instruction. If the adapter is to transmit first, the Processor responds by activating RQ2S in the MODEM Command Register. The local data set returns CL2S after a short delay. With CL2S on, the call is established and handshaking is complete. The adapter may now transmit to the remote terminal. The Processor may now load the UART with the proper character format and load the CLOCK SELECT with the baud rate selection. This should be followed by a series of Write Data instructions. The Write Data loads the Transmit Data Register. The UART then shifts the data serially to the local data set. Data transmission continues until the Processor terminates the Write Data instructions.

For data transfers in the Receive Mode, the call set-up is the same except that the Processor leaves the RQ2S lead OFF. This causes CL2S from the local data set to also remain OFF. The PASLA is now ready to receive characters. Each character is preceded by a Start Bit. When the UART detects this bit, it shifts the serial data into the Receive Data Register. When a complete character has been assembled, the BSY status bit drops causing an interrupt, if enabled.

As each character is being assembled, the presence of the Stop bit and correct parity is determined. These are compared with the programmed number of Stop bits and parity. If an error is detected, one or more appropriate status bits are set.

In FDX operation, data transfers may occur in both directions simultaneously. This requires changing the HDX/FDX straps.

4. FUNCTIONAL SCHEMATIC DESCRIPTION

The multiplexor bus interface is shown on Sheet 1 of 02-279D08. Only the seven most significant bits are input to the address strap circuit since the PASLA must respond to two consecutive addresses. The BADD flip-flop in location 1H7 is set if either the Transmit or Receive side is addressed; in addition, ODD is set for the transmit mode.

A Status Request is steered to the Send or Receive side with the gates in location 1D1 when BADD is set. The SSRGO (Send Side) is active in HDX operation when the WRT flip-flop is set or when ODD is set in FDX operation. Similarly, the RSRGO (Receive Side) is active when WRT is reset in the HDX mode or when ODD is reset in FDX.

The R/S SRGO enables the 4/1 multiplexors on Sheet 3 and also selects the appropriate set of inputs. Note that the Reverse Channel (RCR), Ring, and EX status bits are inhibited on the Send Side by STINH. The resulting status byte agrees with the description in the PASLA Programming Manual, 29-446.

4.1 Commands

The PASLA Programming Manual, Publication Number 29-446, shows the Command and Status byte assignments for the PASLA. The Commands are decoded in location 1D8. Note that there are two commands, CMGA and CMGB. The CMGA command is used to set up the Modem Command Register on Sheet 2 and CMGB sets up the character format, and selects the Baud Rate. The CMG lines are enabled by the BADD flip-flop and CMGA and CMGB are determined by the state of the D15 line. If D15=1, CMGA is active. If D15=0, CMGB is active.

The CMGA command sets up the five bit Modem Register. The EPLEX (Echoplex) flip-flop controls the Transmit Data Line to the data set as shown in location 2K6. If EPLEX=1, the data received from the data set on the RDATA line is returned to the data set on the TDATA line. When EPLEX=0, the data from the UART is transmitted in the data set. The RCT (Reverse Channel Transmit) flip-flop is gated directly to the data set through the RCT transmitter. RCT is a secondary low speed signal path which is optional on some HDX data sets. The TLB (Transmit Line Break) inhibits the TDATA line to the data set. If TLB=1, it causes a permanent space or line break to be transmitted to the data set. The DTR (Data Terminal Ready) is a signal to the data set which permits an incoming call to be answered, and also keeps an existing connection up. The WT (Write) queues a request to put the line in the Transmit (WT=1) or Receive (WT=0) Mode.

The CMGA0 command is OR-tied with D14 to produce SCMG1 or RCMG1 which sets up the ENABLE/DISABLE for the Receive and Send side of each line. The RCMG1 signal toggles the REN (Receive Enable) flip-flop at location 5B6 if D14=0, which selects the Receive Mode. Similarly, SCMG1 toggles the SEN (Send Enable) flip-flop if D14=1 which selects the Transmit Mode. The K input to these JKs is D091 and the J input is D081. This provides the standard Enable/Disable function. Note that there are other hardware functions which affect interrupt enable/disable. These are discussed in the section on the Interrupt Circuit.

As mentioned earlier, CMGB selects the baud rate and character format. The baud rate selection is shown in location 2H1. The CLKSL flip-flop enables one of the two gates in location 4E5 which selects the clock strapped to input J1 or K1. The selected clock is 16 times the desired baud rate which is required by the 19-081. The output, CLK1, is strapped to TCLK1 and RCLK1 in normal operation.

The CMGB command also loads the character format into the Universal Asynchronous Receiver/Transmitter (UART) as shown on Sheet 4. The CMGB1 command loads the inputs on Pins 35 through 39 into the register. This register controls the number of Stop Bits, the Character length, and Parity for both the Receive and Transmit sections of the UART. This is shown in Table 1. Note that one Start Bit is generated for any character format.

TABLE 1. CHARACTER FORMAT

DATA INPUTS (D_ _)					CHARACTER FORMAT			
10	11	12	13	14	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	1	0	0	1	5	ODD	2
0	0	0	0	1	1	5	EVEN	1
0	0	1	0	1	1	5	EVEN	2
0	0	0	1	x	1	5	NONE	1
0	0	1	1	x	1	5	NONE	2
0	1	0	0	0	1	6	ODD	1
0	1	1	0	0	1	6	ODD	2
0	1	0	0	1	1	6	EVEN	1
0	1	1	0	1	1	6	EVEN	2
0	1	0	1	x	1	6	NONE	1
0	1	1	1	x	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	1	0	0	1	7	ODD	2
1	0	0	0	1	1	7	EVEN	1
1	0	1	0	1	1	7	EVEN	2
1	0	0	1	x	1	7	NONE	1
1	0	1	1	x	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	1	0	0	1	8	ODD	2
1	1	0	0	1	1	8	EVEN	1
1	1	1	0	1	1	8	EVEN	2
1	1	0	1	x	1	8	NONE	1
1	1	1	1	x	1	8	NONE	2

4.2 Universal Asynchronous Receiver/Transmitter (UART) Operation

The UART is a 40 pin MOS/LSI device which has TTL/DTL compatible inputs and outputs. The Control section of the UART directs both the Transmitter and Receiver sections. The Control Register is loaded with CMGB1 positive pulse. This pulse must be ≥ 250 nanoseconds. This selects a character format as defined in Table 1. The Control Register should not be changed while a character is being transferred.

The Control section also has an SCLR input (Pin 21). This resets internal registers and also insures that the serial output, TDATA1, from the Transmitter is high.

The Transmitter section provides parallel to serial conversion and generates Start and Stop bits and also Parity, if selected. The Transmitter contains a double character buffer. Each of these registers has a Busy indicator which is generated within the UART. If the Transmitter Buffer Register is empty, BUFE1 is high, and if the Transmit Shift Register is empty, EOT1 is high.

When BUFE=1, the Processor may issue a Write Data which causes DAG0 to go low. This parallel loads the Buffer Register and also causes BUFE1 to go low (BSY=1). If the Transmit Shift Register Busy bit, EOT, is high, this character is immediately loaded into the Shift Register, then EOT goes low (BSY=1), and the Buffer Register Busy goes high (BSY=0). At this time, the Processor may load another character. Note that logic within the UART automatically loads the Shift Register at the correct time. See Figure 1 for the transmitter timing diagram.

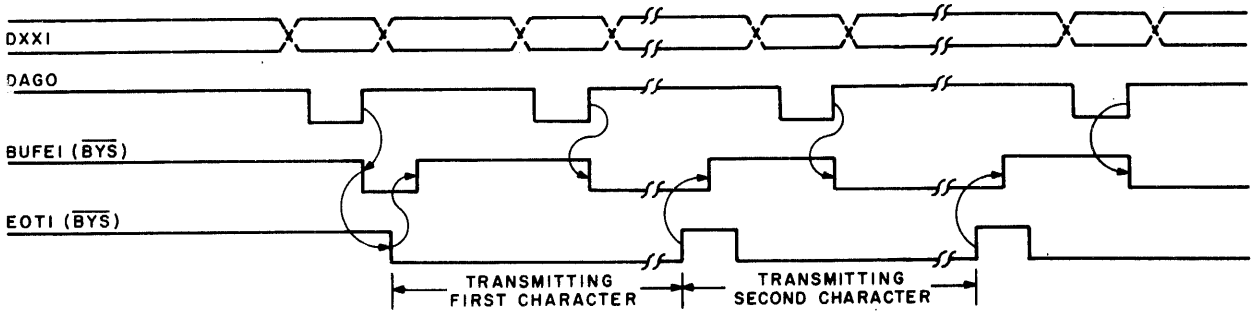


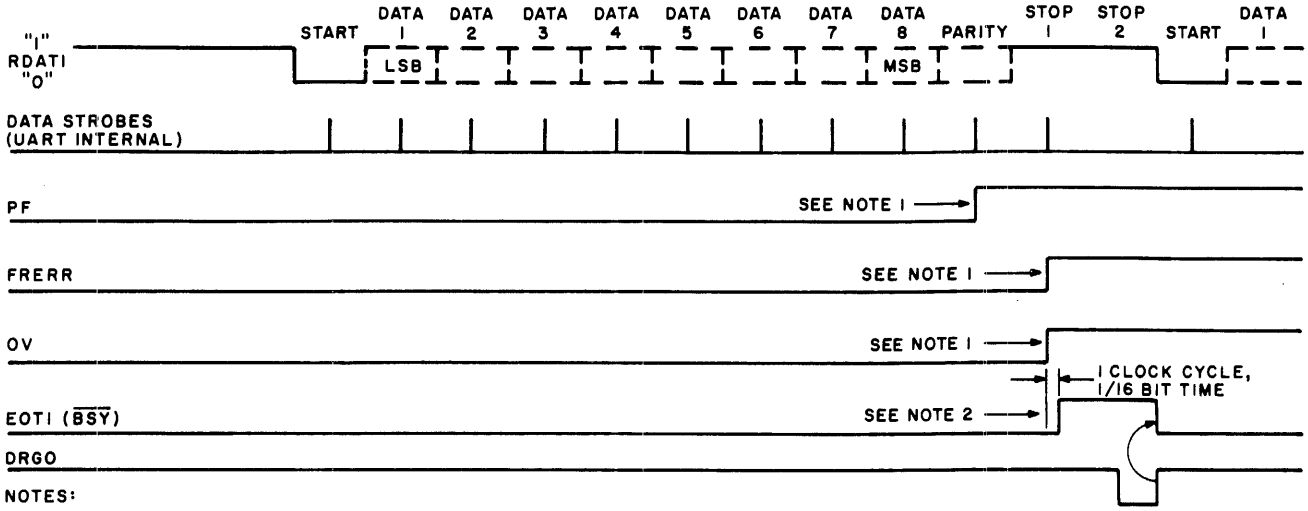
Figure 1. UART Transmitter Timing

The Receiver section of the UART performs the serial to parallel conversion on received characters and also tests Parity, Stop, and Start bits. The EOCI output from the Receiver is the Busy indicator. A hi is BSY=0. The timing for a received character is shown in Figure 2.

The Received Data is input to Pin 20 of the UART. This input is normally a high (binary 1). When this line has a 1→0 transition, the UART starts an interval timer which samples the data at the middle of a bit cell. (The first bit received is always a Start bit which should be in the logic 0 state for one bit time.) If the input is logic 1 at the sample time, the UART assumes a noise condition and returns to the Idle state. If the line is still low at the sample time, the Receiver assembles the character. The received parity is compared with the programmed parity, and, if they differ, the UART raises the PF (Parity Fail) status bit. In addition, the Receiver tests the first Stop bit. If this is a logic 0, the UART sets the FRERR (Framing Error) status bit. After the complete character is assembled, the Receiver tests to see if the previous character had been read by the Processor; if not, the UART sets the OV (Overflow) status bit. The Receiver then loads the assembled character into the Receiver Data Register. This causes EOC=1 (BSY=0). The Processor may then give a Read Data to read the assembled character. Note that the received character is right-justified with unused bits forced to logic 0. This includes Parity and Stop bits. When the Processor executes the Read Data, the receiver busy condition, EOC1 goes low (BSY=1) until another character is assembled.

The status bits PF and FRERR are only reset when another character is received. The OV bit and EOC are reset only with System Clear or when a Read Data is issued.

The status and parallel data outputs from the UART are tri-state and assume the high impedance output when the Status Register or the Receiver Data Register is not enabled. In this application of the UART, both registers are always enabled with the ground on Pins 4 and 16.



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE DETECTED, IF ERROR OCCURS.
2. EOTI IS SET ONLY WHEN THE RECEIVED DATA, PF, FRERR, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS.
3. ALL INFORMATION IS GOOD IN OUTPUT REGISTER UNTIL EOTO TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE, PARITY AND TWO STOP BITS. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL CODE LEVELS, THE DATA IN THE HOLDING REGISTER IS "RIGHT JUSTIFIED".

Figure 2. UART Receiver Timing

4.3 Interrupt Circuit

The Interrupt Circuit on the PASLA contains hardware to enable/disable each side of the line independently and also to detect interrupt conditions associated with BSY and the data communications channel.

The interrupt sources are shown at the left of Sheet 2 and the right of Sheet 4 and are a function of HDX or FDX and also the Transmit or Receive Mode. A further system constraint is that in HDX operation, if an interrupt is detected on either the Transmit or Receive side, the address of the Receive side is always returned.

The SINT00 one-shot in location 4N4 provides an interrupt when Busy on the Transmit side of the line drops. For the Transmit side, Busy is defined as TBSY=$\overline{\text{DSRDY}}$ + $\overline{\text{CL2S}}$ + $\overline{\text{BUFE}}$ + $\overline{\text{WT}}$. Normally, when a telecommunications link is established in the Transmit Mode, DSRDY, CL2S, and WT are all active (high). This means that TBSY follows the Busy status from the UART (BUFE).

The RINT one-shot in location 4N5 provides an interrupt when a character is assembled if DSRDY=1. In this case, RBSY1 goes low to fire the RINT one-shot.

The R/S ATN0 flip-flops in Location 5K7 are set when an interrupt occurs on the Receive and Send sides respectively. The R/S EN flip-flop inhibits the outputs of the RATN and SATN interrupt flip-flops respectively.

In FDX operation, the REN flip-flop is programmed set or reset only if the Command byte (CMGA) has Bit 14=0. Similarly, the SEN flip-flop is programmed set or reset if CMGA has Bit 14=1. Since Bit 14 is the Write/Read selection, this permits enable/disable for the selected mode.

In HDX operation, if the line is in the Transmit Mode, RATN is forced reset with the gate in location 5H7. Similarly, SATN is forced reset when in the Receive Mode in HDX operation. This has the effect of disarming the unused half of the line.

The gates at the left of Sheet 2 steer the interrupt condition to the correct ATN flip-flop depending on HDX or FDX operation. The gate in location 2A5 sets RATN if CARRIER changes state or if Receive Busy drops. The gate in location 2E8 sets RATN if REVERSE CHANNEL changes state, DSRDY drops, or if RING goes to a logic 1. This also sets SATN in HDX operation. Note that only one of the flip-flops, RATN/SATN, gets set in HDX since the unused side is disarmed. The gate in location 2G8 sets SATN when Transmit Busy or CL2S drops.

The gates on the toggle inputs of RATN and SATN are part of a priority circuit which steers the RACK from the Processor to the correct ATN flip-flop. In FDX operation, when both the RATN and SATN flip-flops may be set, this circuit guarantees that the RATN is serviced first.

When the SATN is being serviced, the SATSYN1 toggle input appears as the least significant bit of the interrupt return address, 3N5. This high insures that the odd address (for the send side) is returned. Note that in HDX operation, this least significant bit is grounded to insure that the address of the receive side (even) is returned, as required.

4.4 RS-232 Interface

The Data Set Interface is shown on Sheet 2. This is an interface between the bipolar RS-232C signals and the DTL/TTL circuits on the board. The RS-232C specification defines the interface lines and also specifies the electrical characteristics of these lines.

The important parts of this specification are described in the following paragraphs.

The RS-232C specification classifies all interface lines as either Signal or Control. The Signal lines are the data paths; i.e., Receive Data (RDATA), Transmit Data (TDATA), Reverse Channel Receive (RCR), and Reverse Channel Transmit (RCT). The logic conditions on these signal lines are described as being in the MARK condition or SPACE condition. See Figure 3.

NOTATION	NEGATIVE (BINARY 1)	POSITIVE (BINARY 0)
SIGNAL LINE	MARK	SPACE
CONTROL LINE	OFF	ON

Figure 3. RS-232 Interface Lines

The Control lines convey information to control the state of the telecommunications link and to also indicate the status of the connection. These lines are Data Set Ready (DSRDY), Ring, Carrier (CARR), Request to Send (RQ2S), Clear to Send (CL2S), and Data Terminal Ready (DTR). The logic conditions on these lines are described as being in the ON or OFF condition as shown in Figure 3. Figure 4 shows the RS-232C Electrical Specifications.

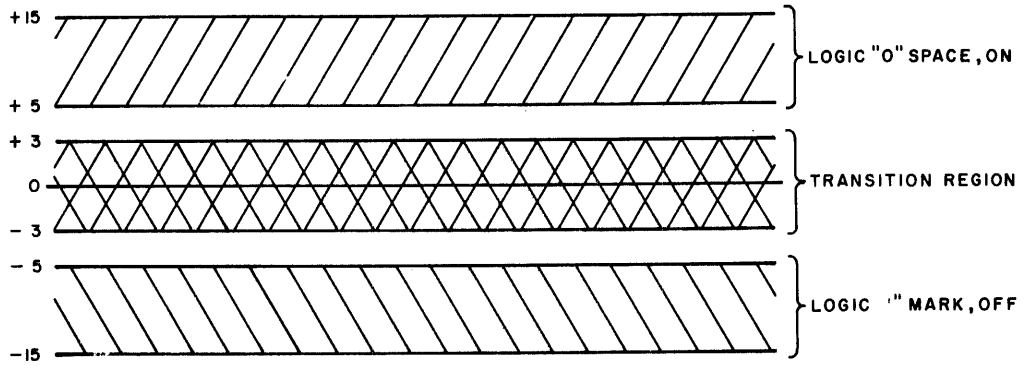


Figure 4. RS-232C Voltage Specification

The RS-232 Transmitters used on the PASLA have a ±12V power supply. This causes the outputs to swing between approximately +10V and -10V. The Transmitters (19-046) are inverting. A high input (+5) results in a negative output. A ground on the input results in a positive output. The Receivers, 19-047, are also inverting.

4.5 Logical Sequence for the Transmit Mode

In order to transmit to a data set, the character format and baud rate must be loaded via an Output Command and the correct mode must be selected with another Output Command.

An Output Command with D15=1 loads the Quad Latch on Sheet 2 to select the mode. For transmitting, this typically sets WT and DTR. When WT is set, WRT is forced set.

The DTR causes the DATA TERMINAL READY signal to the data set to turn ON. If the data set is ready to transfer data, it responds with DATA SET READY. This causes DSRDY1 in location 2F3 to go high which returns RQ2S to the data set since the WRT1 line is high. The data set then responds with CLEAR TO SEND (CL2S1) which indicates that the data set is ready to receive data from the adapter. This completes the handshaking which is required to establish the telecommunications link.

When CL2S goes active, SINT is generated in location 4R4. This is an interrupt source. All of the inputs to the gate at the input of the SINT one-shot are normally high when the CL2S 0 → 1 transition occurs. Note that this forces TBSY=0.

With TBSY=0, a Write Data may be issued to load the first character. The trailing edge of the DAG0 loads the character into the UART and also sets BUFE=0 which forces the TBSY1 high. Refer back to Figure 1. Since the Transmit Shift Register in the UART is empty, this character is immediately loaded into the Shift Register. This causes EOT1 to go low (Shift Register Busy) and BUFE1 to go high (Buffer Register not Busy). The latter generates an interrupt and the Processor may load another character.

The serial data from the UART (TDATA1) contains the Start bit, data bits, Parity and Stop Bits in that order. Serial data TDATA1 is gated to the data set (2C5) provided that the Modem Command Register has EPLEX and TLB reset. If TLB=1, the Transmit Data is forced into a permanent SPACE Condition. If EPLEX=1 and TLB=0, the serial data from the data set is transmitted directly back to the data set and TDATA1 is inhibited.

Character transfers continue as outlined above until the Write Datas cease. After the last Write Data, the UART finishes transmitting the last character and then puts the TDATA1 line high. This guarantees that the Transmit Data line to the data set is in the MARK condition when idle (which is an RS-232C specification).

4.6 Logical Sequence for Receive Mode

As in the Transmit Mode, the character format, baud rate, and mode must be loaded via an Output Command.

For the Receive Mode, the WT flip-flop is programmed reset and DTR is set. In HDX operation, the Transmit Busy bits BUFE and EOT are both high, this permits the gate in location 2M3 to reset WRT when WT0 is reset. With WRT=0, SND0 in location 1K5 is high. This permits steering the Receive status to the Processor.

Normally, when not receiving data, the RDATA1 input to the UART is high and the Busy Status output, EOC1, is low (BUSY=1). When the RDATA1 input goes low, the UART starts to assemble the character. When the complete character is assembled, EOC1 goes high to generate an interrupt and drop the Busy status to the Processor. At this time, if an Overflow, Parity Fail, or Framing Error has occurred, the appropriate output from the UART is high. These status bits are only reset when another character is received without the error condition.

With BSY=0, the Processor responds with a Read Data which activates DRG0 to cause EOC1 to go low (Busy condition). The Read Data also unloads the assembled character by strobing the 4/1 Multiplexors on Sheet 3.

If a Read Data is not issued before the next character is assembled, the OV status bit is set. This is reset only with SCLR or a Read Data.

4.7 Line Turnaround

In HDX operation, the direction of data flow may be reversed by simply commanding the WRT/RD bit to complement.

In the case of turning the line from Receive to Transmit, the WT0 line goes low which forces the WRT flip-flop set, and if DSRDY is active, RQ2S is gated to the data set. Data may be transferred when the data set responds with CL2S.

When turning the line from Transmit to Receive, the adapter must insure that the last character has been transmitted to the data set before initiating a turnaround. Figure 5 shows the required timing to accomplish this.

Referring to Figure 5, a DAG is issued as the last character to be transmitted, but the UART is transmitting the previous character from the Shift Register. An output command READ is then issued which causes WT to be reset.

In this case, the Buffer Register Busy and the Shift Register Busy are both set (BUFE1=EOT1=0). Buffer Register Busy forces TBSY=1. When the UART finishes transmitting the character presently in the Shift Register, it loads the Buffer into the Shift Register and the Buffer Register goes Not Busy. After this character is transmitted, the Shift Register goes Not Busy and the gate in location 2M3 resets WRT. This puts a low on the gate in location 2N5. The output from this gate is delayed for at least one millisecond. After this delay, RQ2S to the data set is finally turned OFF. After a delay in the data set, CL2S turns OFF and the adapter is not in the Receive mode. The BSY continues active until a character is received.

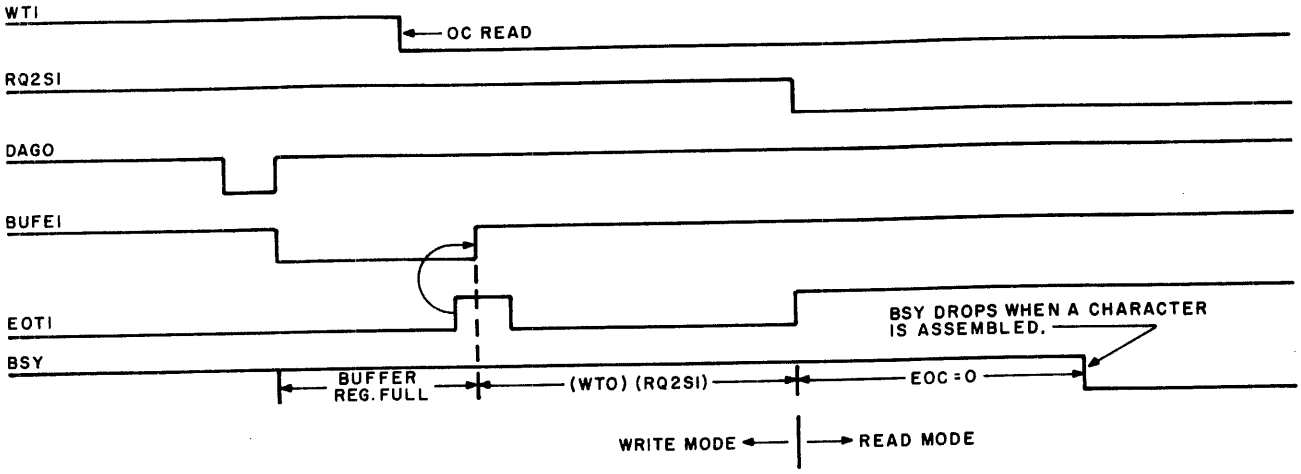


Figure 5. Write Read Line Turnaround

5. BAUD RATE SELECTION AND ADJUSTMENT

The 4-bit counters and one-shots on the left of Sheet 4 develop the required baud rate. The one-shots form an oscillator whose frequency is determined by the external fixed components and the potentiometer. The output is counted down to provide eight binary sub-multiples of the oscillator frequency. Two of these outputs may be connected to the stakes labelled J1 and K1 to permit program selection over these two baud rates. The output from these gates, CLK1, is normally strapped to the TCL1 and RCL1 inputs to the UART. This provides the required clock for serializing the data in the transmitter and de-serializing in the receiver. It must be noted that these clocks must be 16 times the desired baud rate. Table 2 shows the correspondence between some standard baud rates and the 16 times clock.

TABLE 2. CORRESPONDENCE BETWEEN BAUD RATE AND 16X CLOCK

	16X CLOCK
BAUD RATE	FREQUENCY (KHZ)
50	0.800
75	1.200
110	1.760
134.5	2.152
150	2.400
300	4.800
600	9.600
1200	19.200
1800	28.800
2400	38.400
4800	76.800
9600	153.600

Table 3 shows the approximate range of baud rates for each of the four bit counter outputs. Note that consecutive outputs overlap. When strapping a baud rate, an attempt should be made to select one which is closest to a mid-range adjustment of the potentiometer.

TABLE 3. BAUD RATE OPTIONS

CLK OUTPUT	BAUD RANGE (Approx.)			BAUD RANGE (Approx.) for Boards at level R01 or higher		
E1	1.4K	-	4K	6.2K	-	16K
F1	700	-	2K	3.1K	-	8K
G1	350	-	1K	1.5K	-	4K
H1	175	-	500	750	-	2K
A1	90	-	250	380	-	1K
B1	45	-	125	190	-	500
C1	25	-	60	95	-	250
D1	10	-	30	47	-	125

The procedure for achieving the correct baud rate is to select one or more appropriate outputs from Table 3. These should be wired such that the lowest baud rate is strapped to K1 and the highest baud rate to J1. Next, monitor the selected counter output with a frequency meter and adjust the potentiometer to the correct frequency (this may be found in Table 2). In the absence of customer information, for a baud rate, connect B1-K1 and H1-J1 and adjust the potentiometer to obtain 1200 baud (19.2 KHz) on H1. The output CLK1 should be strapped to TCL1 and RCL1.

6. TESTS

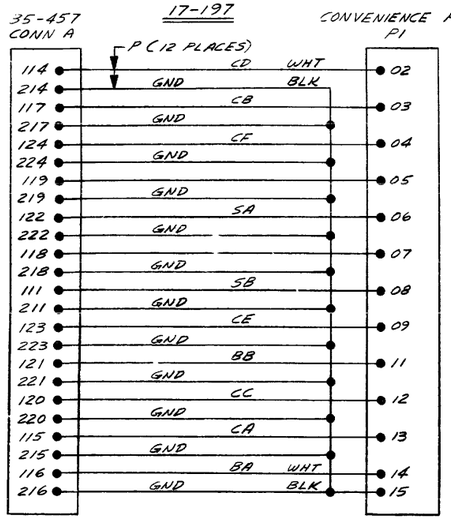
The PASLA is tested with Test Program 06-127.

7. MNEMONICS

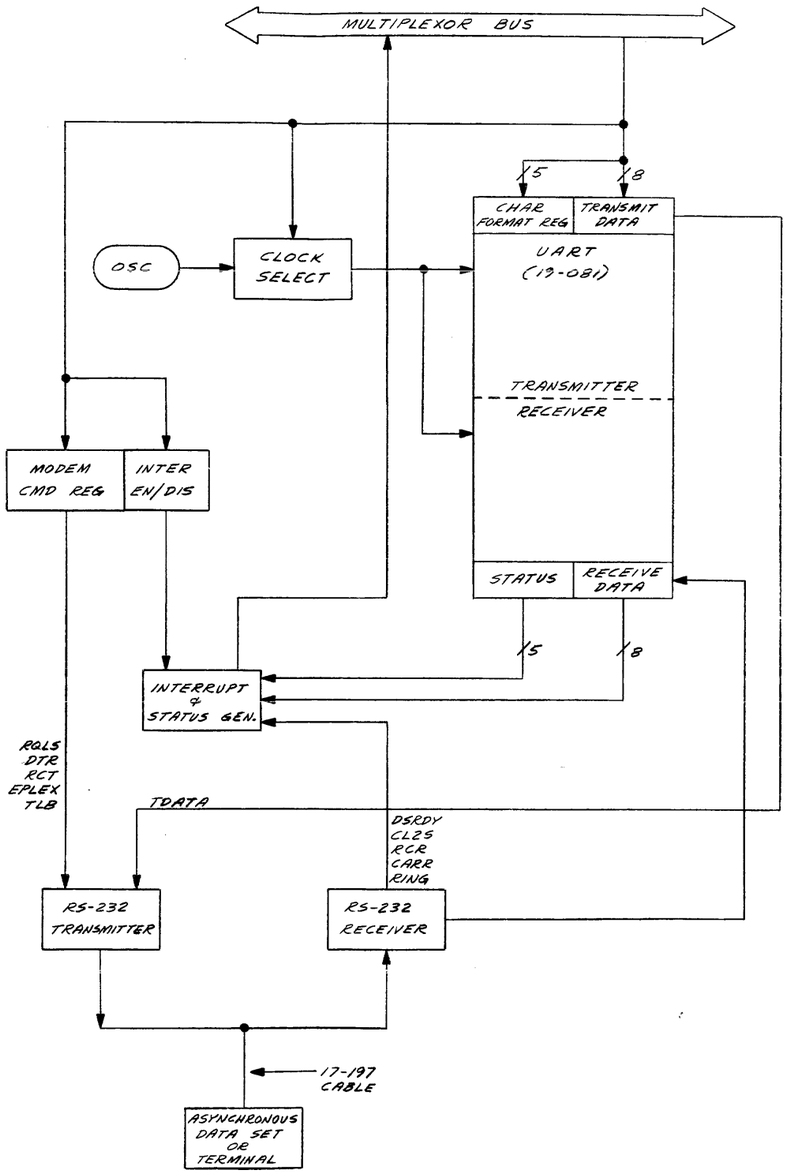
The following is a list of the mnemonics found in the PASLA. A brief description and the 02-279D08 source of each signal is provided.

MNEMONIC	MEANING	LOCATION
ATN	Interrupt Condition to Processor	1E6-1E9
BADD	Set when either line is addressed (Basic Address)	1J8
BUFE	Transmit Buffer Empty	4K4
CARR	Carrier from Data Set	2B4
CL2S	Clear to Send from Data Set	2G4
CMGA	Command to Modem Register	1K4
CMGB	Command for Character Format	1G3

MNEMONIC	MEANING	LOCATION
DSRDY	Data Set Ready from Data Set	2F4
DTR	Data Terminal Ready	2J2
EOC	Receive End of Character	4J6
EOT	Transmit End of Character	4K5
EPLEX	Echoplex	2K3
FDX	Full Duplex	2F6
FRERR	Framing Error	4G8
HDX	Half Duplex	1J6
OV	Receive Overflow Error	4G8
PF	Receive Parity Error	4G8
RATN	Receive Attention	5K7
RCR	Reverse Channel Receive from Data Set	2D4
RCT	Reverse Channel Transmit to Data Set	2K2
RDATA	Receive Data from Data Set	2H4
REN	Receive Enable flip-flop	5B6
RING	Ring from Data Set	2C4
RINT	Receive Interrupt	4R5
RQ2S	Request to Send to Data Set	2M9
RSRG	Receive Status Request	1F2
SATN	Send Attention	5K9
SEN	Send Enable	5B8
SEND	Active for Transmit Mode	1M5
SINT	Transmit Interrupt	4R4
SSRG	Send Status Request	1G2
TDATA	Transmit Data to Data Set	4K5
TLB	Transmit Line Break to Data Set	2L2
WT	Write Queue flip-flop	2M3



BLOCK DIAGRAM



RELEASED FOR PRODUCTION
ENG. DATE 1-16-13

REVISIONS

REVISED SHT. 4, 35-457 MOI WAS R00				
BG	1801	7-11-73	R01
REVISED SHT 4				
BG	2091	3-14-74	R02
REVISED SHT 5; AREA NB, 35-457 MOI WAS R03.				
	2689	3-16-76	R03
REVISED SHTS 1 & 2 35-457 MOI WAS R04 ADDED MANUAL USED IN.				
GP	3546	8-16-78	R04
REVISED SHT # 5, 35-457 MOI WAS R05.				
GM	3812	3-12-79	R05

CONNECTOR A

ROW 1	ROW 2	TERM NO.
CF	GND	24
CE		23
SA		22
BB		21
CC		20
		19
		18
CB		17
BA		16
CA		15
CD		14
		13
		12
SB		11
	GND	10

BACK PANEL MAP

ROW 1	ROW 2	TERM NO.
P5	GND	41
GND	GND	40
		39
		38
		37
		36
		35
		34
		33
		32
		31
		30
		29
		28
		27
SCLRO		26
		25
		24
SYNO	ATNO	23
RACKO	TACKO	22
	DAO	21
DRO	CMDO	20
SRO	ADRSO	19
D140	D150	18
D120	D130	17
D100	D110	16
D080	D090	15
		14
		13
		12
		11
		10
		09
		08
		07
		06
		05
		04
		03
		02
GND	GND	01
P5	GND	00

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

PASLA	~~35-457R00~~
	35-457M01R06

NOTE:
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

USED IN MANUAL 29-301

SHEET	REV. LEVEL	5	1	1		2	2
INDEX	SHEET NO.	0	1	2	3	4	5

NOTES

NAME	TITLE	DATE
D. BARNEK	DRAFT	1-31-73
W. WALTER	CHK	1-31-73
J. MISARCIK	ENGR	2-1-73
W. REES	QE	
E. [illegible]	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER

TASK NO. 03026
DWG NO. 02-279A R05 D08
SHEET OF 0-6

BRUNING 44 231 16042

REVISIONS
AREA L4 - SIGNAL CCMGS1. 2J1 WAS CMGA1. 2J1. A28-10 WAS CONNECTED TO A28-09. ADDED 2J1 AREA L8.
AREA D8 - LOC 2K1 AT D10DA WAS DELETED. LOC 2K1 AT D101A WAS ADDED.
GP 371 | 3546 | 8-16-78 | E01

219 ADR5O — A30 19-015 HG
119 SRO — A30 19-015 HG
120 DRO — A30 19-015 HG
221 DAO — A30 19-015 HG
220 CMDO — A30 19-015 HG
126 SCLRO — A30 19-015 HG
4B5, 5G7 SCLRI
5L8 ATSYNO

A29 19-003 G: ADSYNO, ADDI, ADRSI
A17 19-002 G: RSRGO 3A1; SSRGO 3A1; DRGO 3A1, 4K6; DAGO 4K4; CMGBO; CMGBI 2H1, 4F4
A18 19-004 G
A06 19-017 HG
A10 19-036 HP: SCLROA 5A5
P5 — R22 10K
SENDI, BADDI, SENDO, ATSYNO
A09 19-004 G: SCMGI 5A8; RCMGI 5A6
BRIEN

A19 19-001 G — C19 470PF — A18 19-004 G — A18 19-004 G — A10 19-036 HP: SYNO 123
D3, D1, D2, D4
A28 19-016 HG: 1G4 SCLRDA 10; CCMGS1 2J1
2N1 WRTI — A16 19-003 G
2F6 FDXC
P5A 4B5
A20 JDS1 T 19-095 HF KDC0: 2C5 HDXO; NC
A16 19-003 G — A18 19-004 G — A29 19-003 G: STINHO 3G1

218 D15O — 3N9 — A35 19-016 HG — A45 19-015 HG — 4H2 D151A — D151A — D150A
118 D14O — 3L9 — A35 19-016 HG — A45 19-015 HG — 4H2 D141A — D141A — D140A — 2M1 — ATN141 6 — 3L4 — D5
217 D13O — 3K9 — A35 19-016 HG — A45 19-015 HG — 4H2 D131A — D131A — D130A — 2L1, 4G2 — ATN131 5 — 3K4 — D7
117 D12O — 3H9 — A35 19-016 HG — A45 19-015 HG — 4H2 D121A — D121A — D120A — 2K1 — ATN121 4 — 3H4 — D6
216 D11O — 3G9 — A34 19-016 HG — A44 19-015 HG — 4H2 D111A — D111A — D110A — 2K1 — ATN111 3 — 3G4
116 D10O — 3F9 — A34 19-016 HG — A44 19-015 HG — 4H2 D101A — D101A — D100A — ATN101 2 — 3E4
215 D09O — 3D9 — A34 19-016 HG — A44 19-015 HG — 4H2,5A6 D091A — D091A — D090A — 2H1 — ATN091 1 — 3D4
115 D08O — 3C9 — A34 19-016 HG — A44 19-015 HG — 4H2,5A6 D081A — D081A — D080A — ATN081 0 — 3B4
(NOTE 1)

A96 19-001 G — A95 19-015 HG — A20 JDS1 T 19-095 HF KDC0: BADDI — 2J1; NC
SCLROA

NOTES
1. STANDARD DEVICE ADDRESS IS X'10'.

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	1-26-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER
TASK NO 03026
DWG NO 02-279 R01 D08
SHEET OF 1 —

REVISIONS

AREA J1, A06-01,02, 03,12 WAS ADDED. A15-03 WAS TO D10A 10B. AREA H1 SIGNAL CCMGS1 1L4 WAS CMGA1 1K4			
GP	V1	3546	8-15-78 R01

NOTES

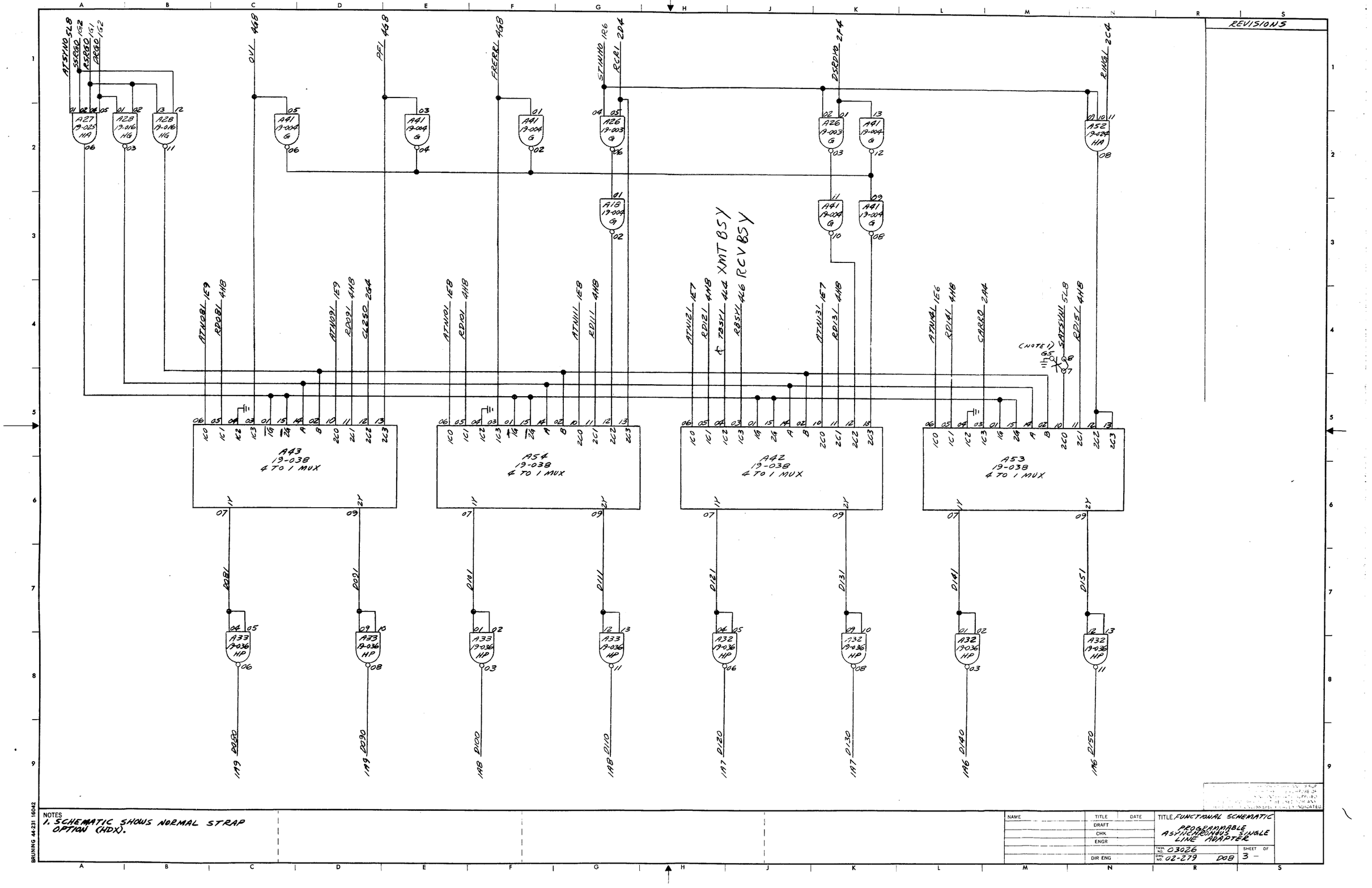
1. SCHEMATIC SHOWS NORMAL STRAP OPTIONS. THE STRAP OPTIONS FOR CF, CC AND CB ARE NORMALLY EQUIPPED FOR LOCAL TERMINALS.

	NAME	DATE
TITLE		
DRAFT		
CHK		
ENGR		
DIR ENG		

TITLE FUNCTIONAL SCHEMATIC
PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER

TASK NO 03326
DWG NO 02-279 R01 D08
SHEET 2 OF —

BRUNING 44-231 16042



NOTES
1. SCHEMATIC SHOWS NORMAL STRAP OPTION (HDX).

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER

TASK NO. 03026
DWG NO. 02-279 D08
SHEET OF 3 —

BRUNING 44-231 16042

REVISIONS				
C20 & C21 WERE .0022MF				
B	[illegible]	1801		R01
STRAPPING WAS H1 TO K1 & F1 TO J1.				
C	[illegible]	2091	[illegible]	R02

A50 19-035 4 BIT UP/DOWN COUNTER

A51 19-035 4 BIT UP/DOWN COUNTER (NOTE 1)

A55 19-081

CONTROL REGISTER

TRANSMITTER DATA REGISTER

TRANSMIT SHIFT REGISTER

CONTROL TRANSMITTER

RECEIVER

RECEIVER SHIFT REGISTER

DATA RECEIVED DETECT

STATUS REGISTER

RECEIVER DATA REGISTER

A14 19-003 G

A23 19-001 G

A24 19-004 G

A37 19-031 ONE SHOT

A38 19-031 ONE SHOT

A39 19-031 ONE SHOT

A36 19-031 ONE SHOT

BAUD RATE ADJUST

NOTES
1. SCHEMATIC SHOWS NORMAL STRAP OPTION 300 & 1200 BAUD.

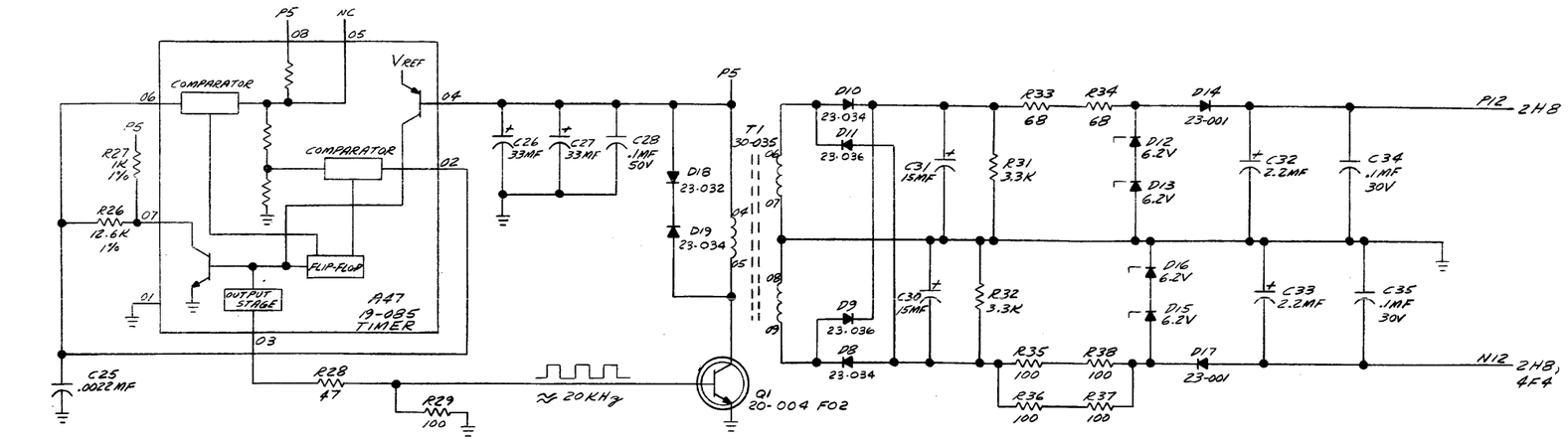
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

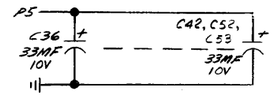
TITLE FUNCTIONAL SCHEMATIC
PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER

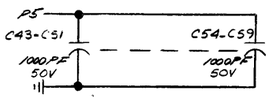
TASK NO. 03026
DWG NO. 02-279R02 D08
SHEET [illegible] OF 4

BRUNING 44-231 16042

REVISIONS			
AREA F2, T1 P/N WAS SPEC'D AS 30-020.			
DNMA-2689	—	3-16-76	R01
EXTENSIVE CHG'S. FOR PREVIOUS REV LEVELS, SEE R01 MICRO FILM			
DNMA-3812		3-12-78	R02





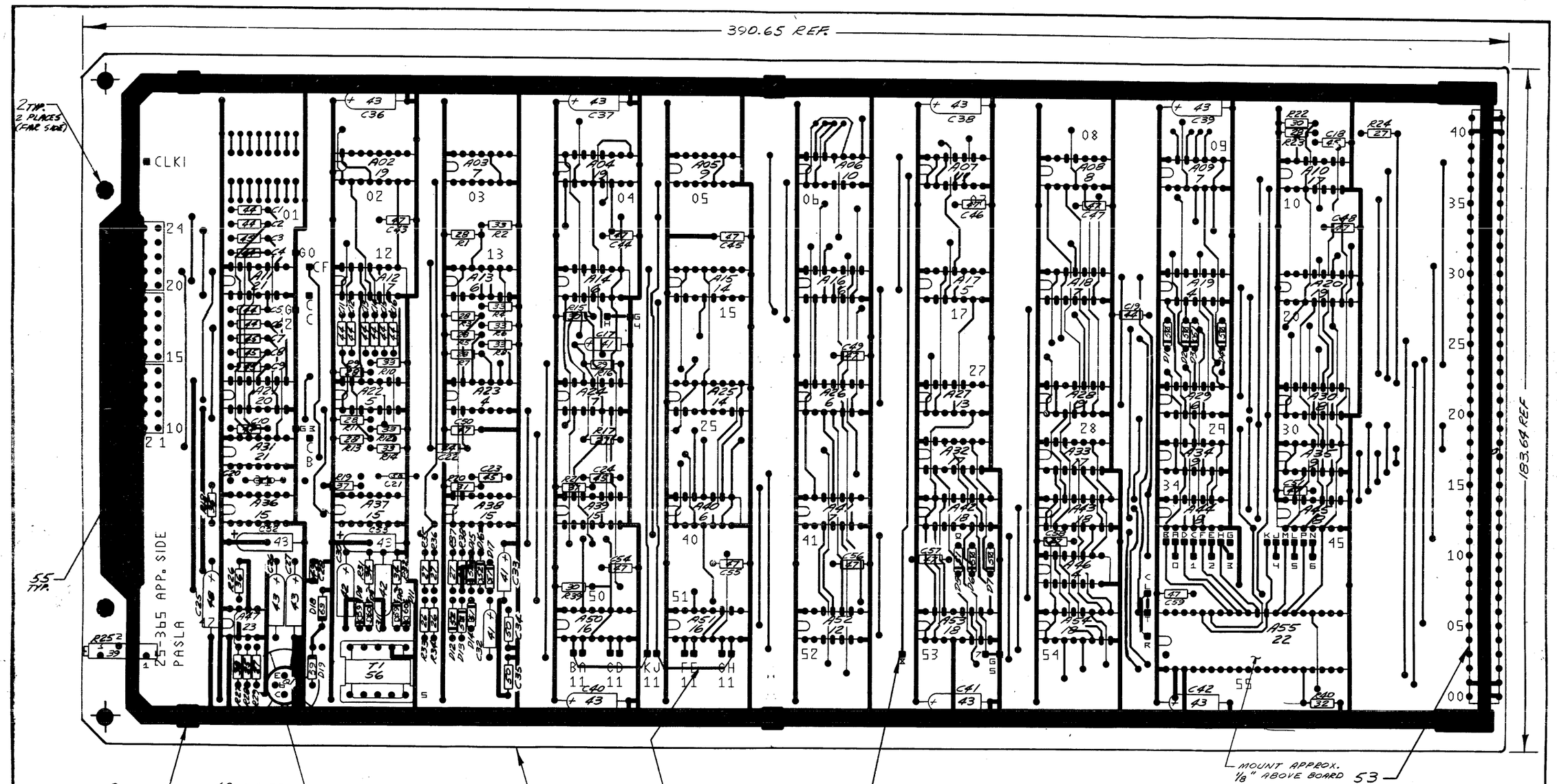


NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER

TASK NO. 03026 SHEET OF 5 - 6
DWG NO. 02-279 F02 D08



MILLIMETER	INCH
183.64	7.23
390.65	15.38

INTEGRATED CKTS	A02 – A47, A50 – A55
TRANSISTOR	Q1
RESISTORS	R1 - 29, R31 - 40
CAPACITORS	C1 - 28, C30 - 59
DIODES	D1 - D19
TRANSFORMER	T1

RELEASED FOR PRODUCTION
MFG. ENG. [signature] DATE 3/25/73

NOTES

METRIC DIMS. & TABLE WERE ADDED.	REVISIONS
GP [illegible] 3546 8-17-78 R03	C20 & C21 WERE ITEM 48
FOR PREVIOUS REV LEV SEE MICROFILM.	BG [illegible] 1801 [illegible] R01
GM [illegible] 3812 11-3-78 R04	STRAPS B1 TO K1 ; H1 TO J1 WERE H1 TO K1 & F1 TO J1 RESP.
	BG [illegible] 2091 [illegible] 4/19/74 R02
	REVISED COPPER TO REFLECT R03 ARTWORK. (CONT)

NAME	TITLE	DATE
D. BARKER	DRAFT	2-5-73
H. MATTER	CHK	2-5-73
J. PISARCIK	ENGR	3-9-73
H. ROSS	Q. C.	3-15-73
R. E. JONES	DIR. ENG.	3-23-73

TITLE
ASSEMBLY, PRINTED CIRCUIT
PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER
SCALE: 2/1

TASK NO. 03026
DWG. NO. 35-457 M01 R04 D03
SHEET 1 OF 1

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