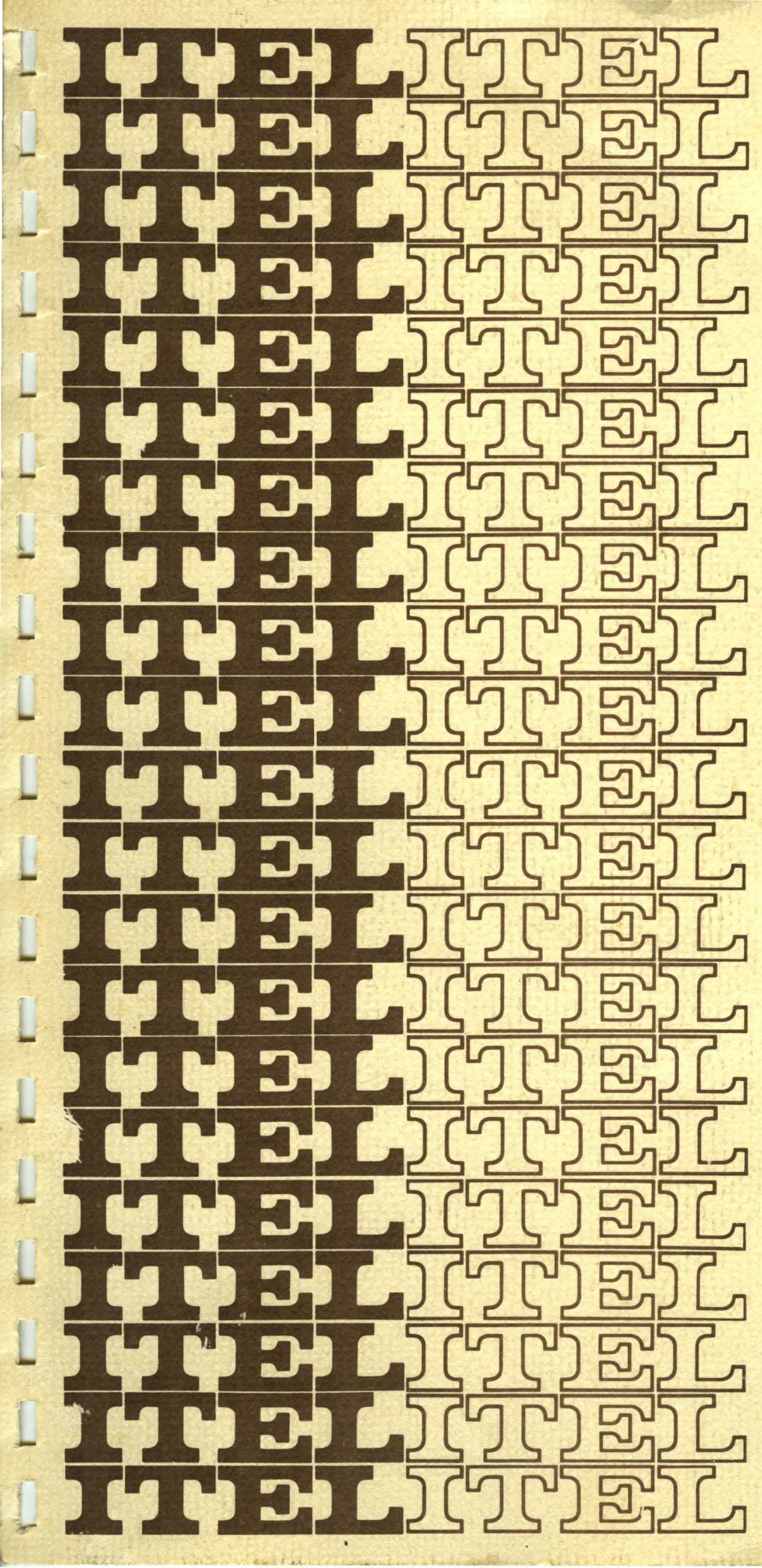

MAGNETIC TAPE WORD PROCESSOR

OPERATION, SERVICE, AND DIAGRAMS MANUAL

UD002441-1

ITEL CORPORATION
FIELD ENGINEERING DIVISION

SEPT., 1972

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ITEL CORPORATION
FIELD ENGINEERING DIVISION

Technical Support Operations
10435 North Tantau Avenue
Cupertino, California 95014
Tel: (408) 257-6220 TWX 910-338-0280

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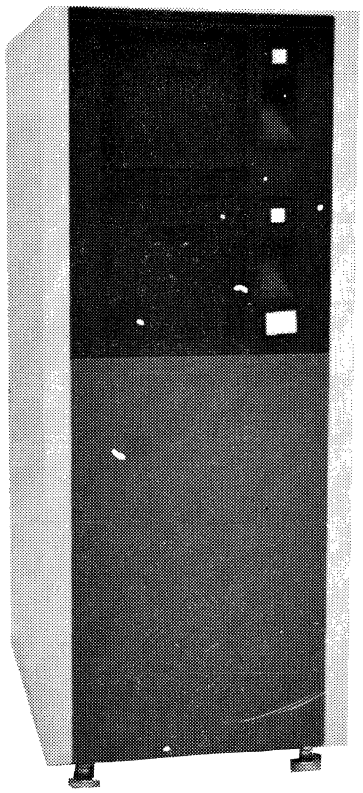
CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides installation, operation, and service instructions for both the single and dual station Magnetic Tape Word Processor (MTWP), shown in Figure 1-1. Both systems combine the functions of a Microprocessor, an electronic keyboard and printer, and one (single station) or two (dual station) magnetic tape transports to form an automatic writing system. The Microprocessor and magnetic tape transports are contained in a compact console. The keyboard and printer are housed in an attractive case suitable for secretarial use.



Console

Typewriter

Figure 1-1. Magnetic Tape Word Processor

1.2 MANUAL CONTENT

This Magnetic Tape Word Processor Operation, Service, and Diagrams Manual is divided into nine chapters. The following paragraphs briefly describe the contents of each chapter.

1.2.1 Chapter 1, General Information

This chapter provides introductory material, a description of manual contents, an equipment description, and the specifications for the system.

1.2.2 Chapter 2, Installation

Chapter 2 discusses unpacking, inspection, and the interconnections required when installing a system. A preoperation checks and adjustments procedure is also provided in this chapter to verify that the system is operating properly.

1.2.3 Chapter 3, Operation

Chapter 3 identifies and describes the function of each key on the keyboard, control and indicator on the console, and system alarm.

1.2.4 Chapter 4, Theory of Operation

The theory of operation is provided in this chapter. Block diagrams, simplified drawings, and timing diagrams are used, where necessary, to support the text.

1.2.5 Chapter 5, Maintenance

Chapter 5 outlines safety precautions, presents maintenance philosophy, and lists required special tools and test equipment.

1.2.6 Chapter 6, Checks and Adjustments

Electrical and mechanical checks and adjustments are contained in Chapter 6.

1.2.7 Chapter 7, Error Analysis

This chapter contains information designed to assist in troubleshooting.

1.2.8 Chapter 8, Replacement Procedures

Chapter 8 presents removal and installation procedures.

1.2.9 Chapter 9, Diagrams

This chapter contains the schematic diagrams for the system as well as those for the Programmed Diagnostic Aid (PDA). The system wire list is also included.

1.3 SYSTEM DESCRIPTION

The ITEL single or dual station Magnetic Tape Word Processor, (MTWP) is an electronic system for automatic writing. The functions of both are identical; therefore, only the dual station system will be discussed. The dual station does, however, extend the capabilities of the single station system. The major components of the system are:

- A Microprocessor.
- A full duplex electronic keyboard.

- An electronic printer.
- Two magnetic tape transports.

Figure 1-2 provides a simplified block diagram of the system.

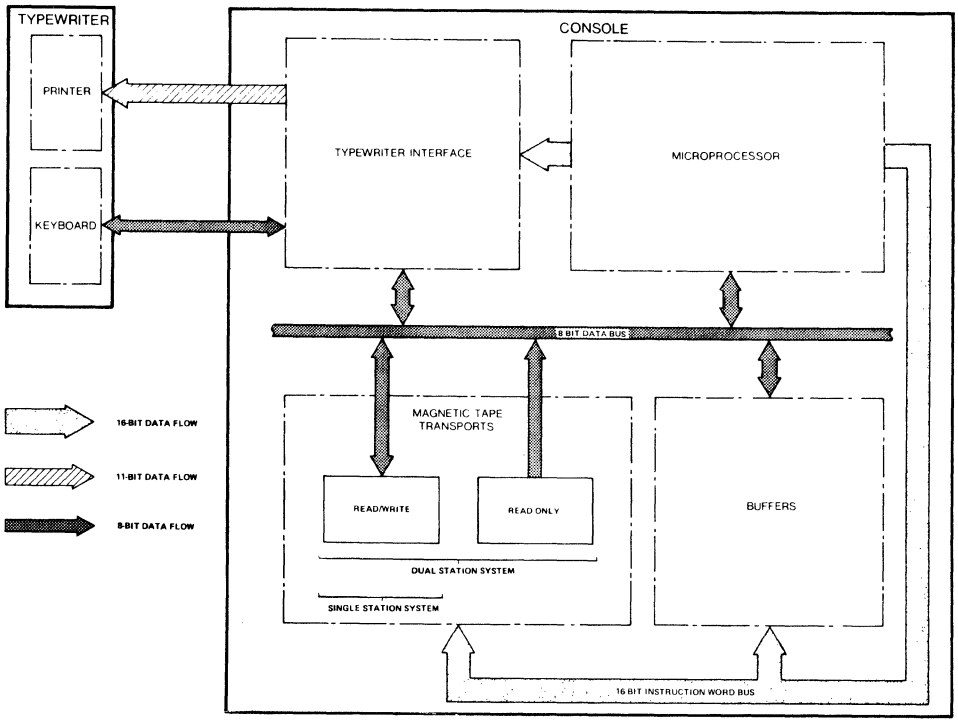


Figure 1-2. Simplified System Block Diagram

1.3.1 Microprocessor

The Microprocessor has the capability of storing 4096 sixteen-bit instruction words. These sixteen-bit instruction words are used to control the operation of the system. It also has an eight-bit parallel data bus (DBØ through DB7). Any information which is processed is processed on this data bus. The data bus links the Microprocessor, keyboard, printer, and both magnetic tape transports together into one unit. Information is gated on and off the data bus by the instruction words stored in the Read Only Memory portion of the Microprocessor.

1.3.2 Keyboard

The keyboard used in this system is a full duplex electronic keyboard. Through the use of this type of keyboard, signals are routed through the Microprocessor to the printer, rather than directly to the printer. All system functions are controlled by the operator from the keyboard. A standard 44-key typewriter array inputs information into the system during normal typing operations. Certain keys are lighted, when depressed, to indicate the present operation. These lighted keys also monitor the Microprocessor

and flash to display input, output, and system error conditions. The function of each key on the keyboard and each alarm is discussed in detail in Chapter 3 of this manual.

1.3.3 Printer

The printer, used as the output device for the system, is of a serial type (prints a single character at a time). It operates at speeds up to 30 characters per second on general text such as letters, specifications, contracts, etc. The 15-inch long platen indexes at six lines per inch (single space) or three lines per inch (double space).

There are three basic printer motions; carrier, print wheel (character), and paper feed. Each motion is controlled by the system through the printer interface. These controls are sent down the eleven data lines. The data lines transmit either the 7-bit ASCII code for the next character to be printed, an 11-bit word which specifies the direction and number of printing spaces to be moved by the carrier (in multiples of 1/60 of an inch), or an 11-bit word which specifies the direction and number of vertical line spaces (indexes) that the paper is to be moved by the paper feed (in multiples of 1/48 of an inch).

Character sets are provided in the form of an 88-character print wheel. These print wheels are easily interchanged by the operator.

Two types of ribbon cartridges are available and these too are easily interchangeable by the operator. The styles available include single reusable fabric and a single-use carbon.

1.3.4 Magnetic Tape Transports

The dual station system has two circulating-type, live-memory, MOS buffers which store a single line of typewritten information. This information, in the form of an 8-bit word on the data bus, comes from either the keyboard or magnetic tape storage enroute to the printer. A single line of typewritten information can contain up to 256 of these 8-bit characters. Information from the keyboard is stored, a line at a time, in the buffer and then outputed, a line at a time, onto the read/write (R/W) magnetic tape.

The magnetic tape transports are capable of unidirectionally reading and writing at 20 inches per second and bidirectionally searching at 70 inches per second. Naturally, the read only magnetic tape transport (dual station system only) is only capable of unidirectionally reading at 20 inches per second and bidirectionally searching at 70 inches per second. The functions of each magnetic tape transport, like any other functions of the system, are controlled by the operator from the keyboard.

1.4 SPECIFICATIONS

The specifications for the dual station Magnetic Tape Word Processor (MTWP) are listed in Table 1-1.

Table 1.1. Dual Station MTWP Specifications

CHARACTERISTICS	SPECIFICATIONS
MICROPROCESSOR:	
Type of storage	Read Only Memory (ROM)
Storage capacity	65,536 (4096 16-bit instruction words)
Instruction cycle time	2 μs
Memory access time	1 μs maximum
KEYBOARD:	
Typewriter array	44 keys
Lighted Function keys	12
Non-Lighted Function keys	4
Repeat keys	Hyphen, backspace, forward index, reverse index, X, carrier return, space bar and period.
Maximum input rate	500 characters per second
PRINTER:	
Number of characters	88
Print speed	>30 characters per second (on general text)
Print line length	132 characters at 10 per inch (10-pitch) or 158 characters at 12 per inch (12-pitch)
Line spacing	6 per inch (single spaced) or 3 per inch (double spaced)
Print quality	Standard typewriter
Paper feed	15-inch platen fed

Table 1-1. Dual Station MTWP Specifications (continued)

CHARACTERISTICS	SPECIFICATIONS
Copy capacity	Original plus five carbons
Ribbon type	Cartridge loaded (reusable fabric or single-use carbon)
Print element	Interchangeable print wheel
MAGNETIC TAPE TRANSPORTS:	
Read/Write speed	20 ips (average)
Search speed	70 ips (average)
Start time	50 ± 10 ms @ 20 ips
Stop time	50 ± 10 ms @ 20 ips
Start distance	0.5 ± 0.1-inch @ 20 ips
Stop distance	0.5 ± 0.1-inch @ 20 ips
MAGNETIC CASSETTE:	
Type	Modified Philips
Tape	Computer grade
Capacity	300, 150 and 75 feet
Storage capacity	50K, 25K, and 12K characters
Maximum search or rewind time	51, 26 and 13 seconds
ENVIRONMENTAL:	
Temperature range	50°F min. to 95°F max.
Humidity range	8% min. to 80% max. (maximum wet bulb temp. 80°F)
POWER:	
Primary power requirement	115 VAC ± 10% @ 15 A
DC supply voltages (developed by internal supplies)	+24V ± 2.6V +15V ± 0.75V +5.12V ± 0.05V -5V ± 0.25V -9V ± 0.45V -15V ± 0.75V

Table 1-1. Dual Station MTWP Specifications (continued)

CHARACTERISTICS	SPECIFICATIONS
PHYSICAL:	
Console service openings	Both side panels
Typewriter service openings	Removable cover and access panel
Console dimensions	
Height	30.5 inches
Width	12 inches
Depth	22 inches
Weight	< 140 lbs.
Mounting	Leveler feet
Typewriter dimensions	
Height	8.45 inches
Width	22.5 inches
Depth	19.63 inches
Weight	< 50 lbs.
Connecting cables	2; AC power and typewriter to console

CHAPTER 2

INSTALLATION

2.1 UNPACKING

The Magnetic Tape Word Processor is inspected for mechanical and electrical operation prior to shipment. Individual units that comprise part of the system (the typewriter and console) are separately packaged into two containers. Perform the following unpacking procedures to attain optimum system performance. Before removing units from their containers, examine each for broken bands, crushed walls, or other signs of damage. If damage is evident, contact the transportation company involved before removing the units from their packaging. Original packaging material should be retained to facilitate any return shipment.

2.1.1 Unpacking the Typewriter Unit

Use the following procedure to remove the typewriter unit from its container. See Figure 2-1.

1. Position the packaged typewriter unit on the floor near the desk or typing stand where it is to be used.
2. Remove the tape securing the top flaps of the outer container.
3. Remove the tape securing the top flaps of the inner container.
4. Remove the plastic sheet from typewriter unit.
5. Remove the typewriter from the inner container and set it into position on desk or typing stand.
6. Visually examine the surfaces of the typewriter unit to ensure that no physical damage has resulted.
7. Retain all packaging materials for possible future use.

2.1.2 Unpacking the Console Unit

Use the following procedure to remove the console unit from its container. See Figure 2-2.

1. Using a hand truck, transport the console unit to a location near a desk or typing stand where it will be used.
2. Remove the two bands wrapped around the container.
3. Lift the container up and away from the console unit.
4. Break down one of the end flaps on the telescoping tray into which the console unit is set.
5. Slide the console unit from the telescoping tray and set it in its operating position.

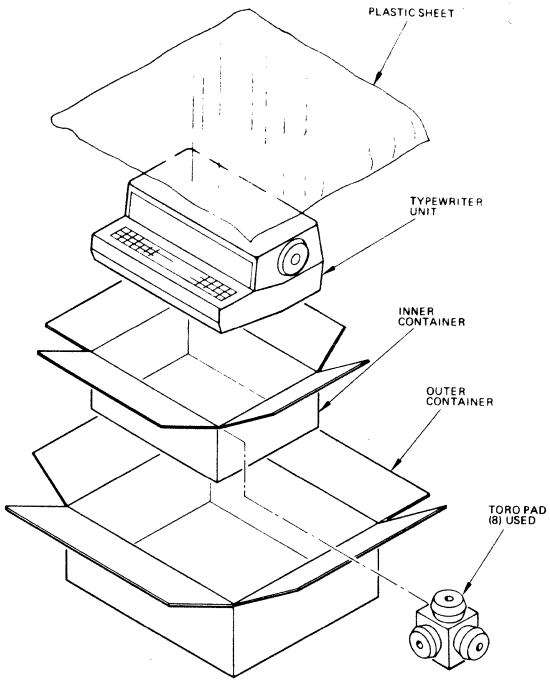


Figure 2-1. Typewriter Unit Packaging

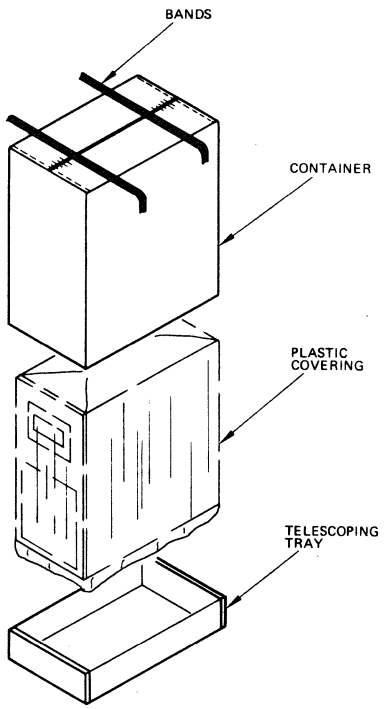


Figure 2-2. Console Unit Packaging

6. Remove the protective plastic covering that surrounds the console unit.
7. Unwind the AC power cord and interconnection cable.
8. Examine the surfaces of the console unit to ensure that no physical damage has resulted.
9. Retain all packaging materials for possible future use.

2.2 SYSTEM INTERCONNECTIONS

Use the following procedure to connect the two system components. See Figures 2-3 and 2-4.

1. Tilt the typewriter platen cover upward to expose the platen.
2. Depress the two platen release levers and lift the platen from the typewriter.
3. Raise the left-hand lever switch bank that supports the MARG LEFT/RIGHT and TAB CLEAR/SET levers.
4. Raise the right-hand lever switch bank that supports the SINGLE/DOUBLE and 10/12 levers.
5. Pull forward on the two upper case release levers and remove the upper case from the typewriter.
6. Remove the two screws that secure the cable clamp to lower case.
7. Lay in the typewriter-to-console innerconnection cable.
8. Locate and mate the four following typewriter-to-console connectors.

   NOTE: Alternately, tighten both screws to secure A7P1, A7P3 and A7P4 in place.

A7P1	34-pin	Printer Interface Connector
A7P2	56-pin	Keyboard Interface Edge Connector
A7P3	14-pin	Power Connector
A7P4	14-pin	Lever Switch Interface Connector

9. Place the cable clamp back into place and secure using the two screws removed in step 6.
10. Examine the interior of the typewriter to ensure there are no loose or broken connections, loose screws, or debris located in the typewriter.
11. Replace the upper cover and then the platen by snapping them back into place.
12. Lower both lever switch banks into place.
13. Lower the platen cover.
14. Remove the right-hand access panel from the console by grasping the lower edge of the panel and pulling it away from the frame structure. Lift it up and away from the frame.

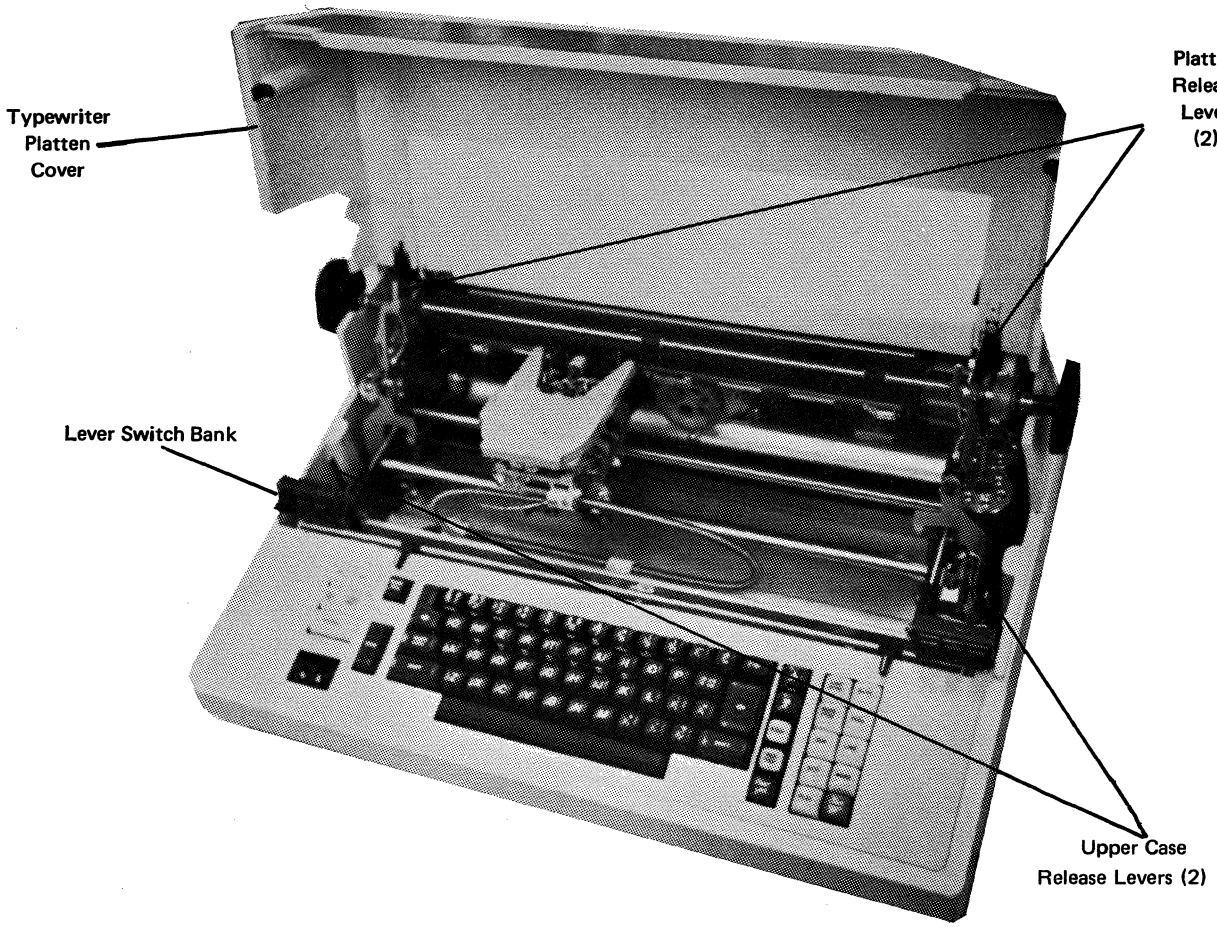


Figure 2-3. Typewriter Cover Removal

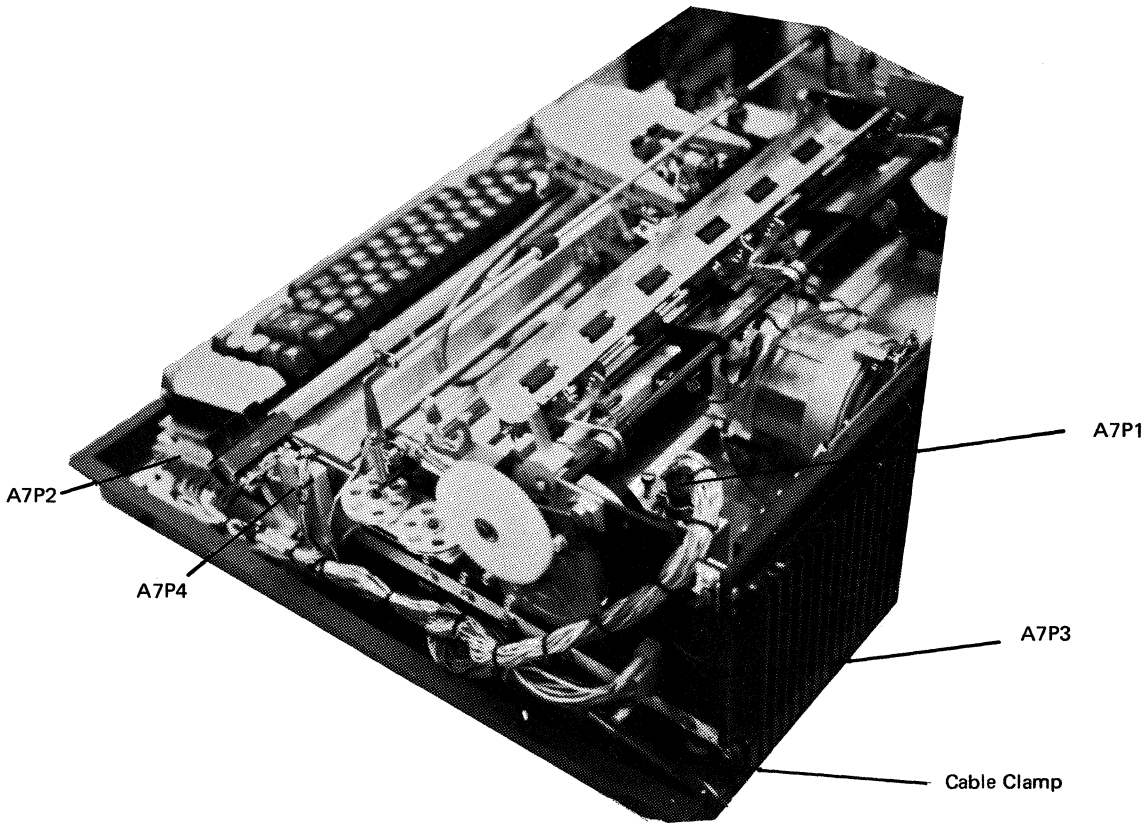


Figure 2-4. System Interconnections

15. Examine the interior of the console from this side to ensure that there are no loose or broken connections, loose screws, or debris located in the console.

16. Verify that each printed wiring assembly (PWA) is properly located and seated in its respective socket of the card cage. The location of each PWA in the card cage is listed in Chapter 4 of this manual.

17. Verify that the following internal connections are secure:

    Printer Interface (PWA 1)
    Keyboard Interface (PWA 3)
    R/W Tape Control (PWA 17) to Tape
    Read/Write (R/W J2)
    RO Tape Control (PWA 20) to Tape
    Read Only (RO J2)

    NOTE: Leave the right-hand side access panel off to facilitate the system diagnostic checkout.

18. Examine each tape transport for physical damage.

19. Release the door to each tape transport and wipe off the heads and EOT sensors with a lint-free wiper dampened with 90% isopropyl alcohol.

2.3 PREOPERATIONAL CHECKOUT

Once the system components have been unpacked, inspected, and connected, they may be checked for proper operation. This involves a power supply voltage and a system diagnostic checkout.

2.3.1 Power Supply Voltage Checkout

Use the following procedure to initially power up the system or to verify power supply voltages. See Figure 2-5.

1. Remove the left-hand side access panel from the console by grasping the lower edge of the panel and pulling it away from the frame structure. Lift it up and away from the frame.

2. Lower the power supply interconnect panel by loosening the two securing screws.

3. Examine the interior of the console from this side to ensure there are no loose or broken connections, loose screws, or debris in the console.

4. Verify that the two 15A fuses (F1 and F2) are installed and both the main circuit breaker (CB1) and POWER switch are set to the OFF position.

5. Connect the power cord to a 115 VAC, 60 Hz power source.

6. Set CB1 to ON.

CAUTION

Use care when probing power circuits. An AC voltage level of 115VAC is present in the power supply section when the POWER pushbutton is depressed to off.

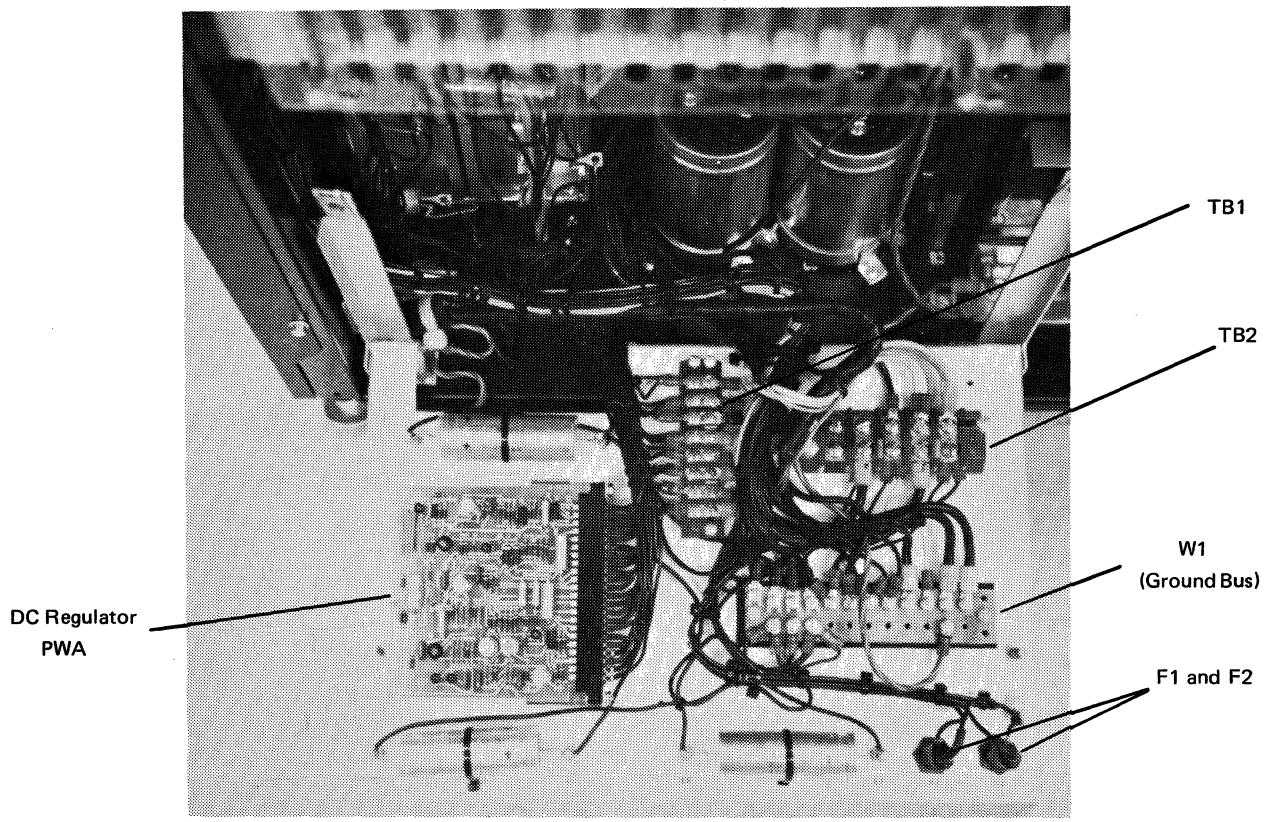


Figure 2-5. Power Supply Interconnect Panel

7. Depress the POWER switch, located on the front panel of the console, to ON.

8. Using a Weston Model 4440 Digital Multimeter (DMM) or an equivalent, measure the voltages present at the terminal strips (TB1 and TB2) with respect to ground bus (W1). Table 2-1 lists voltages present at each terminal.

9. Return the power supply interconnect panel to its upright position and tighten the two securing screws.

10. Replace the left-hand side access panel by setting the upper edge into place and pushing the lower edge against the frame structure.

Table 2-1. Power Supply Voltages

Terminal Strip TB1		Terminal Strip TB2	
Terminal	Voltage	Terminal	Voltage
1	+24 ± 2.6 Vdc	1	+5.12 ± 0.05 Vdc
2	+15 ± 0.75 Vdc	2	
3			
4	-22.5 ± 2.5 Vdc	3	
5	-15 ± 0.75 Vdc	4	+11 ± 1.2 Vdc
6			
7	-9 ± 0.45 Vdc		
8	-5 ± 0.25		

2.3.2 System Diagnostic Checkout

Use the following procedure to verify proper system operation.

1. Ensure that the POWER switch is set to OFF.
2. Install the Programmed Diagnostic Aid (PDA) in sockets 27 and 28.
3. Perform each diagnostic routine outlined in Chapter 6.
4. When all routines have been performed and the system operation verified, remove the PDA.
5. Replace the right-hand side access panel by setting the upper edge into place and pushing the lower edge against the frame structure.
6. Wipe off all exterior covers using a lint-free wiper dampened with 90% isopropyl alcohol.
7. Position the console into its operating position.
8. Adjust each leveller foot, as required.

NOTE: If the console is placed on a carpetted floor, the leveller feet must be adjusted so that a minimum of 1-inch exists between the bottom of the console and the rug pile in order to provide adequate ventilation.

CHAPTER 3

OPERATION

3.1 KEYS, CONTROLS, INDICATORS AND ALARMS

Each key on the keyboard has been classified and presented as follows to provide a better understanding as to their functions:

- Basic Operation Keys
- Mode Keys
- Action Keys
- Encoded Function Keys

In each classification, a key is first identified, and then its function is defined. An illustration is provided for each group to assist in the location of each discussed key.

The controls and indicators located on the Console are then identified and defined and a description of each system alarm is presented.

3.1.1 Basic Operation Keys

Those keys, highlighted in Figure 3-1, are classified as basic operation keys since they control the basic operations of the system. Normally, each is found on a standard typewriter keyboard. All are found on both the single and dual station systems.

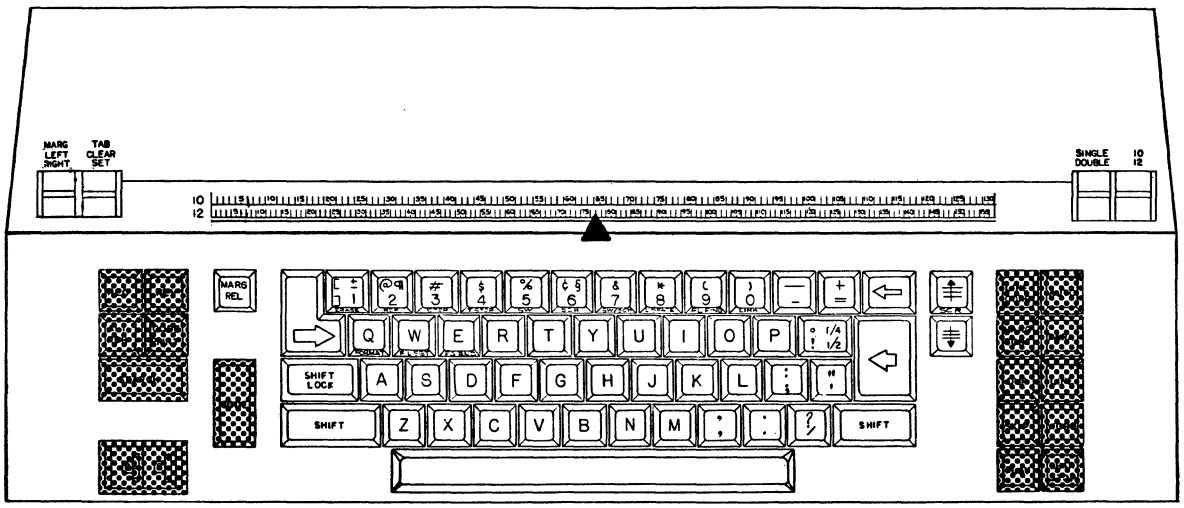


Figure 3-1. Basic Operation Keys

Character Set - There are 44 standard character keys located on the keyboard. All of these are capable of three functions: lower case, upper case, and an encoded function. As each character is struck, the 8-bit ASCII code associated with that character will be transferred to the system. A print sequence will be initiated to cause the character associated with that code to be printed and the carrier to be advanced one character space. The underscore, hyphen, period, and X keys are the only repeatable alpha-numeric keys.

Space Bar - The Space Bar, when depressed, will cause the carrier to move from left to right one character space for each depression. If held for greater than 500 milliseconds, the carrier will continue to move from left to right for so long as the Space Bar remains depressed or until the right-hand stop is reached.

Shift - The left- or right-hand Shift key, when held depressed, will cause an electronic shift of the keyboard (no printer movement). As each character is struck, the upper case 8-bit ASCII code associated with each struck character is transferred to the system.

Shift Lock - The Shift Lock key mechanically locks only the left-hand Shift key in the upper case position. The lock will be released when the Shift key is depressed.

Carrier Return - The Carrier Return key, when depressed, will cause the carrier to move to the left-hand margin and the paper feed to execute the number of forward vertical index operations specified by the setting of the SINGLE/DOUBLE Line Space Lever. If held for greater than 500 milliseconds, the paper feed will continue forward vertical indexing for as long as the Carrier Return key remains depressed.

When depressed together with the CODE key during the Record mode, a "required carrier return" will be encoded onto the tape. Refer to the Operating Insutructions referenced in paragraph 3.2 of this manual for details on the use of this encoded function.

TAB CLEAR/SET Lever - This lever is used to electronically set or clear tab locations. The lever, when placed down (SET) will cause the code for the present position of the carrier to be stored by the system. A tab cannot be set directly at the left- or right-hand margin position. There must be at least one character space to the right of the left-hand margin or to the left of the right-hand margin.

Positioning the carrier to a tab location and placing the lever up (CLEAR) will clear the stored location. When placed up (CLEAR) together with the CODE key, all stored tabs will be cleared. This may be done at any carrier position.

The lever, when placed down (SET) during the Record mode, will cause the code for the carrier position to be encoded onto the tape. In this way, tab locations will automatically be set for playback.

NOTE: Since the storing of tab locations is an electronic function (there are no actual mechanical tabs), all tab locations will automatically be cleared when the power is turned on, except for those encoded onto tape.

Tab - Depression of the Tab key will cause the carrier to move from its present location to the first set tab location provided that the carrier is not at the right-hand stop position.

When depressed together with the CODE key, during the Record mode, a "required tab" will be encoded onto the tape. Refer to the Operating Instructions referenced in paragraph 3.2 of this manual for details on the use of this encoded function.

MARG LEFT/RIGHT Lever - This lever is used to electronically set the left-and right-hand margin position. The lever when placed up (LEFT) will cause the code for the present position of the carrier to be stored by the system. With the carrier repositioned

for the right-hand margin, the lever can be placed down (RIGHT) to store the right-hand margin position.

NOTE: The keyboard does not lock when you reach the right-hand margin. The system buzzer will sound to indicate that five spaces remain before the right-hand margin is encountered.

The lever, when used during the Record mode, will cause the codes associated with the left- and right-hand margin positions to be encoded onto the tape. In this way, the left- and right-hand margins will automatically be set for playback.

During the initial power on sequence, the carrier is positioned to the left most position and then spaced to a standard left-hand margin position. The position is stored and in a similar manner a right-hand margin position is stored. These stored margin positions (10/70 for 10-pitch or 12/84 for 12-pitch) are typical settings for use with 8-1/2" x 11" paper. The operator then has the option of using these standard positions or setting the desired margin positions as previously described.

NOTE: Since the storing of margin positions is an electronic function (there are no actual mechanical stops), all margins will automatically be cleared when the power is turned on except for those encoded onto tape.

MARG REL - The margin release key, when depressed, permits the operator to bypass the present left-hand margin.

Backspace - The Backspace key, when depressed, will cause the carrier to move from right to left one character space for each depression. If held for greater than 500 milliseconds, the carrier will continue to move from right to left for as long as the Backspace key remains depressed or until the left-hand margin is reached.

When depressed together with the CODE key, during the Record mode, a "required backspace" will be encoded onto the tape. Refer to the Operating Instructions referenced in paragraph 3.2 of this manual for details on the use of this encoded function.

Forward Index (⭱) - The Forward Index key, when depressed, will cause the paper feed to execute forward vertical index operations. If held for greater than 500 milliseconds, the paper feed will continue forward vertical indexing for as long as the Forward Index key remains depressed.

During the Record mode, the Forward Index code will be recorded onto the tape. When read during playback, the paper feed will automatically execute each recorded forward vertical index operation.

Reverse Index (⭳) - The Reverse Index key, when depressed, will cause the paper feed to execute reverse vertical index operations. If held for greater than 500 milliseconds, the paper feed will continue reverse vertical indexing for as long as the Reverse Index key remains depressed.

During the Record mode, the Reverse Index code will be recorded onto the tape. When read during playback, the paper feed will automatically execute each recorded reverse vertical index operation.

SINGLE/DOUBLE Line Space Lever - This lever is used to electronically set the line spacing of the printer to six lines per inch (SINGLE) or three lines per inch (DOUBLE).

10/12 Pitch Lever - This lever is used to electronically set the pitch of the printer to ten characters per inch (10) or twelve characters per inch (12).

3.1.2 Mode Keys

Those keys, highlighted in Figure 3-2, are classified as mode keys since they establish the mode of system operation. Each is a lighted key which illuminates, when depressed, to indicate the present system operation. Certain keys flash to signal input, output, or system error conditions. These alarms are discussed in detail in paragraph 3.1.6 of this manual.

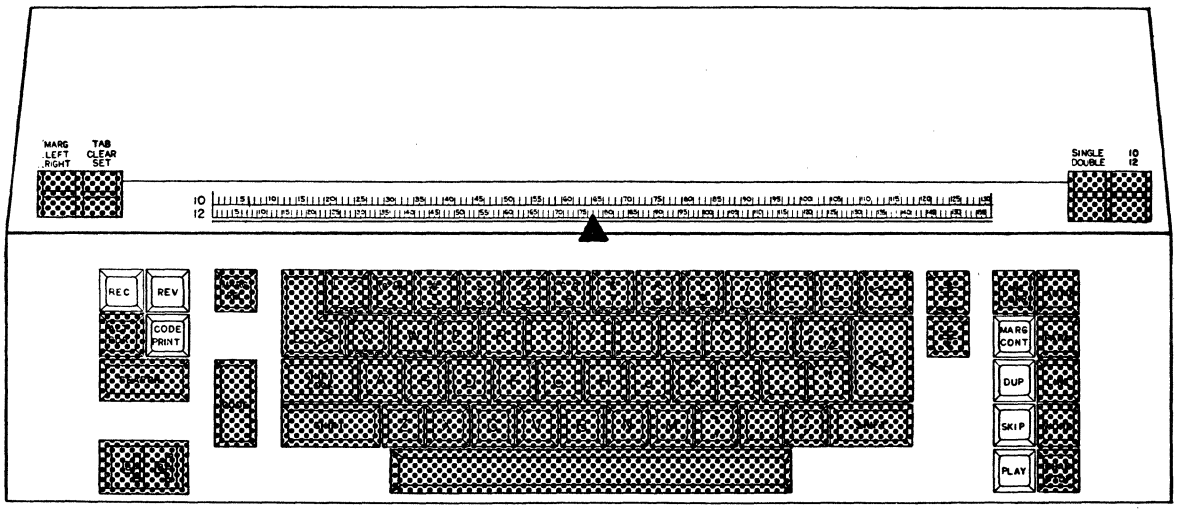


Figure 3-2. Mode Keys

Record (REC) - This lighted key, when depressed, selects the Record mode of operation. In this mode, the read/write (R/W) magnetic tape transport is actuated and the tape is automatically searched for a recordable area. A recordable area is detected when an EOR (end of record) is located. An EOR is recorded on the tape each time the Record mode is turned off. In this way, old data is preserved and new data can be added to the tape.

Revise (REV) - This lighted key, when depressed, selects the Revise mode of operation. This mode is used to make corrections on a prerecorded tape. The corrections must be made within the prerecorded line plus 50 characters. SKIP and PLAY may also be activated during this mode. In this way, minor revisions can be made without the need of an RO to R/W transfer.

CODE PRINT - This lighted key, when depressed, will cause the printing of the typewriter character that is associated with an encoded function. An automatic overprinting

of this character with a slash (/) will follow to indicate that this is an encoded function, not a regular typed character. Those numeric codes that accompany an encoded function will also be printed, but not slashed. Table 3-1 lists those slashed characters and the encoded functions they represent.

When depressed together with the CODE key, all prerecorded margin and tab settings will automatically print out on the paper. If CODE PRINT is not on, the encoded function will occur as specified, but no slashed character will print.

Table 3-1. Encoded Function Codes

CODE	ENCODED FUNCTION	KEY
2/	Reference	REF
3/	Stop	STOP
4/	Transfer Stop	TSTOP
5/	Switch	SW
6/	Search	SCH
7/	Switch and Search	SW/SCH
8/ or 9/	SINGLE/DOUBLE Line Space	L SPACE
9/	First Line Find	FL FIND
0/	Track Link	LINK
Q/	Format	FORMAT
W/	First Line Set	FL SET
E/	Page End (line count)	PG END

Margin Control (MARG CONT) - This lighted key, when depressed during the Play mode, will automatically cause the right-hand margin to readjust within a five character space zone. This zone may be adjusted from 0 to 7 character spaces. Refer to the Operating Instructions referenced in paragraph 3.2 of this manual for details on the use of this mode and the zone adjustment technique.

Duplicate (DUP) - This lighted key (dual station systems only), when depressed, will cause a high speed transfer of data (1000 characters per second) from the RO to the R/W without printing on paper. If a 00 is set into the block address thumbwheels and the AUTO key is depressed, all data from the present location to an EOR will be duplicated. If a block address is set into the thumbwheels and the AUTO key is depressed, all data from the present location up to but not including that data specified by the block address will be duplicated. When the block address is located, the R/W will write the next sequential block address and stop without duplicating that block of information. Depressing the PARA, LINE, WORD, or CHAR/STOP key will then cause only that

selected portion of the data to be duplicated. If the thumbwheels are set to a block address which is lower than that for the present location, no duplication will take place. The duplication of data will only terminate after all selected conditions have been fulfilled. When the duplication is completed, the system buzzer will sound and the lighted action key will extinguish.

SKIP - This lighted key, when depressed, will cause recorded data, including any encoded functions, to be read without printing or performing the encoded function. This key operates in conjunction with the action keys, i.e., AUTO, PARA, LINE, WORD, and CHAR/STOP.

PLAY - This lighted key, when depressed, selects the Play mode of operation. In this mode, the R/W magnetic tape transport is activated and data is read and printed as commanded by the depression of an action key.

The PLAY key, when used in conjunction with the REC key (dual station systems only) will cause data to be read from the RO and written into the R/W, as well as printed on paper.

When used in conjunction with the ALT RDR key (dual station systems only), data will be read from the RO and printed on paper. The system must not be in the Record mode for this operation to function.

3.1.3 Action Keys

Those keys, highlighted in Figure 3-3, are classified as action keys since they cause an action, when depressed.

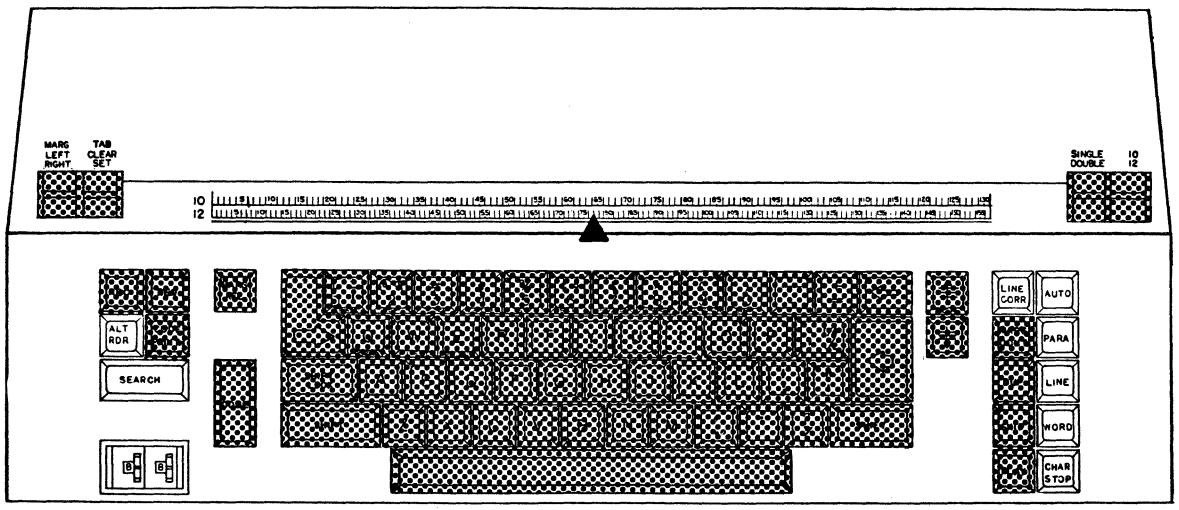


Figure 3-3. Action Keys

SEARCH - This lighted key, when depressed during the Play mode, will actuate the loaded tape transport and automatically search the tape for a block address which corresponds to the particular block address set into the thumbwheels. The key will remain lighted until the block address is located and then it will extinguish.

When used in conjunction with the ALT RDR key (dual station systems only) during an RO to R/W transfer, the RO tape will be searched for the block address.

Block Address Thumbwheels - These thumbwheels are used to set a two-digit block address ranging from 00 to 99. Since block addresses are sequentially prerecorded into the tape, particular segments can easily be searched or located.

ALT RDR - The alternate reader key (dual station systems only), when depressed during the Play mode, will cause the reading of information from the tape to be switched from the R/W (standard reader in the Play mode) to the RO. A subsequent depression will cause the reading to be returned to the R/W. The Active READ Station Indicator associated with the selected reader, will light when the reader is activated. These indicators are located on the console.

LINE CORR - The line correct key, when depressed during the Record mode, will cause that line of information presently being stored in the buffer to be cleared, and the carrier returned to the left-hand margin position without indexing. The information will not appear on the tape, nor will the tape be erased or rewound, since that line was not transferred from the buffer onto the tape. Each subsequent depression will merely rewind the tape and reverse vertical index the paper feed to the beginning of each previous line. The tape, in this case, will be erased and rerecorded as the operator retypes over any portion of the existing information.

AUTO - This lighted key, when depressed during the Play, Revise, Skip, or Duplicate modes, will cause the system to play and print, skip, or duplicate a single block of information. These blocks are separated by prerecorded, sequential block addresses.

During operation in the Duplicate mode, all data up to but not including that data specified by the block address, set into the block address thumbwheels, will be duplicated. If the thumbwheels are set to 00, the remainder of the tape will be duplicated.

PARA - This lighted key, when depressed during the Play, Revise, Skip, or Duplicate modes, will cause the system to play and print, skip, or duplicate a single paragraph of information. Two consecutive carrier returns, a carrier return and a required tab, or a required carrier return will signal the end of a paragraph and stop the operation.

LINE - This lighted key, when depressed during the Play, Revise, Skip, or Duplicate modes, will cause the system to play and print, skip, or duplicate a single line of information. A carrier return, whether a required one or not, signals the end of a line and stops the operation.

WORD - This lighted key, when depressed during the Play, Revise, Skip, or Duplicate modes, will cause the system to play and print, skip, or duplicate a single word including all punctuation, spaces, tabs, and carrier returns that follow it up to the next word. A space or a carrier return, whether a required one or not, signals the end of a word and stops the operation.

CHAR/STOP - This key, when depressed during the Play, Revise, Skip or Duplicate modes, will immediately stop the respective operation. Each subsequent depression will cause a single character, punctuation, space, tab, carrier return, etc. to be played and printed, skipped, or duplicated.

3.1.4 Encoded Function Keys

Those keys, highlighted in Figure 3-4, are classified as encoded function keys since they encode and record onto the tape those codes which control system functions during playback. These codes will not print on the paper unless the CODE PRINT key is depressed.

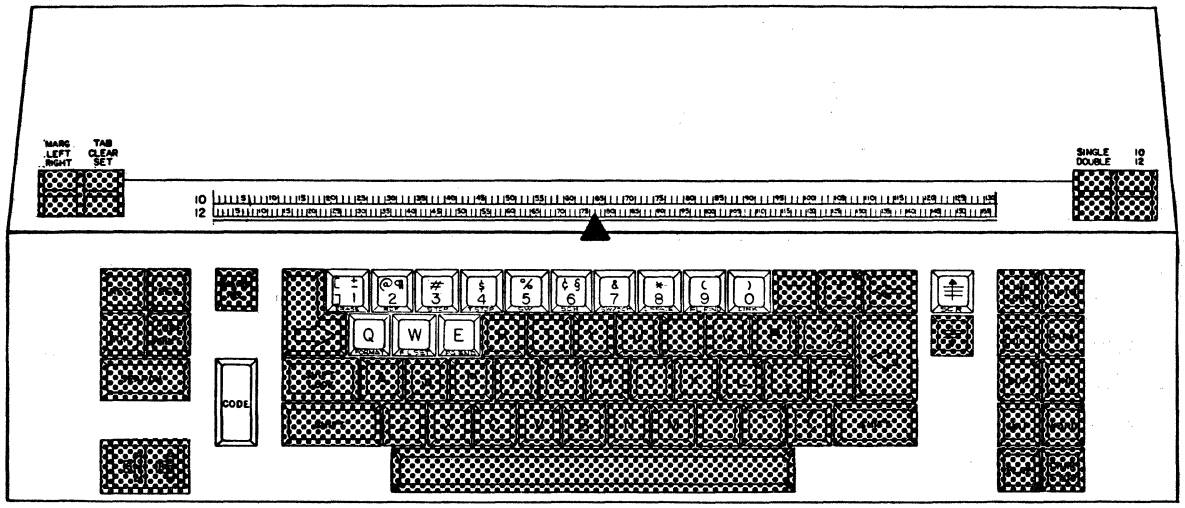


Figure 3-4. Encoded Function Keys

CODE - This key, when held depressed together with any one of the following keys during the Record mode, will cause the system to encode and record onto the tape the code for a particular system function. Table 3-2 lists those keys that will encode functions.

Table 3-2. Encoded Function Keys

KEY	CODE	ENCODED FUNCTION
REF	⁄2	Reference
STOP	⁄3	Stop
TSTOP	⁄4	Transfer Stop
SW	⁄5	Switch
SCH	⁄6	Search
SW/SCH	⁄7	Switch and Search
L SPACE	⁄8 or ⁄9	SINGLE/DOUBLE Line Space
FL FIND	⁄9	First Line Find
LINK	⁄0	Track Link
FORMAT	⁄Q	Format
FL SET	⁄W	First Line Set
PG END	⁄E	Page End (line count)

The following keys and levers, when depressed or set together with the CODE key during the Record mode, will encode and record a required function onto the tape. Refer to the Operating Instructions referenced in paragraph 3.2 of this manual for details on the use of each.

Space Bar	Backspace	Reverse Index
Carrier Return	Forward Index	Hyphen
Tab		

ERASE - This key, when depressed together with the CODE key, will put the system into the Record Mode (REC key lights) and the automatic search for an EOR will be bypassed. In this way, a prerecorded tape can be erased and rerecorded from its beginning rather than from an EOR.

REF (2) - This key, when depressed together with the CODE key during the Record mode, will encode and record a reference code (2) together with a sequential block address onto the tape. The block address counter in the R/W will also be incremented by 1. These block addresses are used to separate particular segments of information on the tape.

STOP (3) - This key, when depressed together with the CODE key during the Record mode, will encode and record a stop code (3) onto the tape. This code, when read during playback, will automatically stop both printing and playback to permit the operator to type in additional information not found on the tape, such as a name, date, etc.

T STOP (4) - This key, when depressed together with the CODE key during the Record mode, will encode and record a transfer stop code (4) onto the tape. This code, when read during playback, will cause a function which is identical to that of the stop code. The difference between the two is that this code must be used when transferring information in the Record mode from the RO to the R/W, since it will transfer onto the new tape and the stop code will not.

SW (5) - This key, when depressed together with the CODE key during the Record mode, will encode and record a switch code (5) onto the tape. This code, when read during playback, will cause the system to switch from one reader to the other. This enables the operator to automatically combine and print information prerecorded on two different tapes.

SCH (6) - This key, when depressed together with the CODE key during the Record mode, will encode and record a search code (6) onto the tape. A two-digit block address must also be entered from the keyboard at this time. The code together with the block address, when read during playback, will cause the system to automatically search to the prerecorded block address. In this way, particular segments of information can be played back irrespective of their chronological order on the tape.

The direction of the search (forward or reverse) is determined by the designated block address as compared to the current block address. An automatic forward search is actuated when the tape is at its beginning and an automatic reverse search is actuated when the tape is at its end or at an EOR.

SW/SCH (7) - This key, when depressed together with the CODE key during the Record mode, will encode and record a switch and search code (7) onto the tape. A two-digit

block address must also be entered from the keyboard at this time. The code together with the block address, when read during playback, will cause the system to automatically switch from one reader to the other and search the active reader for the prerecorded block address. In this way, an operator can automatically combine and print information prerecorded on two different tapes irrespective of their chronological order on the tapes.

L SPACE (ß or ÿ) - This key, when depressed together with the CODE key during the Record mode, will encode and record a line space code (ß for single space and ÿ for double space) for the present setting of the SINGLE/DOUBLE Line Space Lever. The code for the setting of the Line Space Lever, when read during playback, will automatically select the prescribed line spacing, regardless of the present position of the Line Space Lever.

FL FIND (Ø) - This key, when depressed together with the CODE key during the Record mode, will encode and record a first line find code (Ø) onto the tape. When read during playback, this code will cause the paper feed to automatically execute the number of forward vertical index operations specified by the number remaining in the first line counter at that time.

LINK (Ø) - This key, when depressed together with the CODE key during the Revise mode, will encode and record a track link code (Ø) onto the tape. This code, when added as the first character to a prerecorded line, will cause that line to be automatically skipped during playback. When added within a prerecorded line, all of the characters in that line which follow the track link code will be automatically skipped during playback.

SCR - This key, when depressed together with the CODE key during the Revise mode, will cause the carrier to return without recording the contents of the buffer. The special carrier return will be added to the buffer contents and recorded with the line. Since a special carrier return consumes considerably less tape than a regular carrier return, its function becomes especially useful when typing a large number of short lines, such as typing a mailing list.

FORMAT (Ø) - This key, when depressed together with the CODE key during the Record mode, will encode and record a format code (Ø) onto the tape. The new tab or margin settings must follow the format code. In this way, the information read during playback will have those tab and margin settings recorded.

FL SET (Ÿ) - This key, when depressed together with the CODE key, sets the first line counter. A two-digit numeric code, which corresponds to the number of forward vertical index operations required to go from the first line on one form to the first line on the next, must also be entered from the keyboard at this time. This number is stored in the first line counter and as the operator types or plays back information, the number of carrier returns or forward indexes is subtracted from the stored number. When the first line find code (Ø) is read during playback, the paper feed will automatically execute the number of forward vertical index operations specified by the number remaining in the first line counter at that time. The first line counter will then be reset to the value entered from the keyboard.

PG END (É) - This key, when depressed together with the CODE key, sets the carrier return line counter. A two-digit numeric code, which corresponds to the maximum number of lines to be printed on the paper, must also be entered from the keyboard at this time. This number is stored in the carrier return line counter and as the operator

types or plays back information, the number of carrier returns or forward indexes used is subtracted from the stored number. When the number of lines typed or played back equals the number entered from the keyboard, the counter will equal zero. This will cause the keyboard and the tape playback to lock until the CHAR/STOP key is depressed. When depressed, the counter will reset to the value entered from the keyboard and the keyboard and play back will unlock.

The carrier return line counter is automatically set to 00 when power is first turned on. The number 00 permits the counter to free run and thus bypasses the line counter function. It should be reset, by entering Ł 00 from the keyboard, whenever this function is no longer desired.

3.1.5 Console Controls and Indicators

The console controls and indicators, shown in Figure 3-5, apply system power, cause the tape in both tape transports to be rewound, and provide system status indications.

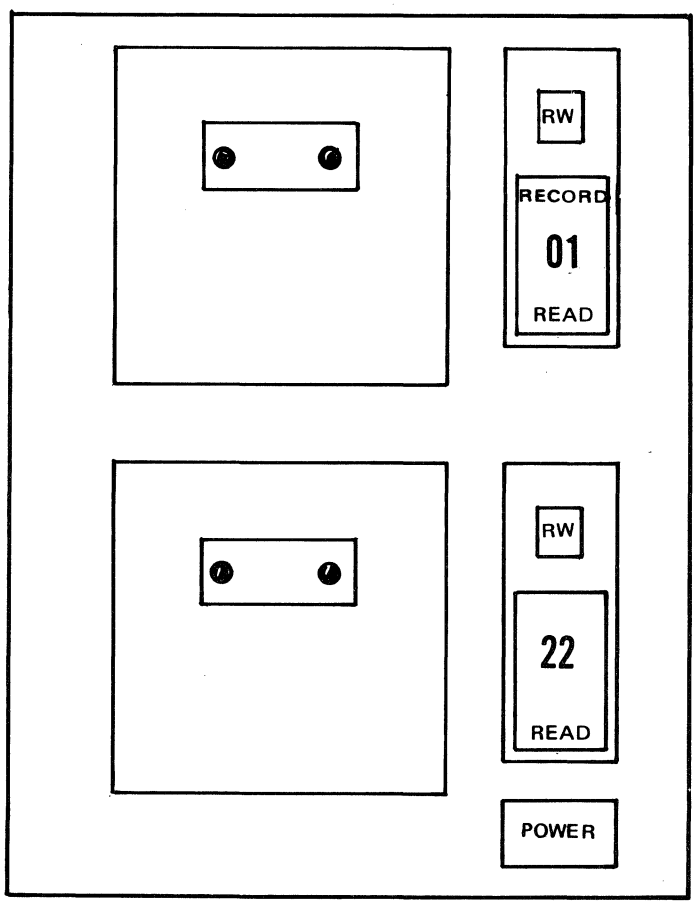


Figure 3-5. Console Controls and Indicators

Rewind/Eject (RW) - These two pushbuttons, when depressed, will cause the associated tape to be rewound. When fully rewound, the door to the associated tape transport will pop open to provide easy access to the cassette.

Block Address Displays - These two two-digit displays indicate the present block address being read from the tape on the associated tape transport. During the Record mode, the R/W (upper tape transport) will display the block address presently being recorded. When neither condition exists, the displays remain blanked.

Active RECORD Station Indicator - This indicator will illuminate when the R/W tape transport is conditioned to record, otherwise it will remain blanked.

Active READ Station Indicators - These two indicators will illuminate when the associated tape transport is conditioned to read, otherwise they will remain blanked.

POWER - This butterfly switch, when depressed, causes primary power to be applied to the system.

3.1.6 Alarms

There are four basic system error conditions that cause both visual and audible alarms. These include:

- Write errors
- Read errors
- Search errors
- Revise errors

Write Error Alarms

The system will attempt to write a line of information three times on two different areas of tape. If unsuccessful, the system will lock, an alarm will sound, and the REC key will flash. This condition can be cleared by depressing the CHAR/STOP key. A new tape should then be installed in the R/W and the information should be retyped.

Another write error condition exists near the end of the tape (NEOT) and at the actual end of the tape (EOT). When either of these conditions is encountered; an alarm will sound, the tape will advance beyond the NEOT hole and write an EOR, then back up to the end of the last recorded line and stop. The REC key will also extinguish.

Read Error Alarms

The system will attempt to read a line of information three times. If unsuccessful, the keyboard will lock, an alarm will sound and the PLAY key will flash. This condition can be cleared by depressing the CHAR/STOP key. This will clear the buffer and the system and permit the operator to retype the line manually, if so desired. The playback is then free to continue.

Search Error Alarms

An unsuccessful search is indicated to the operator by the system alarm together with a flashing SEARCH key. If an EOR or the end of tape is encountered during a forward search without locating the block address, a reverse search will automatically be initiated unless the block address being searched is greater than the address of the EOR.

In this case the system would lock, an alarm would sound, and the SEARCH key would flash. This condition can be cleared by depressing the CHAR/STOP key.

Revise Error Alarms

When operating in the Revise mode, the following error conditions will cause an alarm to sound.

- The Duplicate or Margin Control mode is selected.
- A search is initiated.
- The Rewind (RW) pushbutton is depressed.

When an EOR is encountered, the Revise mode will be turned off and the REV key will extinguish.

When the number of characters being added to an existing line exceeds 50, the keyboard will lock, an alarm will sound, and the REV key will flash.

These conditions can be cleared by depressing the CHAR/STOP key.

3.2 OPERATING INSTRUCTIONS

The step-by-step operating instructions for the basic operations, modes, actions, and encoded functions of the system are presented in two separate volumes; one for the dual station system and the other for the single station system. Each has been prepared in such a way that a typical typing problem, which may arise during the course of an average day at the office, is first outlined. Step-by-step instructions then provide a solution for each problem. Figures showing the location of those keys used in each solution and examples of what to expect from the system are used extensively throughout both books. This problem/solution technique uses the building block approach in which the basics are first taught. These basics are then used as a foundation from which the operator can build or develop a further understanding for the system's many applications. Many of these applications are explained in detail in the later sections of both books.

CHAPTER 4

THEORY OF OPERATION

4.1 FUNCTIONAL DESCRIPTION

The dual station Magnetic Tape Word Processor is an electronic system used for automatic typewriting. A full duplex keyboard and an electronic, servo-controlled printer form the typewriter unit. These are both housed in an attractive case suitable for secretarial use. The electronic circuitry which controls each system function, the two magnetic tape transports (one in a single station system), and the power supplies are contained in a compact console. See Figure 4-1. Twenty-seven printed wiring assemblies (PWA's) comprise the electronic circuitry of the console. Twenty of these are contained in the electronic card cage. Each is listed in Table 4-1 by numerical location. There are two PWA's associated with each magnetic tape transport. These are the Tape Read/Write or Tape Read Only and the Motor Control PWA's which are mounted into the sockets located just behind the respective transport. There is one PWA associated and located with each of the two block address displays. The remaining PWA is the DC Regulator assembly which is associated and located with the DC power supply. Refer to Table 4-2.

Information, in the form of a modified 8-bit ASCII code, is transmitted from the Keyboard through the Keyboard Interface PWA 3 onto the data bus during the Record mode of operation. Refer to the Block Diagram shown in Figure 4-2. The information is moved to the Microprocessor, processed, and routed to a Buffer I/O assembly via the data bus to await distribution. The processed information is then distributed through the Printer Interface PWA 1 to the printer during the Play mode or through the tape control circuitry to tape storage during the Record mode. The various functions of each subsystem or printed wiring assembly are discussed in the following pages.

4.2 MICROPROCESSOR

The heart of the electronic system is the Microprocessor. This unit is comprised of a Read Only Memory (ROM) Program, a ROM Address Register, a Return Address Register, a General Purpose (GP) Register, a Main (M) Register, and an Arithmetic Logic Unit (ALU). Together these circuits function to process information from the keyboard, buffers, magnetic tape storage, etc. Each of the circuits is discussed in the following paragraphs.

4.2.1 Read Only Memory (ROM) Program

The Read Only Memory (ROM) Program (sockets 5 through 8) is comprised of 4096 sixteen-bit instruction words. Each of these words designates a specific system operation. The sixteen bits from ROM (RØ through R15) are buffered by the circuitry on the Keyboard Interface (socket 3) and the Miscellaneous, Clock and IC PWA's (socket 4) to produce the buffered ROM bits BØ through B15.

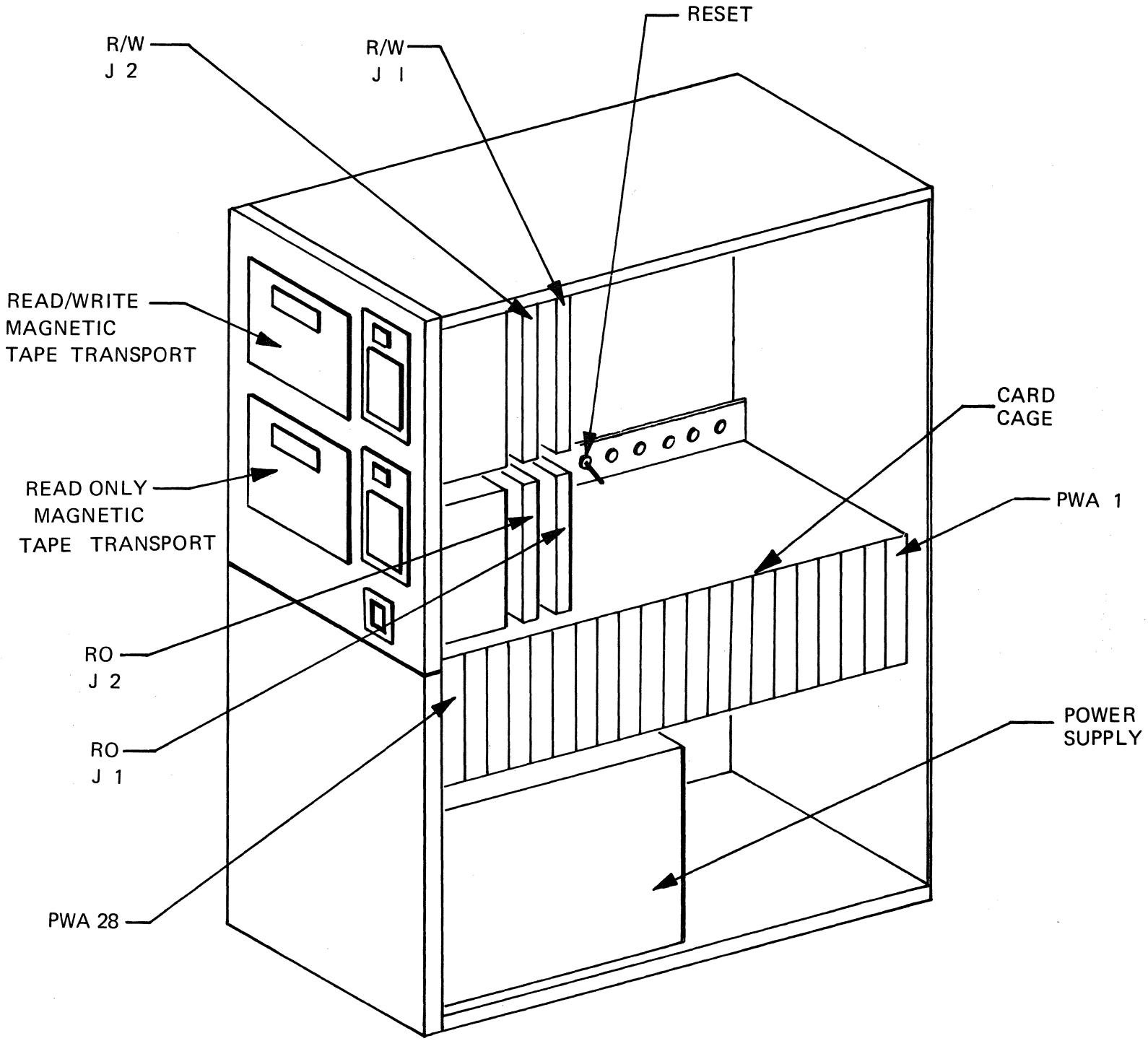


Figure 4-1. Console, Right-Hand Interior View

Table 4-1. Card Cage PWA's

PWA	TITLE	PART NUMBER
1	Printer Interface	75013805
2	Not Used	--------
3	Keyboard Interface	75013800
4	Miscellaneous, Clock, and I. C.	75013801
5	ROM Program	75014400
6	ROM Program	75014400
7	ROM Program	75014400
8	ROM Program	75014400
9	ROM Address Register	75013749
10	Return Address Register	75013750
11	Main and General Purpose Register	75013747
12	Arithmetic Logic Unit	75013748
13	Buffer I/O (Read Only)	75013735
14	Buffer Control (Read Only)	75013563
15	Buffer I/O (Read/Write)	75013735
16	Buffer Control (Read/Write)	75013563
17	Tape Control (Read/Write)	75013733
18	Read Decode (Read/Write)	75013731
19	Write Encode (Read/Write)	75013732
20	Tape Control (Read Only)	75013733
21	Read Decode (Read Only)	75013731
22	Not Used	--------
23	Not Used	--------
24	Not Used	--------
25	Not Used	--------
26	Not Used	--------
27	Programmed Diagnostic Aid	00015500
28	Programmed Diagnostic Aid	00015500

Table 4-2. Other Console PWA's

PWA	TITLE	PART NUMBER
R/W J1	Motor Control	75013804
R/W J2	Tape Read/Write	75013564
RO J1	Motor Control	75013804
RO J2	Tape Read Only	75013564
R/W Display Panel	Display Panel	75013809
RO Display Panel	Display Panel	75013809
Power Supply	DC Regulator	75013806

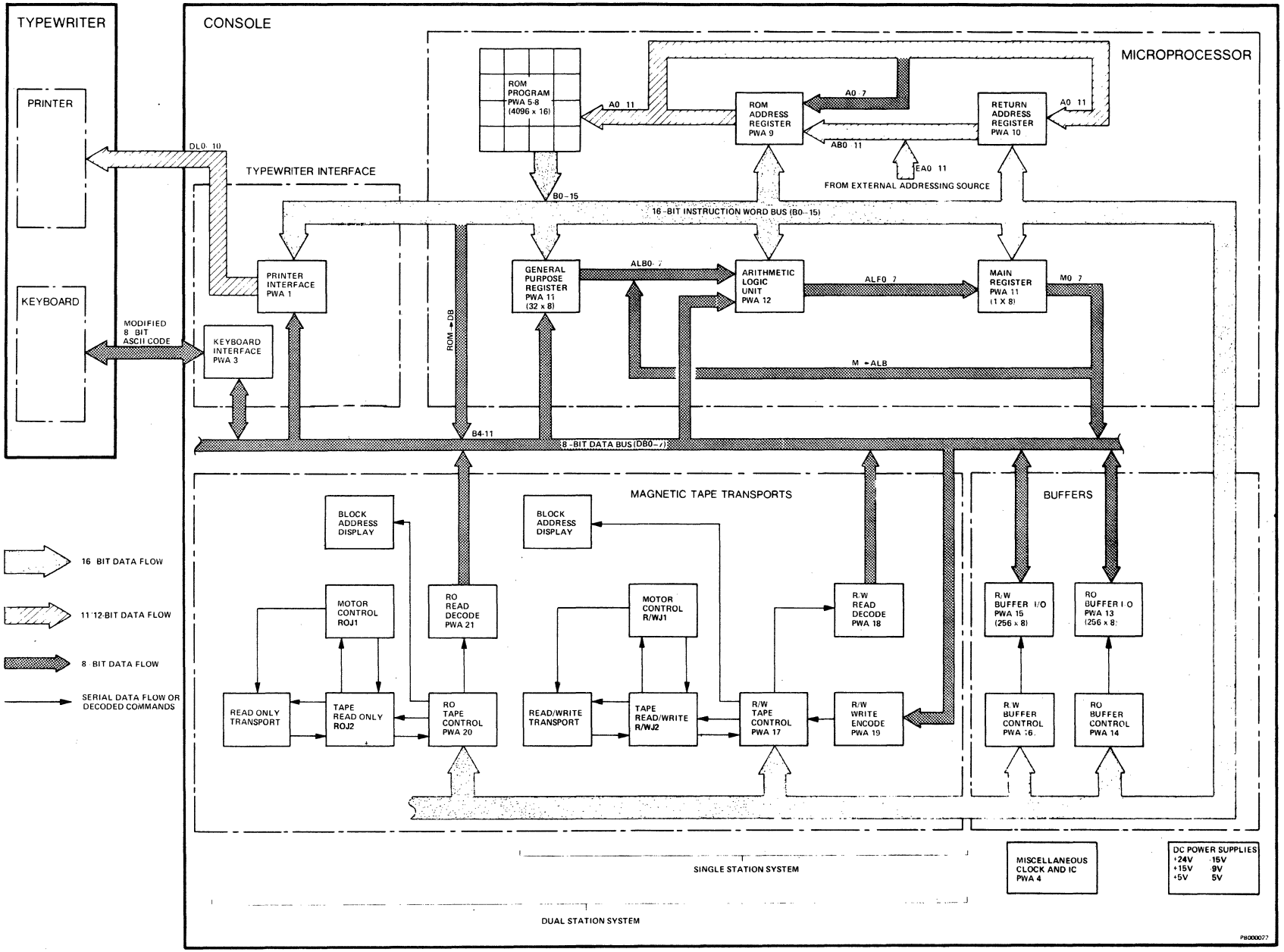


Figure 4-2. Detailed System Block Diagram

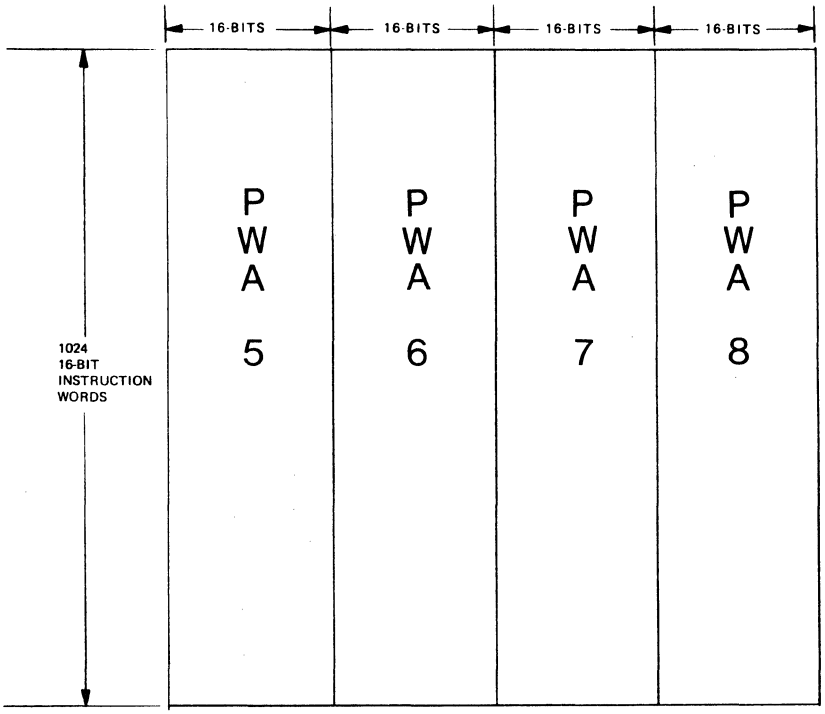


Figure 4-3. K-Page Memory Structure

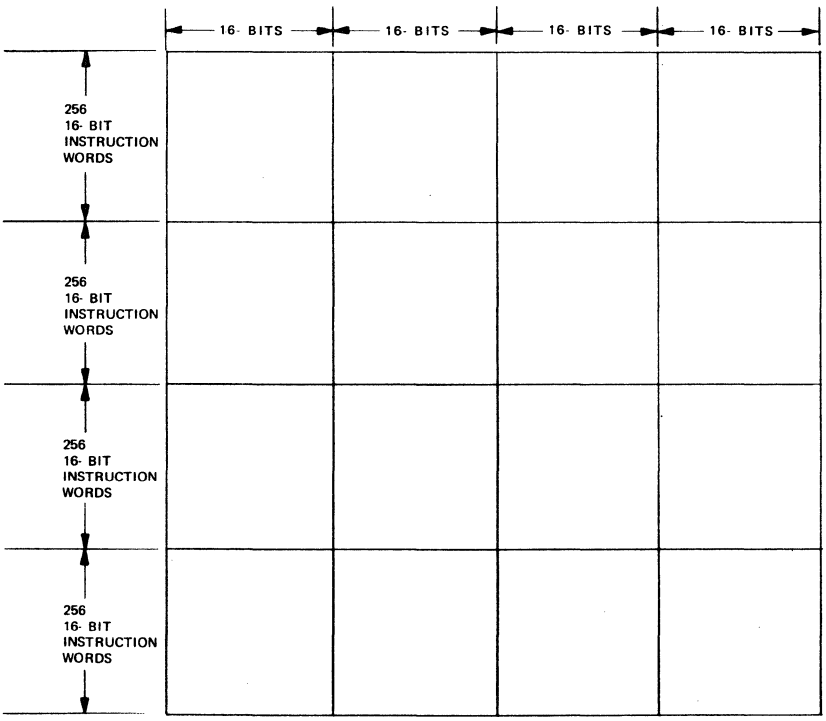


Figure 4-4. Major-Page Memory Structure

ROM Structure

The overall memory structure of the ROM is configured into four sections, one section on each printed wiring assembly. Each section or page stores 1024 of these preprogrammed 16-bit instruction words, therefore, each is referred to as a K-page (1000=1K). See Figure 4-3.

Each K-Page is then subdivided into four sections, called Major-Pages. Thus, there are four Major-Pages to every K-Page or 16 Major-Pages in all. Each Major-Page contains 256 of the 16-bit instruction words. See Figure 4-4.

Addressing

In order to select each of the 4096 sixteen-bit instruction words from ROM, a 12-bit address word is required. The two upper order bits (A10 and A11) of each address word determines which K-Page will be addressed, bits A8 and A9 determine the Major-Page address, and the eight low order bits (AØ through 7) determine the address of each individual word stored in the Major-Page. Figure 4-5 illustrates the format of the 12-bit address word.

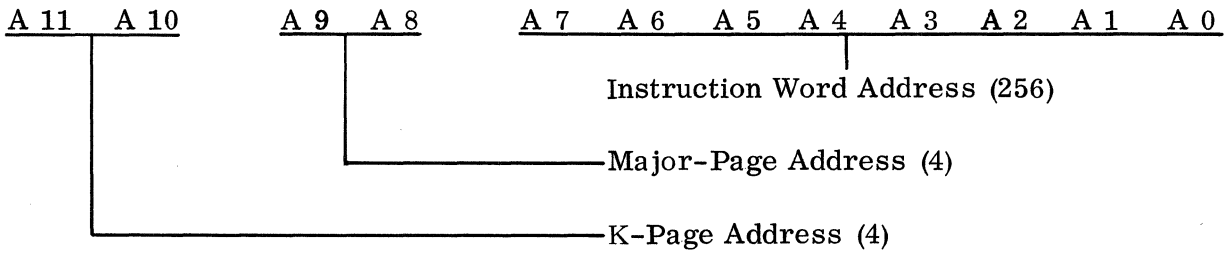


Figure 4-5. 12-Bit Address Word Format

The number shown in parentheses indicates the total number of address combinations possible (4 x 4 x 256 = 4096).

4.2.2 ROM Address Register

The ROM Address Register (socket 9) forms the 12-bit address word used to address each instruction word from ROM. Figure 4-6 illustrates the four major elements that comprise the Register. These elements include the Multiplexer, Adder, Next Absolute Address Register, and the Output Address Register. The Multiplexer is used to select either the 12 low order "B" bits from ROM, the 12 "AB" bits from the Return Address Register (socket 10), or the 12 "EA" bits from an external addressing source. The Adder sums the information present on its input lines and adds a one to the resultant sum if the carry-in input is enabled. The output from the Adder is the next absolute address. This address is then parallel loaded into the 12 flip-flops that constitute the Next Absolute Address Register. From there the address is clocked into the Output Address Register, another group of 12 flip-flops, out onto the address lines.

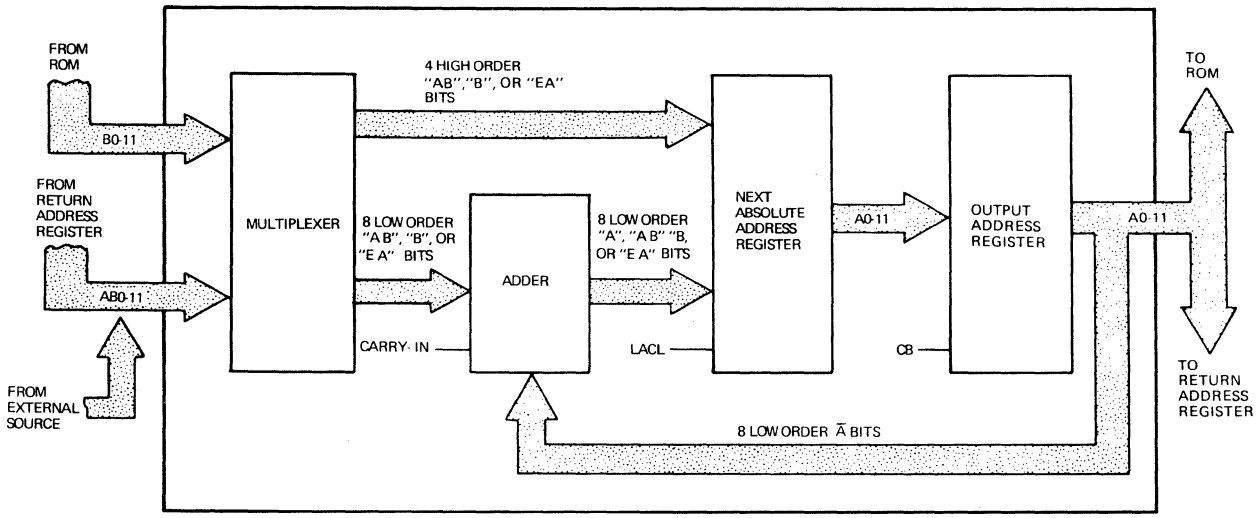


Figure 4-6. ROM Address Register

Combined, these four major elements and the associated gating circuitry provide the means by which the sequential, intrapage branch, extra page branch, extra page branch and return, and external addresses are developed. The gating circuits decode the information contained in the ROM word to determine which one of the five basic addresses will be developed. Typically, the ROM Address Register forms sequential addresses unless otherwise directed by the decode of the ROM word.

4.2.3 Return Address Register

The Return Address Register (socket 10) is used to retain up to four of the 12-bit ROM addresses which consists of bits AØ through A11. These addresses are stored whenever an extra page jump and return operation is commanded. Each is stored, one after another, in a first-in last-out fashion. Therefore, the last address stored will be the first address used. Each of the 12 "A" bits of the present address is stored in separate 4-bit Right-Shift Left-Shift registers. Clocked commands decoded from ROM bits determine whether the address is pushed-up or pushed-down in the registers. The 12-bit return address pushed-up from the registers is applied on the AB lines to the ROM Address Register.

The $\overline{\text{JUMP}}$ and $\overline{\text{RET}}$ commands used in conjunction with ROM addressing are also decoded from ROM bits on this PWA.

4.2.4 General Purpose (GP) and Main (M) Registers

The General Purpose (GP) and Main (M) Registers (socket 11) are used in conjunction with the Arithmetic Logic Unit (socket 12). The GP-Register consists of the G and H registers each having a storage capability of sixteen 8-bit words. Information is transferred from the data bus to either a G or an H register. The status of ROM bits B4 through B7 determines which of the sixteen individual registers will accept the data. ROM bit 14 determines whether the information will be stored in a G or an H register. Information is taken from a G or an H register on the eight ALB lines and applied to the input of the ALU. The processed information from the ALU is transferred to the M-Register on the eight ALF lines. The storage capability of the M-Register is one 8-bit word. M-Register output is coupled back through a multiplexer to the ALB lines. When an M⟶ALB command is decoded from a ROM instruction word, the multiplexer is enabled to permit the data stored in the M-Register to be transferred to the ALU on the ALB lines. M-Register output is multiplexed onto the data bus when the $\overline{\text{DB⟶M}}$, $\overline{\text{0⟶GP}}$, and $\overline{\text{ROM⟶DB}}$ commands are all high.

Another multiplexer provides the means to transfer an 8-bit constant stored in ROM to the data bus. This multiplexer is enabled by a ROM⟶D B command which is decoded from a ROM word. ROM bits B4 through B11 are then transferred to the data bus to provide the constant.

4.2.5 Arithmetic Logic Unit (ALU)

The Arithmetic Logic Unit (socket 12) performs all of the arithmetic and logic functions used by the system. The device accepts 8-bits of data directly from the data bus on the D B lines or from the GP-Register or M-Register on the ALB lines. ROM bits are decoded to produce the ALU operation commands S0, S1, S2, S3, Ci, and ALM. These commands select the ALU function. The output of the ALU is coupled to the M-Register by the eight ALF lines.

ROM bits are also decoded to produce the $\overline{\text{BRANCH}}$ command used in ROM addressing.

4.3 BUFFER I/O AND BUFFER CONTROL

Two Buffer I/O (sockets 13 and 15) and associated Buffer Control (sockets 14 and 16) printed wiring assemblies provide temporary system storage. One pair is associated with the Read/Write magnetic tape transport and the other with the Read Only transport. Commands and clock commands, decoded from ROM bits by Buffer Control gating, regulate the bidirectional flow of information between the respective Buffer I/O PWA and the data bus. Circulating buffer storage for up to 256 eight-bit characters, plus buffer timing, phase detection, and status indications are provided on each Buffer I/O PWA. Information from the data bus is applied to the input of a multiplexer and then clocked into a 256-bit shift register for storage. The clocking is accomplished by the two-phase clock circuitry located on each Buffer I/O PWA. Phase detection and buffer running status circuitry is also provided. Information is shifted out of the shift registers onto the data bus through two multiplexers.

4.4 TAPE CONTROL

There are two Tape Control printed wiring assemblies. One is associated with the Read/Write magnetic tape transport (socket 17) and the other with the Read Only transport (socket 20). Both perform identical functions, therefore, both are interchangeable. Serial information (BIØREC) from the Write Encode PWA (socket 19) is buffered and transferred through the PWA to the Tape Read/Write PWA (socket R/WJ2). This function is not used during operations with the Read Only transport. Serial information (BIØREAD) from either the Tape Read/Write (socket R/WJ2) or Tape Read Only (socket ROJ2) PWA's is buffered and transferred through the appropriate Tape Control PWA to the associated Read Decode PWA.

Various transport status conditions are detected by this PWA, i.e. tape at speed ($\overline{\text{TAS}}$), cassette in place ($\overline{\text{CIN}}$), rewind key depressed (KREW), etc.

Transport control commands, i.e. $\overline{\text{FAST}}$, $\overline{\text{RUN}}$, $\overline{\text{CCW}}$, etc. are also developed.

Data bus information used in conjunction with block address displays is latched into flip-flops on the PWA.

4.5 WRITE ENCODE

There is one Write Encode printed wiring assembly (socket 19) associated with the Read/Write magnetic tape transport in either the single or dual station system. Its main purpose is to convert parallel data from the data bus into bi-phase serial data (BIØREC). This processed serial data is applied to the input of the Read/Write Tape Control PWA (socket 17) where it is inverted and transferred to the Tape Read/Write PWA (socket R/WJ2). The least significant bit (DBØ) is written first. When the write data ready (WDR) command goes true, the write cycle begins.

Clock timing for the serializer shift register is derived from CA time through a flip-flop and the modulo 10 counter.

4.6 READ ENCODE

There are two Read Decode printed wiring assemblies. One is associated with the Read/Write magnetic tape transport (socket 18) and the other with the Read Only transport (socket 21). Both perform identical functions, therefore, both are interchangeable. Bi-phase serial data (BIØREAD) read from the tape is converted into parallel data which is put onto the data bus for processing. To differentiate between a "0" or "1", a modulo 225 counter is used. It counts up when the input is high and down when the input is low. Since a "0" remains high for twice as long as it is low, the counter will complete the cycle at a count of approximately 40. A "1" on the other hand, remains high for half as long as it is low, therefore, the resultant count is approximately -40. This is equivalent to approximately +215, since the counter does not count negatively. It simply continues to count down as the count passes through zero, e.g. 1, 0, 255, 254, etc. Refer to Figure 4-7.

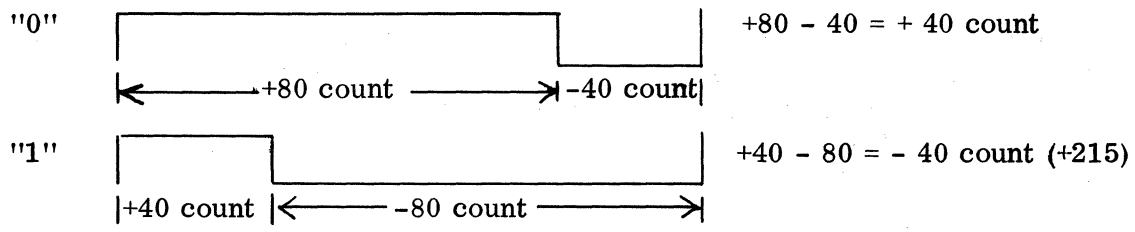


Figure 4-7. Bi-Phase Serial Data

Whenever the count is less than +127 the data is a "0", and when greater than +127 it is a "1". This data output is serially shifted into an 8-bit serial-to-parallel shift register whose outputs are gated onto the data bus whenever the $\overline{RR \longrightarrow DB}$ command goes low.

A digital filter provides noise immunity for the tape-to-circuit interface. Circuits also provide the reverse read capability when the tape is driven by the reverse routine.

4.7 TAPE READ/WRITE AND TAPE READ ONLY

There are two Tape printed wiring assemblies associated with the system. One is located just behind the Read/Write magnetic tape transport in socket R/WJ2 and the other is located just behind the Read Only transport in socket ROJ2. Both perform identical functions, therefore, both are interchangeable. Each provides the read and write circuitry, as well as transport command and status logic circuitry. The write circuitry is not used during operation with the Read Only transport.

4.8 MOTOR CONTROL

There are two Motor Control printed wiring assemblies associated with the system. One is located just behind the R/W magnetic tape transport in socket R/WJ1 and the other is located just behind the RO magnetic tape transport in socket ROJ1. Each provides servo control for its respective transport, as well as servo status indications. Figure 4-8 illustrates the servo loop configured about each motor. As can be seen, drive commands (CCW RUN, CW RUN, FAST CCW, or FAST CW) are applied to the R/W servo loop from the Tape Read/Write PWA or in the case of the RO servo loop from the Tape Read Only PWA. These commands cause a particular drive reference level. The polarity of this reference determines which motor will be driven, while the magnitude determines the speed at which it will run. This reference is summed together with the tachometer feedback signal to provide the servo error signal which drives the inverting amplifier (A). The inverted output from the amplifier drives the clockwise motor driver amplifier (DCW). Once this output has again been inverted, it is used to drive the counterclockwise motor driver amplifier (DCCW). When the input to either driver amplifier goes positive, current is applied to the respective motor. The driver amplifier will remain on during 80 percent of the Main Clock cycle. During the remaining 20 percent of the cycle or approximately one millisecond out of every five, the drive current is shut off, permitting the motor to operate as a tachometer.

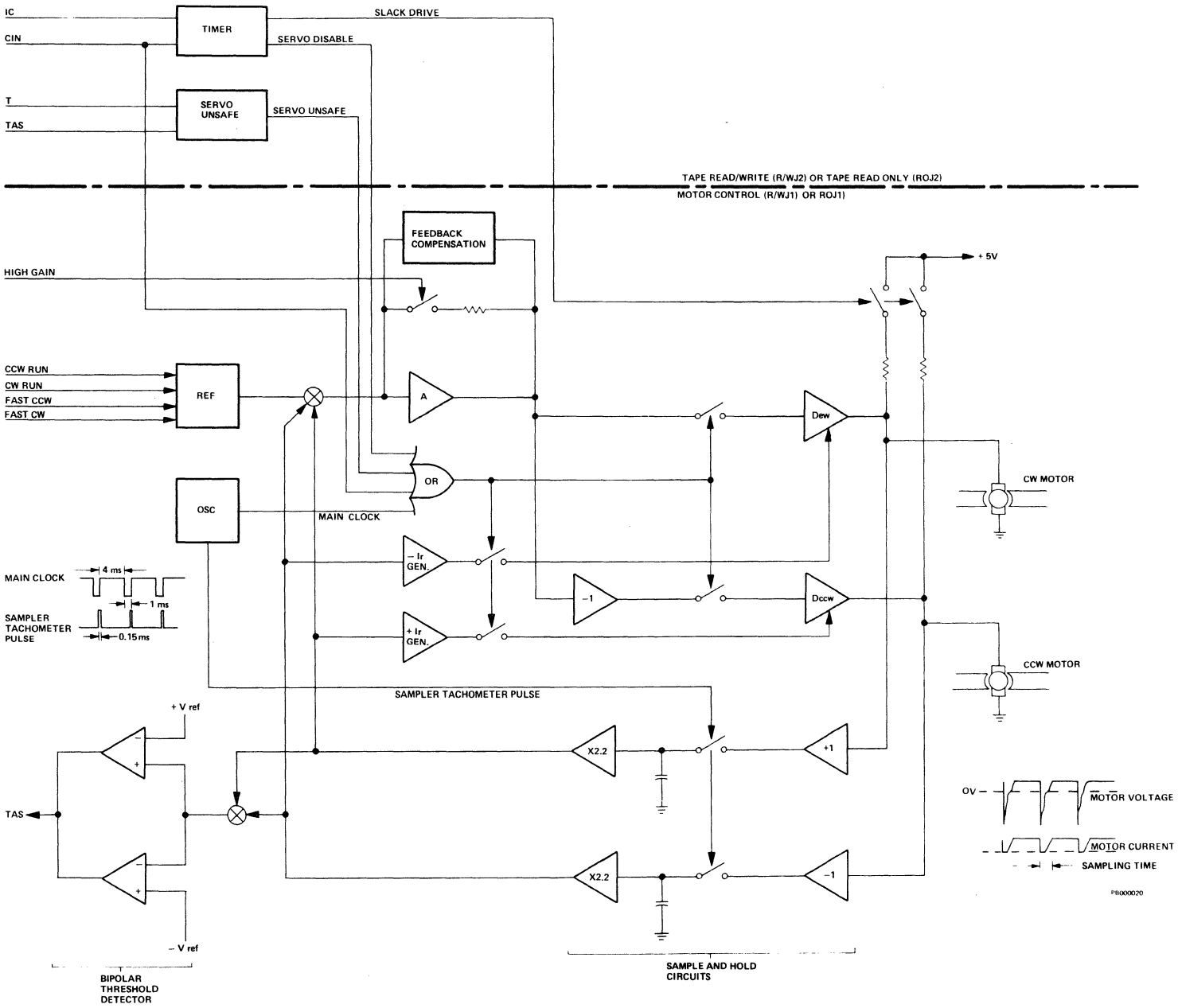


Figure 4-8. Motor Control Block Diagram

A large back voltage will appear across the terminals of the motor due to its self-inductance when operated in this manner. Once this voltage has settled out, the voltage that remains is the back emf of the motor which is proportional to its speed. During this 20 percent time period, the voltage is applied to the respective sample and hold circuit. The switched path is closed by the Sampler Tachometer Pulse and in the last 0.15 millisecond the capacitor is allowed to charge. At the end of this period, current is once again applied to the motor. The output of the sample and hold circuit is filtered and amplified to provide the servo error signal to complete the servo loop. The sample and hold output also supplies drive to the bipolar threshold detector and reverse current generators (Ir). The bipolar threshold detector is used to indicate that the tape is at speed (TAS). This circuit is set to activate at approximately 75 percent of final speed and deactivate at approximately 25 percent of final speed. Current is switched through the driver amplifier to the non-driven motor to provide some tension on the tape. The tachometer feedback signal from the driven motor is applied through a reverse current generator to the non-driven motor to regulate tape tension.

4.9 KEYBOARD INTERFACE

The Keyboard Interface (socket 3) controls the bidirectional transfer of information between the keyboard and the data bus. The eight DBX lines carry information from the keyboard to the input of a bidirectional multiplexer. This multiplexer is enabled by a DBX⟶DB command which permits the transfer of keyboard information to the data bus. When the DBX⟶DB command is not present, information flow is reversed.

The eight low order bits from ROM (RØ through R7) are buffered on this PWA. This provides the buffered bit and its complement (BØ through B7 and $\overline{B\emptyset}$ through $\overline{B7}$) which are used throughout the system to control the various operations.

Various keyboard commands are decoded from ROM bits and keyboard status conditions are detected on this PWA.

4.10 PRINTER INTERFACE

The Printer Interface (socket 1) controls the unidirectional transfer of information from the data bus to the printer. Each of the printer's three basic motions: carrier, print wheel (character), and paper feed, are controlled by the system through the printer interface. These controls are sent down the eleven data lines (DLØ-10). The data lines transmit either the 7-bit ASCII code for the next character to be printed, an 11-bit word which specifies the direction and number of printing spaces to be moved by the carrier (in multiples of 1/60 of an inch), or an 11-bit word which specifies the direction and number of vertical line spaces (indexes) that the paper is to be moved by the paper feed (in multiples of 1/48 of an inch).

Various printer commands are decoded from ROM bits and printer status conditions are detected on this PWA.

4.11 MISCELLANEOUS, CLOCK AND IC

The Miscellaneous, Clock, and IC printed wiring assembly (socket 4) provides the 8-phase system clock, ROM bit buffering, and system status storage. The system clock is comprised of a 4MHz (250 ns) crystal-controlled oscillator and four flip-flops used to divide the output frequency into its eight phases. See Figure 4-9.

The divided output produces the basic 2 microsecond machine cycle used to control the timing of the various system operations.

Buffering of the eight high order bits from ROM (R8 through R15) is perfomed on this PWA. This provides the buffered bit and its complement (B8 through B15 and $\overline{B8}$ through $\overline{B15}$) which are used throughout the system to control the various operations.

System status, such as $\overline{IC}$, $\overline{ST}$, and $\overline{ST}$ is latched into flip-flops and the special address command (SPADDER) is decoded from ROM bits on this PWA. A flip-flop is also provided to determine which transport is the active reader.

4.12 DISPLAY PANEL

A printed wiring assembly is associated and located with each block address display. Its purpose is to convert the modified 8-bit ASCII code for the block address to BCD drive for the block address display. These 8-bits are transferred from the data bus, then stored in registers on the associated Tape Control PWA.

4.13 DC POWER SUPPLIES

The dc power supplies, which are used to furnish all of the dc power for the complete system, are located in the lower portion of the console. All of the voltages used are developed from the three main secondary windings of transformer T1. These three main voltages (+24V, +11V, and -22.5V) are full-wave rectified and filtered. Overload protection for all supplies is provided by the main circuit breaker CB1. In addition, the +24V and -22.5V supplies are each fused at 15 amperes. Further protection for the +11V supply is provided by the dual-section circuit breaker CB1. The +24V supply is used throughout the system. It is also used in conjunction with the +11V supply to develop the regulated +15V and +5V supplies. The -22.5V supply is only used in the development of the regulated -5V, -9V, and -15V supplies. These three main voltages are distributed to the DC Regulator PWA. The regulated outputs from this PWA are then coupled to the power output stages which are located on the heat sink assembly. The voltages developed and used throughout the system are +24 ± 2.6V, +15 ± 0.75V, +5.12 ± 0.05V, -5 ± 0.25V, -9 ± 0.45V, and -15 ± 0.75V. The +5.12V supply is the only supply that requires an adjustment.

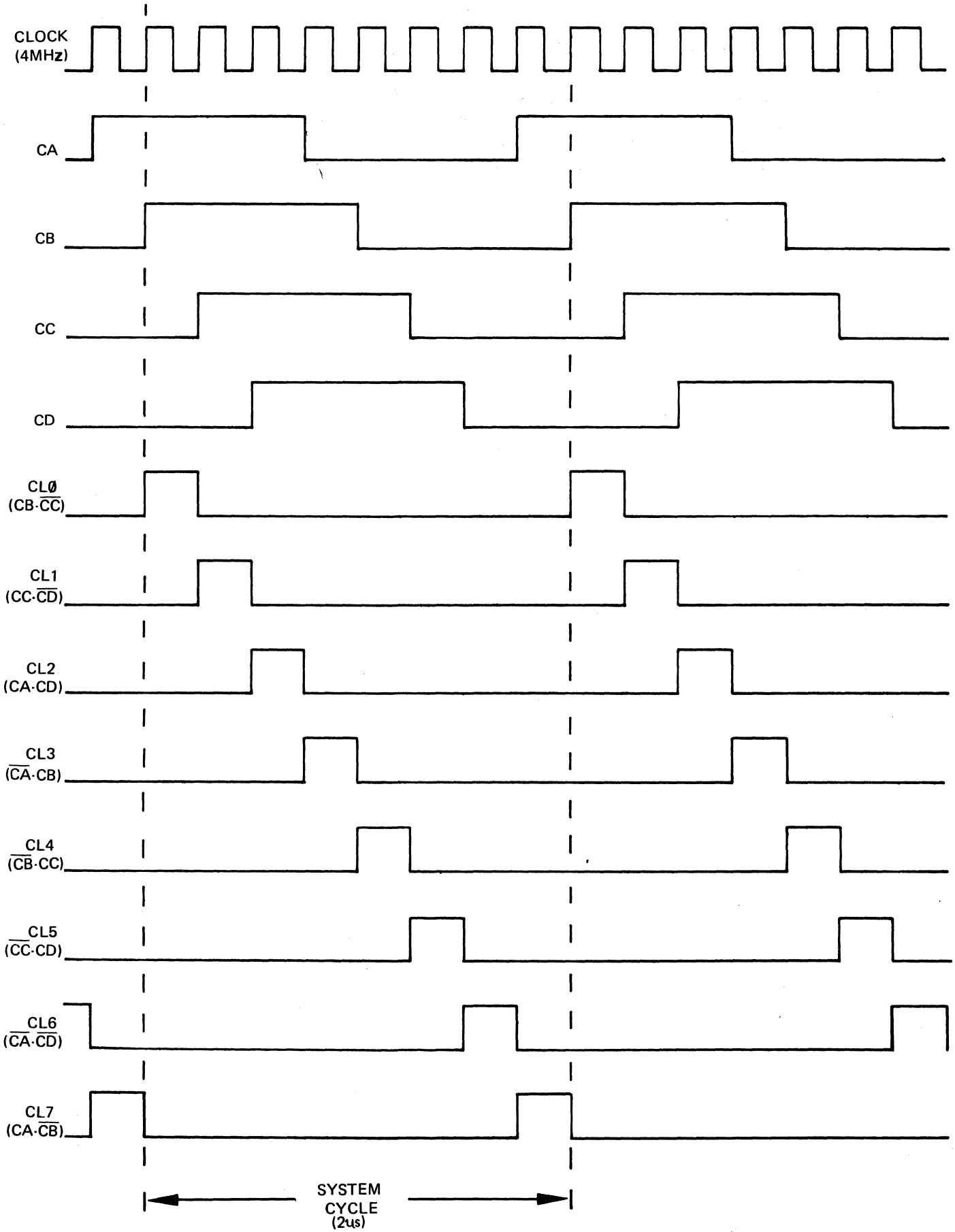


Figure 4-9. System Clock Timing

CHAPTER 5

MAINTENANCE

5.1 SAFETY PRECAUTIONS

Maintenance personnel should use the following safety precautions to prevent injury to themselves or damage to the equipment:

- Keep fingers, hands, or other objects out of the printer while the power is on.
- Use care when working on an operating printer. Remember, the carrier returns at a very high speed and it can inflict a serious injury.
- Potentials up to 115 Vac are present inside the console anytime power is applied.
- Avoid touching or blowing on the read/write or read only heads in the transport. Acids from the skin can etch and ruin these heads. Breathing on them can cause condensation deposits which will disfigure head surfaces.
- Wear safety glasses when applicable.

5.2 MAINTENANCE PHILOSOPHY

5.2.1 Objectives

The prime objective of any maintenance activity is to provide maximum equipment availability to the customer. A preventive maintenance program, properly applied, can assist greatly in achieving this objective, but it is pointless if it fails to increase equipment utilization.

5.2.2 Basic Considerations

The three fundamental considerations in preventive maintenance of mechanical or electromechanical equipment are: INSPECT - CLEAN - LUBRICATE.

Visual observation is the Service Engineer's most valuable preventive maintenance tool. Most mechanical equipment failures will have given visual indication of their presence long before the actual failure occurs. It is, therefore, left to the awareness and perception of the Service Engineer to detect these failures before they occur.

NOTE: Do not perform more than the recommended preventive maintenance on equipment that is operating satisfactorily. Also, do not disassemble equipment in an attempt to locate a potential failure.

5.3 TOOLS AND SERVICING AIDS

This section lists those special single-purpose tools and test equipment used for servicing the system. Refer to the parts catalog for a complete list of recommended tools and ordering information.

5.3.1 Tools

The following is a listing of all special single-purpose tools required for servicing and maintaining the system:

Extender Card with Ground Plane
Card Extractor
Speed setting Cassette 1600 FCPI
E-Z Hook DMM leads

Standard Xerox tool kit
Alcohol 90% Isopropyl
Lint free Q-tips

Cassette, Motor, and Sensor Adjustment Tool P/N 88016036
Motor Positioning Insert P/N 70015833
I.C. Clip
Flush cutting pliers 45°
(Hunter Tools No. ATIAEL)
Soldapullt (Desoldering tool)
Scratch cassette

5.3.2 Test Equipment

The following defines both the standard and special purpose test equipment required for servicing and troubleshooting.

Digital Multimeter (DMM)

A Weston Model 4440 Digital Multimeter or an equivalent is the only item of standard test equipment required for servicing. DMM requirements are not critical, but the meter selected should be of sufficient quality to meet the following minimum range and accuracy specifications:

AC

199.9 m V ± 0.5%	10 MΩ input impedance
1.999 V ± 0.5%	10 MΩ input impedance
19.99 V ± 0.5%	10 MΩ input impedance
199.9 V ± 0.5%	10 MΩ input impedance
999V ± 0.5%	10 MΩ input impedance

DC

199.9 m V ± 0.3%	50 MΩ input impedance
1.999 V ± 0.3%	500 MΩ input impedance
19.99 V ± 0.3%	10 MΩ input impedance
199.9 V ± 0.3%	10 MΩ input impedance
999 V ± 0.3%	10 MΩ input impedance

Resistance

199.9 Ω ± 0.5%
1.999 KΩ ± 0.5%
19.99 KΩ ± 0.5%
199.9 KΩ ± 0.5%
1.999 MΩ ± 0.5%

Programmed Diagnostic Aid (PDA)

A special purpose test unit, the Programmed Diagnostic Aid (PDA) P/N 00015500 is a compact, stored-program diagnostic unit used to service the Microprocessor and its peripherals. It is designed to plug directly into sockets 27 and 28 of the card cage. All system interfacing and DC power for the PDA are provided through these connections. The self-contained unit, through its array of front panel switches and indicators, provides the means by which the integrity of the system can be verified. Diagnostic routines, stored in the read only memory portion of the PDA, permit the Service Engineer to check data flow within the system. These routines begin by testing the system ROM. One by one, the contents of each Major-Page is checked. Failure to pass any one of the sixteen Major-Page checks signifies a defective system ROM. Once proper system ROM operations have been established, the program stored in the PDA's 1K of ROM can be substituted to exercise the Microprocessor through all of its arithmetic and logic functions. Through the use of this technique, a malfunction within the Microprocessor can be diagnosed to a single PWA, in nearly all cases. Once the integrity of the Microprocessor has been ascertained, the various peripherals attached to it via the data bus are tested. The printer is tested for correct character printing and its response to control commands while the keyboard is tested for proper character coding. The two system buffers and the magnetic tape transports are also tested and malfunctions are diagnosed by the PDA. Some service adjustments required by the various peripherals are performed through the use of the PDA's diagnostic routines.

PDA Controls and Indicators

The function of each front panel control and indicator is described in the following paragraphs. Refer to Figure 5-1 for the location of each.

(1) DISPLAY - three-position toggle switch used to select the type of data displayed by the MODULE ADDRESS and/or Data/Address Bit Indicators.

When set to ROM DATA, the state of each bit in the 16-bit instruction word is displayed. The four upper order bits (B12 through B15) that form the module address are displayed by the MODULE ADDRESS Bit Indicators (12 through 15). The twelve low order bits (B0 through B11) that supply data are displayed by the Data/Address Bit Indicators (0 through 11).

When set to ADDR REG, the state of each bit in the 12-bit address is displayed by the Data/Address Bit Indicators (0 through 11). Bit Indicators 10 and 11 display the K-Page address, 8 and 9 display the Major-Page address, and 0 through 7 display the address of the individual word stored in the Major Page.

When set to MAIN REG, the state of each bit on the data bus is displayed by the Data/Address Bit Indicators (0 through 7).

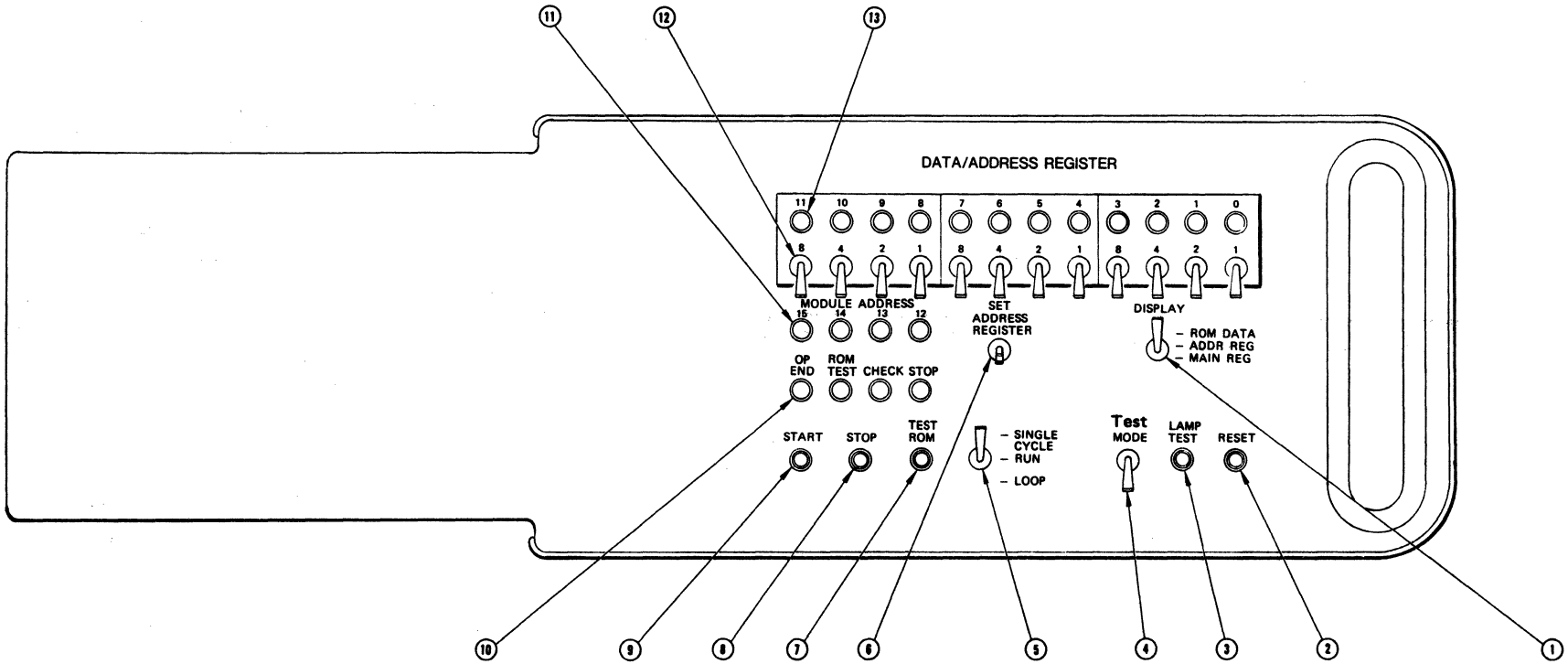


Figure 5-1. PDA Controls and Indicators

(2) RESET - pushbutton used to reset the circuits of the PDA only.

(3) LAMP TEST - pushbutton used to initially ensure that all PDA lamps illuminate.

(4) TEST MODE - two-position toggle switch used to set the PDA into the TEST MODE of operation.

When set to TEST MODE, the +ENABLE SYS ROM signal goes negative to disable all 4K of system ROM. This allows the PDA to exercise the system, since the PDA ROM becomes operational at this time.

When set to TEST MODE during a ROM Test, the +ENABLE SYS ROM signal goes positive to enable the system ROM to function.

(5) Mode - three-position toggle switch used to set the mode of operation.

When set to SINGLE CYCLE, the system will execute the PDA's routines one instruction at a time, for each depression of the START pushbutton.

When set to RUN, the system will execute all of the routines stored in the PDA's memory, once the START pushbutton is depressed. Depressing the STOP pushbutton stops the execution of instructions.

When set to LOOP, the system will execute and repeat a specific routine once the START pushbutton is depressed. Depressing the STOP pushbutton stops this operation.

(6) SET ADDRESS REGISTER - momentary center-off toggle switch used to command an external address branching operation. When it is desired to directly enter a given routine within the PDA's stored diagnostic program, the address of the desired routine is set by the Address Bit Switches. The system must be reset before the SET ADDRESS REGISTER switch is momentarily placed to its up position, then released. When the START pushbutton is depressed the operation will branch to address 009 on the first clock cycle. On the second cycle, operation will be shifted to the address of the desired routine.

(7) TEST ROM - pushbutton used to command the ROM Test.

(8) STOP - pushbutton used to stop system operations. When depressed, a stop signal is generated to inhibit the system Address Register (socket 9). This prevents the next absolute address from being transferred.

(9) START - pushbutton used to initiate an operation. It must be depressed once for each instruction when the Mode switch is set to SINGLE CYCLE. When the Mode switch is set to either RUN or LOOP, the START switch need only be depressed once to initiate the operation.

(10) Status Indicators - four lamps used to display test status.

OP END - used during the ROM Test to indicate that the ROM test operation for the selected major page has ended.

ROM TEST - used to indicate that a ROM Test is in progress. Since each ROM Test takes approximately 500 μs, the off-to-on-to-off states of this lamp are not visually detectable.

CHECK - used to indicate that a malfunction was detected.

STOP - used to indicate that a -CLOCK STOP signal has been generated to inhibit the advancing of the system Address Register. Since each ROM Test takes approximately 500 μs, the on-to-off-to-on states of this lamp are not visually detectable.

(11) MODULE ADDRESS - four lamps used to display the state of each bit in the module address portion (upper order four bits) of the 16-bit instruction word.

(12) Address Bit Switches - twelve two-position toggle switches used to manually set a 12-bit address. The binary weight is shown above each group of four switches to aid in hex conversion. When a switch is placed to its up position a "1" will be set, while a "0" will be set in its down position.

(13) Data/Address Bit Indicators - twelve lamps used to display the states of either data or address bits. The binary weight is shown below each group of four lamps to aid in hex conversion. When a lamp illuminates a "1" is indicated, while a "0" is indicated when it is extinguished.

5.4 POWER SUPPLY VOLTAGE

CAUTION

Use care when probing power circuits. An AC voltage level of 115 Vac is present in the power supply section when the POWER pushbutton is depressed to off.

5.4.1 Voltage Levels

DC voltage levels of +24V, +15V, +11V, +5V, -5V, -9V, -15V, and -22.5V are used throughout the system. These voltage values must be within the required ranges specified in Table 1-1 when referenced to DC ground. Refer to paragraph 2.3.1 for further measurement details.

5.4.2 Logic Levels

The high-low logic voltage levels used in the typewriter and console circuitry are as follows:

High Level . . . . . 2.4V to 5.0V (3.3V typical)
Low Level . . . . . 0.0V to 0.8V (0.22V typical)

5.4.3 Use of Test Probes

When probing or using jumpers, ensure that logic modules are not overloaded. Avoid the use of high voltages which could cause damage or destroy semiconductor devices. For the majority of logic circuit testing, a properly placed ground will create the desired effect.

CHAPTER 6
CHECKS AND ADJUSTMENTS

6.1 GENERAL

The Programmed Diagnostic Aid (PDA) is designed for use by the Service Engineer when verifying system integrity, either at the time of installation or whenever there is a need to troubleshoot the system. The following are those diagnostic routines performed with this test unit:

- ROM Test
- Branch Test
- Branch on Data Test
- PDA Test
- G-Registers Test
- H-Registers Test
- ALU Test
- Buffers Test
- Data Bus Out Test
- Data Bus In Test
- Keyboard Strobe Test
- Printer Test
- Transports Tests

Each of these diagnostic routines is accessable in one of two manners; sequentially through the PDA's internal program, or directly through PDA manual addressing. Since each routine verifies a specific system function and each verified function is used to further expand the PDA's overall test capabilities, the routines must be performed in the order given. Once all tests have been performed, it may be desired to directly enter a given routine to exercise or observe a specific function or to make an adjustment. If so desired, proceed as outlined in the note provided in paragraph 6.2 step 8.

The paragraphs which follow describe each operation as if it is going to be independently tested. In actual practice, the Service Engineer will simply install the PDA and progress from test to test automatically by depressing only the START pushbutton. PDA manipulation is at a minimum and required only during the PDA Test, Data Bus In Test, and Transport Tests.

6.2 PDA INSTALLATION

Use the following procedure to install the PDA:

1. Remove the right-hand side access panel from the console by grasping the lower edge of the panel and pulling it away from the frame structure. Lift it up and away from the frame.
2. Ensure that the POWER switch on the console is set to OFF.

3. Set the following switches to the indicated position:

TEST MODE	down (OFF) position
Mode	RUN
DISPLAY	ADDR REG
All Address Bit Switches . .	"Ø" state (down position)

4. Install the PDA into sockets 27 and 28 of the card cage, as shown in Figure 6-1.

5. Set the POWER switch on the console to ON.

NOTE: The STOP lamp will be illuminated.

6. Depress the LAMP TEST pushbutton and verify that all PDA lamps illuminate.

7. Depress and release the START pushbutton. After the system buzzer sounds, depress and release the system RESET toggle switch to reset the system and zero the ROM Address Register (socket 9). This switch, shown in Figure 6-1, is located on the card cage. It is a momentary type and will spring back when released.

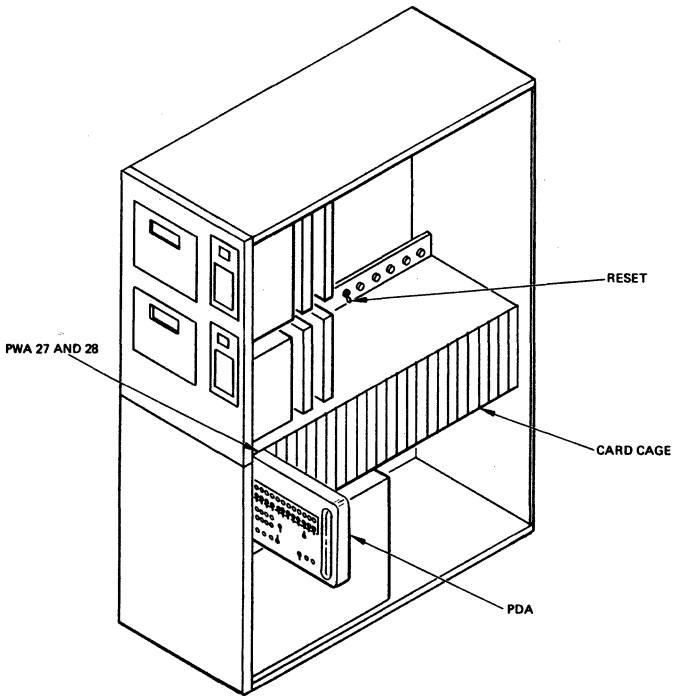


Figure 6-1. PDA Installation

8. Perform each of the tests in the order outlined in the following paragraphs.

NOTE: If a failure is detected while performing any one of these tests, it may be desired to directly enter or return to the routine in which the failure was detected. The following procedure may be used to skip those tests successfully passed. It may also be used to directly enter any routine for testing, troubleshooting or adjustment purposes such as in the case of the Transport Tests:

a. Set the following switches to the indicated position:

TEST MODE	up (TEST MODE)
Mode	SINGLE CYCLE
DISPLAY	ADDR REG
All Address Bit Switches. . .	"Ø" state (down position)

b. Momentarily, depress and release the RESET toggle switch on the card cage and observe that the Data/Address Bit Indicators display hex address ØØØ.

c. Set the Address Bit Switches to the desired hex "starting address" of the routine to be entered. The hex "starting address" and "test end address" for each routine is listed in Table 6-1. The "error addresses" for each routine are listed in Table 6-2.

d. Momentarily, place the SET ADDRESS REGISTER switch to its up position.

e. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display hex address ØØ9.

f. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display the desired hex "starting address."

g. Set the Mode switch to the position specified in each test.

Table 6-1. PDA Routine Addresses

TEST	ROUTINE	STARTING ADDRESS	TEST END ADDRESS
1	ROM Test		
2	Branch Test	ØØØ	Ø13
3	Branch on Data Test	Ø19	ØF7
4	PDA Test	Ø48	Ø4F
5	G-Registers Test	Ø5Ø	ØAE
6	H-Registers Test	ØAF	ØE4
7	ALU Test	ØE6	1BB
8	Buffers Test	1BC	272
9	Data Bus Out Test	281	28F
10	Data Bus In Test	29Ø	295
11	Keyboard Strobe Test	296	2D9
12	Printer Test	3AØ	3B1
13	Transport Tests		
	a. Run Forward Normal	2CØ	2F4
	b. Run Reverse Normal	2C4	2F4
	c. Run Forward Fast	2C8	2F4
	d. Run Reverse Fast	2CC	2F4
	e. Speed Test	34E	3FC
	f. Normal Write Forward	32Ø	2F4

Table 6-2. Error Addresses

TEST	ROUTINE	ERROR ADDRESS
1	ROM Test	---
2	Branch Test	ØØ2 ØØ4
3	Branch on Data Test	Ø1B Ø1E Ø21 Ø24 Ø27 Ø2A Ø2D Ø31 Ø34 Ø37 Ø3A Ø3D Ø41 Ø44 Ø47
4	PDA Test	Ø4E
5	G-Registers Test	Ø5A Ø6E Ø86
6	H-Registers Test	ØB9
7	ALU Test	ØED ØEF ØF2 ØF3 ØF5 ØFA ØFC 1Ø2 1Ø5 1Ø7 1Ø9 1ØF 114 116 11A 11D 12E 132 136 13A 13F 145 15A 164 166 16F 176 17C 185 18A 192 19A 1A4 1AC 1B5
8	Buffers Test	
	a. Read Only	1BE 1CA 1C8 1CD 1D5 1D8 1E2 1EB 1F6 1FB 2Ø5 2Ø9 212
	b. Read/Write	216 21E 223 228 22D 232 23B 243 251 257 259 263 26C
9	Data Bus Out Test	VISUAL (illuminating keys)
10	Data Bus In Test	VISUAL (block address displays)
11	Keyboard Strobe Test	VISUAL (2D9 plus CHECK lamp)
12	Printer Test	VISUAL (printout)
13	Transport Tests	
	a. Run Forward Normal	2D3* 2ED* 2F7* 3DA* 3F8*
	b. Run Reverse Normal	2D3* 2ED* 2F7* 3DA* 3F8*
	c. Run Forward Fast	2D3* 2ED* 3DA* 3F8*
	d. Run Reverse Fast	2D3* 2ED* 3DA* 3F8*
	e. Speed	AUDIO-VISUAL
	f. Normal Write Forward	ØØF 2D3* 2ED* 2F7* 34D 3DA* 3F8*

*These "error addresses" are common to Transport Tests a, b, c, d, and f. See Table 6-9.

6.3 ROM TEST

The purpose of the ROM Test is to verify the contents of each location in the system ROM. Each of the 16 Major-Pages in the ROM is individually tested. Should a failure be detected during any one of these tests, the CHECK lamp will illuminate. When this occurs, the defective PWA is simply replaced and the test rerun to ensure that it operates correctly. Perform all Major-Page tests as follows:

1. Install the PDA as outlined in paragraph 6.2.
2. Momentarily, depress and release the RESET toggle switch on the card cage.

   NOTE: The STOP lamp will be illuminated.

3. Set the TEST MODE switch to the up (TEST MODE) position.
4. Set the Mode switch to RUN.
5. Perform each of the Major-Page tests outlined in Table 6-3 by setting the Address Bit Switches indicated, to either the "1" state (up position) or "Ø" state (down position). Address Bit Switches 10 and 11 manually set the address of the K-Page, while 8 and 9 address the Major-Page. The remainder of the switches (Ø through 7) must be in the "Ø" state (down position) so as not to interfere with the sequential addressing operation of the ROM Address Register. Depress the TEST ROM pushbutton. The OP END lamp will illuminate at the end of the 500 μs test. If the CHECK lamp remains extinguished, the test was successful and the next Major-Page test may be performed. If the CHECK lamp illuminates, a failure was detected, therefore, the associated PWA, listed in Table 6-3, must be replaced. Whenever a PWA is replaced, rerun the test to ensure that it functions correctly in the system. If after replacing the indicated PWA, the CHECK lamp still illuminates each time the test is rerun, replace PWA 9 (ROM Address Register) and repeat the test. If the problem is again not solved, replace PWA 4 (Miscellaneous, Clock, and IC) and repeat the test.

   NOTE: Before beginning each test, momentarily depress and release the RESET toggle switch on the card cage.

Table 6-3. ROM Tests

TEST	ADDRESS BIT SWITCH				DEFECTIVE PWA
	11	10	9	8	
1	Ø	Ø	Ø	Ø	5
2	Ø	Ø	Ø	1	5
3	Ø	Ø	1	Ø	5
4	Ø	Ø	1	1	5
5	Ø	1	Ø	Ø	6
6	Ø	1	Ø	1	6
7	Ø	1	1	Ø	6
8	Ø	1	1	1	6
9	1	Ø	Ø	Ø	7
10	1	Ø	Ø	1	7
11	1	Ø	1	Ø	7
12	1	Ø	1	1	7
13	1	1	Ø	Ø	8
14	1	1	Ø	1	8
15	1	1	1	Ø	8
16	1	1	1	1	8

6.4 BRANCH TEST

The purpose of the Branch Test is to verify the sequential, intrapage branch, extra page branch, and extra page branch and return capabilities of the system. In this test the ROM Address Register (socket 9), Return Address Register (socket 10), and the ROM bit buffering circuits on the Keyboard Interface (socket 3) and the Miscellaneous, Clock and IC(socket 4) PWA's are exercised. Perform the Branch Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

2. Momentarily, depress and release the RESET toggle switch on the card cage.

3. Set the following switches to the indicated position:

   TEST MODE . . . . . up (TEST MODE)
   Mode . . . . . SINGLE CYCLE
   DISPLAY . . . . . ADDR REG
   All Address Bit Switches. "Ø" state (down position)

   NOTE: All Data/Address Bit Indicators (Ø through 11) should be extinguished and the STOP lamp should be illuminated.

4. Momentarily, depress and release the START pushbutton and observe that the Data/Address Bit Indicators illuminate in the pattern shown in Table 6-4. A "1" indicates that the lamp is illuminated, while a "Ø" indicates that it is extinguished. If the pattern is exactly the same as that show, repeat the process until all 12 tests have been completed. If the pattern does not exactly match, replace the indicated PWA and repeat all 12 tests. If after replacing the indicated PWA, the pattern does not exactly match, replace PWA 3 (Keyboard Interface) and repeat all 12 tests. If the pattern still does not exactly match, replace PWA 4 (Miscellaneous, Clock and IC) and repeat all 12 tests.

   NOTE: The equivalent hex address is also shown in Table 6-4, as well as branching operation being tested.

Table 6-4. Branch Tests

TEST	DATA/ADDRESS BIT INDICATORS 11 10 9 8	7 6 5 4	3 2 1 Ø	HEX ADDRESS	BRANCHING OPERATION	DEFECTIVE PWA
- -	Ø Ø Ø Ø	Ø Ø Ø Ø	Ø Ø Ø Ø	ØØØ	start of test	- -
1	Ø Ø Ø Ø	Ø Ø Ø Ø	Ø Ø Ø 1	ØØ1	intrapage branch	9
2	Ø Ø Ø Ø	Ø Ø Ø Ø	Ø Ø 1 1	ØØ3	extra page branch	9
3	Ø Ø Ø Ø	Ø Ø Ø 1	Ø Ø Ø Ø	Ø1Ø	sequential	9
4	Ø Ø Ø Ø	Ø Ø Ø 1	Ø Ø Ø 1	Ø11	extra page branch and return	9
5	Ø Ø Ø Ø	Ø Ø Ø Ø	Ø 1 Ø 1	ØØ5	return	10
6	Ø Ø Ø Ø	Ø Ø Ø 1	Ø Ø 1 Ø	Ø12	extra page branch and return #1	10
7	Ø Ø Ø Ø	Ø Ø Ø Ø	Ø 1 1 Ø	ØØ6	extra page branch and return #2	10
8	Ø Ø Ø Ø	Ø Ø Ø 1	Ø 1 Ø Ø	Ø14	extra page branch and return #3	10
9	Ø Ø Ø Ø	Ø Ø Ø Ø	1 Ø Ø Ø	ØØ8	return #3	10
10	Ø Ø Ø Ø	Ø Ø Ø 1	Ø 1 Ø 1	Ø15	return #2	10
11	Ø Ø Ø Ø	Ø Ø Ø Ø	Ø 1 1 1	ØØ7	return #1	10
12	Ø Ø Ø Ø	Ø Ø Ø 1	Ø Ø 1 1	Ø13	end of test	10

6.5 BRANCH ON DATA TEST

The purpose of the Branch on Data Test is to test the system's capability to transfer a constant from ROM to the Main (M)-Register and its ability to branch on the stored data. In this test, the comparison circuits of the Arithmetic Logic Unit (socket 12) and the storage and transfer capabilities of the M-Register (socket 11) are tested. Perform the Branch on Data Test as Follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode	SINGLE CYCLE
DISPLAY	ADDR REG
All address Bit Switches . .	"Ø" state (down position)

2. Upon completion of the Branch Test (paragraph 6.4), observe that the Data/Address Bit Indicators display the hex "test end address" Ø13.

   NOTE: Do not reset the system.

3. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display the hex "starting address" Ø19 of the Branch on Data Test.

4. Set the Mode switch to RUN.

5. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display the hex "starting address" Ø48 of the PDA Test which indicates a successful end of test.

   Should an error be detected one of the Branch on Data Test hex "error addresses," listed in Table 6-5, will be displayed without illuminating the CHECK or STOP lamps.

Table 6-5. Branch on Data Test "Error Addresses"

Ø1B	Ø34
Ø1E	Ø37
Ø21	Ø3A
Ø24	Ø3D
Ø27	Ø41
Ø2A	Ø44
Ø2D	Ø47
Ø31	

If the test stops at any address other than Ø48, an error will have been detected. If an "error address" is displayed, replace PWA 12 (Arithmetic

Logic Unit) and rerun the test. If after replacing PWA 12, the test does not run successfully, replace PWA 11 (Main and General Purpose Register) and rerun the test. Other PWA's that could affect this test are 3, 4, 9, and 10.

6.6 PDA TEST

The purpose of the PDA Test is to provide a self test for the PDA. In this test, the ability of the PDA to respond to commands from the Microprocessor is tested. These responses include: illuminating the STOP lamp, illuminating the CHECK lamp, and branching on the Mode switch when it is placed in the LOOP position. Perform the PDA Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode.	RUN
DISPLAY	ADDR REG
All Address Bit Indicators. .	"Ø" state (down position)

2. Upon completion of the Branch on Data Test (paragraph 6.5) observe that the Data/Address Bit Indicators display the hex "starting address" Ø48 of the PDA Test. Also, observe that the STOP lamp is illuminated.

   NOTE: Do not reset the system.

3. Set the Mode switch to SINGLE CYCLE.
4. Depress and release the START pushbutton twice and observe that the Data/Address Bit Indicators display hex address Ø4A. Also, observe that both the CHECK and STOP lamps illuminate.
5. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display hex address Ø4B and both the CHECK and STOP lamps remain illuminated.
6. Set the Mode switch to LOOP.
7. Depress the RESET pushbutton on the PDA and observe that the CHECK lamp is extinguished and that the STOP lamp remains illuminated.
8. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display the hex "test end address" Ø4F. Also, observe that the STOP lamp remains illuminated. If the hex "error address" Ø4E is displayed, the test has failed, and the PDA should be replaced.

6.7 G-REGISTERS TEST

The purpose of the G-Registers Test is to test the system's capability to store and transfer data from the M-Register to each of the sixteen G-Registers that constitute one-half of the G P-Register (socket 11). In this test, each of the eight M-Register bits (MØ

through M7) is first set to zero. The data is then incremented by 1 through the carry-in (Ci) input of the ALU and then transferred to the G1 register via the data bus. It is returned, through the ALU on the ALB lines, to the M-Register. The transfer process is repeated until each of the sixteen G-Registers has received the data and returned it to the M-Register. The data is incremented by one and the entire process is repeated until 256 complete transfers, through all registers, have been accomplished. The GØ register, initially tested in this routine, is used to count each complete transfer. On the 256th transfer, the data stored in the GF register is tested for the expected stored data. Perform the G-Registers Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated positions:

TEST MODE	up (TEST MODE)
Mode	LOOP
DISPLAY	ADDR REG
All Address Bit Switches	"Ø" state (down position)

2. Upon completion of the PDA Test (paragraph 6.6), observe that the Data/Address Bit Indicators display the hex "test end address" Ø4F.

   NOTE: Do not reset the system.

3. Set the Mode switch to RUN.

4. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display the hex "test end address" ØAE. Also, observe that the STOP lamp illuminates.

   If an error is detected, the CHECK lamp will illuminate, and one of the G-Registers Test hex "error addresses" will be displayed. If the Data/Address Bit Indicators display the hex "error address" Ø5A, replace PWA 12 (Arithmetic Logic Unit) and rerun the test. If "error address" Ø6E or Ø86 is displayed, replace PWA 11 (Main and General Purpose Register) and rerun the test. Other PWA's that could affect this test are 3, 4, 9, and 10.

6.8 H-REGISTERS TEST

The purpose of the H-Registers Test is to test the system's capability to store and transfer data from the M-Register to each of the sixteen H-Registers that constitute the other half of the GP-Register (socket 11). This test is performed in much the same manner as the G-Registers Test (paragraph 6.7). The GØ register, initially tested during the G-Registers Test, is used to count each complete transfer. On the 256th transfer, the data stored in the HF register is tested for the expected stored data. Perform the H-Registers Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode	RUN
DISPLAY	ADDR REG
All Address Bit Switches	"Ø" state (down position)

2. Upon completion of the G-Registers Test (paragraph 6.7), observe that the Data/Address Bit Indicators display the hex "test end address" ØAE.

   NOTE: Do not reset the system.

3. Set the Mode switch to RUN.

4. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display the hex "test end address" ØE4. Also, observe that the STOP lamp illuminates.

   If an error is detected, the CHECK lamp will illuminate, and the H-Registers Test hex "error address" ØB9 will be displayed. If the Data/Address Bit Indicators display the hex "error address" ØB9, replace PWA 11 (Main and General Purpose Register) and rerun the test. If after replacing PWA 11, the hex "error address" is still displayed, replace PWA 12 (Arithmetic Logic Unit) and rerun the test. Other PWA's that could affect this test are 3, 4, 9, and 10.

6.9 ALU TEST

The purpose of the ALU Test is to test the system's capability to perform both logic and arithmetic operations. In this test, each of the logic and arithmetic functions of the Arithmetic Logic Unit (socket 12) are tested. Perform the ALU Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode	RUN
DISPLAY	ADDR REG
All Address Bit Switches	"Ø" state (down position)

2. Upon completion of the H-Registers Test (paragraph 6.8), observe that the Data/Address Bit Indicators display the hex "test end address" ØE4.

   NOTE: Do not reset the system.

3. Set the Mode switch to RUN.

4. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display the hex "test end address" 1BB. Also, observe that the STOP lamp illuminates.

NOTE: The ALU Test, due to its complexity, will take approximately 10 seconds to complete.

If an error is detected, the CHECK lamp will illuminate and one of the ALU Test hex "error addresses", listed in Table 6-6, will be displayed. If the Data/Address Bit Indicators display one of the ALU Test hex "error addresses", replace PWA 12 (Arithmetic Logic Unit) and rerun the test. If after replacing PWA 12, one of the hex "error addresses" is still displayed, replace PWA 11 (Main and General Purpose Register) and rerun the test. Other PWA's that could affect this test are 3, 4, 9, and 10.

Table 6-6. ALU Test "Error Addresses"

ØED	114	166
ØEF	116	16F
ØF2	11A	176
ØF3	11D	17C
ØF5	12E	185
ØFA	132	18A
ØFC	136	192
1Ø2	13A	19A
1Ø5	13F	1A4
1Ø7	145	1AC
1Ø9	15A	1B5
1ØF	164	

6.10 BUFFERS TEST

The purpose of the Buffers Test is to test the Buffer I/O and Buffer Control functions for the Read Only buffer, (sockets 13 and 14) and the Read/Write buffer (Sockets 15 and 16). Perform the Buffers Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

   TEST MODE . . . . . up (TEST MODE)
   Mode . . . . . RUN
   DISPLAY . . . . . ADDR REG
   All Address Bit Switches . . "Ø" state (down position)

2. Upon completion of the ALU Test (paragraph 6.9) observe that the Data/Address Bit Indicators display the hex "test end address" 1BB.

   NOTE: Do not reset the system.

3. Set the Mode switch to RUN.

4. Depress and release the START pushbutton and observe that the Data/Address Bit Indicators display the hex "test end address" 272. Also observe that the STOP lamp illuminates.

   If an error is detected, the CHECK lamp will illuminate, and one of the Buffers Test hex "error addresses", listed in Table 6-7, will be displayed. If the Data/Address Bit Indicators display one of the Read Only Buffers Test hex "error addresses", replace PWA 13 (Read Only Buffer I/O) and rerun the test. If after replacing PWA 13, the CHECK lamp still illuminates and one of the Read Only hex "error addresses" is still displayed, replace PWA 14 (Read Only Buffer Control) and rerun the test. If the Data/Address Bit Indicators display one of the Read/Write Buffers Test hex "error addresses", replace PWA 15 (Read/Write Buffer I/O) and rerun the test. If after replacing PWA 15 the CHECK lamp still illuminates and one of the Read/Write hex "error addresses" is still displayed, replace PWA 16 (Read/Write Buffer Control) and rerun the test.

Table 6-7. Buffers Test "Error Addresses"

READ ONLY		READ/WRITE	
1BE	1EB	216	243
1C4	1F6	21E	251
1C8	1FB	223	257
1CD	2Ø5	228	259
1D5	2Ø9	22D	263
1D8	212	232	26C
1E2		23B	

6.11 DATA BUS OUT (LAMP) TEST

The purpose of the Data Bus Out (Lamp) Test is to test the data bus "out" lines and thus the ability of the system to communicate with the keyboard via the Keyboard Interface. (socket 3). In this test, one direction of the bidirectional 8-bit data flow path from the console to the keyboard is tested. Perform the Data Bus Out (Lamp) Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode	RUN
DISPLAY	ADDR REG
All Address Bit Switches . .	"Ø" state (down position)

2. Upon completion of the Buffers Test (paragraph 6.10), observe that the Data/Address Bit Indicators display the hex "test end address" 272.

   NOTE: Do not reset the system.

3. Set the Mode switch to RUN.

4. Depress and release the START pushbutton and observe that those keys on the keyboard, listed in Table 6-8, illuminate in the exact sequence and pattern shown. Those keys listed should remain illuminated for approximately four seconds.

Table 6-8. Data Bus Out (Lamp) Test Sequence

SEQUENCE	NUMBER OF KEYS ILLUMINATED	PATTERN (Keys Illuminated)	TIME
1	None	All keys illuminated	≈ 4 sec
2	3	WORD-DUP-REV	"
3	4	LINE-SKIP-MARG CONT-REC	"
4	2	PARA-CODE PRINT	"
5	3	AUTO-PLAY-SEARCH	"
6	3*	PLAY-REC-SEARCH	continuous
7	3*	Test End (single buzzer)	≈1/4 sec

*Flashing

If both the sequence and pattern are exactly as shown, observe that the Data/Address Bit Indicators display the hex "test end address" 28F. Also, observe that the STOP lamp is illuminated.

If both the sequence and pattern are not exactly as shown, replace PWA3 (Keyboard Interface) and rerun the test. If after replacing PWA3, both the sequence and pattern are still not exactly as shown, replace the keyboard and rerun the test.

6.12 DATA BUS IN (THUMBWHEEL) TEST

The purpose of the Data Bus In (Thumbwheel) Test is to test the data bus "in" lines and thus the ability of the keyboard to communicate with the system via the Keyboard Interface (socket 3) and Tape Control (sockets 17 and 20) PWA's. In this test, the

remaining direction of the bidirectional 8-bit data flow path from the keyboard to the console is tested. This is accomplished by setting numbers into the system with the thumbwheels and reading those numbers on the block address displays. Perform the Data Bus In (Thumbwheel) Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode.	RUN
DISPLAY	ADDR REG
All Address Bit Switches . .	"Ø" state (down position)

2. Upon completion of the Data Bus Out (Lamp) Test (paragraph 6.11), observe that the Data/Address Bit Indicators display the hex "test end address" 28F.

   NOTE: Do not reset the system.

3. Set the Mode switch to LOOP.

4. Depress and release the START pushbutton. Rotate each of the two thumbwheels through their full range (numbers Ø-9) and observe that both block address displays indicate the numbers set into the thumbwheels. If the numbers are properly displayed, the test has been successful. After a successful completion of this test, set the Mode switch to SINGLE CYCLE and observe that the Data/Address Bit Indicators display the hex "test end address" 295. Also, observe that the STOP lamp is illuminated.

   If both block address displays fail to indicate the numbers set into the thumbwheels, replace PWA3 (Keyboard Interface) and rerun the test. If both block address displays still fail to indicate properly, replace the keyboard and rerun the test. If only one block address display fails to indicate properly, replace the associated Tape Control PWA, i.e., PWA17 (Read/Write) or PWA20 (Read Only), and rerun the test. If an error is still indicated, replace the corresponding Display Panel PWA associated with the failing block address display and rerun the test.

6.13 KEYBOARD STROBE TEST

The purpose of the Keyboard Strobe Test is to determine whether a keyboard strobe will clear an 8-bit ASCII character bit pattern from the data bus. In this test, a search code (Ø) with a minimum 8-bit ASCII character bit pattern (hex Ø1) and an upper case "O" with a maximum 8-bit ASCII character bit pattern (hex EF) are used. Again the bidirectional 8-bit data flow path from the keyboard to the console via the Keyboard Interface (socket 3) will be tested. Perform the Keyboard Strobe Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode	SINGLE CYCLE
DISPLAY	ADDR REG
All Address Bit Switches . .	"Ø" state (down position)

2. Upon completion of the Data Bus In (Thumbwheel) Test (paragraph 6.12), observe that the Data/Address Bit Indicators display the hex "test end address" 295.

   NOTE: Do not reset the system.

3. Set the Mode switch to RUN.

4. Depress and release the START pushbutton.

5. Depress an upper case "O" and observe that the CHECK lamp does not illuminate.

6. Depress the "6" key together with the CODE key (search code (Ø)) and observe that the CHECK lamp does not illuminate. Also observe that the Data/Address Bit Indicators display the hex "test end address" 2D9 and that the STOP lamp illuminates.

6.14 PRINTER TEST

The purpose of the Printer Test is to functionally test the printer by positioning the carrier at the left-hand margin, and printing 85 characters from the printwheel in a predetermined sequence. This output is visually checked against the sequence for errors. Perform the Printer Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode	RUN
DISPLAY	ADDR REG
All Address Bit Switches . .	"Ø" state (down position)

2. Upon completion of the Keyboard Strobe Test, (paragraph 6.13) observe that the Data/Address Bit Indicators display the hex "test end address" 2D9.

   NOTE: Do not reset the system.

3. Insert a piece of paper into the printer. The paper should provide space for 85 characters. An 8-1/2" x 11" paper inserted endwise is sufficient.

4. Set the Mode switch to RUN.

5. Depress and release the START pushbutton and observe that the printer types out the following sequence on a single line:

   ABCDEFGHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrstuvwxyz{¢!"#%&'()*+,-./0123456789:;<=>?

   If the test is successful, the printer will have typed out on a single line the exact sequence as shown. Observe that the Data/Address Bit Indicators display the hex "test end address" 3B1 and that the STOP light illuminates.

   If the sequence is not typed out exactly as shown, replace PWA 1 (Printer Interface) and rerun the test. If the sequence is still not typed out exactly as shown, replace the printer.

6.15 TRANSPORT TESTS

The purpose of the Transport Tests is to verify proper Read/Write or Read Only transport operation. These tests do not automatically progress from one to another as in the case of the previous test. Each test must be initiated by the Service Engineer as outlined in paragraph 6.2. In this way, the routine required to perform a particular test or to isolate a specific problem can be directly entered. Any one or all of the following tests may be performed. Prior to performing any one of the following tests, an active transport must be selected. This is accomplished by setting the Line Space Lever on the Typewriter to SINGLE space to activate the Read Only (RO) transport or to DOUBLE space to activate the Read/Write (R/W) transport.

The Run Forward Normal and Run Reverse Normal tests will cause the selected transport to drive the tape in the direction specified by the test at the normal speed of 20 ips. The Run Forward Fast and Run Reverse Fast tests will also cause the selected transport to drive the tape in the direction specified by the test, but at the fast speed of 70 ips. The Speed Test is used to verify that the selected transport is operating at a speed within a specified tolerance. The Normal Write Forward test permits continuous writing of a predetermined bit pattern that will aid the Service Engineer in troubleshooting the Read/Write transport electronics. All of these tests can be used by the Service Engineer to verify proper transport operation.

These tests will continuously operate between the clear leader at either end of the tape, unless stopped by a Servo Unsafe ("error address" 2ED) or an NEOT Not Detected ("error address" 2F7) condition. During the Normal Write Forward test, the presence of write current is monitored. A Write Current Not Present ("error address" 39C) condition will cause the transport to stop and the STOP and CHECK lamps to illuminate. Also, if a Read Only tape cassette has been placed in the Read/Write transport, the Normal Write Forward test will not start. If a Read Only tape cassette is detected, both the STOP and CHECK lamps will illuminate and the hex "error address" ØØF will be displayed by the Data/Address Bit Indicators.

Perform each of the tests as outlined in the following paragraphs.

6.15.1 Run Forward Normal Test

Perform the Run Forward Normal Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode.	RUN
DISPLAY	ADDR REG
All Address Bit Switches . .	"Ø" state (down position)

2. Select an active transport as outlined in paragraph 6.15.

3. Place a "scratch" cassette into the selected transport.

   NOTE: If after placing a tape cassette into the transport and closing the door, the door should immediately reopen, wait until the motors have stopped turning before reclosing.

4. Set in the hex "starting address" 2CØ as outlined in paragraph 6.2, steps 8a through 8f.

5. Set the Mode switch to RUN.

6. Depress and release the START pushbutton. The tape will run, if required, in the reverse direction at the fast speed (70 ips) until clear leader is reached, then run in the forward direction at the normal speed (20 ips) until the clear leader at the other end of the tape is reached. The transport will stop and the STOP lamp will illuminate. Observe that the Data/Address Bit Indicators display the hex "test end address" 2F4.

   If an error is detected, the test will stop and the STOP and CHECK lamps will illuminate. Refer to Table 6-9 for an analysis of the error condition. After replacing the PWA most likely defective or checking the most likely problem, rerun the test. If an error is still detected, replace the next most likely defective PWA or check the next most likely problem. Continue this procedure until the hex "test end address" 2F4 is encountered and the STOP lamp illuminates.

7. If testing a dual station system, select the other transport and rerun the Run Forward Normal Test.

Table 6-9. Transport Tests Error Analysis

ERROR ADDRESS	ERROR CONDITION	AFFECTED PWA		CHECK
		RO	R/W	
2D3	Cassette Not In Place	RO J1 (1) RO J2 (2) PWA 20 (3)	R/W J1 (1) R/W J2 (2) PWA 17 (3)	(1) Check CIN switch on the selected transport. (2) Check associated wiring.
2ED	Servo Unsafe	RO J1 (1) RO J2 (2) PWA 20 (3)	R/W J1 (1) R/W J2 (2) PWA 17 (3)	(1) Check for binding in the transport motors and in the tape cassette.
2F7	NEOT Not Detected	RO J1 (1) RO J2 (2) PWA 20 (3)	R/W J1 (1) R/W J2 (2) PWA 17 (3)	(1) Check position and function of NEOT sensor. (2) Check associated wiring.
3DA	Unselected Transport Active	RO J1 (1) RO J2 (2) PWA 20 (3)	R/W J1 (1) R/W J2 (2) PWA 17 (3)	(1) Ensure that there is a tape cassette in the selected transport. (2) Check CIN switch on the unselected transport.
3F8	Selected Transport Not Active	RO J1 (1) RO J2 (2) PWA 20 (3)	R/W J1 (1) R/W J2 (2) PWA 17 (3)	(1) Ensure that there is a tape cassette in the selected transport. (2) Check CIN switch on selected transport.

(1) Most likely (2) Second most likely (3) Third most likely

6.15.2 Run Reverse Normal Test

Perform the Run Reverse Normal Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

   TEST MODE . . . . . up (TEST MODE)
   Mode . . . . . RUN
   DISPLAY . . . . . ADDR REG
   All Address Bit Switches . . "Ø" state (down position)

2. Select an active transport as outlined in paragraph 6.15.
3. Place a "scratch" cassette into the selected transport.

NOTE: If after placing a tape cassette into the transport and closing the door, the door should immediately reopen, wait until the motors have stopped turning before reclosing.

4. Set in the hex "starting address" 2C4 as outlined in paragraph 6.2 steps 8a through 8f.

5. Set the Mode switch to RUN.

6. Depress and release the START pushbutton. The tape will run, if required, in the forward direction at the fast speed (70 ips) until clear leader is reached, then run in the reverse direction at the normal speed (20 ips) until the clear leader at the other end of the tape is reached. The transport will stop and the STOP lamp will illuminate. Observe that the Data/Address Bit Indicators display the hex "test end address" 2F4.

   If an error is detected, the test will stop and the STOP and CHECK lamps will illuminate. Refer to Table 6-9 for an analysis of the error condition. After replacing the PWA most likely defective or checking the most likely problem, rerun the test. If an error is still detected, replace the next most likely defective PWA or check the next most likely problem. Continue this procedure until the hex "test end address" 2F4 is encountered and the STOP lamp illuminates.

7. If testing a dual station system, select the other transport and rerun the Run Reverse Normal Test.

6.15.3 Run Forward Fast Test

Perform the Run Forward Fast Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode	RUN
DISPLAY	ADDR REG
All Address Bit Switches . .	"Ø" state (down position)

2. Select an active transport as outlined in paragraph 6.15.

3. Place a "scratch" cassette into the selected transport.

   NOTE: If after placing a tape cassette into the transport and closing the door, the door should immediately reopen, wait until the motors have stopped turning before reclosing.

4. Set in the hex "starting address" 2C8, as outlined in paragraph 6.2, steps 8a through 8f.

5. Set the Mode switch to RUN.

6. Depress and release the START pushbutton. The tape will run, if required, in the reverse direction at the fast speed (70 ips) until clear leader is reached, then run in the forward direction at the fast speed (70 ips) until the clear leader at the other end of the tape is reached. The transport will stop and the STOP lamp will illuminate. Observe that the Data/Address Bit Indicators display the hex "test end address" 2F4.

   If an error is detected, the test will stop and the STOP and CHECK lamps will illuminate. Refer to Table 6-9 for an analysis of the error condition. After replacing the PWA most likely defective or checking the most likely problem, rerun the test. If an error is still detected, replace the next most likely defective PWA or check the next most likely problem. Continue this procedure until the hex "test end address" 2F4 is encountered and the STOP lamp illuminates.

7. If testing a dual station system, select the other transport and rerun the Run Forward Fast Test.

6.15.4 Run Reverse Fast Test

Perform the Run Reverse Fast Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode	RUN
DISPLAY	ADDR REG
All Address Bit Switches . .	"Ø" state (down position)

2. Select an active transport as outlined in paragraph 6.15.

3. Place a "scratch" cassette into the selected transport.

   NOTE: If after placing a tape cassette into the transport and closing the door, the door should immediately reopen, wait until the motors have stopped turning before reclosing.

4. Set in the hex "starting address" 2CC as outlined in paragraph 6.2, steps 8a through 8f.

5. Set the Mode switch to RUN.

6. Depress and release the START pushbutton. The tape will run, if required, in the forward direction at the fast speed (70 ips) until clear

leader is reached, then run in the reverse direction at the fast speed (70 ips) until the clear leader at the other end of the tape is reached. The transport will stop and the STOP lamp will illuminate. Observe that the Data/Address Bit Indicators display the hex "test end address" 2F4.

If an error is detected, the test will stop and the STOP and CHECK lamps will illuminate. Refer to Table 6-9 for an analysis of the error condition. After replacing the PWA most likely defective or checking the most likely problem, rerun the test. If an error is still detected, replace the next most likely defective PWA or check the next most likely problem. Continue this procedure until the hex "test end address" 2F4 is encountered and the STOP lamp illuminates.

7. If testing a dual station system, select the other transport and rerun the Run Reverse Fast Test.

6.15.5 Speed Tests

Perform the Speed Tests as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode.	RUN
DISPLAY	ADDR REG
All Address Bit Switches . .	"Ø" state (down position)

2. Select an active transport as outlined in paragraph 6.15.

3. Place a 1600 FCPI test cassette into the selected transport.

   NOTE: If after placing a tape cassette into the transport and closing the door, the door should immediately reopen, wait until the motors have stopped turning before re-closing.

4. Set in the hex "starting address" 34E as outlined in paragraph 6.2, steps 8a through 8f.

5. Set the Mode switch to RUN.

6. Depress and release the START pushbutton. The transport will automatically rewind the tape, if required, then it will advance the tape in a forward direction at the fast speed (70 ips). When the center of the tape is reached the transport will stop. The STOP lamp will illuminate and the hex address 35A will be displayed.

7. Look through the window in the transport door and visually ascertain that both spools contain approximately the same amount of tape. In the

event that the transport does not advance to the center of the tape at the start of the test, refer to the Troubleshooting Chart, Table 7-2. If the tape still does not advance to the center of the tape, replace the associated Motor Control PWA (RO J1 or R/W J1) and repeat the procedure. If after replacing the associated Motor Control PWA, the transport still fails to advance to the center of the tape, replace the transport and repeat the procedure.

8. Set the Mode switch to LOOP.

9. Set the DISPLAY switch to MAIN REG.

10. Perform the forward Speed Test as follows:

    a. Depress and release the START pushbutton. The transport will advance the tape approximately 8" in a forward direction and stop. The system buzzer will buzz once, twice, or three times depending upon the test results.

    NOTE:
    1. One buzz indicates that the transport speed is too slow.
    2. Two buzzes indicate that the transport speed is too fast.
    3. Three buzzes indicate that the transport speed is within the specified tolerance (22.4-23.6 ips)

    When the transport stops, its exact speed will be displayed as two hex digits by the Data/Address Bit Indicators Ø through 7. Data/Address Bit Indicators 8 through 11 will not function since the DISPLAY switch is in the MAIN REG position. Refer to Table 6-10 for the conversion of these two hex digits into transport speeds.

Table 6-10. Speed Conversions

SPEED TOO SLOW		SPEED IN TOLERANCE		SPEED TOO FAST	
MAIN REG DISPLAY	ACTUAL SPEED (ips)	MAIN REG DISPLAY	ACTUAL SPEED (ips)	MAIN REG DISPLAY	ACTUAL SPEED (ips)
D9	21.7	EØ	22.4	ED	23.7
DA	21.8	E1	22.5	EE	23.8
DB	21.9	E2	22.6	EF	23.9
DC	22.0	E3	22.7	FØ	24.0
DD	22.1	E4	22.8	F1	24.1
DE	22.2	E5	22.9	F2	24.2
DF	22.3	E6	23.0	F3	24.3
		E7	23.1		
		E8	23.2		
		E9	23.3		
		EA	23.4		
		EB	23.5		
		EC	23.6		

If the speed is not within tolerance, the transport will automatically rewind approximately 8" of the tape and stop.

b. Note the speed displayed and adjust the lower potentiometer on the associated Motor Control PWA (RO J1 or R/W J1) in the required direction (CW decreases speed, CCW increases speed).

c. Depress and release the START pushbutton and observe the resultant speed displayed.

d. Repeat steps 10b and 10c until the system buzzer buzzes three times to indicate that the transport speed is within tolerance. Note the speed displayed.

11. Perform the reverse Speed Test as follows:

NOTE: The reverse Speed Test cannot be performed until the forward speed is within the specified tolerance.

a. Depress and release the START pushbutton twice. The transport will rewind the tape approximately 8" in a reverse direction and stop. The system buzzer will buzz once, twice, or three times depending upon the test results. Refer to the note in step 10a.

When the transport stops, its exact speed will be displayed as two hex digits by the Data/Address Bit Indicators Ø through 7. Data/Address Bit Indicators 8 through 11 will not function since the DISPLAY switch is in the MAIN REG position. Refer to Table 6-10 for the conversion of these two hex digits into transport speeds.

If the speed is not within tolerance, the transport will automatically advance the tape approximately 8" and stop.

b. Note the speed displayed and adjust the upper potentiometer on the associated Motor Control PWA (RO J1 or R/W J1) in the required direction (CW decreases speed, CCW increases speed).

c. Depress and release the START pushbutton and observe the resultant speed displayed.

d. Repeat steps 11b and 11c until the system buzzer buzzes three times to indicate that the transport speed is within tolerance. Note the speed displayed.

12. Once steps 10 and 11 have been completed, the forward and reverse transport speeds can alternately be verified by depressing and releasing the START pushbutton twice each time the transport stops.

NOTE: During the Speed Test a dual depression of the START pushbutton is required to transfer from the hex "test end address" 3FC to the hex "starting addresses" 35A (forward Speed Test) or 38A (reverse Speed Test).

13. If the initial speeds displayed and noted in steps 10b or 11b were slower than 21.7 ips (hex D9) or faster than 24.3 ips (hex F3), rerun the entire test beginning with step 4 to again verify the speeds.

14. If testing a dual station system, select the other transport and rerun the Speed Test.

6.15.6 Normal Write Forward Test

Perform the Normal Write Forward Test as follows:

1. Install the PDA as outlined in paragraph 6.2 and perform all preceding tests.

   NOTE: The following switches should be set to the indicated position:

TEST MODE	up (TEST MODE)
Mode	LOOP
DISPLAY	MAIN REG
All Address Bit Switches . .	"Ø" state (down position)

2. Select the R/W as the active transport as outlined in paragraph 6.15.

3. Place a "scratch" cassette into the R/W transport.

   NOTE: If after placing a tape cassette into the transport and closing the door, the door should immediately reopen, wait until the motors have stopped turning before reclosing.

4. Set in the hex "starting address" 32Ø as outlined in paragraph 6.2, steps 8a through 8f.

5. Set the Mode switch to RUN.

6. Depress and release the START pushbutton. The transport will automatically rewind the tape, if required, then it will advance the tape in a forward direction at the normal speed (20 ips). Writing will begin at the NEOT hole at the beginning of the tape and continue until the NEOT hole at the other end of the tape is reached. The data written will consist of an alternating bit pattern (10101010) which is not formatted in any manner. This bit pattern is read immediately after writing and is compared against the expected bit pattern. Upon successful completion of the test, the transport will stop and the hex "test end address" 2F4 will be displayed with the STOP lamp illuminated.

   Failure to compare while writing will cause the CHECK lamp to illuminate. If the CHECK lamp illuminates, depress the RESET pushbutton on the PDA to extinguish the lamp. Note the number of times it was required to extinguish the CHECK lamp during the entire writing sequence (from NEOT hole to NEOT hole). If this number is less than eight and none of the "error address" listed in Table 6-11 were displayed, the test was successful.

If this number esceeds eight, an excessive number of data errors will have been detected. Replace PWA R/W J2 and rerun the test. If errors are still excessive, replace PWA 17 and rerun the test. If excessive errors are again detected, replace PWA 19 and rerun the test.

NOTE: During this test, the system will continue to run providing the Service Engineer with an opportunity to troubleshoot the system while it makes data errors.

Table 6-11. Normal Write Forward "Error Addresses"

ERROR ADDRESS	CONDITION
ØØF	Read Only Tape in Transport
2D3	Cassette Not in Place
2ED	Servo Unsafe
2F7	NEOT Not Detected
3DA	Unselected Transport Active
3F9	Selected Transport Not Active
39C	Write Current Not Present

CHAPTER 7

ERROR ANALYSIS

7.1 GENERAL

This chapter contains the recommended troubleshooting sequence that should be followed by the Service Engineer. Table 7-1 lists those PWA's which most likely are affected according to priority. Table 7-2 provides transport troubleshooting information.

7.2 RECOMMENDED TROUBLESHOOTING SEQUENCE

1. Perform the Power Supply Voltage Checkout procedure as outlined in paragraph 2.3.1.
2. Perform the System Diagnostic Checkout procedure as outlined in paragraph 2.3.2.

NOTE: Since each routine verifies a specific function and each verified function is used to further expand the PDA's overall test capabilities, the routines must be performed in the following order:

- ROM Test
- Branch Test
- Branch on Data Test
- PDA Test
- G-Registers Test
- H-Registers Test
- ALU Test
- Buffers Test
- Data Bus Out Test
- Data Bus In Test
- Keyboard Strobe Test
- Printer Test
- Transports Tests
  a. Run Forward Normal Test
  b. Run Reverse Normal Test
  c. Run Forward Fast Test
  d. Run Reverse Fast Test
  e. Speed Tests
  f. Write Forward Normal Test

Once all tests have been performed, it may be desired to directly enter a given routine to exercise or observe a specific function or to make an adjustment. If so desired, proceed as outlined in paragraph 6.2, step 8.

If during the Printer Test, a printer problem is evident, replace PWA 1 (Printer Interface).

If during the Speed Tests, the transports are too slow and the Main Register displays ØØ, replace PWA 18 (Read Decode) in the Read/Write

Table 7-1. PWA's Affected According to Priority

NOTES (1) ALSO AFFECTED IS THE ASSOCIATED DISPLAY PANEL
(2) CHECK FOR BURNED OUT LAMPS
(3) CHECK CIN SWITCH AND NEOT SENSOR

HEX ADDRESS STARTING	HEX ADDRESS TEST END	TEST	PWA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	ROJ1	ROJ2	R/WJ1	R/WJ2	---	---	---
			TITLE	PRINTER INTERFACE	-NOT USED-	KEYBOARD INTERFACE	MISC., CLOCK, AND I.C.	ROM PROGRAM	ROM PROGRAM	ROM PROGRAM	ROM PROGRAM	ROM ADDRESS REGISTER	RETURN ADDRESS REGISTER	M AND GP REGISTER	ALU	BUFFER I/O (RO)	BUFFER CONTROL (RO)	BUFFER I/O (R/W)	BUFFER CONTROL (R/W)	TAPE CONTROL (R/W)	READ DECODE (R/W)	WRITE ENCODE (R/W)	TAPE CONTROL (RO)	READ DECODE (RO)	- NOT USED	- NOT USED	- NOT USED	- NOT USED	- NOT USED	PDA	PDA	MOTOR CONTROL	TAPE READ ONLY	MOTOR CONTROL	TAPE READ WRITE	KEYBOARD	PRINTER	TRANSPORTS
			PART NUMBER	75013805	---	75013800	75013801	75014400	75014400	75014400	75014400	75013749	75013750	75013747	75013748	75013735	75013563	75013735	75013563	75013733	75013731	75013732	75013733	75013731	---	---	---	---	---	00015500	00015500	75013804	75013564	75013804	75013564	---	---	---
---	---	ROM					3	1	1	1	1	2																											
000	013	BRANCH				3	4					1	2																									
019	0F7	BRANCH ON DATA				3	4					5	6	2	1																							
048	04F	PDA																												1	1							
050	0AE	G-REGISTERS				3	4					5	6	2	1																							
0AF	0E4	H-REGISTERS				3	4					5	6	1	2																							
0E6	1BB	ALU				3	4					5	6	2	1																							
1BC	272	BUFFERS				3	4					5	6			1	2	1	2																			
281	28F	DATA BUS OUT				1					(SEE NOTE 2)																									2		
290	295	DATA BUS IN				1					(SEE NOTE 1)									2			2														
296	2D9	KEYBOARD STROBE				1																														2		
3A0	3B1	PRINTER	1																																		2	
2C0	2F4	RUN FORWARD NORMAL						(SEE NOTE 3)												3			3								1	2	1	2			4
2C4	2F4	RUN REVERSE NORMAL						(SEE NOTE 3)												3			3								1	2	1	2			4
2C8	2F4	RUN FORWARD FAST						(SEE NOTE 3)												3			3								1	2	1	2			4
2CC	2F4	RUN REVERSE FAST						(SEE NOTE 3)												3			3								1	2	1	2			4
34E	3FC	SPEED						(SEE NOTE 3)												3	4		3	4							1	2	1	2			5
320	2F4	WRITE FORWARD NORMAL																		2		3										1					4

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transport or PWA 21 (Read Decode) in the Read Only transport.

If during the Write Forward Normal Test, the tape cannot be written upon, replace PWA 19 (Write Encode).

Table 7-2. Troubleshooting Chart

PROBLEM	SOLUTION
Transport speed is excessively fast or excessively slow	Place a "scratch cassette" into the selected transport and perform the Speed Test as outlined in paragraph 6.15.5, steps 1 through 6. If both spools contain approximately the same amount of tape, the speed is within course alignment. If the take-up spool has noticeably more tape than the supply spool, the speed is excessively fast. If the supply spool has noticeably more tape than the take-up spool, the speed is excessively slow. In either of the two latter cases, course align the speed by adjusting the appropriate potentiometer and rerun the test. When both spools contain approximately the same amount of tape; place a 1600 FCPI test cassette into the selected transport and perform the entire Speed Test to fine align the transport speeds.
Transport is breaking tapes or noisy	The motor may be running excessively fast. See solution above. If this does not solve the problem, replace the associated Motor Control PWA.
Cannot write on a cassette	Check the File Protect switch and the Cassette In Place (CIN) switch. These switches are located in the upper left-hand side of the transport just inside of the door opening. The left most switch is the File Protect, and the other is the Cassette In Place. If found ok, use the PDA to troubleshoot the transport.
$\overline{\text{STATUS}}$	Is a large dot OR, PWA's affected--output 1, 2, 3, 4, 13, 15, 17, and 20 input 4,
$\overline{\text{DB}\longrightarrow\text{M}}$	Is a large dot OR, PWA's affected--output 1, 2, 3, 13, 14, 15, 16, 17, and 20 input 11,

CHAPTER 8

REPLACEMENT PROCEDURES

8.1 GENERAL

This chapter contains those procedures recommended for removing and installing the printer, keyboard, and transports. Also provided are removal and installation instructions for the various subassemblies that comprise the transport, i.e., the head mounting plate assembly, motors, door latch solenoid, BOT/EOT sensor assembly, and the cassette in place and file protect switches.

8.2 PRINTER REMOVAL AND INSTALLATION

Use the following procedure for removing and installing the printer.

1. Ensure that the POWER switch is set to OFF, then disconnect the power cord from the 115 Vac, 60Hz power source.
2. Tilt the typewriter platen cover upward to expose the platen.
3. Depress the two platen release levers and lift the platen from the typewriter.
4. Raise the left-hand lever switch bank that supports the MARG LEFT/RIGHT and TAB CLEAR/SET levers.
5. Raise the right-hand lever switch bank that supports the SINGLE/DOUBLE and 10/12 levers.
6. Pull forward on the two upper case release levers and remove the upper case from the typewriter.
7. Disconnect the Printer Interface connector A7P1, Power connector A7P3, and Lever Switch Interface connector A7P4.
8. Tilt the typewriter upward and rest it on its rear panel.
9. While supporting the printer, remove the four screws, located in the center of each rubber foot.
10. Carefully, lift the printer from the case.
11. Reverse the procedure when installing the printer into the typewriter case.

8.3 KEYBOARD REMOVAL AND INSTALLATION

Use the following procedure for removing and installing the keyboard.

1. Ensure that the POWER switch is set to OFF, then disconnect the power cord from the 115Vac, 60Hz power source.
2. Tilt the typewriter cover upward to expose the platen.
3. Depress the two platen release levers and lift the platen from the typewriter.

4. Raise the left-hand lever switch bank that supports the MARG LEFT/ RIGHT and TAB CLEAR/SET levers.

5. Raise the right-hand lever switch bank that supports the SINGLE/DOUBLE and 10/12 levers.

6. Pull forward on the two upper case release levers and remove the upper case from the typewriter.

7. Disconnect the Keyboard Interface edge connector A7P2.

8. Tilt the typewriter upward and rest it on its rear panel.

9. While supporting the keyboard, remove the four screws that secure the keyboard and carefully lift it from the case.

10. Reverse this procedure when installing the keyboard into the typewriter case.

8.4 TRANSPORT REMOVAL AND INSTALLATION

REMOVAL

Use the following procedure for removing a transport from the console.

1. Ensure that the POWER switch is set to OFF, then disconnect the power cord from the 115Vac, 60Hz power source.

2. Remove both side access panels from the console by grasping the lower edge of each panel and pulling it away from the frame structure. Lift them up and away from the frame.

3. Disconnect the internal interconnection cable, i.e., R/W Tape Control (PWA17) to Tape Read/Write (R/W J2) or RO Tape Control (PWA20) to Tape Read Only (RO J2).

4. Loosen the three screws that secure the clear plastic terminal board cover to the terminal strip, located on the left-hand side of the transport.

5. Loosen each of the five front-most terminal screws and remove each lead. Label each as it is removed. Refer to Table 8-1.

NOTE: These leads run from the top of the card cage to the terminal strip and supply power to the transport.

Table 8-1. Transport Power Connections

TERMINAL	VOLTAGE
1	No Connection
2	+5.12 Vdc
3	+15 Vdc
4	-15 Vdc
5	No Connection
6	+24 Vdc
7	No Connection
8	Ground

6. Remove the four screws that secure the cassette mounting brackets to the frame. There are two screws on each side of the transport.

CAUTION

When removing the two screws on the left-hand side of the transport, use care so as not to damage the pins on connectors J1 and J2.

7. Carefully slide the transport toward the rear of the console until the door clears the frame.

INSTALLATION

Use the following procedure for installing a transport into the console.

1. Ensure that the POWER switch is set to OFF, then disconnect the power cord from the 115Vac, 60Hz power source.
2. Remove both side access panels from the console by grasping the lower edge of each panel and pulling it away from the frame structure. Lift them up and away from the frame.
3. Carefully slide the transport into the console from the rear. Position it so that the window in the door is toward the top and the door is aligned in the center of the opening.
4. Align the four slots in the cassette mounting bracket (two on each side) with the holes in the frame.
5. Place a screw in each and loosely tighten.
6. Position the transport side-to-side so that there is an equal space at either side of the transport door, then tighten all four screws.

NOTE: If there is not an equal space at the top and bottom of the door, loosen the two screws on either side of the transport that secure the transport to the mounting brackets. Reposition the transport up-and-down so that there is an equal space at the top and bottom of the transport door, then tighten all four screws. Ensure that the transport door opens with no interference.

7. Connect the five leads, removed in step 5 of the removal procedure, to the appropriate terminal and secure in place.
8. Connect the internal connection cable, i.e., R/W Tape Control (PWA17) to Tape Read/Write (R/W J2) or RO Tape Control (PWA20) to Tape Read Only (RO J2).

8.4.1 Head Assembly Removal and Installation

REMOVAL

Use the following procedure for removing the head assembly from the transport.

1. Remove the transport as outlined in paragraph 8.4 (Removal).
2. Remove the head assembly coaxial cable from the pins of connector J2 (See Table 8-2) by grasping the body of the pin connectors and sliding them off the end of the pins. Label each as it is removed.

   NOTE: If necessary, cut any ties that secure the coaxial cable to the transport harness.

   The RO will have a single coaxial cable (read head), while the R/W will have two coaxial cables (read head and write head).

Table 8-2. Head Assembly Connections

READ ONLY		READ/WRITE		
PIN	COLOR		PIN	COLOR
J2-1	red	READ	J2-1	red
J2-3	white		J2-3	white
J2-5	shield		J2-5	shield
		WRITE	J2-29	shield
			J2-33	red
			J2-35	black

3. Remove the cassette holder faceplate by removing the four screws (two on each side) that secure it to the cassette holder assembly.

4. Remove the hinge pin by pushing it through the cassette holder.

   NOTE: Retain the spring washer.

5. Remove the head mounting plate assembly by loosening the two screws that secure the head mounting plate assembly to the cassette holder.

INSTALLATION

Use the following procedure for installing the head mounting plate assembly into the transport.

1. Remove the transport, cassette holder faceplate, and hinge pin as outlined in paragraph 8.4.1 (Removal).

2. Ensure that the two screws with lock washers are started into the mounting holes of the head mounting plate assembly.

   NOTE: Do not tighten these screws as they must pass into the slots of the cassette holder.

3. Hold the cassette holder so that the head mounting plate assembly mounting slots face up.

4. Slide the head mounting plate assembly into the cassette holder with the long flat side positioned up.

5. Ensure that the two screws are positioned in the slots of the cassette holder and that the lock washers are positioned between the screw heads and the cassette holder.

6. Carefully slide the Cassette, Motor, and Sensor Adjustment Tool P/N 88016036 into the cassette holder and align the head such that the tool will slide into the tape guide pins on either side of the head mounting plate assembly.

7. Tighten the two screws to secure the head mounting plate assembly to the cassette holder.

   NOTE: Ensure that the protrusion on the right-hand side of the head mounting plate assembly is against the latch side of the cassette holder.

8. Remove the Cassette, Motor, and Sensor Adjustment Tool and place the spring washer into the hole in the right-hand tab of the cassette main frame.

9. Assemble the cassette holder to the cassette main frame and push the hinge pin through to hold the assembly in place.

10. Replace the cassette holder faceplate using the four screws removed in step 3 of the removal procedure.

11. Reconnect all wiring as outlined in step 2 of the removal procedure.

12. Replace the transport as outlined in the installation procedure in paragraph 8.4

8.4.2 Motor Removal and Installation

REMOVAL

Use the following procedure for removing a motor from the transport.

1. Remove the transport as outlined in paragraph 8.4 (Removal).
2. Remove the cassette holder faceplate by removing the four screws (two on each side) that secure it to the cassette holder assembly.
3. Unsolder and remove the leads on the motor. Label each as it is removed.
4. Remove the two screws that secure the motor to the cassette main frame.

INSTALLATION

Use the following procedure for installing the motor into the transport.

1. With the transport and motor removed as outlined in paragraph 8.4.2 (Removal), install the new motor by replacing the two screws previously removed.

   NOTE: Do not tighten these screws.

2. Release the cassette holder and carefully slide the Cassette, Motor, and Sensor Adjustment P/N 88016036 into place.
3. Latch the cassette holder back into place and place a Motor Positioning Insert P/N 70015833 over the shaft of the motor.
4. Alternately, tighten the two motor screws until the motor is secured in place.

   NOTE: The Motor Positioning Insert must slide on and off of the motor shaft with no interference once the motor screws have been tightened.

5. Remove the Motor Positioning Insert.
6. Release the cassette holder and carefully remove the Cassette, Motor, and Sensor Adjustment Tool.
7. Replace the drive coupling on the shaft of the motor and tighten the set screw. Ensure that the set screw is on the flat side of the motor shaft.
8. Replace the cassette holder faceplate using the four screws previously removed.
9. Reconnect all wiring as outlined in step 3 of the removal procedure.
10. Replace the transport as outlined in the installation procedure in paragraph 8.4.

8.4.3 Door Latch Solenoid Removal and Installation

Use the following procedure for removing and installing the door latch solenoid.

1. Remove the transport as outlined in paragraph 8.4 (Removal).
2. Remove both lock solenoid leads from pin J1-27 and pin 6 of the terminal strip.
3. Remove the two screws that secure the door latch solenoid and solenoid plunger stop to the cassette main frame.
4. Reverse this procedure when installing the door latch solenoid.
5. Adjust the solenoid plunger stop for a gap of 0.005-to 0.020-inch between the plastic tip and the body of the solenoid with the plunger contacting the solenoid plunger stop.

8.4.4 BOT/EOT Sensor Assembly Removal and Installation

REMOVAL

Use the following procedure for removing the BOT/EOT sensor assembly.

1. Remove the transport as outlined in paragraph 8.4 (Removal).
2. Remove the cassette holder faceplate by removing the four screws (two on each side) that secure it to the cassette holder assembly.
3. Remove the four BOT/EOT sensor assembly leads from the pins of connector J1 (See Table 8-3) by grasping the body of the pin connectors and sliding them off the end of the pins. Label each as it is removed.

   NOTE: If necessary, cut any ties that secure the leads to the transport harness.

Table 8-3. BOT/EOT Sensor Assembly Connections

PIN	SIGNAL	LENGTH
J2-12	Source Bias	10-1/2"
J2-17	Sensor Bias	11-1/4"
J2-47	Source Drive	13-1/4"
J2-48	Sensor Output	12"

If the leads are not marked, they may be identified by lead length. See Table 8-3.

4. Remove the screw, spacer, washer, and nut that secures the BOT/EOT sensor assembly to the cassette holder.

INSTALLATION

Use the following procedure for installing the BOT/EOT sensor assembly.

1. With the transport and BOT/EOT sensor assembly removed as outlined in paragraph 8.4.4 (Removal), install the new BOT/EOT sensor assembly by replacing the screw, spacer, washer, and nut previously removed.

   NOTE: Do not tighten this screw.

2. Route the leads and reconnect as outlined in Table 8-3. Replace the ties, as required.

3. Release the cassette holder and carefully slide the Cassette, Motor, and Sensor Adjustment Tool P/N 88016036 into place.

4. Latch the cassette holder back into place.

5. Connect the DMM plus lead to J1-17 and the ground lead to ground.

6. Connect the power cord to a 115Vac, 60Hz power source.

7. Set CB1 to ON.

CAUTION

Use care when probing power circuits.
An AC voltage level of 115Vac is present
in the power supply section when the
POWER pushbutton is depressed to OFF.

8. Depress the POWER switch to ON.

9. Position the BOT/EOT sensor assembly back and forth until a minimum voltage indication is present, then tighten the screw.

8.4.5 Cassette In Place Switch and File Protect Switch Removal and Installation

REMOVAL

Use the following procedure for removing the cassette in place or file protect switches from the transport.

1. Remove the transport as outlined in paragraph 8.4 (Removal).

2. Unsolder and remove the leads on the respective switch. Label each lead as it is removed. Refer to Table 8-4.

Table 8-4. Cassette In Place Switch and File Protect Switch Connections

CASSETTE IN PLACE SWITCH (S1)		FILE PROTECT SWITCH (S2)	
PIN	CONNECTION	PIN	CONNECTION
J2-15	NO	J2-31	NO
J2-49	NC	J1-2	C
J1-2	C		

3. Remove the two screws that secure the switches to the cassette holder.

NOTE: Retain the spacer, flat washers, and hex nuts.

INSTALLATION

Use the following procedure for installing the cassette in place or file protect switches into the transport.

1. With the transport and switches removed as outlined in paragraph 8.4.5 (Removal), install the new switch or switches. First replace the spacer, then the file protect switch (longest actuator), followed by the cassette in place switch, the two flat washers and two hex nuts.
2. Reconnect all wiring as outlined in step 2 of the removal procedure.
3. Release the cassette holder and carefully slide the Cassette, Motor, and Sensor Adjustment Tool P/N 88016036 into place.
4. Check to see that the file protect switch makes as the door is closed and breaks when the actuator enters the cutout in the tool.
5. Remove the Cassette, Motor, and Sensor Adjustment Tool and place a cassette into the cassette holder.
6. Check to see that the drive couplings engage the cassette driving lugs before the cassette in place switch makes. With the actuator resting on the edge of the cassette, check to see that a 0.002-to 0.007-inch gap exists between the arm of the acutator and the body of the switch. If not properly adjusted, loosen the two screws and reposition the switch.

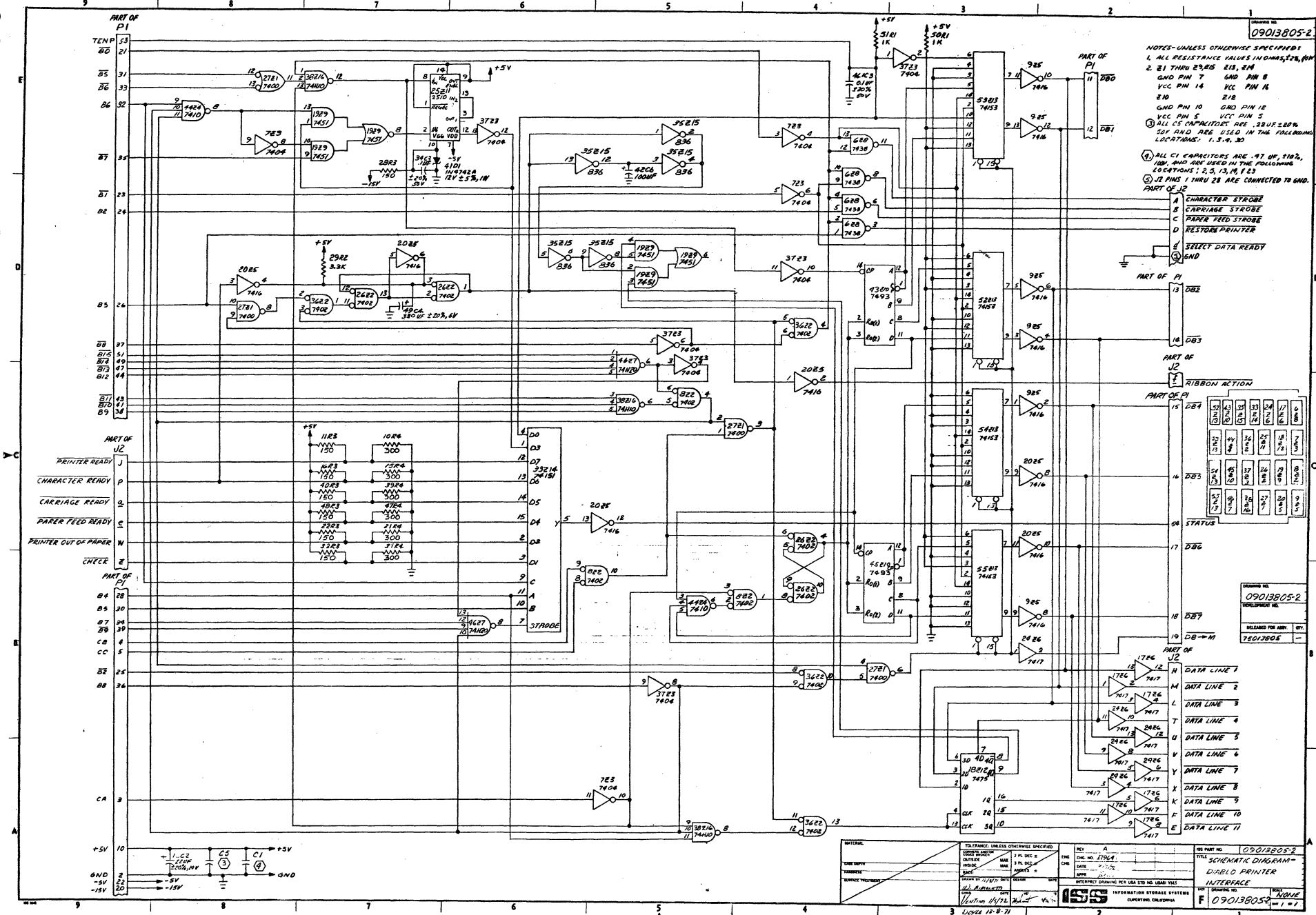
CHAPTER 9
DIAGRAMS

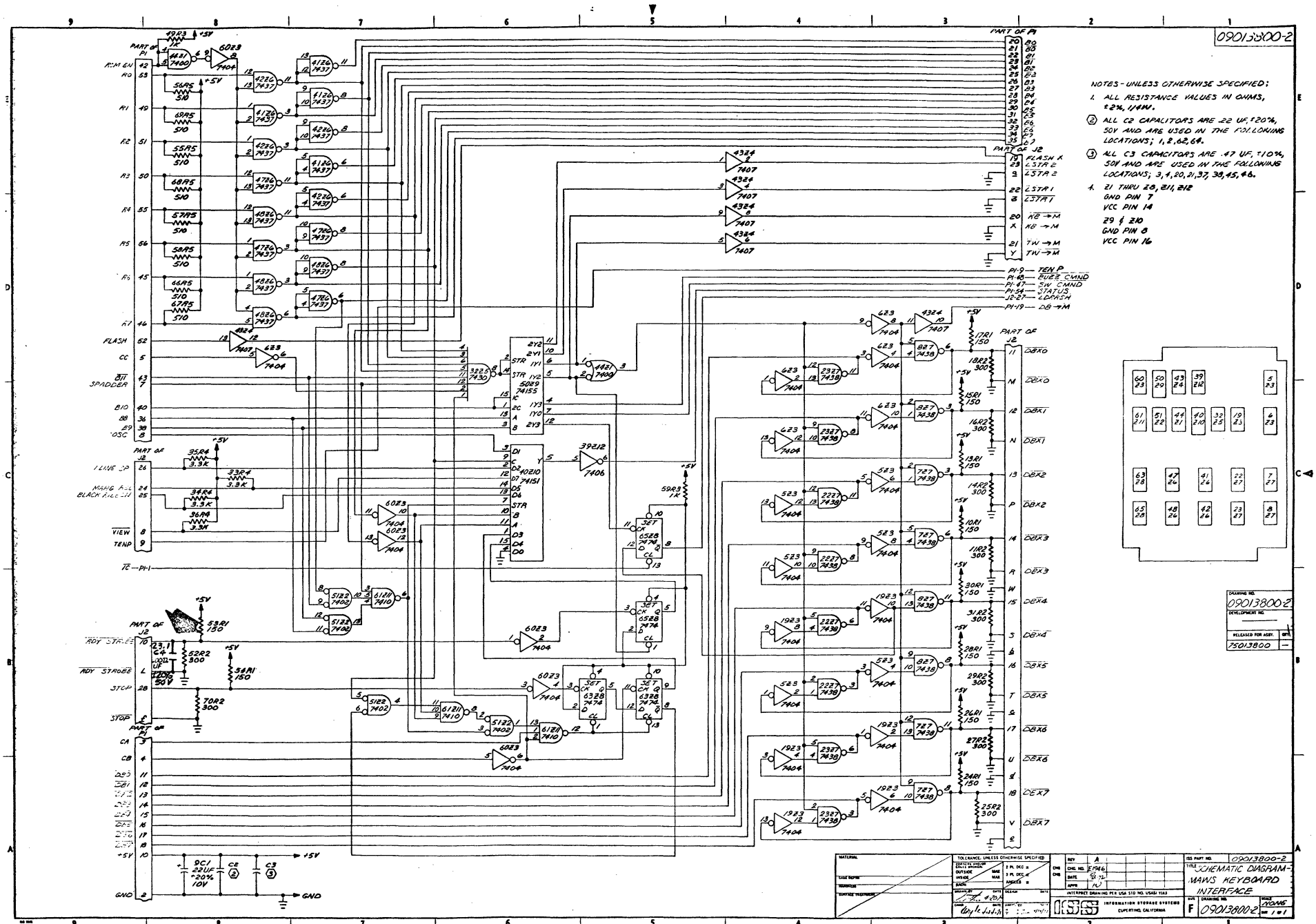
9.1 GENERAL

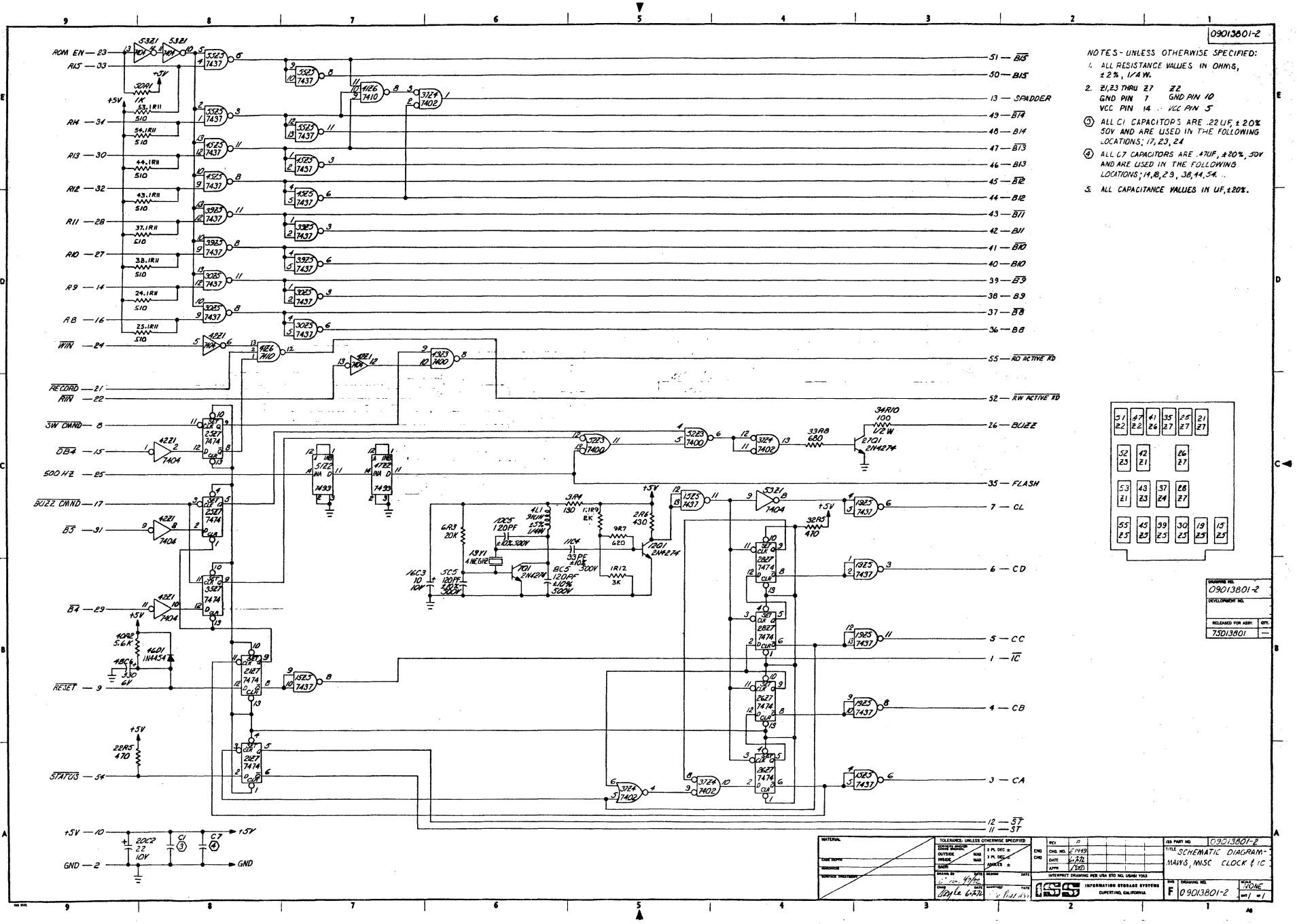
The diagrams contained in this manual are listed and arranged as shown in Table 9-1. Also included is the system wire list.

Table 9-1. Diagrams

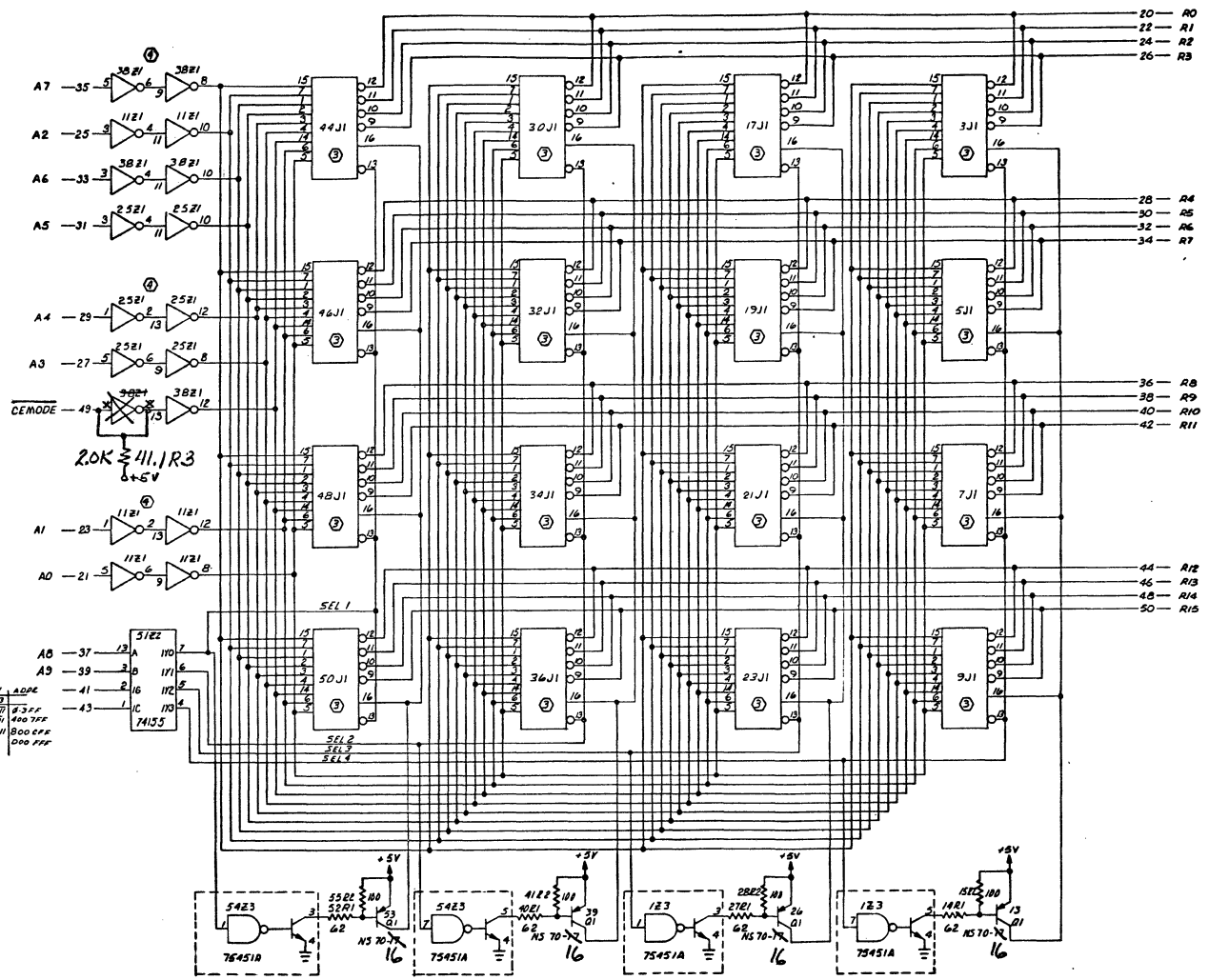
PWA	TITLE	PART NUMBER
1	Printer Interface	75013805
3	Keyboard Interface	75013800
4	Miscellaneous, Clock and I. C.	75013801
5, 6, 7, 8	ROM Program	75014400
9	ROM Address Register	75013749
10	Return Address Register	75013750
11	Main and General Purpose Register	75013747
12	Arithmetic Logic Unit	75013748
13, 15	Buffer I/O (Read Only & Read/Write)	75013735
14, 16	Buffer Control (Read Only & Read/Write)	75013563
17, 20	Tape Control (Read/Write & Read Only)	75013733
18, 21	Read Decode (Read/Write & Read Only)	75013731
19	Write Encode (Read/Write)	75013732
R/W J1, RO J1	Motor Control	75013804
- - -	Cassette Heat Sink	- - -
R/W J2, RO J2	Tape Read/Write, Tape Read Only	75013564
R/W - RO Display Panel	Display Panel	75013809
- - -	DC Power Supply	- - -
- - -	Keyboard Logic	- - -
27	PDA ROM and Controls	75013813
28	PDA Switch and Indicator	75013812


PART OF P1
PART OF J2
PRINTER READY
CHARACTER READY
CARRIAGE READY
PAPER FEED READY
PRINTER OUT OF PAPER
CHECK
STROBE
+5V
-5V
-15V
GND
DATA LINE 1
DATA LINE 2
DATA LINE 3
DATA LINE 4
DATA LINE 5
DATA LINE 6
DATA LINE 7
DATA LINE 8
DATA LINE 9
DATA LINE 10
DATA LINE 11
CHARACTER STROBE
CARRIAGE STROBE
PAPER FEED STROBE
RESTORE PRINTER
SELECT DATA READY
RIBBON ACTION
STATUS
NOTES-UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES IN OHMS, ±5%, 1/4W
2. 21 THRU 29, 215 213, 214
GND PIN 7 GND PIN 8
VCC PIN 14 VCC PIN 16
210 218
GND PIN 10 GND PIN 12
VCC PIN 5 VCC PIN 3
3. ALL C5 CAPACITORS ARE .22UF ±20%
50V AND ARE USED IN THE FOLLOWING LOCATIONS: 1, 3, 4, 30
4. ALL C1 CAPACITORS ARE .47 UF, ±10%, 100V, AND ARE USED IN THE FOLLOWING LOCATIONS: 2, 5, 13, 19, 23
5. J2 PINS 1 THRU 28 ARE CONNECTED TO GND.
09013805-2
ISS
INFORMATION STORAGE SYSTEMS
CUPERTINO, CALIFORNIA
SCHEMATIC DIAGRAM-
DIABLO PRINTER
INTERFACE


09013800-2
NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4W.
2. ALL C2 CAPACITORS ARE .22 UF, ±20%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 1, 2, 62, 64.
3. ALL C3 CAPACITORS ARE .47 UF, ±10%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 3, 4, 20, 21, 37, 38, 45, 46.
4. 21 THRU 28, 211, 212 GND PIN 7 VCC PIN 14
29 & 210 GND PIN 8 VCC PIN 16
PART OF P1
PART OF J2
+5V
GND
DRAWING NO. 09013800-2
DEVELOPMENT NO.
RELEASED FOR ASSY. 75013800
TITLE SCHEMATIC DIAGRAM-MAWS KEYBOARD INTERFACE
SIZE F
DRAWING NO. 09013800-2
SCALE NONE
SHEET 1 of 1
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA


09013801-2
NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4 W.
2. Z1,23 THRU Z7 Z2
GND PIN 7 GND PIN 10
VCC PIN 14 VCC PIN 5
3. ALL C1 CAPACITORS ARE .22 UF, ±20% 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 17, 23, 24
4. ALL C7 CAPACITORS ARE .47UF, ±20%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 14, 8, 29, 38, 44, 54.
5. ALL CAPACITANCE VALUES IN UF, ±20%.
ROM EN — 23
A15 — 33
RA — 34
A13 — 30
A12 — 32
A11 — 28
A10 — 27
A9 — 14
A8 — 16
WIN — 24
RECORD — 21
RIN — 22
SW CMND — 8
DB4 — 15
500 HZ — 25
BUZZ CMND — 17
B3 — 31
B4 — 29
RESET — 9
STATUS — 54
+5V — 10
GND — 2
51 — B15
50 — B15
13 — SPADDER
49 — B14
48 — B14
47 — B13
46 — B13
45 — B12
44 — B12
43 — B11
42 — B11
41 — B10
40 — B10
39 — B9
38 — B9
37 — B8
36 — B8
55 — RO ACTIVE RD
52 — RW ACTIVE RD
26 — BUZZ
35 — FLASH
7 — CL
6 — CD
5 — CC
1 — IC
4 — CB
3 — CA
12 — S7
11 — S7
09013801-2
75013801
SCHEMATIC DIAGRAM - MAIN, MISC CLOCK & IC
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA

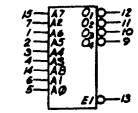
09014400-1



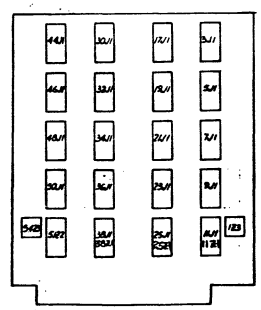
CARD LOC	CARD NO.	PIN 41	PIN 43	ADDR
J7	1	A10	A11	8 3FF
J8	2	A10	A11	400 7FF
J9	3	A10	A11	800 BFF
J10	4	A10	A	C00 FFF

NOTES - UNLESS OTHERWISE SPECIFIED:

1. Z1
   GND PIN 7
   VCC PIN 14
   Z2 AND J1, Z3
   GND PIN 5 GND PIN 4
   VCC PIN 16 VCC PIN 8
3. J1 (Z4 THRU Z19) CONFIGURATION:



4. ALL Z1 IC'S ARE 7404
5. ALL C1 CAPACITORS ARE .047 UF, ±20%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 10, 24, 37, 42
6. ALL RESISTANCE VALUES IN OHMS, ± 2%, 1/4 W.
7. ALL C3 CAPACITORS ARE .01UF, ±20%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 2, 4, 6, 8, 16, 18, 20, 22, 29, 31, 33, 35, 43, 45, 47, 49



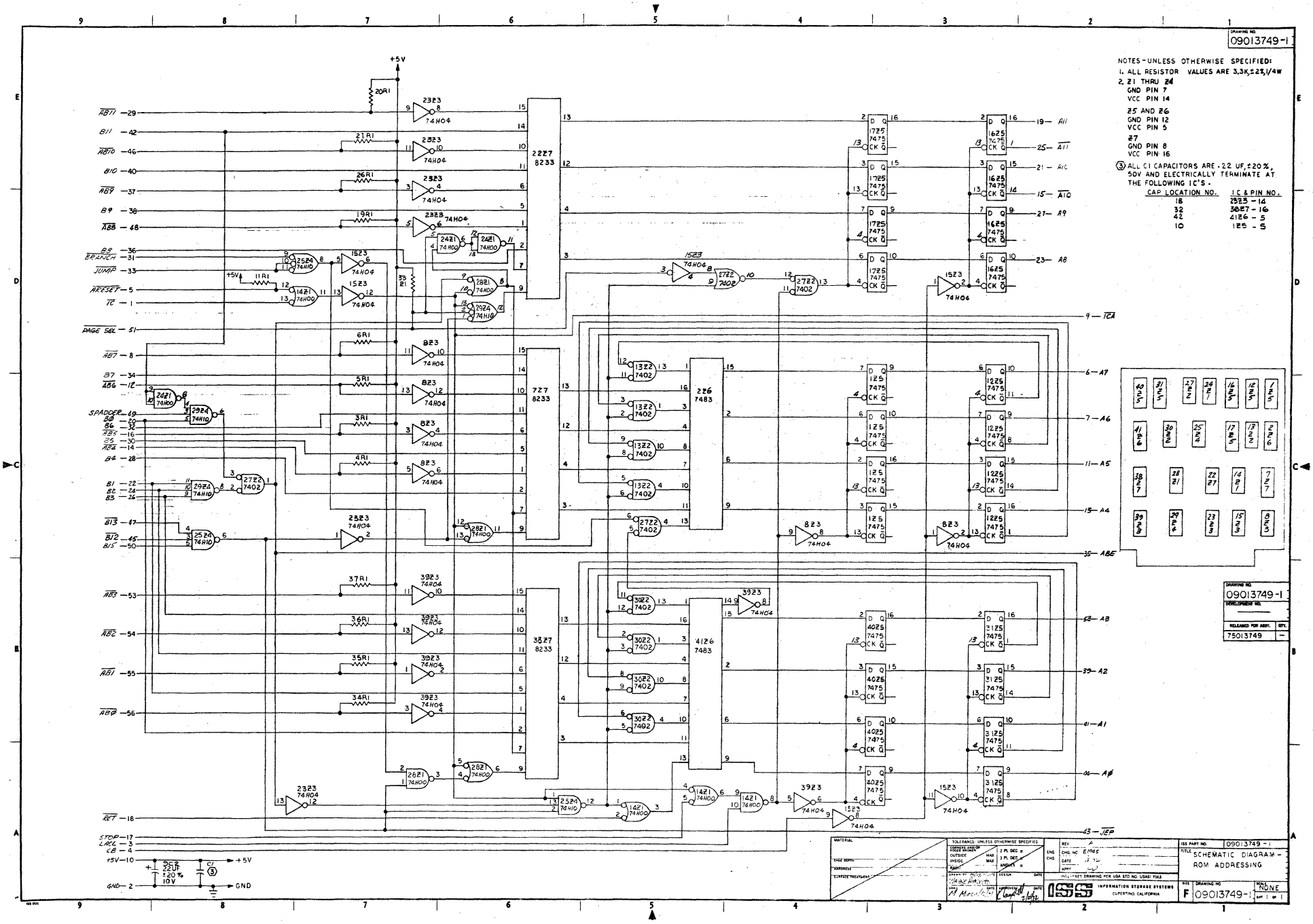
Drawing No.	09014400-1
Development No.	
Released for Assy.	Qty.
75014400	—

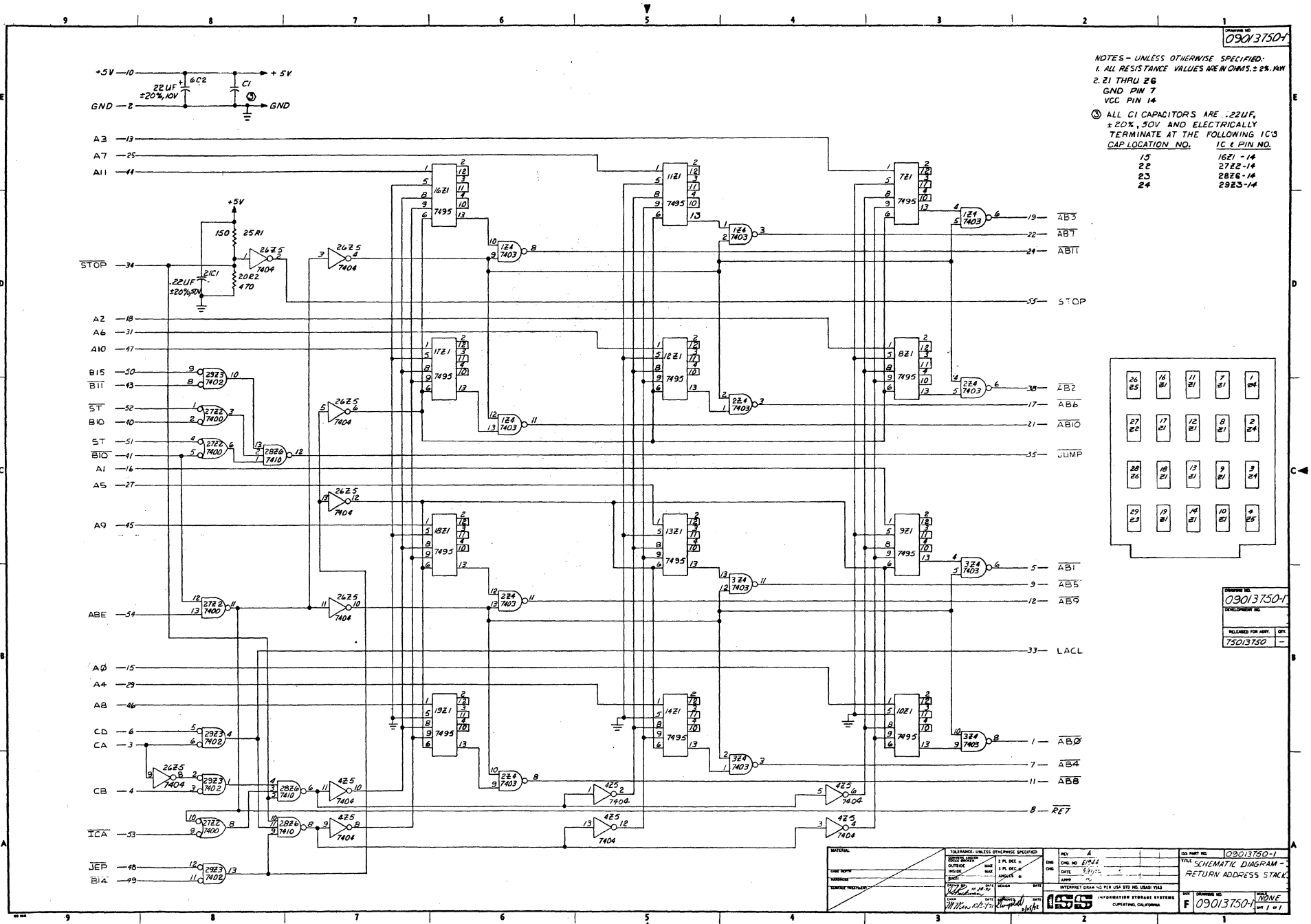
REV	PDD	PDD1	PDD1	PDD	ISS PART NO. 09014400-1
CHG NO.	6628	32444087	25182		TITLE SCHEMATIC DIAGRAM- ROM CONTROL MEMORY
DATE	9/6/72	6/6/73	8/5/73	11/6/73	
APPR		7/24	7/24	7/24	

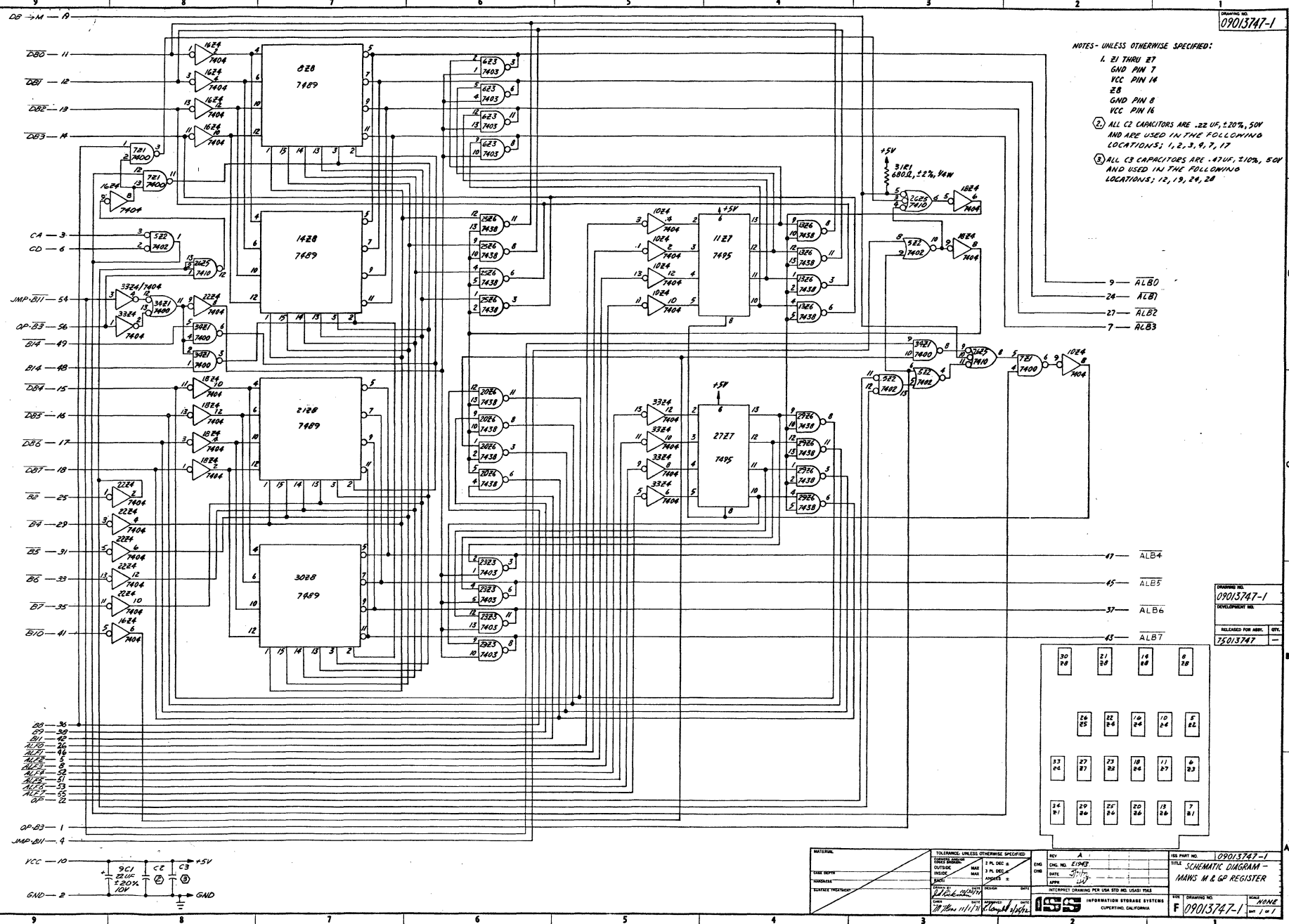
INTERPRET DRAWING PER USA STD NO. USASI Y14.2

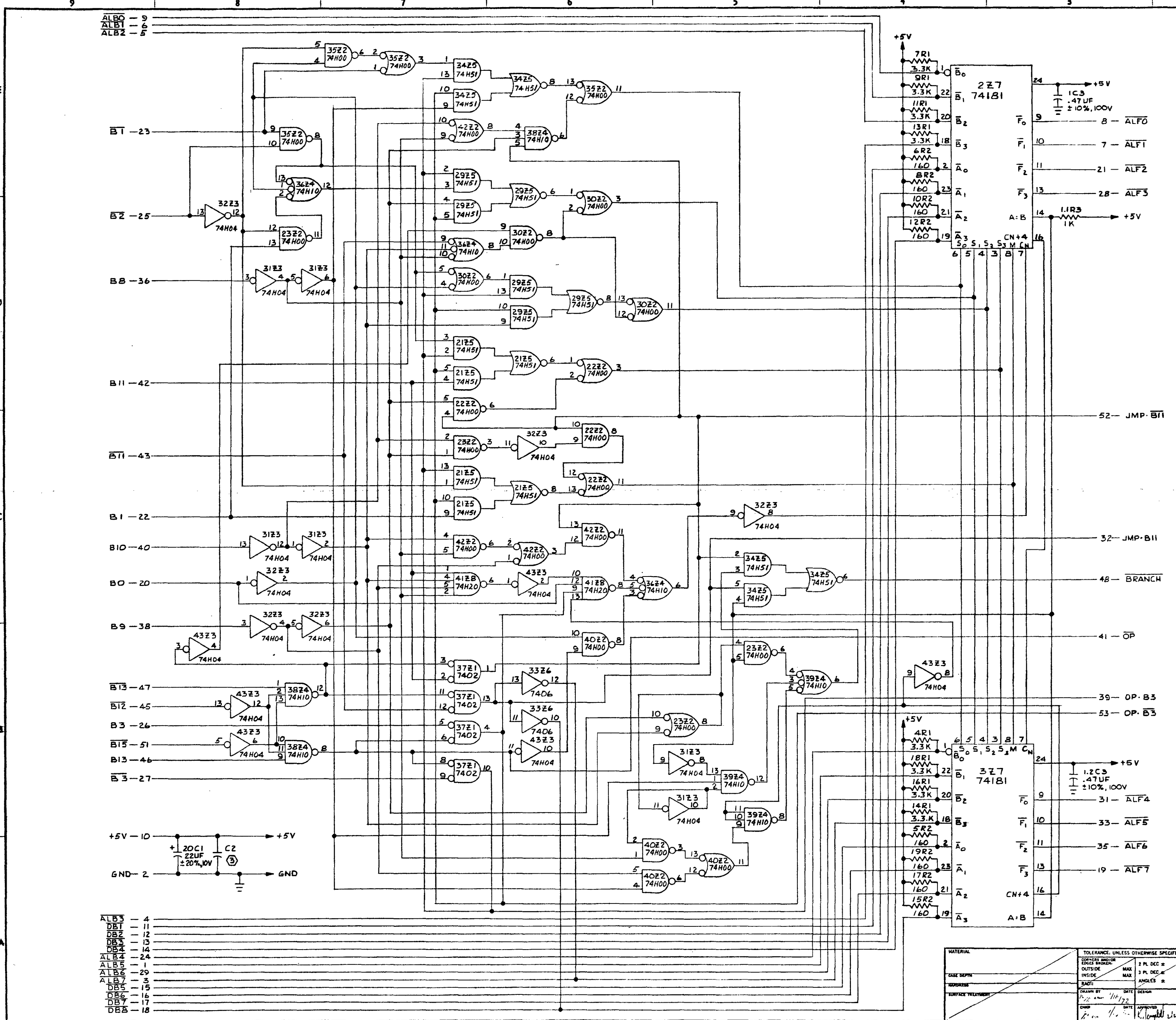
ISS INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA

SIZE F | DRAWING NO. 09014400-1 | SCALE NONE | SHT 1 of 1


DRAWING NO. 09013749-1
NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTOR VALUES ARE 3.3K, ±2%, 1/4W
2. Z1 THRU Z4
GND PIN 7
VCC PIN 14
Z5 AND Z6
GND PIN 12
VCC PIN 5
Z7
GND PIN 8
VCC PIN 16
③ ALL C1 CAPACITORS ARE .22 UF, ±20%, 50V AND ELECTRICALLY TERMINATE AT THE FOLLOWING IC'S.
CAP LOCATION NO. | IC & PIN NO.
18 | 2323 - 14
32 | 3827 - 16
42 | 4126 - 5
10 | 125 - 5
+5V
GND
ABI1
BI1
ABI0
BI0
ABI9
BI9
ABI8
BI8
BS BRANCH
JUMP
RRESET
TC
PAGE SEL
ABI7
BI7
ABI6
SPADDER
BI6
BI5
BI4
BI3
BI2
BI1
ABI3
ABI2
ABI1
ABI0
RET
STOP
LACL
CLB
+5V
GND
20R1
21R1
26R1
19R1
11R1
33 Ω
6R1
5R1
3R1
4R1
37R1
36R1
35R1
34R1
33 Ω ±20% 10V
C1 ③
2227 8233
727 8233
3827 8233
226 7483
4126 7483
1725 7475 CK Q
1625 7475 CK Q
1225 7475 CK Q
125 7475 CK Q
4025 7475 CK Q
3125 7475 CK Q
74H04
74H00
74H10
7402
A11
A10
A9
A8
TCA
A7
A6
A5
A4
ABE
A3
A2
A1
A0
JEP
DRAWING NO. 09013749-1
DEVELOPMENT NO.
RELEASED FOR ASSY. QTY. 75013749 -
ISS PART NO. 09013749 - 1
TITLE SCHEMATIC DIAGRAM - ROM ADDRESSING
SIZE F
DRAWING NO. 09013749-1
SCALE NONE
SHT 1 OF 1
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA


09013750-1
NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 2%, ¼W
2. 21 THRU 26
GND PIN 7
VCC PIN 14
③ ALL C1 CAPACITORS ARE .22UF, ±20%, 50V AND ELECTRICALLY TERMINATE AT THE FOLLOWING IC'S
CAP LOCATION NO. IC & PIN NO.
15 16Z1 - 14
22 27Z2 - 14
23 28Z6 - 14
24 29Z3 - 14
+5V
GND
22UF ±20%, 10V
C2
C1
A3
A7
A11
A2
A6
A10
B15
B11
ST
B10
ST
B10
A1
A5
A9
ABE
AØ
A4
A8
CD
CA
CB
ICA
JEP
B14
STOP
150
25R1
21C1
22UF ±20%, 50V
20R2
470
ABØ
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
STOP
JUMP
LACL
RET
09013750-1
TSO13750
SCHEMATIC DIAGRAM - RETURN ADDRESS STACK
INFORMATION STORAGE SYSTEMS
CUPERTINO, CALIFORNIA
F
09013750-1
NONE

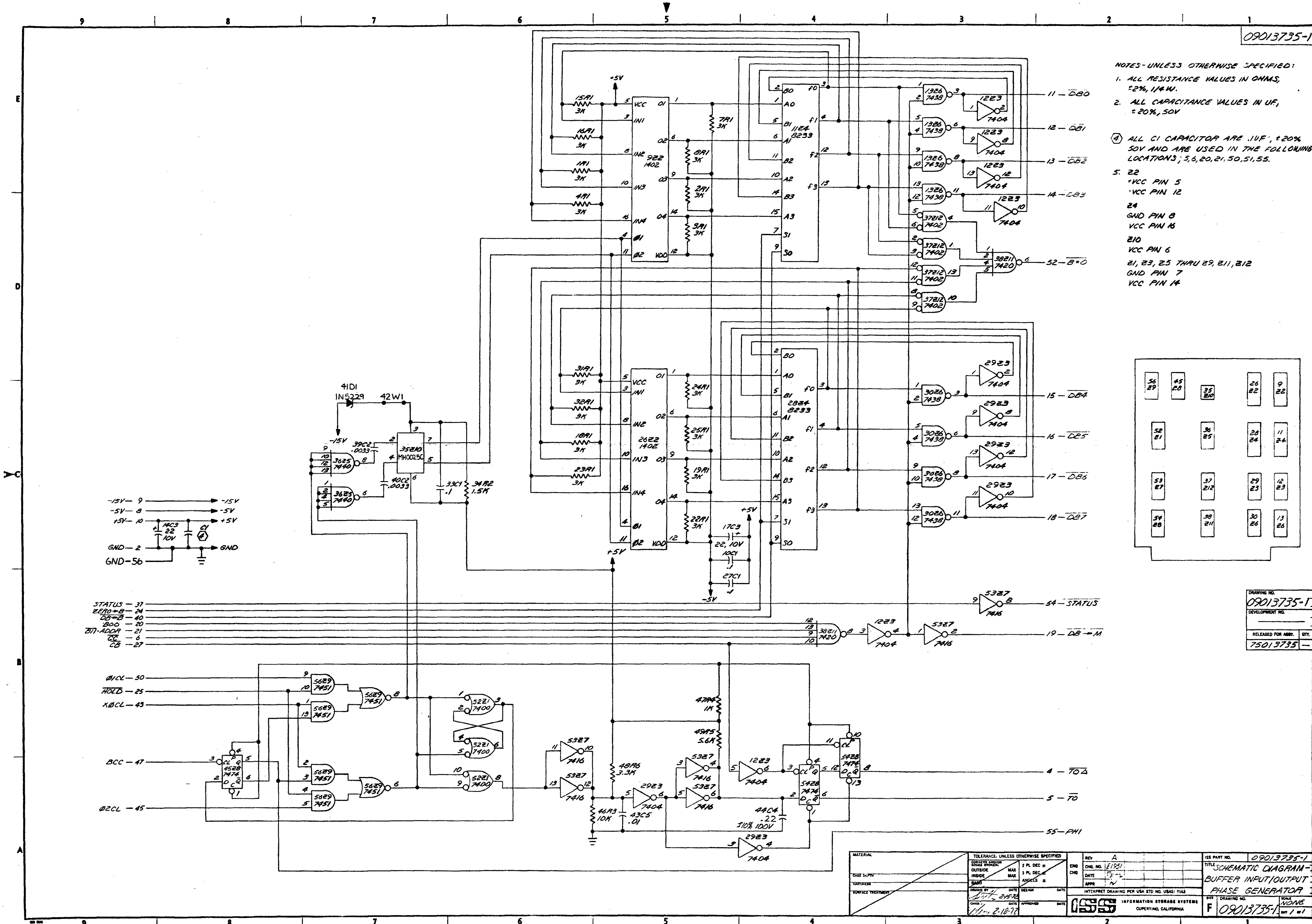

DRAWING NO. 09013747-1
NOTES- UNLESS OTHERWISE SPECIFIED:
1. Z1 THRU Z7 GND PIN 7 VCC PIN 14 Z8 GND PIN 8 VCC PIN 16
2. ALL C2 CAPACITORS ARE .22 UF, ±20%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 1, 2, 3, 9, 7, 17
3. ALL C3 CAPACITORS ARE .47UF, ±10%, 50V AND USED IN THE FOLLOWING LOCATIONS; 12, 13, 24, 28
DB → M — 19
DB0 — 11
DB1 — 12
DB2 — 13
DB3 — 14
CA — 3
CD — 6
JMP·B11 — 54
OP·B3 — 56
B14 — 49
B14 — 48
DB4 — 15
DB5 — 16
DB6 — 17
DB7 — 18
B2 — 25
B4 — 29
B5 — 31
B6 — 33
B7 — 35
B10 — 41
B9 — 36
B7 — 38
B11 — 42
ALF0 — 26
ALF1 — 46
ALF2 — 5
ALF3 — 9
ALF4 — 52
ALF5 — 51
ALF6 — 53
ALF7 — 55
OP — 12
OP·B3 — 1
JMP·B11 — 4
VCC — 10
GND — 2
C1 .22UF ±20% 10V
C2
C3
+5V
GND
1428 7489
2128 7489
3028 7489
0128 7489
1127 7495
2727 7495
9 — ALB0
24 — ALB1
27 — ALB2
7 — ALB3
47 — ALB4
45 — ALB5
37 — ALB6
43 — ALB7
DRAWING NO. 09013747-1
DEVELOPMENT NO.
RELEASED FOR ASSY. 75013747
QTY. —
MATERIAL
TOLERANCE: UNLESS OTHERWISE SPECIFIED
REV A
ENG CHG NO. E1943
CHG DATE 5/15/72
APPR
INTERPRET DRAWING PER USA STD NO. USASI Y14.5
ISS PART NO. 09013747-1
TITLE SCHEMATIC DIAGRAM — MAINS M & GP REGISTER
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA
SIZE F
DRAWING NO. 09013747-1
SCALE NONE
SHT 1 of 1

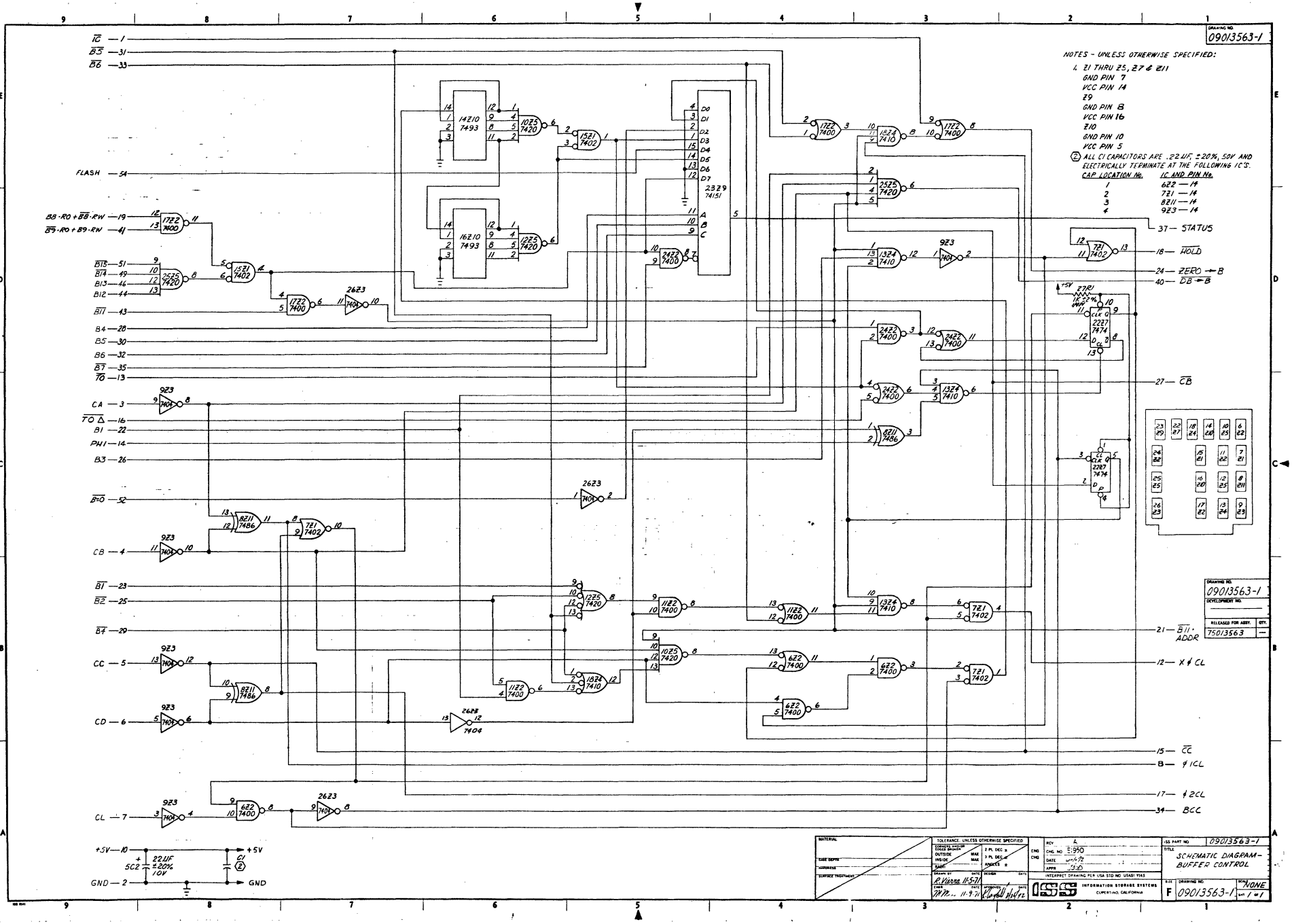


NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4W
2. Z1 THRU Z6 + Z8
GND PIN 7
VCC PIN 14
Z7
GND PIN 12
VCC PIN 24
③ ALL C2 CAPACITORS ARE .22 UF, ± 20%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 24, 25, 26, 27, 28.

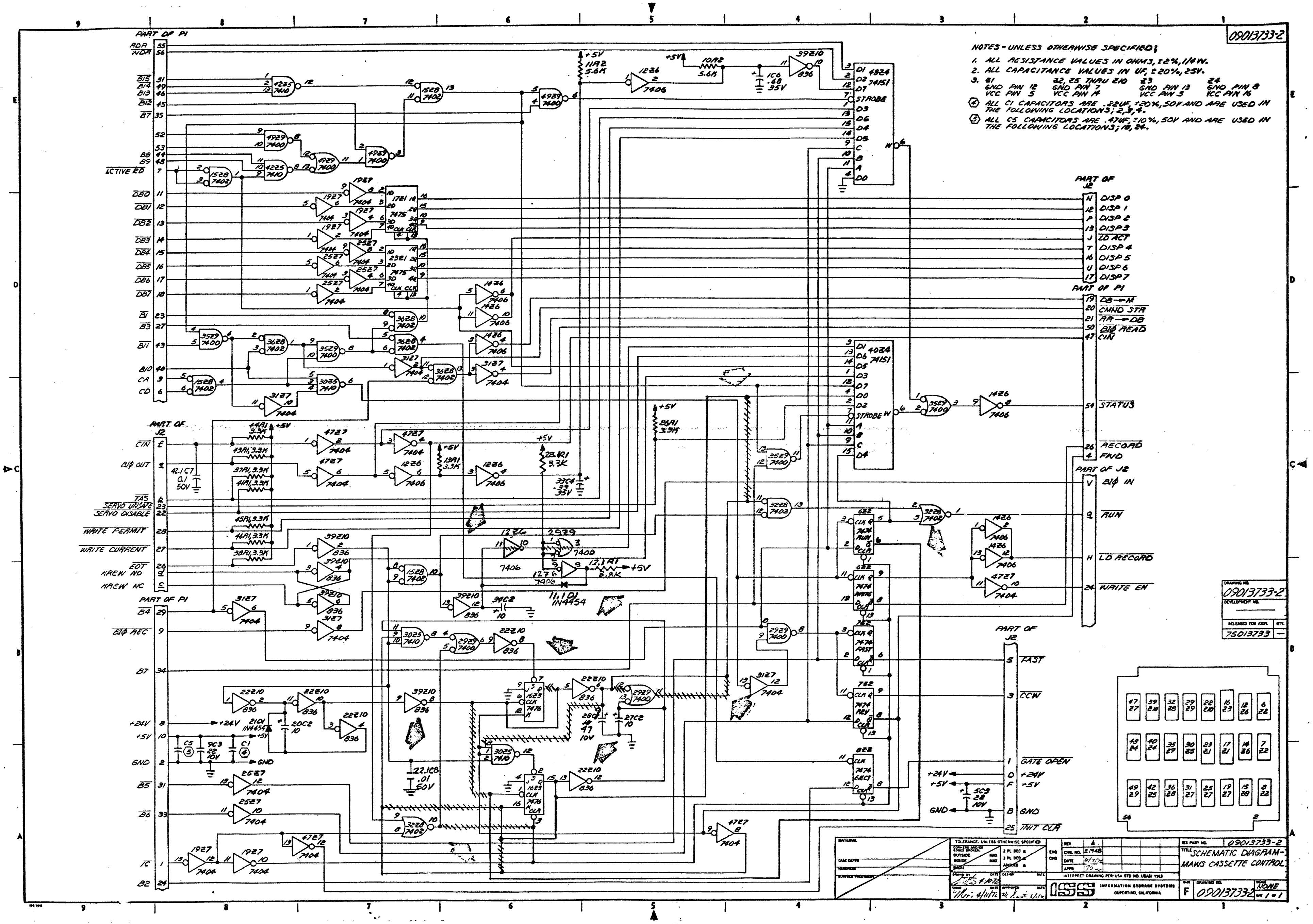
DRAWING NO. 09013748-1
RELEASED FOR ASSY. 75013748

ISS PART NO 09013748-1
TITLE SCHEMATIC DIAGRAM MAWS ARITH/LOGIC UNIT
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA
SIZE F DRAWING NO. 09013748-1 SCALE NONE SHEET 1 OF 1

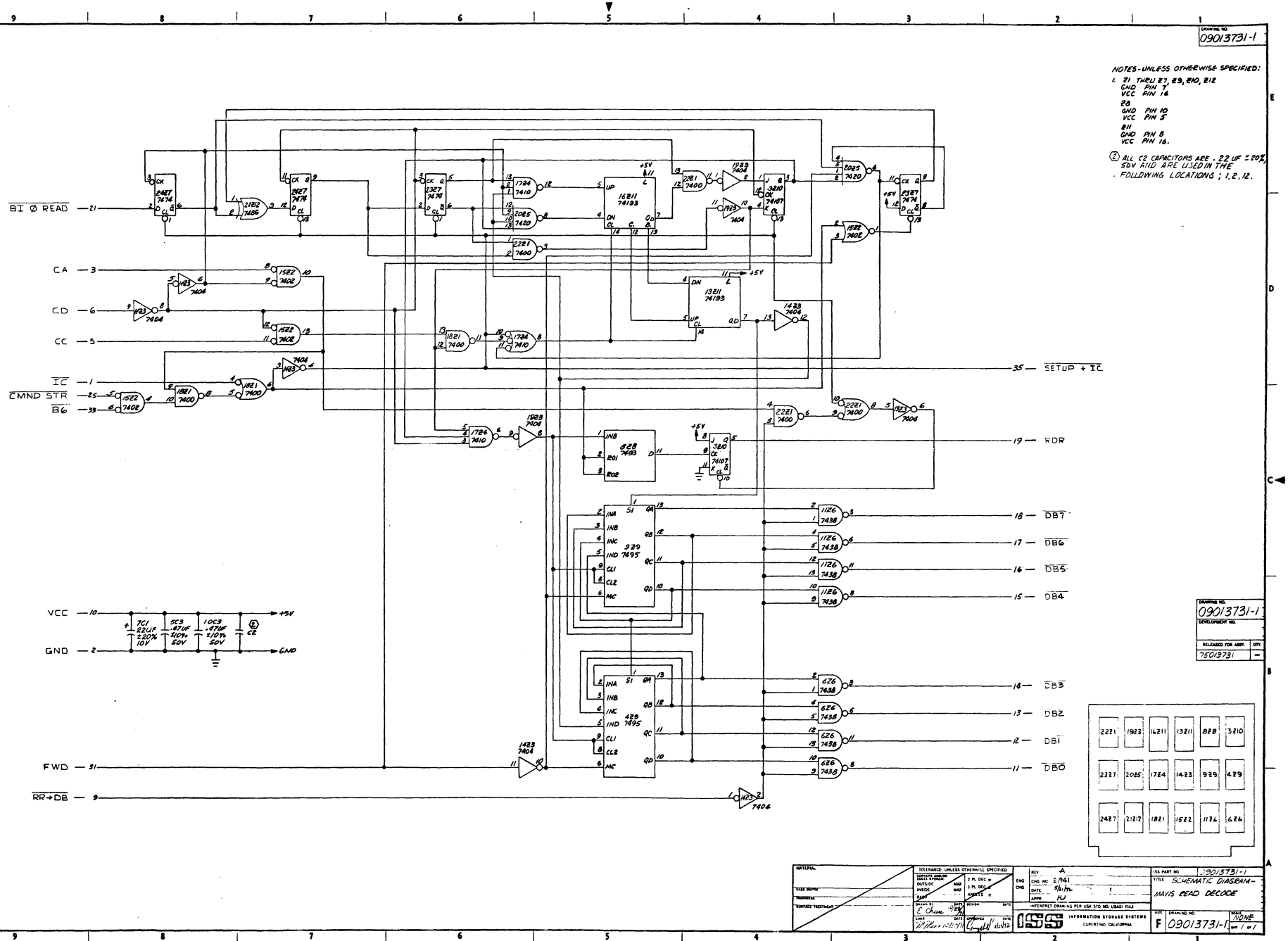

09013735-1
NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4 W.
2. ALL CAPACITANCE VALUES IN UF, ±20%, 50V
4. ALL C1 CAPACITOR ARE .1UF, ±20% 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 5,6,20,21,50,51,55.
5. Z2 +VCC PIN 5 -VCC PIN 12
Z4 GND PIN 8 VCC PIN 16
Z10 VCC PIN 6
Z1, Z3, Z5 THRU Z9, Z11, Z12 GND PIN 7 VCC PIN 14
11 — DB0
12 — DB1
13 — DB2
14 — DB3
52 — B=0
15 — DB4
16 — DB5
17 — DB6
18 — DB7
54 — STATUS
19 — DB→M
4 — TOA
5 — TO
55 — PH1
-15V — 9
-5V — 8
+5V — 10
GND — 2
GND — 56
STATUS — 37
ZERO→B — 24
DB→B — 40
B00 — 20
BII·ADDA — 21
CC — 6
CB — 27
Ø1CL — 50
HOLD — 25
XØCL — 43
BCC — 47
Ø2CL — 45
41D1 1N5229
42W1
35Z10 MH0025C
DRAWING NO. 09013735-1
RELEASED FOR ASSY. 75013735
TOLERANCE: UNLESS OTHERWISE SPECIFIED
INTERPRET DRAWING PER USA STD NO. USASI Y14.5
INFORMATION STORAGE SYSTEMS
CUPERTINO, CALIFORNIA
REV A
CHG. NO. E1951
ISS PART NO. 09013735-1
TITLE SCHEMATIC DIAGRAM - BUFFER INPUT/OUTPUT PHASE GENERATOR
SIZE F
DRAWING NO. 09013735-1
SCALE NONE
SHT 1 of 1

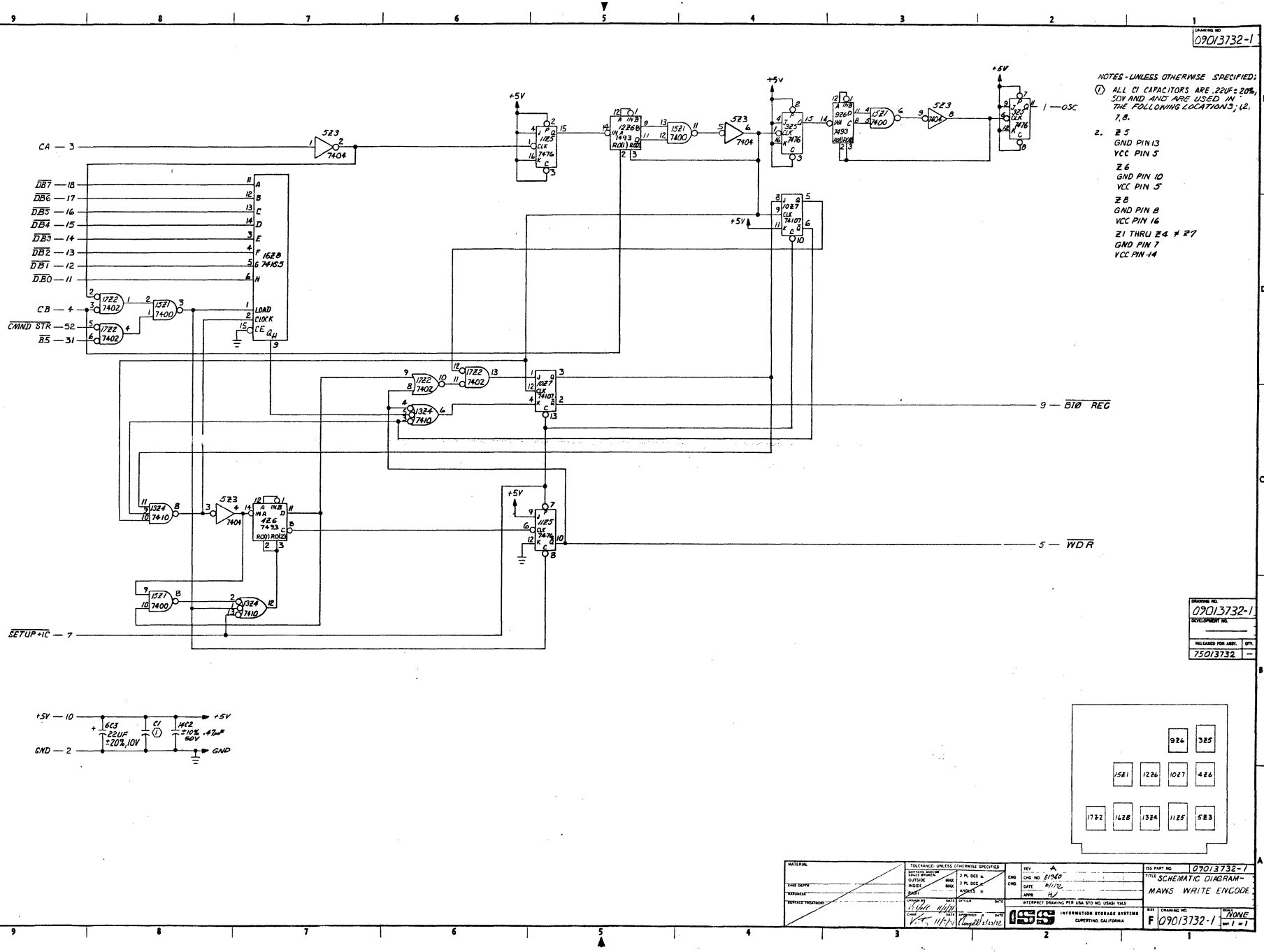

IC
B5
B6
FLASH
B8·RO + B8·RW
B9·RO + B9·RW
B15
B14
B13
B12
B11
B4
B5
B6
B7
70
CA
TO Δ
B1
PH1
B3
B0
CB
B1
B2
B4
CC
CD
CL
+5V
GND
22UF ±20% 10V
C1
(2)
NOTES - UNLESS OTHERWISE SPECIFIED:
1. Z1 THRU Z5, Z7 & Z11
GND PIN 7
VCC PIN 14
Z9
GND PIN 8
VCC PIN 16
Z10
GND PIN 10
VCC PIN 5
(2) ALL C1 CAPACITORS ARE .22 UF, ±20%, 50V AND ELECTRICALLY TERMINATE AT THE FOLLOWING IC'S.
CAP LOCATION No. IC AND PIN No.
1 622 — 14
2 721 — 14
3 8211 — 14
4 923 — 14
37 — STATUS
18 — HOLD
24 — ZERO → B
40 — DB → B
27 — CB
21 — B11 · ADDR
12 — X ∮ CL
15 — CC
8 — ∮ ICL
17 — ∮ 2CL
34 — BCC
DRAWING NO. 09013563-1
DEVELOPMENT NO.
RELEASED FOR ASSY. QTY.
75013563
SCHEMATIC DIAGRAM - BUFFER CONTROL
DRAWING NO. 09013563-1
SIZE F
SCALE NONE
SHT 1 of 1

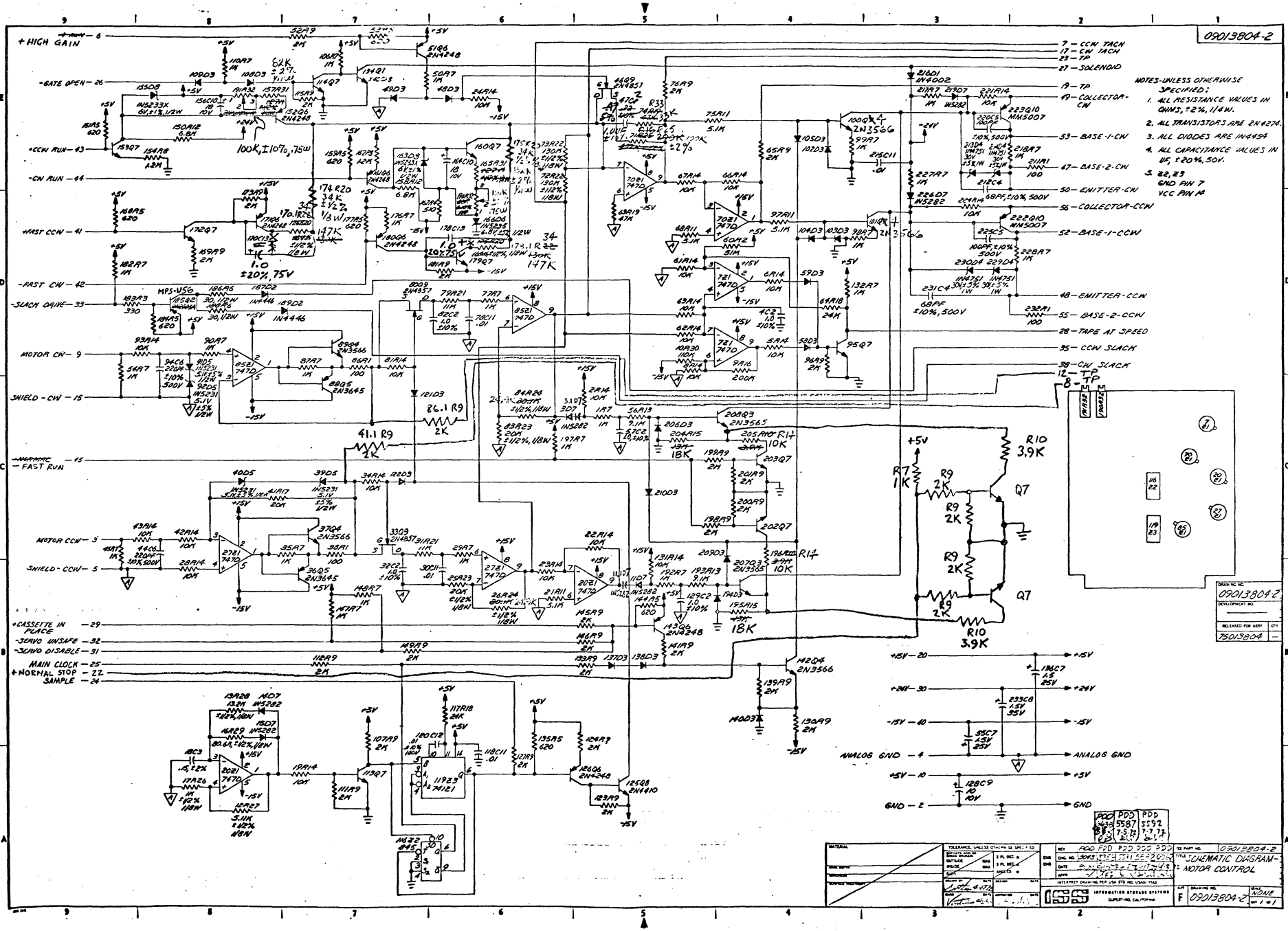
9-12

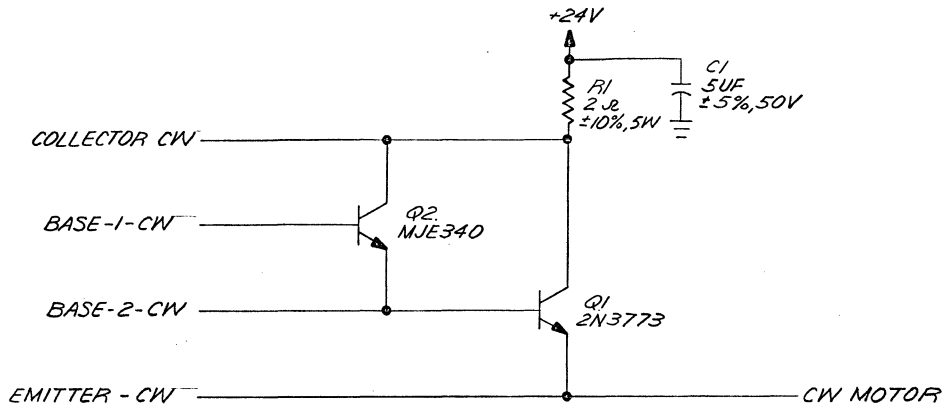

09013733-2
NOTES - UNLESS OTHERWISE SPECIFIED;
1. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4W.
2. ALL CAPACITANCE VALUES IN UF, ±20%, 25V.
3. Z1 GND PIN 12 VCC PIN 5; Z2, Z5 THRU Z10 GND PIN 7 VCC PIN 14; Z3 GND PIN 13 VCC PIN 5; Z4 GND PIN 8 VCC PIN 16
4. ALL C1 CAPACITORS ARE .22UF, ±20%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 2,3,4.
5. ALL C5 CAPACITORS ARE .47UF, ±10%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 18, 24.
PART OF P1
PART OF J2
DISP 0
DISP 1
DISP 2
DISP 3
LD ACT
DISP 4
DISP 5
DISP 6
DISP 7
STATUS
RECORD
FWD
BIØ IN
RUN
LD RECORD
WRITE EN
FAST
CCW
GATE OPEN
INIT CLR
ACTIVE RD
SERVO UNSAFE
SERVO DISABLE
WRITE PERMIT
WRITE CURRENT
TOLERANCE, UNLESS OTHERWISE SPECIFIED
ISS PART NO. 09013733-2
TITLE SCHEMATIC DIAGRAM - MAWS CASSETTE CONTROL
INTERPRET DRAWING PER USA STD NO. USASI Y14.5
ISS INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA
SIZE F
DRAWING NO. 09013733-2
SCALE NONE
SHT 1 OF 1
RELEASED FOR ASSY. 75013733

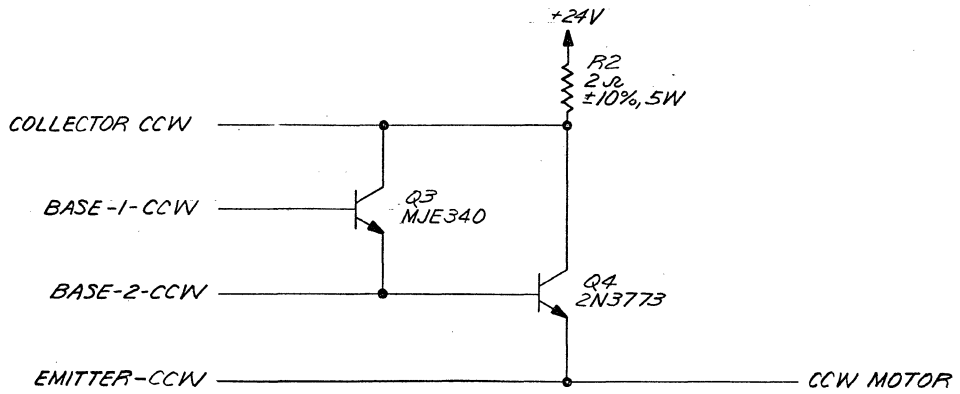
2441-1


DRAWING NO. 09013731-1
NOTES-UNLESS OTHERWISE SPECIFIED:
1. 21 THRU 27, 29, 210, 212
GND PIN 7
VCC PIN 14
29
GND PIN 10
VCC PIN 5
211
GND PIN 8
VCC PIN 16.
2 ALL C2 CAPACITORS ARE .22 UF ±20%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 1,2,12.
BI Ø READ
CA
CD
CC
IC
CMND STR
BG
FWD
RR→DB
VCC
GND
SETUP + IC
RDR
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
C1 22UF ±20% 10V
C3 .47UF ±10% 50V
10C3 .47UF ±10% 50V
C2
+5V
GND
DRAWING NO. 09013731-1
DEVELOPMENT NO.
RELEASED FOR ASSY. QTY. 75013731 —
2221 1923 14211 13211 828 3210
2327 2025 1724 1423 929 429
2427 21212 1821 1522 1126 626
ISS PART NO. 09013731-1
TITLE SCHEMATIC DIAGRAM-MAYIS READ DECODE
SIZE F DRAWING NO. 09013731-1
SHEET NONE
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA


CA — 3
CB — 4
CMND STR — 52
B5 — 31
DB7 — 18
DB6 — 17
DB5 — 16
DB4 — 15
DB3 — 14
DB2 — 13
DB1 — 12
DB0 — 11
SETUP+IC — 7
+5V
GND — 2
LOAD
CLOCK
CE
9 — BIØ REG
5 — WDR
1 — OSC
NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL C1 CAPACITORS ARE .22UF ± 20%, 50V AND AND ARE USED IN THE FOLLOWING LOCATIONS; L2, 7, 8.
2. Z5 GND PIN 13 VCC PIN 5
Z6 GND PIN 10 VCC PIN 5
Z8 GND PIN 8 VCC PIN 16
Z1 THRU Z4 & Z7 GND PIN 7 VCC PIN 14
DRAWING NO. 09013732-1
DEVELOPMENT NO.
RELEASED FOR ASSY. 75013732
QTY. —
TITLE SCHEMATIC DIAGRAM - MAWS WRITE ENCODE
SIZE F
DRAWING NO. 09013732-1
SCALE NONE
SHEET 1 OF 1
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA


09013804-2
+HIGH GAIN
-GATE OPEN
+CCW RUN
-CW RUN
+FAST CCW
-FAST CW
-SLACK CAKE
MOTOR CW
SHIELD-CW
+FAST RUN
MOTOR CCW
SHIELD-CCW
+CASSETTE IN PLACE
-SERVO UNSAFE
-SERVO DISABLE
MAIN CLOCK
+NORMAL STOP SAMPLE
7 - CCW TACH
17 - CW TACH
23 - TP
27 - SOLENOID
19 - TP
49 - COLLECTOR-CW
53 - BASE-1-CW
47 - BASE-2-CW
50 - EMITTER-CW
56 - COLLECTOR-CCW
52 - BASE-1-CCW
48 - EMITTER-CCW
55 - BASE-2-CCW
28 - TAPE AT SPEED
35 - CCW SLACK
38 - CW SLACK
12 - TP
8 - TP
NOTES-UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4W.
2. ALL TRANSISTORS ARE 2N4274.
3. ALL DIODES ARE IN4454
4. ALL CAPACITANCE VALUES IN UF, ±20%, 50V.
5. 22,23 GND PIN 7 VCC PIN 14
R10 3.9K
R7 1K
R9 2K
Q7
R14 10K
18K
+5V
+24V
-15V
ANALOG GND
GND
DRAWING NO. 09013804-2
DEVELOPMENT NO.
RELEASED FOR ASSY
75013804
PDD 5587 7-5-73
PDD 5592 7-7-73
SCHEMATIC DIAGRAM - MOTOR CONTROL
DRAWING NO. 09013804-2
SIZE F
SCALE NONE
SHT 1 of 1





DRAWING NO. 07015307-1

DRAWING NO. 07015307-1
DEVELOPMENT NO.
RELEASED FOR ASS'
QTY
76015307 —

MATERIAL
CASE DEPTH
HARDNESS
SURFACE TREATMENT

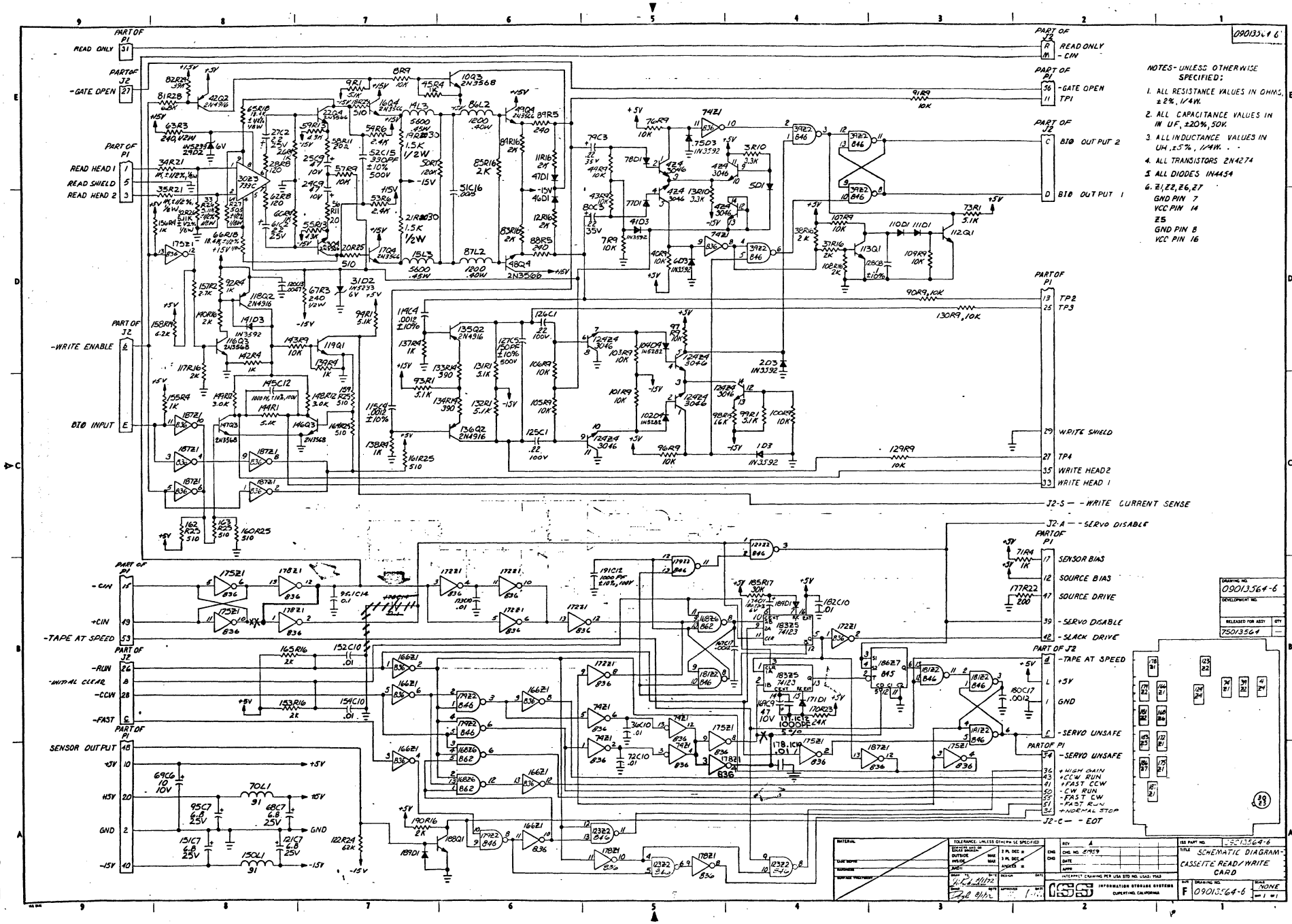
TOLERANCE: UNLESS OTHERWISE SPECIFIED
CORNERS AND/OR EDGES BROKEN: OUTSIDE MAX, INSIDE MAX
RADII
2 PL DEC ±
3 PL DEC ±
ANGLES ±
DRAWN BY 5-4-72 DATE
DESIGN DATE
CHKR DATE
APPROVED DATE

ENG CHG
REV A
CHG. NO. E2035
DATE 7/19/72
APPR

INTERPRET DRAWING PER USA STD NO. USASI Y14.5

INFORMATION STORAGE SYSTEMS
CUPERTINO, CALIFORNIA

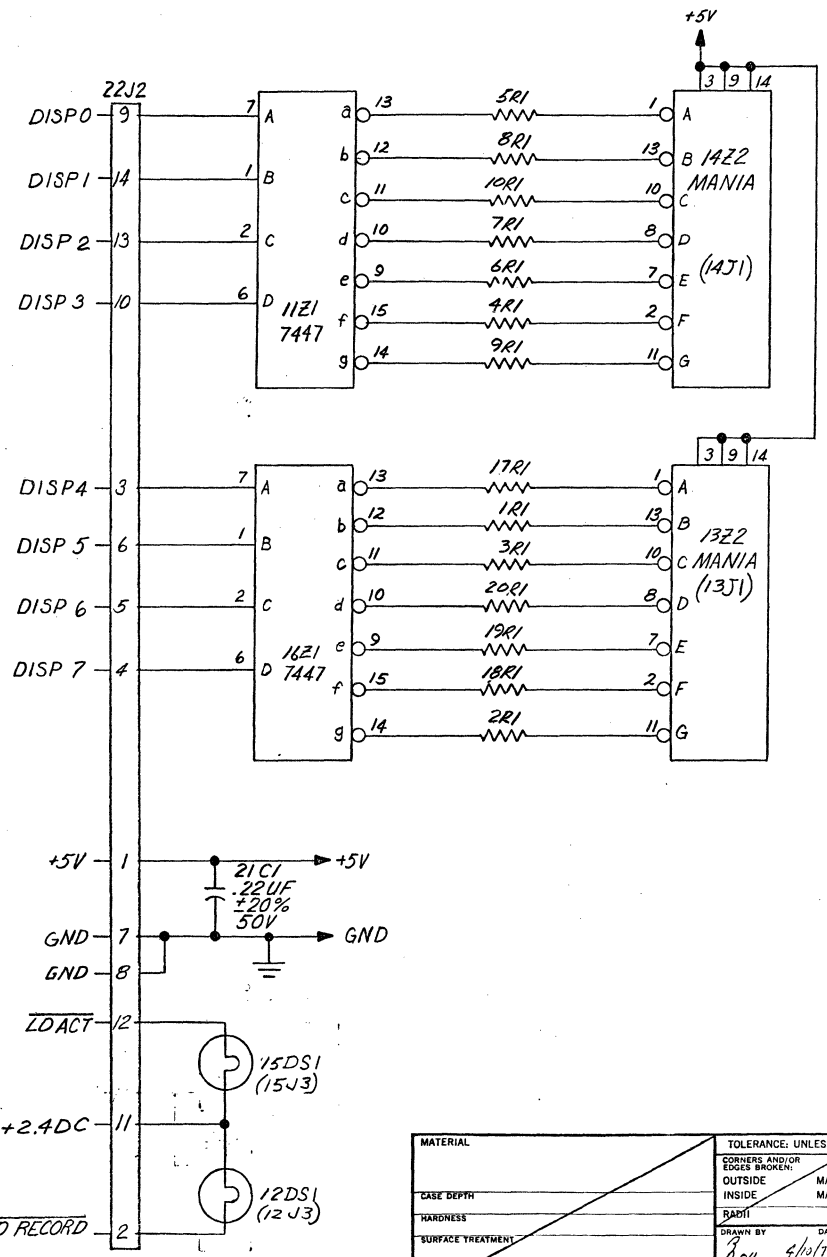
ISS PART NO. 07015307-1
TITLE DIAGRAM— CASSETTE HEAT SINK
SIZE C
DRAWING NO. 07015307-1
SCALE NONE
SHT 1 OF 1


09013564-6
NOTES- UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4W.
2. ALL CAPACITANCE VALUES IN MF UF, ±20%, 50V.
3. ALL INDUCTANCE VALUES IN UH, ±5%, 1/4W. . .
4. ALL TRANSISTORS 2N4274
5. ALL DIODES IN4454
6. 2,12,22,26,27 GND PIN 7 VCC PIN 14
25 GND PIN 8 VCC PIN 16
READ ONLY
-GATE OPEN
READ HEAD 1
READ SHIELD
READ HEAD 2
-WRITE ENABLE
BIO INPUT
-CIN
+CIN
-TAPE AT SPEED
-RUN
-INITIAL CLEAR
-CCW
-FAST
SENSOR OUTPUT
BIO OUTPUT 2
BIO OUTPUT 1
TP2
TP3
WRITE SHIELD
TP4
WRITE HEAD2
WRITE HEAD 1
J2-S — -WRITE CURRENT SENSE
J2-A — -SERVO DISABLE
SENSOR BIAS
SOURCE BIAS
SOURCE DRIVE
-SERVO DISABLE
-SLACK DRIVE
-SERVO UNSAFE
+HIGH GAIN
+CCW RUN
+FAST CCW
-CW. RUN
-FAST CW
-FAST RUN
+NORMAL STOP
J2-C — - EOT
SCHEMATIC DIAGRAM-
CASSETTE READ/WRITE
CARD
DRAWING NO. 09013564-6
DEVELOPMENT NO.
RELEASED FOR ASSY
75013564
INFORMATION STORAGE SYSTEMS
CUPERTINO, CALIFORNIA

DRAWING NO. 09013809-3

NOTES- UNLESS OTHERWISE SPECIFIED:

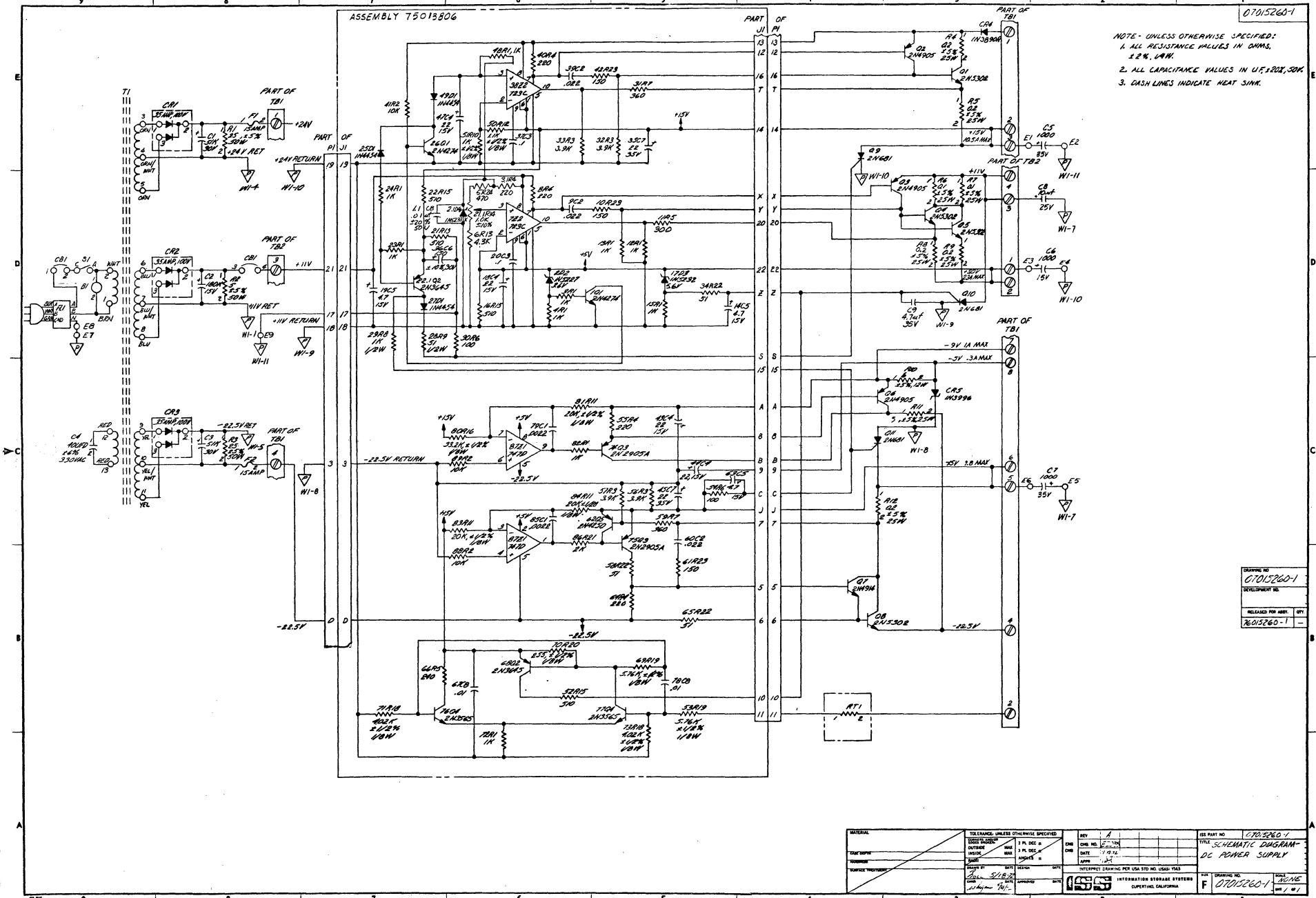
1. ALL RESISTORS ARE 68 OHMS, ±2%, 1/4W.
2. Z1
   GND PIN 8
   VCC PIN 16

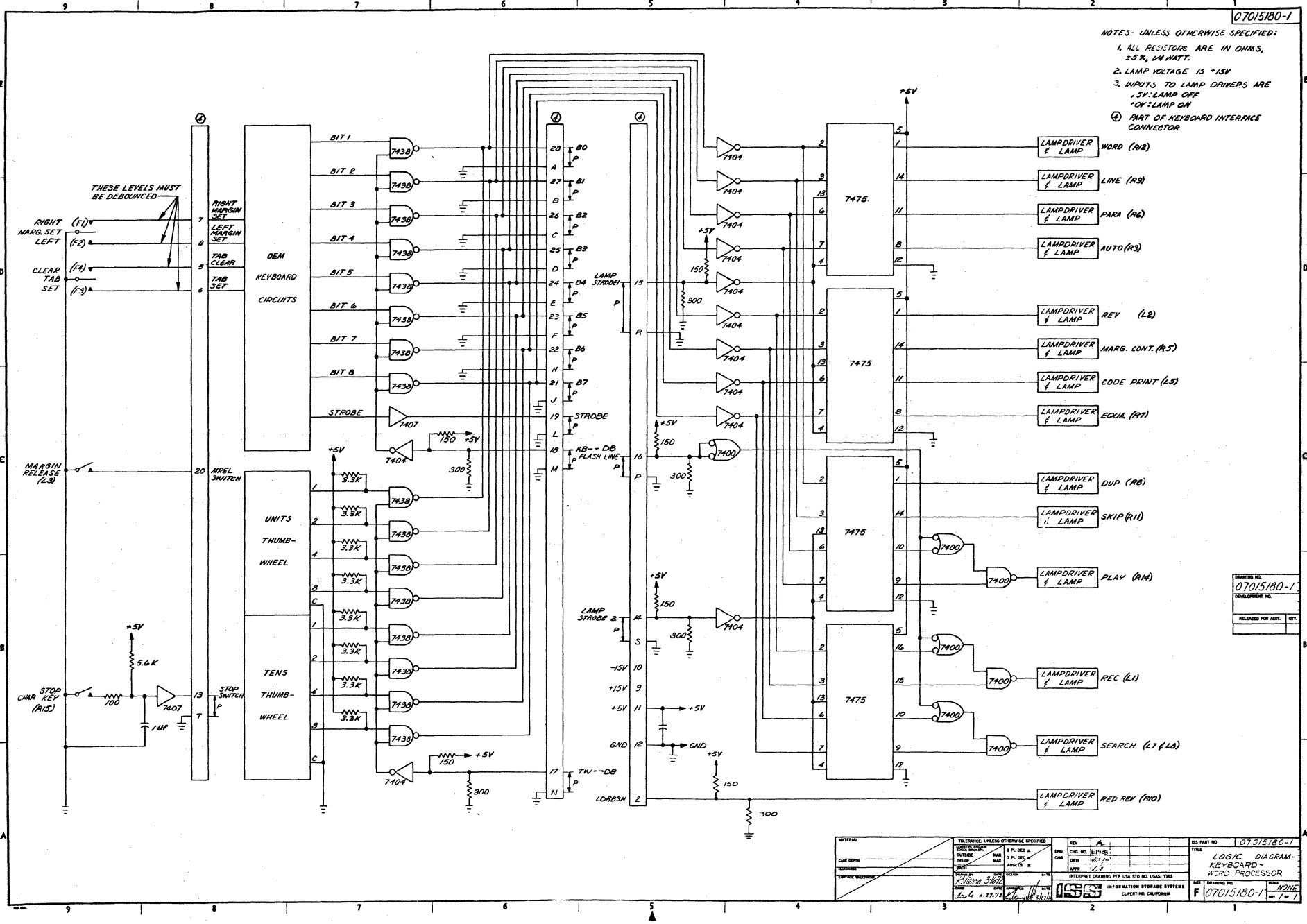


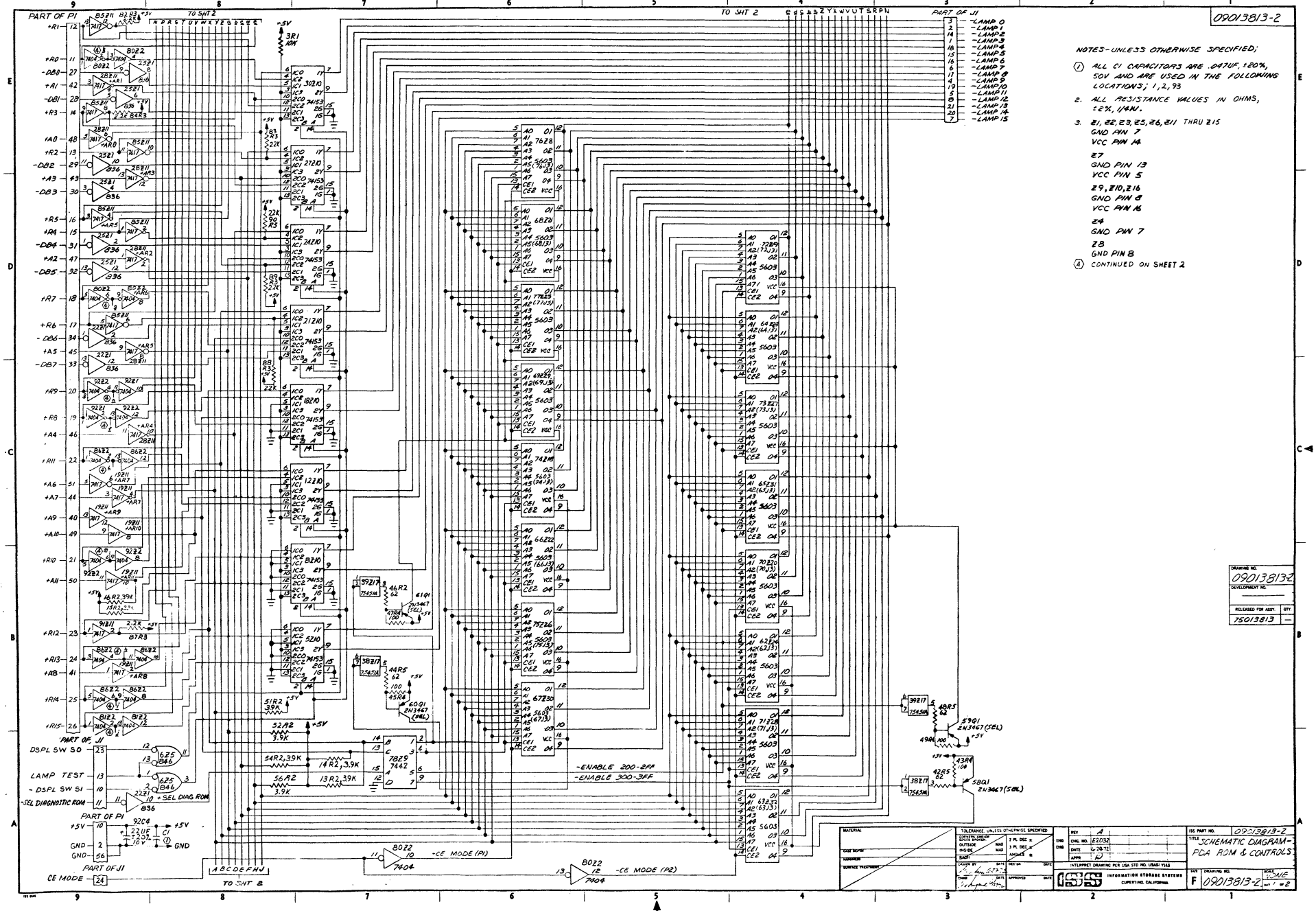
DRAWING NO. 09013809-3
DEVELOPMENT NO.
RELEASED FOR ASSY. | QTY.
75013809

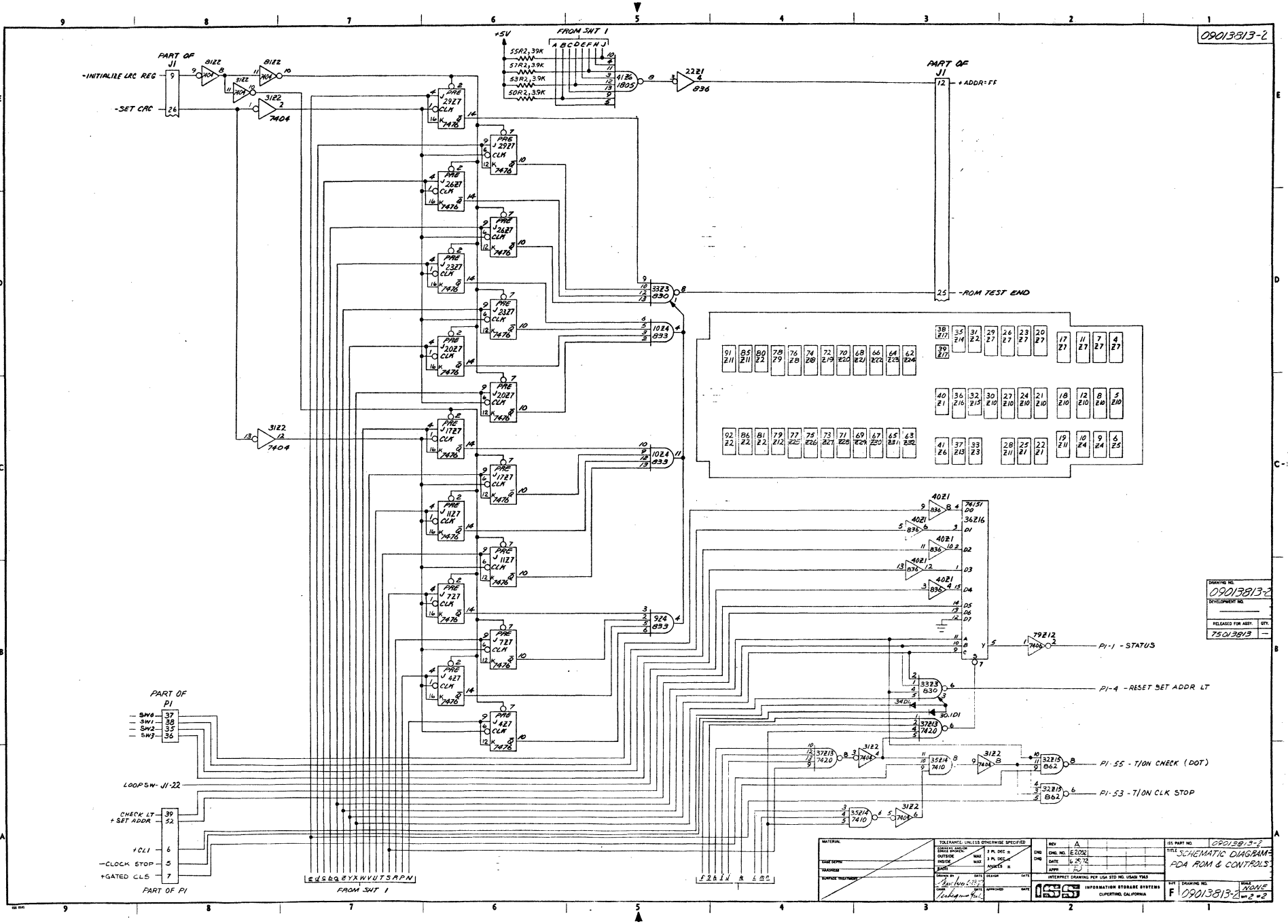
MATERIAL	TOLERANCE: UNLESS OTHERWISE SPECIFIED	REV A	ISS PART NO. 09013809-3
CASE DEPTH	CORNERS AND/OR EDGES BROKEN: OUTSIDE MAX, INSIDE MAX, RADII	2 PL DEC ±	TITLE SCHEMATIC DIAGRAM- DISPLAY PANEL
HARDNESS		3 PL DEC ±	
SURFACE TREATMENT		ANGLES ±	
	DRAWN BY Roll 4/10/72 DATE	DESIGN DATE	ENG CHG. NO. E1939
	CHKR Mac 6/12/72 DATE	IVED DATE	CHG DATE 6/12/72
			APPR KD
	INTERPRET DRAWING PER USA STD NO. USASI Y14.5		
	ISS INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA		SIZE C DRAWING NO. 09013809-3 SCALE NONE SHT 1 OF 1

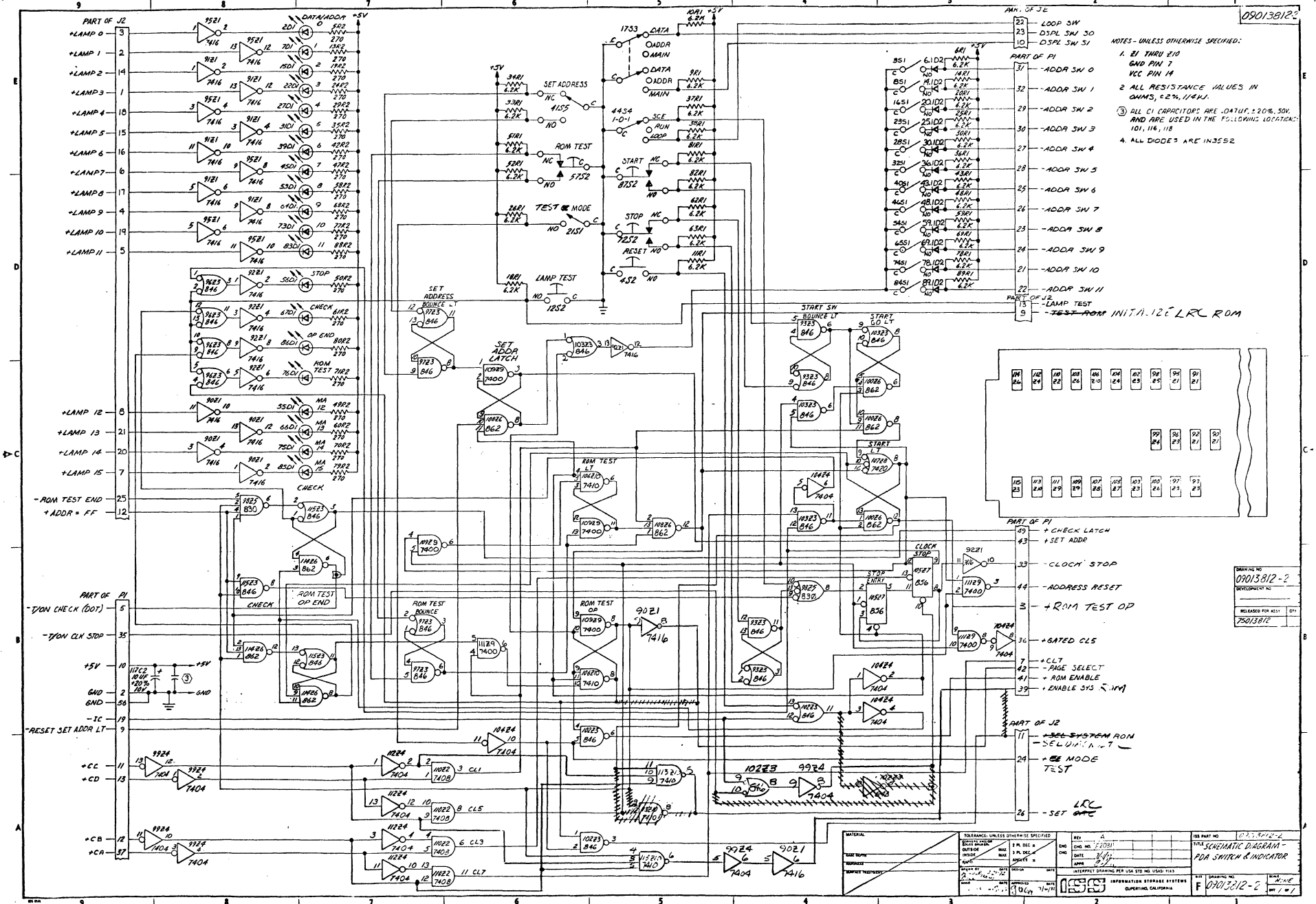
ISS 0139


ASSEMBLY T5013806
07015260-1
NOTE - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4W.
2. ALL CAPACITANCE VALUES IN UF, ±20%, 50V.
3. DASH LINES INDICATE HEAT SINK.
PART OF J1
PART OF P1
PART OF TB1
PART OF TB2
+24V RETURN
+11V RETURN
-22.5V RETURN
-22.5V
-9V 1A MAX
-5V .3A MAX
75V .8 MAX
-12.5V
+24V
+11V
+15V
+5V
DRAWING NO 07015260-1
DEVELOPMENT NO.
RELEASED FOR ASSY. 76015260-1
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA
TITLE SCHEMATIC DIAGRAM-DC POWER SUPPLY
ISS PART NO 07015260-1
SIZE F
DRAWING NO 07015260-1
SCALE NONE


07015180-1
NOTES- UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE IN OHMS, ±5%, ¼ WATT.
2. LAMP VOLTAGE IS +15V
3. INPUTS TO LAMP DRIVERS ARE +5V: LAMP OFF +0V: LAMP ON
④ PART OF KEYBOARD INTERFACE CONNECTOR
THESE LEVELS MUST BE DEBOUNCED
RIGHT MARG. SET (F1)
LEFT (F2)
CLEAR TAB SET (F4)
(F3)
MARGIN RELEASE (L3)
STOP CHAR KEY (A15)
OEM KEYBOARD CIRCUITS
RIGHT MARGIN SET
LEFT MARGIN SET
TAB CLEAR
TAB SET
MREL SWITCH
STOP SWITCH
UNITS THUMB-WHEEL
TENS THUMB-WHEEL
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
STROBE
LAMP STROBE 1
LAMP STROBE 2
KB--DB FLASH LINE
TW--DB
LDRBSH
+5V
-15V
+15V
GND
7438
7407
7404
7400
7475
LAMPDRIVER & LAMP
WORD (A12)
LINE (A9)
PARA (A6)
AUTO (A3)
REV (L2)
MARG. CONT. (A5)
CODE PRINT (L5)
EQUIL (A7)
DUP (A8)
SKIP (A11)
PLAY (A14)
REC (L1)
SEARCH (L7 & L8)
RED REV (A10)
DRAWING NO. 07015180-1
DEVELOPMENT NO.
RELEASED FOR ASSY. QTY.
ISS PART NO 07015180-1
TITLE LOGIC DIAGRAM - KEYBOARD - WORD PROCESSOR
SIZE F DRAWING NO. 07015180-1
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA


09013813-2
NOTES-UNLESS OTHERWISE SPECIFIED;
1. ALL C1 CAPACITORS ARE .047UF, ±20%, 50V AND ARE USED IN THE FOLLOWING LOCATIONS; 1,2,93
2. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4W.
3. Z1, Z2, Z3, Z5, Z6, Z11 THRU Z15
GND PIN 7
VCC PIN 14
Z7
GND PIN 13
VCC PIN 5
Z9, Z10, Z16
GND PIN 8
VCC PIN 16
Z4
GND PIN 7
Z8
GND PIN 8
4 CONTINUED ON SHEET 2
PART OF P1
PART OF J1
TO SHT 2
TO SHT 2
-ENABLE 200-2FF
-ENABLE 300-3FF
-CE MODE (P1)
-CE MODE (P2)
DSPL SW S0
LAMP TEST
-DSPL SW S1
-SEL DIAGNOSTIC ROM
+SEL DIAG ROM
CE MODE
-LAMP 0
-LAMP 1
-LAMP 2
-LAMP 3
-LAMP 4
-LAMP 5
-LAMP 6
-LAMP 7
-LAMP 8
-LAMP 9
-LAMP 10
-LAMP 11
-LAMP 12
-LAMP 13
-LAMP 14
-LAMP 15
DRAWING NO. 09013813-2
DEVELOPMENT NO.
RELEASED FOR ASSY. QTY. 75013813 —
SIS PART NO. 09013813-2
TITLE SCHEMATIC DIAGRAM-PCA ROM & CONTROLS
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA
SIZE F DRAWING NO. 09013813-2 SCALE NONE SHT 1 OF 2


09013813-2
PART OF J1
-INITIALIZE LRC REG
-SET CAC
+5V
FROM SHT 1
+ADDR=FF
-ROM TEST END
PART OF P1
SW0
SW1
SW2
SW3
LOOPSW-J1:22
CHECK LT + SET ADDR
+CLI
-CLOCK STOP
+GATED CLS
PART OF P1
FROM SHT 1
P1-1 - STATUS
P1-4 - RESET SET ADDR LT
P1-55 - T/ON CHECK (DOT)
P1-53 - T/ON CLK STOP
DRAWING NO. 09013813-2
DEVELOPMENT NO.
RELEASED FOR ASSY.
QTY.
7501381B
TITLE SCHEMATIC DIAGRAM PDA ROM & CONTROLS
ISS PART NO. 09013813-2
DRAWING NO. 09013813-2
SIZE F
SHT 2 of 2
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA


PART OF J2
+LAMP 0
+LAMP 1
+LAMP 2
+LAMP 3
+LAMP 4
+LAMP 5
+LAMP 6
+LAMP 7
+LAMP 8
+LAMP 9
+LAMP 10
+LAMP 11
+LAMP 12
+LAMP 13
+LAMP 14
+LAMP 15
-ROM TEST END
+ADDR = FF
PART OF P1
-T/ON CHECK (DOT)
-T/ON CLK STOP
+5V
GND
-IC
-RESET SET ADDR LT
+CC
+CD
+CB
+CA
DATA/ADDR
STOP
CHECK
OP END
ROM TEST
SET ADDRESS
ROM TEST
TEST MODE
LAMP TEST
SET ADDRESS BOUNCE LT
SET ADDR LATCH
ROM TEST LT
ROM TEST BOUNCE
ROM TEST OP
START SW
START BOUNCE LT
START GO LT
START LT
CLOCK STOP
STOP ENTRY
PART OF P1
+CHECK LATCH
+SET ADDR
-CLOCK STOP
-ADDRESS RESET
+ROM TEST OP
+GATED CLS
+CLT
-PAGE SELECT
+ROM ENABLE
+ENABLE SYS ROM
PART OF J2
+SEL SYSTEM ROM
-SEL DIAG CT
+CE MODE TEST
-SET CLR
PART OF J1
-ADDR SW 0
-ADDR SW 1
-ADDR SW 2
-ADDR SW 3
-ADDR SW 4
-ADDR SW 5
-ADDR SW 6
-ADDR SW 7
-ADDR SW 8
-ADDR SW 9
-ADDR SW 10
-ADDR SW 11
PART OF J2
-LAMP TEST
-TEST ROM INIT A-12 LRC ROM
NOTES - UNLESS OTHERWISE SPECIFIED:
1. Z1 THRU Z10 GND PIN 7 VCC PIN 14
2. ALL RESISTANCE VALUES IN OHMS, ±2%, 1/4W.
3. ALL C1 CAPACITORS ARE .047uF, ±20%, 50V. AND ARE USED IN THE FOLLOWING LOCATIONS: 101, 116, 118
4. ALL DIODES ARE IN3552
09013812-2
INFORMATION STORAGE SYSTEMS CUPERTINO, CALIFORNIA
SCHEMATIC DIAGRAM - PDA SWITCH & INDICATOR

R.WL021A CONNECTOR PANEL WIRE LIST PAGE 1
08015311-1 REV A

SOURCE POINT	NET	LINE NAME
A0101	A0101-A0301=A0401-A0501 =A0601-A0701=A0801-A0901 =A1401-A1601=A1701-A1801 =A2001-A2101(A2819	-IC
A0103	A0103-A0203=A0303-A0403 =A0503-A0603=A0703-A0803 =A1003-A1103=A1403-A1603 =A1703-A1803=A1903-A2003 =A2103-A2837	+CA
A0104	A0104-A0304=A0404-A0504 =A0604-A0704=A0804-A0904 =A1004-A1404=A1604-A1730 =A1904-A2030(A2812	+CB
A0105	A0105-A0305=A0405-A0505 =A0605-A0705=A0805-A1405 =A1605-A1732=A1805-A2032 =A2105-A2811	+CC
A0111	A0111-A0211=A0311-A1111 =A1211-A1311=A1511-A1711 =A1811-A1911=A2011-A2111 (A2727	-AADB0
A0112	A0112-A0212=A0312-A1112 =A1212-A1312=A1512-A1712 =A1812-A1912=A2012-A2112 (A2728	-AADB1
A0113	A0113-A0213=A0313-A1113 =A1213-A1313=A1513-A1713 =A1813-A1913=A2013-A2113 (A2729	-AADB2
A0114	A0114-A0214=A0314-A1114 =A1214-A1314=A1514-A1714 =A1814-A1914=A2014-A2114 (A2730	-AADB3
A0115	A0115-A0215=A0315-A0415 =A1115-A1215=A1315-A1515 =A1715-A1815=A1915-A2015 =A2115-A2731	-AADB4
A0116	A0116-A0216=A0316-A1116 =A1216-A1316=A1516-A1716 =A1816-A1916=A2016-A2116 (A2732	-AADB5
A0117	A0117-A0217=A0317-A1117 =A1217-A1317=A1517-A1717 =A1817-A1917=A2017-A2117 (A2734	-AADB6

SOURCE POINT	NET	LINE NAME
A0118	A0118-A0218=A0318-A1118 =A1218-A1318=A1518-A1718 =A1818-A1918=A2018-A2118 (A2733	-AADB7
A0119	A0119-A0219=A0319-A1119 =A1319-A1519=A1719-A2019	-DBXM
A0121	A0121-A0321=A1722-A2022	-B0
A0123	A0123-A0223=A0323-A1223 =A1423-A1623=A1723-A2023	-B1
A0124	A0124-A0324=A0924-A1724 (A2024	+B2
A0125	A0125-A0225=A0325-A1125 =A1225-A1425=A1625-A1725 (A2025	-B2
A0126	A0126-A0326=A0926-A1226 =A1426-A1626	+B3
A0128	A0128-A0328=A0928-A1428 (A1628	+B4
A0130	A0130-A0330=A0930-A1430 (A1630	+B5
A0131	A0131-A0231=A0331-A0431 =A1131-A1431=A1631-A1731 =A1931-A2031	-B5
A0132	A0132-A0332=A0932-A1432 (A1632	+B6
A0133	A0133-A0233=A0333-A1133 =A1433-A1633=A1733-A1833 =A2033-A2133	-B6
A0134	A0134-A0234=A0334-A0934 =A1734-A2034	+B7
A0135	A0135-A0335=A1135-A1435 =A1635-A1735(A2035	-B7
A0136	A0136-A0236=A0336-A0436 =A0936-A1136=A1236-A1419 =A1736-A1744=A2036-A2044 (A2052	+B8
A0137	A0137-A0437=A1619-A1752	-B8

SOURCE POINT	NET	LINE NAME
A0138	A0138-A0238=A0338-A0438 =A0938-A1138=A1238-A1641 =A1738-A1748=A1753-A2038 (A2048	+B9
A0139	A0139-A0439=A1441-A2053	-B9
A0141	A0141-A0441=A1041-A1141 =A1741-A2041	-B10
A0143	A0143-A0243=A0343-A0443 =A1043-A1243=A1443-A1643 =A1743-A2043	-B11
A0144	A0144-A0444=A1444-A1644	+B12
A0147	A0147-A0447=A0947-A1247	-B13
A0149	A0149-A0449=A1049-A1149 =A1449-A1649=A1749-A2049	-B14
A0151	A0151-A0451=A1251-A1451 =A1651-A1751(A2051	-B15
A0153	A0153-A0309	+TENP
A0154	A0154-A0254=A0354-A0454 =A0545-A0645=A0745-A0845 =A1354-A1554=A1754-A2054 (A2701	-STATUS
A0206	A0206-A0406=A0506-A0606 =A0706-A0806=A1006-A1106 =A1406-A1606=A1706-A1806 =A2006-A2106(A2813	+CD
A0220	A0220-A0320=A0920-A1220 =A1320-A1520	+B0
A0226	A0226-A0307=A0413-A0949	+SPADDER
A0227	A0227-A0327=A1227-A1727 (A2027	-B3
A0229	A0229-A0329=A0429-A1129 =A1429-A1629=A1729-A2029	-B4
A0308	A0308-A0425=A1728-A1901 (A2028	+OSC
A0322	A0322-A0922=A1222-A1422 (A1622	+B1

SOURCE POINT	NET	LINE NAME
A0340	A0340-A0440=A0940-A1040 =A1240-A1740(A2040	+B10
A0342	A0342-A0423(A2841	+ROMEN
A0345	A0345-A0532=A0632-A0732 =A0832-A2717	+R6
A0346	A0346-A0534=A0634-A0734 =A0834-A2718	+R7
A0347	A0347-A0408	-SW CMND
A0348	A0348-A0417	-BUZZ CMND
A0349	A0349-A0522=A0622-A0722 =A0822-A2712	+R1
A0350	A0350-A0526=A0626-A0726 =A0826-A2714	+R3
A0351	A0351-A0524=A0624-A0724 =A0824-A2713	+R2
A0352	A0352-A0435(A1654	+FLASH
A0353	A0353-A0520=A0620-A0720 =A0820-A2711	+R0
A0355	A0355-A0528=A0628-A0728 =A0828-A2715	+R4
A0356	A0356-A0530=A0630-A0730 =A0830-A2716	+R5
A0407	A0407-A1407(A1607	+CL
A0411	A0411-A1051	+ST
A0412	A0412-A1052	-ST
A0414	A0414-A0538=A0638-A0738 =A0838-A2720	+R9
A0416	A0416-A0536=A0636-A0736 =A0836-A2719	+R8
A0421	A0421-A1726(A2026	-RECORD
A0422	A0422-A2047	-CINRO

SOURCE POINT	NET	LINE NAME
A0424	A0424-A1747	-CINRW
A0427	A0427-A0540=A0640-A0740 =A0840-A2721	+R10
A0428	A0428-A0542=A0642-A0742 =A0842-A2722	+R11
A0430	A0430-A0546=A0646-A0746 =A0846-A2724	+R13
A0432	A0432-A0544=A0644-A0744 =A0844-A2723	+R12
A0433	A0433-A0550=A0650-AC750 =A0850-A2726	+R15
A0434	A0434-A0548=A0648-A0748 =A0848-A2725	+R14
A0442	A0442-A0942=A1142-A1242	+B11
A0445	A0445-A0945=A1245-A1745 (A2045	-B12
A0446	A0446-A1246=A1446-A1646 =A1746-A2046	+B13
A0448	A0448-A1148	+B14
A0450	A0450-A0950(A1050	+B15
A0452	A0452-A1707	$\overline{\text{RW ACTIVE RD}}$
A0455	A0455- A2007	$\overline{\text{RO ACTIVE RD}}$
A0507	A0507-A0607=A0707-A0807 =A0956-A1001(A2831	-AB0
A0508	A0508-A0608=A0708-A0808 =A0955-A1005(A2832	-AB1
A0509	A0509-A0609=A0709-A0809 =A0954-A1038(A2829	-AB2
A0511	A0511-A0611=A0711-A0811 =A0953-A1019(A2830	-AB3
A0512	A0512-A0612=A0712-AC812 =A0914-A1007(A2827	-AB4
A0513	A0513-A0613=A0713-A0813 =A0916-A1009(A2828	-AB5

SOURCE POINT	NET	LINE NAME
A0514	A0514-A0614=A0714-A0814 =A0912-A1017(A2825	-AB6
A0515	A0515-A0615=A0715-A0815 =A0908-A1022(A2826	-AB7
A0516	A0516-A0616=A0716-A0816 =A0948-A1011(A2823	-AB8
A0517	A0517-A0617=A0717-AC817 =A0937-A1012(A2824	-AB9
A0518	A0518-A0618=A0718-A0818 =A0946-A1021(A2821	-AB10
A0519	A0519-A0619=A0719-AC819 =A0929-A1024(A2822	-AB11
A0521	A0521-A0621=A0721-A0821 =A0944-A1015(A2748	+A0
A0523	A0523-A0623=A0723-A0823 =A0941-A1016(A2742	+A1
A0525	A0525-A0625=A0725-AC825 =A0939-A1018(A2747	+A2
A0527	A0527-A0627=A0727-A0827 =A0952-A1013(A2743	+A3
A0529	A0529-A0629=A0729-A0829 =A0913-A1029(A2746	+A4
A0531	A0531-A0631=A0731-A0831 =A0911-A1027(A2745	+A5
A0533	AC533-A0633=A0733-A0833 =A0907-A1031(A2751	+A6
A0535	A0535-A0635=A0735-A0835 =A0906-A1025(A2744	+A7
A0537	A0537-A0637=A0737-A0837 =A0923-A1046(A2741	+A8
A0539	A0539-A0639=A0739-A0839 =A0927-A1045(A2740	+A9
A0541	A0541-A0741=A0921-A1047 (A2749	+A10
A0543	A0543-A0643(A0925	-A11

SOURCE POINT	NET	LINE NAME
A0547	A0547-A0647=A0747-A0847 =A1034- A2705 (A2833	-STOP
A0549	A0549-A0649=A0749-A0849 (A2839	+ENSYSROM
A0554	A0554-A0754	-15V
A0641	A0641-A0841 (A0915	-A10
A0654	A0654-A0854	-15V
A0743	A0743-A0843=A0919-A1044 (A2750	+A11
A0903	A0903-A1033	+LACL
A0905	A0905-A2844	-ARESET
A0909	A0909-A1053	-ICA
A0917	A0917-A1055	+STOP
A0918	A0918-A1008	-RET
A0931	A0931-A1248	-BRANCH
A0933	A0933-A1035	-JUMP
A0935	A0935-A1054	+ABE
A0943	A0943-A1048	-JEP
A0951	A0951-A2842	-PAGESEL
A1101	A1101-A1239	+OP.B3
A1104	A1104-A1232	+JMP.B11
A1105	A1105-A1221	-ALF2
A1107	A1107-A1204	-ALB3
A1108	A1108-A1228	-ALF3
A1109	A1109-A1209	-ALB0
A1122	A1122-A1241	-OP
A1124	A1124-A1206	-ALB1
A1126	A1126-A1208	-ALF0
A1127	A1127-A1205	-ALB2
A1137	A1137-A1229	-ALB6

SOURCE POINT	NET	LINE NAME
A1143	A1143-A1203	-ALB7
A1145	A1145-A1201	-ALB5
A1146	A1146-A1207	-ALF1
A1147	A1147-A1224	-ALB4
A1151	A1151-A1233	-ALF5
A1152	A1152-A1231	-ALF4
A1153	A1153-A1235	-ALF6
A1154	A1154-A1252	+JMP.B11*
A1155	A1155-A1219	-ALF7
A1156	A1156-A1253	+OP.B3*
A1304	A1304-A1416	-TODRO
A1305	A1305-A1413	-TORO
A1306	A1306-A1415	-CCRO
A1309	A1309-A1509	-15V
A1321	A1321-A1421	+B11*.ADDRRO
A1324	A1524-A1624 A1324-A1424	+ZEROXBRW
A1325	A1325-A1418	-HOLDRO
A1327	A1327-A1427	-CBRO
A1337	A1337-A1437	+STATUSRO
A1340	A1340-A1440	-DBXBRO
A1343	A1343-A1412	+XPCLRO
A1345	A1345-A1417	+P2CLRO
A1347	A1347-A1434	+BCCRO
A1350	A1350-A1408	+P1CLRO
A1352	A1352-A1452	-B=0RO
A1355	A1355-A1414	+PH1RO
A1504	A1504-A1616	-TODRW

SOURCE POINT	NET	LINE NAME
A1505	A1505-A1613	-TORW
A1506	A1506-A1615	-CCRW
A1521	A1521-A1621	+B11*.ADDRRW
A1525	A1525-A1618	-HOLDRW
A1527	A1527-A1627	-CBRW
A1537	A1537-A1637	+STATUSRW
A1540	A1540-A1640	-DBXBRW
A1543	A1543-A1612	+XPCLRW
A1545	A1545-A1617	+P2CLRW
A1547	A1547-A1634	+BCCRW
A1550	A1550-A1608	+P1CLRW
A1552	A1552-A1652	-B=0RW
A1555	A1555-A1614	+PH1RW
A1704	A1704-A1831	+FWDRW
A1709	A1709-A1909	-BIO RECRW
A1720	A1720-A1825(A1952	-CMND STRRW
A1721	A1721-A1809	-RR=DBRW
A1750	A1750-A1821	-BIO READRW
A1755	A1755-A1819	+RDRRW
A1756	A1756-A1905	-WDRRW
A1835	A1835-A1907	-SETUP+ICRW
A2004	A2004-A2131	+FWDRO
A2020	A2020-A2125	-CMND STRRO
A2021	A2021-A2109	-RR=DBRO
A2050	A2050-A2121	-BIO READRO
A2055	A2055-A2119	+RDRRO

SOURCE POINT	NET	LINE NAME
A2704	A2704-A2809	-RESET SET ADDR LT
A2739	A2739-A2849	+CHECK LATCH
A2753	A2753-A2835	-T/ON CLK STOP (DOT)
A2755	A2755-A2805	-T/ON CHECK (DOT)
A2807	A2807-A2706	+CLI
A2836	A2836-A2707	+GATED CLOCK 7
A2843	A2843-A2752	+SET ADDR