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Computer Products

**The
Memory
Bank**

**The
Memory Bank[®]
by
JADE Computer Products**

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SECTION ONE INTRODUCTION

1.0 THE MEMORY BANK - GENERAL DESCRIPTION

The MEMORY BANK is a 64K dynamic RAM memory board utilizing state of the art design principles and incorporating features not normally found in similar memory products.

1.0.1 The MEMORY BANK can be used as a standard 8-bit wide memory board, or as a 16-bit by 32K memory board, either by a parallel transfer of 16 bits through a bidirectional ganged data bus, or by a sequential transfer of a high byte and a low byte. In this, it follows the conventions established by IEEE Standard 696, The S-100 Bus Interface.

1.0.2 The MEMORY BANK may be selected by port addressing per Northstar/Cromemco/Alpha Micro/SD Systems convention, or by using the full 24-bit extended address bus proposed by the IEEE standard.

1.0.3 The MEMORY BANK is known to be compatible with the following CPU products:

- *SBC-100 (SD Systems)

- *SBC-200 (SD Systems)

- *JADE "Big Z" CPU (Jade Computer Products)

- *IA Z80 (Ithaca Intersystems)

- *CB2 (SSM)

- *Cromemco ZPU

- *TDL ZPU

- *Northstar ZPB-A

1.0.4 Although the MEMORY BANK was designed specifically for use with Z80 and Z8000-type systems, it will operate successfully with other CPU types that meet the timing specifications of the S-100 bus and are capable of providing a memory-request signal similar to that of the Z80.

1.0.5 Its timing is designed such that it may be used up to 6 MHz with proper RAM chip selections and without board modification.

1.0.6 The MEMORY BANK also provides an on-board M1 wait state generator and a unique RAM precharge extender which functions without adding wait states to the memory cycle, yet allows slower RAM chips to be used with 4 MHz and 6 MHz CPU chips.

1.0.7 The MEMORY BANK performs its refresh cycles transparently to all CPUs and is capable of being used with DMA devices and disk controllers which utilize extended wait states.

1.0.8 Any 16K bank can be disabled by switch selection. In addition, special circuitry exists on the board that can deselect the top 4K or 8K of memory space, allowing its use with CPU types that have on-board EPROM monitor programs or boot programs without provision for disabling RAM memory when it is in conflict with the EPROM location.

1.0.9 The MEMORY BANK also responds to the PHANTOM* signal, disabling any reads from the board when that signal is asserted.

1.0.10 An LED indicator lights when the board is selected, to aid in memory diagnostics and in troubleshooting multi-user systems.

1.0.11 The MEMORY BANK is the product of a thorough research of existing competitive memory boards and long experience with S-100 systems and their users, from sales to extensive technical support and service. We believe that we have successfully implemented the concepts and features required by dynamic memory users. The MEMORY BANK is an extremely flexible yet extremely stable and reliable memory product with many features and ideas that distinguish it from other memory products.

1.1 SPECIFICATIONS

1.1.1	Memory Capacity	65,536 bytes organized as 64K x 8 or 32K x 16
1.1.2	Memory Access	375 ns maximum; minimum dependent only on the speed of the processor used and the speed of the RAM chips
1.1.3	Memory Cycle	Dependent on CPU and RAM speed
1.1.4	Interface Levels	TTL compatible, conforms to IEEE 696 specification for S-100 bus interface
1.1.5	Power Requirements (1.5 usec memory cycle)	+7 to +10V @ 600 mA (maximum) +14 to +20V @ 200 mA (maximum) -14 to -20V @ 30 mA (maximum)
1.1.6	Physical Dimensions	5.25" x 10.00" x 0.62"
1.1.7	Operating Temperature	0° C to 50° C

1.2 PINOUT FOR S-100 BUS INTERFACE

Pin No.	Signal Name & Direction	(B)=bus (M)=master (CPU) (S)=slave (memory)
1	+8V to +10V	Instantaneous minimum must be greater than +7V, instantaneous maximum less than +25V, and average maximum less than +11V.
2	+14V to +20V	Instantaneous minimum must be greater than 14.5V, instantaneous maximum less than 35V, and average maximum less than 21.5V.
15	A18 (M)	Extended address bit 18.
16	A16 (M)	Extended address bit 16.
17	A17 (M)	Extended address bit 17.

20	Ground (B)	
24	O2 (B)	Master clock signal.
25	pSTVAL* (M)	Status valid strobe.
26	pHLDA (M)	Hold Acknowledge (DMA Grant) signal.
27	pWAIT (M/S)	Wait.
29	A5 (M)	Address bit 5.
30	A4 (M)	Address bit 4.
31	A3 (M)	Address bit 3.
32	A15 (M)	Address bit 15.
33	A12 (M)	Address bit 12.
34	A9 (M)	Address bit 9.
35	DO1 (M) / DATA1 (M/S)	Data out bit 1, bidirectional data bit 1.
36	DO0 (M) / DATA0 (M/S)	Data out bit 0, bidirectional data bit 0.
37	A10 (M)	Address bit 10.
38	DO4 (M) / DATA4 (M/S)	Data out bit 4, bidirectional data bit 4.
39	DO5 (M) / DATA5 (M/S)	Data out bit 5, bidirectional data bit 5.
40	DO6 (M) / DATA6 (M/S)	Data out bit 6, bidirectional data bit 6.
41	DI2 (S) / DATA10 (M/S)	Data out bit 2, bidirectional data bit 10.
42	DI3 (S) / DATA11 (M/S)	Data out bit 3, bidirectional data bit 11.
43	DI7 (S) / DATA15 (M/S)	Data out bit 7, bidirectional data bit 15.
44	sM1 (M)	Status signal indicating op code fetch.
45	sOUT (M)	Status signal indicating write to output device.
47	sMEMR (M)	Status signal indicating memory read which is not interrupt acknowledge instruction fetch cycle.
48	sHLTA (M)	Status signal acknowledging a HALT instruction executing.
50	GROUND (B)	
51	+8V (B)	(See pin 1)
52	-16V (B)	Instantaneous maximum less than -14.5V, instantaneous minimum greater than -35V, average minimum greater greater than -21.5V.
53	GROUND (B)	
54	SLAVE CLR* (B)	Reset signal to reset bus slaves. Must be active with POC*.
58	sXTRQ* (M)	Status signal requesting 16-bit slaves to assert SIXTN*.
59	A19 (M)	Extended address bit 19.
60	SIXTN* (S)	Sixteen acknowledge generated by slave in response to sXTRQ*.
61	A20 (M)	Extended address bit 20.
62	A21 (M)	Extended address bit 21.
63	A22 (M)	Extended address bit 22.
64	A23 (M)	Extended address bit 23.
65	MRQ (M)	Z80 Memory Request signal.
66	REFRESH (M)	Z80 Refresh signal.
67	PHANTOM* (M/S)	Disables read from memory.

68	MWRT (B)	Memory Write status signal.
70	GROUND (B)	
72	RDY (S)	Used in conjunction with wait. Low indicates not ready.
75	RESET*	
77	pWR* (M)	Control signal, signifies valid data on DO or data bus.
78	pDBIN (M)	Control signal requesting data on the DI or data bus from slave.
79	A0 (M)	Address bit 0.
80	A1 (M)	Address bit 1.
81	A2 (M)	Address bit 2.
82	A6 (M)	Address bit 6.
83	A7 (M)	Address bit 7.
84	A8 (M)	Address bit 8.
85	A13 (M)	Address bit 13.
86	A14 (M)	Address bit 14.
87	A11 (M)	Address bit 11.
88	DO2 (M) / DATA2 (M/S)	Data out bit 2, bidirectional data bit 2.
89	DO3 (M) / DATA3 (M/S)	Data out bit 3, bidirectional data bit 3.
90	DO7 (M) / DATA7 (M/S)	Data out bit 7, bidirectional data bit 7.
91	DI4 (S) / DATA12 (M/S)	Data in bit 4, bidirectional data bit 12.
92	DI5 (S) / DATA13 (M/S)	Data in bit 5, bidirectional data bit 13.
93	DI6 (S) / DATA14 (M/S)	Data in bit 6, bidirectional data bit 14.
94	DI1 (S) / DATA9 (M/S)	Data in bit 1, bidirectional data bit 9.
95	DI0 (S) / DATA8 (M/S)	Data in bit 0, bidirectional data bit 8.
96	sINTA (M)	Status signal identifying an interrupt acknowledge.
97	sWO* (M)	Status signal identifying transfer of data from master to slave.
99	POC* (B)	Power-on clear. Active low, must remain low minimum of 10 msec.
100	GROUND (B)	System ground (also common with 20, 50, 53 and 70).

1.2.1 A pin number preceded by an asterisk indicates that the pin is not specified by the IEEE standard.

1.2.2 MRQ* on pin 65 is the MRQ* signal from the Z80 CPU bus master, delayed by not more than 30 nanoseconds from that on pin 19 of the CPU. MRQ* may be inverted in phase from Z80 pin 19, since provision exists on the MEMORY BANK to re-invert it. Most Z80 CPU boards provide this signal.

1.2.3 Pin 27 (pWAIT) is not specified by IEEE; however, it is used by many wait-state based disk controllers and is therefore supported on the MEMORY BANK.

1.2.4 Pin 66 (REFRESH*) is the Z80 RFSH* signal. It must be in-phase with the Z80 RFSH* signal. This signal is not specified by IEEE, but most Z80 CPU boards provide it.

SECTION TWO THEORY OF OPERATION

2.0 INTRODUCTION

Since the advent of third-generation microprocessors, such as the Zilog Z80, there has been an increase in memory requirement for microcomputer systems. In part, this need for larger memory space is due to the availability of higher level languages such as FORTRAN, COBOL, BASIC, PASCAL and others. Additionally, with the introduction of Digital Research MP/M and other multi-user multi-tasking operating systems, the requirement for additional memory has become mandatory.

2.0.1 JADE has chosen to base its new memory product, the MEMORY BANK, on the 16-pin dynamic RAM. Dynamic memory, as opposed to static, has had a long history of use in minicomputers and large mainframe computers. Designers of memory systems for these larger computers have chosen dynamic memory for its reliability, low power consumption, cost effectiveness, performance, and its ability to achieve a high memory density in relatively little board real estate.

2.0.2 Earlier microcomputers, such as the 8080 and 6800, were relatively difficult to interface with dynamic memory, since they did not provide proper interface signals. The Z80 a true third-generation microprocessor, eliminates the interfacing problems and provides signals which allow reliable operation of dynamic memory.

2.1 OPERATION OF 16-PIN DYNAMIC MEMORIES -- ADDRESSING

The 16-pin memory concept was pioneered by Mostek. It uses an address multiplexing technique which allows memories as large as 256K (262,144 bits) to be packaged in a 16-pin package. The MEMORY BANK I is designed around the 4116-type dynamic RAM, a 16K variety.

2.1.1 A 4116 requires 14 bits to select 1 out of 16,384 possible locations. The memory is arranged in a 7 x 7 matrix, or 128 unique rows and 128 unique columns. To access any particular location, a row and column address is issued to the memory chip. Address bits A0 through A6 provide the row address, and address bits A7 through A14 provide the column address.

2.1.2 The row address is strobed into the memory chip by a negative-going clock called the Row Address Strobe (RAS*). Shortly after RAS* goes active, the row address is latched into the memory.

2.1.3 The column address is strobed into the memory chip by a negative-going clock called the Column Address Strobe (CAS*). As with the row address, the column address is also latched into the memory.

2.1.4 Timing of the RAS* and CAS* clocks can be governed by either of two methods. In the first instance, the delay time from RAS* to CAS* is set between the maximum and minimum

values of the specified limits of the particular RAM chip being used. The affect of this setting is that the internal CAS* control signal is inhibited until nearly the maximum delay specified between RAS* and CAS*. In this instance, the external CAS* signal can be applied at any time less than the delay specified as the maximum between RAS* and CAS* without affecting access time. The access time will then be governed by the specified access time referenced to RAS*.

2.1.5 If, however, the delay time between RAS* and CAS* is set greater than the specified maximum value of the limits, the chip's internal CAS* control signals are governed by the external CAS* clock. In this instance, the access time of the memory will be governed by the specified access time referenced to CAS*.

2.1.6 The MEMORY BANK uses the first of these alternatives.

2.2 OPERATION OF 16-PIN DYNAMIC MEMORIES -- DATA INPUT (WRITE CYCLE)

Data which is to be written into an addressed location is supplied to the data input pin (pin 2). Data is strobed into the RAM chip by either WRITE* (pin 3) or by CAS* clock, whichever occurs later. If the WRITE* input is low prior to CAS* going low, then data is strobed into the chip by the CAS* clock. This is referred to as an Early Write Cycle, and the negative-going edge of CAS* provides the reference point for set-up and hold times.

2.2.1 If, however, the CAS* clock goes negative prior to the WRITE* signal going negative, the WRITE* signal serves as the data input strobe and its negative transition provides the reference point for set-up and hold times.

2.3 OPERATION OF 16-PIN DYNAMIC MEMORIES -- DATA OUTPUT (READ CYCLE)

The output of the 4116 is tri-stated or in a high-impedance state at all times when CAS* is high. If the memory cycle in progress is a read, which is signified by WRITE* remaining high throughout the cycle, the data output will go from a high-impedance state to its active condition and the data in the cell addressed by the row and column latches will be read. The polarity of the data output is the same as the input data.

2.3.1 Once the data output has entered its active condition, this condition will be maintained until the CAS* clock goes high. This statement will hold true irregardless of the conditon of RAS* (up to a maximum of about 10 microseconds).

2.4 OPERATION OF 16-PIN MEMORIES -- REFRESH CYCLES

Dynamic memories store their data by placing a charge on a small capacitor, usually on the order of something around 1 picofarad. If the memory is to retain valid data, this charge must be periodically restored before internal leakage has an opportunity to deplete the charge. For a 16K dynamic RAM, the "safe" period is around 2 milliseconds.

2.4.1 The charge is restored on all bits in a given row anytime that row is accessed for a read or write cycle on any given bit within the row. However, this does not guarantee that other

rows in the memory will be accessed at frequent enough intervals to ensure that the charge on the capacitors in these rows will be replenished. Therefore, dynamic memories require that all rows be accessed within 2 milliseconds to retain valid data. Since there are 128 rows, each row must be accessed sequentially in cycles that occur at a minimum of 16 ~~milli~~^{micro}seconds (2 milliseconds divided by 128 rows), with a counter that provides sequential row addresses incremented after each access cycle.

2.4.2 This process is called "refresh." Designers of dynamic memory chips have achieved a significant power conservation by requiring that the refresh cycle shall require only the RAS* clock. It should be noted that most of the power dissipation in a dynamic memory chip occurs when the addresses are strobed by RAS* and CAS*.

2.4.3 During a refresh cycle, *all* RAM chips in the memory array are loaded with the refresh row address and this address is strobed into all RAMs by generating a refresh RAS* clock cycle. This is referred to as a RAS*-only refresh cycle. Since CAS* is inhibited during the refresh cycle, the data output pins remain in their high-impedance state, thus eliminating any possible conflict between the outputs of the RAM chips in the memory array.

2.5 RAM SPECIFICATIONS

There are four specifications of a dynamic memory chip that will be of direct interest to us here:

- (1) The maximum delay time between RAS* and CAS* ($t_d(\text{RAS}^*-\text{CAS}^*)$).
- (2) The minimum delay time between RAS* and CAS* as above.
- (3) The maximum RAS* access time ($t_a(\text{RAS}^*)$).
- (4) The minimum RAS* high pulse width (t_{rp}), which is known as the RAS Precharge Time and will be discussed later.

2.5.1 The first and second parameters will govern the choice of delay line, since we want to choose a delay line that will give us a delay from RAS* to CAS* which is equal to or greater than the minimum but less than the maximum specified.

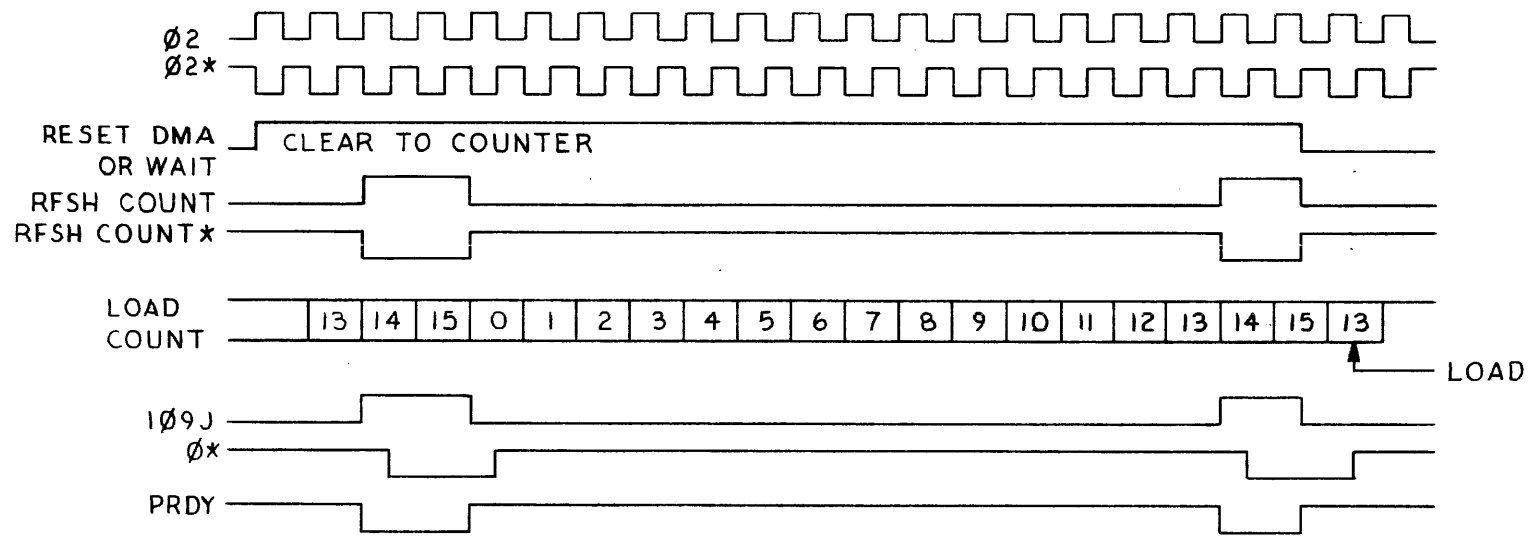
2.5.2 The third parameter will determine the read access timing response of the MEMORY BANK.

2.5.3 The fourth parameter will determine whether we will or will not be required to use the Precharge Extender Option Circuit discussed later in this section.

2.5.4 Having reviewed the pertinent principles of operation of dynamic memories, we are now ready to proceed to a discussion of the theory of operation of the MEMORY BANK where these principles are utilized.

2.6 THE MEMORY BANK -- REFRESH OPERATIONS

Memory refresh on the MEMORY BANK is, *under ordinary circumstances*, generated by the Z80 RFSH* signal applied *non-inverted* to S-100 bus pin 66. This is NOT an IEEE-696 standard specified signal, but nearly every CPU board manufactured using a Z80 microprocessor supplies this signal. If not, it is very easily provided, simply by routing Z80 pin 28 through a non-inverting buffer to bus pin 66.



ON-BOARD REFRESH CYCLE FIG 2.6a

2.6.1 The emphasis placed on "under ordinary circumstances" above was quite intentional. In order to refresh dynamic memory using the RFSH* signal from the Z80, the CPU must be able to execute op codes, since RFSH* occurs during T3 and T4 of an M1 cycle, which is an op code fetch cycle.

2.6.2 The following conditions will cause the execution of op codes to be inhibited and will destroy the contents of dynamic memory unless they are provided for as exceptions:

- (1) A prolonged reset whose period is greater than 1 millisecond.
- (2) A prolonged wait state whose period is greater than 1 millisecond.
- (3) A prolonged bus acknowledge (DMA) operation greater than 1 millisecond.
- (4) A system clock (referred to as phi clock) of less than 1.216 MHz.

2.6.3 To be safe, conditions 1, 2, and 3 above may *always* be considered as being capable of destroying the contents of memory. The clock rate specified in condition 4 above is based on the continuous execution of the worst-case Z80 instructions, which is an EX (SP),HL. This instruction takes 19 T-states to execute.

2.6.4 No provision has been made on the MEMORY BANK to allow for a system clock of less than 1.216 MHz; therefore, one pre-requirement for use of the MEMORY BANK is a system clock that meets the specifications.

2.6.5 Conditions 1, 2, and 3, however, have been provided for by circuitry that generates an on-board refresh request (as opposed to the normal Z80 RFSH REQUEST) when any of these conditions are true. This section will discuss that circuitry.

2.6.6 Upon acknowledgement of a bus request, during a DMA operation, the CPU will assert pHOLDA true (high) on S-100 bus pin 26. If YY is jumpered, this high level will be applied to 3T-D, pin 9. It will be inverted and applied to NAND gate 3U-B, pin 5, causing the output on pin 6 to go high. This signal, under these circumstances, is called DMA REQUEST, active high true, and occurs whenever we have a DMA operation in progress, thus satisfying condition 3 mentioned at the beginning of this section.

2.6.7 When any slave (typically wait-state synchronized disk controllers) asserts pWAIT on S-100 bus pin 27 true (high), this signal will be applied to inverter 3K-F, pin 11. An inverted (low true) signal from the output of the inverter on pin 10 will be applied to the other input of NAND gate 3U-B, pin 4. Again, this will cause the output of the NAND gate, pin 6, to go high. This signal, under these circumstances, is called WAIT REQUEST, active high true, and will occur whenever we have a wait state, thus satisfying condition 2 mentioned at the beginning of this section.

2.6.8 The combined OR of WAIT REQUEST or DMA REQUEST is inverted by inverter 3K-D, pin 9. The output, on pin 8, is called DMA REQUEST* or WAIT REQUEST*. This signal is applied to NAND gate 4T-D, pin 13.

2.6.9 Now let us consider condition 1 mentioned at the beginning of this section. When RESET* (bus pin 75) or POWER-ON CLEAR* (bus pin 99) or SLAVECLEAR* (bus pin 54) are asserted true (low), we have a reset condition. If SS is jumpered, the MEMORY BANK will monitor RESET*. This is the normal option for most CPUs. If RR is jumpered, the MEMORY BANK will monitor POWER-ON CLEAR* (and unless RESET* also asserts POC*, which is not the usual case, this jumper option is not recommended). For IEEE-standard CPUs, jumper PP is provided, which causes the MEMORY BANK to monitor SLAVECLEAR* for a reset condition.

2.6.10 If we have a reset condition, then, the signal BRESET* will go true (low), and this signal is applied directly to pin 12 of 4T-D.

2.6.11 The output of NAND gate 4T-D, on pin 11, is a signal called START REFRESH, active high true whenever (1) RESET* is true or (2) pHOLDA is true (DMA cycle) or (3) pWAIT is true.

2.6.12 START REFRESH is inverted by 3T-C into START REFRESH*, and this signal is applied to pin 1 of NAND gate 4T-A. START REFRESH* true (low) will cause the output of 4T-A, pin 3, to go high. The other input of NAND gate 4T-A, on pin 1, is a signal called RFSH COUNT*. Upon initialization of the MEMORY BANK, this signal will be high (false).

2.6.13 The output of NAND gate 4T-A, on pin 3, is a signal called COUNTER CLEAR*, and it is applied to the Clear input of the 74LS161 counter at 4S. COUNTER CLEAR* will be true (low) only if (1) REFRESH* and pHOLDA and pWAIT are all false and (2) RFSH COUNT* is false (high). If START REFRESH* goes true, or if RFSH COUNT* goes true, the clear condition of the counter at 4S will be removed and the counter will be partially enabled. Enable P input of the counter (pin 7) is tied high through pullup resistor 3N/8, also partially enabling the counter. The remaining condition which is required to cause the counter to count is a high level on enable T input, pin 10. This condition occurs when the output of NAND gate 4T-C, pin 8, is high. The output of 4T-C is a signal called LOAD* and will be false (high) when (1) RFSH COUNT* is true or (2) when BMRQ is false.

NOTE:

BMRQ is derived from the inverted Z80 MRQ signal MREQ*. The Z80 MREQ* (CPU pin 19) should be passed to the bus on S-100 pin 65. Most CPUs provide this signal, and if they do not, it can be easily jumpered. Some CPUs invert the signal MREQ* before passing it to bus pin 65. If this is the case, selection of option jumper 8 should be made. If, however, the CPU passes MREQ* non-inverted to bus pin 65, select option jumper 7. In any case, BMRQ on the MEMORY BANK should be the Z80 signal MREQ* inverted (active high true). This is the reverse phase of Z80 MREQ*.*

2.6.14 BMRQ will be false (low) whenever the Z80 is inhibited (by a reset, a wait state, or a bus request/acknowledge). When LOAD* is false, the counter is fully enabled and will begin counting on the rising edges of the system clock.

2.6.15 Notice that the counter is preset to a count of 13 (hex D). Therefore, at the *first* count, RFSH COUNT, which is the output of 4R, pin 8, will be low or false. One clock cycle later, the count reaches 14 (hex E), and the output of 4R will go high, causing RFSH COUNT to be true. RFSH COUNT* will also be true, and, acting through 4T-C, holding the counter enabled, will continue the count.

2.6.16 RFSH COUNT is also applied to the J* input of the 74LS109 flip-flop at 4L. This flip-flop is clocked by an *inverted* system clock, so one-half clock time after the counter reaches a count of 14, the Q* output of the flip-flop, on pin 9, will toggle. Since the flip-flop was previously held high, Q* will go low. This low-going pulse is applied to NAND gate 4W-D, pin 13, and the output of the NAND gate goes high, pulsing the delay line.

2.6.17 RFSH COUNT is one of the inputs to the refresh-summation NAND gate 3W-C, coming into the gate on pin 11. A high on this pin will cause the output on pin 8 to go low. This signal is called REFRESH GRANT*. REFRESH GRANT* is used to (1) enable all 4 NAND gates of IC 4N and (2) inhibit the generation of CAS* from IC 4W-C.

- 66. Apply power to the board and remeasure the +5V, +12V and -5V regulators to verify that the voltages are still within their proper limits. If not, immediately remove power and check for ICs that have been inserted backwards. *All switches should be open at this time.*
- 67. Set the board up for port selection using the options guidelines in section 3 of this manual.
- 68. Set the port address switch to decode location 40 hex (switch 4E position 7 open, all others closed). Close position 1 of switch 1K. Apply a reset to the computer. The LED should come on to indicate that the board has been selected.
- 69. Using your computer's monitor, write a 00 out to location 40 hex. The LED should go off. Now write out a 01 to location 40. The LED should come back on.
- 70. Open 1K position 1 and close one of the other switches. Reset the computer. The LED should remain off. Now write a word out to port location 40 that would have a 1-bit in the bit location corresponding to the switch setting at 1K. The LED should come on, indicating that the board has been selected. Writing a 00 out to port location 40 should turn the LED off, indicating that the board has been deselected.
- 71. Install RAM chips and verify your option jumpers. Re-insert the MEMORY BANK in the system and hold reset down. With an oscilloscope, verify that pin 8 of IC 4R is low with a high-going pulse occurring every 14th and 15th clock cycle. Remove the reset and verify that pin 8 of 4R remains low. This procedure tests the on-board refresh counter circuitry.
- 72. Perform a memory test, either using your monitor (all JADE-supplied monitors perform memory tests), or by writing a short memory-test program.

Troubleshooting a board beyond this point exceeds the scope of this manual. The operation of the MEMORY BANK is relatively simple and straight-forward. If it is receiving the proper signals from the CPU, it will perform flawlessly provided the ICs are good and it has been properly constructed. The "Theory of Operation" section of this manual should help you understand the board's operation enough to troubleshoot it, provided you have an understanding of digital electronics. JADE also offers a repair service for those customers who need help. Read your warranty and service policy.

2.6.18 With the NAND gates of IC 4N enabled, the NAND gates of IC 4P wait for the 20 nanosecond delayed high-going pulse from the delay line. When this event occurs (assuming option jumper CC is installed), all four RAS* clocks (RAS0*, RAS1*, RAS2*, and RAS3*) will go low, clocking a row address into all RAM chips in the memory array.

2.6.19 Where does this address come from? REFRESH GRANT* is inverted by IC 3K-C to create REFRESH GRANT (positive true). REFRESH GRANT is applied to pins 1 and 2 of the 3242 Dynamic Memory Controller at 4H. The 3242 has an internal 7-bit refresh address counter. When REFRESH GRANT is high (true), the 3242 will provide a 7-bit row address on its memory address output pins. When REFRESH GRANT is low (false), the counter is incremented by one. Each refresh cycle, therefore, increments the refresh row address count, which proceeds sequentially through 128 row addresses.

2.6.20 To prevent a conflict that might exist when a DMA controller is attempting to access the memory during an on-board refresh cycle, REFRESH COUNT* is applied to NAND gate 3U-D, pin 12. This forces the output of the NAND gate high during the time when REFRESH COUNT* is true (low). The high level from 3U-D is applied to open-collector NAND gate 4U, a 7438, at pin 10. If the board is selected (BS is true), and jumper XX is installed, 4U will pull pRDY low (false), on bus pin 72, forcing the current bus master to enter a wait state. This wait state will be maintained for the length of time the MEMORY BANK is in an on-board refresh cycle.

2.6.21 DMA controllers should monitor pRDY to be in proper IEEE spec. If the controller does not monitor pRDY, there is a possibility of conflict if it attempts to access the MEMORY BANK while an on-board refresh is in progress.

2.6.22 When the counter has cycled through a count of 14 and 15, it will wrap around to zero. This occurs because LOAD* is still false and the counter has not been loaded. The counter will then proceed through 14 counts before it reaches a count of 14 again. During these 14 counts, REFRESH COUNT* is false and pRDY is not pulled low; therefore, DMA memory accesses can occur to the MEMORY BANK.

2.6.23 In summary, the initial on-board refresh cycle occurs after one system clock cycle has passed following a DMA operation, a wait state, or a reset. The board will enter a two clock cycle RAS*-only refresh cycle during the second and third succeeding clock cycles. Thereafter, 14 clock cycles will pass before the board enters another on-board refresh cycle of a length of two system clock periods. The refresh cycle is synchronized to an inverted system clock via the LS109 flip-flop at 4L, and the counter is skewed by one-half clock cycle. The reason for this skew is to allow proper synchronization with BMRQ (see figure X).

2.6.24 When BMRQ goes true (high), the LS161 counter will be disabled. Notice that BMRQ cannot possibly go high when REFRESH COUNT* is true, since the MEMORY BANK has asserted pRDY false during this time. The coincidence of BMRQ true and REFRESH COUNT* false will disable the counter, and load it to a count of 13, making it ready for the next on-board refresh sequence.

2.7 NORMAL REFRESH OPERATIONS

Whenever the Z80 is *not* inhibited by one of the three conditions listed at the beginning of the previous section, and it is capable of executing op codes, it will generate a RFSH* signal on CPU pin 28. This is applied to the bus on pin 66 and is received by the MEMORY BANK at IC 3X-D, which inverts it and generates Z80 RFSH (positive true).

Assuming jumper *MM* is installed, Z80 RFSH will be applied to the refresh summation NAND gate 3W-C on pins 9 and 10. The output of the NAND gate will go low, generating REFRESH GRANT* true. REFRESH GRANT* is inverted by 3K-C to create REFRESH GRANT, which is applied to the 3242 Dynamic Memory Controller as explained in the previous section, causing the IC to output a refresh row address to the memory.

2.7.1 REFRESH GRANT* enables the four NAND gates of 4N, as before, and inhibits CAS* generation as previously explained. This leaves one more condition to be satisfied: the delay line must be pulsed to generate the 20 nanosecond RAS ENABLE signal.

2.7.2 During T3 and T4 of the Z80's M1 state, MREQ* on the CPU will be asserted true in coincidence with RFSH* for an op code refresh cycle. MREQ* at the CPU will generate BMRQ on the MEMORY BANK, and this signal is applied to NAND gate 4T-B, on pin 4. Since REFRESH COUNT* will be false (high), the NAND gate is enabled and issues a low-going pulse. This pulse is applied to NAND gate 4W-D, on pin 12, forcing the output on pin 11 high. This high-going pulse is delivered to the delay line where, 20 nanoseconds later, RAS ENABLE will go high. Since the outputs of the NAND gates at 4N are all high, these Nanded with the 20-nanosecond RAS ENABLE will generate all four RAS* clocks. These are passed to the dynamic memory chips in the memory array, and the RAMs are refreshed. When the cycle ends, the refresh counter in the 3242 Dynamic Memory Controller is incremented by one and the MEMORY BANK is ready for the next machine state.

2.7.3 One other effect of the REFRESH GRANT* signal should be mentioned here. When REFRESH GRANT* is true (low), it is applied to NAND gate 3U-C at pin 9. The output of the NAND gate will go high, and this high-going pulse is inverted by 3K-B, to form LATCH* on pin 4. LATCH* is applied to the LS373 output buffers on their latch enable pins, latching the data that was present in the output buffers prior to the refresh cycle.

2.7.4 This completes the description of the refresh circuitry of the MEMORY BANK. Circuitry exists on the board to generate an 8080-type refresh request, but this will be explained later under 8080 options.

2.8 READ AND WRITE TIMING

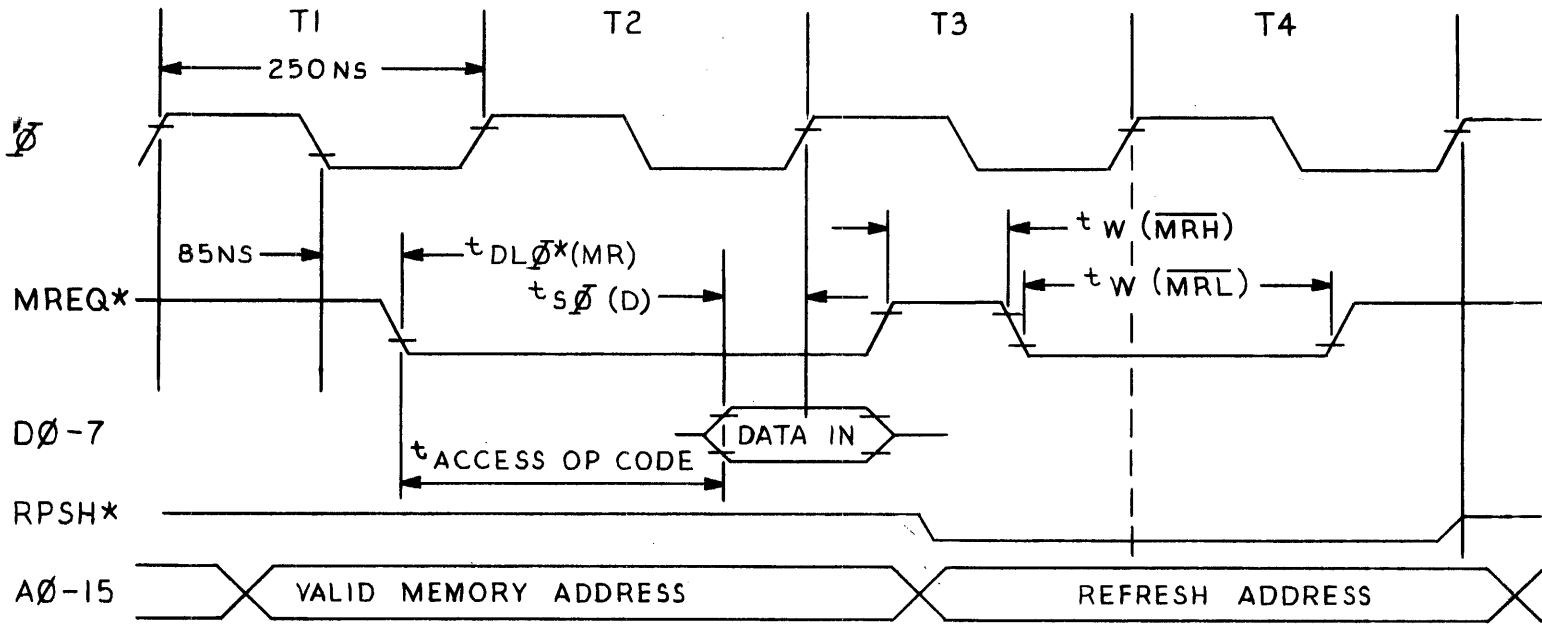
Figures 2.8a, 2.8b, and 2.8c show the timing relationships of the control signals, address bus, and system clock for a Z80. Using these diagrams, we can show the worst case access times for a Z80 CPU operating at 4 MHz. First, we will determine the access time required for an op code fetch cycle (M1 cycle).

2.8.1 An M1 cycle access time can be determined by the following equation:

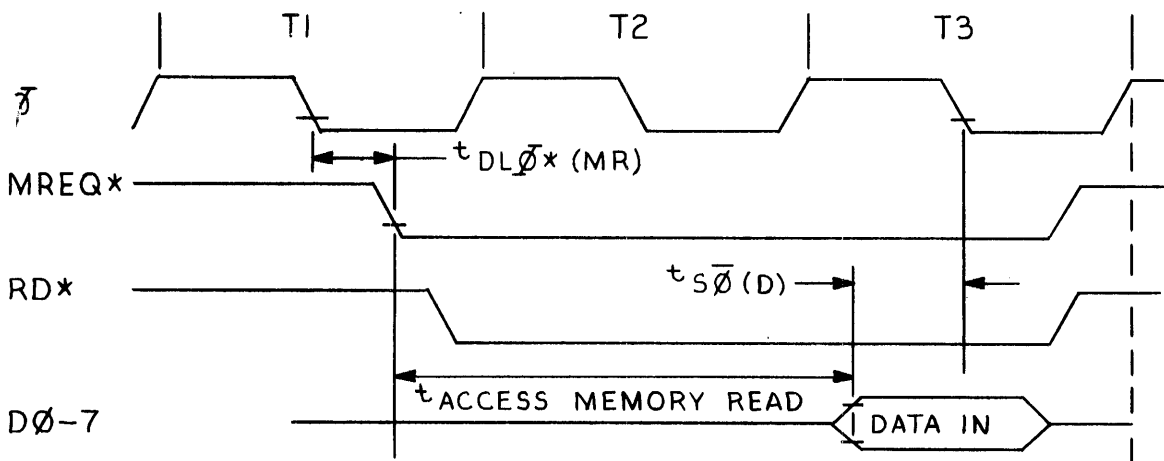
$$[1] \quad T(\text{M1 access}) = 3(t_c/2) - t_{DL\bar{\Phi}^*}(MR) - t_{S\bar{\Phi}}(D)$$

T sub c is the memory cycle time, so 3 times T sub c divided by 2 = 275 nanoseconds. T sub DL $\bar{\Phi}^*(MR)$ is the specified delay between the falling edge of the system clock and the falling edge of MREQ*. For a 4 MHz Z80, this is specified by Zilog as a maximum of 85 nanoseconds. T sub S $\bar{\Phi}(D)$ is the specified data setup time prior to the rising edge of the T2 clock during an op code fetch cycle. For a 4 MHz Z80, this is specified by Zilog as 35 nanoseconds minimum. Putting all this together, we see that the worst-case required memory read access time for an M1 cycle is 375 nanoseconds minus 85 nanoseconds minus 35 nanoseconds, or 255 nanoseconds. Please note that this is referenced to the CPU, and does not count any timing delays introduced by buffers and inverters in the system.

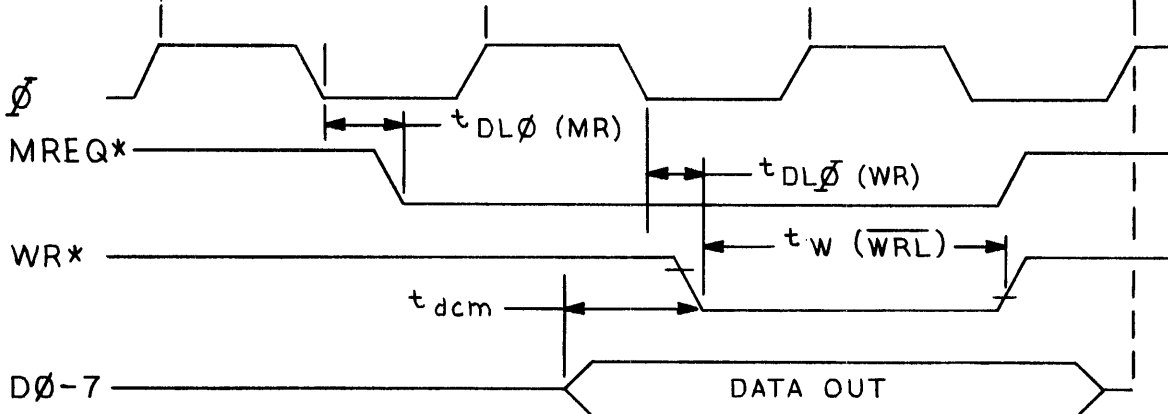
OP CODE FETCH TIMING FIG 2.8a



MEMORY READ TIMING FIG 2.8b



MEMORY WRITE TIMING FIG 2.8c



2.8.2 Now let us derive a worst-case system timing. A typical buffer used to place the Z80 MREQ* signal onto bus pin 65 would introduce a delay of 15 nanoseconds. MRQ* enters the MEMORY BANK through an LS04 inverter, which consumes 9 nanoseconds, and it is then gated through two LS00 NAND gates (4T-B and 4W-D), introducing a delay of 19 nanoseconds. Using the recommended delay line for 4 MHz operation, exactly 10 nanoseconds will pass before RAS ENABLE is generated. The NAND gates at 4P will introduce another 9 nanosecond delay while they are generating RAS* clocks. The data output buffers on the MEMORY BANK will add 15 nanoseconds delay, and the typical data input buffer on a CPU board will introduce another 15 nanoseconds delay.

2.8.3 Thus the total gate delays introduced by the CPU and the MEMORY BANK are 82 nanoseconds. Subtracting this from the 255-nanosecond worst-case op code fetch cycle required accesstime for the Z80, we arrive at a figure of 173 nanoseconds. This is the maximum time allowed for access from the RAS* clock; therefore, a RAM chip with a maximum RAS* access time of 150 nanoseconds would be acceptable for use in the MEMORY BANK with a 4 MHz Z80 processor. In reality, however, the *actual* RAS* access time can be greater, since the delays mentioned here are worst-case delays. In point of fact, 200-nanosecond access RAMs will perform quite satisfactorily.

2.9 MEMORY READ ACCESS TIMING

A memory read access timing that is *not* an M1-cycle (op code fetch), can be determined from the following equation (see figure 2.8b):

$$[2] \quad t(\text{memory read access}) =$$

As before, $T_{sub c}$ is the clock cycle time, so 4 times the clock cycle time divided by two equals 500 nanoseconds for a 4 MHz Z80. $T_{sub DL\Phi^*(MR)}$ is the same specification determined in the first equation, and is 85 nanoseconds for the 4 MHz Z80. $T_{sub S\Phi^*(D)}$ is the specified data setup time prior to the *falling* edge of the clock in T3 of the read cycle, and is specified by Zilog for a 4 MHz Z80 as 50 nanoseconds. Putting this all together, we arrive at a worst-case memory read access time for a memory read that is not an op code fetch (M2-M5 cycle) of 500 nanoseconds minus 85 nanoseconds minus 50 nanoseconds, or 365 nanoseconds. As before, this is referenced to the CPU and does not take into account any delays introduced by buffers and inverters or other gates in the system.

2.9.1 It is easy to see that any RAM memory meeting the required specifications for the M1 read cycle will also meet an M2-M5 read cycle, since for memory reads that are not op code fetches, we have an extra 125 nanoseconds (one-half clock time) to work with, (less, of course, the slight difference between the different data setup requirements for the different types of cycles).

2.10 MEMORY WRITE TIMING

There are two write cycles that are of interest to us. First is the specification for the time that data will be stable at the CPU, which may be expressed by the following equation (see figure 2.8c):

$$[3] \quad t(\text{data stable}) = 3(t_c/2) + t_{DL\Phi^*(WR)} - t_{dcm}$$

$T_{sub DL\Phi^*(WR)}$ is the specified delay from the falling edge of the clock in the T2 cycle

to the falling edge of the WR* signal. T sub dcm is the specified data setup time prior to the falling edge of the WR* signal. The first parameter is specified as 80 nanoseconds maximum for a 4 MHz Z80; the second parameter is the system clock cycle time minus 170, or 80 nanoseconds. It is therefore easy to see that write data will be stable, worst case, at the Z80 in coincidence with the falling edge of the T2 cycle during a memory write, or 375 nanoseconds.

2.10.1 The second parameter of interest is the delay from MREQ* to WR*. The falling edge of MREQ* will occur not later than 210 nanoseconds into the write cycle, and WR* will occur not later than 45 nanoseconds into the cycle. The worst-case difference will, then, be 245 nanoseconds.

2.10.2 The minimum width of the write pulse in its active low state is one clock cycle less 30 nanoseconds, or 220 nanoseconds ($t_w(\text{WRL}^*)$). It may be assumed that the Z80 will hold its write data valid throughout the WR* signal.

2.10.3 There are no specific write access requirements for the MEMORY BANK, since we do not have a bidirectional data bus for the data in and data out pins of the RAM chips.

2.11 INTERFACE TO S100 BUS

The following signals are *required* signals for proper operation of the MEMORY BANK:

Address Lines 0 through 15 (A0-A15)

Data In Lines 0 through 7 (DI0-7)

Data Out Lines 0 through 7 (DO0-7)

Bus Utilities Lines:

+8V on pins 1 and 51

+16V on pin 2 and -16V on pin 52

Ground on pins 20, 50, 70, and 100

Reset* on pin 75

Status Lines:

sOUT on pin 45

sINTA on pin 96

Control Lines:

pHOLDA on pin 26

pWR* on pin 77

pDBIN on pin 78

Miscellaneous Required Lines:

MRQ* or MRQ on pin 65

RFSH* on pin 66

$\bar{\Phi}2$ on pin 24

2.11.1 The following signals are optional:

Optional Lines:

sMEMR on pin 47

sMWRT on pin 68

pSTVAL* on pin 26

sM1 on pin 44
 POC* on pin 99
 SLVCLEAR* on pin 54
 sXTRQ* on pin 58
 pHALTA on pin 48
 pWAIT on pin 27
 PHANTOM* on pin 67
 Address lines 16 through 23 (A16-23)

2.11.2 The MEMORY BANK will provide the following output signals:

pRDY on pin 72
 sXTN* on pin 60

2.12 BOARD SELECTION MECHANISM

The board may be selected as a port, or by decoding the extended address bus defined by IEEE (A16-23). We will discuss the port selection mechanism first. pWR* is received from bus pin 77 by 4C-C, pin 5. R5 and C6 are provided as a noise filter and should be on the order of 200 ohms and 47 picofarads respectively. pWR* is inverted by 4C-C and appears on pin 6 as BPWR.

2.12.1 BPWR is Nanded with sOUT from bus pin 45 by 3U-A to derive the signal BPORT* from the output of 3U-A on pin 3. BPORT* is inverted by 3T-E into BPORT, which is true (high) when sOUT and pWR* are both true. BPORT is then routed to jumper B. If jumper B is selected, the equals-enable input to 3D, a 74LS85 comparator, is an I/O output cycle signal.

2.12.2 If the Port Address jumpers are selected (V, R, L, F, T, N, J, and D), address lines 0 through 7 are applied to the A inputs of the comparators at 3D and 3E, and switch 4E will decode the port address according to the following table:

1	2	3	4	5	6	7	8	Port Address (in hex)
C	C	C	C	C	C	C	C	= 00
C	C	C	C	C	C	O	C	= 02
C	C	C	C	C	C	O	O	= 03
C	C	C	C	C	O	C	C	= 04
C	C	C	C	O	C	C	C	= 08
C	C	C	O	C	C	C	C	= 10
C	C	O	C	C	C	C	C	= 20
C	O	C	C	C	C	C	C	= 40 (Cromemco, etc.)
O	C	C	C	C	C	C	C	= 80
O	O	O	O	O	O	O	O	= FF (SD Systems)

2.12.3 A switch position that is CLOSED compares the corresponding address to a ZERO. Conversely, a switch that is OPEN compares the corresponding address bit to a ONE. If the switches are installed with 1 toward the top of the board, the addresses will run from A0 through A7, top to bottom, sequentially, as shown in the table above.

2.12.4 Comparator 3D has its greater-than and less-than inputs tied high. Its greater-than and less-than outputs are tied to the greater-than and less-than inputs of comparator 3E. Its

equal output is also tied to the equal input of comparator 3E. The equal output of comparator 3E provides a positive-going pulse to flip-flop 4L-A on its clock input pin (pin 4). Therefore, the flip-flop will receive a positive-going clock pulse whenever an I/O write command to the port selected by the switches at 4E is performed.

2.12.5 The data written to the port is received on the data out lines by IC 2K, a 74LS240 *inverting* bus receiver. The outputs of the receiver are routed to Switch 1 at 1K. Properly installed, switch position 1 will correspond to data bit 0, and switch position 8 will correspond to data bit 7. Bits 1 through 7 are tied together at pins 9 through 15 of the switch and this line is then routed to pin 1 of NAND gate 4K-A. A pullup resistor, 4D-7, insures that the line is held high unless a data bit is written out to the port. Data bit 0 is tied, through switch position 1, to pins 2, 12, 13, and 9 of the NAND gate at 4K.

2.12.6 Only *one* switch at 1K should be ON at any one time; all the rest must be off. When a one is written to the data bit corresponding to the switch that is turned on, the board will be selected.

2.12.7 Notice that 4K-A produces high output for a one in bit position 0, OR a one in bit positions 1 through 7, but only if the corresponding switch is thrown. This high-going pulse is applied to the J-K* input of 4L, a 74LS109 flip-flop. Assuming that the preset and clear inputs to the flip-flop are both high (pins 5 and 1 respectively), the flip-flop will be set at the rising edge of the clock pulse and the board will be selected. If, however, a data bit pattern of 00 hex, or a one in a bit position that is not transmitted by the switch position corresponding to the bit's position, is written to the port, then the output of 4K-A will be low and the flip-flop will be reset, deselecting the board.

2.12.8 The conditions under which preset and clear will both be high are as follows: Preset will be held high when (a) BRESET is false OR (b) data bit 0 is a zero on the bus (and therefore false). Clear will be held high when (a) BRESET is false OR (b) when data bit 0 is *true* on the bus. The condition of data bit 0 is overridden by the false condition of BRESET, therefore the condition of bit 0 is of no consequence in this particular state.

2.12.9 The flip-flop will also be set (and the board therefore selected) when preset is low and clear is high, irrespective of the conditions of the clock or J-K* inputs. This occurs under the following conditions:

2.12.10 Preset is made low by (a) BRESET true AND (b) data bit 0 being true. Clear is made high by (a) BRESET being false OR (b) data bit 0 being true. Therefore, RESET* accompanied by a high on data bit 0 will set the flip-flop and select the board.

2.12.11 The flip-flop will be reset (and the board therefore deselected) when preset is high and clear is low, again irrespective of the conditions of the clock or the J-K* inputs. This occurs under the following conditions:

2.12.12 Preset is made high by (a) BRESET being false OR (b) data bit 0 being false. Clear is made low by (a) BRESET being true AND (b) data bit 0 being false. It is easy to see, therefore, that the board will be deselected at any time that RESET* is true and data bit 0 is false.

2.12.13 To select the board under RESET* conditions, therefore, data bit 0 must contain a one. If it does not, then the board must wait for an output to the correct port address which writes a one bit to the bit position selected by switch 1K. Most CPUs in a properly terminated bus will provide a high enough level on the data lines during reset to properly select the MEMORY BANK on which position 1 of switch 1K is closed. If it does not, then pullup resistor 4D-B may

be cut from the line (merely remove pin 8 from the resistor pack). and bus receiver 2K will pass a low enough signal to properly select the board.

2.12.14 The Q* output of flip-flop 4L-A is routed to the PROM enable line and to the cathode side of CR2, an LED. The anode of CR2 is tied through a 1K resistor, R1, to +5V. When the board is selected, Q* will go low, the PROM will be enabled, and CR2 will light. When the board is not selected, Q* will be high, the PROM will be disabled, and CR2 will not light since it will not have enough voltage differential across it to trigger it into conduction.

2.12.15 The Q output of flip-flop 4L-A is routed to NAND gate 4U-C, where it is one of the conditions required to drive pRDY low. (The other condition is explained in the Refresh Circuitry analysis earlier in this section). It is also routed to AND gates 3B and 3C as one of the READ and WRITE enables.

2.12.16 *Port selection is recommended for this manufacturing revision level of the board.* Extended addressing selection is recommended only when there is one MEMORY BANK in the system.

2.13 READ-WRITE CIRCUITRY - GENERAL

The read-write circuitry of the MEMORY BANK consists of the following ICs: A 74LS244 non-inverting bus receiver at 2L; three 74LS373 latched bus drivers at 1L, 1M, and 1N; two 74LS157 multiplexers at 2N and 2M; and steering logic composed of AND gates 3C, 3B, and 3A; NOR gate 4A; two sections of inverter 4B, and the Bank Select PROM at 3L (see figure 2.13a).

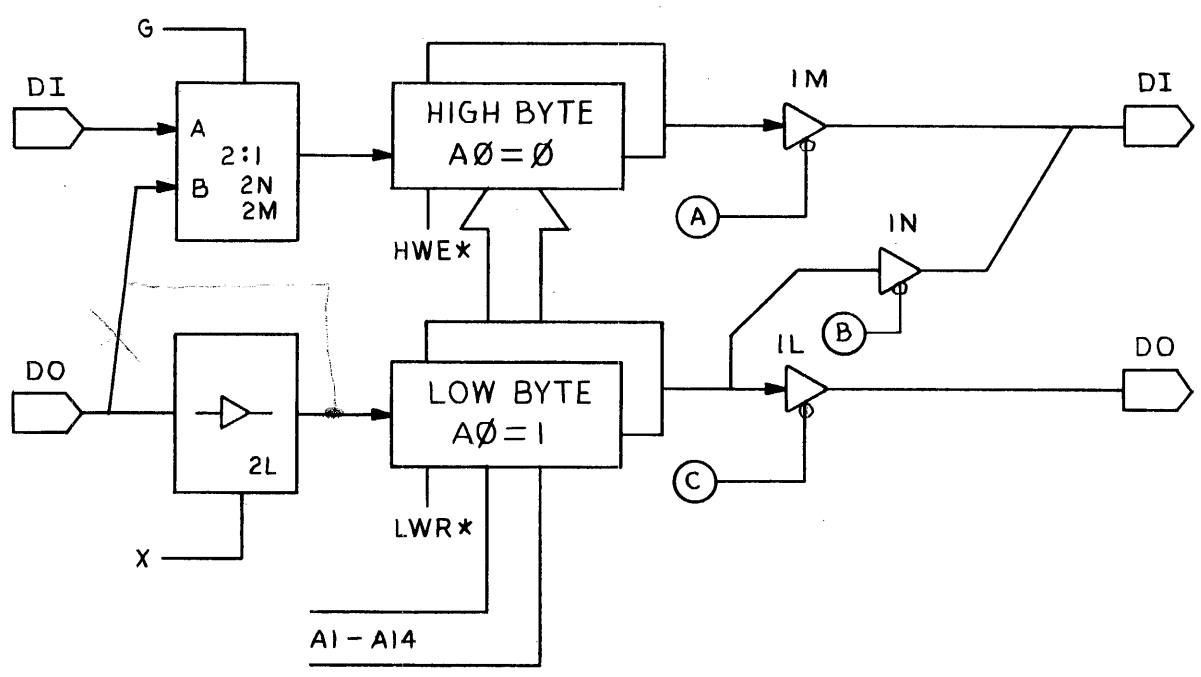
2.13.1 Let us consider the steering logic first. AND gate 3C-A has the task of generating a signal called 8READ. It does this by ANDing BOARD SELECTED (the Q output of flip-flop 4L-A), B16RQ* (sixteen request false), BPDBIN (pDBIN true) and the output of NOR gate 3W-B, a 74LS27 whose inputs are BANKSUM*, BPHANTOM and BSINTA. A high on any one of these latter three inputs will result in a low output from 3W-B, pin 6. An 8READ is, then, disabled by (a) BANKSUM* high (no banks are selected by the PROM), OR (b) PHANTOM* asserted, OR (c) sINTA true. The disabling of 8READ when sINTA is true is to prevent the output buffers from being enabled during a CPU interrupt-acknowledge cycle, which could result in a conflict on the bus. For 8READ to be generated, then, *all* of the following conditions must be true: (a) the board must be selected; (b) pDBIN must be true; (c) sXTRQ* must be false; (d) PHANTOM* must not be asserted; (e) sINTA must be false, and (f) one of the RAM banks must have been selected by the Bank Select PROM.

2.13.2 AND gate 3C-B generates a signal called 16READ under the same conditions explained above, with the following exception: B16RQ must be true (sXTRQ* is asserted low on the bus and the CPU is requesting a 16-bit data transfer). Please notice that 8READ and 16READ are mutually exclusive.

2.13.3 AND gate 3B-A generates a signal called 8WRITE by ANDing together the following signals: (a) B16RQ*, (b) BOARD SELECTED, (c) BPWR, and (d) BMRQ. To generate 8WRITE, the following conditions must be true: sXTRQ* must be false; pWR* must be asserted true; MRQ* on the bus must be asserted true; and the board must be selected.

2.13.4 The other side of AND gate 3B-A generates a signal called 16WRITE by ANDing together the signals mentioned above with the following exception: sXTRQ* must be asserted true (low on the bus, signifying that the CPU is requesting a 16-bit data transfer for a memory

$G : \quad \overline{SXTRQ}$
 $A : (\overline{DEV_SEL} \cdot \overline{SXTRQ} \cdot \overline{PDBIN}) + (\overline{DEV_SEL} \cdot \overline{SXTRQ} \cdot PDBIN \cdot \overline{A0})$
 $B : (\overline{DEV_SEL} \cdot \overline{SXTRQ} \cdot PDBIN \cdot A0)$
 $C : (\overline{DEV_SEL} \cdot \overline{SXTRQ} \cdot PDBIN)$
 $HWE : (\overline{DEV_SEL} \cdot \overline{SXTRQ} \cdot \overline{PWR}) + (\overline{DEV_SEL} \cdot \overline{SXTRQ} \cdot PWR \cdot \overline{A0})$
 $LWR : (\overline{DEV_SEL} \cdot \overline{SXTRQ} \cdot \overline{PWR}) + (\overline{DEV_SEL} \cdot \overline{SXTRQ} \cdot PWR \cdot \overline{A0})$



ORGANIZATION OF RAM ARRAY FIG 2.13a

write cycle).

2.13.5 A 74LS08 AND gate at 3A is charged with the responsibility of steering the 8READ and 8WRITE signals according to the status of bus address line 0 (A0). Section A (pins 1, 2, and 3) generates a signal which is 8WRITE ANDed with BA0 (Address line 0 is asserted true or high). 3A-D generates a signal which is 8WRITE ANDed with BA0F (Address line 0 is asserted false or low).

2.13.6 8WRITE AND A0 is routed from 3A-A pin 3 to NOR gate 4A-B, where it is ORed with 16WRITE. The output of this NOR gate, on pin 4, is routed to option jumper 13 where it will generate a signal called LWRITE*. This signal is applied to the WRITE* pins of all the RAMs in the low-byte section of the memory array.

2.13.7 8WRITE AND -A0 is routed from 3A-D, pin 11, to NOR gate 4A-C where it is ORed with 16WRITE. It generates a signal called HWRITE* from its output pin 10 which is routed to option jumper 15. If option jumper 15 is selected, the signal HWRITE* will be applied to the WRITE* pins of all the RAMs in the high-byte section of the memory array.

2.13.8 8WRITE is also routed to inverter 4B-B, where it is inverted and applied to option jumpers 14 and 16. If these jumpers are selected, the WRITE* pins of all the RAMs in the memory array will be driven low by 8WRITE to provide consecutive byte operation of the board.

2.13.9 8READ is routed to AND gate 3A-B where it is ANDed with BA0 to generate a signal called 8WRITE AND A0. This is inverted by NOR gate 4A-D and is applied to jumper option 6.

2.13.10 8READ is also routed to 3A-C where it is ANDed with BA0*. The output of 3A-C on pin 8 is ORed with 16READ by NOR gate 4A-A and the output of 4A-A (pin 1) is routed to jumper option 4.

2.13.11 If jumper option 6 is selected, 8WRITE AND A0 will enable output driver 1N. If jumper option 4 is selected, 8WRITE AND -A0 OR 16WRITE will enable output driver 1M. 16READ is also applied to inverter 4B-C where it is inverted to generate a signal called 16READ*. 16READ* enables output buffer 1L.

2.13.12 8READ is inverted by 4B-A to generate 8READ* which is applied to jumper options 3 and 5. If these jumper options are selected, both output buffers 1M and 1N will be enabled for consecutive-byte operation of the board.

2.13.13 The inputs to data output buffers 1L and 1M are derived from the high-byte RAM array sections. 1L, when enabled, will place the high-byte (bits 8-15) onto the Data Out bus during a 16-bit transfer. Notice that it is *only* during a 16-bit data read that buffer 1L will be enabled. At all other times it is tri-stated and therefore transparent to the data-out bus pins.

2.13.14 Data output buffer 1M, whose inputs are also derived from the high-byte RAM array sections, will, when enabled, place the high-byte (bits 8-15 of a 16-bit word to be transferred sequentially) onto the data input pins on the bus. This situation occurs when A0 is asserted false (low). Data output buffer 1N has its inputs connected to the low-byte RAM array sections, and it is enabled when A0 is asserted true (high), OR during a 16-bit transfer.

2.13.15 In summary, buffer 1N reads the low-byte RAM array onto the data in bus when (a) 16READ is asserted or (b) 8READ is asserted with A0 asserted true. Buffer 1M reads the high-byte RAM array onto the data in bus when 8READ is asserted with A0 asserted false (low), and buffer 1L reads the high-byte RAM array onto the data *out* bus when 16READ is asserted true. For 16-bit parallel transfers, then, buffers 1L and 1N are enabled. For sequential 16-bit

transfers, first the high-byte is read with A0 asserted false and data output buffer 1M is enabled, followed by a read of the low-byte with A0 asserted true and data output buffer 1N is enabled.

2.14 SEQUENTIAL BYTE REFERENCES

When sXTRQ* is not asserted, memory transfers are single-byte transactions. The proper location in memory is selected by the address output on address lines A1 through A15 (A23 for extended addressing systems), while the A0 line selects the high byte or the low byte.

2.14.1 When A0 is low (false), the high byte of the 16-bit word is selected. When A0 is high (true), the low byte of the 16-bit word is selected.

2.14.2 In the sequential-byte mode, data output from the CPU or bus master is transferred on the DO bus and is connected to the data input lines of both the high-byte and low-byte RAM arrays. The low-byte data input lines of the RAM arrays are connected through bus receiver 2L directly to the DO lines. The high-byte data input lines of the RAM array are connected to the DO bus through 2L via two-to-one multiplexers (74LS157) 2M and 2N. These multiplexers are controlled by sXTRQ*. When sXTRQ* is false (high) on the bus, the B inputs of the multiplexers are transferred to the outputs. The B inputs are connected to the DO bus via bus receiver 2L. The multiplexer outputs are connected to the data input pins of the high-byte RAM arrays.

2.14.3 For an 8-bit sequential read, data output from the low-byte RAM arrays is routed to tri-state buffer and bus driver 1N which is enabled when the read strobe is activated with A0 true (high). Data output from the high byte RAM arrays is routed to tri-state buffer and bus driver 1M which is enabled when the read strobe is activated with A0 false (low). Both of these buffers/bus drivers have their outputs routed to the DI bus, and the selected byte (low-byte or high-byte) is available to the CPU or bus master on the DI bus.

2.15 CONSECUTIVE BYTE REFERENCES

Consecutive byte references are memory transfers in which address lines A14 and A15 select which RAM bank is to be referenced.

2.15.1 Address lines A0 through A13 are routed to the RAM array as opposed to A1 through A14. This enables a 16K bank to be comprised of only one bank of RAM chips where sequential-byte transfers would require 2 banks for the same 16K. For write transactions, both LWRITE* and HWRITE* are asserted at the same time, and for read transactions, both buffer/bus drivers 1M and 1N are enabled. There will be no contention for the DI bus, since the data output pins of any RAM bank not selected will have its RAS* clock high and will therefore be tri-stated.

2.16 WORD REFERENCES

When sXTRQ* is asserted true (low) by the CPU or bus master, memory references are double-byte transfers.

2.16.1 As with sequential-byte transfers, address lines A1 through A15 (A23 in extended address systems) selects the proper word from memory. The condition of the A0 bit is

disregarded and does not participate in the decoding or addressing for word references.

2.16.2 In the 16-bit mode, data output from the CPU or bus master is asserted on the 16 signal lines of the DO bus and the DI bus. Again, the inputs to the low-byte RAM array are routed from the DO bus through bus receiver 2L. Now, however, the multiplexers select the A inputs, and the data input lines to the high-byte RAM array are derived from data present on the DI bus. LWRITE* and HWRITE* are asserted true at the same time. Data bits 0 through 7 are strobed into the low-byte RAM array, and data bits 8 through 15 are strobed into the high-byte RAM array.

2.16.4 The following logic equations summarize the memory organization:

$$\text{HWRITE}^* = 16\text{WRITE} + (8\text{WRITE} \bullet -\text{A0})$$

$$\text{LWRITE}^* = 16\text{WRITE} + (8\text{WRITE} \bullet \text{A0})$$

$$\text{A}^* = 16\text{READ} + (8\text{READ} \bullet -\text{A0})$$

$$\text{B}^* = 8\text{READ} \bullet \text{A0}$$

$$\text{C}^* = 16\text{READ}$$

$$16\text{READ} = \text{board select} \bullet \text{sXTRQ}^* \bullet \text{pDBIN} \bullet \text{BANKSUM}^* \bullet -\text{PHANTOM}^* \bullet -\text{sINTA}$$

$$8\text{READ} = \text{board select} \bullet -\text{sXTRQ}^* \bullet \text{pDBIN} \bullet \text{BANKSUM}^* \bullet -\text{PHANTOM}^* \bullet -\text{sINTA}$$

$$16\text{WRITE} = \text{board select} \bullet \text{sXTRQ}^* \bullet \text{pWR}^*$$

$$8\text{WRITE} = \text{board select} \bullet -\text{sXTRQ}^* \bullet \text{pWR}^*$$

G = L = select A for 16-bit word references

E = H = select B for 8-bit byte references

NOTE: + = OR • = AND - = FALSE CONDITION.

2.17 BANK SELECT PROM

Also governing the RAM array selection mechanism is the high-speed PROM located at IC position 3L. It is a 93427, 256 x 4-bit PROM. It is enabled by BOARD SELECT* (the Q* output of IC 4L-A), and its address inputs are B16RQ, and various options jumpers as explained in section 3 of this manual which select between A0, A14, A15, A16, A17, 16K, 64K, and use of the Partial Bank Disable circuit or not. The status of the various address inputs to the PROM are programmed to provide the proper bank select on its data out pins 9, 10, 11, and 12.

2.17.1 These data out pins are routed to switch 3M, sections 1 through 4, which provide a means of disabling any 16K bank. The bank select signal is active low, and pullup resistors are provided by resistor pack 3N to prevent spurious transitions. Provided the switch sections are closed at 3M, the data out signals from the PROM are routed to NAND gate 4N which, in conjunction with NAND gate 4P, generate RAS0* through RAS3*.

2.18 PARTIAL BANK DISABLE CIRCUIT (FORCED PHANTOM)

IC 4M-A, in conjunction with CR3, two sections of pullup resistor 3N, and switch 3M sections 5 and 6, comprise a partial bank disable circuit. This circuit is provided to disable the upper 4K or 8K of memory for those CPU boards that do not provide a proper PHANTOM* signal when they are reading EPROM Monitors or Boot Loaders. (It may also be used to prevent conflicts with memory-mapped video boards in these upper locations).

2.18.1 AND gate 4M-A will provide a low output which enables the PROM at 3L whenever any one of the inputs are low. This will occur anytime A15 or A15 is low.

2.18.2 It will also occur anytime switch position 6 of 3M is closed. This grounds pin 4 of 4M, forcing a low. Diode CR3 is provided to prevent the grounded address line from being transferred back to A13. Switch position 6, then, can be used to defeat the partial bank circuit.

2.18.3 Switch position 5, when open, disconnects A12 from the circuit and the A12 input to 4M-A is tied high through pullup resistor 3N-6. The status of A12, then, is a "don't care" and addresses E000 hex through FFFF hex will be disabled. If switch position 5 is open, therefore, the top 8K of memory is disabled.

2.18.4 If switch position 5 is closed, however, the status of A12 *does* matter and only addresses F000 through FFFF hex are disabled, thus disabling only the top 4K of memory.

2.18.5 If switch position 6 is closed, the circuit is disabled and no memory will be disabled; to disable the top 4K or 8K of memory, open switch position 6 and set switch position 5 according to the above explanation.

2.18.6 *The use of this circuit is recommended for 8-bit consecutive operation mode only.*
For 16-bit parallel or 8-bit sequential operation, select jumper option 9. To use this circuit, select jumper option 10.

2.19 OP CODE FETCH (M1 CYCLE) WAIT STATE GENERATOR

The M1 (op code fetch cycle) wait state generator consists of IC 3S, a 74LS74 positive-edge triggered D-type flip-flop; pullup resistors 3N-9 and 3N-10, and option jumpers *BB* and *XX* (see figure 2.19a).

2.19.1 The reset inputs to section A and B and the set input to section B are tied high by pullup resistor 3N-10. Both sections are clocked by BO2, a clock having the same polarity as the Z80 CPU clock.

2.19.2 If jumper *BB* is installed, BM1* is routed to the D input of section A. When BM1* is low during T1 of an op-code fetch, the next positive-going clock edge will reset the flip-flop and the Q output of section A will go low. This low signal is connected to the D input of section B and is also connected to NAND gate 3U-D at pin 13. The low-going pulse at 3U-D presents a high from its output to open-collector NAND gate 4U-C at pin 10. If the board is selected, there will also be a high at pin 9 of 4U-C, forcing pRDY low. This will occur on the rising edge of the system clock at the beginning of T2 of the op code fetch cycle. The CPU will sample pRDY during T2 and, when it finds that it is low, will proceed to insert one wait state.

2.19.3 The next rising clock edge will reset section A of the flip-flop, and pRDY will go high. It will be held high until the rising clock, which is the beginning of the T3 cycle. By this time, BM1* is false (high), and the flip-flop remains in its high state until the next time BM1* is asserted low, which will be during the next M1 cycle.

2.19.4 Notice that for pRDY to be enabled onto the bus, jumper option *XX* must be selected.

2.20 PRECHARGE EXTENDER OPTION

The Precharge Extender Option consists of IC 3R, a 74LS74 flip-flop; AND gate 4R-B and pullup resistors 3N-5 and 3N-11. It is enabled by jumper option *DD*. The operation of this circuit can be explained as follows (see figure 2.20a):

2.20.1 The D flip-flops are held in their reset condition by BMRQ being asserted false (low). When BMRQ goes true (high), the D inputs of sections A and B will be transferred to the outputs on the next positive-going clock edge. Now, if BM1 was true (high) when section A was clocked, the Q output of section A will go high. This output is applied to the D input of section B. On the next positive-going clock edge, the Q* output of section B will go low. This will cause the output of 4R-B to go low, disabling the generation of RAS* clocks by NAND gate 4P. When BMRQ goes inactive (low), the flip-flops will be reset.

2.20.2 The Precharge Extender circuit will give a minimum of 126 nanoseconds precharge for dynamic RAMs operating with a 4 MHz Z80. For a computation of the 126 nanosecond modified $t_w(\text{MRH})$, see the timing diagram in figure 2.20a.

SECTION THREE

OPTIONS JUMPERS

3.0 OPTIONS JUMPERS

In an attempt to manufacture a memory board that would be as versatile as possible, we have provided what might, at first, seem to be a bewildering array of options jumpers. However, these are not as bewildering as they might seem at first glance. It is the purpose of this section of the manual to guide the user into the proper selection of the options jumpers.

3.0.1 The first thing the user should do is to determine whether he will address the memory board as a port or use the extended address bits (A16-A23) to select the board. Most current CPU boards require the memory to be addressed as a port (SD Systems, Cromemco, Alpha Micro, Northstar, etc.).

3.1 PORT SELECTION

The MEMORY BANK's board select circuitry can reside at any of the first 256 port locations, with up to 8 boards selectable for the first port address. Multiple port addresses can also be used, and up to 7 boards can reside at any subsequent port location. A total of 1793 boards can be used in the system, or more rationally a board can reside at any of 1793 locations. This is accomplished by a combination of port addressing and writing out one of 8 data bits to the port.

3.1.1 Jumper A/B, located below and to the right of IC 3C, selects extended addressing versus port addressing. If jumper A is installed (center pin to top pin), the equal input to comparator 3D is pulled up to +5 volts through pullup resistor 4D-2, and the comparators are always enabled. If jumper B is installed (center pin to lower pin), the equal input to 3D is derived from the output of 3T-10, which is the inverted NAND of sOUT and pWR* (output to a port).

3.1.2 Jumpers V, R, L, F, T, N, J, and D are used to tie the bus address lines A0 through A7 respectively to the inputs of comparators 3D and 3E. These jumpers are located at IC position 3F, and the proper jumpers for port addressing are all aligned on the right side of 3F. All of these jumpers must be installed.

3.1.3 Assuming A0-A7 are jumpered, switch 4E then selects the port address, with A0 being the topmost switch (furthest from the S-100 bus), and A7 being the lowermost switch. If the switch is ON, the comparison is to a logical zero (low level); conversely, if the switch is OFF, the comparison is to a logical one (high level), since the address inputs are either pulled high by pullup resistors in the resistor pack at location 4D, or grounded through the switch.

3.1.4 If the proper port address and port enable jumpers are installed, the output of 3E-6 will be a high-going pulse when a write to the selected port location is performed. This high-going pulse is applied to the clock input of a 109 flip-flop at 4L, enabling the board to be selected.

3.2 EXTENDED ADDRESSING

The MEMORY BANK is capable of being selected by any one of 256 combinations of the upper address bits (A16-A23). To utilize this feature, select jumper A, which will always enable the comparators. Address lines A16 through A23 are then tied to the inputs of the comparators by utilizing jumpers U, P, K, E, S, M, H, and C. Notice that these jumpers are all aligned on the left side of IC position 3F (center to leftmost pin jumpered). Switch 4E is set up in the same way as for port selection, except that the address being selected corresponds to A16-A23, reading from the top of the switch downward to the S-100 bus.

3.2.1 Jumper W, at the right of the resistor pack located at 3H, must be installed when utilizing the extended address selection mechanism. Jumper W also serves to always enable the board on which it is installed in the port selection mode, regardless of the status of data bits 0-7 written out to the port selected by address switch 4E.

3.2.2 The switch at IC position 1K, in the port selection mode, transmits data bits 0-7 to a NAND gate flip-flop arrangement at 4K. Only *one* of these switches should be on at any one time. Data bit 0 corresponds to the topmost switch position and proceeds downward toward the bottom of the board. A one bit written to the port selected by address switches 4E, in any data bit location where the switch is closed on switch 1K, will select the board.

3.3 SIXTEEN BIT, SEQUENTIAL BYTE, AND CONSECUTIVE BYTE OPTIONS

The MEMORY BANK may be used in a 16-bit wide manner (double-byte transfer), or as sequential 8-bit bytes governed by A0. A third option is operation as a normal 8-bit memory board, referred to as consecutive byte operation. Consecutive byte operation is useful for those who do not wish to install two rows of 4116 memory chips to obtain a 16K bank.

3.3.1 For 16-bit transfers, the status of address line A0 is ignored; two banks (an odd and an even, or a high and low byte bank) are selected, and the transfer occurs in parallel, where Data Out 0-7 corresponds to Data 0-7 and Data In 0-7 corresponds to Data 8-15. The Data In/Data Out pins on the S-100 bus are ganged into one bidirectional data bus.

3.3.2 Bus pin 58 is assigned as sXTRQ*. This is a status signal output from a bus master. When it is in its active true (low) state, it signals a request for a 16-bit data transfer. If jumper TT is closed at 4V, and the board is selected, bus pin 60 will be driven low by the open collector NAND gate at 4U. This is SIXTN*, an acknowledge input to the bus master, which, when it is in its active true (low) state, indicates that a 16-bit transfer is possible. If jumper UU is closed, one side of the NAND gate is grounded, permanently disabling the generation of SIXTN*.

3.3.3 For all 16-bit transfers, the status of A0 is ignored and the board may be considered to be two banks of 16-bit wide memory. (32K x 16). Selection of the upper and lower banks of memory is derived from the status of address line A15.

3.3.4 Sequential byte operation divides the board into an upper and lower bank of a high byte and a low byte. If sXTRQ* is not asserted, SIXTN* obviously will not be asserted either, and the memory transfer operation proceeds by sequential byte transfers. For sequential byte transfers, byte data output from the bus master to the memory device is asserted on the data output lines DO0-DO7. Byte data input from the memory to the bus master is asserted on the

data input lines DI0-DI7. The board switches between its high and low byte banks according to the status of address line A0. If A0 is false (low), the high byte is selected; if A0 is true (high), the low byte bank is selected.

3.3.5 Banks 0 and 2 (lower and upper high-byte banks respectively) are located to the left of the board, with Bank 0 occupying IC positions 1A through 1J (Data Bit 0-7), and Bank 2 occupying IC positions 2A through 2J.

3.3.6 Banks 1 and 3 (lower and upper low-byte banks respectively) are located to the right of the board, with Bank 1 occupying IC positions 1P through 1X and Bank 3 occupying IC positions 2P through 2X (Data Bits 0-7).

3.3.7 There are four groups of jumpers that govern the type of transfers of which the board is capable. For all read operations, jumpers 3/4 and 5/6 (located below IC 3A) are used. Placing jumpers at positions 3 and 5 enables consecutive-byte operation of the board. Jumper position 4 enables the high-byte read output buffer for 16 read or 8 read with A0 false (low). Jumper position 6 enables the low-byte read output buffer for 8 read with A0 true (high).

3.3.8 Jumper positions 13/14 and 15/16 govern low bank write and high bank write. These jumpers are located below IC 4A. For consecutive 8-bit operation, jumpers 14 and 16 are selected. For 16-bit or sequential byte operations, jumpers 13 and 15 are selected. Jumper 13 enables an active low true WRITE* signal to all low-byte RAM chips on a 16 write or an 8 write with A0 true (high). Jumper 15 enables the WRITE* signal to all high-byte RAM chips for a 16 write or an 8 write with A0 false (low). If jumpers 14 and 16 are selected, the board operates in the consecutive byte fashion, with all WRITE* signals to all RAM chips always enabled for any memory write request.

3.3.9 Address lines A0, A14, and A15 also are concerned with governing the type of memory transfer.

3.3.10 Jumper X/Y (below and left of IC 3K) selects between A0 and A14 as an address input to the refresh controller at 4H. For 16-bit or 8-bit sequential operation, select jumper Y, which connects A14 to the refresh controller. For 8-bit consecutive operation, select jumper X, which connects A0 to the refresh controller.

3.3.11 Jumpers 19/20 and 21/22/23 are also concerned with the type of memory transfer. Jumper 19 (center to leftmost pin at the bottom of 3F) ties A17 into the bipolar PROM at 3L. This jumper option is reserved for future expansion of the board using 64K dynamic RAM chips. It should NOT be jumpered for this revision level. Jumper 20 (center to rightmost pin at the bottom of 3F) ties A15 into the PROM, enabling a selection between upper and lower banks of memory.

3.3.12 Jumpers 21/22/23 (located below and between 3N and 3P) are concerned with 16-bit or 8 sequential versus 8 consecutive operation. Jumper position 21 ties A0 into the bipolar PROM. NOTE: Jumper 21 and jumper X are mutually exclusive. If jumper X is selected, jumper 21 must NOT be selected. Jumper 21 is used for 16-bit and 8-bit sequential operations and allows the PROM to select the proper high-byte or low-byte bank. When jumper 21 is selected, *jumper Y must be selected*. Jumper position 22 ties address line A16 into the PROM. As above, this is for future expansion with 64K RAM chips and must NOT be selected on this board revision level. Jumper position 23 ties A14 to the PROM and is used only for 8-bit consecutive operation. If jumper 23 is selected, *jumper X must also be selected*. This will enable the memory board to operate in a linear select scheme, with the first 16K of 8-bit memory located at Bank 0, the second 16K at Bank 1, the third 16K at Bank 2, and the fourth 16K at Bank 3.

3.4 Z80 VS 8080 MODE SELECTION:

It is highly recommended that the MEMORY BANK be used with Z80-type processors in which MRQ* is brought onto the S-100 bus on bus pin 65. This will ensure the most reliable operation of the board.

3.4.1 If the internal board signal MEMREQ is to be derived from MRQ* on bus pin 65, jumper WW should be installed. This establishes a Z80 mode. For 8080 or 8085 processors that are in proper timing, jumper VV may be installed. This enables the board to derive MEMREQ from an OR of sMEMR or MWRITE on bus pins 47 and 68 respectively. WW/VV is located at 4V position.

3.4.2 For those processors providing MRQ* on pin 65, jumper 8/7 selects between an inverted and non-inverted MRQ signal. If your processor puts out an MRQ signal onto the bus which is inverted from the sense in which it is used at pin 19 of the Z80 CPU chip, jumper 8 should be installed. For CPUs which do not invert the MRQ* signal from the Z80 CPU chip, install jumper 7.

3.4.3 The JADE Big Z, and Ithaca Audio CPUs invert MRQ*; therefore jumper 7 should be selected. For TDL, Northstar, and Cromemco CPUs, which provide MRQ* to the bus, select jumper 7. For SD Systems CPU boards, modified as instructed in the appendix of this manual, select jumper 8. For SSM CB2 CPU boards, modified as per the appendix of this manual, also select jumper 8.

3.5 Z80 VS 8080 REFRESH SELECTION:

For all Z80 CPU boards providing the Z80 REFRESH* signal on bus pin 66, install jumper MM (center to lowermost pin of the trio located at the left and below IC 4X). For 8080-type CPU boards, install jumper LL.

3.5.1 Jumper JJ/KK (below and right of 3V) are used only for the 8080 refresh mode (when jumper LL has been selected). Position JJ ties pSTVAL* into IC 3V. Position KK ties MUX into IC 3V.

3.5.2 Jumper 11/12 (below and left of 3V) selects between non-inverting and inverting the signal sM1 on bus pin 44.

3.6 DERIVATION OF ON-BOARD REFRESH REQUEST:

An on-board refresh request is enabled during the following conditions: a DMA operation (signified by pHOLDA on bus pin 26 going true (high), or during the assertion of the active-high signal pWAIT. For 8080-type CPUs, an on-board refresh request must also be made during the time when pHALTA is active.

3.6.1 Jumper ZZ/YY selects between the on-board refresh request being generated by pHOLDA or pHALTA. For normal Z80 operation, jumper YY should be installed, since the REFRESH* signal is generated whenever the Z80 is halted; therefore the memory board will respond to any DMA request by requesting an on-board refresh cycle and will maintain this request as long as pHOLDA is true. For 8080-type operation, select jumper ZZ. Jumper YY/ZZ is located at the bottom of the board, near the S-100 bus connector, to the right of bus pin 50.

3.7 RESPONSE TO RESET, POWER-ON CLEAR, and SLAVECLEAR:

Jumper PP/RR/SS selects between RESET* on bus pin 75, POC* on bus pin 99, and SLAVECLEAR* on bus pin 54. SLAVECLEAR is the preferred IEEE standard signal, and if the CPU provides this signal, jumper PP should be selected. Since most CPUs do not provide this signal, the board should respond to RESET*, and jumper option SS should be selected. (According to IEEE standard, RESET* must be asserted during a power-on clear operation).

3.7.1 The reset signal thus generated is ORed with the DMA or WAIT signal and requests an on-board refresh cycle enable.

3.8 RESPONSE TO GENERATE PREADY:

Any time the memory board is executing an on-board refresh cycle, generated by a reset or DMA request or pWAIT signal, we have a condition which could result in interference with the correct operation of a CPU. Jumper XX asserts pREADY low (false) during this time, placing the CPU in a wait state until the on-board refresh cycle is completed. pREADY is also asserted false during an M1 wait state request if the M1 wait state generator is enabled. If the board is not selected, pREADY will not be asserted false. Jumper XX (at 4V) should always be installed.

3.9 M1 WAIT STATE:

An M1 wait state is generated by IC 3S, which creates one clock cycle of wait time for each M1 cycle. The M1 wait state is enabled by jumper BB, located to the left and below IC 3R. If the jumper is not installed, an M1 wait state will not be generated.

3.10 PRECHARGE EXTENDER OPTION:

The MEMORY BANK contains a precharge extender option for slower RAM chips whose precharge specification does not match that of the Z80 being used. The precharge extender does *not* introduce any wait states; it merely extends the time between a memory read or write and a refresh cycle to match the slower RAM chip requirements.

3.10.1 Jumper DD enables the precharge extender option. Jumper CC enables normal operation of the board without the precharge extender. CC/DD is located below and right of IC 3R.

3.11 PHANTOM RESPONSE:

Jumper HH (below and right of IC 3U) ties the PHANTOM* signal on bus pin 67 onto the memory board. Assertion of PHANTOM* true (low), disables the read circuitry on the board and prevents a bus conflict between a PROM monitor or boot program and the RAM memory.

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3.12 SIXTN* RESPONSE:

Jumper TT/UU determines whether the board will or will not generate SIXTN* in response to sXTRQ*. If the memory board has been set up for 16-bit operation or 8-bit sequential operation, and a 16-bit CPU is being used, jumper TT should be installed. If the board is not selected for 16-bit operation, install jumper UU. TT/UU is located at 4V. Note that for SIXTN* (16-bit grant) to be asserted true, the board must be selected, must be set up for 16-bit operation, and sXTRQ* (16-bit request) must be asserted.

3.13 JUMPER 17/18:

Jumper 17/18 (below the switch at IC position 1K) is provided for future expansion to 64K RAM chips. For this board revision level, jumper 17 must be installed.

3.14 PHI 2 (MASTER BUS CLOCK) SELECT:

Jumpers 1/2 (located between 2T and 3T) selects either an inverted 02 or a non-inverted 02 clock signal. The clock signal provided from the output of 3T-12 must be *inverted* in phase with the Z80 CPU 02 clock signal. For those CPUs that invert the 02 signal provided at the bus on pin 24 from that supplied to the Z80 on the CPU board, install jumper 2. For those CPUs providing an in-phase 02 signal on the bus, install jumper 1. SD Systems boards invert the clock signal.

3.15 SUMMARY OF JUMPER OPTIONS:

G, I, O, Q, and Z are not used.

AA, EE, FF, CC, NN, OO, and QQ are not used.

JUMPER USE & LOCATION

A/B	extended address mode/port select mode (right bottom 3C)
C/D	A23/A7 to comparator - use A7 for port mode
E/F	A19/A3 to comparator - use A3 for port mode
H/J	A22/A6 to comparator - use A6 for port mode
K/L	A18/A2 to comparator - use A2 for port mode
M/N	A21/A5 to comparator - use A5 for port mode
P/R	A17/A1 to comparator - use A1 for port mode
S/T	A20/A4 to comparator - use A4 for port mode
U/V	A16/A0 to comparator - use A0 for port mode
W	board always selected
X/Y	A0/A14 routed to memory chips through dynamic memory controller
BB	enables M1 wait state generator
CC/DD	disable/enable precharge extender option
HH	enable PHANTOM* from bus pin 67

JJ/KK sM1/MUX conditions 8080 refresh enable (use only for 8080-type CPUs)

LL/MM 8080 refresh/Z80 refresh

PP/RR/SS respond to SLAVECLEAR*, POC* or RESET* for board reset

TT/UU BS NANDs with 16RQ* for SIXTN* response/always disable 16 grant

VV/WW 8080/Z80 MEMORY REQUEST mode

XX enable pREADY to bus pin 72

YY/ZZ use HOLDA/HALTA for on-board refresh (HOLDA for DMA and Z80)

27 1/2 invert/noninvert 02 clock

3/4 8 consecutive/16 or 8 sequential (read)

5/6 8 consecutive/16 or 8 sequential (read)

7/8 invert/noninvert MRQ* (NEED MRQ)

9/10 disable/enable forced phantom to PROM (see theory of operation)

34 11/12 noninvert/invert sM1

13/14 16 or 8 sequential/8 consecutive (write)

15/16 16 or 8 sequential/8 consecutive (write)

1K 17/18 16K/64K RAM chips (17 for this level revision)

3F 19/20 A17/A15 conditions PROM (19 for this level revision)

34 21/22/23 A0/A16/A14 conditions PROM (do not use 22)

Switch 1K (used to select which of 8 data bits will select the board in port mode)

Switch 4B (used to select port address or one of 256 extended address locations)

Switch 3M (positions 1-6)

1-closed, enables bank 0, open disables bank 0

2-closed, enables bank 1, open disables bank 1

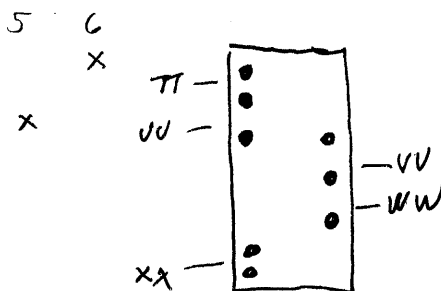
3-closed, enables bank 2, open disables bank 2

4-closed, enables bank 3, open disables bank 3

5-6 decoded as shown in Theory of Operation Section (Partial Bank Disable --

Derived Phantom)

	6
	DEFEAT
DISABLE	E000 - FFFF
DISABLE	F000 - FFFF



SECTION FOUR

BOARD ASSEMBLY INSTRUCTIONS

The JADE MEMORY BANK Dynamic RAM Memory Board is intended for those people who have had some prior experience with kit building and digital electronics. If you do not fall into this category, it is highly recommended that you find an experienced person to help you with the assembly and check-out of the board.

Although there is nothing sacred in the suggested steps that follow, if you will follow them step-by-step you should find your task much easier. We suggest that you start at a time when you will be able to complete the board assembly. It will also help in your construction task if you will mark the boxes as you complete each step.

- 1. Make sure you have the tools you will need to assemble this kit. For the MEMORY BANK you will need the following: (a) a soldering iron (20 watts maximum); (b) *rosin core* solder (preferably 63/37); (c) diagonal cutters (preferably the kind angled for flush cutting); (d) a small magnifying glass; (e) a small thin-bladed screwdriver; (f) a lead former; (g) a pair of needle-nose pliers.
- 2. Check the parts received against the parts list very carefully. Take special care to properly identify look-alike parts; i.e., resistors, capacitors and diodes. If anything is missing from your kit, please call JADE's Customer Service Department and report the shortage immediately. Some parts may be substituted for those called for in the parts list; for instance, the values of pullup resistor packs may vary from those specified and there may be slight variations in the values of capacitors and resistors. Use reasonable judgement before calling JADE, please.
- 3. Read the section of this manual titled "Construction and Soldering Tips." If you have trouble identifying any of the parts, the section titled "Parts Identification" should help you. Do this *now* before you proceed any further.

CAUTION

ALWAYS USE EYE PROTECTION WHILE SOLDERING OR CUTTING LEADS.

- 4. Install 14-pin sockets at IC locations 3A, 3B, 3C, 3H, 3K, 3P, 3R, 3S, 3T, 3U, 3V, 3W, 3X, 4A, 4B, 4C, 4K, 4M, 4N, 4P, 4R, 4T, 4U, and 4W. Do NOT install a 14-pin socket at 4X. Do NOT solder these sockets in yet.
- 5. Install 16-pin sockets at IC locations 1A, 1B, 1C, 1D, 1E, 1F, 1H, 1J, 1P, 1R, 1S, 1T, 1U, 1V, 1W, 1X, 2A, 2B, 2C, 2D, 2E, 2F, 2H, 2J, 2M, 2N, 2P, 2R, 2S, 2T, 2U, 2V, 2W, 2X, 3D, 3E, 3L, 3N, 4D, 4L, and 4S. Do NOT solder them in yet.
- 6. Install 20-pin sockets at 1L, 1M, 1N, 2K, 2L, and 4F. Do NOT solder them in yet.
- 7. Install a 28-pin socket at 4H. Do NOT solder it in yet.
- 8. Make sure that you have oriented the sockets correctly. Pin 1 of the sockets is always oriented toward the *top* of the board. The only exception to this is IC location 3H, where pin 1 is oriented toward the left of the board. See "Parts Identification" section for help in determining which is pin 1 of the various sockets.

- ✓ 9. A handy trick to help you construct your board is to insert all of the sockets into the board first, then place the flat styrofoam cover you received with your kit firmly against the top of the board, covering the sockets. Press it down tight. Now, very carefully, turn the board over, holding the flat styrofoam piece tightly against the board. The ICs should now be on the bottom. Now solder alternating corner pins (only TWO) of the IC sockets to hold them in place temporarily (pins 8 and 16 on a 16-pin socket, for instance).
- ✓ 10. When you have tack soldered the corner pins of the sockets, turn the board over, removing the styrofoam, and very carefully inspect the board to make sure that all the IC socket are down flat against the board. If you find any that are cocked, melt the solder joints at the corners of the socket, while pressing press it down onto the board.
- ✓ 11. Inspect the board to make absolutely certain that *all* the socket pins are coming through the holes correctly. Now is the time to remove any sockets that have bent-under pins. IC sockets are very difficult to remove once they are fully soldered onto the board. For soldering hints, turn to Appendix B of this manual. Solder all IC socket pins on the board.
- ✓ 12. Install a 3-pin header at 17/18 (immediately below 1K).
- ✓ 13. Install a 3-pin header at 1/2 (immediately below 2T).
- ✓ 14. Install a 3-pin header at 3/4 (below and left of 3A).
- ✓ 15. Install a 3-pin header at 5/6 (below and right of 3A).
- ✓ 16. Install a 2-pin header at W (to the right of 3H).
- ✓ 17. Install a 3-pin header at X/Y (below and left of 3K).
- ✓ 18. Install a 3-pin header at 9/10 (below and right of 3M).
- ✓ 19. Install a 2-pin header at BB (below and left of 3R).
- ✓ 20. Install a 3-pin header at CC/DD (below and right of 3R).
- ✓ 21. Install a 2-pin header at HH (below and right of 3U).
- ✓ 22. Install a 3-pin header at 11/12 (below and left of 3V).
- ✓ 23. Install a 3-pin header at JJ/KK (below and right of 3V).
- ✓ 24. Install a 3-pin header at LL/MM (below and left of 3X).
- ✓ 25. Install a 3-pin header at 13/14 (below and left of 4A).
- ✓ 26. Install a 3-pin header at 15/16 (below and center of 4A).
- ✓ 27. Install a 3-pin header at YY/ZZ (above and right of bus pin 50).
- ✓ 28. Install a 3-pin header at TT/UU (left side of box at 4V, place in top 3 holes).
- ✓ 29. Install a 3-pin header at YY/ZZ (right side of box at 4V, center 3 holes).
- ✓ 30. Install a 2-pin header at XX (left side of box at 4V, bottom 2 holes).
- ✓ 31. Install a double-row header 9 pins long at the right side of 3F for jumper options D, F, J, L, N, R, T, N, and 20.
- ✓ 32. Install a single-row header 9 pins long at the left side of 3F for jumper options C, E, H, K, M, P, S, U, and 19. (Make sure this header row is straight and properly aligned with the center row or you may have trouble installing the jumpers later).

- ✓ 33. Install a double-row header 3 pins long at PP/RR/SS (below 4C).
- ✓ 34. Install a double-row header 3 pins long at 21/22/23 (below and between 3N and 3P).
- ✓ 35. Install a 3-pin header at 7/8 (below and left of 3C).
- ✓ 36. Install a 3-pin header at A/B (below and right of 3C).
- ✓ 37. Install a 1N751 zener diode at CR1 (top left of board).
OBSERVE POLARITY - BANDED SIDE SHOULD GO AS MARKED.
- ✓ 38. Install a 1N914 signal diode at CR3 (immediately below 3L).
OBSERVE POLARITY - BANDED SIDE SHOULD GO AS MARKED.
- ✓ 39. Install a 1N914 signal diode at CR4 (just above bus pin 1).
OBSERVE POLARITY - BANDED SIDE SHOULD GO AS MARKED.
- ✓ 40. Install C1, C2, C3, C4, and C5 10 microfarad 35 volt tantalum capacitors.
OBSERVE POLARITY - BANDED SIDE SHOULD GO AS MARKED.
- ✓ 41. Install C6, a 47 picofarad capacitor (below 4B). (Use the holes inside the marked oval).
- ✓ 42. Install C7, a 1 picofarad tantalum capacitor (below C6). The positive side of the capacitor should go toward the right side of the board.
- ✓ 43. Install C8, a 47 picofarad capacitor (below 4X).
- ✓ 44. Install C9 through C40, 0.1 microfarad monolithics at the positions marked on the board.
- ✓ 45. Install R1, a 1K resistor (marked brown-black-red) to the right of CR1.
- ✓ 46. Install R2, a 470 ohm resistor (marked yellow-violet-brown) to the left of CR1.
- ✓ 47. Install R3, a 4.7K resistor (marked yellow-violet-red) below 3S and 3T.
- ✓ 48. Install R4, a 4.7K resistor (marked yellow-violet-red) below 1J.
- ✓ 49. Install R5, a 200 ohm resistor (marked red-black-brown) below 4C.
- ✓ 50. Install R6, a 1K resistor (marked brown-black-red) below R5.
- ✓ 51. R7 is not used. Install R8, a 22 ohm resistor (marked red-red-black) to the right of 4V.
- ✓ 52. Install R9, a 200 ohm resistor (marked red-black-brown) below 4X.
- ✓ 53. Install CR2, a red LED, just above and right of 1A. OBSERVE POLARITY - flat side of LED goes to the right.
- ✓ 54. Install VR1, a 7805 TO-220 regulator at left center of the board. Use the heat sink, silicon grease, and one of the two sets of hardware supplied (#6 bolt, nut and lockwasher).
- ✓ 55. Install VR2, a 7812 TO-220 regulator. Use heat sink and the remaining hardware supplied.
- ✓ 56. Install an 8-position DIP switch at 1K. Position 1 faces top of board.
- ✓ 57. Install an 8-position DIP switch at 4E. Position 1 faces top of board.
- ✓ 58. Install a 6-position DIP switch at 3M. Position 1 faces top of board.

59. Do NOT install any ICs at this time.

We will now proceed to a functional checkout of the MEMORY BANK.

WARNING!

DO NOT INSTALL OR REMOVE THIS BOARD WITH THE POWER ON. PERMANENT DAMAGE TO THIS AND OTHER BOARDS IN THE SYSTEM COULD OCCUR.

The functional checkout procedure that follows does not examine or verify every signal or feature of the MEMORY BANK, but it does verify proper operation of the on-board voltage regulators and the board selection mechanism.

60. With an ohmmeter, measure the resistance between ground (pin 20, 50, 53, 70 or 100 of the S-100 edge connector) and pin 1 of the edge connector. The reading should be 20 ohms or more. If you cannot verify a resistance of 20 ohms or greater, check your board for solder bridges or shorts.

61. Perform the above step for the +12V line. Measure between ground and pin 2 of the S-100 edge connector. Verify a resistance of 20 ohms or greater. If less, check for shorts.

62. Apply power to the board by plugging it into an extender card in the system or by connecting it to a power supply. With a voltmeter, measure the output of the +5V regulator. The output pin will be on the right side of the regulator as it faces you. Be careful not to short your voltmeter lead to the center pin, as this can destroy the regulator.

The voltage obtained from the output of the regulator should be between +4.8V and +5.2V. If the regulator doesn't meet this specification, remove the board and check it again for shorts or errors. Check for tantalum capacitors that have been installed with the wrong polarity.

63. Perform step 62 for the +12V regulator. Verify a voltage reading between +11.8V and +12.2V. If the voltage is not within these limits, check for shorts or errors on the board such as improperly installed tantalum capacitors.

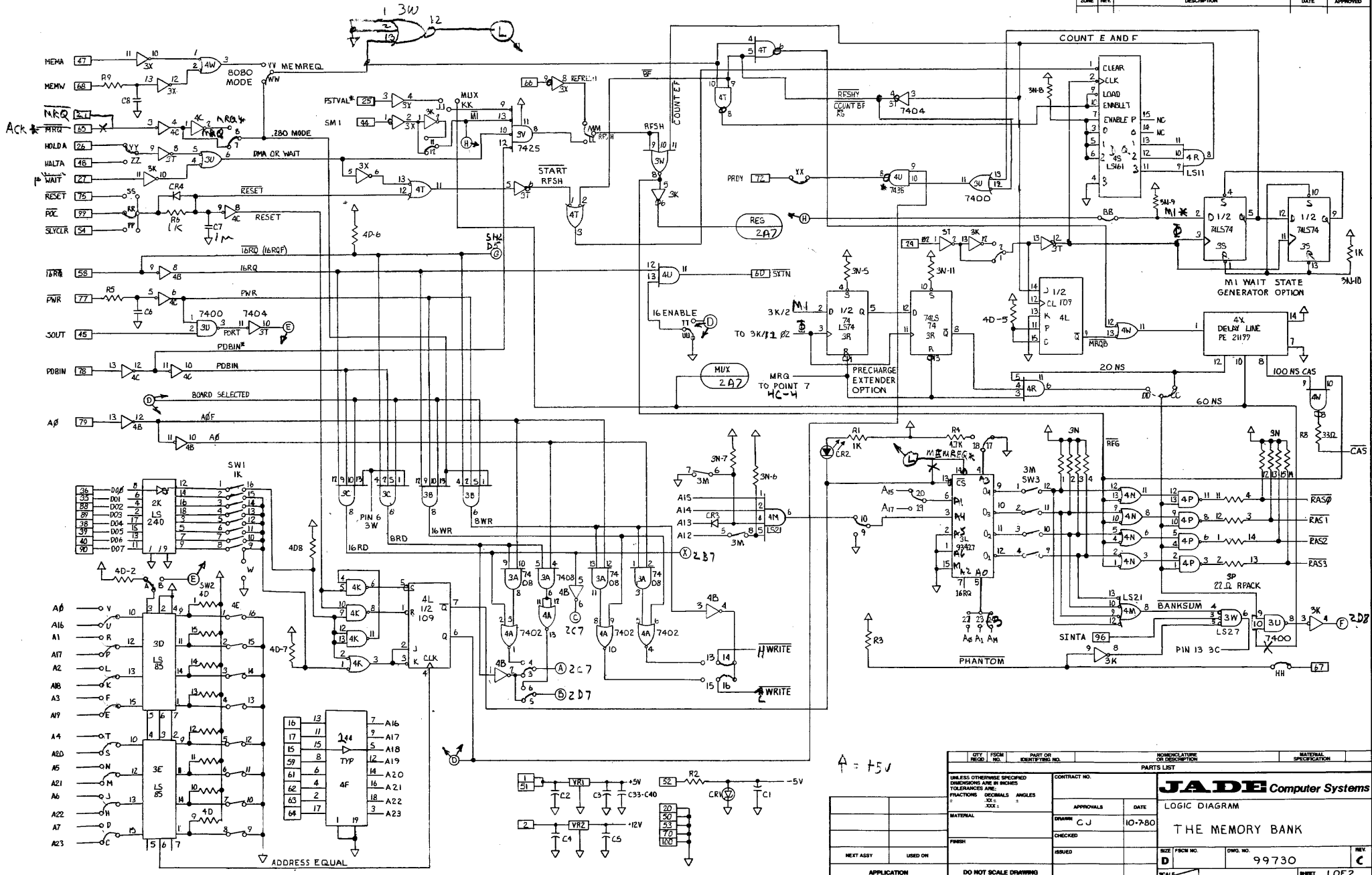
WARNING!

TANTALUM CAPACITORS WHICH HAVE BEEN INSTALLED WITH THE INCORRECT POLARITY HAVE BEEN KNOWN TO EXPLODE. THIS COULD RESULT IN POSSIBLE INJURY TO THE EYES, FACE OR HANDS FROM HOT FLYING DEBRIS. KEEP YOUR HANDS AND FACE CLEAR OF THE BOARD DURING THE ABOVE TESTS.

64. Check for -5V either at pin 1 of the RAM sockets or at the junction of CR1 and R2. Specifications for this voltage are -4.8V to -5.2V. If you do not obtain this voltage, check for shorts on the -5V lines.

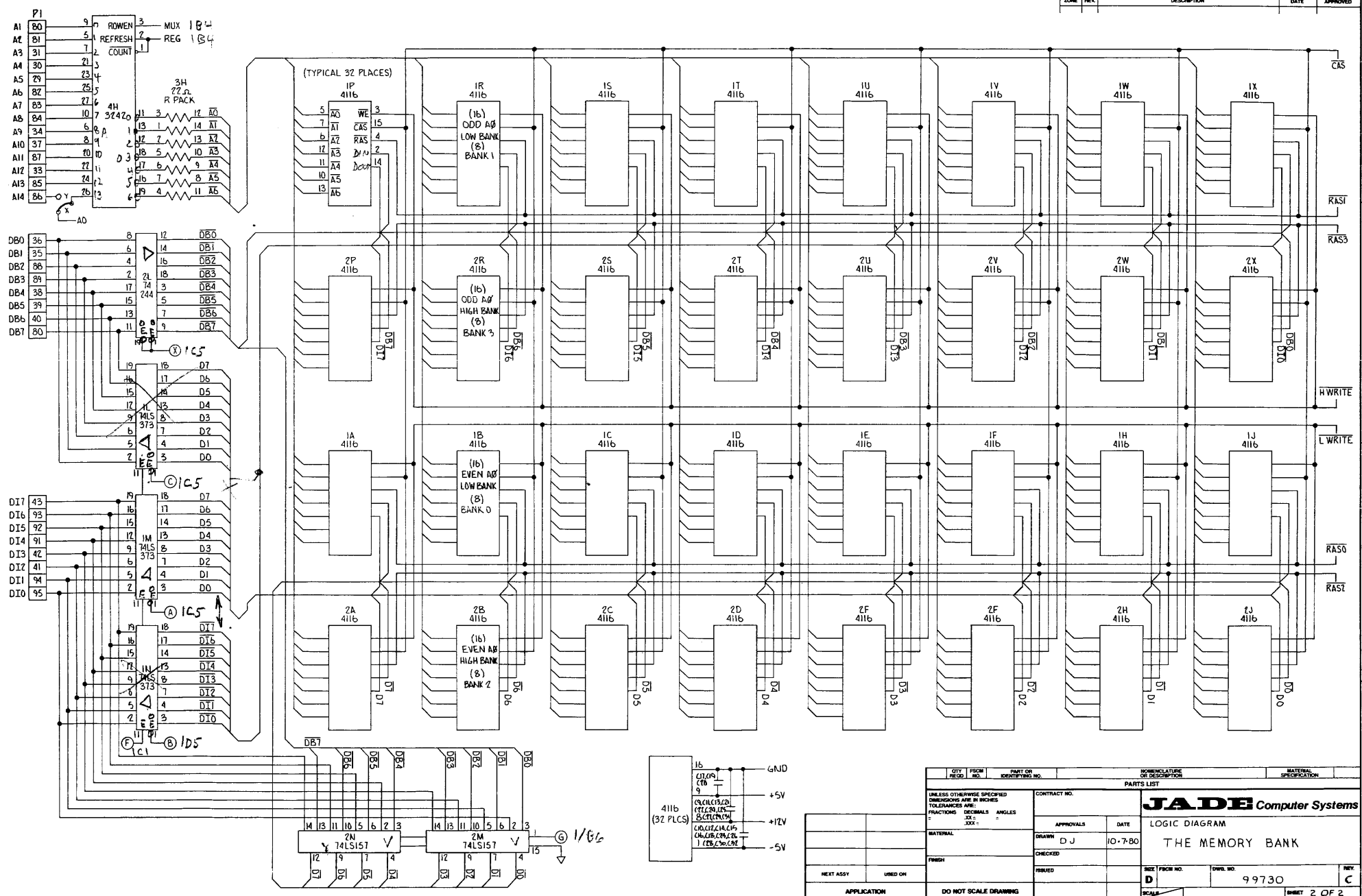
65. If the voltages check out within specification, install all ICs with the exception of the RAM chips. Observe proper polarity. All ICs are oriented with pin 1 toward the top of the board. Use the assembly drawing to determine proper IC placement on the board. Verify proper placement and proper orientation of the ICs before applying power to the board. Be especially careful of the delay line orientation.

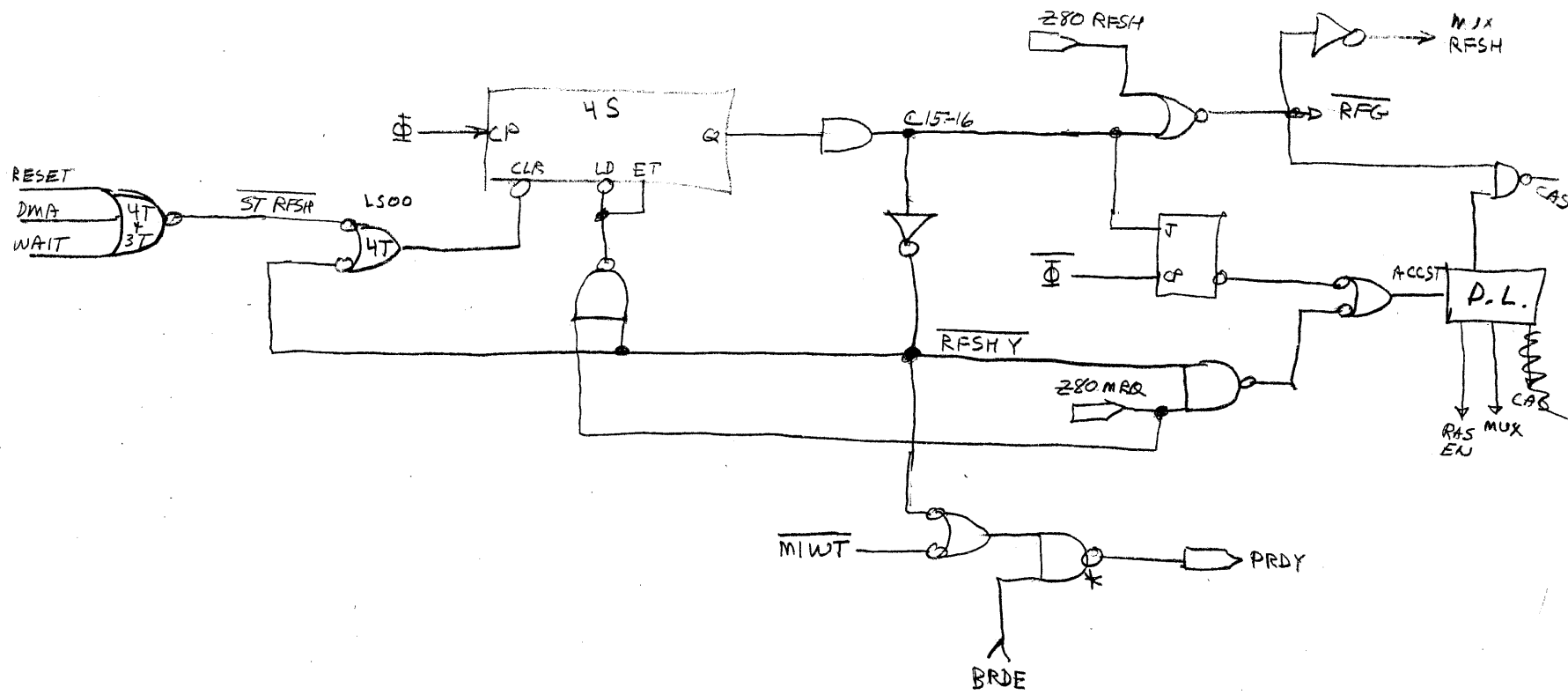
**SECTION FIVE
SCHEMATIC**



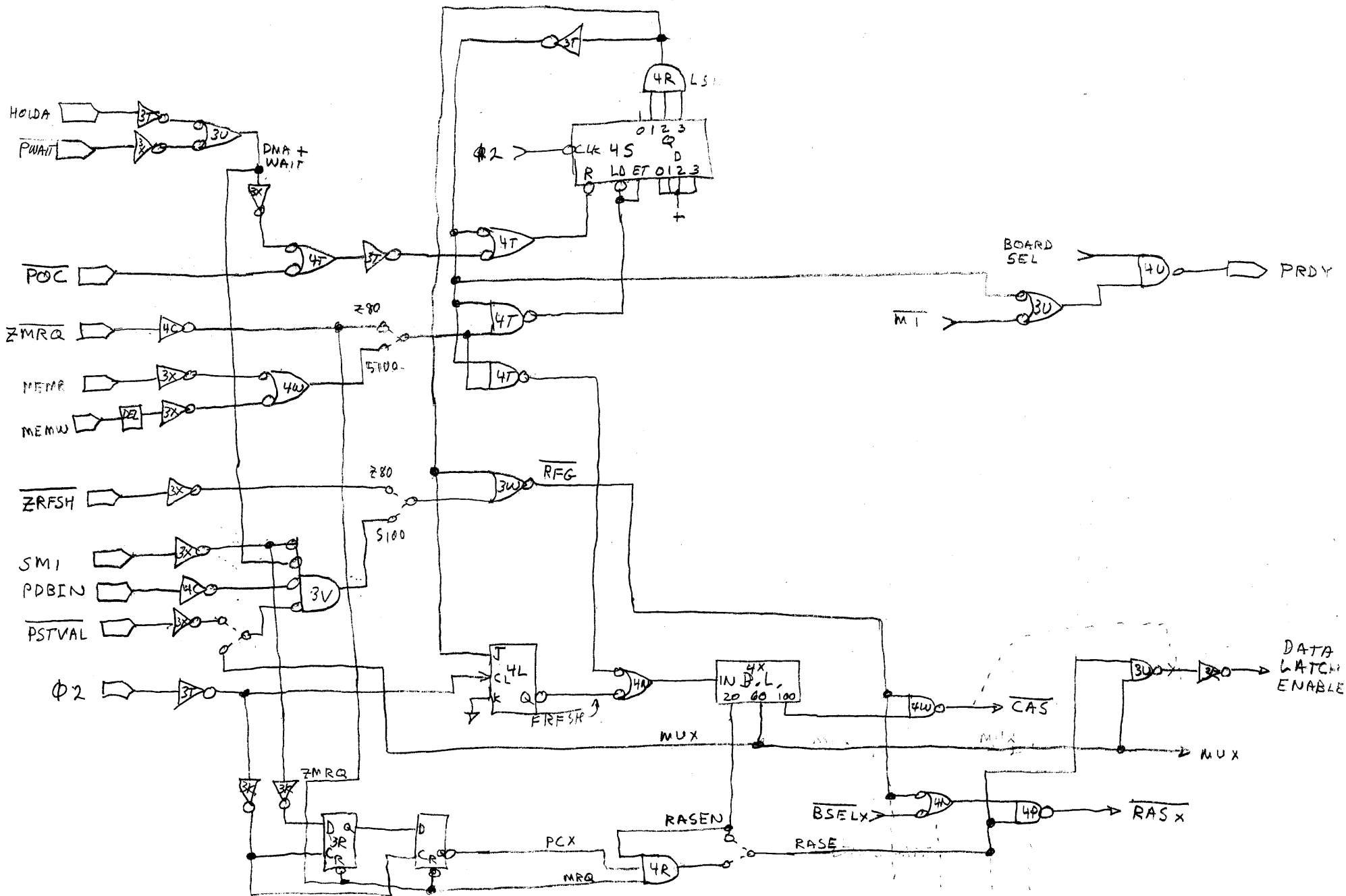
A = +5V

CITY FROM		PART OR IDENTIFICATION NO.		NOMENCLATURE OR DESCRIPTION		MATERIAL SPECIFICATION	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS DECIMALS ANGLES				CONTRACT NO.			
MATERIAL				APPROVALS		DATE	
FINISH				DRAWN		10-7-80	
NEXT ASSY				CHECKED		LOGIC DIAGRAM	
APPLICATION				ISSUED		THE MEMORY BANK	
DO NOT SCALE DRAWING		SIZE FROM NO.		DWG. NO.		REV.	
		D		99730		C	
		SCALE		SHEET		1 OF 2	





REFRESH ENABLE



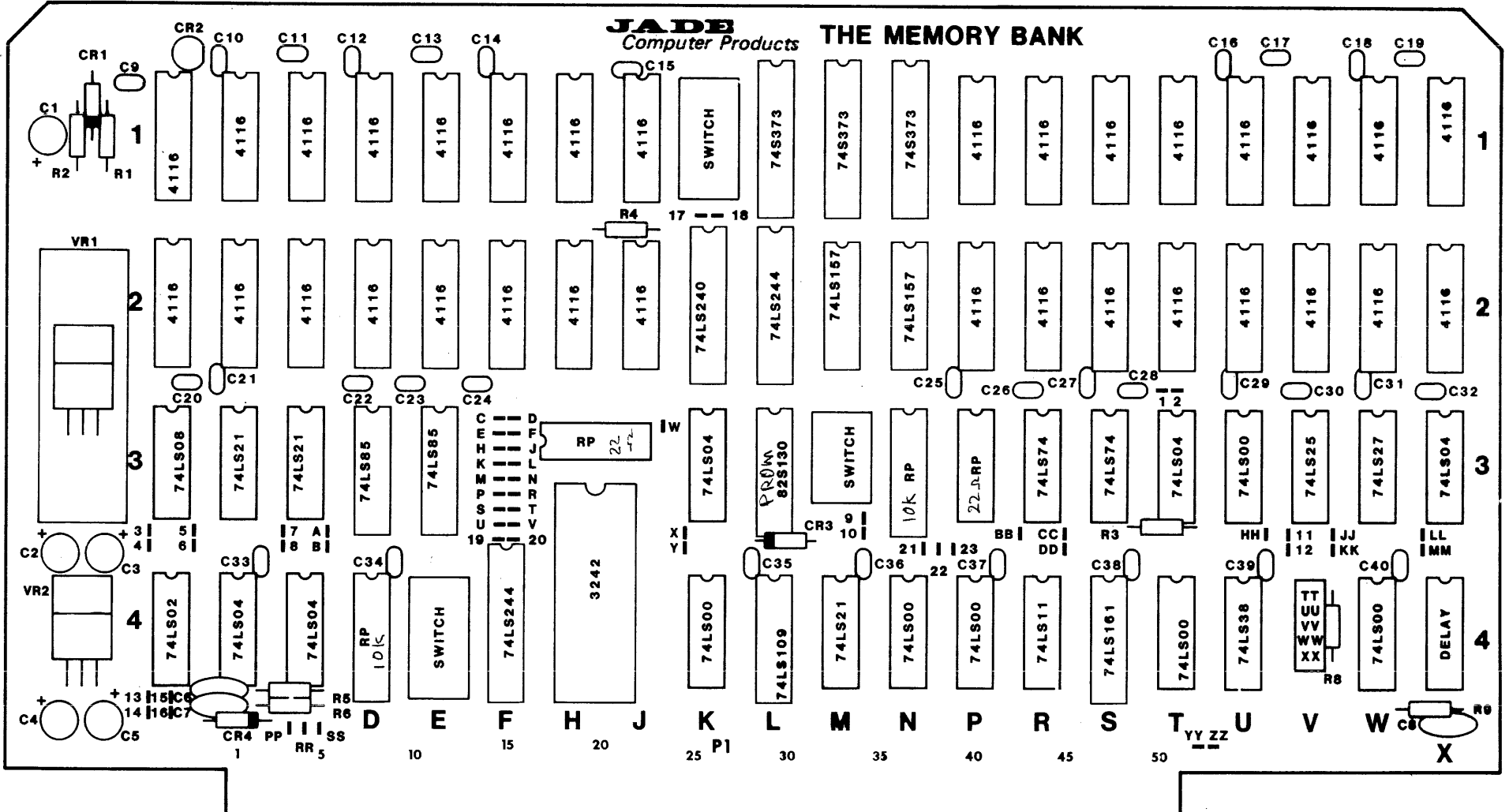
**SECTION SIX
ASSEMBLY DRAWING**

7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0

50.0K
φ
2

BANK
1
3

JADE Computer Products THE MEMORY BANK



JUMPER 11 (below 3V) make
a good jumper wire

SECTION SEVEN PARTS LIST

Item	Qty	Description
1	1	Manual, The Memory Bank
2	1	PC Board Assembly, The Memory Bank
3	6	74LS00 Quad 2-input NAND (3U, 4K, 4N, 4P, 4T, 4W)
4	1	74LS02 Quad 2-input NOR (4A)
5	5	74LS04 Hex Inverter (3K, 3T, 3X, 4B, 4C)
6	1	74LS08 Quad 2-input AND (3A)
7	1	74LS11 Triple 3-input AND (4R)
8	3	74LS21 Dual 4-input AND (3B, 3C, 4N)
9	1	74LS25 Dual 4-input NOR (3V)
10	1	74LS27 Triple 3-input NOR (3W)
11	1	74LS38 Quad 2-input OC NAND (4U)
12	2	74LS74 Dual D Flip-flop (3R, 3S)
13	2	74LS85 4-bit Magnitude Comparator (3D, 3E)
14	1	74LS109 Dual JK Flip-flop (4L)
15	2	74LS157 Quad 2-to-1 Multiplexer (2M, 2N)
16	1	74LS161 Binary Counter (4S)
17	1	74LS240 Inverting Octal Buffer (2K)
18	2	74LS244 Non-inverting Octal Buffer (2L, 4F)
19	3	74LS373 Octal D-type Latch (1L, 1M, 1N)
20	1	3242 Dynamic RAM Controller (4H)
21	1	93427 Custom PROM (3L)
22	1	TTL-DM100 Delay Line (for up to 4 MHz)
22a	1	TTL-DM50 Delay Line (for above 4 MHz)
23	1	LM340T5/7805 +5V regulator (TO-220) (VR1)
24	1	LM340T12/7812 +12V regulator (TO-220) (VR2)
25	25	Socket, 14-pin low profile
26	41	Socket, 16-pin low profile
27	6	Socket, 20-pin low profile
28	1	Socket, 28-pin low profile
29	17	3-pin single row header
30	4	2-pin single row header
31	1	9-pin single row header
32	1	9-pin double row header
33	2	3-pin double row header
34	5	10 microfarad 35V tantalum capacitor (C1-C5)
35	2	47 picofarad silver mica capacitor (C6, C8)
36	1	1 microfarad 25V tantalum capacitor (C7)
37	32	0.1 microfarad monolithic capacitor (C9-C40)
38	2	1K ¼ watt 5% resistor (R1, R6)

39	1	470 ohm ¼ watt 5% resistor (R2)
40	2	4.7K ¼ watt 5% resistor (R3, R4)
41	2	200 ohm ¼ watt 5% resistor (R5, R9)
42	1	22 ohm ¼ watt 5% resistor (R8)
43	1	LED red
44	2	8 position DIP switches (1K, 4E)
45	1	6 position DIP switch (3M)
46	2	Resistor Pack, 14-pin 7 resistor, 22 ohms (3H, 3P)
47	2	Resistor Pack, 16-pin 15 resistor, 10K (3N, 4D)
48	2	Screws, 6-32 x 3/8"
49	2	Nuts, Hex #6
50	2	Lock Washer, #6
51	2	Card Ejector Assembly
52	1	Heat Sink, TO-220 small, use at VR2
53	1	Heat Sink, large, use at VR1
54	32	Shorting Jumpers
55	8-32	4116 RAM (8 per 16K) optional
56	1	1N751 5.1V Zener diode (CR1)
57	2	1N914 Signal diode (CR3, CR4)

Last C Number is C40

Last R Number is R9 (R7 is not used)

Last V Number is VR2

Last CR Number is CR4

SECTION EIGHT

CONSTRUCTION AND SOLDERING TIPS

Choose a well-lighted work space with enough room to place your tools, parts, and instructions where they will be easy to reach. If you have two light sources that can be adjusted, this will help eliminate shadows which interfere with seeing your work.

Familiarize yourself with all of the general operations to be performed. It might even help to do a dry run of sorts, getting everything together and following the procedures.

The tools you will need for each individual kit will be listed in the assembly instructions. A basic set would include: a low wattage soldering iron (20 watts or less - remember, you're working with microcomputers, not building bridges) - and with a 650-degree tip if you can get one; a holder which will keep you from accidentally touching the hot tip; a pair of wire cutters (also called dykes or side cutters, preferably beveled so that you can cut close to the board); a pair of needle-nose pliers; a damp sponge or a moistened cloth to use to wipe the soldering iron's tip; a magnifying glass to examine details, and a lead former to bend leads. The latter is available at most electronics parts houses in an inexpensive plastic version, or you can make your own out of wood. If you're into building lots of electronic kits, they're worth their weight in gold.

Arrange your tools in order of their frequency of use and orient them so they're easy to reach. Make sure that they are clean and in good working order.

Keep your work area clean and uncluttered.

Make sure that your chair is set at a proper height and is comfortable for your work station.

Try to keep food and drink away from your area. Always strive for neatness and uniformity. This means removing bits and pieces of scrap wire and solder blobs, as you work, so they don't become buried in your board and short something out. Inevitably, according to Murphy, they will sneak underneath IC sockets and if there's a place that's hardest to get to to fix, that's exactly where they'll lodge.

Soldering can cause several different kinds of problems in kit building. Heat can damage the PC board and the components, especially diodes and transistors, or create unwanted electrical connections. Most problems can be eliminated by using the right soldering iron (and the right solder - *rosin* core, *not* acid core), and by developing an efficient technique.

Parts are inserted on the component (front) side of the board. Soldering is done on the back side. This is always a rule, unless you are specifically directed otherwise in the assembly instructions.

If you plan on building many kits (and one memory board can be many kits), spend the few extra dollars to buy yourself a quality temperature-controlled soldering station. Spending the \$30 can save you from ruining a \$200 kit.

Use only *rosin core* solder when constructing electronic kits. Never, never, not *ever* use acid core - that's only for pipes and sheet metal. A solder with a high ratio of tin to lead is important, too. 60/40 is good - but 63/37 is better, and the difference will amaze you.

Make sure you have a well-tinned tip. A tip is well tinned when it has a thin film of solder coating on the surface of the iron. Oxide and resin build up as you work it and the bright shiny look will disappear. That's what the wet sponge or moistened cloth is for. The iron should be wiped clean about every ten connections or so to get rid of that oxide and resin.

Some DON'Ts: DON'T have any unnecessary items at your work station. DON'T use worn or damaged tools. NEVER solder equipment that is plugged in. DON'T use unknown cleaning solutions. DON'T pull on a solder joint to see if it's good. NEVER flip excess solder from the tip of your iron - use the sponge or cloth. NEVER put solder on your iron and then transfer it to a cold joint.

Heat both the component wire and the solder pad with the tip of the iron until it looks wet or liquid. Then touch the solder to the junction between the iron, the pad, and the wire. When the solder melts and flows onto the connection, quickly remove the iron's tip. Allow the joint to cool without moving any of the components. A good joint will be smooth and bright. A bad one will be a dull lead-looking glob of solder.

Avoid using too much solder! From our experience at repairing customer's boards, this is the sin most often committed. If little drops of solder appear on the opposite side of the board, you're either using too much solder or too much heat. Be extremely careful when you solder adjacent pads because the heat may cause the solder to flow between them, making a solder "bridge". Bridges are only good for crossing rivers - they don't belong on electrical boards. They make an unwanted electrical connection.

If you do find a bridge, the best way to remove it is to clean your iron on the dampened sponge or cloth and then touch the bridge with the clean hot tip until it wets and sticks to the tip. Then get rid of it.

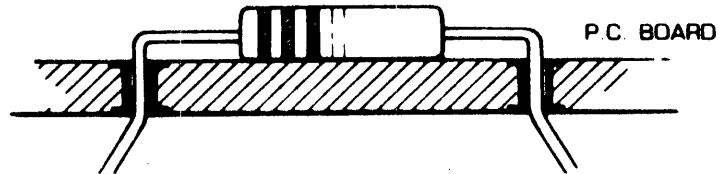
Excess wire can be removed with diagonal cutters. WAIT until the joint has cooled. Beware of flying pieces of wire. *Always use eye protection when soldering or cutting wire!*

After you're all done, use solvent to remove the flux. Flux is that brown stuff that gets on the board near your soldering joints, and it is formed of burned resin. Not only does it *look* bad, it can cause electrical headaches as well, especially in higher-frequency circuits. Not only this, but it makes it much more difficult to find bridges and shorting flakes of solder, since the rosin hides the solder under an effective coverup. Leave coverups to the politicians; clean your board.

JADE technical support people have found that a board works about like it looks. If it's been put together with care and good workmanship, it will work just fine.

SECTION NINE COMPONENT INSTALLATION

Install all components in their proper location, and if polarity is important, observe the proper markings. The component should be installed flush with the circuit board, unless clearance is specifically called for in the instructions. This clearance is usually required for hot components that might burn or discolor the printed circuit board.



The lead should have a discernable length extending straight from the body of the component before beginning the bend. The component body shall not be damaged nor the body-to-lead seal be damaged by the forming operation. The component should be centered between the bends, although this is not a requirement. Where feasible, all forming should be done so that the part number is visible when installed in the printed circuit board.

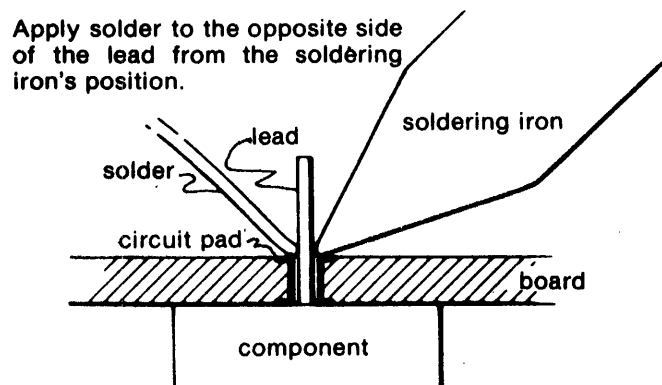
Soldering techniques probably are the hardest to master of any electronic assembly technique. If you have never soldered at all, it is probably best that you practice on some old scrap printed circuit board available at most electronic parts houses and surplus shops.

For electronic assembly, always use rosin core solder, not acid core solder. Acid core solder will corrode, and it's impossible to stop the corrosion once it's begun. It will eventually ruin the printed circuit board.

A soldering iron of small wattage (preferably 27 to 40 watts absolute maximum), should be used. Always keep the tip clean and free from dross (oxidized solder) by wiping on a moistened sponge or folded up Kleenex (moistened). Use small solder with a 60/40 ratio (60% tin and 40% lead).

When ready to solder a joint, apply heat to the joint first, then apply the solder to the opposite side of the joint from the iron (see figure B-1). Then remove the solder and finally the soldering iron. A good solder joint has an even flow of solder over the entire joint. A good joint will have a bright glistening look. A bad solder joint, commonly call a "cold" solder joint, will have a dull appearance. Also, do not move the part or the lead while the solder is cooling or a cold or fractured solder joint will result (see figure B2a-c).

Figure B-1 Illustrates proper soldering techniques



The fillet is well-formed. It is concave and well above the surface of the pad.

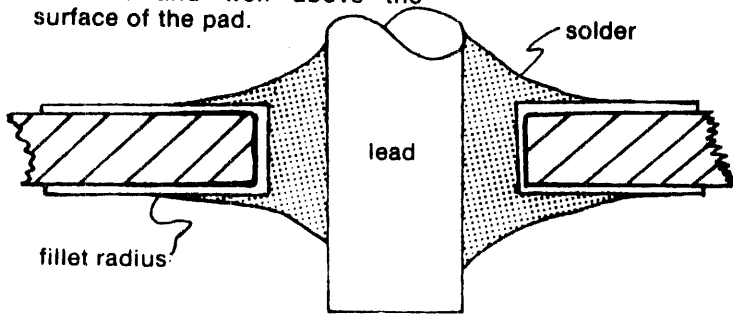


Figure B-2 (a) illustrates an Optimum Solder Joint

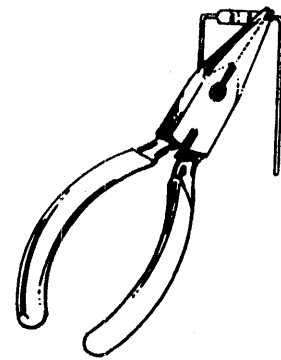


Figure B-3 illustrates lead forming techniques.

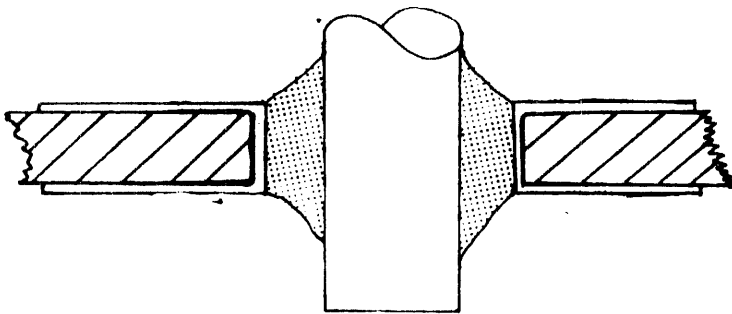


Figure B-2 (b) illustrates the minimum solder acceptable

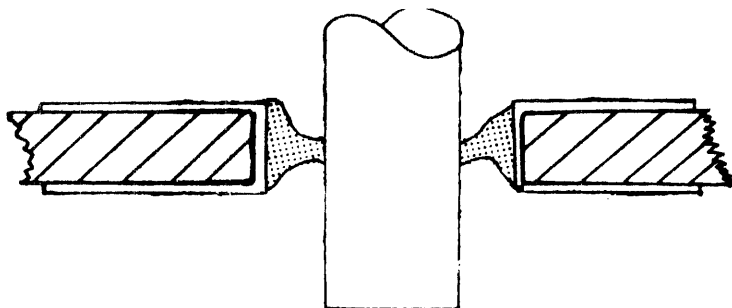
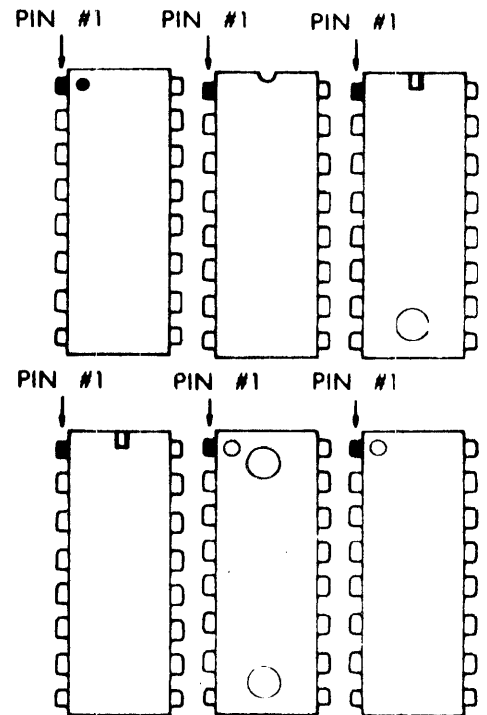


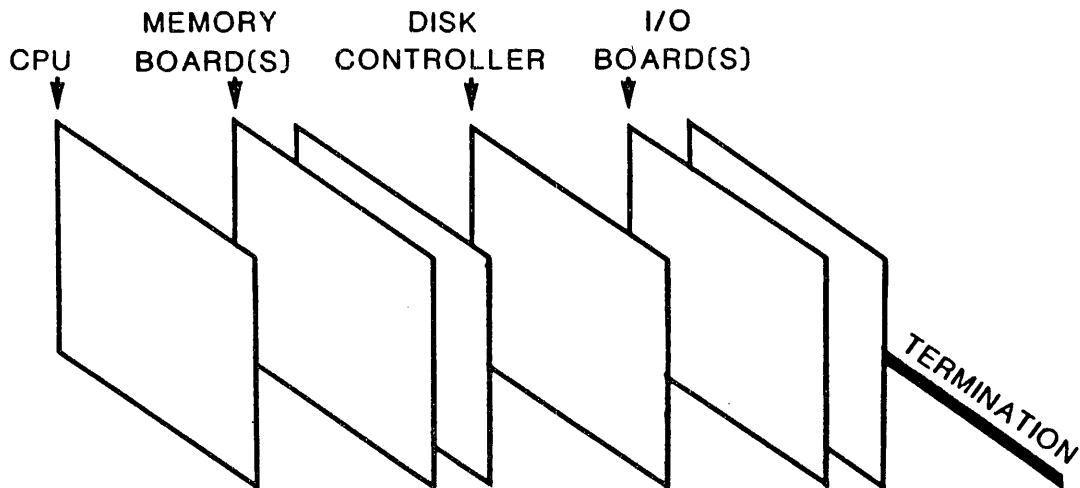
Figure B-2 (c) illustrates insufficient solder.



A NOTE ON S-100 BOARD PLACEMENT

Your S-100 system's performance can be affected by placement of the boards on the system bus, especially at clock speeds in excess of 2 MHz. To achieve the maximum reliability from your system, you should adhere to the following simple rules regarding the placement of individual boards on the bus:

1. Since most of the bus activity is between the CPU and memory, locate memory cards as close as possible to the CPU.
2. On a terminated bus, the CPU should be the furthest board from the bus termination, with all other board located between the CPU and the termination.



EXAMPLE OF BOARD PLACEMENT

PROM DATA
256 x 4

ADDR	DATA
00	7
	B
	D
	E
	5
	5
	A
	A
08	F
:	:
:	:
FF	F

7	6	5	4	3	2	1	0
GND	GND	GND	DISABLE	GND	16RQ	A15	A14
0	0	0	0	0	0	0	0
				0			1
				0	1	0	
				0	1	1	
				0	1	0	0
				0	1	0	1
				0	1	1	0
				0	1	1	1

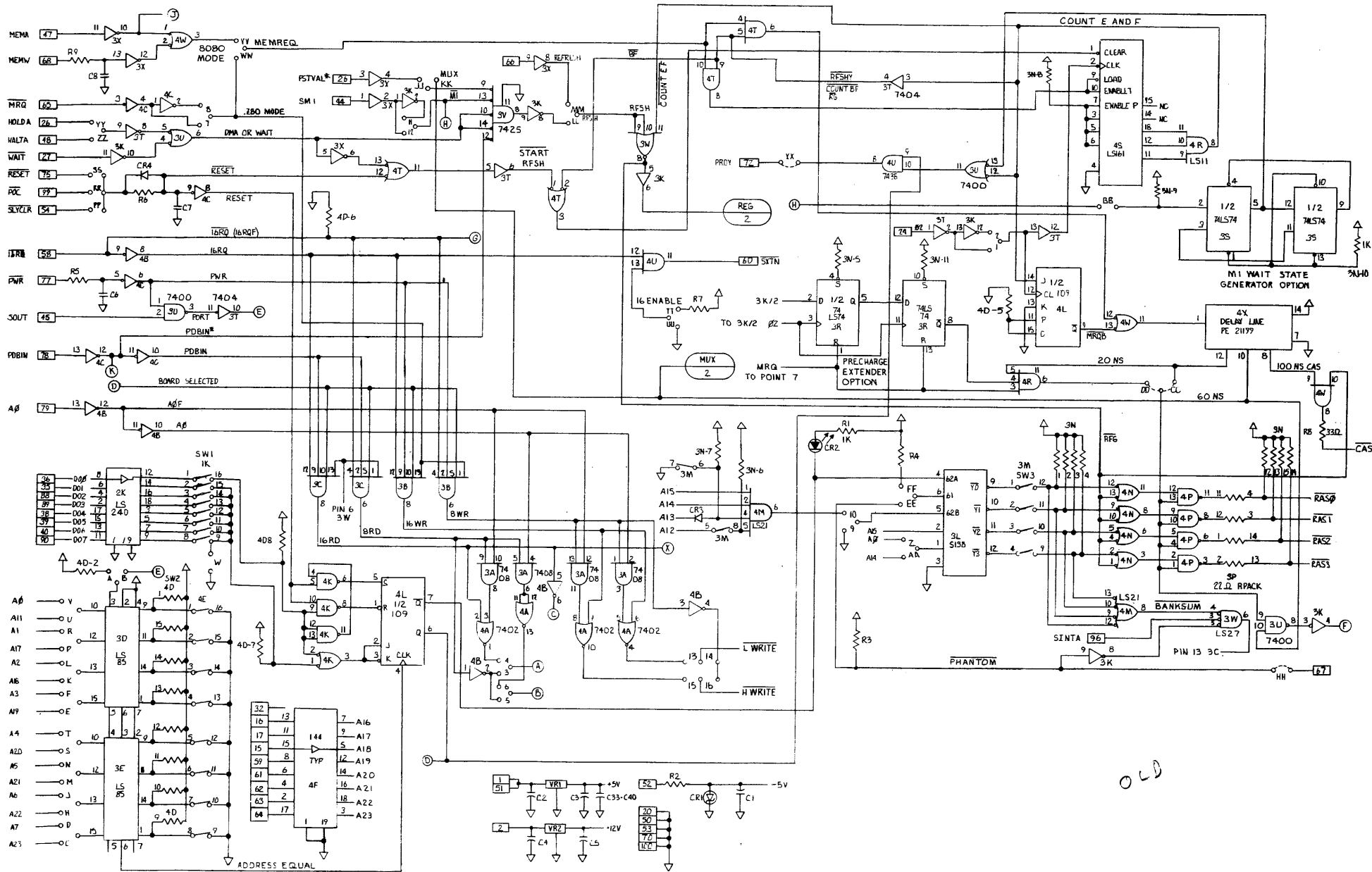
4	3	2	1
CS0*	CS1*	CS2*	CS3*
0	1	1	1
1	0	1	1
1	1	0	1
1	1	1	0
0	1	0	1
0	1	0	1
1	0	1	0
1	0	1	0

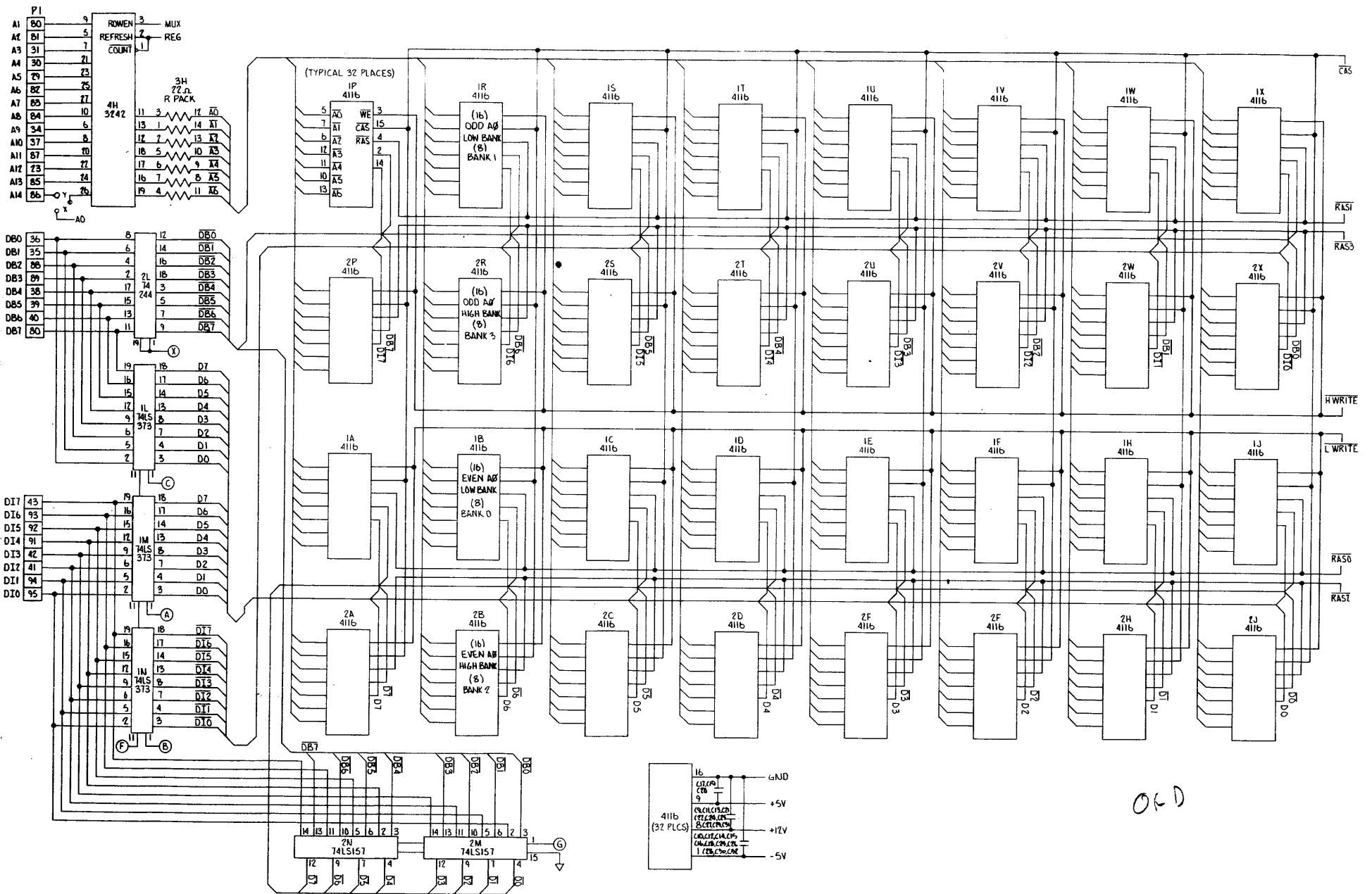
FUNCTION

SELECT	BANK	Ø
"	"	1
"	"	2
"	"	3
"	"	Ø + 2
"	"	4
"	"	1 + 3
"	"	"

CHIP USAGE

LOC	74#	1	2	3	4	5	6	
3A	08	X	X	X	X			✓ NI
3B	21	X	X					✓ NI
3C	21	X	X					✓ NI
3K	04	X	X	X	X	X	X	✓ I
3T	04	X	X	X	X	X	X	✓ I
3U	00	X	X	X	X			✓ I
3V	25	/	X					✓ I
3W	27	X	X	X				✓ I
3X	04	X	X	X	X	X	X	✓ I
4W	00	X	/	X	X			✓ I
4U	38	/	/	X	X			✓ I OC
4T	00	X	X	X	X			✓ I
4R	11	X	X	/				✓ NI
4P	00	X	X	X	X			✓ I
4N	00	X	X	X	X			✓ I
4M	21	X	X					✓ NI
4K	00	X	X	X	X			✓ I
4C	04	X	X	X	X	X	X	✓ I
4B	04	X	X	X	X	X	X	✓ I
4A	02	X	X	X	X			✓ I





OLD



MC3242A

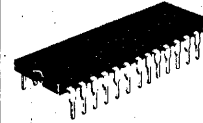
MEMORY ADDRESS MULTIPLEXER FOR 16K RAMS

The Motorola MC3242A is an address multiplexer and refresh counter for 16-pin 16K dynamic RAMs that require a 128-cycle refresh. It multiplexes fourteen system address bits to the seven address pins of the memory device. The MC3242A also contains a 7-bit refresh counter that is clocked externally to generate the 128 sequential addresses required for refresh. The high performance of the MC3242A will enhance the high speed of the N-channel RAMs such as the MCM4116.

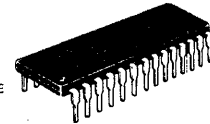
- Simplifies 16-Pin 16K Dynamic Memory Design
- Reduces Package Count
- 7-Bit Binary Counter for 128 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus:
 $I_F = 0.25 \text{ mA Max}$
- Schottky TTL for High Performance Address Input to Output Delay –
 $t_{AO} = 25 \text{ ns @ } C_L = 250 \text{ pF}$
- Second Source to Intel 3242
 (Detect Zero Function Not Included and Additional Chip Enable Feature Added at Pin 15)

MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUITS

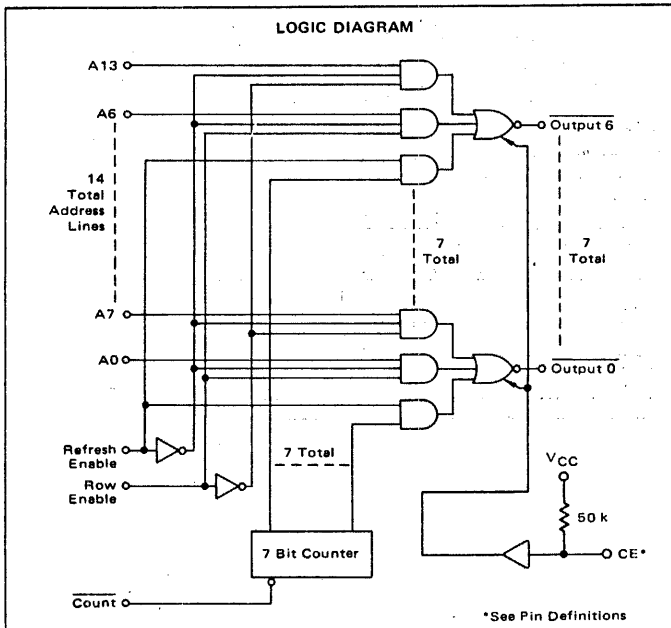


L SUFFIX
CERAMIC PACKAGE
CASE 733



P SUFFIX
PLASTIC PACKAGE
CASE 710

LOGIC DIAGRAM



Count	1	28	VCC
Ref En	2	27	A6
Row En	3	26	A13
N.C.	4	25	A5
A1	5	24	A12
A8	6	23	A4
A2	7	22	A11
A9	8	21	A3
A0	9	20	A10
A7	10	19	O6
O0	11	18	O3
O2	12	17	O4
O1	13	16	O5
Gnd	14	15	CE*

Note: A0 Through A6 Are Row Addresses
 A7 Through A13 Are Column Addresses
 *See Pin Definitions

TRUTH TABLE AND DEFINITIONS

Refresh Enable	Row Enable	Output
H	X	Refresh Address (From Internal Counter)
L	H	Row Address (A0 through A6)
L	L	Column Address (A7 through A13)

Count – Advances Internal Refresh Counter

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to +7.0	V
Output Voltage	V_O	-0.5 to +7.0	V
Output Current	I_O	100	mA
Operating Ambient Temperature	T_A	0 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Junction Temperature	T_J		$^\circ\text{C}$
Ceramic Package		+175	
Plastic Package		+150	

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with $4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $0^\circ\text{C} < T_A < 75^\circ\text{C}$; typical values apply with $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Low Logic State ($V_{IL} = 0.45\text{ V}$)	I_{IL}	—	-0.04	-0.25	mA
Input Current, High Logic State ($V_{IH} = 5.5\text{ V}$)	I_{IH}	—	—	10	μA
Input Voltage, Low Logic State	V_{IL}	—	—	0.8	V
Input Voltage, High Logic State	V_{IH}	2.0	—	—	V
Output Voltage, Low Logic State ($I_{OL} = 5.0\text{ mA}$)	V_{OL}	—	0.25	0.4	V
Output Voltage, High Logic State ($I_{OH} = -1.0\text{ mA}$)	V_{OH}	3.0	4.0	—	V
Input Clamp Voltage ($I_{IK} = -12\text{ mA}$)	V_{IK}	—	-0.8	-1.5	V
Power Supply Current ($V_{CC} = 5.5\text{ V}$)	I_{CC}	—	95	125	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with $4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $0^\circ\text{C} < T_A < 75^\circ\text{C}$; typical values apply with $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					
Address Input to Output (Load = 1 TTL, $C_L = 250\text{ pF}$) (Load = 1 TTL, $C_L = 15\text{ pF}$, $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	t_{AO}	—	12 6.0	25 9.0	ns
Row Enable to Output (Load = 1 TTL, $C_L = 250\text{ pF}$) (Load = 1 TTL, $C_L = 15\text{ pF}$, $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	t_{OO}	12 7	27 12	41 27	ns
Refresh Enable to Output (Load = 1 TTL, $C_L = 250\text{ pF}$) (Load = 1 TTL, $C_L = 15\text{ pF}$, $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	t_{EO}	12 7	30 14	45 27	ns
Count Pulse Width	t_{WC}	30	—	—	ns
Counting Frequency	f_C	5.0	10	—	MHz

FIGURE 1 – AC WAVEFORMS WITH MCM4116 NORMAL CYCLE

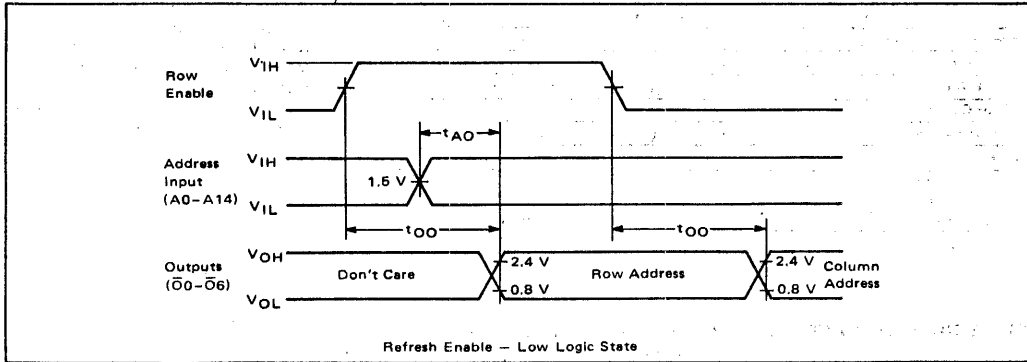
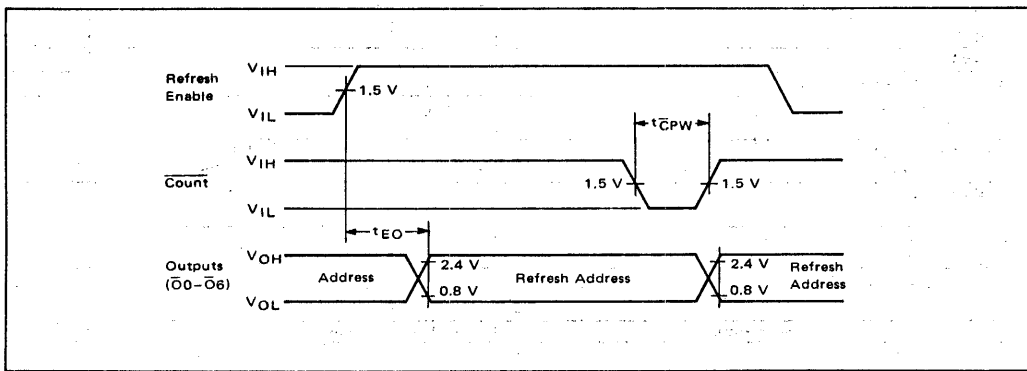


FIGURE 2 – REFRESH CYCLE



TYPICAL CHARACTERISTICS

FIGURE 3 – OUTPUT CURRENT versus OUTPUT LOW VOLTAGE

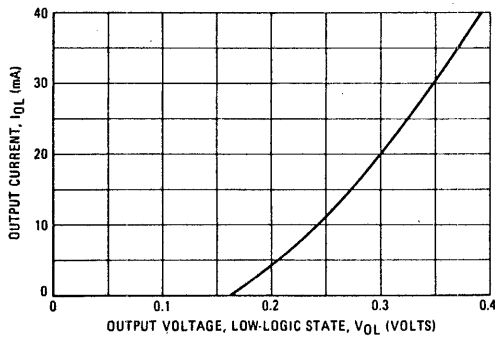
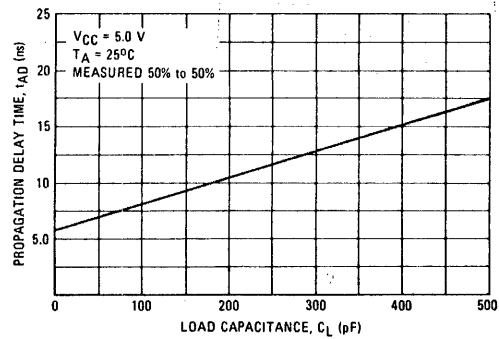


FIGURE 4 – PROPAGATION DELAY versus LOAD CAPACITANCE Row or Column Address to Output



PIN DEFINITIONS

Count Input – Pin 1

Active low input increments internal 6-bit counter by one for each count pulse in.

Refresh Enable Input – Pin 2

Active high input which determines whether the MC3242A is in refresh mode (H) or address enable (L).

A0–A6 Inputs – Pins 9, 5, 7, 21, 23, 27

Row address inputs.

A7–A13 Inputs – Pins 10, 6, 8, 20, 22, 24, 26

Column address inputs.

$\bar{O}0$ – $\bar{O}6$ Outputs – Pins 11, 12, 13, 18, 17, 16, 19

Address outputs to memories. Inverted with respect to address inputs.

Gnd – Pin 14

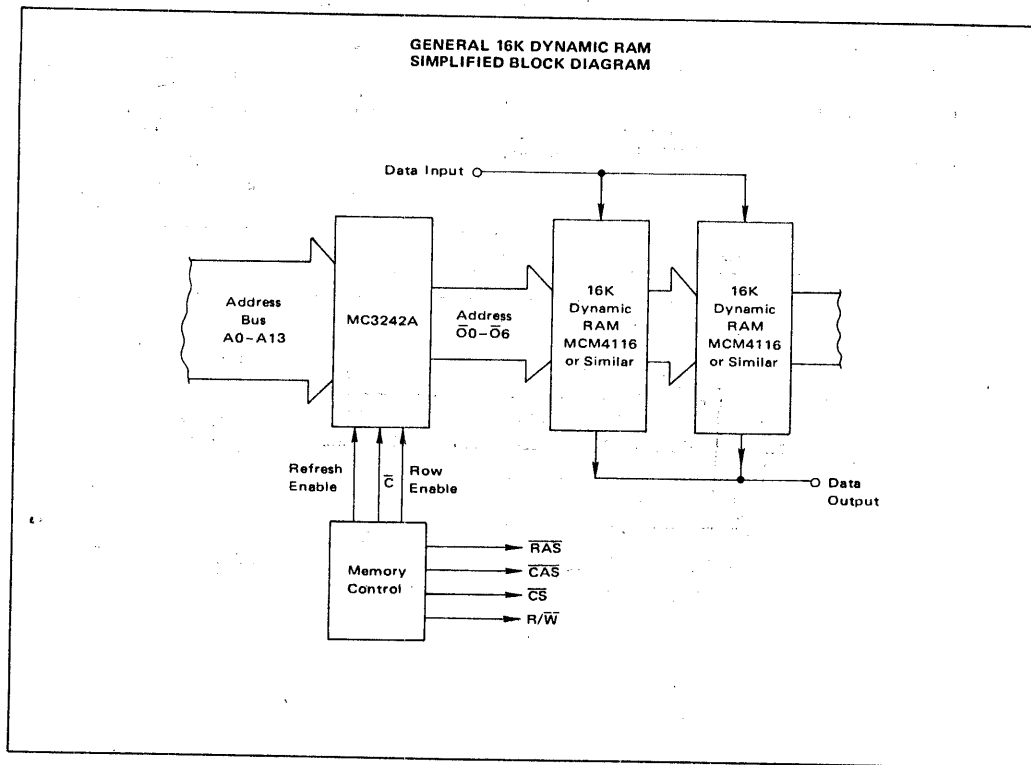
Power supply ground.

CE Input – Pin 15

Optional use, chip enable control pin. Left open, an internal 50 k Ω pullup resistor keeps this pin high and the MC3242A is a functional replacement for the Intel 3242 (without detect zero function). As an active input, when pulled low, all 3242A outputs go three-state. Regardless of Pin 15 (CE) condition, when power (VCC) is removed, all 3242A outputs go three-state. In addition, the refresh address counter is reset to all 1s so that upon return of supply power, control of refresh addressing can be returned to the MC3242A (by pulling Pin 15 high) at a known address (i.e., all 1s). This option is available tested by consulting factory.

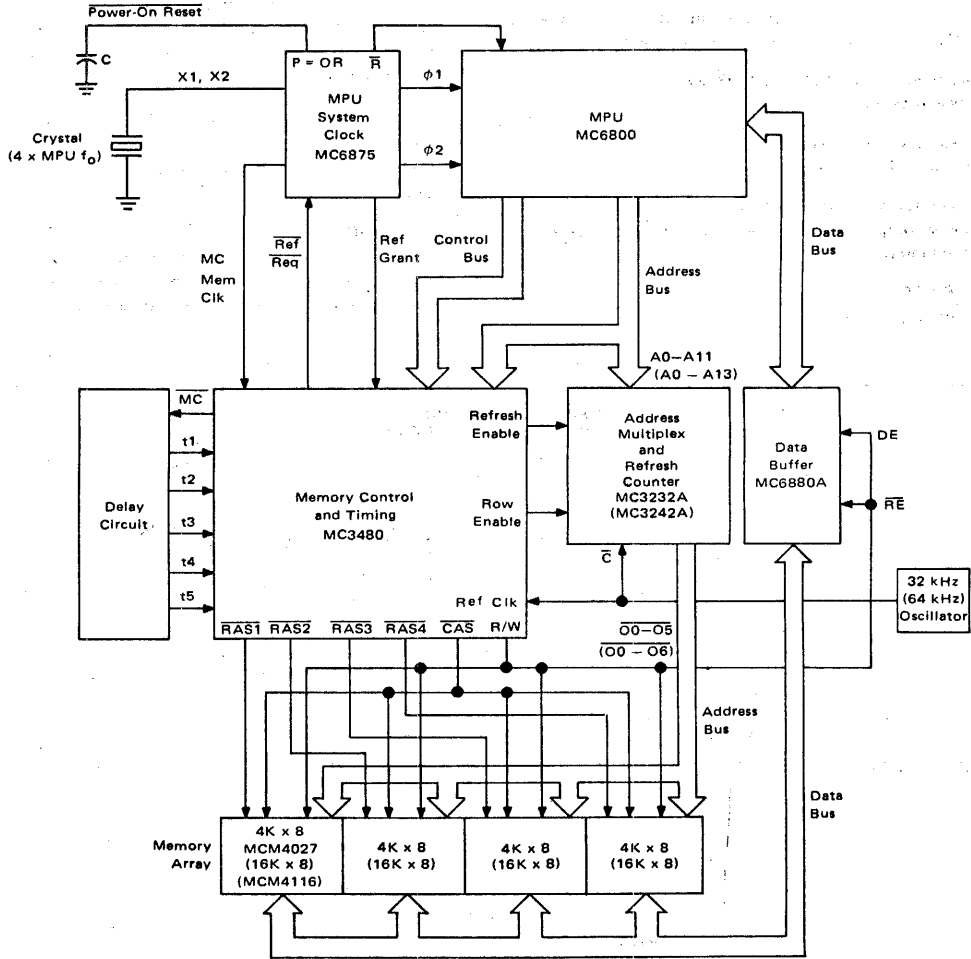
VCC – Pin 28

+5 V power supply input. Due to high capacitance drive capability, a 0.1 μ F capacitor should be used to ground along with careful VCC and Gnd Bus layout.



TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs



ERRATA

The only known error on revision A of the MEMORY BANK has to do with extended address decoding. As it is presently, only one MEMORY BANK may be used in a system with extended addressing. To correct this, proceed as follows:

1. Remove IC 4A-D (NOR gate, pins 11, 12 & 13) from its circuit by cutting the line from pin 6 of 3A to pin 11 & 12 of 4A. Remove the connection between pin 13 of 4A and the center pin of option jumper 5/6.
2. Replace IC 4A-D by routing a jumper from pin 6 of 3A to pin 5 of inverter 3X. Install a jumper from pin 6 of inverter 3X to the center pin of option jumper 5/6.
3. Connect 4A pin 11 to 3E pin 5. Connect 4A pin 12 to 3E pin 7. Connect 4A pin 13 to pin 1 of 4L after removing the connection that presently exists between pin 1 of 4L and pin 8 of 4K.
4. Remove the connection between pin 5 of 4L and pin 6 of 4K. Install a jumper from pin 5 of 4L to pin 3 of the resistor pack at 4D.
5. Install option jumper W.

The purpose of this correction may be explained as follows:

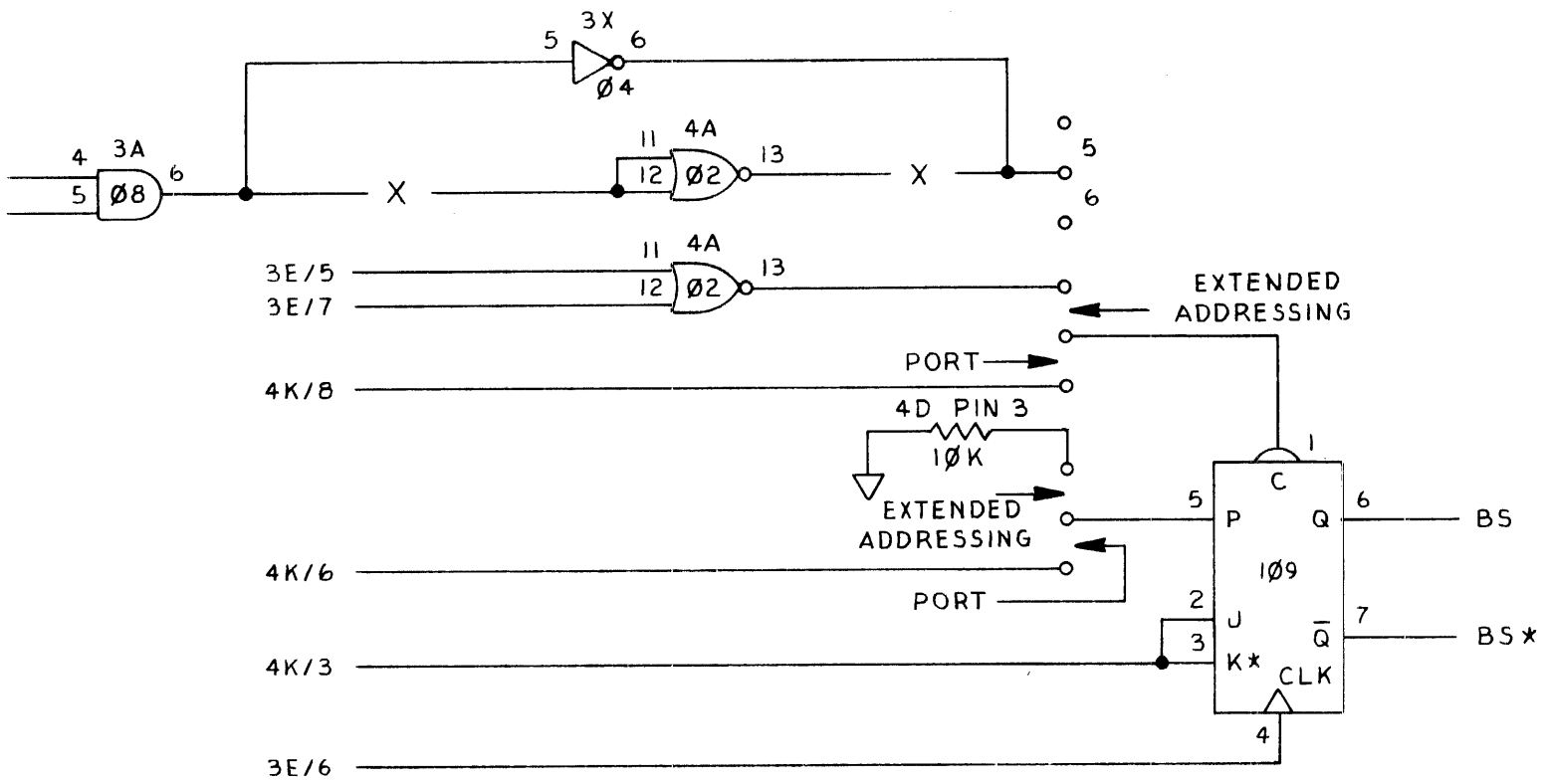
As the board is presently constituted, when the extended addressing options are selected, the equals output of 3E will go high when the address on the extended address bus matches the setting of the switches at 4E, and the board will be properly selected. However, the J-K* flip-flop at 4L has no means of *deselecting* the board once it has been selected, other than by a reset operation. When the equals output of 3E goes back low, the board will remain selected.

This correction NORs the greater-than and less-than outputs of the comparator at 3E, and routes them to the Clear input of the 74LS109 flip-flop. Preset is tied high. Now, when the address decoders respond to an address that is *not* the same as that to which the board is addressed, the LS109 flip-flop will be cleared and the board will be deselected. At the next rising edge of the equals output of 3E, both the greater-than and less-than outputs of the comparator will go low, causing NOR gate 4A-D's output to go high, enabling the flip-flop. Since jumper W is installed, the flip-flop will set at the rising edge of the equals output of the comparator, and the board will be properly selected.

CAUTION:

Since the connections from pin 6 of 3A to pins 11 and 12 of 4A, and the connection from pin 13 of 4A to the center of option 5/6 are run on an interior board plane, you will have to remove the pins of IC 4A from their socket and make your connections outside the socket. The same state of affairs exists for pin 5 of IC 4L.

This error will be corrected in future revisions of the MEMORY BANK.



ERRATA FIG. 1

JADE

Computer Products

Subject: Engineering Product Improvement Bulletin #1
Product: The Memory Bank Revision D
Date: May 18, 1981

Problem: Revision D Board Errata.

The following changes need to be made to all Revision D Memory Bank Boards purchased as a Bare Board or in Kit form. These changes have already been made to all Assembled & Tested Boards.

The enclosed schematic is the proper schematic for the Revision D Board although it does not reflect the following changes.

- Solution:
1. Cut the etch from I.C. 3U Pin 10 (74LS00) to the plated-through-hole on the solder side of the board.
 2. Jumper Pin 10 to Pin 9 on the same I.C. (3U, 74LS00).

