QRGB-GRAPH

Colour Graphics Controller

MANUAL NO. 173-A50-02/2

RELEASE DATE 02/01/84

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FEATURES

- 512 x 512 x 4 or 1024 x 512 x 2 SOFTWARE SELECTABLE RESOLUTION
- Q-BUS PLUG-IN
- 4 BIT PLANES
- PAN and SCROLL
- VECTOR PLOT
- EXPANDABLE
- SCREEN PRESET
- BIT PLANE WRITE ENABLE
- OPTIONAL GRAPHICS SOFTWARE
- INDEPENDENT X and Y ZOOM
- DMA TRANSFERS
- HARDWARE CLIPPING
- VIDEO BUS
- LIGHT PEN INTERFACE
- VIDEO OUTPUT ENABLE
- PROGRAMMABLE DISPLAY FORMAT
- COLOUR LOOK-UP TABLE

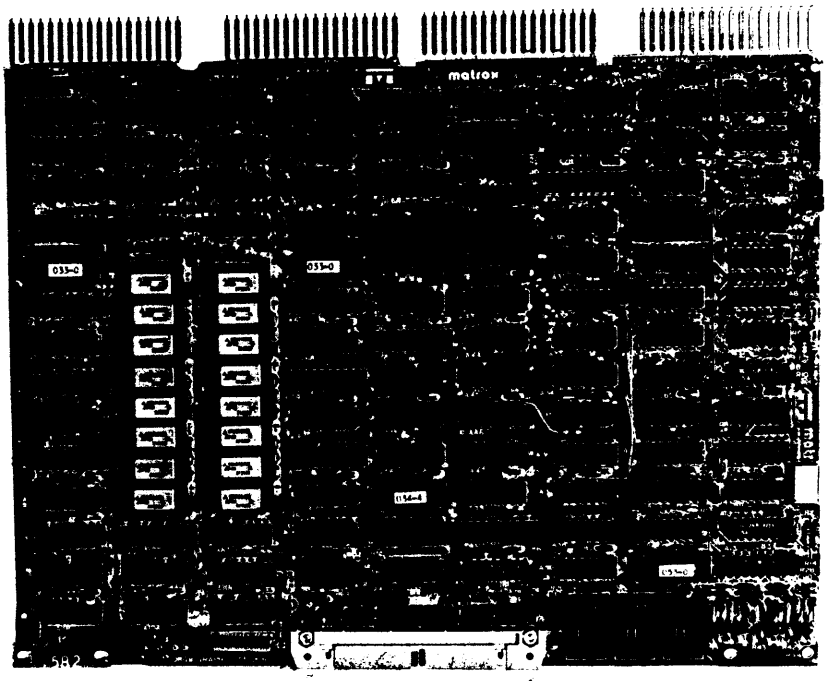

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

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1.0 SPECIFICATIONS:

Bus:

- Q-BUS plug-in.

Resolution:

- QRGB-Graph/64-1. 512 pixels x 512 pixels x 1 bit.
- QRGB-Graph/64-4. 512 pixels x 512 pixels x 4 bits.

- NOTE: The horizontal resolution of the -4 model can be doubled by sacrificing two bit planes.

Display Memory Access:

- Normal: programmed I/O via X and Y address registers and data port.
- DMA: occupies 256 Bytes of system memory I/O page.
- Access Time from BDIN, BDOUT to BRPLY/:
  . 500 ns. to Address Register, Data Register, Status Register, and Vector Register.
  . 50 ns. to all other locations (DMA included) if no internal cycle resulting from a previous access is in process; if a subsequent access is made while an internal cycle is still in process, BRPLY/ will not be generated until that cycle is ended. See Table 1.1 for access cycle times.

FORMAT	X-Y ZOOM	CYCLE TIME (10.000MHz XTAL)		
		BEST TIME	AVERAGE	WORST TIME
256 x 256	X1	800ns	1460ns	2.4us
	X2	800ns	1230ns	2.4us
	X4	800ns	1020ns	2.4us
512 x 256 512 x 512	X1	400ns	730ns	1.2us
	X2	400ns	615ns	1.2us
	X4	400ns	510ns	1.2us

Table 1.1 - CYCLE TIMES.

Special Functions:

- Independent X and Y Zoom:
  . X-Zoom by 1,2,3,4,5,6,7, or 8.
  . Y-Zoom by 1,2, or 4.
- Scroll and Pan:
  . horizontal pan with single pixel precision.
  . vertical scroll with 8 pixel precision.
- Fast preset of display to value in data port.
- DMA access to the Display Memory.
- Light Pen Register.
- Vector Plot.

1.0 SPECIFICATIONS (Cont'd):

Special Functions:(Cont'd)

- Colour Look-up Table.
- Single or continuous frame grab with external frame grabber.
- Software enabled clipping of X and Y Registers.
- Grey-scale DAC.
- Blink.

Video Bus:

- 16 bits of graphics video.
- 8 bits of frame grab data.
- Sync and control signals.
- Interfaces QRGB-Graph boards in groups of up to 4 (16 bits/pixel).
- Allows use of the QRGB-Graph with the QRGB-Alpha alphanumeric controller and/or the QVAF board.

I/O:

- Occupies up to 272 byte locations in system I/O page:
  . 16 locations for registers.
  . 256 locations for DMA buffer (if used).
- Registers can be strapped on any 16 Byte boundary above the DMA space.
- DMA buffer can be strapped on any 256 Byte boundary in device space.

T.V. Standard:

- European (50 Hz) or American (60 Hz) operation.
- Fully functional with 10 MHz RGB monitor.
- Grey scale functions with 10 MHz black and white monitor.
- Functional with standard and direct drive monitors.

Connectors:

- A->D, standard Q-BUS edge connectors: bus signals.

- J1, 10 pin right angle header AMP # 87578-2: composite video. Mates with AMP # 87922-1 or equivalent.

- J2, 10 pin right angle header AMP # 87578-2: outputs for direct drive monitors. Mates with AMP # 87922-1 or equivalent.

- J3, 10 pin right angle header AMP # 87578-2: light pen signals. Mates with AMP # 87922-1 or equivalent.

- J4, 50 pin right angle header MOLEX # 10-25-4505 (# 4700): video bus. Mates with MOLEX #10-55-3505 (# 7404) or equivalent.

1.0 SPECIFICATIONS (Cont'd):

Interrupts:

- Light Pen Interrupt.
- 'Preset Finished' Interrupt.

Power Requirements:

- QRGB-Graph/64-1:
  . +5V ±5% @ 2.5A

- QRGB-Graph/64-4:
  . +5V ±5% @ 3.0A

Dimensions:

- Standard LSI-11 Quad Height card: 12 inches wide by 10.457 inches high by 0.5 inches thick.

Environment:

- Operating temperature: 0° to 55° C (32° to 131° F).

- Relative humidity: 0% to 90% non-condensing.

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2.0 FUNCTIONAL DESCRIPTION:

The QRGB-Graph is a Q-BUS compatible colour graphics video controller board for use with RGB monitors. It utilizes a Colour Look-up Table (contained in PROM) which has 32 colour maps. Each map can contain 16 of a choice of 256 possible colours. The colour map also allows selected areas of the display to blink back and forth from one colour to another. It greatly simplifies the software required to manipulate colours in a graphics system.

A graphics software package (available as an option) renders the QRGB-Graph completely transparent to the user. For further information about this package, refer to Appendix B.

Data can be passed between the QRGB-Graph and other MATROX video controller cards on a well organized video bus that can be implemented with a single 50 line ribbon cable.

The QRGB-Graph is available in two models with maximum resolutions ranging from 512 pixels by 512 pixels by one bit plane to 512 pixels by 512 pixels by four bit planes. The 4 bit plane models can merge bit planes to double the horizontal resolution. The display format is set by the user during a programmed I/O initialization of the board.

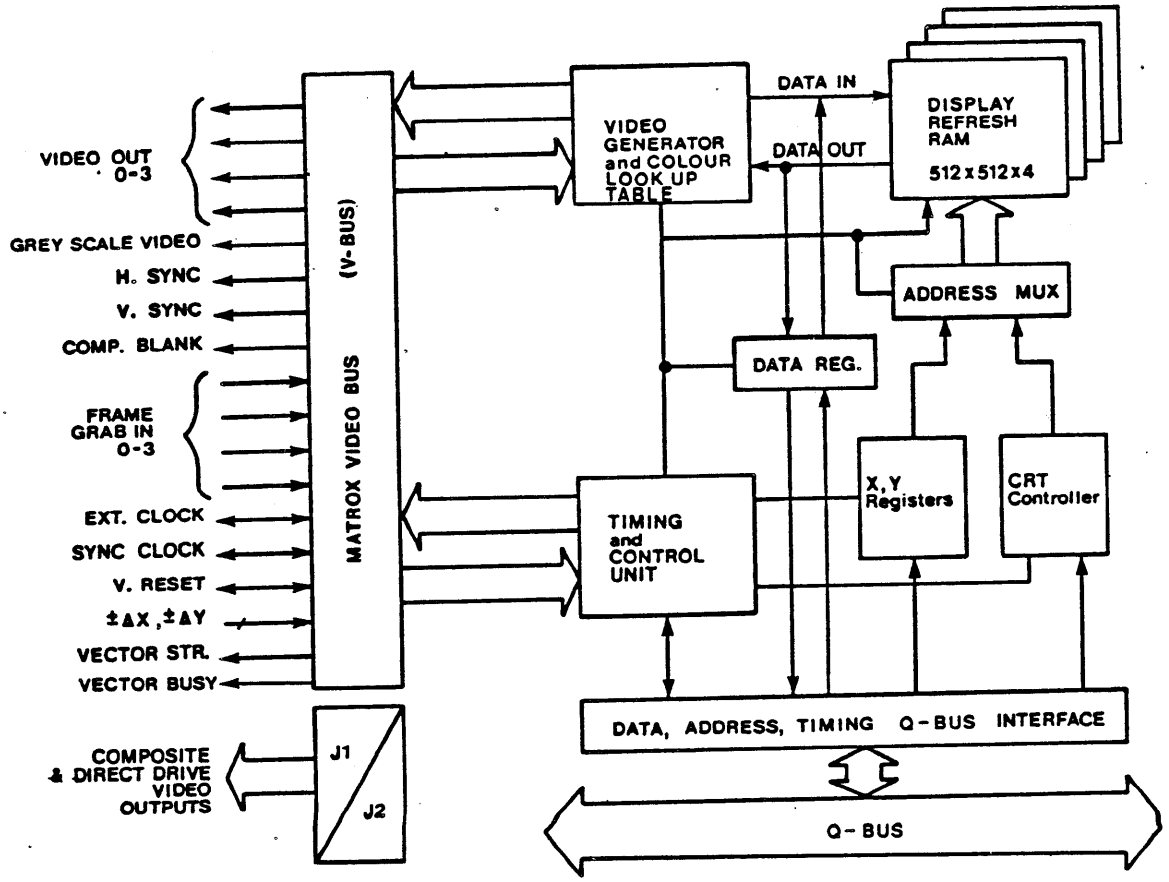


Figure 2.1 - QRGB-Graph BLOCK DIAGRAM.

2.1 DISPLAY MEMORY ACCESS:

The QRGB-Graph's display memory is normally accessed by programmed I/O: Display Memory locations corresponding to pixels are pointed to by the X and Y registers, and are accessed through the Data Register. The X and Y Registers, which contain the pixel's horizontal and vertical coordinates respectively, can be accessed by direct I/O or their contents can be modified via the Vector Register. Depending on the command loaded into it, the Vector Register increments or decrements, independently, the X and Y registers, and it can be commanded to automatically write the contents of the Data Register into the Display Memory. The Vector Register is used to rapidly draw horizontal, vertical, or angular lines.

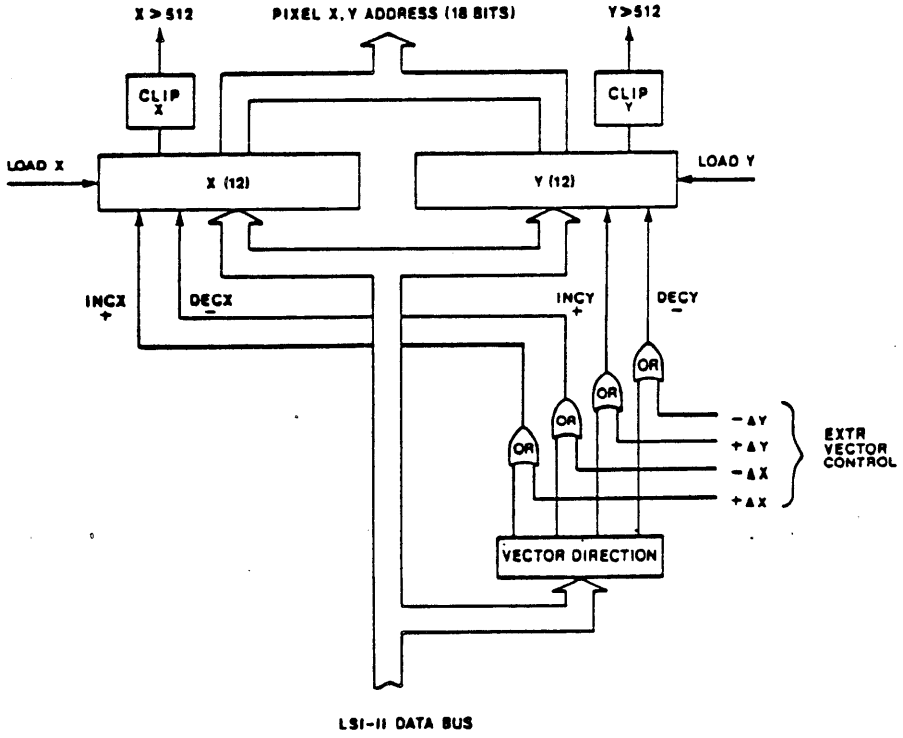


Figure 2.2 - X AND Y REGISTERS.

The Display Memory can also be accessed by an external DMA controller. When the QRGB-Graph is used in DMA mode, it occupies 256 Bytes of system address space that is positioned within the I/O page via straps. The DMA controller does each block transfer into this same 256 byte address block which is mapped into different areas of the Display Memory by the X and Y Registers. As the DMA proceeds, the X and Y Registers are automatically incremented after every 256 byte transfer.

The QRGB-Graph also has a fast preset function which uses one command to fill the entire Display Memory with the data contained in the Data Register. Similarily, provision has been made for the Display Memory to be loaded from an external frame grabbing A/D converter. Both operations are completed in one frame period.

When the QRGB-Graph is not in DMA Mode, the X and Y Registers may be clipped so that any data written to pixels outside the display format will not wrap around on the Display. This provides a total working area, displayed and non-displayed, of 4096 pixels by 4096 pixels for all formats (see figure 2.3).

2.1 DISPLAY MEMORY ACCESS (Cont'd):

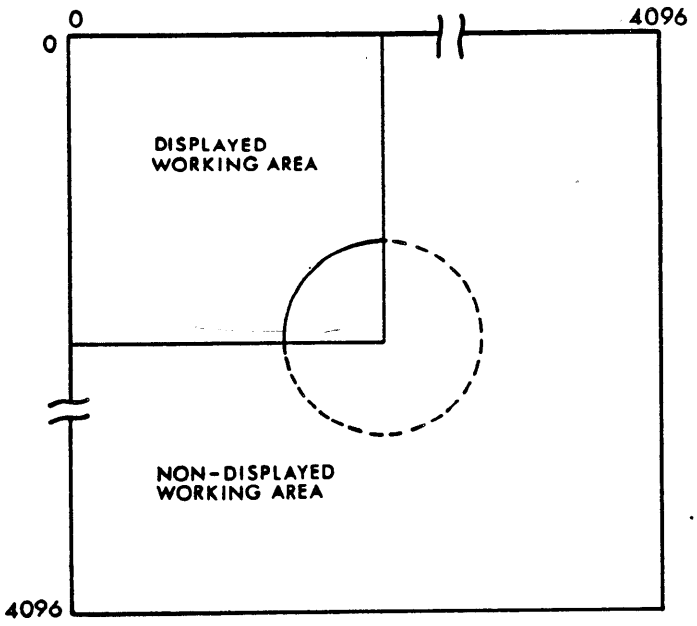


Figure 2.3 - NON-DISPLAYED WORKING AREA.

Normally all bit planes are written to simultaneously; however, the QRGB-Graph has a mask register which allows write access to be interdicted to any or all of the bit planes.

2.2 DISPLAY MANIPULATION:

The QRGB-Graph allows the user to zoom into the display. That is to say, a portion of the display can be selected and expanded to replace the original image from which it was taken. Horizontal expansion (X-zoom) and vertical expansion (Y-zoom) are independently controlled allowing the user to make distorting as well as non-distorting zooms. Horizontal zooms can be made by factors of 1, 2, 3, 4, 5, 6, 7 and 8; vertical zooms can be made by factors of 1, 2, and 4.

The display can be panned horizontally with single pixel precision in both directions, and it can be vertically scrolled with 8 pixel precision in both directions.

A series of light pen registers are provided which allow the CPU to determine the position of a light pen to within one pixel.

2.3 COLOUR LOOK-UP TABLE:

The QRGB-Graph contains a Colour Look-up Table consisting of a fast EPROM (A26) configured as two colour map sets of 256 x 8 bits. The standard Eprom shipped with the QRGB-Graph contains one map set ("A") programmed with a selection of colours. The second map set ("B") is empty so that the user can program custom maps. Each map set is divided into 16 colour maps containing up to 16 colours each. During display refresh, the QRGB-Graph board generates 8 bits per pixel which address the look-up table. The contents of the locations accessed drive three DACs (one for each primary colour) and the grey scale converter. Since the output of the table is 8 bits wide, each DAC can be assigned varying degrees of luminance, which combine to provide a choice of 16 of the 256 available composite colours for each look-up table location .

As well as providing a host of different colours, the look-up table allows portions of the display to be blinked between colours.

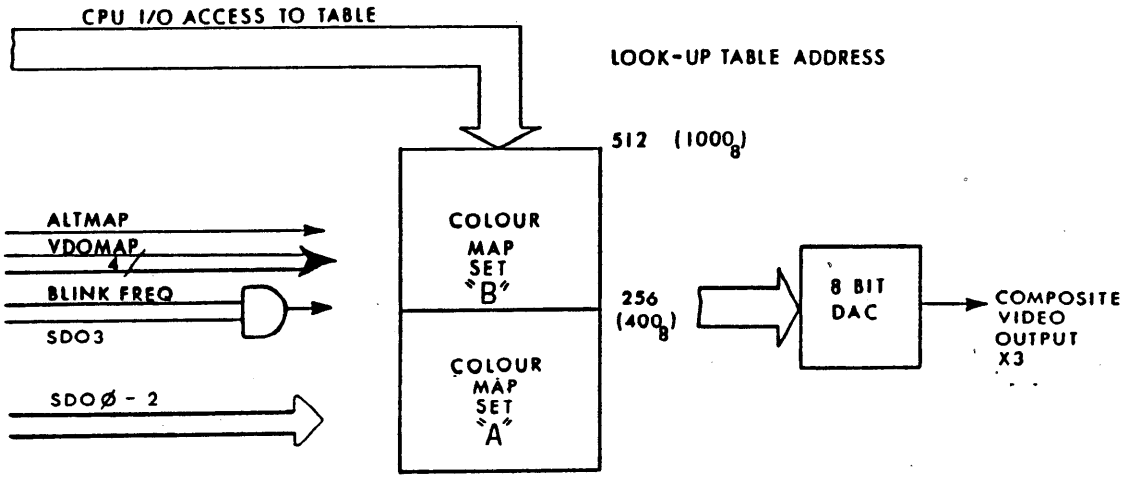


FIGURE 2-4. COLOUR LOOK-UP TABLE.

As shown in figure 2.4, the look-up table is divided into two 256 byte sections, each containing 16 colour maps. Each map contains 16 colours, addressed by bit plane data from the Display Memory (SDO 0-3), the contents of a Control Register (VDOMAP 0-3), and a Map Selection Bit (ALTMAP). The blink frequency is a low frequency square wave generated internally.

The blink frequency can be independently enabled or disabled by software. When disabled, the 4 bit planes of the QRGB-Graph board address colours within one colour map of the look-up table. This map contains digital equivalents of the visible colour spectrum, each map containing a variety of different colours. When the user wishes to display a certain colour at a certain pixel position, he simply loads that colour's look-up table location into the Display Memory location corresponding to the pixel position. For example, to display pure red at pixel location (X=2, Y=2), he could write 001 (octal) to the corresponding Display Memory location, 001 (octal) to Control Register 3, and `0' to Altmap (to direct access to the `A' map set in the look-up table).

2.3 COLOUR LOOK-UP TABLE (Cont'd):

When the blink frequency is enabled, a low frequency square wave toggles the fourth b of the Look-up Table between '0' and the pixel value in Bit Plane 4. This gives the effect of an alteration between two locations in the same colour map, and the type of blink will depend on the colour arrangement in the map chosen. If the colour data in a given map section is different from the colour data in the location that is blinked to, the pixels coloured by that data will blink back and forth between the two colours. If the location that is blinked to contains no colour data, the effect will be an 'on and off' blink instead.

For a further description of the colour maps, refer to Section 4.3.11 (register access), Section 4.5 (Look-up Table access), Appendix B (Quarto Graphics Package), and Appendix D (Color Table Contents).

2.4 VIDEO:

The QRGB-Graph has three DACs which are also the composite video outputs for color (red, green and blue). A 4-bit D/A converter supplies another composite video output for grey scale applications. Since the horizontal and vertical size, sync position, and sync pulse width are software controlled, the QRGB-Graph can easily be adapted to a wide variety of 75 ohm RGB monitors. The QRGB-Graph also has two separate TTL video outputs: one for direct drive monitors and one for the video bus connector. The video bus is a connection system that allows the QRGB-Graph to be used with other vide control products from MATROX (see section 9 and section 7.5).

* * * * *

3.0 START-UP PROCEDURE:

NOTE: The following familiarization procedure will not be valid if the as-shipped strap configuration is changed or if a direct drive monitor is used.

1. Visually inspect the board for any shipping damage.

2. Plug the board into an LSI-11 system and connect an R.G.B. monitor. The video connections will depend on the monitor used; however, section 7 shows where to find any of the video or sync signals that might be required.

3. Use the procedure in table 3.1 to initialize the display, outputting the 50 or 60Hz data to the I/O location indicated. This will establish the parameters for the maximum single density format of 512 x 512. NOTE: All numbers are in OCTAL.

4. If the system does not operate properly, refer to the troubleshooting procedure on page E-1.

STEP	DATA(octal) 60 HZ	DATA(octal) 50 HZ	I/O LOCATION	COMMENTS
1	037442	037442	164406	Control Register No. 1 is initialized; video enabled, single density, no DMA, no frame grab, no preset, X-Pan=0, X-Zoom=1, Y-Zoom=1. Note that two identical outputs are required to initialize this register.
2	037442	037442	164406	
3	000001	000001	164410	Control Register No.3 is initialized, all video outputs are initialized. Colour Map #1 Selected.
4	000000	000000	164412	Control Register No.4 is initialized, access to all bit planes is enabled.
5	010000	010000	164414	The horizontal total minus one is written to CRTC-R0.
6	000117	000117	164416	
7	010001	010001	164414	The format width, in cells, is written to CRTC-R1.
8	000100	000100	164416	
9	010002	010002	164414	The horizontal sync position is written to CRTC-R2
10	000103	000103	164416	
11	010003	010003	164414	The horizontal and vertical sync widths are written to CRTC-R3.
12	000066	000066	164416	

Table 3.1 - DISPLAY INITIALIZATION.

3.0 START-UP PROCEDURE(cont'):

STEP	DATA(octal) 60 HZ	DATA(octal) 50 HZ	I/O LOCATION	COMMENTS
13	010004	010004	164414	The vertical total minus one is written to CRTC-R4.
14	000077	000115	164416	
15	010005	010005	164414	The vertical adjust parameter is written to CRTC-R5.
16	000004	000000	164416	
17	010006	010006	164414	The format height, in cells, is written to CRTC-R6.
18	000074	000100	164416	
19	010007	010007	164414	The vertical sync position is written CRTC-R7.
20	000074	000102	164416	
21	010010	010010	164414	CRTC-R8 is programmed for row and column addressing & to appropriate interlace mode.
22	000007	000007	164416	
23	010011	010011	164414	The No. of scan lines/field per cell row-minus one is written to CRTC-R9.
24	000007	000007	164416	
25	010014	010014	164414	The starting address is set to row zero column zero.
26	000000	000000	164416	
27	010015	010015	164414	
28	000000	000000	164416	
Following the above steps in order, output the 50 or 60Hz data to the I/O location indicated.				

Table 3.1 - DISPLAY INITIALIZATION(cont'd).

5. The display should now be showing random data. Clear the display by outputting 000000 (octal) to the Data Register at 164404 then outputting 010037 to address 164414 to disable the CRTC address & Vector Registers and then writing 101000 to Control Register no. 5 at 164416 .

6. Enter and run the following program (next page), which will fill an RGB display with vertical color bars. On a monochrome monitor, it will be seen as a series of vertical bars of different grey scale levels:

3.0 START-UP PROCEDURE (Cont'd):

COLOR BARS

```
        .ENABL LC

base = 164400                   ; board base address
north = 4000                    ; data for vector reg
vector = base + 14              ; vector reg
data = base + 4                 ; data reg
xreg = base                     ; x regs
yreg = base + 2                 ; y regs
barw = 15.                      ; width of bar - 1
yres = 777                      ; y resolution
xres = 1000                     ; x   "        + 1

        .psect


start::mov      #-1.    ,r2     ; r2 = colour
       mov      #xres   ,r0     ; r0 = x register

newclr:inc      r2              ; inc r2 to next colour
       mov      r2      ,data   ; set new colour
       mov      #barw   ,r3     ; r3 = bar width

nxtcol:mov      #yres   ,r1     ; r1 = yreg
       mov      r1      ,yreg
       dec      r0
       bmi      done
       mov      r0      ,xreg

nxtpix:mov      #north  ,vector
       dec      r1
       bge      nxtpix
       dec      r3
       bge      nxtcol
       bmi      newclr

done:  ;
       ;  (insert return to operating system here)
       ;
       .end
```

In the program above the bar width and resolution may be changed by altering the values of barw, yres, and xres. The bar width in a 16-colour map is 16 pixels, and the map is accessed twice for each display cycle.

* * * * *

4.0 PROGRAMMING:

The QRGB-Graph is initialized and controlled by programmed I/O to a series of registers. There are 13 directly accessed registers plus 14 CRTC registers that are indirectly accessed through an address register and data port. Section 4.3 contains detailed descriptions of the directly accessed registers and the CRTC data sheets in Appendix A contain descriptions of the CRTC registers. Table 4.1 gives a brief overview of the directly accessed registers.

RELATIVE LOCATION	DIRECTION	NAME	FUNCTION
000_8	WRITE ONLY	X-Register.	Pixel X-coordinate.
002_8	WRITE ONLY	Y-Register.	Pixel Y-coordinate.
004_8	WRITE READ	Data Reg.	Data registers contain pixel data (color). From 4 bits/pixel (1-QRGB-GRAPH) to 16 bits/pixel (4-QRGB-GRAPH) user strappable.
006_8	READ ONLY	Status Register.	PRESET/
006_8	WRITE ONLY	Control Register Number 1.	Complement, Clipping, Interrupt/Double Resolution, DMA, Frame Grab Continuous, Blink, Map Sets, X-Pan, X-Zoom, Y-Zoom.
010_8	READ ONLY	Aux. Light Pen Register.	Light Pen Pixel Position
010_8	WRITE ONLY	Control Register Number 3.	Colour Map Select
012_8	WRITE ONLY	Control Register Number 4.	Bit plane write enable register (Preset Mask) From 4 bits to 16 bits, user strappable within two bytes.
014_8	READ ONLY	CRTC Status Register.	Vertical Blanking Flag Light Pen Register Full Flag.
014_8	WRITE ONLY	CRTC Address Register*	Address for CRTC's Internal Reg.
015_8	WRITE ONLY	Vector Register.	Increment/decrement control for X,Y registers for vector plots.
016_8	WRITE READ	CRTC Data Register.*	Data Port for CRTC's Internal Reg.
017_8	WRITE ONLY	Control Register Number 5.	CRTC Disable, Frame Grab, Preset Memory Control.

* These two registers indirectly access 14 more registers within the CRTC, specifying such video parameters as horizontal and vertical Sync, Blanking, Frequency Format, etc.

Table 4.1 - DIRECTLY ACCESSED REGISTER-OVERVIEW.

4.1 Format Programming Tables

Because the CRTC was intended for use with alphanumeric displays, the data sheets refer to characters and the character clock; however, as far as the QRGB-Graph is concerned, the user should read "8 x 8 pixel graphics cell" instead of "character", and "cell clock" instead of "character clock".

The display format is established during the initialization routine by writing the format parameters to Control Register No. 1 and certain CRTC registers. Table 4.2 shows which parameter must be written to which register to establish the standard maximum density format. The user may, however, wish to establish a non-standard format to facilitate some graphics applications. If this is the case, the format parameters can be calculated using the formulas given in Section 4.2.

Note that section 4.4 has been dedicated to the zoom function.

The following table shows which format parameters must be written to which registers to establish the standard formats. Note that there is a column of American parameters (60Hz) and a column of European (50Hz) parameters for each format given.

QRGB-GRAPH							
SINGLE DENSITY FORMAT		256 x 256		512 x 256		512 x 512	
AMERICAN/EUROPEAN		60HZ	50HZ	60HZ	50HZ	60HZ	50HZ
Control Register No. 1		037442_8		037442_8		037442_8	
H. Total	R0	047_8	047_8	117_8	117_8	117_8	116_8
H. Displayed,	R1	040_8	040_8	100_8	100_8	100_8	100_8
H. Sync. Position,	R2	041_8	041_8	105_8	105_8	103_8	103_8
V. & H. Sync Width	R3	063_8	063_8	066_8	066_8	066_8	066_8
V. Total,	R4	037_8	046_8	037_8	046_8	077_8	115_8
V. Adjust,	R5	004_8	000_8	004_8	000_8	004_8	000_8
V. Displayed,	R6	036_8	040_8	036_8	040_8	074_8	100_8
V. Sync. Position,	R7	037_8	044_8	037_8	044_8	074_8	113_8
Mode Control,	R8	004_8	004_8	004_8	004_8	007_8	007_8
Scan Line	R9	007_8	007_8	007_8	007_8	007_8	007_8
Display Start High	R12	000_8	000_8	000_8	000_8	000_8	000_8
Display Start Low	R13	000_8	000_8	000_8	000_8	000_8	000_8

Table 4.2 - STANDARD FORMATS.

Note #1: to alter the maximum display format from the as-shipped 512 x 512 size, a change to some straps will be required. Please refer to section 5.12 for information.

Note #2: Since the maximum number of scan lines on a 60 Hz (American) monitor is 480, only 480 of the 512 vertical pixels produced by the QRGB-Graph will be displayed. This can be compensated by adjusting the parameters shown in Section 4.2, but a higher persistance monitor may have to be used to avoid flicker.

4.2 FORMAT PARAMETER CALCULATIONS:

The QRGB-Graph's format is set by the X and Y zoom factors in Control Register No. 1 and by format parameters written to registers in the board's CRTC. Because the CRTC, an LSI video controller chip, was designed primarily to refresh alphanumeric displays, it sees the display as a field of graphics cells equivalent to characters and it refreshes the display at that level. Each of these graphics cells is 8 pixels by 8 pixels in size; display refresh at the pixel level within the cells is taken care of by circuitry external to the CRTC. Because the format is programmed in the CRTC, which operates at the cell level, the number of pixels in the X or Y axis of any format must be a multiple of 8. If the user conforms to this restriction, he can use the formulas in this section to calculate the parameters for a large number of different formats. The only other restriction, of course, is that the number of pixels in the format times the number of bit planes used must not exceed the capacity of the Display Memory.

In some cases, the user may find that the display does not cover as much of the CRT as might be wished. If such is the case he has the option of changing the crystal to a lower frequency.

The following is a list of formulas that can be used to calculate the format parameters for irregular formats or to calculate the parameter changes required for zoom operations:

1. DOT CLOCK = $\frac{\text{Crystal Freq.}}{\text{X-Zoom Factor}}$

2. CELL CLOCK = $\frac{\text{Dot Clock}}{8}$

   The Cell Clock is the same as the character clock referred to in the CRTC data sheets.

3. HORIZONTAL TOTAL = $\frac{\text{Monitor Spec. Horiz. Scan Period}}{\text{Cell Clock Period}}$

   Choose the nearest integer minus one. This value is written in Octal format to R0.

4. HORIZONTAL DISPLAYED = $\frac{\text{Total X-Axis Pixels}}{8}$

   This is the number of graphics cells in the X-AXIS of the format and is written in Octal to R1.

4.2 FORMAT PARAMETER CALCULATIONS:(cont'd)

5. HORIZONTAL SYNC. POSITION = H. Displayed + $\frac{\text{(H. Total - H. Displayed)}}{2}$

This value may require adjustment. It is written in Octal to R2.

6. ACTUAL HORIZONTAL SCAN PERIOD = $\frac{\text{Horizontal Total}}{\text{Cell Clock}}$

7. CELL ROW PERIOD = (Y-Zoom Factor) x 8 x (Actual Horizontal Scan Period)

8. VERTICAL TOTAL = $\frac{\text{Vertical Scan Period}}{\text{Cell Row Period}}$

This value minus one is written in Octal to R4. The vertical scan period is 33.334ms on American systems and 40.000ms for European systems.

9. VERTICAL TOTAL ADJUST = $\frac{\text{(Vertical Scan Period -(V. Total x Cell Row Period))}}{\text{Actual Horizontal Scan Period}}$

Choose the nearest integer. This value is written in Octal to R5.

10. VERTICAL DISPLAYED = $\frac{\text{Total Y-Axis Pixels}}{8}$

This value is written in Octal to R6.

11. VERTICAL SYNC. POSITION V. Displayed + $\frac{\text{(V. Total - V. Displayed)}}{2}$

Adjust the value as required. It is written in Octal to R7.

12. SCAN LINE = 8 x Y-ZOOM FACTOR

This value minus one is written in Octal to R9.

4.2 FORMAT PARAMETER CALCULATIONS:(cont'd)

13. HORIZONTAL SYNC. WIDTH = $\frac{\text{Monitor Spec. H. Sync. Width}}{\text{Cell Clock Period}}$

Choose the nearest integer. This value goes to bits 0-3 of R3.

14. VERTICAL SYNC WIDTH = $\frac{\text{Monitor Spec. V. Sync. Width}}{\text{Actual Horizontal Scan Period}}$

Choose the nearest integer. This value goes to bits 4-7 of R3.

4.3 REGISTERS: ON ALL REGISTERS USE WORD TRANSFERS ONLY. SEE APPENDIX F

Note that since "Read/Modify/Write" instructions use byte access they must not be used to change the contents of any register in this section. For proper operation, complete and separate Read and Write cycles should be used to modify data in these registers. NOTE: When power is first applied, the registers will be in a random state and will need to be reset once before initialization.

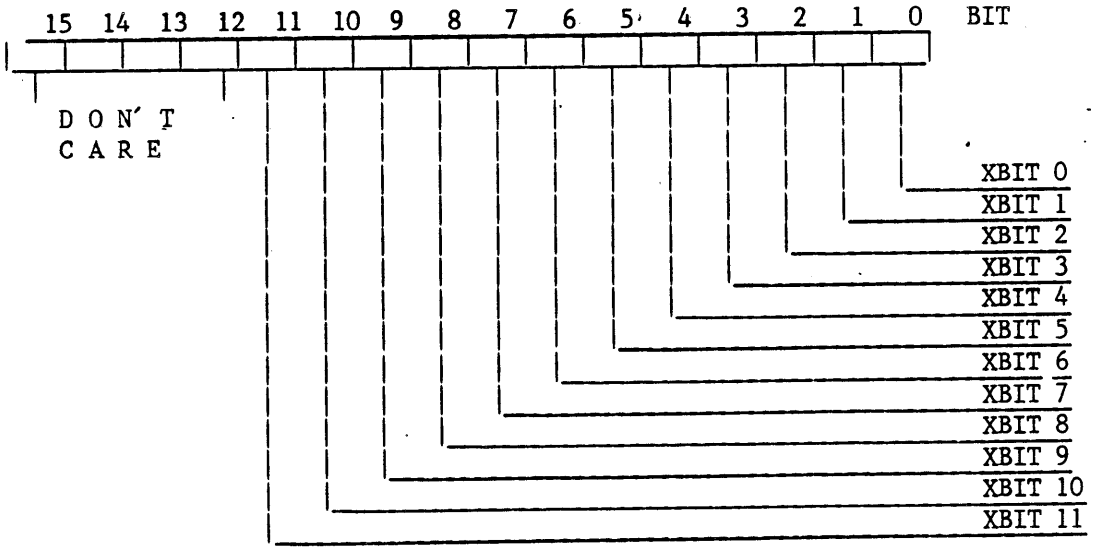
On some Operating Systems user programs will not have direct access to the device page. In this case, a 'Device Handler' routine should be written , to be called by the Operating System. Please check with your system documentation for the correct procedure. The Quarto software package from Infolytica has 'device drivers' built-in, so if it is used this need not be done.

4.3.1 X-REGISTER :

READ/WRITE

BASE ADDRESS + 00_8 = LOC. [ ]

AS-SHIPPED ADDRESS = 164400_8



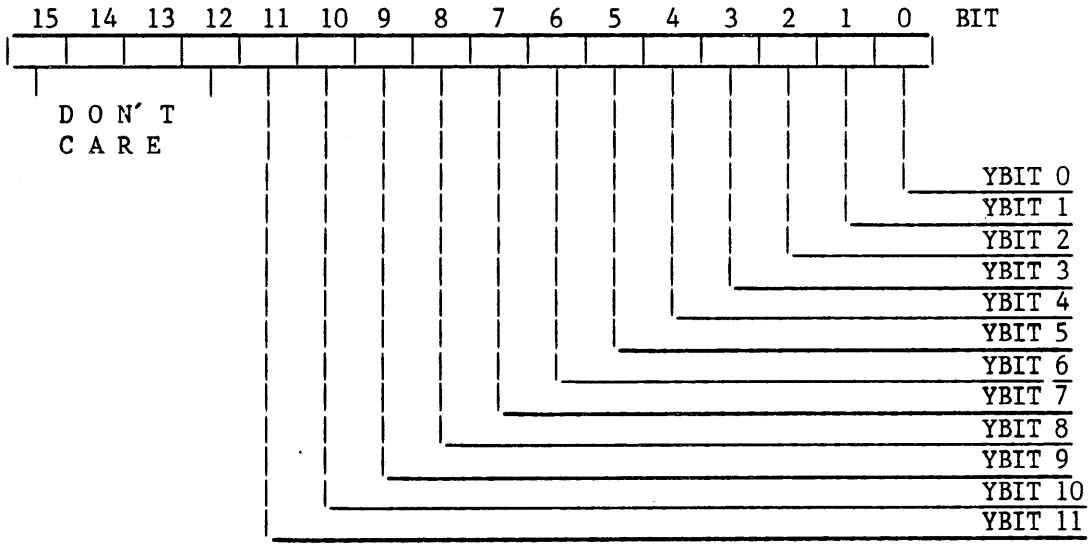
This register holds the 12 bits of the X coordinate of the display memory location that is to be accessed. If a '1' is written to any of bits 9-11 the clipping circuit will interdict memory access on the highest order bits, preventing 'wrap around' of the display on the horizontal axis.

4.3.2 Y-REGISTER :

READ/WRITE

BASE ADDRESS + 02_8 = LOC. ____

AS SHIPPED ADDRESS = 164402_8



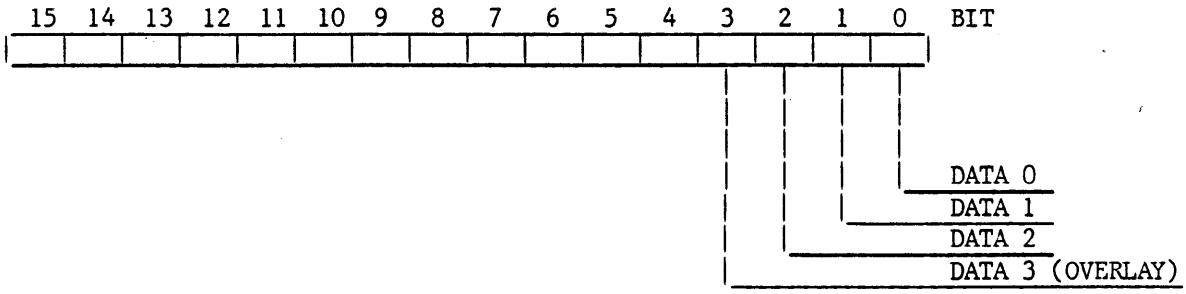
This register holds the 12 bits of the Y coordinate of the display memory location that is to be accessed. If a '1' is written to any of Bits 9-11 the clipping circuit will interdict memory access to the highest order bits thus preventing 'wrap-around' on the vertical axis.

4.3.3 DATA REGISTER :

READ/WRITE

BASE ADDRESS + 04_8 = | LOC. |

AS SHIPPED ADDRESS = 164404_8



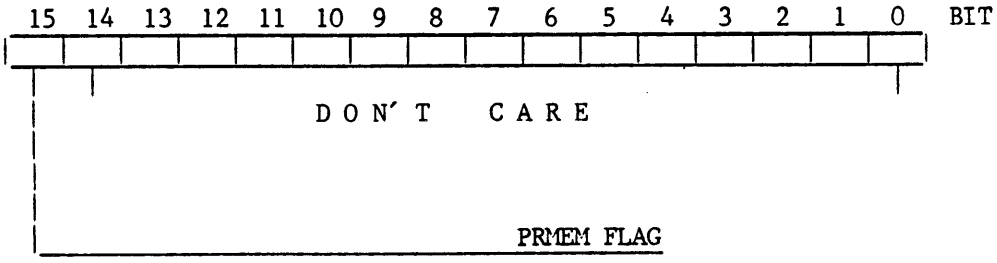
Any four bits of this register can be used as a data port to the Display Memory if the appropriate straps are installed (see Section 5.2). When the board is shipped, straps are installed which allow the display memory to be accessed through the four least significant bits of this register, as shown above. Bits not selected for use are "don't care" for write and zero for read(see Section 5.3).

4.3.4 STATUS REGISTER:

READ ONLY

BASE ADDRESS + 06_8 = | LOC. |

AS SHIPPED ADDRESS = 164406_8



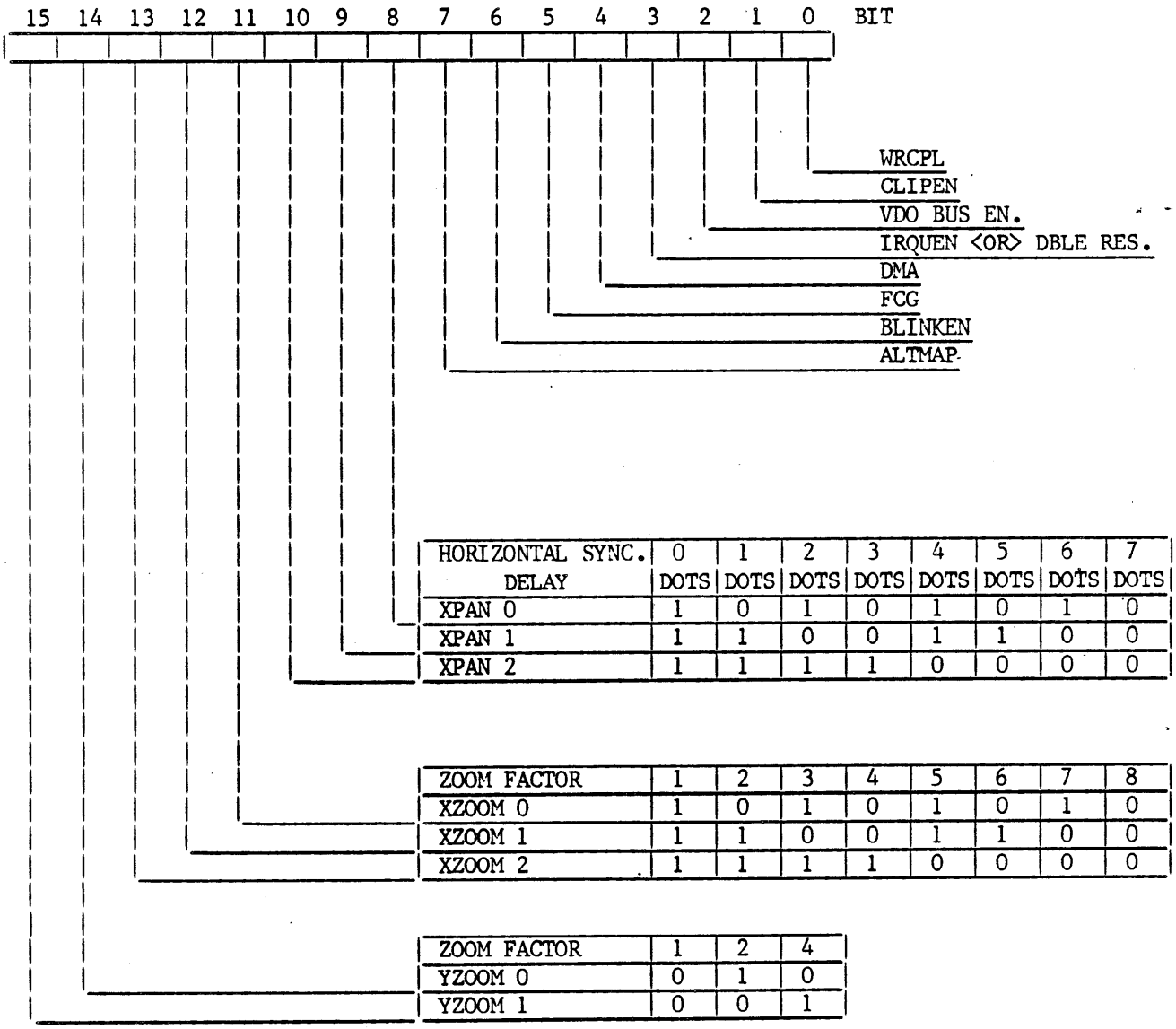
Bit 15: PRMEM FLAG. When this bit is one, the memory is being preset or a frame grab is in process. When this bit is zero, the memory is neither being preset nor is a frame grab in process.

4.3.5 CONTROL REGISTER NO. 1

WRITE ONLY

BASE ADDRESS + 06_8 = LOC. ____

AS SHIPPED ADDRESS = 164406_8



HORIZONTAL SYNC. DELAY	0 DOTS	1 DOTS	2 DOTS	3 DOTS	4 DOTS	5 DOTS	6 DOTS	7 DOTS
XPAN 0	1	0	1	0	1	0	1	0
XPAN 1	1	1	0	0	1	1	0	0
XPAN 2	1	1	1	1	0	0	0	0

ZOOM FACTOR	1	2	3	4	5	6	7	8
XZOOM 0	1	0	1	0	1	0	1	0
XZOOM 1	1	1	0	0	1	1	0	0
XZOOM 2	1	1	1	1	0	0	0	0

ZOOM FACTOR	1	2	4
YZOOM 0	0	1	0
YZOOM 1	0	0	1

NOTE: During initialization, the output operation to this register must be repeated twice. After initialization, one output is enough to load the register.

4.3.5 CONTROL REGISTER NO. 1 (Cont'd):

BIT 0: WRCPL. When this bit is one, writing to the Data Register will cause the data in the memory location addressed by the current contents of the X and Y Registers to be complemented. When this bit is zero automatic complement is disabled. Note: this bit does not work in Vector Plot Mode.

BIT 1: CLIPEN. When this bit is one, clipping is enabled. When this bit is zero, clipping is disabled.

BIT 2: VDO BUS EN. When this bit is'0' access to the video bus is enabled. Writing a '1' to this bit disables access to the video bus.

Bit 3: This bit can be strapped to have one of two functions. The non-selected function can be strapped to '1' or '0', as required. (See Section 5.10).

IRQEN. When this bit is one, the QRGB-Graph's interrupt capability is enabled. When this bit is zero, the QRGB-Graph will be inhibited from generating an interrupt. This is the as-shipped function.

<OR>

DBLE RES. When this bit is one, bit planes 0 and 2 are multiplexed together and bit planes 1 and 3 are multiplexed together to provide twice the X-AXIS resolution. Note however, that the bits per pixel are halved, and that the use of two bit planes will affect how the colour look-up table is accessed (see section 4.3.11). When this bit is zero, resolution is normal and there are four independent bit planes. Note that the as-shipped look-up table does not support double resolution.

Bit 4: DMA. When this bit is one, the Display Memory can be accessed by DMA. All DMA transfers are made at the same 256 Byte block of system address space, the base address of which is set by straps (see Section 5.2). This system address space is mapped into different areas of the Display Memory before the block transfer by loading the X and Y Registers with the transfer's Display Memory starting address minus one. As the transfer proceeds, the X Register is automatically incremented before each byte transfer. The Y Register is automatically incremented before each 256 byte transfer or every 512 byte transfer, depending on a strap (see Section 5.12 - DMA Straps). If several blocks are sequentially transferred to or from contiguous Display Memory, the X-Y starting address need only be loaded before the first block transfer.

When bit 4 is zero the QRGB-Graph's Display Memory is accessed normally and the X and Y registers must be loaded with a new set of coordinates before each byte or word transfer.

4.3.5 CONTROL REGISTER NO. 1 (Cont'd):

Bit 5: FGC. When this bit is 0, the QRGB-Graph operates in continuous frame grab mode. If a frame grabber is connected, the board will continually grab and display sequential frames: in effect, it will display what the camera sees. When the bit is 1, the QRGB-Graph will freeze the frame that was in the display memory at the time the bit changed state. The user can watch the action, then freeze it.

Bit 6: BLINKEN. When this bit is one, blink is enabled. When this bit is zero, blink is disabled.

Bit 7: ALTMAP. When this bit is zero the "A" map set in the Colour Look-up Table is used. When this bit is one, the "B" map set is used. This bit is used in conjunction with Control Register 3 to enable alternate Look-up Table selection. (See Section 4.3.11)

Bit 8-10: XPAN0-XPAN2. These three bits are used in conjunction with the CRTC starting address registers (R12 and R14) to horizontally pan the display. XPAN0-XPAN2 can be set to delay the horizontal sync. pulse by 1 through 7 dots (see Table above). A pan is accomplished by sequentially incrementing this delay until it reaches 7 dots then resetting XPAN0-XPAN2 and incrementing the CRTC starting address registers during vertical blanking. This operation is repeated at a rate that will give the required pan speed.

Bit 11-13: XZOOM0-XZOOM2. These three bits are used in conjunction with several CRTC registers (R0, R1, R2, R3, R12, R13) to expand the display along the horizontal axis (see Section 4.4).

Bit 14-15: YZOOM0 and YZOOM1. These two bits are used in conjunction with several CRTC registers (R3, R4, R5, R6, R7, R9, R12, R13) to expand the display along the vertical axis (see Section 4.4).

APPLICATION NOTES:

1) For a normal display, X and Y zoom factors of one must be loaded.

2) X-zooms of greater than 4 are not possible when using the 256 x 256 format.

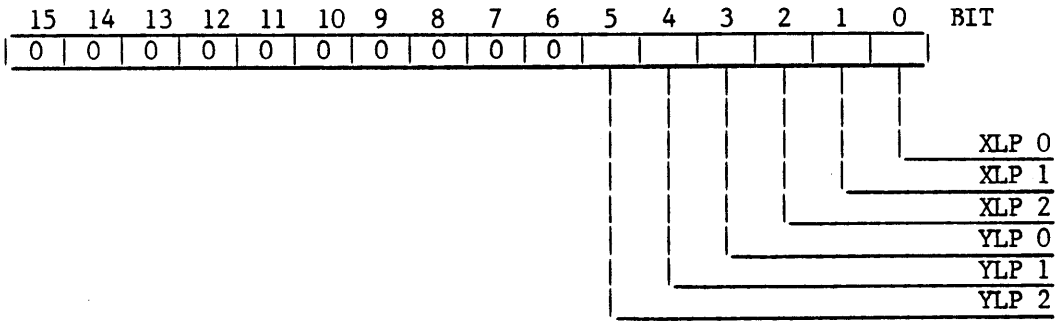
3) We suggest not zooming at 256 x 256 if you intend to pan at this resolution. Zooming at 256 x 256 will cause some minor disruptions in display RAM refresh that will be seen as a small amount of false data as the user pans outside of the currently visible display memory.

4.3.6 AUXILIARY LIGHT PEN REGISTER:

READ ONLY

BASE ADDRESS + 10_8 = | LOC. |

AS SHIPPED ADDRESS = 164410_8



Bits 0-2: XLP0-XLP2. These bits are the three least significant bits of the light pen X coordinate. The most significant bits are provided by CRTC-R17: bits 0-4 represent XLP3-XLP7 for 256 x 256 formats and bits 0-5 represent XLP3-XLP8 for 512 x 512 formats. Note that the data from CRTC-R17 must be shifted to the left three bits before they can be combined with XLP0-XLP2 from this register. Unused bits in CRTC-R17 are zero.

Bits 3-5: YLP0-YLP2. These bits are the three least significant bits of the light pen Y-coordinate. The most significant digits are provided by CRTC-R16: bits 0-4 represent YLP3-YLP7 for 256 x 256 formats and bits 0-5 represent YLP3-YLP8 for 512 x 512 formats. Note that the data from CRTC-R16 must be shifted three spaces to the left before it can be combined with YLP0-YLP2 from this register. Unused bits in CRTC-R16 are zero.

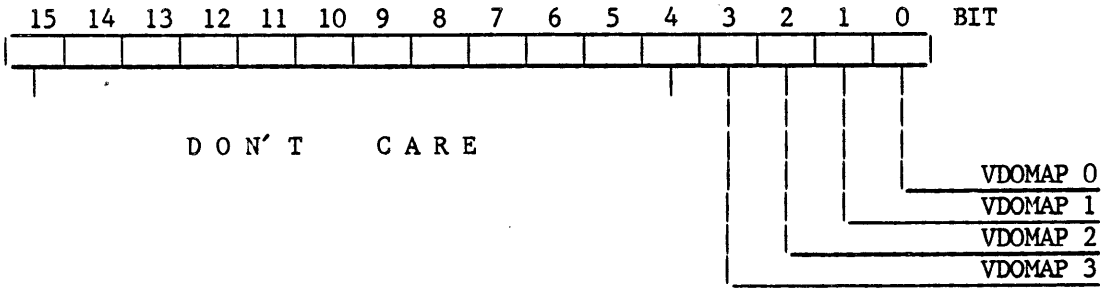
4.3.7 CONTROL REGISTER NO. 3 :

WRITE ONLY

LOC.

BASE ADDRESS + 10_8 = |_____|

AS SHIPPED ADDRESS = 164410_8



BITS 0-3: These bits, used in conjunction with ALTMAP (Control Register 1, Bit 7), select which colour map the bit planes will write to, as shown below (also see section 4.5). The four bits used can be strapped to any four bits shown in the I/O location shown above (see section 5.3), and must be strapped to the same four bits that are used by the data port. The as-shipped configuration is shown here. See Appendix 'D' for colours.

WHEN ALTMAP = 0: The following chart indicates which Colour Map is selected when a certain bit configuration is loaded into Control Register No. 3 :

COLOUR MAP SET 'A'				
VDO3	VDO2	VDO1	VDO0	LOOK-UP TABLE SELECTED
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

4.3.7 CONTROL REGISTER NO. 3 (cont'd):

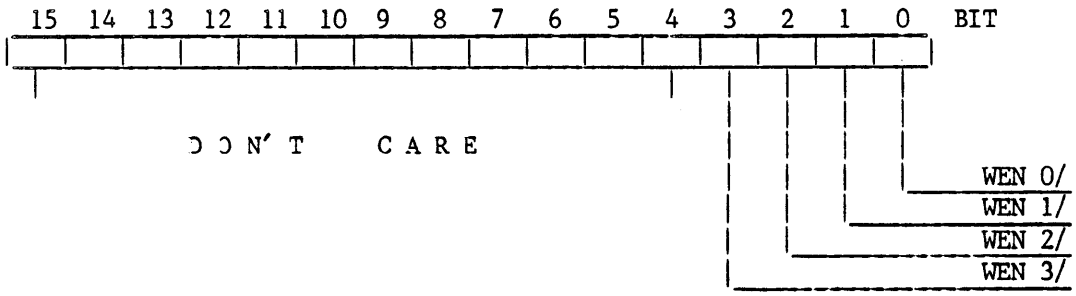
WHEN ALTMAP = 1: The following chart indicates which Colour Map is selected when a certain bit configuration is loaded into Control Register No. 3 :

COLOUR MAP SET 'B'				
VD03	VD02	VD01	VD00	LOOK-UP TABLE SELECTED
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
0	0	1	1	19
0	1	0	0	20
0	1	0	1	21
0	1	1	0	22
0	1	1	1	23
1	0	0	0	24
1	0	0	1	25
1	0	1	0	26
1	0	1	1	27
1	1	0	0	28
1	1	0	1	29
1	1	1	0	30
1	1	1	1	31

4.3.8 CONTROL REGISTER NO. 4:
WRITE ONLY

BASE ADDRESS + 12_8 = | LOC. |

AS SHIPPED ADDRESS = 164412_8



The four bits of Control Register No. 4 can be strapped to any four bits in the I/O locations shown above (see Section 5.3) and must be strapped to the same four bits that are used as the data port. The as-shipped configuration is shown here.

Bit 0: WEN0/. When this bit is zero, bit plane 0 can be written to. When this bit is one, bit plane 0 cannot be written to.

Bit 1: WEN1/. When this bit is zero, bit plane 1 can be written to. When this bit is one, bit plane 1 cannot be written to.

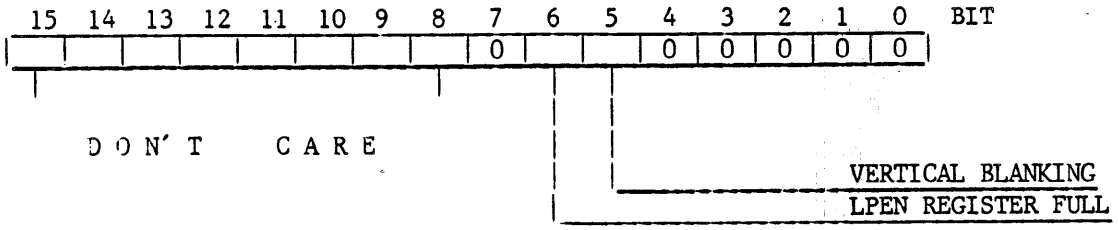
Bit 2: WEN2/. When this bit is zero, bit plane 2 can be written to. When this bit is one, bit plane 2 cannot be written to.

Bit 3: WEN3/. When this bit is zero, bit plane 3 can be written to. When this bit is one, bit plane 3 cannot be written to.

4.3.9 CRTC STATUS REGISTER:
READ ONLY

BASE ADDRESS + 14_8 = LOC. ____

AS SHIPPED ADDRESS = 164414_8

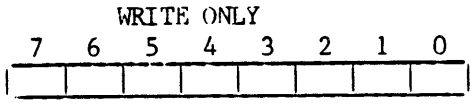


Bit 5: VERTICAL BLANKING. When this bit is one, the scan is in vertical blanking. When this bit is zero, the scan is not in vertical blanking. NOTE: When the QRGB-Graph is used as a pseudo-master or slave in any QRGB-Graph, QRGB-ALPHA or QVAF combination, Bit 5 is used as an internal control signal and indicator only, and is not intended to be a source of vertical blanking pulses to an external device. Externally useable blanking pulses can be obtained only from the master in any master-slave combination.

Bit 6: LPEN REGISTER FULL. This bit goes to one whenever a light pen strobe occurs. This bit goes to zero whenever either CRTC R16 or R17 are read.

4.3.10 CRTC ADDRESS REGISTER:

WRITE ONLY



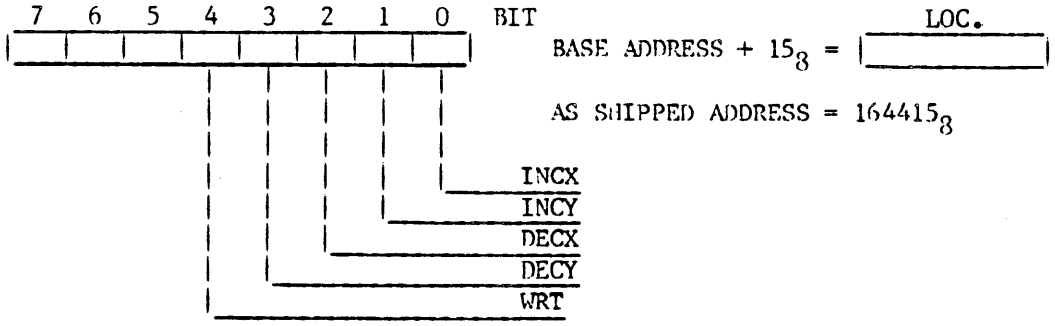
BASE ADDRESS + 14_8 = LOC. ____

AS SHIPPED ADDRESS = 164414_8

When one of the CRTC registers is to be accessed, its address is placed in this register, then data is input or output through the CRTC Data Register. Addresses and descriptions for the CRTC registers are found in the CRTC data sheets. Note that a word transfer to this register will affect the vector register and vice versa.

4.3.11 VECTOR REGISTER:

WRITE ONLY



BIT 0: INCX. When a one is written to this bit, the X-Register is incremented. Writing a zero to this bit has no effect on the X-Y coordinates.

Bit 1: INCY. When a one is written to this bit, the Y-Register is incremented. Writing a zero to this bit has no effect on the X-Y coordinates.

Bit 2: DECX. When a one is written to this bit, the X-Register is decremented. Writing a zero to this bit has no effect on the X-Y coordinates.

Bit 3: DECY. When a one is written to this bit, the Y-Register is decremented. Writing a zero to this bit has no effect on the X-Y coordinates.

Bit 4: WRT. When this bit is zero, the contents of the Data Register are automatically written to the Display Memory when the Vector Registor is loaded. When this bit is one, data is not automatically written to the Display Memory when the Vector Register is loaded.

NOTE: The Vector Register will not function properly if the QRGB-Graph is in DMA mode.

Figure 5-1 shows the direction that the graphics trace will take when different values are written to the Vector Register.

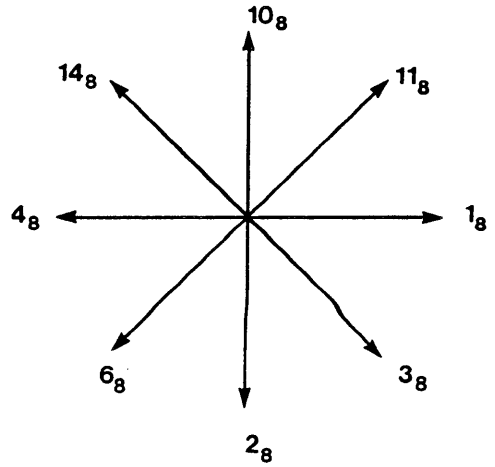
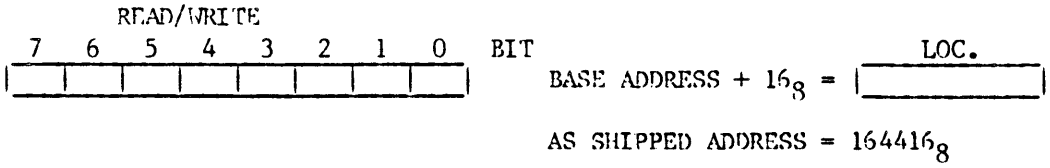


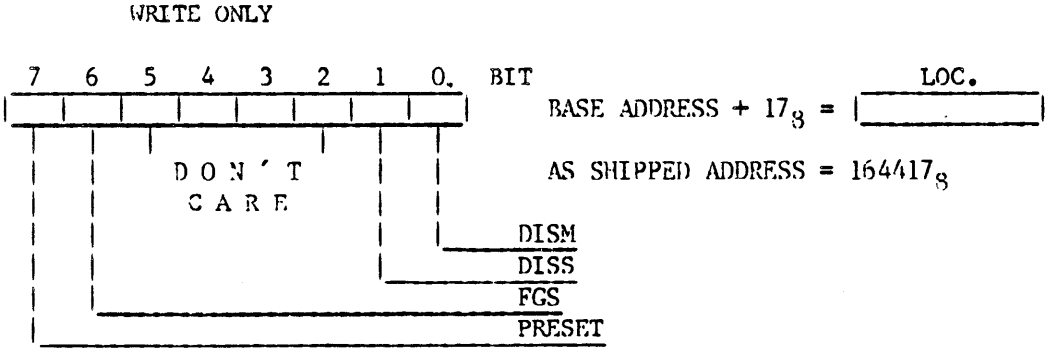
Figure 4.1 - VECTOR DIRECTION (BIT 0-3)

4.3.12 CRTC DATA REGISTER:



This location is the data port to and from the CRTC.

4.3.13 CONTROL REGISTER NO.5:



BIT 0: DISM. When two or more QRGB-Graph boards are arranged in a master-slave configuration this bit is used to disable access to the master's CRTC so that the slave's CRTC can be independently programmed. The byte containing the bit is outputted as the most significant byte in a word transfer where the least significant byte is the data going to the slave's CRTC. If DISM is '1', access to the master's CRTC is disabled.

BIT 1: DISS. The bit has a similar function to DISM; however it disables access to the slave's CRTC so that the master's CRTC can be independently programmed. It is outputted in the same way as DISM and when it is '1' it disables access to the slave's CRTC during the current transfer.

BIT 6: FGS. This is one of two register bits used for frame grabbing operations (also see FGC in section 4.3.8). If a '1' is written to FGS the QRGB-Graph will 'grab' and hold a single frame of video information. It will continue to display that information until '1' is again written to FGS, at which time a new frame will be grabbed. If a zero is written to this bit it will have no effect.

BIT 7: PRESET. When a '1' is written to this bit, the part of the Display Memory currently appearing on the screen is preset to the value in the Data Register. If a zero is written to this bit, it has no effect. See Section 4.5.4. Note that since a preset is performed on a cell level rather than a pixel level the entire visible display may not be preset if Zoom & Pan bits are not all set to '1'. See Section 4.3.8.

4.4 THE ZOOM FUNCTION:

The zoom function allows the user to select a portion of the display and enlarge it to replace the original image from which it was taken. Resolution in the enlarged section is not affected, since it contains the same number of pixels before and after the zoom. Horizontal expansion (X-zoom) and vertical expansion (Y-zoom) are independently controlled by the user. It can be expanded horizontally by factors of 2, 3, 4, 5, 6, 7, and 8 in the 512 x 512 and 512 x 256 formats, and by 2, 3, and 4 in the 256 x 256 format. Since identical horizontal and vertical zoom factors are required to maintain correct image proportions, the horizontal zoom factors of 2 and 4 are the most useful. The remaining horizontal zoom factors should not, however, be ignored since they can be used for controlled distortion of an image.

When considering the zoom function, the display should be considered as a field of graphics cells, each of which is composed of 8 x 8 pixels in a normal resolution display or 16 x 8 pixels in a double resolution display.

The number of these cells in the display depends on the format used: 32 columns by 32 rows for the 256 x 256 format; 64 columns and 32 rows for the 512 x 256 format and 64 columns and 64 rows for the 512 x 512 format. The zoom window (the area to be enlarged) is defined in terms of these cells. Integer values must be used.

The size of the zoom window should be selected so that the actual display is the same size before and after the zoom. The post zoom display can, if necessary, be smaller; however, if it is larger, it will most likely overshoot the CRT and there may be problems programming the CRTC. The best way to determine the size of the zoom window is to divide the times one format X and Y axes, in cells, by the zoom factors to be used. If the result is not an integer value, choose the next lower integer. For example, if a times two X and Y zoom was made into the display of a QRGB-Graph at 512 x 512 (64 x 64 cells), the area to be enlarged would be 32 cells x 32 cells. If a distorting zoom of 4 times on the Y axis and 3 on the X axis was made into the same display, the area to be enlarged would be 21 cells (X-axis) by 16 cells (Y-axis). Table 4.2 gives the sizes, in cells, of zoom windows to be enlarged for X-Y zooms of 2 and 4.

FORMAT	256 x 256		512 x 256		512 x 512	
AXIS	X	Y	X	Y	X	Y
TIMES 2	16 Cells	16 Cells	32 Cells	16 Cells	32 Cells	32 Cells
TIMES 4	8 Cells	8 Cells	16 Cells	8 Cells	16 Cells	16 Cells

Figure 4.2 - THE MOST USED ZOOM WINDOW SIZES.

When doing a zoom, the user first decides the X and Y zoom factors to be used, and then, knowing the times 1 format, he determines the size of the zoom window. He then places an imaginary frame the size of the zoom window around the part of the image to be enlarged. The row and column numbers of the cell in the upper left hand corner of that frame are then written to CRTC register R12 and R13 respectively. Finally, the zoom factors are written to Control Register No. 1 (see Section 4.3.8) and the format parameters in the CRTC Registers are adjusted to accommodate them. This adjustment is necessary because the Dot Clock depends on the X-zoom factor and the number of scan lines per pixel depends on the Y-zoom factor.

4.4 THE ZOOM FUNCTION (Cont'd):

Tables 4.3 and 4.4 show the register values for most zooms. All parameters are in OCTAL.

HOR. FORMAT (X)		256				512			
HOR. ZOOM		1	2	4	8	1	2	4	8
AMERICAN/EUROPEAN *		50-60Hz	50-60Hz	50-60Hz	50-60Hz	50-60Hz	50-60Hz	50-60Hz	50-60Hz
X-ZOOM**	CR#1	034000	030000	020000	000000	034000	030000	020000	000000
HOR. TOTAL	R0	047	023	011	004	117	047	023	011
HOR. DISP.	R1	040	020	010	004	100	040	020	010
HOR. SYNC. POS.	R2	041	020	010	004	103	042	021	010
V. & H. SYNC. WIDTH	R3	064	063	061	061	066	062	061	061

* Parameters are the same for both American & European.
**Control Register #1 = Y Zoom + X Zoom + 3442

Table 4.3 - FORMAT PARAMETERS FOR X-AXIS ZOOMS.

VERT. FORMAT (Y)		256						512					
VERT. ZOOM		1		2		4		1		2		4	
American/European (HZ)		60	50	60	50	60	50	60	50	60	50	60	50
Y ZOOM*	CR#1	000000		40000		100000		000000		40000		100000	
VERT. TOTAL	R4	037	046	017	022	007	010	077	112	037	046	017	022
VERT. ADJ.	R5	004	000	004	010	004	030	004	000	004	000	004	010
VERT. DISP.	R6	036	040	017	017	007	007	074	100	036	036	016	020
VERT. SYNC. POS.	R7	036	042	017	021	007	010	074	102	036	042	016	021
MODE	R8	004	004	004	004	004	004	007	007	007	007	007	007
SCAN LINE	R9	007	007	017	017	037	037	007	007	017	017	037	037

* Control Register #1 = Y-ZOOM + X-ZOOM + 3442

Table 4.4 - FORMAT PARAMETERS FOR Y-AXIS ZOOMS.

EXAMPLE: For a Zoom of 4X x 2Y at 256 x 256 and 60 HZ, a horizontal format of 256 x 4 and a vertical format of 256 x 2 is required. Reading from the previous tables gives:

CR #1 = 040000 + 020000 + 3442
= 063442

R0 = 011 R1 = 010
R2 = 010 R3 = 061
R4 = 017 R5 = 004
R6 = 017 R7 = 017
R8 = 004 R9 = 017

Figure 4.3 represents a 256 x 256 display and shows three areas (A, B and C) that might be zoomed into using X and Y zoom factors of 4. Note that where the zoom window overshoots the display it wraps around:

4.4 THE ZOOM FUNCTION (Cont'd):

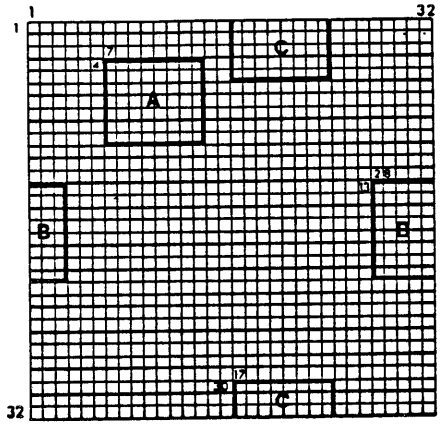


Figure 4.3 - TYPICAL ZOOM AREAS IN A 256 X 256 FORMAT.

NOTE that it is not possible to zoom when the QRGB-Graph is used with a QRGB-Alpha in Slave Mode. Please contact us if your application requires this function.

4.5 COLOUR LOOK-UP TABLE:

As described in section 2.3, the QRGB-Graph contains a Colour Look-up Table EPROM divided into 32 Colour Maps of up to 16 colours each; this section describes the utilization of the maps in a Normal fashion or with Blink or Overlay. It also gives guidelines on how to create your own map set and how the DAC/Colour outputs will respond to the bit patterns emerging from it. Also, there are considerations regarding Single and Double resolution and the auxiliary output (TTL) that will be mentioned as they apply to the Look-Up Table.

4.5.1 COLOUR MAP ACCESS:

The Colour Look-up Table can be viewed as a universal set with two levels of subsets; the first being a 'Map Set' which is selected by a Control Register bit (ALTMAP) the second being a 'Colour Map', which is selected by four bits in another Control Register (VDOMAP), with the element being the colour itself which is selected by the Bit Planes. All accesses, Normal, Overlay, or Blink, are achieved in the same way: through selections among the elements or subsets which make up the Look-Up Table.

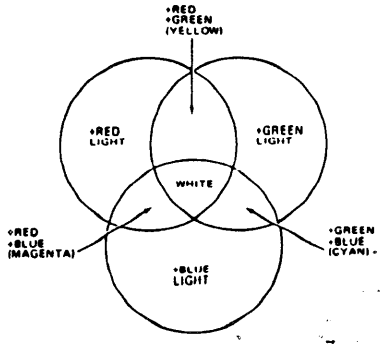
The colour generated by each Bit Plane configuration with the as-shipped EPROM can be determined by referring to the tables in Appendix D. For example, one way to display a red diagonal line on a black background would be the following (all numbers are octal):

DATA	LOCATION	RESULT
000000	164404	Zero Data Register
010037	164414	Reset Display to Zero (Black)
101000	164416	
037442	164406	Select Map Set 'A'
000002	164410	Select Colour Map #1
000001	164404	Select Colour (Red)
000000	164400	Zero X Register
000000	164402	Zero Y Register
001437	164414	Load Display Memory & Draw Line.

4.5.1 COLOUR MAP ACCESS(cont'd):

Normal with Extended Resolution - Note that the two highest order bits (Bit Planes 2 and 3) are not available for colour selection during Extended Resolution so that all colours selected must fall within the two lowest order bits (first and second Bit Planes). This will limit the colours available from any one Colour Map to four. Note that the as-shipped EPROM does not support double resolution.

Normal with TTL Output - The TTL outputs utilize the Look-Up table, but only saturated primary colours are sent to them. Referring to Table 4.5, the red output is activated by RED1, the blue is activated by BLUE2, and the green is activated by GREEN2, yielding a choice of seven colours (3 saturated primarys and four additives) as shown below.



4.5.2 BLINK

The QRGB-Graph has a feature which allows pixels to be blinked between different colours if the colour map is programmed accordingly. The data from the fourth bit plane is ANDed with a low frequency square wave that can be enabled by Bit 6 (BLINKEN) of Control Register No. 1. When it is enabled, any '1' in the fourth Bit Plane will be periodically switched to zero by the square wave causing a change in the Colour Map address. If different colours are in the two locations addressed in this way (Bit 4 = 1 and Bit 4 = 0) a blink will result. Pixels with zero in the fourth bit plane will obviously not be able to blink since the square wave blink frequency can not change their state.

MAP	BIT PLANE [3210]	COLOUR
MAP 12	0xx0	BLACK
	1xx0	DARK GREEN
	0xx1	RED
	1xx1	BROWN

FIGURE 4.5 - COLOUR MAP 12.

Figure 4.5 shows the contents of Colour Map number 12 which we will use here to illustrate how Blink functions. If 1XX1 was written to a given pixel that pixel would appear brown on the display until blink was enabled (BLINKEN) then it would blink back and fourth between brown and red. Similarily writing 1XX0 to a pixel would allow blinking between dark green and black. Note, however, that the Blink function has no effect on 0XX1 or 0XX0 since the blink frequency can not change the state of the zero in the fourth Bit Plane.

4.5.2 BLINK (cont'd):

Blink with Extended Resolution - Note that blink can not be implemented with the Extended Resolution function (Control Register No. 1, Bit 3) since the fourth Bit Plane is multiplexed onto the line from the second Bit Plane, and the position normally occupied by the fourth Bit Plane is taken low.

4.5.3 OVERLAY (Superimposing an image or text on selected areas of a display):

Overlay can be done in the QRGB-Graph by using the fourth bit plane as a separate image generator. The first three bit planes are used to generate the colour image while the fourth bit plane can be written to separately by disabling 'write' in the other three (via Control Register 4). The standard PROM does not support overlay, but the user can easily program a map to perform this function, as shown below:

CREATING AN OVERLAY MAP

1) Determine which map will be used for overlay.

EXAMPLE: We'll choose MAP 15, since it contains a good selection of colors, and does not use Bit Plane 4, which we are using here for overlay.

MAP 15	x000	BLACK
	x100	GREEN
	x010	BLUE
	x110	DARK CYAN
	x001	RED
	x101	BROWN-GREEN
	x011	MAGENTA
	x111	WHITE-PURPLE

Figure 4.6 - MAP 15.

2) Select the overlay color.

EXAMPLE: We'll select white, which is the most common color for text. White, by the way, is binary 1111 1111 when coded in the look-up table.

3) Copy the selected map to the area of ROM reserved for the user.

EXAMPLE: We'll copy MAP 15, which resides at $F0_H$ to FF_H, to the locations $1F0_H$ to $1F7_H$. Note that we are only copying the first eight bytes of MAP 15, which contains the colors we need.

4.5.3 OVERLAY (Cont'd)

4) Write the selected overlay color to all bytes of the new map in which bit plane 4 is significant (the 8 highest bytes).

EXAMPLE: Our selected overlay color is white (Binary 1111 1111) so we'll write FF_H to locations $1F8_H$ to $1FF_H$. The resulting map will look like this:

OVERLAY MAP 15		
	x000	BLACK
	x100	GREEN
	x010	BLUE
	x110	DARK CYAN
	x001	RED
	x101	BROWN-GREEN
	x011	MAGENTA
	x111	WHITE-PURPLE
	1xxx	WHITE

Figure 4.7 - AN OVERLAY MAP.

5) The overlay map can now be used by writing '1' to ALT MAP (Control Register 1, Bit 7), and writing '1111' to control Register 3. Note that using map 15 with ALTMAP = 0 will allow overlayed text in black, which may be useful for writing text over large areas filled with a light colour.

Referring to the contents of Overlay MAP 15 (in figure 4.7, above), it will be seen that writing a '1' to a pixel position on the fourth bit plane will generate a white pixel irrespectively of the contents of the other bit planes, and that writing a '0' to the fourth bit plane will permit the original pixel colour to re-appear, thus allowing pointers, alphanumeric text, or labels to be inserted or deleted without disturbing the original image. Note that the example given allows an overlayed image in white, but in reality any colour could have been chosen. Furthermore, the user does not have to copy a color map that already exists. Any combination of colors could be written into a user map and used as an overlay map, providing the fourth bit plane is not used for any colour except the overlay colour. The table below gives the codes (in hex) for some of the most commonly used colors:

COLOR	CODE	COLOR	CODE
BLACK	00	RED	07
BLUE	18	MAGENTA	1F
GREEN	20	BROWN-GREEN	27
DARK CYAN	38	WHITE-PURPLE	3F
BROWN	C7	LIGHT MAGENTA	DF
LIGHT GREEN	E0	YELLOW-GREEN	E7
LIGHT CYAN	F8	WHITE	FF

TABLE 4.5 - COLOR CODES.

4.5.3 OVERLAY (Cont'd):

Overlay with Extended Resolution - Note that as in the Blink function, Overlay can not be used when the board is operating in Double Resolution since the fourth bit plane is used to extend the resolution of the second bit plane, hence is unavailable for other purposes.

4.5.4 BIT PLANE PRESET:

Using the preset function (C.R. #5, Bit 7) on the QRGB-Graph will allow any bit plane(s) to be rapidly initialized to zero or one. This happens within one television frame, but it can cause a brief disruption which will sometimes make the screen flash. To preset a bit plane without flashing the screen, the bit plane should be prevented from addressing the look-up table while it is being preset. The way to do this is to write '0' to the bit plane that is to be preset, via Control Register 3. The following example ilustrates how to clear the fourth bit plane of overlayed text:

1) Write '0' to VDOMAP3 (C.R. #3, BIT3). This inhibits bit plane 3 from accessing the look-up table.

2) Write '0111' to C.R. #4. This allows Bit Plane 3 to be written to, and prevents writing to Planes 0 to 2.

3) Write '0' to Bit 3 of the Data Register. This is the value to which Bit Plane 3 is to be preset.

4) Write '1' to Bit 7 of Control Register #5. This clears Bit plane 3 to '0'. Not that this register is byte-wide, and must be treated differently from the others. See Appendix F before writing to this Register.

4.5.5 CUSTOM COLOUR MAPS:

The QRGB-Graph permits the use of custom Colour Maps that can be created by the user to fulfill certain functions that might be desired such as varicoloured overlay, different hues, or variable levels of colour saturation. The following text describes how the Colour Map locations are translated into analog displays, and mentions considerations regarding the colour locations with respect to the Look-Up Table. It also gives examples of special-purpose Colour Maps that can be exploited for different effects on the screen. Particulars regarding the actual programming of the Look-Up Table will vary with the type of chip chosen, therefore it is recommended that the user refer to the chip manufacturer's data sheets for this information. The as-shipped Look-Up Table is an MM16349-1 or TBP 28542 512 X 1 byte memory with a worst-case access time of 70 nanoseconds and a worst-case enable time of 35 nanoseconds, and it is important that a PROM with these characteristics or better are chosen. The first byte of the user area of the as-shipped PROM is at 400_8 (256_{10}, 100_H).

4.5.5 CUSTOM COLOUR MAP (Cont'd):

Each location in the Look-Up Table EPROM contains a byte configuration that is read in parallel by the Digital-Analog convertor. Each colour channel in the D/A convertor reads a different portion of this byte and determines its own colour intensity by means of the binary value of the bits presented to it. If a colour channel reads a '1' in every bit position assigned to it, it will deliver maximum intensity (a fully saturated primary colour) to the colour output it is connected to. If a colour channel reads a '0' in every bit position assigned to it, it will deliver zero intensity (no colour, black) to its colour port. All intermediate levels of intensity are determined by the magnitude of the binary number presented to the DAC channel, and the number of intensity levels possible are determined by the number of output bits of the colour table the DAC channel is connected to: Number Of Intensity Levels = 2**N, where N is the number of bits to which the colour channel is connected. The red channel reads three bits from the table, the blue reads two, and the green channel reads three, yielding intensity increments of 8 for the red, 4 for the blue, and 8 on the green channels, respectively. There is also a fourth channel that reads the lowest order bit of the red and blue, and the lowest and highest order bits of the green channel, to give a grey scale video output with 16 levels of intensity.

MEMORY BIT (Q)	COLOUR INTENSITY BIT(RGB)	GREY SCALE BIT(GS)
Q1 (LSB)	RED3 (MSB)	GS4 (MSB)
Q2	RED2	
Q3	RED1 (LSB)	
Q4	BLUE1 (LSB)	GS3
Q5	BLUE2 (MSB)	
Q6	GREEN3 (MSB)	GS2
Q7	GREEN2	
Q8 (MSB)	GREEN1 (LSB)	GS1 (LSB)

TABLE 4.6 - COLOUR TABLE OUTPUT VS. GENERATED COLOUR.

It can be seen from the above table that whatever is written to each row (1 byte wide) of the Colour Table will be displayed as a set of colours of various intensity levels and it is this mix, by addition, of the three primary colours, presented to the CRT screen, that is the source of 256 different colours as described in Section 2.3.

Since the Look-Up Table has few limitations regarding its configuration, its flexibility can be exploited in many ways provided that the convention described in Section 4.5 regarding the addressing of the subsets and elements is observed. An example of a non-standard configuration that can permit varicoloured overlay would be six Colour Maps, each programmed with nine colours, identical except for the last colour in each map (determined by the fourth bit plane). Using the Overlay function as described previously within one map would give a single colour overlay, but selecting between the six members of the map set would, in this case, provide a choice of six overlay colours without disturbing the background image. It should be noted that this would not provide a multicoloured overlay, but would allow the one overlaid colour selected to be changed as desired.

* * * * *

5.0 STRAPS:

Strap options on the QRGB-Graph are implemented by interconnecting numbered wire wrap pins. In this manual, straps between wire wrap pins are referred to as follows:

14-15 IN indicates that wire wrap pin 14 is connected to wire wrap pin 15.
14-15 OUT indicates that wire wrap pin 14 is not connected to wire wrap pin 15.
14<-->15 indicates that wire wrap pin 14 is connected to wire wrap pin 15.

If the QRGB-Graph is to be combined with any other board in a Master-Slave configuration be sure to read the applicable Sections 4.3.18, 5.6, 5.8, 5.12, & 9.

5.1 I/O BASE ADDRESS STRAPS:

The following straps control the position of the I/O window in the system address space. All bits below DAL 4 are used for Register Select, and are 'don't care' during I/O addressing.

ADDRESS BIT	DAL 8	DAL 7	DAL 6	DAL 5	DAL 4
STRAP '0'	81-85 IN	80-85 IN	82-85 IN	83-85 IN	84-85 IN
STRAP '1'	81-85 OUT	80-85 OUT	82-85 OUT	83-85 OUT	84-85 OUT

Table 5.1 - I/O BASE ADDRESS STRAPS.

The following as-shipped strap configuration gives an I/O base address of 164400 (octal) : 81-85 OUT, 80-85 IN, 82-85 IN, 83-85 IN, 84-85 IN.

Note that if a bit is not strapped, it is set high ('1'). If a bit is strapped to pin 85 it is taken low ('0').

5.2 DMA BASE ADDRESS STRAPS:

The following straps control the position of the 256 byte DMA window in the system address space (within a 512 byte boundry). All bits above DAL 12 are high by default:

ADDRESS BIT	DAL 12	DAL 11	DAL 10	DAL 9
STRAP '0'	60-62 IN	58-62 IN	59-62 IN	61-62 IN
STRAP '1'	60-62 OUT	58-62 OUT	59-62 OUT	61-62 OUT

Table 5.2 - DMA BASE ADDRESS STRAPS.

The following as-shipped strap configuration gives a 256 byte DMA address of 164000 (octal): 60-62 IN, 58-62 OUT, 59-62 IN, 61-62 IN.

Note that if a bit is not strapped, it is set high ('1'). If a bit is strapped to pin 62 it is taken low ('0').

Note also that the DMA window and the I/O window are contiguous. This means that a change to one will result in a change to the other, and may produce unexpected results. Read Section 5.1 before altering the above strap configuration.

5.3 STRAPS FOR DATA AND CONTROL REGISTERS 3 AND 4:

Table 5.3 shows how the QRGB-Graph's 4-bit I/O port can be strapped to any 4-bit nibble in the LSI-11 data bus. Bits 0-3 of Control Register 3 and 4 must be strapped to the same Q-BUS data lines used by bits 0-3 of the data port.

REGISTER BIT	PIN	AS-SHIPPED STRAPS	PIN	BUS DATA BIT
VDOMAP 0	36		55	BDAL0 L
WEN 0			51	BDAL4 L
DATA 0			45	BDAL8 L
			41	BDAL12 L
VDOMAP 1	37		54	BDAL1 L
WEN 1			50	BDAL5 L
DATA 1			44	BDAL9 L
			40	BDAL13 L
VDOMAP 2	46		53	BDAL2 L
WEN 2			49	BDAL6 L
DATA 2			43	BDAL10 L
			39	BDAL14 L
VDOMAP 3	47		52	BDAL3 L
WEN 3			48	BDAL7 L
DATA 3			42	BDAL11 L
			38	BDAL15 L

Note: The configuration above is for a Master or a single board. In a Master-Slave system Slave #1 should have 36-51 IN, 37-50 IN, 46-49 IN, 47-48 IN instead of the above.

Table 5.3 - DATA AND MASK REGISTER STRAPS.

The nibble selected must be completely within either the high byte or the low byte, and depending on which byte it occupies one of the two following two strap configurations must be implemented.

DATA PORT IN LOW BYTE (AS-SHIPPED) = 90-89 IN.
DATA PORT IN HIGH BYTE = 90-91 IN.

For Data Port assignment in a Master-Slave situation see Section 5.12 - Master-Slave Groupings.

5.4 FRAME GRAB STRAPS:

Each of the QRGB-Graph's bit planes can be strapped to any of the 8 data lines on the video bus (J4). Table 5.4 shows the appropriate connections.

BIT PLANE	PIN	AS-SHIPPED STRAPS	PIN	J4-PIN
0	144		143	29
			145	33
1	158		157	30
			159	34
2	130		129	31
			131	35
3	123		122	32
			124	36

Table 5.4 - FRAME GRAB STRAPS.

None of these straps are installed when the board is shipped.

5.5 TTL VIDEO STRAPS:

The QRGB-Graph's 4 TTL video signals can be strapped on any one of the 16 lines on the video bus (J4). Table 5.5 shows the wire wrap pins used to accomplish this.

TTL VIDEO	PIN	AS-SHIPPED STRAPS	PIN	J4 PIN
0	128		135	12
			137	16
			139	20
			141	24
1	127		149	13
			151	17
			153	21
			155	25
2	126		136	14
			138	18
			140	22
			142	26
3	125		150	15
			152	19
			154	23
			156	27

NOTE: the above straps are for a master. A slave board would have 128-137 IN, 127-151 IN, 126-138 IN, 125-152 IN instead of the above.

Table 5.5 - TTL VIDEO STRAPS.

5.6 SYNC AND BLANKING STRAPS:

Table 5.6 shows how the horizontal and vertical sync. and blanking (positive or negative) can be connected to J2 and J4. The as-shipped configuration is shown below:

SOURCE	PIN		PIN	DESTINATION
H. SYNC	100	<------->	101	J2 PIN 1
H. SYNC/	102			
V. SYNC	103	<------->	104	J2 PIN 9
V. SYNC/	105			
H. SYNC/	132	<------->	146	J4 PIN 8 *
V. SYNC/	133	<------->	147	J4 PIN 9 *
C. BLANK/	134	<------->	148	J4 PIN 10*
NOTE: Straps must not cross any horizontal lines in the center column.				

* connections marked with an asterix must be out on the slave board(s).

Table 5.6- SYNC AND BLANKING STRAPS.

5.7 VECTORED INTERRUPT STRAPS:

Vectored interrupts can be initiated by the QRGB-GRAPH by strapping 167-168 IN (as-shipped). This strap should be removed and 168-169 IN and 170-169 IN should be installed if a vectored interrupt is not required. For addresses of 400 (octal) or higher the high order bit (172-173 IN, as-shipped) should also be installed.

Table 5.7 shows how the address of a vectored interrupt to the host computer can be changed. Note that the two lowest order bits (DAL0, DAL1) are hard-wired low so that any address selected will be aligned on an even four address boundry.

ADDRESS BIT	DAL 8	DAL 7	DAL 6	DAL 5
STRAP '0'	172-173 OUT	27-34 IN	25-32 IN	23-30 IN
STRAP '1'	172-173 IN	27-34 OUT	25-32 OUT	23-30 OUT

Table 5.7(a) - VECTORED INTERRUPT STRAPS.

ADDRESS BIT	DAL 4	DAL 3	DAL 2	DAL 1-0
STRAP '0'	22-29 IN	24-31 IN	26-33 IN	LOW
STRAP '1'	22-29 OUT	24-31 OUT	26-33 OUT	LOW

Table 5.7(b) - VECTORED INTERRUPT STRAPS.

The following straps (as-shipped) enable the QRGB-Graph to provide an interrupt vector address of 400(octal) for the CPU : 26-33 IN ; 24-31 IN; 22-29 IN; 23-30 IN; 25-32 IN; 27-34 IN; 172-173 IN (high order bit).

5.8 MASTER-SLAVE STRAPS:

The straps given in table 5.8 are used to configure the QRGB-Graph as a master, a pseudo master, or a slave. Straps 98-99 must be out when the QRGB-Graph is not paired with another device (see section 9). When shipped, the QRGB-Graph is configured as a master, except for straps 98-99 which must be OUT when the board is used alone. Also see Sections 4.3.18, 5.12, & 9.

STRAP	109-108	107-106	98-99	88-87	87-86
FUNCTION	SCLK	CCLK	V.RESET/	XYCLK/	XYCLK/
MASTER	IN	IN	IN	IN	OUT
PSEUDO MASTER	OUT	IN	OUT	IN	OUT
SLAVE	OUT	OUT	OUT	OUT	IN

Table 5.8(a)- MASTER-SLAVE STRAPS.

STRAP	148-134	147-133	146-132	161-160	161-162	182-183
FUNCTION	C.BLAK/	V.SYNC/	H.SYNC/	CS/	CS/	CRTC RES\
MASTER	IN	IN	IN	IN	OUT	IN
PSEUDO MASTER	IN	IN	IN	IN	OUT	IN
SLAVE	OUT	OUT	OUT	OUT	IN	OUT

Table 5.8(b)- MASTER-SLAVE STRAPS.

5.9 LIGHT PEN/PRESET MEMORY STRAPS:

If the following straps are installed, a light pen hit or a preset memory command will generate a hardware interrupt to the CPU (shown as-shipped).

166 - 165 IN LPEN. Interrupt
163 - 164 IN PREMEM. Interrupt

5.10 INTERRUPT/RESOLUTION SELECT STRAPS:

The following strap configurations will determine the control aspect of Control Register No. 1, Bit 3; and also the Interrupt and Resolution functions of the QRGB-Graph.

SOURCE	PIN	STRAP	PIN	FUNCTION
+5V	176			
REG1 BIT3	177		175	DBLE. RES.
GND.	174			
+5V	181			
REG1 BIT3	178		180	IRQEN. (interrupt)
GND.	179			

TABLE 5.10 - INTERRUPT/RESOLUTION SELECT STRAPS (as-shipped).

Note that only one of the above functions can be controlled by software at a time. If one is software controlled, the other must be strapped. +5V will enable the function, GND will disable the function, and REG1 BIT3 will implement software control. If double resolution is to be selected, strap 119-120 OUT, 120-121 IN.

5.11 REGISTER READ DISABLE STRAPS

When more than QRGB-Graph is used in a Master/Slave configuration it is necessary, on all but the Master, to disable read access from all registers except the Data Register. This is done by installing the straps shown below:

REGISTER ACCESS(as-shipped): 17-16 OUT, 13-12 IN, 11-10 IN, 15-14 IN (Master/1 board).

DATA REGISTER ONLY: 17-16 IN, 13-12 OUT, 11-10 IN, 15-14 IN. (Slave)

5.12 MISCELLANEOUS STRAPS

The following straps will usually not need to be changed by the user, but are described here for completeness. The straps labelled `as shipped' are IN when the board is shipped. To alter the strap configuration remove the as-shipped straps and install the alternate configuration:

Format Select Straps:

20-18	256 x 256
20-21	512 x 256
20-19	512 x 512 (as shipped)

These straps are used to set the maximum display format.

Refresh Rate Straps (as shipped):

66-65	IN
67-68	IN
63-64	IN
56-57	IN

These straps are used to set a 128 cycle refresh rate for the 64K RAMs.

Master-Slave groupings:

The following straps are used to set the address space when more than two QRGB-Graphs are used in a group.

Boards #1 and #2 (as shipped):

78-79	IN
90-89	IN
93-92	IN

Boards #3 and #4:

78-77	IN
90-91	IN
93-94	IN

5.12 MISCELLANEOUS STRAPS (cont'd):

DMA Straps:

These straps affect DMA transfers as follows:

96-97 IN	Increment Y-Register before every 256 transfers.
96-95 IN	Increment Y-Register before every 512 transfers.

System Clock Alteration:

109-108 IN	Format of up to 512 x 512 with Software Zoom (as shipped)
109-110 IN	Format of 256 x 256 with 2 x 2 zoom (half speed system clock)

Test Point:

171	This is a factory installed test point and should not be connected to any other point on the board.

* * * * *

6.0 CIRCUIT DESCRIPTION:

The following circuit description should help the user to understand some of the more involved sections of the QRGB-Graph's logic. While reading it the user should refer to the schematics at the back of this manual. Where more than one gate is found in an IC, individual gates are referred to by their output pin: thus A10-1 is the gate in A10 that has its output at pin 1 of the IC package.

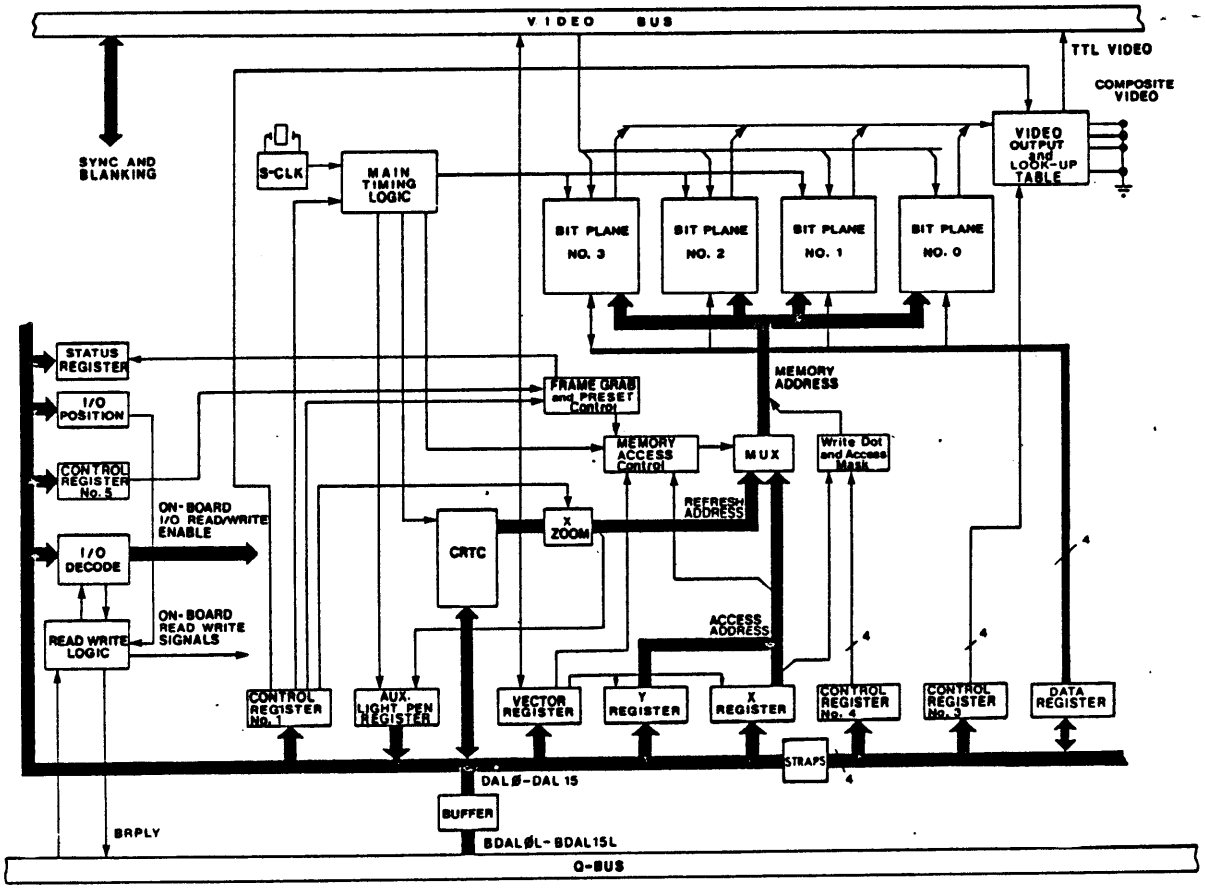


Figure 6.1 - BLOCK DIAGRAM OF QRGB-Graph.

6.1 BIT PLANE:

Figure 6.2 is a block diagram of bit plane zero and its associated data access chips. The QRGB-Graph will have up to four circuits like this (depending on the model selected). The display memory for each bit plane is composed of four RAMs. When the memory is read; all four RAMs are accessed simultaneously (providing four bits corresponding to four consecutive pixels in the display). If the access is part of a display refresh operation, the four bits are latched into A112, then loaded into A114 and shifted out as serial video data. If the access is a read to the Q-BUS, multiplexer A113 allows only the bit addressed by X0 and X1 from the X-Register to go to the data port register (A116). Data enters the bit plane via the multiplexer A115 which selects either the Data Register or the frame grabber port as the data source. When the source is the Data Register, the data bit is presented to the inputs of all four RAMs and only the write enable line of the RAM containing the bit's destination is activated (see section 6.5). When the source is the frame grabber port, incoming serial data is first converted to parallel data in the right half of A114, then four bits are simultaneously written into the bit plane: one bit to each of the RAMs. Note that when the QRGB-Graph is operating in continous frame grab mode, the video data also continues through A114 to the video output section.

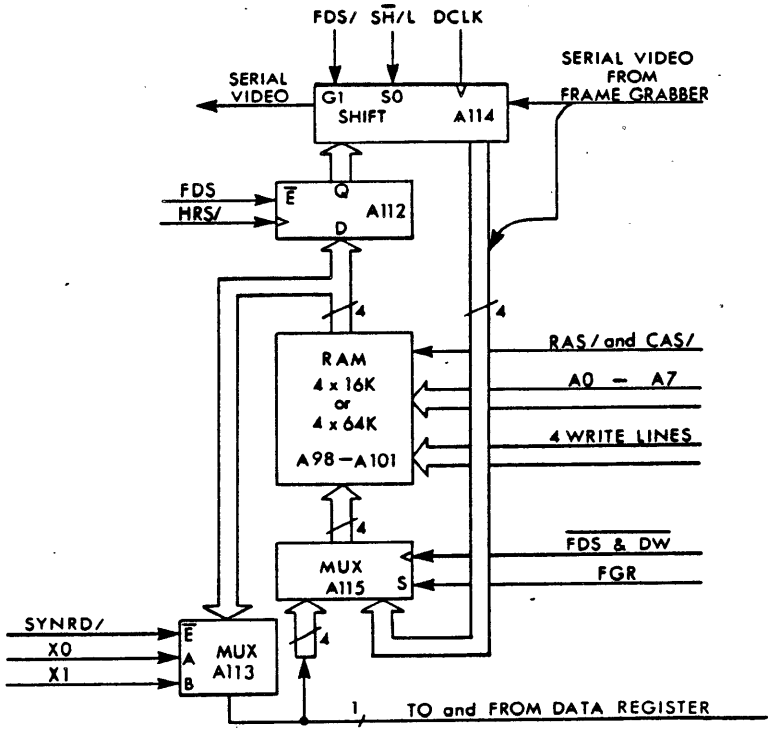


Figure 6.2 - BIT PLANE NO. 0.

6.2 CENTRAL TIMING:

Figure 6.3 is a block diagram of the QRGB-Graph's central timing section. It generates most of the board's timing signals and is controlled principally by CTL11-CTL13 (the X-zoom factor), which set the divisor used by the Dot Clock (A36), the Load Clock (A23), and the Cell Clock (A58). A divisor of one is used for zoom by one, a divisor of two is used for zoom by two, and so on. A58 enables the Load Clock every 4 SCLK Cycles and enables the Cell Clock (CCLK) every 8 SCLK cycles. Figures 6.4 and 6.5 show the timing of A36, A23, and A10 for zoom times one and zoom times two.

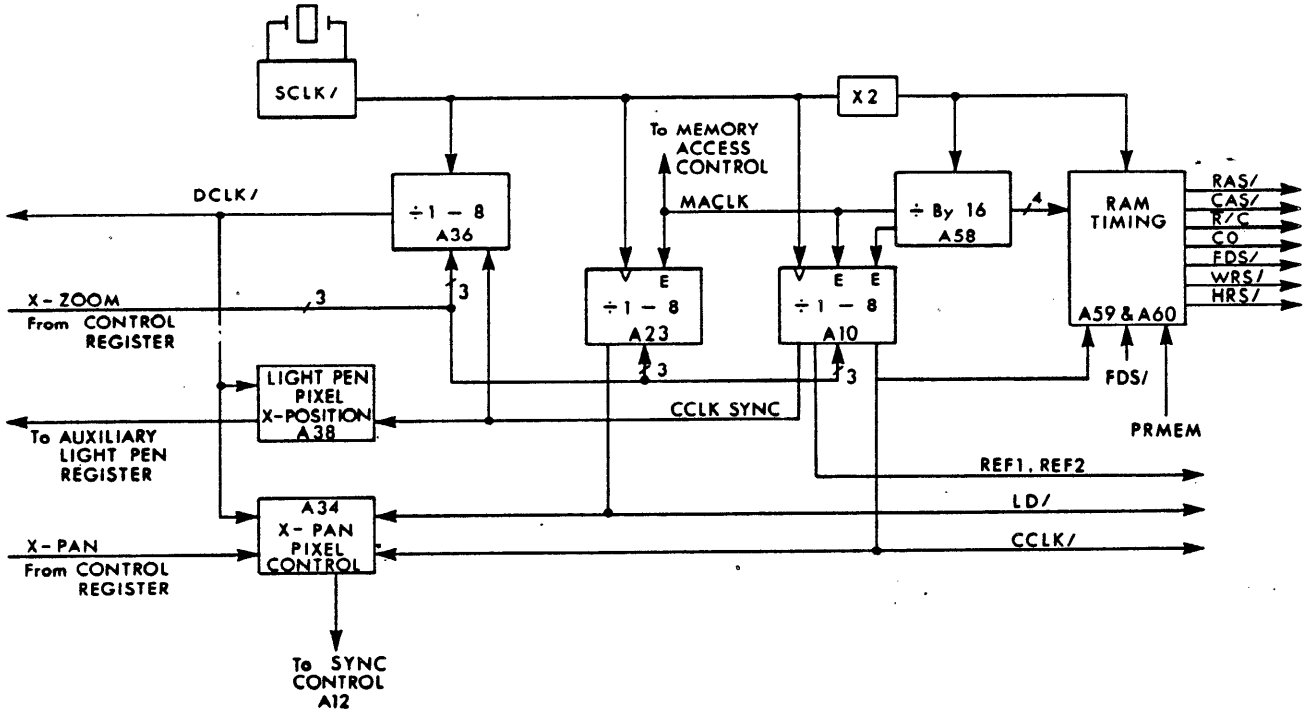


Figure 6.3 - TIMING SECTION BLOCK DIAGRAM.

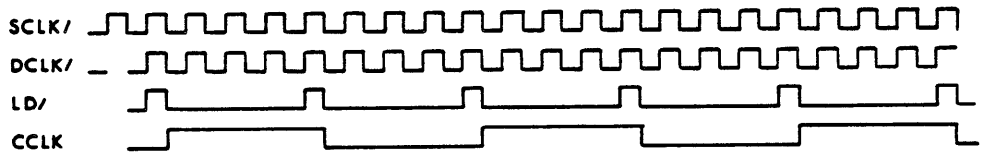


Figure 6.4 - X-ZOOM BY ONE TIMING.

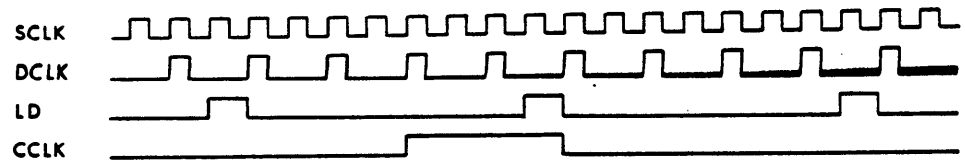


Figure 6.5 - X-ZOOM BY TWO TIMING.

6.2 CENTRAL TIMING (Cont'd):

The three least significant outputs of A58 are used to address a PROM (A59) which generates a series of timing signals for the memory. The relation of these signals to several other timing signals is shown in figure 6.6. Note that the form of the signals depends on the state of CCLK and PRMEM which are also connected to the PROM's address lines. Also note that the display is refreshed when CCLK is high and that there are two memory reads during that period (CAS goes low twice): four bits are read out of each bit plane when C0 is low and another four bits are read out when C0 is high. The period during CCLK low is reserved for accesses from off-board. PRMEM goes high for both frame grab and preset memory operations and the only difference in timing between these operations is that FDS/ is gated on by FGR/ during frame grab.

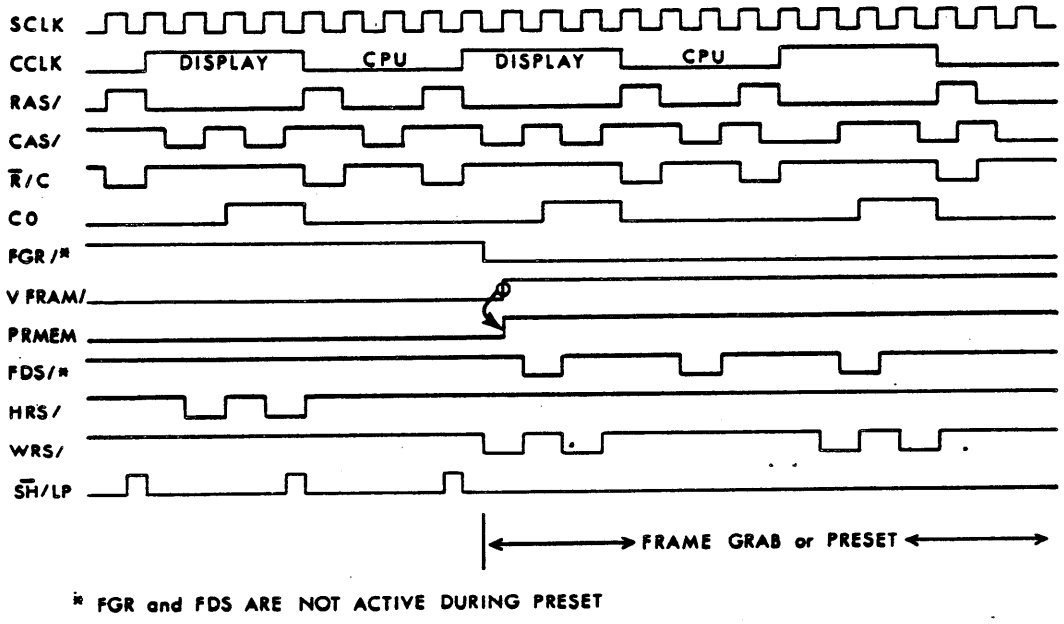


Figure 6.6 - MEMORY TIMING (X-ZOOM BY ONE).

The central timing section also controls the light pen and the X-pan functions at the pixel resolution level. A38 holds the position of the scan as it moves through each cell and provides this information to the Auxiliary Light Pen Register. A34 sets the position of the horizontal sync pulse in response to the CTL8-CTL10 (X-PAN) from Control Register No. 1.

6.3 FRAME GRAB AND PRESET CONTROL:

Figure 6.7 shows a simplified version of the circuit used to control frame grab and memory preset operations. The circuit synchronizes these operations with the VFRAM signal which indicates the start of each new frame. The two flip flops, A57-5 and A9-5, are part of Control Register No.5 and hold bits 6 and 7 respectively. Note that PRMEM, which goes to the memory timing PROM (A59), goes high when either a frame grab or a memory preset operation is initiated. Also note that the Q output of A9-5 is read as bit 7 of the Status Register.

3 FRAME GRAB AND PRESET CONTROL (Cont'd):

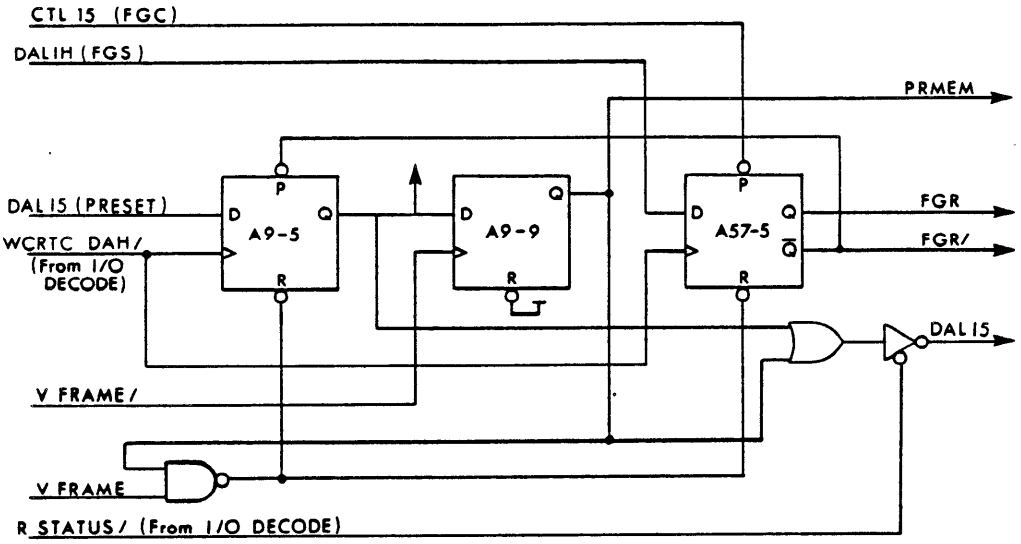


Figure 6.7 - FRAME GRAB AND PRESET CONTROL.

6.4 MEMORY ACCESS CONTROL:

The QRGB-Graph's display memory can be addressed by either the CRTC or the X and Y Registers. The CRTC does so to refresh the display or to do frame grab or preset operations; the X and Y Registers do so when there is an external access from the system CPU or a DMA controller. Since refresh is an on-going process it takes precedence, and the four multiplexers, A65, A78, A93, A108 (see schematic), normally connect the memory address lines to the CRTC. When an external access occurs the address multiplexers are switched to the X and Y Registers by BCLE from the circuit shown in figure 6.8. This circuit arbitrates conflicts between external and internal accesses of the display memory.

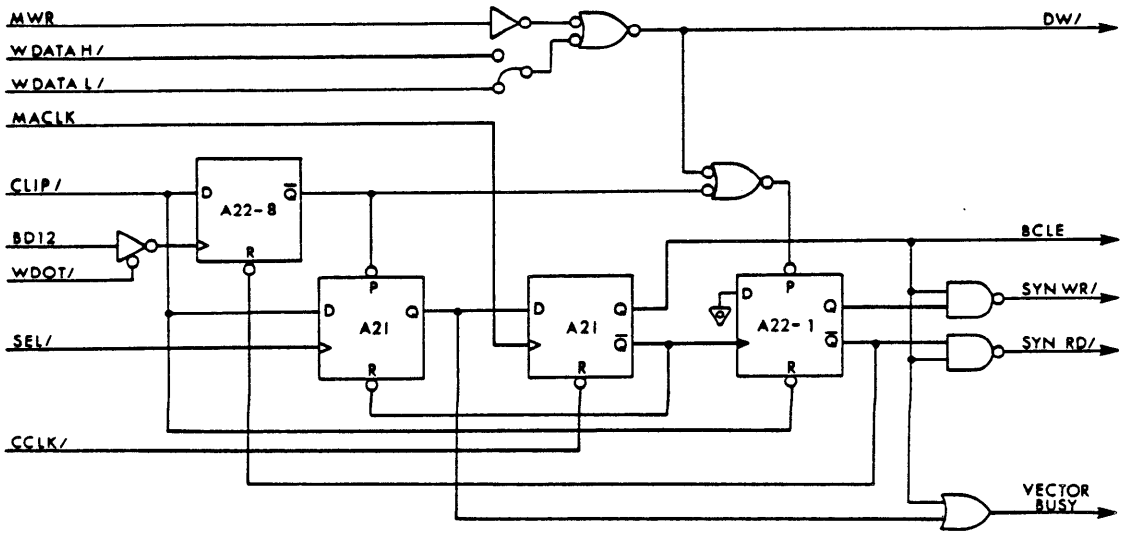
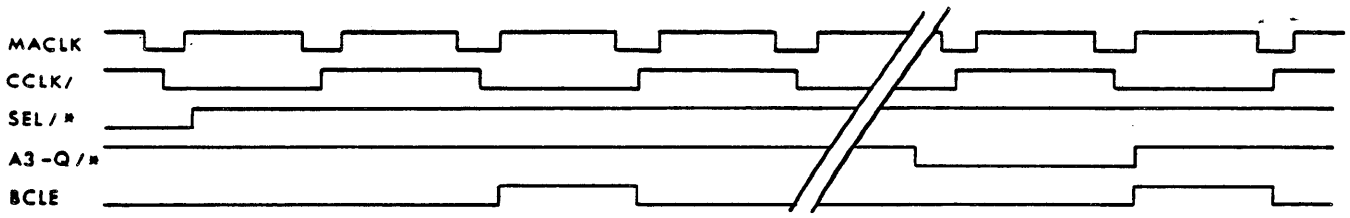


Figure 6.8 - MEMORY ACCESS ARBITRATION LOGIC

6.4 MEMORY ACCESS CONTROL (Cont'd):

The CRTC accesses the display memory only when the CCLK is high, at which time the accessed data is latched into A114 and A112 which mask the display from the display memory. Because of this, the CCLK 'low' period is available for external access. The circuit in figure 6.8 delays any external access until the start of the CCLK low period at which time BCLE is generated and the access is made. Figure 6.9 shows the timing involved in this procedure.



* SEL/ AND A3-Q/ ARE INITIATED BY AN EXTERNAL ACCESS AND THEIR POSITIONS IN THIS DIAGRAM ARE ARBITRARY WITH RESPECT TO THE OTHER TIMING SIGNALS.

Figure 6.9 - BCLE TIMING (ZOOM BY ONE).

Note that BCLE will be generated by either the trailing edge of SEL/ initiated by the Q-BUS or a A3-Q/ initiated by the video bus. A3-Q/ signals a write operation resulting from an access to the Vector Register (BD12=WRT).

When the CLIP/ signal is low, it indicates that there is an overflow condition in the X and Y Registers and it will inhibit BCLE, preventing any externally initiated access. Note that CLIP/ does not go low when there is an overflow during a DMA transfer.

5 DISPLAY MEMORY WRITE ACCESS:

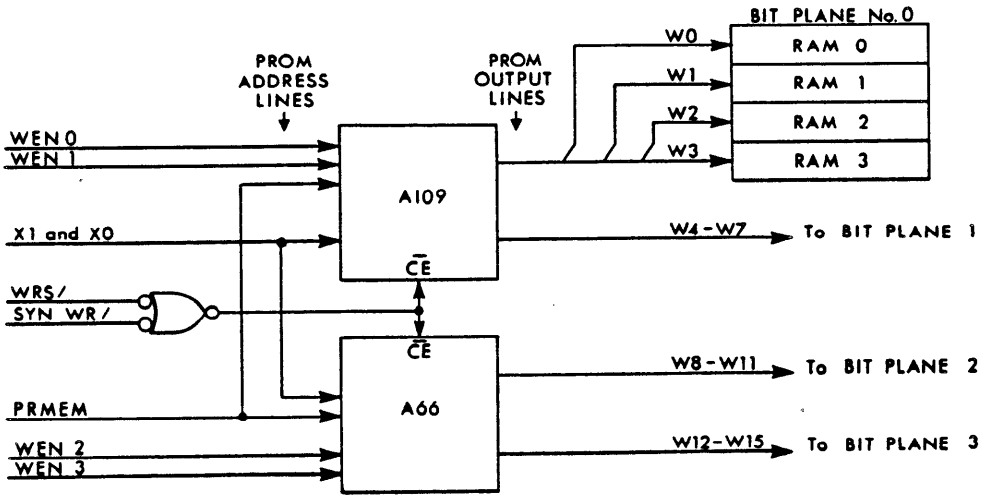


Figure 6.10 - DISPLAY MEMORY WRITE ACCESS LOGIC.

Figure 6.10 shows how the two PROMs, A109 and A66, control the write enable signals for the Display Memory. When there is a frame grab or a memory preset operation the PROMs are enabled by WRS/ from the memory timing PROM (see section 6.2); when there is a write access from off-board, the PROMs are enabled by SYNWR/ from the memory access section (see section 6.4). The PROMs have been programmed to enable the memory write lines (W0-W15) according to the requirements defined by the signals addressing the PROMs. For example if X0 and X1 are low and all the other addresses lines are high, W0 will be pulled low, allowing a write to RAM 0 of bit plane 0. If a WEN line is low access to the corresponding bit plane in interdicted.

6.6 REFRESH ADDRESSING:

Figure 6.11 shows how the Display Memory refresh address is taken from the CRTC. Note that the RAM row address (R0-R7) is contained within the least significant part of the CRTC generated address to assure that the RAMs are refreshed within the required time limit. The Y-zoom multiplexer selects different bits of the scan line counter (RA0-RA4) as RAM row address, R4-R6, depending on the Y-zoom factor. This is done to allow for the fact that the number of scan lines per pixel changes with the Y-zoom factor. The two Exclusive OR gates, A73-6 AND A73-8, are used to assure that all of the RAM columns get refreshed when the larger X-zoom factors are used. In such a case, REF2 and REF3 are automatically pulled high following each display refresh cycle, RAS/ and CAS/ are generated (see figure 6.6), and the unused rows are refreshed without their contents being displayed. In some cases 64K RAMs requiring 256 refresh addresses are used in the QRGB-Graph. When this occurs, the positions of R7 and C2 are interchanged within the CRTC generated address to assure proper RAM refresh.

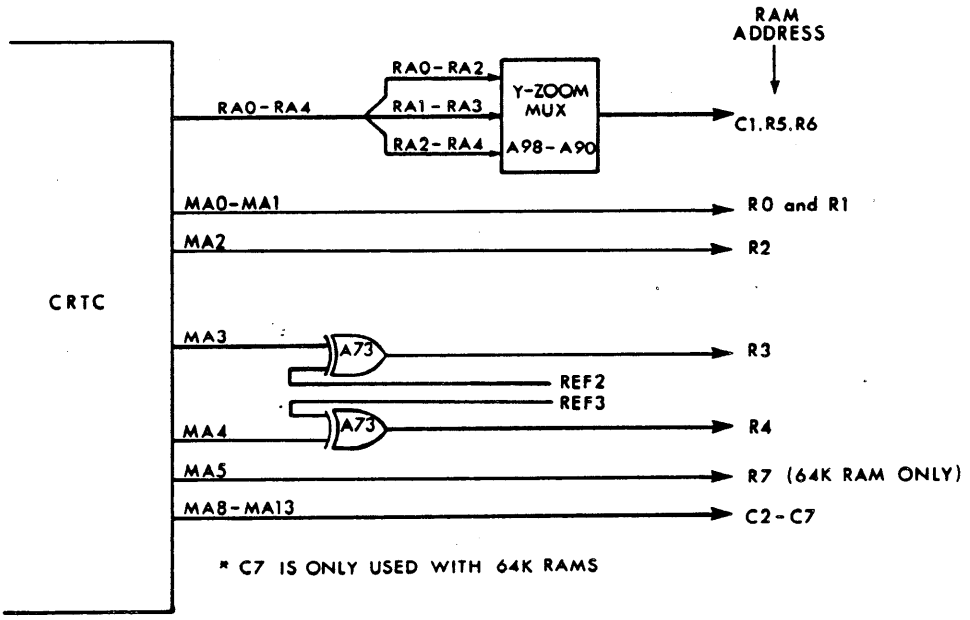


Figure 6.11 - RAM REFRESH ADDRESS.

6.7 VIDEO OUTPUT:

Figure 6.12 shows a block diagram of the video output section. The double resolution function is implemented in A39 by multiplexing the four bit planes onto two video output lines.

SD0-SD3, VDOMAP0-VDOMAP3, and ALTMAP provide the address lines for the 512 X 8 look-up table PROM. Depending on that address the PROM generates different values which produce different intensity levels in the video DACs.

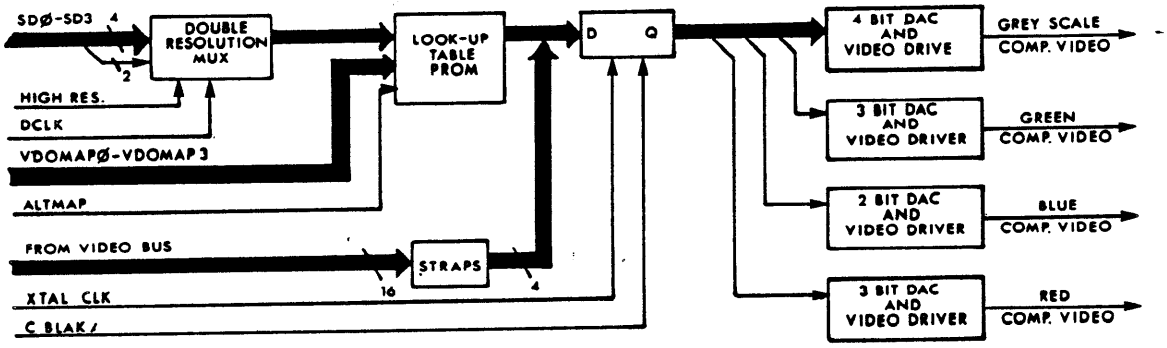


Figure 6.12 - VIDEO OUTPUT SECTION.

* * * * *

7.0 CONNECTORS:

7.1 P1 (BUS CONNECTOR):

P1 consists of 4-36 pin edge connectors as used with the Q-BUS. Table 7.1 shows the pin assignments.

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
AA1	N.C.	AA2	+5V
AB1	N.C.	AB2	N.C.
AC1	BDAL 16L	AC2	GROUND
AD1	BDAL 17L	AD2	+12V
AE1	N.C.	AE2	BDOUTL
AF1	N.C.	AF2	BRPLYL
AH1	N.C.	AH2	BDINL
AJ1	GROUND, SYSTEM SIGNAL GROUND	AJ2	BSYNCL
AK1	N.C.	AK2	BWTBTL
AL1	N.C.	AL2	BIRQ4L
AM1	GROUND	AM2	BIAKIL
AN1	N.C.	AN2	BIAKOL
AP1	N.C.	AP2	BBS7L
AR1	N.C.	AR2	BDMG1L
AS1	N.C.	AS2	BDMGOL
AT1	GROUND, SYSTEM SIGNAL GROUND	AT2	BINITL
AU1	N.C.	AU2	BDALØL
AV1	N.C.	AV2	BDAL1L

TABLE 7.1 - P1-A PIN ASSIGNMENT.

P1 (BUS CONNECTOR):(cont'd)

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
BA1	N.C.	BA2	+5V
BB1	N.C.	BB2	N.C.
BC1	N.C.	BC2	GROUND
BD1	N.C.	BD2	N.C.
BE1	N.C.	BE2	BDAL2L
BF1	N.C.	BF2	BDAL3L
BH1	N.C.	BH2	BDAL4L
BJ1	GROUND	BJ2	BDAL5L
BK1	N.C.	BK2	BDAL6L
BL1	N.C.	BL2	BDAL7L
BM1	GROUND	BM2	BDAL8L
BN1	N.C.	BN2	BDAL9L
BP1	N.C.	BP2	BDAL10L
BR1	N.C.	BR2	BDAL11L
BS1	N.C.	BS2	BDAL12L
BT1	GROUND	BT2	BDAL13L
BU1	N.C.	BU2	BDAL14L
BV1	+5V	BV2	BDAL15L

TABLE 7.1 - P1-B PIN ASSIGNMENT.

7.1 P1 (BUS CONNECTOR):(cont'd)

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
CA1		CA2	-
			N.C.
		CL2	-
		CM2	BIAK1L
		CN2	BIAK0L
		CP2	N.C.
		CR2	BDMG1L
		CS2	BDMG0L
		CT2	N.C.
		CU2	BDAL0L
CV1		CV2	BDAL1L

TABLE 7.1 - P1-C PIN ASSIGNMENT.

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
DA1	-	DA2	+5V
		DB2	N.C.
		DC2	GROUND
		DD2	N.C.
		DE2	BDAL2L
		DF2	BDAL3L
		DH2	BDAL4L
		DJ2	BDAL5L
		DK2	BDAL6L
	N.C.	DL2	BDAL7L
		DM2	BDAL8L
		DN2	BDAL9L
		DP2	BDAL10L
		DR2	BDAL11L
		DS2	BDAL12L
		DT2	BDAL13L
		DV2	BDAL14L
DV1	-	DV2	BDAL15L

TABLE 7.1 - P1-D PIN ASSIGNMENT.

7.2 J1 (COMPOSITE VIDEO):

NOTE: The following figure is the pin configuration for J1, J2, and J3. (Front View).

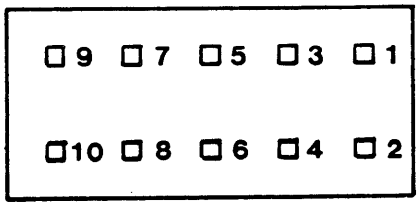


FIGURE 7.1 - 10-PIN HEADER ASSIGNMENT

J1 is a 10 pin right angle header (0.100 IN.) that mates with the AMP # 87922-1 or equivalent. It is used for the composite video outputs. Note that coaxial cable can be attached to this connecter.

PIN	SIGNAL	PIN	SIGNAL
1	GREY SCALE	6	GROUND
2	GROUND	7	BLUE VIDEO
3	RED VIDEO	8	GROUND
4	GROUND	9	N.C.
5	GREEN VIDEO	10	GROUND

Table 7.2 - J1 PIN ASSIGNMENT.

7.3 J2 (DIRECT DRIVE OUTPUTS):

J2 is a 10 pin right angle header (0.100 IN.) that mates with the AMP. 87922-1 or equivalent. It provides the signals required by direct drive monitors. For best signal quality we recommend that the Direct Drive and Composite Video outputs are not used simultaneously unless special precautions are taken by the user to avoid ringing on the external line from J2.

PIN	SIGNAL	PIN	SIGNAL
1	H. DRIVE/	6	GROUND
2	GROUND	7	TTL BLUE
3	TTL RED	8	GROUND
4	GROUND	9	V. DRIVE/
5	TTL GREEN	10	GROUND

Table 7.3 - J2 PIN ASSIGNMENT.

7.4 J3 (LIGHT PEN):

J3 is a 10 pin right angle header (0.100 IN.) that mates with the Molex 15-25-5103 # 4700 or equivalent. It is used for light pen signals.

PIN	SIGNAL	PIN	SIGNAL
1	L.P. ENABLE	6	N.C.
2	N.C.	7	GROUND
3	L.P. STROBE	8	GROUND
4	N.C.	9	N.C.
5	+5V	10	L.P. LO

Table 7.4 - J3 PIN ASSIGNMENT.

NOTE: Pin 9 is not connected but pin 10 must be connected to ground through the light pen's plug (P4) when the light pen is to be used.

7.5 J4 (VIDEO BUS):

J4 is a 50 pin right angle header (0.100 IN.) that mates with the Molex 10-55-3505 or equivalent. It is the connector for the MATROX Video Bus.

PIN	SIGNAL	PIN	SIGNAL
1	GROUND	26	VIDEO DATA E
2	EXTERNAL CLOCK	27	VIDEO DATA F
3	GROUND	28	GROUND
4	EXTERNAL CCLK SYNC/	29	FRAME GRAB 0
5	GROUND	30	FRAME GRAB 1
6	V RESET/	31	FRAME GRAB 2
7	GROUND	32	FRAME GRAB 3
8	HORIZONTAL SYNC/	33	FRAME GRAB 4
9	VERTICAL SYNC/	34	FRAME GRAB 5
10	COMPOSITE BLANKING	35	FRAME GRAB 6
11	GROUND	36	FRAME GRAB 7
12	VIDEO DATA 0	37	GROUND
13	VIDEO DATA 1	38	TTL RED QRGB-Alpha
14	VIDEO DATA 2	39	TTL GREEN QRGB-Alpha
15	VIDEO DATA 3	40	TTL BLUE QRGB-Alpha
16	VIDEO DATA 4	41	RESERVED
17	VIDEO DATA 5	42	GROUND
18	VIDEO DATA 6	43	INC X
19	VIDEO DATA 7	44	DEC X
20	VIDEO DATA 8	45	INC Y
21	VIDEO DATA 9	46	DEC Y
22	VIDEO DATA A	47	WRITE DOT
23	VIDEO DATA B	48	GROUND
24	VIDEO DATA C	49	VECTOR BUSY /
25	VIDEO DATA D	50	CRTC RESET/

Table 7.5 - J4 PIN ASSIGNMENT.

* * * * *

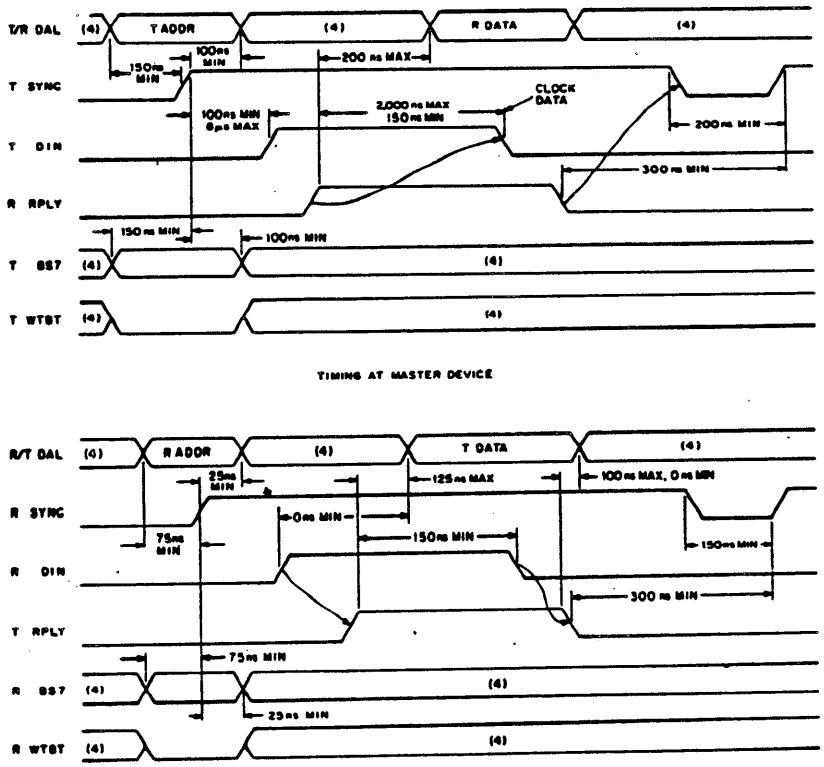
8.0 READ/WRITE TIMING:

The QRGB-Graph conforms to the standard LSI-11 timing set out in figures 9.1 and 9.2. The time from BDINL or BDOUTL to BREPLY varies depending on the type of access, the XTAL frequency, and the position of the access request with respect to the internal refresh cycle. It is always 1500ns for access to registers. Table 9.1 shows the worst and best case access times for the Display Memory when the as-shipped crystal is used. The average access time increases as formats become less dense.

FORMAT	X-Y ZOOM	CYCLE TIME (10.000MHz XTAL)		
		BEST TIME	AVERAGE	WORST TIME
256 x 256	X1	800ns	1460ns	2.4us
	X2	800ns	1230ns	2.4us
	X4	800ns	1020ns	2.4us
512 x 256 512 x 512	X1	400ns	730ns	1.2us
	X2	400ns	615ns	1.2us
	X4	400ns	510ns	1.2us

Table 9.1 - ACCESS TIMES

8.0 READ/WRITE TIMING (cont'd):



TIMING AT MASTER DEVICE

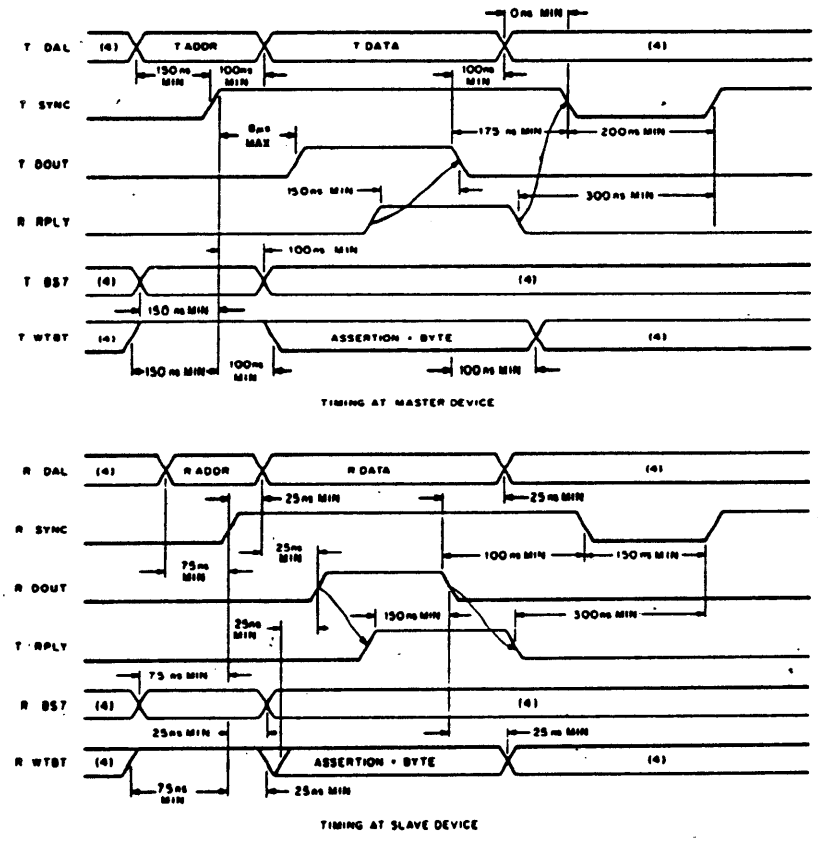
TIMING AT SLAVE DEVICE

NOTES:

1. Timing shown at Master and Slave Device Bus Driver inputs and Bus Receiver Outputs
2. Signal name prefixes are defined below
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix
4. Don't care condition

Figure 9.1 - LSI-11 DAT/ BUS CYCLE TIMING

8.0 READ/WRITE TIMING (Cont'd):



NOTES

1 Timing shown at Master and Slave Device Bus Driver inputs and Bus Receiver Outputs

2 Signal name prefixes are defined below

T = Bus Driver Input
R = Bus Receiver Output

3 Bus Driver Output and Bus Receiver Input signal names include a "B" prefix

4 Don't care condition

Figure 9.2 - LSI-11 DATO or DATOB BUS CYCLE TIMING

* * * * *

9.0 APPLICATIONS:

9.1 COMBINED QRGB-Graph AND QRGB-ALPHA:

The QRGB-Graph and the QRGB-ALPHA can be synchronized and their video outputs can be mixed to provide a combination alphanumerics and graphics display. This is accomplished by simply interconnecting the two boards as illustrated in figure 10.1 and programming their CRTC's to conform to the constraints imposed by formulas 1 through 8.

9.1.1 PROGRAMMING FORMULAS FOR COMBINED QRGB-Graph AND QRGB-ALPHA.*

1. H. TOTAL x H. DOTS/CELL [GRAPH] = H. TOTAL x H. DOTS/CELL [ALPHA]*
2. H. SYNC POSITION [GRAPH] = (H. TOTAL - 1) - (3 CHAR) [GRAPH]
3. V. SYNC WIDTH + V. SYNC POSITION [GRAPH] = (V. TOTAL - 1) + V. ADJUST [GRAPH]
4. V. SYNC WIDTH [GRAPH] = AN ODD NUMBER
5. H. SYNC WIDTH [GRAPH] = 1
6. V. TOTAL [GRAPH] = V. TOTAL [ALPHA]*
7. V. ADJUST [GRAPH] = V. ADJUST [ALPHA]*
8. V. SYNC POSITION [GRAPH] = V. TOTAL [GRAPH]

* Or slaved QRGB-Graph. The [GRAPH] referred to above is a single board or master. Be sure to read Section 5 before slaving two boards.

Note that when these two boards are combined the QRGB-ALPHA can not have character cells 11 dots wide and its cursor blink function will not work in non-interlaced displays.

9.1.2 MASTER-SLAVE SETUP:

This section outlines the steps to be followed when slaving two or more boards, and concludes with two examples of how this is done in practice. Remember that the CRTC values given are for the average monitor, and may have to be adjusted to accomdate monitors that have different characteristics:

1) Try programming and operating each of the boards in a stand-alone mode, using the initialization procedures in Section 3 of each manual. When you have become comfortable with each board on its own, then and only then should the multi-board system be constructed.

2) See Sections 4 & 5 and the following figures 10.1 and 10.2 for Register parameters and strap changes that must be done in order for the multi-board system to work properly.

3) Set up the QRGB Registers on the boards according to your preference.

9.1.2 MASTER-SLAVE SETUP (Cont'd):

EXAMPLE #1-QRGB-GRAPH WITH QRGB-ALPHA

The first example will use one QRGB-GRAPH with four bit planes and an effective display file of 512 x 512 at 60 Hz, and one QRGB-ALPHA.

1) Set up the straps on the boards as shown in the following figure:

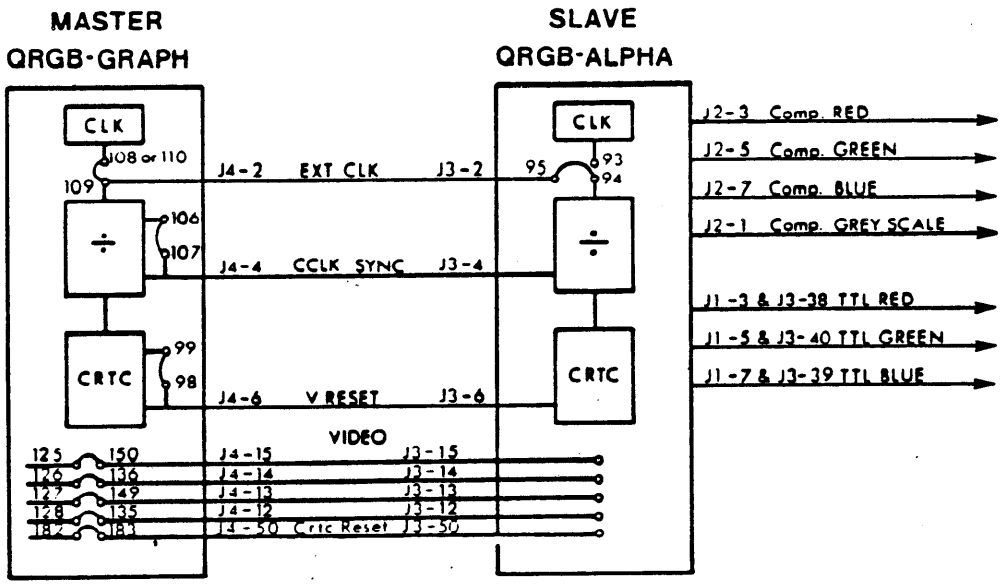


FIGURE 10.1.1 - QRGB-GRAPH with QRGB-ALPHA.

2) Use the following octal parameter list to initialize the boards to a suggested format. After you have become familiar with the operation of the system you will be able to adjust these values to produce special displays, etc:

CRTC REGISTER	GRAPH	ALPHA
R0	117	117
R1	101	100
R2	114	106
R3	061	066
R4	077	031
R5	004	000
R6	074	030
R7	100	030
R8	007	001
R9	007	011
R10	000	100
R11	-	009
R12	000	000
R13	000	000

TABLE 10.1.1 CRTC DATA FOR GRAPH-ALPHA COMBINATION.

9.1.2 MASTER-SLAVE SETUP (Cont'd):

EXAMPLE #2 - QRGB-GRAPH WITH QRGB-GRAPH

This example will use two QRGB-GRAPHS with four bit planes each and a display file of 512 x 512 at 60 Hz.

1) Set up the straps on the boards as shown in the following figure:

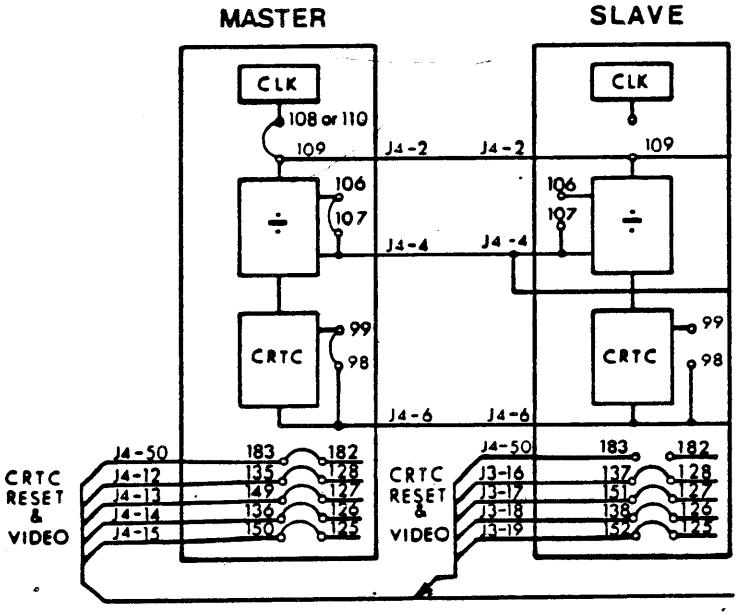


FIGURE 10.1.2 - QRGB-GRAPH WITH QRGB-GRAPH.

2) Use the following parameter list to initialize the boards to a suggested format. After you have become familiar with the operation of the system you will be able to adjust these values to produce special displays, etc:

STEP	DATA(octal) MASTER	DATA(octal) SLAVE	I/O LOCATION	COMMENTS
1	010000	010000	164414	The horizontal total minus one is written to CRTC-R0.
2	000117	000117	164416	
3	010001	010001	164414	The format width, in cells, is written to CRTC-R1.
4	000100	000100	164416	
5	010002	010002	164414	The horizontal sync position is written to CRTC-R2
6	000114	000103	164416	
7	010003	010003	164414	The horizontal and vertical sync widths are written to CRTC-R3.
8	000061	000066	164416	
9	010004	010004	164414	The vertical total minus one is written to CRTC-R4.
10	000077	000077	164416	
11	010005	010005	164414	The vertical adjust parameter is written to CRTC-R5.
12	000004	000004	164416	
13	010006	010006	164414	The format height, in cells, is written to CRTC-R6.
14	000074	000074	164416	
Following the above steps in order, output the data to the I/O location indicated.				

TABLE 10.1.2 - CRTC VALUES FOR GRAPH-GRAPH COMBINATION (more on next page).

.2 MASTER-SLAVE SETUP (Cont'd):

EXAMPLE #2 - QRGB-GRAPH WITH QRGB-GRAPH (cont'd)

STEP	DATA(octal) MASTER	DATA(octal) SLAVE	I/O LOCATION	COMMENTS
15	010007	010007	164414	The vertical sync position is written
16	000100	000075	164416	CRTC-R7.
17	010010	010010	164414	CRTC-R8 is programmed for row and column addressing & to appropriate interlace mode.
18	000007	000007	164416	
19	010011	010011	164414	The No. of scan lines/field per cell row-minus one is written to CRTC-R9.
20	000007	000007	164416	
21	010014	010014	164414	The starting address is set to row zero column zero.
22	000000	000000	164416	
23	010015	010015	164414	
24	000000	000000	164416	
Following the above steps in order, output the data to the I/O location indicated.				

TABLE 10.1.2 - CRTC VALUES FOR GRAPH-GRAPH COMBINATION (cont'd).

9.2 QVAF-512:

Figure 10.2 shows one application where the QRGB-Graph is used with MATROX's new QVAF-512, which will be available sometime in 1983. A preliminary data sheet for the QVAF-512 is also included in this section. The term 'pseudo master' on the diagram below refers to the way the first QRGB-Graph is utilized in the chain. The first QRGB-Graph reads the output VCO pulses from the QVAF and converts them into synchronized clock pulses that are used by the rest of the chain. This allows the QVAF to pass digitized frame grab information to the following boards.

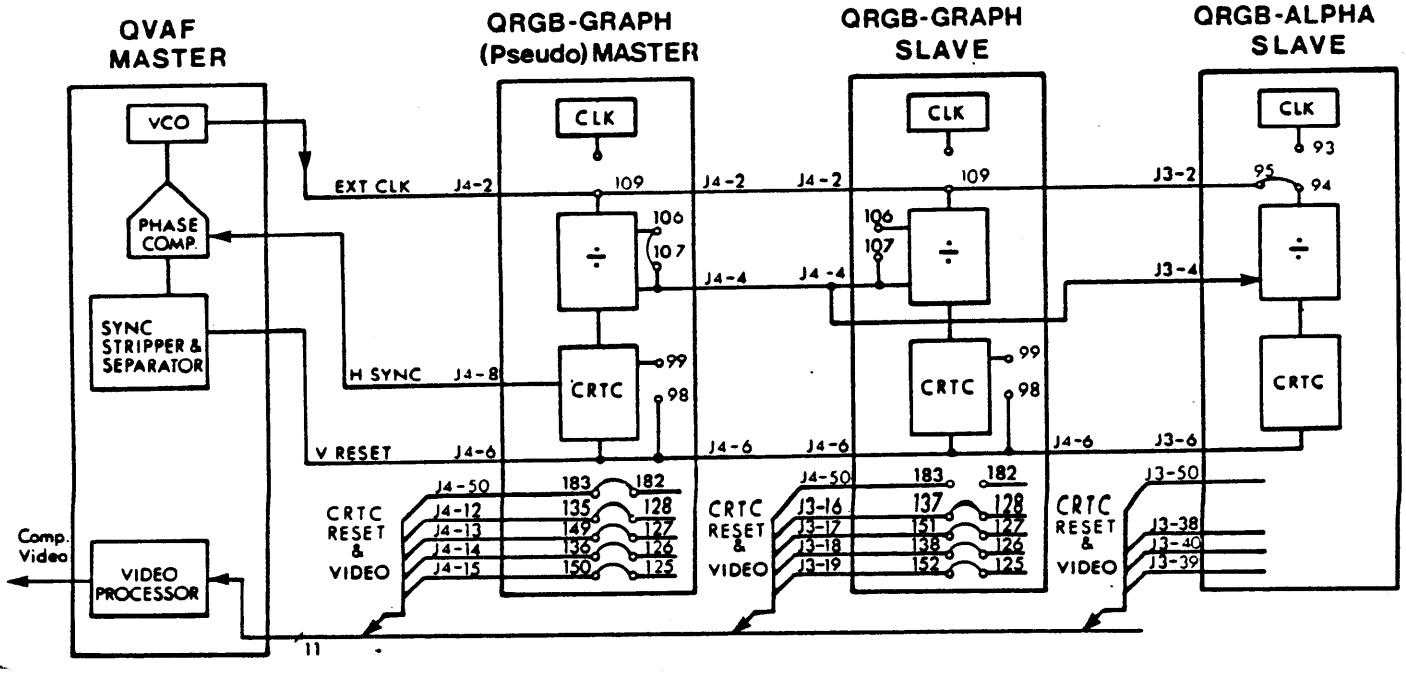


Figure 10.2 - QRGB-Graph, QRGB-ALPHA, QVAF combination.

9.0 APPLICATIONS (Cont'd):

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514-735-1182 TELEX: 05-825651

QVAF-512

1600-2000

QRGB-GRAPH VIDEO INPUT/OUTPUT PROCESSOR FOR LSI-11 Q-BUS

- **Real Time Video Frame Grabber**
  - **4 or 8 bit A/D**
  - **4 input video switch**
  - **Programmable clamping and gain**
  - **Internal/external, block/serrated sync**
  - **Phase locked loop for Genlock**
- **Color Look-Up Table (RAM)**
  - **10 input lines/24 output lines**
  - **Three 8 bit D/A converters (R,G,B)**
  - **16 million color palette**
  - **Blink and overlay control**
- **Hardware Vector Generator**
  - **High speed line drawing (800ns/pixel)**
  - **Length, slope, and texture control**
- **LSI-11 Q-Bus* Compatible**
- **Works With QRGB-GRAPH Board**
- **QRGB-ALPHA Overlay Compatibility**
- **American/European Operation**

The QVAF-512 is a video I/O processor board designed to extend the performance of the Matrox QRGB-GRAPH video controller. The QVAF-512 has three main subsections: a real time video digitizer (frame grabber), a color look-up table, and a high speed vector generator. The video A/D converter provides real time grey scale digitizing, of a camera, videodisk, or VCR signal (4 or 8 bits/pixel), into one or two QRGB-GRAPH frame buffers. The color look-up table provides a palette of over 16 million output shades and colors. The look-up table can accomodate one or two QRGB-GRAPH boards and a QRGB-ALPHA. The on-board vector generator provides high speed line drawings (800ns/pixel). The length, slope, and texture of the displayed lines are all software controlled.

The QVAF-512 plugs into any standard LSI-11 Q-bus backplane and interfaces to the QRGB-GRAPH/QRGB-ALPHA via a single 50-pin ribbon cable. The board will operate in either American or European standard systems.

AVAILABLE

FIRST QUARTER

1983

MATROX products covered by Canadian and foreign patent and/or patent pending.

9.0 APPLICATIONS (Cont'd):

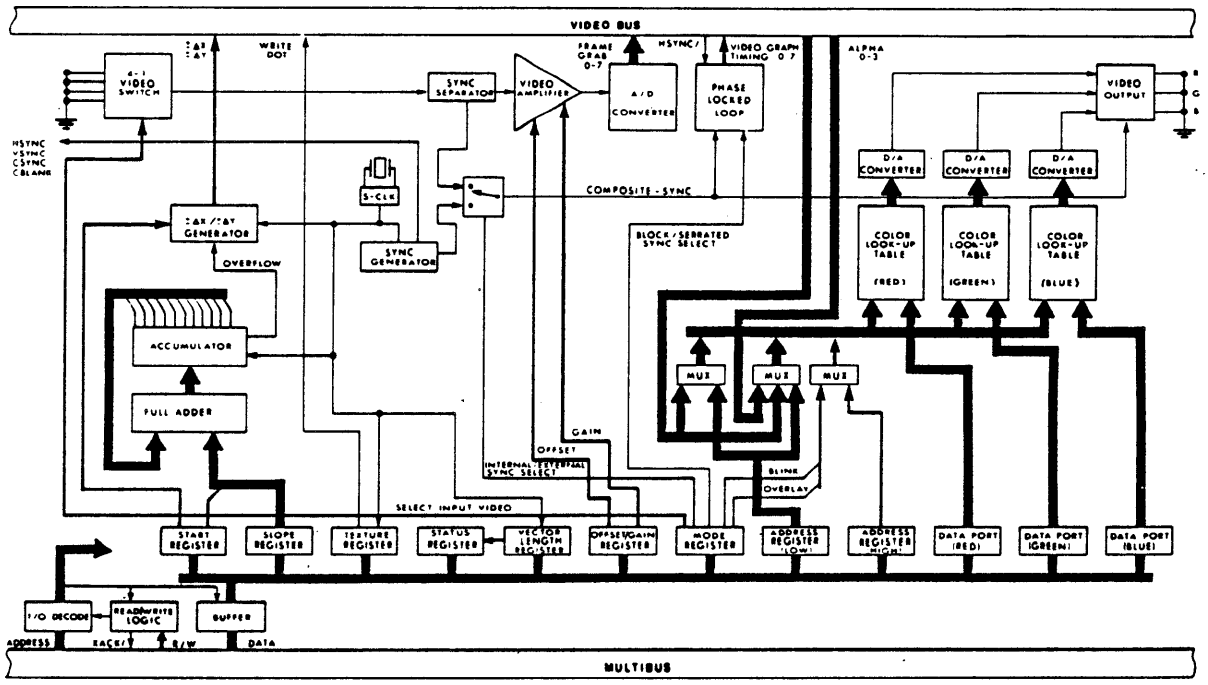


Figure 1. QVAF-512 block diagram

QVAF-512 FEATURES

FRAME GRABBER

High Speed A/D Converter: The QVAF-512 contains an on-board 10 MHz A/D converter for real-time frame grabbing applications. Images can be digitized to either 4 or 8 bits/pixel.

4 Input Video Switch: Up to four different analog video inputs can be accepted by the QVAF-512. Each video source can be individually selected for frame grabbing under software control.

Color Frame Grabbing: By connecting the R,G,B outputs from a color video camera to separate inputs on the video switcher, and then grabbing each channel separately, a color picture can be digitized.

Software Controlled: Gain and Offset: The QVAF-512 Frame Grabber enables the user to introduce a software programmable gain and/or offset to the input video signal. This feature enables the user to concentrate the digitizing operation on that part of the input signal which contains most of the video information — effectively increasing the contrast.

Programmable Sync: Under software control the QVAF-512 can be programmed to lock to either block or serrated sync. Sync signals can be generated on-board, or stripped from the input video signal for broadcast and video mixing applications.

VECTOR GENERATOR

High Speed Line Drawings: Vectors can be drawn to the graphics display, via the QVAF-512 hardware Vector Generator, at speeds that are 20 to 40 times faster than conventional software vector generation techniques.

Vector Texture Control: The texture of the displayed vectors (dotted, dashed, solid, etc.) can be programmed by the user through an on-board 16 bit Texture Register. Up to 65,000 different texture patterns can be defined.

COLOR LOOK-UP TABLE

Programmable Colors: The QVAF-512 Color Look-Up Table allows the user to select the available display colors from over 16 million possible shades. Up to 16 colors can be displayed with systems using one QRGB-GRAPH board, and 256 colors can be displayed using two QRGB-GRAPH boards.

Overlay: Alphanumeric characters (from the QRGB-ALPHA) can be overlayed on the graphics display through the Color Look-Up Table. When characters are to be overlayed on the display, the 4 bits from the QRGB-ALPHA board will replace the four most significant graphics bits on the look-up table address lines.

Blink: The graphics display can be set to blink between any of the available display colors. The QVAF-512 can also be programmed to blink only the overlayed alphanumeric characters. The blink frequency can be software selected for 1.8 Hz or 3.75 Hz.

Q-Bus Interface: The QVAF-512 looks to the user like 7 consecutive I/O locations. All communications between the host CPU and the QVAF-512 (including read/write operations to the Color Look-Up Table) are accomplished via I/O read/write.

ACCESS TIME: Time from CMD/to BRPLY/ for all registers is less than 50ns.

VIDEO-BUS: A 50 pin connector provides all the video input and output lines required to interface the QVAF-512 with up to two QRGB-GRAPH boards and one QRGB-ALPHA board.

9.0 APPLICATIONS (Cont'd):

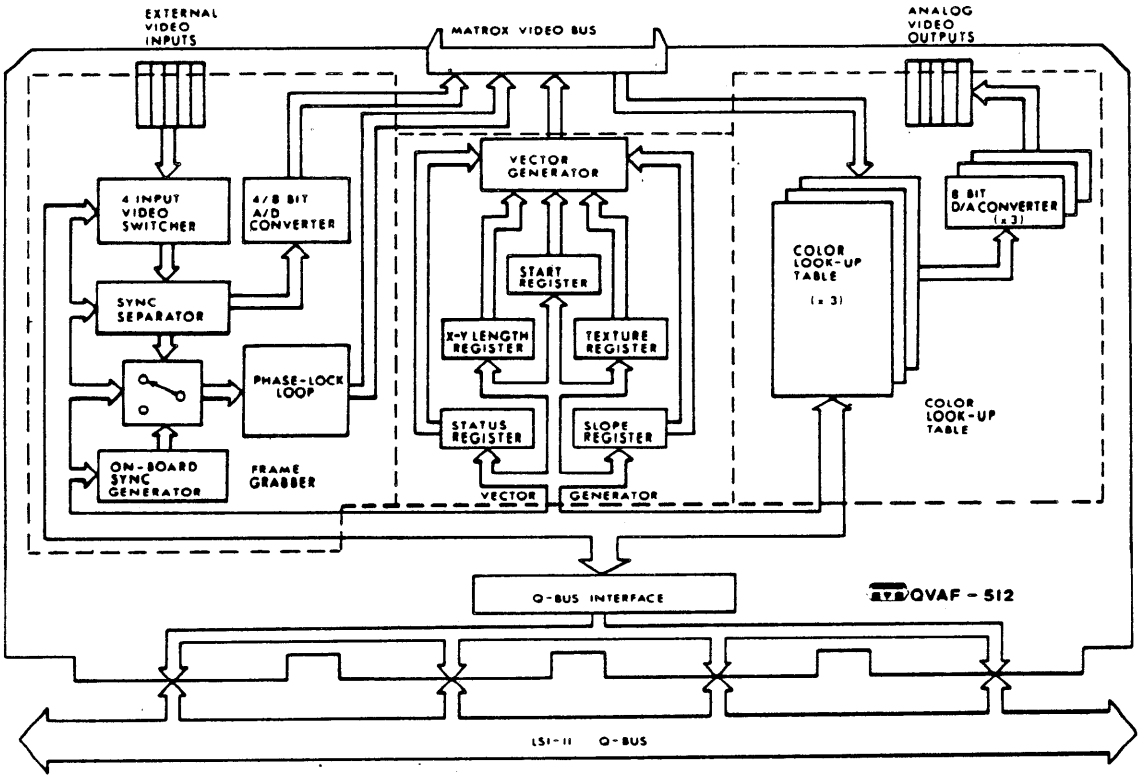


Figure 2. QVAF-512 functional blocks

FUNCTIONAL DESCRIPTION

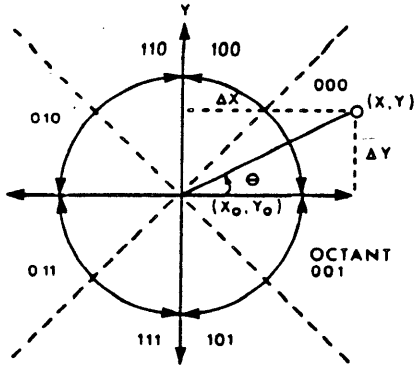
The QVAF-512 has been designed to complement the operation of Matrox's QRGB-GRAPH/QRGB-ALPHA family of color video controllers. The QVAF-512 comprises three independent operational sections (figure 2) contained on a single Q-bus compatible PC board.

The on-board **Hardware Vector Generator** provides an efficient means of drawing vectors to the QRGB-GRAPH display memory. Three parameters are required to specify a line draw operation; length, slope, and texture. The 10 bit Length Register stores the length of the larger of the two components (ΔX, ΔY). This permits vectors of up to 1024 pixels to be drawn with a single software Write command. A 10 bit Slope Register stores, with single pixel precision, the $\tan\theta$ where θ is an angle between 0° and 45°. Three bits in the Start Register define the proper octant. The Vector Generator circuit calculates the X and Y addressing, as required by the QRGB-GRAPH, on a pixel by pixel basis until the full vector has been drawn. A Busy Flag in the Status Register or a hardware interrupt can be used to indicate completion.

The texture of the displayed vector is stored in a 16 bit Texture Register. The contents of the Texture Register defines a 16 bit repeating pattern of pixel information (figure 4). In this way solid, dotted, dashed, and hidden vectors can be drawn. Note that the Data Register on the QRGB-GRAPH board is used to set the color of the vector.

The hardware Vector Generator operates with a drawing speed of 800ns/pixel. This represents an increase of about 20 to 40 times the conventional drawing speeds acheived by software vector generation.

The QVAF-512 **Frame Grabber** enables the user to digitize a frame of video information (from an external video camera, VCR or video disk), with either 4 or 8 bits per pixel, and store that frame in the QRGB-GRAPH display memory (512 x 512 x 4 bits per GRAPH board). Using commands issued by the QRGB-GRAPH, this frame grabbing operation can be continuous (QRGB-GRAPH will display a continually updated or "live" picture) or one shot, effectively "freezing"



IF $|\Delta X| \geq |\Delta Y|$
THEN LENGTH = $|\Delta X|$
AND SLOPE = $\left|\frac{\Delta X}{\Delta Y}\right|$

IF $|\Delta X| < |\Delta Y|$
THEN LENGTH = $|\Delta Y|$
AND SLOPE = $\left|\frac{\Delta Y}{\Delta X}\right|$

Figure 3. Determining vector length and slope parameters

4.0 APPLICATIONS (Cont'd):

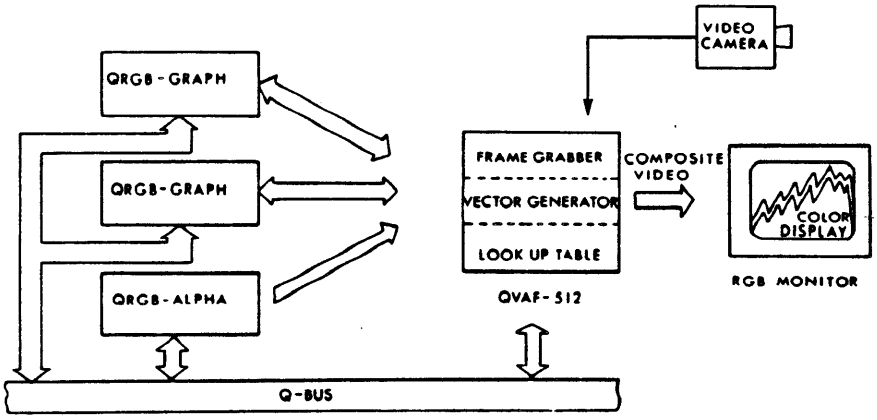


Figure 5. QVAF-512 in system

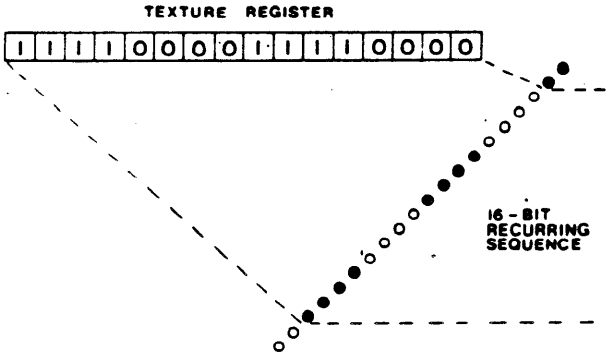


Figure 4. Defining the "Texture" pattern for the displayed vectors

the action. Up to four video cameras can be interfaced to the QVAF-512 through an on-board four input video switcher which permits software selection between the four video sources.

Incorporated into the design of the frame grabber is a Phase-Lock Loop circuit (PLL). The PLL uses the sync signal stripped from the input video signal as a reference frequency to which it synchronizes the rest of the system (QRGB-GRAPH/QRGB-ALPHA). If required, an on-board sync generator (strappable for American EIA or European CCIR standard sync) can be software-selected to act as a master sync source for both the video display boards and the video source. The PLL can also be programmed to accept either block or serrated sync.

The QVAF-512's frame grabber provides software control over the gain of the input signal. This feature, together with a software-variable voltage offset (clamping level) on the input, allows the user to take advantage of the full digitizing range of the A/D converter for a given input signal amplitude. This technique can be used to concentrate the operation of the A/D converter on that part of the input signal that contains the most video information, in effect increasing the contrast of the image. There are sixteen different levels of gain and sixteen different levels of offset.

The QVAF-512 **Color Look-Up Table** is made up of three 1K x 8 RAM look-up tables (one for each primary color: red, green,and blue), each of which are divided into four 256 byte sections: Normal, Overlay, Blink, and Blink And Overlay. These Color Look-Up Table provide the QRGB-GRAPH with a color palette of over 16 million colors. To display a

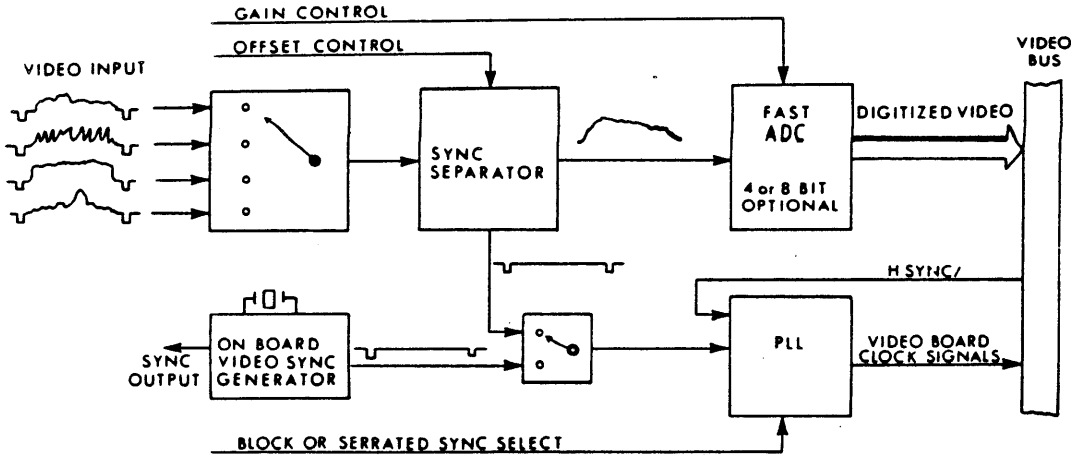


Figure 6. Frame Grabber

9.0 APPLICATIONS (Cont'd):

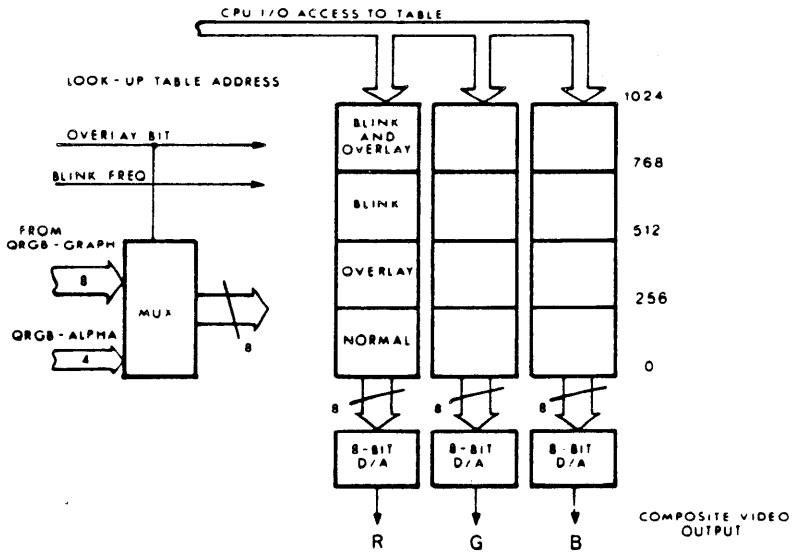


Figure 7. Color Look-Up Table

desired color at a certain pixel location, the user simply loads that color's look-up table address into the QRGB-GRAPH display memory location corresponding to the pixel position. The contents of the look-up table can be changed at any time. A single QRGB-GRAPH board (4 bits) can address 16 different locations in the look-up table. Two QRGB-GRAPH boards (8 bits) can address up to 256 locations in the look-up table. Additionally, the Color Look-Up Table is sectored into four 256 byte blocks (figure 5) in order to allow separate color mappings for overlayed alphanumerics and for blinking. The blink rate is software selectable to be either 1.8 Hz or 3.75 Hz.

When an QRGB-ALPHA is interfaced to the QVAF-512 the four bits from the alpha board replace 4 of the 8 graphic bits in addressing the Color Look-Up Table. When at least one of these bits is high (alphanumeric data is to be displayed) access to the look-up table is shifted to the Overlay section which contains its own color map. As a result, alphanumeric text from the QRGB-ALPHA can be superimposed (overlayed) on the graphics background. The user can also program the QVAF-512 to blink the alphanumeric characters between the colors defined in the Overlay and Overlay And Blink sections of the look-up table (similar to blinking graphics pixels between the Normal and Blinking sections). This method of generating blinking characters is very flexible as it allows characters to blink to colors other than their background color.

MATROX VIDEO BUS

The QVAF-512 is interfaced to the QRGB-GRAPH and QRGB-ALPHA boards by way of a 50-pin Matrox Video Bus. Digitized video data as well as ΔX and ΔY increment/decrement strobes are bussed from the QVAF-512 to the QRGB-GRAPH. The Video Bus also carries the 4 TTL video bits from each of the QRGB-GRAPHs and the QRGB-ALPHA boards for color look-up on the QVAF-512.

BUS INTERFACE

The QVAF-512 plugs directly into the LSI-11 Q-Bus. The seven Command and Status Registers are positioned on any 8 word I/O address boundary between 760 000$_8$ and 777 777$_8$

PROGRAMMING

The QVAF-512 is programmed via seven on-board I/O registers. On power-up or reset all control registers must be loaded with the QVAF-512's operational parameters (table 1).

REGISTER	ADDRESS	DEFINITION
TEXTURE REGISTER	BASE + 0	16 bit vector texture pattern
VECTOR LENGTH REGISTER	BASE + 2	10 bit vector length
GAIN/OFFSET/MODE REGISTER	BASE + 4	Select gain/Select offset/Select input video to frame grabber/Enable on-board sync generator/Select block sync/Enable overlay/Enable blink frequency/Enable blink
VECTOR REGISTER	BASE + 6	10 bit vector slope/Complement Texture Register/Vector slope < 45/vector quadrant
STATUS REGISTER	BASE + 10	QVAF-512 status
ADDRESS REGISTER	BASE + 12	10 bit look-up table address/Select look-up table
DATA PORT	BASE + 14	Read/write data to the selected look-up table

Table 1. Register Definitions

9.0 APPLICATIONS (Cont'd):

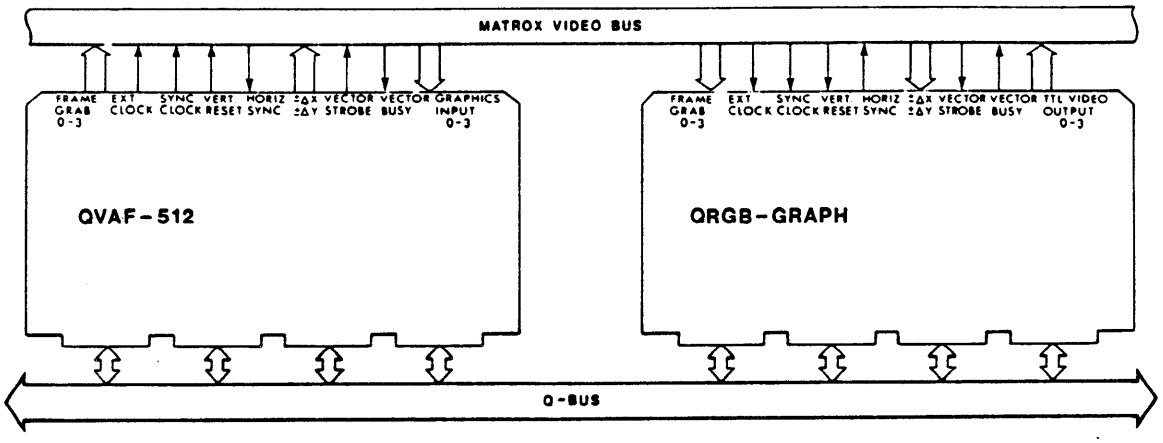


Figure 8. 512 x 512 x 4 video imaging system

DISPLAY SYSTEM CONFIGURATIONS

The Matrox family of advanced color video boards, which include the QVAF-512, QRGB-GRAPH, and QRGB-ALPHA, offer the OEM system designer a unique capability to design a powerful optimal graphics system with the equal or even superior performance of a turn-key graphics system — at a lower cost. Furthermore, by using general purpose OEM boards, the user can add CPUs, memory disk interfaces, etc. to configure his system to his exact requirements. Software support, in the form of a graphics primitive library, further simplifies design of the custom video systems. Hardware upward capability enables adding extra display functions by simply plugging in additional boards (more bits/pixel, higher speed, alphanumeric overlay, etc).

4 BIT/PIXEL IMAGING SYSTEM

Combining the QVAF-512 with a single QRGB-GRAPH (figure 8) yields a video imaging system using 4 bits/pixel. Whole frames of video picture information with up to 16 color or grey levels can be digitized and stored in the display memory of the QRGB-GRAPH.

8 BIT/PIXEL Imaging system

Adding another QRGB-GRAPH graphics controller to the system (figure 9) doubles the number of bit planes to eight. This enables the system to store and display images with a resolution of 512 x 512 dots using up to 256 colors or grey levels.

An alphanumerics overlay can also be added to the graphics display by plugging in a QRGB-ALPHA alphanumerics controller to the system.

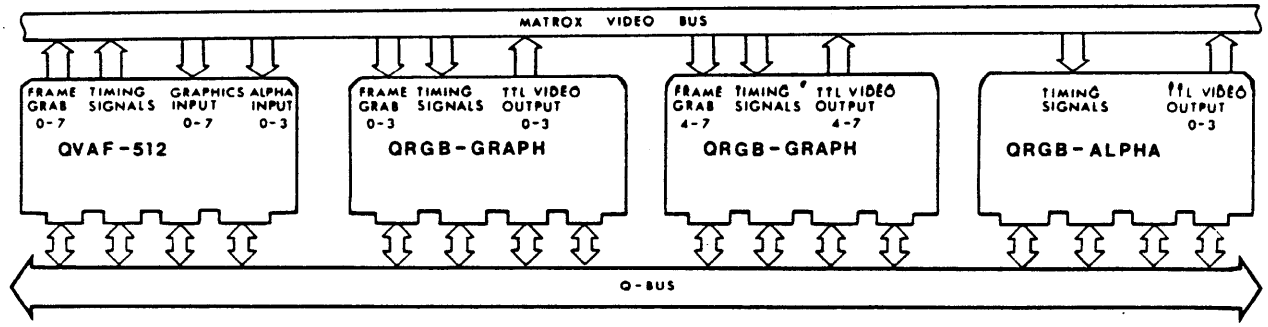


Figure 9. 512 x 512 x 8 video imaging system with alphanumerics overlay

9.0 APPLICATIONS (Cont'd):

SPECIFICATIONS

FUNCTIONAL

OPERATIONAL PARAMETERS

VECTOR GENERATOR

DESCRIPTION	RESTRICTIONS
Drawing Speed	800ns/pixel (512 x 512 resolution)
Vector Texture	65,000 texture patterns (software selectable)

FRAME GRABBER

DESCRIPTION	RESTRICTIONS
Spatial Resolution	512 x 512 max.
Video Inputs	4 analog video inputs (software switchable)
Sync	Internal/external, block/serrated (software selectable)
Bits/pixel	4 or 8 bits
Offset	16 increments from Black level to nominal mid-range (software selectable)
Gain	16 increments from 0.7 to 1.9 of nominal (software selectable)

COLOR LOOK-UP TABLE

DESCRIPTION	RESTRICTIONS
Palette Size	2^{24} = 16,777,216 colors
Addressable Colors	16 colors (1 x QRGB-GRAPH)/256 colors (2 x QRGB-GRAPH)
Blink Rate	1.8 Hz/3.75 Hz (software selectable)

INPUT SIGNALS

ANALOG INPUTS: Camera 0, Camera 1, Camera 2, Camera 3

TTL LEVEL INPUTS: 4/8 graphics bits, 4 overlay bits, HSYNC/, BUSY/

OUTPUT SIGNALS

ANALOG OUTPUTS: Composite Video (RED), Composite Video (BLUE), Composite Video (GREEN)

TTL LEVEL OUTPUTS: 8 Video Bits, System Clock, $\pm\Delta X$, $\pm\Delta Y$, V. Reset, Composite Sync, Horizontal Sync, Vertical Sync, Composite Blanking

BUS INTERFACE

Address, data, and control signals conform to DEC LSI-11 Q-bus specifications.
Command and Status Registers — Selectable on any 8 word I/O address boundaries 760 000$_8$ - 777 777$_8$

CONNECTORS

DESCRIPTION		MATING CONNECTOR
A: 36 pin edge connector, 0.125" centers B: 36 pin edge connector, 0.125" centers C: 36 pin edge connector, 0.125" centers D: 36 pin edge connector, 0.125" centers	LSI-11 Bus interface	DEC H8030 (2 required)
J1: 10 pin right angle header	— Composite Video Output	AMP 87922-1
J2: 10 pin right angle header	— Analog Video Input — Sync Output to Camera	AMP 87922-1
J3: 50 pin right angle header	— Matrox Video Bus	MOLEX 15-25-4505

PHYSICAL

SIZE

WIDTH: 10.45 in. (26.54 cm)
HEIGHT: 8.43 in. (21.41 cm)
DEPTH: 0.50 in. (1.27 cm)

POWER REQUIREMENTS

+5V DC ± 5% @ 3.2A
+12V DC ± 5% @ 120mA
−12V DC ± 5% @ 0.95A (QVAF-512/8)*
−12V DC ± 5% @ 0.55A (QVAF-512/4)*

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: O°C to 55°C
Relative Humidity: 0% to 90% non-condensing

ORDERING INFORMATION

QVAF-512/X-XX

- AS — American standard (60Hz)
- ES — European standard (50Hz)
- Number of bits per pixel (4/8)

Example: QVAF-512/8-AS: American standard board with a 8 bit/pixel A/D converter (frame grabber).

*The −12V power supply is not installed on all DEC systems.

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LSI-11 Q-bus and DEC are all registered trademarks of Digital Equipment Corp

10.0 MAINTENANCE AND WARRANTY:

MATROX products are warranted against defects in materials and workmanship for a period of 180 days from date of delivery. We will repair or replace products which prove to be defective during the warranty period, provided they are returned to MATROX ELECTRONIC SYSTEMS, Ltd. No other warranty is expressed or implied. We are not liable for consequential damages.

Our U.S. customers are requested to return their products to our U.S. branch at the following address: MATROX INTERNATIONAL CORPORATION; Trimex Building, Mooers, N.Y. 12958.

11.0 ORDERING INFORMATION:

The QRGB-Graph can be ordered directly from MATROX ELECTRONIC SYSTEMS, Ltd. or from our worldwide network of distributors.

* * * * *

APPENDIX A DATA SHEETS

CRT Controller

SY6545

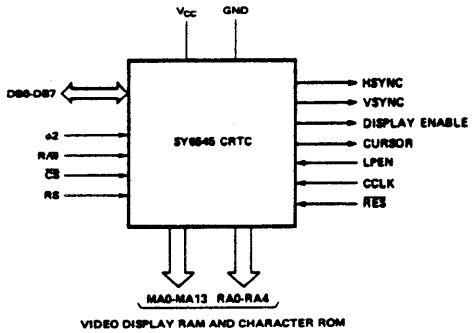
MICROPROCESSOR PRODUCTS

Synertek INCORPORATED

- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required.
- Pin-compatible with MC6845.
- Row/Column or straight-binary addressing for Video Display RAM.
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to 6545.
- Internal status register.

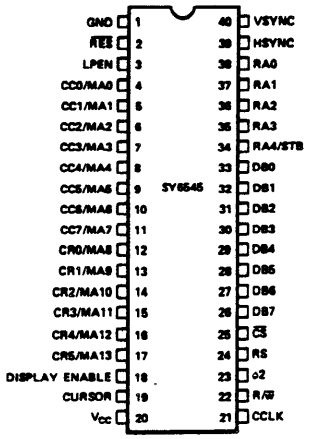
The SY6545 is a CRT Controller intended to provide capability for interfacing the 6500/6800 microprocessor families to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

INTERFACE DIAGRAM



VIDEO DISPLAY RAM AND CHARACTER ROM

PIN DESIGNATION



ORDERING INFORMATION

Part Number	Package	Clock Rate
SYC6545	Ceramic	1 MHz
SYP6545	Plastic	1 MHz
SYC6545A	Ceramic	2 MHz
SYP6545A	Plastic	2 MHz

SY6545

MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.3V to +7.0V
Input/Output Voltage, V_{IN}	-0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

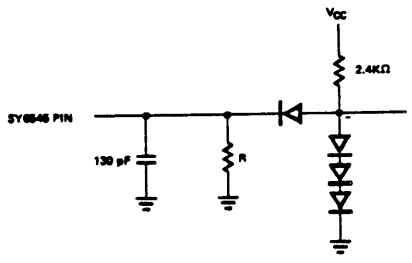
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0-70° C, unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage	2.0	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.8	V
I_{IN}	Input Leakage (ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	–	2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	–	10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = 205μA (DB0-DB7) I_{LOAD} = 100μA (all others)	2.4	–	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	–	0.4	V
P_D	Power Dissipation	–	800	mW
C_{IN}	Input Capacitance ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	– –	10.0 12.5	pF pF
C_{OUT}	Output Capacitance	–	10.0	pF

TEST LOAD

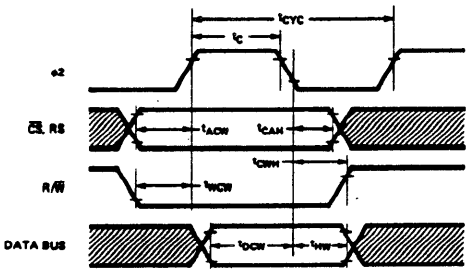


R = 11KΩ FOR DB_0-DB_7
= 24KΩ FOR ALL OTHER OUTPUTS

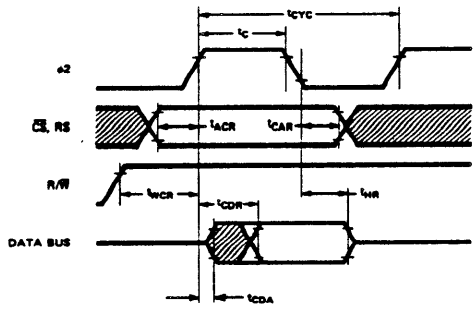
APPENDIX A DATA SHEETS (cont'd)

MPU BUS INTERFACE CHARACTERISTICS

WRITE CYCLE



READ CYCLE



WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0–70°C, unless otherwise noted)

Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{CYC}	Cycle Time	1.0	–	0.5	–	μs
t_C	φ2 Pulse Width	470	–	235	–	ns
t_{ACW}	Address Set-Up Time	180	–	90	–	ns
t_{CAH}	Address Hold Time	0	–	0	–	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
t_{DCW}	Data Bus Set-Up Time	300	–	150	–	ns
t_{HW}	Data Bus Hold Time	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

READ TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0–70°C, unless otherwise noted)

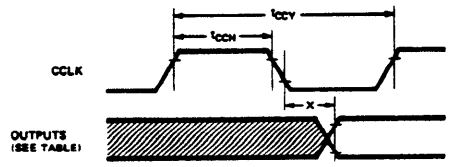
Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{CYC}	Cycle Time	1.0	–	0.5	–	μs
t_C	φ2 Pulse Width	470	–	235	–	ns
t_{ACR}	Address Set-Up Time	180	–	90	–	ns
t_{CAR}	Address Hold Time	0	–	0	–	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
t_{CDR}	Read Access Time (Valid Data)	–	395	–	200	ns
t_{HR}	Read Hold Time	10	–	10	–	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

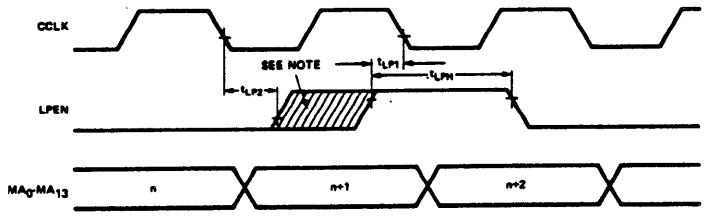
SYSTEM TIMING



Output	Parameter
MA0-MA13	t_{MAD}
RA0-RA4	t_{RAD}
DISPLAY-ENABLE	t_{DTD}
HSYNC	t_{HSD}
VSYNC	t_{VSD}
CURSOR	t_{CDD}

Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{CCY}	Character Clock Cycle Time	0.40	40	0.40	40	µs
t_{CCH}	Character Clock Pulse Width	200	–	200	–	ns
t_{MAD}	MA0-MA13 Propagation Delay	–	160	–	160	ns
t_{RAD}	RA0-RA4 Propagation Delay	–	160	–	160	ns
t_{DTD}	DISPLAY ENABLE Propagation Delay	–	300	–	300	ns
t_{HSD}	HSYNC Propagation Delay	–	300	–	300	ns
t_{VSD}	VSYNC Propagation Delay	–	300	–	300	ns
t_{CDD}	CURSOR Propagation Delay	–	300	–	300	ns

LIGHT PEN STROBE TIMING



NOTE: "Sele" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{LPH}	LPEN Strobe Width	100	–	100	–	ns
t_{LP1}	LPEN to CCLK Delay	120	–	120	–	ns
t_{LP2}	CCLK to LPEN Delay	0	–	0	–	ns

t_r, t_f = 20 ns (max)

SY6545

MPU INTERFACE SIGNAL DESCRIPTION

ϕ2 (Clock)

The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system microprocessor and the SY6545. Since there is no maximum limit to the allowable ϕ2 cycle time, it is not necessary for it to be a continuous clock. This capability permits the SY6545 to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6545; a low on the R/$\overline{W}$ pin allows a write to the SY6545.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The SY6545 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6545. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the SY6545 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0-MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0-MA7 function as column addresses CC0-CC7, and MA8-MA13, as row addresses CR0-CR5. In this case, the software may handle addresses in terms of row and column locations, but additional

address compression circuits are needed to convert CC0-CC7 and CR0-CR5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the SY6545 is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0-MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the SY6545 with only a small amount of external circuitry.

DESCRIPTION OF INTERNAL REGISTERS

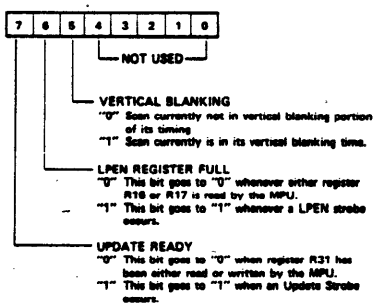
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various SY6545 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct SY6545 data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

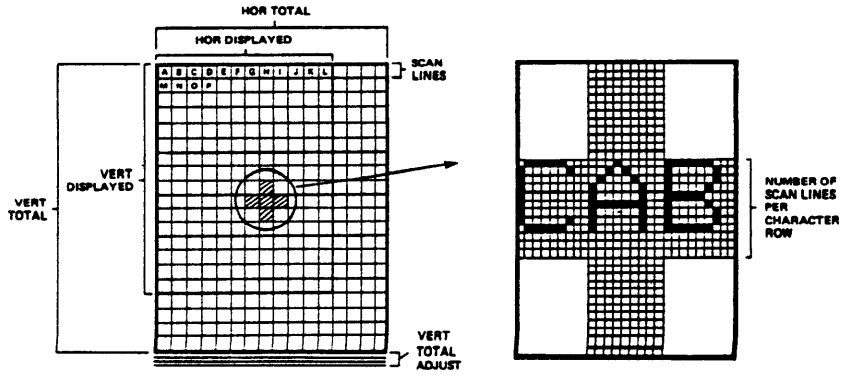


Figure 1. Video Display Format

APPENDIX A DATA SHEETS (cont'd)

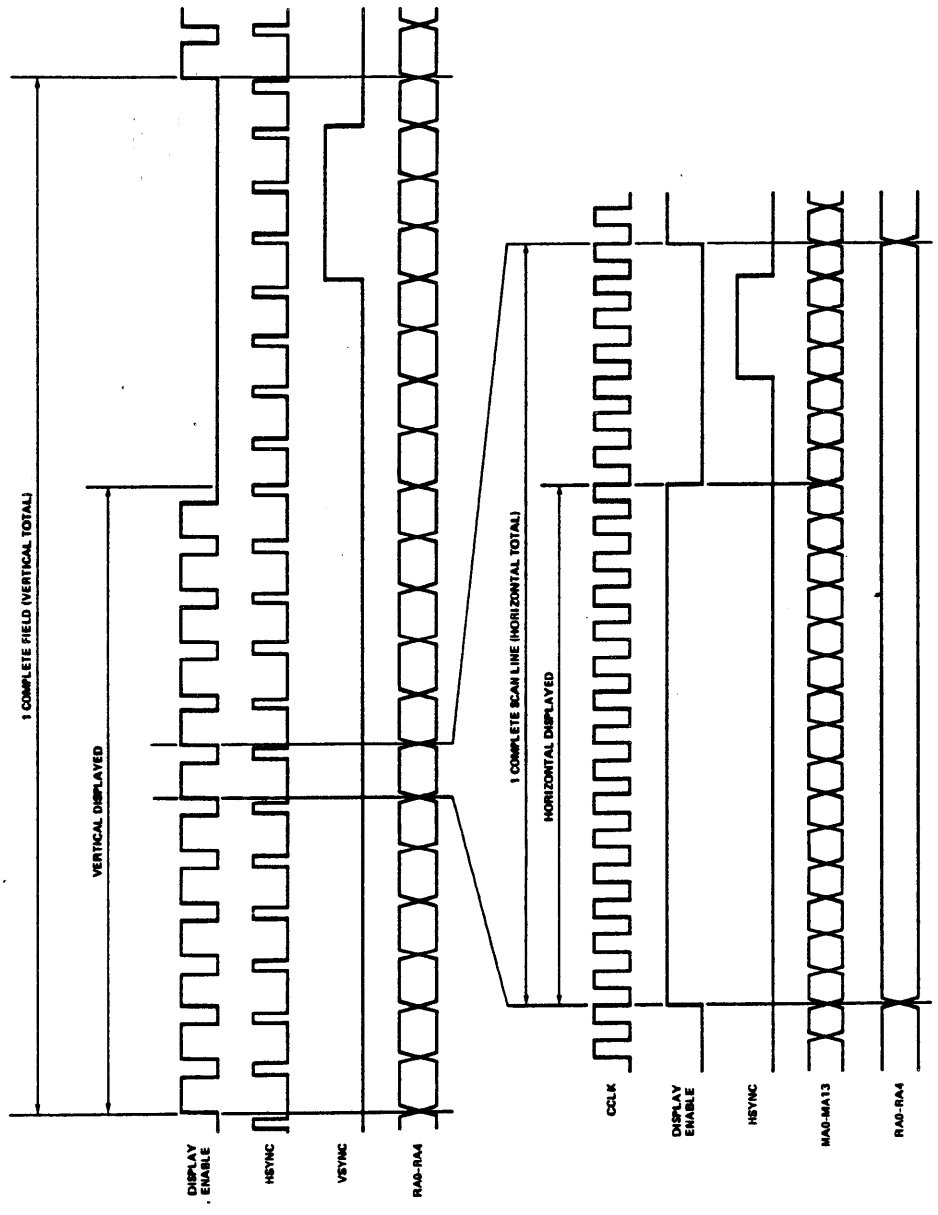
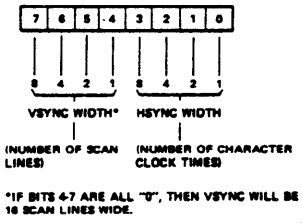


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allows the SY6545 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0		0	–	–	–	–	–	Address Reg.	Reg. No.		√				A_4	A_3	A_2	A_1	A_0
0		0	–	–	–	–	–	Status Reg.		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz. Total	= Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz. Displayed	= Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz. Sync Position	= Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	= Scan Lines and = Char. Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	= Charac. Row		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert. Total Adjust	= Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert. Displayed	= Charac. Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert. Sync Position	= Charac. Rows		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	= Scan Lines		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√			●	●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√			●	●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√				●	●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●
0	1	1	0	0	1	0	R18	Update Location (H)			√			●	●	●	●	●	●
0	1	1	0	0	1	1	R19	Update Location (L)			√	●	●	●	●	●	●	●	●
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: ● Designates binary bit

▨ Designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = "1" which operates likewise.

Figure 3. Internal Register Summary

SY6545

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

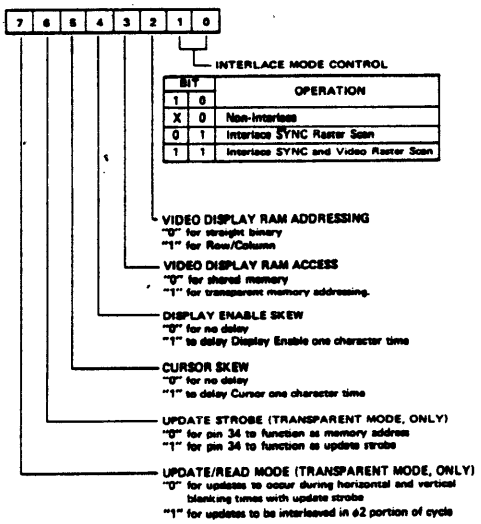
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the SY6545 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT 6	BIT 5	CURSOR MODE
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 1/16 field rate
1	1	Blink at 1/32 field rate

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the SY6545 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

DETAILED DESCRIPTION OF OPERATION

Register Formats

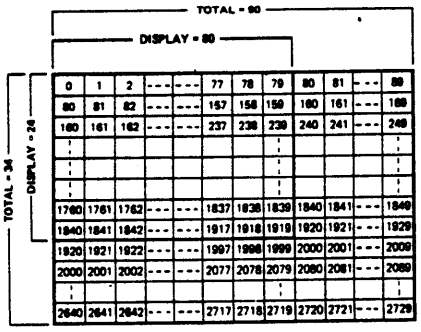
Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

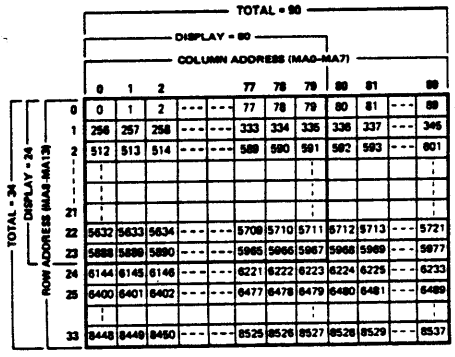
Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.



STRAIGHT BINARY ADDRESSING SEQUENCE



ROW/COLUMN ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory
   In this mode the memory is shared between the MPU address bus and the SY6545 address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the SY6545 must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.
2. Transparent Memory Addressing
   For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the SY6545. All MPU accesses are made via the SY6545 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

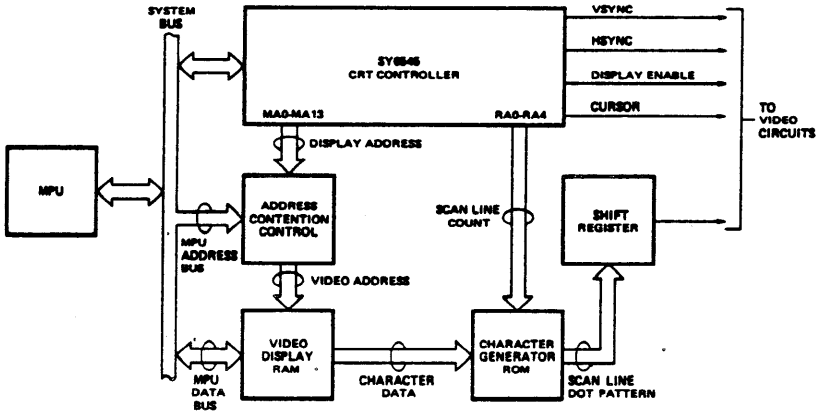


Figure 5. Shared Memory System Configuration

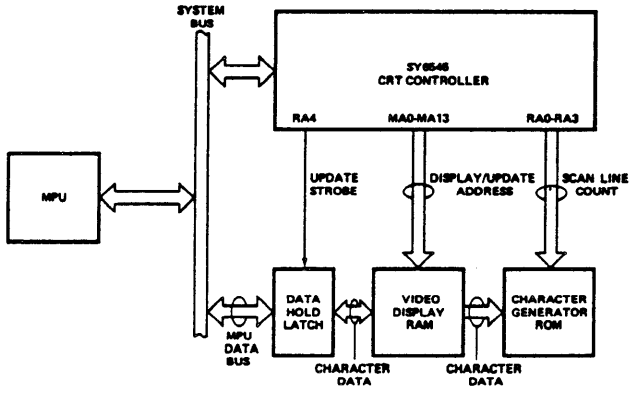


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates, only).

Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 4, it is clear that both the SY6545 and the system MPU must be capable of addressing the video display memory. The SY6545 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the SY6545 unless the MPU needs access, in which case the MPU addresses immediately override those from the SY6545 and the MPU has immediate access.

- $\phi1/\phi2$ Memory Interleaving

  This method permits both the SY6545 and the MPU access to the video display memory by time-sharing via the system $\phi1$ and $\phi2$ clocks. During the $\phi1$ portion of each cycle (the time when $\phi2$ is low), the SY6545 address outputs are gated to the video display memory. In the $\phi2$ time, the MPU address lines are switched in. In this way, both the SY6545 and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

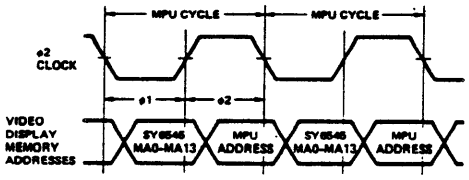


Figure 7. $\phi1/\phi2$ Interleaving

- Vertical Blanking

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the SY6545. In effect, the contention is handled by the SY6545. As a result, the schemes for accomplishing MPU memory access are different:

- $\phi1/\phi2$ Interleaving

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the $\phi2$ address is generated from the Update Address Register (Registers R18 and R19) in the SY6545. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during $\phi2$. Figure 8 shows the timing.

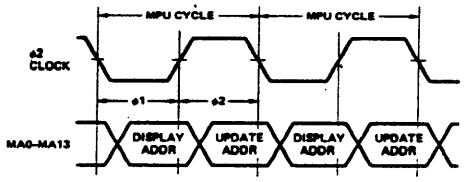


Figure 8. $\phi1/\phi2$ Transparent Interleaving

- Horizontal/Vertical Blanking

  In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

Transparent address modes are quite complex and offer significant advantages in system implementation. The details of their application are covered thoroughly in a related Technical Note available from Synertek.

APPENDIX A DATA SHEETS (cont'd)

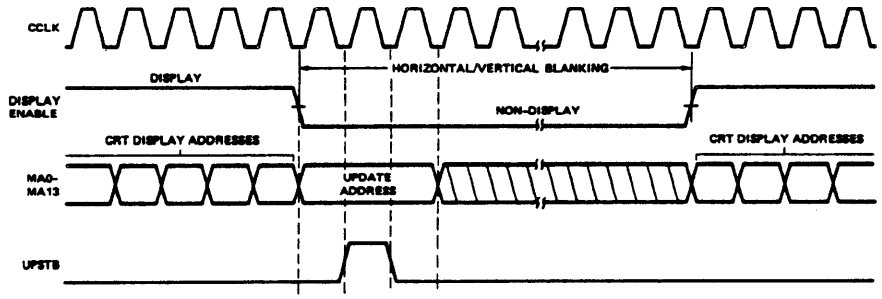


Figure 9. Retrace Update Timings

Interlace Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace-Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 11 and is the only difference in the SY6545 operation in this mode.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered. Figure 12 illustrates the timing.

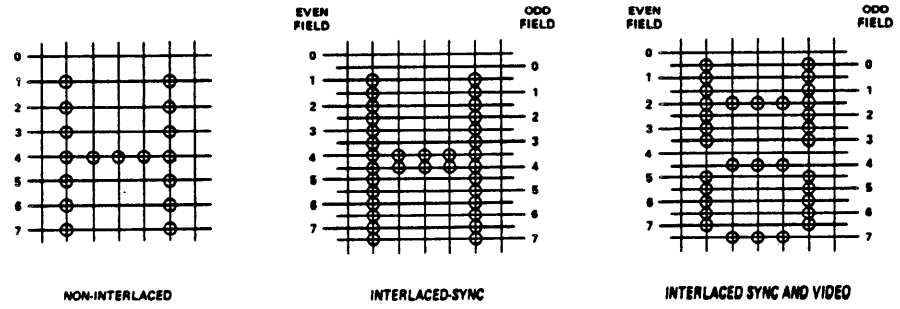


Figure 10. Comparison of Display Modes.

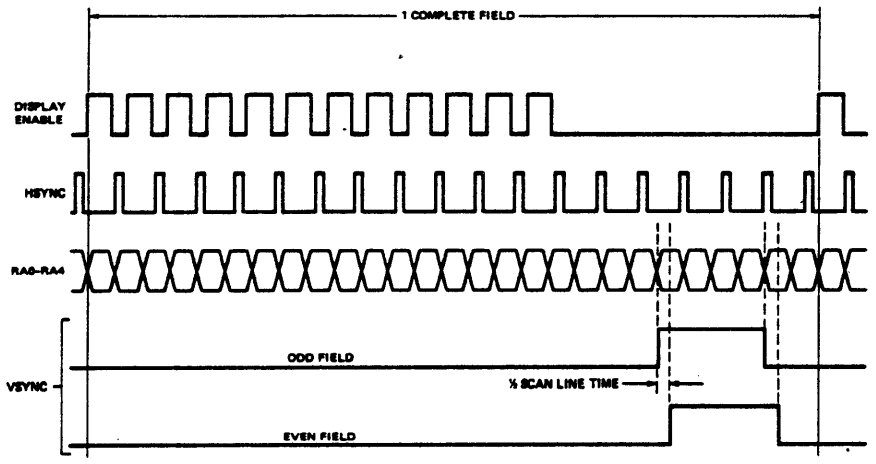


Figure 11. Interlace-Sync Mode Timing

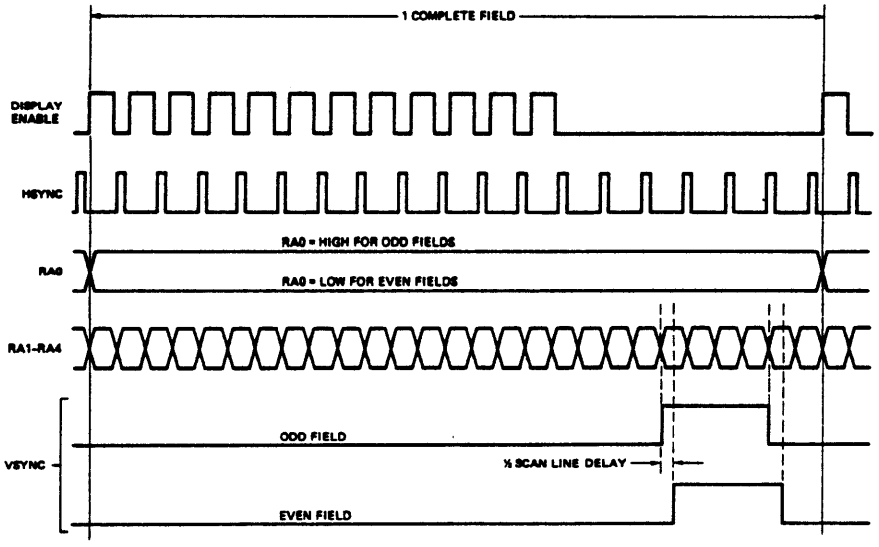


Figure 12. Interlace-Sync-and-Video Mode Timing

Some restrictions on interlace modes of operation are:

a) The Horizontal Total Character count (register R0) must be odd, in order to represent an even number of character times.

b) For Interlaced Sync and Video mode, only, the following registers must be programmed in a non-standard fashion:
   - R4 (Vertical Total) must be programmed to one-half the actual number desired, minus one. For example, for a total of 24 characters high, R4 must contain 11 (decimal).
   - R6 (Vertical Displayed) must be programmed to one-half the actual number desired. For example, for 16 displayed characters high, R6 must contain 8 (decimal).
   - R7 (Vertical Sync Position) must be programmed to one-half the actual number desired.

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 13 illustrates the effect of the delays.

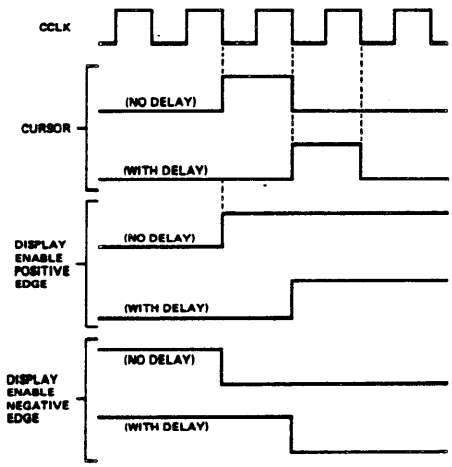


Figure 13. Cursor and Display Enable Skew

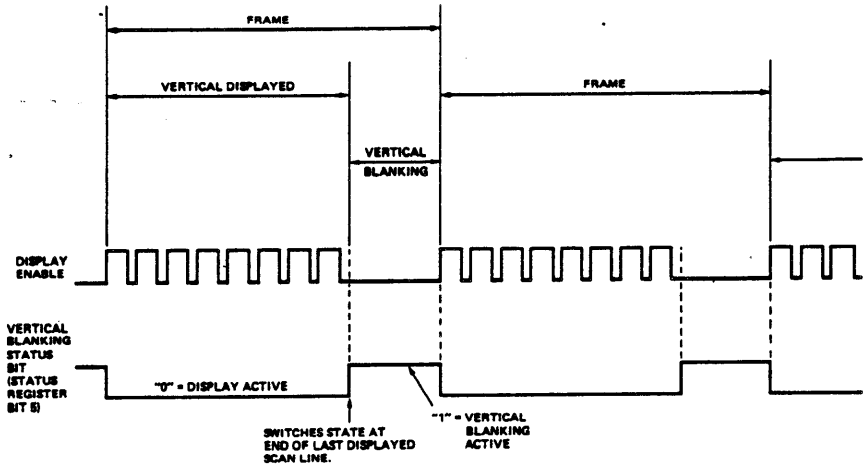


Figure 14. Operation of Vertical Blanking Status Bit

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TEL.: 514-735-1182 TELEX: 05-825651

QUARTO

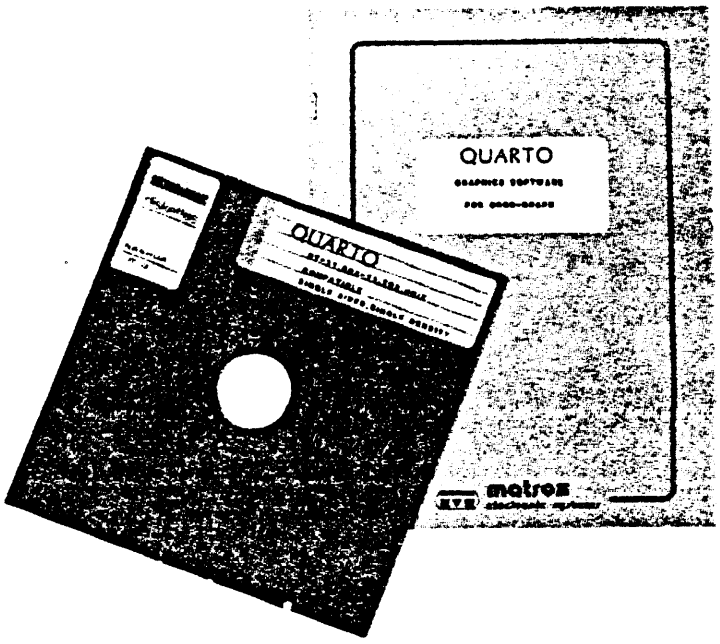
GRAPHICS SOFTWARE PACKAGE FOR QRGB-GRAPH

- **Software support package for QRGB-GRAPH**
- **Page-oriented graphics**
- **Supports scaling and windows**
- **Line, point, and character draw and erase commands**
- **Seed area fill**
- **RT-11, RSX-11, TSX, UNIX, and XENIX drivers available**
- **Special functions include: pan, scroll, zoom, and overlay**
- **Advanced character manipulation including inclined character baseline and character rotation**
- **Supplied on an 8" floppy diskette**

QUARTO is a software system for producing line drawings, plotting diagrams and graphs, and for other tasks in which the computer graphics device is used in the manner of a sketchpad and a set of colored pencils. QUARTO provides an extensive set of subroutines for writing graphic plots onto color or monochrome pages of a display, for making the written pages visible, or for hiding them.

QUARTO is designed to be used with a Matrox QRGB-GRAPH graphics display controller card, driven by a PDP-11/LSI-11 (Q-bus or Uni-bus) computer, and either a color or monochrome display monitor.

QUARTO is available for use with RT-11, RSX-11, TSX, TSX-PLUS, UNIX, XENIX, and other operating systems.



MATROX products covered by Canadian and foreign patent and/or patent pending.

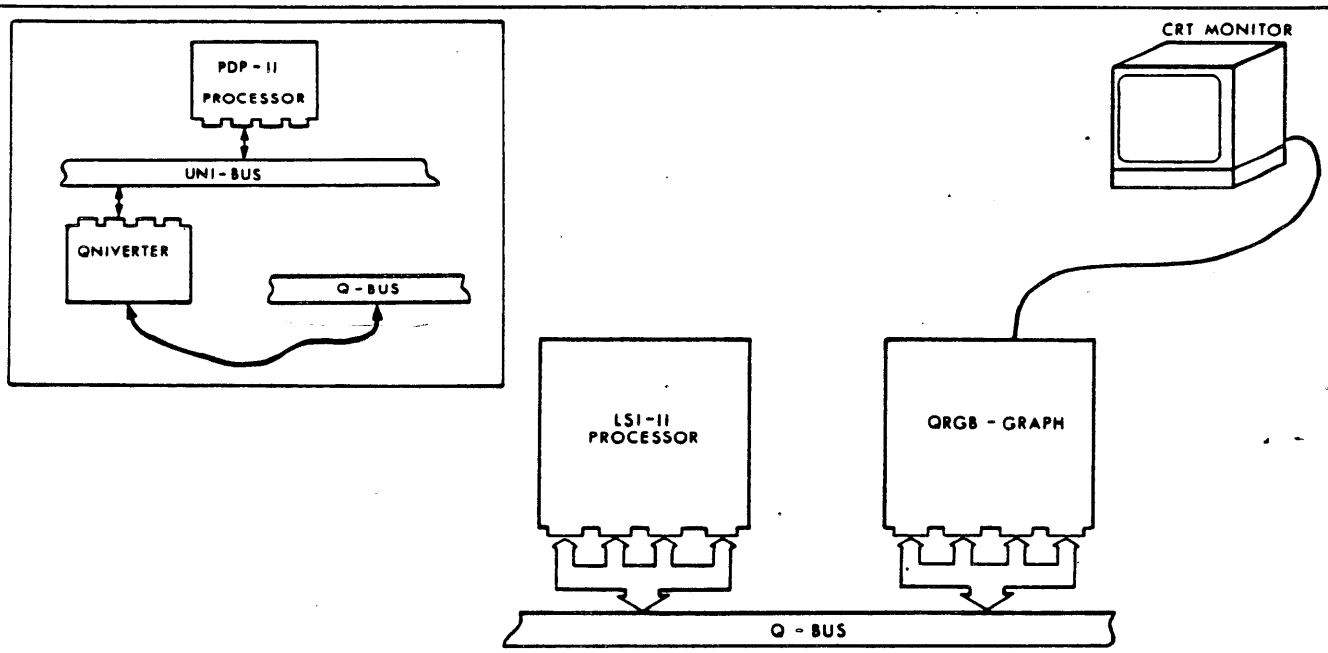


Figure 1. QUARTO — Typical application

FUNCTIONAL DESCRIPTION

The QUARTO software package is a library of subroutines supplied on an 8" floppy diskette. The QUARTO routines enable the user to create and manipulate graphic video displays, with up to 512 x 512 dot resolution, on a color or monochrome CRT monitor.

QUARTO is designed to be used with a Matrox QRGB-GRAPH graphics CRT display controller board driven by a PDP-11/LSI-11 (Q-bus or Uni-bus) processor, and is available for use with RT-11, RSX-11, TSX, TSX+PLUS, UNIX, XENIX, and other operating systems. QUARTO subroutines are furnished as threaded code and make use of the appropriate operating system library. These routines can generally be called from Fortran, Pascal, C, or assembler-language programs provided the standard system library is available. In addition to the subroutine library, a device driver may be required by certain operating systems. Where needed, the standard QUARTO release package includes such a driver.

The QUARTO software package employs a "paged graphics" technique, whereby the four display planes of the QRGB-GRAPH are grouped together to form one or more "pages" (analogous to sheets of drawing paper), each of which can be written on, erased, cleared, displayed, or otherwise manipulated individually. The four display planes of the QRGB-GRAPH can be configured, by QUARTO, to form eight different combinations of pages (Virtual Machines).

MACHINE	NUMBER OF PAGES	DESCRIPTION
1111	4	Four monochrome pages (one plane each)
2110	3	One four-color page (two planes) and two monochrome pages (one plane each)
2111	3	Same as Machine 2110 except using different colors (different plane-page configuration)
2112	3	Same as Machine 2111 except using different colors (different plane-page configuration)
220	2	Two four-color pages (two planes each)
221	2	Same as Machine 220 except using different colors (different plane-page configuration)
222	2	Same as Machine 221 except using different colors (different plane-page configuration)
31	2	One eight-color page (three planes) and one monochrome plane (one plane)

Table 1. Virtual Machines supported by QUARTO

PAGED GRAPHICS

The Paged Graphics routines in QUARTO are used to define and manipulate the working, or "environmental", parameters of the display on a page level. Page control routines allow the user to individually enable the video output from each page, enable/disable writing to each page, or clear a specified page to a specified color. The enable/disable video routine allows several pages to be overlayed on the screen together. Displays may also be combined in many complicated ways by merging the contents of two pages into a single page. In the merging process both pages to be merged are read, pixel by pixel, and rewritten in accordance with whatever logical function the user has chosen to specify. Full or partial images can also be transferred, through QUARTO, between the display and disk.

An initialization routine (QRINIT) loads a set of default parameters for QUARTO (table 2). QRINIT defines such parameters as: currently active Virtual Machine, currently active page, and graphics pen color. Other routines in the Paged Graphics library allow the user to dynamically update these parameters. Routines are included to set the display resolution in terms of virtual coordinates (i.e. X and Y coordinates are expressed in the range of 0 to 1.0) for each page, and to map this virtual window onto a defined portion of the screen. This feature allows the programmer to display several windows on the page simultaneously (figure 2).

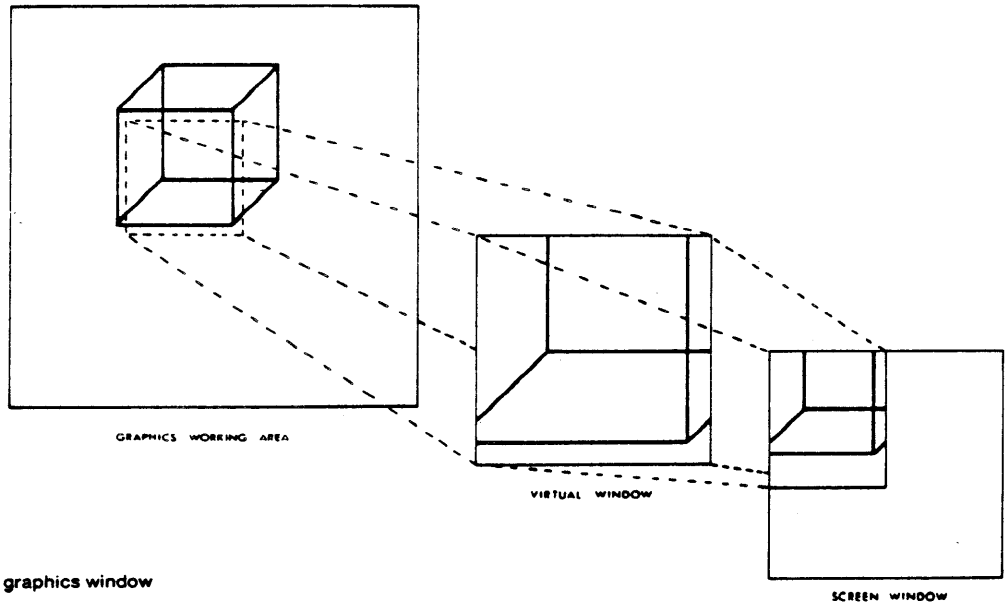


Figure 2. Virtual graphics window

PARAMETER	DESCRIPTION	DEFAULT VALUE
PAN	Starting column number at left side of display	Column 0
SCROLL	Starting row number at top of display	Row 0
ZOOM	X and Y zoom factors	X = 1, Y = 1
RESOLUTION	X and Y resolution	512 x 512
PAGE	Activates page to display	Page 0 active
COLOR	Sets pen color	Red
VIRTUAL WINDOW	Sets resolution of virtual window	1.0 x 1.0
SCREEN WINDOW	Sets resolution of screen window	512 x 512
MACHINE	Select Virtual Machine	31
POSITION	Set X and Y coordinates of graphics pen	X = 0, Y = 0

Table 2. QUARTO default parameters

A separate routine is available to enable the programmer to introduce horizontal and vertical offsets, when drawing characters, to simulate a sloped character baseline.

VIRTUAL LINE GRAPHICS

Virtual Line Graphics routines are used to actually construct the images on the currently active page. Lines, points, and characters can be written to the display using routines found in the Virtual Line Graphics library. Characters that can be drawn to the display include all of the upper and lower case alphanumeric characters as well as any user-defined characters. Strings of characters can be drawn to the currently active page using powerful character manipulation routines. Characters can be increased in size up to 42 times their normal height and can be rotated, in multiples of 90°, to a maximum of 360°.

Writing to the display is done in one of five modes. In mode 0, the graphics pen is moved along its perscribed route without writing. Mode +1 enables writing in a specified color, regardless of the previous or background color. A Masked Complemented Writing mode (−1) causes each point on the pen route to be written in a color obtained by complementing those bits of the existing color which correspond to zero bits in the specified pen color (eg. a cyan pen (110), writing on a yellow background (011), yields a green (010) line). Modes +2 and −2 refer to Additive Relative Writing and Subtractive Relative Writing respectively. In these modes, the new point color is determined by either adding or subtracting the pen color from the previous point color. An area fill routine (QRVNFL) is also incorporated in QUARTO which allows the use to "color" a defined area of the display. QRVNFL can also be used to copy filled areas between pages.

PIXEL ADDRESSED GRAPHICS

The Pixel Addressed Graphics subroutines in QUARTO deal with the pixel addresses as integer pixel numbers and may be regarded as being the low-level access to the actual hardware. For applications requiring maximum memory use, graphics at the pixel level can be very advantageous. Where it is desirable to embed these routines in PROM firmware, a separate "embedded code licence" is available.

DEBUGGING FACILITY

To aid in debugging programs incorporating QUARTO, many of the subroutines supply debugging information to the programmer in the form of error messages displayed at the system console. These error messages are presented in the form of a four character code, of which the first two characters define the error type and the last two characters identify the subroutine.

Parallel versions of subroutines are provided wherever the error reporting facilities have a significant effect on either execution time or code length (routines of the form QDxxxx incorporate debug error reporting). QRxxxx versions of the routines (no error reporting facilities) should be used in the final production program since these routines generally run faster.

SUMMARY OF QUARTO ROUTINES

PAGED GRAPHICS ROUTINES

NAME	FUNCTION
QRCPOS	Specify character pen beginning and ending position
QDCPOS	
QRINIT	Initialize all hardware and software parameters
QRMERG	Merge two pages
QDMERG	
QRPAGE	Write enable selected page (only one page can be write enabled at one time)
QDPAGE	
QRPCLR	Clear specified page to specified color
QDPCLR	
QRPVEN	Enable/disable video from specified page
QDPVEN	
QRECN	Select current virtual machine for page graphics
QDECN	
QRSAVE	Store specified portion of current picture on disk
QDSAVE	
QRSERS	Disable video from all pages
QRSTAT	Display current graphics system status
QRSWIN	Define screen window to be used on specified page
QDSWIN	
QRVWIN	Define virtual window to be used on specified page
QDVWIN	
QRWRIT	Restore saved picture from disk to display buffer
QDWRIT	

VIRTUAL LINE GRAPHICS ROUTINES

NAME	FUNCTION
QRCCHR	Draw an array of ASCII characters
QDCCHR	
QRVCHR	Draw an ASCII character
QDVCHR	
QRVLIN	Draw a line in virtual space
QDVLIN	
QRVNFL	Fill an area
QDVNFL	
QRVPNT	Draw a point at the specified virtual coordinates
QDVPNT	
QRVSCH	Draw a user-defined character
QDVSCH	
QRVVCH	Draw a string of user-defined characters
QDVVCH	

PIXEL ADDRESSED GRAPHICS ROUTINES

NAME	FUNCTION
QRACLR	Clear specified planes and set to specified color
QDACLR	
QRHCLP	Enable/disable hardware clipping
QDHCLP	
QRHPAN	Pan display to specified X coordinate
QDHPAN	
QRHSCR	Scroll display to specified Y coordinate
QDHSCR	
QRHZOM	Zoom display by specified zoom factor
QDHZOM	
QRRPDX	Read pixel color from specified location
QDRPDX	
QRSCHV	Draw a user-defined dot matrix character
QDSCHV	
QRSPCH	Draw a dot matrix character
QDSPCH	
QRWPXL	Write a pixel to the specified location in the specified color
QDWPXL	
QRWREN	Write enable the specified plane (one plane is enabled per call but any number of planes can
QDWREN	be write enabled at any one given time)
QRWVCT	Draw a line of pixels
QDWVCT	

ORDERING INFORMATION

QUARTO Graphics software package on an 8" floppy diskette. When the QUARTO package is ordered, the user must complete a licensing agreement, and a configuration form.

Matrox Electronic Systems Ltd reserves the right to make changes in specifications at any time and without notice. The information furnished by Matrox Electronic Systems Ltd in this publication is believed to be accurate and reliable. However, no responsibility is assumed by Matrox Electronic Systems Ltd for its use; nor for any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of Matrox Electronic Systems Ltd.

LICENSE AGREEMENT AND CONFIGURATION FORM

QUARTO is configured and fully maintained for the target system by Infolytica Corporation. Licenses are available for single systems, multiple systems and embedded use. Quarto can be ordered at your nearest MATROX sales outlet.

The forms on the following pages are for those who wish to purchase the Infolytica Graphics Package (Quarto). The purchaser should fill out the Licence Agreement and the Configuration Form and return it to MATROX or one of its distributors along with the order.

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Installed at:

Signatures

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(organization, site, address)

_____

_____

(signature) (date)

for licensor:
Infolytica Corporation, 1500 Stanley, Suite 321, Montreal, Que. H3A 1R3

_____

(signature) (date)

QUARTO CONFIGURATION

The following form must be completed correctly in order to produce a version of QUARTO which will operate with the user's hardware configuration.

The standard distribution medium for QUARTO is a double density RX02 formatted diskette capable of being read by the operating system for which it has been generated. Other media may be used at a purchaser's request, e.g. single density diskettes or magnetic tape, but will incur an extra charge.

The delivered system will contain two libraries in object form, QUARTO.OBJ and QUADTO.OBJ, the latter being the debugging version. In addition one driver will be included. If a user's hardware configuration changes after purchase of QUARTO so that the supplied libraries will no longer operate, then Infolytica will perform one reconfiguration free of charge. Further reconfiguration will be subject to a small charge.

The information supplied on this form mainly concerns the operating system with which the system will run. It also asks whether the full facilities of QUARTO as described below, are required. Some saving in space may be obtained if, for example, the filling stack depth is reduced; the effect of this being to reduce the complexity of the shapes which may be filled. By omitting filling, saving, and merging, considerable reductions can be made in the size of the driver.

The Filling Operation

QUARTO provides subroutines which will fill areas on the current graphics page using any of the possible drawing modes. The area must be bounded by a polygon. The algorithm used is a 'seed fill'. It is also possible to fill an area on one page by using a polygon defined on another. This operation requires 457 words of memory resident in the driver. In addition a data area is required to act as a stack; the required stack depth depends on the convexity of the polygon. The larger the stack, the more complex the polygon may be. The default stack depth is 200 words, but memory may be saved by reducing the size at the expense of simplifying the shapes that may be filled. It should be noted that any complex area can be constructed from simpler ones and thus several fill operations may well accomplish the task.

The Reading/Writing Blocks Option

QUARTO provides subroutines which can save a section or all of a picture in a disk file, or restore it. Additionally QUARTO can merge pictures on two separate pages, via a user-defined logical function, onto one page. These features allows sections of a screen picture to be moved around a page and to be moved from page to page. It also allows the creation of extra 'pages' on disk, thus allowing the graphics system to appear much larger than it actually is. These facilities require the "Reading/Writing blocks Option' within the driver, and this needs 285 words of memory.

The Chained Characters Option

QUARTO provides subroutines which can display 'chained characters', i.e., characters which are constructed by relative operation using short vectors. Each piece of a character is defined by the direction and distance to be moved from the current pen position. This results in a character definition which allows complex characters to be defined, e.g., a graphic cursor, or special font, and these characters may be magnified or rotated by simple operations. Thus graphics primitives such as a 'box', a 'filled rectangular area', etc., may be added to QUARTO. This facility requires 158 words of memory resident in the driver. In addition, if the virtual level chained character routines are used, a chained character set is loaded which will require 1000 words of user memory.

QUARTO CONFIGURATION FORM

Name of Organization: _____

Address of Organization: _____

_____

_____

Target Operating System:
Circle one of the following:

RT11-SJ, RT11-FB, RT11-XM, TSX, TSX-PLUS

RSX11-M, UNIX V7, XENIX - these systems not available till first quarter 1983

Interrupt Vector Address
(default: 400):

_____

Base Address for QRGB card
(default : 776400) :

_____

For the following question please circle the required response:

European or American T.V.?
(this alters the number of displayed lines) :

EUROPEAN / AMERICAN

_____

512/64/4 OR 512/64/1 card?
(multiple bit plane or single -
default : multiple) :

MULTIPLE / SINGLE

_____

Include Filling
(This requires 457 words of
memory in the driver - default :
included) :

INCLUDE / LEAVE OUT

Stack Depth for Filling
(The greater the depth, the more
complex the shapes filled, default:
200 words) :

300 250 200 150 100 50 Other (specify):

Include Block Read/Write
(This requires 285 words of memory
but allows picture saving, restoring
and merging - default : included) :

INCLUDE / LEAVE OUT

Include Chained Characters
(This requires 158 words of memory
but allows the use of chained
characters - default : included) :

INCLUDE / LEAVE OUT

NOTE: The full driver, with all defaults, occupies 1897 words of memory on RT-11.

Does your Fortran compiler generate
threaded or inline code?
(default : threaded) :

THREADED / INLINE

Is the target operating system
generated with manufacturer's
default SYSGEN options?
(default : yes) :

YES / NO

If the answer is NO, please attach a description of the system generation options.

APPENDIX C GLOSSARY

The following glossary defines some of the terms used by MATROX, and should prove helpful when reading schematics or register bit names.

AB	Address Bus
ADDR	ADDRess (for look-up table)
AEN	Address ENable
A. GND	Analog GrouND
ALTMAP	ALTernate Map
AR	Address Register
BAEN	Bus Address ENable
BB	Blink Background
BDAL	Bus Data Address Line (0-F)
BCLE	Bus CycLe Enable
BD	Bus Data
BDIN	Bus Data INput
BDMGI	Bus DMa Grant Input
BDMGO	Bus DMa Grant Output
BDOUT	Bus INITialization
BF	Blink Foreground
BIAKO	Bus Interrupt Acknowledged Output
BIAKI	Bus Interrupt Acknowledged Input
BIRQ4	Bus Interrupt ReQuest level 4
BRPLY	Bus RePLY
BSYNC	Bus SYNCronization
BUSPIR	BUS DIRection
CAS	Column Address Strobe
CBLAK	Composite BLAnKing
CBLANK	Composite BLANKing

APPENDIX C GLOSSARY

CCLK	Cell CLocK/Continous CLocK
CG	Character Generator
C.G.M.	Character Generator Memory
C.H.P.	Character Height PROM
CLK	CLocK
CMD	CoMmanD
CMP	CoMParator
CO	Carry Out/Column 0
COMP	COMPosite
CPU	CPU access to look-up table
CRT	Cathode Ray Tube
CRTC	Cathode Ray Tube Controller
CSYNC	Composite SYNC (HOR + VERT)
CUDISP	CUrsor DISPlay
DAC	Digital-Analog Converter
DAL	Data Address Line
DB	Data Bus
DCLK	Dot CLocK
DEC	DECoder
DECX	DECrement X
DECY	DECrement Y
D. GND	Digital GrouND
DIN	Data INput
DISPEN	DISPlay ENable
DISPTMG	DISPlay TiMinG

APPENDIX C

GLOSSARY

DOUT	Data OUTput
DOUTOR DIN	Data OUT or Data IN
DW	Data Write
EN	ENable (buffer for look-up table) (0-2)
EXH	EXtended Height
EXHE	EXtended Height
FDS	Frame Data Strobe
FGR	Frame GRab
HRS	Holding Register Storage
HSYNC	Horizontal SYNChronization
IAKI	Interrupt Acknowledged Input
INCX	INCrement X
INCY	INCrement Y
INIT	INITialize (Reset)
INTREQ	INTerrupt REQuest
INTRPLY	INTerrupt RePLY
LAD	Latched ADresses (0-a)
LD	LoaD clock
LPSTB	Light Pen STroBe
LSB	Least Signifigant Bit
MA	Refresh Memory Address
MACLK	Memory Access CLocK
MPU	MicroProcessor Unit
MPX	MultiPleXer
MSB	Most Signifigant Bit
MWR	Memory WRite

APPENDIX C GLOSSARY

OFGN	OFfset and GaiN
P->S	Parallel-Serial Converter
PLL	Phase Lock Loop
PRMEM	PReset MEMory
RA	Raster Address/RAM Address
RAS	Row Address Strobe
R/C	Row/Column
REF	REFerence
RES	RESolution
RM	Refresh Memory
RS	Register Select
R Status	Read STATUS
SCLK	System CLocK
SD	Serial Data
SEL	SELect
SH/LD	SHift/LoaD
SYN RD	ReaD SYNchronize
SYN WR	WRite SYNchronize
TEXT	TEXTure
T.P.	Test Point (0-11)
ULN	UnderLiNe
VB	Video Bus (0-7)
VCO	Voltage Controlled Oscillator
VDO	ViDeO

APPENDIX A GLOSSARY

VEN	Video ENable
VFRAM	start of new FRAMe
VFU	Vertical Format Unit
V. RESET	Vertical Reset
VSYNC	Vertical SYNChronization
WCRTC	Write to CRTC
W DATA H	Write DATA High
W DATA L	Write DATA Low
WDOT	Write DOT
WEN	Write ENable
WR	WRite (look-up table)
WRS	WRiteStrobe
WRT	WRite Texture

* * * * *

APPENDIX D COLOUR MAP TABLE :

This Appendix contains two sections. The first lists all the colors available from the as-shipped color map EPROM. Its Matrox number is 156-0 and it occupies position A26 on the QRGB-Graph board. The second lists all the colors provided in the optional Quarto EPROM, which is provided with the Quarto Software Package. Its Matrox number is 053-1 and it also occupies position A26 on the QRGB-Graph board. Note that the Standard as-shipped EPROM contains 16 maps that are reserved for the user's own colours. These will display white when they are accessed, until are programmed. The lowest order map (MAP 0) resides at the lowest 16 addresses the next map (MAP 1) resides at the next 16 higher addresses, and so on.

The following charts indicate which colour is selected when a certain bit configuration is loaded into the 4 bit planes of the Display Memory (x indicates "don't care"):

D.1 STANDARD EPROM LISTING:

COLOUR MAP #0

MAP	BIT PLANE [3210]	COLOUR
MAP 00	xxxx	BLACK (REGARDLESS OF INPUT)

COLOR MAP #01

BIT PLANE [0123]	SHADE (GREY SCALE)	COLOUR
0000	BLACK	BLACK
0001	GREY 8	RED
0010	" 4	DARK BLUE
0011	" 12	MAGENTA
0100	" 2	GREEN
0101	" 10	BROWN-GREEN
0110	" 6	DARK CYAN
0111	" 14	WHITE-PURPLE
1000	" 1	DARK GREEN
1001	" 9	BROWN
1010	" 5	LIGHT BLUE
1011	" 13	LIGHT MAGENTA
1100	" 3	LIGHT GREEN
1101	" 11	YELLOW-GREEN
1110	" 7	LIGHT CYAN
1111	WHITE	WHITE

1 STANDARD EPROM LISTING (cont'd):

MAP	BIT PLANE [3210]	COLOUR
MAP 02	000x	BLACK
	100x	DARK GREEN
	010x	GREEN
	110x	LIGHT GREEN
	001x	DARK BLUE
	101x	LIGHT BLUE
	011x	DARK CYAN
	111x	LIGHT CYAN
MAP 03	xxx0	BLACK
	xxx1	RED
MAP 04	00xx	BLACK
	10xx	DARK GREEN
	01xx	GREEN
	11xx	LIGHT GREEN
MAP 05	xx0x	BLACK
	xx1x	BLUE
MAP 06	00x0	BLACK
	10x0	DARK GREEN
	01x0	GREEN
	11x0	LIGHT GREEN
	00x1	RED
	10x1	BROWN
	01x1	BROWN-GREEN
	11x1	YELLOW-GREEN
MAP 07	xx00	BLACK
	xx10	BLUE
	xx01	RED
	xx11	MAGENTA
MAP 08	0xxx	BLACK
	1xxx	DARK GREEN
MAP 09	x0xx	BLACK
	x1xx	GREEN
MAP 10	0x0x	BLACK
	1x0x	DARK GREEN
	0x1x	BLUE
	1x1x	LIGHT BLUE

D.1 STANDARD EPROM LISTING (cont'd):

MAP	BIT PLANE [3210]	COLOUR
MAP 11	x00x	BLUE
	x10x	GREEN
	x01x	BLUE
	x11x	DARK CYAN
MAP 12	0xx0	BLACK
	1xx0	DARK GREEN
	0xx1	RED
	1xx1	BROWN
MAP 13	x0x0	BLACK
	x1x0	GREEN
	x0x1	RED
	x1x1	BROWN-GREEN
MAP 14	0x00	BLACK
	1x00	DARK GREEN
	0x10	BLUE
	1x10	LIGHT BLUE
	0x01	RED
	1x01	BROWN
	0x11	MAGENTA
	1x11	LIGHT MAGENTA
MAP 15	x000	BLACK
	x100	GREEN
	x010	BLUE
	x110	DARK CYAN
	x001	RED
	x101	BROWN-GREEN
	x011	MAGENTA
	x111	WHITE-PURPLE

NOTES:

1) The first bit plane (bit plane 0) controls the Red D/A converter.

2) Bit plane 1 controls the Blue D/A converter.

3) Bit plane 2 controls the Light Green D/A converter.

4) The last bit plane (bit plane 3) controls the Dark Green D/A converter.

5) Maps 16-32 (called by ALTMAP=1) have been left un-programmed so that the user can set up his own colours.

D.2 QUARTO EPROM LISTING:

MAP	BIT PLANE [3210]	COLOUR
0	xxxx	BLACK
1	xxx0	BLACK
	xxx1	RED
2	x0xx	BLACK
	x1xx	GREEN
3	xx0x	BLACK
	xx1x	BLUE
4	0xxx	BLACK
	1xxx	WHITE
5	0000	BLACK
	0001	RED
	0010	BLUE
	0011	MAGENTA
	0100	GREEN
	0101	YELLOW
	0110	CYAN
	0111	WHITE
	1xxx	WHITE
6	xx00	BLACK
	xx01	RED
	xx10	BLUE
	xx11	MAGENTA
7	x0x0	BLACK
	x0x1	RED
	x1x0	GREEN
	x1x1	YELLOW

D.2 QUARTO EPROM LISTING (Cont'd):

MAP	BIT PLANE [3210]	COLOUR
8	0xx0	BLACK
	0xx1	RED
	1xxx	WHITE
9	x00x	BLACK
	x01x	BLUE
	x10x	GREEN
	x11x	CYAN.
10	0x0x	BLACK
	0x1x	BLUE
	1xxx	WHITE
11	00xx	BLACK
	01xx	GREEN
	1xxx	WHITE
12	x000	BLACK
	x001	RED
	x010	BLUE
	x011	MAGENTA
	x100	GREEN
	x101	YELLOW
	x110	CYAN
	x111	WHITE
13	0x00	BLACK
	0x01	RED
	0x10	BLUE
	0x11	MAGENTA
	1xxx	WHITE
14	00x0	BLACK
	00x1	RED
	01x0	GREEN
	01x1	YELLOW
	1xxx	WHITE

QUARTO EPROM LISTING (Cont'd):

MAP	BIT PLANE [3210]	COLOUR
15	000x	BLACK
	001x	BLUE
	010x	GREEN
	011x	CYAN
	1xxx	WHITE
16	0x00	BLACK
	0x01	RED
	0x10	BLUE
	0x11	MAGENTA
	1xx0	CYAN
	1xx1	WHITE
17	x000	BLACK
	x001	RED
	x010	BLUE
	x011	MAGENTA
	x10x	YELLOW
	x11x	WHITE
18	0000	BLACK
	0001	RED
	0010	BLUE
	0011	MAGENTA
	010x	YELLOW
	x11x	WHITE
	10x0	CYAN
	1xx1	WHITE
	11xx	WHITE
19	0xxx	BLACK
	1xxx	CYAN
20	x0xx	BLACK
	x1xx	YELLOW

D.2 QUARTO EPROM LISTING (Cont'd):

MAP	BIT PLANE [3210]	COLOUR
21	00xx	BLACK
	01xx	YELLOW
	10xx	CYAN
	11xx	WHITE
22	00x0	BLACK
	00x1	RED
	01x0	GREEN
	01x1	YELLOW
	1xx0	CYAN
	1xx1	WHITE
23	x000	BLACK
	x001	RED
	x01x	MAGENTA
	x100	GREEN
	x101	YELLOW
	x11x	WHITE
24	0000	BLACK
	0001	RED
	001x	MAGENTA
	0100	GREEN
	0101	YELLOW
	x11x	WHITE
	1x00	CYAN
	1xx1	WHITE
	1x1x	WHITE
25	xx0x	BLACK
	xx1x	MAGENTA
26	0x0x	BLACK
	0x1x	MAGENTA
	1x0x	CYAN
	1x1x	WHITE

D.2 QUARTO EPROM LISTING (Cont'd):

MAP	BIT PLANE [3210]	COLOUR
27	0xx0	BLACK
	0xx1	GREEN
	1xx0	BLUE
	1xx1	CYAN
28	0xx0	BLACK
	0xx1	GREEN
	01xx	YELLOW
	1xx0	BLUE
	1xx1	CYAN
	11xx	WHITE
29	0x00	BLACK
	0x01	GREEN
	xx10	MAGENTA
	xx11	WHITE
	1x00	BLUE
	1x01	CYAN
30	0000	BLACK
	0001	GREEN
	x010	MAGENTA
	xx11	WHITE
	010x	YELLOW
	x11x	WHITE
	1000	BLUE
	1001	CYAN
	11xx	WHITE
31	x00x	BLACK
	x01x	MAGENTA
	x10x	YELLOW
	x11x	WHITE

* * * * *

APPENDIX E TROUBLESHOOTING HINTS

The following hints should be followed if the initialization of the board is not succcessful or if trouble develops when the graphics system is altered.

1) Check the bus. Are all boards fully inserted? Are any boards touching? Also do the initialization more than once. (Section 3, Page 3-1). It is very easy to misload a digit or two, and doing this can result in a very strange display, or no display at all. Note that the parameters given are based on the average monitor. The numbers may need to be altered slightly from the values given to work properly with your monitor.

2) Check the monitor. The video output from J1 (Section 7.2, Page 7-4) is a composite signal (video + sync) at 1V P-P. Output impedence is 75 ohms.

3) Check the power supply. For the average fully loaded system, upwards of 10A may be required from 5V supply. Also check the auxiliary supplies. The QRGB-Graph draws about 3.0A from the 5V line.

4) If there are other boards capable of generating a composite video signal, connect the monitor to them to determine where the problem lies.

5) Check the location of all I/O ports and memory addresses to make sure there is no conflict in your system.

Our Addresses:

I/O - 164400 - 164417 (Octal)
DMA - 164000 - 164377 (Octal)
Interrupt - 400 (Octal)

Remember that all these addresses can be changed by altering the strap configurations as shown in Section 5, Page 5-1, so check the addresses to be sure that the board is located where you expect it to be.

6) The Register listing can be found on the following page, and should be used with the diagrams in the back of this book to trace signal paths on the board.

If the system still will not work please contact us for further help. Whether you write or phone, have full details prepared about your system: what happened, your system's environment and peripherals, and anything else you feel will help our staf service your problem.

APPENDIX E TROUBLESHOOTING HINTS (Cont'd)

REGISTER	SECTION	R/W	ADDRESS	I.C.
X-REGISTER	4.3.1	R/W	164400_8	WRITE: A91, A76, A64 READ: A106, A53
Y-REGISTER	4.3.2	R/W	164402_8	WRITE: A92, A77, A63 READ: A107, A53
DATA	4.3.5	R/W	164404_8	A113(-7, -9), A70(-7, -9)
STATUS	4.3.7	R/O	164406_8	A40-11
CONTROL #1	4.3.8	W/O	164406_8	A55, A29
LIGHT PEN	4.3.10	R/O	164410_8	A49
CONTROL #3	4.3.11	W/O	164410_8	A31
CONTROL #4	4.3.13	W/O	164412_8	A30
CRTC STATUS	4.3.14	R/O	164414_8	A42
CRTC ADDRESS	4.3.15	W/O	164414_8	A42
VECTOR	4.3.16	W/O	164415_8	A89
CRTC DATA	4.3.17	R/W	164416_8	A42
CONTROL #5	4.3.18	W/O	164417_8	A9-2, A57-2 STRAP 160, STRAP 162

TABLE E - REGISTER LISTING

*****

APPENDIX F PAIRED REGISTERS

Because of the disciplines imposed by the LSI-11 Q-BUS, access to all registers on the QRGB-Graph must be word-wide (16-bits), and aligned on an even octal word boundary. The inherent nature of some of the registers on the QRGB-Graph, however, because of their function, are byte-wide and aligned on an odd octal boundary. These registers must each be paired with an even-addressed register and the pair must be accessed simultaneously in a 16-bit word transfer. The following list gives the register pairs that must be accessed in this way.

REGISTER PAIR	BASE ADDRESS
Vector Register (High Byte) - CRTC Address Register (Low Byte)	164414_8
Control Register #5 (High Byte) - CRTC Data Register (Low Byte)	164416_8

Obviously, it is often not desirable to change the contents of both registers in the pair at the same time, so the following methods have been developed to enable byte-wide changes in a word-wide environment:

1) To write to CRTC address register (X = your entry)

VECTOR								CRTC ADDRESS							
0	0	0	1	0	0	0	0	X	X	X	X	X	X	X	X

BASE ADDRESS = 164414_8 *

2) To write to vector register (X = Your Entry):

VECTOR								CRTC ADDRESS							
0	0	0	X	X	X	X	X	0	0	0	1	1	1	1	1

BASE ADDRESS = 164414_8

*Note that the entry in the CRTC address register points to dummy register #31, which is a valid location but does nothing.

3) To read from the CRTC Data Register:

   i) Write to CRTC Address Register as in (1).

   ii) Read CRTC Data as a word.

APPENDIX F PAIRED REGISTERS(cont'd)

4) To write to the CRTC Data Register (X = Your Entry):

i) Write to CRTC Address Register as in (1)

ii) Write Data as a word after "OR"ing in Master-slave bits, Frame grab bits, and Preset bits on control register #5.

CONTROL #5								CRTC DATA								
X	X	0	0	0	0	X	X	X	X	X	X	X	X	X	X	BASE ADDRESS = 164416_8

5) To write to Control Register #5 (x = Your Entry):

i) Disable Vector and Address the CRTC Dummy Register:

VECTOR REGISTER								CRTC ADDRESS								
0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	BASE ADDRESS = 164414_8

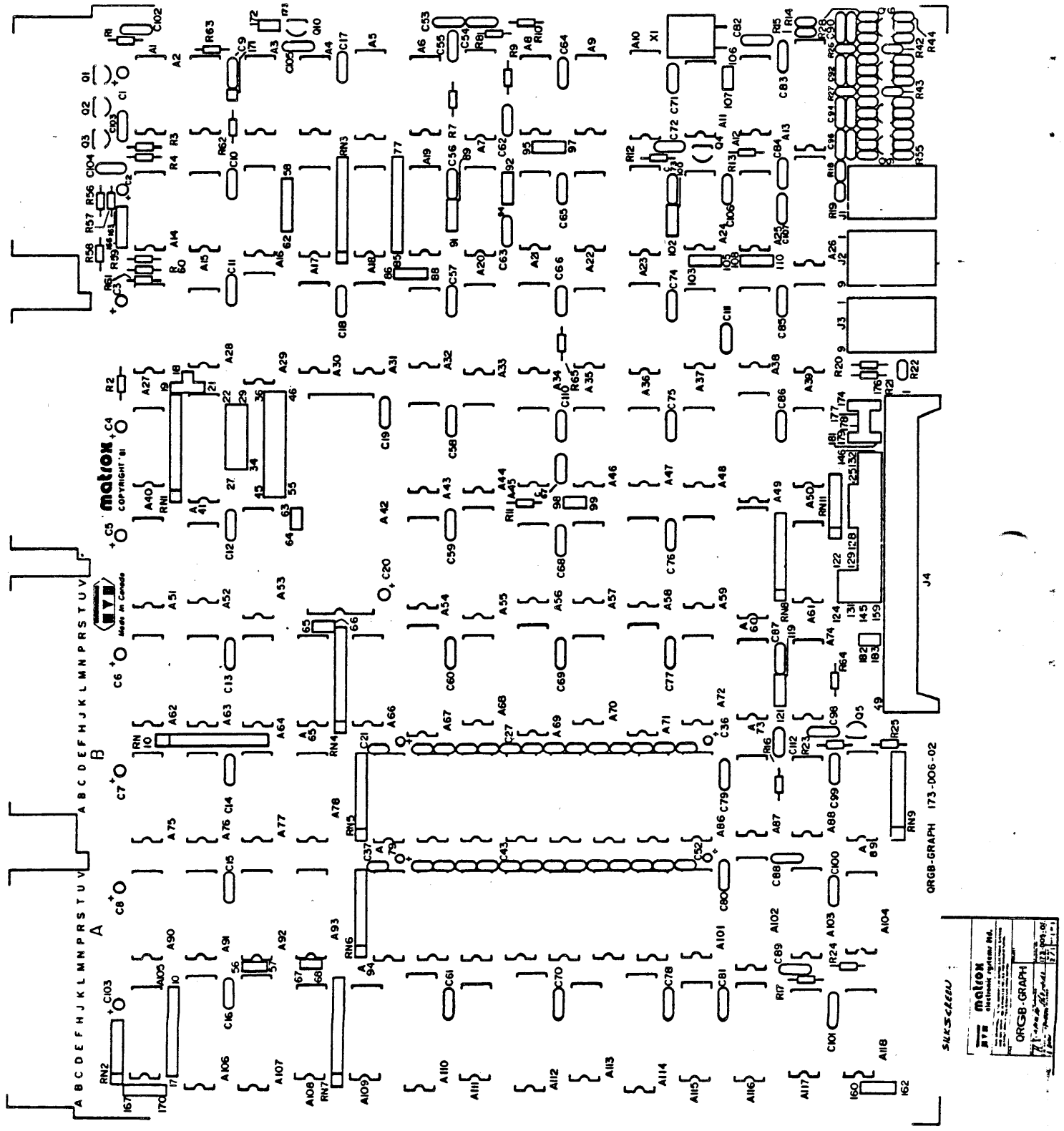
ii) Write to the Register Pair as a word:

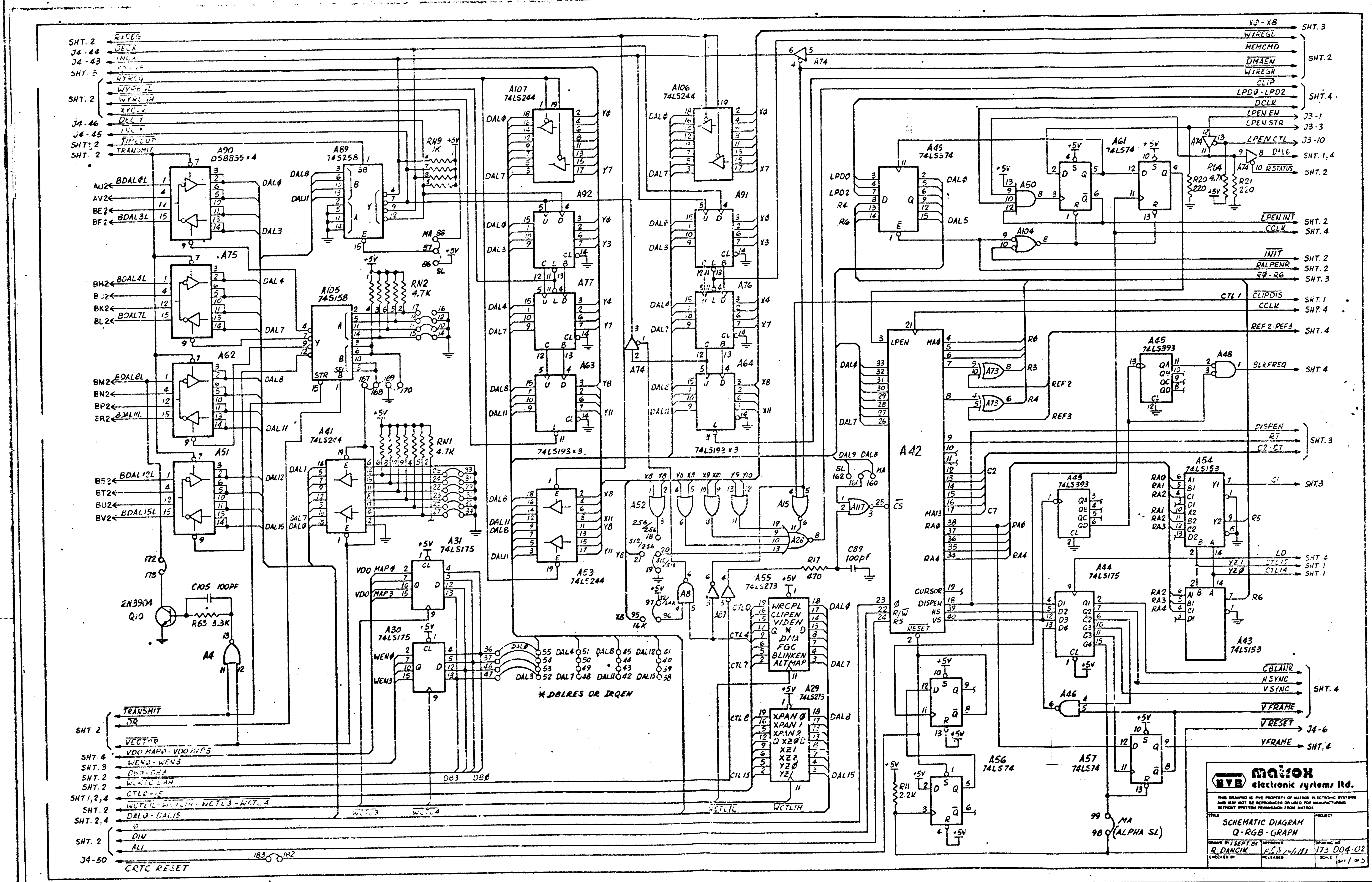
CONTROL #5								CRTC DATA								
X	X	0	0	0	0	X	X	0	0	0	0	0	0	0	0	BASE ADDRESS = 164416_8

* * * * *

APPENDIX G

PARTS LAYOUT

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SCHEMATIC DIAGRAM
Q-RGB-GRAPH
R. DANCIK
173 D04-02
A42
A90 DS8835×4
A89 74S258
A105 74S158
A41 74LS244
A107 74LS244
A106 74LS244
A53 74LS244
74LS193×3
A45 74LS374
A61 74LS74
A56 74LS74
A57 74LS74
A44 74LS175
A54 74LS153
A43 74LS153
A55 74LS273
A29 74LS273
A30 74LS175
A31 74LS175
*DBLRES OR IRQEN
CRTC RESET

BASE ADDRESS
164400_8

AP2 BBSTL
SHT. 1 DAL0 - DAL12
SHT. 1 DMAEN CTL 4
AN2 BIAKOL
AL2 BIRQ4L
AH2 BDINL
AE2 BDOUTL
AN2 BWTBTL
AJ2 BSYNCL
AT2 BINITL
AM2 BIAKIL
SHT.4 MWR
SHT. 2 MRD
SHT. 1,4 DIN
HEMCMD
TRANSMIT
VECTOR INIT
TRANSMIT
LPEN INT
DRM INT
SHT. 4 SEL
AF2 BRPLYL
SHT.4 VECTOR BUSY
SHT. 1 TIMEOUT
SHT. 1 YYCLK
SHT. 4 IRQEN

A16 74LS174
A17 DM8131 x 2
A18
RN3 2.2K
A32
A4
A3
A15
A37
A27 DS8837
A14
A47
A28
A50
A1
A2 74S74
A35
A5 74LS155
A6
A7 9602
A48
A52
A103 74LS157
A116 74LS175
A117
A102 74LS241
A104
A88
A19 74LS155
A20 74LS155

R57 330
R56 680
R4 3.3K
R3 3.3K
C104 100pF
C103 100pF
Q3 2N3904 x 2
Q2
R62 4.7K
R60 330
R61 680
R59 4.7K
R58 4.7K
R10 470
R9 10K
C62 100pf
C53 100pf
C102 100pF
Q1 2N3904
R1 3.3K
R8 470
R7 2.2K
C55 220pf
C54 100pf

DAL12 DAL9 DAL8 DAL4 DAL3 DAL0 AL3 AL0
AL3 AL2 AL1
RCRTCD RCRTCS
R DATA

MD0 - MD3 SHT. 3
DB0 - DB3 SHT. 1
DW SHT. 4
WRCPL-CTL10 SHT. 1
MRD SHT. 2
SYNRD SHT. 4
CAS SHT. 3,4
DR SHT. 1
RALPENR SHT. 1
RSTATUS SHT. 4
RYREG
RXREG
WCRTCD
WCRTCA
AL0 - AL3 SHT. 1
WCTL4
WCTL3
WCTL1L
W DATA SHT. 4
WYREGL SHT. 1
WXREGL SHT. 1
WCRTCDIR SHT. 1,4
WDOT SHT. 4
WCTL1H
WYREGH
WXREGH SHT. 1
Ø SHT. 1

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TITLE: SCHEMATIC DIAGRAM Q-RGB-GRAPH	PROJECT
DRAWN BY: TSEPT 81 R DANCIK	APPROVED
CHECKED BY	RELEASED
DRAWING NO: 173-004-02	SCALE
SHT 2 OF 5	

J4-32 124 122 123 SDI3
J4-36 131 129 130
J4-31 159 157 158
J4-35 145 143 144 SDI0
J4-30
J4-34
J4-29
J4-33

SDI0 SDI1 SDI2 SDI3
SDO0 SDO1 SDO2 SDO3
SDO0-SDO3 DCLK SH/L SHT.4

HRS RAS CAS BCLE R/C SHT.4

A114 74LS299 A110 74LS299 A71 74LS299 A67 74LS299
A112 74LS374 A112 74LS374 A69 74LS374 A69 74LS374
RD00 RD03 RD04 RD07 RD08 RD11 RD12 RD15

R16 33 R24 33

A78 74S153 A93 74S153 A65 74S153 A108 74S153
RN10 1K +5V
RN6 33 RN5 33

C88 22pF

A101 A100 A99 A98 A97 A96 A95 A94 A86 A85 A84 A83 A82 A81 A80 A79
W0 W3 W4 W7 W8 W11 W12 W15

A115 74LS399 A111 74LS399 A72 74LS399 A68 74LS399
A47

A113 74LS253 A70 74LS253 A70 74LS245
MD0 MD1 MD2 MD3

SHT.4 FGR
SHT.4 SYNRD
SHT.1 XO
SHT.1 XI
SHT.2 MD0-MD3
SHT.4 FDS
SHT.4 DW

A109 74S288 A66 74S288
RN7 1K RN4 1K +5V
WEN0 WEN1 WEN2 WEN3

SHT.1 DISPEN
SHT.1 WEN0-WEN3
SHT.4 PRMEM
SHT.4 WRS
SHT.4 SYNWR

A118 A117

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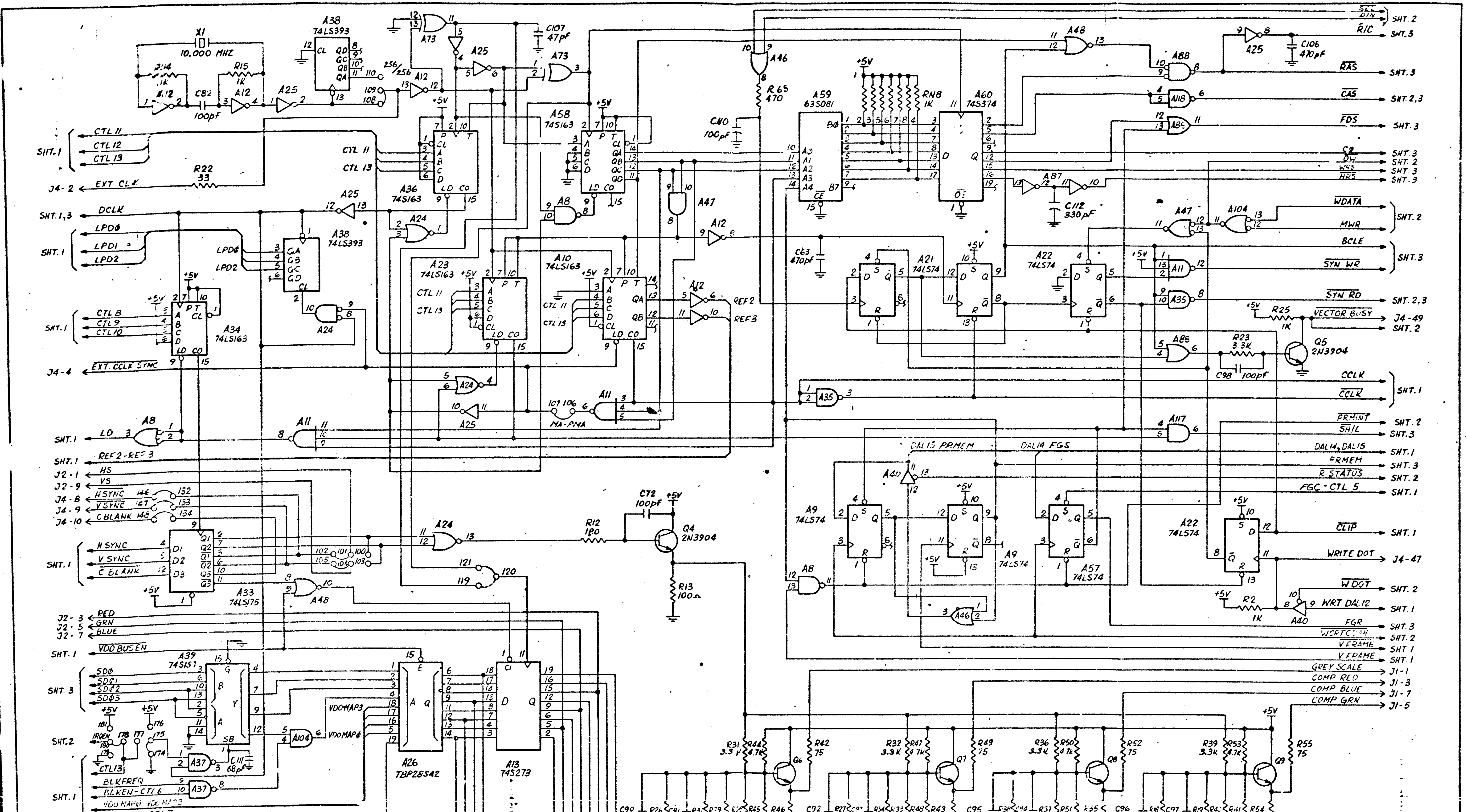
TITLE: SCHEMATIC DIAGRAM Q-RGB-GRAPH
PROJECT:
DRAWN BY: R DANCIK DATE: SEPT 87 APPROVED:
CHECKED BY: RELEASED:
DRAWING NO: 173-004-01
SCALE:
SHT 5 OF 5



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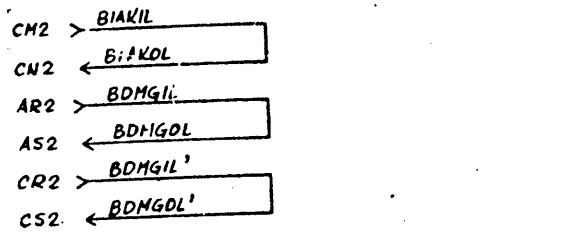
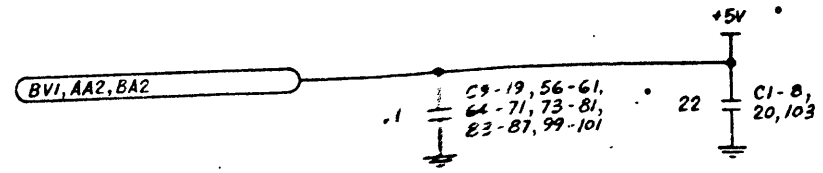
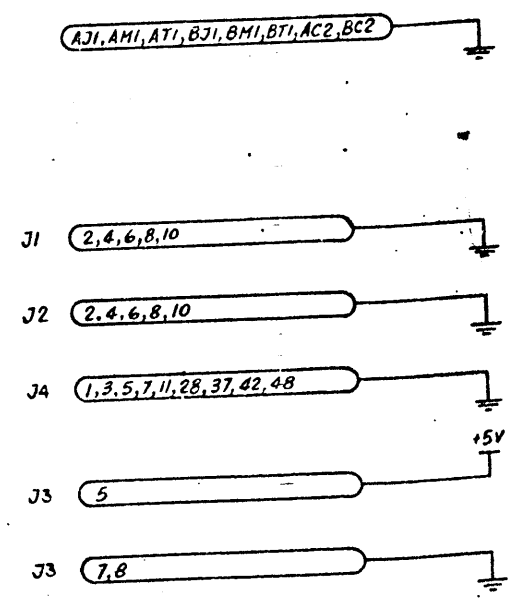
TITLE	SCHEMATIC DIAGRAM Q-RGB-GRAPH
DRAWN BY	R. DANCIK, 1 SEPT 81
DRAWING NO.	173-D04 02
SHEET	4 of 5







PARTS #	IC REFERENCE	+12V	-12V	+5V	-5V	GND
74S00	A35			14		7
74LS00	A8,14,37			14		7
74S02	A24			14		7
74LS02	A4,48			14		7
74S04	A25			14		7
74LS04	A3,12,87			14		7
74LS08	A15,47,104,117			14		7
74LS10	A1,11			14		7
74LS21	A6,50			14		7
7425	A28			14		7
74S32	A88			14		7
74LS32	A32,46,52			14		7
74LS74	A9,21,22,56, 57,61			14		7
74LS86	A73			14		7
74LS125	A40,74			16		8
74S153	A65,78,93,108			16		8
74LS153	A43,54			16		8
74LS155	A5,19,20			16		8
74S157	A39			16		8
74S158	A105			16		8
74S163	A36.58			16		8
74LS163	A10,23,34			16		8
74LS174	A16			16		8
74LS175	A30,31,33,44,116			16		8
74LS193	A63,64,76,77,91,92			16		8
74LS244	A41,53,102,106,107			20		10
74LS253	A70,113			16		8
74S258	A89			16		8
74LS273	A29,55,60			20		10
74S288	A66,109			16		8
74LS299	A67,71,110,114			20		10
74LS374	A69,69,112			20		10
74LS393	A38.45			14		7
74LS399	A68,72,111,115			16		8
74LS157	A103			16		8
74273	A13			20		10
DM8131	A17,18			16		8
DS8835	A51,62,75,90			16		8
DS8837	A27			16		8
9602	A7			16		8
SY6545	A42			20		1
TBP18S42	A26			20		10
4164-150	A79-86, 94-101	8		9	1	16
74S74	A2			14		7
63S081	A59			16		8

PARTS #	IC REFERENCE	SPARES
74LS00	A37	1
74LS04	A87	2
74LS04	A12	1
74LS32	A46	1
74LS241	A53	2

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   - ALL RESISTANCES ARE IN OHMS, ¼W, ±10%.
   - ALL CAPACITORS ARE MICROFARAD.

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TITLE: SCHEMATIC DIAGRAM Q-RGB-GRAPH		PROJECT
DRAWN BY: R DANCIK	APPROVED: [illegible]	DRAWING NO: 173-D04-05
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