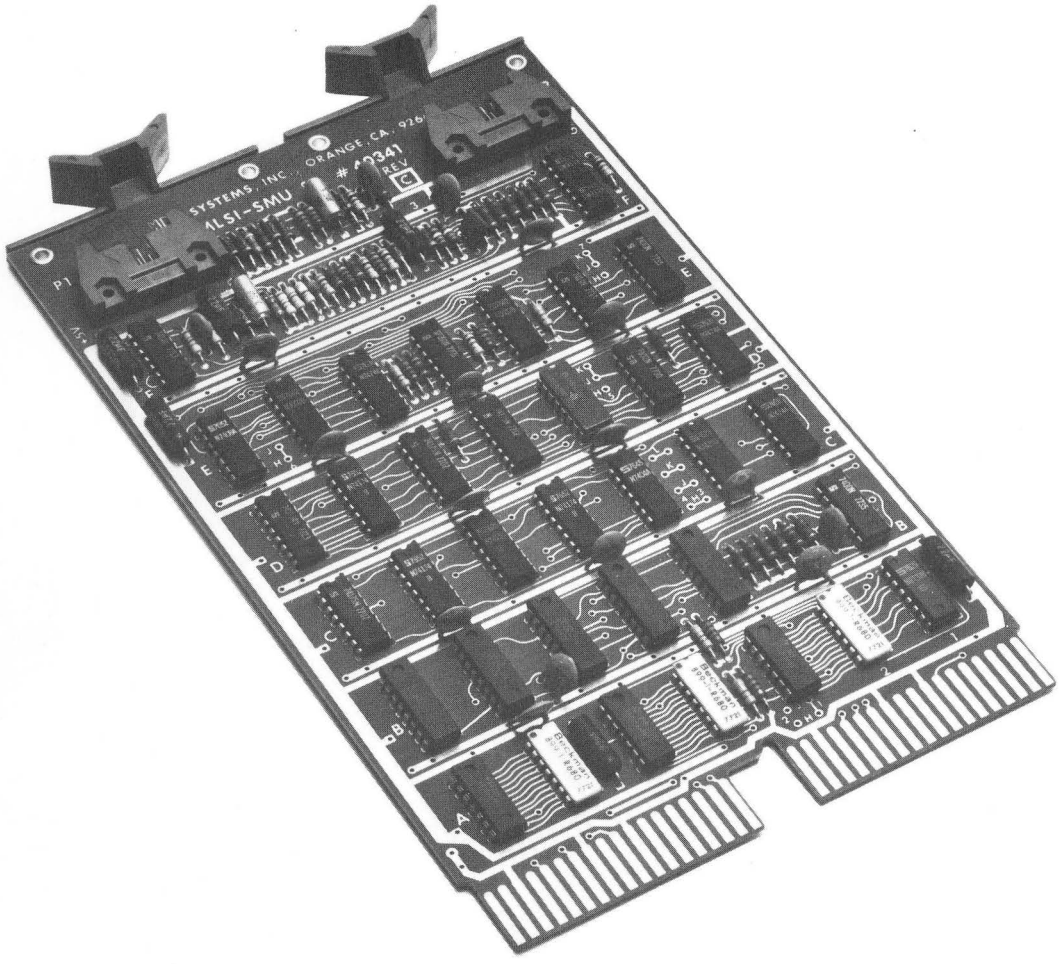
MDB

MLSI-SMU

SYSTEM MONITORING UNIT

INSTRUCTION MANUAL



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MDB SYSTEMS INC.
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Printed in USA

500/6-79

MLSI-SMU SYSTEM MONITORING UNIT

INTRODUCTION

The MDB MLSI-SMU Monitoring Unit provides a variety of monitoring and control functions as follows:

a. AC and DC power monitoring and power-up and power-down sequencing, duplicating monitoring functions of the DEC H780 Power Supply;

b. Pseudo switch register (for PDP-11 compatibility), with addressing logic;

c. Line time clock or KW11L real-time clock compatibility, with addressing and interrupt logic. Jumpers on the module permit the user to select an internal 60-Hz line time clock, an externally generated clock, or the KW11L-type interrupt system;

d. A switch panel equivalent to that of PDP-11/03; and

e. Bus termination.

The MLSI-SMU is a dual module which mounts in one-half quad slot in a MDB BPA84 backplane/cardguide assembly. Because the SMU module contains bus terminations, it should be located at the lowest-priority slot available.

The switch panel associated with the SMU contains:

- RUN and DC ON indicators. The RUN indicator/pushbutton is also used to initiate an initialization cycle.
- A toggle switch to enable or disable the Line Time Clock.
- A toggle switch to control processor HALT/ENABLE.
- An AC ON/OFF switch to control AC line power to the enclosure and to the external power supply.

PHYSICAL DESCRIPTION

The MLSI-SMU Monitoring Unit is a dual module which occupies two slots in the backplane/cardguide assembly. The module is connected to a low AC voltage (to sample the power line frequency), and to the switch panel mounted in the MLSI-BA11 enclosure, by cables terminated with 10-pin Berg connectors. The switch panel is equivalent to the PDP-11/03 switch panel, and is accessible through an opening in the front panel furnished.

Controls are an AC power switch, a HALT/ENABLE switch, and a LTC ON/OFF switch. A RUN indicator shows when the processor is in the RUN status. A DC ON indicator is on whenever AC and DC supply voltage levels are acceptable.

The module requires DC power from the backplane as follows:

- +5V DC at 1.0 ampere.
- +12V DC at 0.1 ampere.

INSTALLATION

General

The MLSI-SMU is installed in the backplane, with cables connected to the switch panel (P2), and to the power supply (P1).

Cable connector P1 is the input to AC voltage detector circuits and must be tied to a low-voltage tap (14 V AC peak) on the power supply (usually the transformer secondary for the +5V DC supply). Table 1 lists P1 pin connections.

Cable connector P2 connects the SMU module to the switch panel printed-circuit board. Table 2 lists pin connections.

Table 1 P1 Connections

Signal	Pin
AC1	1
AC1	5
AC1	6
AC1	10
AC2	3
AC2	8
GND	2
GND	4
GND	7
GND	9

Table 2 P2 Connections

Signal	Pin
LTC ON	1
ENABLE	2
HALT	3
EXT CLOCK	4
+5V DC	5
$\overline{\text{DCINH}}$	6
DC ON	7
LTC OFF	8
RUNNING	9
GND	10

Figure 1 shows the switch panel functions and markings. Figure 2 shows the installed module and switch panel, and the MLSI-BA11-100 enclosure and front panel.

Connecting Jumpers

Certain jumpers must be connected to configure the module for the specific application. Proceed as follows:

a. Determine the Line Time Clock (LTC) mode. The module is normally furnished configured for a 60-Hz LTC using the Event Line Interrupt (BEVNTL) for interrupts (jumper 6 installed).

To use an external clock instead of the internal 60-Hz clock, remove jumper 5 from between locations J and K, and connect between J and H.

For operation with 50-Hz power, value of resistor R39 (Dwg 40341, sheet 2) must be 24K ohms. If operating with 50-Hz power, check module to see that resistor is 24K ohms. (Resistor value is 20K ohms for 60-Hz operation.)

To use the KW11L option (PDP-11 compatible), move jumper 7 from between locations J and K, and connect between J and H. This permits using interrupt logic in response to the KW11L address 777546.

NOTE

When the KW11L option is used, the LTC switch on the switch panel does not control LTC interrupts and must remain in the "off" position.

b. Connect pin AH-1 of the backplane slot occupied by the SMU module to the wire-wrap post marked SRUNL (located on the backplane near the terminal strip). The RUN indicator on the switch panel requires this signal connection in order to indicate processor "run" status.

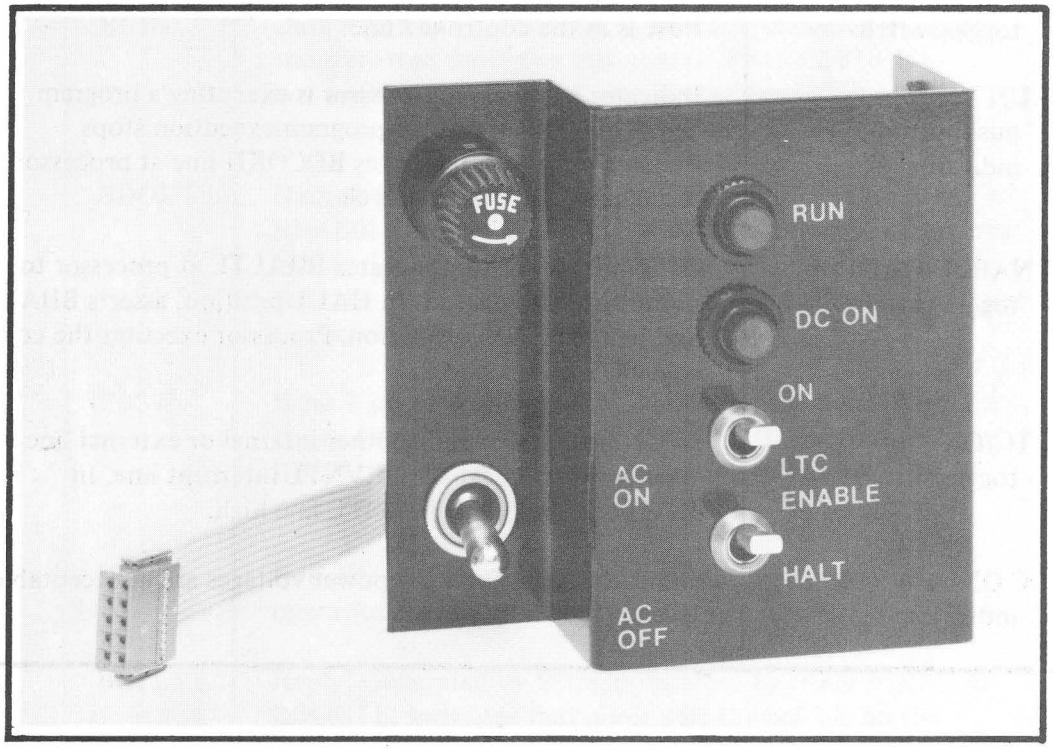


Figure 1 MLSI-SMU Switch Panel

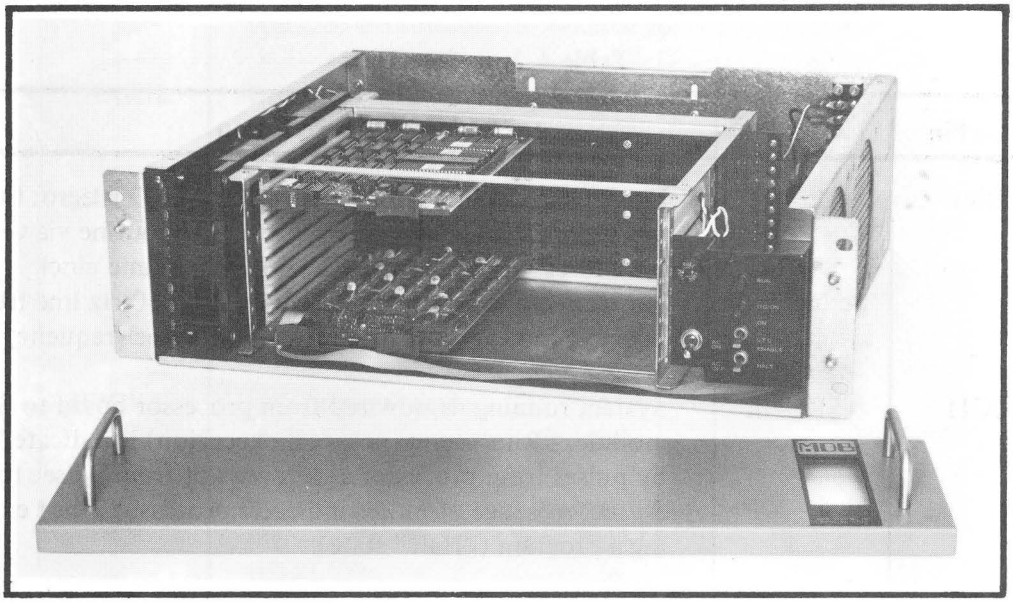


Figure 2 MLSI-SMU Installation

OPERATION

Table 3 lists the controls and indicators on the SMU switch panel and explains the function of each.

Table 3 Controls and Indicators

Control/Indicator	Function
AC ON/AC OFF toggle switch	Controls AC power to DC power supply and to fans. Fuse is in the controlled line.
RUN pushbutton/ indicator	Indicator is *on* when processor is executing a program. Turns off 200 msec after program execution stops. Pressing pushbutton negates BDCOKH line at processor and causes initialization cycle.
ENABLE/HALT toggle switch	In ENABLE position, negates BHALTL at processor to permit program to run. In HALT position, asserts BHALTL and halts program execution. Processor executes the console ODT microcode.
LTC/ON toggle switch	In ON position, permits either internal or external line time clock to assert the BEVNTL interrupt line. In LTC position, holds BEVNTL line high.
DC ON indicator	Indicator is *on* when DC power voltages are at acceptable levels.

INTERFACE TERMS

Table 4 lists and defines signals at the backplane connector of the module.

Table 4 Interface Terms

Bus Pin	Term	Description
BR1	BEVNTL	**External event interrupt request.** If PS bit 7 is zero, the processor responds by entering a service routine via vector address 100_8. Using BEVNTL, a line time clock interrupt occurs every 16-2/3 msec for a 60-Hz line frequency, and every 20 msec for a 50-Hz line frequency.
AH1	SRUNL	**System running.** Hardwired from processor board to SMU module. "Run" state (program execution) is indicated by pulses from processor at intervals of from 3 μsec to 5 μsec. Absence of pulses indicates processor is not executing a program ("Halt" state).

Table 4 Interface Terms (cont'd)

Bus Pin	Term	Description
AL2	BIRQL	**Interrupt request.** Asserted by processor-enabled interrupt enable and interrupt request logic. Indicates to processor that data may be input or output. Program status word bit 7 must be "0" in order for processor to acknowledge an interrupt request.
AH2	BDINL	**Data input.** When BSYNCL is asserted, indicates an input transfer from the active bus master. When BSYNCL is *not* asserted, implies that an interrupt operation is in process.
AE2	BDOUTL	**Data output.** Implies that valid data is available on lines BDAL0L through BDAL15L and, with reference to the bus master device, that an output transfer is in process. The slave device responding to BDOUTL must assert BRPLYL to complete the data transfer.
AP2	BBS7L	**Bank 7 select.** Indicates that address on the bus is from the upper 4k bank (28k-32k). With BSYNCL asserted, BBS7L remains active until addressing of bus cycle is completed.
AT2	BINITL	**Initialize.** Generated by processor during a power-up operation. Clears all devices on the I/O bus.
AF2	BRPLYL	**Reply.** Generated by SMU in response to either BDINL or BDOUTL. Indicates that input data is available on the BDAL bus, or that output data has been accepted from the bus.
BA1	BDCOKH	**DC power OK.** Generated by SMU when DC supply voltages are suitable for reliable system operation.
AM2	BIAKIL	**Interrupt acknowledge.** Asserted by processor in response to BIRQL.
AN2	BIAKOL	**Interrupt acknowledge out.** Normally asserted to device having next-lower priority on interrupt chain, and appears at BIAKIL input to that device. If SMU stores an interrupt request, BIAKOL is negated at the next device.
BB1	BPOKL	**AC power OK.** Asserted by SMU when primary AC power is at an acceptable level.
AJ2	BSYNCL	**Synchronize.** Asserted by bus master device when it has placed an address on lines BDAL0L through BDAL15L.

Table 4 Interface Terms (cont'd)

Bus Pin	Term	Description
AP1	BHALTL	**Processor halt.** When asserted by SMU: – Processor halts normal program execution; – Processor executes ODT microde and invokes the console device. – External interrupts are not recognized, although memory refresh interrupts and DMA request/grant sequences are enabled.
	BDALnL	**Data/address.** One of the 16 data/address bus lines used to transfer all address and data information.
AU2	BDAL0L	Bit 0.
AV2	BDAL1L	Bit 1.
BE2	BDAL2L	Bit 2.
BF2	BDAL3L	Bit 3.
BH2	BDAL4L	Bit 4.
BJ2	BDAL5L	Bit 5.
BK2	BDAL6L	Bit 6.
BL2	BDAL7L	Bit 7.
BM2	BDAL8L	Bit 8.
BN2	BDAL9L	Bit 9.
BP2	BDAL10L	Bit 10.
BR2	BDAL11L	Bit 11.
BS2	BDAL12L	Bit 12.
BT2	BDAL13L	Bit 13.
BU2	BDAL14L	Bit 14.
BV2	BDAL15L	Bit 15.

THEORY OF OPERATION

The following paragraphs describe the theory of operation of the MLSI-SMU in terms of the logic diagram (Dwg. No. 40341) contained in this manual. Figure 3 shows the general functional organization of circuits in the unit.

AC VOLTAGE DETECTOR (BPOKH)

After AC power is turned on, the AC voltage at the secondary winding of the +5V supply (AC1, AC2) is rectified and the resulting half cycles appear at the voltage comparator 1F/B. This circuit compares the sample AC voltage with a 2.5V reference at 1F/B-3.

The first, and subsequent, half-cycles of the normal line voltage sample cause the output of 1F/B to trigger a retriggerable one-shot having a period of 16.7 milliseconds (the line fre-

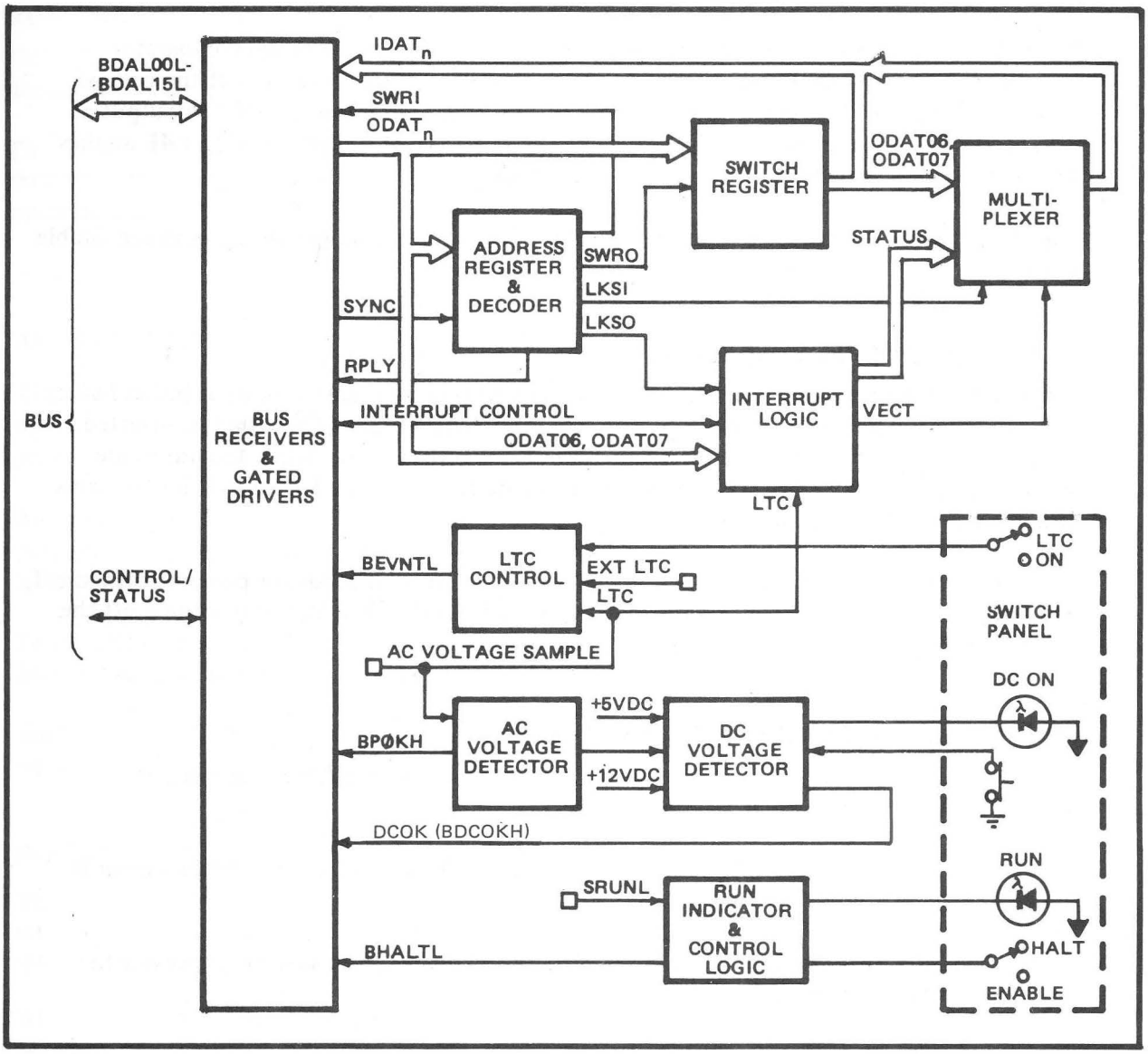


Figure 3 MLSI-SMU Monitoring Unit, Functional Block Diagram

quency period). The resulting signal ACH goes high and triggers an 80-millisecond retriggerable one-shot. After the 80-millisecond period, the output of this one-shot clocks the POK flip-flop, asserting BPOKH to indicate normal AC voltage levels. The 80-millisecond delay permits power supplies to stabilize following application of AC power.

The term ACH also is ANDed (by a "DC normal" level) to a 4-millisecond one-shot which holds the DCOK flip-flop set, causing the DC ON line to go high and turn on the DC ON lamp.

If the AC voltage sample drops below 2.5 volts at 1F/B-2, the ACH one-shot is not retriggered. ACH falls, clearing the POK flip-flop and causing BPOKH to go low indicating a loss or reduction of AC voltage. ACH also permits the 4-millisecond one-shot to return to its stable state and the DCOK flip-flop is cleared, causing the DC ON line to go low and turn off the DC ON Lamp.

DC VOLTAGE DETECTOR (BDCOKH)

The +12V DC and +5V DC supply bus voltages are monitored by a voltage comparator (1F/A) which compares the bus voltage with a 2.5-volt reference at 1F/A-3. If the voltage on the +5V bus falls below 4.6V, or if the +12V bus level falls below 11.3V, the output of 1F/A goes high and clears the DCOK flip-flop 5E. As DCOK goes low, the driver 4E applies a high level at P2-7, turning off the DC ON indicator.

The DC ON indicator is turned on again as soon as DC supply voltages are again at acceptable levels.

RUN INDICATOR (logic diagram, sheet 2)

Whenever the processor is in the Run mode and executing programs, a train of pulses having a period of from 3 to 5 microseconds appears on the SRUNL line. These pulses, inverted, trigger a retriggerable one-shot having a period of 200 milliseconds. While the pulses are present, and for 200 milliseconds after the pulses are removed, the RUNNING line remains low to turn on the RUN indicator.

Two-hundred milliseconds after the processor is put in the Halt mode, or power is turned off, the one-shot reverts to its stable state, making the RUNNING line high and turning off the RUN lamp.

HALT/ENABLE CONTROL (logic diagram, sheet 2)

The cross-coupled inverters 2E-8 and 2E-6 remove effects of switch bounce when the HALT/ENABLE switch is operated.

When the switch is set to the ENABLE position, BHALTL is negated and the processor is free to resume normal program operation.

When the switch is in the HALT position, BHALTL is asserted, causing the processor to execute the console ODT microde.

NOTE

In the Halt mode, the processor will continue to execute memory refresh and respond to DMA requests.

BUS DRIVERS AND RECEIVERS (logic diagram, sheets 2 and 3)

Bus driver and receiver devices (type 8641) condition data and addresses moving in both directions on the bus. Data or address bits put on the bus by the processor (BDALnL) are received and inverted to ODATn lines for transfer to the read/write register and address decoding logic.

Bits to be transferred from the read/write register to the processor (IDATn) are inverted by gated drivers which put the bits on the bus.

Drivers must be enabled by $\overline{\text{SWR1}}$. Interrupt status and vector address bits IDAT07 and IDAT06 are also separately gated by the term $\overline{\text{INP}}$.

Another 8641 device (3B) accepts internally generated control signals and puts them on the bus.

Receivers in an 8837 device (1A) receive the bus control signals from the processor.

READ/WRITE REGISTER (logic diagram, sheet 2)

The 16-bit read/write register (devices 4C, 6C, and 7C) responds when the address 777570 is decoded, and either a DATOUT (load) command, or a DATIN (read) command, is received.

The register is loaded from receiver outputs when the address is decoded and DATOUT is received, asserting $\overline{\text{SWRO}}$. The contents of the register are put on the bus (through drivers) when the address is decoded and DATIN is received, asserting $\overline{\text{SWRI}}$.

ADDRESS DECODER (logic diagram, sheet 3)

The address register (devices 4D, 5D, and 6D) stores the address that selects the unit for operation. The register is loaded from receiver outputs by the SYNC (BSYNCL) signal generated by the bus master device.

Bits stored from lines ODAT06 through ODAT12 (and BS7) appear at a NAND circiut, the output of which is used as an input term at the decoder (3D). The address is decoded to assert $\overline{\text{SWRO}}$ when DATOUT is present, or to assert $\overline{\text{SWRI}}$ when DATIN is present.

Terms $\overline{\text{LKSO}}$ and $\overline{\text{LKSI}}$ (used in interrupt logic) are similarly asserted in response to the decoded address and an accompanying DATOUT or DATIN command.

The receipt of a decoded address, and a DATIN or DATOUT command, is acknowledged by asserting RPLY. RPLY is transferred through a driver circuit to the bus (BRPLYL).

INTERRUPT LOGIC (logic diagram, sheet 2)

The unit is furnished with jumpers connected to supply the signal BEVNTL as a periodic interrupt. BEVNTL is derived from a Line Time Clock which is either the AC power line frequency, or the frequency of an external clock.

When the line time clock interrupt line BEVNTL is disabled and jumper 7 is connected between pins H and J, interrupt logic will respond to the internal line time clock only under program control.

Interrupt logic is enabled to respond only when the program has asserted BDAL06L (ODAT06) along with the address decoded to the $\overline{\text{LKSO}}$ line, $\overline{\text{LKSO}}$ loads the bit into the LKIEN flip-flop, enabling the IRQST (interrupt request) flip-flop.

Similarly, $\overline{\text{LKSO}}$ presents the ODAT07 to the LKRDY flip-flop to *inhibit* an interrupt cycle.

If LKIEN is true, each line time clock sets the IRQST flip-flop, whose output is put on the BIRQL line to the bus master and, if the interrupt mask has been set, sets the LKRDY flip-flop.

The bus master responds with a data input command (DATIN) which stores the request, and then asserts BIAKIL to gate the stored request to the $\overline{\text{VECT}}$ line.

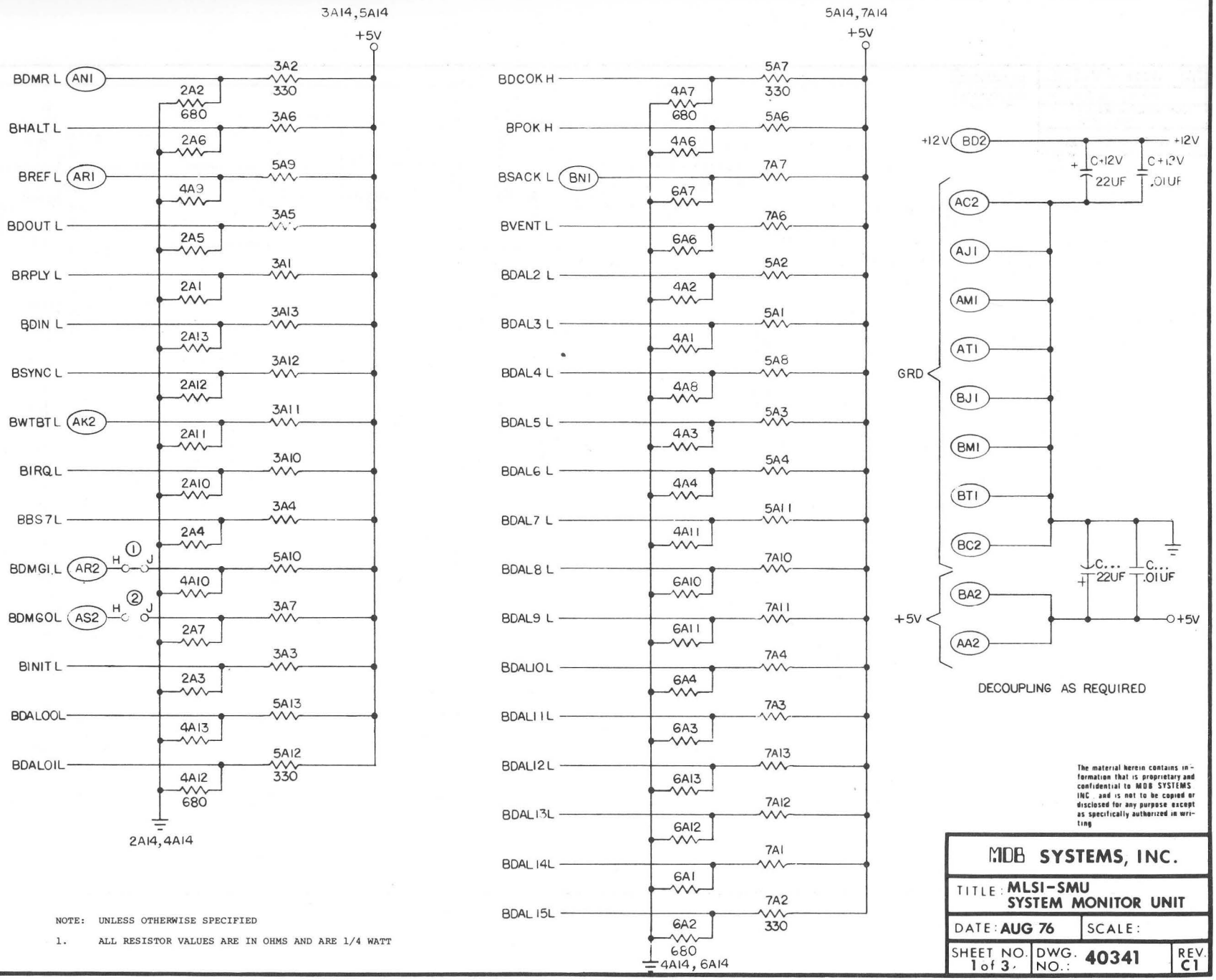
$\overline{\text{VECT}}$ controls the multiplexer (5C) so that LKIEN and LKRDY status bits are put on the IDAT06 and IDAT07 lines, respectively, for transfer to the bus. In the normal state of the multiplexer, an $\overline{\text{LKSI}}$ command puts the contents of the switch register on the bus.

When no interrupt is stored in the MLSI-SMU, BIAKIL asserted on the device priority line causes the unit to assert BIAKOL and grant priority to the device having the next-lower priority. BIAKOL is negated when the unit stores an interrupt, reserving priority to the MLSI-SMU.

MAINTENANCE AND REPAIR

In the event of apparent malfunction, refer to the assembly and logic diagrams contained in this instruction manual. Check to be sure connectors are seated and that switch panel controls are properly set.

Repair the module using appropriate skills, techniques, and materials. If you wish MDB Systems to repair the module, pack the module carefully, along with your best evaluation of trouble symptoms, and ship it, prepaid, to MDB Systems.


3A14,5A14
+5V
BDMR L
ANI
3A2
330
2A2
680
BHALT L
3A6
2A6
BREF L
ARI
5A9
4A9
BDOUT L
3A5
2A5
BRPLY L
3A1
2A1
BDIN L
3A13
2A13
BSYNC L
3A12
2A12
BWTBT L
AK2
3A11
2A11
BIRQ L
3A10
2A10
BBS7L
3A4
2A4
BDMGI L
AR2
5A10
4A10
BDMGO L
AS2
3A7
2A7
BINIT L
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2A3
BDALOOL
5A13
4A13
BDALOIL
5A12
330
4A12
680
2A14,4A14
5A14,7A14
+5V
BDCOK H
5A7
330
4A7
680
BPOK H
5A6
4A6
BSACK L
BNI
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6A7
BVENT L
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6A6
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4A2
BDAL3 L
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4A1
BDAL4 L
5A8
4A8
BDAL5 L
5A3
4A3
BDAL6 L
5A4
4A4
BDAL7 L
5A11
4A11
BDAL8 L
7A10
6A10
BDAL9 L
7A11
6A11
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6A4
BDALI1L
7A3
6A3
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7A12
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7A1
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BDALI5L
7A2
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6A2
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+12V
BD2
+12V
C+12V
22UF
C+12V
.01UF
AC2
AJ1
AM1
AT1
GRD
BJ1
BM1
BT1
BC2
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+5V
AA2
DECOUPLING AS REQUIRED
NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4 WATT
The material herein contains information that is proprietary and confidential to MDB SYSTEMS INC. and is not to be copied or disclosed for any purpose except as specifically authorized in writing
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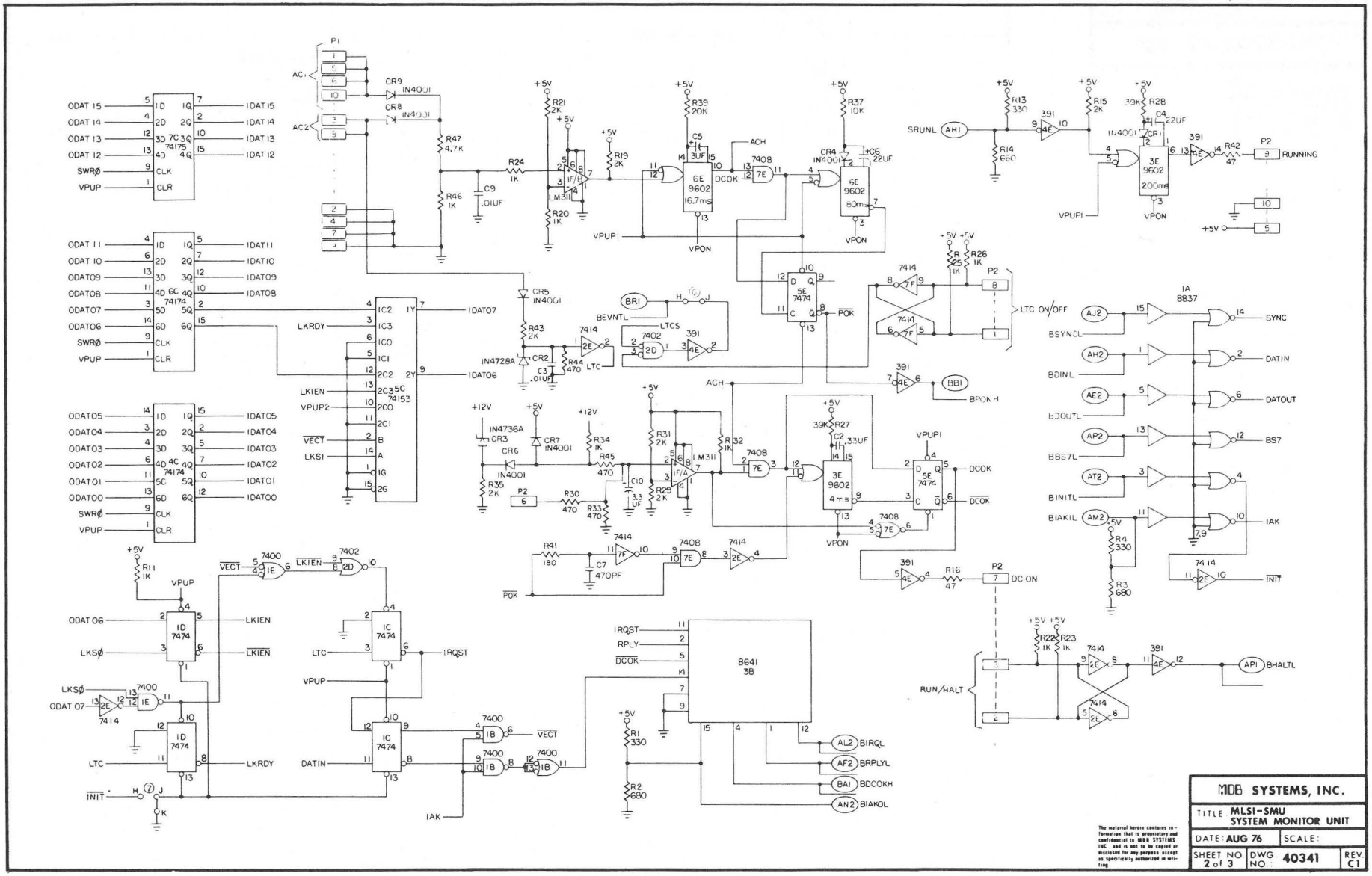
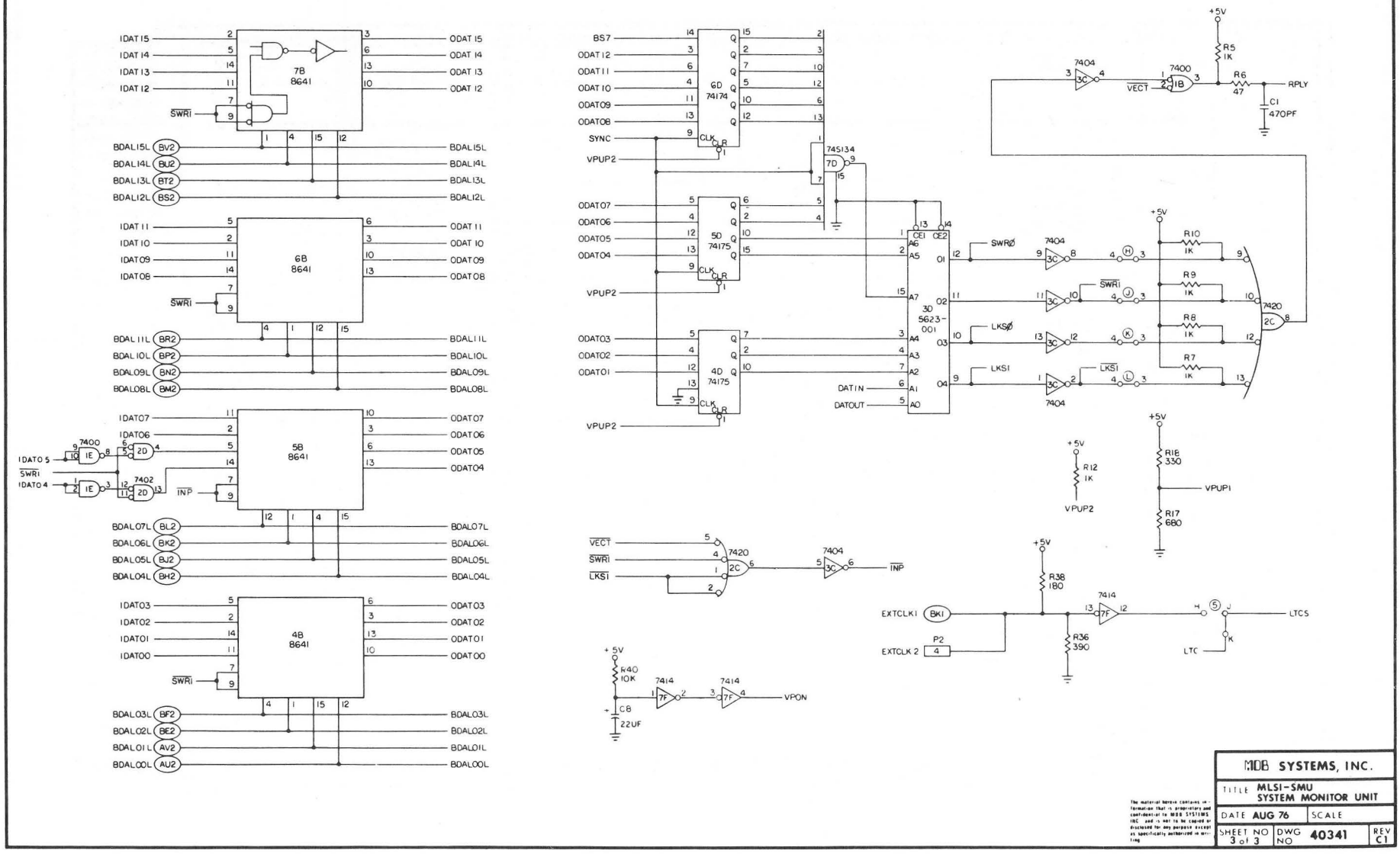
TITLE: MLSI-SMU
SYSTEM MONITOR UNIT
DATE: AUG 76
SCALE:
SHEET NO. 1 of 3.
DWG. NO.: 40341
REV. C1

Schematic change:
Resistor R21 changes from a 1K ohm 1/4 watt to a 2K ohm 1/4 watt resistor. 5/79





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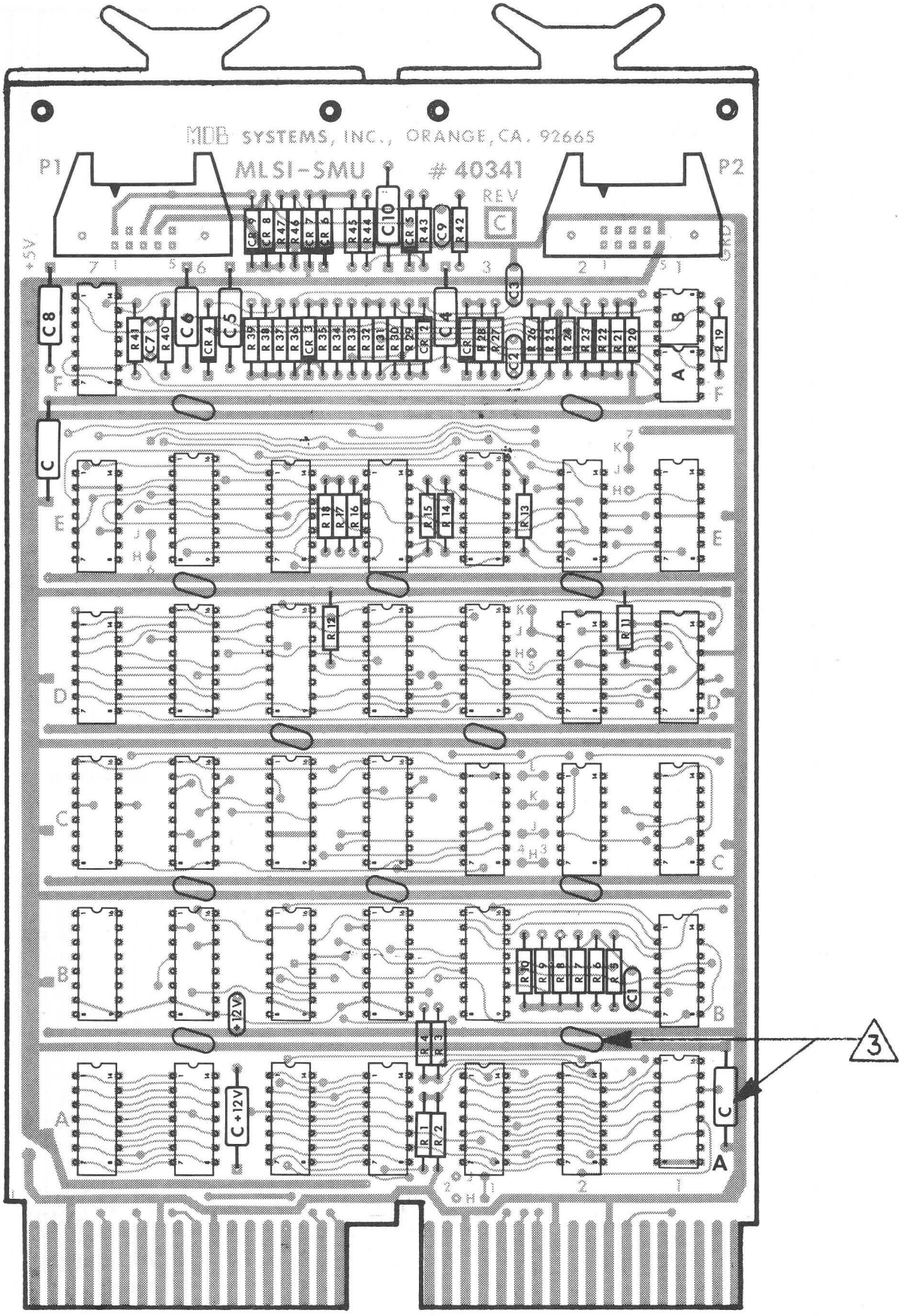
SHEET NO 3 of 3 | DWG NO 40341 | REV C1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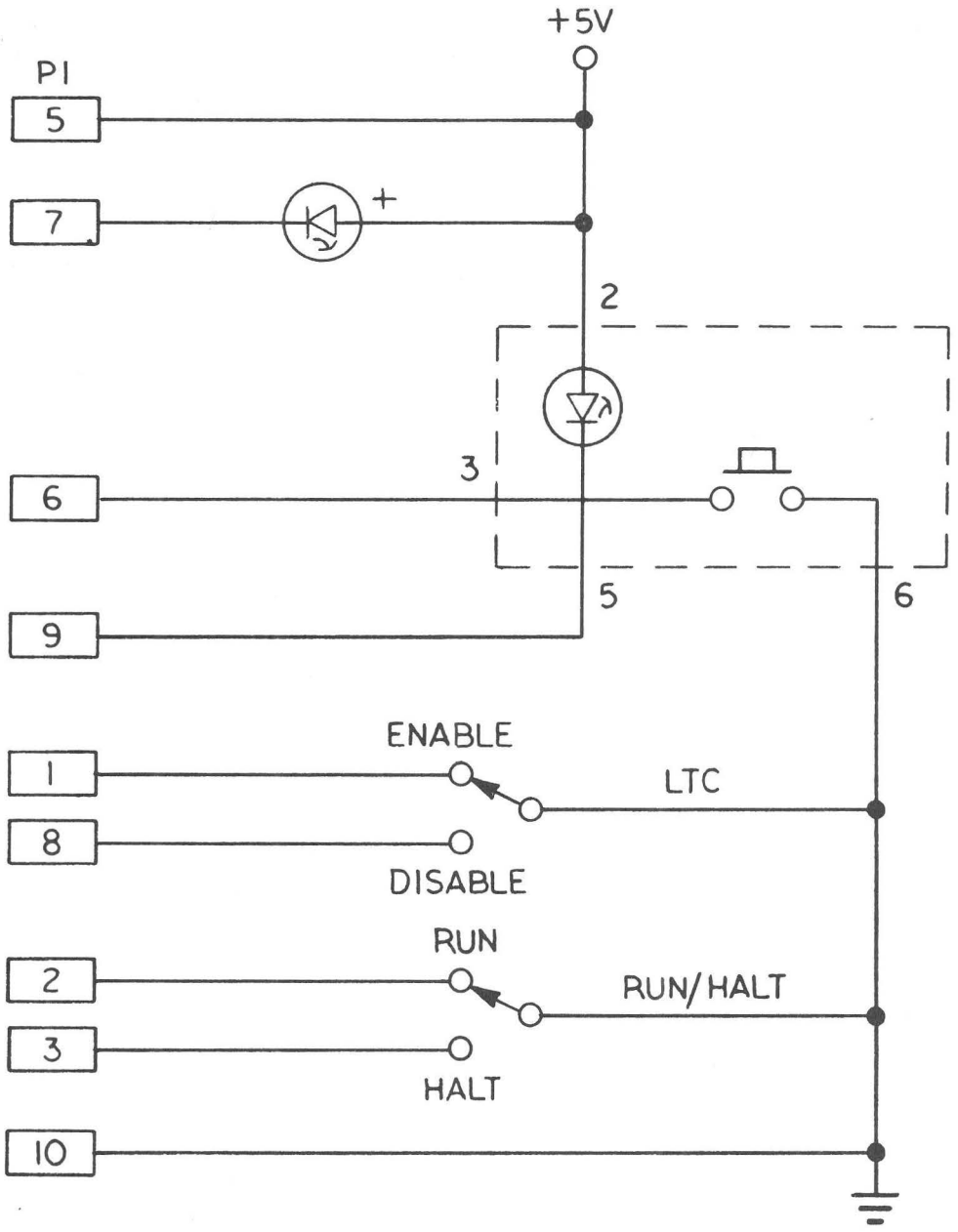
MLSI-SMU
40341
REV
C
P1
P2
+5V
+12V
3



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DATE: **MARCH 77**	SCALE:	
SHEET NO **1 of 1**	DWG NO.: **40342**	REV **A**

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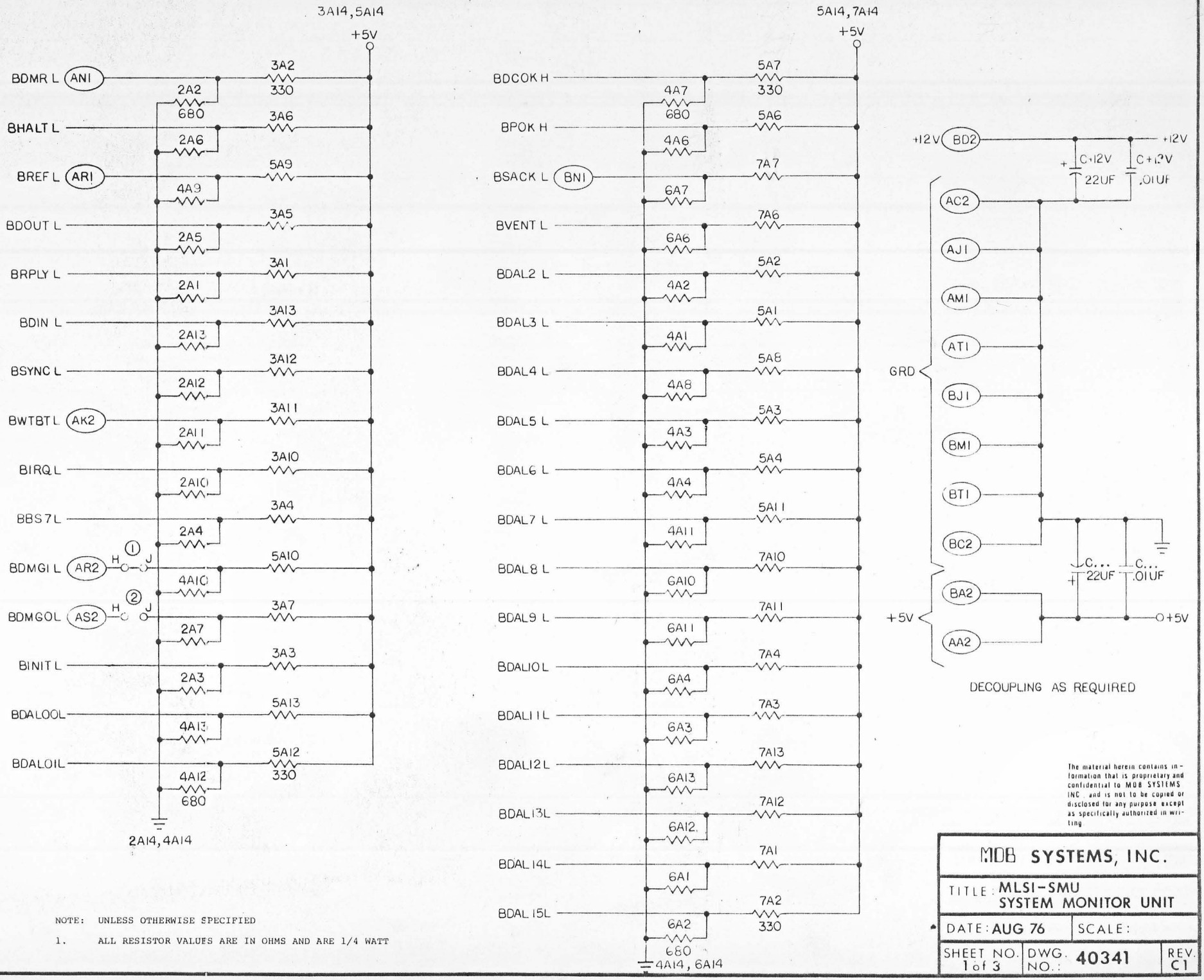

NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4 WATT

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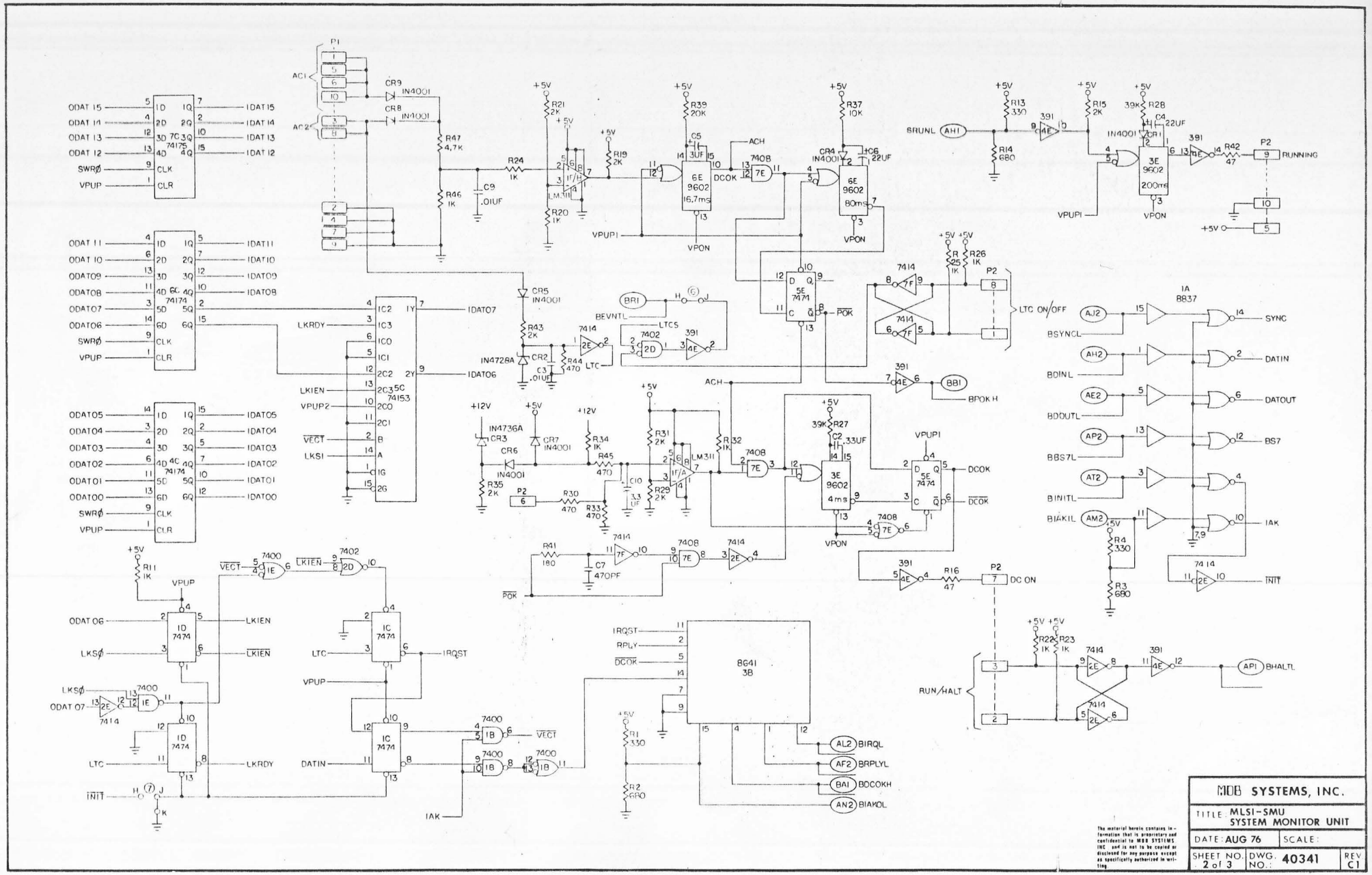
SHEET NO. 1 of 3 | DWG. NO.: 40341 | REV. C1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TITLE: MLSI-SMU SYSTEM MONITOR UNIT
DATE: AUG 76
SCALE:
SHEET NO. 2 of 3
DWG. NO.: 40341
REV C1
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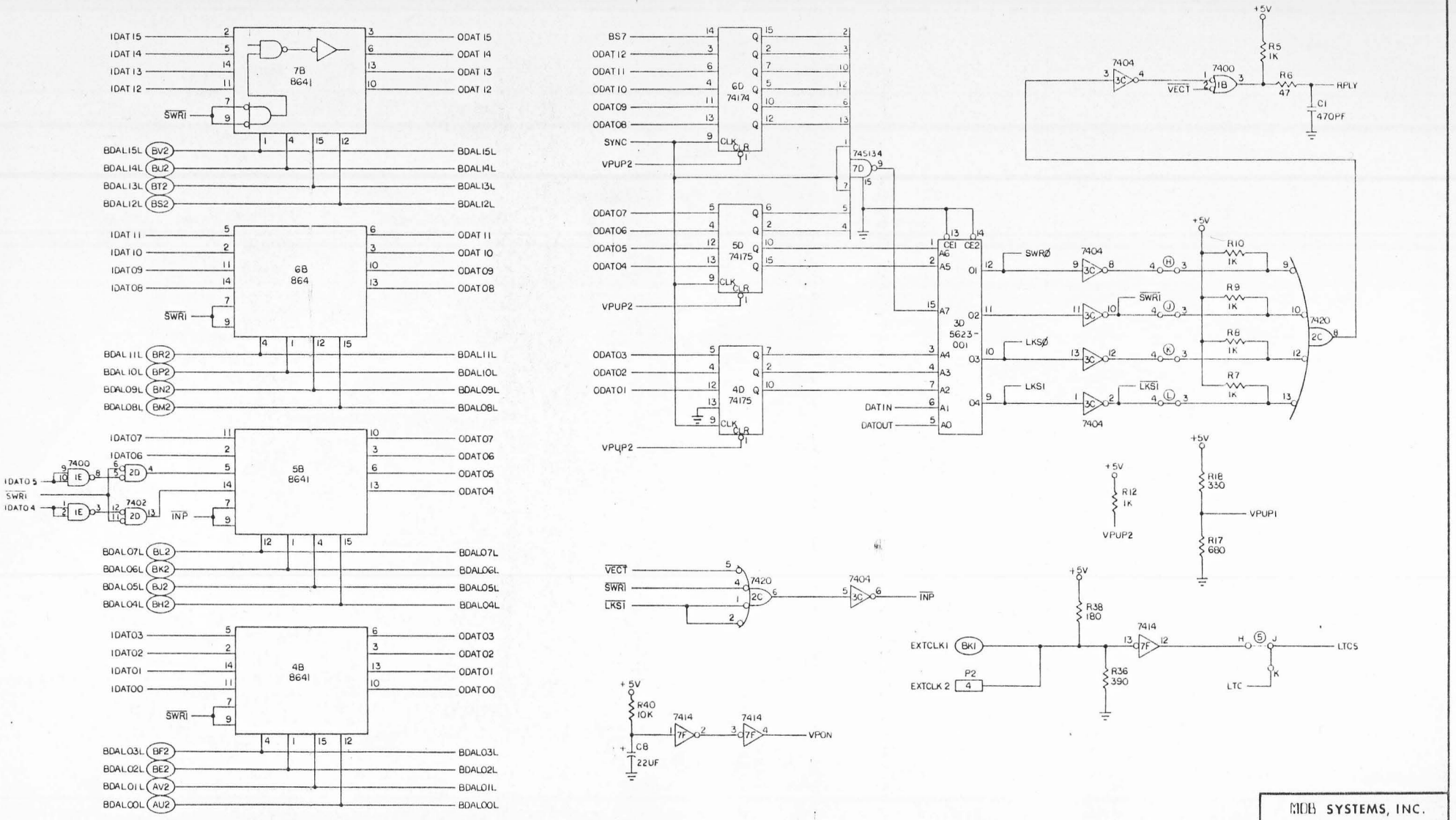

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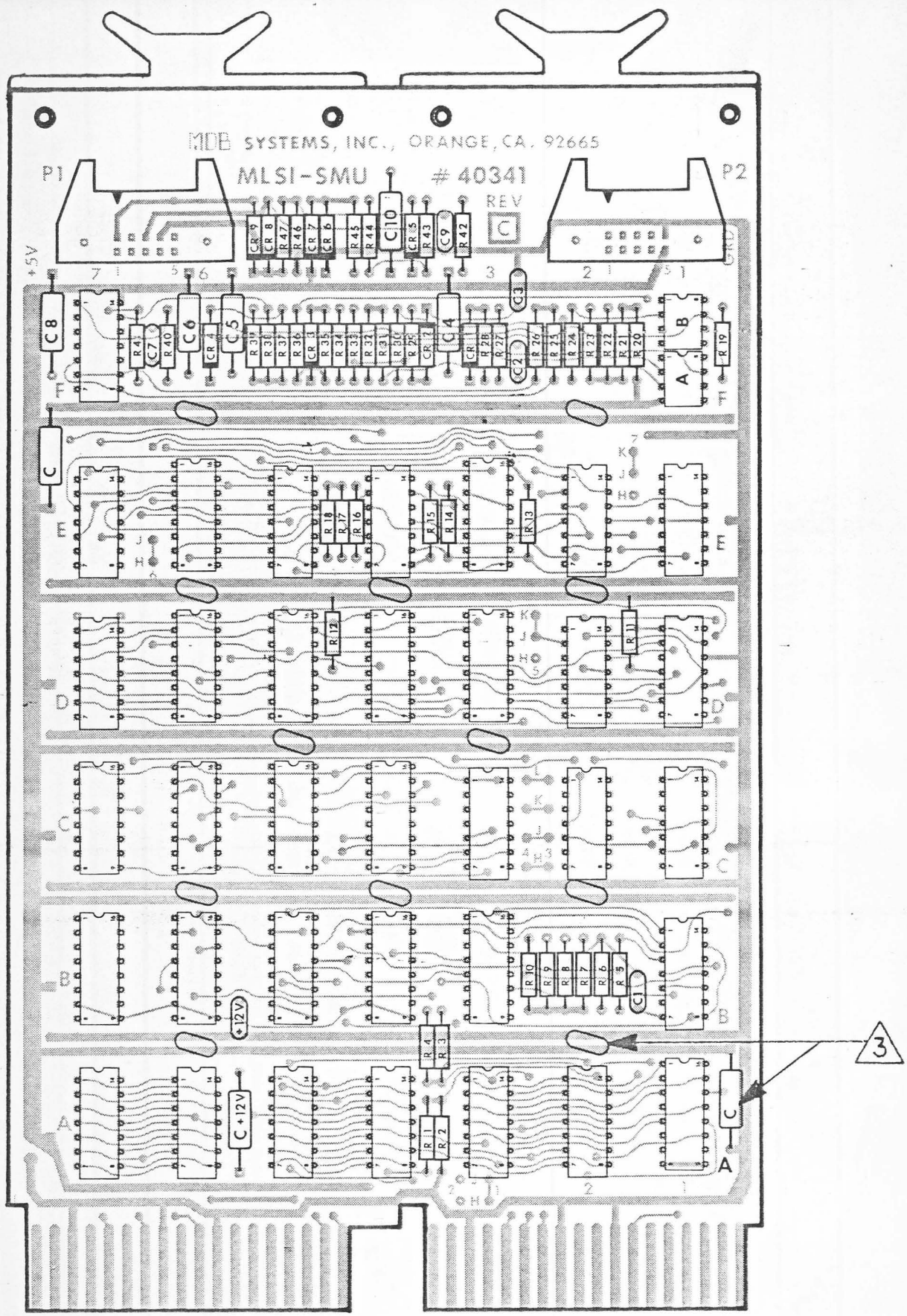
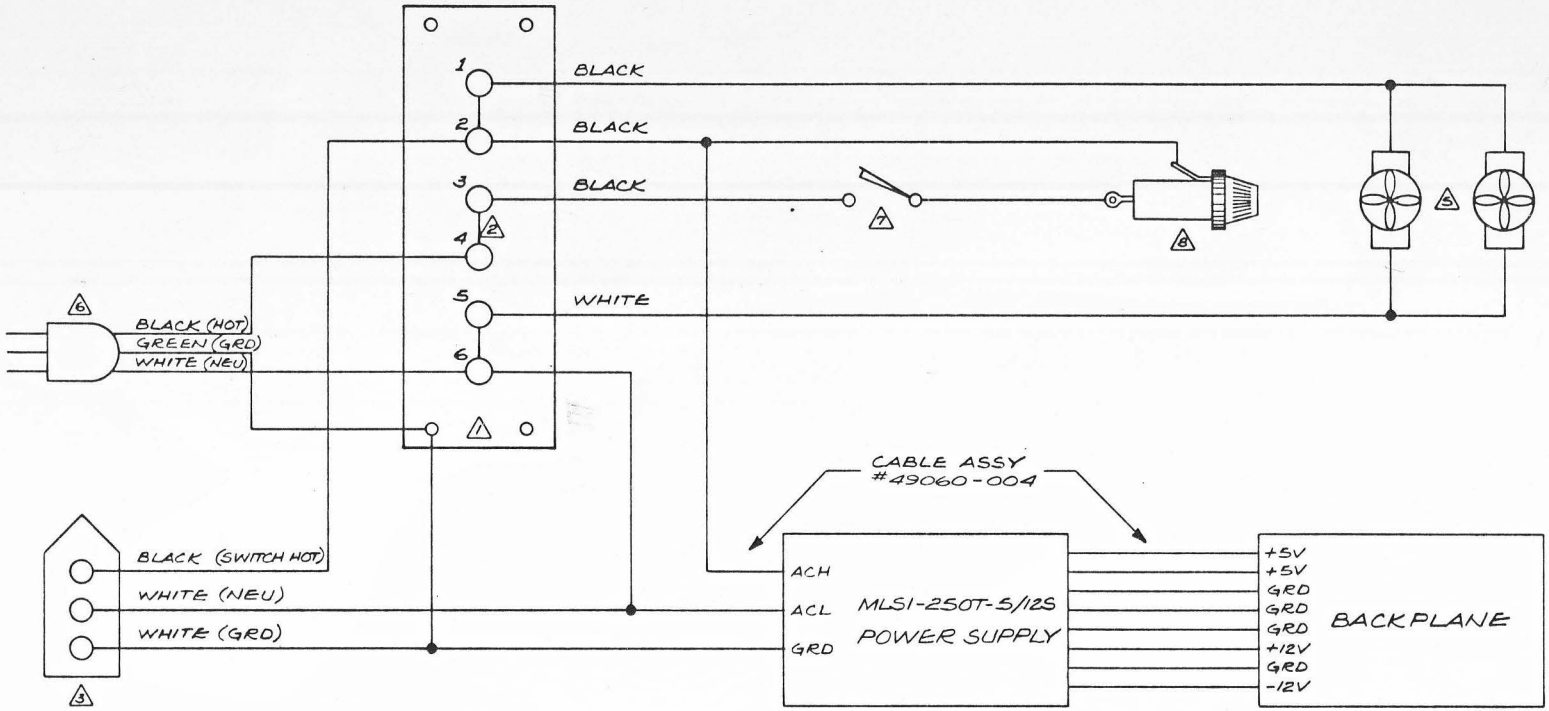

MDB SYSTEMS, INC., ORANGE, CA. 92665
MLSI-SMU
40341
REV
C
P1
P2
+5V
+12V
C +12V
3

COMP. SIDE



PARTS LIST

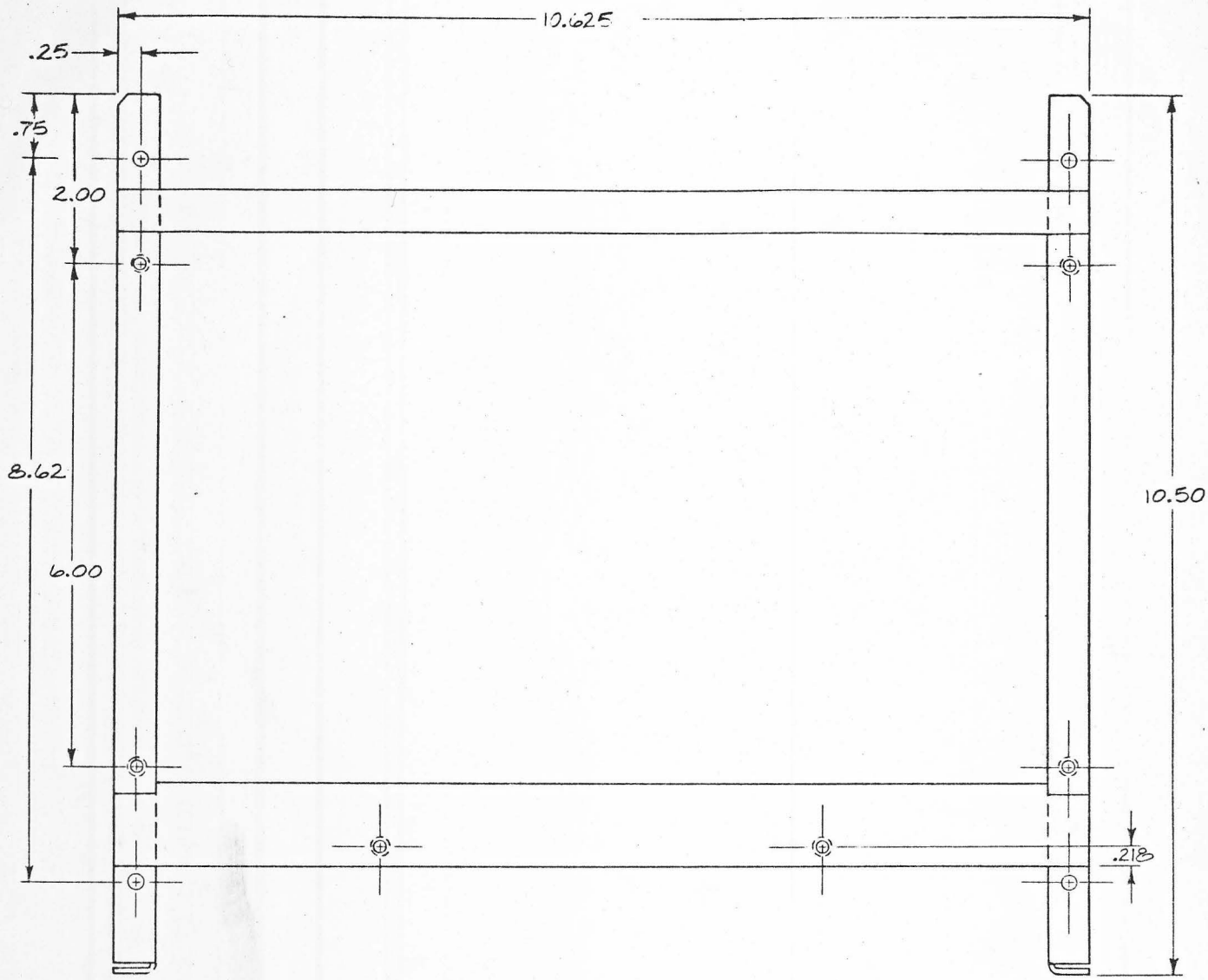
ITEM NO.	DESCRIPTION	PART NO.	QTY
1	TERMINAL BLOCK	601-6	1
2	TERM. BK. JUMPER	601-J	3
3	CONNECTOR, FEMALE	59-03S2000	1
4	PINS, FEMALE	109-1018S	3
5	FAN	MU2A1	2
6	AC LINE CORD, 9'	17419B	1
7	AC SWITCH	7501-K13	1
8	FUSE HOLDER	342012 HKP	1

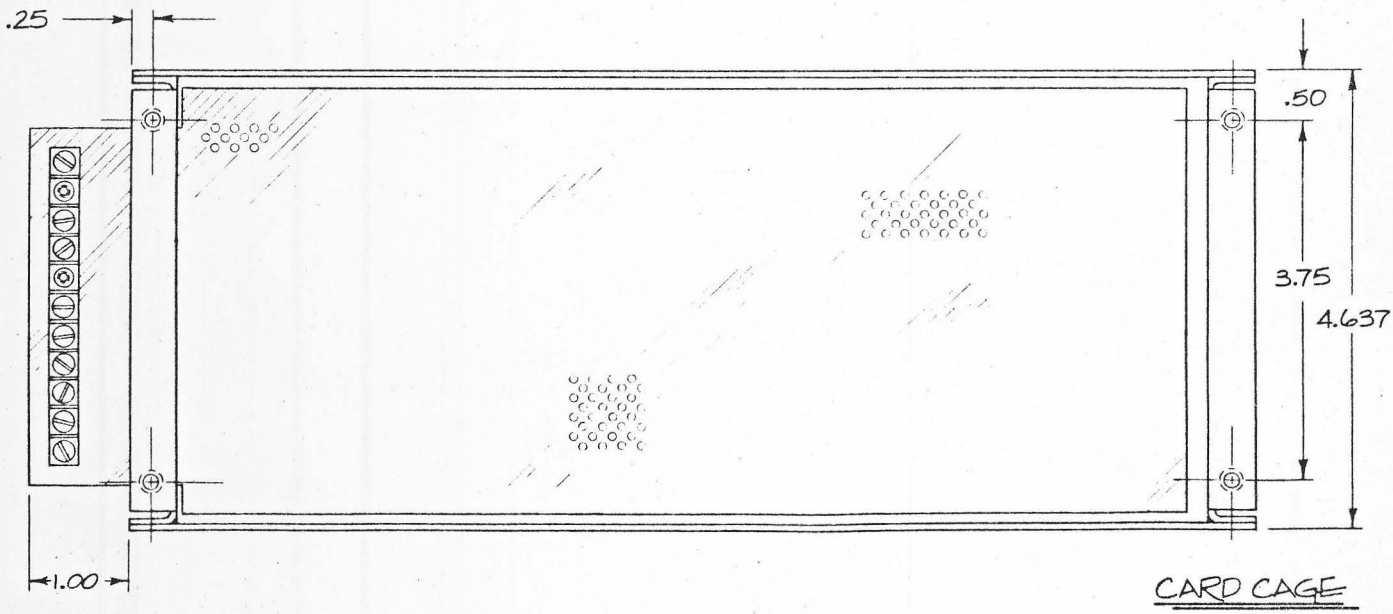
MDB SYSTEMS, INC.

TITLE: BA11-100 CHASSIS WIRING

DATE: APR 79 | SCALE:

SHEET NO. 1 of 1 | DWG. NO.: 50317 | REV.





CARD CAGE

INSTALLATION DWG

MDB SYSTEMS, INC. #40328