MIL-STD-806B
26 February 1962

Superseding
MIL-STD-806A (USAF)
23 May 1960

MILITARY STANDARD

GRAPHIC SYMBOLS FOR LOGIC DIAGRAMS

DEPARTMENT OF DEFENSE

WASHINGTON 25, D.C.

Graphic Symbols for Logic Diagrams

MIL-STD-806B 26 February 1962

1. This standard has been approved by the Department of Defense and is mandatory for use by the Departments of the Army, the Navy, and the Air Force, effective 26 February 1962.

2. Recommended corrections, additions, or deletions shall be addressed to the Standardization Division, Defense Supply Agency, Washington 25, D.C.

CONTENTS

CONTENTS (Continued)

APPENDICES

1. INTRODUCTION AND GENERAL REQUIREMENTS

1.1 PURPOSE. This standard establishes graphic symbols specifically designed for use in the preparation of logic diagrams for systems of two-state devices.

1.2 SCOPE. This standard prescribes the graphic symbols for logic diagrams in which connections between symbols are shown with lines. Definitions of logic functions, the graphic representations of the functions and examples of their application are given. Illustrations shown are not necessarily full size. Examples of circuit/symbol correspondence are illustrated in Appendix A.

1.3 ABBREVIATIONS. Abbreviations used on drawings shall be in accordance with Military Standard MIL-STD-12. Letter combinations within graphic symbols are not abbreviations (see Appendix D).

2. APPLICABLE STANDARDS

2.1 GENERAL. The issues of the following documents in effect on the date of invitation for bids form a part of this standard to the extent specified herein.

STANDARDS

Military MIL-STD-12	Abbreviations for Use on Drawings and in Technical-Type Publications
MIL-STD-15-1	Graphical Symbols for Electrical and Electronic Diagrams
MIL-STD-16	Electrical and Electronic Reference Designations

3. PRESENTATION TECHNIQUES

3.1 SYMBOL ORIENTATION. The orientation of a symbol on a diagram does not alter the meaning of the symbol.

3.2 SYMBOL LINE THICKNESS. The weight of a line does not affect the meaning of a symbol. In specific cases, a heavier line may be used for emphasis.

3.3 SYMBOL SIZE. A symbol may be drawn to any proportional size that suits a drawing, depending on the reduction or enlargement anticipated. Relative sizes of the symbols shall be in accordance with the template drawing shown in 7.

3.4 IDENTIFICATION. Identification information to specify unique location of logic function on the drawing, within the equipment and its circuit diagram identification is accomplished through the use of "tagging" lines within the symbol. The following tagging lines shall be included on detailed logic diagrams:

3.4.1 The first tagging line shall uniquely identify each logic function symbol on the drawing to establish an identification for use in engineering, communication, and technical manual reference.

3.4.2 The second tagging line shall identify the logic hardware.

3.4.3 The third tagging line shall provide the means for locating the logic function within the equipment.

3.4.4 Details such as stylized waveforms and duration of delays shall be included when required for clarity.

3.4.5 Additional notations shall be placed about the periphery of symbols to identify input and output pin numbers and test points. Line conditions, signal routing, etc, shall also be included for clarity.

3.5 SIGNAL FLOW DIRECTION. Logic diagrams indicate direction of signal flow by symbol orientation. For increased clarity, arrows superimposed on lines are desirable. However, arrowheads shall not be placed immediately adjacent to any graphic symbol input or output. Signal lines leaving the logic diagram shall be terminated with a directive arrow.

3.6 STYLIZED WAVEFORMS. Stylized waveforms (6.6.1) may be placed adjacent to signal lines (where required) to indicate the nature and timing of the signals. Waveform symbols shall be used to represent a voltage amplitude, a single pulse, or a pulse train. Voltage amplitudes shall be indicated on the stylized waveforms. The time of occurrence of a pulse or the beginning and ending times of a pulse train shall be indicated.

3.7 POLARITY NOTATIONS. Mnemonic polarity notations are permissible in place of stylized waveforms to indicate active line conditions.

4. DEFINITIONS

4.1 LOGIC SYMBOL. A logic symbol is the graphic representation of the aggregate of all the parts implementing a logic function.

4.2 LOGIC FUNCTION. A combinational, storage, delay, or sequential function expressing a relationship between variable signal input(s) to a system or device and the resultant output(s).

4.3 BASIC LOGIC DIAGRAM. A logic diagram that depicts logic functions with no reference to physical implementations. It consists primarily of logic symbols and is used to depict all logic relationships as simply and understandably as possible. Non-logic functions are not normally shown.

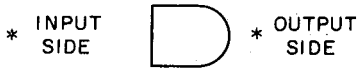
4.4 DETAILED LOGIC DIAGRAM. A diagram that depicts all logic functions and also shows nonlogic functions, socket locations, pin numbers, test points, and other physical elements necessary to describe the physical and electrical aspects of the logic. The detailed logic diagram is used primarily to facilitate the rapid diagnosis and localization of equipment malfunctions. It also is used to verify the physical consistency of the logic and to prepare fabrication instructions. The symbols are connected by lines that represent signal paths.

4.5 TABLE OF COMBINATIONS. For purposes of this standard, tables of combinations describe the active input/output conditions of the basic logic functions (i.e. HIGH (H) more positive and LOW (L) relatively less positive).

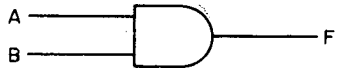
5. LOGIC SYMBOLS

In the following list of logic symbols, explanations accompany the graphic representations.

5.1 AND. The symbol shown below represents the AND function.



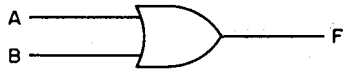
5.1.1 The AND output is high if and only if all the inputs are high.



Input		Output
A	B	F
L	L	L
L	H	L
H	L	L
H	H	H

5.2 OR. The symbol shown below represents the INCLUSIVE OR function.

5.2.1 The OR output is high (H) if and only if any one or more of the inputs are high (H).



Input		Output
A	B	F
L	L	L
L	H	H
H	L	H
H	H	H

5.3 STATE INDICATOR (Active). The presence of the small circle symbol at the input(s) or output(s) of a function indicates:

(a) Input Condition. The electrical condition at the input terminal(s) which control the active state of the respective function.

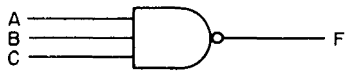
(b) Output Condition. The electrical condition existing at the output terminal(s) of an activated function.

5.3.1 A small circle(s) at the input(s) to any element (logical or nonlogical) indicates that the relatively low (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively high (H) input signal activates the function.

* Not part of symbol

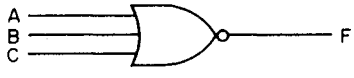
5.3.2 A small circle at the symbol output indicates that the output terminal of the activated function is relatively low (L). This small circle shall never be drawn by itself on a diagram.

5.4 The symbol shown below represents one version of the AND function. The output is low if and only if all the inputs are high.



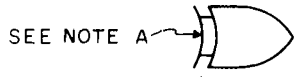
Input			Output
A	B	C	F
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

5.5 The symbol shown below represents one version of the INCLUSIVE OR function. The output is low if any one or more inputs are high.



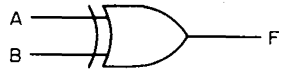
Input			Output
A	B	C	F
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

5.6 EXCLUSIVE OR. The symbol shown below represents the EXCLUSIVE OR function.



NOTE A: Arc displacement determined by location of paragraph 7 template center input line guide hole.

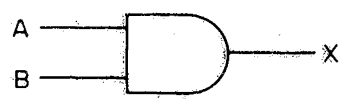
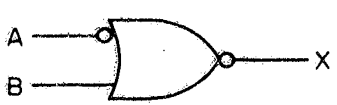
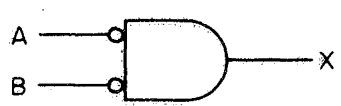
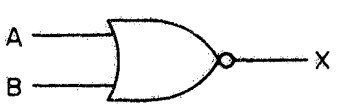
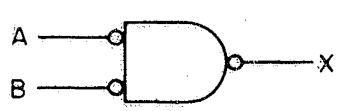
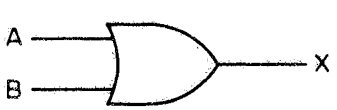
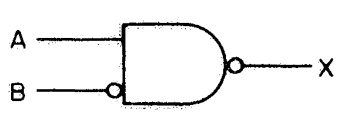
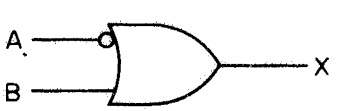
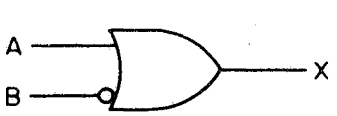
5.6.1 The EXCLUSIVE OR output is high if and only if any one input is high and all other inputs are low.



Input		
A	B	F = A (H) and B (L) or B (H) and A (L)
L	L	L
L	H	H
H	L	H
H	H	L

EXCLUSIVE OR may also be represented as shown in Appendix A, figure 11.

5.7 The following table of combinations illustrates the applications and functions of two variables and equivalents:

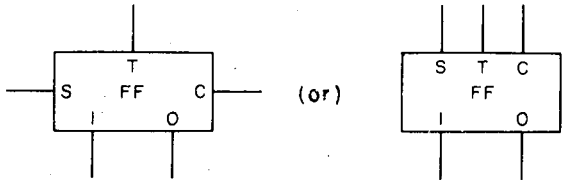
AND	OR	TABLE OF COMBINATIONS A	B	X
		H H L L	H L H L	H L L L
		H H L L	H L H L	L L H L
		H H L L	H L H L	L H L L
		H H L L	H L H L	L L L H
		H H L L	H L H L	H H H L
		H H L L	H L H L	H L H H
		H H L L	H L H L	H H L H
		H H L L	H L H L	L H H H

5.7.1 Additional information regarding the equivalences of logic functions and operations will be found in the Appendix.

5.8 FLIP-FLOP. The flip-flop is a device which stores a single bit of information. It has three possible inputs, set (S), clear (reset) (C), and toggle (trigger) (T), and two possible outputs, 1 and 0. When not used, the trigger input may be omitted.

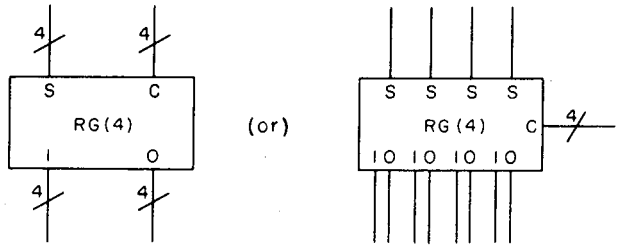
5.8.1 Polarity. The two outputs are normally of opposite polarity. A "1" is stored in the flip-flop when the "1" output level is active and the "0" output level is inactive. A "0" is stored in the flip-flop when the above condition is reversed.

5.8.2 States. The flip-flop assumes the "1" state when an active signal appears at the "S" input regardless of the original state. It assumes the "0" state when an active signal appears at the "C" input regardless of the original state. It reverses its state when an active signal appears at the "T" input. There are several possible variations to normal flip-flop operations, depending upon the response of the device when active inputs are applied to more than one input simultaneously.



"S" input shall be in proximity to the "1" output. "C" input shall be in proximity to the "0" output. The aspect ratio of the symbol shall be 1.75 to 1. (See application examples in Appendix A.)

5.9 BINARY REGISTER. The binary register symbol represents a group of flip-flops used in parallel to constitute a single register (as to store four bits of a character). It is necessary to indicate the number of "bits" or individual flip-flops in the register. Examples below show four "S" inputs grouped on one multiple input line and four each "1" and "0" grouped output lines. In some applications individual input and output lines are shown as in right hand figure.



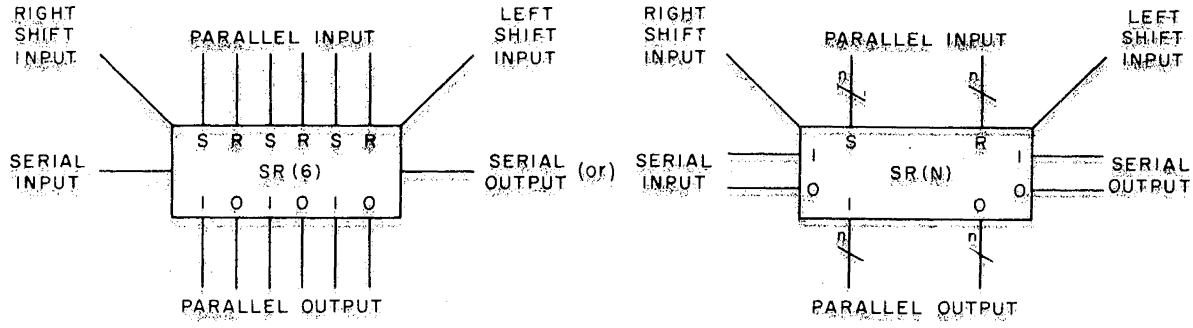
The aspect ratio of the symbol shall be 2.5 to 1 or greater, as required.

5.10 SHIFT REGISTER. The shift-register symbol represents a binary register with provision for displacing or shifting the content of the register one stage at a time to the right or left by means of the "shift" input.

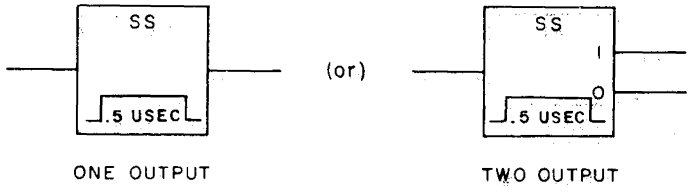
5.10.1 The words "right shift input" shall be placed at a left corner of the symbol to indicate a shift from left to right. If the shift is from right to left, the words "left shift input" shall be placed at a right corner of the symbol.

5.10.2 The aspect ratio of the symbol shall be 2.5:1 or greater, as required.

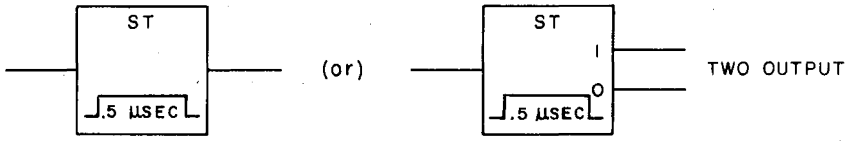
5.10.3 The choice of one of the following symbols depends on the diagram arrangement of the associated symbology.



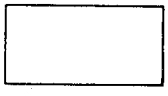
5.11 SINGLE SHOT FUNCTIONS. The symbols shown below are used to represent single-shot (SS) functions. Output signal shape, amplitude, duration, and polarity are determined by the circuit characteristics of the "SS," (not by the input signal) and may be shown inside or outside the symbol. The unactuated state of the "SS" is either zero or one. When actuated, it changes to the opposite state and remains in the opposite state for the duration of the active time of the device. The aspect ratio of the symbol shall be 1:1.



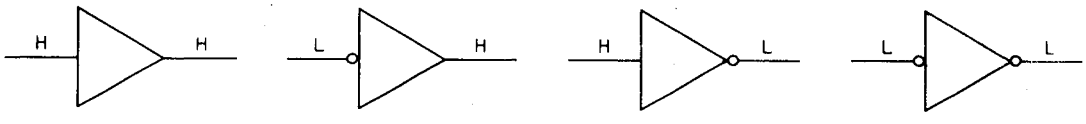
5.12 SCHMITT TRIGGER. The symbols shown below represent the Schmitt Trigger (ST) function. The device is actuated when the input signal crosses a certain "threshold" voltage. Output signal amplitude and polarity are determined by the circuit characteristics of the "ST," (not by the input signal). Stylized waveforms may be shown (inside or outside the symbol), indicating amplitude, polarity, threshold voltage and duration. The unactuated state of "ST" is either zero or one. When actuated, it changes to the opposite state and remains in the opposite state as long as the input exceeds the threshold value. The aspect ratio of the symbol shall be 1:1.



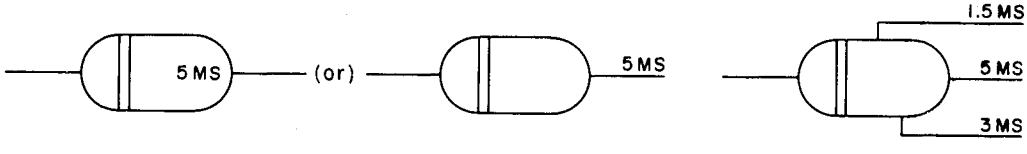
5.13 GENERAL LOGIC SYMBOL. Symbol for functions not elsewhere specified. The symbol shall be adequately labeled to identify the function performed. It is not intended that this symbol be used for functions which can be logically expressed by a single symbol established in this standard. Aspect ratio shall be 2:1 or greater.



5.14 AMPLIFIER. Refer to MIL-STD-15-1, (2.1). This symbol represents a linear or nonlinear current or voltage amplifier. This amplifier may have one or more stages and may or may not produce gain or inversion. Level changers and inverters, pulse amplifiers, emitter followers, cathode followers, relay pullers, lamp drivers, and shift register drivers are examples of devices for which this symbol is applicable.



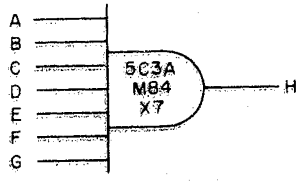
5.15 TIME DELAY SYMBOL. Refer to MIL-STD-15-1, (31). The duration of the delay is included with the symbol. If the delay device is tapped, the delay time with respect to the input shall be included adjacent to the tap output. Twin vertical lines indicates the input side.



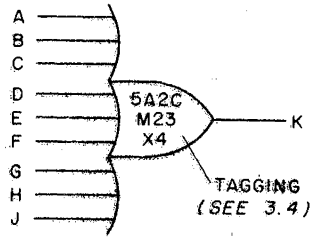
6. PRACTICE

6.1 Multiple inputs to a single function.

AND Function

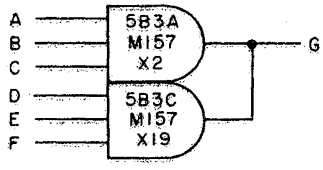


OR Function

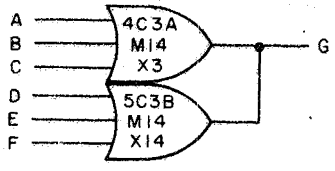


6.2 Multiple inputs to physically separated functions with common outputs.

AND Function



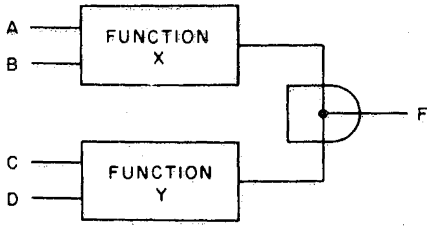
OR Function



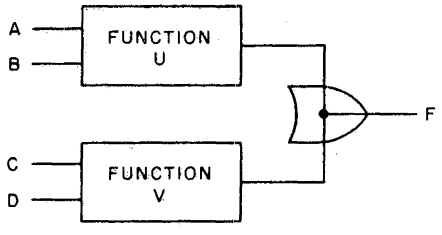
6.3 OUTPUT COMBINATIONS

Use of Separate Circuits. Where functions have the capability of being combined according to the AND (or OR) function, simply by having the outputs connected, that capability shall be shown by enveloping the branched connection with a smaller sized AND or OR symbol.

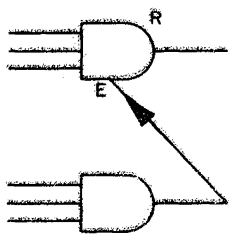
Dot "AND"



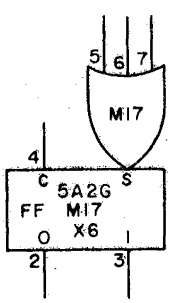
Dot "OR"



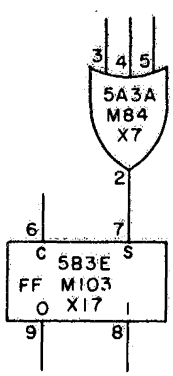
6.4 EXTENDED INPUTS. In the case where a circuit is used to add inputs to another AND or OR circuit, and the connection from this second circuit to the first is made at other than a normal input or output of the first circuit, the connection will be as shown below, and will be labeled E to indicate extension of the input. See also Appendix A, figure 7. The letter R, when shown adjacent to a symbol, indicates that the output resistor is adjacent to or in the vicinity of the hardware's physical location described by the internal tagging of that symbol.



6.5 MULTIPLE FLIP-FLOP INPUTS. Multiple inputs physically integral with flip-flop functions are drawn as shown in Example 1, and so "tagged." Multiple inputs physically separated from the flip-flop functions are drawn as shown in Example 2, and separately tagged. See also Appendix A, figure 12.



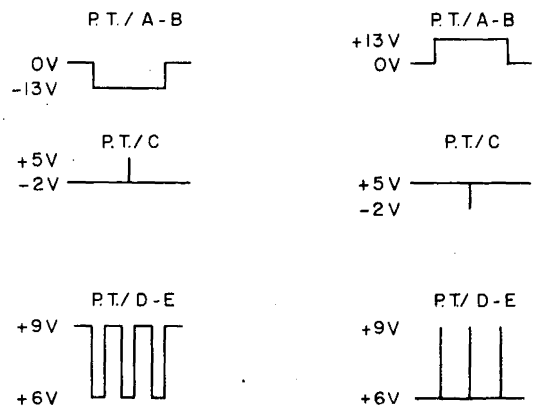
Example 1



Example 2

6.6 STYLIZED WAVEFORMS AND NOTATIONS

6.6.1 STYLIZED WAVEFORMS. Stylized waveforms may be placed adjacent to signal lines to indicate the nature and timing of the signals. Waveform symbols shall be used to represent a level, a single pulse, or a pulse train. Voltage levels shall be indicated, as shown. The time of occurrence of a pulse or the beginning and ending times of a pulse train or of a level may be indicated.



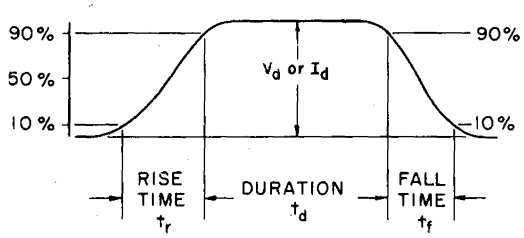
Level starting at pulse time A and ending at pulse time B.

Pulse occurring at pulse time C from the less positive level (-2V) to the more positive level (+5V), in the left-hand figure; and from the more positive level (+5V) to the less positive level (-2V) in the right-hand figure.

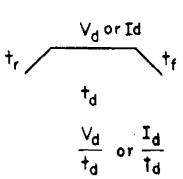
Pulse train with first pulse occurring at pulse time D and last pulse at pulse time E. (In the case of an information bearing pulse train, not all pulses are necessarily shown.)

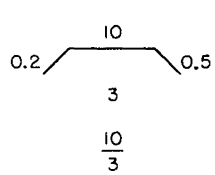
NOTE: Pulse may be represented as a single or double line, as appropriate, to clarify logic.

6.6.2 WAVEFORM NOTATIONS. The following figures illustrate the application of waveform analysis notations to stylized waveforms.



PULSE CHARACTERISTIC NOTATION:

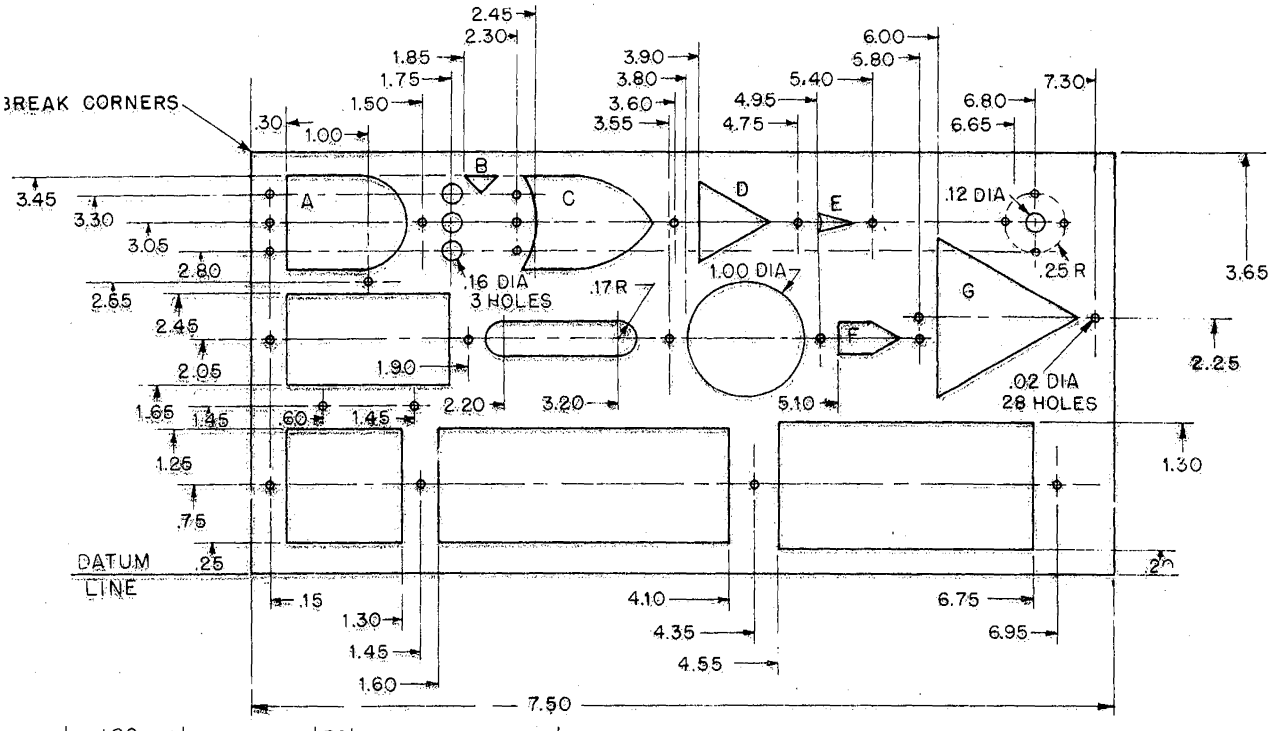


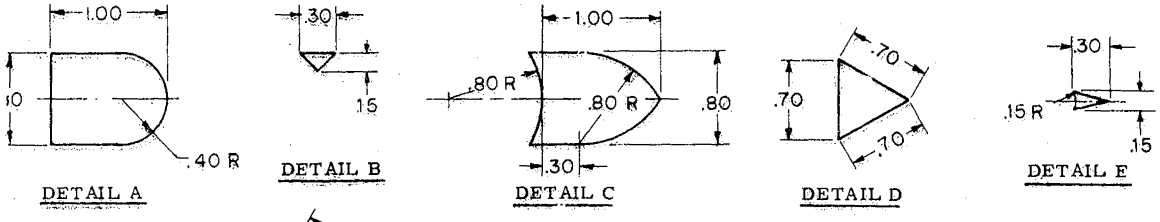


t_r	(0.2)	indicates the rise time in microseconds
t_d	(3)	indicates the duration in microseconds
t_f	(0.5)	indicates the fall time in microseconds
v_d	(10)	indicates the amplitude in volts
i_d	(10)	indicates the amplitude in amperes

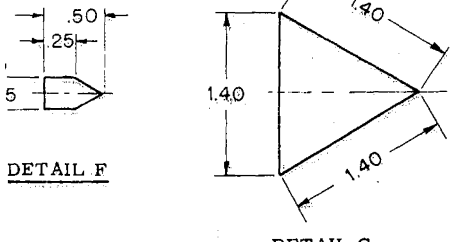
7. MECHANICAL AID

7.1 The template shown below illustrates the relative sizes of logic symbols.

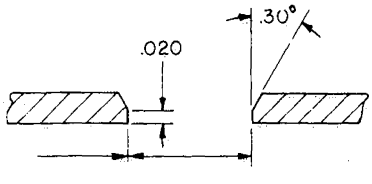




DETAIL A DETAIL B DETAIL C DETAIL D DETAIL E



DETAIL F DETAIL G



TYPICAL SECTION

MATERIAL - CELLULOSE ACETATE BUTYRATE .060 THK, GREEN, TRANSPARENT. BOTH SURFACES POLISHED.

NOTES

1. SIDES TO BE SQUARE AND PARALLEL.
2. ALL CUTOUTS TO BE CHAMFERED AS SHOWN IN TYPICAL SECTION.
3. ALL DIMENSIONS ARE GIVEN TO THE SMALLEST SECTION OF OPENINGS, AS SHOWN IN TYPICAL SECTION, AND REFER TO LINES MADE USING THE TEMPLATE AND A SHARP PENCIL EXCEPT 28 EACH .02 HOLES ARE PENCIL POINT HOLES.
4. TOLERANCE ON ANGLES $\pm 2^{\circ}$.

APPENDIX A

CIRCUIT AND SYMBOL CORRESPONDENCE EXAMPLES

10.1 Examples below illustrate:

(a) Basic circuitry of typical digital device hardware. In practice the hardware chosen to implement basic logic functions may be in many other forms, dependent on design criteria or the state of the art.

(b) Applications of graphic symbols relating hardware to logic functions drawn on detailed logic diagrams. Numerals on illustrations are input-output pin numbers.

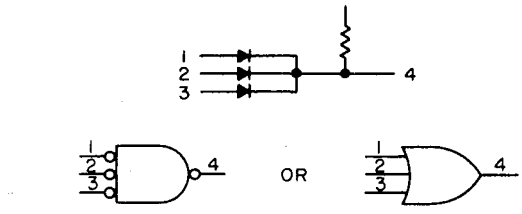


FIG. 1

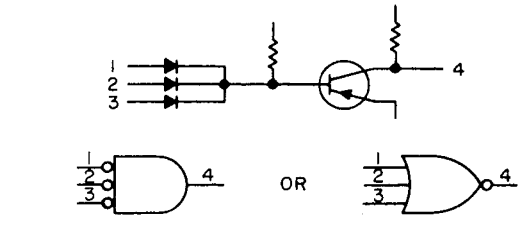


FIG. 2

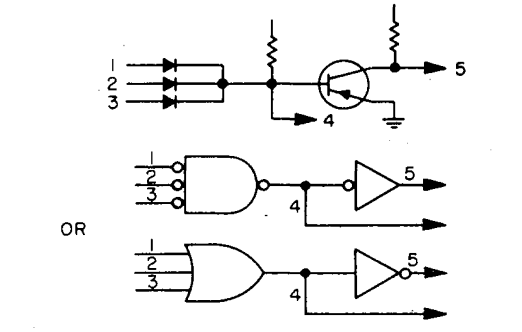


FIG. 3

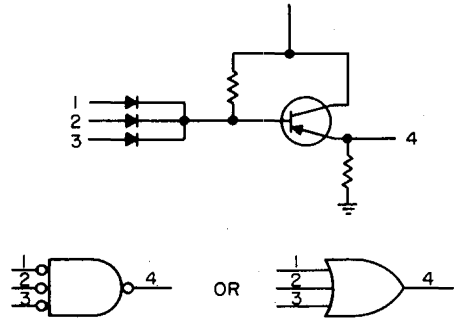


FIG. 4

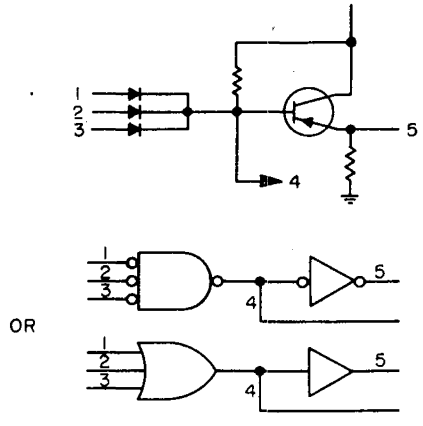


FIG. 5

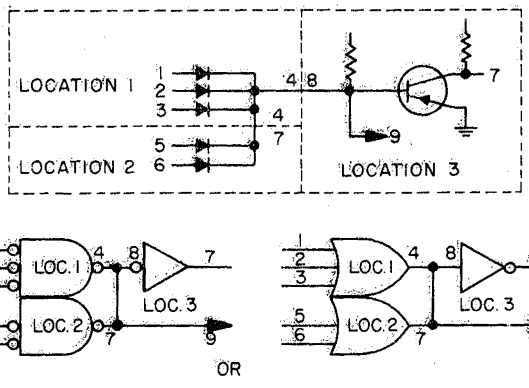


FIG. 6

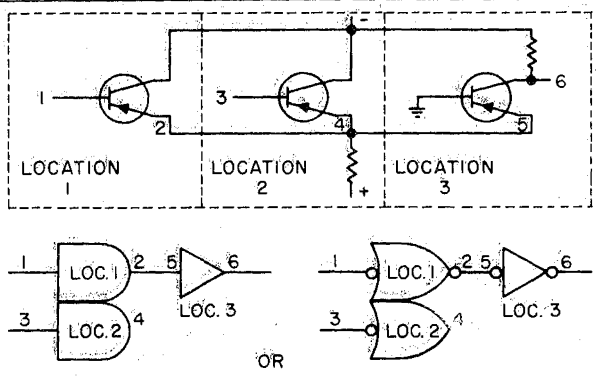


FIG. 10

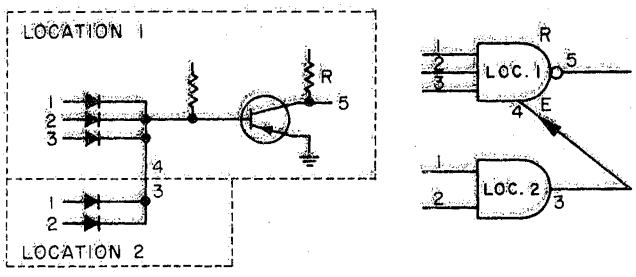


FIG. 7

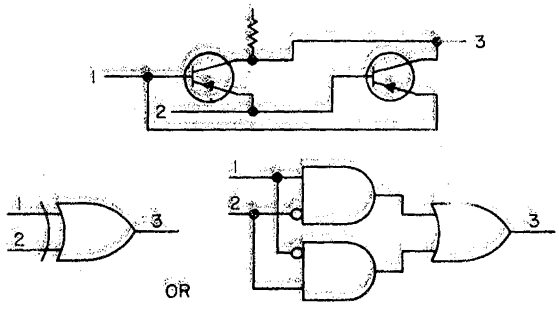


FIG. 11

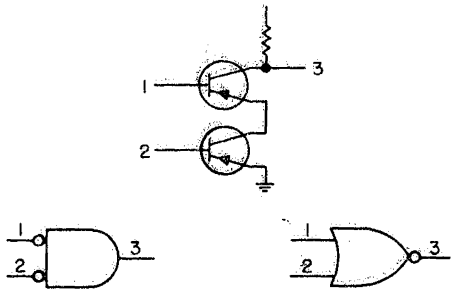


FIG. 8

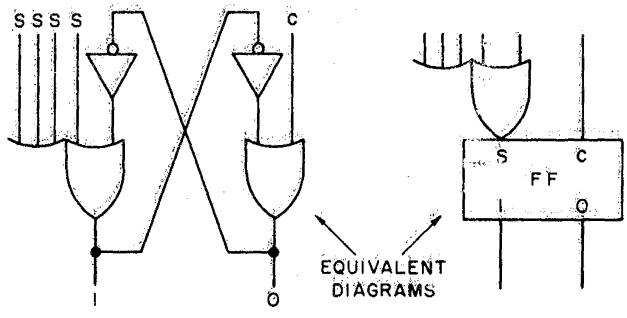


FIG. 12 FIG. 12A

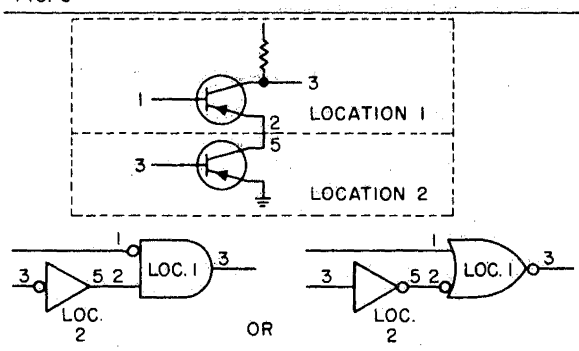


FIG. 9

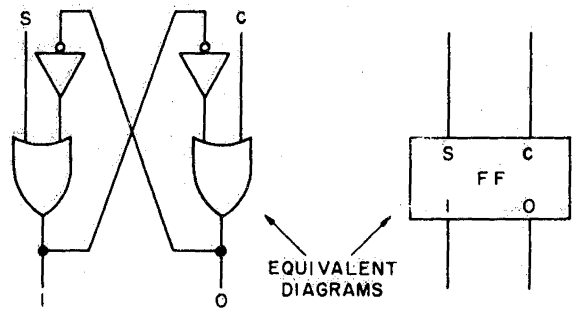


FIG. 13 FIG. 13A

APPENDIX B

ASSIGNMENT OF LOGIC LEVELS TO BINARY LOGIC ELEMENTS

20.1 A single arrangement of hardware may perform both the AND function or the OR function. This functional duality is employed in numerous single device, as well as multi-device systems.

The following tables and their related paragraphs develop the convention of considering the AND function as an element whose output is "active" when all its inputs are "active". Any AND input "nonactive" will produce a "nonactive" output. The OR function is considered an element whose output is "active" when any one or more input(s) are "active". All OR inputs "nonactive" will produce a "nonactive output".

Note that the above activity definitions do not refer to logical one, logical zero or electrical reference states.

To identify the activity of a device selected to implement the logic, the state condition of active input(s) and the resultant active output are identified by the presence or absence of active state signal indicators (small circles) at the input(s) or output of logic functions (AND/OR).

These graphic representations as well as English notations are employed to illustrate the relationship of specific functions operating individually or interconnected to perform machine functional operations as a system.

A small circle at the input(s) indicates that the relatively low (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively high (H) input signal activates the function.

A small circle at the symbol output side indicates that the output of the activated function is relatively low (L). Absence of a small circle at the symbol output indicates that the output of the activated function is relatively high (H).

The presence of an indicated active output does not necessarily provide a useful input to other elements. It may prevent the operation of some and enable others. Conversely, the absence of the indicated output signal state may provide a useful input to elements in the logical net and prevent the operation of others.

Activating input(s) or an activated output of a function may be (a) logical "one" in either the more positive high state (H) or the less positive low state (L), (b) a logical "zero" either high or low, or (c) a mixture of both "one" or "zero" either high or low.

20.2a Consider a device whose active output (F) is a function of two signals (A, B). The output and both input levels are capable of assuming only the arbitrarily chosen values, +2 volts (High "H") and -3 volts (Low "L"). The circuit behaves according to Device Activity States Table 1 below.

Substitution of mnemonic abbreviation "H" for the +2V levels and "L" for the -3V levels in Table 1 results in Activity Combinations Table 3 below.

When the +2V level is considered the activating level and is assigned the logic value 1 and the -3V level is considered the inactive level and is the logic value 0, substitution of these logic state values for the Table 1 active voltage levels results in AND Function Activity States (Internal) Table 2. The device is now said to perform the AND function and is symbolized without level indicators.

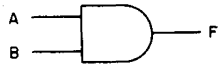


Fig. 1

20.2b Consider the same device behaving according to Table 1.

Substitution of mnemonic abbreviation "H" for the +2V levels and "L" for the -3V levels in Device Activity States Table 1 results in Activity Combinations Table 3 below.

When the -3V level is considered the activating level and is assigned the logic value 1 and the +2V level is considered the inactive level and is the logic value 0, substitution of these logic state values for the Table 1 active voltage levels results in OR Function Activity States (Internal) Table 4. The device is now said to perform the OR function and is symbolized with active level indicators.

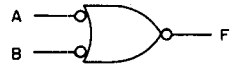


Fig. 2

Note upon comparison of Tables 2 and 3 with Tables 4 and 3, that logical "one", the active level, has been High for AND and Low for OR. Logic value one has been assigned to active presence signals.

(Electrical Truth)
Device Activity States
Table 1

Input		Output
A	B	F
+2V	+2V	+2V
+2V	-3V	-3V
-3V	+2V	-3V
-3V	-3V	-3V

AND Function Activity States
Table 2

Input		Output
A	B	F
1	1	1
1	0	0
0	1	0
0	0	0

Activity Combinations
Table 3

Input		Output
A	B	F
H	H	H
H	L	L
L	H	L
L	L	L

OR Function Activity States
Table 4

Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

20.3a Consider a different device whose active output (F) is a function of two signals (B, C). The output and both input levels are capable of assuming only the arbitrarily chosen values +2 volts (High "H") and -3 volts (Low "L"). The circuit behaves according to Device Activity States Table 5 below.

Substitution of mnemonic abbreviation "H" for +2V levels and "L" for -3V levels in Device Activity States Table 5 results in Activity Combinations Table 6 below.

Inputs (B, C) -3V levels are considered the activating input levels and are assigned the logic value 1, the +2V output level (F) is considered the activated output and is also assigned the logic value 1, inactive input levels +2V and the inactive -3V output level are assigned the logic value 0.

Substitution of these logic state assignments for Table 5 circuit voltage levels results in AND Function Activity States Table 7.

The device is now said to perform the AND logic function as defined by Table 7 and the AND electrically inverting operation as defined by Table 5 and combinations Table 6. Note that AND Function Activity States Tables 2 and 7 are identical.

The device is symbolized by combining the AND function symbol with input level indicators (electrically less positive than F).

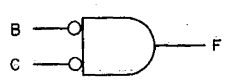


Fig. 3

20.3b Consider 20.3a device behaving according to Table 5.

Substitution of mnemonic abbreviations "H" for +2V levels and "L" for -3V levels results in Activity Combinations Table 6 below.

Inputs (B, C) +2V levels are considered the activating input levels and are assigned the logic value 1 and the -3V output level (F) is considered the activated output and is also assigned the logic value 1, inactive input levels -3V and the inactive +2V output level are assigned to the logic value 0.

Substitution of these logic state assignments for Table 5 circuit voltage levels results in OR Function Activity States Table 8.

The device is now said to perform the OR logic function as defined by Table 8 and the OR electrically inverting input operation as defined by Table 5 and combination Table 6. Note that OR Function Activity States Tables 4 and 8 are identical.

The device is symbolized by combining the OR function symbol with an output level indicator (electrically less positive than B, C).

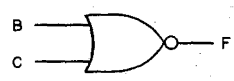


Fig. 4

(Electrical Truth)
Device Activity States
Table 5

Input		Output
B	C	F
-3V	-3V	+2V
-3V	+2V	-3V
+2V	-3V	-3V
+2V	+2V	-3V

AND Function Activity States
Table 7

Input		Output
B	C	F
1	1	1
1	0	0
0	1	0
0	0	0

OR Function Activity States
Table 8

Input		Output
B	C	F
0	0	0
0	1	1
1	0	1
1	1	1

Activity Combinations
Table 6

Input		Output
B	C	F
L	L	H
L	H	L
H	L	L
H	H	L

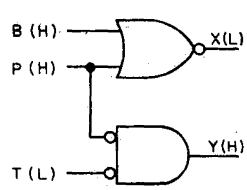
20.4 Notice in 20.3a and 20.3b discussions that logic value one has been assigned to presence signals for devices that are in their electrically active high or low input/output prescribed active states.

20.5 Electrical state English notations are added to signal line inputs and outputs when necessary to identify when that line is either logical one or zero within a logic network of operations. For example, if line P (H) is placed at the input to logic element(s), notation (H) indicates that line P signal is high when it exists, that is, a logical one. If upon inspection, line input P (H) is low, then it is in the logical zero state. This nonactive logical zero low state output may be utilized to activate a device input within the logic network that requires a low input for activation. Table 9 below illustrates this concept.

Table 9

Activity State	Device States	
	+2V	-3V
P (H)	1	0
B (H)	1	0
T (L)	0	1

Figure 5 illustrates that a given line signal P (H) will be active or inactive depending on what point in a logical network is being considered.



X = (B + P)(L)
B (H) or P (H) or both B (H) and P (H)

Y = ($\overline{P}$ • T) (H)
P (L) and T (L) = $\overline{P}$ and T (H)

Fig. 5

Notice that when P (H) is high as noted, it is in the logical one state, and will produce output X but will inhibit output Y. Conversely, when P does not exist as a high, it is in the logical zero state for the OR function and will produce AND output Y if line T is low.

The above illustrated that a given signal must be considered and when necessary notated in terms of three independently variable parameters listed below for every point in the logic network:

(1) Logical State; presence ("1") or absence ("0").
(2) Electrical State; high or low.
(3) Activity State; Signal Line condition, noted by graphic representation (presence or absence of small circles) or English notations (line name high or low).

APPENDIX C

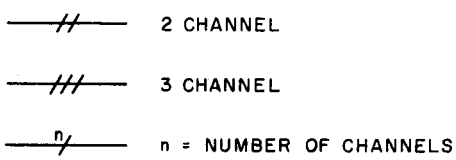
APPLICABLE SYMBOLS FROM OTHER MIL STANDARDS

30.1 The material contained in this appendix is provided to guide users to appli cable paragraphs in MIL-STD-15-1.

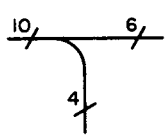
30.2 Single channel path. Refer to MIL-STD-15-1, item 58.1.

30.3 Signal flow. Refer to MIL-STD-15-1, item 32.1.

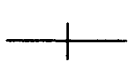
30.4 Multiple channel paths. Proposed revision to MIL-STD-15-1, items 58.2. 58.2.2 and 58.2.3.



30.4.1 Application: multiple channel paths with takeoff.



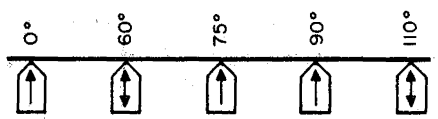
30.5 Signal paths crossing with no connection (not necessarily perpendicular). Refer to MIL-STD-15-1, item 58.5.



30.6 Junction of signal paths. Refer to MIL-STD-15-1, item 58.6.

30.7 Magnetic Heads. Refer to MIL-STD-15-1, item 61. These symbols represent reading, writing, and erasing functions or combinations thereof of magnetic heads.

30.7.1 Application: The following illustration represents a magnetic recording drum with magnetic heads.



30.8 Relay Electromagnetic. Refer to MIL-STD-15-1, item 66 for letter combinations to identify relay type (e.g., SO, SR, SA, etc).

30.8.1 Relay Coil. Refer to MIL-STD-15-1, item 16 for relay coil symbol.

30.8.2 Relay Contacts. Refer to MIL-STD-15-1, item 23.

APPENDIX D

LETTER COMBINATIONS

40.1 The following letter combinations shall be used with the graphic symbols to identify functions on logic diagrams:

BO	Blocking Oscillator
C	Clear (Reset)
CF	Cathode Follower
EF	Emitter Follower
FF	Flip-Flop
(N)	Number of Bits
SS	Single Shot
RG	Register
RG(N)	Register, N Stages
S	Set
ST	Schmitt Trigger
SR	Shift Register
T	Toggle (Trigger)

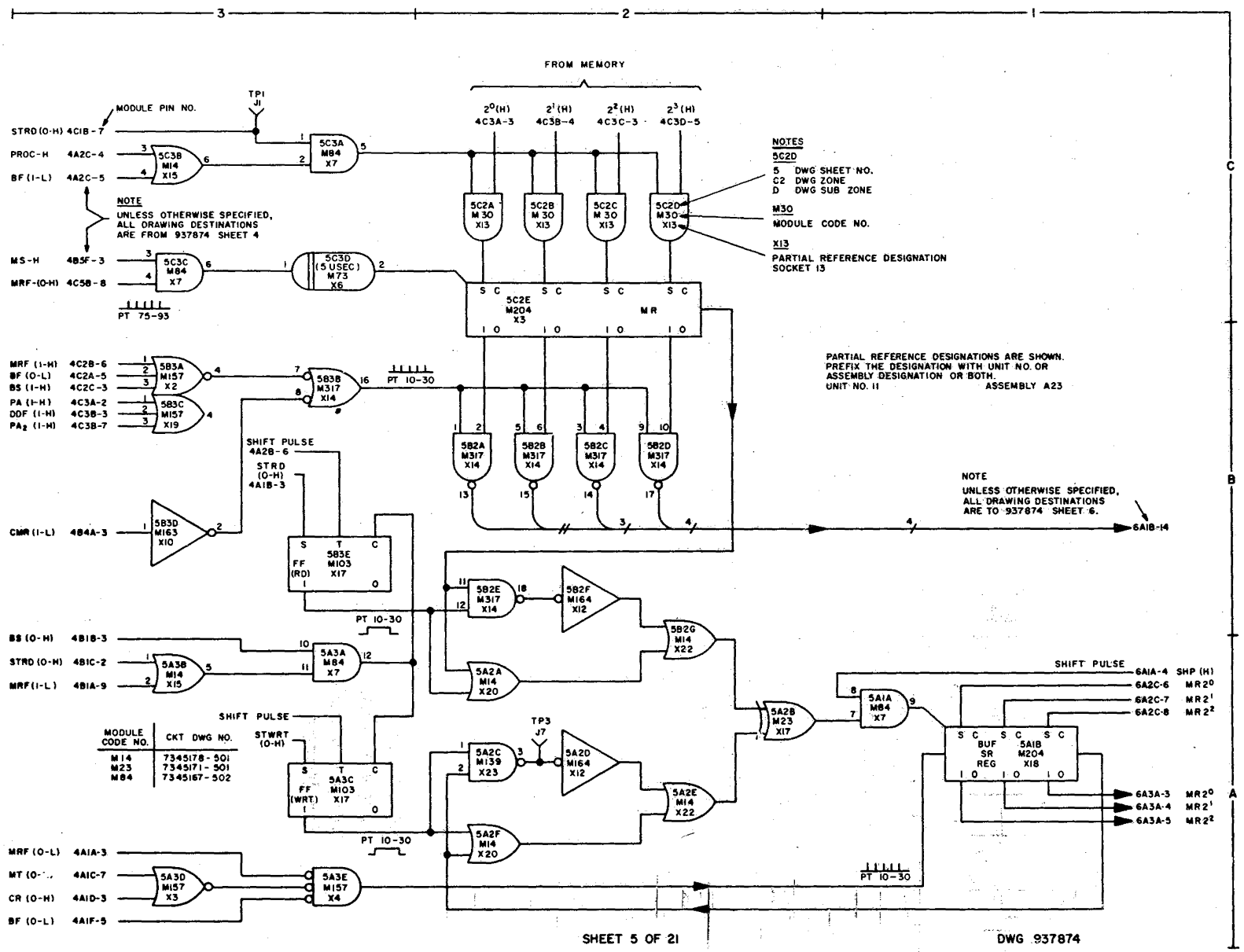
40.2 Letter combinations other than those in 40.1, shall receive prior approval by the procuring activity before they are used on logic diagrams.

40.3 Letter combinations and the General Symbol:

Functional identification placed within the General Symbol (5.13) shall always be spelled out.

APPENDIX E

EXAMPLE OF DETAILED LOGIC DIAGRAM



NOTICES

When government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication, or otherwise as in any manner licensing the holder or any other person, or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

Copies of specifications, standards, drawings and publications required by contractors in connection with specific procurement functions should be obtained from the procuring agency or as directed by the contracting officer.

Copies of this standard for military use may be obtained as indicated in the foreword to, or the general provisions of the Index of Military Specifications and Standards.

The title and identifying symbol should be stipulated when requesting copies of military standards.

Custodians:
Army - SigC
Navy - Ships
Air Force - AFSC

Preparing activity:
Air Force - AFSC
(Project MISC-0152)