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A TRANSISTOR SELECTION SYSTEM FOR A MAGNETIC-CORE MEMORY

by

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ABSTRACT

A TRANSISTOR SELECTION SYSTEM

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Square-hysteresis-loop magnetic material, magnetic-core memory operation, and various selection systems are discussed with emphasis on a two-coordinate READ, three-coordinate WRITE system using two-to-one selection-current ratios.

The proposed circuit is introduced in which selection is performed with saturated transistors and driving is a separate function. The requirements of a 64x64x17 memory operating with a 6 μsec duty cycle are used to specify the following transistor parameters:

$\alpha_n \geq 0.91$, $\alpha_I \geq 0.90$, $f_n \geq 6.7$ mc, $f_I \geq 6.7$ mc,

$V_{B_n} \geq 35$ V, $V_{B_I} \geq 20$ V, and $V_P \geq 20$ V.

Theoretical and empirical equations are used to predict the following construction limits for a high-current transistor-gate:

for an npn, $1 < \rho_b < 2$ Ω-cm, $0.2 < W_b < 0.5$ mils;

for a pnp, $1 < \rho_b < 2$ Ω-cm, $0.3 < W_b < 0.5$ mils.

The matrix and amplifier necessary to drive the transistor-gate are designed using a transistor matrix that is driven from transistor flip-flops.

Tests of some commercial transistors are described. Results are presented of an experimental transistor-gate level amplifier.

Thesis Supervisor: Richard D. Thornton

Title: Instructor in Electrical Engineering

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CHAPTER I

THE MAGNETIC-CORE MEMORY

1.0 Introduction: Solid-State Electronics Developments

Two solid-state devices have entered the commercial electronics field in the last few years, both being an outgrowth of research that took place during and after World War II.[1,2] The first of these devices to be used in digital computer applications was the square-hysteresis-loop magnetic core. These cores were initially made from ultra-thin metal tape;[3] later compressed forms of manganese-magnesium ferrites[3] having suitable characteristics were developed.

The development of the point contact transistor[4] excited computer engineers, but problems in manufacturing reliable transistors prohibited early application to computer design. The development of the junction transistor in 1950[5] again aroused hopes, but a poor frequency response and more manufacturing problems damped efforts to utilize this component in the computer field at that time. Recent developments[6] have placed the transistor on at least the same level as the vacuum tube with respect to reliability and control of characteristics, and there is a definite effort to use the transistor wherever its characteristics are superior to those of other devices.[7,8,9,10, 11]

This thesis evaluates the transistor as it is applied to the selection system of a magnetic-core memory in a digital computer. This first chapter includes a discussion of the magnetic core, an outline of an operating core memory, and a review of some possible selection systems.

1.1.0 History of Magnetic-Cores in the Digital Computer Field

The first application of magnetic-cores in the digital computer field was to the static delay line, or stepping register by A. Wang at the Harvard Computational Laboratory in 1948.[12] In 1949, J. W. Forrester[13] proposed that the cores be used in a three-dimensional storage device that could accept and return the complete binary number (a word) for each interrogation of the storage unit, i.e. the memory. In a stepping register it is necessary to shift the number out of the register one bit at a time (in series) as opposed to the three-dimensional memory from which a complete word is withdrawn as a unit (in parallel). In 1950 W. N. Papian[14] put a three-dimensional system into operation, however, the metallic cores employed did not prove satisfactory in this application because of the manner in which the selection was performed.

1.1.1 Metal-Tape Cores vs Ferrite Cores

If the hysteresis loop in Fig. 1.1 receives plus or minus $\frac{Hm}{2}$ units of magnetization, no permanent flux change will be induced for either remnant flux density condition, +Br or -Br (the only two possible quiescent flux states in this system). If the excitation is increased to +Hm and the core was originally at -Br, the flux will change to +Br, if originally at +Br, there will be little change in flux. The speed with which the flux change takes place is not indicated on the hysteresis loop, but is proportional to $H - \frac{Hm}{2}$ (where H is the total drive).

Ferrite cores are cheaper, smaller, more rugged, and have more closely controlled properties than metallic cores but their outstanding useful feature is a fast switching time when excited with Hm units of

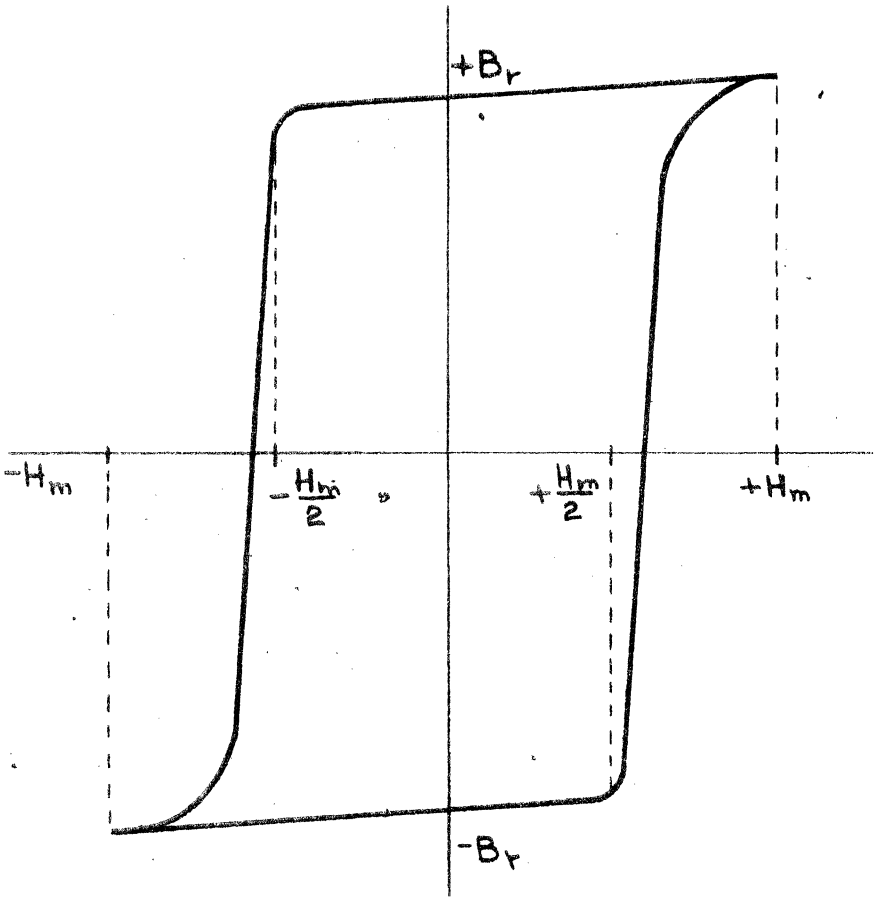

FIG. 1.1

TYPICAL MEMORY CORE HYSTERESIS LOOP

excitation. The square-hysteresis-loop ferrite material produced in 1952 by Dr. E. Albers-Schoenberg[15] needed more excitation than the metallic materials to move out to the $\frac{Hm}{2}$ point;* however, when the core was excited with Hm, the switching took place in approximately one microsecond. By comparison, the best metallic cores switch in 7 μs when excited with Hm. A metallic core of the same geometry as a ferrite core and with the same drive will switch faster and produce more flux change than the ferrite core. Consequently, metallic cores are more useful in stepping registers and matrix switches, while ferrite cores are more desirable in coincident-current applications where the maximum drive is limited to Hm.[3]

1.1.2 Magnetic-Core Memory Operation[13,14]

The ferrite cores, one for each binary bit, are assembled into arrays (a digit plane). These digit planes are then assembled in layers, one layer for each bit of word length, to form a complete memory as is shown in Fig. 1.2. If the memory is to contain 16 binary words, there will be eight drivers needed to select the cores, four on the Y coordinate and four on the X coordinate. The wires are so arranged and the directions of the currents in the X and Y lines are such that the magnetomotive forces add when both the X and Y wires through a core are excited.

The first step in interrogating the memory, the READ operation, is to send a pulse of current, $\frac{Im}{2}$ in magnitude, (corresponding to an mmf of $\frac{Hm}{2}$ in Fig. 1.1) down one x line and one y line.
The number of planes that will be excited corresponds

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* Hm varies from 8 amps/meter for the metallic tape material to 160 amps/meter for the ferrite material.

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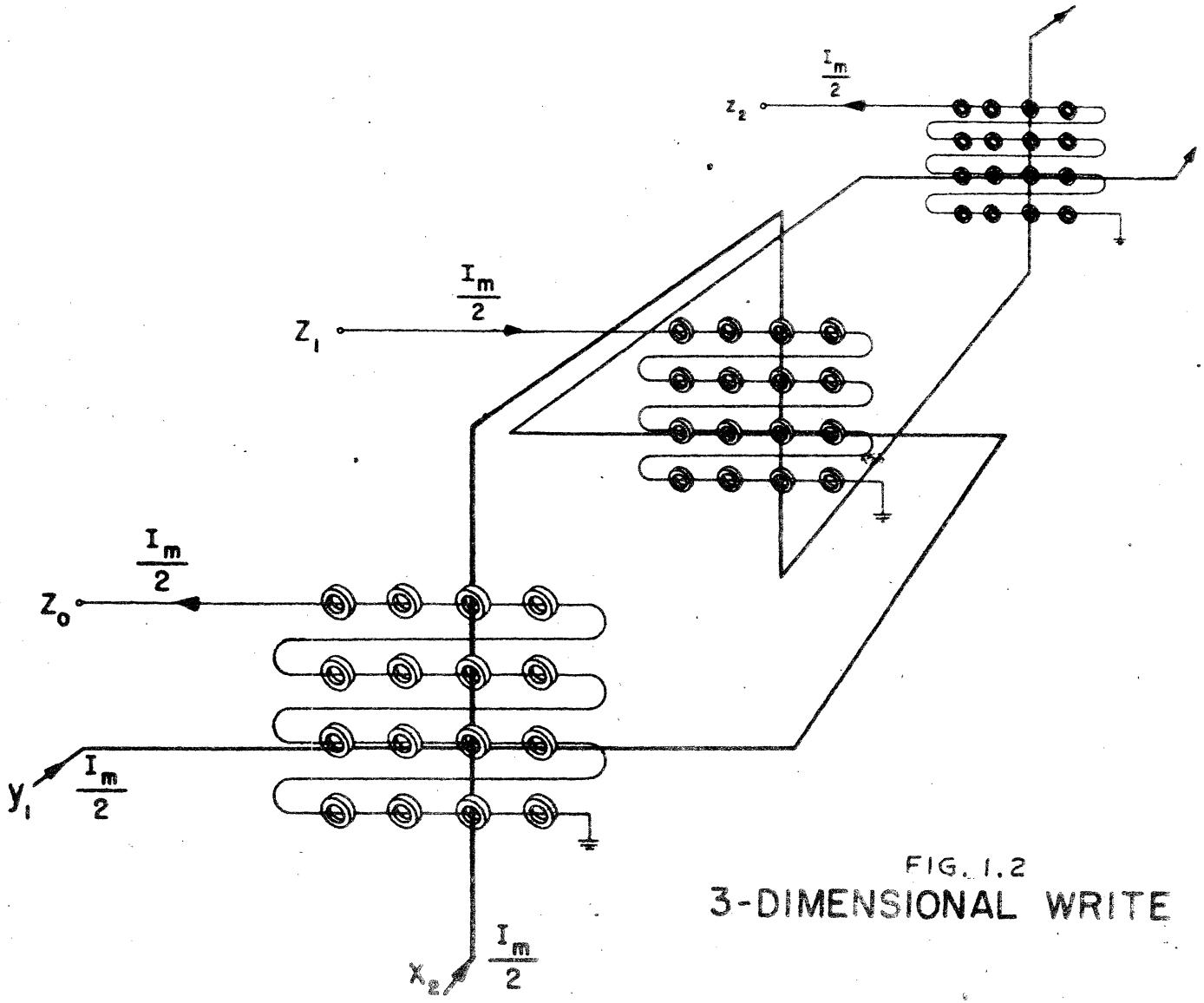

FIG. 1.2
3-DIMENSIONAL WRITE

to the number of binary bits in a word and there will be four cores on both the X line and the Y line in each plane that will receive excitation. Six of the cores in each plane receive $\frac{Im}{2}$ and there will be little flux change regardless of their original flux state. The core common to both the X and Y lines receives the sum of the two excitations, Im (an mmf of Hm), which is in the direction associated with the binary ZERO. If the core were already in the ZERO state, there would be a very small flux change, but if it had been in the remnant flux state defined as a binary ONE, there would be a large flux change during the time the core is switching to the ZERO state. A flux change will generate a voltage in any conductor threading the flux, therefore all the conductors passing through a core containing a ONE will have a voltage induced in them when the core is switched to the ZERO state. In each plane only one core per interrogation can generate a ONE signal since only one core receives Im excitation, therefore, a winding passing through every core in the plane will detect the signal from the selected core. Note also that the information in the memory at this particular address is now a binary ZERO. There are also small outputs from the cores that receive $\frac{Im}{2}$ and in a large plane they would mask the single ONE, so a special winding, the sense winding, is threaded through the cores in such a way that the noise signals tend to cancel and only the ONE signal remains at the output.

The next operation, WRITE, reverses the direction of the current pulses in the X and Y selection lines so that all the cores at the intersections are now driven in the ONE direction. All cores driven in this manner are switched to the ONE state.

To WRITE a ZERO into a particular bit in a word, the Z winding associated with the bit is driven in a direction to set all the cores in this particular plane to the ZERO state with a pulse (called the INHIBIT pulse) of $\frac{Im}{2}$ amplitude. Cores that were unexcited during the READ operation now receive $\frac{Im}{2}$ in the ZERO direction, cores that have an X or Y drive of $\frac{Im}{2}$ in the ONE direction, have no net drive; the single core with the X and Y drive of $\frac{Im}{2}$ has a resulting drive of $\frac{Im}{2}$ in the ONE direction and remains in the ZERO state; therefore, none of the cores change their flux state.

The logical equipment needed to perform the selection of the X and Y coordinates is shown in Fig. 1.3 for a memory with 4096 words of storage. The memory-address-register (MAR) receives its information from the digit-transfer-bus and feeds out complementary levels to two separate diode matrixes,[16] one for the X and one for the Y coordinate lines. The output of each diode matrix consists of 63 low (unselected) levels, and one high (selected) level. Each of the 64 levels is fed to a READ gate and a WRITE gate associated with a particular selection line in the memory. When the READ driver is pulsed, one of the READ gates will conduct allowing $\frac{Im}{2}$ to flow through the selected line. The READ drivers in both X and Y are controlled by the same flip-flop so that both X and Y currents flow at the same time. When the WRITE driver is pulsed, the WRITE gate, associated with the READ gate that was just activated, conducts and $\frac{Im}{2}$ flows along the lines in the opposite direction performing the WRITE operation.

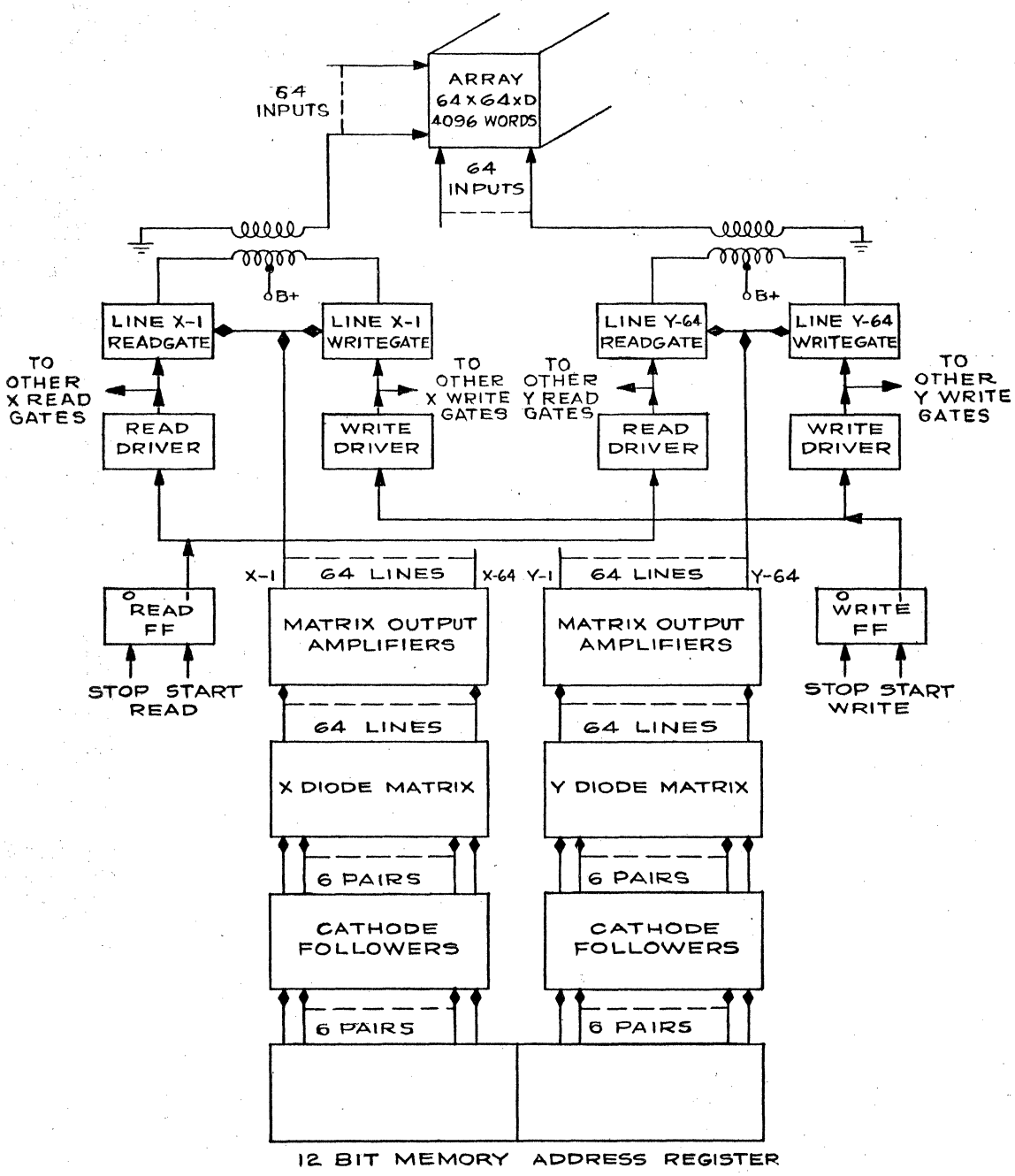

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FIG. 1.3

SELECTION SYSTEM BLOCK DIAGRAM

The timing diagram for the Whirlwind* memory cycle is shown in Fig. 1.4 and includes the relationship between the READ, WRITE, and INHIBIT pulses. The CLOCK pulse puts information into the MAR and starts the sequence that activates the current generators. The STROBE pulse samples the sense winding output at a time when the noise associated with ZERO pulses has dropped to zero and the ONE is just reaching its peak. The noise signals are associated with the rise and fall of the selection line and digit plane currents. The inhibit signal is much larger than any other signal on the sense winding since almost every core in the plane received $\pm \frac{Im}{2}$.

1.1.3 Other Selection Systems

The system described above is one of a group of multi-coordinate selection systems[17,18] in which the magnitude of the selected-to-unselected current ratio is an important parameter. In the above system it was 2:1 during both the READ and WRITE operation (i.e., the selected core received Im while the largest unselected signal was $\frac{Im}{2}$) although 2 coordinates, X and Y, were used to READ and 3 coordinates, X, Y, and Z, were used to WRITE. When the same selection system is used for reading as is used for writing, one more dimension, or coordinate, must be used during the WRITE operation to control the information to be written back into each digit of the selected word.

If more than three coordinates are used, the current ratio will decrease and the core will switch more slowly, less current will be required per coordinate (a desirable feature in a transistor system), and fewer driving lines will be needed.

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* Whirlwind is a digital computer in the Digital Computer Laboratory, Massachusetts Institute of Technology, and in 1953 became the first operational computer to use a magnetic-core memory.

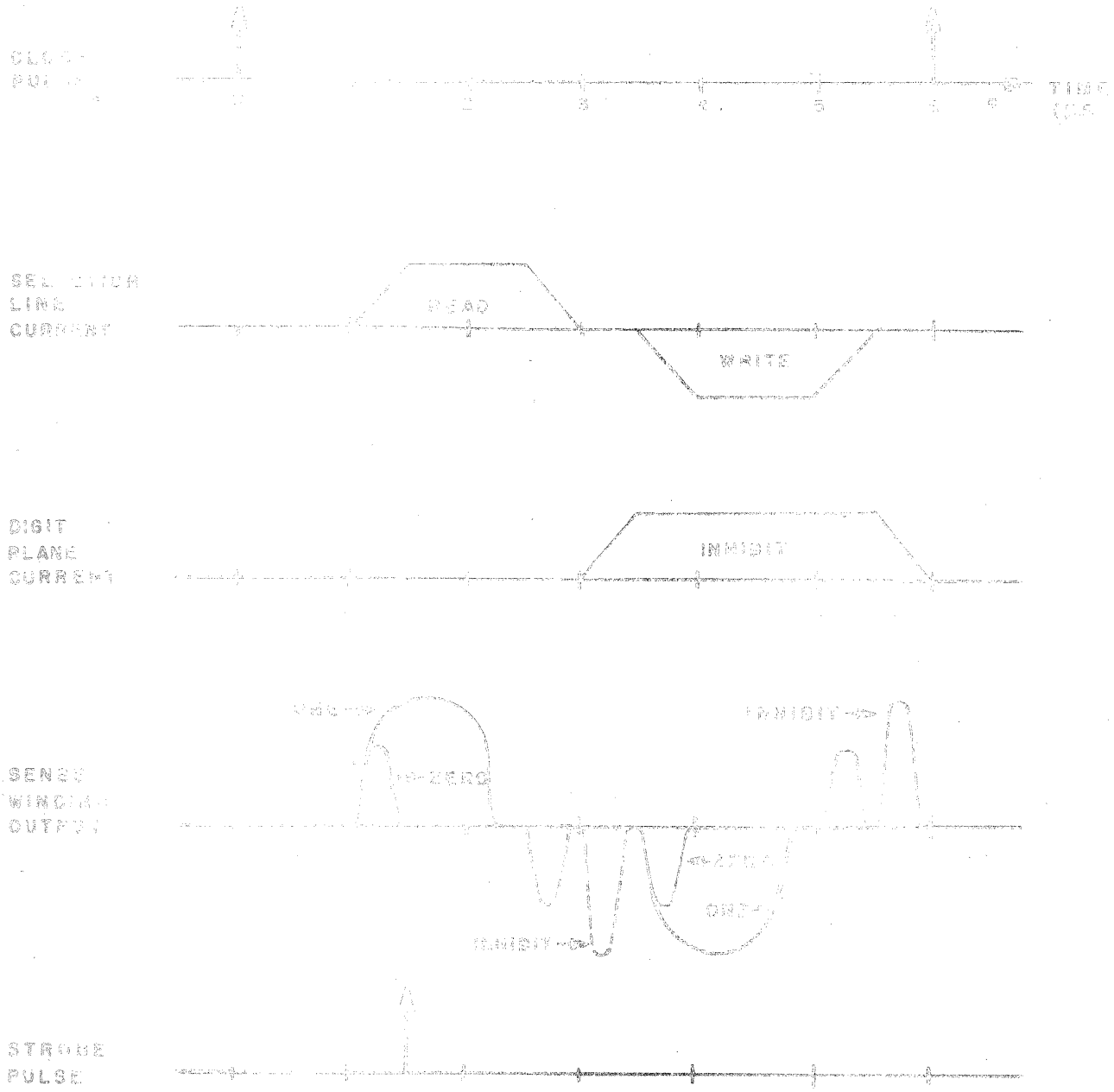


FIG. 1.4

MEMORY CYCLE TIMING DIAGRAM

For a register drive system in which one coordinate is selected[19,20] for READ, two coordinates will be necessary for WRITE and the maximum current ratio will be 3:1. Faster switching time is thereby possible but at the expense of a great increase in selection equipment for one selection line is required for each word and for each digit plane.

Redundant coordinate selection systems[21] result in high selected-to-unselected current ratios on the READ operation, but the additional coordinate on WRITE reduces the system to a non-redundant one with its restriction of low selected-to-unselected current ratio resulting in long switching times.

1.1.4 Characteristics of a 64 x 64 x 17 Magnetic-Core Memory

Although the design procedure will be carried out in general terms, it will be specifically aimed at developing the characteristics of a selection system for a 4096 word magnetic-core memory where the words are 17 binary bits long. A memory of this size, 64 x 64 x 17, is in use at Lincoln Laboratory and represents enough storage to perform many scientific problems.

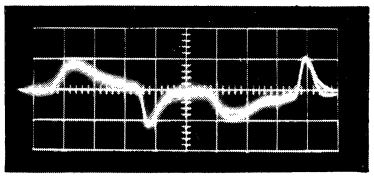
Although the type of magnetic material was narrowed down to the ferrites in Sec. 1.1.1, there are two types of ferrites in the size suitable for memory cores.* General Ceramics S-1 material, in the memory -core size, has a coercive force of 0.41 amp-turns and switches in 1 μsec with twice the coercive force applied (Im in the previous discussion). S-3 material has a coercive force of only 0.175 amp-turns,

* Present memory cores have an outside diameter of 0.080", an inside diameter of 0.050" and a height of 0.025".

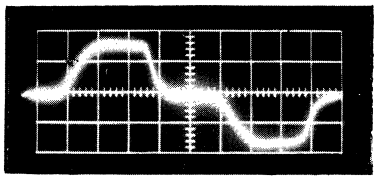
but takes 5 μsec to switch. The S-1 material will be selected on the bases of its shorter switching time, but the S-3 material should be kept in mind in case a serious problem develops with respect to the amplitude of current.

When a selection line is driven with a step of current, the half-selected cores, which greatly outnumber the fully-selected cores, present an inductive load to the current driver, and the equivalent inductance per memory core is 0.01 μhenry. To switch the selected cores in the shortest time they should be driven by a step of current; however, the rise and fall time of the current should be as long as possible to reduce the back voltage of the half-selected cores. As a compromise, the rise and fall times are chosen as 1/2 μsec, and the 0.41 amp pulse produces about 0.01 volt per core driven. With 1088 cores on a selection line there is a peak back voltage of about 11 volts. The current and voltage waveforms for a particular selection line are shown in Fig. 1.5 while writing alternately ONE's and ZERO's. Although it is possible to break one selection line into several segments, it seems possible and it is desirable to drive the above selection line as a unit-the design will be on this basis.

To take advantage of the short memory-core switching time, the turn-on and turn-off times of the selection lines should be a small part of the total memory cycle time. The cycle timing shown in Fig. 1.4 will be used as a guide in the transistor design since it is representative of the actual timing used in developmental core-memories in Lincoln Laboratory. The selected line must be ready for the READ current 1 μs after the clock pulse occurs. The previously selected line must be ready for the back voltage associated with the



SELECTION LINE VOLTAGE



SELECTION LINE CURRENT

FIG. 1.5

SELECTION LINE VOLTAGE & CURRENT FOR A 64 X 64 X 17 MEMORY

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READ pulse in the same time interval; however, if the transistors are unable to recover in 1 μs, the selected line might be turned off 1/2 μs before the clock pulse occurs and thus give 1 1/2 μs for recovery.

CHAPTER II

SELECTION SYSTEM REQUIREMENTS

2.0 Introduction

The fundamental task of the selection system is to accept at its input a binary coded address and at the proper time, as determined by other input signals, cause the information to be read out of the memory by setting all of the selected cores to ZERO. After a specified interval, it must drive the cores so that the word just read will be set to all ONE's if other equipment is not used to inhibit this action.

The particular manner in which the currents are controlled is dependent to some extent upon the memory selection system. The following discussion will apply to a two-coordinate-READ, three-coordinate-WRITE memory, in which the READ and WRITE currents use the same wires. The last restriction is due to the sizes of the memory cores and the wires used in the construction of the arrays. Larger memory cores would require more driving current and smaller wires would impose difficult construction problems.

2.1 Transformer Coupled Gates

Using the vacuum-tube selection system described in Sec. 1.1.2 as a guide, a transistor equivalent may be developed and one possible system is shown in Fig. 2.1 in block diagram form. If the line X_n is selected then the READ and WRITE gate outputs will be low impedances to ground, and if unselected, high impedances to ground. If the READ driver is pulsed when line X_n is selected, current will flow through

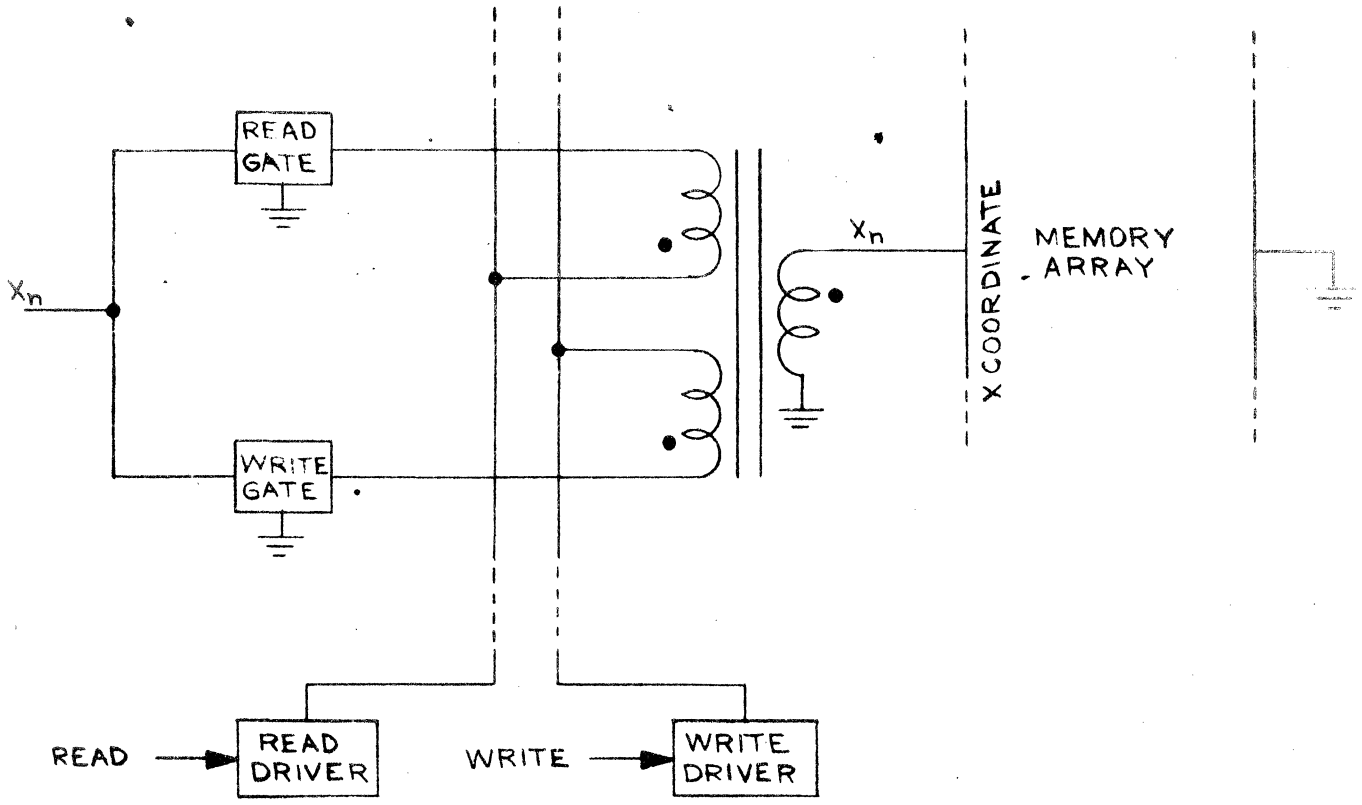

FIG. 2.1

TRANSFORMER COUPLED DRIVING SYSTEM

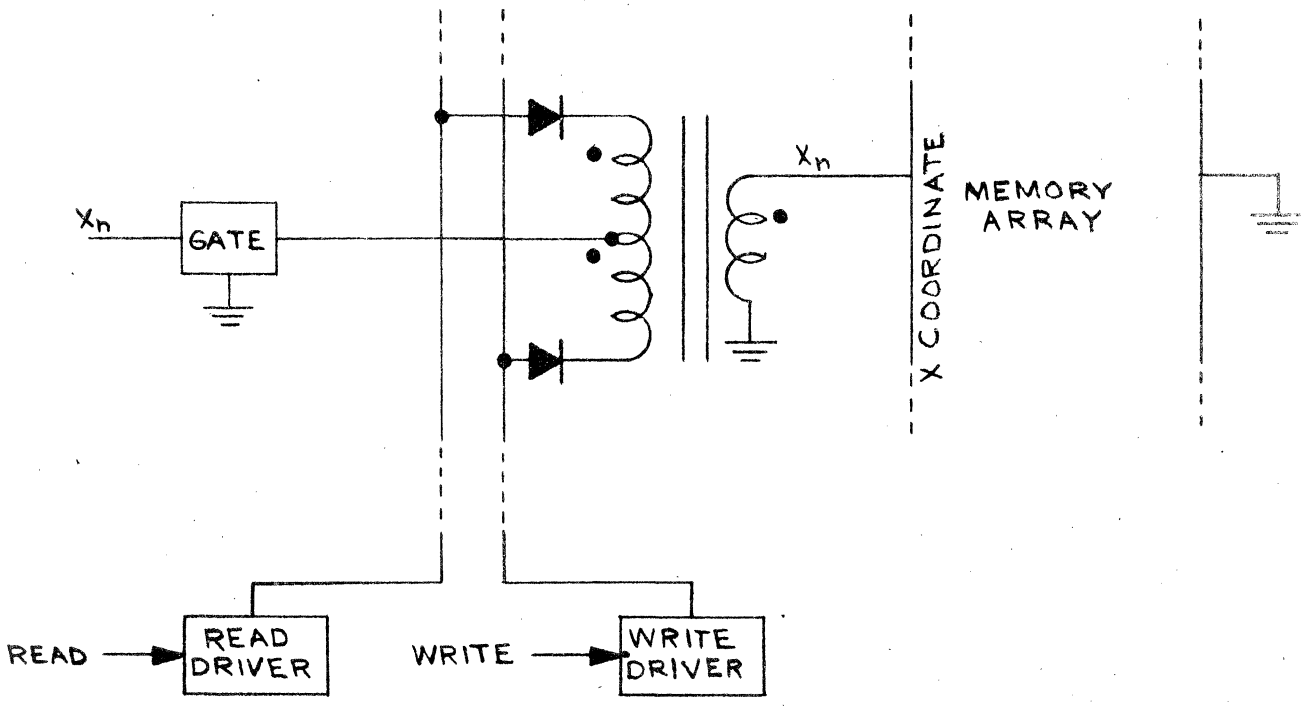

FIG. 2.2

TRANSFORMER COUPLED DRIVING SYSTEM WITH ONE GAT

one half of the primary of the pulse transformer[22] and through the READ gate to ground. The pulse will be coupled to the secondary (with an impedance transformation, if desirable,) and the half-select READ pulse, $\frac{Im}{2}$, will flow on line X_n. There will be a voltage developed across the pulse transformer that will appear at the READ driver and will also appear at the output of all the unselected READ gates. Due to inductive coupling there will also be a voltage developed at the WRITE driver and all the WRITE gates except the one selected. When the WRITE driver is pulsed the same action will take place except the current in the memory will be reversed.

Since the READ and WRITE gates each pass the driver currents, but at different times, it would be desirable to combine their operation. When this is done a system as is shown in Fig. 2.2 results. First consider the operation with the diodes shorted out. If X_n is selected and the READ driver pulsed, current will flow through the top half of the primary and through gate X_n to ground. There is also a path for current from the READ line through the rest of the pulse transformers, all in parallel, to the WRITE line and then through the bottom of the primary to the center-tap and to ground through the gate X_n. Since the primary is a continuous winding, the currents produce equal and opposite magnetization resulting in zero output and the system will not work. Inserting the diodes prevents current flow from the READ bus to the WRITE bus since one of the diodes will be reverse biased for current flow in either direction.

Unfortunately, the induced voltage across the lower half of the primary is of the polarity opposite to the voltage at the READ bus so that the diodes from the WRITE bus to the transformer have twice the READ bus voltage across them. They must also be able to carry the full driver current and, in general, as the forward current rating of diodes increases, the voltage ratings and reverse recovery characteristics deteriorate.

2.2 Direct Coupled Gates

Transformer coupling is useful in vacuum tube circuits, but it is not a necessary part of the selection system and certainly the losses and recovery time associated with transformers would not be missed.

If a vacuum tube has zero bias, current can flow from plate to cathode if the plate is made positive; but until the breakdown voltage is reached, making the plate negative will not cause plate current to flow in the reverse direction.

With a pnp transistor operated grounded-emitter and with current flowing out of the base, current will flow out of the collector when it is made negative. If the collector is made positive, current will flow into it.[23] For the same magnitude of voltage, the current will be higher for a negative collector unless the unit is symmetrical and then the currents will be about equal. Use will be made of the bilateral collector characteristics in the system described below to eliminate the pulse transformer.

Some of the first attempts to drive memory cores with transistors incorporated gating and driving in one transistor.[7] Transistors

had to operate in their active region where dissipation was a serious limitation. To operate units in parallel to meet this dissipation requirement is not economical when gating and driving can be performed in separate units as it is in vacuum tube systems. Olsen[24] suggested using symmetrical transistors (normal current gain, α_n, equal to inverse current gain, α_I) as gates. The gate would be saturated so that collector current could flow in either direction and the collector voltage would be low, resulting in little power dissipation. The driver can use several transistors since only two READ drivers and two WRITE drivers are required for the complete memory as compated to 128 gates for a 64 x 64 x 17 memory.

One end of each memory selection line will be connected to a transistor gate. The other ends of the X lines will all go to a common X coordinate READ-WRITE bus and the Y lines will go to the Y coordinate READ-WRITE bus. Although Fig. 2.3 shows the circuit for a single selection line with a pnp transistor, an npn could be used as well. When the line is unselected, the base-to-emitter voltage, V_{be}, is at a positive level, V_{OFF}, resulting in zero base current, I_b. The collector-to-emitter voltage, V_{ce}, swings positive and negative due to the voltage at the READ-WRITE bus, but the collector current, I_c, will be zero if the peak V_{ce}, V_m, is less than V_{OFF}. When selected, V_{be} drops to a slightly negative value and a base current, Ib_1, flows saturating the transistor. When the READ generator is pulsed, current will flow through the transistor, from either the collector-to-emitter or emitter-to-collector producing only a small V_{ce} due to saturation resistance of the transistor. If this line remains selected, the base

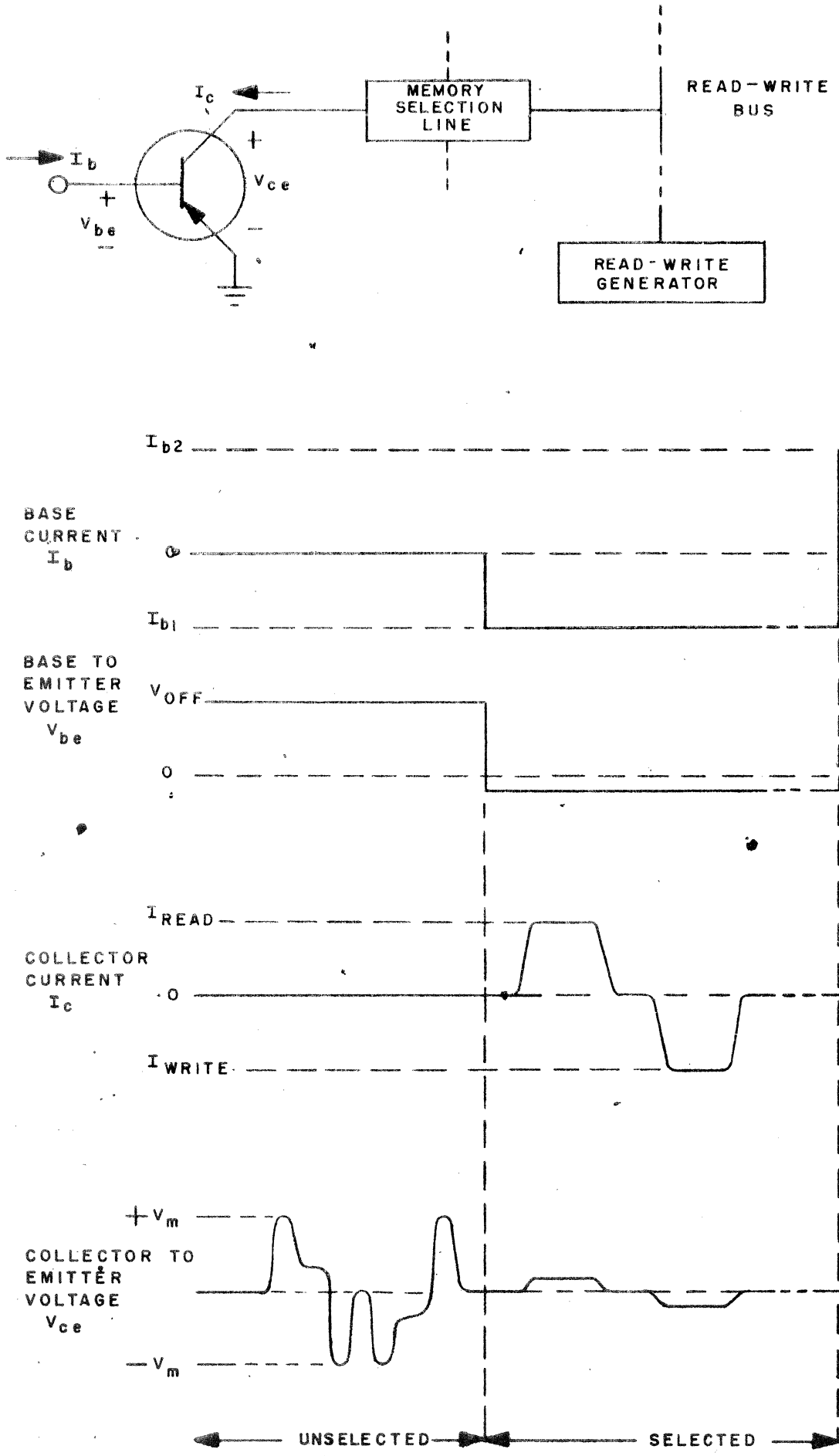

FIG. 2.3

VOLTAGES AND CURRENTS APPLIED TO TRANSISTOR SWITCH.

current remains constant and collector current will flow when the next interrogation of the memory is desired. When a different address is selected, V_b rises to a slightly positive value and the reverse base current, I_{b2}, removes the large charge of minority carriers that were stored in the base region. As the last of these carriers leave, the base-to-emitter resistance increases and V_{be} rises to V_{OFF}. If the transistor were an npn instead of a pnp, the base voltage and current would be reversed, but the operation of the remainder of the circuit would be unchanged.

2.3 Modifications to Direct Coupled Circuit

Although it is expected that suitable symmetrical transistors will be available, the same results can be obtained by connecting two transistors collector-to-emitter, base-to-base, and emitter-to-collector. The dual unit acts a symmetrical transistor[23] with a high current for either direction of collector current. The dissipation will be divided between the two units so that the power rating per transistor could be lower.

A combination of npn and pnp transistors would also provide the required gate action, but the opposite polarity of base drive required by the two types calls for dual sets of complementary input equipment.

2.4 Driving Specifications

The nominal value of collector current is ± 410 ma, but the transistor will be designed around a value of ± 425 ma in order to take care of possible variations in the selection currents. With the proper driving circuit, practically any transistor might be able to

perform the selection function but the necessary driving currents might well be larger than the current to be controlled as will be shown in Sec. 5.1.1. To keep the number of transistors in the driving circuit down to a reasonable level, a minimum grounded-emitter current gain (B) of 10 will be required for a collector current of 425 ma in either direction. This means that normal alpha ($\alpha_n = \frac{I_c}{I_e}$) must be greater than 0.91 with I_c = 425 ma, and that inverted alpha ($\alpha_I = \frac{I_e}{I_c}$) must be greater than 0.90 at I_e = 380 ma.

The base current should be as high as possible to decrease the turn-on time, slightly above $\frac{I_c}{B}$ during the ON time, and as low as possible just before the transistor is turned off. An increase in base current may be achieved during the turn-on time by shunting the external base resistance with a capacitor. Judging from some early experimental work, a minimum of 50 ma of base current can be expected during the first 1/2 μsec after a gate is activated. For the following calculations, it will be assumed that the base current can be controlled between the limits of 45 to 48 ma after the first μsec of base current flow.

A large reverse base current (I_{b_2} in Fig. 2.3) reduces the effect of minority carrier storage [25, 26, 27] in the base region; moreover, a large I_{b_2} is essential in the above system to shut the transistor off on the required time. This current will be supplied by connecting the base of the transistor to the OFF voltage through a low impedance path.

The maximum voltage that will appear on any non-selected memory line is 64 x 17 x 0.01 = 11 volts. To insure that each line is

turned off, the input line to the transistor-gates will be held at the OFF voltage (+ 15 volts).

2.5.0 Transistor Specifications

From the preceeding sections, the following requirements must be met by a suitable transistor:

1. The transistor must have $\alpha_n \geq 0.91$ with $I_C = 425$ ma, and $\alpha_I \geq 0.90$ with $I_C = 425$ ma.
2. It must be capable of dissipating the power associated with a continuous base current of 48 ma and an output current of 425 ma occuring with a 50% duty factor.
3. It must be ready to pass the output current 1/2 μsec after a 45 ma step of current is applied to the base.
4. It must be able to withstand the back voltage 1/2 μsec after it has been shifted from a selected to a non-selected state. This requirement can be decreased to 1 μsec if it would materially aid the transistor design.
5. The turn-off must be accomplished with a maximum peak reverse base-current of 100 ma.

2.5.1 Voltage Ratings

The sequence of voltages and currents to be applied to the transistor gate are shown in Fig. 1.5 for a pnp transistor. During the OFF condition, the base is held at V_{OFF}, and both the emitter and collector are at ground potential. This means that the body breakdown

voltage [28,29] (V_B, see Sec. 3.1.3.3) for BOTH emitter and collector diodes must be greater than V_{OFF}. When the READ-WRITE generator is activated a positive and negative peak in voltage occurs so that the maximum base-to-collector voltage, V_{cb}, is $V_{OFF} + V_M$ and the minimum collector body breakdown voltage (V_{BN}), must be greater than this value. The maximum voltage difference between the collector and emitter is V_m; therefore, the minimum punch through voltage [28,29] (V_P, see Sec. 3.1.3.2) must be greater than V_m.

2.5.2 Alpha Cutoff Frequency

If a transistor-gate is changed from OFF to ON, it must be in saturation before the READ driver is turned on. If a transistor has a load resistor and a voltage connected to the collector as in Fig. 2.4, and a step of current is applied to the base, the transistor will be in saturation when there is an excess of minority carriers at the collector junction. During the time that the transistor is moving through the active region, the minority carriers are being drawn out of the collector so that the time to get the transistor saturated is slightly longer than if the collector were open-circuited. Thus if the equation for the loaded case is used, it will be slightly pessimistic. The equations have been developed by Ebers and Moll [30] for the active region and Moll[27] has extended the analysis to large signal operation.

The turn-on time, τ_0, as shown in Fig. 2.4 is for the rise from 10% to 90% of the final value of current. In the above references τ_0 is calculated as the time to go from zero to 90% of the final value of current. In the system described above, it is mandatory that the

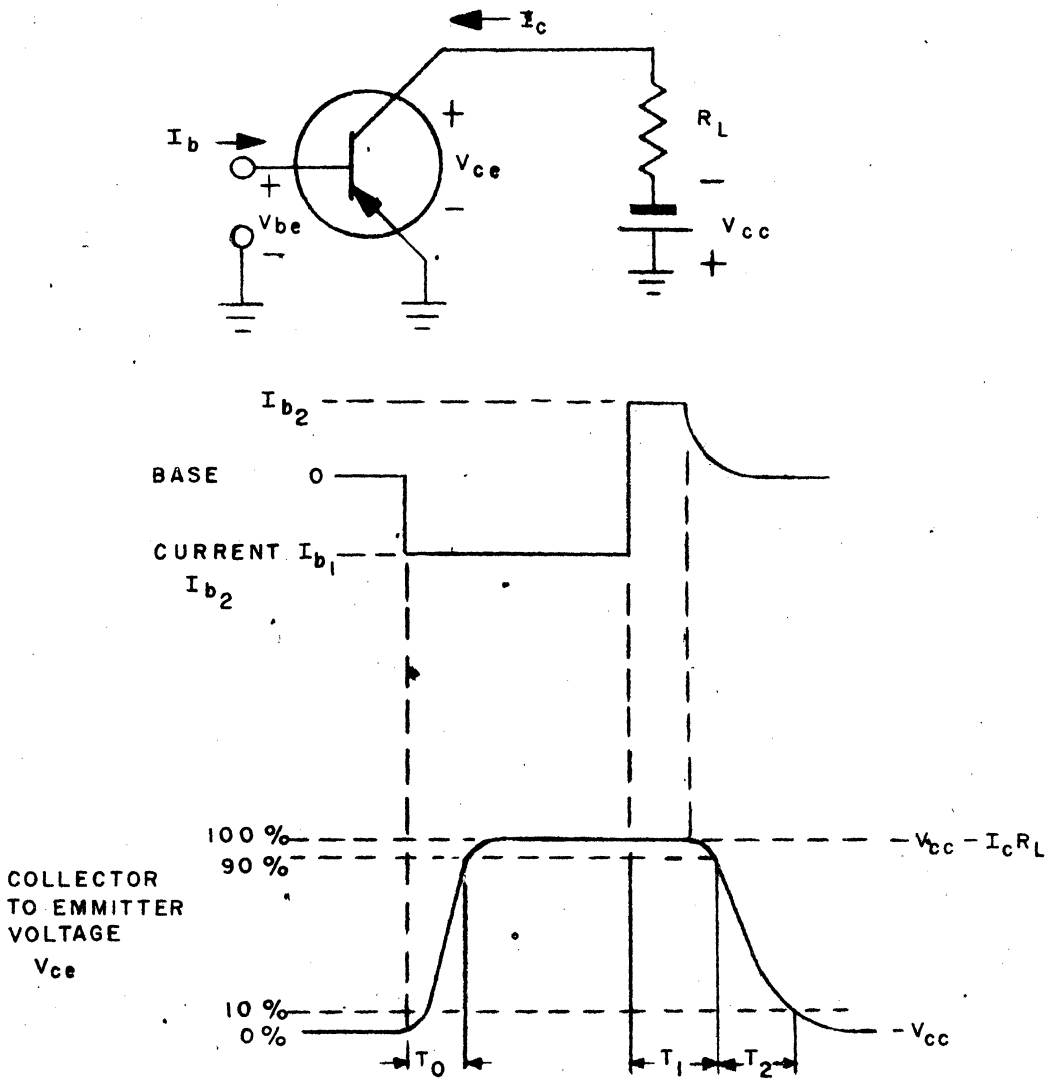

FIG. 2.4

RISE AND FALL TIME DEFINITIONS

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transistor be capable of carrying 100% of the final value of current τ_0 seconds after the step of base current is applied. Since the value of current in the equations is rising above the circuit's 100% value, it is possible to find the 100% value, and in fact, there is not too much difference in the value of τ_0 and it results in a factor of 0.9 being left out of Moll's equation for τ_0. In the following equations τ_0 is the complete turn-on time, α_n is the normal current gain when the transistor is operated grounded base, f_n is the frequency in cps at which α_n decreases to 0.707 of its low frequency value, I_{b_1} is the value of the step in base current and I_c is the value of the desired collector current.

$$\tau_0 = \frac{1}{2\pi f_n(1-\alpha_n)} \ln \frac{1}{1 - \frac{I_c}{I_{b_1}} \frac{1-\alpha_n}{\alpha_n}} . \qquad 2.1$$

For a specified maximum allowable turn-on time,

$$f_n \geq \frac{1}{2\pi\tau_0(1-\alpha_n)} \ln \frac{1}{1 - \frac{I_c}{I_{b_1}} \left(\frac{1-\alpha_n}{\alpha_n}\right)} . \qquad 2.2$$

f_n will be determined by the minimum value of I_{b_1} during turn-on and the maximum value of I_c. The variation with α_n is not immediately obvious because the quantity $\frac{1}{1-\alpha_n}$ is a maximum for the maximum value of α_n, unity, while the logarithmic term is zero at that point. Equation 2.2 is differentiated and set equal to zero in Appendix A, but it is shown that there are no critical points of f_n in the region $\frac{I_c}{I_c+I_{b_1}} \leq \alpha_n \leq 1$. To find the value of f_n at $\alpha_n = 1$, the limit must be taken because both the numerator and denominator go

to zero.

$$\lim_{\alpha_n \to 1}(f_n) = \lim_{\alpha_n \to 1} \frac{1}{2\pi\tau_0(1-\alpha_n)} \ln \frac{1}{1 - \frac{I_c}{I_{b1}}\left(\frac{1-\alpha_n}{\alpha_n}\right)}, \qquad 2.3$$

$$\lim_{\alpha_n \to 1}(f_n) = \frac{1}{2\pi} \frac{\frac{\partial}{\partial \alpha_n} \ln \frac{1}{1 - \frac{I_c}{I_{b1}}\left(\frac{1-\alpha_n}{\alpha_n}\right)}}{\frac{\partial}{\partial \alpha_n} \tau_0(1-\alpha_n)} = \frac{1}{2\pi} \lim_{\alpha_n \to 1}$$

$$\left[\frac{-\frac{I_c}{I_{b1}\alpha_n^2\left[1 - \frac{I_c}{I_{b1}}\left(\frac{1-\alpha_n}{\alpha_n}\right)\right]}}{-\tau_0} \right], \qquad 2.4$$

$$\lim_{\alpha_n \to 1}(f_n) = \frac{I_c}{2\pi\tau_0 I_{b1}} . \qquad 2.5$$

At $\alpha_n = \frac{I_c}{I_{b1} + I_c}$, the denominator of the logarithm goes to zero and the logarithm grows without limit. Since the coefficient remains non-zero, f_n must be infinite at this point.

The preceeding analysis indicates that for a given collector current, base current and turn on time, the minimum f_n can be lower if α_n is higher. There is a lower limit on f_n that is equal to $\frac{I_c}{2\pi\tau_0 I_{b1}}$ at α_n equal to 1, and as α_n decreases to $\frac{I_c}{I_c + I_b}$, the minimum required f_n increases without limit.

The turn-off time[27] Fig. 2.4, is divided into two regions corresponding to the period in which minority carriers are removed, τ_1, and the period in which the base to collector voltage is recovering, τ_2. If collector current is flowing, then the storage time, τ_1, will

be shorter for a given base current than it would be if the collector were open circuited. Unfortunately, the latter is the case in the transistor switch since the memory may have been inactive, but the transistor switch will still have base current flowing and the switch will be saturated. The expression for τ_1 is:

$$\tau_1 = \frac{f_n + f_I}{2\pi f_n f_I (1 - \alpha_n \alpha_I)} \ln \frac{I_{b1} - I_{b2}}{I_c(\frac{1-\alpha_n}{\alpha_n}) - I_{b2}} \quad . \tag{2.6}$$

The subscript I refers to the inverted parameters and I_{b2} is the reverse base current. If we substitute $I_c = 0$ and $I_{b2} = -NI_{b1}$ then

$$\tau_1 = \frac{f_n + f_I}{f_n f_I (1 - \alpha_n \alpha_I)} \ln \frac{N + 1}{N} \quad . \tag{2.7}$$

The expression for τ_2 involves I_c again, but now it must be left in the expression as it indicates the amount of collector current that would flow if the READ driver were activated. For the current to return to zero the expression is as follows:

$$\tau_2 = \frac{1}{2\pi f_n (1-\alpha_n)} \ln \frac{I_c - \frac{\alpha_n}{1-\alpha_n} I_{b2}}{-\frac{\alpha_n}{1-\alpha_n} I_{b2}}$$

$$= \frac{1}{2\pi f_n (1-\alpha_n)} \ln \left[1 + \frac{I_c (1-\alpha_n)}{N I_{b1} \alpha_n} \right] \quad . \tag{2.8}$$

The total turn-off time is $\tau_1 + \tau_2 = \tau_T$.

$$\tau_T = \frac{f_n + f_I}{2\pi f_n f_I (1-\alpha_n \alpha_I)} \ln \left(1 + \frac{1}{N}\right)$$

$$+ \frac{1}{2\pi f_n (1-\alpha_n)} \ln \left[1 + \frac{I_c (1-\alpha_n)}{N I_{b1} \alpha_n} \right] \quad . \tag{2.9}$$

If the transistor is symmetrical, then the assumption that $f_n = f_I$ is reasonable. The equation for the τ_T is:

$$\tau_T = \frac{1}{\pi f_n(1-\alpha_I\alpha_n)} \ln\left(1 + \frac{1}{N}\right) + \frac{1}{2\pi f_n(1-\alpha_n)} \ln\left[1 + \frac{I_c\,(1-\alpha_n)}{NI_{b1}\,\alpha_n}\right] . \qquad 2.10$$

Or, for a maximum turn-off time,

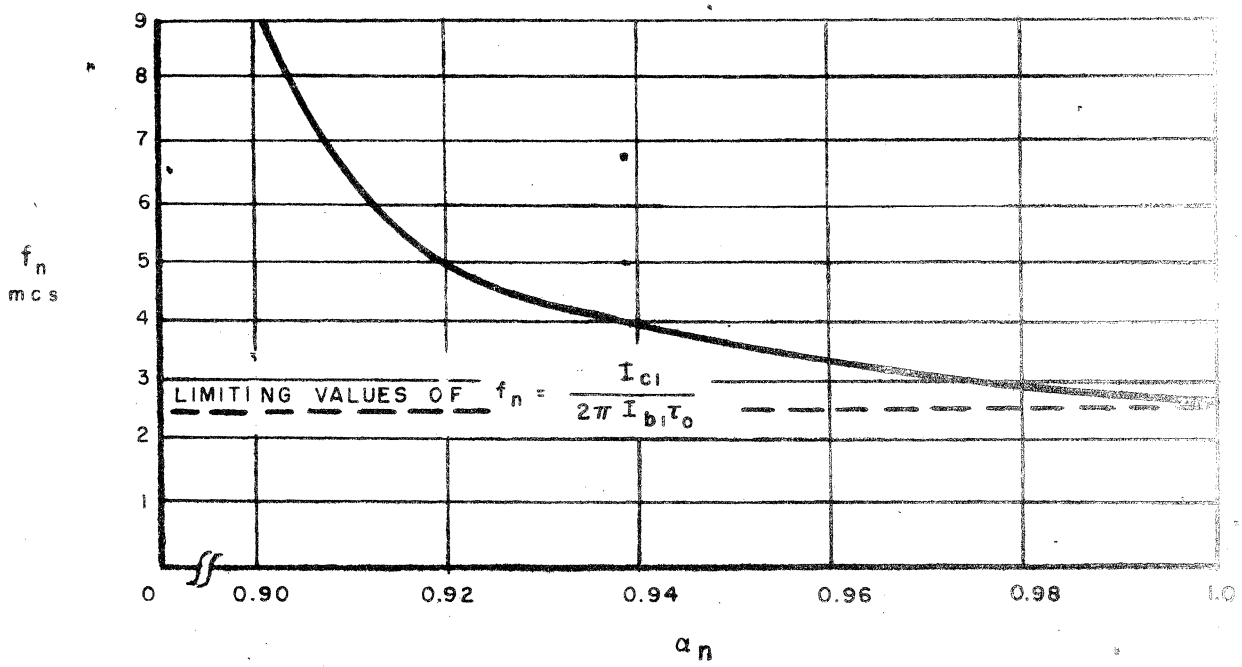
$$f_n \geq \frac{1}{2\pi\tau_T} \frac{2}{1-\alpha_I\alpha_n} \ln\left(1 + \frac{1}{N}\right) + \frac{1}{1-\alpha_n} \ln\left[1 + \frac{I_{c1}\,(1-\alpha_n)}{NI_{b1}\,\alpha_n}\right] . \qquad 2.11$$

In this equation N is an important factor. The required f_n may be determined from the turn-on time (equation 2.2) and that particular f_n may be used to indicate the required value of N.

When the minimum turn-on base current 50 ma, the maximum collector current, 425 ma, and the maximum turn-on time, 0.5 μsec, are substituted into Equation 2.2, it becomes:

$$f_n \geq \frac{0.318}{1-\alpha_n} \ln\left[\frac{1}{1 - 8.5\left(\frac{1-\alpha_n}{\alpha_n}\right)}\right] . \qquad 2.12$$

A graph of f_n (at the equality) vs α_n is shown in Fig. 2.5. It indicates that the f_n requirements could be reduced for units having a higher α_n but the maximum reduction would only be to 2.7 mc at α_n equal to unity instead of 6.7 mc at α_n equal to 0.91. With a group of transistors made by a similar process, variations in α_n and f_n will probably be caused by variations in the base width and an increase



$\tau_o = 0.5\ \mu s$

$I_{c1} = 425\ ma$

$I_{b1} = 50\ ma$

$$f_n = \frac{1}{2\pi\tau_o(1-\alpha_n)}\ \ell n\ \frac{1}{1-\frac{I_{c1}}{I_{b1}}\left(\frac{1-\alpha_n}{\alpha_n}\right)}$$

FIG. 2.5

MINIMUM POSSIBLE f_n FOR PARTICULAR VALUES OF α_n (TURN-ON)

in α_n will also be accompanied by an increase in f_n. No advantage will be gained from the above variation in the requirements on f_n, so a minimum f_n of 6.7 mc will be placed on the frequency response.

Use of the values for the maximum I_{b1} (48 ma), I_c (425 ma), and τ_T (0.5 μsec) together with the minimum values of α_n (=0.909) and α_I (=0.90) reduces the expression for the minimum allowable f_n on turn-off (Equation 2.11) to:

$$f_n \geq \frac{1}{\pi} \frac{2}{1 - (0.909)(0.90)} \ln \left(1 + \frac{1}{N}\right)$$

$$+ \frac{1}{1 - 0.909} \ln \left[1 + \frac{425\ (1 - 0.909)}{48\ (0.909)N}\right] . \qquad 2.13$$

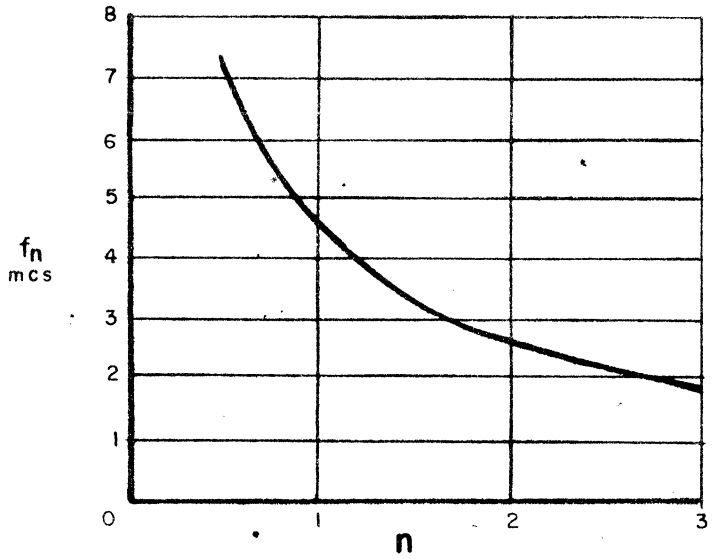
This reduces to:

$$f_n \geq 3.5 \ln \left(1 + \frac{1}{N}\right)\left(1 + \frac{0.885}{N}\right), \quad N = - \frac{I_{b2}}{I_{b1}} . \qquad 2.14$$

This is plotted in Fig. 2.6 for the range of N's that were encountered in some early tests. With high frequency transistors I_{b2} is not a constant value, but rather a ramp function of current. The rise time of the current is limited by the turn-on time of the transistor-gate level amplifier; nevertheless, an N of 2 is a conservative estimate of the peak of the lowest reverse base current to be expected. Substituting in the original expression for f_n (equation 2.11) N = 2, I_{b1} = 48, and I_c = 425, produces:

$$f_n \geq \frac{1}{\pi} \left(\frac{2}{1 - \alpha_I \alpha_n}\right) \ln 1.5 + \frac{1}{1 - \alpha_n} \ln \left[1 + \frac{425}{2\ (48)} \left(\frac{1 - \alpha_n}{\alpha_n}\right)\right] . \qquad 2.15$$

The maximum value of f_n occurs when α_I is a maximum. That substitution yields:



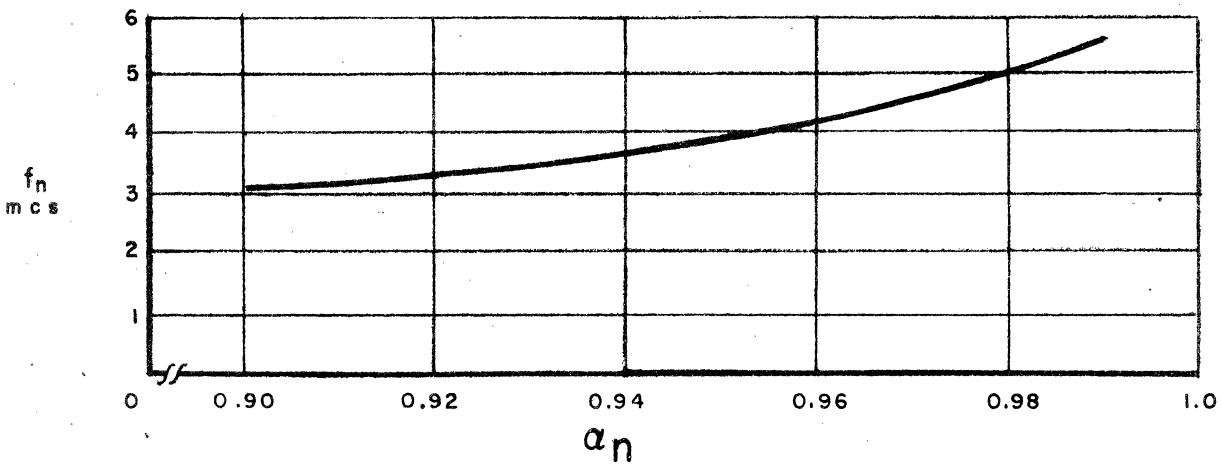
$\tau_T = 0.5\ \mu SEC$
$I_{b1} = 48$
$I_{c1} = 425$
$\alpha_n = 0.909$
$\alpha_I = 0.9$

$$f_n = \frac{1}{2\pi\tau_T}\left\{\frac{2}{1-\alpha_n\alpha_I}\ln\left(1+\frac{1}{n}\right)+\frac{1}{1-\alpha_n}\ln\left[1+\frac{I_{c1}(1-\alpha_n)}{nI_{b1}\alpha_n}\right]\right\}$$

$$n = -\frac{I_{b2}}{I_{b1}}$$

FIG. 2.6

MINIMUM POSSIBLE f_n FOR PARTICULAR VALUES OF n (TURN-OFF)



$\tau_T = 0.5\,\mu SEC$
$I_{c1} = 425$
$I_{b1} = 48$
$n = 2$
$\alpha_I = 0.95$

$$f_n = \frac{1}{2\pi\tau_T}\left\{\frac{2}{1-\alpha_n\alpha_I}\ln\left(1+\frac{1}{n}\right)+\frac{1}{1-\alpha_n}\ln\left[1+\frac{I_{c1}(1-\alpha_n)}{nI_{b1}\alpha_n}\right]\right\}$$

FIG. 2.7

MINIMUM POSSIBLE f_n FOR PARTICULAR VALUES OF α_n (TURN-OFF)

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$$f_n \geq \frac{0.258}{1 - .95\alpha_n} + \frac{0.318}{1-\alpha_n} \ln \left[1 + 4.43 \left(\frac{1-\alpha_n}{\alpha_n}\right)\right]. \qquad 2.16$$

This is plotted in Fig. 2.7 and indicates that the transistor must have a higher f_n if α_n is higher, but there is not a large change in f_n for $0.909 \leq \alpha_n \leq 0.99$. This range of f_n's, 3.1 to 5.5 mc, also falls below the minimum f_n as determined by the turn-on time restriction. Thus no restriction is necessary on the maximum α_n if N = 2 can be satisfied and the base currents fall within the required limits.

2.5.3. Saturation Currents

The collector-to-base saturation current (I_{c_o}, collector current with emitter open-circuited) and the emitter-to-base saturation current (I_{e_o}, emitter current with collector open-circuited) must be low to prevent erroneous operation of the memory. Errors can occur if there is too much current on one or more of the non-selected lines as there will be partial switching of the word at the intersection of this particular non-selected line and the selected line on the other coordinate. If the driving currents were adjusted for 410 ma of drive on each coordinate, then one line could have up to 20 ma of leakage current without affecting the disturbed word. This would leave 390 ma of drive for the selected line and as a result on the READ operation the ONE signals would peak later than normal because the cores received too little excitation. Since the STROBE pulse comes at a fixed time, reducing the drive would eventually cause ONE's to be read as ZERO's. Since there are 63 non-selected lines tied to the READ-WRITE bus, as little as 300 μamps on each line adds up to 20 ma

lost on the selected line. Whether or not a memory can operate with a 5% variation in the switching currents depends on the uniformity of cores and the operating margins in the sensing amplifiers, but 5% seems to be in line with present system limits. The most critical point comes when the READ-WRITE bus is of the opposite polarity from the base voltage. In the system being designed, the maximum is 26 volts. With larger memories this value increases proportionally so that for a 256 x 256 x 38 memory[31] the maximum voltage would be about 200 volts.

The above voltage and current ratings apply to the collector-to-base junction. The emitter-to-base junction has the constant V_{OFF} applied and as long as the voltage at the base remains at V_{OFF} the memory operation is not affected. Limits on I_{eo} will be based on the size of the power supply for V_{OFF} but a value of 150 μamps at 15 volts is consistent with the collector rating.

2.5.4 Collector Capacity

The collector capacitance has not yet been considered but it undoubtedly is very important. Besides varying with the junction area and the resistivity of the base material, the capacity also varies inversely as the square-root of the applied voltage.[32] In the above system the collector capacity will vary over at least a 3:1 ratio and analysis becomes difficult. The important quantity is the current on the selected line and for a given rise and fall time of this current, the voltage at the READ-WRITE bus is completely determined. If the current that this voltage causes to flow through the non-selected lines is added to the READ-WRITE current generators then the correct

current will flow on the selected line.

To get an idea of the magnitude of current involved, a collector capacitance of 50 μμfd will be assumed as the worst case. Referring to Fig. 1.5, the fastest voltage change that is taking place is about 10 volts per 0.1 μsec. This will cause 5 ma to flow through the above capacity and the generator would have to put out 315 ma for the OFF transistors alone.

The critical point in the operation occurs when the polarity of voltage is such that the junction potential on the OFF transistors is low for then the capacity is high. Any time that the junction voltage is decreasing and the generator current is increasing, the capacity is supplying current to the circuit and the current generators have less to supply. When the junction voltage increases the generators must supply more current or the current in the selected line will take longer to rise. When the current generators are turned off, the current must also be adjusted to prevent the capacity from determining the fall time of the current. It is general practice in the memories using vacuum-tube selection to place damping resistors across the selection lines to prevent ringing and this represents another current that the generator must supply.

The optimum voltage waveform at the selected line will be one in which all changes in voltage such that the junction capacity is being charged, take place slowly, and all changes that take place such that the capacity is discharging, take place quickly. This change will undoubtedly take place automatically due to the limitations of the current generators. The effect on the memory operation will be that the noise on the sensing

winding during the rise and fall of the currents will be higher in amplitude, but will be shorter in duration.

No definite limits will be placed on the capacity, but the area of the collector and emitter junctions should be kept as small as other factors will allow.

2.6 Summary:

The circuit must perform as follows:

A. Supply a minimum of 50 ma to turn on the transistor switch.

B. Maintain that current within the limits of 45 and 48 ma as long as that address is selected.

C. Supply a minimum of 100 ma peak reverse base current to turn off the transistor switch.

D. Hold all OFF transistor bases at +15 volts.

The transistor switch must have the following characteristics:

A. Alpha normal, $\alpha_n \geq 0.909$ with $I_c = 425$ ma.

B. Alpha inverted, $\alpha_I \geq 0.90$ with $I_c = 425$ ma.

C. Alpha cut-off freq, $f_n, \geq 6.7$ mc

D. Punch through voltage, $V_P \geq 15$ V.

E. Body breakdown voltage, collector junction, $V_{B_N} \geq 35$ V.

F. Body breakdown voltage, emitter junction, $V_{B_I} \geq 20$ V.

G. Collector saturation current, $I_{co} \leq 300$ μa at $V_c = 30$ V.

H. Emitter saturation current, $I_{eo} \leq 150$ μa at $V_e = 15$ V.

CHAPTER III

TRANSISTOR DESIGN

3.0 Introduction

When a circuit has been designed on paper there is always the problem of finding real components to perform the assigned tasks. Transistors do not differ much from vacuum tubes in this respect since for both devices the maximum power to be dissipated, maximum current, maximum voltage, maximum frequency of operation, and desired reliability must be fitted into existing devices. As with vacuum tubes,[33] there are theoretical relationships that enable the interested transistor designer[32] to determine if he is asking too much of the transistor or if it is merely technical difficulties that are holding back the necessary device. The transistor ratings will be discussed first and the design of a suitable transistor will be attempted.

3.1.0 Ratings of Transistors

Transistors have certain maximum ratings that must not be exceeded if the unit is to function properly; moreover, as opposed to vacuum tubes where the ratings may be exceeded for a short period of time with no immediate damage, the nature of the transistor is such that exceeding the maximum ratings even momentarily may result in catastrophic failure of the unit. It is, therefore, important to understand the nature and reason for the maximum ratings.

3.1.1 Maximum Power Dissipation

In the manufacturing process of alloyed-junction germanium transistors, one of the steps involves heating the transistor so that impurities diffuse into the block of germanium. The regions infected

with the impurities become the emitter and collector of the transistor. If the heating process continues too long, or if the transistor is re-heated due to over-dissipation in the circuit, the diffusion continues until the region between the emitter and collector (the base) ceases to exist, and the emitter-to-collector impedance decreases to a very low value. The unit is then said to have alloyed-through or punched-through and is no longer a transistor.

Unpublished life test data has shown that while units stored at 100°C remained in operating condition, units operated with internal dissipation to bring the junction temperature up to 100° and still have reverse bias on the collector junction, failed in a short time from the diffusion effect. The temperature and dissipation were quite a bit higher in the tests than the manufacturer's rating, however the tests point out the extreme undesirability of operating at elevated temperatures.

The maximum power rating should not let the temperature of the junction approach the point at which diffusion starts, and will be based on the thermal conductivity of the surrounding media. If one of the elements of the transistor is connected thermally to the case of the transistor, the dissipation can be increased; and if in addition the case is connected to a heat sink, the dissipation can be increased further.

In circuits that operate in the active region of the transistor with current flow and relatively high bias voltages, the dissipation at any point on the load line must be within the manufacturer's ratings. The junction temperature will then be below the maximum permissible value, and the circuit operation will be stable. In transistor-gate level amplifiers, where operation switches between high voltage with little current, and little voltage with high current, the load line may pass

through a region that exceeds the maximum dissipation. Due to the short time in this region, the average power dissipation will be small and must be less than the maximum rated dissipation. A condition may arise in which the transistor operation will move into the region of excessive dissipation by a process known as thermal runaway.[34,35] If the ambient temperature should increase, or if the sequence of circuit operations should happen to be such that the temperature of the junction increases, there will be an increase in the off condition current because the leakage current, I_{co}, in germanium, doubles for each 10°C increase in junction temperature. The increased current causes additional dissipation which increases the temperature. The temperature increase, in turn, increases the leakage current and also the heat carried away from the junction. When the heat carried away equals the total dissipation, then the temperature stops rising and a new stable point has been reached. It is possible that before a stable point is reached, the temperature of the junction will become high enough to cause permanent damage to the transistor. Transistors that might possibly operate close to the maximum dissipation rating should be provided with adequate heat sinks if stable operation is to be expected.

3.1.2 Maximum Current

The current gain of all transistors decreases at high currents, and so a limitation may be placed on the current in order to realize a usable gain at the maximum current and also to have a more uniform current gain from zero current to the upper limit.[36,37]

If the input current to a transistor is increased to the point where the external circuitry determines the output current, then the transistor is said to be in saturation. The impedance from the output

terminal of the transistor to ground will be low, and the voltage drop will be small. The maximum output current is that which causes the voltage drop across this impedance to increase the transistor dissipation to the maximum allowable value. This value of current will probably be higher for a particular unit than the published value, since the saturation voltage may vary from unit to unit, and the ratings are based on the highest expected value. Another limit that might be reached is the maximum current carrying capacity of the wire. It is common in low power transistors to make connections to the emitter and collector with wire a few mils in diameter, so that high current densities would result with fifty ma of current. The effect of the fine wire would also show up in the minimum impedance when the transistor is saturated.

The maximum current limit then appears to be less of an absolute maximum rating and more of a suggested maximum, although the physical construction of the transistor should be investigated before using very large currents.

3.1.3 Maximum Voltage Ratings

There are three phenomena involved in the maximum voltage ratings. These are discussed below.

3.1.3.1 Surface Effects[38]

The undesirable actions taking place on the surface of germanium are not well defined, contribute little to transistor operation and result in lower voltage ratings and perhaps shorter life of the transistors. In the interior of the transistor, atoms are arranged in a diamond lattice, and, except for the impurity atoms, all the covalent bonds are complete. At the surface the exact structure is quite complex, but there are strong forces due to the unsatisfied bonds in the crystal structure. In some

work performed at Philco Corporation for Lincoln Laboratory, it has been found that encapsulation in a medium containing dry oxygen prevented the surface of p type germanium from changing to n type. Water vapor has a very strong effect on the surface potential, and it accounts for the difficulties encountered in early transistors not hermetically sealed.

The anomalies generally observed when surface effects are present are sharp changes in the dynamic collector resistance before the breakdown voltage is reached. Hysteresis is often seen when the characteristics are displayed on an oscilloscope. The resistance along the surface is generally high, which accounts for the sharp change in collector resistance rather than a sudden change to zero or a gradual change. It has been observed that applying high voltage and current to some of the units that have poor characteristics at lower levels will cause the characteristics to resume a more normal position so that the anomalies are no longer observed. How permanent the change is is not known, but a heat cycle is a part of the manufacturing process of some, if not all, transistor manufacturers!

3.1.3.2 Punch-Through Effect[29,32]

When the collector-to-base junction is reverse biased, the potential is dropped across a volume in which all the minority carriers have been removed, leaving a space-charge region. The width of this region is determined by the density of impurities and by the applied voltage. An example of a pn junction reverse biased is shown in Fig. 3.1. If the region should become large enough so that the emitter-to-base junction is broached, then the emitter potential will follow any further increases in the collector potential. The voltage at which this occurs is known as the punch-through voltage, V_p, and if any higher potentials

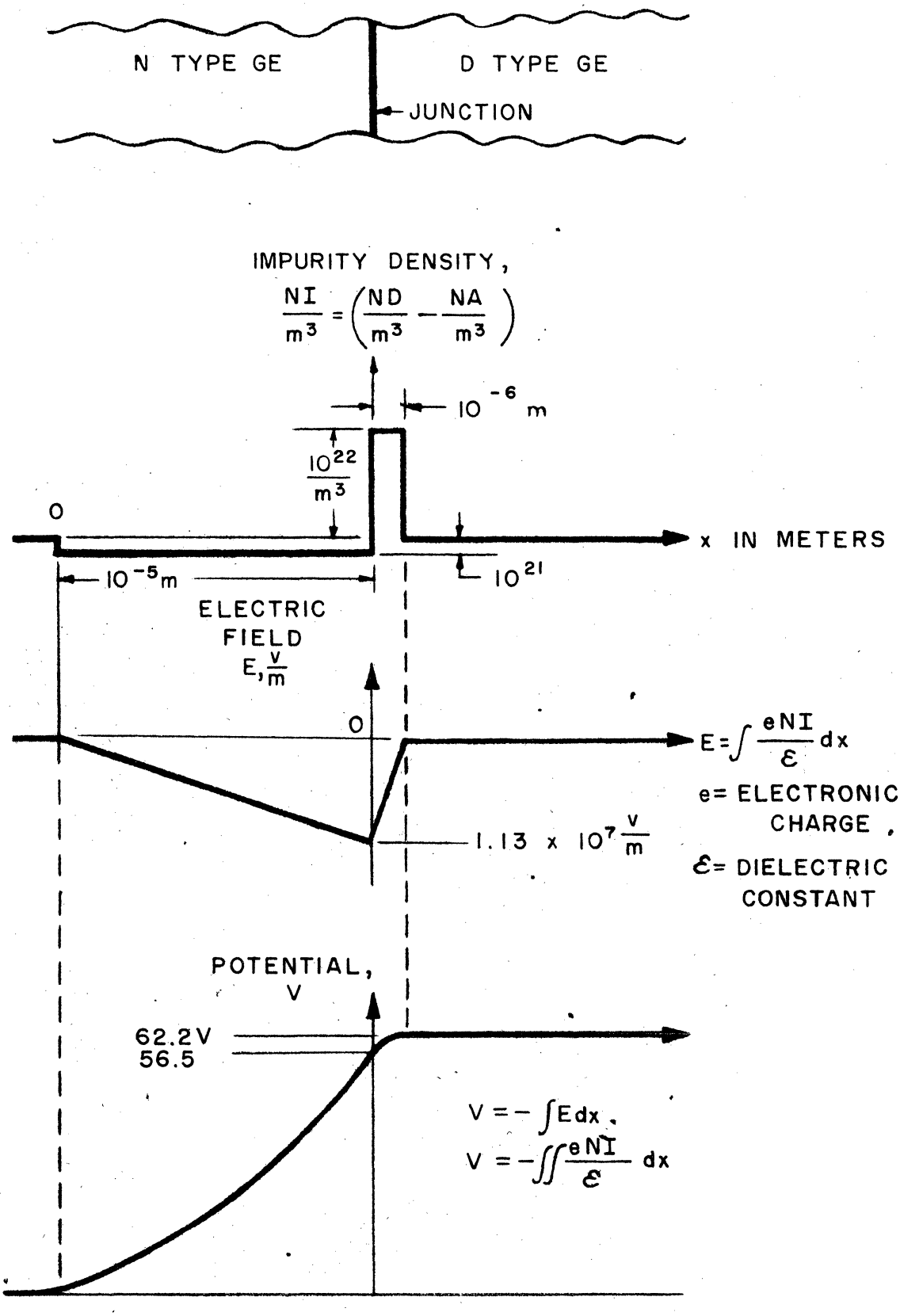

FIG. 3.1

PN JUNCTION POTENTIAL, ELECTRIC FIELD, AND IMPURITY DENSITY DIAGRAM

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are applied to the collector, the current will be determined by the external resistance in the emitter or collector.

An exception to this can occur if the emitter junction is also reverse biased. The space-charge region may then extend completely across the base and there will be no current flow until the difference between the emitter and collector bias voltage equals V_p. When the emitter is reverse biased, the field problem becomes three dimensional, as the space-charge region then extends past the edges of the emitter and collector junctions into the base tab. Although an analytic solution was not attempted, the surface in Fig. 3.2 indicates in a general manner the variation of potential across a section through the base, emitter, and collector. The two lowest edges represent the potential at the emitter and collector.

Fig. 3.3 shows a plot of emitter current vs. collector voltage for three cases: emitter with zero bias, emitter bias less than V_p, and emitter bias greater than V_p. A similar situation to the last case arises in the transistor gate in which the emitter has a large reverse bias. The collector potential varies about this same point, and from the above Fig. 3.3, the peak to peak collector swing could approach twice V_p if the emitter bias was equal to V_p. Here is a case in which the collector-to-base voltage exceeds V_p by a factor of almost two and circuit operation is normal. Note that the collector-to-emitter voltage is always less than V_p.

3.1.3.3 Avalanche Effect[28,32,39,40]

A carrier entering the space-charge region will be accelerated toward the opposite side of the junction, and it is possible that there may be collisions between the carrier and valence electrons. If the total

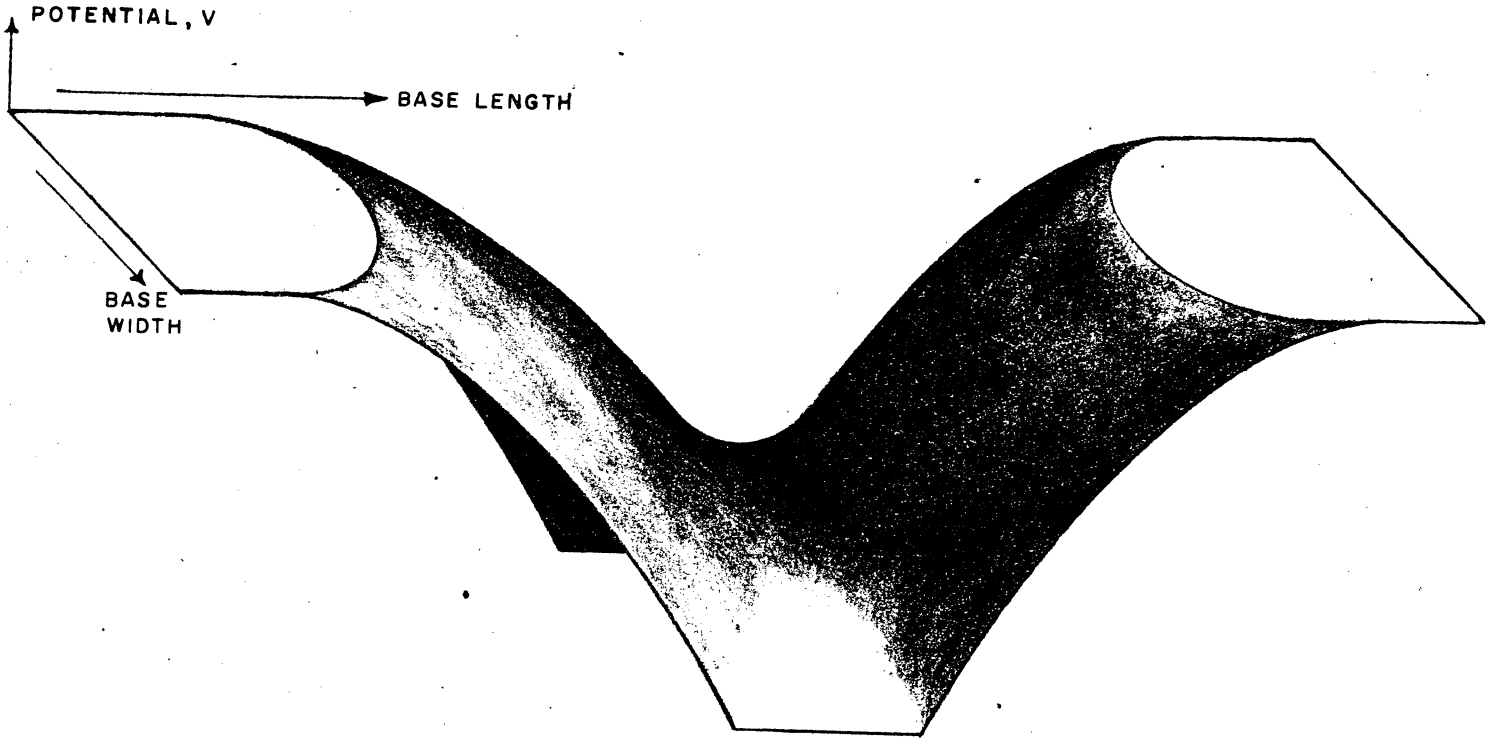

FIG. 3.2
POTENTIAL DIAGRAM FOR SECTION THROUGH EMITTER, BASE, & COLLECTOR WITH EMITTER & COLLECTOR REVERSE BIASED.

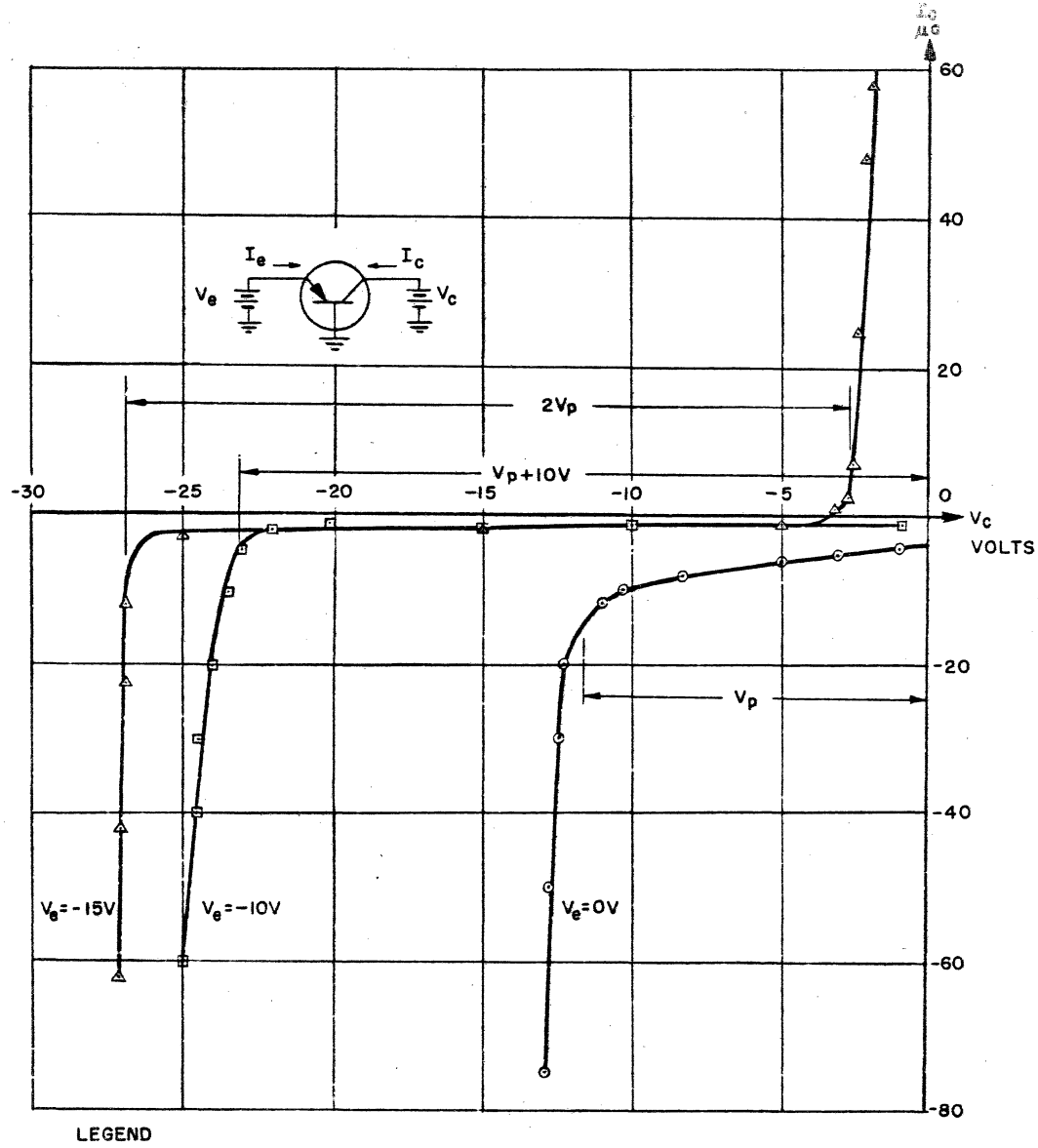

FIG. 3.3

PUNCH THROUGH EFFECT

potential drop is 10 volts and there are no collisions, the carrier will have an energy of 10 ev when it reaches the opposite side; however, the ionization energy of valence band electrons is only 0.75 ev and several may be produced by the original carrier. The low-voltage current-gain, α_0 , will be increased by this multiplication (M) at the collector junction, and the voltage at which $\alpha_0 M$ equals unity is the avalanche voltage (V_A). It is the maximum operating voltage if the transistor is operated grounded-emitter. A surface has been drawn in Fig. 3.4 that represents the variation of $\alpha_0 M$ with collector voltage and collector current. The plane α, M=1 is shown intersecting the surface and grounded-emitter operation must remain below this plane.

If the voltage is increased further, M will keep increasing until at the body breakdown voltage (V_B), M approaches infinity; this is the maximum grounded-base operating voltage. With a narrow base, the punch-through effect, rather than the avalanche effect, might be the limiting voltage rating for grounded-base or even for grounded-emitter operation, as is common in very-narrow-base surface-barrier transistors.

The applied voltage in a circuit must be lower than the breakdown voltage by at least a few volts. However, the transistor manufacturer must set the maximum ratings, such that the transistor with the lowest V_p, V_A or V_B will not fail with the stated voltage applied. Most of the units will have their breakdown voltages quite a bit higher than the ratings, and if a higher rating is desirable for a particular application, it is possible to select some units having higher ratings. The circuit designer prefers to work with stock items. Transistor selection means that the circuit design does not have a sufficiently wide margin of operation or that the manufacturer does not have complete control over the manufacturing process.

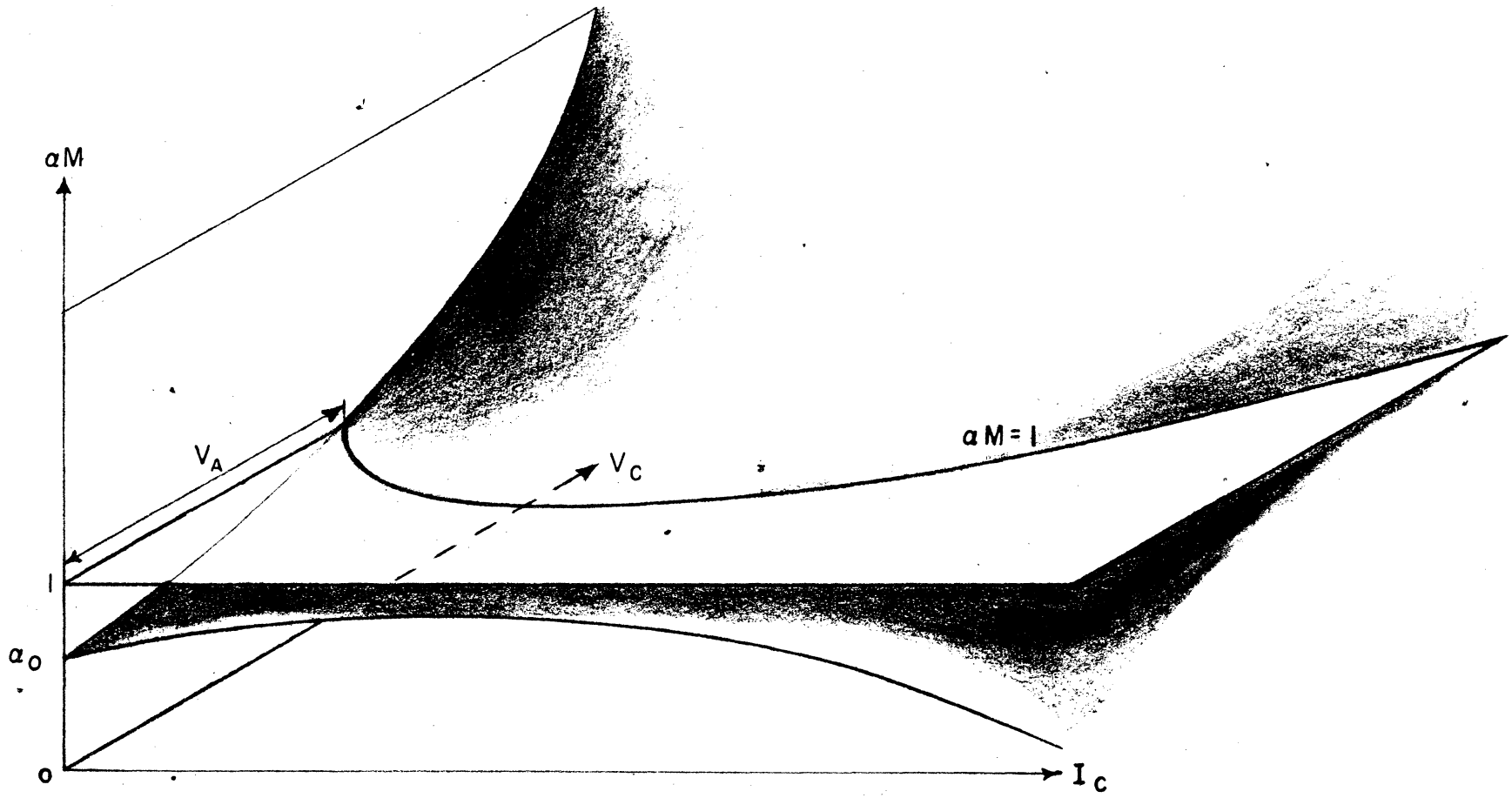

FIG. 3.4

VARIATION OF αM WITH V_C & I_C

3.2 Construction Limits

3.2.0 Introduction

There are several theoretical relationships that relate the maximum alpha, the minimum alpha cut off frequency, and the voltage ratings to the base resistivity (ρ_b) and base width (W_b). Ebers and Stevens have collected the latest data, and it is presented in an excellent manner in their paper.[32] The technique can be used to find a region in which satisfactory transistors can be produced, or to find out if a certain design requires a transistor that cannot be made with the alloy process. As mentioned in Sec. 3.1.3.1, surface effects may reduce the predicted maximum voltage ratings; therefore, the results of this section will only reflect the internal phenomenon of the transistor.

The variation in the d-c current gain,[36] $B=\frac{Ic}{Ib}\Big|_{Vce}$, from unit to unit and with increasing currents is unpredictable; however, at high currents there is less gain variation within a group of transistors than there is at lower currents. For example, a group of transistors had a current gain at 1 ma ranging from 26 to 100, while at 400 ma the variation was from 10 to 20. Using this as a guide, the high current alpha specification, $\alpha_n \geq 0.909$, can be translated into the range $0.95 \leq \alpha_n \leq 0.99$ at low collector currents. This allows P_b and W_b to be determined and does not represent a restriction on the α of the actual transistor. The α at the high currents does represent the restriction.

Although there is no way to relate surface phenomenon to body breakdown voltage (V_B, Sec. 3.1.3.3) and to avalanche voltage (V_A, Sec. 3.1.3.3) an analysis can be based on a value of V_A equal to the maximum emitter-to-collector voltage plus a safety factor. Twenty volts seem reasonable for this figure in view of the fact that the maximum emitter-

to-collector voltage is 11 volts, and the maximum base-to-collector voltage is 26 volts.

3.2.1 Maximum Base Width

Transistor action is based on the diffusion of minority carriers across the base region to the collector junction. A wider base (W_b) lengthens the diffusion time and reduces the alpha cut off frequency (f_n). The equation for f_n has been derived in several references[5,41] and is $f_n = \frac{D}{\pi W_b^2}$ (D is the diffusion coefficient). Because D varies slightly with resistivity, ρ, it has been plotted in Fig. 3.5 as A, where $f_n = \frac{A}{W_b^2}$, W_b is in mils and f_n is in mc, for both pnp and npn transistors. The approximate 2:1 ratio between the curves follows from the 2:1 ratio in the mobility of electrons and holes.[42]

Using the relation $W_b = \sqrt{\frac{A}{f_n}}$ with f_n equal to the minimum value given in section 2.5.2, (6.7 mc) and using the curves in Fig. 3.5 for A, the maximum base width vs. base resistivity has been plotted in Fig. 3.6 for pnp and in Fig. 3.7 for npn germanium transistors.

3.2.2 Minimum Base Resistivity

The reverse current of a pn junction is relatively constant at I_s, the saturation current, as the bias is varied from a few tenths of a volt to the body breakdown voltage, V_B. The body breakdown is an avalanche process[28] in which carriers multiply in a manner analogous to ionization in a Townsend gaseous discharge. The value of the breakdown voltage is determined by the region having the smaller space charge density, and as a result most of the potential drop is as shown in Fig. 3.1. This sketch is exaggerated in that the high impurity region may have 10^4 more impurity centers (NI) than the low impurity-center region, rather than 10^1 as indicated. There is a 2:1 ratio in NI between p and n type material

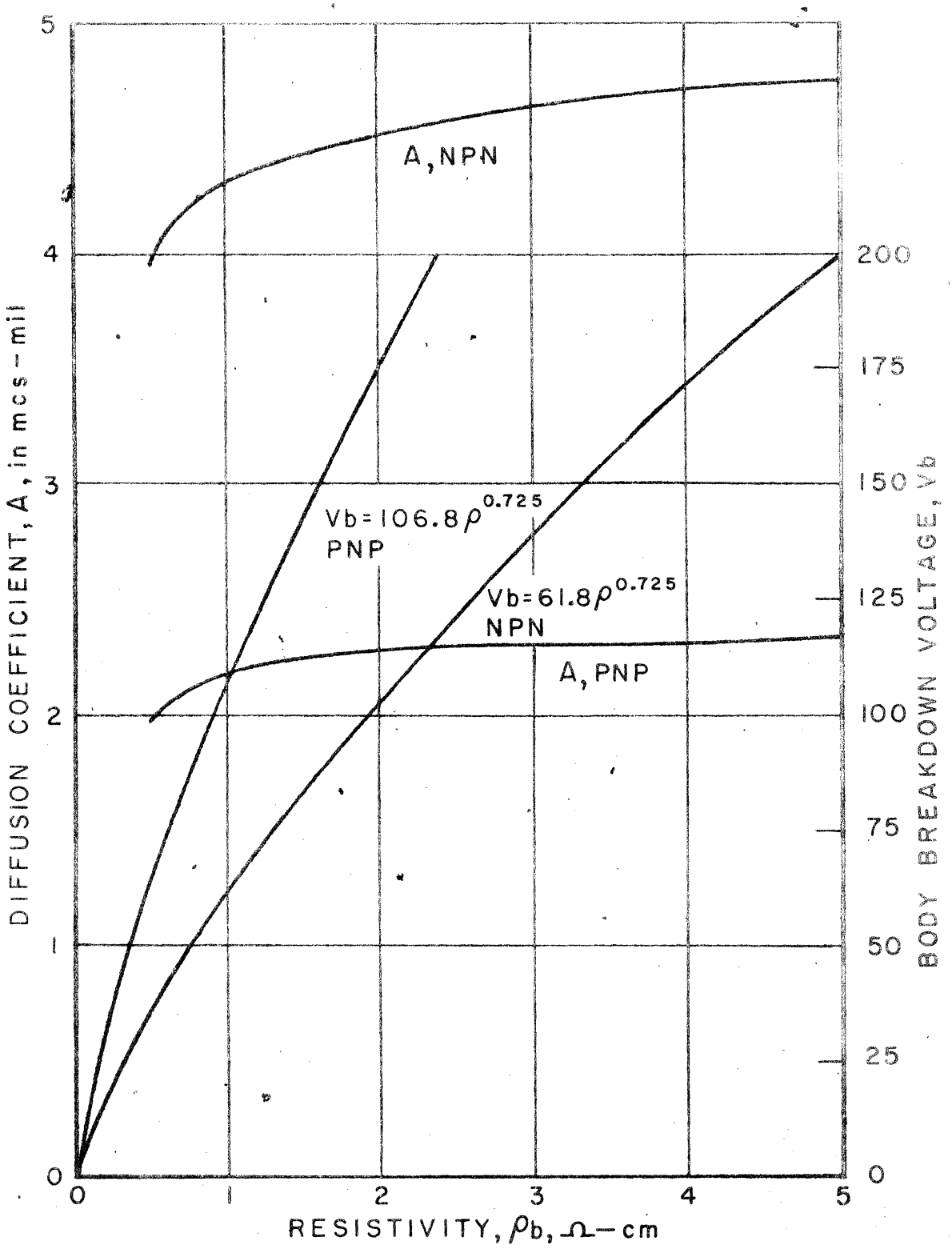

FIG. 3.5

DIFFUSION COEFFICIENT AND BODY BREAKDOWN VOLTAGE VS BASE RESISTIVITY FOR GERMANIUM

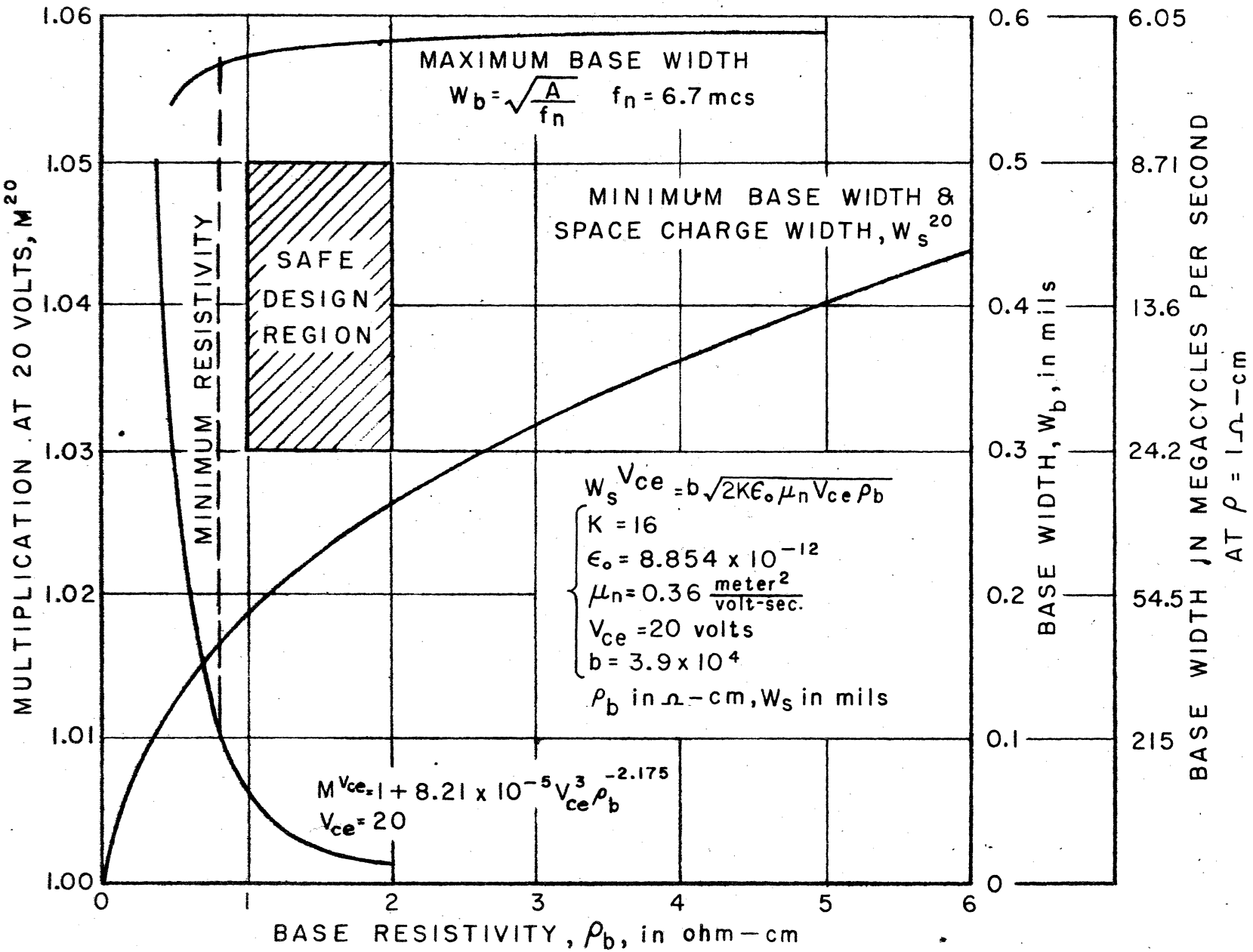

FIG. 3.6

LIMITS ON BASE RESISTIVITY AND BASE WIDTH FOR PNP GERMANIUM TR[illegible]

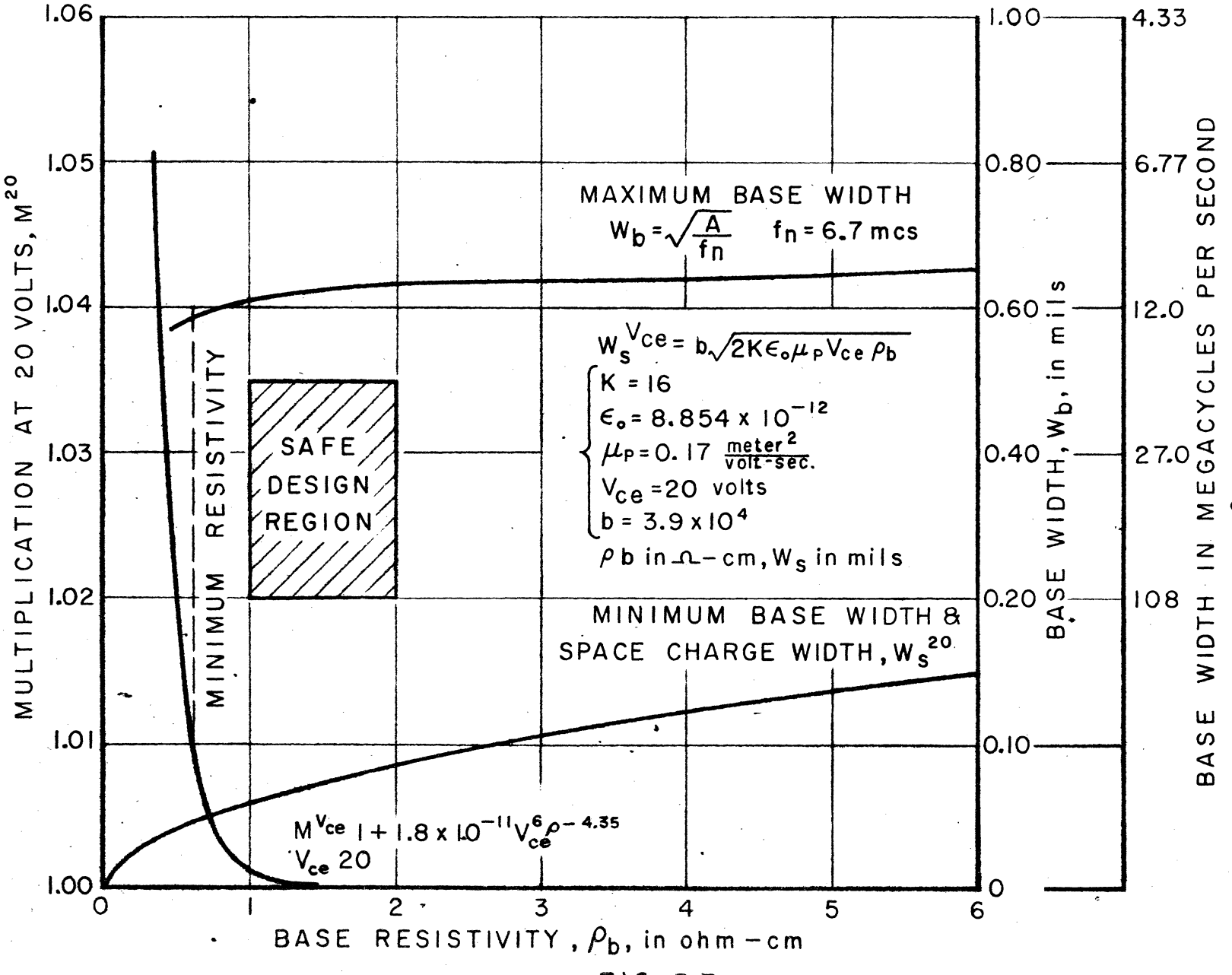

FIG. 3.7

LIMITS ON BASE RESISTIVITY AND BASE WIDTH FOR NPN GERMANIUM TRANSISTORS

having the same resistivity; however, the base NI is always much lower than either the collector or emitter NI in alloyed-junction germanium transistors, so that most of the potential drop takes place in the base region, independent of whether the transistor is pnp or npn.

S. L. Miller[28] has found that in germanium $V_B = 1.14 \times 10^{13} (NI)^{-0.725}$. The relation between NI and ρ is $NI = \frac{1}{eu\rho}$, where e is the electronic charge and u is the majority carrier mobility. For n type germanium this becomes $NI = 1.6 \times 10^{15} \rho^{-1}$, and for p type germanium it is $NI = 3.4 \times 10^{15} \rho^{-1}$ when the proper values are substituted in the equation p is in Ωcm. These two relationships lead to $V_B = 106.8\rho^{0.725}$ for n type germanium and $V_B = 61.8\rho^{0.725}$ for p type germanium.

Miller also derived the relationship that $M^V = \frac{1}{1-(\frac{V}{VB})^n}$ from experimental data in which M^V is the multiplication at the junction with V volts applied, and n depends on the type of material on the high resistivity side of the junction. Using the above equations for V_B and making the approximation $M^V = 1+(\frac{V}{V_B})^n$ produces $M^V = 1+8.21 \times 10^{-5} V^3 \rho^{-2.175}$ for n type germanium (n=3) and $M^V = 1 = 1.8 \times 10^{-11} V^6 \rho^{-4.35}$ for p type germanium (n=6). These two expressions are plotted in Figs. 3.6 and 3.7 for V equal to 20 volts. The exponent n is not well defined because Miller has listed only seven points for which n was determined. The values used were those he found at $\rho_b = 2\Omega$-cm.

To use the curves, the maximum value of α must be known since avalanche occurs when αM goes to unity or $M = \frac{1}{\alpha}$. For a given value of M, the value of ρ_b can be found that will produce this multiplication with the application of the specified maximum voltage. A lower value of ρ_b produces a higher M so that this point determines the minimum resistivity of the base region. With a maximum α of 0.99, M cannot exceed 1.01.

The minimum value of ρ_b corresponding to this value of M and a voltage of twenty volts is, from Fig. 3.6, 0.84Ω-cm for n type germanium (pnp transistor) and, from Fig. 3.7, 0.61Ω-cm for p type germanium (npn transistor). In each case a value of ρ_b larger than these values is satisfactory as far as the avalanche voltage rating is concerned.

3.2.3 Minimum Base Width and Maximum Resistivity

As was discussed in Section 3.1.3.2, applying a voltage between collector and either the base or the emitter so as to reverse bias the collector junction results in a decrease in the space-charge-free region of the base between the collector and emitter. Corresponding to a maximum collector-to-emitter voltage, V_{ce}, and a certain base resistivity, ρ_b, the space charge region will extend into the base a distance, W_{sc} which is equal to $\sqrt{2K\varepsilon_o\rho_b\mu V_{ce}}$ where $K\varepsilon_o$ is the dielectric constant. For a pnp germanium transistor this reduces to $W_{sc}=3.98 \times 10^{-2}\sqrt{\rho_b V_{ce}}$, and for an npn germanium transistor $W_{sc}=2.73 \times 10^{-2}\sqrt{\rho_b V_{ce}}$, ρ in Ω-cm, V in volts in each equation. With V_{ce} equal to 20 volts, the two curves are plotted in Figs. 3.6 and 3.7. The curves represent the maximum width of the space-charge region with the given V_{ce}. The minimum base width, W_b, must be greater than shown on this curve at any value of ρ_b.

3.2.4 Design Center

From the information as plotted in Fig. 3.6 and Fig. 3. 7, it is evident that design restrictions are less severe for an npn transistor than for a pnp transistor. In either case, the possible region of operation appears broader than is necessary for the present application. Several other factors which have not yet been considered will indicate the most desirable region.

When the equation for the variation of current gain with

increasing current is expressed in terms of W_b and ρ_b,[36] it turns out to be desirable to keep the base width as small as possible and the base resistivity as high as possible. However, a high resistivity would contribute to an increased power dissipation in the region between the junctions and the external base lead. Part of the problem then must be resolved by the transistor designer who can exchange low dissipation for a higher base resistivity in order to prevent the high current gain from decreasing too severely.

The V_p rating of the transistor determines the absolute minimum W_b. For if the space-charge region at the collector-to-base junction extends to the closest point of the emitter-to-base junction, the transistor will cease to function properly. The minimum f_n determines the maximum W_b, but if all of the diffusion paths are not the same length, the average rather than the minimum W_b will determine f_n. If the junction is not flat, the average W_b might be twice the minimum,[29] and the danger of punch through will be higher or f_n will be lower than with a flat junction.

With jet etching techniques,[43] flat junctions only a few tenths of a mil thick can be produced with good control of the actual spacing. Large area junctions have not been produced by this method although there seems to be no fundamental reason why the technique cannot be similarly applied. Jet etching appears to be the only reliable technique commercially available for producing narrow base pnp transistors. An associated problem is designing the junction shape so that the center portion of the transistor is not biased into cut off by a concentration of current on the edge of the junction. A higher base resistivity would tend to make this condition more critical, but there are some construction techniques that avoid this trouble entirely.[44]

Although there could be some changes in the actual ρ_b and W_b, the regions marked off in Fig. 3.6 and in Fig. 3.7 are satisfactory for meeting the requirements of V_p, V_A and f_n. For a pnp the region is as follows:

$$1 \leq \rho_b \leq 2 \Omega\text{-cm} ,$$

$$0.3 \leq W_b \leq 0.5 \text{ mils}.$$

For a npn transistor:

$$1 \leq \rho_b \leq 2 \Omega\text{-cm} ,$$

$$0.2 \leq W_b \leq 0.5 \text{ mils}.$$

CHAPTER IV

TRANSISTOR-GATE LEVEL AMPLIFIER

4.0 Introduction

The characteristics of the transistor gate must be known before its level amplifier can be designed; nevertheless, the design of the transistor is influenced greatly by the ability of the level amplifier to turn the transistor-gate on and off in short intervals of time. The values of base current specified in Sec. 2.4 were based on experience with early experimental level amplifiers and also with transistors that did not qualify for the gating operation because of one fault or another. Larger amplitudes of current could be produced but they are not necessary if the transistor can be built to the specifications in Sec. 3.2.

A design of a transistor-gate level amplifier is included in the next few sections beginning with the output from a memory-address-register and including the necessary signal to the input of the transistor-gate.

4.1 Memory Address Register[45]

A transistor memory address register (MAR) has been in operation for some time at Lincoln Laboratory utilizing the surface barrier transistor for high speed operation. The circuit for one flip-flop is shown in Fig. 4.1 and there will be as many flip-flops in the MAR as there are binary numbers in the address of the word in the memory, i.e. 2^n selection lines require n flip-flops.

Each flip-flop has two output lines, one being high when the other is low. One state corresponds to a ZERO address and the opposite to a ONE address. When an output line is in the low state, an emitter

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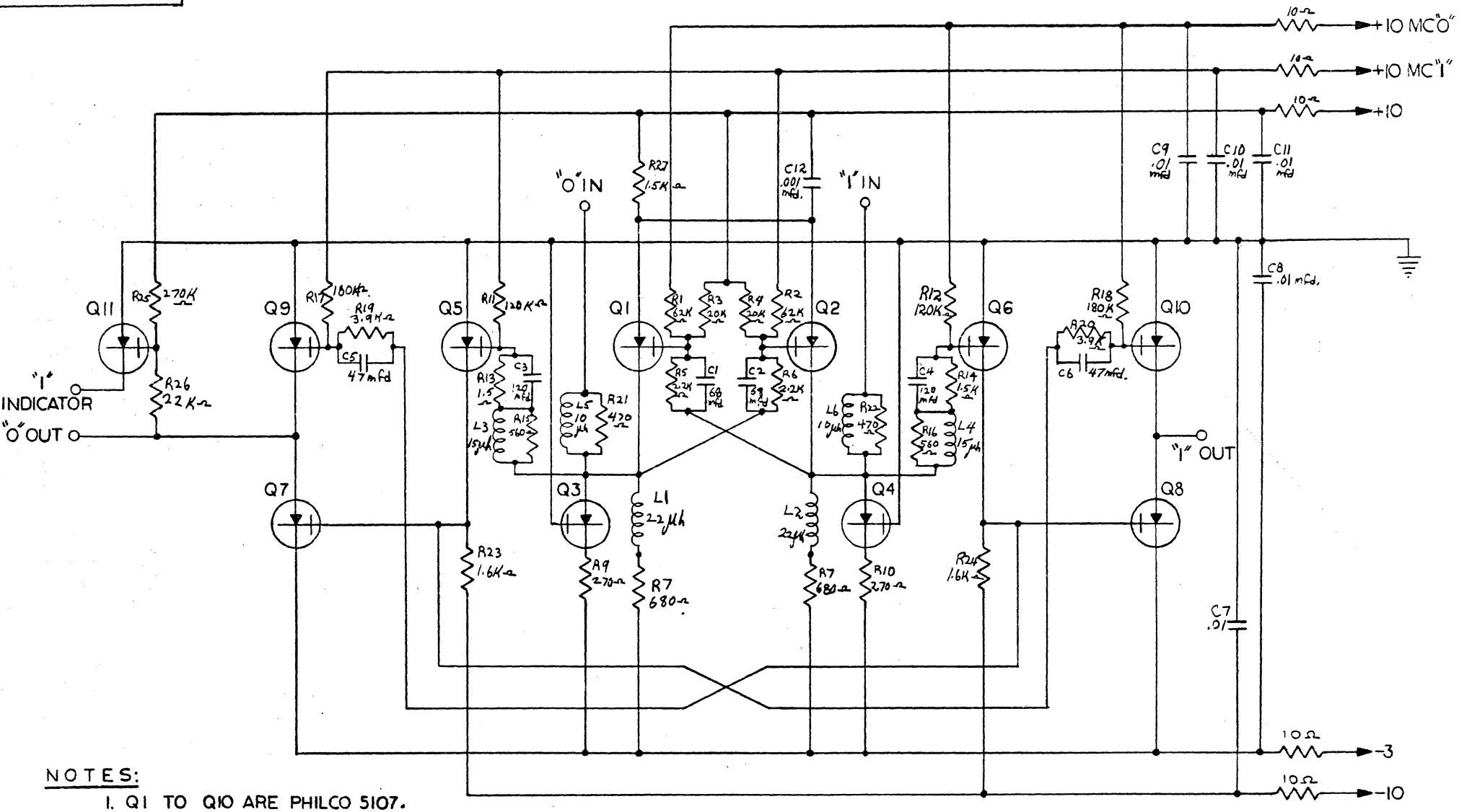

NOTES:

1. Q1 TO Q10 ARE PHILCO 5107.
2. Q11 IS GE 2N43A.

FIG. 4.1

EXPERIMENTAL FLIP FLOP, B

ENG. B. Gurley 12-30-55

DR. MLSTORM 12-30-55

follower (Q_8) clamps the voltage to the -3 volt supply. The output impedance in this case is very low. When a line switches to the high state, a saturated grounded-emitter (Q_{10}) clamps the output line to ground. This in itself is not enough to cause fast switching in subsequent stages but the technique of positive bias[46] can be used to give a swing to a positive voltage instead of to zero voltage.

4.2.0 Transistor Matrix

There are several ways[47] of obtaining the desired output signal from the input levels, the only necessary item is a device to encode the binary inputs to a single level output. A resistance matrix[48] is impractical for any appreciable number of input lines and, as a result, the diode matrix[16,49] has been the main encoding device used in digital computers. The diode matrix must operate with large swings in voltage to make the one-half to one volt forward-current voltage-drop across the diodes appear small when compared to the total voltage swing. If the low levels from the MAR were amplified, a diode matrix would suffice, but it seems desirable to construct a transistor matrix wherein the amplification can take place at the same time the encoding process is being formed.

P. J. Griffith has developed several transistor-matrix circuits in preparation[47] for a Master's thesis at the Massachusetts Institute of Technology and the circuit using the least number of transistors is described below. Once the logical operation has been determined from the available circuits, the circuit designer must determine which devices and components to use to perform the required operation. This has been done in the second section for the case of a pnp transistor-gate. If the transistor-gate had been an npn transistor, the output voltage swing would

have been different but the input the same. The inverter, described below, would be on the opposite control lines.

4.2.1 Transistor-Matrix Logical Operation

If the address of the memory is an m-bit binary word, the input to X coordinate selection system will be a $\frac{m}{2}$ = n-bit binary word. (The Y coordinate selection system is a duplicate of the X system from this point on). The two level outputs of the flip-flop described in Sec. 4.1 are the n inputs to a system described by Griffith[†] and shown in Fig. 4.2. The n inputs are divided into two groups of $\frac{n}{2}$ pairs of lines, and each group is fed into a set of OR gates. The property of an OR gate in this application is that the output is low if any of its $\frac{n}{2}$ input lines is low, (but due to the inversion of the grounded-emitter stage, the output is high if either input line is low). The inputs in Fig. 4.2 are the vertical lines from the MAR to the bases of the transistors labeled Q_1 and Q_2. The output lines are from the collectors of the same two groups of transistors. One output line in each group will be at a low level and the other $2^{\frac{n}{2}} - 1$ lines will be at a high level.

The information from the two OR gates is now fed to an AND gate[9]. The AND gate is characterized by the fact that the output is low when (for an npn transistor) the base is high and the emitter is low. Under all other conditions it is high. Only one of the n^2 base lines on the Q_4 transistors should be high at a given time. At the intersection of this line with the one low emitter line is the selected AND gate with its low output. All the other $2^n - 1$ AND gates will have high outputs. Since

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† Private communication.

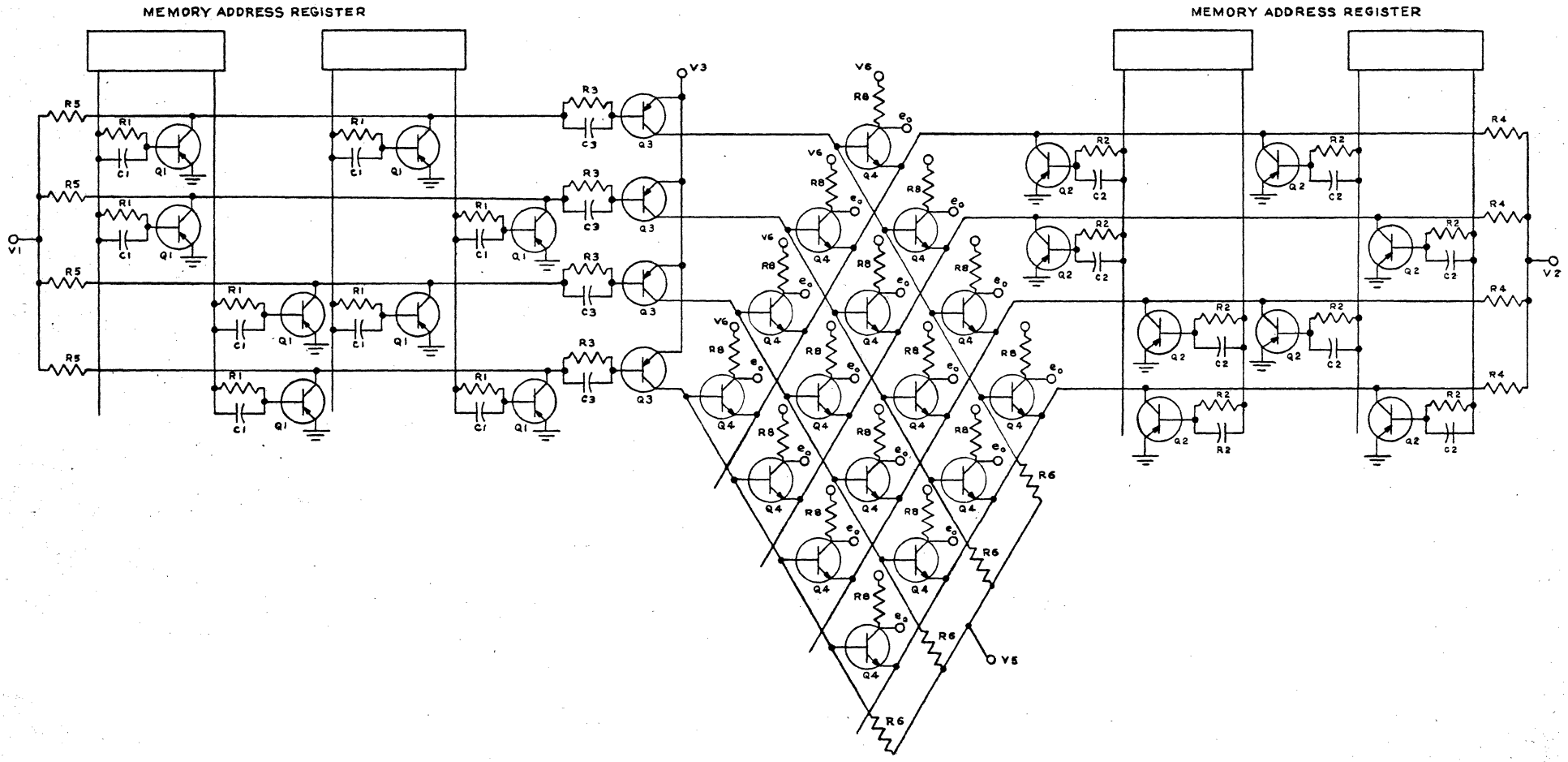


FIG. 4.2

TRANSISTOR MATRIX

the output of the OR gate is one low line and all the other lines high, it is of the correct polarity to drive the emitters of the AND gates. The signal from the OR gates to the bases must be inverted to keep one line high and all the other lines low.

4.2.2 Transistor-Matrix Design

The matrix described above is logically designed for the polarity of output necessary to drive the transistor-gate. The actual value of that voltage swing will be controlled by the matrix, and so a knowledge of the signal desired at the transistor-gate is necessary before the matrix design can proceed. The positive voltage has been specified in Sec. 2.4 as $V_{OFF} = +15v$. The negative value of the base voltage may vary slightly from unit to unit, but the important parameter is the base current which should be kept very close to the design value (45-48 ma); for this reason, a current source is desirable in the base circuit. The input voltage swing will be negative and the current can be adjusted by selecting the correct value of resistance. The larger this voltage, the more independent of variations in transistors will be the base current; however, the necessary voltage ratings on the preceding transistors becomes prohibitively high. It is desired to control the base current to within 5 per cent with an expected variation in base voltage of 0.4 V to 0.6 V. A resistor connected to a 4.5 volt supply will give about a 5 per cent variation in current with the given variation in base voltage and this value of supply voltage does not increase transistor ratings excessively. The desired output swing is from + 15 V to - 4.5 V.

The value of current in Q_2 must be determined from a knowledge of the expected variation in current gain of Q_2, the maximum current rating of Q_2, and the maximum allowable base drive to Q_2. The transistor used for Q_2, the 2N136, has no specified range of current gain, but a test of 29 transistors at 1 ma of collector current produced 18 units that had a grounded emitter current gain, B, in the range from 30 to 60. The maximum current rating is 50 ma, but a collector current of 20 ma will be used here because of the limited drive available. At 20 ma, 24 of the transistors had B's in the range from 20 to 47. It is found, therefore, that the minimum base current, Ib, is 1 ma. The current flow through R_2 is greater than this by the value of the positive bias, Ib_2. The greater Ib_2, the shorter the turn-off time of the transistor; however, this additional current must be supplied by the input line during the ON time. A value of Ib_2 equal to Ib_1 will be used so that the desired overshoot on the turn-on will not exceed the maximum allowable current of 5 ma per input line. The positive bias resistors are not shown in Fig. 4.2 but they are connected from a positive voltage supply to the bases of the Q_2 transistors. A 15 KΩ resistor going to + 15 volts will supply the necessary 1 ma of current. The base-to-emitter voltage, V_{be}, is not zero during the time the transistor is turned on and, therefore, the 3 volt input signal is not entirely dropped across R_2. A maximum V_{be} of 0.6 volts is conservative since for most transistors the voltage is in the range of 0.3 to 0.4 volts[50]. The 2 ma of current will drop 2.4 volts across an R_2 of 12 KΩ.

To avoid pulse-repetition-rate (prf) sensitivity, the R_2C_2 time constant will be selected as approximately 0.1 μsec. If C_2 is

100 μμf, the time constant is equal to, or less than, 0.12 μsec. However, hole storage may drain much of the charge, and the capacitor may have to be increased if the turn-off time is too long.

The values of R_4 and V_2 are partially defined by the choice of collector current in Q_2, however, a Q_4 transistor exhibits emitter follower action when turned on so that its emitter voltage is equal to V_3. V_3 is determined in part by the desired low output level, - 4.5 volts. However, it is necessary to clamp the output, e_o, to - 4.5 volts in order to prevent Q_4 from going into saturation and, as a result, V_3 will be slightly lower,-- -6 volts. The emitter current of Q_4 remains to be defined. It must be less than the collector current of Q_2 so that the voltage at the emitter can fall from zero to V_3 when Q_2 is turned off. The collector current of Q_4 is slightly less than the emitter current and should be as large as possible to produce fast switching. An emitter current of 10 ma is consistent will all the requirements and results in a V_2 of - 12 volts and an R_4 of 600Ω. If a higher current had been desired both V_2 and R_4 would be larger so that the supply would approach a current source. During the transient state, the voltage at the emitter of Q_4 starts falling to V_2, and if V_2 is very large the voltage at the collector of the OFF Q_2 transistors might exceed their maximum ratings.

At the selected transistor in the Q_4 array, the base and emitter are at approximately - 4.5 volts and 10 ma is flowing out of the emitter. The collector voltage, V_6, has been defined by specifying V_{OFF}; it is + 15 volts. The variation in current gain is greater in Q_4, a 2N94A, than it was in Q_2. Even at 100 ma of collector current the gain

varied from 33 to 71 for the ten transistors tested. At 1 ma of collector current the variation in gain was from 31 to 100; thus, a minimum gain of 30 will be used to determine R_8. It is very important that the output voltage of all the Q_4's be at the clamping voltage of the diode because this voltage determines the base current of the transistor-gate. To insure adequate clamping, the collector voltage should fall to -6 volts with the clamping diode disconnected. With a minimum gain of 30 and an emitter current of 10 ma the minimum collector current will be 9.7 ma. R_8 is, therefore, $\frac{15 + 6}{9.7} = 2.16 \cong 2.2$ KΩ.

R_6 is the load for Q_3 and also serves as the path to V_5 for the turn-off current of Q_4. Since the emitter voltages of the Q_4 transistors, in the steady stage condition, are always at -6 volts or at zero volts, the base must be below -6 volts. The -12 volt supply will be used for V_5 since it is available and the result is a net collector-to-emitter supply voltage of -6 volts for Q_3. The maximum reverse base current of Q_4 is approximately the same as the collector current of Q_3 if the emitter voltage of Q_4 remains constant and just one of the lines coming from the Q_3 transistors is shifted. If both Q_3 and the emitter of Q_4 shift at the same time the maximum reverse current will be $\frac{V5}{R6}$ and a more rapid turn-off time will result. The more critical case is when Q_3 is shut off and the emitter of Q_4 remains at -6 volts. To insure fast turn-off in the latter case (because shunting with capacity is impossible) the maximum reverse base current will be specified as 10 ma. R_6 is then $\frac{6}{10} = 0.6$ KΩ.

The inverter stage, Q_3, will also use 2N136 transistors and if the current gain is again assumed to vary from 20 to 47, a minimum base current of 0.5 ma will be required. The emitter is now at -6 volts and

the collector supply voltage of Q_1 must be more negative in order to draw base current from Q_3, so the -12 volt supply will be used. Although it would be possible to short out R_3 and C_3, R_5 would then have to be large to determine the base current of Q_3. The turn-on time of Q_3 would, however, then be limited by the collector capacity. Faster switching can be obtained by specifying the collector current of Q_1 to be 10 ma. R_5 is $\frac{12}{10} = 1.2$ KΩ.

The total base resistance required for Q_3 is $\frac{6}{0.5} = 12$ KΩ. R_3 must be 12 - 1.2 = 10.8 K, a nominal value of 10 KΩ will suffice. The maximum reverse base current of Q_3 is only 0.6 ma, therefore, shunting R_3 with a capacitor, C_3, of 10 $\mu\mu$fd gives a time constant of 0.1 μsec., which will shorten switching time.

In Q_1 (a 2N136 transistor) with a collector current of 10 ma, a base current of 0.5 ma is required. As was done for Q_2, positive bias will be used to shorten the turn-off time. Because the ON base current was 0.5 ma, a maximum reverse base current of the same value will be demanded. If the positive bias is taken from the + 15 volt supply the resistor will be 30 KΩ. R_1 now carries 1 ma, and with 2.4 volts across it, has a value of 2.4 KΩ. C_1 can be 40 $\mu\mu$fd in order to retain the 0.1 μsec time contstant.

4.2.3 Summary of Components Required for Transistor Matrix

Following the notation in Fig. 4.2 the components are:

Q_1, Q_2, Q_3	2N136 (pnp)
Q_4	2N94A (npn)
R_1	2.4 KΩ
R_2	1.2 KΩ

R_3	10 K Ω
R_4	600 Ω
R_5	1.2 K Ω
R_6	600 Ω
Positive Bias Resistor to Q_1	30 K Ω
Positive Bias Resistor to Q_2	15 K Ω
V_1, V_2, V_5	- 12 v
V_3	- 6 v
V_6, Positive Bias Supply	+ 15 v
Diode Clamp Voltage	- 4.5 v

4.3 Complementary Symmetry

The signal at the output of the matrix has the necessary voltage swing, but the current levels are not high enough to drive the transistor-gate. As opposed to the above matrix where the transistors were not heavily in saturation, the transistor-gate will be driven heavily into saturation when the matrix levels change. Reverse base currents on the order of 100 ma will be required to turn the transistor-gate off, and if this is supplied by the positive bias method,[46] the imput drive to turn the transistor on will be 50 ma plus the 100 ma of positive bias.

The technique of complementary symmetry[23, 51] allows the requirement of a large reverse base-current to be satisfied; and, at the same time, the input current is only that which is required for the base of the transistor-gate. In Fig. 4.3 is an early model of the transistor-gate level amplifier that did not use selection at the base of Q_2 (which is equivalent to Q_4 in Fig. 4.2). The swing at the collector of Q_2 is the same as the swing at e_o in Fig. 4.2. Referring again to Fig. 4.3, the collector voltage of Q_2 is applied to the bases of the first stage of

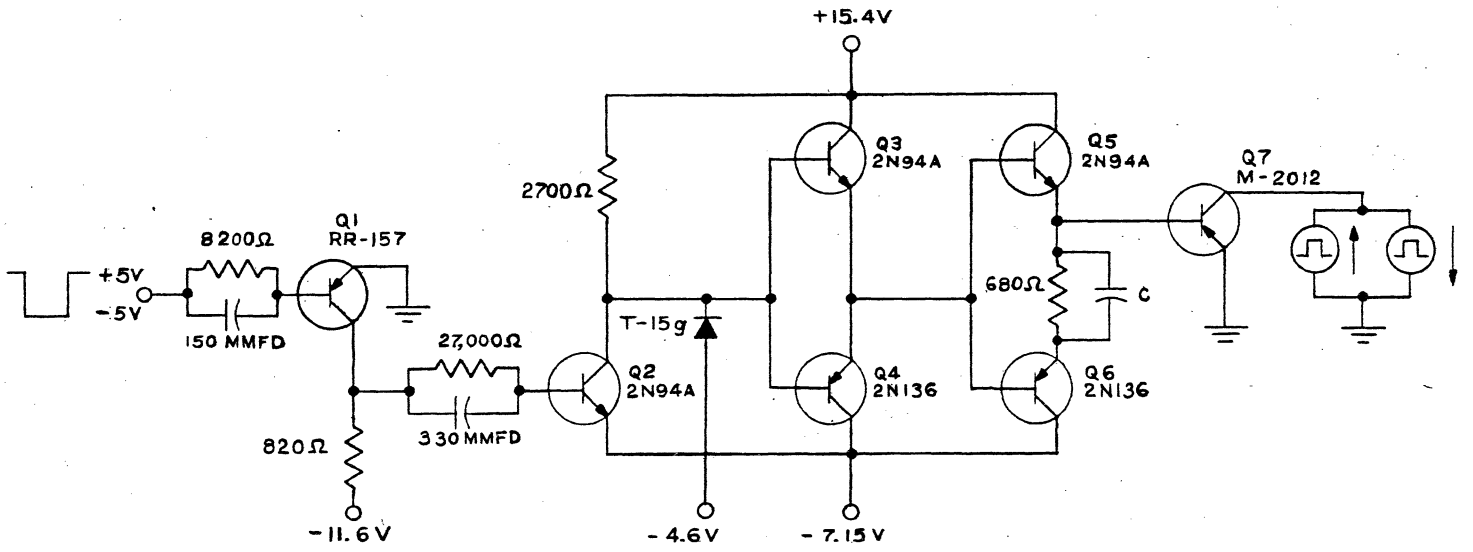


FIG. 4.3

EXPERIMENTAL TRANSISTOR-GATE
LEVEL AMPLIFIER

complementary-symmetry circuitry. When the base voltage of Q_4 is at the high level (corresponding to Q_2 being turned off) its emitter is at a lower potential than the base, and the transistor is turned off. The collector and base of Q_3 are at the same potential, and the emitter is slightly negative with respect to either of them. The only current flowing in this circuit will be a few microamps of leakage current from Q_6. As a result, the emitter of Q_3 will be practically at the base potential. The same now holds true for Q_5 as the only collector current is the leakage current of Q_7.

The emitter of Q_6 is slightly reverse-biased by the drop from base to emitter of Q_5, and the only current flow is the base-to-collector leakage current.

When Q_2 goes on, the base of Q_3 falls below the emitter potential, and as a result, Q_3 is turned off during the transient state (except for leakage currents). As the base of Q_4 falls, the emitter is forward biased by an amount equal to the difference between the fall of the base and emitter voltages. Although the frequency response of the grounded collector circuit is lower than f_n, the base currents can be high during the transient and this results in a short turn-on time.

Q_5 is reverse biased in the same manner as Q_3, and does not enter into the operation of the circuit during the turn-on transient. The operations of Q_6 and Q_4 are similar, and until the emitter voltage reaches ground potential, the main load on the emitter of Q_6 is the collector capacity of Q_7. The emitter-to-base diode of Q_7 then becomes conductive and clamps the base of Q_7 to approximately ground potential. Any further decrease in the base voltage of Q_6 leads to a large emitter current until capacitor C charges. The initial charging current of C helps to turn on

Q_7 by providing an overshoot in the base current. The base current of Q_6 appears as emitter current of Q_4; and the base current necessary in Q_4 to produce the charging of C will be small. Thus the fall time of the collector voltage of Q_2 will not be limited by the current in Q_4 and Q_6.

When the voltage at the collector of Q_2 reaches -4.6 volts, (the particular battery voltage measured in the experimental setup) the diode begins to conduct and prevents the voltage from decreasing any more than a few tenths of a volt. The emitter of Q_4 will fall to a potential slightly above the base potential, and the emitter of Q_6 will also be a few tenths of a volt above its base potential. The base current in Q_7 is determined by the 680Ω resistor and the emitter voltage of Q_6. Approximately 6 ma of base current was measured in the circuit and the ON base current of Q_6 was less than 200 μ amp.

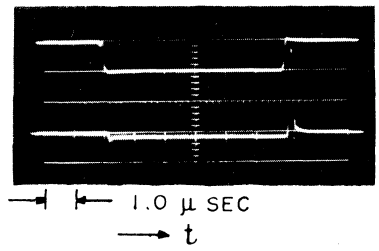
The only unit that will have hole-storage effects other than the transistor-gate, Q_7, is the diode, but fast switching diodes[25] have less hole storage than the transistors if allowed to saturate.

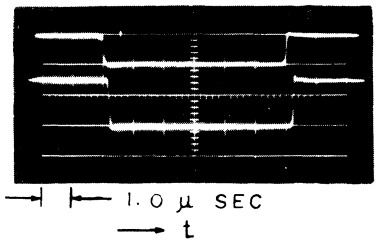
When the base of Q_2 is turned off, the collector current goes to zero before much happens in the circuit. The 7.4 ma that had been flowing through the 2.7 KΩ resistor now flows into the diode since it remains a low impedance until all the stored carriers have been removed. During this time Q_4, Q_6, and Q_7 remain conducting. In Fig. 4.4 the base current of the transistor-gate begins to decrease almost as soon as the input signal is changed, indicating that hole-storage is very small in the diode.

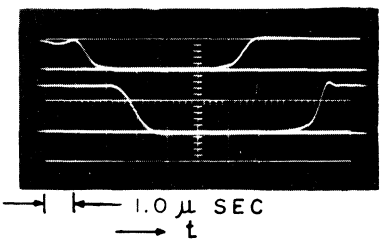
As the voltage at the collector of Q_2 rises, Q_3 and Q_5 are forward biased, and Q_4 and Q_6 are turned off. The base current of Q_3 starts out at 7.4 ma, but as the base voltage rises, the current decreases.

The base voltage rises until it reaches zero potential, then Q_7 becomes a very low impedance to ground until the stored minority carriers are removed. When the base voltage is constant, the base current of Q_3 will also be constant at 5.6 ma. The collector current of Q_3 will be rising to the value of the current gain times this 5.6 ma; however, the cut-off frequency, which determines the rise time, is divided by the current gain. Therefore, the turn-on time will be determined by $\frac{I_c}{2\pi f_n I_b}$ in the same manner that it was in Sec. 2.5. For an f_n of 3mc, the collector current will rise to 10 ma in 0.1 μsec. The emitter current rises to 15 ma in the same time.

The emitter current of Q_3 is about equal to the base current of Q_5, but an approximate analysis is more involved here because the input current is not constant. To obtain a rough estimate of the turn-on time, the input current can be assumed to be zero for the first 0.1 μsec and then to be no less than 15 ma. When this 15 ma starts to flow, the output will rise to 100 ma of collector current in 0.3 μsec. The total time needed to rise to 100 ma will be 0.4 μsec from the time that the voltage swing at the base of Q_3 reaches the zero level. The actual waveform (Fig. 4.4) of the base current of Q_7 shows it to be a linear rise. The turn-off time of Q_7 was calculated in Sec. 2.5 for a constant reverse current of 100 ma. Since the base current is not constant, the turn-off time will be in error. However, in the above circuit, the current is not limited to 100 ma. If the transistor-gate is still in saturation, the current continues to rise to a value equal to the product of the input current times the current gains of Q_3 and Q_4. For various transistors tested, the peak current varied over a wide range and was as high as 150 ma.







NOTE:
TIME SCALE BROKEN IN CENTER TO SHOW TURN-ON AND TURN-OFF WAVEFORMS IN GREATER DETAIL.

FIG. 4.4
EXPERIMENTAL
LEVEL AMPLIFIER WAVEFORMS

A-64954

The power ratings of the transistors Q_2 through Q_6 have not yet been considered, but Q_1, Q_2, Q_3 and Q_4 do not carry appreciable current when the collector voltage is high. Q_6 carries the steady state base current of Q_7, but in the circuit of Fig. 4.3 the current was only 6 ma. However, with the transistor designed in Sec. 2.5, base currents up to 48 ma will be expected. The dissipation in Q_6 will then be approximately 50 mw per collector-to-emitter volt. In the circuit of Fig. 4.3 this would mean a dissipation of 125 mw; however, this could be reduced by raising the -7.15 volt supply to -6 volts. Then 100 mw transistors could be used for Q_6.

The quiescent current in Q_5 is very small as has been noted above; however, the transient current may be very high. If the values above are used, the peak dissipation is 15 x 0.150= 2.25 w. The rise to this value is from zero current, and so the average dissipation over the time that current is flowing will be 1/3 x 2.25= 0.75 w. The repetition of this dissipation is low because it only occurs on the turn-off of a particular transistor-gate. This same position can not be turned on until the next cycle ends. Therefore, it will be 12 μsec before the transient can occur again. The maximum average dissipation is 1/24 x 0.75=0.031 w=31 mw, well within the rated dissipation of most alloyed-junction transistors.

The voltage ratings of all the units are about the same, because in the worst case the collector-to-base diode on each transistor has 15 + 6=21 volts of bias. This occurs on Q_3, Q_4, Q_5 and Q_6 when the emitter-to-base diode is concurrently reverse biased with the collector-to-base diode. Thus, the only restriction on the applied voltage is that it be less than the grounded-base breakdown voltage, V_B. A maximum I_{co} of 100 ma with

25 volts of collector voltage should be sufficient. The emitter-to-base junction on Q_5 is reverse biased by the value of the voltage across the 690 resistor (4.5 volts) and I_{eo} should, therefore, be less than 100 μamps at 10 volts.

The results of this section can be tabulated as follows:

Transistor (Fig. 4.3)	f_n mc	I_c max. ma	α_n @ I_c min	I_c ma	P average mw	I_{co} @ V_c μamps	V_c volts	I_{co} @ μamps	V_c volts	V_P
Q_3(npn)	3	7.4	30	5	50<	100	25			30
Q_4(pnp)	3	<10	30	10	50<	100	25			30
Q_5(npn)	3	150 peak	20	150	30	100	25	10	10	30
Q_6(pnp)	3	50	25	50	75	100	25			30

4.4 Safety Features

If one of the transistor-gate level amplifiers fails in such a way that the transistor-gate is left in the OFF condition when it should be ON, then there will not be a path for current from the READ-WRITE generator. The voltage on the READ-WRITE bus will, as a result, vary over a larger range than predicted in Sec. 2.4. When the voltage rises to the OFF voltage, then all the transistor-gates will conduct from collector-to-emitter with inverted transistor action taking place and the base current of Q_7 in Fig. 4.3 flowing out through Q_6. With 63 lines conducting 425 ma, there will be 7 ma per line and a dissipation per unit of 100 mw, which is within the capabilities of the transistors to be used as gate.

When the voltage swings negative, nothing will happen until one of the transistors suffers body breakdown, and then all the current will pour through the one unit. This would probably overheat the transistor, and it would become a short to ground, thereby saving all the other units. It seems more reasonable though to add a circuit to the READ-WRITE

generators that would prevent the voltage at the bus from going more than a few volts past the maximum expected negative peak in voltage. A diode clamping circuit should suffice, although this adds a little more capacitive load to the drivers. It could also be accomplished by making the current generators bottom at $\pm$ 15 volts. With transistor drivers, this would be acomplished easily since they remain current sources until the collector voltage is below a few volts. Vacuum tubes, however, require high plate voltages to draw the high currents and diode clamping would have to be used.

4.5 Marginal Checking[52]

The concept of marginal checking is a very useful one for insuring that a system does not slowly deteriorate. Possible troubles in the selection system would be a slow turn-on or turn-off time due to changing transistor characteristics. In all the applications in the transistor-gate level amplifier, circuits were overdriven so that minor changes in current gain (B) would not affect the switching time as it is more dependent on the driving currents and the cut-off frequency (f_n) than it is on B. Since f_n is determined by the physical construction (Sec. 3.2.1) of the transistor, one would not expect this parameter to vary.

To detect large changes in alpha, it would be desirable to inspect the collector voltage of the transistor-gates while varying some of the supply voltages. It would be impractical to look at each collector individually, and the voltage at the READ-WRITE bus is too large to detect small changes in collector voltage that could indicate serious trouble in one transistor-gate. Ideally, if the collectors of each transistor-gate could be shorted together, the voltage at one point would indicate the

state of all the transistor-gates, and it would be relatively simple to check for slow turn-on time.

Turn-off time does not lend itself to a straight forward solution, as there is no one spot at which the base voltages can be observed. However, the transistor (Q_5) that turns off the gate draws a large pulse of current from the +15 volt supply. Although generally undesirable, the variation in the voltage might be a good indication of when the circuit was turning off fast.

If one of the many signals that are present on the power supply voltage when rastering through the coordinates begins to decrease and shift in time, the indication would be that one particular line is taking longer to turn off than the others. While still observing the power supply voltage, the slow line could be isolated and then investigated directly.

CHAPTER V

EXPERIMENTAL RESULTS

5.0 Introduction

As with most experimental theses, considerable time was spent on measurement problems not directly associated with the thesis topic. Many blind alleys were encountered, but data was taken on prospective transistor-gates, and on the operation of the associated level amplifier. The results are reported below.

5.1.0 Transistor-Gate

Commercial manufacturers are, at the present time, producing two types of transistors: the high-frequency (low-power, low-voltage) unit, as exemplified by the surface-barrier transistor[6], and the high-power (low-frequency, low collector resistance) transistor such as the 20 w Minneapolis Honeywell H-2.

Neither type of transistor meets all of the specifications listed in Sec. 2.5, but samples of each type were tested to determine the transistors' shortcomings.

In order to compare different units some criteria had to be established. The maximum rated dissipation of each unit could have been a common tie. In a test, such as the maximum collector current for a given step of base current, the collector current would have been adjusted until the total dissipation equaled the rated dissipation. As a result the collector voltage would have been quite large for the power transistors.

It was felt, however, that the most important parameter of the transistor-gate was its low impedance to ground. In this case slight variations in transistor parameters will not affect the selection line currents. Therefore, all measurements concerning current gain were taken

with the collector current adjusted to give a maximum collector voltage of 1 volt.

Since static measurements would not indicate the pulse characteristics of various transistors, it was necessary to perform pulse measurements.

5.1.1 High-Power Transistors

A Minneapolis Honeywell H-4 was selected as a high-power unit having a dissipation that perhaps was close to that needed for the transistor gate. The current gain varied over a wide range of values depending on the relative timing between the application of the step of base current and the application of the pulses of positive or negative collector current. Thus, it is found, for example, that pushing current into the collector within 5 μsec after the base drive had been applied, results in an initial peak of voltage which decreases to a very low value if the collector current is left on for more than 5 μsec. On the other hand, if, after the application of base drive, more than 5 μsec is allowed to elapse before the application of a pulse of collector current, then, (starting at the time when collector current begins) the initial collector-to-base voltage will be low initially. It will increase to its final value after an additional 10 or more μsec. The peak of voltage in the first case was probably due to a lack of carriers at the collector-to-base junction because the base is quite wide (judging from the low alpha cut off frequency -- 200 kc) and a few microseconds was required to build up the stead state carrier density. If the emitter-to-base junction had been forward biased for a period of time, the carriers would have become quite dense in the base region. Applying a collector current now draws these excess carriers off but the density of carriers needed

for the total collector current creats a field across the base region and results in a voltage once the initial charge of carriers has been used up.

An interesting feature was observed on these units that was not observed on high-frequency transistors, probably because of the short times involved. If current were pushed into the collector so that it acted as an emitter of carriers, a higher current gain could be realized for the first few microseconds than could be realized by drawing the current out of the collector. The static normal and inverted current gains of the transistor at 1 ma were 20 and 3 respectively. Fig. 5.1 indicates the variation in normal current gain that was experienced by demanding that the base current be of sufficient magnitude to allow 410 ma of collector current to flow at some later time, with no more than 1 volt of collector-to-emitter voltage. With a one microsecond delay, 370 ma of base current is required to keep the collector-to-emitter voltage below one volt. At 10 μsec only 63 ma are required, but further delay does not reduce the required base current appreciatively.

Aside from the long turn-on time, the final value of the current gain is low even though the maximum current rating of the unit is 400 ma. The two units tested had rather low collector resistance, 60 K at 30 volts and although not measured, probably very high collector capacitances due to the large physical size of the collector. Without too much more testing, the high-power transistors were set aside as having too low a frequency response and too low a current gain (a high current gain had been hoped for in order to overcome the known low frequency response).

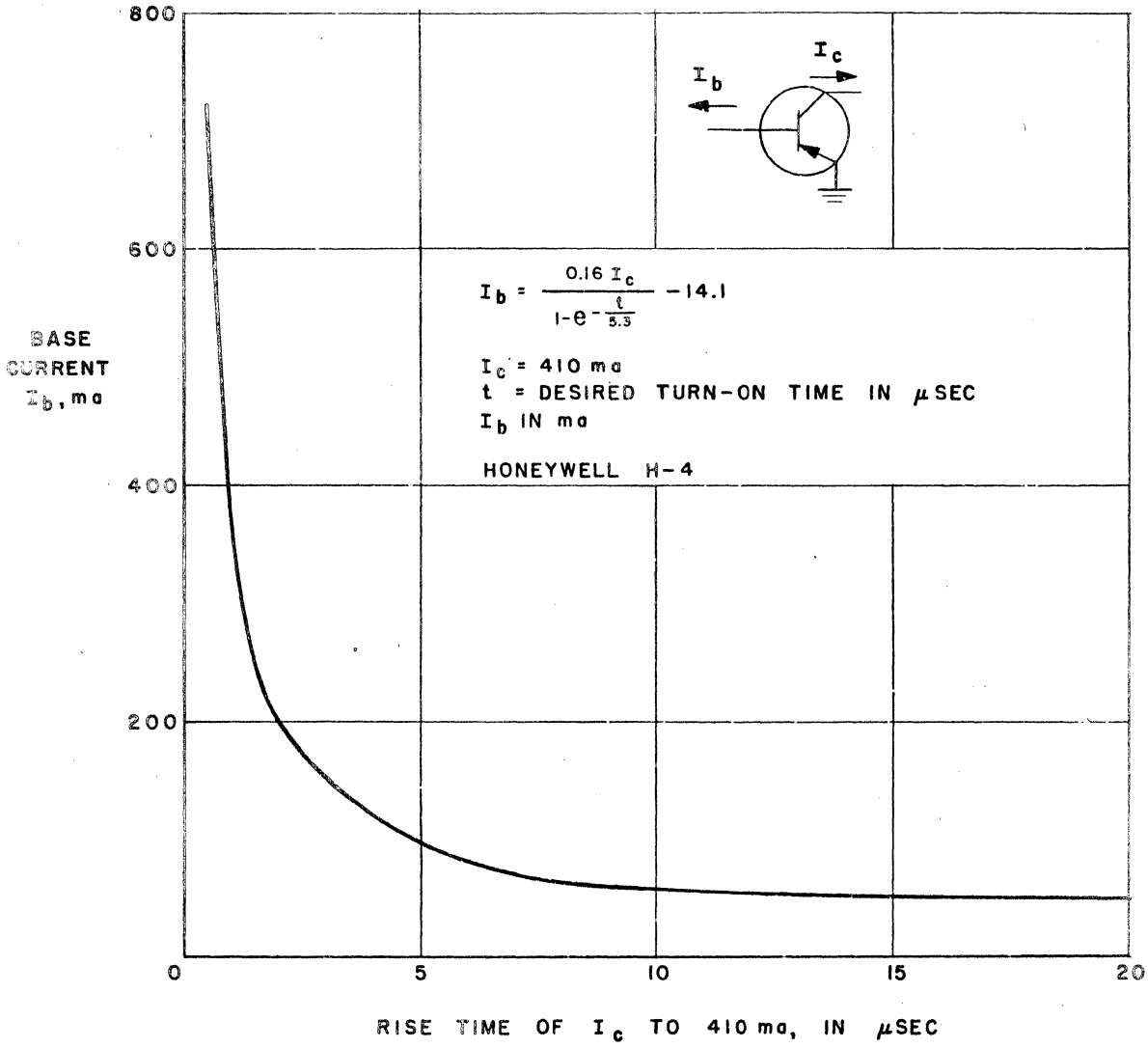


FIG. 5.1

REQUIRED BASE CURRENT vs. TURN-ON TIME

FOR A LOW-FREQUENCY TRANSISTOR

8-80034

5.2.0 High Frequency Transistors

The power rating of the transistor-gate has not been specified, but it must have the ability to dissipate the necessary power associated with the 425 ma pulses of collector current and the specified base drive (45 to 48 ma). Olsen[24]'s original idea was to use low-power, high-frequency transistors if the saturated resistance was low enough to prevent the rated dissipation from being exceeded. Along with saturation resistance, the variation of current gain and breakdown voltage were measured.

5.2.1 Saturation Resistance

Ebers and Moll[30] have derived an equation for the saturation voltage during grounded-emitter operation. Since their equation neglects the body resistance, and the resistance of connecting leads might also be appreciable, it was decided to pulse test these units too. All of the transistors tested (Raytheon 2N113's and 2N114's, Radio Receptor RR157's, and some special units from Philco) had saturation resistances in the range of 1 to 2 ohms. This was not the resistance with 45 ma of base current and 425 ma of collector current, but was the saturation line as seen on a plot of the collector characteristics. Assuming that the transistors were saturated, the power input while carrying the 425 ma of collector current is about 500 mw. With a 50% duty factor, this might be reduced to 250 mw. The static base input power must also be added to the collector dissipation and since the equivalent base resistance in some units is as much as 50 ohms, the base power is appreciable. The total dissipation here might be as high as 375 mw. With a 50% derating on the transistor manufacturer's ratings a 750 mw unit would be required. All the units tested had 50 mw ratings. Since the saturation resistance can-

not be decreased without driving the transistors far into saturation, the units are not satisfactory for this purpose.

5.2.2 Current Gain

Since transistors with the desired characteristics were not available, it was decided that experience with the high-frequency transistors, operating at a low duty cycle, would indicate in a general way what to expect from the desired units.

The saturation resistance has been found as part of the experiment on the measurement of the pulse current gain (as in Sec. 5.1). The results were quite startling, considering the experience with the high-power units, because the high-current gains of the high-frequency transistors were as good, and in some cases better, than the steady state current gain of the high-power units. The high frequency units had a high current gain of 10 or better, within a microsecond after applying the base current. Some of the units were very symmetrical although they were not constructed with this property in mind. Webster's article[36] provides an insight into the results since he has shown that the variation in current gain is a function of base width (the distance between the emitter and collector regions). The narrower the base the less the variation in gain and also the higher the initial gain. It had been expected that the gain was a function of the area of the junction, but the narrow base masks the effect of a smaller junction area in the high frequency units.

The symmetry of some of the units indicated that the units could be made symmetrical with little loss in their high current gain.

If the unit is made to the specifications developed in Chapters 2 and 3, any decrease in current gain, due to an increased base width, should be compensated for by an increase in the collector and emitter area to keep the current density constant.

5.2.3 Cutoff Frequency

The cutoff frequencies of the transistors tested were in the range from 5 to 10 mc, and are, therefore, fairly close to the desired value of 7 mc. There were high peaks of voltage associated with the turn on of the current pulses. Since the rise time of the collector current affected the peak in collector-to-emitter voltage, the current rise was adjusted to be the one-half microsecond asked for in the memory specification. This reduced the peak in voltage so that a higher current gain could be obtained.

Generally, a decrease in the amplitude of the collector-to-emitter voltage will accompany a shift in collector current from 1 μsec delay to 2 μsec after the application of base current. Any further increase in delay will not decrease the voltage, indicating that the steady state condition had been reached.

5.2.4 Voltage Ratings

Most of the high frequency units had voltage ratings of five to ten volts and were to be used in general for amplification of radio frequency signals at low levels. The base width and/or base resistivity of the transistors were not controlled too closely and the actual breakdown voltages varied over a large range. The avalanche voltage V_A varied from 10 to 20 in four 2N114's, while the punch-through voltage, V_P, varied from 11 to 32 in these four units.

Even though the voltage ratings were exceeded and the pulses of current were extremely large, the reason for transistors failing could always be traced to a circuit error and never to a sudden change in the transistors characteristics.

5.3.0 Experimental Transistor-Gate Level Amplifier

When the driving circuitry for the transistor-gate was being developed, two radically different techniques were tested. The first was similar to the positive bias technique discussed in Sec. 4.2.2 and the second was the complimentary symmetry circuitry discussed in Sec. 4.3. The first technique has the advantage of requiring only one transistor to drive the base circuit; but it has the disadvantage of having to supply a drive to the transistor gate equal to the sum of the positive bias current and the required base current. The second technique needs only to supply the actual transistor-gate base current during the ON time, and it can supply large reverse base currents at the turn-off time to provide fast switching. However, it requires two transistors for each one required in the first technique.

5.3.1 Turn-off Times

To keep the turn-off time short, large reverse currents must be supplied to the base of the transistor gate. In the first system described above a small resistance to the positive voltage supply will provide this current, but the input current must necessarily be increased by the addition of reverse current. If 100 ma of reverse current is required, the ON current will be 150 ma. While the tests on turn-off time were being performed, vacuum tube current sources were used to drive the base because of the large currents required.

Without taking extensive data it became apparent that even with the high frequency units, a large reverse base current was required to obtain the desired turn-off time, and the complementary-symmetry circuitry was adopted from another group at Lincoln Laboratory. In Fig. 4.3,

transistors Q_3 through Q_6 comprise the complementary-symmetry circuitry, and the operation is described in Sec. 4.3. With some transistors, the turn-off can be completed in about 0.5 μsec with only one pair of transistors. Using both pairs of transistors decreases the turn-off time to less than 0.3 μsec. The number of transistors required for this circuitry depends upon the alpha cut-off frequency of both the transistor-gate and the npn transistors used to turn the gate off.

The voltage ratings of the npn's and the pnp's in the complementary-symmetry circuitry will be determined by the difference between the OFF voltage and the negative supply voltage of the pnp's [15.4-(-7.5)= 22.55 volts]. If it is desired to make the base input resistor larger to reduce variations in base current, a larger voltage will be necessary, and the required voltage rating of all the transistors will have to be increased. A larger sized memory will also increase the voltage ratings because the OFF voltage must be increased.

A difficulty that arises is the fact that a high alpha cut-off frequency transistor will have a low breakdown voltage. On 10 2N94A's (a 6 mc npn transistor) the actual avalalanche voltage (V_A) ranged from 22.3 to 35.5 volts. The punch-through voltage (V_p) was greater than 30 volts on all units. The only rating the manufacturer placed on the units was the maximum collector-to-base voltage---20V. The maximum collector-to-emitter voltage, when operating grounded-emitter or grounded-collector, should not exceed 15 volts. If higher ratings are desired, then the units cannot come from stock items, but must be individually tested to insure that the actual operating voltages are safely below the breakdown voltages.

If one of the transistors in this circuit alloys through (Sec. 4.1),

the complementary transistor associated with it willbe destroyed if the supply voltage is not removed in a very short time. Consider in Fig. 4.3 that Q_4 has shorted from emitter-to-collector, but that the base-to-emitter and base-to-collector resistance is still high. When Q_2 is turned off so that the base of Q_3 is returned to +15 volts through 2.7K ohm, the base current of Q_3 will be $\frac{15+7.2}{2.7}$ =8.2ma. The collector current will rise to a high value, perhaps greater than 100 ma; moreover, the collector-to-emitter voltage will remain practically fixed at 22.2 volts. How long the transistor will last when dissipating more than 2 watts is a matter of speculation, but the power supply must be capable of delivering 100 ma pulses to the final stage and would have to be fused accordingly. Part of the difficulty is that low current fuses have appreciable resistance, i.e., a 125 ma fuse has approximately 20 ohms resistance. If the fuse is by-passed by a capacitor, then the action of the fuse is delayed. Transistors were destroyed by this sequence of events in the experimental circuit, but it was always because of operating a transistor above its punch-through voltage and the transistor failed when power was first applied. If the transistors are carefully selected, then it might be reasonable to assume that there will be few, if any, failures. Therefore, fuses will only provide protection against the high current shorts.

5.3.2 Turn-On Time

When turning on the transistor-gate, an overshoot in base current is desired to decrease the turn-on time. If the base resistor of the gate is bypassed by a capacitor, then the turn-on current will be increased. During the turn-off, the only path for the capacitor discharge is through the base resistor, because Q_6, in Fig. 4.3, is an open circuit. If the

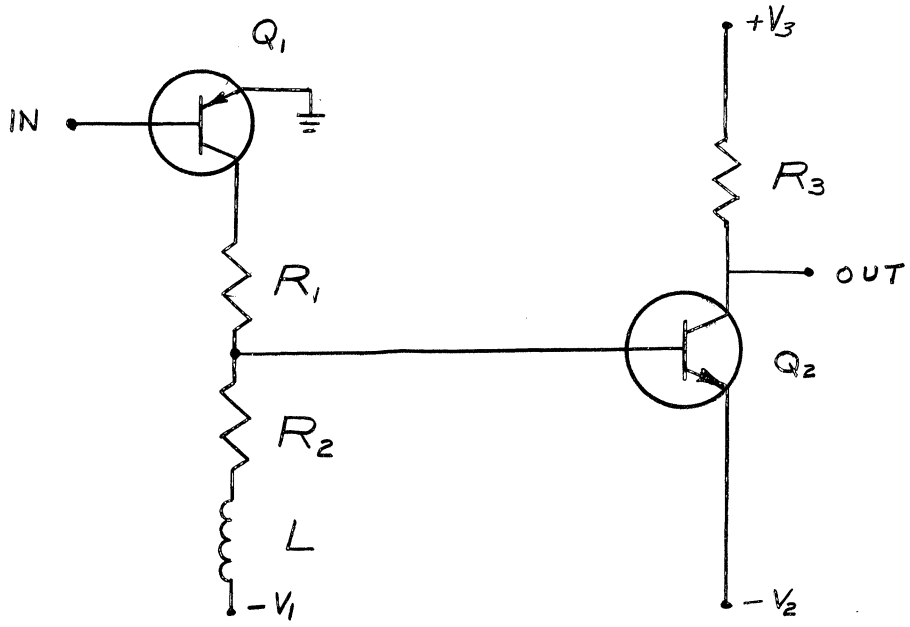
capacitor is not fully discharged within 6 μsec, and the same line is reselected on the next clock pulse, the turn-on base current will be lower than it was the first time, because the capacitor is partially charged. As a result, the transistor-gate turn-on time will be longer. There is no disadvantage in making the capacitor larger in this case; however, care should be taken to measure the longest turn-on time. If a time constant of 0.1 μsec is used as a start, the value of C will be 150 μμfd. Comprehensive data has not been taken on this variation, as the higher frequency units were capable of turning on in the required time without assistance from capacity. With a slightly lower alpha cut-off frequency transistor (2 to 4 mc) the Western Electric GA-52830 (Bell Laboratories M-2012), a capacitor of C=1000 μμfd doubled the input current during the first few tenths of a microsecond of base current flow. The tests have not been completed on this particular transistor, and this large a capacitor may not be required because the effect observed when the above information was measured was the variation in amplitude and shape of the peak in base current during the turn-on time.

5.3.3 Speed-Up Circuits

A resistance-capacitance network in the base of a transistor, such as the matrix input circuits in Fig. 4.2, provides a higher current to turn the transistor both ON and OFF with a minimum of delay. Some other circuits were given cursory inspection to determine if they added anything to the RC networks operation.

One circuit tested involved a pnp transistor with two load resistors in series. The common point of the two resistors was connected directly to the base of the next transistor, an npn. The resistor going

to the negative supply was also in series with an inductance, L. (Shown in the figure below.)



When the first transistor was turned on, the choke blocked the path of current flow to the power supply. The collector current was then determined by the resistor between the collector of the first unit and the base of the second unit, together with the emitter supply voltage on the second stage, based on the assumption that the first stage was driven into saturation. The initial base current was high and provided a short turn-on time. If the current in L has risen to its final value by the time the input is turned off, this current must now flow through the base of the second transistor and should provide the necessary reverse current to give a short turn-off time.

When a circuit was constructed and the value of L varied, the turn-on time decreased from 1.0 μsec to 0.4 μsec as the inductance increased from 0.1 mhy, to 1 mhy. Values of inductance lower than 0.1 mhy also resulted in a 1 μsec turn-on time, and, increasing the inductance to

more than 1 mhy did not decrease the turn-on time. The turn-off time remained constant as the inductance was increased from zero to 1 mhy. As the inductance was increased further, the circuit started to ring during turn-off, and the turn-off time increased. The ringing was due to self resonance in the coil. The voltage supply of the first stage was more negative than the emitter supply of the second stage; therefore, this circuit had negative bias on the second stage (an npn). The value of negative bias current was approximately equal to the steady state current flowing through L, so that increasing L had no effect on the turn-off time. If the two negative supplies were the same value, then there would have been little current in L, and again changing L would not vary the turn-off time.

Another curcuit technique investigated briefly was the use of a lumped-parameter delay line in place of the capacitor in the base of the transistor. This allows the transistor to be turned on and off with a step of base current instead of with the exponential rise and fall, which is not the most desirable waveform, according to C. Kirk*. The impedance looking out of the delay line terminals is not the same during the turn-on and turn-off times, and the one line constructed rang violently. If the circuit configuration happened to be such that the impedance remained relatively constant, then this technique might be applicable.

S. Bradspies** suggested the use of a non-linear capacitor to shorten the transient time and provide a more nearly constant current during the turn-on and turn-off times. With the present materials and techniques, voltages on the order of 50 volts are required to switch the

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*Massachusetts Institute of Technology, Lincoln Laboratory, Staff: Private Communication

**Massachusetts Institute of Technology, Lincoln Laboratory, Staff: Private Communication

dielectric material in a microsecond. Since the voltages across the base resistors are generally under ten volts, this could not be investigated as a possible speed-up device.

CHAPTER VI

CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER STUDY

6.0 Introduction

It appears as though, using present techniques and devices, a transistor can be built that will satisfy the specifications of the transistor gate. At the present time, however, no such transistor has been developed. It is also possible, considering the rapidity with which the transistor art is developing, that in the near future new techniques and devices will appear that will make it relatively easy to construct transistors that are very well suited for use as gates. Whether the specifications developed in this thesis were stringent enough to insure satisfactory operation is a matter of speculation, due to the fact that a large system has not been built.

6.1 Transistor-Gate Level Amplifier

Although the matrix was not constructed, the logical operations have been observed and no great difficulties will be expected from the assembled array. Some changes in values of components may be needed to speed up any slow circuits. A total delay of 0.2 or 0.3 μsec might be expected from the time the signal indexes the MAR till the time the signal appears at the transistor-gate. The most critical point appears to be the voltage ratings of the transistors that take the full output voltage swing. The normal alpha cutoff frequency (f_n) affects operation more than the current gain (B), so long as the transistor is in saturation. The two important characteristics of the transistor, the voltage rating and f_n, oppose each other, that is, increasing the voltage rating generally results in a lower f_n, and increasing f_n decreases the voltage ratings.

6.2 Transistor Gate

There are no suitable transistors now commercially available that satisfy all the specifications for the transistor gate. However, the major requirement lacking in most transistors is the power rating, and it seems that a minimum dissipation of 750 mw will be necessary. The decrease in current gain, as experienced with earlier transistors, has been eliminated to a great extent. The most promising transistors for the gating operation are the Western Electric GA-52830 and a special transistor that Philco Corporation is developing for Lincoln Laboratory. The Western Electric transistors are not symmetric and have a slightly lower f_n than called for in the specifications. The Philco units have low power ratings but this is not an inherent characteristic of the transistor. It is hoped that further development of the transistor will raise the power ratings.

All of the theoretical relationships indicate that the units can be constructed as either pnp or npn germanium transistors. The silicon transistor has not entered the high-power, high-frequency field because the present devices have high saturation resistances.

6.3 System Operation

Due to its non-linear nature, the effect on the selection line current of the collector-to-base capacity will be hard to evaluate in more detail than was carried out in Sec 2.5.4. Further study of this effect will have to involve measurements on the actual memory because of the complex interrelationships of the windings in the memory. The sensing problem may be quite different if the rise and fall times of the selection line currents are not the same as in the present system.

6.4 Recommendations for Further Study

Even though the complete system was not built, a good idea of the problems and limitations can be obtained from the work performed. It would be useful to compare this system to other possible systems, one such possibility being a register drive selection system[20]. Since only one word is being driven instead of a complete selection plane, it might be possible to drive the selection line directly with the transistor instead of separating the gating and driving functions. This is also one system that allows an increase in speed over the coincident-current operation.

The design procedure for the transistor gate using silicon instead of germanium should be carried out to indicate the future possibilities in that field.

One area in which study could well be directed is the development of the READ-WRITE generator. The thesis was started with the idea that a vacuum tube makes a better driver than the transistor does; but if the dissipation can be circumvented by paralleling transistors or if one transistor's dissipation is high enough, then the transistor driver could replace the vacuum-tube current generator without any change in the selection system.

APPENDIX A

It is desired to find any critical points of the following function in the range $\frac{I_c}{I_c+I_b} \leq \alpha_n \leq 1$.

$$\omega_n = \frac{1}{\tau_0(1-\alpha_n)} \ln \frac{1}{1 - \frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)}, \qquad \omega_n = 2\pi f_n . \tag{A-1}$$

$$\frac{\partial \omega_n}{\partial \alpha_n} = \frac{1}{\tau_0(1-\alpha_n)^2} \ln\left(\frac{1}{1 - \frac{I_c}{I_b}\frac{1-\alpha_n}{\alpha_n}}\right) - \frac{1}{\tau_0(1-\alpha_n)}\left(1 - \frac{I_c}{I_b}\frac{1-\alpha_n}{\alpha_n}\right)\frac{\frac{I_c}{I_b \alpha_n^2}}{\left(1 - \frac{I_c}{I_b}\frac{1-\alpha_n}{\alpha_n}\right)^2}. \tag{A-2}$$

To find a maximum or minimum, the derivative is set equal to zero:

$$\frac{\partial \omega_n}{\partial \alpha_n} = \frac{1}{\tau_0(1-\alpha_n)}\left[\frac{1}{1-\alpha_n} \ln\left(\frac{1}{1 - \frac{I_c}{I_b}\frac{1-\alpha_n}{\alpha_n}}\right) - \frac{1}{\alpha_n^2\left(\frac{I_b}{I_c}\frac{1-\alpha_n}{\alpha_n}\right)}\right] = 0. \tag{A-3}$$

If $1-\alpha_n$ does not go to zero then,

$$\ln \frac{1}{1 - \frac{I_c}{I_b}\frac{1-\alpha_n}{\alpha_n}} = \frac{1}{\alpha_n\left(\frac{\alpha_n}{1-\alpha_n}\frac{I_b}{I_c} - 1\right)} = \frac{\frac{1-\alpha_n}{\alpha_n}\frac{I_c}{I_b}}{\alpha_n\left(1 - \frac{1-\alpha_n}{\alpha_n}\frac{I_c}{I_b}\right)}. \tag{A-4}$$

Let $$Z = \frac{1}{1 - \frac{I_c}{I_b}\frac{1-\alpha_n}{\alpha_n}}. \tag{A-5}$$

Then $$Z - 1 = Z\frac{I_c}{I_b}\frac{1-\alpha_n}{\alpha_n} = \frac{ZI_c}{\alpha_n I_b} - \frac{ZI_c}{I_b}, \tag{A-6}$$

$$\frac{1}{\alpha_n} = \frac{I_b}{I_c}\left(\frac{Z-1}{Z}\right) + 1, \text{ and } \frac{1-\alpha_n}{\alpha_n} = \frac{I_b}{I_c}\left(\frac{Z-1}{Z}\right). \qquad \text{A-7}$$

Substituting,

$$\ln Z = Z \cdot \frac{Z-1}{Z} \cdot \left(\frac{I_b}{I_c}\cdot\frac{Z-1}{Z}+1\right) = (Z-1)\left(1+\frac{I_b}{I_c}\frac{Z-1}{Z}\right). \qquad \text{A-8}$$

This is satisfied at $Z=1$ because $\ln 1=0$ and $1-1=0$.

$$Z = 1 = \frac{1}{1 - \frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)}. \qquad \text{A-10}$$

$$1 = 1 - \frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right). \qquad \text{A-11}$$

$$1-\alpha_n = 0. \qquad \text{A-12}$$

$$\alpha_n = 1. \qquad \text{A-13}$$

However, this is a point at which the derivative, Equation A-2, is not defined because the coefficient that was dropped, $(\frac{1}{1-\alpha_n})$, becomes infinite. Limits must be taken then to determine if $\left.\frac{\partial \omega_n}{\partial \alpha_n}\right|_{\alpha_n=1} = 0$.

$$\lim_{\alpha_n \to 1}\left(\frac{\partial \omega_n}{\partial \alpha_n}\right) = \lim_{\alpha_n \to 1}\left\{\frac{\alpha_n^2\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right)\ln\left[\frac{1}{1-\frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)}\right] - 1 + \alpha_n}{\tau_0 \alpha_n^2 (1-\alpha_n)^2\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right)}\right\}. \qquad \text{A-14}$$

$$= \lim_{\alpha_n \to 1}\left\{\frac{2\alpha_n\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right)\ln\left[\frac{1}{1-\frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)}\right] + \alpha_n^2\left(\frac{1}{\alpha_n^2}\right)\ln\left[\frac{1}{1-\frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)}\right] + \alpha_n^2\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right)\left[1-\frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)\right]\frac{I_c}{I_b \alpha_n^2} + 1}{2\tau_0\alpha_n(1-\alpha_n)^2\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right) - 2\tau_0\alpha_n^2(1-\alpha_n)\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right) + \tau_0\frac{\alpha_n^2(1-\alpha_n)^2}{\alpha_n^2}}\right\}. \qquad \text{A-15}$$

$$= \lim_{\alpha_n \to 1} \frac{\left[2\alpha_n\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right)+1\right] \ln\left[\frac{1}{1 - \frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)}\right] + \left[1 - \frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)\right]^2 + 1}{2\tau_0\alpha_n(1-\alpha_n)^2\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right) - 2\tau_0\alpha_n^2(1-\alpha_n)\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right) + \tau_0(1-\alpha_n)^2}. \quad \text{A-16}$$

The numerator goes to 2 while the denominator remains zero, so there is no limit and there is no critical point at $\alpha_n = 1$.

Equation A-8 is also satisfied at Z equal to infinity because the logarithm of infinity is equal to infinity. The reciprocal of Z will be zero, so Equation A-5 becomes:

$$1 - \frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right) = 0. \quad \text{A-17}$$

$$I_c - \alpha_n I_c = \alpha_n I_b. \quad \text{A-18}$$

$$\alpha_n = \frac{I_c}{I_c + I_b}. \quad \text{A-19}$$

Equation A-3 for the derivative of ω_n with respect to α_n is equal to the difference of two large numbers at this point, so again the limit must be taken to determine if the derivative goes to zero.

$$\lim_{\alpha_n \to \left(\frac{I_c}{I_c+I_b}\right)} \frac{\partial \omega_n}{\partial \alpha_n} = \lim_{\alpha_n \to \left(\frac{I_c}{I_c+I_b}\right)} \left\{ \frac{\alpha_n^2\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right) \ln\left[\frac{1}{1 - \frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)}\right] - 1 + \alpha_n}{\tau_0\alpha_n^2(1-\alpha_n)^2\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right)} \right\}. \quad \text{A-20}$$

Taking the derivative of the numerator and denominator: A-21

$$\lim_{\alpha_n \to \left(\frac{I_c}{I_c+I_b}\right)} \frac{\partial \omega_n}{\partial \alpha_n} = \lim_{\alpha_n \to \left(\frac{I_c}{I_c+I_b}\right)} = \left\{ \frac{\left[2\alpha_n\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right)+1\right] \ln\left[\frac{1}{1 - \frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)}\right] + \left[1 - \frac{I_c}{I_b}\left(\frac{1-\alpha_n}{\alpha_n}\right)\right] + 1}{2\tau_0\alpha_n(1-\alpha_n)^2\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right) - 2\tau_0\alpha_n^2(1-\alpha_n)\left(\frac{I_b}{I_c} - \frac{1-\alpha_n}{\alpha_n}\right) + \tau_0(1-\alpha_n)^2} \right\}.$$

$$\lim_{\alpha_n \to \left(\frac{I_c}{I_c+I_b}\right)} \frac{\partial \omega_n}{\partial \alpha_n} \longrightarrow \infty$$

since the numerator increases without limit and the denominator remains finite.

Therefore, equation A-1 has no critical points in the range

$$\frac{I_c}{I_c + I_b} \leqslant \alpha_n \leqslant 1.$$

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