MOTOROLA®
HCA 6200/6300 HCMOS
Semicustom IC Design Kit

October 1986

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000-0144-00

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ABOUT THIS MANUAL

This manual describes the Motorola® HCA6200/6300 HCMOS Semicustom IC Design Kit, which consists of P-CAD's NX-M6300 translator program and the Motorola HCA6200/6300 HCMOS Macrocell Array Library.

The manual is divided into two sections: Section I describes the design kit and Section II describes the macrocell library.

Section I, DESIGN KIT USER'S MANUAL, contains the following:

Chapter 1, INTRODUCTION, provides an overview of the design kit and installation instructions.

Chapter 2, PREPARING THE INPUT FILES, gives instructions for creating the files to be input into the NX-M6300 translator program.

Chapter 3, TRANSLATING THE NETLIST, gives instructions for using the NX-M6300 program to translate netlists into LOGCAP™files.

Chapter 4, VIEWING THE OUTPUT FILES, describes the NX-M6300 output files.

Section II, MOTOROLA HCA6200/6300 HCMOS COMPONENT LIBRARY, contains an overview and detailed descriptions of the macrocell components.

NOTATION

This manual gives step-by-step procedures and examples. To make it easy for you to follow these procedures, we use the following notation.

<xxxx> Angle brackets around lowercase letters indicate a variable name that may be entered by the system or by you. For example:

<filename>.SCH

[ ] Square brackets indicate the name of a key. For example:

[Return]

[Return] [Return] indicates the key that is used to execute a command or accept an option. This key may be labeled differently, depending on your system. For example:

[RETURN], [↵], [Enter], [Enter↵], [ENTER]

[ ]-[ ] Square brackets connected with a hyphen indicate keys that must be pressed simultaneously. For example:

Press [Ctrl]-[Alt]-[Del].

UPPER Uppercase letters indicate a command or an element that must be typed as shown. For example:

Type PCPLOTS and press [Return]

/ A forward slash separates main menu and submenu command combinations. For example:

DRAW/ARC

* An asterisk in a filename or in a filename extension indicates that any character(s) can occupy that position and all the remaining positions in the filename or extension. For example, the DOS command

DIR *.SYM

displays a list of all the filenames with the extension .SYM in the current directory.

TESTFILE TESTFILE is a sample filename, which you must replace with the filename you intend to use. For example:

Database Filename : TESTFILE.SCH
Netlist Filename : TESTFILE.NLT

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CHAPTER 1. INTRODUCTION

The Motorola HCA6200/6300 HCMOS Semicustom IC Design Kit consists of this manual, and six diskettes containing the macrocell component library, the netlist files extracted by PC-NODES from each of the library components, and the NX-M6300 translator program.

This manual serves as a guide to using the Motorola HCA6200/6300 HCMOS Macrocell Array Library on the P-CAD design system. It assumes that you have the manuals for the P-CAD programs and are familiar with their use. If you are not yet familiar with the P-CAD system, we recommend that you complete the tutorials provided with the system before using the component library.

OVERVIEW

With this design kit, and PC-CAPS, PC-NODES and PC-LINK, you can create a schematic design using Motorola CMOS macrocell components. This design can be prepared for either PC-LOGS or Motorola's CAD system.

There are five stages in this process:

1. Using PC-CAPS, prepare the schematic design. The design consists of one or more schematic files (<filename>.SCH), which are created by connecting symbols (<filename>.SYM) from the Motorola Macrocell Array Library.

2. Using PC-NODES, extract a netlist (<filename>.NLT) from each schematic file. The design kit already contains netlists extracted from each macrocell component. Netlist files contain component and interconnection information for each schematic file or macrocell file.

3. After you extract all the netlists, use PC-LINK to link all the netlists you intend to use into a single expanded netlist file (<filename>.XNL).

   You can use the expanded netlist as input into either PC-LOGS or the NX-M6300 translator program. Use step 4 to use P-CAD's PC-LOGS program for local analysis, or step 5 to use the Motorola CAD system for mainframe analysis.

4. To use PC-LOGS, input the expanded netlist into PRESIM, which outputs the <filename>.NET file for input to PC-LOGS and simulation by PC-LOGS and the POSTSIM postprocessor. PRESIM, PC-LOGS, and POSTSIM are described in their corresponding manuals.

5. To translate the design for the Motorola CAD system, input the expanded netlist into the NX-M6300 translator program. NX-M6300 outputs two files:

   - The Motorola-compatible LOGCAP file (<filename>.LCP) can be input into the LOGCAP program and other analysis tools in Motorola's CAD system.

   - The cross-reference file (<filename>.XRF) lists component aliases assigned by PC-LINK and used in the LOGCAP file.

Figure 1-1 illustrates the process described above.

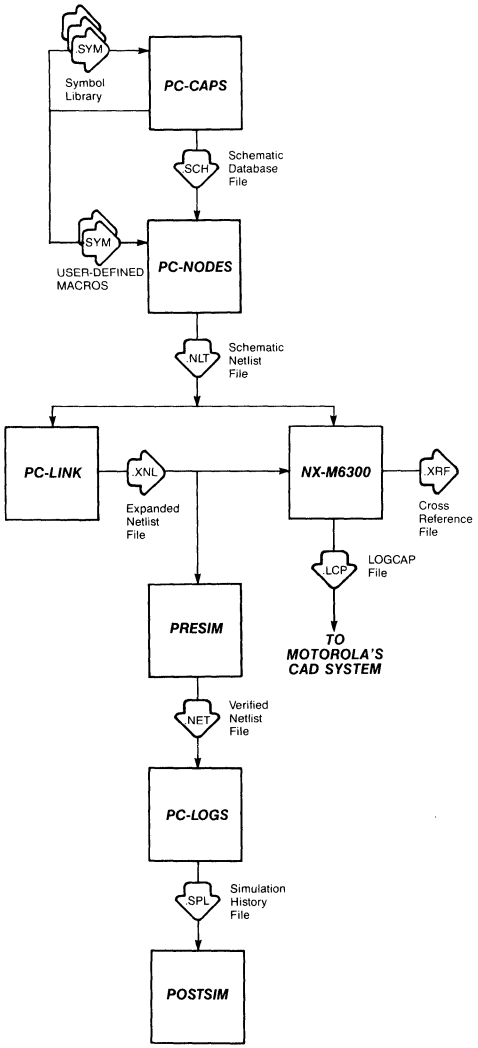


Figure 1-1. Design Kit Data Flow

SYSTEM REQUIREMENTS

Before you can install the design kit, your computer system must have the following minimum configuration:

- IBM PC, PC/XT, PC/AT, TI PC, Tandy 2000 or equivalent
- 640K of RAM
- P-CAD supported graphics board and monitor
- DOS 2.0 or higher operating system
- CONFIG.SYS in the root directory, containing a BUFFERS value of at least 12 and a FILES value of at least 15
- The PCADDRV.SYS file (created automatically when you use the P-CAD INSTALL program) in the root directory and the appropriate loadable device driver files in the appropriate directory

INSTALLATION

The design kit consists of six diskettes -- three diskettes containing the symbol library, two diskettes of netlist files, and the translator diskette.

To install the design kit on your hard disk, follow the procedures below. These procedures assume that you are using the P-CAD-recommended directory structure.

First, create three new directories for the symbols and netlists by typing

```
MD \PCAD\MOTOROLA [Return]
MD \PCAD\MOTOROLA\M6300 [Return]
MD \PCAD\MOTOROLA\M6300\NLT [Return]
```

To install the symbol library, first change directories by typing

```
CD \PCAD\MOTOROLA\M6300 [Return]
```

Then in turn insert each of the three symbol diskettes into drive A. For each diskette, copy the files by typing

```
COPY A:*.* [Return]
```

Remove each diskette after copying the files.

To install the netlist files, change directories by typing

```
CD \PCAD\MOTOROLA\M6300\NLT [Return]
```

Then insert each netlist diskette into drive A, and copy the files by typing

```
COPY A:*.* [Return]
```

Remove each diskette after copying the files.

To install the translator, first change to the \PCAD\EXE directory by typing

```
CD \PCAD\EXE [Return]
```

Then insert the translator diskette into drive A and copy the file by typing

COPY A:NXM6300.EXE [Return]

We suggest that you use the library and translator from a project directory created as a subdirectory of \PCAD\MOTOROLA.

CHAPTER 2. PREPARING THE INPUT FILES

Preparation of a design involves capturing the schematic using PC-CAPS, then generating, flattening, and linking netlists using PC-NODES and PC-LINK.

CREATING THE SCHEMATIC

Use PC-CAPS to prepare the schematics. Make all designs hierarchical. The topmost level should contain a symbol representing the functional design, and PADIN and PADOUT symbols to represent input and output pins. NX-M6300 extracts LOGCAP files from this top level. Use netlists extracted from the lower levels for PC-LOGS.

Unconnected input pins are allowed in schematics for LOGCAP files, but are not allowed in PC-LOGS. If you plan to simulate a design using PC-LOGS, connect the unconnected input pins to global nets called "CON1" for a logic high or "CON0" for a logic low. The stimulus command file for PC-LOGS must have statements that force the net "CON1" to a strong high level and "CON0" to a strong low level.

Net names can be from one to eight alphanumeric characters. If you want to name a net as an active low signal, use an apostrophe as the last character of the net name. PC-CAPS will display the net name with a bar over the top.

The P-CAD symbol library allows you to group partial functions into a single cell. The attributes and grouping information are included in the component symbols. Use the PC-CAPS SCMD/PNUM command to assign reference designators and sections to the functions. For

example, the macrocell C008 contains four separate inverters. When you instantiate this device, you see only the symbol for one of the four inverters, which represents one-fourth of the entire macrocell. You would assign this inverter to the third section of a macrocell named U1 by using the SCMD\PNUM command and entering "U1/C", where U1 is the macrocell name and C represents the third section. See the *PC-CAPS User's Manual* for instructions.

If your design has more than one sheet, assign the SHEET attribute to each sheet. To assign this attribute, use the PC-CAPS ATTR/ACOM command in SYMB mode and type

SHEET=<sheet id>

where

<sheet id> is two characters (generally digits) and is unique for each sheet in the design.

Input and Output Signals

Each circuit input requires a PADIN.SYM component. A net connected to the output pin of the PADIN.SYM component will be listed in the $INP statement of the LOGCAP output file. This signal can be viewed as the input signal to the circuit from an external source.

Each circuit output requires a PADOUT.SYM component. A net connected to the output pin of an output cell must be connected to the input pin of the PADOUT.SYM component. A net connected to the input pin of a PADOUT.SYM will be listed as an output signal on the $OUT statement of the LOGCAP output. This signal can be viewed as the output signal to the external environment.

Wired Outputs

Wired outputs require the explicit use of a WIREDx.SYM component, where x is the number of inputs. The library provides wired symbols with two to eight inputs. A $WIRED statement will appear in the LOGCAP output file for each WIREDx.SYM component in the circuit.

Tribus Structures

Tristate-bus structures require the explicit use of a TRIBUSx.SYM component, where x is the number of inputs. The library provides tribus symbols with two to sixteen inputs. If you have a tribus structure that requires a tribus symbol other than those supplied, use a tribus symbol larger than you need and connect all the unused input pins to one of the other nets used as input. NX-M6300 will ignore any duplicate nets attached to the input pins of the tribus component. A $TRIBUS statement will appear in the LOGCAP output file for each TRIBUSx.SYM component in the circuit.

Bidirectional Pads

Each bidirectional pad is modeled by one of several bidirectional buffers. The bidirectional input is treated as separate input and output signals. The net connected to the BPI pin is the input net and the net connected to the BPO pin is the output net.

Figure 2-1 illustrates the use of a bidirectional buffer.

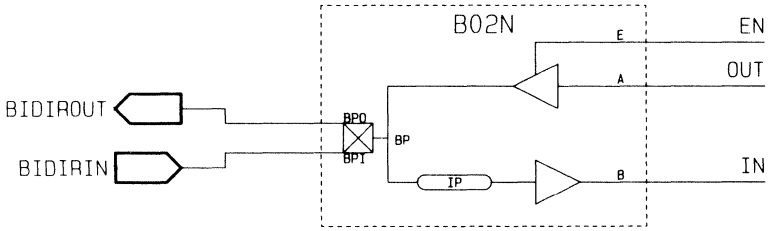


Figure 2-1. Bidirectional Pad

ANALYSIS

You can analyze the circuit using PC-LOGS. PC-LOGS provides local functional simulation, while Motorola provides mainframe analysis with their LOGCAP simulator. P-CAD's simulation models function the same as the LOGCAP simulation models except in cases where illegal input conditions, such as two simultaneous input transitions, cause the macrocells to malfunction. The LOGCAP simulation models go to an indeterminate state under such conditions and the outputs are considered "unknown" (X). PC-LOGS simulation models may not necessarily malfuntion in the same manner as the LOGCAP simulation models. Indeterminate states may assume a high or low state, or may oscillate. Refer to the *PC-LOGS User's Manual* for more information.

EXTRACTING AND LINKING THE NETLISTS

Run PC-NODES to extract a netlist for each network and sheet of a schematic. Use the instructions in the *PC-NODES User's Manual.* PC-NODES assigns names to unnamed nets and component instances in the format UNsssnnn and UCsssnnn, respectively, where sss is the sheet ID assigned to the design using the SHEET attribute, and nnn is a number assigned sequentially starting with 000. If sheet IDs are not assigned, or are not unique, the expanded netlist may contain several nets or components with the same name.

After you run PC-NODES, run PC-LINK to link together all the sheet and hierarchical component netlists to create an expanded netlist suitable for either NX-M6300 or PC-LOGS. Use the instructions in the *PC-LINK User's Manual.*

PC-LINK prompts you for a library path. This entry specifies alternate directories where PC-LINK will look for hierarchical netlist files (all Motorola CMOS symbols are hierarchical). If the hierarchical netlists reside in more than one directory, enter all the directories, separated by a plus sign. If you are extracting a netlist for NX-M6300, do not specify the path pointing to the library netlist files since the expanded netlist would contain references to PC-LOGS primitives. When you run PC-LINK to extract a netlist for NX-M6300, an error message will appear at the bottom of the screen. Review the PCLINK.MSG file; if all the errors indicate that the .NLT files for the Motorola CMOS library components cannot be found, disregard the error messages and run NX-M6300.

CHAPTER 3. TRANSLATING THE NETLIST

This chapter describes the required conditions and procedures for configuring and running NX-M6300.

Before running NX-M6300, be sure that:

- Your system is correctly configured.
- You have installed the NX-M6300 program file (NXM6300.EXE).
- You have assembled the schematic circuit.
- You have extracted and linked the netlist files.

To run NX-M6300, be sure you are in the appropriate directory, and follow the steps below.

1. Type

   NXM6300 [Return]

   The NX-M6300 Title Screen appears. Press any key to continue. The system displays the NX-M6300 Program Screen and prompts for the input netlist filename as shown in Figure 3-1.

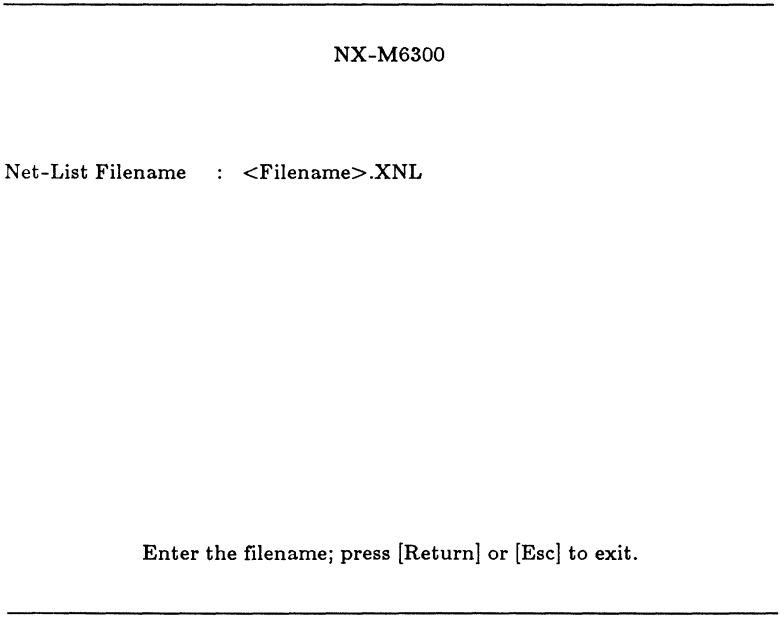


Figure 3-1. NX-M6300 Program Screen

NOTE: At any prompt, if you decide not to continue with the program, press [Esc] to cancel and return to DOS.

2. Type the netlist filename and press [Return]. If you do not enter the filename extension, NX-M6300 adds the .XNL extension.

   The system prompts for the output LOGCAP filename. The default is the input netlist filename with the .LCP extension.

3. Press [Return] to accept the default filename, or type another LOGCAP filename and press [Return].

The system prompts for the output cross-reference filename. The default is the input netlist filename with the .XRF extension as shown in Figure 3-2

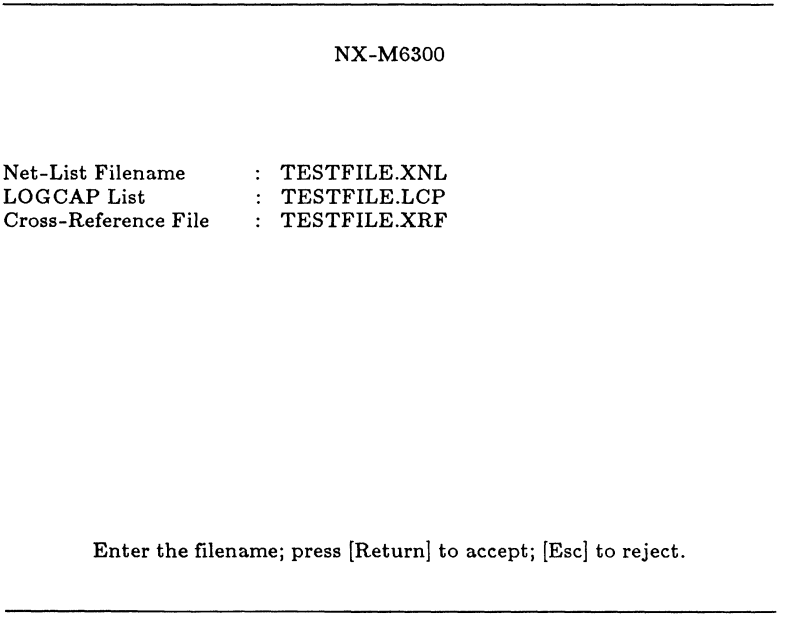


Figure 3-2. Sample Program Screen

4. Press [Return] to accept the default filename, or type another cross-reference filename and press [Return].

   NX-M6300 sets up the netlist database environment and generates the LOGCAP netlist output. It displays progress reports and error messages on the lower section of the screen. When processing is complete, the system returns you to the Netlist prompt.

CHAPTER 4. VIEWING THE OUTPUT FILES

The NX-M6300 outputs two files, the LOGCAP netlist and the cross-reference files. The following sections describe these files.

THE LOGCAP NETLIST

The basic LOGCAP statements are $NETWORK for network identification, $INP and $OUT for circuit inputs and outputs, and $WIRED, $TRIBUS and $SUBU for macrocells and interconnects.

The following sections discuss these statements. An example of a schematic and the corresponding LOGCAP netlist output file are shown in the Design Example section. Refer to the sample netlist for examples of the statements.

$NETWORK Statement

$NETWORK is the first line in the LOGCAP netlist output. It denotes the type of file used to generate the LOGCAP netlist.

$INP Statement

A single $INP statement directly follows the $NETWORK statement. NX-M6300 uses the PADIN.SYM components for the inputs of the circuits being modeled. All nets connected to output pins of PADIN.SYM components are listed in the LOGCAP

$INP statement as input signals. This signal can be viewed as the input signal to the circuit from an external source.

The format of the $INP statement is

$INP <net1> <net2> ... <netn>

where

netn is the name of a net connected to a PADIN.SYM output pin.

$OUT Statement

A single $OUT statement follows directly after the $INP statement. NX-M6300 uses the PADOUT.SYM components for the outputs of the circuit being modeled. All nets connected to input pins of PADOUT.SYM components are listed in the $OUT statement as output signals. The LOGCAP output signal can be viewed as the output signal to the external environment.

The format of the $OUT statement is

$OUT <net1> <net2> ... <netn>

where

netn is the name of a net connected to a PADOUT.SYM input pin.

$WIRED Statement

The LOGCAP file contains a $WIRED statement for each WIREDx.SYM component, where x is the number of outputs wired together. The $WIRED statement lists the names of the nets tied to the input and output pins of the WIREDx.SYM component and shows the number of inputs. A WIREDx.SYM component has one output and from two to eight inputs.

The format of a $WIRED statement is

```
$WIRED 0 0
<outnet> x <innet1> <innet2> ... <innetx>
```

where

outnet is the name of the net connected to the WIREDx.SYM output pin.

x is the number of input pins.

innet1 through **innetx** are the names of the nets connected to the WIREDx.SYM input pins.

$TRIBUS Statement

The LOGCAP file contains a $TRIBUS statement for each TRIBUSx.SYM component, where x is the number of outputs wired together. The $TRIBUS statement lists the names of the nets tied to the input and output pins of the TRIBUSx.SYM component and shows the number of inputs. A TRIBUSx.SYM component has one output and from two to sixteen inputs.

The format of a $TRIBUS statement is

$TRIBUS 0 0
<outnet> x <innet1> <innet2> ... <innetx>

where

outnet is the name of the net connected to the TRIBUSx.SYM output pin.

x is the number of input pins.

innet1 through **innetx** are the names of the nets connected to the TRIBUSx.SYM input pins.

$SUBU Statement

The LOGCAP file contains one $SUBU statement for each component (cell) in the circuit. Each $SUBU statement gives the definition name of the component and the names of the nets tied to the component input and output pins.

The format of a $SUBU statement is

$SUBU <compname>
<outnet1> <outnet2> ... <outnetn> / &
<innet1> <innet2> ... <innetm>

where

compname is the name of the component.

outnetn is the name of a net connected to an output pin.

innet1 through **innetm** are the names of nets connected to input pins.

The nets tied to the output pins are listed first. A slash separates the outputs from the inputs. An ampersand indicates that the list is continued on the following line. An asterisk indicates unused input and output pins.

NX-M6300 translates apostrophes, which PC-CAPS uses for netnames representing inverted signals, into the character "-". Apostrophes are invalid LOGCAP characters.

The following is an example of a $SUBU statement in a LOGCAP netlist

```
$SUBU I03N
HN000010 / &
S1
```

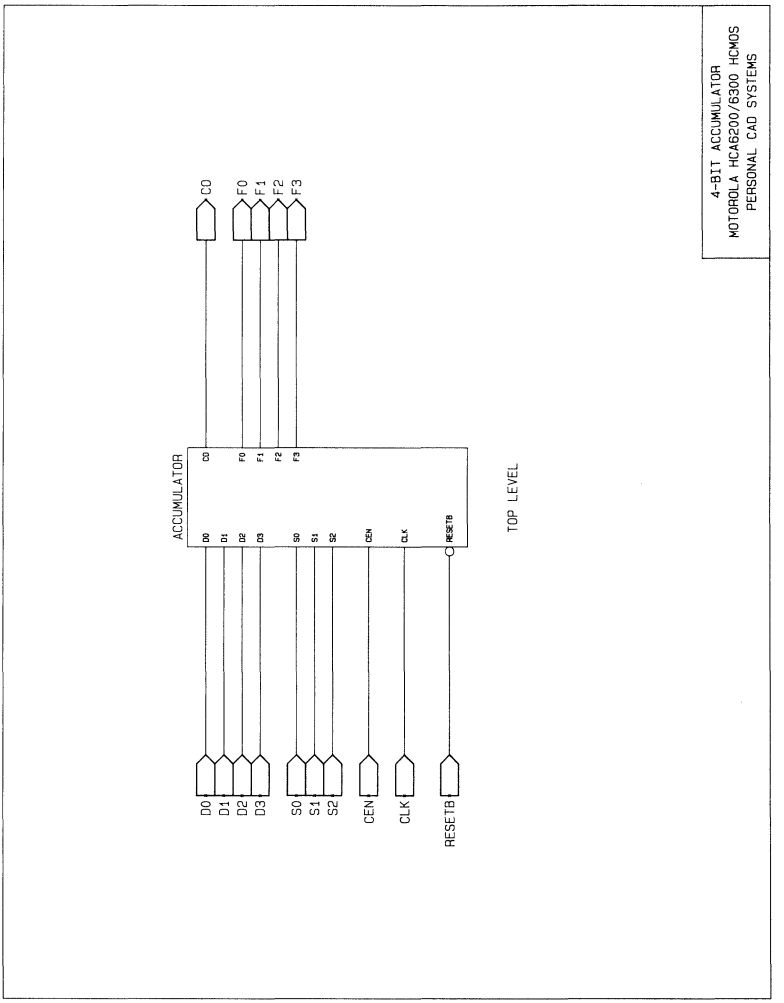
THE CROSS-REFERENCE FILE

The cross-reference file created by NX-M6300 lists the names of all nets and components renamed by NX-M6300, and their aliases. The aliases are used in the LOGCAP output file. NX-M6300 resolves duplicate default net and component names by changing the names to the form HNsssnnn and HCsssnnn, respectively, where sss is the sheet ID assigned with the SHEET attribute, and nnn is a three-digit number.

DESIGN EXAMPLE

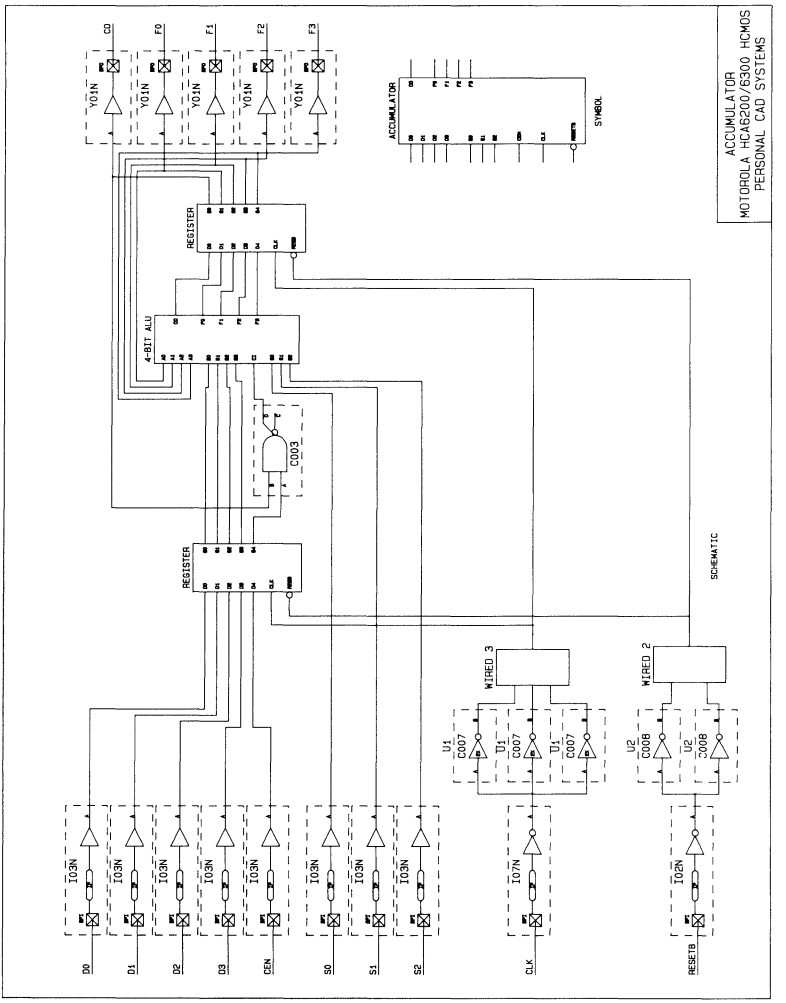
The following pages contain a design example showing a hierarchical design that was created using the CMOS library, and the resulting LOGCAP and cross-reference files output by NX-M6300.

Top Level Schematic of a 4-BIT ACCUMULATOR



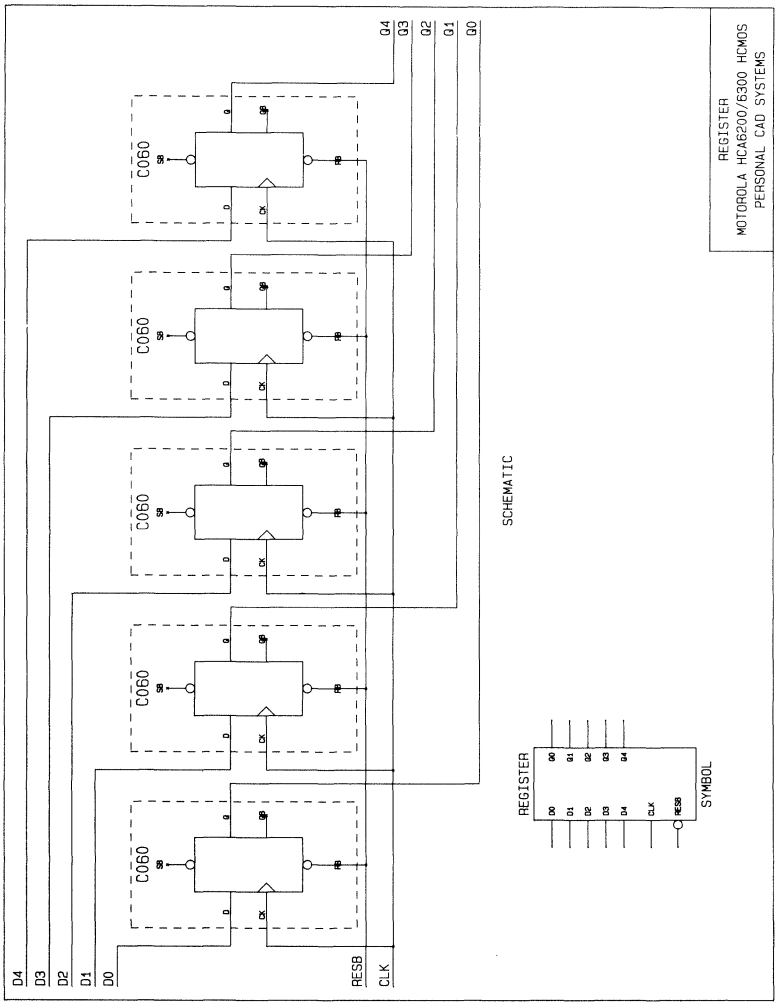
000-0144-00

Schematic Representation of an ACCUMULATOR

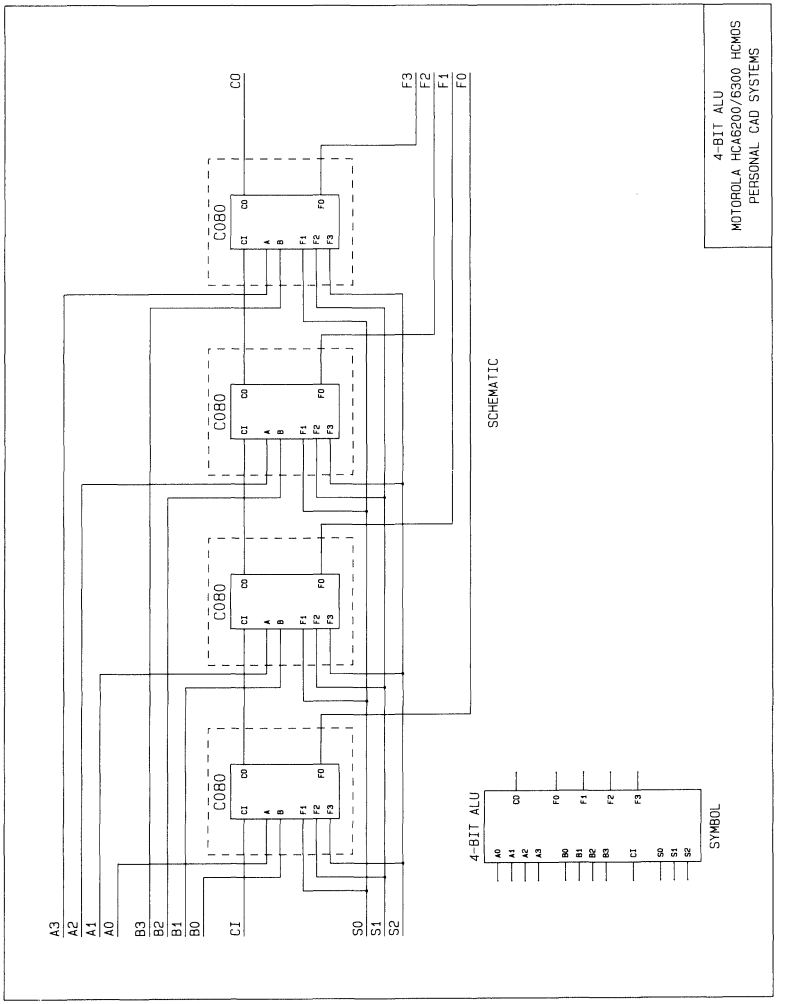


000-0144-00

Schematic Representation of a REGISTER



Schematic Representation of a 4-BIT ALU



LOGCAP Netlist File

```
$$*************************************************************************
$$      Copyright (C) 1983,1986 - Personal CAD Systems, Inc.             *
$$                                                                       *
$$      Program  :   NX-M6300  VERSION 1.31                              *
$$      Date     :   Aug 07 1986                                         *
$$      Time     :   05:13:57 PM                                         *
$$      File In  :   4BITACUM.XNL                                        *
$$      File Out :   4BITACUM.LCP                                        *
$$      Format   :   LOGCAP LIST                                         *
$$*************************************************************************

$NETWORK
$INP D0 D1 D2 D3 S0 S1 S2 CEN CLK RESETB
$OUT CO F0 F1 F2 F3
$WIRED 0 0
HN000020 3 HN000023 HN000025 HN000026
$WIRED 0 0
HN000021 2 HN000027 HN000035
$SUBU C080
HN000017 HN000013 / &
HN000008 HN000000 HN000004 HN000009 HN000010 HN000011
$SUBU C080
HN000018 HN000014 / &
HN000017 HN000001 HN000005 HN000009 HN000010 HN000011
$SUBU C080
HN000019 HN000015 / &
HN000018 HN000002 HN000006 HN000009 HN000010 HN000011
$SUBU C080
HN000012 HN000016 / &
HN000019 HN000003 HN000007 HN000009 HN000010 HN000011
$SUBU C060
HN000001 * / &
* HN000014 HN000020 HN000021
$SUBU C060
HN000002 * / &
* HN000015 HN000020 HN000021
$SUBU C060
HN000000 * / &
* HN000013 HN000020 HN000021
$SUBU C060
HN000022 * / &
* HN000012 HN000020 HN000021
$SUBU C060
HN000003 * / &
* HN000016 HN000020 HN000021
$SUBU C060
HN000006 * / &
* HN000031 HN000020 HN000021
$SUBU C060
HN000007 * / &
* HN000032 HN000020 HN000021
$SUBU C060
HN000005 * / &
* HN000030 HN000020 HN000021
$SUBU C060
HN000004 * / &
* HN000029 HN000020 HN000021
$SUBU C060
HN000033 * / &
```

LOGCAP Netlist File (Continued)

```
* HN000034 HN000020 HN000021
$SUBU I03N
HN000029 / &
D0
$SUBU C003
* HN000008 * * / &
HN000033 HN000022 * *
$SUBU I03N
HN000030 / &
D1
$SUBU I03N
HN000031 / &
D2
$SUBU I03N
HN000032 / &
D3
$SUBU I03N
HN000034 / &
CEN
$SUBU Y01N
CO / &
HN000022
$SUBU Y01N
F0 / &
HN000000
$SUBU Y01N
F1 / &
HN000001
$SUBU Y01N
F2 / &
HN000002
$SUBU Y01N
F3 / &
HN000003
$SUBU I07N
HN000024 / &
CLK
$SUBU I02N
HN000028 / &
RESETB
$SUBU I03N
HN000009 / &
S0
$SUBU I03N
HN000010 / &
S1
$SUBU I03N
HN000011 / &
S2
$SUBU C007
HN000023 HN000025 HN000026 / &
HN000024 HN000024 HN000024
$SUBU C008
HN000027 * HN000035 * / &
HN000028 * HN000028 *
```

Cross-Reference File Created by NX-M6300

```
*****************************************************************************
*                                                                           *
*                          ALIAS NAME CROSS-REFERENCE                       *
*                                                                           *
*  NX-M6300 Version 1.31                                                    *
*  Copyright (C) 1986 - Personal CAD Systems, Inc.                          *
*                                                                           *
*                                                                           *
*****************************************************************************


Net List Filename : 4BITACUM.XNL

COMPONENT    SIGNAL     FULL PATH NAME

HC000000               = /UC000000/UC000000
          HN000000     = /UC000000/UN000025
          HN000001     = /UC000000/UN000005
          HN000002     = /UC000000/UN000010
          HN000003     = /UC000000/UN000011
          HN000004     = /UC000000/UN000009
          HN000005     = /UC000000/UN000008
          HN000006     = /UC000000/UN000007
          HN000007     = /UC000000/UN000006
          HN000008     = /UC000000/UN000014
          HN000009     = /UC000000/UN000030
          HN000010     = /UC000000/UN000031
          HN000011     = /UC000000/UN000032
          HN000012     = /UC000000/UN000004
          HN000013     = /UC000000/UN000003
          HN000014     = /UC000000/UN000002
          HN000015     = /UC000000/UN000001
          HN000016     = /UC000000/UN000000
HC000001               = /UC000000/UC000000/UC000000
          HN000017     = /UC000000/UC000000/UN000000
HC000002               = /UC000000/UC000000/UC000001
          HN000018     = /UC000000/UC000000/UN000001
HC000003               = /UC000000/UC000000/UC000002
          HN000019     = /UC000000/UC000000/UN000002
HC000004               = /UC000000/UC000000/UC000003
HC000005               = /UC000000/UC000001
          HN000020     = /UC000000/UN000026
          HN000021     = /UC000000/UN000027
          HN000022     = /UC000000/UN000012
HC000006               = /UC000000/UC000001/UC000000
HC000007               = /UC000000/UC000001/UC000001
HC000008               = /UC000000/UC000001/UC000002
HC000009               = /UC000000/UC000001/UC000003
HC000010               = /UC000000/UC000001/UC000004
HC000011               = /UC000000/UC000002
          HN000023     = /UC000000/UN000021
          HN000024     = /UC000000/UN000028
HC000012               = /UC000000/UC000003
          HN000025     = /UC000000/UN000020
          HN000026     = /UC000000/UN000022
HC000013               = /UC000000/UC000004
HC000014               = /UC000000/UC000005
HC000015               = /UC000000/UC000006
          HN000027     = /UC000000/UN000024
          HN000028     = /UC000000/UN000029
    HC000016               = /UC000000/UC000007
```

Cross-Reference File Created by NX-M6300 (Continued)

```
          HN000034  = /UC000000/UN000019
HC000017            = /UC000000/UC000007/UC000000
HC000018            = /UC000000/UC000007/UC000001
HC000019            = /UC000000/UC000007/UC000002
HC000020            = /UC000000/UC000007/UC000003
HC000021            = /UC000000/UC000007/UC000004
HC000022            = /UC000000/UC000008
HC000023            = /UC000000/UC000009
HC000024            = /UC000000/UC000010
HC000025            = /UC000000/UC000011
HC000026            = /UC000000/UC000012
HC000027            = /UC000000/UC000013
HC000028            = /UC000000/UC000014
          HN000035  = /UC000000/UN000023
HC000029            = /UC000000/UC000015
HC000030            = /UC000000/UC000016
HC000031            = /UC000000/UC000017
HC000032            = /UC000000/UC000018
HC000033            = /UC000000/UC000019
HC000034            = /UC000000/UC000020
HC000035            = /UC000000/UC000021
HC000036            = /UC000000/UC000022
HC000037            = /UC000000/UC000023
HC000038            = /UC000000/UC000024
HC000039            = /UC000000/UC000025
```

COMPONENT LIBRARY

OVERVIEW

The library diskettes contain the following files for use with the PC-CAPS schematic capture program:

- Component files
- Special symbol files
- Netlist files for each component
- Behavioral model files for several components
- Standard-size drawing sheet files

COMPONENT FILES

The Motorola HCA6200/6300 HCMOS Macrocell Array Library contains all the components specified in the *Motorola HCA6000 Series Macrocell Array Design Manual.*

SPECIAL SYMBOL FILES

In addition to the standard Motorola component symbols, the library includes special "noncomponent" symbols. Use these symbols with NX-M6300 to translate your design information into a LOGCAP format that is compatible with Motorola CAD systems. Each special symbol in the circuit is described on a line of the LOGCAP output. The symbols are:

PADIN.SYM - Represents a circuit input.

PADOUT.SYM - Represents a circuit output.

WIRED2.SYM through **WIRED8.SYM** - Represent wired-output connections with two to eight outputs wired together.

TRIBUS2.SYM through **TRIBUS16.SYM** - Represent tribus structure connections with two to sixteen tribus outputs wired together.

NETLIST FILES

Each symbol in the component library is hierarchical, composed of a network of PC-LOGS primitives. Each CMOS macrocell in the library has an associated netlist file that contains all the network information of the simulation model.

BEHAVIORAL MODEL FILES

Several components are too complex to be easily simulated using PC-LOGS primitives. Behavioral models were used to describe the function of these macrocells. Files with the extension .PML and .MDL are behavioral model files. Refer to the *PC-MODEL User's Manual* for more information.

DRAWING SHEET FILES

The library includes standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH, for circuit design. These files provide the normal layer structure plus a drawing sheet border.

LAYER STRUCTURE

The layer structure shown in Table 1 is the default layer structure used by PC-CAPS. This layer structure was used to create the Motorola CMOS symbols included in this library.

Table 1. Default Layer Structure

Layer	Name	Pen	Status	Use
1	WIRES	1	OFF	Interconnecting wires
2	BUS	1	OFF	Not used
3	GATE	2	ABL	Gate geometry/symbol
4	IEEE	2	OFF	Not used
5	PINFUN	3	OFF	Not used
6	PINNUM	1	OFF	Pin numbers for macrocell sections
7	PINNAM	6	ABLE	Pin names
8	PINCON	4	ABL	Pin connections (dot)
9	REFDES	2	OFF	Macrocell section
10	ATTR	6	OFF	Visible attributes
11	SDOT	1	OFF	Not used
12	DEVICE	5	ABL	Macrocell ID
13	OUTLIN	5	ABL	Macrocell outline
14	ATTR2	6	OFF	Invisible attributes
15	NOTES	6	OFF	Not used

Table 1 Continued

Layer	Name	Pen	Status	Use
16	NETNAM	4	OFF	Net names
17	CMPNAM	5	OFF	Component instance names
18	BORDER	5	OFF	Drawing border

COMPONENT LIST BY SEQUENCE

The component filename consists of the macrocell number plus the extension .SYM; for example, H01.SYM. "Plot" refers to the plot number of the component plot in the last section of this manual. "Disk" refers to the disk on which the component is stored.

Component	Plot No.	Disk No.
B02D	3	1
B02N	1	1
B02U	2	1
B03D	6	1
B03N	4	1
B03U	5	1
B04D	9	1
B04N	7	1
B04U	8	1
B05D	12	1
B05N	10	1
B05U	11	1
C001	13	1
C002	14	1
C003	15	1
C004	16	1
C005	17	1
C006	18	1
C007	19	1
C008	20	1
C009	21	1
C010	22	1
C012	23	1
C013	24	1
C017	25	1
C019	26	1

Component	Plot No.	Disk No.
C020	27	1
C022	28	1
C025	29	1
C026	30	1
C027	31	1
C028	32	1
C029	33	1
C030	34	1
C031	35	1
C032	36	1
C033	37	1
C034	38	1
C035	39	1
C036	40	1
C037	41	2
C038	42	2
C039	43	2
C040	44	2
C041	45	2
C042	46	2
C053	47	2
C054	48	2
C055	49	2
C056	50	2
C057	51	2
C058	52	2
C059	53	2
C060	54	2
C080	55	2
C081	56	2
C082	57	2
C084	58	2
C085	59	2
C086	60	2
C087	61	2

Component	Plot No.	Disk No.
C088	62	2
C090	63	2
C091	64	2
C093	65	2
C094	66	2
C095	67	2
C096	68	2
C097	69	2
C700	70	2
C701	71	2
C702	72	2
C703	73	2
I01D	76	3
I01N	74	3
I01U	75	3
I02D	79	3
I02N	77	3
I02U	78	3
I03D	82	3
I03N	80	3
I03U	81	3
I05D	85	3
I05N	83	3
I05U	84	3
I06D	88	3
I06N	86	3
I06U	87	3
I07D	91	3
I07N	89	3
I07U	90	3
I08D	94	3
I08N	92	3
I08U	93	3
I09N	95	3
I10D	98	3

Component	Plot No.	Disk No.
I10N	96	3
I10U	97	3
PADIN	114	3
PADOUT	115	3
TRIBUS16	106	3
TRIBUS2	101	3
TRIBUS3	102	3
TRIBUS4	103	3
TRIBUS5	104	3
TRIBUS8	105	3
WIRED2	107	3
WIRED3	108	3
WIRED4	109	3
WIRED5	110	3
WIRED6	111	3
WIRED7	112	3
WIRED8	113	3
Y01N	99	3
Y02N	100	3

COMPONENT LIST BY FUNCTION

The component filename consists of the component number plus the extension .SYM; for example, H01.SYM.

Bidirectional Buffers

B01N	3-state out - short ckt inp
B01U	3-state out - short ckt inp with pull-up
B01D	3-state out - short ckt inp with pull-down
B02N	3-state out - TTL inp (non-inv)
B02U	3-state out - TTL inp (non-inv) with pull-up
B02D	3-state out - TTL inp (non-inv) with pull-down
B03N	3-state out - CMOS inp (inv)
B03U	3-state out - CMOS inp (inv) with pull-up
B03D	3-state out - CMOS inp (inv) with pull-down

Bidirectional Buffers (Continued)

B04N	3-state out - CMOS inp (non-inv)
B04U	3-state out - CMOS inp (non-inv) with pull-up
B04D	3-state out - CMOS inp (non-inv) with pull-down
B05N	3-state out - Schmitt trig inp (non-inv)
B05U	3-state out - Schmitt trig inp (non-inv) with pull-up
B05D	3-state out - Schmitt trig inp (non-inv) with pull-down

Output Buffers

Y01N	Output only (non-inv)
Y02N	Open drain output
Y03N	Short ckt output

Input Buffers

I01N	TTL input (non-inv)
I01U	TTL input (non-inv) with pull-up
I01D	TTL input (non-inv) with pull-down
I02N	CMOS input (inv)
I02U	CMOS input (inv) with pull-up
I02D	CMOS input (inv) with pull-down
I03N	CMOS input (non-inv)
I03U	CMOS input (non-inv) with pull-up
I03D	CMOS input (non-inv) with pull-down
I04N	Short ckt input
I04U	Short ckt input with pull-up
I04D	Short ckt input with pull-down
I05N	Schmitt trigger input (non-inv)
I05U	Schmitt trigger input (non-inv) with pull-up
I05D	Schmitt trigger input (non-inv) with pull-down
I06N	Schmitt trig clk driver input (n-i)
I06U	Schmitt trig clk driver input (n-i) with pull-up
I06D	Schmitt trig clk driver input (n-i) with pull-down
I07N	Clock buffer input (inv)
I07U	Clock buffer input (inv) with pull-up
I07D	Clock buffer input (inv) with pull-down
I08N	Clock buffer input (n-i)
I08U	Clock buffer input (n-i) with pull-up
I08D	Clock buffer input (n-i) with pull-down

Buffers/Inverters

C007	Triple inverting buffer
C008	Quad inverter
C009	Dual 3-state inverter buffer
C010	3-state non-inverting buffer

Gates

C001	Triple 2-input NAND
C002	Dual 3-input NAND
C003	Dual 2-input NAND/AND
C004	Triple 2-input NOR
C005	Dual 3-input NOR
C006	Dual 2-input NOR/OR
C017	Triple 4-input NAND
C019	Triple 3-input NAND/AND
C020	Triple 4-input NOR
C022	Triple 3-input NOR/OR
C053	2-input X-OR buffer
C054	2-input 2-wide OR-AND/invert
C055	2-input 2-wide AND-OR/invert
C057	5-input NAND/AND
C058	5-input NOR/OR

Latches

C012	NAND latch and 2-input NAND
C013	NOR latch and 2-input NOR
C026	D latch with reset (L) and enable (L)
C027	Triple NAND latch
C031	Triple NOR latch

Flip-Flops

C034	Parallel load D F/F with reset (L)
C035	Multiplexed D F/F with reset (L)
C036	Toggle enable F/F with reset (L)
C037	J-K F/F with reset and set
C059	Buffered D F/F
C060	D F/F with reset (L) and set (L)

Data Selectors/Multiplexers

C028	4-to-1 multiplexer with 3-state enable (L)
C029	4-to-1 data multiplexer
C056	2-to-1 multiplexer buffer

Decoders

C033	1-to-4 decoder with outputs (L) and 2 inverts

Shift Registers

C039	2-bit serial in/serial parallel out shift register
C042	2-bit serial/parallel shift register

Arithmetic Circuits

C032	Full adder
C040	1-bit ALU - 7 functions
C041	2-bit magnitude comparator

Miscellaneous Functions

C025	Schmitt trigger
C030	4-bit parity checker
C038	1-bit presettable up/down counter with set

Special Symbols

TRIBUS2	2-input tribus
TRIBUS3	3-input tribus
TRIBUS4	4-input tribus
TRIBUS5	5-input tribus
TRIBUS8	8-input tribus

Special Symbols (Continued)

TRIBUS16	16-input tribus
WIRED2	2-input wired output
WIRED3	3-input wired output
WIRED4	4-input wired output
WIRED5	5-input wired output
WIRED6	6-input wired output
WIRED7	7-input wired output
WIRED8	8-input wired output
PADIN	Input pad
PADOUT	Output pad

COMPONENT PIN SEQUENCES

The component filename consists of the macrocell number plus the extension .SYM; for example, H01.SYM.

B01N:	BPO	B	E	A	BPI
B01U:	BPO	B	E	A	BPI
B01D:	BPO	B	E	A	BPI
B02N:	BPO	B	E	A	BPI
B02U:	BPO	B	E	A	BPI
B02D:	BPO	B	E	A	BPI
B03N:	BPO	B	E	A	BPI
B03U:	BPO	B	E	A	BPI
B03D:	BPO	B	E	A	BPI
B04N:	BPO	B	E	A	BPI
B04U:	BPO	B	E	A	BPI
B04D:	BPO	B	E	A	BPI
B05N:	BPO	B	E	A	BPI
B05U:	BPO	B	E	A	BPI
B05D:	BPO	B	E	A	BPI
Y01N:	BPO	A			
Y02N:	BPO	A			
Y03N:	BPO	A			
I01N:	A	BPI			
I01U:	A	BPI			
I01D:	A	BPI			
I02N:	A	BPI			

I02U:	A	BPI		
I02D:	A	BPI		
I03N:	A	BPI		
I03U:	A	BPI		
I03D:	A	BPI		
I04N:	A	BPI		
I04U:	A	BPI		
I04D:	A	BPI		
I05N:	A	BPI		
I05U:	A	BPI		
I05D:	A	BPI		
I06N:	A	BPI		
I06U:	A	BPI		
I06D:	A	BPI		
I07N:	A	BPI		
I07U:	A	BPI		
I07D:	A	BPI		
I08N:	A	BPI		
I08U:	A	BPI		
I08D:	A	BPI		
C001:	C	A	B	
C002:	D	A	B	C
C003:	C	D	A	B
C004:	C	A	B	
C005:	D	A	B	C
C006:	C	D	A	B

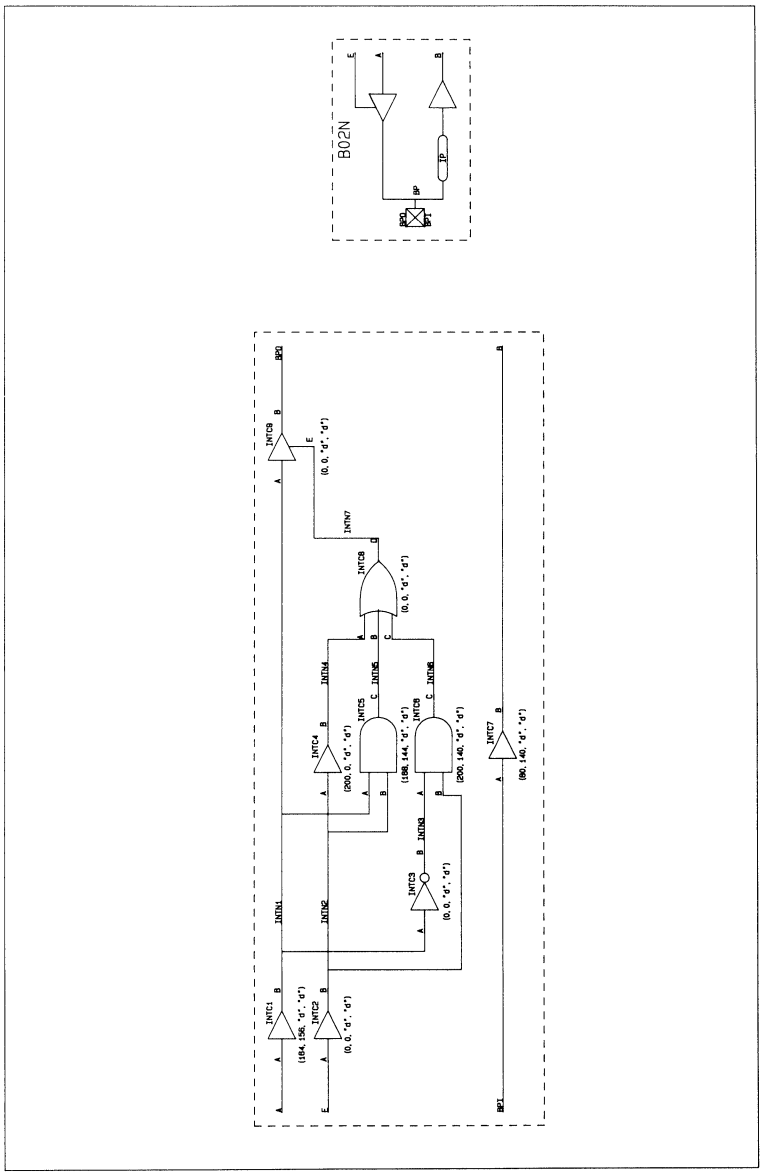
C007:	B	A					
C008:	B	A					
C009:	B	A	EB				
C010:	B	A	E				
C012:	C	Q	QB	A	B	SB	RB
C013:	C	Q	QB	A	B	R	S
C017:	E	A	B	C	D		
C019:	D	E	A	B	C		
C020:	E	A	B	C	D		
C022:	D	E	A	B	C		
C025:	B	A					
C026:	Q	QB	D	EB	RB		
C027:	Q	QB	SB	RB			
C028:	Y SL2	D0 SL3	D1 EB	D2	D3	SL0	SL1
C029:	Y SLA	YB SLB	D0	D1	D2	D3	
C030:	Y	A	B	C	D	EO	
C031:	Q	QB	R	S			
C032:	CO	SM	A	B	CI		
C033:	Y0B	Y1B	Y2B	Y3B	A	B	EB
C034:	Q	QB	PEB	PD	D	CK	R
C035:	Q	QB	D0	D1	SL	CK	R
C036:	Q	QB	CK	TE	RB		
C037:	Q	QB	S	J	CK	K	R
C038:	Q MD	TOB	S	PD	PEB	CK	TIB

C039:	Q0	Q1	DO	D	CK	R	
C040:	CO	FO	CF3	A	B	F1	F2
C041:	AGO AGI	AEO AEI	ALO ALI	A1	B1	A0	B0
C042:	Q0 PD1	Q1	DO	DI	CK	PEB	PD0
C053:	C	A	B				
C054:	E	F	A	B	C	D	
C055:	E	F	A	B	C	D	
C056:	C	A	SL	B			
C057:	F	G	A	B	C	D	E
C058:	F	G	A	B	C	D	E
C059:	Q	QB	D	CK			
C060:	Q	QB	SB	D	CK	RB	
TRIBUS2:	OUT	IN1	IN2				
TRIBUS3:	OUT	IN1	IN2	IN3			
TRIBUS4:	OUT	IN1	IN2	IN3	IN4		
TRIBUS5:	OUT	IN1	IN2	IN3	IN4	IN5	
TRIBUS8:	OUT IN7	IN1 IN8	IN2	IN3	IN4	IN5	IN6
TRIBUS16:	OUT IN7 IN14	IN1 IN8 IN15	IN2 IN9 IN16	IN3 IN10	IN4 IN11	IN5 IN12	IN6 IN13
WIRED2:	OUT	IN1	IN2				
WIRED3:	OUT	IN1	IN2	IN3			
WIRED4:	OUT	IN1	IN2	IN3	IN4		
WIRED5:	OUT	IN1	IN2	IN3	IN4	IN5	
WIRED6:	OUT	IN1	IN2	IN3	IN4	IN5	IN6

WIRED7:	OUT	IN1	IN2	IN3	IN4	IN5	IN6
	IN7						
WIRED8:	OUT	IN1	IN2	IN3	IN4	IN5	IN6
	IN7	IN8					
PADIN:	OUT	IN					
PADOUT:	OUT	IN					

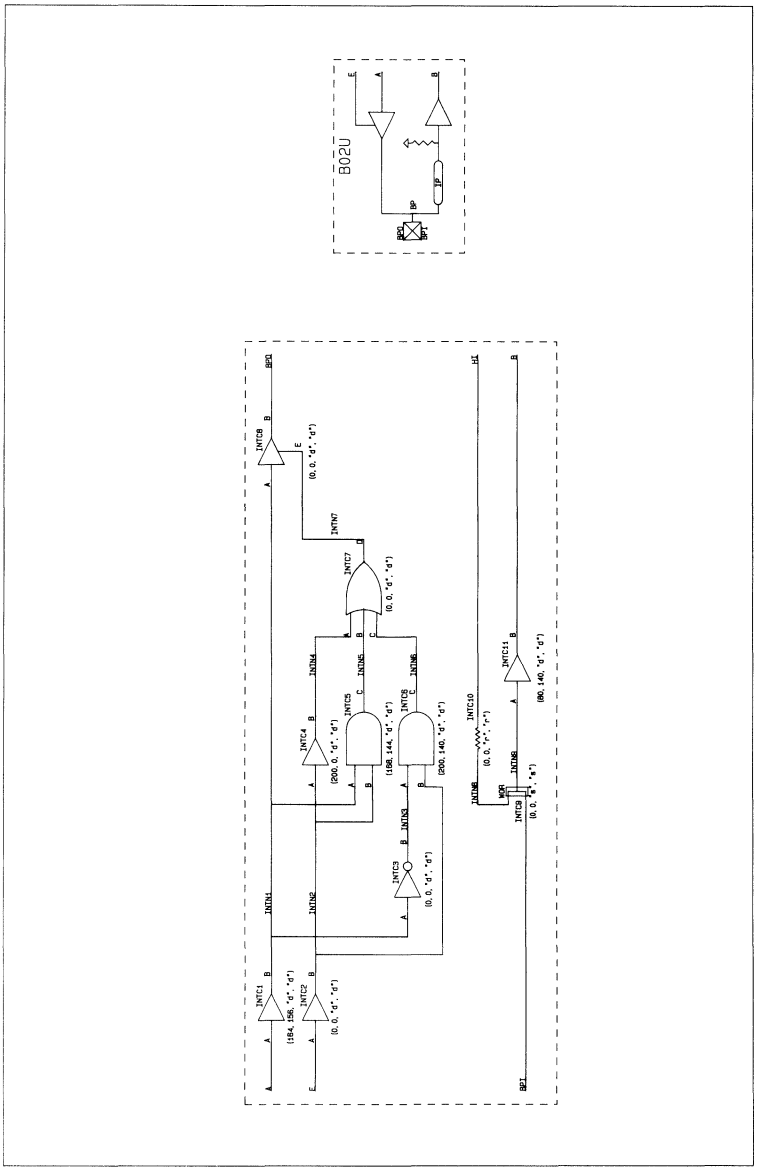
COMPONENT PLOTS

Plot 1



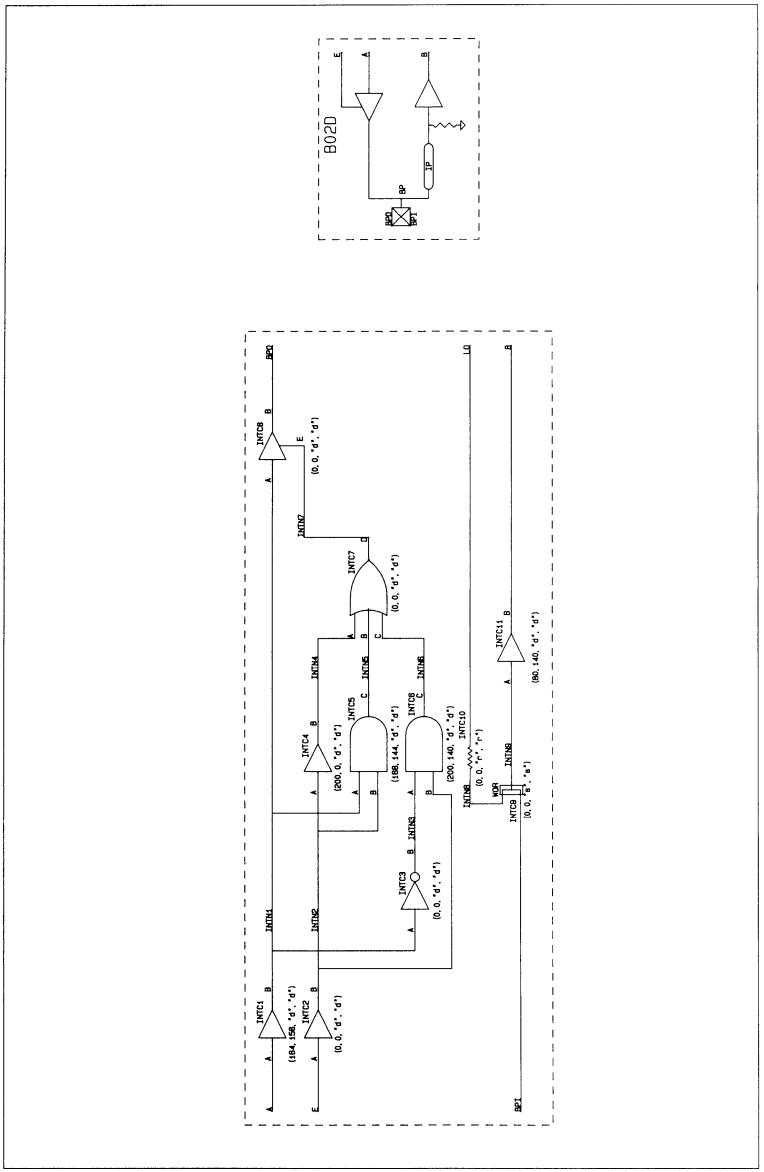
COMPONENT PLOTS

Plot 2



COMPONENT PLOTS

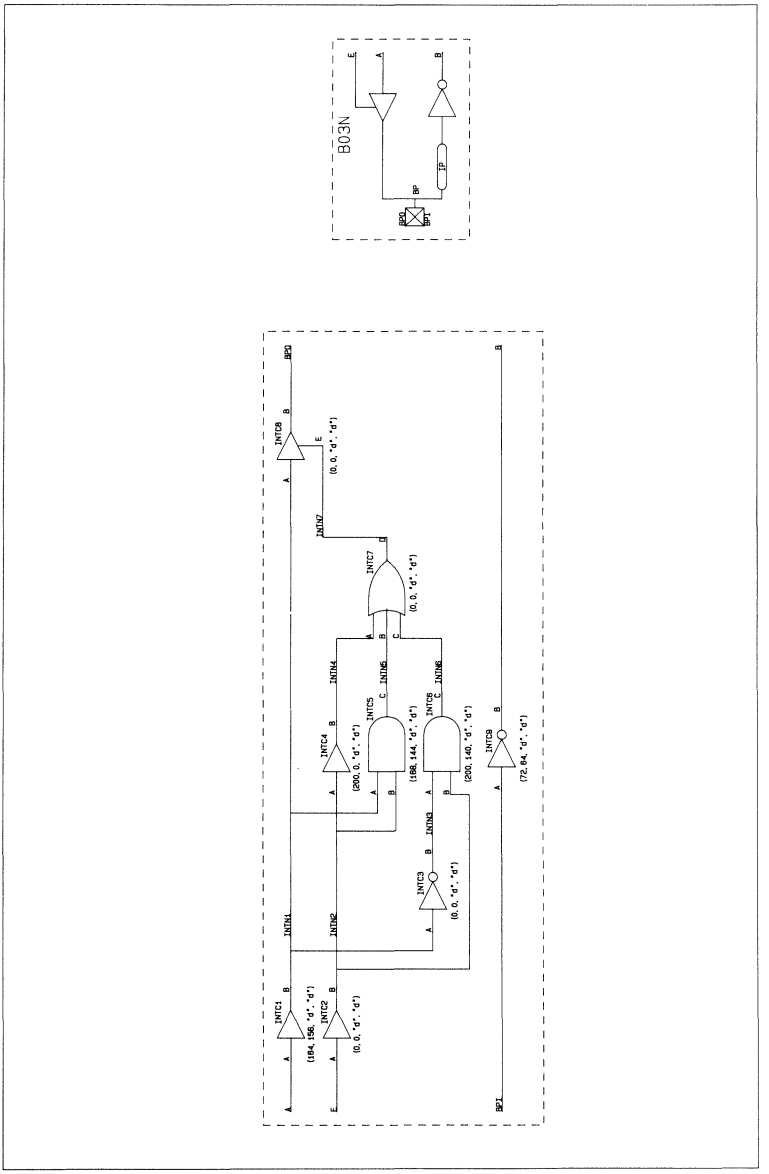
Plot 3



000-0144-00

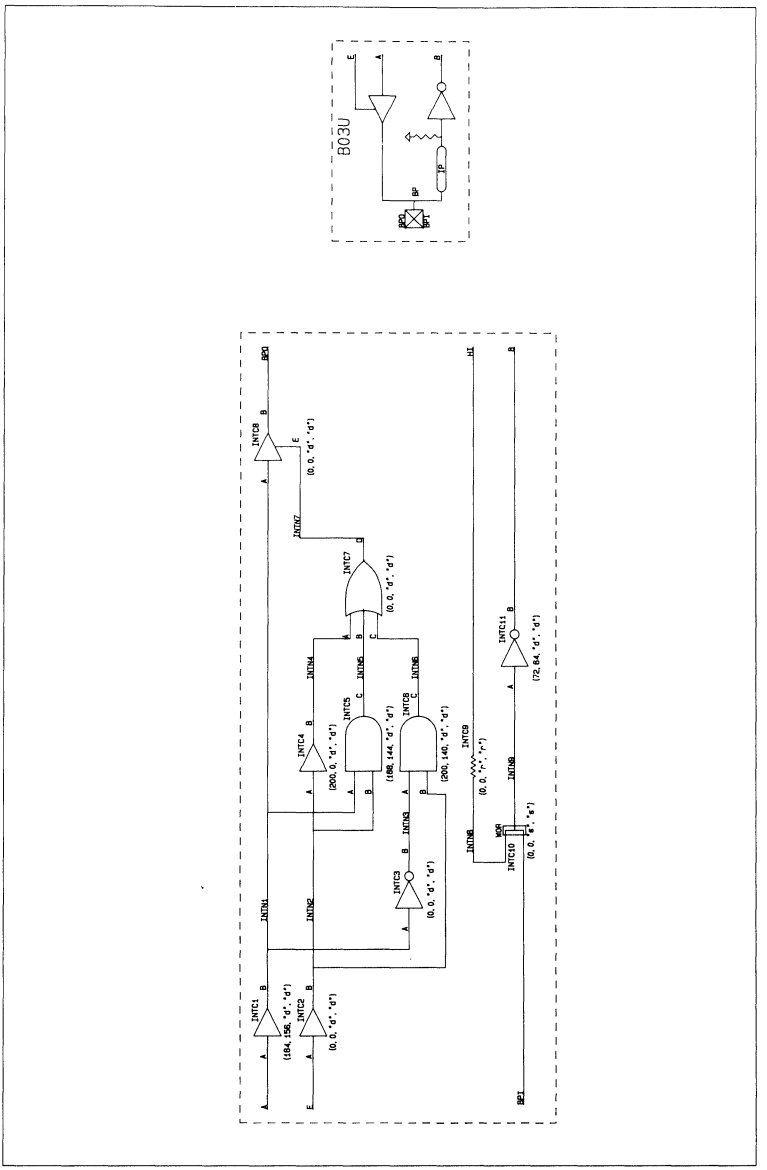
COMPONENT PLOTS

Plot 4



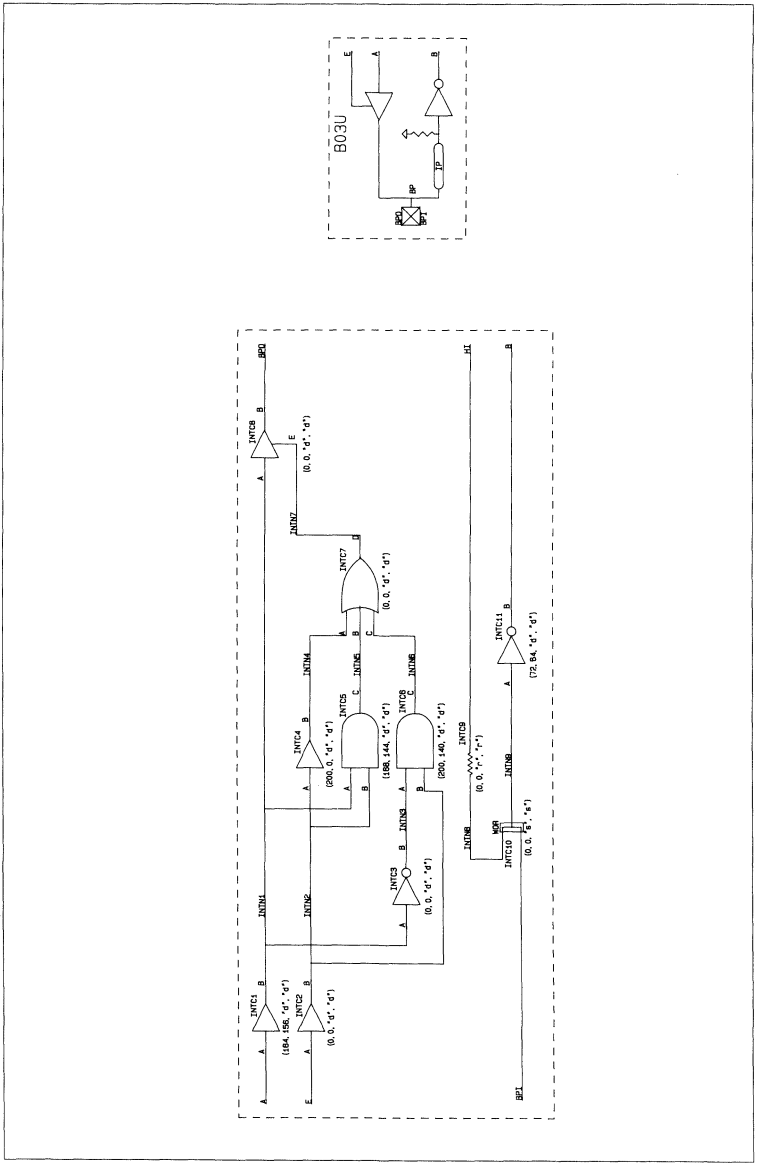
COMPONENT PLOTS

Plot 5



COMPONENT PLOTS

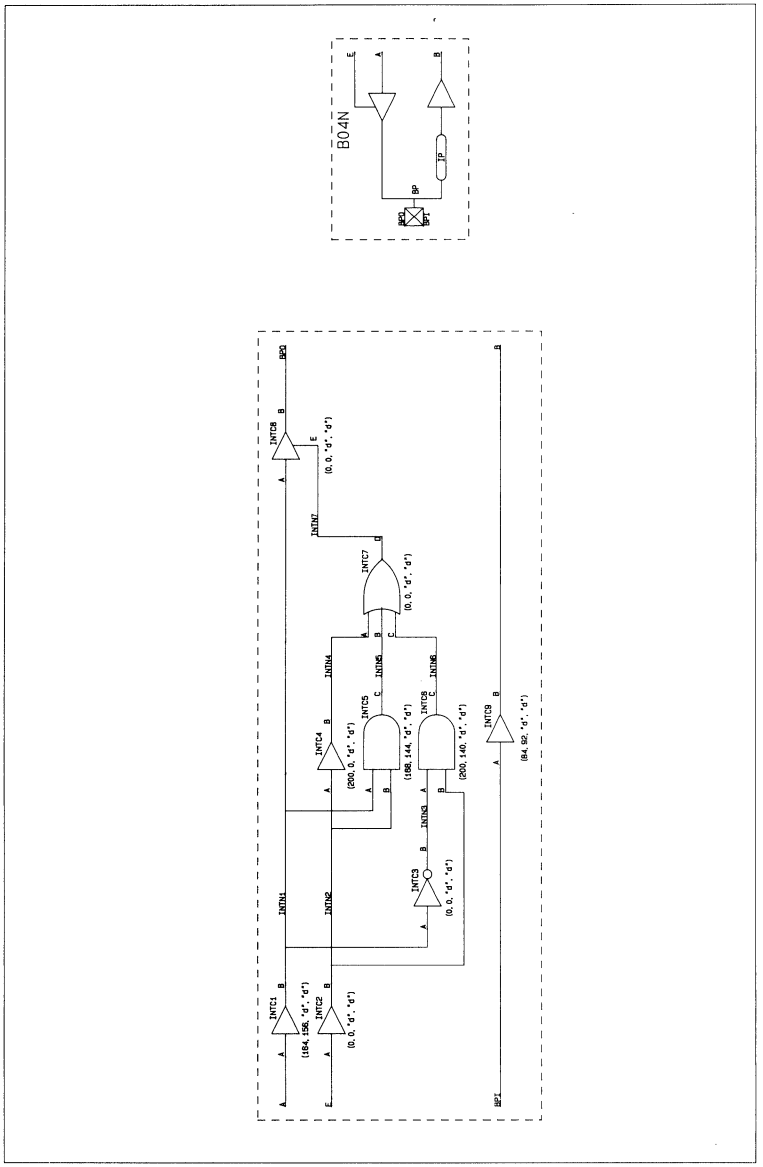
Plot 6



000-0144-00

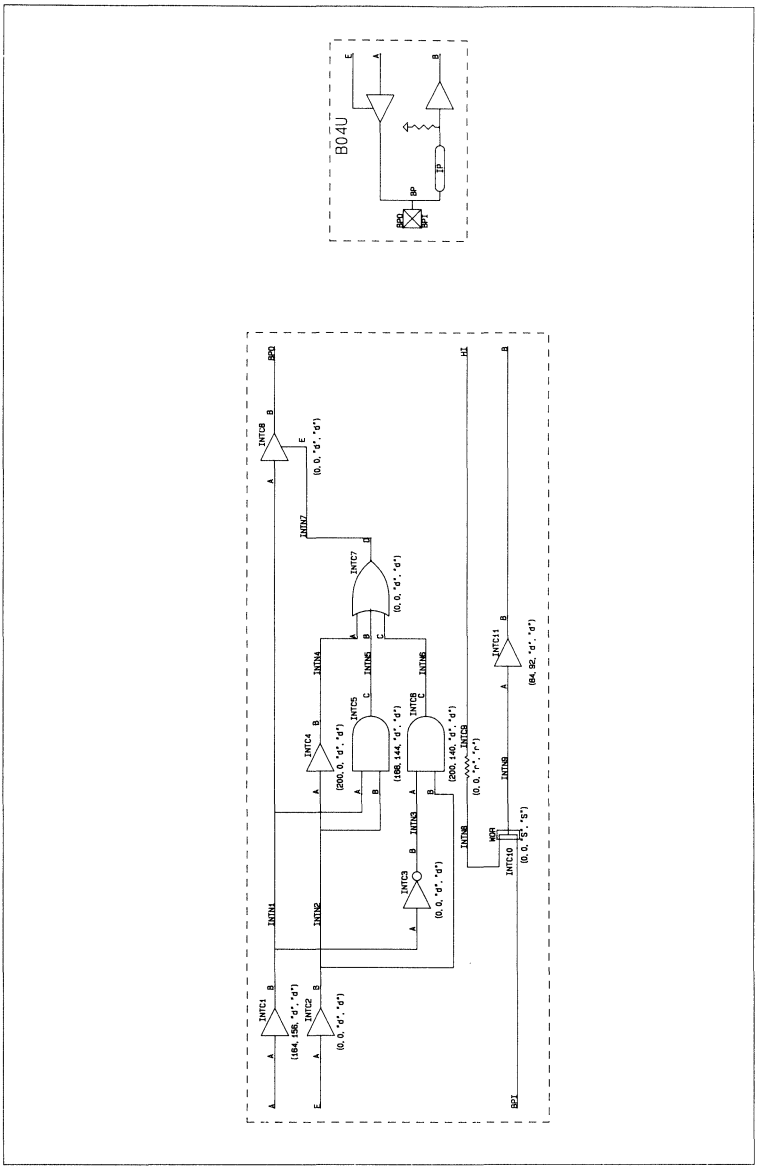
COMPONENT PLOTS

Plot 7



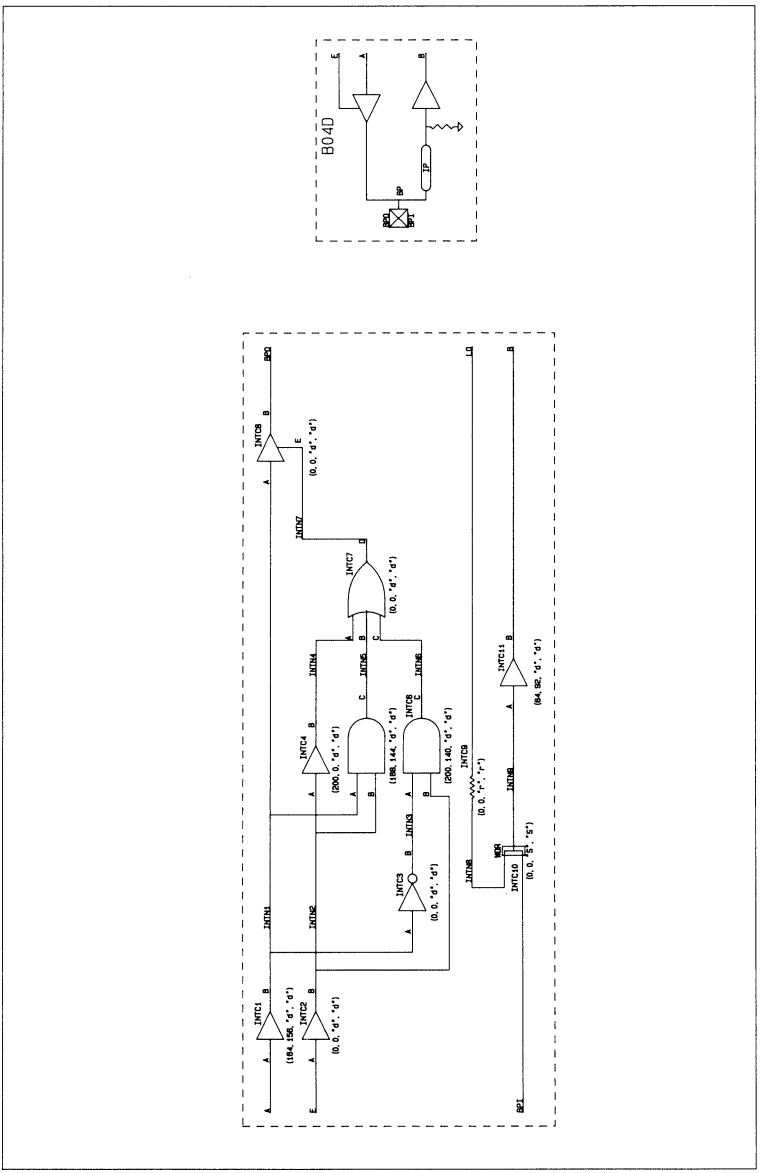
COMPONENT PLOTS

Plot 8



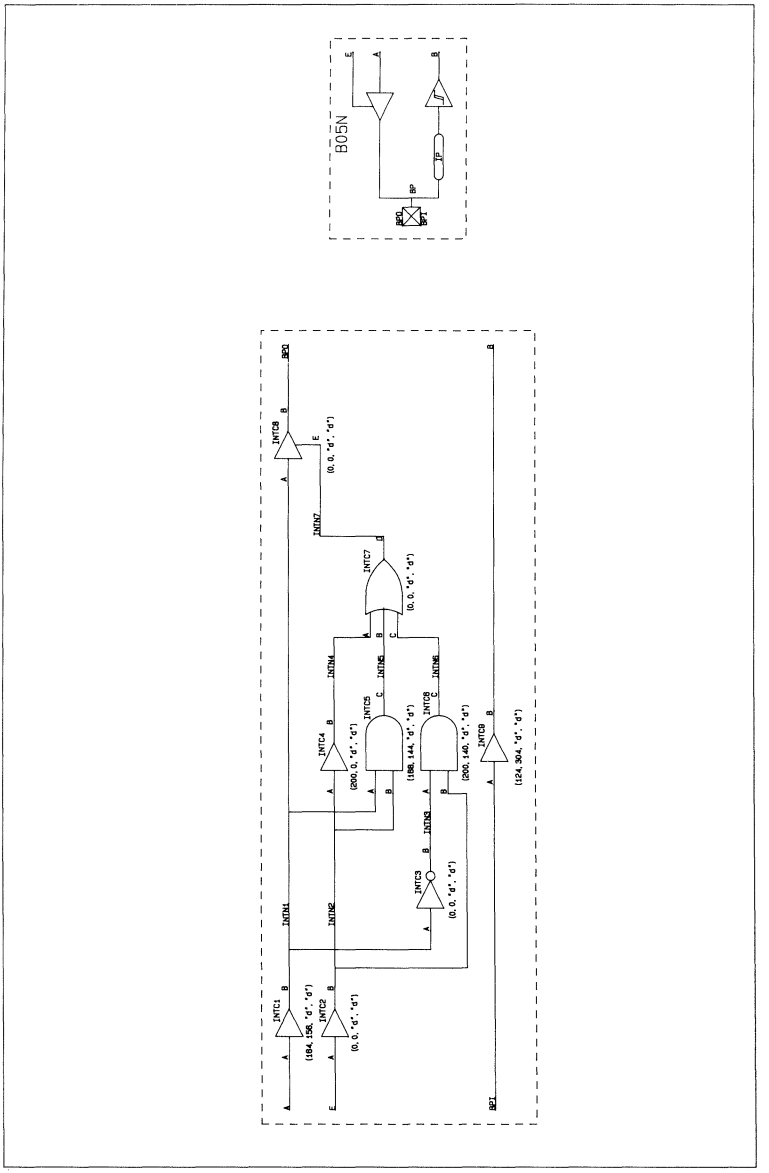
COMPONENT PLOTS

Plot 9



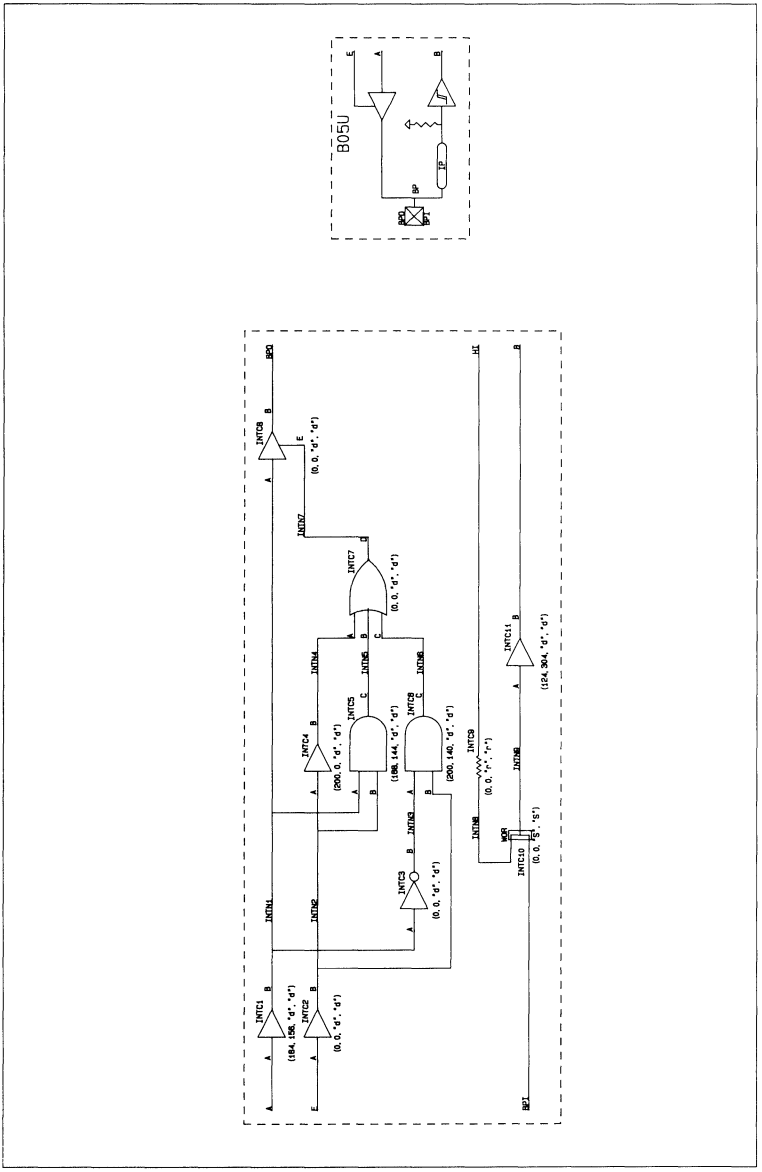
COMPONENT PLOTS

Plot 10



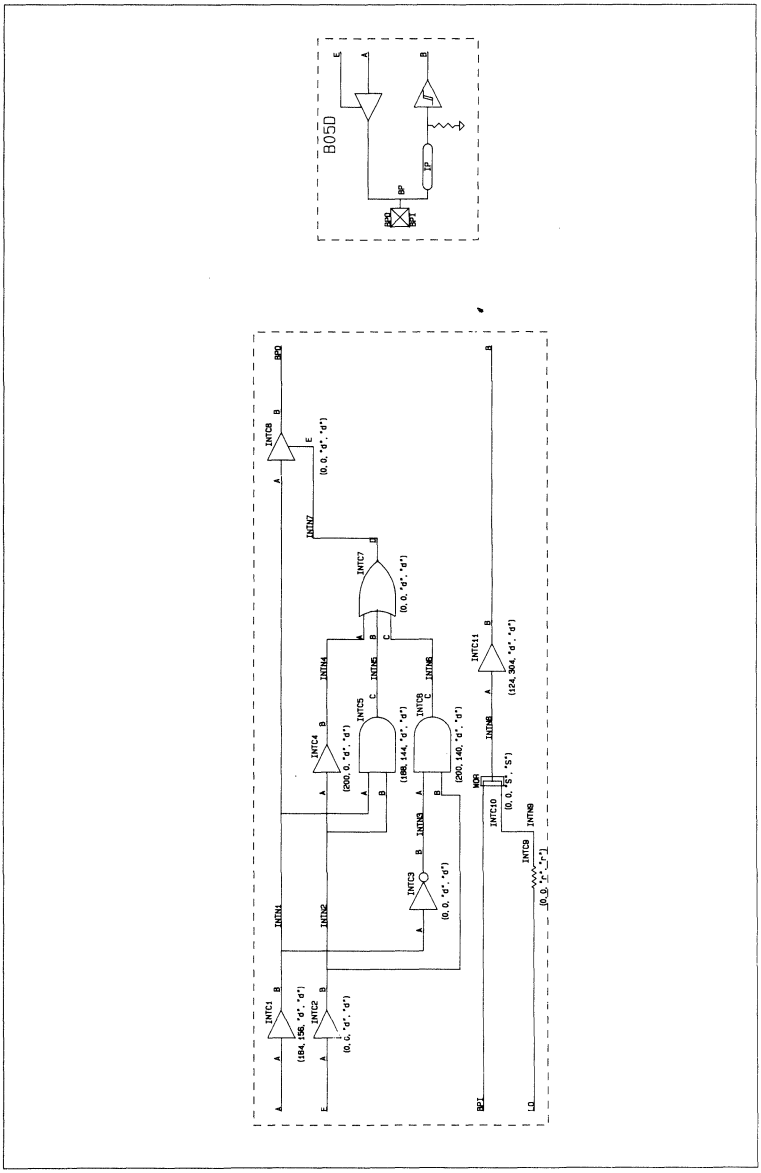
COMPONENT PLOTS

Plot 11



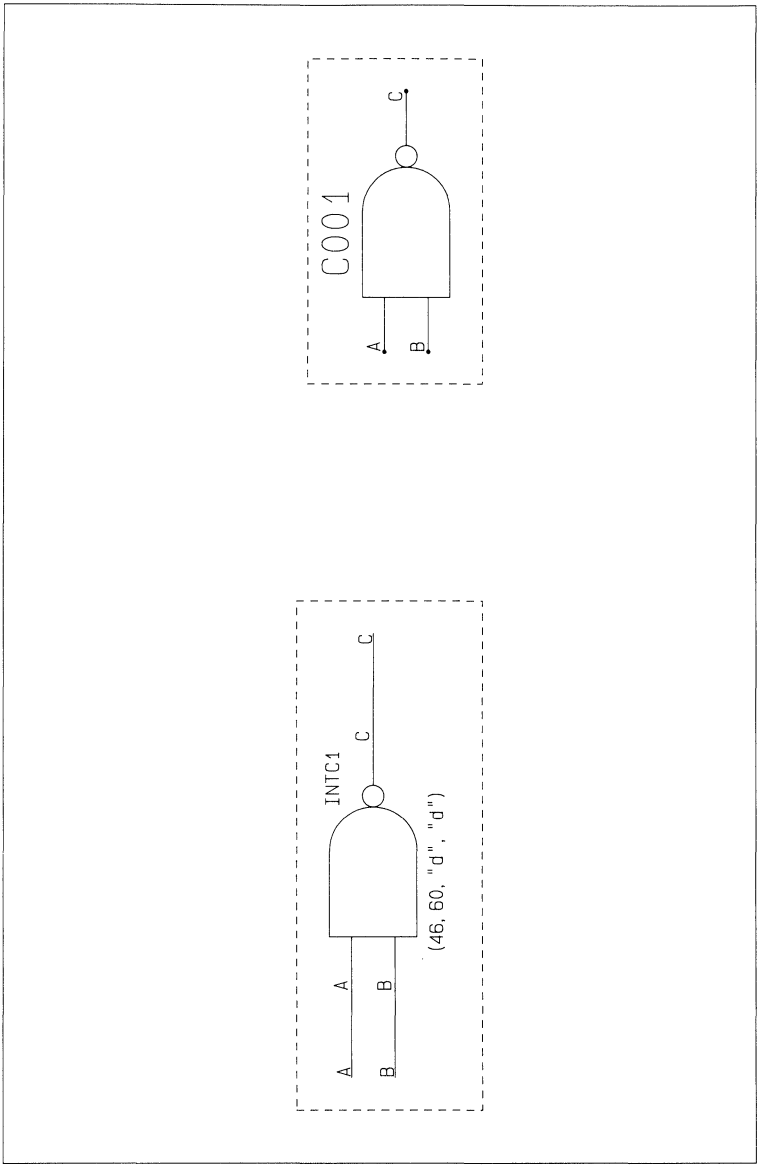
COMPONENT PLOTS

Plot 12



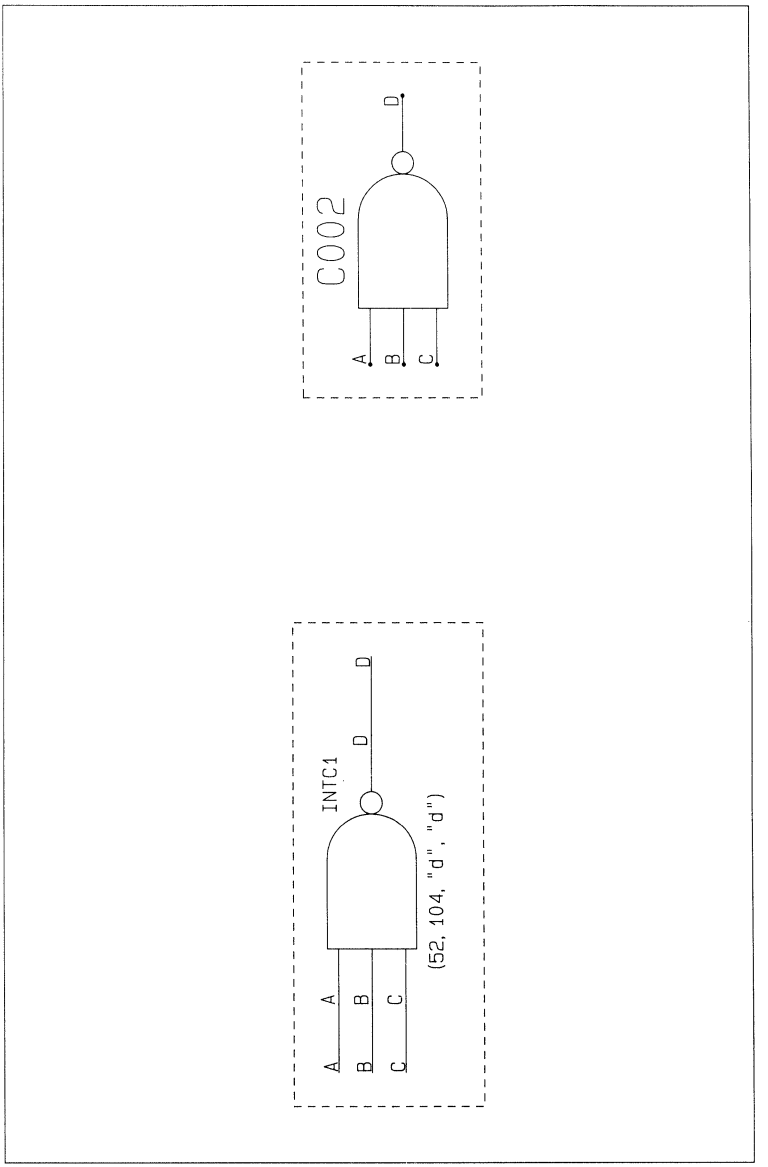
COMPONENT PLOTS

Plot 13



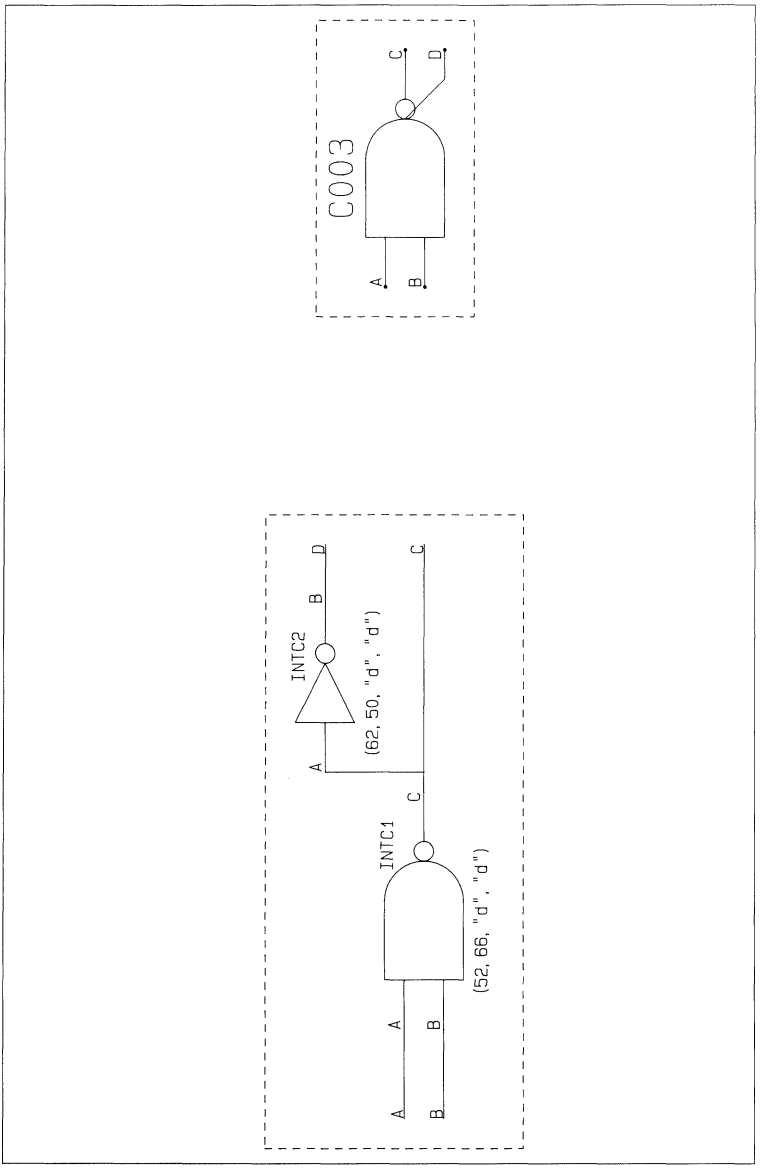
COMPONENT PLOTS

Plot 14



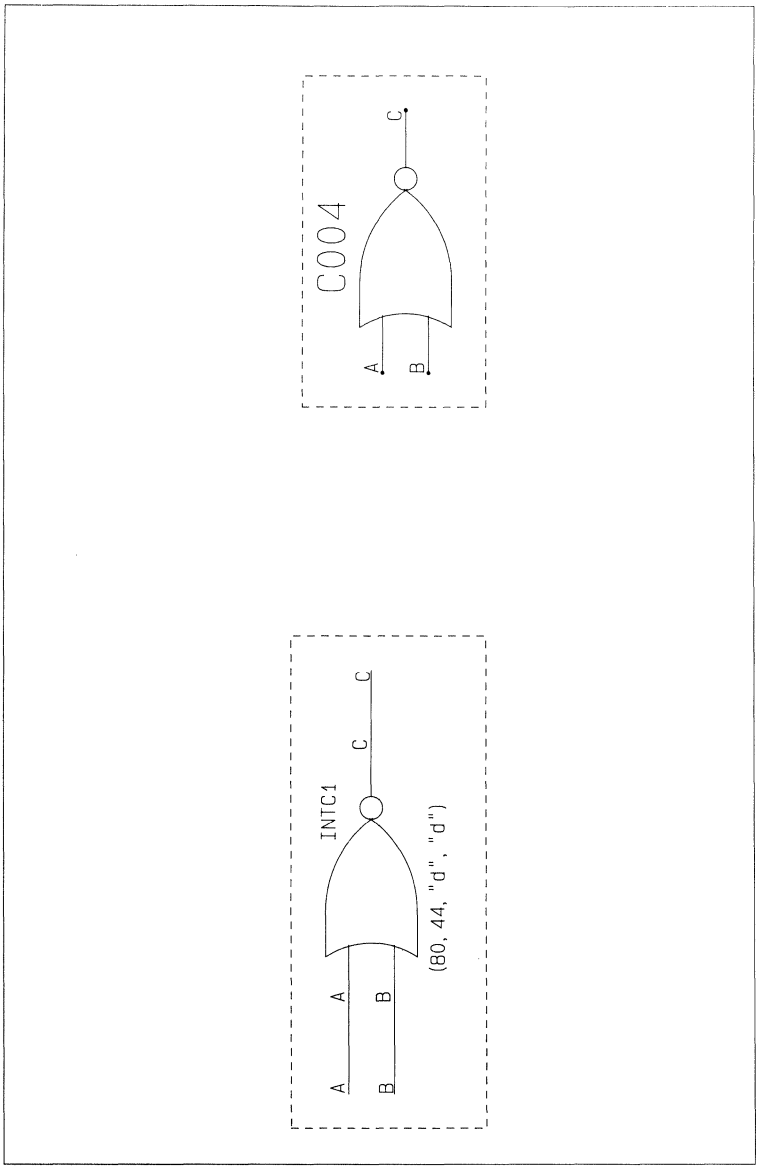
COMPONENT PLOTS

Plot 15



COMPONENT PLOTS

Plot 16



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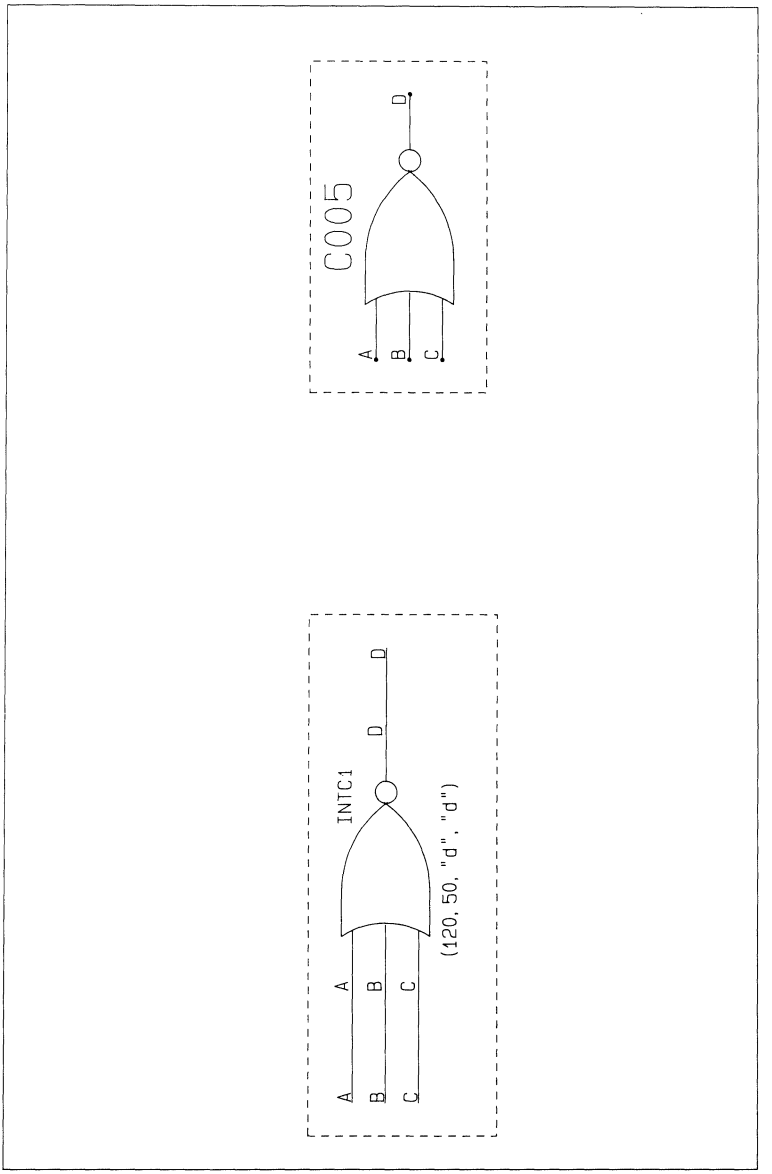
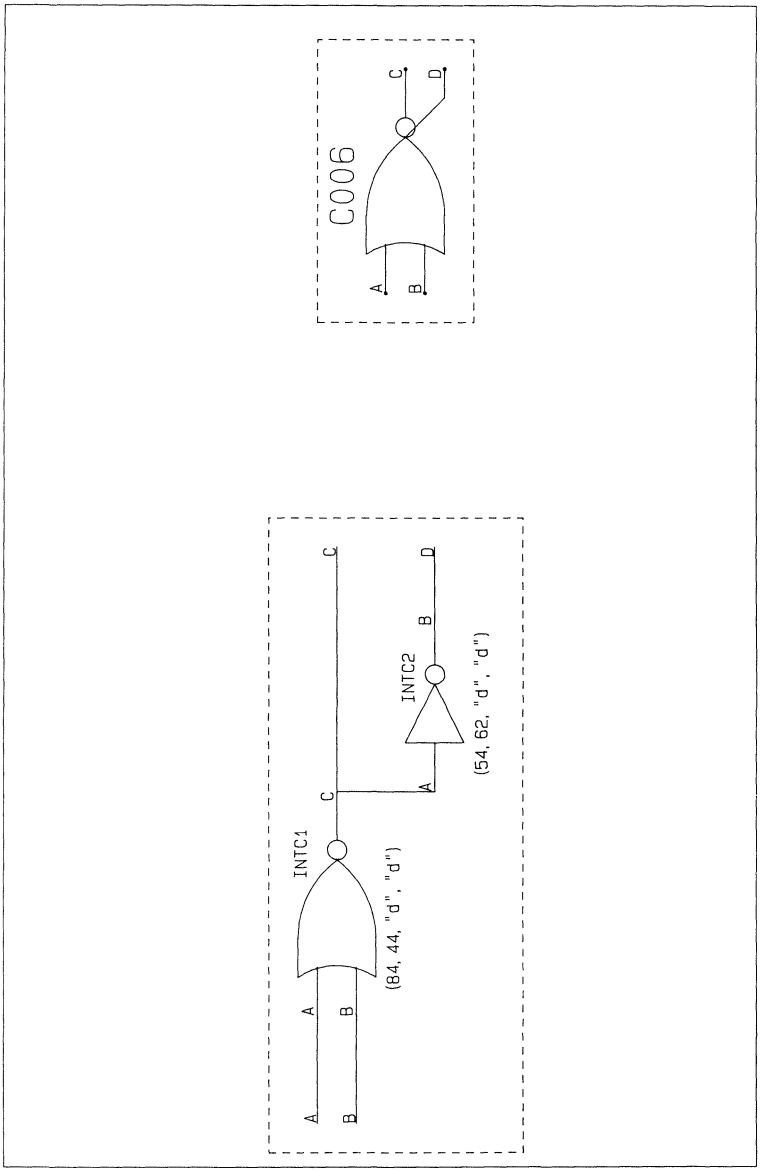
COMPONENT PLOTS

Plot 17



COMPONENT PLOTS

Plot 18



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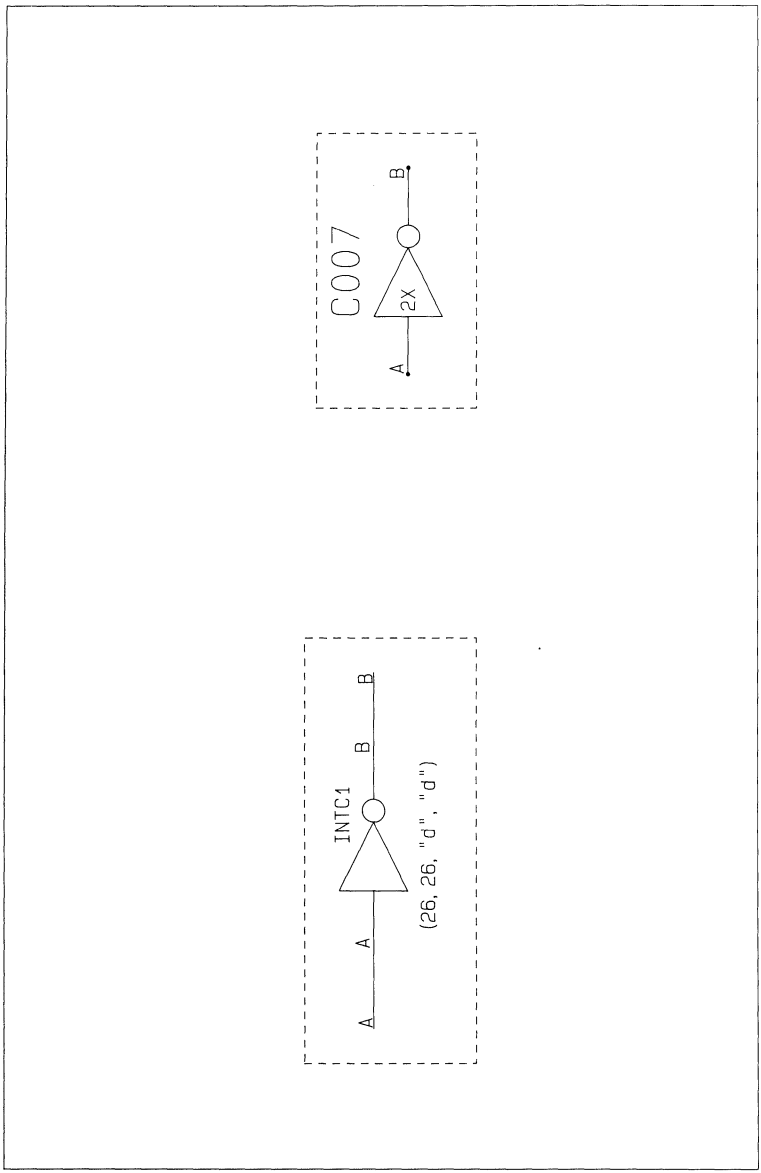
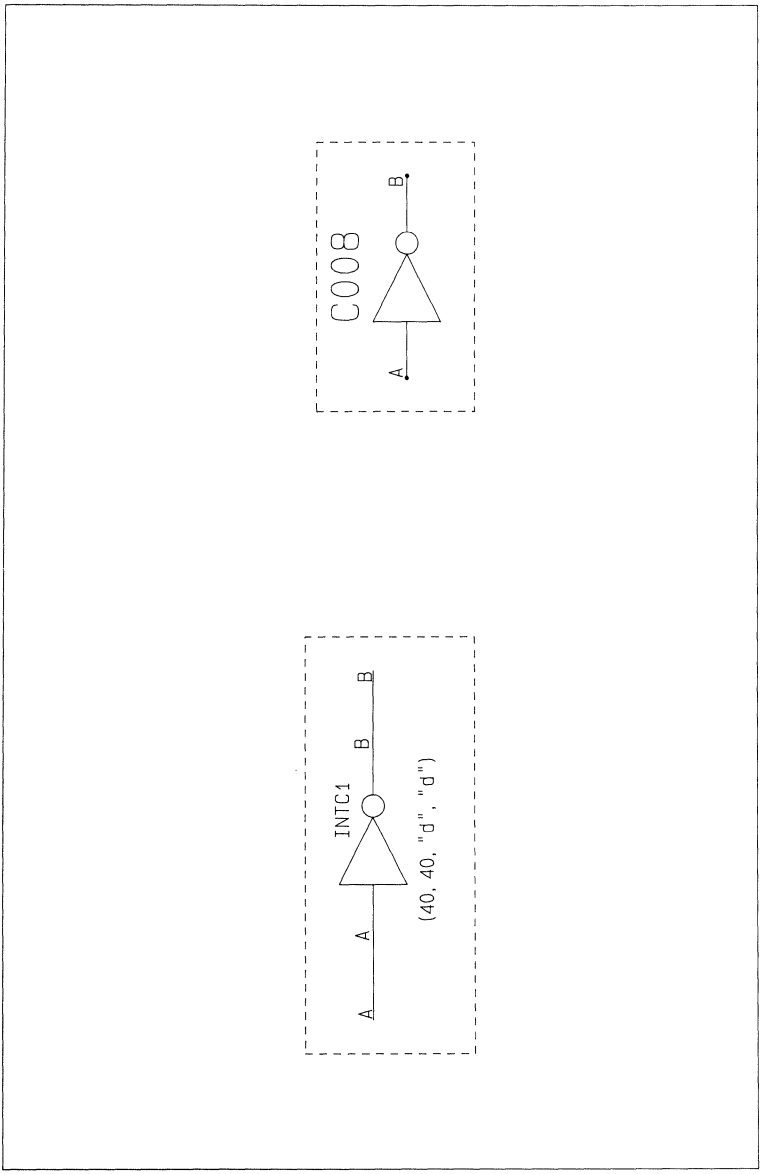
COMPONENT PLOTS

Plot 19



COMPONENT PLOTS

Plot 20



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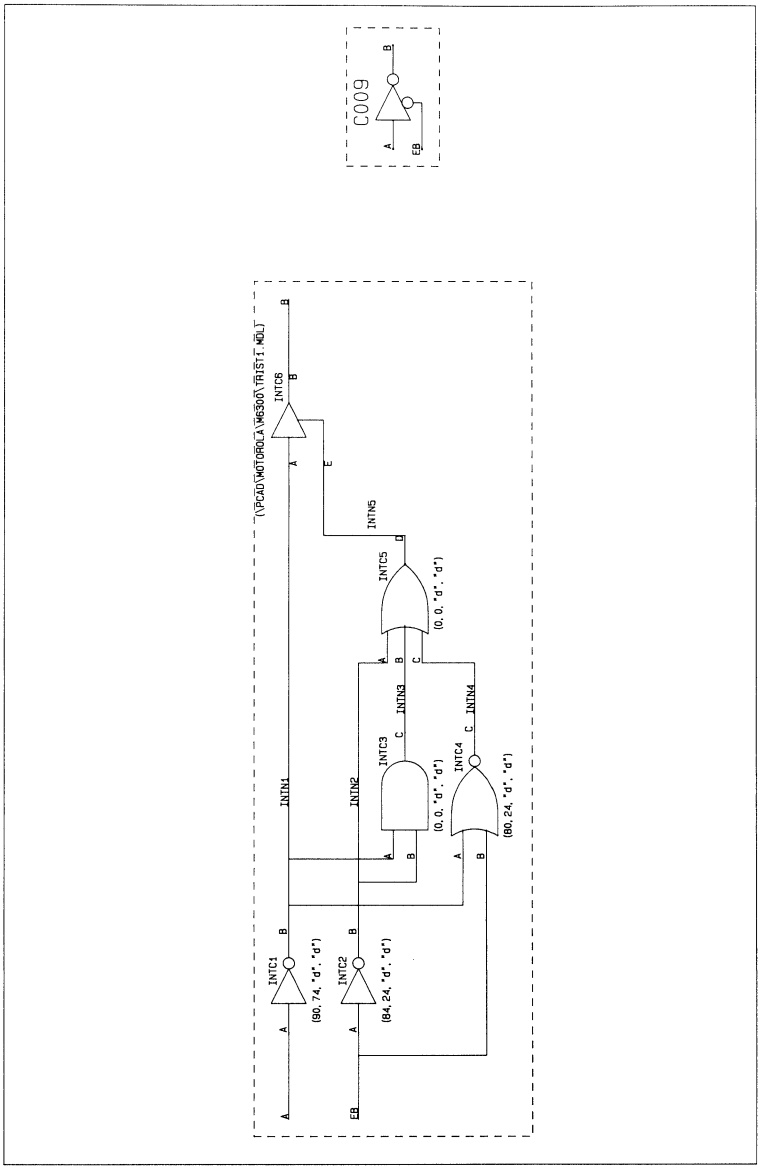
COMPONENT PLOTS

Plot 21



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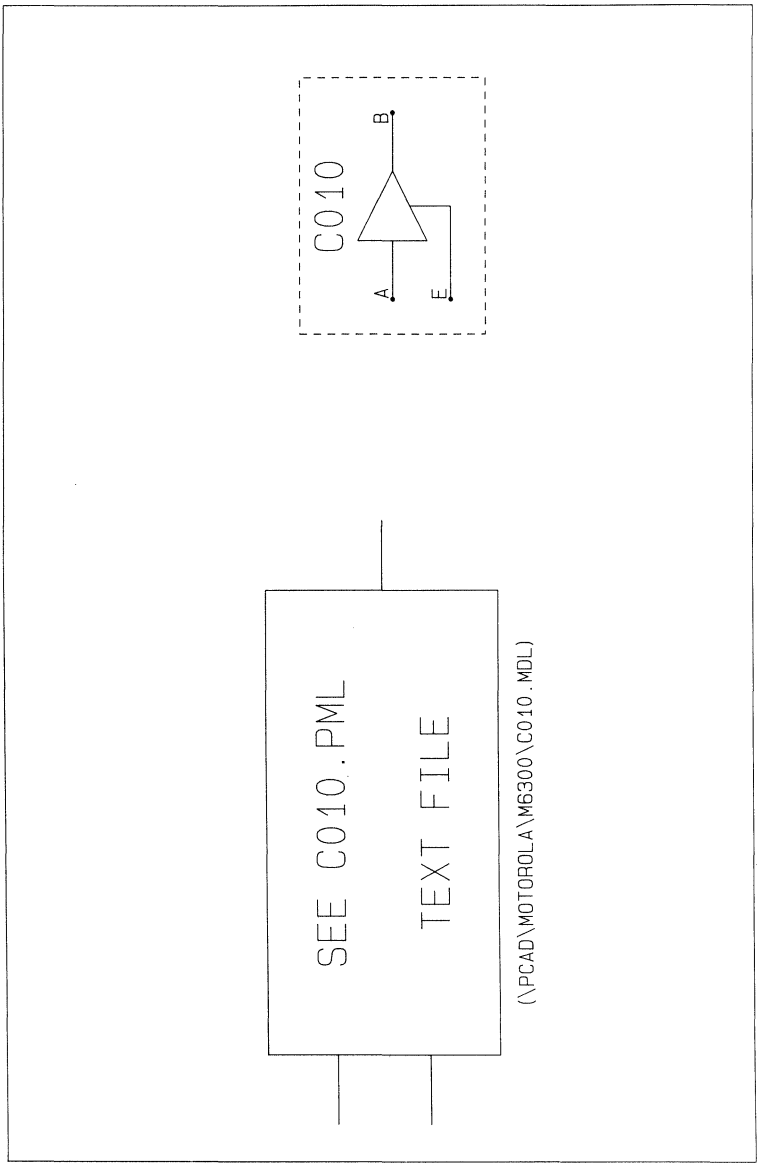
COMPONENT PLOTS

Plot 22



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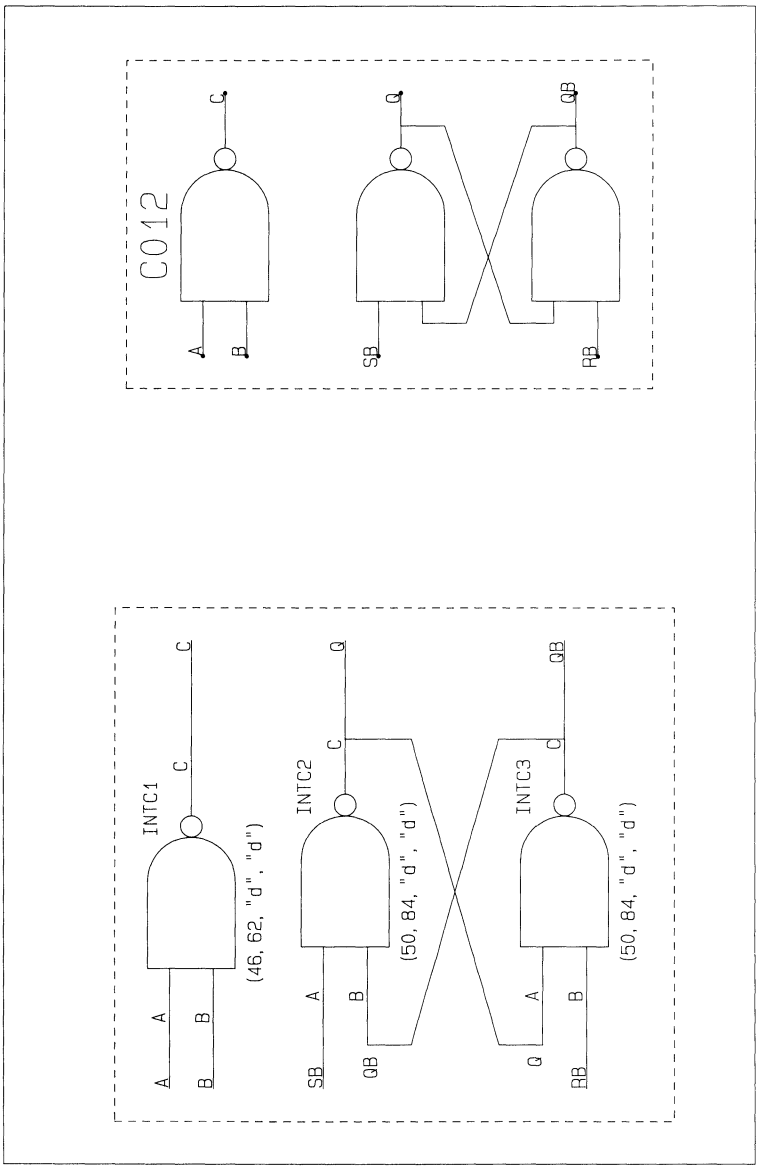
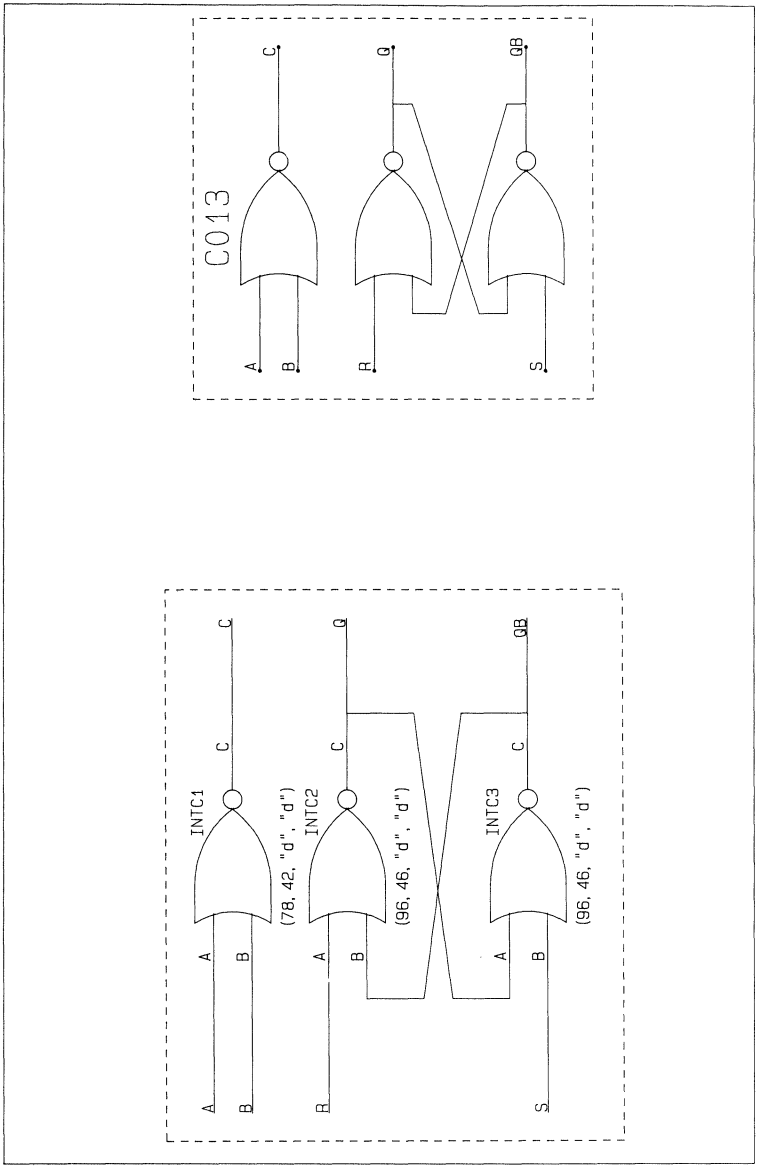
COMPONENT PLOTS

Plot 23



COMPONENT PLOTS

Plot 24



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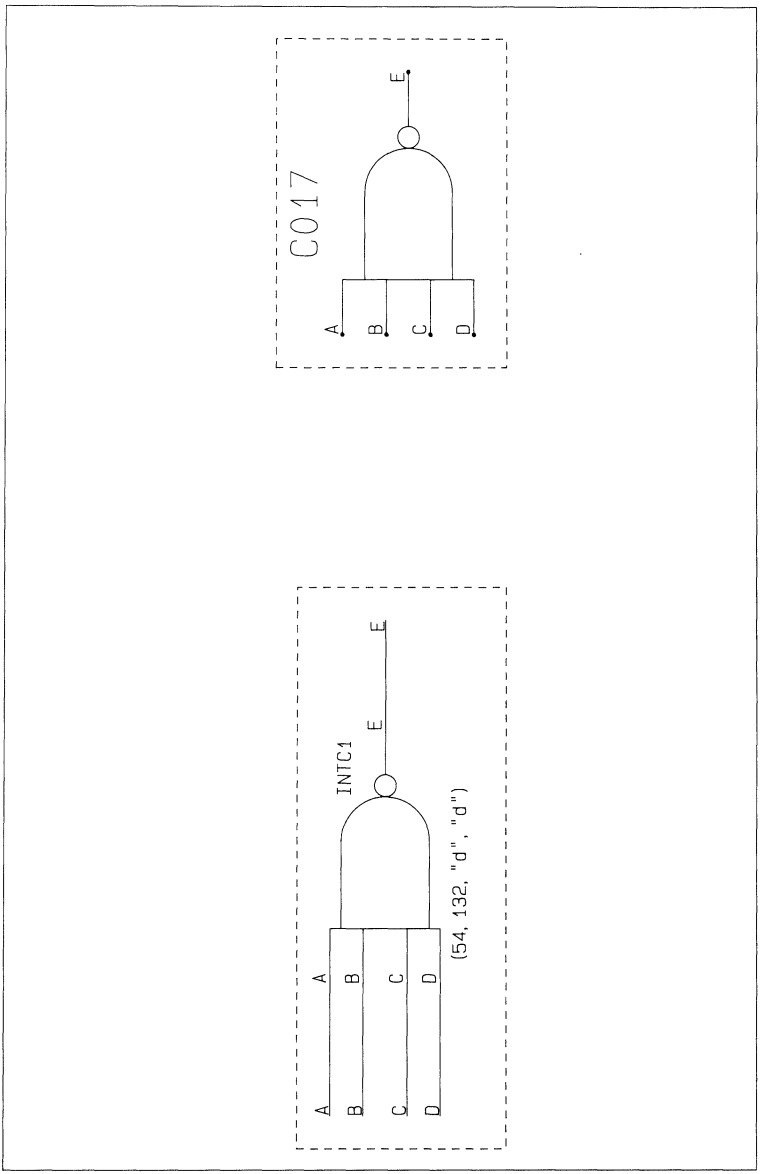
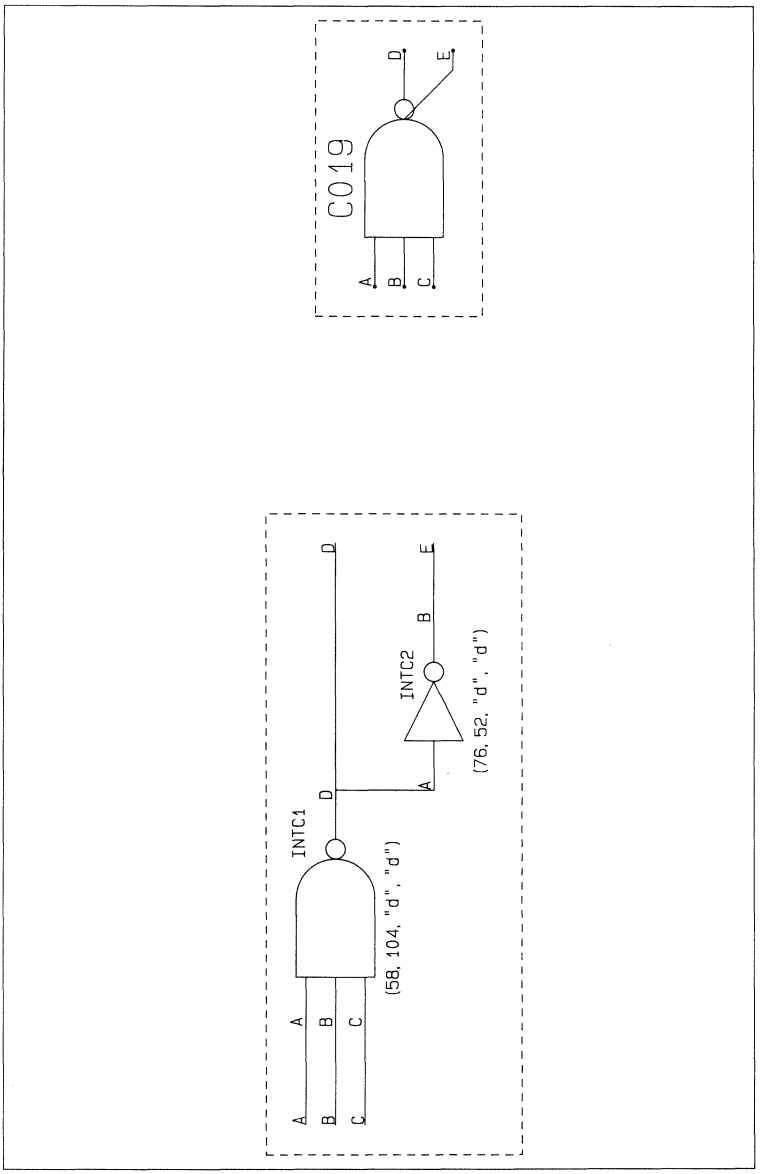
COMPONENT PLOTS

Plot 25



COMPONENT PLOTS

Plot 26



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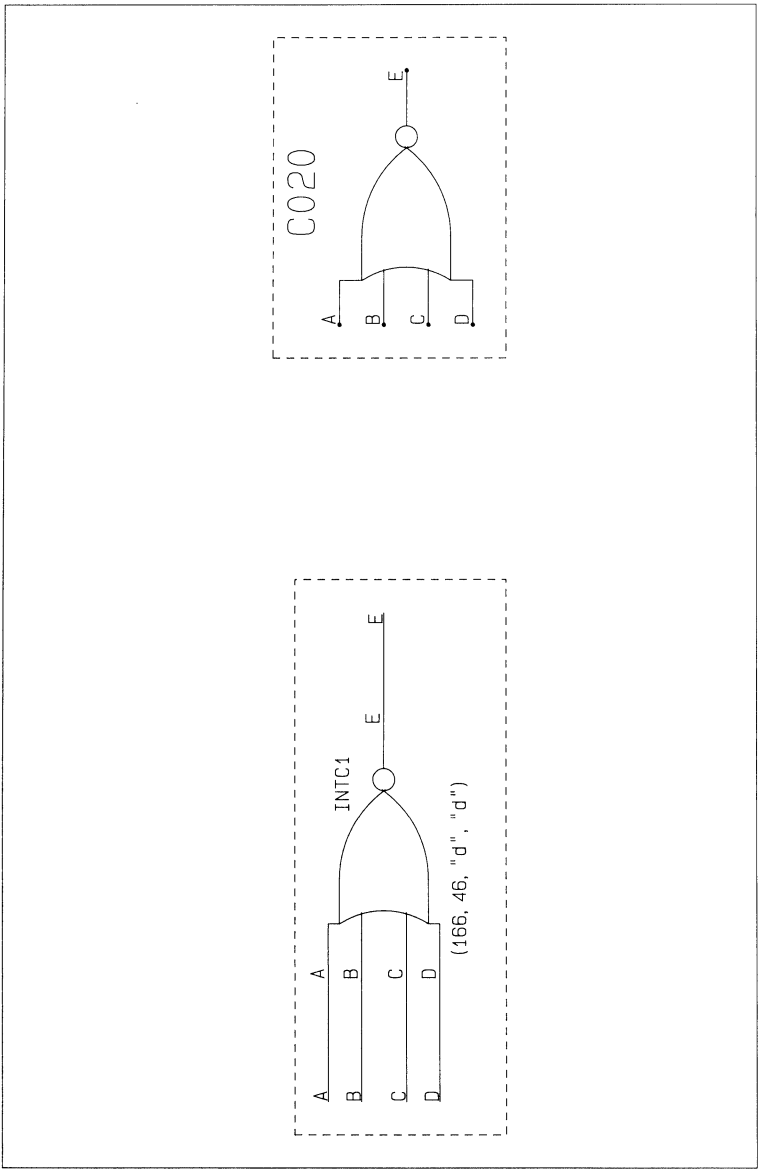
COMPONENT PLOTS

Plot 27



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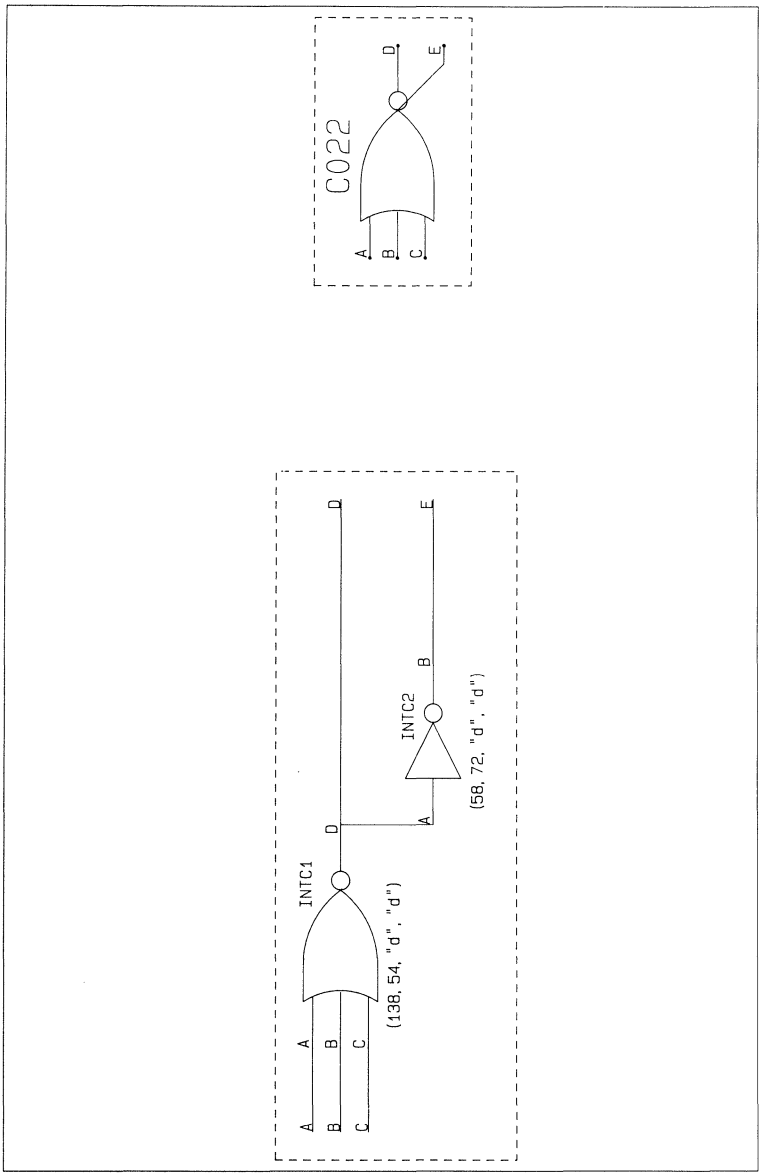
COMPONENT PLOTS

Plot 28



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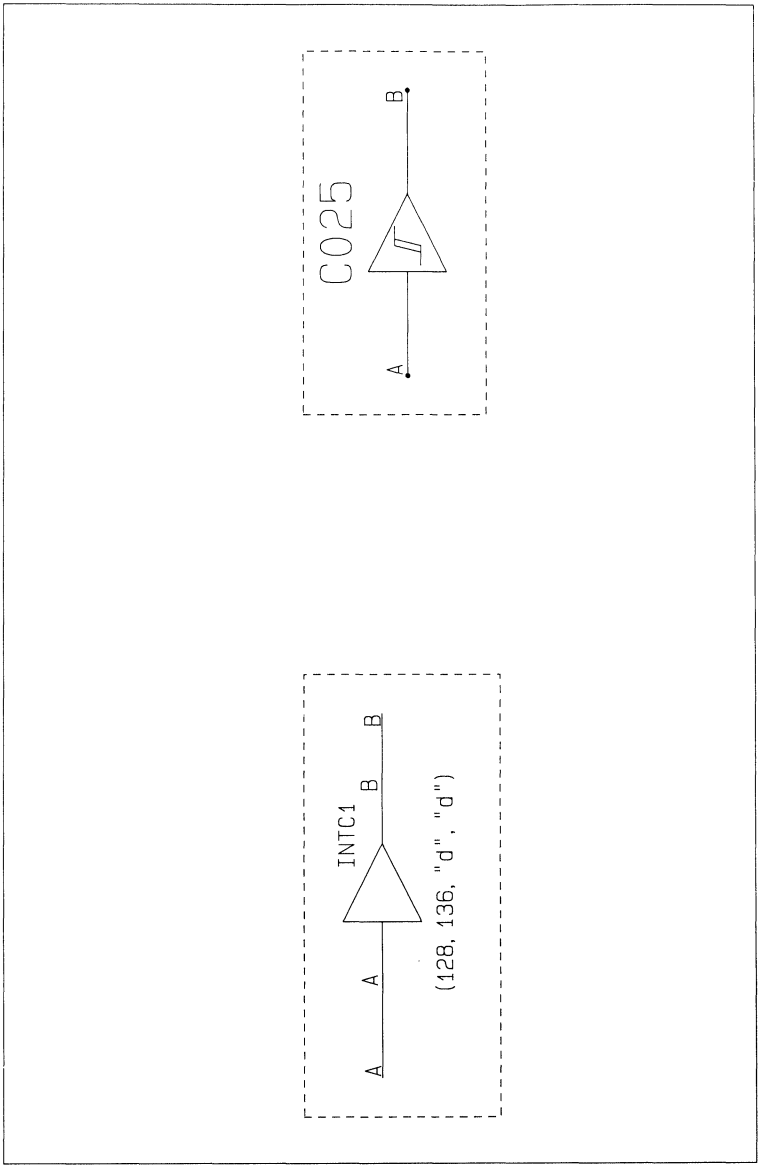
COMPONENT PLOTS

Plot 29



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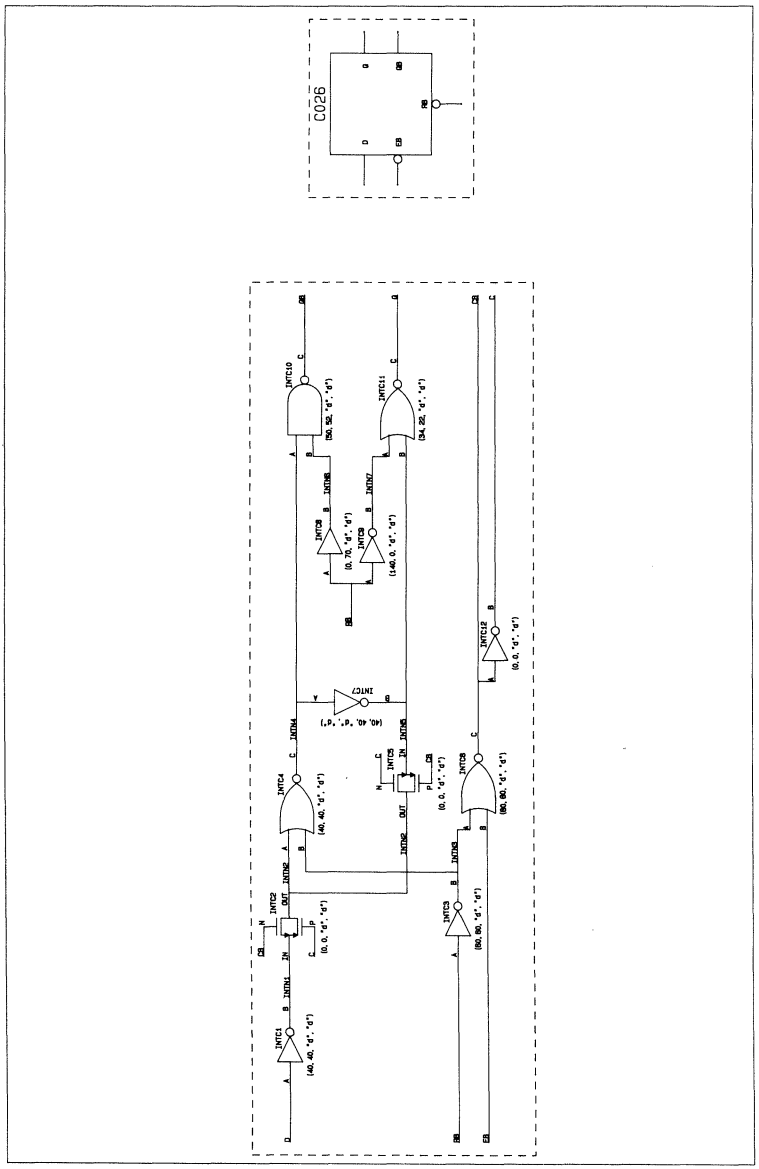
COMPONENT PLOTS

Plot 30



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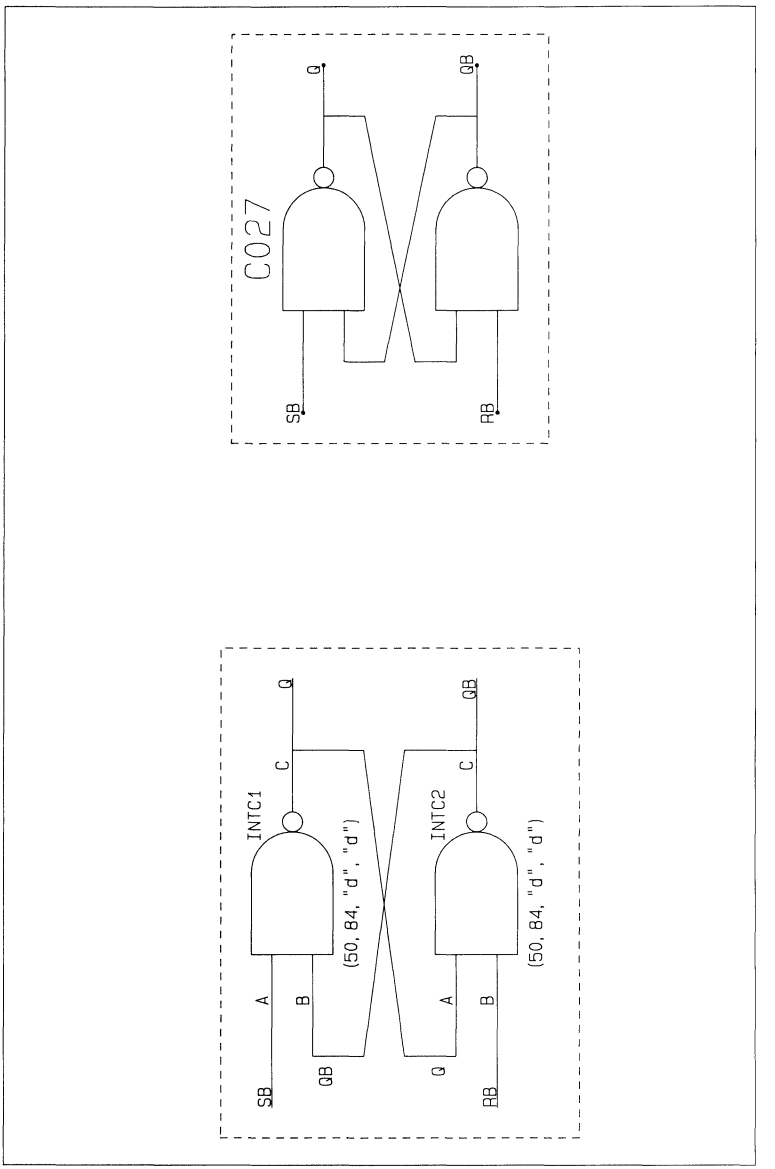
COMPONENT PLOTS

Plot 31



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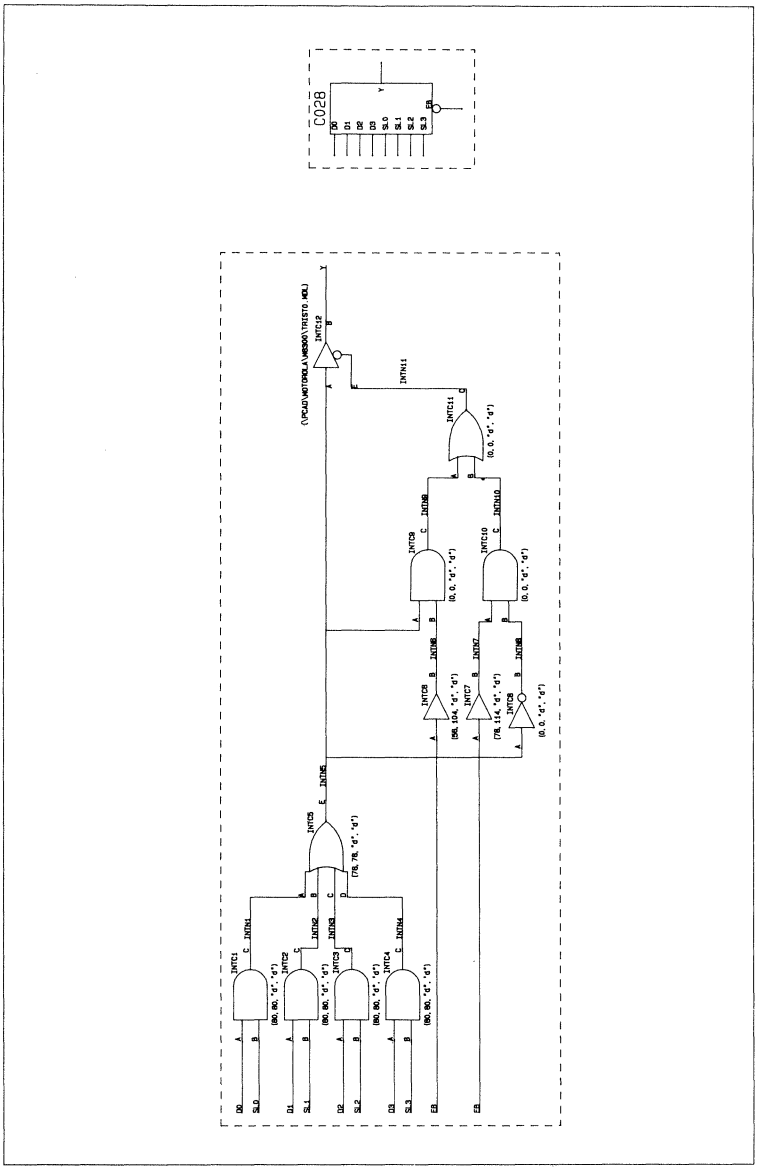
COMPONENT PLOTS

Plot 32



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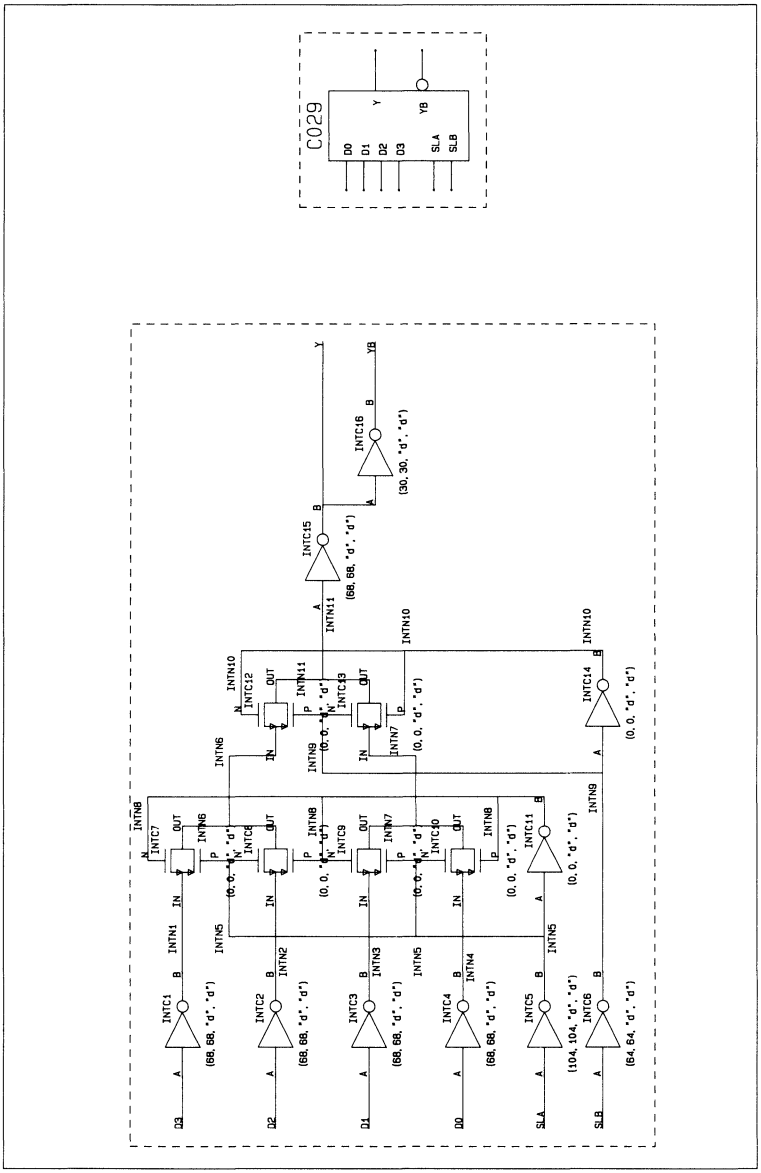
COMPONENT PLOTS

Plot 33



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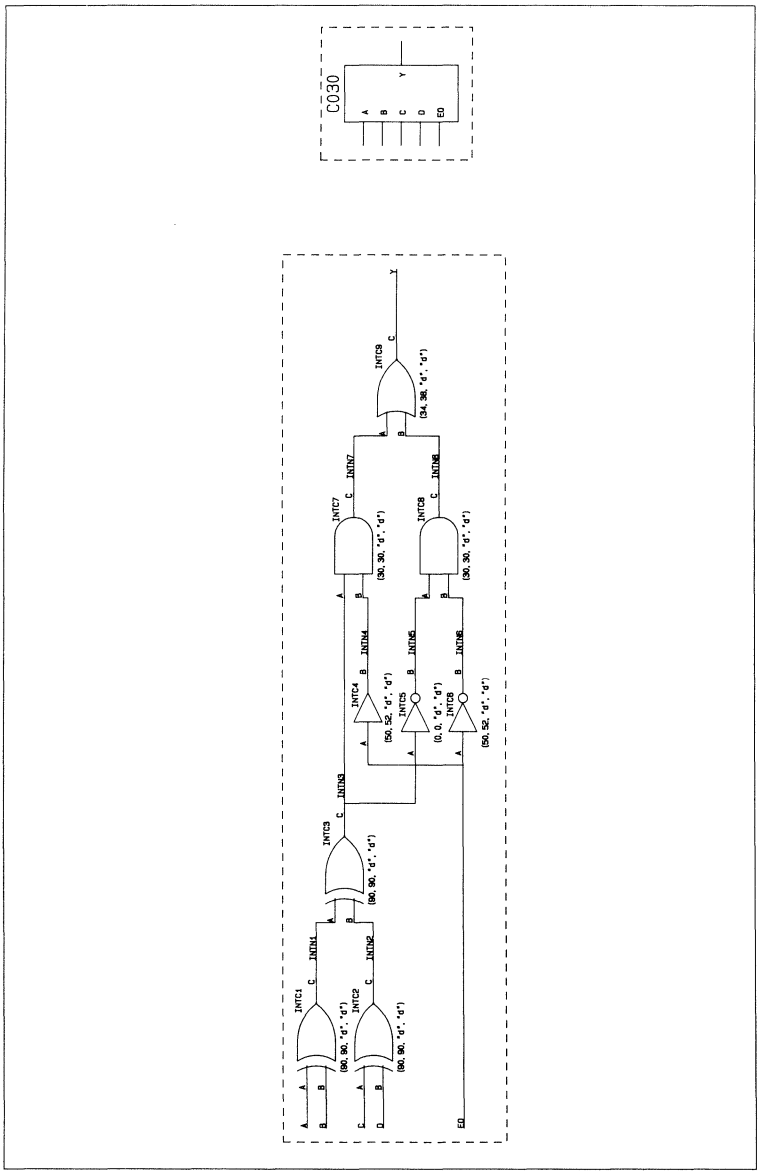
COMPONENT PLOTS

Plot 34



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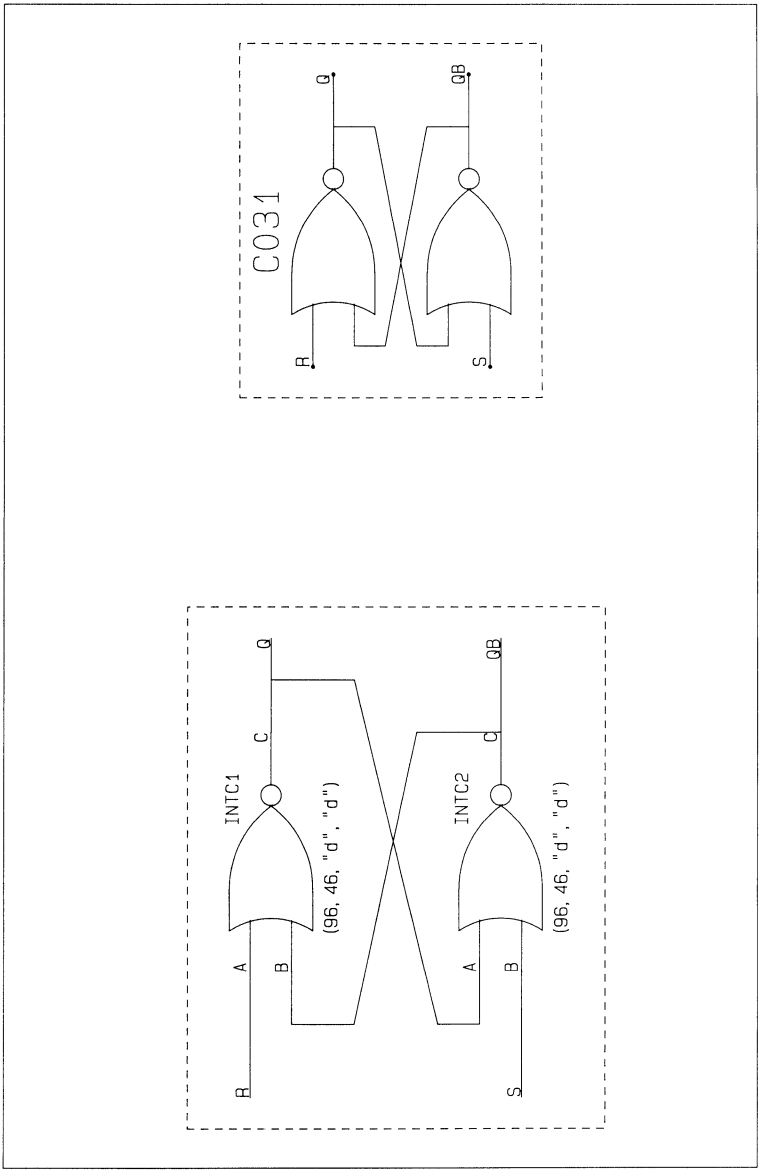
COMPONENT PLOTS

Plot 35



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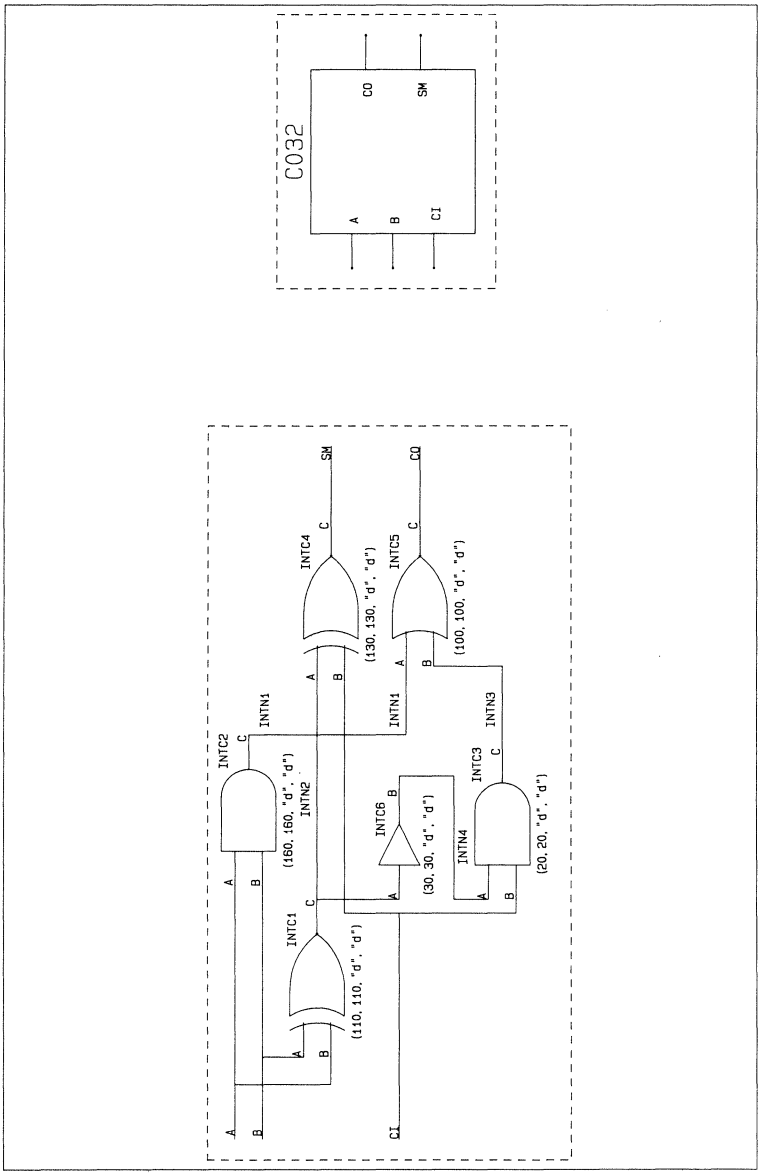
COMPONENT PLOTS

Plot 36



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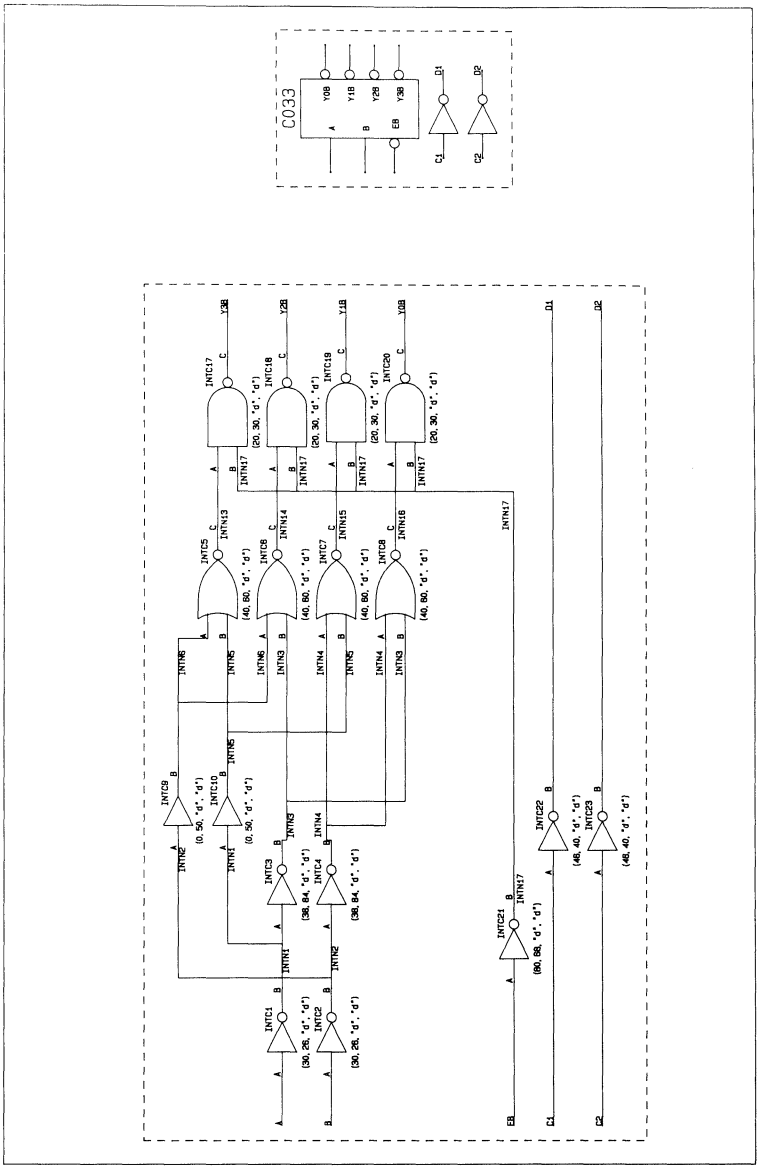
COMPONENT PLOTS

Plot 37



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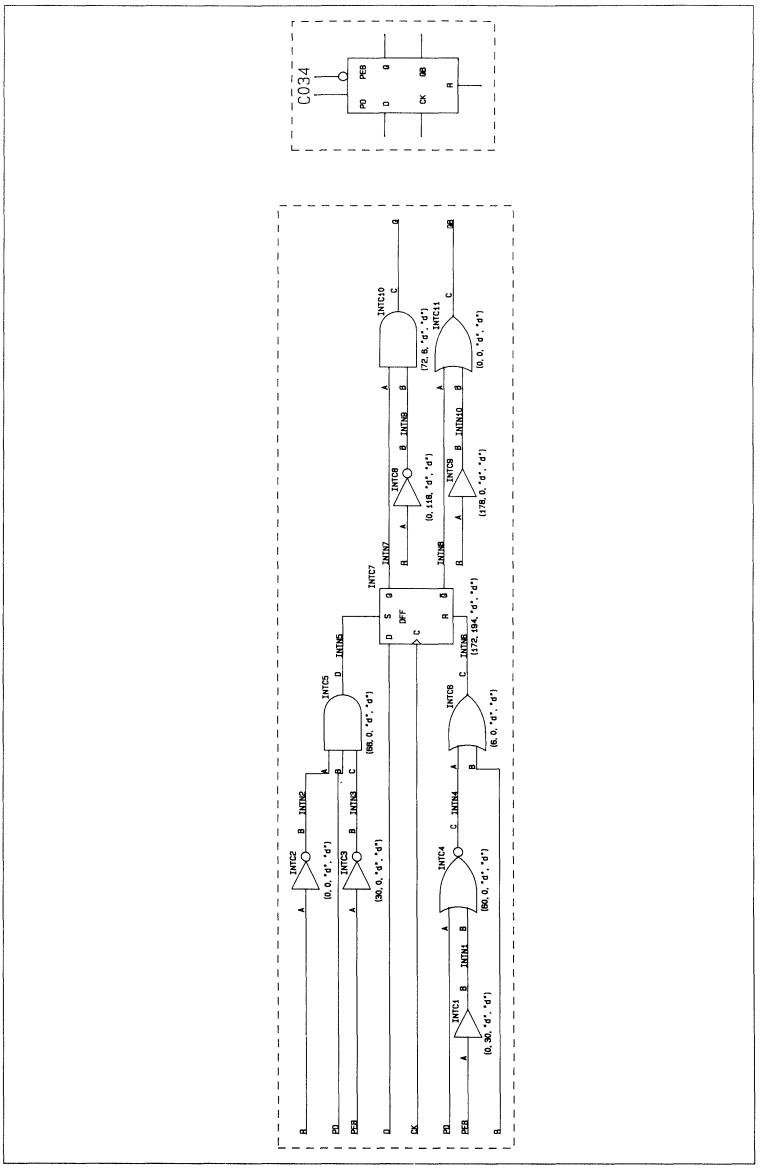
COMPONENT PLOTS

Plot 38



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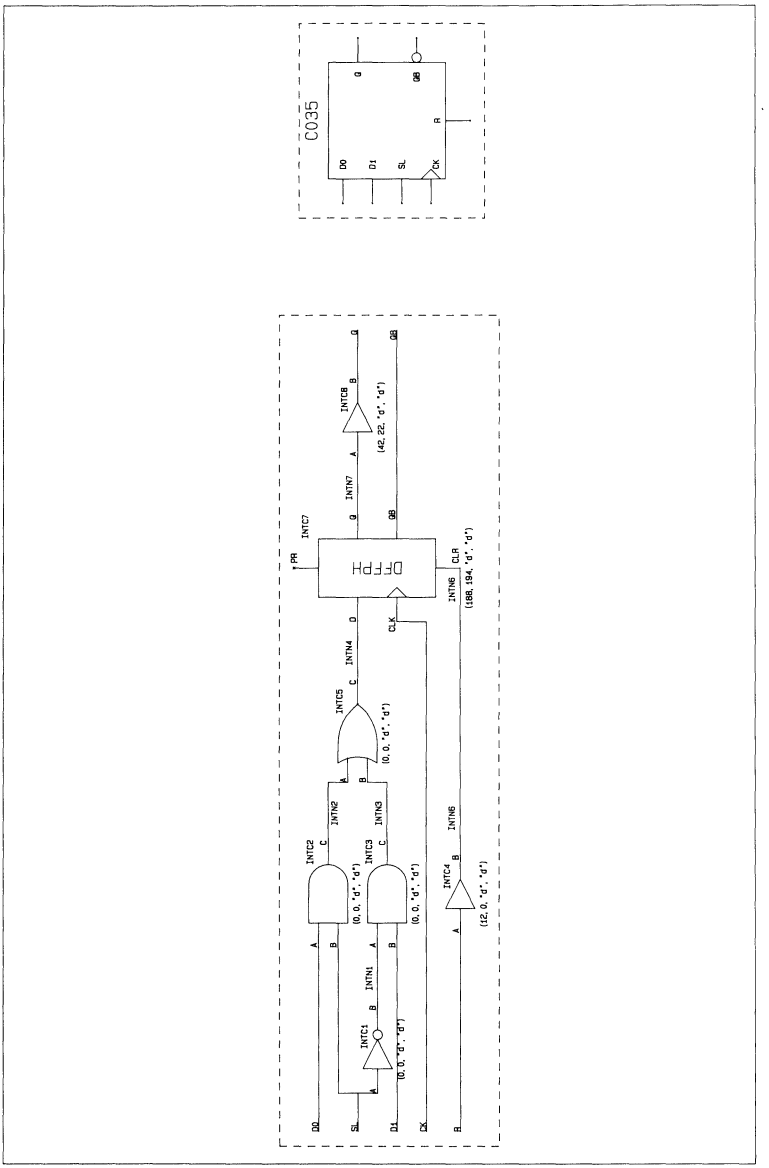
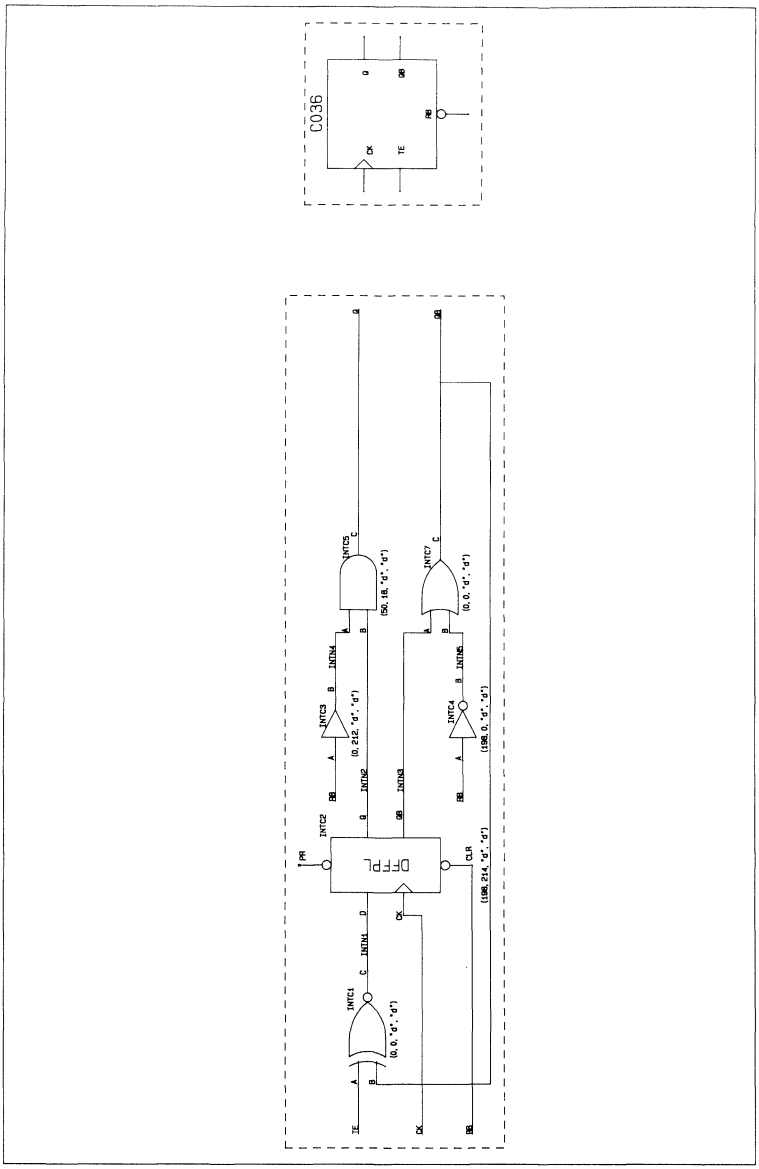
COMPONENT PLOTS

Plot 39



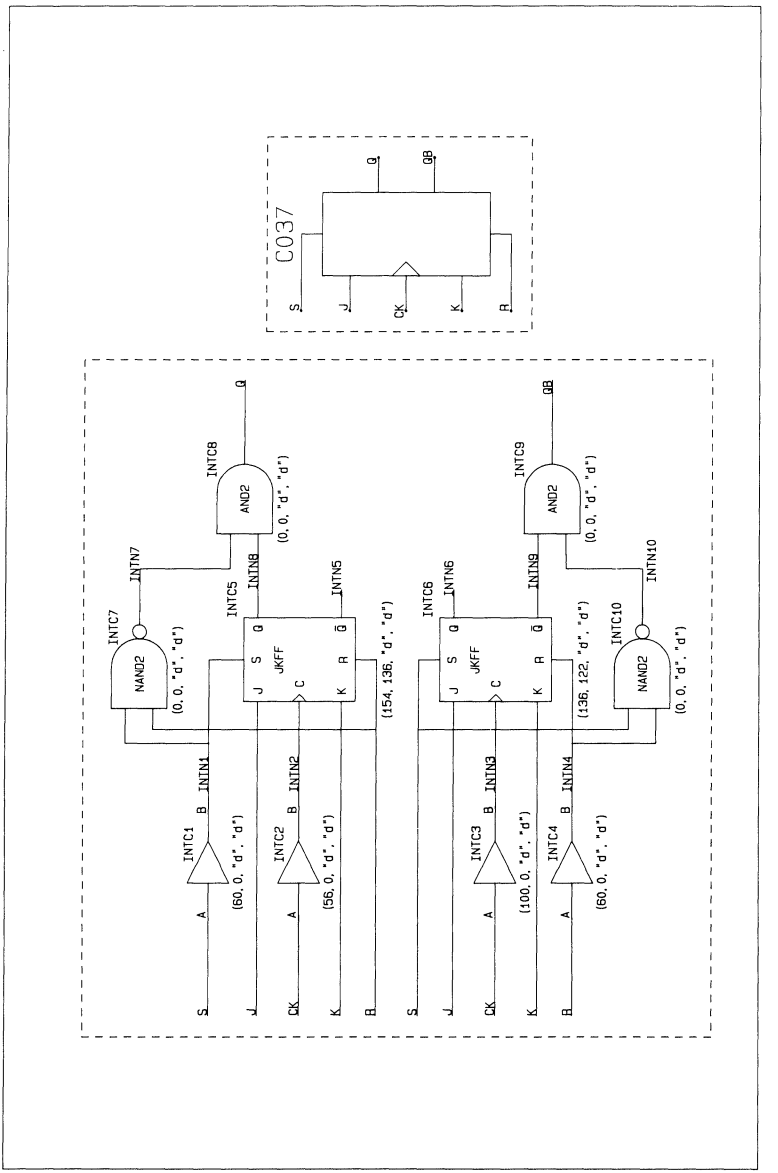
COMPONENT PLOTS

Plot 40



COMPONENT PLOTS

Plot 41



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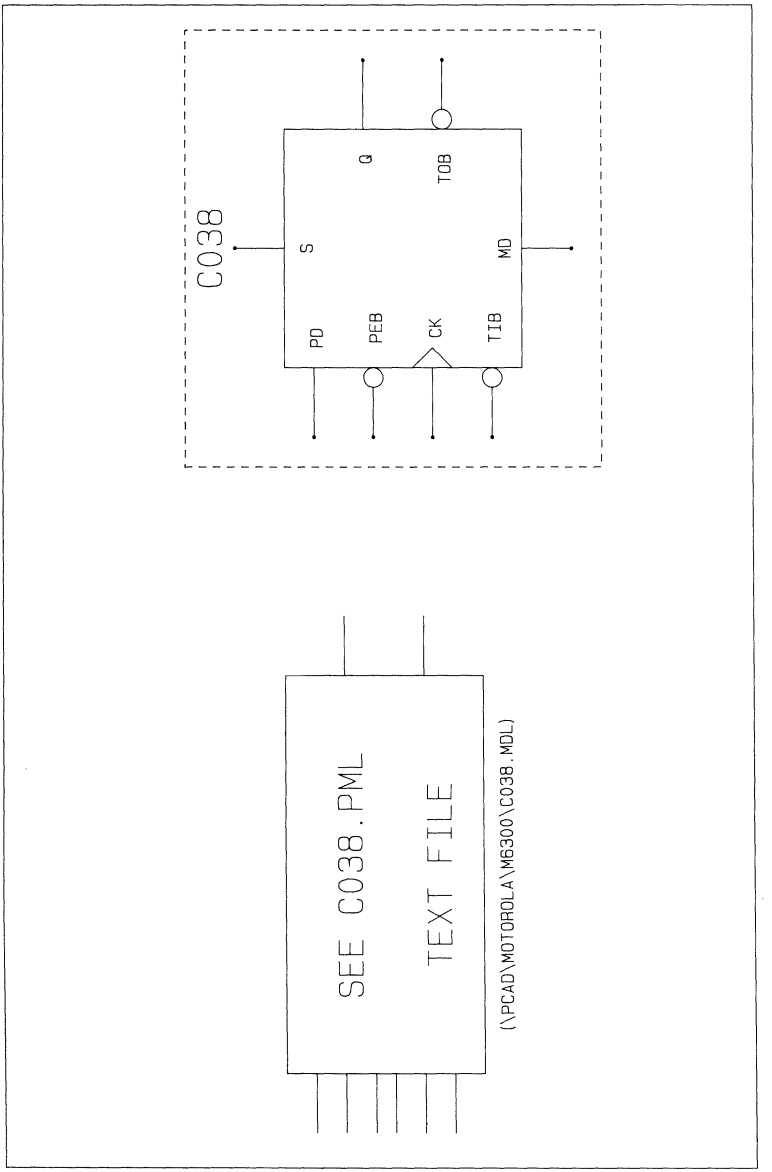
COMPONENT PLOTS

Plot 42



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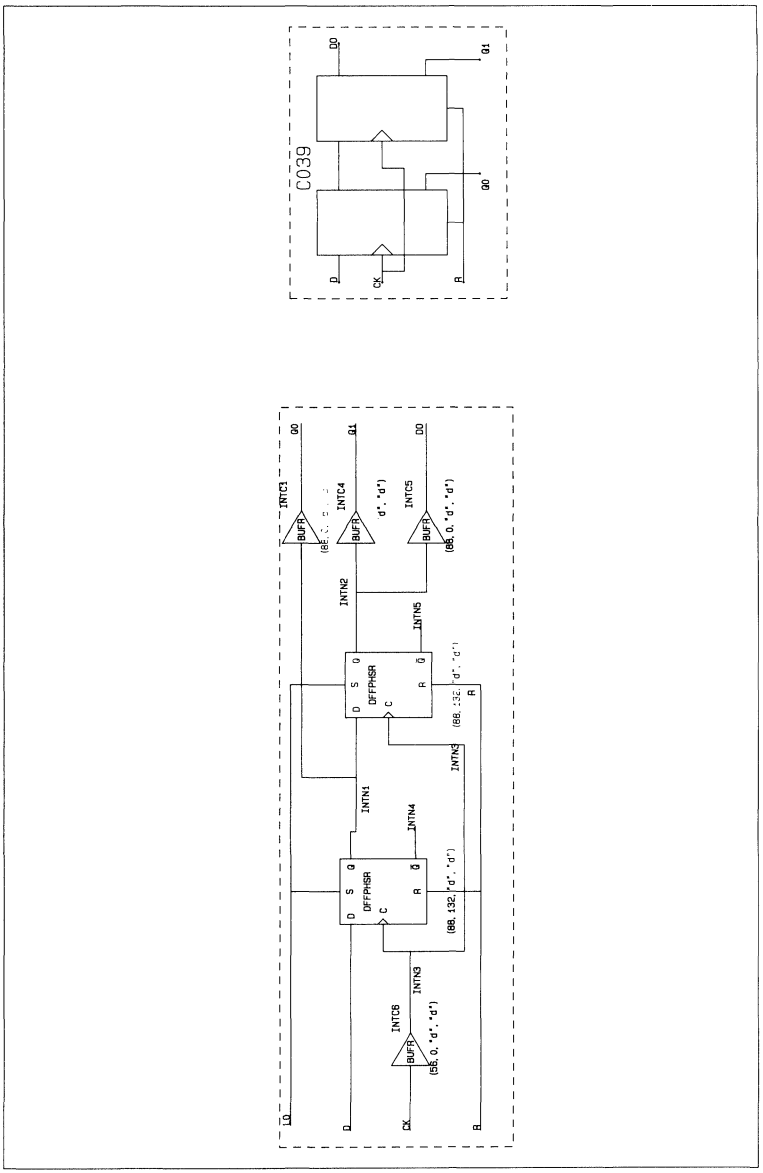
COMPONENT PLOTS

Plot 43



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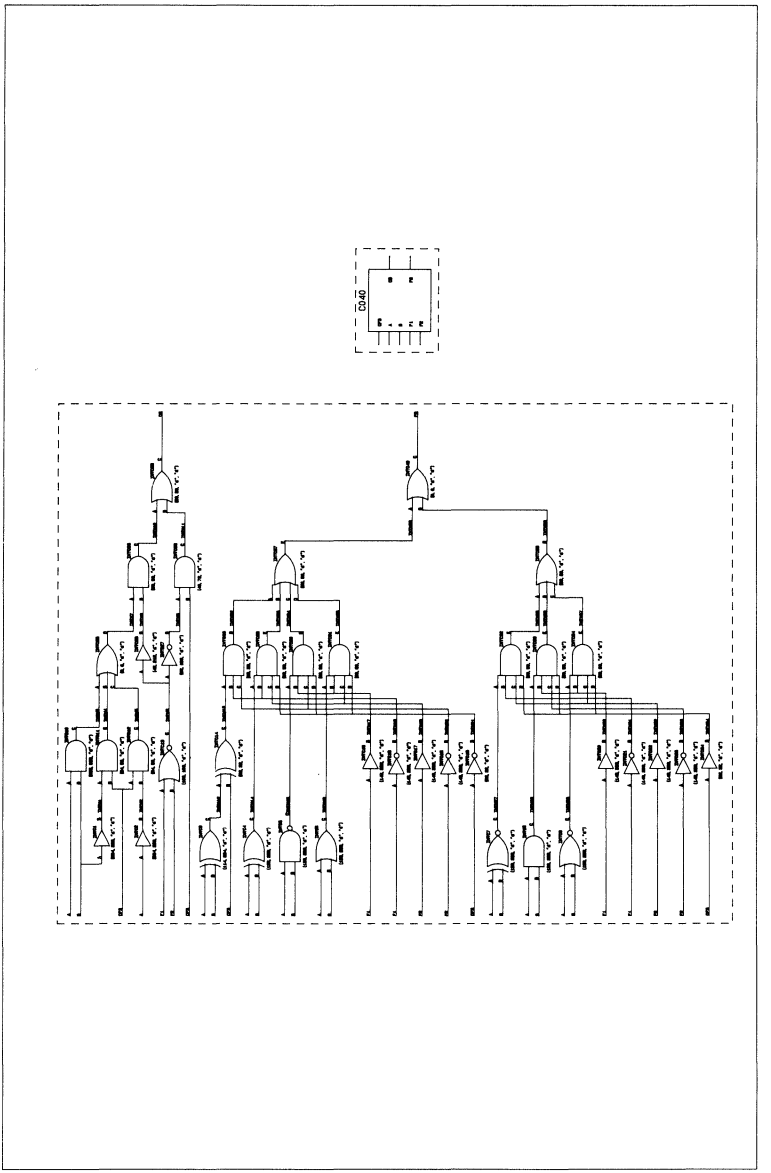
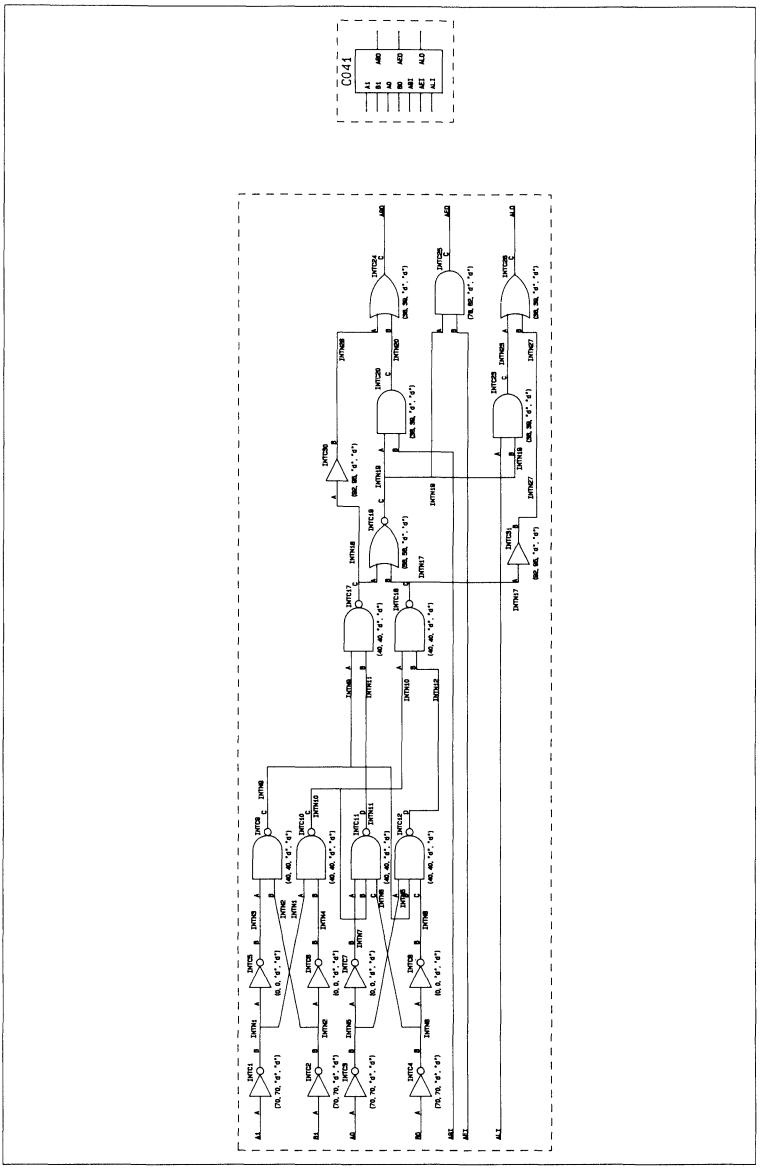
COMPONENT PLOTS

Plot 44



COMPONENT PLOTS

Plot 45



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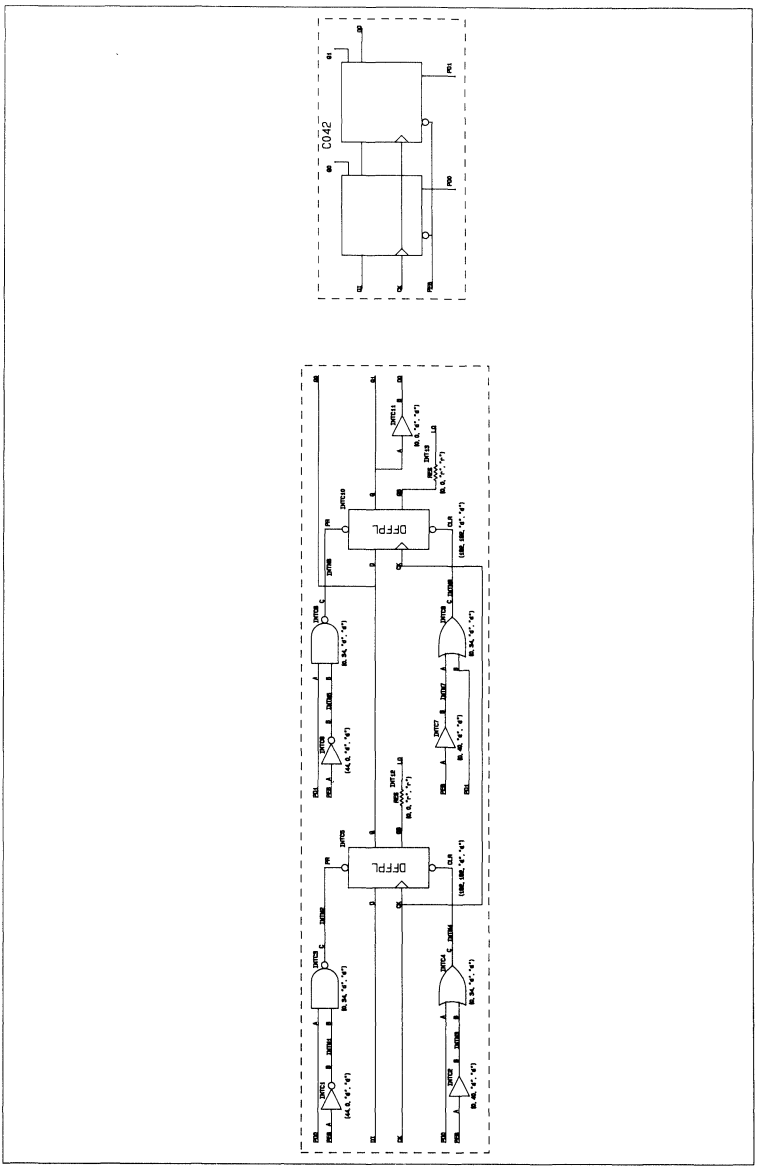
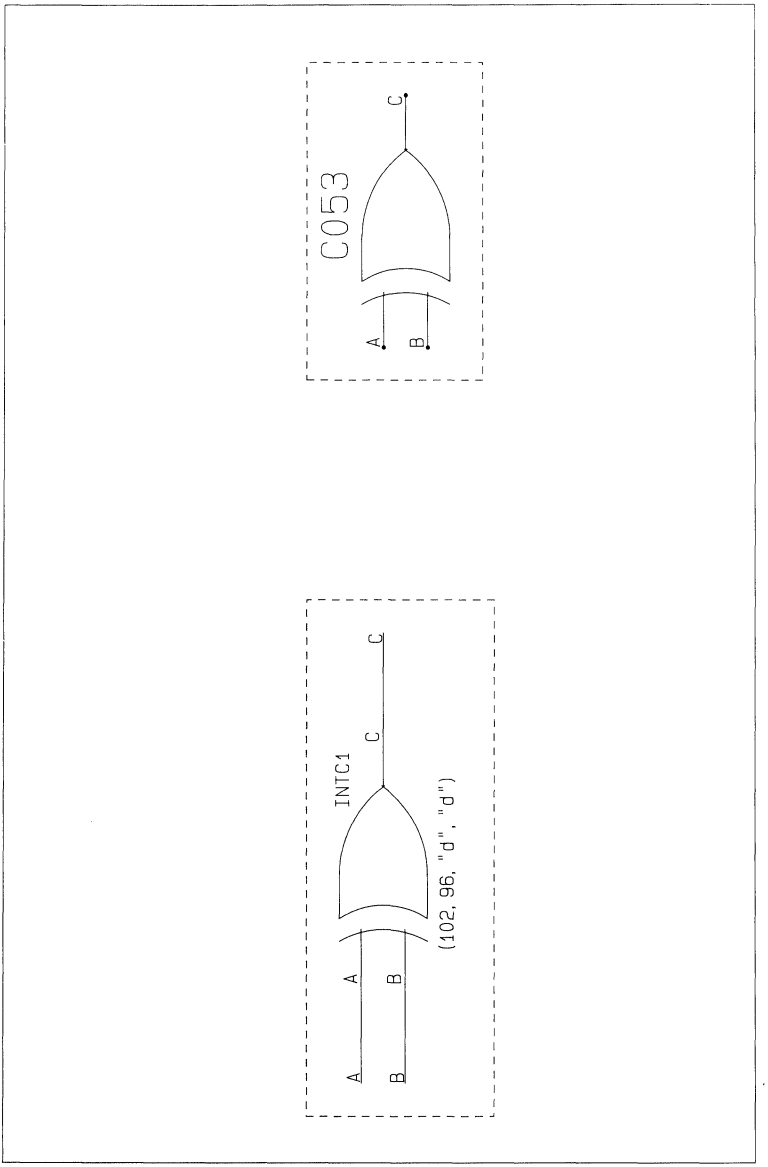
COMPONENT PLOTS

Plot 46



COMPONENT PLOTS

Plot 47



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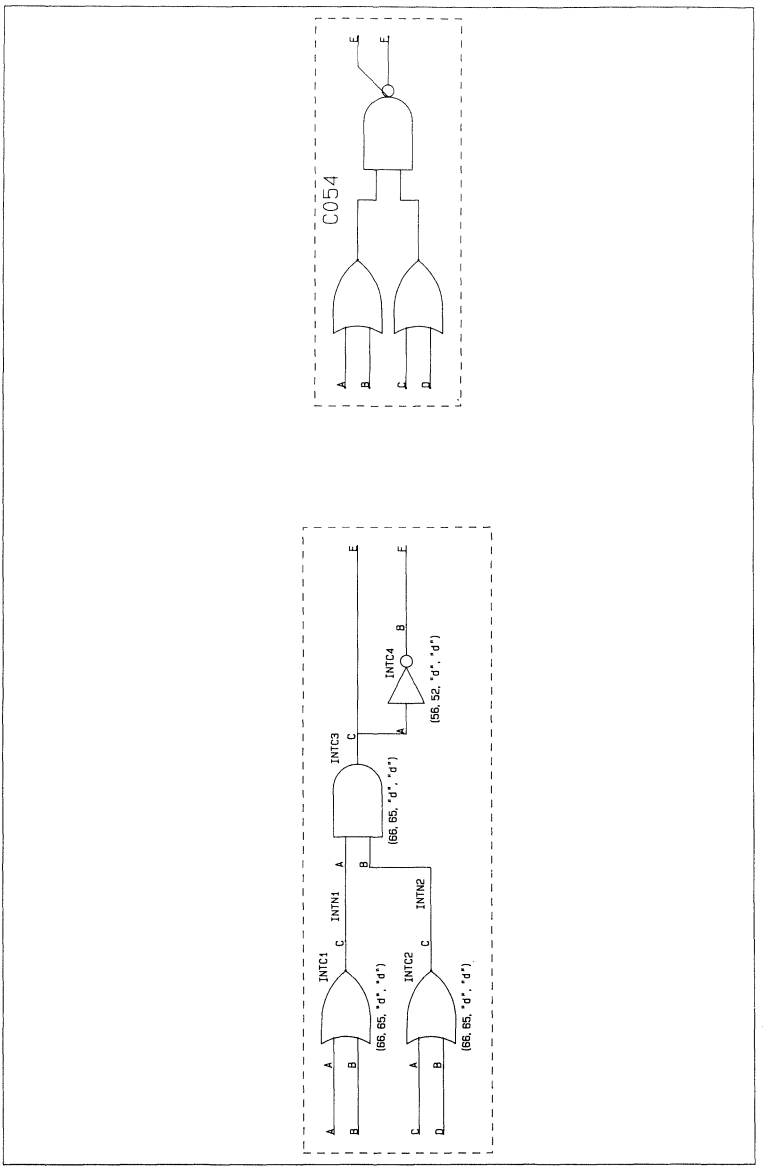
COMPONENT PLOTS

Plot 48



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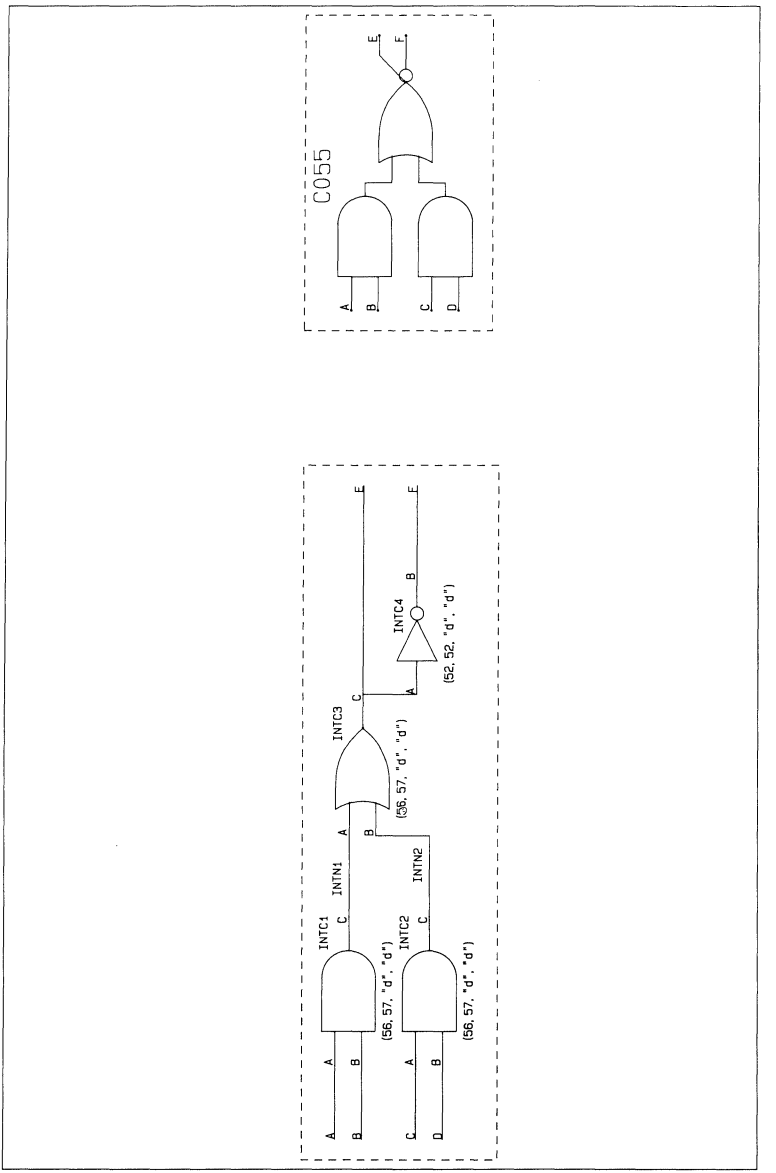
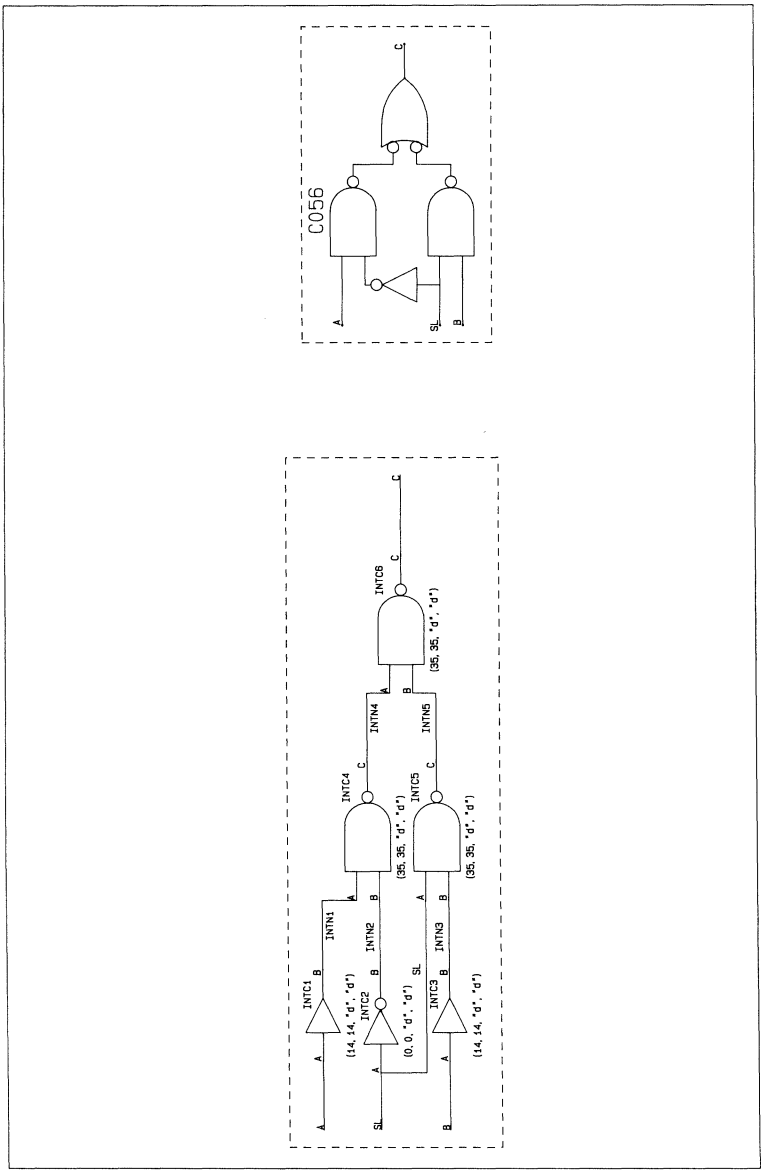
COMPONENT PLOTS

Plot 49



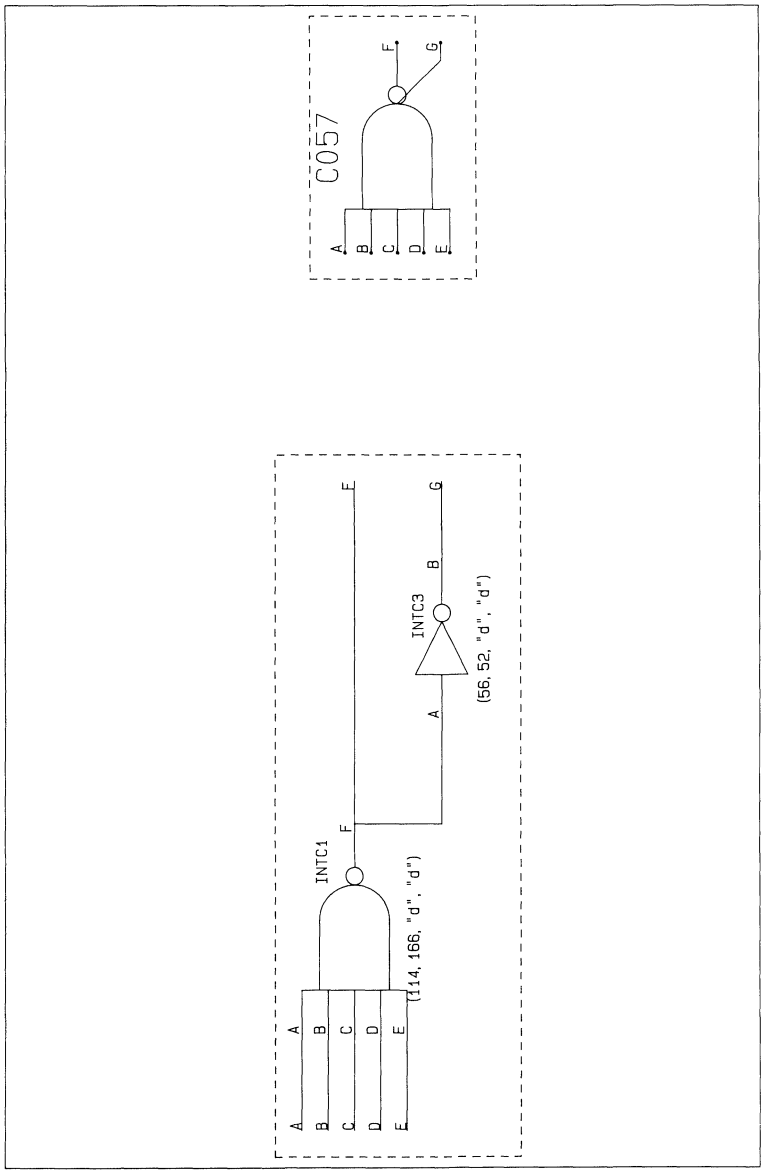
COMPONENT PLOTS

Plot 50



COMPONENT PLOTS

Plot 51



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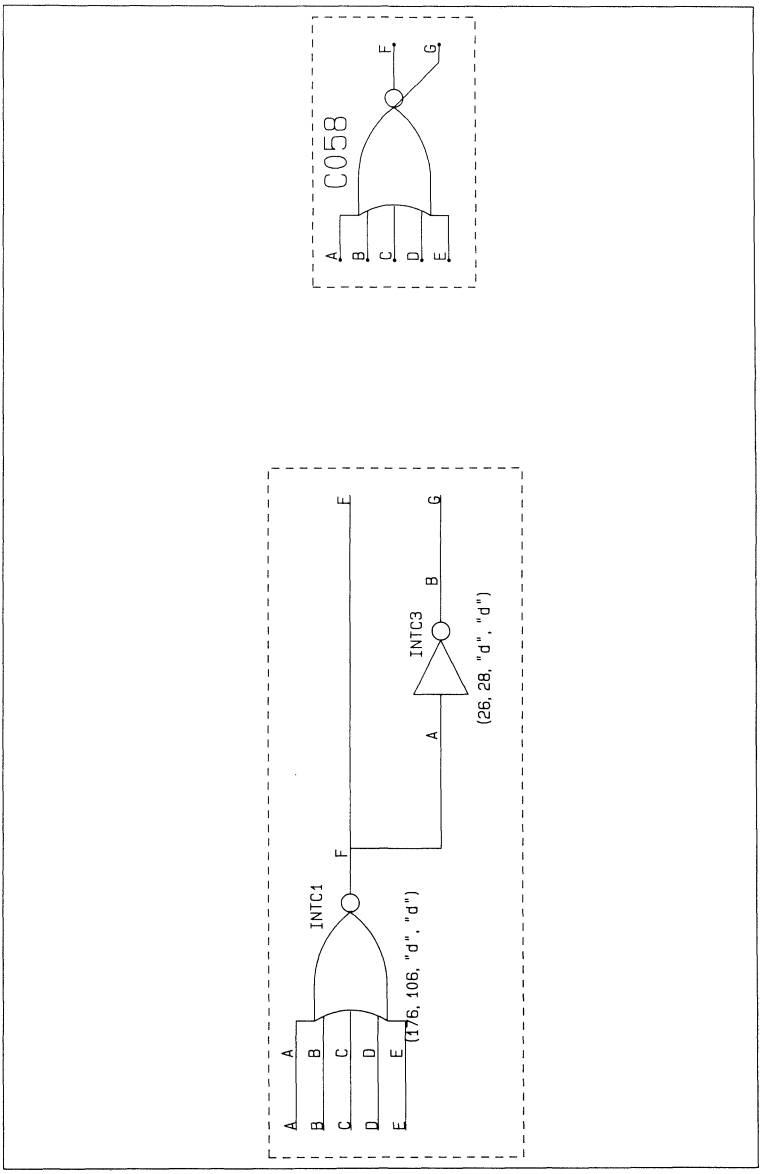
COMPONENT PLOTS

Plot 52



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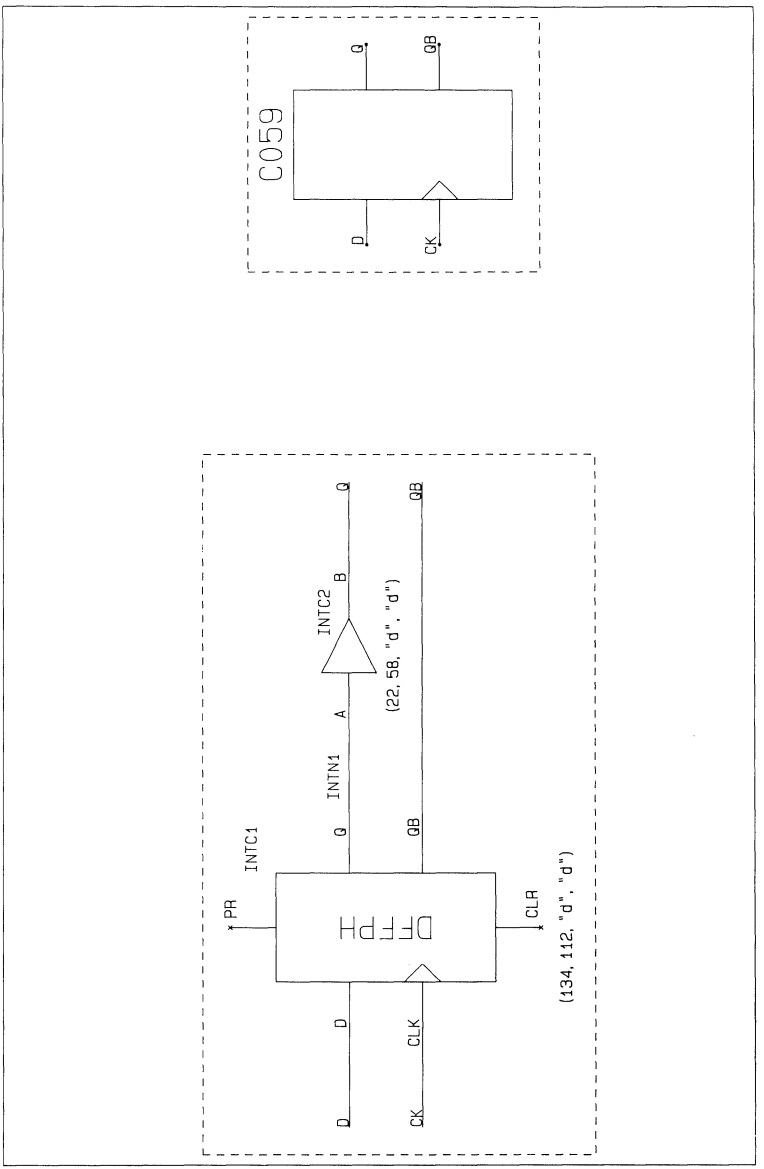
COMPONENT PLOTS

Plot 53



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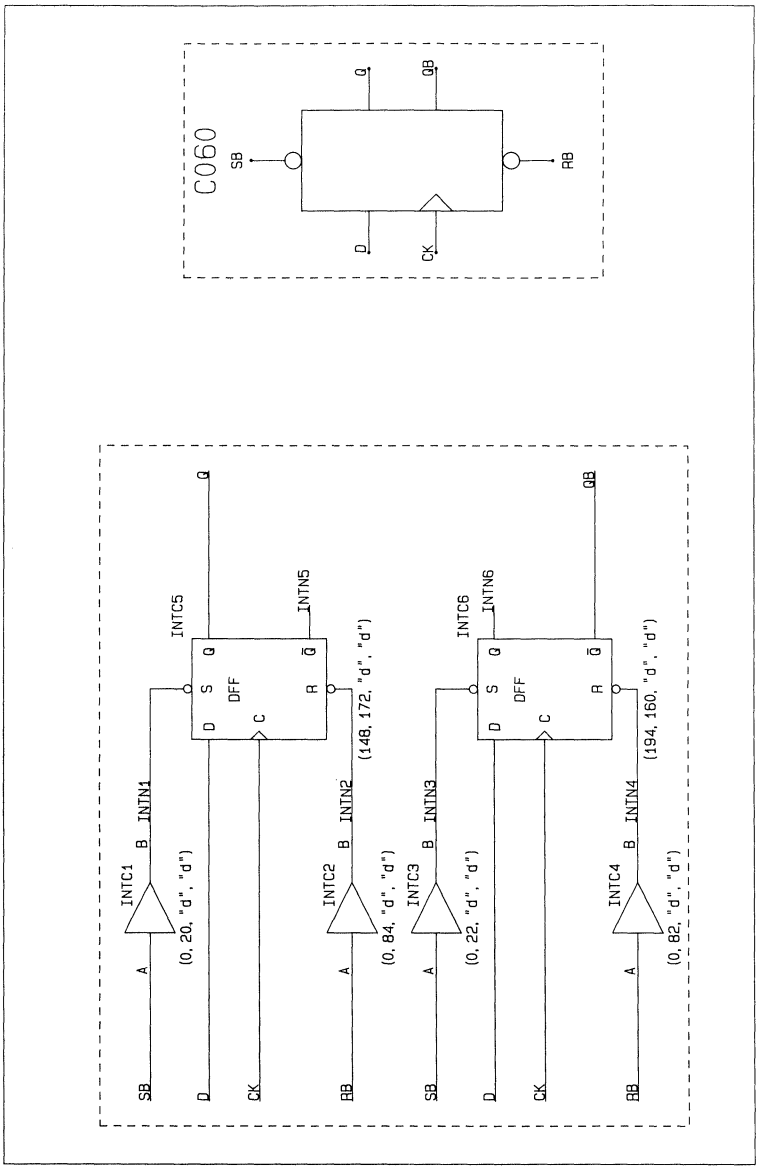
COMPONENT PLOTS

Plot 54



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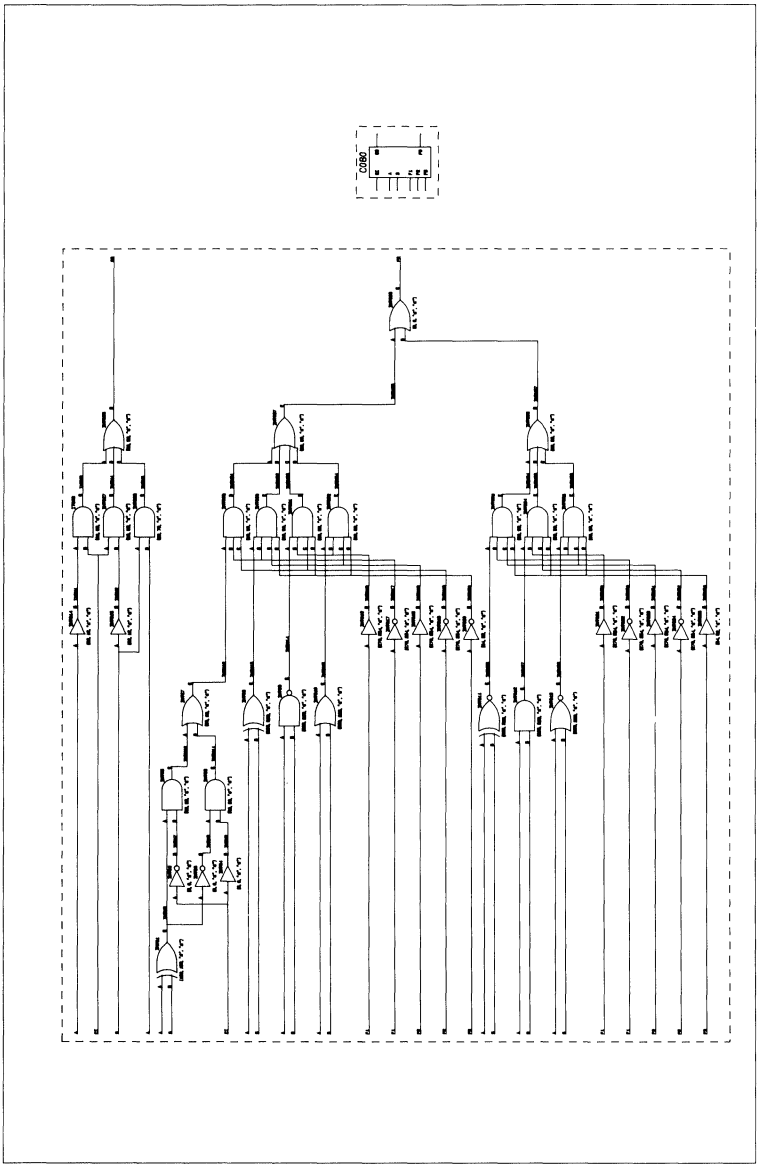
COMPONENT PLOTS

Plot 55



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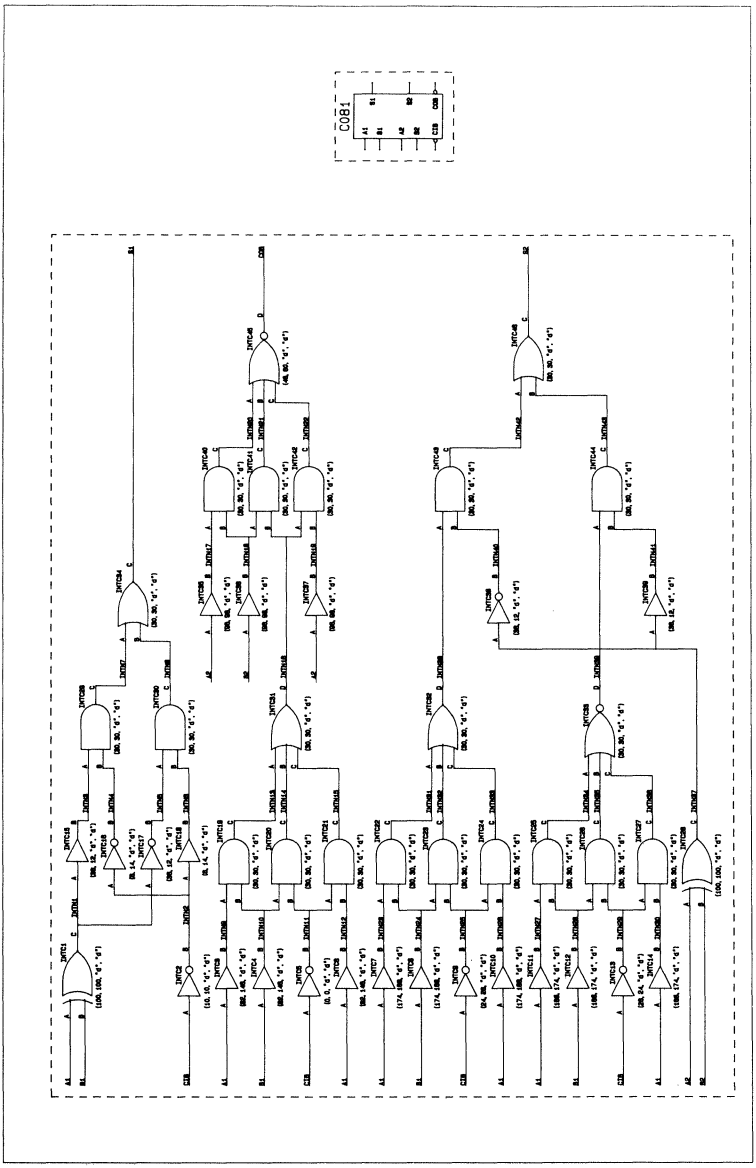
COMPONENT PLOTS

Plot 56



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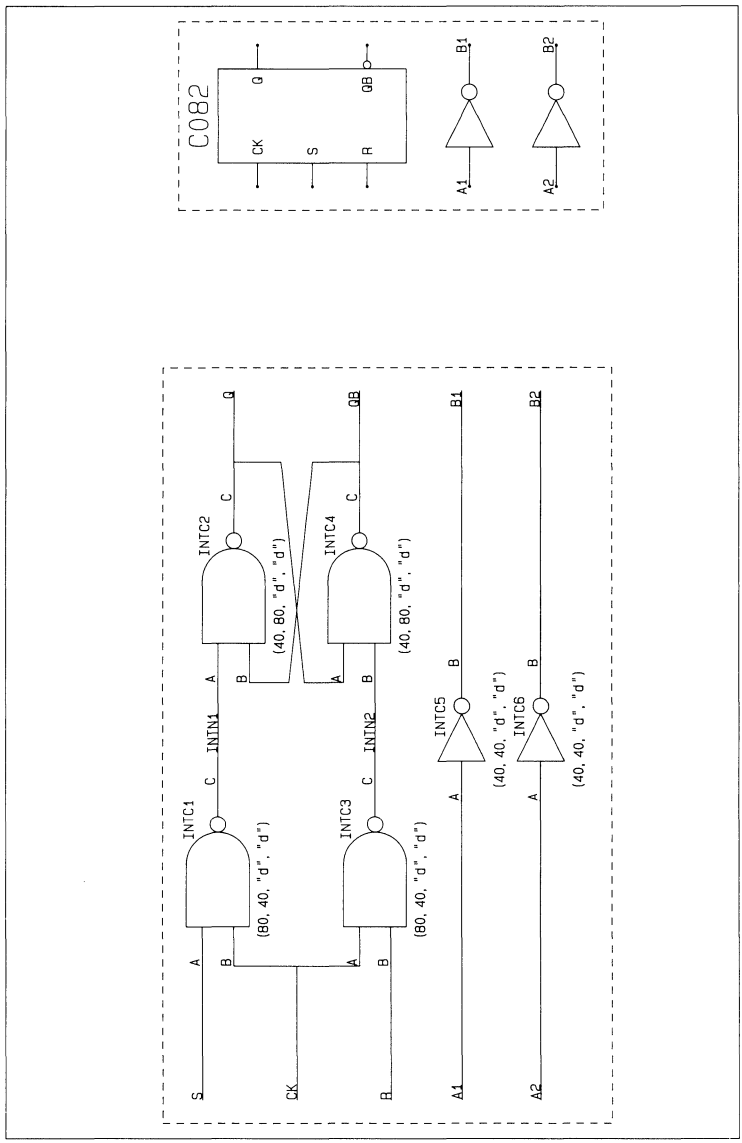
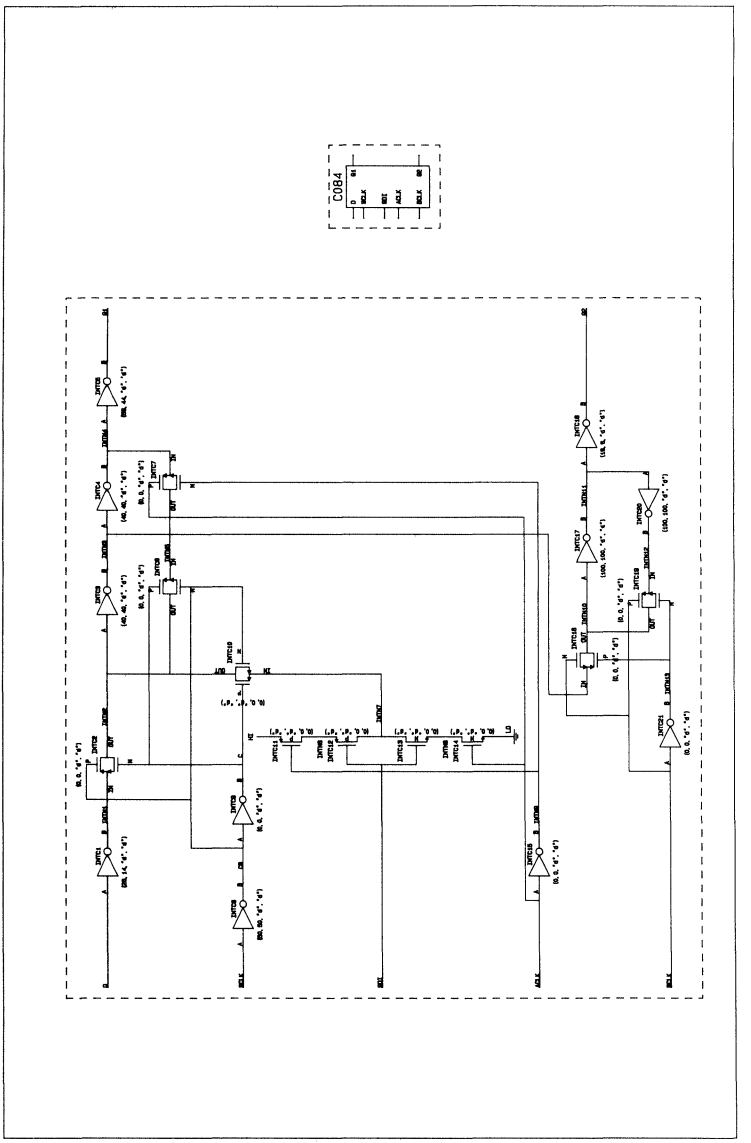
COMPONENT PLOTS

Plot 57



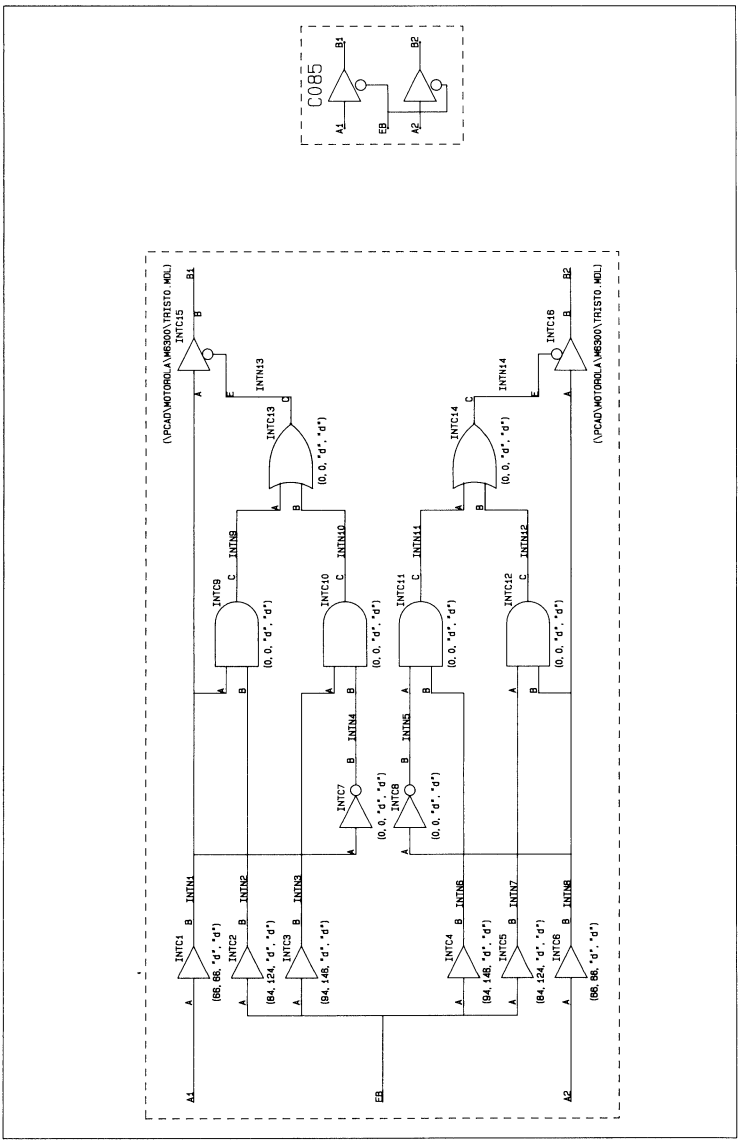
COMPONENT PLOTS

Plot 58



COMPONENT PLOTS

Plot 59



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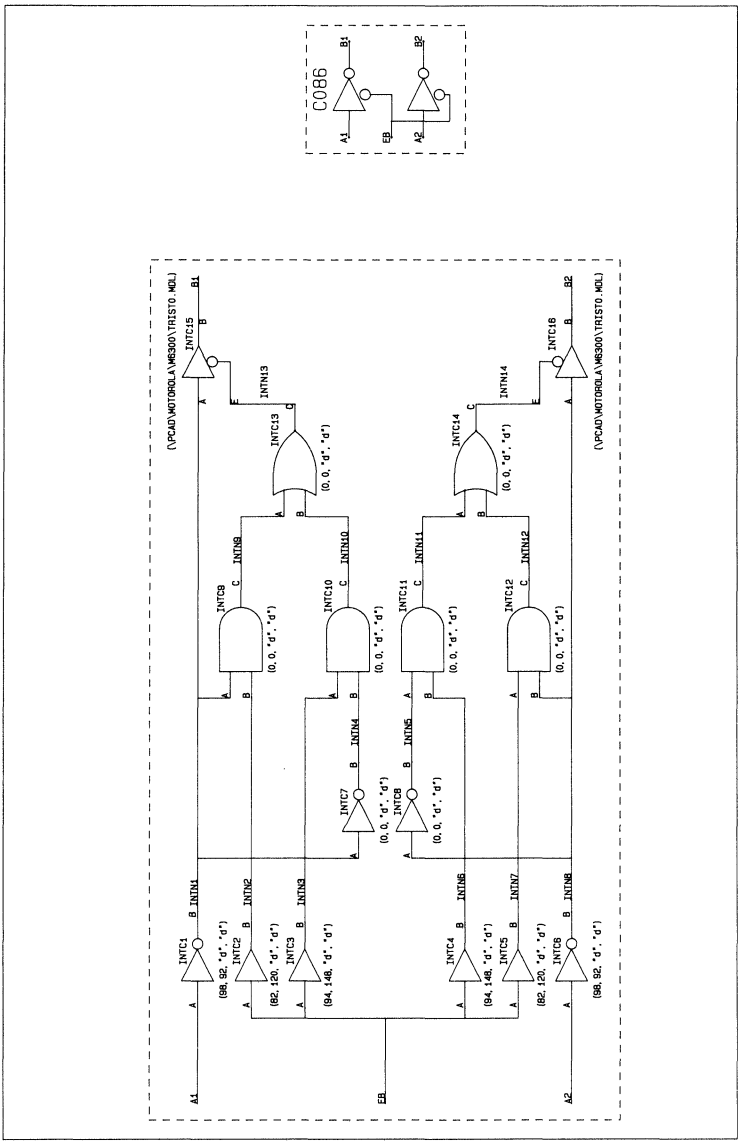
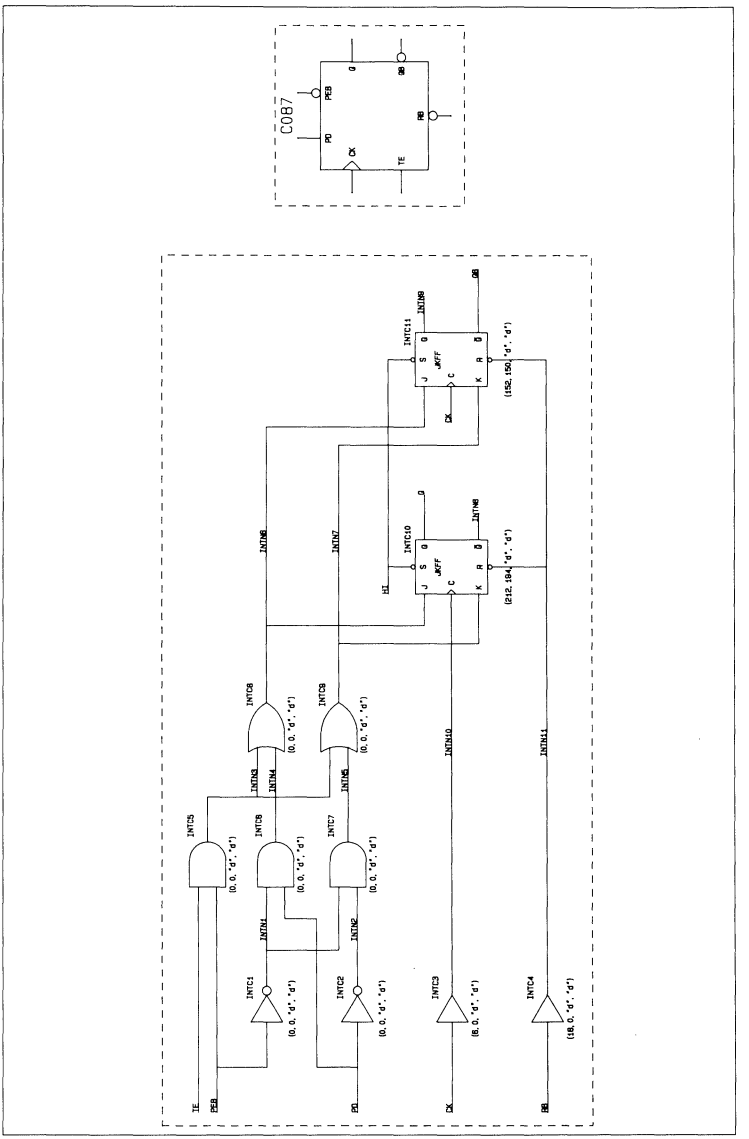
COMPONENT PLOTS

Plot 60



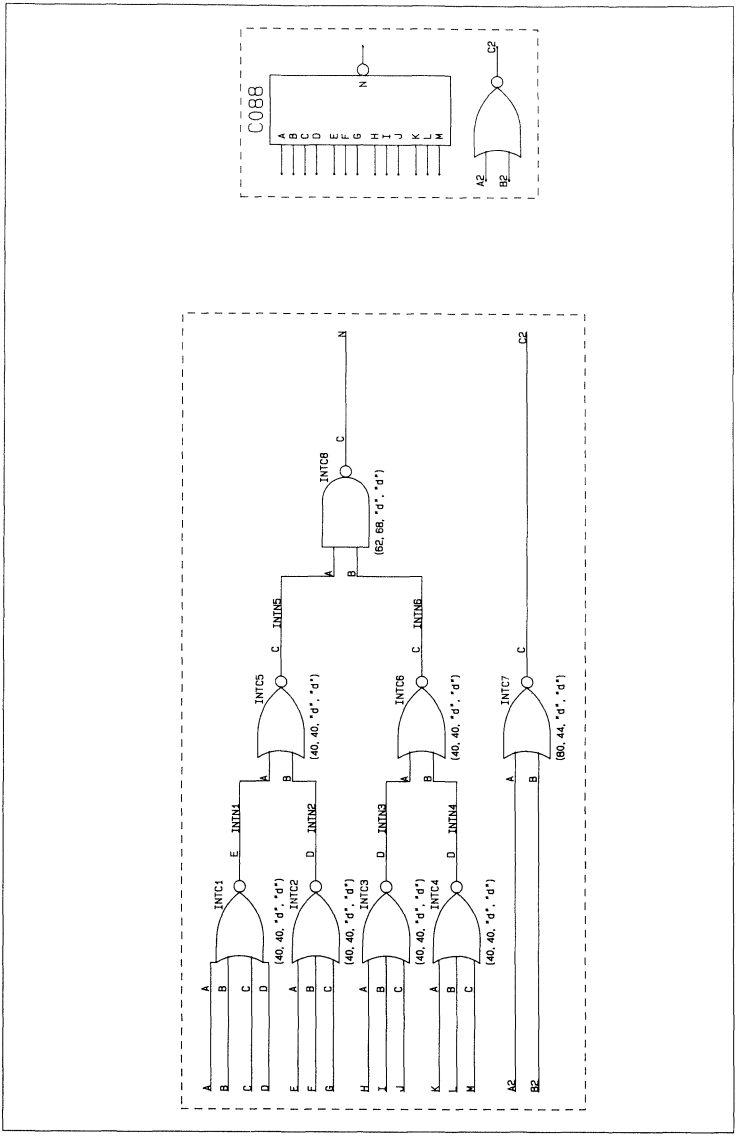
COMPONENT PLOTS

Plot 61



COMPONENT PLOTS

Plot 62



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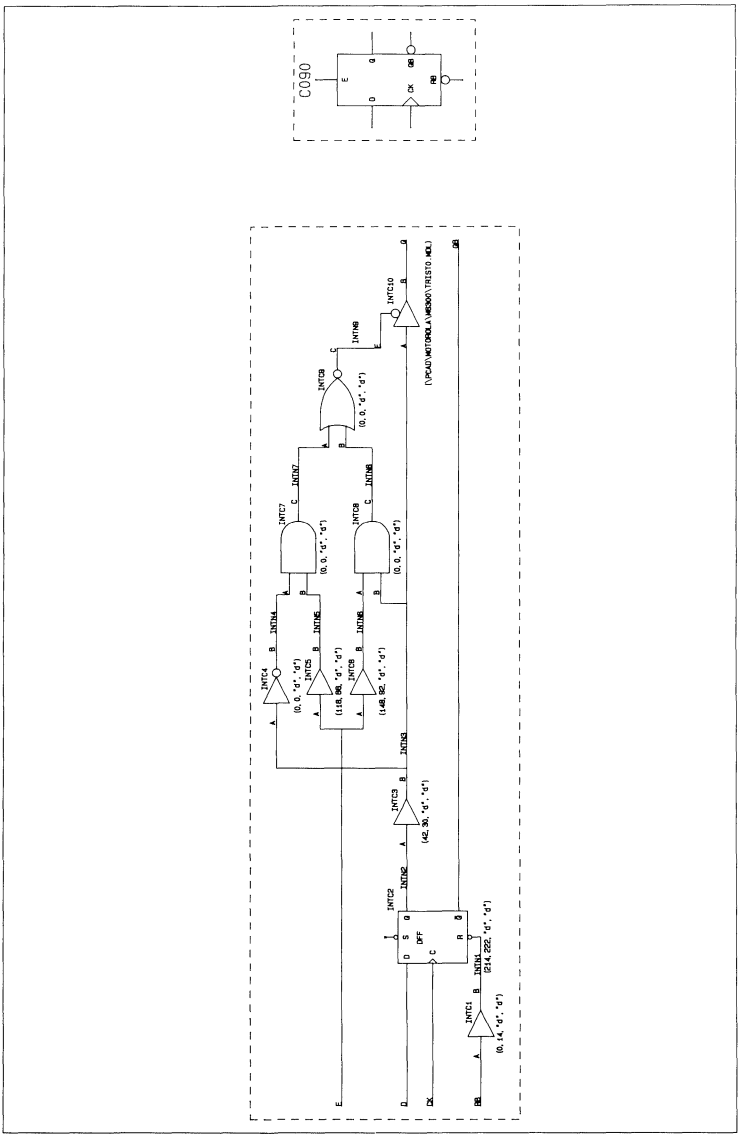
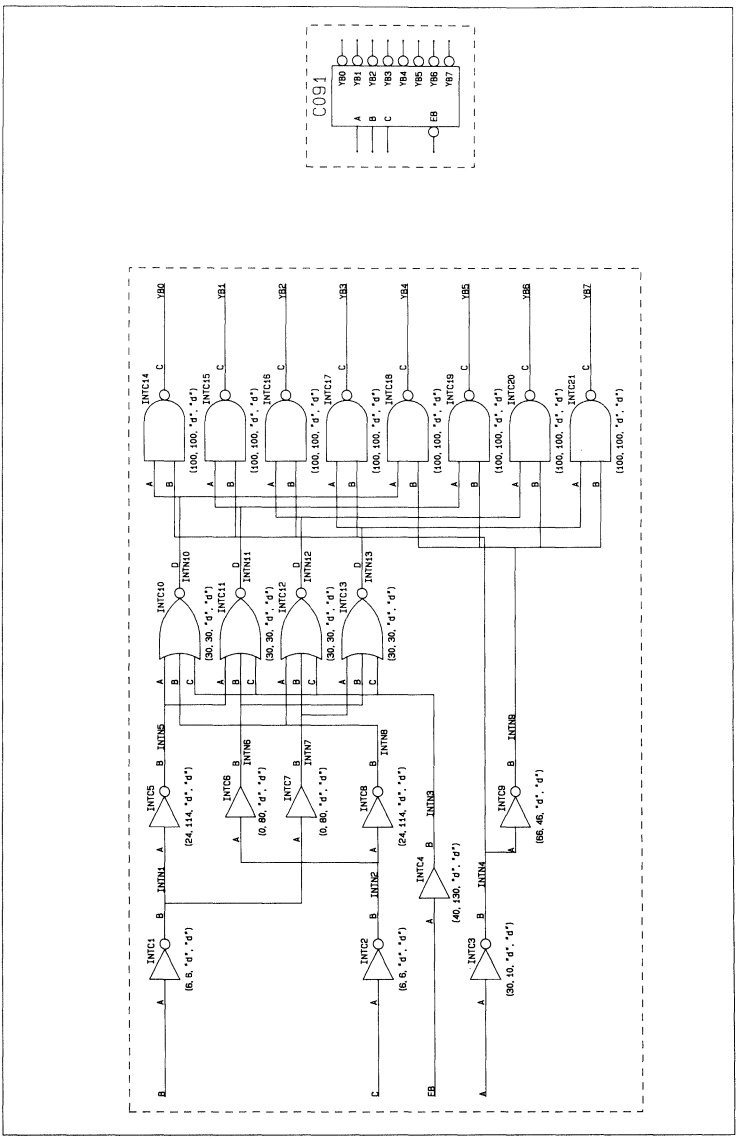
COMPONENT PLOTS

Plot 63



COMPONENT PLOTS

Plot 64



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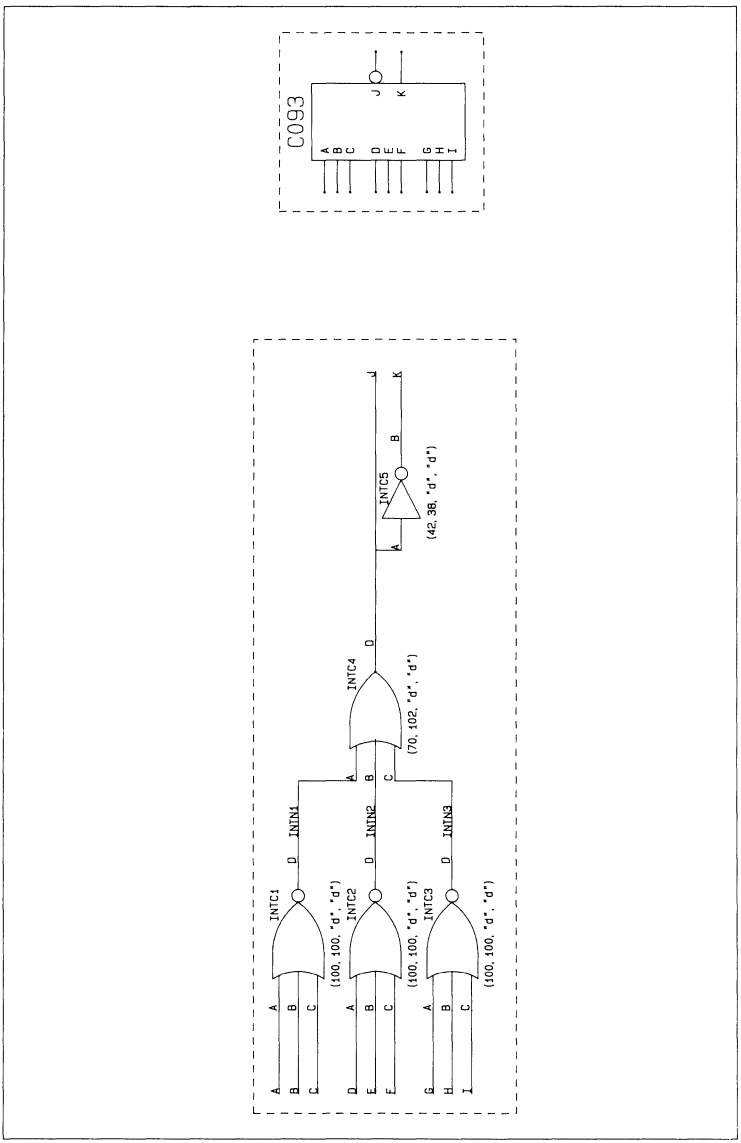
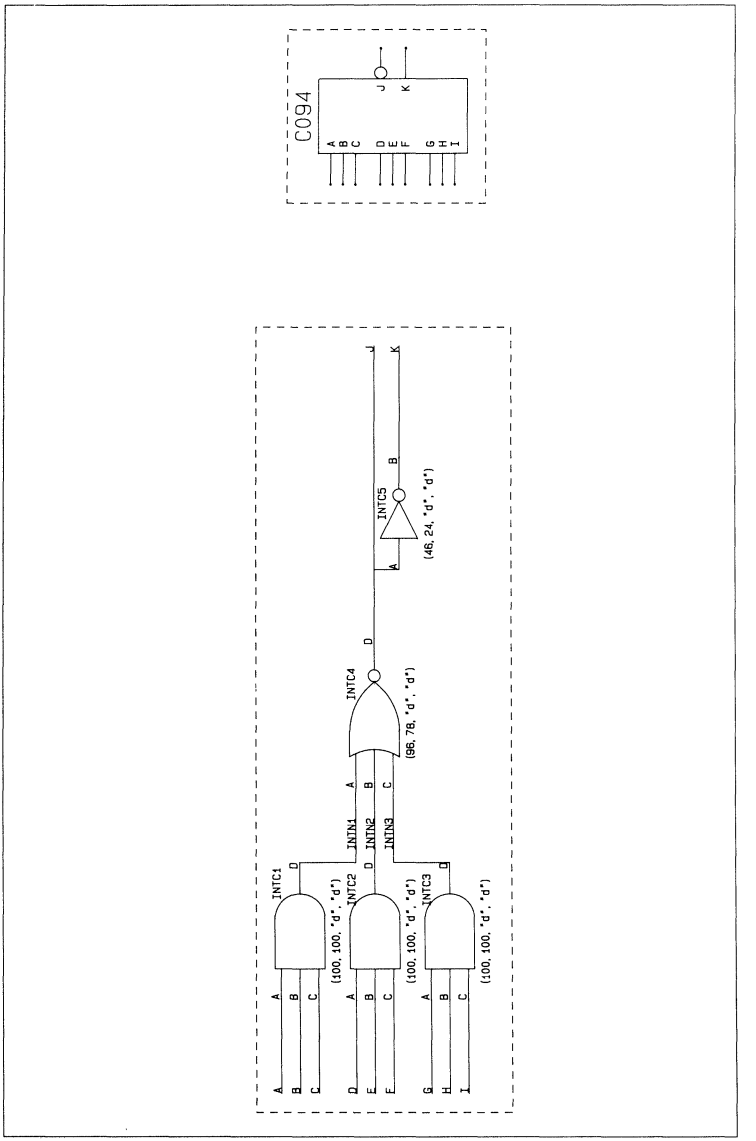
COMPONENT PLOTS

Plot 65



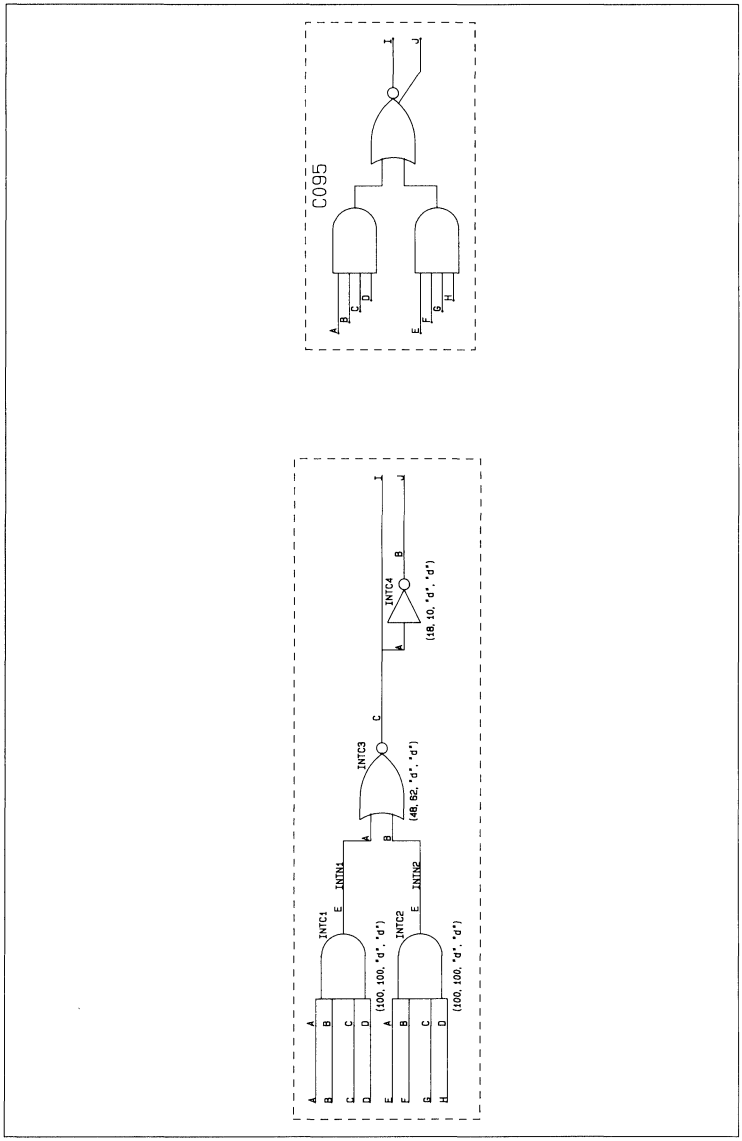
COMPONENT PLOTS

Plot 66



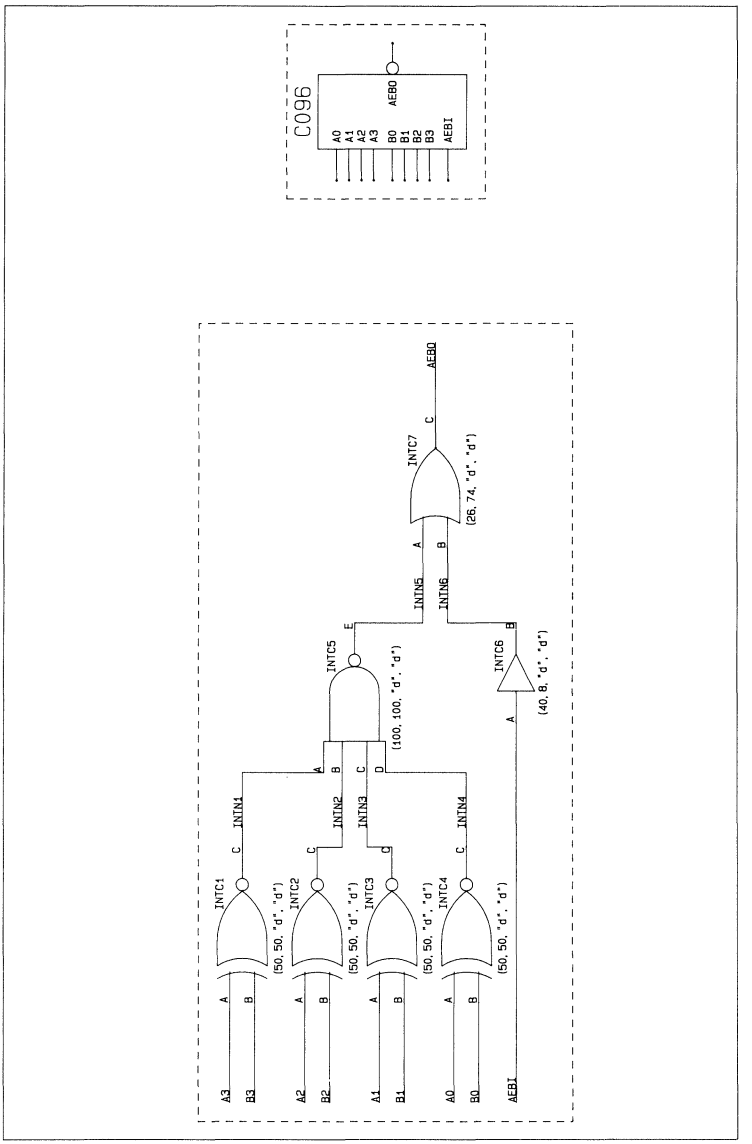
COMPONENT PLOTS

Plot 67



COMPONENT PLOTS

Plot 68



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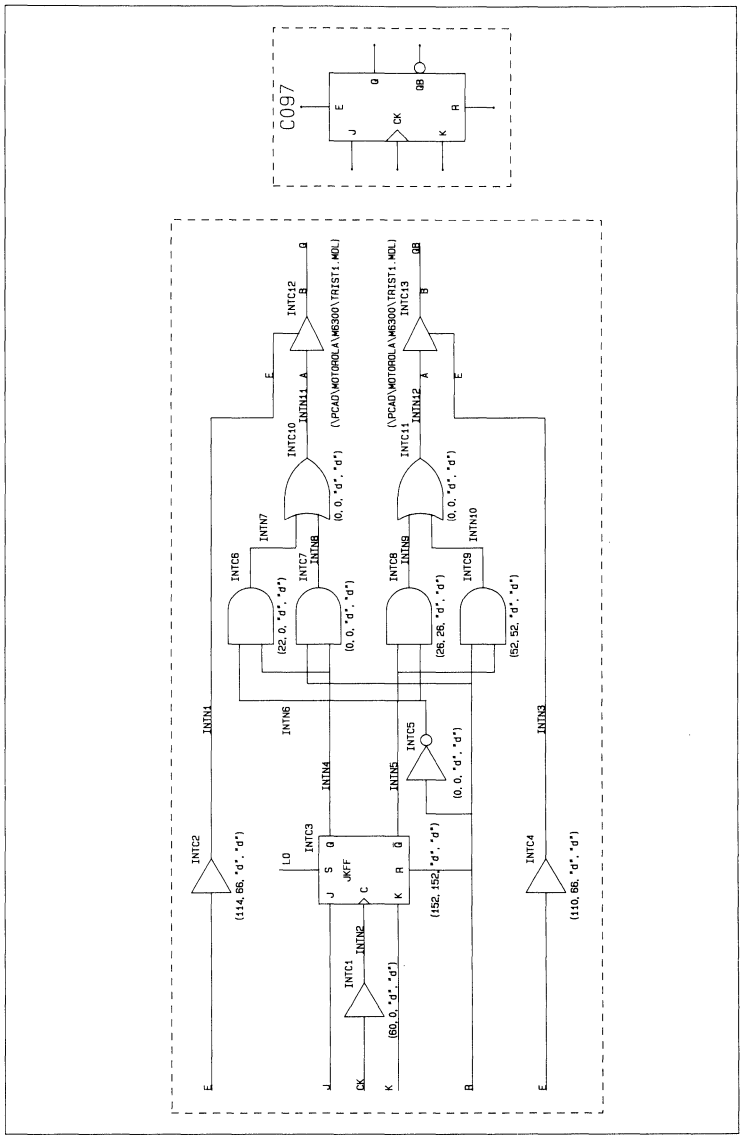
COMPONENT PLOTS

Plot 69



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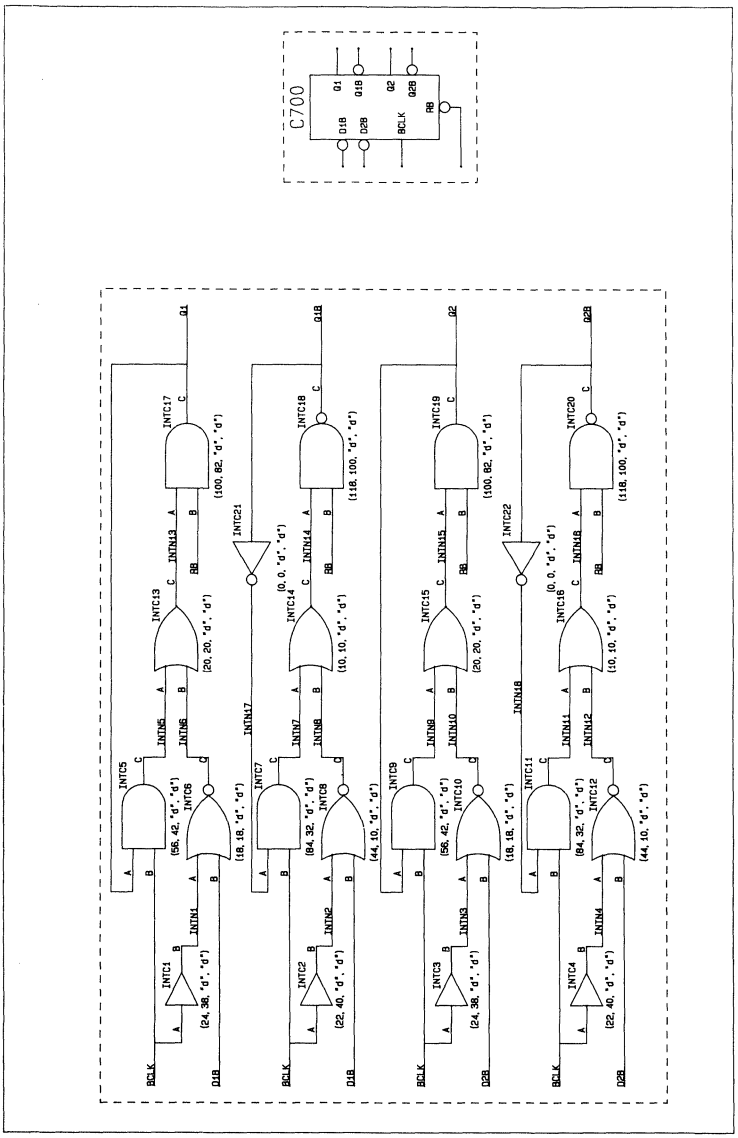
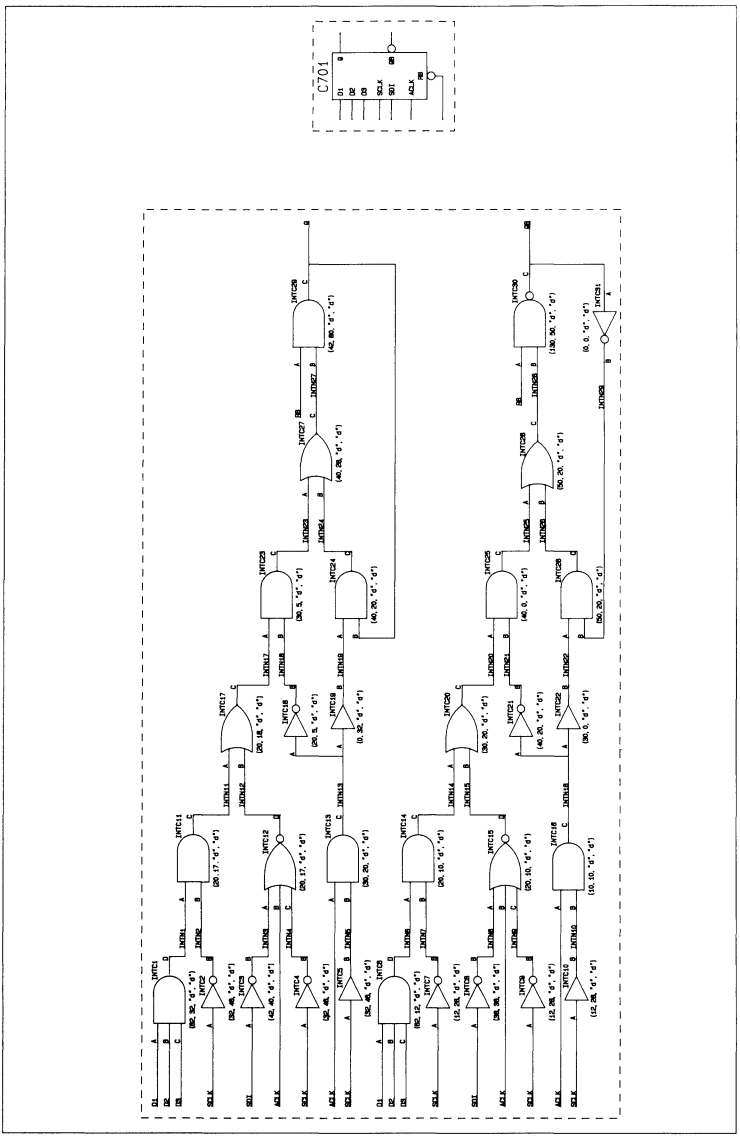
COMPONENT PLOTS

Plot 70



COMPONENT PLOTS

Plot 71



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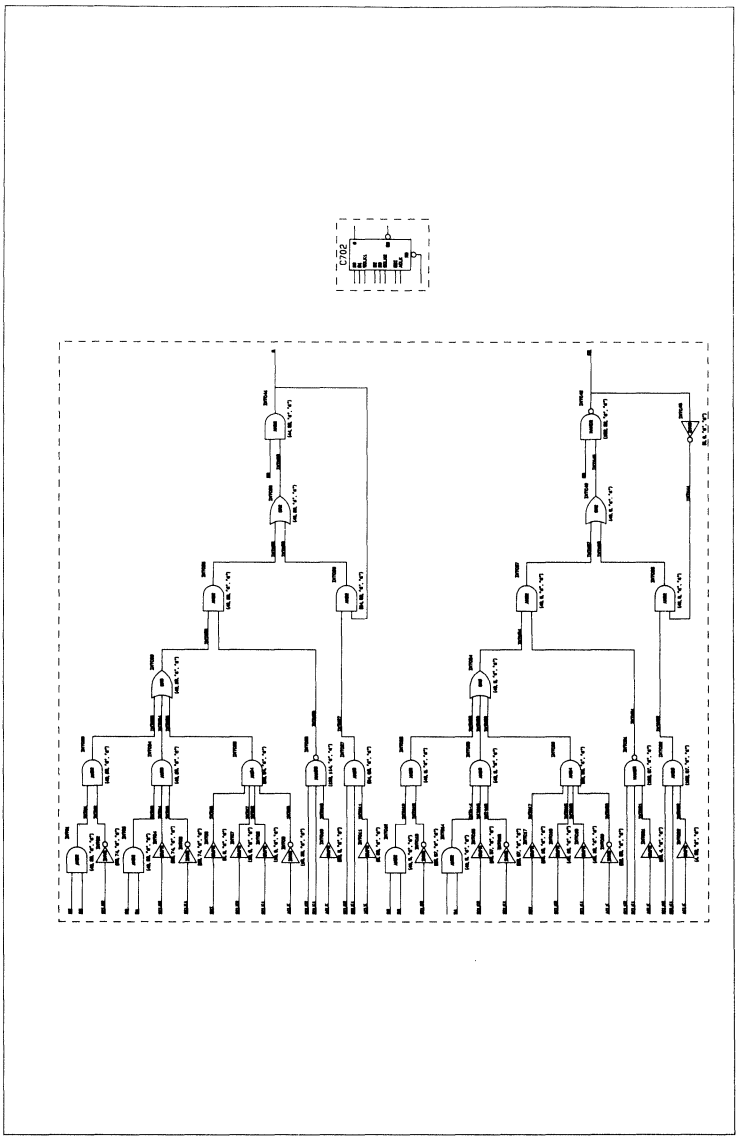
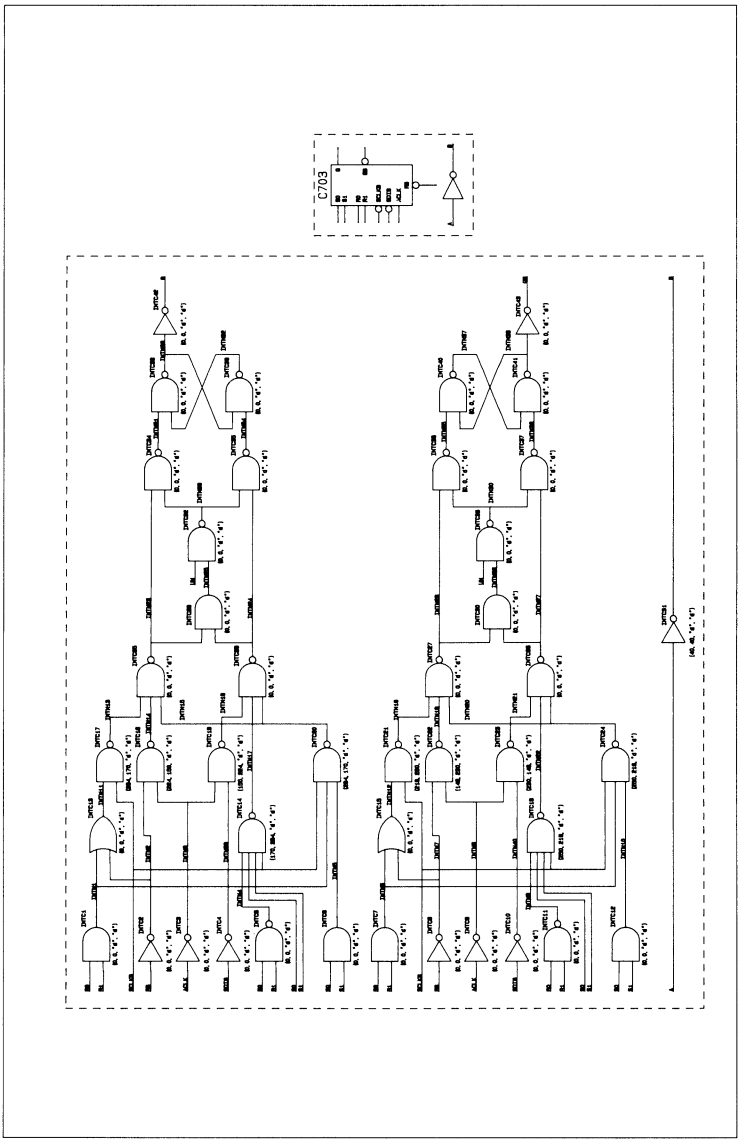
COMPONENT PLOTS

Plot 72



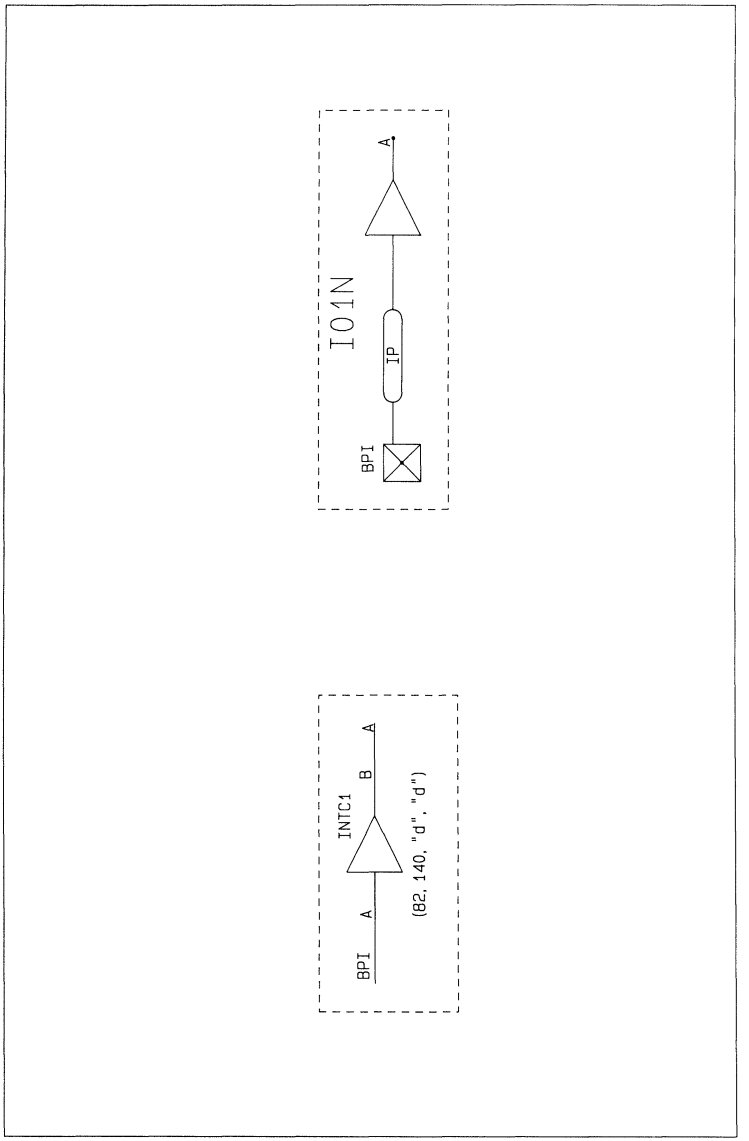
COMPONENT PLOTS

Plot 73



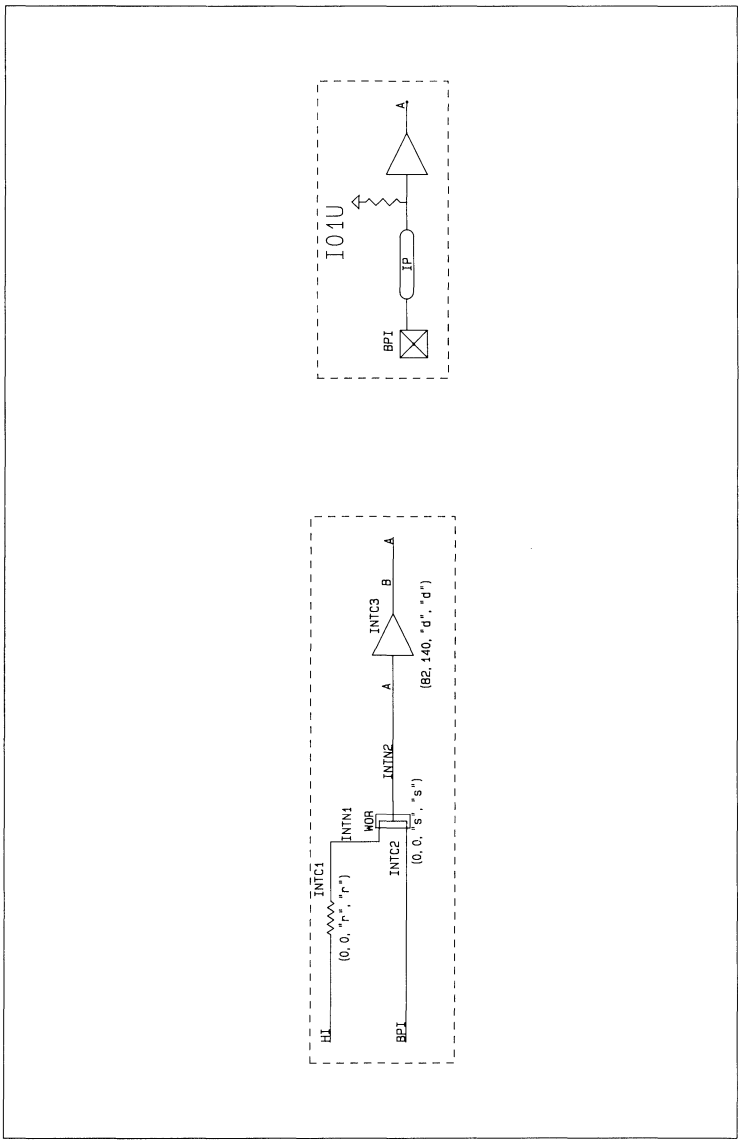
COMPONENT PLOTS

Plot 74



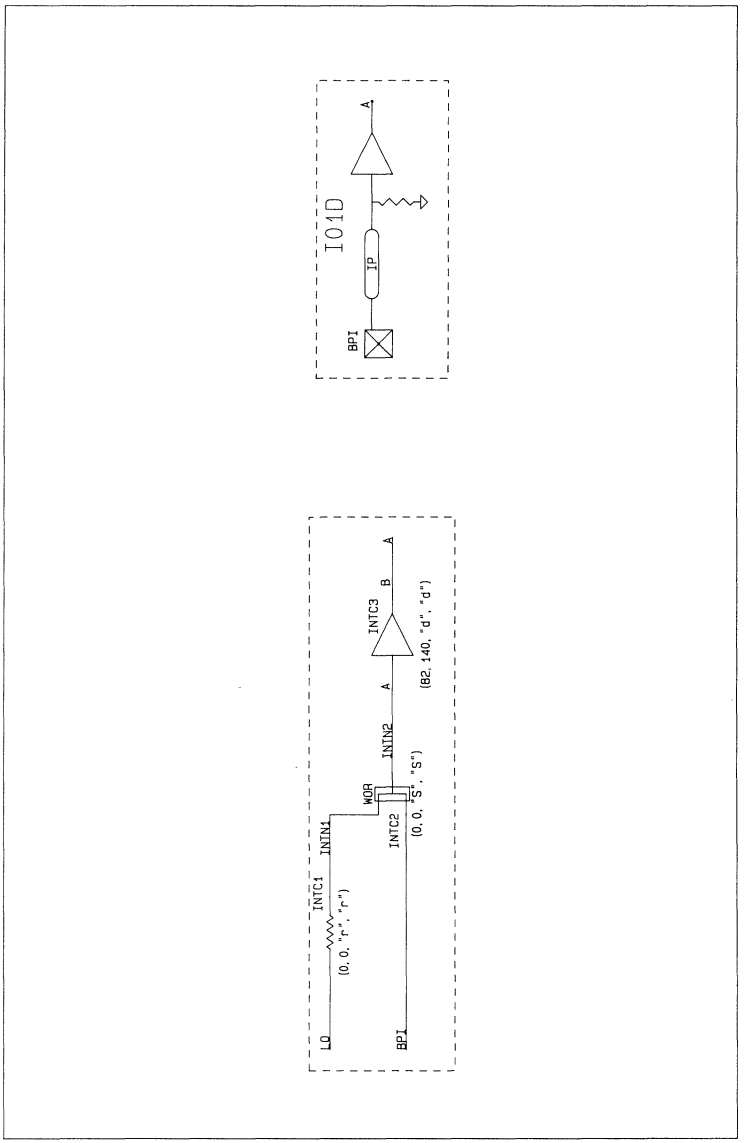
COMPONENT PLOTS

Plot 75



COMPONENT PLOTS

Plot 76



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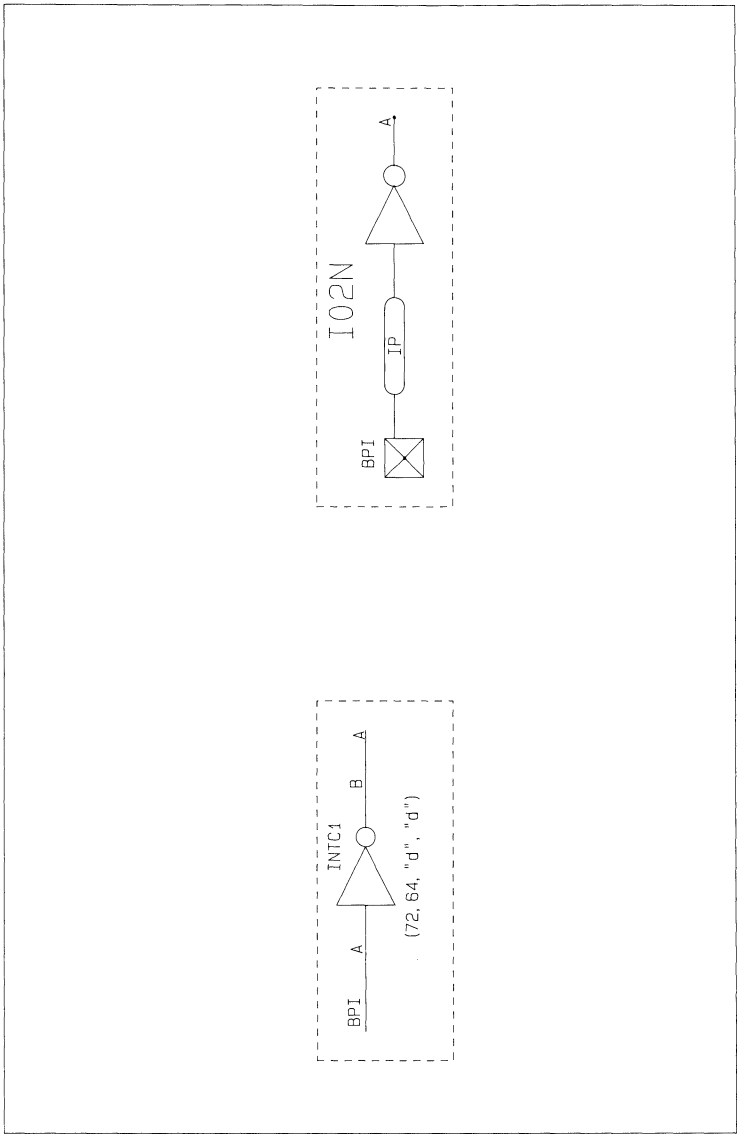
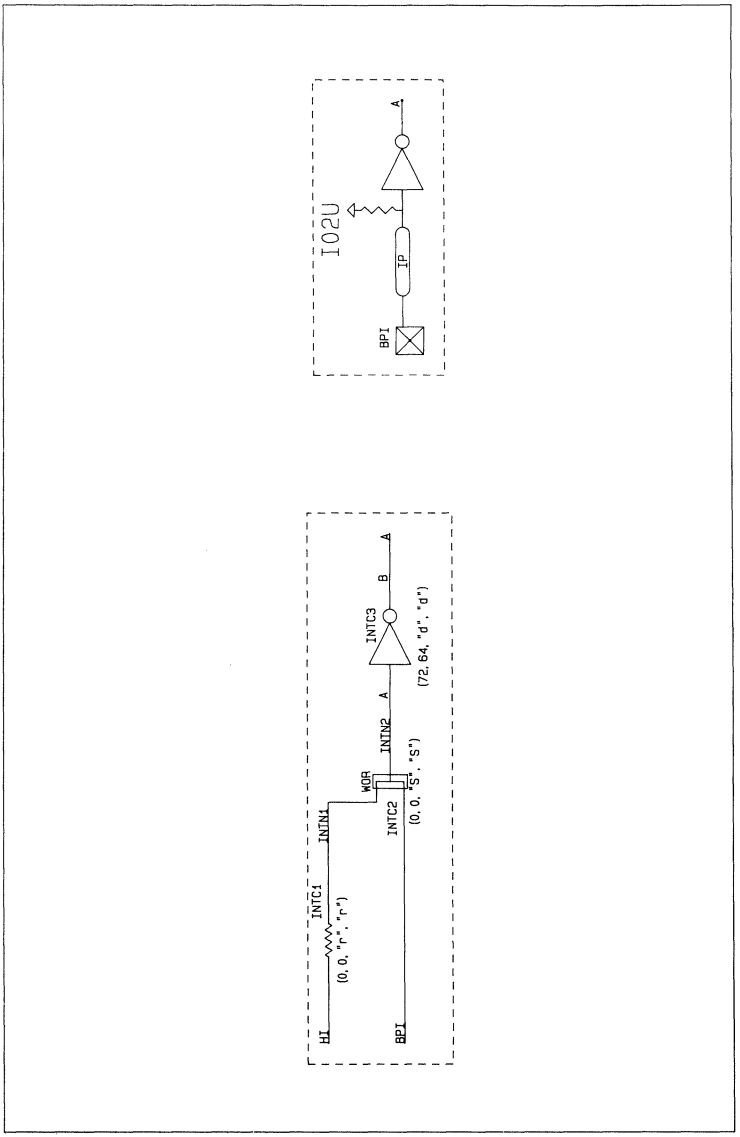
COMPONENT PLOTS

Plot 77



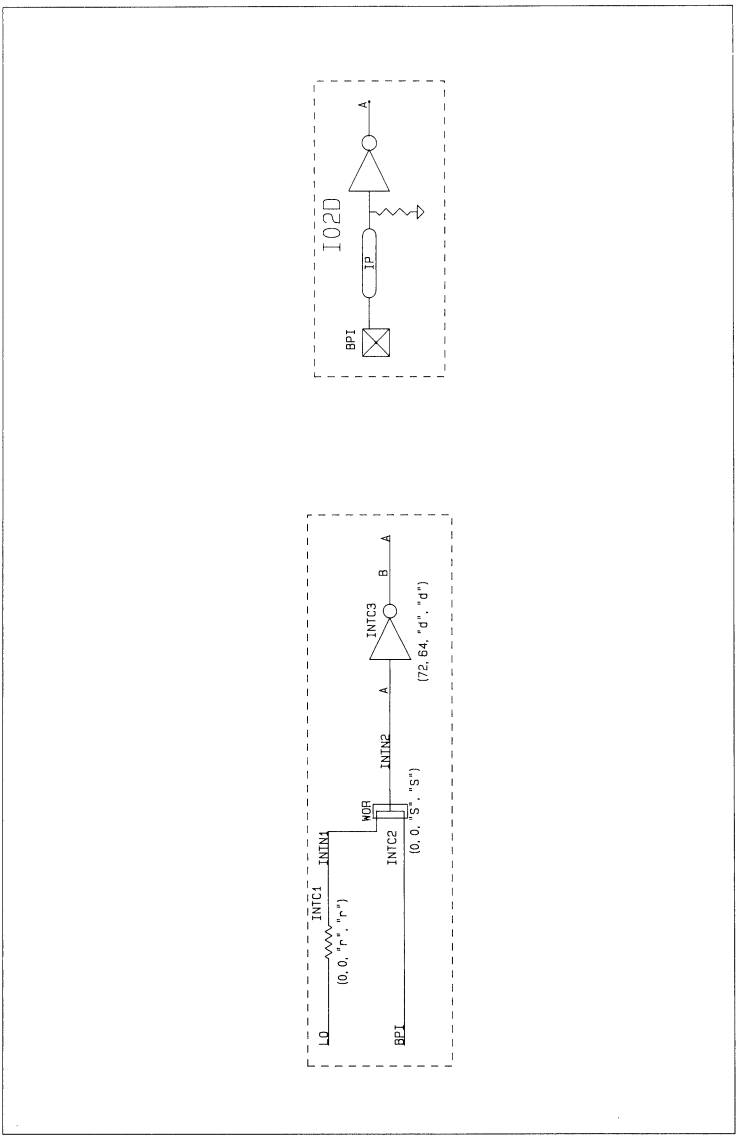
COMPONENT PLOTS

Plot 78



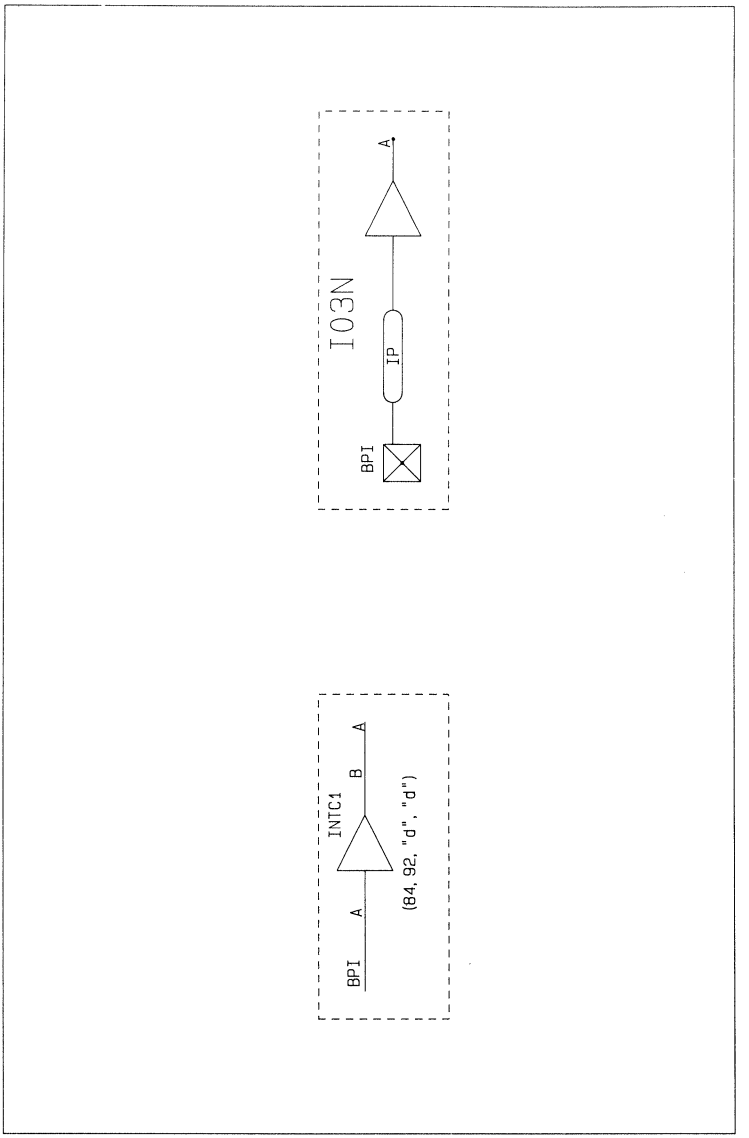
COMPONENT PLOTS

Plot 79



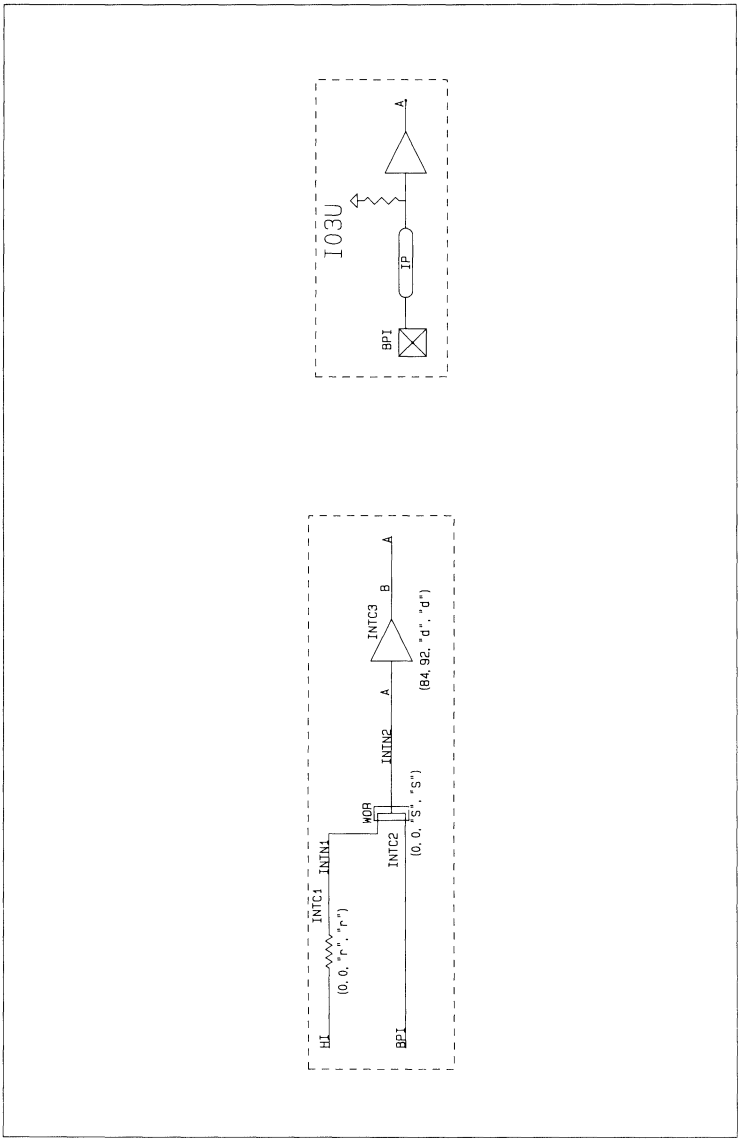
COMPONENT PLOTS

Plot 80



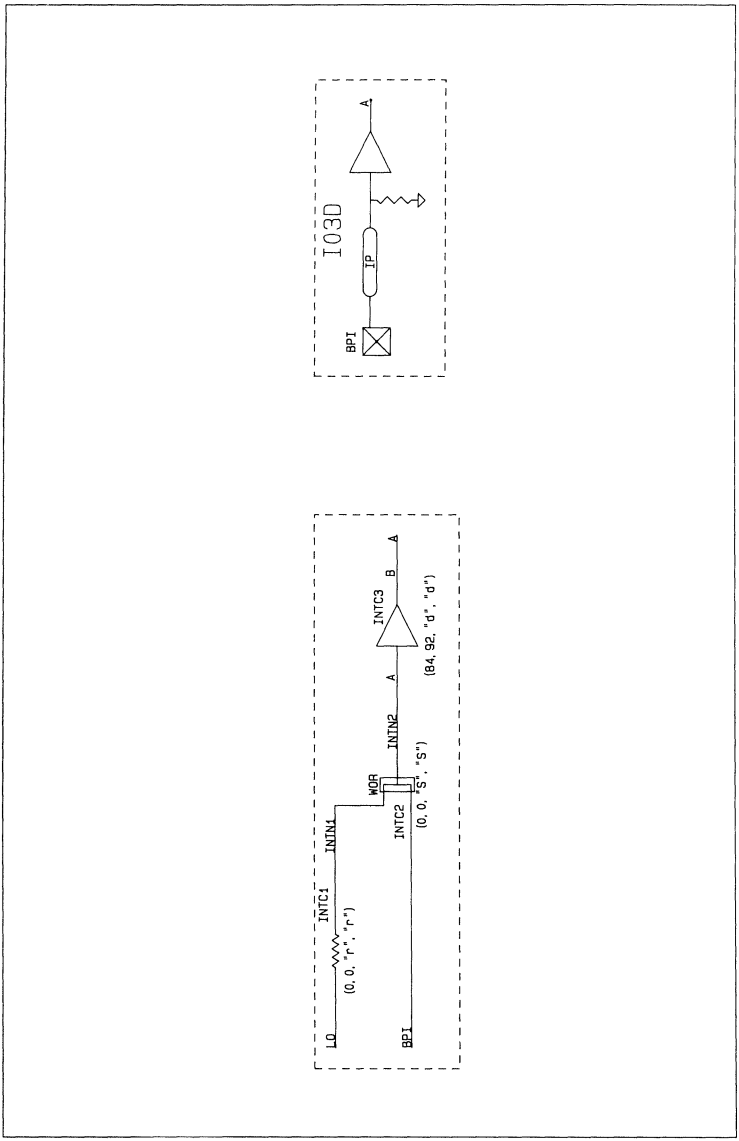
COMPONENT PLOTS

Plot 81



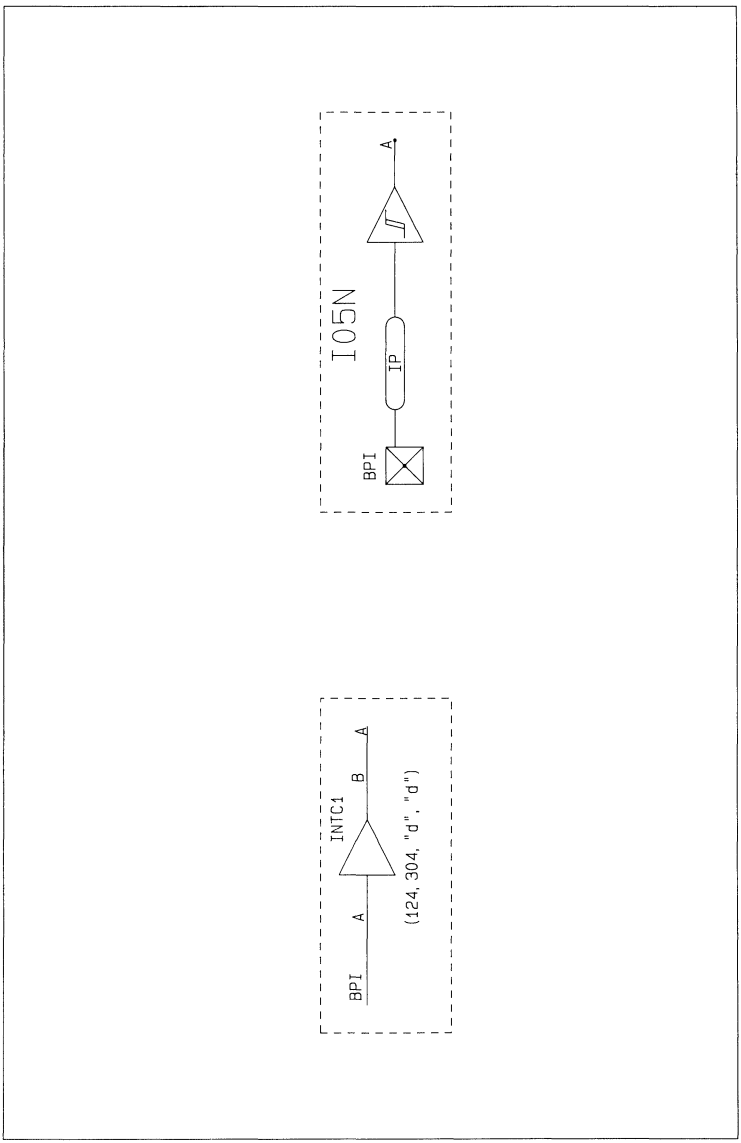
COMPONENT PLOTS

Plot 82



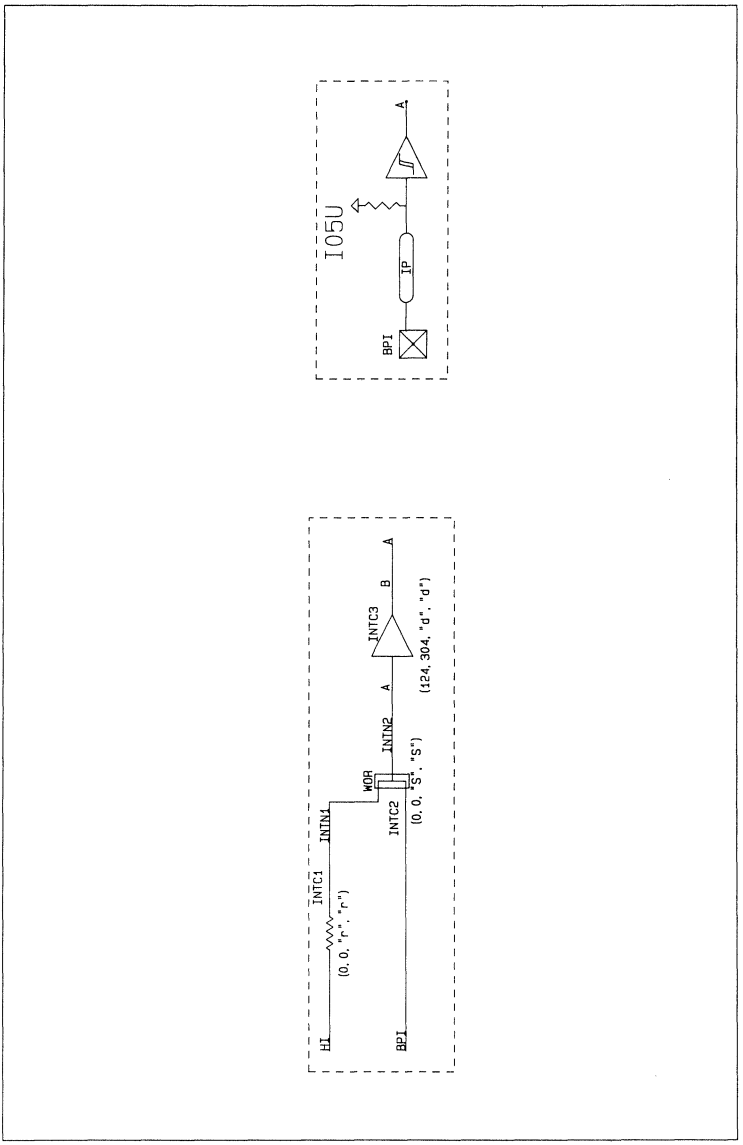
COMPONENT PLOTS

Plot 83



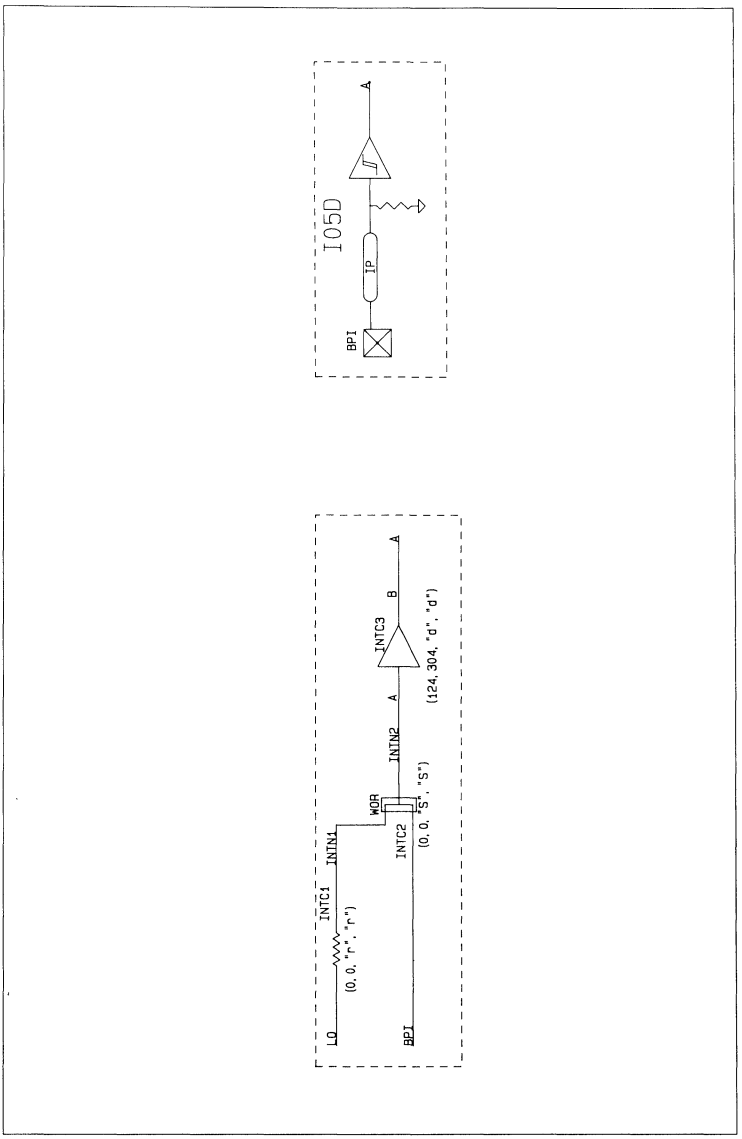
COMPONENT PLOTS

Plot 84



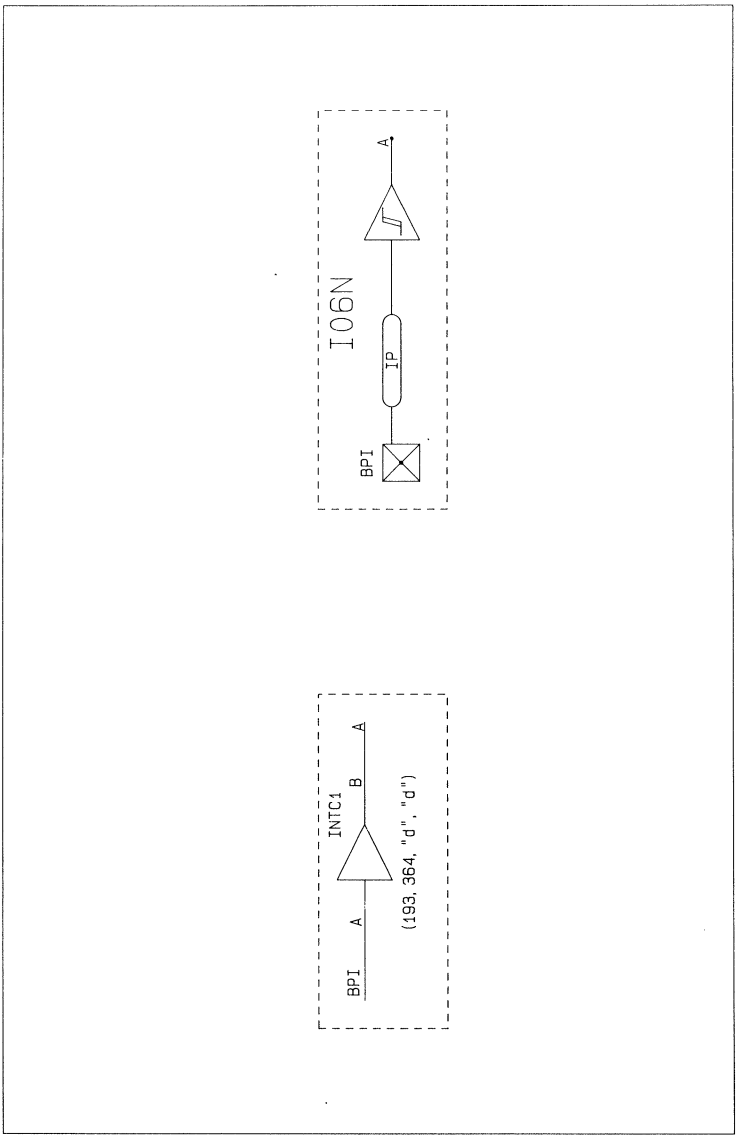
COMPONENT PLOTS

Plot 85



COMPONENT PLOTS

Plot 86



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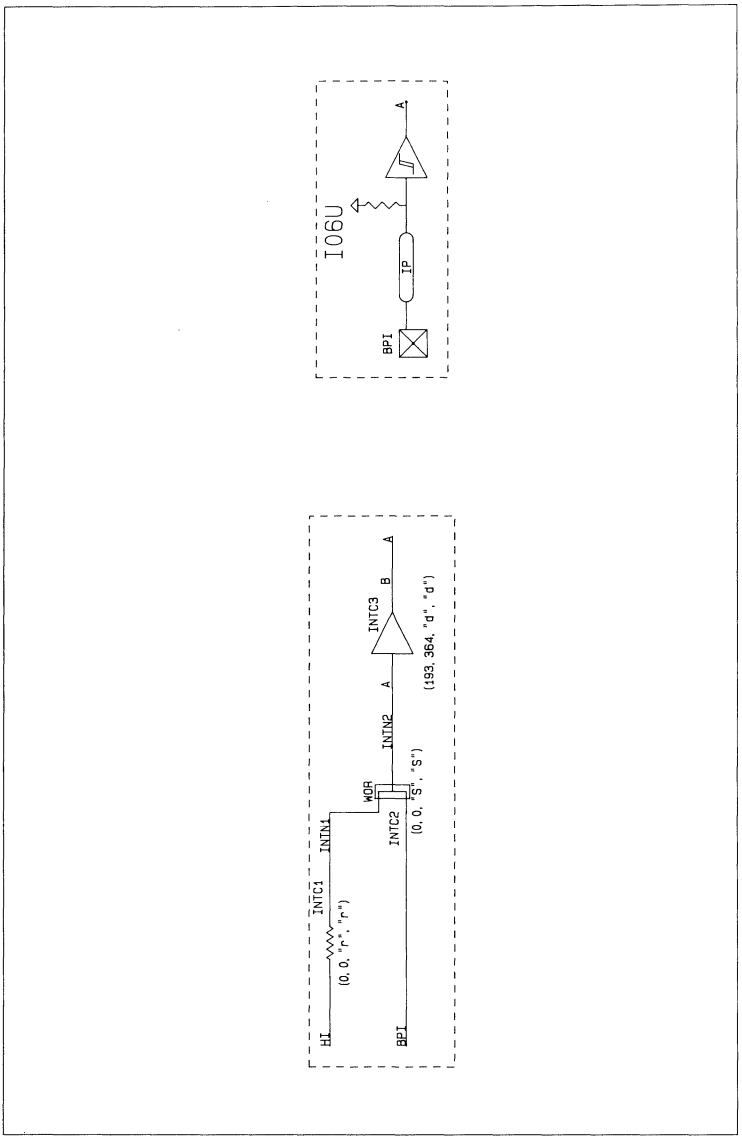
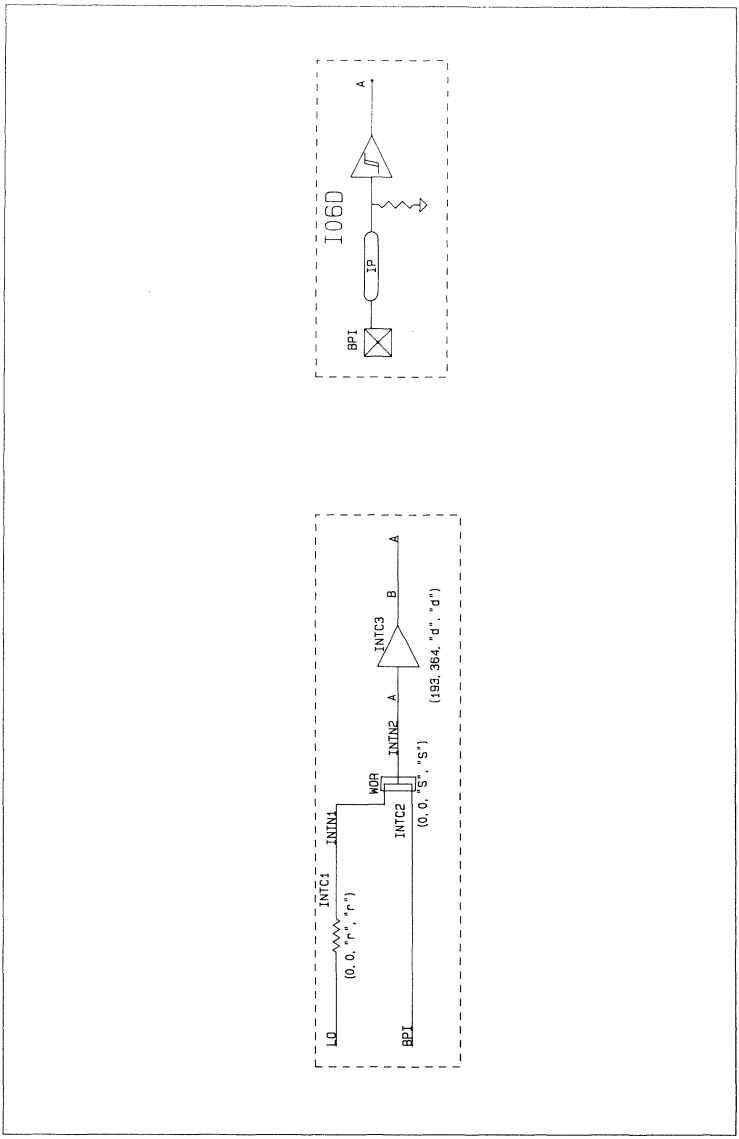
COMPONENT PLOTS

Plot 87



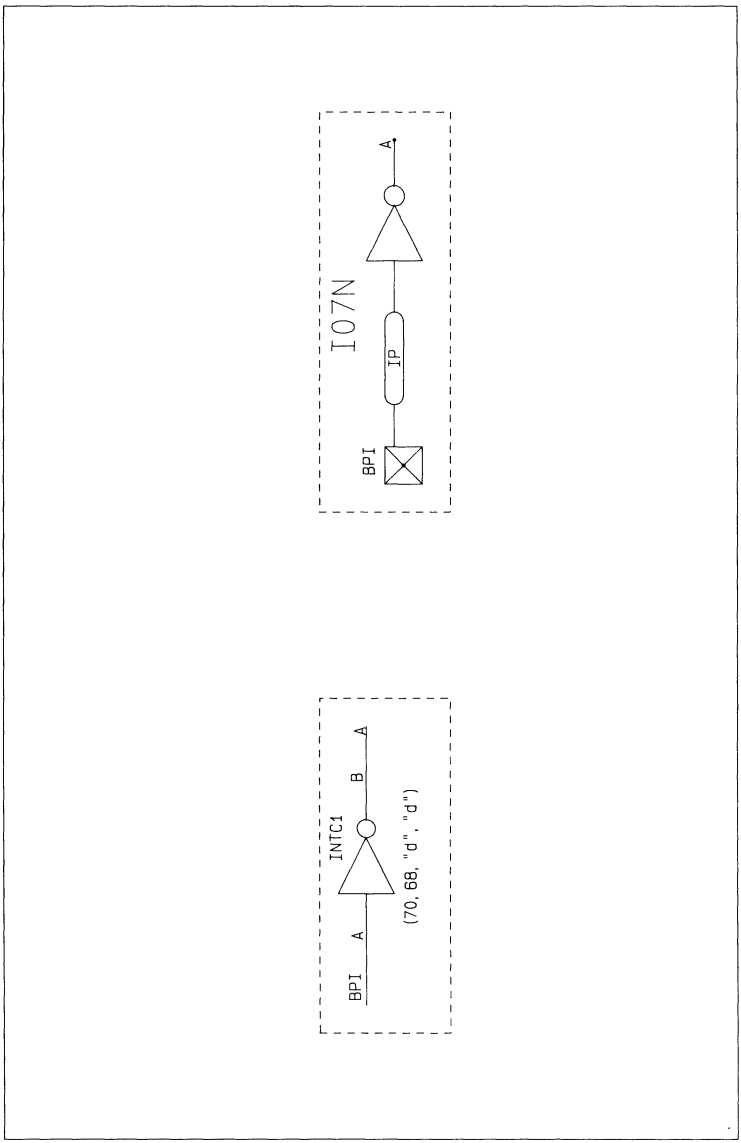
COMPONENT PLOTS

Plot 88



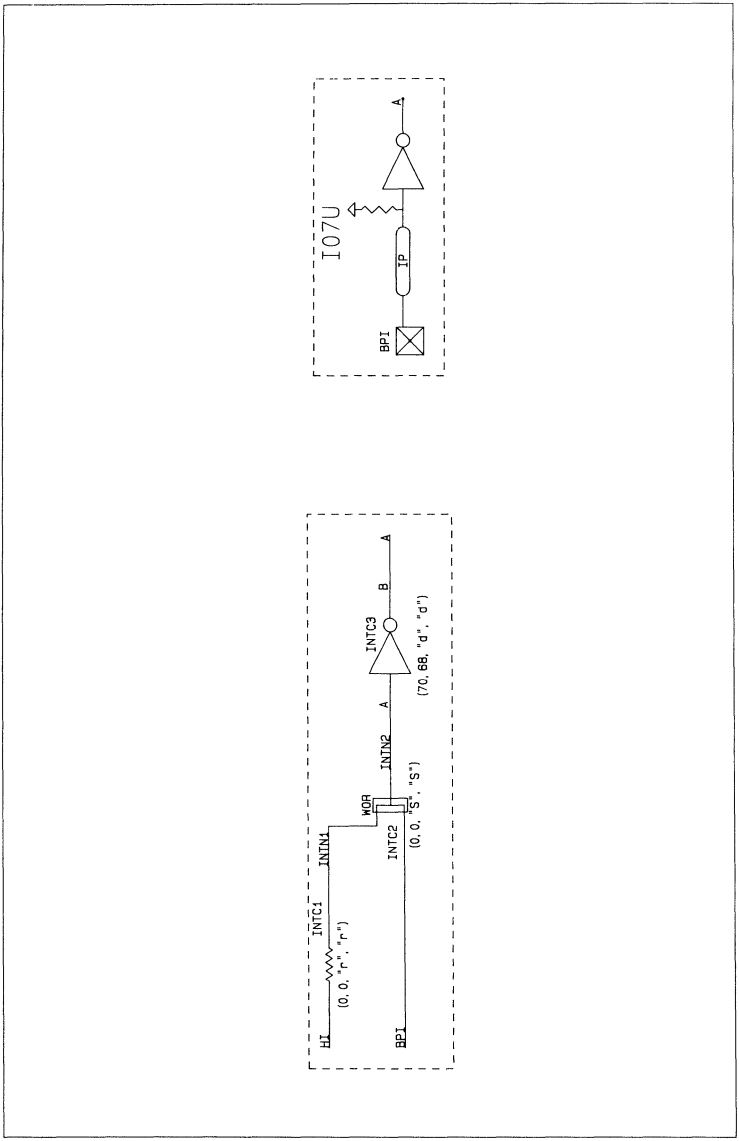
COMPONENT PLOTS

Plot 89



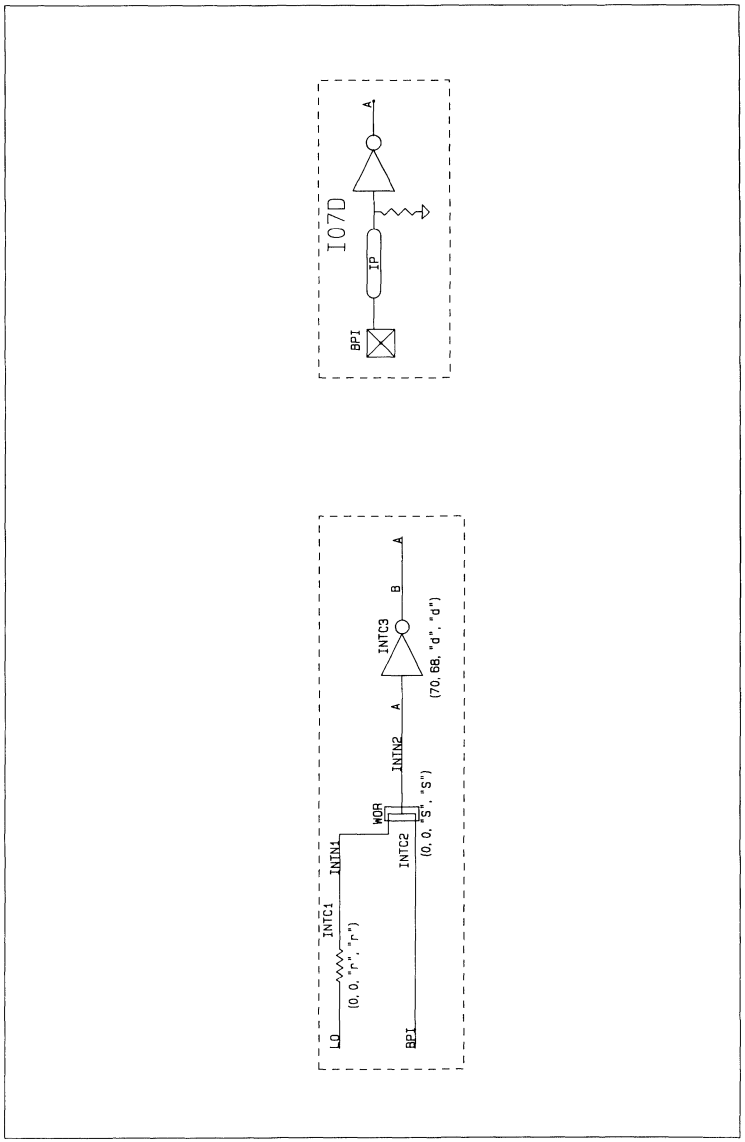
COMPONENT PLOTS

Plot 90



COMPONENT PLOTS

Plot 91



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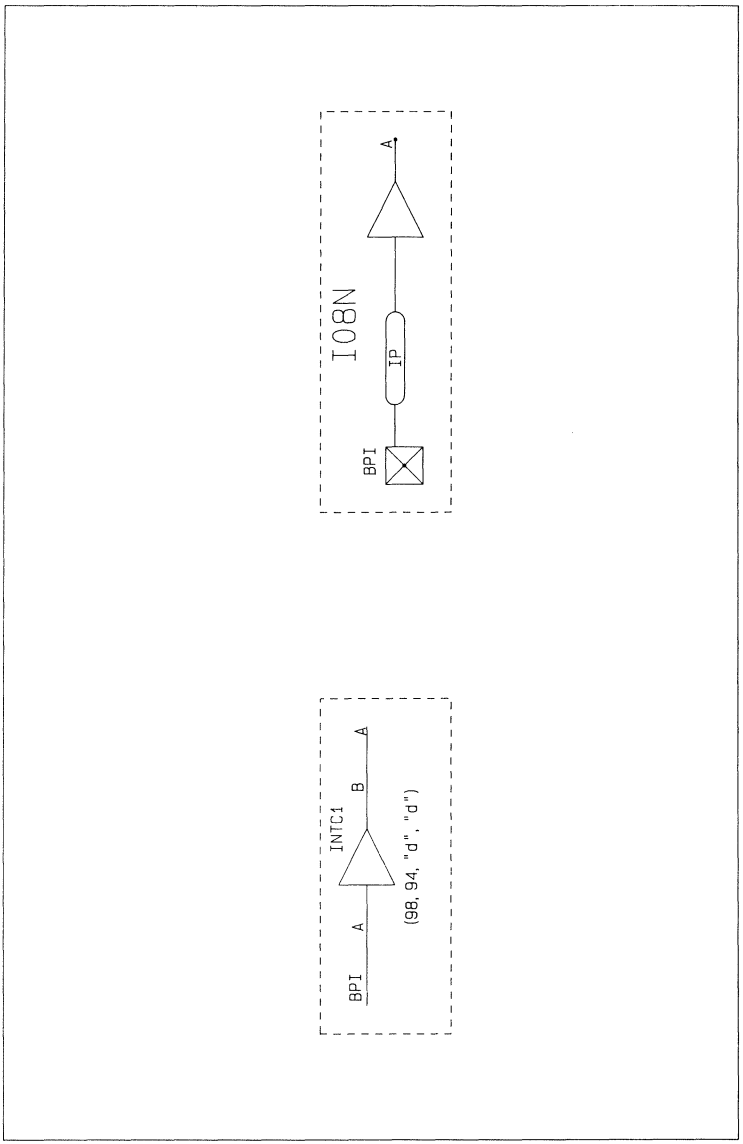
COMPONENT PLOTS

Plot 92



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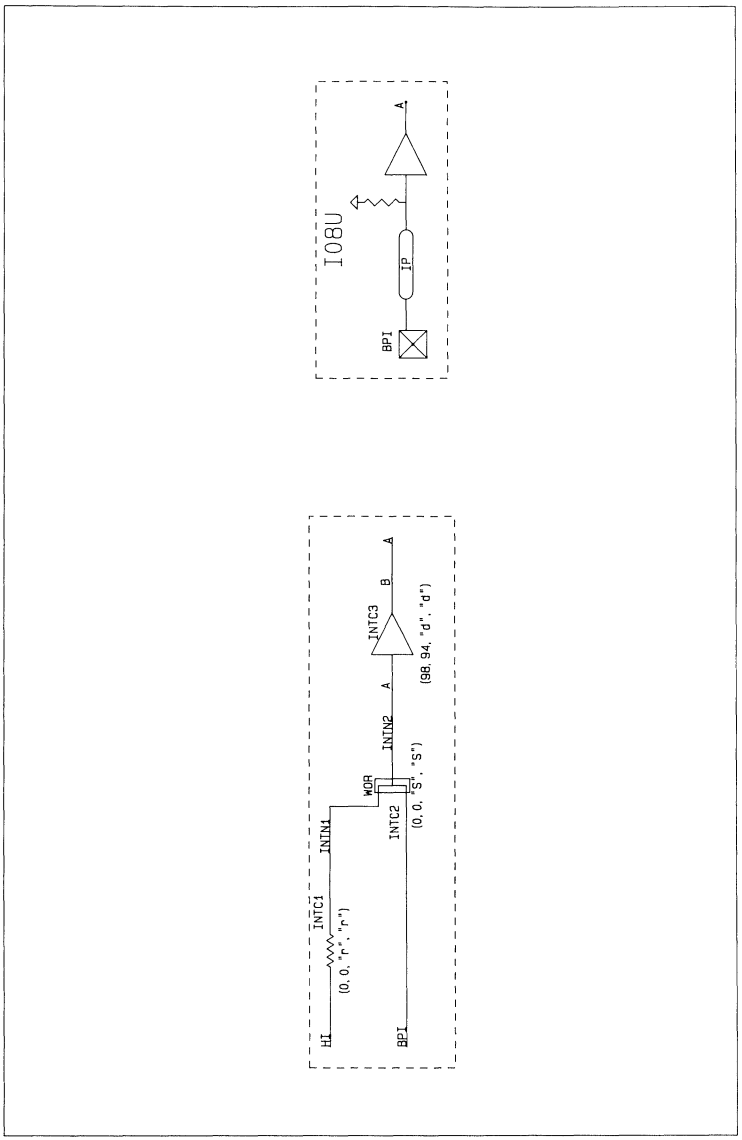
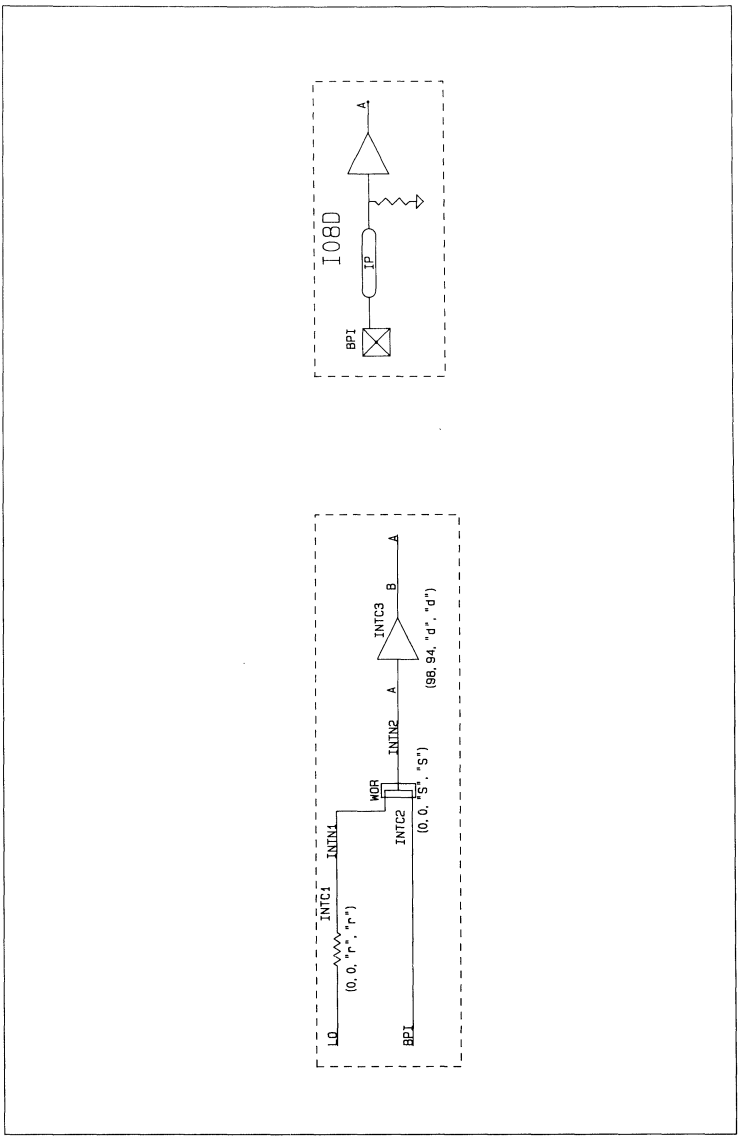
COMPONENT PLOTS

Plot 93



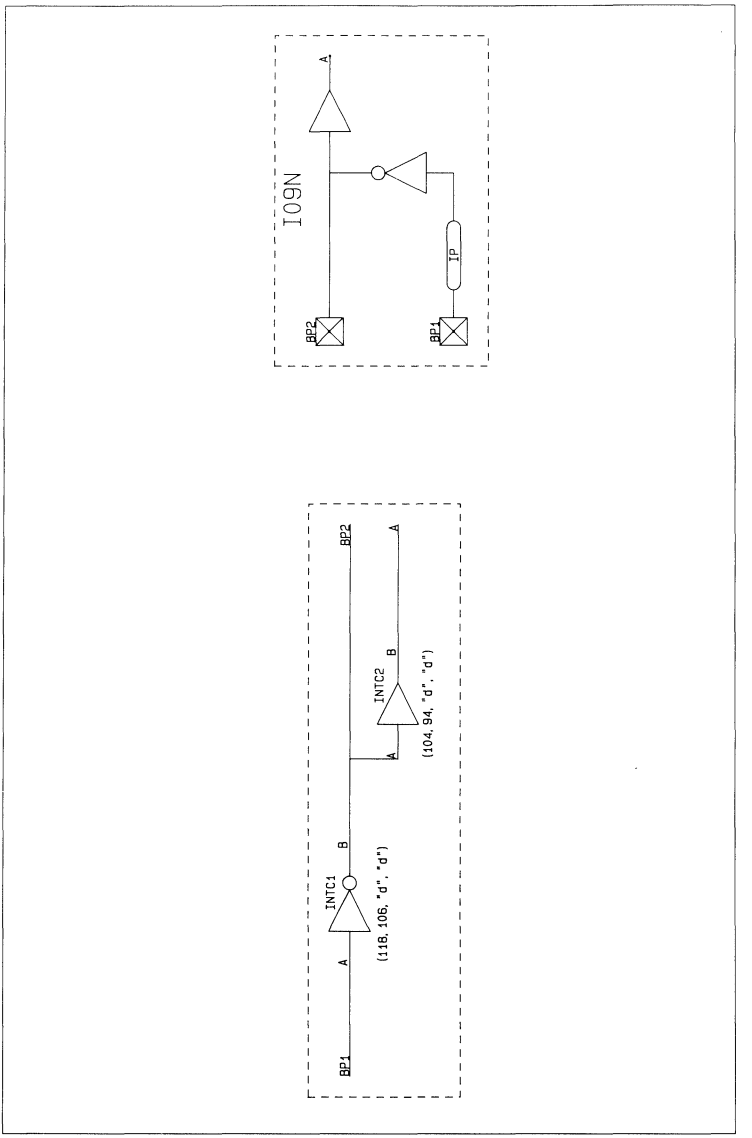
COMPONENT PLOTS

Plot 94



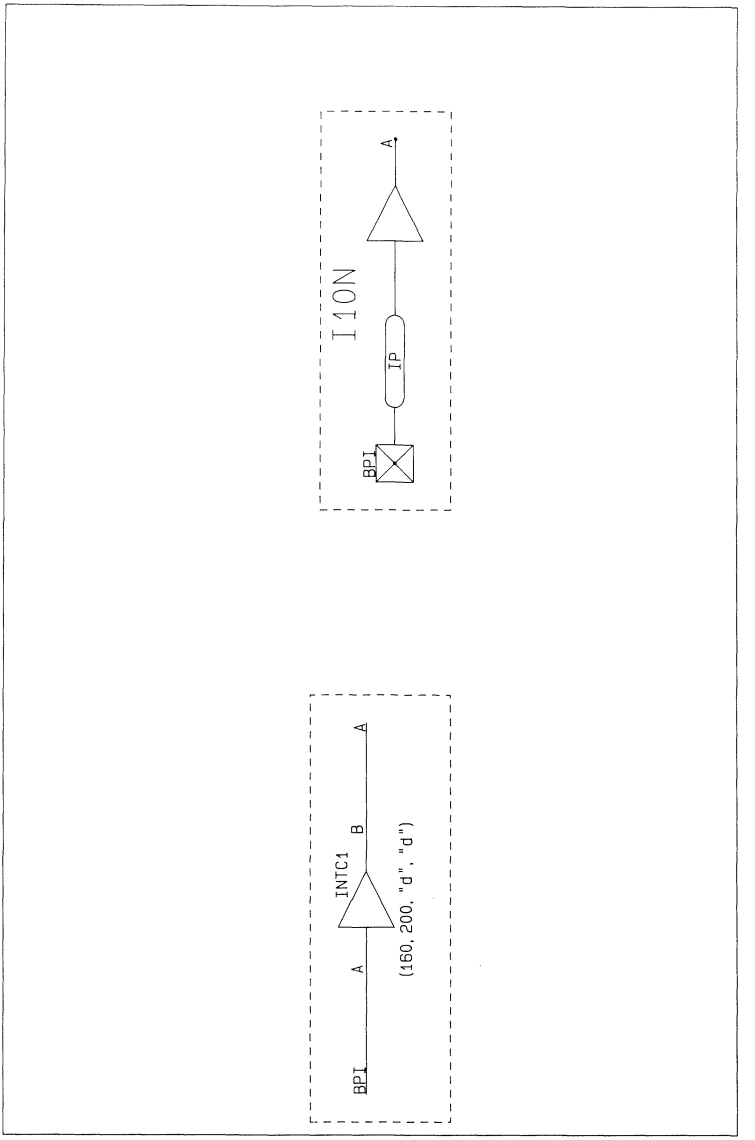
COMPONENT PLOTS

Plot 95



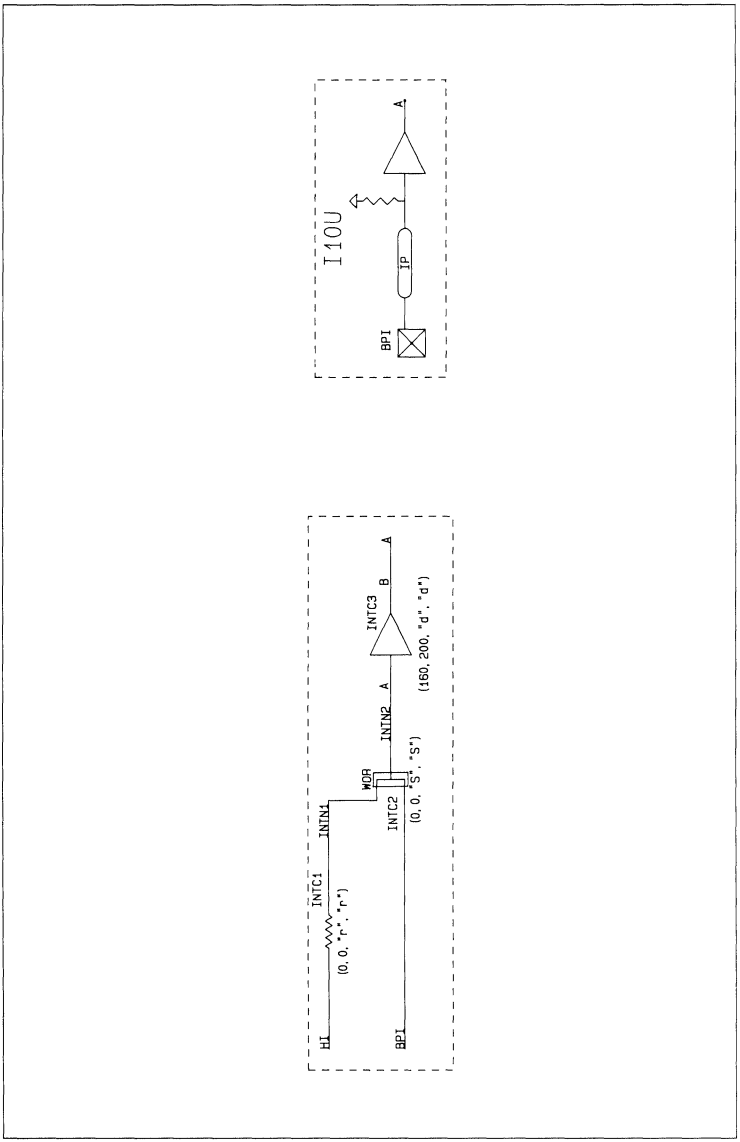
COMPONENT PLOTS

Plot 96



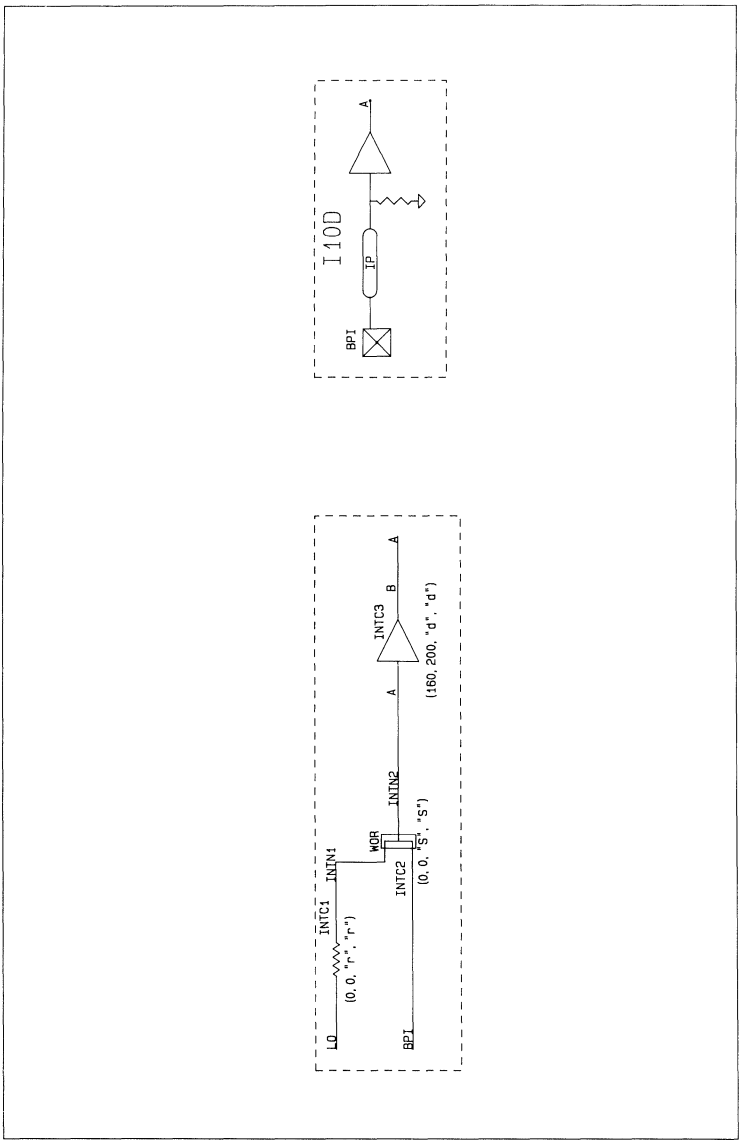
COMPONENT PLOTS

Plot 97



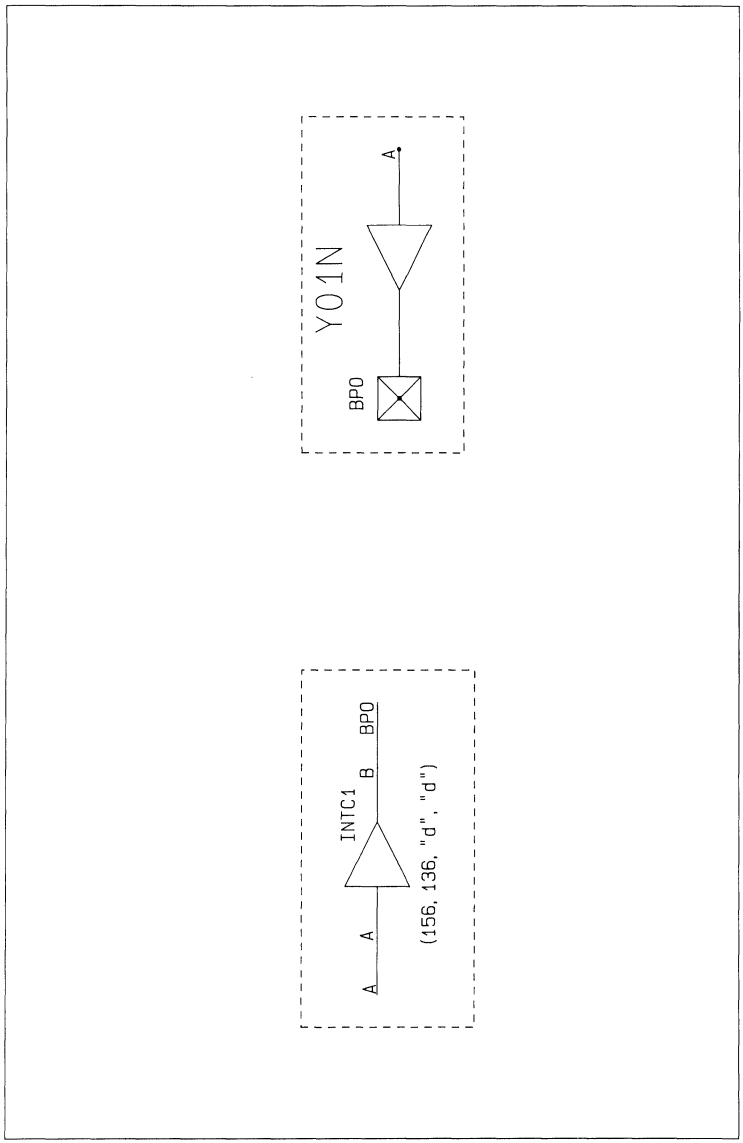
COMPONENT PLOTS

Plot 98



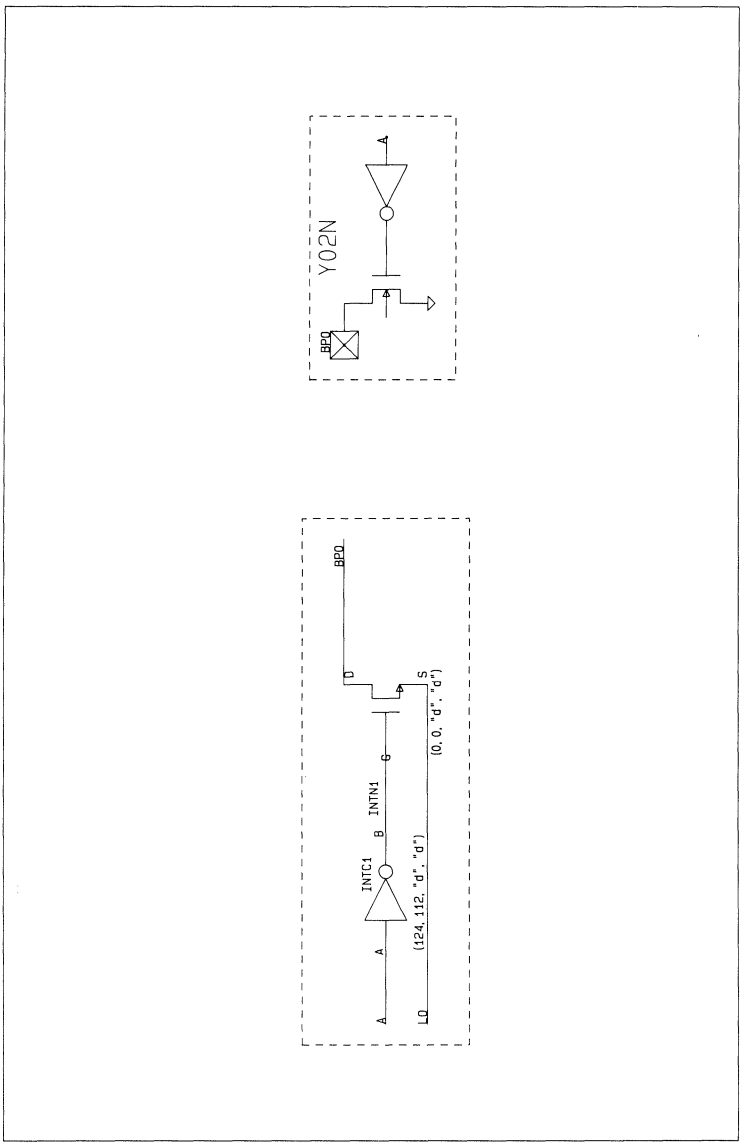
COMPONENT PLOTS

Plot 99



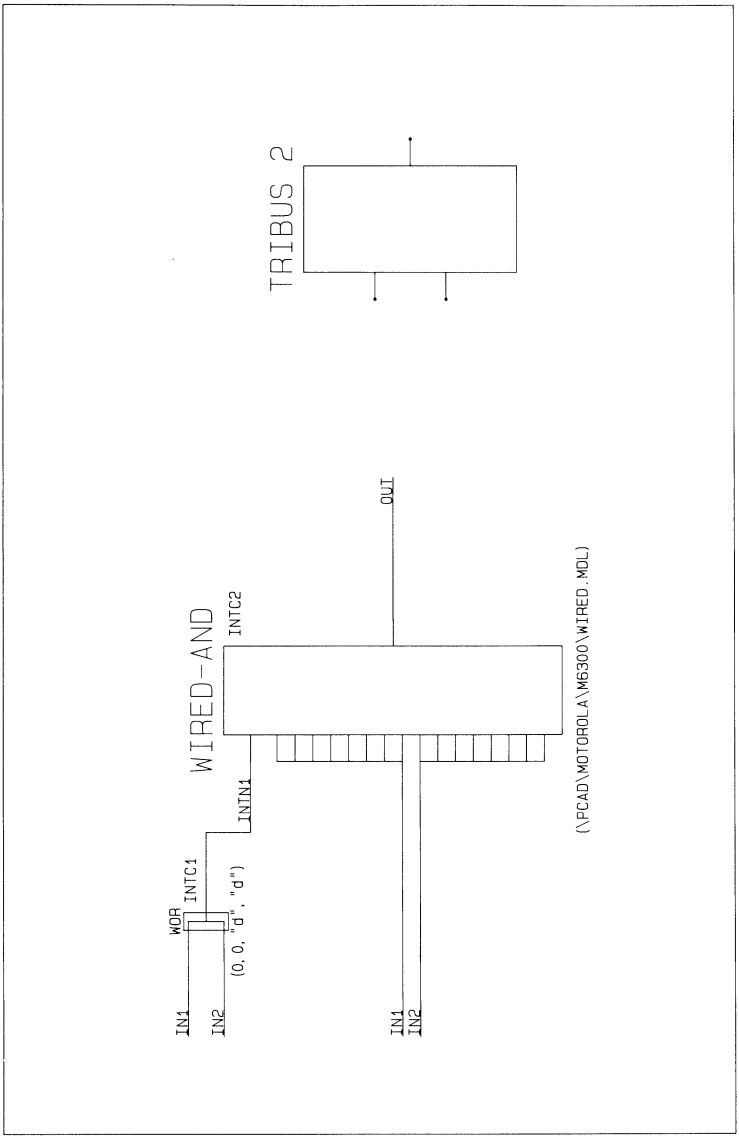
COMPONENT PLOTS

Plot 100



COMPONENT PLOTS

Plot 101



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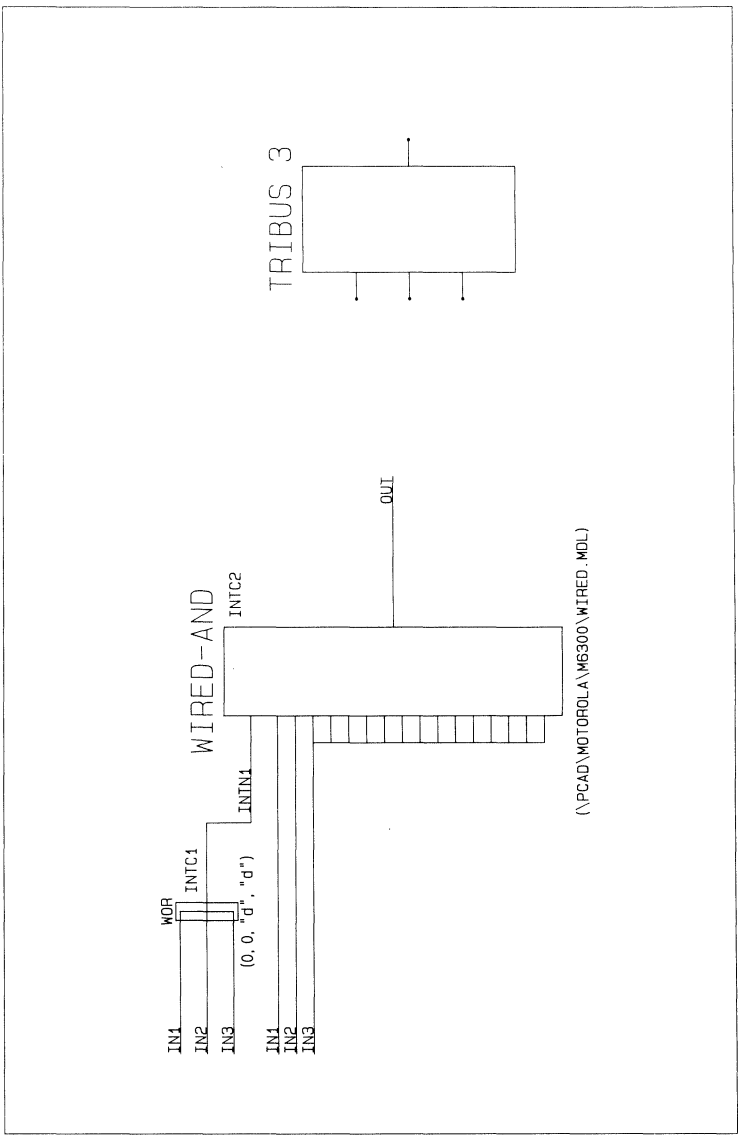
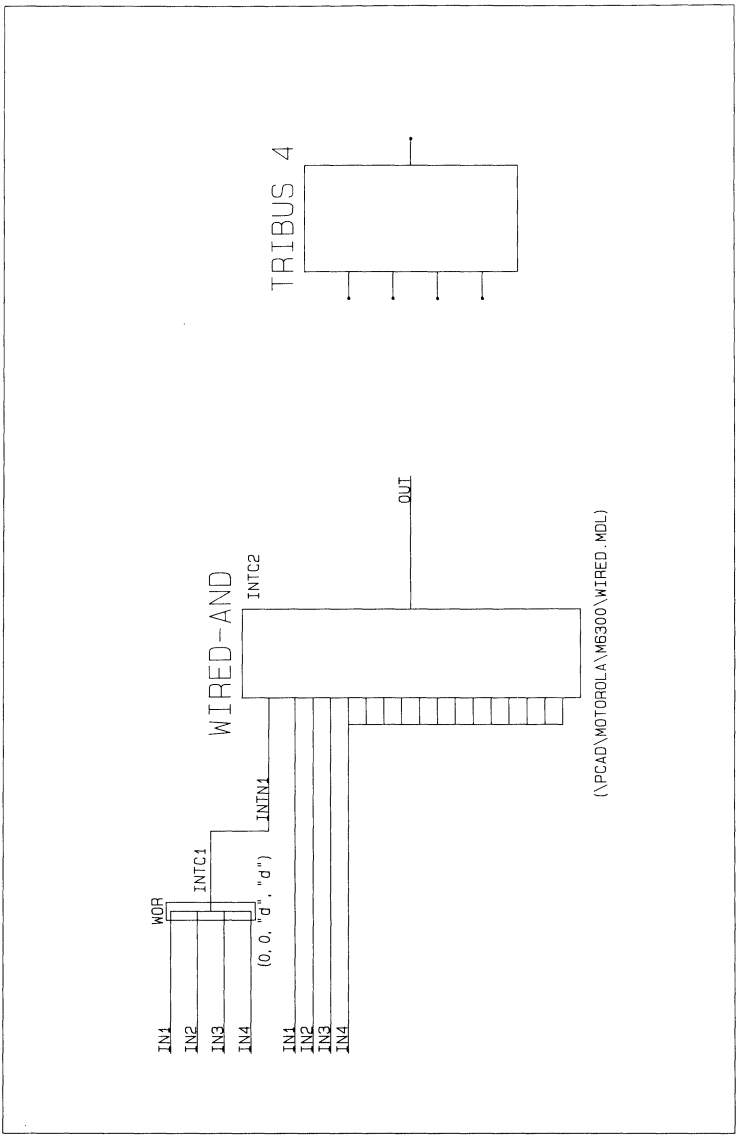
COMPONENT PLOTS

Plot 102



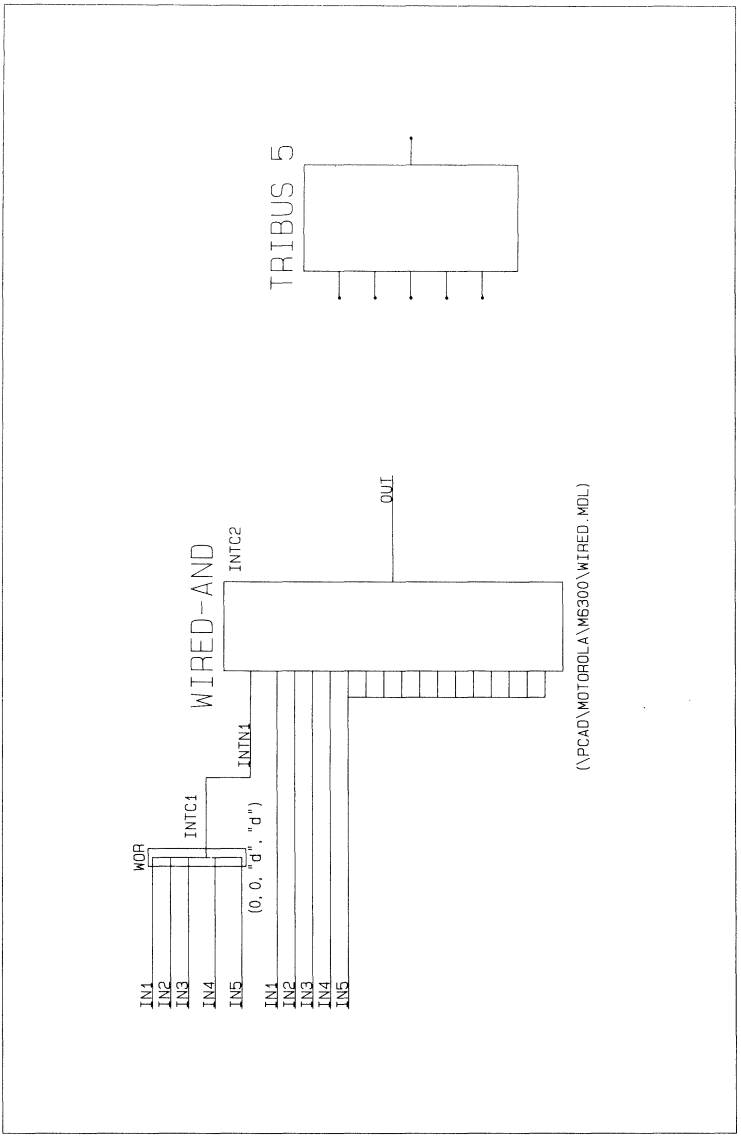
COMPONENT PLOTS

Plot 103



COMPONENT PLOTS

Plot 104



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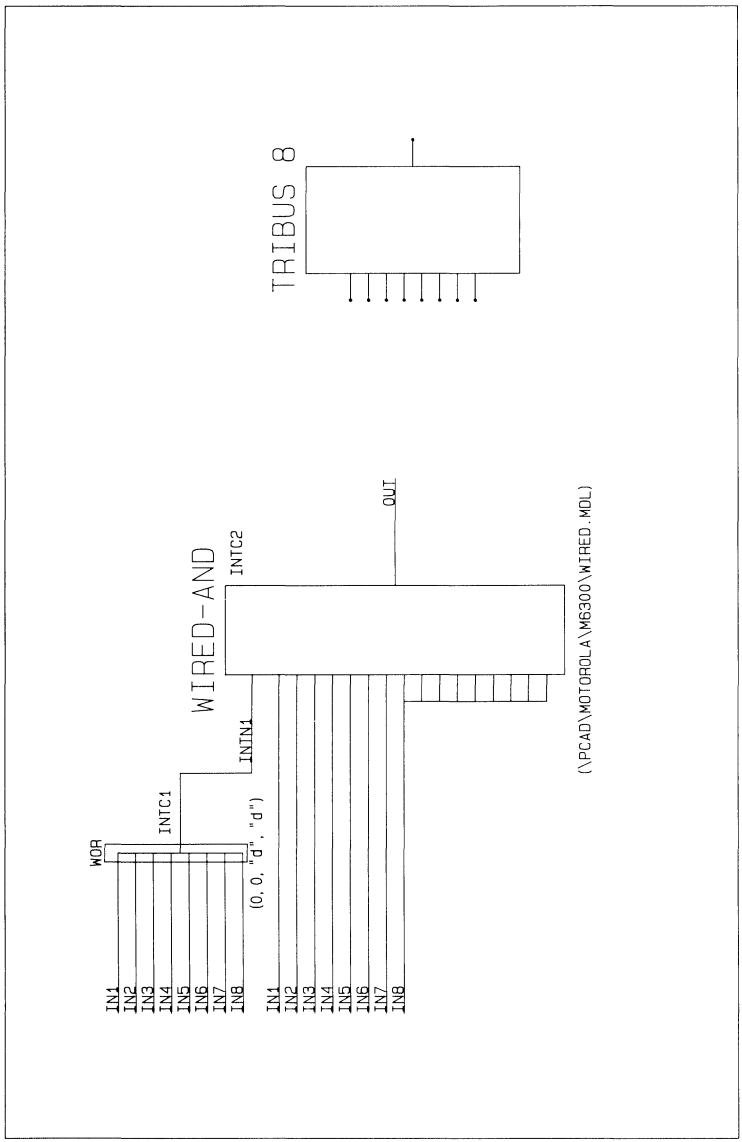
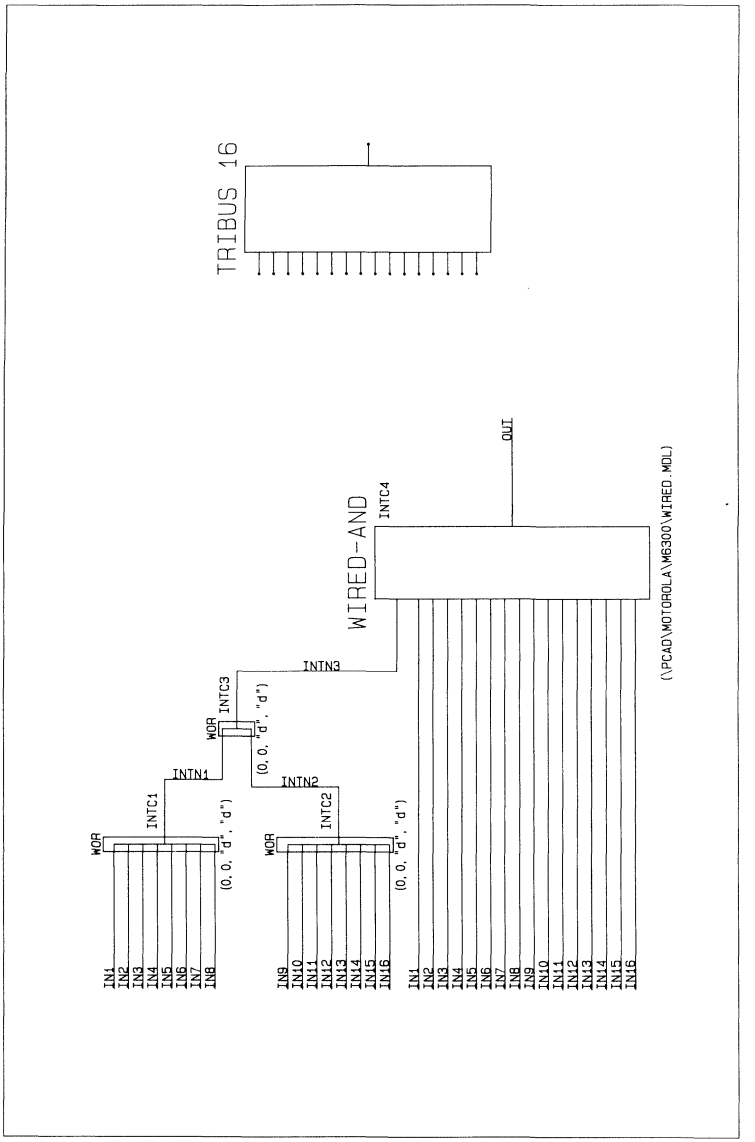
COMPONENT PLOTS

Plot 105



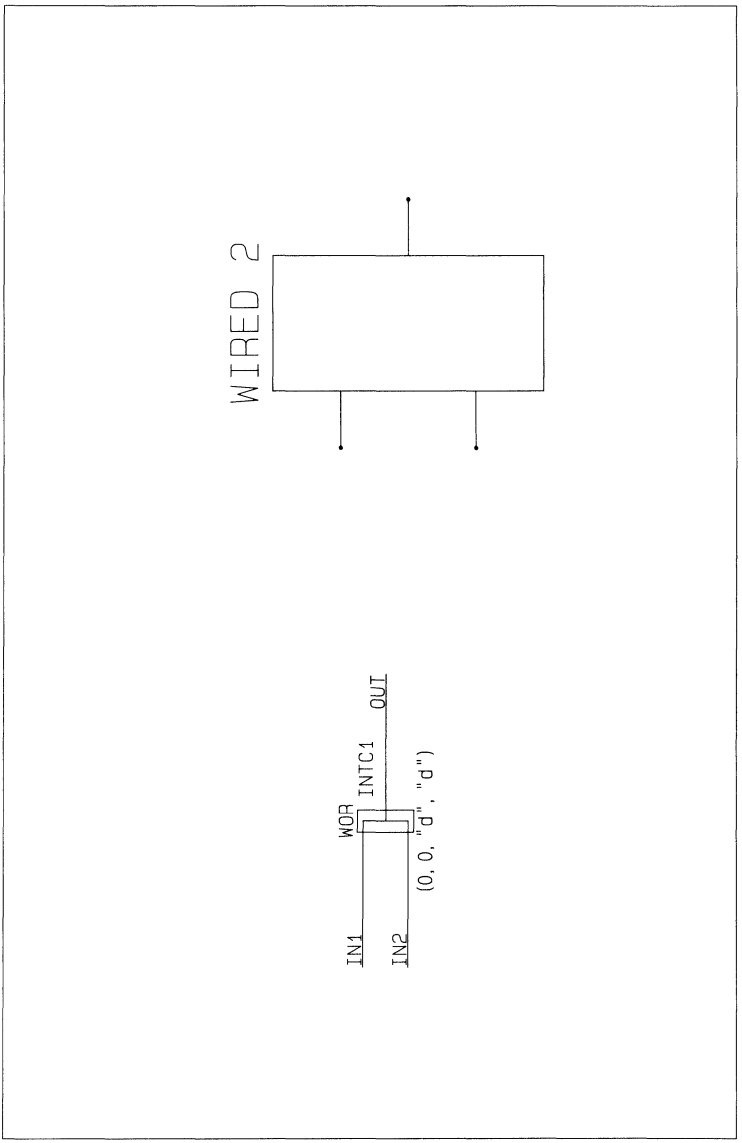
COMPONENT PLOTS

Plot 106



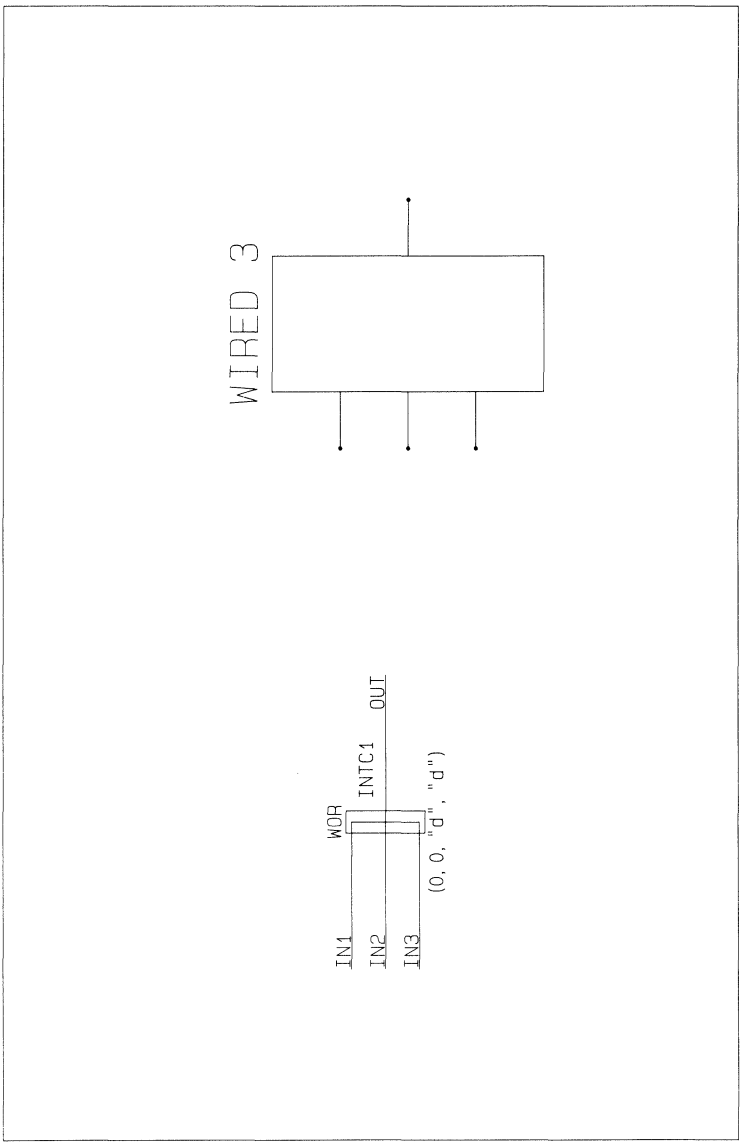
COMPONENT PLOTS

Plot 107



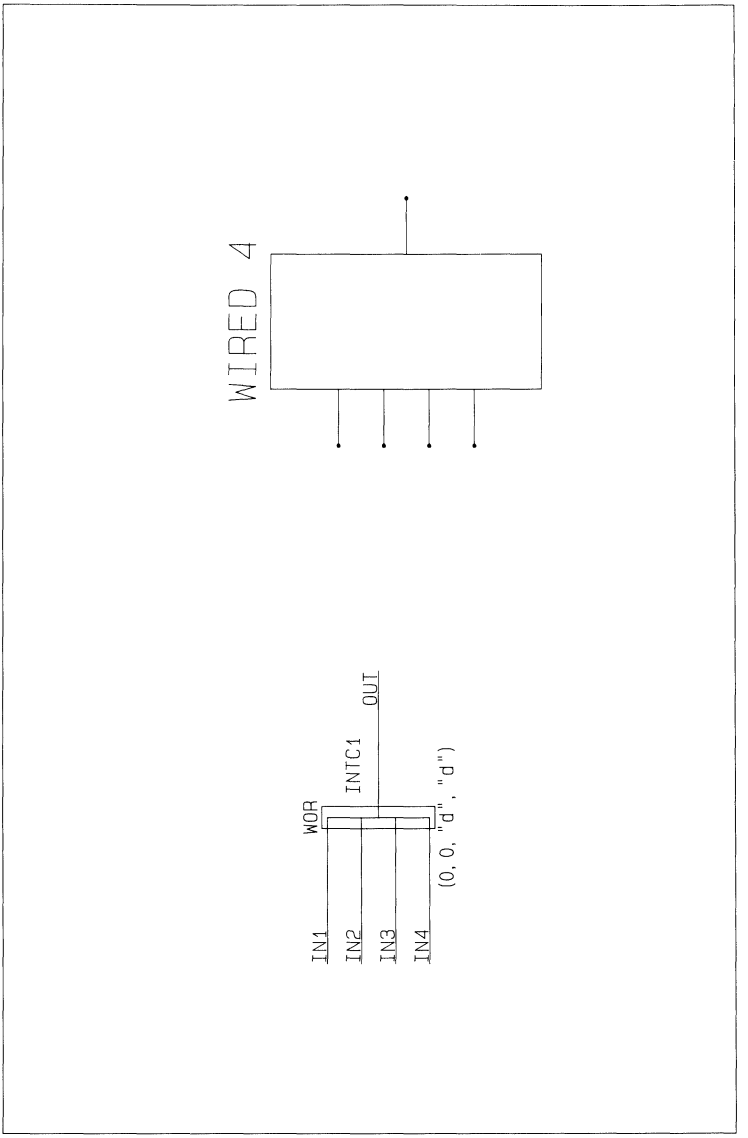
COMPONENT PLOTS

Plot 108



COMPONENT PLOTS

Plot 109



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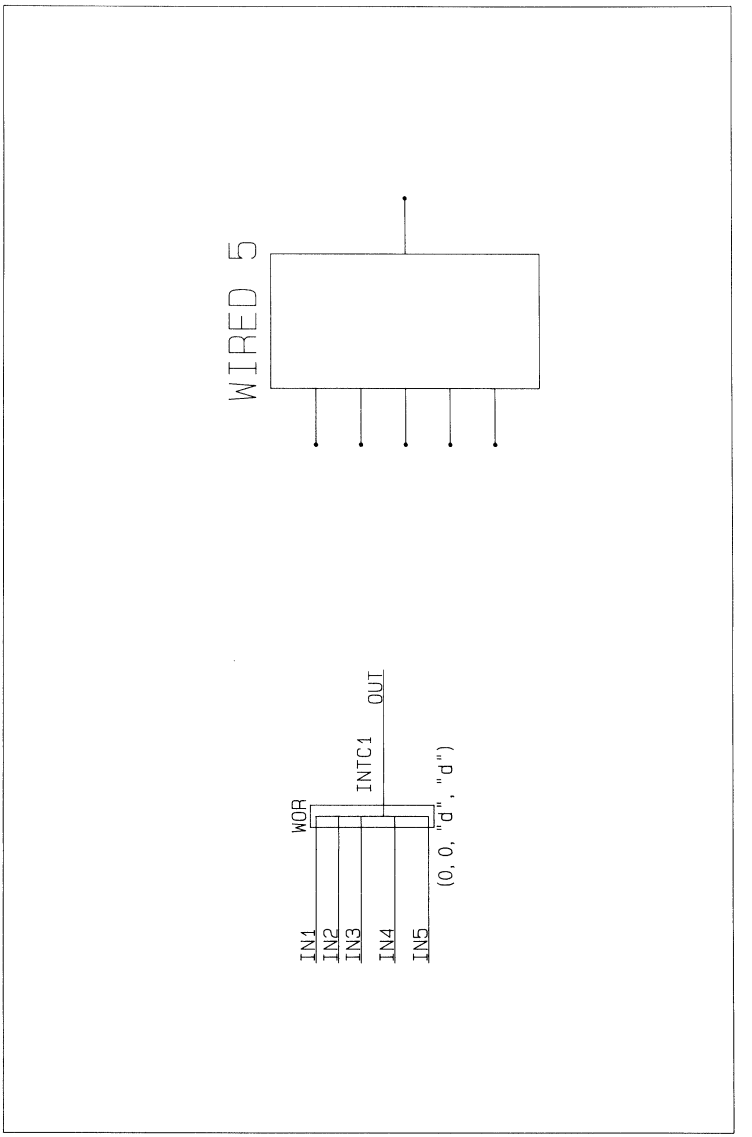
COMPONENT PLOTS

Plot 110



COMPONENT PLOTS

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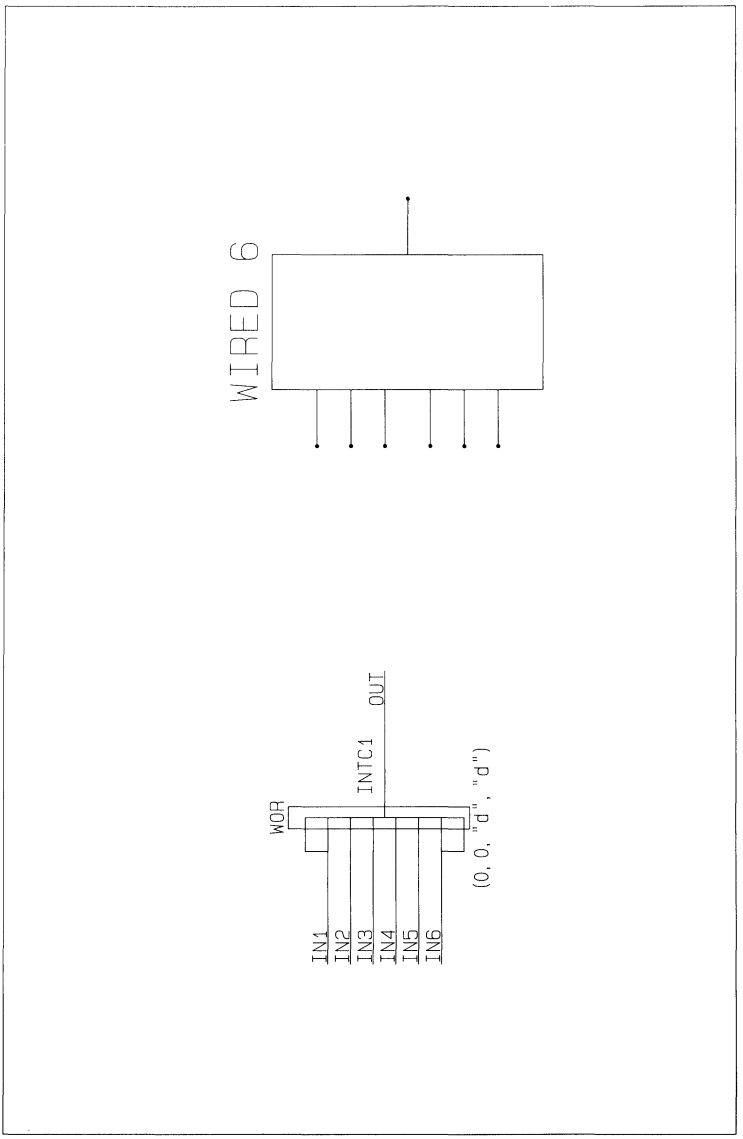
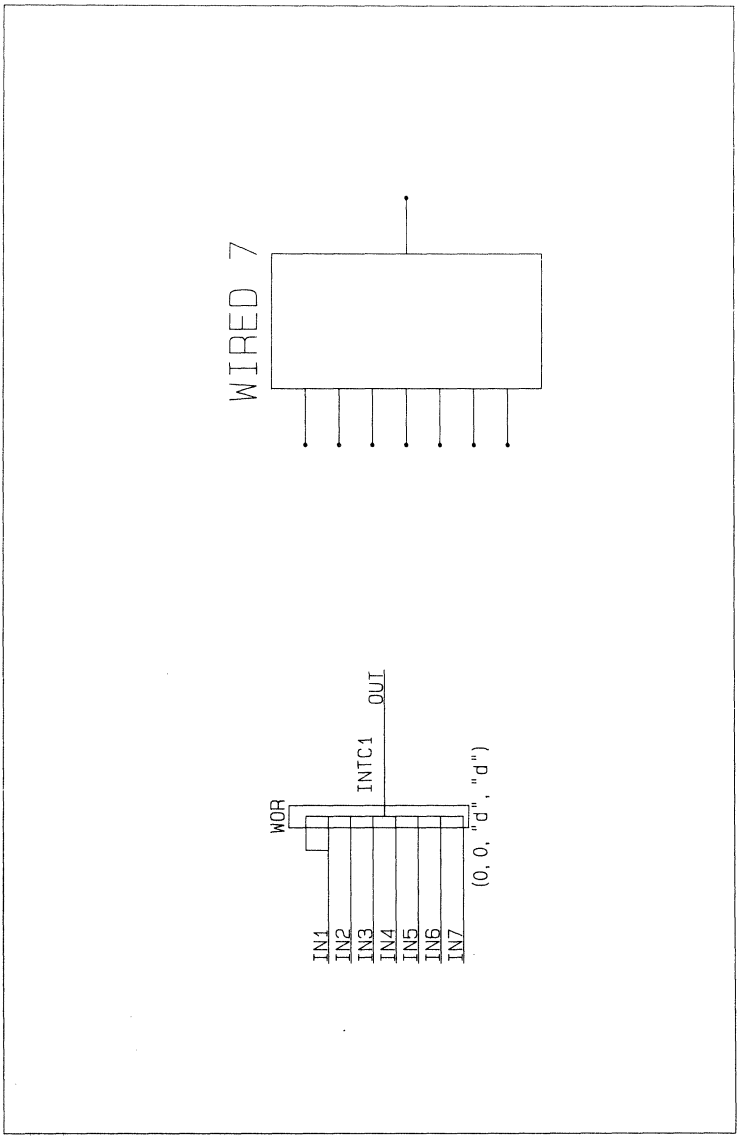


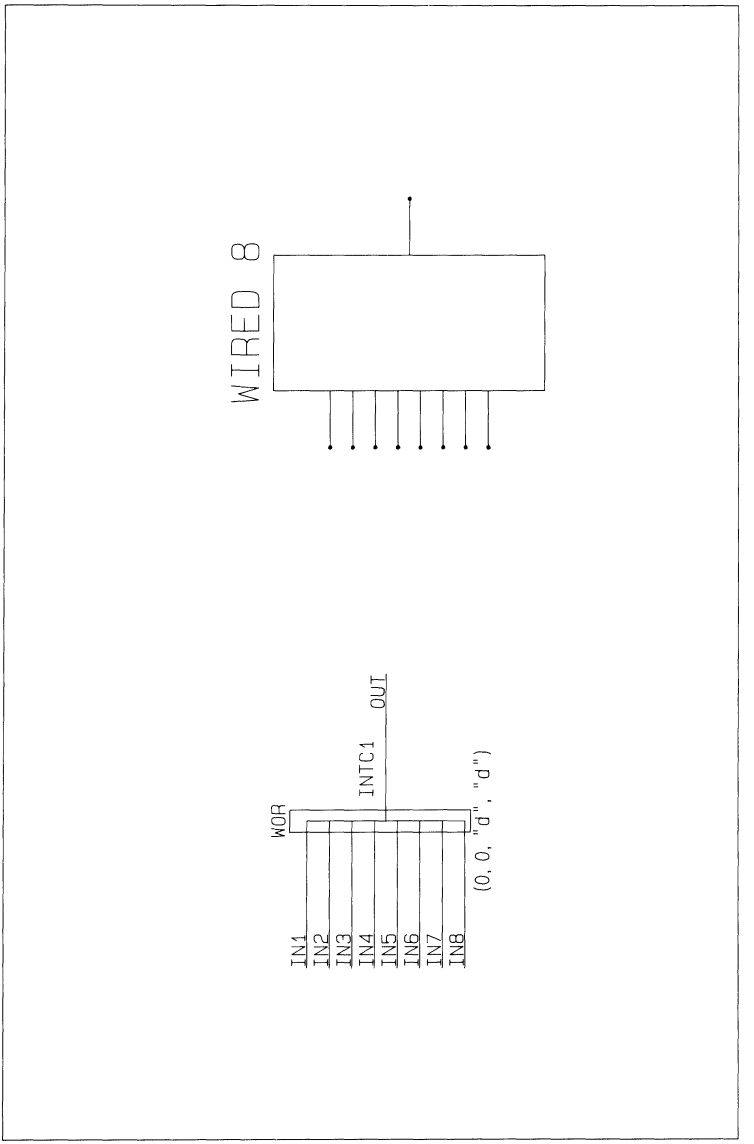
COMPONENT PLOTS

Plot 112



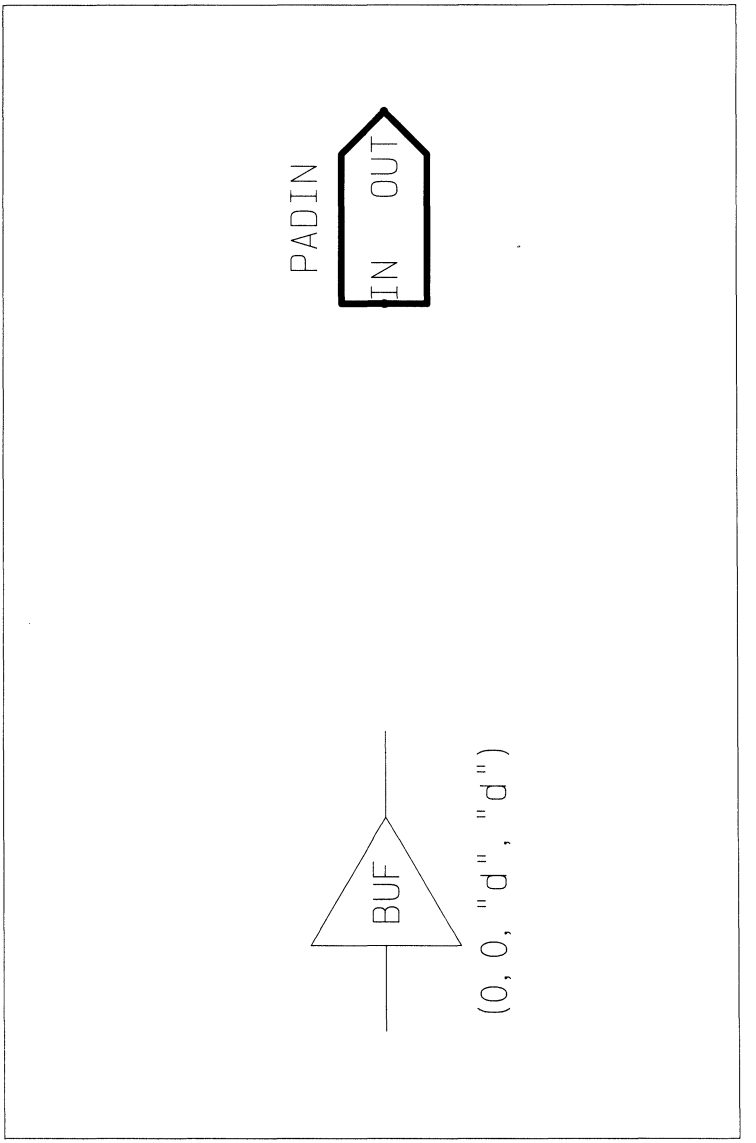
COMPONENT PLOTS

Plot 113



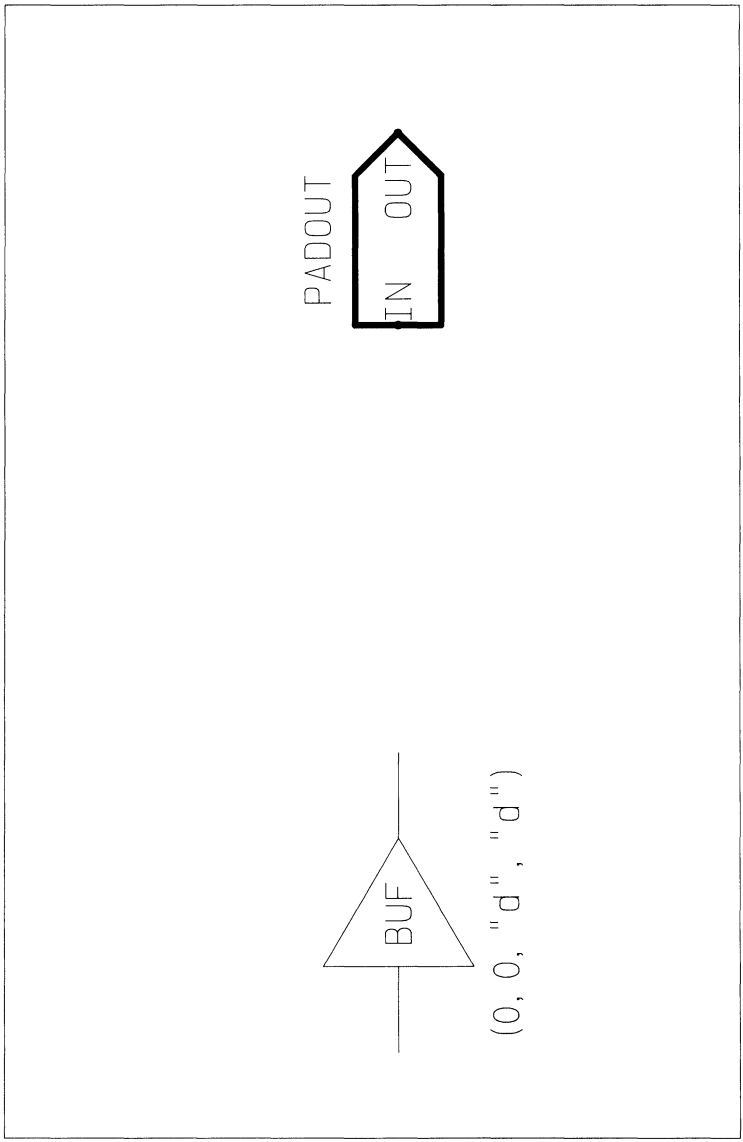
COMPONENT PLOTS

Plot 114



COMPONENT PLOTS

Plot 115



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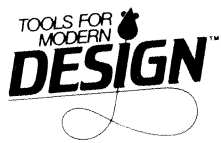
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