MOTOROLA®
MCA 600/1200 ECL
Semicustom IC Design Kit

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TRADEMARKS

ABOUT THIS MANUAL

This manual describes the Motorola® MCA600/1200 ECL Semicustom IC Design Kit, which consists of P-CAD's NX-M600 translator program and the Motorola MCA600/1200 ECL Macrocell Array Library.

The manual is divided into two sections: Section I describes the design kit and Section II describes the macrocell library.

Section I, DESIGN KIT USER'S MANUAL, contains the following:

Chapter 1, INTRODUCTION, provides an overview of the design kit and installation instructions.

Chapter 2, PREPARING THE INPUT FILES, gives instructions for creating the files to be input into the NX-M600 translator program.

Chapter 3, TRANSLATING THE NETLIST, gives instructions for using the NX-M600 program to translate netlists into LOGCAP™ files.

Chapter 4, VIEWING THE OUTPUT FILES, describes the NX-M600 output files.

Section II, MOTOROLA MCA600/1200 ECL COMPONENT LIBRARY, contains an overview and detailed descriptions of the macrocell components.

NOTATION

This manual gives step-by-step procedures and examples. To make it easy for you to follow these procedures, we use the following notation.

<xxxx> Angle brackets around lowercase letters indicate a variable name that may be entered by the system or by you. For example:

<filename>.SCH

[ ] Square brackets indicate the name of a key. For example:

[Return]

[Return] [Return] indicates the key that is used to execute a command or accept an option. This key may be labeled differently, depending on your system. For example:

[RETURN], [↵], [Enter], [Enter↵], [ENTER]

[ ]-[ ] Square brackets connected with a hyphen indicate keys that must be pressed simultaneously. For example:

Press [Ctrl]-[Alt]-[Del].

UPPER Uppercase letters indicate a command or an element that must be typed as shown. For example:

Type PCPLOTS and press [Return]

/ A forward slash separates main menu and submenu command combinations. For example:

DRAW/ARC

* An asterisk in a filename or in a filename extension indicates that any character(s) can occupy that position and all the remaining positions in the filename or extension. For example, the DOS command

DIR *.SYM

displays a list of all the filenames with the extension .SYM in the current directory.

TESTFILE TESTFILE is a sample filename, which you must replace with the filename you intend to use. For example:

Database Filename : TESTFILE.SCH
Netlist Filename : TESTFILE.NLT

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CHAPTER 1. INTRODUCTION

The Motorola MCA600/1200 ECL Semicustom IC Design Kit consists of this manual, and six diskettes containing the macrocell component library, the netlist files extracted by PC-NODES from each of the library components, and the NX-M600 translator program.

This manual serves as a guide to using the Motorola MCA600/1200 ECL Macrocell Array Library on the P-CAD design system. It assumes that you have the manuals for the P-CAD programs and are familiar with their use. If you are not yet familiar with the P-CAD system, we recommend that you complete the tutorials provided with the system before using the component library.

OVERVIEW

With this design kit, and PC-CAPS, PC-NODES and PC-LINK, you can create a schematic design using Motorola ECL macrocell components. This design can be prepared for either PC-LOGS or Motorola's CAD system.

There are five stages in this process:

1. Using PC-CAPS, prepare the schematic design. The design consists of one or more schematic files (<filename>.SCH), which are created by connecting symbols (<filename>.SYM) from the Motorola Macrocell Array Library.

2. Using PC-NODES, extract a netlist (<filename>.NLT) from each schematic file. The design kit already contains netlists extracted from each macrocell component. Netlist files contain component and interconnection information for each schematic file or macrocell file.

3. After you extract all the netlists, use PC-LINK to link all the netlists you intend to use into a single expanded netlist file (<filename>.XNL).

   You can use the expanded netlist as input into either PC-LOGS or the NX-M600 translator program. Use step 4 to use P-CAD's PC-LOGS program for local analysis, or step 5 to use the Motorola CAD system for mainframe analysis.

4. To use PC-LOGS, input the expanded netlist into PRESIM, which outputs the <filename>.NET file for input to PC-LOGS and simulation by PC-LOGS and the POSTSIM postprocessor. PRESIM, PC-LOGS, and POSTSIM are described in their corresponding manuals.

5. To translate the design for the Motorola CAD system, input the expanded netlist into the NX-M600 translator program. NX-M600 outputs two files:

   - The Motorola-compatible LOGCAP file (<filename>.LCP) can be input into the LOGCAP program and other analysis tools in Motorola's CAD system.

   - The cross-reference file (<filename>.XRF) lists component aliases assigned by PC-LINK and used in the LOGCAP file.

Figure 1-1 illustrates the process described above.

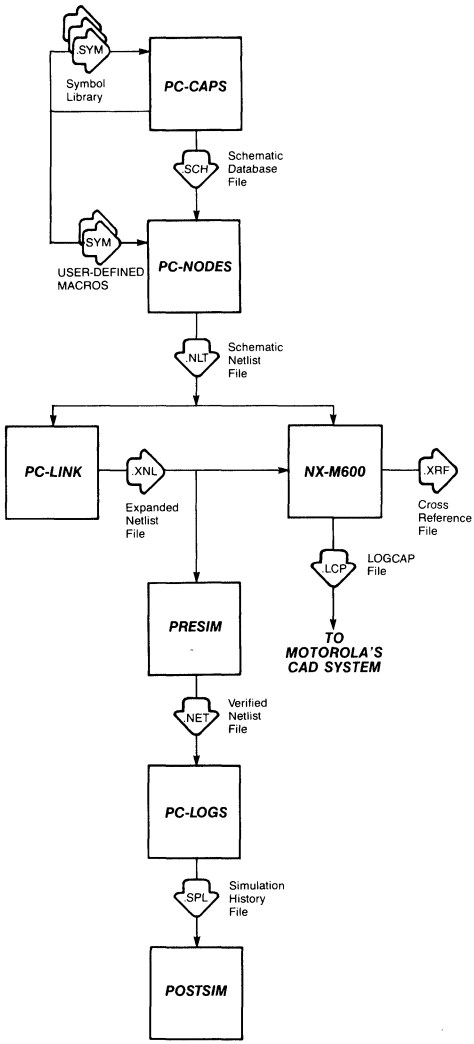


Figure 1-1. Design Kit Data Flow

SYSTEM REQUIREMENTS

Before you can install the design kit, your computer system must have the following minimum configuration:

- IBM PC, PC/XT, PC/AT, TI PC, Tandy 2000 or equivalent
- 640K of RAM
- P-CAD supported graphics board and monitor
- DOS 2.0 or higher operating system
- CONFIG.SYS in the root directory, containing a BUFFERS value of at least 12 and a FILES value of at least 15
- The PCADDRV.SYS file (created automatically when you use the P-CAD INSTALL program) in the root directory and the appropriate loadable device driver files in the appropriate directory

INSTALLATION

The design kit consists of six diskettes -- three diskettes containing the symbol library, two diskettes of netlist files, and the translator diskette.

To install the design kit on your hard disk, follow the procedures below. These procedures assume that you are using the P-CAD-recommended directory structure.

First, create three new directories for the symbols and netlists by typing

```
MD \PCAD\MOTOROLA [Return]
MD \PCAD\MOTOROLA\M600 [Return]
MD \PCAD\MOTOROLA\M600\NLT [Return]
```

To install the symbol library, first change directories by typing

```
CD \PCAD\MOTOROLA\M600 [Return]
```

Then in turn insert each of the three symbol diskettes into drive A. For each diskette, copy the files by typing

```
COPY A:*.* [Return]
```

Remove each diskette after copying the files.

To install the netlist files, change directories by typing

```
CD \PCAD\MOTOROLA\M600\NLT [Return]
```

Then insert the netlist diskette into drive A, and copy the files by typing

```
COPY A:*.* [Return]
```

Remove the diskette.

To install the translator, first change to the \PCAD\EXE directory by typing

```
CD \PCAD\EXE [Return]
```

Then insert the translator diskette into drive A and copy the file by typing

COPY A:NXM600.EXE [Return]

We suggest that you use the library and translator from a project directory created as a subdirectory of \PCAD\MOTOROLA.

CHAPTER 2. PREPARING THE INPUT FILES

Preparation of a design involves capturing the schematic using PC-CAPS, then generating, flattening, and linking netlists using PC-NODES and PC-LINK.

CREATING THE SCHEMATIC

Use PC-CAPS to prepare the schematics. Make all designs hierarchical. The topmost level should contain a symbol representing the functional design, and PADIN and PADOUT symbols to represent input and output pins. NX-M600 extracts LOGCAP files from this top level. Use netlists extracted from the lower levels for PC-LOGS.

Unconnected input pins are allowed in schematics for LOGCAP files, but are not allowed in PC-LOGS. If you plan to simulate a design using PC-LOGS, connect the unconnected input pins to global nets called "CON1" for a logic high or "CON0" for a logic low. The stimulus command file for PC-LOGS must have statements that force the net "CON1" to a strong high level and "CON0" to a strong low level.

Net names can be from one to eight alphanumeric characters. If you want to name a net as an active low signal, use an apostrophe as the last character of the net name. PC-CAPS will display the net name with a bar over the top.

If your design has more than one sheet, assign the SHEET attribute to each sheet. To assign this attribute,

use the PC-CAPS ATTR/ACOM command in SYMB mode and type

SHEET=<sheet id>

where

<sheet id> is two characters (generally digits) and is unique for each sheet in the design.

Input and Output Signals

Each circuit input requires a PADIN.SYM component. A net connected to the output pin of the PADIN.SYM component will be listed in the $INP statement of the LOGCAP output file. This signal can be viewed as the input signal to the circuit from an external source.

Each circuit output requires a PADOUT.SYM component. A net connected to the output pin of an output cell must be connected to the input pin of the PADOUT.SYM component. The actual output net is the net connected to the output pin of the PADOUT.SYM component. A net connected to the output pin of a PADOUT.SYM will be listed as an output signal on the $OUT statement of the LOGCAP output. This signal can be viewed as the output signal to the external environment.

Nets connected to the pins of the PADOUT symbols will also be listed as input and output signals in the $SUBU BOUT statement of the LOGCAP output.

Bidirectional Pads

Each bidirectional pad must be modeled by a two-input wired OR, an input pad, and an output pad. The

wired OR must be represented by a WOR2.SYM symbol. A $OR statement will appear in the LOGCAP output file for each WOR2.SYM component in the circuit.

Figure 2-1 illustrates the use of wired OR components for bidirectional pads.

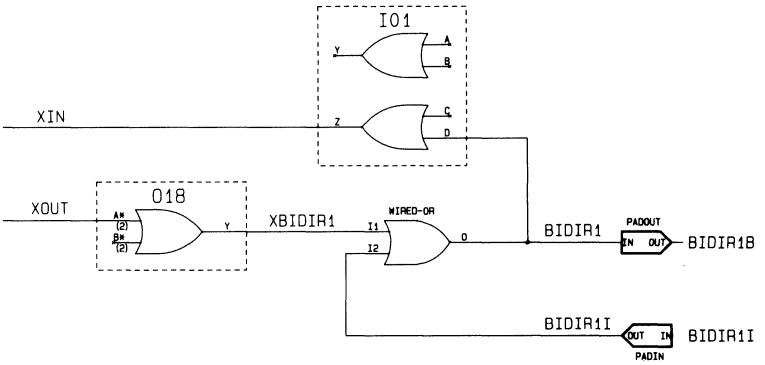


Figure 2-1. Bidirectional Pad

Wired OR

For each wired OR component used in the circuit, there must be one WOR.SYM with the appropriate number of inputs. The library provides WOR symbols for wired OR components with two to eight inputs. A $OR statement will appear in the LOGCAP output file for each WOR.SYM in the circuit.

EXTRACTING AND LINKING THE NETLISTS

Run PC-NODES to extract a netlist for each network and sheet of a schematic. Use the instructions in the *PC-NODES User's Manual.* PC-NODES assigns names to unnamed nets and component instances in the format UNsssnnn and UCsssnnn, respectively, where sss is the sheet ID assigned to the design using the SHEET attribute, and nnn is a number assigned sequentially starting with 000. If sheet IDs are not assigned or are not unique, the expanded netlist may contain several nets or components with the same name.

After you run PC-NODES, run PC-LINK to link together all the sheet and hierarchical component netlists to create an expanded netlist suitable for either NX-M600 or PC-LOGS. Use the instructions in the *PC-LINK User's Manual.*

PC-LINK prompts you for a library path. This entry specifies alternate directories where PC-LINK will look for hierarchical netlist files (all Motorola ECL symbols are hierarchical). If the hierarchical netlists reside in more than one directory, enter all the directories, separated by a plus sign. If you are extracting a netlist for NX-M600, do not specify the path pointing to the library netlist files since the expanded netlist would contain references to PC-LOGS primitives. When you run PC-LINK to extract a netlist for NX-M600, an error message will appear at the bottom of the screen. Review the PCLINK.MSG file; if all the errors indicate that the .NLT files for the Motorola ECL library components cannot be found, disregard the error messages and run NX-M600.

CHAPTER 3. TRANSLATING THE NETLIST

This chapter describes the required conditions and procedures for configuring and running NX-M600.

Before running NX-M600, be sure that:

- Your system is correctly configured.
- You have installed the NX-M600 program file (NXM600.EXE).
- You have assembled the schematic circuit.
- You have extracted and linked the netlist files.

To run NX-M600, be sure you are in the appropriate directory, and follow the steps below.

1. Type

   NXM600 [Return]

   The NX-M600 Title Screen appears. Press any key to continue. The system displays the NX-M600 Program Screen and prompts for the input netlist filename as shown in Figure 3-1.

NX-M600

Net-List Filename : <Filename>.XNL

Enter the filename; press [Return] or [Esc] to exit.

Figure 3-1. NX-M600 Program Screen

NOTE: At any prompt, if you decide not to continue with the program, press [Esc] to cancel and return to DOS.

2. Type the netlist filename and press [Return]. If you do not enter the filename extension, NX-M600 adds the .XNL extension.

   The system prompts for the output LOGCAP filename. The default is the input netlist filename with the .LCP extension.

3. Press [Return] to accept the default filename, or type another LOGCAP filename and press [Return].

The system prompts for the output cross-reference filename. The default is the input netlist filename with the .XRF extension as shown in Figure 3-2.

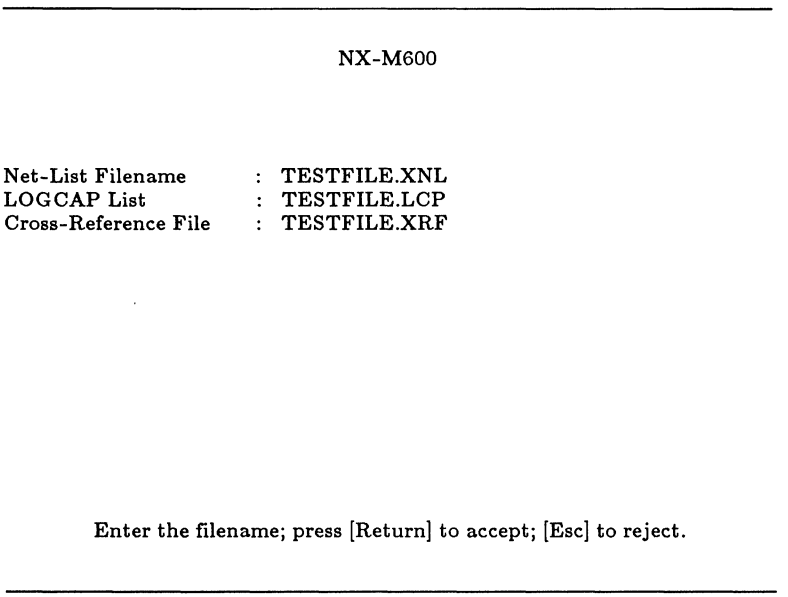


Figure 3-2. Sample Program Screen

4. Press [Return] to accept the default filename, or type another cross-reference filename and press [Return].

   NX-M600 sets up the netlist database environment and generates the LOGCAP netlist output. It displays progress reports and error messages on the lower section of the screen. When processing is complete, the system returns you to the Netlist prompt.

CHAPTER 4. VIEWING THE OUTPUT FILES

The MCA600 outputs two files, the LOGCAP netlist and the cross-reference files. The following sections describe these files.

THE LOGCAP NETLIST

The basic LOGCAP statements are $NETWORK for network identification, $INP and $OUT for circuit inputs and outputs, and $OR, $SUBU, and $SUBU BOUT for macrocells and interconnects.

The following sections discuss these statements. An example of a schematic and the corresponding LOGCAP netlist output file are shown in the Design Example section. Refer to the sample netlist for examples of the statements.

$NETWORK Statement

$NETWORK is the first line in the LOGCAP netlist output. It denotes the type of file used to generate the LOGCAP netlist.

$INP Statement

A single $INP statement directly follows the $NETWORK statement. NX-M600 uses the PADIN.SYM components for the inputs of the circuits being modeled. All nets connected to output pins of PADIN.SYM components are listed in the LOGCAP $INP statement as input signals. This signal can be viewed as the input signal to the circuit from an external source.

The format of the $INP statement is

$INP <net1> <net2> ... <netn>

where

netn is the name of a net connected to a PADIN.SYM output pin.

$OUT Statement

A single $OUT statement follows directly after the $INP statement. NX-M600 uses the PADOUT.SYM components for the outputs of the circuit being modeled. All nets connected to output pins of PADOUT.SYM components are listed in the $OUT statement as output signals. The LOGCAP output signal can be viewed as the output signal to the external environment.

The format of the $OUT statement is

$OUT <net1> <net2> ... <netn>

where

netn is the name of a net connected to a PADOUT.SYM output pin.

$OR Statement

The LOGCAP file contains a $OR statement for each WORx.SYM component (wired OR), where x is the number of nets wire ORed together. The $OR statement lists the names of the nets tied to the input and output pins of the WORx.SYM component and shows the

number of inputs. A WORx.SYM component has one output and from two to eight inputs.

The format of a $OR statement is

```
$OR 0 0
<outnet> x <innet1> <innet2> ... <innetx>
```

where

outnet is the name of the net connected to the WORx.SYM output pin.

x is the number of input pins.

innet1 through **innetx** are the names of the nets connected to the WORx.SYM input pins.

$SUBU Statement

The LOGCAP file contains one $SUBU statement for each component (cell) in the circuit. Each $SUBU statement gives the definition name of the component and the names of the nets tied to the component input and output pins.

The format of a $SUBU statement is

```
$SUBU <compname>
<outnet1> <outnet2> ... <outnetn> / &
<innet1> <innet2> ... <innetm>
```

where

compname is the name of the component.

outnetn is the name of a net connected to an output pin.

innet1 through **innetm** are the names of nets connected to input pins.

The nets tied to the output pins are listed first. A slash separates the outputs from the inputs. An ampersand indicates that the list is continued on the following line.

NX-M600 lists an unused output pin as "UN0", "UN1", etc. It lists an unused input pin as "CON0", with the following exceptions:

- The pin is called "CON1" if the component with the unused input pin has an attribute of FTYPE="INP".
- The pin is called "CON1" if the component has an attribute of FTYPE="OUT" and the unused pin is an enable pin named "E".

NX-M600 translates apostrophes, which PC-CAPS uses for netnames representing inverted signals, into the character "-". Apostrophes are invalid LOGCAP characters.

The following is an example of a $SUBU statement in a LOGCAP netlist:

```
$SUBU I01
HN000017 HN000016 / &
A20 CON0 A21 CON0
```

$SUBU BOUT Statement

The LOGCAP file contains a $SUBU BOUT statement for each output signal listed in the LOGCAP $OUT statement. A $SUBU BOUT statement models the input and output signals of the PADOUT.SYM components.

The format of the $SUBU BOUT statement is

$SUBU BOUT
<outname> / <inname>

where

outname is the name of the net attached to the output pin of the PADOUT.SYM component.

inname is the name of the net attached to the input pin of the PADOUT.SYM component.

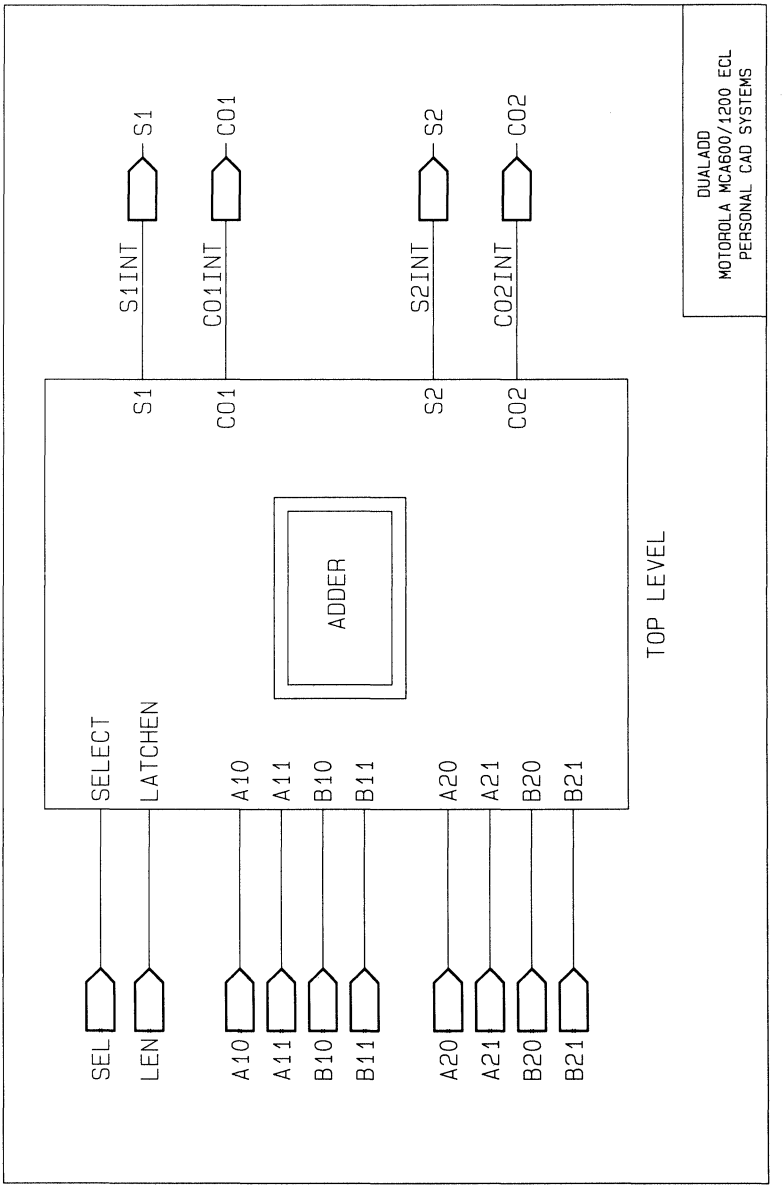
THE CROSS-REFERENCE FILE

The cross-reference file created by NX-M600 lists the names of all nets and components renamed by NX-M600, and their aliases. The aliases are used in the LOGCAP output file. NX-M600 resolves duplicate default net and component names by changing the names to the form HNsssnnn and HCsssnnn, respectively, where sss is the sheet ID assigned with the SHEET attribute, and nnn is a three-digit number.

DESIGN EXAMPLE

The following pages contain a design example showing a hierarchical design that was created using the ECL library, and the resulting LOGCAP and cross-reference files output by NX-M600.

Top Level Schematic of a DUALADD



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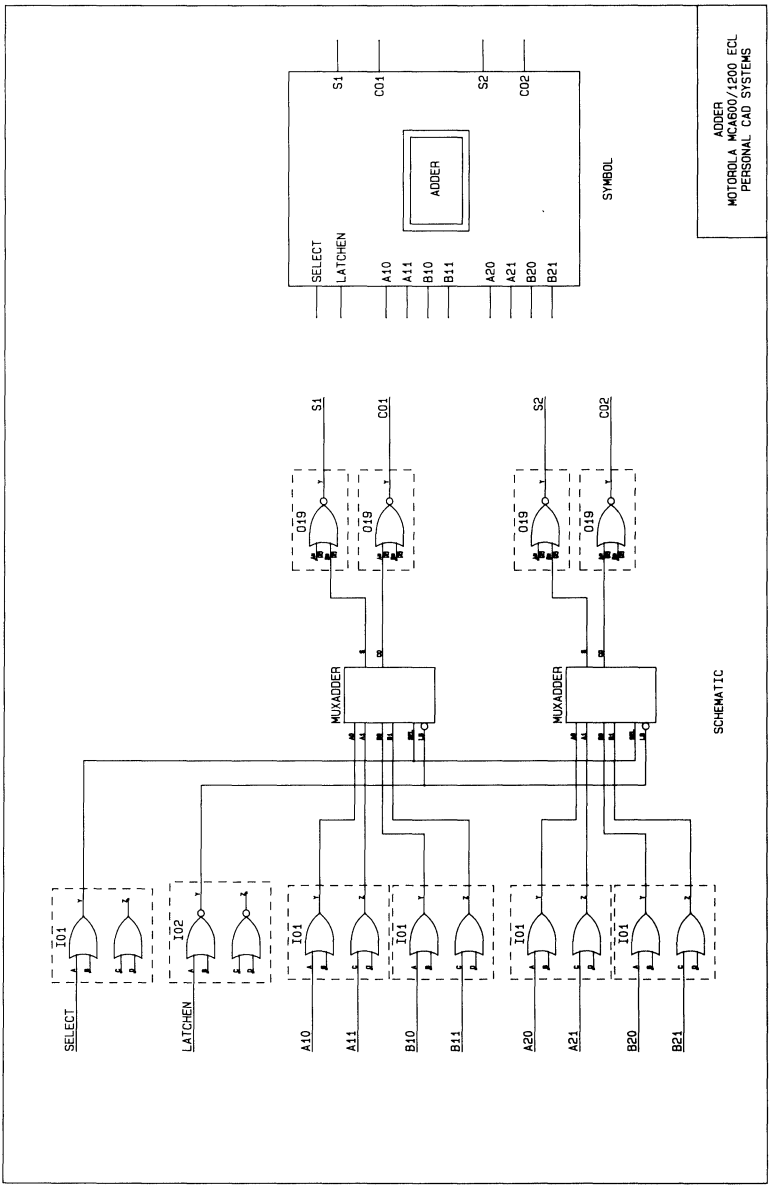
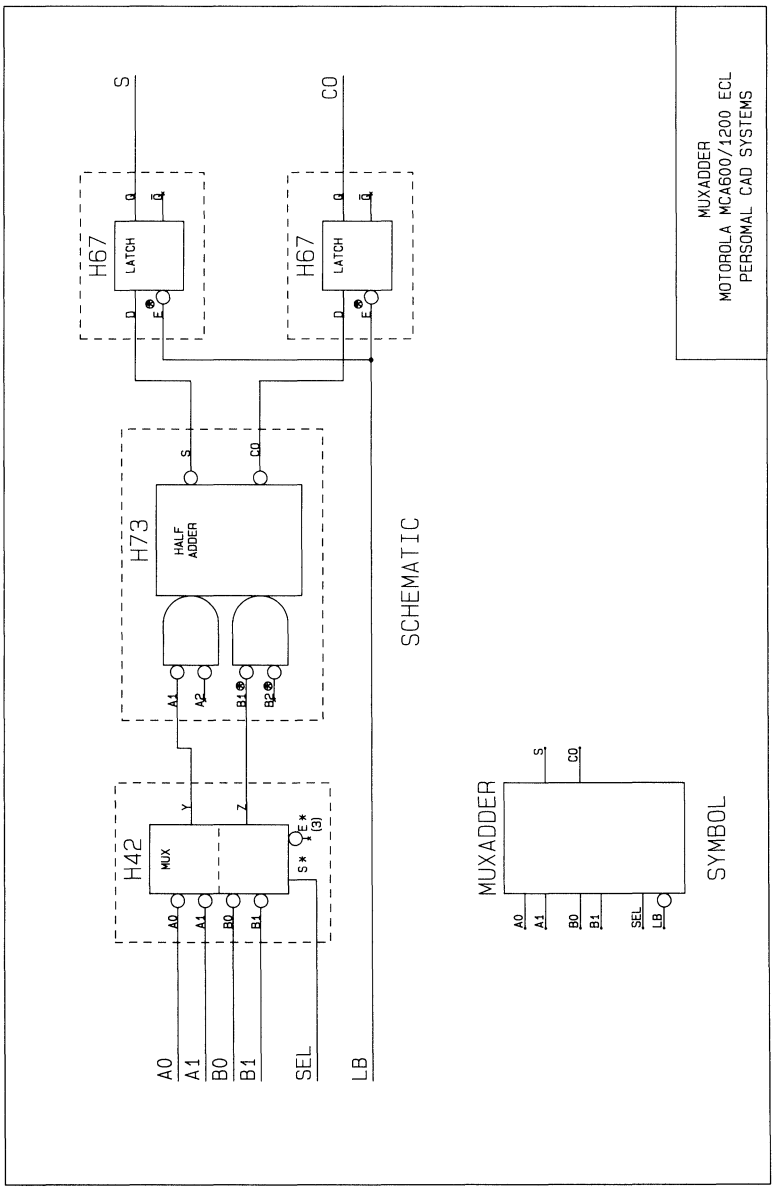
Schematic Representation of an ADDER



000-0145-00

Schematic Representation of a MUXADDER



000-0145-00

LOGCAP Netlist File

```
$$*************************************************************************
$$                                                                        *
$$     Copyright (C) 1983,1986 - Personal CAD Systems, Inc.               *
$$                                                                        *
$$     Program  :   NX-M600  VERSION 1.31                                 *
$$     Date     :   Aug 04 1986                                          *
$$     Time     :   03:15:05 PM                                          *
$$     File In  :   DUALADD.XNL                                          *
$$     File Out :   DUALADD.LCP                                          *
$$     Format   :   LOGCAP LIST                                          *
$$                                                                        *
$$*************************************************************************


$NETWORK
$INP SEL LEN A10 A11 B10 B11 A20 A21 B20 B21
$OUT S1 CO1 S2 CO2
$SUBU I02
UNO HN000000 / &
LEN CONO CONO CONO
$SUBU I01
HN000001 HN000002 / &
A10 CONO A11 CONO
$SUBU I01
HN000003 HN000004 / &
B10 CONO B11 CONO
$SUBU H42
HN000008 HN000009 / &
HN000002 HN000001 HN000004 HN000003 CONO HN000007
$SUBU H73
HN000010 HN000011 / &
HN000008 CONO HN000009 CONO
$SUBU H67
UN1 HN000005 / &
HN000011 HN000000
$SUBU H67
UN2 HN000006 / &
HN000010 HN000000
$SUBU I01
HN000012 HN000013 / &
B20 CONO B21 CONO
$SUBU I01
UN3 HN000007 / &
SEL CONO CONO CONO
$SUBU H42
HN000018 HN000019 / &
HN000016 HN000017 HN000013 HN000012 CONO HN000007
$SUBU H73
HN000020 HN000021 / &
HN000018 CONO HN000019 CONO
$SUBU H67
UN4 HN000014 / &
HN000021 HN000000
```

LOGCAP Netlist File (Continued)

```
$SUBU H67
UN5 HN000015 / &
HN000020 HN000000
$SUBU I01
HN000017 HN000016 / &
A20 CON0 A21 CON0
$SUBU O19
S1INT / &
CON0 HN000005
$SUBU O19
CO1INT / &
HN000006 CON0
$SUBU O19
S2INT / &
CON0 HN000014
$SUBU O19
CO2INT / &
HN000015 CON0
$SUBU BOUT
S1 / &
S1INT
$SUBU BOUT
CO1 / &
CO1INT
$SUBU BOUT
S2 / &
S2INT
$SUBU BOUT
CO2 / &
CO2INT
```

Cross-Reference File Created by NX-M600

```
*****************************************************************************
*                                                                           *
*                          ALIAS NAME CROSS-REFERENCE                       *
*                                                                           *
*  NX-M600 Version 1.31                                                     *
*  Copyright (C) 1986 - Personal CAD Systems, Inc.                          *
*                                                                           *
*                                                                           *
*****************************************************************************


Net List Filename : DUALADD.XNL

COMPONENT    SIGNAL     FULL PATH NAME

HC000000               = /UC000000/UC000000
          HN000000     = /UC000000/UN000008
HC000001               = /UC000000/UC000001
          HN000001     = /UC000000/UN000001
          HN000002     = /UC000000/UN000000
HC000002               = /UC000000/UC000002
          HN000003     = /UC000000/UN000003
          HN000004     = /UC000000/UN000002
HC000003               = /UC000000/UC000003
          HN000005     = /UC000000/UN000010
          HN000006     = /UC000000/UN000011
          HN000007     = /UC000000/UN000009
HC000004               = /UC000000/UC000003/UC000000
          HN000008     = /UC000000/UC000003/UN000000
          HN000009     = /UC000000/UC000003/UN000001
HC000005               = /UC000000/UC000003/UC000001
          HN000010     = /UC000000/UC000003/UN000003
          HN000011     = /UC000000/UC000003/UN000002
HC000006               = /UC000000/UC000003/UC000002
HC000007               = /UC000000/UC000003/UC000003
HC000008               = /UC000000/UC000004
          HN000012     = /UC000000/UN000007
          HN000013     = /UC000000/UN000006
HC000009               = /UC000000/UC000005
HC000010               = /UC000000/UC000006
          HN000014     = /UC000000/UN000013
          HN000015     = /UC000000/UN000012
          HN000016     = /UC000000/UN000004
          HN000017     = /UC000000/UN000005
HC000011               = /UC000000/UC000006/UC000000
          HN000018     = /UC000000/UC000006/UN000000
          HN000019     = /UC000000/UC000006/UN000001
HC000012               = /UC000000/UC000006/UC000001
          HN000020     = /UC000000/UC000006/UN000003
          HN000021     = /UC000000/UC000006/UN000002
HC000013               = /UC000000/UC000006/UC000002
HC000014               = /UC000000/UC000006/UC000003
HC000015               = /UC000000/UC000007
HC000016               = /UC000000/UC000008
HC000017               = /UC000000/UC000009
HC000018               = /UC000000/UC000010
HC000019               = /UC000000/UC000011
```

COMPONENT LIBRARY

OVERVIEW

The library diskettes contain the following files for use with the PC-CAPS schematic capture program:

- Component files
- Special symbol files
- Netlist files for each component
- Standard-size drawing sheet files

COMPONENT FILES

The Motorola MCA600/1200 ECL Macrocell Array Library contains all the components specified in the *Motorola MCA600ECL and MCA1200ECL MECL 10,000 Macrocell Arrays Design Manual.*

Three types of attributes have been assigned to the library symbols for use with the NX-M600 program. These attributes are described below.

The first attribute has the form FTYPE="INP" or FTYPE="OUT". It is used with certain input or output cells that have one or more unconnected input pins or an unconnected enable pin named "E". In the LOGCAP $SUBU statement describing the cell inputs and output, the unconnected pins are designated "CON0" or "CON1", as appropriate. Several examples are shown on the sample schematic and accompanying LOGCAP output.

The second attribute is used either with an alternate symbol for a macrocell, or for a symbol representing an alternate simulation model for an output cell. The form of the attribute is

ALT=<filename>

where

filename is the macrocell ID.

For example, the M50 macrocell has two library symbols, M50.SYM and M50A.SYM. The alternate symbol, M50A, has the attribute ALT="M50" and will be shown in the LOGCAP output as "M50".

Many of the output cells have different timing characteristics if the "Y" output of the cell is not used. If you are going to use only the "Y1" output of the cell, then you should use the version of the cell that has a filename ending in "Y1". For example, the output cell O01 has two representations, O01.SYM and O01Y1.SYM. You would normally use O01.SYM, but if you are not going to use the "Y" output, then you would use O01Y1.SYM. These cells also use the ALT attribute.

The third attribute defines the name of a binary file that describes the behavior of the component. This attribute is used for those components that require the use of a behavioral model. The form of the attribute is

MDL=(<filename>)

where

filename is the name of the behavioral model file.

SPECIAL SYMBOL FILES

In addition to the standard Motorola component symbols, the library includes special "noncomponent" symbols. Use these symbols with NX-M600 to translate your design information into a LOGCAP format that is compatible with Motorola CAD systems. Each special symbol in the circuit is described on a line of the LOGCAP output. The symbols are:

PADIN.SYM - Represents a circuit input.

PADOUT.SYM - Represents a circuit output.

WOR2.SYM through **WOR8.SYM** - Represent wired OR components with two to eight inputs.

NETLIST FILES

Each symbol in the component library is hierarchical, composed of a network of PC-LOGS primitives. Each ECL macrocell in the library has an associated netlist file that contains all the network information of the simulation model.

BEHAVIORAL MODEL FILES

To simulate properly, a few of the components require use of a behavioral model description. Files with the extension .MDL and .PML are the behavioral model files for these components. The files with the extension .PML are ASCII model description files. The files with the extension .MDL are binary model files compiled by PC-MODEL from the .PML files. Refer to the *PC-MODEL User's Manual* for more information on behavioral models.

DRAWING SHEET FILES

The library includes standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH, for circuit design. These files provide the normal layer structure plus a drawing sheet border.

LAYER STRUCTURE

The layer structure shown in Table 1 is the default layer structure used by PC-CAPS. This layer structure was used to create the Motorola ECL symbols in this library.

Table 1. Default Layer Structure

Layer	Name	Pen	Status	Use
1	WIRES	1	OFF	Interconnecting wires
2	BUS	1	OFF	Not used
3	GATE	2	ABL	Gate geometry/symbol
4	IEEE	2	OFF	Not used
5	PINFUN	3	OFF	Not used
6	PINNUM	1	OFF	Not used
7	PINNAM	6	ABLE	Pin names
8	PINCON	4	ABL	Pin connections (dot)
9	REFDES	2	OFF	Not used
10	ATTR	6	OFF	Visible attributes

Table 1 Continued

Layer	Name	Pen	Status	Use
11	SDOT	1	OFF	Not used
12	DEVICE	5	ABL	Macrocell ID
13	OUTLIN	5	ABL	Macrocell outline
14	ATTR2	6	OFF	Invisible attributes
15	NOTES	6	OFF	Not used
16	NETNAM	4	OFF	Net names
17	CMPNAM	5	OFF	Component instance names
18	BORDER	5	OFF	Drawing border

COMPONENT LIST BY SEQUENCE

The component filename consists of the macrocell number plus the extension .SYM; for example, H01.SYM. "Page" refers to the page number of the component plot in the last section of this manual. "Disk" refers to the disk on which the component is stored.

Component	Plot No.	Disk No.
H01	1	1
H02	2	1
H03	3	1
H04	4	1
H05	5	1
H06	6	1
H07	7	1
H08	8	1
H09	9	1
H10	10	1
H11	11	1
H12	12	1
H15	13	1
H16	14	1
H17	15	1
H18	16	1
H27	17	1
H31	18	1
H33	19	1
H34	20	1
H35	21	1
H40	22	2
H41	23	2
H42	24	2
H43	25	2
H52	26	2
H52A	27	2

Component	Plot No.	Disk No.
H54	28	2
H57	29	2
H58	30	2
H59	31	2
H60	32	2
H61	33	2
H62	34	2
H63	35	2
H64	36	2
H65	37	2
H66	38	2
H67	39	2
H69	40	2
H71	41	2
H72	42	2
H72A	43	2
H73	44	2
H75	45	2
H77	46	2
H78	47	3
H81	48	3
H82	49	3
H83	50	3
H84	51	3
I01	52	3
I02	53	3
I03	54	3
I04	55	3
I05	56	3
I06	57	3
I07	58	3
I08	59	3
I09	60	3
I10	61	3
I11	62	3

Component	Plot No.	Disk No.
I12	63	3
I13	64	3
I14	65	3
I15	66	3
I16	67	3
I20	68	3
M13	69	1
M14	70	1
M19	71	1
M20	72	1
M21	73	1
M22	74	1
M23	75	1
M24	76	1
M25	77	1
M26	78	1
M28	79	1
M29	80	1
M30	81	1
M32	82	1
M36	83	1
M37	84	1
M38	85	1
M39	86	2
M44	87	2
M45	88	2
M46	89	2
M47	90	2
M48	91	2
M49	92	2
M50	93	2
M50A	94	2
M51	95	2
M51A	96	2
M53	97	2

Component	Plot No.	Disk No.
M55	98	2
M56	99	2
M68	100	2
M74	101	2
M74A	102	2
M76	103	2
M79	104	3
M80	105	3
O01	106	3
O01Y1	107	3
O02	108	3
O02Y1	109	3
O03	110	3
O03Y1	111	3
O04	112	3
O04Y1	113	3
O05	114	3
O05Y1	115	3
O06	116	3
O06Y1	117	3
O07	118	3
O07Y1	119	3
O08	120	3
O08Y1	121	3
O09	122	3
O09Y1	123	3
O10	124	3
O10Y1	125	3
O11	126	3
O11Y1	127	3
O12	128	3
O12Y1	129	3
O13	130	3
O13Y1	131	3
O14	132	3

Component	Plot No.	Disk No.
O14Y1	133	3
O15	134	3
O15Y1	135	3
O16	136	3
O17	137	3
O18	138	3
O19	139	3
O20	140	4
O20Y1	141	4
O21	142	4
O21Y1	143	4
O24	144	4
O25	145	4
PADIN	153	4
PADOUT	154	4
WOR2	146	4
WOR3	147	4
WOR4	148	4
WOR5	149	4
WOR6	150	4
WOR7	151	4
WOR8	152	4

COMPONENT LIST BY FUNCTION

The component filename consists of the component number plus the extension .SYM; for example, H01.SYM.

Gates

H01	M24
H02	M25
H03	M26
H04	M27
H05	M28
H06	M29
H07	M30
H08	M55
H09	M56
H10	H57
H11	H58
H12	H59
M13	H60
M14	H61
H15	H62
H16	H63
H17	H64
H18	H65
M19	H66
M20	H71
M21	H75
M22	H76
M23	H77

Flip-Flops

H31	Dual D F/F
M32	D F/F with MUX
H78	Dual D F/F
H81	Dual D F/F with diff, clock and data
H82	Dual D F/F with set and reset

Latches

H33	Dual 2-bit latch
H34	Dual latch with MUX
H35	Quad latch
H67	Dual latch

Multiplexers

M36	4 to 1 MUX with enable
M37	4 to 1 MUX with enable
M38	4 to MUX with enable
M39	4 to 1, 2 to 1 MUX
H40	Quad 2 to 1 MUX, com sel
H41	Quad 2 to 1 MUX
H42	Quad 2 to 1 MUX with enable
H43	Dual 2 to 1 MUX
M68	4 to 1 MUX
H69	Dual 2 to 1 MUX
M80	4 to 1 MUX with enable

Decoders

M44	1/4 decoder (high)
M45	1/4 decoder (low)
M46	1/4 decoder (high)
M47	1/4 decoder (low)
M79	1/4 decoder (low)

Adders

M50	Dual adder
M50A	Dual adder
M51	Dual adder
M51A	Dual adder

Adders (Continued)

H52	Dual full adder
H52A	Dual full adder
M53	Dual adder and half adder
H54	Dual half adder
H72	Dual full adder
H73	Dual half adder
M74	Full adder

Miscellaneous Functions

M48	Priority encoder
M49	Priority expander
H83	High resolution diff comp
H84	High gain receiver

Interface Cells

I01
I02
I03
I04
I05
I06
I07
I08
I09
I10
I11
I12
I13
I14
I15
I16
I20

Output Cells

O01
O02
O03
O04
O05
O06
O07
O08
O09
O10
O11
O12
O13
O14
O15
O16
O17
O18
O19
O20
O21
O24
O25

Special Symbols

WOR2	2-input wired OR
WOR3	3-input wired OR
WOR4	4-input wired OR
WOR5	5-input wired OR
WOR6	6-input wired OR
WOR7	7-input wired OR
WOR8	8-input wired OR
PADIN	Input pad
PADOUT	Output pad

COMPONENT PIN SEQUENCES

The component filename consists of the macrocell number plus the extension .SYM; for example, H01.SYM.

H01:	Y'	Y	Z	Z'	A	B	C
	D	E	F	G			
H02:	Y	Y'	Z'	Z	A	B	C
	D	E	F	G			
H03:	Y	Y'	Z'	Z	A	B	C
	D	E	F	G			
H04:	Y'	Y	Z	Z'	B	C	A
	D	E					
H05:	Y	Y'	A	B	C	D	E
	F	G					
H06:	Y	Y'	A	B	C	D	E
	F						
H07:	Y	B	C	A	D	E	F
H08:	Y	B	C	A	D	E	F
H09:	Y'	Y	A	B	C	D	
H10:	Y	Y'	A	B	C		
H11:	Y	A	B	C	D		
H12:	Y	A	B	C	D		
M13:	Y	Y'	A	B	C	D	E
	F	G	H	I	J	K	L
M14:	Y'	Y	A	B	D	E	G
	H	J	K	C	F	I	L
H15:	Y	Y'	A	B	C	D	E
	F						
H16:	Y'	Y	A	B	C	D	E
	F						
H17:	Y	Y'	A	B	C	D	E
	F	G					

H18:	Y	A	B	C	D	E	
M19:	Y F	Z G	A H	B	C	D	E
M20:	Y F	Y' G	A H	B I	C J	D K	E L
M21:	Y F	Y' G	A H	B I	C J	D K	E L
M22:	Y F	Y' G	A H	B I	C J	D K	E L
M23:	Z D K	Y' E	Y F	Z' G	A H	B I	C J
M24:	Y F M	Y' G N	A H	B I	C J	D K	E L
M25:	Y F N	Y' G	A H	B I	C J	D L	E M
M26:	Y' F	Y G	A H	B I	C J	D K	E L
H27:	Y	Y'	A	B	C	D	E
M28:	Y' D K	Z' E L	Y F	Z G	A H	B I	C J
M29:	Y' L	Y F	A G	B H	C I	D J	E K
M30:	Z' D K	Y E	Z F	Y' G	A H	B I	C J
H31:	Q	Q'	C1	C2	D	R	
M32:	Q R	Q'	C1	C2	D0	D1	S
H33:	Q0' D1	Q0 R	Q1	Q1'	E1	E2	D0
H34:	Q	D0	D1	S	E1	E2	R

H35:	Q0' E1	Q0	Q1	Q1'	D0	D1	E0
M36:	Y E	A0	A1	A2	A3	S0	S1
M37:	Y E	A0	A1	A2	A3	S0	S1
M38:	Y E	A0	A1	A2	A3	S0	S1
M39:	Y B0	Z' B1	Z S	A0 S0	A1 S1	A2	A3
H40:	Y A1	Y' B0	Z' B1	Z	S1	S2	A0
H41:	Y B1	Y' SA	Z' SB	Z	A0	A1	B0
H42:	Y S	Z	A0	A1	B0	B1	E
H43:	Y'	Y	A0	B0	A1	B1	S
M44:	Y2	Y3	Y1	Y0	A0	A1	E
M45:	Y3	Y2	Y0	Y1	A0	A1	E
M46:	Y3	Y1	Y0	Y2	A0	A1	E
M47:	Y3	Y2	Y0	Y1	A0	A1	E
M48:	Y1	Y2	Y0	D0	D1	D2	D3
M49:	Y1 L2	Y2 H0	Y3 H1	Y0	H2	L0	L1
M50:	CO	S	B1	B2	A	CI	
M50A:	CO	S	B1	B2	A	CI	
M51:	S	CO	B1	B2	A	CI	
M51A:	S	CO	B1	B2	A	CI	
H52:	S	CO	B1	B2	A	CI	
H52A:	S	CO	B1	B2	A	CI	

M53:	P A1	H1 B1	H0 CI	CO	G	A0	B0
H54:	CO	S	A1	A2	B1	B2	
M55:	Y G	A S	B	C	D	E	F
M56:	Y G	A H	B I	C S	D	E	F
H57:	Y	A	B	C	D		
H58:	Y	A	B	C	D		
H59:	Y' D	Y E	Z F	Z' G	A H	B	C
H60:	Y D	Y' E	Z' F	Z G	A H	B	C
H61:	Y D	Y' E	Z' F	Z G	A H	B	C
H62:	Y' D	Y E	Z F	Z'	A	B	C
H63	Y'	Y	A	B	C	D	
H64:	Y	Y'	A	B	C	D	
H65:	Y	Y'	A	B	C	D	
H66:	Y'	Y	A	B	C		
H67:	Q'	Q	D	E			
M68:	Y	A0	A1	A2	A3	S0	S1
H69:	Y	Y'	A0	A1	SA		
H71:	Y	A	B	C	D		
H72:	S	CO	B1	B2	A	CI	
H72A:	S	CO	B1	B2	A	CI	
H73:	CO	S	A1	A2	B1	B2	
M74:	CO	S	B1	B2	A	CI	

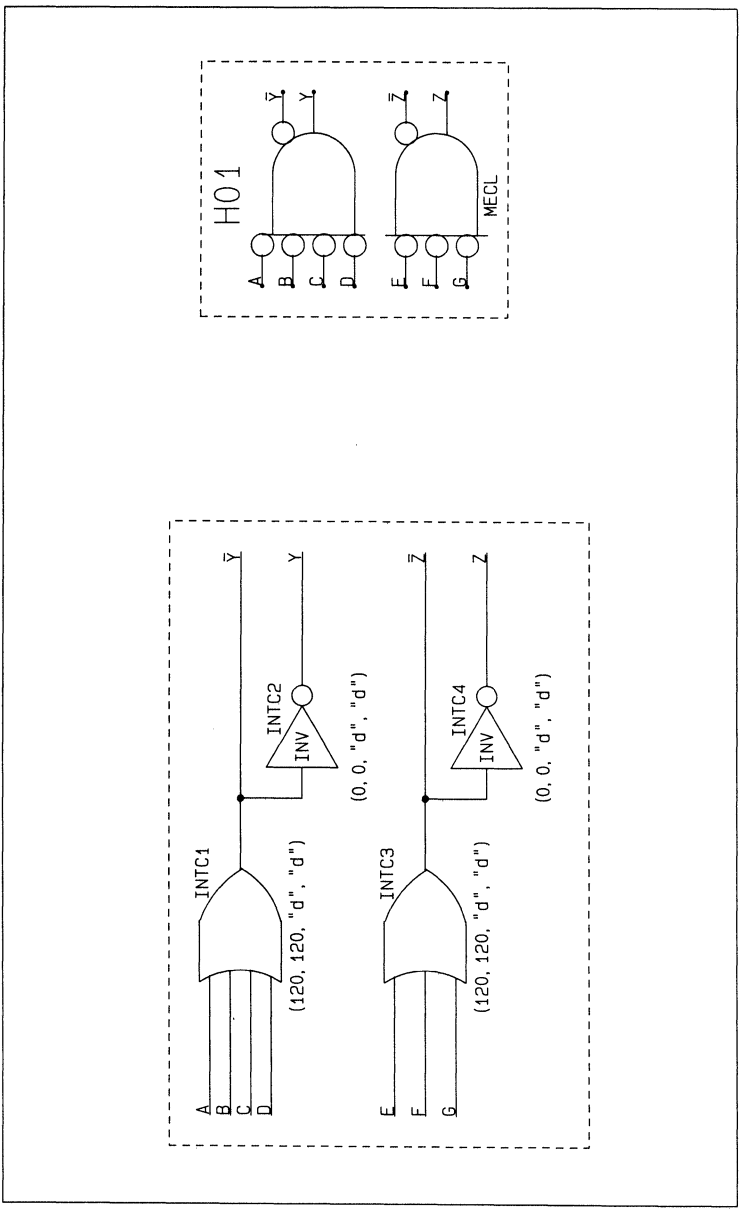
M74A:	CO	S	B1	B2	A	CI	
H75:	Y F	Y' G	A	B	C	D	E
M76:	Y F M	Y' G N	A H	B I	C J	D K	E L
H77:	Y	Y'	A	B	C	D	E
H78:	Q'	Q	C1	C2	D	R	
M79:	Y3	Y2	Y0	Y1	A0	A1	E
M80:	Y E	A0	A1	A2	A3	S0	S1
H81:	Q R2	Q'	C+	C-	D+	D-	R1
H82:	Q'	Q	C1	C2	D	R	S
H83:	Y'	Y	AP	AM			
H84:	Y	Y'	A				
I01:	Z	Y	A	B	C	D	
I02:	Z	Y	A	B	C	D	
I03:	Z	Y	A	B	C	D	
I04:	Z	Y	A	B	C	D	
I05:	Z	Y	A	B	C	D	
I06:	Y	Z	A	B	C		
I07:	Y	Z	A	B	C		
I08:	Y'	Y	A	B	C		
I09:	Y	Y'	B	C	A		
I10:	Y'	Y	B	C	A		
I11:	Y	Y'	B	C	A		
I12:	Y	Y'	S1	S2	A0	A1	

I13:	Q	Q'	E1	E2	D	
I14:	Q	Q'	E1	E2	D	
I15:	Y1	Y2	Y3	A	B	
I16:	Y	Y'	A	B	C	
I20:	Y	Z	AP	AM	BP	BM
O01:	Y1	Y	B	C	A	
O02:	Y1	Y	B	C	A	
O03:	Y1	Y	B	C	A	
O04:	Y1	Y	B	C	A	
O05:	Y1	Y	A	B	C	
O06:	Y1	Y	A	B	C	
O07:	Y1	Y	A	B	C	
O08:	Y1	Y	A	B	C	
O09:	Y1	Y	B	C	A	
O10:	Y1	Y	B	C	A	
O11:	Y1	Y	B	C	A	
O12:	Y1	Y	S	A0	A1	
O13:	Y1	Y	E	S	A0	A1
O14:	Y1	Y	E1	E2	D	
O15:	Y1	Y	E1	E2	D	
O16:	Y	Z	A	B	C	D
O17:	Y	Z	A	B	C	D
O18:	Y	A	B			
O19:	Y	A	B			
O20:	Y1	Y	A	B	C	D
O21:	Y1	Y	A	B	C	

O24:	Y	A	B				
O25:	Y	A	B				
WOR2:	O	I1	I2				
WOR3:	O	I1	I2	I3			
WOR4:	O	I1	I2	I3	I4		
WOR5:	O	I1	I2	I3	I4	I5	
WOR6:	O	I1	I2	I3	I4	I5	I6
WOR7:	O I7	I1	I2	I3	I4	I5	I6
WOR8:	O I7	I1 I8	I2	I3	I4	I5	I6
PADIN:	OUT	IN					
PADOUT:	OUT	IN					

COMPONENT PLOTS

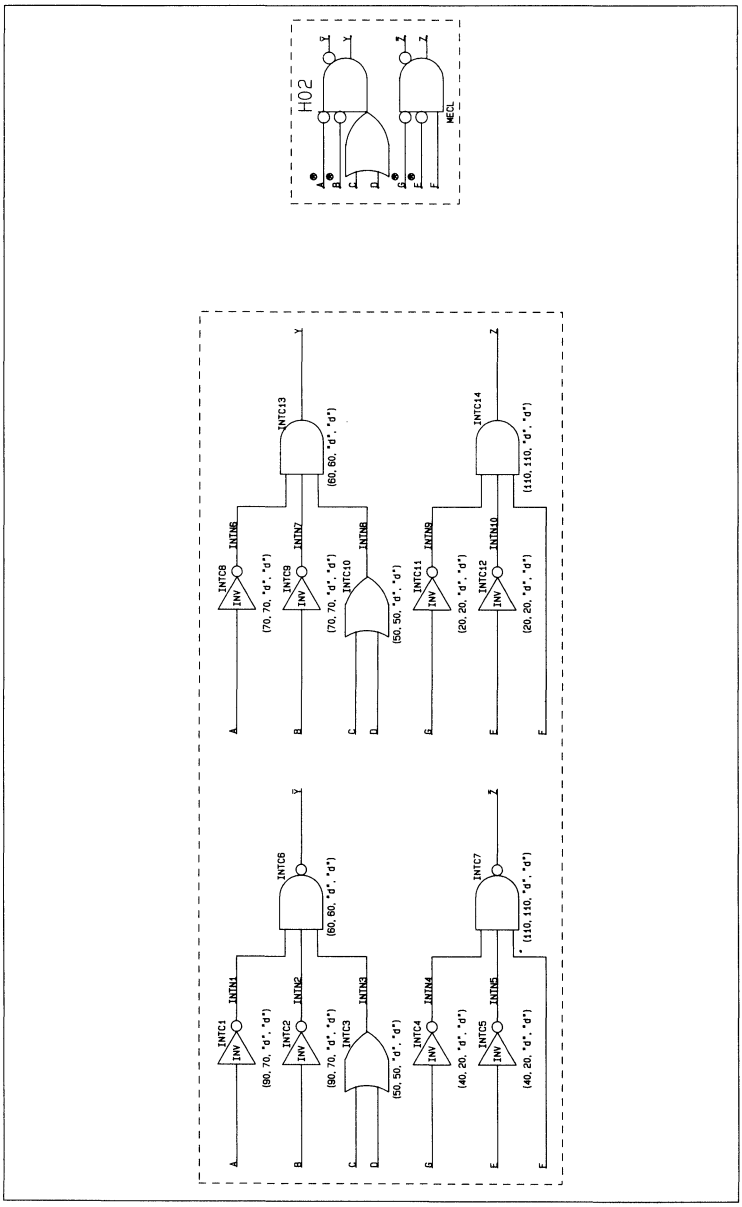
Plot 1



000-0145-00

COMPONENT PLOTS

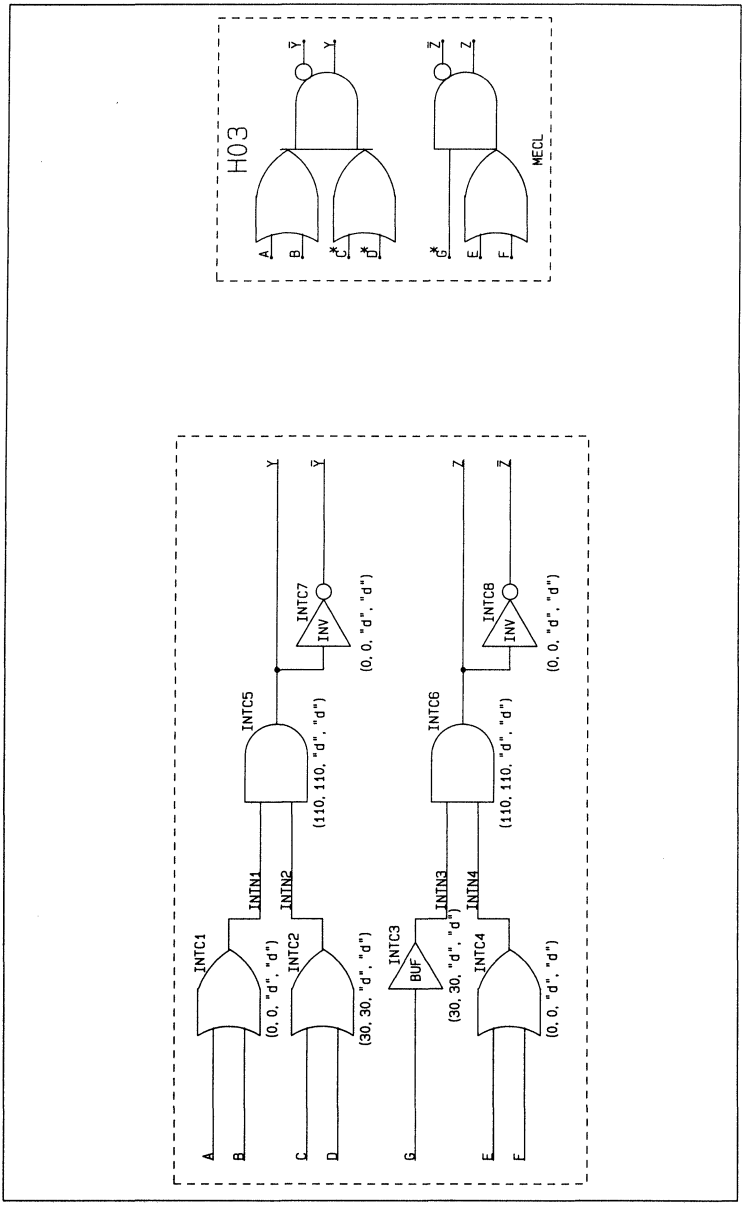
Plot 2



000-0145-00

COMPONENT PLOTS

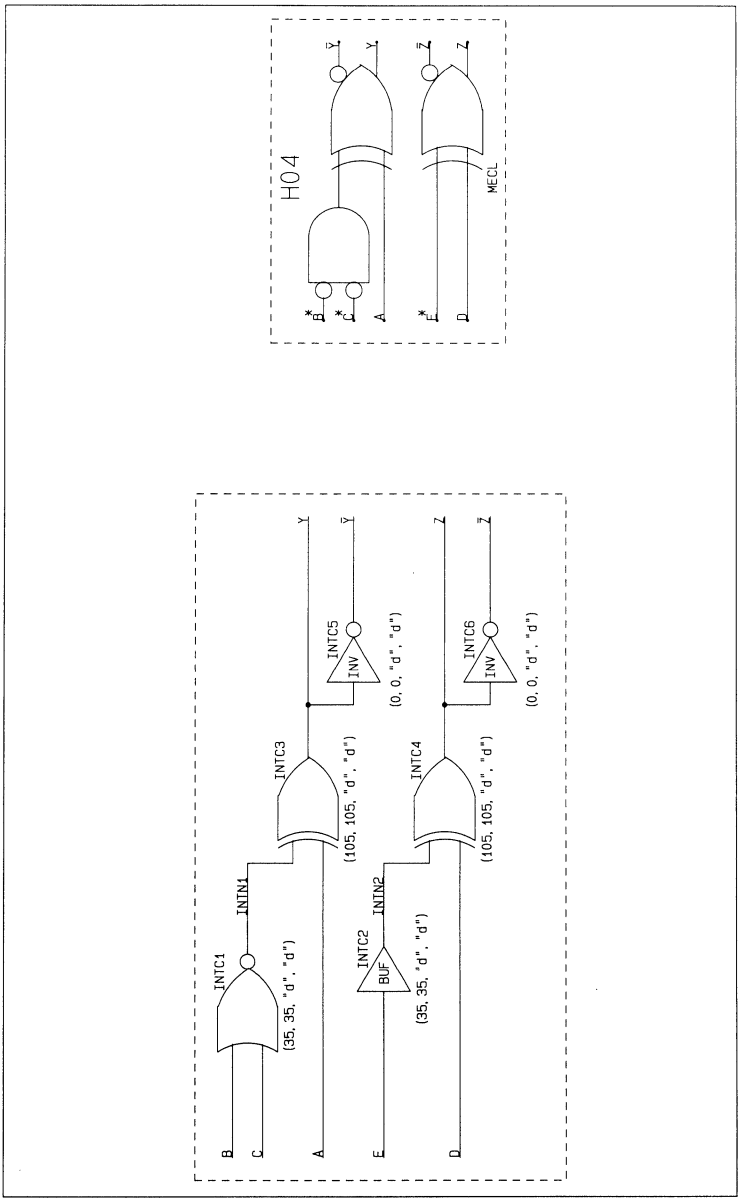
Plot 3



000-0145-00

COMPONENT PLOTS

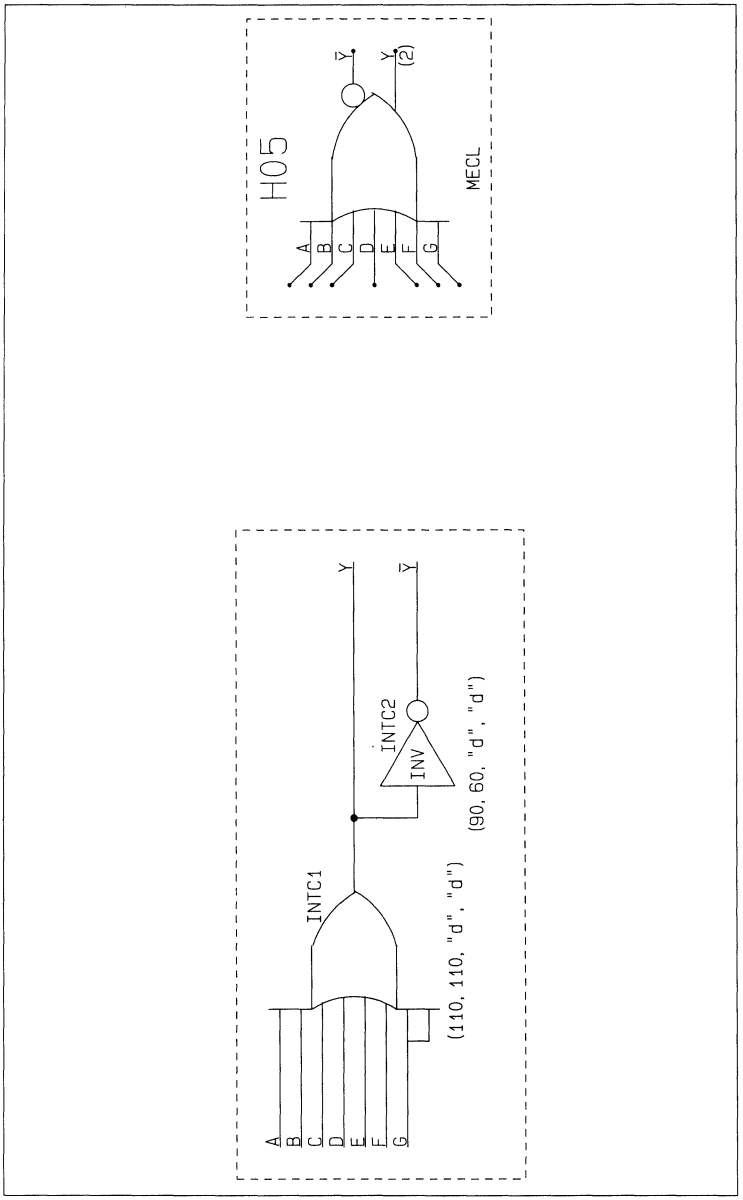
Plot 4



000-0145-00

COMPONENT PLOTS

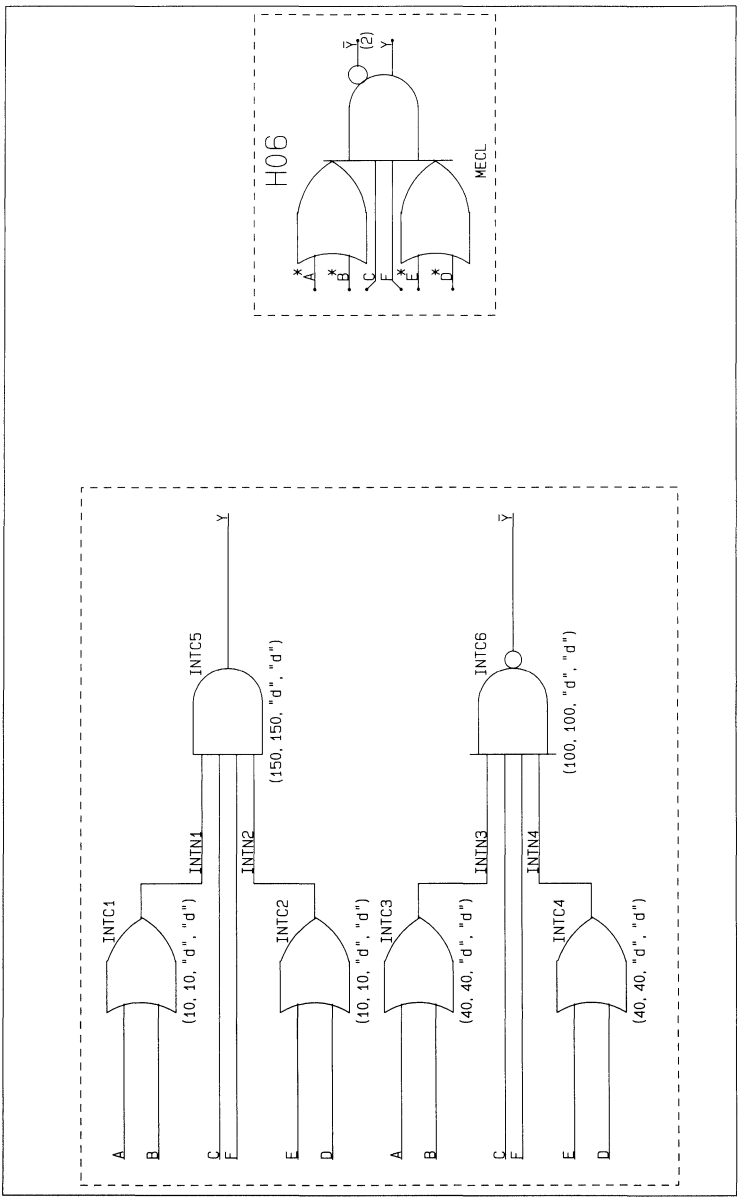
Plot 5



000-0145-00

COMPONENT PLOTS

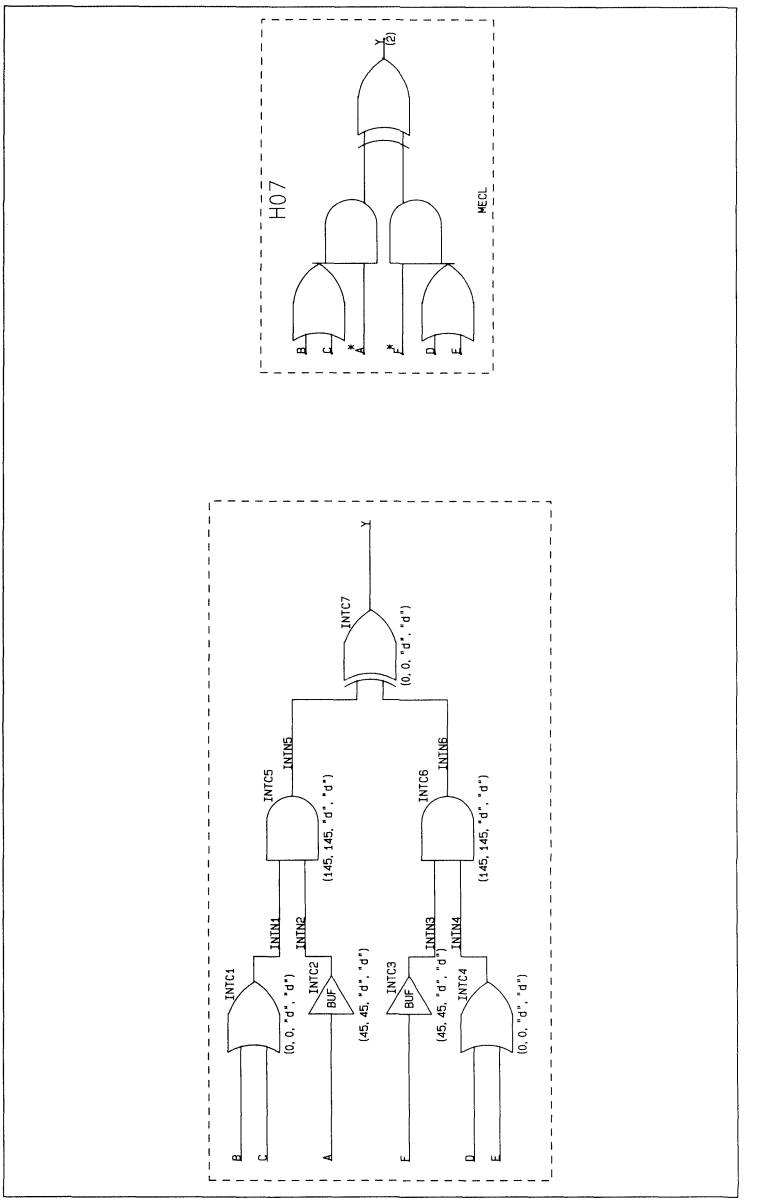
Plot 6



000-0145-00

COMPONENT PLOTS

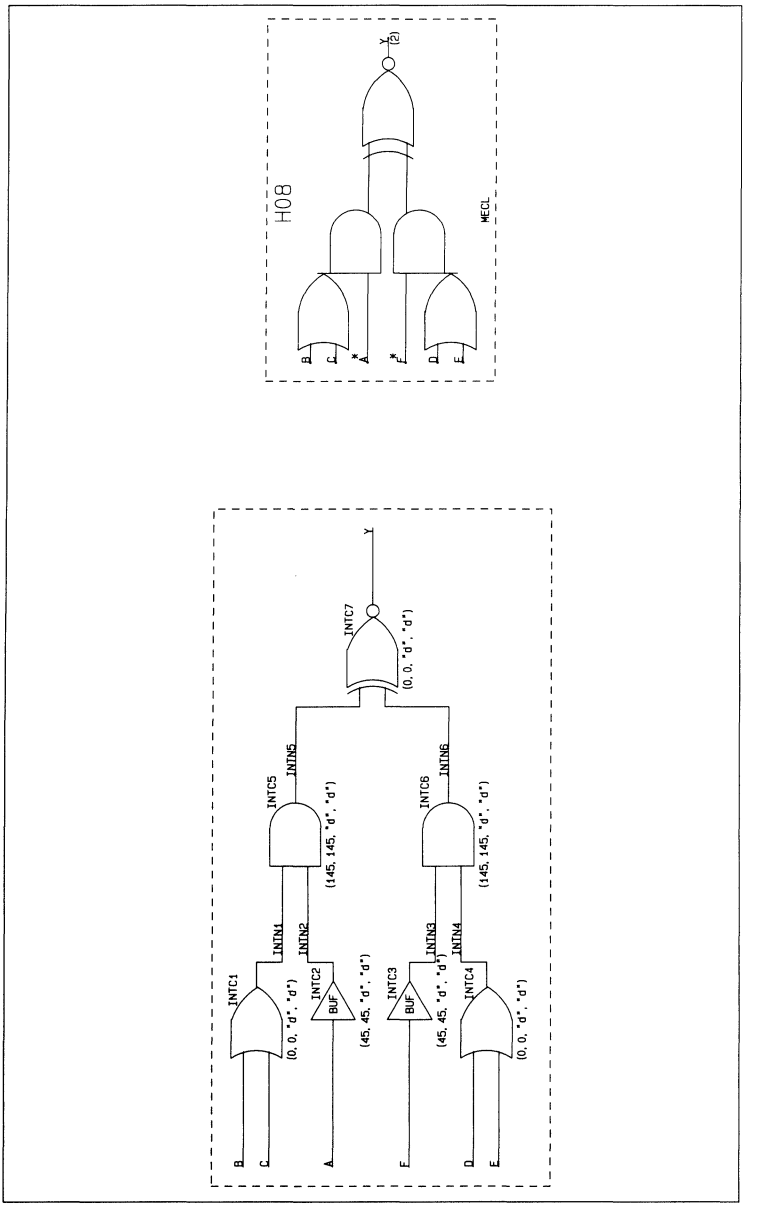
Plot 7



000-0145-00

COMPONENT PLOTS

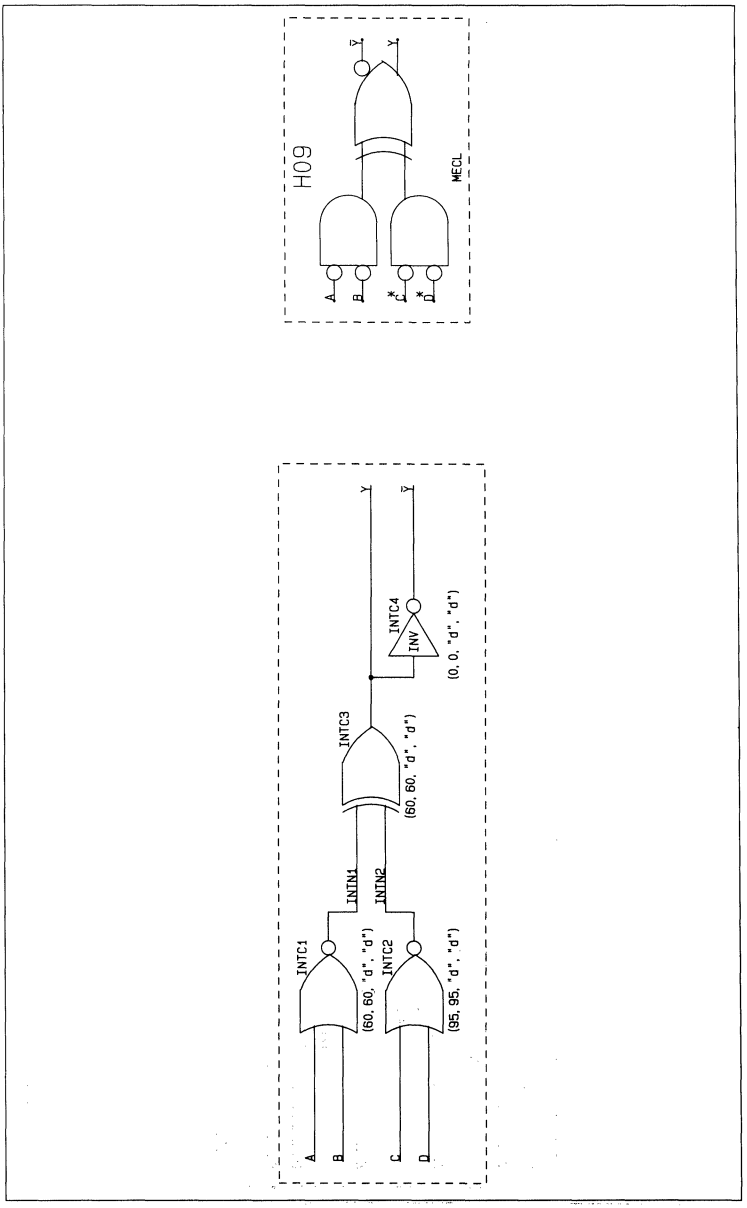
Plot 8



000-0145-00

COMPONENT PLOTS

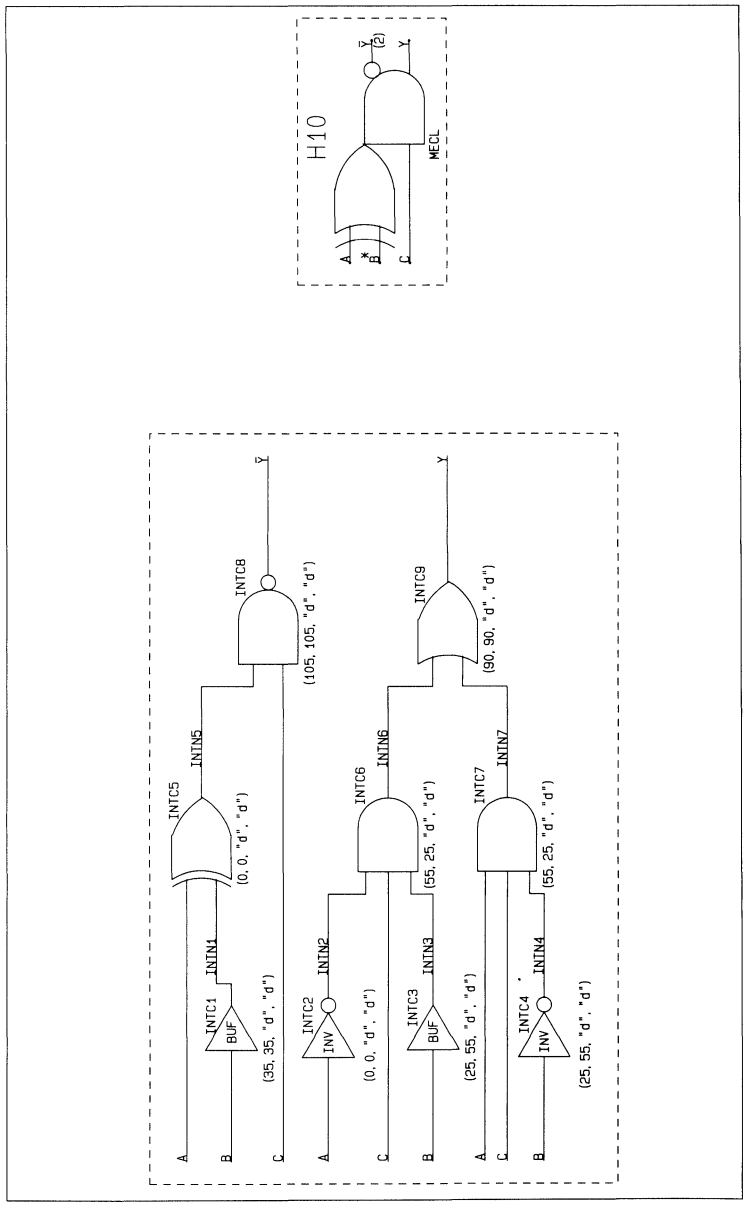
Plot 9



000-0145-00

COMPONENT PLOTS

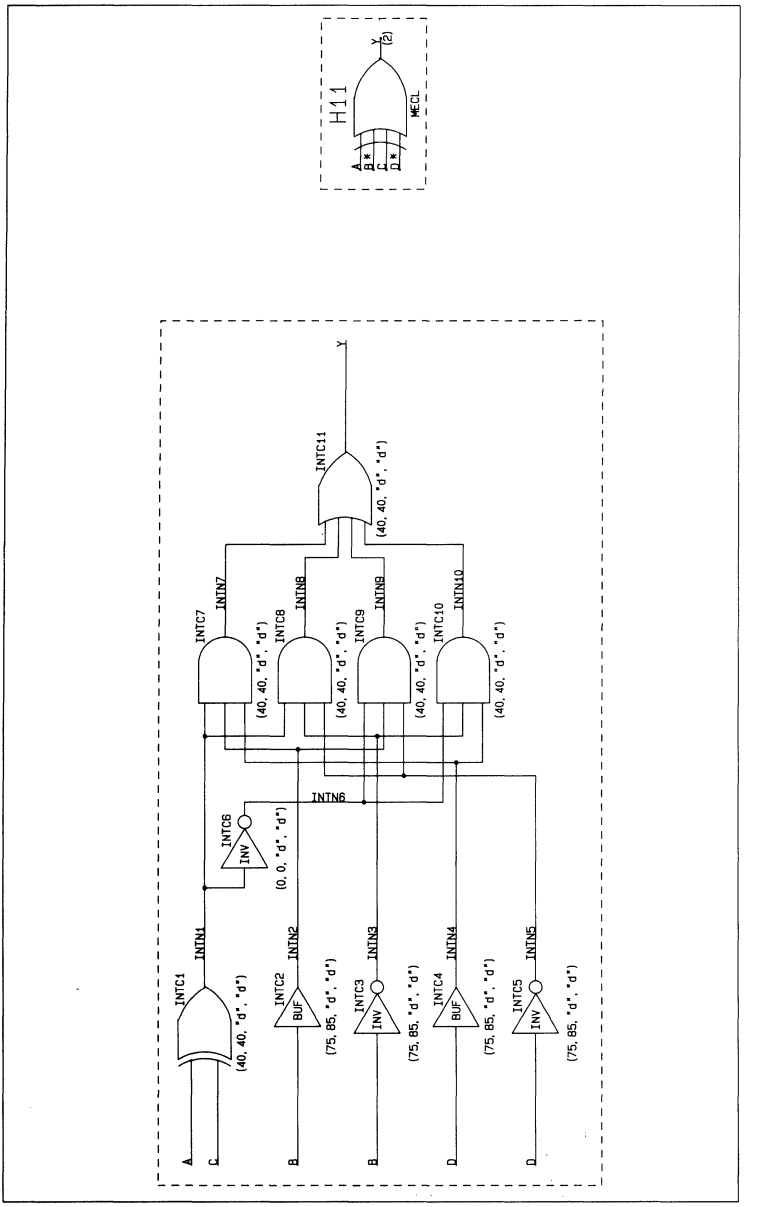
Plot 10



000-0145-00

COMPONENT PLOTS

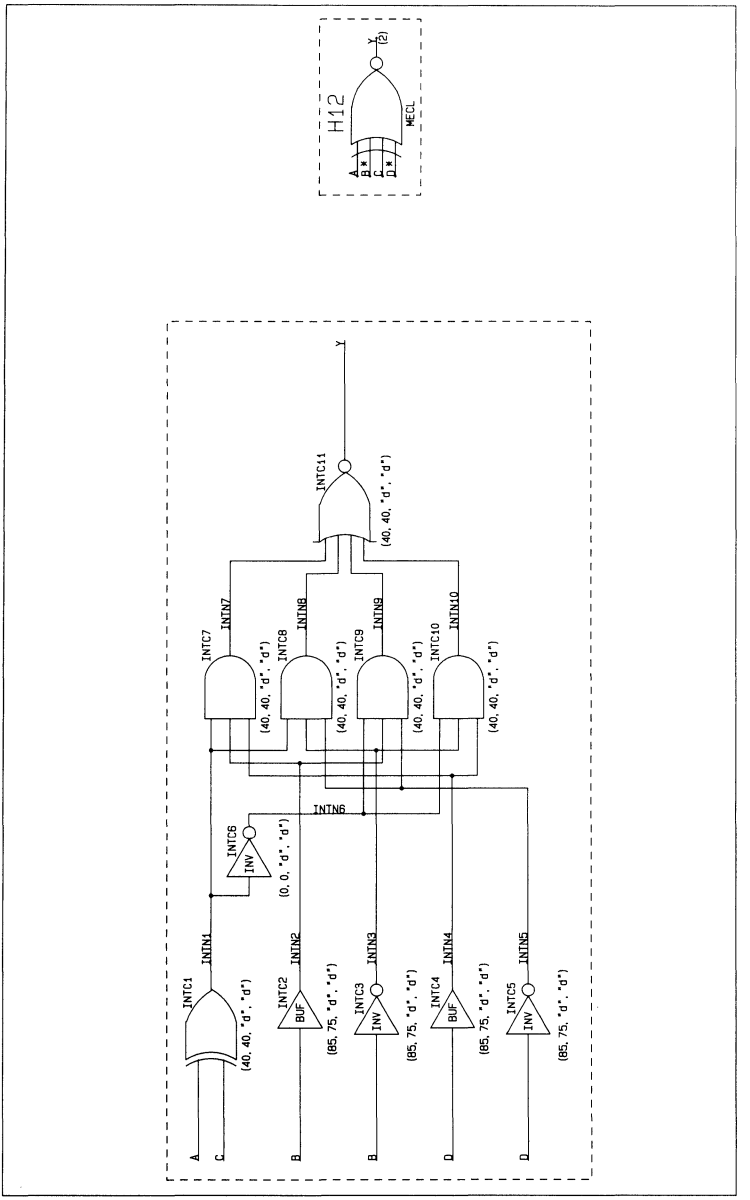
Plot 11



000-0145-00

COMPONENT PLOTS

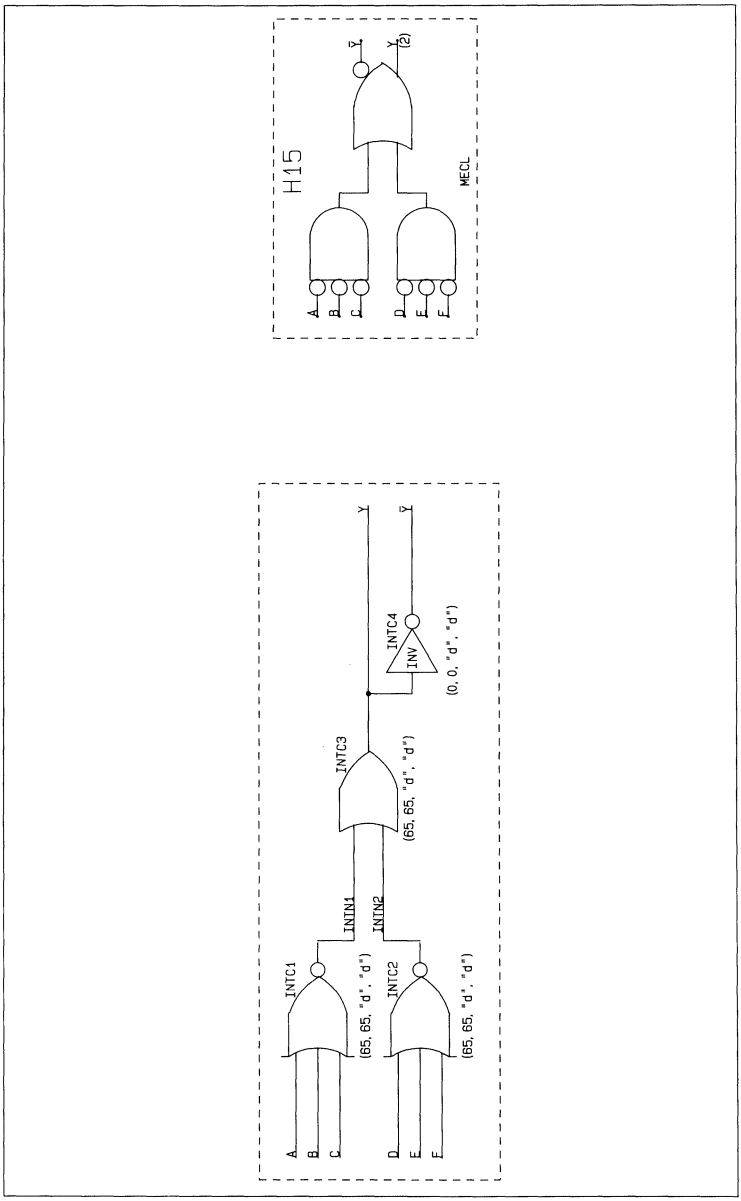
Plot 12



000-0145-00

COMPONENT PLOTS

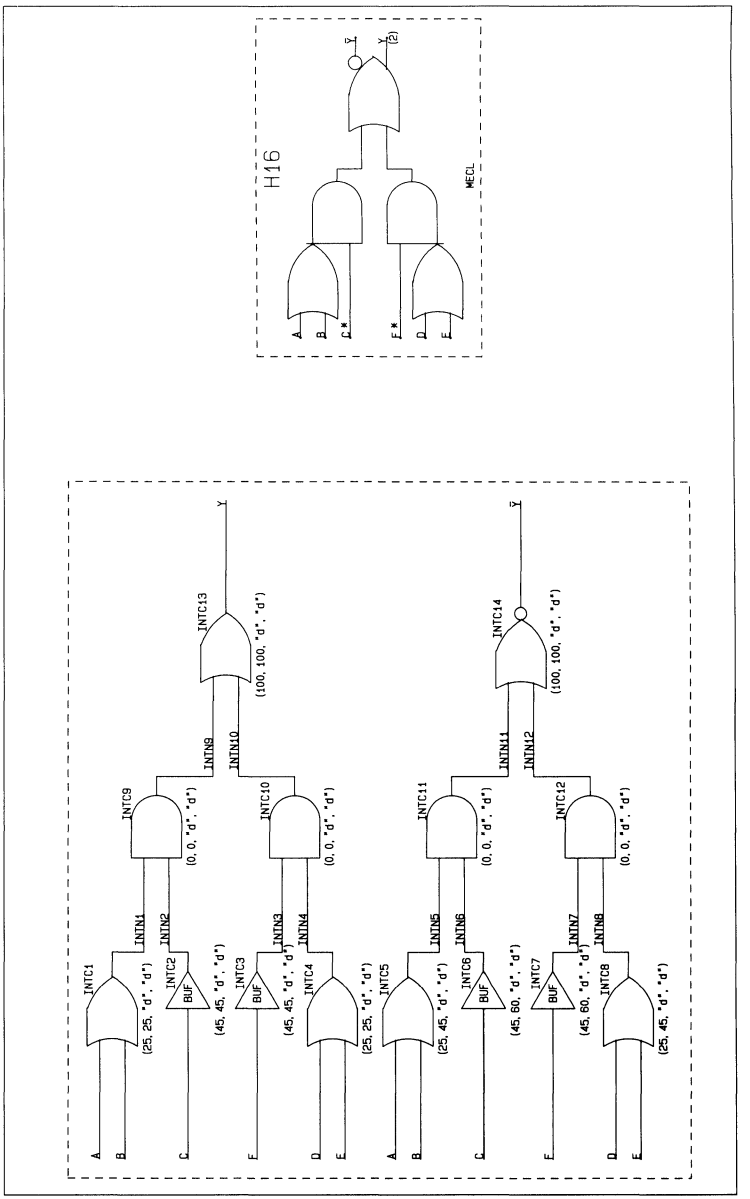
Plot 13



000-0145-00

COMPONENT PLOTS

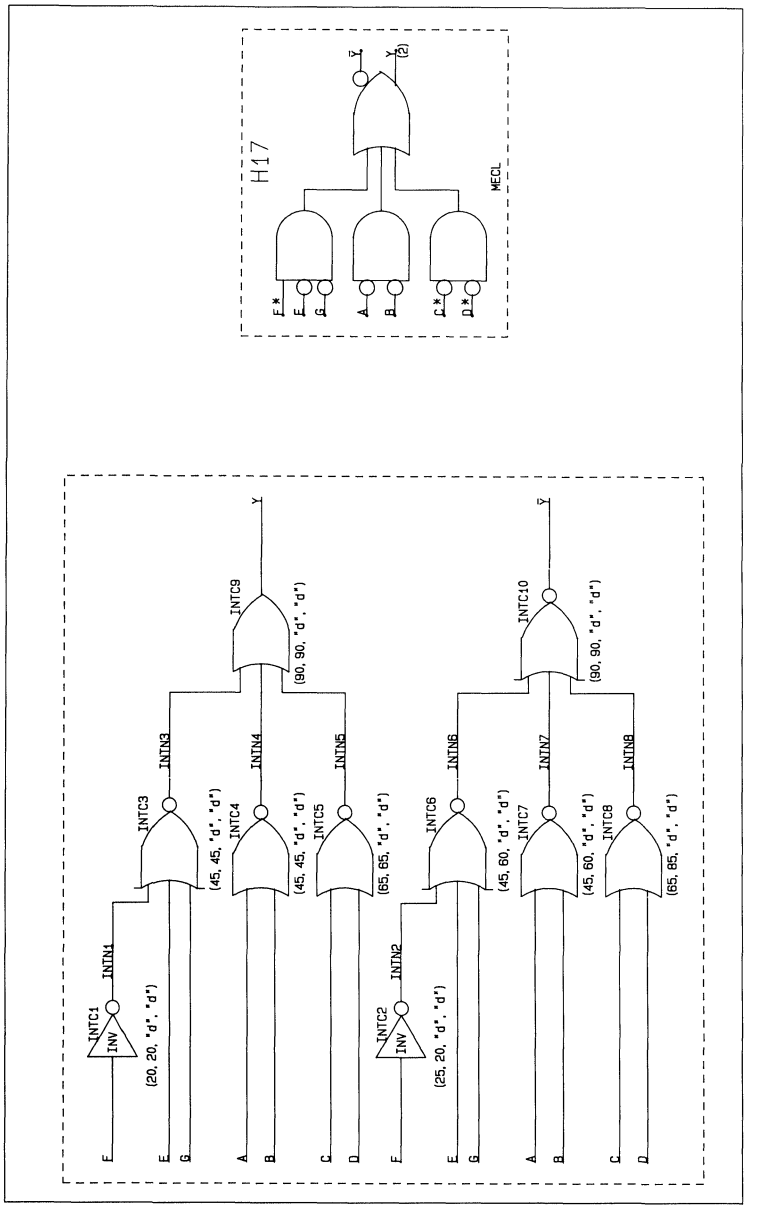
Plot 14



000-0145-00

COMPONENT PLOTS

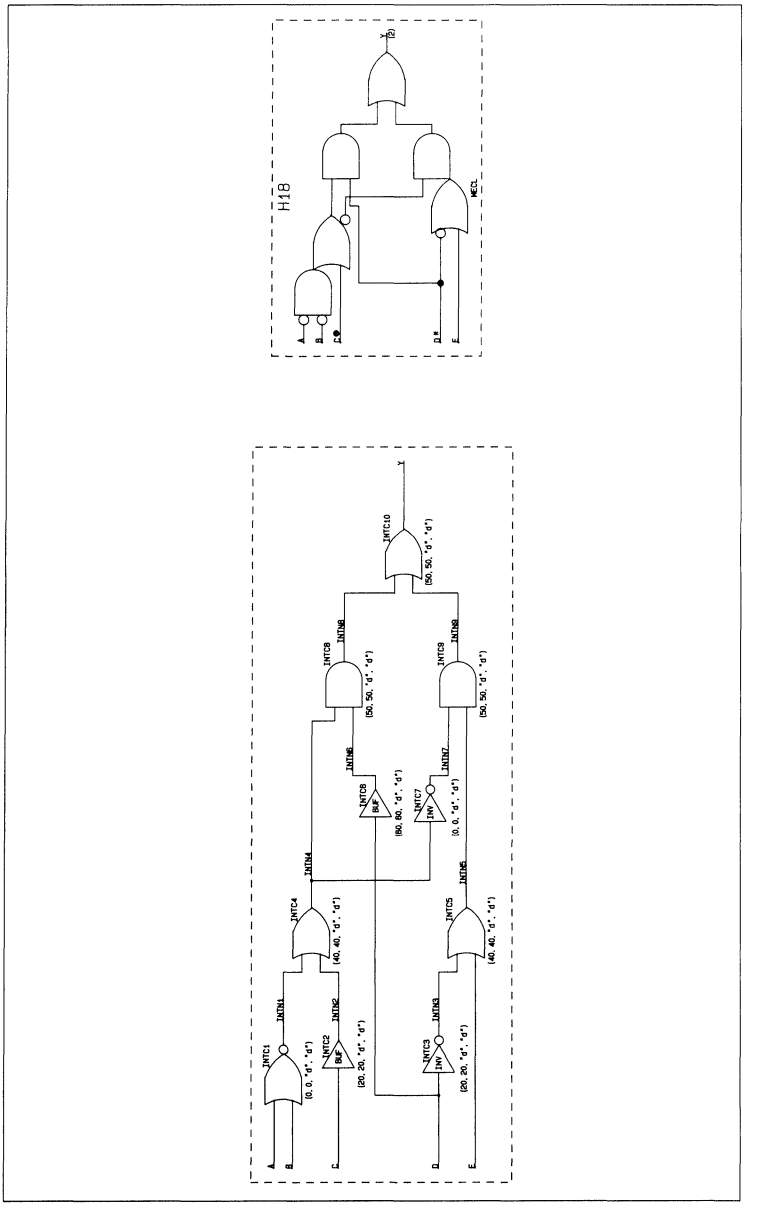
Plot 15



000-0145-00

COMPONENT PLOTS

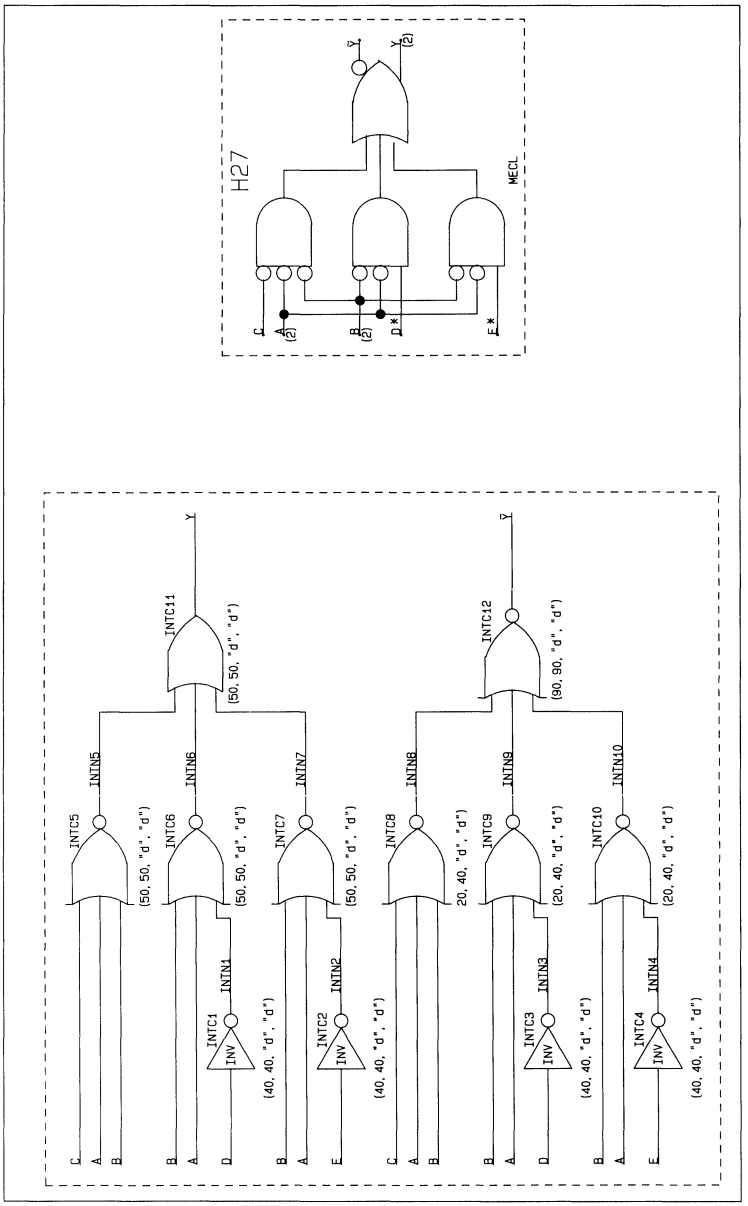
Plot 16



000-0145-00

COMPONENT PLOTS

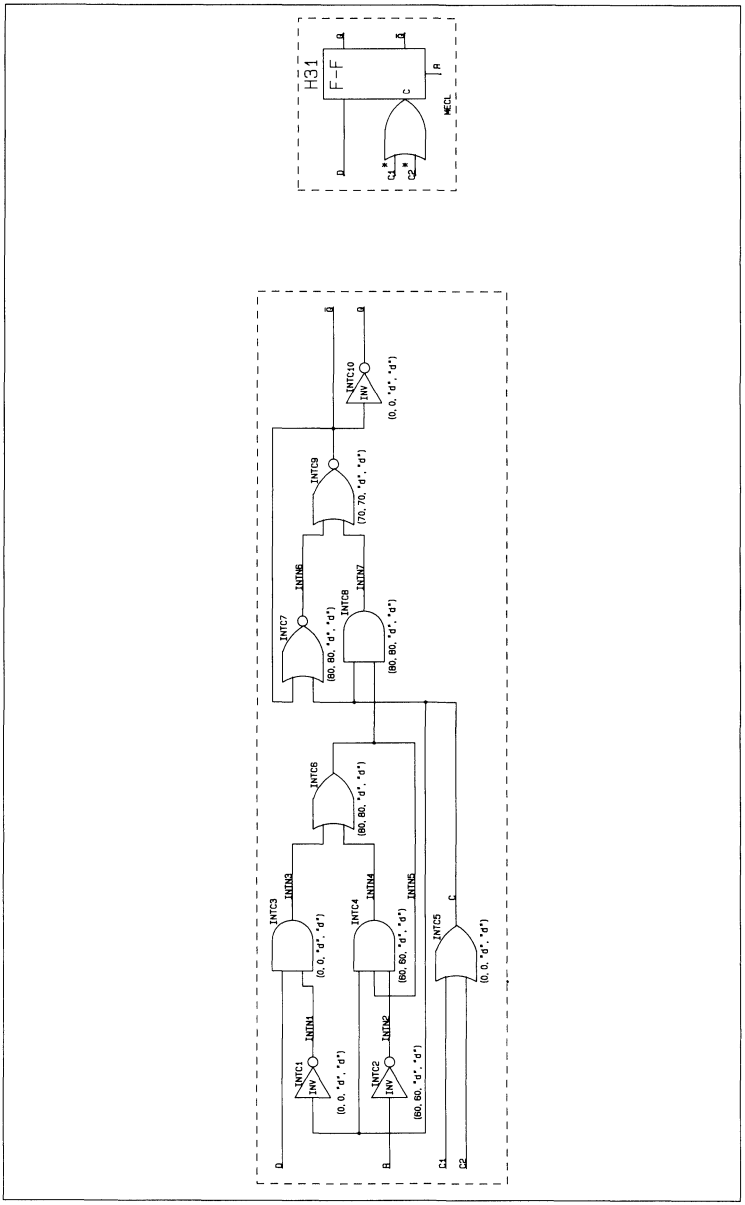
Plot 17



000-0145-00

COMPONENT PLOTS

Plot 18



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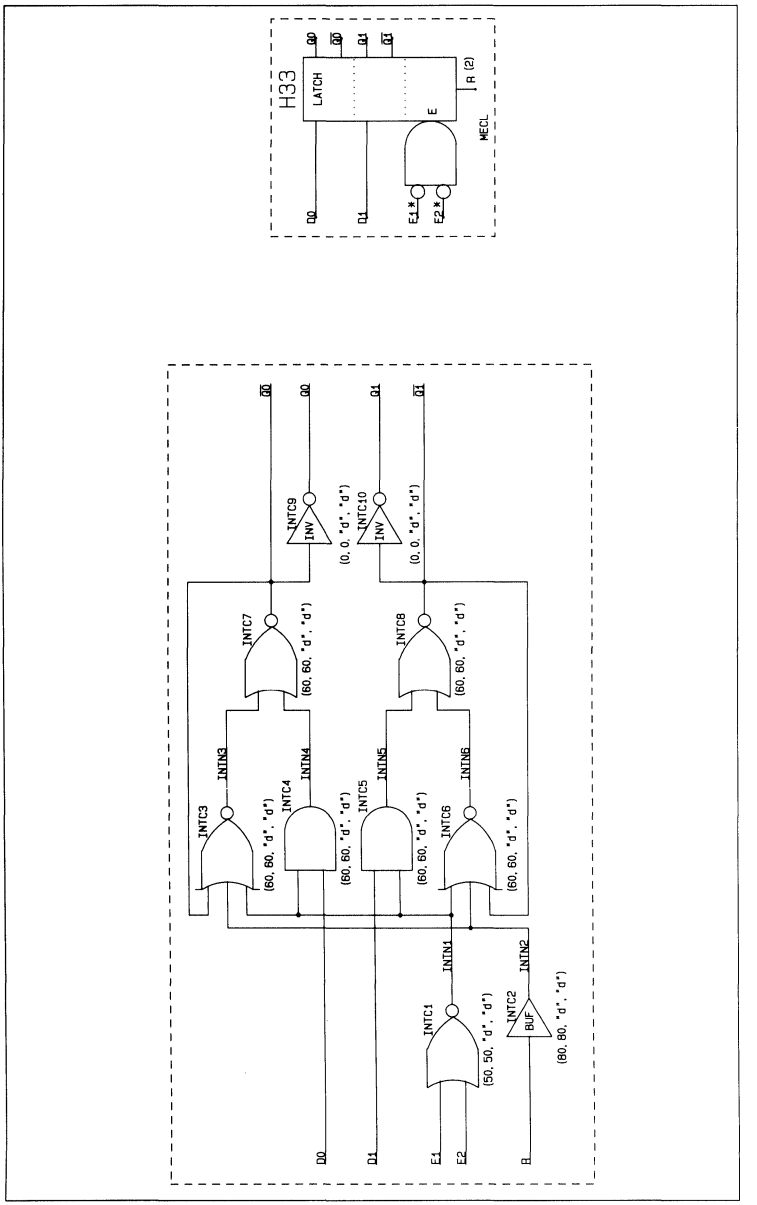
COMPONENT PLOTS

Plot 19



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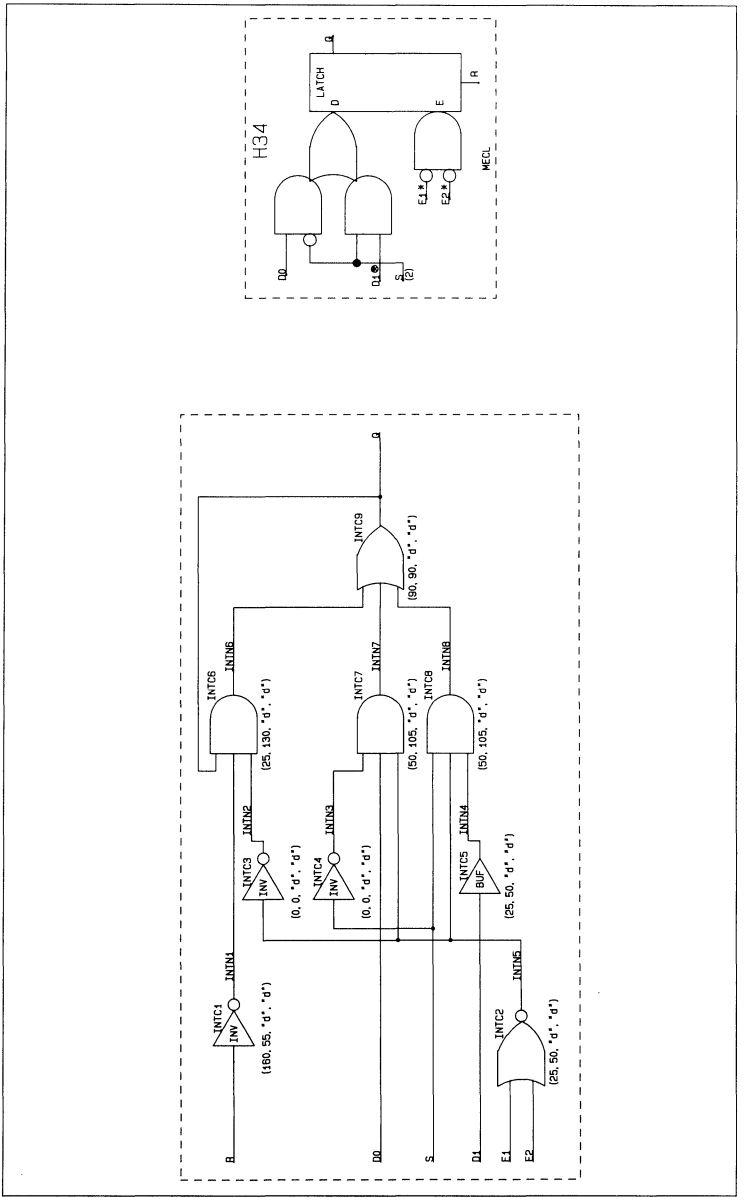
COMPONENT PLOTS

Plot 20



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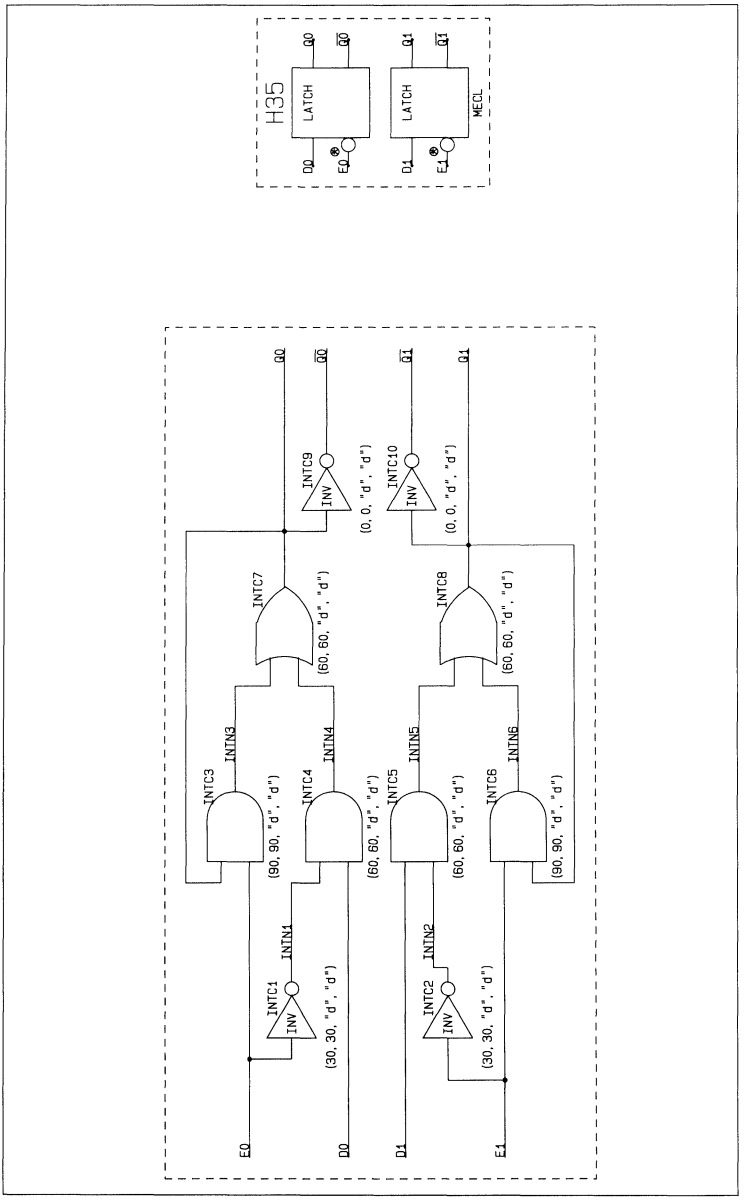
COMPONENT PLOTS

Plot 21



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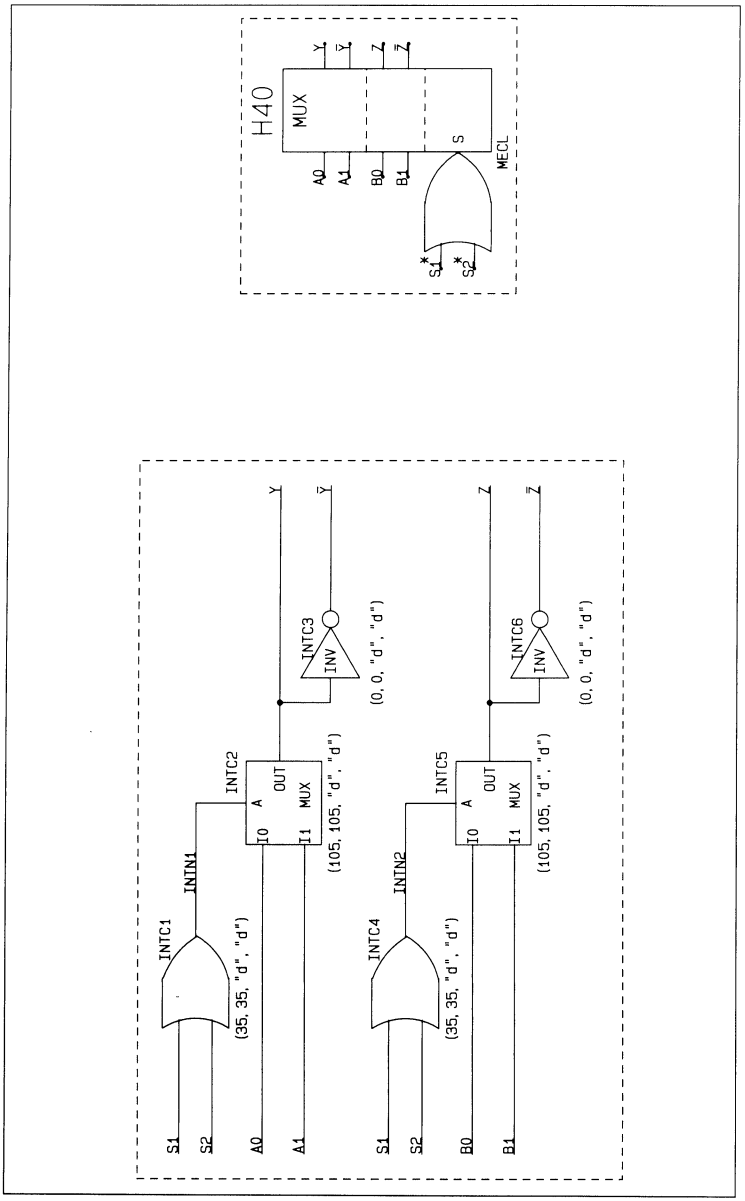
COMPONENT PLOTS

Plot 22



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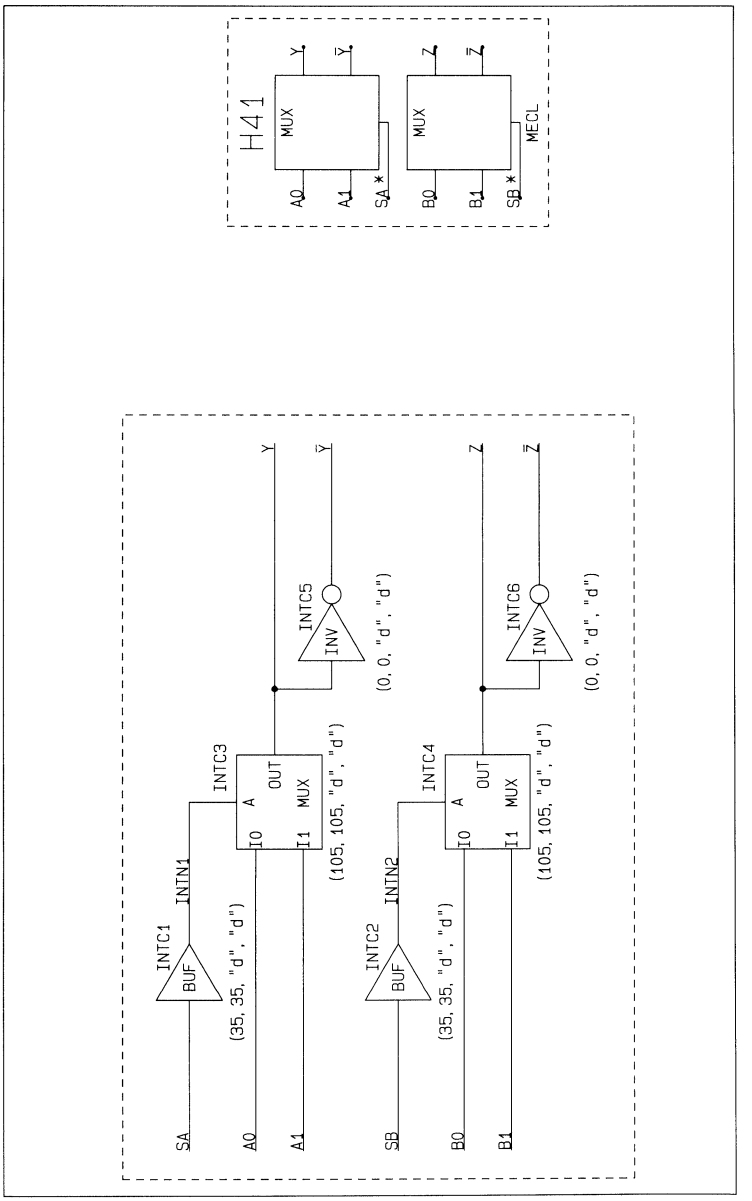
COMPONENT PLOTS

Plot 23



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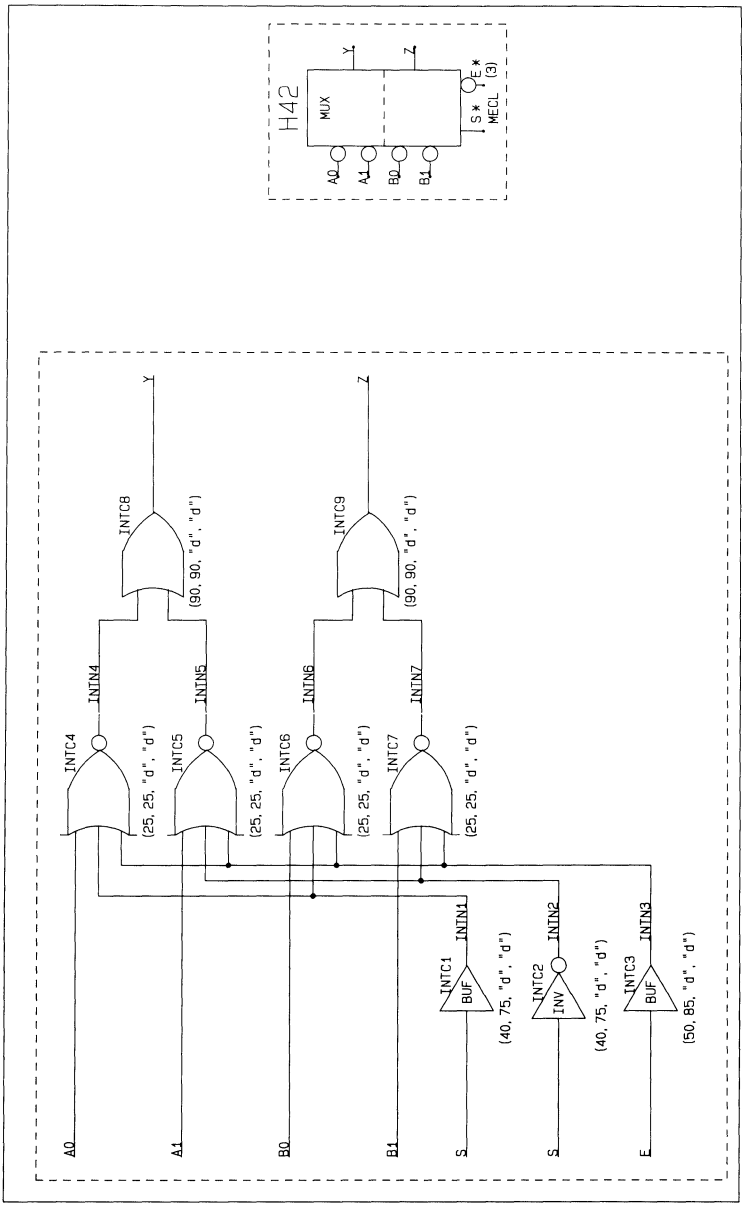
COMPONENT PLOTS

Plot 24



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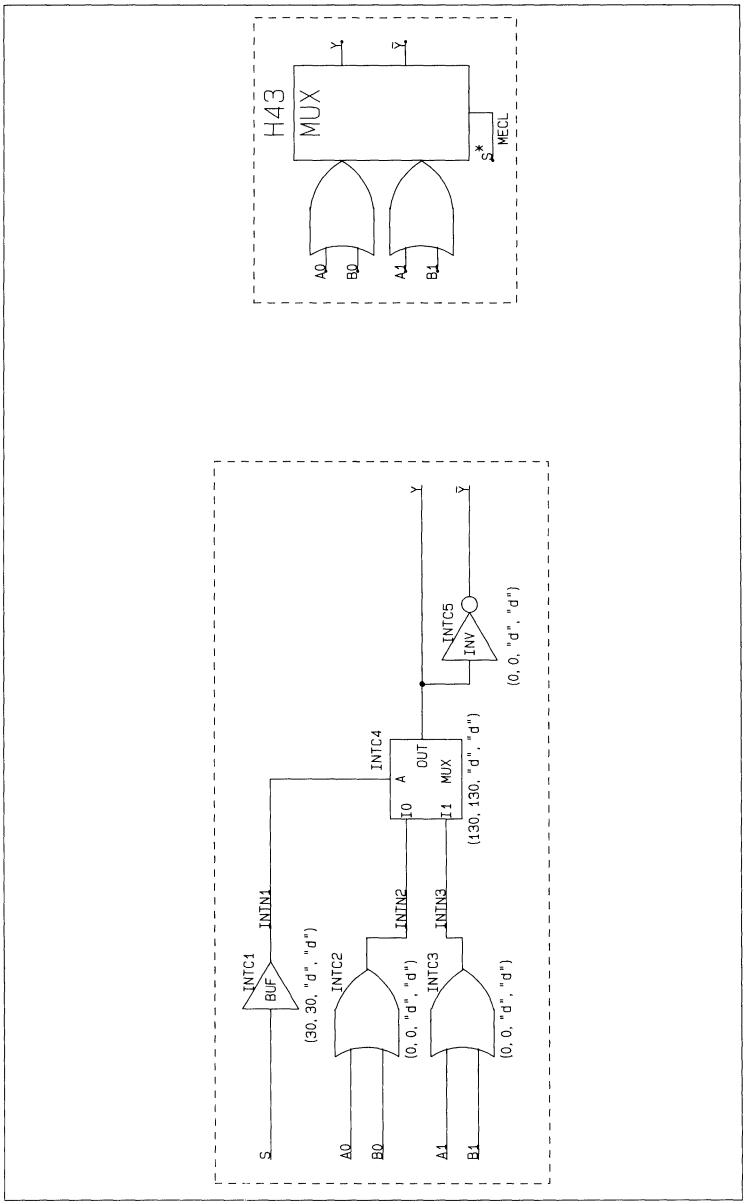
COMPONENT PLOTS

Plot 25



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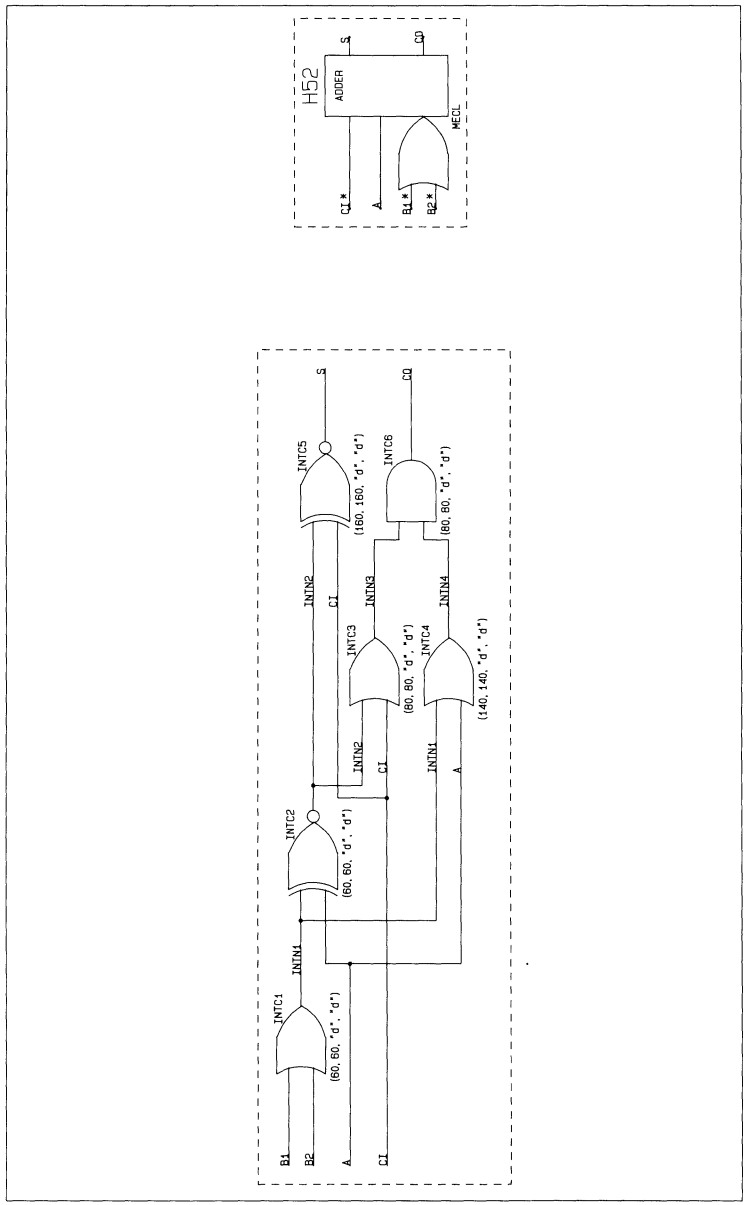
COMPONENT PLOTS

Plot 26



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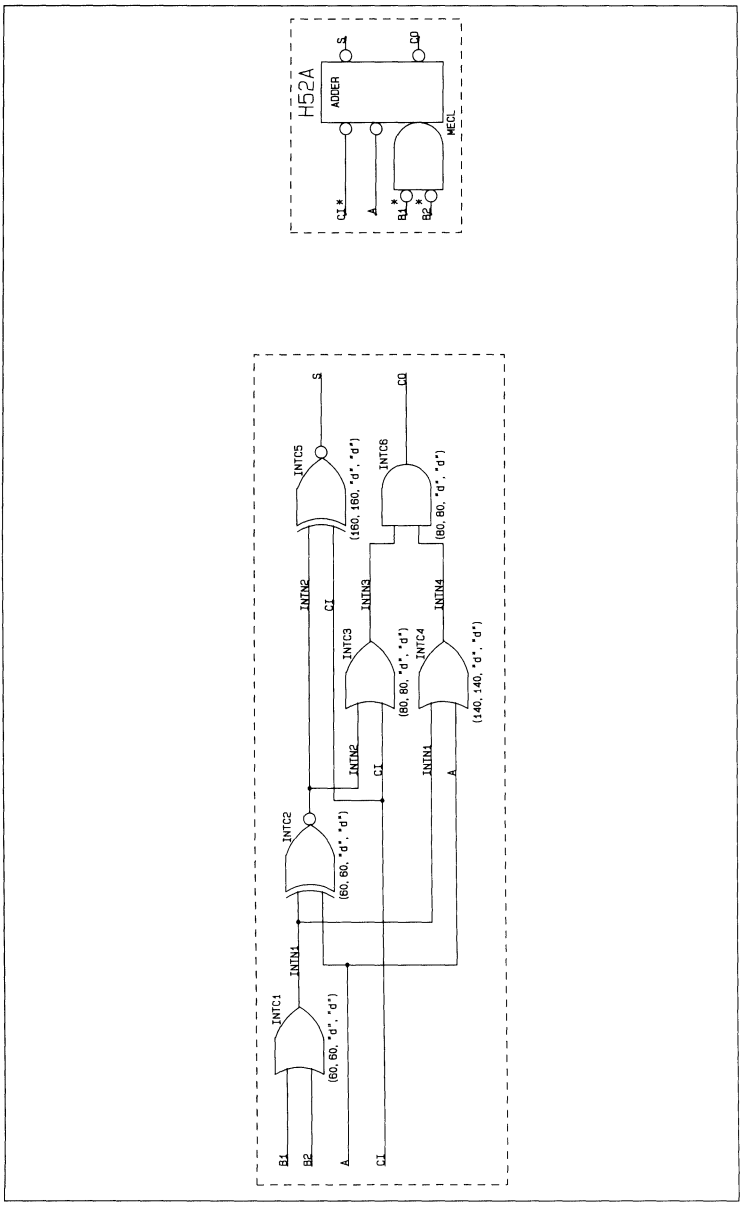
COMPONENT PLOTS

Plot 27



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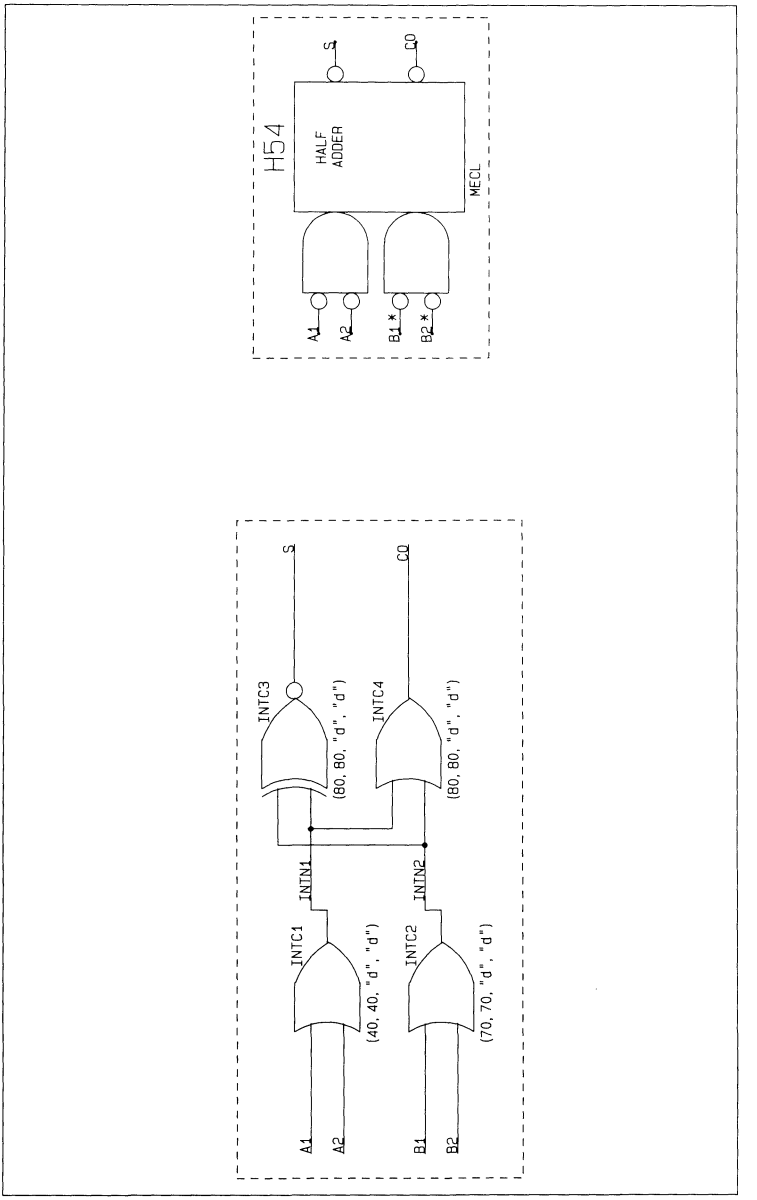
COMPONENT PLOTS

Plot 28



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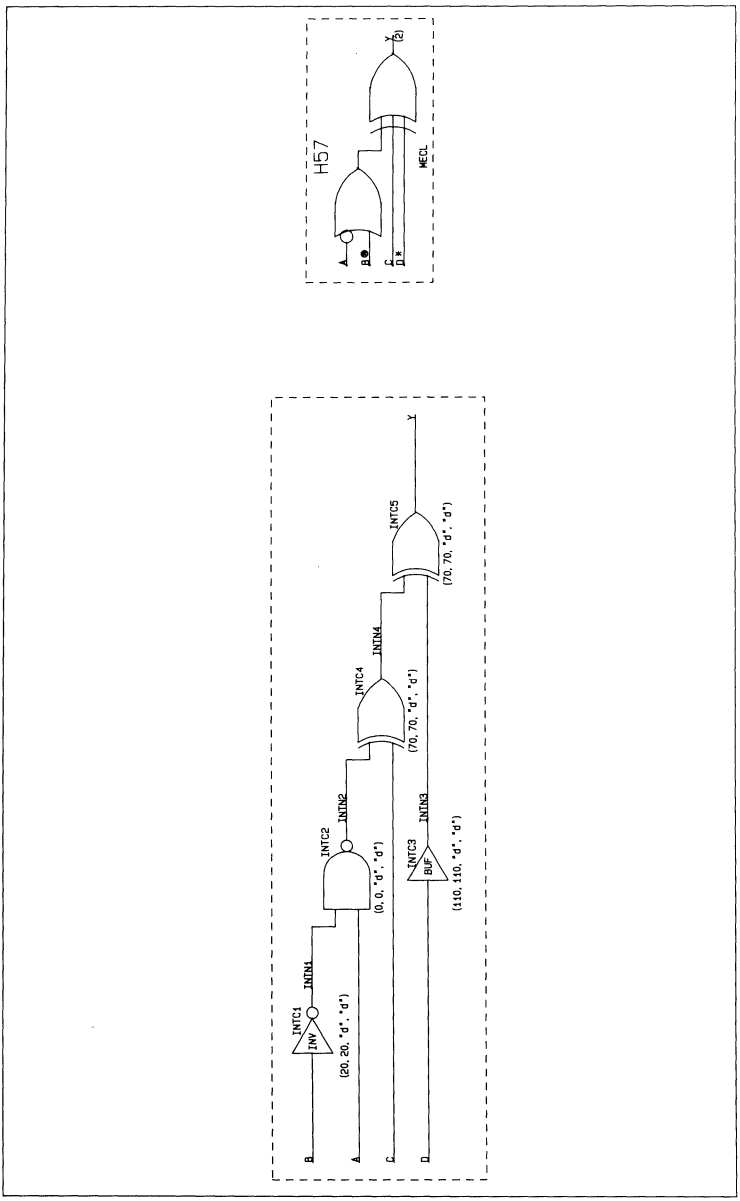
COMPONENT PLOTS

Plot 29



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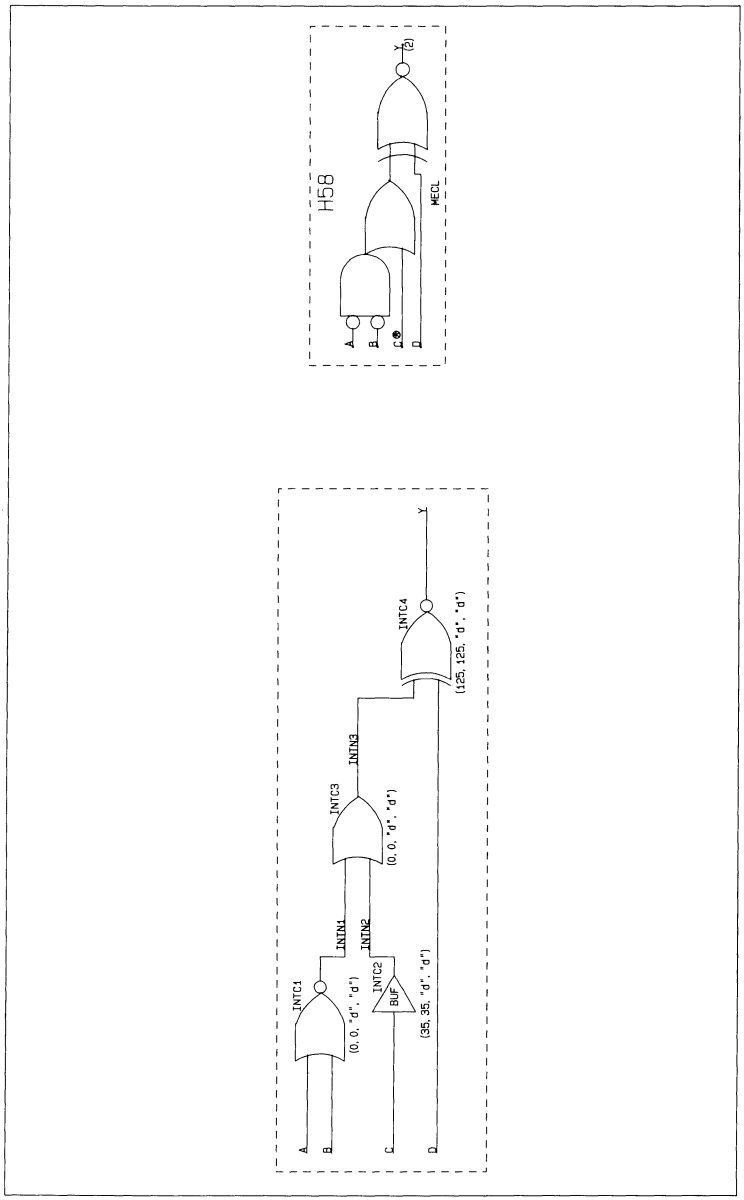
COMPONENT PLOTS

Plot 30



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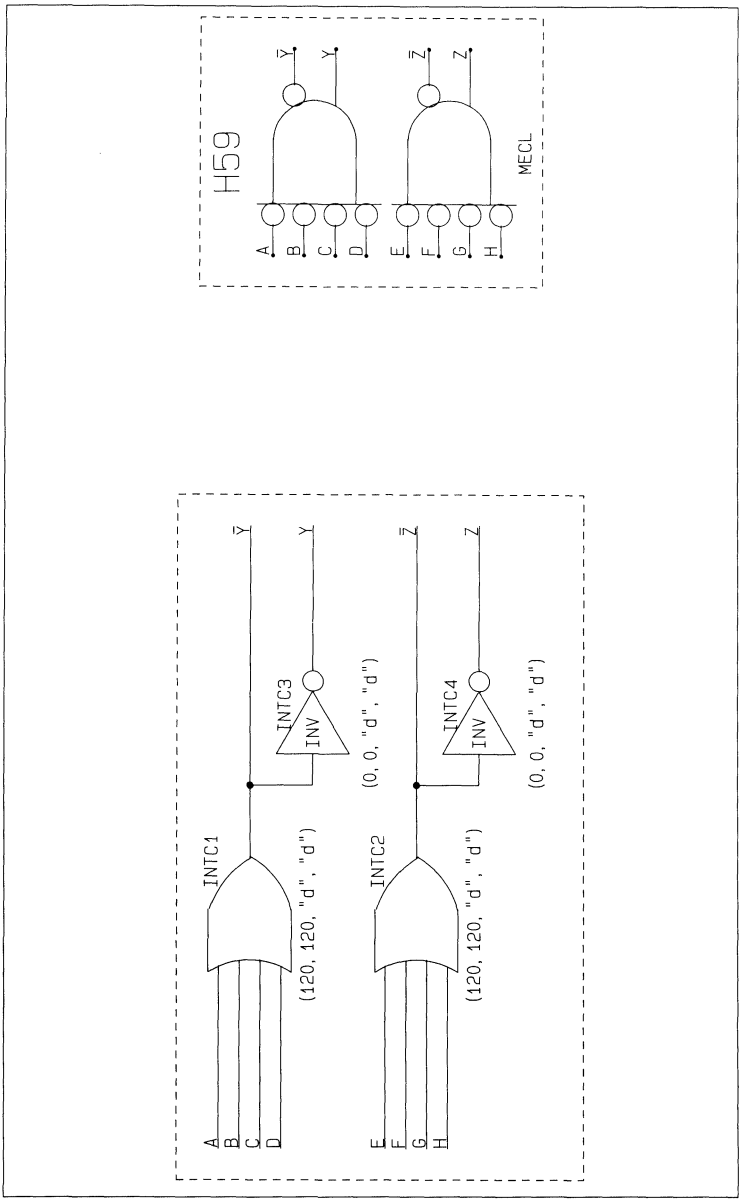
COMPONENT PLOTS

Plot 31



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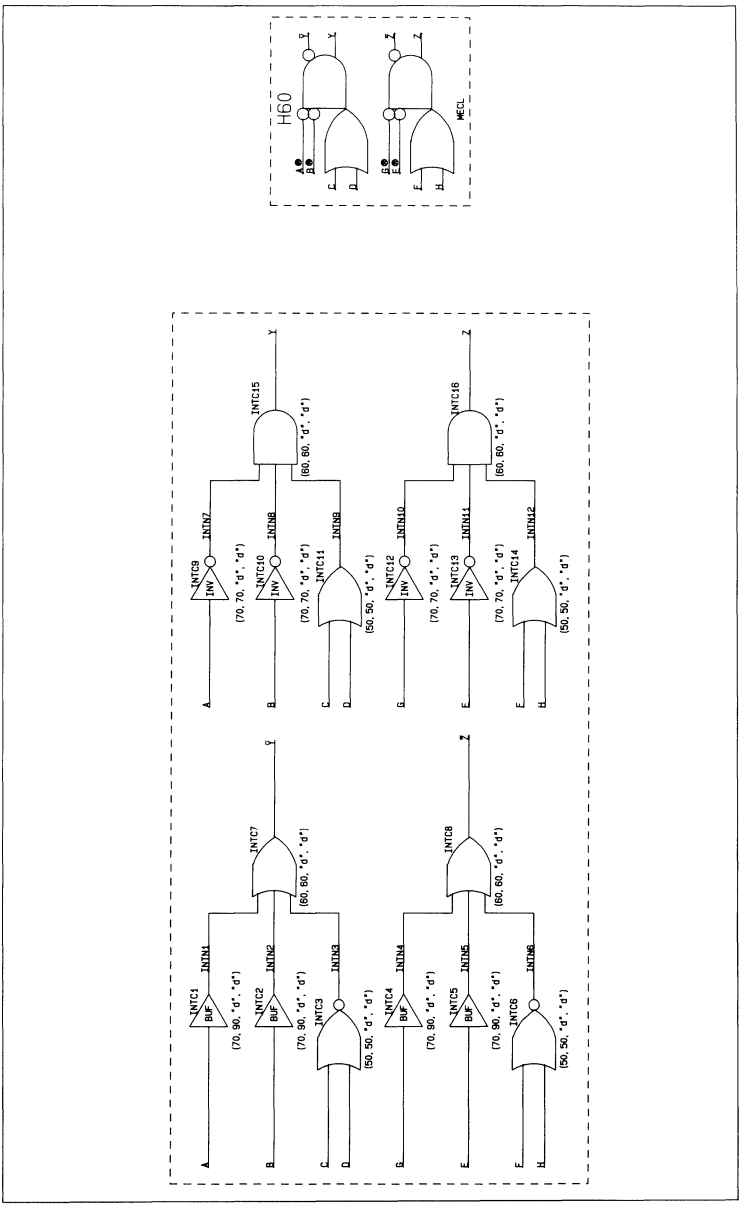
COMPONENT PLOTS

Plot 32



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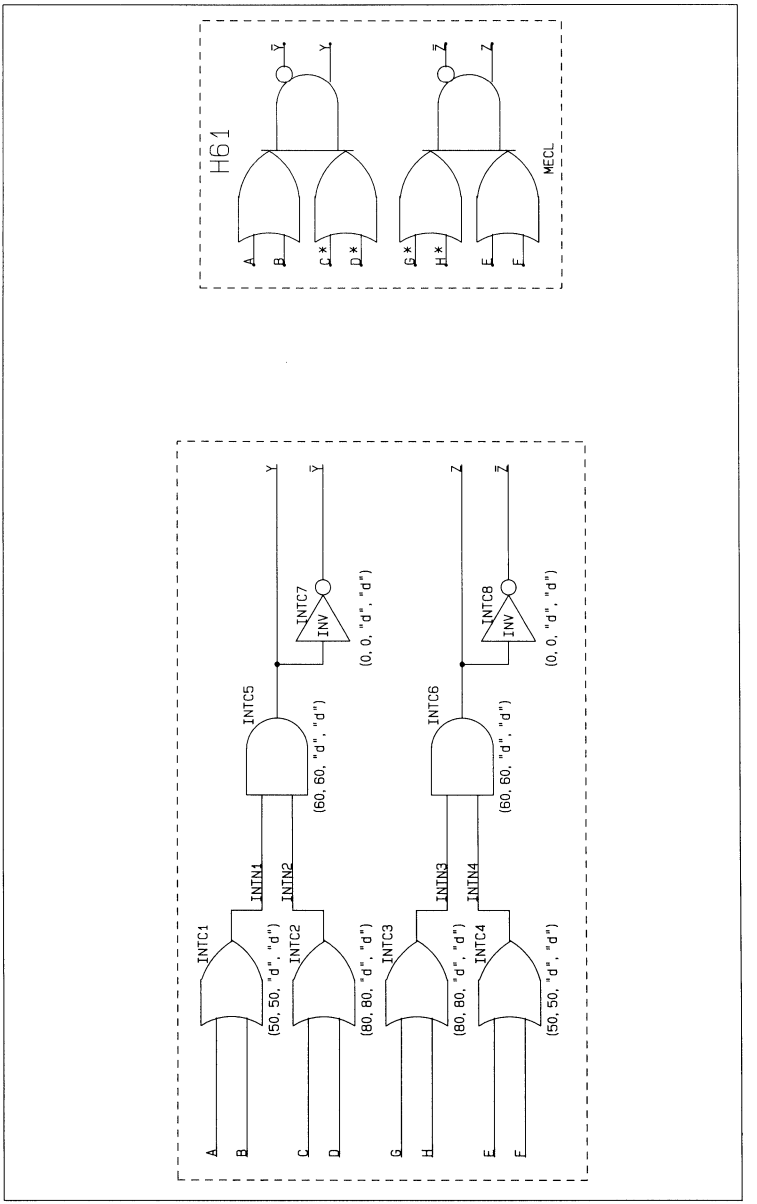
COMPONENT PLOTS

Plot 33



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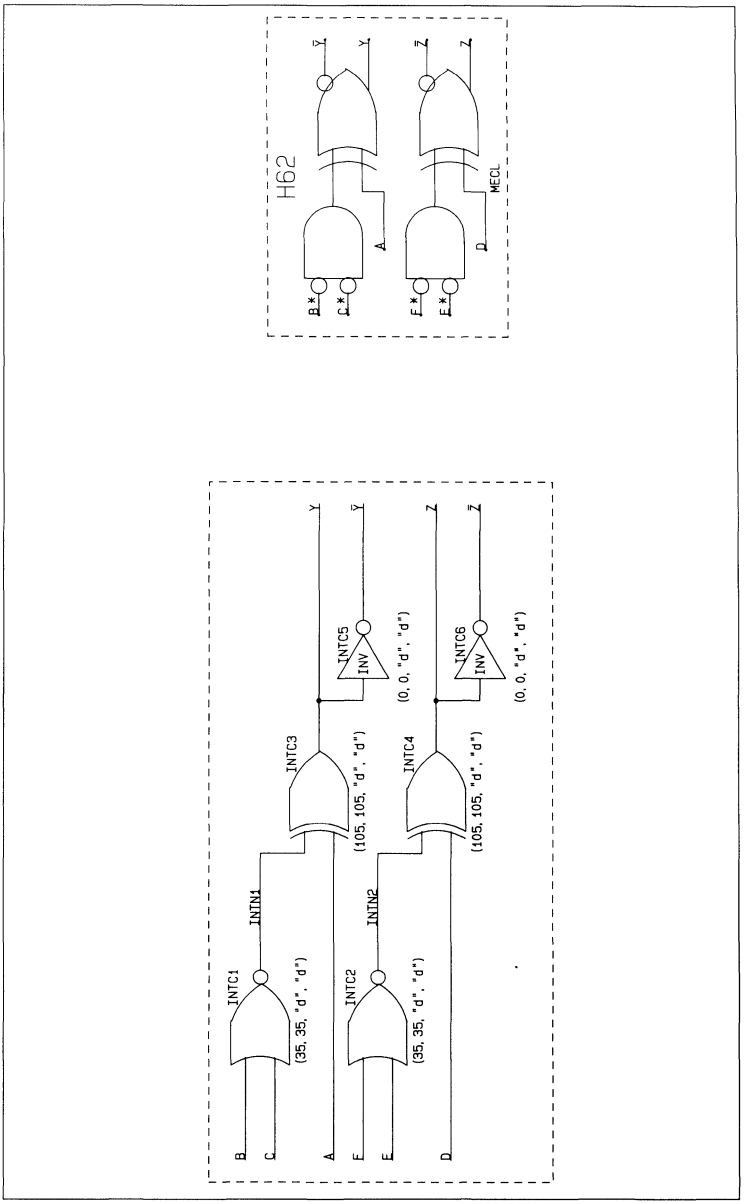
COMPONENT PLOTS

Plot 34



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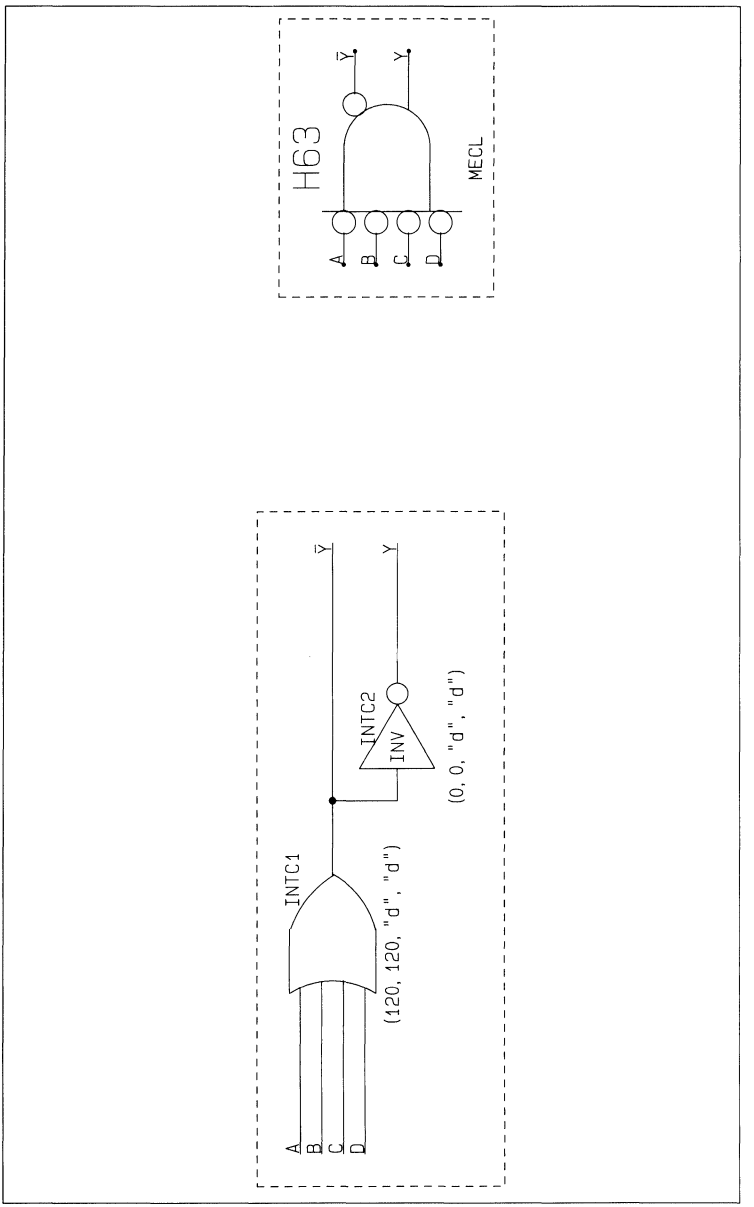
COMPONENT PLOTS

Plot 35



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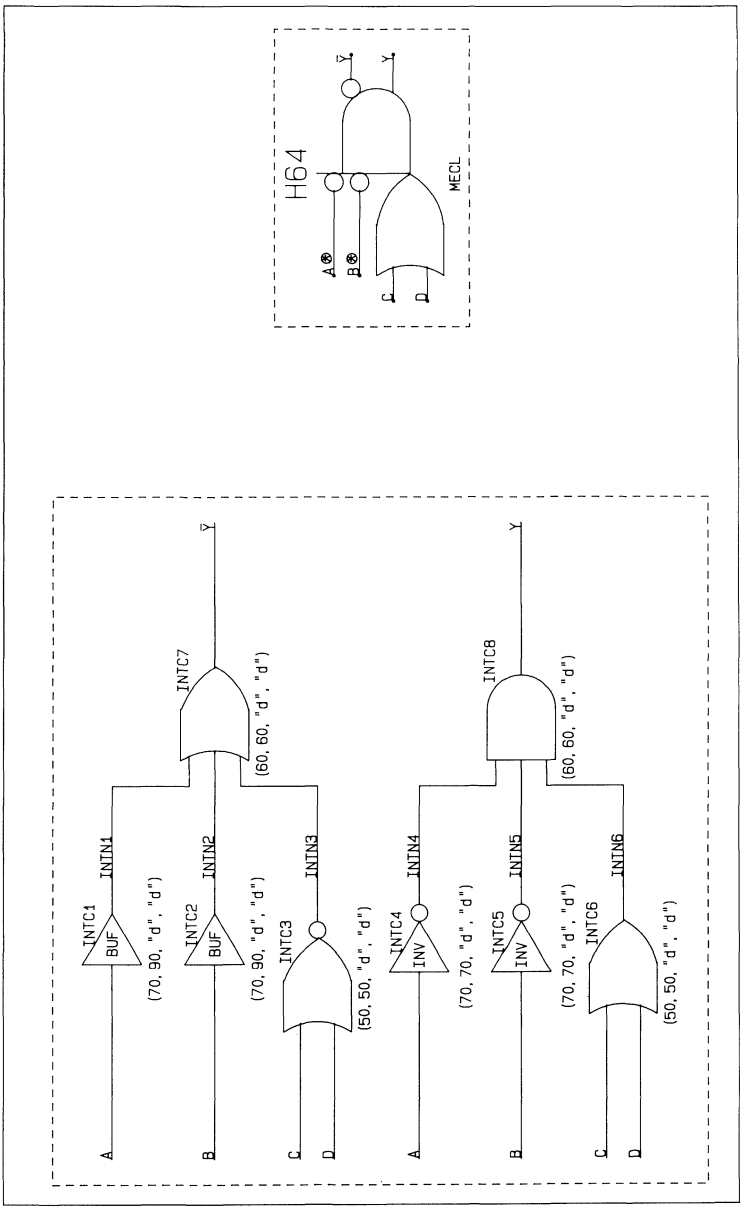
COMPONENT PLOTS

Plot 36



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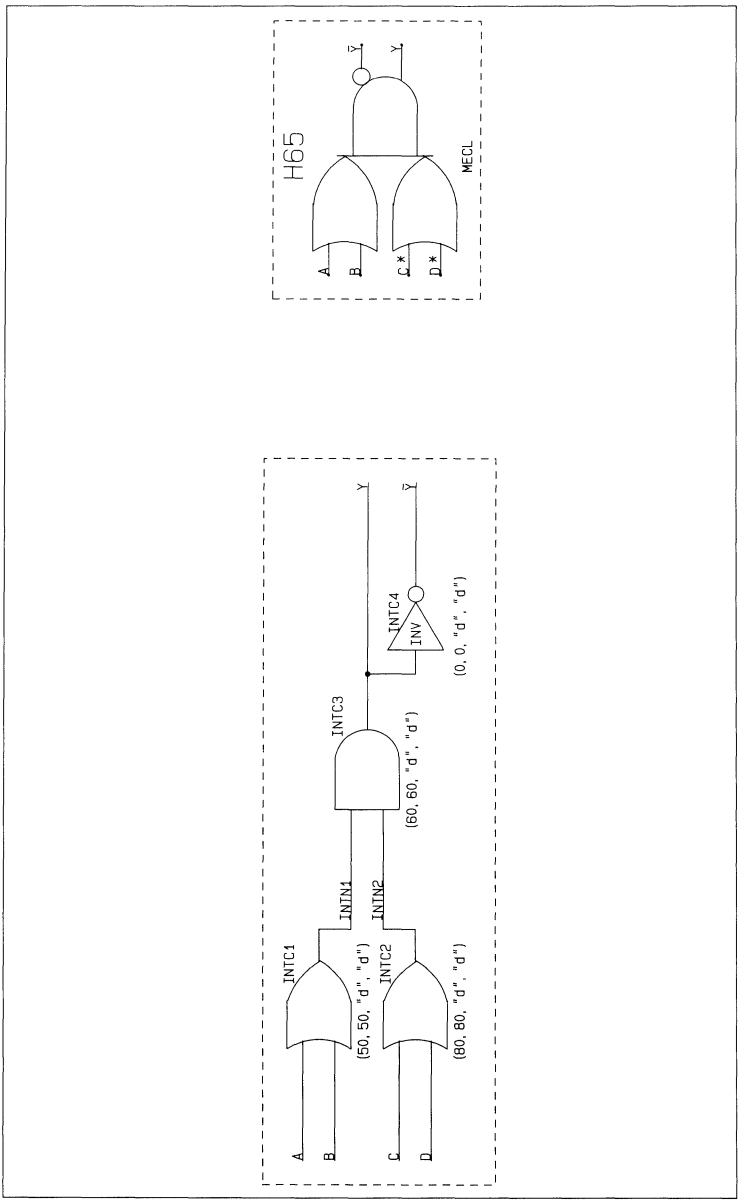
COMPONENT PLOTS

Plot 37



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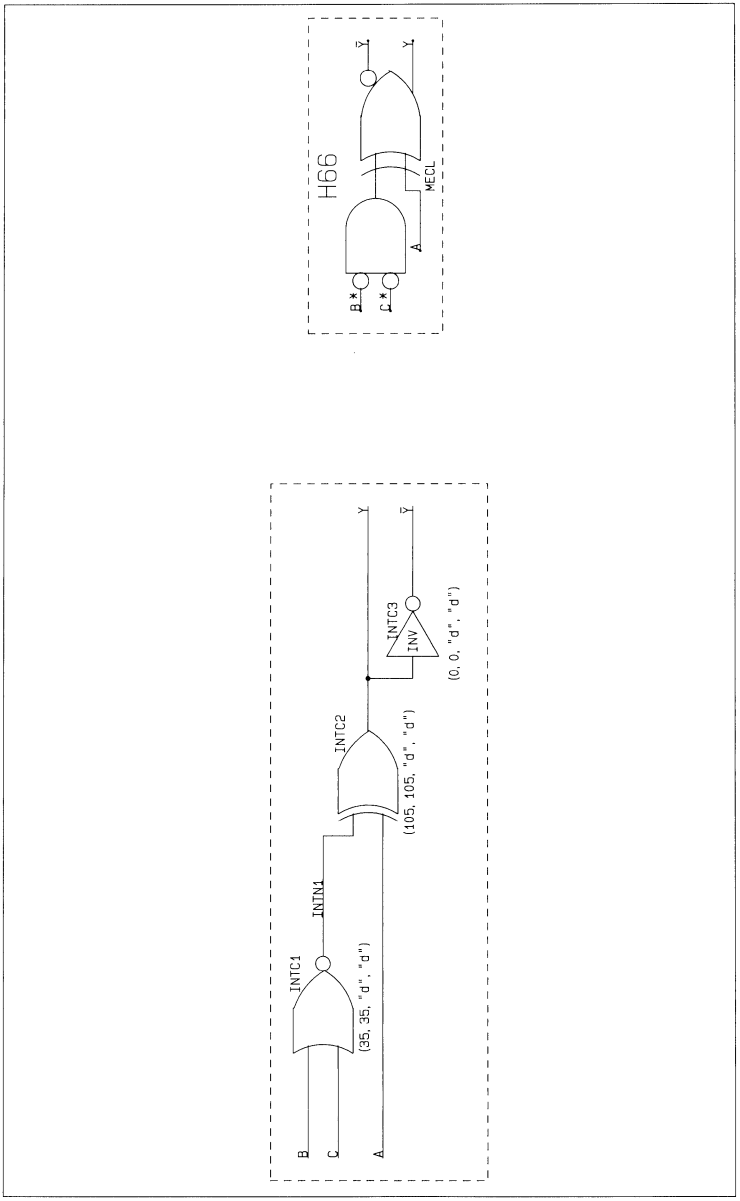
COMPONENT PLOTS

Plot 38



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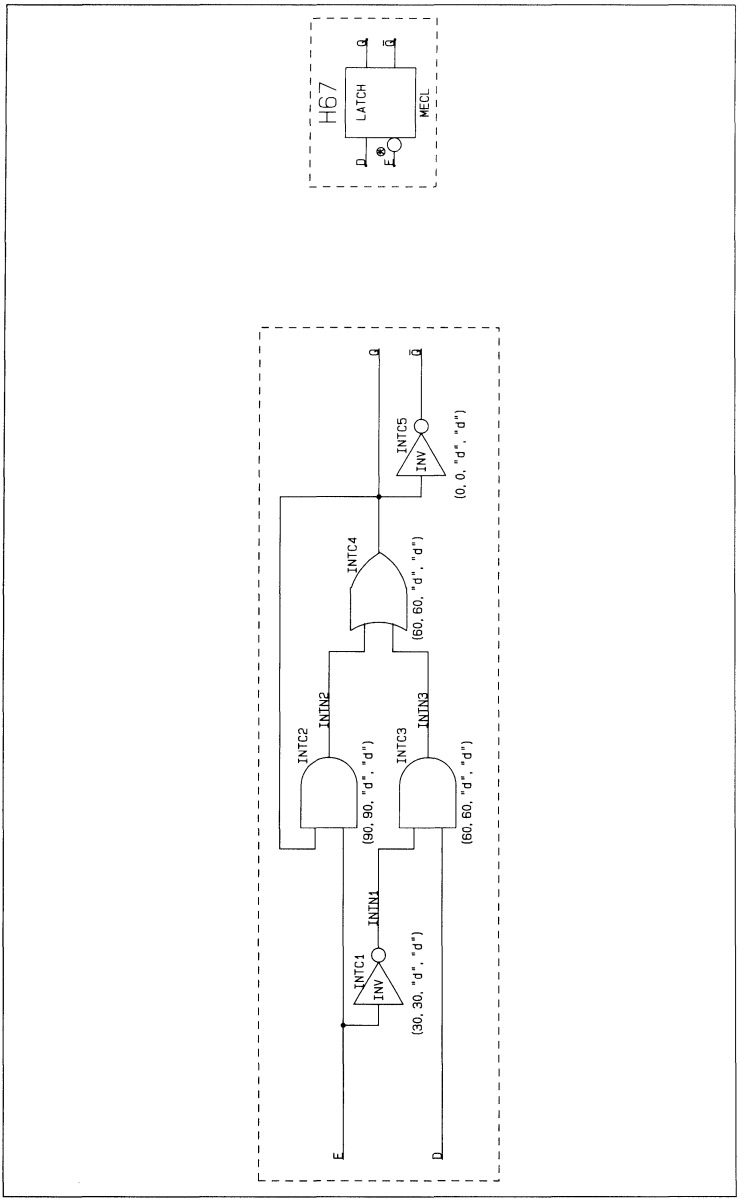
COMPONENT PLOTS

Plot 39



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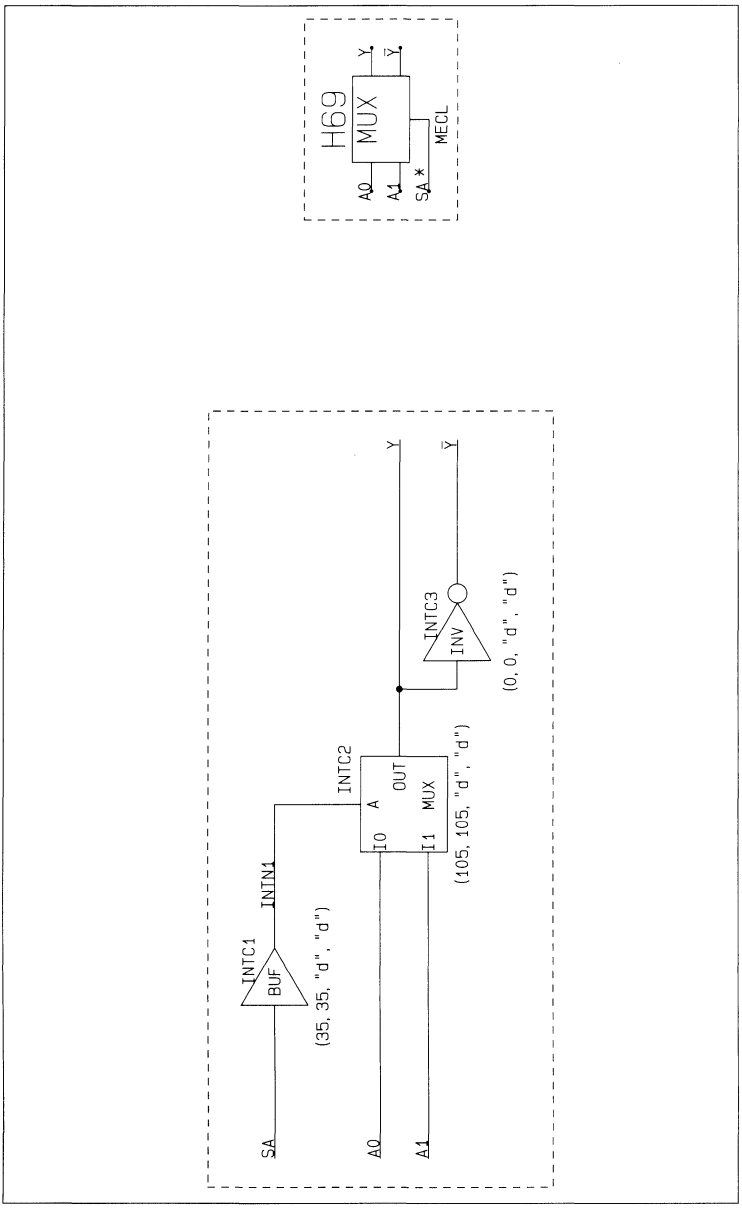
COMPONENT PLOTS

Plot 40



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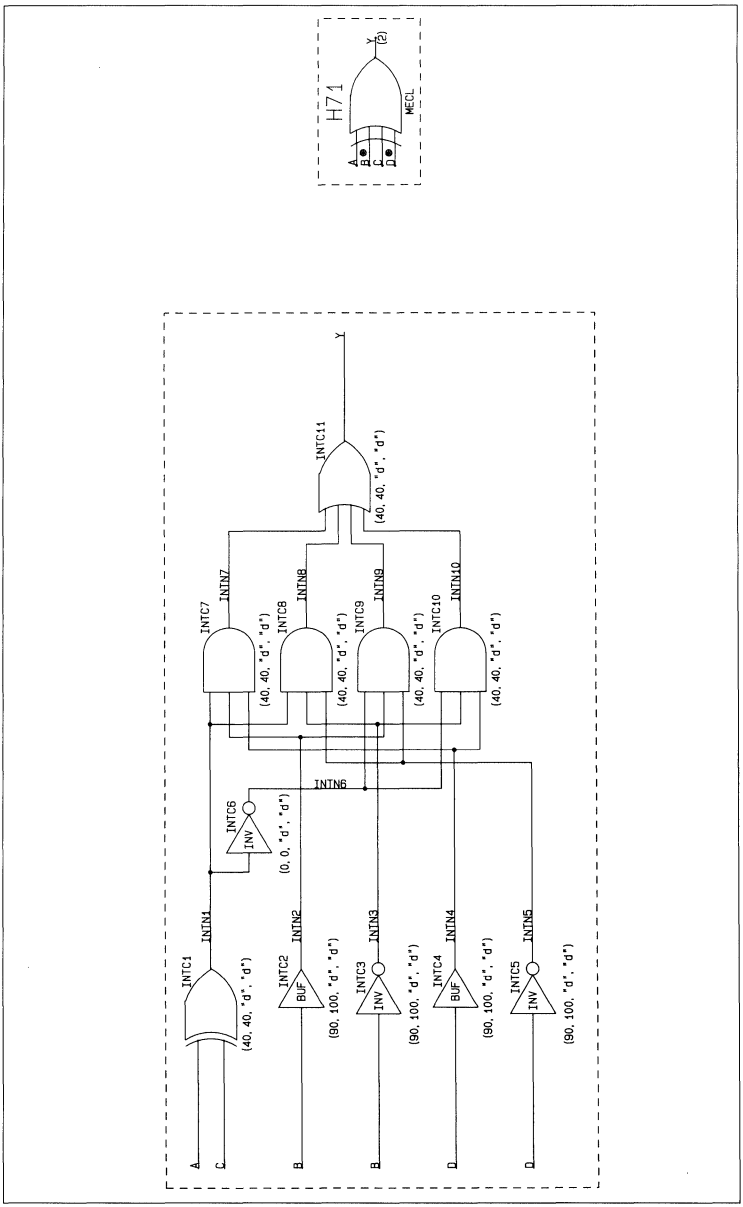
COMPONENT PLOTS

Plot 41



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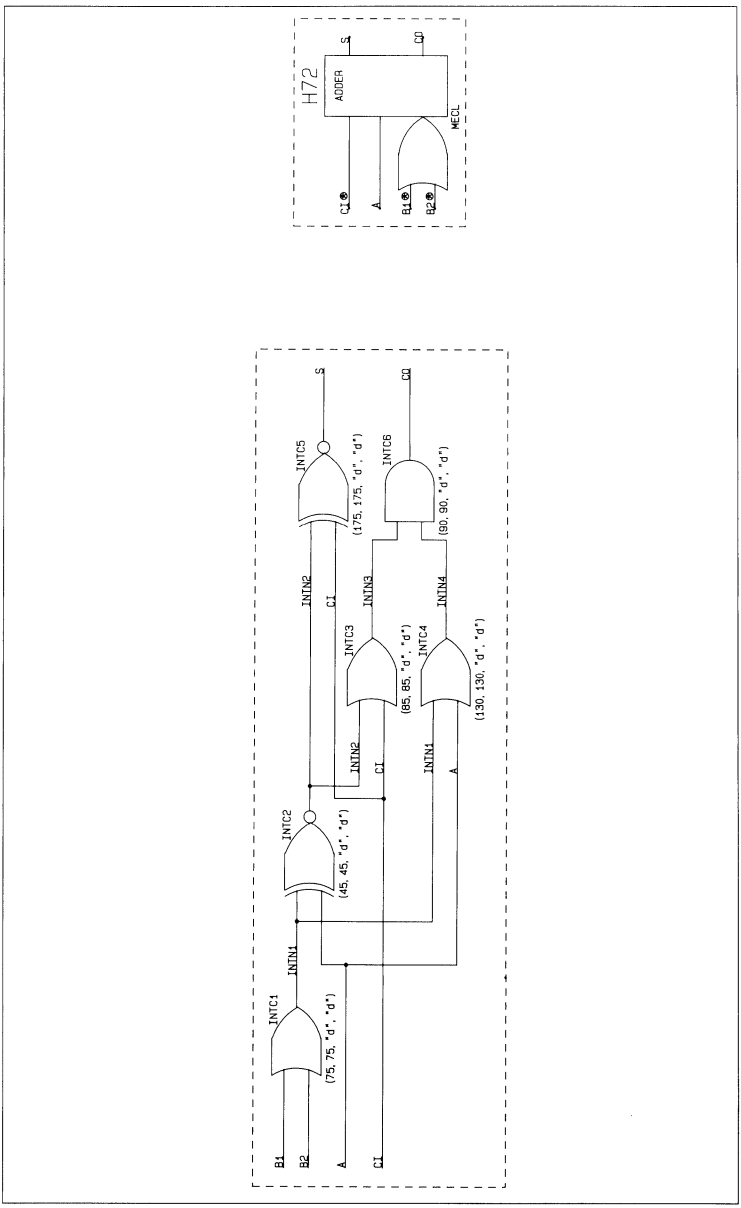
COMPONENT PLOTS

Plot 42



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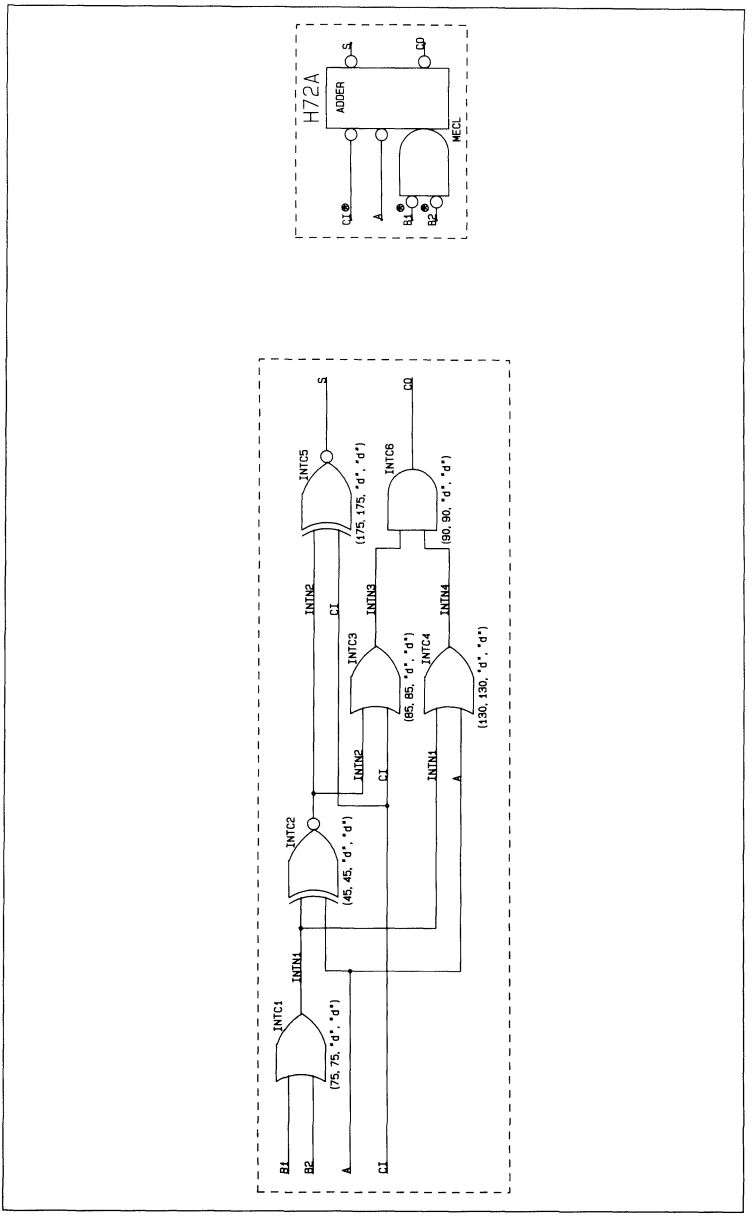
COMPONENT PLOTS

Plot 43



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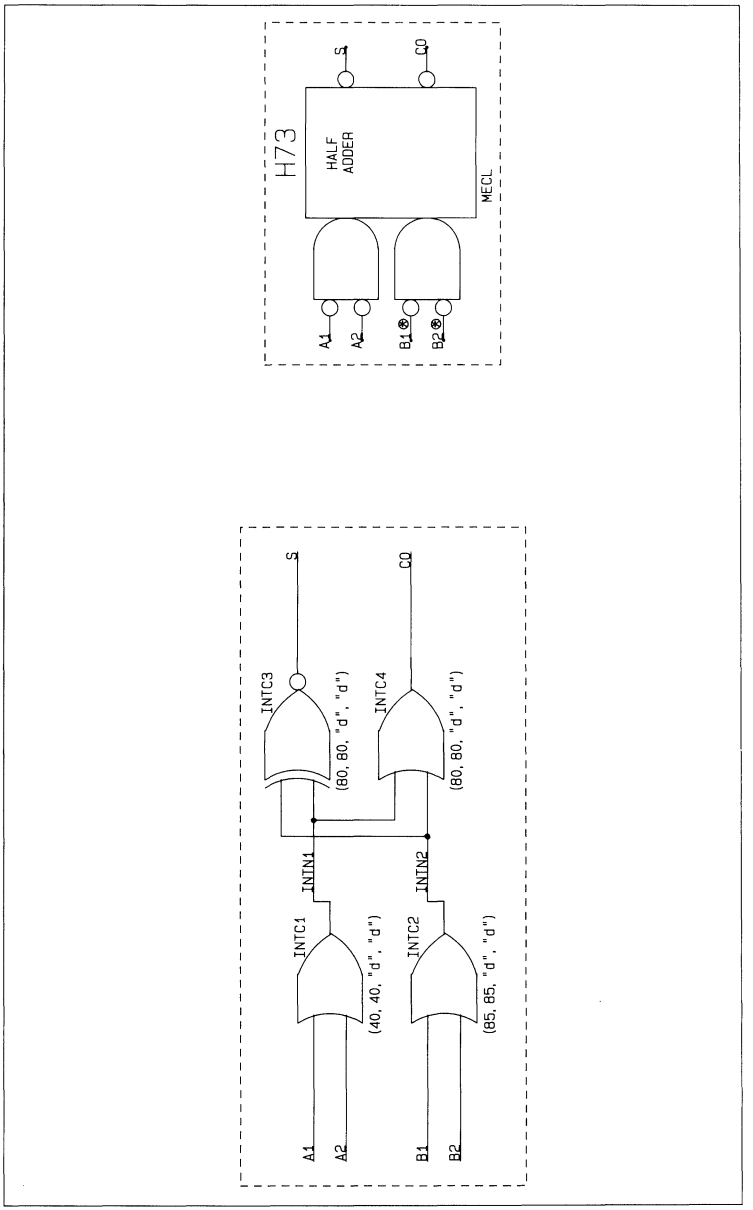
COMPONENT PLOTS

Plot 44



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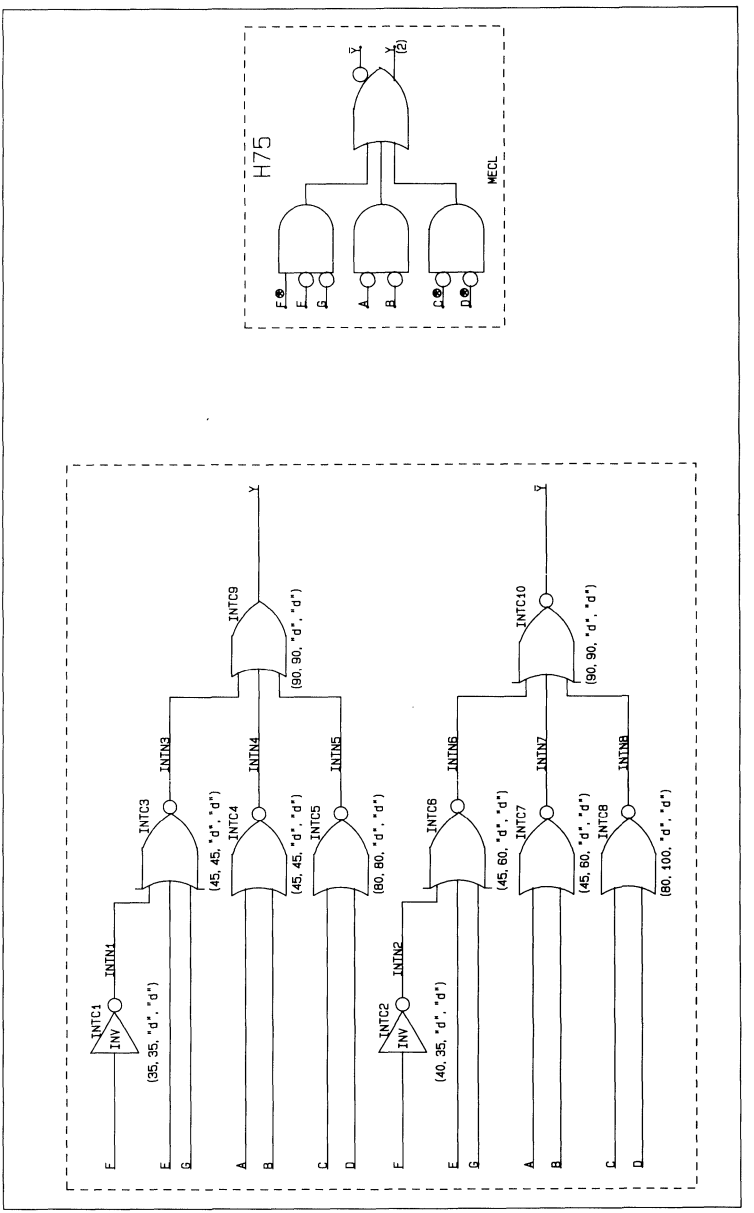
COMPONENT PLOTS

Plot 45



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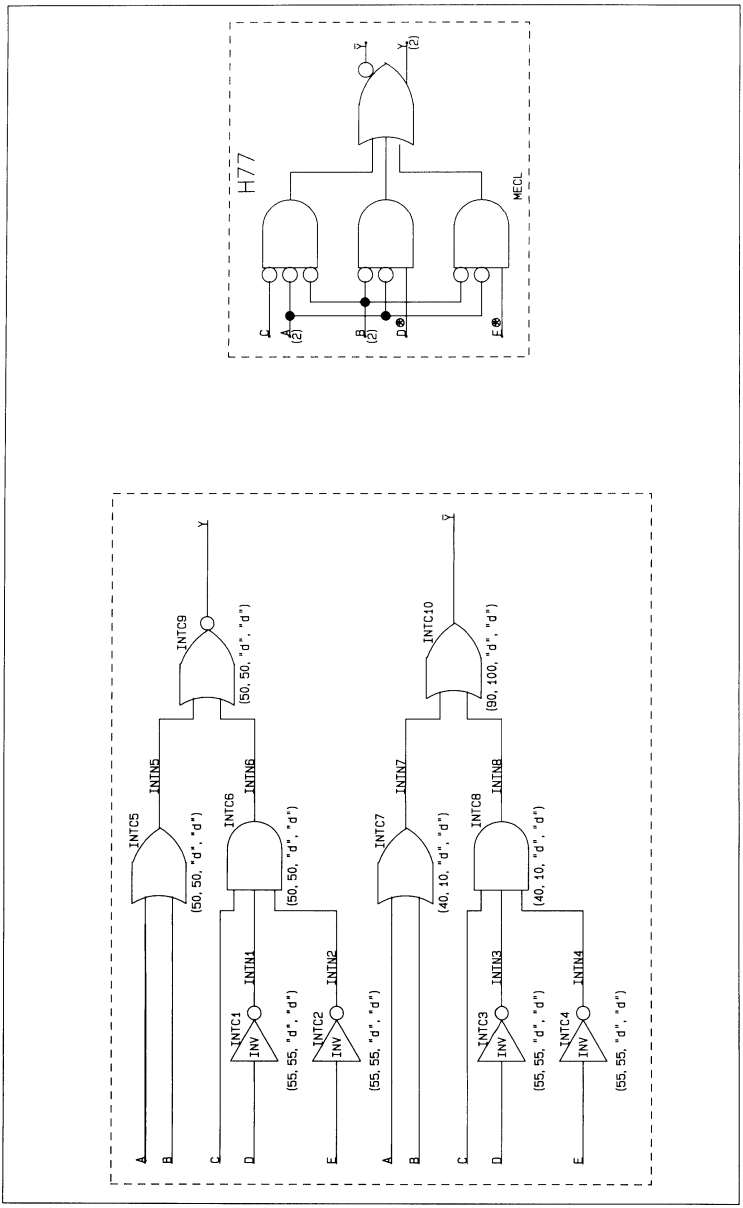
COMPONENT PLOTS

Plot 46



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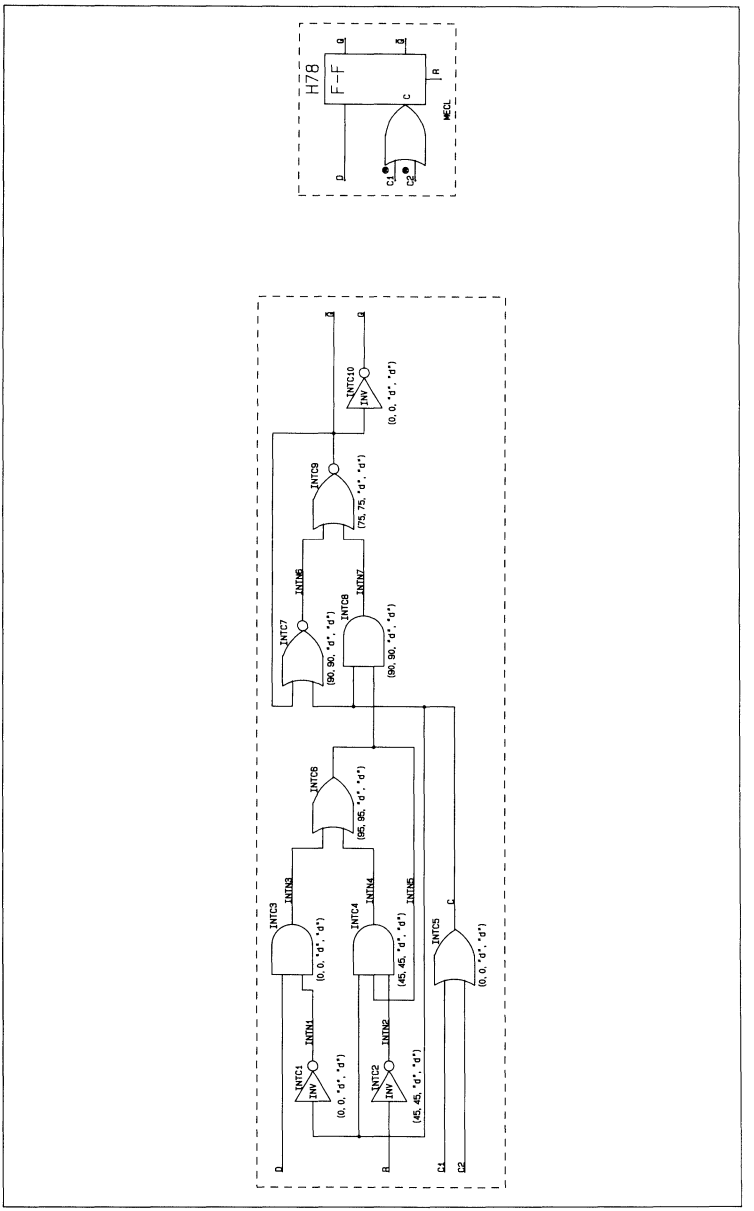
COMPONENT PLOTS

Plot 47



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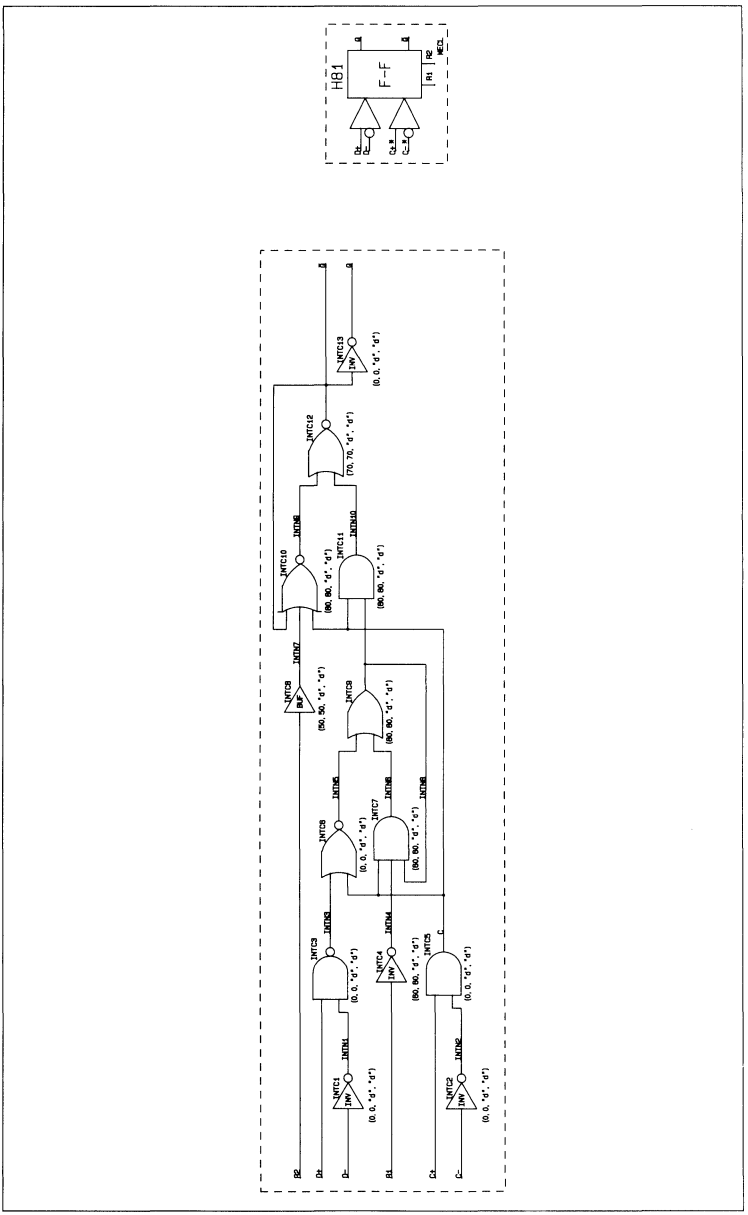
COMPONENT PLOTS

Plot 48



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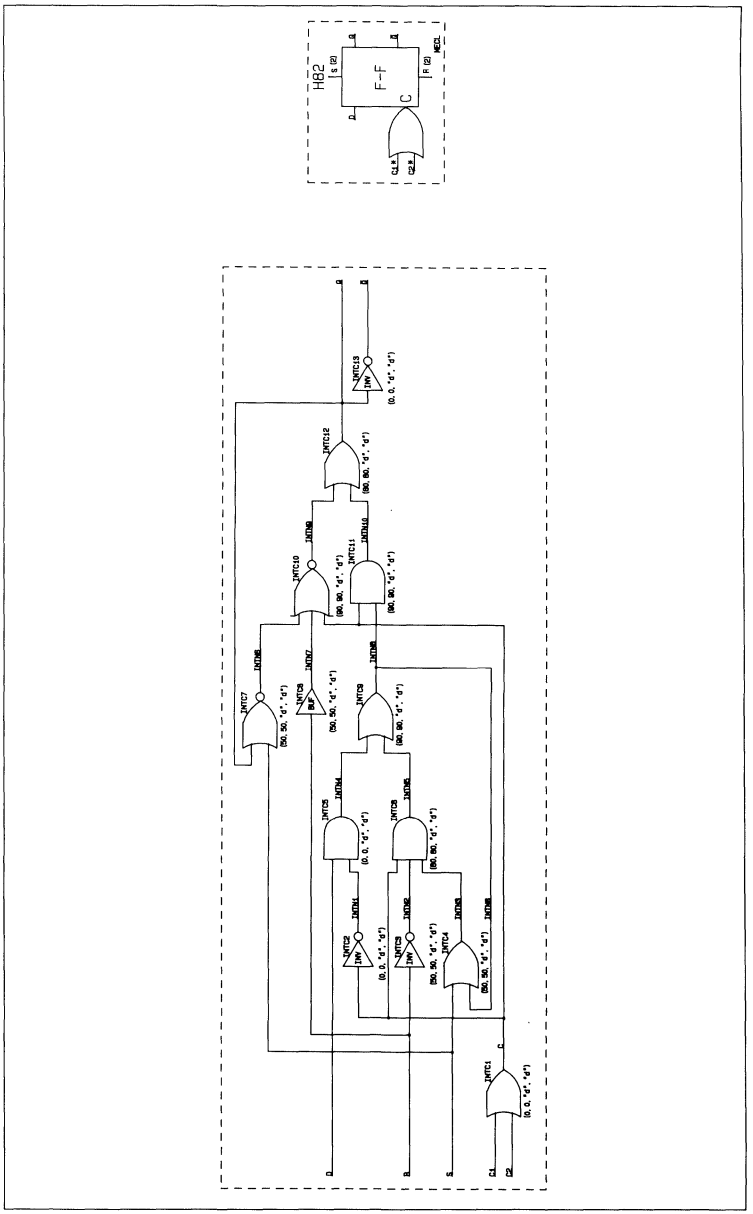
COMPONENT PLOTS

Plot 49



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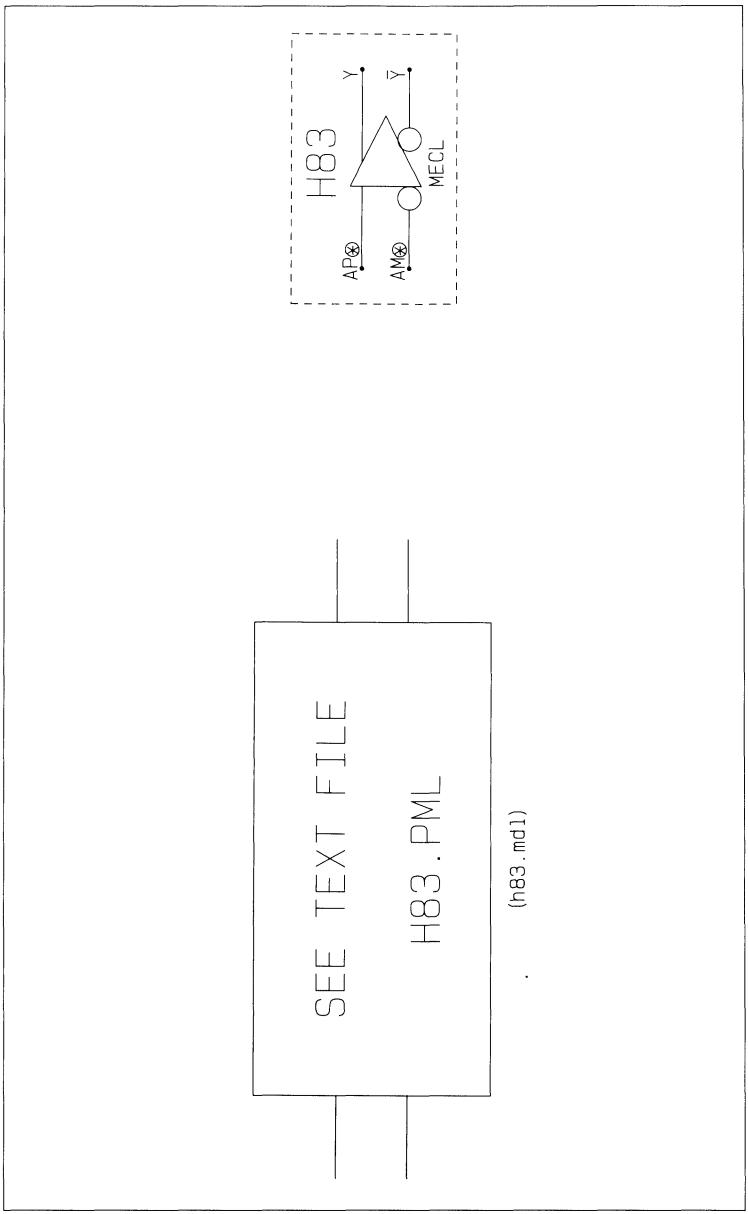
COMPONENT PLOTS

Plot 50



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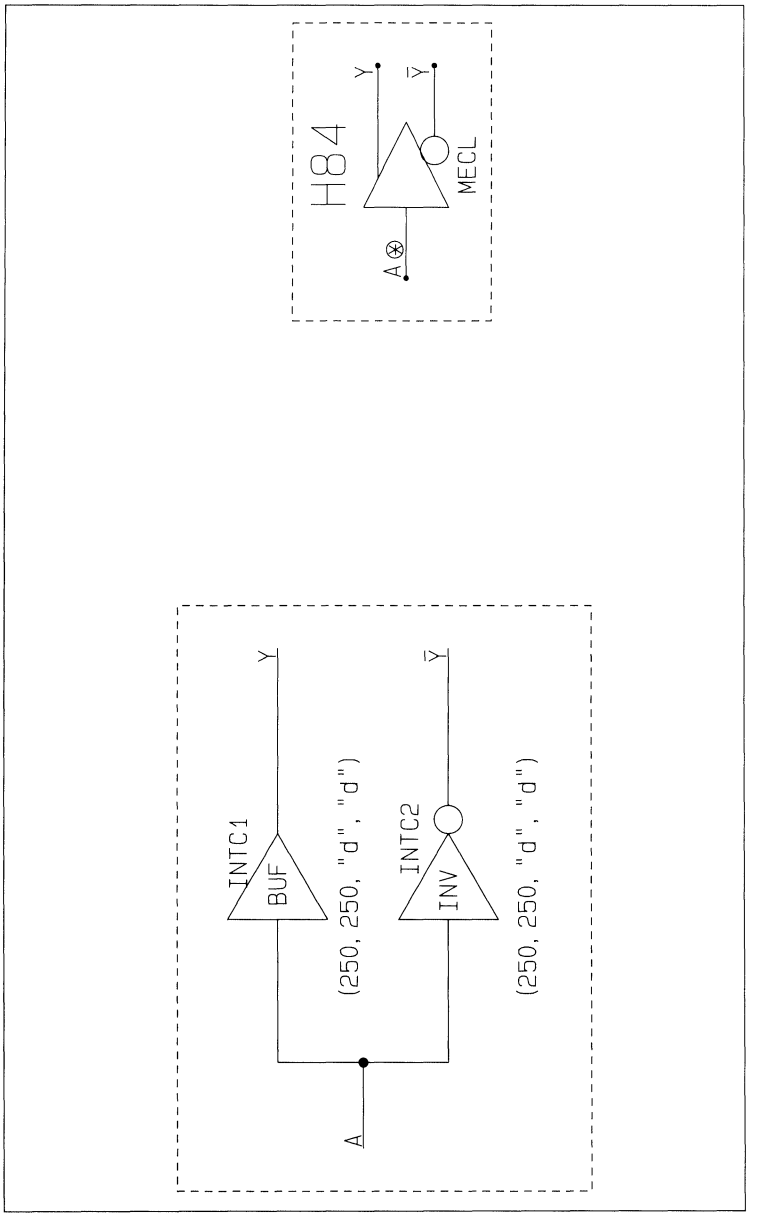
COMPONENT PLOTS

Plot 51



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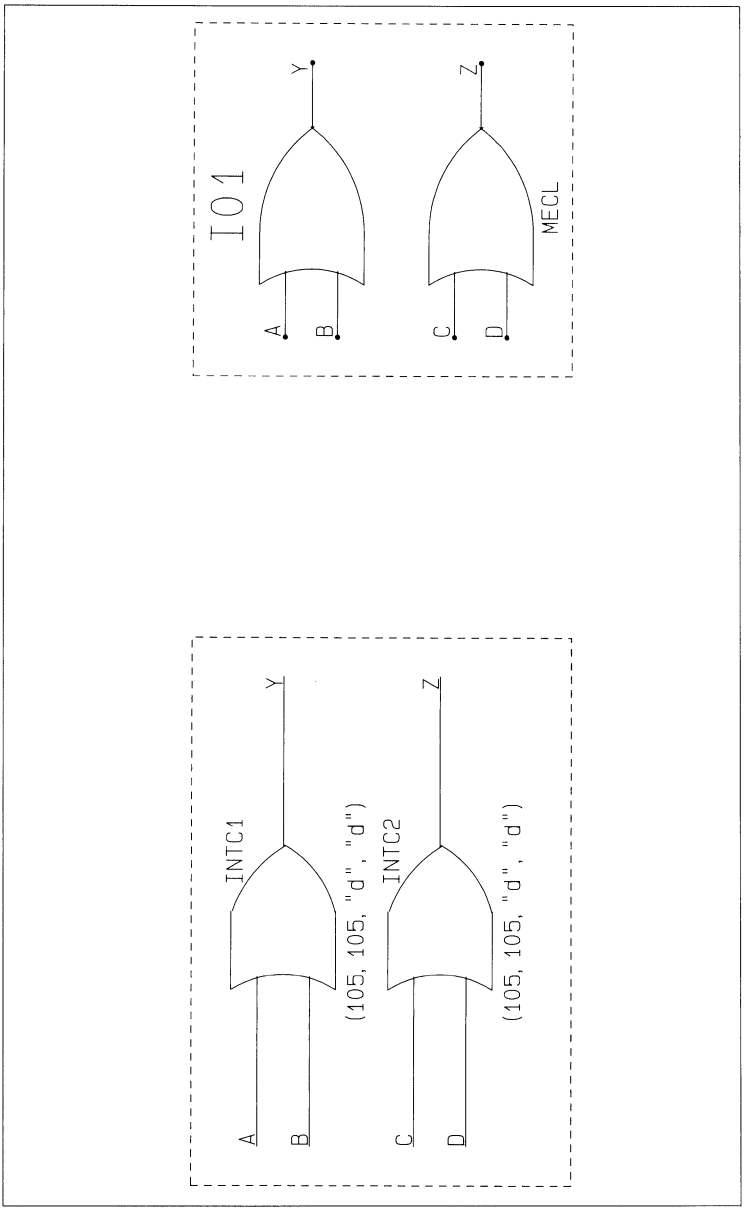
COMPONENT PLOTS

Plot 52



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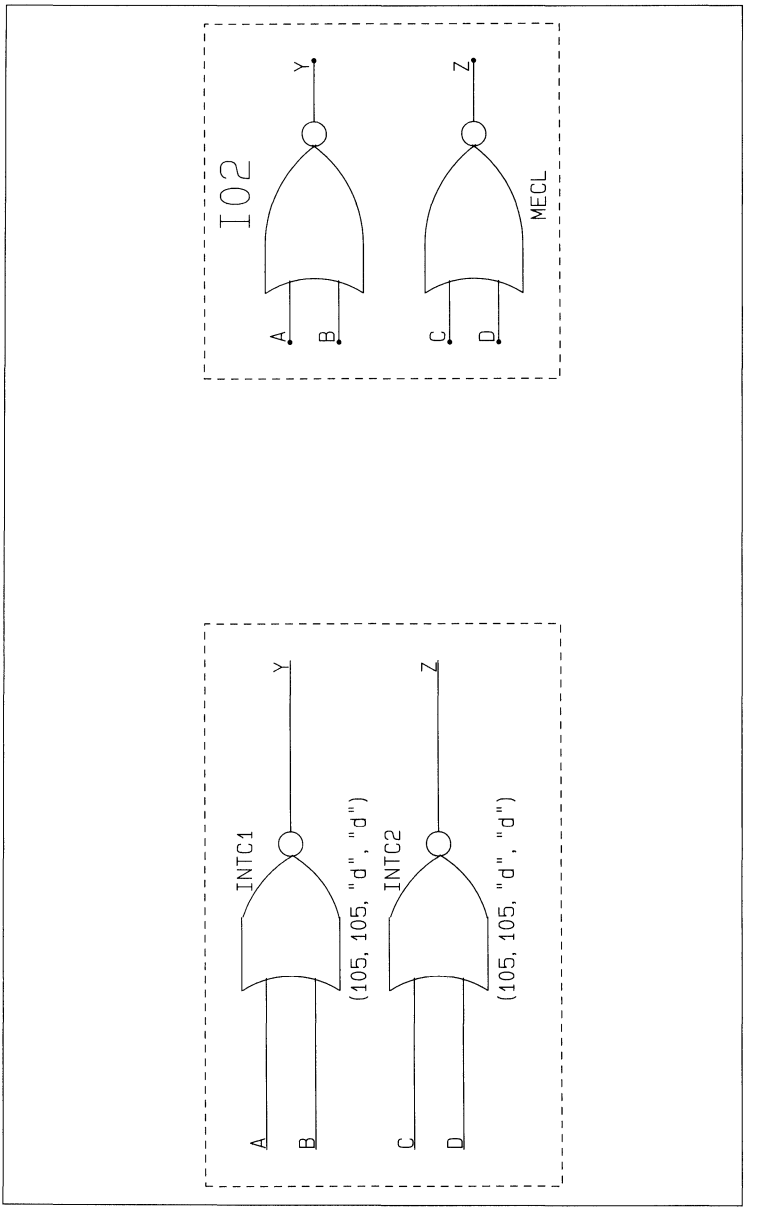
COMPONENT PLOTS

Plot 53



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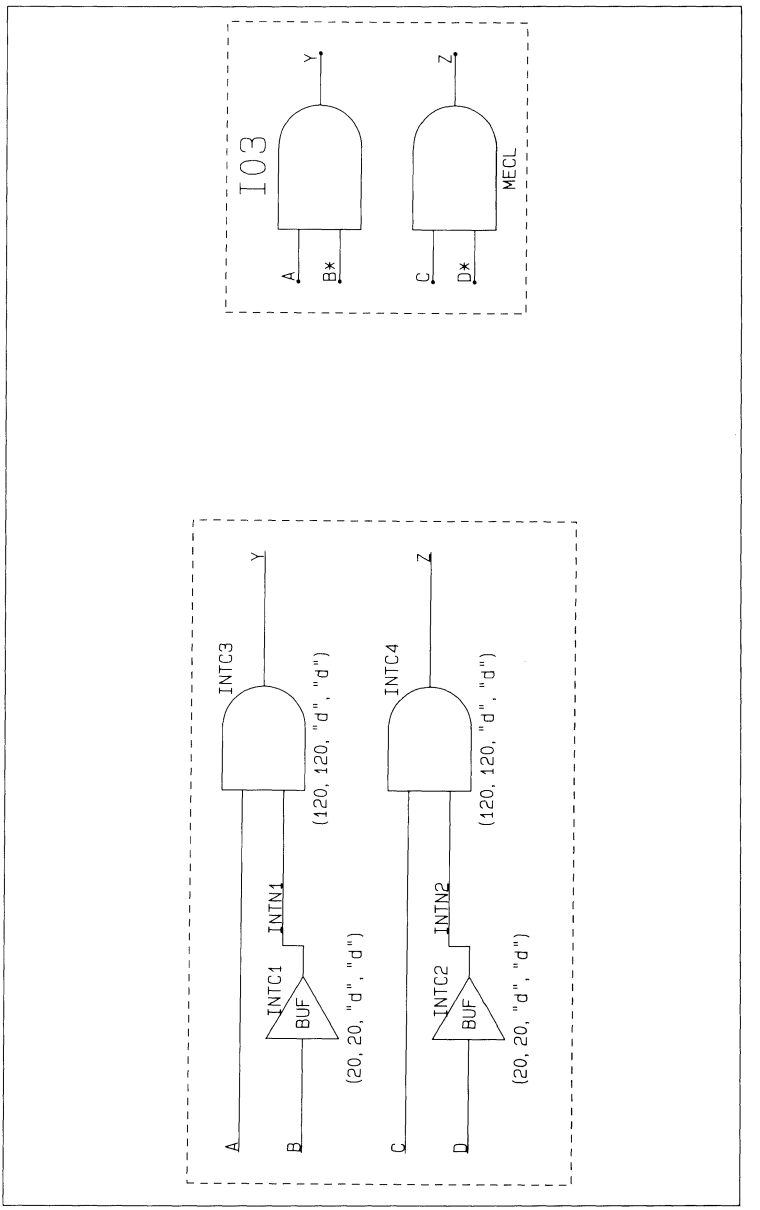
COMPONENT PLOTS

Plot 54



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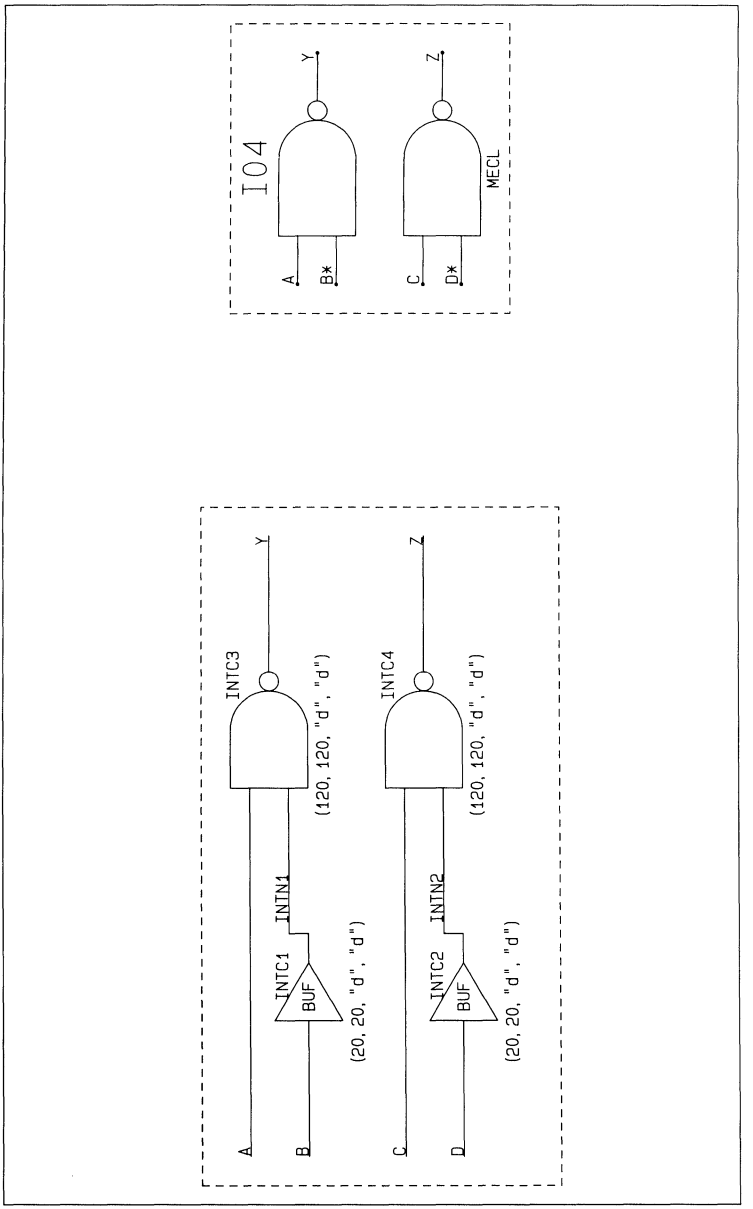
COMPONENT PLOTS

Plot 55



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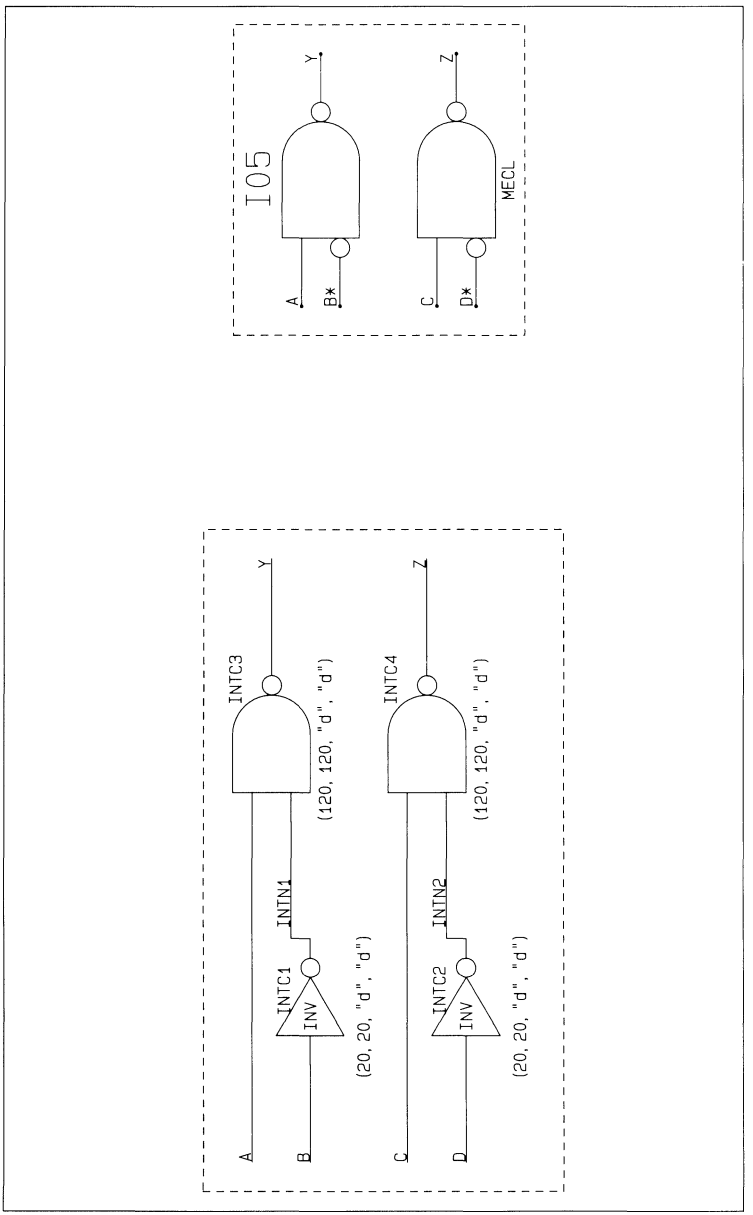
COMPONENT PLOTS

Plot 56



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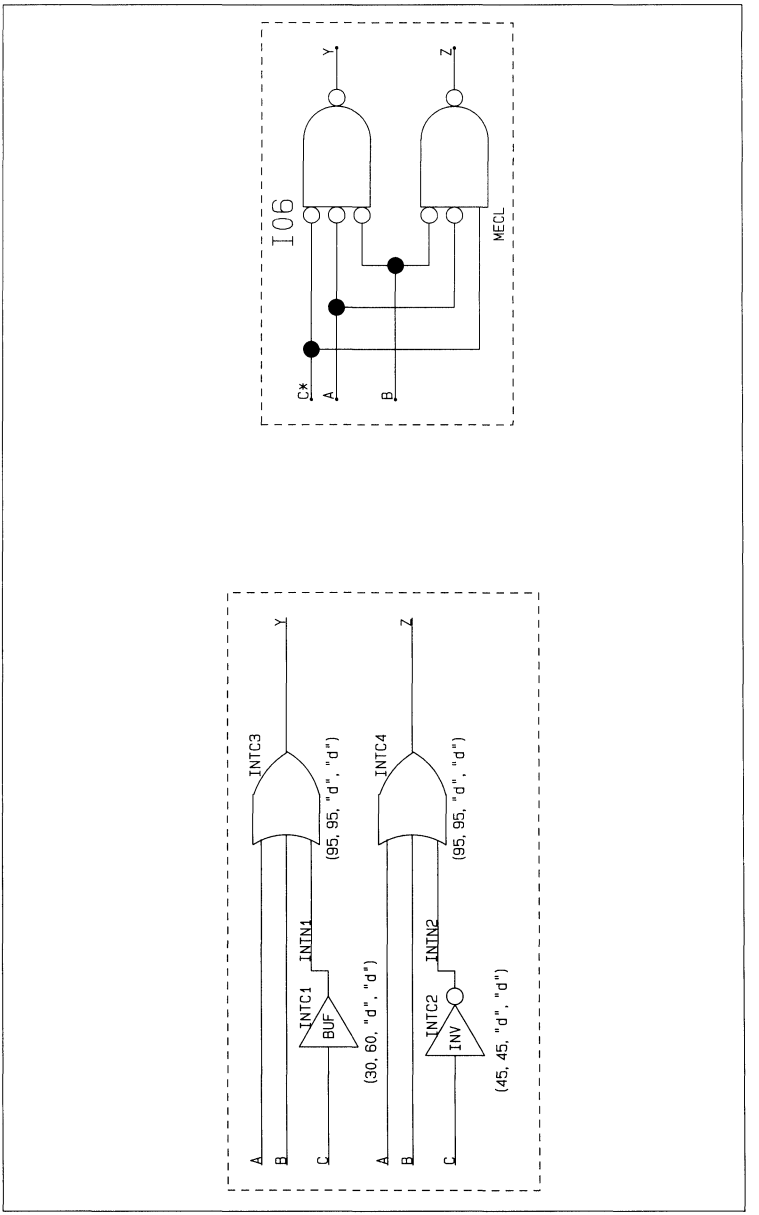
COMPONENT PLOTS

Plot 57



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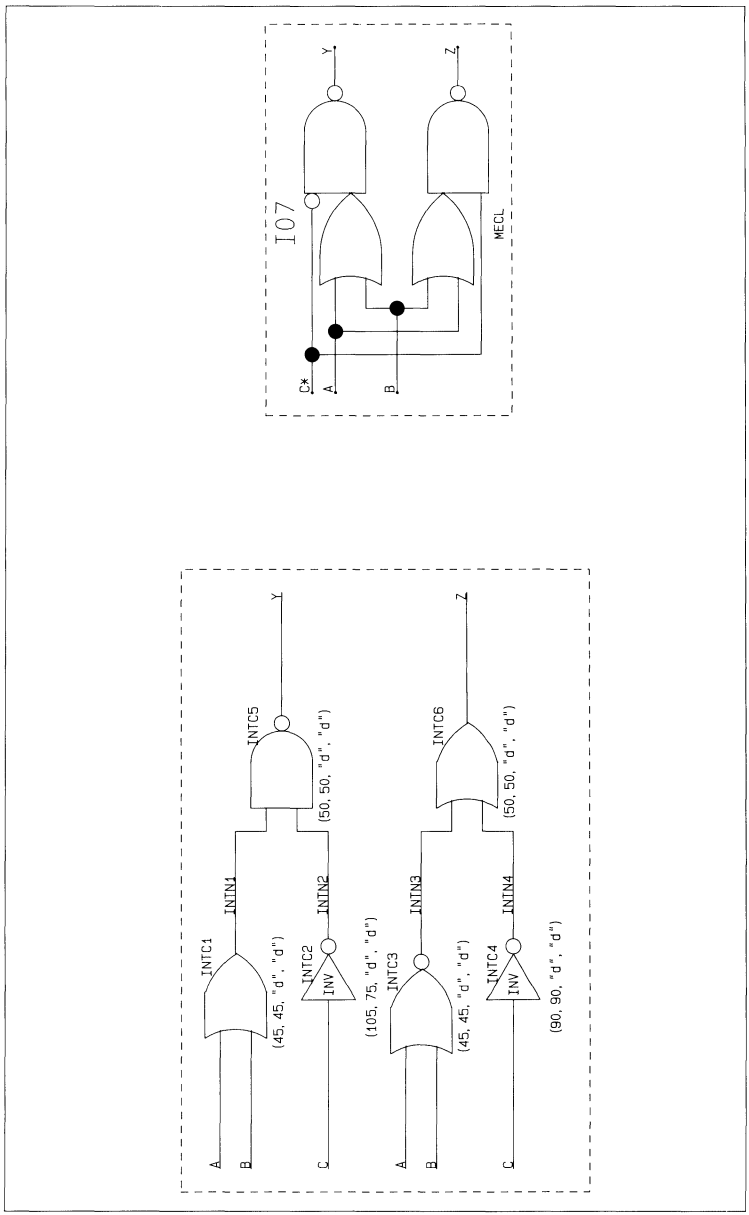
COMPONENT PLOTS

Plot 58



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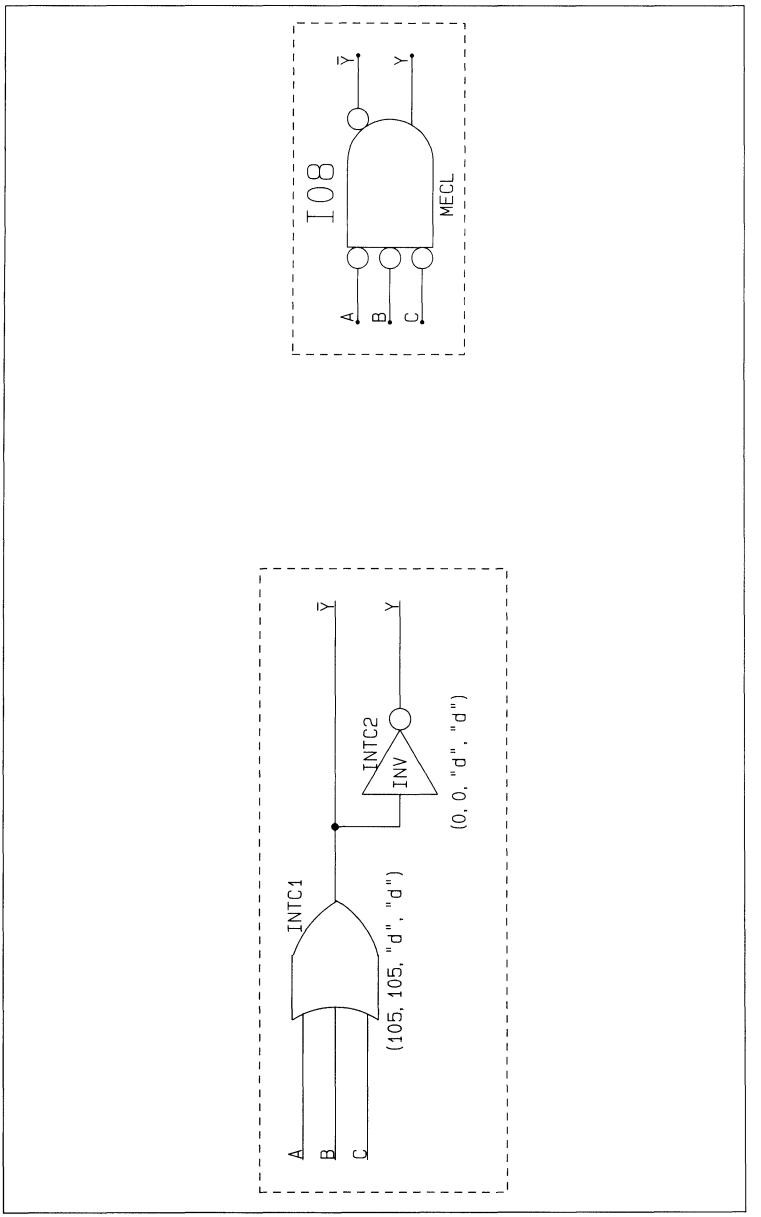
COMPONENT PLOTS

Plot 59



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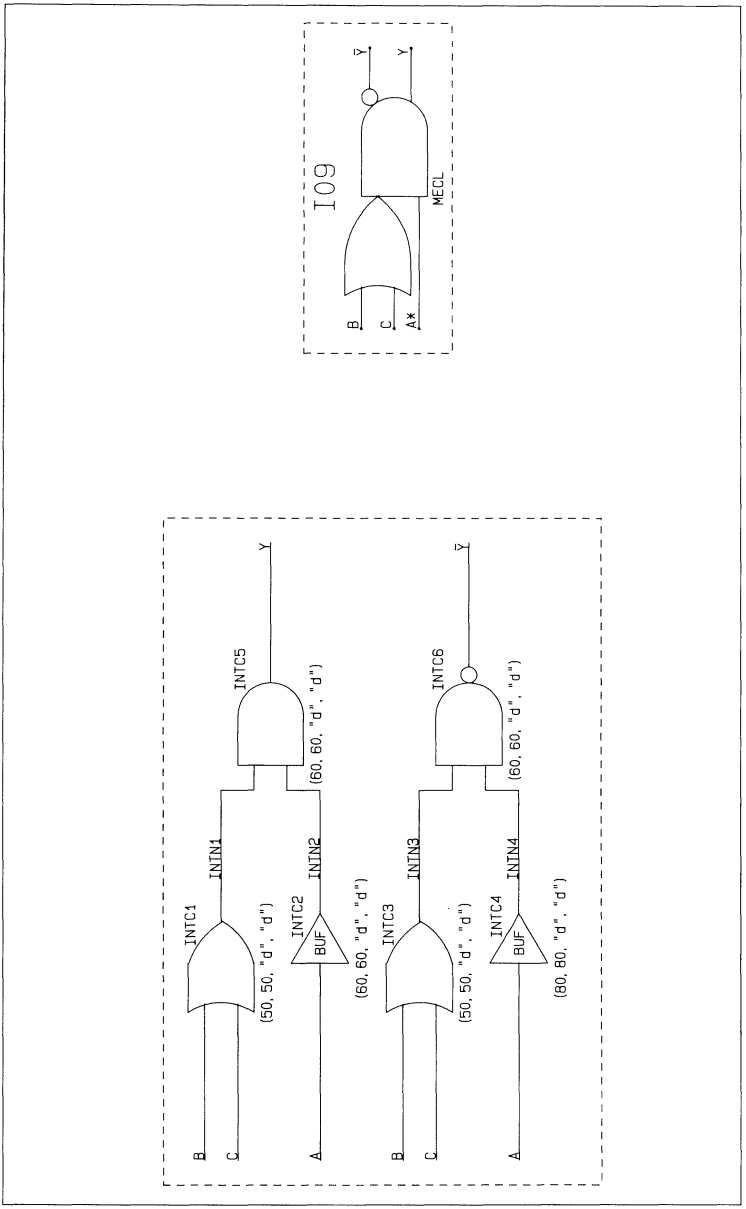
COMPONENT PLOTS

Plot 60



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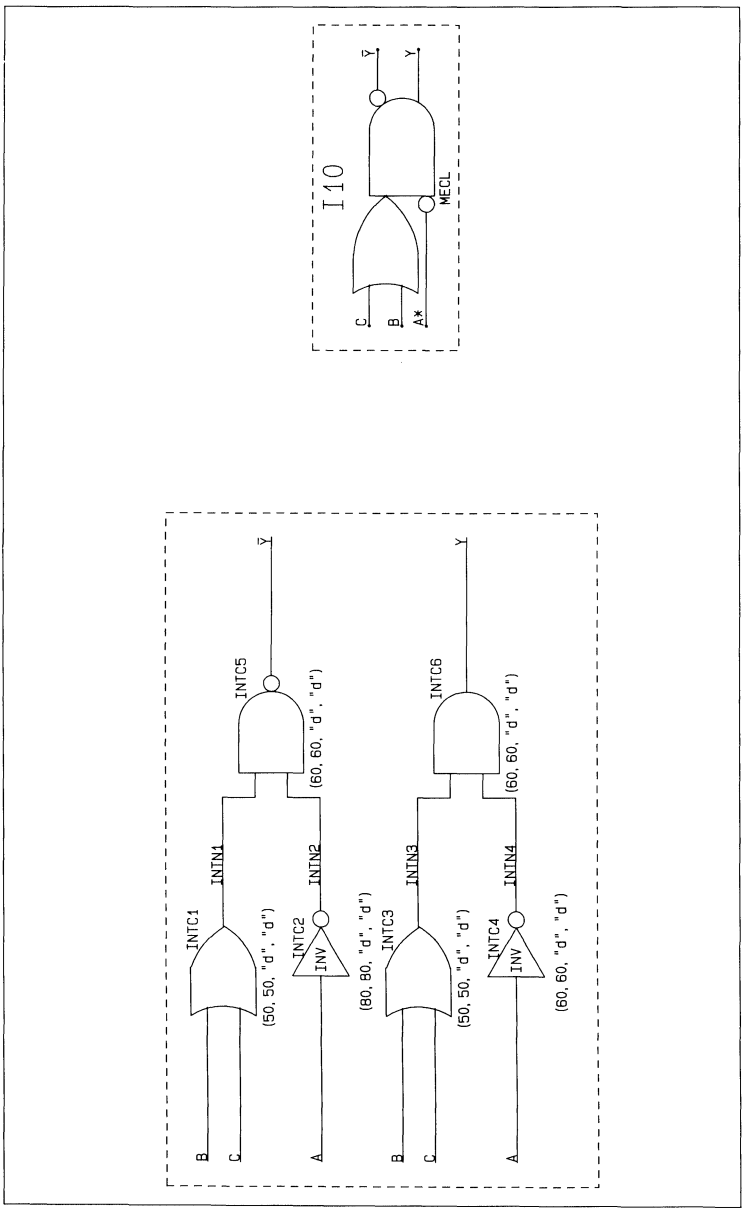
COMPONENT PLOTS

Plot 61



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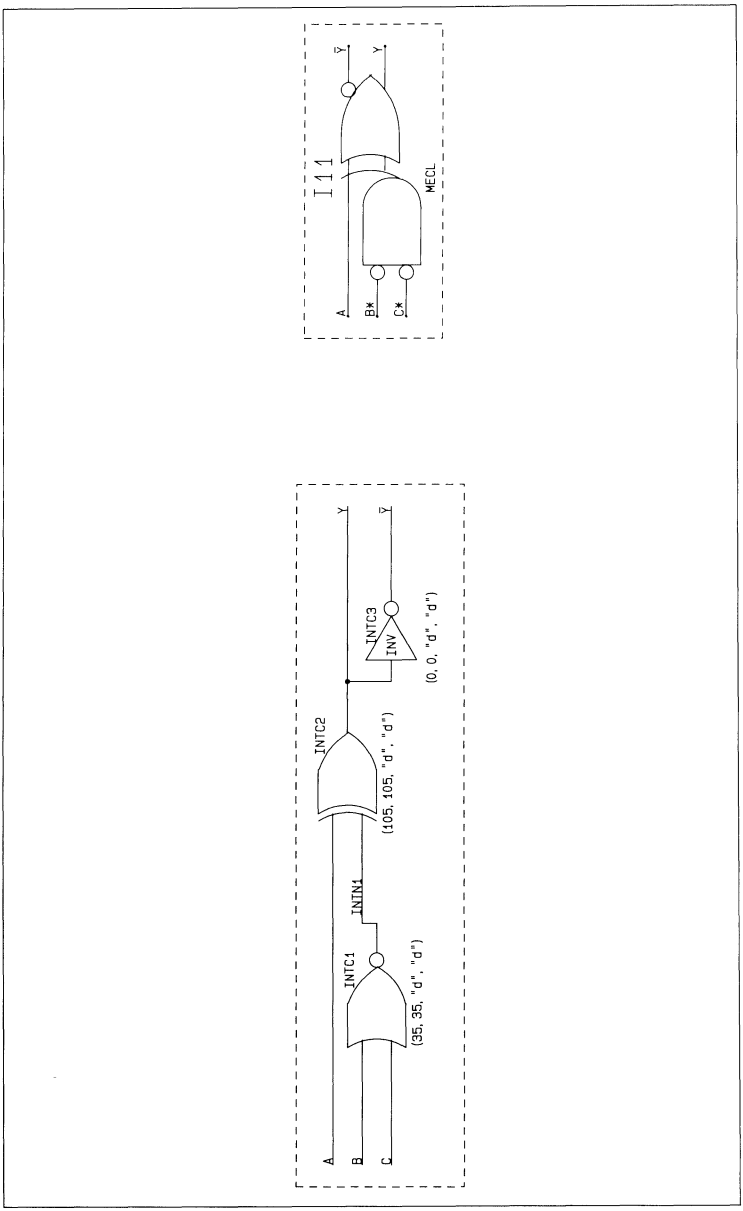
COMPONENT PLOTS

Plot 62



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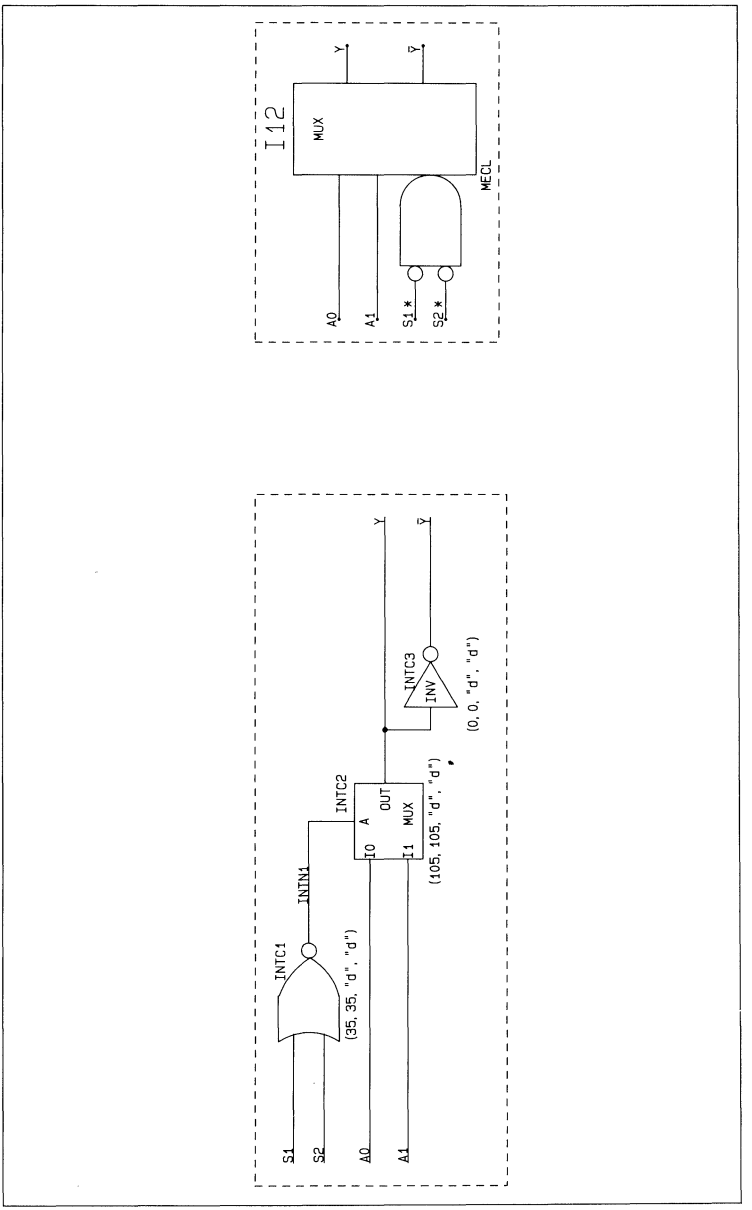
COMPONENT PLOTS

Plot 63



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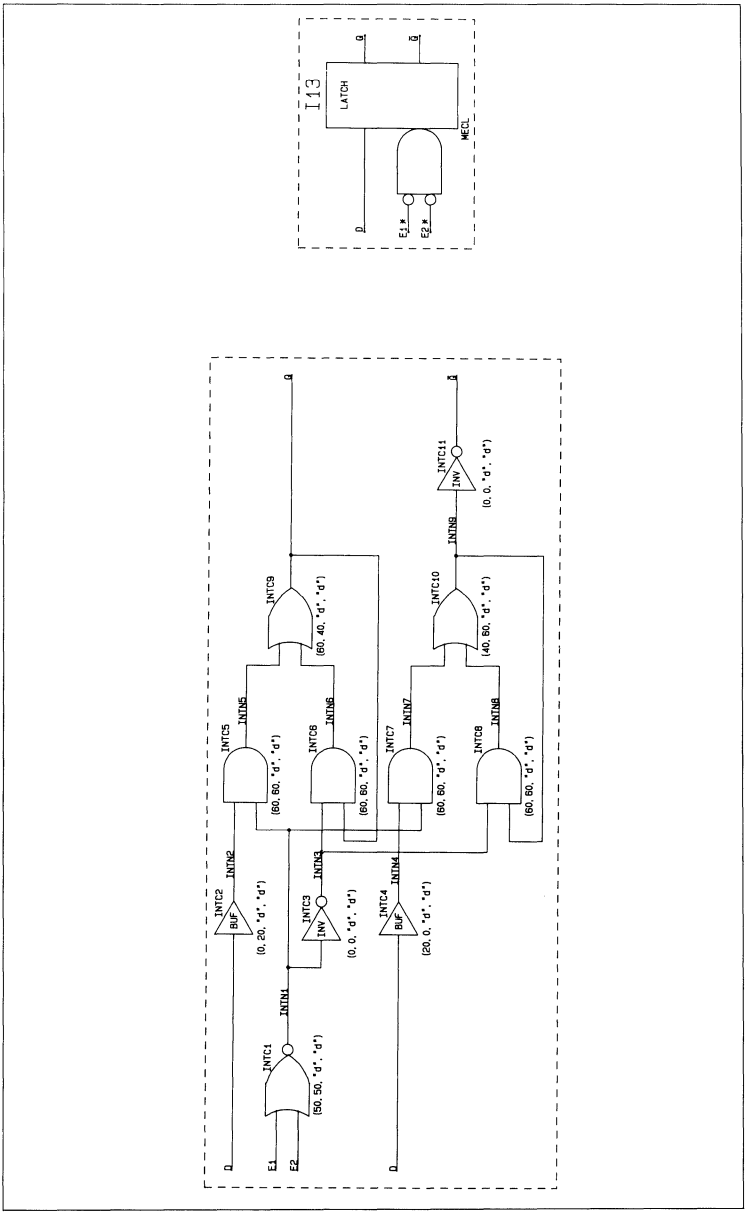
COMPONENT PLOTS

Plot 64



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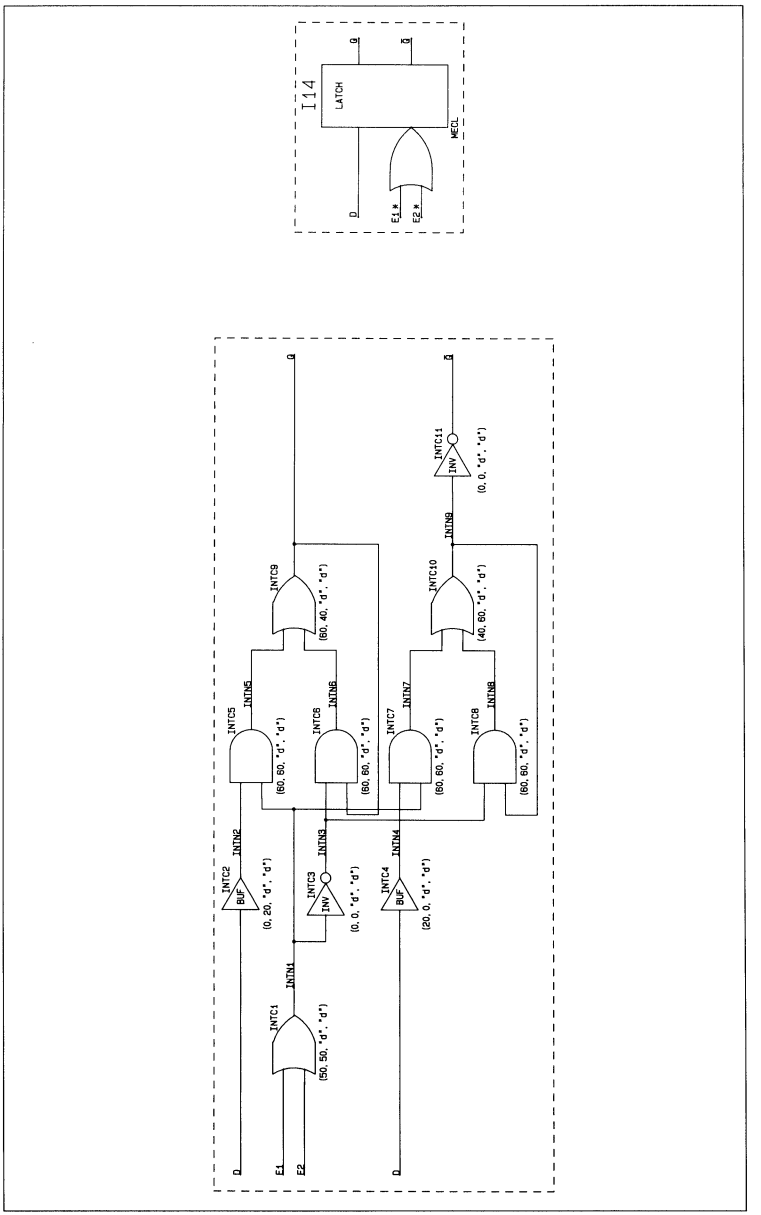
COMPONENT PLOTS

Plot 65



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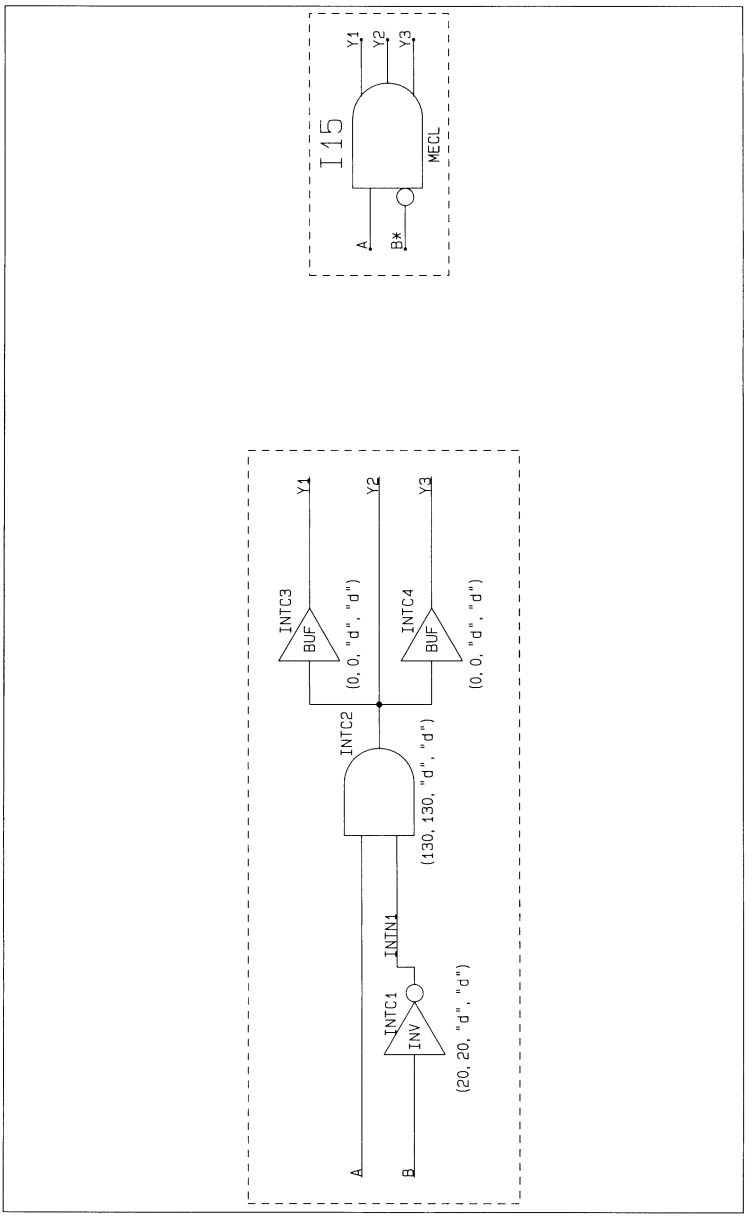
COMPONENT PLOTS

Plot 66



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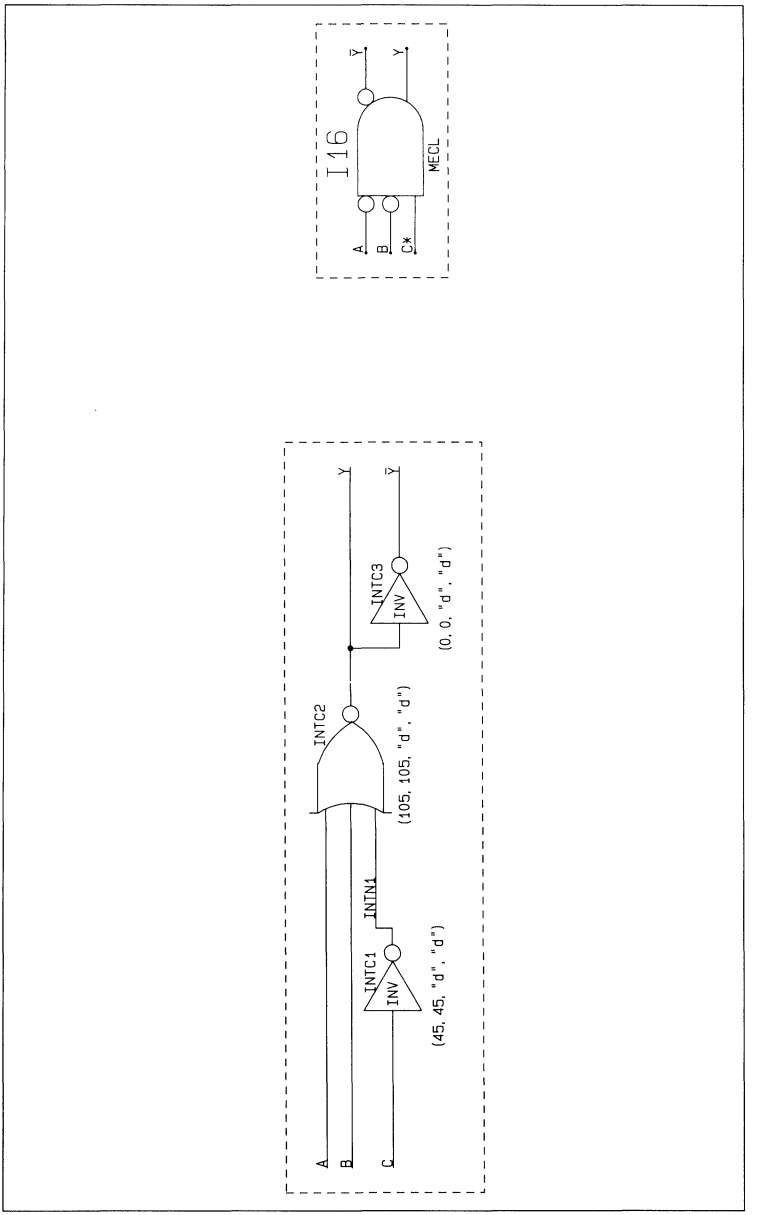
COMPONENT PLOTS

Plot 67



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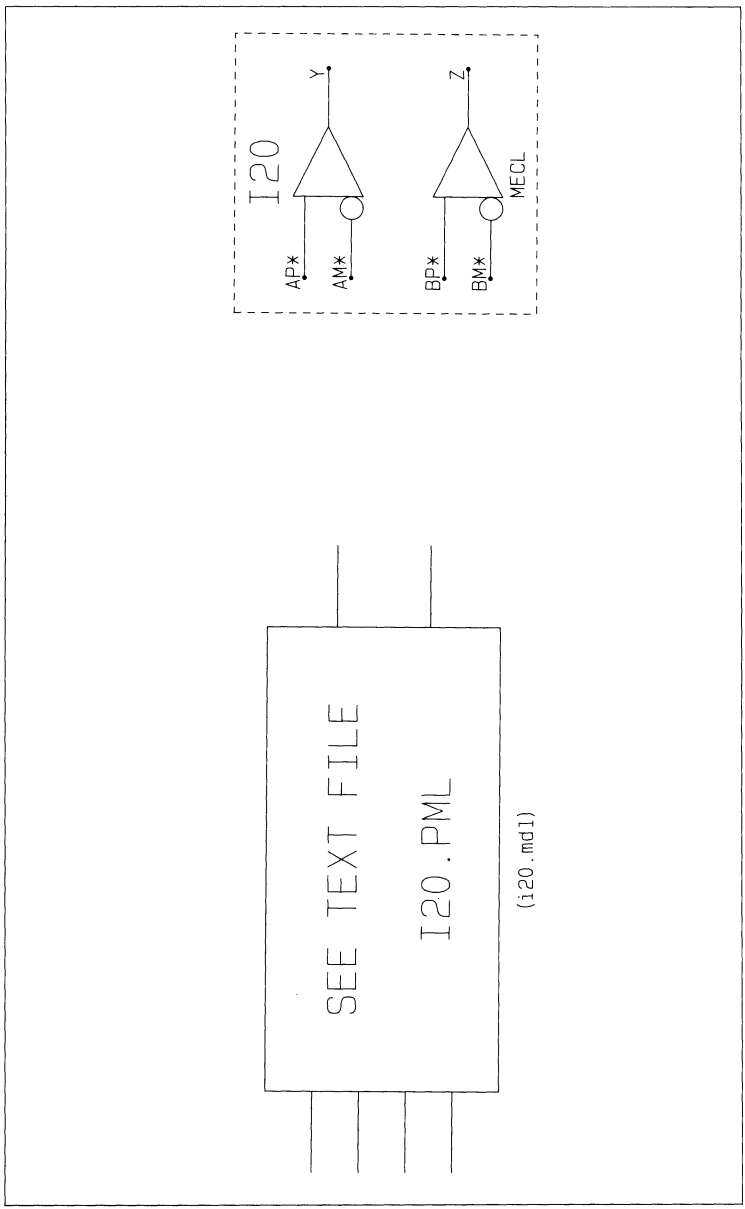
COMPONENT PLOTS

Plot 68



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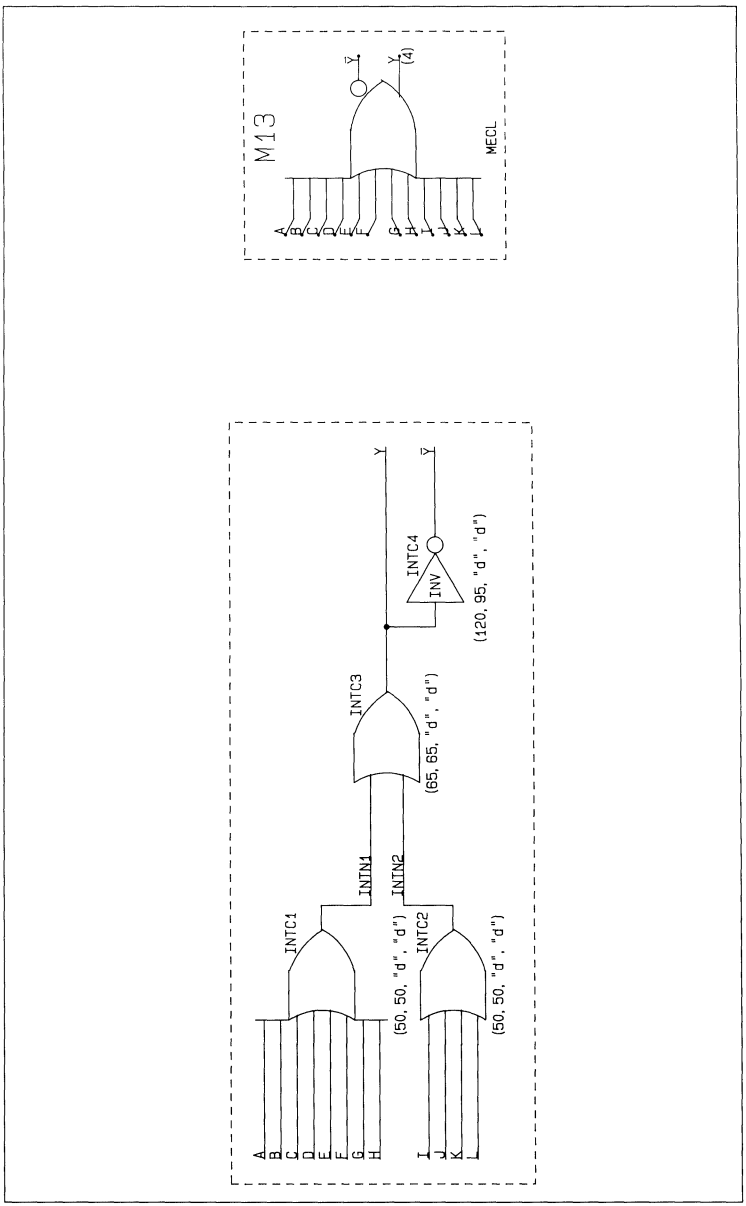
COMPONENT PLOTS

Plot 69



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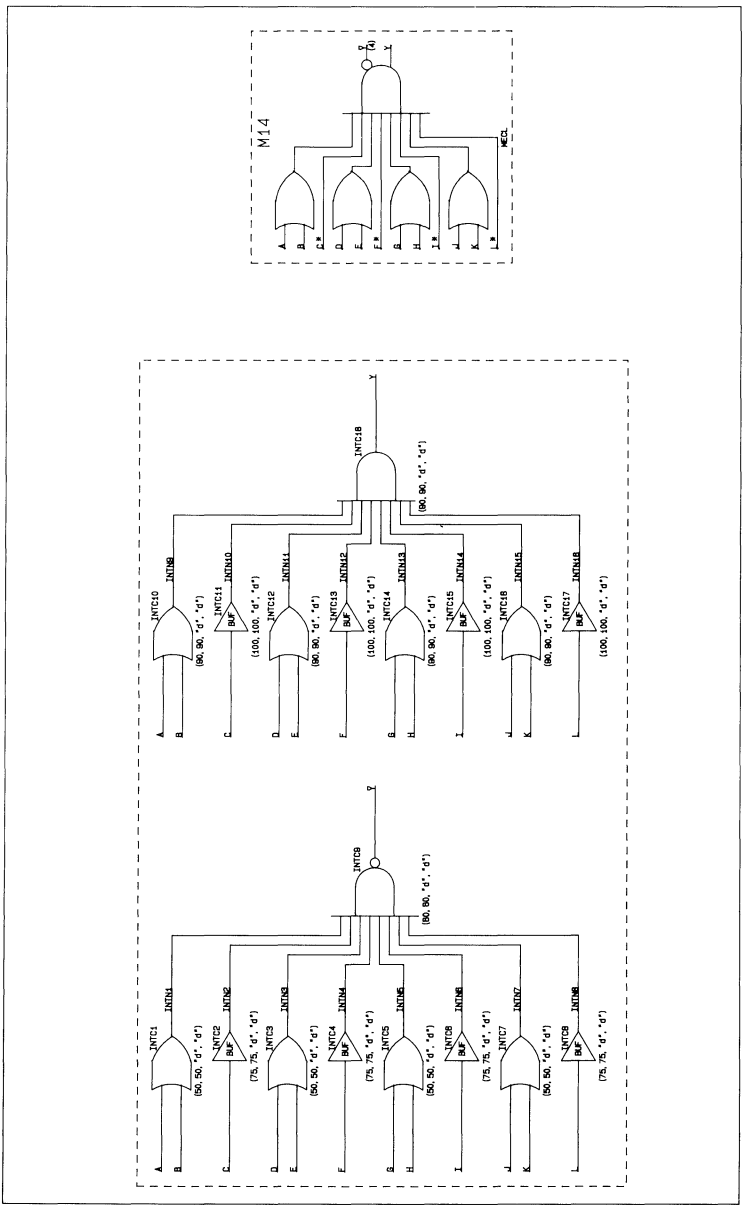
COMPONENT PLOTS

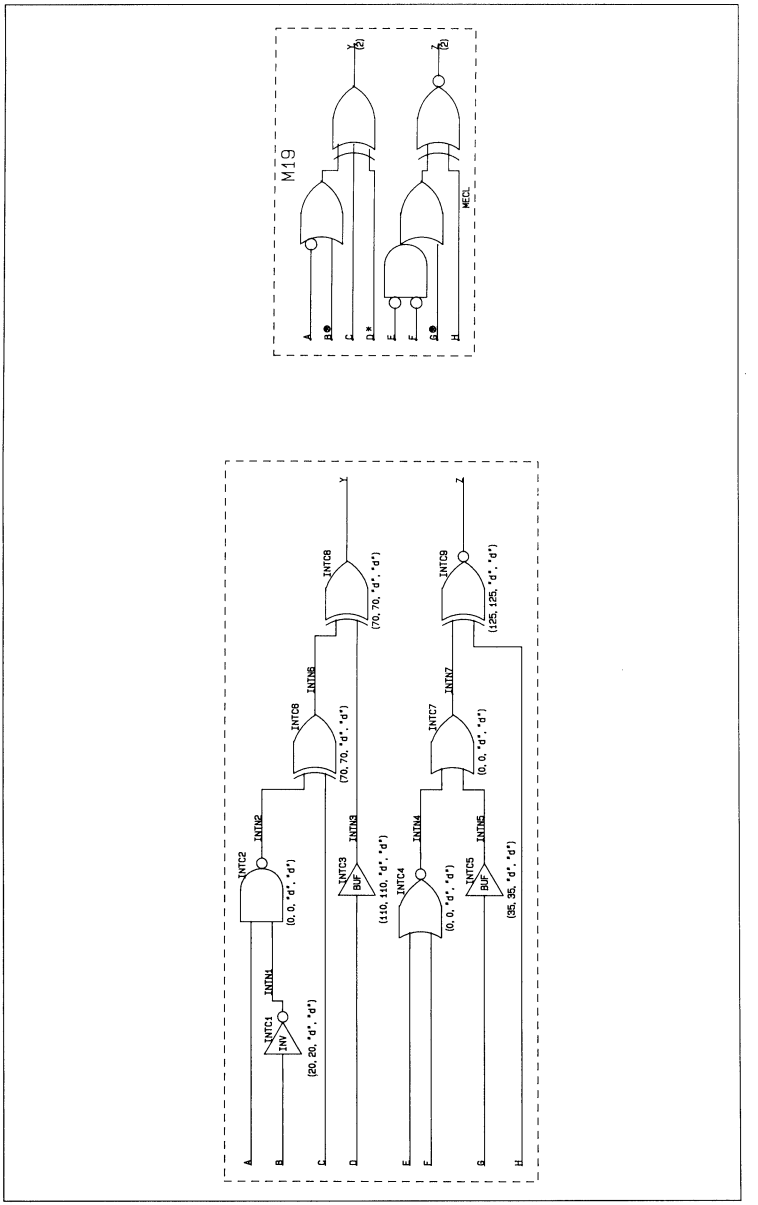
Plot 70



000-0145-00

COMPONENT PLOTS

Plot 71



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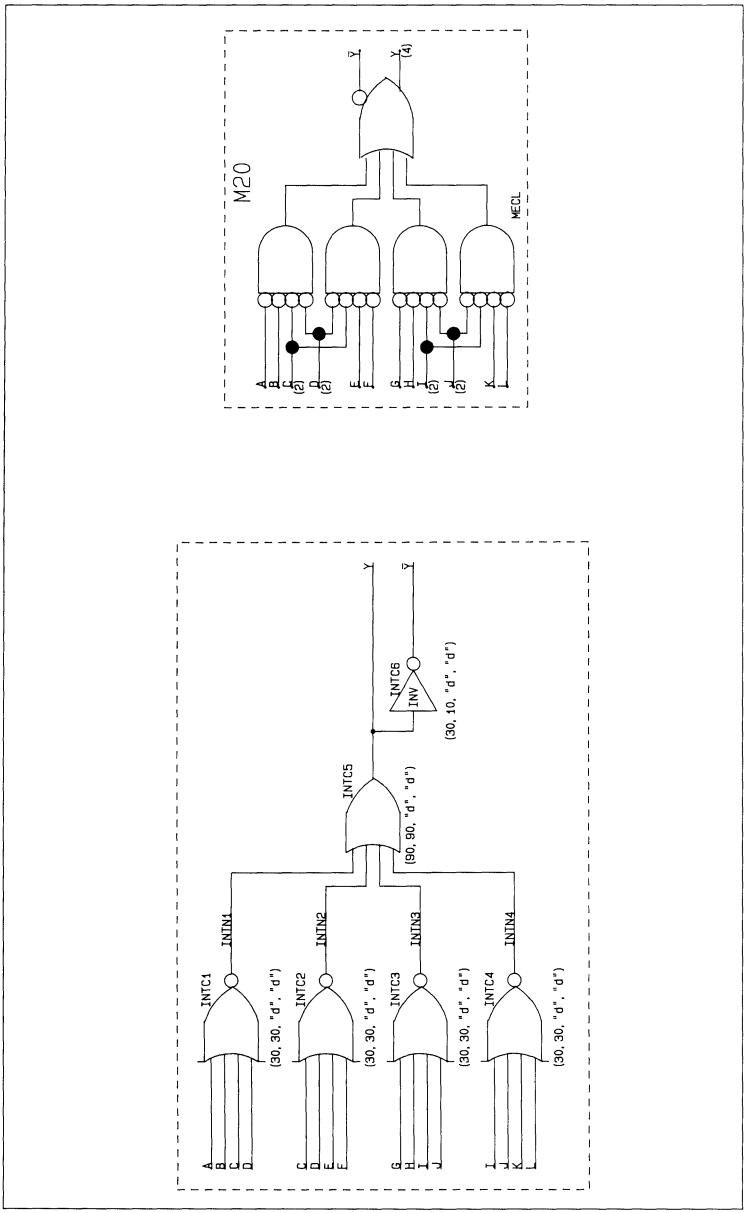
COMPONENT PLOTS

Plot 72



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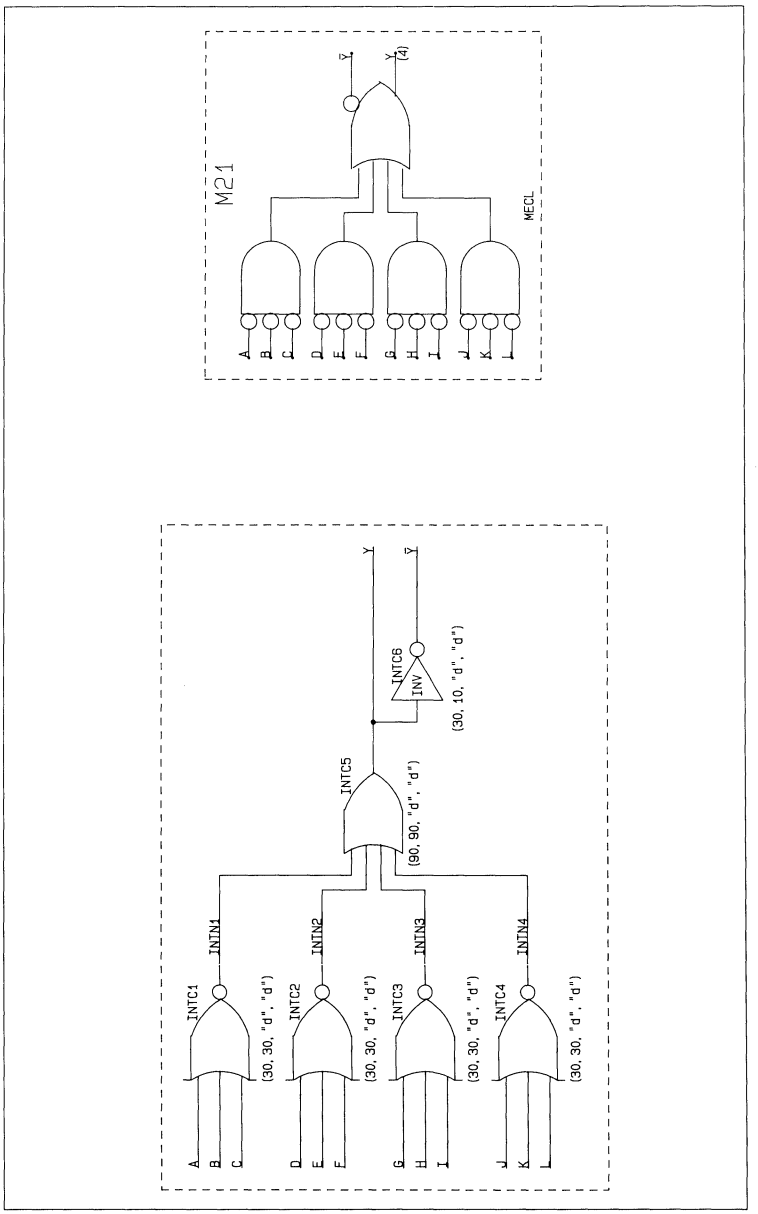
COMPONENT PLOTS

Plot 73



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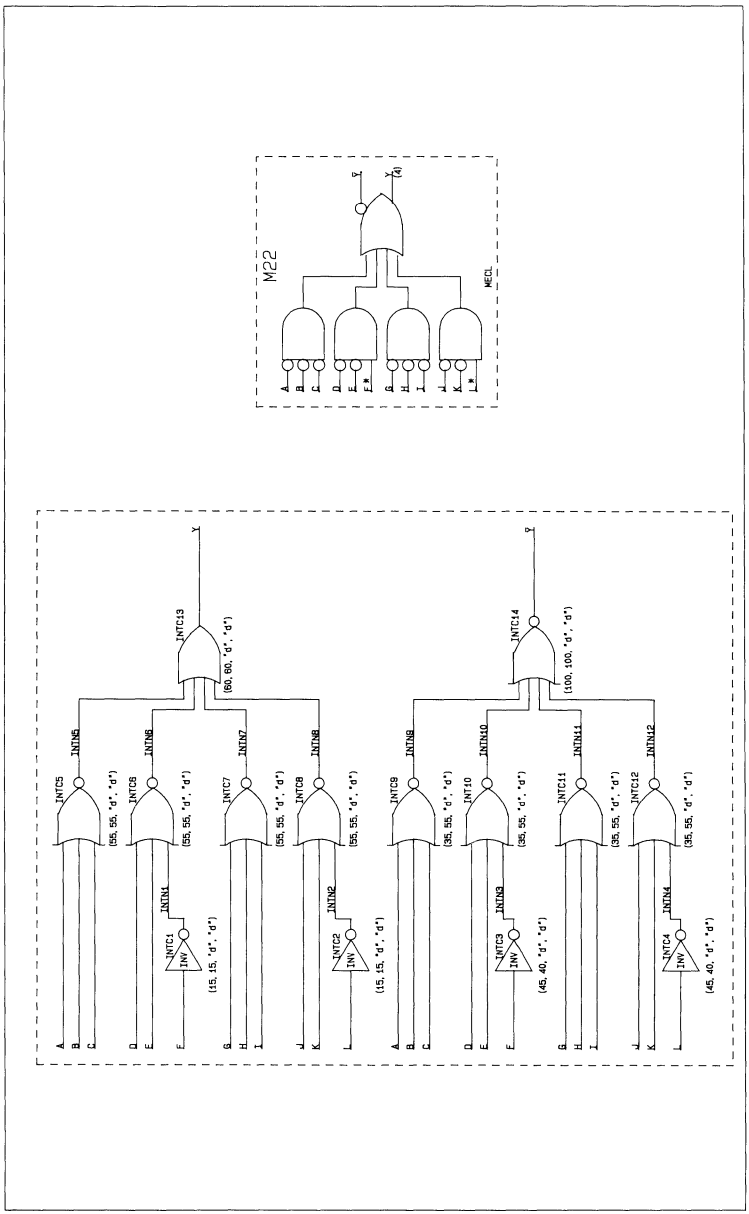
COMPONENT PLOTS

Plot 74



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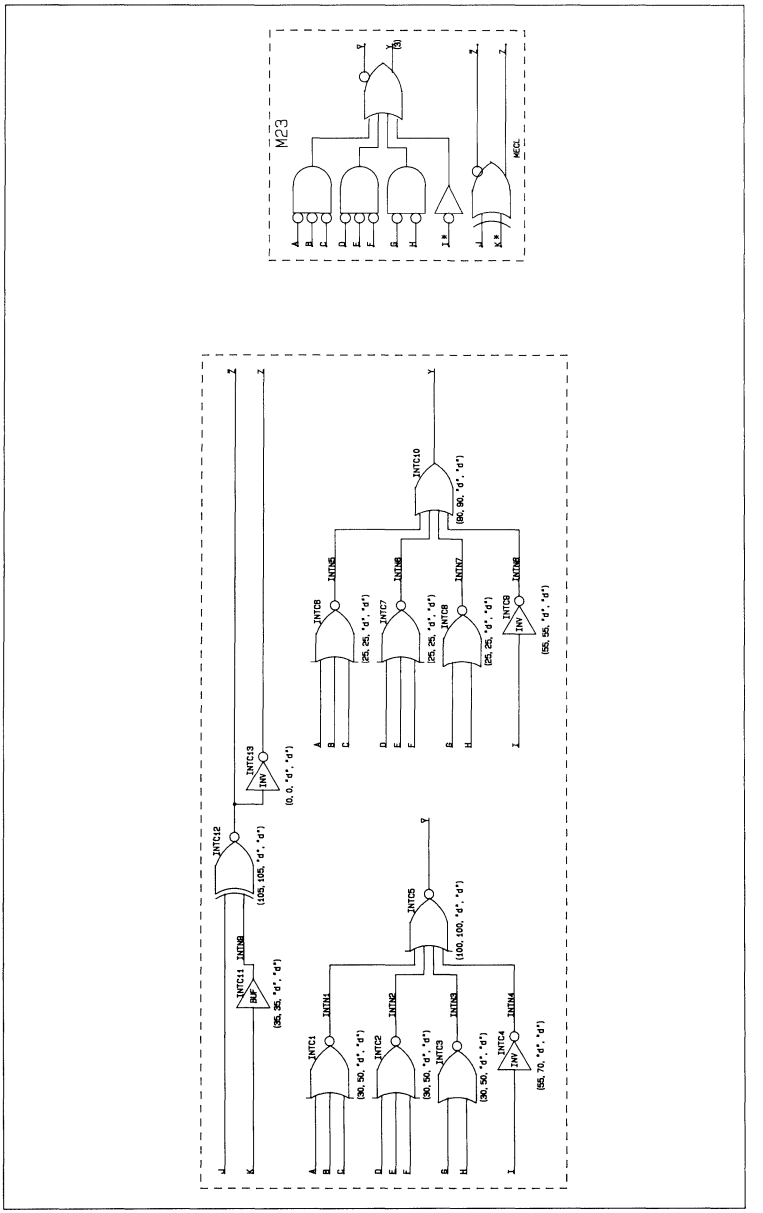
COMPONENT PLOTS

Plot 75



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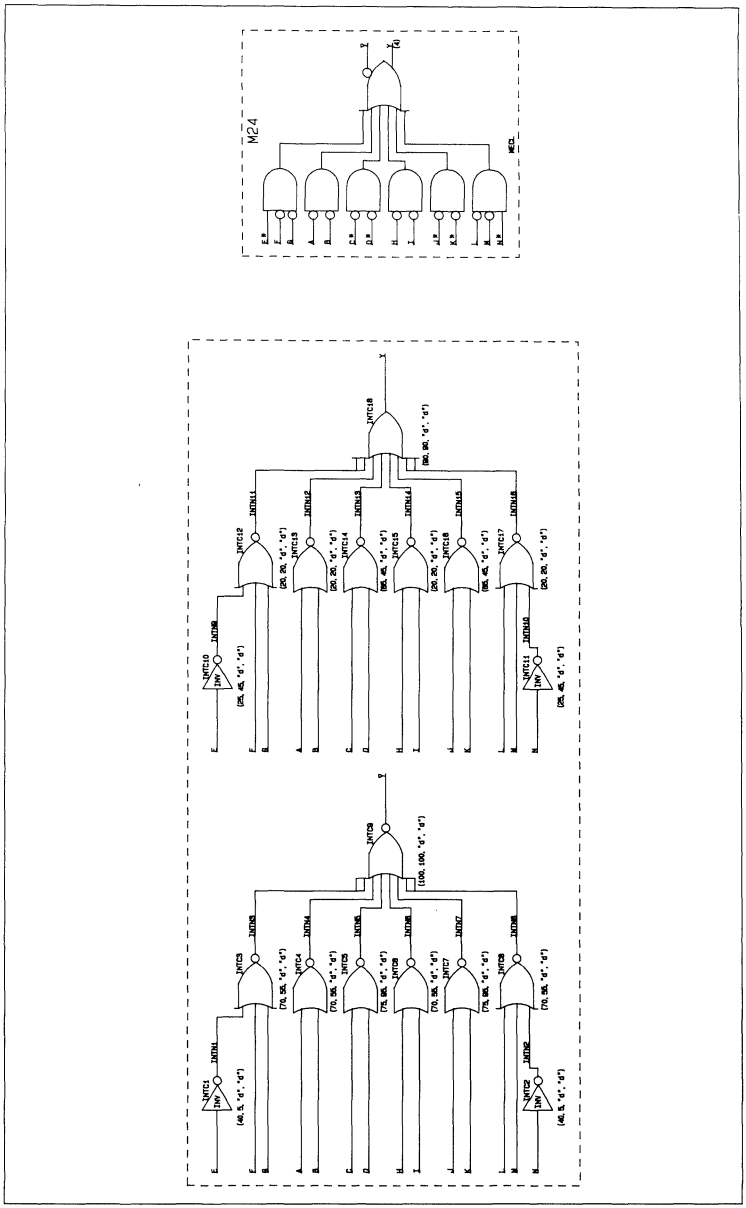
COMPONENT PLOTS

Plot 76



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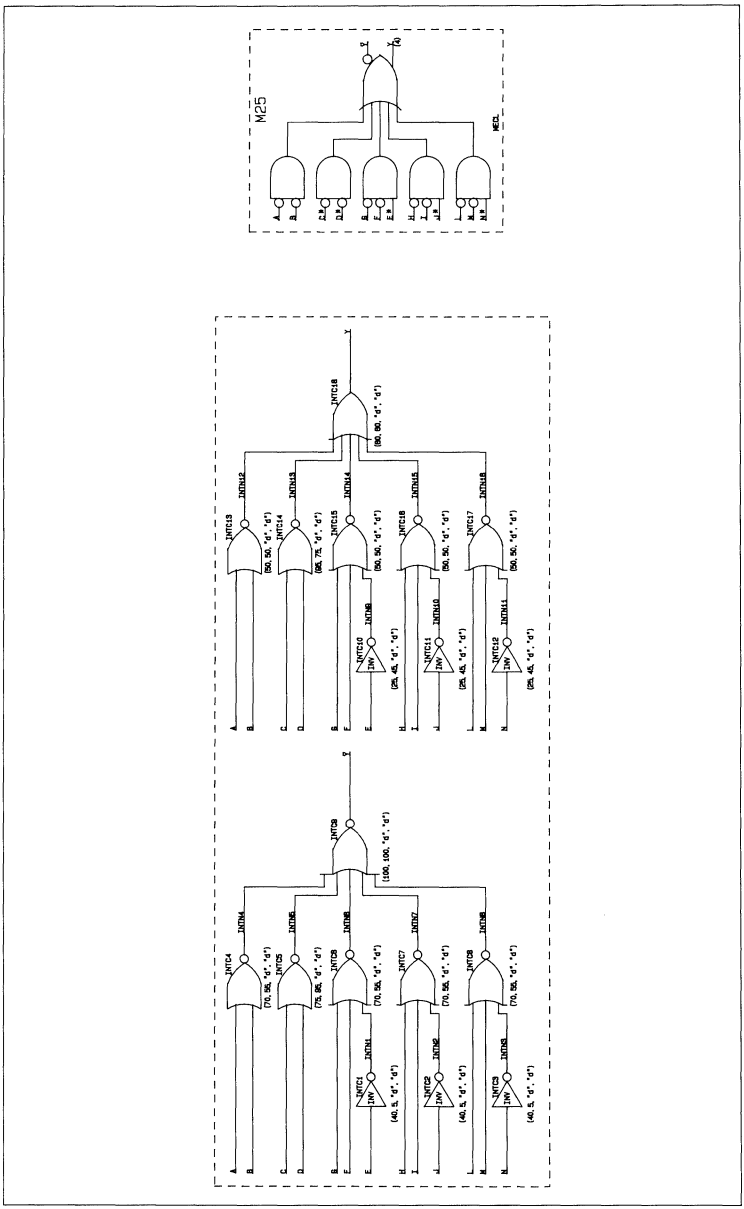
COMPONENT PLOTS

Plot 77



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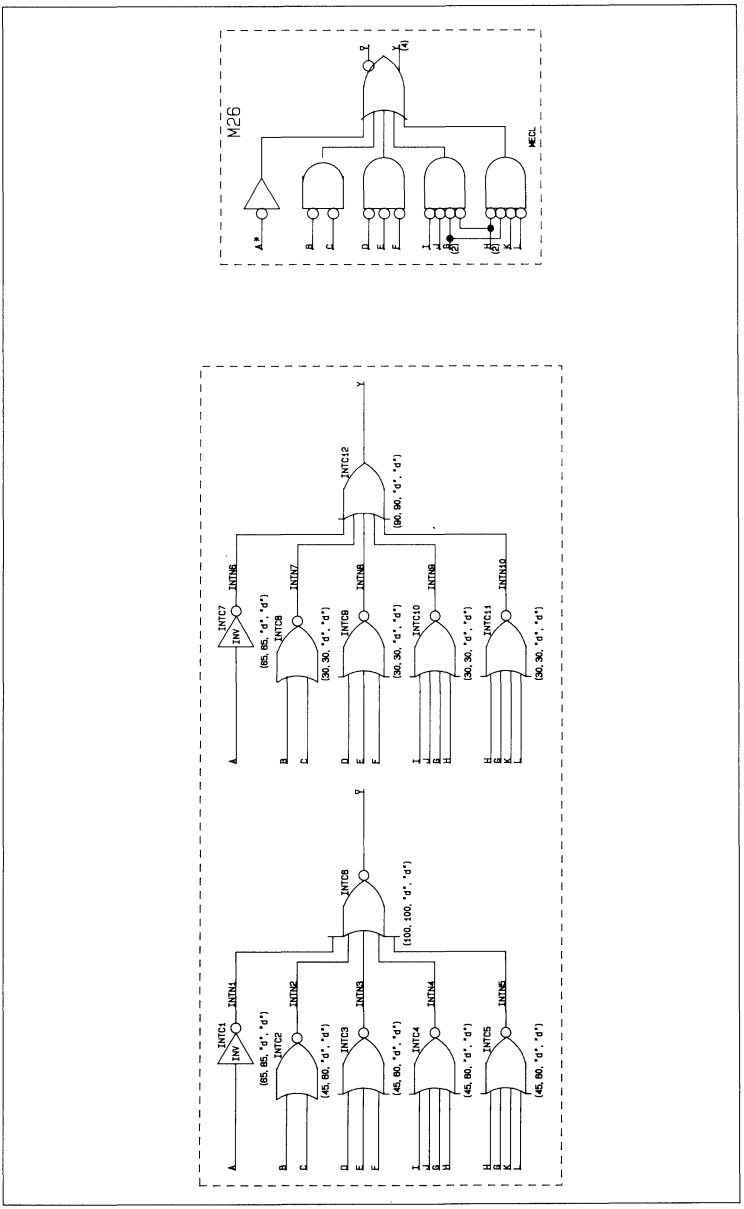
COMPONENT PLOTS

Plot 78



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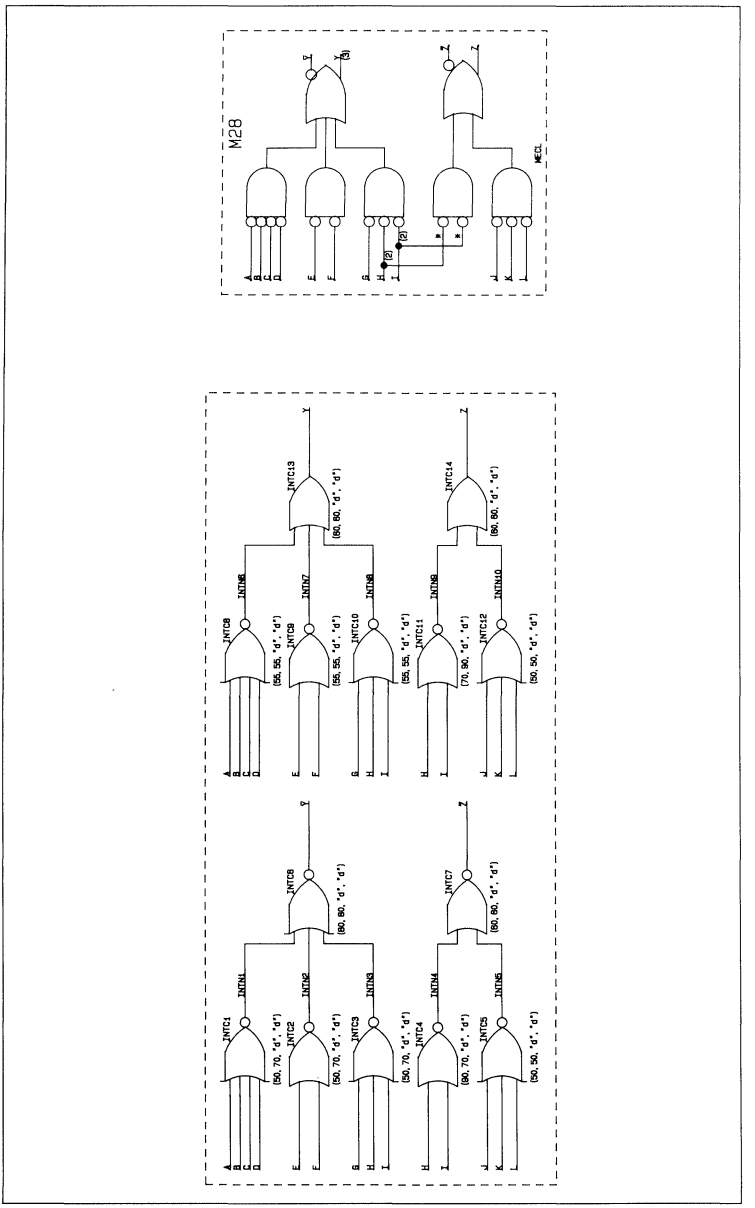
COMPONENT PLOTS

Plot 79



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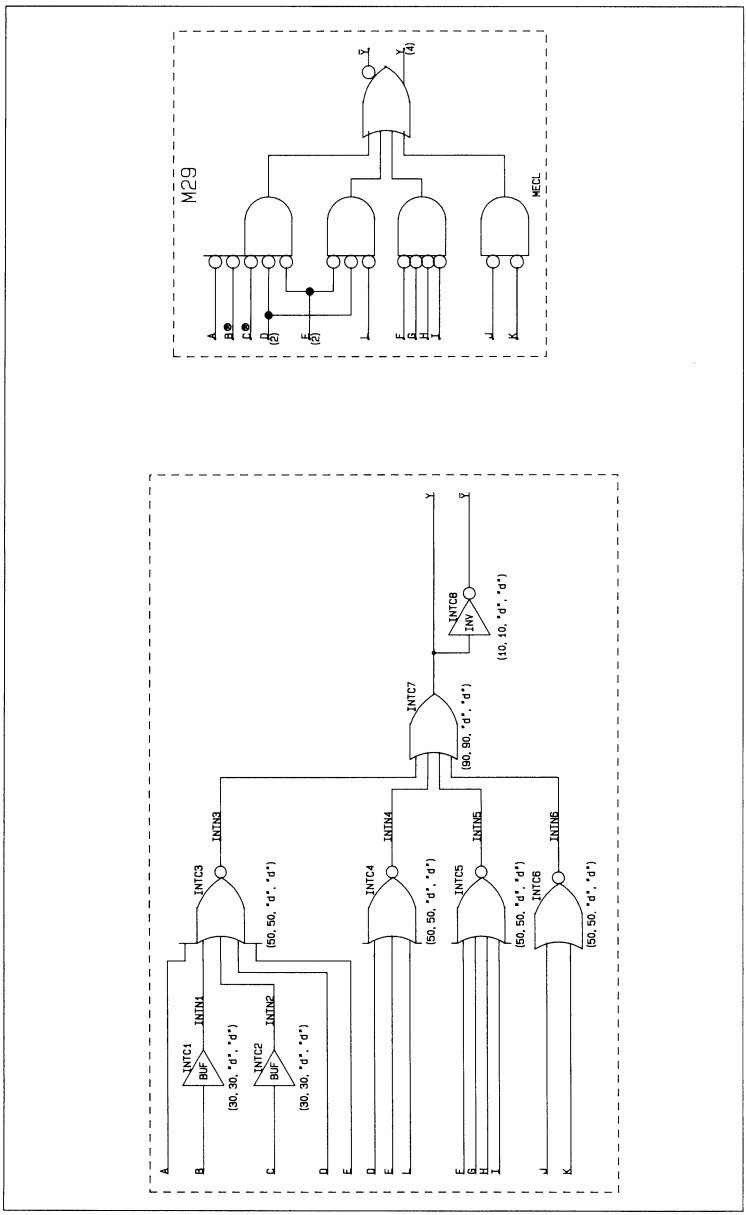
COMPONENT PLOTS

Plot 80



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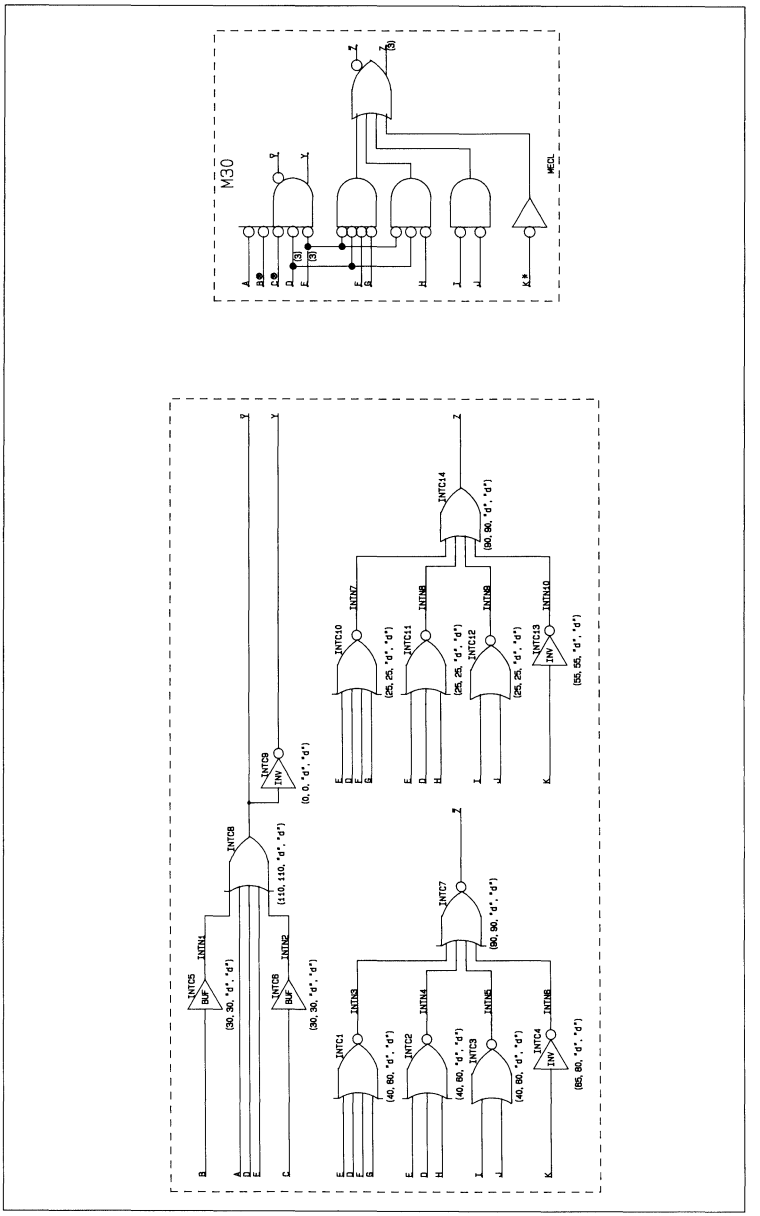
COMPONENT PLOTS

Plot 81



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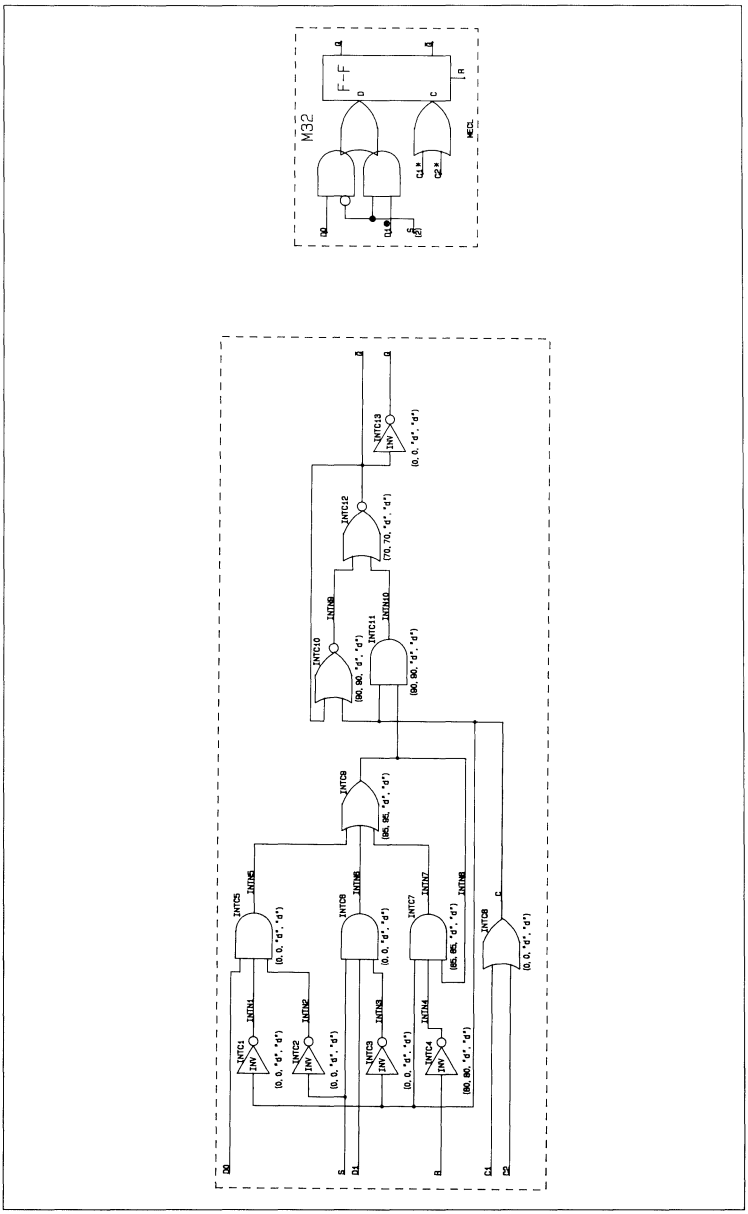
COMPONENT PLOTS

Plot 82



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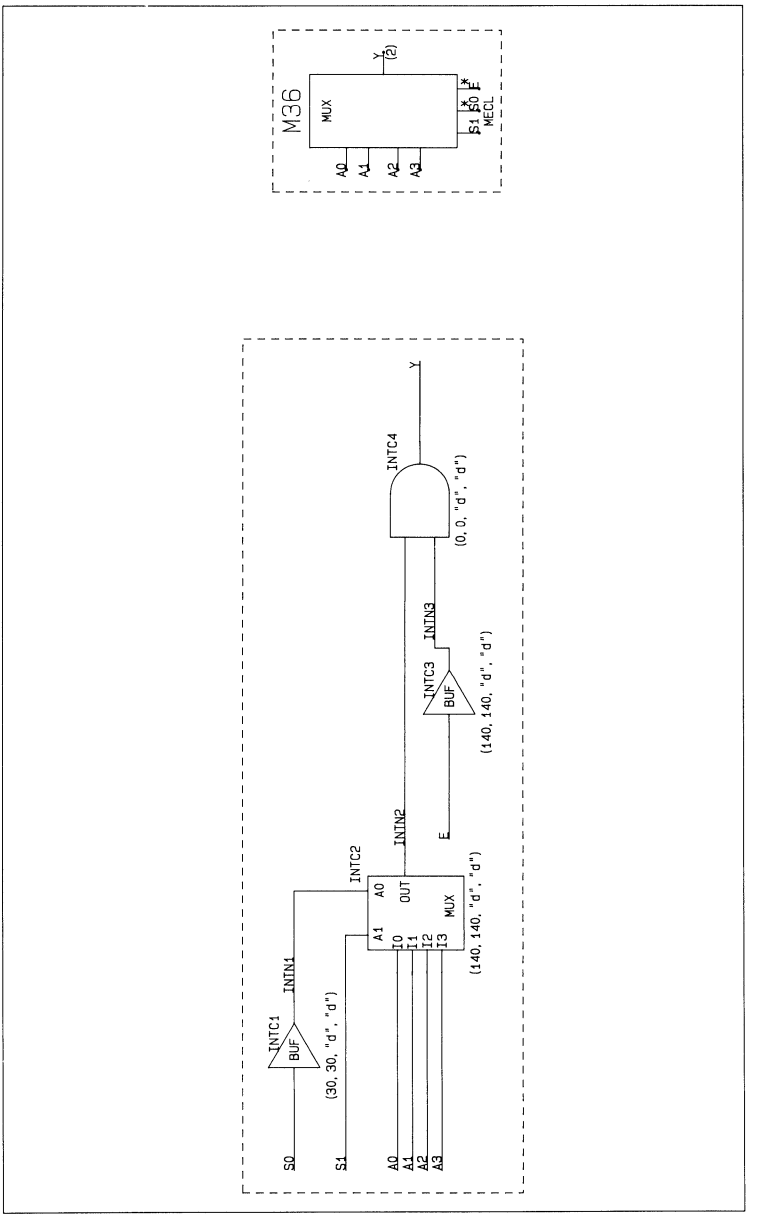
COMPONENT PLOTS

Plot 83



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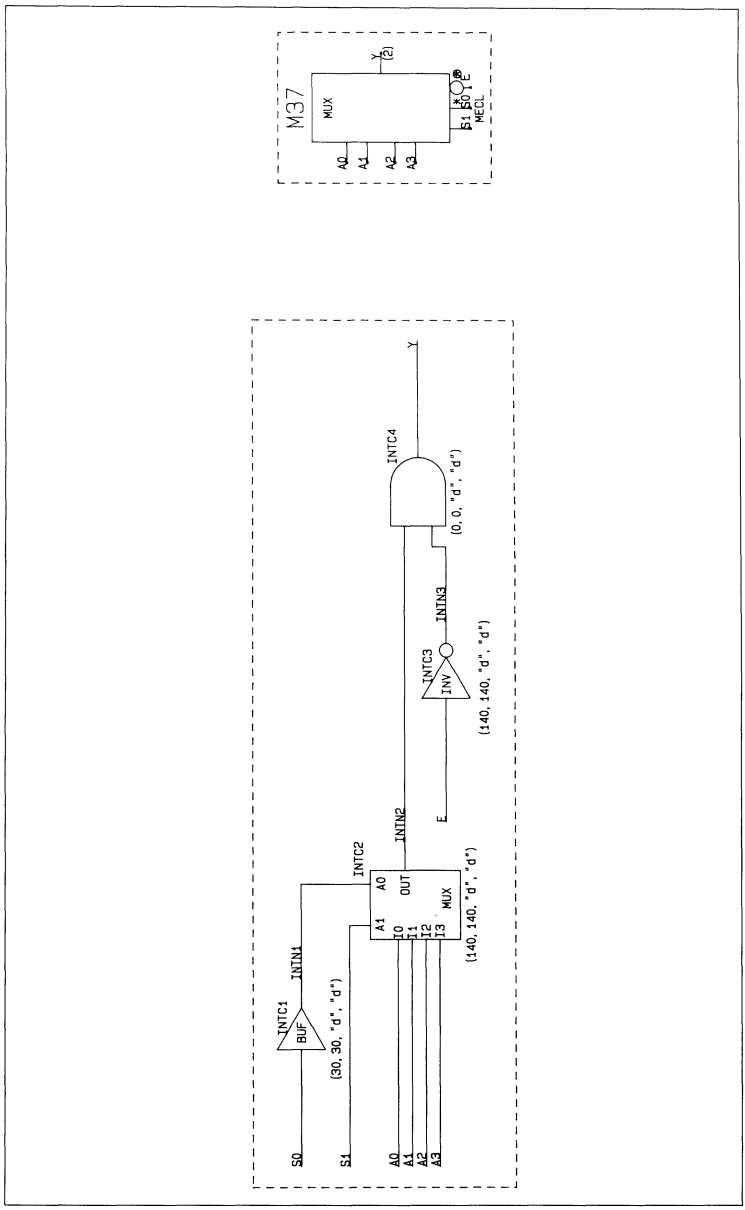
COMPONENT PLOTS

Plot 84



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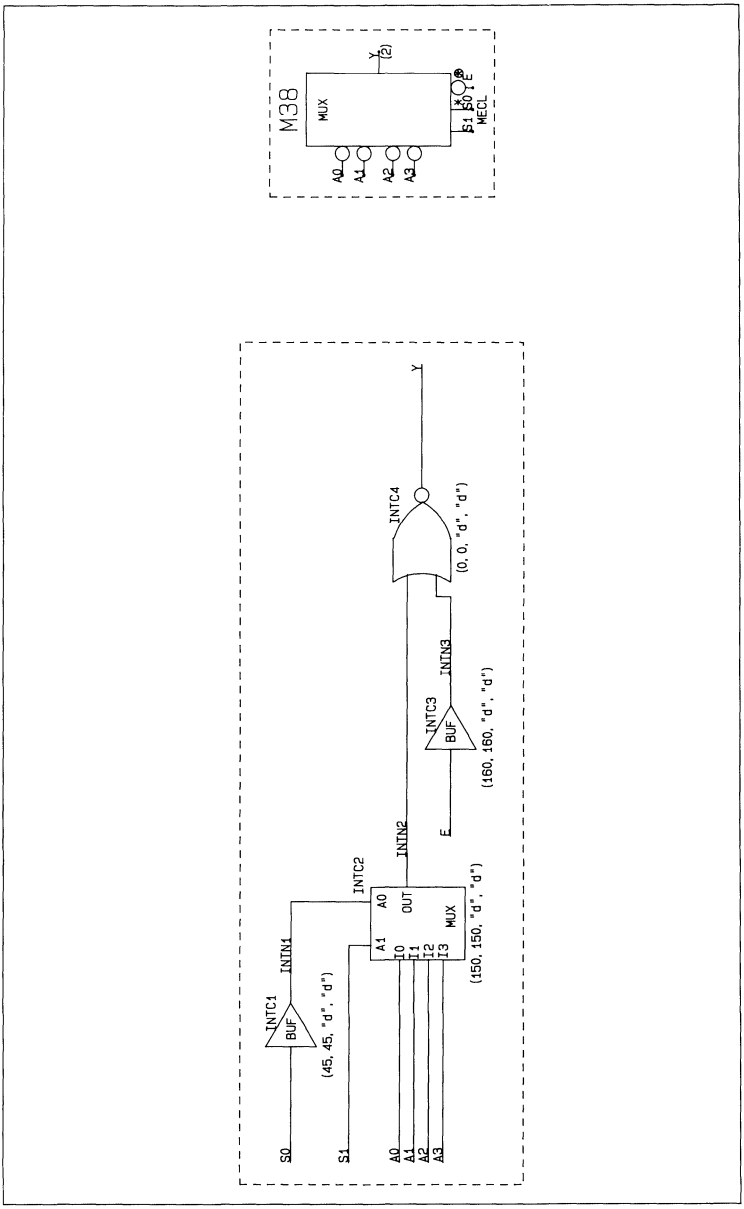
COMPONENT PLOTS

Plot 85



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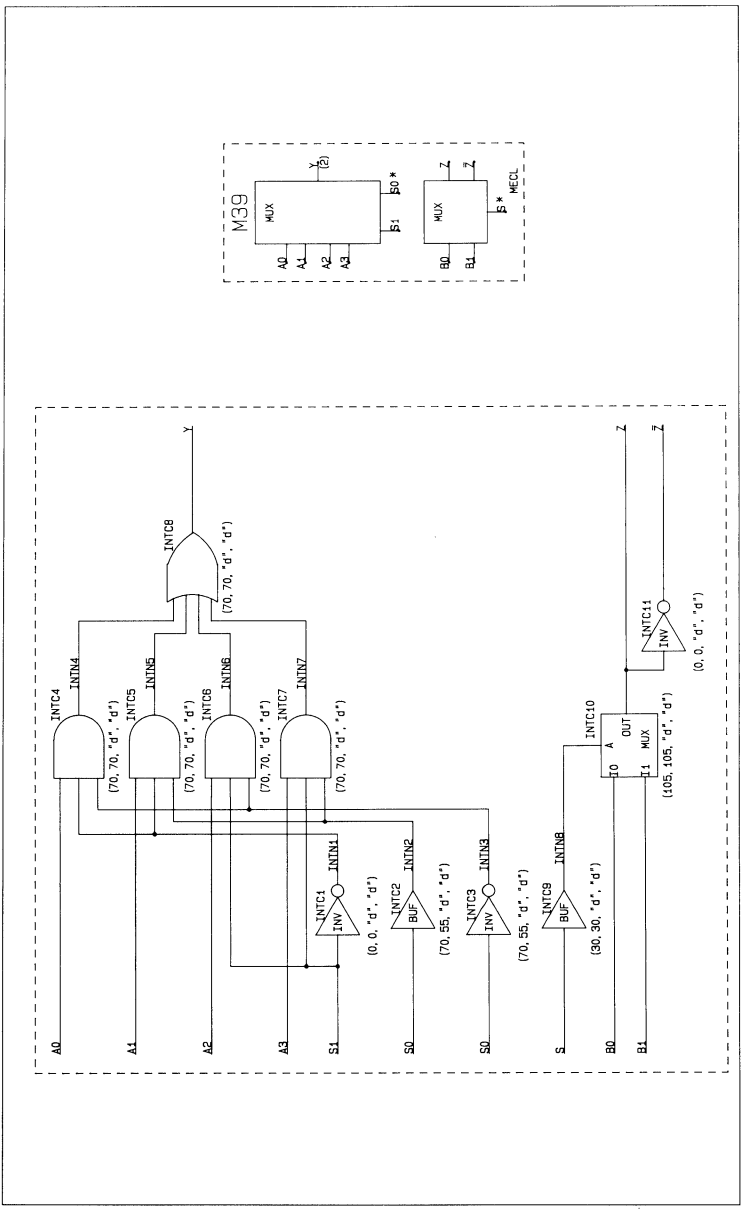
COMPONENT PLOTS

Plot 86



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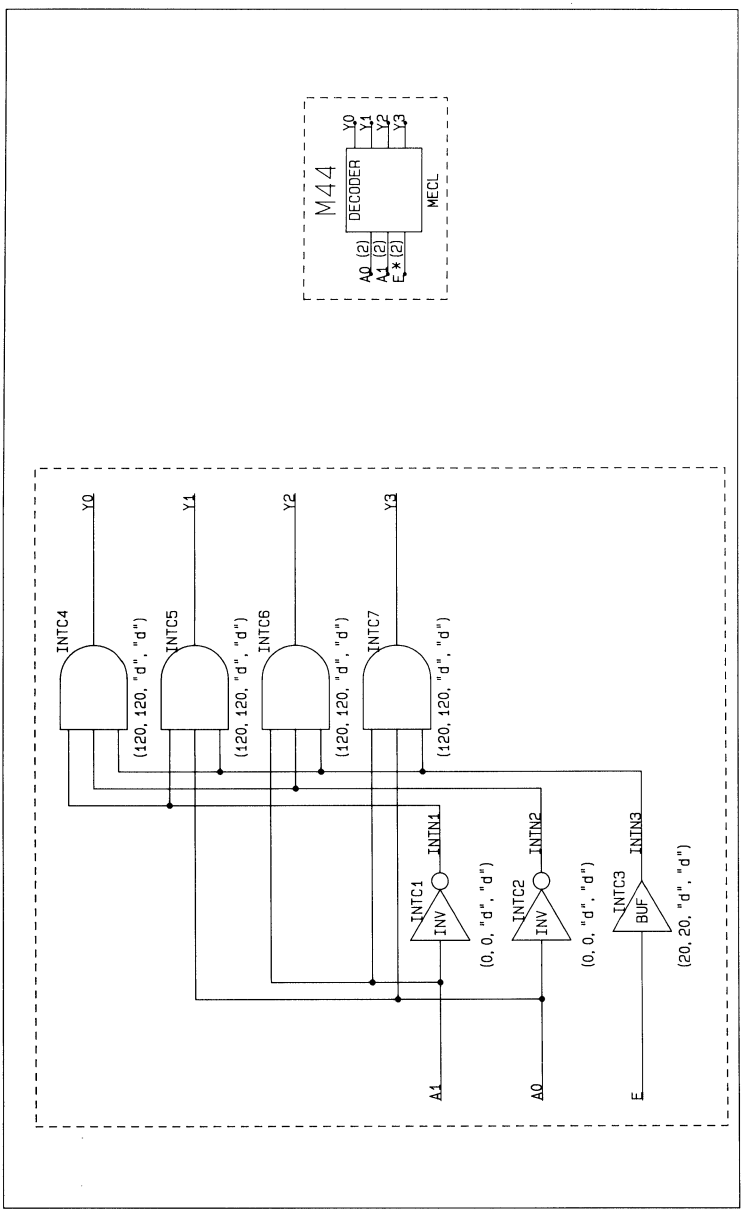
COMPONENT PLOTS

Plot 87



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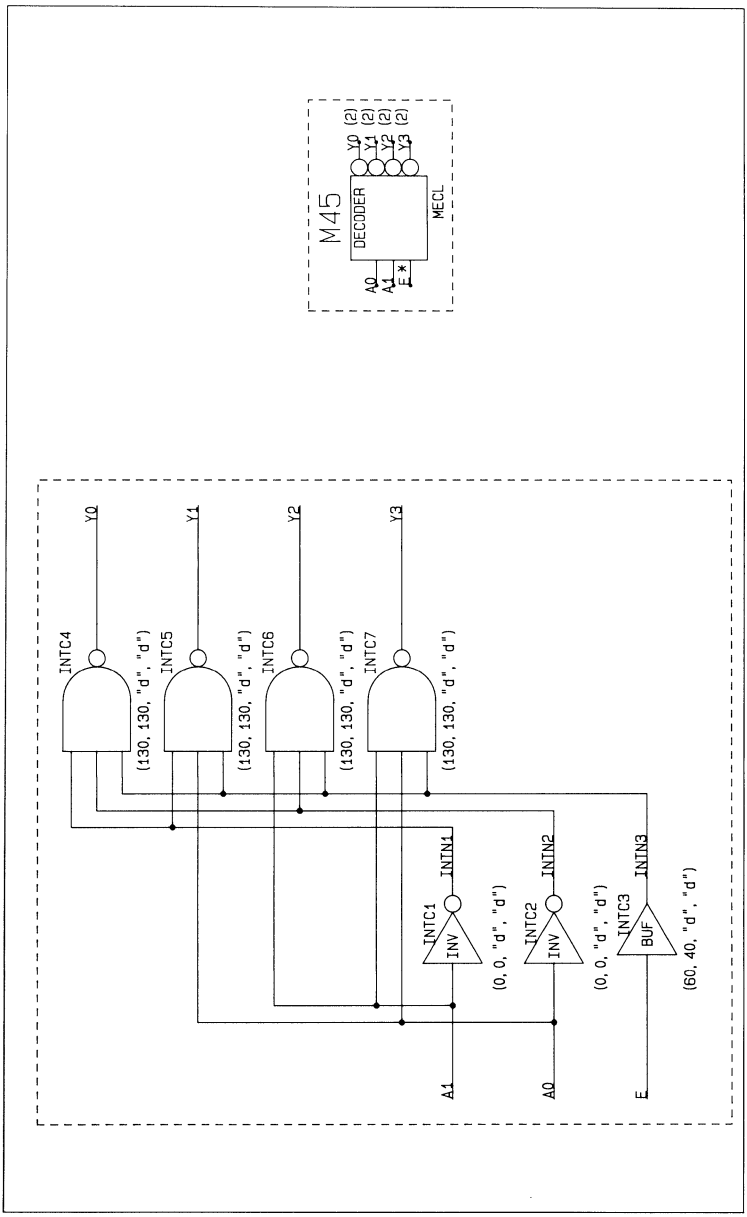
COMPONENT PLOTS

Plot 88



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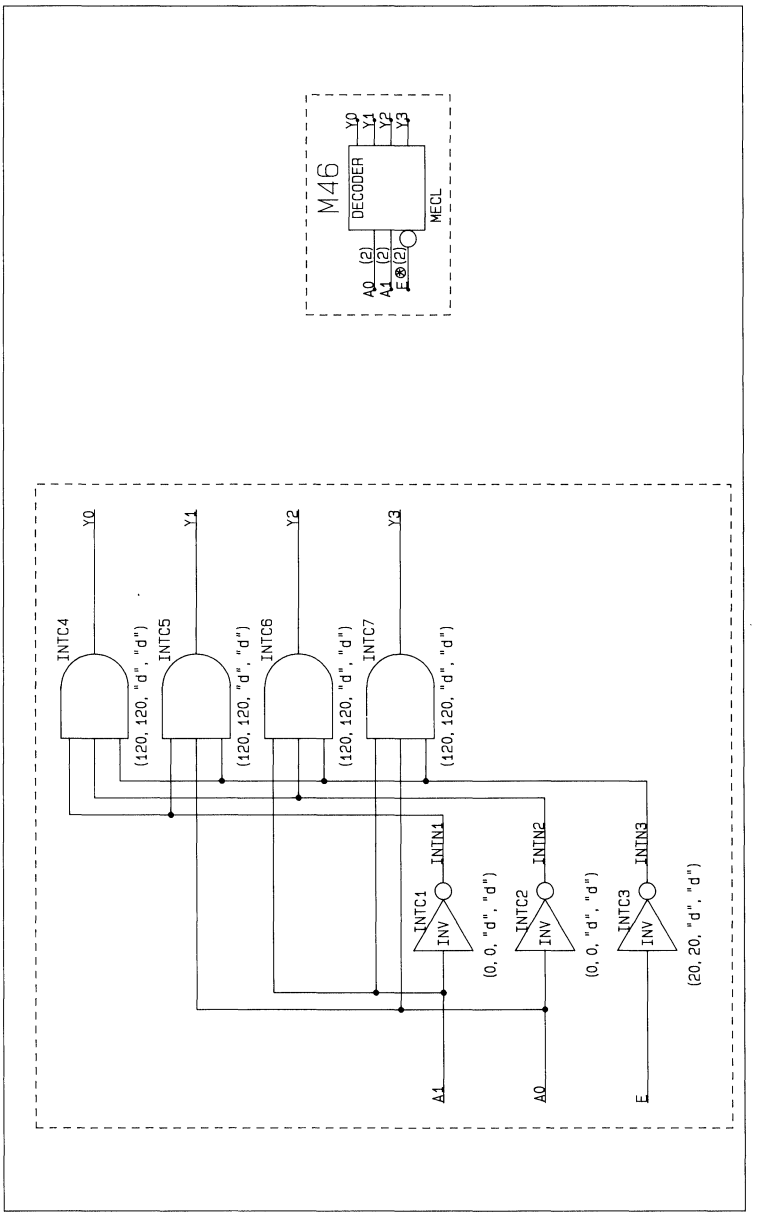
COMPONENT PLOTS

Plot 89



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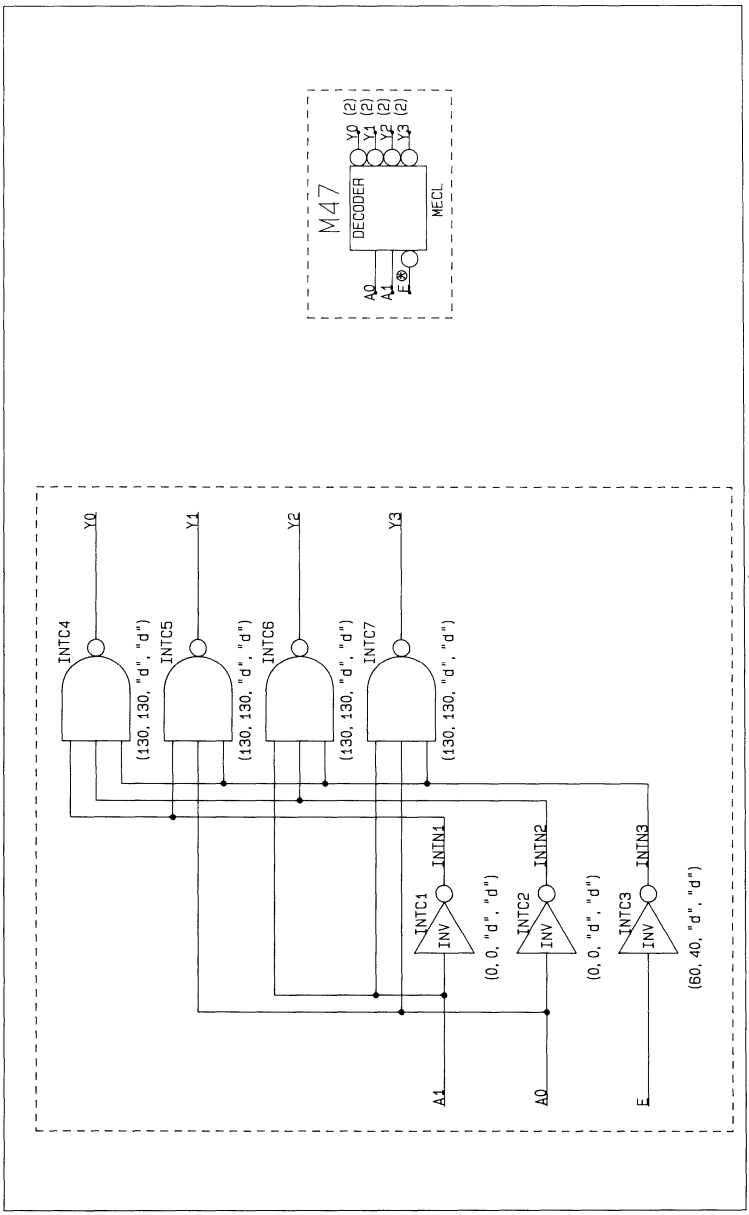
COMPONENT PLOTS

Plot 90



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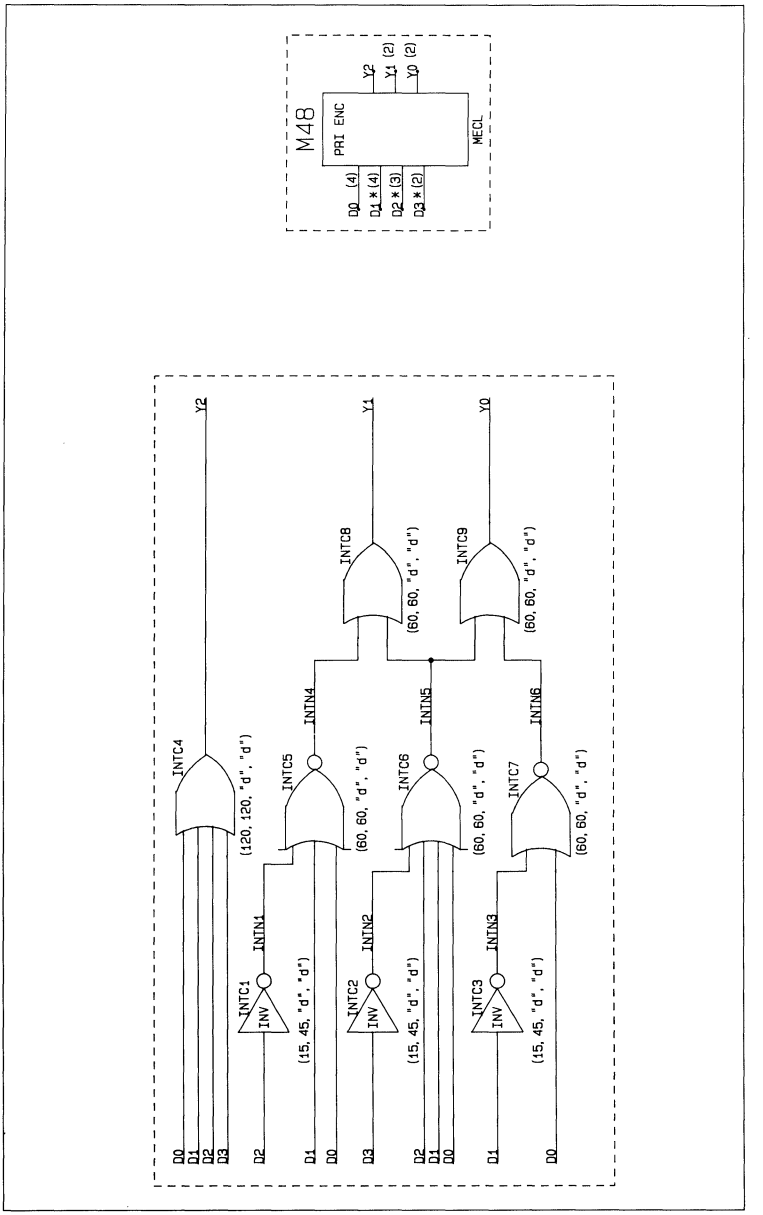
COMPONENT PLOTS

Plot 91



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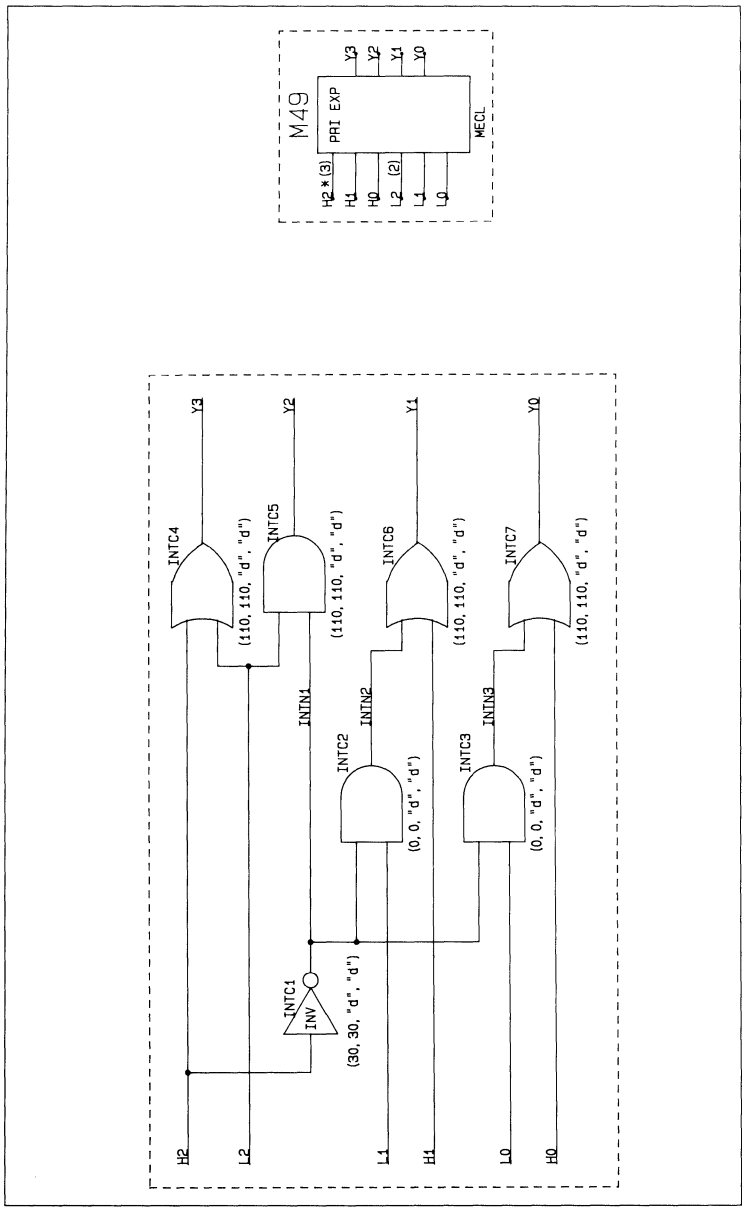
COMPONENT PLOTS

Plot 92



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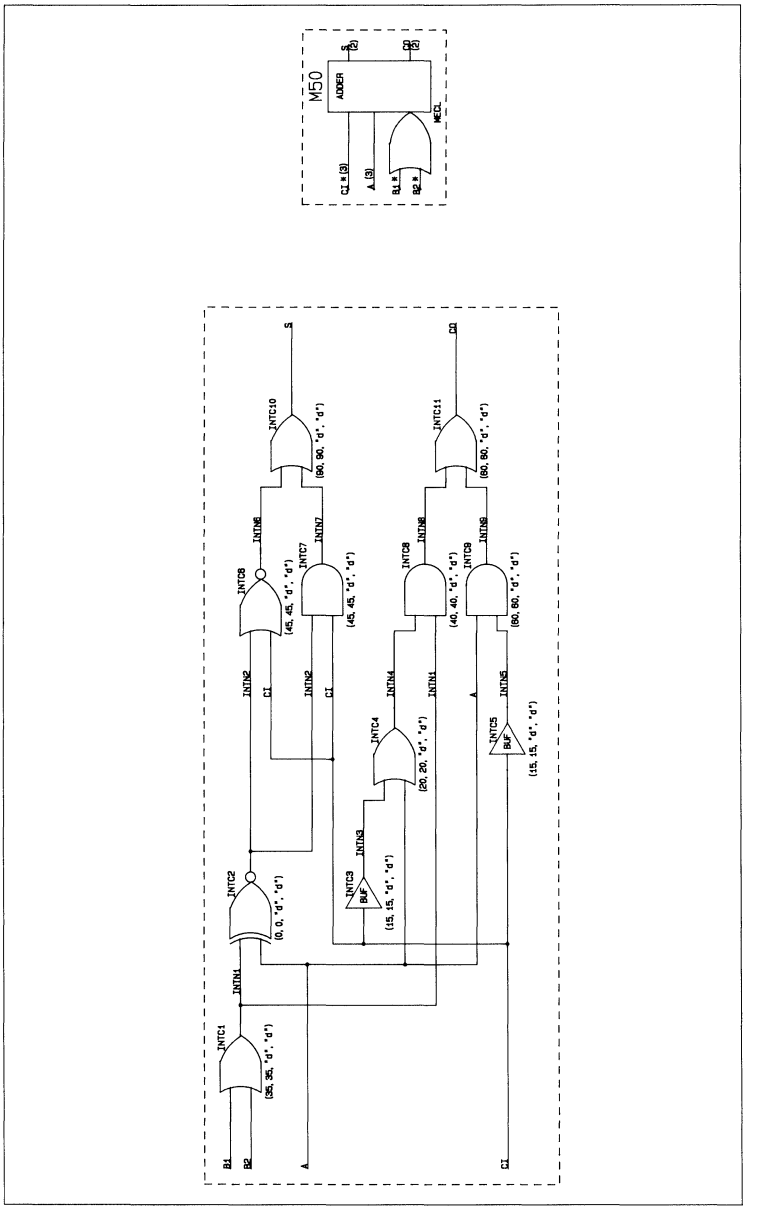
COMPONENT PLOTS

Plot 93



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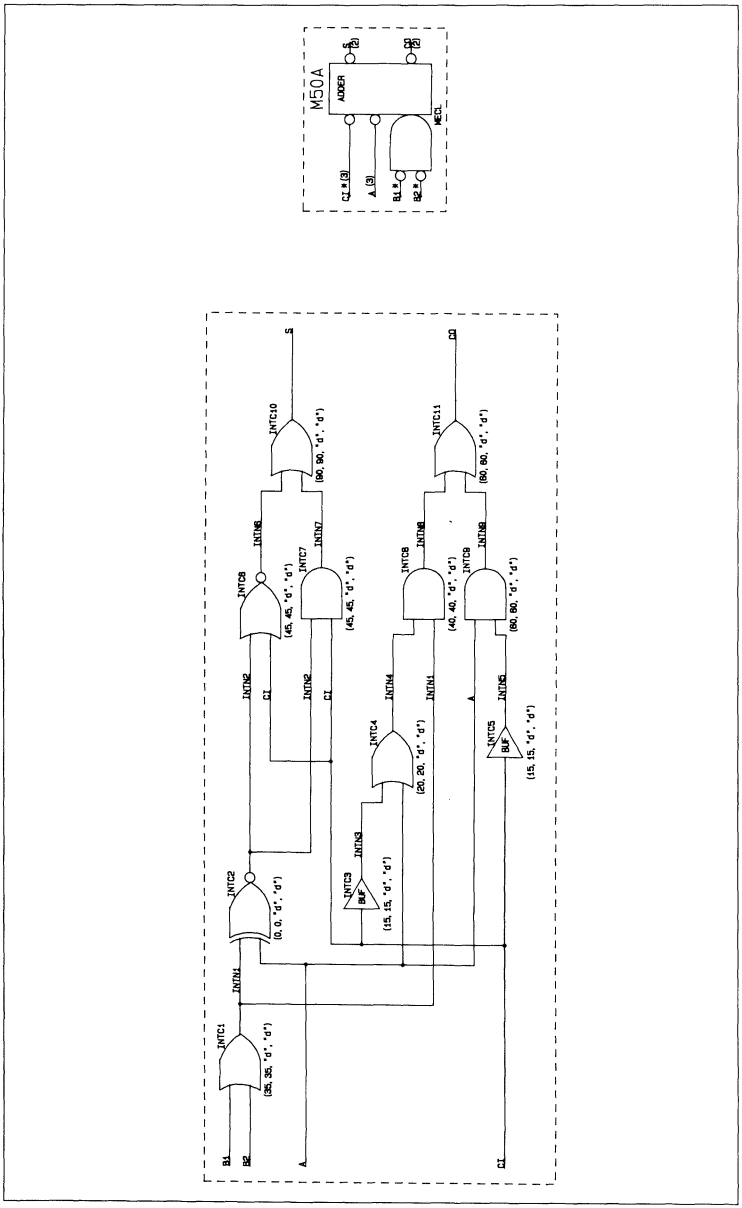
COMPONENT PLOTS

Plot 94



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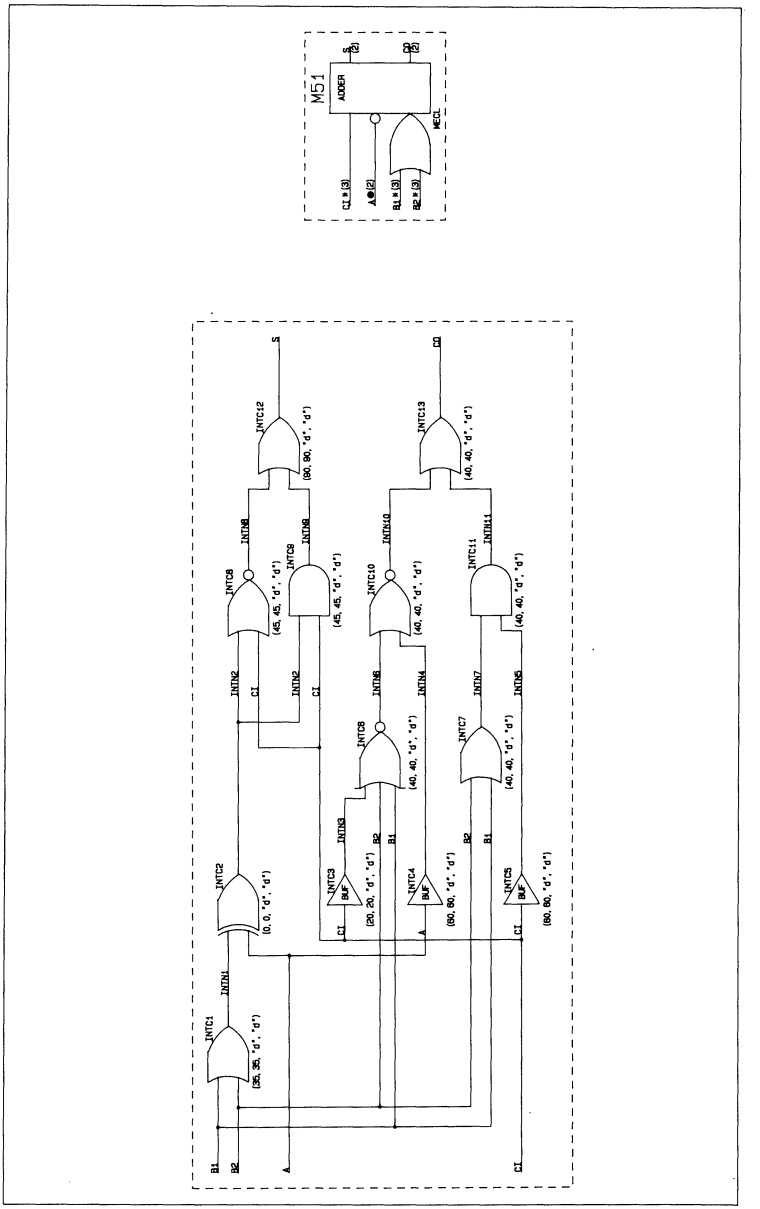
COMPONENT PLOTS

Plot 95



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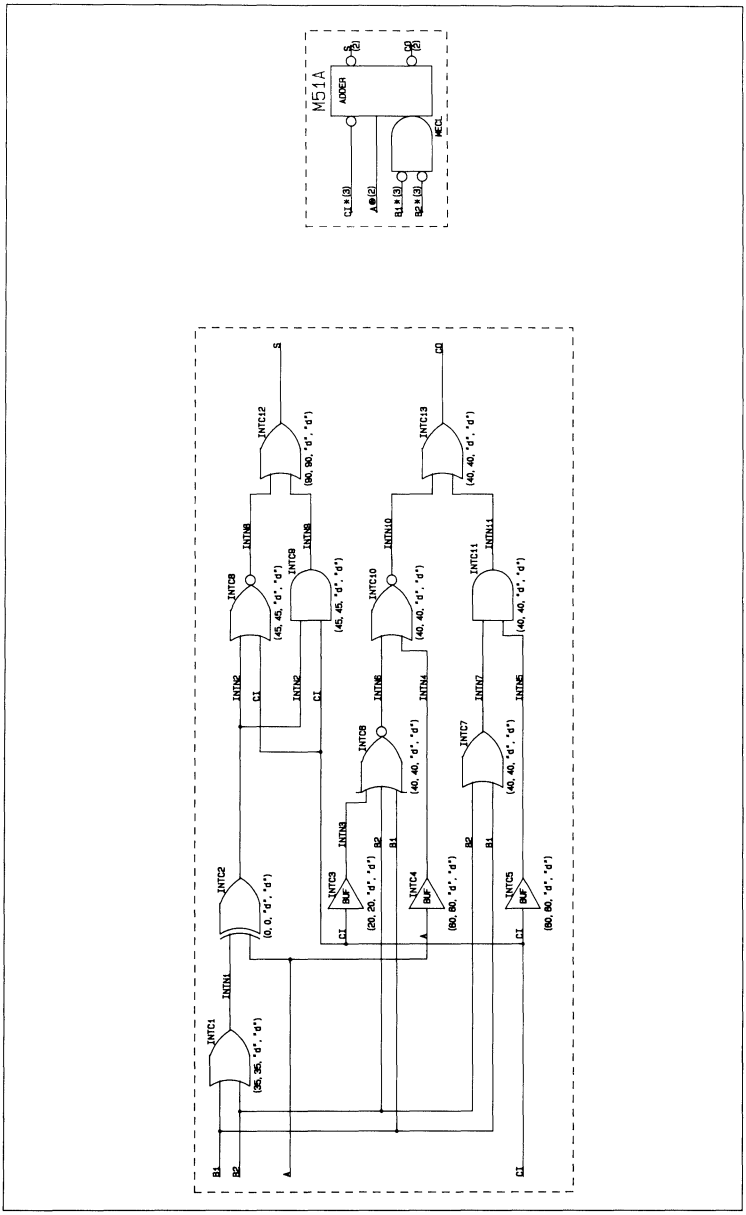
COMPONENT PLOTS

Plot 96



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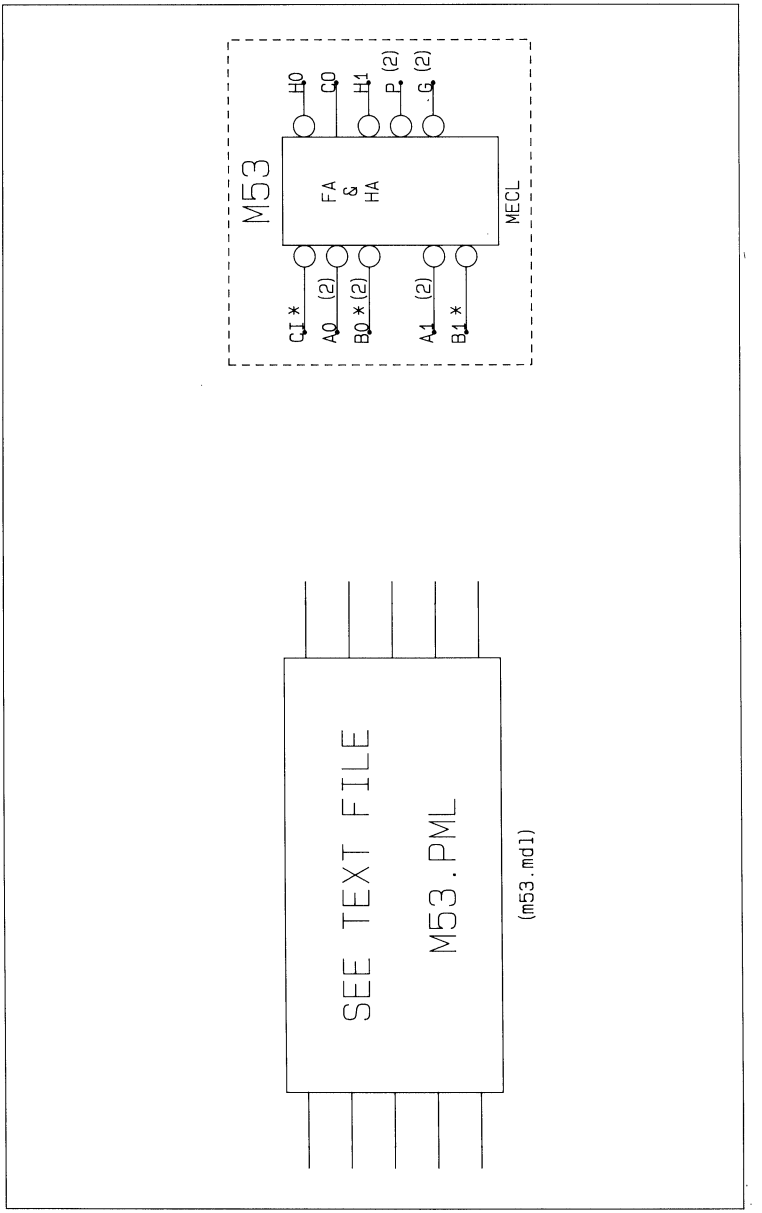
COMPONENT PLOTS

Plot 97



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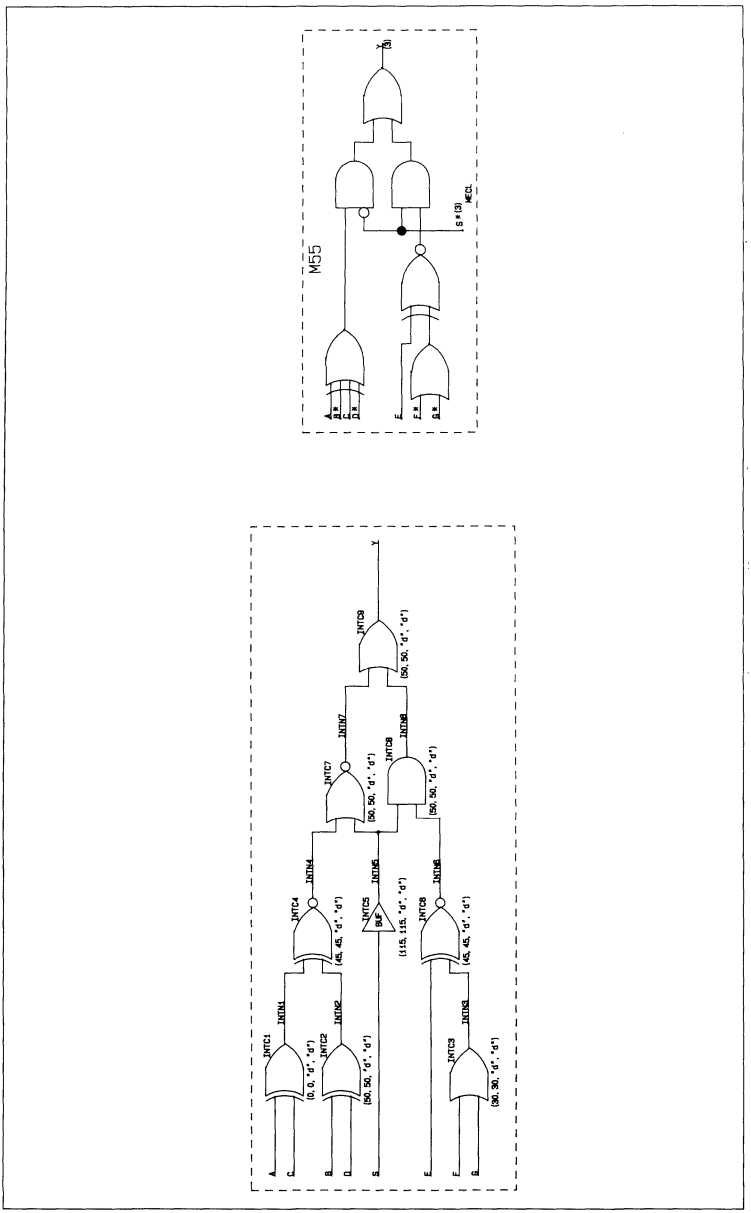
COMPONENT PLOTS

Plot 98



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COMPONENT PLOTS

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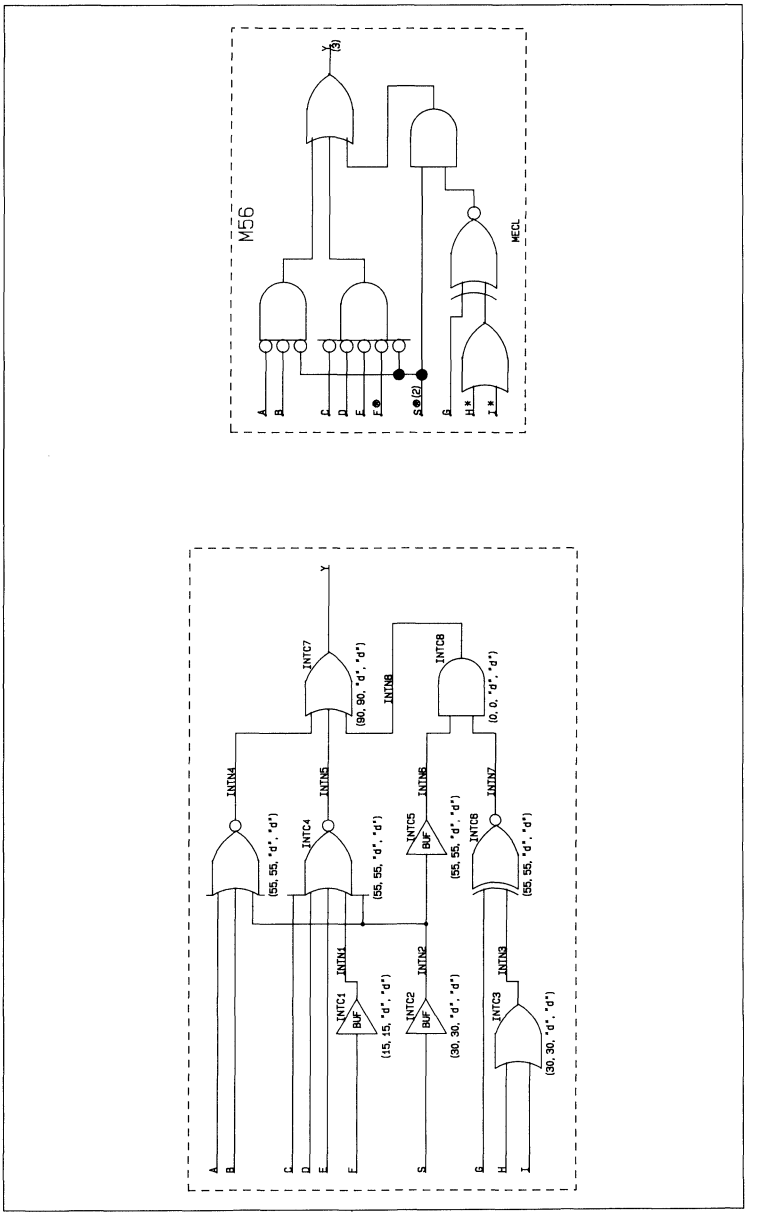

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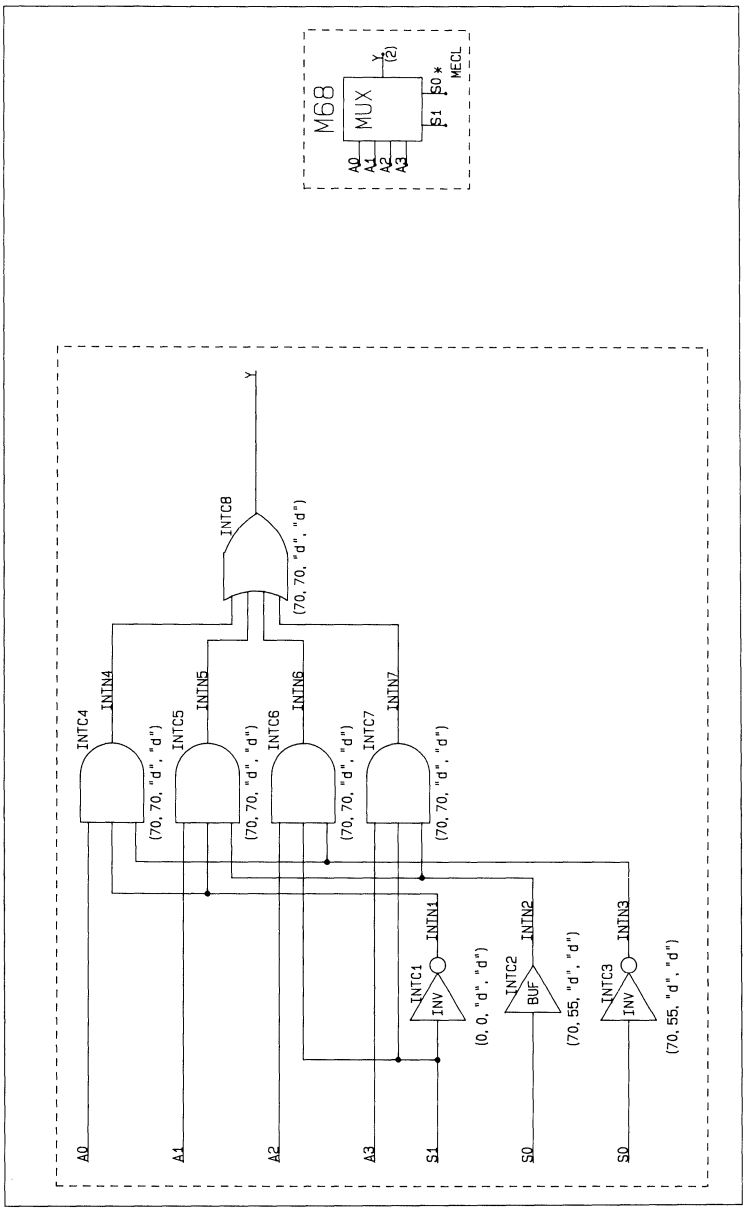
COMPONENT PLOTS

Plot 100



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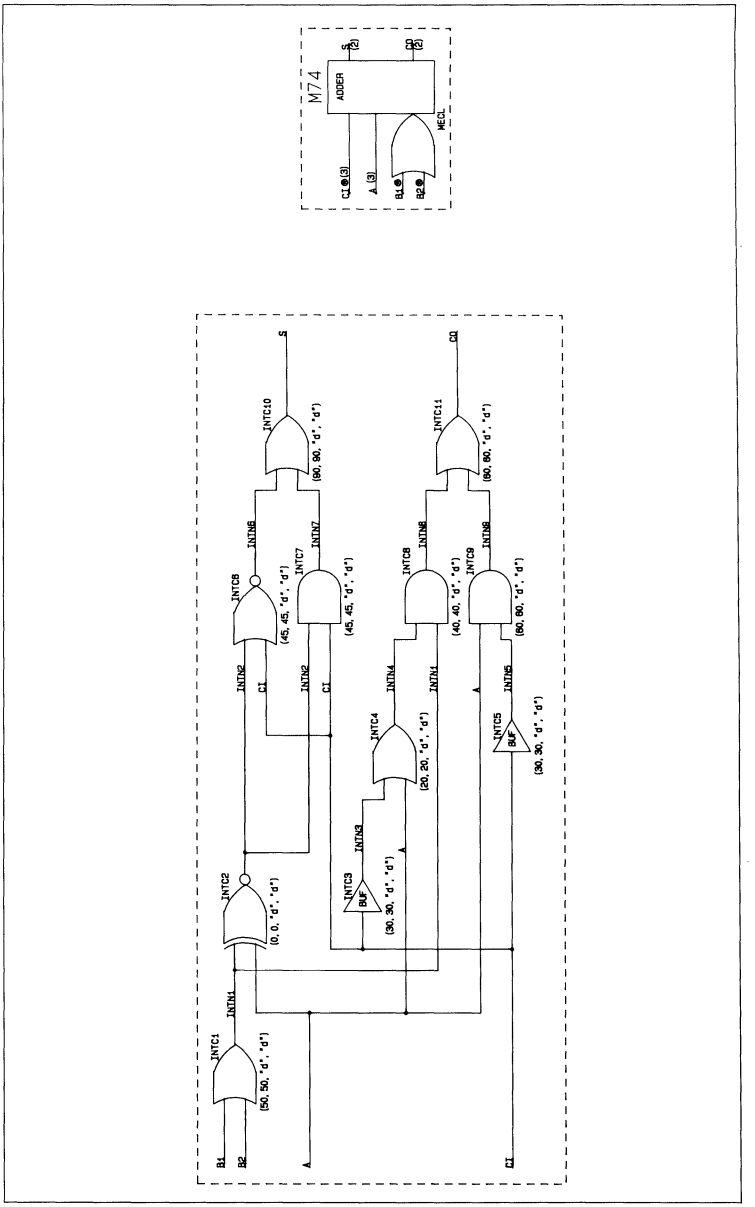
COMPONENT PLOTS

Plot 101



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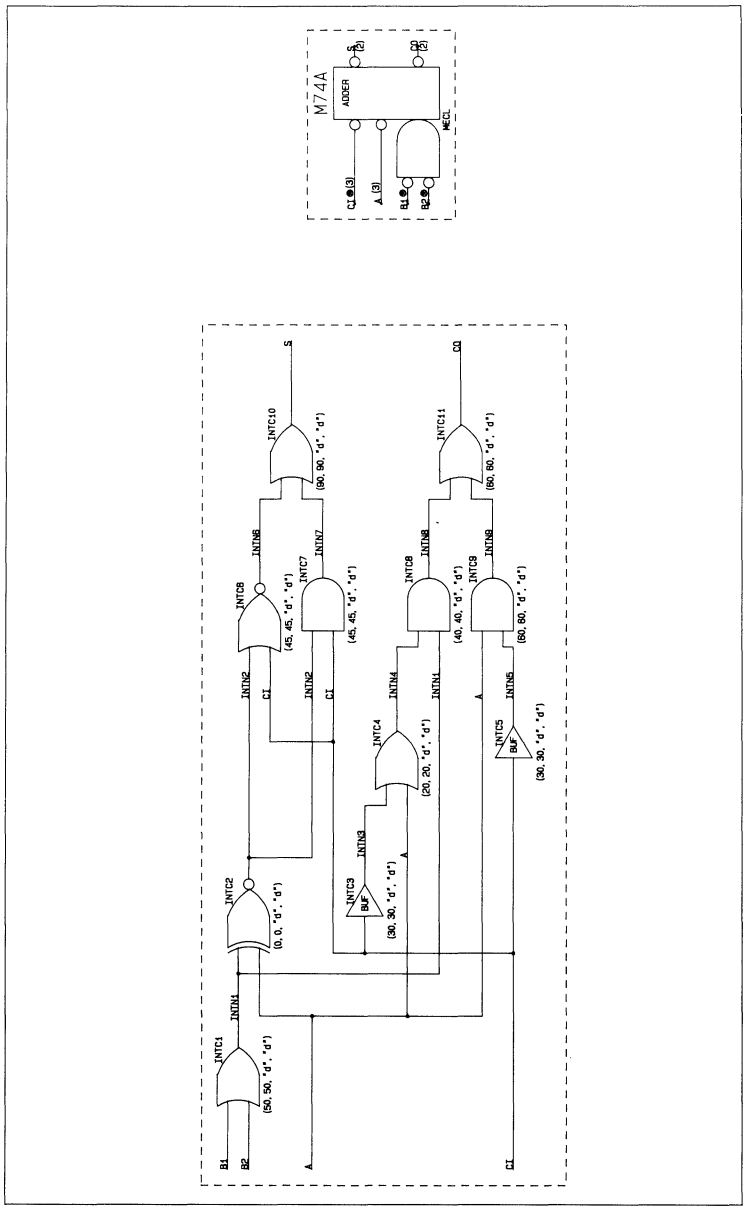
COMPONENT PLOTS

Plot 102



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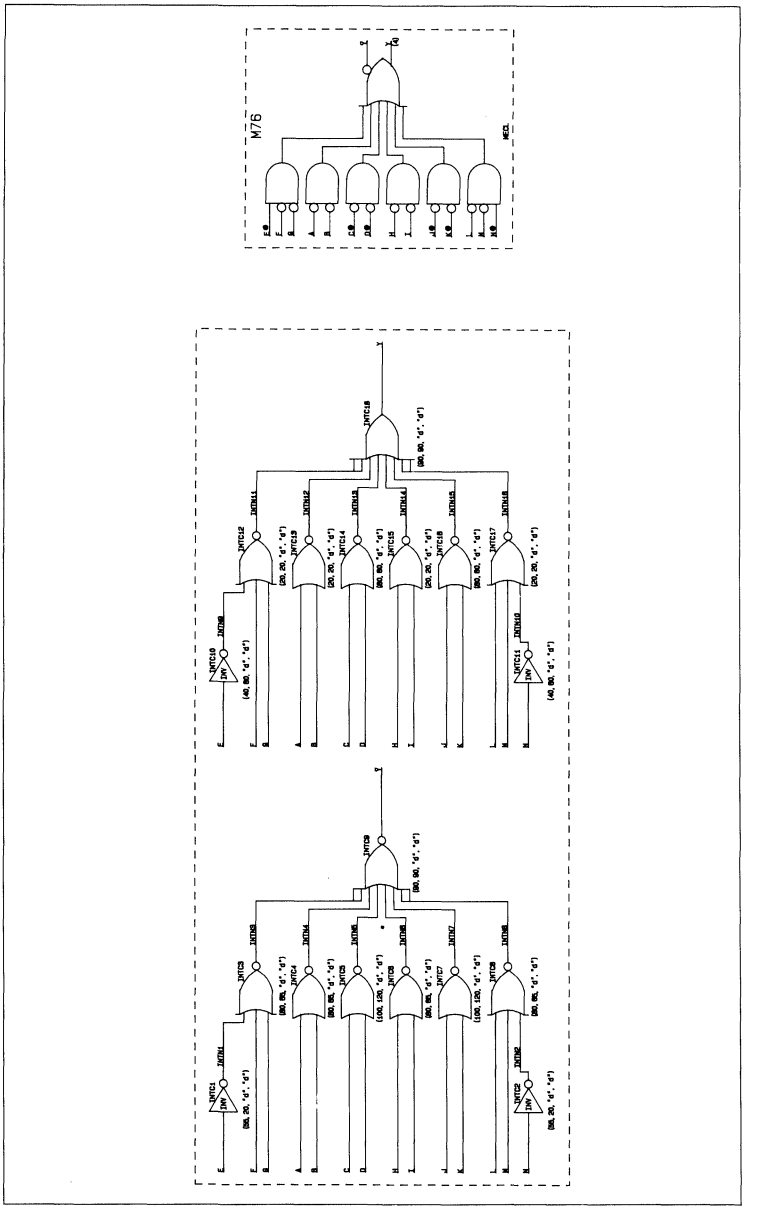
COMPONENT PLOTS

Plot 103



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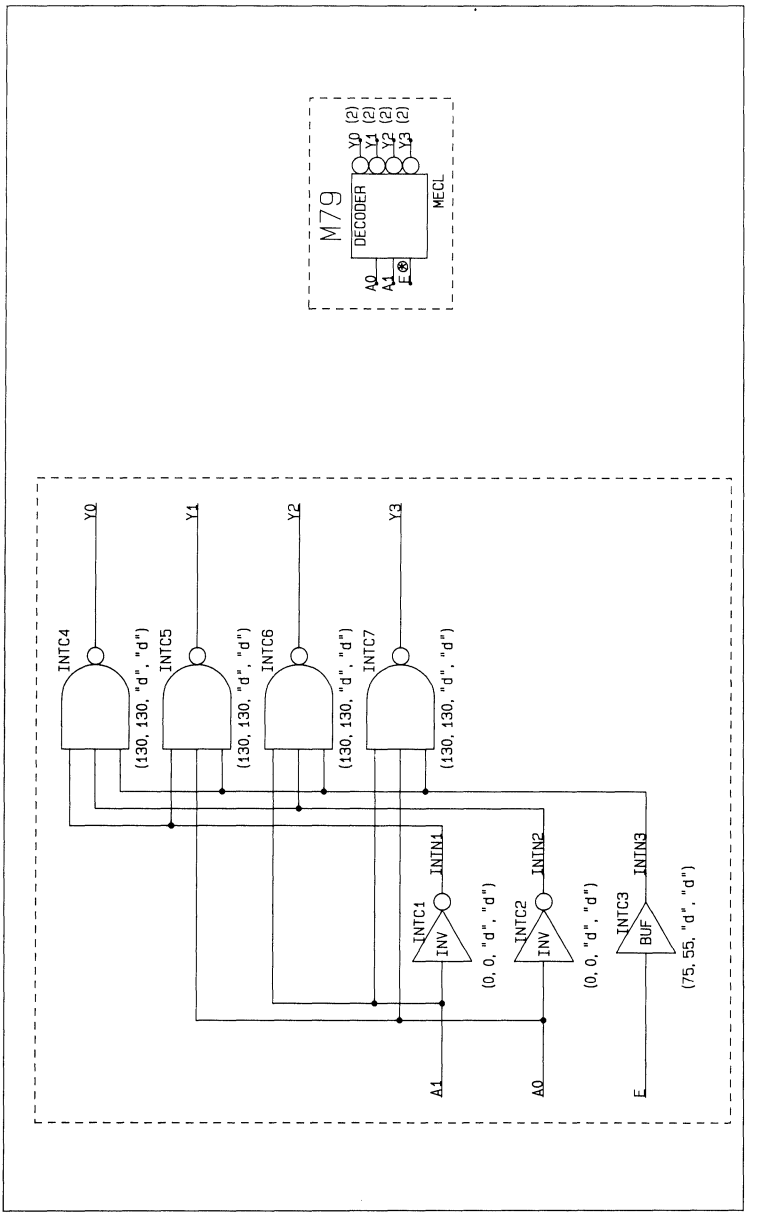
COMPONENT PLOTS

Plot 104



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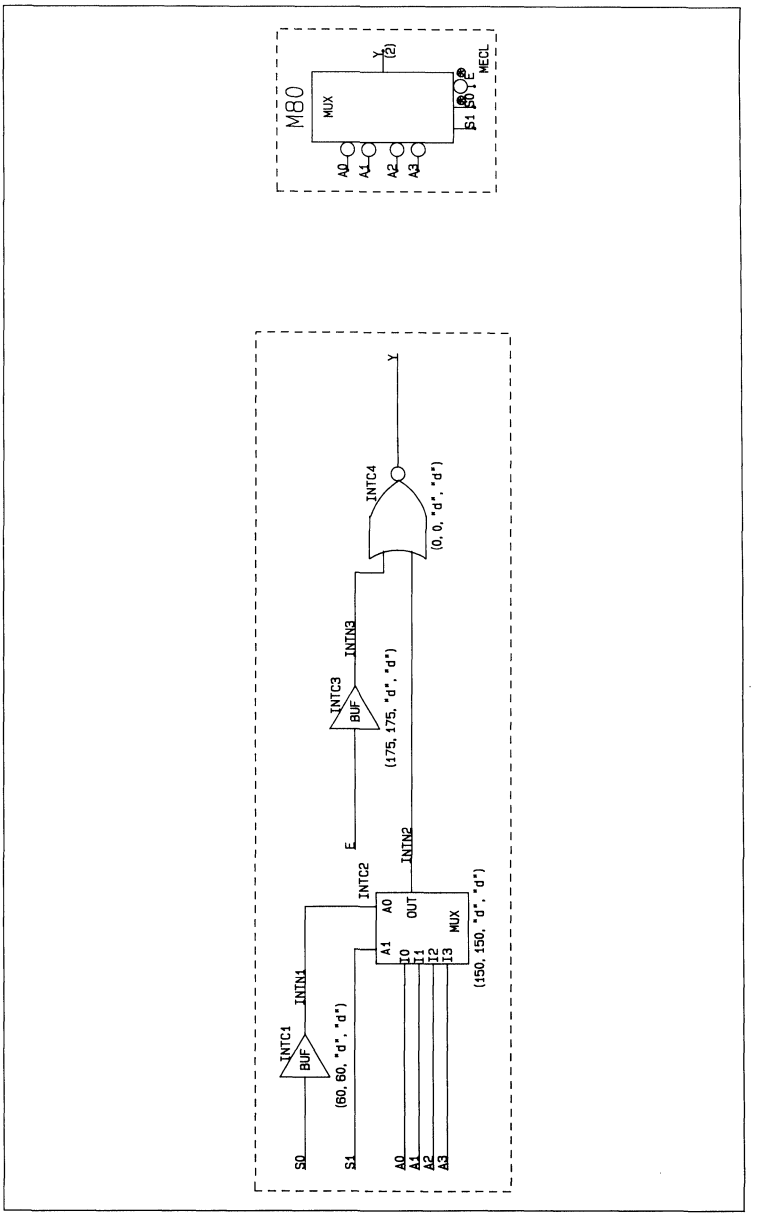
COMPONENT PLOTS

Plot 105



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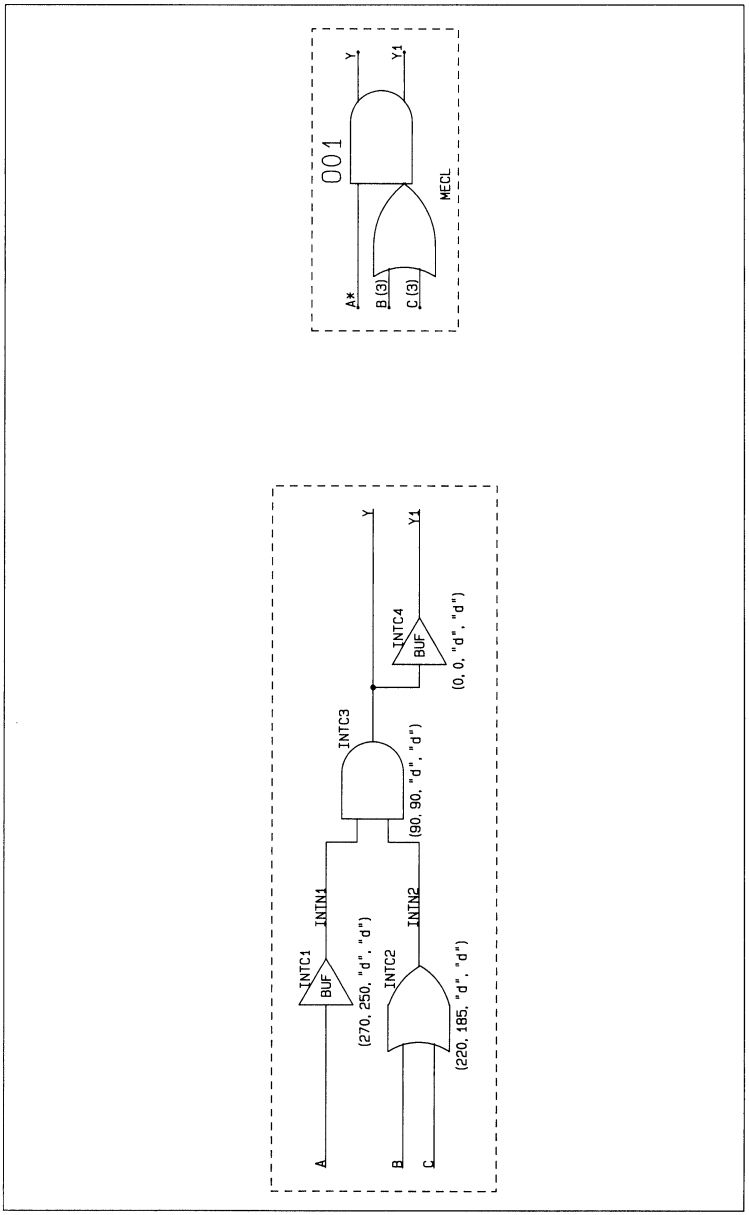
COMPONENT PLOTS

Plot 106



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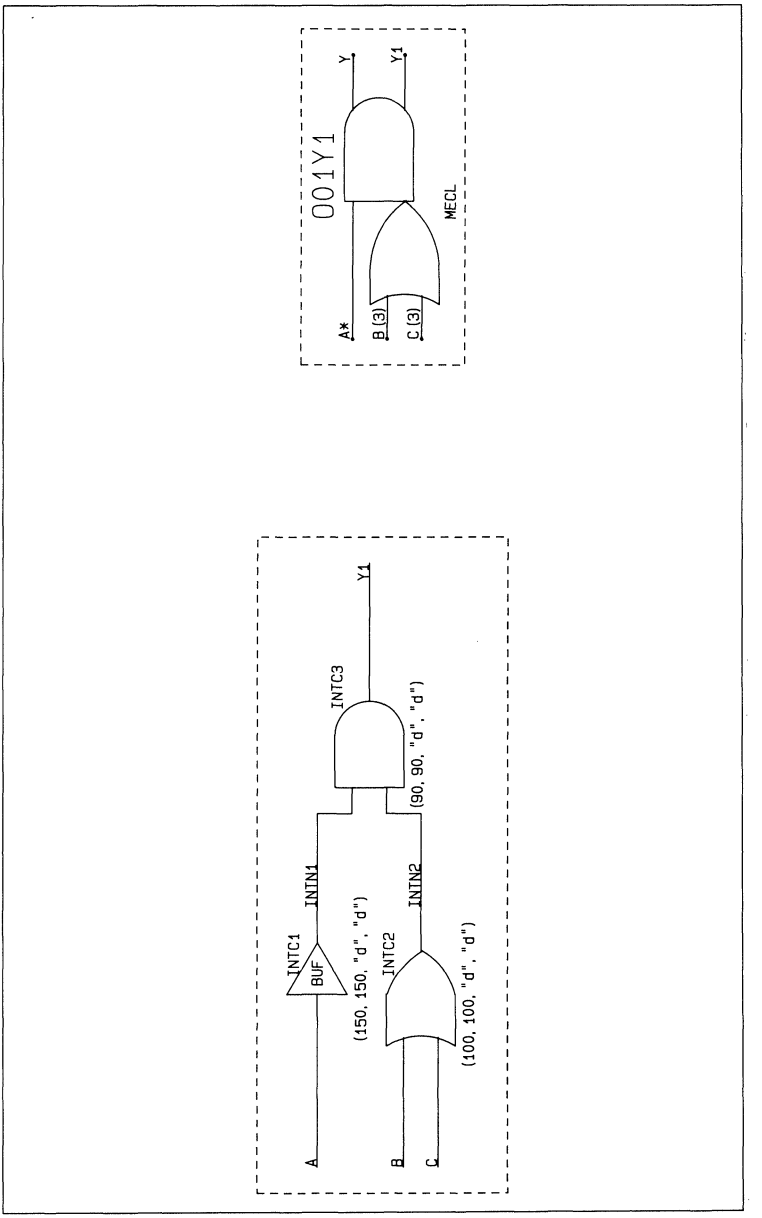
COMPONENT PLOTS

Plot 107



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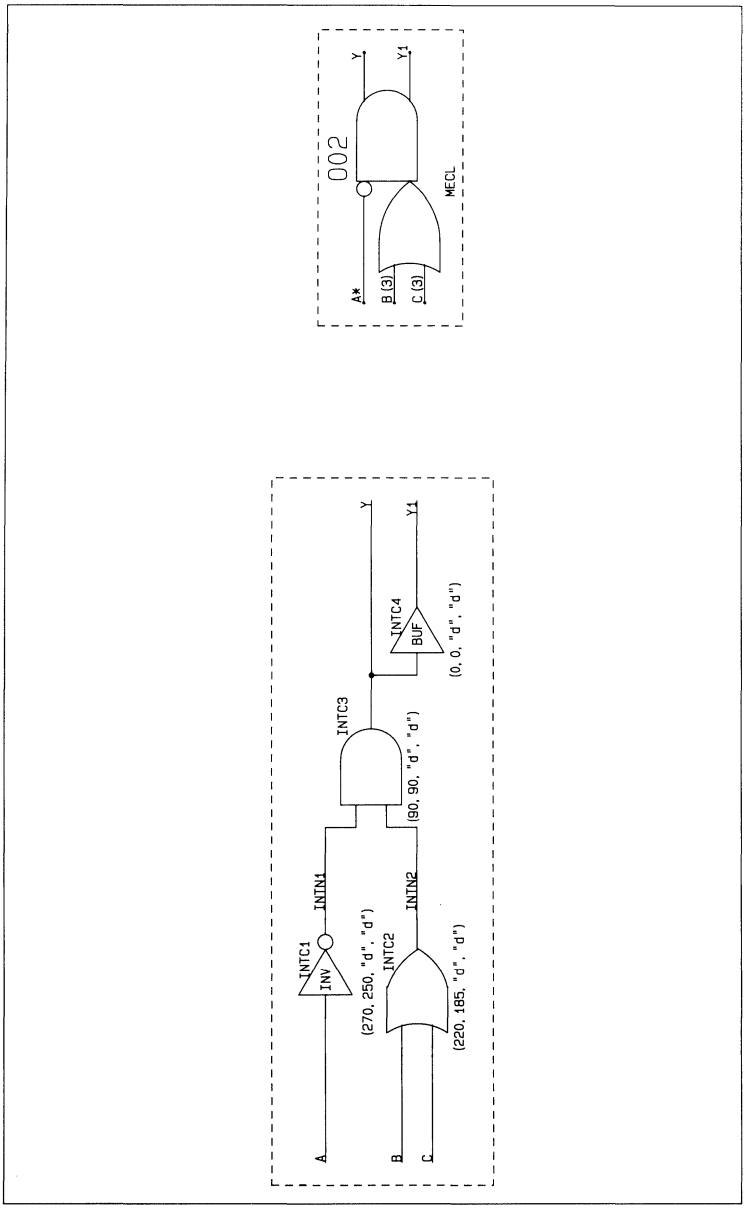
COMPONENT PLOTS

Plot 108



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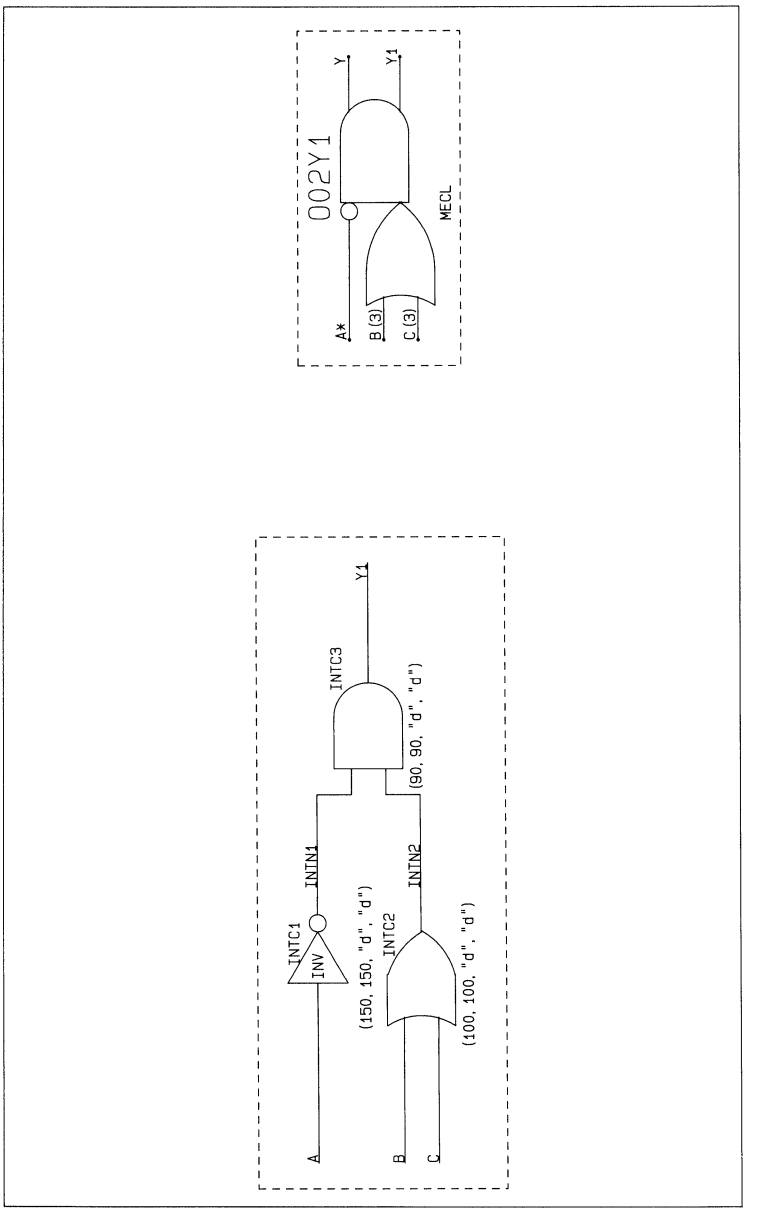
COMPONENT PLOTS

Plot 109



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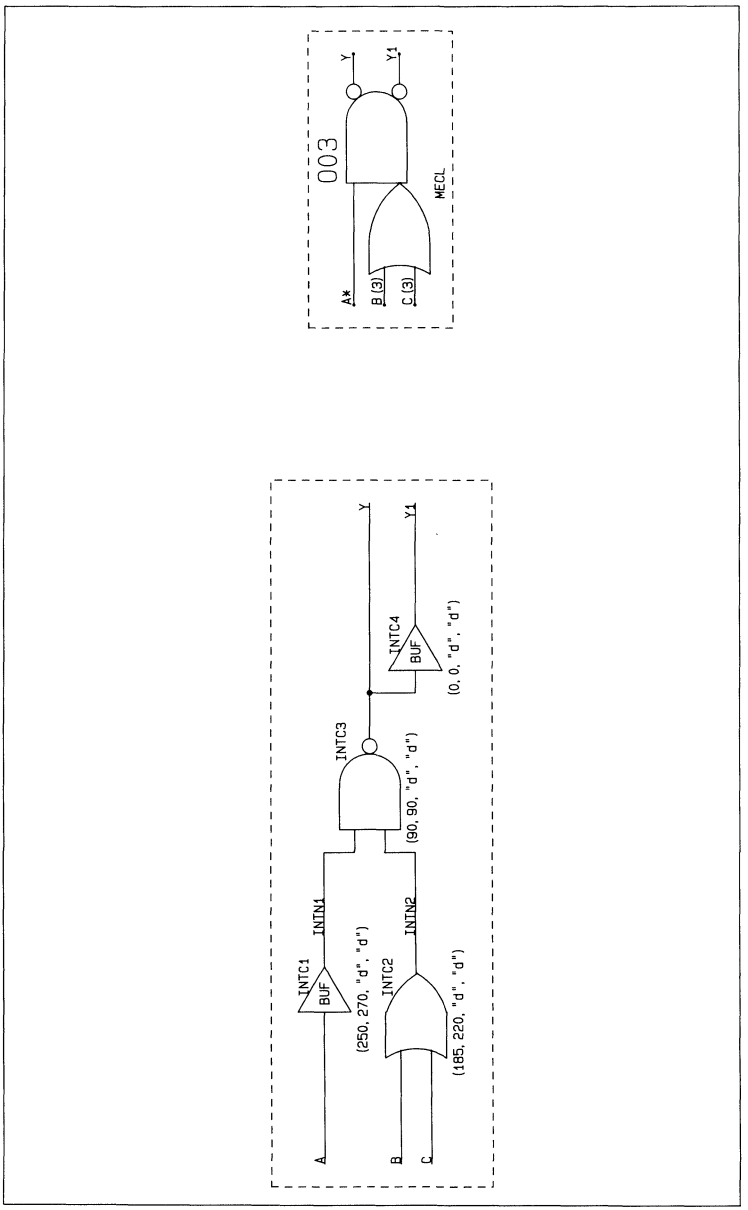
COMPONENT PLOTS

Plot 110



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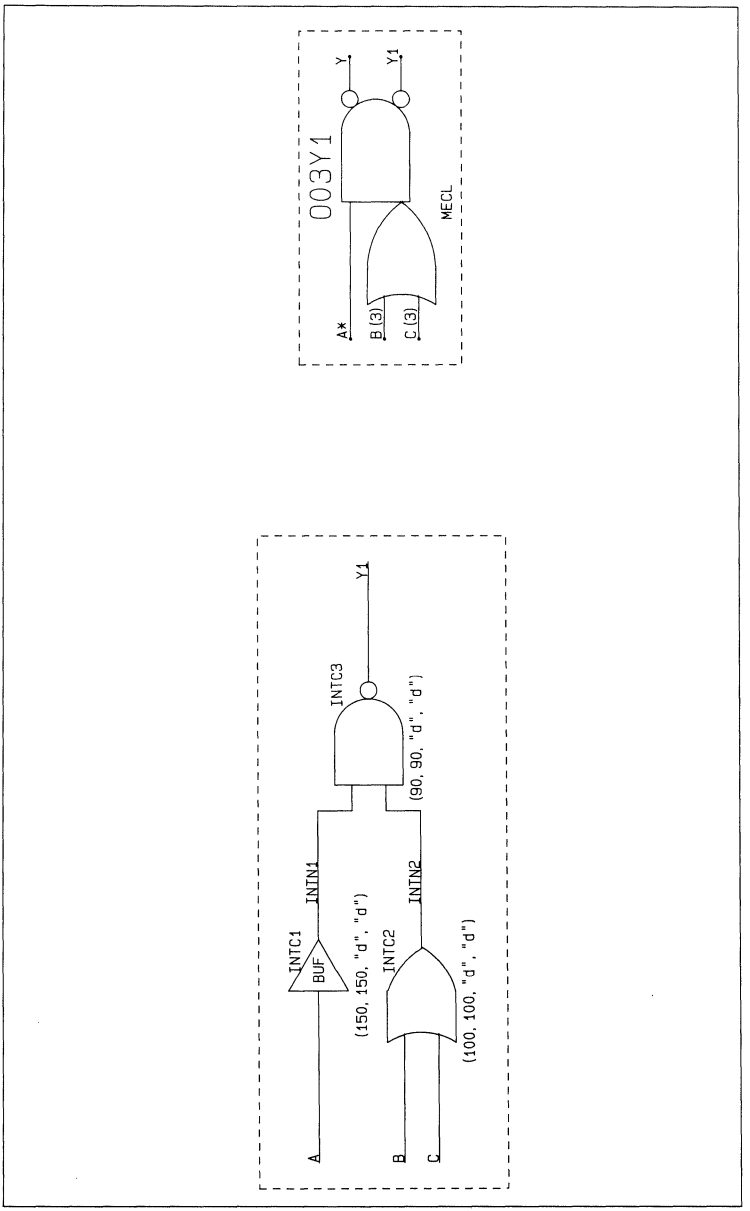
COMPONENT PLOTS

Plot 111



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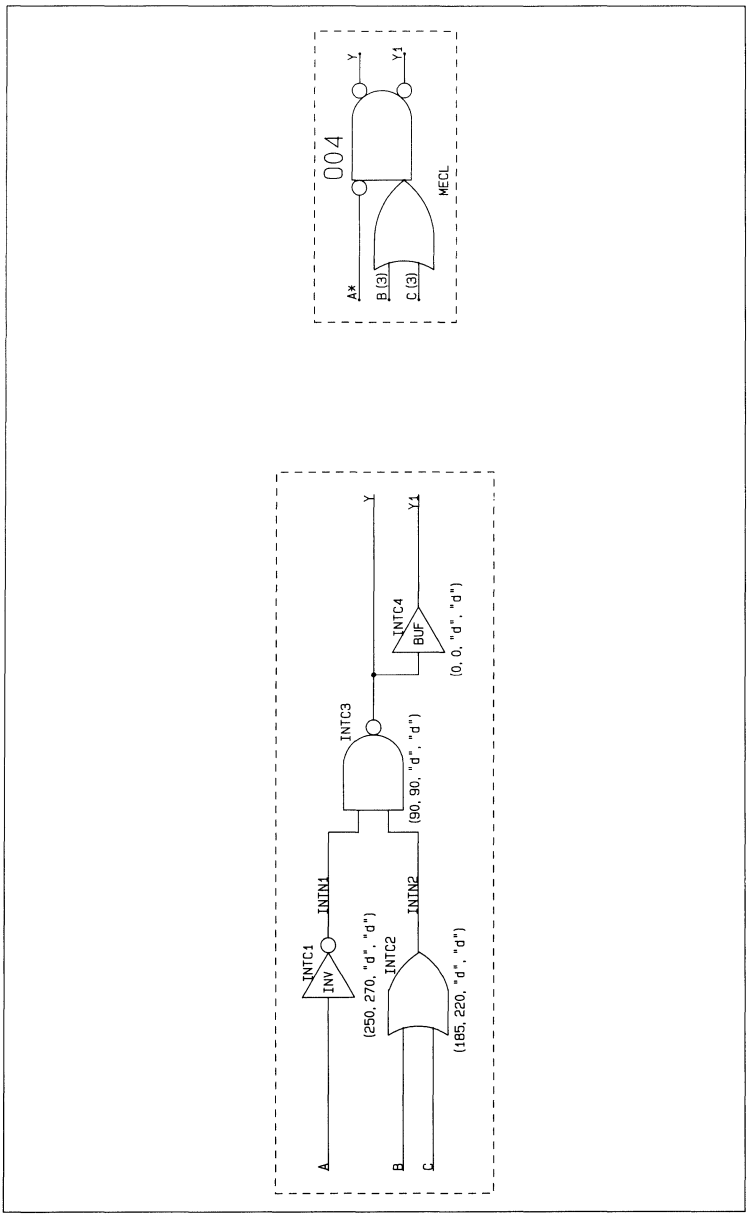
COMPONENT PLOTS

Plot 112



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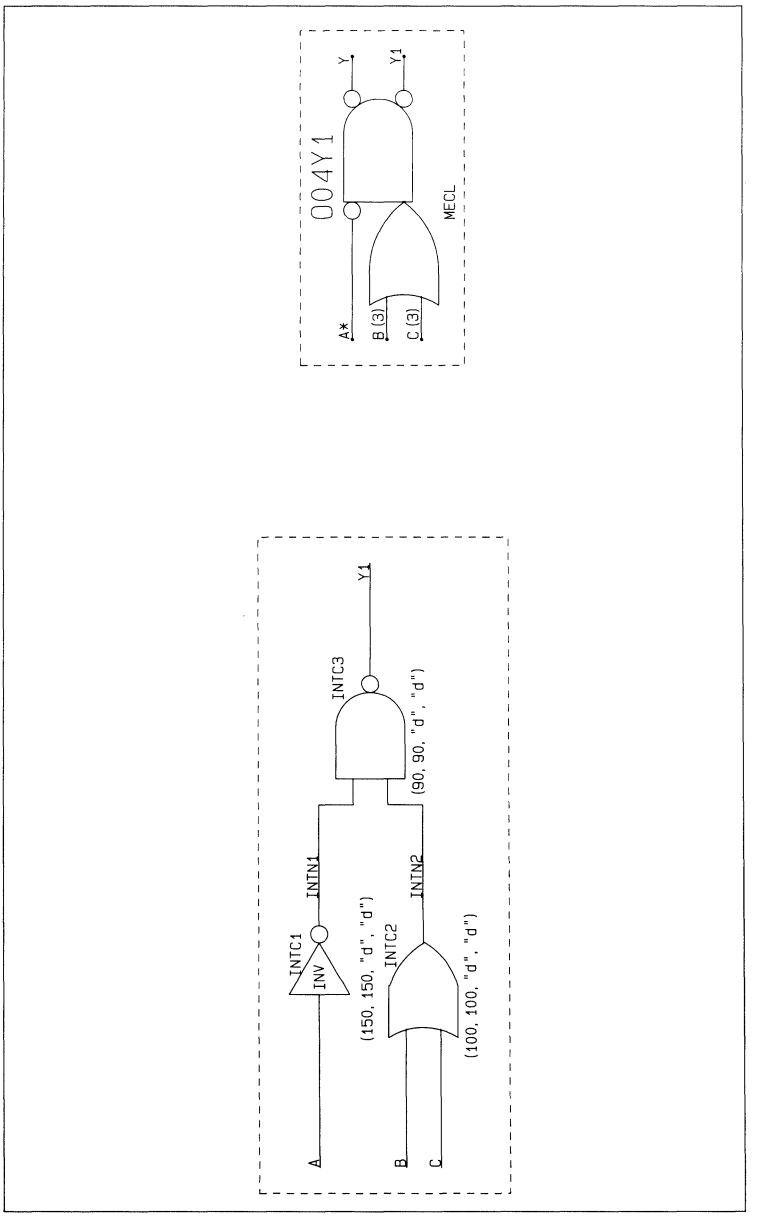
COMPONENT PLOTS

Plot 113



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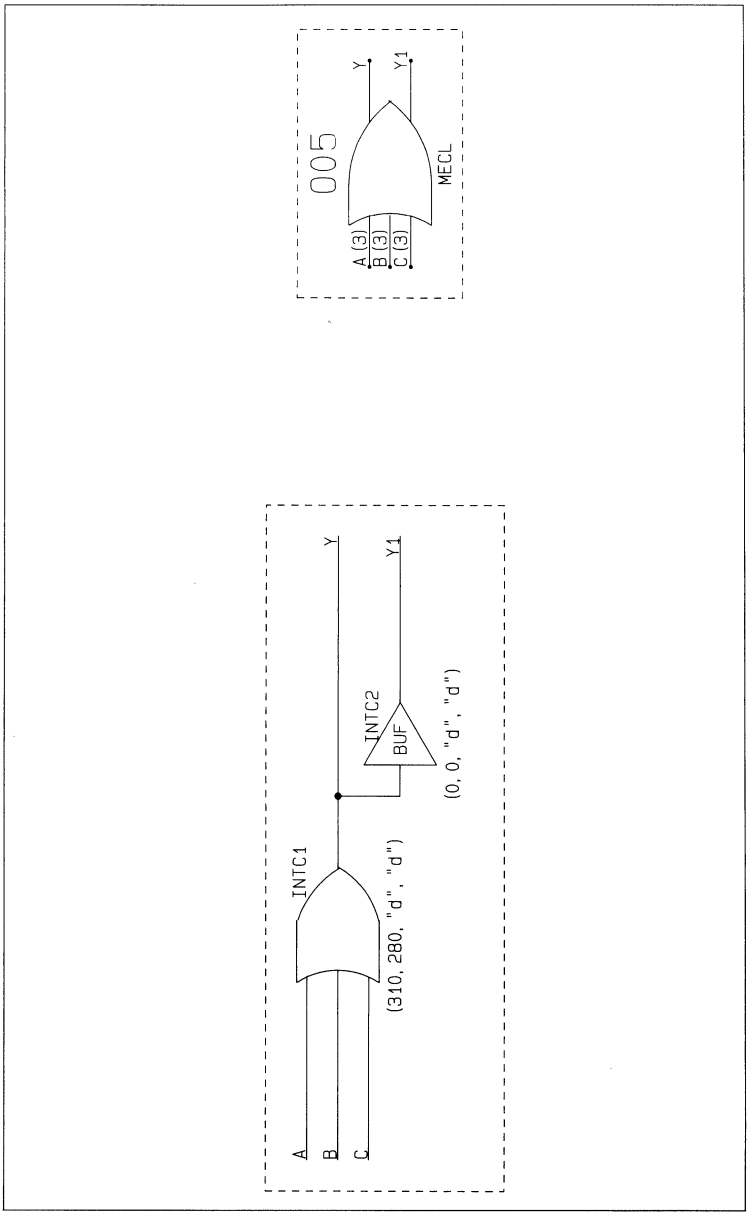
COMPONENT PLOTS

Plot 114



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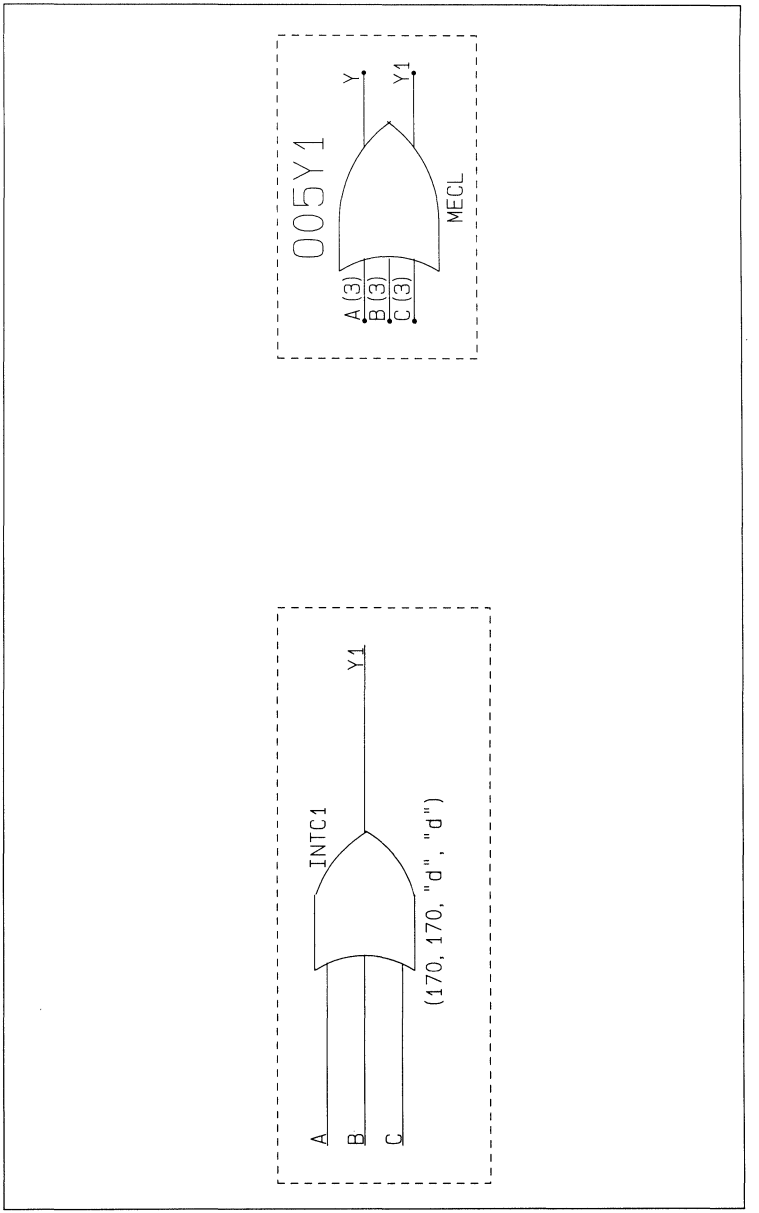
COMPONENT PLOTS

Plot 115



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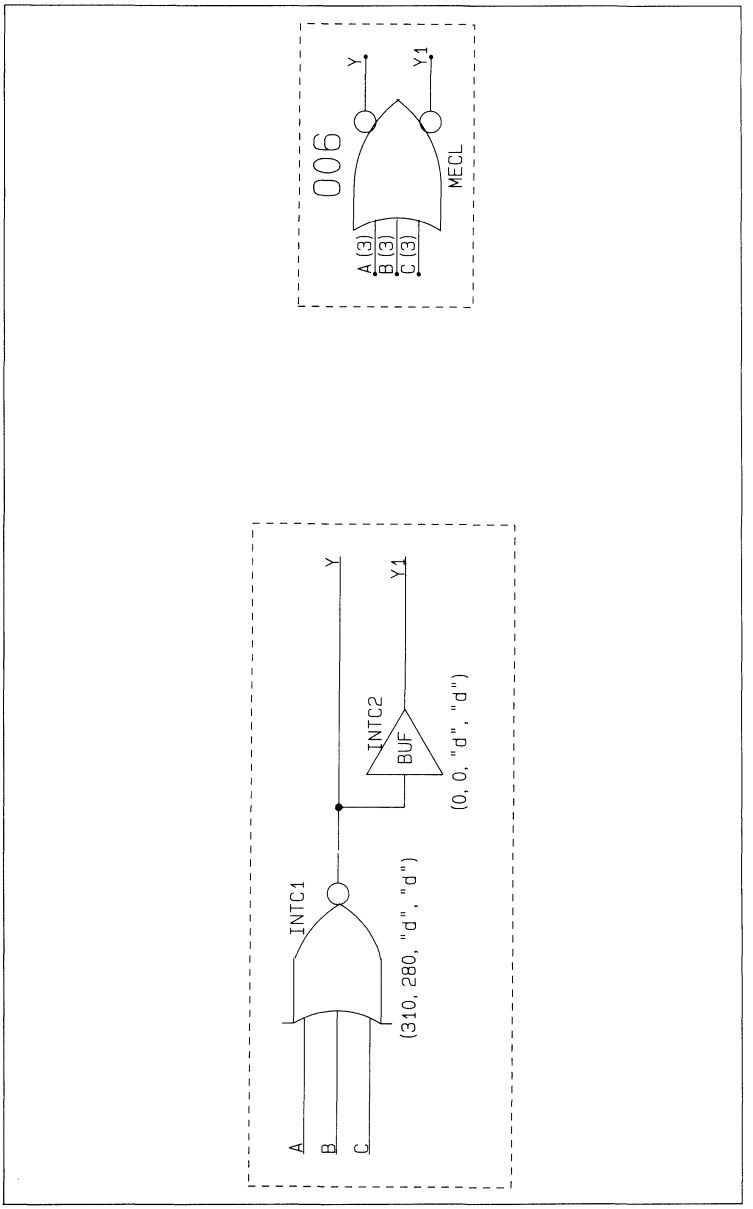
COMPONENT PLOTS

Plot 116



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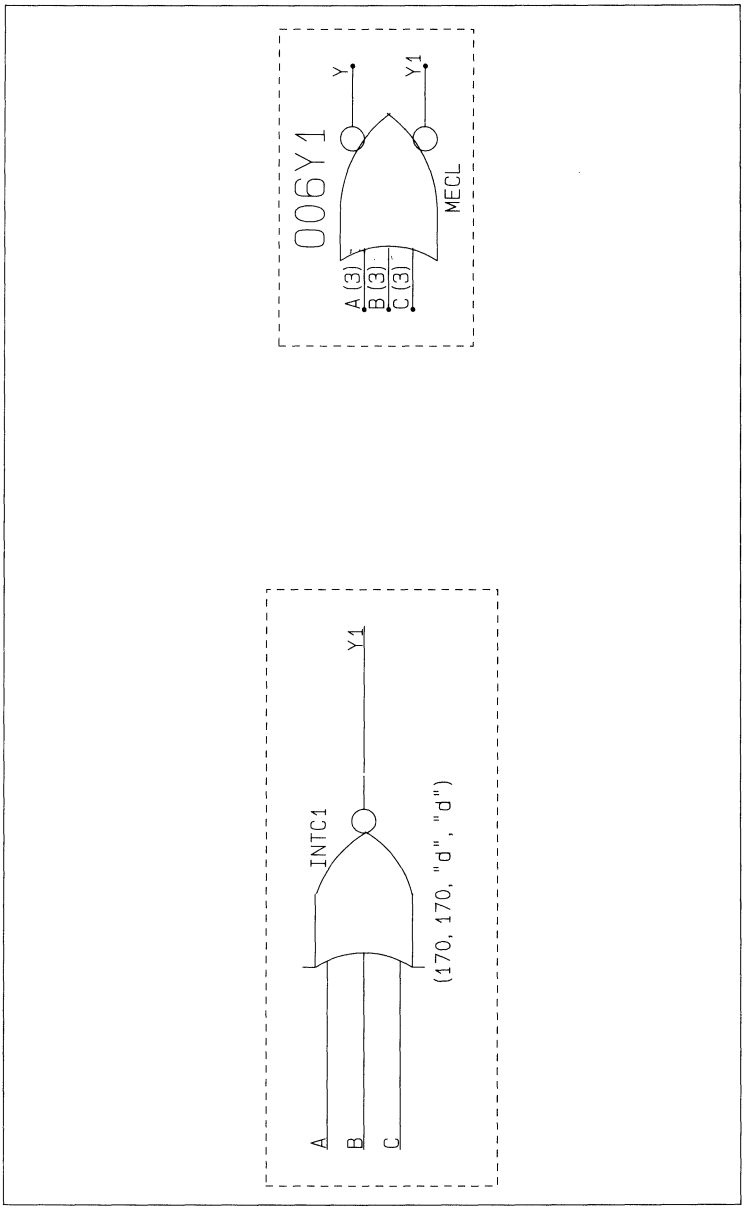
COMPONENT PLOTS

Plot 117



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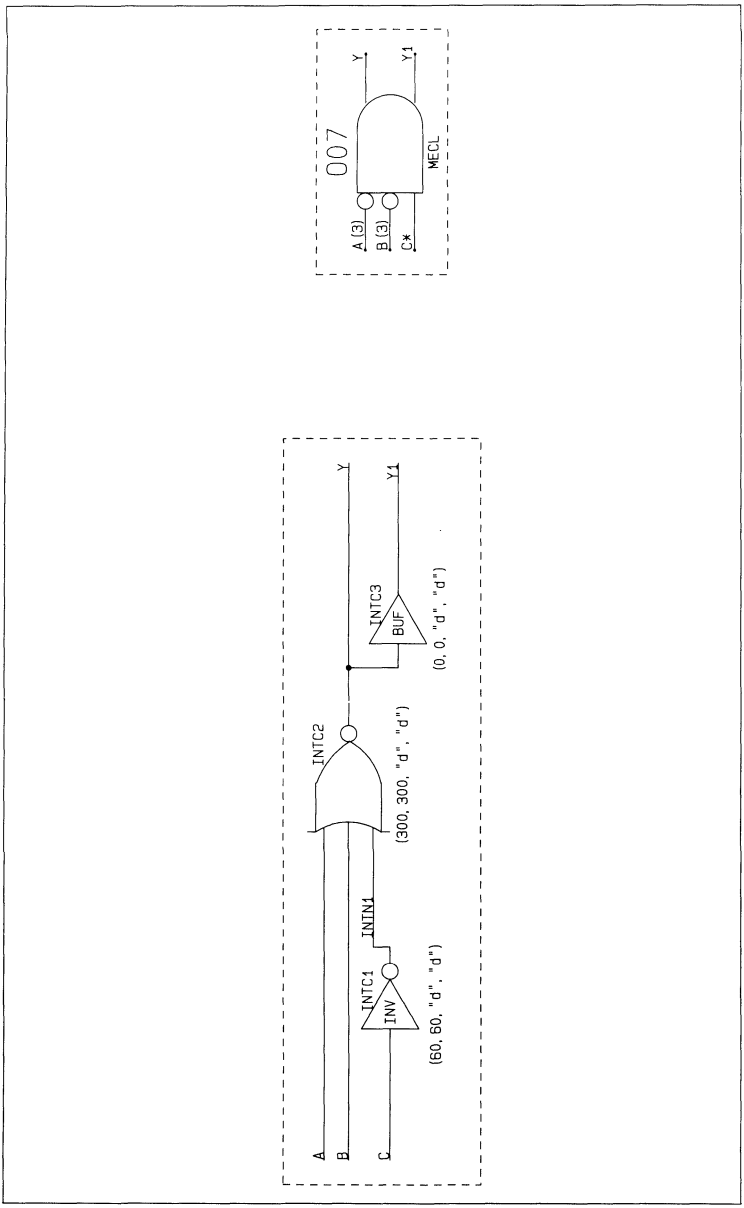
COMPONENT PLOTS

Plot 118



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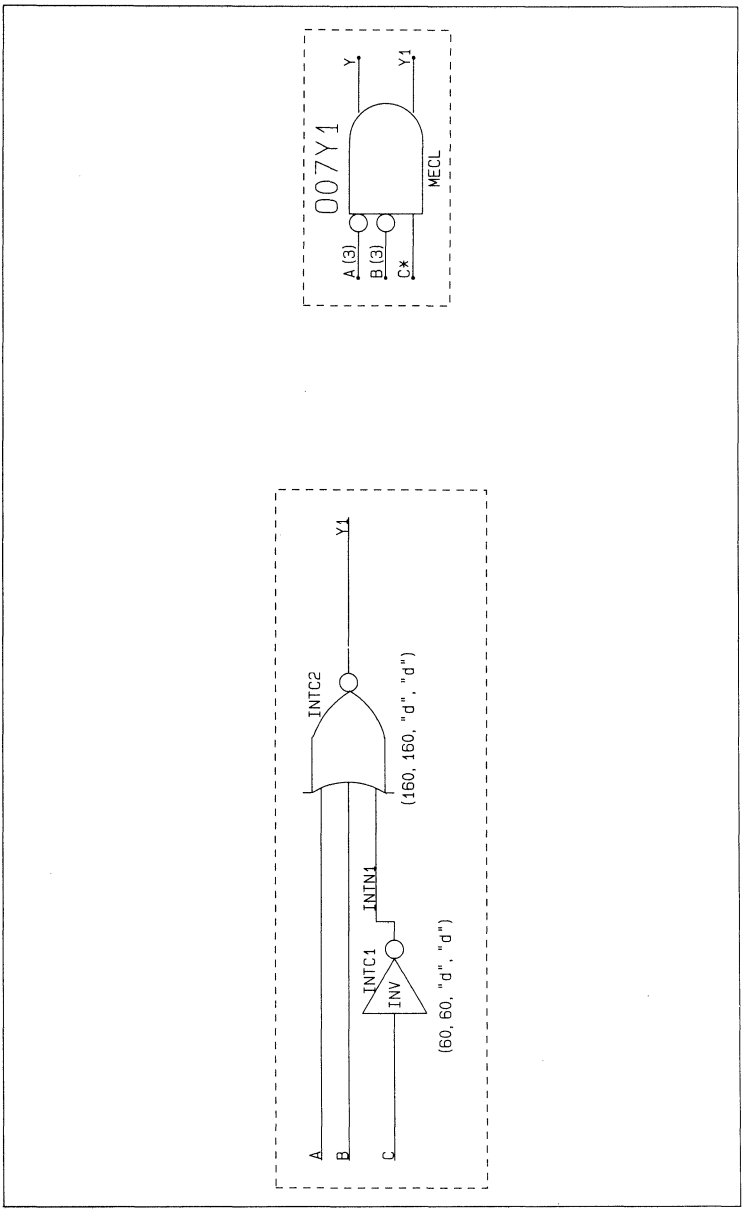
COMPONENT PLOTS

Plot 119



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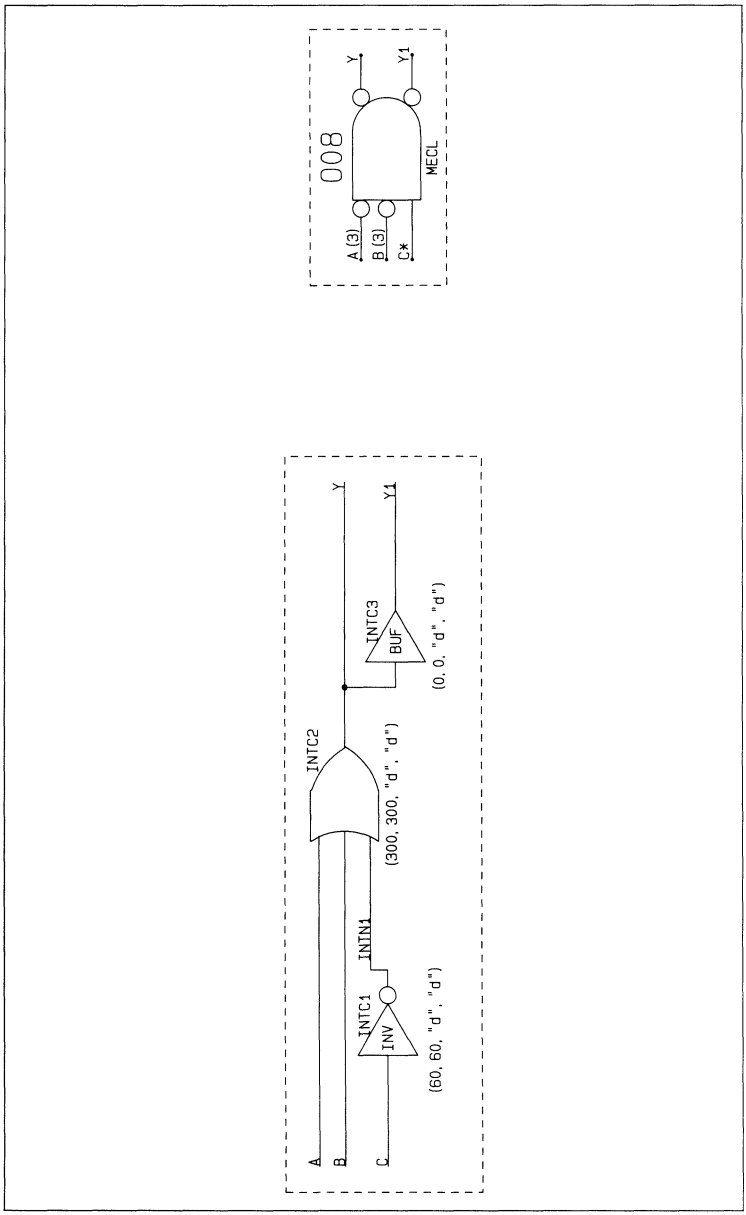
COMPONENT PLOTS

Plot 120



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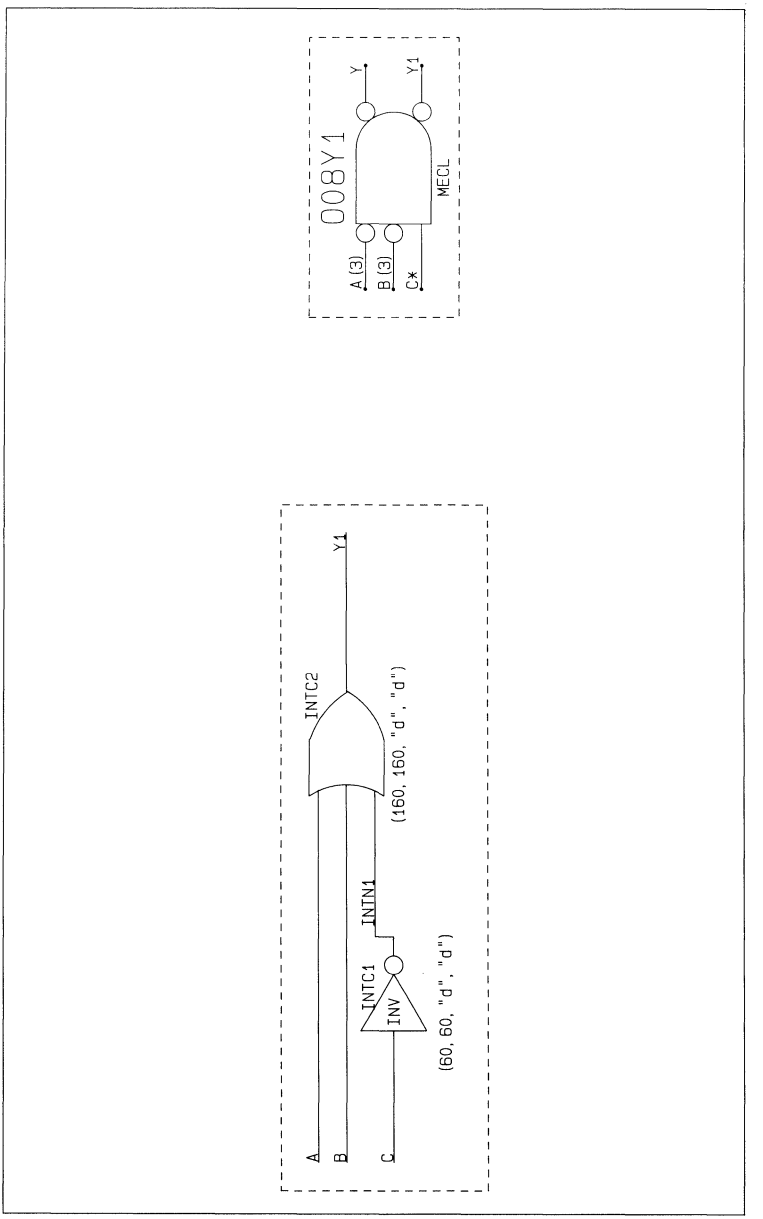
COMPONENT PLOTS

Plot 121



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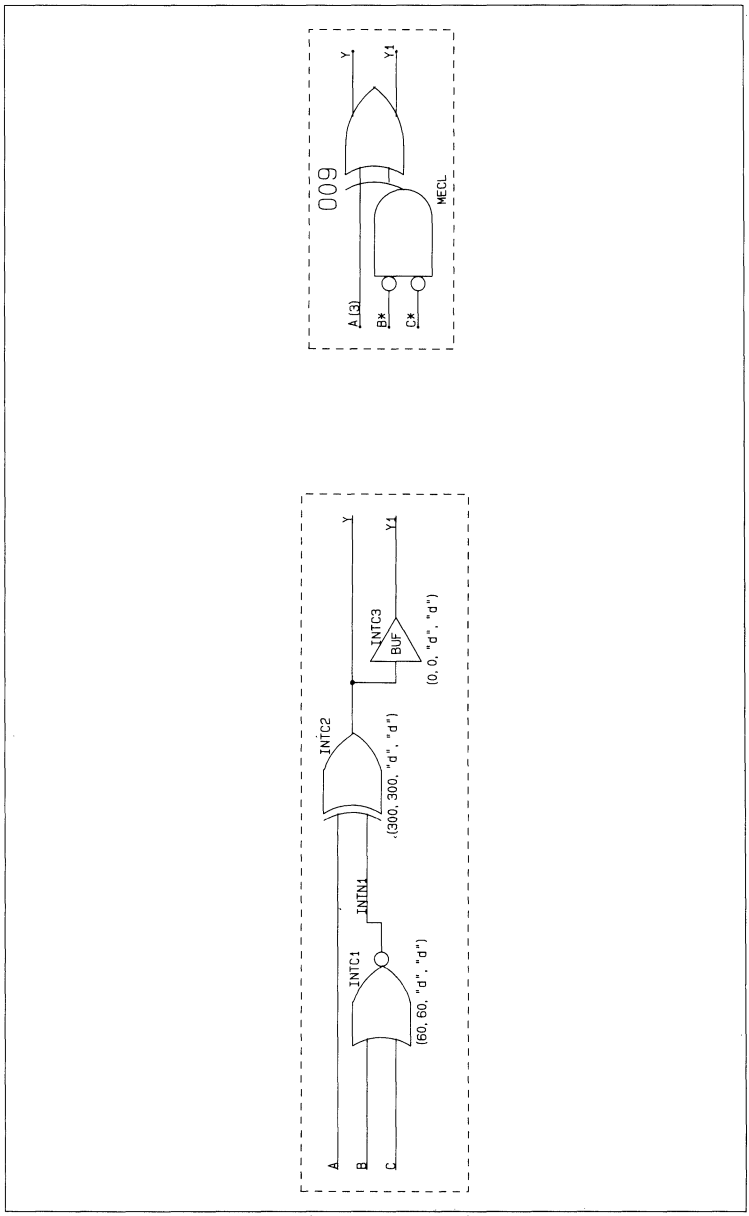
COMPONENT PLOTS

Plot 122



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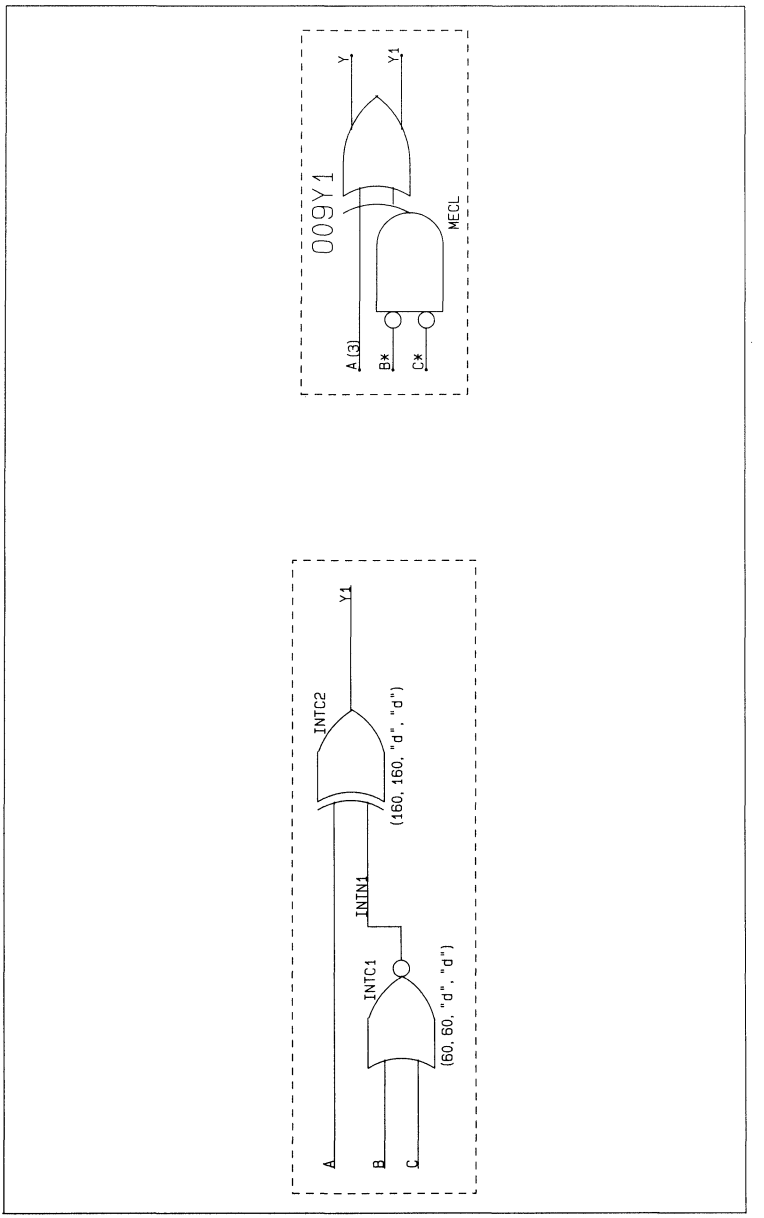
COMPONENT PLOTS

Plot 123



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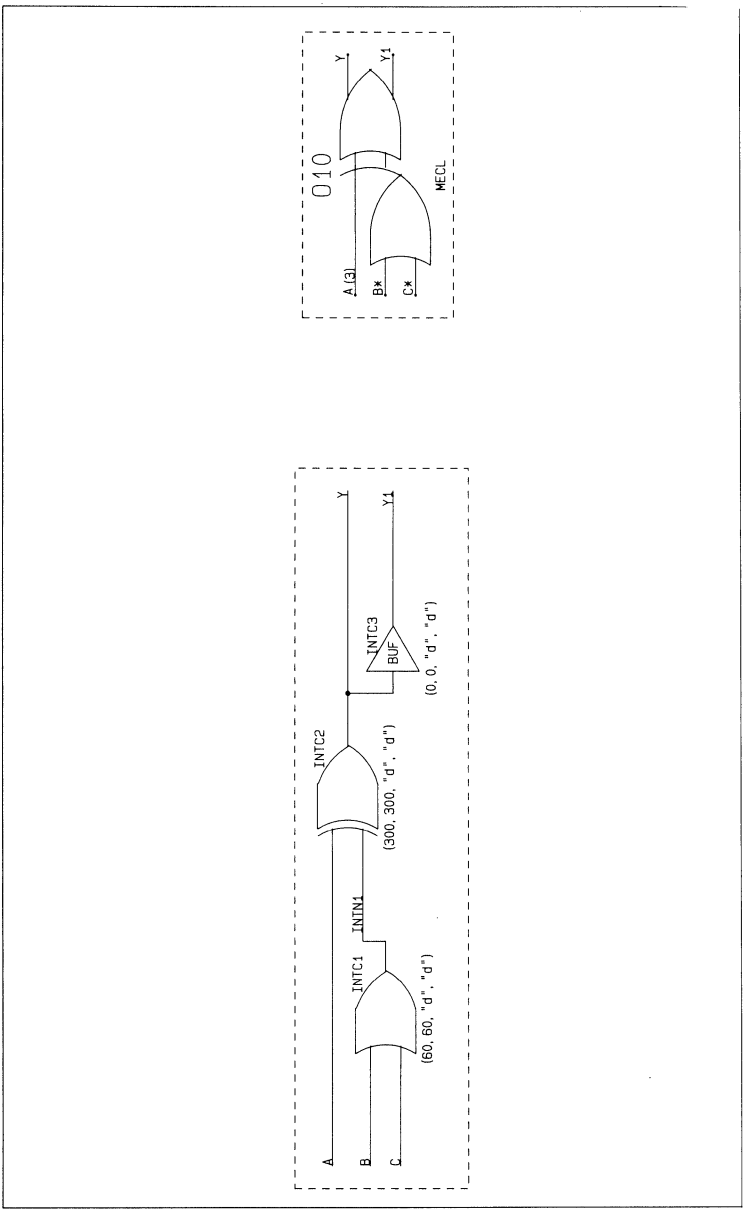
COMPONENT PLOTS

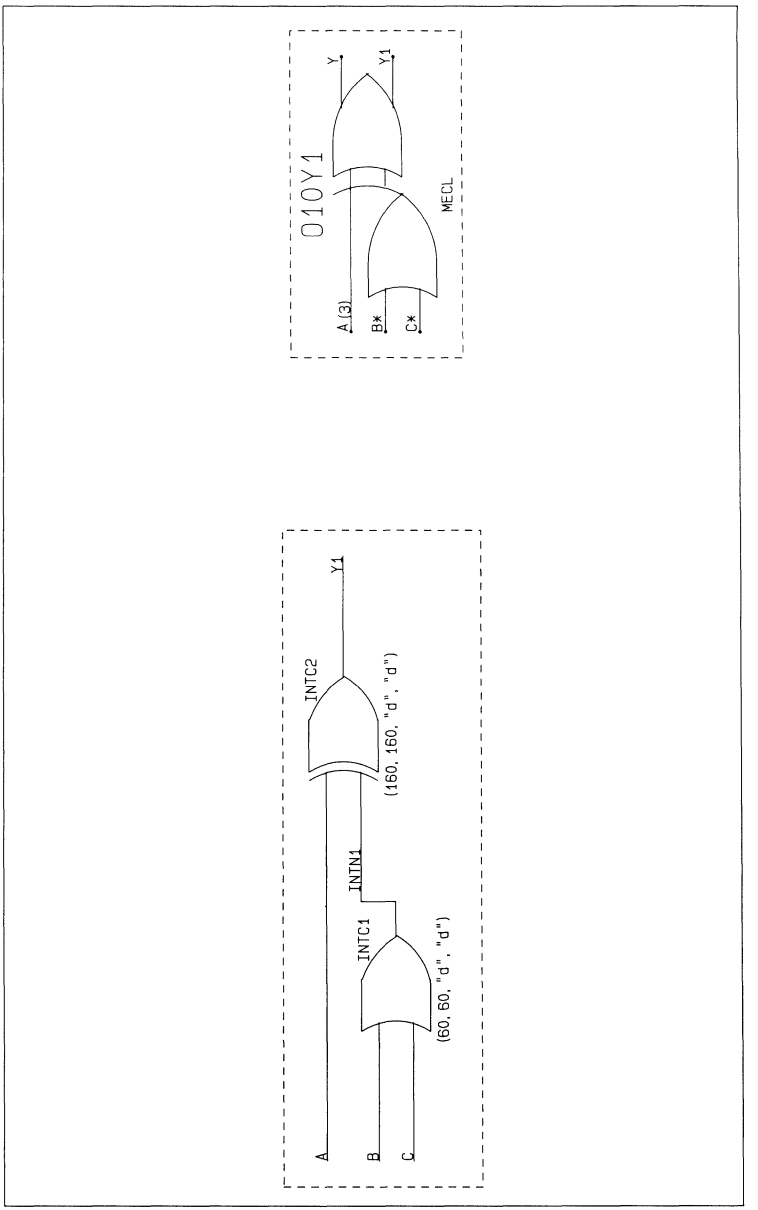
Plot 124



000-0145-00

COMPONENT PLOTS

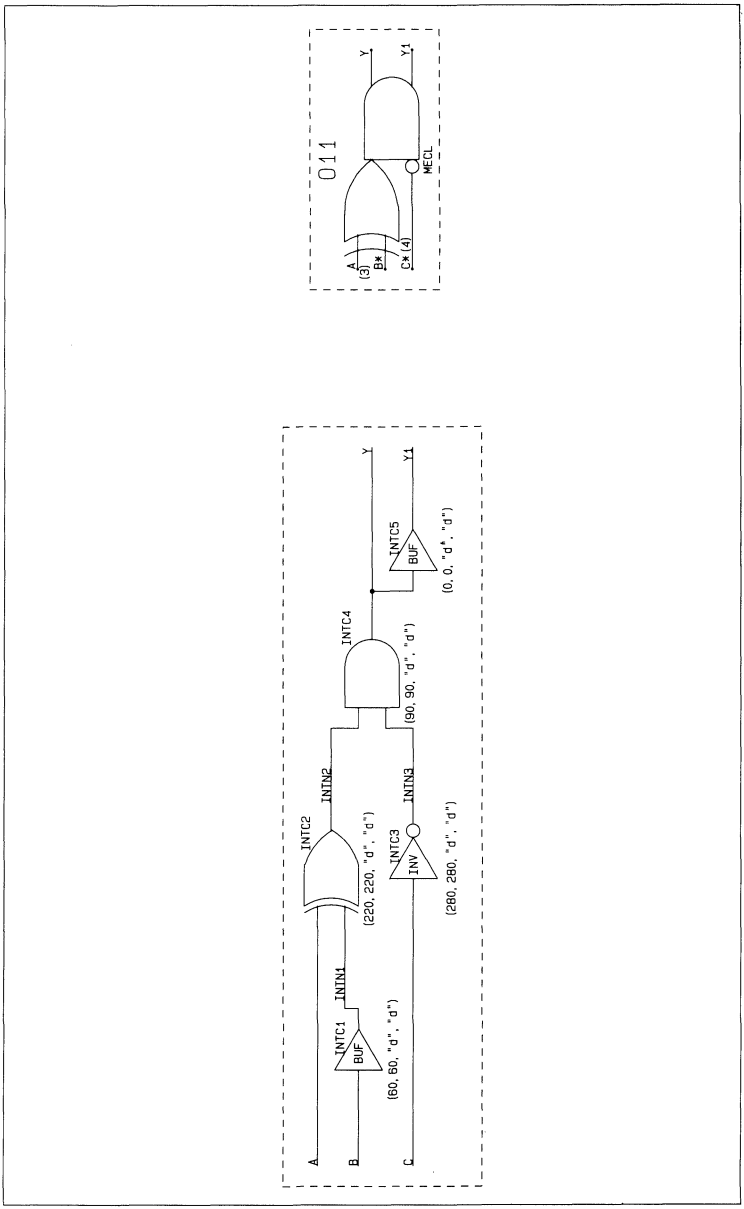
Plot 125



000-0145-00

COMPONENT PLOTS

Plot 126



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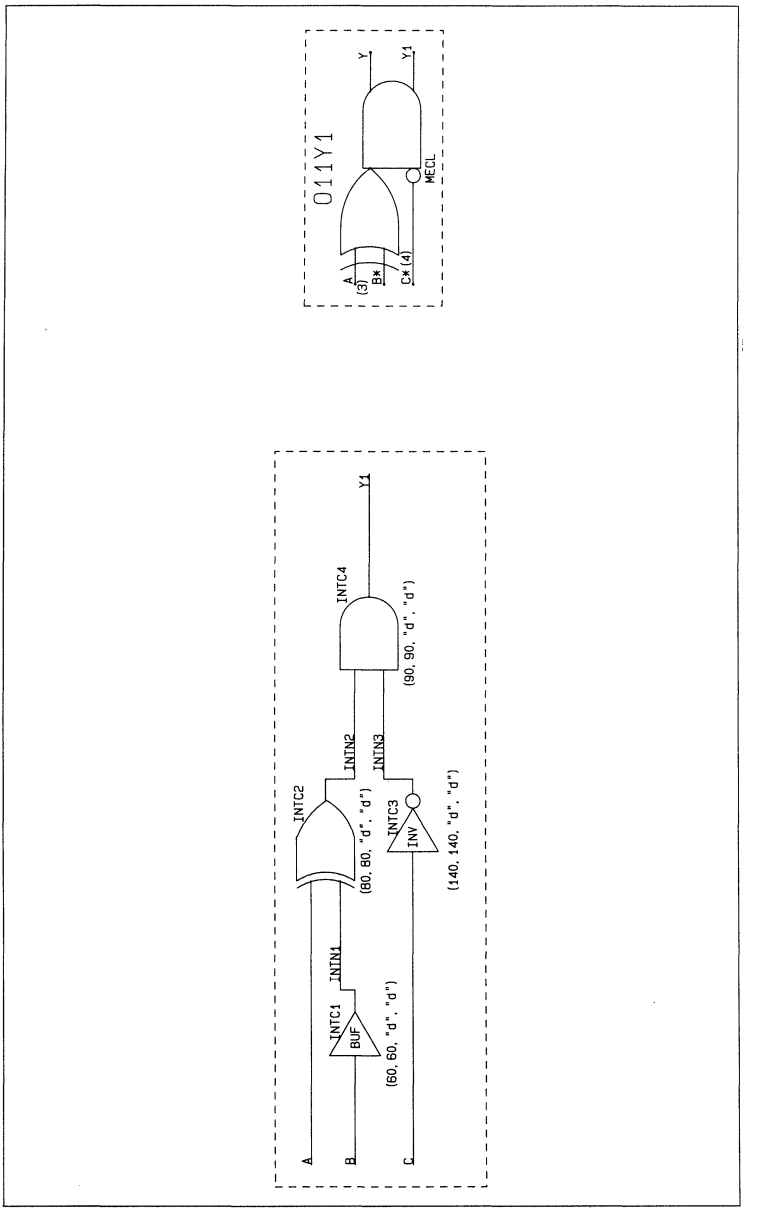
COMPONENT PLOTS

Plot 127



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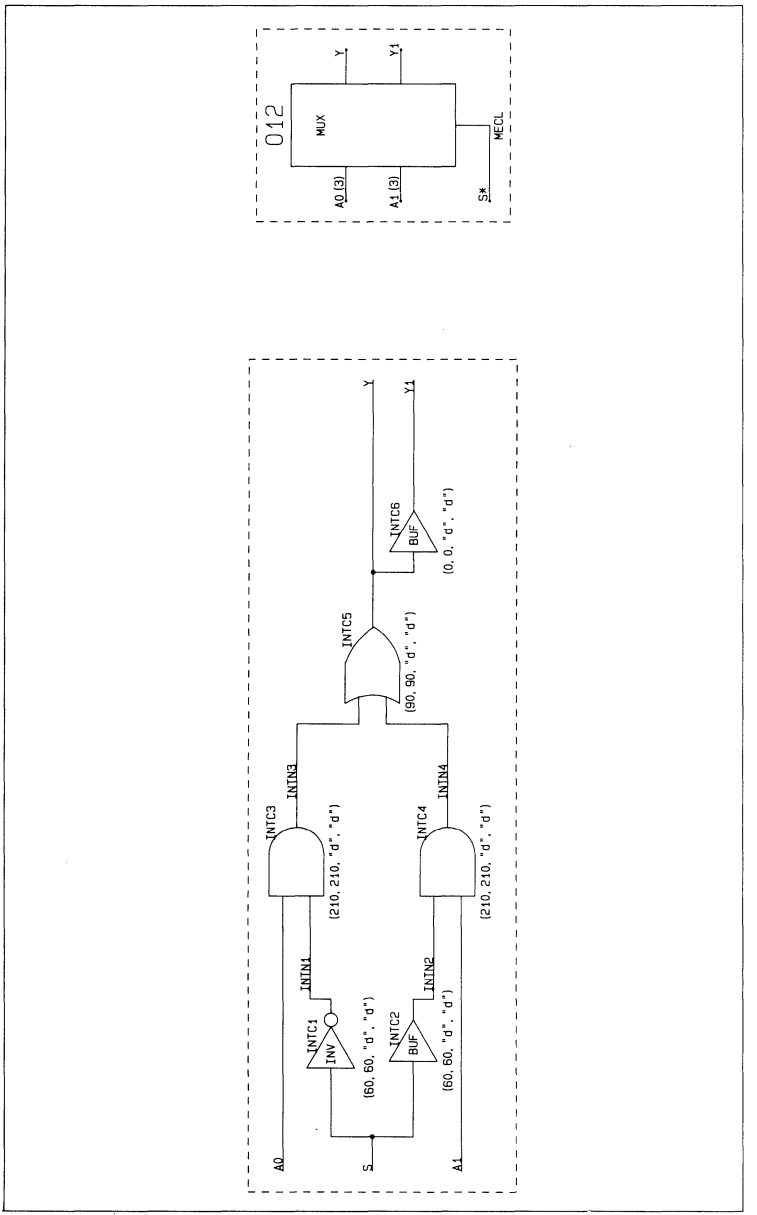
COMPONENT PLOTS

Plot 128



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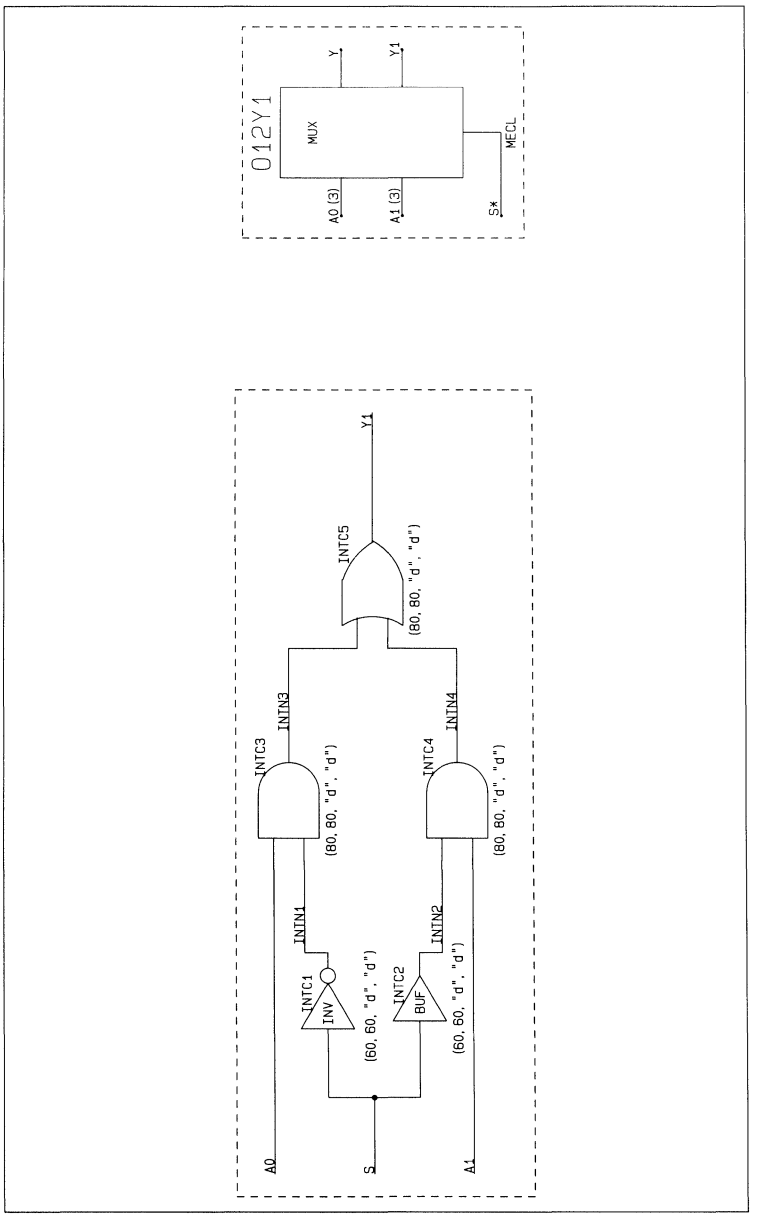
COMPONENT PLOTS

Plot 129



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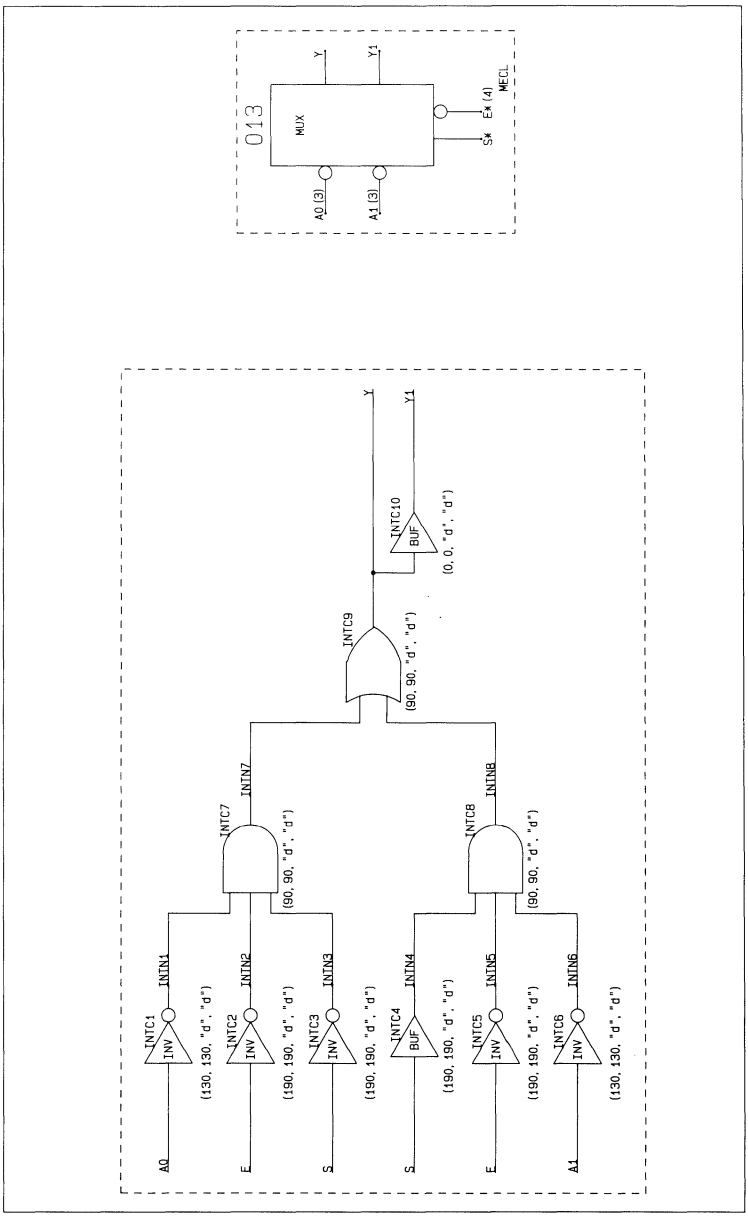
COMPONENT PLOTS

Plot 130



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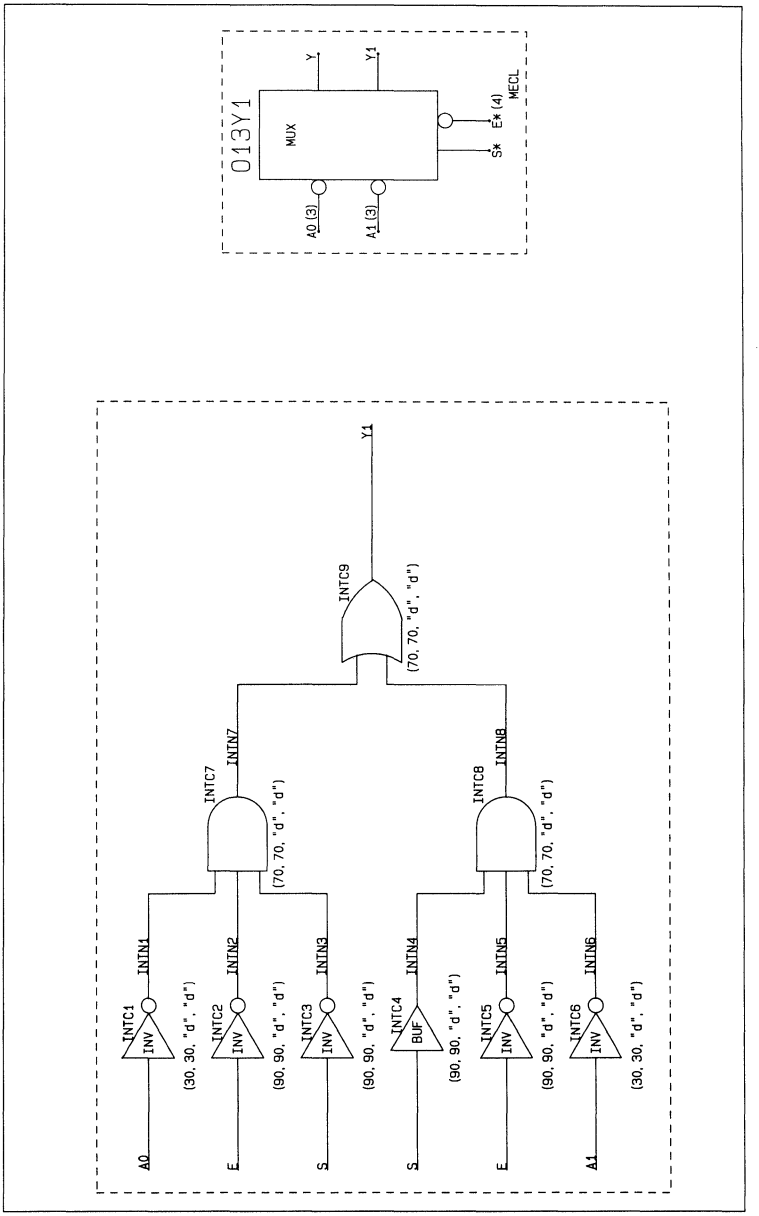
COMPONENT PLOTS

Plot 131



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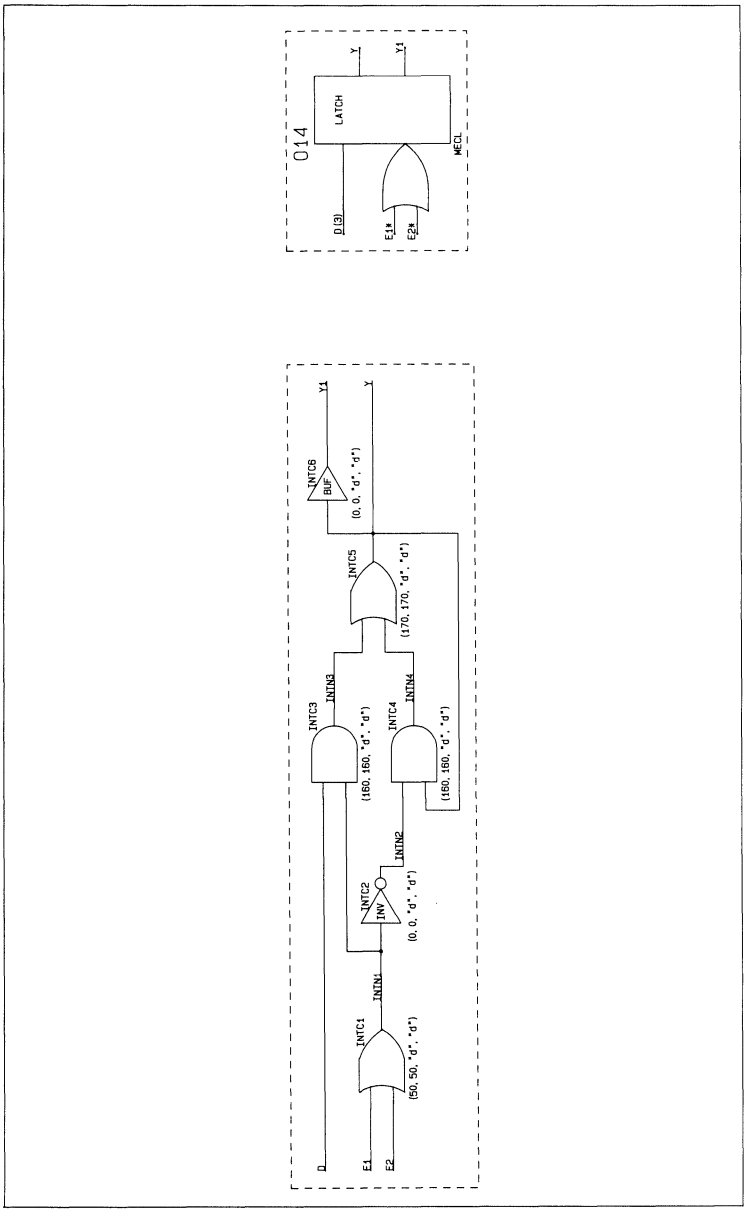
COMPONENT PLOTS

Plot 132



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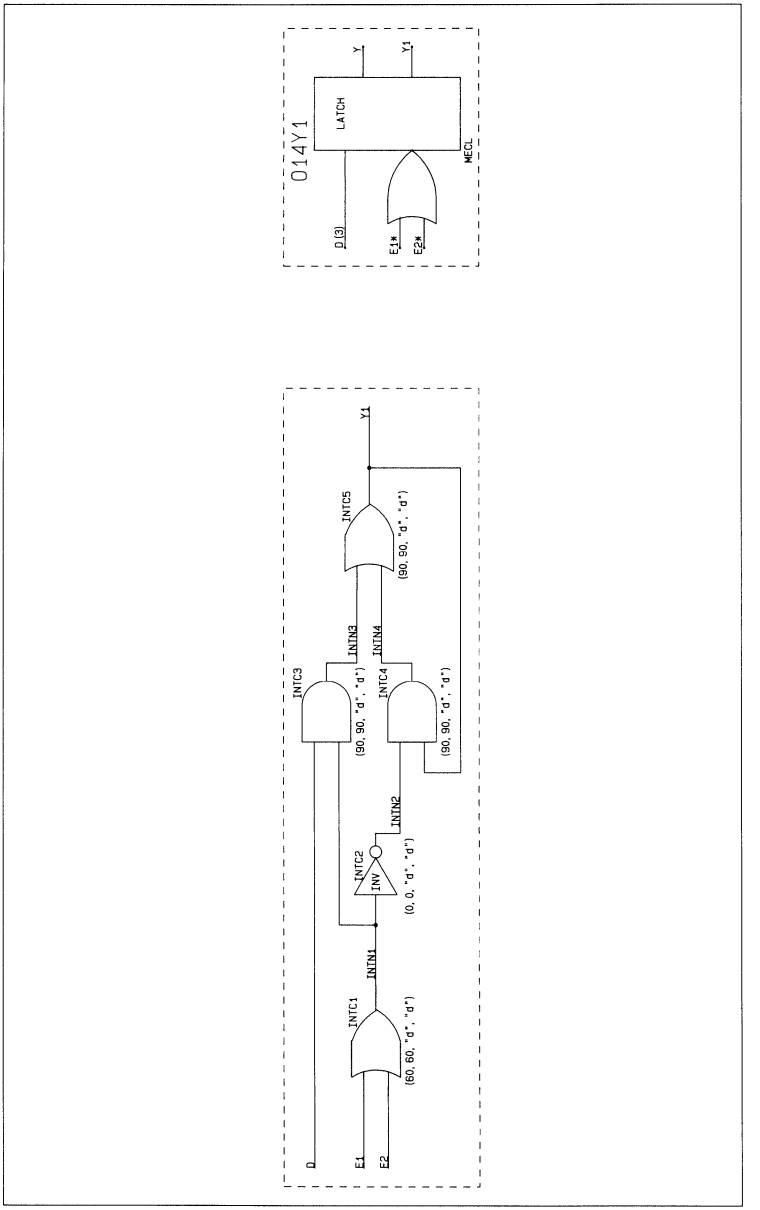
COMPONENT PLOTS

Plot 133



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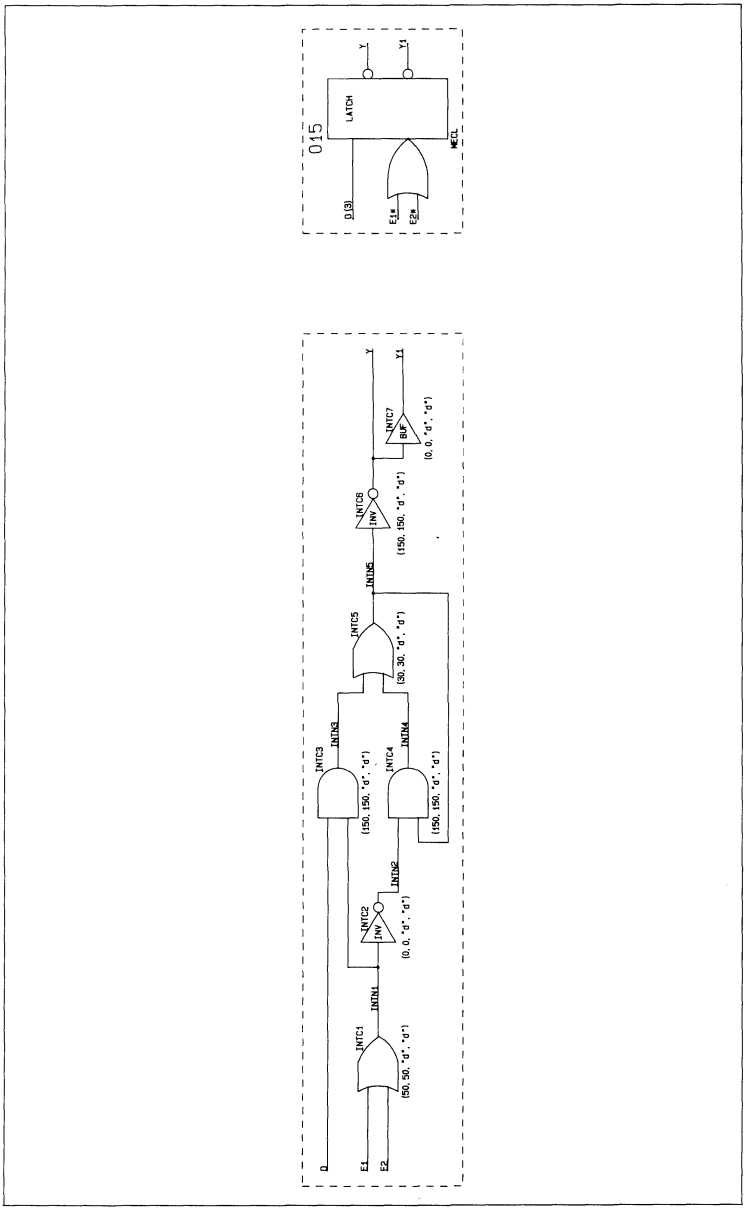
COMPONENT PLOTS

Plot 134



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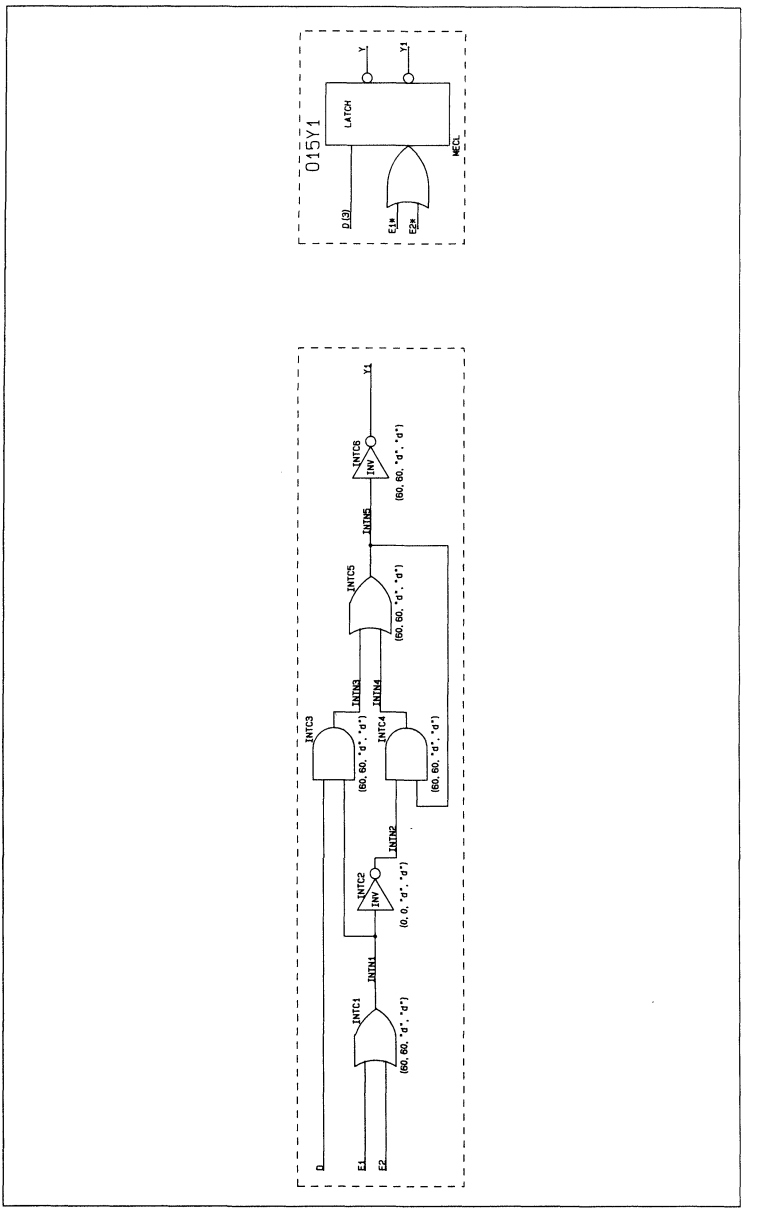
COMPONENT PLOTS

Plot 135



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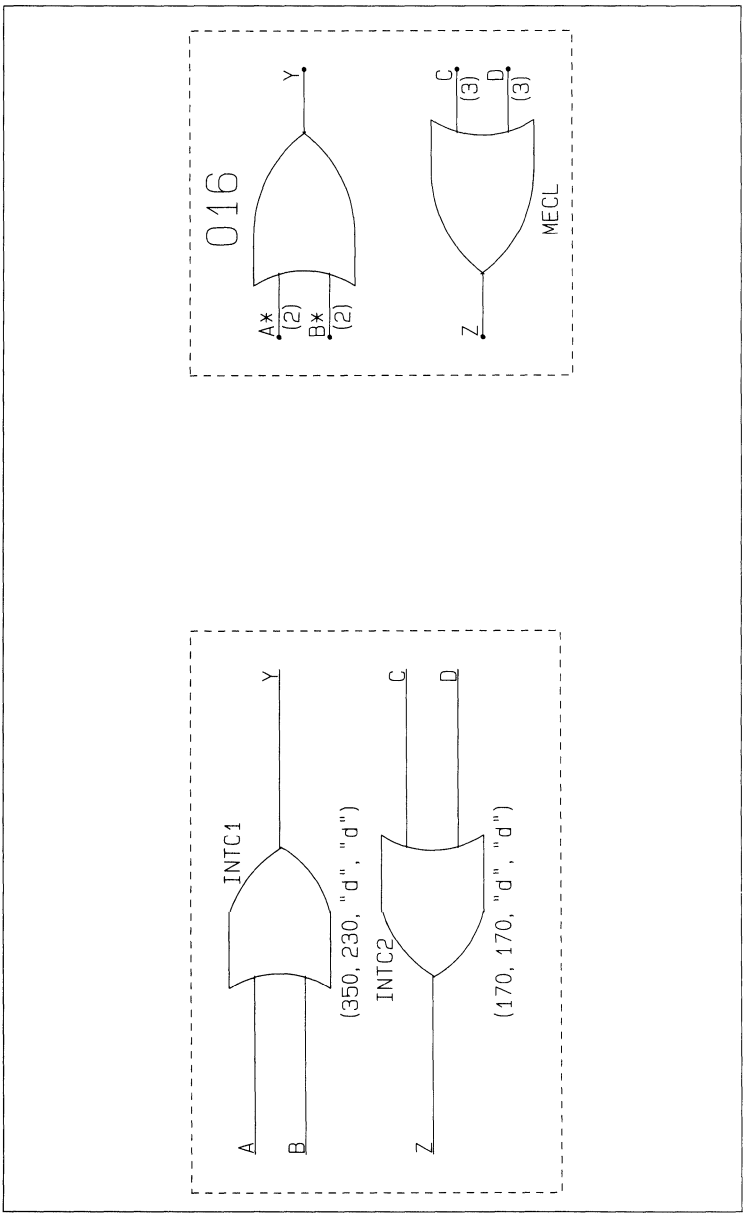
COMPONENT PLOTS

Plot 136



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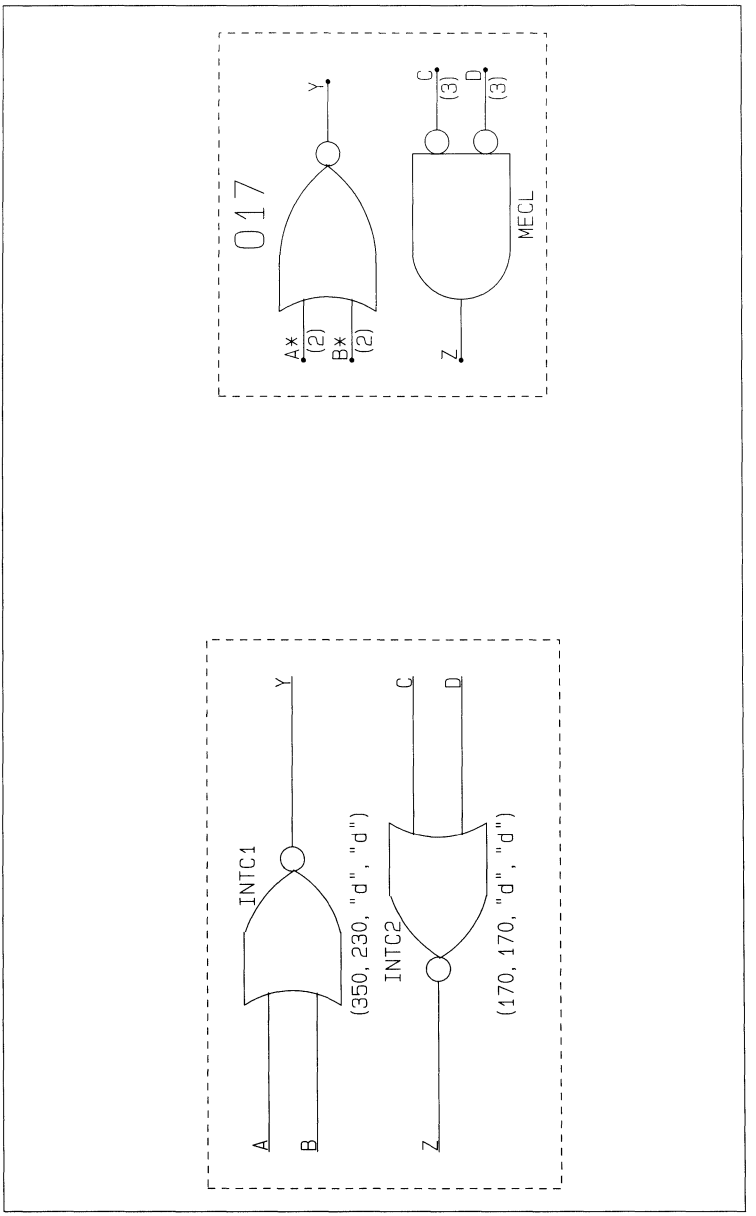
COMPONENT PLOTS

Plot 137



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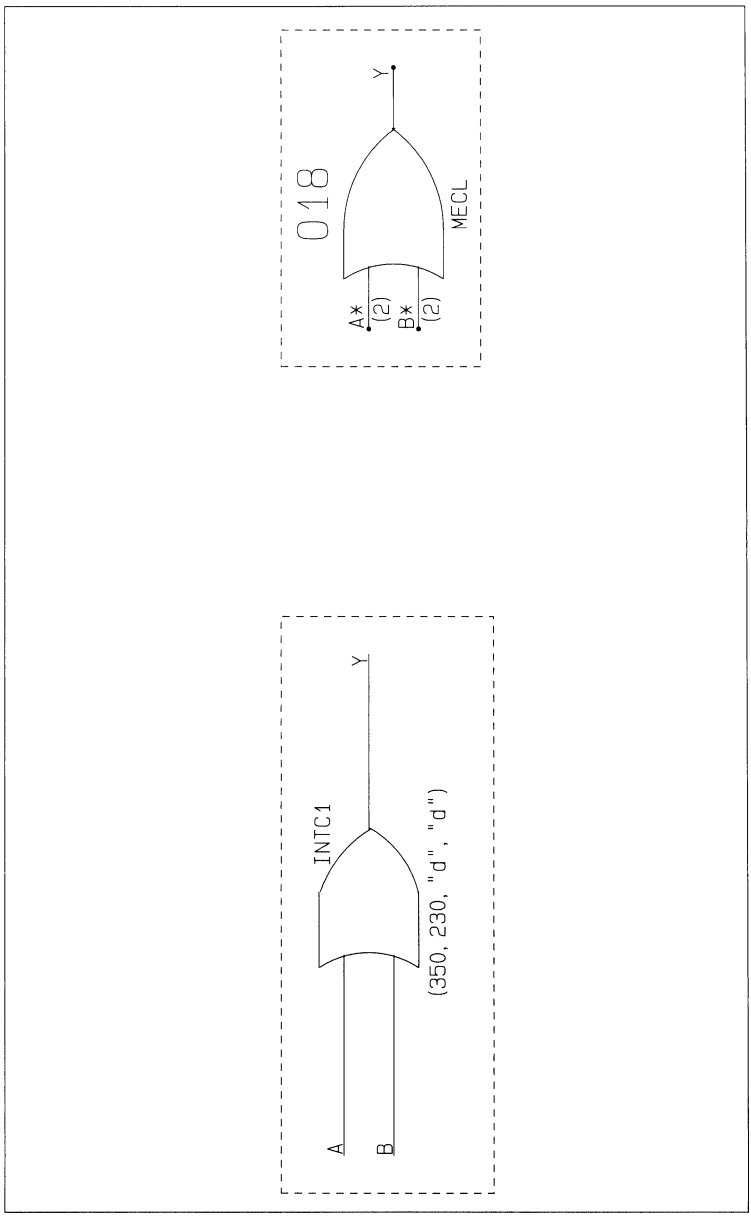
COMPONENT PLOTS

Plot 138



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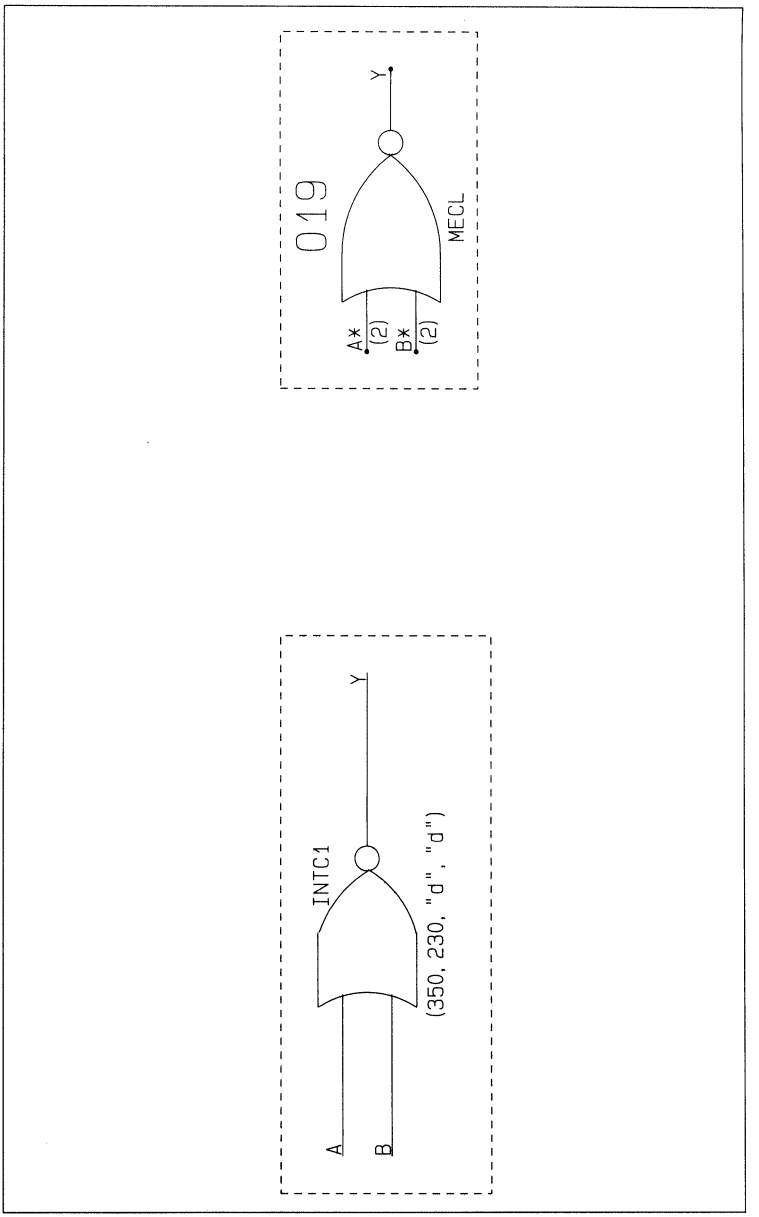
COMPONENT PLOTS

Plot 139



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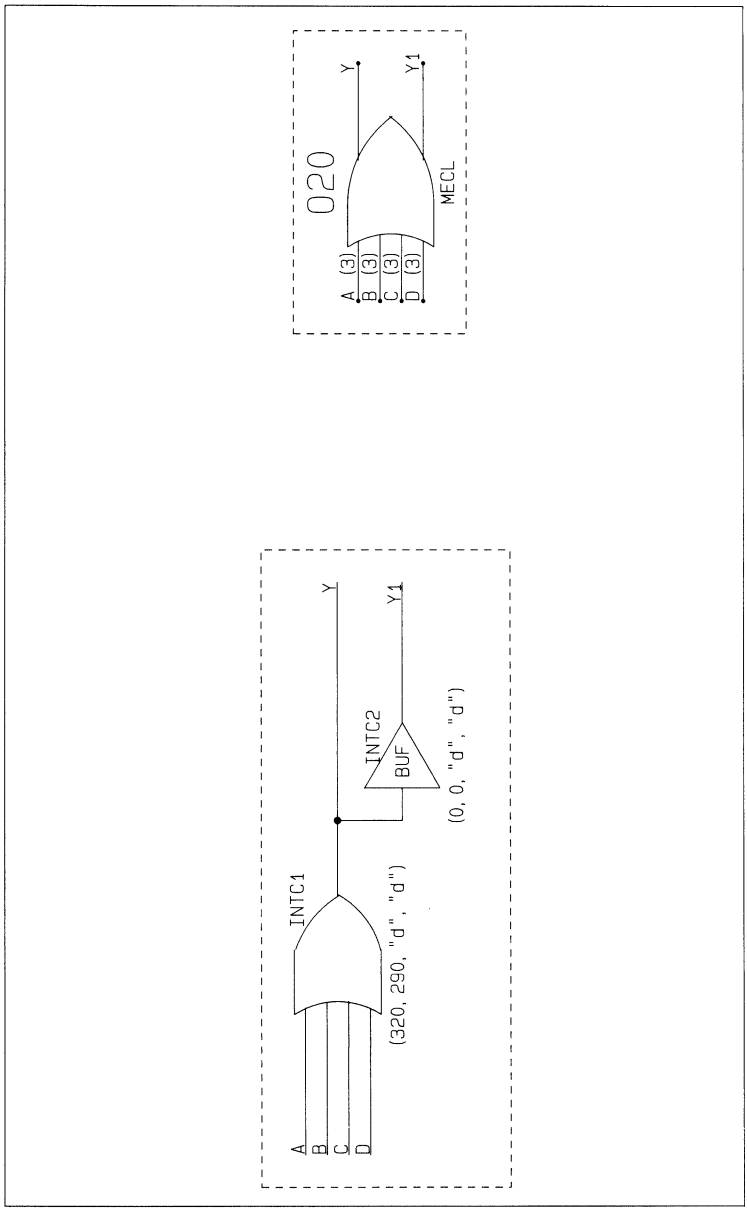
COMPONENT PLOTS

Plot 140



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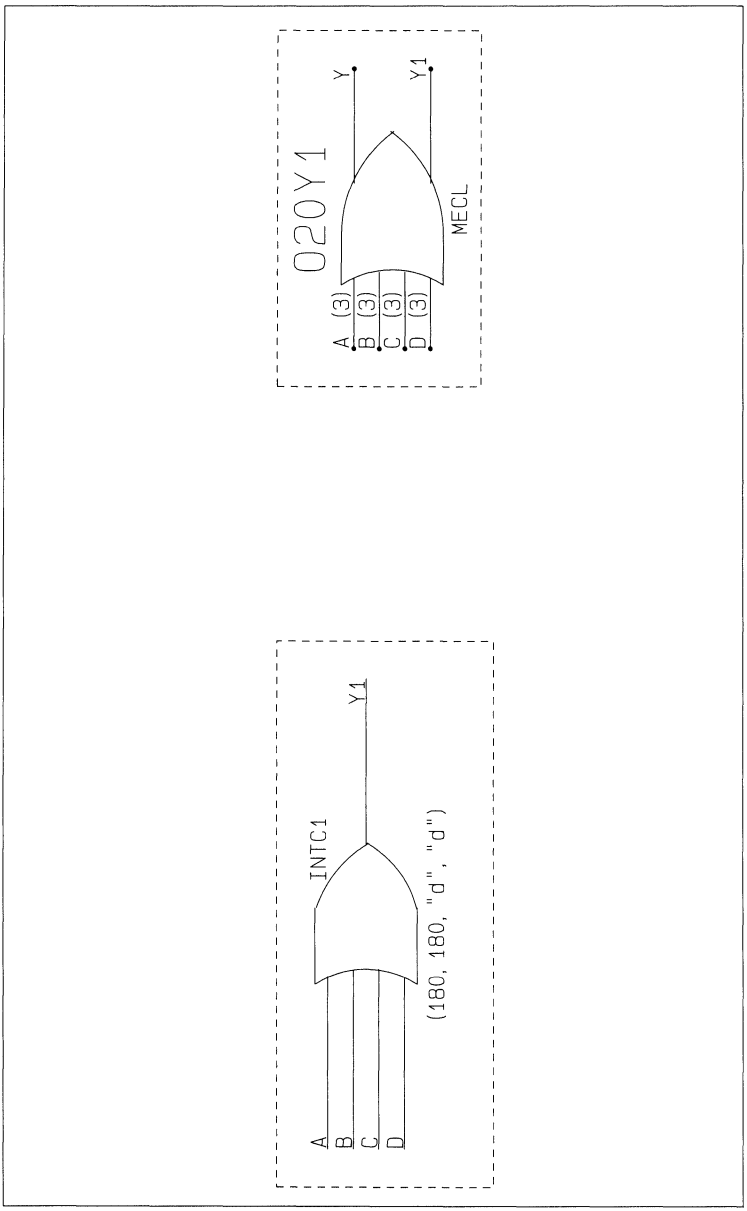
COMPONENT PLOTS

Plot 141



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COMPONENT PLOTS

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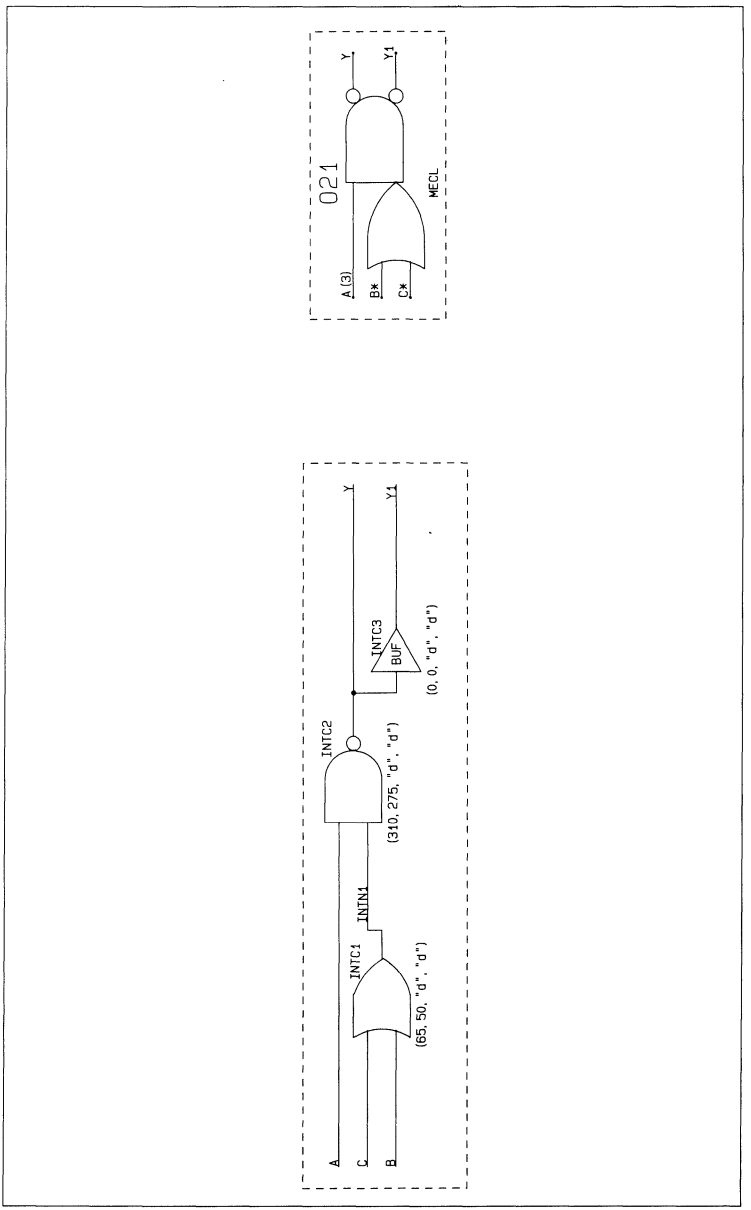

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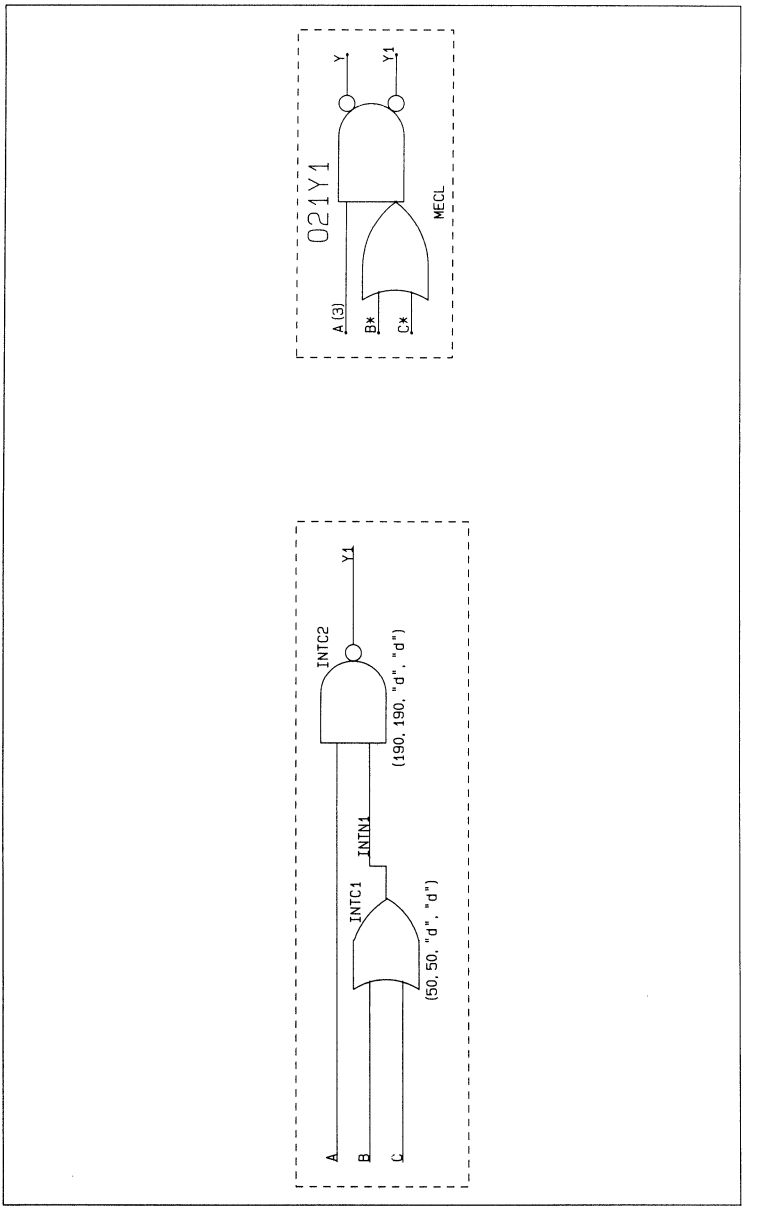
COMPONENT PLOTS

Plot 143



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COMPONENT PLOTS

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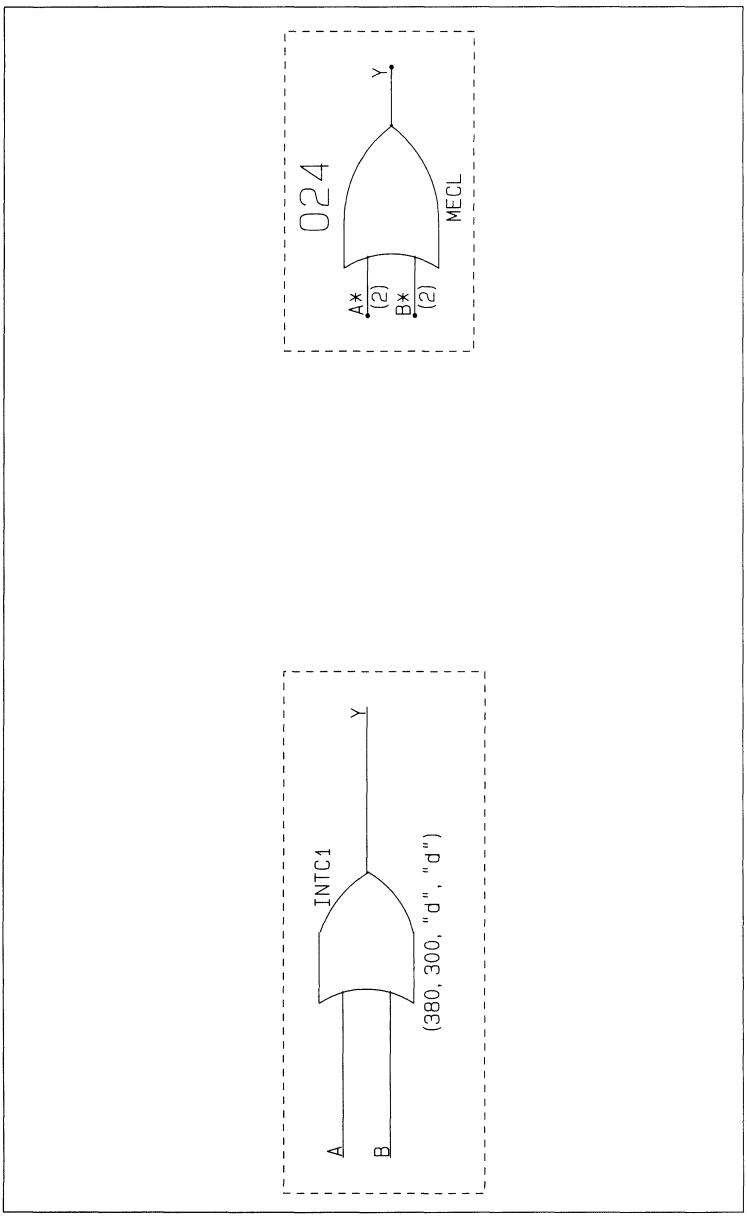

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COMPONENT PLOTS

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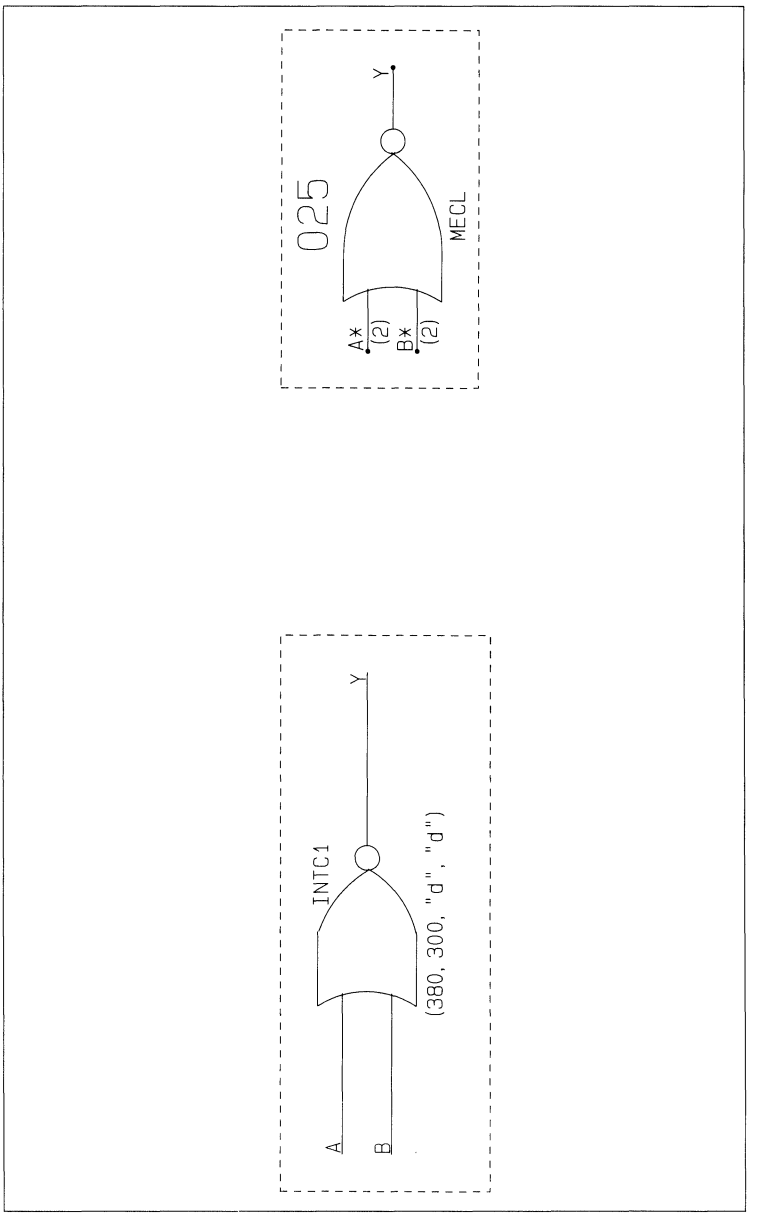

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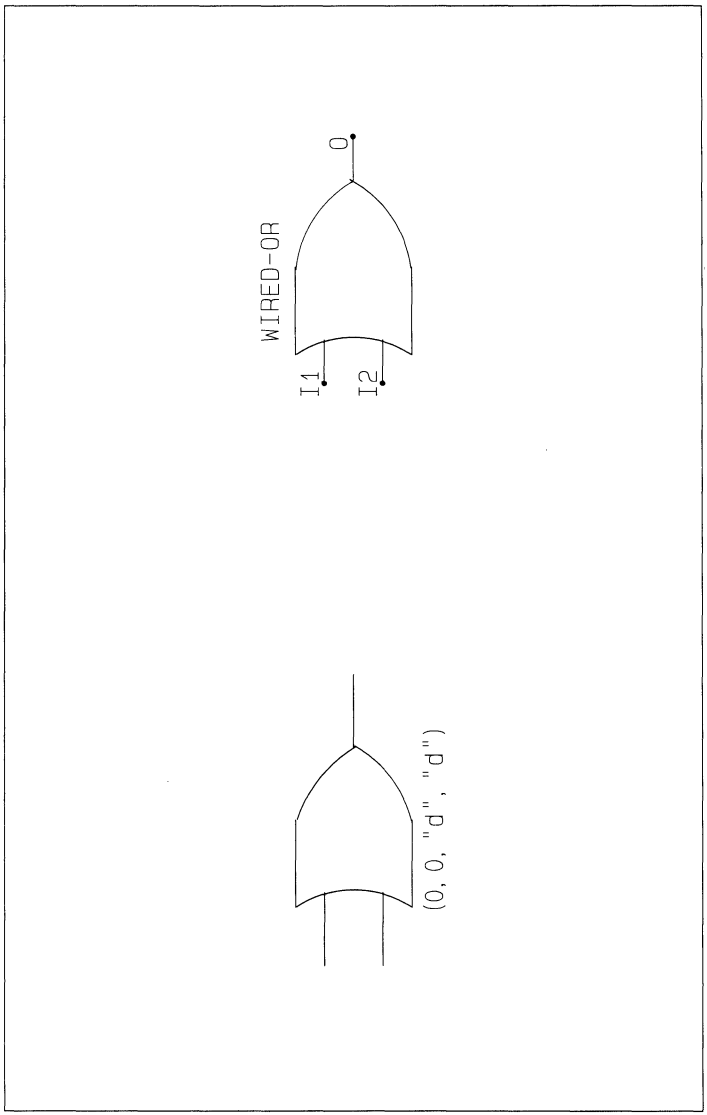
COMPONENT PLOTS

Plot 146



COMPONENT PLOTS

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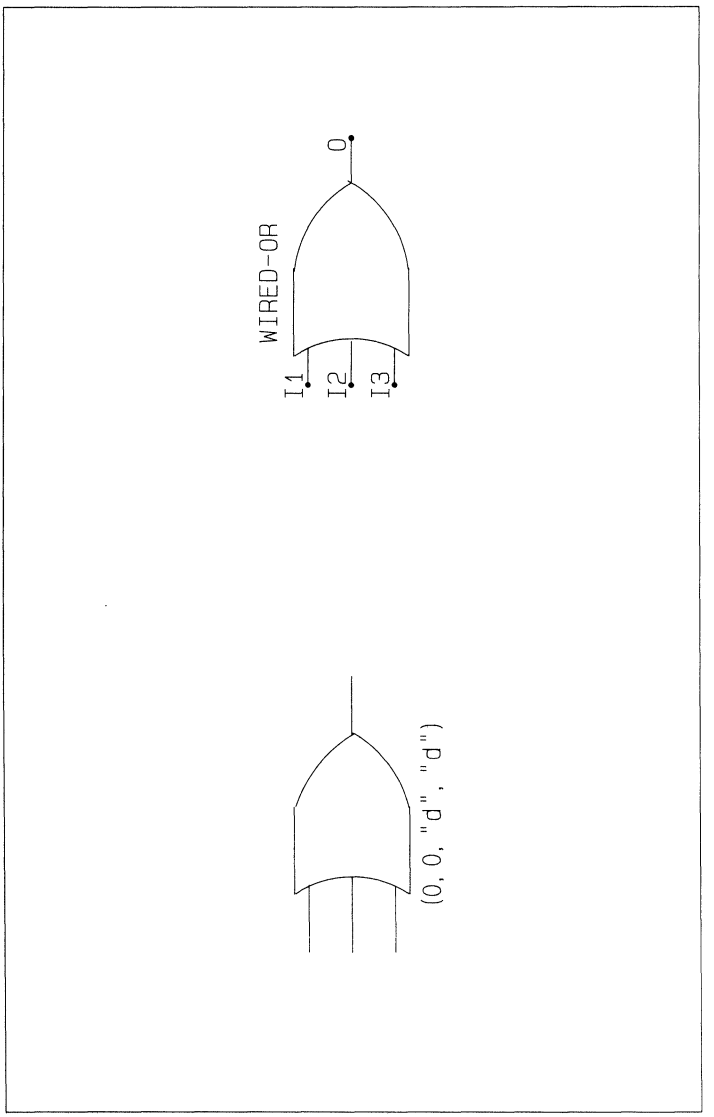

COMPONENT PLOTS

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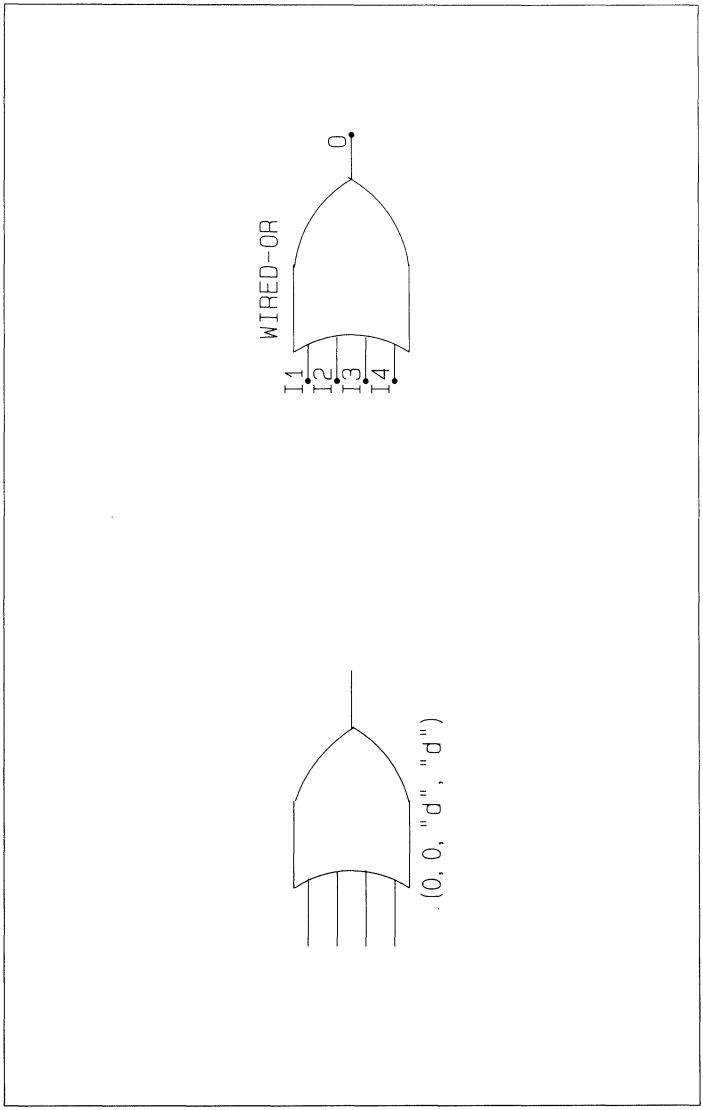

COMPONENT PLOTS

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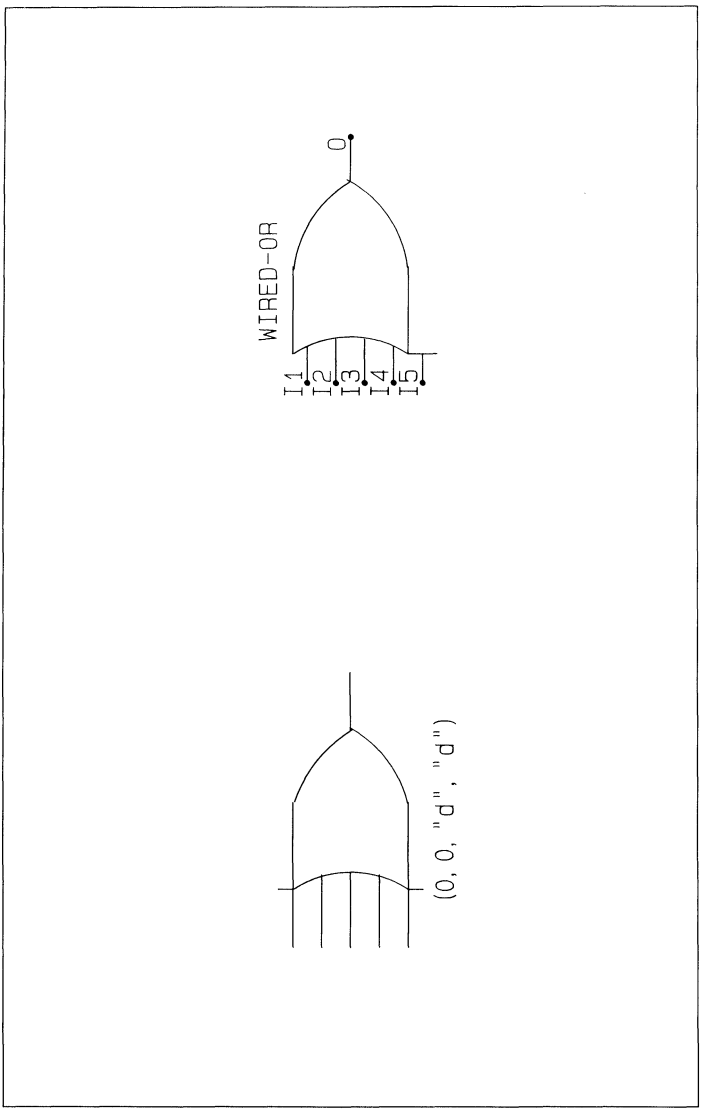

COMPONENT PLOTS

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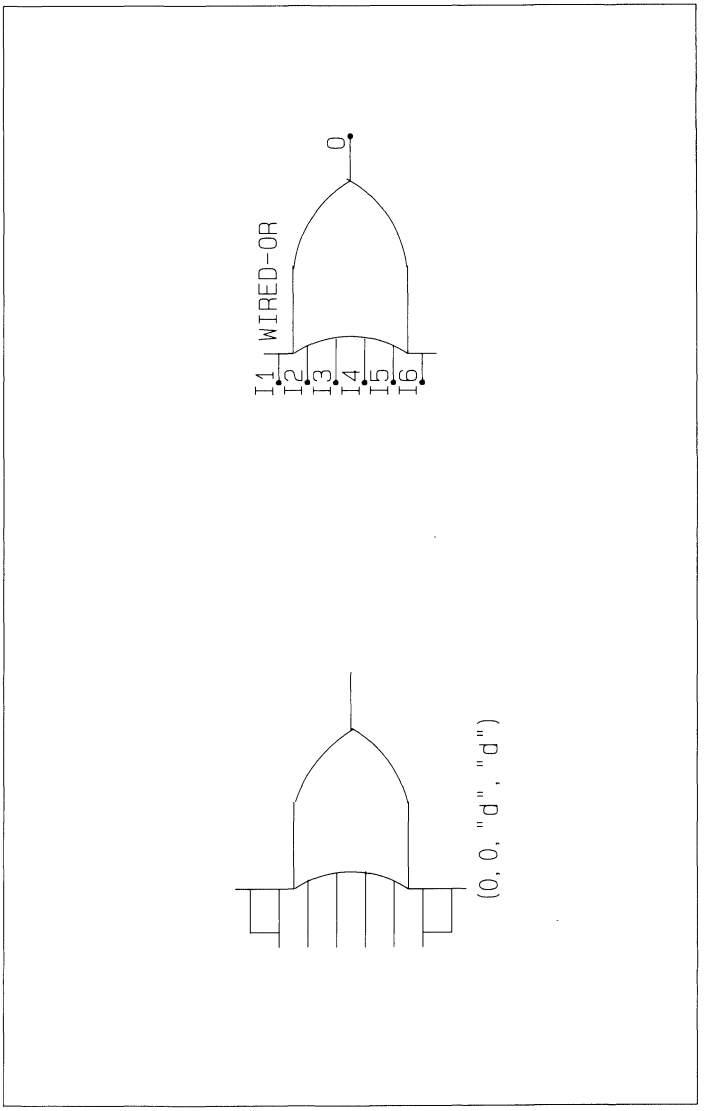

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COMPONENT PLOTS

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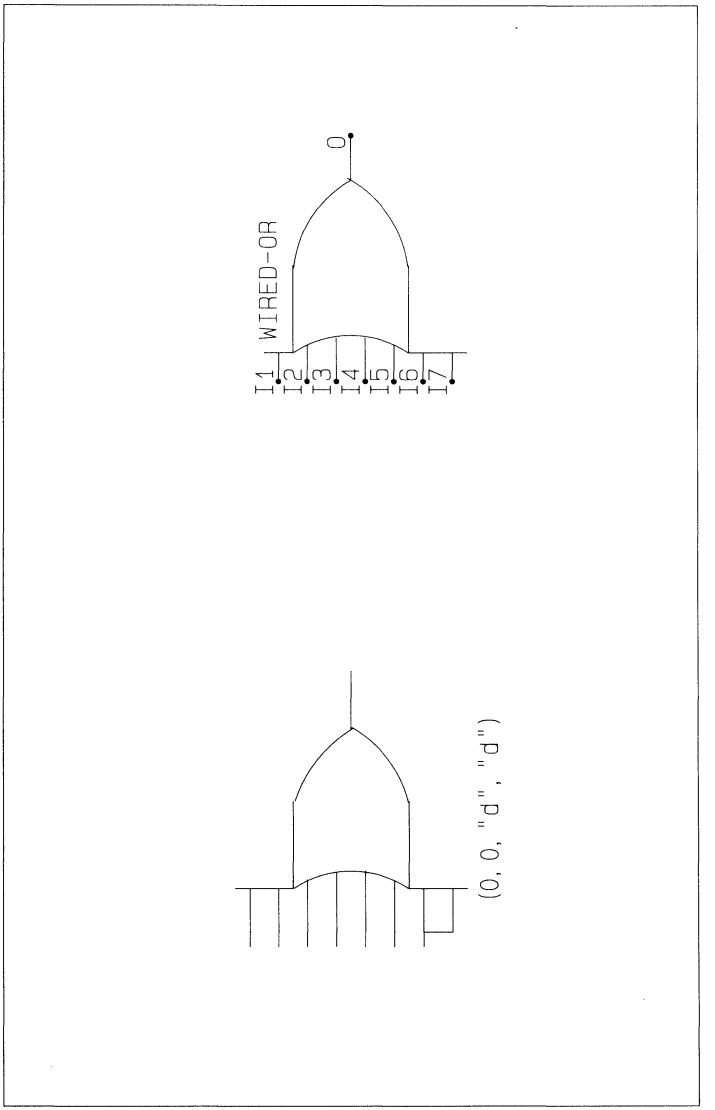

COMPONENT PLOTS

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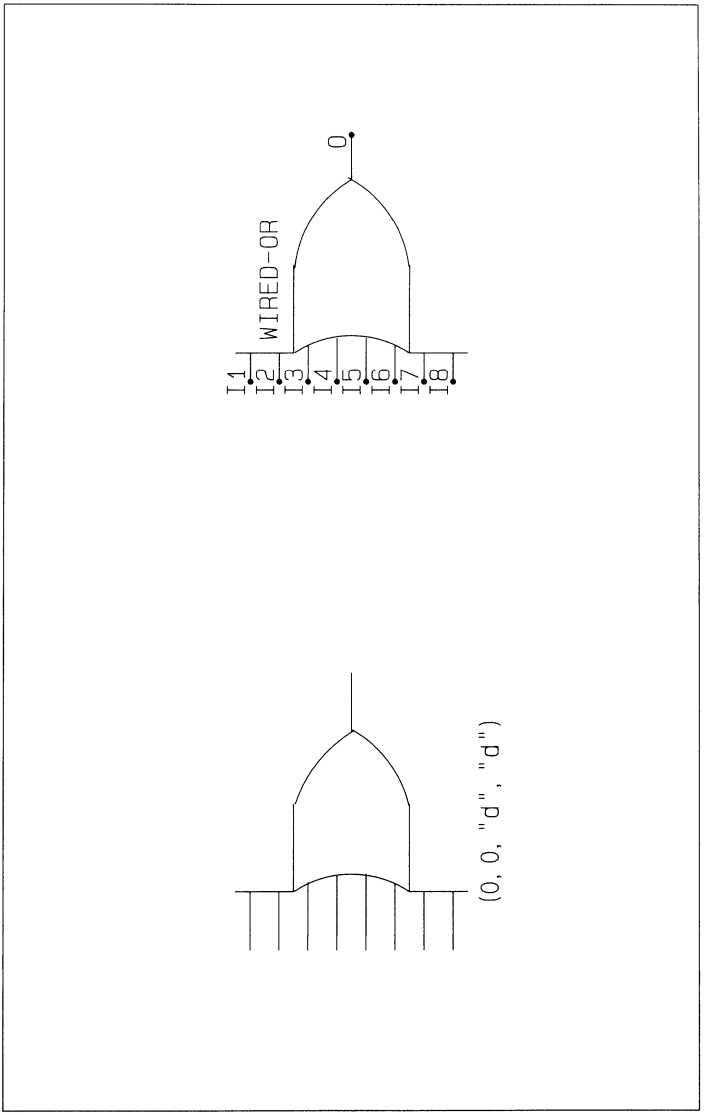

COMPONENT PLOTS

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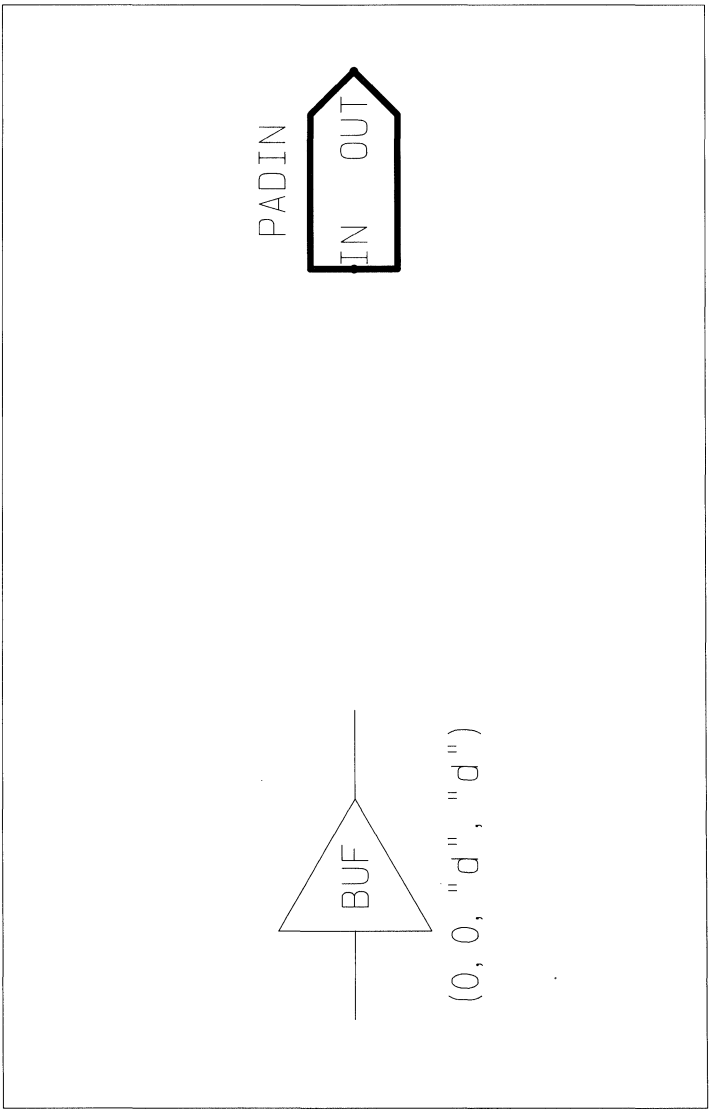

COMPONENT PLOTS

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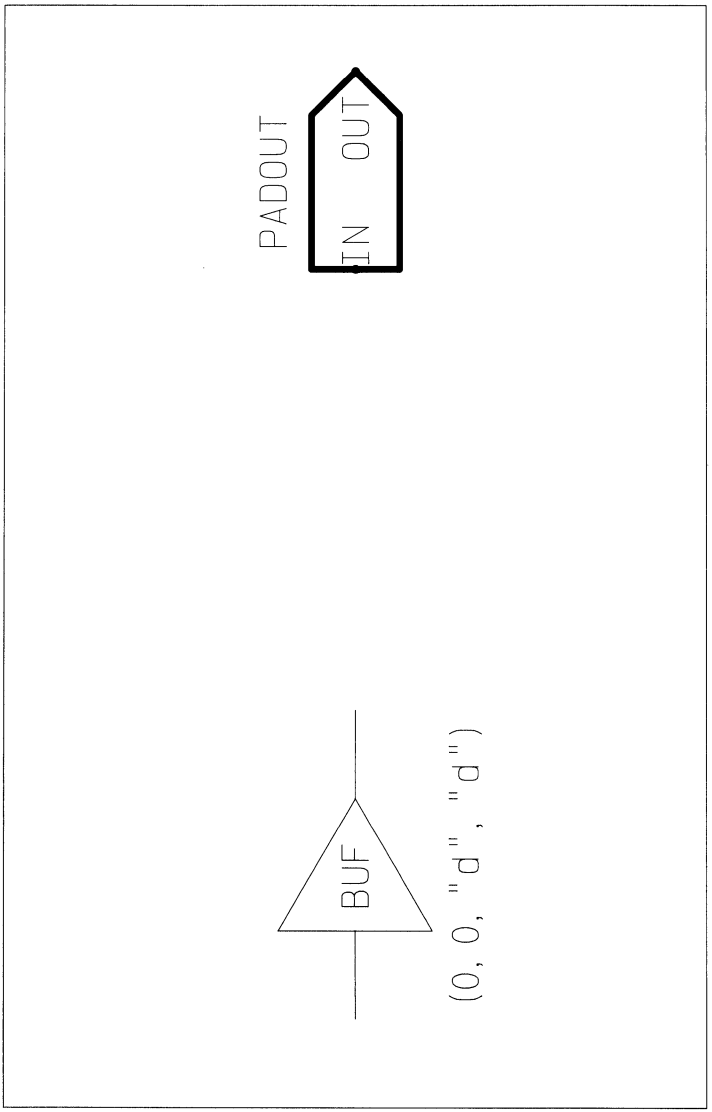

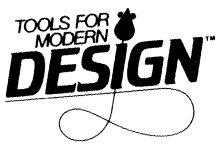
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