MODEL NO. T6840-9

SERIAL NO. 470215909

MODELS T6X40 AND T6X60
SYNCHRONOUS WRITE
SYNCHRONOUS READ
TAPE TRANSPORTS

PCC PERTEC

a division of Pertec Computer Corporation

9600 IRONDALE AVENUE, CHATSWORTH, CA 91311

OPERATING AND SERVICE MANUAL NO. 100884

FOREWORD

This manual provides operating and service instructions for the Synchronous Write/ Synchronous Read Tape Transport, Models T6X40 and T6X60, manufactured by PCC PERTEC, Chatsworth, California.

The content includes a detailed description, specifications, installation instructions, and checkout procedures for the transport. Also included is the theory of operation and preventive maintenance instructions. Section VII contains photo parts lists and schematics.

All graphic symbols used in logic diagrams conform to the requirements of ANSI Y32.14 and all symbols used in schematic diagrams are as specified in ANSI Y32.2.

SERVICE AND WARRANTY

This PERTEC product has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected wherever possible from manufacturer's off-the-shelf stock. Should a component fail, it may be readily replaced from PERTEC or your local supplier. The unit has been designed for plug-in replacement of circuit boards or major components which will ensure a minimum of equipment down time.

PERTEC warrants products of its manufacture to be free from defect in design, workmanship, and material under normal use and service for a period twelve (12) months, or in the case of flexible disk products 120 days, after the date of shipment. PERTEC agrees to repair or replace at its authorized repair center, without charge, all defective parts in systems which are returned for inspection to said center within the applicable warranty period; provided such inspection discloses that the defects are as specified above, and provided further the equipment has not been altered or repaired other than with authorization from PERTEC and by its approved procedures, not been subjected to misuse, improper maintenance, negligence or accident, damaged by excessive current or otherwise had its serial number or any part thereof altered, defaced or removed. All defective items released hereunder shall become the property of seller. THIS WARRANTY IS IN LIEU OF, AND BUYER WAIVES, ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THOSE OF MERCHANTABILITY OR FITNESS FOR PURPOSE.

Please read the instruction manual thoroughly as to installation, operation, maintenance, and component reference list. Should you require additional assistance in servicing this equipment, please contact PERTEC SERVICE — our trained service staff will be pleased to assist you.

PERTEC SERVICE

North America:

California & Canada — (213) 998-7676
All other — TOLL FREE (800) 423-5156
TWX (910) 494-2093

Europe:

10 Portman Road
Reading, Berkshire RG3 1DU
England
Phone Reading (734) 582-115
TWX (851) 847-101

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides a physical description, functional description, and specifications for the Synchronous Write/Synchronous Read Tape Transport, Models T6X40 and T6X60, manufactured by PCC PERTEC, Chatsworth, California.

1.2 PURPOSE OF EQUIPMENT

The tape transport has the capability of recording digital data on either 7- or 9-track magnetic tape at tape speeds of up to 45 ips in an ANSI and NRZI IBM-compatible format. The data can be completely recovered when the tape is played back on an IBM digital tape transport or its equivalent.

The transport can also synchronously read either 7- or 9-track magnetic tape at a speed up to 45 ips, which has been recorded in a NRZI IBM-compatible format.

The T6X40 transport is equipped with a dual-stack head which has the read and write heads separated by 0.15 inch. The dual-stack head enables simultaneous read and write operations to be performed so data just recorded by the write head can be read by the read head after the tape has moved on approximately 0.15 inch. This technique allows writing and checking of data in a single pass.

The T6X60 transport utilizes a single head for both reading and writing data. Therefore, changing from the Read to the Write mode is accomplished through internal switching logic when one mode or the other is selected.

The transport operates directly from 115v ac or 230v ac, single phase, 48 to 400 Hz power.

1.3 PHYSICAL DESCRIPTION OF EQUIPMENT

The Model T6X40 Transport is shown in Figure 1-1 (Model T6X60 is identical in appearance). Tape reels up to 10½ inches in diameter may be used. All electrical and mechanical components necessary to operate the transports are mounted on the deck which is designed to be hinge mounted in a standard 19-inch EIA rack.

The transport is equipped with an erase head which is automatically activated when writing.

Access to the printed circuit boards is from the rear. The dust cover, which is hinged, protects the magnetic tape, magnetic head, capstan, and other tape path components from dust and other contaminants.

The operational controls, which are illuminated when the relevant function is being performed, are mounted on a control panel on the front trim and are accessible when the dust cover door is closed. Power is supplied through a strain-relieved cord having a standard 3-pin plug. Interface signals are routed through three printed circuit connectors that plug directly into the PCBAs.

In certain transports, a fourth PCBA is used. This is the EOT/BOT Amplifier which is mounted on the Write Lockout assembly bracket at the rear of the tape deck.

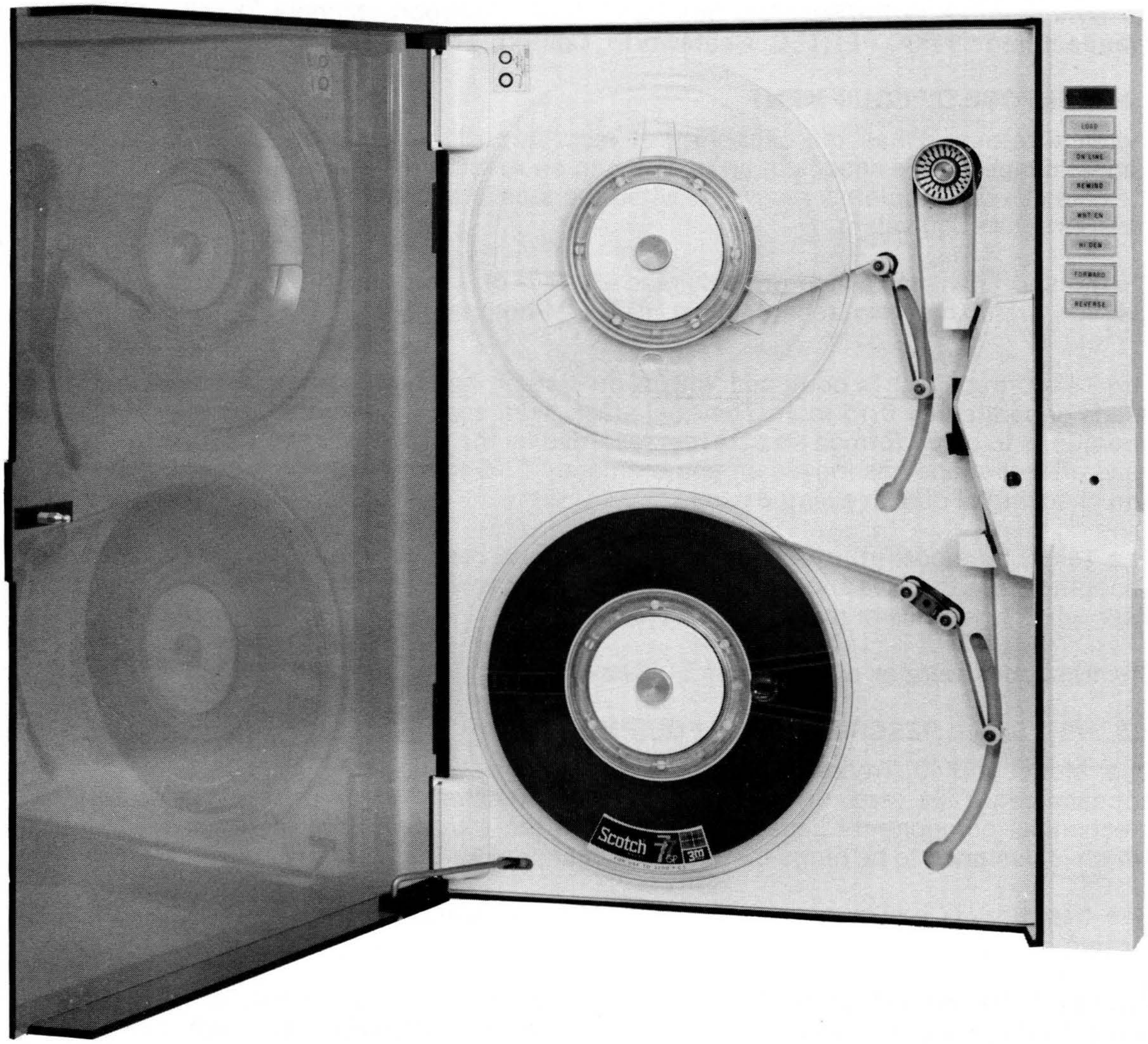


Figure 1-1. Model T6X40 Tape Transport

1.4 FUNCTIONAL DESCRIPTION

Figures 1-2 and 1-3 are block diagrams of the T6X40 and T6X60 models, respectively. The transports use a single capstan drive for controlling tape motion during their Synchronous Write, Synchronous Read, and Rewind modes. Tape is under a constant tension of 8 ounces, thus eliminating the possibility of tape cinch when the tape reel is played on a computer transport.

The capstan is controlled by a velocity servo. The velocity information is generated by a dc tachometer that is directly coupled to the capstan motor shaft. The servo voltage is proportional to the angular velocity of the capstan. This voltage is compared to the reference voltage from the ramp generators by applying operational amplifier techniques and the difference is used to control the capstan motor. This capstan control technique gives precise control of tape accelerations and tape velocities, thus minimizing tape tension transients.

During a writing operation, tape is accelerated in a controlled manner to the required velocity. This velocity is maintained constant and data characters are written on the tape at a constant rate such that:

$$\text{Bit Density} = \frac{\text{Character Rate}}{\text{Tape Velocity}}$$

When data recording is complete, tape is decelerated to zero velocity in a controlled manner.

Since the writing operation relies on a constant tape velocity, Inter-Record Gaps (IRGs) (containing no data) must be provided to allow for tape acceleration and deceleration periods. Control of tape motion to produce a defined IRG is provided externally by the customer controller, in conjunction with the tape acceleration and deceleration characteristics defined within the transport.

During a reading operation, tape is accelerated to the required velocity. The acceleration time is such that the tape velocity becomes constant before data signals are received.

Seven or nine data channels are presented to the interface. They are accompanied by a READ DATA STROBE (RDS) pulse derived by conventional ORed clock techniques.

The end of a record is detected in the customer controller by using *Missing Pulse Detector* circuits and the tape is commanded to decelerate in a controlled manner.

The transports can operate in the Read mode in either the forward or reverse direction. When operating in a *shuttling* mode (e.g., synchronous forward, stop, synchronous reverse, and stop), no turnaround delay is required between the end of one motion command and the beginning of the next motion command in the opposite direction.

In addition to the capstan control system, the transports have a mechanical tape storage system, supply and take-up reel servo systems, magnetic head and its associated electronics, and the control logic.

The mechanical storage system buffers the relatively fast starts and stops of the capstan from the high inertia of the supply and take-up reels. As tape is taken from or supplied to the storage system, a photoelectric sensor measures the displacement of the storage arm

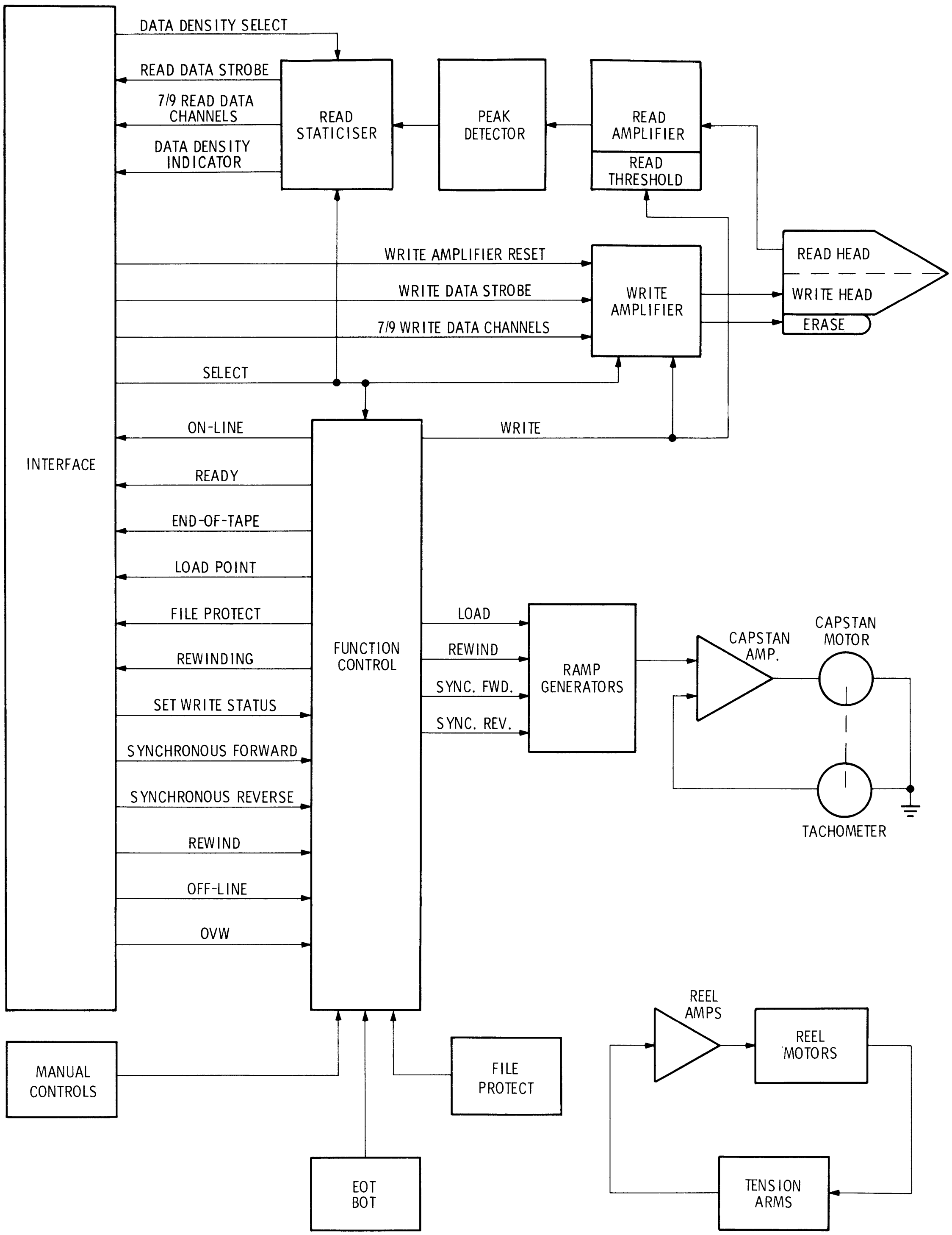


Figure 1-2. Model T6X40 Tape Transport Block Diagram

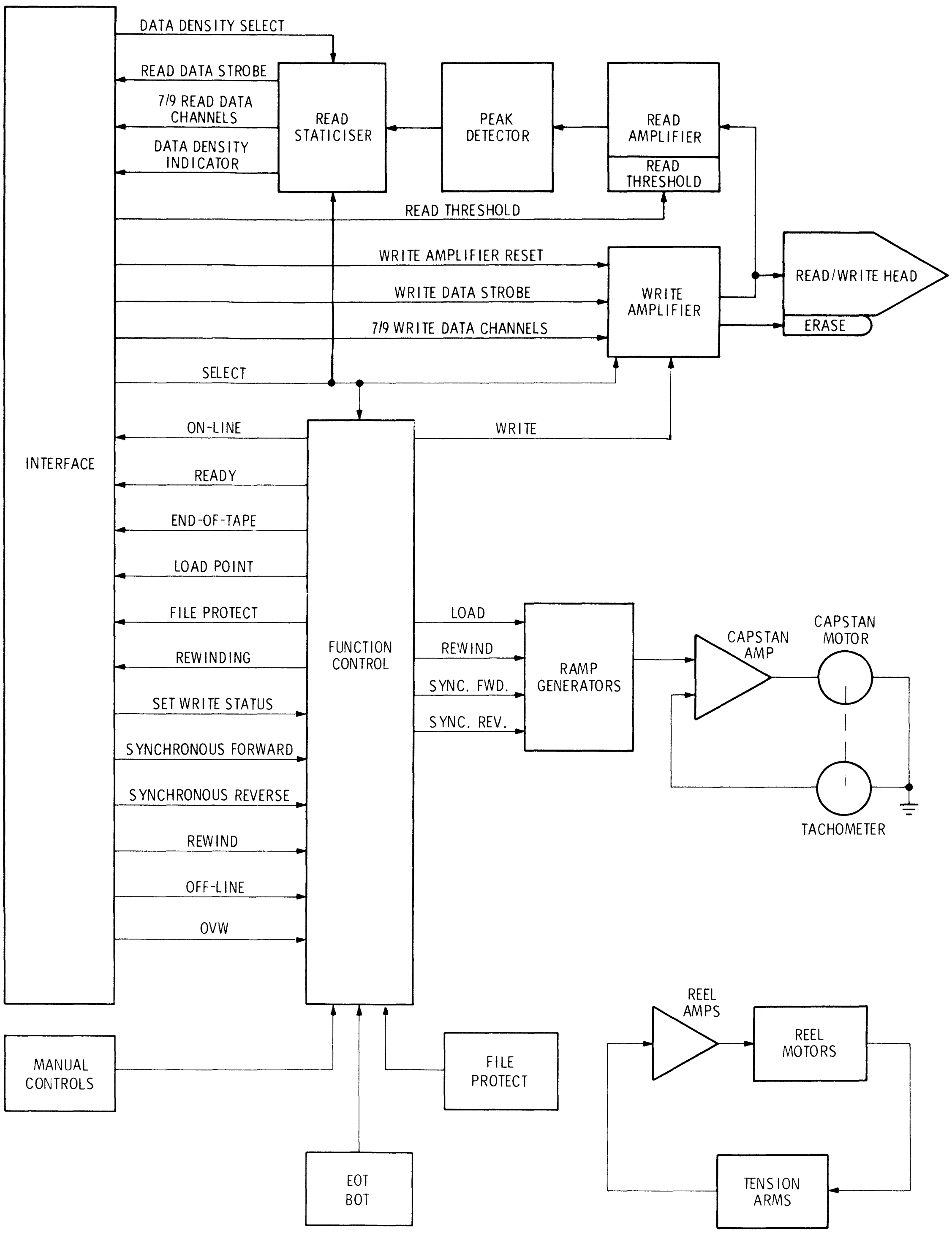


Figure 1-3. Model T6X60 Tape Transport Block Diagram

and feeds an error signal to the reel motor amplifier. This signal is amplified and used to control the reel motor such that the reel will either supply or take up tape to maintain the storage arm in its nominal operating position. The storage arm system is designed to give a constant tape tension as long as the arm is within its operating region. This tape path design minimizes tape wear because there is only relative motion on the tape oxide at the magnetic head.

The magnetic head writes and reads the flux transitions on the tape under control of the data electronics. Switching from the Read-After-Write to the Read-Only mode on T6X40 models is accomplished by remote command. Switching from the Write to the Read mode on T6X60 models is also accomplished by remote command.

The control logic operates on manual commands to enable the loaded tape to be brought to the Load Point. At this stage, remote commands control tape motion, writing, and reading. The logic also provides rewind and unload functions in conjunction with the manual REWIND control.

The transports are also equipped with a photoelectric sensor to detect the Beginning of Tape (BOT) tab and End of Tape (EOT) tab. The EOT signal is sent as a level to the customer while the BOT signal is also used internally in the transport for control purposes.

The transports are designed with an interlock to protect tape from damage due to component or power failure, or incorrect tape threading. A tape cleaner is provided to minimize tape contamination.

1.5 MECHANICAL AND ELECTRICAL SPECIFICATIONS

Table 1-1 details the mechanical and electrical specifications for the T6X40 tape transport; Table 1-2 details the mechanical and electrical specifications for the T6X60 transport.

1.5.1 INTERFACE SPECIFICATIONS

Levels: True = 0 to +0.4v (approximately)
False = High = +3v (approximately)

Pulses: Levels as above. Edge transmission delay over 20 feet of cable is not greater than 200 nsec.

The interface circuits are designed so any disconnected wire results in a false signal.

Figure 1-4 shows the configuration for which the transmitters and receivers have been designed.

Table 1-1

Model T6X40 Mechanical and Electrical Specifications

Tape (computer grade) Width Thickness	 12.6492 ±0.508 mm (0.5 inch) 0.0381 mm (1.5 mil)
Tape Tension	2.224 ±0.139 N (8.0 ounces)
Reel Diameter	266.7 mm (10.5 inches) maximum
Recording Mode (IBM Compatible)	NRZI
Magnetic Head	Dual Stack (with Erase Head)
Tape Speed, Standard	1.143, 0.953, 0.635, 0.476, 0.317 m/s (45, 37.5, 25, 18.75, 12.5 ips)
Instantaneous Speed Variation	±1%
Long-Term Speed Variation	±1%
Rewind Speed	3.81 m/s (150 ips) nominal
Interchannel Displacement Error Read Write	 381 μm (150 μinches) maximum (Note 1) 381 μm (150 μinches) maximum (Note 2)
Stop/Start Time at 1.143 m/s (45 ips) (inversely proportional to tape speed)	 8.33 ±0.55 msec
Stop/Start Displacement	4.826 ±0.50 mm (0.19 ±0.02 inch)
Beginning of Tape (BOT) and End of Tape (EOT) Detectors (Note 3)	Photoelectric IBM Compatible
Weight	38.55 kg (85 pounds)
Dimensions Height Width Depth (from mounting surface) Depth (from front surface)	 622.3 mm (24.5 inches) (Note 4) 482.6 mm (19.0 inches) 317.5 mm (12.5 inches) 381.0 mm (15.0 inches)
Operating Temperature	2°C to 50°C (35°F to 122°F)
Non-operating Temperature	—45°C to 71°C (—50°F to 160°F)
Operating Altitude	6096 m (0 to 20,000 feet)
Non-operating Altitude	15240 m (0 to 50,000 feet)
Power Volts ac Watts (maximum on high line) Hertz	 95, 105, 115, 125, 190, 210, 220, 230, 240, 250 300 to 400 48 to 400
Mounting	Standard 482.6 mm (19-inch) EIA Rack
Electronics	All Silicon

NOTE:

1. The maximum displacement between any two bits of a character when reading an IBM master tape using the Read section of the Read-After-Write head.
2. The maximum displacement between any two bits of a character on a tape written with all ones using the Write section of the Read-After-Write head.
3. Approximate distance from detection area to head gap equals 30.48 mm (1.2 inches).
4. Includes 12.7 mm (½-inch) spacer furnished with unit.

884S

Table 1-2

Model T6X60 Mechanical and Electrical Specifications

Tape (computer grade) Width Thickness	 12.6492 ±0.508 mm (0.5 inch) 0.0381 mm (1.5 mil)
Tape Tension	2.224 ±0.139 N (8.0 ounces)
Reel Diameter	266.7 mm (10.5 inches) maximum
Recording Mode (IBM Compatible)	NRZI
Magnetic Head	Single Stack (with Erase Head)
Tape Speed, Standard	1.143, 0.953, 0.635, 0.476, 0.317 m/s (45, 37.5, 25, 18.75, 12.5 ips)
Instantaneous Speed Variation	±1%
Long-Term Speed Variation	±1%
Rewind Speed	3.81 m/s (150 ips) nominal
Interchannel Displacement Error (Note 1) 800 cpi 556 cpi	 381 μm (150 μinches) maximum 508 μm (200 μinches) maximum
Stop/Start Time at 1.143 m/s (45 ips) (inversely proportional to tape speed)	 8.33 ±0.55 msec
Stop/Start Displacement	4.826 ±0.50 mm (0.19 ±0.02 inch)
Beginning of Tape (BOT) and End of Tape (EOT) Detectors (Note 2)	Photoelectric IBM Compatible
Weight	38.55 kg (85 pounds)
Dimensions Height Width Depth (from mounting surface) Depth (from front surface)	 622.3 mm (24.5 inches) (Note 3) 482.6 mm (19.0 inches) 317.5 mm (12.5 inches) 381.0 mm (15.0 inches)
Operating Temperature	2°C to 50°C (35°F to 122°F)
Non-operating Temperature	—45°C to 71°C (—50°F to 160°F)
Operating Altitude	6096 m (0 to 20,000 feet)
Non-operating Altitude	15240 m (0 to 50,000 feet)
Power Volts ac Watts (maximum on high line) Hertz	 95, 105, 115, 125, 190, 210, 220, 230, 240, 250 300 to 400 48 to 400
Mounting	Standard 482.6 mm (19-inch) EIA Rack
Electronics	All Silicon

NOTE:

1. Defined as the maximum displacement between any two bits of a character when reading an IBM master tape.
2. Approximate distance from detection area to head gap equals 30.48 mm (1.2 inches).
3. Includes 12.7 mm (½-inch) spacer furnished with unit.

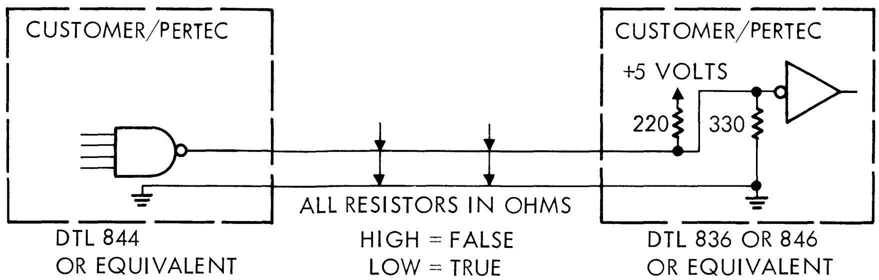


Figure 1-4. Interface Configuration

SECTION II
INSTALLATION AND INITIAL CHECKOUT

2.1 INTRODUCTION

This section contains a summary of interface lines, information for uncrating the transport, and the procedure for electrically connecting and performing the initial checkout of the transport.

2.2 UNCRATING THE TRANSPORT

The transport is shipped in a protective container which meets the National Safe Transit Specification (Project 1A, Category 1). The container is designed to minimize the possibility of damage during shipment. The following procedure describes the recommended method for uncrating the transport.

(1) Place the shipping container on a low, flat surface. Ensure that the carton is positioned so that the shipping label, model, and serial number information are visable on the top surface of the carton.

(2) Remove or cut tape from around top of carton and open flaps. Refer to Figure 2-1(A). Leave the four polyurethane corner blocks in place between the inner and outer cartons.

(3) Fold outer carton flaps out and away from carton.

(4) Remove Operating and Service Manual from carton.

(5) Slit tape holding inner carton flaps together.

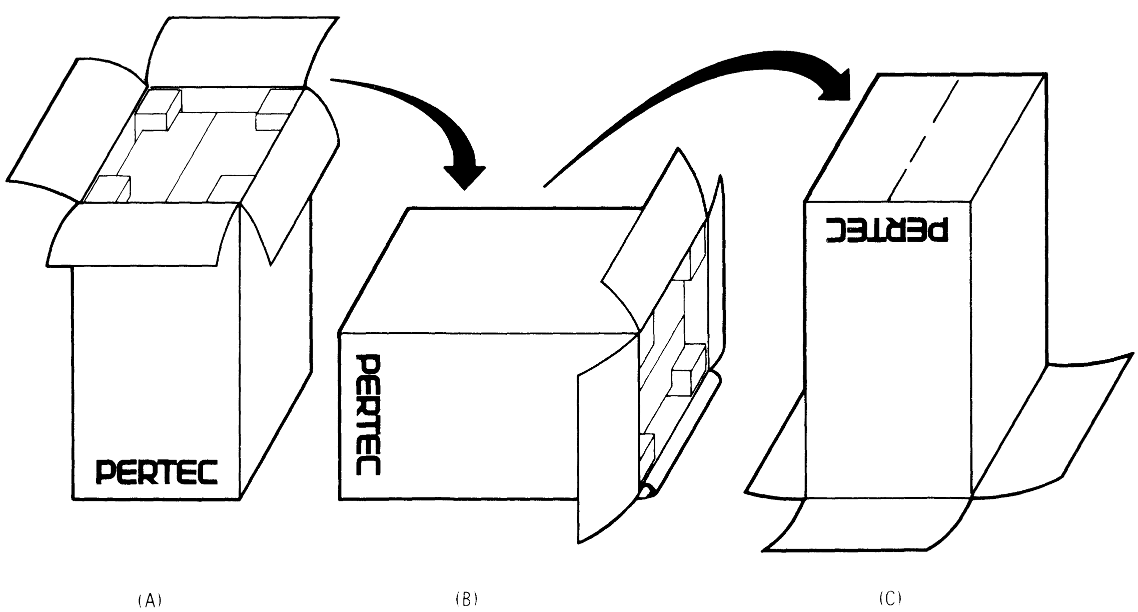


Figure 2-1. Carton Placement for Removal of Transport

884S

(6) With the four corner blocks still in place, rotate packing assembly 90° to position shown in Figure 2-1(B); rotate another 90° until the entire packing assembly is in the position shown in Figure 2-1(C).

NOTE

Leaving corner blocks in place prevents the inner carton from the possibility of dropping down and causing uncrating damage.

(7) Lift outer carton up and away from inner carton.

(8) Tilt inner carton and remove corner blocks at each corner and at the same time fold inner carton flaps out and away from carton.

(9) Lift inner carton up and away from steel shipping framework supporting transport. Note that transport is upside down. Invert shipping framework 180°.

(10) Before removing protective cardboard surrounding rear area of transport from shipping framework, remove hardware kit stapled to it and remove one-half-inch filler panel taped to the left inboard side of protective cardboard. Remove tape from power cord and remove protective cardboard from shipping framework.

NOTE

Hardware kit contains all necessary hardware to place transport in service.

(11) Remove tape from transport door and head cover.

(12) Check the contents of the shipping container against the packing slip; investigate the contents for possible damage — notify the carrier immediately if any damage is noted.

(13) Inspect the printed circuit boards for correct installation.

(14) Check the plug-in relays on the printed circuit for seating.

(15) Check the identification label for correct model number and line voltage requirements.

CAUTION

IF THE ACTUAL LINE VOLTAGE AT THE INSTALLATION DIFFERS FROM THAT ON THE IDENTIFICATION LABEL, THE POWER TRANSFORMER TAPS MUST BE CHANGED. REFER TO SECTION IV.

2.3 POWER CONNECTIONS

A fixed, strain-relieved power cord is supplied for plugging into a polarized 115v outlet. For other power sockets, the power plug supplied must be removed and the correct plug installed.

2.4 INITIAL CHECKOUT PROCEDURE

Section III contains a detailed description of all controls. To check for proper operation of the transport before placing it in the system, perform the following.

(1) Connect the power cord (replace power plug and change jumper plug if necessary).

(2) Load tape on the transport as described in Paragraph 3.3.

(3) Turn the transport power on by depressing the POWER control.

(4) Depress the LOAD control momentarily to apply capstan- and reel-motor power.

(5) Depress the LOAD control momentarily a second time to initiate the load sequence. The tape will move forward until it reaches the BOT tab — at which point it stops. The LOAD indicator should illuminate when the BOT reaches the photosensor and remain illuminated until the tape moves off the Load Point. At this point, there will be no action when the LOAD control is depressed.

(6) Check On-line by depressing the control repeatedly and observe that the ON LINE indicator is alternately illuminated and extinguished.

(7) With the transport Off-line (ON LINE indicator not illuminated), press the alternate action FORWARD control. Run several feet of tape onto the take-up reel and press the FORWARD control again to stop tape.

Check that, if the transport is On-line, the action of the FORWARD control is inhibited although the indicator light will still show the status of the control.

(8) Press the alternate action REVERSE switch. Tape will move in reverse until BOT tab reaches the photosensor, when it will stop. Check that the action of the REVERSE control is inhibited when the transport is On-line.

(9) Using the FORWARD control, run several feet of tape onto the take-up reel. Depress the REWIND control momentarily to initiate the Rewind mode and light the REWIND indicator. Tape will rewind past the BOT tab, enter the Load sequence, return to the BOT tab, and stop with the LOAD indicator illuminated. If the REWIND control is momentarily depressed when tape is at BOT, the LOAD indicator will be extinguished, the REWIND indicator illuminated, and tape will rewind until tape tension is lost. This action is used to unload tape. The reel can be removed as outlined in Paragraph 3.3.2.

(10) Visually check the components of the tape path for correct tape tracking (tape rides smoothly in the head guides, etc.).

2.5 INTERFACE CONNECTIONS

It is assumed that interconnection of PERTEC and Customer equipment uses a harness of individual twisted pairs, or a PERTEC-approved flat ribbon cable; either with the following characteristics.

(1) Maximum length of 20 feet.

(2) Impedance between 110 to 150 ohms.

(3) 22- or 24-gauge conductor with minimum insulation thickness of 0.01 inch.

It is important that the ground side of each twisted pair is grounded within a few inches of the signal source.

Three printed circuit edge connectors are required for each transport. These are ELCO connectors, Part No. 00-6007-036-980-002 (PERTEC Part No. 503-0036), which can be supplied upon request at no charge. Each connector must be wired by the customer and strain relieved as shown in Figure 2-2. Interface signals are thus routed directly to and from the printed circuit boards. Table 2-1 shows the Input/Output lines for the T6X40 transport; Table 2-2 shows the Input/Output lines for the T6X60 transport. Details relating to the interface are contained in Section III.

2.6 RACK MOUNTING THE TRANSPORT

The physical dimensions of the transport are such that it may be mounted in a standard 19-inch EIA rack; 24.5 inches of panel space is required. It requires a depth behind the mounting surface of at least 13 inches.

Figures 2-3 and 2-4 illustrate the procedure for mounting the transport, as follows.

(1) Install the hinge pin blocks on the EIA rack (see Figure 2-3 for correct position) using 10-32 pan head screws. Do not fully tighten the screws. Place a No. 10 shim washer on each pin.

(2) Set the shipping frame down with the front door of the transport facing up (i.e., lying in a horizontal position). Remove the screws securing the Z-shaped shipping blocks to the frame.

CAUTION

SECURE THE EIA RACK SO THAT IT WILL NOT TIP OR MOVE WHEN THE TRANSPORT IS POSITIONED UPON THE HINGE PIN BLOCKS. TWO PERSONS SHOULD HANDLE THE TRANSPORT WHEN MOUNTING TO PREVENT DAMAGE TO THE PCBAS OR OTHER ACCESSORY PARTS.

(3) Lift the transport out of the shipping frame and hang the transport on the hinge pin blocks (see Figure 2-4). Hang the transport by placing it up to the hinge pin blocks on an angle of 60° to its closed position.

(4) Remove the Z-shaped shipping blocks from the tape deck.

(5) Adjust the hinge pin blocks on the EIA rack so that the transport hangs symmetrically in the rack. Tighten the screws.

(6) Open the tape deck to 90° and install the safety block using 4-40 screws (see Figure 2-4).

(7) Check that the fastener engages behind the EIA rack.

(8) Clean the tape deck as described in the maintenance procedure.

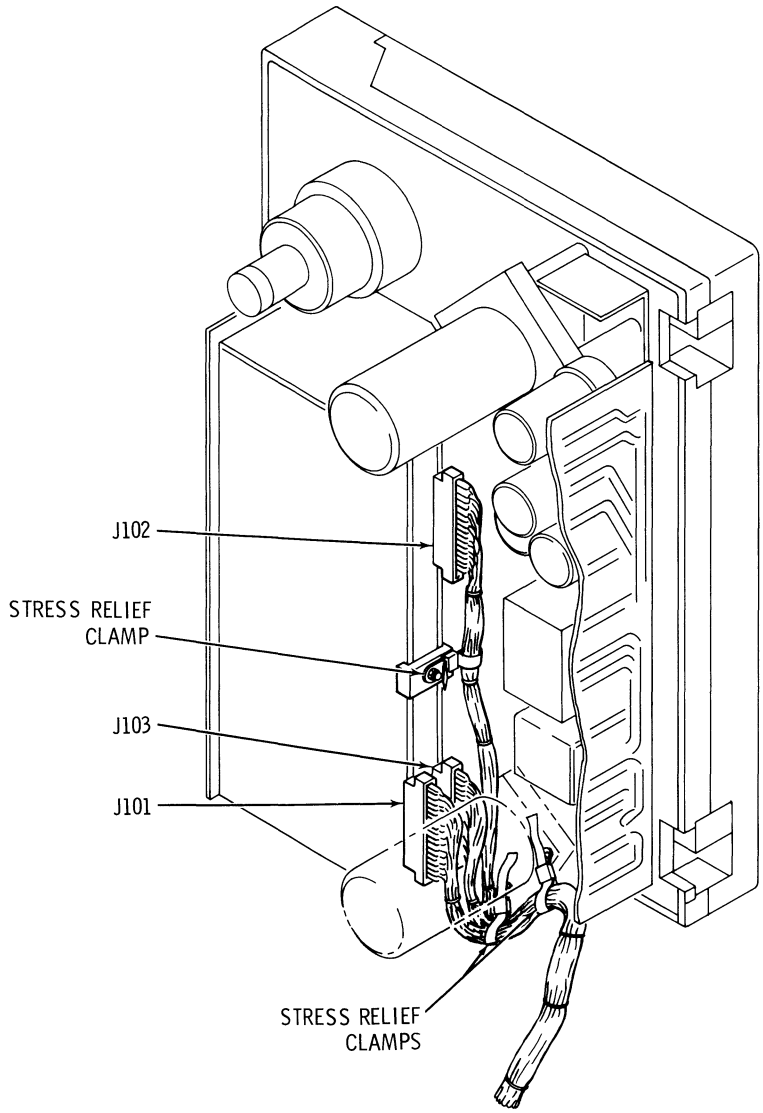


Figure 2-2. Interface Cable Installation

Table 2-1

Model T6X40 Interface Connections

Transport Connector	36-Pin Etched PC Edge Connector
Mating Connector	36-Pin ELCO 00-6007-036-980-002

Connector	Live Pin	Gnd Pin	Signal*
J101 Tape Control PCBA	B	2	OVERWRITE (IOVW)
	J	8	SELECT (ISLT)
	C	3	SYNCHRONOUS FORWARD Command (ISFC)
	E	5	SYNCHRONOUS REVERSE Command (ISRC)
	H	7	REWIND Command (IRWC)
	L	10	OFF-LINE Command (IOFFC)
	K	9	SET WRITE STATUS (ISWS)
	D	4	DATA DENSITY SELECT (IDDS) (Optional)
	T	16	READY (IRDY)
	M	11	ON-LINE Command
	N	12	REWINDING (IRWD)
	U	17	END OF TAPE (IEOT)
	R	14	LOAD POINT (ILDP)
	P	13	FILE PROTECT (IFPT)
	F	6	DATA DENSITY INDICATOR (IDDI)
	15	—	WRITE AMPLIFIER RESET (IWARS)**
J102 Data PCBA	A	1	WRITE DATA STROBE (IWDS)
	C	3	WRITE AMPLIFIER RESET (IWARS)
	L	10	WRITE DATA PARITY (IWDP)
	M	11	WRITE DATA 0 (IWD0) } Omit for 7-Ch Head
	N	12	WRITE DATA 1 (IWD1) } Omit for 7-Ch Head
	P	13	WRITE DATA 2 (IWD2)
	R	14	WRITE DATA 3 (IWD3)
	S	15	WRITE DATA 4 (IWD4)
	T	16	WRITE DATA 5 (IWD5)
	U	17	WRITE DATA 6 (IWD6)
	V	18	WRITE DATA 7 (IWD7)
J103 Data PCBA	2	B	READ DATA STROBE (IRDS)
	1	A	READ DATA PARITY (IRDP)
	3	C	READ DATA 0 (IRD0) } Omit for 7-Ch Head
	4	D	READ DATA 1 (IRD1) } Omit for 7-Ch Head
	8	J	READ DATA 2 (IRD2)
	9	K	READ DATA 3 (IRD3)
	14	R	READ DATA 4 (IRD4)
	15	S	READ DATA 5 (IRD5)
	17	U	READ DATA 6 (IRD6)
	18	V	READ DATA 7 (IRD7)

*See Section III for details.

**IWARS is required on this pin only when the OVW feature is utilized (Paragraph 4.3.4.4). If interface cabling is provided by Customer, pin 15 on J101 must be jumpered to pin C on J102.

Table 2-2
Model T6X60 Interface Connections

Transport Connector	36-Pin Etched PC Edge Connector
Mating Connector	36-Pin ELCO 00-6007-036-980-002

Connector	Live Pin	Gnd Pin	Signal*
J101 Tape Control PCBA	B	2	OVERWRITE (IOVW)
	J	8	SELECT (ISLT)
	C	3	SYNCHRONOUS FORWARD Command (ISFC)
	E	5	SYNCHRONOUS REVERSE Command (ISRC)
	H	7	REWIND Command (IRWC)
	L	10	OFF-LINE Command (IOFFC)
	K	9	SET WRITE STATUS (ISWS)
	D	4	DATA DENSITY SELECT (IDDS) (Optional)
	T	16	READY (IRDY)
	M	11	ON-LINE Command
	N	12	REWINDING (IRWD)
	U	17	END OF TAPE (IEOT)
	R	14	LOAD POINT (ILDP)
	P	13	FILE PROTECT (IFPT)
	F	6	DATA DENSITY INDICATOR (IDDI)
	15	—	WRITE AMPLIFIER RESET (IWARS)**
J102 Data PCBA	A	1	WRITE DATA STROBE (IWDS)
	C	3	WRITE AMPLIFIER RESET (IWARS)
	E	5	READ THRESHOLD (IRTH)
	L	10	WRITE DATA PARITY (IWDP)
	M	11	WRITE DATA 0 (IWD0) } Omit for 7-Ch Head
	N	12	WRITE DATA 1 (IWD1) } Omit for 7-Ch Head
	P	13	WRITE DATA 2 (IWD2)
	R	14	WRITE DATA 3 (IWD3)
	S	15	WRITE DATA 4 (IWD4)
	T	16	WRITE DATA 5 (IWD5)
	U	17	WRITE DATA 6 (IWD6)
	V	18	WRITE DATA 7 (IWD7)
J103 Data PCBA	2	B	READ DATA STROBE (IRDS)
	1	A	READ DATA PARITY (IRDP)
	3	C	READ DATA 0 (IRD0) } Omit for 7-Ch Head
	4	D	READ DATA 1 (IRD1) } Omit for 7-Ch Head
	8	J	READ DATA 2 (IRD2)
	9	K	READ DATA 3 (IRD3)
	14	R	READ DATA 4 (IRD4)
	15	S	READ DATA 5 (IRD5)
	17	U	READ DATA 6 (IRD6)
	18	V	READ DATA 7 (IRD7)

*See Section III for definitions.

**IWARS is required on this pin only when the OVW feature it utilized (Paragraph 4.3.4.4). If interface cabling is provided by customer, J15 on J101 must be jumpered to pin C on J102.

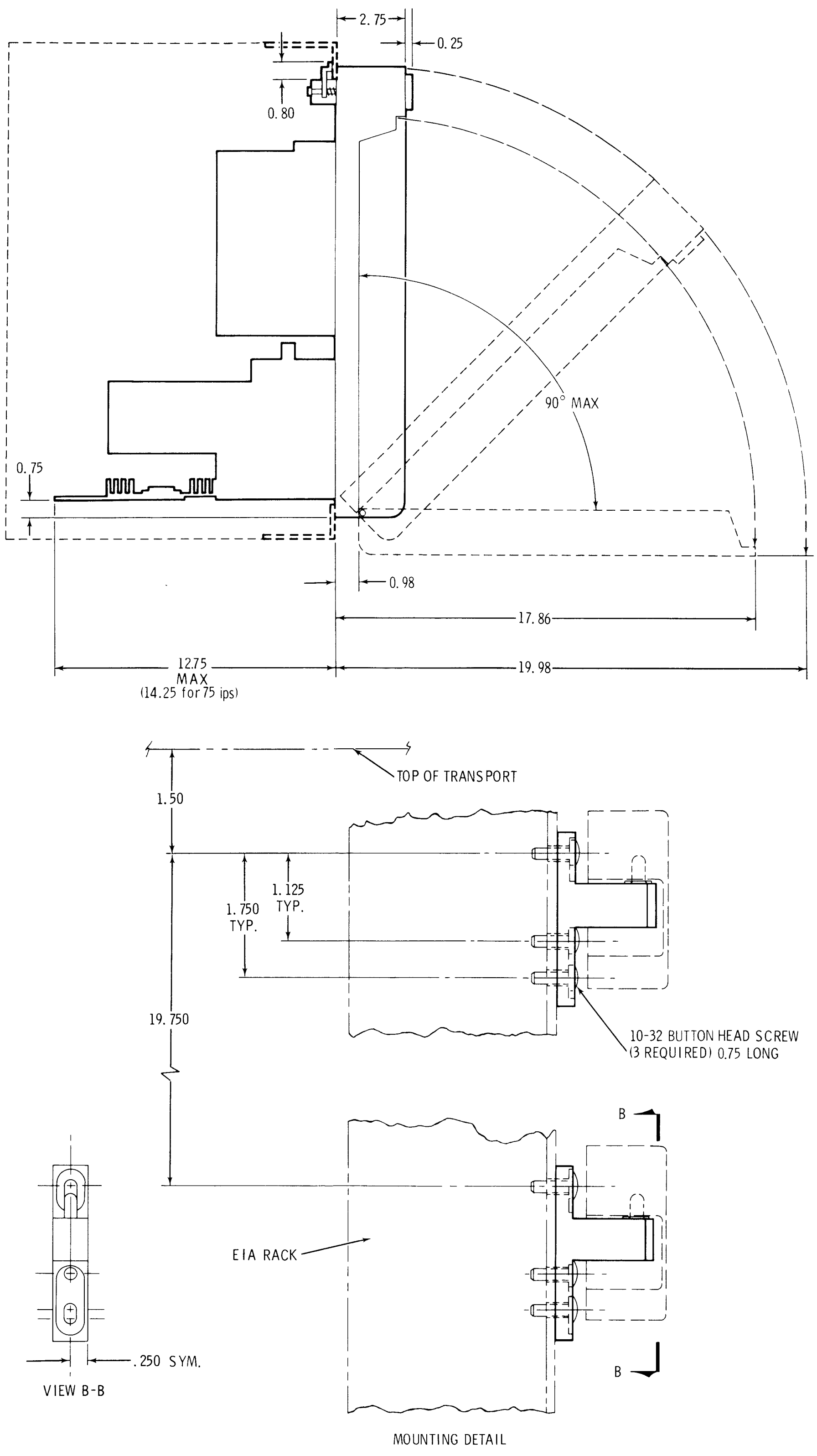


Figure 2-3. Rack Mounting the Transport

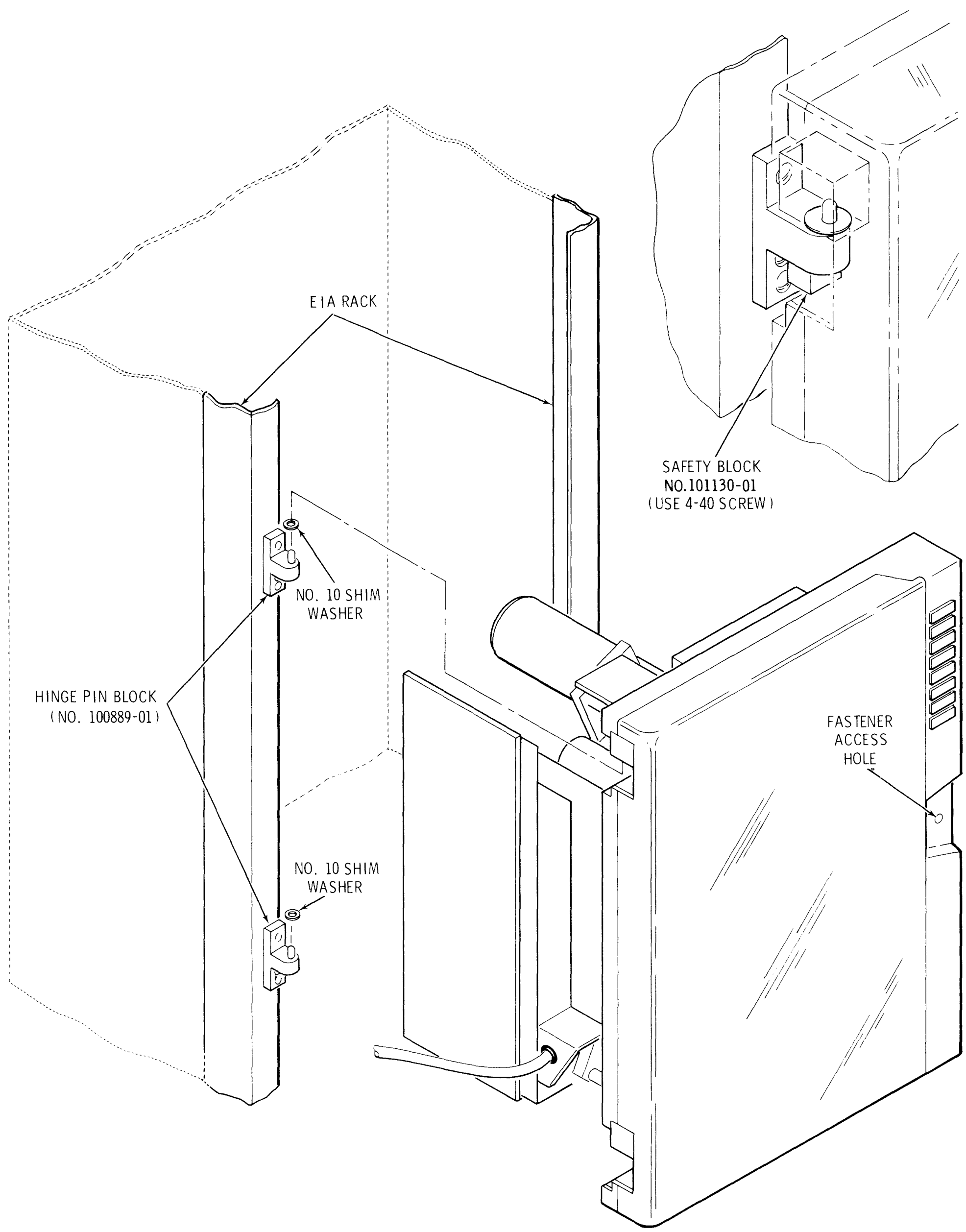


Figure 2-4. Installation Diagram

SECTION III
OPERATION

3.1 INTRODUCTION

This section explains the manual operation of the transport and defines the interface functions with regard to timing, levels, and interrelationships.

3.2 CLEANING THE HEAD AND GUIDES

The brief operation described in Paragraph 6.4 should be performed daily to realize the data reliability capabilities of the transport.

3.3 LOADING TAPE ON THE TRANSPORT

The T6X40 and T6X60 transports have the supply reel (reel to be recorded or reproduced) at the bottom; see Figure 3-1. The tape must unwind from the supply reel when the reel is turned in a clockwise direction. Note that the presence of a Write Enable ring on the reel is required to close the interlocks which allow writing.

To load a tape reel (maximum reel size is 10½ inches in diameter with 2400 feet of tape), position the reel over the quick-release hub and depress the center plunger. This allows the reel to slip over the rubber ring on the hub. Press the reel evenly and firmly against the back flange of the hub with the center plunger depressed. Release the center plunger. The reel is now properly aligned in the tape path and ready for tape threading.

Thread the tape along the path shown in Figure 3-1. (On the T6X40 model, it will be necessary to open and hold the Flux Gate unit away from the head during tape threading.) Wrap the tape leader onto the take-up reel so that the tape will be wound onto the reel when it is rotated clockwise. Wind several turns onto the take-up reel, then turn the supply reel counterclockwise until slack tape has been taken up.

3.3.1 BRINGING TAPE TO LOAD POINT (BOT)

After tape has been manually tensioned and checked for correct seating in the guides, bring tape to Load Point as follows.

(1) Turn power on by depressing the POWER control.

(2) Depress the LOAD control and release it. This applies power to the capstan and reel motors and brings tape to the correct operating tension. The tape storage arms are now in the operating position.

CAUTION

CHECK THAT THE TAPE IS POSITIONED CORRECTLY ON ALL GUIDES OR TAPE DAMAGE MAY RESULT.

(3) Depress the LOAD control a second time and release it. This causes tape to move forward at the prescribed operating velocity. Check tape tracking in the guides again and close the dust cover.

CAUTION

THE DUST COVER SHOULD REMAIN CLOSED AT ALL TIMES WHEN TAPE IS ON THE TAKE-UP REEL. DATA RELIABILITY MAY BE IMPAIRED BY CONTAMINANTS IF THE COVER IS LEFT OPEN.

When the reflective BOT tab reaches the Load Point, tape stops with the front edge of the tab approximately 1 inch from the magnetic head gap. The transport is now ready to receive external commands.

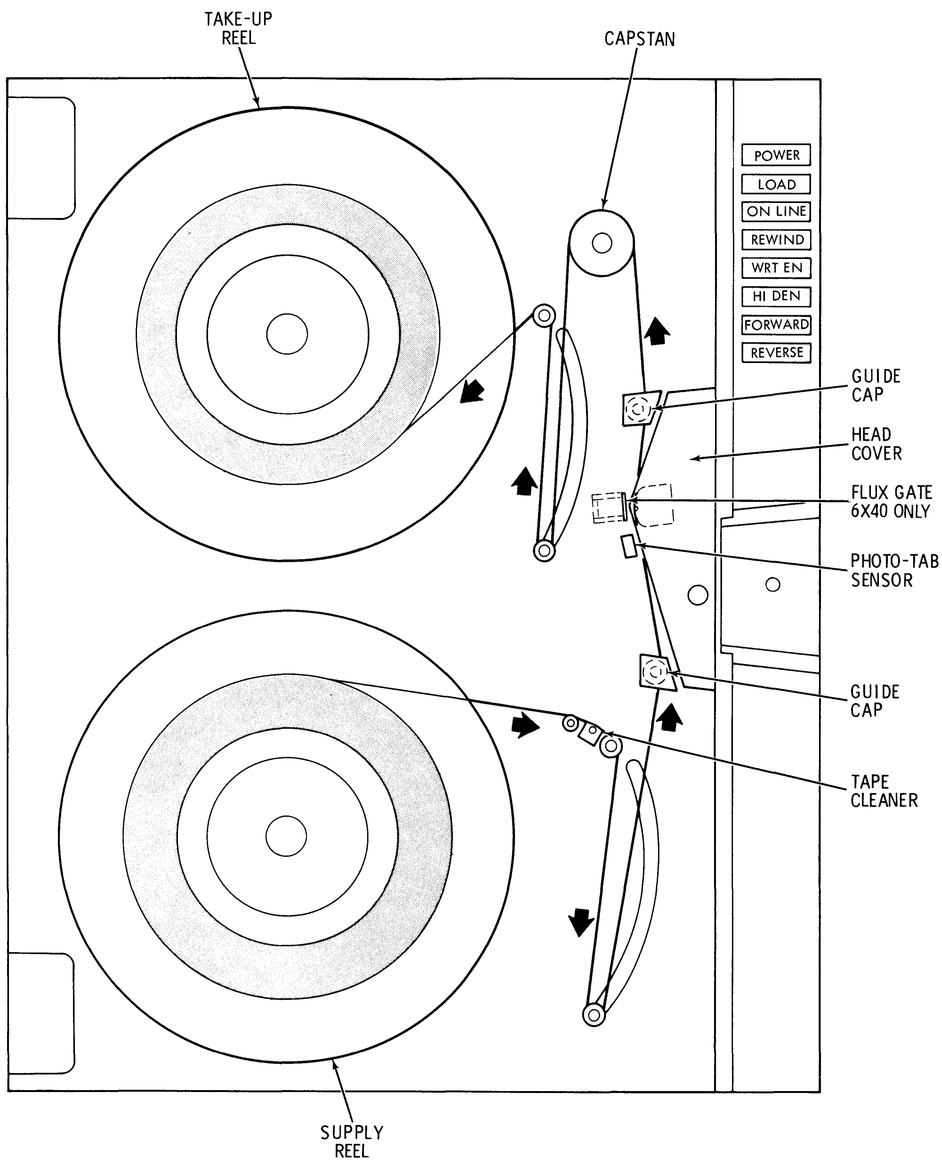


Figure 3-1. Tape Path and Controls

3.3.2 UNLOADING THE TAPE

To unload a recorded tape, complete the following procedure if power has been switched off; if power is on, start at Step (3).

(1) Turn power on by depressing the POWER control.

(2) Depress the LOAD control and release it; this applies tape tension.

(3) Depress the REWIND control and release it. When tape has rewound to the BOT tab it comes to a controlled stop. The tape overshoots and the transport enters the Load sequence to bring tape to rest at the BOT.

(4) Depress the REWIND control a second time and release it; this initiates a further rewind action which continues until tension is lost.

(5) Open the dust cover and wind the end of tape onto the supply reel. Depress the hub center plunger and remove the reel. Close the dust cover.

3.4 MANUAL CONTROLS

Eight operational controls with indicators are located on the control panel on the front of the transport, as shown in Figure 3-1. The following paragraphs describe the functions of these controls.

3.4.1 POWER

The POWER control is an alternate action switch/indicator which connects line voltage to the power transformer. When power is turned on: all power supplies are established, all of the motors are open-circuited (low value resistors are connected across the reel motors), and a reset signal is applied to key control flip-flops.

3.4.2 LOAD

The LOAD control is a momentay switch/indicator. Depressing and releasing the control for the first time after power is switched on energizes the servo system by applying ground returns to all motors and removes the reset signal. Tape will now be tensioned.

Depressing and releasing the LOAD control for the second time causes tape to move to and stop at the Load Point. The transport is now ready to receive external commands. While the BOT tab is located over the photo-tab sensor (see Figure 3-1), the LOAD indicator is illuminated. The LOAD control is disabled after the first LOAD or manual REWIND command has been given and can only be re-enabled by loss of tape tension or restoration of power after power has been off.

3.4.3 REWIND

The REWIND control is a momentary switch/indicator which is enabled only in the Off-line mode. Depressing and releasing the control causes tape to rewind at approximately 150 ips. On reaching the BOT tab, the rewind drive ceases and the Load sequence automatically entered. The BOT tab will overshoot the photo-tab sensor, move forward, and stop at the Load Point.

If the REWIND control is depressed and released when tape is at Load Point (LOAD indicator illuminated), the tape rewinds off the take-up reel and tension is lost.

The REWIND indicator is illuminated throughout any rewind operation including the subsequent Load sequence where relevant.

A manual REWIND command will override the Load sequence.

3.4.4 ON LINE

The ON LINE control is a momentary switch/indicator which is enabled after an initial Load or Rewind sequence has been initiated.

Depressing and releasing the switch after an initial Load or Rewind sequence is initiated switches the transport to an On-line mode and illuminates the indicator.

In this condition the transport can accept external commands provided it is also Ready and Selected.

The transport will revert to the Off-line mode if the following occur.

(1) ON LINE is depressed a second time.

(2) An external OFF-LINE command (IOFFC) is received.

(3) Tape tension is lost.

3.4.5 WRT EN (WRITE ENABLE)

This is an indicator which is illuminated whenever power is on and a reel of tape with a Write Enable ring installed is mounted on the transport.

3.4.6 HI DEN (HIGH DENSITY)

The HI DEN control is an alternate action switch/indicator. It is provided in all models of the transport, but is only relevant to 7-track operation where it determines the character packing density at which the Read electronics operates.

When the indicator is illuminated, the Read electronics is conditioned to operate in the High Density mode. If the indicator is not illuminated, the transport will be in the Low Density mode.

The following possible density combinations are available.

Model	Density Combination
T6840-75 T6860-75	800/556
T6840-72 T6860-72	800/200
T6540-72 T6560-72	556/200

For 9-track transports, only 800-cpi operation is allowed; thus, the switch is disabled and the indicator is permanently illuminated. When the external Data Density Select (IDDS) option is used, the switch is also disabled and the indicator reflects the state of the IDDS command.

3.4.7 FORWARD

The FORWARD control is an alternate action switch/indicator which is enabled only in the Off-line mode and when the transport is Ready.

When the switch is depressed, the indicator is illuminated and tape will move forward at the prescribed speed. When the switch is depressed again, tape stops and the indicator is extinguished.

If the EOT tab is encountered while moving forward, tape stops but the indicator will remain illuminated.

3.4.8 REVERSE

The REVERSE control is an alternate action switch/indicator which is enabled only in the Off-line mode and when the transport is Ready.

When the switch is depressed, the indicator is illuminated and the tape will move in the reverse at the prescribed speed. When the switch is depressed again, tape stops and the indicator is extinguished.

If the BOT tab is encountered while moving in the reverse, tape stops but the indicator will remain illuminated.

3.5 INTERFACE INPUTS (CONTROLLER TO TRANSPORT)

All waveform names correspond to the logical true condition. Drivers and receivers belong to the DTL 830 series where the True level is 0v and the False level is between +3v and +5v. Figure 1-4 is a schematic of the interface circuit.

3.5.1 SELECT (ISLT)

This is a level which, when true, enables all interface drivers and receivers in the transport, thus connecting the transport to the controller.

It is assumed that all of the Interface inputs discussed in the following paragraphs are gated with SELECT.

3.5.2 SYNCHRONOUS FORWARD COMMAND (ISFC)

This is a level which, when true and the transport is Ready (Paragraph 3.6.1), causes tape to move forward at the specified velocity. When the level goes false, tape motion ceases. The velocity profile ile is trapezoidal with nominally equal rise and fall times.

3.5.3 SYNCHRONOUS REVERSE COMMAND (ISRC)

This is a level which, when true and the transport is Ready (see Paragraph 3.6.1), causes tape to move in the reverse direction at the specified velocity. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times. An SRC will be terminated upon encountering the BOT tab, or ignored if given when the tape is at Load Point.

3.5.4 REWIND COMMAND (IRWC)

This is a pulse (minimum width of 2 μsec) which, if the transport is Ready, causes tape to move in the reverse direction at approximately 150 ips. Upon reaching BOT, the rewind ceases and the Load sequence is automatically initiated. Tape now moves forward and comes to rest at BOT.

The REWIND indicator is illuminated for the duration of the Rewind and the following Load sequence.

An RWC is ignored if tape is already at BOT.

The velocity profile is trapezoidal with nominally equal rise and fall times of approximately 0.5 second.

3.5.5 SET WRITE STATUS (ISWS)

This is a level which must be true for a minimum period of 20 μsec after the front edge of an ISFC (or ISRC) when the Write mode of operation is required. The front edge of the delayed ISFC (or ISRC) is used to sample the ISWS signal and sets the Write/Read flip-flop in the transport to the Write state.

If the Read mode of operation is required, the ISWS signal must be false for a minimum period of 20 μsec after the front edge of a ISFC (or ISRC), in which case the Write/Read flip-flop will be set to the Read state.

3.5.6 WRITE DATA LINES (IWDP, IWD0 — IWD7, 9-Channel; IWDP, IWD2 — IWD7, 7-CHANNEL)

These are levels which, when true at WRITE DATA STROBE (IWDS) time (when the transport is in the Write status), result in a flux reversal being recorded on the corresponding tape track. These lines must be held steady during the IWDS and for 0.5 μsec before and after the IWDS pulse.

3.5.7 WRITE DATA STROBE (IWDS)

This is a pulse (2 μsec minimum) for each character to be recorded. It samples each of the WRITE DATA lines and toggles the appropriate flip-flops in the write register when a one is written. The IWDP, IWD0 — IWD7 levels must be steady during and for 0.5 μsec before and after the IWDS. Toggling of the write register is initiated by the trailing edge of IWDS.

The recording density is determined by tape speed and the frequency of the IWDS pulses. Frequency stability should normally be better than 0.25 percent.

An additional IWDS pulse, accompanied by the appropriate levels on IWDP, IWD0 — IWD7 is required to write the Cyclic Redundancy Check Character (CRCC) in 9-channel systems, four character spaces after the last data character. The Longitudinal Redundancy Check Character (LRCC) is written by a pulse on control line IWARS, eight character spaces after the last data character (four character spaces for 7-channel).

3.5.8 WRITE AMPLIFIER RESET (IWARS)

This is a pulse (2 μsec minimum) which causes the LRCC to be written onto tape eight character spaces (four character spaces for 7-channel) after the last data character has been written. The pulse resets the write register causing all channels to be erased in a uniform direction in the Inter-Record Gap (IRG). The LRCC is written coincident with the leading edge of this pulse.

3.5.9 OFF-LINE (IOFFC)

This is a level or pulse of a minimum width of 2 μsec which resets the On-line flip-flop to the false state, placing the transport under manual control.

It is gated by SELECT only, allowing an OFF-LINE command to be given while a rewind is in progress.

OFF-LINE must be separated from a REWIND command by at least 2 μsec.

3.5.10 OVERWRITE (IOVW)

This is a level which, when true, conditions appropriate circuitry in the transport to allow updating (rewriting) of a selected record. The transport must be in the Write mode of operation to utilize the OVW feature.

3.5.11 DATA DENSITY SELECT (IDDS) (OPTIONAL)

This is a level which, when true, conditions the Read electronics to operate in the High Density mode and causes the HI DEN indicator to be illuminated.

When this option is selected, the manual HI DEN switch is disabled.

3.5.12 READ THRESHOLD (IRTH) (6X60 TRANSPORT ONLY)

This level is employed only in the 6X60 transport. When true, it selects the higher of two read threshold levels. IRTH must be held steady for the duration of each record. The high threshold level should be selected only when it is desired to perform a read-after-write data check. When reading a pre-recorded tape, the IRTH line should be in a false state.

3.6 INTERFACE OUTPUTS (TRANSPORT TO CONTROLLER)

It is assumed that all Interface outputs discussed in the following paragraphs are gated with SELECT.

3.6.1 READY (IRDY)

This is a level which is true when the transport is ready to accept any external command, i.e., when

(1) Tape tension is established.

(2) The initial LOAD or REWIND command has been completed.

(3) There is no subsequent REWIND command in progress.

(4) The transport is On-line.

3.6.2 READ DATA (IRDP, IRD0 — IRD7, 9-CHANNEL; IRDP, IRD2 — IRD7, 7-CHANNEL)

The individual bits of each character are assembled into parallel form in a one-stage deskewing register. The register outputs drive the Read Data interface lines.

The complete character is obtained by sampling the interface lines simultaneously with the trailing edge of the Read Data Strobe (IRDS).

3.6.3 READ DATA STROBE (IRDS)

This is a pulse with a minimum width of 2 μsec for each data character read from tape. The trailing edge of this pulse should be used to sample the Read Data lines.

Although the average time between adjacent IRDS pulses is

$$\frac{1}{BV}$$

where B = Bit Density, V = Tape Velocity

this time may vary considerably because of skew and bit crowding effects.

3.6.4 ON-LINE

This is a level which is true when the On-line flip-flop is set. When true, the transport is under remote control; when false, the transport is under local control.

3.6.5 LOAD POINT (ILDP)

This is a level which is true when the transport is Ready and tape is at rest with the BOT tab under the photo-tab sensor. The signal goes false after the tab leaves the photosensor area.

3.6.6 END OF TAPE (IEOT)

This is a level which is true when the EOT reflective tab is positioned under the photo-tab sensor.

3.6.7 REWINDING (IRWD)

This is a level which is true when the transport is engaged in any Rewind operation or the Load sequence following a Rewind operation.

3.6.8 FILE PROTECT (IFPT)

This is a level which is true when power is on and a reel of tape, without a Write Enable ring installed, is mounted on the transport.

3.6.9 DATA DENSITY INDICATOR (IDDI)

This is a level which is true whenever the Read electronics are conditioned to operate in the High Density mode. This condition can be created either by the external IDDS signal or the local HI DEN switch, depending on the option selected (see Paragraphs 3.4.6 and 3.5.11).

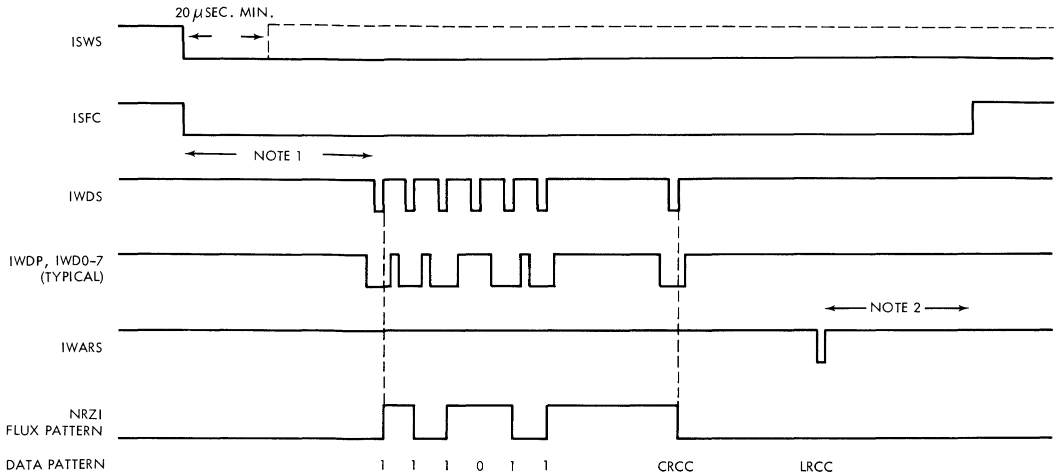
3.7 INTERFACE TIMING

3.7.1 WRITE WAVEFORMS

Figure 3-2 shows the write waveforms. The controller generates all command waveforms.

3.7.2 READ WAVEFORMS

Figure 3-3 shows the read waveforms.



NOTES:

1. PRE-RECORD DELAY IN THE 6 X 40 TRANSPORT SHOULD BE CALCULATED TO PRODUCE 3.5 INCHES OF TRAVEL WHEN STARTING FROM BOT; OTHERWISE 0.4 INCH IN A 9-CHANNEL TRANSPORT AND 0.51 INCH IN A 7-CHANNEL TRANSPORT.

   PRE-RECORD DELAY IN THE 6 X 60 TRANSPORT SHOULD BE CALCULATED TO PRODUCE 3.5 INCHES OF TRAVEL WHEN STARTING FROM BOT; OTHERWISE 0.25 INCH IN A 9-CHANNEL TRANSPORT AND 0.36 INCH IN A 7-CHANNEL TRANSPORT.

2. THE POST-RECORD DELAY SHOULD BE CALCULATED TO PRODUCE 0.075 INCH OF TRAVEL AFTER THE LRCC HAS BEEN DETECTED BY THE READ ELECTRONICS, BEFORE REMOVING THE SFC.

Figure 3-2. Write Waveforms

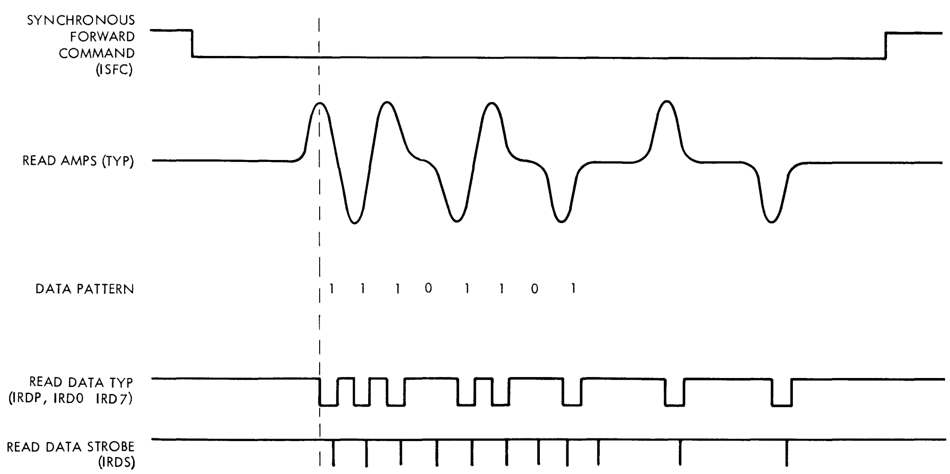


Figure 3-3. Read Waveforms

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section provides a description of the operation of the T6X40 and T6X60 Tape Transports.

The transports have the mechanical and electronic components necessary to handle magnetic tape in such a manner that data can be reproduced from a tape recorded on an IBM digital tape transport or its equivalent; and, a tape can be generated from which data can be completely recovered when played back on an IBM transport or its equivalent.

The transport consists of the following components.

(1) Power supply

(2) Capstan drive system

(3) Tape storage and reel servo systems

(4) Magnetic head and associated tape guides and cleaner

(5) Data electronics

(6) Control logic and interlock system

4.2 ORGANIZATION OF THE TRANSPORT

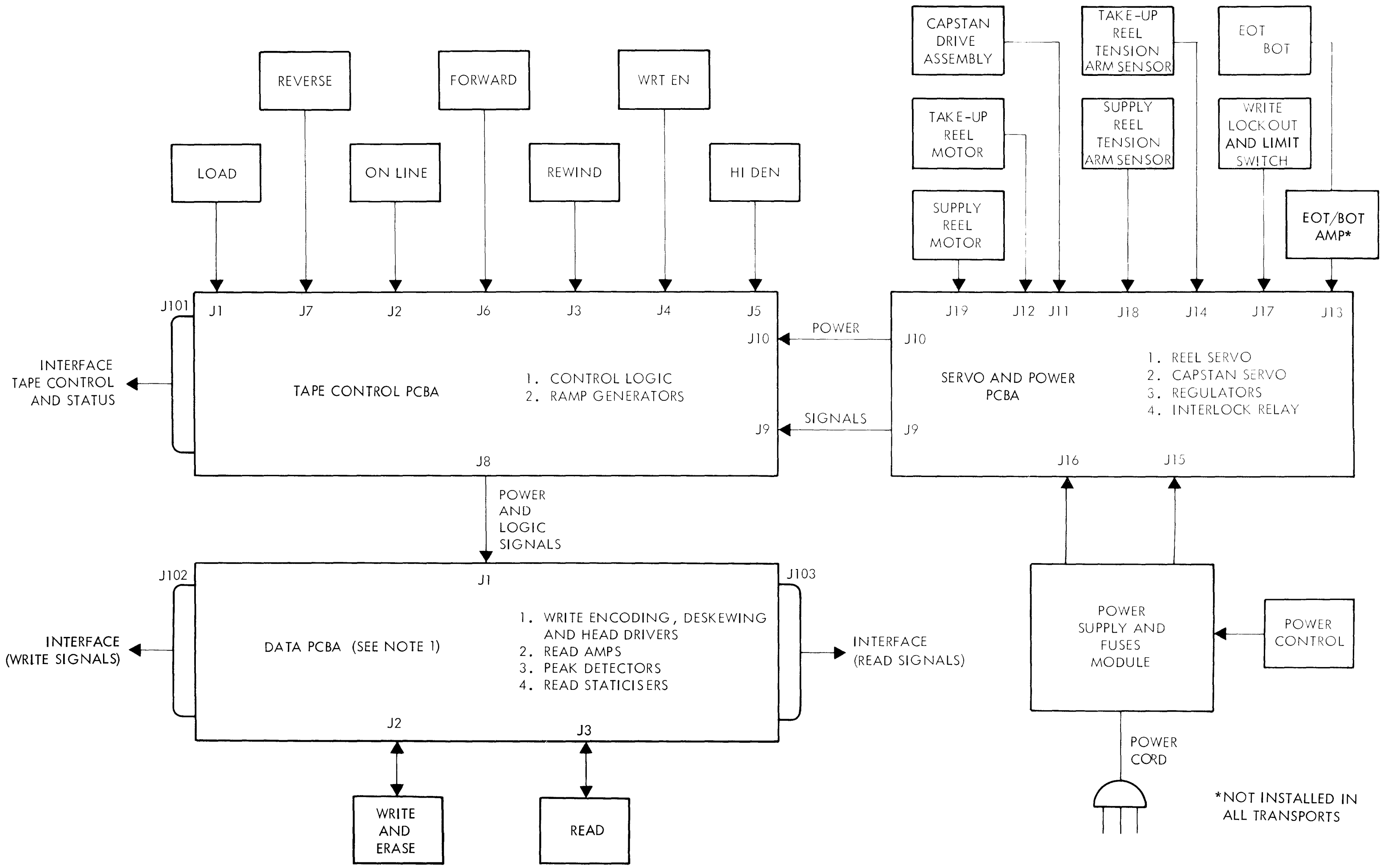
A highly modular construction technique has been adopted with all of the major components and subassemblies interconnected by connectors rather than the more conventional wiring techniques. Refer to Figure 4-1 for organization of the T6X40 transport and to Figure 4-2 for organization of the T6X60 transport.

Three (or four) printed circuit boards are employed. The first, the Servo and Power Supply PCBA, is mounted to a common heatsink extrusion which is secured to the power supply module. It contains the reel servo amplifiers, capstan servo amplifier, voltage regulators, photo-tab sensor amplifiers, and interlock relay. With the exception of the magnetic head and the manual control switches, all of the deck-mounted components (power supply, motors, tension arm position sensors, photo-tab sensors, etc.) plug directly into locations on the board.

Two other boards are mounted in slides parallel to the rear of the deck plate. They are the Data PCBA (closest to the deck), and the Tape Control PCBA.

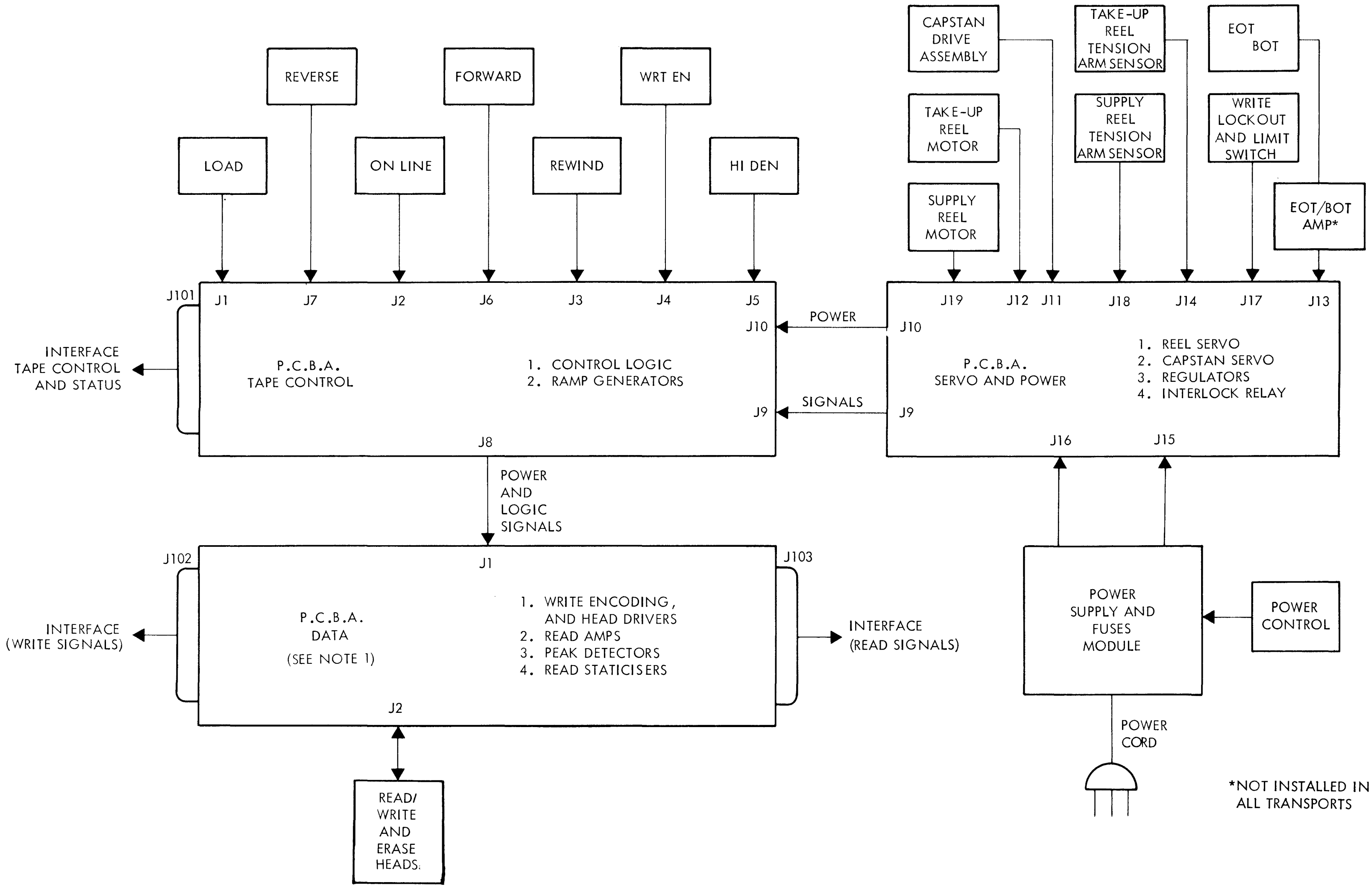
The Data PCBA is concerned with the writing and reading of data. Write data enters by means of a printed-circuit edge connector on one end of the board; it is encoded, deskewed, and the results transferred to the write head through the appropriate connector (one connector in the T6X60; one of two connectors in the T6X40) in the middle of the board. Signals from the read head enter the board via the second of the two connectors in the T6X40 and are fed to the amplifiers, peak detectors, read staticisers, and transmitters. Digital read signals, together with a READ DATA STROBE are transmitted by means of a second interface edge connector.

Dc power and three control levels are obtained from the Tape Control PCBA via a single harness.



NOTES:
1. FOR E19 AND E17 PCBA'S, POWER AND LOGIC SIGNALS FROM TAPE CONTROL PCBA, WRITE HEADS AND READ HEADS ARE J8, J1, AND J3 RESPECTIVELY.

Figure 4-1. T6X40 Tape Transport Organization



NOTES:

1. FOR DATA D1 PCBA, POWER AND LOGIC SIGNALS FROM TAPE CONTROL PCBA, WRITE AND READ HEADS ARE J8 AND J1 RESPECTIVELY.

Figure 4-2. T6X60 Tape Transport Organization

884S

The Tape Control PCBA contains the ramp command generators for the capstan servo, together with the control logic. All of the manual controls (except POWER) plug directly into this board. The printed-circuit edge connector carries interface signals to and from the board.

DC power and control signals are passed between this board and the Servo and Power Supply PCBA via a twin harness.

The harnesses from the three interface connectors are merged, strain relieved, and leave the transport.

The fourth board is the EOT/BOT Amplifier PCBA which is present only on certain transports since early versions did not incorporate the EOT/BOT feature.

4.3 FUNCTIONAL SUBSYSTEMS DESCRIPTIONS

4.3.1 POWER SUPPLY

Figure 4-3 is a block diagram of the power supply which is in two parts. The first part, the power supply module, is fastened to the deck plate and contains the power transformer, rectifier, capacitors, fuses, and a number of power resistors and diodes. Four unregulated supplies are generated at nominal voltages of ±45v and ±18v.

The second part consists of the ±10v and ±5v regulators which are located on the Servo and Power Supply PCBA. Interconnections between the two parts is provided by a harness from the power supply module which plugs into the Servo and Power Supply PCBA via two 9-pin connectors.

Selection of proper ac voltage taps on the power transformer is facilitated through use of a coded jumper plug assembly shown in Figure 4-3. A cross reference of various line voltages to jumper plug assemblies, PERTEC part numbers, and pin connections is also shown. Line voltage is connected to the transformer via the ON/OFF power control. The power control indicator (115v ac neon lamp) is connected to the transformer. The jumper plug is configured to supply 115v ac nominal to the lamp at any input line voltage. Unregulated dc (at a nominal ±18v under load) is used to power the motors and voltage regulators. Four unregulated supplies are generated. The ±10v supplies can supply up to 1.0 amp. The ±5v supplies are adjusted, regulated, and can supply 3.0 amps and 1.0 amp, respectively.

Since Diode Transistor Logic (DTL) integrated circuits are widely used, it is necessary to use an SCR for *crowbar* protection against over-voltage on the +5v line. The circuits can withstand up to 12v for 1 second. When the +5v line rises to +8v, the SCR connected between +18v and 0v fires. This holds the voltage on the ICs down until the fuse blows a few milliseconds later.

The ±45v supplies are utilized by the reel servos during high-speed rewind operation so that the final amplifiers can supply the necessary drive voltage to the reel motors. The power diodes form part of the switch circuit that supplies the ±45v during rewind. The power resistors are used to reduce dissipation in the heatsink from the reel amplifier and the +5v regulator.

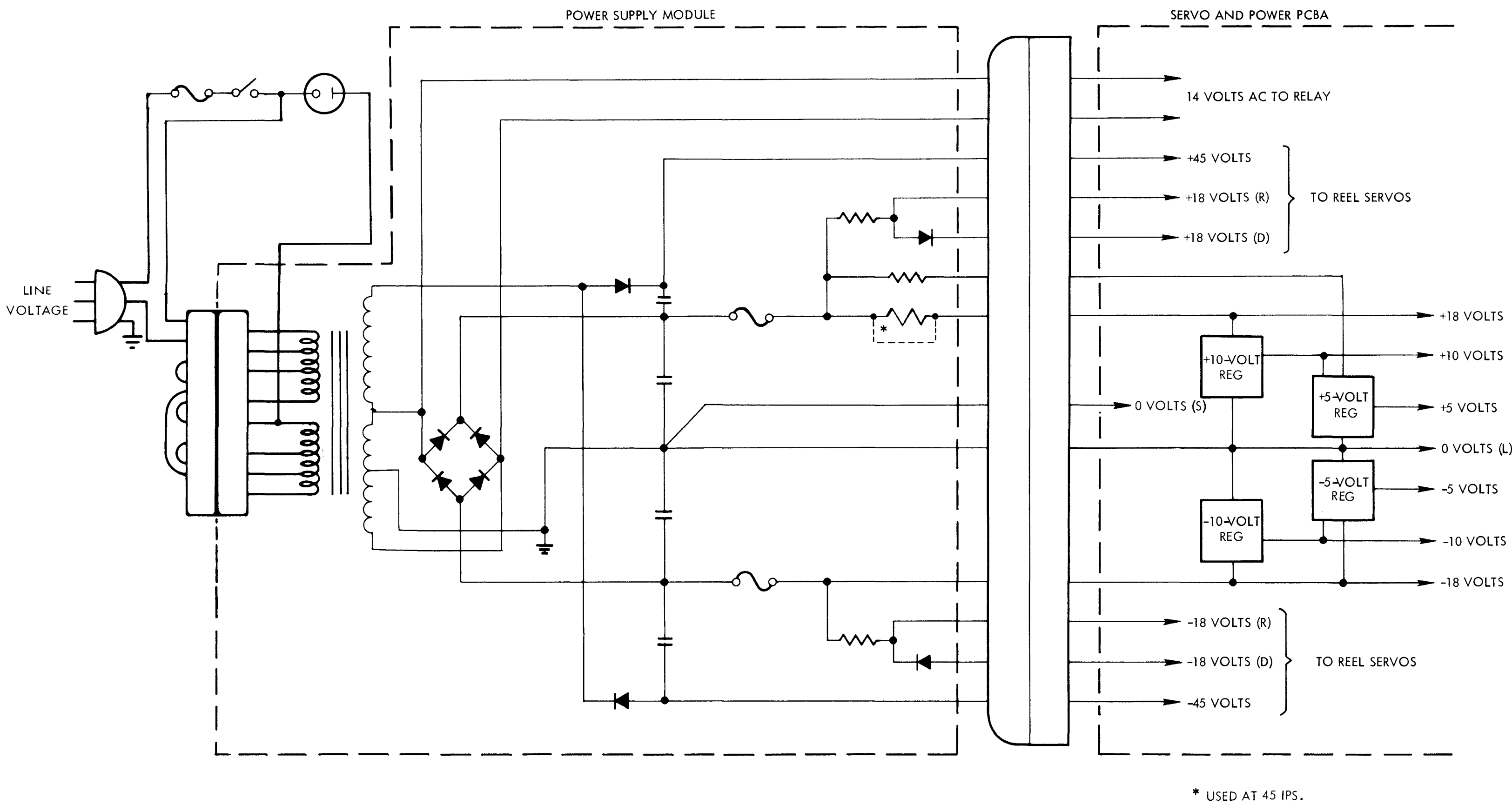
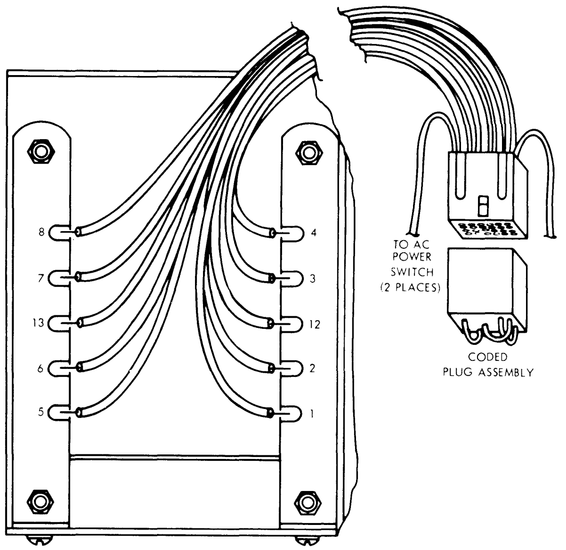


Figure 4-3. Power Supply Block Diagram



AC LINE VOLTAGE	PERTEC PART NO.	CONNECT				CONNECT	
		PIN 2 TO	PIN 23 TO	PIN 1 TO	PIN 24 TO	FROM	TO
95	104586-01	3	19	8	16		
105	104586-02	3	14	8	9		
115	104586-03	6	22	11	17		
125	104586-04	6	9	11	14		
190	104586-05	3	19			8	16
200	104586-06	3	9			8	16
210	104586-07	3	9			8	14
220	104586-08	3	9			11	16
230	104586-09	6	22			11	17
240	104586-10	6	22			11	14
250	104586-11	6	9			11	14

Figure 4-4. Transformer Primary Connections

4.3.2 CAPSTAN SERVO

Figure 4-5 is a block diagram of the capstan servo. It consists of three parts: the deck-mounted capstan drive assembly, consisting of the motor-tachometer combination and the capstan; the ramp generators on the Tape Control PCBA; and, the capstan drive amplifier on the Servo and Power Supply PCBA. A relay contact disconnects the motor when tape tension is lost.

Tape is moved by the capstan at a velocity determined by the velocity servo and the output of one of the two ramp generators. If the Forward ramp generator is selected by the logic, the voltage at resistor R1 rises at a rate corresponding to the required start time of the tape. The amplifier then accelerates the motor and the tape; the feedback voltage from the tachometer produces current in resistor R4, which tends to reduce the amplifier input current produced by the selected ramp generator. The voltage at resistor R1 stops rising after the required start time and the velocity builds up to the point where the currents in resistors R4 and R1 are approximately equal and opposite.

The Forward ramp generator is activated by the SYNCHRONOUS FORWARD Command (ISFC) or by a Load sequence. The Reverse ramp generator is activated by a SYNCHRONOUS REVERSE Command (ISRC) and the Rewind ramp generator by a REWIND Command (IRWC) — either remote or manual. When the transport is in the standby condition, neither ramp generator is activated. In this case, the capstan position is maintained by motor friction.

Both Forward and Reverse ramps rise and fall in a time calculated to produce start-stop distances of 0.19 ±0.02 inch, e.g., 8.33 milliseconds for a 45 ips transport. Typical waveforms are shown in Figure 4-6.

The Rewind ramp rise and fall times are not critical; they are approximately 0.5 second and are chosen so as to allow the reel servos to keep up with the rise and fall in tape speed.

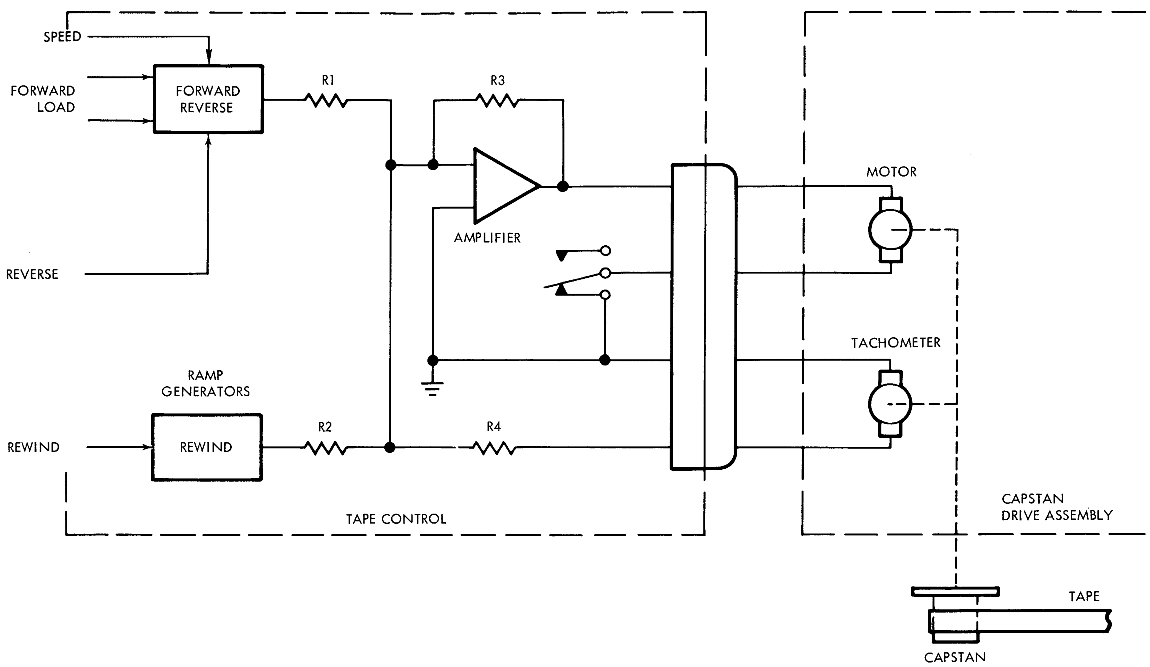


Figure 4-5. Capstan Servo Block Diagram

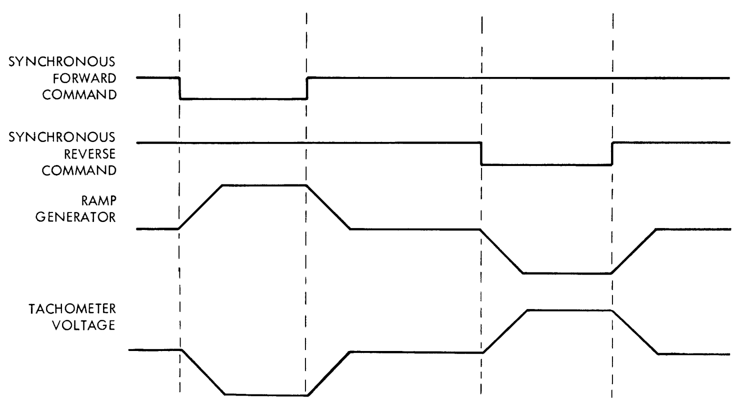


Figure 4-6. Typical Capstan Servo Waveforms

4.3.3 REEL SERVO SYSTEM

Identical position servos control the supply and take-up of tape by the reels. Figure 4-7 is a diagram of one complete reel servo together with part of a second and the relevant interconnections.

The components of the servo are: tension arm position sensor; pulleys, belt, tension arm, and tape reel; reel motor; and, servo amplifiers on the Servo and Power Supply PCBA.

The tension arms establish tape tension and isolate the inertia of the reels from the capstan. Low-friction ball bearing guides are used to minimize tape tension variations. The angular position of the tension arm is sensed by a photosensitive potentiometer which produces a voltage output proportional to the arm position. This output is amplified and drives the reel motor in the direction to center the tension arm. The geometry of the tension arm and spring ensures that only negligible tape tension changes occur as the storage arm moves through a 60° arc.

There are two basic versions of the Servo and Power Supply PCBA.

(1) *Servo and Power Supply A* utilizes a low gain linear amplifier; this provides a critically damped linear servo system which can be used at tape speeds up to 37.5 ips.

(2) *Servo and Power Supply B* utilizes a high gain amplifier in conjunction with current limiting to provide a non-linear servo system. This PCBA enables operation to be extended to a tape speed of 45 ips without changing the mechanical and electro-mechanical components of the transport.

4.3.3.1 Operation with Servo and Power Supply A PCBA

With tape stationary, the storage arms take a position such that the amplified tension arm sensor output, when applied to the reel motor, provide sufficient torque to balance the pull of the tension arm spring.

Initially, the sensor is set by rotating the shutter on the tension arm shaft so that the tension arms operate in the center of their range. The position of the tension arm changes for different steady-state tape velocities. This occurs because the amplifier output varies with the motor back-emf requiring corresponding changes in voltages from the sensor.

When the capstan injects a tape velocity transient in either direction, the arm moves and the sensor output changes, driving the reel motor in the direction to re-center the arm.

Each reel motor is driven by a linear amplifier with lead-lag servo stablization. The zero of the stabilization network is at 2.7 Hertz and the pole is at 12.8 Hertz. The low-frequency gain of the amplifier is approximately 3.6 volts per volt. With 10v across the arm sensor, the sensor gain is 4.2 volts per radian and the motor gain is 10 radians per second per volt. The motor velocity is stepped down by a pulley ratio of 4 to 1, so that the open loop gain (reel velocity divided by arm displacement) is 37.5 radians per second per radian. Thus, the arm displacement for a change in tape velocity from 37.5 ips forward to 37.5 ips reverse (an empty reel: $\pm$14.6 radians per second) is approximately 0.8 radian at 46°.

Without tape, the arm rests against the stops and the tension arm limit switch opens, de-energizing the interlock relay. When the relay is de-energized, the two reel motors are disconnected from their respective amplifiers and connected together through a low resistor (see Figure 4-7) thus providing a dynamic braking effect. The characteristics of the

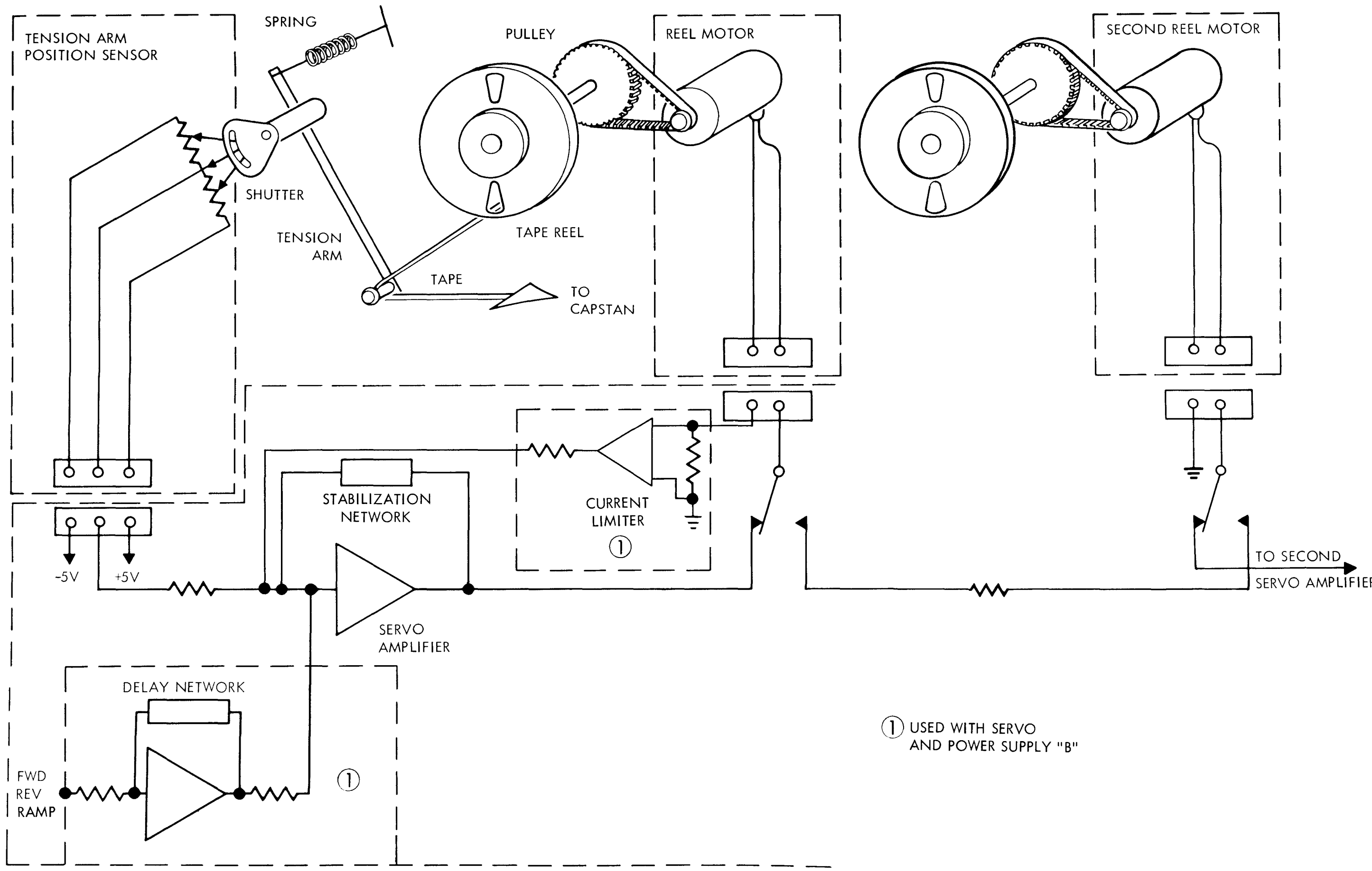


Figure 4-7. Reel Servo Diagram

884S

system ensure that when power is lost in the Rewind mode, the two reels come to rest in such a manner that tape tension is never exceeded and significant tape spillage never occurs. The dynamic braking feature is also useful when tape tension is lost in the tape unload operation.

In the Rewind mode, the characteristics of the reel servos are altered by electronic switching as follows.

(1) The relevant parts of the two reel servo amplifiers are connected to +36v and —36v instead of +18v and —18v. This allows the amplifiers to supply sufficient output voltage to enable the reel servos to follow tape speeds of 150 ips.

(2) The low frequency gain of the servos is increased by a factor of approximately 2; in addition, a voltage from the Rewind ramp generator is added to the feedback from the tension arm sensor. Therefore, the displacement of the tension arm required to generate the necessary amplifier output at 150 ips is reduced, minimizing the tension arm stroke requirements.

4.3.3.2 Operation with Servo and Power Supply B PCBA

With tape stationary, the storage arms take a position such that the amplified tension arm sensor output, when applied to the reel motor, provides sufficient torque to balance the pull of the tension arm spring.

Initially, the sensor is set by rotating the shutter on the tension arm shaft so that the tension arms operate in the center of their range.

When the capstan injects a tape velocity transient in either direction the arm moves and the high gain amplifier, together with the current limiter, cause a pre-determined current to flow in the reel motor in such a direction to recenter the arm. In addition, however, a voltage from the Forward/Reverse capstan ramp generator, suitably delayed, is subtracted from the arm sensor input. This causes the steady state displacement of the arm to be large in spite of the high amplifier gain so that storage associated with the complete arm movement is available when the capstan velocity reverses. The high amplifier gain ensures little variation in arm displacement as the reel velocity varies due to changes in effective reel diameter from an empty to full reel.

The amplifier gain is 33 volts per volt, the motor gain is 10 radians per second per volt, and the motor velocity is stepped down by 4 to 1. If the arm is displaced 0.4 radian (one-half of the total possible displacement) the output from the arm sensor gain (4.2 volts per radian) is 0.4 X 4.2 — 1.68v. The magnitude of the voltage from the Forward/Reverse ramp generator is 4.8v and the gain of the delay network is 0.305 volts per volt. Thus, the output of the delay network is 0.305 X 4.8 = 1.46v. The angular velocity of the reel, therefore, is

$$(1.68 - 1.46) \times 33 \times 10 \div 4 = 18 \text{ radians per second}$$

This corresponds to a linear tape speed of 45 ips for an empty reel (5-inch diameter). Thus, the arm displacement from 45 ips forward to 45 ips reverse is 0.8 radian. When the reel is full (10-inch diameter) the required velocity is only 9 radians per second. This requires an arm sensor input of 1.57v instead of 1.68v which corresponds to a change of arm displacement of 0.03 radian, or less than 10 percent.

The zeros of the stabilization network are at 1.45 Hz and 1.75 Hz and two poles at 0.3 Hz and 150 Hz.

Without tape, the arms rest against the stops and the tension arm limit switch opens, de-energizing the interlock relay. When the relay is de-energized, the two reel motors are disconnected from their respective amplifiers and connected together through a low resistor (see Figure 4-7) thus providing a dynamic braking effect. The characteristics of the system ensure that when power is lost in the Rewind mode, the two reels come to rest in such a manner that tape tension is never exceeded and significant tape spillage never occurs. The dynamic braking feature is also useful when tape tension is lost in the tape unload operation.

In the Rewind mode the relevant parts of the two reel servos are connected to +36v and —36v instead of +18v and —18v. This allows the amplifiers to supply sufficient output voltage to enable the reel servos to follow tape speeds of 150 ips.

4.3.4 DATA ELECTRONICS

Information is recorded in the NRZI mode, i.e., a one on the information line causes a change of direction of magnetization between positive and negative saturation levels. Two tape formats are in general use; they are the IBM 727/729 7-track format which can operate at 200, 556, and 800 cpi, and the IBM 2400 9-track format which operates at 800 cpi.

Figures 4-8 and 4-9 illustrate the relevant 9- and 7-track allocations and spacing. In the 9-track system, consecutive data channels are not allocated to consecutive tracks. This organization increases tape system reliability because the most used data channels are located near the center of the tape. Consequently, they are least subject to errors caused by contamination of the tape.

Illustrated in Figure 4-10 are waveforms that occur on a channel during a write and read-back operation. Magnetization transitions recorded on the tape are not perfectly sharp because of the limited resolution of the magnetic recording process.

During reading, the amplified read-back voltage is full-wave rectified (because no significance is attributable to the sign of the read-back voltage) and clipped to remove baseline noise. This is necessary because there is no read signal output for a recorded 0. The output of the rectifier is peak detected and a pulse generated for each 1 recorded. These pulses are fed to a set of read staticisers and then to the interface.

Figure 4-11* is a functional logic diagram of one channel of T6X40 data electronics and the relevant common control logic. This diagram is to be used only for describing system operation.

Figure 4-12* is a functional logic diagram of one channel of T6X60 data electronics and the relevant common control logic. This diagram is to be used only for describing system operation.

4.3.4.1 Operation with Dual- and Single-Stack Heads

A dual-stack head, used on the T6X40, enables simultaneous read and write operations to take place, thus allowing writing and checking of data in a single pass.

Gap scatter in both the write and read heads is held within tight limits so that correction is not necessary. However, the azimuth angles of both heads are not held within such tight limits, and correction is therefore necessary.

---

*Foldout drawing, see end of this section.

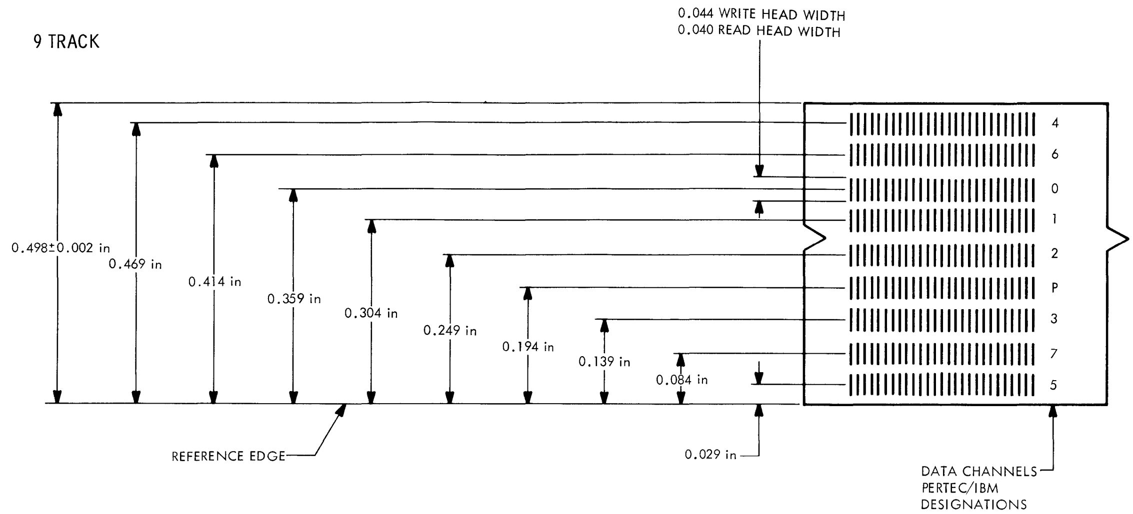


Figure 4-8. 9-Track Allocation and Spacing

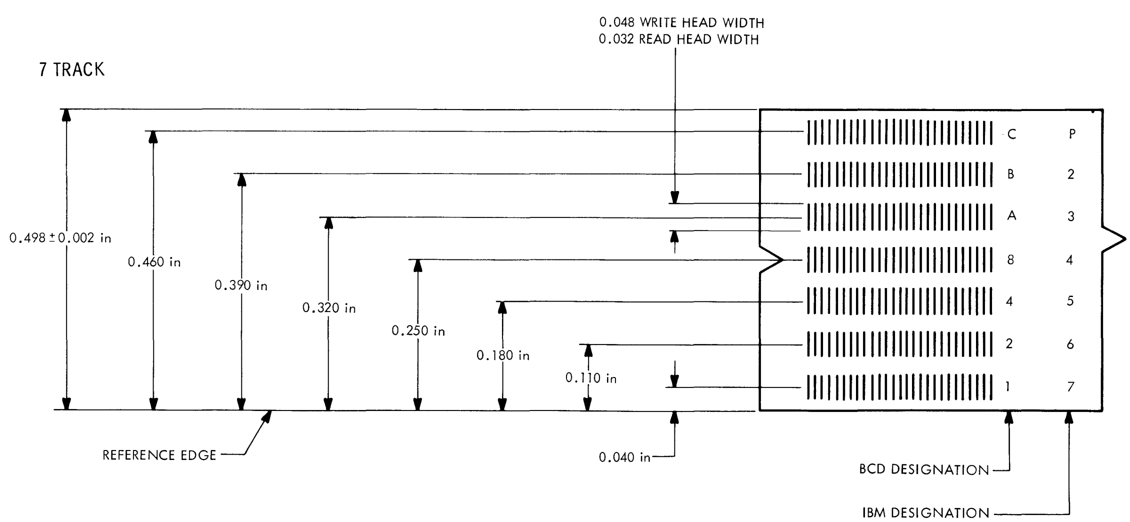


Figure 4-9. 7-track Allocation and Spacing

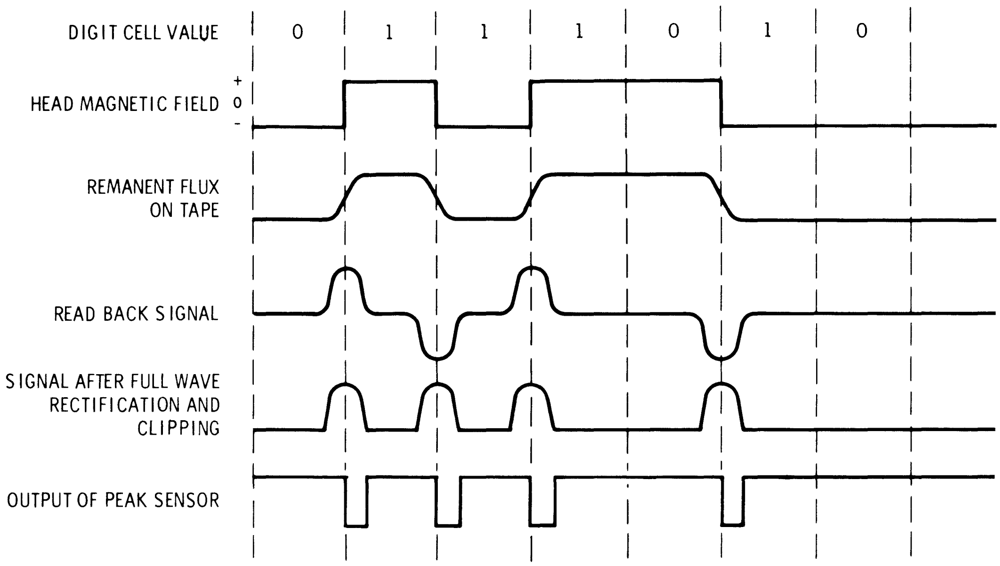


Figure 4-10. Write and Read Waveforms

The read head azimuth adjustment is provided by shimming the fixed head guides adjacent to the head so that the tape tracks at 90 degrees to the read azimuth. Since the write and read heads are constructed in the same block, an independent method of azimuth adjustment is required for the write head. This is achieved electronically by triggering the write waveform generators for different channels sequentially and at such times that the azimuth error in the write head is nullified.

The T6X60 transport utilizes a single-stack head for both read and write operations. Azimuth alignment for the single-stack head is accomplished by shimming the fixed head guides adjacent to the head so the tape will track at exactly 90 degrees to the head gap. Since the same gap is used for both reading and writing, no additional azimuth compensation is required.

4.3.4.2 Data Recording (Dual-Stack Model T6X40)

Figure 4-13* shows a timing diagram for data recording in T6X40 models. Assume that the transport is Selected, Ready, On-line, and has a Write Enable ring installed. The WRT PWR control line will therefore be at +5v, providing power for the head driver circuits.

When a SYNCHRONOUS FORWARD command is received, the MOTION signal generated on the Tape Control PCBA goes high, removing one input of OR gate U8. See Figure 4-11.

In operation, the front edge of the SYNCHRONOUS FORWARD command is delayed and differentiated and the resulting pulse is used to sample the condition of the SET WRITE STATUS line. If this is true, the following action takes place.

(1) The Write/Read mode flip-flop U20 (see Paragraph 4.3.5.6) is set.

(2) The NWRT waveform becomes low.

(3) Erase driver Q3 is energized.

---

*Foldout drawing, see end of this section.

(4) Both the S_D and C_D inputs of flip-flop U4 go high. The action of the *stretcher* circuit is to delay the rise of the C_D input relative to the S_D input, ensuring that the flip-flop is in the reset state before a recording starts.

The polarity of the field from the erase and write heads under these conditions is such that tape will be erased in an IBM-compatible direction.

(5) The C_D input of control flip-flop U9 goes high, unclamping the flip-flop.

The ISFC command (Plot 1 on Figure 4-13) also enables the ramp generator, which causes tape to accelerate to the prescribed velocity (Plot 2). After a time (T1) determined by the required IRG displacement, the WRITE DATA inputs, together with the IWDS are supplied to the interface connector.

The WRITE DATA (IWD*) input is received by interface receiver U1 and, when true, enables one input of AND gate U2. The IWDS pulse is received by interface receiver U5 and fed to AND gate U2. The output of gate U2 is thus a positive-going pulse at WDS time. The leading edge of the positive-going pulse from U2 enables the J input of the J-K write waveform generator flip-flop U4 directly, and also the K input of the flip-flop via OR gate U3. Since the clock input of U4 is high at this time, the master section of U4 is toggled whenever the IWD signal is true.

Each IWDS (Plot 3) is also fed to flip-flop U9 which is set on the trailing edge (Plot 4). This unclamps the oscillator, which then generates a series of pulses at a high frequency (Plot 5). The pulses are fed to the shift register, which produces ten negative-going outputs consecutively on ten wires.

The outputs (T1 through T9) are used to toggle the output (slave) sections of the write waveform generator flip-flops (U4 typically) in the appropriate time order so as to achieve azimuth deskewing of the recording system. Plots 6 and 7 show the write current in the IWD5 and IWD2 channels for a 9-track system. The tenth output (T10) resets flip-flop U9, terminating the sequence of events. In practice, the oscillator frequency is adjusted to compensate for the azimuth error in the particular head being used.

Both outputs of flip-flop U4 are fed to head driver transistors Q1 and Q2 which cause current to flow in one half or the other of the center-tap head winding. Consequently, magnetization on the tape is maintained in the appropriate direction between changeovers and changes direction for each one bit to be recorded (as required by the IBM NRZI format).

At the end of each record, check characters have to be recorded and an IRG inserted. Figures 4-14 and 4-15 show the IBM IRG format for 9- and 7-track systems, respectively.

In a 9-track system, both a CRCC and LRCC are written. The CRC character is supplied by the customer to the interface, together with a single IWDS signal whose trailing edge is separated by four character times from the trailing edge of the last IWDS. The LRC character is written by resetting all the write waveform generator flip-flops using the WRITE AMPLIFIER RESET signal (IWARS) received by interface receiver U6. The timing of this reset operation is controlled by the leading edge of the IWARS signal, which should be separated by eight character times from the trailing edge of the last IWDS (Plot 8).

The output of U6 is fed to OR gate U3 and the positive-going output is fed to the K input of the write waveform generator flip-flops (typically U4) and resets the master sections of these flip-flops. In addition, the leading edge of the IWARS signal is differentiated and sets flip-flop U9.

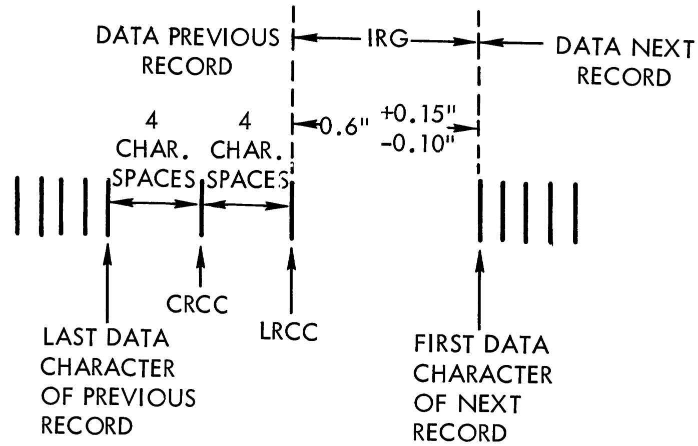


Figure 4-14. 9-Track IRG Format

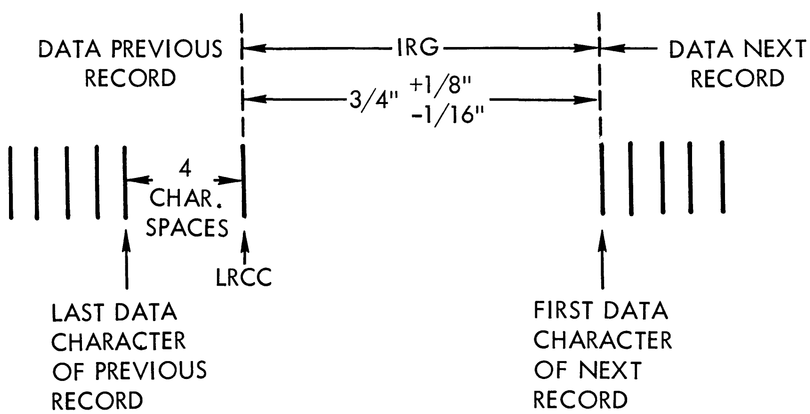


Figure 4-15. 7-Track IRG Format

A sequence of pulses is produced as described, which toggles the write waveform generator flip-flops to the reset state in the appropriate order. The LRCC is written such that the total number of magnetization transitions in any track is even.

In a 7-track system, only the LRCC is written; this is achieved again by the IWARS signal. Consequently, the leading edge must be separated four character times from the trailing edge of the last IWDS.

When the LRCC has been recorded, the ISFC command goes false after the post-record delay time (T2), the ramp generator is disabled and the tape decelerates to zero velocity.

The IRG displacement consists of the following.

(1) The stop distance: the distance traveled during the tape deceleration period to zero velocity.

(2) The start distance: the distance traveled while the tape is accelerating to the prescribed velocity.

(3) An additional distance determined by the pre-record time (T1), from the SFC command going true to the time of the first IWDS and the post-record time (T2) from the LRCC to the ISFC going false. (Time delays T1 and T2 are provided by the customer's controller.)

To separate files of information on tape, a file gap is used. This is identified by a special character on the tape followed by its LRC character. Figures 4-16 and 4-17 describe the IBM file gap formats for 9- and 7-track systems, respectively.

A file gap is inserted under external control by the customer controller. An SFC is given, followed at the appropriate time by the File Mark character (a 1 in data bit positions IWD4, 5, 6, and 7 for 7-track systems, and a 1 in data bit positions IWD3, 6, and 7 for 9-track systems), together with its IWDS, followed by the LRC character (written using the IWARS signal) after four character times in a 7-track system, and after eight character times in a 9-track system.

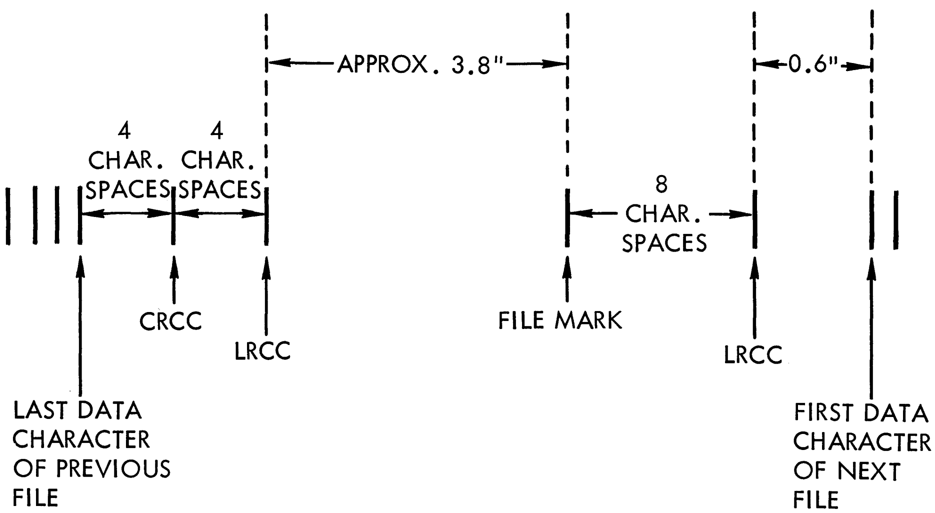


Figure 4-16. 9-Track File Gap Format

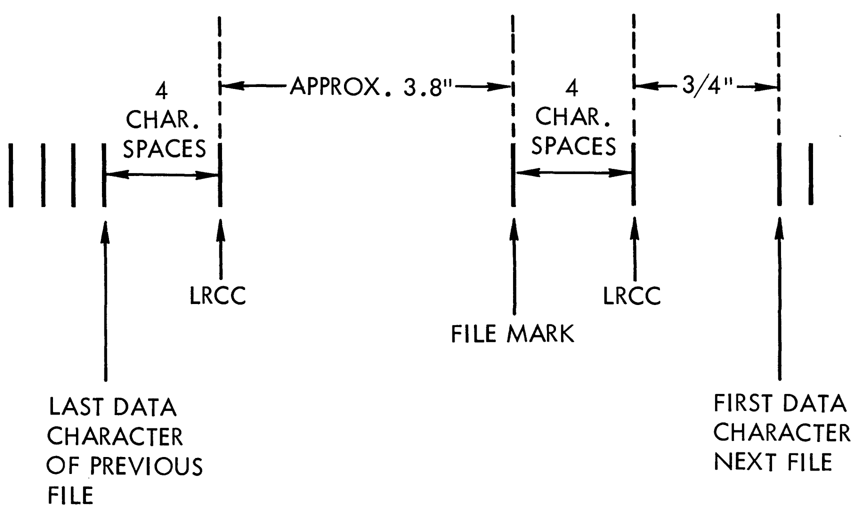


Figure 4-17. 7-Track File Gap Format

4.3.4.3 Data Recording (Single-Stack Model T6X60)

Figure 4-18* shows a timing diagram for data recording. To write a record, the transport must be Selected, Ready, On-line, and have a Write Enable ring installed. The WRT PWR control line will therefore be at +5v providing power for the head driver circuits.

When a SYNCHRONOUS FORWARD command (ISFC) is received, the MOTION signal generated on the Tape Control PCBA goes high removing the reset signal on flip-flop U5.

In operation, the front edge of the ISFC is delayed and differentiated and the resulting pulse used to sample the condition of the SET WRITE STATUS line. If this is true, the following action occurs.

(1) The Write/Read mode flip-flop U20 (see Paragraph 4.3.5.6) is set.

(2) The NWRT waveform becomes low.

(3) The erase driver Q3 is energized.

(4) Both the S_D and C_D inputs of flip-flop U5 go high. The action of the *stretcher* circuit is to delay the rise of the C_D input relative to the S_D input, ensuring that the flip-flop is in the reset state before recording commences.

The polarity of the field from the erase and write heads under these conditions is such that tape will be erased in an IBM-compatible direction.

The ISFC also enables the ramp generator which causes the tape to accelerate to the prescribed velocity. After a time (T1) determined by the required IRG displacement, the WRITE DATA (IWD) inputs, together with the WRITE DATA STROBE (IWDS), are supplied to the interface connectors.

The IWD input is received by interface receiver U1 (see Figure 4-12) and, when true, enables both the J and K inputs of flip-flop U5. IWDS signals are received by interface receiver U2 and will cause flip-flop U5 to change state on the trailing edge of the strobe, provided the IWD signal is true at this time.

The characteristics of the flip-flop are such that the IWD signal must be stable (in the appropriate direction) throughout the period of the strobe.

Both outputs of flip-flop U5 are fed to the head driver circuit which causes current to flow in one half or the other half of the center-tapped head winding. Consequently, magnetization of the tape is maintained in the appropriate direction between changeovers and changes direction for each 1 bit to be recorded (as required by the NRZI format).

At the end of each record, check characters have to be recorded and an IRG inserted. Figures 4-14 and 4-15 show the IBM IRG format for 9- and 7-track systems.

In a 9-track system, both a CRCC and LRCC are written. The CRC character is supplied by the customer to the interface, together with a single IWDS signal whose trailing edge is separated by four character times from that of the last IWDS. The LRC character is written by resetting all the write flip-flops with OR gate U6, using the WRITE AMPLIFIER RESET (IWARS) signal received by interface receiver U4. The write flip-flops are reset on the leading edge of IWARS, which should be separated by eight character times from the trailing edge of the last IWDS.

The LRCC is written such that the total number of magnetization transitions in any track is even.

---

*Foldout drawing, see end of this section.

In a 7-track system, only the LRCC is written; this is achieved by the IWARS signal. In this case, the leading edge must be separated four character times from the trailing edge of the last IWDS.

When the LRCC has been recorded, ISFC goes false, the ramp generator is disabled, and the tape decelerates to zero velocity.

The IRG displacement consists of the following.

(1) The stop distance: the distance traveled during the tape deceleration period to zero velocity.

(2) The start distance: the distance traveled while the tape is accelerating to the prescribed velocity.

(3) An additional distance determined by the pre-record time T1, from ISFC going true to the time of the first IWDS and the post-record time T2 from the LRCC to ISFC going false. (Time delays T1 and T2 are provided by the customer's controller.)

To separate files of information on tape, a File Gap is used. This is identified by a special character on the tape followed by its LRC character. Figures 4-16 and 4-17 describe the IBM file gap formats for 9- and 7-track systems.

A File Gap is inserted under external control by the customer's controller.

An ISFC is given, followed at the appropriate time by the File Mark character (a 1 in data bit positions IWD4, 5, 6, and 7 for 7-track systems, and a 1 in data bit positions IWD3, 6, and 7 for 9-track systems), together with its IWDS followed by the LRC character (written using the IWARS signal) after four character times in a 7-track system and after eight character times in a 9-track system.

4.3.4.4 Overwrite (IOVW) (T6X40, T6X60)

The Overwrite function allows updating (rewriting) of a selected record. The new data block to be inserted must be exactly the same length as the data block being replaced. This restriction is necessary since replacing a block of data with a block longer than the original could result in an IRG distance which is less than the minimum allowed, or in writing over the next record. If the new data is shorter than the existing block, errors could result since some unerased portion of the old data would remain.

Additionally, when write and erase currents are switched off abruptly there is a small area of tape which is influenced by the collapsing magnetic fields of the heads. This constitutes flux transients on the tape which appear as spurious signals when read back. The Overwrite feature of the transport has effectively eliminated this problem by turning the write current off slowly while tape is still in motion.

NOTE

Refer to PERTEC Application Note No. 70711 concerning the control and timing restrictions associated with Overwrite.

To update a previously recorded record the transport must be Selected, Ready, On-line, and have a Write Enable ring installed. Additionally, the Overwrite (IOVW) signal from the controller must be true and coincident with ISWS and ISFC.

Overwrite operation is terminated by the IWARS signal disabling the WRT PWR circuitry. This action causes the write current to ramp down to zero as the tape decelerates to rest. The transient pulse, generated when the write current is switched off, is spread over a longer distance on the tape and produces a negligible signal on replay.

4.3.4.5 Data Reproduction (T6X40)

When an ISFC is received, the following occurs (refer to Figure 4-11).

(1) The MOTION signal generated on the Tape Control PCBA goes true so that the output of OR gate U15 correspondingly will go high, thus removing the reset signal from the read staticiser flip-flops (typically U14).

(2) The Forward ramp generator is enabled and tape accelerates to the prescribed velocity.

Data signals from the magnetic head at a level of approximately 10 to 20mv peak-to-peak are fed by a shielded cable to the read amplifier. The amplifier output at a level of approximately 10.5v peak-to-peak is full-wave rectified and baseline clipped. The clip level is variable and is under control of the NWRT waveform.

In a dual-gap transport, the read system always operates whether the transport is in the Write or Read mode. However, in the Write mode where the reading facility is used to check the data that have been recorded, the NWRT waveform is low and a high clip level of 50 percent is generated. This ensures that data are written with enough margin to ensure data recovery when tape is read on another transport.

If the transport is in the Read mode, the NWRT waveform is high and a clip level of approximately 20 percent is generated, which is only sufficient to reject system noise. After clipping, the signal is fed to a feedback differentiator which generates an edge bearing a fixed time relationship (ideally zero delay) to the peak of the input signal. This edge is differentiated by differentiator $\delta 2$ to form a pulse for each 1 bit detected. Plots 1 and 2 in Figure 4-19* show outputs from the read amplifier for two different channels. In general, skew will exist between the signals as shown. Plots 3 and 4 are the pulse outputs from the peak detector differentiator for the two channels.

The output pulse from differentiator $\delta 2$ is fed to the clock input of the read staticiser flip-flop U14. This flip-flop is set on the negative-going edge of the pulse (Plots 5 and 6 in Figure 4-19).

The Q output from U14 is fed to interface driver U16 while the $\bar{Q}$ output is fed to OR gate U11, where it is ORed with the corresponding outputs of the other channels so that the first data 1 of a character causes the output of U11 to go high (Plot 7), enabling the run-down circuit. The circuit is set for half-a-character period and at the end of this time the output goes low. This edge is differentiated by differentiator $\delta 3$ and generates a nominal 2 μsec IRDS (Plot 8), which is fed to interface driver U17.

The output of the rundown circuit is also delayed and resets the read staticiser flip-flops (typically U14) via OR gate U15. This causes the $\bar{Q}$ outputs of all read staticiser flip-flops to go high and the rundown circuit is therefore clamped back to its quiescent level. The delay in the loop prevents the READ DATA interface lines from resetting before the trailing edge of IRDS.

After the last character of a record has been read (the LRC character), the SFC goes false, the Forward ramp generator is disabled, and tape decelerates to rest. In addition, the MOTION signal goes false, applying a reset signal to flip-flop U14 via OR gate U15. (Reproduction in reverse is identical.)

By varying the timing of the rundown circuit, the read staticiser may be used at different packing densities as required for 7-track operation. Control of this timing is provided by the HI DEN manual control on the transport via OR gate U13. Alternatively, the IDDS interface line can be used to provide the same function.

---

*Foldout drawing, see end of this section.

4.3.4.6 Data Reproduction (T6X60)

When an ISFC is received, the following occurs (refer to Figure 4-19).

(1) The MOTION signal generated on the Tape Control PCBA goes true so that the output of OR gate U10 correspondingly will go high, thus removing the reset signal from the Read Staticiser flip-flops (typically U11).

(2) The Forward ramp generator is enabled and tape accelerates to the prescribed velocity.

Data signals from the magnetic head at a level of approximately 10 to 20mv peak-to-peak are transmitted by a shielded cable to the connector on the Data PCBA. When the transport is in the Read mode, both Q1 and Q2 (see Figure 4-12) are turned off. The read amplifier boosts the signal level to 12v peak-to-peak. The signal is full-wave rectified and baseline clipped. The clip level is variable and controlled by the READ THRESHOLD (IRTH) interface line. A false level results in approximately a 20-percent clip level and should be used when reading a pre-recorded tape. A true level results in approximately a 50-percent clip level and should be used when performing a read-after-write check.

The high clip level ensures that data are written with enough margin to ensure data recovery when the tape is read on another transport.

After clipping, the signal is fed to a feedback differentiator which generates an edge bearing a fixed time relationship (ideally zero delay) to the peak of the input signal. This edge is differentiated by differentiator $\delta 1$ to form a pulse for each 1 bit detected. Plots 1 and 2 (Figure 4-19) show outputs from the read amplifier for two different channels. In general, skew will exist between the signals as shown. Plots 3 and 4 are the pulse outputs from the peak detector differentiator for the two channels.

The output pulse from differentiator $\delta 1$ is fed to the toggle input of the read staticiser flip-flop U11. This flip-flop is set on the negative-going edge of the pulse (Plots 5 and 6).

The Q output from U11 is fed to the interface driver U13 while the $\overline{Q}$ output is fed to OR gate U7, where it is ORed with the corresponding outputs of the other channels so that the first data 1 of a character causes the output of U7 to go low (Plot 7), enabling the run-down circuits.

The circuit is set for half a character period and at the end of this time the output goes low. This edge is differentiated by differentiator $\delta 2$ and generates a 2 μsec RDS (Plot 8) which is fed to the interface driver U12.

The output of the run-down circuit is also delayed and resets the read staticiser flip-flop U11 via OR gate U10. This, in turn, causes the $\overline{Q}$ outputs of all read staticiser flip-flops to go high and the run-down circuit is therefore clamped back to its quiescent level. The delay in the loop prevents the read data interface lines resetting before the trailing edge of the RDS.

After the last character of a record has been read (the LRC character) ISFC goes false, the Forward ramp generator is disabled, and the tape decelerates to rest. In addition, the MOTION signal goes false, applying a reset signal to flip-flop U11 via OR gate U10. (Reproduction in reverse is identical except for tape direction.)

By varying the timing of the run-down circuit, the read staticiser may be used at different packing densities as required for 7-track operation. Control of this timing is provided by the HI DEN manual control on the transport via OR gate U9. Alternatively, the DATA DENSITY SELECT (IDDS) interface line can be used to provide the same function.

4.3.5 TAPE CONTROL SYSTEM

The second major electronic subsystem consists of the circuits necessary to control tape motion. This includes manual controls, interlocks, and logic. Operation can best be described by detailing the Bring-to-Load-Point sequence, subsequent tape motion commands, Rewind sequence, and subsequent unloading of tape. Figure 4-20* is a functional logic diagram of the Tape Control system.

4.3.5.1 Bring-to-Load-Point System

The system will be described by considering the sequence required to bring a tape to the BOT (or Load Point). Figure 4-21* shows the waveforms during the operation.

Associated with each of the manual control switches is a *switch clean-up* flip-flop (U1, U2, U25) which eliminates the problems of a switch contact bounce. Relay K1 has four changeover contacts, three of which (K1A, K1B, and K1C) are used to disconnect the reel and capstan servo motors, and the fourth (K1D) is used in conjunction with the tension arm limit switch as a system interlock. The tension arm limit switch is operated by a cam on the supply reel tension arm and is closed when the cam is in its normal operating position. The tension arm limit switch opens at both extremes of the arm travel so that protection against over-tension, as well as under-tension, conditions is provided.

The Write Lockout (WLO) switch is located on the File Protect assembly located behind the supply reel. The switch is closed when a Write Enable ring is mounted on the supply reel. The probe, which detects the Write Enable ring, is retracted when power is switched on and K1D is closed. A solenoid whose transistor driver is supplied with base currents through the WLO switch and K1D retracts the probe. Write current is also supplied on demand through K1D and the WLO switch.

4.3.5.2 Actuate POWER Control

When power is turned on initially (Plot 1), the relay contacts on the tension arm limit switch are open. The INTLK signal is low and is connected either directly or through OR gate U30 to the reset inputs of the five control flip-flops RW1, RW2, RW3, Load, and FLR (U15, U16, U17, U18, and U31).

4.3.5.3 Depress LOAD Control (First Time)

When the LOAD control is depressed for the first time (Plot 3), the relay driver for K1 is turned on, the four contacts close, activating the reel servos which tension the tape, thus closing the tension arm limit switch. The tension arm limit switch supplies an alternate source of base current for the delay driver, thus latching the relay (which remains activated after the LOAD control is released). When K1D closes, a high level appears at the INTLK output (Plot 2), removing the reset signal from the control flip-flops. Load flip-flop U18 is not set by the first operation of the LOAD control because, at the time the C input of U18 goes low (which normally sets the flip-flop), the INTLK signal is still holding the reset input low (closure of the relay contacts is delayed from the appearance of the command level by several milliseconds while the relay contacts close).

If, at any time, the tension arm moves outside its operating region, the interlock relay de-energizes, power is disconnected from the motors, and the INTLK signal returns to the low state, resetting the five control flip-flops.

---
*Foldout drawing, see end of this section.

4.3.5.4 Depress LOAD Control (Second Time)

When the LOAD control is depressed momentarily a second time (Plot 3), the following sequence occurs.

(1) Since the INTLK signal is high, the Load flip-flop U18 and the FLR flip-flop U31 set (Plots 4 and 5). The Q output of U18 is fed to one input of OR gate U21. The output of OR gate U21 goes low, enabling the Forward ramp generator that drives the capstan servo (not shown). The tape accelerates to the specified speed (Plot 9) and continues to move until the BOT tab reaches the BOT sensor, at which time the BOT signal goes high, enabling one input of AND gate U29. In addition, the single-shot is triggered, generating an 0.5-sec negative-going waveform (NBOTD) (Plot 7).

(2) Since the LOAD waveform and the output of gate U28 are high at this time, AND gate U29 is enabled (Plot 10) and the Load flip-flop is reset. This causes tape to decelerate to rest with the photo-tab under the photo-tab sensor. At this time, all three inputs to AND gate U41 are high so that the NLDP waveform is low (Plot 11), indicating that the transport is at Load Point and enabling the Load lamp driver.

(3) At the end of the 0.5-sec delay, the NBOTD waveform (Plot 7) goes high and, since the other two inputs to AND gate U38 are both high at this time, the NREADY waveform at the output of gate U38 goes low (Plot 8), enabling one input of AND gate U39.

(4) The setting of the FLR flip-flop causes the NFLR waveform to go low, disabling AND gate U10 and thus inhibiting the possibility of further manual LOAD commands.

4.3.5.5 Depress ON LINE Control

If the ON LINE control is momentarily depressed, On-line flip-flop U26 is set (if it is depressed a second time, U26 is reset), and the second input of AND gate U39 is enabled. The $\bar{Q}$ output of the flip-flop U26 enables the On-line lamp driver. The output of gate U39 goes high, indicating that the transport is Ready and On-line (RO). If the transport is also selected, the output of AND gate U40, the Selected, Ready, On-line (SRO) waveform goes high.

When the transport is On-line, the output of the manual REWIND control flip-flop is disabled by NONLINE at gate U12.

If the transport is Selected, the ISLT waveform is low. The following options are available.

(1) If W4 is not present, then the ISLT waveform goes high-true when the transport is Selected.

(2) If W4 is present, ISLT only goes true if the transport is Selected and On-line.

(3) If W3 is not present, the SLTA waveform is permanently high and the status lines are enabled. This option is used when interrogation of transport status lines is required, whether the transport is Selected or not.

(4) If W3 is present, the status lines are gated with the ISLT waveform.

When the FLR or INTLK waveforms are low, the On-line flip-flop is held reset by OR gates U23 and U24, ensuring that the On-line flip-flop cannot be set until the interlock has been made and the First Load Rewind sequence has been entered. The On-line flip-flop can also be reset from the interface by the OFF-LINE command (IOFFC) via interface receiver U22 and OR gate U24.

The transport is now ready to receive external commands.

4.3.5.6 Operation From External Commands

Assuming the transport is Selected, Ready, and On-Line (SRO is high), receipt of an ISFC will cause the output of interface receiver U4 to go high and the output of AND gate U6 to go low. The MOTION signal will go high and the Forward ramp generator will be enabled via OR gate U21.

The MOTION signal is delayed approximately 10 μsec, differentiated, and a positive-going GO pulse generated at the output of differentiator δ1. This pulse samples the status of the SET WRITE STATUS (ISWS) line. If ISWS is true, indicating that the Write mode is required, then Write/Read flip-flop U20 is set and the NWRT waveform goes low. If ISWS is false, U20 is reset and the NWRT waveform goes high. For a SYNCHRONOUS REVERSE command, a similar sequence of events occurs.

If the BOT tab is encountered during the execution of an ISRC, the BOT signal goes high, the NBOT signal goes low, and the single-shot is triggered. As a result, AND gate U7 is disabled, inhibiting the action of ISRC and the NBOTD waveform goes low for 0.5 sec so that the transport becomes Not Ready for this period of time.

4.3.5.7 Operation From Control Panel — Forward

Forward tape motion in response to a remote input command was described in Paragraph 4.3.5.6. When the transport is in the Off-line mode (NONLINE is true) and the FORWARD control is depressed, tape will advance at the specified speed until the FORWARD control is again depressed (or until the transport is placed in the On-line mode).

NOTE

The FORWARD control should be de-activated prior to placing the transport in the On-line mode. Failure to de-activate the FORWARD control will cause the tape to advance the next time the transport is placed in the Off-line mode.

The transport cannot write information on tape when motion is caused by the FORWARD command since the Write/Read flip-flop is held reset.

4.3.5.8 Operation From Control Panel — Reverse

Reverse operation is identical to Forward operation as described in Paragraph 4.3.5.7, except for tape motion direction.

4.3.5.9 Rewind Sequence, Case 1 — Tape Not at Load Point

This is the normal Rewind to Load Point sequence that results from either a remote or manual command. Figure 4-22* shows the waveforms that occur during the operation.

In response to either a remote or manual command, the RW1 flip-flop is set (Plot 3). The Q output of the flip-flop enables the Rewind ramp generator via AND gate U28 (since the $\bar{Q}$ output of the RW3 flip-flop is high at this time) and the tape accelerates to a reverse velocity of 150 ips in approximately 0.5 sec (Plot 13). In addition, when flip-flop RW1 is set, the output of gate U33 goes low, disabling AND gate U38 and causing the SRO waveform to go false (Plot 12).

When the BOT tab is detected, flip-flop RW2 is set on the leading edge of the BOT waveform (Plot 6), flip-flop RW3 is set on the trailing edge (Plot 7) and the 0.5-sec single-shot is triggered (Plot 8). The $\bar{Q}$ output of flip-flop RW3 goes low, disabling AND gate U28. The output of gate U28 goes high, disabling the Rewind ramp generator so that the tape decelerates to rest.

*Foldout drawing, see end of this section.

At the end of the 0.5-sec delay, the trailing edge of the NBOTD waveform is differentiated by differentiator $\delta 2$ generating a positive-going BOTDP pulse (Plot 9). Since the Q output of flip-flop RW3 is high at this time, Load flip-flop U18 is set via gates U9 and U11. This enables the Forward ramp generator.

The characteristics of the ramp generators are such that the BOT tab overshoots the photosensor and then returns. When the BOT tab is detected for the second time, the 0.5-sec single-shot is triggered (Plot 8), AND gate U29 is enabled and its output goes low, resetting the RW1, RW2, RW3, and Load flip-flops (Plots 3, 6, 7, and 10). The Forward ramp generator is thus disabled and the tape decelerates to rest. The delay between the LOAD waveform and AND gate U29 ensures that the reset waveform is the appropriate length. At the end of the 0.5-sec period, the NBOTD waveform goes high and, since the other two inputs are high at this time, gate U38 is enabled and the SRO waveform goes true.

The RW1 waveform (Plot 3) is true throughout the Rewind sequence and is used to generate the REWINDING (IRWD) interface waveform.

4.3.5.10 Rewind Sequence, Case 2 — Tape at Load Point

A manual REWIND command initiates the Rewind sequence as previously described. However, in this case the tape unwinds from the take-up reel and tape tension is lost. Remote REWIND commands are inhibited by the NBOT waveform on AND gate U13, i.e., it is impossible to unload tape remotely — operator intervention is required.

4.3.5.11 Ready Mode From Tape Not at Load Point

An option is available which allows the transport to be placed in the Ready mode after a power-off, power-on sequence even though tape has previously been brought beyond the Load Point, e.g., in the middle of a reel.

When this option is present (by deleting jumper W4), depress the LOAD control once to establish tape tension, then depress the ON LINE control. The Ready line will go true and the transport can accept remote commands.

4.3.5.12 Data Density Select

This remote input command is applicable only to 7-track systems. A negative-true level at the DATA DENSITY SELECT (IDDS) input will disable the Hi Density lamp driver, indicating the lower density condition.

The NHID signal is routed to the Data PCBA to enable the appropriate density conditioning for the system.

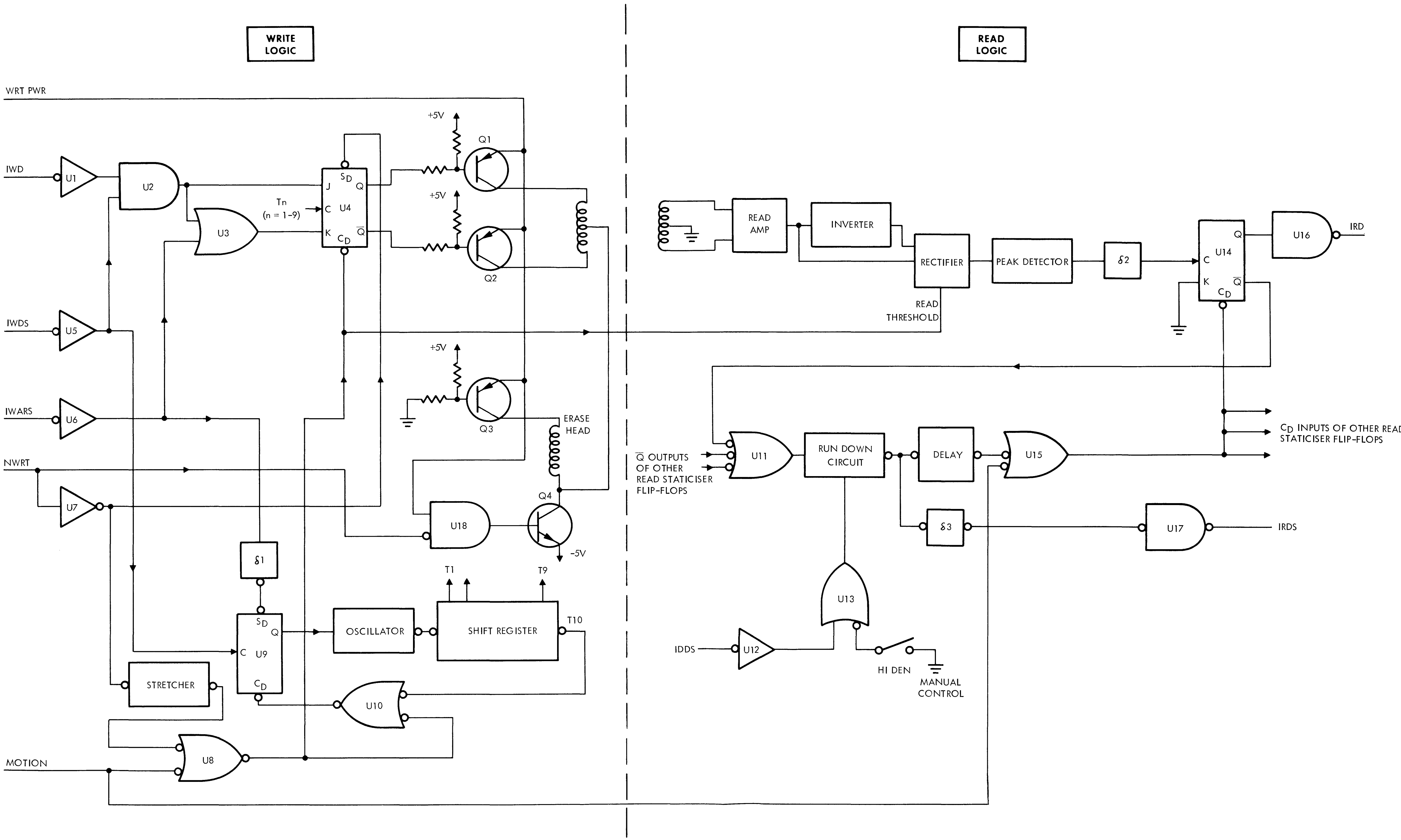


Figure 4-11. One Channel of T6X40 Data Electronics, Block Diagram

884S

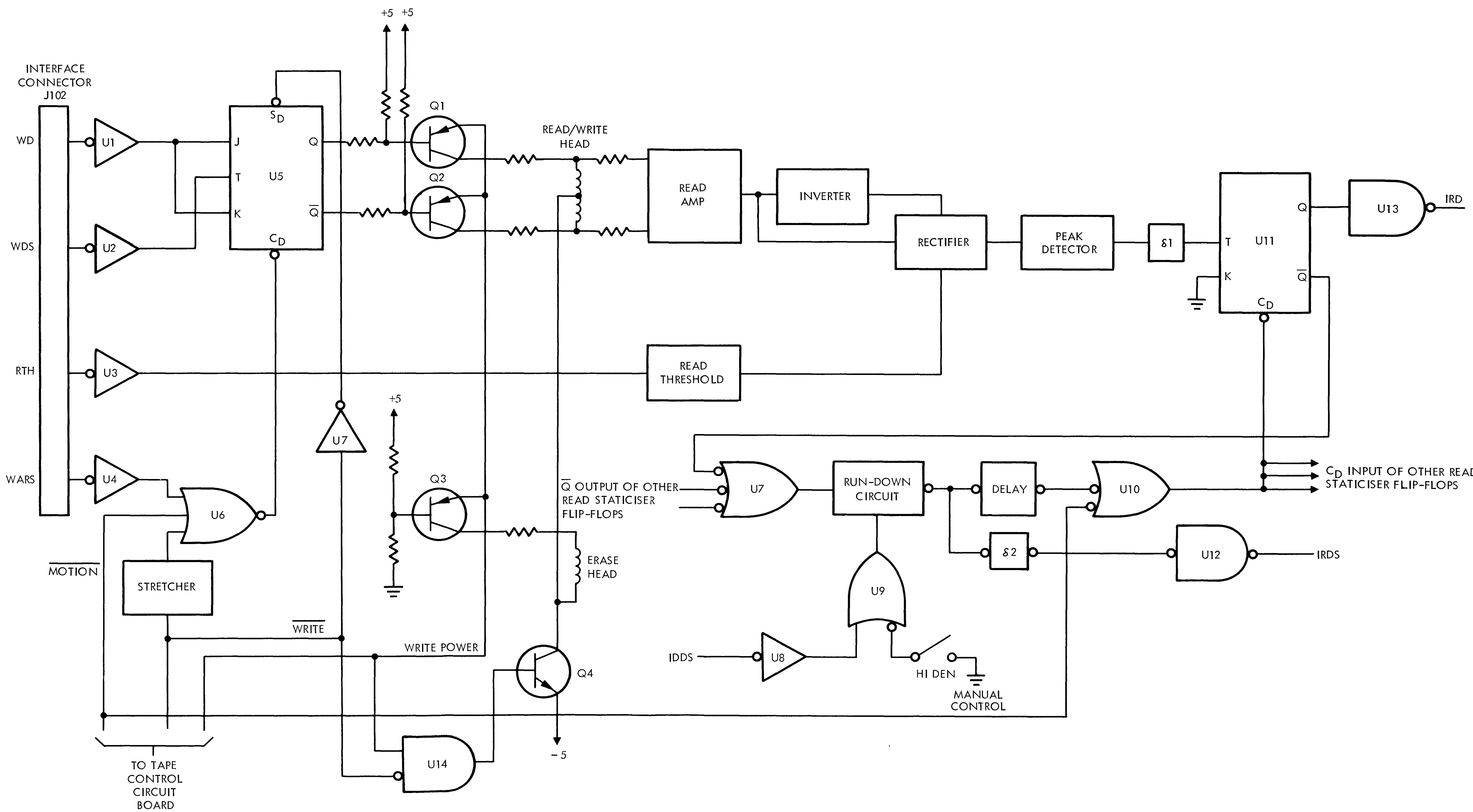
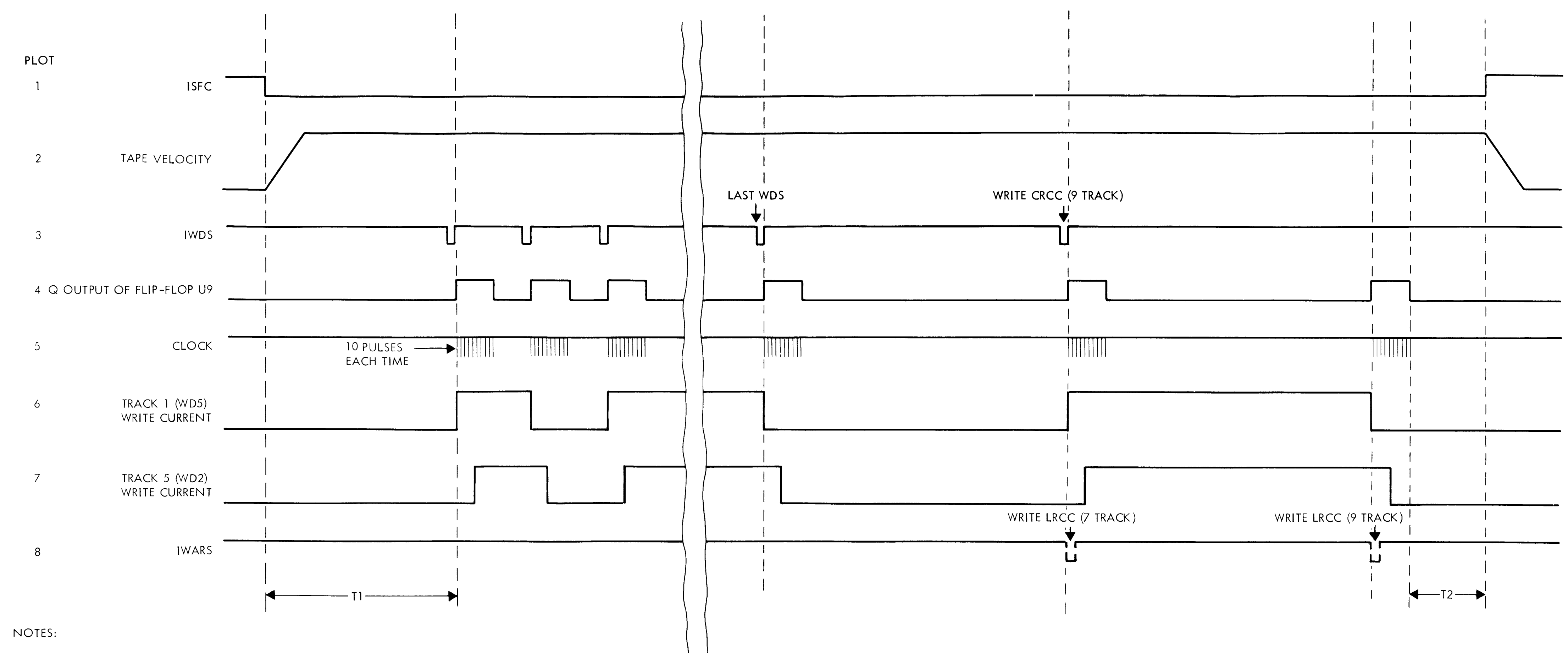


Figure 4-12. One Channel of T6X60 Data Electronics, Block Diagram

884S

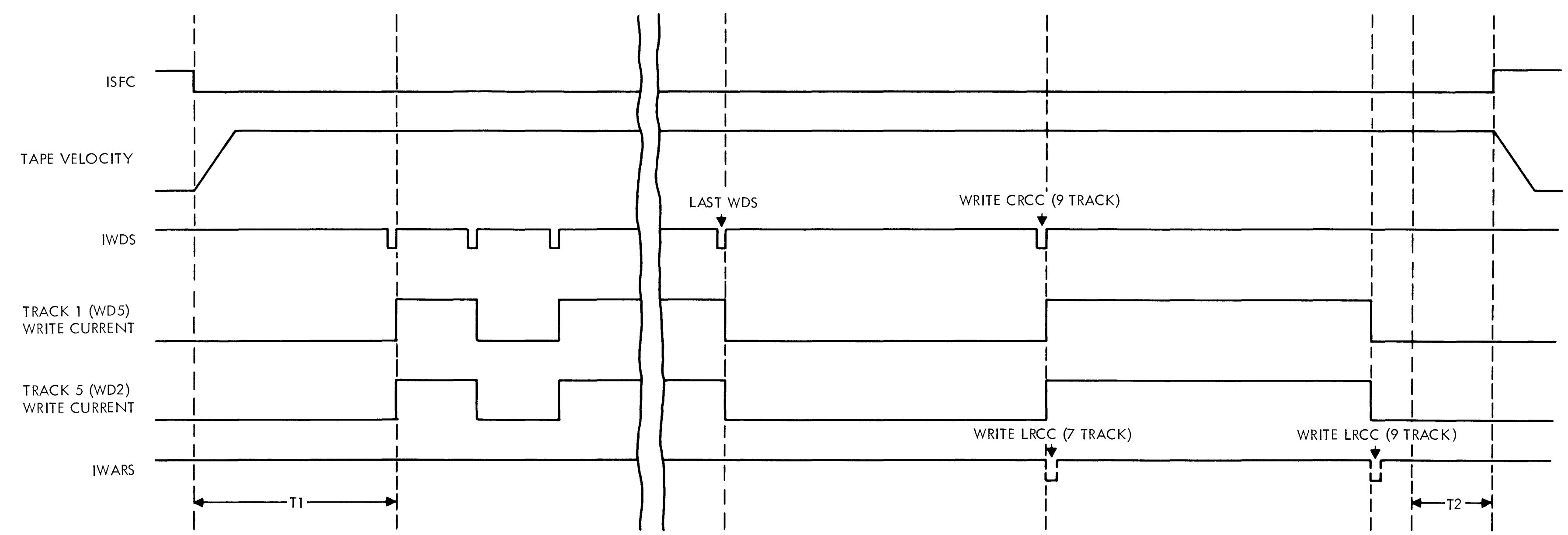


NOTES:

1. DIAGRAM IS FOR 9-TRACK OPERATION. FOR 7-TRACK OPERATION, THE WDS PULSE (LABELLED WRITE CRCC) AND THE WARS PULSE (LABELLED WRITE LRCC (9-TRACK)) ARE OMITTED AND THE DOTTED WARS PULSE (LABELLED WRITE LRCC (7-TRACK)) IS USED.

Figure 4-13. T6X40 Data Recording, Timing Diagram

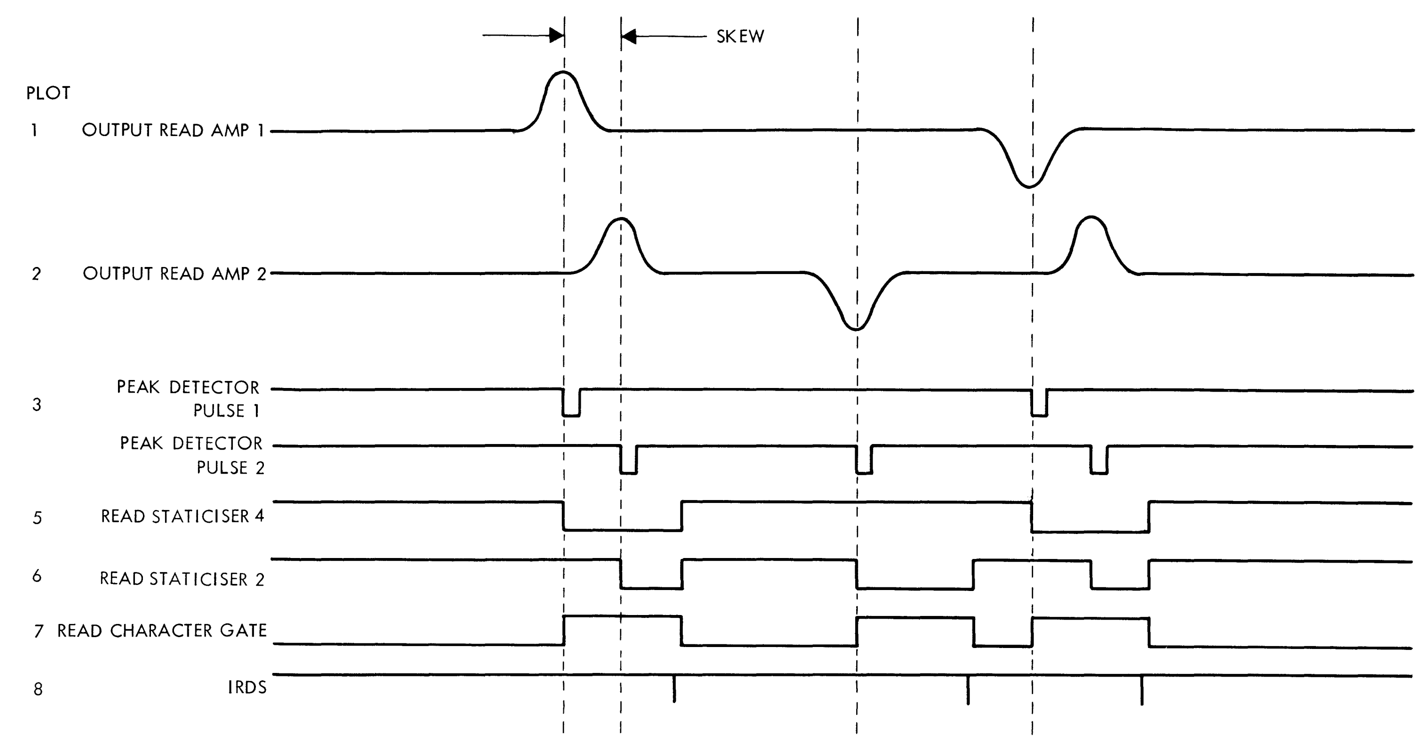
884S



NOTES:

1. DIAGRAM IS FOR 9-TRACK OPERATION. FOR 7-TRACK OPERATION, THE WDS PULSE (LABELLED WRITE CRCC) AND THE WARS PULSE (LABELLED WRITE LRCC (9-TRACK)) ARE OMITTED AND THE DOTTED WARS PULSE (LABELLED WRITE LRCC (7-TRACK)) IS USED.

Figure 4-18. T6X60 Data Recording, Timing Diagram



NOTES:

1. SKEW AS SHOWN IS THE TIME DISPLACEMENT BETWEEN THE READ SIGNALS FROM THE TWO TRACKS.

2. THE TOTAL TIME DISPLACEMENT WHILE READING IS THE SUM OF THE SKEW COMPONENT WHICH WAS PRODUCED WHEN THE TAPE WAS WRITTEN (ON THIS OR ANY OTHER TRANSPORT) AND THE SKEW COMPONENT PRODUCED DURING THIS READING PROCESS.

Figure 4-19. T6X40/T6X60 Data Reproduction, Timing Diagram

884S

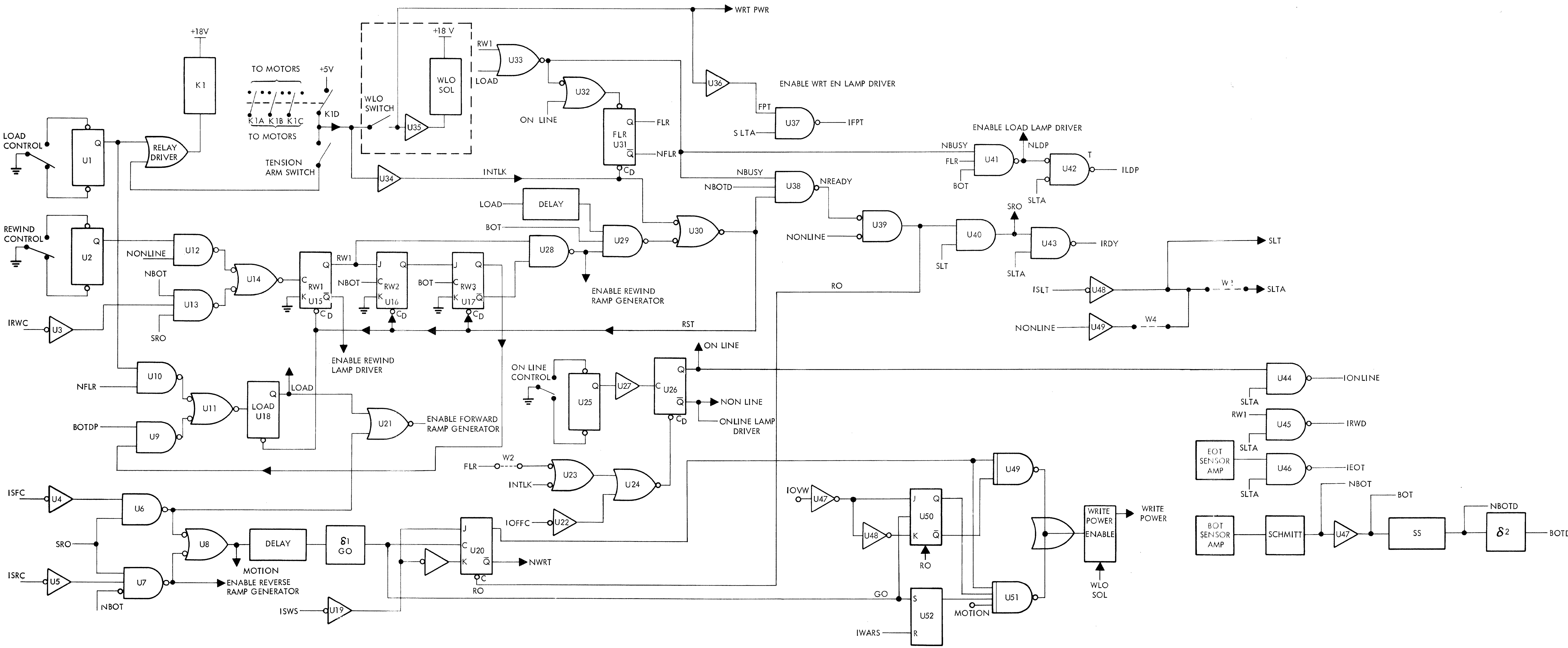


Figure 4-20. Tape Control System, Block Diagram

884S

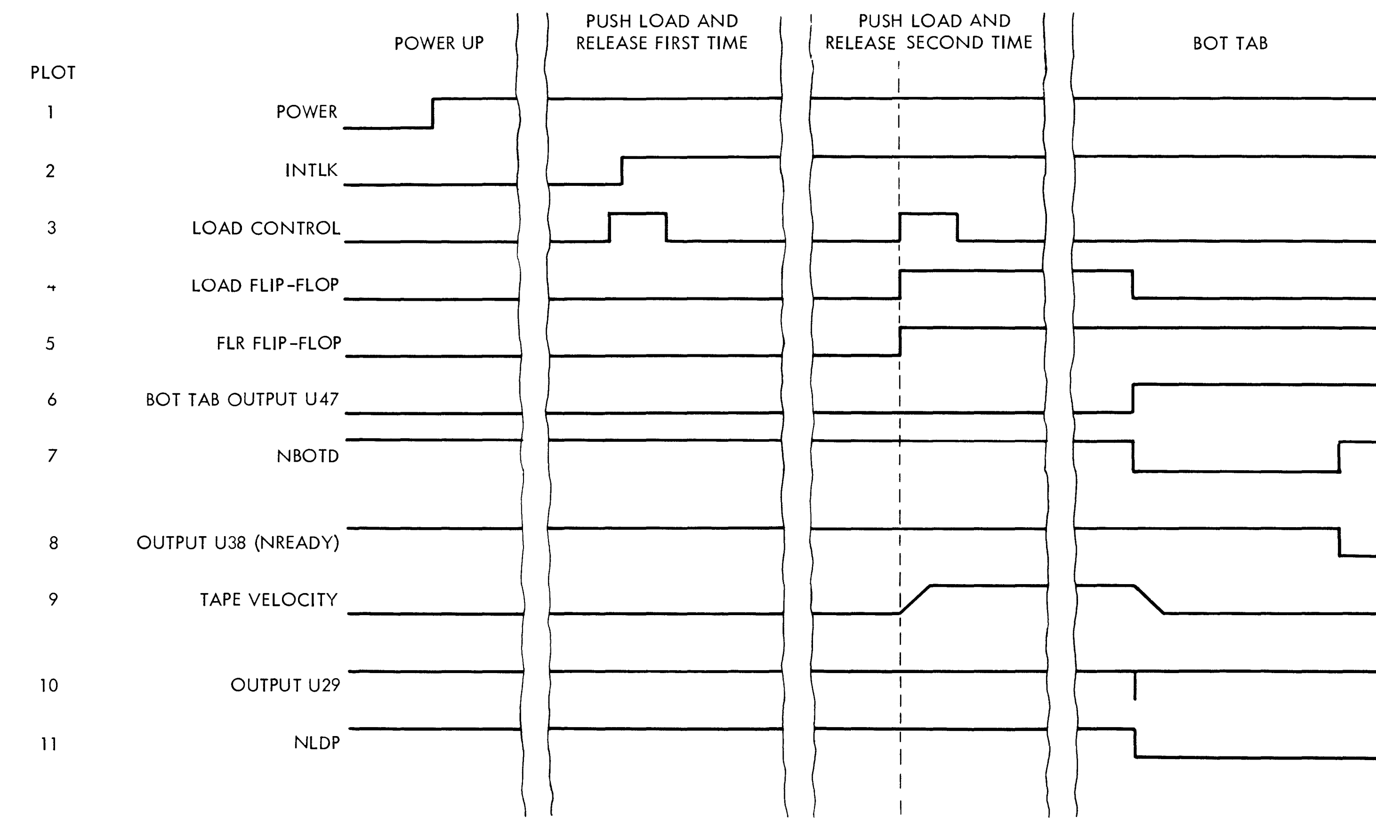


Figure 4-21. Bring to Load Point Sequence, Timing Diagram

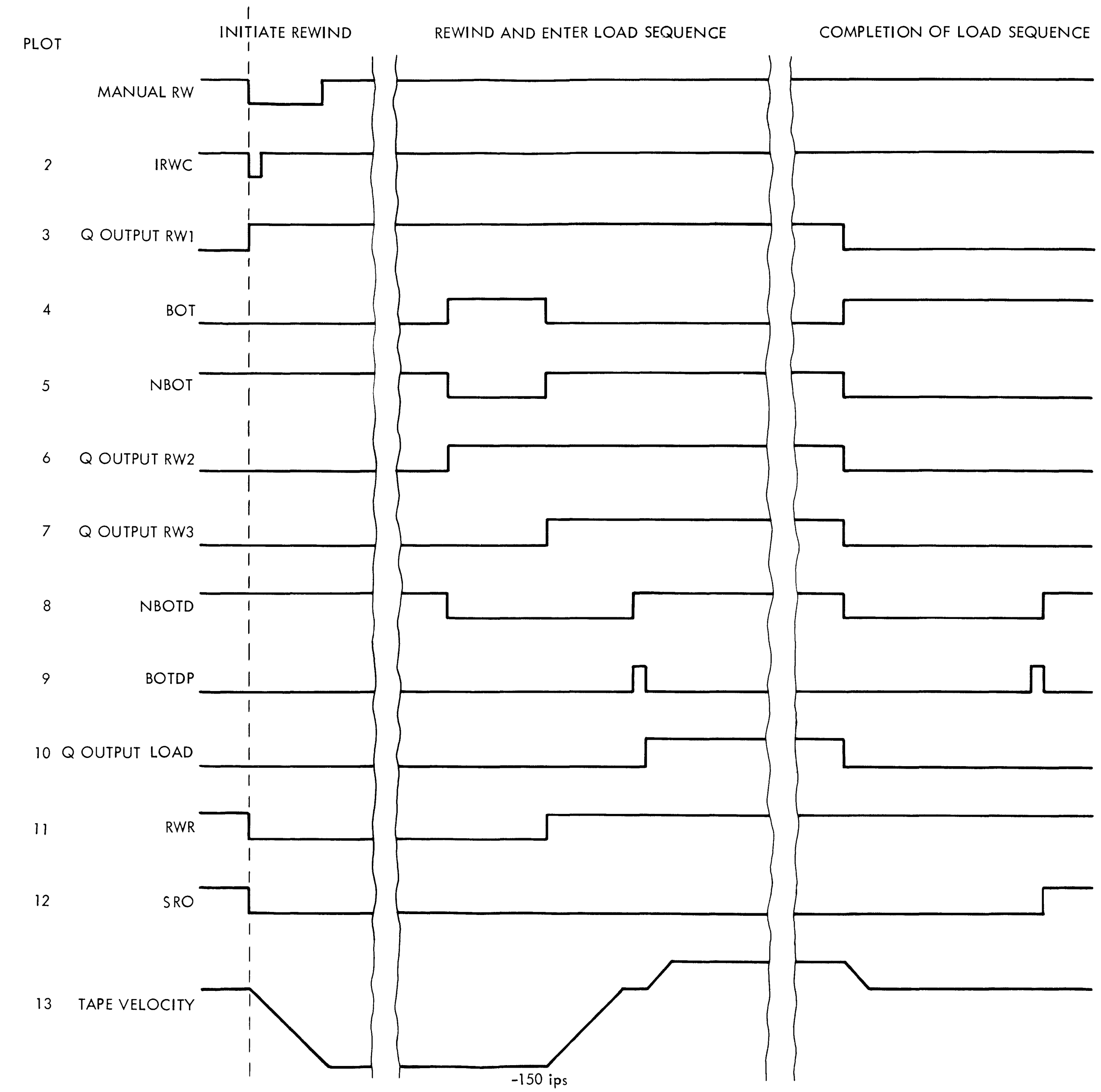


Figure 4-22. Rewind to Load Point Sequence, Timing Diagram

SECTION V
PRINTED CIRCUIT BOARDS THEORY OF OPERATION

5.1 INTRODUCTION

This section contains the theory of operation of the printed circuit boards used in the Model T6X40 and T6X60 Tape Transports. The schematic and assembly drawings for each board are contained at the end of Section VII.

A better understanding of the logic utilized in the tape transport can be gained when the operation of the J-K flip-flop is fully understood. The following paragraphs provide a brief summary of the operation of the 852 J-K flip-flop, which is the type most commonly used in the system.

This flip-flop operates on a *Master-Slave* principle. A logic diagram of the flip-flop is shown in Figure 5-1. The flip-flop is designed so that the threshold voltage of AND gates 101 and 102 is higher than that of AND gates 103 and 104. Since operation depends exclusively on voltage levels, any waveform of the proper voltage levels can trigger the J-K flip-flop.

Assume that the trigger voltage is initially low. As the trigger voltage goes high, AND gates 103 and 104 are disabled. Subsequently, AND gates 101 and 102 are enabled by the trigger pulse, the J and K inputs, and the information previously stored at the output of the *slave* unit.

The J and K input information at this time is transferred to the input of the *master* unit. As the trigger voltage goes low, AND gates 101 and 102 are disabled. AND gates 103 and 104 are then enabled and the information stored in the *master* unit is transferred to the output of the *slave* unit.

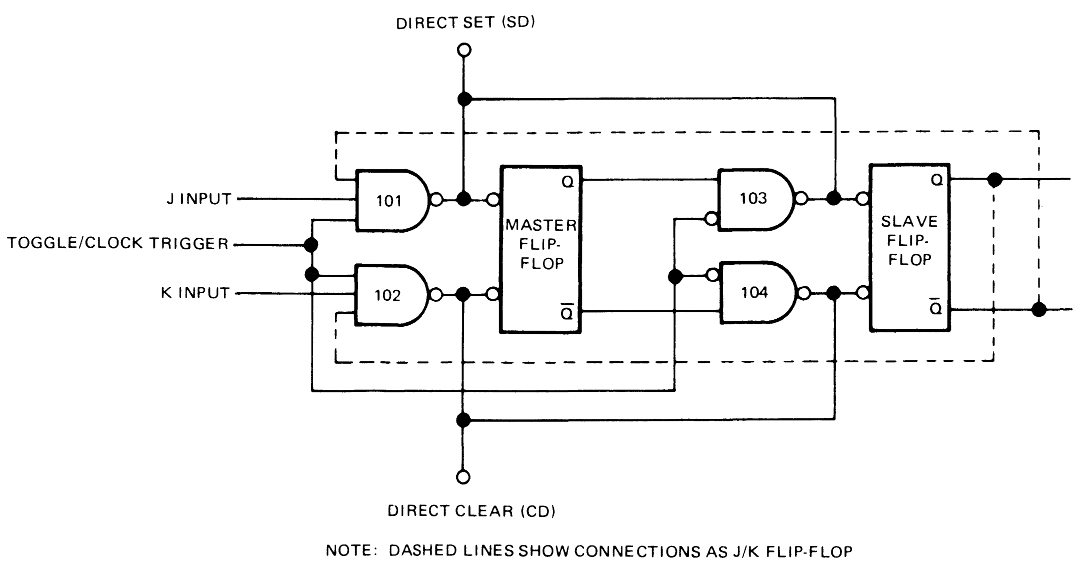


Figure 5-1. Simplified Logic Diagram, Master-Slave Flip-Flop

884S

5.2 THEORY OF OPERATION

Tables 7-7 and 7-8 list all interconnections between the various PCBAs installed in the T6X40 and T6X60 transports, respectively.

5.2.1 DATA E9 AND E7 PCBAS (T6X40 TRANSPORT)

The following is a description of the Data E9 PCBA which is installed in 9-track T6X40 transports designed to operate at 12.5, 25, and 37.5 ips (refer to Schematic 101010 and Assembly 101011).

The Data E9 is approximately 16.5 inches long with edge connectors at each end, along one edge. Figure 5-2 illustrates the placement of each connector and test point. J102 and J103 are the interface connectors and are slotted to mate with keys in the mating plugs. There are three additional connectors on the Data E9; J1 is used to connect power and control signals from the Tape Control PCBA; J2 and J3 are the connectors into which the write and read head cables plug.

5.2.1.1 Circuit Description

The board operation is described with reference to circuit 100, which is identical to circuits 200 through 900. All interface signals relevant to writing data (seven or nine WRITE DATA signals (IWD0, etc.), WRITE DATA STROBE (IWDS), and WRITE AMPLIFIER RESET (IWARS)) enter via J102 and are terminated by a resistor combination and an IC inverter.

Referring to circuit 100, the Write Data Parity (IWDP) data line is terminated by resistors R101,R102, and inverter U5-A. Inverters U5-A and U5-B perform a low-true AND function between IWDP and the WDS pulse received by U5-D, boosted by power gate U6-A, and bussed to all channels. Thus, a true signal on the IWDP line at WDS time results in a positive-going pulse being fed directly to the J input of the write waveform generator flip-flop U13-A and via inverter U5-C and OR gate U14-A to the K input of U13-A. Since the clock input level is high at this time, the *master* section of U13-A is toggled.

The WDS pulse also toggles clock control flip-flop U13-B which initiates the write deskewing operation. The Q output goes high, switching off clamp transistor Q2 for the clock oscillator Q3, Q4. This is an emitter-coupled multivibrator which generates 100-nsec negative pulses at the base of Q4 of a width determined by resistor R19 and capacitor C6; the frequency is determined by resistors R17 and R18 and capacitor C6.

The pulses are fed to two 5-bit shift registers (U17 and U16), which generate 10 negative-going edges which occur sequentially on 10 output pins. Outputs T1 through T9 are fed to the relevant write waveform generator flip-flops and cause the *slave* section of the flip-flop to toggle on the negative-going edge.

The tenth output (C) resets the control flip-flop U13-B via U14-B and U14-C. The $\overline{Q}$ output of U13-B goes high, clamping the shift register; also, the Q output goes low, clamping the oscillator.

The outputs of the write waveform generator flip-flops drive write amplifier transistors Q101 and Q102, whose emitters are taken to +5v when the WRT POWER line (J1-4) is high. The transistor connected to the low (approximately 0v) output of the flip-flop will conduct and a current will flow in the associated half of the head winding. When the WRT POWER line is low (approximately 0v), writing is inhibited because the write amplifier transistors cannot be turned on. Similarly, the erase current supplied by transistor Q1 is inhibited when the WRT POWER line is low. In operation, the write current is defined by resistors R105 and R106, while R107 is the associated damping resistor.

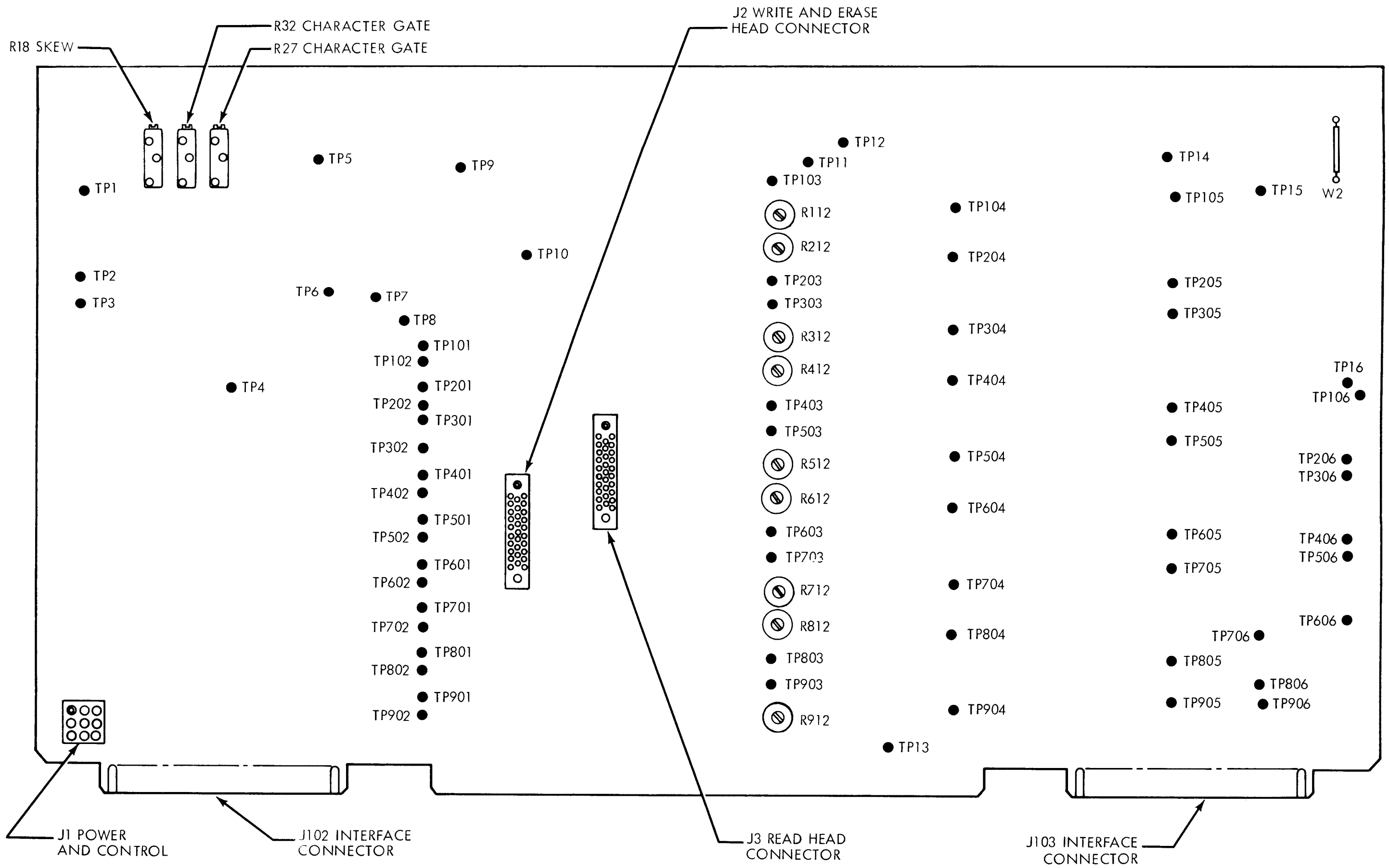


Figure 5-2. Data E9 PCBA, Test Point and Connector Placement

The write waveform generator flip-flops are primed for writing by the NWRT line (J1-9). This signal is inverted by power gate U15-B and bussed to the S_D inputs of the write waveform generator flip-flops. The signal is also connected via an R-C delay to OR gate U14-D and power gate U15-A. The output of U15-A is bussed to the C_D inputs of all the write waveform generator flip-flops. Thus, when the NWRT line is high, the ability to write is removed because both the Q and $\overline{Q}$ outputs of the write waveform generator flip-flops are at +5v. When the NWRT level is lowered to allow writing, the R-C network delays the removal of the C_D input with respect to the S_D input, leaving the flip-flops in the reset state.

The head windings are so phased that the reset flip-flops cause current to flow in the standard *erase* direction. Lowering of the NWRT level also turns on the erase current driver (Q1). The MOTION level received at J1-6 prevents write current from flowing unless tape is in motion.

The IWARS pulse received by inverter U5-E is used to reset all the write waveform generator flip-flops as required to write LRCC at the end of the record. The pulse is fed to the K inputs of all write waveform generator flip-flops via inverter OR gates U14-A, U11-D, etc., resetting the *master* section of all flip-flops.

The leading edge of the IWARS pulse is differentiated by capacitor C4 and resistors R12 and R13 and sets clock control flip-flop U13-B. This initiates a Write Deskewing sequence resulting in toggling of the write waveform generator flip-flops and the writing of the LRC character in a deskewed manner.

During reading, signals from the read head at a level of 10 to 20 mv are fed via connector J3 to the read amplifier which is one-half of a dual operational amplifier IC (U22-B for 9-track, and U19-B for 7-track). The amplifier output is maintained close of 0v in the absence of an input signal by the feedback path of resistors R110 and R113, which determine a fairly low dc gain. The low frequency cutoff is determined by capacitors C101 and C102. The operating gain of the amplifier is defined by resistor network R111, R114, and R112. R112 is a variable resistor used in the initial setup to set the output peak-to-peak amplitude.

The read amplifier output is fed to a unity gain inverting amplifier, using transistors Q103, Q104, and Q105. The positive-going halves of the two phases of the read signal are added by means of diodes CR101, CR102, and transistors Q106 and Q107. The exact voltage at which CR101 and CR102 conduct is controlled by the level at TP13, to which R120 is connected. This level is controlled by the level at TP13, to which R120 is connected. This level is controlled by the NWRT line. When NWRT is low, indicating a write operation, a voltage close to +2v is obtained at TP13 which results in a clip level of close to 50 percent of the read amplitude. When NWRT is high, indicating a read operation, a voltage close to 0v is obtained at TP13, which results in a clip level of close to 20 percent of the read amplitude.

The double emitter-follower stage Q106, Q107 is used to drive the input of the peak detector.

The peak detector is essentially a feedback differentiator circuit which uses one-half of a dual operational amplifier (U27-B for 9-track, U23-B for 7-track). The amplifier is prevented from saturating by feedback diodes CR103, CR104, CR105, and CR106. The amplifier is biased to a negative output in the absence of an input signal by resistor R123. At this point, a positive-going transition from —1v to +1v corresponds to a peak of the read waveform. The output of the peak detector operational amplifier is passed to Q108, which converts the signal to standard logic levels. At this point, a negative-going edge corresponds to the peak of the read waveform. Resistor R128 and the corresponding resistors of the other 8 circuits are connected to TP15. Examination of the output at TP15 with an oscilloscope while reading an *all ones* tape allows a good estimate to be made of the condition of the tape path. Skew is indicated by a progression of steps on the negative-going edge and the magnitude of skew by the ratio of fall time to the character time (see Paragraph 6.7.5).

The output of Q108 is differentiated by capacitor C110 and resistor R129 and fed to the clock input of Read Staticiser flip-flop U37-A, setting it.

The $\overline{Q}$ output of U37-A, together with those of the other eight Read Staticiser flip-flops are ORed by gate U40-B. The first flip-flop to be set causes a positive-going transition at TP11, which switches off clamp transistor Q8. This initiates rundown circuit Q7, Q8, Q9, and Q10. The voltage at the cathode of CR2 decays toward —5v from +4.5v with a time constant (R31 + R32) C10.

At approximately 0v, Q9 starts to cut off. This action is regenerative due to the positive feedback via capacitor C11 and resistors R36, resulting in a negative-going transition at the collector of Q10 (TP9). This transition is differentiated and subsequently shaped in single-shot U39, U40, and associated components to form a 2-μsec READ DATA STROBE (IRDS) pulse which is fed to the interface via power gate U38-B.

In addition, the negative transition is delayed via U39-F, resistor R41, capacitor C14, and inverter U39-A, and fed via OR gate U38-A and power gate U36-B to the reset inputs of the Read Staticiser flip-flops. This causes the output of U40-B to go negative, turning on Q8, therefore re-applying the clamp to the rundown circuit.

The delay is such that the data lines reset a minimum of 0.5 μsec after the trailing edge of the IRDS.

The Read Staticisers are reset whenever the MOTION signal (J1-6) is false, i.e., tape is not in motion.

The 7-channel version of the Data PCBA (Data E7) has a different configuration. Circuits 200 and 300 are omitted from both the write and read sections of the board and the deskewing connections from the shift register to the write waveform generator flip-flops are different to accommodate the different track layout format (see Figures 4-8 and 4-9). Figure 5-3 shows the placement of each connector and test point.

5.2.2 DATA E19 AND E17 PCBAS (T6X40 TRANSPORT)

The following is a description of the Data E19 PCBA which is installed in 9-track T6X40 transports (refer to Schematic 101710 and Assembly 101711).

The Data E19 is approximately 16.5 inches long with edge connectors at each end, along one edge. Figure 5-4 illustrates the placement of each connector and test point. J102 and J103 are the interface connectors and are slotted to mate with keys in the mating plugs. There are three additional connectors on the Data E19; J8 is used to connect power and control signals from the Tape Control PCBA; J1 and J2 are the connectors into which the write and read head cables plug.

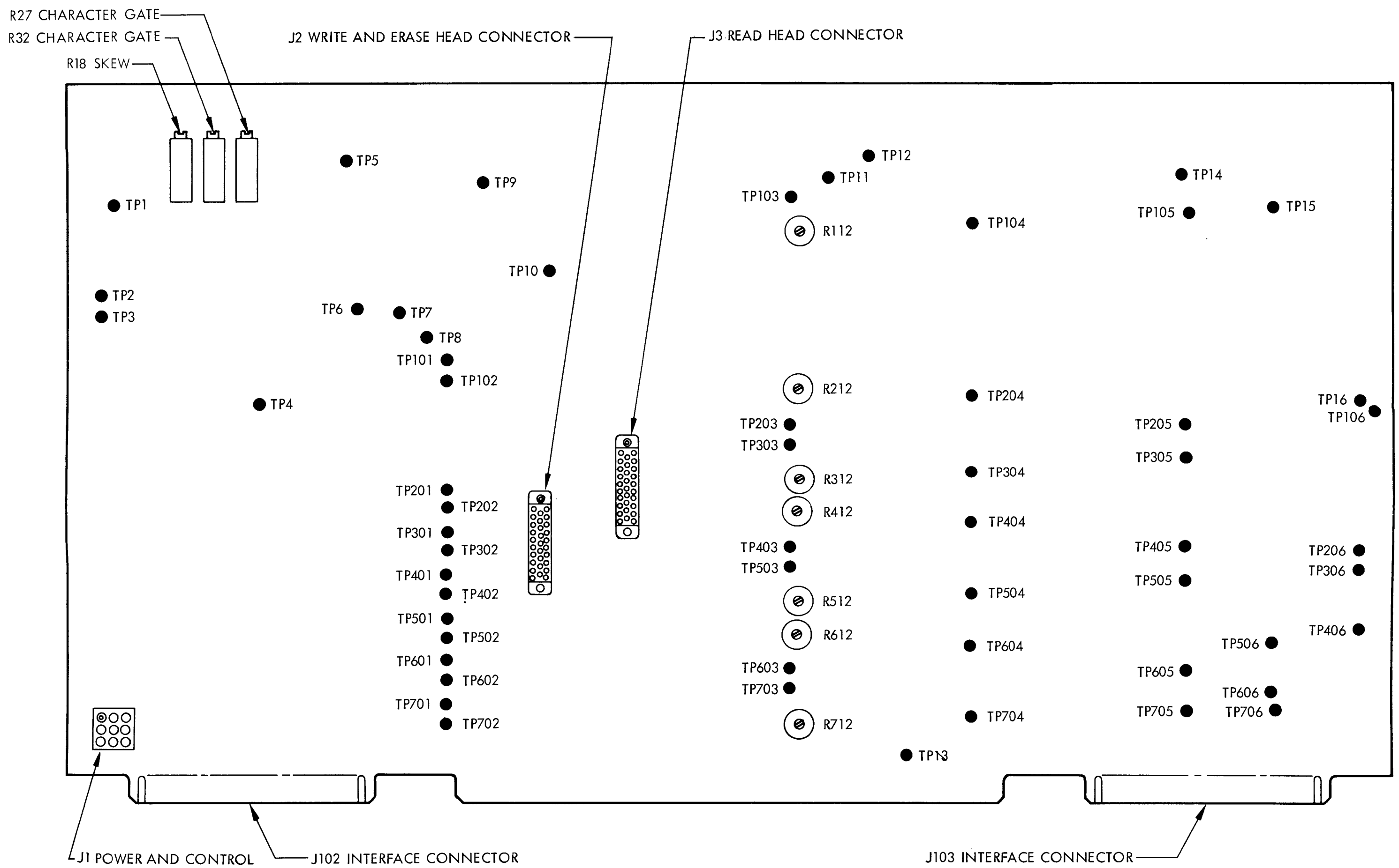


Figure 5-3. Data E7 PCBA, Test Point and Connector Placement

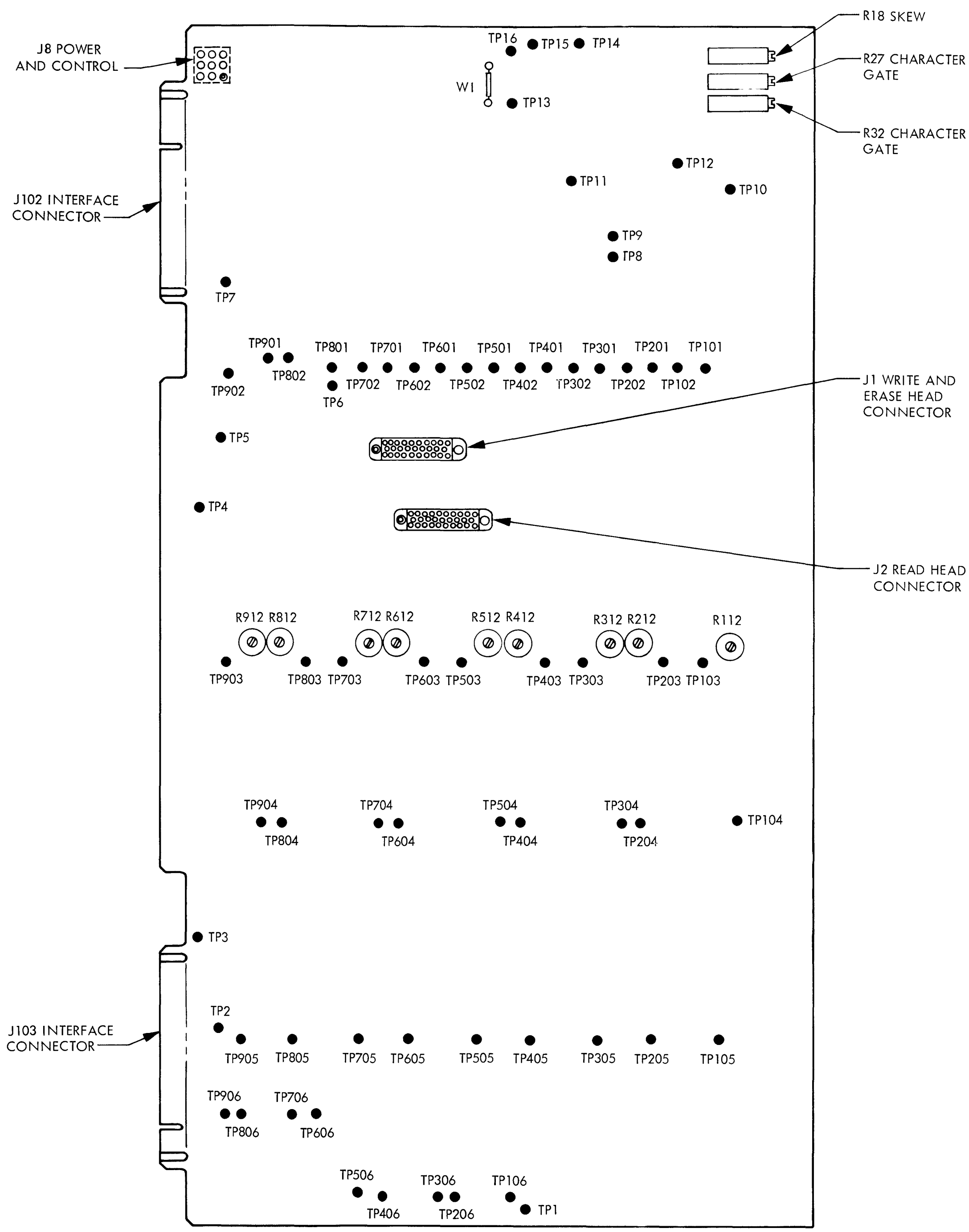


Figure 5-4. Data E19 PCBA, Test Point and Connector Placement

5.2.2.1 Circuit Description

The board operation is described with reference to circuit 100, which is identical to circuits 200 through 900. All interface signals relevant to writing data (seven or nine WRITE DATA signals (IWD0, etc.), WRITE DATA STROBE (IWDS), and WRITE AMPLIFIER RESET (IWARS)) enter via J102 and are terminated by a resistor combination and an IC inverter.

Referring to circuit 100, the WRITE DATA PARITY (IWDP) line is terminated by resistors R101, R102, and inverter U36-A. Inverters U36-A and U36-B perform a low-true AND function between IWDP and the IWDS pulse received by U36-D, boosted by power gate U35-A, and bussed to all channels. Thus, a true signal on the IWDP line at WDS time results in a positive-going pulse being fed directly to the J input of the write waveform generator flip-flop U28-A and via inverter U36-C and OR gate U27-A to the K input of U28-A. Since the clock input level is high at this time, the *master* section of U28-A is toggled.

The IWDS pulse also toggles clock control flip-flop U28-B which initiates the Write Deskewing operation. The Q output goes high, switching off clamp transistor Q2 for the clock oscillator Q3, Q4. This is an emitter-coupled multivibrator which generates 100-nsec negative pulses at the base of Q4 of a width determined by resistor R19 and capacitor C6; the frequency is determined by resistors R17 and R18 and capacitor C6.

The pulses are fed to two 5-bit shift registers (U24 and U25), which generate ten negative-going edges which occur sequentially on ten output pins. Outputs T1 through T9 are fed to the relevant write waveform generator flip-flops and cause the *slave* section of the flip-flop to toggle on the negative-going edge.

The tenth output (C) resets the control flip-flop U28-B via U27-B and U27-C. The $\overline{Q}$ output of U28-B goes high, clamping the shift register. Also, the Q output goes low, clamping the oscillator.

The outputs of the write waveform generator flip-flops drive write amplifier transistors Q101 and Q102, whose emitters are taken to approximately +5v when the WRT PWR line (J8-4) is high. The transistor connected to the low (approximately 0v) output of the flip-flop will conduct and a current will flow in the associated half of the head winding whose center tap is connected to approximately —5v through Q12, and this is, in turn, driven into saturation by Q11 when the WRT PWR line (J8-4) is high and the NWRT line (J8-9) is low. When the WRT PWR line is low (approximately 0v) or the NWRT line is high, writing is inhibited because the write amplifier transistors cannot be turned on, and Q11 cannot drive Q12 into saturation. Similarly, the erase current supplied by transistor Q1 is inhibited when the WRT PWR line is low, or the NWRT line is high. In operation, the write current is defined by resistors R105 and R106, while R107 is the associated damping resistor.

The write waveform generator flip-flops are primed for writing by the NWRT line (J8-9). This signal is inverted by power gate U26-B and bussed to the S_D inputs of the write waveform generator flip-flops. The signal is also connected via an R-C delay to OR gate U27-D and power gate U26-A. The output of U26-A is bussed to the C_D inputs of all the write waveform generator flip-flops. Thus, when the NWRT line is high, the ability to write is removed because both the Q and $\overline{Q}$ outputs of the write waveform generator flip-flops are at +5v. When the NWRT level is lowered to allow writing, the R-C network delays the removal of the C_D input with respect to the S_D input, leaving the flip-flops in the reset state.

The head windings are so phased that the reset flip-flops cause current to flow in the standard *erase* direction. The MOTION level received at J8-6 prevents write current from flowing unless tape is in motion.

The IWARS pulse received by inverter U36-E is used to reset all the write waveform generator flip-flops as required to write the LRC character at the end of the record. The pulse is fed to the K inputs of all write waveform generator flip-flops via inverter OR gates U27-A, U30-D, etc., resetting the *master* section of all flip-flops.

The leading edge of the IWARS pulse is differentiated by capacitor C4 and resistors R12 and R13 and sets clock control flip-flop U28-B. This initiates a Write Deskewing sequence resulting in toggling of the write waveform generator flip-flops and the writing of the LRC character in a deskewed manner.

During reading, signals from the read head at a nominal level of 48 millivolts are fed via connector J2 to the read amplifier, which is one-half of a dual operational amplifier IC (U19-B). The amplifier output is maintained close to 0v in the absence of an input signal by the feedback path of resistors R110 and R113, which determine a fairly low dc gain. The low frequency cutoff is determined by capacitors C101 and C102. The operating gain of the amplifier is defined by resistor network R111, R114, and R112. R112 is a variable resistor used in the initial setup to set the output peak-to-peak amplitude.

The read amplifier output is fed to a unity gain inverting amplifier, using transistors Q103, Q104, and Q105. The positive-going halves of the two phases of the read signal are added by means of diodes CR101, CR102, and transistors Q106 and Q107. The exact voltage at which CR101 and CR102 conduct is controlled by the level at TP12 (threshold level) to which R120 is connected. This level is controlled by the NWRT line. When NWRT is low, indicating a write operation, a voltage close to +2v is obtained at TP12 which results in a clip level of close to 45 percent of the read amplitude.

When NWRT is high indicating a read operation, a voltage close to 0v is obtained at TP12, which results in a clip level of close to 20 percent of the read amplitude.

The double emitter-follower stage Q106, Q107 is used to drive the input of the peak detector.

The peak detector is essentially a feedback differentiator circuit which uses one-half of a dual operational amplifier (U14-B). The amplifier is prevented from saturating by feedback diodes CR103, CR104, CR105, and CR106. The amplifier is biased to a negative output in the absence of an input signal by resistor R123. At this point, a positive-going transition from —1v to +1v corresponds to a peak of the read waveform. The output of the peak detector operational amplifier is passed to Q108, which converts the signal to standard logic levels. At this point, a negative-going edge corresponds to the peak of the read waveform. Resistor R128 and the corresponding resistors of the other eight circuits are connected to TP2. Examination of the output at TP2 with an oscilloscope while reading an *all ones* tape allows a good estimate to be made of the condition of the tape path. Skew is indicated by a progression of steps on the negative-going edge and the magnitude of skew by the ratio of fall time to the character time (see Paragraph 6.7.5).

The output of Q108 is differentiated by capacitor C110 and resistor R129 and fed to the clock input of Read Staticiser flip-flop U4-A, setting it.

The $\overline{Q}$ output of U4-A, together with those of the other eight Read Staticiser flip-flops are ORed by gate U2-B. The first flip-flop to be set causes a positive-going transition at TP9, which switches off clamp transistor Q8. This initiates run-down circuit Q7, Q8, Q9, and Q10. The voltage at the cathode of CR2 decays toward —5v from +4.5v with a time constant (R31 + R32) C10.

At approximately 0v, Q9 starts to cut off. This action is regenerative due to the positive feedback via capacitor C11 and resistor R36, resulting in a negative-going transition at the collector of Q10 (TP10). This transition is differentiated, and subsequently shaped in single-shot U1-B, U2-A, U40, and associated components, to form a 1 μsec READ DATA STROBE (IRDS) pulse which is fed to the interface via power gate U3-B.

In addition, the negative transition is delayed via U1-D, U1-F, resistor R41, capacitor C14, and inverter U1-A, and fed via OR gate U3-A and power gate U5-B to the reset inputs of the Read Staticiser flip-flops. This causes the output of U2-B to go negative, turning on Q8, therefore, re-applying the clamp to the run-down circuit.

The delay is such that the data lines reset a minimum of 0.5 μsec after the trailing edge of the IRDS.

The Read Staticisers are reset whenever the MOTION signal (J8-6) is low; i.e., tape is not in motion.

Data E17 is the 7-channel version (refer to Schematic 101715 and Assembly 101716). It is essentially the same as the Data E19 except for configuration; circuits 200 and 300 are omitted from both the write and read sections of the board and the deskewing connections from the shift register to the write waveform generator flip-flops are different to accommodate the different track layout format (see Figures 4-8 and 4-9). Figure 5-5 shows the placement of test points and connectors.

5.2.3 DATA D PCBA (T6X60 TRANSPORT)

The following is a description of the Data D Printed Circuit Board Assembly which may be installed in 6X60 transports designed to operate at 12.5, 25, and 37.5 ips. Refer to Schematic 101031 and Assembly 101032.

The Data D PCBA is approximately 16.5 inches long with edge connectors at each end along one edge. Figure 5-6 illustrates the placement of each connector and test point. J102 and J103 are the interface connectors and are slotted to mate with keys in the mating plugs. There are two additional connectors on the Data D. J1 is used to connect power and control signals from the Tape Control circuit board. The read/write head cable plugs into connector J2.

5.2.3.1 Circuit Description

The circuit board operation is described with reference to circuit 100, which is identical to circuits 200 through 900. All interface signals relevant to writing data (seven or nine WRITE DATA signals (IWD0, etc.), WRITE DATA STROBE (IWDS), and WRITE AMPLIFIER RESET (IWARS)) enter via J102 and are terminated by a resistor combination and an IC inverter.

Referring to circuit 100, the WRITE DATA PARITY (IWDP) data line is terminated by resistors R101, R102, and inverter U2-C (zone H18). The inverter output is connected to the J and K inputs of the write flip-flop U9-A so that a true interface signal results in the toggling of the flip-flop when the IWDS pulse is received by U3-A, which is bussed to all the clock inputs.

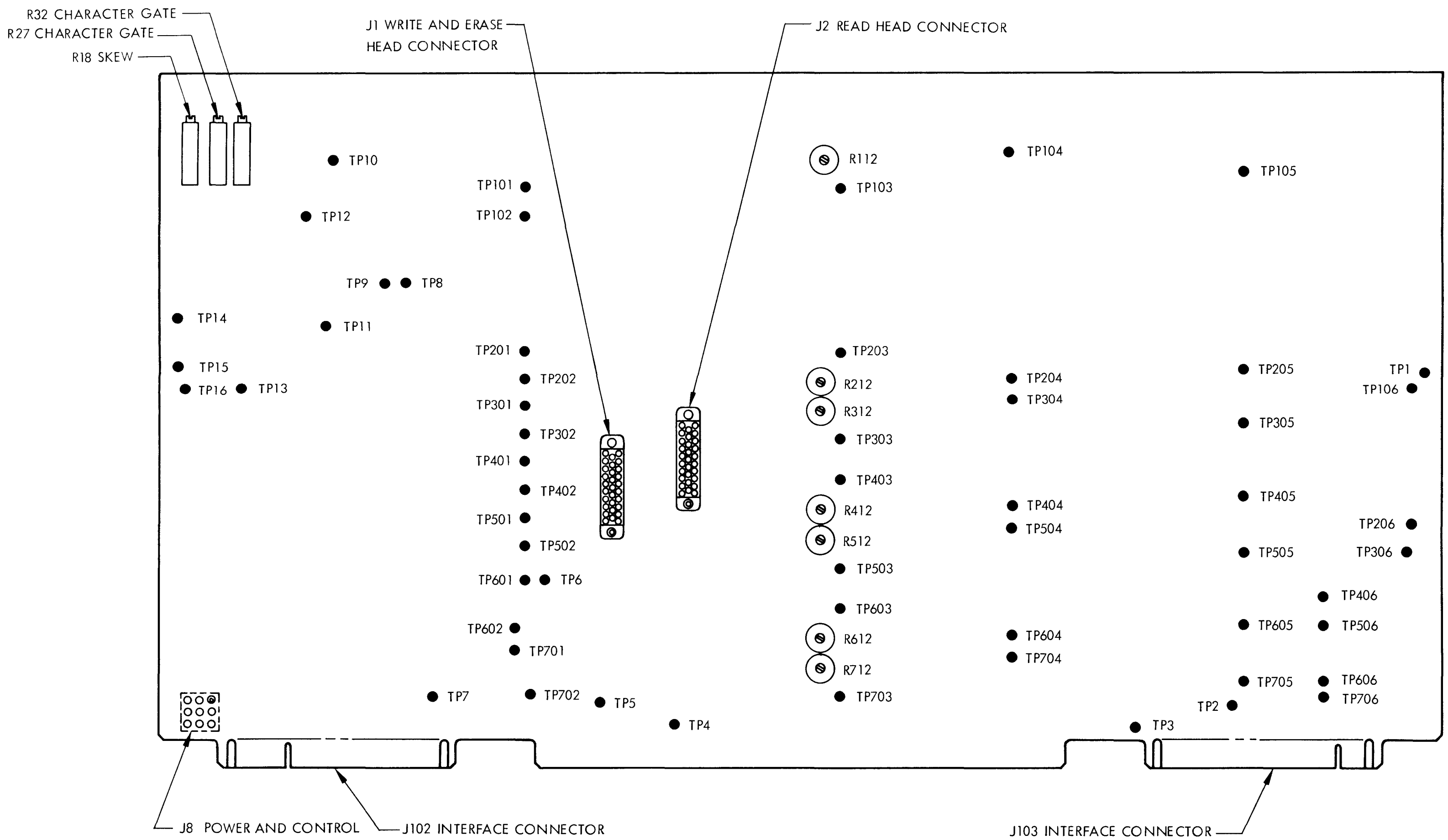


Figure 5-5. Data E17 PCBA, Test Point and Connector Placement

884S

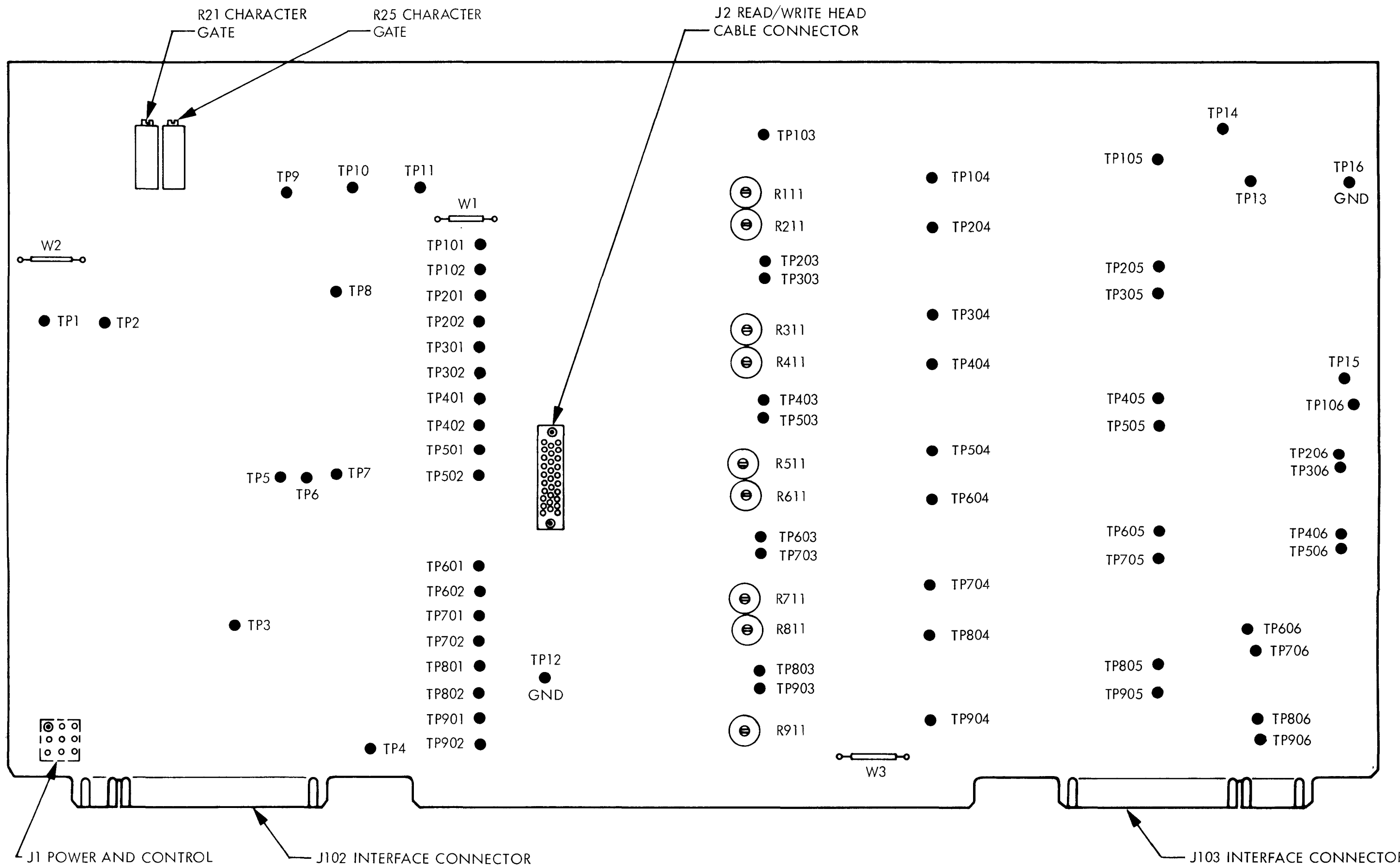


Figure 5-6. Data D PCBA, Test Point and Connector Placement

884S

The output of the write flip-flop drives the write amplifier transistors Q101 and Q102, whose emitters are taken to +5v when the WRT POWER level (J1-4) is high. This allows current to flow in the transistor whose flip-flop is low. When the WRT POWER level is low (close to 0v), writing is inhibited because the write amplifier transistors cannot be turned on. In the same way, the erase current supplied by Q1 is inhibited when WRT POWER is low.

The write flip-flops are primed for writing by the NWRT line (J1-9). This signal is inverted by power gate U4-B and bussed to all set inputs of the write flip-flops. This signal is also connected through an R-C delay to a pair of inverting stages (U4-A and U4-B) and bussed to all reset inputs of the write flip-flops. Thus, when the NWRT level is high, the ability to write is removed because both true and false outputs of the flip-flops are raised to +5v. When the NWRT level is lowered to allow writing, the R-C network delays the removal of the reset input with respect to the set input, leaving the flip-flops in the reset state.

The head windings are so phased that the reset flip-flops cause current to flow in the standard *erase* direction. Lowering of the NWRT level also turns on the erase current driver (Q1).

The MOTION level received at J1-6 prevents write current from flowing unless the tape is in motion.

The IWARS signal is used to write the LRC character at the end of a record. The leading edge of the IWARS pulse resets all the write flip-flops causing the head currents to be switched in those tracks where a 1 is required in the LRC character. The write current is defined by R105 and R106 and the damping resistor across the head which is the sum of R107 and R108.

During reading, transistors Q101 and Q102 are held nonconducting and, for practical purposes, the effect of the write circuits is removed; therefore the head windings are left loaded by the read amplifier input resistors R107 and R108. The signals, at this point during read, are so low that CR101 and CR102 do not conduct.

The read amplifier is one-half of a dual operational amplifier (U15-B). The amplifier output is maintained close to 0v by the feedback path of R109 and R112, which produces a fairly low dc gain. The low frequency cutoff is determined by capacitors C103 and C104. Diodes CR103 and CR104 shunting capacitors C103 and C104 are used to prevent large voltages from building up during a write operation that might prevent recovery of the amplifier during the available time prior to a subsequent read operation.

The operating gain of the amplifier is defined by the resistor network R110, R111, and R113. R111 is a variable resistor used in the initial setup to set the output peak-to-peak amplitude to 12v.

The read amplifier output is fed to a unity gain inverting amplifier, using transistors Q103, Q104, and Q105. The positive-going halves of the two phases of the read signal are added by means of diodes CR105 and CR106, and transistors Q106 and Q107. The exact voltage at which CR105 and CR106 conduct is controlled by the level at TP9, to which R119 is connected. This level is controlled by the IRTH interface line of J102. When IRTH is high (false), a voltage close to 0v is obtained at TP9, which results in a clip level of close to 20 percent of the read amplitude. When IRTH is low (true) a voltage close to +2v is obtained at TP9, which results in a clip level of close to 50 percent of the read amplitude.

The double emitter-follower stage Q106, Q107 is used to drive the input of the peak detector.

The peak detector is essentially a feedback differentiator circuit which uses one-half of a dual operational amplifier (U20-B). The amplifier is prevented from saturating by feedback diodes CR107, CR108, CR109, and CR110. The amplifier is biased to a negative output in the absence of an input signal by resistor R122. At this point, a positive-going transition from —1v to +1v corresponds to a peak of the read waveform. The output of the peak detector operational amplifier is passed to Q108, which converts the signal to standard logic levels. At this point, a negative-going edge corresponds to the peak of the read waveform. Resistor R127 and the corresponding resistors of the other eight circuits are connected to TP13. Examination of the output at TP13 with an oscilloscope while reading an *all ones* tape allows a good estimate to be made of the condition of the tape path. Skew is indicated by a progression of steps on the negative-going edge and the magnitude of skew by the ratio of fall time to the character time (see Paragraph 6.7.5).

The output of Q108 is differentiated by capacitor C110 and resistor R128 and fed to the clock input of Read Staticiser flip-flop U30-A, setting it.

The $\overline{Q}$ output of U30-A together with those of the other eight Read Staticiser flip-flops are ORed by gate U31-B (zone B10). The first flip-flop to be set causes a positive-going transition at TP10, which switches off clamp transistor Q5. This initiates run-down circuit Q4, Q5, Q6, and Q7.

With the transport operating in the Low Density mode, transistor Q4 is switched on by the NHID signal at J1-5. The conduction of Q4 places +5v at the cathode of CR1. This effectively reverse-biases CR1, removing R-20 and R-21 from the run-down circuit.

Switching off clamp transistor Q5 removes the +4.5v from the junction of R23 and R24. This allows the positive voltage on the cathode of CR2 to decay toward —5v with a time constant (R24 + R25) C4.

At approximately 0v, Q6 starts to cut off and this action is regenerative due to the positive feedback via capacitor C5 and resistor R29, resulting in a negative-going transition at the collector of Q7 (TP8). This transition is differentiated to form a 2-µsecond READ DATA STROBE pulse which is fed to the interface via power gate U31-A.

In addition, the negative transition is delayed via U10-E, resistor R34, capacitor C8, and inverter U10-C and fed via OR gate U32-B and power gate U32-A to the reset inputs of the Read Staticiser flip-flops. This causes the output of U31-B to go negative, turning on Q5, therefore, re-applying the clamp to the run-down circuit.

The delay is such that the data lines reset a minimum of 0.5 second after the trailing edge of the READ DATA STROBE.

The Read Staticisers are reset whenever the MOTION signal (J1-6) is false; i.e., tape is not in motion.

When the transport is operated in the High Density mode, transistor Q4 is cut off by the positive-going NHID signal at J1-5. Switching off Q4 removes the +5v at the cathode of CR1. This effectively places R20 and R21 in parallel with R24 and R25.

Switching off clamp transistor Q5 allows the positive voltage at the cathode of CR2 to decay toward —5v with a time constant determined by C4 and the parallel combination of R20, R21, and R24, R25.

Circuit action continues in the manner previously described under the Low Density mode of operation.

The 7-track version of the Data D is obtained by omitting circuits 200 and 300 from both the write and read sections of the circuit board. Jumper W-2 is employed in the 9-track transport to hold Q4 cut off, thus allowing only one packing density (800 cpi).

5.2.4 DATA D1 PCBA (T6X60 TRANSPORT)

The following is a description of the Data D1 PCBA which may be installed in T6X60 transports. Refer to Schematic 101720 and Assembly 101721.

The Data D1 PCBA is approximately 16.5 inches long with edge connectors at each end along one edge. Figure 5-7 illustrates the placement of each connector and test point. J102 and J103 are the interface connectors and are slotted to mate with keys in the mating plugs. There are two additional connectors on the Data D1. J8 is used to connect power and control signals from the Tape Control circuit board. The read/write head cable plugs into connector J1.

5.2.4.1 Circuit Description

The circuit board operation is described with reference to circuit 100, which is identical to circuits 200 through 900. All interface signals relevant to writing data (seven or nine WRITE DATA signals (IWD0,etc.), WRITE DATA STROBE (IWDS), and WRITE AMPLIFIER RESET (IWARS)) enter via J102 and are terminated by a resistor combination and an IC inverter.

Referring to circuit 100, the WRITE DATA PARITY (IWDP) data line is terminated by resistors R101, R102, and inverter U32-C. The inverter output is connected to the J and K inputs of the write flip-flop U24-A so that a true interface signal results in the toggling of the flip-flop when the WDS pulse is received by U31-A, which is bussed to all the clock inputs.

The output of the write flip-flop drives the write amplifier transistors Q101 and Q102, whose emitters are taken to +5v when the WRT POWER level (J8-4) is high. This allows current to flow in the transistor whose flip-flop output is low. When the WRT POWER level is low (close to 0v), writing is inhibited because the write amplifier transistors cannot be turned on. In the same way, the erase current supplied by Q1 is inhibited when WRT POWER is low.

The write flip-flops are primed for writing by the NWRT line (J8-9). This signal is inverted by power gate U30-B and bussed to all set inputs of the write flip-flops. This signal is also connected through a R-C delay to a pair of inverting stages (U30-A and U31-B) and bussed to all reset inputs of the write flip-flops. Thus, when the NWRT level is high, the ability to write is removed because both true and false outputs of the flip-flops are raised to +5v. When the NWRT level is lowered to allow writing, the R-C network delays the removal of the reset input with respect to the set input, leaving the flip-flops in the reset state.

The head windings are so phased that the reset flip-flops cause current to flow in the standard *erase* direction. Raising the WRT POWER also turns on the erase driver (Q1). Q2 conducts whenever NWRT is low and WRT POWER is high, causing Q3 to conduct. Thus, transistor Q3 acts as a switch to provide —5v to the center-taps of all head windings.

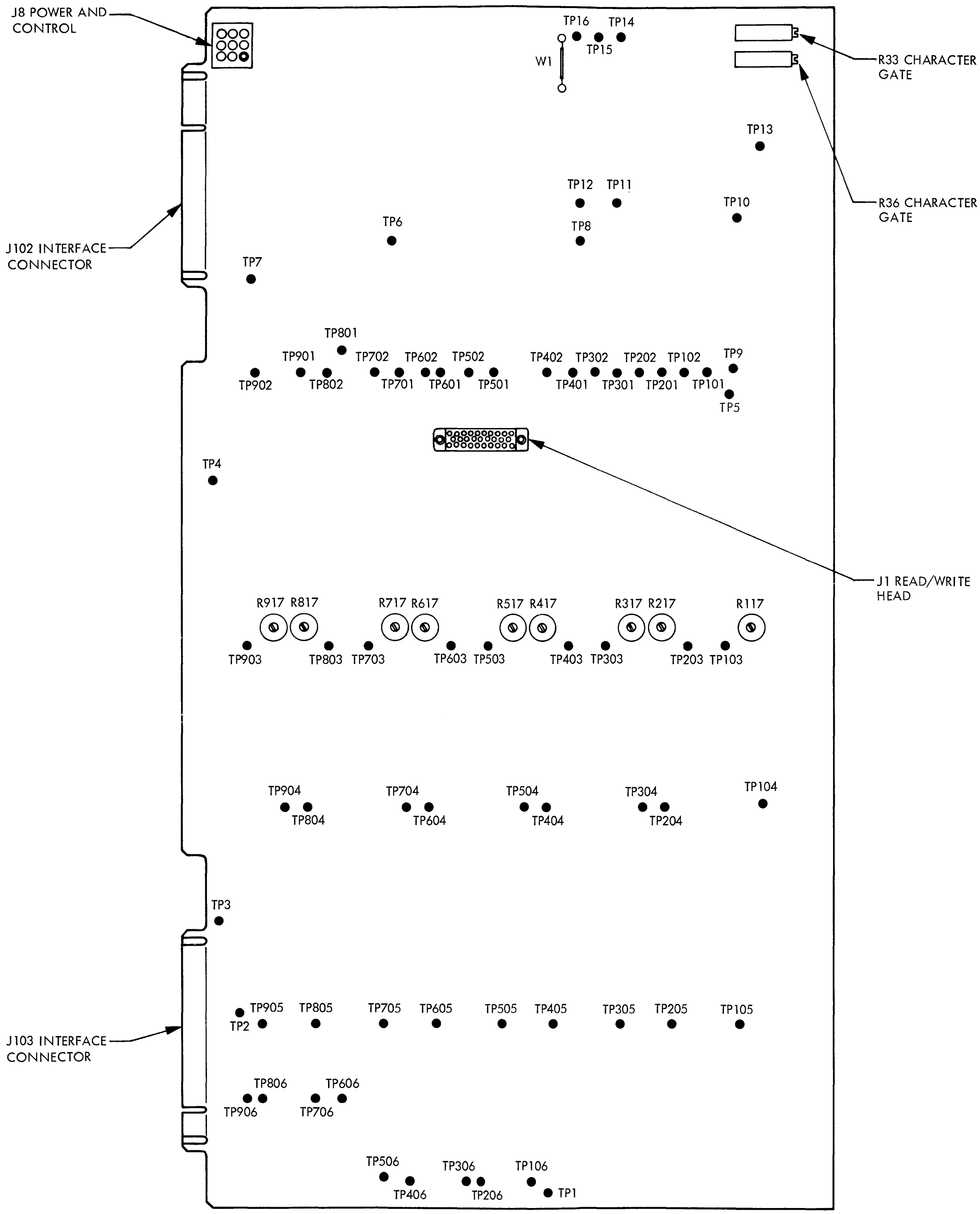


Figure 5-7. Data D1 PCBA, Test Point and Connector Placement

The MOTION level received at J8-6 prevents write current from flowing unless the tape is in motion.

The IWARS signal is used to write the LRC character at the end of a record. The leading edge of the IWARS pulse resets all the write flip-flops causing the head currents to be switched in those tracks where a 1 is required in the LRC character. The write current is defined by R107 and R108 and the damping resistor across the head which is the sum of R109 and R110.

During a read operation, transistors Q101 and Q102 are held nonconducting and, since Q1, Q2, and Q3 are cut-off, the effect of the write circuits is removed; therefore the head windings are left loaded by the read amplifier input resistors R109 and R110. The signals, at this point during a read operation, are so low that CR101 and CR102 do not conduct.

The read amplifier is one-half of a dual operational amplifier (U19-B). The amplifier output is maintained close to 0v by the feedback path of R116 and R113, which produces a fairly low dc gain. The low frequency cut-off is determined by capacitors C102 and C103. Diodes CR103 and CR104, shunting capacitors C102 and C103 are used to prevent large voltages from building up during a write operation. These are voltages which could prevent recovery of the amplifier during the available time prior to a subsequent read operation.

The operating gain of the amplifier is defined by the resistor network R114, R115, and R117. R117 is a variable resistor used in the initial setup to set the output peak-to-peak amplitude to 12v.

The read amplifier output is fed to a unity gain inverting amplifier, using transistors Q103, Q104, and Q105. The positive-going halves of the two phases of the read signal are added by means of diodes CR105 and CR106, and transistors Q106 and Q107. The exact voltage at which CR105 and CR106 conduct is controlled by the level at TP10, to which R123 is connected. This level is contolled by the IRTH interface line of J102. When IRTH is high (false), a voltage close to 0v is obtained at TP10, which results in a clip level of close to 20 percent of the read amplitude. When IRTH is low (true) a voltage close to +2v is obtained at TP10, which results in a clip level of close to 50 percent of the read amplitude.

The double emitter-follower stage Q106, Q107 is used to drive the input of the peak detector.

The peak detector is essentially a feedback differentiator circuit which uses one-half of a dual operational amplifier (U14-B). The amplifier is prevented from saturating by feedback diodes CR107, CR108, CR109, and CR110. The amplifier is biased to a negative output in the absence of an input signal by resistor R126. At this point, a positive-going transition from —1v to +1v corresponds to a peak of the read waveform. The output of the peak detector operational amplifier is passed to Q108, which converts the signal to standard logic levels. At this point, a negative-going edge corresponds to the peak of the read waveform. Resistor R131 and the corresponding resistors of the other eight circuits are connected to TP2. Examination of the output at TP2 with an oscilloscope while reading an *all ones* tape allows a good estimate to be made of the condition of the tape path. Skew is indicated by a progression of steps on the negative-going edge and the magnitude of skew by the ratio of fall time to the character time.

The output of Q108 is differentiated by capacitor C110 and resistor R132 and fed to the clock input of Read Staticiser flip-flop U4-A, setting it.

The $\overline{Q}$ output of U4-A together with those of the other eight Read Staticiser flip-flops are ORed by gate U2-B. The first flip-flop to be set causes a positive-going transition at TP11, which switches off clamp transistor Q7. This initiates run-down circuit Q6, Q7, Q8, and Q9.

With the transport operating in the Low Density mode, transistor Q6 is switched on by the NHID signal at J8-5. The conduction of Q6 places +5v at the cathode of CR1. This effectively reverse-biases CR1, removing R-32 and R-33 from the run-down circuit.

Switching off clamp transistor Q7 removes the +4.5v from the junction of R34 and R35. This allows the positive voltage on the cathode of CR2 to decay toward —5v with a time constant (R35 + R36) C28.

At approximately 0v, Q8 starts to cut off and this action is regenerative due to the positive feedback via capacitor C29 and resistor R40, resulting in a negative-going transition at the collector of Q9 (TP13). This transition is shaped by the single-shot circuit consisting of U2-A, U1-B, and capacitor C31 to form a 2-μsecond READ DATA STROBE pulse which is fed to the interface via power gate U3-B.

In addition, the negative transition is delayed via U1-F, resistor R46, capacitor C32, and inverter U1-A and fed via OR gate U3-A and power gate U5-B to the reset inputs of the Read Staticiser flip-flops. This causes the output of U2-B to go negative, turning on Q7; therefore, re-applying the clamp to the run-down circuit.

The delay is such that the data lines reset a minimum of 0.5 second after the trailing edge of the READ DATA STROBE.

The Read Staticisers are reset whenever the MOTION signal (J8-6) is false; i.e., tape is not in motion.

When the transport is operated in the High Density mode, transistor Q6 is cut off by the positive-going NHID signal at J8-5. Switching off Q6 removes the +5v at the cathode of CR1. This effectively places R32 and R33 in parallel with R35 and R36.

Switching off clamp transistor Q7 allows the positive voltage at the cathode of CR2 to decay toward —5v with a time constant determined by C28 and the parallel combination of R32, R33, and R34, R35.

Circuit action continues in the manner previously described under the Low Density mode of operation.

The 7-track version of the Data D1 is obtained by omitting circuits 200 and 300 from both the write and read sections of the circuit board. Jumper W-2 is employed in the 9-track transport to hold Q4 cut-off, thus allowing only one packing density (800 cpi).

5.2.5 SERVO AND POWER SUPPLY TYPES

The following are descriptions of the different Servo and Power Supply PCBAs, only one of which is applicable to a particular tape transport. Refer to the schematic/assembly documents at the end of this manual, or to the part number marked on the Servo and Power Supply PCBA to determine which assembly is installed.

Servo and Power Supply A (101021) is used for tape speeds up to and including 37.5 ips; Servo and Power Supply B (101262) can be used at any speed up to and including 45 ips.

A small EOT/BOT pre-amplifier circuit board (Assembly 101949) is utilized. This board is mounted on the Write Lockout bracket at the rear of the tape deck. It is required in addition to the basic EOT/BOT circuitry already on the Servo and Power Supply PCBAs to ensure correct operation.

5.2.6 SERVO AND POWER SUPPLY A (Schematic 101020 and Assembly 101021)

The Servo and Power Supply A (101021) is approximately 18 inches long and contains the reel servo amplifiers, capstan servo amplifiers, regulators, write enable and interlock circuitry, and the basic EOT/BOT sensor amplifier. The power transistors associated with the circuits are mounted on a heatsink.

The PCBA is secured to the heatsink by use of screws that also serve as connections between the transistor cases and the printed circuitry.

Connections are made to the PCBA via connectors which are strategically located with respect to their associated circuitry. Figure 5-8 shows the placement of each connector and test point. The connectors are used to:

(1) Connect all deck-mounted assemblies to the board, e.g., power supply, motors, tension arm sensors, photo-tab sensors, Write Lockout assembly, and the tension arm limit switch.

(2) Feed power and signal levels to the Tape Control PCBA.

5.2.6.1 Circuit Description (Schematic 101020, Assembly 101021)

The description of the circuit board consists of a discussion of the circuits associated with each of the connectors.

J17 is used to connect the tension arm interlock switch, the write lockout switch, and write lockout solenoid to the associated circuitry.

When the LOAD switch is depressed, the junction of resistors R120 and R121 is no longer grounded and base current is supplied to relay driver transistor Q56, turning it on. Relay K1 energizes, closing contacts 9 and 10, thus establishing an alternate source of base current for transistor Q56 via the interlock switch. When the LOAD control is released, the relay remains energized, completing the circuits for the capstan and reel servo motors and supplying write power from the +5v line to the write circuits via relay contacts 9 and 10.

For the capstan motor, the relay contact is placed on the ground return from the motor. For the reel motors, one side of each motor is grounded and the other connected to the appropriate amplifier output via the relay contact. When the relay is de-energized, the contacts connect the two reel motors together through a resistor (R41). This provides optimum regenerative braking conditions.

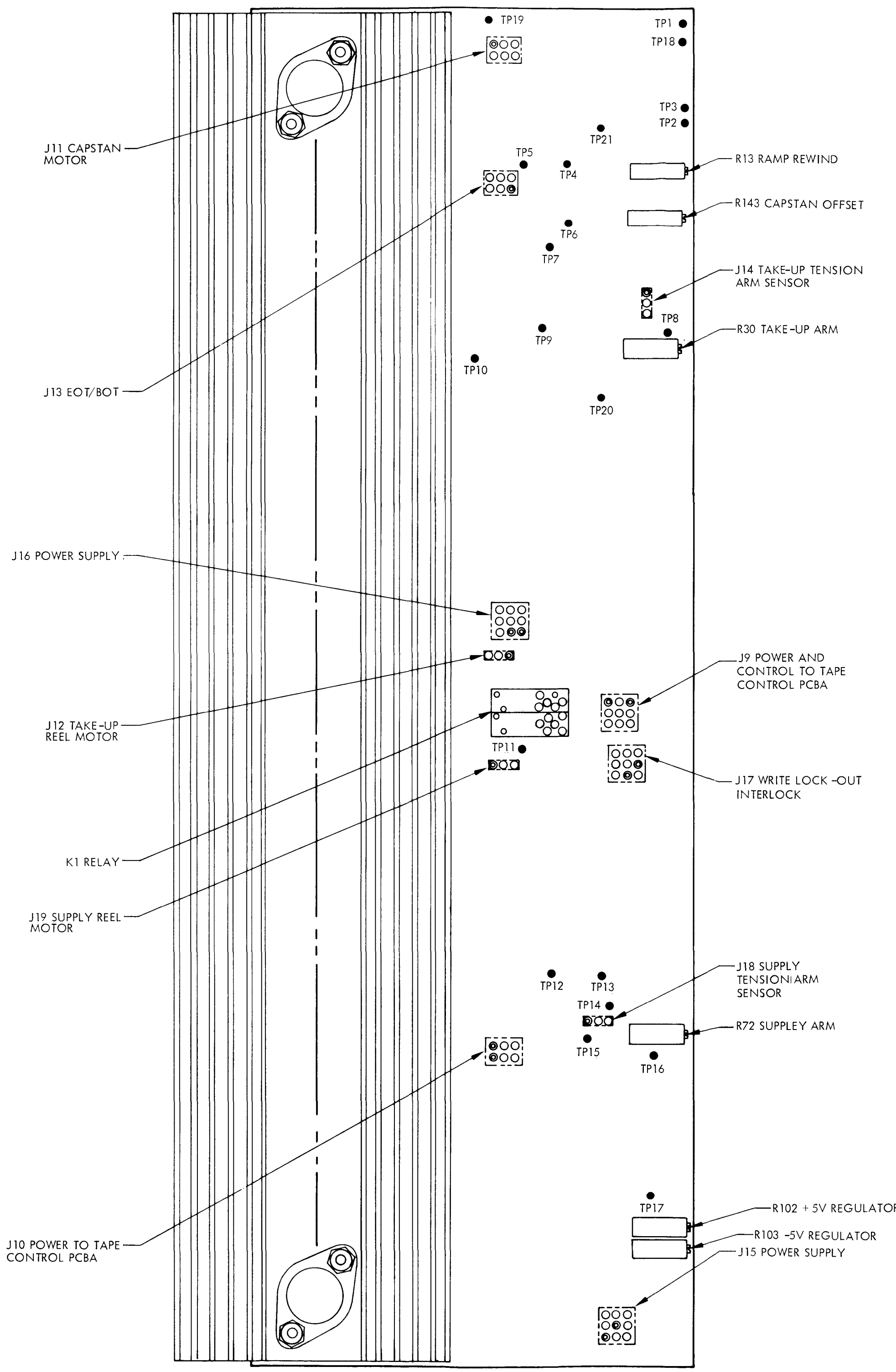


Figure 5-8. Servo and Power Supply A PCBA, Test Point and Connector Placement

Diodes CR2, CR3, CR14, CR15, CR4, and CR5 prevent arcing of the relay contacts when they are open.

Write lockout solenoid driver transistor Q57 is turned on by the appearance of the WRT POWER level and causes the write lockout solenoid to retract the write enable ring probe.

The relay voltage is derived from an auxiliary supply that decays rapidly upon loss of line voltage. This ensures that the relay drops out, removing motor power (and write current) before the main power supplies have had time to decay to the point where inadvertent motor motion (or writing) could occur.

J13 connects the photo-tab sensors mounted on the head plate to the Servo and Power Supply A PCBA, via the EOT/BOT Amplifier PCBA which is mounted on the Write Lockout bracket at the rear of the tape deck. Note that with the inclusion of this EOT/BOT Amplifier PCBA, potentiometers R1 and R10 on the Servo and Power Supply A PCBA are no longer used for adjustments and should always be set fully clockwise. Refer to Paragraph 5.2.9 for a description of the EOT/BOT Amplifier.

J15 and J16 connect unregulated +18v and —18v, +45v and —45v, and the auxiliary 14v ac for the relay, to the Servo and Power Supply PCBA. The +18v and —18v supplies are also fed via power diodes and power resistors in the power supply module (see Figure 4-3) to form the lines labeled +18v (D), —18v (D), +18v (R), and —18v (R), which are used in the reel servos and are connected to the Servo and Power Supply A PCBA via J15 and J18.

Two pins are allocated to the high current lines to reduce the current density in the pins.

Two regulators supply +5v and —5v to the digital ICs, photo-tab sensors, tension arm sensor lamps, indicator lamps, etc., and consist of two similar circuits whose outputs are set up by potentiometers R102 and R103. The +5v and —5v references are zener diodes CR16 and CR20. Diodes CR17 and CR19 improve the temperature stability of the supplies.

The zener diode references are also used by the +10v and —10v regulators. The majority of the current for the zener diodes is supplied from the +10v and —10v regulators via resistor R116 and diode CR18 for the +5v reference, and by resistor R99 and diode CR23 for the —5v reference. Resistors R97 and R98 provide the currents to prime the regulators. This system results in improved ripple characteristics for the regulator supplies.

A *crowbar* over-voltage protection circuit is provided and uses zener diode CR24 to detect an increase in the +5v level to +8v, in which case the SCR (CR25) is fired, which blows the +18v fuse on the power supply module and removes the +18v supply.

J11 connects the capstan motor assembly to the associated servo amplifier and relay contact. When the relay is energized, the ground return path of the motor is completed to 0v (S). The capstan servo amplifier uses one-half of a dual operational amplifier as an input stage and discrete transistors Q3, Q4, Q5, Q6, Q7, and Q8 to drive the high currents in the motor. Output transistors Q6 and Q8 are mounted on the heatsink.

In operation, defined currents are fed to the virtual ground input of the IC amplifier (pin 9 of U1-B) from either the Forward /Reverse ramp generator or the Rewind ramp generator (depending on the operation mode of the transport). R143 is provided to adjust a zero offset at TP5. These currents are amplified and cause the capstan motor-tachometer to rotate. The output voltage from the tachometer is fed back to the virtual ground input of the IC in such phase as to produce negative feedback. This system is a velocity servo in which the motor rotates at a speed such that the current from the tachometer is equal and opposite to that from the ramp generator.

The system is designed so motor tachometers from two different manufacturers (Electrocraft Corp. and Printed Motors, Inc.) can be used interchangeably. The tachometer voltage constants are different in the two cases, therefore two different tachometer feedback paths are provided: J11 pin 2 and resistors R23 and R24 for the Electrocraft motor; J11 pin 1 and resistors R129 and R24 for the Printed Motors, Inc. motor. The overall gain of the tachometer input is (R15 + R17)/(R23 + R24) for the Electrocraft, and R15 + R17) / (R129 + R24) for the Printed Motors, Inc. motor. Potentiometer R13 allows the rewind speed to be adjusted.

J14 and J18 connect the take-up and supply tension arm sensors to the reel servo amplifiers on the Servo and Power Supply A PCBA.

The take-up servo circuit is a conventional dc amplifier with transient phase lead compensation. The low frequency gain is defined by the ratio of resistors (R48 + R44 + R43) to (R31 + R30). This gain can be changed using variable resistor R30 to compensate for variations in tension arm sensor sensitivity. The low frequency gain is approximately 3 when R30 is set at the mid-point. The high frequency gain is increased to 14 by capacitors C12 and C13 and resistor R125. Output transistors Q16 and Q18 are located on the heatsink.

In the Rewind mode the characteristics of the reel servo amplifier are altered in the following manner.

(1) The loop gain is increased by a factor of 2 (approximately) by switching resistor R46 into the circuit. This is accomplished from the rewind ramp command waveform via transistors Q19 and Q21.

(2) An offset signal is fed to the servo amplifier via R32.

(3) The +18v (D) return voltage is raised to +36v by switching in the 36v *regulator* circuit Q22, Q23, Q24, and Q25. The appropriate diode on the power supply module isolates the +36v supply from the +18v supply.

Items (1) and (2) result in a reduction in the arm movement required in the Rewind mode.

A current limiting circuit consisting of resistor R40 and transistor Q14 is used to hold the reel servo current in the —18v supply to less than 9 amps when the take-up tension arm is released, e.g., when tape tension is lost at the end of an unload operation.

The supply servo operates in exactly the same manner except that:

(1) The gain switching utilizes resistor R78.

(2) The offset voltage is supplied via resistor R74.

(3) The current limiting components, resistor R94 and transistor Q39 are in the +18v supply.

(4) The —18v (D) return voltage is increased to —36v by components Q26, Q27, Q28, and Q29.

5.2.7 SERVO AND POWER SUPPLY B (Schematic 101261 and Assembly 101262)

The Servo and Power Supply B PCBA is approximately 18 inches long and contains the reel servo amplifiers, capstan servo amplifier, regulators, write enable and interlock circuitry, and the basic EOT/BOT sensor amplifier. The power transistors associated with the circuits are mounted on an 18-inch long heatsink. The PCBA is secured to the heatsink by screws that also serve as connections between the transistor cases and the printed circuit.

Connections are made to the board via connectors which are strategically located with respect to their associated circuitry. Figure 5-9 shows the placement of each connector and test point. The connectors are used to:

(1) Connect all deck-mounted assemblies to the board, e.g., power supply, motors, tension arm sensors, photo-tab sensors, Write Lockout assembly, and the tension arm limit switch.

(2) Feed power and signal levels to the Tape Control PCBA.

5.2.7.1 Circuit Description (Schematic 101261, Assembly 101262)

The description of the circuit board consists of a discussion of the circuits associated with each of the connectors.

J17 is used to connect the tension arm interlock switch, the write lockout switch, and write lockout solenoid to the associated circuitry.

When the LOAD switch is depressed, the junction of resistors R138 and R139 is no longer grounded and base current is supplied to relay driver transistor Q53, turning it on. Relay K1 energizes, closing contacts 9 and 10, thus establishing an alternate source of base current for transistor Q53 via the interlock switch. When the LOAD control is released, the relay remains energized, completing the circuits for the capstan and reel servo motors and supplying write power from the +5v line to the write circuits via relay contacts 9 and 10.

For the capstan motor, the relay contact is placed in the ground return from the motor. For the reel motors, one side of each motor is grounded and the other connected to the appropriate amplifier output via the relay contact. When the relay is de-energized, the contacts connect the two reel motors together by a resistor (R76). This provides optimum regenerative braking conditions.

Diodes CR2, CR3, CR14, CR15, CR8, and CR9 prevent arcing of the relay contacts when they are opened.

Write lockout solenoid driver transistor Q54 is turned on by the appearance of the WRT POWER level and causes the write lockout solenoid to retract the write enable ring probe.

The relay voltage is derived from an auxiliary supply that decays rapidly upon loss of line voltage. This ensures that the relay drops out, removing motor power (and write current) before the main power supplies have had time to decay to the point where inadvertent motor motion (or writing) could occur.

J13 connects the photo-tab sensors mounted on the head plate to the Servo and Power Supply B PCBA via the EOT/BOT Amplifier PCBA which is mounted on the Write Lockout bracket at the rear of the tape deck. Note that, with the inclusion of this EOT/BOT Amplifier PCBA, potentiometers R2 and R10 on the Servo and Power Supply board are no longer used for adjustments and should always be set fully clockwise. Refer to Paragraph 5.2.9 for a description of the EOT/BOT Amplifier circuit.

The EOT sensor output drives emitter-follower transistor Q2 via an R-C network (R128, C32) which filters any spurious signals. The output of the emitter-follower is fed to the interface transmitter on the Tape Control board and is not used elsewhere.

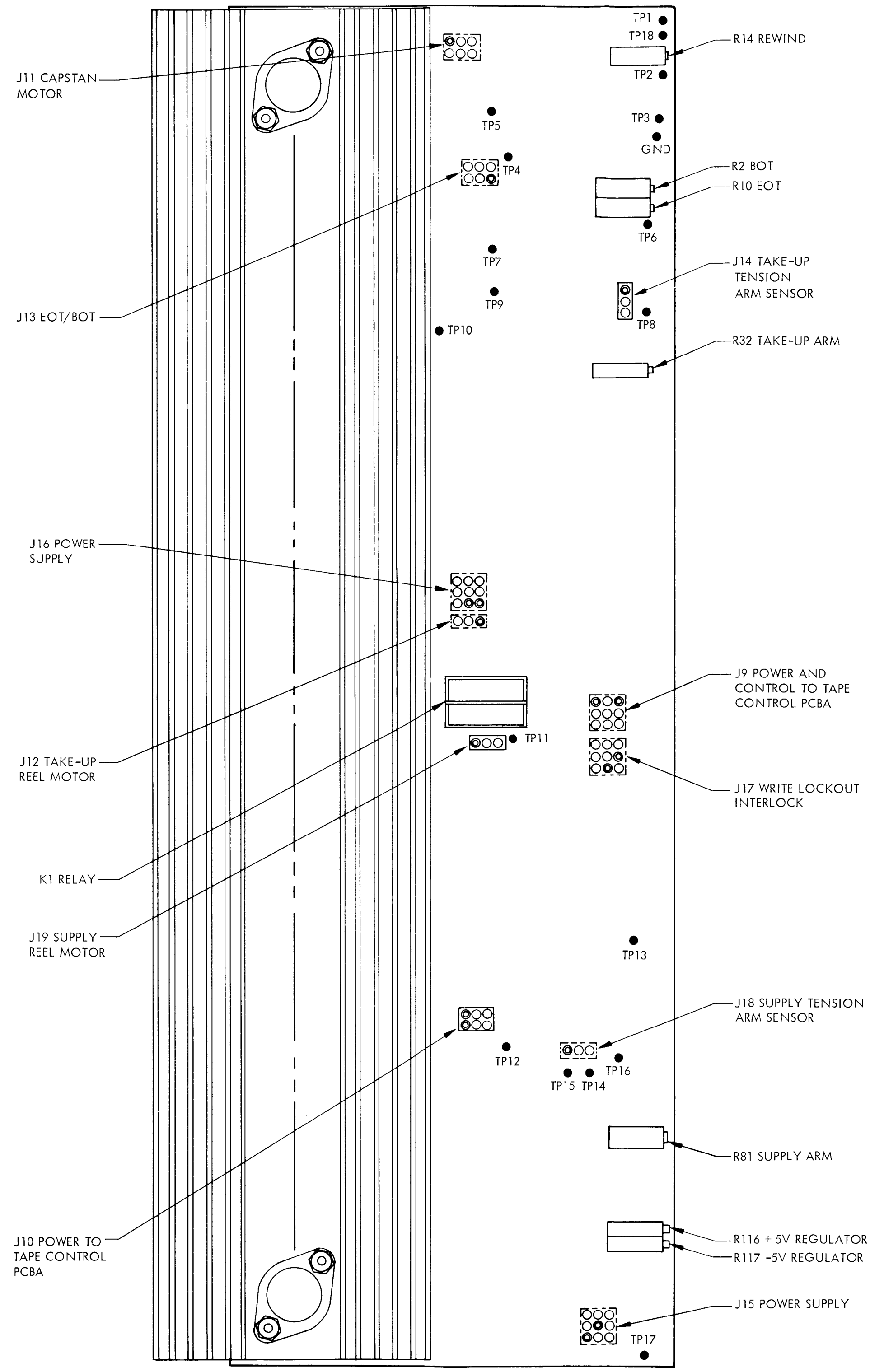


Figure 5-9. Servo and Power Supply B PCBA, Test Point and Connector Placement

The BOT signal is fed via an R-C network (R4, C1) to a Schmitt trigger circuit to remove the possibility of multiple pulses at the leading and trailing edges of the BOT tab. The Schmitt trigger uses one-half of a dual operational amplifier IC (U1-A) connected in a positive feedback mode and set to switch at approximately 2.3v. The output of the BOT phototransistor drops upon detection of the photo-tab. The output of the Schmitt trigger is inverted by transistor Q1 and connected to the Tape Control board by J9.

J15 and J16 connect unregulated +18v and —18v, +45v and —45v, and the auxiliary 14v ac for the relay to the Servo and Power Supply B PCBA. The +18v and —18v supplies are also fed via power diodes and power resistors in the power supply module (see Figure 4-2) to form the lines labeled +18v (D), —18v (D), +18v (R), and —18v (R), which are used in the reel servos and are connected to the Servo and Power Supply B PCBA via J15 and J16.

Two pins are allocated to the high current lines to reduce the current density in the pins.

Two regulators supply +5v and —5v to the digital ICs, photo-tab sensors, tension arm sensor lamps, indicator lamps, etc., and consist of two similar circuits whose outputs are set up by potentiometers R116 and R117. The +5v and —5v references are zener diodes CR16 and CR19. Diodes CR17 and CR18 improve the temperature stability of the supplies.

The zener diode references are also used by the +10v and —10v regulators. The majority of the current for the zener diodes is supplied from the +10v and —10v regulators via resistor R134 and diode CR20 for the +5v reference, and by resistor R119 and diode CR2 for the —5v reference. Resistors R115 and R118 provide the currents to prime the regulators.

A *crowbar* over-voltage protection circuit is provided and uses zener diode CR24 to detect an increase in the +5v level to +8v, in which case the SCR (SCR1) is fired, which blows the +18v fuse on the power supply module and removes the +18v from the regulators.

J11 connects the capstan motor assembly to the associated servo amplifier and relay contact. When the relay is energized, the ground return path of the motor is completed to 0v (S). The capstan servo amplifier uses one-half of a dual operational amplifier as an input stage and discrete transistors Q3, Q4, Q5, Q6, Q7, and Q8 to drive the high currents in the motor. Output transistors Q6 and Q8 are mounted on the heatsink.

In operation, defined currents are fed to the virtual ground input of the IC amplifier (pin 9 and U1-B) from either the Forward/Reverse ramp generator or the Rewind ramp generator (depending on the operation mode of the transport). These currents are amplified and cause the capstan motor-tachometer to rotate. The output voltage from the tachometer is fed back to the virtual ground input of the IC in such phase as to produce negative feedback. This system is a velocity servo in which the motor rotates at a speed such that the current from the tachometer is equal and opposite to that from the ramp generator.

The system is designed so that motors/tachometers from two different manufacturers (Electrocraft Corp. and Printed Motors, Inc.) can be used interchangeably. The tachometer voltage constants are different in the two cases, therefore two different tachometer feedback paths are provided: J11 pin 2 and resistors R18 and R19 for the Electrocraft motor; J11 pin 1 and resistor R17 and R19 for the Printed Motors, Inc., motor. The overall gain of the tachometer input is (R23 + R21) / (R18 + R19) for the Electrocraft, and (R23 + R21) / (R17 + R19) for the Printed Motors, Inc. Potentiometer R14 allows the Rewind speed to be adjusted.

J14 and J18 connect the take-up and supply tension arm sensors to the reel servo amplifiers on the Servo and Power Supply B PCBA.

The take-up servo circuit is a conventional dc amplifier with lead-lag compensation. The low frequency gain is defined by the ratio of resistors R54 to (R34 + R35) and is approximately 33. The high frequency gain is increased by capacitors C11 and C12. Output transistors Q15 and Q17 are located on the heatsink.

The reel motor current is limited to approximately 8 amps by amplifying (via U3B) the voltage developed by the reel motor current across resistor R77 and feeding this in proper phase to the input of the reel servo amplifier via pick-off diodes CR6 and CR7. Potentiometer R32 adjusts the amplitude of the take-up arm swing.

In the Rewind mode, the characteristics of the reel servo amplifier are altered so that the +18v (D) return voltage is raised to +36v. This is accomplished by switching in the 36v regulator circuit Q20, Q21, Q22, and Q23. An appropriate diode on the power supply module isolates the +36v supply from the +18v supply.

The supply servo operates in the same manner; potentiometer R81 adjusts the amplitude of the supply arm swing. In Rewind, the —18v (D) return voltage is increased to —36v by the components Q24, Q25, Q26, and Q27 which are supplied by unregulated —45v. The reel motor current limiting components are U3A, R114, CR12, and CR13.

5.2.8 TAPE CONTROL C1

The following is a description of the Tape Control C1 PCBA (refer to Schematic 101240 and Assembly 101241).

The Tape Control C1 contains the control logic together with command ramp generators for the capstan servo. Figure 5-10 shows the placement of each connector and test point. The PCBA is approximately 16.5 inches long with an edge connector (J101) at one end; this is the interface connector and is slotted to mate with a key in the mating plug. At the same end of the board is a row of connectors which are used to connect the manual control switches to the Tape Control board. In addition, two connectors (J9 and J10) transmit power and control levels from the Servo and Power Supply PCBA to the Tape Control while connector J8 supplies power and control levels to the Data PCBA. The power supplies (+10v and —10v, +5v and —5v, and 0v) as well as the MOTION, NWRT, and WRT POWER signals associated with the writing of data are picked off from this latter connector.

5.2.8.1 Circuit Description

A description of the logic sequences used in the Tape Control PCBA is detailed in Paragraphs 4.3.5 through 4.3.5.11. Table 5-1 will assist in identifying the major components in the system; however, 100 percent correspondence is not possible since Figure 4-20 is a logic diagram, while the schematic shows every component.

The remaining circuitry on the Tape Control is concerned with the generation of ramp command signals for the capstan servo and the BOT single-shot.

J101 is the interface connector for tape motion commands and status signals. ISFC, ISRC, and IRWC commands are received and gated with the SRO (Selected, Ready, and On-line) signal. They then pass on to the ramp generator (circuit 900), where the digital signals are converted to analog levels with controlled transition times, which are the inputs to the

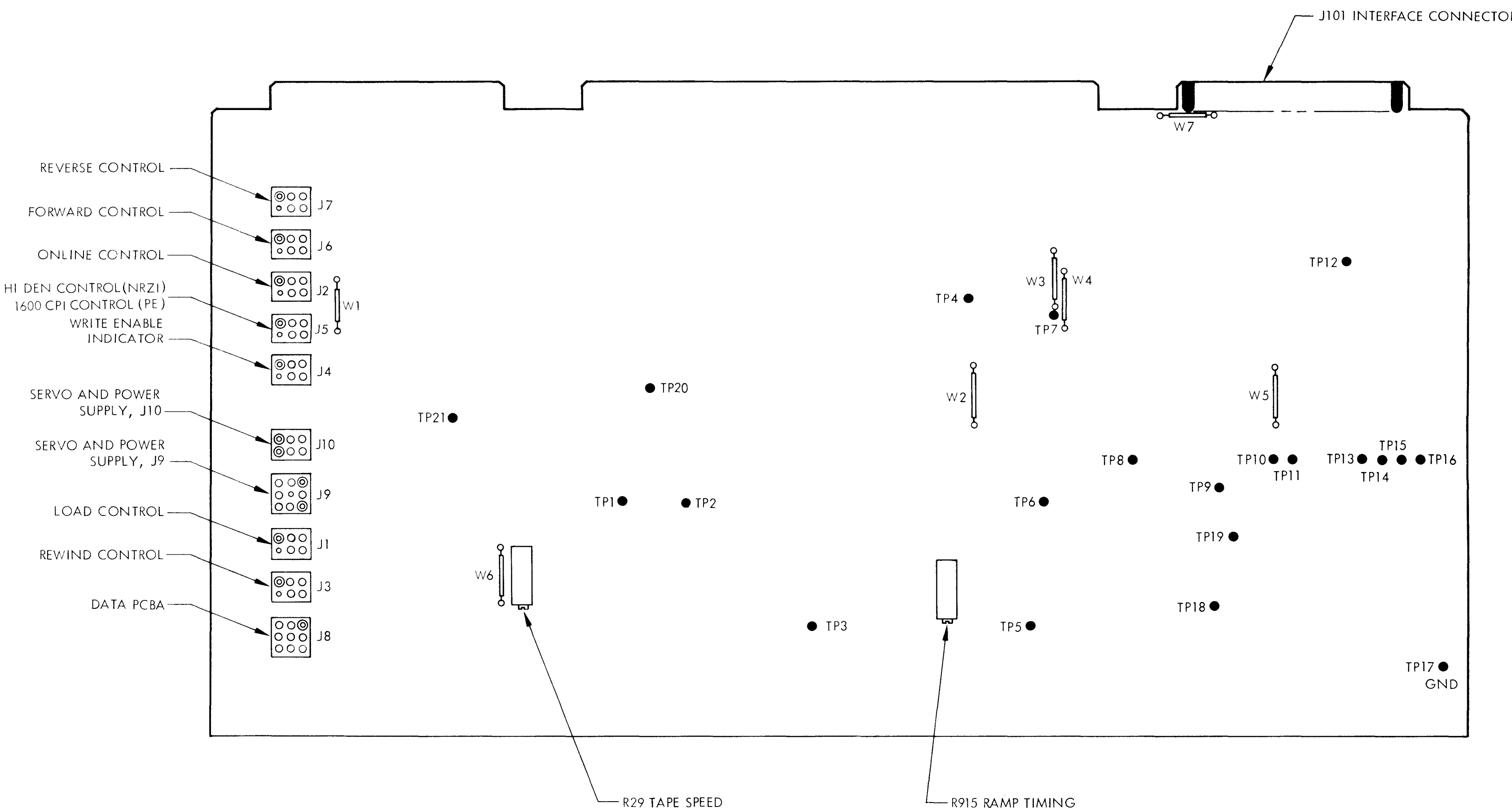


Figure 5-10. Tape Control C1 PCBA, Test Point and Connector Placement

Table 5-1
Cross Reference Chart

Figure 4-20 Reference Designation	Schematic 101240 Reference Designation
U1	U11-A, U11-B
U2	U11-C, U13-C
U15	U17-A
U16	U17-B
U17	U15-B
U18	U15-A
U20	U7-B
U25	U8-F, U8-C
U26	U7-A
U31	U9-A, U9-B
SS	Circuit 700
U12	U13-B
U13	U18-B
U10	U13-D
U9	U13-A
U6	U21-A
U8	U21-D
U38	U12-B

capstan servo. The ISFC and ISRC are fed via transistors Q1 and Q2 to the dual operational amplifier circuit (U17-A, U17-B) whose output levels are determined by the +5v and —5v lines, and the ratios of R905 and R907 to R913; the circuit rise and fall times are determined by the +5v and —5v lines, R915, R916, and C904. The transition times are varied by means of variable resistor R915. The forward and reverse speeds are determined by the variable resistor R29 and associated circuitry which is contained on the Servo and Power Supply PCBA.

The REWIND command is fed to circuit 800, which includes transistors Q801 and Q802. The rewind speed is determined by the —5v line to which transistor Q802 saturates when a rewind is in process, feeding an associated resistor in the capstan servo amplifier located on the Servo and Power Supply PCBA.

The rise and fall times of the rewind ramp are determined by resistors R801 and R802 in conjunction with capacitors C801 and C802.

The BOT single-shot consists of the components in circuit 700. The circuit is triggered by the leading edge of the BOT waveform, producing a pulse approximately 0.5-second wide. This width is determined by capacitors C701 and C702 in conjunction with resistors R703 and R704. The single-shot pulse (NBOTD) is inverted and the trailing edge is differentiated by capacitor C5 in conjunction with resistors R24 and R25 and fed to inverter U14A. In this manner, a narrow pulse (BOTDP) is generated whose width is determined by capacitor C5 in conjunction with resistors R24 and R25.

The Write Power Enable circuit is basically an R-C ramp utilizing a Darlington-pair transistor circuit. Write power is applied to the circuit from the Servo and Power Supply PCBA via J9 pin 4.

NOTE

A Write Enable ring must be installed on the supply reel to complete the Write Power interlock circuit.

When a Write or Overwrite operation is initiated, voltage at pin A of circuit 1000 drops sharply to 0v and the +5v charge on capacitor C1 discharges toward 0v. (The R-C time of discharge determined by the values of C1, R1.) Transistor Q1 conducts and causes transistor Q2 to conduct. The rate of conduction is determined by the discharge time of C1. The voltage at the collector of Q2 rises toward +5v as determined by the current flow through R4 and Q2. The output voltage is supplied via J8 pin 4 to the Write logic on the Data PCBA.

Termination of a Write or Overwrite operation causes the voltage at pin A of circuit 1000 to rise sharply to +5v. Conduction of transistors Q1 and Q2 decrease toward cutoff at a rate determined by (R34 + R1) C1. The output voltage at the collector of Q2 ramps from +5v to 0v as Q2 cuts off.

5.2.9 EOT/BOT AMPLIFIER PCBA

The following is a description of the EOT/BOT Amplifier PCBA (refer to Schematic 101948 and Assembly 101949).

5.2.9.1 Circuit Description

J1 connects the photo-tab sensor, mounted on the head plate, to the EOT/BOT Amplifier PCBA which is mounted on a bracket at the rear of the tape deck.

The amplifier is designed to operate on the differential output from the EOT and BOT sensors (both tabs are never allowed to be under the sensors simultaneously). This system is basically insensitive to changes in ambient conditions.

In operation, when neither the BOT tab nor the EOT tab is under the photosensor, the outputs of the BOT and EOT sensors are high (approximately +4v) and are adjusted to be equal by the use of variable resistors R9 and R3. The bases of Q2 and Q5 are therefore at approximately +4v so that diodes CR1, CR3, and CR2, CR4 are forward biased by current flowing via R6 to ground. Thus, the base of Q3 is 1.2v below that of Q2, and the base of Q4 is 1.2v below that of Q5. Hence, Q2 and Q1 and Q5 and Q6 are cut off and the NBOT and NEOT outputs are high (pulled up by resistors on the Servo and Power Supply PCBA).

The characteristics of the photosensors are such that the *no tab* voltages, once set to be equal, track adequately with changes in ambient conditions to ensure that the NBOT and NEOT outputs remain high.

When the BOT tab moves under the sensor, its output drops toward 0v. Thus, the base of Q5 goes negative while that of Q4 remains referenced to the still high output of the EOT sensor. When the difference of voltage between the bases of Q5 and Q4 exceeds 1.2v, current flows in Q5, turning Q6 on. The NBOT output therefore goes low as required. Similarly, when the EOT tab moves under the sensor, the NEOT output goes low.

The output of the EOT/BOT amplifier board is connected to J13 on the Servo and Power Supply PCBA.

SECTION VI
MAINTENANCE AND TROUBLESHOOTING

6.1 INTRODUCTION

This section provides information necessary to perform electrical and mechanical adjustments, parts replacement, and troubleshooting. Sections IV and V contain the theory of operation and schematics required for reference when electrical adjustments or troubleshooting are necessary.

6.2 FUSE REPLACEMENT

Fuses are located on the Power Supply module at the rear of the transport.

Line Fuse: 5 amp, 3AG, slow-blow, 125v ac and below, or
3 amp, 3AG, slow-blow, 190v ac, and above

+18v dc Fuse: 10 amp, 3AG

—18v dc Fuse: 10 amp, 3AG

6.3 SCHEDULED MAINTENANCE

The tape transport is designed to operate with a minimum of maintenance and adjustments. Replacement of parts is designed to be as simple as possible. Repair equipment is kept to a minimum and only common tools are required in most cases. A list of tools required to maintain the tape transport is given in Paragraph 6.8.

To assure that the transport operates at its optimum design potential and to assure high MTBF, a program of scheduled preventive maintenance is recommended. This schedule is given in Table 6-1.

Table 6-1

Preventive Maintenance Schedule

Maintenance Operation	Frequency (Hours)	Qty to Maintain	Time Req'd (Minutes)	Manual Para. Ref.
Clean Head, Guides, Roller Guides, and Capstan	8 (or start of operating day)	—	5	6.4
Clean Tape Cleaner	50	1	5	6.4
Check Skew, Tape Tracking and Speed	500	—	15	6.7.5 or 6.7.6, 6.6.10
Check Head Wear	2,500	1	3	6.7.8
Replace Reel Motors and Capstan Motor	10,000	3	30	6.7.11

6.4 CLEANING THE TRANSPORT

The transport requires cleaning in these major areas: head and associated guides, capstan, roller guides, and tape cleaner.

To clean the head and guides, use a lint-free cloth or cotton swab moistened in 91 percent isopropyl alcohol. Wipe the head carefully to remove all accumulated oxide and dirt.

CAUTION

A ROUGH OR ABRASIVE CLOTH SHOULD NOT BE USED TO CLEAN THE HEAD AND HEAD GUIDES; USE ONLY ISOPROPYL ALCOHOL. OTHER SOLVENTS, SUCH AS CARBON TETRACHLORIDE, MAY RESULT IN DAMAGE TO THE HEAD LAMINATION ADHESIVE.

To clean the capstan, use only a cotton swab moistened with 91 percent isopropyl alcohol to remove accumulated oxide and dirt.

To clean the roller guides, use a lint-free cloth or cotton swab moistened with 91 percent isopropyl alcohol. Wipe the guide surfaces carefully to remove all accumulated oxide and dirt.

CAUTION

DO NOT SOAK THE GUIDES WITH EXCESSIVE SOLVENT. EXCESSIVE SOLVENT MAY SEEP INTO THE PRECISION GUIDE BEARINGS, CAUSING CONTAMINATION AND A BREAKDOWN OF THE BEARING LUBRICANT.

Clean the tape cleaner by removing the Allen head retaining screw accessible at the top of the cleaner assembly. Remove the cleaner from the tape deck by firmly grasping the cleaner and pulling straight upward and away from the tape deck. When removed, loosen the two side screws holding the cleaner blade to the housing and remove the blade. The accumulated oxide and dirt is then blown out of the housing and the blade and housing are cleaned with a cotton swab moistened with 91 percent isopropyl alcohol. Care should be taken to avoid particles of the cotton swab from adhering to the blade. The blade is then relocated and the two side retaining screws are tightened. The tape cleaner is reinstalled on the deck.

CAUTION

CARE SHOULD BE TAKEN TO ENSURE THAT THE TAPE CLEANER BLADE SURFACE IS PARALLEL TO THE TAPE AND THAT THE TAPE IS WRAPPED SYMMETRICALLY AROUND THE TAPE CLEANER [THE ENTRY ANGLE IS EQUAL TO THE EXIT ANGLE].

6.5 PART REPLACEMENT ADJUSTMENTS

Table 6-2 indicates the adjustments necessary when a part is replaced. The details of the adjustments are given in Paragraph 6.6 through 6.7.16.

Table 6-2

Part Replacement Adjustments

Part Replaced	Auxiliary Adjustments	Time Req'd (Minutes)	Manual Para. Ref.
Control Switch	None	2	—
Photo-Tab Sensor	EOT/BOT Potentiometers on EOT/BOT Amplifier or Servo and Power PCBA	10	6.7.9
Tension Arm Sensor	Tension Arm Shutter	10	6.7.2, 6.7.3, or 6.7.4
Limit Switch Assy	None	10	—
Capstan Drive Assy	Tape Speed, Ramp on Tape Control PCBA	30	6.7.11
Reel Motor Assy	Belt Tension	10	6.7.15
Power Supply Assy	None	20	—
Tape Control PCBA	Ramp Timing, Tape Speed	20	6.6.9, 6.6.10
Data PCBA	Read Amplifier Gain, Read Staticiser, Write Skew (6X40 Only)	20	6.6.12 or 6.6.13, 6.6.15 or 6.6.16, 6.7.6.2
EOT/BOT Amplifier Assy	None	10	—
Head	Read Skew, Write Skew (6X40 Only), Read Amplifier Gain	30	6.7.5, 6.7.6, 6.6.12 or 6.6.13
Write Lockout Assy	None	10	—
Servo and Power Supply PCBA	5v Regulators, EOT/BOT Amplifiers, Reel Servo Gain, Rewind Speed (Servo and Power B Only), Capstan Offset, Tension Arm	25	6.6.3, 6.6.4, 6.6.6, 6.6.7, 6.6.11

6.6 ELECTRICAL ADJUSTMENTS

Paragraphs 6.6.2 through 6.6.14 describe the test configurations, test procedures, adjustment procedures, and related adjustments for the 5v regulators, BOT and EOT amplifiers, ramp timing, tape speed, reel servo gain, read amplifier gain, read staticiser, and write deskewing.

The following equipment (or equivalent) is required.

(1) Oscilloscope, Tektronix 561 (vertical and horizontal sensitivity specified to + 3 percent accuracy)

(2) Digital Volt Meter, Fairchild 7050 (+ 0.1 percent specified accuracy)

(3) Counter Timer, Monsanto Model 100B (+ 0.1 percent specified accuracy) *

(4) Master Skew Tape, IBM No. 432640

(5) Optical Encoder, 500-Line, PERTEC No. 512-1100 *

6.6.1 ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified in Paragraph 6.6.

When the measured value of any parameter is within the specified acceptable limits NO ADJUSTMENTS should be made. Should the measured value fall outside the specified acceptable limits, adjustment should be made in accordance with the relevant procedure.

When adjustments are made, the value set should be the exact value specified (to the best of the operator's ability).

CAUTION

SOME ADJUSTMENTS MAY REQUIRE CORRESPONDING ADJUSTMENTS IN OTHER PARAMETERS. ENSURE CORRESPONDING ADJUSTMENTS ARE MADE AS SPECIFIED IN THE INDIVIDUAL PROCEDURES. THE +5 AND —5 REGULATOR VOLTAGES MUST BE CHECKED PRIOR TO ATTEMPTING ANY ELECTRICAL ADJUSTMENT.

*Used only if Optical Encoder method of setting tape speed is desired (Paragraph 6.6.11).

6.6.2 SERVO AND POWER SUPPLY PCBA TYPES

One of two types of the Servo and Power Supply PCBA is installed in the transport. Refer to Paragraph 5.2.5 for details regarding the differences.

NOTE

Independent adjustment procedures are given, where applicable, for the different Servo and Power Supply PCBA types; ensure that the appropriate procedures are followed.

6.6.3 +5V AND —5V REGULATORS (SERVO AND POWER SUPPLY A PCBA NO. 101021 ONLY)

The +5v and —5v regulators are located on the Servo and Power Supply A PCBA (101021) and are adjusted by means of variable resistors R102 and R103. The numerical value of the voltage difference, disregarding polarity, between the +5v and —5v lines must be less than 0.07v.

6.6.3.1 Test Configuration (Assembly No. 101021 Only)

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlock and tension the tape.

(4) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.3.2 Test Procedure (Assembly No. 101021 Only)

(1) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the voltage difference between TP18 (+5v) on the Tape Control PCBA, and TP17 (0v) on the Servo and Power Supply A PCBA.

(2) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the voltage difference between TP19 (—5v) on the Tape Control PCBA, and TP17 (0v) on the Servo and Power Supply A PCBA.

(3) Acceptable Limits

- ☐ +5v Regulator
  - +4.85v minimum
  - +5.15v maximum
- ☐ —5v Regulator
  - —4.85v minimum
  - —5.15v maximum

(4) Compare the voltages obtained in Steps (1) and (2). Voltages must fall within the acceptable limits and the absolute difference between the +5v and —5v lines must be less than 0.07v.

6.6.3.3 Adjustment Procedure (Assembly No. 101021 Only)

When the acceptable limits are exceeded, or the voltage difference between the +5v and —5v lines exceed 0.07v, perform the following adjustments.

(1) Adjust variable resistor R102 on the Servo and Power Supply A PCBA to +5.0v as observed at TP18 on the Tape Control PCBA (using TP17 on the Servo and Power Supply A PCBA as the 0v reference).

(2) Adjust variable resistor R103 on the Servo and Power Supply A PCBA to —5v as observed at TP19 on the Tape Control PCBA (using TP17 on the Servo and Power Supply A PCBA as the 0v reference).

6.6.3.4 Related Adjustments (Assembly No. 101021 Only)

The following areas must be checked and adjusted subsequent to adjusting the +5v and —5v regulators.

(1) Ramp Timing (Paragraph 6.6.9).

(2) Tape Speed (Paragraph 6.6.10).

6.6.4 +5V AND —5V REGULATORS (SERVO AND POWER SUPPLY B PCBA NO. 101262 ONLY)

The +5v and —5v regulators are located on the Servo and Power Supply B PCBA (101262) and are adjusted by means of variable resistors R116 and R117. The numerical value of the voltage difference, disregarding polarity, between the +5v and —5v lines must be less than 0.07v.

6.6.4.1 Test Configuration (Assembly No. 101262 Only)

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlock and tension the tape.

(4) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.4.2 Test Procedure (Assembly No. 101262 Only)

(1) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the voltage difference between TP18 (+5v) on the Tape Control PCBA, and TP17 (0v) on the Servo and Power Supply B PCBA.

(2) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the voltage difference between TP19 (—5v) on the Tape Control PCBA, and TP17 (0v) on the Servo and Power Supply B PCBA.

(3) Acceptable Limits

- ☐ +5v Regulator
  - +4.85v minimum
  - +5.15v maximum
- ☐ —5v Regulator
  - —4.85v minimum
  - —5.15v maximum

(4) Compare the voltages obtained in Steps (1) and (2). Voltages must fall within the acceptable limits and the absolute difference between the +5v and —5v lines must be less than 0.07v.

6.6.4.3 Adjustment Procedure (Assembly No. 101262 Only)

When the acceptable limits are exceeded, or the voltage difference between the +5v and —5v lines exceed 0.07v, perform the following adjustments.

(1) Adjust variable resistor R116 on the Servo and Power Supply B PCBA to +5.0v as observed at TP18 on the Tape Control PCBA (using TP17 on the Servo and Power Supply B as the 0v (ground) reference).

(2) Adjust variable resistor R117 on the Servo and Power Supply B PCBA to —5v as observed at TP19 on the Tape Control PCBA (using TP17 on the Servo and Power Supply B as the 0v (ground) reference).

6.6.4.4 Related Adjustments (Assembly No. 101262 Only)

The following areas must be checked and adjusted subsequent to adjusting the +5v and —5v regulators.

(1) Ramp Timing (Paragraph 6.6.9).

(2) Tape Speed (Paragraph 6.6.11).

(3) EOT/BOT Amplifier (Paragraph 6.6.6).

(4) Capstan Servo Offset (Paragraph 6.6.10).

6.6.5 EOT/BOT AMPLIFIER SYSTEMS

Two different EOT/BOT amplifier systems may be installed in the transport. The Servo and Power Supply PCBA includes EOT/BOT circuitry integrated on the board. In some cases, an additional EOT/BOT Amplifier PCBA is included; this PCBA is approximately 2 X 4 inches and is located on the Write Lockout bracket at the rear of the tape deck. Test and adjustment procedures are given for each system.

6.6.6 EOT/BOT AMPLIFIER (SCHEMATIC NO. 101948, ASSEMBLY NO. 101949)

The EOT/BOT Amplifier PCBA is located on the Write Lockout bracket at the rear of the tape deck. The following procedures are employed in testing and adjusting the EOT/BOT Amplifier PCBA.

NOTE

The +5v and —5v regulator voltages must be checked and adjusted prior to adjusting the EOT/BOT amplifier system. Measurements and adjustments should be made at room temperature.

6.6.6.1 Test Configuration (Assembly 101949)

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.6.2 Test Procedure (Assembly 101949)

(1) Advance tape until the reflective tab is past the photosensor, i.e., photosensor is over a non-tab area.

(2) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the off-tab voltage between TP1 (EOT) on the EOT/BOT Amplifier PCBA and TP17 (0v) on the Servo and Power Supply PCBA.

(3) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the off-tab voltage between TP2 (BOT) on the EOT/BOT Amplifier PCBA and TP17 (0v) on the Servo and Power Supply PCBA.

(4) Acceptable Limits (Off-tab)

- + 3.50v minimum
- + 4.50v maximum

(5) Compare the voltages obtained in Steps (2) and (3). Voltages must fall between the acceptable limits and the difference between TP1 (EOT) and TP2 (BOT) voltages must be less than 0.40v.

(6) Manually position the tape until the reflective BOT tab is located under the photosensor.

(7) Measure and note the on-tab differential voltage between TP1 and TP2. This voltage must be greater than 2.75v.

(8) Advance tape until the EOT tab is positioned under the photosensor.

(9) Measure and note the on-tab differential voltage between TP1 and TP2.

(10) Acceptable Limits (On-tab)

- On-tab voltages measured in Step (9) must be greater than 2.75v.

6.6.6.3 Adjustment Procedure (Assembly 101949)

When the acceptable limits are exceeded, or the off-tab voltage difference compared in Paragraph 6.6.6.2, Step (5), is greater than 0.40v the following adjustments are performed.

(1) Verify that the adjusting screws of variable resistors R2 and R10 located on the Servo and Power Supply PCBA are turned fully clockwise.

(2) Position the tape so that the EOT and BOT reflective tabs are clear of the photosensor area.

(3) Adjust variable resistor R3 on the EOT/BOT Amplifier PCBA to + 4.0v as observed at TP1.

(4) Adjust variable resistor R9 on the EOT/BOT Amplifier PCBA to + 4v as observed at TP2.

(5) Interaction between R3 and R9 may cause a voltage differential to exist between TP1 and TP2. Verify that voltage at TP1 is + 4.0v. Repeat Steps (3) and (4) as required.

(6) Position the tape so that the EOT reflective tab is located under the photosensor.

(7) Measure the on-tab differential voltage between TP1 and TP2. This voltage must be greater than 2.75v. If the voltage is less than 2.75v, the sensor and/or amplifier should be replaced.

(8) Depress and release the REWIND control; tape will rewind to the BOT, enter a load sequence, and stop.

(9) Measure the on-tab differential voltage between TP1 and TP2. This voltage must be greater than 2.75v. If the voltage is less than 2.75v, the sensor and/or amplifier should be replaced.

6.6.6.4 Related Adjustments (Assembly 101949)

- None.

6.6.7 BOT AMPLIFIER

On transports not equipped with an EOT/BOT Amplifier PCBA, circuitry connected to J13 on the Servo and Power Supply PCBA is utilized as the BOT amplifier. The following test and adjustment procedure is used.

NOTE

The +5v and —5v regulator voltages must be checked and adjusted prior to adjusting the BOT amplifier system. Measurements and adjustments should be made at room temperature.

6.6.7.1 Test Configuration

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlock and tension the tape.

(4) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.7.2 Test Procedure

(1) Manually position the BOT reflective tab clear of the photosensor area.

(2) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the off-tab voltage between TP4 and TP17 (0v) on the Servo and Power Supply PCBA.

(3) Manually position tape so that the BOT reflective tab is positioned under the photosensor.

(4) Using a Fairchild 7050 (or equivalent) measure and note the on-tab voltage between TP4 and TP17 (0v) on the Servo and Power Supply PCBA.

(5) Acceptable Limits

- ☐ On-tab
  - +0.9v maximum
- ☐ Off-tab
  - +3.0v minimum

6.6.7.3 Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are performed.

(1) Position the BOT reflective tab under the photosensor.

(2) Adjust variable resistor R2 to obtain an on-tab voltage of +0.85v as observed at TP4.

(3) Position the BOT reflective tab clear of the photosensor.

(4) Check TP4 to ensure that the off-tab voltage is +3.0v minimum.

6.6.7.4 Related Adjustments

- None.

6.6.8 EOT AMPLIFIER

On transports not equipped with an EOT/BOT Amplifier PCBA, circuitry connected to J13 on the Servo and Power Supply PCBA is used as the EOT amplifier. The following test and adjustment procedure is used.

NOTE

The +5v and —5v regulator voltages must be checked and adjusted prior to adjusting the EOT amplifier system. Measurements and adjustments should be made at room temperature.

6.6.8.1 Test Configuration

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlock and tension the tape.

(4) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.8.2 Test Procedure

(1) Manually position the EOT reflective tab clear of the photosensor area.

(2) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the off-tab voltage between TP6 and TP17 (0v) on the Servo and Power Supply PCBA.

(3) Manually position the EOT reflective tab under the photosensor.

(4) Using a Fairchild 7050 (or equivalent) measure and note the on-tab voltage between TP6 and TP17 on the Servo and Power Supply PCBA.

(5) Acceptable Limits

- ☐ On-tab
  - +0.3v maximum
- ☐ Off-tab
  - +2.8v minimum

6.6.8.3 Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are made.

(1) Position the EOT reflective tab under the photosensor.

(2) Adjust variable resistor R10 to obtain an on-tab voltage of +0.2v as observed at TP6.

(3) Position the EOT reflective tab clear of the photosensor.

(4) Check TP6 to ensure that the off-tab voltage is +2.8v minimum.

6.6.8.4 Related Adjustments

- None

6.6.9 RAMP TIMING

The four tape acceleration and deceleration ramps (Forward and Reverse, Start and Stop) are controlled by a single potentiometer adjustment located on the Tape Control PCBA. This adjustment controls the start/stop time, and is dependent upon the tape speed.

6.6.9 RAMP TIMING

The four tape acceleration and deceleration ramps (Forward and Reverse, Start and Stop) are controlled by a single potentiometer adjustment located on the Tape Control PCBA. This adjustment controls the start/stop time, and is dependent upon the tape speed.

The ramp adjustment time is chosen to ensure that the correct start/stop distance is correlated to the specified start/stop time.

NOTE

The +5v and —5v regulator voltages must be checked and adjusted prior to adjusting Ramp Timing. Measurements and adjustments should be made at room temperature.

6.6.9.1 Test Configuration

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.9.2 Test Procedure

The customer's computer or PERTEC's Hand Held Tape Exerciser may be used in lieu of Step (8) of this procedure.

(1) Connect a signal probe of a Tektronix Model 561 (or equivalent) oscilloscope to TP5 on the Tape Control PCBA.

(2) Connect the ground connection of the oscilloscope probe to TP17 (0v) on the Tape Control PCBA.

(3) Apply a 5 Hz symmetrical square wave with a 3v amplitude (+3.0v to 0v) to the interface line ISFC (J101 pin C or TP14).

(4) Trigger the oscilloscope externally on the negative-going edge of the square wave input.

(5) Adjust the oscilloscope variable vertical (volt/div) control to display 0 to 100 percent of the ramp waveform over four large divisions of the oscilloscope graticule.

(6) Observe that the ramp adjustment time intersects 90 percent of the ramp amplitude (18 small divisions of oscilloscope graticule). Figure 6-1 illustrates ramp levels and timing.

NOTE

For reverse operation the ramp is a negative-going waveform.

(7) Acceptable Limits (90 percent of actual speed)

- ☐ 45 ips transports
  - 7.3 msec maximum
  - 6.7 msec minimum
- ☐ 37.5 ips transports
  - 8.6 msec maximum
  - 7.8 msec minimum

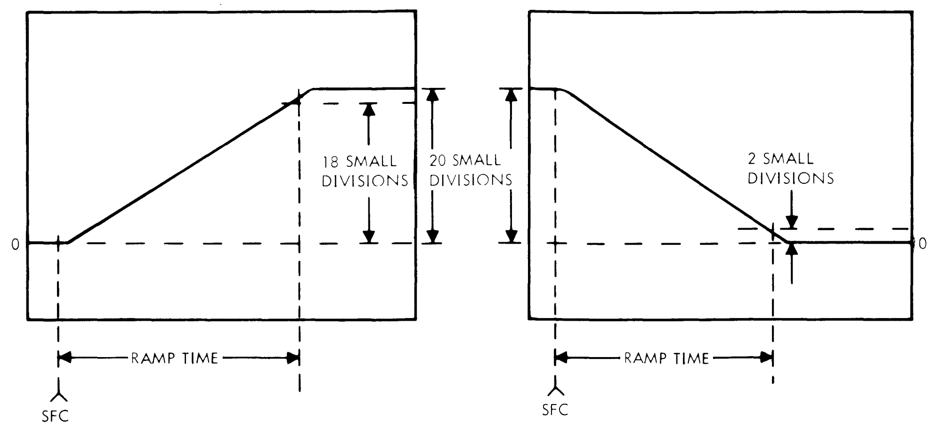


Figure 6-1. Ramp Levels and Timing

- ☐ 25 ips transports
  - 13.3 msec maximum
  - 12.3 msec minimum
- ☐ 22.5 ips transports
  - 14.8 msec maximum
  - 13.6 msec minimum
- ☐ 18.75 ips transports
  - 17.9 msec maximum
  - 16.5 msec minimum
- ☐ 12.5 ips transports
  - 27.4 msec maximum
  - 25.2 msec minimum

(8) Remove the square wave input from J101 pin C (ISFC) and apply the square wave input to ISRC line (J101 pin E or TP13).

(9) With the oscilloscope adjusted as specified in Step (5) observe that the reverse ramp timing is within the limits specified in Step (7).

6.6.9.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed. It should be noted that the customer's computer or PERTEC's Hand Held Tape Exerciser may be used in lieu of Step (8) of this procedure.

(1) Establish test configuration described in Paragraph 6.6.9.1.

(2) Perform test procedure described in Paragraph 6.6.9.2 Steps (1) through (5).

(3) Adjust variable resistor R915 on the Tape Control PCBA to obtain ramp adjustment time as follows.

NOTE

The specified time results of oscilloscope display are illustrated in Figure 6-1. The ramp adjustment time intersects 90 percent of ramp amplitude when accelerating and 10 percent of ramp amplitude when decelerating.

- ☐ 45 ips transports
  - 7.0 msec
- ☐ 37.5 ips transports
  - 8.2 msec
- ☐ 25 ips transports
  - 12.8 msec
- ☐ 22.5 ips transports
  - 14.2 msec
- ☐ 18.75 ips transports
  - 17.2 msec
- ☐ 12.5 ips transports
  - 26.3 msec

(4) Remove the square wave input from ISFC line (J101 pin C) and apply the square wave input to interface line ISRC (J101 pin E or TP13).

(5) Observe oscilloscope display of reverse ramp and re-adjust R915 to obtain ramp time as specified in Step (3).

6.6.9.4 Related Adjustments

- None.

6.6.10 CAPSTAN SERVO OFFSET

The Capstan Servo Offset potentiometer R143 is located on the Servo and Power Supply A PCBA and should be checked and adjusted prior to adjusting tape speed.

NOTE

The 5v regulators must be checked and adjusted, if necessary, prior to adjusting the Capstan Servo Offset potentiometer.

6.6.10.1 Test Configuration

(1) Apply power to the transport.

(2) Load a reel of tape on the transport.

(3) Depress and release the LOAD control twice to establish interlocks and tension tape, and to advance tape to the Load Point.

6.6.10.2 Test Procedure

(1) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the voltage between TP5 and TP19 on the Servo and Power Supply A PCBA. Measured voltage is the output of the capstan motor amplifier.

(2) Acceptable limits:

- +0.20v maximum
- —0.20v minimum

6.6.10.3 Adjustment Procedure

When the acceptable limits are exceeded, perform the following adjustment.

(1) Establish the test configuration described in Paragraph 6.6.10.1.

(2) Using a Fairchild DVM Model 7050 (or equivalent) measure the voltage between TP5 and TP19 on the Servo and Power Supply A PCBA.

(3) Adjust variable resistor R143 to obtain 0v, nominal.

(4) Verify voltage between TP21 and TP19 is —0.3v to +0.3v.

6.6.10.4 Related Adjustments

The Tape Speed and Read Amplifier Gain must be checked and adjusted after adjustments are made to the Capstan Servo Offset.

6.6.11 TAPE SPEED

Only the Synchronous Forward speed is adjustable; the Synchronous Reverse function utilizes the same voltage reference as Synchronous Forward and is not independently adjustable.

NOTE

The +5v and —5v regulator voltages and capstan servo offset must be checked and adjusted prior to adjusting tape speed. Measurements and adjustments should be made at room temperature.

Two methods of tape speed adjustments are given. Paragraphs 6.6.11.1 through 6.6.11.4 describe the optical encoder method; Paragraphs 6.6.11.5 through 6.6.11.9 describe the strobe disk method.

6.6.11.1 Tape Speed (Optical Encoder Adjustment)

Table 6-3 lists the nominal optical encoder counter frequency readings to which the 6000 Series transports are adjusted.

Tape speed may be calculated from the following formula used in conjunction with the specified counter timer.

$$V \text{ ips} = \text{Counter Frequency (Hz)} \times \frac{C}{500} \text{ inches}$$

where

C = Capstan Circumference

NOTE

Capstan circumference for 6000 Series transports is 5.00 inches.

Table 6-3

Counter Frequency Readings

Tape Speed	Counter Frequency (Hz)
45.0	4500
37.5	3750
25.0	2500
22.5	2250
18.75	1875
12.5	1250

6.6.11.2 Test Configuration (Optical Encoder Method)

(1) Couple an Optical Encoder, PERTEC Part No. 512-1100, to the front of the capstan shaft. Five volts dc must be applied to the optical encoder lamp input (pins 1 and 2). This voltage can be obtained between TP19 (—5v) and TP17 (0v) on the Tape Control PCBA.

(2) Load a reel of tape on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD control to establish interlocks and tension tape.

(5) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.11.3 Test Procedure (Optical Encoder Method)

(1) Connect input probes of Counter Timer Monsanto Model 100B (or equivalent) to pins 6 and 7 of the Optical Encoder.

(2) Depress and release the FORWARD control; tape will move in the forward direction.

(3) Adjust the sample interval of the counter timer to monitor the encoder output over a 1-second interval.

(4) Acceptable Limits

- ☐ 12.5 ips
  - 1262 Hz maximum
  - 1237 Hz minimum
- ☐ 18.75 ips
  - 1894 Hz maximum
  - 1856 Hz minimum
- ☐ 22.5 ips
  - 2272 Hz maximum
  - 2227 Hz minimum
- ☐ 25.0 ips
  - 2525 Hz maximum
  - 2475 Hz minimum
- ☐ 37.5 ips
  - 3787 Hz maximum
  - 3713 Hz minimum
- ☐ 45.0 ips
  - 4545 Hz maximum
  - 4455 Hz minimum

(5) Depress and release the FORWARD control; tape will decelerate to stop. Depress and release the REVERSE control; tape will move in the reverse direction.

(6) With the counter timer connected as specified in Step (1) monitor the output of the optical encoder.

(7) The reverse tape speed, as monitored with the counter timer, must be within the following limits.

- ☐ 12.5 ips
  - 1288 Hz maximum
  - 1212 Hz minimum
- ☐ 18.75 ips
  - 1931 Hz maximum
  - 1819 Hz minimum
- ☐ 22.5 ips
  - 2318 Hz maximum
  - 2182 Hz minimum
- ☐ 25.0 ips
  - 2575 Hz maximum
  - 2425 Hz minimum
- ☐ 37.5 ips
  - 3863 Hz maximum
  - 3637 Hz minimum
- ☐ 45.0 ips
  - 4635 Hz maximum
  - 4365 Hz minimum

6.6.11.4 Adjustment Procedure (Optical Encoder Method)

When the forward or reverse tape speeds exceed the specified limits the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.6.11.2.

(2) Perform the test procedure described in Paragraph 6.6.11.3, Steps (1) through (3).

(3) Depress the FORWARD control; tape will move in the forward direction.

(4) Adjust the variable resistor R29 on the Tape Control PCBA for the following counter timer values.

- ☐ 45 ips transports
  - 4500 Hz
- ☐ 37.5 ips transports
  - 3750 Hz
- ☐ 25.0 ips transports
  - 2500 Hz
- ☐ 22.5 ips transports
  - 2250 Hz
- ☐ 18.75 ips transports
  - 1875 Hz
- ☐ 12.5 ips transports
  - 1250 Hz

(5) Monitor the counter timer to ensure that the reverse speed is within the acceptable limits established in Paragraph 6.6.11.3, Step (7). Repeat Steps (2) through (5) as required.

6.6.11.5 Tape Speed (Strobe Disk Adjustment)

The capstan mounted strobe disk may be used when making fine adjustments to the tape speed on 6000 Series tape transports.

Tape speed adjustments made using the strobe disk are accomplished by illuminating the capstan hub from a fluorescent light source and adjusting the capstan servo until the disk image, created by the pulsating light source, becomes stationary. Table 6-4 lists the available disks, synchronous tape speeds, and light source frequencies.

Some strobe disks have two or three concentric sets of strobe markings on each disk. The following rules apply to disks marked with multiple sets of strobe markings.

(1) Part No. 101744-02 (12.5/25 ips). The outer ring is used when the fluorescent light source is 60 Hz. The inner ring is used when the fluorescent light source is 50 Hz.

(2) Part No. 101744-03 (18.75/37.5 ips). There are three sets of strobe markings on this disk. The outer ring is used when checking and adjusting synchronous tape speeds of 18.75 or 37.5 ips from a 60-Hz fluorescent light source.

The middle ring is used at a tape speed of 37.5 ips and from a 50 Hz light source. The inner ring is used at a tape speed of 18.75 ips from a 50 Hz light source.

(3) Part No. 101744-04 (20/40 ips). The outer ring is used when the fluorescent light is from a 60 Hz source. The inner ring is used when the fluorescent light source is from 50 Hz.

(4) Part No. 101744-05 (22.5/45 ips). The outer ring of strobe markings is used when checking and adjusting a tape speed of 45 ips from a 60 Hz fluorescent light source. The middle ring is used at a tape speed of 22.5 ips from a 60 Hz light source. The inner ring is used at a tape speed of 22.5 ips from a 50 Hz light source.

(5) Part No. 101744-07 (30 ips). The outer ring is used when the fluorescent light source is 60 Hz. The inner ring is used when the fluorescent light source is 50 Hz.

The use of the capstan-mounted strobe disk should be limited to fine tape adjustments of the synchronous tape speed. When it is necessary to make gross speed adjustments (e.g., when replacing a Servo and Power Supply PCBA) refer to the test and adjustment procedures described in Paragraphs 6.6.11.1 through 6.6.11.4.

Table 6-4

Strobe Disks

PERTEC Part No.	Tape Speed (ips)	Light Source Frequency (Hz)
101744-02	12.5/25	60/50
101744-03	18.75/37.5	60/50
101744-04	20/40	60/50
101744-05	22.5/45	60/50
101744-06	24	60
101744-07	30	60/50

6.6.11.6 Test Configuration (Strobe Disk Method)

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

(5) Illuminate the capstan-mounted strobe disk with a fluorescent light source at the appropriate frequency.

6.6.11.7 Test Procedure (Strobe Disk Method)

(1) Establish the test configuration described in the foregoing paragraph.

(2) Depress and release the FORWARD tape control; tape will move in the forward direction.

(3) Observe the appropriate strobe disk image; the image should appear stationary.

(4) On dual speed transports, Steps (2) and (3) must be repeated at the second speed.

6.6.11.8 Adjustment Procedure (Strobe Disk Method)

(1) Establish the test configuration previously described.

(2) Adjust potentiometer R29 on the Tape Control PCBA until the strobe disk image appears stationary for the appropriate tape speed.

6.6.12 REWIND SPEED

The rewind speed should be between the following limits.

- 135 ips minimum
- 165 ips maximum

NOTE

The +5v and —5v regulator voltages and capstan servo offset must be checked and adjusted prior to adjusting the speed. Measurements and adjustments should be made at room temperature.

6.6.12.1 Test Configuration

(1) Couple an Optical Encoder, PERTEC Part No. 512-1100, to the front of the capstan shaft. Five volts dc must be applied to the Optical Encoder lamp inputs (pins 1 and 2). This voltage can be obtained between TP19 (—5v) and TP17 (0v) on the Tape Control PCBA.

(2) Load a reel of tape on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD control to establish interlocks and tension the tape.

(5) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.12.2 Test Procedure

(1) Connect input probes of a Counter Timer, Monsanto Model 100B (or equivalent), to pins 6 and 7 of the Optical Encoder.

(2) With a full reel of tape on the take-up reel, depress and release the REWIND control.

(3) Adjust the sample interval of the counter timer to monitor the encoder output over a one-second interval.

(4) Acceptable Limits

- 16,000 Hz maximum
- 14,000 Hz minimum

6.6.12.3 Adjustment Procedure

(1) Establish the test configuration described in Paragraph 6.6.12.1.

(2) Perform the test procedure described in Paragraph 6.6.12.2.

(3) Adjust variable resistor R13 on Servo and Power Supply A, or R14 on Servo and Power Supply B, to obtain a counter timer value of

- 15,000 Hz — this corresponds to 150 ips rewind speed.

6.6.12.4 Related Adjustments

- None

6.6.13 READ AMPLIFIER GAIN (T6X40)

The gain of each of the read amplifiers located on the Data PCBA is independently adjustable.

NOTE

The Tape Speed must be checked and adjusted prior to adjusting the Read Amplifier Gain.

Read amplifier gain may be determined by reading (in the Read Only mode) an all-ones tape which was recorded on the transport. Paragraph 6.6.15 details a method for generating an all-ones tape.

6.6.13.1 Test Configuration

(1) Clean the head assembly and tape path as described in Paragraph 6.4.

(2) Load a pre-recorded all-ones tape on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD control to establish interlocks and tension tape.

(5) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.13.2 Test Procedure

(1) Depress and release the FORWARD control; tape will move forward at the specified velocity.

(2) Using the signal probe of an oscilloscope, Tektronix 561 (or equivalent), measure and record the peak-to-peak amplitude of the read amplifier waveforms viewed at

TP103 through TP903 on Data E9 or E19 PCBA, or TP103 through TP703 on Data E7 or E17 PCBA.

NOTE

Oscilloscope vertical sensitivity should be set to display 2v per division.

(3) Acceptable limits (peak-to-peak when utilizing an all-ones tape generated on the transport):

- 11.50v maximum
- 9.20v minimum

6.6.13.3 Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.6.13.1.

(2) Depress and release the FORWARD control.

(3) Using the signal probe of an oscilloscope, observe TP103 through TP903 on the Data E9 or E19 PCBA, or TP103 through TP703 on the Data E7 or E17 PCBA. Adjust variable resistors R112 through R912 associated with test points to 10.5v peak-to-peak.

6.6.13.4 Related Adjustments

- None

6.6.14 READ AMPLIFIER GAIN (T6X60)

The gain of each of the read amplifiers located on the Data PCBA is independently adjustable.

NOTE

The Tape Speed must be checked and adjusted prior to adjusting the Read Amplifier Gain.

Read amplifier gain may be determined by reading (in the Read Only mode) an all-ones tape which was recorded on the transport. Paragraph 6.16.4 details a method for generating an all-ones tape. A quality tape such as 3M777 should be utilized for this purpose.

6.6.14.1 Test Configuration

(1) Clean the head assembly and tape path as described in Paragraph 6.4.

(2) Load a pre-recorded all-ones tape on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD control to establish interlocks and tension tape.

(5) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.14.2 Test Procedure

(1) Connect TP8 to ground; tape will move forward at the specified velocity.

(2) Using the signal probe of an oscilloscope, Tektronix 561 (or equivalent), measure and record the peak-to-peak amplitude of the read amplifier waveforms viewed at TP103 through TP903 on the Data D or D1 PCBA.

NOTE

Oscilloscope vertical sensitivity should be set to display 2v per division.

(3) Acceptable Limits — peak-to-peak when utilizing an all-ones tape generated on the transport.
   - 13.50v maximum
   - 9.50v minimum

6.6.14.3 Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.6.14.1.

(2) Connect TP8 to ground.

(3) Using the signal probe of an oscilloscope, observe TP103 through TP903 on the Data PCBA. Adjust R111 through R911 (Data D), or R117 through R917 (Data D1) associated with test points to 12v peak-to-peak.

6.6.14.4 Related Adjustments

- None

6.6.15 GENERATION OF ALL-ONES TAPE

An all-ones tape may be generated using the customer's computer, the PERTEC Hand Held Tape Exerciser, or may be generated as follows.

(1) Ensure that the head assembly and tape path are clean.

(2) Load a good quality work tape on the transport.

(3) Bring the transport to Load Point as described in Paragraph 6.6.3.1.

(4) Apply a ground to interface line ISWS (J101 pin K).

(5) Apply a ground to interface line ISFC (J101 pin C).

(6) Apply a ground to interface lines IWDP — IWD7 (J102 pins L, M, N, P, R, S, T, U, and V).

(7) Apply negative-going pulses (+3v to 0v) of 2 μsec duration at the specified transfer rate to interface line IWDS (J102 pin A).

(8) Maintain the transport in this record mode for approximately 3 minutes.

(9) Remove the signal source from interface line IWDS (J102 pin A).

(10) Remove the ground from interface lines ISWS and ISFC (J101 pin K and pin C, respectively.

(11) Depress and release the REWIND control; tape will rewind to the Load Point and stop.

In considering the overall gain of the read system, it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape, i.e., new or used.

The read amplifier output should be adjusted as detailed in Paragraph 6.6.13.3 for T6X40 transports, or Paragraph 6.6.14.3 for T6X60 transports. A read amplifier gain adjusted too high will result in amplifier saturation; gain set too low will increase the susceptibility to data errors due to dropouts.

6.6.16 READ STATICISER DENSITY ADJUSTMENT (T6X40)

The duration of the read character gate is adjusted by means of variable resistors located on the Data PCBA. Nominally, the duration of the character gate is one-half of the character time.

It is important to note that only one density (800 cpi) is relevant to the 9-track PCBA (Data E9 or E19); dual density operation can be selected on the 7-track PCBA (Data E7 or E17) through use of the HI DEN manual control, or remotely through use of optional IDDS interface line.

There are three combinations of two densities available for 7-track: 800/556, 800/200, and 556/200 cpi. The particular combination in any transport will depend upon the character gate adjustments on the PCBA.

NOTE

Tape Speed and Read Amplifier Gain must be checked and adjusted prior to adjusting the Read Staticiser Density.

6.6.16.1 Test Configuration

(1) Load a reel of tape on the transport.

NOTE

An all-ones tape, recorded at the lower of the two densities, should be utilized. Refer to Paragraph 6.6.15 for details on generating an all-ones tape.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension tape.

(4) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.16.2 Test Procedure

The customer's computer or PERTEC's Hand Held Tape Exerciser may be used in lieu of Steps (1), (2), and (3) of this procedure.

(1) Apply a ground to J101 pin J (ISLT).

(2) Place the transport in the On-Line mode.

(3) Apply a ground to J101 pin C (ISFC); tape will move forward at the specified velocity.

(4) Using the signal probe of an oscilloscope, Tektronix 561 (or equivalent), measure and note the duration of the waveform observed at TP11 on Data E7 or E9, or TP9 on Data E17 or E19.

NOTE

The oscilloscope should be set to trigger on the positive-going edge of the observed waveform.

(5) Calculate the ideal character gate duration using the following formula.

$$t\ (\mu sec) = \frac{10^6}{2\ DV} = \text{one-half character time}$$

where

D = density in cpi (recorded tape)

V = tape speed in ips

(6) Acceptable limits (given for 25 ips only; for other speeds, see Step (5) above and calculate the limits based on ±5% of nominal).

- ☐ 800 cpi density, 25 ips, for Data E7, E17, E9 and E19 PCBAs
  - 26.2 μsec maximum
  - 23.8 μsec minimum
- ☐ 556 cpi density, 25 ips, for Data E7 and E17 PCBAs
  - 37.8 μsec maximum
  - 34.2 μsec minimum
- ☐ 200 cpi density, 25 ips, for Data E7 and E17 PCBAs
  - 105.0 μsec maximum
  - 95.0 μsec minimum

6.6.16.3 Adjustment Procedure (7-track Transports)

When the acceptable limits are exceeded the following procedure is performed. It should be noted that the customer's computer or PERTEC's Hand Held Tape Exerciser may be used in lieu of Steps (2), (3), and (4) of this procedure.

(1) Establish the test configuration described in Paragraph 6.6.16.1.

(2) Apply a ground to J101 pin J (ISLT).

(3) Place the transport in the On-Line mode.

(4) Apply a ground to J101 pin C (ISFC); tape will move forward at the specified velocity.

(5) Select the lower of the two packing densities (HI DEN control extinguished) on versions equipped for dual-density operation.

(6) Connect a signal probe of a Tektronix 561 oscilloscope (or equivalent) to TP11 on Data E7, or TP9 on Data E17.

(7) Connect the oscilloscope reference probe to TP12 on Data E7, or TP3 on Data E17.

(8) Adjust variable resistor R32 on Data E7 or E17 to display a character gate waveform according to speed and density as follows (see Paragraph 6.6.16.2 for other speeds).

- ☐ 556 cpi density, 25 ips
  - 36 μsec
- ☐ 200 cpi density, 25 ips
  - 100 μsec

(9) Select the higher of the two densities (HI DEN control illuminated) on versions equipped for dual density operation.

(10) Adjust variable resistor R27 on Data E7 or E17 to display a character gate waveform according to speed as follows (see Paragraph 6.6.16.2 for other speeds).

- ☐ 800 cpi density, 25 ips
  - 25 μsec
- ☐ 556 cpi density, 25 ips
  - 36 μsec

NOTE

The foregoing adjustments must be performed in the order specified.

6.6.16.4 Adjustment Procedure (9-track transports)

When the acceptable limits are exceeded, the following adjustments are performed. It should be noted that the customer's computer or PERTEC's Hand Held Tape Exerciser may be used in lieu of Steps (2), (3), and (4) of this procedure.

(1) Establish the test configuration described in Paragraph 6.6.16.1.

(2) Apply a ground to J101 pin J (ISLT).

(3) Place the transport in the On-Line mode.

(4) Apply a ground to J101 pin C (ISFC); tape will move forward at the specified velocity.

(5) Connect the oscilloscope signal probe to TP11 on Data E9, or TP9 on Data E19.

(6) Connect the oscilloscope reference probe to TP12 on Data E9, or TP3 on Data E19.

(7) Adjust R32 on the Data E9 or E19 to display the positive-going portion of the character gate waveform as follows for 800 cpi at 25 ips (see Paragraph 6.6.16.2 for other speeds).

- 25 μsec

6.6.16.5 Related Adjustments

- None

6.6.17 READ STATICISER DENSITY ADJUSTMENT (T6X60)

The duration of the read character gate is adjusted by means of variable resistors located on the Data PCBA. Nominally, the duration of the character gate is one-half of the character time.

It is important to note that only one density (800 cpi) is relevant to the 9-track PCBA, while dual density operation can be selected on the 7-track PCBA through use of the HI DEN manual control, or remotely through use of the optional IDDS interface line.

There are three combinations of two densities available for 7-track: 800/556, 800/200, and 556/200 cpi. The particular combination in any transport will depend upon the version of the PCBA.

NOTE

Tape Speed and Read Amplifier Gain must be checked and adjusted prior to adjusting the Staticiser Density.

6.6.17.1 Test Configuration

(1) Load a reel of tape with a Write Enable ring on the transport.

NOTE

An all-ones tape, recorded at the lower of the two densities, should be utilized. Refer to Paragraph 6.6.15 for details on generating an all-ones tape.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension tape.

(4) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

6.6.17.2 Test Procedure

The customer's computer or PERTEC's Hand Held Tape Exerciser may be used in lieu of Steps (1), (2), and (3) of this procedure.

(1) Apply a ground to J101 pin J (ISLT).

(2) Place the transport in the On-Line mode.

(3) Apply a ground to J101 pin C (ISFC); tape will move forward at the specified velocity.

(4) Using the signal probe of an oscilloscope, Tektronix 561 (or equivalent), measure and note the duration of the waveform observed at TP10 on Data D, or TP11 on Data D1.

NOTE

The oscilloscope should be set to trigger on the positive-going edge of the observed waveform.

(5) Calculate the ideal character gate duration using the following formula.

$$t\ (\mu\text{sec}) = \frac{10^6}{2\ DV} = \text{one-half character time}$$

where

D = density in cpi (recorded tape)

V = tape speed in ips

(6) Acceptable limits (given for 25 ips only; for other tape speeds, see Step (3) above and calculate the limits based on ±5% of nominal).

- ☐ 800 cpi density, 25 ips, for Data D and D1 PCBAs
  - 26.2 μsec maximum
  - 23.8 μsec minimum
- ☐ 556 cpi density, 25 ips, for Data D PCBA
  - 37.8 μsec maximum
  - 34.2 μsec minimum
- ☐ 200 cpi density, 25 ips, for Data D PCBA
  - 105.0 μsec maximum
  - 95.0 μsec minimum

6.6.17.3 Adjustment Procedure (7-track transports)

When the acceptable limits are exceeded the following procedure is performed. It should be noted that the customer's computer or PERTEC's Hand Held Tape Exerciser may be used in lieu of Steps (2), (3), and (4) of this procedure.

(1) Establish the test configuration described in Paragraph 6.6.17.1.

(2) Apply a ground to J101 pin J (ISLT).

(3) Place the transport in the On-Line mode.

(4) Apply a ground to J101 pin C (ISFC); tape will move forward at the specified velocity.

(5) Select the lower of the two packing densities (HI DEN control extinguished) on versions equipped for dual-density operation.

(6) Connect the oscilloscope signal probe to TP10 on the Data D, or to TP11 on the Data D1 PCBA.

(7) Connect the oscilloscope reference probe to TP12 on the Data D, or TP3 on the Data D1 PCBA.

(8) Adjust variable resistor R25 on the Data D, or R36 on the Data D1 PCBA to display a character gate waveform according to speed and density as follows (see Paragraph 6.6.17.2 for other speeds).

- ☐ 556 cpi density, 25 ips
  - 36 μsec
- ☐ 200 cpi density, 25 ips
  - 100 μ sec

(9) Select the higher of the two densities (HI DEN control illuminated) on versions equipped for dual density operation.

(10) Adjust variable resistor R21 on the Data D, or R33 on the Data D1, to display a character gate waveform according to speed as follows (see Paragraph 6.6.17.2 for other speeds).

- ☐ 800 cpi density, 25 ips
  - 25 μsec
- ☐ 556 cpi density, 25 ips
  - 36 μsec

NOTE

The foregoing adjustments must be performed in the order specified.

6.6.17.4 Adjustment Procedure (9-track Transports)

When the acceptable limits are exceeded, the following adjustments are performed. It should be noted that the customer's computer or PERTEC's Hand Held Tape Exerciser may be used in lieu of Steps (2), (3), and (4) of this procedure.

(1) Establish the test configuration described in Paragraph 6.6.17.1.

(2) Apply a ground to J101 pin J (ISLT).

(3) Place the transport in the On-Line mode.

(4) Apply a ground to J101 pin C (ISFC); tape will move forward at the specified velocity.

(5) Connect the oscilloscope signal probe to TP10 on Data D, or TP11 on Data D1 PCBA.

(6) Connect the oscilloscope reference probe to TP12 on the Data D, or TP3 on the Data D1 PCBA.

(7) Adjust R25 and R21 on the Data D, or R36 and R33 on the Data D1, to display the positive-going portion of the character gate waveform as follows for 800 cpi at 25 ips (see Paragraph 6.6.17.2 for other speeds).

- 25 μsec

6.6.17.5 Related Adjustments

- None

6.7 MECHANICAL ADJUSTMENTS

6.7.1 TENSION ARM LIMIT SWITCH

When the tension arm is resting against its backstop the position of the limit switch roller, with respect to the cam, should be as shown in Figure 6-2 (Section A-A). At this time the switch contacts should be open. If the relative positions of the roller and cam are not as illustrated, the following adjustment is performed.

(1) Loosen the cam retaining set-screw.

(2) Rotate the cam on its shaft until the limit switch roller is in the position illustrated in Figure 6-2.

(3) Firmly tighten the cam retaining set-screw.

CAUTION

THE CAM RETAINING SET-SCREW MUST BE TIGHTENED SUFFICIENTLY TO PREVENT ROTATION OF THE CAM WHEN THE TENSION ARM IMPACTS ON ITS BACKSTOP.

The limit switch plate is slotted at one mounting screw and may be rotated about the second screw to facilitate setting the switching point of the limit switch. The plate should be rotated to a position where the limit switch trips with its roller one-half of the distance up the slope from its rest position. The switch should be closed when the roller moves on the cam lobe between the semi-circular cutouts.

Replacement of the limit switch is accomplished as follows.

(1) Unplug the limit switch connector P17 from J17 of the Servo and Power Supply PCBA.

(2) Remove the yellow and green leads from the limit switch connector (P17) using an extractor tool.

(3) Remove the two mounting screws which mount the limit switch to its plate and remove the switch.

(4) Attach the new limit switch to the plate using the two mounting screws removed in Step (3).

(5) Adjust the limit switch position as described in the preceding paragraph.

(6) Tighten the two mounting screws and recheck the position of the limit switch roller.

(7) Connect the limit switch connector (P17) to J17 of the Servo and Power Supply PCBA.

(8) Plug the connector (P14 for take-up reel sensor, P18 for supply reel sensor) into the respective jack on the Servo and Power Supply PCBA.

(9) Perform the relevant adjustment procedure.

6.7.2 TENSION ARM POSITION SENSOR (APPLIES TO SERVO AND POWER SUPPLY A, ASSEMBLY 101021)

There are two tension arm position sensors: one on the take-up tension arm, and the second on the supply arm. Each of the sensors has a 3-pin plug which connects the output of the sensor to the reel servo amplifier on the Servo and Power Supply PCBA.

CAUTION

ENSURE THAT THE 5V REGULATORS, RAMP TIMING, AND TAPE SPEEDS ARE CORRECT AS DETAILED IN PARAGRAPHS 6.6.3 [OR 6.6.4], 6.6.9, AND 6.6.10, RESPECTIVELY, BEFORE ADJUSTING THE TENSION ARM POSITION SENSORS.

6.7.2.1 Preliminary Adjustment (Assembly 101021)

The tension arm photosensors on the supply reel and take-up reel are initially adjusted as follows.

(1) Loosen the No. 10 retaining nut securing the shutter on the tension arm shaft in such a way that the shutter can be rotated by hand.

NOTE

Ensure that there is sufficient friction to prevent the setting from changing when the nut is tightened.

(2) To place the shutter in approximately the correct position, remove tape from the transport and rotate the shutter until moving the tension arm to the middle of its range stops reel motion.

NOTE

The LOAD control must be continuously depressed or the limit switch shorted to facilitate this procedure.

(3) Load a reel of tape on the transport.

(4) Establish an environment which ensures that the tension arm sensors are shielded from high ambient light. Failure to do so could result in a shift in the arm operating region when the unit is rack-mounted.

6.7.2.2 Take-Up Arm Adjustment (Assembly 101021)

When the preliminary adjustments are completed, proceed as follows.

(1) Ensure that the take-up reel is nearly empty.

(2) Place the arm movement measuring tool (PERTEC Part No. 101137) in position against the fixed guide near the top of the arm swing. The words *Top Arm* should be visible on the tool.

(3) Alternately depress the FORWARD and REVERSE controls to cause tape to *shuttle* back and forth.

(4) If Step (3) causes loss of tape tension by moving the supply arm to either switch point of the limit switch, re-tension tape by depressing LOAD. Move the supply arm shutter so that the arm rests in the center of its travel. Adjust R72 on the Servo and Power Supply PCBA 5 turns CW so as to reduce total arm movement. Repeat this step as required.

(5) Note the total arm movement.

(6) Adjust variable resistor R30 on the Servo and Power Supply PCBA until the total arm movement is equal to the distance between the appropriate marks on the tool.

NOTE

The actual arc of movement may not coincide with that specified on the tool because the shutter may not yet be in the correct position.

(7) Re-adjust the shutter position so that the arc of the arm movement and the mark on the tool coincide.

(8) The arm position in Forward and Reverse motion should coincide with the marks on the tool within +0.0, —0.5 inch.

(9) Torque the optical shutter retaining nut to 30 in-lb, taking care that the shutter does not move.

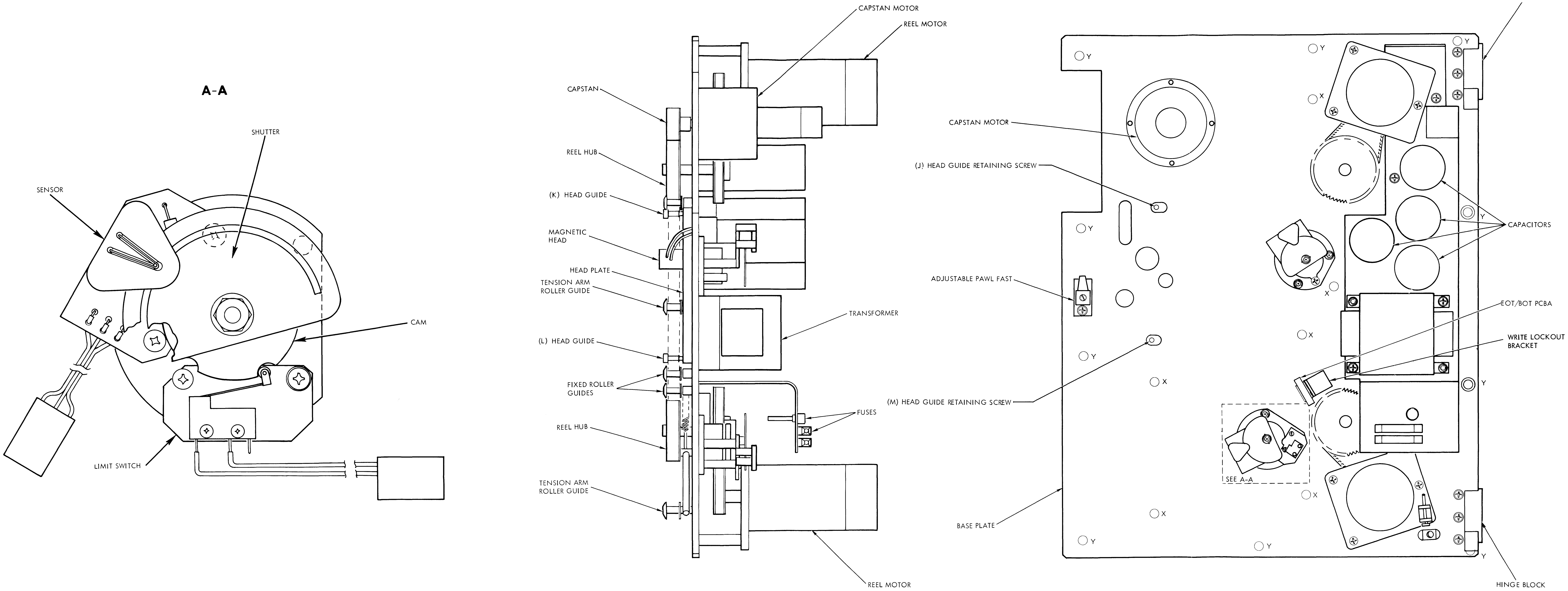


Figure 6-2. Tape Deck Diagram, Rear View

884S

6.7.2.3 Supply Arm Adjustment (Assembly 101021)

When the preliminary adjustments are completed, proceed as follows.

(1) Ensure that the supply reel is nearly empty.

(2) Place the arm movement measuring tool, PERTEC Part No. 101137, in position against the fixed guide near the bottom of the arm stroke. The words *Bottom Arm* should be visible on the tool.

(3) Adjust the shutter, if necessary, so that the supply arm rests in the center of its travel.

(4) Alternately depress the FORWARD and REVERSE controls to cause tape to *shuttle* back and forth.

(5) Note the total arm movement.

(6) Adjust variable resistor R72 on the Servo and Power Supply PCBA until the total arm movement is equal to the distance between the appropriate marks on the tool.

NOTE

The actual arc of movement may not coincide with that specified on the tool because the shutter may not yet be in the correct position.

(7) Re-adjust the shutter position so that the arc of the arm movement and the mark on the tool coincide.

(8) The arm position in forward and reverse motion should coincide with the mark on the tool within +0.0 —0.5 inch.

(9) Torque the optical shutter retaining nut to 30 in-lb, taking care that the shutter does not move.

6.7.3 TENSION ARM POSITION SENSOR (APPLIES TO SERVO AND POWER SUPPLY B, ASSEMBLY 101262)

There are two tension arm position sensors: one on the take-up tension arm, and the second on the supply arm. Each of the sensors has a 3-pin plug which connects the output of the sensor to the reel servo amplifier on the Servo and Power Supply PCBA.

CAUTION

ENSURE THAT THE 5V REGULATORS, RAMP TIMING, AND TAPE SPEEDS ARE CORRECT AS DETAILED IN PARAGRAPHS 6.6.3 [OR 6.6.4], 6.6.9 AND 6.6.10, RESPECTIVELY, BEFORE ADJUSTING THE TENSION ARM POSITION SENSORS.

6.7.3.1 Preliminary Adjustment (Assembly 101262)

The tension arm photosensors on the supply reel and take-up reel are initially adjusted as follows.

(1) Loosen the No. 10 retaining nut securing the shutter on the tension arm shaft in such a way that the shutter can be rotated by hand.

NOTE

Ensure that there is sufficient friction to prevent the setting from changing when the nut is tightened.

(2) To place the shutter in approximately the correct position, remove tape from the

transport and rotate the shutter until moving the tension arm to the middle of its range stops reel motion.

NOTE

The LOAD control must be continuously depressed or the limit switch shorted to facilitate this procedure.

(3) Load a reel of tape on the transport.

(4) Establish an environment which ensures that the tension arm sensors are shielded from high ambient light. Failure to do so could result in a shift in the arm operating region when the unit is rack-mounted.

6.7.3.2 Take-up Arm Adjustment (Assembly 101262)

When the preliminary adjustments are completed, proceed as follows.

(1) Ensure that the take-up reel is nearly empty.

(2) Place the arm movement measuring tool, PERTEC Part No. 101137, in position against the fixed guide near the top of the arm swing. The words *Top Arm* should be visible on the tool.

(3) Move the take-up shutter so that the arm rests approximately in the center of its travel.

(4) Alternately depress the FORWARD and REVERSE controls to cause tape to *shuttle* back and forth.

(5) If Step (4) causes loss of tape tension because the supply arm exceeds its operating range, re-tension tape by depressing LOAD. Adjust R81 on the Servo and Power Supply PCBA 5 turns CCW so as to reduce the total arm movement. Repeat this step as required.

(6) Adjust variable resistor R32 on the Servo and Power Supply PCBA until the extreme arm movement is equal to the distance between the appropriate marks on the tool.

NOTE

The actual arc of movement may not coincide with that specified on the tool because the shutter may not yet be in the correct position.

(7) Re-adjust the shutter position so that the arc of the arm movement and the marks on the tool coincide.

(8) The arm position in the Forward and Reverse motion should coincide with the marks on the tool within +0.0, —0.5 inch.

(9) Torque the optical shutter retaining nut to 30 in-lb, taking care that the shutter does not move.

6.7.3.3 Supply Arm Adjustment (Assembly 101262)

When the preliminary adjustments are completed, proceed as follows.

(1) Ensure that the supply reel is nearly empty.

(2) Place the arm movement measuring tool in position against the fixed guide near the bottom of the arm stroke. The words *Bottom Arm* should be visible on the tool.

(3) Adjust the shutter, if necessary, so that the supply arm rests in the center of its travel.

(4) Alternately depress the FORWARD and REVERSE controls to cause tape to *shuttle* back and forth.

(5) Note the total arm movement.

(6) Adjust variable resistor R81 on the Servo and Power Supply PCBA until the extreme arm movement is equal to the distance between the appropriate marks on the tool.

NOTE

The actual arc of movement may not coincide with that specified on the tool because the shutter may not yet be in the correct position.

(7) Re-adjust the shutter position so that the arc of the arm movement and the mark on the tool coincide.

(8) The arm position in Forward and Reverse motion should coincide with the marks on the tool within +0.0, —0.5 inch.

(9) Torque the optical shutter retaining nut to 30 in-lb, taking care that the shutter does not move.

6.7.4 TENSION ARM SENSOR REPLACEMENT

The tension arm optical sensors are replaced as follows.

(1) Loosen the No. 10 retaining nut which secures the optical shutter to the tension arm.

(2) Rotate the shutter to clear the countersunk screws which retain the tension arm sensor printed circuit board to the deck standoffs.

(3) Remove two retaining screws from the tension arm sensor printed circuit board.

NOTE

Retain the two screws removed in Step [3]*; they will be used to mount the replacement sensor.*

(4) Unplug the connector (P14 for take-up reel sensor, P18 for supply reel sensor) from the Servo and Power Supply PCBA and remove the sensor assembly.

(5) Mount the replacement assembly on the deck standoffs using the two screws which were removed in Step (3).

(6) Plug the connector (P14 for take-up reel sensor, P18 for supply reel sensor), into the respective jack on the Servo and Power Supply PCBA.

(7) Perform the relevant adjustment procedure.

6.7.5 READ SKEW MEASUREMENT AND ADJUSTMENT

Dynamic and static skew can be measured and adjusted by using an 800-cpi master tape (which can be obtained from IBM) and an oscilloscope.

6.7.5.1 Read Skew Measurement

An indication of total read system skew may be obtained by observing the algebraic sum of the peak detectors at TP15 on Data E7 and E9, or TP2 on Data E17 and E19. TP13 is used on the Data D and TP2 is used on the Data D1 to observe this waveform. Figure 6-3 illustrates an example of correctly adjusted skew. This method of determining the system read skew is accomplished as follows.

(1) Set the vertical sensitivity on the oscilloscope to 1.0v/cm.

(2) Set the oscilloscope to trigger on Channel 1, negative slope, alternate mode.

(3) Load an 800-cpi master tape on the transport, bring to BOT, and initiate an SFC by tying the interface input (pin C of J101) to 0v.

(4) Observe the oscilloscope waveform and adjust the horizontal time/division fixed and variable controls to display one complete cycle.

NOTE

With an 800-cpi tape, each cycle represents 1250 μinches. The scope graticule is divided into 10 major divisions, each of which is divided into 5 divisions; therefore

$$\frac{1250\ \mu inch}{50\ divisions} = 25\ \mu inch/division$$

(5) On T6X40 Models, observe that the fall time of the waveform viewed at TP15 on Data E7 and E9, or at TP2 on Data E17 and E19, is less than six small divisions of the oscilloscope graticule, i.e., 150 μinches. This measurement should be taken between the 95- and 5-percent points of the waveform.

On T6X60 Models, observe that the fall time of the waveform viewed at TP13 on Data D, or at TP2 on Data D1, is less than six small divisions of the oscilloscope graticule, i.e., 150 μinches. This measurement should be taken between the 95- and 5-percent points of the waveform.

6.7.5.2 Read Skew Adjustment

To reduce skew to within acceptable limits, the following procedure is performed.

(1) Perform the measurement procedure described in Paragraph 6.7.5.1.

(2) While observing the waveform at the test points called out in Paragraph 6.7.5.1, Step (5), and with tape moving in the forward direction, ease the edge of the tape off the head guide cap toward the spring-loaded washer. This should be done on first one guide, then the other.

NOTE

Moving the tape one- to two-thousandths of an inch from one of the guides will reduce the skew to within the specified range.

(3) Observe the waveform and determine which movement (upper or lower guide) improves the display. If moving the tape off the upper guide improved the display, the lower guide should be shimmed.

NOTE

The shims are burr-free, etched, one-half of a thousandths inch thick berrylium copper.

(4) Remove the SFC by removing the 0v to interface input (pin C of J101).

(5) Remove the head guide retaining screw (accessible from the rear of the deck) and remove the guide.

NOTE

When removing the guide care should be taken not to drop the spring and washer.

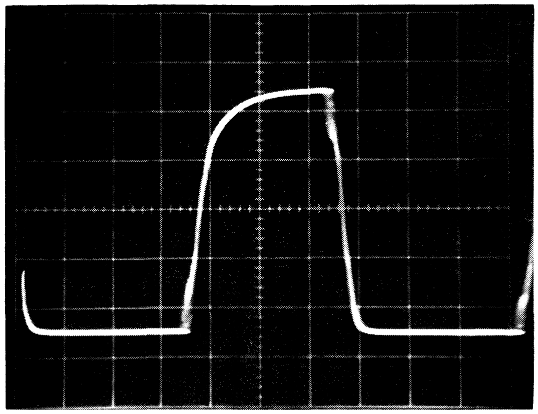


Figure 6-3. Skew Waveform (Typical)

(6) With the oscilloscope set up as described in Paragraph 6.7.5.1, Step (4), observe and note the fall time of the waveform observed at test points called out in Paragraph 6.7.5.1, Step (5).

(7) Since the character spacing at 800 cpi is 1250 μinches, the actual skew can be calculated. The skew correction provided by the addition of one shim (each shim is 500 μinches thick) is 500 ÷ 12 = 42 μinches. The number of shims used must satisfy the following.

- Skew must be reduced to a minimum consistent with the maximum number of shims allowable — the maximum number of shims allowable is four.

Therefore, if, for example, the measured skew is 180 μinches, four shims will yield a skew correction of 168 μinches (i.e., 4 X [500 ÷ 12] = 168 μinches); this satisfies the foregoing.

(8) Insert the required number of shims and replace the head guide.

NOTE

Shim only one head guide.

(9) Recheck skew measurement described in Paragraph 6.7.5.1.

6.7.6 WRITE SKEW MEASUREMENT AND ADJUSTMENT (T6X40 ONLY)

The read skew measurement and adjustment should be accomplished prior to adjustment of the write skew.

6.7.6.1 Write Skew Measurement

Measurement of write skew is accomplished by writing and simultaneously reading an all-ones tape. This is accomplished as follows.

(1) Set the vertical sensitivity of an oscilloscope, Tektronix 561 (or equivalent), to 1.0v/cm and the horizontal range to 5 μsec/cm.

(2) Set the oscilloscope to trigger on Channel 1, negative slope, alternate mode.

(3) Ensure that the head assembly and tape path are clean.

(4) Load a good quality work tape with a write enable ring in place on the transport.

(5) Bring the transport to Load Point.

(6) Place the transport On-Line.

(7) Apply a ground to TP9 on the Tape Control PCBA.

(8) Apply a ground to interface line ISLT (J101 pin J) on the Tape Control PCBA.

(9) Apply a ground to interface line ISFC (J101 pin C) on the Tape Control PCBA.

(10) Apply a ground to interface lines IWDP, IWD0 — IWD7 (J102 pins L, M, N, P, R, S, T, U, and V) on the Data PCBA.

(11) Apply negative-going pulses (+3v to 0v) of 2 μsec duration at the specified transfer rate to interface line IWDS (J102 pin A) on the Data PCBA.

NOTE

Transfer rate = D X V, where D = density in cpi and V = speed in ips; i.e., 20Kc at 800 cpi, 25 ips.

(12) Connect the oscilloscope signal probe to TP15 on Data E7 and E9, or TP2 on Data E17 and E19. Adjust the horizontal time/division variable control to display one complete cycle.

NOTE

With an 800 cpi tape, each cycle represents 1250 μinches. The scope graticule is divided into 10 major divisions, each of which is divided into 5 divisions; therefore

$$\frac{1250\ \mu inch}{50\ divisions} = 25\ \mu inch/division$$

(13) Observe that the fall time of the waveform viewed at TP15 on Data E7 and E9, or TP2 on Data E17 and E19, is less than eight small divisions of the oscilloscope graticule, i.e., 200 μinches. Note that this value includes the effect of gap scatter of the read head. Tape will actually be recorded with less than 150 μinches of skew.

6.7.6.2 Write Skew Adjustment

To reduce write skew to within acceptable limits, the following procedure is performed.

(1) Perform the write skew measurement procedure described in Paragraph 6.7.6.1.

(2) While observing the waveform viewed at TP15 on Data E7 and E9, or TP2 on Data E17 and E19, adjust R18 on the Data PCBA to reduce skew to less than eight small divisions of the oscilloscope graticule, i.e., 200 μinches. (See Paragraph 6.7.6.1, Step (13).)

6.7.7 FLUX GATE ADJUSTMENT (T6X40 ONLY)

Crosstalk can be checked and, if necessary, reduced to within acceptable limits by mechanically positioning the flux gate. The check and adjustment procedure is accomplished as follows.

(1) Load a reel of tape with a write enable ring installed on the transport — do not pass tape over the capstan.

(2) Apply power to the transport.

(3) Bring the transport to Load Point artificially by placing a white card between the tape and photosensor assembly and depressing the LOAD control.

(4) Place the transport On-Line.

(5) Apply a ground to TP9 on the Tape Control PCBA.

(6) Apply a ground to interface line ISLT (J101 pin J) on the Tape Control PCBA.

(7) Apply a ground to interface line ISFC (J101 pin C) on the Tape Control PCBA.

(8) Apply a ground to interface lines IWDP and IWD0 through IWD7 (J102 pins L, M, N, P, S, T, U, and V) on the Data PCBA.

(9) Apply negative-going (+5v to 0v) pulses of 2 μsec duration to the interface line IWDS (J102 pin A) on the Data PCBA. (For the proper repetition rate see Paragraph 6.7.6.1, Step (11).

(10) Using an oscilloscope, Tektronix 561 (or equivalent), observe the waveforms at TP103 through TP903 on the Data E9 and E19, or TP103 through TP703 on the Data E7 or E17.

(11) Observe that the waveforms viewed in Step (10) are approximately sinusoidal with no pronounced peaks. The maximum allowable crosstalk voltage is 1.0v peak-to-peak.

NOTE

If the observed waveforms in Step [10] falls within the limit specified in Step [11], no adjustment should be attempted.

(12) Partially loosen the screws which secure the flux gate assembly. Care should be taken to ensure that the flux gate spring does not move the assembly.

(13) Place a white card (e.g., business card) between the flux gate and the magnetic head and press the flux gate assembly lightly against the head.

(14) One of two flux gates is installed on the transport. Figure **6-4** (A or B) illustrates the correct relationship between the magnetic head and the flux gate.

NOTE

It may be necessary to move or rotate the assembly slightly to achieve the best compromise between all tracks.

(15) Tighten the flux gate assembly screws and repeat Steps (1) through (11).

CAUTION

ENSURE ADEQUATE CLEARANCE BETWEEN THE FLUX GATE AND THE MAGNETIC HEAD [0.005-INCH MIN.]. FAILURE TO ALLOW CORRECT CLEARANCE WILL RESULT IN DAMAGE TO THE HEAD.

6.7.8 HEAD REPLACEMENT

The head may require replacement because of internal faults in the head or cable, or because of wear. The first reason can be established by reading a master tape; the second can be verified by measuring the depth of the wear pattern on the head crown. In those heads which have *guttering* (grooves cut on the crown, each side of the tape path), the head should be replaced when it has worn down to the depth in excess of 0.010-inch. In those heads not having guttering, the head wear should be measured with a brass shim that is ten-thousandths of an inch thick. The shim width should be less than the minimum tape width (0.496-inch). The shim should be placed in the worn portion of the head crown with one side butted against the worn step. When the upper surface of the shim is below the unworn surface of the head crown (i.e., the head has worn to a depth greater than 0.010-inch), the head should be replaced.

To remove the head assembly from the tape deck, proceed as follows.

(1) Remove the head cover.

(2) Disconnect the head cable(s) from connector(s) on the Data PCBA.

(3) Loosen the screws (identified as 'X' and 'Y' in Figure 6-2) that retain the overlay.

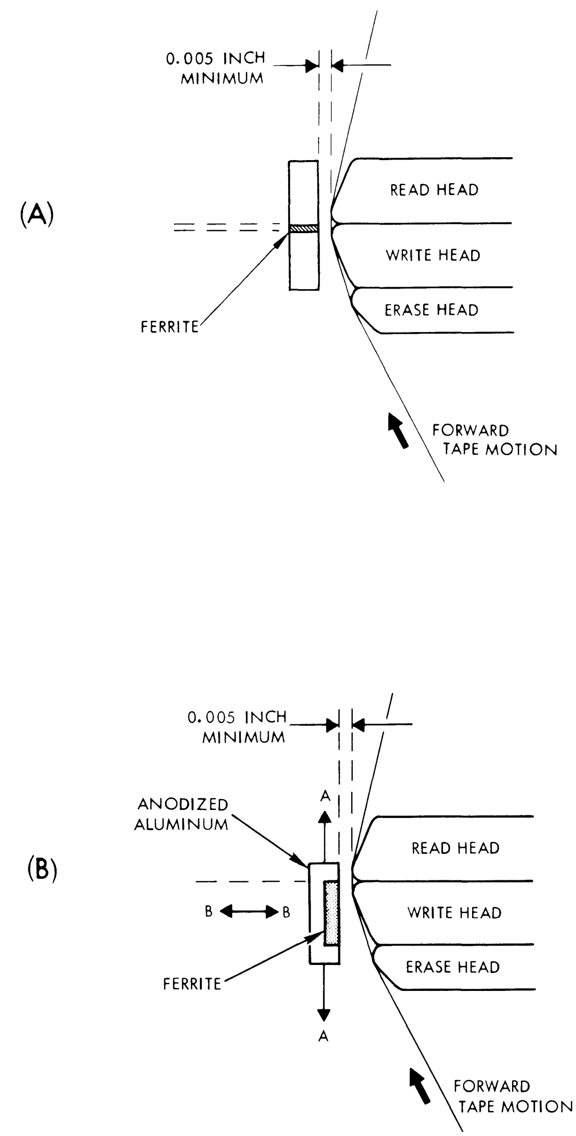


Figure 6-4. Flux Gate Adjustment

(4) Remove the two screws located behind the tape deck that attach the head to the head plate.

(5) Ease the cable(s) through the hole in the deck and, by moving the overlay outward from the deck, make clearance for the connector to pass through the deck and overlay.

(6) Before installing the replacement head, check the mounting surface of the head and head plate for contamination on either surface.

NOTE

The mounting surface must be free of all foreign substances or excessive skew will result.

(7) Pass the head connector and the cables of the replacement head through the cable access hole in the tape deck.

(8) Install the replacement head to the head plate using the screws removed in Step (3).

(9) A T6X40 dual-stack head in place is shown in Figure 6-5; a T6X60 single-stack head in place is shown in Figure 6-6. Adjustment is made by using PERTEC Head Adjustment Tool, Part No. 103259-01.

6.7.8.1 Installation, Head Adjustment Tool

Install the head adjustment tool as follows.

(1) Remove the guide caps from the fixed head guides (refer to Paragraph 6.7.12.1, Step (5).

(2) Remove the photo-tab sensor assembly (refer to Paragraph 6.7.9).

(3) Install the head adjustment tool to the fixed head guides; refer to Figures 6-5 and 6-6. Two, one-half inch long, 4-40 button head screws are required; install one No. 4 flat washer beneath each screw head.

(4) With the head screws and adjustment tool screws just snug, carefully position the head upward via the slotted screw holes in the head plate to a point where the side and crown of the head are in contact with the tool; tighten all screws at this point. Visually check for any gaps at the crown or side of head. If no gaps exist, the head alignment is correct.

(5) Remove the adjustment tool and re-install the guide caps.

(6) Connect the head cable(s) to the relevant connector(s) on the Data PCBA.

(7) Replace the overlay.

6.7.8.2 Operational Test

Perform the following test.

(1) Install an all-ones tape and thread the tape through the tape path to the take-up reel.

(2) Apply power to the transport and bring tape to Load Point to establish operating tape tension.

(3) Ensure that the crown area of the head is perpendicular to, and in contact with, the tensioned tape.

(4) Ensure the tape and tape head are in full contact across the width of the tape.

(5) Place the tape in motion and set all Read Amplifier gains (if required) as described in Paragraph 6.6.12 or 6.6.13.

(6) Replace the all-ones tape with an 800-cpi master tape. Apply power to the transport and bring tape to the Load Point to establish tape tension.

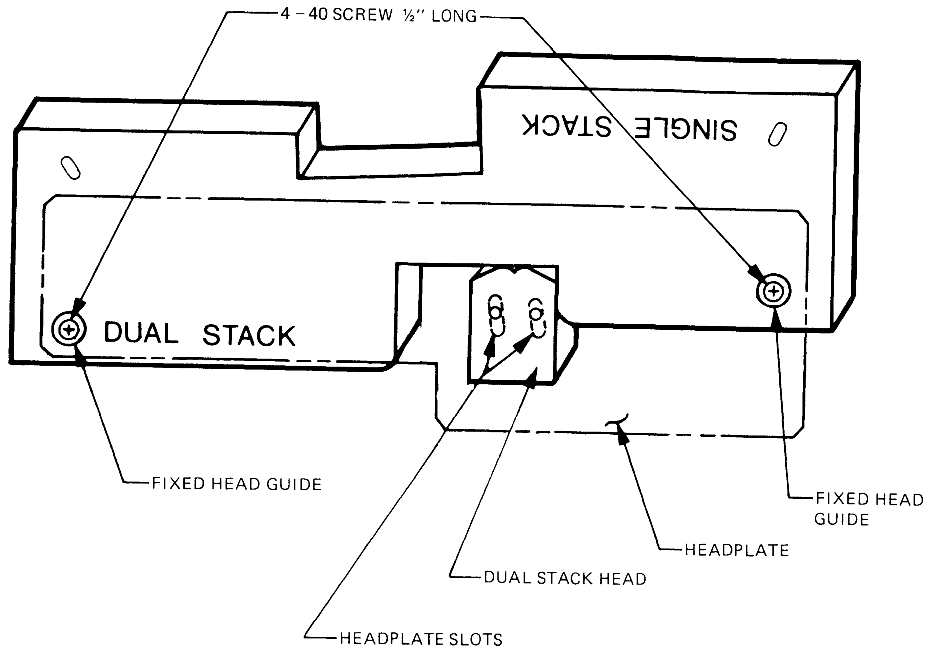


Figure 6-5. T6X40 Head Adjustment Tool

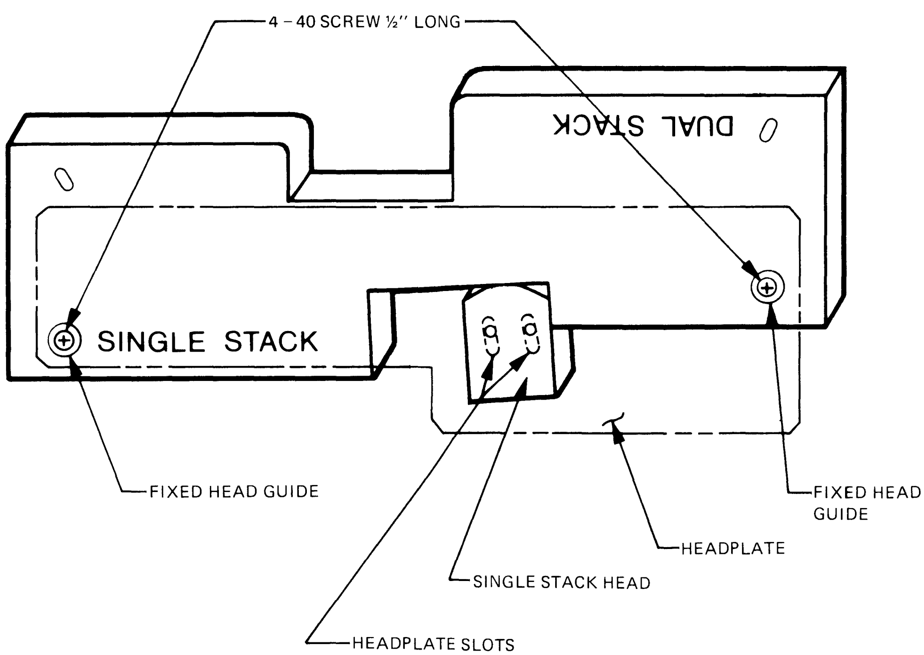


Figure 6-6. T6X60 Head Adjustment Tool

(7) Place tape in motion and observe the skew of all channels.

(8) Make any skew corrections by following the procedures in Paragraphs 6.7.5 and 6.7.6. The output waveform should approach that shown in Figure 6-3.

NOTE

Shim only one head guide.

(9) Rewind tape to the supply reel and remove the reel.

(10) Replace the head cover.

6.7.9 PHOTO-TAB SENSOR REPLACEMENT

Replacement of the photo-tab sensor is accomplished as follows.

(1) Disconnect the cable connecting the photo-tab sensor to the Servo and Power Supply PCBA, or to the EOT/BOT Amplifier PCBA, as applicable.

(2) Remove the screw that retains the sensor assembly; the screw is accessible from the rear of the deck.

(3) Loosen the screws, identified as 'X' and 'Y' in Figure 6-2, that retain the overlay.

(4) Remove the pins from the plug by using the extractor tool and feed the pins through the hole in the deck, then through the hole in the head plate.

(5) Insert the cable of the replacement photosensor through the head plate and deck.

(6) Replace the connector pins in the plastic connector body as follows.

- Brown wire — pin 1
- Red wire — pin 2
- Orange wire — pin 3
- Yellow wire — pin 4

(7) Align the surface of the photosensor parallel to the tape and tighten the retaining screw.

(8) Adjust the relevant BOT and EOT amplifiers as previously described.

6.7.10 REMOVAL OF TRIM AND OVERLAY

Some adjustments require removal of the vinyl overlay and trim on the front deck of the transport. The following procedure is followed when access is required.

(1) Loosen the two screws at the top of the door that secure the mounting block to the plastic door (do not remove the screws).

(2) Slide the door with respect to the mounting to align the hole in the door with the corresponding hole in the block.

(3) Insert a rod of less than 1/16-inch diameter in the hole at the top of the door and push down the spring plunger, releasing the top of the door.

(4) Carefully pull the top of the door forward approximately two inches. Ease the door downward to clear the bottom spring plunger and remove the door.

(5) Remove the spring plungers from the hinge blocks using the Vlier spring plunger wrench (No. VW-52).

(6) Unplug the Molex and magnetic tape head connectors from the Tape Control and Data PCBAs; remove the boards.

NOTE

Ensure each cable bundle is identified to enable correct re-installation.

(7) Remove and identify the three wires from the POWER switch/indicator.

(8) Remove the supply reel, take-up reel, and head cover.

(9) Remove the tape guide shields.

(10) Remove the ten 4-40 screws around the perimeter of the trim assembly, identified as 'Y' in Figure 6-2.

(11) Remove the six 4-40 screws holding the overlay to the base plate, identified as 'X' in Figure 6-2.

(12) Ease the trim out slowly past the tape guides and head. Gently pry the plastic trim out to clear the hinge blocks. Remove the trim and overlay, taking care to clear the door-stop arm.

6.7.11 CAPSTAN MOTOR ASSEMBLY REPLACEMENT

(1) Remove the trim as described in Paragraph 6.7.10.

(2) Disconnect the capstan motor connector from J11 of the Servo and Power Supply PCBA.

(3) Remove the four mounting screws from the capstan motor assembly; remove the motor. Discard any shims under the motor mounting screws.

(4) Mount the replacement capstan assembly and replace the four retaining screws.

NOTE

The mounting surface must be free of all foreign substances to ensure the perpendicularity of the capstan to the tape path.

(5) Connect the plug which connects the motor to J11 of the Servo and Power Supply PCBA.

(6) Perform a check of the read system skew as described in Paragraph 6.7.5.

6.7.12 TAPE PATH ALIGNMENT

Alignment of the supply and take-up guide rollers to the head guides is accomplished by using PERTEC Tape Alignment Tool, Part No. 102382-01. This alignment tool is also used to establish guide roller parallelism and the positioning of each tape reel.

CAUTION

THE TOOL IS PRECISION MADE. IT MUST BE HANDLED WITH CARE TO AVOID DAMAGE, ESPECIALLY TO ALL SURFACES. WHEN NOT IN USE, ATTACH THE CROSSBAR TO THE U-FRAME USING THE THUMB-SCREWS LOCATED AT EACH END OF THE CROSSBAR. STORE IN A PROTECTIVE AREA.

6.7.12.1 Transport Preparation

Refer to Figure 3-1 for location of parts referred to in Steps (1) and (3).

(1) Remove the protective cover enclosing the head and the tape guides by firmly grasping the cover and pulling away from the tape deck.

(2) Remove the upper and lower plastic tape guide caps; the Phillips head screws that secure the caps in place are accessible from the rear of the tape deck.

(3) Protect the tape path area of the head from damage and contamination.

(4) Remove the trim and overlay as outlined in Paragraph 6.7.10.

CAUTION

WHEN REMOVING THE OVERLAY, CARE MUST BE TAKEN TO PREVENT THE OVERLAY FROM COMING IN CONTACT WITH THE HEAD.

(5) Remove the guide caps from the fixed head guides with an Allen wrench. Prevent loosening of the guide post retaining screws ('J' and 'M' in Figure 6-2) which are accessible from the rear of the transport, by engaging and holding a second Allen head wrench in each respective screw head to prevent turning. Removal of the guide caps will enable installation of the tape alignment tool U-frame onto the tape guide posts.

6.7.13 TAKE-UP GUIDE ROLLER ALIGNMENT

Perform the transport preparation procedure described in Paragraph 6.7.12.1.

6.7.13.1 Take-up Guide Roller Height Check

(1) Install the U-frame to the guide posts; ensure that the wide end of the U-frame is toward the top of the tape deck. Insert a thumbscrew through mounting hole 'b', and one through mounting hole 'c' (see Figure 6-7). Tighten each thumbscrew finger-tight.

(2) Install the crossbar to the underside of the wide end of the U-frame through mounting hole 'a' as shown in Figure 6-7. Use the threaded screw hole at either end of the crossbar; do not tighten the thumbscrew until Step (3) is completed.

(3) Place the crossbar between the flanges of the take-up arm guide roller with the take-up arm positioned away from its end stop, shown as crossbar position 'A' in Figure 6-7. Tighten the crossbar thumbscrew finger-tight to the U-frame.

(4) Determine that the crossbar is centered between the flanges of the guide roller. If it is not centered, a guide roller height adjustment is required.

6.7.13.2 Take-up Guide Roller Height Adjustment

If the take-up arm height check performed in Paragraph 6.7.13.1 indicates that a height adjustment is required, proceed as follows.

(1) With the crossbar placed as in Paragraph 6.7.13.1, Step (3), and the guide roller still positioned away from its end stop, loosen take-up guide roller set-screw 'D' located on the take-up tension arm (see Figure 6-7).

(2) Center the guide roller flanges on the crossbar.

(3) When height is established, tighten the take-up guide roller set-screw 'D'.

6.7.13.3 Take-up Guide Roller Parallelism Check

(1) Install the tape path alignment tool as described in Paragraph 6.7.13.1, Steps (1) through (3).

(2) Observe an equal, but minimal, space between the flat (tape) area of the take-up guide roller and the bottom (narrow surface) of the crossbar.

(3) If the space is unequal from edge to edge, an adjustment between the two surfaces is required.

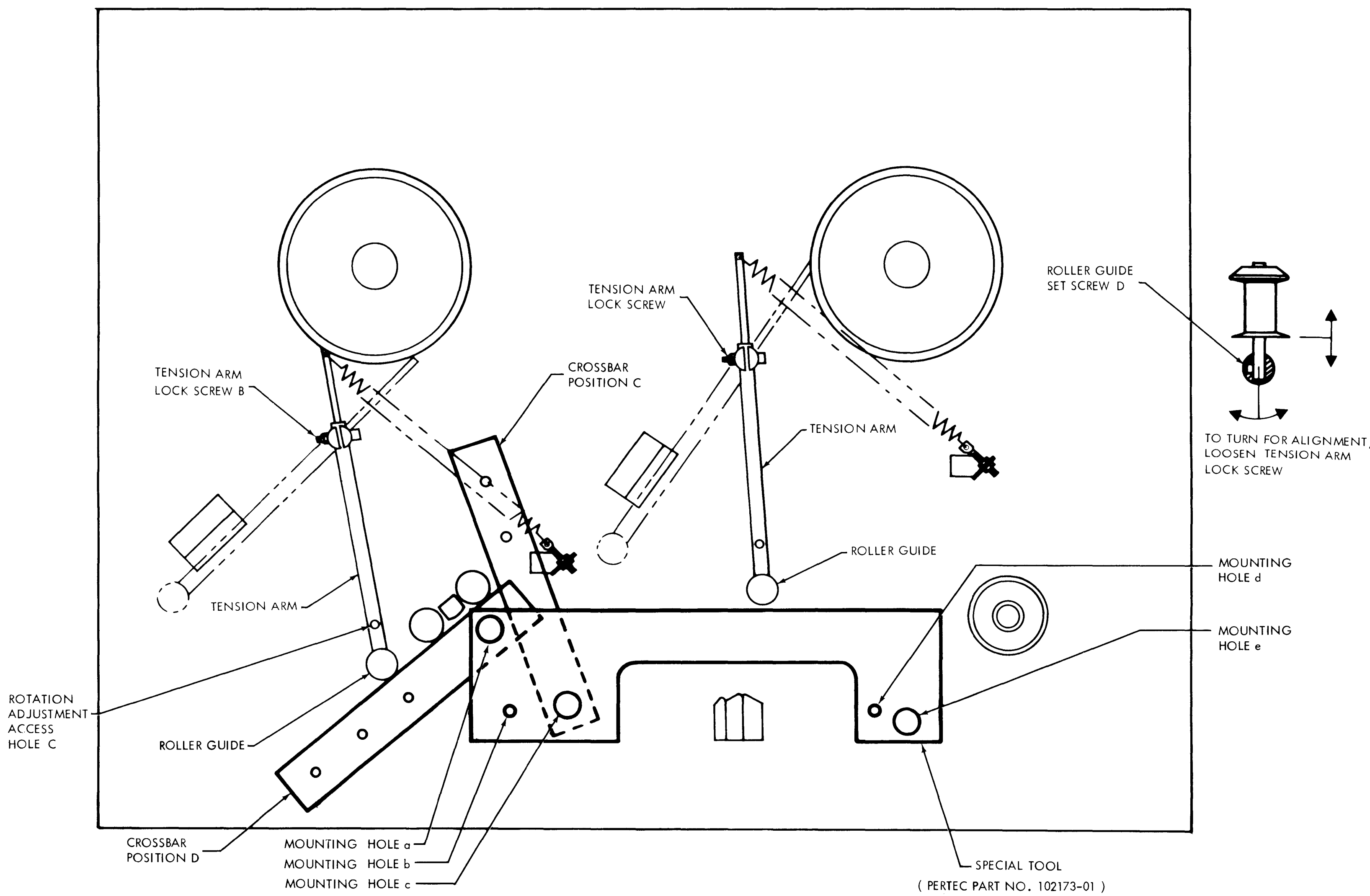


Figure 6-7. Take-up Guide Roller Alignment

6.7.13.4 Take-up Guide Roller Parallelism Adjustment

If the take-up guide roller parallelism check performed in Paragraph 6.7.13.3 indicates that an adjustment is required, proceed as follows.

(1) Engage an Allen wrench in the head of tension arm lock-screw 'B' (Figure 6-7) and, by using an open-end wrench, loosen the tension arm lock-nut. Loosen the lock-nut so that the tension arm can be rotated by inserting a suitable rod or tool into the through-hole 'C' on the tension arm.

(2) Rotate the tension arm until the face of the guide roller and the narrow crossbar surface are parallel. Test by observing a minimum and equal distance between the two inner vertical surfaces of the guide roller flanges and the vertical surfaces of the crossbar.

(3) Recheck the height of the guide roller.

(4) Tighten tension arm lock-screw 'B' to a torque setting of 25 in-lb, nominal.

6.7.13.5 Take-up Reel Flange Centering Check and Adjustment

Install the tape path alignment tool as described in Paragraph 6.7.13.1, Step (1).

(1) Remove the crossbar and retaining thumbscrews.

(2) Install the crossbar so that it falls between the flanges of the take-up reel shown as crossbar position 'B' in Figure 6-7. Tighten the thumbscrew finger-tight.

(3) With the crossbar secured in place, observe the centering of the narrow surfaces of the crossbar between the take-up reel flanges.

(4) If one surface of the crossbar is closer to one edge of the reel flange than the other, center the reel by loosening the two reel hub retaining screws located on the take-up reel hub. Equalize the flange-to-crossbar distances and retighten the hub screws.

6.7.13.6 Re-assembly

After the take-up adjustments have been completed, perform the following operations.

(1) Clean and install the guide caps, overlay, and trim.

(2) Make a general inspection of the tape deck to ensure that all items removed or disconnected are in place and ready to function.

(3) Refer to Paragraph 6.7.14.7 for the care of the alignment tool.

6.7.14 SUPPLY GUIDE ROLLER ALIGNMENT

Perform the transport preparation procedure described in Paragraph 6.7.12.1.

6.7.14.1 Supply Guide Roller Height Check

(1) Install the U-frame to the guide posts. Ensure that the wide end of the U-frame is toward the bottom of the tape deck. Insert a thumbscrew through mounting hole 'b' and one through mounting hole 'e' (see Figure 6-8); tighten each thumbscrew finger-tight.

(2) Install the crossbar to the underside of the wide end of the U-frame through mounting hole 'a' as shown in Figure 6-8. Use the threaded screw hole at either end of the crossbar; do not tighten the thumbscrew until Step (3) is completed.

(3) Place the crossbar between the flanges of the supply arm guide roller with the supply arm positioned away from its end stops. Tighten the thumbscrew finger-tight to the U-frame.

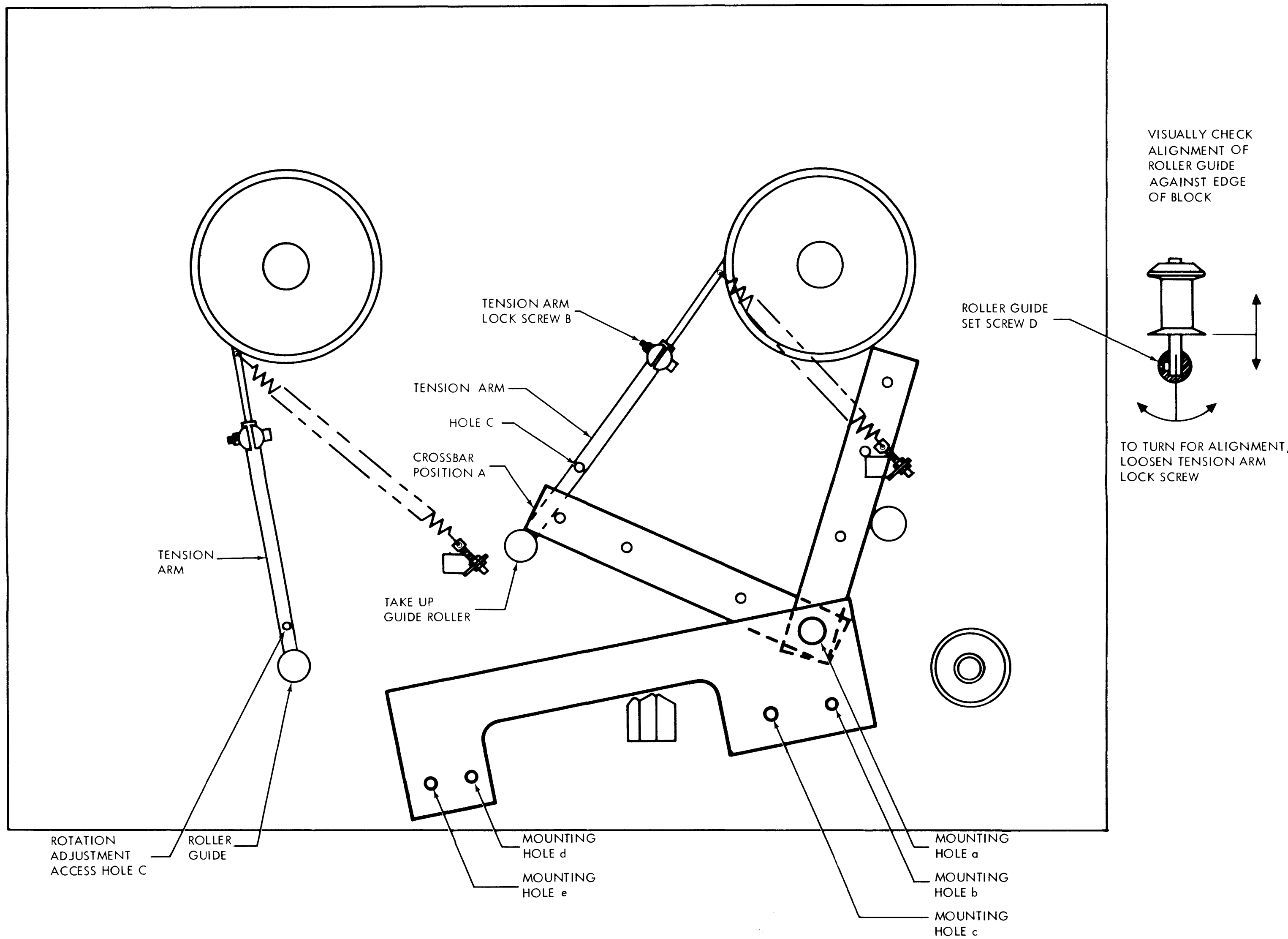


Figure 6-8. Supply Guide Roller Alignment

(4) Determine that the crossbar is centered between the flanges of the supply guide roller. If it is not centered, a guide roller height adjustment is required.

6.7.14.2 Supply Guide Roller Height Adjustment

If the supply guide roller check performed in Paragraph 6.7.14.1 indicates that a height adjustment is required, proceed as follows.

(1) With the crossbar placed as in Paragraph 6.7.14.1, and the guide roller still positioned away from the end stop, loosen the supply guide roller set-screw 'D' located on the supply tension arm (see Figure 6-8).

(2) Center the guide roller flanges on the crossbar.

(3) When height is established, tighten the supply guide roller set-screw 'D'.

6.7.14.3 Supply Guide Roller Parallelism Check

(1) Perform the check and adjustment procedures detailed in Paragraph 6.7.14.1 and 6.7.14.2, respectively.

(2) With the crossbar installed as described in Paragraph 6.7.14.1, observe an equal, but minimal, space between the flat (tape) area of the supply roller and the bottom (narrow surface) of the crossbar.

(3) If the space is unequal from edge to edge, an adjustment between the two surfaces is required.

6.7.14.4 Supply Guide Roller Parallelism Adjustment

If the supply guide roller parallelism guide check performed in Paragraph 6.7.14.3 indicates that an adjustment is required, proceed as follows.

(1) Engage an Allen wrench in the head of tension arm lock-screw 'B' (Figure 6-8) and, by using an open end wrench, loosen the tension arm lock-nut. Loosen the lock-nut so that the tension arm can be rotated by inserting a suitable rod or tool into rotation adjustment through-hole 'C' in the tension arm.

(2) Rotate the tension arm until the face of the guide roller and the narrow crossbar surface are parallel. Test by observing a minimum and equal distance between the two inner vertical surfaces of the guide roller flanges and the vertical surfaces of the crossbar.

(3) Recheck the height of the guide roller.

(4) Tighten the tension arm lock-screw 'B' to a setting of 25 in-lb nominal.

6.7.14.5 Supply Reel Flange Centering Check and Adjustment

Install the tape path alignment tool as described in Paragraph 6.7.14.1, Step (1).

(1) Place an empty tape reel onto the supply hub.

(2) Install the crossbar with the thumbscrew through mounting hole 'C'. Use threaded screw holes at either end of the crossbar.

(3) Swing the crossbar into place between the flanges of the supply reel as shown in Figure 6-8, position 'C'; tighten the thumbscrew finger-tight.

(4) With the crossbar in place, observe the centering of the narrow surfaces of the crossbar between the supply reel flanges.

(5) If one surface of the crossbar is closer to one edge of the reel flange than the other, center the reel by loosening the two reel hub retaining screws located on the supply reel hub. Equalize flange to crossbar distances and re-tighten the hub screws.

6.7.14.6 Re-assembly

After the supply adjustments have been completed, perform the following operations.

(1) Clean and install the guide caps, overlay, and trim.

(2) Make a general inspection of the tape deck to ensure that all items removed or disconnected are in place and ready to function.

6.7.14.7 Care of Alignment Tool

For storage, assemble the crossbar to the U-frame using thumbscrews through mounting holes 'C' and 'D'. Both thumbscrews will engage with threaded holes at each end of the crossbar.

The third thumbscrew should be threaded into one of the threaded holes on the crossbar for storage.

6.7.15 REEL SERVO BELT TENSION

The toothed belts that couple the motors to the reel hubs must have sufficient tension to prevent the teeth from skipping or servo instability due to backlash. The belts must not have excessive tension as this will cause overloading of the motor or reel shaft bearings in the radial direction. The belt tension can be adjusted as follows.

(1) Loosen the three screws that fasten the motor mounting plate to the deck standoffs.

NOTE

The slots in the motor mounting plate allow motion of the motor in the line of action of belt tension.

(2) Adjust the pulley so that the timing belt is snug. Note the last belt tooth that is completely seated in a slot on the large pulley (refer to Figure 6-9).

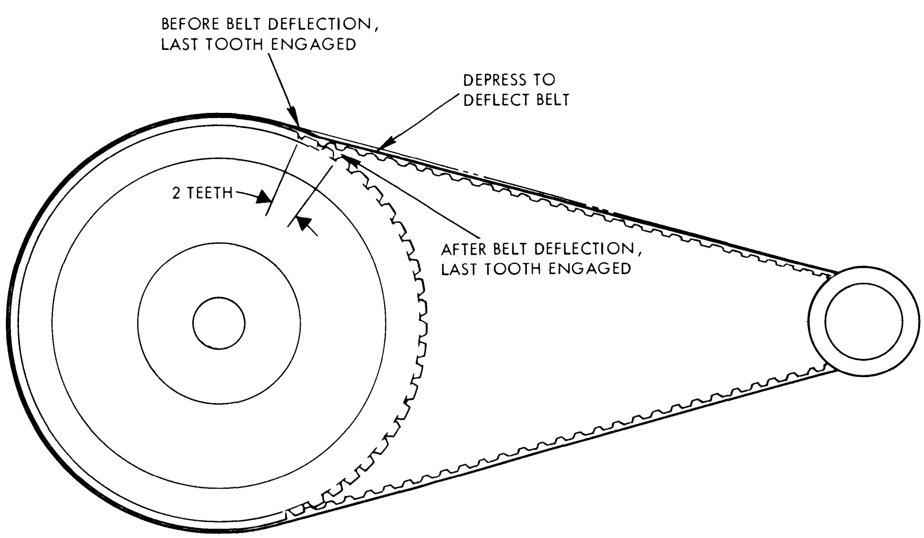


Figure 6-9. Reel Servo Belt Tension Adjustment

(3) Count two to three teeth from the last engaged tooth. Hold the large pulley to ensure that it does not turn. Depress the toothed belt at the point between the second and third teeth with sufficient force to deflect the belt flush against the gear.

CAUTION

DO NOT APPLY EXCESSIVE FORCE ON THE TOOTHED BELT.

(4) Adjust the drive motor assembly so that the second tooth is firmly engaged in a slot on the large pulley, but the third belt tooth is not engaged.

(5) Tighten the three screws on the motor mounting plate and recheck for the condition in Step (2).

6.7.16 TAPE TENSION ADJUSTMENT

Tape tension is controlled by the spring attached to each of the tension arms. The tension is adjusted by means of the anchor screws. Figure 6-10 shows the measurement and adjustment of the supply tape tension. A 2-foot length of tape with loops at each end is used and, after removing the trim as described in Paragraph 6.7.10, tape is mounted as shown. A 1-pound force gauge is used to measure tape tension. Care must be taken to zero the scale in the correct orientation of the gauge and to pull on the tape in the direction shown. The anchor screw is adjusted until the tension is 8 ounces with the arm in the center of its operating region.

Figure 6-11 shows the measurement and adjustment of the take-up tape tension. Using the same piece of tape mounted as shown, with the gauge zeroed against the correct orientation, the anchor screw is adjusted until tape tension is 8 ounces with the arm in the center of its operating region.

6.7.17 REEL HUB ASSEMBLY REPLACEMENT

Replacement of the standard push button, or the quick-release reel hub assembly, can be accomplished as follows.

(1) Loosen the two No. 10 set-screws which hold the belt-driven gear on the shaft.

(2) Slide the belt-driven gear to the rear and off the shaft (the toothed belt will disengage from the gear).

(3) Loosen the No. 10 set-screw, or No. 4-40 screw, in the shaft bearing housing.

NOTE

It may be necessary to rotate the hub to align the set-screw with the access hole.

(4) Remove the hub by withdrawing it from the front of the transport.

(5) Install the replacement hub assembly. Care should be taken to ensure line-up of each set-screw to the appropriate flat surface on the shaft.

(6) Adjust the hub height before tightening the set-screw in the bearing housing.

NOTE

Refer to Tape Path Alignment Procedure, Paragraph 6.7.12 for alignment procedure.

(7) Adjust the write lockout plunger as required (refer to Paragraph 6.7.19).

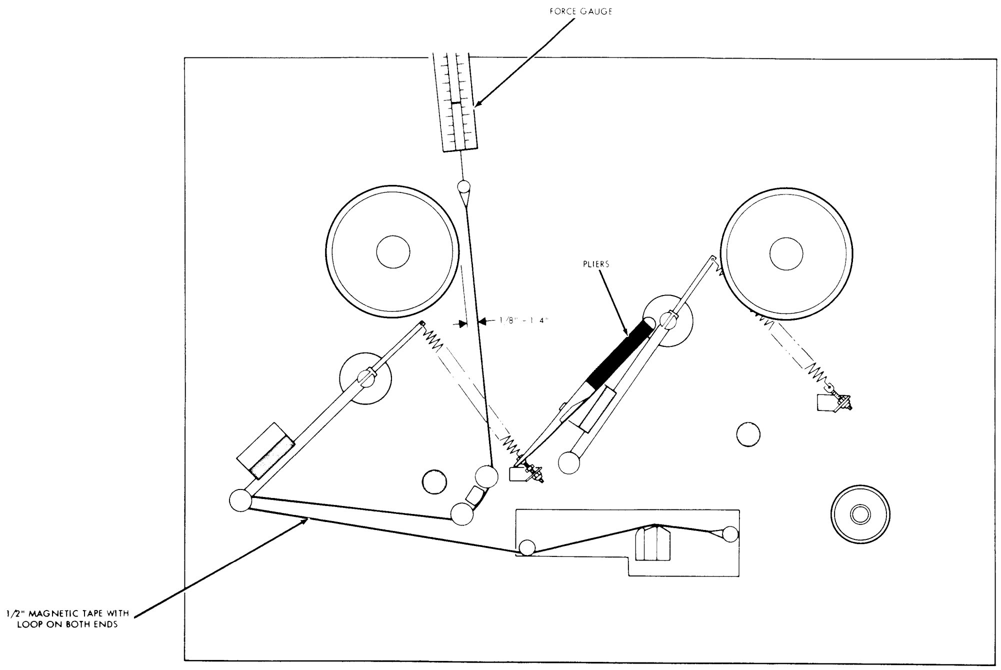


Figure 6-10. Supply Tape Tension Adjustment

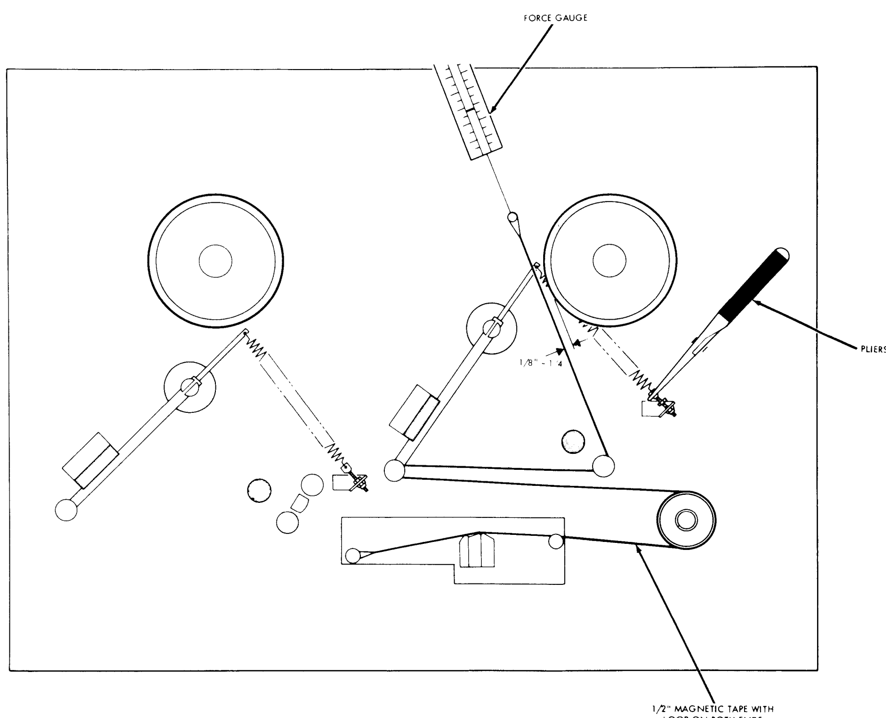


Figure 6-11. Take-up Tape Tension Adjustment

6.7.18 QUICK-RELEASE REEL HUB EXPANSION RING ADJUSTMENT

Some T6000 series transports are equipped with a quick-release type reel hub as shown in Figure 6-12. When this type of reel hub is replaced, adjustment of the hub expansion ring is required. Adjustment is also necessary if slippage of either reel is noted.

Adjustment of the expansion ring is accomplished as follows (refer to Figure 6-12).

(1) Place the quick-release latch on the hub in the unload position.

(2) Load a reel of tape on the transport.

(3) Lock the quick-release latch by depressing the indented portion of the latch (identified as 'B' in Figure 6-12).

(4) Using a suitable force gauge, exert pressure on the quick-release latch at point 'B' until the latch releases; note the reading.

(5) If the applied force required to release the latch is less than 6 pounds, the expansion ring should be adjusted.

(6) To increase the pressure required to release the latch, insert an Allen wrench into adjustment hole 'A' (Figure 6-12) and turn one-quarter turn clockwise.

(7) Repeat Steps (4), (5), and (6) until the release force required is 6 pounds.

6.7.19 WRITE LOCKOUT ASSEMBLY

When a supply reel hub assembly or a write lockout assembly has been replaced, adjustment of the write lockout plunger may be required. The plunger height should be adjusted so that when the plunger is fully retracted, the plunger end is just flush with the back side of the reel hub assembly flange. Adjustment may be accomplished by removing the write lockout assembly, loosening the safety nut, and rotating the plunger adjusting screw to the desired position. The safety nut is then tightened.

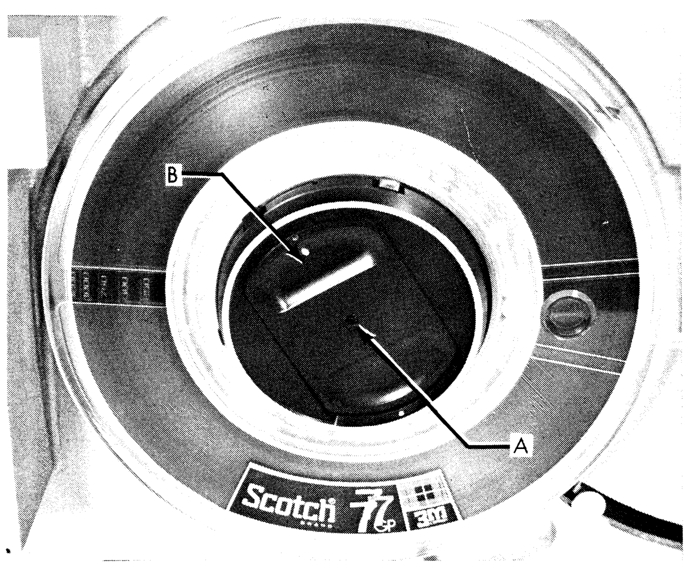


Figure 6-12. Reel Hub Expansion Ring Adjustment

6.8 MAINTENANCE TOOLS

The following list of tools is required to maintain the tape transport.

(1) Hex socket keys for 5/32, 1/8, 3/32 set-screws, and a splined drive socket key for a 4-40 set-screw.
(2) Open-end wrenches for 3/16-, 1/4-, 5/16- and 3/8-inch bolts.
(3) Long-nose pliers.
(4) Phillips screwdriver set.
(5) Standard blade screwdriver set.
(6) Soldering aid.
(7) Soldering iron.
(8) One-pound force gauge.
(9) Lint-free cloth.
(10) Cotton swabs.
(11) 91 percent isopropyl alcohol.
(12) Torque wrench, 0-35 in-lb.
(13) Tape Path Alignment Tool (tension arm guide alignment), PERTEC Part No. 102382-01.
(14) Arm Movement Measuring Tool (take-up arm adjustment), PERTEC Part No. 101137.
(15) Molex pin extractor (Mfg. Part No. HT2285).
(16) Spring plunger wrench, Vlier VW-52.
(17) Head Adjustment Tool, PERTEC Part No. 103259-01.

6.9 TROUBLESHOOTING

Table 6-5, System Troubleshooting chart, provides a means of isolating faults, possible causes, and remedies. The troubleshooting chart is used in conjunction with the schematics and assembly drawings in Section VII.

Table 6-5

System Troubleshooting

Symptom	Probable Cause	Remedy	Reference
Tape does not tension and capstan shaft rotates freely when LOAD control is depressed for first time after threading tape.	Interlock relay K1 does not close.	Check relay operation; replace if necessary.	Paragraph 5.2.6 or 5.2.7
	LOAD control not operative.	Check LOAD operation; replace if necessary.	Paragraph 5.4.1 or 5.4.2
	Relay driver defective.	Check collector voltage of relay driver transistor with LOAD control depressed; it should be less than +1v — if greater, isolate defective relay driver component and replace.	Paragraph 5.4.1 or 5.4.2
Tape is tensioned when LOAD is depressed, but tension is lost when control is released.	Relay latching contacts 9 and 10 do not mate.	Check that voltage at J9-7 goes to +5v when LOAD control is depressed.	Paragraph 5.4.1 or 5.4.2
	Limit switch is not operative.	Adjust; possibly replace limit switch assembly.	Paragraph 6.7.1
Tape unwinds or tension arm hits stop when LOAD is depressed first time.	Tape is improperly threaded.	Rethread tape (see F 3-1).	Paragraph 3.3
	+5v or —5v missing from tension arm sensor.	Check tension arm sensor lamps. Isolate problem if lamp is extinguished.	Paragraph 6.7.2 or 6.7.3
	Fault in reel servo amplifier.	Check that movement of reels responds to tension arm position without tape on the transport.	Paragraph 5.2.6 or 5.2.7
Tape *runs away* or rewinds when LOAD control is depressed for second time.	Fault on Tape Control PCBA or capstan motor assembly.	Replace/repair Tape Control PCBA or capstan motor assembly.	Paragraph 5.2.8 or 6.7.11
Tape runs past BOT tab.	BOT tab defective.	Replace tab or increase sensitivity of photosensor amplifier.	Paragraph 6.6.6, 6.6.7, or 6.7.9
	Photosensor not properly adjusted.	Adjust photosensor amplifier.	
	Photosensor or amplifier defective.	Check for appropriate voltage levels in sensor systems with tab not over appropriate voltage levels in sensor systems when tab is over photosensor.	
	Logic fault (Load flip-flop does not reset).	Replace/repair Tape Control PCBA.	Paragraph 5.2.8

Table 6-5

System Troubleshooting (cont'd)

Symptom	Probable Cause	Remedy	Reference
Transport does not move in response to SYNCRONOUS FORWARD or REVERSE commands.	Interface cable fault or receiver fault.	Check levels at inputs and outputs of receivers on Tape Control PCBA. Replace or repair cable or Tape Control PCBA.	Paragraph 5.2.8
	Transport is not Ready.	Replace/repair Tape Control PCBA.	
	Fault in ramp generator or capstan servo amplifier.	Check TP5 on Tape Control PCBA. Replace/repair Tape Control or Servo and Power PCBA.	Paragraph 5.2.6, 5.2.7, or 5.2.8
Transport responds to SFC, but tape is not written.	Write current is not enabled.	Check presence of Write Enable ring on supply reel (WRT EN indicator illuminated). Check TP1 on Tape Control PCBA (+5v for writing). Replace Write Lockout Assy if faulty. Check that WRT PWR is +5v at Data PCBA interface connector and appropriate TP on Data PCBA when writing.	Paragraph 5.2.1, 5.2.2, 5.2.8
	Write status or Motion signal to Data PCBA is not correct.	Check receiver on Tape Control PCBA for Write status and on Data PCBA for Write status.	
		Check Data PCBA for Motion signal. Replace/repair Data or Tape Control PCBA if faulty.	
	WRITE DATA or WRITE DATA STROBE is not received correctly on Data PCBA from interface.	Check presence of correct levels on Data PCBA; replace/repair Data PCBA or interface cable if faulty.	Paragraph 5.2.1, 5.2.2, 5.2.3, 5.2.4
	Head not plugged in correctly.	Check read/write heads on Data PCBA (on T6X40, read cable enters head nearest take-up reel).	—

Table 6-5
System Troubleshooting (cont'd)

Symptom	Probable Cause	Remedy	Reference
Data incorrectly written.	Incorrect data format.	Use correct format.	IBM Form A22-6589-3 (727 or 729 Series); IBM Form A22-6866-3 (2400 Series)
	Fault on one track due to failure in write circuits.	Check receiver and write amplifier on Data PCBA. Replace/repair Data PCBA if faulty.	Paragraph 5.2.1, 5.2.2, 5.2.3, 5.2.4
	Intermittent WRT PWR, WRITE, MOTION, or WARS signal.	Examine signals and replace/repair Tape Control PCBA or Write Lockout Assy on Data PCBA if faulty.	Paragraph 5.2.1, 5.2.2, 5.2.7
	Write deskew circuit faulty.	Check TP10 (Data E7/E9) or TP8 (Data E17/E19) for a sequence of 10 pulses for each WDS. Replace Data PCBA if necessary.	Paragraph 5.2.1, 5.2.2
Correct tape cannot be read.	Interface cable or transmitter fault.	Replace/repair interface cable or Data PCBA.	Paragraph 5.2.1, 5.2.2, 5.2.3, 5.2.4.
	Head is not plugged in.	Check read/write heads.	—
	Tape tracking on skew is badly adjusted.	Re-adjust according to Section VI.	Paragraph 6.7.5.2
	Head and guides need cleaning.	Clean head and guides.	Paragraph 6.4
	Tape cleaner needs cleaning or positioning.	Remove tape cleaner; clean and re-install.	
	Read amplifier gains incorrectly adjusted.	Check and adjust amplifier gains.	Paragraph 6.6.12
	Faulty write amplifier causes current to be passed through head while reading.	Check write amplifier output test points and replace or repair Data PCB.	Paragraph 5.2.1, 5.2.2, 5.2.3, 5.2.4
	Component fault in read channel.	Check test points on Data PCBA; replace / repair Data PCBA.	
	Read staticiser adjustment faulty.	Check TP11 (Data E7/E9) or TP9 (Data E17/E19). Check duration of positive section of waveform for one-half of a bit time.	Paragraph 6.6.15

SECTION VII
PARTS LISTS, LOGIC LEVELS AND WAVEFORMS, AND SCHEMATICS

7.1 INTRODUCTION

This section includes illustrated parts lists, logic level and waveform definitions, interconnect lists, and schematic and assembly drawings.

7.2 ILLUSTRATED PARTS BREAKDOWN (IPB)

Figures 7-1 through 7-3, used in conjunction with Tables 7-1 through 7-3, respectively, provide identification by PERTEC part number of the mechanical and electrical components of the T6000 Series Tape Transports.

When part numbers for a particular part differ due to a change in transport configuration, descriptions and part numbers for all configurations are listed.

7.3 RECOMMENDED SPARE PARTS

Table 7-4 provides a list of recommended spare parts for the T6000 Series Transports. The customer should always furnish model number and serial number of the transport when ordering parts.

7.4 PART NUMBER CROSS REFERENCE

Table 7-5 provides a cross reference to the manufacturer's part number from typical PERTEC part numbers.

7.5 PCBA INTERCONNECTIONS

Interconnections between PCBAs installed in the T6X40 and T6X60 transports are listed in Tables 7-6 and 7-7, respectively.

7.6 LOGIC LEVELS AND WAVEFORMS

The transport control and interface logic uses the DTL800 series of logic elements. Logic levels are: +5.0v — logical true; +0.4v — logical false.

All basic waveform names correspond to the logical true condition, e.g., SET WRITE STATUS (ISWS) enables the write circuits when it is logically true (+5.0v), or disables the write circuits when it is logically false (0v).

The inverse of a waveform is denoted by the prefix 'N'. Therefore, NBOT will be 0.4v when the BOT tab is under the photosensor head, or +5.0v otherwise.

All interface lines connecting the transport to the controller are prefixed by 'I'. Each line must be terminated at the receiver end of the cable by a 220/330-ohm divider chain between +5.0v and 0v.

All interface waveforms are low-true. Their logic levels are: +3.0v — logical false; +0.4v — logical true. For example, SYNCHRONOUS FORWARD command (ISFC) will be +0.4v when the transport is being driven in the forward direction, or +3.0v otherwise.

The Glossary contains the waveform mnemonics referred to in this manual.

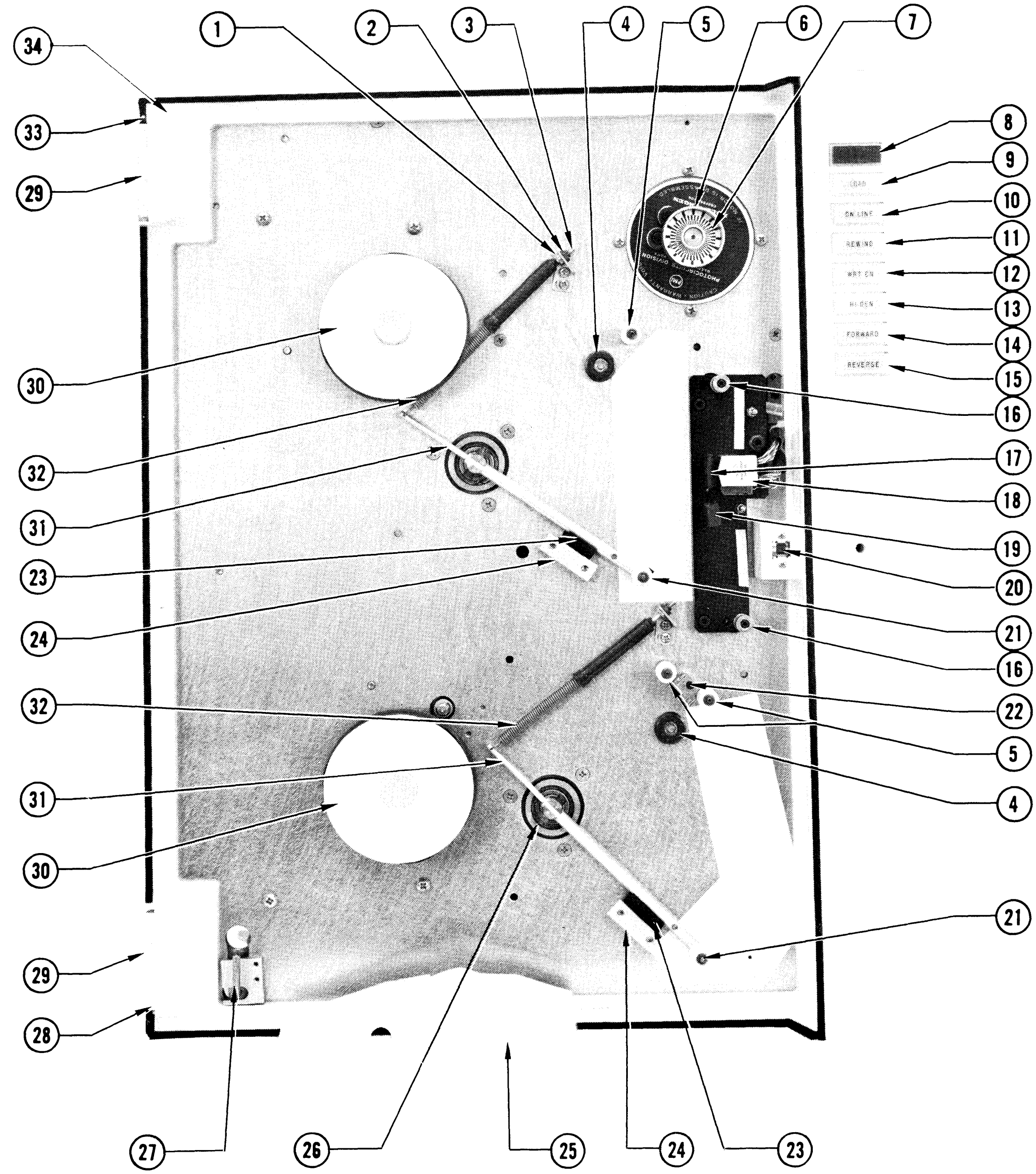


Figure 7-1. T6000 Series Transports Photo Parts Index, Front View

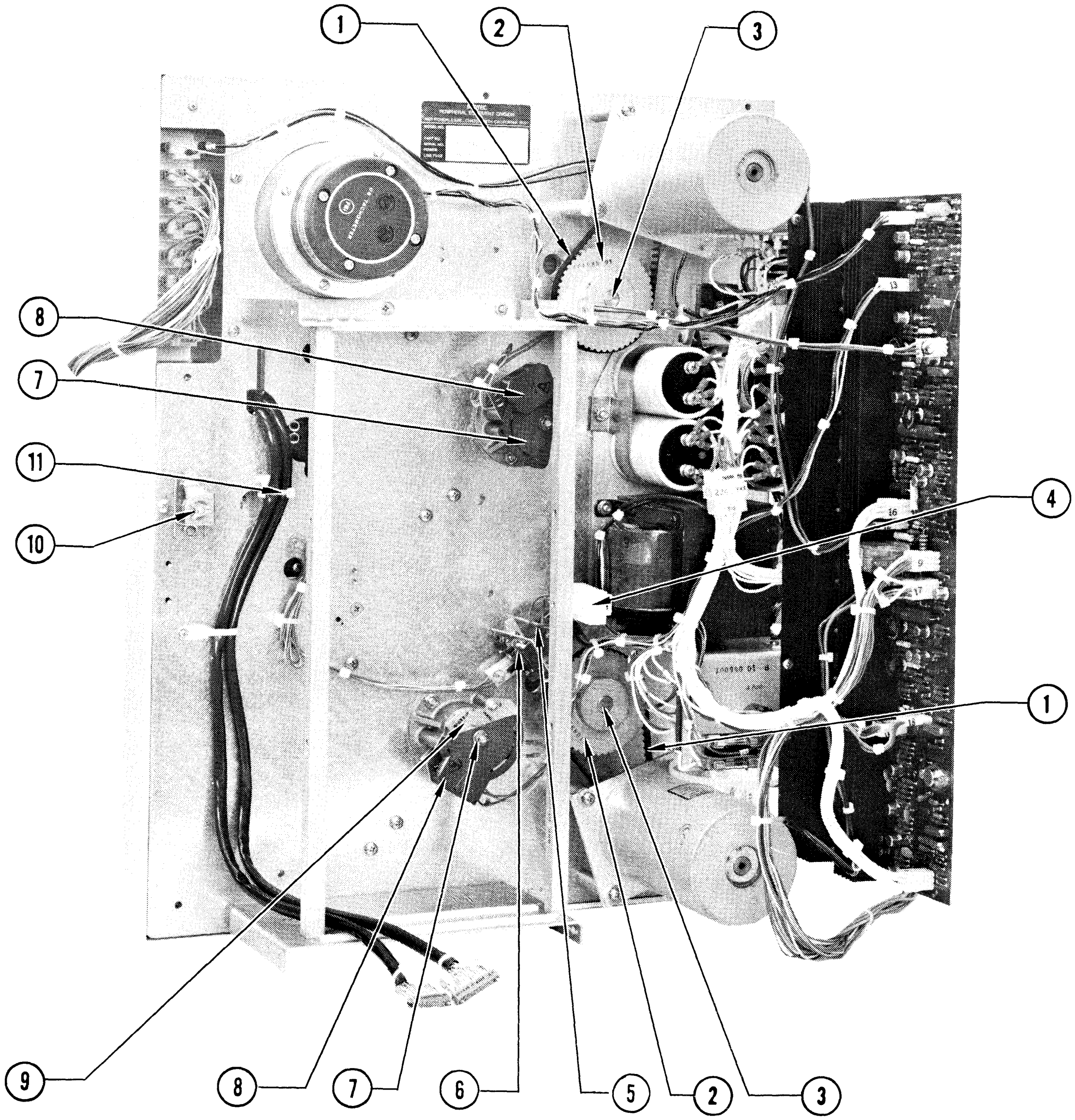


Figure 7-2. T6000 Series Transports Photo Parts Index, Rear View

Table 7-2

T6000 Series Transports Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-2		
-1	610-0007	Timing Belt
-2	104777-01	Pulley
-3	100179-01	Reel Drive Assembly
-4	101070-01	Card Alignment Block
-5	101003-01	Write Lockout Assembly
-6	101949-01	EOT/BOT Amplifier Assembly
-7	100925-01	Shutter
-8	100858-02	Tension Arm Sensor
-9	101669-01 506-6360	Limit Switch Cam Switch
-10	615-4410	Pawl Fastener
-11	661-0003	Tie Wrap

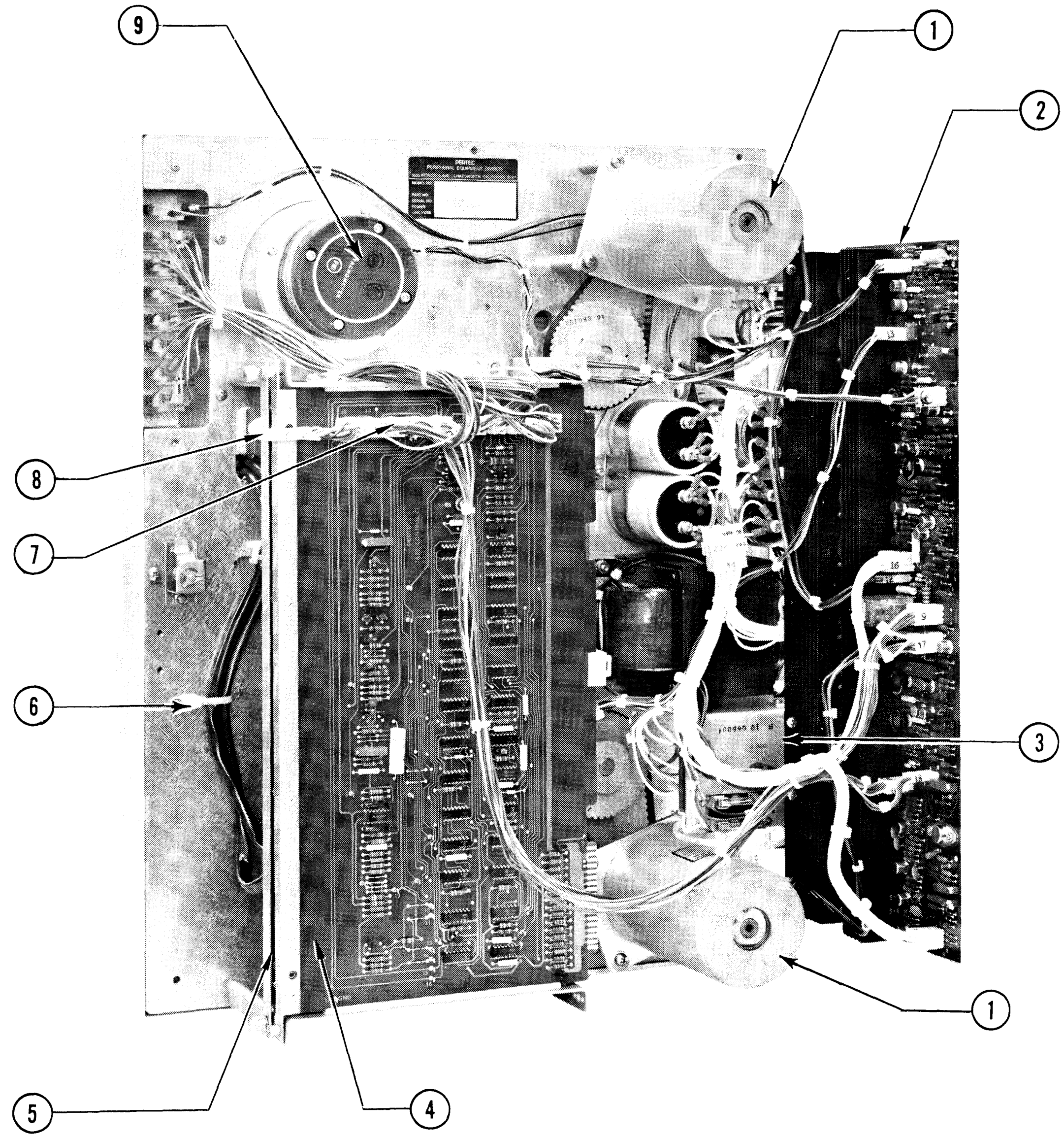


Figure 7-3. T6000 Series Transports Photo Parts Index, Rear View with Card Cage

Table 7-3

T6000 Series Transports Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-3		
-1	101004-01	Reel Motor Assembly
	100162-01	Motor Pulley
	603-1603	Set Screw
-2	*	Servo and Power PCBA
-3	100990-01	Power Supply Assembly (≤40 ips)
	100990-02	Power Supply Assembly (>40 ips)
-4	*	Tape Control PCBA
-5	*	Data PCBA
-6	661-0008	Tie Wrap
-7	102021-02	Switch Cable Assembly
-8	101077-01	Cable Assembly
-9	*	Capstan Motor Assembly

*Refer to Table 7-4 for specific part number.

Table 7-4
T6000 Series Recommended Spare Parts List

Item	Part No.
Data G PCBA (6660)	101376-*
Data F PCBA (6640)	101346-*
Data K PCBA (6X11/6X12)	101887-*
Data K1 PCBA (6640-98)	102326-*
Data D1 PCBA (6X60)	101721-*
Data E17 PCBA (6X40, 7-track)	101716-*
Data E19 PCBA (6X40, 9-track)	101711-*
PE/NRZI Write PCBA (6640-98)	102308-*
Deskew A PCBA	101892-*
Tape Control C1 PCBA	101241-*
Tape Control C2 PCBA (6640-98, 6X11/6X12)	101882-*
Power and Servo A PCBA	101021-*
Power and Servo B PCBA (45 ips)	101262-*
Reel Motor Assembly	101004-01
Capstan Motor Assembly (≤45 ips)	101073-01
Capstan Motor Assembly (25 — 40 ips)	101073-02
Photosensor Assembly	100807-01
Flux Gate Assembly (Dual Stack Only)	102581-01
Tension Arm Sensor	100858-02
POWER Switch (Horizontal Marking)	505-1801
POWER Switch (Vertical Marking)	505-1812
LOAD Switch (Horizontal Marking)	505-1803
LOAD Switch (Vertical Marking)	505-1814
ON LINE Switch (Horizontal Marking)	505-1804
ON LINE Switch (Vertical Marking)	505-1815
REWIND Switch (Horizontal Marking)	505-1805
REWIND Switch (Vertical Marking)	505-1816
WRT EN Switch (Horizontal Marking)	505-1806
WRT EN Switch (Vertical Marking)	505-1817
HI DEN Switch (Horizontal Marking)	505-1807
HI DEN Switch (Vertical Marking)	505-1818
1600 CPI Switch (Horizontal Marking)	505-1827
1600 CPI Switch (Vertical Marking)	505-1831
9 TRACK Switch (Horizontal Marking)	505-1830
9 TRACK Switch (Vertical Marking)	505-1834
FORWARD Switch (Horizontal Marking)	505-1808
FORWARD Switch (Vertical Marking)	505-1819
FORWARD Switch (6640-98, 6X11/6X12) (Horizontal Marking)	505-1828
FORWARD Switch (6640-98, 6X11/6X12) (Vertical Marking)	505-1832
REVERSE Switch (Horizontal Marking)	505-1809
REVERSE Switch (Vertical Marking)	505-1820
REVERSE Switch (6640-98, 6X11/6X12) (Horizontal Marking)	505-1829
REVERSE Switch (6640-98, 6X11/6X12) (Vertical Marking)	505-1833
Head, 6X40 7-track, All Speeds	510-6187
Head, 6X40 9-track, All Speeds	510-6189
Head, 6640 9-track, All Speeds	510-6269
Head, 6640-98 9-track, All Speeds	510-6269
Head, 6X60 7-track, All Speeds	510-5187
Head, 6X60 9-track, All Speeds	510-5189
Head, 6660 9-track, 12.5 ips	510-5169
Head, 6660 9-track, 18.75 ips	510-5269
Head, 6660 9-track, 25—45 ips	510-5369
Head, 6X11 7-track, All Speeds	510-5287
Head, 6X11 9-track, All Speeds	510-5289
Head, 6611 9-track, All Speeds	510-5469
Head, 6612, 6X12 9- & 7-track, All Speeds	510-8179
Head Guide Shim	100298-01

*Refer to your unit for version.

Table 7-5
Part Number Cross Reference

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Composition Resistors	(Comply with MIL-R-11)	
100-0395		3.9 ohms ±5%, 1/4w
100-1005		10 ohms ±5%, 1/4w
100-1015		100 ohms ±5%, 1/4w
100-1025		1.5k ohms ±5%, 1/4w
100-1055		1 meg ohm ±5%, 1/4w
100-1235		150 ohms ±5%, 1/4w
100-1525		1.5k ohms ±5%, 1/4w
100-1535		15k ohms ±5%, 1/4w
100-1815		180 ohms ±5%, 1/4w
100-1825		1.8k ohms ±5%, 1/4w
100-1845		180k ohms ±5%, 1/4w
100-2215		220 ohms ±5%, 1/4w
100-2225		2.2k ohms ±5%, 1/4w
100-2235		22k ohms ±5%, 1/4w
100-2705		27 ohms ±5%, 1/4w
100-2725		2.7k ohms ±5%, 1/4w
100-3305		33 ohms ±5%, 1/4w
100-3315		390 ohms ±5%, 1/4w
100-3325		3.3k ohms ±5%, 1/4w
100-3925		3.9k ohms ±5%, 1/4w
100-4705		47 ohms ±5%, 1/4w
100-4715		470 ohms ±5%, 1/4w
100-4725		4.7k ohms ±5%, 1/4w
100-5625		5.6k ohms ±5%, 1/4w
100-6805		68 ohms ±5%, 1/4w
100-6815		680 ohms ±5%, 1/4w
100-8215		820 ohms ±5%, 1/4w
100-8235		82k ohms ±5%, 1/4w
101-1025		1k ohms ±5%, 1/2w
101-1505		15 ohms ±5%, 1/2w
101-1515		150 ohms ±5%, 1/2w
101-2205		22 ohms ±5%, 1/2w
101-2715		270 ohms ±5%, 1/2w
101-3305		33 ohms ±5%, 1/2w
101-3325		3.3k ohms ±5%, 1/2w
101-3915		390 ohms ±5%, 1/2w
101-4715		470 ohms ±5%, 1/2w
101-6805		68 ohms ±5%, 1/2w
101-8205		82 ohms ±5%, 1/2w
102-5615		560 ohms ±5%, 1w
102-8205		82 ohms ±5%, 1w
103-1215		120 ohms ±5%, 2w
103-1815		180 ohms ±5%, 2w
103-4705		47 ohms ±5%, 2w

Table 7-5
Part Number Cross Reference (Continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Precision Resistors	(Comply with MIL-R-11)	
104-1000		100 ohms ±1%, 1/4w
104-1001		1k ohms ±1%, 1/4w
104-1002		10k ohms ±1%, 1/4w
104-1003		100k ohms ±1%, 1/4w
104-1100		110 ohms ±1%, 1/4w
104-1101		1.1k ohms ±1%, 1/4w
104-1102		11k ohms ±1%, 1/4w
104-1211		1.21k ohms ±1%, 1/4w
104-1330		133 ohms ±1%, 1/4w
104-1331		1.33k ohms ±1%, 1/4w
104-1332		13.3k ohms ±1%, 1/4w
104-1623		162k ohms ±1%, 1/4w
104-1781		1.78k ohms ±1%, 1/4w
104-1782		17.8k ohms ±1%, 1/4w
104-1961		1.96k ohms ±1%, 1/4w
104-1962		19.6k ohms ±1%, 1/4w
104-2151		2.15k ohms ±1%, 1/4w
104-2152		21.5k ohms ±1%, 1/4w
104-2370		237 ohms ±1%, 1/4w
104-2610		261 ohms ±1%, 1/4w
104-2611		2.61k ohms ±1%, 1/4w
104-2612		26.1k ohms ±1%, 1/4w
104-2870		287 ohms ±1%, 1/4w
104-3481		3.48k ohms ±1%, 1/4w
104-3831		3.83k ohms ±1%, 1/4w
104-3832		38.3k ohms ±1%, 1/4w
104-3833		383 ohms ±1%, 1/4w
104-3482		34.8k ohms ±1%, 1/4w
104-3483		348k ohms ±1%, 1/4w
104-4220		422 ohms ±1%, 1/4w
104-4221		4.22k ohms ±1%, 1/4w
104-4222		42.2k ohms ±1%, 1/4w
104-4641		4.64k ohms ±1%, 1/4w
104-4753		475k ohms ±1%, 1/4w
104-5110		511 ohms ±1%, 1/4w
104-5111		5.11k ohms ±1%, 1/4w
104-5113		511k ohms ±1%, 1/4w
104-5620		562 ohms ±1%, 1/4w
104-5621		5.62k ohms ±1%, 1/4w
104-6192		61.9k ohms ±1%, 1/4w
104-6811		6.81k ohms ±1%, 1/4w
104-6812		68.1k ohms ±1%, 1/4w
104-7500		750 ohms ±1%, 1/4w
104-8252		82.5k ohms ±1%, 1/4w
104-9090		909 ohms ±1%, 1/4w

Table 7-5
Part Number Cross Reference (Continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Precision Resistors (Continued)		
104-9092		90.9k ohms ±1%, 1/4w
104-9093		909k ohms ±1%, 1/4w
107-1000		100 ohms ±1%, 1/8w
107-1001		1k ohms ±1%, 1/8w
107-1002		10k ohms ±1%, 1/8w
107-1003		100k ohms ±1%, 1/8w
107-1101		1.1k ohms ±1%, 1/8w
107-1102		11k ohms ±1%, 1/8w
107-1211		1.21k ohms ±1%, 1/8w
107-1332		13.3k ohms ±1%, 1/8w
107-1471		1.47k ohms ±1%, 1/8w
107-1781		1.78k ohms ±1%, 1/8w
107-1782		17.8k ohms ±1%, 1/8w
107-1961		1.96k ohms ±1%, 1/8w
107-1962		19.6k ohms ±1%, 1/8w
107-1963		196k ohms ±1%, 1/8w
107-2152		21.5k ohms ±1%, 1/8w
107-2611		2.61k ohms ±1%, 1/8w
107-2612		26.1k ohms ±1%, 1/8w
107-2870		287 ohms ±1%, 1/8w
107-3482		34.8k ohms ±1%, 1/8w
107-3483		348k ohms ±1%, 1/8w
107-3832		38.3k ohms ±1%, 1/8w
107-4221		4.22k ohms ±1%, 1/8w
107-4222		42.2k ohms ±1%, 1/8w
107-5110		511 ohms ±1%, 1/8w
107-5111		5.11k ohms ±1%, 1/8w
107-5112		51.1k ohms ±1%, 1/8w
107-5113		511k ohms ±1%, 1/8w
107-5620		562 ohms ±1%, 1/8w
107-6192		61.9k ohms ±1%, 1/8w
107-6811		6.81k ohms ±1%, 1/8w
107-6812		68.1k ohms ±1%, 1/8w
107-8252		82.5k ohms ±1%, 1/8w
107-9090		909 ohms ±1%, 1/8w
109-0003		0.10 ohms ±3%, 5w
113-0111		10 ohms ±1%, 1w
Variable Resistors		
121-1020	Beckman	79PR1K, Variable, 1k ohms ±10%, 3/4w
121-1030	Beckman	79PR10K, Variable, 10k ohms ±10%, 3/4w
121-5020	Beckman	79PR5K, Variable, 5k ohms ±10%, 3/4w
123-5020	Spectrol	53-1-1-502, Variable, 5k ohms ±10%, 1/2w

Table 7-5

Part Number Cross Reference (Continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Dipped Mica Capacitors		
130-1005	(Comply with MIL-C-5)	10 pf ±5%, 500v dc
130-1015		100 pf ±5%, 500v dc
130-1515		150 pf ±5%, 500v dc
130-2205		22 pf ±5%, 500v dc
130-2215		220 pf ±5%, 500v dc
130-3305		33 pf ±5%, 500v dc
130-4705		47 pf ±5%, 500v dc
130-4715		470 pf ±5%, 500v dc
130-5605		56 pf ±5%, 500v dc
130-6805		68 pf ±5%, 500v dc
130-7515		750 pf ±5%, 500v dc
Mylar Film Capacitors		
131-1020	TRW	663uw series, .001μfd ±10%, 100v dc
131-1030	TRW	663uw series, .01μfg ±10%, 100v dc
131-2220	TRW	663uw series, .0022μfd ±10%, 100v dc
131-4720	TRW	663uw series, .0047μfd ±10%, 100v dc
Solid Tantalum Polarized Capacitors		
132-1062	Mallory	TIM106M010POW, 10μfd ±20%, 10v dc
132-2752	Mallory	TIM275M035POW, 2.7μfg ±20%, 35v dc
139-2244	Kemet	T310A225M020AS, 2.2μfd ±20%, 20v dc
139-2262	Kemet	T310B226M015AS, 22μfd ±20%, 15v dc
139-3352	Kemet	T310A335M015AS, 3.3μfg ±20%, 15v dc
Aluminum Foil Polarized Capacitor		
134-2680	Mallory	TOW282N025N1R3P, 2600 μfg +100% —10%, 20v dc
Ceramic Capacitors		
135-1002	Centralab	DD-102, .001μfg ±10%, 1000v dc
135-1040	TRW	663uw series, .10μfd ±10%, 100v dc
135-4742	Erie	8131-050651-474M, .47μfd ±20%, 50v dc
Transistors		
200-3053	RCA	2N3053, NPN, Silicon Annular, T0-5
200-3251	Motorola	2N3251, PNP, Switching, T0-18
200-4123	Motorola	2N4123, NPN, Silicon, T0-92
200-4125	Motorola	2N4125, PNP, Silicon, T0-92
200-4400	Motorola	2N4400, NPN, Silicon, T0-92
200-4402	Motorola	2N4402, PNP, Silicon, T0-92
200-5321	RCA	2N5321, NPN, Silicon, T0-5
200-5323	RCA	2N5323, PNP, Silicon, T0-5
200-6051	Motorola	2N6051, PNP, Power Darlington, T0-3
200-6058	Motorola	2N6058, NPN, Power Darlington, T0-3
200-6282	Motorola	2N6282, NPN, Power Darlington, T0-3
200-6285	Motorola	2N6285, PNP, Power Darlington, T0-3

Table 7-5

Part Number Cross Reference (Continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No. * / Description
Field Effect Transistors		
204-0074	National	TIS-74, N-Channel, Switching, T0-106
Diodes		
300-4002	Motorola	IN4002, Rectifier, 1A, 100 PIV, D0-41
300-4446	Components, Inc.	IN4446, Switching, 75PIV, D0-7
Zener Diodes		
300-0475	Motorola	IN4732A, Zener, 4.7v dc ±5%, 1w, D0-41
330-0515	Motorola	IN4733A, Zener, 5.1v dc ±5%, 1w, D0-41
330-1005	Motorola	IN4740A, Zener, 10v ±5%, 1w, D0-41
330-1205	Motorola	IN4742A, Zener, 12v ±5%, 1w
331-0275	Motorola	IN5223B, Zener, 2.7v dc ±5%, 500mw, D0-7
331-0395	Motorola	IN5228B, Zener, 3.9v dc ±5%, 500mw, D0-7
331-0515	Motorola	W5231B, Zener, 5.1v dc ±5%, 500mw, D0-7
331-0605	Motorola	IN5233B, Zener, 6v dc ±5%, 500mw, D0-7
Light Emitting Diode		
301-0055	Optron	OR133W-3, Light Emitting, Infra Red, T0-46
Operational Amplifiers		
400-0307	National	LM307N, IC, Op Amp
400-0319	National	LM319N, IC, Dual Comparator
400-0592	Signetics	NE592A, IC, Op Amp
400-5558	National	LM1458N, IC, Dual Op Amp
Relays		
502-1205	Amer Zett	AZ-535-11-1, 12v dc, SPDT, Contract Rating 5A at 26v dc
502-1242	Allied Control	TF-154-4C-12v dc, 12v dc, 4PDT, Contact Rating 5A at 28v dc
Inductors		
515-1015	Delevan	1537-76, 100µH ±5%, 4.5 ohms
515-3305	Delevan	1537-52, 33µH ±5%, 2.9 ohms
515-6805	Delevan	1537-68, 68µH ±5%, 3.3 ohms
Crystals		
524-0002	Northern Eng Lab	NE12, 10.00 MHz ±.005

Table 7-6
Model T6X40 PCBA Interconnections

Tape Control PCBA	
J1	LOAD Control
J2	ON LINE Control
J3	REWIND Control
J4	WRT EN Indicator
J5	HI DEN Control
J6	FORWARD Control
J7	REVERSE Control
J8	Data E9/E7 PCBA, J1 Data E19/E17 PCBA, J8
J9	Servo and Power Supply PCBA, J9
J10	Servo and Power Supply PCBA, J10
Servo and Power Supply PCBA	
J11	Capstan Drive Assembly
J12	Take-up Reel Motor
J13	EOT/BOT Amplifier
J14	Take-up Reel Tension Arm Sensor
J15	Power Supply
J16	Power Supply
J17	WLO and Limit Switch
J18	Supply Reel Tension Arm Sensor
J19	Supply Reel Motor
Data PCBA	
J1	Write/Erase Head, Data E19/E17 PCBA
J2	Read Head, Data E19/E17 PCBA
J2	Write/Erase Head, Data E9/E7 PCBA
J3	Read Head, Data E9/E7 PCBA
EOT/BOT Amplifier PCBA	
J1	Photo-tab Sensor

Table 7-7

Model T6X60 PCBAInterconnections

Tape Control PCBA	
J1	LOAD Control
J2	ON LINE Control
J3	REWIND Control
J4	WRT EN Indicator
J5	HI DEN Control
J6	FORWARD Control
J7	REVERSE Control
J8	Data D PCBA, J1 Data D1 PCBA, J8
J9	Servo and Power Supply PCBA, J9
J10	Servo and Power Supply PCBA, J10
Servo and Power Supply PCBA	
J11	Capstan Drive Assembly
J12	Take-up Reel Motor
J13	EOT/BOT Amplifier
J14	Take-up Reel Tension Arm Sensor
J15	Power Supply
J16	Power Supply
J17	WLO and Limit Switch
J18	Supply Reel Tension Arm Sensor
J19	Supply Reel Motor
Data PCBA	
J1	(Data D) Pwr/Control, Tape Control, J8
J2	(Data D) Read/Write Head
J1	(Data D1) Read/Write Head
J8	(Data D1) Pwr/Control, TapeControl, J8
EOT/BOT Amplifier PCBA	
J1	Photo-tab Sensor

Table 7-1
T6000 Series Transports Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-1		
-1	604-0600	Nut
-2	615-4210	Spade Bolt
-3	615-0012	Lock Nut
-4	660-0001	Rubber Cushion
-5	101026-01 603-0402	Fixed Guide Assembly Set Screw
-6	100562-01	Capstan
-7	101744-02 101744-03 101744-04 101744-05 101744-06 101744-07	Strobe Disk, 12.5/25.0 ips (60/50 Hz) Strobe Disk, 18.75/37.5 ips (60/50 Hz) Strobe Disk, 20.0/40.0 ips (60/50 Hz) Strobe Disk, 22.5/45.0 ips (60/50 Hz) Strobe Disk, 24.0 ips (60 Hz) Strobe Disk, 30.0 ips (60/50 Hz)
-8	505-*	POWER Switch
-9	505-*	LOAD Switch
-10	505-*	ON LINE Switch
-11	505-*	REWIND Switch
-12	505-*	WRT EN Switch
-13	505-*	HI DEN Switch (NRZI Only) 1600 CPI Switch (PE Only)
-14	505-*	FORWARD Switch
-15	505-*	REVERSE Switch
-16	100810-01 100298-01	Head Guide (Top and Bottom Set) Head Guide Shim
-17	102581-01	Flux Gate (Dual Stack Only)
-18	510-*	Head
-19	100807-01	Photo-tab Sensor Assembly
-20	615-0007	Catch Spring
-21	100808-01	Roller Guide Assembly
-22	100811-01	Tape Cleaner
-23	667-0017	Rubber Strip
-24	101001-01	Stop Block
-25	100997-01	Head Assembly Cover
-26	100923-90	Tension Arm Bearing Housing
-27	101027-01 616-0005 615-9755	Limit Shaft Cover Stop Spring Hitch Pin Clip
-28	103331-01	Pivot Pin
-29	100888-01	Hinge Block (Wht)
-30	100792-01 102261-01	Reel Hub, 37.5 ips and Below Reel Hub, 45.0 ips
-31	100886-01	Tension Arm
-32	100995-01	Tension Arm Spring
-33	615-0553	Spring Plunger
-34	100891-01	Trim Housing
Not Shown	100998-01 101085-01 101117-01 100892-01	Overlay Head Guide Cover (Top) Head Guide Cover (Bottom) Cover Door

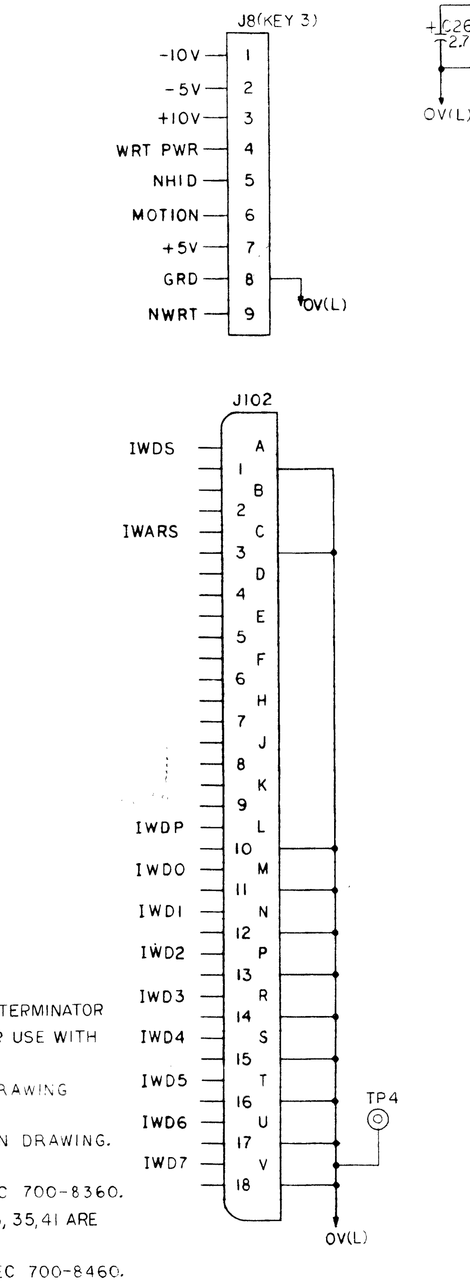
*Refer to Table 7-4 for specific part number.

APPENDIX A — GLOSSARY

Symbol	Description	Symbol	Description
B1B	Buffer 1 Busy	EPNP	Encoder Pulse Narrow Powerful
BCD10	Binary Coded Decimal	EPS	Erase Power Start
BOT	Beginning of Tape	EPW	Encoder Pulse Wide
BOTD	Beginning of Tape Delay	ERASE*	Erase
BOTDP	Beginning of Tape Delay Pulse	ES	Erase Winding Start
BOTI	Beginning of Tape Input	EWPC	Enable Write Power Control
BOTO	Beginning of Tape Output	EWRS	Enable Write/Read Status
BOV*	Buffer Overflow	FAD*	Formatter Address
CBY	Command Busy	FBY*	Formatter Busy
CCG*	Check Character Gate	FEN*	Formatter Enable
CCS	Check Character Strobe	FER*	Formatter Error
CER*	Correctable Error	FGC	File Gap Command
CHARDET*	Character Detect	FGL	File Gap Lamp
CLRNZDATA*	Clear NRZI Data	FGR	File Gap Ramp
CMP1,2	Clamp Waveform 1, 2	FLR	First Load — or Rewind
COPY*	Copy	FM	File Mark
CPI	Characters Per Inch	FMK*	File Mark
CRC0—CRC7	Cyclic Redundancy Check, Ch 0—7	FMKNZ*	File Mark NRZI
CRCC	Cyclic Redundancy Check Character	FMKPE*	File Mark PE
CRCP	Cyclic Redundancy Check Parity	FPT	File Protect
CT0—CT7	Center Tap 0—7	FWD	Forward
CTP	Center Tap Parity	GIP	Gap In Process
CT4	Count 4	GO	Motion signal delayed
CT8	Count 8	GO1*	Go
CUR	Clean-up Ramp	GRS	General Reset
CURLIM	Reel Servo Current Limit	HER*	Hard Error
D8CT	Disables 8 Count	HERNZ*	Hard Error NRZI
DBY	Data Busy	HID	Hi Density
DDI	Data Density Indicator	ID*	Identification
DDS	Data Density Select	IDGATE*	Identification Gate
DDSX	Data Density Select External	INTLK	Transport Interlock Signal
DEN*	Density	IRGC	Record Gap Command
DGATE*	Data Gate	K2ENERG	Relay K2 Energize
DI*	Data In	LD	Lamp Driver
DMC	Disable Manual Controls	LDCRC*	Load Cyclic Redundancy Check
DROPDET*	Drop Detected	LDFAIL	Load Fail
DUN	Done and Unload	LDLOOP	Load Loop
EAO	Encoder Amplifier Output	LDP	Load Point
ECC	Enable Check Character	LDWRTDATA*	Load Write Data
ECD	Echo Check Disable	LFC	Load Forward Command
ECE	Echo Check Error	LFR	Load Forward Ramp
ECLK*	Envelope Clock	LOCK	Interlock off pulse
ECO0—ECO7	Echo Check Output, Ch 0—7	LOCKA	Interlock A
ECOP	Echo Check Output Parity	LOCKB	Interlock B
ECR	Echo Check Reset	LOCKTIME	Locktime pulse
ECRC	Enable CRC	LOL*	Load-On-Line
EDIT*	Edit	LRCC	Longitudinal Redundancy Check Character
EEC	Enable Echo Check	LWD*	Last Word
EEP	Enable Encoder Pulse	MOTION	Tape Motion as result of SFC/SRC Command
EF	Erase Winding Finish	NRZ*	NRZI
EFM	Enable File Mark	OFC*	Off Line Command
ENV*	Envelope Detected	OFFC	Off-Line Input Command
EOT*	End of Tape	OFL*	Off Line
EOTI	End of Tape Input	OLUNL	Off-Line Unload
EOTO	End of Tape Output	ONEDET*	Ones Detected

NOTES:
1. * Microformatter Only
2. I Symbol Prefix = Interface Signal
3. N Symbol Prefix = Low Active Signal

Symbol	Description	Symbol	Description
OOLL	On-Line/Off-Line Lamp	RYC	Ready Command
ORD	ORed Data	SBY	Start Busy Delay
OVW	Overwrite	SFC	Synchronous Forward Command
PARC*	Parity Correcting	SFCD	Synchronous Forward Command Delayed
PICKK1	Pick K-1 Relay	SFL1—SFL4	Step Forward Level 1—4
POSTJUMP*	Postamble Jump	SGL*	Single
POSTEST*	Postamble Test	SHLCLK*	Shift Left Clock
PR*	Parity	SHRCLK*	Shift Right Clock
PRESET*	Preset	SKLP	Seek Load Point
PSEN*	Power Supply Enable	SKTO	Seek Time Out
PSO0—PSO7	Peak Sensor Output, Ch 0—7	SLT	Select Transport
PSOP	Peak Sensor Output Parity	SPC*	Space Command
PSP	Peak Sensor Parity	SPD*	Speed
RA01, RA02	Read Amplifier Track 0, Output 1, Output 2	SRC	Synchronous Reverse Command
RA11, etc.	Read Amplifier Track n, Output 1 or 2	SRO/SRO1	Selected—Ready—On Line
RAC	Read Amplifier Clamp	SWS	Set Write Status
RACT	Read Amplifier Center Tap	TAD	Turnaround Delay
RAP1, RAP2	Read Amplifier Parity, Output 1, Output 2	TAD0, 1*	Transport Address
RCLK*	Read Clock	TBY	Turnaround Busy
RD0—RD7	Read Data, Ch 0—7	TENCNT	Tension Control
RDI	Relay Driver Input	THR*	Read Threshold
RDNZ*	Read NRZI Data	TIP	Tape-In-Place
RDP	Read Data Parity	TNT	Tape Not Tensioned
RDS	Read Data Strobe	TRR	Transport Ready
RDY	Ready	W*	Write Data
REN*	Read Enable	WARS	Write Amplifier Reset
RENDNZ*	Read End NRZI	WCLK*	Write Clock
RENDPE*	Read End PE	WCN*	Write Control
REV	Reverse	WCRC	Write CRC
REW*	Rewind	WD*	Write Data
REW RAMP A	Rewind Ramp Output A	WD0—WD7	Write Data, Ch 0—7
REW RAMP B	Rewind Ramp Output B	WDP	Write Data Parity
REWRI	Rewind Ramp Initiate	WDS	Write Data Strobe
RF0—RF7	Read Finish 0—7	WDSN	Write Data Strobe Narrow
RFP	Read Finish Parity	WDSW	Write Data Strobe Wide
RGATENZ*	Read Gate NRZI	WF0—WF7	Write Finish, Ch 0—7
RGATEPE*	Read Gate PE	WFM	Write File Mark
RGC	Inter-Record Gap Command	WFP	Write Finish Parity
RGR	Inter-Record Gap Ramp	WLO	Write Lockout
RRS	Remote Reset	WDP	Write Power Control
RS1	Rewind Step 1	W/RF0—W/RF7	Write/Read Head Winding Finish, Ch 0—7
RSC*	Read Strobe Counter	W/RFP	Write/Read Heading Winding Finish Parity
RSP	Read Start Parity	WDO	Write/Read Output
RST	Reset	WDP	Write Pulse
RSTR*	Read Strobe	WRS	Write/Read Status
RSTRNZ*	Read Strobe NRZI	W/RS0—W/RS7	Write/Read Head Winding Start, Ch 0—7
RSTRPE*	Read Strobe PE	W/RSP	Write/Read Head Winding Start Parity
RTH	Read Threshold	WRT*	Write
RTN1	Front Panel Switches Gnd Return 1	WRT EN	Write Enable
RW1	Rewind 1 FF	WS0—WS7	Write Start, Ch 0—7
RWC	Rewind Command	WSC	Write Step Command
RWD	Rewinding	WSP	Write Start Parity
RWFWD	Rewind Forward	WSTR*	Write Strobe
RWR	Rewind Ramp		



[11] VERSIONS WITHOUT TERMINATOR RESISTORS ARE FOR USE WITH MTA.

10. FOR ASSEMBLY DRAWING SEE 101711.
    FOR SPECIFICATION DRAWING. SEE 101714.
9. U1,36-40 ARE PEC 700-8360.
   U2,3,5,7,9,11,13,26,35,41 ARE PEC 700-8440.
   U27,30,33 ARE PEC 700-8460.
   U4,6,8,10,12 ARE PEC 700-8530.
   U14-23 ARE PEC 400-1437.
   U28,29,31,32,34 ARE PEC 700-7476(+5V IS PIN 5,0V IS PIN 13).
   U24,25 ARE PEC 700-7496 (+5V IS PIN 5,0V IS PIN 12).
8. PIN 7 OF ALL IC'S IS 0V
   PIN 14 OF ALL IC'S IS +5V.
7. ALL NPN TRANSISTORS ARE PEC 200-4123.
   ALL PNP TRANSISTORS ARE PEC 200-4125.
6. ALL CAPACITORS IN MICROFARADS, 35V, 20%.
5. ALL DIODES ARE PEC 300-4446.
4. ALL RESISTORS IN OHMS, 1/4W, 5%.
3. CIRCUIT 100 IS TYPICAL OF CIRCUIT 200 THRU 900.
2. 3 DIGIT REF NOS. ARE ASSIGNED TO REPETITIOUS CIRCUITS.
   EX: TP101 IS CIRCUIT 100. TP 901 IS CIRCUIT 900. SINGLE DIGIT NOS.
   ARE ASSIGNED TO NON REPETITIVE CIRCUITS. EX: TP1-TP2.
[1] SEE VERSION TABLE FOR VALUE AND USAGE.

NOTES: UNLESS OTHERWISE SPECIFIED:

LAST USED		DELETED	
R934	R56	CR104 THRU 904	
C910	C47	CR106 THRU 906	
Q908	Q12	C1	R8
CR907	CR7		
TP906	TP16		
	U41		
	W1		

VERSION	SPEED (IPS)	R109-909 R108-908	R110-R910	R111-911	R19	R26	R31	R18	R132-932	C104-C904	C106-906 100V, 10%	C107-907 100V, 10%	C109-909 500V, 5%	C6 500V 5%	C10 100V 10%		C44	C103-903 500V, 5%	C101-901	R1,3,101 THRU 901 [11]	R2,4,102 THRU 902 [11]
-01	75	5110	8200	75K	330	3900	3900	10K	22K	15PF	.0015	.001	33PF	150PF	.0015		470PF 500V 5%	33PF	OMIT	USE	USE
-02	75	5110	8200	75K	330	3900	3900	10K	22K	15PF	.0015	.001	33PF	150PF	.0015		470PF 500V 5%	33PF	OMIT	OMIT	OMIT
-03	45	2610	27K	68100	330	10K	10K	20K	18K	22PF	.0022	.0015		220PF	.001		.0015 100V 10%			USE	USE
-04	45	2610		68100	330				18K	22PF	.0022	.0015			.001					OMIT	OMIT
-05	37.5	2610		90900	330				27	22PF	.0033	.0022			.0015					USE	USE
-06	37.5	2610		90900	330				27	22PF	.0033	.0022			.0015					OMIT	OMIT
-07	25	1620		90900	330				27	33PF	.0047	.0033			.0015					USE	USE
-08	25			90900	330				27	33PF	.0047	.0033		220PF	.0015					OMIT	OMIT
-09	18.75			121K	180				39K	33PF	.0068	.0047		330PF	.0022					USE	USE
-10	18.75			121K	180				39K	33PF	.0068	.0047		330PF	.0022					OMIT	OMIT
-11	12.5			178K	180				56K	33PF	.01	.0068		330PF	.0033					USE	USE
-12	12.5	1620		178K	180				56K	33PF	.01	.0068		330PF	.0033					OMIT	OMIT
-13	45	2610		68100	330				18K	22PF	.0022	.0015		220PF	.001					USE	USE
-14	45	2610		68100	330				18K	22PF	.0022	.0015		220PF	.001					OMIT	OMIT
-15	37.5	2610		90900	330				27	22PF	.0033	.0022		220PF	.0015					USE	USE
-16	37.5	2610	27K	90900	330	10K	10K	20K	27	22PF	.0033	.0022	33PF	220PF	.0015		.0015 100V 10%	33PF	OMIT	OMIT	OMIT

TOP ASSY | NEXT ASSY | 1ST USED ON | APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
XX ± .010
XXX ± .005
$\frac{X}{X} \pm \frac{1}{32}$
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX .010

FINISH:

MATL:

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE.

SIGNATURES | DATE
DR | 2/26/70
CHK
DES
ENGR
ENGR | 3/23/71

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC DATA E19 READ AFTER WRITE

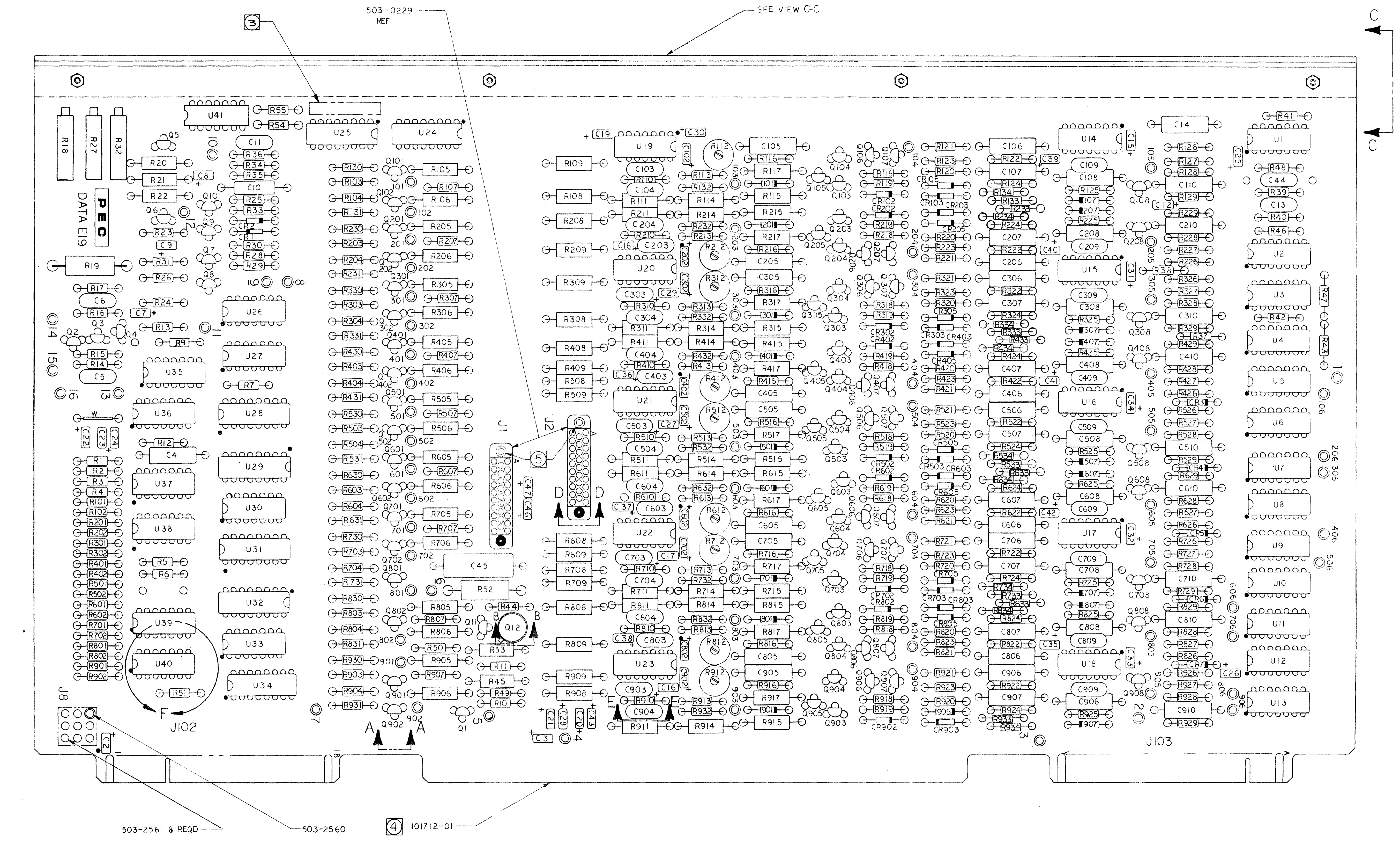
SIZE J | CODE IDENT NO | DWG NO. 101710 | REV J

SCALE — | DO NOT SCALE DWG | SHEET 1 OF 2

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				

VERSION	R50,51	R 56
-01	USE	OMIT
-02		
-03		
-04		
-05		
-06		
-07		
-08		
-09		
-10	USE	OMIT
-11	OMIT	USE
-12	USE	OMIT
-13		
-14		
-15		
-16	USE	OMIT

SIZE	CODE IDENT NO.	DWG NO.	REV
J		101710	J
SCALE —		DO NOT SCALE DWG	SHEET 2 OF 2



7 VERSIONS WITHOUT TERMINATOR RESISTORS ARE FOR USE WITH MTA.

6 FOR PART NO.'S WHICH ARE AFFECTED BY VERSION NO SEE TABLE II.

5 ORIENTATE CONNECTORS J1 AND J2 AS SHOWN.

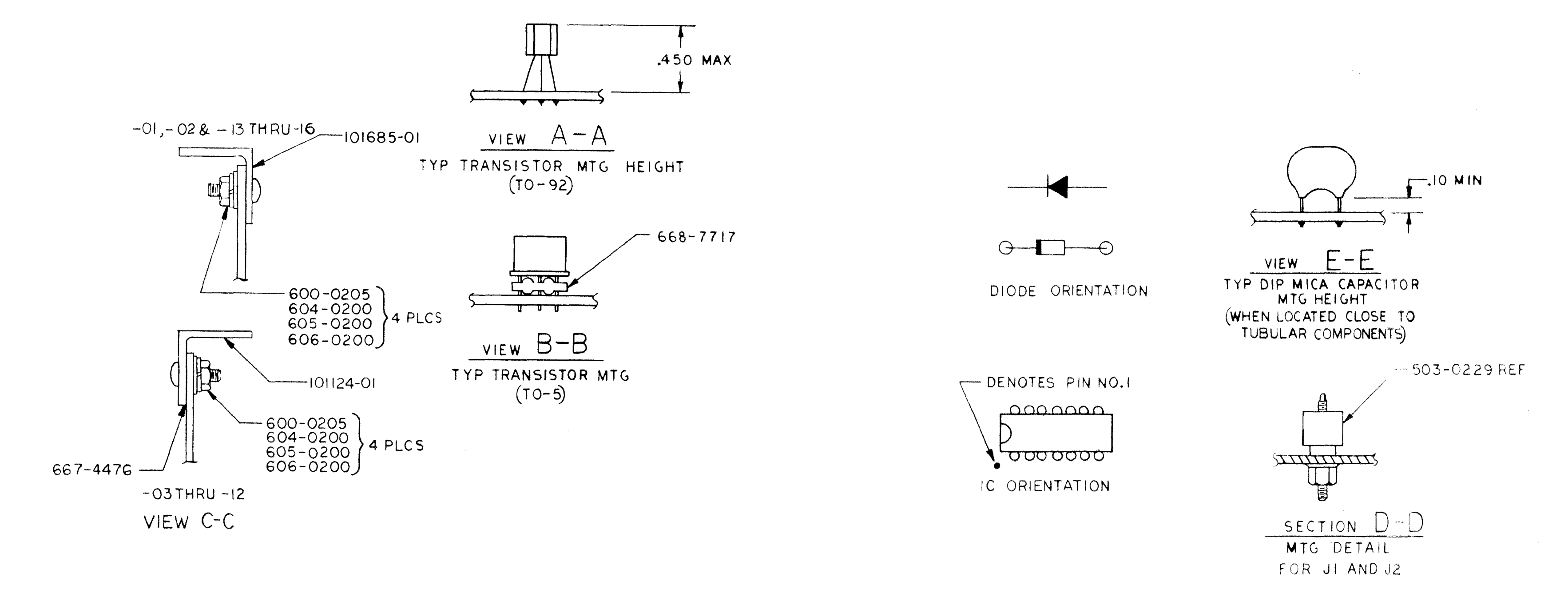
4 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101712-01 REV "F" AND SUBSEQUENT.

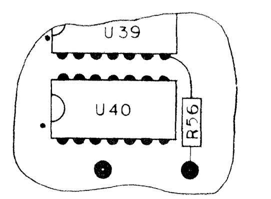
3 MARK PART NO. 101711, INCLUDING VERSION NO. AND VERSION ISSUE LETTER

2. ASSEMBLE PER STANDARD MFG METHODS.

1. REFERENCE DRAWINGS: SCHEMATIC - 101710
SPECIFICATION - 101714

NOTES: UNLESS OTHERWISE SPECIFIED:





DETAIL F
COMP. SIDE
SCALE 4/1
(USED ON -11 ONLY)

REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-CT	19 MAR 1971			
B	ECN 2727A	6-29-71			
C	ECN 2977				
D	ECN 3105A	9/18/72	RAS		
E	ECN 4257	9/18/72	RAS		RCA
F	ECN 4360	11/10/72			
G	ECN 4545	11/13/72			
H	ECN 4824	1/17/73			
J	ECN 4714	7/3/73			
K	ECN 5416	8/22/73			
L	ECN 5745	11/7/73			
M	ECN 6456	7/10/74	CJ		
M1	ECN 6442	7/12/74	CJ		
N	ECN 8117	1/7/76		RK	
P	ECN 9112	11/3/76			
R	ECN 9309	11/23/76			
S	ECN 92[illegible]A	12-15-76	RJ		B.P

TABLE I

PART NO.	REF DESIGNATION
100-1025	R10, 17, 35, 38, 42, 43, 47, 48, 49, 127-927, 23
100-1045	R33, 124-924, 128-928
100-1055	R123-923
100-1225	R103-903, 104-904, 134-934
100-1235	R118-918, 120-920
100-1515	R30, 41
100-1525	R14, 29, 116-916, 125-925
100-1825	R5, 6, 7, 129-929, 54, 55
100-1835	R34
100-2215	R37
100-2225	R12, 24, 39, 119-919 130-930, 131-931
100-3315	R11
100-3325	R13, 25, 28, 40, 107-907
100-3915	R9
100-4715	R15, ,44, 46, 122-922
100-4725	R121-921, 126-926
100-6815	R16
100-8215	R 133-933
100-8225	R113-913
100-2735	R36
101-1015	R45
101-2215	R105-905, 106-906
101-4715	R53
102-1815	R52
104-1002	R115-915, 117-917
104-1101	R22
104-3160	R20
104-3482	R114-914
104-9090	R21
121-5030	R27, 32
123-5020	R112-912

TABLE I (CONT)

PART NO.	REF DESIGNATION
130-1015	C5
130-1005	C11
130-4715	C13
131-1020	C4, 110-910
131-1030	C105-905
131-4720	108-908
131-4730	C45
131-1520	C14
132-2262	C12, 102-902
132-2752	C2, 3, 7-9, 15-43, 46, 47
200-4123	Q3-6, 9, 10, 103-903, 104-904, 106-906, 107-907, 108-908
200-4125	Q1, 2, 7, 8, 11, 101-901, 102-902, 105-905
200-5321	Q12
300-4446	CR1-7, 101-901, 102-902, 103-903, 105-905, 107-907
400-1437	U14-23
700-7476	U28, 29, 31, 32, 34
700-7496	U24, 25
700-8360	U1, 36-40
700-8440	U2, 3, 5, 7, 9, 11, 13, 26, 35, 41
700-8460	U27, 30, 33
700-8530	U4, 6, 8, 10, 12
503-0229	J1, 2
100373-02	W1

TABLE II 6

REFERENCE DESIGNATION	PART NUMBERS															
IPS	75	75	45	45	37.5	37.5	25	25	18.75	18.75	12.5	12.5	45	45	37.5	37.5
VER	-01	-02	-03	-04	-05	-06	-07	-08	-09	-10	-11	-12	-13	-14	-15	-16
R132-932	100-2235	100-2235	100-1835	100-1835	100-2735	100-2735	100-2735	100-2735	100-3935	100-3935	100-5635	100-5635	100-1835	100-1835	100-2735	100-2735
R26, 31	100-3925	100-3925	100-1035	100-1035	100-1035	100-1035	100-1035	100-1035	100-1035	100-1035	100-1035	100-1035	100-1035	100-1035	100-1035	100-1035
R110-910	100-8225	100-8225	100-2735	100-2735	100-2735	100-2735	100-2735	100-2735	100-2735	100-2735	100-2735	100-2735	100-2735	100-2735	100-2735	100-2735
R19	102-3315	102-3315	102-3315	102-3315	102-3315	102-3315	102-3315	102-3315	102-1815	102-1815	102-1815	102-1815	102-3315	102-3315	102-3315	102-3315
R50	100-1025	100-1025	100-1025	100-1025	100-1025	100-1025	100-1025	100-1025	100-1025	100-1025	OMIT	100-1025	100-1025	100-1025	100-1025	100-1025
R108-908, 109-909	104-5111	104-5111	104-2611	104-2611	104-2611	104-2611	104-1621	104-1621	104-1621	104-1621	104-1621	104-1621	104-2611	104-2611	104-2611	104-2611
R111-911	104-7502	104-7502	104-6812	104-6812	104-9092	104-9092	104-9092	104-9092	104-1213	104-1213	104-1783	104-1783	104-6812	104-6812	104-9092	104-9092
R51	100-8215	100-8215	100-8215	100-8215	100-8215	100-8215	100-8215	100-8215	100-8215	100-8215	OMIT	100-8215	100-8215	100-8215	100-8215	100-8215
R18	121-1030	121-1030	121-2030	121-2030	121-2030	121-2030	121-2030	121-2030	121-2030	121-2030	121-2030	121-2030	121-2030	121-2030	121-2030	121-2030
R56	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	100-8215	OMIT	OMIT	OMIT	OMIT	OMIT
C109-909	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305
C104-904	130-1505	130-1505	130-2205	130-2205	130-2205	130-2205	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-2205	130-2205	130-2205	130-2205
C6	130-1515	130-1515	130-2215	130-2215	130-2215	130-2215	130-2215	130-2215	130-3315	130-3315	130-3315	130-3315	130-2215	130-2215	130-2215	130-2215
C103-903	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305	130-3305
C44	130-4715	130-4715	131-1520	131-1520	131-1520	131-1520	131-1520	131-1520	131-1520	131-1520	131-1520	131-1520	131-1520	131-1520	131-1520	131-1520
C10	131-1520	131-1520	131-1020	131-1020	131-1520	131-1520	131-1520	131-1520	131-2220	131-2220	131-3320	131-3320	131-1020	131-1020	131-1520	131-1520
C106-906	131-1520	131-1520	131-2220	131-2220	131-3320	131-3320	131-4720	131-4720	131-6820	131-6820	131-1030	131-1030	131-2220	131-2220	131-3320	131-3320
C107-907	131-1020	131-1020	131-1520	131-1520	131-2220	131-2220	131-3320	131-3320	131-4720	131-4720	131-6820	131-6820	131-1520	131-1520	131-2220	131-2220
R1, 3, 101-901 7	100-2215	OMIT	100-2215	OMIT	100-2215	OMIT	100-2215	OMIT	100-2215	OMIT	100-2215	OMIT	100-2215	OMIT	100-2215	OMIT
R2, 4, 102-902	100-3315	OMIT	100-3315	OMIT	100-3315	OMIT	100-3315	OMIT	100-3315	OMIT	100-3315	OMIT	100-3315	OMIT	100-3315	OMIT

TOP ASSY	6000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR
.XXX ± .005 ± 1/2°
X/X ± 1/32
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

SIGNATURES	DATE
DR	19 MAR 1971
CHK	3/23/71
DES	
ENGR	
ENGR	3/23/71

MATL:

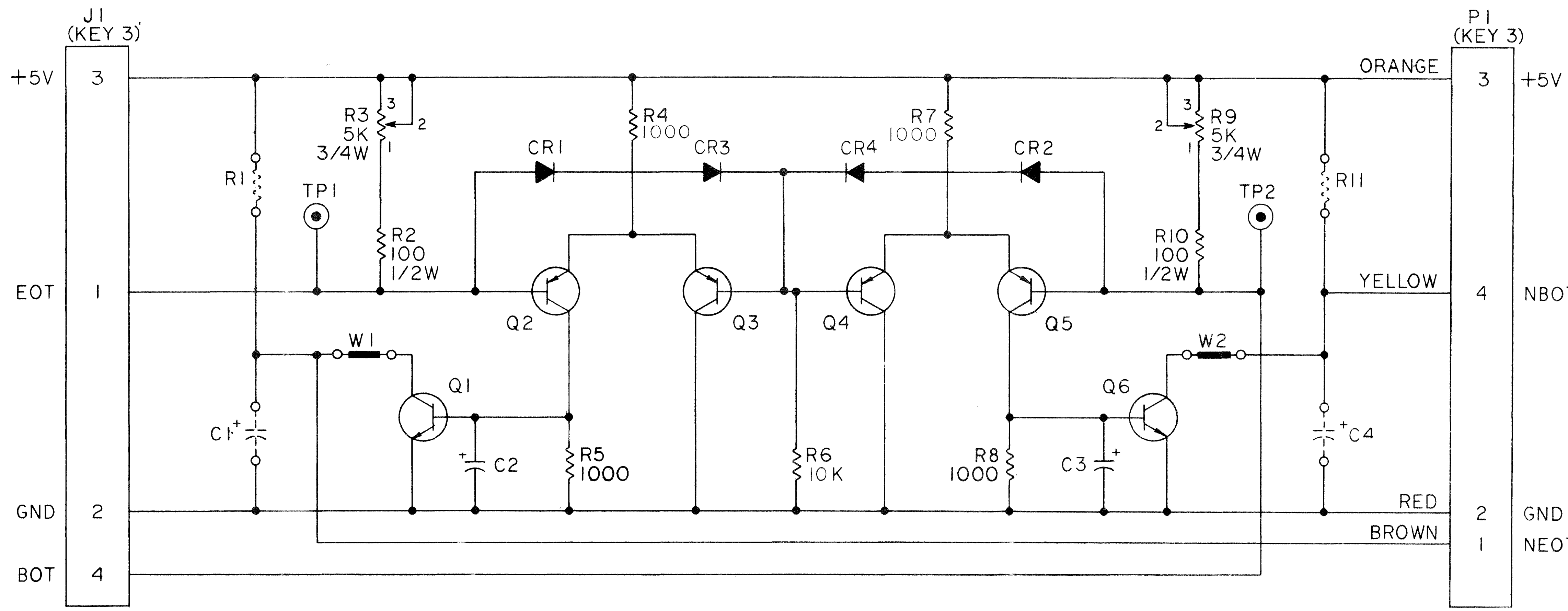
PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA
DATA E19
READ AFTER WRITE

SIZE E | CODE IDENT. NO. | DWG NO. 101711 | REV S

SCALE 2:1 | DO NOT SCALE DWG | SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 2-UG	9/24/70			
B	ECN 4726A	1-10-73			RCA
C	ECN 5105	5-2-73	C.W.		RCA



6. ALL DIODES ARE PEC 300-4446.
5. ALL PNP TRANSISTORS ARE PEC 200-4125.
4. ALL NPN TRANSISTORS ARE PEC 200-4123.
3. ALL RESISTORS ARE 1/4W, ±5%.
2. ALL CAPACITORS ARE 2.7UF, 35V, ±20%.
1. REFERENCE DRAWINGS: ASSEMBLY – 101949
SPECIFICATION – 101952

NOTES: UNLESS OTHERWISE SPECIFIED:

101136	6000
100800	7000
101129	6000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 X/X ± 1/32 ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. 010
FINISH:
MATL:

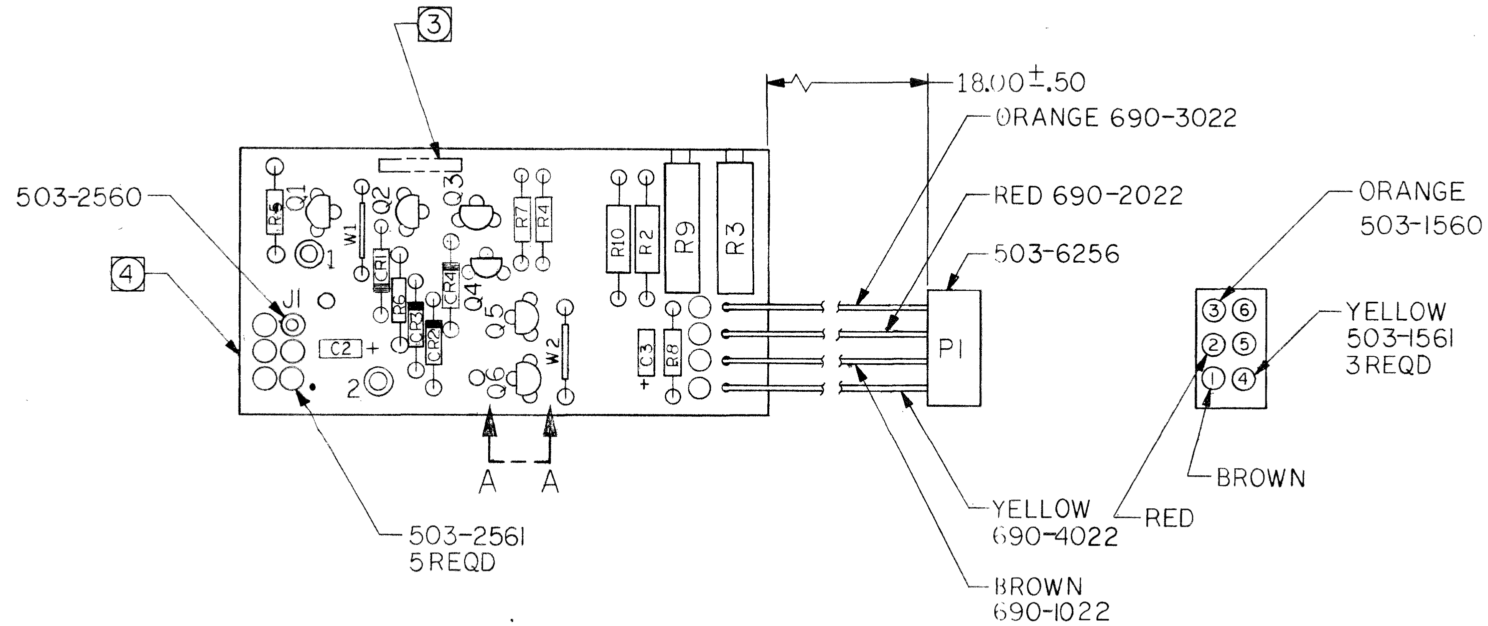
SIGNATURES	DATE
DR L. L. Smith	9/24/70
CHK	9/24/70
DES	
ENGR	9/24
ENGR	9/25/70

PEC PERIPHERAL EQUIPMENT CORPORATION

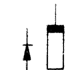
TITLE SCHEMATIC
EOT/BOT AMPLIFIER

SIZE D | CODE IDENT. NO. | DWG NO. 101948 | REV C
SCALE | DO NOT SCALE DWG | SHEET 1 OF 1

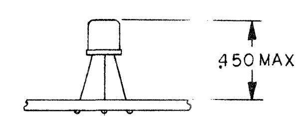
REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ERN 2-UG	5-22-70			
C	ECN 2096	3/25/71	T.B		
D	ECN 4726A	1-10-73	K		
E	ECN 5105	5-2-73	C.W.		
F	ECN 5430	9/12/73			
G	ECN 5703	11/14/73			



PART NO.	REF DESIGNATION
100-1025	R4,5,7,8
100-1035	R6
101-1015	R2,10
121-5020	R3,9
132-2752	C2,3
200-4123	Q1,6
200-4125	Q2,3,4,5
300-4446	CR1,2,3,4
10037302	W1,2



DIODE ORIENTATION



TYP TRANSISTOR MTG HEIGHT
VIEW A-A

PART NO. 101949- REV

4 THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 101950-01 REVG AND SUBSEQUENT.
3 MARK PART NO. 101949 INCLUDING VERSION NO. AND VERSION ISSUE LETTER
2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.
1. REFERENCE DRAWINGS: SCHEMATIC 101948
SPECIFICATION 101952
NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY	1ST USED ON
101136	6000
100800	7000
101129	6000

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 ANGULAR ± 1/2° X/X ± 1/32
BREAK ALL SHARP CORNERS APPROX. .010
FINISH:

SIGNATURES		DATE
DR		9/21/70
CHK		9/24/70
DES		
ENGR		
ENGR		

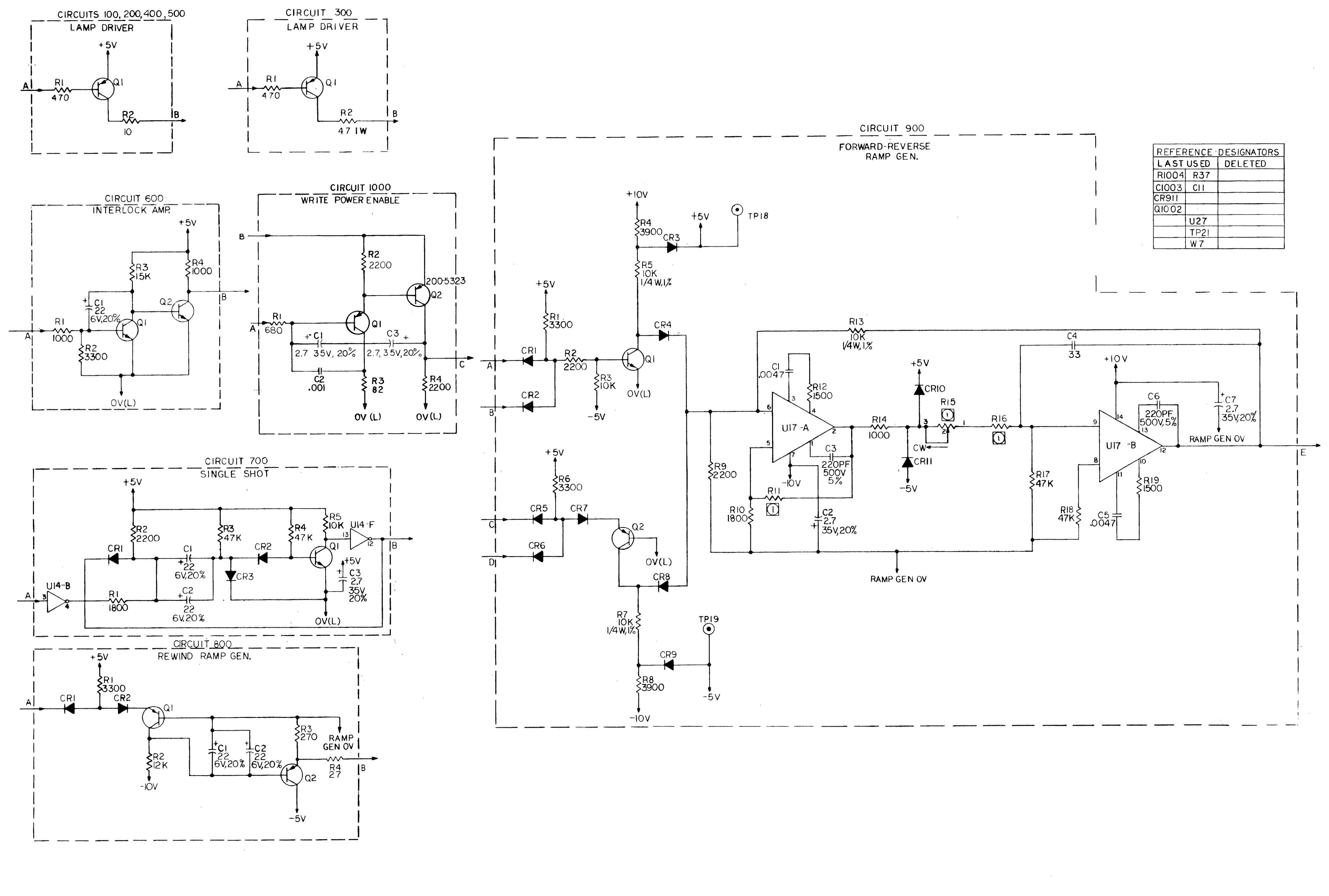
MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA EOT/BOT AMPLIFIER

SIZE	CODE IDENT. NO.	DWG NO.	REV
D		101949	G

SCALE 2/1 DO NOT SCALE DWG SHEET 1 OF 1



[10] VERSIONS WITHOUT TERMINATOR RESISTORS, ARE FOR USE WITH MTA.

9. U4,12,14,15,21,24,27 ARE PEC 700-8360
U2,6,7,8,10,16,19,23,25 ARE PEC 700-8440
U1,5,9,13,18,26 ARE PEC 700-8460
U3,11,20,22 ARE PEC 700-8530
U17 IS PEC 400-1437

8. ON ALL DIGITAL IC'S PIN 14 IS +5V, PIN 7 IS 0V.

7. ALL NPN TRANSISTOR ARE 200-4123, ALL PNP TRANSISTOR ARE 200-4125.

6. ALL DIODES ARE 300-4446.

5. ALL CAPACITORS IN MICROFARADS, 100V, 10%.

4. ALL RESISTORS IN OHMS, 1/2W, 5%.

3. FOR ASSY DWG SEE 101241 FOR SPEC DWG SEE 101244

2. REF DESIGNATORS ARE NOT COMPLETE. FOR COMPLETE DESIGNATIONS ADD CIRCUIT NO. TO DESIGNATOR. FOR EXAMPLE: CR3 OF CIRCUIT 700 IS CR703; R4 OF CIRCUIT 600 IS R604.

[1] SEE VERSION TABLE FOR VALUE

NOTES: UNLESS OTHERWISE SPECIFIED

VERSION TABLE

IPS	MODEL	ASSEMBLY	W1	W2	W3	W4	W5	W6	W7	R37 1/4W,1%	R916 1/4W,1%	R29	R915	R911	R2,4,10,12,16,22,26,32	R3,5,11,13,17,23,27,33
37.5-25.0	HI-DENSITY LOCAL/ON LINE AT BOT SELECT	101241-01	X	X	X			X			21.5K	50K	50K	330K	220	330
	HI-DENSITY LOCAL/ON LINE MIDDLE OF TAPE/SELECT	-02	X		X			X								
	HI-DENSITY LOCAL/SELECT/ON LINE/ON LINE IN MIDDLE OF TAPE	-03	X		X	X		X								
	HI-DENSITY REMOTE/SELECT/ON LINE/ON LINE AT BOT	-04		X	X	X	X	X								
	HI-DENSITY REMOTE/ON LINE AT BOT/SELECT	-05		X	X		X	X								
	HI-DENSITY LOCAL/ON LINE AT BOT/SELECT/ON LINE	-06	X	X	X	X		X								
	HI-DENSITY REMOTE/ON LINE MIDDLE OF TAPE/SELECT	-07			X		X	X								
37.5-25.0	HI-DENSITY REMOTE/ON LINE MIDDLE OF TAPE/SELECT/ON LINE	-08			X	X	X	X								
37.5-24.0	HI-DENSITY LOCAL/ON LINE MIDDLE OF TAPE SELECT	-09	X		X			X	X		21.5K	50K	50K	330K	220	330
		-10														
15.0-10.0	HI-DENSITY LOCAL/ON LINE AT BOT/SELECT	-11	X	X	X					46.4K	51.1K	100K	100K	330K	220	330
	HI-DENSITY LOCAL/ON LINE MIDDLE OF TAPE/SELECT	-12	X		X											
	HI-DENSITY LOCAL/SELECT/ON LINE/ON LINE IN MIDDLE OF TAPE	-13	X		X	X										
	HI-DENSITY REMOTE/SELECT/ON LINE/ON LINE AT BOT	-14		X	X	X	X									
	HI-DENSITY REMOTE/ON LINE AT BOT/SELECT	-15		X	X		X									
	HI-DENSITY LOCAL/ON LINE AT BOT/SELECT/ON LINE	-16	X	X	X	X										
	HI-DENSITY REMOTE/ON LINE MIDDLE OF TAPE/SELECT	-17			X		X									
	HI-DENSITY REMOTE/ON LINE MIDDLE OF TAPE/SELECT/ON LINE	-18			X	X	X									
15.0-10.0	HI-DENSITY LOCAL/ON LINE MIDDLE OF TAPE SELECT	-19	X		X				X	46.4K	51.1K	100K	100K	330K	220	330
		-20														
45	HI-DENSITY LOCAL/ON LINE AT BOT SELECT	-21	X	X	X			X			21.5K	20K	10K	82K	220	330
	HI-DENSITY LOCAL/ON LINE MIDDLE OF TAPE/SELECT	-22	X		X			X								
	HI-DENSITY LOCAL/SELECT/ON LINE/ON LINE IN MIDDLE OF TAPE	-23	X		X	X		X								
	HI-DENSITY REMOTE/SELECT/ON LINE/ON LINE AT BOT	-24		X	X	X	X	X								
	HI-DENSITY REMOTE/ON LINE AT BOT/SELECT	-25		X	X		X	X								
	HI-DENSITY LOCAL/ON LINE AT BOT/SELECT/ON LINE	-26	X	X	X	X		X								
	HI-DENSITY REMOTE/ON LINE MIDDLE OF TAPE/SELECT	-27			X		X	X								
	HI-DENSITY REMOTE/ON LINE MIDDLE OF TAPE/SELECT ON LINE	-28			X	X	X	X								
45	HI-DENSITY LOCAL/ON LINE MIDDLE OF TAPE SELECT	-29	X		X			X	X		21.5K	20K	10K	82K	220	330
		-30														
18.75-15.0	HI-DENSITY LOCAL/ON LINE AT BOT/SELECT	-31	X	X	X					17.8K	51.1K	100K	100K	330K	220	330
	HI-DENSITY LOCAL/ON LINE MIDDLE OF TAPE SELECT	-32	X		X											
	HI-DENSITY LOCAL/SELECT/ON LINE/ON LINE IN MIDDLE OF TAPE	-33	X		X	X										
	HI-DENSITY REMOTE/SELECT/ON LINE/ON LINE AT BOT	-34		X	X	X	X									
	HI-DENSITY REMOTE/ON LINE AT BOT/SELECT	-35		X	X		X									
	HI-DENSITY LOCAL/ON LINE AT BOT/SELECT/ON LINE	-36	X	X	X	X										
	HI-DENSITY REMOTE/ON LINE MIDDLE OF TAPE/SELECT	-37			X		X									
	HI-DENSITY REMOTE/ON LINE MIDDLE OF TAPE/SELECT/ON LINE	-38			X	X	X									
18.75-15.0	HI-DENSITY LOCAL/ON LINE MIDDLE OF TAPE SELECT	101241-39	X		X				X	17.8K	51.1K	100K	100K	330K	220	330

VERSION TABLE

		ASSEMBLY	W1	W2	W3	W4	W5	W6	W7	R37 1/4W,1%	R916 1/4W,1%	R29	R915	R911	R2,4,10,12,16,22,26,32	R3,5,11,13,17,23,27,33
		101241-41	X	X	X			X	X		21.5K	50K	50K	330K	OMIT	OMIT
		-42	X		X			X								
		-43	X		X	X		X								
		-44		X	X	X	X	X								
		-45		X	X		X	X								
		-46	X	X	X	X		X								
		-47			X		X	X								
		-48			X	X	X	X								
		-49	X		X			X	X		21.5K	50K	50K	330K	OMIT	OMIT
		-50														
		-51	X	X	X				X	46.4K	51.1K	100K	100K	330K	OMIT	OMIT
		-52	X		X											
		-53	X		X	X										
		-54		X	X	X	X									
		-55		X	X		X									
		-56	X	X	X	X										
		-57			X		X									
		-58			X	X	X									
		-59	X		X				X	46.4K	51.1K	100K	100K	330K	OMIT	OMIT
		-60														
		-61	X	X	X			X	X		21.5K	20K	10K	82K	OMIT	OMIT
		-62	X		X			X								
		-63	X		X	X		X								
		-64		X	X	X	X	X								
		-65		X	X		X	X								
		-66	X	X	X	X		X								
		-67			X		X	X								
		-68			X	X	X	X								
		-69	X		X			X	X		21.5K	20K	10K	82K	OMIT	OMIT
		-70														
		-71	X	X	X				X	17.8K	51.1K	100K	100K	330K	OMIT	OMIT
		-72	X		X											
		-73	X		X	X										
		-74		X	X	X	X									
		-75		X	X		X									
		-76	X	X	X	X										
		-77			X		X									
		-78			X	X	X									
		101241-79	X		X				X	17.8K	51.1K	100K	100K	330K	OMIT	OMIT

REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	EP 2-XX, B-1529, C-1609, D-1733, E-2026				
	F-2211, G-2209, H-2535, J-2706, K-2829				
L	ECN 2847A (REDRAWN)	10/5/71	T.B	[illegible]	RCA
M	ECN 2848A	10/29/71	T.B	[illegible]	RCA
N	ECN 2873	11/11/71	RAS	[illegible]	RCA
P	ECN 5366 A	3/8/73	[illegible]	[illegible]	[illegible]
P1	ECN 8321	7/3/76	SK	ZK	[illegible]

101241	TOP ASSY
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± 1/2°
.XXX ± .005
X/X ± 1/32
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:
MATL:

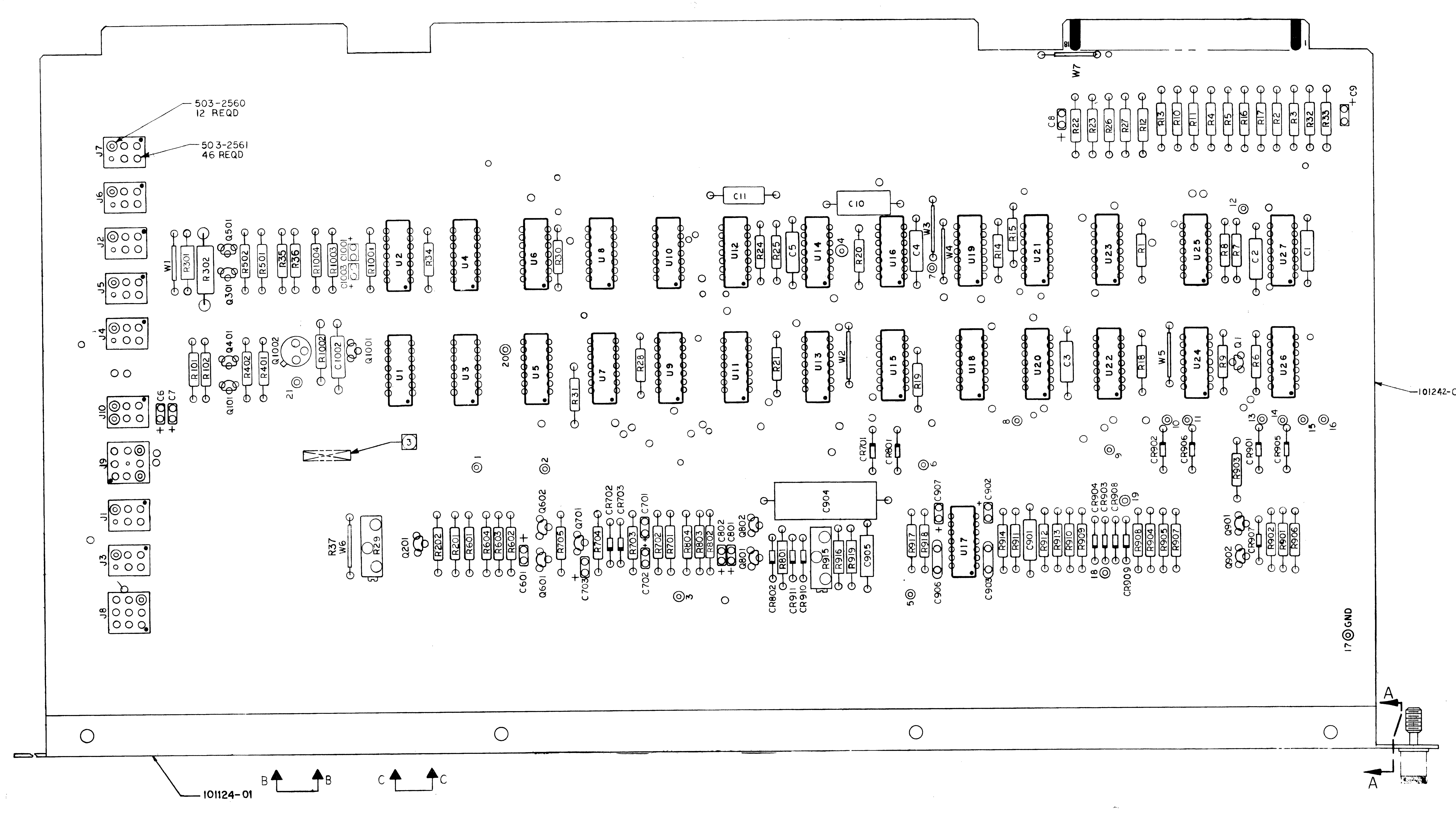
SIGNATURES	DATE
DR	
CHK M. Festejo Jr.	
DES	
ENGR [illegible]	1/12/71
ENGR	

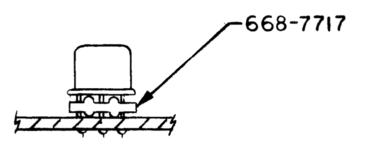
PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC TAPE CONTROL C1

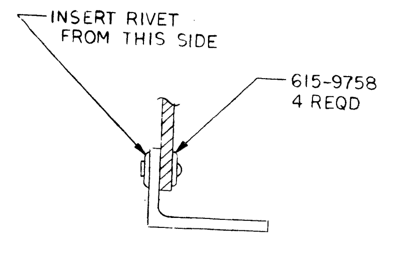
SIZE J | CODE IDENT. NO. — | DWG NO. 101240 | REV P1
SCALE — | DO NOT SCALE DWG | SHEET 1 OF 2


REVISIONS
FORWARD
REVERSE
REWIND
LOAD
J101
J8 (KEY 3)
TO DATA PCBA
J9 (KEY 3-9)
TO SERVO POWER PCBA
J10 (KEY 3-6)
TO SERVO POWER PCBA
FWD REV RAMP GEN
FORWARD-REVERSE RAMP
CKT 100 LAMP DRIVER 1
CKT 200 LAMP DRIVER 2
CIRCUIT 800 REWIND RAMP GEN
REWIND RAMP
CIRCUIT 600 INTERLOCK AMP.
INTERLOCK
HIGH DENSITY
CKT 300 LAMP DRIVER 3
CKT 400 LAMP DRIVER 4
WRT EN
CKT 500 LAMP DRIVER 5
ON LINE
CIRCUIT 700 SINGLE SHOT
CIRCUIT 1000 WRITE POWER ENABLE
WRT PWR
GND
101240
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
H
G
F
E
D
C
B
A

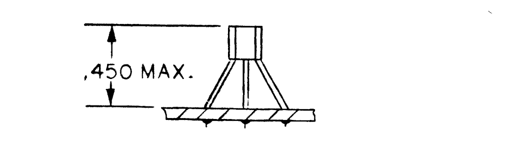




VIEW B-B
CARD SUPPORT ANGLE NOT SHOWN
TYP TO-5 MTG CONFIG.



VIEW A-A



VIEW C-C
ROTATED 90° CW

TABLE I

4

PART NO.	REF DESIGNATION
101-1005	R102,202,402,502,
102-4705	R302
101-1025	R7,9,31,601,604,914
101-1035	R24,705,903
101-1235	R802
101-1515	R6,30
101-1525	R912,919
101-4715	R101,201,301,401,501
101-1535	R25,603
101-1825	R701,910
101-6815	R34,1001
101-2225	R702,902,909,
	R1002,1004
101-2705	R804
101-3325	R602,801,901,906
101-3925	R904,908
101-4725	R1,8,14,15,18,20,21,28
101-4735	R703,704,R917,R918
104-1002	R905,907,913
130-2215	C903,C906
131-1020	C2,3,4,5
131-3340	C904
131-4720	C1,901,905
132-2262	C701,702,801,802,601
132-2752	C6-9,703,902,907
	C1001,1003
200-4123	Q1,602,601,701,901
200-4125	Q101,201,301,401,501,
	801,802,902,1001
300-4446	CR701,702,703,801,
	802,901 THRU 911
101-2715	R19,803
400-1437	U17
700-8360	U4,12,14,15,21,24,27
700-8440	U2,6,7,8,10,16,19,23,25
700-8460	U1,5,9,13,18,26
700-8530	U3,11,20,22
200-5323	Q1002
131-2230	C10
131-6820	C11
131-	
131-1020	C1002
101-8205	R1003
101-1505	R35,36

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 2-KP	11-25-9	CJ		
B	ECN 1508		TK		
C	ECN 1608	5-5-70	TG		
D	ECN 2026	1-18-71	T.K		
E	ECN 2212		T.K		
F	ECN 2333		T.B		
G	ECN 2209		T.		
H	ECN 2706	6-16-71			
J	ECN 2829	9-8-71	T.B		
K	ECN 2847A	9/30/71	TB		
L	ECN 2848A	10/27/71	T.B		RCA
M	ECN 2873	11/11/71	RAS		RCA
N	ECN 3105A	3-15-72	D.C		RCA
P	ECN 3150	3-15-72	D.C		RCA
P1	ECN 5183	7/16/73			RCA
R	ECN 5366A	8/8/73			
S	ECN 5412	8/22/73	J.J.		RCA

7 VERSIONS WITHOUT TERMINATOR RESISTORS ARE FOR USE WITH MTA.

6 THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 101242-01 REVISION 'J' AND SUBSEQUENT

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO., SEE TABLE II ON SHEET 2.

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

3 RUBBER STAMP PART NO. INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC - 101240
SPECIFICATION - 101244

NOTES: UNLESS OTHERWISE SPECIFIED

PART NO. 101241- REV

TOP ASSY	6000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
X/X ± 1/32
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE.

SIGNATURES	DATE
DR Caroline Jones	11-25-9
CHK	
DES	
ENGR	12/10/9
ENGR	

MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA - TAPE CONTROL C1

SIZE	CODE IDENT. NO.	DWG NO.	REV
E	—	101241	S

SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 2

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHT 1	—	TB	—	—

⑤ TABLE II

PART NUMBERS

REFERENCE DESIGNATION / VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09	-10	-11	-12	-13	-14	-15	-16	-17	-18	-19	-20
W 1	100373-01		100373-01			100373-01			100373-01		100373-01		100373-01			100373-01			100373-01	
W 2	100373-01			100373-01		100373-01					100373-01			100373-01	100373-01	100373-01				
W 3	100373-01								100373-01		100373-01								100373 01	
W 4			100373-01	100373-01		100373-01		100373-01					100373-01	100373-01		100373-01		100373-01		
W 5				100373-01	100373-01		100373-01	100373-01						100373-01	100373-01		100373-01	100373-01		
W 6	100373-01								100373-01											
W 7									100373-01										100373-01	
R37											104-4642								104-4642	
R916	104-2152								104-2152		104-5112								104-5112	
R29	121-5030								121-5030		121-1040								121-1040	
R915	121-5030								121-5030		121-1040								121-1040	
R911	101-3345								101-3345		101-3345								101-3345	
R2,4,10,12,16,22 26,32 ⑦	101-2215								101-2215		101-2215								101-2215	
R3,5,11,13,17, 23,27,33 ⑦	101-3315								101-3315		101-3315								101-3315	

REFERENCE DESIGNATION / VER.	-21	-22	-23	-24	-25	-26	-27	-28	-29	-30	-31	-32	-33	-34	-35	-36	-37	-38	-39	-40
W 1	100373-01		100373-01			100373-01			100373-01		100373-01		100373-01			100373-01			100373-01	
W 2	100373-01			100373-01		100373-01					100373-01			100373-01	100373-01	100373-01				
W 3	100373-01								100373-01		100373-01								100373-01	
W 4			100373-01	100373-01		100373-01		100373-01					100373-01	100373-01		100373-01		100373-01		
W 5				100373-01	100373-01		100373-01	100373-01						100373-01	100373-01		100373-01	100373-01		
W 6	100373-01								100373-01											
W 7									100373-01										100373-01	
R37											104-1782								104-1782	
R916	104-2152								104-2152		104-5112								104-5112	
R29	121-2030								121-2030		121-1040								121-1040	
R915	121-1030								121-1030		121-1040								121-1040	
R911	101-8235								101-8235		101-3345								101-3345	
R2,4,10,12,16,22 26,32 ⑦	101-2215								101-2215		101-2215								101-2215	
R3,5,11,13,17, 23,27,33 ⑦	101-3315								101-3315		101-3315								101-3315	

REFERENCE DESIGNATION / VER.	-41	-42	-43	-44	-45	-46	-47	-48	-49	-50	-51	-52	-53	-54	-55	-56	-57	-58	-59	-60
W 1	100373-01		100373-01			100373-01			100373-01		100373-01		100373-01			100373-01			100373-01	
W 2	100373-01			100373-01		100373-01					100373-01			100373-01	100373-01	100373-01				
W 3	100373-01								100373-01		100373-01								100373-01	
W 4			100373-01	100373-01		100373-01		100373-01					100373-01	100373-01		100373-01		100373-01		
W 5				100373-01	100373-01		100373-01	100373-01						100373-01	100373-01		100373-01	100373-01		
W 6	100373-01								100373-01											
W 7	100373-01								100373-01		100373-01								100373-01	
R37											104-4642								104.4642	
R916	104-2152								104-2152		104-5112								104-5112	
R29	121-5030								121-5030		121-1040								121-1040	
R915	121-5030								121-5030		121-1040								121-1040	
R911	101-3345								101-3345		101-3345								101-3345	
R2,4,10,12,16, 22,26,32 ⑦	OMIT								OMIT		OMIT								OMIT	
R3,5,11,13,17 23,27,33 ⑦	OMIT								OMIT		OMIT								OMIT	

REFERENCE DESIGNATION / VER.	-61	-62	-63	-64	-65	-66	-67	-68	-69	-70	-71	-72	-73	-74	-75	-76	-77	-78	-79	-80
W 1	100373-01		100373-01			100373-01			100373-01		100373-01		100373-01			100373-01			100373-01	
W 2	100373-01			100373-01		100373-01					100373-01			100373-01		100373-01				
W 3	100373-01								100373-01		100373-01								100373-01	
W 4			100373-01	100373-01		100373-01		100373-01					100373-01	100373-01		100373-01		100373-01		
W 5				100373-01	100373-01		100373-01	100373-01						100373-01	100373-01		100373-01	100373-01		
W 6	100373-01								100373-01											
W 7	100373-01								100373-01		100373-01								100373-01	
R37											104-1782								104-1782	
R916	104-2152								104-2152		104-5112								104-5112	
R29	121-2030								121-2030		121-1040								121-1040	
R915	121-1030								121-1030		121-1040								121-1040	
R911	101-8235								101-8235		101-3345								101-3345	
R2,4,10,12,16, 22,26,32 ⑦	OMIT								OMIT		OMIT								OMIT	
R3,5,11,13,17 23,27,33 ⑦	OMIT								OMIT		OMIT								OMIT	

PEC	PERIPHERAL EQUIPMENT CORPORATION
TITLE	PCBA TAPE CONTROL CI
SIZE	E
CODE IDENT. NO	
DWG NO.	101241
REV	S
SCALE	NONE
DO NOT SCALE DWG	SHEET 2 OF 2

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ERN 2-VP	10770	T.B.	[illegible]	[illegible]
C	ECN 2173	1/25/71	T.B	[illegible]	[illegible]
D	ECN 2317A	1/25/71	T.B	[illegible]	[illegible]
E	ECN 2350	2/12/71	T.B	[illegible]	GBR
F	ECN 2361B	2/12/71	T.B	[illegible]	GBR
G	ECN 2370A	2/14/71	T.B	[illegible]	GBR
H	ECN 2374A	2/24/71	T.B	[illegible]	GBR
J	ECN 2424A	3/4/71	T.B	[illegible]	GBR
K	ECN 2425	3/12/71	[illegible]	[illegible]	GBR
L	ECN 2680	11/4/71	DC	[illegible]	RCA
M	ECN 2821	12/21/71	DC	JBR	RCA
N	ECN 3167	12/21/71	DC	JBR	RCA
P	ECN 4528	11-27-72	DC	JBR	RCA
R	ECN 6139	[illegible]	RAS	[illegible]	[illegible]
S	ECN 6483B	[illegible]	[illegible]	JBR	[illegible]
T	ECN 6563	8/14/74	[illegible]	JBR	[illegible]
U	ECN 7049	[illegible]/75	[illegible]	JBR	[illegible]

11. ALL 1/2 WATT RESISTORS ARE 5%.
10. ALL CAPACITOR VALUES ARE IN MICROFARADS.
9. ALL IC'S ARE PEC 400-1437.
8. ⬡ INDICATES TRANSISTOR MOUNTED HEATSINK.
7. ◇ INDICATES TRANSISTORS MOUNTED ON EXTRUDED HEATSINK, QTY 12 REQD.
6. ON ALL IC'S PINS 14 & 15 ARE +10V; PINS 7 & 15 ARE -10V.
5. ALL NPN TRANSISTORS ARE 200-4123; ALL PNP TRANSISTORS ARE 200-4125
4. ALL DIODES ARE 300-4446.
3. ALL CAPACITORS 100V, 10%.
2. ALL RESISTORS IN OHMS 1/4 WATT, 5%.
1. FOR ASSEMBLY DRAWING SEE 101262. FOR SPECIFICATION DRAWING SEE 101265.

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DESIGNATIONS	
LAST USED	DELETED
R154	CR4,5,10,11
C60	W1,2
CR30	C5,26,37
SCR1	C49,50,40,41
Q57	C45,46
U3	
TP19	
K1	

101262	6000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 X/X ± 1/32 ANGULAR ± 1/2° ✓
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE

SIGNATURES	DATE
DR John [illegible]	7/24/70
CHK [illegible]	10/29/70
DES	
ENGR [illegible]	[illegible]
ENGR [illegible]	

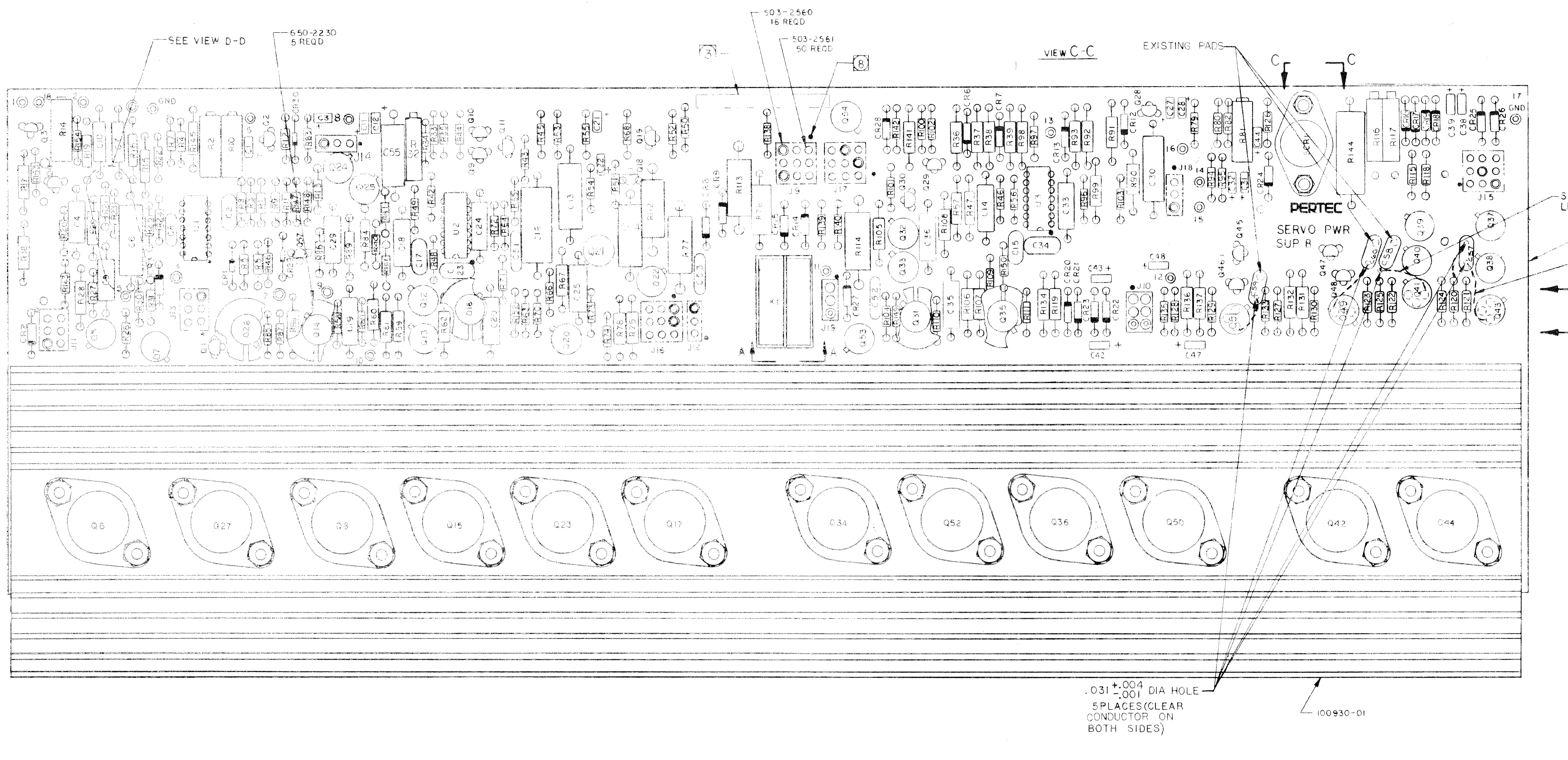
MATL:

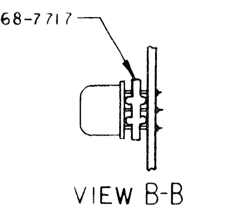
PEC PERIPHERAL EQUIPMENT CORPORATION

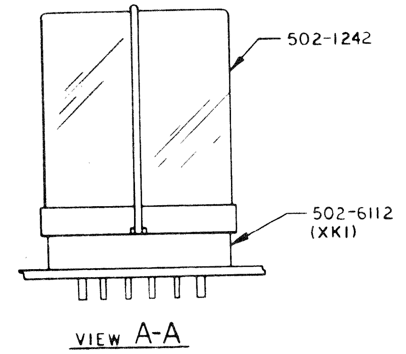
TITLE SCHEMATIC SERVO POWER SUPPLY "B"

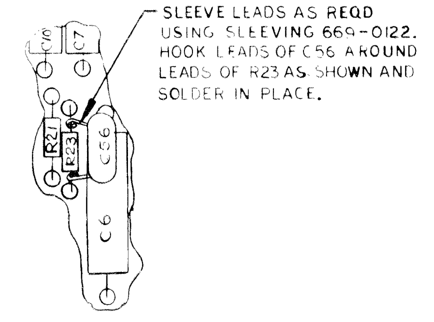
SIZE J | CODE IDENT NO. | DWG NO. 101261 | REV U

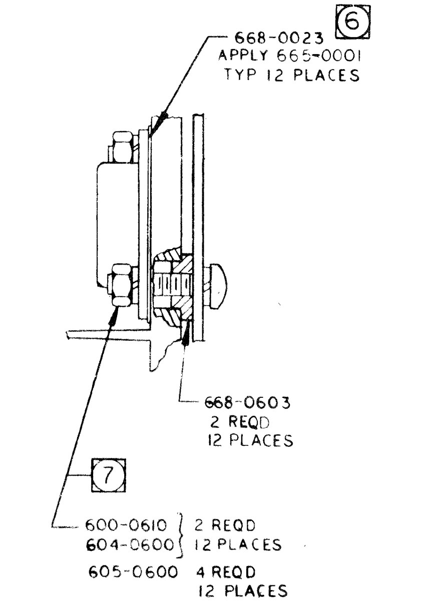
SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1

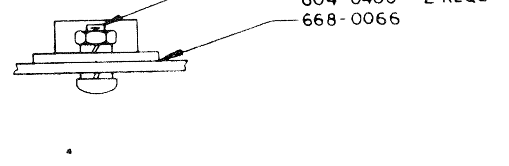


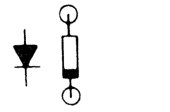


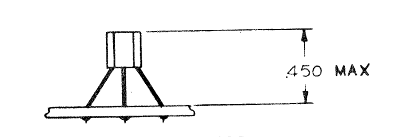









DIODE ORIENTATION



TYPICAL TRANSISTOR
MTG HEIGHT (TO-92)

NOTES: UNLESS OTHERWISE SPECIFIED

1. REF DWGS: SCHEMATIC - 101261
   SPECIFICATION - 101265
2. ASSEMBLE PER STANDARD MANUFACTURING METHODS
3. [3] RUBBER STAMP PART NO., INCLUDING VERSION NO. AND VERSION ISSUE LETTER.
4. [4] FOR PART NO.S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I
5. [5] THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101263-01 REV _ AND SUBSEQUENT.
6. [6] MINIMUM OF 90% COVERAGE REQD ON ALL TRANSISTORS ON HEATSINK, WITH 665-0001 SILICONE GREASE APPLIED BOTH SIDES OF MICA WASHERS. ALL SCREWS 600-0610 MUST BE TORQUED 12 IN. LBS. (TYP 12 PLACES).
7. [7] BEFORE INSTALLING TRANSISTORS TO HEATSINK EXTREME CARE MUST BE TAKEN TO SEE THAT ALL BURRS AND MISC. CHIPS OF METAL ARE WIPED OFF ENTIRE MOUNTING SURFACE.
8. [8] DOT INDICATES PIN 1 ON CONNECTORS AND IC'S.

TABLE I [4]

PART NO.	REF DESIGNATION
100-1015	R1,9,35,80,149-154
100-5605	R27,31,69,70,110,111
100-2215	R143
100-1035	R34,64,71,79,146,40
100-1225	R127,128
100-1245	R41
100-1515	R11,142
100-1525	R25,46,49,72,96
100-1545	R8
100-1825	R30,63,52,85,109, R123,43,101
100-2225	R50,51,138
100-4735	R20
100-3345	R54,94,21,23
115-0002	R144
100-3925	R7
100-4725	R3,22,53,103,
100-1535	R 42
100-5645	R24
100-5625	R44,65,102,147,148
100-6835	R55,95
100-5615	R140
100-6815	R26,104,126,139,58,66
100-8215	R13,120,121,122
101-1215	R119,134
101-1025	R28,60,106
101-4715	R59,62,105,108
103-1525	R112,113
115-0003	R77,114
104-1001	R57,98
104-1101	R19
104-1211	R75,88
104-1472	R99,47
104-1621	R131,137
104-6190	R132,136
104-7501	R78,89
104-1102	R15
104-1332	R18
104-1961	R145

TABLE I (CONT)

PART NO.	REF DESIGNATION
104-2872	R16
104-2871	R38,92
104-3831	R37,91
102-0335	R76
121-1020	R116,117
121-2030	R32,81
121-5020	R2,10,14
130-1015	C2,
130-2215	C8,15,17,23,34
131-1020	C9,10
131-1540	C16
131-4720	C7,14,18,24,33
131-4730	C6,
131-6820	C19,20,25,29,35, 36
132-2262	C11,27
132-2752	C1,3,21,22,31,32,38, 39,42,43,44,47,48
100-1845	R48
100-1025	R4,6,12,56,68,97
100-2205	R73,86
100-4715	R83,129,130
101-1015	R29,61,107
101-2725	R67,84
200-3053	Q12,21,22,32,37,38, 41,53,54,49
200-3055	Q23,27,42,44,50,52
200-5323	Q14,31,5,20
200-3771	Q6,8
200-3772	Q15,17,34,36,
200-4123	Q1,2,3,9,10,19,28,29, 45,46,57
200-4125	Q4,11,18,30,47,48,
200-4037	Q13,51,24,25,33,39 40,43
200-5321	Q16,35,26,7
132-1262	C12,28
131-3330	C54,55
130-1015	C2

TABLE I (CONT)

PART NO.	REF DESIGNATION
300-4002	CR2,3,8,9,14,15,22,23
300-4446	CR1,6,7,12,13,17,18,20 21 25 26 27 28 29 30
201-3228	SCR1
330-0685	CR16,19,24,
131-6830	C13,30
100-6825	R5,33,45,82,100,115, 118
101-6805	R141
104-2371	R17
104-5621	R36,39,90,93
135-4741	C51,52
502-1242	K1
502-6113	XK1
400-1437	U1,2,3
100-5605	R27,31,69,70,110,111
100-3305	R74,87,124,125,133,135
135-4740	C53

TABLE I (CONT)

PART NO.	REF DESIGNATION
130-4715	C56
131-1030	C4
135-1002	C57, 58, 59, 60,

REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ERN 2-VP	[illegible]	[illegible]	[illegible]	RA.H
C	ECN 2172	1/21/71	T.B	[illegible]	[illegible]
D	ECN 2317A	1/21/71	T.B	[illegible]	[illegible]
E	ECN 2351A	2/12/71	T.B	[illegible]	GBR
F	ECN 2361A	[illegible]	T.B	[illegible]	GBR
G	ECN 2370A	[illegible]	T.B	[illegible]	GBR
H	ECN 2376B	2/26/71	T.B	[illegible]	GBR
J	ECN 2424A	3/4/71	T.B	[illegible]	GBR
K	ECN 2395	3/15/71	T.B	[illegible]	GBR
L	ECN 2592	5/19/71	T.B	[illegible]	GBR
M	ECN 2680	11/4/71	DC	[illegible]	RCA
N	ECN 3167	12/23/71	DC	GBR	RCA
P	ECN 3777	6/2/72	C.J.	[illegible]	RST
R	ECN 4528	10/11/72	CJ	GBR	RCA
S	ECN 4410	12/13/72	J.M.	GBR	RCA
S1	ECN 5182	7/10/73	MAL	[illegible]	[illegible]
T	ECN 5322	7/25/73	[illegible]	[illegible]	[illegible]
U	ECN 6069	3/6/74	[illegible]	GJR	[illegible]
V	ECN 6139	3/14/74	RAS	[illegible]	[illegible]
W	ECN 6483B	7/10/74	[illegible]	GJR	[illegible]
Y	ECN 6563	8/14/74	[illegible]	GJR	[illegible]
Z	ECN 7049	1/20/75	[illegible]	GJR	[illegible]
AA	ECN 7782	9/24/75	GJR	[illegible]	[illegible]

PART NO. 101262- REV

TOP ASSY	6000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
X/X ± 1/32
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

SIGNATURES	DATE
DR Livingston	7-30-70
CHK [illegible]	10/12/70
DES	
ENGR [illegible]	[illegible]
ENGR [illegible]	

MATL:

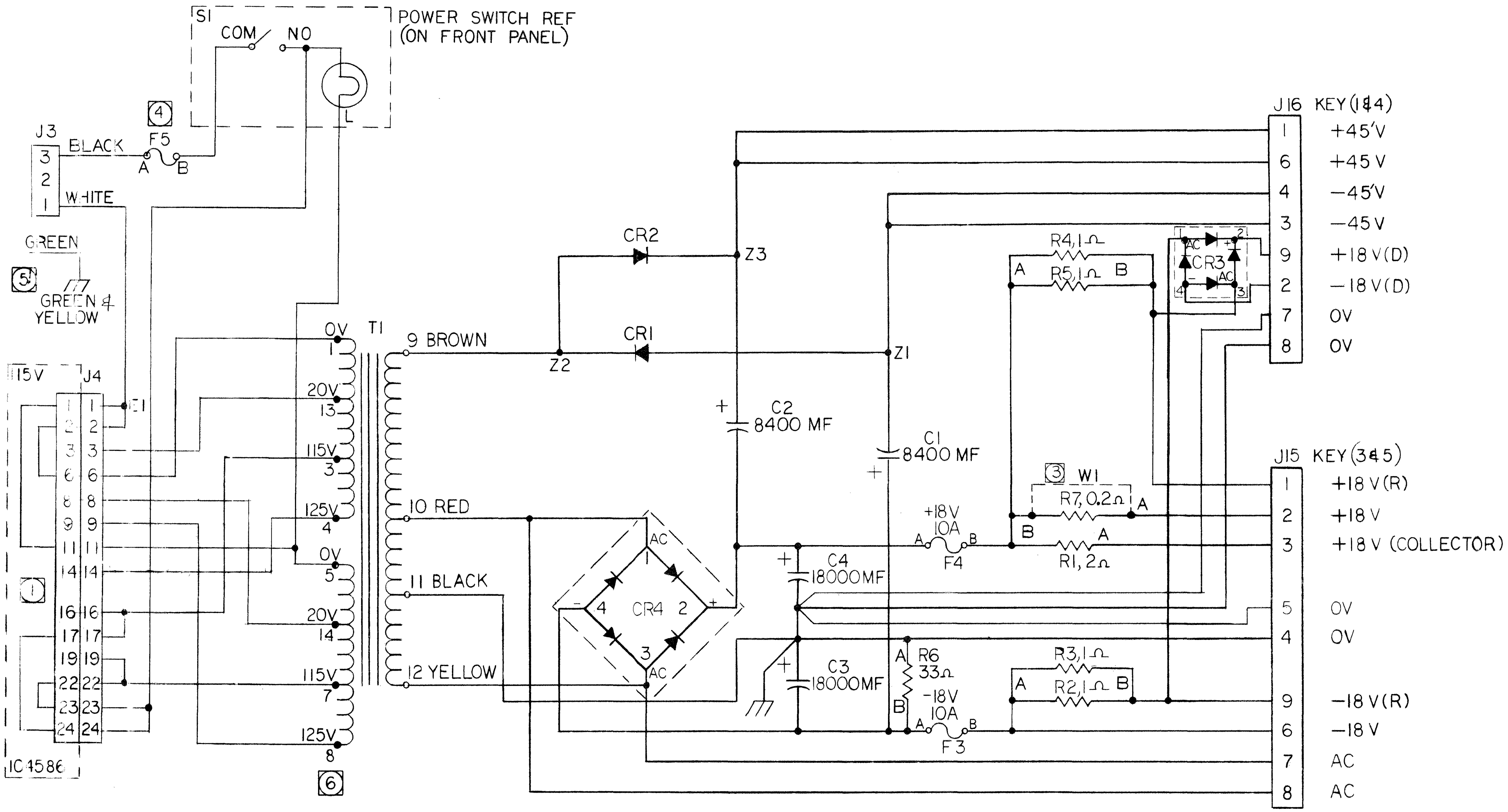
PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA-
SERVO/POWER SUPPLY 'B'

SIZE E | CODE IDENT. NO. | DWG NO. 101262 | REV AA
SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

H
G
A
2
1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 2-GR	8-1-69	EMS	[illegible]	BA
B	ECN 2194	1/13/71	GB	[illegible]	GBR
C	ECN 2367	3-23-71	[illegible]	[illegible]	GBR
D	ECN 2746 A	7-13-71	T.B	[illegible]	GBR
E	ECN 3362	6/29/72	RAS	[illegible]	RCA
F	ECN 5299	7/16/73	[illegible]	[illegible]	[illegible]
G	ECN 7498	8/6/75	GR	WH.	CP.
H	ECN 7691	9/10/75	GJR	WH	CP.
J	ECN 7778 A	10/1/75	AU	WH	CP.
K	ECN 10116	6/22/77	[illegible]	[illegible]	BP



1 TABLE I

VOLTAGE VARIATIONS	
LINE VOLTS	USE CODED PLUG
95	104586 - 01
105	- 02
115	- 03
125	- 04
190	- 05
200	- 06
210	- 07
220	- 08
230	- 09
240	- 10
250	104586 - 11

VERSION	SPEED	W1
01	≤40 IPS	OMIT
02	>40 IPS	USE

7 FOR WIRE LIST, SEE DRAWING NO. 104773.

6 10V TAPS ARE NOT USED.

5 THESE COLORS APPLY FOR EUROPEAN POWER CORD.

4 SEE TOP ASSY FOR FUSE RATING. FUSE IS 5 AMPS AT 115 VAC AND 3 AMPS AT 240 VAC.

3 T6000 45 IPS ONLY.

2. ALL RESISTORS ARE 20W, 5%

1 FOR TRANSFORMER PRIMARY CONNECTIONS SEE TABLE I. (115V SHOWN) LAMP IS ALWAYS CONNECTED ACROSS 115 VAC.

NOTES: UNLESS OTHERWISE SPECIFIED

100990	6000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 $\frac{X}{X} \pm \frac{1}{32}$ ANGULAR $\pm 1/2°$
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

SIGNATURES	DATE
DR E. Stange	8-1-69
CHK W. Kemp	1/22/71
DES	
ENGR [illegible]	[illegible]
ENGR	

MATL:

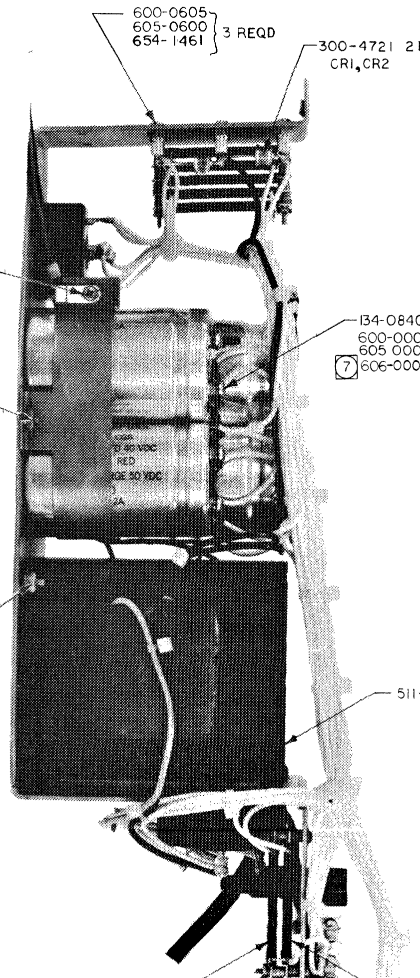
PEC PERIPHERAL EQUIPMENT CORPORATION

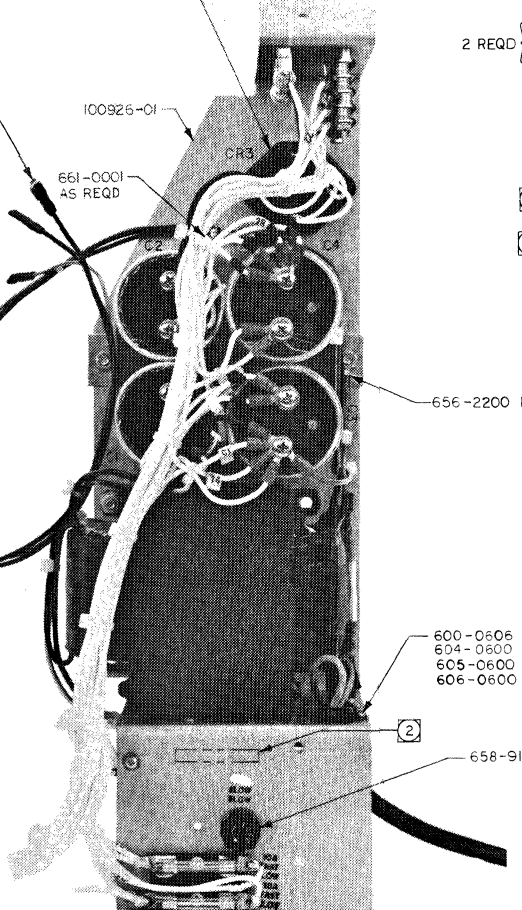
TITLE SCHEMATIC - POWER SUPPLY 6000

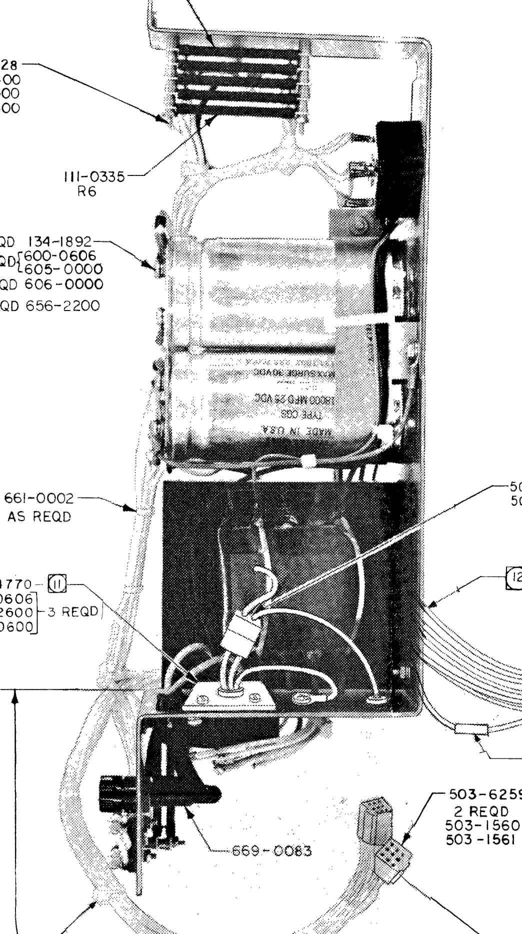
SIZE D | CODE IDENT. NO. | DWG NO. 101132 | REV K

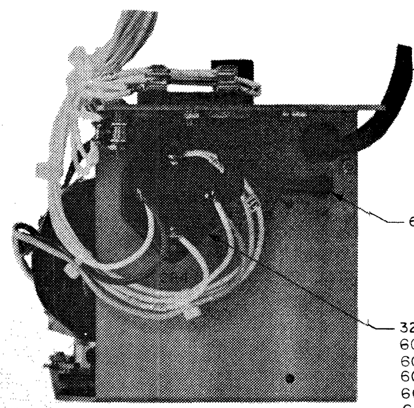
SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1

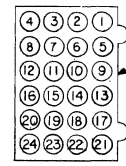
REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	A I-YZ, B ECN787, C ECN923				
	D ECN 1033, E ECN 1159, F ECN 1452, G ECN 1546, H ECN 2137, J ECN 2193 K ECN 2367				
L	ECN 2748 REPLACES REV K WITH CHANGES	7-2-71	HLL		ABR
M	ECN 3622	6/29/72	RAS		RCA
N	ECN 5299	7/16/73			
P	ECN 7081	3/12/75			
R	ECN 7691	9/10/75	GJR		CP
S	ECN 7778 A	10-1-75			CP
T	ECN 10116	6/22/77			BP











J4
PIN INSERTION END
VIEW OF CONNECTOR

13 FOR WIRE LIST SEE DRAWING NO 104773

12 SEE TABLE I ON SCHEMATIC 101132 FOR VOLTAGE CONNECTION.

11 SEE SALES ORDER FOR APPLICABLE VERSION NO.

10 SEE SHEET 2 FOR DETAILS

9 SEE TOP ASSEMBLY FOR FUSE RATING.

8 STAMP 1/8 CHARACTERS APPROX AS SHOWN WITH ACME PERMI-DRI INK #177

7 DUE TO THE IRREGULARITY IN THE DEPTH OF THE TAPPED HOLES IN THE CAPACITORS IT MAY BE NECESSARY TO PUT EXTRA FLAT WASHERS (P/N 606-0000) UNDER THE HEADS OF THE SCREWS TO KEEP THEM FROM BOTTOMING OUT (SHIM A/R)

6 USE TIE WRAP P/N 661-0002 FOR WIRE ROUTING AS REQD.

5 ALL WIRE LENGTHS AS REQD.

4 REMOVE HARDWARE FURNISHED WITH ITEMS AND REPLACE WITH DESIGNATED HARDWARE.

3 ASSEMBLE PER STANDARD MFG. METHODS.

2 RUBBER STAMP ASSY. NO. AND LATEST REVISION LETTER 1/8 HIGH, COLOR: BLACK, NEARSIDE

1. PART NO. TO BE 100990 & REV LETTER

NOTES: UNLESS OTHERWISE SPECIFIED

100999-01	6000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR
.XXX ± .005 ± 1/2°
X/X ± 1/32
BREAK ALL SHARP CORNERS APPROX. .010
FINISH:

SIGNATURES	DATE
DR E. STABER	4-3-69
CHK	
DES J R BAEHNE	5/26/69
ENGR BEN ALIAMS	5/22/69
ENGR EMD	5/22/69

MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE ASSEMBLY, POWER SUPPLY

SIZE E | CODE IDENT. NO. | DWG NO. 100990 | REV T
SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1

pg 2 - var 1 m

PCC PERTEC
a division of Pertec Computer Corporation
9600 Irondale Avenue, Chatsworth, California 91311, Phone (213) 882-0030, TWX (910) 494-2093