MODEL FT7640
FORMATTED
TAPE TRANSPORT

PCC
PERTEC
COMPUTER
CORPORATION
PERTEC DIVISION

FOREWORD

This manual provides operating and service instructions for the Synchronous Read After Write Formatted Tape Transport, Model FT7640-9F, manufactured by PCC PERTEC, Chatsworth, California.

The content includes a detailed description, specifications, installation instructions, and checkout of the transport. Also included is the theory of operation and preventive maintenance instructions. Section VII contains photo parts lists and schematics.

The Microformatter Addendum includes a functional block diagram of a dual microformatter, with supporting text. A fault isolation procedure is given to isolate faults between the microformatter and the tape transport. Also included is the theory of operation and fault isolation to a stage of the microformatter power regulator.

MODEL NO. FT7640

SERIAL NO. 3841000329

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TAPE TRANSPORT

PCC PERTEC

a division of Pertec Computer Corporation

9600 IRONDALE AVENUE, CHATSWORTH, CA 91311

OPERATING AND SERVICE MANUAL NO. 104922

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SERVICE AND WARRANTY

This PERTEC product has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected wherever possible from manufacturer's off-the-shelf stock. Should a component fail, it may be readily replaced from PERTEC or your local supplier. The unit has been designed for plug-in replacement of circuit boards or major components which will ensure a minimum of equipment down time.

PERTEC warrants products of its manufacture to be free from defect in design, workmanship, and material under normal use and service for a period twelve (12) months, or in the case of flexible disk products 120 days, after the date of shipment. PERTEC agrees to repair or replace at its authorized repair center, without charge, all defective parts in systems which are returned for inspection to said center within the applicable warranty period; provided such inspection discloses that the defects are as specified above, and provided further the equipment has not been altered or repaired other than with authorization from PERTEC and by its approved procedures, not been subjected to misuse, improper maintenance, negligence or accident, damaged by excessive current or otherwise had its serial number or any part thereof altered, defaced or removed. All defective items released hereunder shall become the property of seller. THIS WARRANTY IS IN LIEU OF, AND BUYER WAIVES, ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THOSE OF MERCHANTABILITY OR FITNESS FOR PURPOSE.

Please read the instruction manual thoroughly as to installation, operation, maintenance, and component reference list. Should you require additional assistance in servicing this equipment, please contact PERTEC SERVICE — our trained service staff will be pleased to assist you.

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SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides a physical description, functional description, and specifications for the Synchronous Read After Write Tape Transport, Model T7640, manufactured by PCC PERTEC, Chatsworth, California.

1.2 PURPOSE OF EQUIPMENT

The tape transport has the capability of recording digital data on 9-track magnetic tape at speeds up to 25 ips in 1600 cpi phase encoded ANSI and IBM compatible format. The data can be completely recovered when the tape is played back on any 9-track phase encoded ANSI and IBM compatible transport or its equivalent.

The transport can also synchronously read any 9-track phase encoded magnetic tape at speeds up to 25.0 ips which has been recorded in ANSI and IBM compatible format.

The transport utilizes a dual-stack read-after-write head which has the read and write heads separated by 0.15 inch. This enables simultaneous read and write operations to be performed so that data which has just been recorded by the write head can be read by the read head after tape has moved approximately 0.15 inch. This technique allows writing and checking of data in a single pass.

The transport operates directly from 95v to 230v ac, single phase 48 to 400 Hz power.

1.3 PHYSICAL DESCRIPTION OF EQUIPMENT

The Model T7640 transport, shown in Figure 1-1, can accommodate tape reels up to 7 inches in diameter. All electrical and mechanical components necessary to operate the transport are mounted on the deck casting which may be mounted in a standard 19-inch EIA rack.

In addition to the dual-stack head, the transport is equipped with an erase head which is automatically activated when writing.

Access to the hinged printed circuit boards is from the rear, as shown in Figure 1-2. The dust cover, which is also hinged, protects the magnetic tape, magnetic head, capstan, and other tape path components from dust and other contaminants.

The operational controls are mounted on the front control panel and are accessible with the dust cover door closed. Each indicator is illuminated when the relevant function is being performed. Power is supplied through a strain-relieved cord with a standard 3-pin plug. Interface signals are

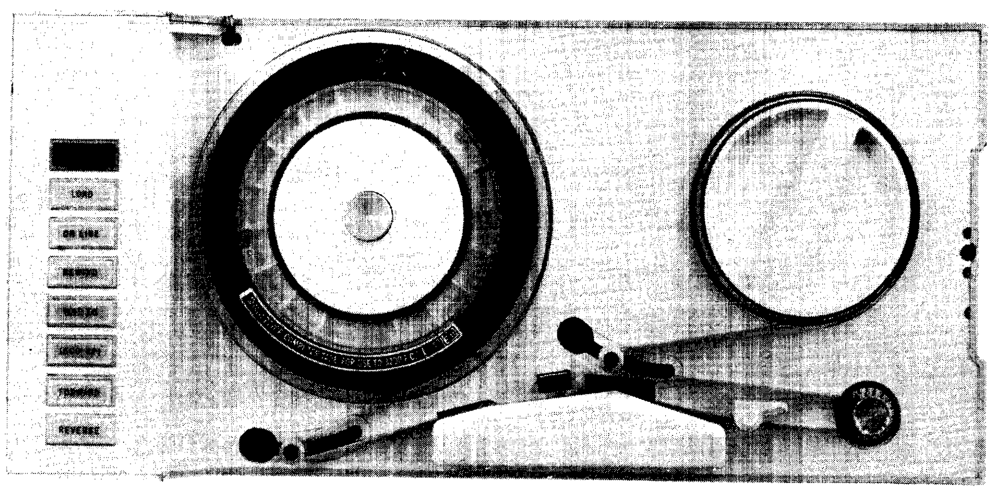

Figure 1-1. Model T7640 Tape Transport

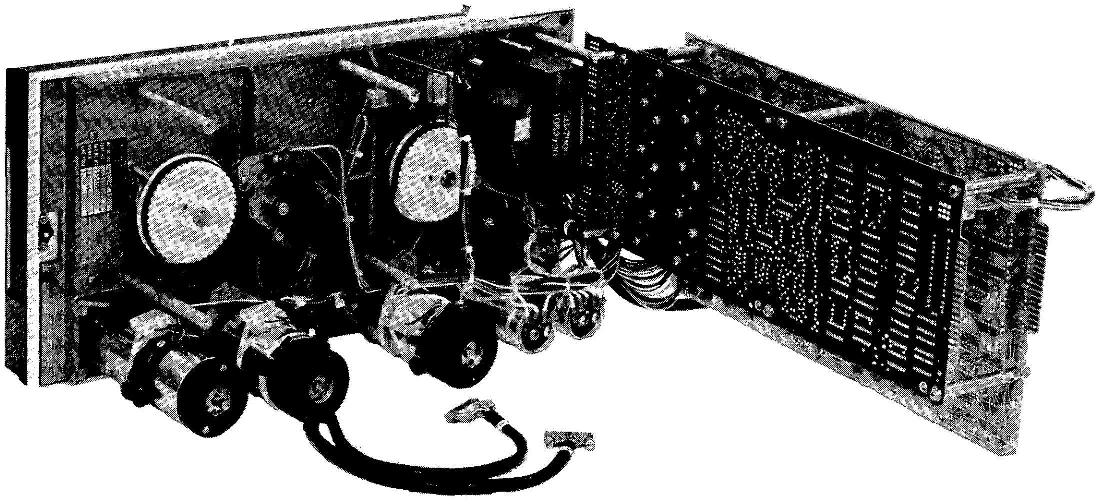

Figure 1-2. Model T7640 Tape Transport, Rear View

routed through three printed circuit connectors that plug directly into the printed circuit boards.

The take-up reel is fitted with a non-migrating pick-up strip to facilitate tape loading.

1.4 FUNCTIONAL DESCRIPTION

Figure 1-3 shows a block diagram of the system. The transport utilizes a single capstan drive for controlling tape motion during the synchronous write, synchronous read, and rewind modes. The tape is under a constant tension of 7 ounces, thus eliminating the possibility of tape "cinch" when the tape reel is placed on a computer transport.

The capstan is controlled by a velocity servo. The velocity information is generated by a dc tachometer that is directly coupled to the capstan motor shaft and produces a voltage that is proportional to the angular velocity of the capstan. This voltage is compared to the reference voltage from the ramp generators using operational amplifier techniques and

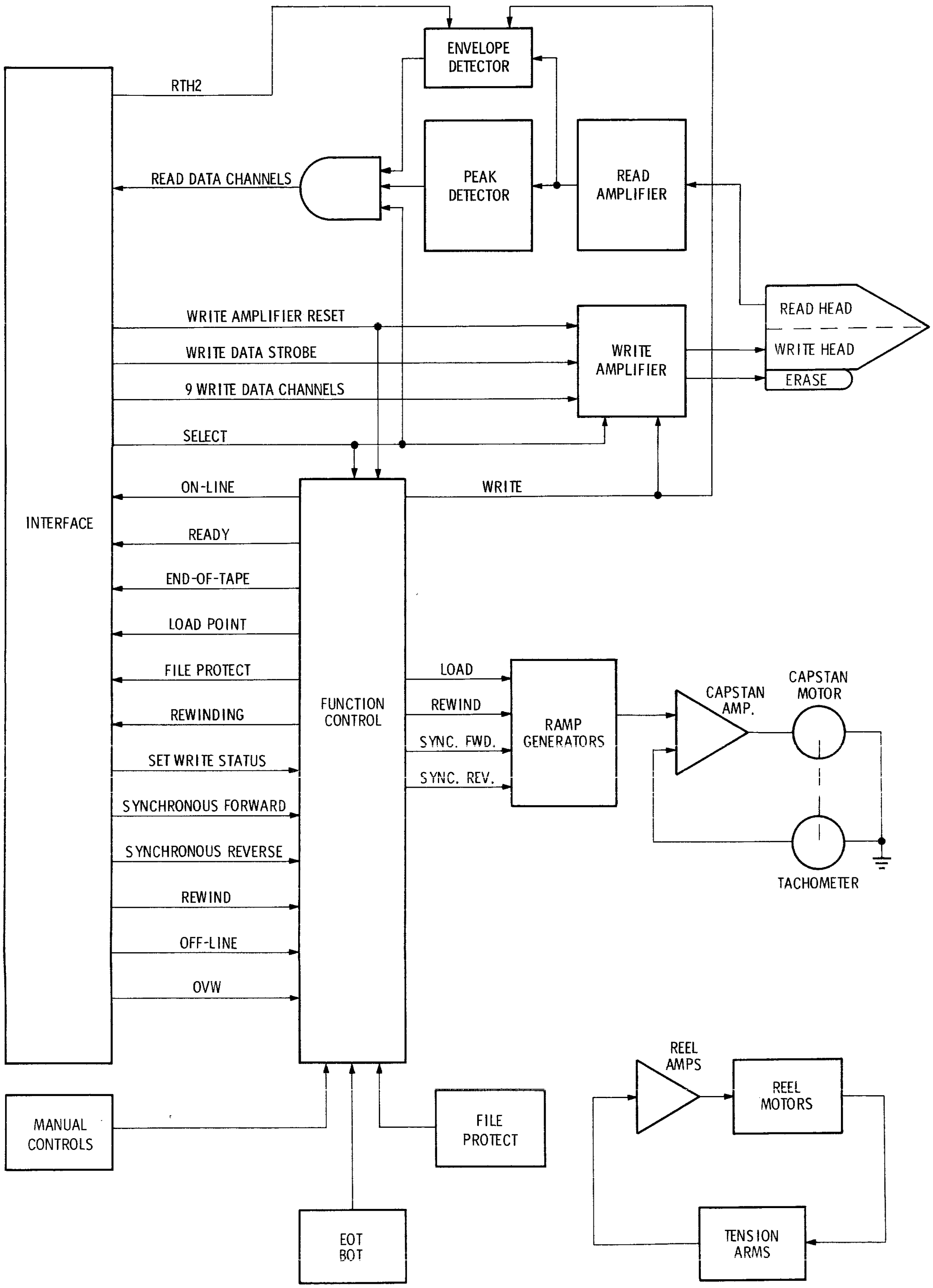

Figure 1-3. Block Diagram of Model T7640 Tape Transport

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the difference is used to control the capstan motor. This capstan control technique gives precise control of tape acceleration and tape velocities, thus minimizing tape tension transients.

During a writing operation, tape is accelerated in a controlled manner to the required velocity. This velocity is maintained constant and data characters are written on the tape at a constant rate such that:

$$\text{Bit density} = \frac{\text{Character Rate}}{\text{Tape Velocity}}$$

When data recording is complete, the tape is decelerated to zero velocity in a controlled manner.

Since the writing operation relies on a constant tape velocity, Inter-Record Gaps (IRGs) (containing no data) must be provided to allow for the acceleration and deceleration periods. Control of tape motion to produce a defined IRG is provided externally by the customer controller, in conjunction with the tape acceleration and deceleration characteristics defined within the transport.

During a reading operation, tape is accelerated to the required velocity. The acceleration time is such that the tape velocity becomes constant before data signals are received.

Nine data channels are presented to the interface. The end of a record is detected in the controller using "Missing Pulse Detector" circuits and the tape commanded to decelerate in a controlled manner.

The transport can operate in the Read mode in either the forward or reverse direction.

When operating in a "shuttling" mode (e.g., synchronous forward, stop, synchronous reverse, and stop) no turnaround delay is required between the end of one motion command and the beginning of the next motion command in the opposite direction.

In addition to the capstan control system, the transport consists of a mechanical tape storage system, supply and take-up reel servo systems, magnetic head and its associated electronics, and the control logic.

The mechanical storage system buffers the relatively fast starts and stops of the capstan from the high inertia of the supply and take-up reels. As tape is taken from or supplied to the storage system, a photoelectric sensor measures the displacement of the storage arm and feeds an error signal to the reel motor amplifier. This signal is amplified and used to control the reel motor such that the reel will either supply or take up tape to maintain the storage arm in its nominal operating position. The storage arm system is designed to give a constant tape tension as long as the arm is within its operating region. This tape path design minimizes tape wear because there is only relative motion of the tape oxide at the magnetic head.

The magnetic head writes and reads the flux transitions on the tape under control of the data electronics. Switching from the read-after-write to the read-only mode is accomplished by remote command.

The control logic operates on manual commands to enable tape, once loaded, to be brought to Load Point. At this stage, remote commands control tape motion, writing, and reading. The logic also provides rewind and unload functions in conjunction with the manual REWIND control.

The transport is also supplied with a photoelectric sensor for detection of the Beginning-of-Tape (BOT) tab and End-of-Tape (EOT) tab. The EOT signal is sent as a level to the customer while the BOT signal is used internally in the transport for control purposes.

The transport is designed with interlocks to protect the tape from damage due to component or power failure, or incorrect tape treading, and is provided with a tape cleaner to minimize tape contamination.

1.5 MECHANICAL AND ELECTRICAL SPECIFICATIONS

The mechanical and electrical specifications for the tape transport are shown in Table 1-1.

1.6 INTERFACE SPECIFICATIONS

Levels: True = Low = 0v to 0.4v (approximately)
False = High = 3v (approximately)

Pulses: Levels as above. Edge transmission delay over 20 feet of cable is not greater than 200 nanoseconds.

The interface circuits are designed so that a disconnected wire results in a false signal. Figure 1-4 shows the configuration for which the transmitters and receivers have been designed.

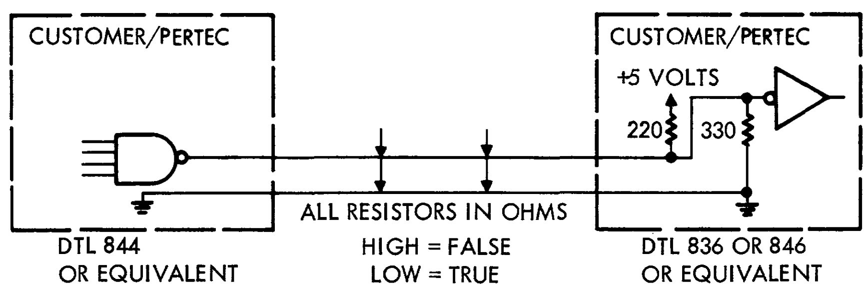


Figure 1-4. Interface Configuration

Table 1-1

Mechanical and Electrical Specifications

Tape (computer grade) Width Thickness	 12.7 mm (0.5 inch) 38.1 μm (1.5 mil)
Tape Tension	1.946 N (7.0 ounces)
Reel Diameter	177.8 mm (7.0 inches) (max.)
Reel Capacity (38.1 μm (1.5 mil) tape)	182.88 m (600 feet)
Recording Mode (IBM Compatible)	PE
Magnetic Head	Dual Stack with Erase Head
Tape Speed, Standard	0.633, 0.476, 0.317, m/s (25.0, 18.75, 12.5 ips)
Instantaneous Speed Variation	±3%
Long-Term Speed Variation	±1%
Rewind Speed 0.317, 0.476 m/s (12.5, 18.75 ips) transports 0.633 m/s (25.0 ips) transports	 1.27 m/s (50 ips) nominal 2.54 m/s (100 ips) nominal
Interchannel Displacement Error Read Write	 5.08 μm (200 μinches) maximum (See Note 1) 10.16 μm (400 μinches) maximum (See Note 2)
Stop/Start Time at 0.633 m/s (25 ips) (inversely proportional to tape speed)	15 ±1 msec
Stop/Start Displacement	4.826 ±0.5080 mm (0.19 +0.02 inch)
Beginning of Tape (BOT) and End of Tape (EOT) Detectors	Photoelectric (See Note 3) IBM Compatible
Weight	11 34 kg (25 pounds)
Dimensions Height Width Depth (from mounting surface) (See Note 4) Depth (total)	 222.2 mm (8.75 inches) 482.6 mm (19.0 inches) 273.0 mm (10.75 inches) 326.1 mm (12.84 inches)
Operating Temperature	5°C to 45°C (41°F to 113°F)
Non-Operating Temperature	—45°C to 71°C (—50°F to 160°F)
Operating Altitude	0 to 6,096 m (0 to 20,000 feet)
Non-Operating Altitude	0 to 15,240 m (0 to 50,000 feet)
Power Volts ac Watts (maximum on high line) (See Note 5) Frequency	 95, 105, 115, 125, 200, 210, 220, 230, 240, 250 120 48 to 400 Hz
Mounting	Standard EIA Rack
Electronics	All Silicon

NOTES:

1. The maximum displacement between any two bits of a character when reading an IBM master tape using the read section of the read-after-write head is 5.08 μm (200 μinches).
2. The maximum displacement between any two bits of a character on a tape written with all ones using the write section of the read-after-write head is 10.16 μm (400 μinches).
3. Approximate distance from detection area to head gap equals 30.5 mm (1.2 inches).
4. For optional microformatter, the depth increases 76.2 mm (3 inches) due to the Microformatter PCBA and cable clearance.
5. Transport only. For power consumption of optional microformatter, refer to Section I of the microformatter addendum.

SECTION II
INSTALLATION AND INITIAL CHECKOUT

2.1 INTRODUCTION

This section contains a summary of interface lines, information for uncrating the transport, as well as the procedure for electrically connecting and initially checking out the transport.

2.2 UNCRATING THE TRANSPORT

The transport is shipped in a protective container to minimize the possibility of damage during shipping.

Place the shipping container in the position indicated on the container.

Open the shipping container and remove the packing material so the transport and its shipping frame can be lifted from the container.

Lift the transport from the container using the shipping frame and set it down so access to the front and rear of the deck is available.

Check the contents of the shipping container against the packing slip and investigate for possible damage. If there is any damage, notify the carrier.

Check the printed circuit boards and all Molex connectors for correct installation. Check the plug-in relay for proper seating on the printed circuit board immediately above the power transformer.

CAUTION

> ENSURE THAT ALL PRINTED CIRCUIT CONNECTORS ARE PLUGGED IN THE CORRECT LOCATION AND ARE FULLY ENGAGED WITH THEIR MATING PARTS. DAMAGE TO CIRCUITRY CAN OTHERWISE OCCUR.

Check the identification label on the back of the tape deck for the correct model number and line voltage requirement. If the actual line voltage at the installation differs from that on the identification label, the power transformer taps should be changed as shown in Figure 4-3. The POWER switch/indicator wire should not be moved.

2.3 POWER CONNECTIONS

A fixed, strain-relieved power cord is supplied for plugging into a polarized 115v outlet. For other power sockets, the plug supplied must be removed and a correct plug installed.

2.4 INITIAL CHECKOUT PROCEDURE

Section III contains a detailed description of all controls. To check the proper operation of the transport before placing it in the system, follow the specified procedure.

(1) Ensure proper primary connection to the power transformer; refer to Paragraph 4.3.1.

(2) Load tape on the transport as described in Paragraph 3.3.

(3) Turn the transport power on by depressing the POWER control.

(4) Depress the LOAD control momentarily to apply capstan-motor and reel-motor power.

(5) Depress the LOAD control momentarily a second time to initiate the Load sequence. The tape will move forward until it reaches the BOT tab, when it stops. The LOAD indicator should become illuminated when the BOT reaches the photosensor and remain illuminated until tape moves off the Load Point. At this point, there will be no action when the LOAD control is depressed.

(6) Check On-line status by depressing the ON LINE control repeatedly and observing that the indicator is alternately illuminated and extinguished.

(7) With the transport Off-line (ON LINE indicator not illuminated) press the alternate action FORWARD control. Run several feet of tape onto the take-up reel and press the FORWARD control again to stop the tape.

Check that if the transport is On-line, the action of the FORWARD control is inhibited although the indicator light will still show the status of the control.

(8) Press the alternate action REVERSE switch. Tape will move in the reverse direction until the BOT tab reaches the photosensor, when it will stop. Check that the action of the REVERSE control is inhibited when the transport is On-line.

(9) Using the FORWARD control, run several feet of tape onto the take-up reel. Depress the REWIND control momentarily to initiate the Rewind mode and illuminate the REWIND indicator. Tape will rewind past the BOT tab, enter the Load sequence, return to the BOT tab and stop with the LOAD indicator illuminated. If the REWIND control is momentarily depressed when tape is at BOT, the LOAD indicator will be extinguished, the REWIND indicator illuminated, and tape will rewind until tape tension is lost. This action is used to unload tape. The reel can be removed as outlined in Paragraph 3.3.2.

(10) Visually check the components of the tape path for correct tape tracking (tape rides smoothly in the head guides, etc.).

2.5 INTERFACE CONNECTIONS

It is assumed that interconnection of PERTEC and Customer equipment uses a harness of individual twisted pairs, each with the following characteristics.

(1) Maximum length of 20 feet.

(2) Impedance between 110 to 150 ohms.

(3) 22 or 24 gauge conductor with minimum insulation thickness of 0.01 inch.

It is important that the ground side of each twisted pair is grounded within a few inches of the board to which it is connected.

Three printed circuit edge connectors are supplied with each transport. These are ELCO connectors, Part No. 00-6007-036-980-002 (PERTEC Part No. 503-0036) which can be supplied upon request at no charge. The connectors must be wired by the customer and strain relieved as shown in Figure 2-1. Interface signals are thus routed directly to and from the printed circuit boards. Table 2-1 shows the Input/Output lines required. Details relating to the interface are contained in Section III.

2.6 RACK MOUNTING THE TRANSPORT

The physical dimensions of the transport are such that it may be mounted in a standard EIA rack; 8-3/4 inch panel space is required. It requires a minimum depth behind the mounting surface of 11 inches (for optional microformatter the mounting depth is 14 inches). Unless free access to the back of the disk is available, it is desirable to install the interface connectors before rack mounting.

The transport's mounting holes are for a standard EIA rack. Figure 2-2 illustrates the procedure for mounting and Figure 2-3 is an installation diagram with dimensions. To rack mount the transport, follow this procedure.

(1) Place the transport on a flat surface with the reels facing the operator. Locate the socket wrench and the mounting screws supplied with the transport.

(2) Remove the control panel located on the left front of the transport (Figure 2-2(A)). Removal is most easily accomplished by tapping the control panel corners (from the rear) with a screwdriver handle or similar object.

CAUTION

CARE SHOULD BE TAKEN TO ENSURE THAT THE CONTROL PANEL WIRING IS NOT STRESSED.

(3) Remove the three No. 8 one-inch screws holding the transport to the shipping frame (Figure 2-2(B) and (C)).

(4) Locate the transport in the rack and insert the two socket head screws in the access holes on the left front of the transport. Do not tighten at this point.

(5) Open the dust cover and locate the single captive screw on the right over the hole in the rack (using the socket wrench) and tighten the screw.

(6) Tighten the two screws on the left and snap the control panel into position.

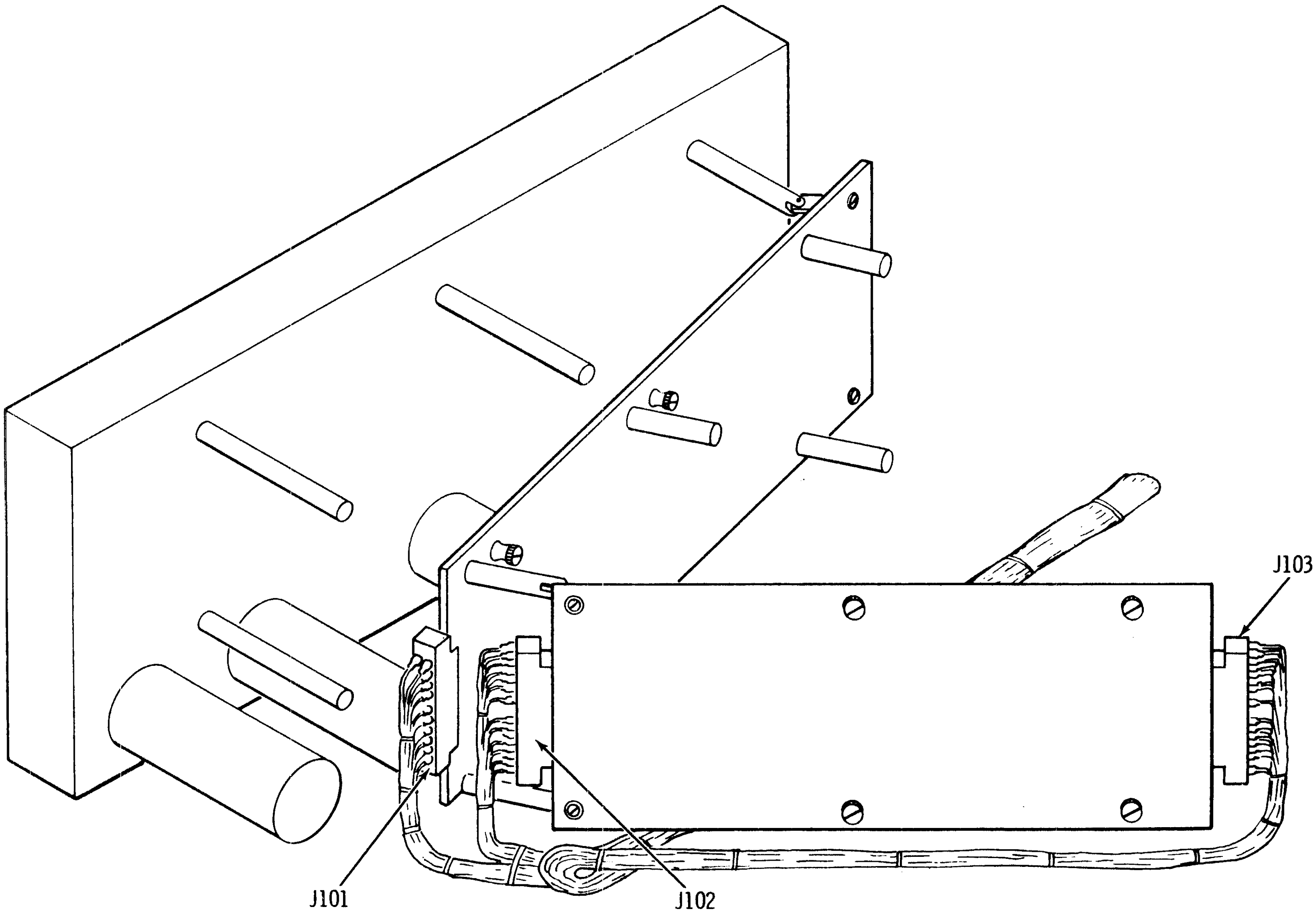


Figure 2-1. Interface Cable Installation

Table 2-1

Interface Connections

Transport Connector Mating Connector			36 Pin Etched PC Edge Connector 36 Pin ELCO 00-6007-036-980-002
Connector (Reference Figure 2-1)	Live Pin	Ground Pin	Signal*
J101	J	8	→ SELECT (ISLT)
	C	3	→ SYNCHRONOUS FORWARD Command (ISFC)
	E	5	→ SYNCHRONOUS REVERSE Command (ISRC)
	H	7	→ REWIND Command (IRWC)
	L	10	→ OFF-LINE Command (IOFFC)
	K	9	→ SET WRITE STATUS (ISWS)
	B	2	→ OVERWRITE Command (IOVW)
	T	16	← READY (IRDY)
	M	11	← ON-LINE Command
	N	12	← REWINDING (IRWD)
	U	17	← END OF TAPE (IEOT)
	R	14	← LOAD POINT (ILDP)
	P	13	← FILE PROTECT (IFPT)
J102	A	1	→ WRITE DATA STROBE (IWDS)
	C	3	→ WRITE AMPLIFIER RESET (IWARS)
	F	6	→ READ THRESHOLD (IRTH2)
	L	10	→ WRITE DATA PARITY (IWDP)
	M	11	→ WRITE DATA 0 (IWD0)
	N	12	→ WRITE DATA 1 (IWD1)
	P	13	→ WRITE DATA 2 (IWD2)
	R	14	→ WRITE DATA 3 (IWD3)
	S	15	→ WRITE DATA 4 (IWD4)
	T	16	→ WRITE DATA 5 (IWD5)
	U	17	→ WRITE DATA 6 (IWD6)
	V	18	→ WRITE DATA 7 (IWD7)
J103	1	A	← READ DATA PARITY (IRDP)
	3	C	← READ DATA 0 (IRD0)
	4	D	← READ DATA 1 (IRD1)
	8	J	← READ DATA 2 (IRD2)
	9	K	← READ DATA 3 (IRD3)
	14	R	← READ DATA 4 (IRD4)
	15	S	← READ DATA 5 (IRD5)
	17	U	← READ DATA 6 (IRD6)
	18	V	← READ DATA 7 (IRD7)

* See Section III for definitions of interface functions.

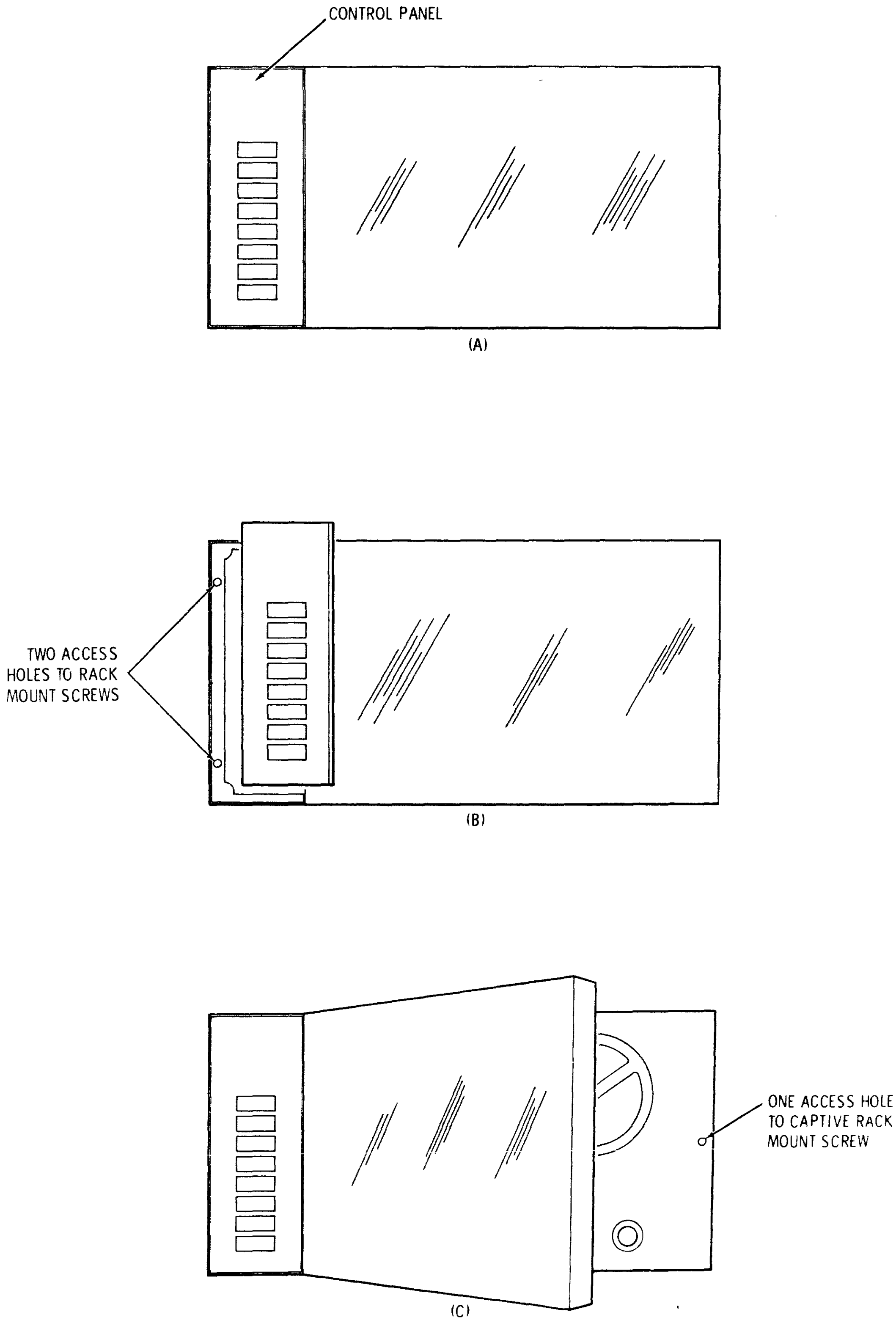


Figure 2-2. Rack Mounting the Transport

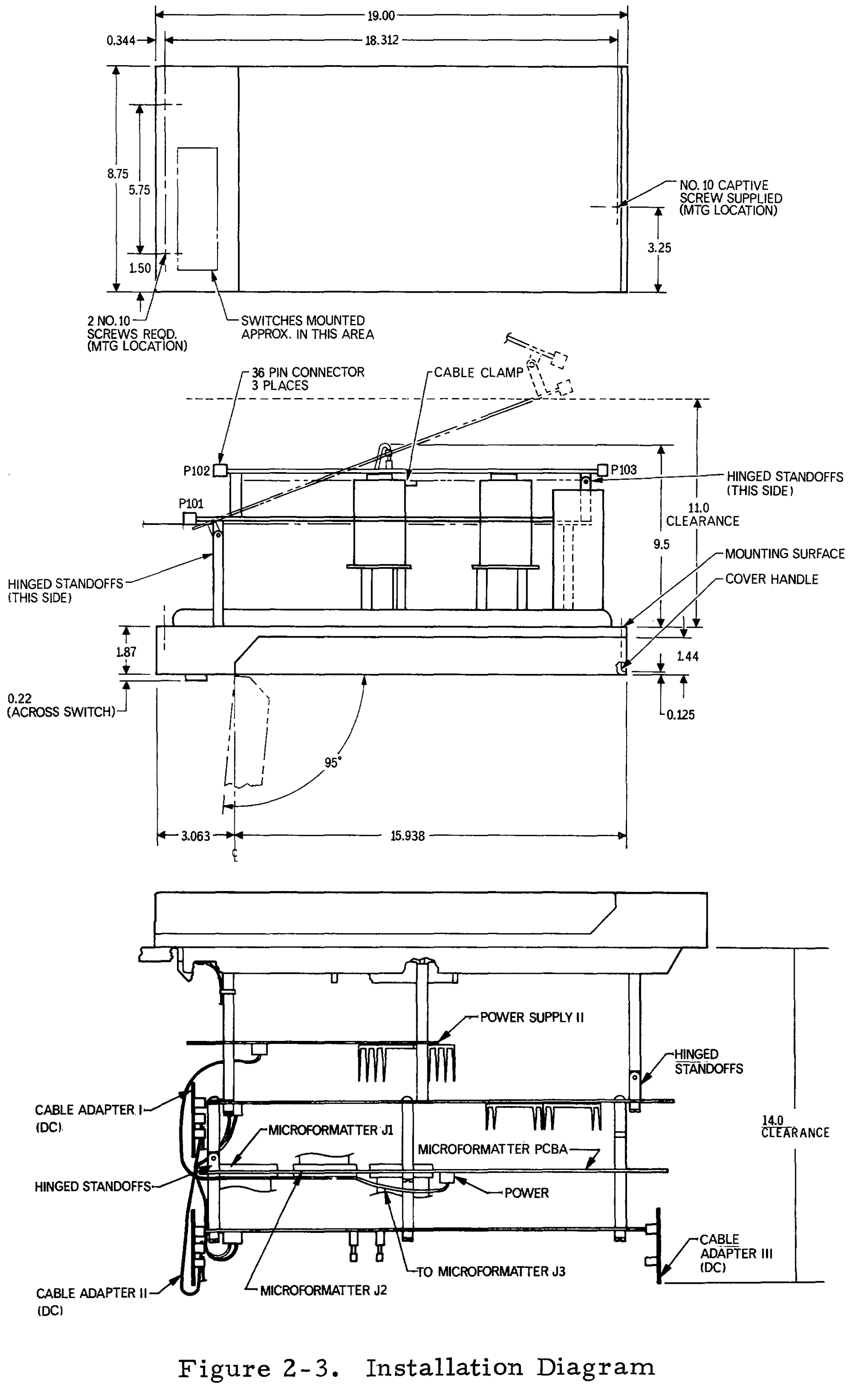


Figure 2-3. Installation Diagram

SECTION III
OPERATION

3.1 INTRODUCTION

This section explains the manual operation of the tape transport and defines the interface functions with regard to timing, levels, and interrelationships.

3.2 CLEANING THE HEAD AND GUIDES

The brief operation described in Paragraph 6.3.1 must be performed daily to realize the data reliability capabilities of the transport.

3.3 LOADING TAPE ON TRANSPORT

The Model T7640 transport, as shown in Figure 3-1, has the supply reel (reel to be recorded or reproduced) on the left side, adjacent to the manual controls. The tape must unwind from the supply reel when the reel is turned in a clockwise direction. Note that a Write Enable ring on the reel is required to close the interlocks which allow writing.

To load a tape reel (maximum reel size is 7 inches in diameter with 600 feet of tape), position the reel over the quick-release hub and depress the center plunger. This allows the reel to slip over the rubber ring on the hub. Press the reel evenly and firmly against the back flange of the hub with the center plunger depressed. Release the center plunger. The reel is now properly aligned in the tape path and ready for tape threading.

Thread tape along the path shown in Figure 3-1. The tape path is delineated by a fine line on the overlay. The take-up or fixed reel is equipped with a retaining strip which greatly facilitates take-up of the

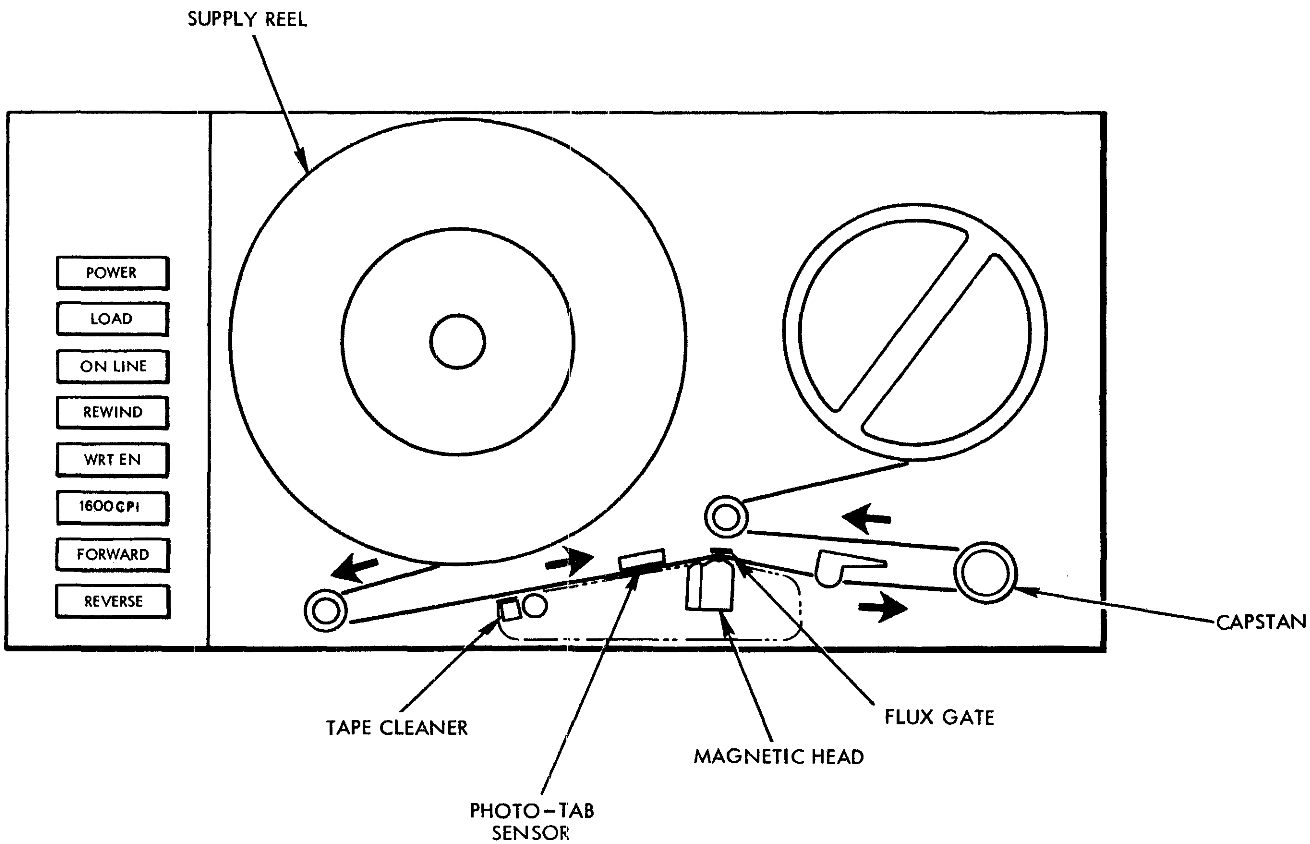


Figure 3-1. Model T7640 Tape Path and Controls

tape. It will be necessary to hold the Flux Gate unit away from the head during tape threading. It is necessary to lay only approximately 3 inches of tape onto the take-up reel and apply a wiping action quickly with the finger to produce adequate friction between the tape and reel when tension is applied.

3.3.1 BRINGING TAPE TO LOAD POINT (BOT)

The tape should be manually tensioned and checked for correct seating in the guides by rotating the supply hub. To bring the tape to the Load Point:

(1) Turn the power on by depressing the POWER control.

(2) Depress and release the LOAD control. This applies power to the capstan and reel motors and brings the tape to the correct operating tension. The tape storage arms are now in the operating position.

CAUTION

CHECK THAT THE TAPE IS POSITIONED CORRECTLY ON ALL GUIDES OR TAPE DAMAGE MAY RESULT.

(3) Depress and release the LOAD control a second time. This causes tape to move forward at the prescribed operating velocity. Check tape tracking in the guides again and close the dust cover.

CAUTION

THE DUST COVER SHOULD REMAIN CLOSED AT ALL TIMES WHEN TAPE IS ON THE TAKE-UP REEL. DATA RELIABILITY MAY BE IMPAIRED BY CONTAMINANTS IF THE COVER IS LEFT OPEN.

When the reflective BOT tab reaches the Load Point the tape stops with the front edge of the tab approximately one inch from the magnetic head gap. The transport is now ready to receive external commands.

3.3.2 UNLOADING THE TAPE

To unload a recorded tape, complete the following procedure if power has been switched off; if power is on, start at Step (3).

(1) Turn the power on by depressing the POWER control.

(2) Depress and release the LOAD control, which applies tape tension.

(3) Depress and release the REWIND control. When the tape has rewound to the BOT tab, it comes to a controlled stop. The tape overshoots and the transport enters the Load sequence to bring the tape to rest at the BOT.

(4) Depress and release the REWIND control a second time. This initiates a further rewind action which continues until tension is lost.

(5) Open the dust cover and wind the end of the tape onto the supply reel. Depress the hub center plunger and remove the reel. Close the dust cover.

3.4 MANUAL CONTROLS

The operational controls with indicators are located on the control panel on the front of the transport (see Figure 3-1). The following paragraphs describe the functions of these controls.

3.4.1 POWER

The POWER control is an alternate action switch/indicator which connects line voltage to the power transformer. When power is turned on,

(1) All power supplies are established.

(2) The ground returns of all motors are open-circuited.

(3) A reset signal is applied to appropriate control flip-flops.

3.4.2 LOAD

The LOAD control is a momentary switch/indicator. Depressing and releasing the control for the first time after power has been applied to the transport energizes the servo system by applying ground returns to all motors and removes the reset signal. The tape will now be tensioned.

Depressing and releasing the LOAD control for the second time causes tape to move to and stop at the Load Point. The transport is now ready to receive external commands. While the BOT tab is located over the photo-tab sensor the LOAD indicator is illuminated. The LOAD control is disabled after the first LOAD or manual REWIND command has been given and can only be re-enabled by loss of tape tension or restoration of power after power has been off.

3.4.3 ON LINE

The ON LINE control is a momentary switch/indicator which is enabled after an initial Load or Rewind sequence has been initiated.

Depressing and releasing the switch after an initial Load or Rewind sequence is initiated switches the transport to an On-line mode and the indicator is illuminated. In this condition the transport can accept external commands, provided it is also Ready and Selected.

The transport will revert to the Off-line mode if any of the following occur.

(1) The ON LINE control is depressed a second time.

(2) An external OFF-LINE command (IOFFC) is received.

(3) Tape tension is lost.

3.4.4 REWIND

The REWIND control is a momentary switch/indicator which is enabled only in the Off-line mode. Depressing and releasing the control causes tape to rewind. On reaching the BOT tab, the rewind drive ceases and the Load sequence automatically entered. The BOT tab will overshoot the photo-tab sensor, move forward, and stop at the Load Point.

If the REWIND control is depressed and released when tape is at Load Point (LOAD indicator illuminated) the tape rewinds off the take-up reel and tension is lost.

The REWIND indicator is illuminated throughout any rewind operation including the subsequent Load sequence where relevant.

A manual REWIND command will override the Load sequence.

3.4.5 WRT EN (WRITE ENABLE)

This is an indicator which is illuminated whenever power is on and a reel of tape, with a Write Enable ring installed, is mounted on the transport.

3.4.6 1600 CPI

This is an indicator which is illuminated whenever power is applied to the transport.

3.4.7 FORWARD

The FORWARD control is an alternate action switch/indicator which is enabled only in the Off-line mode and when the transport is Ready.

When the switch is depressed, the indicator is illuminated and tape will move forward at the prescribed speed. When the switch is depressed again, the tape stops and the indicator is extinguished.

If the EOT tab is encountered while moving forward under control of the FORWARD switch, the tape stops but the indicator will remain illuminated.

3.4.8 REVERSE

The REVERSE control is an alternate action switch/indicator which is enabled only in the Off-line mode and when the transport is Ready.

When the switch is depressed, the indicator is illuminated and tape will move in the reverse direction at the prescribed speed. When the switch is depressed again the tape stops and the indicator is extinguished.

If the BOT tab is encountered while tape is moving in the reverse direction, the tape stops but the indicator will remain illuminated.

3.5 INTERFACE INPUTS (CONTROLLER TO TRANSPORT)

All waveform names are chosen to correspond to the logical true condition. Drivers and receivers belong to the DTL830 series where the True level is 0v to 0.4v, and the False level is between +3v and +5v. Figure 1-4 is a schematic of the interface circuit.

3.5.1 SELECT (ISLT)

This is a level which, when true, enables all of the interface drivers and receivers in the transport, thus connecting the transport to the controller.

It is assumed that all of the interface inputs discussed in the following paragraphs are gated with SELECT (ISLT).

3.5.2 SYNCHRONOUS FORWARD COMMAND (ISFC)

This is a level which, when true and the transport is Ready (see Paragraph 3.6.1), causes tape to move forward at the specified velocity. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times.

3.5.3 SYNCHRONOUS REVERSE COMMAND (ISRC)

This is a level which, when true and the transport is Ready (see Paragraph 3.6.1), causes tape to move in the reverse direction at the specified velocity. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times. An ISRC will be terminated upon encountering the BOT tab or ignored if given when tape is at Load Point.

3.5.4 REWIND COMMAND (IRWC)

This is normally a 1-μsec pulse which, if the transport is Ready, causes tape to move in the reverse direction. Upon reaching BOT, the rewind ceases and the Load sequence is automatically initiated. Tape now moves forward and comes to rest at BOT.

The REWIND indicator is illuminated for the duration of the rewind and the following Load sequence.

An IRWC is ignored if tape is already at BOT.

The velocity profile is trapezoidal with nominally equal rise and fall times of approximately 0.25-second.

3.5.5 SET WRITE STATUS (ISWS)

This is a level which must be true for a minimum period of 20 μsec after the front edge of an ISFC (or ISRC) when the Write mode of operation is required. The front edge of the delayed ISFC (or ISRC) is used to sample the ISWS signal and sets the Write/Read flip-flop in the transport to the Write state.

If the Read mode of operation is required the ISWS signal must be false for a minimum period of 20 μsec after the front edge of an ISFC (or ISRC), in which case the Write/Read flip-flop will be set to the Read state. The Write/Read flip-flop is also set to the Read state by any of the following.

(1) An IRWC or IOFFC.

(2) Loss of tape tension.

(3) Switching to the Off-line mode.

3.5.6 WRITE DATA LINES (IWDP, IWD0 – IWD7)

These are phase encoded waveforms representative of data bits which, at the time of IWDS, are transferred into the Write flip-flops. The transport must be in the Write mode for transfer to occur.

The Write Data lines should have settled at least 0.5 μsec before the leading edge of the IWDS and should remain steady until 0.5 μsec after the trailing edge of the IWDS pulse.

3.5.7 WRITE DATA STROBE (IWDS)

This is a pulse (1 μsec minimum width) for each flux reversal to be recorded. The frequency of the IWDS is twice the character transfer rate. The IWDP and IWD0 – IWD7 levels must be steady for 0.5 μsec before, during, and after the IWDS. The trailing edge of IWDS is employed to trigger the write waveform generator in the transport.

3.5.8 WRITE AMPLIFIER RESET (IWARS)

The IWARS is employed only in transports which have the overwrite option included (see Paragraph 3.5.10). This is a pulse (1 μsec minimum width) which, when true, turns off the write current in the transport. This signal occurs coincidental with the last flux transition of the postamble.

3.5.9 OFF-LINE (IOFFC)

This is a level or pulse (1 μsec minimum width) which resets the On-line flip-flop to the false state placing the transport under manual control.

It is gated in the transport by SELECT (ISLT) only, allowing an OFF-LINE command to be given while a rewind is in progress.

OFF-LINE must be separated by at least 1 μsec from a REWIND command.

3.5.10 OVERWRITE (IOVW)

This is a level which must be true for a period of 20 μsec beginning with the leading edge of an ISFC (or ISRC) when the Overwrite mode of operation is required. Additionally, the Write mode must be selected to enable the Overwrite capability.

The leading edge of the ISFC (or ISRC) delayed is used to sample the IOVW signal and set an Overwrite flip-flop in the transport.

If the IOVW level is false for a minimum period of 20 μsec beginning with the leading edge of an ISFC (or ISRC) the transport will revert to a normal Write mode of operation.

The signal will be used in addition to the ISWS signal when isolated records are to be updated.

The IWARS signal must also be employed with IOVW (see Paragraph 3.5.8).

3.5.11 READ THRESHOLD (IRTH2)

This is a level which, when true, selects a low threshold level for the Read circuits in the transport. This level is selected only when it is required to recover very low amplitude data. IRTH2 must be held steady for the duration of each recording being read.

3.6 INTERFACE OUTPUTS (TRANSPORT TO CONTROLLER)

It is assumed that all Interface outputs discussed in the following paragraphs are gated with SELECT.

3.6.1 TRANSPORT READY (IRDY)

This is a level which is true when the transport is ready to accept any external command; i.e., when

(1) Tape tension is established.

(2) The initial LOAD or REWIND command has been completed.

(3) There is no subsequent REWIND command in progress.

(4) The transport is On-line.

3.6.2 READ DATA (IRDP, IRD0 – IRD7)

The signals on these 9 lines are the outputs of the 9 peak detectors, individually gated with the outputs of an envelope detector associated with each channel. These signals are a replica of the PE waveforms used to drive the write amplifiers.

The characteristics of the threshold detector are such that the signal from approximately four successive bits must exceed the threshold level before the detector will enable the output gate for its channel. If the signal suddenly ceases (e.g., due to a dropout) the threshold detector disables the output gate to its channel approximately two bits after the dropout.

3.6.3 ON-LINE

This is a level which is true when the On-line flip-flop is set. When true, the transport is under remote control; when false, the transport is under local control.

3.6.4 LOAD POINT (ILDP)

This is a level which is true when the transport is Ready and tape is at rest with the BOT tab under the photo-tab sensor. The signal goes false after the tab leaves the photosensor area.

3.6.5 END OF TAPE (IEOT)

This is a level which, when true, indicates that the EOT reflective tab is positioned under the photo-tab sensor.

3.6.6 REWINDING (IRWD)

This is a level which is true when the transport is engaged in any Rewind operation or the Load sequence following a rewind operation.

3.6.7 FILE PROTECT (IFPT)

This is a level which is true when power is on and a reel of tape (without a Write Enable ring installed) is mounted on the transport.

3.7 INTERFACE TIMING

3.7.1 WRITE AND READ WAVEFORMS

Figure 3-2 illustrates the PE write and read waveforms. The controller generates all command waveforms.

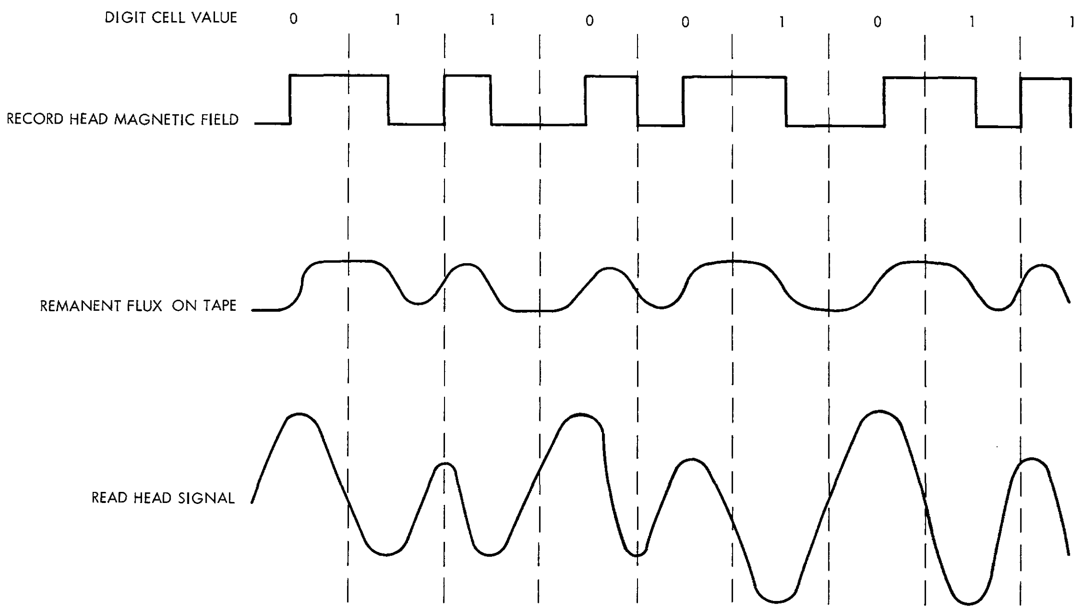


Figure 3-2. PE Write and Read Waveforms

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section provides a description of the operation of the tape transport.

The tape transport consists of the mechanical and electronic components necessary to handle magnetic tape in such a manner that data can be reproduced from a tape recorded on any 9-track, phase encoded, ANSI and IBM compatible tape transport, and a tape can be generated from which data can be completely recovered when played back on any 9-track ANSI and IBM compatible tape transport.

The transport consists of the following components.

(1) Power supply

(2) Capstan drive system

(3) Tape storage and reel servo systems

(4) Magnetic head and associated tape guides and cleaner

(5) Data electronics

(6) Control logic and interlock system

4.2 ORGANIZATION OF THE TRANSPORT

A highly modular construction has been adopted with all of the major components and subassemblies interconnected by means of connectors rather than the more conventional wiring techniques (see Figure 4-1).

Three printed circuit boards are employed. The first, the Tape Control PCBA, is mounted on hinged standoffs adjacent to the tape deck. It contains the control logic, the reel servo amplifiers, capstan servo amplifier,

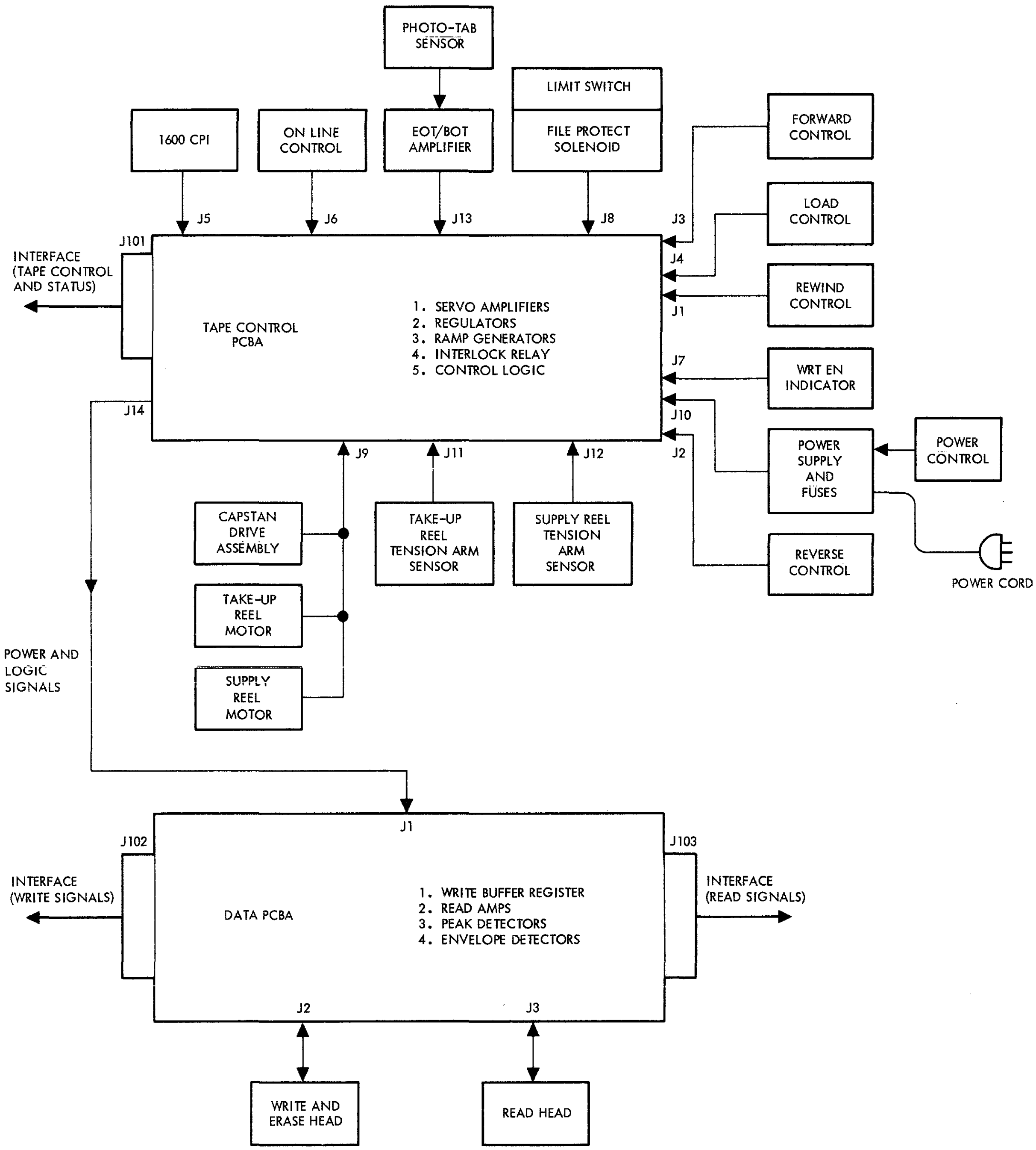


Figure 4-1. Organization of the Model T7640 Tape Transport

621D

voltage regulators, photo-tab sensor amplifiers, and interlock relay. With the exception of the magnetic head, all of the deck-mounted components (power supply, motors, tension arm position sensors, photo-tab sensors, etc.) plug directly into locations on the circuit board. A printed circuit edge connector carries interface signals to and from the board.

The second hinged board, the Data PCBA, is concerned only with the writing and reading of data. Write data enters by means of a printed circuit edge connector on one end of the board; data is buffered and transferred to the write head through the appropriate connector (one of two) in the middle of the board. Signals from the read head enter the circuit board via the second of the two connectors and are fed to the amplifiers, peak detectors, envelope detectors, and transmitters. Digital read signals are transmitted by means of a second interface edge connector.

A third board, the EOT/BOT Amplifier PCBA, is mounted on the Write Lockout bracket at the rear of the tape deck.

DC power and three control levels are obtained from the Tape Control PCBA via a single harness.

The harnesses from the three interface connectors are merged, strain relieved, and leave the transport.

4.3 FUNCTIONAL SUBSYSTEMS DESCRIPTION

4.3.1 POWER SUPPLY

Figure 4-2 is a block diagram of the power supply which is in two parts. The first part, the power supply module with rectifiers, capacitors, transformer, power cord, etc., is fastened to the deck; it is connected to the second part, the +5v and -5v regulators, on the Tape Control PCBA by a 6-pin connector. Two connections may be provided for an optional 5 volt microformatter regulator.

Selection of proper ac voltage taps on the power transformer is facilitated through use of a coded jumper plug assembly shown in Figure 4-3. A cross reference of various line voltages to jumper plug assemblies, PERTEC part numbers, and pin connections is also shown.

The line voltage is connected across the transformer primary when the POWER control is depressed. The POWER control neon indicator is connected across 115v ac, independent of selected line voltage. Unregulated dc (at a nominal ±12v, or ±21v for 25 ips transports, under load) is used to power the motors and voltage regulators. Two regulated supplies are generated. The ±5v supplies are adjusted and regulated within ±0.2 percent and can supply up to 2.0 amps. Since TTL integrated circuits are used, it is necessary to use an SCR for "crowbar" protection against overvoltage on the +5v line. The circuits used can withstand up to 7v. When the +5v line rises to +5.5v, the SCR connected between the positive unregulated supply and 0v is turned on. This holds the voltage on the ICs down until the fuse opens a few milliseconds later.

4.3.2 CAPSTAN SERVO

Figure 4-4 is a block diagram of the capstan servo. It consists of two parts: the deck mounted capstan drive assembly with the motor-tachometer combination and the capstan; and, the amplifier and ramp generators on the Tape Control PCBA. A relay contact disconnects the motor when tape tension is lost.

Tape is moved by the capstan whose velocity is determined by the velocity servo, and the output of one of the two ramp generators. If the Reverse

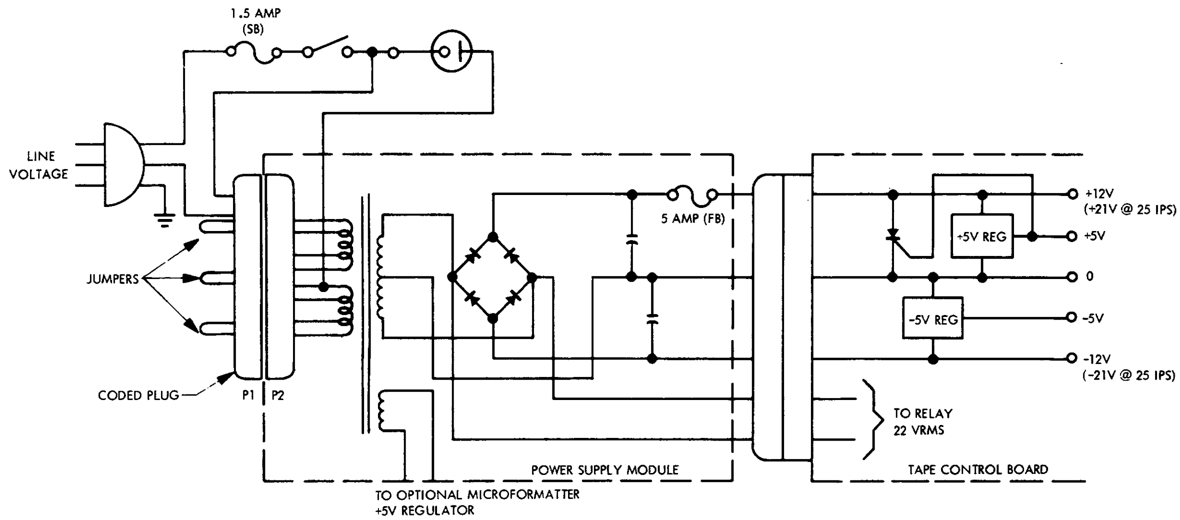
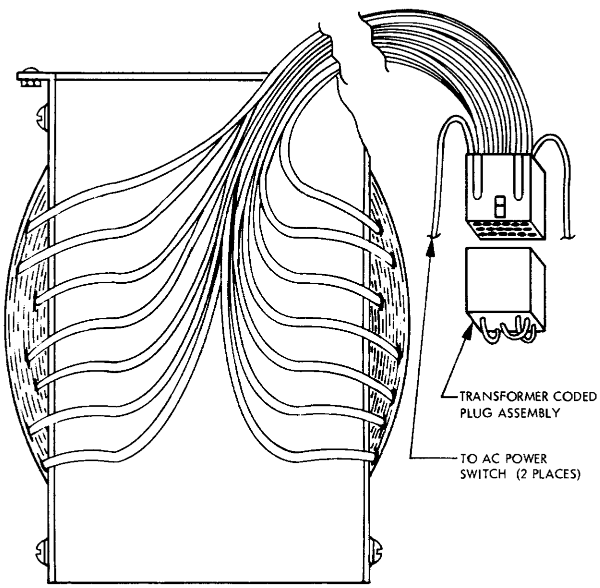


Figure 4-2. Block Diagram of Power Supplies



TRANSFORMER CODED-PLUG AND JUMPER IDENTIFICATION						
AC LINE VOLTAGE	PERTEC PART NO.	PIN 2 TO	PIN 8 TO	PIN 11 TO	PIN 24 TO	PIN 23 TO
95	104586-01	3	1		16	19
105	104586-02	3	1		9	14
115	104586-03	6		1	17	22
125	104586-04	6		1	14	9
190	104586-05	3	16			19
200	104586-06	3	16			9
210	104586-07	3	14			9
220	104586-08	3		16		9
230	104586-09	6		17		22
240	104586-10	6		14		22
250	104586-11	6		14		9

Figure 4-3. Transformer Primary Connections

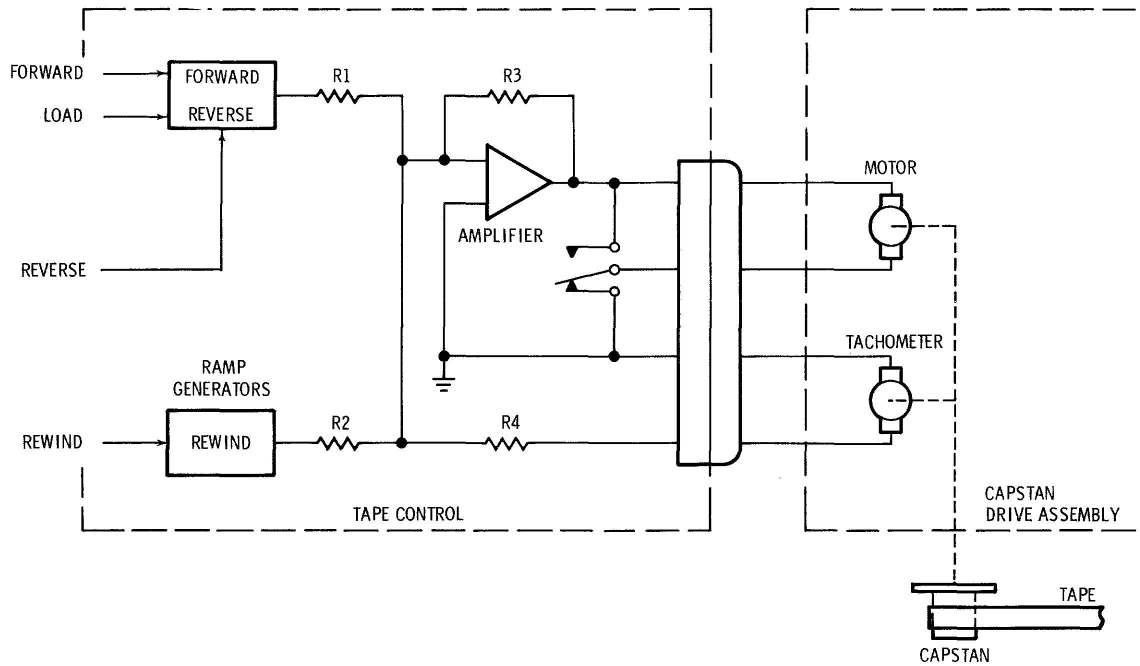


Figure 4-4. Capstan Servo Block Diagram

ramp generator is selected by the logic, the voltage at R1 rises at a rate corresponding to the specified start time of the tape. The amplifier then accelerates the motor and the tape; the feedback voltage from the tachometer produces current in R4 which tends to reduce the amplifier input current produced by the ramp generator. The voltage at R1 stops rising after the specified start time and the velocity builds up to the point where the current in R4 approximately equals that in R1.

The Forward ramp generator is activated by the SYNCHRONOUS FORWARD command (if On-line), or by depressing the FORWARD control (if Off-line), or by a Load sequence. The Reverse ramp generator is activated by a SYNCHRONOUS REVERSE command (if On-line), or by depressing the REVERSE control (if Off-line). The Rewind ramp generator is activated by a REWIND command (if On-line), or by depressing the REWIND control (if Off-line). When the transport is in the standby condition, the capstan position is maintained by motor friction.

Both Forward and Reverse ramps rise and fall in a time calculated to produce a tape movement of 0.19 ±0.02 inch when tape reaches the specified velocity, e.g., 30 milliseconds for a 12.5 ips transport.

The Rewind ramp rise and fall time is not critical; it is approximately 0.25 second and simply long enough to allow the reel servos to keep up with the rise or fall in tape speed. Typical waveforms are shown in Figure 4-5.

4.3.3 REEL SERVOS

Identical linear position servos control the supply and take-up of tape by the reels. Figure 4-6 is a diagram of one reel servo.

The components of the servo are: tension arm position sensor; pulleys, belt, tension arm, and tape reel; reel motor; and, servo amplifier on the Tape Control PCBA.

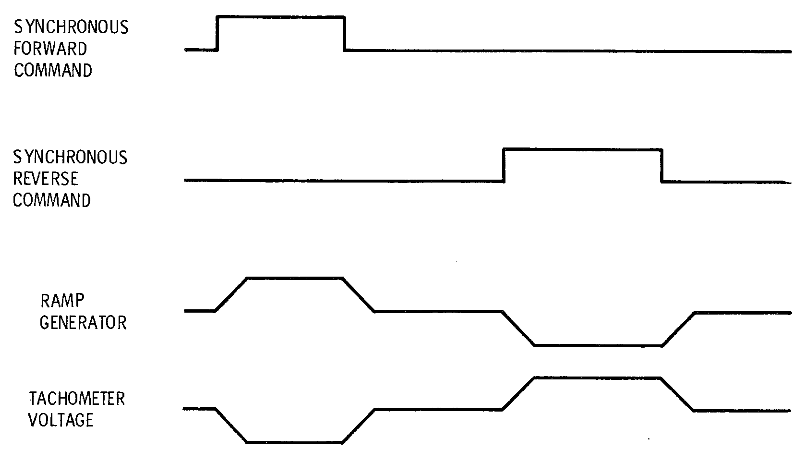


Figure 4-5. Typical Capstan Servo Waveforms

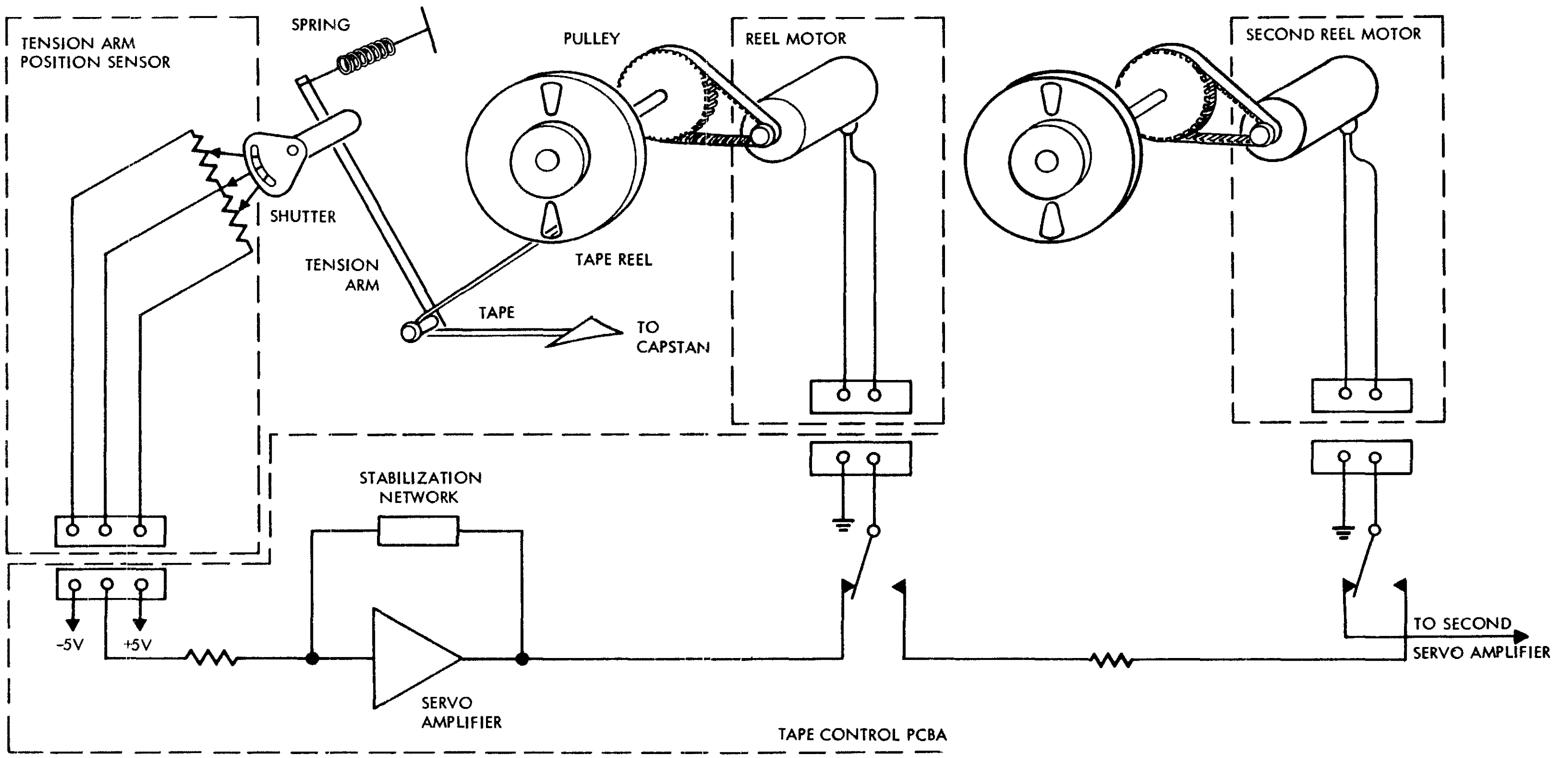


Figure 4-6. Reel Servo Diagram

The tension arms establish tape tension and isolate the inertia of the reels from the capstan. Low-friction ball bearing guides are used to minimize tape tension variations. The angular position of the tension arm is sensed by a photosensitive potentiometer which produces a voltage output proportional to the arm position. This output is amplified and drives the reel motor in the direction to center the tension arm. The geometry of the tension arm and spring ensures that only negligible tape tension changes occur as the storage arm moves through a 30-degree arc.

With the tape stationary, the storage arms take a position such that the amplified tension arm sensor output, when applied to the reel motor, produces enough torque to balance the spring torque. Initially, the sensor is set by rotating the shutter on the tension arm shaft so that the tension arms operate in the center of their range. The position of the tension arm changes for different steady-state capstan velocities. This occurs because the amplifier output varies with the motor back-emf requiring corresponding changes in voltages from the potentiometer.

When the capstan injects a tape velocity transient in either direction, the arm moves and the sensor output changes, driving the reel motor in the direction to recenter the arm.

Without tape, the arms rest against the stops and the tension-arm limit switch is open, removing power to all motors.

Each reel motor is driven by a linear amplifier with transitional lead servo stabilization. For example, for 12.5 ips transports, the low-frequency gain of the amplifier is 6 volts per volt. The zero of the stabilization network is at 1.5 Hz and the pole is at 7.5 Hz.

With 10v across the potentiometer, the gain is 3 volts per radian. The amplifier gain is 6 volts per volt and the motor gain is 15 radians per second per volt. The motor velocity is stepped down by a pulley ratio of 4 to 1 so that the open-loop gain (reel velocity divided by arm displacement) is 70 radians per second per radian. From this description, the arm displacement for the change in velocity from 12.5 ips forward to 12.5 ips reverse (i.e., 10 radians per second) is approximately one-seventh radian or 8 degrees. A voltage derived from the Rewind ramp generator is added to the feedback from the tension arm sensor. Therefore, displacement of the tension arm is not required to generate the amplifier output at rewind speed, thus minimizing the tension arm stroke requirement.

4.3.4 DATA ELECTRONICS

Information is recorded on tape in the Phase Encoded (PE) mode. The PE system interprets a flux change toward the magnetization direction of the IBG as a one bit. A flux change in the opposite direction represents a zero bit. A phase flux reversal is written between successive one bits or between successive zero bits to establish proper polarity. Thus, up to two flux changes are required per bit for the PE method of data encoding.

The PE method of recording data differs from the NRZI method in that the NRZI employs only one flux change in either direction to represent a one (1) bit, and the lack of a flux change to represent a zero (0) bit.

Figure 4-7 illustrates the basic recording waveform components of the NRZI and PE modes. Note that in the PE mode there is a flux shift within each cell period indicative of a one or zero bit. The direction of magnetic flux change on tape at the center of the bit cell determines its value (zero or one).

Figure 4-8 illustrates the relevant 9-track allocation, spacing, and format of 1600 cpi PE tape. Consecutive data channels are not allocated to

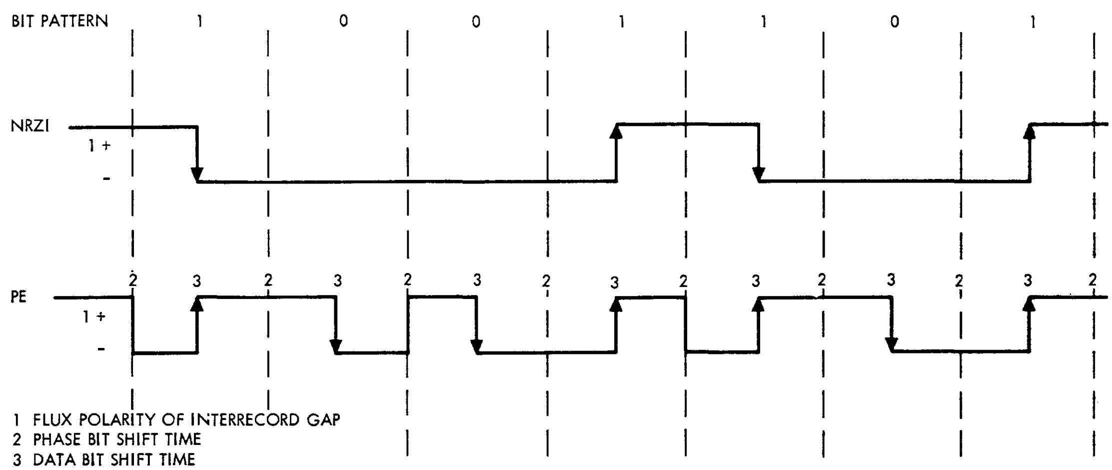


Figure 4-7. Comparison of NRZI and PE Recording Modes

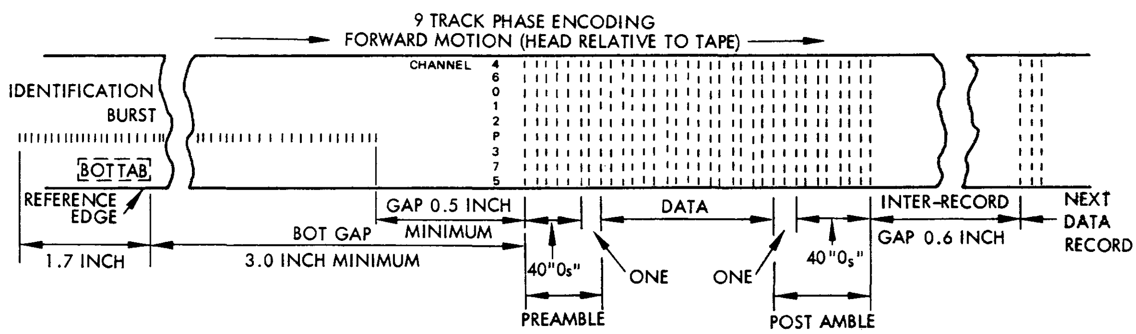


Figure 4-8. 9-Track PE Allocation, Spacing and Format

consecutive tracks. This organization increases tape system reliability because the most used data channels are located near the center of tape. Consequently, they are least subject to errors caused by contamination of tape.

The data block is preceded by a preamble consisting of 40 bytes of all zeros and one byte of all ones. Note that the data block is followed by a postamble which is the mirror image of the preamble, i.e., one byte of all ones followed by 40 bytes of all zeros.

NOTE

> The configuration of the preamble and postamble bursts are such that during a Read Reverse operation their functions are interchangeable.

During a Read operation, as tape passes over the Read/Write head, any flux pattern recorded on tape (one or zero) generates a waveform in its appropriate data track. It is important to note that during a Read Reverse operation the Read signal is inverted, i.e., a one bit is a negative transition and a zero bit is a positive transition.

Illustrated in Figure 4-9* are waveforms that occur on a channel during a write and read-back operation. Magnetization transitions recorded on tape are not perfectly sharp because of the limited resolution of the magnetic recording process.

During read-back, the voltage induced in the head is amplified, differentiated, and then applied to a Schmitt trigger and an envelope detector. The differentiator and Schmitt trigger form a peak detector. The envelope detector performs a gating function. Thus, the output is present on the interface line only when a data block is present.

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*Foldout drawing, see end of this section.

Figure 4-10* is a block diagram of one channel of data electronics and the relevant common control logic. This diagram is used for describing system operation.

4.3.4.1 Operation with a Dual Stack Head

The 7640 Tape Transport utilizes a dual stack head which enables simultaneous read and write operations to take place, thus permitting writing and checking of data in a single pass.

Gap scatter in both the write and read heads is held within tight limits so that correction is not necessary. Conversely, the azimuth angle of both heads is not held within such tight limits and correction is therefore necessary. The write head adjustment is provided by shimming the fixed head guides adjacent to the head so that the tape tracks at 90 degrees to the write head gap.

4.3.4.2 Data Recording

Assume that the transport is Selected, Ready, On-line, and has a Write Enable ring installed. The WRT POWER control line will therefore be at +5v, providing power for the head driver circuits.

When a SYNCHRONOUS FORWARD command is received, the MOTION signal generated on the Tape Control PCBA goes high, removing one input of OR gate U7.

In operation, the front edge of the SYNCHRONOUS FORWARD command is delayed and differentiated and the resulting pulse used to sample the condition of the SET WRITE STATUS line. If this is true, the following action takes place.

(1) The Write/Read mode flip-flop is set.

(2) The NWRT waveform becomes low.

*Foldout drawing, see end of this section.

(3) The -5v driver (Q3) is turned on.

(4) The erase head is energized.

(5) The C_D input of U3 goes high. The polarity of the field from the erase and write heads under these conditions is such that tape will be erased in an IBM-compatible direction.

Figure 4-11* is a timing diagram illustrating relationships of signals during data recording and should be referred to in conjunction with Figure 4-10.

The SFC command (Plot 1) enables the ramp generator which causes tape to accelerate to the prescribed velocity (Plot 2). After a time (T1) determined by the required Inter-Record Gap (IRG) displacement, the WRITE DATA inputs (Plot 3) together with the IWDS (Plot 4) are supplied to the interface connector. Preamble, data block, and postamble are recorded.

The WRITE DATA (IWD) input is received by interface receiver U1 and is strobed into flip-flop U3 at the trailing edge of the WRITE DATA STROBE (IWDS). On the Write Data lines (IWDP - IWD7) a one is a positive-going edge at data flux reversal time and a zero is a negative-going edge. The phase edge can be positive- or negative-going. Both outputs of flip-flop U3 are fed to head driver transistors Q1 and Q2, which cause current to flow in one half or the other of the center-tap head winding. Consequently, magnetization on the tape is maintained in the appropriate direction between changeovers and changes direction in accordance with the input signal IWD.

At the completion of the postamble, ISFC goes false after the post-record delay time (T2). The ramp generator is disabled and the tape velocity decelerates to zero.

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*Foldout drawing, see end of this section.

The IRG displacement consists of the following.

(1) The stop distance: the distance traveled during the tape deceleration period to zero velocity.

(2) The start distance: the distance traveled while tape is accelerating to the prescribed velocity.

(3) An additional distance determined by the pre-record time (T1), from the ISFC command going true to the time of the first IWDS and the post-record time (T2), from the end of the postamble to ISFC going false. (Time delays T1 and T2 are provided by the customer's controller.)

4.3.4.3 Overwrite Operation

The Overwrite function allows updating (rewriting) of a selected record. The new data block to be inserted must be exactly the same length as the data block being replaced. This restriction is necessary since replacing a block of data with a block longer than the original could result in an IRG distance which is less than the minimum allowed, or in writing over the next record. If the new data is shorter than the existing block, errors could result since some unerased portion of the old data would remain.

Additionally, when write and erase currents are switched off abruptly there is a small area of tape which is influenced by the collapsing magnetic fields of the heads. This constitutes flux transients on the tape which appear as spurious signals when read back. The Overwrite feature of the 7640 Transport has effectively eliminated this problem by turning the write current off slowly while tape is still in motion.

NOTE

Refer to PERTEC Application Note No. 70711 concerning the control and timing restrictions associated with Overwrite.

To update a previously recorded record the transport must be Selected, Ready, On-line, and have a Write Enable ring installed. Additionally, the Overwrite (IOVW) signal from the controller must be true and coincident with ISWS and ISFC.

Overwrite operation is terminated by the IWARS signal disabling the Write Power circuitry. This action causes the write current to ramp down to zero as the tape decelerates to rest. The transient pulse, generated when the write current is switched off, is spread over a longer distance on the tape and produces a negligible signal on replay.

4.3.4.4 Data Reproduction

When a SFC is received, the following occurs.

(1) The MOTION signal generated on the Tape Control PCBA goes true so that NAND gate U4 (Figure 4-10) is enabled.

(2) The Forward ramp generator is enabled and the tape accelerates to the prescribed velocity.

Figure 4-12* illustrates typical PE read timing and waveforms and should be referred to in conjunction with Figure 4-10. Data signals from the magnetic head at a level of approximately 5 to 15 millivolts peak-to-peak are fed by a shielded cable to the read amplifier (Plot 2). The read amplifier gain is adjusted so that the output of the differentiator is 6v peak-to-peak (Plot 3).

*Foldout drawing, see end of this section.

The differentiated signal is fed to a Schmitt trigger which squares the signal and outputs it to LINE DRIVER U4 (Plot 4). The differentiated signal is also applied to the envelope detector which requires four successive characters greater than the threshold before its output goes high to enable the LINE DRIVER U4 (Plot 5). The output of the envelope detector goes false when the differentiated read signal envelope goes below the threshold for more than two successive characters.

In a dual stack transport, the read system is always enabled whether the transport is in the Write or Read mode. However, in the Write mode where the reading facility is used to check the data that have been recorded, the NWRT waveform is low and a high threshold level of approximately 30 percent is generated. This ensures that data are written with enough margin to assure data recovery when tape is read on another transport.

When the transport is in the Read mode, the NWRT waveform is high and a threshold level of approximately 10 percent is generated, which is only sufficient to reject system noise.

The IRTH2 line, when true and the transport is in the Read mode, will generate a read threshold of approximately 5 percent to enable the user to recover very low amplitude data. Operation at this threshold is recommended only after an attempt has been made to read the data at the normal read threshold level.

4.3.5 TAPE CONTROL SYSTEM

The second major electronic subsystem consists of the circuits necessary to control tape motion. This includes manual controls, interlocks, and logic. The operation can best be described by detailing the Bring-to-Load-Point sequence, subsequent tape motion commands, the Rewind sequence, and subsequent unloading of tape.

Figure 4-13* is a logic diagram for the Tape Control system. Note that the identification of the elements in Figure 4-13 is closely related to the Tape Control schematic. One-hundred percent correspondence is not possible since the schematic contains many functions which are only represented in simplified form in Figure 4-13.

4.3.5.1 Bring-to-Load-Point Sequence

The system will be described by considering the sequence required to bring a tape to the BOT (Load Point). Figure 4-14 shows the waveforms during the operation.

Associated with each of the momentary manual control switches is a "switch clean-up" flip-flop (U13-C, U11-B, U1-D) which eliminates the problems of switch contact bounce. Relay K1 has four changeover contacts, three of which (K1A, K1B, and K1C) are used to disconnect the reel and capstan servo motors, the fourth (K1D) is used in conjunction with the tension arm limit switch as a system interlock. The tension arm limit switch is operated by a cam on the take-up reel tension arm and is closed when the arm is in its normal operating position. The tension arm limit switch opens at both extremes of the arm travel so that protection against over-tension as well as under-tension conditions is provided.

The Write Lockout (WLO) switch is located on the File Protect assembly located behind the supply reel. The switch is closed when a Write Enable

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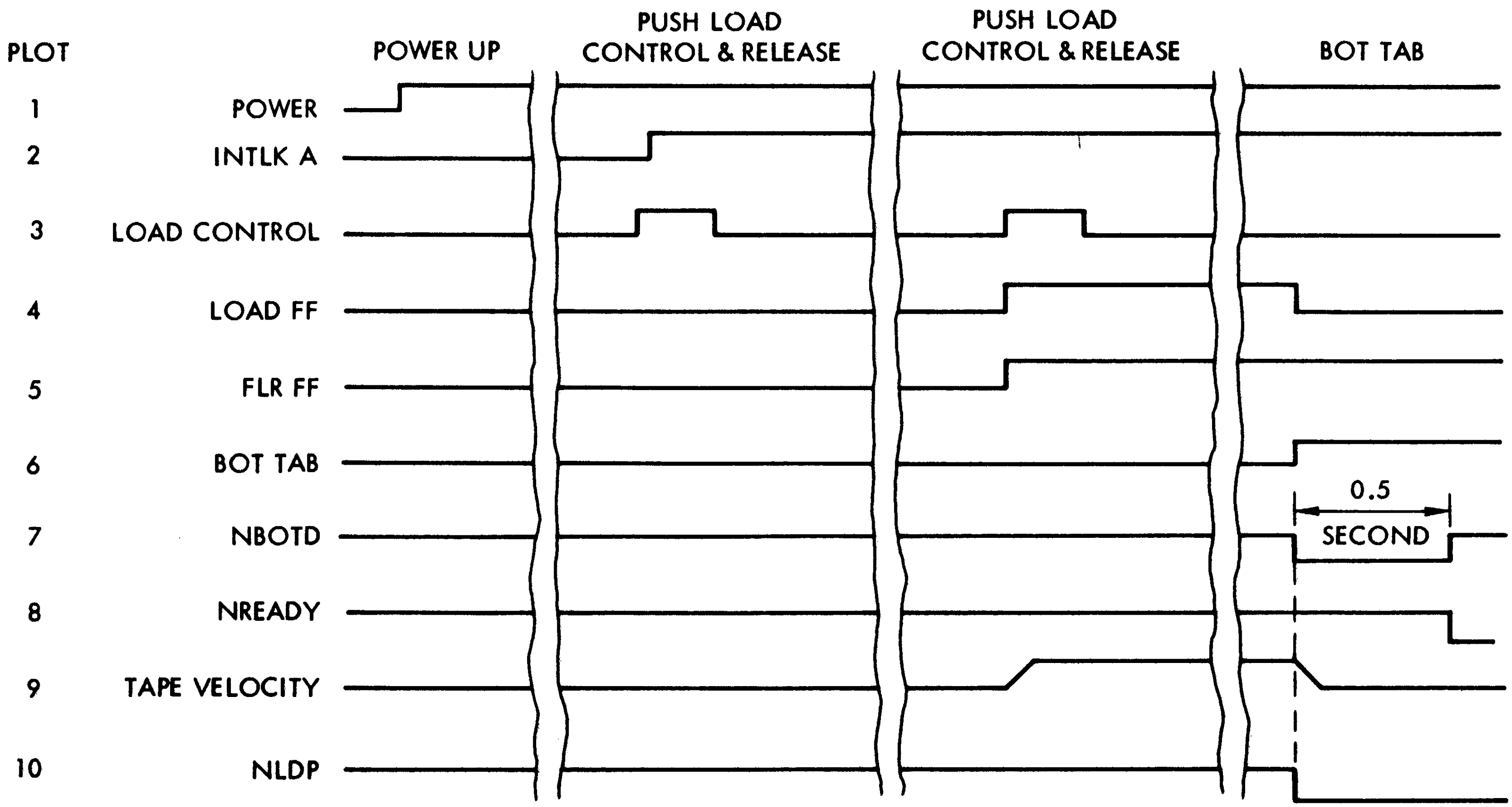
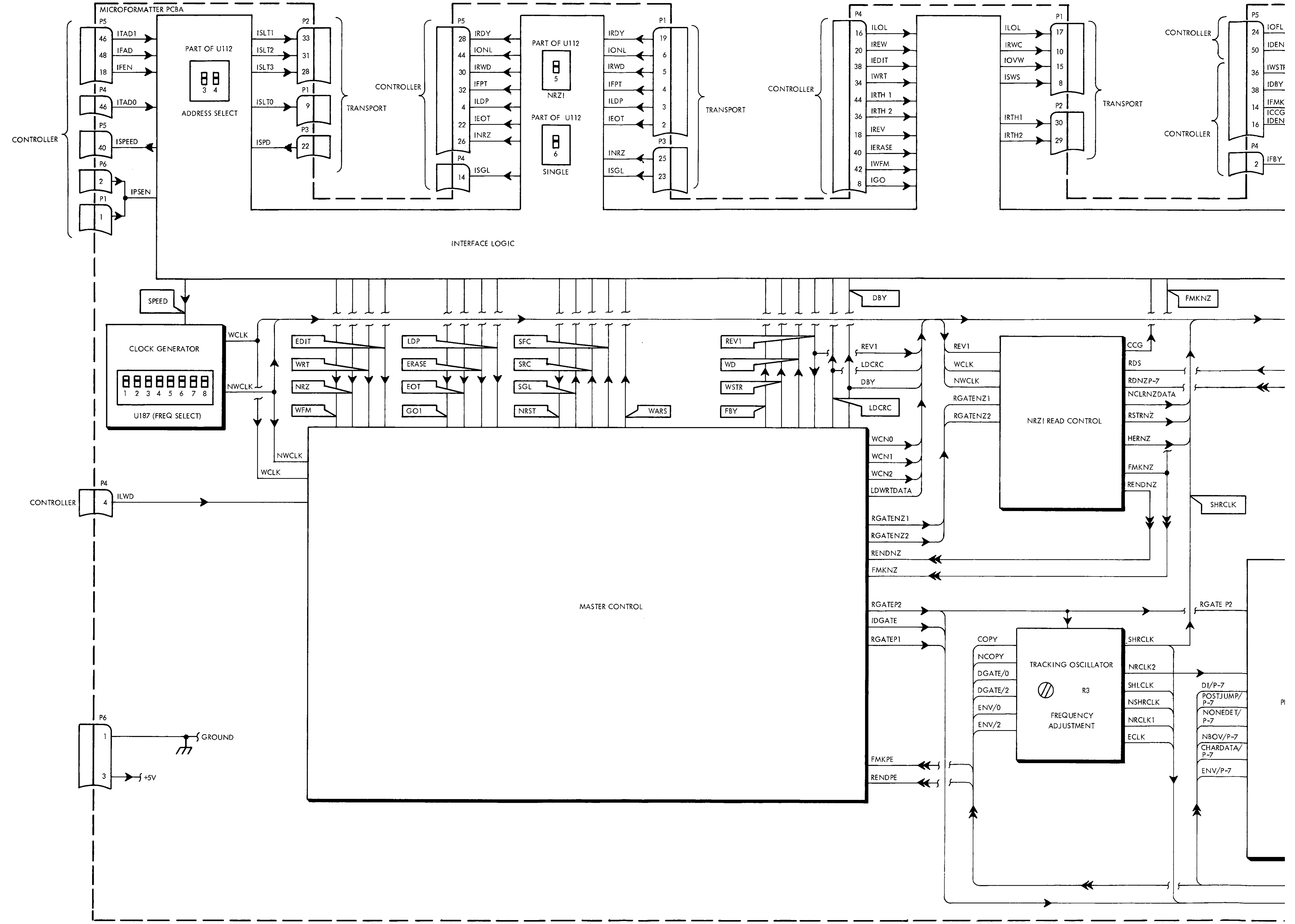
*Foldout drawing, see end of this section.



NOTES:
1. HIGH LEVEL IS TRUE

Figure 4-14. Tape Control Waveforms During Load Sequence



MICROFORMATTER PCBA
CONTROLLER
TRANSPORT
PART OF U112
ADDRESS SELECT
NRZI
SINGLE
INTERFACE LOGIC
CLOCK GENERATOR
U187 (FREQ SELECT)
MASTER CONTROL
NRZI READ CONTROL
TRACKING OSCILLATOR
R3
FREQUENCY ADJUSTMENT
GROUND
+5V

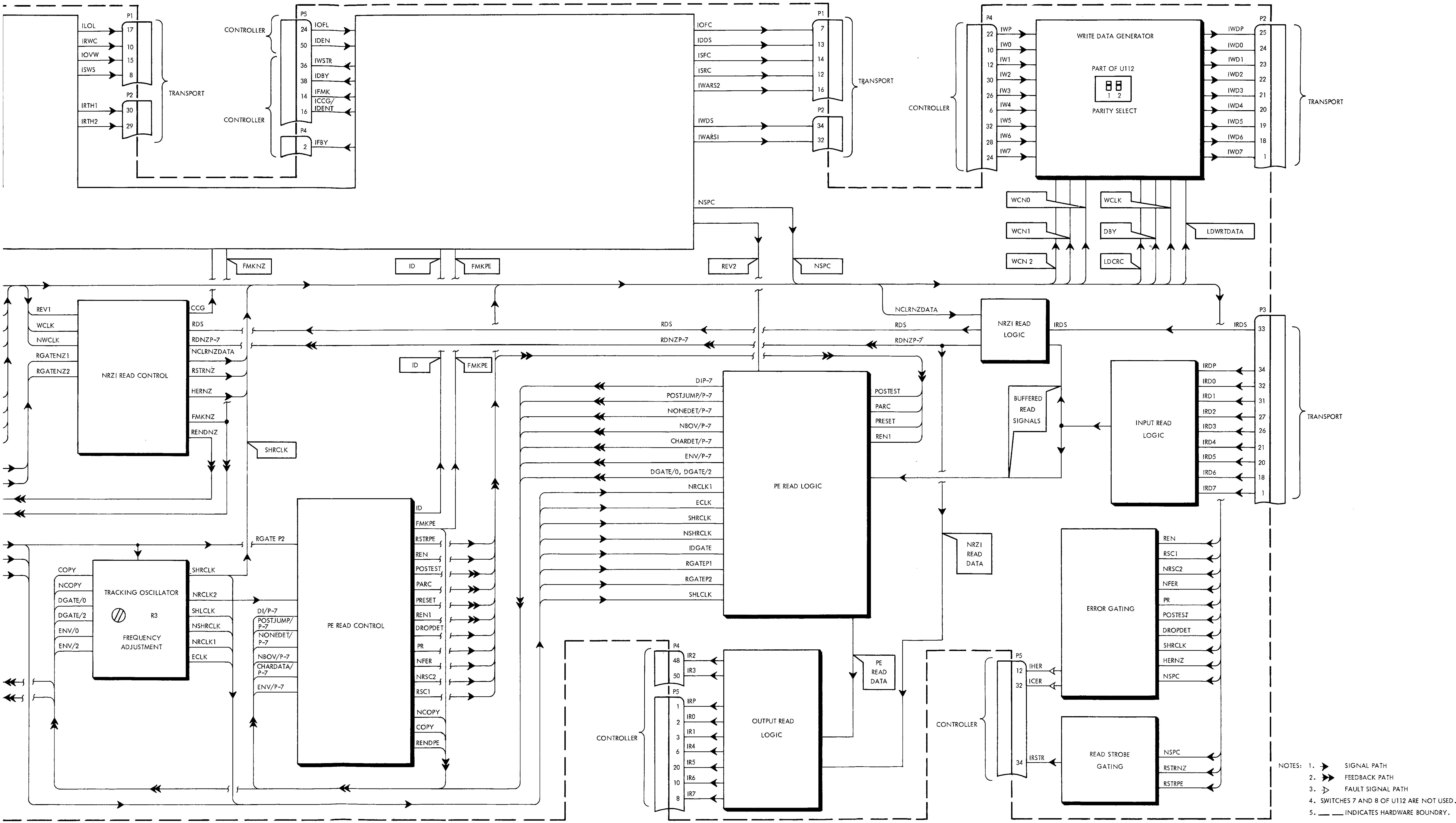


Figure 4-1. Dual Microformatter Block Diagram

ring is mounted on the supply reel. The probe, which detects the Write Enable ring, is retracted when power is switched on and relay K1 is closed. A solenoid, whose transistor driver is supplied with base current when the LOAD control is depressed or the tension arm limit switch is closed, retracts the probe.

Write current is also supplied upon demand through K1D and the WLO switch.

4.3.5.2 Actuate POWER Control

When power is turned on initially (Plot 1), the relay contacts and the tension arm limit switch are open. The INTLK-A signal is low and is connected either directly or through appropriate gates to the reset inputs of the five control flip-flops RW1, RW2, On-line, Load, and FLR (U14-A, U15-B, U9-B, U15-A, and U17-C).

4.3.5.3 Depress LOAD Control (First Time)

When the LOAD control is depressed for the first time (Plot 3), the relay driver for K1 is energized, the four contacts close activating the reel servos which tension the tape, thus closing the tension arm limit switch. The tension arm limit switch supplies an alternate source of base current for the relay driver, thus latching the relay (which then remains activated after the LOAD control is released). When K1D closes, a high level appears at the INTLK-A output (Plot 2), removing the reset from the control flip-flops. The Load flip-flop U15-A is not set by the first operation of the LOAD control because at the time that the T input of U15-A goes low (which normally sets the flip-flop), the INTLK-A signal is still holding the reset input low.

If, at any time, the tension arm moves outside its operating region, the interlock relay de-energizes, power is disconnected from the motors, and the INTLK-A signal returns to the low state, resetting the five control flip-flops.

4.3.5.4 Depress LOAD Control (Second Time)

When the LOAD control is depressed momentarily a second time (Plot 3), the following sequence occurs.

(1) Since the INTLK-A signal is high, the Load flip-flop sets and its Q output goes high enabling the Forward ramp generator (not shown) that drives the capstan servo. Tape accelerates to the specified speed (Plot 9) and continues to move until the BOT tab reaches the BOT sensor, at which time the BOT signal goes high, enabling one input of AND gate U20-B. Also, the single-shot is triggered, generating an 0.5-sec negative-going waveform (NBOTD) (Plot 7).

(2) Since the LOAD waveform and the NRW1 waveform are high at this time, AND gate U20-B is enabled (Plot 10) and the Load flip-flop is reset. This causes the tape to decelerate to rest with the photo-tab under the photo-tab sensor.

At this time, all three inputs to AND gate U22-B are high so that the ILDP waveform is low indicating that the transport is at Load Point; the Load lamp driver is enabled.

At the end of the 0.5-sec delay, the NBOTD waveform goes high and, since the other inputs to gate U22-A are high at this time, the NREADY waveform at the output of gate U22-A goes low (Plot 8), enabling one input to AND gate U13-B.

(3) The setting of the FLR flip-flop causes the NFLR waveform to go low, disabling AND gate U17-A which inhibits the possibility of action from further manual LOAD commands.

4.3.5.5 Depress ON LINE Control

If the ON LINE control is momentarily depressed, the On-line flip-flop U9-B is set (if it is depressed a second time, U9-B is reset), enabling the second input of AND gate U13-B. The $\overline{Q}$ output of flip-flop U9-B enables the On-line lamp driver. The output of gate U3-B goes low, indicating that the transport is Ready. If the transport is Selected, the output of inverter U4-C (Selected, Ready, On-line (SRO)) goes high.

Whenever the transport is On-line, the manual REWIND control is disabled by gate U6-B.

If the transport is Selected, the ISLT waveform is low. The following options are available.

(1) If W2 is not present, then the SLT waveform goes high-true.

(2) If W2 is present, SLT goes true only if the transport is also On-line.

(3) If W3 is not present, the SLTA waveform is permanently high. This option is used when interrogation of transport status lines is required whether the transport is Selected or not.

(4) If W3 is present, the status lines are gated with the SLT waveform.

Whenever the FLR or INTLK-A waveforms are low, the On-line flip-flop is held reset by OR gate U11-C, ensuring that the On-line flip-flop cannot be set until the interlock has been made and the First-Load-or-Rewind (FLR) sequence has been entered. The On-line flip-flop can be reset from the interface by the OFF LINE command (OFFC) via interface receiver U10-D.

The transport is now ready to receive external commands.

4.3.5.6 Operation From External Commands

Assuming the transport is Selected, Ready, and On-line (SRO is high), receipt of a SYNCHRONOUS FORWARD command will cause the output of interface receiver U4-D to go high and the output of AND gate U12-C to go low. The MOTION signal will go high and the Forward ramp generator will be enabled.

The MOTION signal is delayed approximately 10 μsec, differentiated, and a positive-going "GO" pulse generated at the output of differentiator $\delta 1$. This pulse samples the status of the SET WRITE STATUS (ISWS) line. If ISWS is true, indicating that the Write mode is required, then the Write/Read flip-flop U14-B is set and the NWRT waveform goes low. If ISWS is false, flip-flop U14-B is held reset and the NWRT waveform is high. In the case of a SYNCHRONOUS REVERSE command, a similar sequence of events occurs.

If the BOT tab is encountered during the execution of a SYNCHRONOUS REVERSE command, the BOT signal goes high and the single-shot is triggered. As a result, AND gate U12-D is disabled, inhibiting the action of the SYNCHRONOUS REVERSE command. The NBOTD waveform goes low for 0.5 second so that the transport becomes Not Ready (via gates U22-A, U13-B, and U3-B) for this period of time.

4.3.5.7 Operation From Control Panel - Forward

Forward tape motion, in response to a remote input command, was previously described. When the transport is in the Off-line mode (NONLINE is true) and the FORWARD control is depressed, tape will run forward at the specified speed until the control is again depressed (or until the transport is placed in the On-line mode).

NOTE

> The FORWARD control should be deactivated prior to placing the transport in the On-line mode; failure to deactivate the FORWARD control will cause tape to advance the next time the transport is placed in the Off-line mode.

The transport cannot write information on the tape when motion is caused by the FORWARD control since the Write/Read flip-flop is held reset by the Non-line mode via gate U13-B.

4.3.5.8 Operation From Control Panel - Reverse

Reverse operation is identical to the description for Forward operation in Paragraph 4.3.5.7, except for the direction of tape motion.

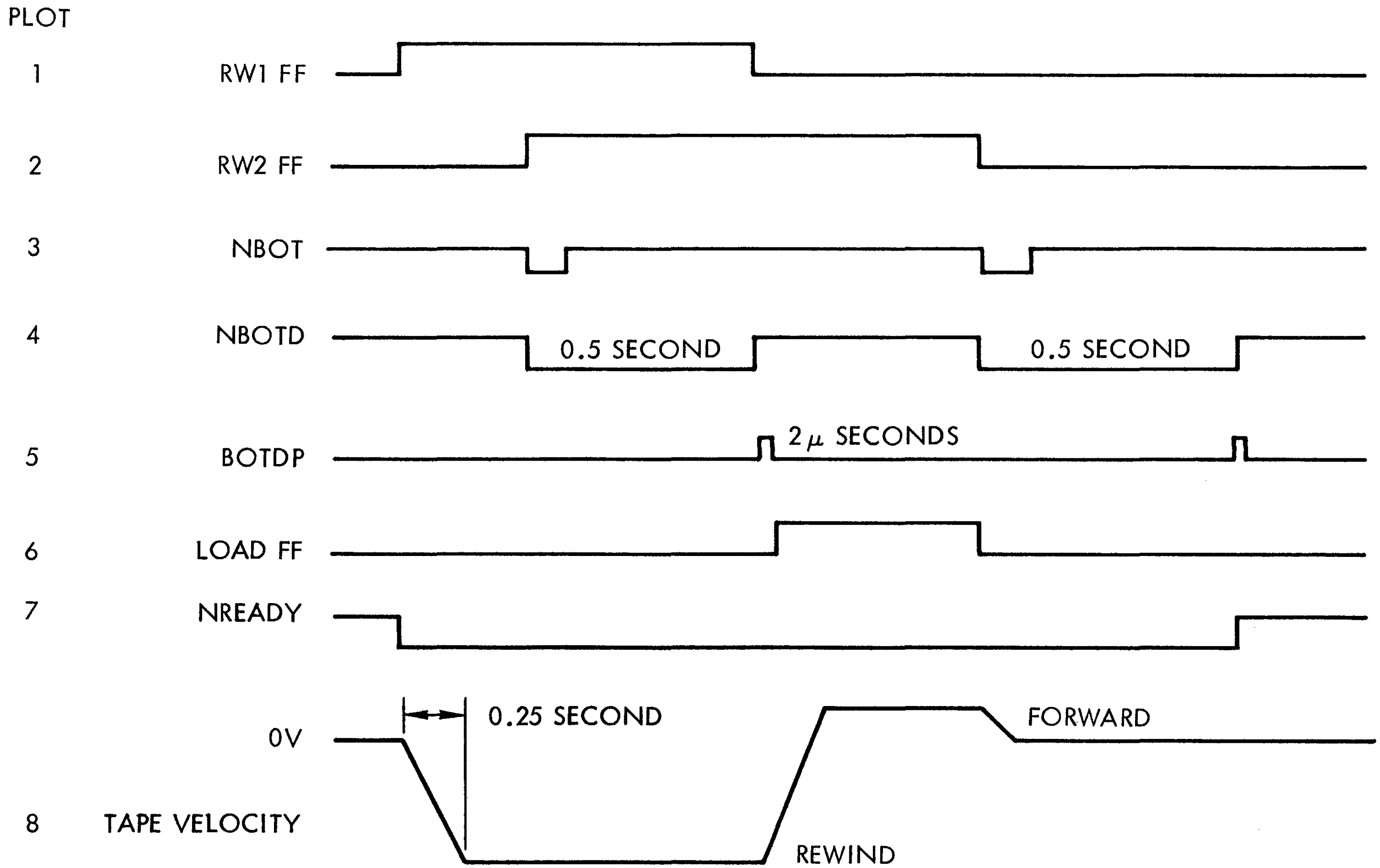
4.3.5.9 Rewind Sequence, Case 1 - Tape Not at Load Point

This is the normal Rewind-to-Load-Point sequence that results from either a remote or manual command. Figure 4-15 shows the waveforms that occur during the operation.

In response to either a remote or manual REWIND command given the correct conditions, the RW1 flip-flop U14-A is set (Plot 1). The $\overline{Q}$ output of the flip-flop enables the Rewind ramp generator and the tape accelerates to the rewind velocity in approximately 0.25 second (Plot 8).

When the BOT tab is detected, flip-flop RW2 (U15-B) is set on the leading edge of the NBOT waveform (Plot 3). The 0.5-sec single-shot is triggered (Plot 4). At the end of the 0.5-sec delay, the trailing edge of the NBOTD waveform is differentiated by differentiator $\delta 2$, generating a positive-going BOTDP pulse (Plot 5), which resets RW1 via U17-B. The $\overline{Q}$ output of flip-flop RW1 goes high, disabling the Rewind ramp generator so that the tape decelerates to rest. The Load flip-flop U15-A is also set via gates U17-B and U16-E. This enables the Forward ramp generator (Plot 6).

The timing characteristics of the ramp generators are such that the BOT tab overshoots the photosensor and then returns. When the BOT tab is detected for the second time, the 0.5-sec single-shot is triggered (Plot 4)



NOTES:
1. HIGH LEVEL IS TRUE

Figure 4-15. Tape Control Waveforms During Rewind to Load Point Sequence and AND gate U20-B is enabled and its output goes low, resetting the RW2 and Load flip-flops (Plots 2 and 6). The Forward ramp generator is thus disabled and the tape decelerates to rest. The delay between the LOAD waveform and AND gate U20-B ensures that the reset waveform is sufficiently long. At the end of the 0.5-sec period, the NBOTD waveform goes high which causes NREADY to go low and, if SLT is high at this time, gate U6-C is enabled and the SRO waveform goes true.

The $\overline{Q}$ output of the RW2 flip-flop is low throughout the Rewind sequence and is used to generate the REWINDING (IRWD) interface waveform.

4.3.5.10 Rewind Sequence, Case 2 - Tape at Load Point

A manual REWIND command initiates the Rewind sequence as just described. In this case, however, the tape unwinds from the take-up reel and tape tension is lost. Remote REWIND commands are inhibited by the NBOT waveform at AND gate U5-A; i.e., it is impossible to unload tape remotely - operator intervention is required.

4.3.5.11 Ready Mode From Tape Not at Load Point

An option is available which allows the transport to be placed in the Ready mode after a power-off, power-on sequence even though tape has previously been brought beyond the Load Point, e.g., in the middle of a reel.

When this option is present (by deleting jumper W4) depress the LOAD control once to establish tape tension, then depress the ON LINE control. The READY line will go true and the transport can accept remote commands.

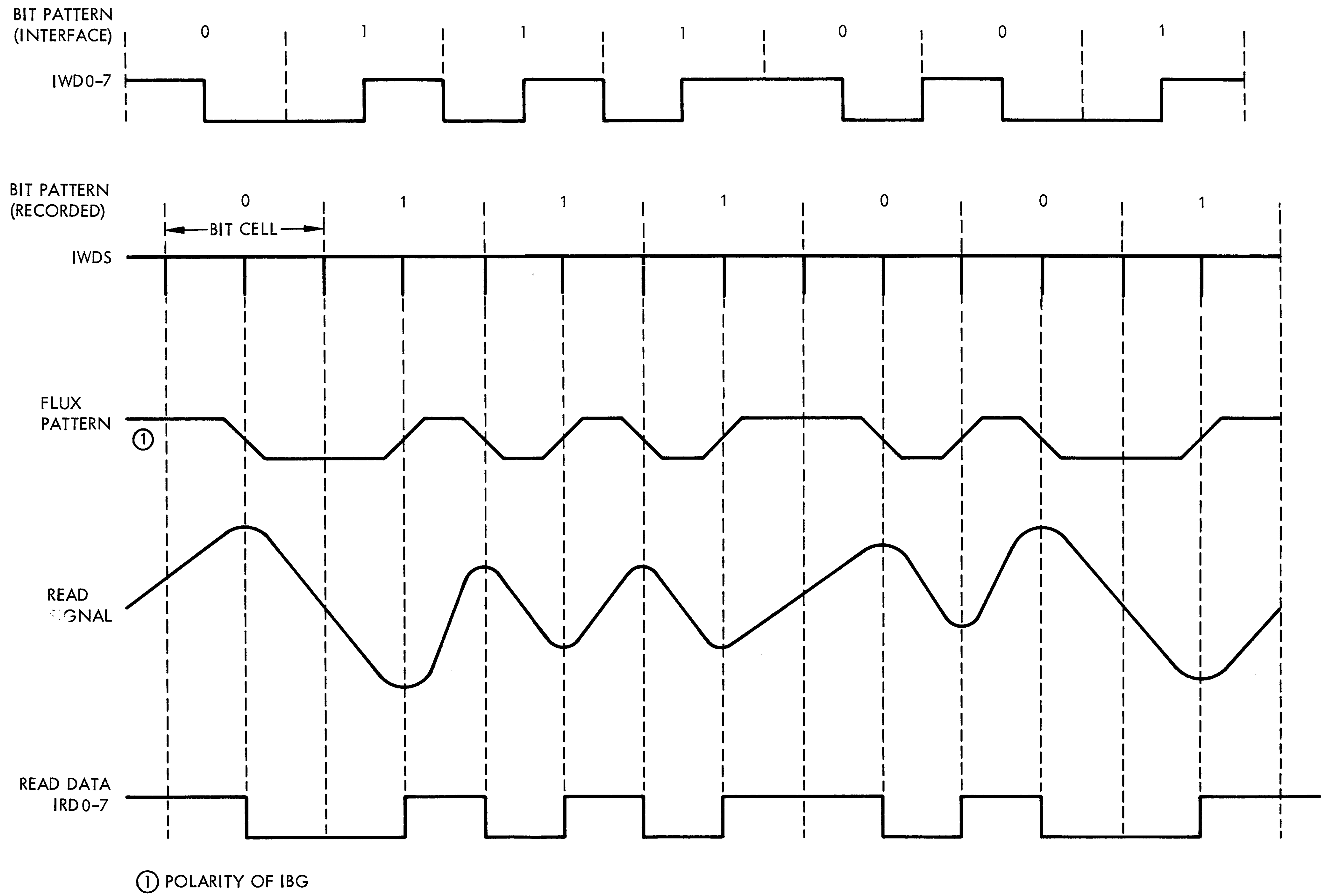


Figure 4-9. PE Write and Read Waveforms

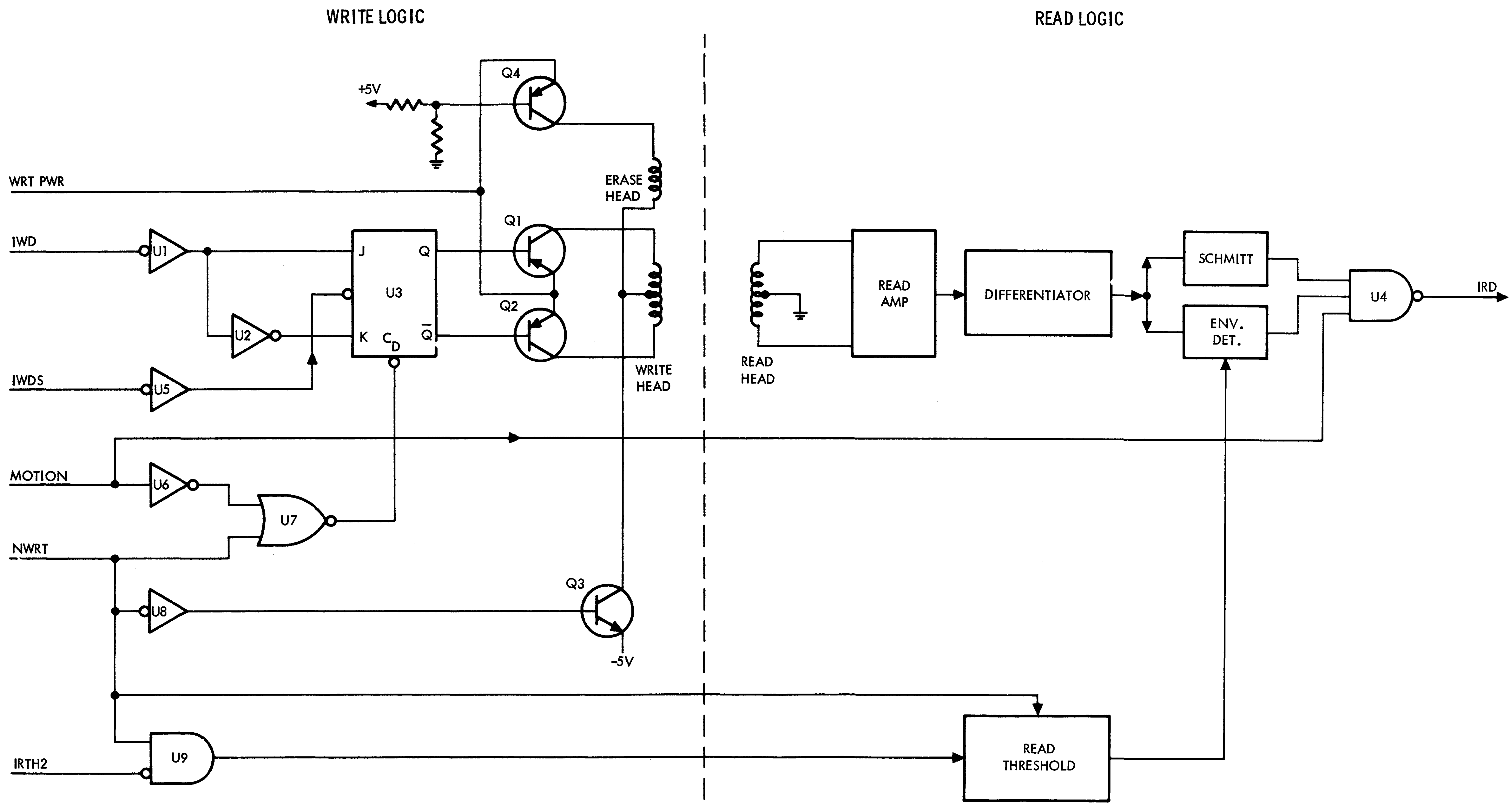


Figure 4-10. One Channel of Data Electronics

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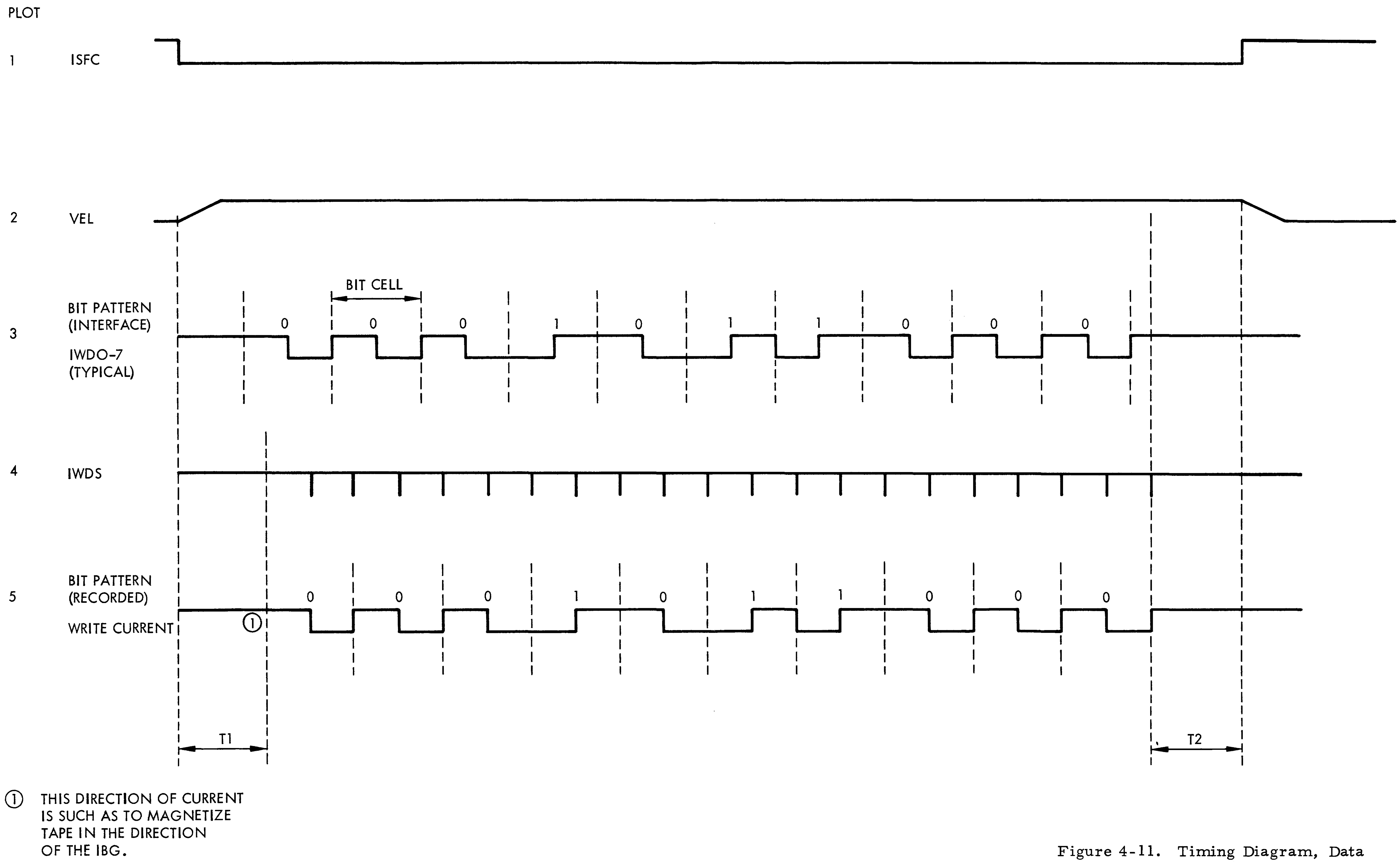
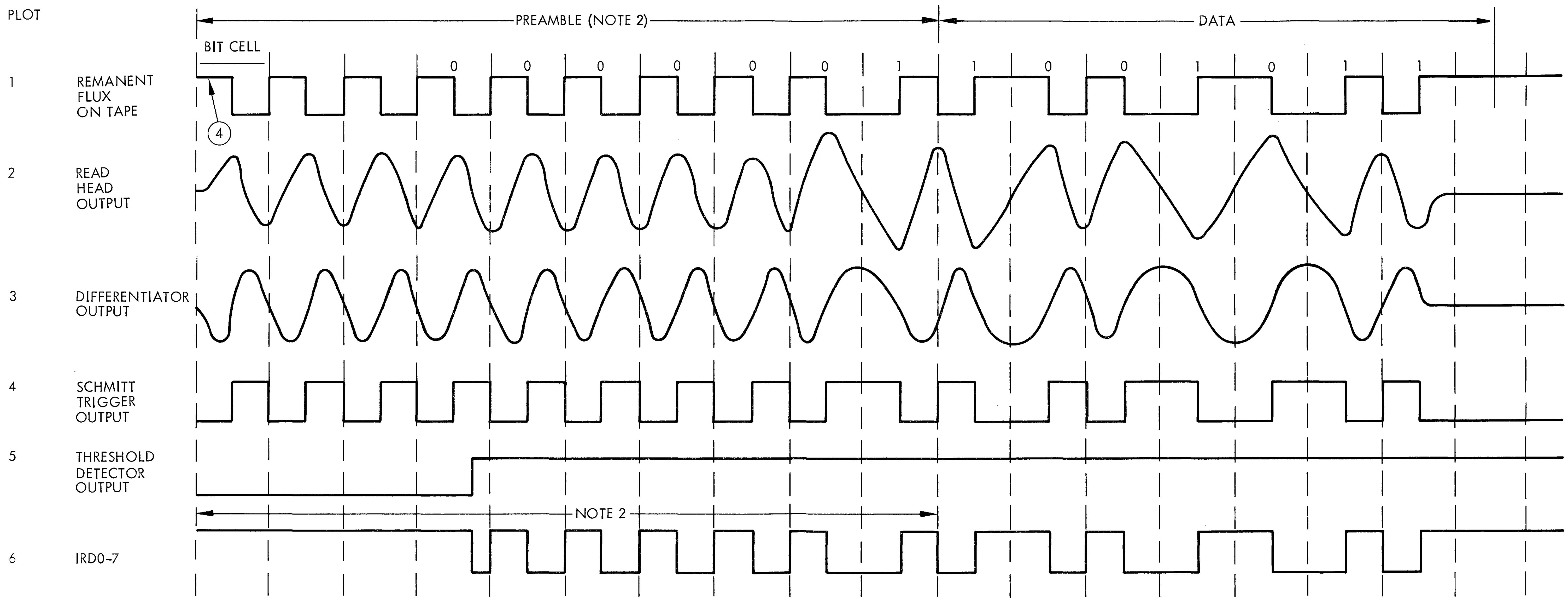
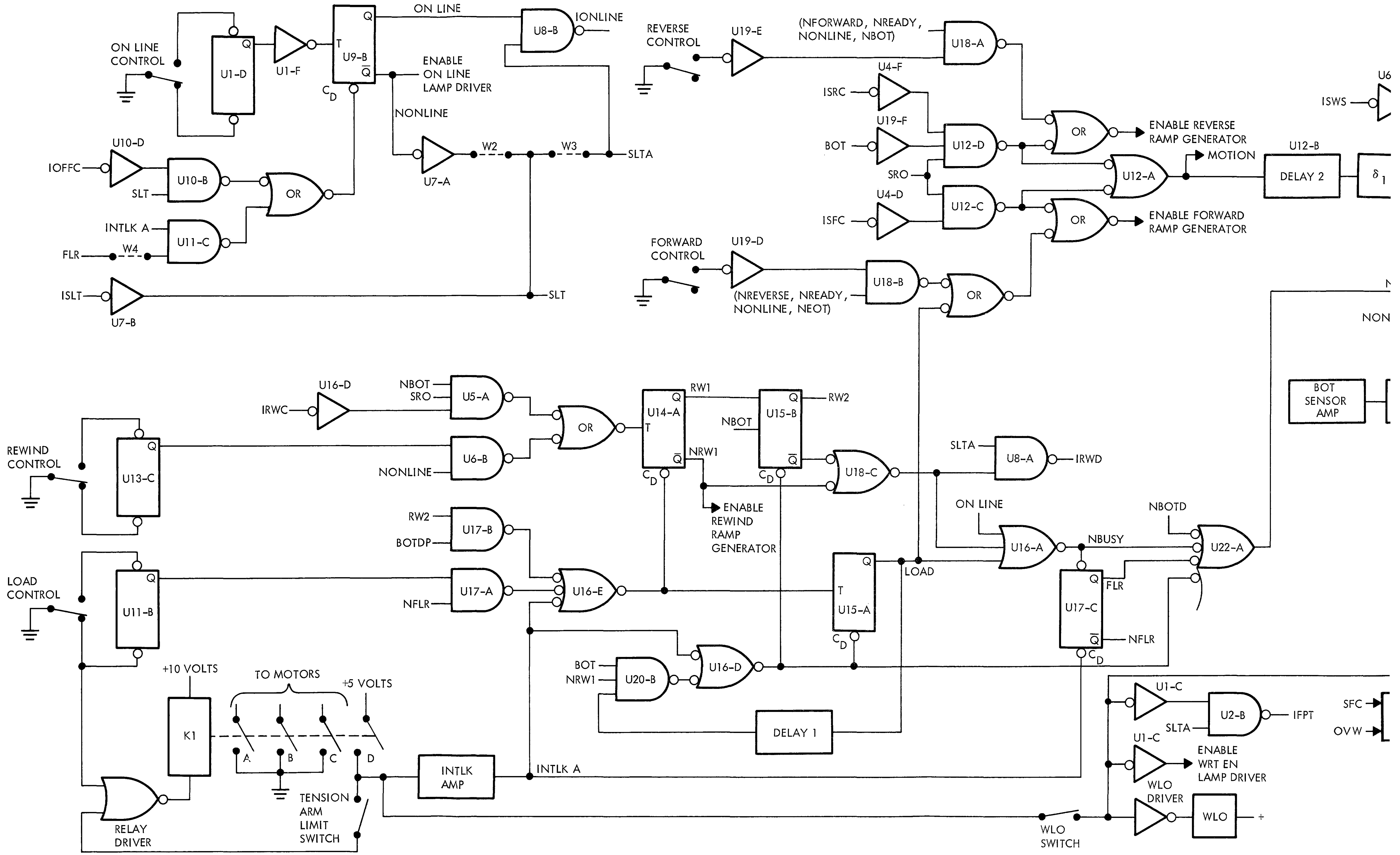


Figure 4-11. Timing Diagram, Data Recording



NOTES:
1. TRANSPORT MUST BE SELECTED, READY, AND ON-LINE AND GATED WITH SFC OR SRC.
2. PREAMBLE IS SHOWN SHORTENED TO SIMPLIFY DRAWING. PREAMBLE CONSISTS OF 40 ZEROS FOLLOWED BY ONE 1.
3. POSTAMBLE NOT SHOWN. POSTAMBLE CONSISTS OF ONE 1 FOLLOWED BY 40 ZEROES.
4. FLUX POLARITY OF INTERBLOCK GAP.

Figure 4-12. Timing Diagram, Data Reproduction



ON LINE CONTROL
U1-D
U1-F
U9-B
ON LINE
U8-B
IONLINE
ENABLE ON LINE LAMP DRIVER
NONLINE
U7-A
W2
W3
SLTA
U10-D
IOFFC
U10-B
SLT
OR
INTLK A
U11-C
FLR
W4
ISLT
U7-B
SLT
REVERSE CONTROL
U19-E
(NFORWARD, NREADY, NONLINE, NBOT)
U18-A
U4-F
ISRC
U19-F
BOT
U12-D
SRO
U4-D
ISFC
U12-C
OR
ENABLE REVERSE RAMP GENERATOR
MOTION
U12-A
U12-B
DELAY 2
ENABLE FORWARD RAMP GENERATOR
FORWARD CONTROL
U19-D
U18-B
(NREVERSE, NREADY, NONLINE, NEOT)
ISWS
NON
U16-D
IRWC
NBOT
SRO
U5-A
U6-B
NONLINE
REWIND CONTROL
U13-C
U14-A
RW1
NRW1
U15-B
RW2
NBOT
U18-C
ENABLE REWIND RAMP GENERATOR
SLTA
U8-A
IRWD
ON LINE
U16-A
NBUSY
NBOTD
U22-A
BOT SENSOR AMP
RW2
U17-B
BOTDP
U17-A
NFLR
U16-E
LOAD CONTROL
U11-B
U15-A
LOAD
U17-C
FLR
NFLR
BOT
NRW1
U20-B
U16-D
DELAY 1
+10 VOLTS
TO MOTORS
+5 VOLTS
K1
A
B
C
D
TENSION ARM LIMIT SWITCH
INTLK AMP
INTLK A
RELAY DRIVER
U1-C
U2-B
IFPT
SLTA
U1-C
ENABLE WRT EN LAMP DRIVER
WLO DRIVER
WLO
WLO SWITCH
SFC
OVW

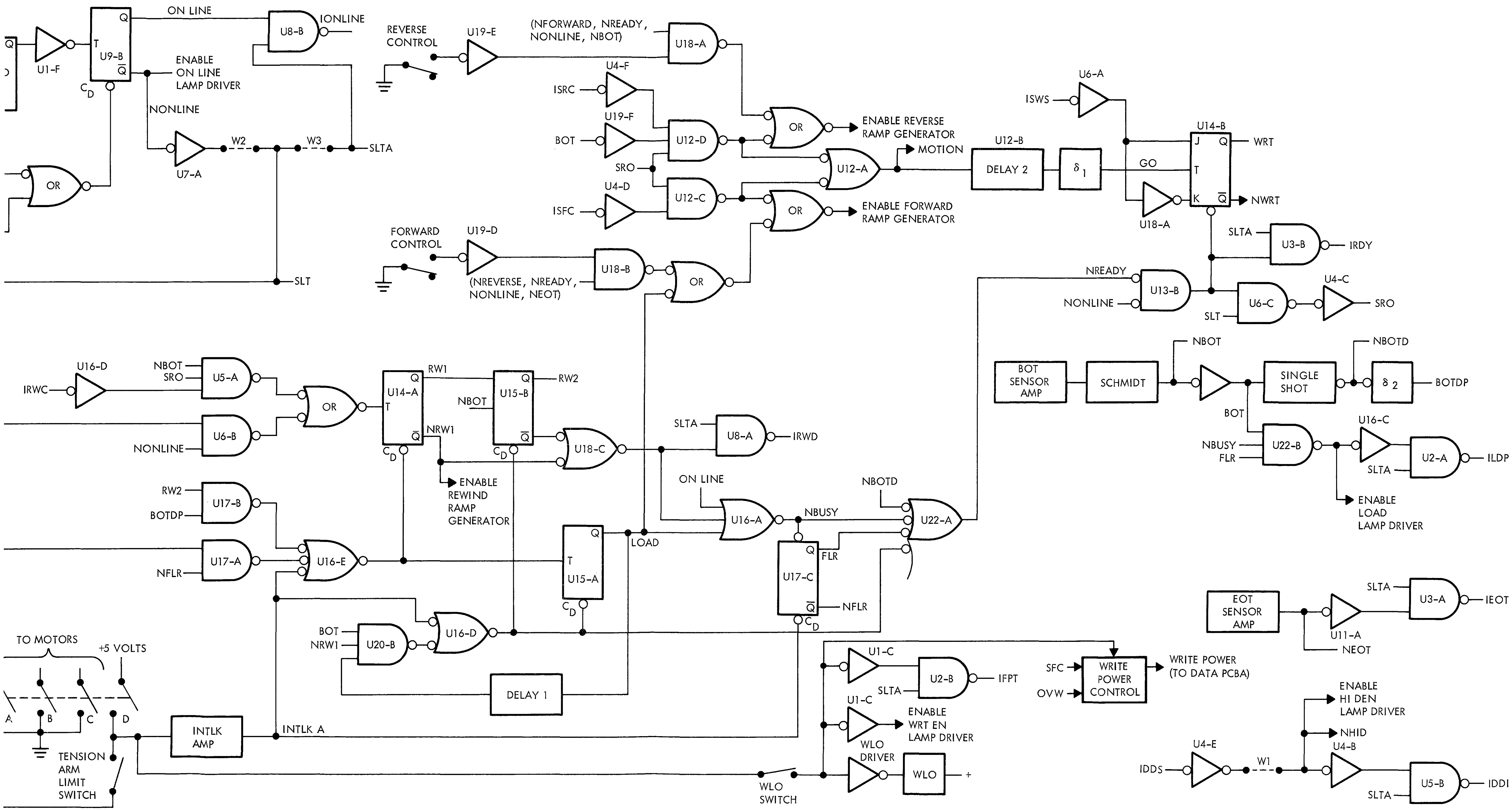


Figure 4-13. Block Diagram, Tape Control Logic

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SECTION V
PRINTED CIRCUIT BOARDS THEORY OF OPERATION

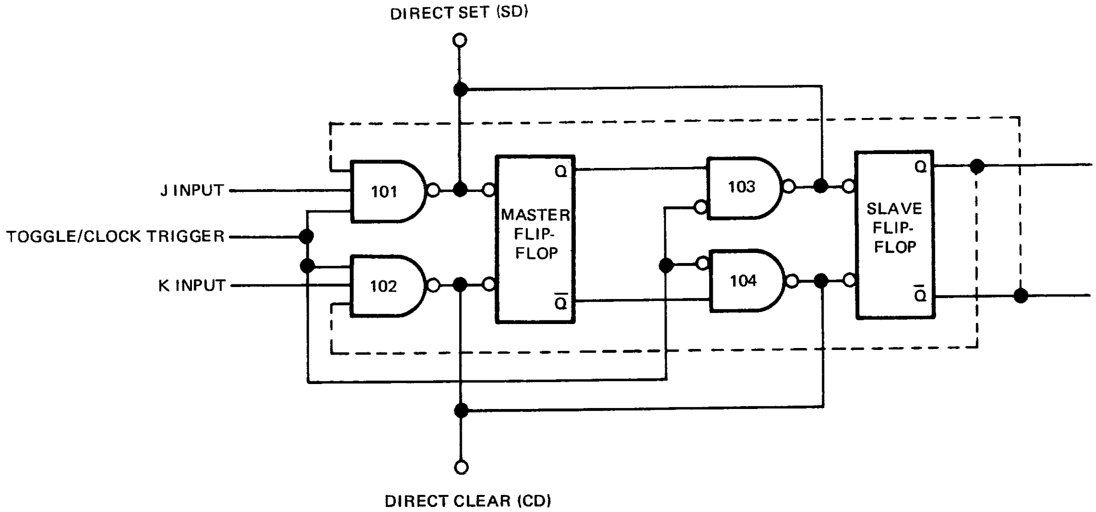
5.1 INTRODUCTION

This section contains the theory of operation of the printed circuit boards used in the Model 7640 Tape Transport. The schematic and assembly drawings for each board are contained at the end of Section VII.

A better understanding of the logic utilized in the tape transport can be gained when the operation of the J-K flip-flop is fully understood. The following paragraphs provide a brief summary of the operation of the 852 J-K flip-flop which is a type commonly used in the system.

This flip-flop operates on a "Master-Slave" principle. A logic diagram of the flip-flop is shown in Figure 5-1. The flip-flop is designed so that the threshold voltage of AND gates 101 and 102 is higher than that of AND gates 103 and 104. Since operation depends exclusively on voltage levels, any waveform of the proper voltage levels can trigger the J-K flip-flop.

Assume that the trigger voltage is initially low. As the trigger voltage goes high, AND gates 103 and 104 are disabled. Subsequently, AND gates 101 and 102 are enabled by the trigger pulse, the J and K inputs, and the information previously stored at the output of the "slave" unit. The J and K input information at this time is transferred to the input of the "master" unit. As the trigger voltage goes low, AND gates 101 and 102 are disabled. AND gates 103 and 104 are then enabled and the information stored in the "master" unit is transferred to the output of the "slave" unit.



NOTE: DASHED LINES SHOW CONNECTIONS AS J/K FLIP-FLOP

Figure 5-1. Simplified Logic Diagram, "Master-Slave" Flip-Flop

5.2 THEORY OF OPERATION

5.2.1 DATA H PCBA

The following is a description of the Data H PCBA (refer to Schematic No. 101580 and Assembly No. 101581).

The Data H PCBA is approximately 16 inches long with edge connectors (J102 and J103) at each end. These are interface connectors and are slotted to mate with keys in the mating plugs. There are three additional connectors on the Data H PCBA. J1 is used to connect power and control signals from the Tape Control PCBA. J2 and J3 are the connectors into which the write and read head cables, respectively, plug. Figure 5-2 illustrates the placement of each connector and test point.

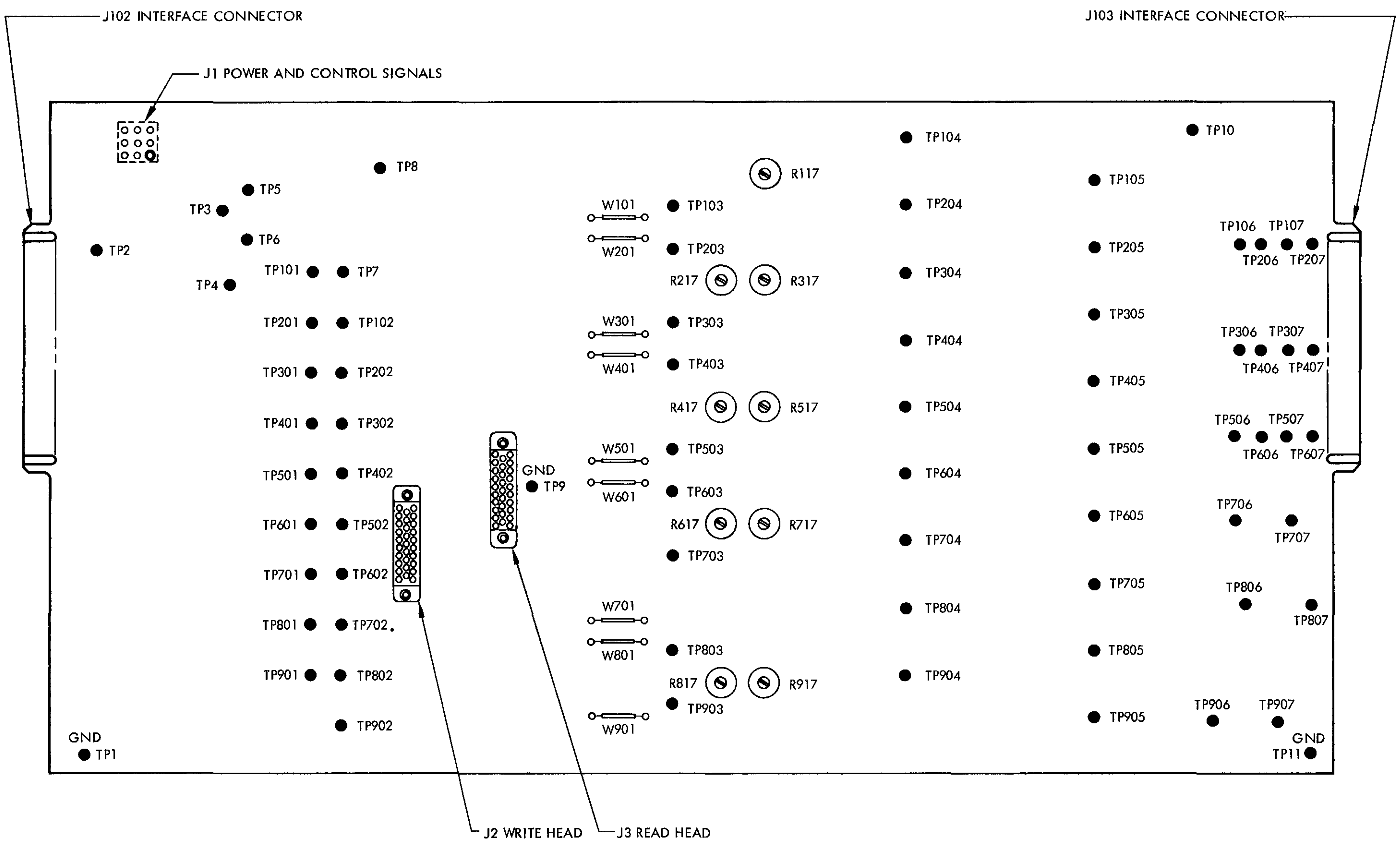


Figure 5-2. Data H PCBA Connector and Test Point Location

5.2.1.1 Circuit Description

The board operation is described with reference to circuit 100, which is identical to circuits 200 through 900. All interface signals relevant to writing data (nine WRITE DATA signals, IWD0 - IWD7, and WRITE DATA STROBE, IWDS) enter via J102 and are terminated by a resistor combination and an IC inverter.

Referring to circuit 100, the WRITE DATA PARITY (IWDP) data line is terminated by resistors R101, R102, and inverter U6-E. IWDP and its complement are applied to the "J" and "K" inputs of write buffer flip-flop U4-A. At the trailing edge of IWDS, which is applied to the toggle input of U4-A from power gate U2-A, flip-flop U4-A copies in the inverse of IWDP.

The outputs of the write buffer flip-flop drive write amplifier transistors Q101 and Q102 whose emitters are taken to +5v when the WRT POWER line (J8-4) is high. The transistor connected to the low (approximately 0v) output of the flip-flop will conduct and a current will flow in the associated half of the head winding. The center taps of all the windings are connected to the collector of Q3 which goes to -5v when the NWRT signal is false (i.e., the transport is in the Write mode). When the WRT POWER line is low (approximately 0v) or the NWRT signal is high, writing is inhibited because the write amplifier transistors cannot conduct. Similarly, the erase current supplied by transistor Q1 is inhibited when the WRT POWER line is low or the NWRT signal is high. In operation, the write current is defined by resistors R107 and R108. R109 is the associated damping resistor.

To improve the writing characteristics at 3200 flux reversals per inch (frpi) the write compensation capacitors C101 and C102 are used to cause an overshoot of current on each leading edge.

The head windings are phased so that the output of the write buffer flip-flops, when reset, cause current to flow in the standard "erase" direction. The write buffer register is held reset unless the transport is in the Write mode (NWRT is low) and tape is moving (MOTION, J8-6, is high).

The IWARS signal is received by resistors R22 and R23 but is not used on the Data PCBA. A jumper from J102-C (Data PCBA) to J101-15 (Tape Control PCBA) routes IWARS to the Overwrite circuitry on the Tape Control PCBA. IWARS is issued at the end of writing the postamble and is used in conjunction with IOVW to reset the WRT flip-flop on the Tape Control PCBA. The purpose of this is to turn off the write and erase current so that the adjacent record will not be erased during an Overwrite operation.

When reading data from tape, signals from the read head are fed via connector J3 to the read amplifier (U16-B) which is one-half of a dual operational amplifier IC. The amplifier output is maintained close to 0v in the absence of an input signal by the feedback path of resistors R114 and R116. The cutoff frequency of the amplifier is determined by C104 and R114. The operating gain of the amplifier is defined by resistor network R114, R116 and R117. R117 is a variable resistor used in the initial setup to set the differentiator output peak-to-peak amplitude.

Figure 5-3 illustrates typical read signal and timing relationships and should be referred to in the following discussion.

Amplifier U17-B is connected as a differentiator so that a peak in the output voltage of U16-B (TP103) is changed to a zero crossing at the output of amplifier U17-B (TP104). The gain of U17-B is determined by R118, R119, and C105. Since the capacitive reactance of C105 decreases as frequency increases, the gain of U17-B increases with frequency until

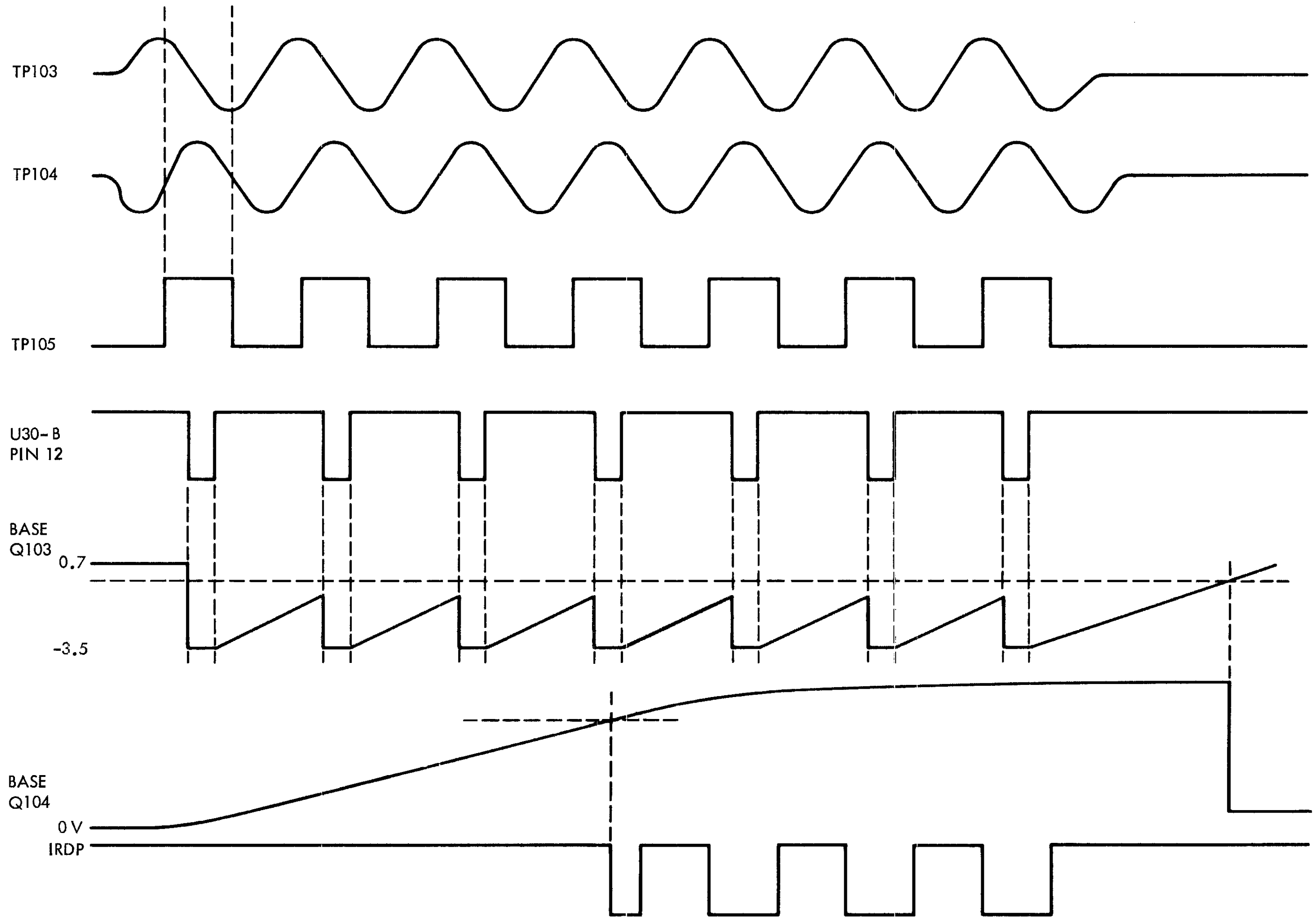


Figure 5-3. Timing and Signal Relationships,
One Channel Read Electronics

cut off by C106 and R119. Therefore, the amplitude of the envelope at TP104 is essentially independent of the data pattern. R117 should be adjusted so that the amplitude at TP104 is 6v peak-to-peak.

The differentiated signal is fed to U22-A, a Schmitt trigger (an amplifier with a small amount of positive feedback) which squares and inverts the signal (TP105). The read data is then applied to the power NAND gate U31-A.

The output of the differentiator (U17-B) is also fed to the input of the Envelope Detector (U22-B). The envelope detector compares the positive peaks of the differentiator signal (TP104) on Pin 9 of U22-B against the divided threshold level on Pin 8 of U22-B. The threshold level, when the transport is in the Write mode, is approximately 30 percent and is determined by R18 and R19. Q4 and Q5 are cut off during a Write operation. During a normal Read operation Q4 is conducting and the threshold is approximately 10 percent. If RTH2 is true during a Read operation, Q5 also conducts and the threshold drops to approximately 5 percent.

During the portion of the positive peak of the differentiated signal the output at Pin 12 of U22-B goes to approximately -4v; this also pulls C111 to -3.3v through CR104 and causes Q103 to cut off. When the peak falls below the threshold the output of U22-B goes positive and C111 is charged by R131 until Q103 conducts. The charge time for C111 is two times the period for a single character. While Q103 is cut off, C109 is charging through R132. When the voltage on C109 reaches approximately +2v the conduction level of emitter follower Q104 enables power NAND gate U31-A. Read data from U22-A is presented to the interface line when U31-A is enabled by the outputs of U22-B, and the MOTION signal being high. The charge time for C109 is about four character times. If no positive peaks exceed the threshold for two consecutive character periods C111 will charge to +0.7v and cause Q103 to conduct. C109 will discharge, until Q104 conducts, and disables U31-A. Since C109 requires four character periods to enable U31-A, there must have been four continuous peaks of the differentiated signal before U31-A was enabled.

5.2.2 TAPE CONTROL B1 PCBA

The following is a description of the Tape Control B1 PCBA (refer to Schematic No. 101291 and Assembly No. 101292).

The Tape Control PCBA is approximately 16.5 inches long with an edge connector at one end (J101). This is the interface connector and it is slotted to mate with a key in the mating plug. Figure 5-4 illustrates the location of each connector and test point. An additional connector (J14) is at the same end of the board and transmits power and control levels to the Data PCBA. The power, motors, controls, tension arm sensors, photo-tab sensors, and interlocks are all connected to the Tape Control PCBA through a row of connectors at the opposite end of the board (J1 through J13).

5.2.2.1 Circuit Description

A description of the logic sequences used in the tape control is detailed in Paragraph 4.3.5.

J1, J4, and J6 are used to connect the REWIND, LOAD, and ON LINE controls. Both normally open and closed contacts are used and the switch "bounce" is removed by the "clean-up" flip-flops.

The lamp drivers of circuits 100, 200, and 300 supply the lamp current in response to a low input. Depressing the LOAD control turns on relay driver Q3.

J8 is used to connect the tension arm interlock switch and the Write Lockout switch and solenoid, when required for writing, to the associated circuits on the Tape Control PCBA.

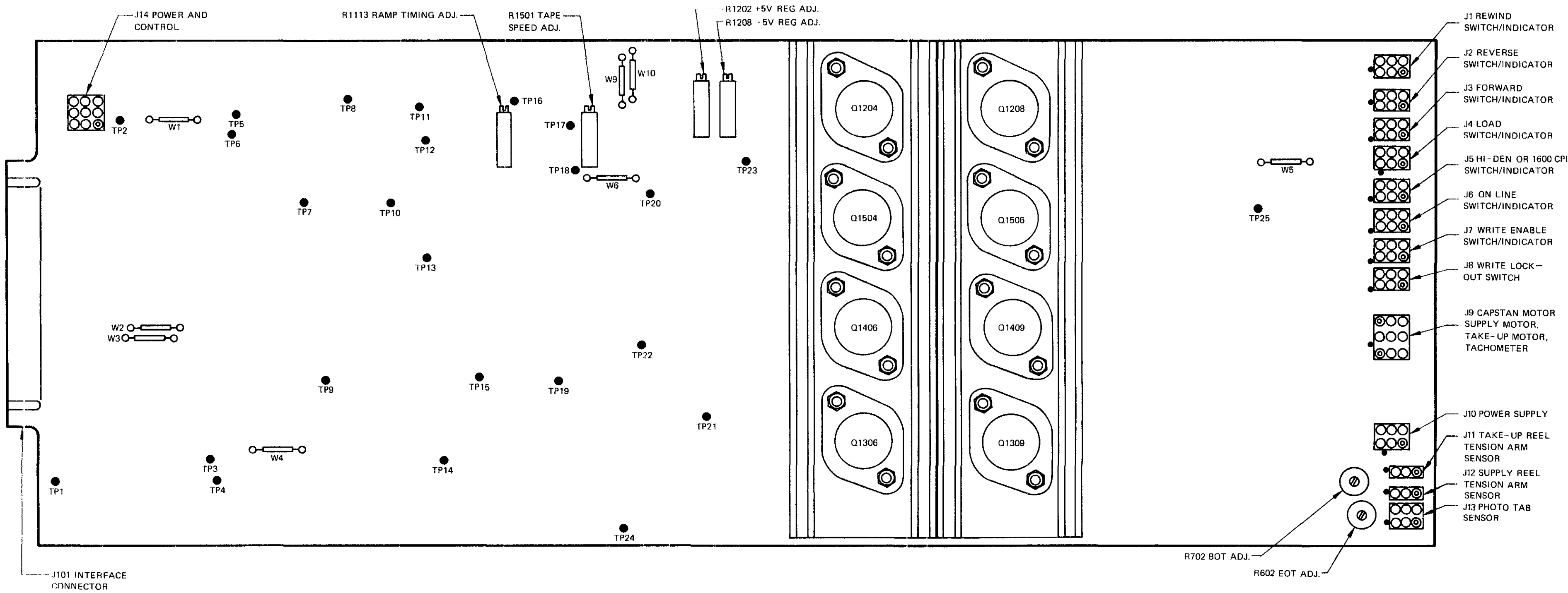


Figure 5-4. Tape Control B1 PCBA, Connector and Test Point Locations

When the interlock switch is closed, relay driver Q3 is held conducting, closing the normally open relay contacts. The relay voltage is derived from an auxiliary supply which decays very rapidly upon loss of line voltage. This ensures that the relay drops out, removing motor power and write current before the main power supplies have had time to decay to the point where inadvertent writing or tape motion could occur.

Diodes CR3, CR4, CR5, and CR6 eliminate relay arcing when the contacts are opened. The WLO solenoid driver (Q2) is turned on by the appearance of the WRT POWER level and causes the WLO solenoid to retract the Write Enable ring probe.

One of two different EOT/BOT amplifier systems may be employed in the transport. Some versions utilize circuits 600 and 700 as the EOT and BOT amplifiers. In these models, adjustment resistors R602 and R702 are utilized to adjust for the effects of the variable gain of the photo-transistors in the photo-tab sensor.

Some versions utilize an additional EOT/BOT amplifier circuit which is mounted on a bracket at the rear of the tape deck. Refer to Paragraph 5.2.3 for details concerning this amplifier.

The BOT signal is connected to a "Schmitt trigger" (circuit 800) to remove the possibility of multiple pulses at the leading and trailing edges of the BOT tab. The Schmitt trigger uses one-half of a dual operational amplifier IC connected in the positive feedback mode and is set to switch at approximately +1.5v. The output of the BOT and EOT amplifiers drop from +3v to approximately 0v upon detection of the photo-tab. The output of the Schmitt trigger is inverted and connected to a single-shot (circuit 900) which produces a 0.5-second pulse triggered by the leading edge of the tab. The single-shot pulse width is determined by C901, R903, and R904. The single-shot pulse (NBOTD) is inverted and the trailing edge triggers a narrow pulse (BOTDP), whose width is determined by C6, R27, and R28.

J10 connects the unregulated +13v and -13v (±21v for 25 ips transports) and the auxiliary 22v ac for the relay to the Tape Control board. The unregulated supplies are used by servo amplifiers (circuits 1300, 1400, and 1500) and the +5v and -5v regulators (circuit 1200).

The regulators supply +5v and -5v to the digital ICs, photo-tab sensors, tension arm sensors, etc., and consist of two essentially identical circuits whose outputs are set by potentiometers R1202 and R1208. The +5v and -5v references are zener diodes CR1201 and CR1205. The output transistors (Q1204 and Q1208) of each regulator are located on the heatsink. A "crowbar" overvoltage protection circuit is provided and uses zener diode CR1203 to detect an increase in the +5v level to +6v, in which case the SCR (CR1204) is fired, which blows the 5-amp fuse on the external power supply module and removes the positive unregulated voltage.

J9 connects the three motor assemblies to the servo amplifiers and the relay contacts on the Tape Control board. The capstan drive assembly has an additional pair of leads which are connected to a tachometer, integral with the motor. When the relay is de-energized, the contacts short the motor leads, which provides dynamic braking to prevent tape spillage. When the relay is energized, one side of each motor is connected to 0v and the other to its servo amplifier.

The capstan servo amplifier (circuit 1500) uses one-half of a dual operational amplifier as an input stage and discrete transistors to drive the high currents in the motor. Output transistors Q1504 and Q1506 are mounted on the heatsinks. The overall gain of the tachometer input is determined by R1511 divided by the sum of R1504 and R1505. Pin 5 of the IC is the virtual ground point into which the currents from the forward/reverse ramp generator and the rewind ramp generator (circuit 1100), the tachometer, and the amplifier output are summed. Tape speed is adjusted for both directions by means of R1501.

J11 and J12 connect the take-up and supply tension arm sensors to the reel servo amplifiers on the Tape Control board. The signals from the tension arm sensors are amplified by circuits 1300 and 1400, the supply reel servo amplifier, and the take-up reel servo amplifier. The low-frequency gain of the supply reel amplifier is defined by the ratio of (R1312 plus R1313) to R1303. The high-frequency gain is increased by means of C1302, C1303, and R1314. Output transistors Q1306, Q1309, Q1406, and Q1409 are located on the heatsink. Resistor R1301 is a supplementary input driven from the rewind ramp generator which removes the need for the tension arm to move through a large angle during rewind. Resistor R1402 performs the same task for the take-up servo.

J3 and J2 connect the FORWARD and REVERSE switches and indicators to the ramp generator inputs on the Tape Control board. These are alternate action switches. The transport must be Off-line for these switches to affect operation.

J14 is the outlet for connections between the Tape Control and Data boards. The power supplies +12v and -12v (or ±18v for 25 ips transports), +5v and -5v, and 0v, as well as the MOTION, NWRT, WRT POWER, and NHID (NHID not used in this transport) signals associated with the writing and reading of data, are picked off from this connector.

J101 is the interface connector for tape motion and status signals. ISFC, ISRC, and IRWC commands are received and gated with the Select, Ready, and On-line status. They then pass on to the ramp generator (circuit 1100), where the digital signals are converted to analog levels with controlled transition times which are the inputs to the capstan servo. The SFC and SRC are dealt with by a dual-operational amplifier circuit whose output levels are determined by the +5v and -5v, and the ratios of R1103, R1105 to R1111, and whose rise and fall times are determined by the +5v and -5v, R1113, R1114, and C1104. The transition times are varied by means of R1113. The RWC is dealt with by the circuit which includes Q1103 and Q1104. The rewind speed is determined by the -5v line to which Q1104 saturates when a rewind is in process, and resistor R1502 on the capstan servo amplifier. The rise and fall time of the rewind speed is determined by R1118, R1119, and C1108.

Jumper W1 is not applicable in this transport system.

Jumpers W2 and W3 are used to effect the several Select functions which are described in Paragraph 4.3.5.5.

Jumper W4 provides for the capability of the option where the transport can only be placed On-line when at Load Point (W4 inserted), or at any place in the tape reel (W4 omitted).

The Overwrite circuit is basically a R-C ramp utilizing a Darlington-pair transistor circuit. Write power is applied to pin B of the Overwrite circuit (1600) from pin 1 of J8.

NOTE

A Write Enable ring must be installed on the supply reel to complete the Write Power Interlock circuit.

When a Write or Overwrite operation is initiated, voltage at pin A of circuit 1600 drops sharply to 0v and the +5v charge on capacitor C1601 discharges toward 0v. (The RC time of discharge is determined by the values of C1601, R1601.) Transistor Q1601 conducts and causes transistor

Q1602 to conduct. The rate of conduction is determined by the discharge time of C1601. The voltage at the collector of Q1602 rises toward +5v as determined by the current flow through R1604 and Q1602. The output voltage is supplied via J14 pin 4 to the emitter circuits of the write amplifiers on the Data PCBA.

Termination of a Write or Overwrite operation causes the voltage at pin A of circuit 1600 to rise sharply to +5v. Conduction of transistors Q1601 and Q1602 decrease toward cutoff at a rate determined by (R36 + R1601), C1601. The output voltage at pin C ramps toward 0v in approximately 10 milliseconds, thus the write current decreases to 0 as the tape decelerates to rest.

5.2.3 EOT/BOT AMPLIFIER PCBA

The following is a description of the EOT/BOT Amplifier PCBA which is incorporated in some versions of the transport. Refer to Schematic 101948 and Assembly 101949.

5.2.3.1 Circuit Description

J1 connects the photo-tab sensor, mounted on the tape deck, to the EOT/BOT Amplifier PCBA which is mounted on the write lockout bracket.

The amplifier is designed to operate on the differential output from the EOT and BOT sensors (both tabs are never allowed to be under the sensors simultaneously). This system is basically insensitive to changes in ambient conditions.

In operation, when neither the BOT tab nor the EOT tab is under the photosensor, the outputs of the BOT and EOT sensors are high (approximately +4v) and are adjusted to be equal by the use of variable resistors R9 and R3. The bases of Q2 and Q5 are therefore at approximately +4v so that diodes CR1, CR3, and CR2, CR4 are forward biased by current flowing via R6 to ground. Thus, the base of Q3 is 1.2v below that of Q2, and the base of Q4 is 1.2v below that of Q5. Hence, Q2 and Q1, and Q5 and Q6 are cut off and the NBOT and NEOT outputs are high (pulled up by resistors on the Tape Control PCBA).

The characteristics of the photosensors are such that the "no tab" voltages, once set to be equal, track adequately with changes in ambient conditions to ensure that the NBOT and NEOT outputs remain high.

When the BOT tab moves under the sensor, its output drops toward 0v. Thus, the base of Q5 goes negative while that of Q4 remains referenced to the still high output of the EOT sensor. When the difference of voltage between the bases of Q5 and Q4 exceeds 1.2v current flows in Q5, turning Q6 on. The NBOT output therefore goes low as required. Similarly, when the EOT tab moves under the sensor, the NEOT output goes low.

The output of the EOT/BOT Amplifier PCBA is connected to J13 on the Tape Control PCBA.

SECTION VI
MAINTENANCE AND TROUBLESHOOTING

6.1 INTRODUCTION

This section provides information necessary to perform electrical and mechanical adjustments, parts replacement, and troubleshooting. Sections IV and V contain the theory of operation of components and circuits for reference.

6.2 FUSE REPLACEMENT

The following fuses are located under the control plate (refer to Paragraph 2.6, Step (2), for removal of this plate).

Line Fuse:	1.5 amp, 3AG, slow blow
+13v Fuse: *	5 amp, 3AG, fast blow

6.3 SCHEDULED MAINTENANCE

The tape transport is designed to operate with a minimum of maintenance and adjustments. Replacement of parts is designed to be as simple as possible. Repair equipment is kept to a minimum and only common tools are required in most cases. A list of tools required to maintain the tape transport is given in Paragraph 6.7.

To assure that the transport operates at its optimum design potential and to assure high MTBF, a program of scheduled preventive maintenance is recommended. This schedule is given in Table 6-1.

6.3.1 CLEANING THE TRANSPORT

The transport requires cleaning in five major areas: head and associated guides, capstan, roller guides, tape cleaner, and take-up hub.

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*21v fuse on 25 ips models

Table 6-1

Preventive Maintenance Schedule

Maintenance Operation	Frequency (Hours)	Quantity to Maintain	Time Required (Minutes)	Manual Paragraph Reference
Clean Head, Guides, Roller Guides, and Capstan	16 (or start of operating day)	—	5	6.3.1
Clean Tape Cleaner	80	1	5	6.6.14
Clean Take-up Hub	500	1	3	6.3.1
Check Skew, Tape Tracking, and Speed	1,000	—	15	6.6.3, 6.6.9, 6.5.7
Check Head Wear	5,000	1	3	6.6.4
Replace Reel Motors and Capstan Motor	10,000	3	30	6.6.8, 6.6.7

To clean the head and guides, use a lint-free cloth or cotton swab moistened in 91 percent isopropyl alcohol. Wipe the head carefully to remove all accumulated oxide and dirt.

CAUTION

ROUGH OR ABRASIVE CLOTHS SHOULD NOT BE USED TO CLEAN THE HEAD AND HEAD GUIDES. USE ONLY 91 PERCENT ISOPROPYL ALCOHOL. OTHER SOLVENTS, SUCH AS CARBON TETRACHLORIDE, MAY RESULT IN DAMAGE TO HEAD LAMINATION ADHESIVE.

To clean the capstan, use only a cotton swab moistened with 91 percen isopropyl alcohol to remove accumulated oxide and dirt.

To clean the roller guides, use a lint-free cloth or cotton swab moistened in 91 percent isopropyl alcohol. Wipe the guide surfaces carefully to remove all accumulated oxide and dirt.

CAUTION

DO NOT SOAK THE GUIDES WITH EXCESSIVE SOLVENT. EXCESSIVE SOLVENT MAY SEEP INTO THE PRECISION GUIDE BEARINGS, CAUSING CONTAMINATION AND A BREAKDOWN OF THE BEARING LUBRICANT.

The tape cleaner must be removed from the transport for proper cleaning. Paragraph 6.6.14 details the procedure for removal, cleaning, and reinstallation of the tape cleaner.

The take-up hub tape retention strip is cleaned by using a cotton swab moistened with 91 percent isopropyl alcohol.

CAUTION

USE OF EXCESSIVE SOLVENT WHEN CLEANING THE TAPE RETENTION STRIP MAY CAUSE THE VINYL TO DETERIORATE.

6.4 PART REPLACEMENT ADJUSTMENTS

Table 6-2 indicates the adjustments necessary when a part is replaced. The details of the adjustments are given in Paragraphs 6.5 through 6.6.

6.5 ELECTRICAL ADJUSTMENTS

Paragraphs 6.5.2 through 6.5.9 describe the test configurations, test procedures, adjustment procedures, and related adjustments for the +5v and -5v Regulators, BOT and EOT Amplifiers, Ramp Timing, Tape Speed, and Read Amplifier Gain.

The following equipment (or equivalent) is required.

(1) Oscilloscope, Tektronix 561 (vertical and horizontal sensitivity specified to ±3 percent accuracy).

(2) Digital Volt Meter, Fairchild 7050 (±0.1 percent specified accuracy).

(3) Counter Timer, Monsanto Model 100B (±0.1 percent specified accuracy).

(4) Master Skew Tape, IBM No. 432640.

(5) Optical Encoder, 500 Line, PERTEC No. 512-1100.

(6) Hand Held Exerciser, TE-T02, PERTEC No. 895360-01.

Table 6-2

Part Replacement Adjustments

Part Replaced	Auxiliary Adjustments	Time Required (Minutes)	Manual Paragraph Reference
Control Switch	None	2	—
Photo-tab Sensor	EOT/BOT Potentiometers on Tape Control PCBA or EOT/BOT Amplifier PCBA	10	6.6.5
Tension Arm Sensor	Tension Arm Shutter	10	6.6.2
Limit Switch Assembly	None	10	6.6.1
Capstan Drive Assembly	Tape Speed, Ramp on Tape Control PCBA	20	6.6.7
Reel Motors Assembly	Belt Tension	10	6.6.8
Power Supply Assembly	None	20	—
Tape Control PCBA	+5v and -5v Regulators, Tape Speed and Ramps, EOT/BOT	20	6.5.2 through 6.5.7.10
Data PCBA	Read Amplifier Gain	15	6.5.8
EOT/BOT Amplifier Assembly	EOT/BOT Sensor	10	6.6.5
Head	Skew Adjustment, Read Amplifier Gain	30	6.6.4 6.5.8
Write Lockout Assembly	None	10	—
Take-up Hub	None	5	—

6.5.1 ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure taking into consideration the assumed accuracy of the test equipment specified in Paragraph 6.5.

When the measured value of any parameter is within the specified acceptable limits NO ADJUSTMENTS should be made. Should the measured value fall outside the specified acceptable limits adjustments should be made in accordance with the relevant procedure.

CAUTION

SOME ADJUSTMENTS MAY REQUIRE CORRESPONDING ADJUSTMENTS IN OTHER PARAMETERS. ENSURE CORRESPONDING ADJUSTMENTS ARE MADE AS SPECIFIED IN THE INDIVIDUAL PROCEDURES. THE +5 AND -5 REGULATOR VOLTAGES MUST BE CHECKED PRIOR TO ATTEMPTING ANY ELECTRICAL ADJUSTMENT.

When adjustments are made, the value set should be the exact value specified (to the best of the operator's ability).

6.5.2 +5V AND -5V REGULATORS

The +5v and -5v regulators are located on the Tape Control PCBA. The regulators are adjusted by means of variable resistors R1202 (+5v) and R1208 (-5v). The numerical value of the voltage difference, disregarding polarity, between the +5v and -5v lines must be less than 0.07v.

6.5.2.1 Test Configuration

(1) Load a 7-inch reel of tape with a Write Lockout ring in place.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6.5.2.2 Test Procedure

(1) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the voltage between TP17 (+5v) and TP22 (0v) on the Tape Control PCBA.

(2) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the voltage between TP23 (-5v) and TP22 (0v) on the Tape Control PCBA.

(3) Acceptable Limits

(a) +5v Regulator

- +4.85v minimum
- +5.15v maximum

(b) -5v Regulator

- -4.85v minimum
- -5.15v maximum

(4) Compare the voltages obtained in Steps (1) and (2). Voltages must fall within the acceptable limits and the difference between the +5v and -5v lines must be less than 0.07v.

6.5.2.3 Adjustment Procedure

When the acceptable limits are exceeded or the voltage difference between the +5 and -5 voltages exceeds 0.07v, the following adjustments are performed.

(1) Adjust variable resistor R1202 on the Tape Control PCBA to +5v as observed at TP17.

(2) Adjust variable resistor R1208 on the Tape Control PCBA to -5v as observed at TP23.

6.5.2.4 Related Adjustments

The following areas must be checked and adjusted subsequent to adjusting the +5v and -5v regulators.

(1) BOT/EOT Amplifier (Paragraph 6.5.3).

(2) Ramp Timing (Paragraph 6.5.6).

(3) Tape Speed (Paragraph 6.5.7).

6.5.3 BOT/EOT AMPLIFIER SYSTEMS

There are presently two different EOT/BOT systems used in the Model T7640 transport. One EOT/BOT amplifier system is integrated in the Tape Control PCBA and is described in Paragraphs 6.5.4 and 6.5.5. The other EOT/BOT amplifier system is a 2 × 4 inch PCBA (Schematic 101948 and Assembly 101949) located at the rear of the tape deck and is shown in Figure 7-2. The following procedure is employed for testing and adjusting this EOT/BOT Amplifier PCBA system.

NOTE

The +5v and -5v regulator voltages must be checked and adjusted prior to adjusting the EOT/BOT Amplifier system. Measurements and adjustments should be performed at room temperature.

6.5.3.1 Test Configuration (Assembly 101949)

(1) Load a 7-inch reel of tape with a Write Lockout ring in place.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6.5.3.2 Test Procedure (Assembly 101949)

(1) Advance tape until the reflective BOT tab is past the photosensor, i.e., photosensor is over a non-tab area.

(2) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the off-tab voltage between TP1 (EOT) on the EOT/BOT Amplifier PCBA and TP24 (0v) on the Tape Control PCBA.

(3) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the off-tab voltage between TP2 (BOT) on the EOT/BOT Amplifier PCBA and TP24 (0v) on the Tape Control PCBA.

(4) Acceptable Limits (Off-tab)

- +4.5v maximum
- +3.25v minimum

(5) Compare the voltages obtained in Steps (2) and (3). Voltages must fall between the acceptable limits and the difference between TP1 (EOT) and TP2 (BOT) voltages must be less than 0.50v.

(6) Manually position tape until the reflective BOT tab is located under the photosensor.

(7) Measure and note the on-tab differential voltage between TP1 and TP2. This voltage difference must be greater than 2.0v.

(8) Advance tape until the EOT tab is positioned under the photosensor.

(9) Measure and note the on-tab differential voltage between TP1 and TP2. This voltage difference must be greater than 2.0v.

(10) Acceptable Limits (On-tab)

- On-tab voltage differential between TP1 and TP2 must be greater than 2.0v.

6.5.3.3 <u>Adjustment Procedure (Assembly 101949)</u>

When the acceptable limits are exceeded or the off-tab voltage difference compared in Paragraph 6.5.3.2, Step (5), is greater than 0.50v, the following adjustments are performed.

(1) Verify that the adjusting screws of variable resistors R602 and R702 located on the Tape Control PCBA are turned fully clockwise.

(2) Position tape so that the EOT/BOT reflective tabs are clear of the photosensor area.

(3) Adjust variable resistor R3 on the EOT/BOT Amplifier PCBA to +4.0v as observed at TP1.

(4) Adjust variable resistor R9 on the EOT/BOT Amplifier PCBA to +4.0v as observed at TP2.

(5) Interaction between R3 and R9 may cause a voltage differential to exist between TP1 and TP2. Verify that the voltage at TP1 is +4.0v. Repeat Steps (3) and (4) as required.

(6) Position the tape so that the EOT reflective tab is located under the photosensor.

(7) Measure the on-tab differential voltage between TP1 and TP2. This voltage must be greater than 2.0v; if not sensor and/or amplifier should be replaced.

(8) Depress and release the REWIND control. Tape will rewind to the BOT, enter a Load sequence, and stop.

(9) Measure the on-tab differential voltage between TP1 and TP2. This voltage must be greater than 2.0v. If the measured differential voltage is less than 2.0v, the sensor and/or amplifier should be replaced.

6.5.3.4 <u>Related Adjustments (Assembly 101949)</u>

- None

6.5.4 BOT AMPLIFIER

For transports not equipped with an EOT/BOT Amplifier PCBA circuit 700 located on the Tape Control PCBA is utilized as the BOT amplifier. The following test and adjustment procedure is employed.

NOTE

The +5v and -5v regulator voltages must be checked and adjusted prior to adjusting the BOT amplifier system. Measurements and adjustments should be performed at room temperature.

6.5.4.1 Test Configuration

(1) Load a 7-inch reel of tape with a Write Lockout ring in place.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6.5.4.2 Test Procedure

(1) Manually position tape so that the BOT reflective tab is clear of the photosensor area.

(2) Using a Fairchild DVM Model 7050 (or equivalent) measure and note the off-tab voltage between TP19 and TP24 (0v) on the Tape Control PCBA.

(3) Manually position tape so that the BOT reflective tab is positioned under the photosensor.

(4) Using a Fairchild 7050 (or equivalent) measure and note the on-tab voltage between TP19 and TP24 (0v) on the Tape Control PCBA.

(5) Acceptable Limits

(a) On-tab

- +0.3v maximum

(b) Off-tab

- +2.8v minimum

6.5.4.3 Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are performed.

(1) Manually position tape so that the BOT reflective tab is clear of the photosensor area.

(2) Adjust variable resistor R702 to a minimum of +2.8v as observed at TP19.

(3) Position tape so that the BOT reflective tab is positioned under the photosensor.

(4) Readjust variable resistor R702, if necessary, to obtain an on-tab voltage of less than +0.2v.

(5) Position tape so that the BOT reflective tab is clear of the photosensor area and check TP19 to ensure that the voltage is +2.8v (minimum).

(6) Repeat Steps (2) through (5) if necessary.

6.5.4.4 Related Adjustments

- None

6.5.5 EOT AMPLIFIER

For transports not equipped with an EOT/BOT Amplifier PCBA, circuit 600 located on the Tape Control PCBA is utilized as the EOT amplifier. The following test and adjustment procedure is employed.

NOTE

The +5v and -5v regulator voltages must be checked and adjusted prior to adjusting the EOT amplifier system. Measurements and adjustments should be performed at room temperature.

6.5.5.1 Test Configuration

(1) Load a 7-inch reel of tape with a Write Lockout ring in place.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6.5.5.2 Test Procedure

(1) Manually position the tape so that the EOT reflective tab is clear of the photosensor area.

(2) Using a Fairchild 7050 (or equivalent) measure and note the off-tab voltage between TP11 and TP24 (0v) on the Tape Control PCBA.

(3) Manually position the tape so that the EOT reflective tab is positioned under the photosensor.

(4) Using a Fairchild 7050 (or equivalent) measure and note the on-tab voltage between TP11 and TP24 (0v) on the Tape Control PCBA.

(5) Acceptable Limits

(a) On-tab

- +0.3v maximum

(b) Off-tab

- +2.8v minimum

6.5.5.3 Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are performed.

(1) Manually position tape so that the EOT reflective tab is clear of the photosensor area.

(2) Adjust variable resistor R602 to a minimum of +2.8v as observed at TP11.

(3) Position tape so that the EOT reflective tab is positioned under the photosensor.

(4) Readjust variable resistor R602, if necessary, to obtain an on-tab voltage of less than +0.2v.

(5) Position tape so that the EOT reflective tab is clear of the photosensor area and check TP11 to ensure that the voltage is +2.8v (minimum).

(6) Repeat Steps (2) through (5) if necessary.

6.5.5.4 Related Adjustments

- None

6.5.6 RAMP TIMING

The four tape acceleration and deceleration ramps (Forward and Reverse, Start and Stop) are controlled by a single potentiometer adjustment located on the Tape Control PCBA.

This adjustment controls the Start/Stop time and its value is dependent upon the tape speed. Start/Stop times should be calculated from the following formula which will result in a constant Start and Stop distance of 0.19 inch when the tape speed is correct.

$$\text{Start/Stop Time (milliseconds)} = \frac{375}{\text{Speed (ips)}}$$

Example: 30 millisecond Start/Stop time at 12.5 ips

The ramp adjustment time is chosen to ensure that the correct Start/Stop distance is correlated to the specified Start/Stop time.

NOTE

> The +5 v and -5 v regulator voltages must be checked and adjusted prior to adjusting the Ramp Timing. Measurements and adjustments should be performed at room temperature.

6.5.6.1 Test Configuration

(1) Load a 7-inch reel of tape with a Write Lockout ring in place.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6.5.6.2 Test Procedure

(1) Connect a signal probe of a Tektronix Model 561 (or equivalent) oscilloscope to TP18 on the Tape Control PCBA.

(2) Connect the oscilloscope reference probe to TP24 (0v) on the Tape Control PCBA.

(3) Apply a 5Hz symmetrical square wave with a 3v amplitude (+3.0v to 0v) to the interface line ISFC (J101 pin C or TP8).

(4) Synchronize the oscilloscope on the negative-going edge of the square wave input.

(5) Adjust the oscilloscope Variable Vertical (volt/div) control to display 0 to 100 percent of the ramp waveform over four large divisions on the oscilloscope graticule.

(6) Observe that the ramp adjustment time intersects 90 percent of the ramp amplitude (18 small divisions of oscilloscope graticule). Figure 6-1 illustrates ramp levels and timing.

NOTE

For reverse operation the ramp is a negative-going waveform.

(7) Acceptable limits (90 percent of actual speed).

(a) 25.0 ips transports
- 12.2 – 13.4 milliseconds

(b) 18.75 ips transports
- 16.3 – 17.9 milliseconds

(c) 12.5 ips transports
- 23.9 – 26.5 milliseconds

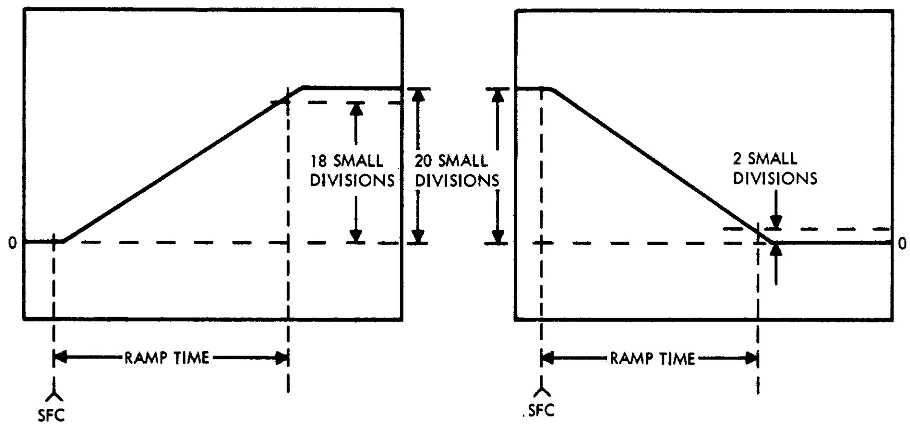


Figure 6-1. Ramp Levels and Timing

(8) Remove the square wave input from J101 pin C (ISFC) and apply the square wave input to ISRC line (J101 pin E or TP5).

(9) With the oscilloscope connected as specified in Step (5), observe that the reverse ramp timing is within the limits specified in Step (7).

6.5.6.3 Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.5.6.1.

(2) Perform the test procedure described in Paragraph 6.5.6.2, Steps (1) through (5).

(3) Adjust variable resistor R1113 on the Tape Control PCBA to obtain ramp adjustment times as follows.

(a) 25.0 ips transports

- 12.8 milliseconds

(b) 18.75 ips transports

- 17.1 milliseconds

(c) 12.5 ips transports

- 25.2 milliseconds

NOTE

Specified time results in oscilloscope display illustrated in Figure 6-1. The ramp adjustment time intersects 90 percent of ramp amplitude when accelerating and 10 percent of ramp amplitude when decelerating.

(4) Remove the square wave input from ISFC line (J101 pin C) and apply the square wave input to the interface line ISRC (J101 pin E or TP5).

(5) Observe oscilloscope display of reverse ramp and readjust R1113 to obtain ramp time as specified in Step (3).

6.5.6.4 Related Adjustments

- None

6.5.7 TAPE SPEED

In the Synchronous mode, only the forward speed is adjustable. The Synchronous Reverse function utilizes the same voltage reference as Synchronous Forward and is not independently adjustable.

NOTE

> The +5 v and -5 v regulator voltages must be checked and adjusted prior to adjusting the Tape Speed. Measurements and adjustments should be performed at room temperature.

Two methods of tape speed checks and adjustments are given. Paragraphs 6.5.7.1 through 6.5.7.5 describe the method utilizing an optical encoder; Paragraphs 6.5.7.6 through 6.5.7.10 describe the strobe disk method.

6.5.7.1 Tape Speed (Optical Encoder Adjustment Method)

Table 6-3 lists the nominal counter frequency readings to which the tape speed is adjusted for 7000 Series tape transports.

Table 6-3
Counter Frequency Readings

Tape Speed (ips)	Counter Frequency
25.0	4008
18.75	3006
12.50	3317

621D

Tape speed may be calculated from the following formula used in conjunction with the specified counter timer.

$$V \text{ ips} = \text{Counter Frequency (Hz)} \times \frac{C}{500 \text{ inches}}$$

where

C = Capstan Circumference

Table 6-4 lists the capstan circumference for various tape speeds.

Table 6-4

Capstan Circumference

Tape Speed (ips)	Capstan Circumference (inches)
25.0	3.118
18.75	3.118
12.50	1.884

6.5.7.2 Test Configuration (Optical Encoder Method)

(1) Couple an Optical Encoder PERTEC Part No. 512-1100 to the rear of the capstan shaft utilizing a coupling device PERTEC Part No. 100124-01. A voltage of 5v dc must be applied to the Optical Encoder lamp inputs (pins 1 and 2). This voltage can be obtained between TP17 (+5v) and TP22 (0v) on the Tape Control PCBA.

(2) Load a 7-inch reel of tape with a Write Lockout ring in place.

(3) Apply power to the transport.

(4) Depress and release the LOAD control to establish interlocks and tension the tape.

(5) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6.5.7.3 Test Procedure (Optical Encoder Method)

(1) Connect input probes of Counter Timer Monsanto Model 100B (or equivalent) to pins 6 and 7 (or pins 8 and 9) of the Optical Encoder PERTEC Part No. 512-1100.

(2) Connect the interface line ISFC (J101 pin C or TP8) to ground. Tape will move in the forward direction.

(3) Adjust the sample interval of the counter timer to monitor the encoder output over a 1-second interval.

(4) Acceptable limits

(a) 25.0 ips transports
- 4049 maximum
- 3965 minimum

(b) 18.75 ips transports
- 3036 maximum
- 2975 minimum

(c) 12.5 ips transports
- 3358 maximum
- 3384 minimum

(5) Remove the ground from J101 pin C (ISFC) and apply a ground to the interface line ISRC (J101 pin E or TP5). Tape will move in the reverse direction.

(6) With the counter timer connected as specified in Step (1), monitor the output of the optical encoder.

(7) The reverse tape speed, as monitored with the counter timer, must be within the following limits.

(a) 25.0 ips transports
- 4125 maximum
- 3885 minimum

(b) 18.75 ips transports
- 3095 maximum
- 2915 minimum

(c) 12.5 ips transports
- 3424 maximum
- 3226 minimum

6.5.7.4 Adjustment Procedure (Optical Encoder Method)

When the forward or reverse tape speeds exceed the specified limits the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.5.7.2.

(2) Perform the test procedure described in Paragraph 6.5.7.3, Steps (1) through (3).

(3) Adjust the variable resistor R1501 on the Tape Control PCBA for the following counter timer value.

(a) 25.0 ips transports
- 4008

(b) 18.75 ips transports
- 3006

(c) 12.5 ips transports
- 3317

(4) Remove the ground from J101 pin C (ISFC) and apply a ground to the interface line ISRC (J101 pin E or TP5).

(5) Monitor the counter timer to ensure that the reverse speed is within the acceptable limits established in Paragraph 6.5.7.3, Step (7). Repeat Steps (2) through (5) as required.

6.5.7.5 Related Adjustments (Optical Encoder Method)

- None

6.5.7.6 Tape Speed (Strobe Disk Adjustment Method)

Tape speed adjustments made using this method are accomplished by illuminating the capstan hub and strobe disk with a fluorescent light source, then adjusting the capstan servo until the disk image appears stationary. Table 6-5 lists the strobe disks for the various tape speeds.

It is important to note that if the tape speed is substantially different from the nominal, the strobe disk may give an erroneous reading.

Table 6-5

Strobe Disks

PERTEC Part No.	Tape Speed (ips)	Light Source Frequency (Hz)
101744-08	25.00	60/50
101744-09	18.75	60
101744-10	6.25/12.50	60/50

Some strobe disks have two concentric sets of strobe marks. The following rules apply to strobe disks marked with multiple sets of strobe markings.

(1) Part No. 101744-08 (25 ips). The outer set of strobe markings are utilized when the input power frequency for the transport and the fluorescent light source are 60 Hz. The inner strobe disk is utilized when the transport power and fluorescent light frequency is 50 Hz.

(2) Part No. 101744-10 (6.25/12.5 ips). The outer set of strobe markings are utilized when the fluorescent light frequency and the transport input power frequency are 60 Hz. The inner strobe disk is utilized for 50 Hz.

6.5.7.7 Test Configuration (Strobe Disk Method)

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6.5.7.8 Test Procedure (Strobe Disk Method)

(1) Establish the test configuration described in Paragraph 6.5.7.7.

(2) Connect the ISFC interface line, J101 pin C, of the Tape Control PCBA to ground. Tape will move in the forward direction.

(3) Observe the appropriate strobe disk image. The image should appear stationary.

6.5.7.9 Adjustment Procedure (Strobe Disk Method)

If the strobe disk image observed in Paragraph 6.5.7.8, Step (3), does not appear stationary perform the following adjustment.

- Adjust variable resistor R1501 located on the Tape Control PCBA until the appropriate disk image appears stationary.

6.5.7.10 Related Adjustments (Strobe Disk Method)

- None

6.5.8 READ AMPLIFIER GAIN

The gain of each of the read amplifiers located on the Data PCBA is independently adjustable.

NOTE

- The Tape Speed must be checked and adjusted prior to adjusting the Read Amplifier Gain.

Read amplifier gain may be determined by reading (in the Read Only mode) an all-ones tape which was recorded on the transport. Paragraph 6.5.8.4 details a method for generating an all-ones tape. A quality tape, such as 3M 777 should be utilized for this purpose.

6.5.8.1 Test Configuration

(1) Clean the head assembly and tape path as described in Paragraph 6.3.1.

(2) Load a pre-recorded tape (see Paragraph 6.5.8.4).

(3) Apply power to the transport.

(4) Depress and release the LOAD control to establish interlocks and tension the tape.

(5) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6.5.8.2 Test Procedure

(1) Connect the interface line ISFC (J101 pin C or TP8) to ground. Tape will move forward at the specified velocity.

(2) Using the signal probe of a Tektronix 561 oscilloscope (or equivalent), measure and record the peak-to-peak amplitude of the read amplifier waveforms viewed at TP104 through TP904 on the Data PCBA.

NOTE

Oscilloscope vertical sensitivity should be set to display 2 volts per division.

(3) Acceptable limits (peak-to-peak when utilizing an all-ones tape generated on the transport).

- 6.5v maximum
- 4.9v minimum

6.5.8.3 Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.5.8.1.

(2) Connect the interface line ISFC (J101 pin C or TP8) to ground.

(3) Using the signal probe of a Tektronix 561 oscilloscope (or equivalent) observe TP104 through TP904 on the Data PCBA. Adjust variable resistors R117 through R917 associated with test points to 6.0v peak-to-peak.

6.5.8.4 Generation of All-Ones Tape

In considering the overall gain of the read system it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape, i.e., new or used.

The read amplifier output should be adjusted as detailed in Paragraph 6.5.8.3, Step (3). A read amplifier whose gain is adjusted too high will result in amplifier saturation; gain which is set too low will increase the susceptibility to data errors due to dropouts.

An all-ones tape may be generated as follows.

(1) Ensure that head assembly and tape path are clean.

(2) Load a good quality work tape with a Write Enable ring in place on the transport.

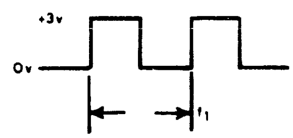
(3) Bring the transport to Load Point as described in Paragraph 6.5.3.1.

(4) Apply a ground to the interface line ISWS (J101 pin K).

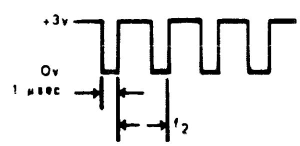
(5) Apply a ground to the interface line ISLT (J101 pin J).

(6) Apply a ground to the interface line ISFC (J101 pin C).

(7) Apply a square wave to interface lines WDP - WD7 (J102 pins L, M, N, P, R, S, T, U, and V).



(8) Apply negative-going pulses (+3v to 0v) of 1-μsec duration to the interface line IWDS (J102 pin A).



(9) Maintain the transport in this record mode for approximately 5 minutes.

(10) Remove the signal source from the interface line IWDS (J102 pin A).

(11) Remove the ground from the interface lines ISWS, ISFC, and ISLT (J101 pins K, C, and J, respectively).

(12) Remove the signal connected to the interface in Step (7).

(13) Depress and release the REWIND control; tape will rewind to the Load Point and stop.

6.5.8.5 Related Adjustments

- None.

6.5.9 THRESHOLD GENERATOR

The output voltage of the threshold generator can be checked at TP5 on the Data PCBA in the different modes of operation. The following values are included as a check only; no adjustment procedure is applicable. If the limits listed are exceeded, this is indicative of a fault in the threshold circuitry.

(1) Write Mode
- +4.30v maximum
- +3.90v minimum

(2) Read Mode

(a) IRTH2 False
- +1.40v maximum
- +1.00v minimum

(b) IRTH2 True
- +0.70v maximum
- +0.50v minimum

6.6 MECHANICAL ADJUSTMENTS

6.6.1 TENSION ARM LIMIT SWITCH

When the tension arm is resting against its backstop, the position of the limit switch roller with respect to the cam should be as shown in Figure 6-2. At this time the switch contacts should be open. If the relative positions of the roller and cam are not as illustrated, the following adjustment is performed.

(1) Loosen the cam retaining set-screw.

(2) Rotate the cam on its shaft until the limit switch roller is in the position illustrated in Figure 6-2.

(3) Firmly tighten the cam retaining set-screw.

CAUTION

THE CAM RETAINING SET-SCREW MUST BE TIGHTENED SUFFICIENTLY TO PREVENT ROTATION OF THE CAM WHEN THE TENSION ARM IMPACTS ON ITS BACKSTOP.

The limit switch plate is slotted at one mounting screw and may be rotated about the second screw to facilitate setting the switching point of the limit switch. The plate should be rotated to a position where the limit switch trips with its roller one-half of the distance up the slope from its rest position. The switch should be closed when the roller moves on the cam lobe between the semi-circular cutouts.

Replacement of the limit switch is accomplished as follows.

(1) Unplug the limit switch connector (P8) from J8 on the Tape Control PCBA.

(2) Remove the yellow and green leads from the limit switch connector (P8) using an extractor tool.

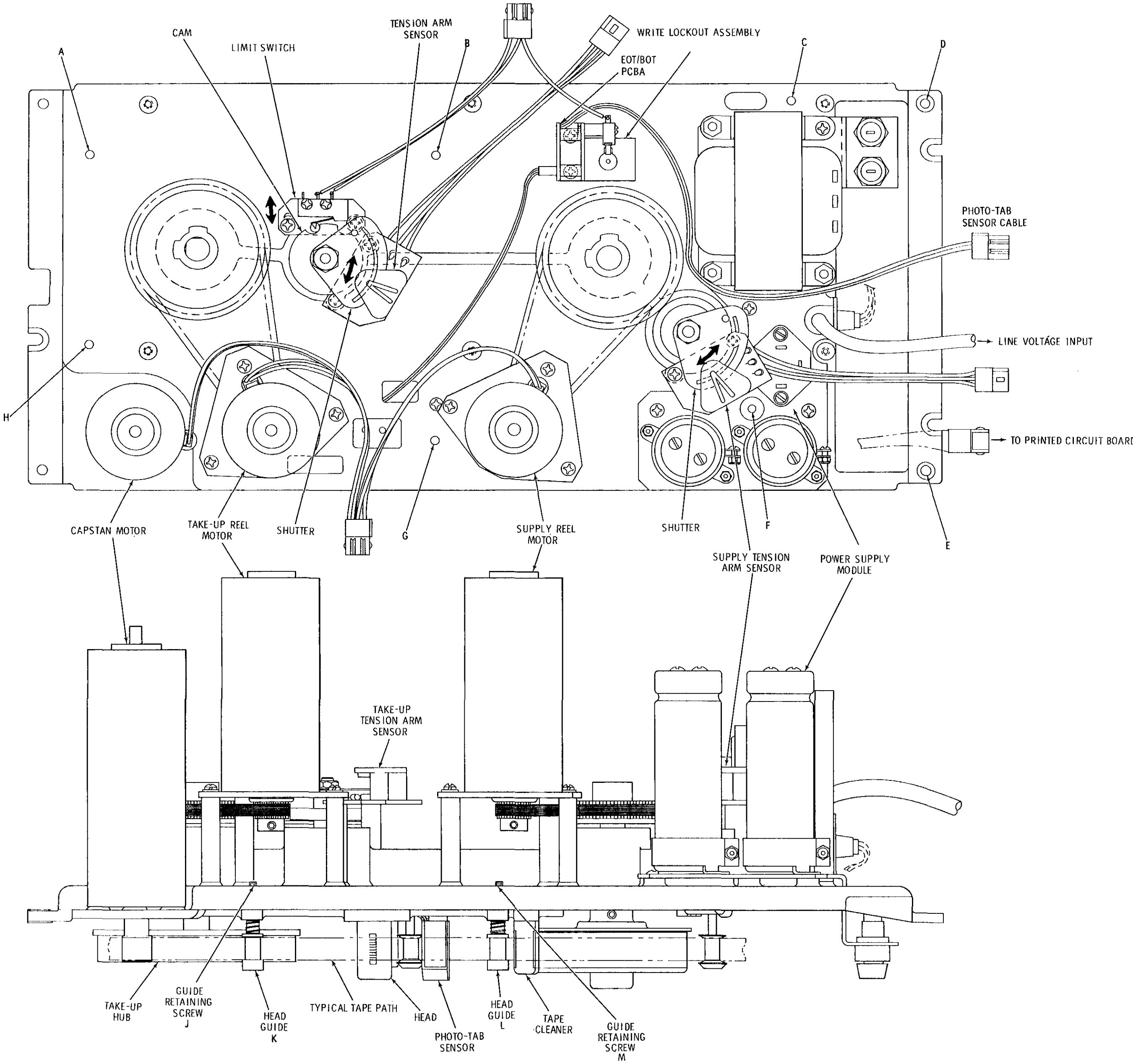


Figure 6-2. Tape Deck Diagram (Rear View)

(3) Remove the two mounting screws which mount the limit switch to its plate and remove the switch.

(4) Attach the new limit switch to the plate using the two mounting screws removed in Step (3).

(5) Adjust the limit switch position as described in the preceeding paragraph.

(6) Tighten the two mounting screws and recheck position of the limit switch roller.

(7) Connect the limit switch connector (P8) to J8 of the Tape Control PCBA.

6.6.2 TENSION ARM POSITION SENSOR

There are two tension arm position sensors: one on the take-up tension arm, and the second on the supply arm. Each of the sensors has a 3-pin plug which connects the output of the sensor to the reel servo amplifier on the Tape Control PCBA.

CAUTION

ENSURE THAT THE +5 AND -5 REGULATED VOLTAGES, RAMP TIMING, AND TAPE SPEED ARE CORRECT AS DETAILED IN PARAGRAPHS 6.5.2, 6.5.6, AND 6.5.7, RESPECTIVELY, BEFORE ADJUSTING THE TENSION ARM POSITION SENSORS.

6.6.2.1 Preliminary Adjustment

The tension arm photosensors on the supply reel and take-up reel are initially adjusted as follows.

(1) Remove tape from the transport.

(2) Establish an environment which ensures that the tension arm sensors are shielded from high ambient light. Failure

to do so will result in a shift in the arm operating region when the unit is rack mounted.

(3) Loosen the No. 10 retaining nut securing the optical shutter to the tension arm shaft.

NOTE

Loosen the nut in such a manner that the shutter can be rotated by hand, yet there is sufficient friction to prevent the setting from changing when the nut is tightened.

(4) Apply power to the transport.

(5) Rotate the shutter until moving the tension arm to the middle of its range stops reel motion.

NOTE

The LOAD control must be continuously depressed or the limit switch shorted to facilitate this procedure.

(6) Load a 7-inch reel of tape on the transport.

(7) Depress and release the LOAD control to establish interlocks and tension the tape.

(8) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6.6.2.2 Supply Arm Adjustment - Optical Shutter

When the preliminary adjustments described in Paragraph 6.6.2.1 are completed, proceed as follows.

(1) Apply ground to the interface line ISFC (J101 pin C or TP8). Tape will move forward at the specified velocity.

(2) When the supply reel is nearly empty remove the ground from the interface line ISFC.

(3) Alternately ground the interface line ISRC (J101 pin E or TP5) and the interface line ISFC (J101 pin C or TP8) so that the tape shuttles back and forth.

(4) Note the total arm movement.

(5) Re-adjust the shutter, if necessary, so that the arm displacement forward and reverse is approximately equidistant about the center of the arm cutout in the overlay.

(6) Torque the optical shutter retaining nut to 35 inch-pounds taking care that the shutter does not move.

6.6.2.3 Take-up Arm Adjustment - Optical Shutter

When the supply arm adjustments are completed, proceed as follows.

(1) Ensure that the limit switch cam (Paragraph 6.6.1) is centered (limit switch actuating roller rests in approximately the same position in the cutout with the tension arm at each stop).

(2) Apply ground to interface line ISRC (J101 pin E or TP5). Tape will move in the reverse direction at the specified velocity.

(3) When the take-up reel is nearly empty, remove the ground from the interface line ISRC (J101 pin E or TP5).

(4) Alternately ground the interface line ISFC (J101 pin C or TP8) and the interface line ISRC (J101 pin E or TP5) so that tape shuttles back and forth.

(5) Readjust the shutter, if necessary, so that the arm displacement forward and reverse is approximately equidistant about the center of the arm cutout in the overlay.

(6) Depress and release the REWIND control and observe that the limit switch roller remains on the top surface of the cam.

(7) Repeat Steps (1) through (6) as required.

(8) Torque the optical shutter retaining nut to 35 inch-pounds taking care that the shutter does not move.

6.6.2.4 Tension Arm Sensor Replacement

The tension arm optical sensors are replaced as follows.

(1) Loosen the No. 10 retaining nut which secures the optical shutter to the tension arm.

(2) Rotate the shutter to clear the countersunk screws which retain the tension arm sensor printed circuit board to the deck standoffs.

(3) Remove two retaining screws from the tension arm sensor printed circuit board.

NOTE

Retain the two screws removed in Step (3). They will be used to mount the replacement sensor.

(4) Unplug the connector (P11 for the take-up reel sensor, and P12 for the supply reel sensor) from the Tape Control PCBA and remove the sensor assembly.

(5) Mount the replacement assembly on the deck standoffs using the two screws which were removed in Step (3).

(6) Plug the connector (P11 for the take-up reel sensor, and P12 for supply reel sensor) into the respective jack on on the Tape Control PCBA.

(7) Perform the relevant adjustment procedure detailed in Paragraph 6.6.2.

6.6.3 SKEW MEASUREMENT AND ADJUSTMENT

Transport skew is adjusted by first checking and mechanically adjusting write head skew and then checking the read skew. The requirements on PE read skew are not as severe as those for NRZI since the PE system utilizes a multiple buffer register per channel for read data recovery.

6.6.3.1 Write Skew Measurement

An indication of the write head skew may be obtained by observing the algebraic sum of the peak detectors at TP10 on the Data PCBA with the write head connector plugged into the read head receptacle (J3) on the Data PCBA.

Figure 6-3 illustrates an example of correctly adjusted skew. This method of determining the system write head skew is accomplished as follows.

(1) Disconnect the write head and read head connectors from J2 and J3 respectively on the Data PCBA.

(2) Plug the write head connector into the read head connector (J3) on the Data PCBA.

(3) Set the vertical sensitivity on the oscilloscope to 1.0 volt/cm.

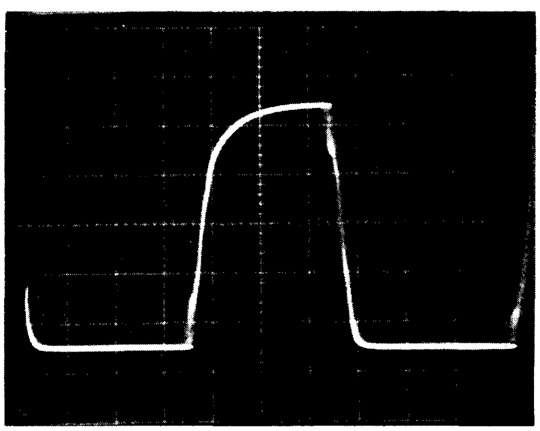


Figure 6-3. Skew Waveform (Typical)

(4) Set the oscilloscope to trigger on Channel 1 negative slope, alternate mode.

(5) Load an 800-cpi master tape on the transport, bring to BOT, and activate the FORWARD control.

(6) Observe oscilloscope waveform and adjust the horizontal time/division fixed and variable controls to display one complete cycle.

NOTE

With an 800 cpi tape, each half-cycle represents 1250 μinches. The scope graticule is divided into 10 major divisions, each of which is divided into 5 divisions; therefore

$$\frac{2500\ \mu\text{inch}}{50\ \text{divisions}} = 50\ \mu\text{inch/division}$$

(7) Observe that the fall time of the waveform viewed at TP10 is less than four small divisions of the oscilloscope graticule, i.e., 200 μinches. This measurement should be taken between the 95- and 5-percent points of the waveform.

(8) Disconnect the write head connector from the read head jack (J3). Connect the write and read head connections to J2 and J3, respectively, on the Data PCBA.

6.6.3.2 Write Skew Adjustment

To reduce skew to within acceptable limits the following procedure should be performed.

(1) Perform skew measurement procedure described in Paragraph 6.6.3.1, Steps (1) through (5).

(2) While observing the waveform at TP10 on the Data PCBA with the tape moving in the forward direction, ease the

edge of the tape off the head guide cap toward the spring-loaded washer. This should be done on first one guide, then the other.

NOTE

Moving the tape one- to two-thousandths of an inch from one of the guides will reduce the skew to within the specified range.

(3) Observe the waveform and determine which movement (left or right guide) improves the display. If moving the tape off the left guide improved the display, the right guide should be shimmed.

NOTE

The shims are burr-free, etched, one-half of a thousandths inch thick berrylium copper.

(4) Observe and note the fall time of the waveform observed at TP10 with the oscilloscope set up as described in Paragraph 6.6.3.1, Step (4).

(5) Since the character spacing at 800 cpi is 1250 μinches, the actual skew can be calculated. The skew correction provided by the addition of one shim (each shim is 500 μinches thick) is $\frac{500}{10} = 50$ μinches. The number of shims used must satisfy the following.

(a) Skew must be reduced to a minimum consistent with the maximum number of shims allowable.

(b) The maximum number of shims used must not exceed four.

Therefore, if, for example the measured skew is 350 μinches, four shims will yield a skew correction of 200 μinches (i.e., $4 \times \frac{500}{10} = 200$ μinches). This satisfies the requirements listed in (a) and (b).

(6) Depress and release the FORWARD control; tape motion will cease.

(7) Remove the head guide retaining screw (accessible from the rear of the deck) and remove the guide.

NOTE

When removing the guide care should be taken not to drop the spring and washer.

(8) Insert the required number of shims and replace the head guides.

NOTE

Shim only one head guide.

(9) Recheck skew measurement as described in Paragraph 6.6.3.1, Steps (1) through (6).

6.6.3.3 Read Skew Measurement

Measurement of read skew is accomplished by reading an all-ones tape with the read head connector plugged into the read head receptacle (J3) on the Data PCBA. This measurement is accomplished as follows.

(1) Set the vertical sensitivity of a Tektronix 561 oscilloscope (or equivalent) to 1.0v/cm.

(2) Set the oscilloscope to trigger on Channel 1, negative slope, alternate mode.

(3) Load an 800 cpi master tape on the transport, bring to BOT, and activate the FORWARD control.

(4) Observe oscilloscope waveform and adjust the horizontal time/division fixed and variable controls to display one complete cycle.

NOTE

With an 800 cpi tape, each half-cycle represents 1250 μinches. The scope graticule is divided into 10 major divisions, each of which is divided into 5 divisions; therefore,

$$\frac{2500\ \mu\text{inch}}{50\ \text{divisions}} = 50\ \mu\text{inch/division}$$

(5) Observe that the fall time of the waveform viewed at TP10 is less than eight small divisions of the oscilloscope graticule, i.e., 400 μinches. This measurement should be taken between the 95- and 5-percent points of the waveform.

NOTE

If the fall time of the waveform is greater than 400 μinches, perform the Write Skew Adjustment (Paragraph 6.6.3.2) and repeat the Read Skew Measurement (Paragraph 6.6.3.3).

6.6.4 HEAD REPLACEMENT

The head may require replacement for one of two reasons: internal fault in the head or cable, or wear. The first reason can be established by reading a master tape; the second can be verified by measuring the depth of the wear on the head crown. In those heads which have "guttering" (grooves cut on the crown, each side of the tape path), the head should be replaced when it has worn down to the depth of the gutter. In those heads which do not have guttering, the head wear should be measured with a brass shim that is ten-thousandths of an inch thick. The shim width should be placed in the worn portion of the head crown with one side butted against the outer worn step. When the upper surface of the shim is below the unworn surface of the head crown (i.e., the head has worn to a depth of greater than 0.010 inch) the head should be replaced.

Replacement of the head is accomplished as follows.

(1) Remove the head cover.

(2) Disconnect the head connectors from the Data PCBA.

(3) Loosen the screws that retain the overlay.

(4) Remove the two screws that attach the head to the deck.

(5) Ease the head cable through the hole in the deck.

(6) Check the replacement head for particles adhering to the mounting surface.

NOTE

The mounting surface must be free of all foreign substances or excessive skew will result.

(7) Route the head connectors and cable through the overlay and the deck.

(8) Mate the cable connector to J2 and J3 on the Data PCBA.

(9) Attach the head with the two screws removed in Step (4).

(10) Set up the read amplifier gains and skew as described in Paragraphs 6.5.8 and 6.6.3, respectively.

NOTE

Shim only one head guide.

(11) Replace the head cover.

6.6.5 PHOTO-TAB SENSOR REPLACEMENT

Replacement of the photo-tab sensor is accomplished as follows.

(1) Disconnect the cable connecting the photo-tab sensor to the Tape Control PCBA or the EOT/BOT Amplifier PCBA.

(2) Remove the screw that retains the sensor assembly (the screw is accessible from the rear of the deck).

(3) Remove all of the photo-tab sensor wires from the Molex connector with a Molex pin extractor tool.

(4) Pass the cable through the hole in the deck.

(5) Insert the replacement photo-tab sensor cable, without the connector, through the overlay and deck. Install Molex connector.

(6) Align the surface of the photo-sensor parallel to the tape and tighten the retaining screw.

(7) Adjust the BOT and EOT amplifiers as described in Paragraphs 6.5.3 through 6.5.5.

6.6.6 FLUX GATE ADJUSTMENT

Crosstalk can be checked and reduced, if necessary, to within acceptable limits by mechanically positioning the flux gate. The check and adjustment procedure is accomplished as follows.

(1) Load a reel of tape with a write enable ring installed on the transport. Do not pass tape over the capstan.

(2) Apply power to the transport.

(3) Bring the transport to Load Point artificially by placing a white card between the tape and photosensor assembly and depressing the LOAD control.

(4) Place the transport On-line.

(5) Write a continuous all-ones tape (see Paragraph 6.5.8.4).

(6) Using a Tektronix 561 oscilloscope (or equivalent), with the transport operating in the forward direction, observe the waveforms at TP104 through TP904 on the Data PCBA.

(7) Observe that the waveforms viewed in Step (6) are approximately sinusoidal with no pronounced peaks. The maximum allowable crosstalk voltage is 2v peak-to-peak.

NOTE

If the waveforms fall within the limit specified, no adjustment should be attempted.

(8) Partially loosen the screws which secure the flux gate assembly. Care should be taken to ensure that the flux gate spring does not move the assembly.

(9) Place a white card (e.g., business card) between the flux gate and the magnetic head and press the flux gate assembly lightly against the head.

(10) Figure 6-4 illustrates the correct relationship between the magnetic head and the flux gate.

NOTE

It may be necessary to move or rotate the assembly slightly to achieve the best compromise between all tracks.

(11) Tighten the flux gate assembly screws and repeat Steps (1) through (11).

<u>CAUTION</u>

ENSURE ADEQUATE CLEARANCE BETWEEN THE FLUX GATE AND THE MAGNETIC HEAD (0.005 INCH MINIMUM). FAILURE TO ALLOW CORRECT CLEARANCE WILL RESULT IN DAMAGE TO THE HEAD.

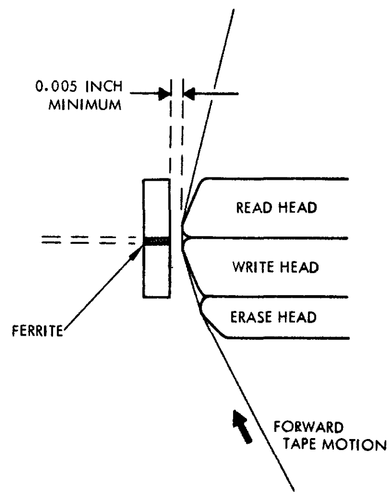


Figure 6-4. **Flux Gate Adjustment**

6.6.7 CAPSTAN MOTOR ASSEMBLY REPLACEMENT

Replacement of the capstan motor assembly is accomplished as follows.

(1) Remove the head cover.

(2) Remove the take-up hub by loosening one set-screw accessible through the hole in the rim of the hub.

(3) Remove the capstan by loosening one set-screw accessible between the overlay and the deck.

(4) Loosen screws 'A' through 'H' that retain the overlay (as illustrated in Figure 6-2). Note that screw 'F' is a No. 6 Allen head screw; this screw must be removed and reinstalled with an Allen wrench bit that is at least 6-1/2 inches long.

(5) Remove the trim assembly.

(6) Disconnect the plug which connects the three deck-mounted motors to the Tape Control PCBA.

(7) Remove the four leads from the capstan motor (at the connector) using the molex pin extractor tool.

(8) Loosen the four screws that secure the capstan motor to the tape deck. Inspect each screw shank and note the number of shims (if any) on each screw. If shims are present, note quantity and location.

(9) Remove the capstan motor.

(10) Mount the replacement capstan motor. When replacing screws, ensure that the same number of shims are used in the same positions as noted in Step (8).

NOTE

The mounting surface must be free of all foreign substances to ensure the perpendicularity of the capstan to the tape path.

(11) Refer to Schematic 101291 for corresponding lead colors and pin numbers at J9 on the Tape Control PCBA; insert the four leads in the correct location in the plug.

(12) Connect the plug which connects the motor to the Tape Control PCBA.

(13) Remount the capstan and take-up hub temporarily and check the read system skew as described in Paragraph 6.6.3.1.

(14) Remove the capstan and take-up hub and reinstall the trim assembly.

(15) Reinstall the capstan and take-up hub. Tighten the setscrews.

(16) Replace the head cover.

6.6.8 REEL SERVO BELT TENSION

The toothed belts that couple the motors to the reel hubs must have sufficient tension to prevent the teeth from skipping or servo instability due to backlash. The belts must not have excessive tension as this will cause overloading of the motor or reel shaft bearings in the radial direction. Belt tension can be adjusted as follows.

(1) Loosen the three screws that fasten the motor mounting plate to the deck standoffs.

NOTE

The slots in the motor mounting plate allow motion of the motor in the line of action of belt tension.

(2) Adjust the pulley so that the timing belt is snug. Note the last belt tooth that is completely seated in a slot on the large pulley. Refer to Figure 6-5.

(3) Count two to three teeth from the last engaged tooth. Hold the large pulley to ensure that it does not turn. Depress the toothed belt at the point between the second and third teeth with sufficient force to deflect the belt flush against the gear.

(4) Adjust the drive motor assembly so that the second tooth is firmly engaged in a slot on the large pulley but the third belt tooth is not engaged.

(5) Tighten the three screws on the motor mounting plate and recheck for the condition in Step (2).

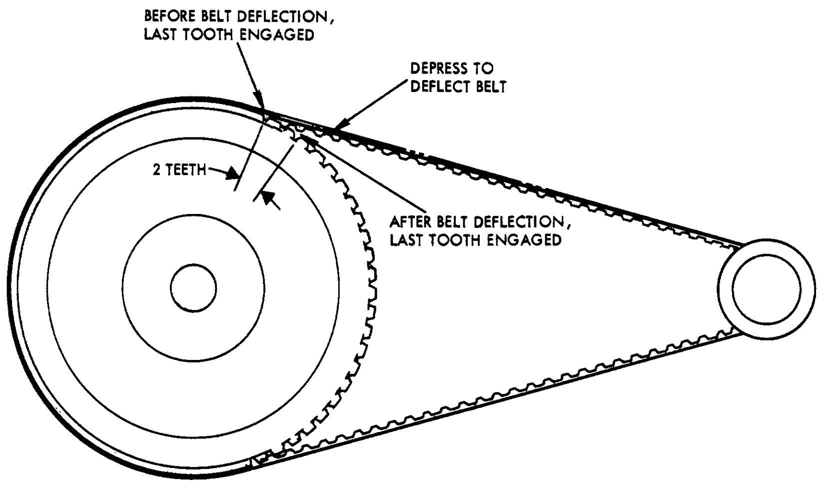


Figure 6-5. Reel Servo Belt Tension Adjustment

6.6.9 TAPE PATH ALIGNMENT

Alignment of the supply and take-up guide rollers to the head guides is accomplished by using the PERTEC Universal Tape Alignment Tool, Part No. 102382-01. This alignment tool is also used to establish guide roller parallelism and the positioning of the tape reel.

Since this tool can be used on all PERTEC tape transports, not all hole combinations or tool positions are used on any one transport for alignment. Only those holes required to accomplish tape path alignment on this model transport will be identified within the text and shown on the supporting figures.

CAUTION

THE PERTEC ALIGNMENT TOOL IS A PRECISION INSTRUMENT. CARE MUST BE TAKEN TO AVOID DAMAGE TO ALL CONTACTING SURFACES. STORE TOOL IN THE PROTECTIVE CONTAINER FURNISHED.

The user of this Universal Tape Path Alignment Tool will note that there are 13 clearance holes through the U-frame lettered 'a' through 'm'. The crossbar used in conjunction with the U-frame has 4-40 tapped holes lettered 'n', 'o', 'p', 'r' and 's'. Three identical knurled 4-40 thumbscrews are furnished and they will be referred to in the text as thumbscrews 'A', 'B' and 'C'.

6.6.10 TAPE PATH ALIGNMENT – TAKE-UP

6.6.10.1 Transport Preparation

Refer to Figure 6-2 for parts location relevant to the following procedure.

(1) Remove the protective cover enclosing the head, the tape guides and tape cleaner by firming grasping the head cover and pulling upward and away from the tape deck.

(2) Remove machine screws 'A' through 'H' that retain the overlay. Note that screw 'F' is an Allen head screw. This screw is removed using an Allen wrench with a shank at least 6-1/2 inches long.

CAUTION

WHEN REMOVING OVERLAY, CARE MUST BE TAKEN TO PREVENT OVERLAY FROM COMING IN PHYSICAL CONTACT WITH THE HEAD.

(3) After removal of overlay protect the tape path area of the head from damage and contamination by taping a pad of soft, non-abrasive, material over the head laminations.

(4) Remove tape guide cap screws 'K' and 'L', from each fixed tape guide post. Prevent loosening of guide post retaining screws 'J' and 'M' by engaging and holding an Allen wrench in the respective socket heads.

(5) Install U-frame to head guide posts using thumbscrews 'B' and 'C'.

CAUTION

ENSURE THAT HEAD CABLE IS NOT DAMAGED BY EDGE OF U-FRAME DURING INSTALLATION.

(a) Pass thumbscrew 'B' through U-frame clearance hole 'i' and thread into right tape guide post.

(b) Pass thumbscrew 'C' through U-frame clearance hole 'c' and thread into left tape guide post.

(6) Remove tape cleaner (refer to Paragraph 6.6.14).

(7) Depress ring guides on each head guide towards tape deck. Secure in place with an adhesive type tape.

6.6.11 TAKE-UP ARM GUIDE ROLLER

Refer to the stamped clearance hole lettering on the alignment tool and Figure 6-6 in conjunction with the following procedures.

6.6.11.1 Take-Up Arm Guide Roller Height Check

(1) Pass thumbscrew 'A' through U-frame clearance hole 'a' and thread into crossbar hole 'p'.

(2) Swing take-up guide roller away from stop.

(3) Position crossbar so contact is made between bottom side of crossbar and top side of guide roller. Tighten thumbscrew 'A' finger tight.

(4) Determine that the crossbar contacts the center of the tape traction area of guide roller. If crossbar is not centered, a guide roller height adjustment is required.

(5) Return take-up arm to rest position.

NOTE

Retain crossbar in present location for the following adjustment.

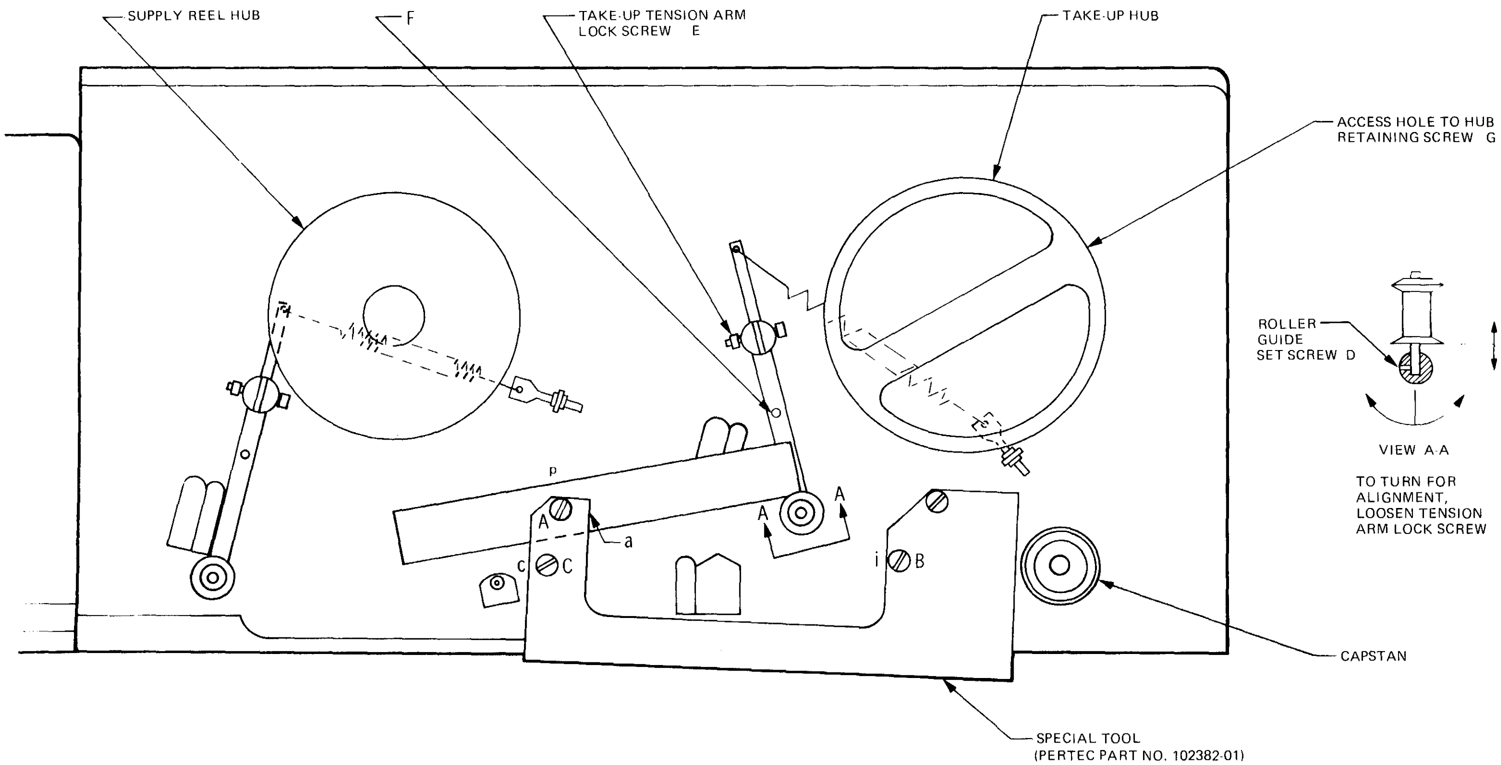


Figure 6-6. Take-up Reel Tension Arm Guide Roller Adjustments

6.6.11.2 Take-Up Arm Guide Roller Height Adjustment

If the take-up arm guide roller height check, performed in Paragraph 6.6.11.1, indicates a height adjustment is required, proceed as follows.

(1) With crossbar in place, loosen take-up arm guide roller set screw 'D', located on the take-up tension arm. See illustration at extreme right of Figure 6-6.

(2) Center tape traction area of guide roller on crossbar when guide roller is positioned at the midpoint of its operating arc.

(3) When height is established, tighten the take-up guide roller set-screw 'D'.

(4) Remove crossbar from U-frame.

6.6.11.3 Take-Up Arm Guide Roller Parallelism Check

Check take-up arm guide roller parallelism as follows.

(1) Reposition crossbar. Pass thumbscrew 'A' through U-frame clearance hole 'm' and thread into crossbar hole 'p'.

(2) Swing take-up arm to a position where end section of crossbar contacts tape traction area of guide roller.

(3) Sight along the end section of crossbar that is now in contact with the tape traction area of the guide roller.

(4) Observe an equal contact between the tape traction area of the guide roller and the end section of crossbar.

(5) If a light path is observed between the two surfaces, an adjustment is required.

NOTE

Retain crossbar in present location for the following adjustment.

6.6.11.4 Take-Up Arm Guide Roller Parallelism Adjustment

If the take-up arm guide roller parallelism check, performed in Paragraph 6.6.11.3, indicates that an adjustment is required, proceed as follows.

(1) Engage an Allen wrench in the head of Allen head lock-screw 'E' (Figure 6-6). With an open end wrench of appropriate size, slightly back off tension arm lock-nut.

(2) Insert a suitable rod or tool into through-hole 'F'.

(3) Rotate tension arm until the face of guide roller and the contacting surface of the crossbar are parallel.

(4) Test by sighting between the two surfaces. Observe a minimum amount of light between the parallel surfaces.

(5) Tighten tension arm lock-screw 'E' to a torque setting of 20 inch-pounds, nominal.

NOTE

Retain crossbar in present location for the following adjustment.

6.6.11.5 Take-Up Hub Centering Check

For proper tape stacking, the tape from the guide roller must be centered upon the tape retaining area of the hub. To check the centering, proceed as follows.

(1) Position crossbar so there is contact with the tape retention area of the hub. Tighten thumbscrew 'A' finger tight.

(2) With the crossbar secured in place, observe centering of the parallel edges of the crossbar contacting the tape retention area on the hub.

(3) If one edge of the crossbar is closed to either edge of the hub, a height adjustment is required.

NOTE

Retain crossbar in present location for the following adjustment.

6.6.11.6 Take-Up Hub Height Adjustment

Take-up hub height adjustment is made as follows.

(1) Remove tape retention strip from take-up hub.

(2) Loosen hub retaining screw 'G'.

(3) Adjust hub to required height so centerline of hub aligns with centerline of crossbar.

(4) Tighten retaining screw 'G'.

(5) Replace tape retention strip.

NOTE

Retain crossbar in present location for the following adjustment.

6.6.11.7 Capstan Height and Parallelism Check

Capstan height adjustment is accomplished as follows.

(1) Position crossbar so bottom surface contacts tape transporting area of capstan. Tighten thumbscrew 'A'.

(2) Observe contacting area between crossbar and tape transporting area. Observe an equal display of tape traction area on each side of crossbar.

(3) Rotate capstan hub and observe any out-of-roundness between crossbar and tape traction area.

(4) If capstan does not run true, check tightness of capstan motor mounting screws. Recheck for out-of-round condition of capstan. Replace capstan if tightening of motor mounting screws does not correct out-of-round condition.

(5) If capstan requires centering (height adjustment) loosen setscrew in capstan flange and adjust height to conform to requirements of Step (2).

(6) Remove crossbar from U-frame.

6.6.11.8 Tape Head Guide Check (Right Guide)

(1) Reposition crossbar. Pass thumbscrew 'A' through U-frame clearance hole 'f' and thread into crossbar hole 'p'.

(2) Position narrow section of crossbar against tape transporting area of head guide. Tighten thumbscrew 'A' finger tight.

(3) Observe contacting area between crossbar and tape transporting area.

(4) Determine that head guide is parallel and contacts entire narrow section of crossbar.

(5) If tape guide is not parallel to crossbar, loosen head guide retaining screw on back of tape deck and rotate head guide post.

(6) Tighten head guide post retaining screw and recheck.

(7) Remove crossbar from U-frame.

6.6.11.9 Return Transport To Operation Status

(1) Remove U-frame from guide posts.

(2) Replace tape guide caps, remove adhesive-type tape from ring guides.

(3) Clean and install tape cleaner.

(4) Replace overlay. Perform Steps (1) and (2) of Paragraph 6.6.10.1 in reverse order.

(5) Perform inspection of transport for general condition of servo belts and condition of wiring.

(6) Replace alignment tool in case.

6.6.12 TAPE PATH ALIGNMENT – SUPPLY

6.6.12.1 Transport Preparation

Refer to Figure 6-2 for parts location relevant to the following procedure.

(1) Remove the protective cover enclosing the head, the tape guides and tape cleaner by firmly grasping the head cover and pulling upward and away from the tape deck.

(2) Remove machine screws 'A' through 'H' that retain the overlay. Note that screw 'F' is an Allen head screw. This screw is removed using an Allen wrench with a shank at least 6-1/2 inches long.

CAUTION

WHEN REMOVING OVERLAY, CARE MUST BE TAKEN TO PREVENT OVERLAY FROM COMING IN PHYSICAL CONTACT WITH THE TAPE AREA OF THE HEAD.

(3) After removal of overlay protect the tape path area of the head from damage and contamination by taping a pad of soft, non-abrasive, material over the head laminations.

(4) Remove tape guide cap screws 'K' and 'L' from each fixed tape guide post. Prevent loosening of guide post retaining screws 'J' and 'M' by engaging and holding an Allen wrench in the respective socket heads.

(5) Install U-frame to head guide posts using thumbscrews 'B' and 'C'.

CAUTION

ENSURE THAT HEAD CABLE IS NOT DAMAGED BY EDGE OF U-FRAME DURING INSTALLATION.

(a) Pass thumbscrew 'B' through U-frame clearance hole 'i' and thread into right tape guide post.

(b) Pass thumbscrew 'C' through U-frame clearance hole 'c' and thread into left tape guide post.

(6) Remove tape cleaner. (Refer to Paragraph 6.6.14.)

(7) Depress ring guides on each head guide towards tape deck. Secure in place with an adhesive-type tape.

6.6.13 SUPPLY ARM GUIDE ROLLER

Refer to the stamped clearance hole lettering on the alignment tool and Figure 6-7 in conjunction with the following procedures.

6.6.13.1 Supply Arm Guide Roller Height Check

(1) Pass thumbscrew 'A' through U-frame clearance hole 'a' and thread into hole 'n' of crossbar.

(2) Position crossbar so contact is made between bottom side of supply guide roller and top surface of crossbar.

(3) Swing supply guide roller away from stop to a point midway of its operating arc. Tighten thumbscrew 'A' finger-tight.

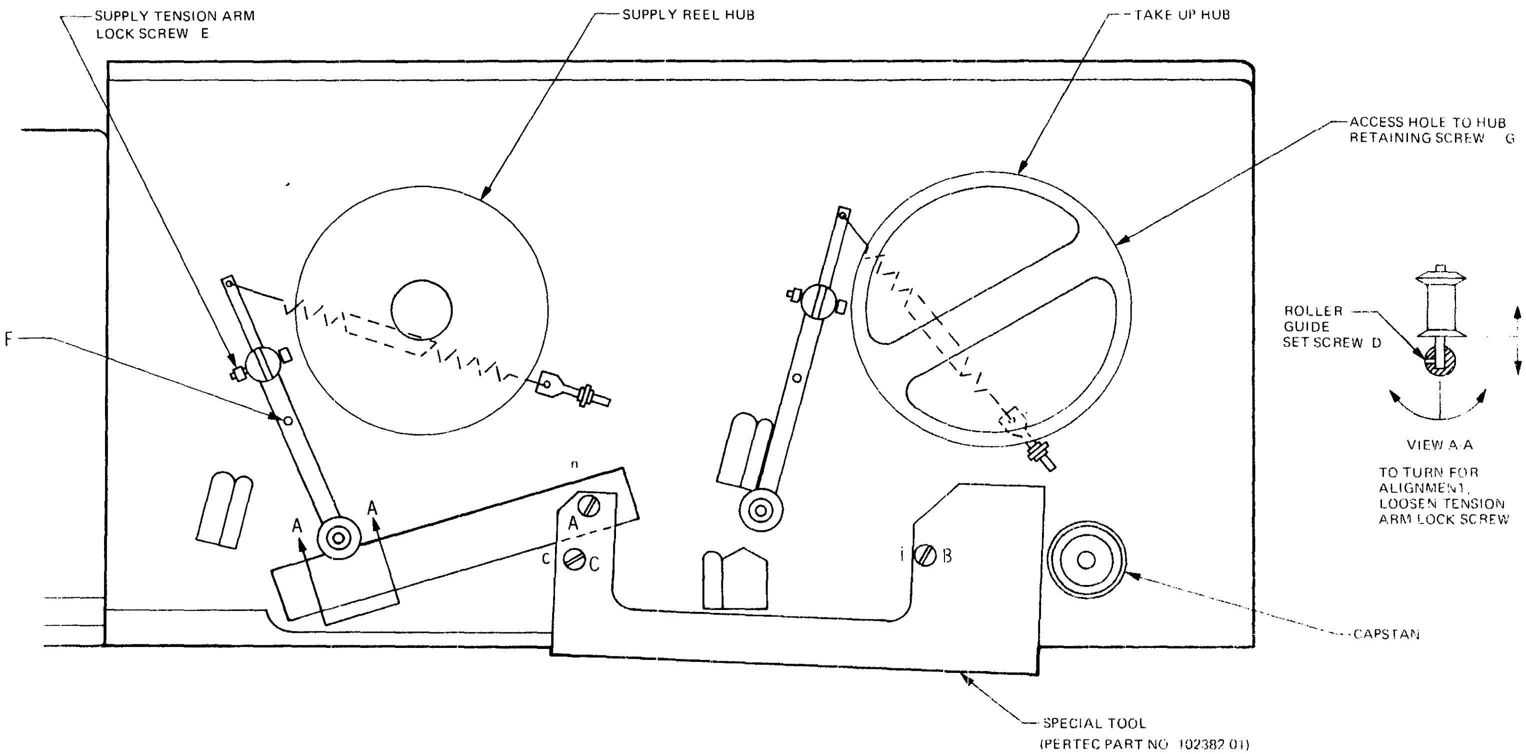


Figure 6-7. Supply Reel Tension Arm Guide Roller Adjustments

(4) Determine that the crossbar contacts the center of the tape traction area of the guide roller. If crossbar is not centered, a guide roller height roller adjustment is required.

(5) Return supply arm to rest position.

NOTE

Retain crossbar in present location for the following adjustment.

6.6.13.2 Supply Arm Guide Roller Height Adjustment

If the supply guide roller height check, performed in Paragraph 6.6.13.1, indicates a height adjustment is required, proceed as follows.

(1) With crossbar in place, loosen supply guide roller set-screw 'D', located on the supply tension arm. See illustration at extreme right of Figure 6-8.

(2) Center tape traction area of guide roller on crossbar when guide roller is positioned at the midpoint of its operating arc.

(3) When height is established, tighten supply guide roller set-screw 'D'.

(4) Remove crossbar from U-frame.

6.6.13.3 Supply Arm Guide Roller Parallelism Check

(1) Reposition crossbar. Pass thumbscrew 'A' through U-frame clearance hole 'e' and thread into crossbar hole 'p'.

(2) Swing supply arm to a position where end section of crossbar contacts tape traction area of guide roller.

(3) Sight along the end section of crossbar that is now in contact with the tape traction area of the guide roller.

(4) Observe an equal contact between the tape traction area of the supply roller and the end section of the crossbar.

(5) If a light path is observed from edge to edge, an adjustment between the two surfaces is required.

NOTE

Retain crossbar in present location for the following adjustment.

6.6.13.4 Supply Arm Guide Roller Parallelism Adjustment

If the supply guide roller parallelism guide check, performed in Paragraph 6.6.13.3, indicates that an adjustment is required, proceed as follows.

(1) Engage an Allen wrench in the head of the Allen head lock-screw 'E' (Figure 6-7). With an open end wrench of appropriate size, slightly back off tension arm locknut.

(2) Insert a suitable rod or tool into the through-hole 'F'.

(3) Rotate tension arm until the face of the guide roller and the contacting surface of the crossbar are parallel.

(4) Test by sighting between the two surfaces. Observe a minimum amount of light between the two surfaces.

(5) Tighten tension arm lock-screw 'E' to a torque setting of 20 pinch-pounds, nominal.

NOTE

Retain crossbar in present location for the following adjustment.

6.6.13.5 Tape Head Guide Alignment Check (Left Guide)

(1) Loosen thumbscrew 'A'.

(2) Position crossbar so lower surface contacts the tape head guide. Tighten thumbscrew 'A'.

(3) Observe contacting area between crossbar and head guide.

(4) Determine that head guide is parallel and contacts entire width of crossbar.

(5) If not parallel to crossbar, loosen head guide retaining screw on back of tape deck and rotate head guide post.

(6) Tighten retaining screw and recheck.

(7) Remove crossbar from U-frame.

6.6.13.6 Supply Reel Flange Centering and Height Adjustment

(1) Install an empty tape reel on supply reel hub. Ensure tape reel is fully seated.

(2) Position crossbar (removed in Step (7) of Paragraph 6.6.13.5) in contact with tape delivery surface of the reel prior to attaching to crossbar as directed in Step (3).

(3) Reinstall crossbar to U-frame. Pass thumbscrew 'A' through clearance hole 'a' and thread into crossbar hole 'n'.

(4) Rotate reel and determine that reel surface is parallel to contacting surface of crossbar.

(5) While rotating reel observe average clearance between reel flanges. Each reel flange should be equidistant from the sides of crossbar. If not, ensure that reel

flanges are not warped or distorted out of shape. Recheck that supply reel is fully seated upon reel hub.

(6) If one edge of crossbar is closer to one reel flange, center reel flanges by loosening the two Allen head retaining screws located on the supply reel retained hub.

(7) Recheck alignment.

(8) Remove crossbar from U-frame.

(9) Remove tape reel from supply hub.

6.6.13.7 Return Transport To Operational Status

(1) Remove U-frame from guide posts.

(2) Replace tape guide caps. Remove adhesive-type tape from ring guides.

(3) Clean and install tape cleaner.

(4) Replace overlay. Perform Steps (1) and (2) of Paragraph 6.6.12.1 in reverse order.

(5) Perform inspection of transport for condition of servo belts and condition of wiring.

(6) Replace alignment tool in case.

6.6.14 TAPE CLEANER, CLEANING AND INSTALLATION

The tape cleaner is cleaned by removing the perforated mesh from the housing and blowing the accumulated oxide and dirt from the housing. The perforated mesh and housing should then be cleaned using a cotton swab moistened with 91 percent isopropyl alcohol. Care should be taken to ensure that fibers from the cotton swab do not adhere to the mesh. The mesh is relocated on the housing and the retaining screws tightened.

Installation is accomplished by carefully installing the tape cleaner as located by the dowel pin. Secure in place and tighten the Allen head screw.

CAUTION

ENSURE THAT THE PERFORATED MESH SURFACE OF THE TAPE CLEANER IS PARALLEL TO THE TAPE AND THAT THE TAPE IS WRAPPED SYMMETRICALLY AROUND THE TAPE CLEANER (THE ENTRY ANGLE IS EQUAL TO THE EXIT ANGLE).

6.6.15 TAPE TENSION

Tape tension is controlled by the spring attached to each of the tension arms. The tension is adjusted by means of the anchor screws. Figures 6-8 and 6-9 show the measurement and adjustment of the supply tape and take-up tape tension, respectively. A two-foot length of tape with loops at each end is used; after removing the overlay as described in Paragraph 6.6.12.1, Steps (1) and (2), tape is mounted as shown. A one-pound force gauge is used to measure tape tension. Care must be taken to zero the scale in the correct orientation and to pull on the tape in the direction shown. The anchor screw is adjusted until the tension is 7 ounces with the arm in the center of its operating region.

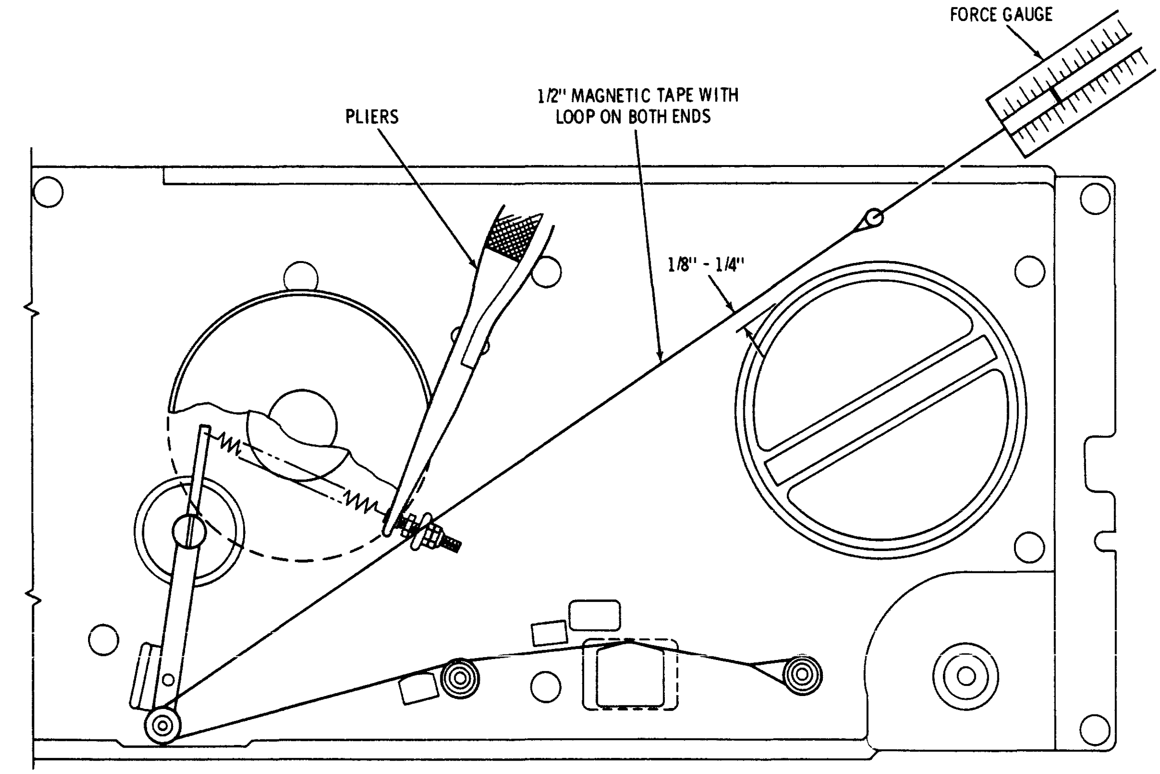


Figure 6-8. Tension Adjustment for Supply Reel

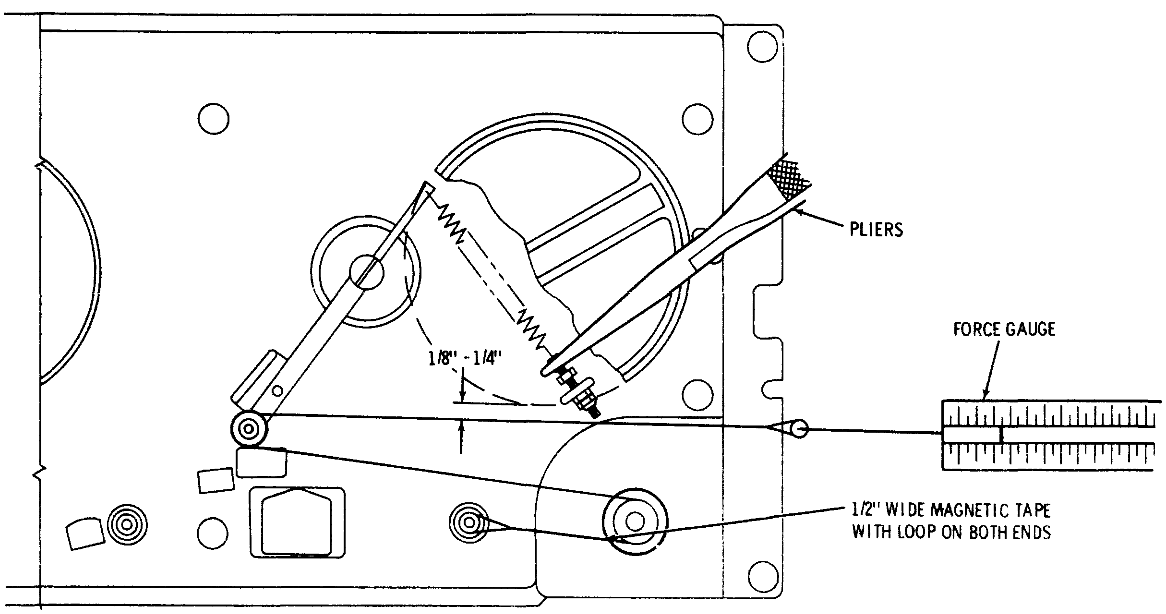


Figure 6-9. Tension Adjustment for Take-up Reel

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6.7 MAINTENANCE TOOLS

The following list of tools is required to maintain the tape transport. All tools, except for the tape path alignment tool (item 13) and the Molex pin extractor (item 15) may be obtained from local sources.

(1) Hex socket keys for 5/32, 1/8, 3/32 setscrews and a splined drive socket key for a 4-40 setscrew.

(2) Open-end wrenches for 3/16, 1/4, 5/16, and 3/8 bolts.

(3) Long-nose pliers.

(4) Phillips screwdriver set.

(5) Standard blade screwdriver set.

(6) Soldering aid.

(7) Soldering iron.

(8) One-pound force gauge.

(9) Lint-free cloth.

(10) Cotton swabs.

(11) 91 percent isopropyl alcohol.

(12) Torque wrench, 0 - 50 inch/pounds.

(13) Tape Path Alignment Tool, PERTEC Part No. 102382-01.

(14) Brass shims 0.010 for head wear measurement.

(15) Molex pin extractor, PERTEC Part No. 617-2023.

(16) Loctite Sealant, Grade C.

(17) Allen wrench, No. 6, with 6-1/2-inch shank.

6.8 TROUBLESHOOTING

Table 6-6, System Troubleshooting chart, provides a means of isolating faults, possible causes, and remedies. The troubleshooting chart is used in conjunction with the schematics, assembly drawings, and wiring diagrams in Section VII.

Table 6-6

System Troubleshooting

Symptom	Probable Cause	Remedy	Reference
Tape does not tension and the capstan shaft rotates freely when the LOAD control is depressed for the first time after threading tape.	Interlock relay K1 does not close.	Check operation of relay. Replace if necessary.	Paragraph 5.2.2.1
	LOAD control is not operative.	Check operation of control. Replace if necessary.	Paragraph 5.2.2.1
	Relay driver defective.	Check collector voltage of Q3 with LOAD control depressed. It should be less than +1 volt. If greater, isolate defective relay driver component and replace.	Paragraph 5.2.2.1
Tape is tensioned when the LOAD control is depressed, but tension is lost when control is released.	Relay latching contacts 15 and 16 do not make.	Check that voltage at TP23 goes to +5 volts when LOAD control is depressed.	Paragraph 5.2.2.1
	Limit switch is not operative.	Adjust as described in Paragraph 6.6.1; possibly replace limit switch assembly.	Paragraph 6.6.1
Tape unwinds or tension arm hits stop when the LOAD control is depressed for the first time.	Tape is improperly threaded.	Rethread tape – see molded arrows on overlay.	Paragraph 3.3
	+5 or -5 volts is missing from tension arm sensor.	Check tension arm sensor lamps. Isolate problem if lamp is extinguished.	Paragraph 6.6.2
	Fault in reel servo amplifier.	Check that movement of reels responds to tension arm position without tape on the transport.	Paragraph 5.2.2.1

Table 6-6

System Troubleshooting (Continued)

Symptom	Probable Cause	Remedy	Reference
Tape "runs away" or rewinds when LOAD control is depressed for the second time.	Fault on Tape Control or capstan motor assembly.	Replace or repair Tape Control or capstan motor assembly.	Paragraph 5.2.2.1, 6.6.7
Tape runs past the BOT marker.	BOT tab dirty or tarnished.	Replace tab or increase sensitivity of photosensor amplifier.	Paragraph 6.5.3
	Photosensor not properly adjusted.	Adjust photosensor amplifier.	Paragraph 6.5.3.3
	Photosensor or amplifier defective.	Check for +3.25 to +4.5v at TP2 on EOT/BOT Amplifier PCBA with blank tape under sensor. Check that voltage drops at least 0.8v when tab is under the photosensor.	Paragraph 6.5.3.2
	Logic fault (Load flip-flop does not reset).	Replace or repair Tape Control.	Paragraph 5.2.2.1
Transport does not move in response to SYNCHRONOUS FORWARD or SYNCHRONOUS REVERSE commands.	Interface cable fault or receiver fault.	Check levels at outputs and inputs of receivers on Tape Control. Replace or repair cable or Tape Control.	Paragraph 5.2.2.1
	Transport is not READY.	Replace or repair Tape Control.	Paragraph 5.2.2.1
	Fault in ramp generator or capstan servo amplifier.	Check TP18 on Tape Control. Replace or repair Tape Control.	Paragraph 5.2.2.1

Table 6-6

System Troubleshooting (Continued)

Symptom	Probable Cause	Remedy	Reference
Transport responds to SYNCHRONOUS FORWARD command, but tape is not written.	Write current is not enabled.	Check presence of Write Enable ring on supply reel (WRT EN indicator should be lit). Check TP16 on Tape Control (should be +5v for writing). Replace Write Lockout assembly if faulty. Check that WRT POWER level is +5v on Data board.	Paragraph 5.2.1.1 and Paragraph 5.2.2.1
	Write status or MOTION signal to Data board is not correct.	Check receiver on Tape Control for WRITE status and on Data board for WRITE status.	Paragraph 5.2.1.1 and Paragraph 5.2.2.1
		Check Data board for MOTION signal. Replace or repair Data board or Tape Control board if faulty.	Paragraph 5.2.1.1 and Paragraph 5.2.2.1
	WRITE DATA or WRITE DATA STROBE is not correctly received on Data board from interface.	Check presence of correct levels on Data board. Replace or repair Data board or interface cable if faulty.	Paragraph 5.2.1.1
	Head not plugged in.	Check J2 and J3 on Data board.	—

Table 6-6

System Troubleshooting (Continued)

Symptom	Probable Cause	Remedy	Reference
Data are incorrectly written	Incorrect data format.	Use correct format.	IBM Form A22-6589-3 (729 or 727 Series) IBM Form A22-6866-3 (2400 Series)
	Fault on one track due to failure in write circuits.	Check receiver and write amplifier on Data PCBA. Replace or repair Data PCBA if faulty.	Paragraph 5.2.1.1
	Intermittent WRT POWER, WRITE MOTION, or WARS signal.	Examine those signals and replace or repair Tape Control PCBA or Write Lockout assembly or Data PCBA if faulty.	Paragraph 5.2.1.1 and Paragraph 5.2.2.1
Correct tape cannot be read.	Interface cable or transmitter fault.	Replace or repair interface cable or Data PCBA.	Paragraph 5.2.1.1
	Head is not plugged in.	Check J2 on Data PCBA; Check J3 on Data PCBA.	—
	Head and guides need cleaning.	Clean head and guides.	Paragraph 6.3.1

Table 6-6

System Troubleshooting (Continued)

Symptom	Probable Cause	Remedy	Reference
Correct tape cannot be read (continued)	Tape cleaner needs emptying.	Remove tape cleaner and clean.	Paragraph 6.6.14
	Read amplifier gains are incorrectly adjusted.	Check and adjust amplifier gains.	Paragraph 6.5.8
	Faulty write amplifier causes current to be passed through head while reading.	Check write amplifier output test points and replace or repair Data PCBA if faulty.	Paragraph 5.2.1.1
	Component fault in read channel.	Check test points on Data PCBA. Replace or repair Data PCBA.	Paragraph 5.2.1.1
	Threshold level incorrect.	Check level at TP6 on Data PCBA. Replace or repair Data PCBA.	Paragraph 6.5.9

SECTION VII

SCHEMATICS, PARTS LISTS, LOGIC LEVELS, AND WAVEFORMS

7.1 INTRODUCTION

This section includes the schematics, assembly drawings, illustrated parts lists, interconnect lists, logic level, and waveform definitions.

7.2 ILLUSTRATED PARTS BREAKDOWN (IPB)

Figure 7-1 through 7-4, used in conjunction with Tables 7-1 through 7-4, provide identification by PERTEC part number of the mechanical and electrical components of the transport.

When part numbers for a particular part differ due to a change in transport configuration, descriptions and part numbers for all configurations are listed.

7.3 RECOMMENDED SPARE PARTS

Table 7-5 provides a description of the recommended spare parts for the transport. The customer should always furnish model number and serial number of the transport when ordering parts.

7.4 PART NUMBER CROSS REFERENCE

Table 7-6, Part Number Cross Reference, provides a cross reference to the manufacturer's part number from typical PERTEC part numbers.

7.5 PCBA INTERCONNECTIONS

Interconnections between PCBAs installed in the transport are listed in Table 7-7.

7.6 LOGIC LEVELS AND WAVEFORMS

The transport control and interface logic uses the DTL800 series of logic elements. Logic levels are defined as follows.

+5v	logical true
+0.4v	logical false

All basic waveform names are chosen to correspond to the logical true condition; e.g., SET WRITE STATUS (ISWS) enables the write circuits when it is logically true (+5v), or disables the write circuits when it is logically false (0v).

The inverse of a waveform is denoted by the prefix "N". Therefore, NBOT will be 0.4v when the BOT tab is under the photosensor head, or +5v otherwise.

All interface lines connecting the transport to the controller are prefixed by "I". Each line must be terminated at the receiver end of the cable by a 220/330-ohm divider chain between +5v and 0v.

All interface waveforms are low-true with logic levels: +3v — logical false; 0.4v — logical true.

For example, ISFC (SYNCHRONOUS FORWARD command) will be 0.4v when the transport is being driven in the forward direction, or +3v otherwise.

The Glossary contains the waveform mnemonics referred to in this manual.

NOTES

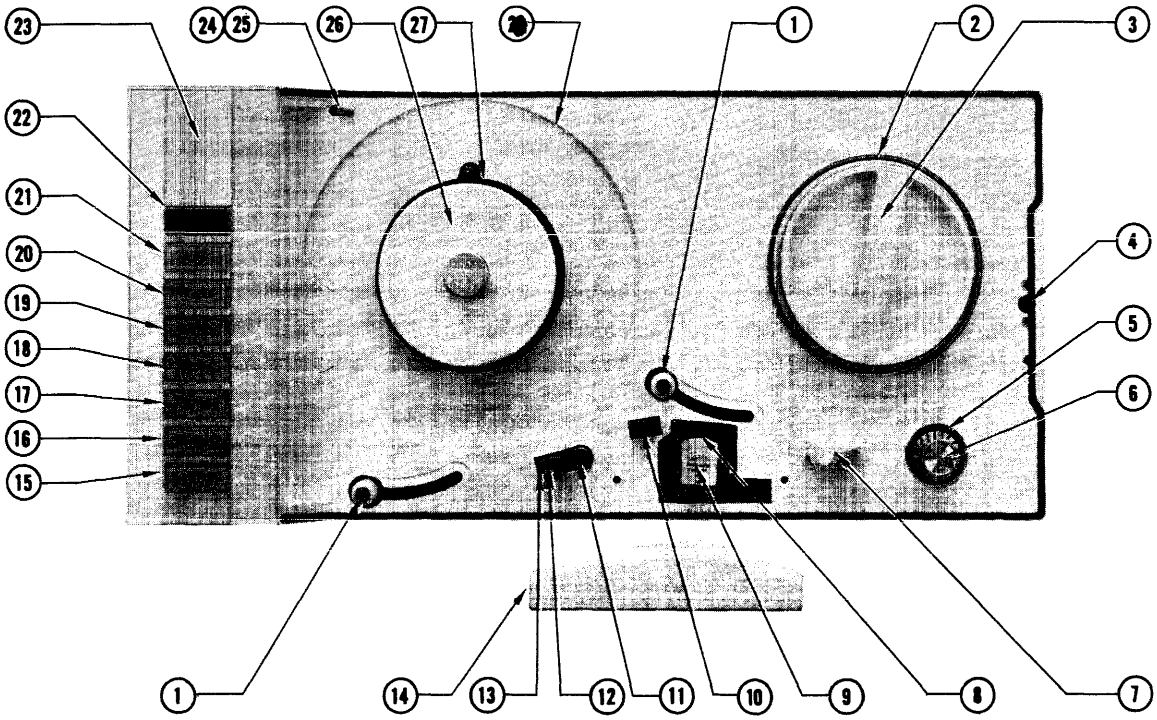


Figure 7-1. T7640 Transport Photo Parts Index

Table 7-1

T7640 Transport Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-1		
-1	100808-02	Guide Roller Assembly
-2	100821-01	Friction Ring
-3	100812-01	Take-up Hub Assembly
-4	615-0006	Catch Spring
-5	101744-10	Strobe Disk, 6.25 or 12.5 ips
	101744-09	Strobe Disk, 18.75 ips
	101744-08	Strobe Disk, 25.0 ips
-6	100725-01	Capstan, 6.25 or 12.5 ips
	102517-01	Capstan, 18.75 or 25.0 ips
-7	101166-01	Head Guide Cover
-8	103221-01	Flux Gate Assembly
-9	510-*	Magnetic Head
-10	100807-01	Photosensor Assembly
-11	100810-01	Head Guide Assembly (Matched Set)
	100298-01	Head Guide Shim
-12	602-0418	Cap Screw, 4-40, 1-1/8
-13	100811-01	Tape Cleaner Assembly
-14	100724-01	Head Assembly Cover
-15	505-1809	REVERSE Switch
-16	505-1808	FORWARD Switch
-17	505-1827	1600 CPI Switch (PE Units)
	505-1807	HI DEN Switch (7-track NRZI Units)
-18	505-1806	WRT EN Switch
-19	505-1805	REWIND Switch
-20	505-1804	ON LINE Switch
-21	505-1803	LOAD Switch
-22	505-1801	POWER Switch
	505-1847	POWER Switch (48V System)
-23	100815-01	Control Plate (8 Slots)
	100815-02	Control Plate (7 Slots, 9-track NRZI Units)
-24	611-0004	Retaining Ring, 3/16-inch Shaft
-25	100774-01	Limit Shaft Cover Door Stop
-26	100792-01	Supply Hub Assembly
-27	100117-01	Hold-down Ring
-28	101287-01	Overlay
Not Shown	101165-01	Cover Door Assembly

*Refer to Spare Parts List Table 7-5 for specific part number.

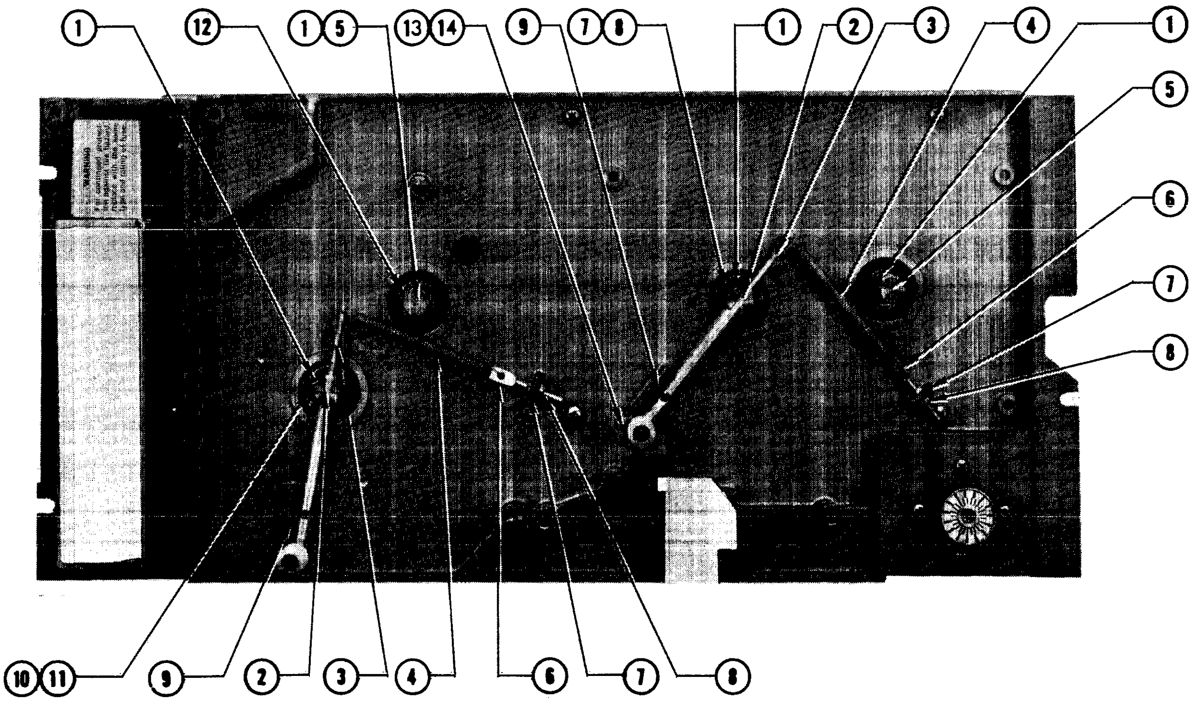


Figure 7-2. T7000 Series Transports Photo Parts Index

Table 7-2

T7000 Series Transports Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-2		
-1	613-0012	Bearing
-2	100846-01	Tension Arm Shaft
-3	102221-01	Tension Arm
-4	100275-01	Tension Arm Spring
-5	100846-02	Take-up Reel Shaft
-6	615-4210	Spade Bolt
-7	604-0400	Nut
-8	604-2600	Nut
-9	667-0028	Rubber Strip
-10	615-0832	Nut
-11	602-0812	Screw
-12	612-5624	Shim
	612-5623	Shim (Not Shown)
	102556-01	Bushing (Not Shown)
-13	602-0406	Screw
-14	605-0400	Washer

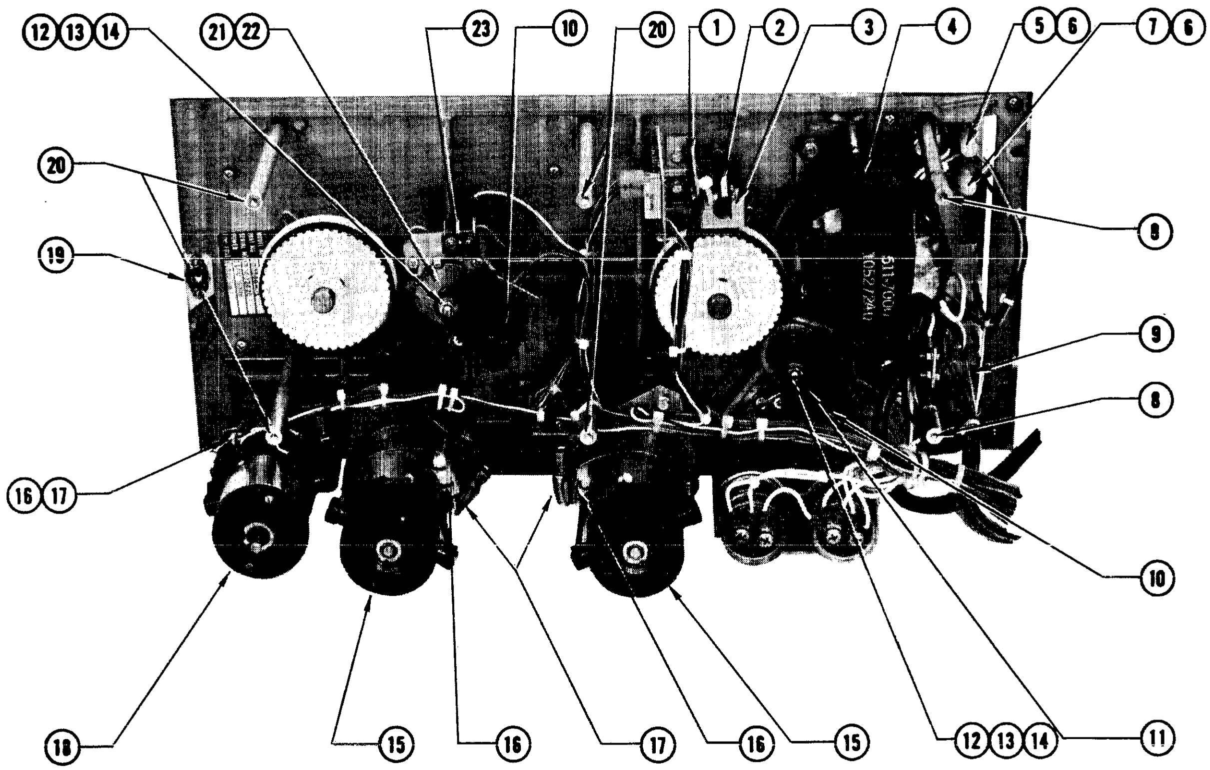


Figure 7-3. T7000 Series Transports Photo Parts Index

Table 7-3

T7000 Series Transports Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-3		
-1	101949-01	EOT/BOT Amplifier Assembly
-2	506-6360	Write Lockout Switch
-3	100817-01	Write Lockout Assembly
-4*	100803-01 100803-02	Power Supply Assembly, 18.75 ips and Less 25.0 ips
-5*	663-3050	Fuse, 5A, 3AG, Fast Blow, Bussman AGC-5
-6*	658-9160	Fuse Holder, Littlefuse 342014
-7*	663-3515	Fuse, 1.5A, 3AG, Slow Blow, Bussman MDX1.5
-8	100730-01	Hinged Standoff
-9	102021-01 102021-03	Switch Cable Switch Cable, Power Only, 48V System
-10	100858-01	Tension Arm Sensor Assembly
-11	100842-01	Shutter
-12	615-1032	Nut
-13	606-0001	Washer, Flat
-14	612-0021	Washer
-15	100805-01	Reel Motor Assembly
-16	102245-01	RFI Filter
-17	615-0114	Clamp
-18	100804-01 100804-02	Capstan Motor Assembly, 18.75 ips and Less 25.0 ips
-19	615-0006	Catch Spring
-20	100870-02	PCBA Standoff, 4-inch
-21	101669-01	Limit Switch Cam
-22	603-0002	Setscrew
-23	506-6360 506-0311	Limit Switch (only) for Limit Switch Assembly No. 100868-01, -02, -03, and -04 Versions; for -05 Versions only.

*Not Used on 48V Systems.

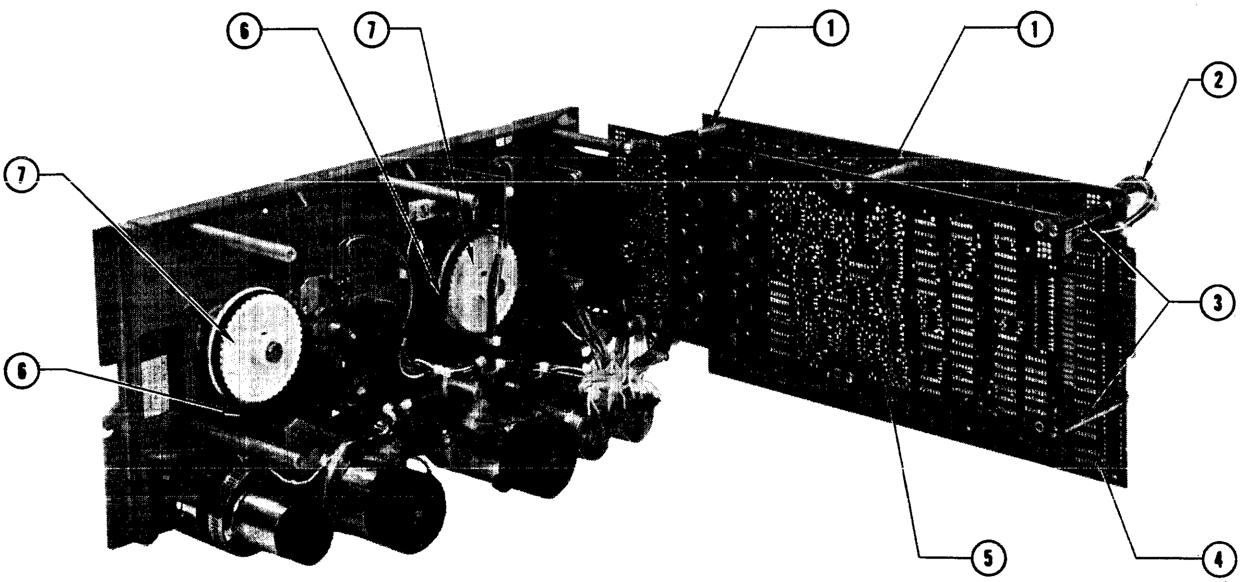


Figure 7-4. T7000 Series Transports Photo Parts Index

Table 7-4

T7000 Series Transports Photo Parts Index

Figure and Index No.	Part Number	Description
Figure 7-4		
-1	100870-03	PCBA Standoff, 2.81-inch
-2	100837-01	Cable and PCBA Interconnect
-3	100730-03	Hinged Standoff, 2.81-inch
-4	*	Data PCBA
-5	*	Tape Control PCBA
-6	610-0005	Belt, 70-tooth
-7	100775-01	Pulley, 44-tooth
	603-0002	Set Screw
Not Shown	104709-01	Power Input Cable (48V System)

*Refer to Spare Parts List Table 7-5 for Specific Part Number.

Table 7-5

T7640 Transport Recommended Spare Parts List

Item	Part No.
1. Tape Control B1 PCBA	101292-*
2. Data H (T7640) Data C9 (T7X40 9-track) Data C7 (T7X40 7-track)	101581-* 101105-* 101147-*
3. 48V Converter PCBA	102111-*
4. Capstan Motor Assembly (≤18.75 ips) Capstan Motor Assembly (25.0 ips)	100804-01 100804-02
5. Reel Motor Assembly (All Speeds)	100805-01
6. Photosensor Assembly	100807-01
7. Tension Arm Sensor Assembly	100858-01
8. POWER Switch POWER Switch, 48V System	505-1801 505-1847
10. LOAD Switch	505-1803
11. ON LINE Switch	505-1804
12. REWIND Switch	505-1805
13. WRT EN Switch	505-1806
14. HI DEN Switch (T7X40, 7-track) 1600 CPI Switch (T7640)	505-1807 505-1826
15. FORWARD Switch	505-1808
16. REVERSE Switch	505-1809
17. Roller Guide Assembly	100808-02
18. Head, T7X40 7-track Head, T7X40 9-track Head, T7640	510-6187 510-6189 510-6169
19. Head Guide Shim	100298-01

*Refer to your unit for version.

Table 7-6

Part Number Cross Reference

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Composition Resistors	(Comply with MIL-R-11)	
100-0395		3.9 ohms ±5%, 1/4w
100-1005		10 ohms ±5%, 1/4w
100-1015		100 ohms ±5%, 1/4w
100-1025		1.5k ohms ±5%, 1/4w
100-1055		1 meg ohm ±5%, 1/4w
100-1235		150 ohms ±5%, 1/4w
100-1525		1.5k ohms ±5%, 1/4w
100-1535		15k ohms ±5%, 1/4w
100-1815		180 ohms ±5%, 1/4w
100-1825		1.8k ohms ±5%, 1/4w
100-1845		180k ohms ±5%, 1/4w
100-2215		220 ohms ±5%, 1/4w
100-2225		2.2k ohms ±5%, 1/4w
100-2235		22k ohms ±5%, 1/4w
100-2705		27 ohms ±5%, 1/4w
100-2725		2.7k ohms ±5%, 1/4w
100-3305		33 ohms ±5%, 1/4w
100-3315		390 ohms ±5%, 1/4w
100-3325		3.3k ohms ±5%, 1/4w
100-3925		3.9k ohms ±5%, 1/4w
100-4705		47 ohms ±5%, 1/4w
100-4715		470 ohms ±5%, 1/4w
100-4725		4.7k ohms ±5%, 1/4w
100-5625		5.6k ohms ±5%, 1/4w
100-6805		68 ohms ±5%, 1/4w
100-6815		680 ohms ±5%, 1/4w
100-8215		820 ohms ±5%, 1/4w
100-8235		82k ohms ±5%, 1/4w
101-1025		1k ohms ±5%, 1/2w
101-1505		15 ohms ±5%, 1/2w
101-1515		150 ohms ±5%, 1/2w
101-2205		22 ohms ±5%, 1/2w
101-2715		270 ohms ±5%, 1/2w
101-3305		33 ohms ±5%, 1/2w
101-3325		3.3k ohms ±5%, 1/2w
101-3915		390 ohms ±5%, 1/2w
101-4715		470 ohms ±5%, 1/2w
101-6805		68 ohms ±5%, 1/2w
101-8205		82 ohms ±5%, 1/2w
102-5615		560 ohms ±5%, 1w
102-8205		82 ohms ±5%, 1w
103-1215		120 ohms ±5%, 2w
103-1815		180 ohms ±5%, 2w
103-4705		47 ohms ±5%, 2w

Table 7-6

Part Number Cross Reference (continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Precision Resistors	(Comply with MIL-R-11)	
104-1000		100 ohms ±1%, 1/4w
104-1001		1k ohms ±1%, 1/4w
104-1002		10k ohms ±1%, 1/4w
104-1003		100k ohms ±1%, 1/4w
104-1100		110 ohms ±1%, 1/4w
104-1101		1.1k ohms ±1%, 1/4w
104-1102		11k ohms ±1%, 1/4w
104-1211		1.21k ohms ±1%, 1/4w
104-1330		133 ohms ±1%, 1/4w
104-1331		1.33k ohms ±1%, 1/4w
104-1332		13.3k ohms ±1%, 1/4w
104-1623		162k ohms ±1%, 1/4w
104-1781		1.78k ohms ±1%, 1/4w
104-1782		17.8k ohms ±1%, 1/4w
104-1961		1.96k ohms ±1%, 1/4w
104-1962		19.6k ohms ±1%, 1/4w
104-2151		2.15k ohms ±1%, 1/4w
104-2152		21.5k ohms ±1%, 1/4w
104-2370		237 ohms ±1%, 1/4w
104-2610		261 ohms ±1%, 1/4w
104-2611		2.61k ohms ±1%, 1/4w
104-2612		26.1k ohms ±1%, 1/4w
104-2870		287 ohms ±1%, 1/4w
104-3481		3.48k ohms ±1%, 1/4w
104-3831		3.83k ohms ±1%, 1/4w
104-3832		38.3k ohms ±1%, 1/4w
104-3833		383 ohms ±1%, 1/4w
104-3482		34.8k ohms ±1%, 1/4w
104-3483		348k ohms ±1%, 1/4w
104-4220		422 ohms ±1%, 1/4w
104-4221		4.22k ohms ±1%, 1/4w
104-4222		42.2k ohms ±1%, 1/4w
104-4641		4.64k ohms ±1%, 1/4w
104-4753		475k ohms ±1%, 1/4w
104-5110		511 ohms ±1%, 1/4w
104-5111		5.11k ohms ±1%, 1/4w
104-5113		511k ohms ±1%, 1/4w
104-5620		562 ohms ±1%, 1/4w
104-5621		5.62k ohms ±1%, 1/4w
104-6192		61.9k ohms ±1%, 1/4w
104-6811		6.81k ohms ±1%, 1/4w
104-6812		68.1k ohms ±1%, 1/4w
104-7500		750 ohms ±1%, 1/4w
104-8252		82.5k ohms ±1%, 1/4w
104-9090		909 ohms ±1%, 1/4w

Table 7-6

Part Number Cross Reference (continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Precision Resistors (Continued)		
104-9092		90.9k ohms ±1%, 1/4w
104-9093		909k ohms ±1%, 1/4w
107-1000		100 ohms ±1%, 1/8w
107-1001		1k ohms ±1%, 1/8w
107-1002		10k ohms ±1%, 1/8w
107-1003		100k ohms ±1%, 1/8w
107-1101		1.1k ohms ±1%, 1/8w
107-1102		11k ohms ±1%, 1/8w
107-1211		1.21k ohms ±1%, 1/8w
107-1332		13.3k ohms ±1%, 1/8w
107-1471		1.47k ohms ±1%, 1/8w
107-1781		1.78k ohms ±1%, 1/8w
107-1782		17.8k ohms ±1%, 1/8w
107-1961		1.96k ohms ±1%, 1/8w
107-1962		19.6k ohms ±1%, 1/8w
107-1963		196k ohms ±1%, 1/8w
107-2152		21.5k ohms ±1%, 1/8w
107-2611		2.61k ohms ±1%, 1/8w
107-2612		26.1k ohms ±1%, 1/8w
107-2870		287 ohms ±1%, 1/8w
107-3482		34.8k ohms ±1%, 1/8w
107-3483		348k ohms ±1%, 1/8w
107-3832		38.3k ohms ±1%, 1/8w
107-4221		4.22k ohms ±1%, 1/8w
107-4222		42.2k ohms ±1%, 1/8w
107-5110		511 ohms ±1%, 1/8w
107-5111		5.11k ohms ±1%, 1/8w
107-5112		51.1k ohms ±1%, 1/8w
107-5113		511k ohms ±1%, 1/8w
107-5620		562 ohms ±1%, 1/8w
107-6192		61.9k ohms ±1%, 1/8w
107-6811		6.81k ohms ±1%, 1/8w
107-6812		68.1k ohms ±1%, 1/8w
107-8252		82.5k ohms ±1%, 1/8w
107-9090		909 ohms ±1%, 1/8w
109-0003		0.10 ohms ±3%, 5w
113-0111		10 ohms ±1%, 1w
Variable Resistors		
121-1020	Beckman	79PR1K, Variable, 1k ohms ±10%, 3/4w
121-1030	Beckman	79PR10K, Variable, 10k ohms ±10%, 3/4w
121-5020	Beckman	79PR5K, Variable, 5k ohms ±10%, 3/4w
123-5020	Spectrol	53-1-1-502, Variable, 5k ohms ±10%, 1/2w

Table 7-6

Part Number Cross Reference (continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No. * / Description
Dipped Mica Capacitors		
130-1005	(Comply with MIL-C-5)	10 pf ±5%, 500v dc
130-1015		100 pf ±5%, 500v dc
130-1515		150 pf ±5%, 500v dc
130-2205		22 pf ±5%, 500v dc
130-2215		220 pf ±5%, 500v dc
130-3305		33 pf ±5%, 500v dc
130-4705		47 pf ±5%, 500v dc
130-4715		470 pf ±5%, 500v dc
130-5605		56 pf ±5%, 500v dc
130-6805		68 pf ±5%, 500v dc
130-7515		750 pf ±5%, 500v dc
Mylar Film Capacitors		
131-1020	TRW	663uw series, .001μfd ±10%, 100v dc
131-1030	TRW	663uw series, .01μfd ±10%, 100v dc
131-1040	TRW	663uw series, .10μfd ±10%, 100v dc
131-2220	TRW	663uw series, .0022μfd ±10%, 100v dc
131-4720	TRW	663uw series, .0047μfd ±10%, 100v dc
Solid Tantalum Polarized Capacitors		
132-1062	Mallory	TIM106M010POW, 10μfd ±20%, 10v dc
132-2752	Mallory	TIM275M035POW, 2.7μfd ±20%, 35v dc
139-2244	Kemet	T310A225M020AS, 2.2μfd ±20%, 20v dc
139-2262	Kemet	T310B226M015AS, 22μfd ±20%, 15v dc
139-3352	Kemet	T310A335M015AS, 3.3μfd ±20%, 15v dc
Aluminum Foil Polarized Capacitor		
134-2680	Mallory	TOW282N025N1R3P, 2600μfd + 100% —10%, 20v dc
Ceramic Capacitors		
135-1002	Centralab	DD-102, .001μfg ±10%, 1000v dc
135-4742	Erie	8131-050651-474M, .47μfd ±20%, 50v dc
Transistors		
200-3053	RCA	2N3053, NPN, Silicon Annular, T0-5
200-3251	Motorola	2N3251, PNP, Switching, T0-18
200-4123	Motorola	2N4123, NPN, Silicon, T0-92
200-4125	Motorola	2N4125, PNP, Silicon, T0-92
200-4400	Motorola	2N4400, NPN, Silicon, T0-92
200-4402	Motorola	2N4402, PNP, Silicon, T0-92
200-5321	RCA	2N5321, NPN, Silicon, T0-5
200-5323	RCA	2N5323, PNP, Silicon, T0-5
200-6051	Motorola	2N6051, PNP, Power Darlington, T0-3
200-6058	Motorola	2N6058, NPN, Power Darlington, T0-3
200-6282	Motorola	2N6282, NPN, Power Darlington, T0-3
200-6285	Motorola	2N6285, PNP, Power Darlington, T0-3

Table 7-6

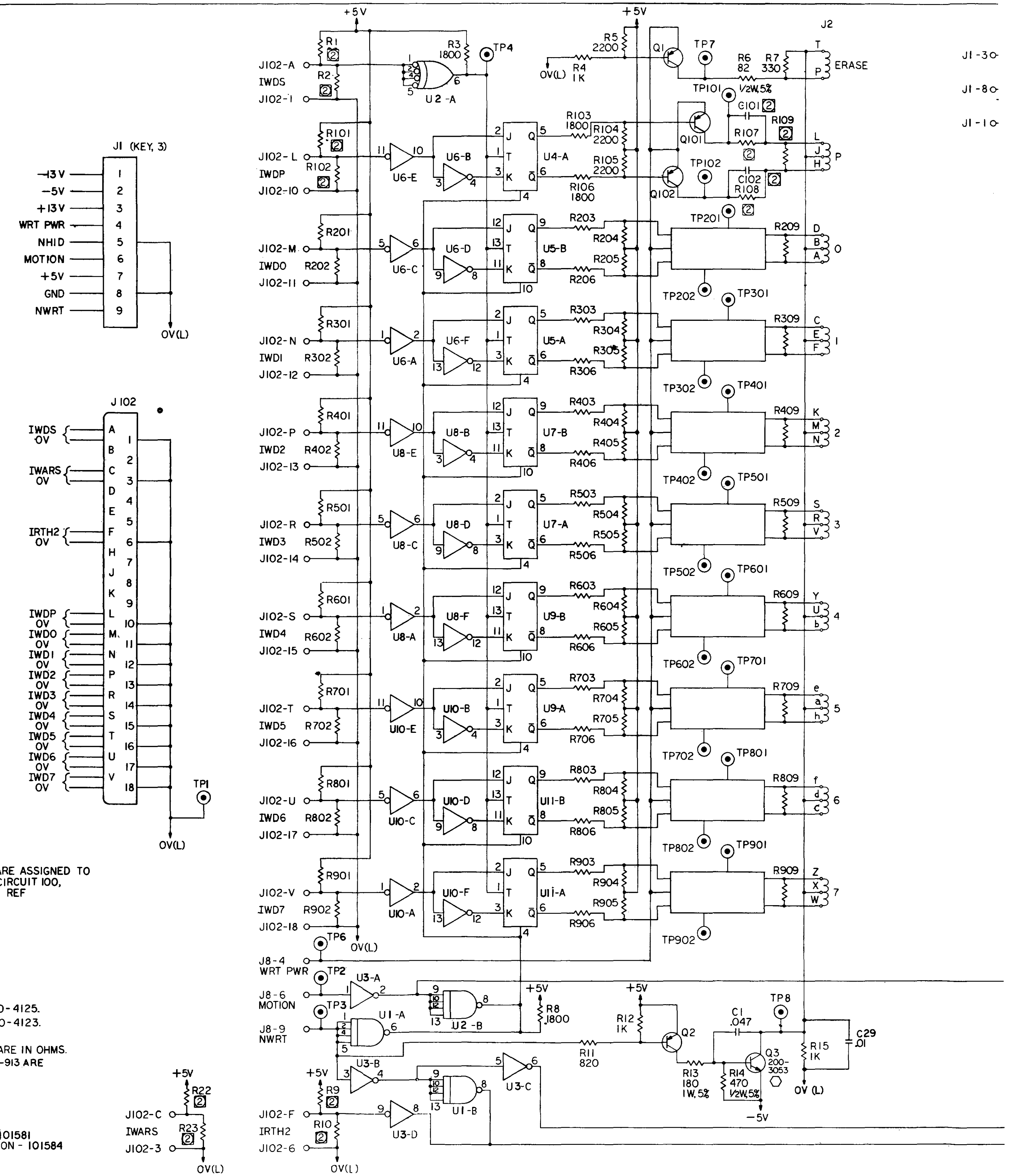
Part Number Cross Reference (continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Field Effect Transistors		
204-0074	National	TIS-74, N-Channel, Switching, T0-106
Diodes		
300-4002	Motorola	IN4002, Rectifier, 1A, 100 PIV, D0-41
300-4446	Components, Inc.	IN4446, Switching, 75PIV, D0-7
Zener Diodes		
300-0475	Motorola	IN4732A, Zener, 4.7v dc ±5%, 1w, D0-41
330-0515	Motorola	IN4733A, Zener, 5.1v dc ±5%, 1w, D0-41
330-1005	Motorola	IN4740A, Zener, 10v ±5%, 1w, D0-41
330-1205	Motorola	IN4742A, Zener, 12v ±5%, 1w
331-0275	Motorola	IN5223B, Zener, 2.7v dc ±5%, 500mw, D0-7
331-0395	Motorola	IN5228B, Zener, 3.9v dc ±5%, 500mw, D0-7
331-0515	Motorola	W5231B. Zener, 5.1v dc ±5% 500mw, D0-7
331-0605	Motorola	IN5233B, Zener, 6v dc ±5%, 500mw, D0-7
Light Emitting Diode		
301-0055	Optron	OR133W-3, Light Emitting, Infra Red, T0-46
Operational Amplifiers		
400-0307	National	LM307N, IC, Op Amp
400-0319	National	LM319N, IC, Dual Comparator
400-0592	Signetics	NE592A, IC, Op Amp
400-5558	National	LM1458N, IC, Dual Op Amp
Relays		
502-1205	Amer Zett	AZ-535-11-1, 12v dc, SPDT, Contract Rating 5A at 26v dc
502-1242	Allied Control	TF-154-4C-12v dc, 12v dc, 4PDT, Contact Rating 5A at 28v dc
Inductors		
515-1015	Delevan	1537-76, 100μH ±5%, 4.5 ohms
515-3305	Delevan	1537-52, 33μH ±5%, 2.9 ohms
515-6805	Delevan	1537-68, 68μH ±5%, 3.3 ohms
Crystals		
524-0002	Northern Eng Lab	NE12, 10.00 MHz ± .005

Table 7-7

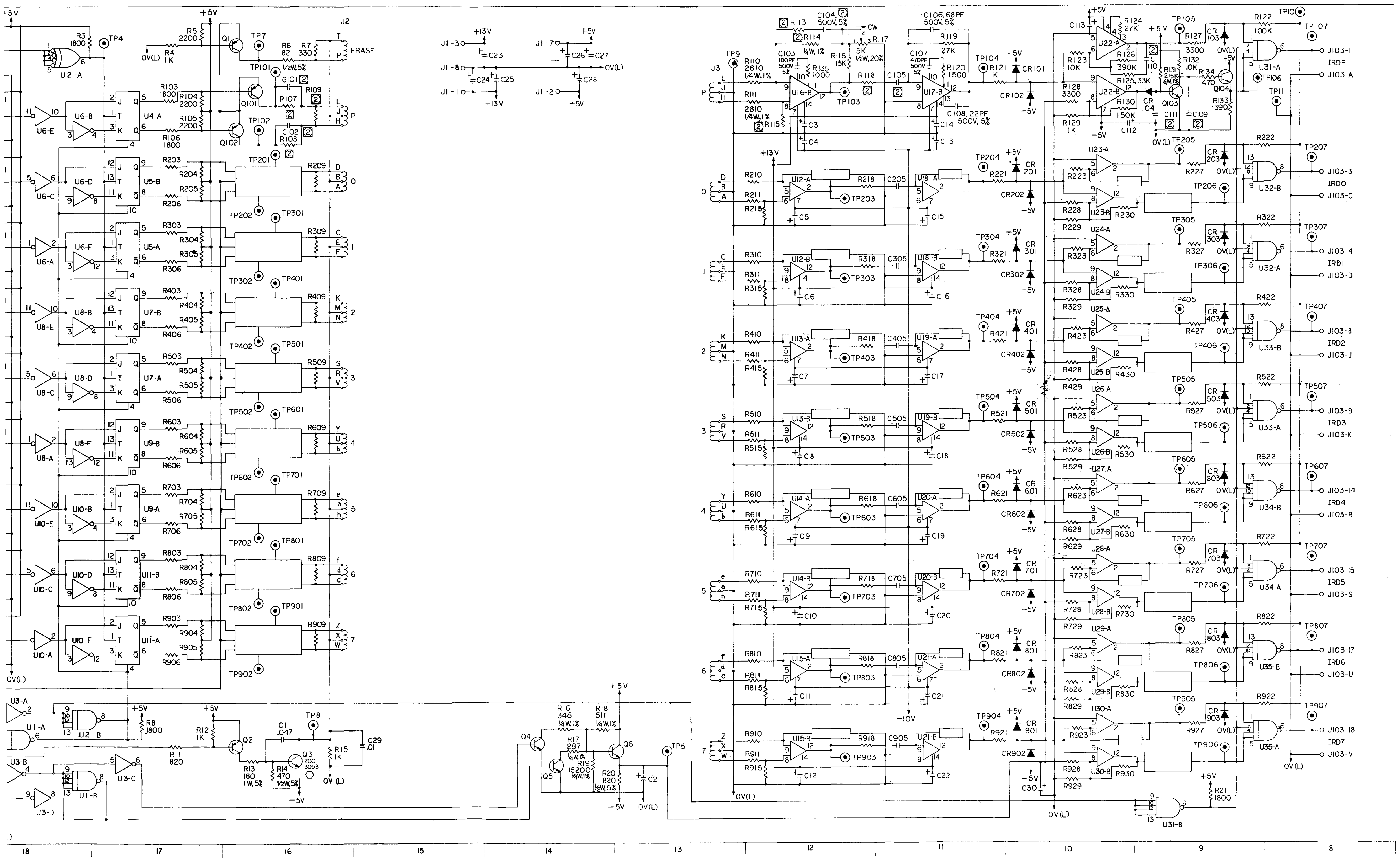
PCBA Interconnections

Tape Control PCBA	
J1	REWIND Control
J2	REVERSE Control
J3	FORWARD Control
J4	LOAD Control
J5	HI DEN/1600 CPI Indicator
J6	ON LINE Control
J7	WRT EN Indicator
J8	Limit Switch and WLO Switch
J9	Motors
J10	Power Supply
J11	Take-up Tension Arm Sensor
J12	Supply Tension Arm Sensor
J13	EOT/BOT Amplifier PCBA
J14	Data PCBA, J1
EOT/BOT Amplifier	
J1	Photo-tab Sensor
Data PCBA	
J2	Write and Erase Head
J3	Read Head

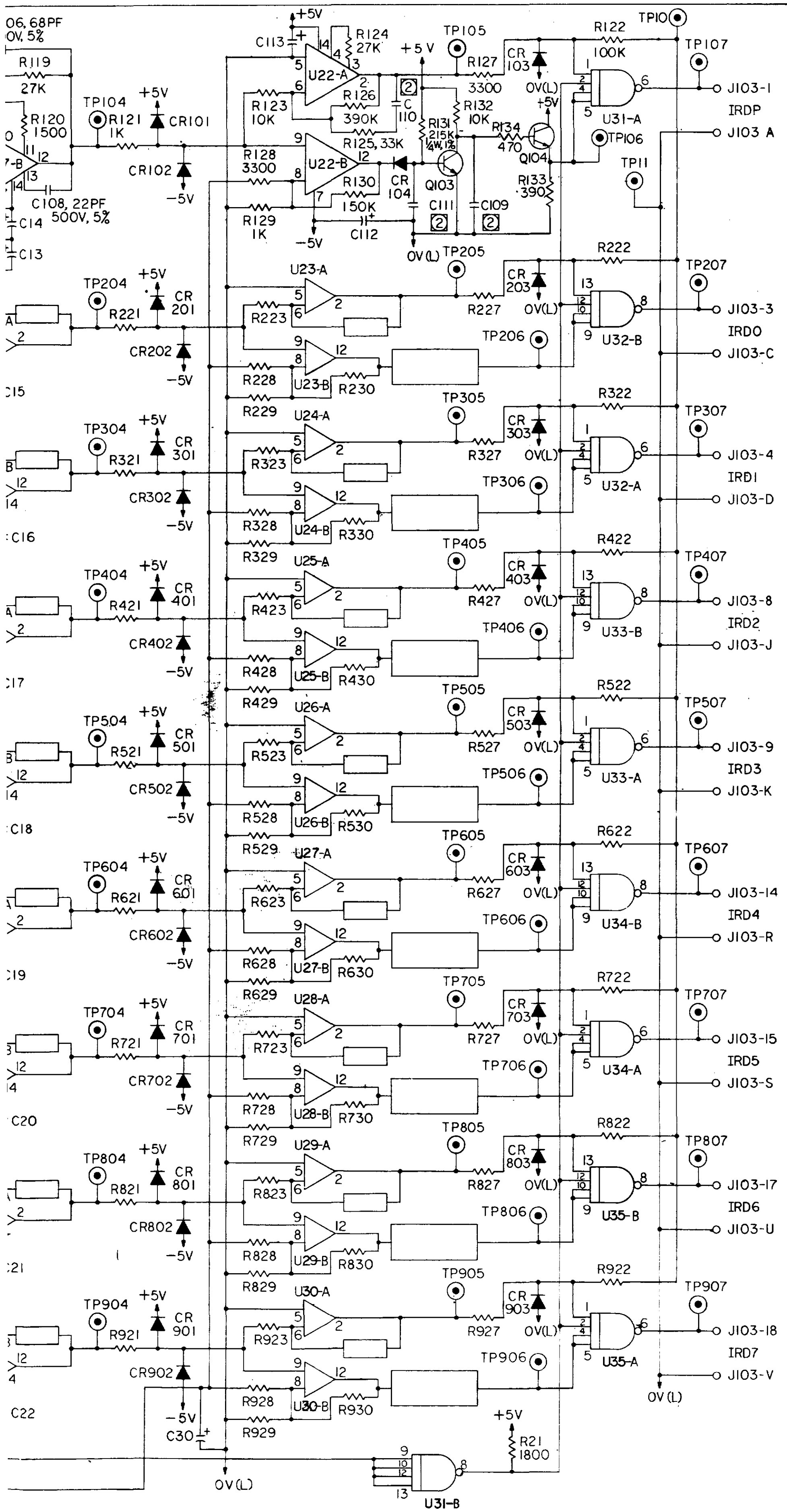


13. CIRCUIT 100 IS TYPICAL OF CIRCUITS 200 THRU 900.
12. 3 DIGIT REFERENCE DESIGNATIONS ARE ASSIGNED TO REPETITIVE CIRCUITS. EX: TP101 IS CIRCUIT 100, TP901 IS CIRCUIT 900. SINGLE DIGIT REF DESIGNATIONS ARE ASSIGNED TO NON REPETITIVE CIRCUITS. EX: TP1, TP2.
11. PIN 14 OF ALL IC'S IS +5V.
10. PIN 7 OF ALL IC'S IS OV(L).
9. INTEGRATED CIRCUITS:
U3,6,8,10 ARE PEC 700-8360.
U1,2, 31-35 ARE PEC 700-8440.
U4,5,7,9,11 ARE PEC 700-8530.
U12-30 ARE PEC 400-1437.
8. ALL PNP TRANSISTORS ARE PEC 200-4125.
7. ALL NPN TRANSISTORS ARE PEC 200-4123.
6. ALL DIODES ARE PEC 300-4446.
5. ALL RESISTORS ARE 1/4W, 5%, VALUES ARE IN OHMS.
4. CAPACITORS C2-28, C30, C112-912, C113-913 ARE 2.7UF, 35V, 20% ALL OTHERS ARE IN MICROFARADS, 100V, 10%.
3. ⬡ INDICATES TRANSISTOR MOUNTED HEATSINK.
2. SEE VERSION TABLE FOR VALUE.
1. REFERENCE DRAWINGS: ASSEMBLY - 101581
SPECIFICATION - 101584
NOTES: UNLESS OTHERWISE SPECIFIED:

21 | 20 | 19 | 18 | 17 | 16 | 15



ERASE
J2
J3
TP4
TP5
TP7
TP8
TP9
TP10
TP11
TP101
TP102
TP103
TP104
TP105
TP106
TP107
U2-A
U2-B
U4-A
U6-E
U6-B
U6-C
U6-D
U6-A
U6-F
Q1
Q2
Q3
Q4
Q5
Q6
Q101
Q102
Q103
Q104
U16-B
U17-B
U22-A
U22-B
U31-A
U31-B
J103-1
IRDP
J103 A
J103-3
IRD0
J103-C
J103-4
IRD1
J103-D
J103-8
IRD2
J103-J
J103-9
IRD3
J103-K
J103-14
IRD4
J103-R
J103-15
IRD5
J103-S
J103-17
IRD6
J103-U
J103-18
IRD7
J103-V
J1-3
J1-8
J1-1
J1-7
J1-2
C23
C24
C25
C26
C27
C28
+13V
-13V
+5V
-5V
-10V
OV(L)
C104 500V, 5%
C106, 68PF 500V, 5%
R116 15K
5K 1/2W, 20% R117
CW
R1 100K
R124 27K
R126 390K
R125, 33K
R130 150K
R128 3300
R129 1K
R123 10K
R127 3300
R132 10K
R134 470
R133 390
R131 215K 1/4W,1%
C108, 22PF 500V, 5%
C107 470PF 500V 5%
C103 100PF 500V 5%
R110 2610 1/4W,1%
R111 2610 1/4W,1%
R135 1000
R119 27K
R120 1500
R121 1K
CR101
CR102
R3 1800
R4 1K
R5 2200
R6 82
R7 330
R8 1800
R11 820
R12 1K
R13 180 1W, 5%
R14 470 1/2W,5%
R15 1K
C1 .047
C29 .01
R16 348 1/4W,1%
R17 287 1/4W,1%
R18 511 1/4W,1%
R19 16200 1/4W,1%
R20 820 1/2W,5%
C2
R21 1800
C30
U1-A
U1-B
U3-A
U3-B
U3-C
U3-D
18
17
16
15
14
13
12
11
10
9
8



VERSION TABLE

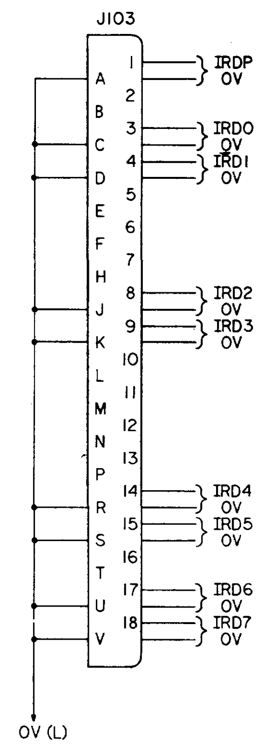
VERSION	SPEED (IPS)	——		R118—918 1/4W, 5%	C104—904 500V, 5%	R113—913 1/4W, 5%	R114—914 R115—915 1/4W, 1%	C101—901 C102—902 100V 10%	C105—905 100V, 10%	C109—909 100V, 10%	C110—910 500V, 5%	C111—911 500V, 5%	R109—909 1/4W, 5%	R107—907 R108—908 1/2W, 5%	R1,9,22, 101-901 1/4W, 5%	R2,10,23 102-902 1/4W 5%
-01	12.5			1000	68PF	2200	31,600	OMIT	.0033UF	.033UF	68PF	470PF	680	270	220	330
-02	18.75			1200	47PF	3300	31,600	.0068	.0022UF	.01UF	47PF	470PF	1000	390	220	330
-03	25			1200	33PF	2200	23,700	.0047	.0015UF	.01UF	33PF	330PF	1500	390	220	330
-04	12.5			1000	68PF	2200	31,600	OMIT	.0033UF	.033UF	68PF	470PF	680	270	OMIT	OMIT
-05	18.75			1200	47PF	3300	31,600	.0068	.0022UF	.01UF	47PF	470PF	1000	390	OMIT	OMIT
-06	25			1200	33PF	2200	23,700	.0047	.0015UF	.01UF	33PF	330PF	1500	390	OMIT	OMIT

REVISIONS

REV	DESCRIPTION
B	ERN 2-WQ
C	ECN 2571
D	ECN 2709
E	ECN 3497A
F	ECN 4716
G	ECN 4839
H	ECN 6164
J	ECN 6225
K	ECN 9331
L	ECN 11211

REFERENCE DESIGNATION

LAST USED		DELETED
C30	C913	R112-R912
	CR904	
Q6	Q904	
R23	R935	
U35		
TP11	TP907	
	W901	W101-901



PEC PERIPHERAL EQUIPMENT CORPORATION

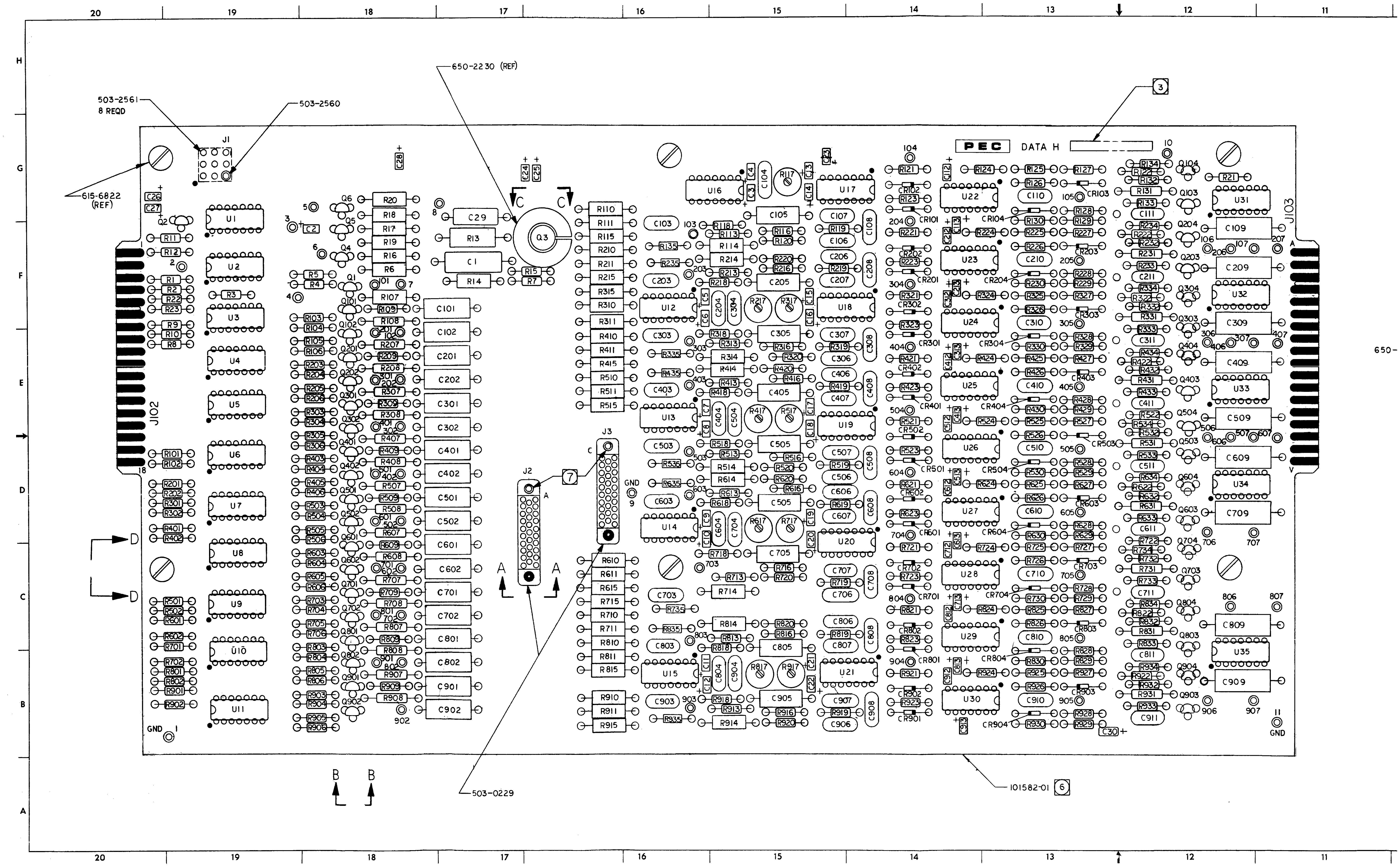
TITLE SCHEMATIC DATA 'H' READ WHILE WRITE

SIZE J | DWG NO. 101580 | REV L

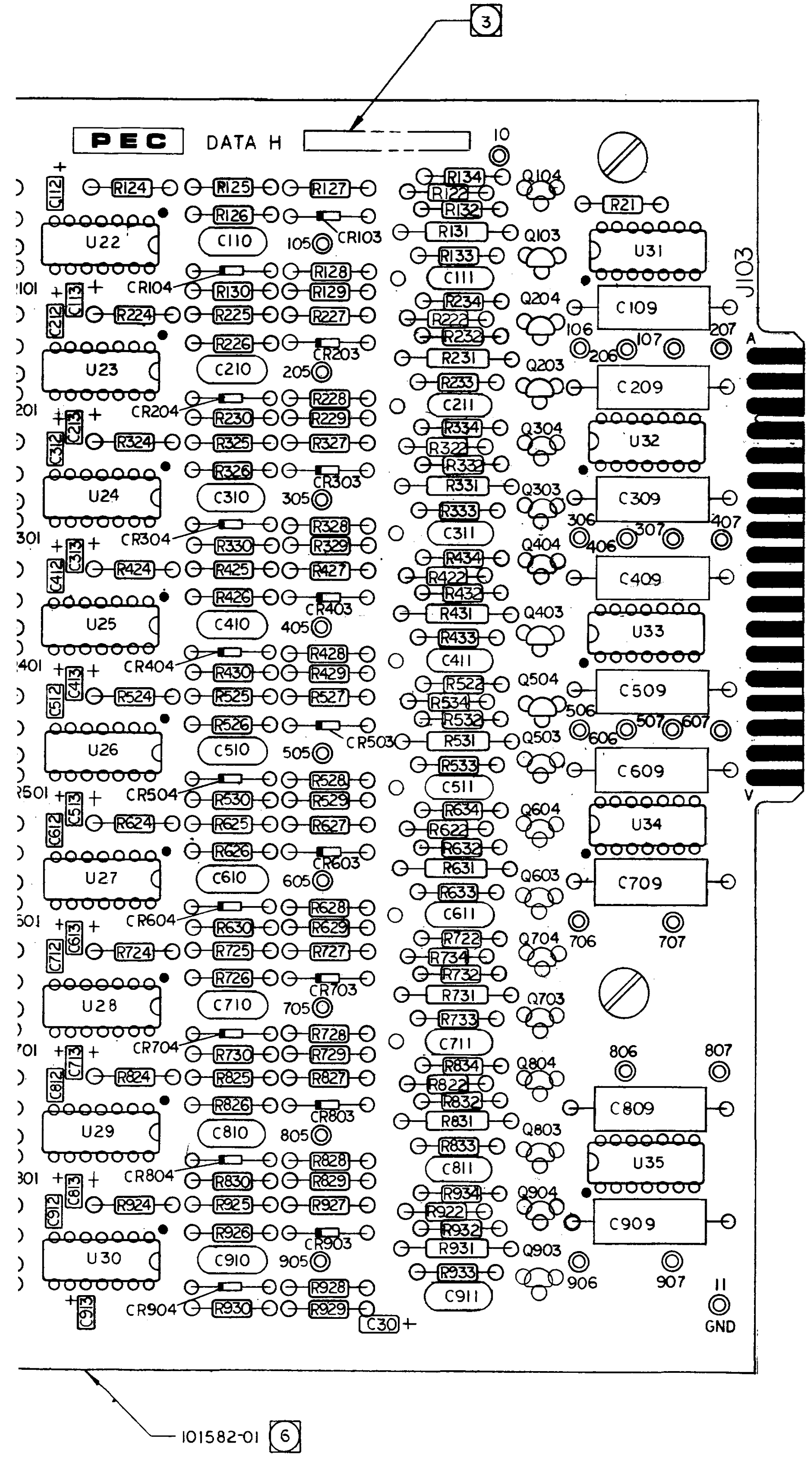
101581 NEXT ASSY | 1ST USED ON | APPLICATION

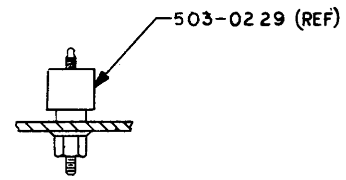
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH: | MATL: | SCALE | DO NOT SCALE DWG | SHEET 1 OF 1

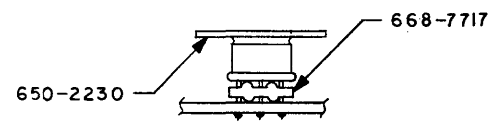


650-2230 (REF)
503-2561
8 REQD
503-2560
615-6822
(REF)
J1
J2
J3
J102
J103
PEC
DATA H
503-0229
101582-01
650-
GND

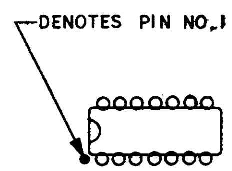




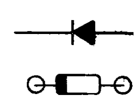
SECTION A-A
MTG DETAIL
FOR J2 AND J3



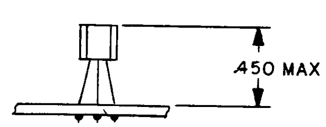
VIEW C-C
TO-5 MTG CONFIGURATION
ROTATED 180°



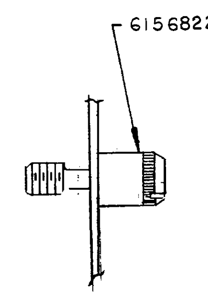
I C ORIENTATION



DIODE ORIENTATION



VIEW B-B
TYP TRANSISTOR MTG HEIGHT (TO 92)



VIEW D-D
TYP 6 PLACES

4 TABLE I

PART NO.	REF DESIGNATION
100-1025	R121-921, 129-929, 4, 12, 15, 135-935
100-1035	R123-923, 132-932
100-1045	R122-922
100-1545	R130-930
100-1825	R103-903, 106-906, 3, 8, 21
100-2225	R104-904, 105-905, 5
100-1525	R120-920
100-3315	R7
100-3325	R127-927, 128-928
100-3335	R125-925
100-3915	R133-933
100-1535	R116-916
100-3945	R126-926•
100-4715	R134-934
100-8215	R11
100-2735	R124-924, 119-919
101-4715	R14
101-8205	R6
101-8215	R20
102-1815	R13
104-1622	R19
104-2611	R110-910, 111-911
104-2870	R17
104-3480	R16
104-2153	R131-931
104-5110	R18

TABLE I CONTINUED

PART NO.	REF DESIGNATION
123-5020	R117-917
130-1015	C103-903
130-4715	C107-907
130-2205	C108-908
130-6805	C106-906
131-1030	C29
131-4730	C1
132-2752	C2-28, C112-912, 113-913, 30
200-3053	Q3
200-4123	Q103-903, 104-904, 4-6
200-4125	Q101-901, 102-902, 1, 2
300-4446	CR101-901, 102-902,
	103-903, 104-904
400-1437	U12-30
700-8360	U3, 6, 8, 10
700-8440	U1, 2, 31-35
700-8530	U4, 5, 7, 9, 11

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS			
IPS	12.5	18.75	25	12.5
VER	-01	-02	-03	-04
R113-913	100-2225	100-3325	100-2225	100-22
R109-909	100-6815	100-1020	100-1525	100-68
R114-914, 115-915	104-3162	104-3162	104-2372	104-31
C111-911	130-4715	130-4715	130-3315	130-47
C110-910	130-6805	130-4705	130-3305	130-68
C101-901, 102-902	OMIT	131-6820	131-4720	OMI
C109-909	131-3330	131-1030	131-1030	131-33
C105-905	131-3320	131-2220	131-1520	131-33
R107-907, 108-908	101-2715	101-3915	101-3915	101-27
R118-918	100-1025	100-1225	100-1225	100-10
C104-904	130-6805	130-4705	130-3305	130-68
R1, 9, 22, 101-901	100-2215	100-2215	100-2215	OMI
R2, 10, 23, 102-902	100-3315	100-3315	100-3315	OMI

NOTES: UNLESS OTHERWISE SPECIFIED:

1. REF DWG: SCHEMATIC - 101580
   SPECIFICATION - 101584
2. ASSEMBLE PER STANDARD MFG METHODS.
3. RUBBER STAMP ASSY PART NO. INCLUDING VERSION AND ISSUE LETTER.
4. FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.
5. FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.
6. THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101582-01 REV 'C' AND SUBSEQUENT.
7. ORIENTATE CONNECTORS J2 AND J3 AS SHOWN.

TOP ASSY	7
NEXT ASSY	1
APPLICATI	

TABLE I CONTINUED

PART NO.	REF DESIGNATION
123-5020	R117-917
130-1015	C103-903
130-4715	C107-907
130-2205	C108-908
130-6805	C106-906
131-1030	C29
131-4730	C1
132-2752	C2,-28, C112-912, 113-913, 30
200-3053	Q3
200-4123	Q103-903, 104-904, 4-6
200-4125	Q101-901, 102-902, 1, 2
300-4446	CR101-901, 102-902,
	103-903, 104-904
400-1437	U12-30
700-8360	U3, 6, 8, 10
700-8440	U1, 2, 31-35
700-8530	U4, 5, 7, 9, 11

(5) TABLE II

REFERENCE DESIGNATION	PART NUMBERS					
IPS	12.5	18.75	25	12.5	18.75	25
VER	-01	-02	-03	-04	-05	-06
R113-913	100-2225	100-3325	100-2225	100-2225	100-3325	100-2225
R109-909	100-6815	100-1020	100-1525	100-6815	100-1020	100-1525
R114-914, 115-915	104-3162	104-3162	104-2372	104-3162	104-3162	104-2372
C111-911	130-4715	130-4715	130-3315	130-4715	130-4715	130-3315
C110-910	130-6805	130-4705	130-3305	130-6805	130-4705	130-3305
C101-901, 102-902	OMIT	131-6820	131-4720	OMIT	131-6820	131-4720
C109-909	131-3330	131-1030	131-1030	131-3330	131-1030	131-1030
C105-905	131-3320	131-2220	131-1520	131-3320	131-2220	131-1520
R107-907, 108-908	101-2715	101-3915	101-3915	101-2715	101-3915	101-3915
R118-918	100-1025	100-1225	100-1225	100-1025	100-1225	100-1225
C104-904	130-6805	130-4705	130-3305	130-6805	130-4705	130-3305
R1, 9, 22, 101-901	100-2215	100-2215	100-2215	OMIT	OMIT	OMIT
R2, 10, 23, 102-902	100-3315	100-3316	100-3315	OMIT	OMIT	OMIT

REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 2-WQ	11/13/70	[illegible]	[illegible]	[illegible]
B	ECN 2572	5/11/71	C.J.	[illegible]	[illegible]
C	ECN 2709	[illegible] 26-71	[illegible]	[illegible]	[illegible]
D	ECN 3497A	4/14/72	[illegible]	L.B.	[illegible]
E	ECN 3786	[illegible]	RAS	[illegible]	[illegible]
F	ECN 4716	12-20-72	[illegible]	JBR	RCA
G	ECN 4839	1/17/73	[illegible]	JBR	RCA
H	ECN 6164	3/22/74	RAS	JBR	[illegible]
J	ECN 6225	4/17/74	[illegible]	[illegible]	[illegible]
K	ECN 9331	12/15/76	[illegible]	[illegible]	[illegible]
L	ECN 11211	3/22/78	J.S.	[illegible]	[illegible]

(7) ORIENTATE CONNECTORS J2 AND J3 AS SHOWN.

(6) THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101582-01 REV 'C' AND SUBSEQUENT.

(5) FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.

(4) FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

(3) RUBBER STAMP ASSY PART NO. INCLUDING VERSION AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MFG METHODS.

1. REF DWG: SCHEMATIC - 101580
   SPECIFICATION - 101584

NOTES: UNLESS OTHERWISE SPECIFIED:

PART NO. 101581-06 REV B

TOP ASSY	7000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
$\frac{X}{X} \pm \frac{1}{32}$
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. 010

FINISH:

SIGNATURES	DATE
DR [illegible]	[illegible]
CHK [illegible]	10/29/70
DES [illegible]	11/13/70
ENGR [illegible]	11/13/70
ENGR [illegible]	11/16/70

MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA DATA-H READ WHILE WRITE

SIZE	CODE IDENT. NO.	DWG NO.	REV
E		101581	L
SCALE 2:1		DO NOT SCALE DWG	SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-YZ PRE PROD RELEASE	[illegible]	[illegible]	[illegible]	[illegible]
B	ECN 9711	[illegible]	[illegible]	[illegible]	[illegible]
C	ECN 9893A	[illegible]	[illegible]	[illegible]	[illegible]
	ERN 9-NZ PROD RELEASE	[illegible]	[illegible]	[illegible]	[illegible]
D	ECN 9949	6/8/77	[illegible]	[illegible]	[illegible]
E	ECN 10243	[illegible]	[illegible]	[illegible]	[illegible]
F	ECN 10874	[illegible]	[illegible]	[illegible]	[illegible]
G	ECN 11134	[illegible]	[illegible]	[illegible]	[illegible]

(1) TABLE I

PART NO.	REFERENCE DESIGNATION
100-1015	R1
101-8205	R2
120-0001	U10, 94, 173, 214
120-0003	U186
132-2752	C4, 5, 7, 8, 11, 12, 14, 17, 18, 20, 21, 22, 25, 26, 29, 30, C32 THRU 47, 50, 51
135-1002	C31
402-1115	U181
514-0009	U112, 187
700-7404	U134, 251
700-7416	U91, 111, 151, 190, 210
700-7433	U69, 109, 169, 233, 267
700-7438	U92, 113, 132, 253
710-4151	U228, 268, 269, 270, 288
710-4163	U184, 185, 230, 248, 249, 250, 289, 290
710-4174	U34, 41, 49, 101, 149, 161, 172, 188, 192, 204, 209, U212, 229, 273, 274, 284
710-4175	U152, 272
710-4280	U193
710-7400	U182, 207, 232, 252, 254, 286
710-7402	U266, 90
710-7404	U50, 222
710-7408	U263
710-7410	U227
710-7411	U110, 133, 154
710-7414	U9, 93, 114, 130, 153, 174, 194, 213
710-7432	U245
710-7474	U183
710-7476	U208
710-7486	U150, 189, 234
107651-03	U291
107651-04	U293
107651-05	U292
107651-06	U294
107651-07	U170, 171
107651-08	U191
107651-09	U211
107651-10	U231

(3) TABLE III

PART NO.	REFERENCE DESIGNATION
100-1025	R9
100-1535	R7
100-2225	R6
100-6815	R4
107-4220	R8
107-6810	R5
124-1021	R3
130-4715	C48
132-2752	C1, 2, 3, 6, 9, 10, 13, 15, 16, 19, 23, 24, 27, 28,
139-4755	C49
200-4123	Q1, 2, 3
200-4125	Q4
700-4040	U223
700-7400	U262
700-7404	U244
710-4153	U7, 27, 47, 67, 87, 107, 128, 147, 167
710-4161	U242, 243
710-4163	U8, 13, 14, 28, 31, 48, 68, 88, 108, 129, 148, 168, 201, U221, 241
710-4164	U264
710-4174	U6, 26, 46, 66, 86, 106, 127, 146, 166
710-4280	U51, 202
710-7400	U265
710-7402	U71, 287
710-7404	U247
710-7408	U225
710-7410	U226, 285
710-7411	U4, 24, 44, 64, 84, 104, 125, 144, 164, 203, 224, 246
710-7427	U1, 61, 122
710-7430	U70, 72
710-7432	U11, 205
710-7476	U30, 52, 53, 54, 73, 74
710-7486	U29, 89
710-7495	U2, 22, 42, 62, 82, 102, 123, 142, 162
710-7496	U3, 23, 43, 63, 83, 103, 124, 143, 163
103983-03	U33
107649-01	U283
107649-02	U12
107650-01	U206
107651-01	U5, 25, 45, 65, 85, 105, 126, 145, 165
107651-02	U21, 81, 141

(2) TABLE II

ASSEMBLY 107605 VERSION NO.	VERSION CHARACTER-ISTIC	W1, 3	W2, 4	U11 THRU 14, 30, 31, 33, U51 THRU 54, 70 THRU 74	C1, 2, 3, 6, 9, 10, 13, 15, 16, 19, 23, 24, 27, 28, 48, 49 R3 THRU 9 Q1 THRU 4 U1 THRU 8, 21 THRU 29, 42 THRU 48, 61 THRU 68, 81 THRU 89, 102 THRU 108, 122 THRU 129, 141 THRU 148, U162 THRU 168, 201, 202, 203, 205, 206, 221, 223 THRU 226, 241 THRU 244, 246, 247, 262, 264, 265, 283, 285, 287
		100-0005	100-0005	USAGE (3)	USAGE (3)
-01	PE AND NRZI	OMIT	OMIT	USE	USE
-02	PE ONLY	OMIT	USE	OMIT	USE
-03	NRZI ONLY	USE	OMIT	USE	OMIT

TABLE VII

(13) OPTION CONFIGURATIONS

FUNCTION		U112 SWITCHES OPEN	U112-SWITCHES CLOSED
PARITY	INTERNAL	S1	S2
	EXTERNAL	S2	S1
FMTR ADDRESS	ZERO	S4	S3
	ONE	S3	S4
FORMAT	PE - NOT DAISY CHAIN		S5
	ALL OTHERS	S5	
HEAD	SINGLE - NOT DAISY CHAIN		S6
	ALL OTHERS	S6	

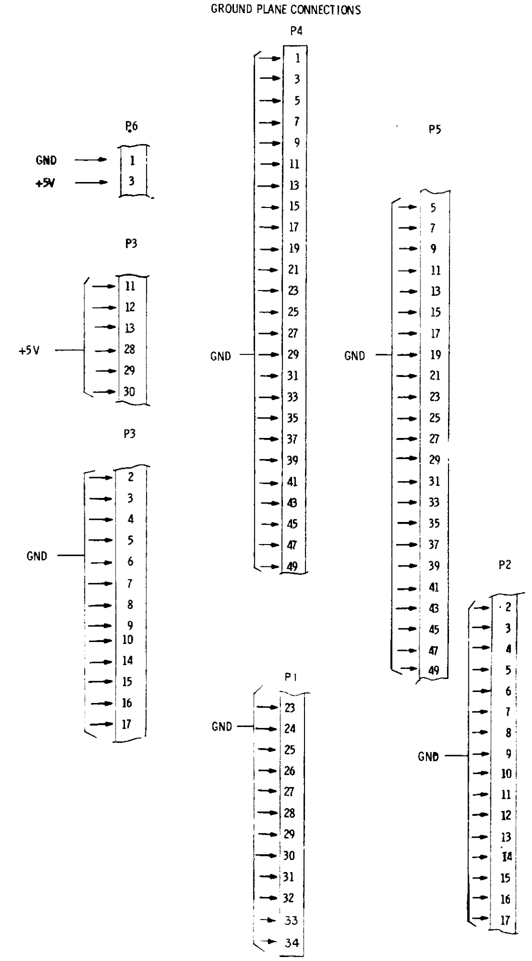
TABLE VI

(12) SPEED CONFIGURATIONS

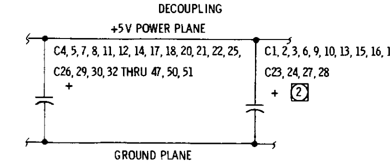
SPEED (IPS)	U187-SWITCHES OPEN	U187-SWITCHES CLOSED	FOR PE INSTALL 107609-XX IN U282 (11)
12.5	S1, S2, S3, S6, S8	S4, S5, S7	-01
18.75	S1, S3, S7, S8	S2, S4, S5, S6	-02
25	S3, S5, S7, S8	S1, S2, S4, S6	-04
37.5	S1, S2, S6, S7, S8	S3, S4, S5	-05
45	S4, S6, S7, S8	S1, S2, S3, S5	-06
75	S2, S5, S6, S7, S8	S1, S3, S4	-07
112.5	S1, S2, S3, S5, S6, S7, S8	S4	-08
125	S4, S5, S6, S7, S8	S1, S2, S3	-09

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	DELETED
C51		
R9		
Q4		
U294	10	
W4		

GROUND PLANE CONNECTIONS



DECOUPLING



(5) TABLE IV

TYPE	REFERENCE DESIGNATION
7433	U169B, U169C, U169D, U233A, U233C, U233D
74LS00	U207A, U232D, U252C, U286C
74LS02	U71B, U266C
74LS08	U225D, U263B
74LS10	U226B
74LS11	U110A, U110B, U154A, U154D, U246A, U246D
74LS14	U194B
7416	U91B, U111C, U190A, U210A, U210B
74LS86	U234C, U234D
120-0003	U186B, C, D, E, F
74LS32	U245B

(9) TABLE V

TYPE	FUNCTIONAL DESCRIPTION
74LS95	4-BIT SHIFT REGISTER
74LS96	5-BIT SHIFT REGISTER
74LS151	8-TO-1 DATA SELECTOR
74LS153	DUAL 4-TO-1 DATA SELECTOR
74LS161	4 BIT CNTR/SYNCHRONOUS CLR
74LS163	4 BIT CNTR/SYNCHRONOUS CLEAR
74LS164	8-BIT SHIFT REGISTER
74LS174	6-BIT D TYPE FLIP FLOP
74LS280	9-BIT PARITY GENERATOR

(14) "T" OR "C" SUFFIX ON MNEMONIC IS FOR REFERENCE ONLY.

(13) SEE TABLE VII FOR OPTION CONFIGURATIONS.

(12) SEE TABLE VI FOR SPEED CONFIGURATIONS.

(11) PLUG ASSY 107609-XX IS SPECIFIED AT TOP ASSEMBLY.

(10) REFERENCE DESIGNATIONS NOT USED: U15, 16, 17, 18, 19, 20, 32, 35, 36, 37, 38, 39, 40, 55, 56, 57, 58, U59, 60, 75, 76, 77, 78, 79, 80, 95, 96, 97, 98, 99, 100, 115, 116, 117, 118, 119, 120, 121, 131, 135, 136, 137, U138, 139, 140, 155, 156, 157, 158, 159, 160, 175, 176, 177, 178, 179, 180, 195, 196, 197, 198, 199, 200, 215, U216, 217, 218, 219, 220, 235, 236, 237, 238, 239, 240, 255, 256, 257, 258, 259, 260, 261, 271, 275, 276, 277, U278, 279, 280, 281.

(9) FOR I. C. FUNCTIONAL DESCRIPTION, SEE TABLE V.

8. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING WITH THE ASSOCIATED LOGIC TERM MNEMONIC. THE NO. SHOWN IS THE SHEET NO.

7. CAPACITOR VALUES ARE 2.7 MICROFARADS, 20%, 35V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

(5) FOR SPARE LOGIC ELEMENTS SEE TABLE IV.

4. ON 14 PIN I. C.'s PIN 7 IS GND AND PIN 14 IS +5V, ON 16 PIN I, C.'s PIN 8 IS GND AND PIN 16 IS +5V.

(3) FOR PART NUMBER, SEE TABLE III.

(2) FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II.

(1) FOR PART NUMBER OF COMPONENTS NOT AFFECTED RY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY NO. 107605
SPECIFICATION NO.

REFERENCE DRAWINGS

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	FIN.	REF. DES.	ITEM NO

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
X/X ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. T. MORTON	9/29/76
CHK [illegible]	[illegible]
DES	
ENGR	
PROJ. ENGR [illegible]	[illegible]

PERTEC PERIPHERAL EQUIPMENT

TITLE SCHEMATIC, MICROFORMATTER BOARD

107605	FT7XXX
NEXT ASSY	1ST USED ON
APPLICATION	

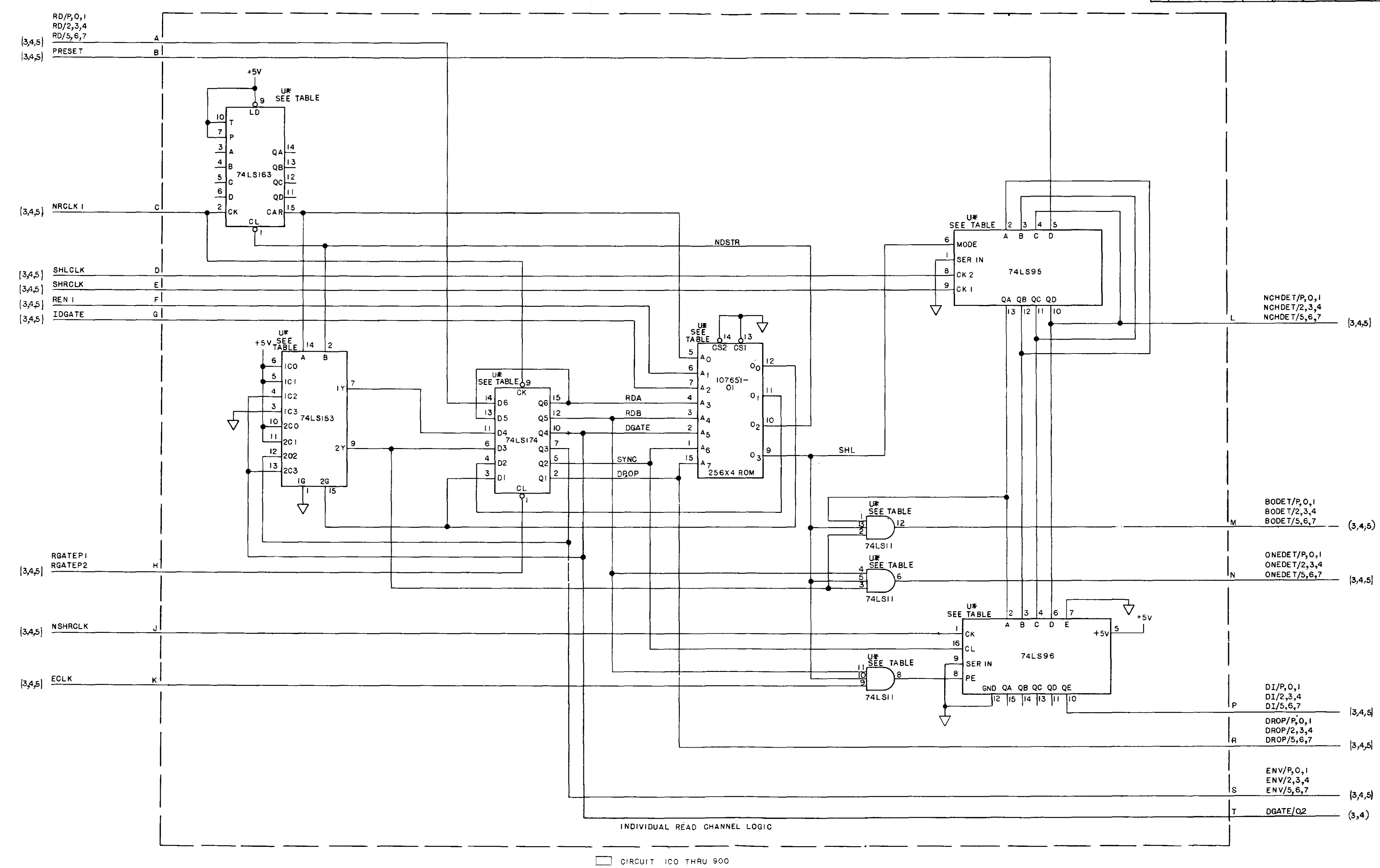
FINISH:

MATL:

SIZE E | CODE IDENT NO. | DWG NO. 107604 | REV G

SCALE —— | DO NOT SCALE DWG | SHEET 1 OF 15

REF. DESIGNATION TABLE [2]									
	INDIVIDUAL READ CHANNEL								
IC TYPE	P	0	1	2	3	4	5	6	7
74LS95	U2	U22	U42	U62	U82	U102	U123	U142	U162
74LS96	U3	U23	U43	U63	U83	U103	U124	U143	U163
74LS11	U4	U24	U44	U64	U84	U104	U125	U144	U164
107651-01	U5	U25	U45	U65	U85	U105	U126	U145	U165
74LS174	U6	U26	U46	U66	U86	U106	U127	U146	U166
74LS153	U7	U27	U47	U67	U87	U107	U128	U147	U167
74LS163	U8	U28	U48	U68	U88	U108	U129	U148	U168

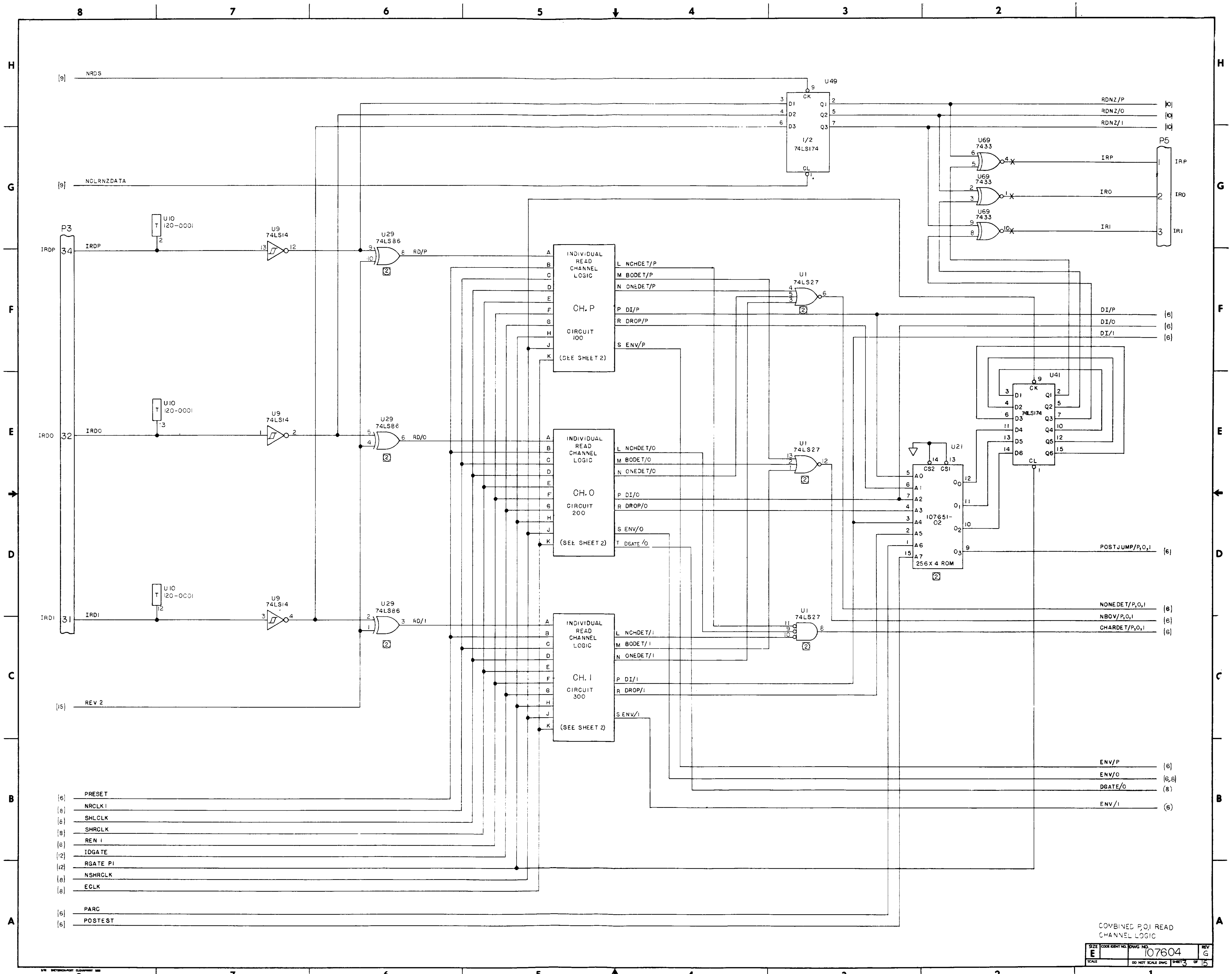


CIRCUIT 100 THRU 900

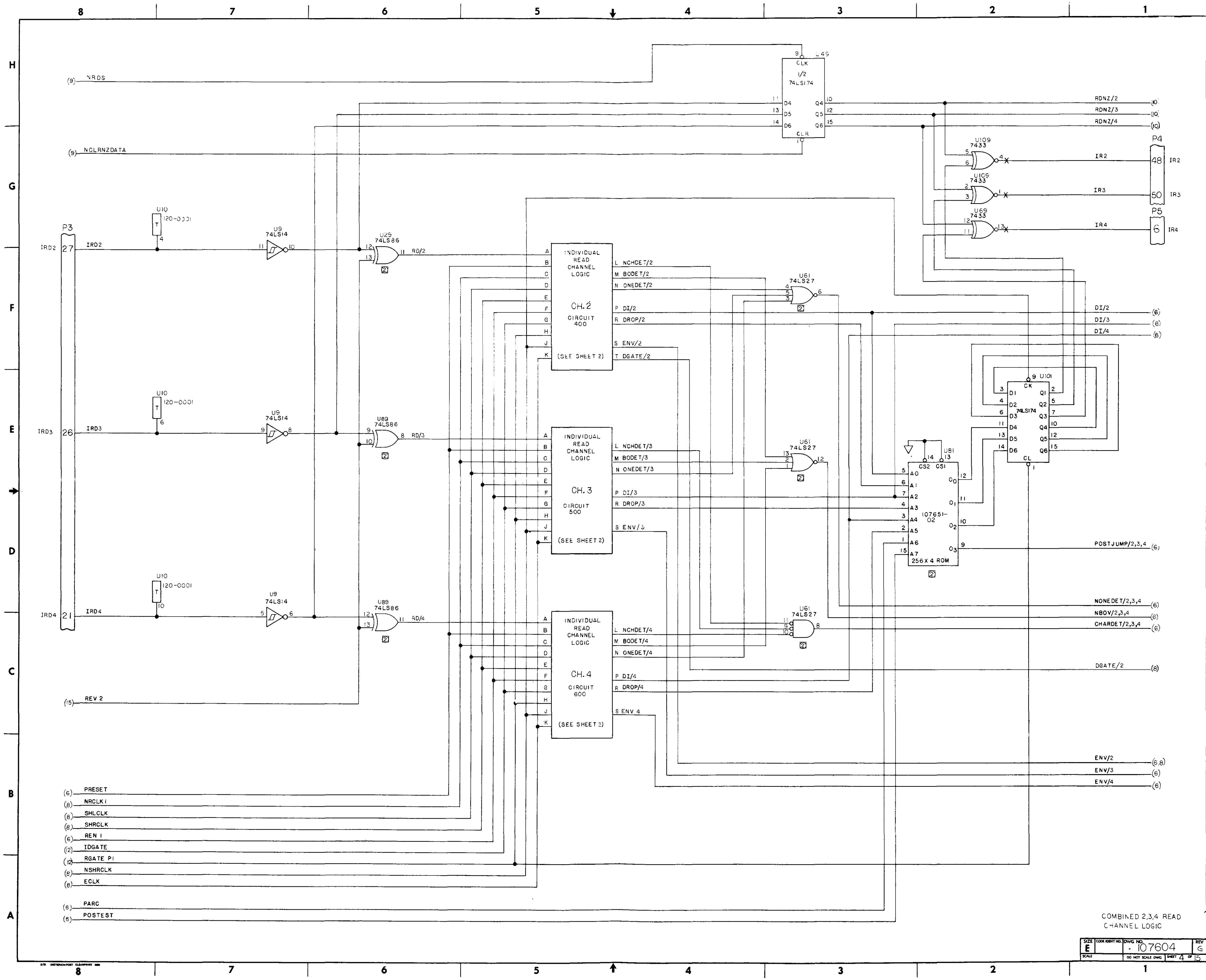
INDIVIDUAL READ CHANNEL LOGIC

SIZE	DWG NO.	REV
E	107604	G

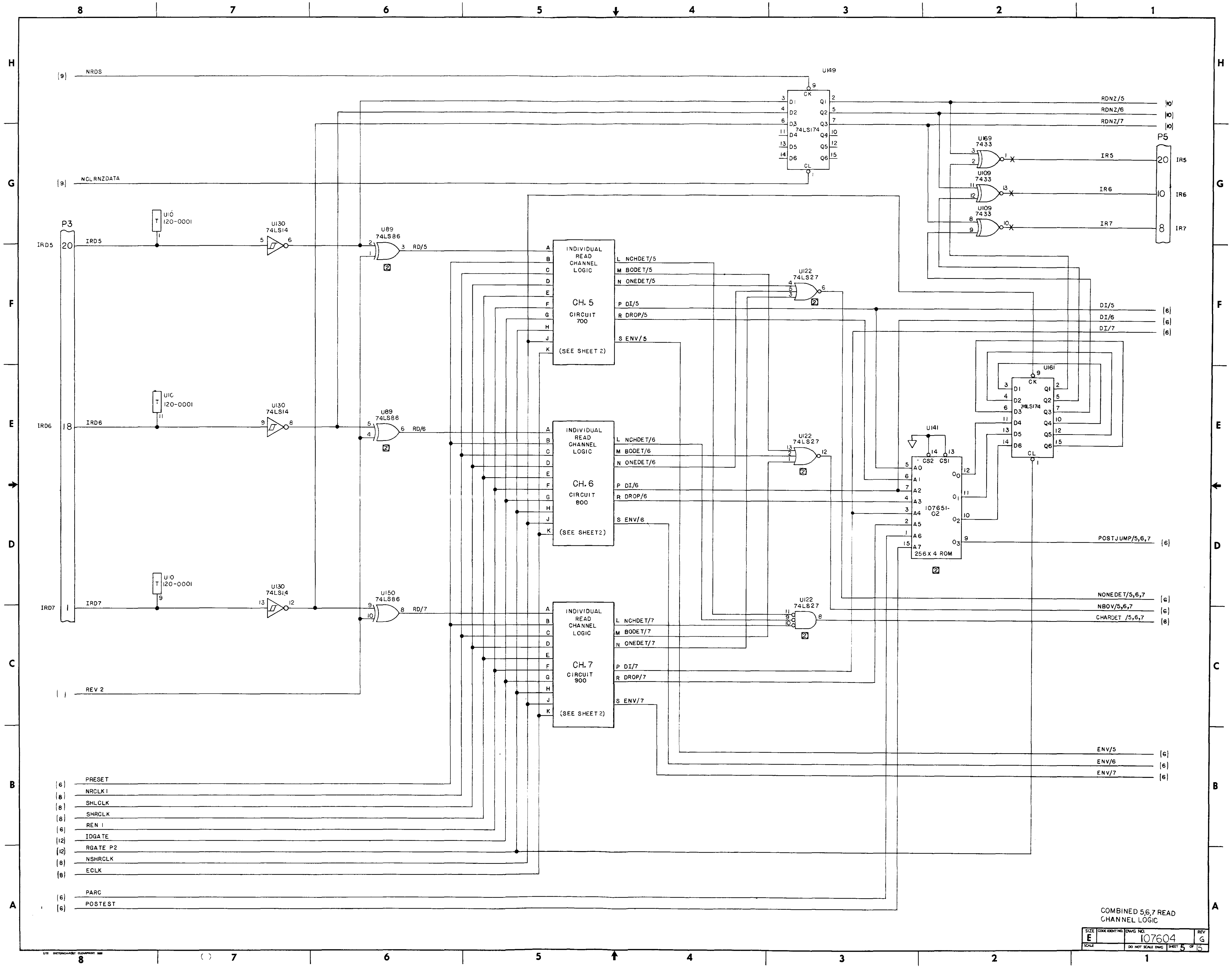
SHEET 2 OF 5



NRDS
NCLRNZDATA
U49
1/2 74LS174
RDNZ/P
RDNZ/O
RDNZ/I
U69 7433
P5
IRP
IRO
IRI
P3
IRDP
IRDO
IRDI
U10 120-0001
U9 74LS14
U29 74LS86
RD/P
RD/O
RD/I
REV 2
INDIVIDUAL READ CHANNEL LOGIC
CH. P
CIRCUIT 100
CH. O
CIRCUIT 200
CH. I
CIRCUIT 300
(SEE SHEET 2)
NCHDET/P
BODET/P
ONEDET/P
DI/P
DROP/P
ENV/P
NCHDET/O
BODET/O
ONEDET/O
DI/O
DROP/O
ENV/O
DGATE/O
NCHDET/I
BODET/I
ONEDET/I
DI/I
DROP/I
ENV/I
U1 74LS27
U41 74LS174
U21
107651-02
256 X 4 ROM
POSTJUMP/P,O,I
NONEDET/P,O,I
NBOV/P,O,I
CHARDET/P,O,I
PRESET
NRCLKI
SHLCLK
SHRCLK
REN I
IDGATE
RGATE PI
NSHRCLK
ECLK
PARC
POSTEST
COMBINED P,O,I READ CHANNEL LOGIC
SIZE E
DWG NO. 107604
REV G
DO NOT SCALE DWG.
SHEET 3 OF 5



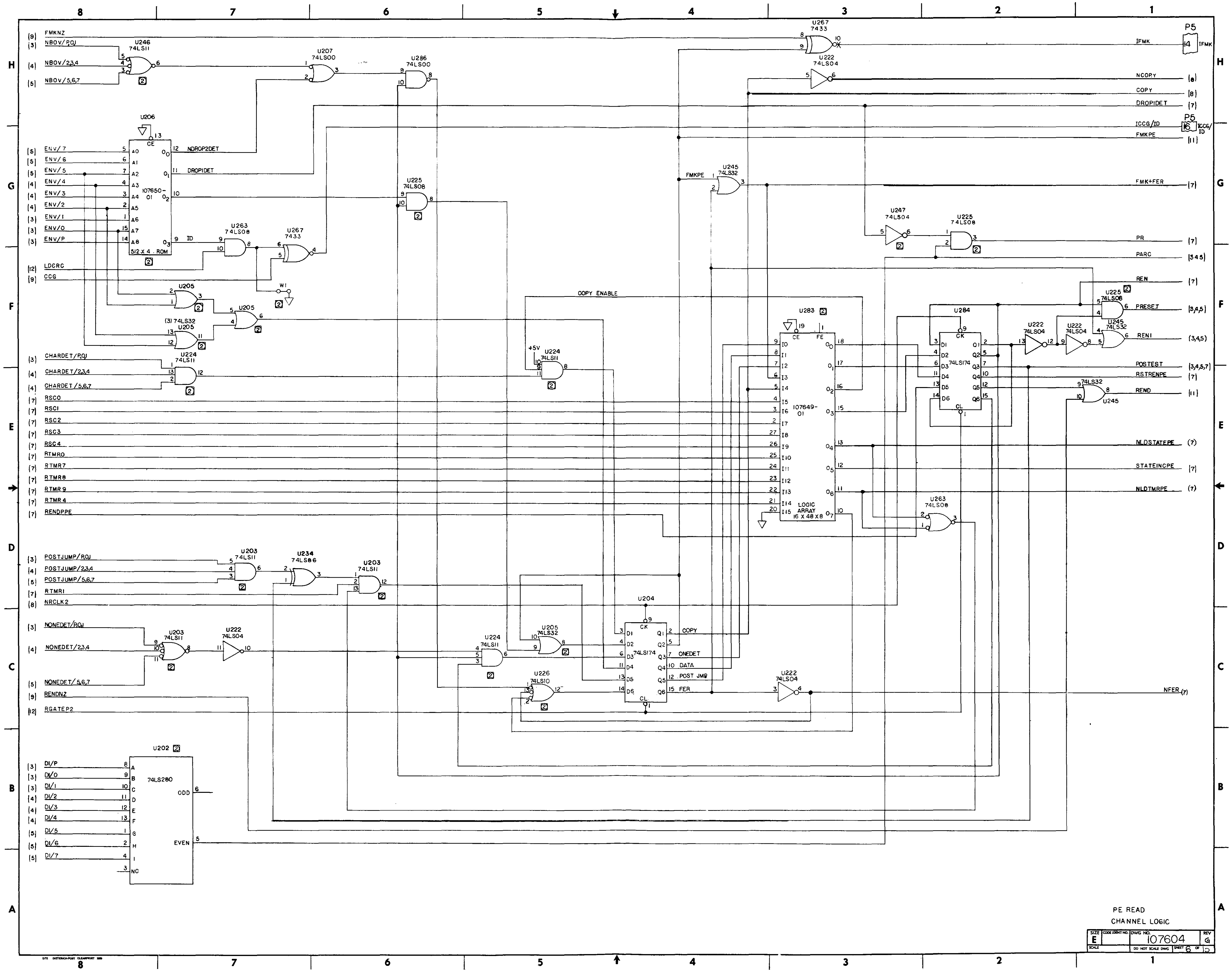
NRDS
NCLRNZDATA
1/2 74LS174
RDNZ/2
RDNZ/3
RDNZ/4
U109 7433
U105 7433
U69 7433
IR2
IR3
IR4
P4
P5
P3
IRD2
IRD3
IRD4
U10 120-0001
U9 74LS14
U25 74LS86
U89 74LS86
RD/2
RD/3
RD/4
INDIVIDUAL READ CHANNEL LOGIC
CH. 2 CIRCUIT 400
CH. 3 CIRCUIT 500
CH. 4 CIRCUIT 600
(SEE SHEET 2)
NCHDET/2
BODET/2
ONEDET/2
DI/2
DROP/2
ENV/2
DGATE/2
NCHDET/3
BODET/3
ONEDET/3
DI/3
DROP/3
ENV/3
NCHDET/4
BODET/4
ONEDET/4
DI/4
DROP/4
ENV 4
U61 74LS27
U101 74LS174
U81 107651-02 256X4 ROM
POSTJUMP/2,3,4
NONEDET/2,3,4
NBOV/2,3,4
CHARDET/2,3,4
REV 2
PRESET
NRCLK1
SHLCLK
SHRCLK
REN 1
IDGATE
RGATE P1
NSHRCLK
ECLK
PARC
POSTEST
COMBINED 2,3,4 READ
CHANNEL LOGIC
SIZE E
DWG NO. 107604
REV G
DO NOT SCALE DWG
SHEET 4 OF 5



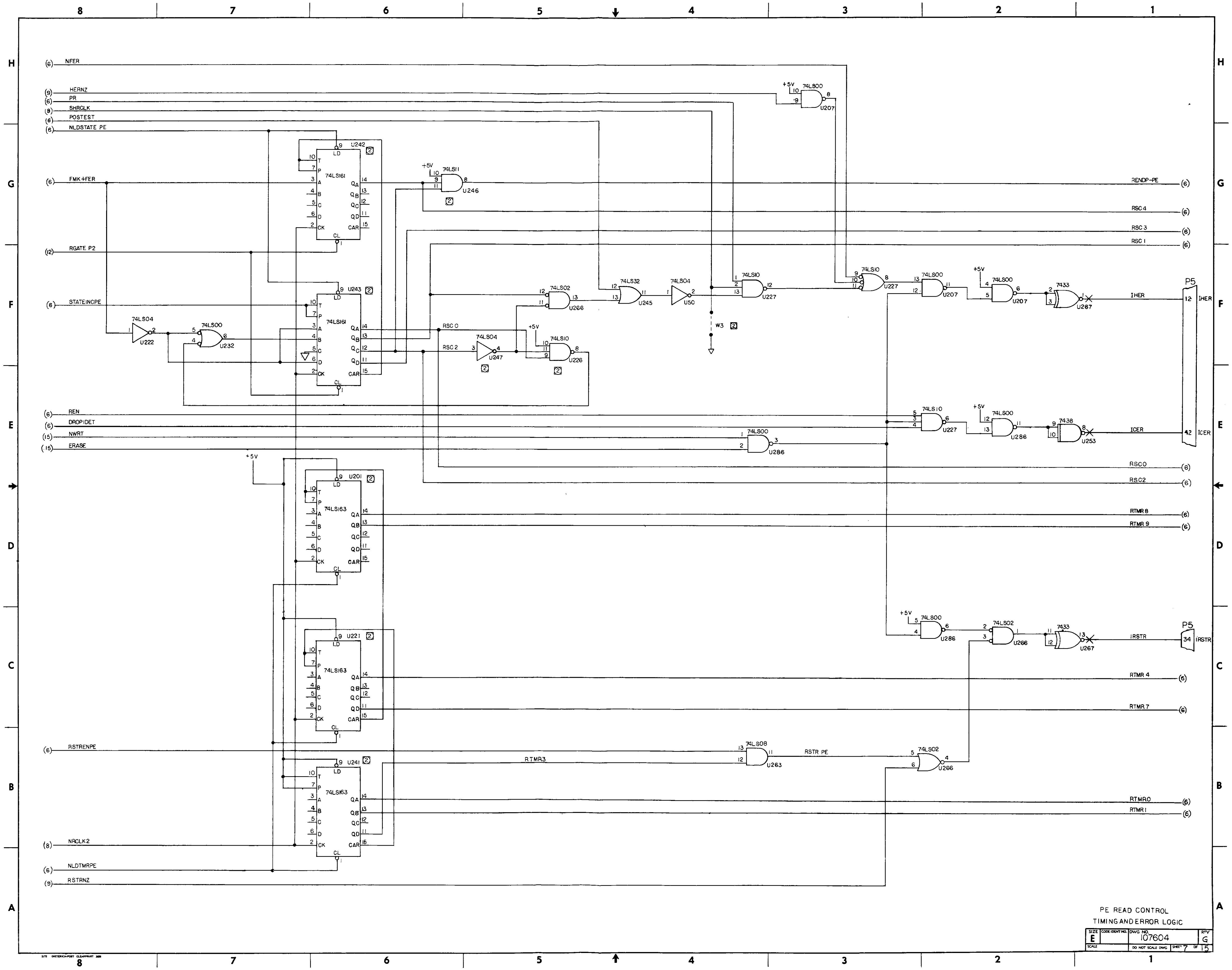
COMBINED 5,6,7 READ CHANNEL LOGIC

SIZE	DWG NO.	REV
E	107604	G

SHEET 5 OF 15



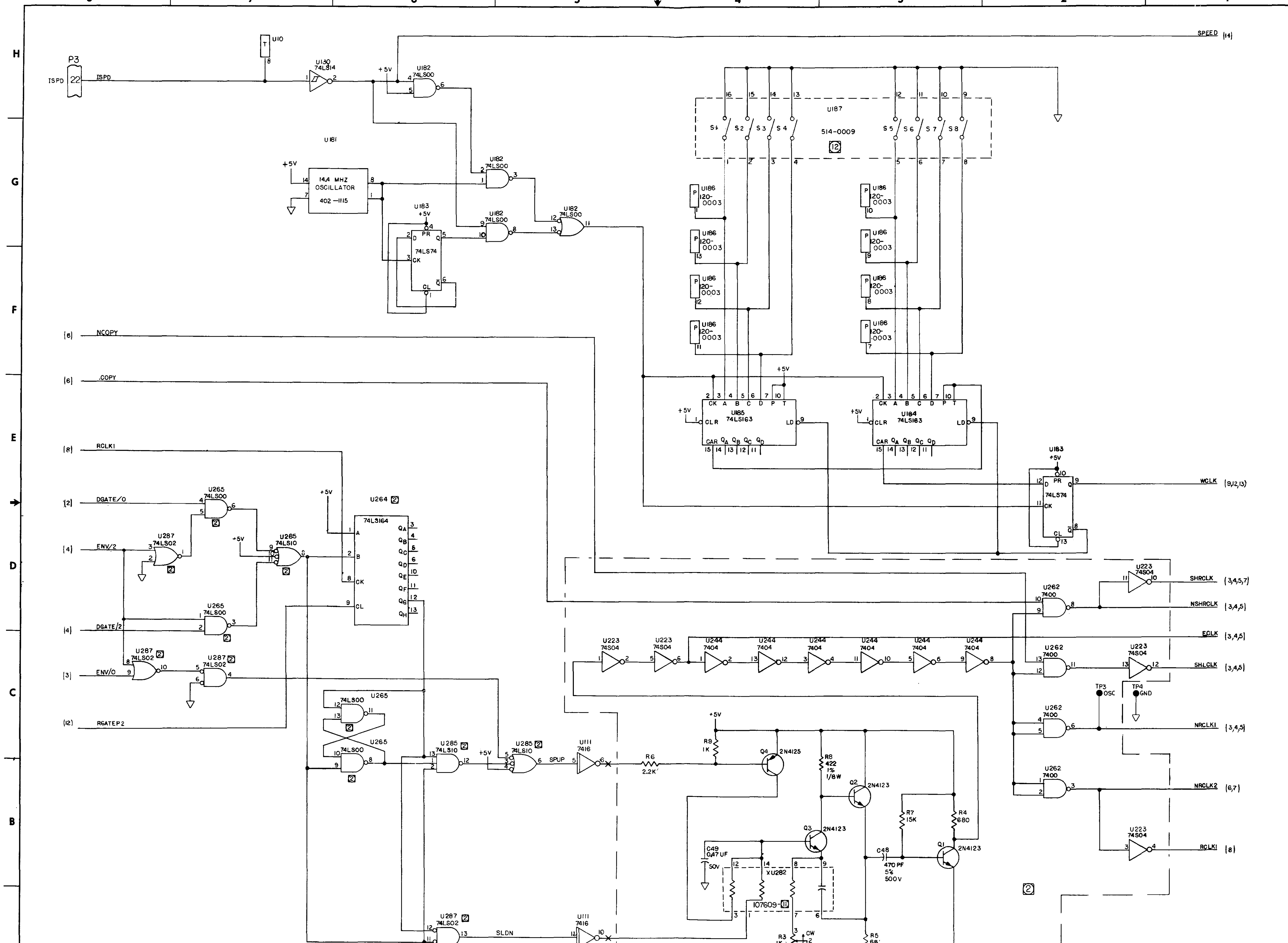
FMKNZ
NBOV/RQJ
NBOV/2,3,4
NBOV/5,6,7
ENV/7
ENV/6
ENV/5
ENV/4
ENV/3
ENV/2
ENV/1
ENV/0
ENV/P
LDCRC
CCG
CHARDET/RQJ
CHARDET/2,3,4
CHARDET/5,6,7
RSC0
RSC1
RSC2
RSC3
RSC4
RTMR0
RTMR7
RTMR8
RTMR9
RTMR4
RENDPPE
POSTJUMP/RQJ
POSTJUMP/2,3,4
POSTJUMP/5,6,7
RTMR1
NRCLK2
NONEDET/RQJ
NONEDET/2,3,4
NONEDET/5,6,7
RENDNZ
RGATEP2
DI/P
DI/0
DI/1
DI/2
DI/3
DI/4
DI/5
DI/6
DI/7
U246 74LS11
U207 74LS00
U286 74LS00
U206
107650-01
512 X 4 ROM
NDROP2DET
DROPIDET
U225 74LS08
U263 74LS08
U267 7433
W1
U205 74LS32
U224 74LS11
COPY ENABLE
+5V
U203 74LS11
U234 74LS86
U222 74LS04
U204
74LS174
COPY
ONEDET
DATA
POST JMP
FER
U226 74LS10
U202
74LS280
ODD
EVEN
U245 74LS32
FMKPE
U283
107649-01
LOGIC ARRAY 16 X 48 X 8
U284
74LS174
U247 74LS04
U263 74LS08
P5
IFMK
NCOPY
COPY
DROPIDET
ICCG/ID
FMKPE
FMK+FER
PR
PARC
REN
PRESET
REN1
POSTEST
RSTRENPE
REND
NLDSTATEPE
STATEINCPE
NLDTMRPE
NFER
PE READ
CHANNEL LOGIC
SIZE E
DWG NO. 107604
REV G
SHEET 6 OF 10
DO NOT SCALE DWG



PE READ CONTROL
TIMING AND ERROR LOGIC

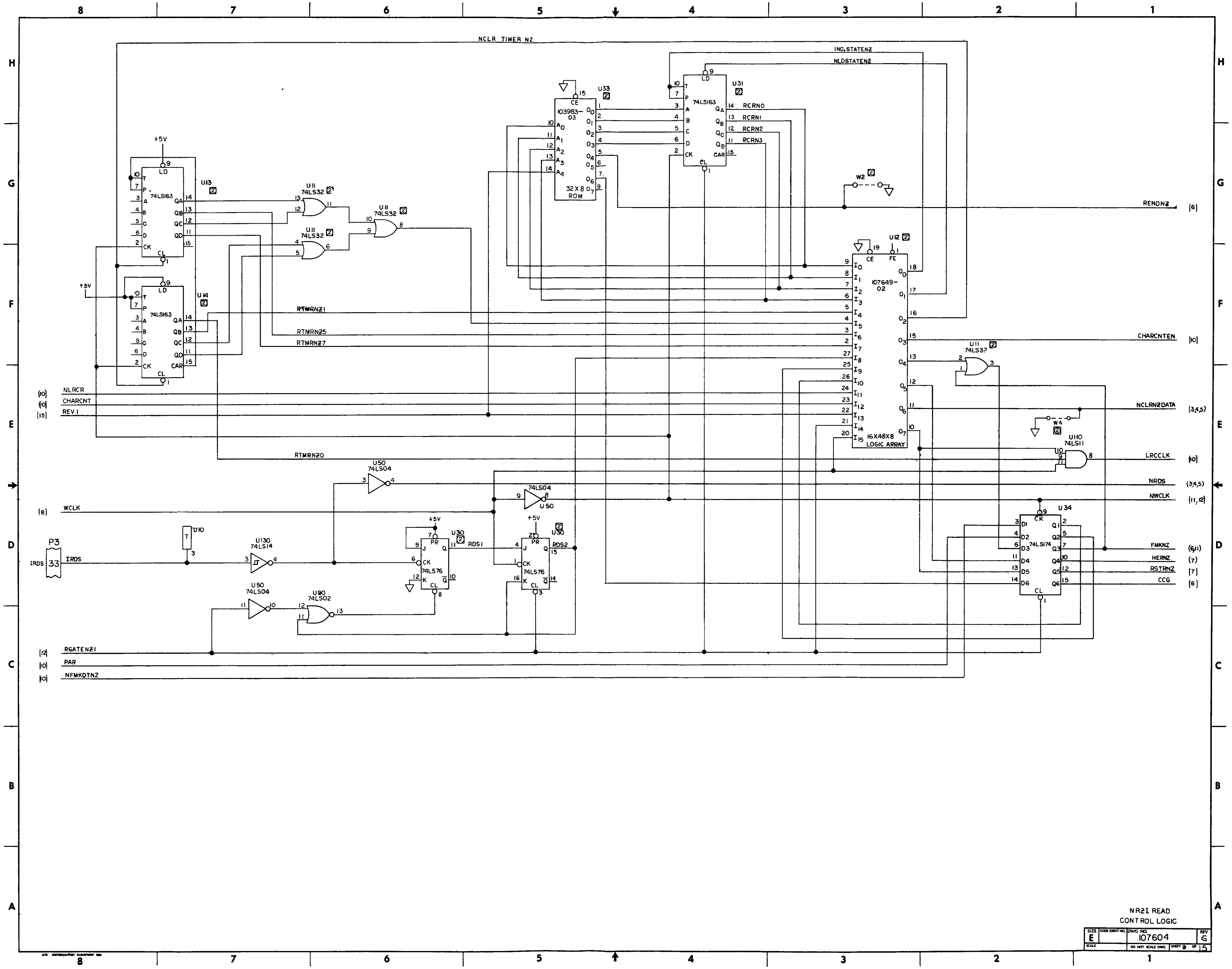
SIZE	DWG NO.	REV
E	107604	G

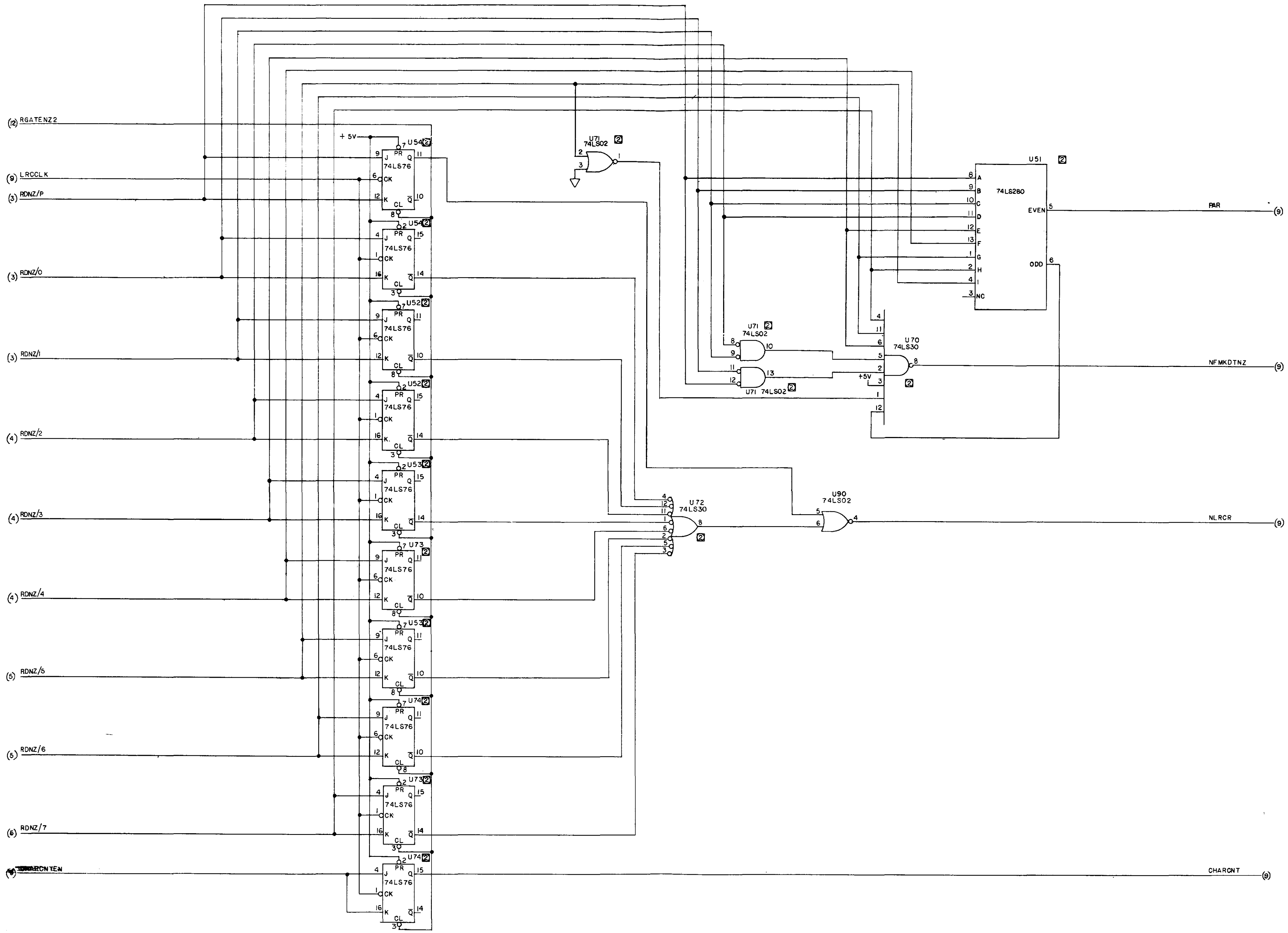
SHEET 7 OF 15



FIXED AND TRACKING OSCILLATORS

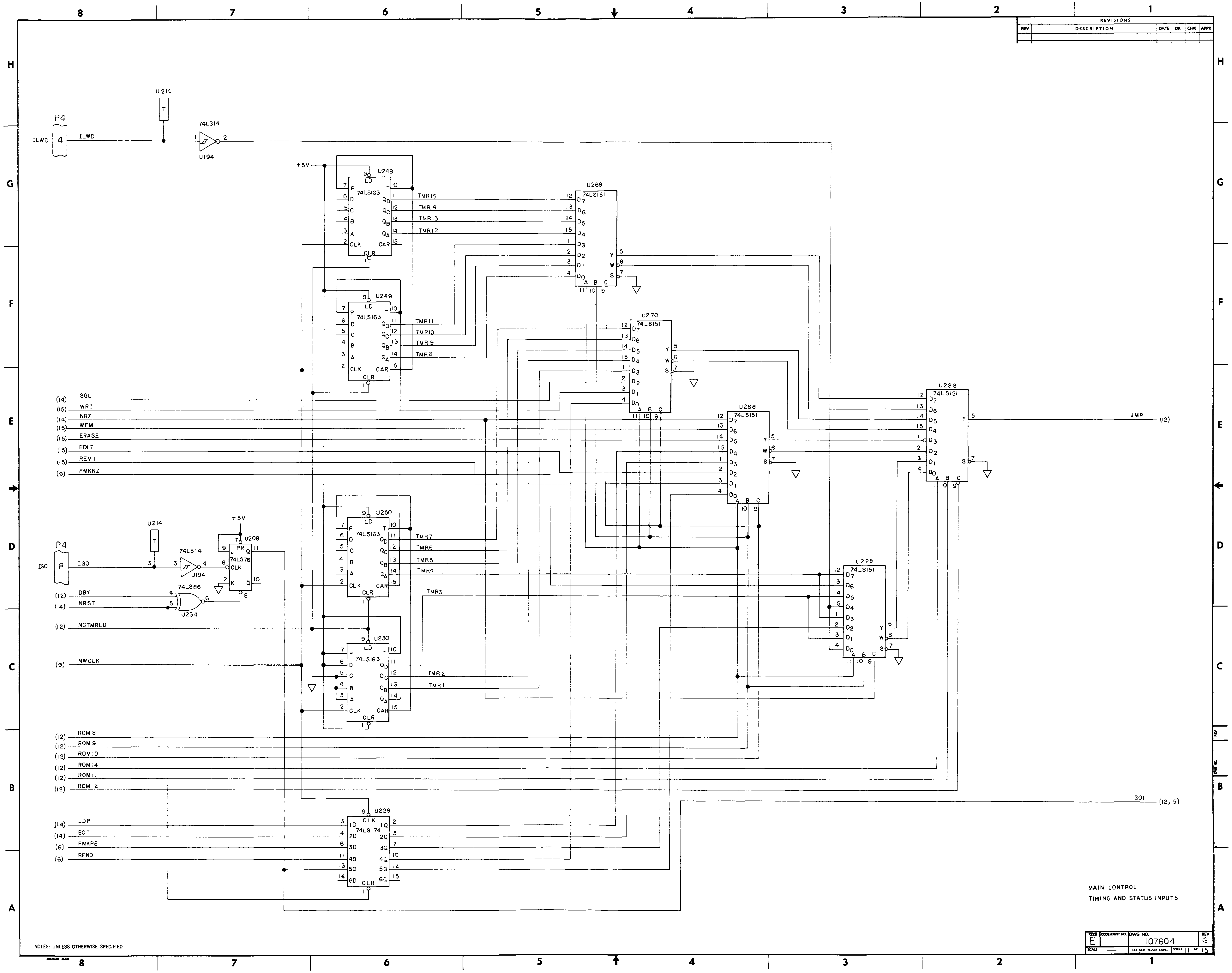
SIZE	CODE IDENT NO.	DWG NO.	REV
E		107604	G
SCALE		DO NOT SCALE DWG	SHEET 8 OF 15


NCLR TIMER NZ
INC STATENZ
NLDSTATENZ
U13
74LS163
U14
74LS163
U11
74LS32
U33
103983-03
32 X 8 ROM
U31
74LS163
RCRN0
RCRN1
RCRN2
RCRN3
W2
RENDNZ
U12
107649-02
16X48X8 LOGIC ARRAY
RTMRNZ1
RTMRNZ5
RTMRNZ7
RTMRNZ0
CHARCNTEN
NCLRNZDATA
W4
U110
74LS11
LRCCLK
NRDS
NWCLK
NLRCR
CHARCNT
REV1
U50
74LS04
WCLK
P3
IRDS
U10
U130
74LS14
U30
74LS76
RDS1
RDS2
U90
74LS02
U34
74LS174
FMKNZ
HERNZ
RSTRNZ
CCG
RGATENZ1
PAR
NFMKDTNZ
+5V
NR21 READ
CONTROL LOGIC
107604



NRZI ERROR
CHECK LOGIC

SIZE	CODE IDENT NO.	DWG NO.	REV
E		107604	G
SCALE		DO NOT SCALE DWG	SHEET 10 OF 15

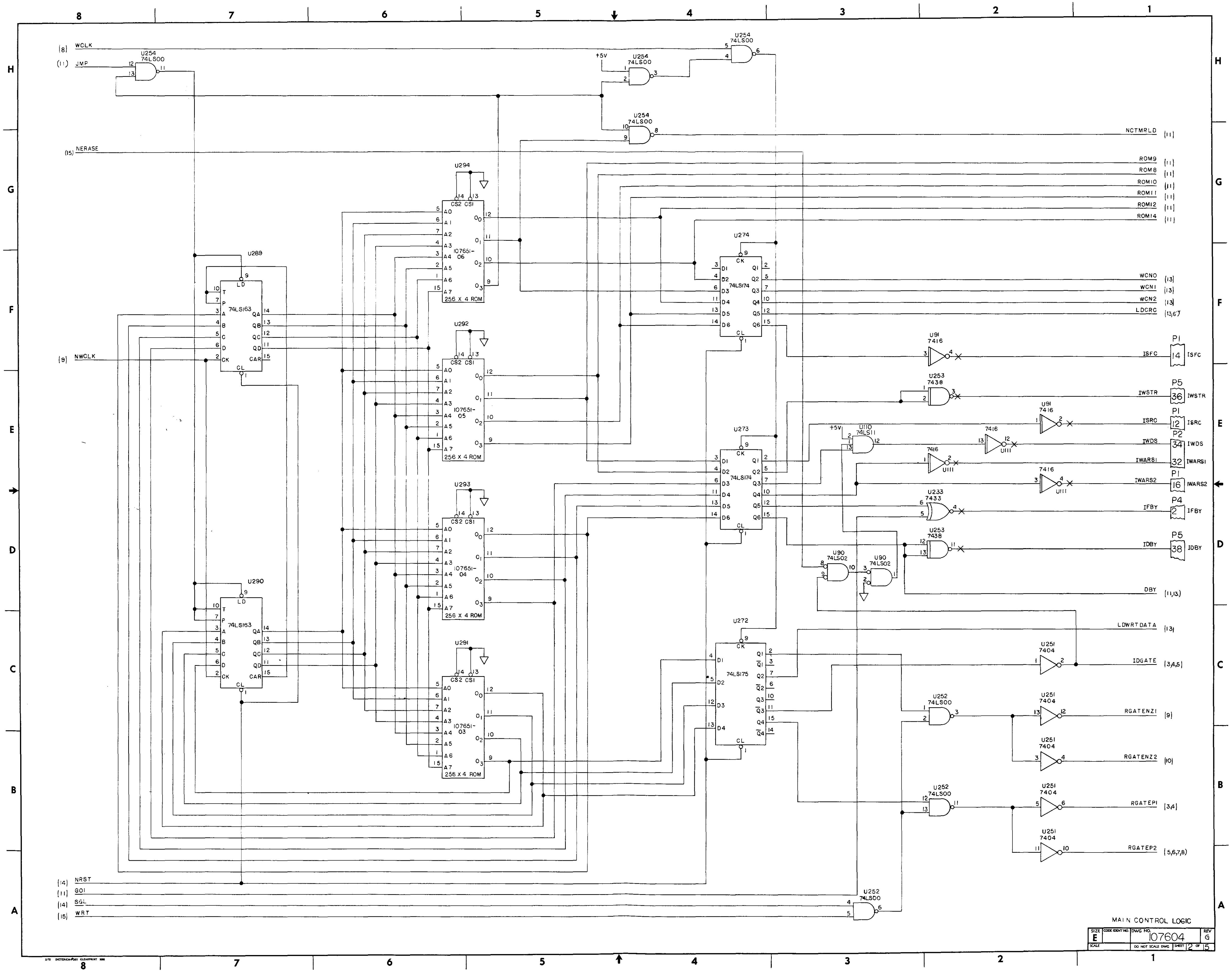


MAIN CONTROL
TIMING AND STATUS INPUTS

NOTES: UNLESS OTHERWISE SPECIFIED

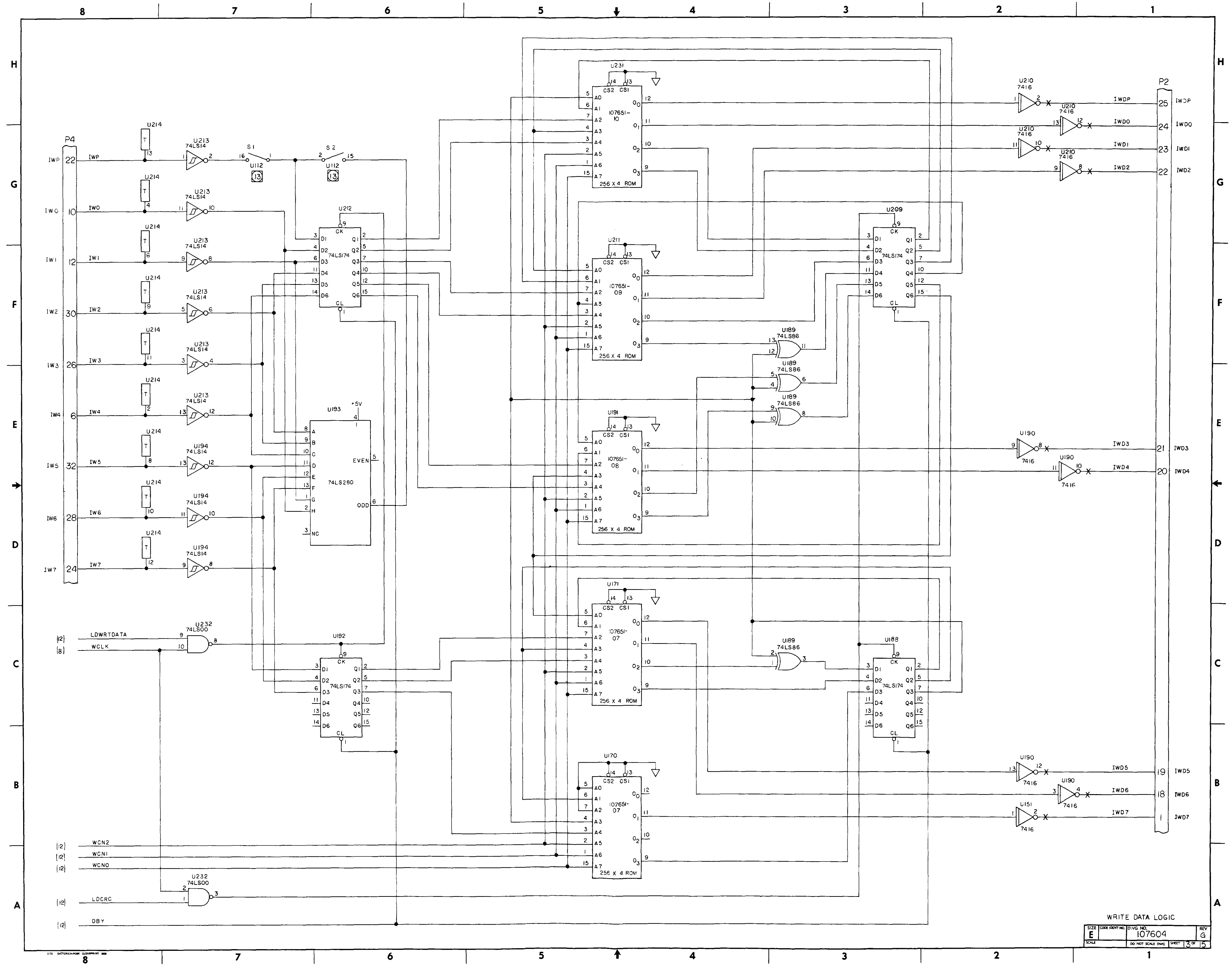
SIZE E DWG NO. 107604 REV G

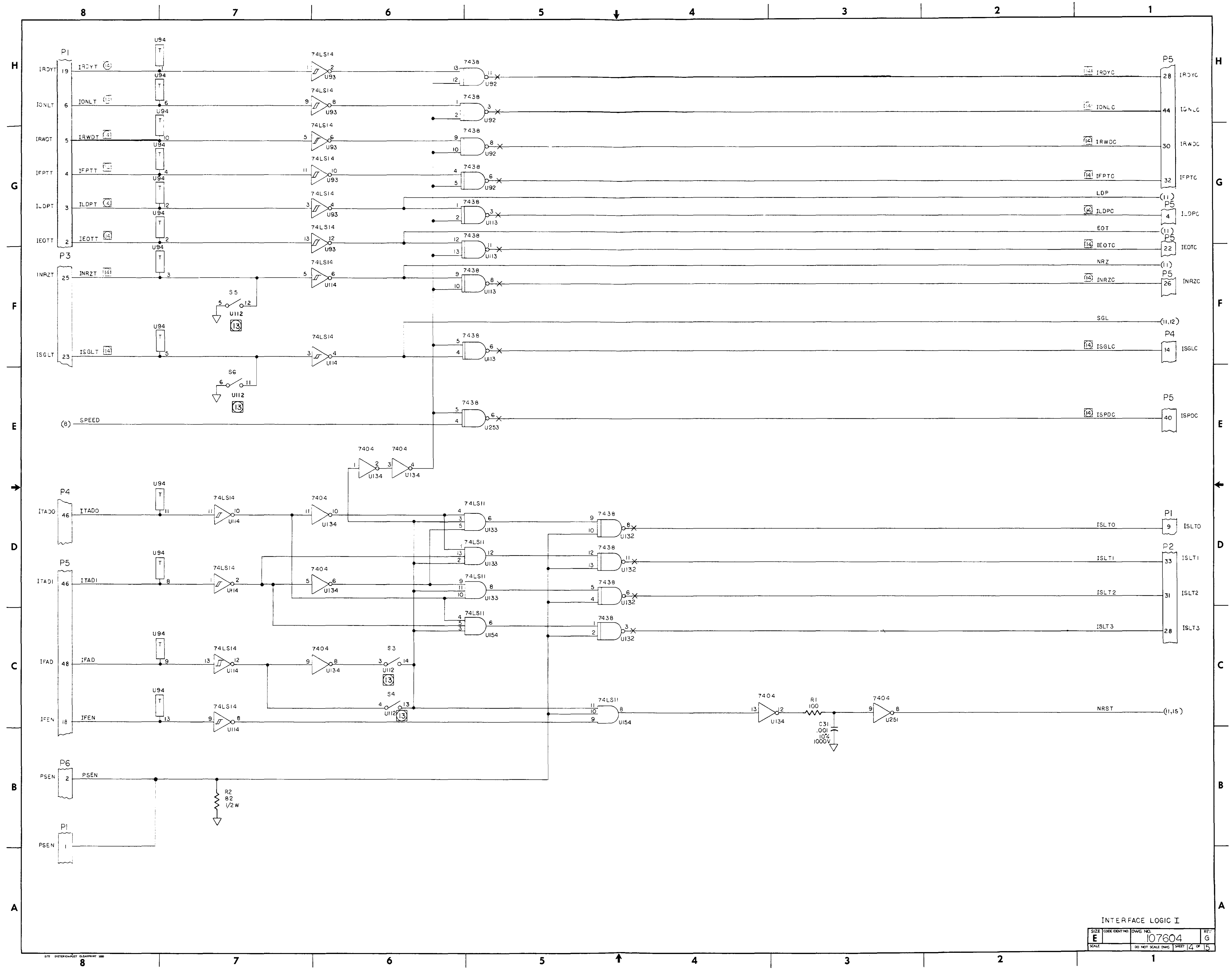
SCALE — DO NOT SCALE DWG SHEET 11 OF 15



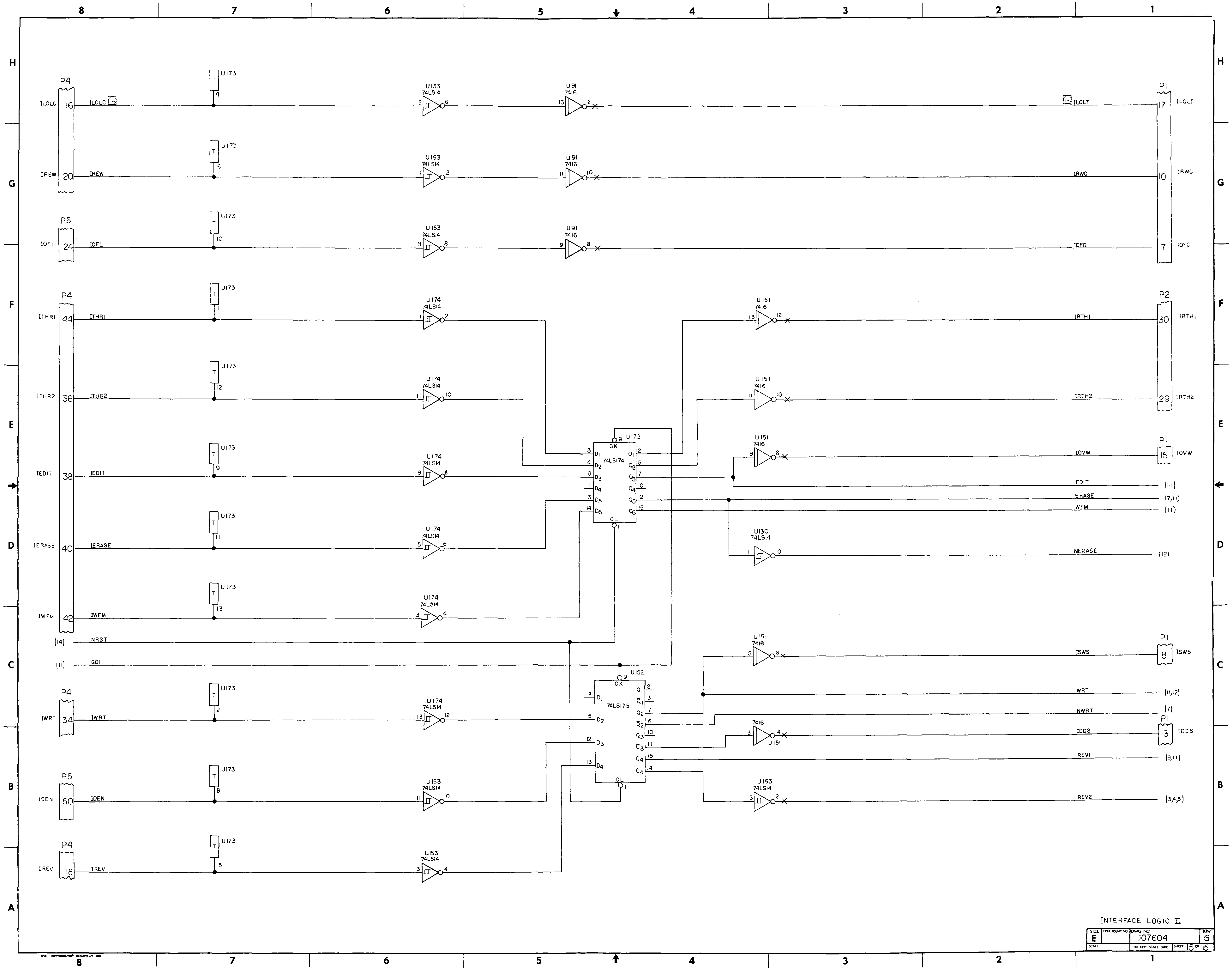
MAIN CONTROL LOGIC

SIZE	CODE IDENT NO.	DWG. NO.	REV
E		107604	G
SCALE		DO NOT SCALE DWG	SHEET 12 OF 15


P4
IWP
IW0
IW1
IW2
IW3
IW4
IW5
IW6
IW7
U214
U213
74LS14
U194
S1
S2
U112
U212
74LS174
U193
74LS280
EVEN
ODD
+5V
U232
74LS00
LDWRTDATA
WCLK
U192
WCN2
WCN1
WCN0
LDCRC
DBY
U231
U211
U191
U171
U170
107651-10
107651-09
107651-08
107651-07
256 X 4 ROM
CS2
CS1
U189
74LS86
U209
U188
U210
7416
U190
U151
IWDP
IWD0
IWD1
IWD2
IWD3
IWD4
IWD5
IWD6
IWD7
P2
WRITE DATA LOGIC
107604
G

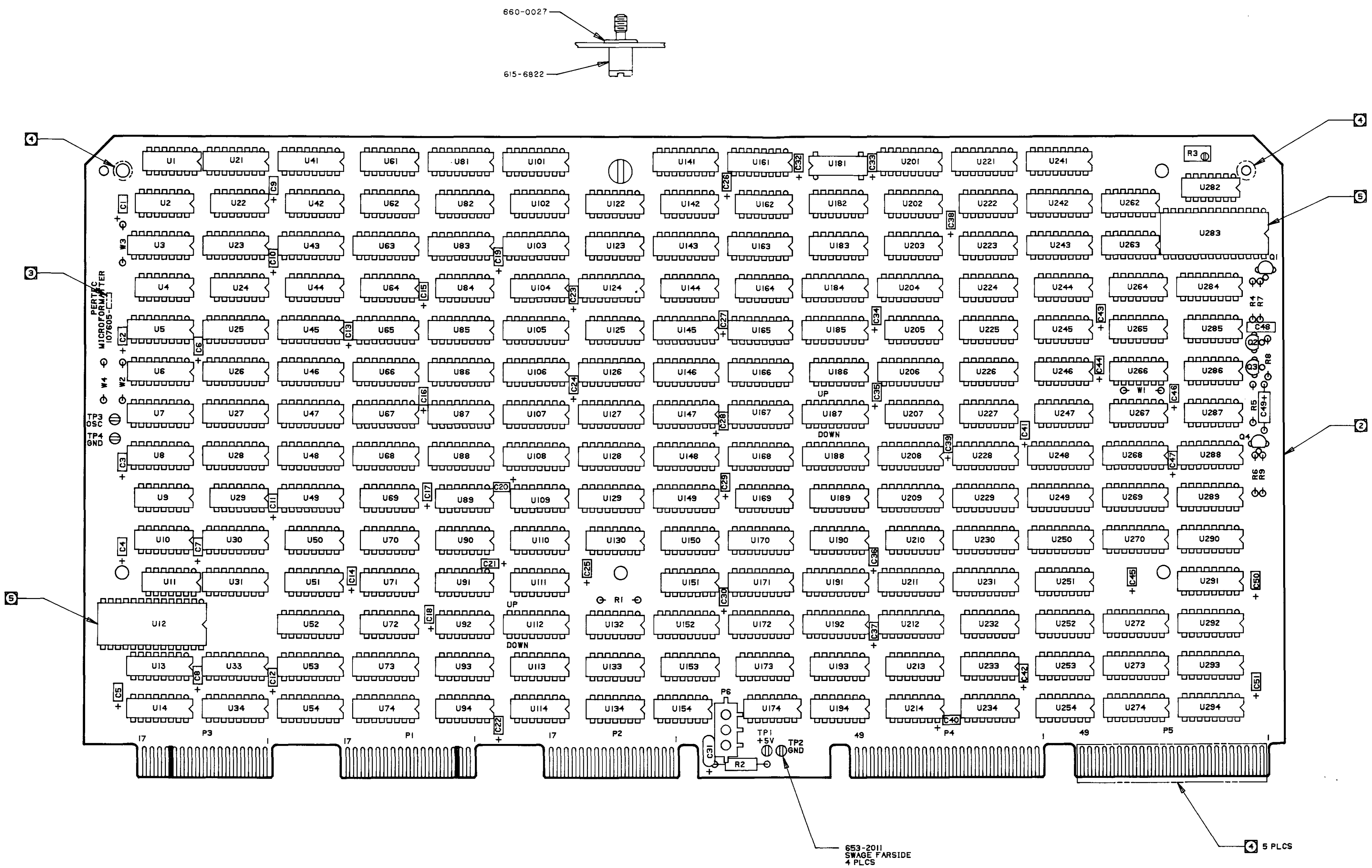


P1
IRDYT
IONLT
IRWDT
IFPTT
ILDPT
IEOTT
P3
INRZT
ISGLT
S5
S6
U112
SPEED
P4
ITAD0
P5
ITAD1
IFAD
IFEN
P6
PSEN
R2
82
1/2 W
U94
74LS14
U93
U114
7438
U92
U113
U253
7404
U134
74LS11
U133
U154
U132
S3
S4
R1
100
C31
.001
10%
1000V
U251
LDP
EOT
NRZ
SGL
NRST
IRDYC
IONLC
IRWDC
IFPTC
ILDPC
IEOTC
INRZC
ISGLC
ISPDC
ISLT0
P2
ISLT1
ISLT2
ISLT3
INTERFACE LOGIC I
SIZE
E
CODE IDENT NO.
DWG. NO.
107604
REV
G
SCALE
DO NOT SCALE DWG
SHEET 14 OF 15



INTERFACE LOGIC II
SIZE E
DWG NO. 107604
REV G
SHEET 15 OF 15
DO NOT SCALE DWG
P4
P5
P1
P2
U173
U153 74LS14
U91 7416
U174 74LS14
U151 7416
U172 74LS174
U152 74LS175
U130 74LS14
ILOLC
IREW
IOFL
ITHR1
ITHR2
IEDIT
IERASE
IWFM
NRST
GO1
IWRT
IDEN
IREV
ILOLT
IRWC
IOFC
IRTH1
IRTH2
IOVW
EDIT
ERASE
WFM
NERASE
ISWS
WRT
NWRT
IDDS
REV1
REV2

REV	DESCRIPTION	DATE	DR	CHK	APPR
	A, ERN 8-YZ PRE-PROD RELEASE: B, ECN 9750: C, ECN 9893A & ERN 9-NZ PROD RELEASE D, ECN 10243				
E	ECN 10874 REPLOT		RAS		
F	ECN 11134	3/1/78			



SCHEMATIC: 107604
SPECIFICATION:
REF DWGS:

PART NO. 107605-02 REV E

5. INSTALL SOCKETS 503-0112 PRIOR TO INSTALLATION OF I.C.'S
4. MASK AREAS SHOWN DURING FLOW SOLDER OPERATION.
3. MARK VERSION NO. AND VERSION ISSUE LETTER IN AREA SHOWN.
2. THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 107606-01 REV F AND SUBSEQUENT.
1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ±.01 .XXX ±.005 ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. CADDS	12/21/77
CHK	
DES	
ENGR	
PROJ. ENGR	

FT7000	
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:

MATL: SEE L/M

PERTEC
a division of Pertec Computer Corporation

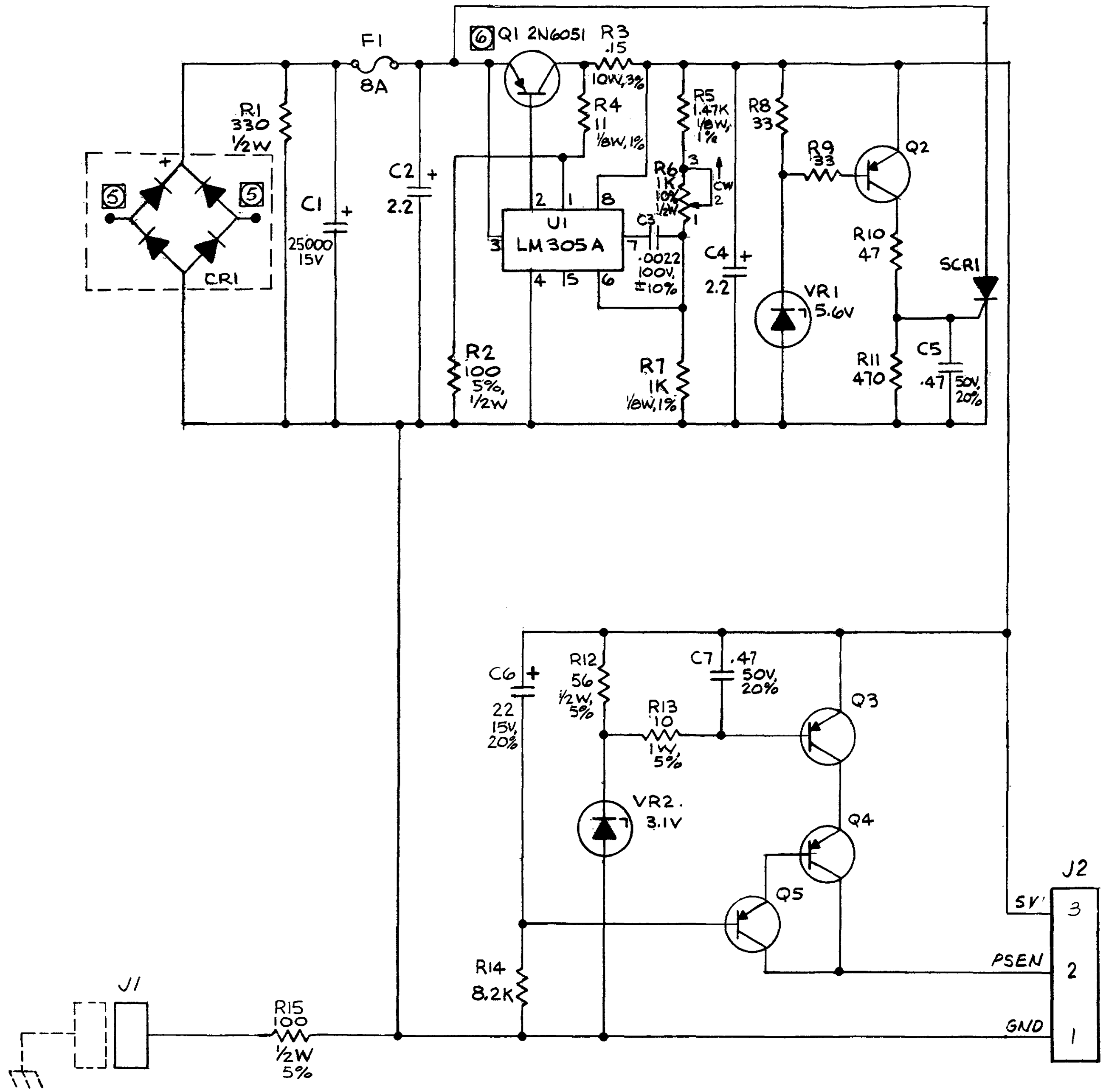
TITLE
PCBA MICROFORMATTER

SIZE	CODE IDENT NO.	DWG NO.	REV
E	32097	107605	F

SCALE 2:1 DO NOT SCALE DWG SHEET 1 OF 1

CADDS

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
1	PROTOTYPE	[illegible]	TM		
2	REVERSE PINS 1&3 ON J3			✓	
A	ERN 8-YN PROD RELEASE	[illegible]	SK	[illegible]	E.A.
B	ECN 9965	5-25-77	ES	[illegible]	E.A.



1 TABLE I

PART NO.	REF DES
101-3315	R1
101-1015	R2,15
118-0013	R3
107-0110	R4
107-1471	R5
124-1021	R6
107-1001	R7
100-3305	R8, 9
100-4705	R10
100-4715	R11
101-5605	R12
102-1005	R13
100-8225	R14
134-2591	C1
139-2244	C2, 4
131-2220	C3
135-4742	C5, 7
139-2262	C6
200-6051	Q1
200-4402	Q2, 3, 4, 5
330-0565	VR1
330-0395	VR2
201-0126	SCR1
400-0305	U1
320-1010	CR1
663-3080	F1

6 COMPONENT IS MOUNTED ON HEATSINK.

5 TRANSFORMER OUTPUT LEADS ARE CONNECTED TO FAST-ON TERMINALS ON THE DIODE BRIDGE.

4. PNP TRANSISTORS ARE 2N4402.

3. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 20V.

2. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

1 FOR PART NUMBER SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY NUMBER- 107615

REFERENCE DRAWINGS-

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	REF. DES.	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .03 ANGULAR
.XXX ± .010 ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. T. MORTON	8/16/76
CHK [illegible]	11/5/76
DES	
ENGR	
PROJ. ENGR E. [illegible]	11/8/76

PERTEC PERIPHERAL EQUIPMENT

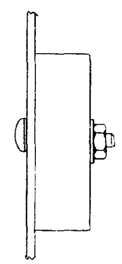
TITLE
SCHEMATIC, POWER SUPPLY II

107615 NEXT ASSY | 1ST USED ON
APPLICATION
FINISH:
MATL:

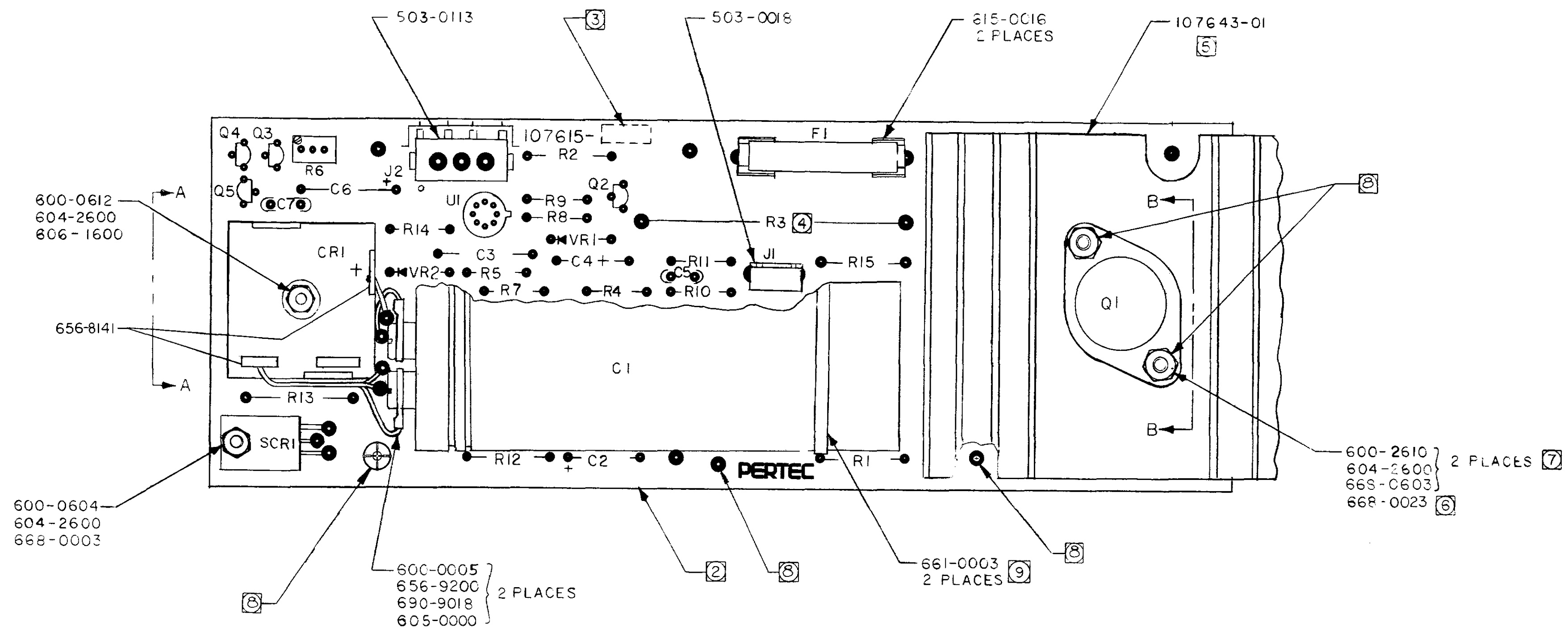
SIZE D | CODE IDENT NO. | DWG NO. 107614 | REV B
SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1

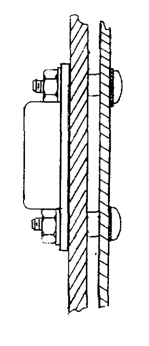
DWG. NO. 107614 REV. B

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
1	PROTOTYPE	9/4/76			
A	ERN 8-YN PROD RELEASE	10/25/76	SK		
B	ECN 9965	5-25-77			
C	ECN 10649A	10-5-77	RDB		
D	ECN 11088				



VIEW A-A





SECTION E-E

(9) TYWRAP (661-0003) TO GO THRU P.C. BOARD AND AROUND C1 CAPACITOR.

(2) MASK AREAS SHOWN DURING FLOW SOLDER OPERATION.

(7) TORQUE TO 11 INCH LBS.

(6) IF NON-GREASED INSULATOR IS USED COVER BOTH SIDES WITH SILICONE GREASE.

(5) BEFORE INSTALLATION OF COMPONENTS, REMOVE ALL BURRS AND METAL CHIPS FROM MOUNTING SURFACES.

(4) MAINTAIN MINIMUM AIR GAP OF .10 BETWEEN COMPONENT BODY AND BOARD.

(3) MARK VERSION NO AND VERSION ISSUE LETTER IN AREA SHOWN.

(2) THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 107616-01 REV C. & SUBSEQUENT.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

2/72 DIETERICH-POST CLEARPRINT 1020

NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
X/X ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

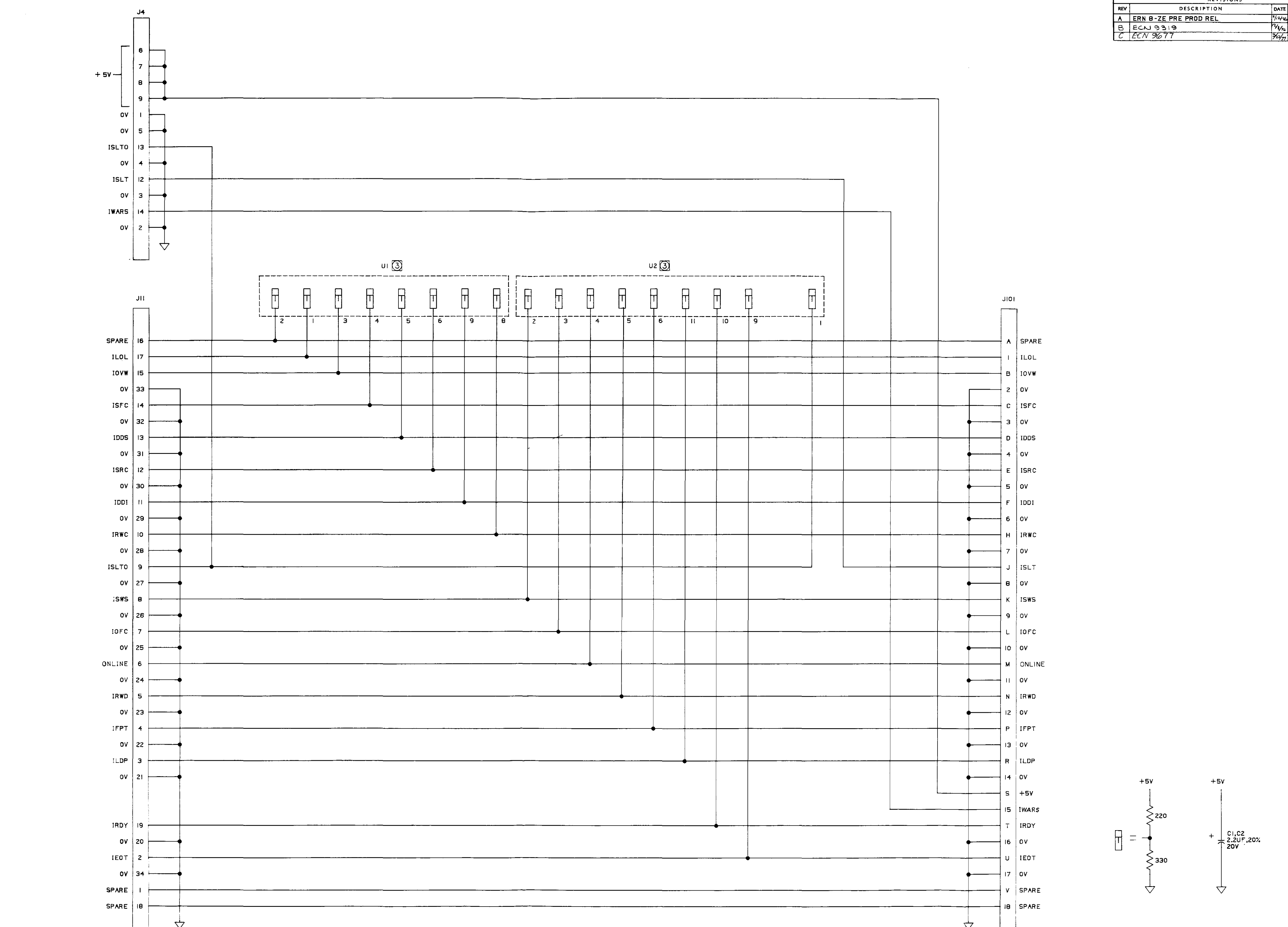
SIGNATURES	DATE
DR.	9/4/76
CHK	11/5/76
DES	
ENGR	
PROJ. ENGR	11/8/76

MATL: SEE L/M

PERTEC PERIPHERAL EQUIPMENT

TITLE
PCBA
POWER SUPPLY II

SIZE	CODE IDENT NO.	DWG NO.	REV
F		107615	D
SCALE 2/1		DO NOT SCALE DWG	SHEET 1 OF 1



REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-ZE PRE PROD REL	11/12/76			
B	ECN 9319	12/1/76	TBH		
C	ECN 9677	3/22/77	GMP	K.T.	

3 TERMINATING RESISTOR PACK SPECIFIED AT TOP ASSEMBLY.

2. ALL CAPACITORS ARE PERTEC P/N 1139-2244).

1. RESISTOR VALUES ARE IN OHMS. TERMINATORS ARE LOCATED ON U1 AND U2 PERTEC P/N (120-0001). PIN 14 IS +5V, PIN 7 IS GND.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	FIN.	REF. DES.	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR.	11/13/76
CHK	11/14/76
DES	
ENGR	
PROJ. ENGR	11/15/76

PERTEC PERIPHERAL EQUIPMENT

TITLE
SCHEMATIC
CABLE ADAPTER I
(DC)

107631	FT7000
NEXT ASSY	1ST USED ON
APPLICATION	

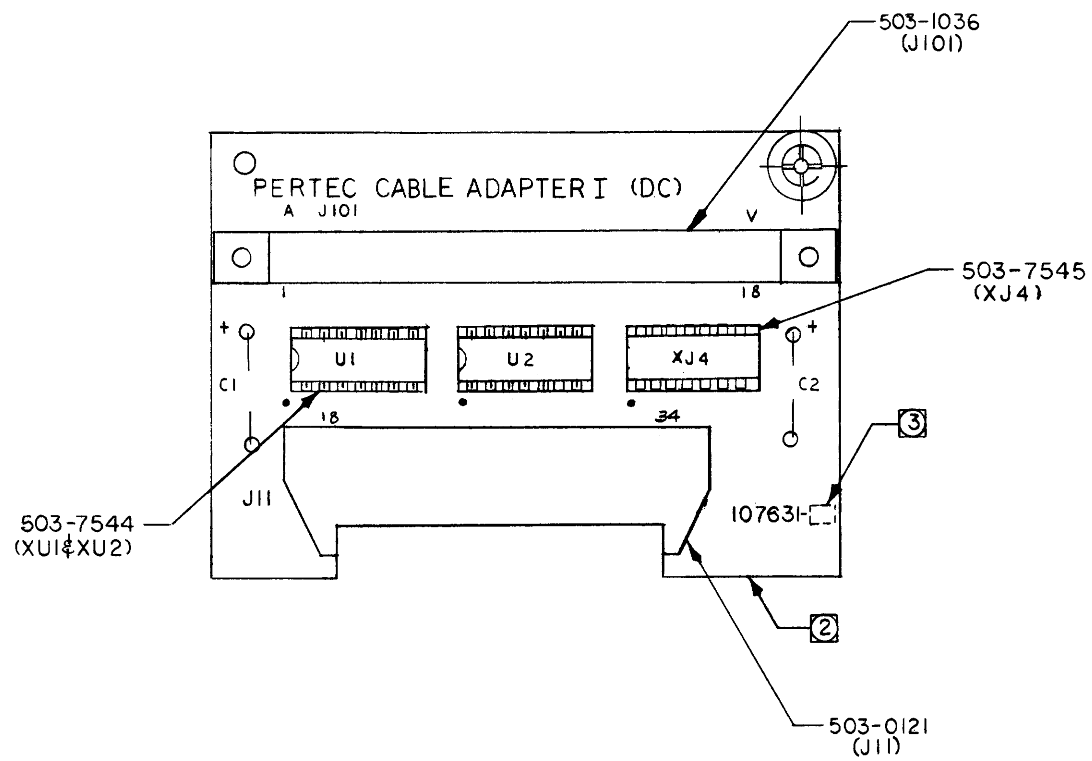
FINISH:

MATL:

SIZE	CODE IDENT NO.	DWG NO.	REV
E		107630	C
SCALE NONE		DO NOT SCALE DWG	SHEET 1 OF 1

10-85

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 82E PRE-PROD RELEASE	11/1/76		K.T.	E.B.
B	ECN 9677	3/22/77	9MP	K.T.	E.B.



SCHEMATIC 107630

REF DWGS:

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	REF. DES.	ITEM NO.

LIST OF MATERIAL

The information hereon is the property of PERTEC CORPORATION. No portion of this data shall be released, disclosed, used, or duplicated, for procurement or manufacturing purposes without specific written consent of PERTEC.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .03
.XXX ± .010
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR	11/1/76
CHK	11/1/76
DES	
ENGR	
PROJ. ENGR	11/15/76

PERTEC PERIPHERAL EQUIPMENT

TITLE
PCBA
CABLE ADAPTER I (DC)

NEXT ASSY	1ST USED ON
104857	FT 7000

APPLICATION

FINISH:

MATL: SEE L/M

SIZE D | CODE IDENT NO. | DWG NO. 107631 | REV B

SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

3 MARK VERSION NO AND VERSION ISSUE LETTER IN AREA SHOWN.

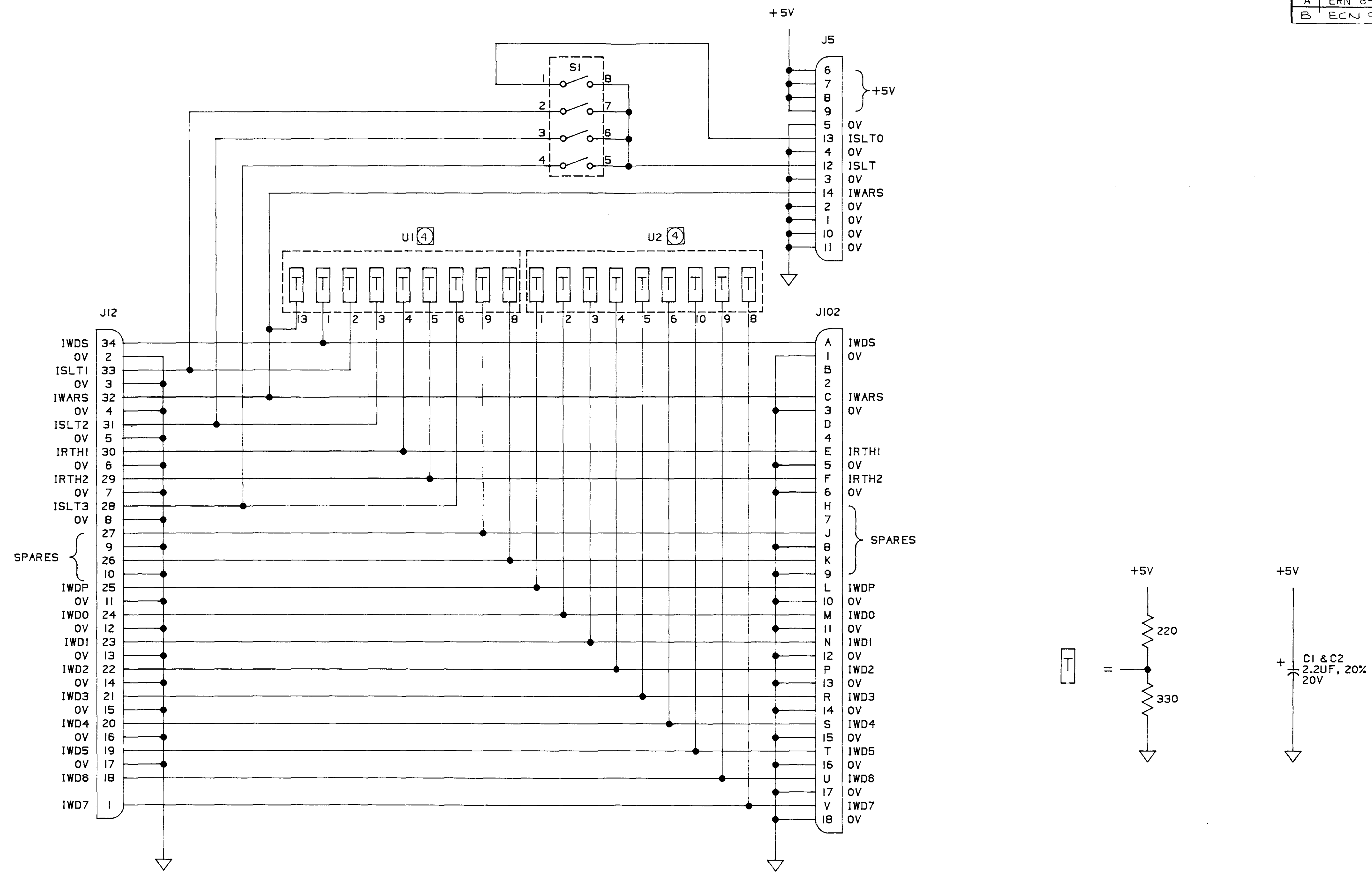
2 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 107632-01 REV 'B' AND SUBSEQUENT.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

DWG. NO. 107631 REV. B

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-ZG PRE-PROD RELEASE	11/12/76	RAS		
B	ECN 9319	12/1/76			



4 TERMINATING RESISTOR PACKS ARE SPECIFIED AT TOP ASSEMBLY.
3. S1 IS PERTEC PART NO. 514-0008.
2. ALL CAPACITORS ARE PERTEC PART NO. 139-2244.
1. RESISTOR VALUES ARE IN OHMS. TERMINATORS ARE LOCATED ON U1 AND U2 PERTEC PART NO. 120-0001. PIN 14 IS +5V, PIN 7 IS GND.

NOTES: UNLESS OTHERWISE SPECIFIED

107635	FT7000
NEXT ASSY	1ST USED ON
APPLICATION	

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .XXX ± ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010
FINISH:
MATL:

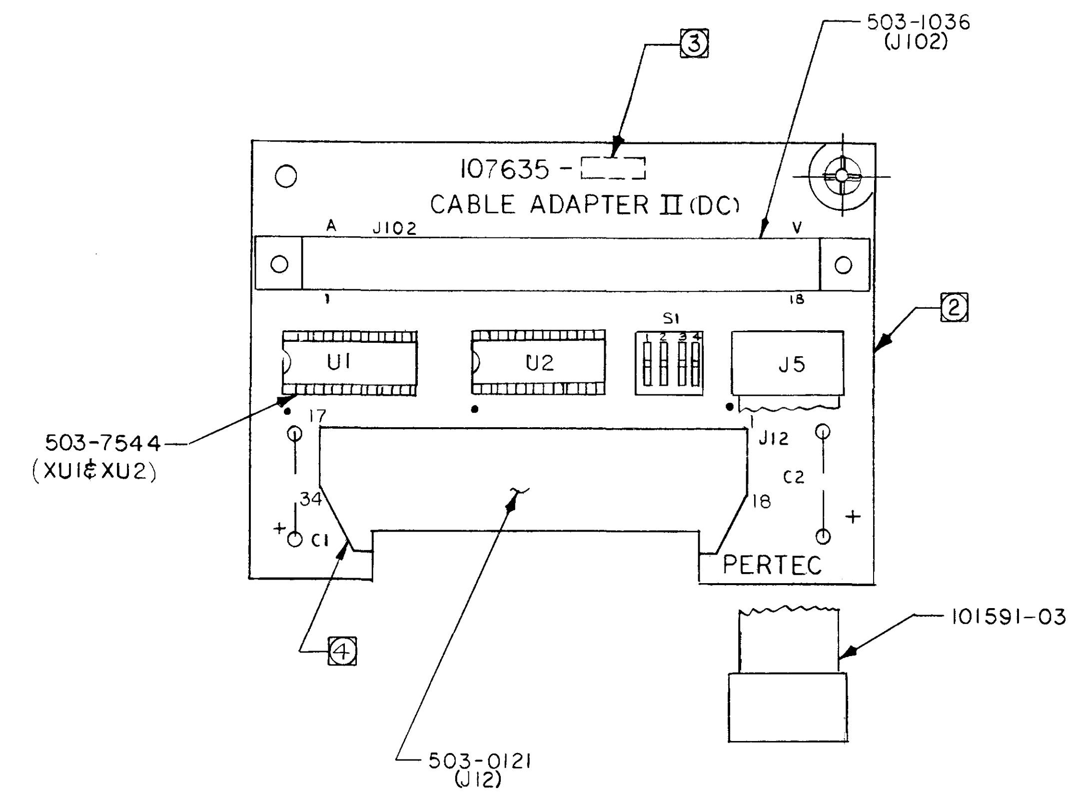
SIGNATURES	DATE
DR. R. SORG	11/12/76
CHK	11/12/76
DES	
ENGR	
PROJ. ENGR	11/17/76

PERTEC PERIPHERAL EQUIPMENT DIVISION

TITLE SCHEMATIC CABLE ADAPTER II (DC)

SIZE D | CODE IDENT NO. 32097 | DWG NO. 107634 | REV B
SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-ZG PRE-PROD. RELEASE	11/1/76			E.B.
B	ECN 9624A				E.B.
	ERN 9-RE PROD. RELEASE				E.B.
C	ECN 10743	11/4/78	J.S.		



SCHEMATIC 107634

REF DWGS

4 BEFORE INSTALLING J12 REMOVE PIN 27

3 MARK VERSION NO. AND VERSION ISSUE LETTER IN AREA SHOWN.

2 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 107636-01 REV B AND SUBSEQUENT.

1. ASSEMBLE STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	REF. DES.	ITEM NO.

LIST OF MATERIAL

NEXT ASSY	1ST USED ON
104857	FT7000

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .03
.XXX ± .010
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

SIGNATURES	DATE
DR	11/1/76
CHK	11/1/76
DES	
ENGR	
PROJ. ENGR E. B.	11/15/76

MATL: SEE LM

PERTEC PERIPHERAL EQUIPMENT

TITLE
PCBA
CABLE ADAPTER II (DC)

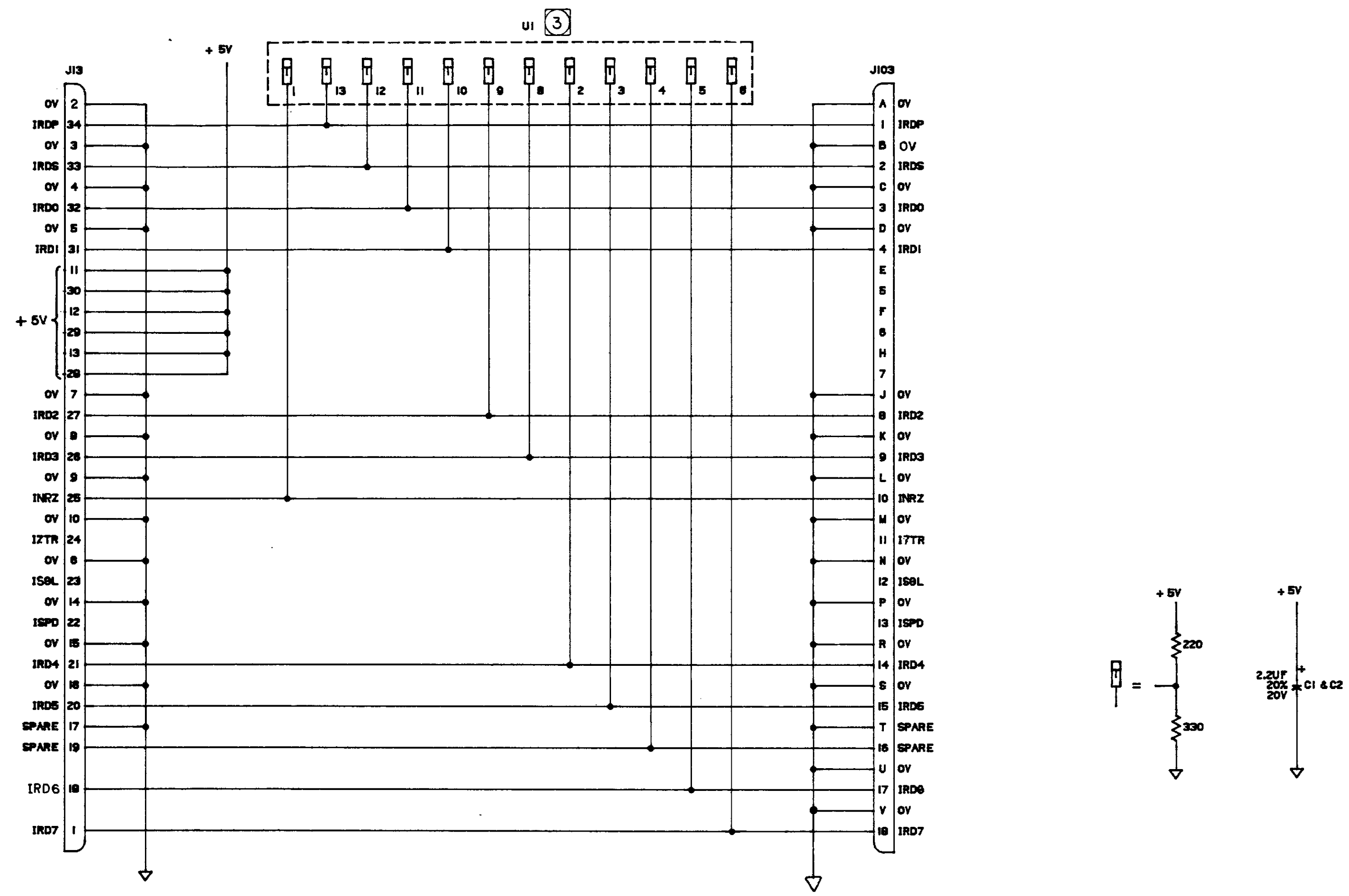
SIZE D | CODE IDENT NO. | DWG NO. 107635 | REV C

SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

REV. C
DWG. NO. 107635

10/73 BRUNING 40-307

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-ZH PRE PROD. RELEASE	11/12/76	RAS		E.B
B	ECN 9319	12/1/76			E.B



3 TERMINATING RESISTOR PACK SPECIFIED AT TOP ASSEMBLY.

2. ALL CAPACITORS ARE PERTEC PART NO. 139-2244.

1. RESISTOR VALUES ARE IN OHMS. TERMINATORS ARE LOCATED ON U1 & ARE PERTEC PART NO. 120-0001. PIN 14 IS +5V PIN 7 IS GND.

NOTES: UNLESS OTHERWISE SPECIFIED

107639	FT7000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .XXX ± ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010
FINISH:

SIGNATURES	DATE
DR. R. SORG	11/12/76
CHK	11/12/76
DES	
ENGR	
PROJ. ENGR E.	11/12/76

MATL:

PERTEC
PERIPHERAL EQUIPMENT DIVISION

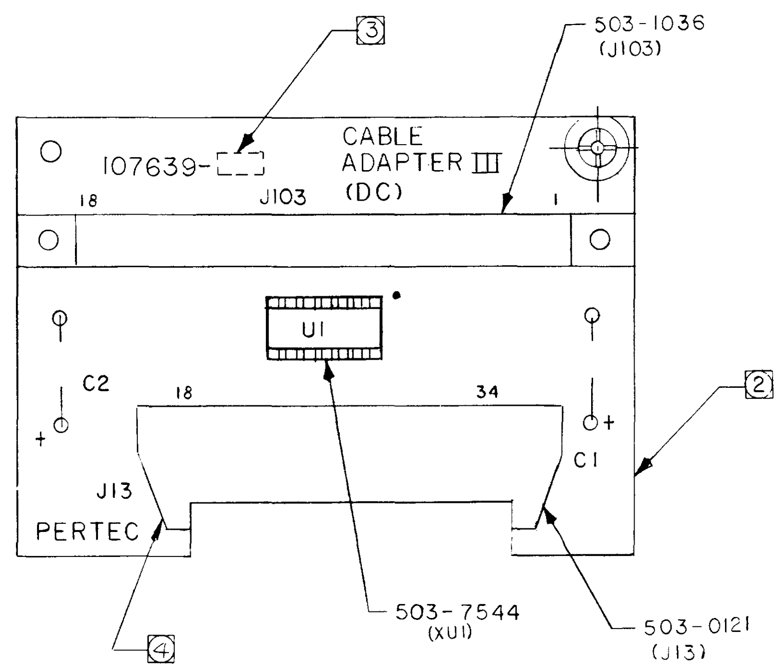
TITLE
SCHEMATIC
CABLE ADAPTER
III (DC)

SIZE	CODE IDENT NO.	DWG NO.	REV
D	32097	107638	B
SCALE NONE	DO NOT SCALE DWG	SHEET 1 OF 1	

DWG. NO. 107638 REV. B

PRINTED ON DIETERICH-POST CLEARPRINT 1020

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-ZH PRE-PROD RELEASE				
B	ECN 9997 PRE PROD REL		CJ		
	ERN 9-RE PRODUCTION RELEASE		CJ		



SCHEMATIC: 107638

REF DWGS:

4 BEFORE INSTALLING J13 REMOVE PIN 19.

3 MARK VERSION NO AND VERSION ISSUE LETTER IN AREA SHOWN.

2 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 107640-01 REV 'B' AND SUBSEQUENT.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

104857	FT7000
NEXT ASSY	1ST USED ON
APPLICATION	

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .XXX ± ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

SIGNATURES	DATE
DR	
CHK	
DES	
ENGR	
PROJ. ENGR	

MATL: SEE L/M

PERTEC
PERIPHERAL EQUIPMENT DIVISION

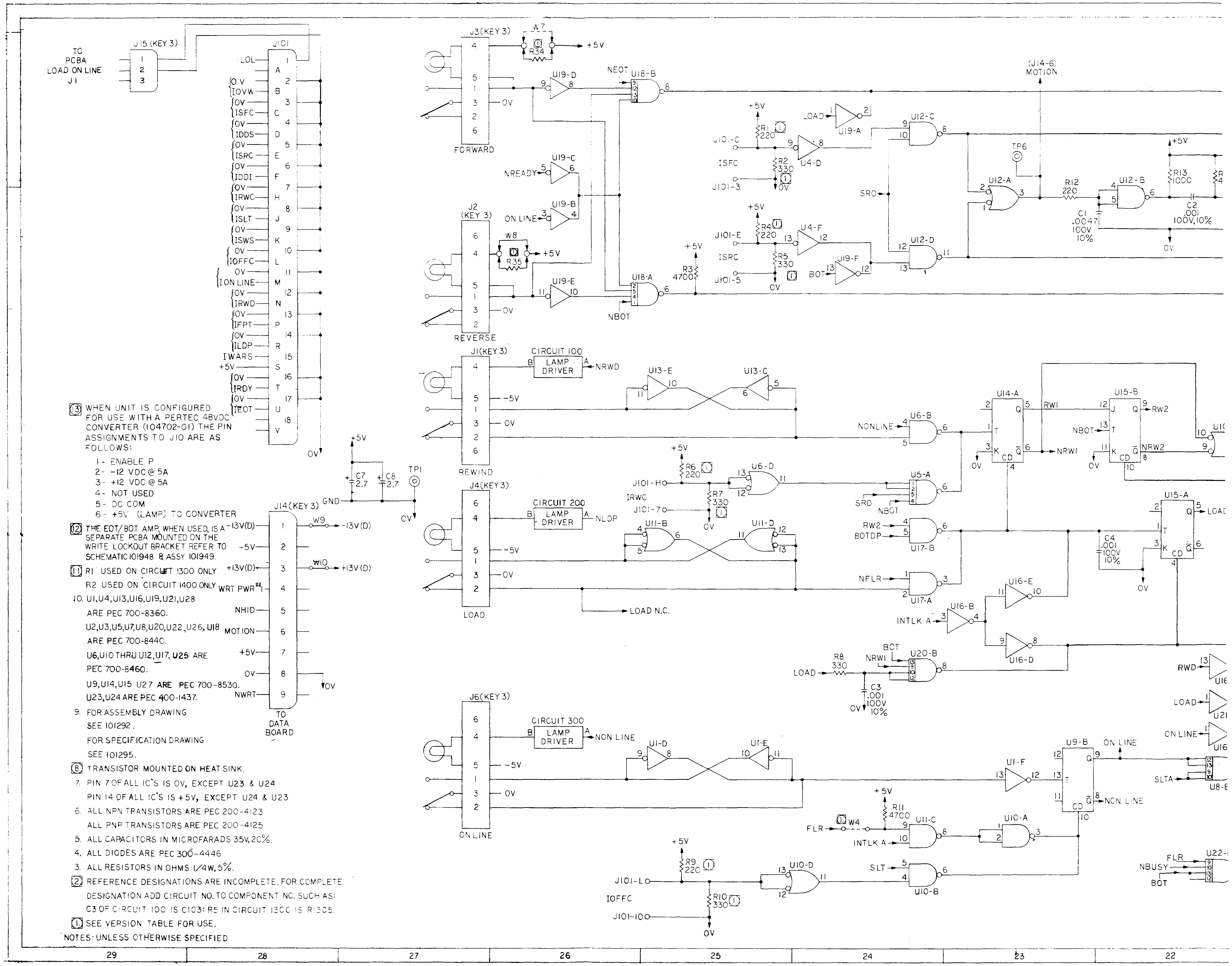
TITLE
PCBA
CABLE ADAPTER III (DC)

SIZE	CODE IDENT NO.	DWG NO.	REV
D	32097	107639	B

SCALE 2/1 DO NOT SCALE DWG SHEET 1 OF 1

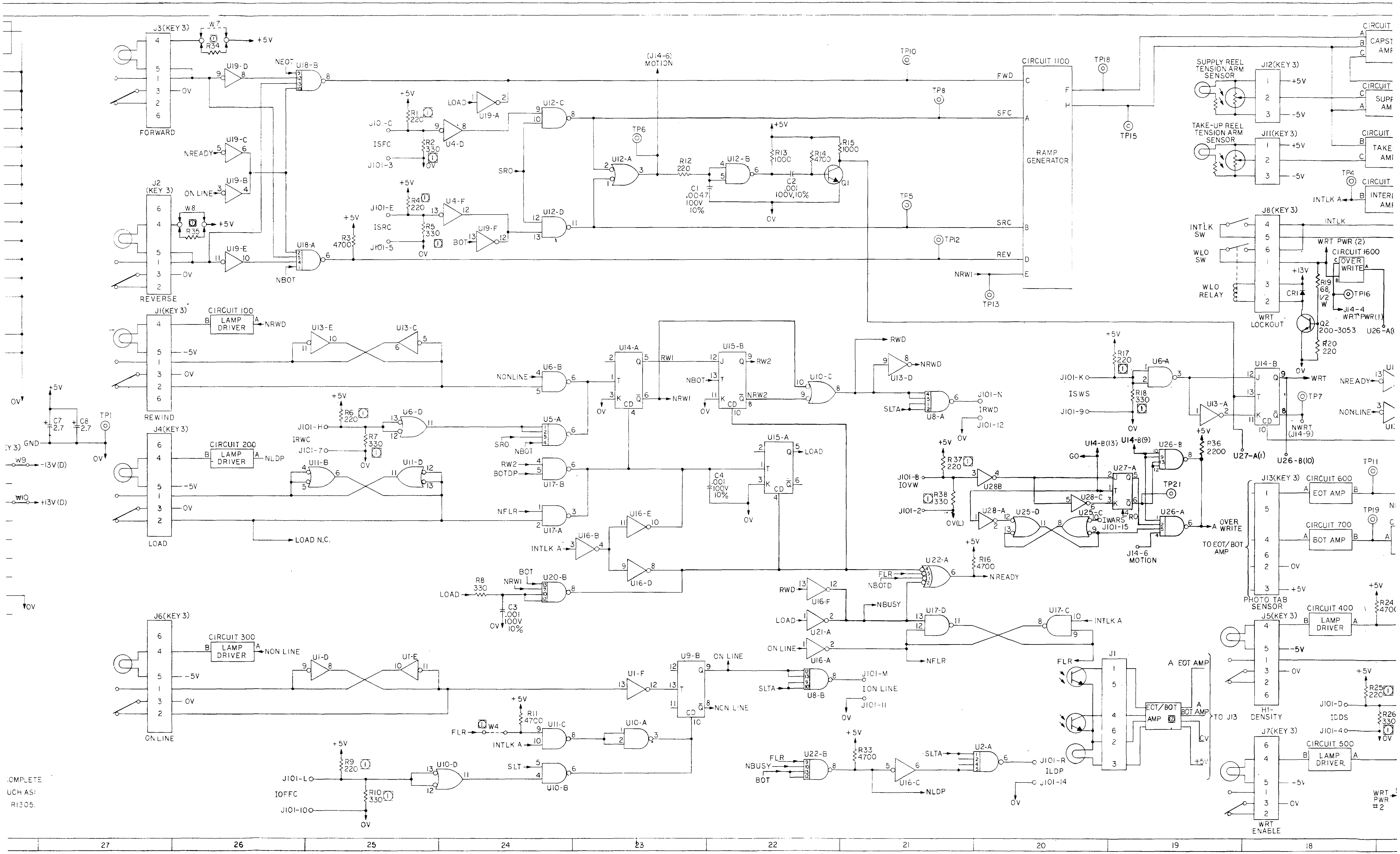
DWG. NO. 107639 REV. B

PRINTED ON DIETERICH-POST CLEARPRINT 1020

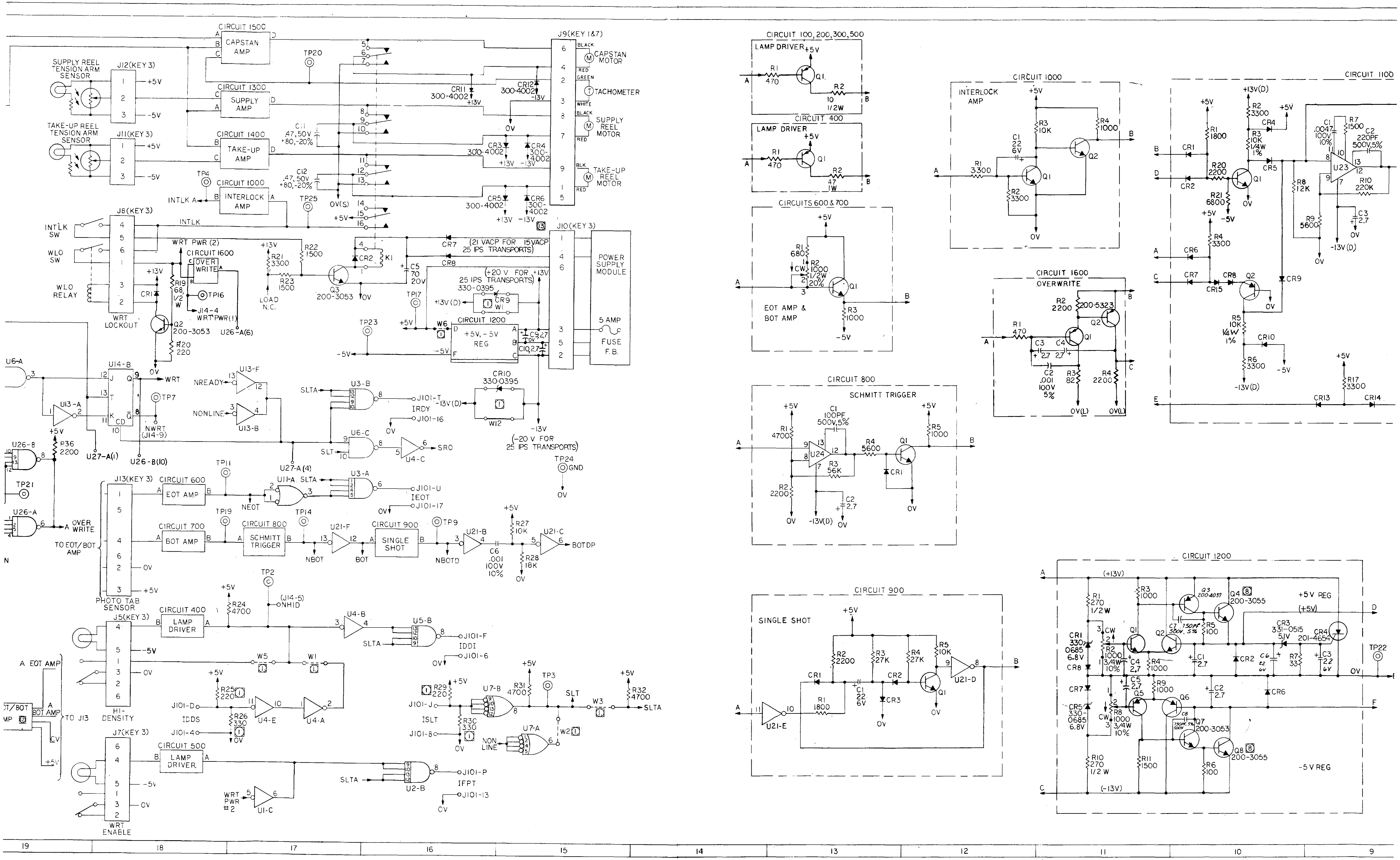


13. WHEN UNIT IS CONFIGURED FOR USE WITH A PERTEC 48VDC CONVERTER (104702-01) THE PIN ASSIGNMENTS TO J10 ARE AS FOLLOWS:
   1- ENABLE P
   2- -12 VDC @ 5A
   3- +12 VDC @ 5A
   4- NOT USED
   5- DC COM
   6- +5V (LAMP) TO CONVERTER
12. THE EOT/BOT AMP, WHEN USED, IS A SEPARATE PCBA MOUNTED ON THE WRITE LOCKOUT BRACKET REFER TO SCHEMATIC 101948 & ASSY 101949.
11. R1 USED ON CIRCUIT 1300 ONLY
    R2 USED ON CIRCUIT 1400 ONLY
10. U1,U4,U13,U16,U19,U21,U28 ARE PEC 700-8360.
    U2,U3,U5,U7,U8,U20,U22,U26,U18 ARE PEC 700-8440.
    U6,U10 THRU U12, U17, U25 ARE PEC 700-8460.
    U9,U14,U15 U27 ARE PEC 700-8530.
    U23,U24 ARE PEC 400-1437.
9. FOR ASSEMBLY DRAWING SEE 101292.
   FOR SPECIFICATION DRAWING SEE 101295.
8. TRANSISTOR MOUNTED ON HEAT SINK.
7. PIN 7 OF ALL IC'S IS 0V, EXCEPT U23 & U24
   PIN 14 OF ALL IC'S IS +5V, EXCEPT U24 & U23
6. ALL NPN TRANSISTORS ARE PEC 200-4123
   ALL PNP TRANSISTORS ARE PEC 200-4125
5. ALL CAPACITORS IN MICROFARADS 35V, 20%.
4. ALL DIODES ARE PEC 300-4446
3. ALL RESISTORS IN OHMS 1/4W, 5%.
2. REFERENCE DESIGNATIONS ARE INCOMPLETE. FOR COMPLETE DESIGNATION ADD CIRCUIT NO. TO COMPONENT NO. SUCH AS: C3 OF CIRCUIT 100 IS C103; R5 IN CIRCUIT 1300 IS R1305.
1. SEE VERSION TABLE FOR USE.

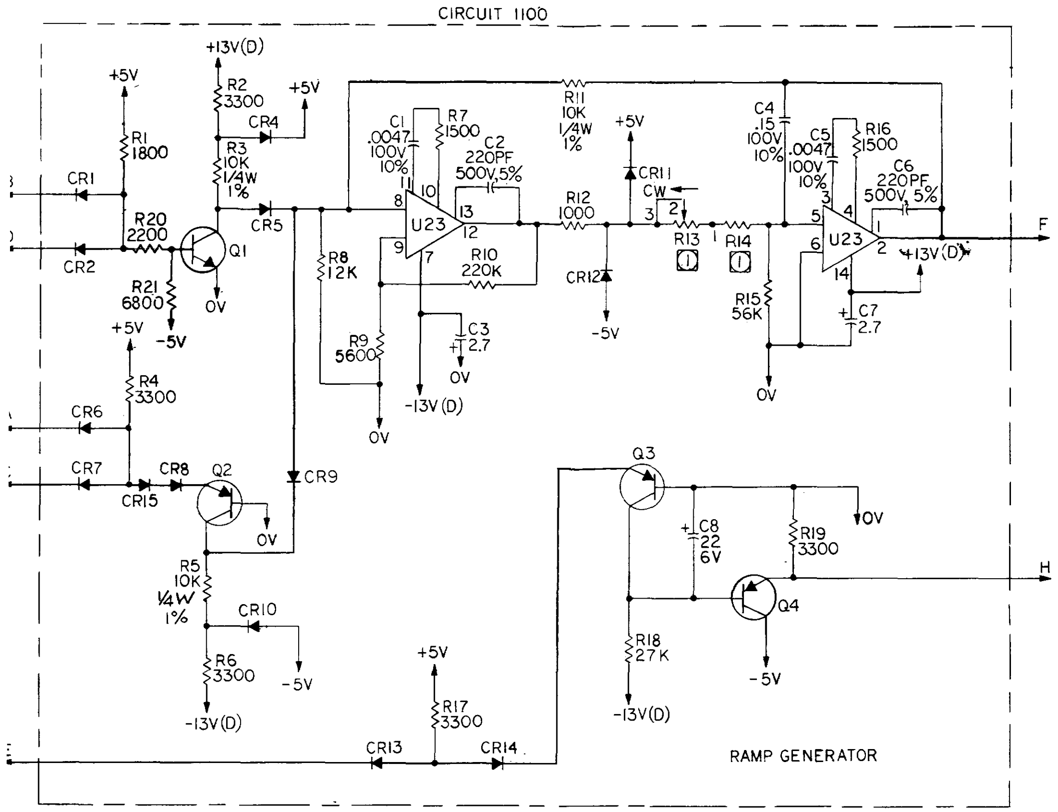
NOTES: UNLESS OTHERWISE SPECIFIED

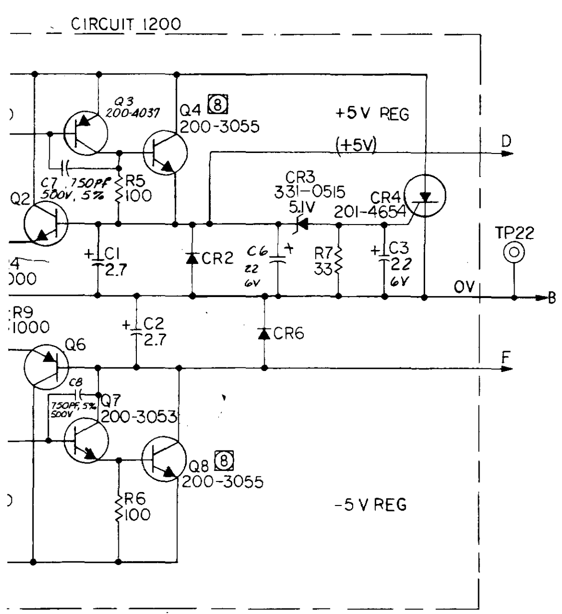


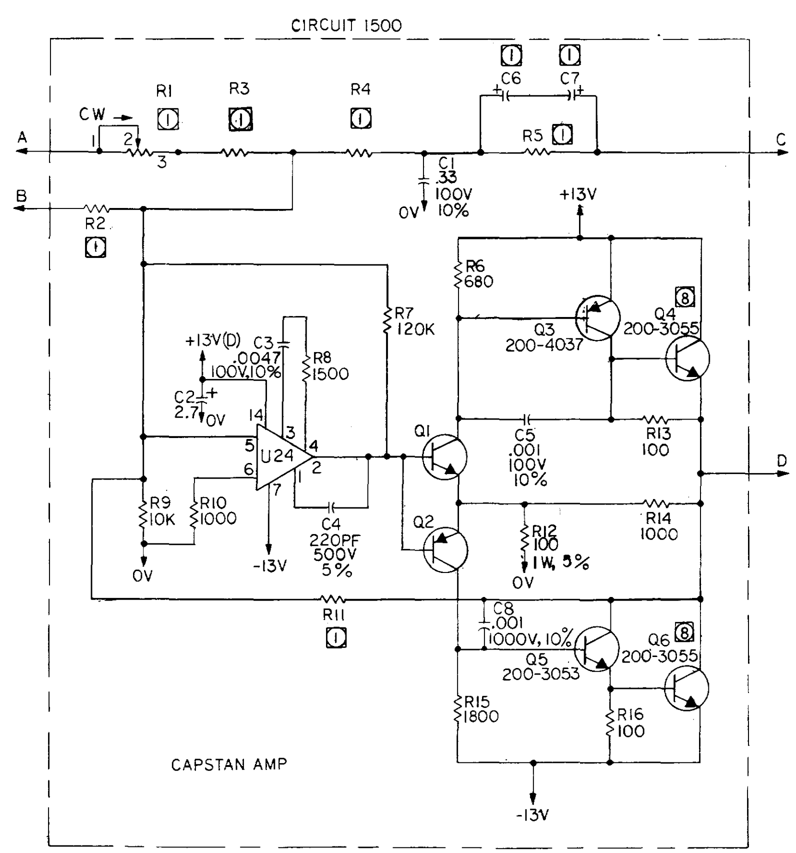
J3(KEY 3)
W7
R34
+5V
FORWARD
U19-D
NEOT
U18-B
(J14-6)
MOTION
TP10
CIRCUIT 1100
TP18
FWD
SFC
SRC
REV
NRWI
RAMP
GENERATOR
TP15
TP8
TP6
TP5
TP12
TP13
U19-C
NREADY
U19-B
ON LINE
J2
(KEY 3)
W8
R35
U19-E
U18-A
NBOT
REVERSE
LOAD
U19-A
U12-C
R1 220
U4-D
J10-C
ISFC
R2 330
J101-3
R4 220
U4-F
J101-E
ISRC
R5 330
J101-5
U19-F
BOT
R3 4700
SRO
U12-A
U12-D
R12 220
U12-B
C1 .0047 100V 10%
R13 1000
R14 4700
R15 1000
C2 .001 100V,10%
Q1
SUPPLY REEL
TENSION ARM
SENSOR
J12(KEY 3)
TAKE-UP REEL
TENSION ARM
SENSOR
J11(KEY 3)
-5V
CIRCUIT
CAPST
AMP
SUPP
AMP
TAKE
AMP
INTERL
TP4
INTLK A
J8(KEY 3)
INTLK
INTLK SW
WLO SW
WLO RELAY
WRT PWR (2)
CIRCUIT 1600
OVER WRITE
R19 68, 1/2 W
CR1
+13V
TP16
J14-4
WRT PWR(1)
WRT LOCKOUT
Q2
200-3053
U26-A(
R20 220
J1(KEY 3)
CIRCUIT 100
LAMP DRIVER
NRWD
U13-E
U13-C
REWIND
U6-B
NONLINE
U14-A
RWI
U15-B
RW2
NBOT
NRW2
U10-C
RWD
U13-D
U8-A
SLTA
J101-N
IRWD
J101-12
R17 220
U6-A
J101-K
ISWS
R18 330
J101-9
U14-B
WRT
NREADY
TP7
NWRT
(J14-9)
U13-A
NONLINE
U27-A(1)
U26-B(10)
U14-B(13)
U14-B(9)
GO
U26-B
P36 2200
U27-A
+5V
R6 220
U6-D
J101-H
IRWC
J101-7
R7 330
U5-A
SRO
NBOT
RW2
BOTDP
U17-B
J4(KEY 3)
CIRCUIT 200
NLDP
U11-B
U11-D
C4 .001 100V 10%
U15-A
LOAD
J101-B
IOVW
R37 220
U28B
R38 330
J101-2
OV(L)
U28-C
U28-A
U25-D
U25-C
IWARS
J101-15
RO
U26-A
OVER WRITE
TP21
J14-6
MOTION
TO EOT/BOT AMP
J13(KEY 3)
CIRCUIT 600
EOT AMP
TP11
CIRCUIT 700
BOT AMP
TP19
PHOTO TAB SENSOR
NFLR
U17-A
LOAD N.C.
U16-E
U16-B
INTLK A
U16-D
R8 330
LOAD
NRWI
U20-B
C3 .001 100V 10%
U22-A
FLR
NBOTD
R16 4700
NREADY
U16-F
NBUSY
U21-A
U17-D
U17-C
INTLK A
U16-A
NFLR
J1
A EOT AMP
EOT/BOT AMP
A BOT AMP
TO J13
J5(KEY 3)
CIRCUIT 400
R24 4700
HI-DENSITY
R25 220
J101-D
IDDS
R26 330
J101-4
J7(KEY 3)
CIRCUIT 500
WRT ENABLE
WRT PWR #2
J6(KEY 3)
CIRCUIT 300
NON LINE
U1-D
U1-E
ON LINE
U1-F
U9-B
ON LINE
NON LINE
U8-B
J101-M
ION LINE
J101-11
R11 4700
W4
FLR
U11-C
INTLK A
U10-A
SLT
U10-B
U10-D
R9 220
J101-L
IOFFC
R10 330
J101-10
U22-B
NBUSY
BOT
R33 4700
U16-C
NLDP
U2-A
J101-R
ILDP
J101-14
+5V
C7 2.7
C8 2.7
TP1
GND
W9
-13V(D)
W10
+13V(D)
OV
COMPLETE
UCH AS
R1305.
27
26
25
24
23
22
21
20
19
18

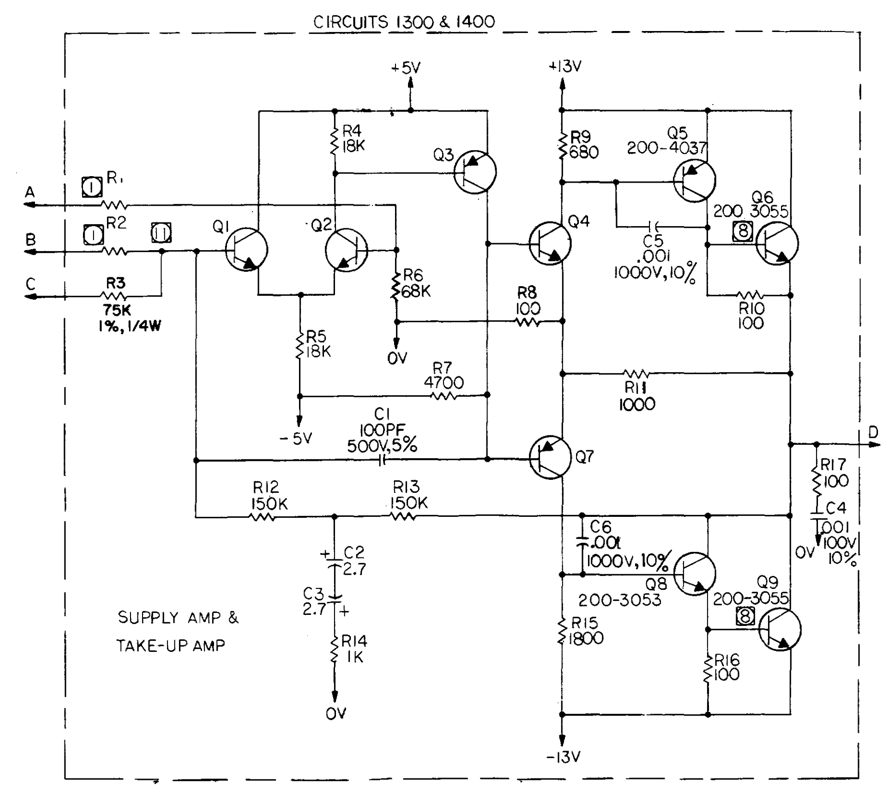


CIRCUIT 150C
CAPSTAN AMP
CIRCUIT 1300
SUPPLY AMP
CIRCUIT 1400
TAKE-UP AMP
CIRCUIT 1000
INTERLOCK AMP
SUPPLY REEL TENSION ARM SENSOR
TAKE-UP REEL TENSION ARM SENSOR
J12(KEY 3)
J11(KEY 3)
J9(KEY 1&7)
CAPSTAN MOTOR
TACHOMETER
SUPPLY REEL MOTOR
TAKE-UP REEL MOTOR
J8(KEY 3)
INTLK SW
WLO SW
WLO RELAY
WRT LOCKOUT
CIRCUIT 1600
OVER WRITE
J10(KEY 3)
POWER SUPPLY MODULE
5 AMP FUSE F.B.
(21 VACP FOR 15VACP 25 IPS TRANSPORTS)
(+20 V FOR +13V 25 IPS TRANSPORTS)
CIRCUIT 1200
+5V, -5V REG
(-20 V FOR 25 IPS TRANSPORTS)
J13(KEY 3)
CIRCUIT 600
EOT AMP
CIRCUIT 700
BOT AMP
CIRCUIT 800
SCHMITT TRIGGER
CIRCUIT 900
SINGLE SHOT
TO EOT/BOT AMP
PHOTO TAB SENSOR
J5(KEY 3)
CIRCUIT 400
LAMP DRIVER
HI-DENSITY
J7(KEY 3)
CIRCUIT 500
LAMP DRIVER
WRT ENABLE
CIRCUIT 100,200,300,500
LAMP DRIVER
CIRCUIT 400
LAMP DRIVER
CIRCUITS 600 & 700
EOT AMP & BOT AMP
CIRCUIT 800
SCHMITT TRIGGER
CIRCUIT 900
SINGLE SHOT
CIRCUIT 1000
INTERLOCK AMP
CIRCUIT 1600
OVERWRITE
CIRCUIT 1100
CIRCUIT 1200
+5V REG
-5V REG
19
18
17
16
15
14
13
12
11
10
9









REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ERN 2-NC				
C	ECN 2040		T.B		
D	ECN 2114		T.B		
E	ECN 2214		T.B		
F	ECN 2303		T.B		
G	ECN 2349B		T.B		
H	ECN 2245		T.B		
J	ECN 2365		T.B		
K	ECN 2514A		T.B		
L	ECN 2804		D.C		
M	ECN 3055				
N	ECN 3141		RAS		
P	ECN 3426				
R	ECN 3567A	6-12-72			
S	ECN 4339				RCA
T	ECN 4420				RCA
U	ECN 4509				RCA
V	ECN 5207				RCA
W	ECN 5310				RCA
Y	ECN 5604				
Z	ECN 6019				
AA	ECN 6055				
AB	ECN 6134		RAS		
AC	ECN 6347				
AD	ECN 6404				
AE	ECN 6540				
AF	ECN 7959				
AF1	ECN 8134				
AG	ECN 9340		SK		
AH	ECN 9682				
AJ	ECN 6528		J.S.		

REFERENCE DESIGNATIONS 2

LAST USED		DELETED
C1604	C12	CR1103, 1203, C1601
CR1208	CR12	
R1804	R38	
Q1602	Q3	
	U28	
	TP25	
	W12	

MODEL	FUNCTIONS
A	HI-DEN LOCAL/SELECT/ ON LINE AT BOT
B	HI-DEN LOCAL/SELECT/ ON LINE MID TAPE
C	HI-DEN LOCAL /SELECT ON LINE/ON LINE MID TAPE
D	HI-DEN REMOTE/SELECT ON LINE/ON LINE AT BOT
E	HI DEN REMOTE/SELECT ON LINE/AT BOT
F	HI DEN LOCAL/SELECT ON LINE/ON LINE AT BOT
G	HI-DEN REMOTE/SELECT ON LINE MID TAPE
H	HI-DEN REMOTE/SELECT ON LINE/ON LINE MIDTAPE
J	HI-DEN LOCAL/SELECT ON LINE/MID TAPE (FOR USE WITH "LOAD ON LINE")

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 X/X ± 1/32 ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

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SIGNATURES / DATE: DR, CHK, DES, ENGR, ENGR

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC TAPE CONTROL "BI"

NEXT ASSY	1ST USED ON
	TOP ASSY

APPLICATION

FINISH:
MATL:

SIZE J | CODE IDENT. NO. — | DWG NO. 101291 | REV AJ

SCALE — | DO NOT SCALE DWG | SHEET 1 OF 2

SPEED	MODEL	VERSION	W1	W2	W3	W4	W5	W6	W7	W8	R34,35 1/2W,5%	R1503 1/4W,1%	R1502 1/4W,5%	R1504 1505 1/4W,1%	R1511 1/4W,1%	R1114 1/4W,1%	R1113 3/4W,10%	R1301 1/4W,5%	R1402 1/4W,5%	C1506, 1507	CR9, 10	W11,12	R1501 3/4W,10%	R1,4,6,9,17,25, R29,37	R2,5,7,10,18,26, R30,38
12.5	A	-01			X	X	X	X			15	3.16K	820	2.15K	51.1K	162K	100K	220K	220K			X	2K	X	X
	B	-02			X		X	X																	
	C	-03		X	X		X	X																	
	D	-04	X	X	X	X		X																	
	E	-05	X		X	X		X																	
	F	-06		X	X	X	X	X																	
	G	-07	X		X			X																	
	H	-08	X	X	X			X			15														
12.5	J	-09			X		X	X	X	X		3.16K			51.1K	162K							2K		
6.25	A	-11			X	X	X	X			15	5.11K			42.2K	422K							5K		
	B	-12			X		X	X																	
	C	-13		X	X		X	X																	
	D	-14	X	X	X	X		X																	
	E	-15	X		X	X		X																	
	F	-16		X	X	X	X	X																	
	G	-17	X		X			X																	
	H	-18	X	X	X			X			15														
6.25	J	-19			X		X	X	X	X		5.11K	820		42.2K	422K									
18.75	A	-21			X	X	X	X			15	2.87K	1.2K		75K	75K				2.7					
	B	-22			X		X	X																	
	C	-23		X	X		X	X																	
	D	-24	X	X	X	X		X																	
	E	-25	X		X	X		X																	
	F	-26		X	X	X	X	X																	
	G	-27	X		X			X																	
	H	-28	X	X	X			X			15														
18.75	J	-29			X		X	X	X	X			1.2K	2.15K	75K		100K	220K	220K			X			
25	A	-31			X	X	X	X			15		1.5K	750	287K		50K	82K	120K		X				
	B	-32			X		X	X																	
	C	-33		X	X		X	X																	
	D	-34	X	X	X	X		X																	
	E	-35	X		X	X		X																	
	F	-36		X	X	X	X	X																	
	G	-37	X		X			X																	
	H	-38	X	X	X			X			15														
25	J	-39			X		X	X	X	X		2.87K	1.5K	750	287K	75K	50K	82K	120K	2.7	X		5K	X	X
12.5	A	-41			X	X	X	X			15	3.16K	820	2.15K	51.1K	162K	100K	220K	220K			X	2K		
	B	-42			X		X	X																	
	C	-43		X	X		X	X																	
	D	-44	X	X	X	X		X																	
	E	-45	X		X	X		X																	
	F	-46		X	X	X	X	X																	
	G	-47	X		X			X																	
	H	-48	X	X	X			X			15														
12.5	J	-49			X		X	X	X	X		3.16K			51.1K	162K							2K		
6.25	A	-51			X	X	X	X			15	5.11K			42.2K	422K							5K		
	B	-52			X		X	X																	
	C	-53		X	X		X	X																	
	D	-54	X	X	X	X		X																	
	E	-55	X		X	X		X																	
	F	-56		X	X	X	X	X																	
	G	-57	X		X			X																	
	H	-58	X	X	X			X			15														
6.25	J	-59			X		X	X	X	X		5.11K	820		42.2K	422K									
18.75	A	-61			X	X	X	X			15	2.87K	1.2K		75K	75K				2.7					
	B	-62			X		X	X																	
	C	-63		X	X		X	X																	
	D	-64	X	X	X	X		X																	
	E	-65	X		X	X		X																	
	F	-66		X	X	X	X	X																	
	G	-67	X		X			X																	
	H	-68	X	X	X			X			15														
18.75	J	-69			X		X	X	X	X			1.2K	2.15K	75K		100K	220K	220K			X			
25	A	-71			X	X	X	X			15		1.5K	750	287K		50K	82K	120K		X				
	B	-72			X		X	X																	
	C	-73		X	X		X	X																	
	D	-74	X	X	X	X		X																	
	E	-75	X		X	X		X																	
	F	-76		X	X	X	X	X																	
	G	-77	X		X			X																	
	H	-78	X	X	X			X			15														
25	J	-79			X		X	X	X	X		2.87K	1.5K	750	287K	75K	50K	82K	120K	2.7	X		5K		

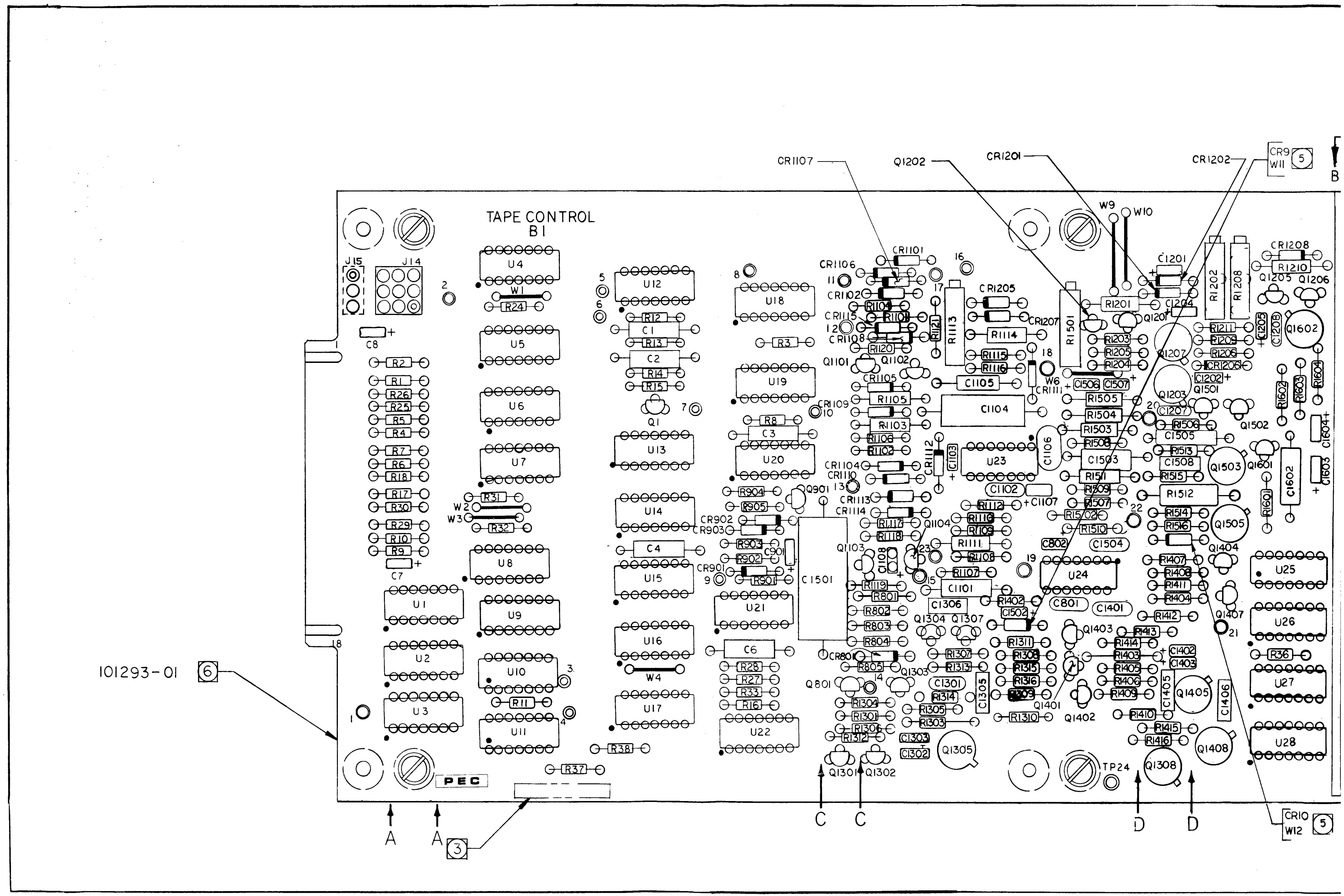
(NOTES: 'X' INDICATES USED)

R1402 1/4W,5%	C1506, 1507	CR9, 10	W11,12	R1501 3/4W,10%		R1,4,6,9,17,25, R29,37	R2,5,7,10,18,26, R30,38
220K			X	2K		X	X
				2K			
				5K			
	2.7						
220K			X				
120K		X					
120K	2.7	X		5K		X	X
220K			X	2K			
				2K			
				5K			
	2.7						
220K			X				
120K		X					
120K	2.7	X		5K			

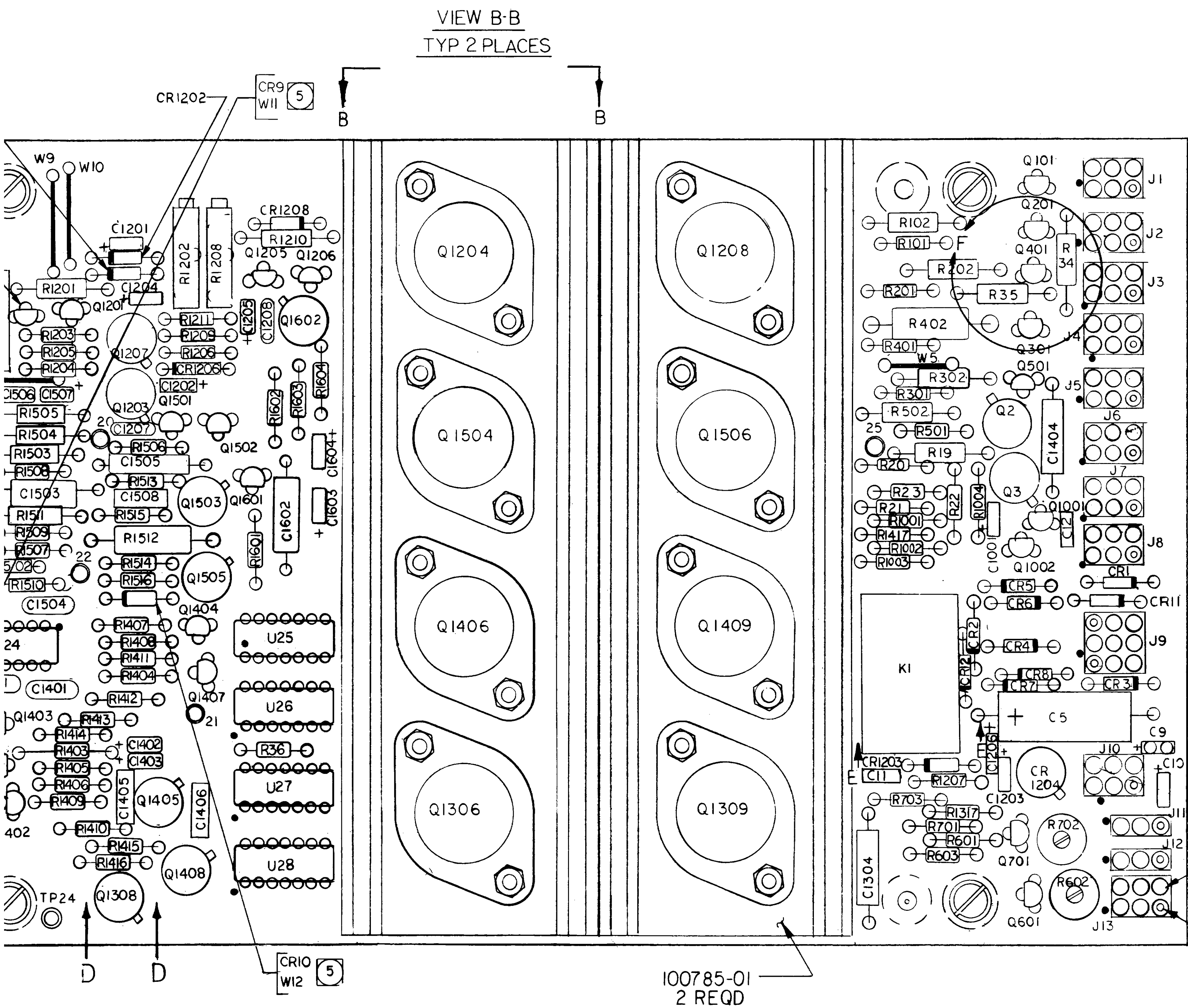
REVISIONS

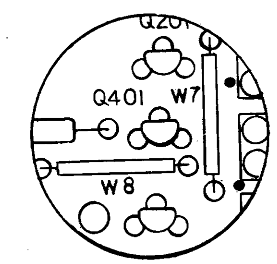
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHT. 1				

SIZE	CODE IDENT NO.	DWG NO.	REV
J		101291	AJ
SCALE NONE	DO NOT SCALE DWG	SHEET 2 OF 2	



TAPE CONTROL
B1
101293-01
6
3
A
A
C
C
D
D
B
CR1107
Q1202
CR1201
CR1202
CR9
W11
5
CR10
W12
5
PEC
TP24





VIEW F 5

6 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101293-01 REV. T AND SUBSEQUENT.

5 FOR PART NO'S. AND USAGE OF COMPONENTS WHICH AFFECTED BY VERSION NO. SEE TABLE II.

4 FOR PART NO S. WHICH ARE NOT AFFECTED BY VERS NO. SEE TABLE I.

3 RUBBER STAMP ASSY PART NO INCLUDING VERSION NO AND ISSUE LETTER.

2 ASSEMBLE PER STANDARD MANUFACTURING METHODS

1 REF DRAWINGS: SCHEMATIC-101291
SPECIFICATION-101295

NOTES: UNLESS OTHERWISE SPECIFIED

4 TABLE I

PART NO.	REF DESIGNATION
100-1015	R1205,1206,1308,1310,1316,1317 1408,1410,1416,1417, 1513,1516
100-2215	R12,20
100-3315	R8
100-6815	R601,701,1309,1409,1506
100-1025	R13,15,603,703,805,1004,1112 1203,1204, 1209,1311,1411, 1514,1414,1314,1510
100-1525	R22,23,1107, 1116,1211,1508
100-1825	R901,1315,1415,1515,1101
100-2225	R802,902,36,1120, ,1602, 1604
100-3325	R21, 1001,1002,1102,1104, 1106,1117,1119.
100-4725	R3,11,14,16,24,31,32,33,801,1307, 1407,
100-5625	R804,1109
100-1035	R27,905,1509,1003
100-3305	R1207
100-1835	R1304,1404,1305,1405,28
100-2735	R903,904,1118
100-5635	R803,1115
100-6835	R1306,1406
100-1545	R1312,1412,1313,1413
100-2245	R1110
100-1245	R1507
100-8205	R1603
100-1235	R1108
104-1002	R1105,1111,1103
100-4715	R101, 201, 301, 401, 501,1601

TABLE

PART NO.	
123-1020	R60
121-1020	R120
130-7515	C1
135-4742	C11,1
101-1005	R102
102-4705	R402
104-7502	R130
101-6805	R19
331-0515	CR12
101-2715	R120
130-1015	C80
130-2215	C110
131-1020	C2,
131-4720	C1,1
131-1540	C110
131-3340	C15
132-2752	C7,8 1204,1 150
132-2262	C90
133-7060	C5
135-1002	C130
200-4123	Q1,6 1101 130
200-4125	Q10 1104 1102
200-4037	Q12
200-3053	Q2,
200-3055	Q12 140
201-4654	CR1
200-5323	Q16

BE MADE FROM PROCESS BOARD
AND SUBSEQUENT.

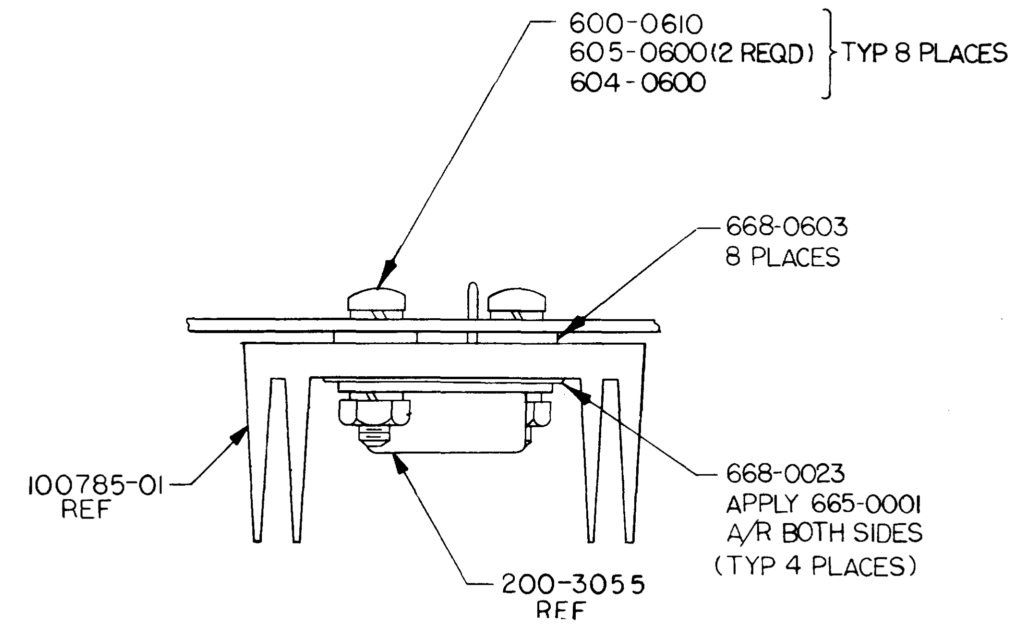
AND USAGE OF COMPONENTS WHICH ARE
ION NO. SEE TABLE II.

HICH ARE NOT AFFECTED BY VERSION

SY PART NO INCLUDING VERSION NO.
R.

ANDARD MANUFACTURING METHODS.

CHEMATIC- 101291
PECIFICATION-101295
ERWISE SPECIFIED



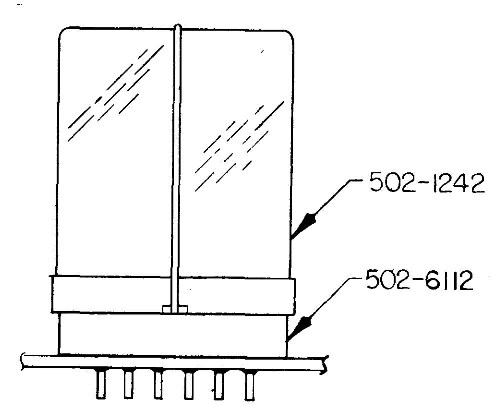
...NATION
...8,1310,1316,1317 ...417, 1513,1516
...1409,1506
805,1004,1112 1209,1311,1411, ...510
1515,1101
1120, ,1602,
...02,1102,1104,
...,32,33,801,1307,
1003
...5,1405,28
...3,1413
...
401, 501,1601

TABLE I

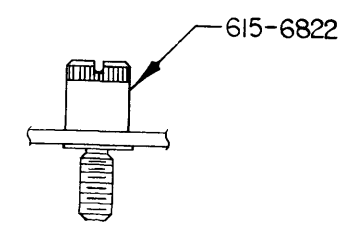
PART NO.	REF DESIGNATION
123-1020	R602,702
121-1020	R1208,1202
130-7515	C1207, 1208
135-4742	C11,12
101-1005	R102,202, 502,302
102-4705	R402
104-7502	**R1303,1403**
101-6805	R19
331-0515	CR1203
101-2715	R1201, 1210
130-1015	C801,1301, 1401
130-2215	C1102,1106,1504
131-1020	C2,3,4,6, 1505, 1602,1304,1404
131-4720	C1,1101,1105,1503,
131-1540	C1104
131-3340	C1501
132-2752	C7,8,9,10,802,1103,1107,1201,1202 1204,1205,1302,1402,1303,1403, 1502,1603,1604
132-2262	C901,1001,C1108 C1203, C1206
133-7060	C5
135-1002	C1305,1306,1405,1406,1508
200-4123	Q1,601,701,801,901,1001,1002 1101,1201, 1202, 1301, 1302, 1304,1401,1402,1404,1501
200-4125	Q101,201,301,401,501,1103, 1104,1205,1206,1303,1307, 1102,1403,1407,1502,1601,
200-4037	Q1203,1305,1405,1503
200-3053	Q2,3,1207,1308,1408,1505
200-3055	Q1204,1208,1306,1309,1406, 1409, 1504,1506
201-4654	CR1204
200-5323	Q1602

TABLE I

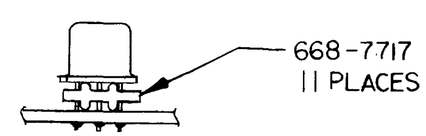
PART NO.	REF DESIGNATION
330-0685	CR1201, 1205
300-4002	CR3,4,5,6,11,12
300-4446	CR1,2,7,8,801,901,902,903 1101, 1102,1202,1206,1207, 1208,1104-1115
400-1437	U23, 24
700-8530	U9,14,15,27
700-8460	U6,10,11,12,17,25
700 8440	U2,3,5,7, 8,18,20,22,26
700-8360	U1,4,13,16,19,21,28
502-1242	K1
102-1015	R1512
100-6825	R1121
100373-01	W9,10



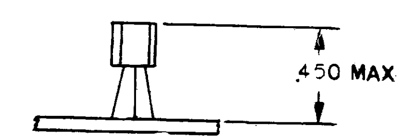
VIEW E-E
NO SCALE



VIEW A-A
TYP 6 PLACES



VIEW D-D
TYP TRANSISTOR MTG
TO 5 CASE



VIEW C-C
TYP TRANSISTOR MTG HEIGHT (TO-92)

REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ERN 2-NC	8/5/70	F.L.	[illegible]	[illegible]
C	ECN 2114	12/2/70	T.B	[illegible]	[illegible]
D	ECN 2207	2/4/71	T.E	[illegible]	TCL
E	ECN 2256	2/4/71	T.B	[illegible]	TCL
F	ECN 2303	2/4/71	T.B	[illegible]	TCL
G	ECN 2349A	2/4/71	T.B	[illegible]	TCL
H	ECN 2246D REPLACES REV G WITH CHANGE	2/4/71	T.B	[illegible]	[illegible]
J	ECN 2364	3/8/71	T.B	[illegible]	[illegible]
K	ECN 2514A | K1 | ECN 3238	9/12/71	T.B.	[illegible]	[illegible]
L	ECN 2804	10/20/71	D.C	JBR	[illegible]
M	ECN 3055	2/7/72	[illegible]	L.B.	[illegible]
N	ECN 3141	2/9/72	RAS	L.B. 2-14-72	[illegible]
P	ECN 3426	3/16/72	[illegible]	L.B. 3-17-72	[illegible]
R	ECN 3567A	6-12-72	D.C	[illegible] 6-12-72	[illegible]
S	ECN 4339	10-13-72	[illegible]	KJK	RCA
T	ECN 4420	11-27-72	D.C	[illegible]	RCA
U	ECN 4509	10-17-72	[illegible]	JBR	RCA
U1	ECN 5192	7/13/73	[illegible]	JBR	[illegible]
V	ECN 5395	8/1/73	J.L.	JBR	[illegible]
W	ECN 5310	8/22/73	[illegible]	JBR	RCA
Y	ECN 5604	9/26/73	[illegible]	[illegible]	[illegible]
Z	ECN 6019	3/6/74	[illegible]	JBR	[illegible]
AA	ECN 6055	2/24/74	J.L.	JBR	[illegible]
AB	ECN 5772	4/16/74	S.L.	JBR	[illegible]
AC	ECN 6347	5/17/74	[illegible]	CCA	[illegible]
AD	ECN 6404	6/19/74	[illegible]	CCA	[illegible]
AE	ECN 6540	9/18/74	[illegible]	[illegible]	[illegible]
AF	ECN 7959	12/18/75	[illegible]	[illegible]	[illegible]
AG	ECN 9340	12/15/76	SK	[illegible]	[illegible]
AH	ECN 9682	3/2/77	[illegible]	[illegible]	[illegible]
AJ	ECN 6528	5/11/77	J.S.	[illegible]	[illegible]

H

G

PART NO. 101292-16 REV A

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR
.XXX ± .005 ± 1/2°
$\frac{X}{X} \pm \frac{1}{32}$
BREAK ALL SHARP CORNERS
APPROX. .010

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE

SIGNATURES | DATE
DR
CHK
DES
ENGR
ENGR

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA — TAPE CONTROL B1

TOP ASSY	7000
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:
MATL:

SIZE E | CODE IDENT. NO | DWG NO. 101292 | REV AJ
SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 2

2 1

A

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
—	SEE SHT. 1	—	—	—	—

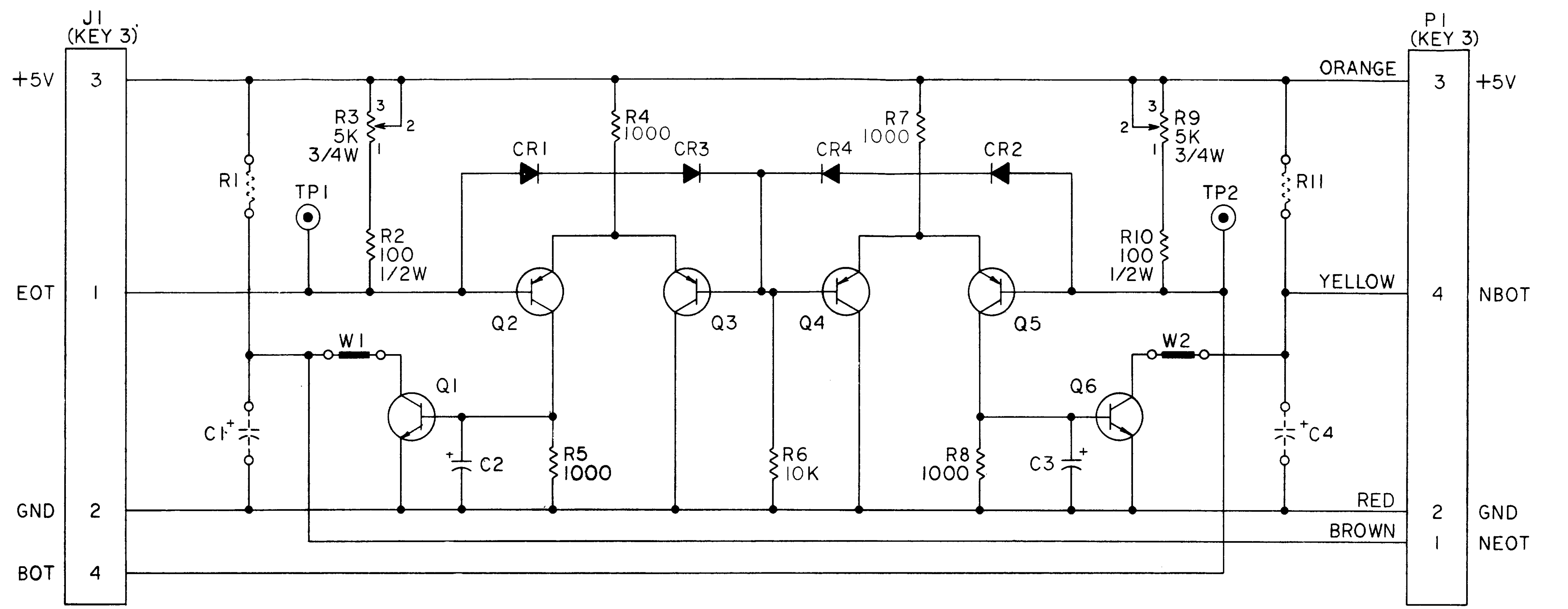
TABLE II

SPEED (IPS)	ASSEMBLY	W1	W2	W3	W4	W5	W6	W7	W8	R34,35	R1503	R1502	R1504,1505	R1511	R1114	R1113	R1301	R1402	C1506,1507	CR9,10	W11,12	R1501	R1,4,6,9,17,25, R29,37	R2,5,7,10,18,26, R30,38
12.5	101292-01			X	X	X	X			101-1505	104-3161	100-8215	104-2151	104-5112	104-1623	121-1040	100-2245	100-2245			X	121-2020	100-2215	100-3315
	-02			X		X	X																	
	-03		X	X		X	X																	
	-04	X	X	X	X		X																	
	-05	X		X	X		X																	
	-06		X	X	X	X	X																	
	-07	X		X			X																	
	-08	X	X	X			X			101-1505														
12.5	-09			X		X	X	⊗	⊗		104-3161			104-5112	104-1623							121-2020		
6.25	-11			X	X	X	X			101-1505	104-5111			104-4222	104-4223							121-5020		
	-12			X		X	X																	
	-13		X	X		X	X																	
	-14	X	X	X	X		X																	
	-15	X		X	X		X																	
	-16		X	X	X	X	X																	
	-17	X		X			X																	
	-18	X	X	X			X			101-1505														
6.25	-19			X		X	X	⊗	⊗		104-5111	100-8215		104-4222	104-4223									
18.75	-21			X	X	X	X			101-1505	104-2871	100-1225		104-7502	104-7502				132-2752					
	-22			X		X	X																	
	-23		X	X		X	X																	
	-24	X	X	X	X		X																	
	-25	X		X	X		X																	
	-26		X	X	X	X	X																	
	-27	X		X			X																	
	-28	X	X	X			X			101-1505														
18.75	-29			X		X	X	⊗	⊗			100-1225	104-2151	104-7502		121-1040	100-2245	100-2245			X			
25	-31			X	X	X	X			101-1505		100-1525	104-7500	104-2873		121-5030	100-8235	100-1245		330-0395				
	-32			X		X	X																	
	-33		X	X		X	X																	
	-34	X	X	X	X		X																	
	-35	X		X	X		X																	
	-36		X	X	X	X	X																	
	-37	X		X			X																	
	-38	X	X	X			X			101-1505														
25	-39			X		X	X	⊗	⊗		104-2871	100-1525	104-7500	104-2873	104-7502	121-5030	100-8235	100-1245	132-2752	330-0395		121-5020	100-2215	100-3315
12.5	-41			X	X	X	X			101-1505	104-3161	100-8215	104-2151	104-5112	104-1623	121-1040	100-2245	100-2245			X	121-2020		
	-42			X		X	X																	
	-43		X	X		X	X																	
	-44	X	X	X	X		X																	
	-45	X		X	X		X																	
	-46		X	X	X	X	X																	
	-47	X		X			X																	
	-48	X	X	X			X			101-1505														
12.5	-49			X		X	X	⊗	⊗		104-3161			104-5112	104-1623							121-2020		
6.25	-51			X	X	X	X			101-1505	104-5111			104-4222	104-4223							121-5020		
	-52			X		X	X																	
	-53		X	X		X	X																	
	-54	X	X	X	X		X																	
	-55	X		X	X		X																	
	-56		X	X	X	X	X																	
	-57	X		X			X																	
	-58	X	X	X			X			101-1505														
6.25	-59			X		X	X	⊗	⊗		104-5111	100-8215		104-4222	104-4223									
18.75	-61			X	X	X	X			101-1505	104-2871	100-1225		104-7502	104-7502				132-2752					
	-62			X		X	X																	
	-63		X	X		X	X																	
	-64	X	X	X	X		X																	
	-65	X		X	X		X																	
	-66		X	X	X	X	X																	
	-67	X		X			X																	
	-68	X	X	X			X			101-1505														
18.75	-69			X		X	X	⊗	⊗			100-1225	104-2151	104-7502		121-1040	100-2245	100-2245			X			
25	-71			X	X	X	X			101-1505		100-1525	104-7500	104-2873		121-5030	100-8235	100-1245		330-0395				
	-72			X		X	X																	
	-73		X	X		X	X																	
	-74	X	X	X	X		X																	
	-75	X		X	X		X																	
	-76		X	X	X	X	X																	
	-77	X		X			X																	
	-78	X	X	X			X			101-1505														
25	101292-79			X		X	X	⊗	⊗		104-2871	100-1525	104-7500	104-2873	104-7502	121-5030	100-8235	100-1245	132-2752	330-0395		121-5020		

NOTE: X INDICATES 100373-02 USED
⊗ INDICATES 100373-01 USED

SIZE	CODE IDENT NO.	DWG NO.	REV
E		101292	AJ
SCALE 2/1		DO NOT SCALE DWG	SHEET 2 OF 2

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 2-UG	9/24/70			
B	ECN 4726A	1-10-73			RCA
C	ECN 5105	5-2-73	C.W.		RCA



6. ALL DIODES ARE PEC 300-4446.
5. ALL PNP TRANSISTORS ARE PEC 200-4125.
4. ALL NPN TRANSISTORS ARE PEC 200-4123.
3. ALL RESISTORS ARE 1/4W, ±5%.
2. ALL CAPACITORS ARE 2.7UF, 35V, ±20%.
1. REFERENCE DRAWINGS: ASSEMBLY–101949
SPECIFICATION–101952

NOTES: UNLESS OTHERWISE SPECIFIED:

NEXT ASSY	1ST USED ON
101136	6000
100800	7000
101129	6000

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
$\frac{X}{X} \pm \frac{1}{32}$
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010
FINISH:

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE.

SIGNATURES	DATE
DR Z. Z. Smith	9/24/70
CHK	9/24/70
DES	
ENGR	9/24
ENGR	9/24/70

MATL:

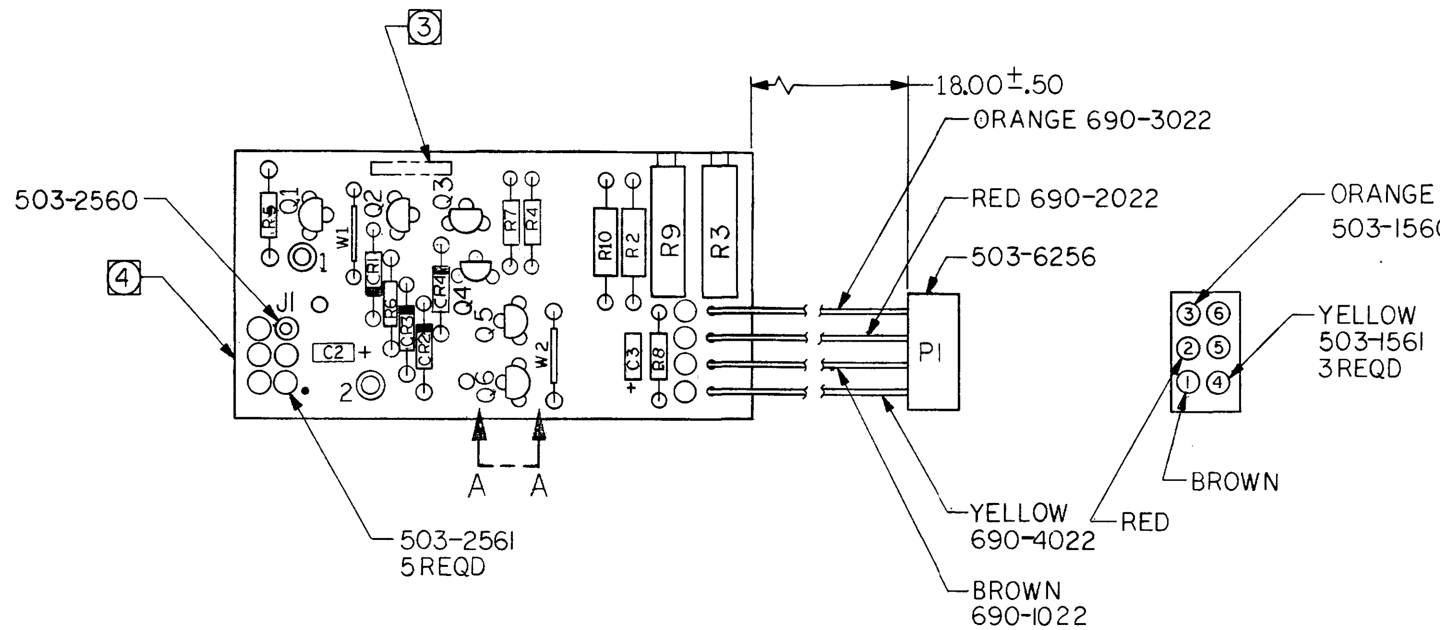
PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC
EOT/BOT AMPLIFIER

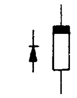
SIZE D | CODE IDENT. NO. | DWG NO. 101948 | REV C

SCALE | DO NOT SCALE DWG | SHEET | OF

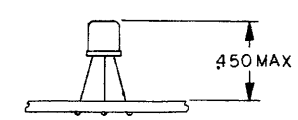
REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ERN 2-UG	5-22-70			
C	ECN 2096		T.B		
D	ECN 4726A	1-10-73			
E	ECN 5105	5-2-73			R.A
F	ECN 5930				
G	ECN 5703				



PART NO.	REF DESIGNATION
100-1025	R4,5,7,8
100-1035	R6
101-1015	R2,10
121-5020	R3,9
132-2752	C2,3
200-4123	Q1,6
200-4125	Q2, 3, 4, 5
300-4446	CR1,2,3,4
10037302	W1, 2



DIODE ORIENTATION



TYP TRANSISTOR MTG HEIGHT
VIEW A-A

PART NO. 101949- 01 REV G

4 THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 101950-01 REV G AND SUBSEQUENT.
3 MARK PART NO. 101949 INCLUDING VERSION NO. AND VERSION ISSUE LETTER
2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.
1. REFERENCE DRAWINGS: SCHEMATIC 101948
SPECIFICATION 101952

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY	1ST USED ON
101136	6000
100800	7000
101129	6000

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 $\frac{X}{X} \pm \frac{1}{32}$ ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010
FINISH:

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE.

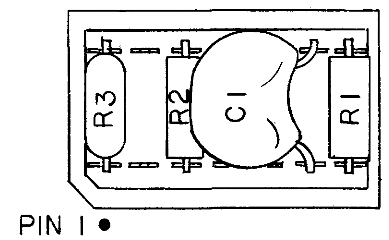
SIGNATURES / DATE
DR 9/21/70
CHK
DES
ENGR
ENGR
MATL:

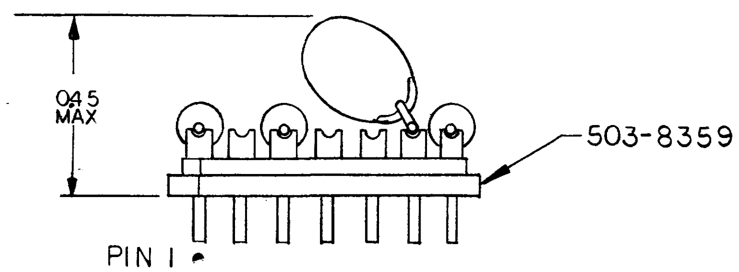
PEC PERIPHERAL EQUIPMENT CORPORATION

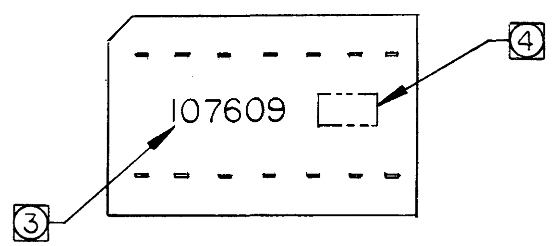
TITLE PCBA EOT/BOT AMPLIFIER

SIZE D | DWG NO. 101949 | REV G
SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-WU PROD. RELEASE	9/29/76	TGM		EB
B	ECN 9707	3/16/77	TGM		BP







ASSY VERSION NO.	TAPE SPEED (IPS)	2 C1		1 R1		1 R2		1 R3	
		VALUE (PF)	PART NO.	VALUE (OHM)	PART NO.	VALUE (OHM)	PART NO.	VALUE (OHM)	PART NO.
-01	12.5	750	130-7515	2370	107-2371	3480	107-3481	1620	107-1621
-02	18.75	750	130-7515	1210	107-1211	1780	107-1781	825	107-8250
-03	22.5	470	130-4715	1960	107-1961	1960	107-1961	909	107-9090
-04	25	470	130-4715	1620	107-1621	1470	107-1471	681	107-6810
-05	37.5	330	130-3315	1470	107-1471	1000	107-1001	464	107-4640
-06	45	330	130-3315	1100	107-1101	750	107-7500	348	107-3480
-07	75	220	130-2215	750	107-7500	348	107-3480	162	107-1620
-08	112.5	100	130-1015	1470	107-1471	316	107-3160	147	107-1470
-09	125	100	130-1015	1100	107-1101	261	107-2610	121	107-1210

4 MARK VERSION NO. & REV LEVEL AS SHOWN.

3 MARK ASSEMBLY NO. AS SHOWN.

2 CAPACITORS ARE ±5%, 500 WDC.

1 RESISTORS ARE ±1%, 1/8W.

NOTES: UNLESS OTHERWISE SPECIFIED

TOP BILL	FT8000A
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

MATL:

SIGNATURES		DATE
DR.	T. Morton	9/29/76
CHK	Larry Tollen	11/5/76
DES		
ENGR		
PROJ. ENGR	E. Ouellette	11/3/76

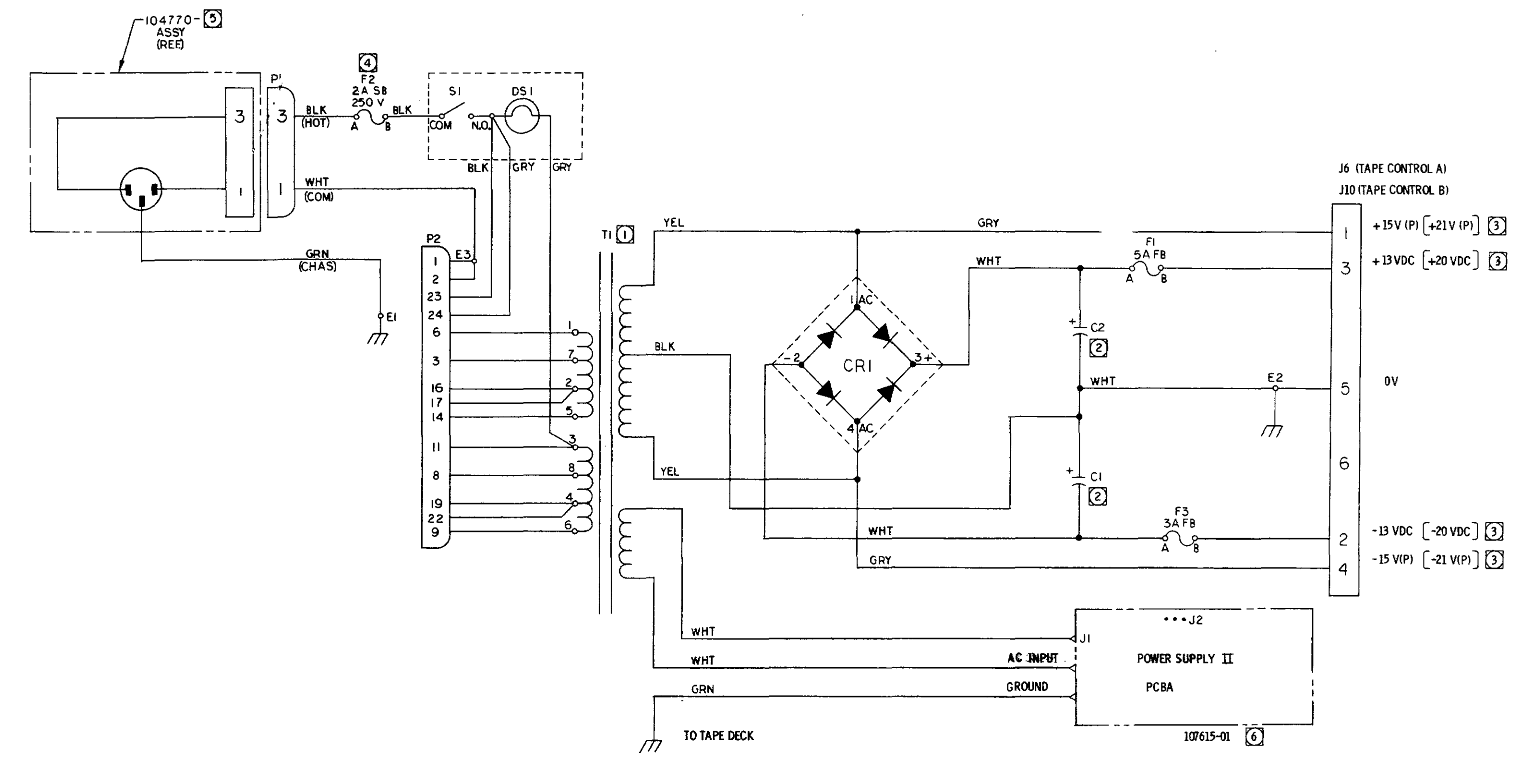
PERTEC
PERIPHERAL EQUIPMENT DIVISION

TITLE
PLUG ASSY, MICROFORMATTER TRACKING OSCILLATOR

SIZE	CODE IDENT NO.	DWG NO.	REV
C		107609	B
SCALE 4-1		DO NOT SCALE DWG	SHEET 1 OF 1

REV. B
DWG. NO. 107609

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-ZL PRE. PROD. RELEASE	11/2/76			
B	ECN 9458	2/14/77			B.P.
	ERN 9-NY PROD RELEASE				
C	ECN 10717	10-26-77			



1 TABLE I

VOLTAGE VARIATIONS	
LINE VOLTS	USE CODED PLUG
95	104586-01
105	104586-02
115	104586-03
125	104586-04
190	104586-05
200	104586-06
210	104586-07
220	104586-08
230	104586-09
240	104586-10
250	104586-11

2 TABLE II

VERSION	C1, C2	T1
-01	14,000	511-7001
-02	20,000	511-7251

REFERENCE DESIGNATION		
LAST USED	NOT USED	DELETED
C2		
CR1		
F3		
T1		

6 USED ON FT7000 ONLY
5 SEE SALES ORDER FOR APPLICABLE VERSION NO.
4 FUSE RATING IS THE SAME FROM 90 VAC THRU 250 VAC.
3 VOLTAGES IN [ ] APPLY TO -02 VERSION FOR 25 IPS TRANSPORT.
2 FOR VALUE AND PART NO. OF COMPONENTS AFFECTED BY VERSION NO. SEE TABLE II.
1 FOR TRANSFORMER PRIMARY CONNECTIONS SEE TABLE I.
NOTES: UNLESS OTHERWISE SPECIFIED

WIRE LIST 107659
POWER SUPPLY ASSY 107658
REFERENCE DRAWINGS

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	FIN.	REF. DES.	ITEM NO.

LIST OF MATERIAL

NEXT ASSY	USED ON
107658	FT 7000

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. G. MERRITT	10/29/76
CHK	11/9/76
DES	
ENGR	11/9/76
PROJ. ENGR	

FINISH:
MATL:

PERTEC PERIPHERAL EQUIPMENT

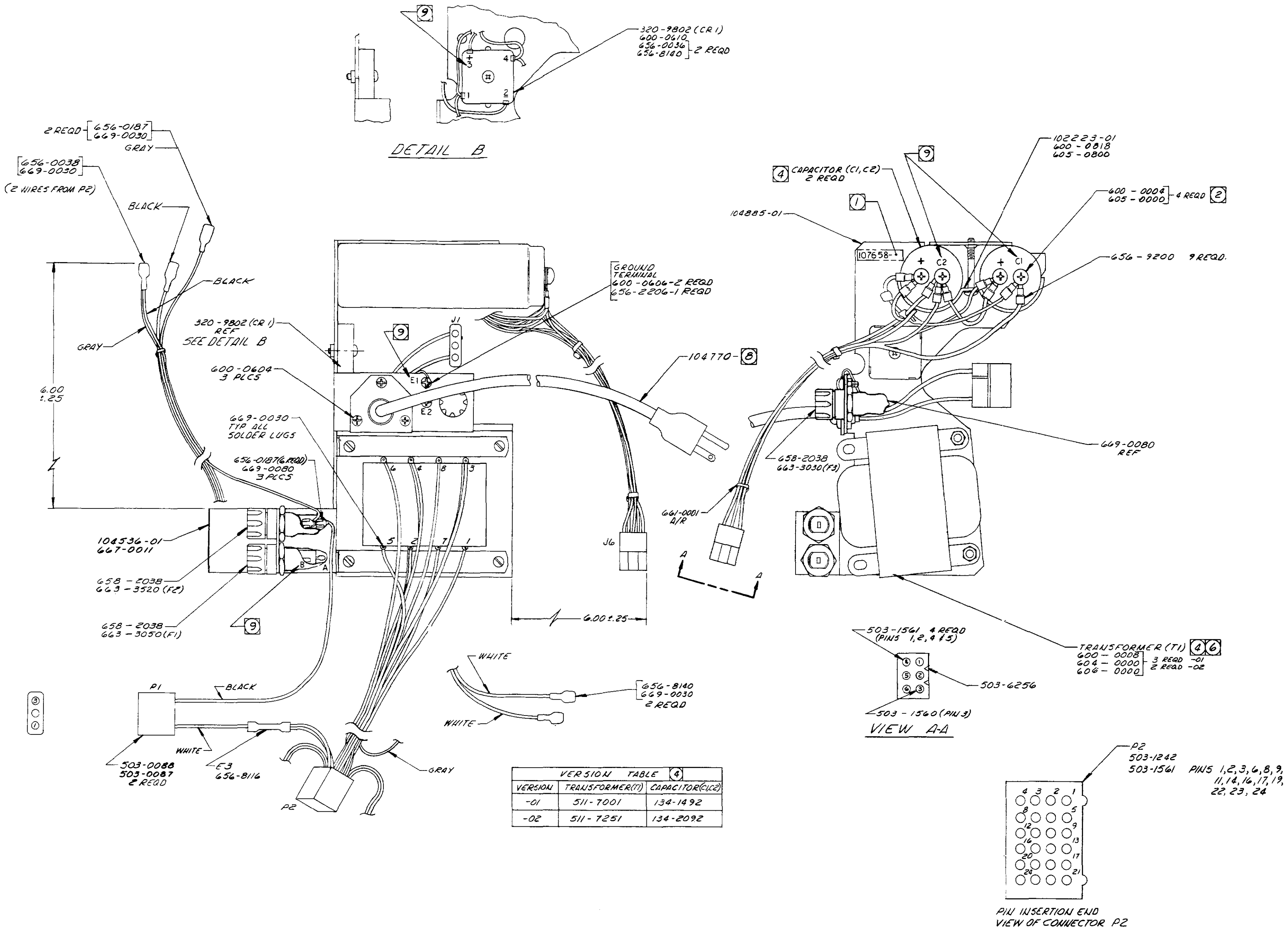
TITLE
SCHEMATIC
POWER SUPPLY
FT 7000

SIZE	CODE IDENT NO.	DWG NO.	REV
E		107657	C

SCALE — DO NOT SCALE DWG — SHEET 1 OF 1

DWG NO. 107657 REV C

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-ZL PRE PROD RELEASE				
B	ECN 9458				
C	ECN 9569				
	ERN 9-NY PROD RELEASE				
D	ECN 10717				



VERSION TABLE (4)		
VERSION	TRANSFORMER (T1)	CAPACITOR (C1, C2)
-01	511-7001	134-1492
-02	511-7251	134-2092

9. REF DESIGNATIONS ARE FOR REF ONLY AND DO NOT APPEAR ON PART.
8. SEE ORDER RELEASE FOR PROPER VERSION NO.
7. FOR WIRE LIST SEE DWG NO. 107659
6. SEE TABLE I ON SCHEMATIC 107657 FOR VOLTAGE CONNECTIONS.
5. ASSEMBLE PER STANDARD MFG. METHODS
4. FOR PART NUMBERS AFFECTED BY DASH NO. SEE VERSION TABLE.
3. FOR SCHEMATIC SEE DWG NO. 107657
2. REMOVE SUPPLIED HARDWARE AND USE THAT INDICATED.
1. MARK VERSION NO. AND VERSION ISSUE LETTER APPROX WHERE SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

106856	FT 7000
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. G MERRITT	
CHK	
DES WILLETS	
ENGR B PATEL	
PROJ. ENGR B. PATEL	

FINISH:

MATL: SEE LM

PERTEC
PERIPHERAL EQUIPMENT DIVISION

TITLE: POWER SUPPLY ASSY FT7000

SIZE: E | CODE IDENT NO. | DWG NO. 107658 | REV D
SCALE 1/1 | DO NOT SCALE DWG | SHEET 1 OF 1

APPENDIX A – GLOSSARY

Symbol	Description	Symbol	Description
B1B	Buffer 1 Busy	EPNP	Encoder Pulse Narrow Powerful
BCD10	Binary Coded Decimal	EPS	Erase Power Start
BOT	Beginning of Tape	EPW	Encoder Pulse Wide
BOTD	Beginning of Tape Delay	ERASE*	Erase
BOTDP	Beginning of Tape Delay Pulse	ES	Erase Winding Start
BOTI	Beginning of Tape Input	EWPC	Enable Write Power Control
BOTO	Beginning of Tape Output	EWRS	Enable Write/Read Status
BOV*	Buffer Overflow	FAD*	Formatter Address
CBY	Command Busy	FBY*	Formatter Busy
CCG*	Check Character Gate	FEN*	Formatter Enable
CCS	Check Character Strobe	FER*	Formatter Error
CER*	Correctable Error	FGC	File Gap Command
CHARDET*	Character Detect	FGL	File Gap Lamp
CLRNZDATA*	Clear NRZI Data	FGR	File Gap Ramp
CMP1,2	Clamp Waveform 1, 2	FLR	First Load — or Rewind
COPY*	Copy	FM	File Mark
CPI	Characters Per Inch	FMK*	File Mark
CRC0—CRC7	Cyclic Redundancy Check, Ch 0—7	FMKNZ*	File Mark NRZI
CRCC	Cyclic Redundancy Check Character	FMKPE*	File Mark PE
CRCP	Cyclic Redundancy Check Parity	FPT	File Protect
CT0—CT7	Center Tap 0—7	FWD	Forward
CTP	Center Tap Parity	GIP	Gap In Process
CT4	Count 4	GO	Motion signal delayed
CT8	Count 8	GO1*	Go
CUR	Clean-up Ramp	GRS	General Reset
CURLIM	Reel Servo Current Limit	HER*	Hard Error
D8CT	Disables 8 Count	HERNZ*	Hard Error NRZI
DBY	Data Busy	HID	Hi Density
DDI	Data Density Indicator	ID*	Identification
DDS	Data Density Select	IDGATE*	Identification Gate
DDSX	Data Density Select External	INTLK	Transport Interlock Signal
DEN*	Density	IRGC	Record Gap Command
DGATE*	Data Gate	K2ENERG	Relay K2 Energize
DI*	Data In	LD	Lamp Driver
DMC	Disable Manual Controls	LDCRC*	Load Cyclic Redundancy Check
DROPDET*	Drop Detected	LDFAIL	Load Fail
DUN	Done and Unload	LDLOOP	Load Loop
EAO	Encoder Amplifier Output	LDP	Load Point
ECC	Enable Check Character	LDWRTDATA*	Load Write Data
ECD	Echo Check Disable	LFC	Load Forward Command
ECE	Echo Check Error	LFR	Load Forward Ramp
ECLK*	Envelope Clock	LOCK	Interlock off pulse
ECO0—ECO7	Echo Check Output, Ch 0—7	LOCKA	Interlock A
ECOP	Echo Check Output Parity	LOCKB	Interlock B
ECR	Echo Check Reset	LOCKTIME	Locktime pulse
ECRC	Enable CRC	LOL*	Load-On-Line
EDIT*	Edit	LRCC	Longitudinal Redundancy Check Character
EEC	Enable Echo Check	LWD*	Last Word
EEP	Enable Encoder Pulse	MOTION	Tape Motion as result of SFC/SRC Command
EF	Erase Winding Finish	NRZ*	NRZI
EFM	Enable File Mark	OFC*	Off Line Command
ENV*	Envelope Detected	OFFC	Off-Line Input Command
EOT*	End of Tape	OFL*	Off Line
EOTI	End of Tape Input	OLUNL	Off-Line Unload
EOTO	End of Tape Output	ONEDET*	Ones Detected

NOTES:
1. * Microformatter Only
2. I Symbol Prefix = Interface Signal
3. N Symbol Prefix = Low Active Signal

APPENDIX A – GLOSSARY (Continued)

Symbol	Description	Symbol	Description
OOLL	On-Line/Off-Line Lamp	RWR	Rewind Ramp
ORD	ORed Data	RYC	Ready Command
OVW	Overwrite	SBY	Start Busy Delay
PARC*	Parity Correcting	SFC	Synchronous Forward Command
PICKK1	Pick K-1 Relay	SFCD	Synchronous Forward Command Delayed
POSTJUMP*	Postamble Jump	SFL1—SFL4	Step Forward Level 1—4
POSTEST*	Postamble Test	SGL*	Single
PR*	Parity	SHLCLK*	Shift Left Clock
PRESET*	Preset	SHRCLK*	Shift Right Clock
PSEN*	Power Supply Enable	SKLP	Seek Load Point
PSO0—PSO7	Peak Sensor Output, Ch 0—7	SKTO	Seek Time Out
PSOP	Peak Sensor Output Parity	SLT	Select Transport
PSP	Peak Sensor Parity	SPC*	Space Command
RA01, RA02	Read Amplifier Track 0, Output 1, Output 2	SPD*	Speed
RA11, etc.	Read Amplifier Track n, Output 1 or 2	SRC	Synchronous Reverse Command
RAC	Read Amplifier Clamp	SRO/SRO1	Selected—Ready—On Line
RACT	Read Amplifier Center Tap	SWS	Set Write Status
RAP1, RAP2	Read Amplifier Parity, Output 1, Output 2	TAD	Turnaround Delay
RCLK*	Read Clock	TAD0, 1*	Transport Address
RD0—RD7	Read Data, Ch 0—7	TBY	Turnaround Busy
RDI	Relay Driver Input	TENCNT	Tension Control
RDNZ*	Read NRZI Data	THR*	Read Threshold
RDP	Read Data Parity	TIP	Tape-In-Place
RDS	Read Data Strobe	TNT	Tape Not Tensioned
RDY	Ready	TRR	Transport Ready
REN*	Read Enable	WARS	Write Amplifier Reset
RENDNZ*	Read End NRZI	WCLK*	Write Clock
RENDPE*	Read End PE	WCN*	Write Control
REV	Reverse	WCRC	Write CRC
REW*	Rewind	WD*	Write Data
REW RAMP A	Rewind Ramp Output A	WD0—WD7	Write Data, Ch 0—7
REW RAMP B	Rewind Ramp Output B	WDP	Write Data Parity
REWRI	Rewind Ramp Initiate	WDS	Write Data Strobe
RF0—RF7	Read Finish 0—7	WDSN	Write Data Strobe Narrow
RFP	Read Finish Parity	WDSW	Write Data Strobe Wide
RGATENZ*	Read Gate NRZI	WF0—WF7	Write Finish, Ch 0—7
RGATEPE*	Read Gate PE	WFM	Write File Mark
RGC	Inter-Record Gap Command	WFP	Write Finish Parity
RGR	Inter-Record Gap Ramp	WLO	Write Lockout
RRS	Remote Reset	WDP	Write Power Control
RS1	Rewind Step 1	W/RF0—W/RF7	Write/Read Head Winding Finish, Ch 0—7
RSC*	Read Strobe Counter	W/RFP	Write/Read Heading Winding Finish Parity
RSP	Read Start Parity	WDO	Write/Read Output
RST	Reset	WDP	Write Pulse
RSTR*	Read Strobe	WRS	Write/Read Status
RSTRNZ*	Read Strobe NRZI	W/RS0—W/RS7	Write/Read Head Winding Start, Ch 0—7
RSTRPE*	Read Strobe PE	W/RSP	Write/Read Head Winding Start Parity
RTH	Read Threshold	WRT*	Write
RTN1	Front Panel Switches Gnd Return 1	WRT EN	Write Enable
RW1	Rewind 1 FF	WS0—WS7	Write Start, Ch 0—7
RWC	Rewind Command	WSC	Write Step Command
RWD	Rewinding	WSP	Write Start Parity
RWFWD	Rewind Forward	WSTR*	Write Strobe

Errata No. 5024
April, 1978
Microformatter Addenda:
FT1640-98 Manual No. 104933
FT7640 Manual No. 104922
FT7840 Manual No. 104923
FT8640A Manual No. 104925
FT8640A-98 Manual No. 104926
FT8840A Manual No. 104927
FT9640 Manual No. 104930
FT9640-98 Manual No. 104931
FT9840 Manual No. 104932

Make the following changes to the subject manual addendum.

1. Page 2-1, Paragraph 2.4, Interface Connections, add the following paragraph.

   The two 50-lead flat cables are not supplied by PERTEC. Two edge connectors are required and will be supplied by PERTEC upon request at no charge. Edge connector part numbers are: PERTEC P/N 503-0147; 3M P/N 3415.

SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides the physical description, functional description and specifications for the NRZI, PE, and Dual Microformatters manufactured by PCC PERTEC, Chatsworth, California.

1.2 PURPOSE OF EQUIPMENT

The microformatter, in conjunction with the companion PERTEC tape transport, enables the generation and decoding of ANSI compatible 9-track NRZI (800 cpi) and ANSI compatible PE (1600 cpi) tapes. All timing and control necessary for the recording and reproduction of NRZI or PE data are also provided by the microformatter.

The model numbers for formatter tape transport systems are given in Table 1-1. The system is comprised of a PERTEC tape transport and an internally mounted microformatter.

1.3 PHYSICAL DESCRIPTION

The Microformatter PCBA is mounted within the PERTEC tape transport as illustrated in Section II of the companion Operating and Service Manual. An additional 5-volt regulator is added to the transport to supply voltage to the Microformatter PCBA. The interface signals from the customer's controller are connected to the Microformatter PCBA via edge connectors.

1.4 FUNCTIONAL DESCRIPTION

All logic and functions associated with the reading and writing of 9-channel NRZI or 9-channel PE ANSI and IBM compatible tape are contained in the microformatter.

For NRZI operation, all logic for the generation of the initial gap, inter-record gaps (IRGs), and file mark gaps is provided, in addition to the logic necessary to record data on tape. The logic for complete data recovery (including buffering, error and file mark detection) is also provided.

The NRZI functions of the microformatter include the following:

(1) Compatibility with transports having either single- or dual-stack heads.

(2) Provision for fixed and variable length Erase commands.

(3) Facility for the generation of special commands for editing previously recorded tapes.

(4) Facility for internal or external parity.

For PE operation, all logic for the generation of the preamble, postamble, PE data, and file mark is provided, in addition to the logic necessary to record data on tape. The logic for complete data recovery (including data decoding, buffering, error and file mark detection, and error correction) is also provided.

Table 1-1
PERTEC Formatted Transport Systems

Read Only Model No.	Read-After-Write Model No.	Read/Write Model No.	Data Format Transport PE	Data Format Transport NRZI	Data Format Transport PE/NRZI	Data Format Formatter PE	Data Format Formatter NRZI	Data Format Formatter PE/NRZI	Transport Tape Speeds Available 12.5	18.75	25	37.5	45	75	112.5	125
	FT7840-9F	FT7820-9F		X			X		X	X	X					
	FT7640-9F	FT7620-9F	X			X			X	X	X					
	FT7640-9DF	FT7620-9DF	X					X	X	X	X					
FT8811A-000F	FT8840A-9F	FT8860A-9F		X			X		X	X	X	X	X			
FT8611A-000F	FT8640A-9F	FT8660A-9F	X			X			X	X	X	X	X			
FT8811A-000DF	FT8840A-9DF	FT8860A-9DF		X				X	X	X	X	X	X			
FT8611A-000DF	FT8640A-9DF	FT8660A-9DF	X					X	X	X	X	X	X			
FT8611A-800DF	FT8640A-98DF				X			X	X	X	X	X	X			
FT9811-000F	FT9840-9F	FT9860-9F		X			X					X	X	X		
FT9611-000F	FT9640-9F	FT9660-9F	X			X						X	X	X		
FT9811-000DF	FT9840-9DF	FT9860-9DF		X				X				X	X	X		
FT9611-000DF	FT9640-9DF	FT9660-9DF	X					X				X	X	X		
FT9611-800DF	FT9640-98DF				X			X				X	X	X		
	FT1640-98DF				X			X						X	X	X

The PE functions of the microformatter include the following:

(1) All timing necessary for the generation of IBM compatible inter-block gaps (IBG's) and for correct head positioning between records.

(2) Compatibility with transports having either single- or dual-stack heads.

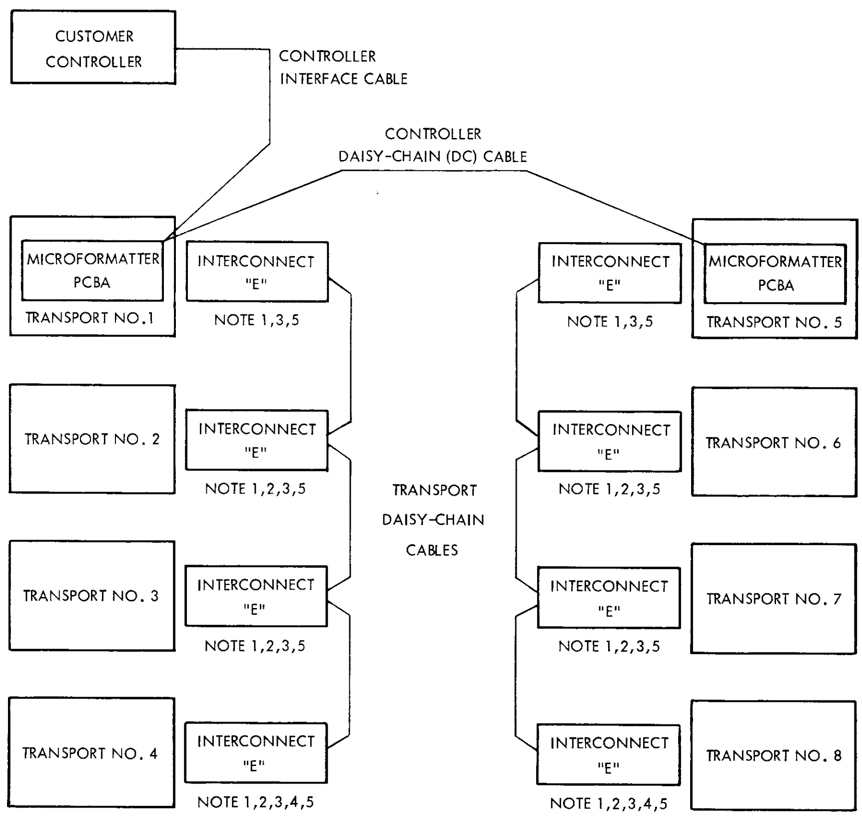
(3) Automatic recording of a PE identification burst prior to recording the first record on a tape.

(4) Automatic testing for the PE identification burst when reading the first record on a tape.

(5) Provision for fixed and variable length Erase commands.

(6) Facility for the generation of special commands for editing previously recorded tapes.

Two microformatters may be daisy-chained to a controller and up to four transports may be daisy-chained to a microformatter. Figure 1-1 illustrates a system configuration of eight transports, two of which are Microformatted Transports.



NOTES:
1. THESE INTERCONNECT "E" PCBA'S ARE DC PCBA'S WHEN USED WITH T7000 TRANSPORTS ONLY.
2. THESE INTERCONNECT "E" PCBA'S ARE MTA II WHEN USED WITH T6000, T8000 AND T9000 TRANSPORTS THAT DO NOT HAVE MICROFORMATTER CAPABILITY.
3. THESE INTERCONNECT "E" PCBA'S ARE NOT REQUIRED WHEN USED WITH T1000 TRANSPORTS.
4. TERMINATORS ARE REQUIRED ON THE LAST DC PCBA ON A DAISY-CHAIN.
5. THE UNIT SELECT SWITCH IS LOCATED ON THE DC #2 PCBA OR THE INTERCONNECT "E" PCBA.

Figure 1-1. Typical System Configuration

SECTION II
INSTALLATION AND INTERFACE CONNECTION

2.1 INTRODUCTION

This section contains a summary of the physical interface connections for the microformatter. Also given are the configuration requirements of master and slave transports when used in a daisy-chain configuration.

2.2 INTERFACE ELECTRICAL SPECIFICATIONS

Levels: True = Low = 0v (approximately)
False = High = +3v

Pulses: Levels as above. Minimum pulsewidth is 1 μsec.

The interface circuits are designed so that an open circuit results in a high signal.

Figure 2-1 shows the configuration of the receivers and transmitters between the controller and microformatter.

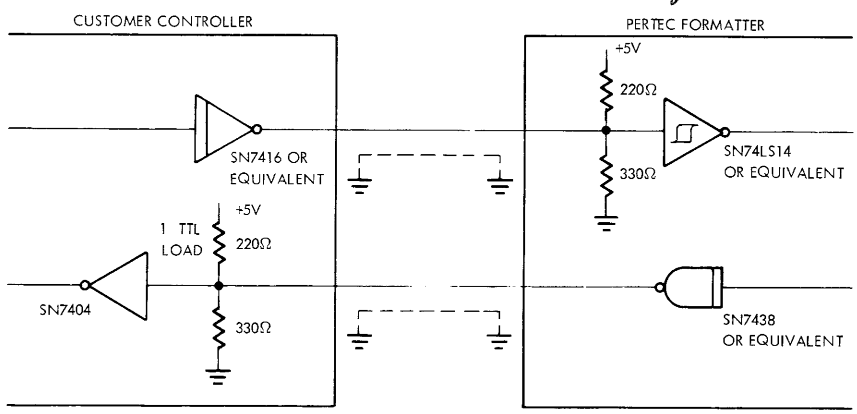
2.3 POWER SPECIFICATIONS

The power consumption of the Microformatter PCBA and the +5 volt regulator is 60 watts (maximum). This consumption is in addition to the transport power requirements listed in Section I of the companion transport manual.

2.4 INTERFACE CONNECTIONS

Two 50-lead flat cables (3M 3365-50 or equivalent) are required for the microformatter to controller interface. This interface is given in Table 2-1. These two cables connect directly to P4 and P5 on the Microformatter PCBA. 2 · 50 lead flat cables are not supplied

P#
P-M. 503-0147
2 connectors



NOTES: 1. NO MORE THAN 1 TTL LOAD SHOULD BE DRIVEN BY INTERFACE SIGNALS TO THE CONTROLLER.

2. IMPROVED NOISE MARGIN WILL BE ACHIEVED IF THE RECEIVER IN THE CUSTOMER CONTROLLER SHOWN ABOVE IS REPLACED WITH AN SN74LS14 WITH SCHMITT TRIGGER INPUT CHARACTERISTICS THIS IMPROVEMENT IN SIGNAL-TO-NOISE RATIO BECOMES MORE SIGNIFICANT AS CABLE LENGTHS INCREASE TO THE MAXIMUM ALLOWABLE SIZE.

Figure 2-1. Interface Configuration

Table 2-1

Controller to Microformatter Interface

Microformatter P4/P5			Microformatter P4/P5		
Live Pin	Return Pin	Signal (Controller to Microformatter)	Live Pin	Return Pin	Signal (Microformatter to Controller)
P5-48	P5-47	FORMATTER ADDRESS (IFAD)	P4-2	P4-1	FORMATTER BUSY (IFBY)
P4-46	P4-45	TRANSPORT ADDRESS (ITAD0)	P5-38	P5-37	DATA BUSY (IDBY)
P5-46	P5-45	TRANSPORT ADDRESS (ITAD1)	P5-16	P5-15	CHECK CHARACTER GATE (ICCG)*
P4-8	P4-7	INITIATE COMMAND (IGO)	P5-16	P5-15	IDENTIFICATION (IDENT)*
P4-18	P4-17	REVERSE/FORWARD (IREV)	P5-12	P5-11	HARD ERROR (IHER)
P4-34	P4-33	WRITE/READ (IWRT)	P5-14	P5-13	FILE MARK (IFMK)
P4-42	P4-41	WRITE FILE MARK (IWFM)	P5-28	P5-27	READY (IRDY)
P4-38	P4-37	EDIT (IEDIT)	P5-44	P5-43	ON-LINE (IONL)
P4-40	P4-39	ERASE (IERASE)	P5-30	P5-29	REWINDING (IRWD)
P4-44	P4-43	READ THRESHOLD 1 (IRTH1)	P5-32	P5-31	FILE PROTECT (IFPT)
P4-36	P4-35	READ THRESHOLD 2 (IRTH2)	P5-4	P5-5	LOAD POINT (ILDP)
P5-50	P5-49	DENSITY SELECT (IDEN)	P5-22	P5-21	END OF TAPE (IEOT)
P4-20	P4-19	REWIND (IREW)	P5-26	P5-25	NRZI (INRZ)
P5-24	P5-23	OFF-LINE (IOFL)	P4-14	P4-13	SINGLE (ISGL)
P4-4	P4-3	LAST WORD (ILWD)	P5-40	P5-39	SPEED (ISPEED)
P5-18	P5-17	FORMATTER ENABLE (IFEN)	P5-36	P5-35	WRITE STROBE (IWSTR)
P4-22	P4-21	WRITE DATA PARITY (IWP)	P5-34	P5-33	READ STROBE (IRSTR)
P4-10	P4-9	WRITE DATA 0 (IW0)	P5-1	P5-5	READ DATA PARITY (IRP)
P4-12	P4-11	WRITE DATA 1 (IW1)	P5-2	P5-5	READ DATA 0 (IR0)
P4-30	P4-21	WRITE DATA 2 (IW2)	P5-3	P5-5	READ DATA 1 (IR1)
P4-26	P4-25	WRITE DATA 3 (IW3)	P4-48	P5-47	READ DATA 2 (IR2)
P4-6	P4-5	WRITE DATA 4 (IW4)	P4-50	P4-49	READ DATA 3 (IR3)
P4-32	P4-31	WRITE DATA 5 (IW5)	P5-6	P5-5	READ DATA 4 (IR4)
P4-28	P4-27	WRITE DATA 6 (IW6)	P5-20	P5-19	READ DATA 5 (IR5)
P4-24	P4-23	WRITE DATA 7 (IW7)	P5-10	P5-9	READ DATA 6 (IR6)
P4-16	P4-15	LOAD ON LINE (ILOL)	P5-8	P5-7	READ DATA 7 (IR7)
			P5-42	P5-41	CORRECTED ERROR (ICER)

*ICCG and IDENT line shared by NRZI and PE

To connect the interface, the following must be considered.

(1) When connecting a controller to a single microformatter, the length of cable should be limited to 12.2 m (40 feet).

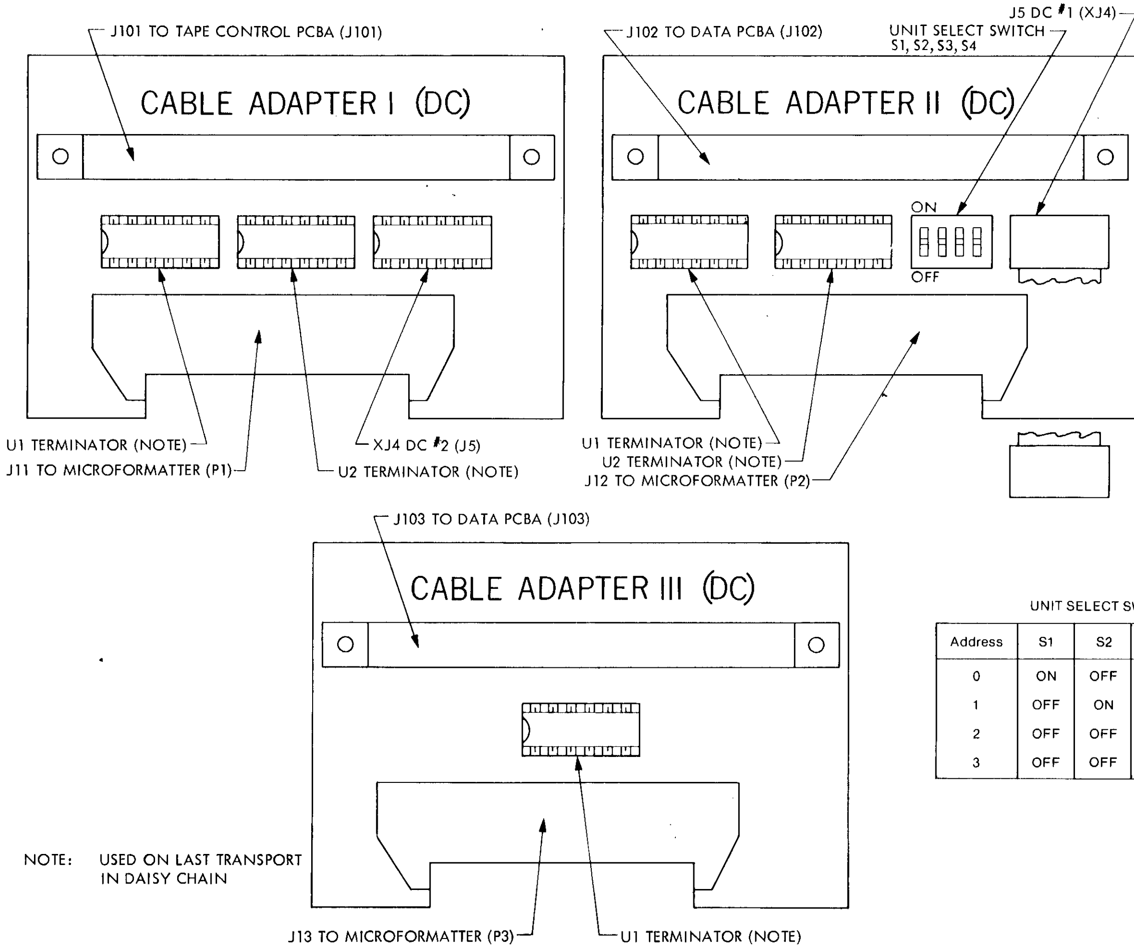
(2) When two microformatters are connected in a daisy-chain configuration to a controller, the *total* cable length should be limited to 12.2 m (40 feet). There should be no more than 1.5 m (5 feet) of cable between the two microformatters, although this distance may be increased to 6.1 m (20 feet) if a 220/330 ohm DIP terminator for each microformatter to controller interface signal is installed within 305 mm (12 inches) of the last microformatter in the daisy-chain.

2.5 DAISY-CHAIN CONNECTIONS

Three 34-lead flat cables (3M 3365-34 or equivalent) are required for the transport daisy-chain interface.

When one, two, or three slave transports are daisy-chained to a master transport, the interconnecting cables may be 12.2 m (40 feet) maximum length. These three cables connect to J11, J12, and J13 of the Cable Adapter (DC) PCBAs when used with the FT7000 series transports. These cables connect to the Interconnect E PCBA when used with FT8000 and FT9000 series transports. When used with the FT1000 model, the cables connect to the Interconnect D PCBA.

The Cable Adapter (DC) PCBAs are shown in Figure 2-2 and the Interconnect E PCBA is shown in Figure 2-3. When using the microformatter with an FT1000 model, refer to the companion Operating and Service Manual for the description of the Interconnect D PCBA. The daisy-chain interface is described in Table 2-2.

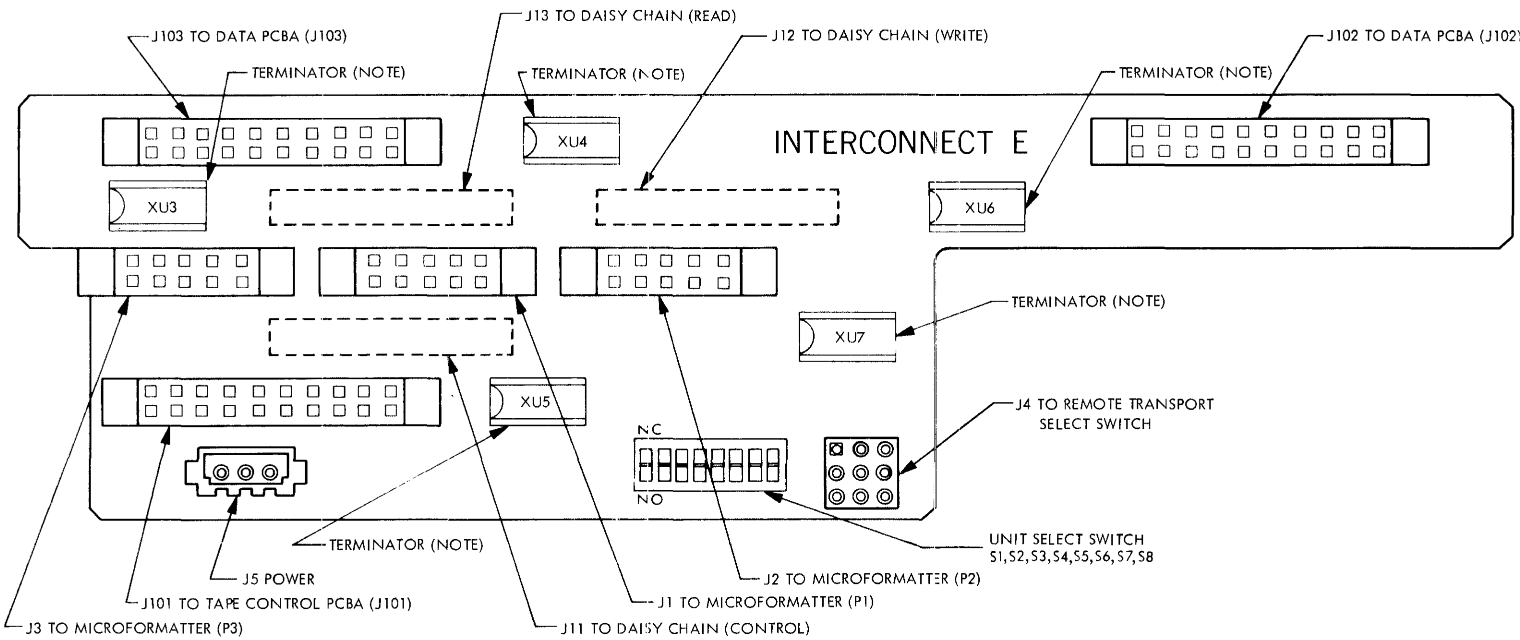


UNIT SELECT SWITCH

Address	S1	S2	S3	S4
0	ON	OFF	OFF	OFF
1	OFF	ON	OFF	OFF
2	OFF	OFF	ON	OFF
3	OFF	OFF	OFF	ON

NOTE: USED ON LAST TRANSPORT IN DAISY CHAIN

Figure 2-2. Cable Adapter (DC) PCBAs



NOTE: USED ON LAST TRANSPORT IN DAISY CHAIN.
PHANTOM LINES INDICATE BOTTOM OF BOARD.

UNIT SELECT SWITCH

COMMAND	S1	S2	S3	S4	S5	S6	S7	S8
TRANSPORT 0	NC	NO	NO	NO	NO			
TRANSPORT 1	NO	NC	NO	NO	NO			
TRANSPORT 2	NO	NO	NC	NO	NO			
TRANSPORT 3	NO	NO	NO	NO	NO			
REMOTE SELECT					NC			
NRZI						NC		
PE						NO		
SGL HEAD							NC	
DUAL HEAD							NO	
LOW SPEED								NC
HIGH SPEED								NO

Figure 2-3. Interconnect E PCBA

Table 2-2 (A)

Control Signals, Transport/Cable Adapter I, Interconnect D, or Interconnect E

Transport J101		Cable Adapter (DCI) J11 or Interconnect E, J11 or T1000, J201		Signal
Live	Return	Live	Return	
1	2	17	—	LOAD ON LINE (ILOL)
A	8	16	—	WRITE AMPLIFIER RESET #2 (IWARS2)
B	2	15	33	OVERWRITE (IOVW)
C	3	14	32	SYNCHRONOUS FORWARD COMMAND (ISFC)
D	4	13	31	DATA DENSITY SELECT (IDDS)
E	5	12	30	SYNCHRONOUS REVERSE COMMAND (ISRC)
F	6	11	29	DATA DENSITY INDICATOR (IDDI)
H	7	10	28	REWIND COMMAND (IRWC)
K	9	8	26	SET WRITE STATUS (ISWS)
L	10	7	25	OFF-LINE COMMAND (IOFC)/REWIND UNLOAD (IRWU)*
M	11	6	24	ON-LINE (IONL)
N	12	5	23	REWIND (IRWD)
P	13	4	22	FILE PROTECT (IFPT)
R	14	3	21	LOAD POINT (ILDP)
T	16	19	20	READY (IRDY)
U	17	2	34	END OF TAPE (IEOT)
J	8	9	27	SELECT 0 (ISLT0)**
—	—	1	—	POWER SUPPLY ENABLE (IPSEN)

*REWIND UNLOAD applies to T9000 and T1000.
**Provided through Select Switch.

Table 2-2 (B)

Write Signals, Transport/Cable Adapter II, Interconnect D, or Interconnect E

Transport J102		Cable Adapter (DCII) J12 or Interconnect E, J12 or T1000, J202		Signal
Live	Return	Live	Return	
A	1	34	2	WRITE DATA STROBE (IWDS)
C	3	32	4	WRITE AMPLIFIER RESET (IWARS)
E	5	30	6	READ THRESHOLD 1 (IRTH1)
F	6	29	7	READ THRESHOLD 2 (IRTH2)*
L	10	25	11	WRITE DATA PARITY (IWDP)
M	11	24	12	WRITE DATA 0 (IWD0)
N	12	23	13	WRITE DATA 1 (IWD1)
P	13	22	14	WRITE DATA 2 (IWD2)
R	14	21	15	WRITE DATA 3 (IWD3)
S	15	20	16	WRITE DATA 4 (IWD4)
T	16	19	17	WRITE DATA 5 (IWD5)
U	17	18	—	WRITE DATA 6 (IWD6)
V	18	1	—	WRITE DATA 7 (IWD7)
—	—	33	2	SELECT 1 (ISLT1)**
—	—	31	5	SELECT 2 (ISLT2)**
—	—	28	8	SELECT 3 (ISLT3)**

*Not applicable to FT7000.
**Provided through Select Switch.

Table 2-2 (C)

Read Signals, Transport/Cable Adapter III, Interconnect D, Interconnect E

Transport J103		Cable Adapter (DCIII) J13 or Interconnect E, J13 or T1000, J203		Signal
Live	Return	Live	Return	
1	A	34	2	READ DATA PARITY (IRDP)
2	B	33	3	READ DATA STROBE (IRDS)*
3	C	32	4	READ DATA 0 (IRD0)
4	D	31	5	READ DATA 1 (IRD1)
8	J	27	7	READ DATA 2 (IRD2)
9	K	26	8	READ DATA 3 (IRD3)
—	—	25	9	NRZI (INRZ)**
—	—	24	10	7-, 9-TRACK (I7TR/I9TR)**
—	—	23	6	SINGLE (ISGL)**
—	—	22	14	SPEED (ISPD)**
14	R	21	15	READ DATA 4 (IRD4)
15	S	20	16	READ DATA 5 (IRD5)
17	U	18	—	READ DATA 6 (IRD6)
18	V	1	—	READ DATA 7 (IRD7)
—	—	19	—	TACHOMETER (ITACH)**

NOTE:
The following pins provide +5v from the microformatter to the dc assemblies.

J11	J13	
18	11	28
	12	29
	13	30

*Relevant to NRZI operation only.

**Not applicable to FT7000.

2.5.1 T7000 DAISY-CHAIN

When connecting the Cable Adapter (DC) PCBAs to a T7000, Cable Adapter I (DC) connects to J101 of the Tape Control PCBA, Cable Adapter II (DC) connects to J102 of the Data PCBA, and Cable Adapter III (DC) connects to J103 of the Data PCBA. Refer to Paragraph 2.5.4 for configurations and to Table 2-3 for details of the PERTEC cable assembly used for these connections.

The three flat cables referred to in Paragraph 2.5 connect to:

(1) P1 of the Microformatter PCBA and J11 of Cable Adapter II (DC) PCBA.

(2) P2 of the Microformatter PCBA and J12 of Cable Adapter II (DC) PCBA.

(3) P3 of the Microformatter PCBA and J13 of Cable Adapter III (DC) PCBA.

2.5.2 T8000 OR T9000 DAISY-CHAIN

When connecting the Interconnect E PCBA to a T8000 or T9000, J101 of the Interconnect E PCBA connects to J101 of the Tape Control PCBA, J102 and J103 of the Interconnect E PCBA connects to J102 and J103 of the Data PCBA, and J1, J2, and J3 of the Interconnect E PCBA connect to P1, P2, and P3 of the Microformatter PCBA. Refer to Paragraph 2.5.4 for configurations.

One end of the three flat cables referred to in Paragraph 2.5 connect to J11, J12, and J13 of the Interconnect E PCBA, the other ends connect to the remaining transports in the daisy-chain. Refer to Table 2-4 for details of the PERTEC cable assembly used for these connections.

Table 2-3

FT7000 Daisy Chain Cable Assemblies

Max. No. of Units	Cable Lengths mm (inches)				Part No.(s) Required
	A*	B**	C**	D**	
1	0.25 (10) 0.43 (17) 0.70 (27.5)				107647-01 107647-02 107647-03
2	0.25 (10) 0.43 (17) 0.70 (27.5)	1.52 (60) 1.52 (60) 1.52 (60)			107647-04***
4	0.25 (10) 0.43 (17) 0.70 (27.5)	1.52 (60) 1.52 (60) 1.52 (60)	3.04 (120) 3.04 (120) 3.04 (120)	1.52 (60) 1.52 (60) 1.52 (60)	107647-05***

*Microformatter to DC PCBAs in first unit.

**DC PCBAs to DC PCBAs.

***Includes the three required cables.

order

Table 2-4

FT8000/FT9000/FT1000 Daisy Chain Cable Assemblies

Max. No. of Units	Cable Lengths m (feet)				Cable Part No.
	A	B	C	D	
2	1.52 (5)				103936-01
2	3.04 (10)				103936-02
4		1.52 (5)	3.04 (10)	1.52 (5)	103936-03
4		3.04 (10)	3.04 (10)	3.04 (10)	103936-04

2.5.3 T1000 DAISY-CHAIN

When daisy chaining T1000 Transports, connectors J201, J202, and J203 of the Interconnect D PCBA are used. Refer to Table 2-4 for details of the PERTEC cable assembly used for these connections.

2.5.4 CONFIGURATIONS

The master/slave transport configurations which may be daisy chained are given in Table 2-5.

Referring to Table 2-5, it should be noted that the format must be NRZI when the higher speed is selected. Also, that PE format may be used on dual speed systems if a dual format microformatter is employed.

In the case when the master transport is not the high speed transport, the customer must so indicate when ordering so that the microformatter will be configured properly.

Table 2-5

Configuration Requirements of Slave Transports Daisy-Chained to Master Transports

Master Transport	Slave Transport	MTA II Required on Slave Transport	DC Adapters Required on Slave Transport	These Slave Characteristics Must be Same as Master: Tape Speed	Head Type	Data Format	Notes
FT7XXX-9F	T7XXX-9		X	X	X	X	
FT7X40-9F	T6XXX-9	X		Note 3		X	
	T8XXXA-9	X		Note 3		X	
FT7X20-9F	T6X20-9	X		Note 3	X	X	
	T8X20A-9	X		Note 3	X	X	
FT7XXX-9DF	T7XXX-9		X	X	X	X	
FT7640-9DF	T6XXX-9	X		Note 3			
	T8XXXA-9	X		Note 3			
FT7620-9DF	T6X60-9	X		Note 3	X		
	T8X60A-9	X		Note 3	X		
FT8840A-9F	T7840-9		X	X	X	X	2
FT8860A-9F	T7820-9		X	X	X	X	1,2
	T7840-9		X	X		X	2
FT8640A-9F	T7640-9		X	X	X	X	
FT8660A-9F	T7620-9		X	X	X	X	1
	T7640-9		X	X		X	
FT8640A-9DF	T7640-9		X	X	X	X	
FT8660A-9DF	T7620-9		X	X	X	X	1
	T7640-9		X	X		X	
FT8840A-9DF	T7640-9		X	X	X		
	T7840-9			X	X	X	2
FT8860A-9DF	T7640-9		X	X			
	T7620-9		X	X	X		1
	T7840-9		X	X		X	
	T7820-9		X	X	X	X	1,2
FT8640A-98DF	T7840-9		X	X	X		
FT8XXXA-9F	T68XX-9	X		Note 3		X	
or	T88XXA-9	X		Note 3		X	
FT9XXX-9F	T98XX-9	X		Note 3		X	
	T8640A-98	X		Note 3		Note 4	
	T9640-98	X		Note 3		Note 4	
	T1640-98			Note 3		Note 4	
FT8XXXA-9DF	T6XXX-9	X		Note 3			
98. or	T8XXXA-9	X		Note 3			
FT9XXX-9,DF	T9XXX-9	X		Note 3			
98. or	T8XXXA-98	X		Note 3			
FT1640-98DF	T9XXX-98	X		Note 3			
	T1640-98	X		Note 3			

NOTES:

1. The Head Type Configuration Switch on the Microformatter PCBA must be set to the down position.
2. The Format Configuration Switch on the Microformatter PCBA must be set to the down position.
3. Tape speed of slave transports must be the same as tape speed of master transports with the following exceptions.

Master Transport: Model	Speed (ips)	Slave Transport: Model	Speed (ips)
FT6, FT7, FT8A	25	T6, T8A	12.5
FT6, FT8A	12.5	T6, T7, T8A	25
FT6, FT8A, FT9	37.5	T6, T8A	18.75
FT6, FT8A	18.75	T6, T8A, T9	37.5
FT6, FT8A, FT9	45	T8611A	22.5
FT8611A	22.5	T6, T8A, T9	45
FT1, FT9	75	T9, T6, T8A	37.5
FT6, FT8A, FT9	37.5	T1, T9	75

4. A TXXXX-98 slave transport may be used only in the format of the master transport.

To daisy-chain a Model FT7000 to T7000 models, both the master and slave transports require the Cable Adapter (DC) PCBA, Figure 2-2. In order to daisy-chain a model FT7000 to T6000 and/or T8000 models, the master transport requires the Cable Adapter (DC) PCBAs and the slave transports require an MTA II. Refer to PERTEC Operating and Service Manual No. 103920 for details of the MTA II.

NOTE

When T7000 transports are daisy-chained, the Cable Adapter [DC] PCBAs must be used.

When daisy-chaining a model FT8000 or FT9000 to either T8000 or T9000 models, the master transport requires an Interconnect E PCBA (see Figure 2-3) and the slave transports require an MTA II.

To daisy chain the model FT1000 to T1000 models, no adapters are required. When daisy chaining a model FT1000 to T8000 or T9000 models, the slave transports require an MTA II.

SECTION III
OPERATION

3.1 INTRODUCTION

This section contains the basic microformatter operation and a detailed definition of the microformatter to controller interface lines.

3.2 BASIC OPERATION

The microformatter is capable of executing the commands necessary to enable the modes of operation described in the following paragraphs. All commands, with the exception of REWIND (IREW), OFF LINE (IOFL) and LOAD ON LINE (ILOL), are executed by sampling the logic states of the REVERSE/FORWARD (IREV), WRITE/READ (IWRT), WRITE FILE MARK (IWFM), EDIT (IEDIT), and ERASE (IERASE) interface lines as given in Table 3-1. REWIND, OFF LINE, and LOAD ON LINE commands are executed directly from the interface without combination.

Refer to Table 3-1 in conjunction with the following command descriptions.

3.2.1 READ FORWARD

The Read Forward command causes tape on the selected transport to be accelerated to the normal transport operating speed. The microformatter reads the first record of data encountered and then decelerates the tape to a stop. The microformatter generates the delays necessary for proper positioning of the transport read head in the inter-record gap (IRG). It is possible to read the next record on tape by supplying a new Read Forward command to the microformatter prior to the completion of the tape deceleration, thereby improving the access time to the next record by as much as one ramp time. This is referred to as *on the fly* operation.

3.2.2 READ REVERSE

The Read Reverse command is similar to a Read Forward command except that tape motion is in the reverse direction. Records may also be read in reverse *on the fly*. During any reverse operation, the microformatter always resets to the quiescent state when the BOT signal is present. A Read Reverse command may be modified to position the head further back in the gap after reading a record. This change in position of the head is to facilitate the editing of a record, and is done by the microformatter in response to an EDIT command. Details of the EDIT command are contained in Paragraph 3.2.4.

3.2.3 WRITE

When executing a Write command, the microformatter accelerates tape and, after the appropriate pre-record delay time, begins to transfer data from the controller to the transport. The process continues until a LAST WORD (ILWD) is received from the controller. If the transport is a single-stack head configuration, the tape will then decelerate to a stop. If the transport is a dual-stack head configuration, the tape will continue to move forward until the record has been read by the read head, then the tape will be decelerated to a stop with the write head properly located in the center of the inter-record gap (IRG).

Consecutive records may be written *on the fly* on both single- and dual-stack head configuration transports.

Table 3-1
Microformatter Commands

Command	IREV	IWRT	IWFM	IEDIT	IERASE
READ FORWARD	H	H	H	H	H
READ REVERSE (Normal)	L	H	H	H	H
READ REVERSE (Edit)	L	H	H	L	H
WRITE	H	L	H	H	H
EDIT	H	L	H	L	H
WRITE FILE MARK	H	L	L	H	H
ERASE (Variable Length)	H	L	H	H	L
ERASE (Fixed Length)	H	L	L	H	L
SPACE FORWARD	H	H	H	H	L
SPACE REVERSE	L	H	H	H	L
FILE MARK SEARCH FORWARD	H	H	L	H	H
FILE MARK SEARCH REVERSE	L	H	L	H	H
FILE MARK SEARCH FORWARD (ignore data)	H	H	L	H	L
FILE MARK SEARCH REVERSE (ignore data)	L	H	L	H	L
L = Low = True H = High = False					

3.2.4 EDIT

Edit operations are similar to Write operations except that the write current is switched off slowly at the end of an edit sequence to minimize the possibility of recording a *glitch* on tape. For proper head positioning, Edit commands should be preceded by a Read Reverse (Edit) command.

3.2.5 WRITE FILE MARK

The Write File Mark command causes a file mark to be written on tape; Paragraphs 3.4.6 and 3.5.5 provide details of the Write File Mark command for PE Format and NRZI Format, respectively.

3.2.6 ERASE (VARIABLE LENGTH)

The Erase (Variable Length) command causes tape to be moved in the forward direction with erase current on. An ILWD signal from the controller terminates the erase operation. It should be noted that in the PE mode, the ID burst will not be erased when an Erase command is given from BOT.

3.2.7 ERASE (FIXED LENGTH)

The Erase (Fixed Length) command causes a 102 mm (4.0 inch) length of tape to be erased. This command is always executed while moving tape in the forward direction.

3.2.8 SPACE FORWARD

The Space Forward command is similar to a Read Forward command except that no READ STROBE (IRSTR) signals are supplied to the controller. Although error checking is not performed, a test is made to determine if the record spaced over was a File Mark.

3.2.9 SPACE REVERSE

The Space Reverse command is similar to a Read Reverse command except that no READ STROBE (IRSTR) signals are supplied to the controller. Although error checking is not performed, a test is made to determine if the record spaced over was a File Mark.

3.2.10 FILE MARK SEARCH FORWARD

A File Mark Search Forward command causes the transport to execute a series of Read Forward commands while in the *on the fly* mode of operation. This series is terminated by the recognition of either a File Mark character or the EOT tab. Tape is stopped following the reading of a File Mark in a manner similar to terminating a normal Read operation. If the EOT tab is encountered during a File Mark Search operation, the operation will terminate and tape will be stopped at the end of the record currently being processed. The File Mark Search Forward command may be combined with a Space Forward command, thereby preventing IRSTR, ICER AND IHER signals from being presented at the Microformatter to Controller Interface.

3.2.11 FILE MARK SEARCH REVERSE

The File Mark Search Reverse command causes the transport to execute a series of Read Reverse commands while in the *on the fly* mode of operation. This series is terminated by the recognition of either a File Mark character or the EOT tab. The tape is stopped after reading a File Mark in a manner similar to terminating a normal Read operation. If the EOT tab is encountered during a File Mark Search operation, the operation is terminated and tape will be stopped at the end of the record currently being processed. The File Mark Search Reverse command may be combined with a Space Reverse command, thereby preventing IRSTR, ICER and IHER signals from being presented at the Microformatter to Controller Interface.

3.2.12 REWIND

The Rewind command causes the transport to rewind to BOT. In systems where more than one transport is daisy-chained, it is possible to rewind several transports while transferring data to or from another transport in the chain.

3.2.13 OFF-LINE

The Off-Line command places the transport under local control. Only the selected transport is placed off-line in daisy-chained systems. In some tape transports (e.g., T9000 series), this command causes the tape transport to perform a Rewind/Unload operation.

3.2.14 LOAD-ON-LINE

The Load-On-Line command enables a remote load sequence.

3.3 GAP GENERATION

3.3.1 INTER-RECORD GAP GENERATION

The microformatter provides timing to generate the necessary 15.2 mm (0.6-inch) gap between records. Longer gaps can be generated by using the Erase command.

3.3.2 INITIAL GAP

When writing in the NRZI format, the first data record is written approximately 89 mm (3.5 inches) down tape from the trailing edge of the BOT tab. In the PE format, the gap follows the ID burst.

3.3.3 FILE MARK GAP

A File Mark will be preceded by a gap of approximately 102 mm (4.0 inches) of tape and followed by a normal IBG.

3.4 PHASE ENCODED FORMAT

The following features apply only to PE and dual format transports. These models write tapes in accordance with ANSI Interchangeability Specification No.X3.39-1973 for 1600 cpi 9-track recording.

3.4.1 DATA

Phase Encoded (PE) data are characterized as follows.

(1) A zero bit corresponds to a transition in the middle of the bit cell away from the erase direction of magnetization. When writing, this corresponds to a high-to-low transition at the microformatter output to the transport.

(2) A one bit corresponds to a transition in the middle of the bit cell toward the erase direction of magnetization. When writing, this corresponds to a low-to-high transition at the microformatter output to the transport.

(3) In the case of successive zero bits or successive one bits, an additional transition is required at the cell boundary. This transition is referred to as the *phase transition* and is in the opposite direction from that of the *data transition*.

3.4.2 PREAMBLE

The preamble is a burst of 40 zero bits and a one bit in all nine tracks at the beginning of each record. When reading, the microformatter tracking circuit uses this burst to synchronize the decoding circuits. The detection of the one bit indicates the beginning of the data field.

3.4.3 DATA FIELD

The data field is written with data and phase transitions as defined in Paragraph 3.4.1. The length of the data field may be a minimum of 18 characters and a maximum of 2,048 characters, in accordance with the ANSI Interchangeability Specification for 1600 cpi 9-track recording. The microformatter is capable of writing and reading records of a minimum of three characters. There is no hardware limitation to the maximum number of data characters that may be included in a single data record.

3.4.4 POSTAMBLE

The postamble is comprised of a single one bit and a burst of 40 zero bits at the end of the record. The postamble provides a means of synchronization when reading tape in the reverse direction. The microformatter interprets a one bit and two consecutive zero bits in all tracks as as being a valid postamble.

3.4.5 PARITY

When writing, the data in the parity data track are generated by the microformatter in such a way as to provide odd parity for all characters in the data field. An external parity generator may also be used.

3.4.6 FILE MARK

When a Write File Mark command is executed, the microformatter generates the file mark gap and then generates a File Mark consisting of 256 flux reversals at 3200 frpi in Channels P, 0, 2, 5, 6, and 7. Channels 1, 3, and 4, are dc erased.

When reading, the microformatter will recognize a File Mark if there are at least 64 flux reversals in Channels 2, 6, and 7 with Channels 1, 3, and 4 dc erased. Channels P, 0, and 5 are ignored for this test.

3.4.7 IDENTIFICATION BURST

When performing a Write command from BOT, the microformatter writes an ANSI and IBM compatible identification (ID) burst consisting of a sequence of 1600 frpi flux reversals in Channel P, with all other tracks dc erased. To write this ID burst properly, a Write command from BOT should not be preceded by any Reverse command except Rewind.

In the Read mode, the microformatter samples the output of Channel P as the BOT tab traverses the read head. If an ID burst is detected, the IDENT interface line is pulsed.

3.4.8 DROPOUT AND ERROR CORRECTION

A dropout is detected by the microformatter for a particular track if no data are present on that track for more than one and one-fourth bit cell times. This test is made after approximately 20 zero bits of the preamble have been read in each track. If only one of the nine tracks has a dropout detected in the microformatter, the microformatter will correct this track by using the odd parity nature of the data in conjunction with the single track dropout indication.

If a dropout of more than one track is indicated by the microformatter, data are invalid and the command is immediately terminated. Tape motion is not stopped until the end of the record is found.

3.4.9 DESKEW OF READ DATA

As data are read from tape, the data transitions corresponding to bits of a specific character may arrive at the microformatter at different times, due to the skewed relationship of the nine data tracks. Data may be skewed as much as 2.9 characters and still be deskewed properly to be presented at the controller interface.

3.4.10 ERROR DETECTION

If the data read back from the tape shows even parity for a particular data character with no track dropout indication, an error indication is provided during the transfer of that specific character to the controller. The command is not aborted. The microformatter continues execution of the current command, provided that none of the following errors occur. If one of these errors is detected, the command is aborted and the microformatter will search for the IBG.

(1) A one bit is detected in either the preamble or postamble.

(2) An overflow condition is detected in the deskew buffer, indicating excessive tape skew, i.e., greater than 2.9 characters.

(3) One or more channels fails to detect the one bit at the end of the preamble.

(4) A false postamble is detected in the middle of the record.

(5) A dropout indication is generated for two or more channels.

3.4.11 TRACKING OSCILLATOR

When reading PE data, a tracking oscillator is used to decode data. This oscillator follows the long-term and short-term speed variation of the data being read. The characteristics of the oscillator are such that any PE tape that complies with the ANSI Interchangeability Specification may be read by any PERTEC Microformatter/Transport PE tape system.

3.4.12 RECORD RECOGNITION

When a Read command is given to the microformatter, tape is ramped up to nominal speed and the microformatter searches for the preamble of a data record. Channels 2, 0, 4, and 5 inclusive are monitored. A valid preamble is declared if data are present on Channels 2, 0, 4, or 5 inclusive continuously for 10 character times.

If data are present on Channels 2, 0, 4, or 5 continuously for a time period less than 10 character times, the microformatter will assume that the few data pulses received were due to erroneous flux transitions occurring prior to the actual data record, and the microformatter will continue to search for the data record.

Once a valid record has been recognized at 10 character times into the preamble, any loss of data (as determined from Channels 2, 0, 4, and 5) results in the microformatter stopping tape motion. This is due to either the loss of data in these four channels or the valid end of the data record. The data loss must be continuous for greater than 22 character times for tape motion to stop.

3.5 NRZI FORMAT

The following NRZI format description applies to all NRZI and dual format models. The data format described is consistent with ANSI Interchangeability Specification X3.22-1973 for 9-track, 800 cpi NRZI recording.

3.5.1 DATA

NRZI data are characterized as follows.

(1) A one bit corresponds to a flux transition in the center of the bit cell on tape. This corresponds to a logic true (one) on the WRITE DATA interface line to the transport during a Write operation.

(2) A zero bit corresponds to a lack of any flux transition on tape or a logic false (zero) on the WRITE DATA interface line to the transport during a Write operation.

3.5.2 DATA RECORD

A record of NRZI data may contain between 18 and 2048 ASCII characters. This is in accordance with the ANSI Interchangeabilty Specification for 800 cpi 9-track recording. The microformatter is capable of writing and reading records of a minimum of three characters. There is no hardware limitation to the maximum number of data characters that may be included in a record. Channel P on tape is written to provide odd parity for all data characters. Nominal spacing between characters is 3175 μm (1250 μinches).

3.5.3 CYCLIC REDUNDANCY CHECK CHARACTER

The Cyclic Redundancy Check Character (CRCC) is written on tape after a four character delay from the last data character. The CRCC is generated in accordance with the ANSI Interchangeability Specification for 800 cpi NRZI magnetic tape recording.

3.5.4 LONGITUDINAL REDUNDANCY CHECK CHARACTER

The Longitudinal Redundancy Check Character (LRCC) is written on tape after a four character delay from the CRC character. The data in this character is such that the total number of one bits in a track (including the CRCC and LRCC) is even. The LRCC will never be an all-zeros character. The LRCC is generated by the reset of the write register in the tape transport. The LRCC also serves to set the tape magnetization in the proper direction for IRG.

3.5.5 FILE MARK

When executing a Write File Mark command, the microformatter generates a one-character record. This single data character consists of a one bit in Channels 3, 6, and 7 and a zero bit in all other channels. The CRCC contains all zeros. The LRCC is equivalent to the single data character.

The microformatter tests for the presence of the file mark pattern during every Read operation. When this is detected, the IFMK interface line to the controller is pulsed and the file mark characters are transmitted to the controller.

3.5.6 ERROR DETECTION

In the NRZI format, all deskewing functions during a Read operation are performed in the tape transport. The microformatter receives a nine-bit word from the transport and relays this word to the customer's controller. A HARD ERROR (IHER) is generated by the microformatter if any of the following read errors occur.

(1) A data character is read from tape containing even parity.

(2) A CRCC is read from tape containing even parity and the record contains an even number of data characters.

(3) A CRCC is read from tape containing odd parity and the record contains an odd number of data characters.

(4) Longitudinal parity on any track is odd.

(5) A track dropout occurs in such a way as to cause more than two check characters, i.e., CRCC and LRCC, to be detected when the microformatter interprets the dropout as an end-of-record condition.

It should be noted that all of the foregoing errors except (5) are checked during both Read Forward and Read Reverse operations. The error described in (5) is checked only during Read Forward operations.

3.6 CONTROLLER-TO-MICROFORMATTER INTERFACE

3.6.1 FORMATTER ADDRESS (IFAD)

This is a level which selects one of the two possible microformatters attached to the controller to microformatter interface.

High = Address 0

Low = Address 1

The microformatter's address is predetermined by a switch on the Microformatter PCBA.

When selected, a microformatter is connected to the controller and all controller to microformatter interface lines are activated.

Unless otherwise noted, the description of all other controller to microformatter lines will assume that the microformatter is selected.

3.6.2 TRANSPORT ADDRESS (ITAD0, ITAD1)

The levels on these two lines select one of the four transports which may be daisy-chained to the microformatter. These lines are decoded by the microformatter and transmitted to the microformatter to transport interface as follows.

ITAD0	ITAD1	Address
High	High	ISLT0
High	Low	ISLT1
Low	High	ISLT2
Low	Low	ISLT3

3.6.3 INITIATE COMMAND (IGO)

This pulse initiates the commands given in Table 3-1. On the trailing edge of IGO, the command lines described in Paragraphs 3.6.4 through 3.6.8 are copied into the microformatter and the FORMATTER BUSY signal (IFBY) is set low. IFBY is described in Paragraph 3.7.1.

3.6.4 REVERSE/FORWARD (IREV)

This signal specifies forward or reverse tape motion.

Low = Reverse

High = Forward

3.6.5 WRITE/READ (IWRT)

This signal specifies the operation mode of the system.

Low = Write

High = Read

3.6.6 WRITE FILE MARK (IWFM)

This pulse causes a Write File Mark to be written on the tape, if IWRT is also low during this time.

3.6.7 EDIT (IEDIT)

The EDIT signal is employed in two ways:

(1) Read reverse. Modifies the read reverse stop delay to optimize head positioning when editing tapes.

(2) Write. The transport write current is turned off gradually at the end of the record, thus preventing an adjacent data record from being erased.

3.6.8 ERASE (IERASE)

When the IERASE and IWRT signals are low, the microformatter is conditioned to perform a dummy Write command. The microformatter goes through all the functions of a normal Write operation except that no data are recorded. A length of tape is erased equivalent to the length of the dummy record as defined by LAST WORD (ILWD) Paragraph 3.6.14.

Alternatively, if the IERASE, IWRT, and IWFM signals are low, the microformatter is conditioned to perform a dummy Write File Mark operation. A fixed length of tape of approximately 102 mm (4.0 inches) is erased.

The IERASE signal is also used to inhibit READ STROBE (IRST) during a space operation (Space Forward or Space Reverse) (NSPC) or File Mark Search operation.

3.6.9 READ THRESHOLD LEVEL 1 (ITHR1)

This signal is used only on transports having a single-stack head, and specifies the operating read circuit threshold level. ITHR1 is normally made low only when it is required to perform a read-after-write data check.

Low = High Threshold

High = Normal Threshold

3.6.10 READ THRESHOLD LEVEL 2 (ITHR2)

This signal is used on transports having a low read threshold capability and is normally made low only when it is required to recover low amplitude data.

Low = Extra Low Threshold

High = Normal Threshold

3.6.11 DENSITY SELECT (IDEN)

The IDEN signal is used only when dual format microformatters are used in conjunction with transports equipped with PE or NRZI format selection capability. The state of this line is loaded into the microformatter with each INITIATE COMMAND (IGO).

Low = 800 cpi (NRZI)

High = 1600 cpi (PE)

3.6.12 REWIND (IREW)

IREW is a pulse which causes the selected transport to rewind to Load Point, providing the transport is Ready and On-Line. The pulse is routed directly to the transport and does not cause the microformatter to become busy.

3.6.13 OFF-LINE (IOFL)

This pulse causes the selected transport to be placed in the Off-Line mode of operation. IOFL is routed directly to the transport and does not cause the microformatter to become busy.

3.6.14 LAST WORD (ILWD)

During the execution of a Write command or an Erase (Variable Length) command, this pulse is used to indicate that the next character to be strobed into the microformatter is the last character of the record. The line will be set low by the controller at the time the last data character is set on the interface lines.

3.6.15 FORMATTER ENABLE (IFEN)

This is a level which, when high, causes the microformatter to reset to the quiescent state. The signal is not gated by IFAD, hence, if two microformatters are connected to the interface, both will be simultaneously reset.

This line may be used to disable the microformatter if the controller power is lost, or, to clear the microformatter logic.

3.6.16 WRITE DATA LINES (IW0—7)

These eight lines transmit write data from the controller to the microformatter. The eight data bits appearing on WRITE DATA LINES (IW0—7) are written onto the corresponding channels on tape. IW7 corresponds to the least significant bit of the character.

The first character of the data record should be available on these lines within one character period after IDBY goes true and should remain true until the trailing edge of the first IWSTR pulse issued by the microformatter. The next character of information must then be set up in less than half a character period. Subsequent characters will be processed in this way until ILWD is set low, indicating that the last character is being transferred. Table 3-2 identifies these lines with regard to interface identification, ANSI Track Number and binary weight.

3.6.17 WRITE DATA PARITY (IWP)

This line is used only when the external parity generation option is used. This option requires the customer to generate odd parity on the eight data lines (IW0—7) and apply this parity bit to IWP. Setup timing requirements for this line are consistent with requirements for IW0—7. This line is ANSI track number 4.

3.6.18 LOAD-ON-LINE COMMAND (ILOL) (Optional)

The ILOL pulse, when low (1.0 second minimum width), can be given at any time after ac power is applied to the transport. Tape is tensioned after the first ILOL pulse. When a second ILOL pulse (1.0 μsec minimum duration) is given, the transport goes into an On-Line mode. The two pulses must be separated by at least 1.0 μsec.

Table 3-2
Write Data Line Identification

Interface Line	Track Number	ANSI Track Number	Binary Weight
W0	0	7	2^7
W1	1	6	2^6
W2	2	5	2^5
W3	3	3	2^4
W4	4	9	2^3
W5	5	1	2^2
W6	6	8	2^1
W7	7	2	2^0

3.7 MICROFORMATTER-TO-CONTROLLER INTERFACE

3.7.1 FORMATTER BUSY (IFBY)

When a command is issued to the microformatter, FORMATTER BUSY (IFBY) goes low at the trailing edge of IGO and remains low until tape motion ceases after execution of the command. This signal may be used by the controller to inhibit further commands.

3.7.2 DATA BUSY (IDBY)

The IDBY signal goes low when the transport has reached operating speed, traversed the IRG, and the microformatter is about to write data on the tape or read data from the tape. IDBY remains low until the data transfer is finished and the appropriate post-record delay completed. IDBY goes high at the same time that the capstan starts to decelerate the tape. A new command may be given when IDBY goes high for an *on the fly* operation. *On the fly* commands must be of the same Read/Write mode and the same tape direction.

3.7.3 CHECK CHARACTER GATE (ICCG) - IDENTIFICATION (IDENT)

This interface line is shared by NRZI and PE formats. In the NRZI format, the signal is ICCG and is set low by the microformatter when the read information currently being transmitted to the controller is either a CRCC or an LRCC. The signal is high when data characters are being transmitted. Data and check information can be distinguished by gating READ STROBE (IRSTR) with ICCG or its inverse.

In the PE format, the signal on this line is IDENT. The line is pulsed when an ID burst is read from the tape.

3.7.4 HARD ERROR (IHER)

The IHER signal is set low if a read error is detected by the microformatter. Read errors are defined in Paragraphs 3.4.10 and 3.5.6 for PE Format and NRZI Format respectively.

All error information is reported to the controller before DATA BUSY (IDBY) goes high.

3.7.5 CORRECTED ERROR (ICER)

The CORRECTED ERROR signal (ICER) is used only in the PE mode. It is set low by a single track dropout during a Read or Read-After-Write operation. ICER in a Read-After-Write operation indicates that the record should be rewritten.

3.7.6 FILE MARK (IFMK)

This is a pulse which indicates that the microformatter read logic has detected a File Mark. This may be during execution of any Read Forward or Read Reverse operation, or during a Write File Mark operation for a read-after-write transport.

3.7.7 TRANSPORT STATUS AND CONFIGURATION LINES

Status: IRDY, IONL, IRWD, IFPT, ILDP, IEOT
Configuration: INRZ, ISGL, ISPEED

These lines are used to indicate the status and configuration of the selected transport and are defined exactly the same as in the transport-to-microformatter interface description, except that they have also been gated with the FORMATTER ADDRESS LINE (IFAD). Refer to companion Operating and Service Manual (Section III) for these definitions.

3.7.8 WRITE STROBE (IWSTR)

The IWSTR line is pulsed for each data character to be written on tape. The pulsewidth of IWSTR is approximately 25 percent of a character time. IWSTR samples the WRITE DATA lines (IWP, IW0—7) from the controller and copies this information, character by character, into the microformatter write logic.

The first character must be available before the first IWSTR is issued, and succeeding characters must be set up within half a character period after the trailing edge of each IWSTR pulse.

This line is also active during Erase (Variable Length) commands; however, the data being copied into the microformatter will not be written on tape.

For a Write File Mark or Erase (Fixed Length) command, the required pattern is generated internally by the microformatter and IWSTR is not used.

3.7.9 READ STROBE (IRSTR)

The READ STROBE line (IRSTR) is pulsed for each character of read information (data, CRCC, and LRCC) to be transmitted to the controller. IRSTR is used to sample the READ DATA lines (IRP, IR0—7).

The transmission of check characters (CRCC and LRCC) is flagged by the CHECK CHARACTER GATE line (ICCG) as described in Paragraph 3.7.3 and in the event of an all zeros character, an IRSTR pulse is provided.

Note that although the average time between adjacent IRSTR pulses is $1/BV$

where B = packing density

V = tape velocity

this time may vary considerably due to the combined effects of bit crowding and skew. The minimum time between adjacent pulses is one-half character period.

3.7.10 READ DATA LINES (IRP, IR0—7)

These nine lines transmit read data from the microformatter to the controller. Each character read from the tape is available by sampling IRP, IR0—7 in parallel by IRSTR.

Data remains set on IRP, IR0—7 for a full character period. The corresponding IRSTR pulse is placed centrally during the time that data are available.

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section provides a block diagram description and the theory of operation of the microformatter. The microformatter consists of the Microformatter PCBA and the Power Supply II PCBA. Also presented are methods of fault isolation and maintenance procedures.

Figure 4-1* is a block diagram of a dual microformatter and should be referred to in conjunction with the following paragraphs. It is important to note that the functional discussion of the block diagram is addressed to dual operation of the microformatter and individual NRZI and PE operations are discussed as subsets of the dual operation.

4.2 BASIC CONFIGURATION AND OPERATION

The microformatter may be configured as NRZI only, PE only, or Dual (both NRZI and PE).

Referring to Figure 4-1, it can be seen that the NRZI section contains the Clock Generator, Interface Logic, Master Control, NRZI Read Control, NRZI Read Logic, Error Gating, Read Strobe Gating, Input Read Logic, Output Read Logic and Write Data Generator.

Similarly, it can be seen that the PE section contains the Clock Generator, Interface Logic, Master Control, PE Read Control, Tracking Oscillator, PE Read Logic, Error Gating, Read Strobe Gating, Input Read Logic, Output Read Logic and Write Data Generator.

The microformatter must be selected to operate. Selection is according to the FORMATTER ADDRESS line (IFAD) and the settings of U112-S3 and S4 (refer to Table 4-1).

The microformatter logic must be conditioned according to the type of transport, i.e., PE, NRZI, or Dual. The transport must be selected by the switch settings on the Cable Adapter PCBA (DC) (FT7000 series), Interconnect E PCBA (FT8000 and FT9000 series), or the Select Switch on the FT1000 series.

Additionally, if the transports are daisy-chained, U112-S5 and S6 must be set. Table 4-2 describes the method of format selection.

The transport status lines are received by the Interface Logic and coupled to the Master Control. The Interface Logic transmits these signals to the controller.

The SPEED signal is coupled through the Interface Logic and into the Clock Generator.

The Clock Generator controls all the timing within the microformatter for both NRZI and PE operation. The clock frequency is dependent on the speed of the transport and is programmed by the setting of U187 (Frequency Select). When SPEED is high, the output of the Clock Generator (WCLK and NWCLK) is divided by two. These clocks are applied to the Master Control, the Write Data Generator, and the NRZI Read Control.

The Master Control receives signals from the Interface Logic via status and command lines and conditions the microprogram on Read Only Memory (ROM) chips. The Master Control provides the required control for both NRZI and PE Write and Read logic. The Write signal (WRT) input to the Control Logic determines whether the microprogram selects a Write operation or a Read operation.

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*Foldout drawing, see end of this section.

Table 4-1

Formatter Address (U112)

Formatter Address	S3	S4
Zero	Down	Up
One	Up	Down

Table 4-2

Format Select (U112)

Switch	Format	Model FT7000	Models FT8000, FT9000, FT1000
Format S5	PE	Up	Up
	NRZI	Down	Up
	Dual	Up	Up
Head S6	Single	Down	Up
	Dual	Up	Up

When the Master Control receives a GO1 signal from the Interface Logic, the status and command lines set the Master Control. Formatter Busy (FBY) is set at this time. Data Busy (DBY) is set when the microformatter is processing data (write or read).

When WRT is high, the Master Control microprogram selects a Write operation. The coding of the Write Commands (WCN0, WCN1, WCN2) determines the type of data to be written. Also, Load Write Data (LDWRTDATA), Load Cyclic Redundancy Character (LDCRC) are provided to the Write Data Generator. Write Strobe (WSTR) is provided to the Interface Logic.

When WRT is low, the Master Control microprogram selects a Read operation. The state of the REVERSE command (IREV) determines if the Read operation is to be executed in a forward or reverse direction.

When in the PE mode, the LAST WORD (ILWD) sets a jump condition and a postamble is written.

4.3 WRITE OPERATION

The Write Data Generator receives and buffers Write signals (IWP, IW0-IW7) from the controller and transmits them to the transport (IWDP, IWD0-IWD7). The WRITE PARITY signal (IWP) may be selected either internally or externally by setting U112-S1 and S2 (refer to Table 4-3).

4.3.1 NRZI WRITE OPERATION

Figure 4-2 is a timing diagram for a NRZI Write operation and should be referred to in conjunction with Figure 4-1. The Write Data Generator is enabled when DBY is high. The Write Data Generator transfers data when LDWRTDATA is high. WCN0, WCN1, WCN2 determine the type of data to be written.

After one character time, the first byte of data is coupled to the transport data lines. At the end of the character period, the WRITE DATA STROBE (IWDS) line is pulsed which transfers the byte of data to the selected tape transport. The transport encodes the data into NRZI form and writes it on the tape.

The data are also transferred into a CRC register and the register generates the CRC character, which is written on the tape after the end of the record.

At the end of the character period, a WRITE STROBE (IWSTR) pulse informs the controller that processing of this character is complete and that a new byte is required. The controller must set the new byte on IWP, IW0-7 within one-half character period after the trailing edge of IWSTR.

Subsequent characters are processed in this manner until the controller sets LAST WORD (ILWD) low, indicating that the last bit is being transmitted. Following the IWSTR pulse, the Write Data Generator starts a termination sequence and causes the CRC and/or LRC characters to be written on the tape.

The contents of the CRC register are coupled to the transport during the fourth character period after the last data bit is written. An additional IWDS pulse causes the information to be written on the tape. Four character periods later, the WRITE AMPLIFIER RESET (IWARS) line is pulsed, which resets the transport write register and causes the LRC character to be written on the tape.

After the LRC character is written, a post-record delay is entered. For transports having a single-stack head, the post-record delay is initiated immediately after the LRC character. For transports having a dual-stack head, the post-record delay is initiated when the microformatter Read logic completes a read-after-write check on the data. An internal signal, End NRZI (RENDNZ), indicates the end of the Read-After-Write operation.

Table 4-3

Parity Select (U112)

PARITY	S1	S2
Internal	Up	Down
External	Down	Up

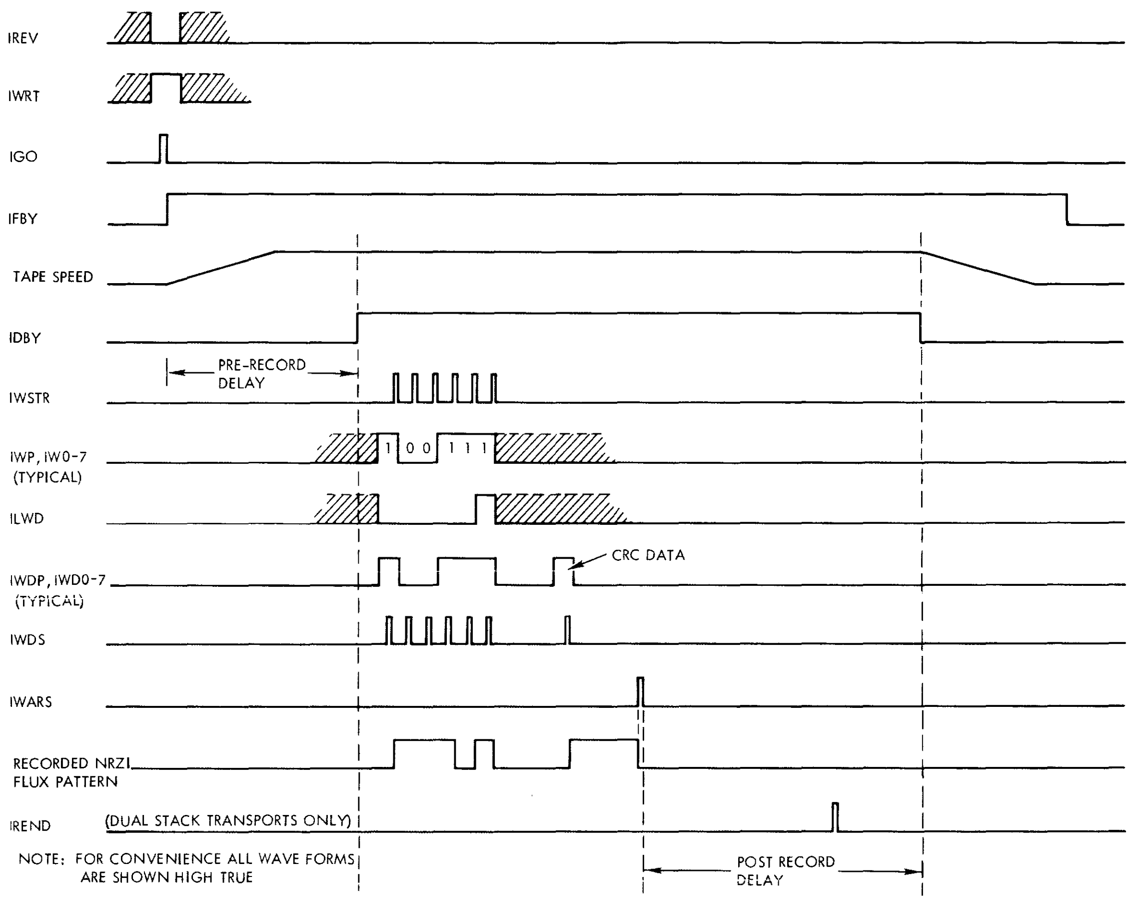

Figure 4-2. 9-Channel NRZI Write Operation

The Erase (Variable Length) command is a dummy Write File Mark (WFM) command. A fixed length of tape is erased (approximately 102 mm [4.0 inches]).

The NRZI format requires that the first record appearing on tape be placed approximately 127 mm (5 inches) past the BOT marker. To accomplish this, the microformatter generates an extra long pre-record delay when a Write command is issued at BOT.

A File Mark consists of a single character record having one bits in channels 3, 6, and 7 for both the data character and the LRCC. The CRCC contains all *zeros*. This record is separated from the previous record by approximately 102 mm (4.0 inches) and by a normal IBG of 15.2 mm (0.6 inch) from the following record.

4.3.2 PE WRITE OPERATION

Figure 4-3 is a timing diagram of a PE Write operation. The Write Data Generator is enabled when DBY is high, and transfers data when LDWRTDATA is high. WCN0, WCN1, WCN2 determine the type of data to be written.

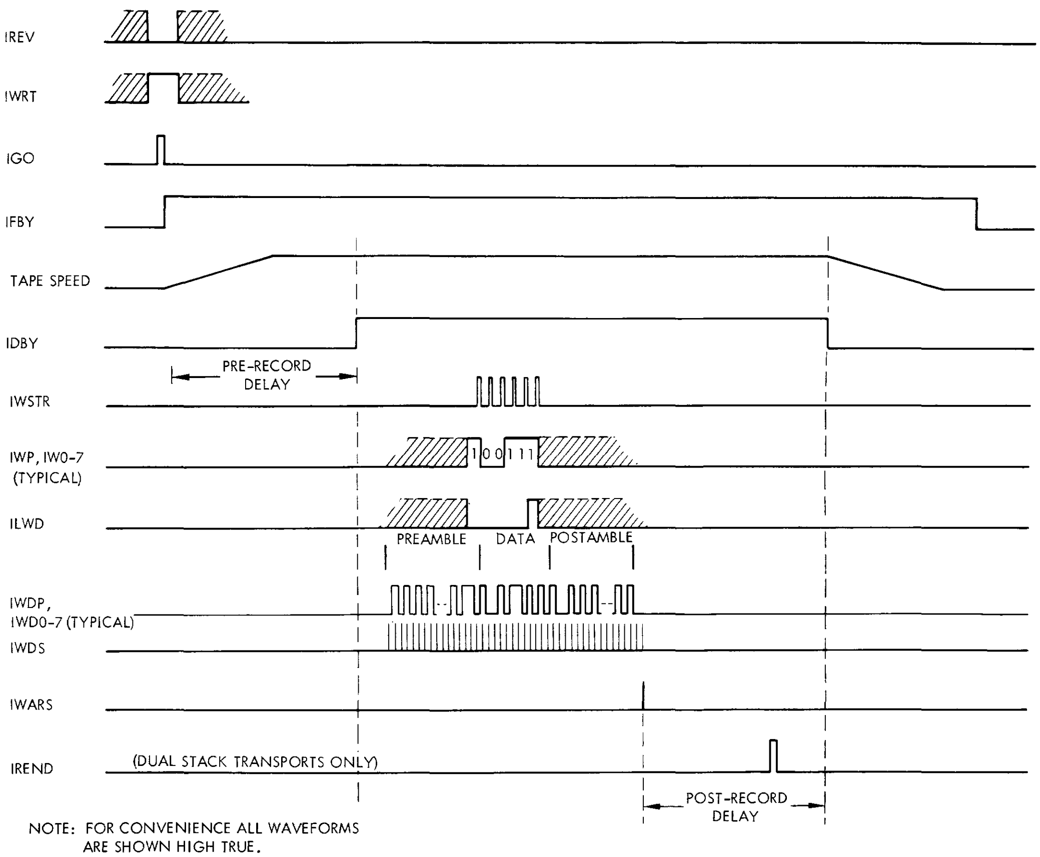

Figure 4-3. 9-Channel PE Write Operation

When DBY goes high, the microformatter generates a preamble data pattern consisting of 40 zero bits followed by a one bit. This pattern is phased encoded and written on the nine data channels on the tape.

During the time period in which the last preamble one bit is being recorded, an IWSTR pulse is sent to the controller. On the trailing edge of IWSTR, the data appearing on IWP, IW0-7 is transferred to the microformatter, encoded, and then written on the tape immediately following the preamble one bit.

The controller uses the trailing edge of the IWSTR pulse to set the next byte of data on IWP, IW0-IW7. The microformatter requires the first bit be set on the data lines before the first IWSTR is sent and the subsequent bits are set within one-half of a character period after the trailing edge of IWSTR.

The controller sets ILWD low when the last data byte is set on IWP, IW0-7. When the following IWSTR pulse occurs, the microformatter samples ILWD and then enters a postamble sequence immediately following the writing of the last data byte.

The postamble pattern is a mirror image of the preamble and consists of a one bit followed by 40 zero bits. The postamble is phase encoded and written simultaneously on the nine tape tracks.

Shortly after the last postamble bit is recorded, a WRITE AMPLIFIER RESET (IWARS) pulse is issued by the microformatter. In some tape transport models, the IWARS pulse is used to control write current turn-off at the end of an Edit operation.

When operating a transport using a single-stack head, the post-record delay is initiated immediately after the last postamble bit.

When operating a dual-stack transport, the write sequence is terminated in a different manner. The post-record delay is initiated after the transport read electronics have completed a read-after-write check on the data just recorded. An internal signal, RENDPE, is used to indicate the end of the Read-After-Write operation.

The 1600 cpi PE format requires tapes which are recorded in the PE mode be identified by a burst of alternate ones and zeros at the BOT marker. It also requires the first record be written approximately 127 mm (5 inches) after the marker.

When writing from BOT, the microformatter generates an extra long pre-record delay. In a suitable time interval during the delay, the PE identification burst, consisting of a pattern of alternate ones and zeros (1 0 1 0 1 0 1 0), is written in the Parity Channel. All other channels are erased.

After completion of the pre-record delay, the tape is positioned approximately 127 mm (5 inches) past the BOT marker and the first record is written.

A File Mark record consists of 256 flux reversals at 3200 frpi in Channels P, 0, 2, 5, 6, and 7. Channels 1, 3, and 4 are dc erased. The File Mark is separated from the preceding record by approximately 102 mm (4.0 inches) and from the following record by a nominal IBG of 15.2 mm (0.6 inch).

The microformatter generates a long pre-record delay equivalent to a 95 mm (3.75-inch) IBG. The Write logic then generates and encodes 128 preamble zero bits and records this on Channels P, 0, 2, 5, 6, and 7. This pattern is equivalent to 256 flux reversals at 3200 frpi.

At the completion of the Write File Mark operation, the command is terminated the same as other Write operations.

The Erase (Variable Length) is a dummy Write command used to erase any length of tape. This operation is useful in applications which require the ability to erase inidividual records on a previously recorded tape.

When executing the Erase (Variable Length) command, the microformatter performs all operations of a normal Write command except that the dummy data being transmitted from the controller to the microformatter is not recorded. Therefore, a length of tape equivalent to the dummy record is erased. The ILWD signal determines the record length, in the manner previously described.

The Erase (Fixed Length) command is a dummy Write File Mark command. When enabled, a fixed length of tape (approximately 102 mm [4.0 inches]) is erased.

4.4 READ OPERATION

Referring to Figure 4-1, it can be seen that there are two Read Logic sections of the microformatter, NRZI Read Logic and PE Read Logic. The NRZI section consists of the NRZI Read Control and the NRZI Read Logic. The PE section consists of the Tracking Oscillator, PE Read Control, and the PE Read Logic.

The Input Read Logic, Output Read Logic, Error Gating and Read Strobe Gating are common to both NRZI and PE Read operations. A Read operation is enabled by GO1.

Incoming Read data are routed through the Input Read Logic, buffered and supplied to either the NRZI Read Logic or the PE Read Logic.

Outgoing Read data are routed through the Output Read Logic from either the NRZI Read Logic or the PE Read Logic. The data are buffered and transmitted to the controller.

The Error Gating Logic and the Read Strobe Gating Logic are discussed within the NRZI and PE Read operations (Paragraphs 4.4.1 and 4.4.2).

4.4.1 NRZI READ OPERATION

The NRZI Read operation is enabled when the NRZ signal is high and WRT signal is low to the Master Control from the Interface Logic. The microprogram in the Master Control sets the NRZI Read Gate signal (RGATENZ1 and RGATENZ2) high. Refer to Figure 4-4.

The microformatter reads data either in the forward or reverse direction, depending on the state of REV1.

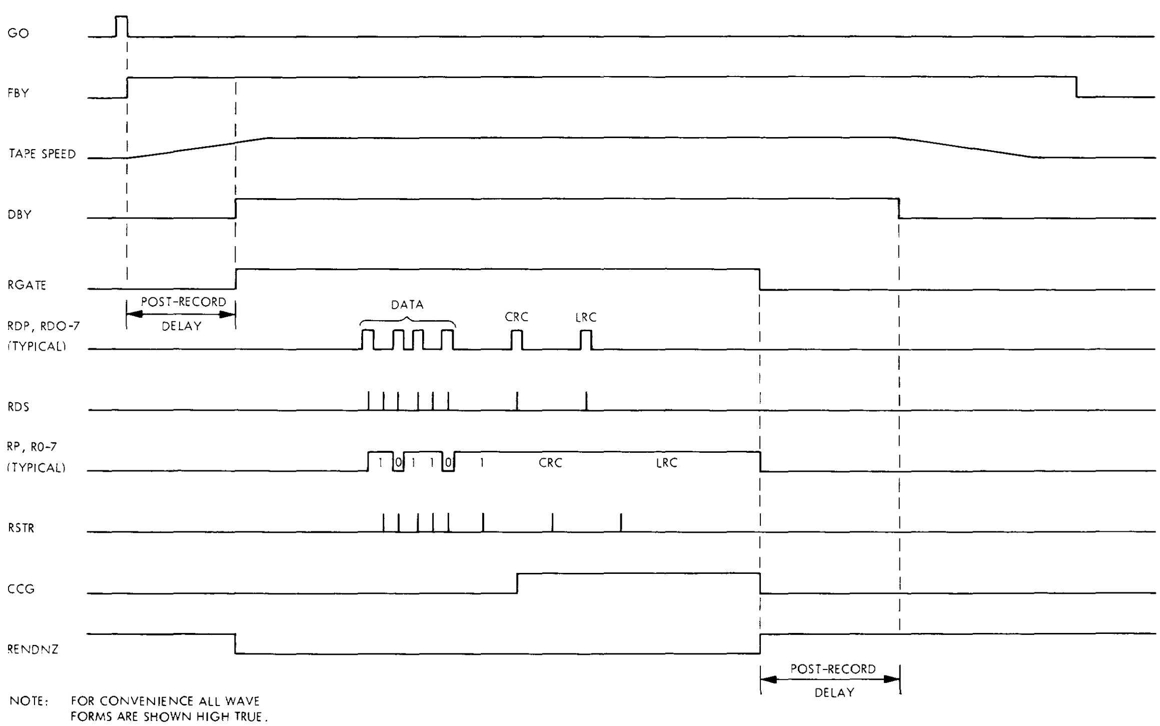

Figure 4-4. NRZI Read Operation

The Read data are received and buffered by the Input Read Logic and coupled to the NRZI Read Logic.

The RGATENZ inputs and the Read Strobe (RDS) input to the NRZI Read Control Logic enables the NRZI Read Strobe (RSTRNZ) and forces Not Clear NRZI Data (NCLRNZDATA) high. The NCLRNZDATA signal enables the NRZI Read Logic. The Buffered Read signals and the Read Data Strobe (IRDS) from the transport provide RDS and the nine channels of Read Data (RDNZP-7), which are coupled to the Output Read Logic and the NRZI Read Control Logic. The Output Read Logic buffers and transmits the data to the controller.

The RDNZP-7 signals fed back to the NRZI Read Control provide the following information.

(1) File Mark detection and the File Mark character (FMKNZ) are supplied to the Interface Logic and to the Master Control.

(2) LRCC and CRCC detection (CCG) is supplied to the Interface Logic.

(3) Error information (HERNZ) is supplied to the Error Gating logic.

(4) End of data (RENDNZ) is supplied to the Master Control.

The HERNZ signal is supplied to the Error Gating logic, buffered, and transmitted to the controller as HARD ERROR (IHER).

RENDNZ is fed back to the Master Control and disables the RGATENZ signals. The low RGATENZ signals disable RSTR and sets NCLRNZDATA low. NCLRNZDATA clears the NRZI Read Logic and the Read operation is complete.

If a Space Forward or Reverse (NSPC) is commanded, the Error Gating logic and the Read Strobe Gating logic are disabled.

4.4.2 PE READ OPERATION

The Tracking Oscillator, the PE Read Control logic, and the PE Read Logic form a phase-lock-loop (PLL) oscillator.

The PE Read operation is enabled when the NRZ and WRT signals are low to the Master Control. The microprogram in the Master Control sets the PE Read Gate signals (RGATEPE1 and RGATEPE2) and the Identification Gate (IDGATE) high. Refer to Figure 4-5.

The microformatter reads data either in the forward or reverse direction, depending on the state of REV2.

The READ DATA (IRDP, IRD0-7) are received and buffered by the Input Read Logic and coupled to the PE Read Logic.

The free running Tracking Oscillator provides all the clocks immediately except the Shift Right clocks (SHRCLK and NSHRCLK).

Plug-in R-C networks are used to determine the basic frequency of the oscillator. This basic frequency is dependent on the transport speed. Potentiometer R3 is provided for fine frequency adjust.

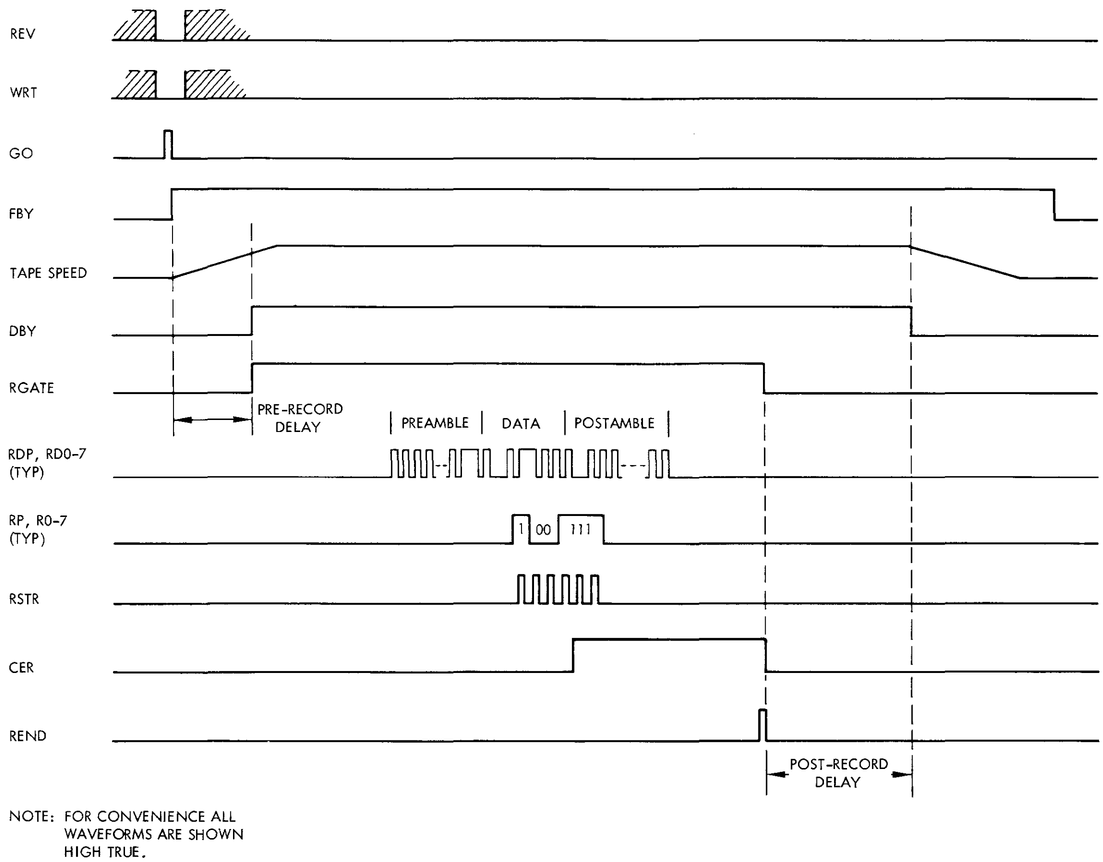

Figure 4-5. PE Read Operation Illustrating Error Correction for Last Two Data Bytes

The clocks, SHRCLK and NSHRCLK, and signals, RGATE and IDGATE, are provided to the PE Read Logic. PE information is recognized and the feedback signals are generated. The feedback signals are:

(1) Delay Gate signals (DGATE/0 and DGATE/2) are supplied to the Tracking Oscillator to phase lock the oscillator.

(2) Envelope signals (ENV/P-7, ENV/0 and ENV/2) are supplied to the Tracking Oscillator to phase lock the oscillator. The ENV/P-7 signals are also supplied to the PE Read Control logic to generate the Drop signal (DROPDET), File Mark PE (FMKPE), and ID pulse (ID).

(3) Data In (D1/P-7) and Ones Detector (NONEDET/P-7) are supplied to the PE Read Control and provide control signals Postamble Test (POSTEST), Parity Correcting (PARC), Read Enable (REN1), Preset (PRESET), and Read Strobe (RSTRPE). The error status signals, Parity (PR), Formatter Error (NFER), and the Read Counter signals (RSC1 and NRSC2) are also provided to the Error Gating Logic.

(4) Character Detector signals (CHARDET/P-7) are supplied to the PE Read Control to trigger End of Data (RENDPE).

RSTRPE is supplied to the Read Strobe Gating logic and is buffered and transmitted to the controller as READ STROBE (IRSTR).

The clocks and error signals are supplied to the Error Gating logic. All error signals provide a HARD ERROR (IHER) indication except a single channel dropout (DROPDET1). DROPDET1 is a CORRECTED ERROR (ICER). RENDPE is fed back to the Master Control and disables the RGATEPE signals (low). The Read operation is complete.

If a Space Forward or Reverse (NSPC) is commanded, the Error Gating logic and the Read Strobe Gating logic are disabled.

4.5 FUNCTIONAL DESCRIPTION

The following paragraphs describe the major functional blocks of the microformatter. These blocks are shown in Figure 4-1 and should be referred to in conjunction with the following discussion.

4.5.1 INTERFACE LOGIC

The Interface Logic receives, buffers, and transmits status signals between the transport and controller. It also provides status signals to the microformatter circuits. U112-S3 and U112-S4 select either Microformatter Address 1 or 0. U112-5 (NRZI) is used for Format definition and U112-6 (SGL) is used for Head Type definition. Refer to Table 4-2.

4.5.2 CLOCK GENERATOR

The Clock Generator provides two programmed clock pulses, WCLK and NWCLK. U187 is set to provide the proper clock frequency, dependent on the transport speed. Refer to Table 4-4 for transport and switch settings.

Table 4-4

Master Oscillator Frequency Select (U187)

Transport (ips)	Frequency (kHz)	Switch Setting							
		1	2	3	4	5	6	7	8
12.5	160	U	U	U	D	D	U	D	U
18.75	240	U	U	U	D	D	D	U	U
22.5	288	Low Speed Only *							
25	320	D	D	U	D	U	D	U	U
37.5	480	U	U	D	D	D	U	U	U
45	576	D	D	D	U	D	U	U	U
75	960	D	U	D	D	U	U	U	U
112.5	1440	U	U	U	D	U	U	U	U
12.5	1600	D	D	D	U	U	U	U	U

U = Up
D = Down

*This frequency is selected by setting the switch to the 45 ips positions and SPEED is high.

The frequency of the clock pulses is eight times the PE data rate and sixteen times the NRZI data rate.

The SPEED signal causes the output frequency to be divided by two. This signal is used on dual speed systems only.

4.5.3 MASTER CONTROL

The Master Control stores the microprogram, contains the address counter, and provides the output buffer logic and the jump and output instructions. The Master Control also provides the Write Control logic signals (WCN0, WCN1 and WCN2) and the Write Load signal (LDWRTDATA).

Also provided by the Master Control logic are the PE Read Enable logic signals (RGATEP1, RGATEP2) or the NRZI Read Enable logic signals (RGATENZ1, RGATENZ2).

4.5.4 NRZI READ CONTROL

The NRZI Read Control provides control for decoding 9-track NRZI read data. This function is enabled by Reverse Command 1 (REV1) and allows the microformatter to decode read signals in both the forward and reverse directions.

4.5.5 TRACKING OSCILLATOR

The Tracking Oscillator provides selected clock frequencies determined by the transport speed. The frequency is nominal until locked to the data rate by the Data Gate (DGATE) and the Envelope (ENV) signals. Deskew is controlled by the feedback signals, NCOPY and COPY. Refer to Table 4-5 for transport speed and frequency of the Tracking Oscillator. The frequency is selected by plug-in R-C networks and is adjusted by potentiometer R3 (Frequency Adjust).

Table 4-5

Tracking Oscillator Frequency

Tape Speed (ips)	Config. Plug 107609 Version No.	Maximum Frequency Limit (kHz)	Minimum Frequency Limit (kHz)	Exact Frequency Value (kHz)
12.5	-01	465	455	460
18.75	-02	697	683	690
22.5	-03	836	820	828
25	-04	929	911	920
37.5	-05	1394	1366	1380
45	-06	1672	1639	1656
75	-07	2788	2732	2760
112.5	-08	4181	4100	4140
125	-09	4700	4500	4600

4.5.6 PE READ CONTROL

The PE Read Control provides control for decoding 9-track PE read data. It also provides feedback signals to deskew the PE read data.

4.5.7 INPUT READ LOGIC

The Input Read Logic receives and buffers read signals from the transport.

4.5.8 PE READ LOGIC

The PE Read Logic buffers and decodes 9-track PE read data from the transport. This function is enabled by Reverse Command 2 (REV2) and allows the microformatter to decode read signals in both the forward and reverse directions. It also provides feedback signals to lock the Tracking Oscillator to the incoming data.

4.5.9 NRZI READ LOGIC

The NRZI Read Logic buffers and decodes 9-track NRZI read data from the transport. The circuits are enabled via the interface signal, READ DATA STROBE (IRDS) and an internal signal, Not Clear NRZI Data (NCLRNZDATA).

4.5.10 OUTPUT READ LOGIC

The Output Read Logic buffers and transmits read signals to the controller.

4.5.11 WRITE DATA GENERATOR

The Write Data Generator receives and buffers write signals from the controller, processes the signals, and transmits the write signals to the transport. Depending on the states of the write control signals, PE or NRZI data are written. These signals also determine when the CRCC is written.

U112-S1 selects external parity and U112-S2 selects internal parity.

4.5.12 ERROR GATING

Error Gating provides error signals to the controller. The error signals are HARD ERROR (IHER) or CORRECTED ERROR (ICER). NSPC disables Error Gating during a space command.

4.5.13 READ STROBE GATING

The Read Strobe Gating provides either a NRZI or PE read strobe to the controller. NSPC disables Read Strobe Gating during a space command.

4.6 MICROFORMATTER MAINTENANCE AND ADJUSTMENT

The following paragraphs provide a method of fault isolation between the microformatter and the transport. Electrical adjustment procedures for the microformatter are also given.

4.6.1 MICROFORMATTER—TRANSPORT(S) FAULT ISOLATION

The recommended level of fault isolation is to the Microformatter PCBA and to the transport components. Two methods of fault isolation, in order of preference, are:

(1) Use PERTEC Hand Exerciser, TE-TF1, Part No. 895460-1 and the Operating Instructions fo the exerciser, Document No. 895463, and refer to Section VI of the applicable operating and service manual for the transport.

— OR —

(2) Use the procedure defined in Paragraph 4.6.1.1.

4.6.1.1 Fault Isolation

It is recommended that an all ones tape for NRZI transport configurations, or an all zeros tape for PE transport configurations be generated. Also, a test tape to check errors and file marks should be available.

(1) Check the interface commands between the microformatter and the transport(s) using an oscilloscope. Refer to the fault isolation flow chart given in Figure 4-6.

(2) Using the previously generated test tapes, monitor (with an oscilloscope) the read interface lines between the microformatter and transport(s).

(3) Remove the all ones or all zeros tape from the transport.

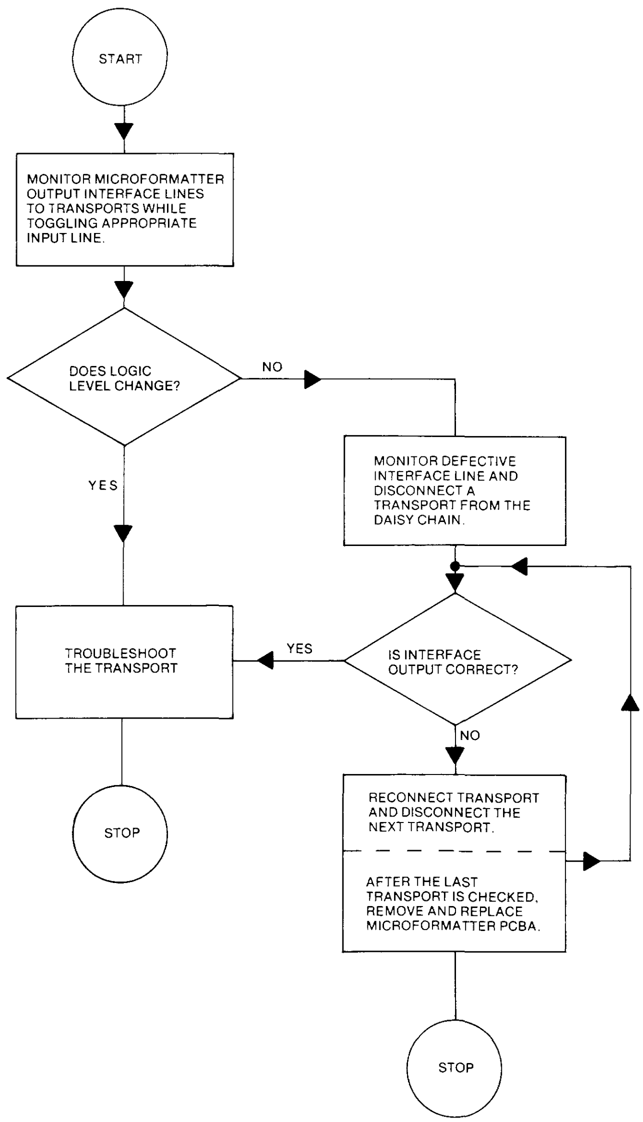

Figure 4-6. Fault Isolation Flow Chart

(4) Load a work tape, which is known to be good, onto the transport. Write an all ones or an all zeros tape. Monitor the write interface lines between the microformatter and the transport(s).

When the fault is isolated to the microformatter or the transport, either replace the Microformatter PCBA or refer to Section VI of the applicable operating and service manual to fault isolate within the transport.

4.6.2 MICROFORMATTER ADJUSTMENTS

Electrical adjustments to the Microformatter PCBA are made as follows.

(1) Connect a DVM between TP1 and TP2 on the Microformatter PCBA.

(2) Acceptable Limits:

- +5.0v (maximum)
- +4.9v (minimum)

(3) If the reading observed in step (2) is outside the acceptable limits, adjust R6 on Power Supply II PCBA for +4.95v.

(4) Set switch U112 as defined in Table 4-1, 4-2, or 4-3.

(5) Set switch U187 as defined in Table 4-4.

(6) Connect a frequency counter between TP3 and TP4 on the Microformatter PCBA.

(7) Monitor the output of the frequency counter. The frequency of the Tracking Oscillator should fall within the maximum and minimum frequency limits given in Table 4-5 for the transport tape speed.

(8) If the observed frequency falls outside the maximum and minimum frequency range, adjust R3 on the Microformatter PCBA for the exact Tracking Oscillator frequency given in Table 4-5.

4.7 POWER SUPPLY II PCBA (NOT USED ON FT1000 SERIES)

Refer to Schematic No. 107614 and Assembly No. 107615 for discussion of the power supply functions.

(1) Rectifier
(2) +5v Regulator
(3) Overcurrent Protection
(4) Overvoltage Protection
(5) Power Supply Enable

4.7.1 RECTIFIER

Rectifier CR1 is a full wave rectifier. The output of the rectifier is filtered, fused, and supplied to the regulator.

4.7.2 +5V REGULATOR

The +5v Regulator consists of U1, R5, R6, R7 and Q1. The regulator provides base drive to the series pass transistor, Q1. The voltage divider (R5, R6 and R7) determines the voltage output. R6 is adjusted to provide +4.95v at TP1 on the Microformatter PCBA. The regulator also has a current foldback circuit.

4.7.3 OVERCURRENT PROTECTION

The overcurrent protection is provided by a voltage divider (R2, R3 and R4). R3 is the current sense resistor. If the current increases across R3, the signal is fed back to U1 causing U1 to decrease its output. A short at the output causes U1 to shut off and remain shut off until the short is removed.

4.7.4 OVERVOLTAGE PROTECTION

The overvoltage protection is provided by Q2, VR1 and SCR1. If the output voltage exceeds +5.7 volts, VR1 conducts. This causes Q2 to conduct and fire SCR1. When SCR1 fires, a direct short (crowbar) occurs causing fuse F1 to open.

4.7.5 POWER SUPPLY ENABLE (PSEN)

The POWER SUPPLY ENABLE signal (IPSEN) is used to reset all microformatter logic to the quiescent state. This is done while the +5v supply is being established after power is applied and while the supply is decaying after power is turned off. This ensures that the logic is in a defined state after power on and that no spurious signals are sent to the transport logic.

When ac power is applied, the regulated output builds up to +5v causing C6 to charge through R14 and R15. When the voltage on C6 reaches 2.5v, the voltage on the base of Q5 will be greater than the voltage on the base of Q3. Q4 and Q5 will then turn on causing the output PSEN to go to +4v approximately 50 msec after power is applied. A loss of dc power is detected by Q3 when the voltage on C7 drops below +3v.

4.8 POWER SUPPLY II ELECTRICAL ADJUSTMENTS

The following paragraphs provide a method of fault isolation to a stage in the power supply.

4.8.1 POWER SUPPLY II

Figure 4-7 is a functional block diagram of the power supply. Table 4-6 lists measurement points and voltage readings for a normally operating power supply. All readings assume that the output voltage of the power supply as measured between pins 3 and 1 of Power Supply J2 is:

- +5.36v (maximum)
- +5.14v (minimum)

In the event that the voltage read between J2 pins 3 and 1 falls outside the acceptable limits, perform the adjustment given in Paragraph 4.8.2.

4.8.2 POWER SUPPLY II ALIGNMENT

Electrical adjustments to the power supply are made as follows.

(1) Connect a DVM between TP1 and TP2 on the Microformatter PCBA.

(2) Acceptable Limits:

- +5.0v (maximum)
- +4.9v (minimum)

(3) If the reading observed in step (2) is out of tolerance, adjust R6 on Power Supply II PCBA until a voltage reading of +4.95v is obtained between TP1 and TP2 on the Microformatter PCBA.

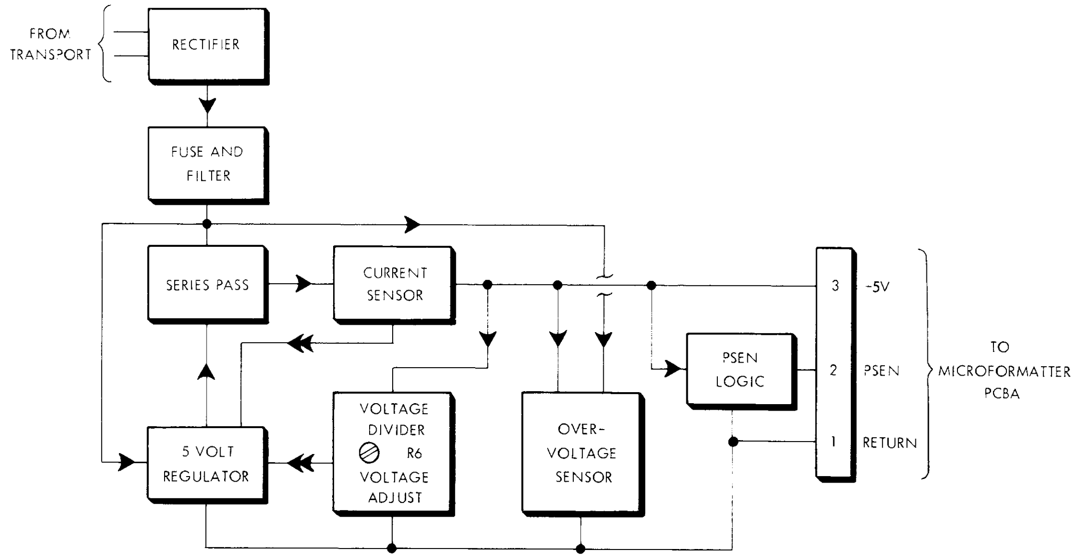

Figure 4-7. Power Supply Functional Block Diagram

Table 4-6
Nominal Power Supply Voltage Readings

Measurement Point	Voltage Reading
Across rectifier input	10.4v ac
Q1E/GND	+10.5
Q1B/GND	+9.0
Q1C/GND	+6.0
JCT R3-R5/GND	+5.25
JCT R6-R7/GND	+1.8
VR1 Cathode/GND	+5.2
Q2B/GND	+5.2
Q2C/GND	0V

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