MODEL NO. T1940-96

SERIAL NO. 322802620

MODEL T1940-96
GCR/PE
READ AFTER WRITE
TAPE TRANSPORT

SUBSIDIARY OF TRIUMPH-ADLER

OPERATING AND SERVICE MANUAL NO. 107930

FOREWORD

This manual provides operating and service instructions for the Model T1940-96 GCR/PE Tape Transport, manufactured by Pertec Computer Corporation, Chatsworth, California.

The T1940-96 Tape Transport is a magnetic tape data storage unit designed for writing and reading data in Group Coded Recording (GCR) and Phase Encoded (PE) recording formats.

Section I provides a brief physical and functional description. Section II defines installation and initial checkout requirements. Section III describes the operating procedures. Sections IV and V discuss overall and detailed theories of operation, respectively. Section VI provides maintenance and troubleshooting procedures. Section VII lists parts that may be required for maintenance.

A Multiplexer Interface Adapter (MIA) PCBA is used in the tape transport to make it compatible with an F6250 Formatter or equivalent. The MIA is discussed in a separate Addendum placed in the back of this manual.

SERVICE AND WARRANTY

This Pertec Computer Corporation (Pertec) product has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected wherever possible from manufacturer's off-the-shelf stock. Should a component fail, it may be readily replaced from Pertec Peripherals Division or your local supplier. The unit has been designed for plug-in replacement of circuit boards or major components which will ensure a minimum of equipment down time.

Pertec warrants products to be in accordance with its applicable specifications and to be free from defect in workmanship and material under normal use and service for a period of twelve (12) months from the date of shipment to Buyer or for such shorter period as may be set forth by contract.

Pertec's sole and exclusive obligation under this warranty is limited to repair or replace, at Pertec's option, at its authorized repair centers, all Products that are returned to said repair centers within the applicable warranty period and found by Pertec to be defective, excluding those Product parts that are subject to normal wear. In the event Pertec's inspection discloses that returned Product is not defective, the Buyer shall reimburse Pertec for shipment costs to return Product to Buyer.

Buyer is responsible for properly packaging Product to be returned, at Buyer's expense, in accordance with applicable user manual instructions and shall ship Product prepaid at Buyer's expense. Pertec shall return Product to Buyer prepaid at Pertec's expense.

This warranty shall immediately be null and void if, in Pertec's sole judgement, the Product has been altered or repaired other than with authorization from Pertec and by its approved procedures, has been subjected to misuse, abuse, negligence or accident, damaged by excessive current, damaged in shipment, subjected to improper environmental conditions, or had its serial numbers and/or other Product markings altered, defaced or removed.

Adjustments of the Products, as set forth in Pertec's Operating and Service Manuals, are the responsibility of the Buyer and excluded from this warranty.

This warranty will remain in effect notwithstanding Buyer's shipment to third parties, but warranty remedies defined herein are applicable only to Buyer and are not transferrable.

Buyer shall disclose to third parties, prior to sale, the precise terms of this warranty and all the disclaimers and limitations set forth herein and shall indemnify Pertec from any failure to make such disclosure and from any warranties made by Buyer beyond those set forth herein.

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Please read the instruction manual thoroughly as to installation, operation, maintenance, and component reference list.

Contact your local Pertec Division Sales office for servicing and maintenance on all Pertec equipment except flexible and D8000 disk drives. Flexible and D8000 disk drives must be returned to the Peripherals Division factory Repair Depot for servicing.

Please contact the following groups for assistance with your specific problem.

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- For all servicing requirements on Pertec Peripherals Division equipment, please contact your local Pertec Sales office.

NEW EQUIPMENT ORDERS
- For price quotation, order placement, and delivery schedules on new equipment orders contact your local Pertec Sales office.

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21111 Erwin Street, Woodland Hills, California 91367, (213) 999-2020
Mailing Address: P.O. Box 2198, Mail Station 40-08, Chatsworth, CA 91311

Our Woodland Hills facility is staffed to provide assistance in the following areas.

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- For spare parts price quotation, spare parts order placement and delivery schedules.

SPARES SUPPORT
- For part number identification, recommended spare parts lists and other questions on spare parts.

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9600 Irondale Avenue, Chatsworth, California 91311, (213) 882-0030
Mailing Address: P.O. Box 2198, Mail Station 42-06, Chatsworth, CA 91311

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- For applications information.
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Mailing Address: P.O. Box 2198, Mail Station 51-01, Chatsworth, CA 91311

Our Canoga Park Facility is staffed to provide assistance in the following areas.

REPAIR DEPOT
- For all questions related to equipment sent back or being sent back to the Repair Depot. This includes schedules, repair costs, or refurbishments and authorization to return equipment for repair.
- All equipment being returned for repair should be sent to the Peripherals Division Repair Depot, 21029 Osborne Street, Canoga Park, California, 91307.
- Paperwork sent with the equipment being returned for repair should include the Returned Goods Authorization (RGA) number.

EMERGENCY SPARES
- For spare parts that are required immediately to repair a down unit at a customer (end-user) site, and warranty exchange.

EUROPE AND INDIA

10 Portman Road, Reading, Berkshire RG3 1DU, England
Phone Reading (734) 582115 / TWX 847-101

Users of Pertec Peripherals Division equipment in Europe and India should direct all inquiries on the subjects listed for North America to the Reading office.

Servicing of all Pertec Peripherals Division equipment is coordinated through the Reading office, including U.S. OEMs that ship systems to Europe.

PACIFIC

Users of Pertec Peripherals Division equipment in Australia, Japan, New Zealand, and South America should direct all inquiries on the subjects listed for North America to their local Pertec representatives.

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SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides a brief physical description, functional description, and concise specifications for the Dual Format (GCR/PE) Synchronous Read After Write Tape Transport, Model T1940-96, manufactured by Pertec Computer Corporation, Chatsworth, California. Group-Coded Recording (GCR) or Phase-Encoded (PE) modes of operation are selectable by manual switching or software control. Tape speed options require different hardware configuations.

1.2 PURPOSE OF EQUIPMENT

The Dual Format (GCR/PE) Synchronous Read After Write Tape Transport (refer to Figure 1-1) provides accessible storage of information in binary form. It accepts control signals and data from a Controller, either directly or through a Formatter. For PE format, the Formatter may be a separate unit or included in the transport as optional circuitry. For GCR or GCR/PE, the Multiplexer Interface Adapter PCBA and the optional, separate, Pertec F6250 Formatter are recommended.

The T1940-96 transport has the capability of synchronously recording and reading data on 9-track magnetic tape at speeds of 1.905 or 3.175 m/s (75 or 125 ips) in either 246 c/mm (6250 cpi) Group Coded Recording format or 63 c/mm (1600 cpi) Phase Encoded (PE) IBM-compatible format. Data recorded in either format can be completely recovered when played on an IBM digital tape transport or its equivalent. The standard T1000 series does not include a 7-track model; therefore, 7-track selection circuits shown in some documentation are not used in equipment covered in this manual.

Rewind time is 80 seconds, maximum, and 65 seconds, nominal, for 3.175 m/s (125 ips) models; and 133 seconds, maximum, and 108 seconds, nominal, for 1.905 m/s (75 ips) models.

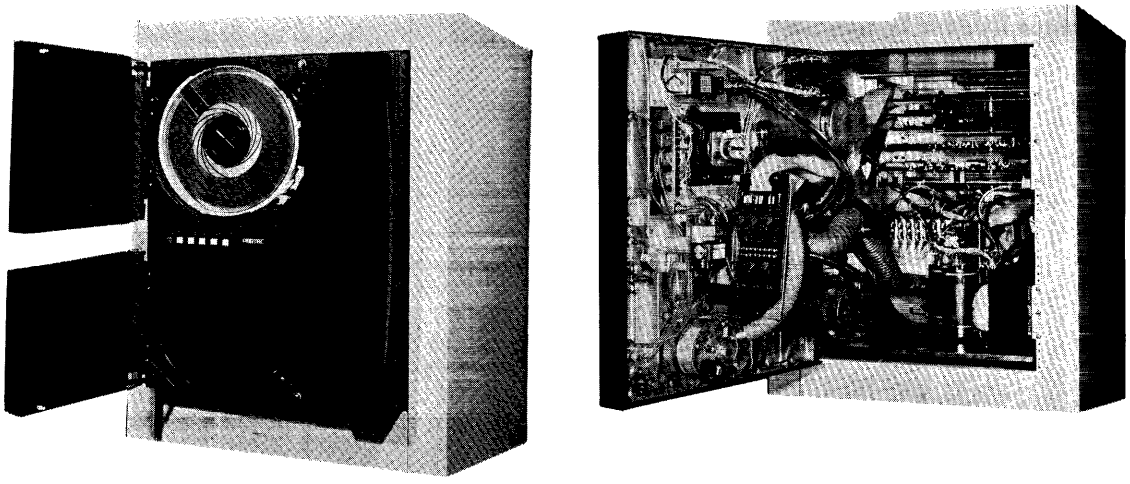


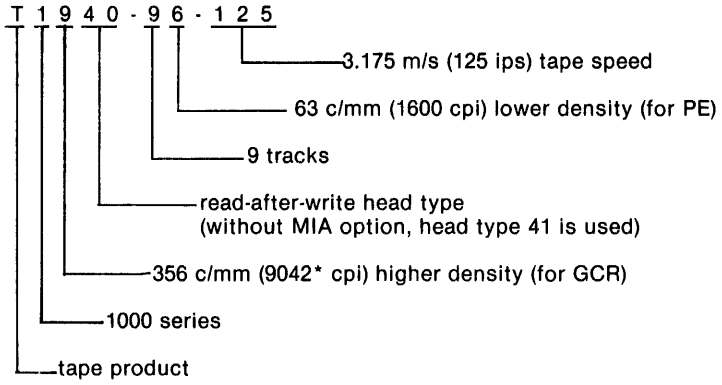
Figure 1-1. Model T1940 Tape Transport

The transport is equipped with a dual-stack head with read and write portions separated by 3.81 mm (0.15 inch). The dual-stack head enables reading data just recorded after the tape has moved approximately 3.81 mm (0.15 inch). Thus, in Write Mode, read and write operations are performed in a single pass. The head assembly is also equipped with an erase head, which is automatically activated when writing, to prepare the tape before it passes over the write head.

The transport may be optionally configured to use any of various voltages between 190 and 250v ac, in 10 volt increments, at either 50 or 60 Hz. Line variations must be within ± 10 percent from normal.

1.3 MODEL IDENTIFICATION

The T1940 transport designates a group within the T1000 series of tape transports. The complete model number identifies a specific configuration as illustrated in the following example:



1.4 MECHANICAL AND ELECTRICAL SPECIFICATIONS

Table 1-1 details the mechanical and electrical specifications for the transport.

1.5 PHYSICAL DESCRIPTION

All electrical and mechanical components of the transport (refer to Figure 1-2) are included in three major subassemblies:

(1) Transport Base Assembly — includes the hinged base for the tape transport reels and related mechanisms. (Refer to Paragraph 1.5.3.)

(2) Power Pack Assembly — includes power transformers, rectifiers, capacitors, ac motor, blower, and compressor. (Refer to Paragraph 1.5.1.)

(3) Card Cage Assembly — includes the printed circuit boards (PCBAs) for control and data processing. (Refer to Paragraph 1.5.2.)

The three subassemblies that comprise the complete transport assembly are collectively referred to as the transport. The complete assembly is designed for mounting in a standard 482.6 mm (19-inch) EIA rack and requires 622.3 mm (24.5 inches) vertical space. Power is supplied through a standard cord and 3-pin plug.

*Includes 246 c/mm (6250 cpi) data characters and up to 110 c/mm (2792 cpi) error-checking and control characters.

Table 1-1
Mechanical and Electrical Specifications

Tape (ANSI X3.40) Width Thickness	 12.6492 ±0.0508mm (0.498 ±0.002 inch) 0.0381 mm (1.5 mil)
Tape Tension	2.780 N (10.0 $^{+0.0}_{-1.0}$ ounces) nominal
Reel Diameter (Autoload)	266.7 mm (10.5 inches) maximum (Note 1) and Easy Load Cartridge #1 and #2*
Recording Modes (IBM Compatible) (Meaningful data bits)	246 c/mm (6250 cpi) GCR per ANSI X3.54-1976 63 c/mm (1600 cpi) PE per ANSI X3.39-1973
Magnetic Head	Dual Stack (with Erase Head)
Tape Speeds (Standard Options)	1.905 and 3.175 m/s (75 and 125 ips)
Instantaneous Speed Variation (ISV)	±3 percent
Long Term Speed Variation	±1 percent, forward; ±2 percent, reverse
Rewind Time using 731.5 m (2400 ft) tape: For 3.175 m/s (125 ips) Transports For 1.905 m/s (75 ips) Transports	 65 seconds, nominal; 80 seconds maximum 108 seconds, nominal; 133 seconds maximum
Tape Cleaner	Dual blade type connected to vacuum supply
Interchannel Displacement Error Read Read After Write	 3.81 μm (150 μinches) maximum (Note 2) 8.89 μm (350 μinches) maximum (Note 3)
Stop/Start Time (Inversely proportional to tape speeds): For 3.175 m/s (125 ips) Transports For 1.905 m/s (75 ips) Transports	 1.3 ±0.1 milliseconds 2.0 ±0.2 milliseconds
Start Distance	1.91 $^{+0.25}_{-0.38}$ mm (0.075 $^{+0.010}_{-0.015}$ inch)
Stop Distance	2.16 $^{+0.25}_{-0.38}$ mm (0.085 $^{+0.010}_{-0.015}$ inch)
Beginning of Tape (BOT) and End of Tape (EOT) Detectors (Note 4)	Photoelectric
Weight (maximum)	124.75 kg (275 pounds)
Rack Requirements	Standard 482.6 mm (19-inch) EIA
Rack Opening Dimensions Height Width Depth (from face of mounting angle to rear of cabinet) Depth of front recess (from face of mounting angle to face of cabinet)	 622.3 mm (24.5 inches) minimum 482.6 mm (19.0 inches) minimum 584.2 mm (23.0 inches) minimum 736.6 mm (29.0 inches) maximum 38.1 mm (1.5 inches) maximum
Door Assembly thickness (from mounting angle face to face of door)	101.6 mm (4.0 inches)
Temperature (Electronics) Operating Non-operating	 5° to 44°C (40° to 112°F) (Note 5) −46° to 71°C (−50° to 160°F)
Humidity Operating Non-operating	 30% to 80% RH (without condensation) 5% to 95% RH (without condensation)
Altitude Operating Non-operating	 0 to 2134m (0 to 7,000 feet) 15,240m (50,000 feet) maximum
Power Volts ac Frequency	 220, 230, 240, 250 (Note 6) 50 ±2 or 60 ±2 Hz
Power Consumption (nominal) Standby (Loaded) Start/Stop	 1150 watts 2450 watts

NOTES:
* Easy Load #1 and #2 are Registered Trademarks of IBM.

1. 177.8 mm (7-inch) and 216.0 mm (8.5-inch) reels may be used but cannot be autoloaded.
2. The maximum displacement between any two bits of a character when reading an IBM master tape using the read section of the read-after-write head.
3. The maximum displacement between any two bits of a character on a tape written with all ones using the write section of the read-after-write head.
4. Approximate distance from detection area to read head gap is 60.96 ±1.52 mm (2.40 ±0.06 inches).
5. For data transfer, the operating temperature is dictated by the nature of the tape material. For 35°C (95°F) environment, outside cabinet, ventilate at 0.1888 m^3/s (400 cfm). Allow additional ventilation for other units sharing cabinet.
6. Line variations must be within ±10 percent.

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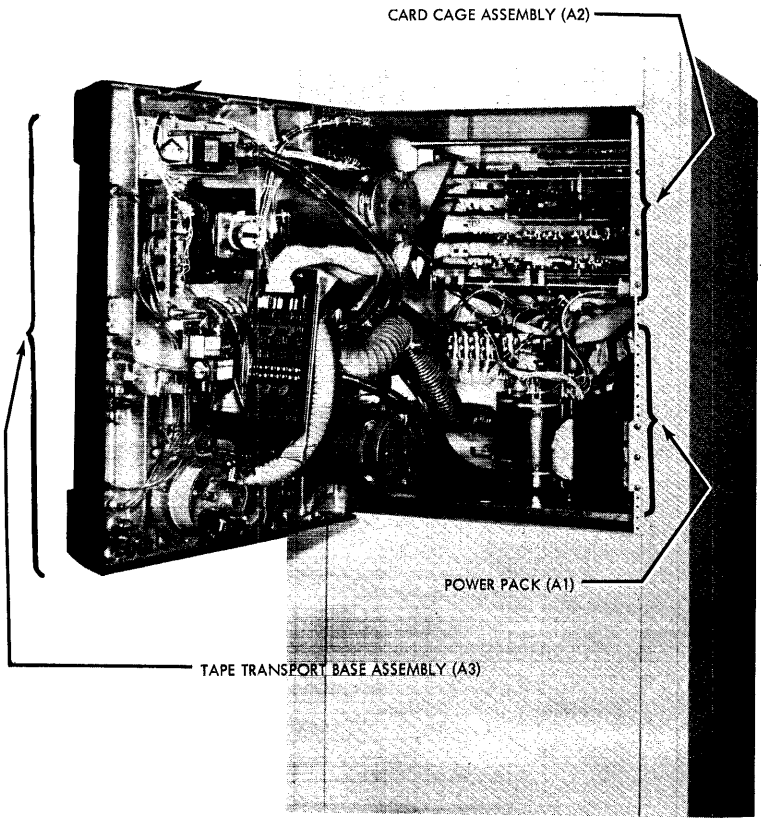

Figure 1-2. Tape Transport Major Subassemblies

The assembly doors are latched to protect the magnetic tape, heads, capstan, and other tape transport components from dust. The doors should remain closed during normal operation to ensure maximum data reliability and, when necessary, should be opened only by means of the handle flanges located near the catches.

To access the cabinet interior, proceed as follows:

(1) Carefully pull open the reel doors, using the flanges provided for this purpose.

(2) Press the upper and lower latches that secure the buffer box door, and open the door.

(3) With a screwdriver, loosen the base assembly latch, located below the right-hand buffer box (tape-loop air column), and swing the assembly on its hinges.

The controls and indicators are located near the center of the front panel of the transport and are accessible for operation with the doors closed. Refer to Table 1-2.

1.5.1 POWER PACK ASSEMBLY

The Power Pack Assembly includes the fuses, rectifiers, capacitors, relays, etc., and the following subassemblies.

(1) Transformer

(2) Compressor

(3) AC Motor

(4) Blower

Table 1-2 .
Front Panel Controls and Indicators

CONTROLS	
Identification	Description and Purpose
0—3	Thumbwheel switch for setting the transport unit's selection (address) number (4 to 9 not used).
POWER	Input power control switch.
LOAD/REW	Momentary switch for initiating either load or rewind procedure, both of which terminate with tape at the beginning of tape (BOT) position.
ON-LINE	Momentary switch for placing the unit on line to the controller.
UNLOAD	Momentary switch to command the return of the tape to the supply reel and to close the cartridge in preparation for removing the reel of tape.
RESET	Momentary switch for initializing all circuits prior to operation. Also terminates any operation in progress except forward and reverse in Maintenance mode.
DENSITY	Density selector: 6250, GCR; 1600, PE
INDICATORS	
Identification	Meaning When Lighted
POWER	Power On.
BOT	Beginning of tape mark is sensed.
ON LINE	Transport is on line to the controlling device.
FILE PROTECT	Write mode is inhibited.
LOAD FAULT	Proper tape loading has not been achieved.
6250	246 c/mm (6250 cpi) Density Mode (for GCR) has been selected.
1600	63 c/mm (1600 cpi) Density Mode (for PE) has been selected.

1.5.2 CARD CAGE ASSEMBLY

The Card Cage Assembly includes the following major subassemblies.

(1) Interconnect D/D1 PCBA
(2) Reel Servo PCBA
(3) Capstan/Regulator PCBA
(4) Read PCBA
(5) Write PCBA
(6) Control M/M2 PCBA
(7) Multiplexer Interface Adapter (MIA) — Optional; see Addendum
(8) Self Test PCBA*

*Optional

The Interconnect F (or F1) PCBA and the GCR/PE Preamp 1 PCBA, although mounted on the Base Assembly, are considered part of the card cage assembly in the discussions of electrical circuitry.

NOTE

Interconnect D and D1 PCBAs are interchangeable as are Interconnect F and F1 PCBAs; however, adjustment and maintenance procedures for F and F1 are different, as covered in Section VI.

1.5.3 BASE ASSEMBLY

The Base Assembly includes the following subassemblies.

(1) Control and Indicator Assembly
(2) Buffer Box Door Assembly
(3) Trim Assembly
(4) Capstan Motor Assembly
(5) Reel Motor Assembly
(6) Reel Hub Assembly
(7) Pressure Transducer Assembly
(8) Column Switch Assembly
(9) EOT/BOT Assembly (End-of-Tape/Beginning-of-Tape Sensor)
(10) TIP (Tape in Path) Assembly
(11) Pack Sense Assembly (Low Tape Sensor)
(12) Reel Sense Assembly
(13) Vacuum Valve Assembly
(14) Pressure Valve Assembly
(15) Write Lockout Assembly
(16) Interconnect F PCBA or Interconnect F1 PCBA
(17) GCR/PE Preamp 1 PCBA
(18) Head
(19) Cartridge Actuator Assembly

1.5.4 REFERENCE DESIGNATION PLAN

Reference designations conform generally to published industry standards. The complete designation includes the symbol marked on the equipment and a prefixed symbol designating the next higher assembly (e.g., terminal board number one (TB1) in the power pack assembly (A1) is designated as A1TB1 while terminal board number one (TB1) in the card cage assembly is designated A2TB1.

Table 1-3 is a list of major components and connectors identified by reference designations. Resistors, capacitors, and other small items are identified on the schematics and are not included in this list. Items have been selected for listing on the basis of their significance in circuit tracing and in understanding the theory of operation.

NOTE

Part numbers, pin numbers, reference designation numbers, specifications, etc., used in this manual are typical of T1000 series Transports but should not be considered accurate for all models. For precise information, refer to the specific drawing package, included as part of Section VII, in manuals supplied with the equipment.

1.5.5 REFERENCES TO DRAWINGS, SCHEMATICS, ETC.

References to engineering drawings will be by drawing number (e.g., Schematic No. 000000). Reference to detail areas will be by sheet number, horizontal location number, and vertical location letter (e.g., zone 2-7G) for sheet 2, near the intersection of coordinates 7 and G as noted in the margins of the drawings. The drawing number will not be repeated for later references in the same discussion unless necessary for clarity.

Table 1-3
Major Reference Designations

Reference Designator		Location	Description/Purpose
Assy	Item		
Power Pack Asembly			
A1		Lower shelf	Power Pack Assembly.
	CB1	Rear panel	AC power input circuit breaker switch.
	S2	Front face of rear panel	Solid-state switch operated by manual switch S1, to control transport power.
	S3	Front face of rear panel	Solid state switch operated by vacuum sensing system, and dc power ON, to control blower compressor and elapsed time meter.
	TB1	Rear panel (TB1 is covered to prevent accidental contact with high voltage terminals.)	Terminal board used mainly for interfacing input power with primary winding of transformer T1.
	T1	Lower shelf	Transforms input ac power to lower voltages.
	CR1,CR2, CR3	Lower shelf	Rectify T1 secondary winding outputs to provide basic unregulated dc power.
	C1—C5 (C1, C2 for 24v dc; C3 for 12v dc; C4, C5 for 36v dc.)	Lower shelf	DC power smoothing capacitors.
	E1	Front side or rear panel at ac input connector	Ties ac input ground line to chassis.
	E2	Above ± 36v capacitors	Ties dc common bus to chassis ground.
	E3,E4	Connects transport mechanism base assembly to cabinet	Grounds hinged base assembly to main chassis.
	F1—F7 (F2, F3 for 24v dc; F1 for 12v dc; F4—7 for 36v dc.)	Fuse panel below card cage	DC power fuses.

Table 1-3
Major Reference Designations (Continued)

Reference Designator		Location	Description/Purpose
Assy	Item		
Card Cage Assembly			
A2		Upper bay area of cabinet	Card cage for transport logic circuitry.
	TB1	Rear side of vertically mounted interconnect PCBA	Power supply terminal board.
	J1—J3	Interconnect D/D1 PCBA	Connectors for P1—P3 on Multiplexer Interface Adapter or other optional circuit boards.
	J4* (J102)	Read PCBA in card cage	For ribbon cable to 9TK Preamp PCBA on base assembly.
	J5	On Interconnect D/D1 PCBA	Main connector for Read PCBA P5* (P103).
	J6* (J1)	On Write PCBA	For ribbon cable to 9TK Preamp PCBA.
	J7	On Interconnect D/D1 PCBA	Main connector for Write PCBA P7* (P1).
	J8	On Interconnect D/D1 PCBA	Main connector for Control M/M2 PCBA.
	J10	On Control M/M2 PCBA	For ribbon cable to manual controls on transport front panel.
	J11	On Interconnect D/D1 PCBA	Main connector for Capstan/Regulator PCBA.
	J12	On Interconnect D/D1 PCBA	Main connector for Reel Servo PCBA.
	J13	On Reel Servo PCBA	For +36v to unregulated dc supply.
	J14	On Reel Servo PCBA	For supply reel motor drive power (+).
	J15	On Reel Servo PCBA	For supply reel motor drive power (—).
	J16	On Reel Servo PCBA	For —36v to unregulated dc supply.
	J17	On Reel Servo PCBA	For +36v from unregulated dc supply.
	J18	On Reel Servo PCBA	For takeup reel drive power (+).
	J19	On Reel Servo PCBA	For takeup reel drive power (—).
	J20	On Reel Servo PCBA	For —36v from unregulated dc supply.
	J21	Accommodates P21 of cable from J24 in card cage to Interconnect F/F1 PCBA on base assembly.	For connecting card cage circuits to base assembly sensor and control circuits.
	J22	On GCR/PE Preamp 1 PCBA attached to rear of base assembly)	Read head input to Preamp PCBA.
	J23	On GCR/PE Preamp 1 PCBA	Output from GCR/PE Preamp 1 to write heads.
	J24	On Interconnect D1 PCBA	For cable to Interconnect F/F1 PCBA. (Cable is captive on Interconnect D PCBA.)
	J25* (J2)	On Write PCBA	Connects to Multiplexer Interface Adapter PCBA.
	S1	On Control M/M2 PCBA	Maintenance switch for manually controlling tape motion.
	S1	On Reel Servo PCBA	Maintenance switch for controlling reel servo operation.

*Designator on earlier PCBA's is shown in parentheses.

Table 1-3
Major Reference Designations (Continued)

Reference Designator		Location	Description/Purpose
Assy	Item		
Tape Transport Base Asembly			
A3		Hinged base assembly	Tape transport mechanism including capstan, reel motors, etc.
	TB1—TB4	On Interconnect F/F1 PCBA, attached to top of inside surface of hinged base assembly	Terminal boards for feeding signals from base assembly source and control mechanisms to Interconnect F/F1 PCBA for processing and/or delivery to logic through J21 and Interconnect D/D1 PCBA.
	CM	On rear side of base assembly	Capstan Motor.
	SM	On rear side of base assembly	Supply reel motor.
	TM	On rear side of base assembly	Takeup reel motor.
	M1	On rear side of base assembly	Cartridge motor.
	J22,J23	——	See Card Cage Assembly part of table.
	E1,E2	On GCR/PE Preamp 1 PCBA	Connectors for leads to erase head.
	S1	Front Panel	Power ON-OFF switch.
	S2	Front Panel	LOAD/REW switch for commanding tape to rewind to BOT and load positions.
	S3	Front Panel	ON LINE switch for placing transport on line in the host system.
	S4	Front Panel	UNLOAD switch for rewinding tape for removal of supply reel.
	S5	Front Panel	RESET switch for stopping current mode and resetting circuits for new command.
	S6	Front Panel	6250—1600 density selector.
	S7	Not used	
	S8	Front Panel	For setting the transport's identification number in the host system.

1.6 FUNCTIONAL DESCRIPTION

Transport operation depends on a combination of functions, as shown in the simplified block diagram in Figure 1-3.

(1) System Control
(2) Air System
(3) Capstan Servo
(4) Reel Servo
(5) Read
(6) Write
(7) Power Supply

The System Control Function processes the interface and manual commands to initiate and coordinate the other functions in order to efficiently write and read data on the tape.

The Air System Function controls and monitors the air pressures at various points along the tape path. Precisely controlled pressures are required to shape the tape loops and to maintain optimum tape tension.

The Capstan Servo Function controls the capstan motor which also establishes direction and speed of the tape as it is transported between the reels. Capstan rotation is monitored by electronic interpretation of a feedback signal that is produced by a tachometer mechanically linked to the capstan.

NOTE

Synchronous forward and synchronous reverse speeds are carefully controlled for optimum reading and writing, as distinguished from the noncritical rewind speed.

The Reel Servo Function controls the speed of rotation of the tape reels on the basis of feedback information pertaining to formation of the tape path as interpreted from Air System Function pressure sensing. Supply reel and takeup reel control is handled by two essentially similar but separate servo loops.

The Read Function processes data picked up from the tape by the read heads and translates the information from the recorded GCR or PE format to binary data acceptable to the external controlling circuits. The function includes the read-after-write capability that permits verification of the execution of a write command while writing is in progress. GCR and PE formatted data are decoded in a separate unit, such as a Pertec F6250 Formatter.

NOTE

If the transport uses the Multiplexer Interface Adapter (MIA) for adapting to the F6250 Formatter or similar external equipment, utilizing bidirectional lines, the data read after writing will not be available for external checking, but are used internally as the bases for the Amplitude Track in Error (AMTIE) signals.

The Write Function prepares incoming GCR or PE formatted data for recording and writes the information on the tape in the selected format. In GCR mode, the Write PCBA also monitors read-after-write data and produces the Amplitude Track in Error (AMTIE) signals.

The Power Supply Function includes transforming, rectifying, regulating, and distributing input electric power as required to supply the various electronic and electrical operations.

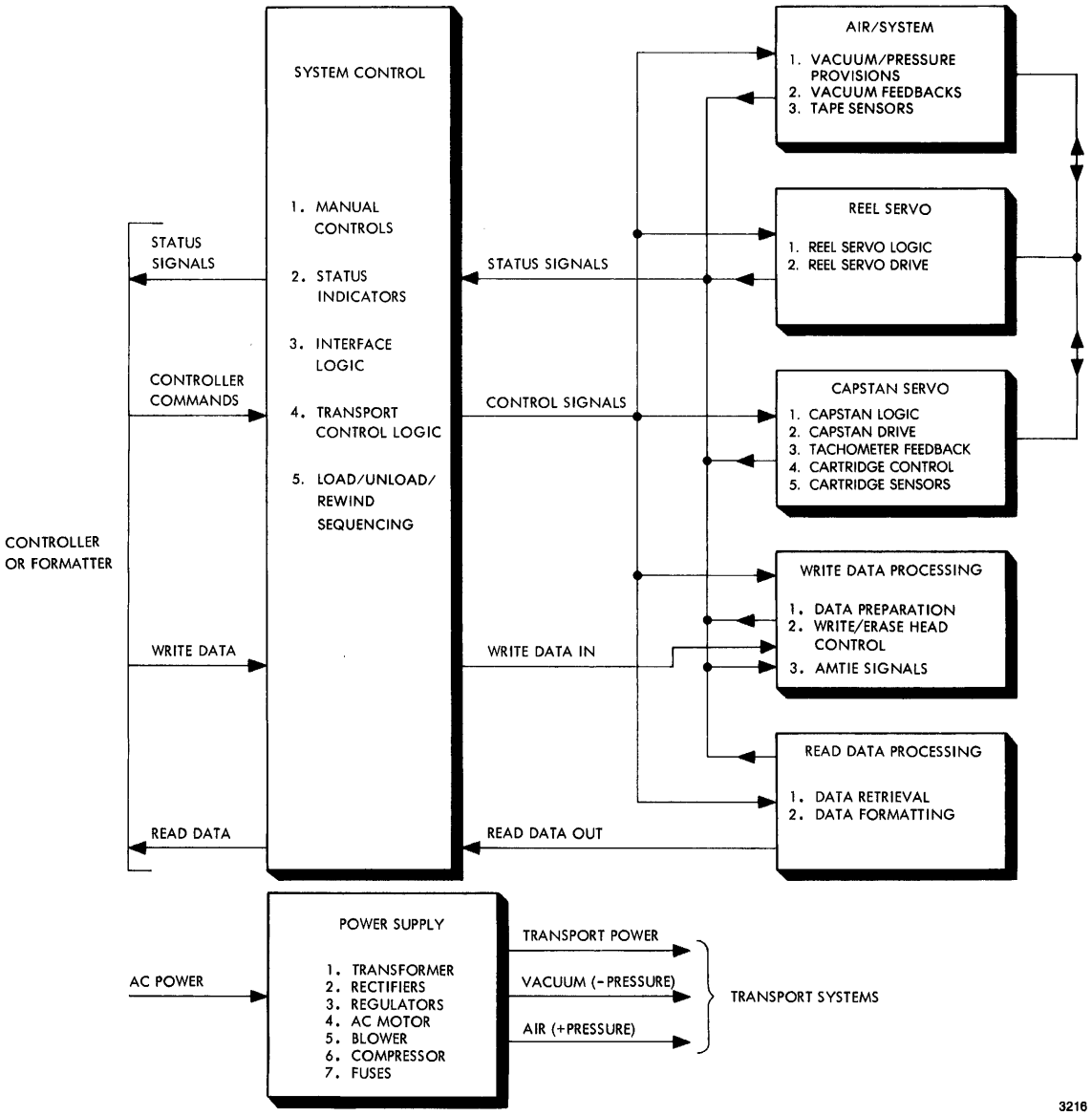

Figure 1-3. Transport Simplified Block Diagram

SECTION II
INSTALLATION AND INITIAL CHECKOUT

2.1 INTRODUCTION

This section contains instructions for uncrating the transport, and the procedure for electrically connecting and performing the initial checkout of the transport.

2.2 UNCRATING THE TRANSPORT

The transport is shipped in a protective container which meets the National Safe Transit Specification (Project 1A, Category 1). The container is designed to minimize the possibility of damage during shipment. The following procedure describes the recommended method for uncrating the transport. Refer to Figure 2-1 in conjunction with the procedure.

(1) Place shipping carton in the position shown in Figure 2-1A.

(2) Remove the shipping bands from the carton.

WARNING

SHIPPING BANDS ARE UNDER SUBSTANTIAL TENSION. EXERCISE CAUTION WHEN REMOVING BANDS.

(3) Remove cover cap, bonded assembly, tray and sleeve (Figure 2-1A).

(4) Carefully tip the frame and base to position shown in Figure 2-1B.

WARNING

THE PACKAGED UNIT WEIGHS OVER 125 KG (275 LBS). SUFFICIENT HELP MUST BE USED TO AVOID INJURIES. NOTE POSITION SHOWN IN FIGURE 2-1B.

(5) Remove tray, fiberboard assembly, and base assembly (Figure 2-1B).

(6) Remove plastic bag from transport.

(7) Remove tape from doors of the transport.

(8) Remove installation kit.

(9) Open buffer box door and remove microfoam padding.

(10) Open the installation kit. Remove the power cord and connect it to the back of the power chassis.

(11) Perform the procedure detailed in Paragraphs 2.3. and 2.4.

NOTE

Initial checkout procedures outlined in Paragraphs 2.3 and 2.4 are conducted before removing the transport from the shipping frame.

2.3 POWER CONNECTIONS

A quick change power cord is supplied for use in a polarized 220v outlet. Table 2-1 lists (in several languages) the color code for the power cord supplied with the unit.

2.4 INITIAL CHECKOUT PROCEDURE

A detailed description of the operator controls and indicators is contained in Section III. The procedure to be followed during initial checkout of the transport is given in Paragraph 2.4.1.

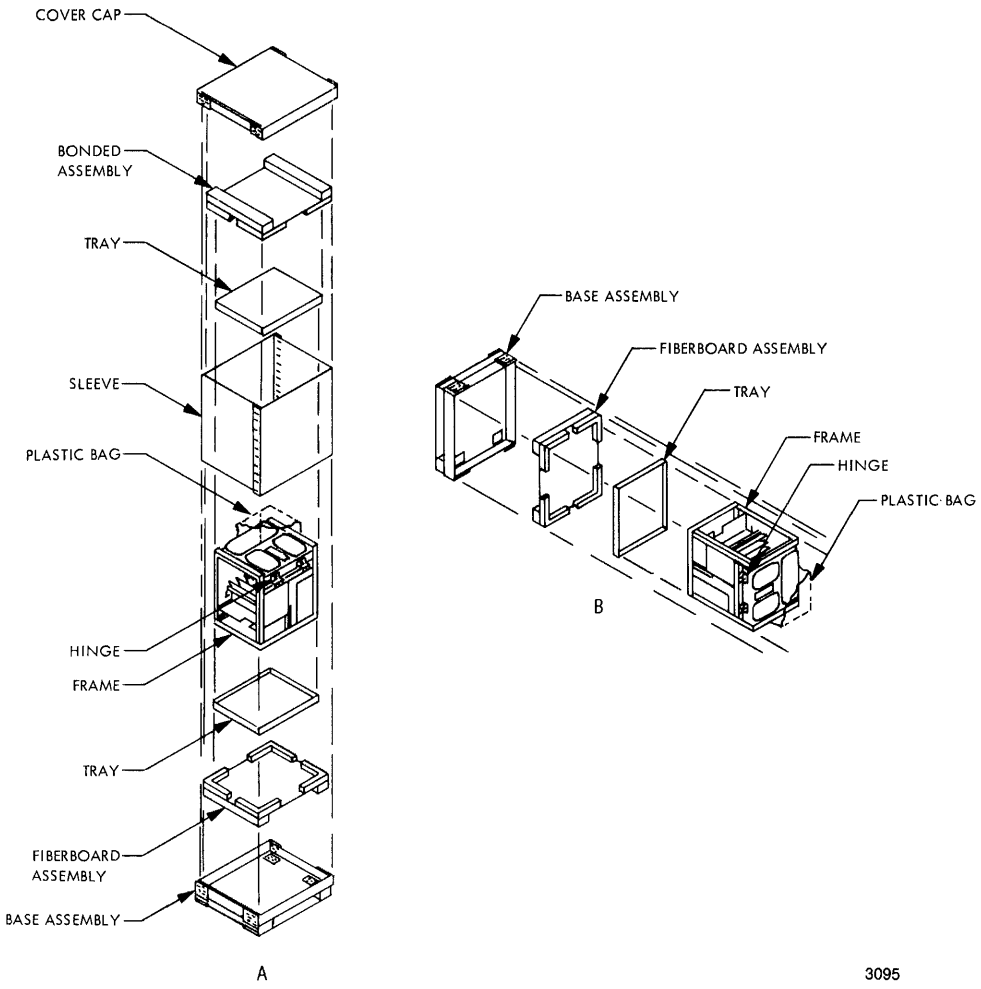

Figure 2-1. Uncrating the Transport

Table 2-1
Power Cord Color Code

Black or Brown AC 'Hot' (Live)	**Nero o Marrone** (Vivo)	**Noir ou Brun** (haut Voltage)	**Negro o Moreno** (Vivo)	**Schwarz oder Braun** (Heiss)
White or Blue AC Return (Neutral) (Common)	**Bianco o Blue** AC Ritorno (Neutro) (Comune)	**Blanc ou Blue** AC Retour (Neutre) (Commun)	**Blanco o Azul** AC Neutro (Neutro) (Comun)	**Weiss oder Blau** AC Zuruck (Neutral) (Gemeinsamer)
Green or Green with Yellow Stripes Chassis (Ground)	**Verde o Verde con le Righe Gialle** Telaio (Terra o massa)	**Vert ou Vert avec Rayure Jaune** Chassis (Terre)	**Verde o Verde con Rayas Amarillas** Chasis (Tierra)	**Grun oder Grun mit Gelben Streifen** Chassis (Grund)

The turnon and checkout procedure is given in Figure 2-2 in chart form. It can be seen that the chart is divided into four sections, as follows.

(1) Column Headings — Lists the audio and visual indications.

(2) Sequential Checkout — Lists step-by-step instructions for checkout of the transport.

(3) Matrix — Gives the results of the Sequential Checkout with respect to time.

(4) Reference — Lists the function affected and the alignment and maintenance paragraphs that pertain to each *checkout.*

2.4.1 VISUAL INSPECTION

Prior to applying power to the transport, the following visual inspection must be performed.

(1) Check the primary power connections located at the rear of the power chassis; refer to Table 2-2.

(2) Open the supply and takeup reel doors on the transport to access the buffer box door.

(3) Open the buffer box door, and with a screwdriver, release the door latch. Open the transport door.

(4) Check that all hose and plug connections, screws and mounting hardware are secure.

(5) Visually check all fuses.

(6) Ensure that the Maintenance Switch on the Control M/M2 PCBA is set to the center position, that the Maintenance Switch on the Reel Servo PCBA is set toward the front of the transport, AGC Exerciser Switch on the Read PCBA is in center position, and Test Write Switch on the MIA is in the right-hand position.

(7) Check jumper connections (located on the vertical Interconnect D/D1 PCBA) and terminating resistor packs (located on the Read, Control M/M2, and Write PCBAs) as follows.

(a) If only one transport is involved and the interface is to use the transports' logic voltage level, W1 must be installed. If the host system voltage level is to be used, W1 must be removed and W2 must be installed. In some configurations, W2 is replaced by a hardwire connection.

(b) If more than one transport is to be daisy-chained between the respective (J201, J202, J203, and J204) connectors of the transports, W1 must be removed from all transports except the master (first, or most closely connected to the host controller). W1 must be removed from the master also if the system is to be operated at the host system voltage level.

(c) Terminating resistor packs are required only in the last transport of the chain.

CAUTION

JUMPER CONNECTIONS MUST COMPLY WITH (7) TO AVOID POSSIBLE DAMAGE TO THE EQUIPMENT.

(8) Close the Base Assembly.

(9) Open all front panel doors and visually check the tape path; refer to Figure 3-2. Ensure that the tape path is clean and contains no obstructions.

(10) Close the buffer box and takeup reel door.

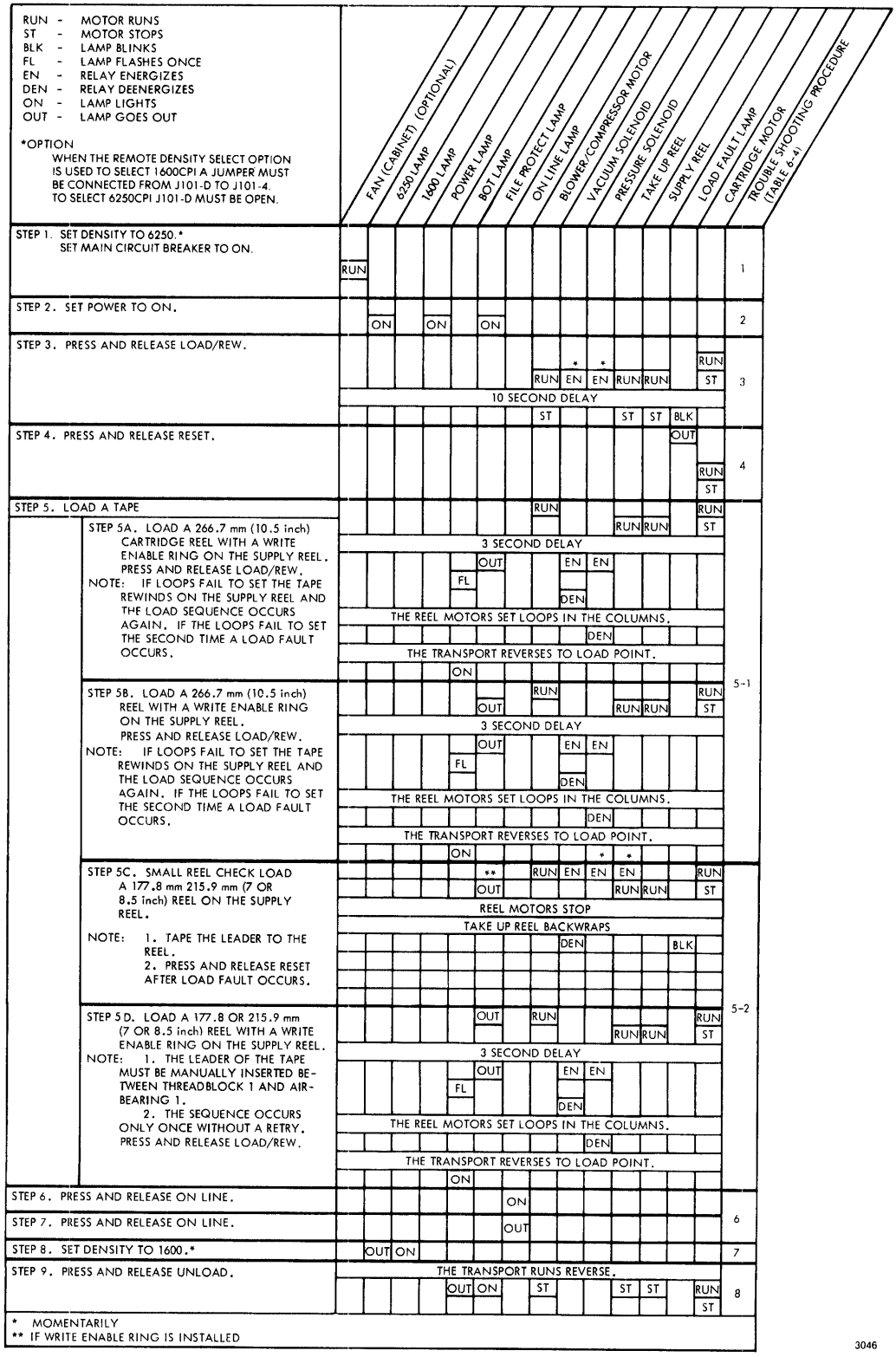

Figure 2-2. Turnon and Checkout Procedure

Table 2-2
Primary Power Connections

Input	Wht/Blk Wire	Wht/Red Wires (2)
220V	TB1-4	TB1-8
230V	TB1-3	TB1-8
240V	TB1-4	TB1-9
250V	TB1-3	TB1-9

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(11) Connect the power plug to the appropriate ac outlet.

CAUTION

DO NOT OPERATE TRANSPORTS EQUIPPED WITH A HIGH-ALTITUDE BELT/PULLEY KIT AT ALTITUDES BELOW 1220 m (4,000 FEET). THIS WILL OVERLOAD THE AC MOTOR.

2.4.2 CHECKOUT

After completing the visual inspection given in Paragraph 2.4.1, perform the checkout procedures given in Figure 2-2.

2.5 RACK-MOUNTING THE TRANSPORT

WARNING

THE RACK IN WHICH THE TRANSPORT IS TO BE INSTALLED MUST BE SUFFICIENTLY WEIGHTED OR ANCHORED TO SAFELY ACCOMMODATE THE HIGH CENTER OF GRAVITY.

The T1000 transport is designed to be mounted in a standard 19-inch EIA rack; 622.3 mm (24.5 inches) of panel space is required. The depth behind the mounting surface must be a minimum of 584.2 mm (23 inches) and a maximum of 736.6 mm (29 inches).

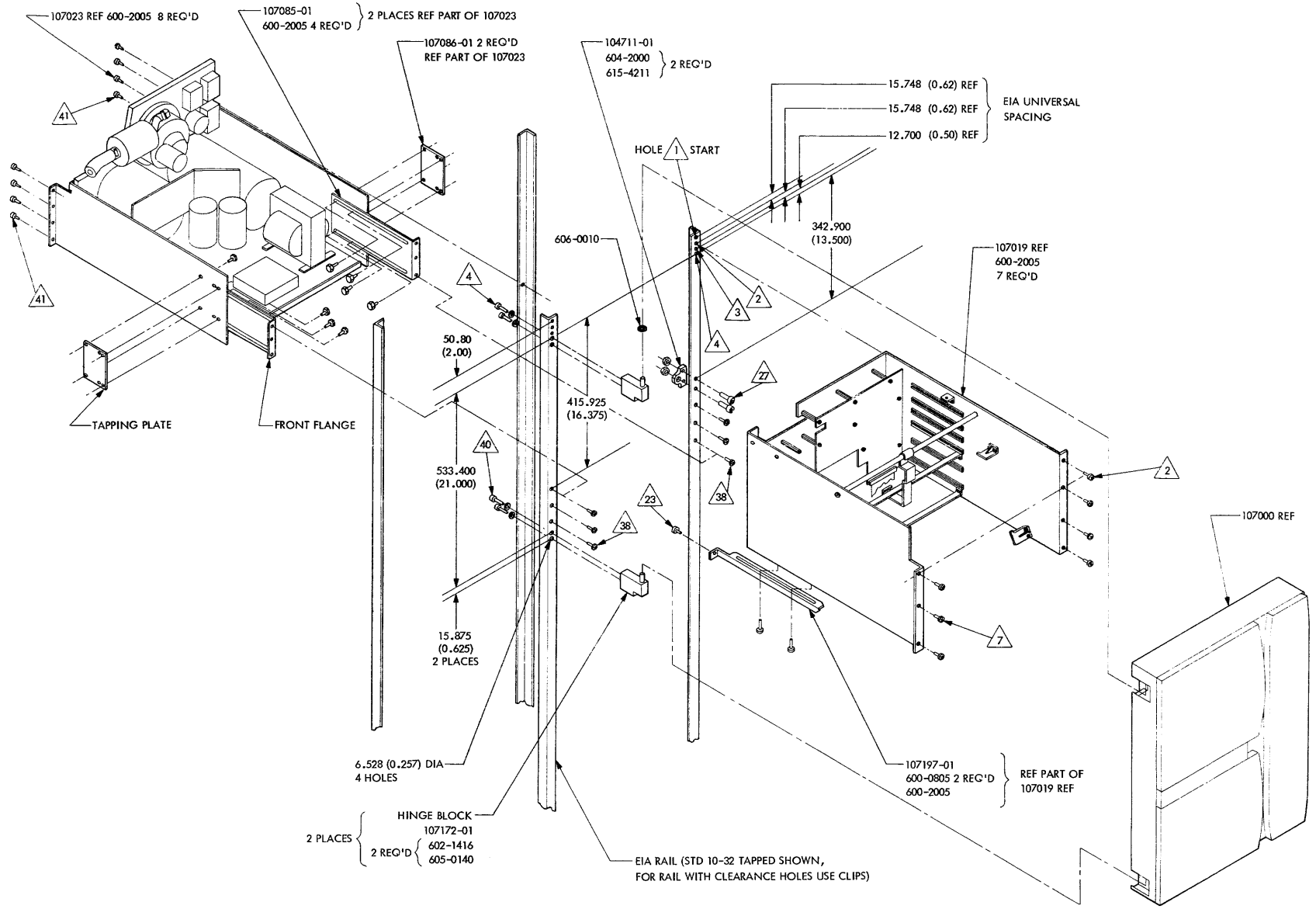
NOTE

A 0.257-inch drill bit and the following readily-available material are required for this procedure: (a) 1 piece of lumber, 50x100x305 mm (2x4x12 inches); (b) 1 piece of plywood, 6.350x152x915 mm (¼x6x36 inches); (c) 1 piece of tape, 50.8x305 mm (1x12 inches) with adhesive on 2 sides.

Rack mounting requires two people; one to prepare the rack and one to prepare the transport. The two are then required to work as a team to remove the transport from its shipping frame and install the transport in the rack. Figure 2-3 should be referred to in conjunction with the following procedures. Figure 2-4 gives the critical dimensions of the transport.

NOTE

The following steps refer to certain holes in standard cabinet rails. If EIA hole placement cannot be confirmed, locate the holes by measurements specified in Figure 2-4.



NOTE: A. ALL DIMENSIONS ARE mm (inches)

B. THE NUMBER ENCLOSED IN THE △ SYMBOL INDICATES THE EIA MTG HOLE NUMBERS FROM TOP TO BOTTOM. THE NUMBERS DESIGNATE THE UNIVERSAL EIA HOLE SPACING ONLY. FOR ALTERNATE SPACING, DIMENSIONS SHOWN MUST BE USED.

Figure 2-3. Rack Mounting the Transport

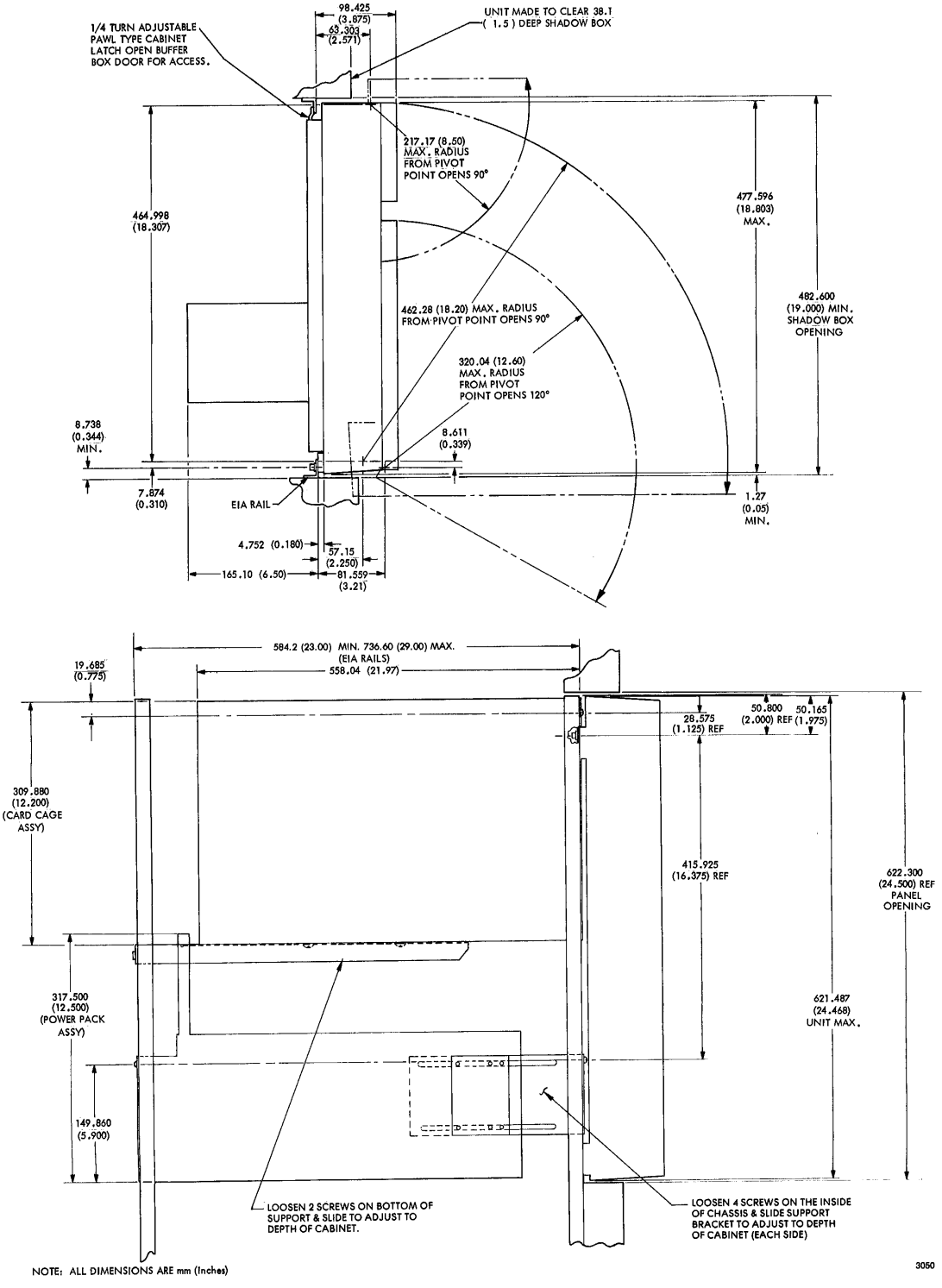


Figure 2-4. Outline Dimensions

(1) On the left vertical mounting bracket facing the EIA cabinet, count and mark the mounting holes as follows. From the top, mark holes 4, 5, 7, 32, 35, 38, 40, 41, 43, and 44. On the right vertical mounting bracket facing the EIA cabinet, count and mark the mounting holes as follows. From the top, mark holes 2, 27, 29, 32, 35, 38, 43, and 44.

(2) Count and mark the mounting holes on the back of the EIA cabinet. The holes to be marked are: from the top, mark both sides at holes 41, 43, 44, and on the right rear side, hole 23.

(3) On the front left side, drill out holes 4, 5, 40, and 41 to 6.528 mm (0.257 inch) diameter.

(4) From the Installation Kit (Pertec Part No. 107017-01), remove hinge blocks, four 1/4-20 socket head cap screws and four 1/4 spring lock washers.

(5) Install hinge blocks as shown in Figure 2-3 at holes 4 and 5, and at holes 40 and 41.

(6) Remove the flat washer from the Installation Kit and place it over the top hinge block pin.

(7) Remove the leveling block, the two 10-32 button head screws, and the two No. 10 nuts with washers attached from the Installation Kit.

(8) On the right side, install the leveling block as shown in Figure 2-3 at holes 27 and 29.

NOTE

The Power Pack Mounting Kit referred to in the following steps is available as an option.

(9) Open the Power Pack Mounting Kit (Pertec Part No. 107282-01), and remove the two 3/4-inch diameter supports and four 10-32 X 5/8-inch screws and 10-32 nuts. (Refer to Figure 2-5).

(10) Install the two 3/4-inch diameter supports on both sides of the front of the rack at holes 43 and 44.

(11) From the Power Pack Mounting Kit, remove the two 1-inch diameter supports and four 10-32 X 5/8-inch screws.

(12) Install the two 1-inch diameter supports on both sides of the back of the rack at holes 43 and 44.

(13) From the Power Pack Mounting Kit, remove one large diameter tube and one small diameter tube.

(14) Insert the small diameter tube into the large diameter tube.

NOTE

Be sure the two small holes in the ends of the tube are showing.

(15) Install the tubes in the support holes (see Step 12).

(16) From the Power Pack Mounting Kit, remove four cotter pins and install them on each side of the supports.

(17) Repeat Steps (13) through (16) for the other side of the rack.

(18) On the transport shipping frame, remove the shipping hinge on the right side.

(19) Open supply and takeup reel doors on the transport to access the buffer box door.

(20) Open the buffer box door, and with a screwdriver, release the door latch (located below the supply reel loop air column). Open the transport door.

(21) Close the buffer box door and the supply and takeup reel doors.

(22) On the Card Cage Assembly, remove the ribbon cable plugs from the Read PCBA, the Write PCBA, and the Control M/M2 PCBA.

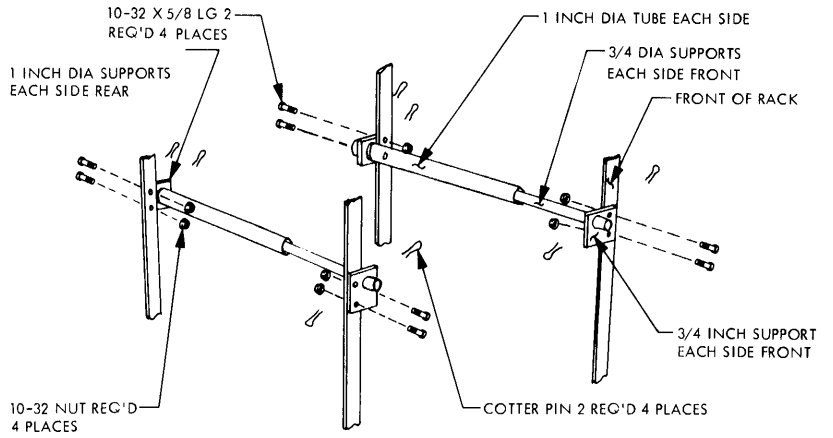


Figure 2-5. Power Pack Mounting Kit (Optional)

(23) On the back of the Base Assembly, remove the ribbon cable plug from the Interconnect F/F1 PCBA.

NOTE

Before disconnecting any wires, cables, air lines, etc., check to see that they are identified in a way that will facilitate correct reinstallation.

(24) On the back of the Base Assembly, remove the 1/2-inch diameter clear plastic hose from the pressure valve.

(25) On the back of the Base Assembly, remove the 1-3/4-inch diameter hose from the vacuum valve.

(26) On the Reel Servo PCBA, ascertain that cables to J14 through J20 are identified; then disconnect the cables.

(27) Cut the tiewraps on the side and bottom of the Card Cage and the wraps to free the white and gray twisted wire pair from the Controls Assembly to the solid state switch on the Power Pack Chassis. Mark the contacts on the switch where the white wire and gray wire were removed.

(28) On the back of the Card Cage, remove the red wire (TB1-2) and the orange wire (TB1-3) and cut the tiewraps to free the wires.

(29) Slide all wires and cables away from the shipping frame. Ensure the Base Assembly is not connected to the other subassemblies.

(30) Open the supply and takeup reel doors and remove the seven Phillips head screws holding the trim assembly. Close both doors and remove the trim assembly.

WARNING

BASE ASSEMBLY IS HEAVY, EXERCISE CARE WHEN LIFTING.

(31) Place a 50x100x305 mm (2x4x12 inch) block of wood under the Base Assembly. With a person steadying the Base Assembly, remove the two hinges from the left side of the shipping frame; rest the Base Assembly on the block of wood.

(32) Lift the Base Assembly from the shipping frame and lean it against a stable vertical member; e.g., a wall.

(33) Remove the block of wood and slide a 6.350x152x915 mm (1/4x6x36 inch) plywood between the Power Pack Chassis and the shipping frame (long axis).

(34) On the Power Pack Chassis, remove the 1-3/4-inch diameter hose from between the blower and the Card Cage.

(35) On the Card Cage, remove the quick-disconnect wires from TB1. Mark the wires with the terminal numbers.

(36) Ensure that the Air Filter and Muffler are free from the shipping frame.

(37) Remove the eight screws holding the Power Pack Chassis to the shipping frame. Allow the Power Pack Chassis to rest on the plywood.

(38) Remove the four hex head screws from each of the front flanges. The tapping plates (Figure 2-3) will fall off.

(39) With double-sided adhesive tape, mount the tapping plates to the outside of the Power Pack Chassis. Ensure the clearance holes in the wraparound and the tapping plates are aligned.

WARNING

ONE PERSON SHOULD NOT ATTEMPT TO LIFT THE TRANSPORT POWER PACK CHASSIS.

(40) Slide and lift the Power Pack Chassis out of the rear of the shipping frame and install it on the Power Pack Mounting Kit brackets.

(41) With the Power Pack Chassis resting on the mounting brackets, attach the front flanges to the wraparound using the hex head screws. Do not tighten at this time.

(42) Slide the Power Pack Chassis in the rack until the rear flanges touch the back of the rack.

(43) With a large screwdriver, lift one rear corner of the Power Pack Chassis until the bottom hole in the rear flange lines up with hole 41 on the rack.

(44) Insert a 10-32 screw in hole 41 and hand tighten.

(45) With a large screwdriver, lift the other rear corner of the Power Pack Chassis until the bottom in the rear flange lines up with hole 41 on the rack.

(46) Insert a 10-32 screw in hole 41 and hand tighten.

(47) Using a large screwdriver, shift one side of the Power Pack Chassis until the other three 10-32 screws can be inserted. Hand tighten.

(48) Using a large screwdriver, shift the other side of the Power Pack Chassis until the other three 10-32 screws can be inserted. Hand tighten.

(49) Slide one front flange in until it is flush with the front of the rack.

(50) Using a large screwdriver, lift one corner of the Power Pack Chassis until the bottom hole of the front flange lines up with hole 38 of the rack.

(51) Insert a 10-32 screw in hole 38 and hand tighten.

(52) With a large screwdriver, lift the other corner until the bottom hole of the front flange lines up with hole 38 of the rack.

(53) Insert a 10-32 screw in hole 38 and hand tighten.

(54) Using a large screwdriver, shift one side of the Power Pack Chassis until the other two 10-32 screws can be inserted. Hand tighten.

(55) Using a large screwdriver, lift the other corner of the Power Pack Chassis until the other two 10-32 screws can be inserted. Hand tighten.

(56) Tighten the front flange screws to the rack.

(57) Tighten the rear flange screws to the rack.

(58) Tighten the front flanges to the wraparound.

(59) While holding the Card Cage, loosen and remove the screws holding the Card Cage to the shipping frame.

(60) On the bottom of the Card Cage, remove the rear bracket.

(61) Install the Card Cage from the front of the rack, the right side should be flush with the top. Insert the top 10-32 screw.

(62) On the left side of the rack, adjust the Card Cage so the top hole lines up with hole 7. Insert a 10-32 screw.

(63) Shifting the Card Cage, insert the other five 10-32 screws. Tighten the front screws.

(64) On the right rear, install the rear bracket at hole 23 using one 10-32 screw.

(65) Attach the bracket to the bottom of the Card Cage.

(66) Tighten the bracket to the rack.

(67) Tighten the bracket to the bottom of the Card Cage.

(68) Remove the Power Pack Mounting Kit and save for future use.

(69) Allow the Muffler and Air Filter to hang and, using two tiewraps, attach them to the EIA rails.

(70) Connect the 1-3/4-inch diameter hose to the Card Cage from the blower.

(71) Route the cable to the Card Cage and connect the wires to TB1. Be careful to connect properly.

(72) With two persons, lift the Base Assembly and hang it on the hinge blocks.

(73) Connect the 1/2-inch diameter clear plastic hose to the pressure valve on the Base Assembly (Step 24).

(74) On the Base Assembly, connect the 1-3/4-inch diameter hose to the vacuum valve (Step 25).

(75) Connect the white and gray wires from the Control Assembly to the solid state switch on the Power Pack Chassis (Step 27).

(76) Connect the red and orange wires from the Capstan Motor to the Card Cage TB1 (Step 28).

(77) Connect J13 through J20 to the Reel Servo PCBA (Step 26).

CAUTION

PROPER CONNECTION OF CABLES TO JACKS J13 THROUGH J20 IS IMPORTANT. IF IDENTIFICATION OF CABLES IS IN DOUBT, CHECK FIGURE 2-6.

(78) Connect ribbon cables to Control M/M2, Write, Read, and Interconnect F/F1 PCBAs.

(79) Connect the braided ground strap between the base assembly and the Card Cage back shell hole marked E. This is near the hole used when the transport is installed in the shipping frame.

(80) Remove the tiewraps from the Installation Kit and fasten the cable bundles.

(81) Install the trim.

(82) Perform the checkout procedure detailed in Paragraph 2.4.

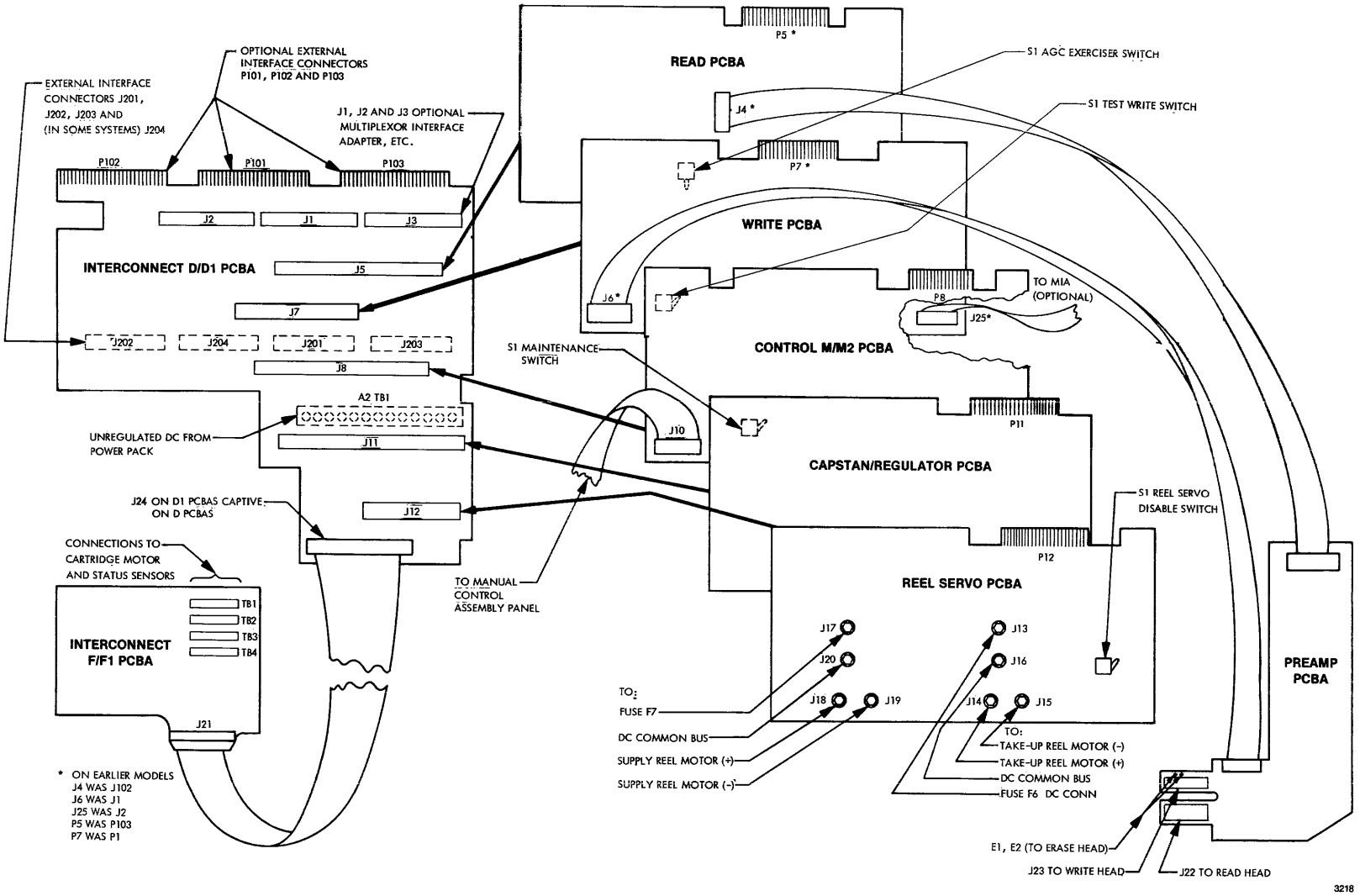


Figure 2-6. Interface Provisions and Card Cage Interconnections

2.6 INTERFACE SPECIFICATIONS AND INFORMATION

The following paragraphs contain a summary of the physical and electrical interface specifications for the T1940 tape transport. Three methods of interfacing are provided:

(1) Basic interface (J201, J202, J203, and J204).

(2) Internal Multiplexer Interface Adapter (MIA).

(3) Edge connectors J101, J102 and J103.

Interfacing and interconnecting provisions are illustrated in Figure 2-6.

2.6.1 INTERFACE CABLES

The interconnection cables between Pertec and Customer equipment must be Pertec-approved flat ribbon cables (3M Part No. 3365) or a harness of individual twisted pairs with the following characteristics.

(1) Maximum length: 12.2m (40 feet).

(2) Characteristic impedance: 110 to 150 ohms.

(3) 22 or 24 gauge conductors with an insulation thickness of 0.25 mm (0.01 inch) minimum.

NOTE

For MIA interfacing cables, refer to the MIA Addendum.

It is important that signal lines are capacitively shielded, i.e., arrange the lines in the cable ground-signal-ground. Three methods of interfacing connections are given, in order of preference. Refer to Figure 2-6, Interconnect D/D1, in conjunction with the following paragraphs.

2.6.2 BASIC INTERFACE (J201, J202, J203, J204)

The basic interface configuration uses four 3M Header connectors to interface a single transport to a controller/formatter. These connectors are 3M Part No. 3414 or 3431 (Pertec Part No. 503-3414 or 3431, depending on configuration) and are available upon request. Each connector must be wired by the customer. J201, J202, J203, and J204 are on the rear side of Interconnect D/D1 PCBA. Details relating to the interface signals are contained in Section III. These connectors are on the rear side of Interconnect D/D1 PCBA.

To daisy-chain up to four transports, J201, J202, J203, and J204 are used. A special cable assembly, Pertec Part No. 103936-05 through -08, is available to connect the controller/formatter and the transports in a daisy chain configuration.

2.6.3 MULTIPLE INTERFACE ADAPTER (MIA) PCBA

The optional Multiplexer Interface Adapter (MIA) may be plugged into J1, J2, and J3, on the front side of Interconnect D/D1 PCBA. This assembly is designed to interface with the host system or a Pertec F6250 formatter via two cables. This interface features time-multiplexed signals and bi-directional use of conductors. Driver/receiver requirements are shown in the MIA Addendum.

Daisy-chain connections are possible to an additional four transports via J201, J202, J203, and J204, using 3M-3431-2002 connectors.

2.6.4 EDGE CONNECTOR (J101, J102, J103)

Three printed circuit edge connectors are required to interface a single transport via J101, J102, and J103, or the first transport in a daisy-chain to a controller/formatter by means of the top edge connectors on the Interconnect D/D1 PCBA. These are ELCO connectors, Part No. 00-6007-036-980-002 (Pertec Part No. 503-0036) and are available upon request. Each connector must be wired by the customer. Details relating to the interface signals are contained in Section III of this manual.

To daisy-chain up to four transports, J201, J202, and J203 are used. Cable Assembly, Pertec Part No. 103936-01 through -04, is used to connect the transports in a daisy-chain configuration. Refer to Paragraph 2.6.5 for daisy-chain information.

2.6.5 DAISY-CHAIN REQUIREMENTS

To daisy-chain T1000 transports, the line terminators must be removed from the Control M, Read, and the Write PCBAs in all transports except the last transport in the daisy chain. Refer to Table 2-3. The terminators are on DIP sockets for easy removal and installation.

Jumper W1, located between interface connectors J201 and J204 on the Interconnect D/D1 PCBA, must be removed from all transports except the master (first in the daisy chain). It must also be removed from the master if the transports are to operate on the host system voltage at the interface. Refer to Table 2-3 for appropriate use of jumpers W1 and W2.

CAUTION

TO AVOID CIRCUIT DAMAGE IN MULTI-TRANSPORT DAISY-CHAINED SYSTEMS, W1 MUST BE REMOVED FROM ALL TRANSPORTS EXCEPT THE MASTER.

Levels: True = Low = 0 to +0.4v (approximately)
False = High = +3v (approximately)

Pulses: Levels as above; minimum pulsewidth is 1 microsecond. Edge transmission delay over 6.096m (20 feet) of cable is not greater than 200 nsec.

The interface circuits are designed so any disconnected wire results in a false signal.

Figure 2-7 shows the configuration for which the transmitters and receivers have been designed. The nominal +5 volts at the terminating resistors is referred to as +5v (T), which is equal to the level of the internal logic referred to as nominal +5v (L), or to the host system's interface voltage, referred to as nominal +5v (I). Refer to Table 2-3. For daisy-chain cable requirements, refer to Paragraph 2.6.2, 2.6.3, or 2.6.4, as appropriate.

Table 2-3
W1, W2, and Terminator Requirements

SYSTEM CONFIGURATION						TAPE UNIT REQUIREMENTS								
						Master Unit (Connected to host)			Each Intermediate Unit (If any)			Terminal Unit (End of daisy chain)		
No. of Tape Units	Terminator Power Source	Tape Unit Interface Connectors	MIA or Microformatter Used	Daisy Chain Connector		W1	W2	TERM. PKS	W1	W2	TERM. PKS	W1	W2	TERM. PKS
1	TUL	Any	Yes/No	N/A	→	Use	Omit	Use	N/A	N/A	N/A	N/A	N/A	N/A
1	HOST	J201-J204	No	N/A	→	Omit	Use	Use	N/A	N/A	N/A	N/A	N/A	N/A
2,3,4	TUL	Any	Yes/No	J201-J204	→	Use	Use	Omit	Omit	Omit	Omit	Omit	Use	Use
2,3,4	HOST	J201-J204	No	J201-J204	→	Omit	Use	Omit	Omit	Omit	Omit	Omit	Use	Use

NOTES:

W1, W2 — Jumpers located on Interconnect D/D1 PCBA.

TERM. PKS — Terminator resistor packs:
Tape Control M PCBA — U161, U162
Read PCBA — U6
Write PCBA — U161, U218

TUL — Tape transport unit logic power.

HOST — Host system interface power.

ANY — Interconnections with host system may be made via Interconnect D/D1 PCBA connectors J201-J204, P101-P103, Microformatter P4-P5 or MIA connectors J2 and J3. Daisy-chain connections between tape units may be via Interconnect D/D1 PCBA connectors J201-J204 only.

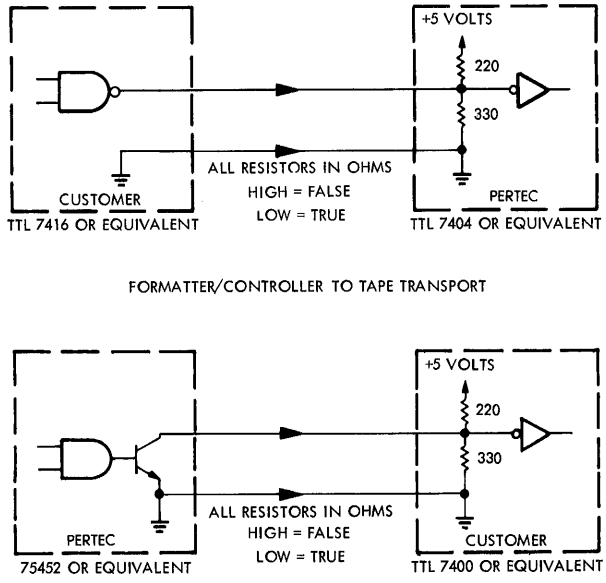


Figure 2-7. Driver/Receiver Requirements for Parallel Interface Configuration

SECTION III
OPERATION

3.1 INTRODUCTION

This section provides specific and unique information pertaining to operating the transport. Procedures for manual control, automatic and manual tape loading, maintenance operation, and interfacing are explained.

3.2 PRELOADING INFORMATION

The following general information applies to procedures followed before loading tape into the transport.

(1) Check the heads, tape guides and buffer boxes for dirt, dust, etc. Clean if necessary. (Refer to Section VI for cleaning procedures.)

(2) If the task requires recording data on the tape, install a write enable ring on the supply reel.

(3) If the tape to be run is on a small reel, such as a 216 mm (8.5-inch) reel, or if it is on a 267 mm (10.5-inch) reel but without sufficient tape, the automatic loading feature is not applicable. The minimum quantity of tape for efficient automatic loading is such that the outer turn of tape must be between 15.875 and 6.35 mm (0.625 and 0.250-inch) from the outer edge of the reel, as shown in Figure 3-1. Manual loading procedure for large reels is similar to that for small reels. (Refer to Paragraph 3.3.2.)

(4) To ensure proper automatic loading, the end of the tape must be trimmed with a tape crimper (IBM Part No. 2512063).

3.3 LOADING TAPE IN THE TRANSPORT

In all of the following tape-loading procedures, the takeup (lower) reel is assumed to be in place and empty. The supply reel, containing the tape on which reading or writing is to be performed, will be positioned in such a way that the tape will unwind if the reel is turned clockwise.

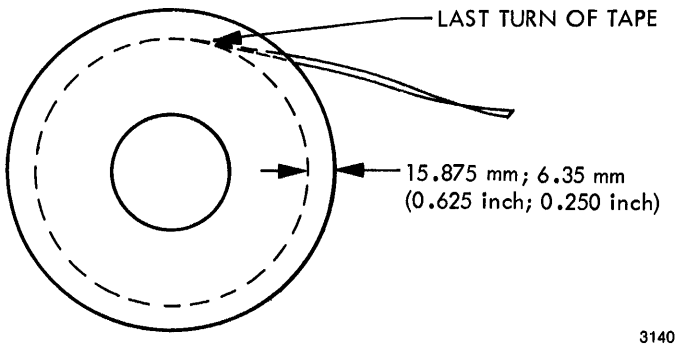


Figure 3-1. Minimum Tape Limit for Automatic Loading

3.3.1 LOADING 267 mm (10.5-INCH) REEL OR CARTRIDGE

(1) Turn POWER switch ON or, if ON, momentarily press the RESET switch.

NOTE

The transport is designed to handle IBM Easy Load #1 and Easy Load #2 wraparound cartridges.*

(2) Place the supply reel on the upper hub, rotate the reel to align the cartridge key so it will slip easily into place, and press the reel-retaining actuator. It is not necessary to remove or open an acceptable cartridge.

(3) Close all doors.

(4) Momentarily press the LOAD/REW switch.

The cartridge, if any, will automatically open, the reel will turn backward (counter-clockwise) a few turns, then turn forward (clockwise) and eject the tape into the tape path. Figure 3-2 illustrates the tape routing. After a few turns have been captured by the takeup reel, the reel turns backward, providing slack in the tape, and the extra tape is drawn into the buffer boxes and tape pocket by the Air system.

If the tape fails to load the first time, the supply reel backwinds all of the tape and tries to load a second time. If the tape fails to load on the second attempt, the LOAD FAULT indicator blinks.

To attempt another load sequence, RESET must be pressed and released before pressing LOAD/REW again.

NOTE

Some units are equipped with a backwrap defeat *door switch. When a 267 mm (10.5-inch) open reel is installed, and the supply reel door is open, the reel will not backwrap and it must be loaded in the same manner as in Paragraph 3.3.2. If the backwrap is to be reinstated, the operator must pull on the switch plunger. Reels mounted in an Easy Load* cartridge always backwrap, whether the supply reel door is open or closed.*

3.3.2 LOADING 178- OR 216-mm (7- OR 8.5-INCH) REELS

After the reel has been loaded on the supply reel:

(1) Manually place the tape leader between Thread Block #1 and Air Bearing #1; refer to Figure 3-2.

NOTE

Ensure that there is no tape slack or sag between the supply reel and Thread Block #1.

(2) Close all doors.

(3) Set POWER control to ON.

(4) Press and release LOAD/REW.

The operation is the same as Paragraph 3.3.1 except there is no automatic retry if tape fails to load. If the tape fails to load, the LOAD FAULT indicator blinks. To attempt another load sequence, RESET must be pressed and released before repeating Steps 1 through 4.

*Easy Load #1 and #2 are Registered Trademarks of IBM.

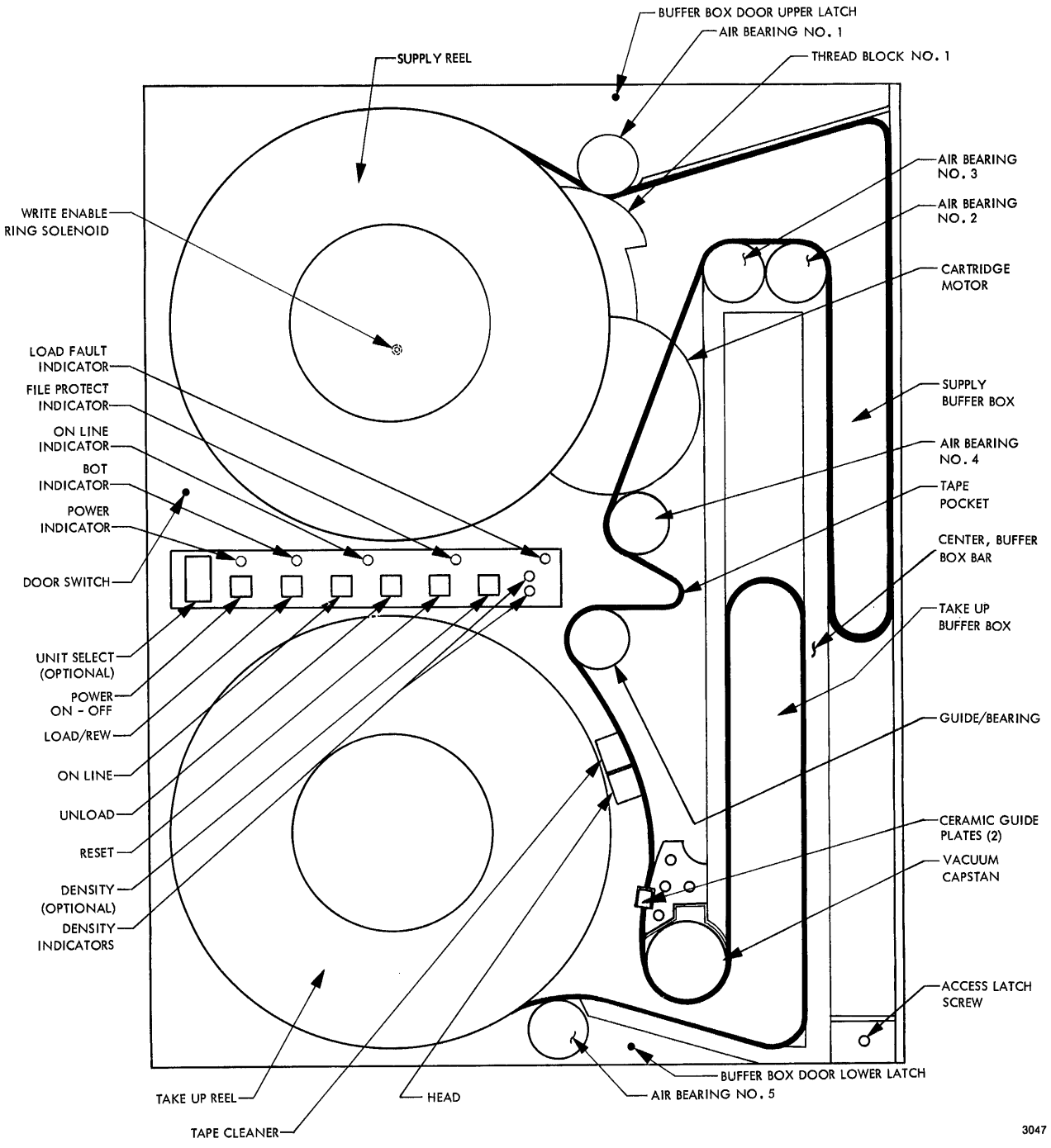


Figure 3-2. Tape Path and Controls

3.3.3 MID-REEL LOADING

A Mid-Reel Load is usually required after a power failure or a lost interlock.

(1) Press and release ON LINE. The transport will go off line.

(2) Manually rewind the tape to remove slack.

CAUTION

DO NOT ATTEMPT MID-REEL LOAD UNTIL ALL SLACK IS REMOVED FROM THE TAPE BETWEEN THE REELS.

(3) Press and release RESET.

(4) Press and release LOAD/REW.

The transport loads tape and starts a reverse operation to BOT. To stop the transport, press and release RESET. Any other commands may now be given. If a LOAD FAULT occurs, press and release RESET before attempting another load sequence.

3.3.4 UNLOADING TAPE

(1) Press and release ON LINE; this causes the transport to go Off-line.

(2) Press and release UNLOAD; tape will be backwound onto the supply reel.

3.4 CONTROLS AND INDICATORS

The operational controls and indicators located on the control panel of the transport (refer to Figure 3-2), as well as the maintenance switches described in Table 3-1, are functionally described in the succeeding paragraphs.

3.4.1 FRONT PANEL CONTROLS AND INDICATORS

The front panel controls and indicators allow the operator to control and monitor the transport operation.

3.4.1.1 POWER ON/OFF

The POWER ON/OFF control is an alternate action switch that connects the power supply to the remaining circuits. When power is turned on, all power supplies are established and a reset signal is applied to the logic. Illumination of the POWER LED indicates the presence of secondary ac and dc power.

Table 3-1

Maintenance Switches

Switch	Location	Non-activated Position
Control Maintenance Switch (S1)	Control M/M2 PCBA	Center
Reel Servo Disable (S1)	Reel Servo PCBA	*Forward
AGC Exerciser (S1)	Read PCBA	Center

NOTES:

1. During normal operation, the maintenance switches must be in the non-activated position.
2. *Toward front of cabinet.
3. Refer to Multiplexer Interface Adapter for information on switches located on that board.

3.4.1.2 LOAD/REW

The LOAD/REW control is a momentary switch. The three separate functions performed by this switch are described as follows.

CAUTION

DO NOT ATTEMPT MID-REEL LOAD, UNLOAD OR RE-WIND UNTIL ALL UNTENSIONED SLACK IS MANUALLY REMOVED FROM THE TAPE BETWEEN THE REELS.

(1) AUTOLOAD — Pressing and releasing the LOAD/REW switch initiates the Autoload sequence. The Autoload sequence automatically loads a 267 mm (10.5-inch) reel or cartridge to BOT. One retry is attempted, if the Autoload sequence is not completed on the second try, a LOAD FAULT occurs. The transport must be RESET after a LOAD FAULT indication. There is no automatic retry on 178 or 216 mm (7- or 8.5-inch) reels.

NOTE

Some units are equipped with a switch that defeats backwrap if the door is open, unless an Easy Load cartridge is installed.*

(2) REWIND — Pressing and releasing the LOAD/REW switch, with tape tensioned and the transport Off-line causes the tape to rewind to BOT. When the switch is pressed and released with the tape at BOT, no action occurs.

(3) MID-REEL LOAD — Pressing and releasing the LOAD/REW switch, with tape in path but not tensioned causes the tape to load and run in the reverse direction to BOT unless the RESET switch is pressed.

3.4.1.3 ON LINE

The ON LINE control is a momentary switch that is enabled after an initial Load or Rewind sequence has been completed. Pressing and releasing the switch changes the transport to an On-line mode and causes the indicator to become illuminated. In this condition the transport can accept external commands provided it is also Selected and Ready.

The transport will revert to the Off-line mode if any of the following occur.

(1) ON LINE is pressed a second time.

(2) An external REWIND UNLOAD command (IRWU) is received.

(3) Vacuum column interlock is broken.

(4) AC power is lost.

(5) RESET is commanded.

3.4.1.4 UNLOAD

The UNLOAD control is a momentary switch. Pressing and releasing the switch with the system Off-line and the tape at BOT causes tape to unload. When pressed and released in mid-reel and Off-line, tape will rewind and unload.

3.4.1.5 RESET

The RESET control is a momentary switch. Pressing and releasing the switch terminates all functions except operations controlled by the maintenance switch on the Control M/M2 PCBA. The control also clears a Load Fault indication.

*Easy Load #1 and #2 are Registered Trademarks of IBM.

3.4.1.6 DENSITY

The DENSITY control is a rocker-type switch. The control selects either 246 c/mm (6250 cpi) or 63 c/mm (1600 cpi) modes. The 6250 LED is illuminated when the GCR mode is selected and the 1600 LED is illuminated when the PE mode is selected.

3.4.1.7 UNIT SELECT (0—3)

The Unit Select is a 4-position rotary switch. The control sets the address of the transport as specified within the host system.

3.4.1.8 FILE PROTECT

The FILE PROTECT LED, when illuminated, indicates when a reel of tape without a write enable ring is installed on the transport.

3.4.1.9 LOAD FAULT

The LOAD FAULT LED blinks when a Load Fault is detected.

3.4.1.10 BOT

The BOT LED lights to indicate that the tape is at the beginning-of-tape position.

3.4.2 MAINTENANCE CONTROLS

In addition to the front panel controls and indicators, certain maintenance controls are also provided. These controls are located on the PCBAs in the Card Cage Assembly.

3.4.2.1 Forward/Reverse Maintenance Switch

The forward/reverse Maintenance switch is a 3-position toggle switch located on the Control M/M2 PCBA. (Refer to Figure 6-5.) This switch provides manual control of tape motion when the transport is Off-line.

When the switch is set toward the front, tape moves in the forward direction; when set in the center position, tape motion stops; when set toward the rear, tape moves in the reverse direction.

3.4.2.2 TP30

Test Point TP30 is located on the Control M/M2 PCBA. This test point may be used in conjunction with the Maintenance switch. When TP30 is grounded, tape starts and stops at a 10 Hz rate in the direction selected. This test point is used to adjust ramp timing, as instructed in Section VI.

3.4.2.3 TP31

Test Point TP31 is located on the Control M/M2 PCBA. When TP31 is grounded and the Maintenance switch is in its center position, tape shuttles at an 0.5 Hz rate. This test point is used to adjust loop travel, as instructed in Section VI.

3.4.2.4 DISABLE REEL SERVO (RS)

The Disable RS control is a 2-position toggle switch located on the Reel Servo PCBA.This control provides for manual operation of the reels. When the control is set toward the rear, the reel servos are disabled.

3.4.2.5 AGC Exerciser Switch

The AGC exerciser switch on the Read PCBA provides for testing the automatic gain control circuits. The switch must be in center position during normal operation.

3.4.2.6 Multiplexer Interface Adapter (MIA) Controls and Indicators

In configurations using the Multiplexer Interface Adapter (MIA), refer to the Addendum provided for these configurations.

3.4.2.7 Write/Control/Status (WCS) Miniature Switches

In configurations using the Multiplexer Interface Adapter (MIA), the WCS miniature switches mounted on that assembly must be set as required by the host system. Refer to the Addendum provided for these configurations.

3.5 INTERFACE SIGNALS — CONTROLLER TO TRANSPORT

All waveform names are chosen to correspond to the logical true condition. Drivers and receivers belong to the TTL family where the true level is 0v and the false level is between +3v and +5v. Interface signals are described in the following paragraphs and are summarized in Table 3-2.

NOTE

The following paragraphs pertain to interface inputs to the Interconnect D/D1 PCBA. If the Multiplexer Interface Adapter (MIA) is used, interfacing is as specified in the Addendum provided for MIA configurations.

3.5.1 SELECT 0 (ISLT0)

ISLT0 is a level which, when low, enables all the interface drivers and receivers in the transport, thus connecting the transport to the controller. (For multi-transport systems, refer to Paragraph 3.5.2.)

3.5.2 SELECT 1,2,3 (ISLT1, ISLT2, ISLT3)

SELECT lines 1 through 3 can be used in conjunction with ISLT0 in multiple transport configurations. This signal is a level which, when low and the Select switch setting corresponds, enables all the interface drivers and receivers in the transport, thus connecting the selected transport to the controller.

It is assumed that all of the interface inputs discussed in the following paragraphs are gated with SELECT.

3.5.3 SYNCHRONOUS FORWARD COMMAND (ISFC)

ISFC is a level which, when low and the transport is selected, ready, and on line (see Paragraph 3.6.1), causes tape to move forward at the specified velocity. When the level goes high, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times.

3.5.4 SYNCHRONOUS REVERSE COMMAND (ISRC)

ISRC is a level which, when low and the transport is selected, ready, and on line (see Paragraph 3.6.1), causes tape to move in the reverse direction at the specified velocity. When the level goes high, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times. An SRC will be terminated upon encountering the BOT tab, or ignored if given when tape is at Load Point.

3.5.5 DATA DENSITY SELECT (IDDS)

IDDS is a level which, when low, conditions the Read electronics to operate in the 63 c/mm (1600 cpi) density mode. In addition, the DATA DENSITY line (IDDI) to the controller/formatter will go low and the 1600 indicator will become illuminated. Conversely, when IDDS is high, the Read electronics will operate in the 246 c/mm (6250 cpi) density mode, the 800 indicator will become illuminated, and IDDI will go high.

Table 3-2
Interface Signals

At Interconnect D/D1 PCBA									
Connector	Signal Pin	Gnd	Signal	Connector	Signal Pin	Gnd	Connector	Signal Pin	Gnd
J201	9	27	SELECT 0 (ISLT0)	J101	J	8	J1	9	26
	14	32	SYNCHRONOUS FORWARD Command (ISFC)		C	3		14	32
	12	30	SYNCHRONOUS REVERSE Command (ISRC)		E	5		12	30
	13	31	DATA DENSITY SELECT (IDDS) (optional)		D	4		13	31
	10	28	REWIND Command (IRWC)		H	7		10	28
	7	25	REWIND & UNLOAD (IRWU)		L	10		7	25
	8	26	SET WRITE STATUS (ISWS)		K	9		8	26
	19	20	READY (IRDY)		T	16		19	20
	6	24	ON-LINE (IONL)		M	11		6	24
	5	23	REWINDING (IRWD)		N	12		5	23
	2	34	END OF TAPE (IEOT)		U	17		2	34
	3	21	LOAD POINT (ILDP)		R	14		3	21
	4	22	FILE PROTECT (IFPT)		P	13		4	22
	11	29	DATA DENSITY INDICATOR (IDDI)		F	6		11	29
	—	—	+5V at 100 mA		S	—		—	—
	—	—	SELECT 1 (ISLT1)		A	—		—	—
	—	—	SELECT 2 (ISLT2)		18	—		—	—
	—	—	SELECT 3 (ISLT3)		V	—		—	—
	18	—	+5V (I)		—	—		—	—
J202	33	3	SELECT 1 (ISLT1)	J102	B	2	J2	33	—
	31	5	SELECT 2 (ISLT2)		D	4		31	—
	28	8	SELECT 3 (ISLT3)		H	7		28	—
	34	2	WRITE DATA STROBE (IWDS)		A	1		34	2
	32	4	WRITE AMPLIFIER RESET (IWARS)		C	3		32	4
	29	7	READ LOW THRESHOLD (IRTH2)		F	6		29	7
	25	11	WRITE DATA PARITY (IWDP)		L	10		25	11
	24	12	WRITE DATA 0 (IWD0)		M	11		24	12
	23	13	WRITE DATA 1 (IWD1)		N	12		23	13
	22	14	WRITE DATA 2 (IWD2)		P	13		22	14
	21	15	WRITE DATA 3 (IWD3)		R	14		21	15
	20	16	WRITE DATA 4 (IWD4)		S	15		20	16
	19	17	WRITE DATA 5 (IWD5)		T	16		19	17
	18	—	WRITE DATA 6 (IWD6)		U	17		18	—
	1	9	WRITE DATA 7 (IWD7)		V	18		1	—
	26	10	TACHOMETER (ITACH)		K	9		26	9
J203	33	3	READ DATA STROBE (IRDS)	J103	2	B	J3	33	3
	34	2	READ DATA PARITY (IRDP)		1	A		34	2
	32	4	READ DATA 0 (IRD0)		3	C		32	4
	31	5	READ DATA 1 (IRD1)		4	D		31	5
	27	7	READ DATA 2 (IRD2)		8	J		27	7
	26	8	READ DATA 3 (IRD3)		9	K		26	8
	21	15	READ DATA 4 (IRD4)		14	R		21	15
	20	16	READ DATA 5 (IRD5)		15	S		20	16
	18	—	READ DATA 6 (IRD6)		17	U		18	—
	1	—	READ DATA 7 (IRD7)		18	V		1	—
	25	9	NPE (IPE)		10	L		25	9
	24	10	7 TRACK (I7TR)*		11	M		24	10
	22	14	SPEED (ISPEED)*		13	P		22	14
	23	6	SINGLE (ISGL)*		12	N		23	6
J204	1	—	+5V (T)						
	18	—	+5V (T)						
	25	8	IAMTIEP —/A1						
	26	9	IAMTIE0 DCHP/A2						
	27	10	IAMTIE1 DCH0/A3						
	28	11	IAMTIE2 DCH1/A4						
	29	12	IAMTIE3 DCH2/A5						
	30	13	DCH3/NARA						
	31	14	IAMTIE4 DCH4/A6						
	32	15	IAMTIE5 DCH5/A7						
	33	16	IAMTIE6 DCH6/A8						
	34	17	IAMTIE7 DCH7/A9						
	20	3	SPARE						

NOTES:

1. For Multiplexer Interface Adapter interfacing refer to the MIA Addendum.
2. Connectors
   J201—J204 Connector: PCB Header Connector 3M 3431-2002
   Mating Connector: 3M 3414
   J101—J103 Connector: 36 Pin Etched PC Edge Connector
   Mating Connector: 36 Pin ELCO 00-6007-036-980-002
3. *Signal not used.

Table 3-2 (Continued)
Interface Signals

At Write PCBA J1 (J25)		
Connector	Pin	Signal
J1 (J25)	1	IAMTIE7
	2	IAMTIE5
	3	IAMTIE4
	4	—
	5	ILTH (NLTH, Low Threshold)
	6	—
	7	—
	8	—
	9	IWRT BIN (Write Binary)
	10	—
	11	IARA ERR
	12	IAMTIE3
	13	IAMTIE6
	14	IWRT STAT H (Write Status)
	15	ISTDTH H (Standard Threshold)
	16	IMOTION H (Tape in Motion)
	17	IAMTIEP
	18	IAMTIE0
	19	IAMTIE1
	20	IAMTIE2

NOTES:
1. Connectors
   J1 (J25) Connector: PCB Header Connector 3M 3428-2002
   Mating Connector: 3M 3421
2. AMTIE: Amplitude of track is in error.

3.5.6 REWIND COMMAND (IRWC)

IRWC is a pulse (minimum width of 1 μsec) which, if the transport is selected, ready and on line, causes tape to move in the reverse direction, moving at rewind speed unless a low tape (LT) condition has been sensed, in which case movement is at reverse speed until it comes to rest at BOT. An IRWC is ignored if tape is already at BOT.

3.5.7 SET WRITE STATUS (ISWS)

ISWS is a level that must be low for a minimum period of 20 μsec after the front edge of an ISFC when the Write mode of operation is required. The front edge of the delayed ISFC is used to sample the ISWS signal and sets the Write/Read flip-flop in the transport to the Write state.

If the Read mode of operation is required, the ISWS signal must be high for a minimum period of 20 μsec after the front edge of an ISFC (or ISRC), in which case the Write/Read flip-flop will be set to the Read state.

3.5.8 WRITE DATA LINES (IWDP, IWD0—IWD7)

These are levels which, when low at Write Data Strobe (IWDS) time (when the transport is in the Write mode), result in a flux reversal being recorded on the corresponding tape track. These lines must be held steady during the IWDS and for 0.5 μsec before and after the IWDS pulse.

3.5.9 WRITE DATA STROBE (IWDS)

3.5.9.1 PE Mode

In PE mode, IWDS is a pulse (1 μsec minimum) for each character to be recorded. The frequency of the IWDS is equal to twice the character transfer rate. The IWDP, IWD0—IWD7 levels must be steady during and for 0.5 μsec before and after the IWDS. The trailing edge of IWDS is used to copy the Phase Encoded waveform into the transport.

3.5.9.2 GCR Mode

In GCR mode, IWDS is a pulse (1 μsec minimum) for each character to be recorded. The frequency of the IWDS is equal to the character transfer rate. IWDP, IWD0—IWD7 levels must be steady during and for 0.5 μsec before and after the IWDS. The trailing edge of IWDS is used to toggle the write register whenever a one is written.

3.5.10 READ THRESHOLD 2 (IRTH2)

IRTH2 sets the read-only mode thresholds at 1.0 ± 0.1v (false) and 0.1 ± 0.1v (true). IRTH2 level must be held low while low-amplitude data recovery is required. Normal thresholds and read-after-write mode thresholds are 2.5 ± 0.2v for GCR and 3.0 ± 0.3v for PE.

3.5.11 WRITE AMPLIFIER RESET (IWARS)

In T1940-96 Tape Transports, the IWARS interface is not used. The write amplifiers are reset by the RESET 1 signal, which is generated by the MOTION signal input to the Write PCBA.

3.5.12 REWIND AND UNLOAD (IRWU)

IRWU is a pulse (1 μsec minimum) which resets the On-line flip-flop and initiates a rewind operation. Upon completion of the rewind, an unload sequence is automatically executed.

3.5.13 + 5V POWER

This line is used to supply + 5.0v to the interface.

3.6 INTERFACE SIGNALS — TRANSPORT TO CONTROLLER

It is assumed that all interface outputs discussed in the following paragraphs are gated with SELECT (refer to Paragraphs 3.5.1 and 3.5.2).

NOTE

The following paragraphs pertain to interface outputs from the Interconnect D/D1 PCBA. If the Multiplexer Interface Adapter (MIA) is used, interfacing is as specified in the Addendum provided for MIA configurations.

3.6.1 READY (IRDY)

IRDY is a level that is low when the transport is ready to accept any external command, i.e., when:

(1) Tape is under tension in the vacuum column.
(2) A LOAD or REWIND command has been completed.
(3) There is no UNLOAD command in progress.
(4) The transport is On-line.

3.6.2 READ DATA (IRDP, IRD0—IRD7)

3.6.2.1 PE Mode

In the PE mode, Read Data signals on these 9 lines are the outputs of the 9 peak detectors individually gated with the outputs of an envelope detector associated with each channel. These signals are replicas of the PE waveforms used to drive the write amplifiers.

3.6.2.2 GCR Mode

In the GCR mode, each character bit is deskewed in the data output register that drives the read data lines, IRDP, IRD0—IRD7. These data lines, when gated with MOTION, are strobed into the tape controller on the trailing edge of the READ DATA STROBE (IRDS).

3.6.3 ON-LINE (IONL)

IONL is a level that is low when the On-line flip-flop is set. When low, the transport is under remote control; when high, the transport is under local control.

3.6.4 LOAD POINT (ILDP)

ILDP is a level that is low when the transport is ready and on line and tape is at rest with the BOT tab under the photosensor. The signal goes high after the tab leaves the photosensor area.

3.6.5 END OF TAPE (IEOT)

IEOT is a level which, when low and the transport is ready and on line, indicates that the EOT reflective tab is positioned under the photosensor.

3.6.6 REWINDING (IRWD)

IRWD is a level that is low when the transport is engaged in any rewind operation.

3.6.7 FILE PROTECT (IFPT)

IFPT is a level that is low when tape is loaded and under tension in the vacuum column and the supply reel has the write enable ring removed.

3.6.8 DATA DENSITY INDICATOR (IDDI)

IDDI is a level that is low when the PE density mode is selected.

3.6.9 DATA DENSITY SELECT (IDDS)

IDDS is a level that is low when the transport is conditioned to read PE. When high, the transport is conditioned to read GCR.

3.6.10 7 TRACK (I7TR)

I7TR level is high (false) for all T1940-96 units.

3.6.11 TACHOMETER (ITACH)

ITACH is a pulse (1 μsec) that is triggered by the positive and negative transitions of the capstan optical tachometer. The tape movement between alternate pulses is 0.254 mm (0.01 inch).

3.6.12 AMPLITUDE TRACK IN ERROR (AMTIE) SIGNALS

An AMTIE signal is generated for each of the nine tracks on the basis of the amplitude of the data as received from the GCR/PE Preamp 1 PCBA. An unsatisfactory channel output causes the Write PCBA AMTIE circuits to issue a low = true IAMTIE signal to the interface and a low = true NAMTIE signal to the MIA circuits via Write PCBA connector J25.

3.6.13 LATE AGC

The high = true LATE AGC signal is generated on the Read PCBA and sent to the MIA if any of the channel ALL SET signals are not present when the AGC period times out. It is effective in either Read or Write mode.

3.6.14 AUTOMATIC READ AMPLIFIER ERROR SIGNAL (NARA) (IARA ERRL)

The low = true NARA signal is generated on the Read PCBA and sent through the Write PCBA to the MIA or other interface via cable as IARA ERRL. It is effective in Write mode only and notifies the system that the automatic read amplifier burst expected at the transport for recording has failed to record properly within the allotted time.

3.6.15 LOW THRESHOLD STATUS (NLTH)

The low = true NLTH signal is sent to the MIA or the interface via cable from the Write PCBA and indicates that the transport is reading in low threshold mode.

3.6.16 STANDARD THRESHOLD (STDTH)

The high = true STDTH signal is routed similarly to the NLTH via cable from the Write PCBA and indicates normal threshold read mode.

3.6.17 WRITE STATUS (WRT STAT)

Write status is indicated by a high = true WRT STAT signal to the interface or MIA via cable from the Write PCBA.

3.6.18 TAPE MOTION (MOTION)

The MOTION high = true signal via cable from the Write PCBA to the interface or MIA indicates that the tape transport is in motion.

3.6.19 WRITE BINARY (WRT BIN)

WRT BIN indicates that the tape transport is writing binary data. It is routed from the Write PCBA to the MIA or other interface via cable.

3.7 WRITE AND READ WAVEFORMS

Figures 3-3 and 3-4 show typical PE and GCR Write and Read waveforms, respectively. The external controller, Formatter (F6250), or Multiplexer Interface Adapter supplies all command waveforms.

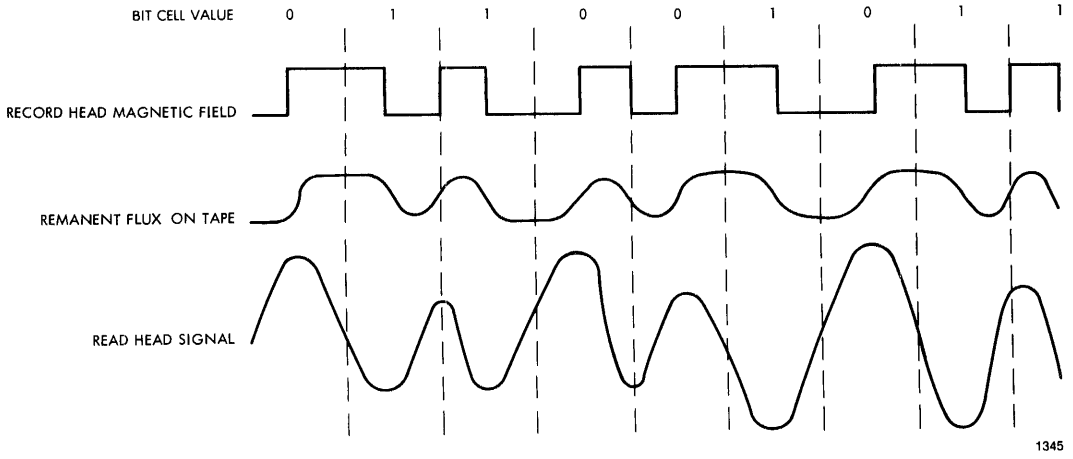


Figure 3-3. PE Write and Read Waveforms

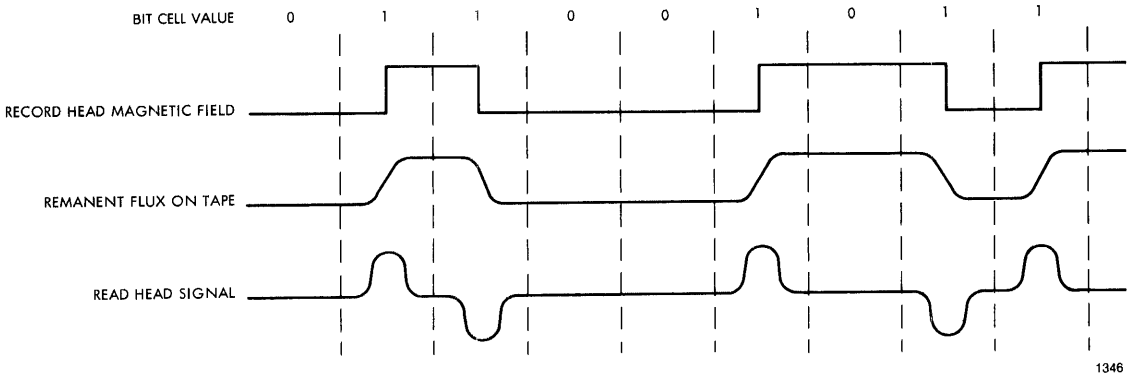


Figure 3-4. GCR Write and Read Waveforms

SECTION IV
GENERAL THEORY OF OPERATION

4.1 INTRODUCTION

4.1.1 PRIME FUNCTIONS AND MODES

The Model T1940-96 Dual-Format Read-After-Write Tape Transport provides accessible storage of information in binary form. It accepts control signals and data from a controller, either directly or through a formatter. Selectable modes of operation provide for writing and/or reading in either GCR or PE format.

The T1940-96 Tape Transport basic configuration uses an optional Multiplexer Interface Adapter (MIA) and operates in conjunction with a separate F6250 Formatter. The MIA is plugged into J1, J2, and J3 of Interconnect D/D1 PCBA. Some of the traffic between the F6250 Formatter and the MIA is via bidirectional lines that are used at different times for different purposes. The main purpose of the MIA is to demultiplex inputs and multiplex outputs to make the Transport and Formatter circuits compatible.

If the F6250 Formatter is not used, the host system must interface with the MIA as specified in the Addendum. If the MIA is not used, the host system must provide the same interfacing with the Transport as would be provided by the MIA.

The T1940-96 Transport handles GCR or PE data much as similar T1000 Transports would handle NRZI or PE data. The GCR magnetic recording code, like NRZI, uses a flux reversal in either direction within a cell time to record a true or a 1, and no flux reversal to record a false or 0. PE recording uses a transition toward the erase direction of magnetization to record a true or a 1, and a transition in the opposite direction to record a false or a 0. A meaningful transition occurs in the middle of a bit cell. When two 1s or two 0s occur in succession, a nonsignificant transition occurs at the beginning edge of the second bit cell time in order to prepare for a second meaningful transition in the same direction as the first.

The rapid transfer, high density, and extreme reliability of GCR storage requires pre-input processing as provided by the F6250 Formatter and the MIA. This processing is essentially as follows:

(1) Seven consecutive characters (bytes) of write data are isolated and an error check and correction (ECC) character is added. This forms a *data group*:

D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E

(2) An odd parity bit is added to each character, and the data group is divided into two *data subgroups*:

D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E
D D D D D D D E
P P P P P P P P

(3) The data subgroups are then translated, according to a table stored in the Formatter. This forms two *storage subgroups*:

S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S

Note that in the translation the parity and checking bits are not distinguishable from data bits.

(4) The two storage subgroups are then recombined to form a *storage group* of ten 9-bit characters:

S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S
S S S S S S S S S S

(5) The Formatter also generates preambles, tape marks and other necessary control bytes, assembles them with the data, and sends the signals (with associated commands) to the MIA. The final tape format is detailed in Paragraph 4.5.12.

(6) The MIA distributes the signals through the Transport's Interconnect D/D1 PCBA to the circuits that process and record the data and control bytes on tape.

For information on MIA circuits refer to the Addendum. For information on F6250 Formatter circuits, refer to the F6250 Formatter Operating and Service manual. Systems which do not use the F6250 Formatter or the MIA must provide for processing the data, as summarized above, and interfacing with the Transport (via J201 through J204) in such a way as to provide the Transport with data in the same format as would be provided by the MIA. This interfacing is defined in Table 3-2 and discussed in the following paragraphs.

4.1.2 INPUT/OUTPUT (I/O) THEORY

Data and control inputs and outputs travel over parallel lines between the transport and controller or formatter. (Time multiplexed systems are discussed in the Multiplexer Interface Adapter (MIA) Addendum.) In the basic system, the interconnections are made by

means of four cables that can be plugged into J201, J202, J203, and J204 attached to the rear side of the vertically mounted Interconnect D or D1 PCBA (Figure 2-6). If more than one T1940 Transport is used in the system, the interconnect cables may be continued from the first transport to the corresponding receptacles (J201—J204) of the next transport, etc., in a daisy-chain arrangement. Terminating resistors are required in the transport that is connected to the end of the daisy-chain or in any transport that is used alone in a system. Multiple transport systems connected radially from the controller require terminating resistors in each transport.

Optional interconnections for various input/output formats may be made at the top edge connectors (J101, J102, J103) of the vertical Interconnect D/D1 PCBA, or through connectors on the Multiplexer Interface Adapter. The MIA is designed to be plugged into J1, J2, J3 on the front side of the Interconnect D/D1 PCBA. Refer to the Addendum for MIA I/O details.

The basic interface provisions are detailed in Section II. In all cases, daisy-chain connections between transports are made by interconnecting the three basic interface connectors (J201, J202, J203). Properly formatted inputs and outputs should be available at these connectors and associated testpoints.

Logic input/output nominal voltage levels are:

Low (True) = 0v

High (False) = 3v

The terms *logic low* and *logic high* are avoided on the premise that a logical proposition, such as the proposition that a transport is ON LINE, can only be true or false, and its truth can be electronically coded as either a high or a low voltage level, bit, or pulse.

A true signal from the controller or formatter will be 0v (nominal) at the input to the transport's receiver circuits. Similarly, a true signal from the transport to the controller or formatter will be 0v (nominal) at the output of the transport's driver circuits. At interface, therefore, low = true, and a mnemonic term with a prefix I for interface is always interpreted as low = true, whether the interface signal is an input or output. When necessary for clarification, a mnemonic term includes an R, for receiver, or D, for driver.

At other points in a circuit, a signal may be low = false; for example, ISIGNAL applied to a NOR gate or inverter produces SIG, which is high = true. If SIG is similarly inverted it produces NSIG, which is low = true. As far as voltage levels are concerned, NSIG is the same as ISIG; ISIG is known to be low = true without the N because the I indicates an interface signal, which are standardized as low = true.

In some circuitry, the voltage level of a signal, when true, is indicated by an L (for low) or an H (for high). A data or numeric bit is true if the bit is a 1.

An interface signal that may appear to be irregular in regard to voltage level is the high/low density select signal (NPE). This is because the signal is essentially true in either high or low state, depending on whether GCR or PE is selected. To simplify understanding the logic, this is considered a PE select signal. It is true (PE mode is selected) when the voltage level is low. If the voltage level is high, the NPE signal is false and the system operates in GCR mode.

4.1.3 TERMINOLOGY

Standard symbology is used in all schematics, logic drawings, etc. Mnemonic terms are defined in the Glossary, Appendix A.

4.1.4 EXPLANATION OF ILLUSTRATIONS

The text is supported by applicable schematics, simplified detail diagrams, and other conventional illustrations. In addition, block diagrams for major functions are provided as follows.

(1) System Functions Integrated
(2) Power Supply and Distribution.
(3) System Controls
(4) Capstan Servo Subsystem
(5) Air Subsystem
(6) Reel Servo Subsystem
(7) Write Function
(8) Read Function

Functional block diagrams listed in items (2) through (8) each present one essential function, such as the Read function. The subject function of each diagram is covered completely, if required for clarity, from input signals to outputs, regardless of circuit location in the hardware. This distinguishes the functional block diagram from the schematic, which in most cases is confined to a single Printed Circuit Board Assembly (PCBA) or other hardware unit. The schematics provide greater detail and may be identified by hardware references on the functional block diagrams.

Symbols used in the functional block diagrams are illustrated in Figure 4-1. Parts of signal paths confined to hardware assemblies are placed within boundaries which indicate the subassembly level. Hardware of one level (such as a PCBA) is included within boundaries of the next higher level assembly (such as the Card Cage).

Block diagrams illustrate the purposes of the modules, cards, assemblies, or components involved in the operation of the overall function. The active components in each block are shown in the schematic. Interconnecting wires, plugs, jacks, terminal boards, controls, indicators, test points, and adjustments are shown or listed as required.

Signal lines are coded by means of special arrowheads and are identified by signal flags. Signal lines illustrate significance of the signal in the discussion by the weight of the line. Refer to Figure 4-1 for an explanation of the symbols used in this section.

Hardware reference designations are printed in the upper left corner of the area representing that hardware. Controls visible when the equipment is mounted and operating under normal conditions (dust covers, doors closed, etc.) are considered front panel controls. Front panel controls appear symbolically on the diagram or in a line art window in the function and hardware on which they are located.

Signals that are generated in a particular function, and are used in another function, are interfaced by terminating the signal in a shadow box area representing the other function that uses the signal. Since all functions are located in hardware, all pins of plugs and jacks the signal passes through are shown to provide an easy method of tracing signals from one functional block diagram to another. Signal flags (mnemonic terms) aid the user in more rapidly locating the desired signal. The mnemonic terms, and other abbreviations when appropriate, are defined in the glossary.

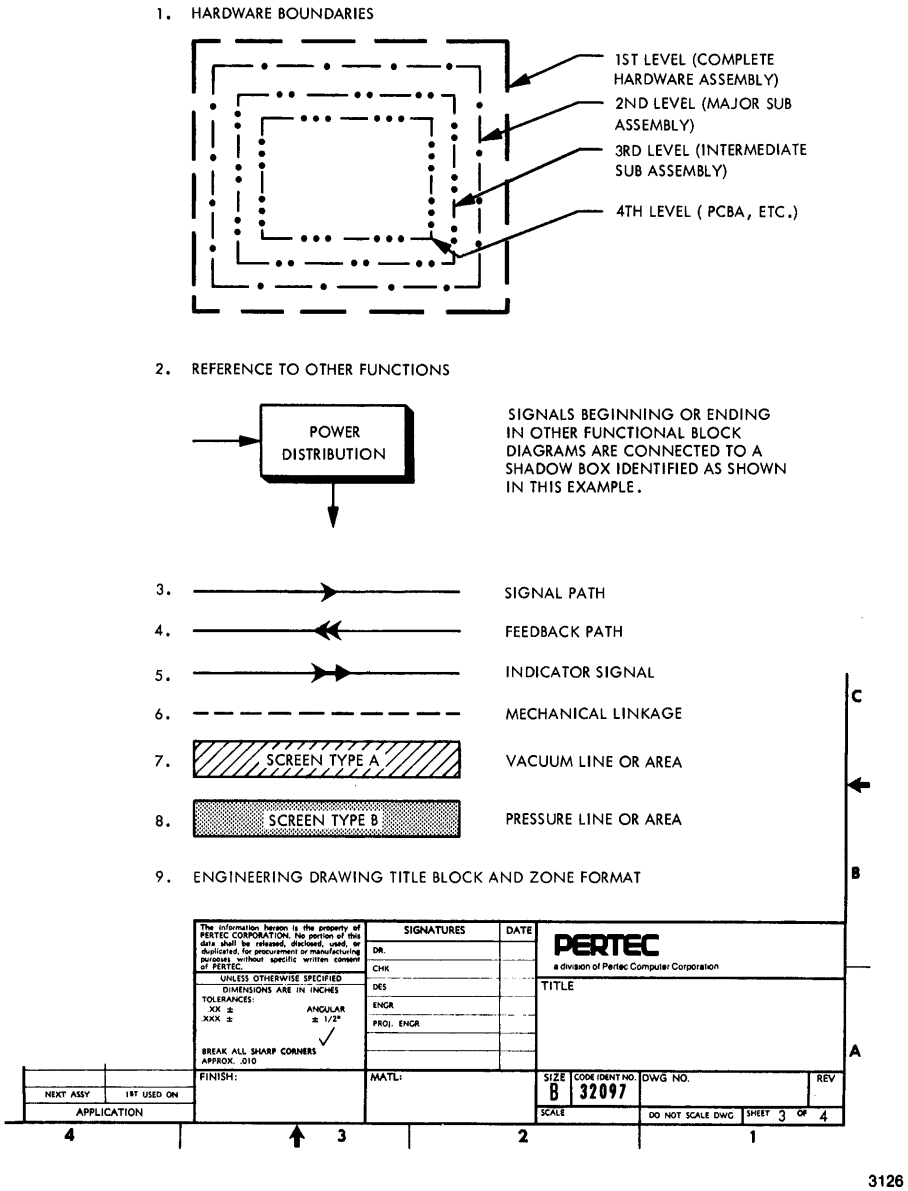


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Figure 4-1. Illustration Symbology

The text provides a description of the functional block's operation within the overall function. The text is written to establish how a particular portion of the function interplays with the other portions of the function. References to engineering drawings, schematics, etc., include document number and a zone code formed of the document sheet number, vertical coordinate number and horizontal coordinate letter.

4.2 GENERAL SYSTEM THEORY

The Dual-Format Read-After-Write Tape Transport provides for storage of digital data on reel-to-reel magnetic tape. In normal operation the transport is completely subject to the commands of an external computer or controller, which commands tape motion, provides data, determines when to read and write, etc. The transport provides status and informational outputs to the controller, and manual controls for preparing the transport, putting it on-line, testing, loading and unloading the tape, etc. External controls may be applied directly by the controlling equipment or through a formatter.

Figure 4-2 illustrates the basic transport functions with emphasis on the unique pneumatic tape-handling provisions, which make high-speed (125 ips) transport of tape from reel to reel practical.

The path followed by the tape in either direction between the supply reel and takeup reel produces two loops in the tape. Each loop is separately formed and maintained by positive (atmospheric) and negative (vacuum) pressure in cooperation with automatically controlled reel and capstan speeds.

The speed of tape motion past the reading and writing heads is determined by the capstan. The capstan motor drive power is controlled by a summing amplifier on the basis of basic commands and feedbacks, including the output of a tachometer mounted on the capstan motor shaft.

The speeds of the supply and takeup reels are separately controlled by servo circuits and maintain the proper tape tension by feedback control of the tape loop positions. Feedback is based on variations in the pressure differential between the buffer box areas separated by the tape loop.

Data are magnetically recorded on the tape as covered in Paragraph 4-1.

The read-after-write feature provides the transport interface with an echo of written data as read from the tape immediately after the writing process. This provides for checking by the controller (in parallel line interconnection systems) or by the MIA and formatter (in bidirectional line interconnection systems).

4.3 THEORY OF FUNCTIONAL SUBSYSTEMS

The functions of the T1940 Transport are shown in detail in Figure 4-3* and divided for discussion into the major categories listed in Paragraph 4.1.4.

Figure 4-3 illustrates the interrelationship between the transport functions and the interface connections to the host system.

Interface inputs and outputs are identified by connector and pin designations and by mnemonic terms for the signals. These terms are defined in the glossary.

Interface connections are grouped to show the available options: connectors J201, J202, J203, and J204 (most commonly used); external formatter connectors J101, J102, and J103; internal connectors J1, J2, and J3. If a formatter or MIA is used, interface with the host system will be via connectors on the optional assembly. These are covered in documentation for the MIA, and are not illustrated or discussed in this manual. (Refer to the Addendum.)

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*Foldout drawing, see end of section.

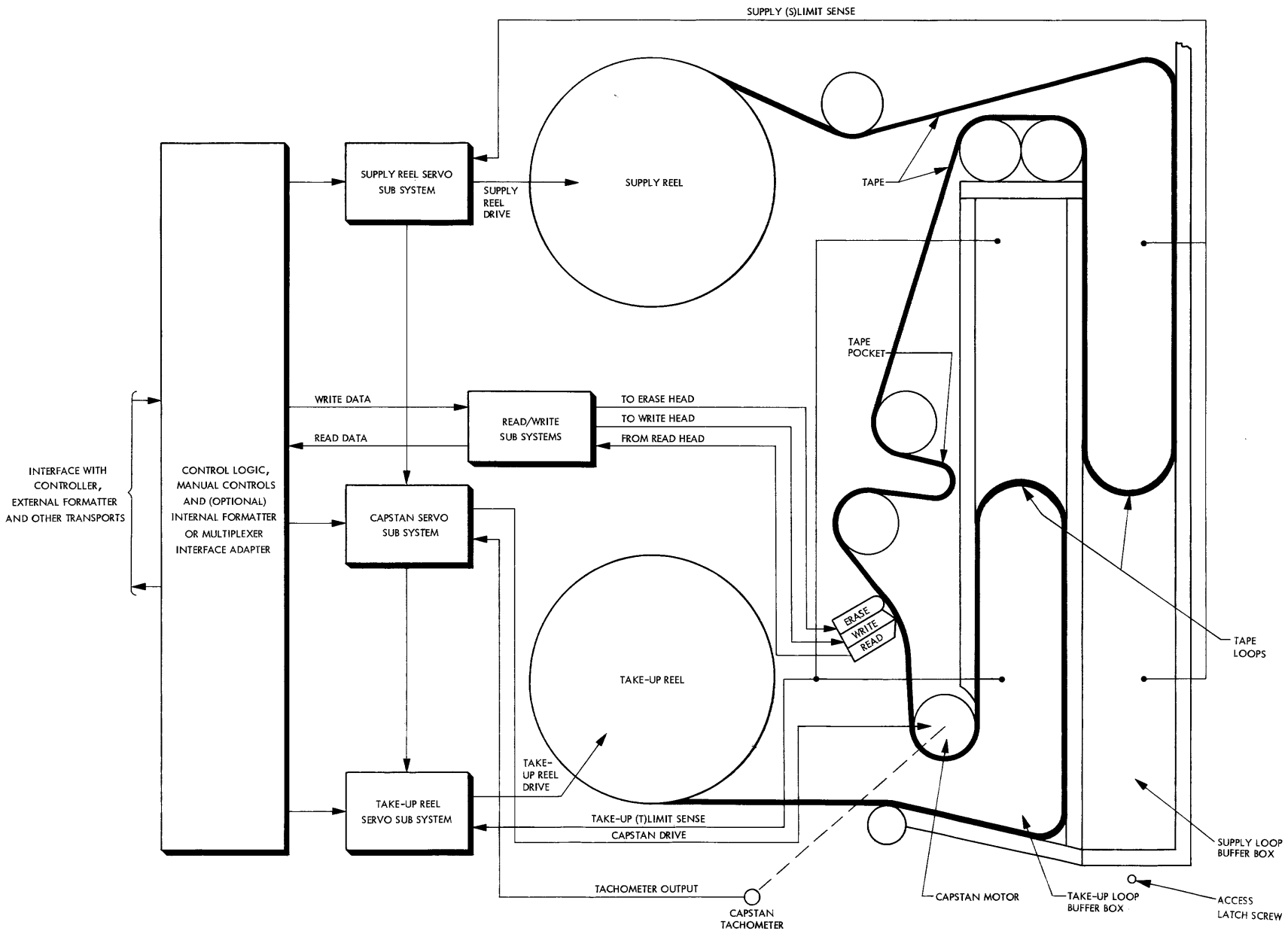


Figure 4-2. Simplified Theory Diagram

All interface connectors identified in Figure 4-3 are attached to a part of the vertically mounted Interconnect D/D1 PCBA. This PCBA provides the conductors that integrate the optional interfaces and the internal PCBAs. (Refer to Table 5-1 for Interconnect D/D1 PCBA conductor connections.)

Signal flow between the six internal functions is also shown. These functions (control, capstan, reel servo, write, read, and power distribution) are separately covered, so connectors are not identified in Figure 4-3.

4.4 POWER SUPPLY AND DISTRIBUTION

The transport derives all power from a single ac input as shown in simplified form in Figure 4-4. Primary ac power is used for the motor that drives the blower and compressor. A secondary winding output of transformer T1 provides 8.5v ac to the power reset (NPORST) circuits. Other secondary winding outputs are rectified and delivered to the Capstan/Regulator PCBA, where they are regulated. Reel servo unregulated ±36v dc power is supplied to the Reel Servo PCBA. Power used for the read, write and erase heads is regulated on the 9-Track Preamplifier PCBA.

WARNINGS

- ***DANGEROUS VOLTAGES ARE PRESENT.***
- ***ONLY QUALIFIED TECHNICIANS SHOULD HAVE ACCESS TO INTERNAL AREAS OF THE CABINET.***
- ***REFER TO FIGURES 5-2—5-5 FOR POWER DISTRIBUTION INFORMATION.***
- ***BEFORE WORKING IN POWER PACK ASSEMBLY AREA, DISCONNECT PRIMARY INPUT POWER AND WAIT FIVE MINUTES FOR CAPACITORS TO DISCHARGE.***

Details of the power circuits are presented in Section V of this manual.

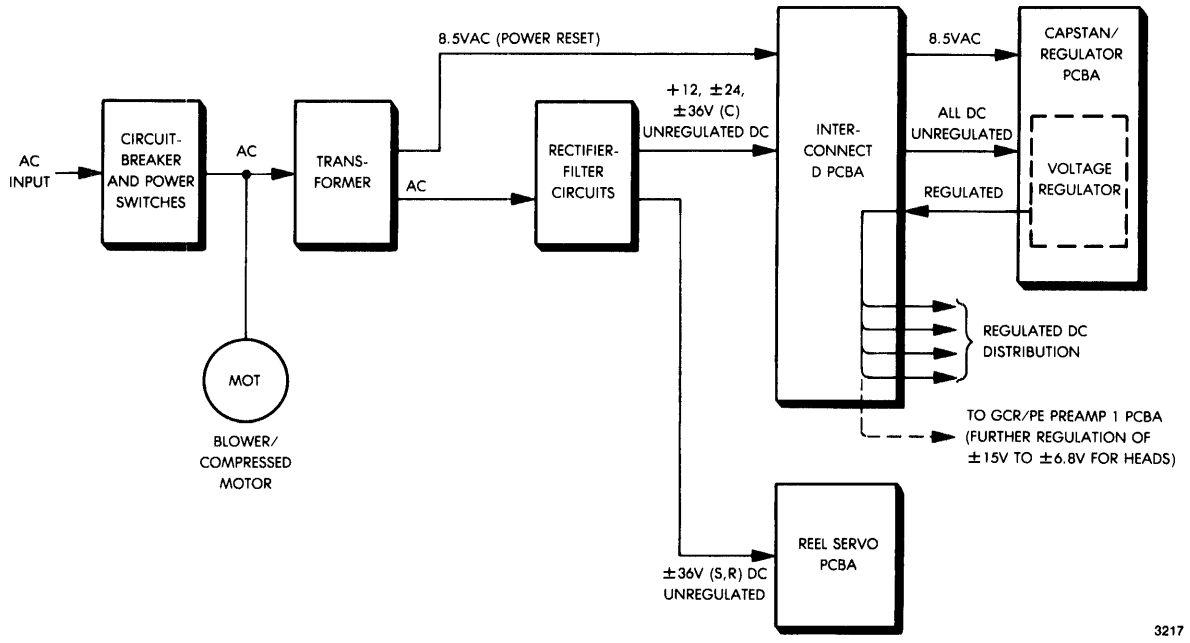


Figure 4-4. Power Supply Simplified Block Diagram

4.5 SYSTEM CONTROL

4.5.1 CONTROL SYSTEM OVERVIEW

The control logic circuitry manages the operation of the transport on the basis of commands received from the host system and/or manual commands entered by means of switches provided on the transport. Figure 4-5 is a simplified block diagram of the control logic.

Most of the control circuits are mounted on the Control M/M2 PCBA, which is plugged into connector J8 on the vertical Interconnect D/D1 PCBA. The Control M/M2 PCBA circuits are covered in detail in Section 5. The following text covers the control system in general.

Inputs and outputs from the host system are connected directly or indirectly to the card cage via J201, J202, and J203; J101, J102, and J103; or J1, J2, and J3 on the Interconnect D/D1 PCBA. The options provided by these groups of connectors are explained in Section II. An additional connector on the Write PCBA provides for interfacing by cable to the MIA or other controller. The MIA Addendum to this manual describes I/O interfacing if the MIA is used. Table 5-1 lists the connections provided by conductors on the Interconnect D/D1 PCBA. Figure 4-6 illustrates the general routing of control signals throughout the transport assembly.

4.5.2 MANUAL CONTROLS

Manual controls (refer to Table 1-2) include the system unit code select thumbwheel switch, POWER ON-OFF switch, LOAD/REW switch, ON-LINE switch, UNLOAD switch, RESET switch, and the 6250/1600 selector. Manual switching theory is shown in Figure 4-7.

The power circuit breaker switch, mounted on the rear panel, is discussed in the power supply and distribution text. (Refer to Section V.)

Manual POWER switch (S1) is an SPST rocker switch. ON position completes the circuit that remotely closes solid-state switch S2. This in turn completes the circuit that applies power to transformer T1. (Refer to Section V.)

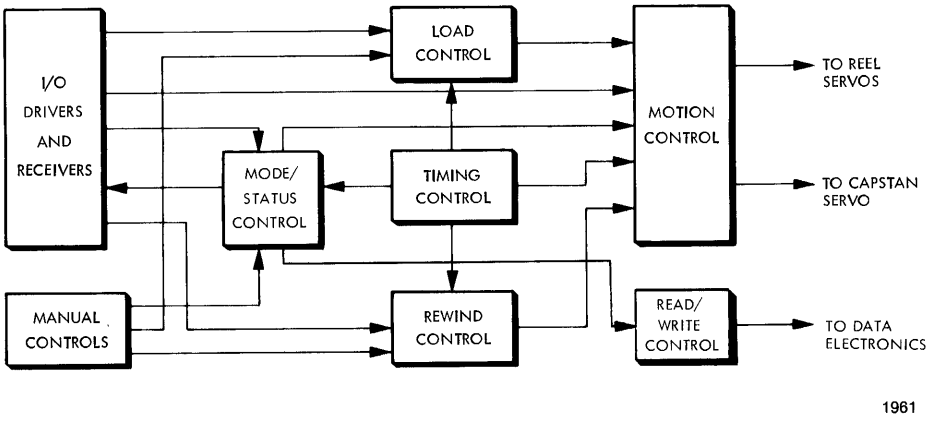


Figure 4-5. Control Logic Block Diagram

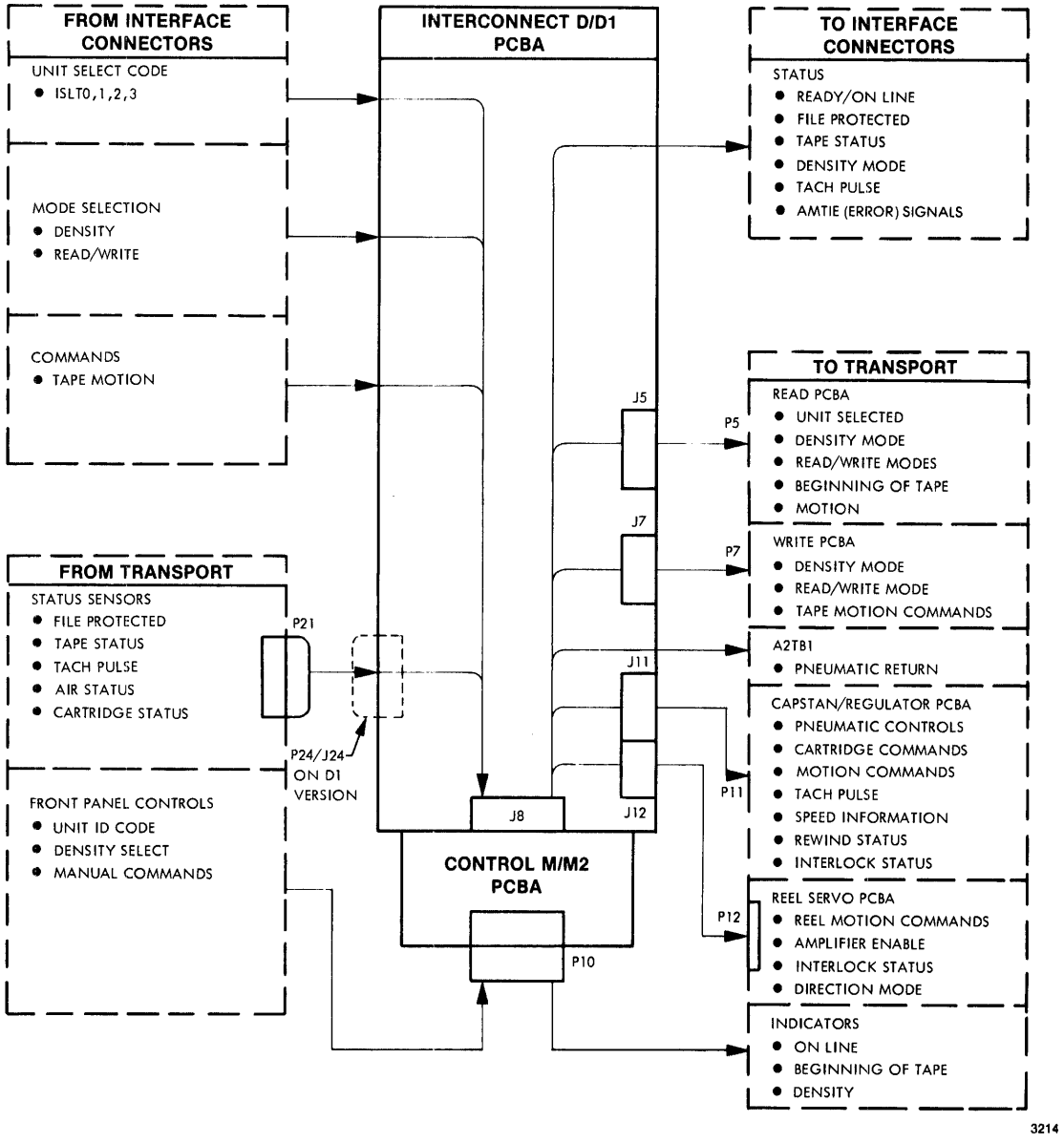


Figure 4-6. Control Signal General Routing

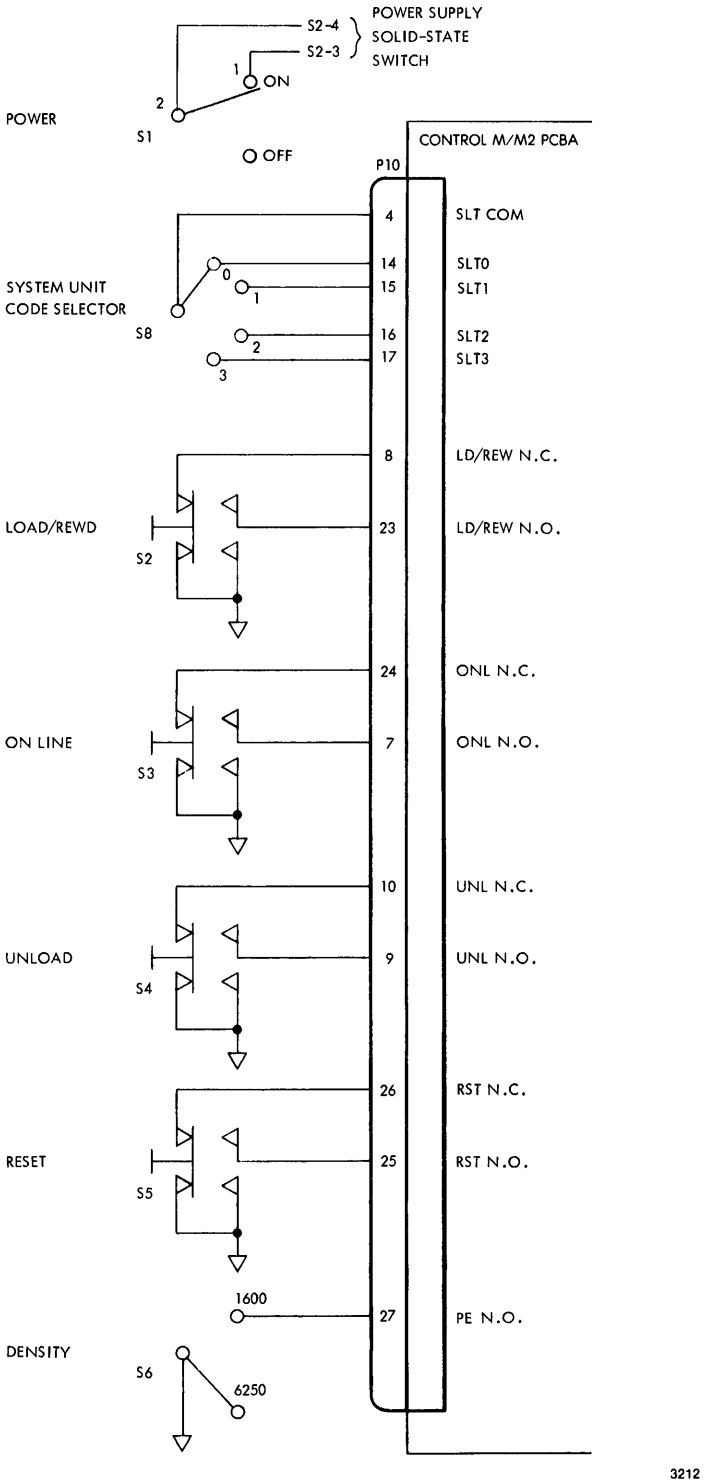


Figure 4-7. Manual Control Switching Theory

The decade thumbwheel switch located next to the POWER switch sets the transport circuits so they will respond when properly addressed by the host system. Positions 0, 1, 2, and 3 are used; other positions are spares. Contacts 0, 1, 2, and 3 are connected to the host system interface. Switch S8 connects the selected line to the select (SLT) and select A (SLTA) circuits. (Refer to Schematic No. 104745, zone 2-13C or 106875, zone 3-6C.) If the selected line is low at the interface, SLT and SLTA enable the various transport circuits involved in host system operation. In single transport systems, jumper W1 and/or W17 may be used to produce SLTA and/or SLT in place of the switch selection and input previously described.

LOAD/REW, ON LINE, UNLOAD, and RESET switches S2 through S5 (refer to Figure 4-7) are momentary, pushbutton devices that normally hold one circuit at low (nominal 0v) level. When depressed they disconnect that circuit from signal ground and momentarily bring the other switch output to nominal 0v. Circuits operated by these switch commands are located on the Control M/M2 PCBA, discussed in Section V. (Note that door switch inhibits backwrap if door is open and certain reels are used. See Paragraph 3.3.2.)

DENSITY switch S6 is an SPST rocker switch. When 6250 position is selected, the connection between the switch and P10-27 on the Control M/M2 PCBA is high (nominal +5v), which makes the low = true NPE signal false. The logic then works in the GCR mode using a recording density of 246 c/mm (6250 cpi). When the switch is placed in the 1600 position, the NPE line is low = true, and the PE high density of 63 c/mm (1600 cpi) mode is effective. The application of these selections is covered in Section V.

In addition to the operational controls, maintenance switches are provided as listed in Table 3-1. Refer to text on specific PCBAs for board-mounted maintenance LEDs.

4.5.3 LED STATUS INDICATORS

Panel LED indicators include POWER, BOT, ON-LINE, FILE PROTECT, LOAD FAULT, 6250, and 1600. All indicators are connected to system circuitry through connector P10, which is mounted on the Control M/M2 PCBA. Refer to Figure 4-8. BOT becomes illuminated to indicate that the BOT marker has been sensed and that the tape is in the beginning-of-tape position. ON-LINE indicates that the transport has been switched to the host system. (It is not an active part of the host system, however, until selected by the system and the transport is in ready status.) FILE PROTECT (FPT) is illuminated to indicate that the write-enable ring is not in place and that the file is protected against writing. When illuminated, the LOAD FAULT (LDF) indicator cautions the operator that the tape is not loaded or ready for operation. The 6250 indicator is illuminated when the adjacent switch is set for GCR operation; the 1600 indicator becomes illuminated when the switch is set for PE operation.

The indicator common (IND COM) makes +5v available to the indicators whenever transport power is ON. Any of the LEDs will conduct and emit light when the controlling input to the LED is low = true.

4.5.4 CONTROL SYSTEM INPUTS/OUTPUTS

Inputs and outputs to the control system are generalized in Figure 4-6. Interface connectors are mounted directly on the Interconnect D/D1 PCBA, which routes command/status signals between the interface and the Control M/M2 PCBA edge connector, P8. (Refer to Table 5-1 for this routing.) Alternate MIA interface connections are discussed in the MIA Addendum.

Manual control switches and associated LED indicators are connected directly to J10 on the Control M/M2 PCBA.

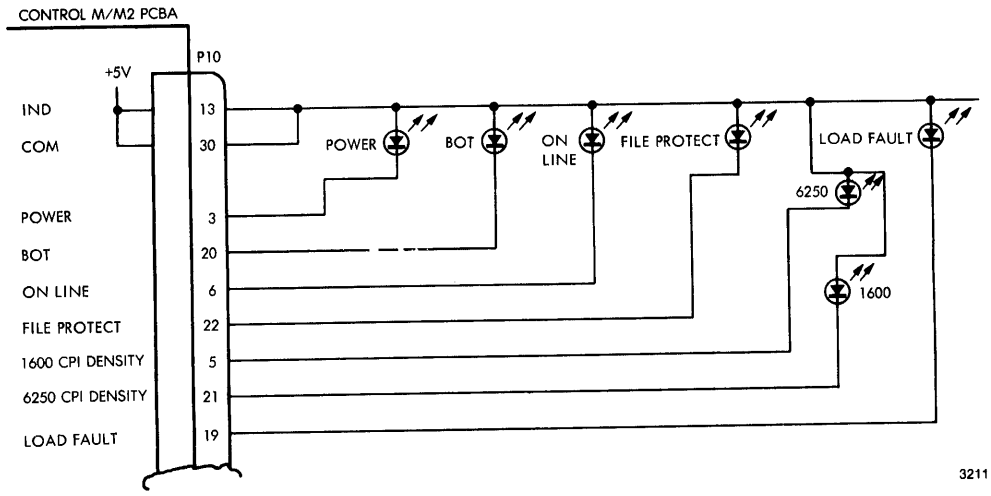


Figure 4-8. Front Panel Indicator Connections

Status sensor information (tape, cartridge, write (file) protect, etc.) is connected through Interconnect F/F1 PCBA and J21 to a fixed connection on Interconnect D/D1 PCBA, which routes them to the Control M/M2 PCBA. Outputs from the Control M/M2 PCBA to the various other card cage PCBAs (Read, Write, Capstan, Reel, Servo, etc.) are all routed via the Interconnect D/D1 PCBA, as shown in Figure 4-6 and Table 5-1.

4.5.5 GENERAL MODES OF OPERATION

Transport operational modes may be divided into two categories: Off-line modes and On-line modes.

Off-line operation includes tape loading, unloading, and maintenance/test procedures. Front panel control switches are used to select and run off-line operations. In addition to these controls, maintenance test procedures involve use of manual controls listed in Table 4-1.

On-line operation essentially includes read/write and motion procedures under control of the host system. Initiation of on-line operation requires that the ON-LINE switch is ON, the transport (in a multi-transport system) has been selected by the host controller, tape has been loaded, all interlocks have been made, and the transport has provided the Selected, Ready, and On-line (SRO) signals.

The primary commands to the control logic circuitry originate at the operator manual controls. (Refer to Figure 4-3.) The first command recognized by this logic is the Power On signal. The Capstan/Regulator PCBA logic recognizes power turnon and generates a Power-On Reset (NPORST) and Master Reset (NMRSTP) that clear the logic. This enables the logic to receive the second required manual command, LOAD. Until the tape is loaded and the necessary interlocks are made, the logic will ignore all other commands with the exception of RESET. RESET will stop the load operation and prepare for another LOAD command, in addition to its normal clearing and resetting functions.

Upon completion of a succcessful load operation, the control logic will accept all other commands except LOAD. In order to execute another LOAD, one of the vacuum interlocks must have been opened.

When the tape is loaded and positioned between the BOT and EOT, a REWIND command can be initiated via the interface or manual operator control.

NOTE

If more than one transport is used in the system, the unit select thumbwheel switch must be set to correspond with the controller's unit address code in order to operate on interface signals.

Receipt of the REWIND command by the rewind control logic causes the following:

(1) REWIND command is initiated.

(2) A high-speed reverse signal is sent to the capstan servo.

(3) Tape is wound onto the supply reel at high speed until low tape is sensed.

(4) The tape slows to synchronous reverse speed.

(5) Tape continues to wind onto the supply reel until it reaches BOT tab, where it stops.

An UNLOAD command returns the tape to the supply reel and closes the cartridge. It can be initiated from the control panel (off-line) or the interface (on-line). If the tape is not at the BOT, a rewind will be executed, then the unload operation. If the tape is at the BOT, only the unload operation will be executed.

The select lines (ISLT) from the interface to the Select switch are connected through Interconnect D/D1 PCBA J8 to the Control M/M2 PCBA routed to the front panel unit select switch via J10. If the ISLT number agrees with the unit select switch setting, the switch provides the select signal (NSLT) to the input logic via J10. The input logic provides the select signal (SLTA) to the output logic; the output logic NSLTA to the Read Function via J8-23.

After power is on, the reset signal (NPORST) enables the input and output logic and the front panel switches to provide control of the transport. When NPORST is low or the RESET switch is pressed and released, the logic provides the master reset signal (NMRSTP) to the rewind generator and the Air Subsystem NMRSTP clears the rewind generator and the logic in the Air Subsystem. When NPORST goes high it initiates enabling of the front panel indicators.

The +5v and logic return lines are connected to the EOT/BOT assembly via TB2 on the Interconnect F PCBA. The EOT/BOT assembly provides the off-tab voltage and either the EOT or BOT voltage depending on which tab is detected. These voltages are supplied to the EOT/BOT amplifier. The EOT/BOT amplifier provides the NBOT or NEOT signals, via P21, to the input logic. R6 (R22) on Interconnect F (F1) PCBA adjusts NBOT and NEOT voltages.

At power on, inputs to the Control M/M2 PCBA initiate a PE and a data density indicator signal (DDI) to the PCBAs output logic. The output logic provides either a low NPE1 or a low PE1 to light the 6250 indicator depending on the optional DENSITY switch position or the state of the interface signal, IDDS. The output logic also provides the density signal (NPE) to the Read function and Write function via J8-25. At the same time, the Write function provides a file protect signal (FPT) to the output logic via J8-60. The output logic provides a low FPT1 to light the FILE PROTECT indicator if the Write Enable ring is not installed.

When the Air Subsystem detects a load command, it provides a low load status signal (NLDS) to the ready generator (Control M/M2 PCBA). The low NLDS disables the ready generator during a load sequence.

After the loops are set in the buffer boxes, the Air Subsystem initiates an interlock signal (INTLK1), not more than one second after interlock has been detected, to the rewind generator. Approximately one second after INTLK1, the delayed interlock signals (DINTLK and NDINTLK) and the interlock pulse (INTLKP1) are generated (Control M/M2 PCBA), DINTLK is applied to the rewind generator, the ready generator and the input logic. At the same time, NDINTLK and INTLKP1 are coupled to the input logic. If interlock is lost, the function provides a loss of interlock pulse (NLOIP) to the rewind generator. NLOIP disables the rewind generator.

The high DINTLK from the Air Subsystem to the rewind generator causes the generator to produce the rewind signals REV, RWS and NRWS. REV is applied to the Capstan Servo function and causes the transport to rewind to BOT. At the same time, the low NRWS disables the ready signal (RDY). If either NMRSTP from the input logic or NLOIP from the Air Subsystem are low, the rewind generator provides a reset signal (NRST1) to the input logic.

When the BOT tab is detected, NBOT is sent from the EOT/BOT amplifier to the input logic (J8-52). The input logic applies NBOT1 to the rewind generator and the motion control. NBOT1 resets the rewind generator and provides a low REV that removes the drive from the Capstan Servo function. The high NRWS enables the ready generator. The input logic also provides BOT and NBOT to the output logic and BOT to the Air Subsystem. The output logic provides the drive signal, NBOT2, that lights the BOT indicator on the front panel. The output logic also provides the BOT1 signal to the Read function via J8-48.

When DINTLK, NLDS and the unload signal (NUNL1) are high from the Air Subsystem and NRWS is high from the rewind generator, the ready generator provides the ready signal (RDY) for the motion control and the input logic. TP24 (Control M/M2 PCBA) is used to monitor the ready signal.

The ONL N.O. and ONL N.C. are provided to the input logic from S3, the front panel ON LINE switch. When ONL N.O. is low, the input logic provides three on-line signals (ONL, NONL, and a delayed signal, DONL). The high ONL from the input logic to the output logic provides NONL1 which lights the front panel ON LINE indicator. At the same time, NONL is sent to the motion control and Air Subsystem. The delayed on line signal, DONL, is sent to the output logic. If the transport is Selected, Ready and On-line, the input logic provides the SRO signal to the output logic.

The SRO signal at J8 (from Control M/M2 PCBA output logic) enables the status interface lines. The status lines reflect the state of the transport. If the transport is:

(1) At BOT, ILDP is low
(2) File Protected, IFPT is low
(3) On Line, IONL is low
(4) RSO, IRDY is low
(5) PE, IDDI is low.

The other status lines (ITACH, IRWD, and IEOT) are enabled later.

When the transport is Selected, Ready, and On-line, the input interface lines become active. When the input logic detects a forward command (ISFC low) or a reverse command (ISRC low), the input logic provides a low NSFC or a low NSRC to the motion control.

The motion control is enabled by a low NONL from the input logic and a high RDY from the ready generator. If the transport is at BOT (NBOT1 low), the motion control is enabled to accept NSFC and disables NSRC. If the transport is at EOT (NEOT), the motion control is

enabled to accept NSRC and NSFC. When a valid NSFC or NSRC is detected by the motion control, it provides the motion signals (NGOP, MOT, NMOT, MOTION, and NMOTION) and the direction signal, REV (REV high = reverse, REV low = forward) depending on the state of NSRC and NSFC. MOTION is supplied to the Read function and the Write function via J8-28. NMOTION is coupled to the stop pulse generator. MOT and NGOP are provided to the Capstan Servo function and NGOP is also provided to the input logic. NMOT is applied to the Capstan Servo function via J8-51, REV is also sent to the Capstan Servo function and the Reel Servo function via J8-66.

When NONL is high, the maintenance switch (S1 on Control M/M2 PCBA) is enabled. This switch allows for off-line testing of the transport. S1 moves tape in a forward and reverse direction. TP21 is used to monitor MOTION. TP22 is used to monitor reverse and TP23 is used to monitor forward. TP30 and TP31 are for applying a clock (CLKE or CLKG) to test the manual FWD/REV circuits.

When the motion control output (TP21 Control M/M2 PCBA) goes high, it initiates the output of a high stop pulse on the NDRV line at P8-65. This causes NMOT and the stop pulse to apply dynamic braking to the transport mechanism for a specified time determined by the duration of the pulse. Refer to Section V for details of circuits on Control M/M2 PCBA.

4.5.6 AIR SUBSYSTEM

The Air Subsystem includes the air and electronic provisions that control and monitor the path travelled by the tape between the reels. Refer to Figure 4-9.

The speed at which the tape passes the read and write heads is controlled by the Capstan Servo subsystem (refer to Paragraph 4.5.8). The speed of the supply and takeup reels must vary according to the quantity of tape on the reels. For example, when the supply reel is full and the takeup reel nearly empty, the takeup reel must rotate much faster than the supply reel in order to properly transfer the tape. Each of the reels is driven by a separate motor, controlled by a servo system (refer to Paragraph 4.5.7) that adjusts the speed as required to maintain proper tape transfer and tension. The subject Air Subsystem provides tape loop status signals to the Reel Servo circuits, which use the information to regulate the power applied to the reel motors.

The input port of the cabinet-venting centrifugal blower is used as the source of vacuum (minus atmosphere) pressure that forms the tape loops. (Refer to Figure 1-2.) Vacuum is applied to the buffer boxes, loop pocket, corner pockets, and the capstan. Energizing solenoid K3, on the vacuum valve, switches vacuum to the hub of the takeup reel to facilitate threading. A typical tape loop formation is illustrated in Figure 4-10.

4.5.7 REEL SERVOS AND LOADING/UNLOADING

4.5.7.1 General

The Reel Servo controls the speed of the tape reels as required to maintain optimum tension on the tape between the supply and takeup reels, the tension being interpreted from the positions of the tape loops as sensed by the Air Subsystem.

Figure 4-11 illustrates the basic theory of operation as applied to each of the reels. Servo operation is initiated by any of the tape motion commands; e.g., Synchronous Forward, Synchronous Reverse, or Rewind. If the tape filled supply reel is properly loaded, the Air Subsystem in operation and interlock circuit status is acceptable, reel motion will begin. The speed of reel rotation is subject to feedback information from the Air Subsystem (Paragraph 4.5.6). This information includes the tape loop position transducer output for the appropriate servo (supply or takeup) as well as information on certain unsatisfactory

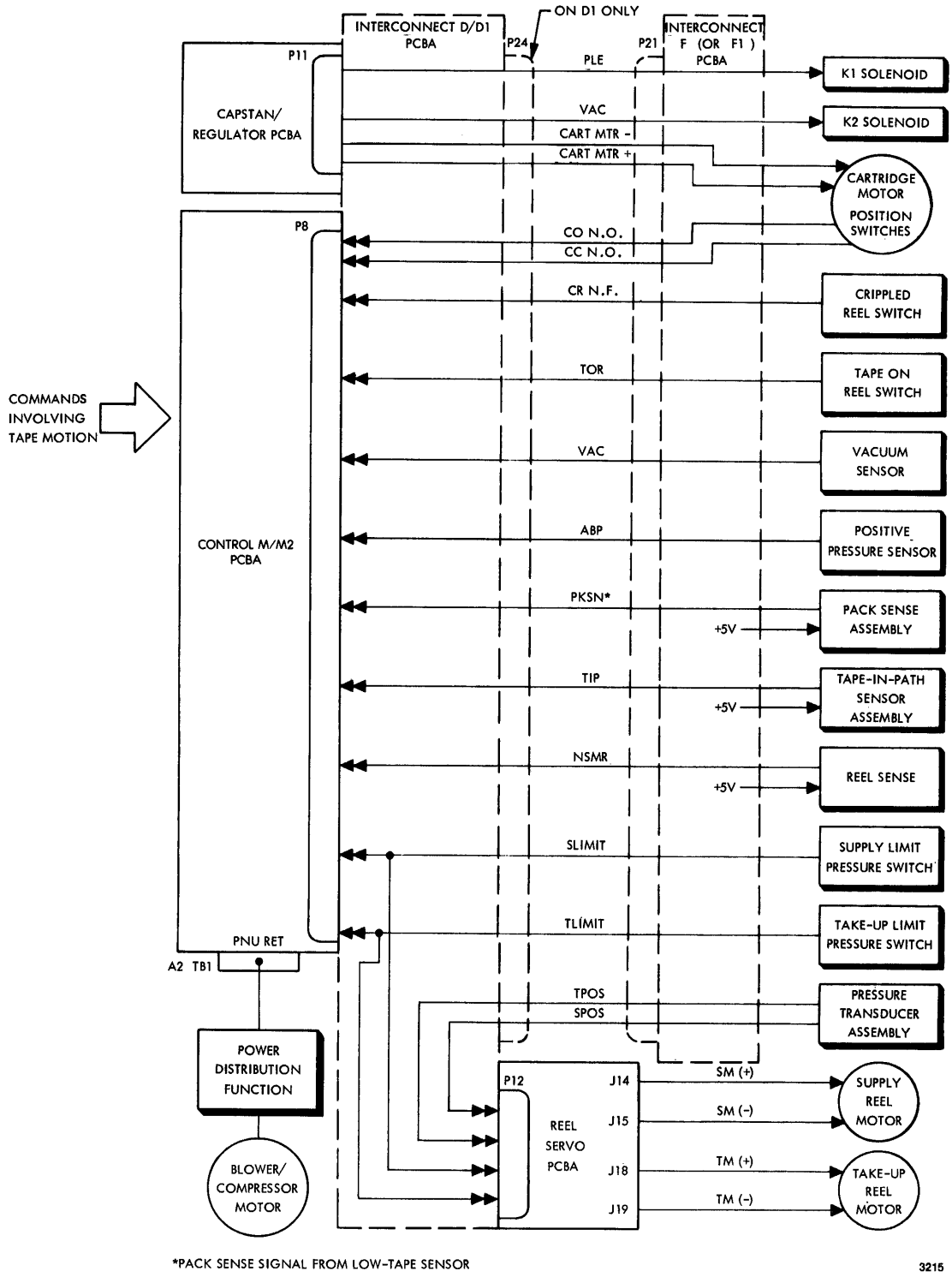


Figure 4-9. Air Subsystem

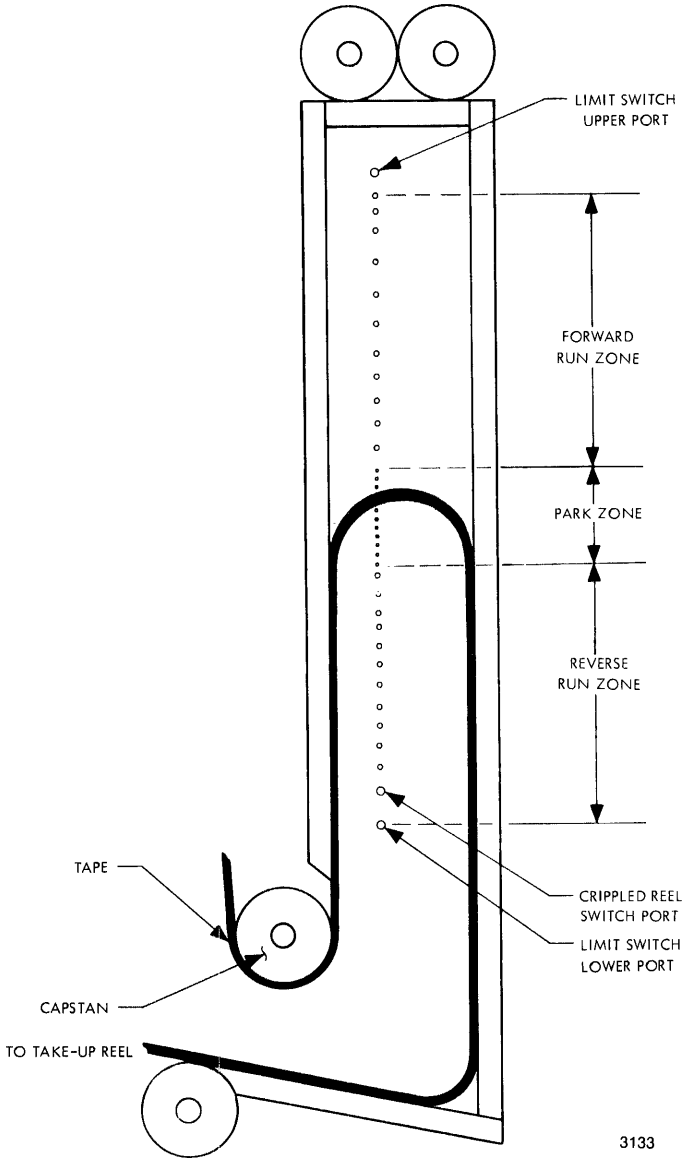


Figure 4-10. Tape Loop In Take-up Buffer Box

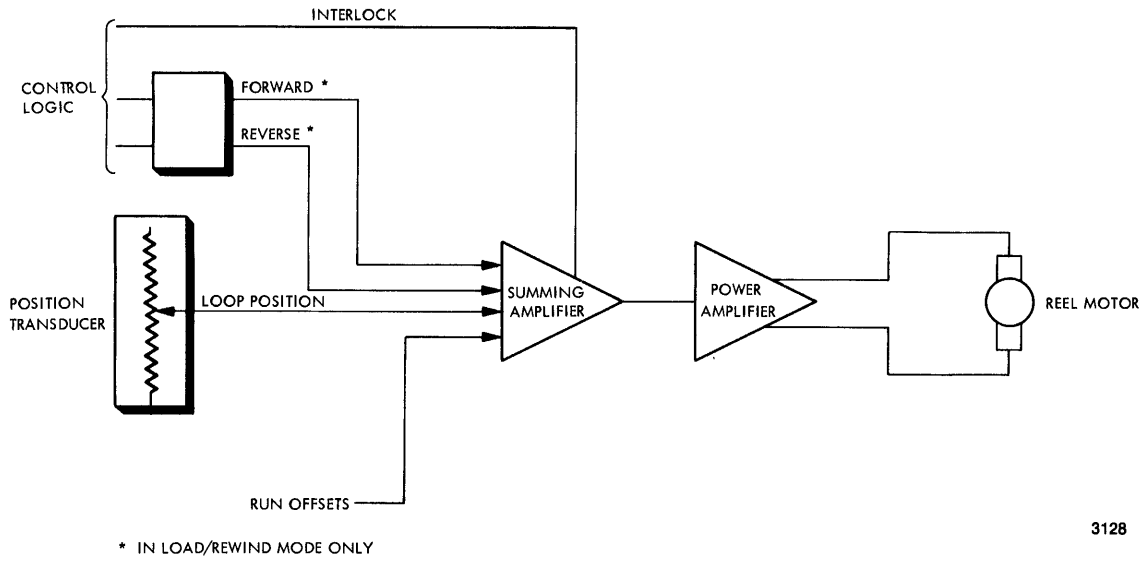


Figure 4-11. Reel Servo Block Diagram

conditions. The run offset inputs are not necessarily unsatisfactory inputs. They pertain to adjusting the reel motion to achieve a different loop configuration for different tape motion directions.

The supply and takeup reel servo networks are identical except for the polarity of the position transducer outputs and the inclusion of the crippled reel signal in the takeup reel servo circuits.

During load and unload operations, when the tape path has not stabilized, the speed of the reels is totally a function of voltage specified by the control electronics. Load and unload sequences are described briefly in the following paragraphs; however, hardware circuits involved are detailed in Section V.

4.5.7.2 Tape Loading Operation

During a load operation, the following series of events occur. Refer to Figure 4-12 in conjunction with this description.

NOTE

If tape is loaded, all slack should be removed by manually turning the reels before pressing the LOAD/REW switch.

(1) When the LOAD/REW button is depressed, the blower and compressor will activate, the cartridge motor will open the cartridge, the reel servo amplifiers are enabled, and the takeup reel motor will turn clockwise (CW).

(2) If there is tape in path at this time, a midreel load situation is assumed and the unit will set loops and start towards BOT.

(3) If tape was not in the tape path, a normal load will be initiated as follows.

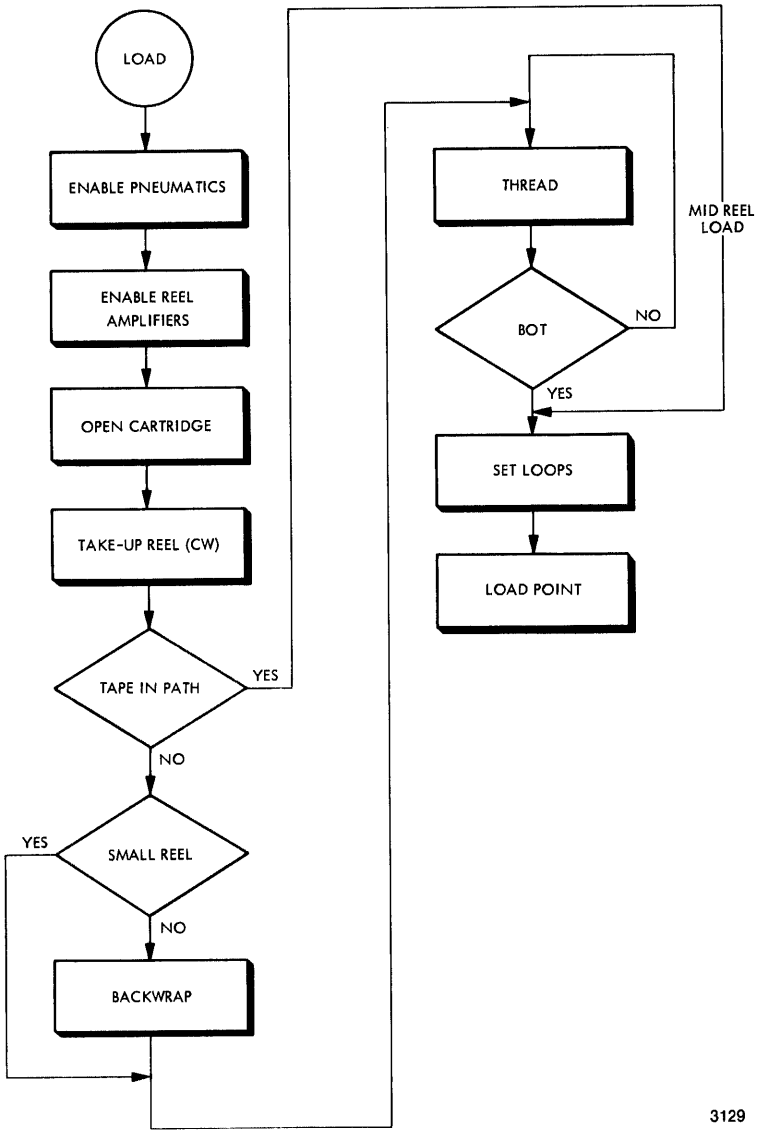


Figure 4-12. Simplified Load Sequence Flow Chart

(4) With the supply reel door closed (or the door switch manually set), the reel will backwrap for approximately two turns before starting the threading process.

NOTE

If the diameter of the outside turn of tape is too small, it may be necessary for the operator to manually place the tape in the tape path. Also, reels smaller than 267 mm (10.5 inch) diameter require the operator to place the leader over thread block 1 (refer to Figure 3-2).

(5) After backwrapping, the supply reel will start forward and tape will thread through the tape path.

(6) When beginning of tape (BOT) is detected, vacuum is applied to the buffer boxes and the reel motors will turn such that tape loops will be set in the buffer boxes and interlock will be made.

(7) The transport is then ready for controller commands and data run operation.

4.5.7.3 Reel Servo Circuits, Read/Write Modes

When the tape is satisfactorily loaded, the transport is ready to make data runs, etc., as commanded by the controller. When a motion command arrives at the interface, the System Control subsystem sends a drive (NDRV) and direction (REV, true or false) signal to reel servo system. These signals are applied to the summing logic for the supply and takeup loops. Mode Control outputs and status signals received from the Control M PCBA are also applied to the summing logic and the resulting output is applied to the power amplifiers that drive the reel motors.

4.5.7.4 Reel Servo Circuits, Unload Operation

The same auxiliary circuits employed to load tape and form loops in the buffer boxes (load operation) are used during an unload operation. Refer to the flow chart shown in Figure 4-13. When the UNLOAD button is depressed while the unit is at mid tape, the following sequence is initiated:

(1) Tape rewinds to BOT.

(2) Blower motor is turned off causing the interlock to be broken.

(3) Tape is wound onto the supply reel.

(4) Reel motors are stopped.

(5) Cartridge is closed.

Unload procedure with tape at BOT is identical to the above but without rewind operation.

4.5.8 CAPSTAN SERVO

The Capstan Servo is a velocity management system that acts as the prime tape mover to pull tape across the magnetic head assembly for data recording or reproduction. The capstan servo consists of the functional blocks shown in Figure 4-14.

The heart of the servo is the Summing Amplifier. This amplifier receives current signals from three sources, sums them, and forces the Power Amplifier to the proper voltage. The Power Amplifier applies this voltage to the Capstan Motor which responds with the appropriate speed. The Capstan Tachometer is shaft-coupled to the Capstan Motor and produces a frequency output proportional to the speed of the Capstan Motor. This frequency is converted to voltage, which is the tachometer feedback required for constant velocity operation.

The primary inputs to the capstan servo are the logic control signals. These signals initiate either a positive or negative ramp for forward and reverse operation, or a long rewind ramp used to accelerate the Capstan Motor to rewind speed. The ramp slopes and final velocities for forward and reverse are adjusted to achieve the desired start/stop characteristics.

Figure 4-15 illustrates typical capstan servo waveforms. The following sequence of events describes the normal operation of the capstan servo:

(1) When power is applied, tape loaded, and interlock is made, the capstan power amplifier is enabled.

(2) Upon receipt of an ISFC command, capstan drive current is applied in the forward direction. The magnitude of the current is constant and determines the constant rate of acceleration.

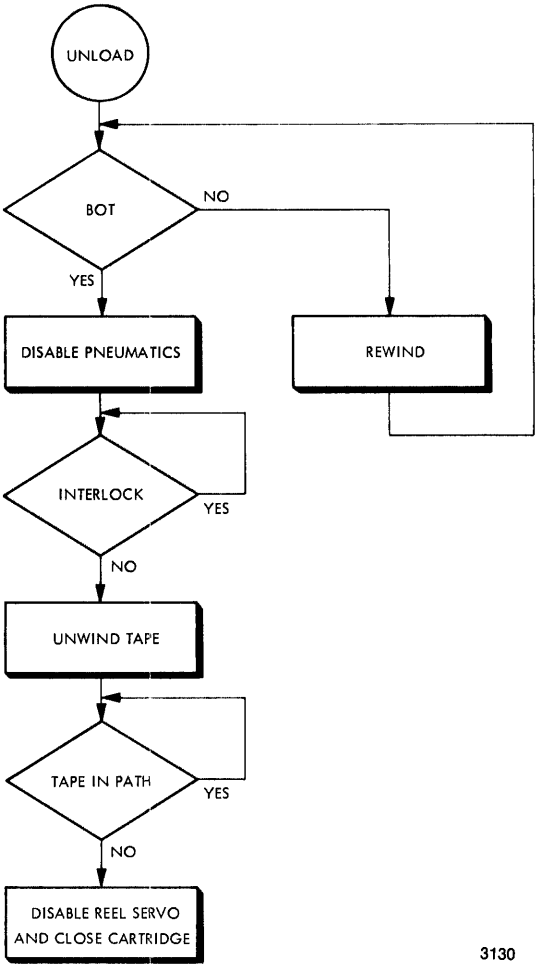


Figure 4-13. Simplified Unload Sequence Flow Chart

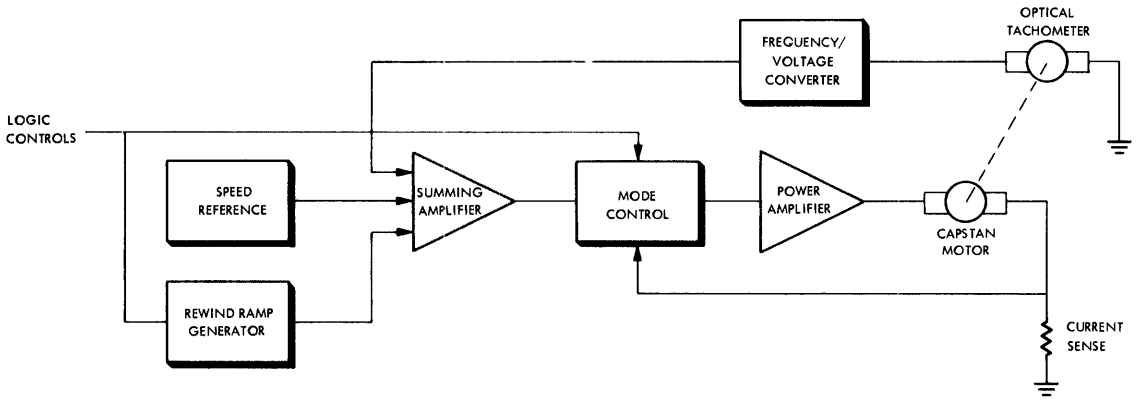


Figure 4-14. Capstan Servo Block Diagram

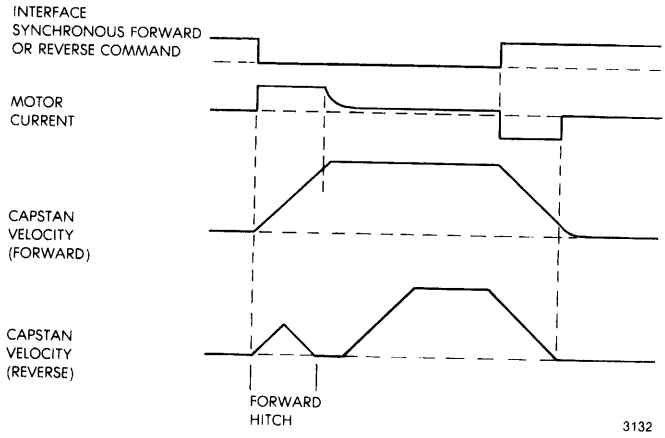


Figure 4-15. Capstan Servo Waveform for Forward or Reverse Start and Stop

(3) As the capstan approaches synchronous speed the difference between the commanded speed and the actual speed decreases as does the capstan drive speed.

(5) When ISFC is terminated, the polarity of the drive circuit is reversed. This reverse current is maintained at a constant level for a fixed time.

(6) At the end of the reverse current pulse the capstan motor drive voltage is brought to and held at ground level to produce a dynamic braking effect.

NOTE

The synchronous reverse mode (ISRC) procedure is identical except for reversals of direction and drive current, unless a delay of 10 to 20 milliseconds has ensued since the termination of the previous motion command. Refer to step (7).

(7) Upon receipt of an ISRC command following a delay, a brief forward motion hitch is initiated to break loose the tape surface tension prior to initiating reverse motion.

Each time power is applied to the unit, the Power Distribution block generates a reset signal (NPORST) to the velocity decoder on the Control M/M2 PCBA and the Capstan Control logic on the Capstan/Regulator PCBA. After tape is loaded into the vacuum column, the interlock signal (NINTLK) from the Air Subsystem goes low and enables the capstan amplifier.

The System Control function, upon receipt of a motion command, supplies the following signals to the capstan mode control logic: drive (NDRV), direction (REV), motion (NMOT), and speed greater than 80 percent (N>80%). (N indicates low = true.)

The Power Amplifier provides drive to the capstan motor via J11 and TB1-2,3 on the Interconnect D/D1 PCBA.

Tachometer pulses, from the optical sensor mounted on the capstan shaft, are amplified on Interconnect F/F1 PCBA. The signal is routed through Interconnect D/D1 PCBA to Control M/M2 PCBA where it is squared and sent to the velocity decoder (TAP1) and the interface (TACHP). There are 8 tachometer pulses per capstan revolution. The velocity decoder generates a 20 μsec pulse for each TAP1. This is called NTAP2 and is sent to the Capstan/Regulator PCBA where it is converted by the tachometer frequency/voltage converter to the feedback analog (ATACH) signal for the capstan summing amplifier.

4.5.9 DATA ELECTRONICS AND MAGNETICS

Contemporary data handling requires the coding of data in terms of a binary language (in the generalized, non-computer sense) composed of two elementary symbols. The data may consist of any information, idea, or quantity that might otherwise be expressed by means of 26 alphabetic-character symbols, 10 decimal-number symbols, and/or a variety of miscellaneous marks used for punctuation, abbreviations, etc.

The two elements of the binary-coding system are referred to variously as 1 and 0, true and false, yes and no, high and low (not necessarily respectively), set and reset, asserted and nonasserted, etc., depending on the discipline or context involved. The written symbols for the two elements are usually 1 and 0, regardless of connotations. In discussions regarding the logic (meaning) of the data, without reference to the electronic or magnetic implementation, the significance of the symbols is uniformly as follows:

1 = numeric (binary) 1, true, yes, set (as a flag), or asserted

0 = numeric (binary) 0, false, no, reset (as a flag), or nonasserted (negated)

Electronically, 1 and 0 are coded by two voltage levels. In most circuits these levels are nominally +5v dc and 0v dc, although in the formatter internal circuits the actual threshold for the high voltage is approximately +2.5v dc. The 0v level is referred to as *low* and the +5v dc as *high*. There is no consistent relationship between the 1 or 0 symbols and the low or high voltage levels, because hardware economy requires frequent inversion of the voltage levels. The terms *logic high* and *logic low*, therefore, are ambiguous. Magnetically, as impressed upon the tape, the two symbols may be encoded in various ways, depending on the coding method(s) chosen for the system.

The T1960 Tape Transport uses either the Group Coded Recording (GCR) method or the Phase Encoded (PE) method. Magnetically, GCR is identical to Non-Return to Zero, Inverted (NRZI) but in other respects there is considerable difference between GCR and NRZI formats. These differences, however, are in translation of data before reaching the tape transport.

Figure 4-16 illustrates differences between PE and GCR magnetic formats with respect to the history of tape format development. An arbitrarily chosen pattern is presented on the Data Sample line at the top of the illustration. One bit of data is placed in each cell defined by the vertical dash lines.

The Return to Zero (RZ) data 1s are coded on tape by magnetization in the positive (+) direction within the center of the cell, with a return to zero magnetization before the end of the cell time. Data 0s are coded on tape by similar magnetization in the opposite direction.

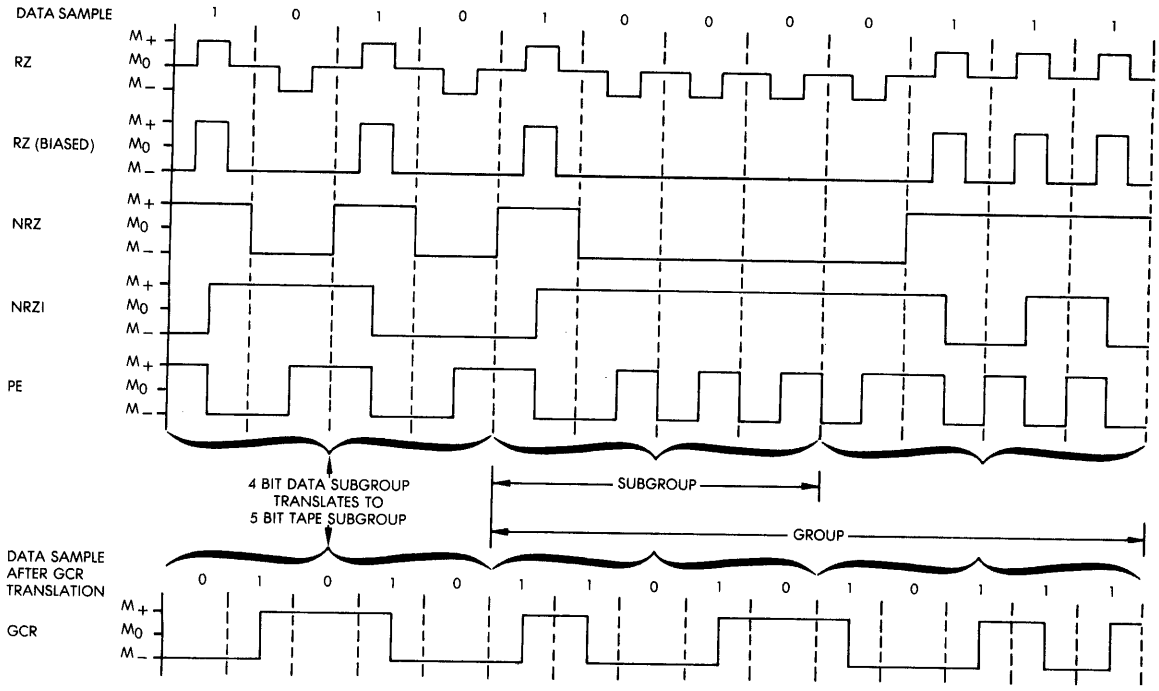
NOTE

In this discussion, the direction of magnetization of the Inter-Block Gap (IBG) is that in which the north pole of magnetic particles on the tape point to the supply-reel end of the tape. This is called the negative direction of magnetization.

In Return to Zero (RZ), Biased, coding, the entire tape is biased (magnetically recorded) in the negative direction and interpreted as all 0s except where a data 1 is recorded by magnetization in the positive direction within the appropriate cell time.

Non-Return to Zero (NRZ) is similar to RZ except that a series of 1s can be recorded in the same manner as a series of 0s; i.e., there is no return to zero magnetization or to magnetization in the negative direction between 1s.

Non-Return to Zero, Inverted, (NRZI) provides for encoding 1s by any change in the direction of magnetization within a cell. Whether the change is from negative to positive direction or from positive to negative has no significance. Conversely, any cell in which there is no change in the direction of magnetization is interpreted as a data 0.

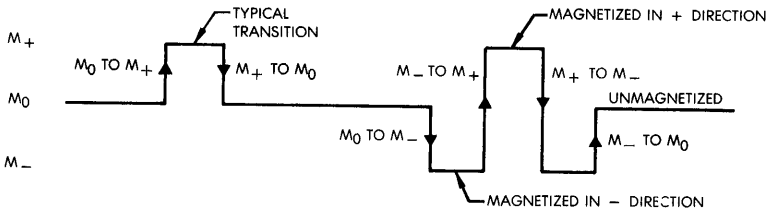


LEGEND

1. VERTICAL DASH LINES DEMARK BIT TIME CELLS.
2. DIRECTION OF MAGNETIZATION (PARTICLE ORIENTATION).
   - M_+ MAGNETIZATION IN THE POSITIVE DIRECTION.
   - M_0 UNMAGNETIZED STATE.
   - M_- MAGNETIZATION IN THE NEGATIVE DIRECTION.

   EXAMPLE: IN THE NEGATIVE DIRECTION, NORTH-SOUTH PARTICLE ORIENTATION IS AS FOLLOWS:

3. WAVEFORM ELEMENTS



ARROWS SHOW DIRECTION OF FLUX CHANGES (TRANSITIONS). CHANGES FROM M_+ TO M_- AND M_- TO M_+ ARE OFTEN CALLED FLUX REVERSALS.

4. IN GCR AND NRZI, ANY TRANSITION BETWEEN FLUX DIRECTIONS IS A 1 BIT. NO CHANGE IS A 0 BIT.
5. IN PE, A TRANSITION TOWARD THE DIRECTION OF IBG FLUX IS A 1 BIT; A CHANGE IN THE OPPOSITE DIRECTION IS A 0 BIT.

3348

Figure 4-16. Tape Magnetic Format Evolution

Phase Encoded (PE) recording involves interpretation of the phase (direction) of change of magnetization, a change within a bit cell window from negative direction to positive direction symbolizes a data 0 and a change from positive direction to negative direction symbolizes a data 1. This method requires an unreadable change at the edge of a cell (between cell windows) in order to record two 1s or two 0s, consecutively, since the *direction of flux change* is the significant factor in PE encoding. For this reason, PE requires a greater number of flux changes than does NRZI for the same data pattern unless the pattern is a series of alternate 1s and 0s.

Group Coded Recording (GCR) is identical to NRZI with respect to magnetic encoding: a flux change within a cell time symbolizes a data 1; no flux change symbolizes a data 0. The difference between GCR and NRZI is that in GCR data are translated in the formatter to a different serial configuration of bits in which no more than two 0s will occur in sequence. This translation provides for self-clocking of data, as in PE and the flux change economy of NRZI. These translations and error detection and correction features make it possible to record data more densely on the tape. The arbitrary data sample (top line in Figure 4-1) is translated to the data sample shown in the lower (GCR) portion of the illustration. Although seven bits of the original data plus one ECC bit require ten bits in the translation, the efficiency of GCR permits recording meaningful data, exclusive of control bits, at a density of 246 c/mm (6250 bpi) as compared to 32 c/mm (800 bpi) in straight NRZI recording, and 63 c/mm (1600 bpi) for PE. Comparison of the NRZI and GCR waveforms, however, show that in both cases a 1 is magnetically symbolized by a flux change in either direction and a 0 by the absence of a flux change.

Figures 3-3 and 3-4 illustrate waveforms representative of data written on a channel along with the readback waveforms for PE and GCR formats, respectively. Magnetization transitions recorded on the tape are not perfectly sharp due to the limited resolution of the magnetic recording process.

During a Read operation, as the tape passes over the Read head, any flux pattern recorded on the tape (one or zero) generates a waveform in its appropriate data track. It is important to note that during a Read Reverse operation, the Read signal is inverted, i.e., a PE one bit is a negative transition and a PE zero bit is a positive transition.

In extreme cases when the PE data signal drops below the normal threshold, an extra-low read-recovery threshold level is employed. This extra-low threshold level can be selected through the interface (IRTH2 Command) and reduces the threshold level to approximately 5 percent while IRTH2 is low = true. The lowest level set for GCR format is 15 percent.

The data electronics do not include provisions for deskewing PE data. The customer must provide this function through use of an external formatter or similar device.

There are two types of skew associated with reproducing data; these are static and dynamic. Static skew is caused by misalignment of the head azimuth and gap scatter. Azimuth misalignment is normally corrected by adjusting the tape path and/or head plate. Dual-stack models also employ electronic deskew since the tape path cannot be separately aligned for both stacks.

Dynamic skew refers to a lack of synchronization of the various bits in a character due to imperfect tracking or processing of bits in any of the channels. Circuits on the Read PCBA provide a time frame for receipt of all bits of nine-track GCR character. These circuits also initiate a status warning (LATE AGC) if certain all-1s test/control characters are not complete within the time frame. PE characters are externally deskewed.

The dual-stack head enables simultaneous read and write operations to take place, thus allowing writing and checking of data on a single pass. Gap scatter in both the write and read heads is held within tight limits so that correction is not necessary. However, the azimuth angles of both heads are not held within tight limits, and correction is therefore necessary.

The read head azimuth adjustment is provided by mechanically positioning the head plate so that the tape tracks at approximately 90 degrees to the read head gap. Since the write and read heads are constructed in the same block, an independent method of azimuth adjustment is required for the write head. This is achieved electronically by triggering the write waveform generator for different channels sequentialy and at such times that the azimuth error in the write head is minimized.

4.5.10 PE/GCR COMMON TAPE FORMATS

The following definitions of recording format elements apply to both the PE and GCR modes. The terms are illustrated in Figure 4-17.

(1) **Bit** — The smallest unit of binary information, either 0 or 1.

(2) **Byte**, or **Character** — Made up of several bits; e.g., a byte on tape consists of 9 parallel bits.

(3) **Block**, or **Record** — Consists of multiple bytes taken in series. The number of bytes within any given block is determined by the programmer.

(4) **File** — Made up of many blocks taken in series and separated by Inter-Block Gaps. The number of blocks within any given file is determined by the programmer.

(5) **Tape Mark**, or **File Mark** — A special control block which separates data elements.

(6) **Inter-Block Gap**, or **Inter-Record Gap** — A portion of tape containing no information, used to separate blocks of data.

(7) **Channel** — The path taken by serial bits read from (or that will be recorded on) a single track on the tape.

NOTE

In practice, channel and track are often used as synonymous terms; but the number assigned to a channel is a function of the order of bits in a parallel byte, while track numbers are assigned in numerical order from the reference edge of the tape.

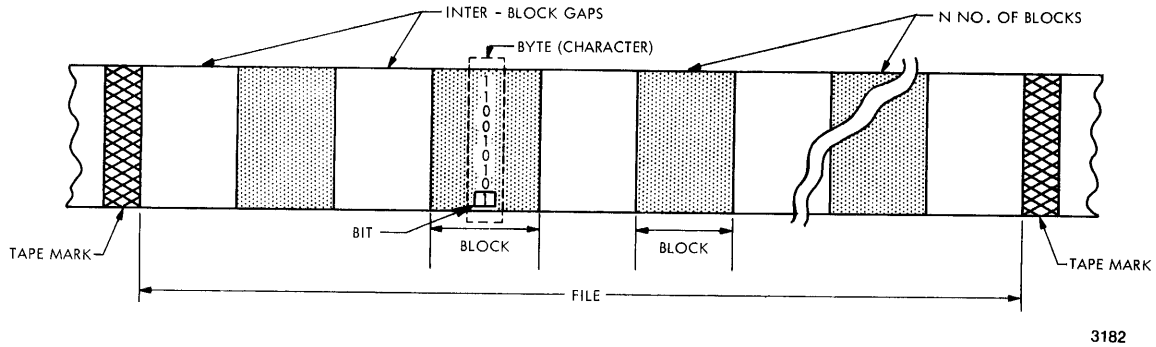


Figure 4-17. Common Data Format Elements

(8) **Track** — The portion of the tape on which one channel of bits in series may be magnetically recorded.

(9) **Tape Format** — The entire set of parameters that uniquely define the characteristics of information as written on magnetic tape during a specified recording mode.

4.5.11 PHASE ENCODED (PE) MODE FORMATS

Recording formats for the Phase Encoded mode, operating at a character density of 63 c/mm (1600 cpi) are presented in the following illustrated text. ANSI interchange parameter limits and Pertec values within these limits are discussed.

4.5.11.1 PE Mode Overall Tape Format

The overall tape format for PE mode is illustrated in Figure 4-18. Portions of this format are detailed in Paragraphs 4.5.11.2 and 4.5.11.3.

4.5.11.2 PE Mode Tape Mark Format

Figure 4-19 details the tape mark format used in PE mode. The tape mark is a special control block consisting of 64 to 256 flux reversals, at 126 flux reversals per millimeter (fr/mm) (3200 frpi), in channels 2, 6, and 7. Channels 1, 3, and 4 are dc-erased. Channels 5, P, and 0, in any combination, may be dc-erased or recorded in the manner stated for channels 2, 6, and 7. The Pertec system uses 64—256 flux reversals in a tape mark. Tape marks are generated externally.

4.5.11.3 PE Mode Data Block Format

Figure 4-20 details the format for the data block. The Preamble consists of 40 characters of 0s followed by one character of 1s. A character is defined as nine bits in parallel, one bit per track (channel). The Postamble consists of one character of 1s, followed by 40 characters of 0s.

4.5.12 GROUP-CODED RECORDING (GCR) MODE FORMATS

Recording formats for Group-Coded Recording mode, operating at a character density of 246 c/mm (6250 cpi) are presented in the following illustrated text. ANSI interchange parameter limits and Pertec values within these limits are included.

4.5.12.1 GCR Mode Overall Tape Format

The overall tape format for GCR mode is illustrated in Figure 4-21. Portions of this format are detailed in Paragraphs 4.5.12.2 and 4.5.12.3.

The Density Identification Area in the GCR recording format is identified by a burst of the recording at the BOT marker. This burst is in the PE frequency range on channel 1, with erasure on all other tracks. The ID burst begins 43.18 mm (1.7 inches) minimum before the trailing edge of the BOT marker and continues past the trailing edge of the BOT marker.

The Automatic Read Amplification (ARA) Burst, immediately following the ID burst, consists of all 1s in all tracks, separated from the ID burst by an undefined gap. The burst of 1s is placed as follows: It begins no sooner than 38.1 mm (1.5 inches) and no later than 109.21 mm (4.3 inches), as measured from the leading edge of the BOT marker. It ends no sooner than 241.3 mm (9.5 inches) and no later than 292.1 mm (11.5 inches), as measured from the leading edge of the BOT marker.

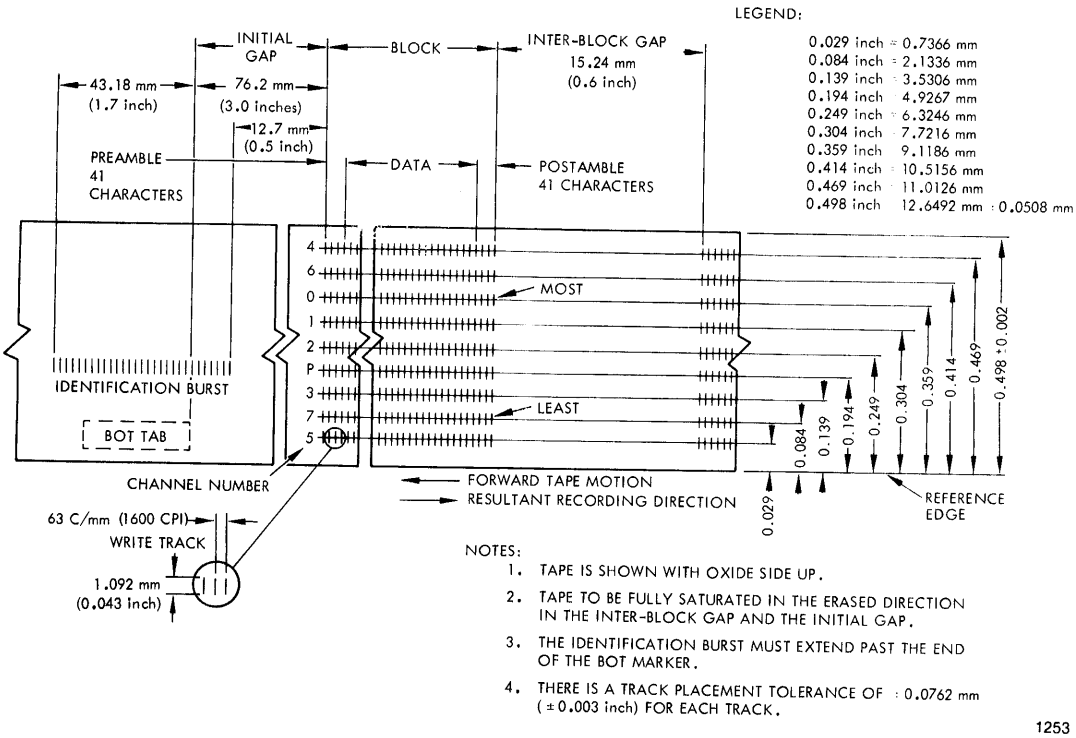


Figure 4-18. PE Overall Tape Format

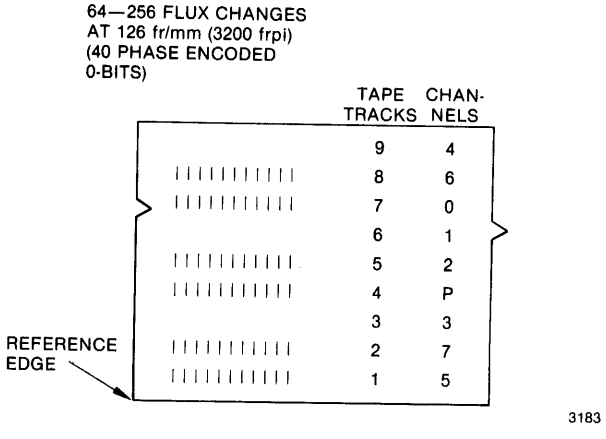


Figure 4-19. PE Tape Mark Format Detail

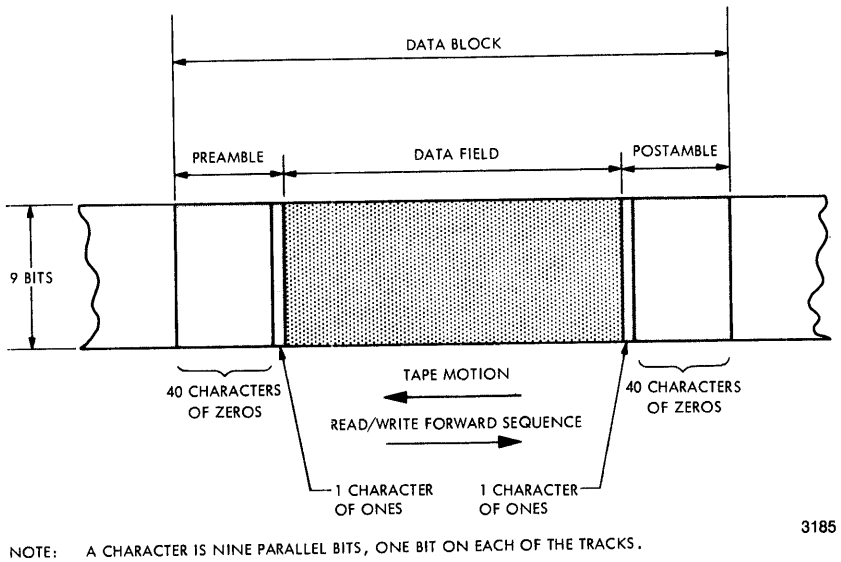


Figure 4-20. PE Data Block Format

Appended to the end of the 1s burst is an ID character consisting of 1s in channels 7, 3, 2, 1, 6, and 4, and erasure in channels 5, P, and 0. This ID character is approximately 50.8 mm (2 inches) long. (At least a contiguous 6.35 mm (0.25 inch) of this length must be error-free in all tracks at once.) There is a normal inter-block gap (IBG) between the ARA ID character and the first data block.

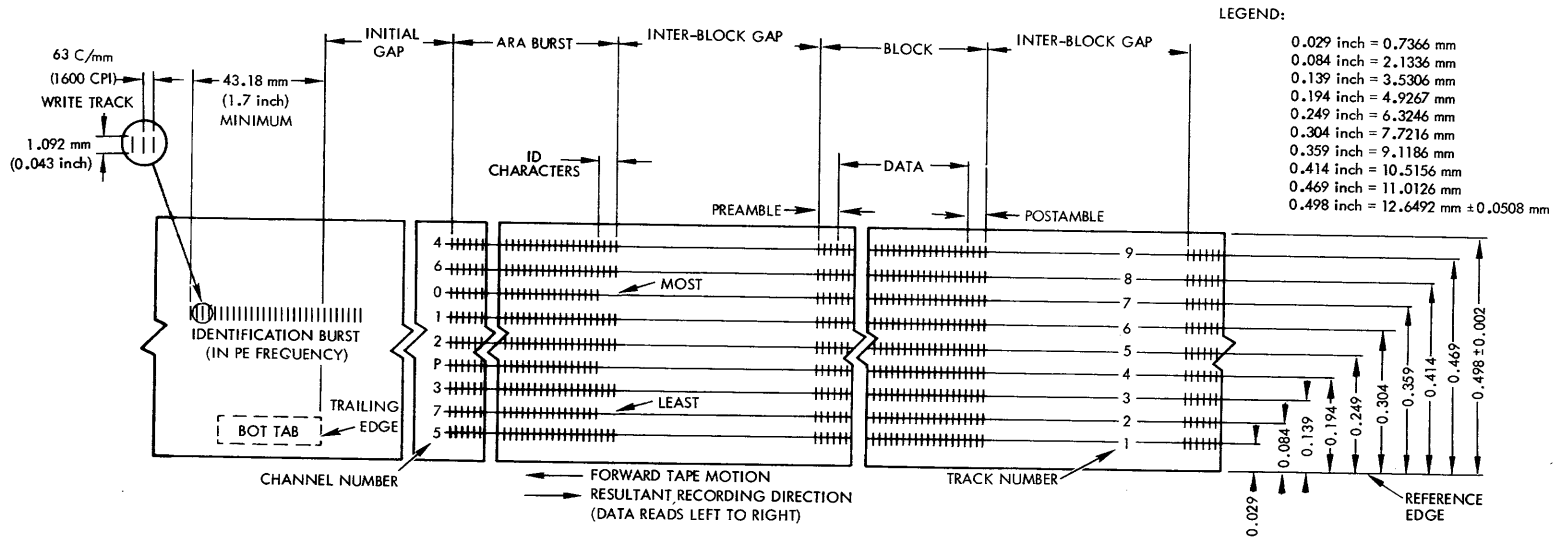
4.5.12.2 GCR Mode Tape Mark Format

Figure 4-22 details the tape mark format used in GCR mode to mark the end of a file. The tape mark is a special block generated in response to the Write Tape Mark GCR command. One or more files may be written on a reel of tape.

The tape mark is specified as 250 to 400 flux changes, all 1s, at 356 fr/mm (9042 frpi) in channels 7, 2, 6, 5, P, and 0, and no recording in channels 3, 1, and 4.

NOTE

The flux reversal rate of 356 fr/mm (9042 frpi) is equal to the number of bit cells per inch per track and also to the number of characters per inch for all tracks. Maximum density used, therefore, is 356 c/mm (9042 cpi). This accommodates data, encoding, error checking, and other overhead requirements. The payload (data) density is 246 c/mm (6250 cpi).



NOTES:

1. TAPE IS SHOWN WITH OXIDE SIDE UP.
2. TAPE TO BE FULLY SATURATED IN THE ERASED DIRECTION IN THE INTER-BLOCK GAP AND THE INITIAL GAP.
3. THE IDENTIFICATION BURST MUST EXTEND PAST THE END OF THE BOT MARKER.
4. THERE IS A TRACK PLACEMENT TOLERANCE OF ±0.0762 mm (±0.003 inch) FOR EACH TRACK.

3179

Figure 4-21. GCR Overall Tape Format

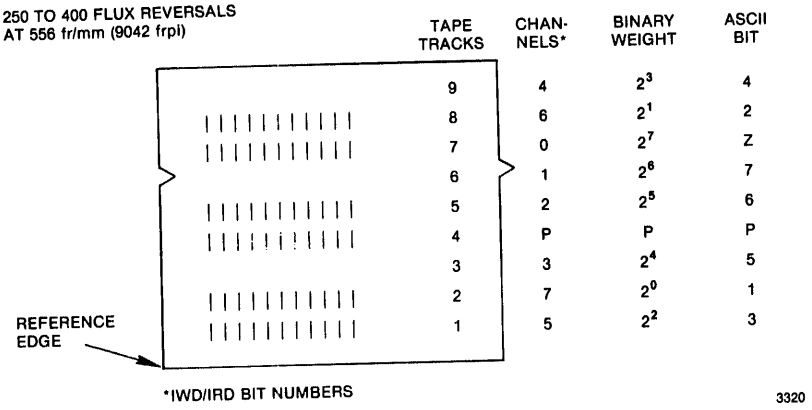


Figure 4-22. GCR Mode Tape Mark Format

4.5.12.3 GCR Mode Data Block Format

Figure 4-23 details the format for the data block. The various elements of the data block are further defined in the following paragraphs.

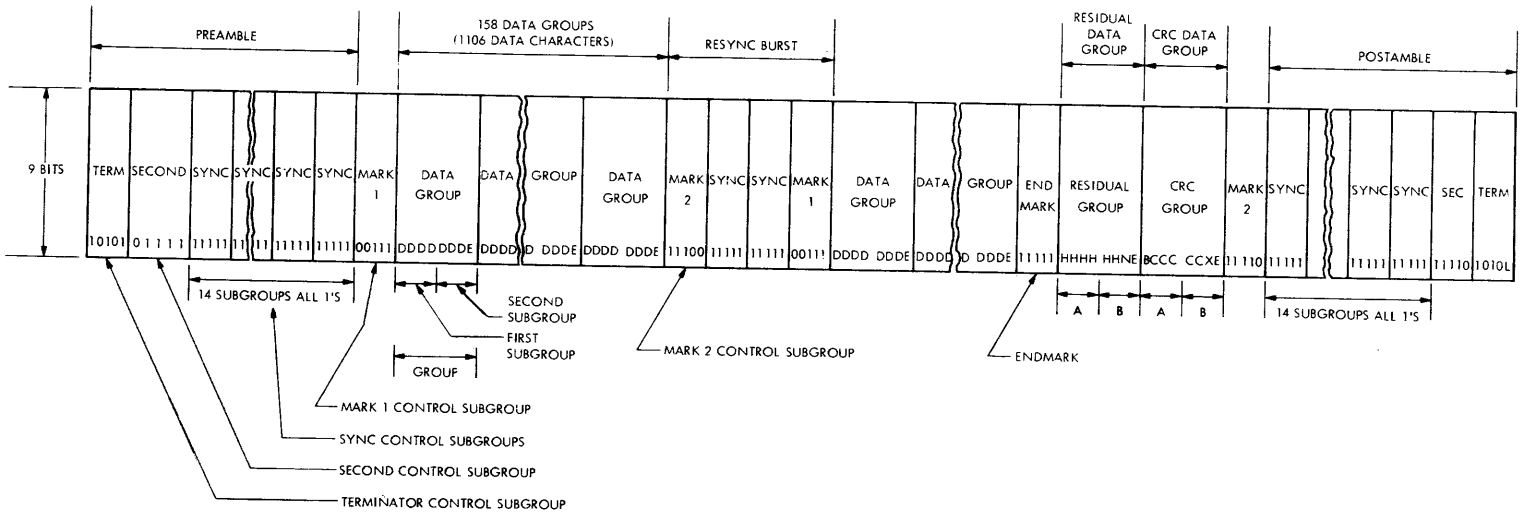
(1) Preamble — Each block of data is preceded by a preamble for synchronization purposes. The preamble, as recorded, consists of 80 characters, divided into sixteen 5-character subgroups: one Terminator Control Subgroup, one Second Control Subgroup, and 14 Sync Control Subgroups.

- The Terminator Control Subgroup (TERM) is one set of nine parallel 5-bit serial values of 10101 in the respective tracks located at the BOT end of each block and 1010L at the EOT end of each block, where L represents even longitudinal parity. The L bit of the last character restores the magnetic remanence to the erase state.
- The Second Control Subgroup is one set of nine parallel 5-bit serial values of 01111 in the respective tracks for the BOT end of the block and 1110 for the EOT end of the block interleaved between the respective terminator control subgroups and the sync control subgroups.
- The Sync Control Subgroup is one set of nine parallel 5-bit serial values, 11111 in the respective tracks. It is used to indicate recorded frequency and phase to allow synchronization of the variable frequency clock (VFC).

(2) Mark 1 Control Subgroup — This subgroup is one set of 5-bit serial values (00111) in each of the nine parallel tracks simultaneously. Mark 1 acts as the boundary between control subgroups and data. When the tape moves in the forward direction, Mark 1 indicates that data will follow.

(3) Data Group — A Data Group is an essential element of group-coded recording. Before encoding it develops as seven data characters plus an error correction code (ECC) character, as shown in Figure 4-23. Each data group is recoded into a storage group of ten characters. In both cases, the group is divided into two subgroups during external processing. The transport receives only the 10-character storage groups.

(4) Resync Burst — After each 158 data groups (1106 data characters as calculated in data-group format), a resync burst consisting of a Mark 2 control subgroup, two Sync Control Subgroups and one Mark 1 subgroup occurs. The Sync Control subgroups are formatted as described in Paragraph (1). The Mark 2 subgroup that ends the 158 data group series is the same as Mark 1, refer to Paragraph (2), except that the 5-bit serial value is 11100. The Mark 1 subgroup that indicates the end of the resync burst is described in Paragraph (2).



NOTE: DATA, RESIDUAL AND GCR GROUPS ARE TRANSLATED FROM 8-BYTE TO 10-BYTE CODES BEFORE THEY ARE SENT TO THE TRANSPORT FOR RECORDING ON TAPE.

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Figure 4-23. GCR Mode Data Block Format

(5) End Mark Control Subgroup — The End Mark is used to indicate the end of a series of complete data groups, and the beginning of the Residual Group. The End Mark is one set of nine parallel 5-bit serial numbers (11111) in each of the tracks.

NOTE

The Residual Data Group (6) and the Cyclic Redundancy Check (CRC) Data Group (7) are defined in Data Group format to assist in understanding GCR recording. These groups are translated into 10-character Storage Groups before reaching the transport. In transport circuits the bit-position elements listed are not distinguishable.

(6) Residual Data Group — The Residual Data Group positions are as follows:

- Group positions 1—6 contain Residuum data characters (remainder of the number of characters divided by 7) or padding (H).
- Group position 7 contains an Auxiliary Cyclic Redundancy Check (ACRC) character (H).
- Group position 8 contains an ECC character (E). The Residuum data characters occupy the lower-numbered positions, with the higher-numbered group positions containing padding characters of all 0s with odd parity. The group positions 1—6 may contain all padding or all data characters in accordance with the number of Residuum characters modulo 7 (remainder after dividing the block data bytes by 7).

(7) Cyclic Redundancy Check (CRC) Data Group — This specially formatted data group contains the CRC character and the residual character. The group positions are as follows:

- Group position 1 contains an all 0s character with odd parity or the CRC character (B).
- Group positions 2—6 each contain the CRC character (C).
- Group position 7 contains the residual character (X), which specifies the number of 7-byte data groups and, separately, the number of 32-byte data groups in the block.
- Group position 8 contains the ECC character (E).

(8) Postamble — The postamble follows the CRC group and a Mark 2 subgroup, which is the same as Mark 1, Paragraph (2), except that the 5-bit serial value is 11100. The postamble consists of 80 characters of which the first 14 subgroups are all 1s in all tracks followed by 11110 and 1010L in all tracks. (The L character is the last character.) The postamble is recorded for the purpose of electronic synchronization in reverse reading mode.

4.5.13 WRITE FUNCTION

The Write function records the formatted digital information on tape and checks the read-after-write data for track amplitude problems. The data format is ANSI and IBM compatible, 9-track GCR or PE, as discussed in Paragraphs 4.5.9—4.5.12. Figure 4-24 is a simplified block diagram of the write function.

Assume power is applied and a reel with a write enable ring is installed on the supply reel. Switch S8, on the Base Assembly, closes and supplies Write Power (WRT PWR) via P21-29 and 32 to the Capstan/Regulator PCBA (J11-69) and to the Write PCBA (J7-24 and 60). If the write enable ring is not installed on the reel, WRT PWR is not applied to the circuitry.

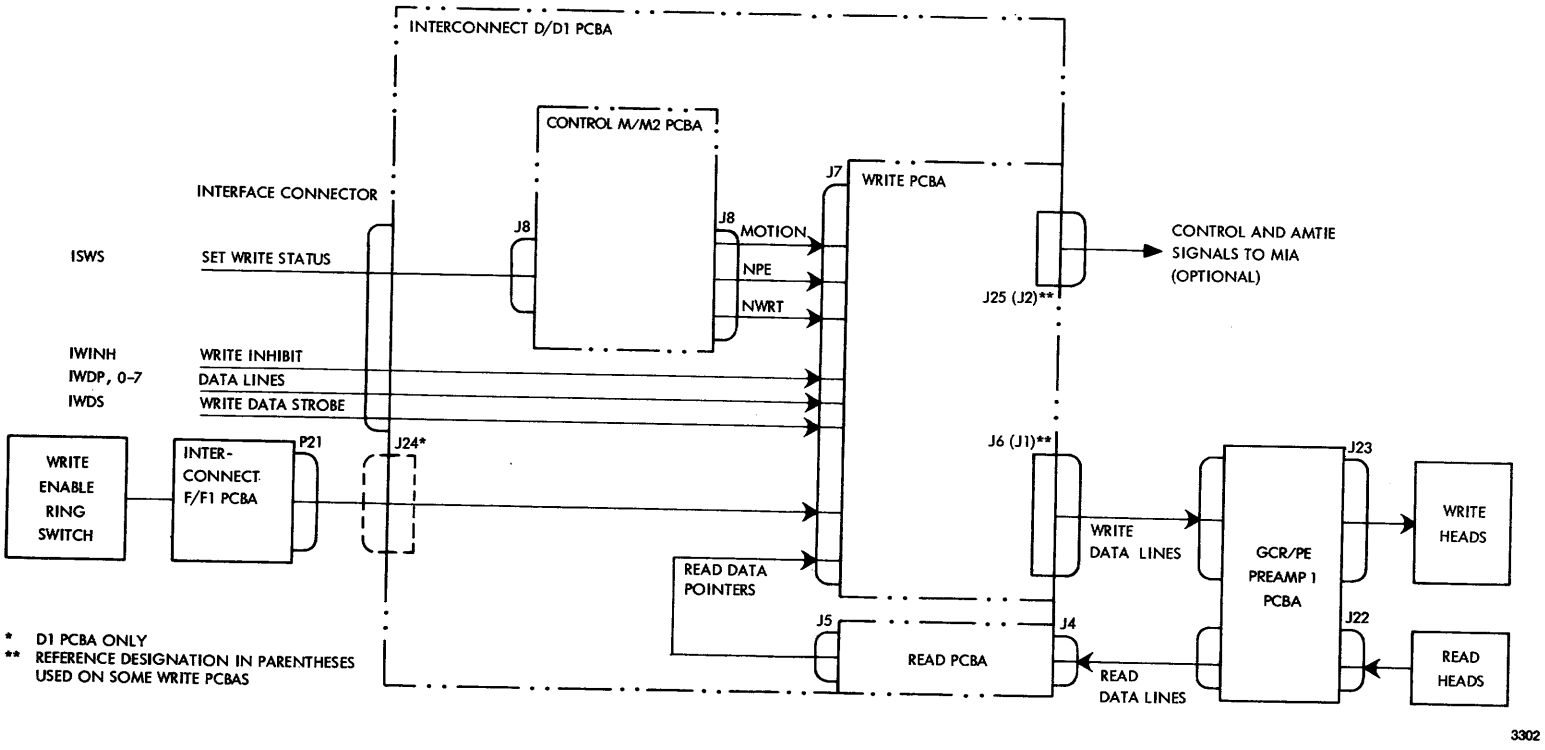

Figure 4-24. Write Functional Block Diagram

The Phase Encoded signal (NPE) from the Control M/M2 PCBA (J8-25) is applied to the Write Control logic on the Write PCBA at P7-61. The density command may be selected from either the front panel or the interface depending on the configuration. NPE is used to elect either PE or GCR format (high = GCR, low = PE).

When a load command is detected, the Air Subsystem provides a low Reel Servo Enable signal (NRSAE) to the Capstan/Regulator PCBA via J8-34.

The WRT PWR signal from S8 (P21-29 and 32) and NRSAE from the Air Subsystem (J8-34) are applied to the Write Driver on the Capstan/Regulator PCBA. The Write Driver provides a low File Protect signal (FPT) to the System Control function via J11-19 and the low holding path Write Lockout Feedback signal (NWLFB) to the WLO Solenoid, K2, via J11-33 and 73. NWLFB is coupled through the Interconnect F/F1 PCBA (P21-27 and 28) and energizes the WLO Solenoid, K2, which closes S8 and maintains WRT PWR. If WRT PWR is not present, the Write Driver provides a high FPT signal to the System Control function (J11-19) and NWLFB to the WLO Solenoid (J11-33 and 73). The NWLFB does not energize the WLO Solenoid and no WRT PWR is available. TP51 (Capstan/Regulator PCBA) is used to monitor the File Protect signal and TP58 (Capstan/Regulator PCBA) is used to monitor the Write Lockout Feedback signal.

If the transport is selected, ready, and on line and the System Control function detects an interface write command and an interface motion command, the System Control function provides a high Motion signal (MOTION) via J8-28 and a low Write signal (NWRT) via J8-26 to J7-26 and J7-25, respectively of the Write Control logic.

The interface input data lines (IWDP, IWD0—IWD7) are routed to the Write Data Buffers via either the edge connectors (J100 series), the 3M connectors (J200 series), or the MIA/Microformatter (J2). The interface also provides the two test signals (NTEST and NTSTR) to the Write Test Inverters (J7-56 and J7-20, respectively) and the Write Data Strobe (IWDS) to the Write Strobe logic via J7-47. Amplitude Track In Error (AMTIE) signals are generated on the Write PCBA from the read-after-write data. The data arrives at the Write PCBA from the Read PCBA as Pointers (POP, PO0—PO7). J25 on the Write PCBA is used to connect the AMTIE signals to the optional MIA.

Refer to Section V for detailed discussion of circuits on the Write PCBA.

4.5.14 READ FUNCTION

The Read function recovers and formats the digital information from magnetic tape in either the forward or reverse direction. The format is ANSI and IBM compatible, 9-track, GCR or PE. Figure 4-25 is a simplified block diagram of the read function.

The Phase Encoded signal (NPE) from the Control M/M2 PCBA (J8-25) is applied to the read control logic on the Read PCBA. The density command may be selected from either the front panel or the interface depending on the configuration. NPE is used to select either PE or GCR format (high = GCR, low = PE).

When the system control function detects a read command and an interface motion command, the Control M/M2 PCBA provides a high Motion signal (MOTION) via J8-28 and a Write signal (NWRT) via J8-26 to the Read PCBA. NWRT is used to select either a read or write operation (high = read, low = write).

Because of the read-after-write feature, the transport reads in both read and write modes, and selection of the read-only function is essentially a suppression of the write mode.

Data retrieved by the read heads are preamplified on the 9TK Preamplifier PCBA and routed directly to J4 on the Read PCBA, where they are processed and presented to the interface in binary form required by the host system or MIA. The read data is also sent to the Write PCBA as Pointers (POP, PO0—PO7) for development of the AMTIE signals.

Refer to Section V for detailed description of the Read PCBA circuits.

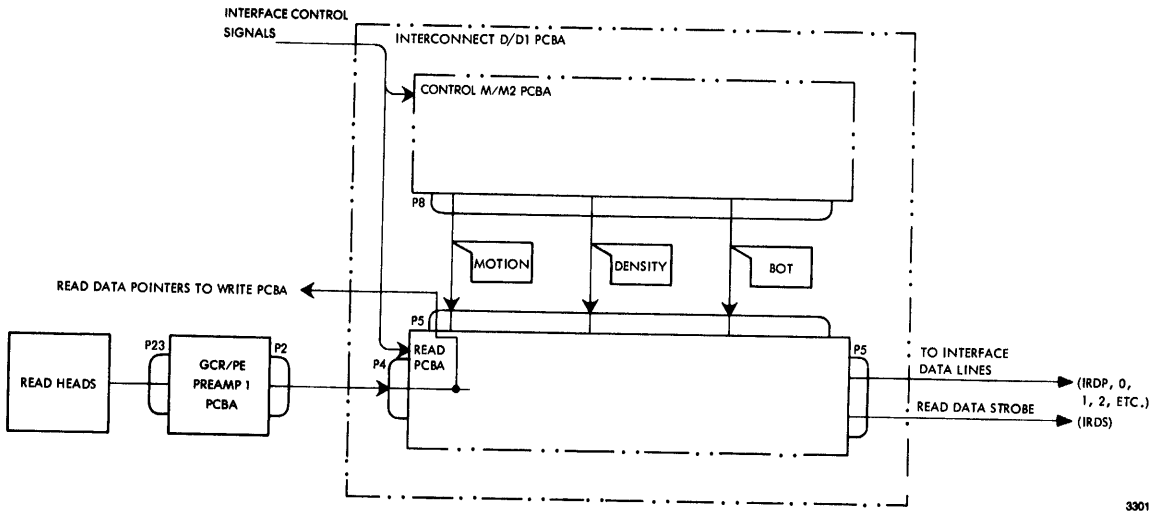

Figure 4-25. Read Functional Block Diagram

SECTION V
PCBA AND CIRCUIT DETAIL THEORY

5.1 GENERAL INFORMATION

This section gives information on the theory of operation of detail circuits, particularly those provided by printed circuit board assemblies (PCBAs). General theory of operation of the overall functional systems is summarized in Section IV.

Pertinent engineering drawings are inserted at the end of this section and are referred to by drawing (schematic) number and zone. The zone reference includes the sheet and coordinate intersection designation (e.g., zone 2-4F) as explained in Figure 4-1.

5.2 INTERNAL INTERCONNECTIONS

Interconnections between various functional PCBAs (Control M, Write, etc.) are provided by the Interconnect D/D1 PCBA, into which the other boards in the card cage are plugged. Refer to Figure 5-1. The conductors on the Interconnect D/D1 PCBA integrate the logic signals, distribute power, and route commands. Conductor connections on the Interconnect D/D1 PCBA are listed in Table 5-1. The few logic interconnections made by cable are illustrated in Figure 2-6. Primary and secondary power circuit cables are covered in Paragraph 5.3.

Interconnect D and D1 PCBAs are interchangeable as are Control M and M2 PCBAs and Interconnect F and F1 PCBAs; however, adjustment and maintenance procedures for F and F1 are different, as covered in Section VI.

5.3 POWER CIRCUITS

The following paragraphs describe in detail the power supply and distribution circuits for a typical T1940 transport operating on 230v 60 Hz power. Details are similar for all systems in the series, but the user should refer to the appropriate drawings for specific equipment, using the following information as a general guide.

For equipment using voltages and frequencies other than 230v 60 Hz, it must be determined that the input receptacle is properly connected to the primary winding taps. Various connections are listed in Table 2-3 and further detailed in the following paragraphs. For clarification, the subject matter is divided into the following topics.

(1) Primary Power Connection and Controls

(2) Blower/Compressor Motor Power

(3) Unregulated DC Power Supplies

(4) DC Power Regulation and Distribution

WARNING

DANGEROUS VOLTAGES ARE PRESENT. ONLY EXPERIENCED TECHNICIANS ARE QUALIFIED TO WORK ON INTERNAL CIRCUITS OF THE TRANSPORT. BEFORE WORKING ON POWER PACK CIRCUITS, DISCONNECT INPUT POWER AND WAIT 5 MINUTES FOR CAPACITORS TO DISCHARGE.

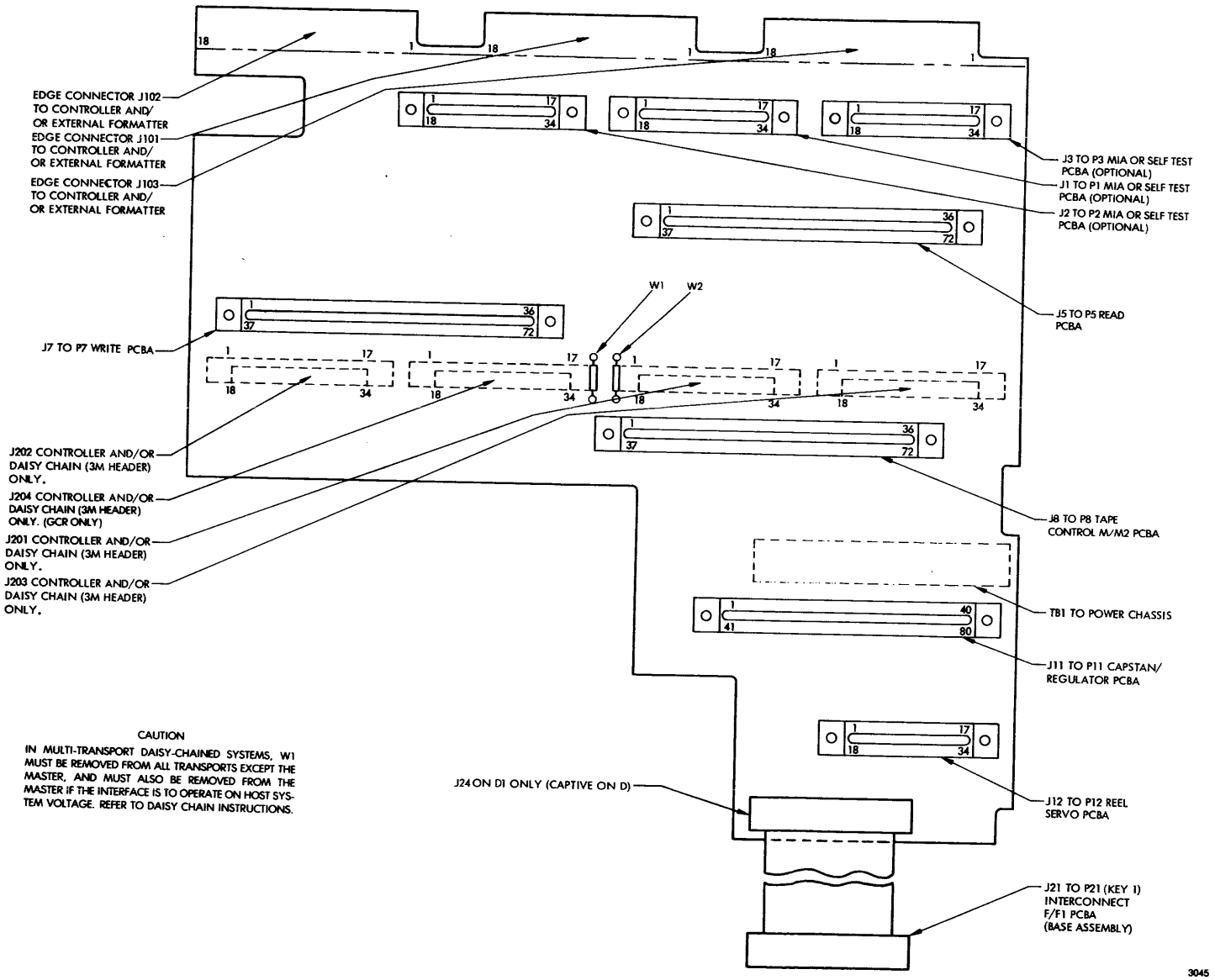

Figure 5-1. Interconnect D/D1 PCBA

Table 5-1
Interconnect D/D1 PCBA Conductor Connections

A. POWER DISTRIBUTION

LEVEL/ SIGNAL	TERMINATION			
	FROM	TO	TO	TO
+12VDC +24VDC −24VDC	A2TB1-6 A2TB1-7 A2TB1-8	J11-15,55 J11-16,56 J11-20,60	P21-22,23,24*	J24-27,28,29*
+36V(C) DC COM 2 −36V(C)	A2TB1-1 A2TB1-4 A2TB1-5	J11-1,2,41,42 J11-9,10,11,49,50,51 J11-12,13,52,53		
DC COM 1 8.5VAC CM(+)	A2TB1-9 A2TB1-10 A2TB1-3	J11-26,27,66,67 J11-40 J11-6,7,8,46,47,48		
CM(−)	A2TB1-2	J11-3,4,5,43,44,45		
0V(L)	J11-26,27,66,77	P21-11,12,14* J24-37,39,40* J8-22,58	J5-3,4,39,40 J12-4,5,21,22	J7-15,16,17,51,52,53
0V(I)	J11-26,27,66,77	J1-23 thru 34 J5-26 thru 36,38 J101-2 thru 14,16,17	J2-2 thru 17 J7-1 thru 10 J102-1 thru 18	J3-2 thru 10, 14 thru 17 J8-38 J103-A,B,C,D,J thru V
		J201-20 thru 34 J204-2 thru 17	J202-2 thru 17	J203-2 thru 10, 14 thru 17
+5V(L)	J11-22,23,62,63	P21-2,4* J24-47,49* J5-8,9,44,45 J12-1,2,18,19	J1-18 J7-18,19,54,55 J101-S	J3-11,12,13,28,29,30 J8-21,57 W1-1
+5V(I)	J203-11,12,13,28,29,30	J201-18	W2-1	
+5V(T)**	W1-2,W2-2	J5-7,43 J204-1,18	J7-21,57	J8-37
+15V	J11-21,61	J5-5,41 J12-6,23	J7-22,58 P21-39*	J8-56 J24-12*
−15V	J11-14,54	J5-6,42 J12-7,24	J7-23,59 P21-33,36*	J8-55 J24-15,18*

*On Interconnect D1 PCBAs only, J24 connector is provided for the ribbon cable terminated by P21, that plugs into J21 on Interconnect F/F1 PCBA.

**The I/O line terminator voltage (+5v(T)) is supplied by the transport (+5v(L)) if jumper W1 is installed, or by the host system (+5v(I)) if jumper W2 is installed. In multiple transport systems, W1 must be removed from all except the first transport. Refer to Section II for daisy-chain instructions.

Table 5-1
Interconnect D/D1 PCBA Conductor Connections (Continued)

B. DECK INTERFACE RIBBON TO INTERCONNECT PCBA

LEVEL/ SIGNAL	TERMINATION				
	FROM	TO	TO	TO	TO
TACH TACH COM SPARE 2	P21-44 P21-46 P21-49	J24-7 J24-5 J24-2	J8-53 J8-54	 J11-68	
S.POS T.POS 0V(R)	P21-37 P21-21 P21-19	J24-14 J24-30 J24-32			J12-20 J12-3 J12-34
SPARE S.LIMIT T.LIMIT	P21-1 P21-6 P21-10	J24-50 J24-45 J24-41	 J8-1 J8-2		 J12-30 J12-31
CR N.O. NEOT TIP	P21-8 P21-50 P21-45	J24-43 J24-1 J24-6	 J8-50 J8-49	J11-80	
NBOT PKSN NSMR	P21-42 P21-30 P21-3	J24-9 J24-21 J24-48	J8-52 J8-42 J8-8		
CART N.O. CO CC	P21-43 P21-41 P21-40	J24-8 J24-10 J24-11	 J8-10 J8-11	J11-79	
CART M + CART M – C.SOL.RET	P21-31,34 P21-25,26 P21-17,20	J24-20,17 J24-25,26 J24-31,34		J11-30,70 J11-31,71 J11-34,74	
SPARE 1 VAC VAC.SOL.RET.	P21-5,7 P21-48 P21-15,18	J24-44,46 J24-3 J24-33,36	 J8-3	J11-36,76 J11-32,72	
WP2 WP1 W.P.SOL.RET.	P21-35,38 P21-29,32 P21-27,28	J24-13,16 J24-19,22 J24-23,24		 J11-69 J11-33,73	 J7-60,24
P.SOL.RET. ABPNO TOR	P21-13,16 P21-9 P21-47	J24-33,38 J24-42 J24-4	 J8-4 J8-9	J11-35,75	

*On Interconnect D1 PCBAs only, J24 connector is provided for the ribbon cable terminated by P21, that plugs into J21 on Interconnect F/F1 PCBA.

Table 5-1

Interconnect D/D1 PCBA Conductor Connections (Continued)

C. INTERNAL CONTROL

LEVEL/ SIGNAL	TERMINATION					
	FROM	TO	TO	TO	TO	TO
NSLTA NHID NWRT	J8-23 J8-25 J8-26	J5-46 J5-10 J5-47	J7-61 J7-25			J103-7
9TK MOTION FPT	J8-27 J8-28 J8-60	J5-11 J5-48	J7-62 J7-26	J11-19		
BOT NMOT SRF	J8-48 J8-51 J8-29	J5-12		J11-24	J12-17	
SRR TRF TRR	J8-30 J8-31 J8-32				J12-16 J12-15 J12-14	
MRL REWR REV	J8-5 J8-66		J7-63	J11-78 J11-18	J12-28 J12-13 J12-33	
NDRV N□80% NTAP2	J8-65 J8-67 J8-62			J11-64 J11-25 J11-57	J12-27	
NTEN NINTLK NRWR	J8-63 J8-69 J8-33			J11-17 J11-65 J11-38	J12-8,25	
NRSAE NCCC NCOC	J8-34 J8-70 J8-71			J11-58 J11-29 J11-28	J12-11	
NXFR NTP	J8-72 J8-64			J11-39 J11-59		
NPORST	J11-37,77	J1-1 J12-9,26	J7-11 J201-1*	J8-61		
PNU RET	J8-68	A2TB1-11				

*Connection deleted on P/N 107298-02 Interconnect D1 PCBAs.

Table 5-1
Interconnect D/D1 PCBA Conductor Connections (Continued)

D. INTERFACE CONTROL SIGNALS

LEVEL/ SIGNAL	TERMINATION			
	FROM	TO	TO	TO
ISFC IODS ISRC	J101-C J101-D J101-E	J1-14 J1-13 J1-12	J201-14 J201-13 J201-12	J8-20 J8-19 J8-18
IDDI IRWC ISLT0	J101-F J101-H J101-J	J1-11 J1-10 J1-9	J201-11 J201-10 J201-9	J8-17 J8-16 J8-15
ISWS IRWU IONL	J101-K J101-L J101-M	J1-8 J1-7 J1-6	J201-8 J201-7 J201-6	J8-14 J8-13 J8-12
IRWD IFPT ILDP	J101-N J101-P J101-R	J1-5 J1-4 J1-3	J201-5 J201-4 J201-3	J8-47 J8-46 J8-45
IRDY IEOT	J101-T J101-U	J1-19 J1-2	J201-19 J201-2	J8-7 J8-44

E. INTERFACE READ SIGNALS

LEVEL/ SIGNAL	TERMINATION				
	FROM	TO	TO	TO	TO
IRDP IRDS IRD0	J103-1 J103-2 J103-3	J3-34 J3-33 J3-32	J5-72 J5-71 J5-70	J203-34 J203-33 J203-32	
IRD1 IRD2 IRD3	J103-4 J103-8 J103-9	J3-31 J3-27 J3-26	J5-69 J5-68 J5-67	J203-31 J203-27 J203-26	
INRZ I7TK ISGL	J103-10 J103-11 J103-12	J3-25 J3-24 J3-23	J5-66 J5-65 J5-64	J203-25 J203-24 J203-23	
ISPEED IRD4 IRD5	J103-13 J103-14 J103-15	J3-22 J3-21 J3-20	J5-63 J5-62 J5-61	J203-22 J203-21 J203-20	
IRD6 IRD7 NSEL	J103-17 J103-18	J3-18 J3-1	J5-59 J5-58 J5-22	J203-18 J203-1	J1-20

Table 5-1

Interconnect D/D1 PCBA Conductor Connections (Continued)

F. INTERFACE WRITE SIGNALS

LEVEL/ SIGNAL	TERMINATION								
	FROM	TO	TO	TO	TO	TO	TO	TO	TO
IWDS ISLT1 IWARS	J102-A J102-B J102-C	J101-A J101-15	J2-34 J2-33 J2-32	J1-16	J7-47 J7-46	J202-34 J202-33 J202-32	J201-16	J8-39	
ISLT2 IRTH1 IRTH2	J102-D J102-E J102-F	J101-18	J2-31 J2-30 J2-29			J202-31 J202-30 J202-29		J8-40	J5-2 J5-1
ISLT3 IWDP IWD0	J102-H J102-L J102-M	J101-V	J2-28 J2-25 J2-24		J7-45 J7-44	J202-28 J202-25 J202-24		J8-41	
IWD1 IWD2 IWD4	J102-N J102-P J102-R		J2-23 J2-22 J2-21		J7-43 J7-42 J7-41	J202-23 J202-22 J202-21			
IWD3 IWD5 IWD6	J102-S J102-T J102-U		J2-20 J2-19 J2-18		J7-40 J7-39 J7-38	J202-20 J202-19 J202-18			
IWD7 ITACH	J102-V J102-K		J2-1 J2-26		J7-37	J201-1 J202-26		J8-6	

G. SELF-TEST

LEVEL/ SIGNAL	TERMINATION				
	FROM	TO	TO	TO	TO
NTEST	J3-22	J5-60	J7-56	J8-36	J103-6
NTSFC	J103-H			J8-24	
NTSRC	J103-F			J8-35	
NTRWC	J103-E			J8-59	
NTSTR	J3-19		J7-20		J103-16
NTWRT	J102-J			J8-43	
NTSKEW	J1-21	J5-37			J103-5

Table 5-1
Interconnect D/D1 PCBA Conductor Connections (Continued)

H. READ-DESKEW/GCR READ

LEVEL/ SIGNAL	TERMINATION		
	FROM	TO	TO
—/A1 CHP/NA DCHP/A2	 J5-49 J5-13	J7-27 J7-64 J7-28	J204-25* J204-26*
CH0/NA2 DCH0/A3 CH1/NA3	J5-50 J5-14 J5-51	J7-65 J7-29 J7-66	J204-27*
DCH1/A4 CH1/NA4 DCH2/A5	J5-15 J5-52 J5-16	J7-30 J7-67 J7-31	J204-28* J204-29*
CH3/NA5 DCH3/NARA CH4/NA6	J5-53 J5-17 J5-54	J7-68 J7-32 J7-69	J204-30*
DCH4/A6 CH5/NA7 DCH5/A7	J5-18 J5-55 J5-19	J7-33 J7-70 J7-34	J204-31* J204-32*
CH6/NA8 DCH6/A8 CH7/NA9	J5-56 J5-20 J5-57	J7-71 J7-35 J7-72	J204-33*
DCH7/A9 SPARE SPARE	J5-21 J5-23	J7-36 J7-12 J7-48	J204-34*
SPARE SPARE SPARE	J5-24 J5-25	J7-14 J7-50 J7-49	 J204-20*

*J204 connections listed here are not used on all models.

5.3.1 PRIMARY POWER CONNECTIONS AND CONTROLS

The transport derives all required power from a single ac input. The input voltage is optional between 220 and 250v ac, in 10v increments, but the input must correspond to the connections between power circuitbreaker CB1 and the primary winding taps of the transformer. These taps are available at power supply terminal board A1TB1. Refer to Figure 5-2. The transport can also be prepared for either 50 or 60 Hz power. These require different blower/compressor motor pulleys and different drive belts.

Figure 5-2 shows that the ac power input is available to the transport when circuitbreaker CB1 is closed, but power is not applied to the primary winding of T1 until the front panel POWER switch S1 is closed. Closing S1 causes solid state switch S2 to close the ac line between terminal board A1TB1-1 and -3.

CAUTION

DO NOT CONNECT THE TRANSPORT TO A POWER SOURCE WITHOUT FIRST VERIFYING THAT THE TRANSFORMER IS PROPERLY WIRED FOR THE INTENDED INPUT VOLTAGE. (REFER TO FIGURE 5-2.)

5.3.2 BLOWER/COMPRESSOR MOTOR POWER

The Blower/Compressor AC Motor operates directly on the ac input as shown in Figure 5-3. It is turned on automatically when solid-state switch S3 closes the circuit between A1TB1-1 and -2. Switch S3 is controlled by +12v dc at S3-3 and a low (0v dc) pneumatic return PNU RET at S3-4. The +12v dc is supplied by rectifier CR3 when the secondary winding of transformer T1 is energized. S3-4 goes low during load operation and stays low unless interlock is lost or air or vacuum pressure is inadequate. The motor has an internal thermal switch, that interrupts power to the motor windings during periods of over-temperature conditions. The switch contacts close whenever motor temperature returns to normal.

WARNING

THE MOTOR WILL RESTART WHEN THE OVERTEMPERATURE CONDITION CEASES TO EXIST. ALWAYS TURN OFF OR DISCONNECT AC POWER BEFORE WORKING NEAR MOTOR PULLEYS AND BELTS.

5.3.3 ELAPSED-TIME METER (OPTIONAL) POWER

The optional Elapsed-Time Meter (ETM1) is connected as shown in Figure 5-3. The hot line is connected to the appropriate post on terminal board A1TB1, depending on the voltage rating of the meter. The return line is connected to A1TB1-2, which is connected through S3 to CB1. Control of ETM1 is the same as for the blower/compressor motor. Refer to Paragraph 5.3.2.

5.3.4 AC POWER

AC power is used in the transport to operate the blower/compressor drive motor and the optional elapsed time meter, to initiate the power-on reset process (NPORST, etc.) and to protect the circuits from capacitance discharge at shutdown. Refer to Paragraph 5.3.8. The voltage applied to the motor and the meter depend upon the rating of the selected hardware.

The power-on reset requirement is 8.5v ac derived directly from the secondary winding of transformer T1. The connection to the secondary tap is made physically at the input to rectifier CR2, which is connected to A2TB1-10. A2TB1 is located at the rear of the card cage and provides direct inputs to the vertically mounted Interconnect D/D1 PCBA it is

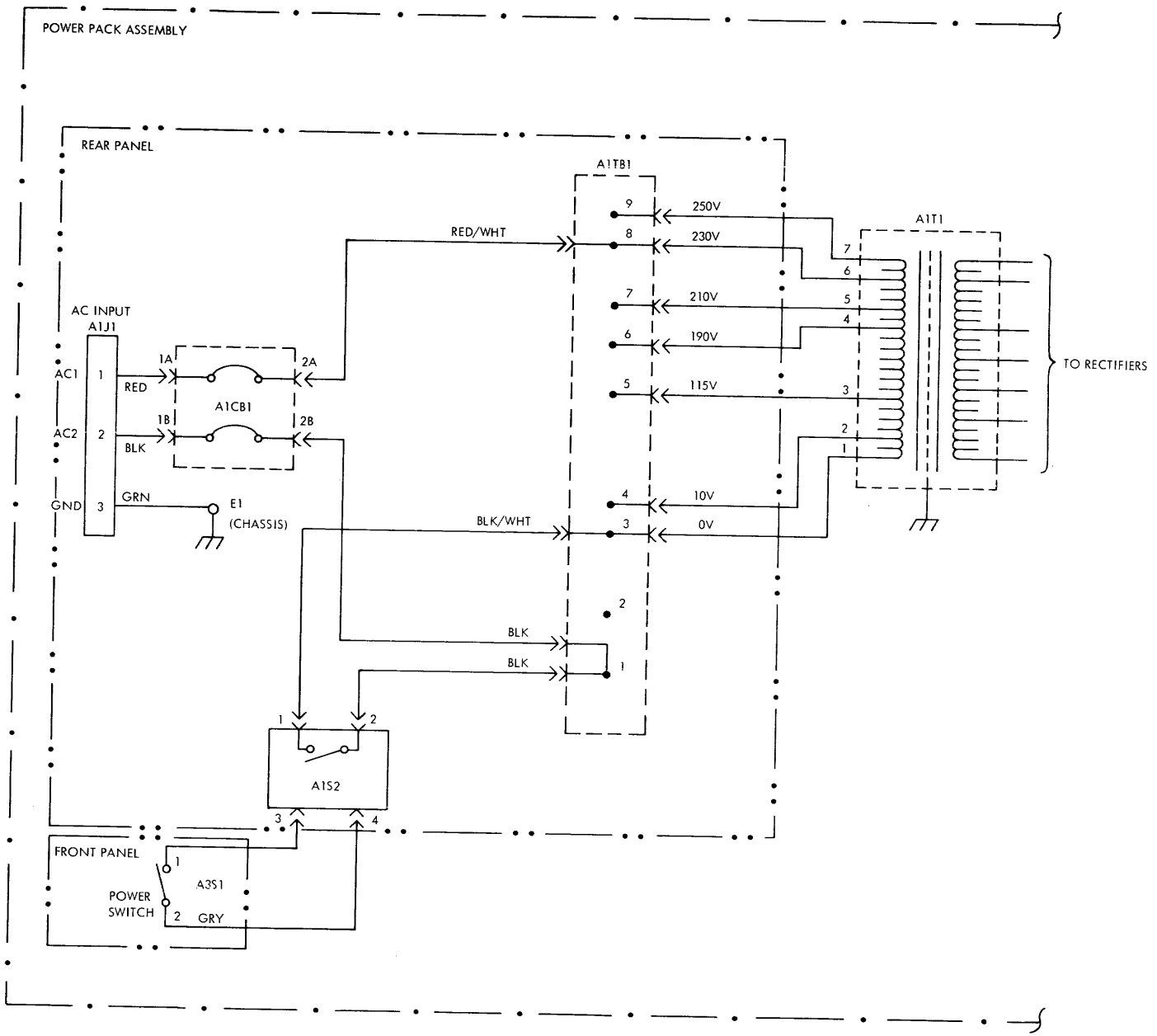

Figure 5-2. Primary Power Hookup and Control

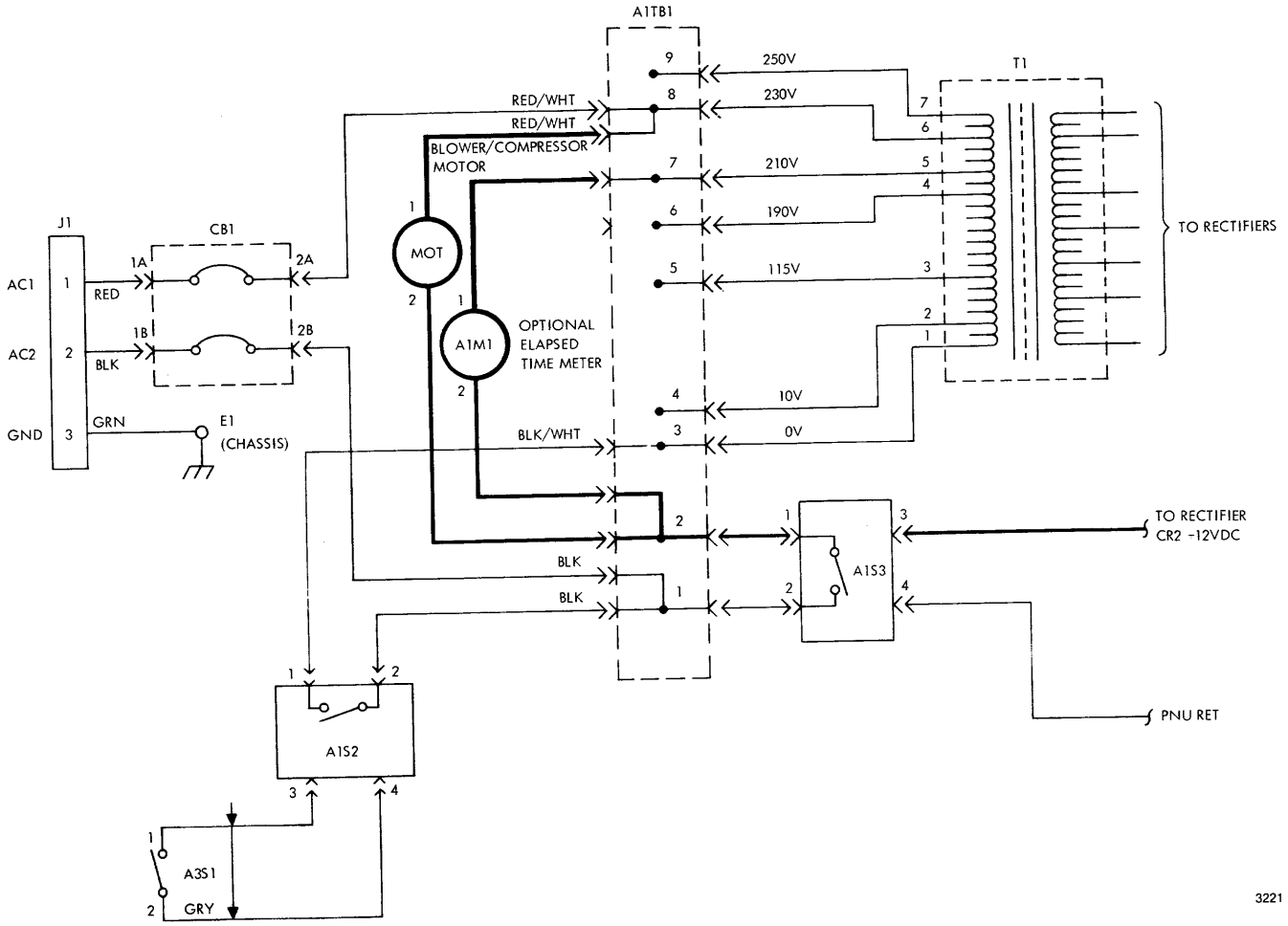

Figure 5-3. Blower/Compressor Motor Power and Control

attached to. The 8.5v ac is delivered to pin 40 of J11 for use in the Capstan/Regulator PCBA for generating the power-on reset command (NPORST).

5.3.5 UNREGULATED DC POWER SUPPLIES

Power for the dc circuits is derived from various taps of the secondary winding of transformer T1, as shown in Figure 5-4. The + 12v dc, ± 24v dc, and ± 36v dc unregulated voltages are rectified by CR1, CR2, and CR3.

Actual rectifier outputs are as follows:

Nominal	Rectifier Output
+ 12	9.0 to 11.0v dc at 10 amps, 2v peak-to-peak maximum ripple at 10 amps
+ 24	21.5 to 24.5v dc at 5 amps, 2v peak-to-peak maximum ripple at 5 amps
− 24	− 21.5 to − 24.5v dc at 5 amps, 2v peak-to-peak maximum ripple at 5 amps
+ 36	33.0 to 37.0v dc at 15 amps, 43v dc maximum at no load, 2v peak-to-peak maximum ripple at 15 amps
− 36	− 33.0 to 37.0v dc at 15 amps, − 43v dc maximum at no load, 2v peak-to-peak maximum ripple at 15 amps

Rectifier outputs are routed through the respective fuses to terminal A2TB1, attached to the rear of Interconnect D/D1 PCBA, as shown in Figure 5-4. They are connected through Interconnect D/D1 PCBA conductors to the Capstan/Regulator PCBA for regulation and further distribution, except that the PNU RET line is routed to the Control M/M2 PCBA.

Supply reel and takeup reel + 36v dc unregulated power is routed directly from the respective fuse to the Reel Servo PCBA, without going through the Interconnect D/D1 PCBA. Similarly, − 36v dc unregulated power reel lines go directly to − 36v dc at the capacitor.

All dc return lines terminate at the dc common bus, mounted on the top of the capacitors. The bus is connected to the center tap of the T1 secondary winding.

5.3.6 DC POWER REGULATION

The 12 and 24v dc unregulated power outputs are later regulated to provide the required + 5, ± 15, and + 5/ − 6v dc power (refer to Figure 5-5) as follows.

5.3.6.1 + 5v dc

The + 12v dc unregulated voltage is received by the + 5v regulator on the Casptan/Regulator PCBA dc. The + 5v regulator uses a Type LM305-IC to control the series power transistor and has a full load capacity of 8 amps. TP11 (on Capstan/Regulator PCBA) is used to monitor the regulated + 5v dc output.

The + 5v is used primarily in the logic and lamp drive circuitry. Current is limited in the + 5v supply by means of current foldback techniques, thus providing over-current protection.

Overvoltage protection is provided on the + 5v lines. A voltage over 6.2v fires an SCR and crowbars the output voltage to zero. Primary power must be removed for a short period of time in order to reset the crowbar circuitry.

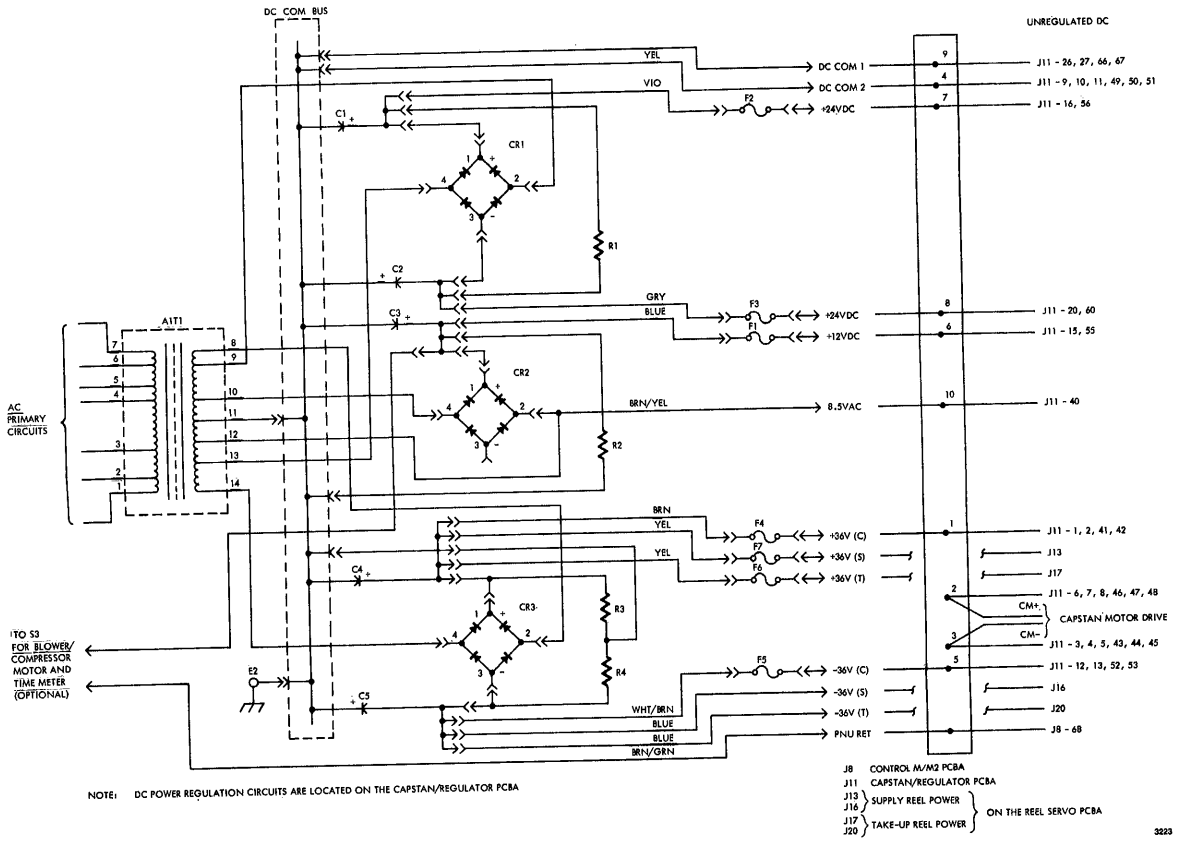

Figure 5-4. Unregulated Power Distribution Circuits

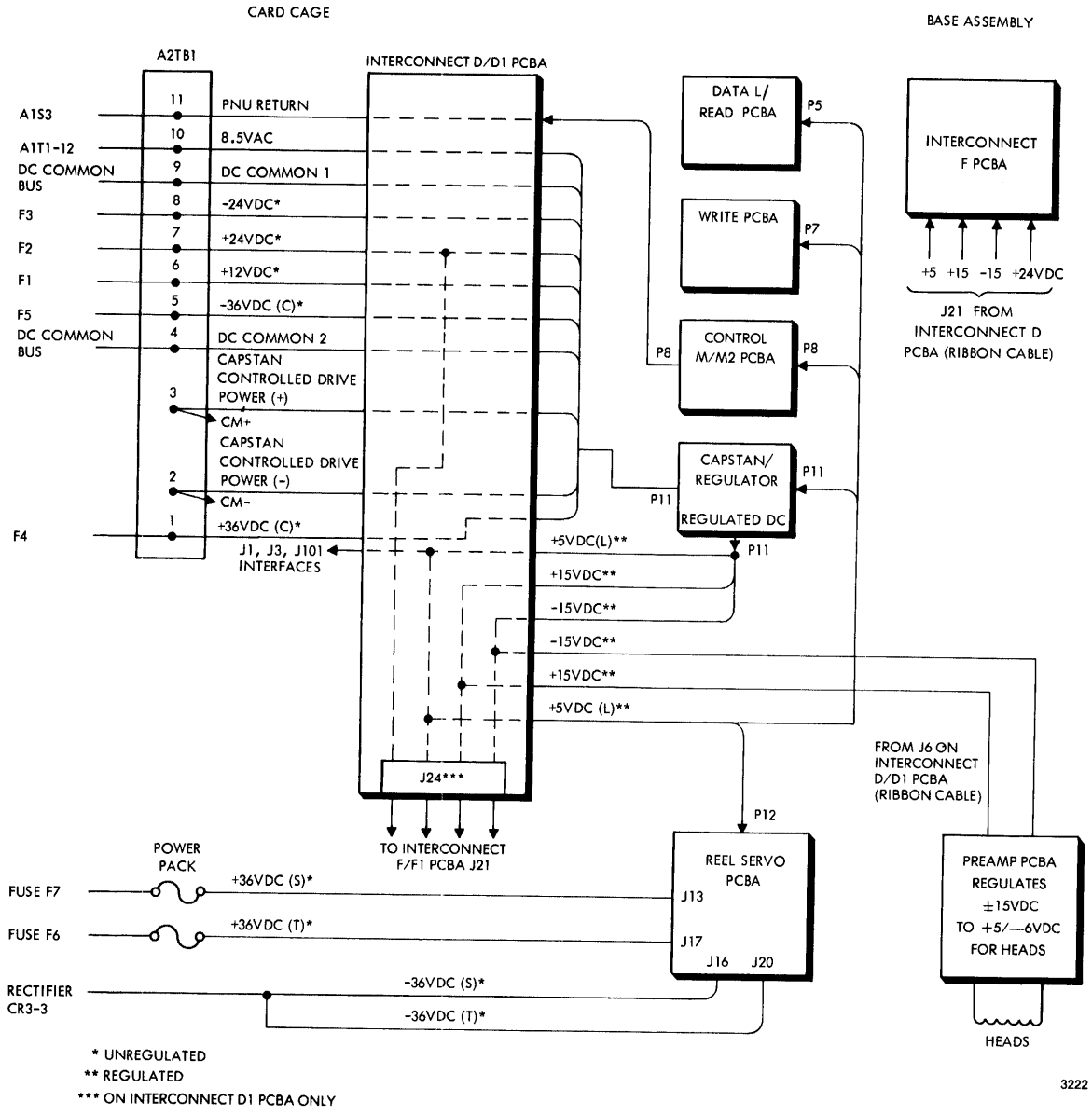

Figure 5-5. DC Power Regulation and Distribution

Separate 5v regulation is provided on the Reel Servo PCBA for its internal logic, + 5v dc (L), and amplifier, + 5v dc (A), circuits.

Interface driver and receiver 5v dc nominal voltage levels are made compatible with the host system by means of jumpers W1 or W2 on the Interconnect D/D1 PCBA.

W1 is used to electrically connect the internal + 5v (L) power at J11-22, 23, 62, and 63 to the interface terminator circuits available at J5-7, 43; J7-21, 57; J8-37; J204-1, 18. If the host system logic level is required, W1 is disconnected and W2 is installed to electrically connect the host system's interface level, + 5v (I), which is available at J201-18 and J203-11, 12, 13, 28, 29, and 30 to J5-7, 43; J7-21, 57; J8-37; J204-1, 18. The level at the latter pins (J5-7, etc.) is the level applied at the driver and receiver terminators. Terminator voltage is identified as + 5 (T), and can be the same level as either + 5 (L) or + 5 (I), depending on whether W1 or W2 jumper is installed.

5.3.6.2 ± 15v dc

The ± 24v dc unregulated voltage is received by the ± 15v regulator on the Capstan/Regulator PCBA and converted into ± 15v dc. The ± 15v regulator uses a Type LM325 IC to control the series power transistors and has a full load capacity of 2.5 amps. TP15 is used to monitor regulated + 15v dc output and TP18 to monitor regulated − 15v dc.

5.3.6.3 + 5/ − 6v dc

The + 5v and − 6v dc used in the head circuitry are derived from the + 15v and − 15v dc by voltage regulators U13 and U14 on the GCR/PE Preamp 1 PCBA, which is mounted on the rear of the transport drive base assembly behind the read/write head area.

5.3.6.4 ± 36v dc (C)

Unregulated + 36v dc (C) for the capstan motor is connected from fuse F4 to A2TB1, on the Interconnect D/D1 PCBA, through the PCBA conductors to J11 and the Capstan/Regulator PCBA. Unregulated − 36v dc (C) is routed similarly from fuse F5.

NOTE

A2TB1-2 and -3 serve as connecting points for controlled capstan motor drive power (− and +, respectively). These are part of the capstan circuits and are not part of the power distribution system.

5.3.6.5 ± 36v dc (S)

Unregulated + 36v dc (S) for the supply reel motor is connected from fuse F7 directly to J13 on the Reel Servo PCBA, without using Interconnect D/D1 PCBA circuits. Unregulated − 36v dc (S) is connected from rectifier CR3-3, without fusing, to J16 on the Reel Servo PCBA.

5.3.6.6 ± 36v dc (T)

Unregulated + 36v dc (T) for the takeup reel motor is connected directly from fuse F6 to J17 on the Reel Servo PCBA. Unregulated − 36v dc (S) is connected from CR3-3, without fusing, directly to J20 on the Reel Servo PCBA.

5.3.7 REGULATED POWER DISTRIBUTION

All 5v dc and 15v dc power is regulated on the Casptan/Regulator PCBA and is distributed to other boards via J11 and conductors on the Interconnect D/D1 PCBA, the internal connections of which are listed in Table 5-1. Regulated power distribution is illustrated in Figure 5-5.

The Reel Servo PCBA contains voltage regulators for + 5v dc (L) and + 5v dc (A) used in the logic and amplifier circuits, respectively, on the same board. Similarly, the 6.8v dc used by the read, write, and erase heads is regulated internally on the 9TK Preamp PCBA.

5.3.8 POWER RESET (NPORST), ENABLE (ENBL, NENBLE), AND MASTER RESET PULSE (NMRSTP) GENERATION

Restoring power, after an interruption, initiates pulses that reset or preset various flip-flops, etc., preparatory to starting operation. The following unregulated power at inputs to the Capstan/Regulator PCBA are involved:

+ 24v dc input at P11-16, 56

– 24v dc input at P11-20, 60

+ 12v dc input at P11-15, 55

8.5v ac input at P11-40

Figure 5-5 shows the source of the power, and Schematic No. 104757 shows the circuits on the Capstan/Regulator PCBA that develop the resetting pulses and enabling conditions. The + 24v dc and – 24v dc inputs are regulated to + 15v dc and – 15v dc, respectively, by LM235N (U1) and transistors Q32 and Q35 (zones 3-8E,F).

Resistors R114 and R121 (zone 3-7E,F) provide for dividing the difference between + 15v dc and – 15v dc at approximately the – 5v dc level. This level is regulated by VR4 (zone 3-6E), inverted to nominal + 5v dc at U11-11 (zone 3-5H), and applied to adjacent U11-4. Similarly, resistors R115 and R122 (zones 3-7E,F) provide a + 5v dc level, that is connected directly at U11-5 (zone 3-5H). When + 15v dc and – 15v dc supplies are functioning, U11-6 is high, turning on Q29 (zone 3-4G) and delivering a high through diode CR7 and the 3.9v voltage regulator VR2 to Q31 (zone 3-3G). Q31 conducts, dropping Q30 base input to 0v. This turns Q30 off, applying a high to Q55 and a low to Q56. Q56 is turned off and Q55 conducts sending a high = false NPORST through P11-37, 77 and to the base of Q51. Q51 conducts turning on Q50 and Q52 making the enable (ENBL) signal low = false. The preceding conditions are valid, when power is applied, after a brief delay. The delay provides the low = true NPORST and high = true ENBL pulses. After the duration of the pulses, the previously described false conditions will be sustained as long as the 8.5v ac, entering at P11-40 (zone 3-10E), maintains a charge in the C20 network (zone 3-5G, 3-4G) between diodes CR8 and CR9. When power is disconnected, the 8.5v ac is disconnected, allowing the input to VR2 (zone 3-4G) to bleed through CR9 and R110, disabling the above circuits. The 8.5v ac feature protects the circuits from damage by rapid discharge of the power pack capacitors whenever power is switched off or disconnected.

Since Q29, CR6, and R99 (zone 3-4G) are connected to the + 12v dc supply (after regulation to + 5v by LM305 (U2) in zone 3-8G), all of the outputs of the power pack except ± 36v dc contribute to the reset/enable (NPORST/ENBL) network. These supplies must be in operating order to provide the appropriate reset/enable signals. This signal availability effectively checks the supplies before operation of the transport ENBL is used on the Capstan/Regulator PCBA to enable the cartridge motor drive circuits (zone 3-8C).

NPORST, gated with NINTLK (zone 2-8H) to produce the capstan enable signal is delivered through J11-37 and J11-77, via the Interconnect D/D1 PCBA to the Write PCBA (J7-11), Control M/M2 PCBA (J8-1), Reel Servo PCBA (J12-9,26) external interface connector (J201-1), and microformatter connector (J1-1). NPORST is used to reset and enable various circuits as required after a power interruption. The Master Reset pulse (NMRSTP) is initiated by either NPORST or the manual RESET switch output, as applied to P8-61 or J10-25, respectively, on the Control M/M2 PCBA. (Refer to Schematic No. 104745, zone 2-7C or 106875, zone 4-7C).

5.3.9 POWER INDICATOR

The POWER indicator is lighted when power is ON by lamp driver U5 (Control M PCBA) or U15 (Control M2 PCBA). This is one of the indicator drivers on the Control M/M2 PCBA that are enabled and, in this case, switched on by NPORST from the Capstan/Regulator PCBA.

5.4 CONTROL M OR CONTROL M2 PCBA

The Model T1940-96 Tape Transport may be supplied with either a Control M PCBA (refer to Schematic No. 104745) or a Control M2 PCBA (refer to Schematic No. 106875). The Control M PCBA functional description is contained in paragraph 5.4.1. The Control M2 PCBA functional description is contained in paragraph 5.4.2.

5.4.1 CONTROL M PCBA

The Control M Printed Circuit Board Assembly integrates, develops, and applies the commands received from the host system and/or from the manual control switches.

External commands, including transport selection codes, are delivered from the interface to the Control M PCBA via the Interconnect D/D1 PCBA, connector J8. Manual commands from the control panel are connected via J10 on the Control M PCBA.

Internal signals used in the control process include feedbacks and status signals. These arrive at the Control M PCBA via the Interconnect F/F1 PCBA (J21/J24) and J10 on the Interconnect D/D1 PCBA. Timing is provided by a 1-MHz oscillator and a battery of frequency dividers, which are part of the Control M PCBA.

Inputs and outputs are detailed in Figure 5-6. The following text describes the Control M PCBA circuits that develop the inputs into control outputs for the other transport circuits and the host system. Refer to Section 4 for for the theory of operation of the entire control subsystem external to the Control M PCBA. Refer to Figure 5-7*for source of sensor feedbacks.

5.4.1.1 Control System Timing

Control M PCBA clocks are derived from the 1-MHz oscillator circuits associated with crystal Y1. (Refer to Schematic No. 104745, zone 1-17F.) The 1-MHz prime frequency is referred to as Clock A (CLKA) and can be monitored at TP20.

The oscillator output is cascaded through a series of decade dividers and one final flip-flop to provide the required additional frequencies. The available frequencies, including the oscillator output, are listed in Table 5-2. Load/unload sequence counter outputs are discussed in Paragraph 5.4.1.10.

5.4.1.2 Transport Selection (NSLTA)

In host systems that use more than one transport, each unit is assigned a selection code number. The designated number (0, 1, 2, or 3) is set on the front-panel thumbwheel switch. When the host system addresses a unit, one of the select inputs (P8-15, 39, 40, or 41) goes low. (Refer to Schematic No. 104745, zone 2-17C.) If the selected line corresponds with the switch setting, the low input is applied to U44-5 (zone 2-13C), producing SLT and SLTA signals. SLT is applied to the Motion command circuits (zone 2-16D) as one of the enabling inputs. SLTA is routed to U102-1 (zone 2-3F) to produce the NSALTA control signal at P8-23. NSLTA is applied to other transport circuits through Interconnect D/D1 PCBA. Refer to Table 5-1. In some installations, such as those using an F6250 Formatter, actual selection is made by selection of the formatter's applicable tape unit port. In such cases, the switch-setting information is used for status information only.

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*Foldout drawing, see end of section.

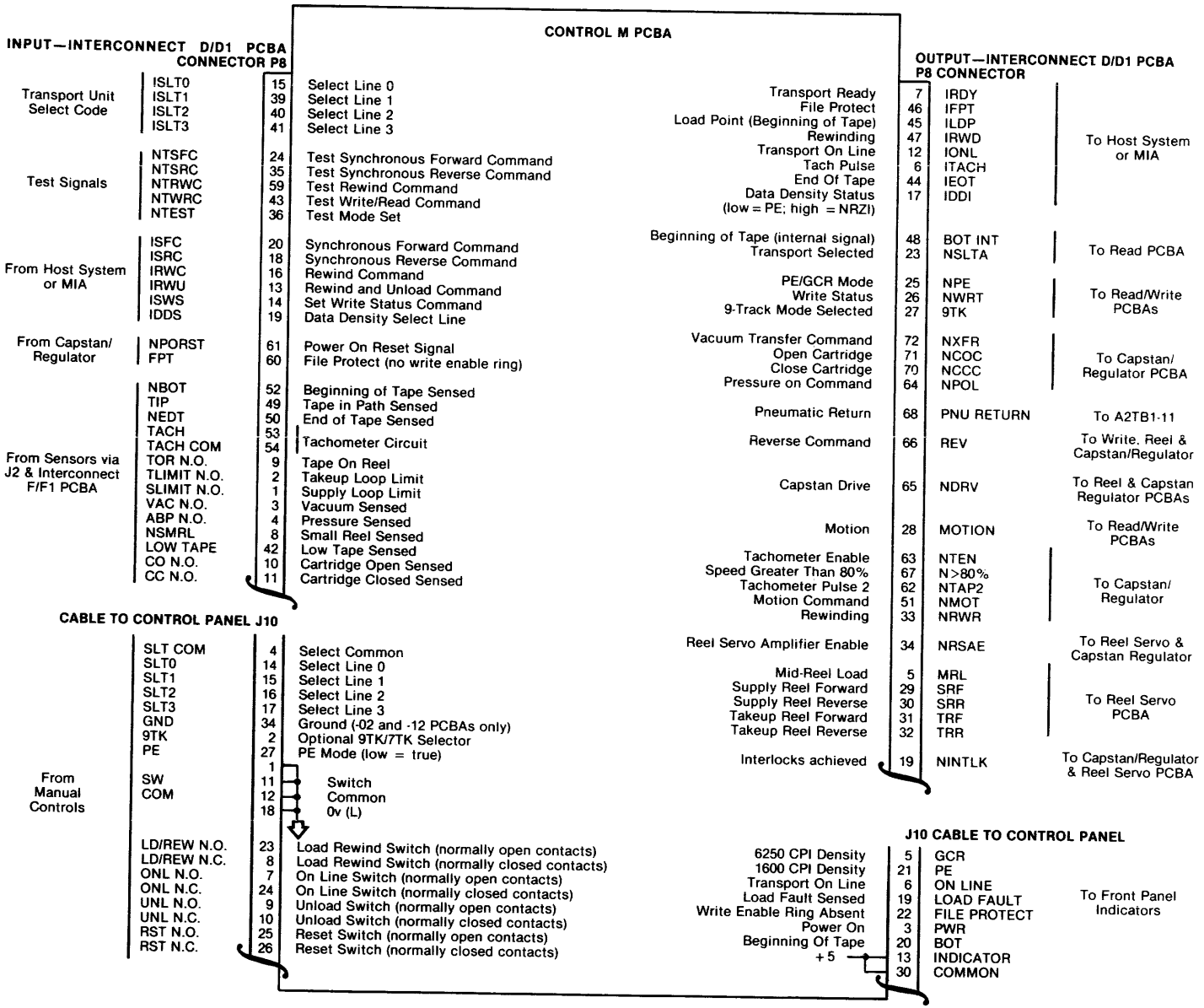

Figure 5-6. Control M PCBA Inputs and Outputs

Table 5-2

Basic Timing Frequencies
(Refer to Schematic No. 104745)

Name	Frequency	Testpoint	Distribution	Sheet and Zone	Primary Use	Associated Signals
CLKA	1 MHz	TP20	U113-3,11	3-14A	Tachometer pulse generation	TAPEN, TACHP, NTAP2, NTEN, NRWR, N>80%
			U115-5	3-12A	GO pulse generation	NGOP
CLKB	100 KHz	TP15	U35-11, U25-11	2-8C	Master reset pulse generation	NMRSTP
			U35-3, U34-3,11	2-8F	Load reset pulse, load pulse and rewind pulse generation	NLRSTP, NLDP NREWP
CLKC	10 KHz	TP39	U214-11, U215-11	3-6F	Stop pulse generation	NDRV
	1 KHz				Not used	
	100 Hz	TP17			Not used	
CLKE	10 Hz	TP19	U65-9	2-4C	Load fault indicator control	LOAD FAULT (LDFS)
			U54-13	3-15F	GO pulse, stop pulse generation	NGOP, NDRU, NMOT
			U114-11	4-11B	Load fault signal	LDFS
					Vacuum control	NXFR
					Reel motion	SRF, SRR, TRF, TRR
			U163-5	4-11E	Thread signal	THDS
			U196-11, U205-3	4-12D	Set tape loops command	STL
			U101-14	4-7D	Load fault	LDFO, LDFS
CLKF	1 Hz		U164-11,3	4-14G	Interlock circuits	INTLK1, DINTLK, NDINTLK, INTLKPI
CLKG	0.5 Hz		U64-13, U74-1	3-15G	Forward/reverse motion	NGOP (NTSFC, NTSRC mode check)

5.4.1.3 Modes of Operation

The Control M PCBA processes internal and external commands to establish the required modes of operation. The major modes, as determined by the purposes that the transport is to be used for are:

(1) Read Only, Forward
(2) Read Only, Reverse
(3) Write and Read Forward
(4) Write and Read Reverse
(5) PE Recording Density
(6) GCR Recording Density
(7) Load Tape
(8) Rewind Tape
(9) Unload Tape
(10) Test

Some of these modes are effective simultaneously with each other and with certain machine status modes that define the conditions required to enable the major modes of operation. The machine status modes are Power-On Status, which initiates Power-On Reset (NPORST); Reset, initiated by master reset pulse (NMRSTP); Ready (RDY); On-line (ONL); Unit Selected (NSLTA); various monitored conditions that establish the interlock signals (such as INTLK, NINTLK, INTLKP), etc. These modes are discussed in the following paragraphs.

Control M PCBA circuits that process the various commands and the operational task modes (Load, etc.) are discussed later in this section.

5.4.1.4 Reset/Preset Mode

The Reset/Preset mode clears and resets the transport's circuits for a new operation. It is initiated automatically when power is applied after an interruption. It may be initiated by the operator at other times by momentarily pressing the RESET pushbutton.

The circuits that check the conditions (adequate power, etc.) and develop the reset/preset signals (NPORST, and ENBL) are located on the Capstan/Regulator PCBA and are discussed on a system basis in Paragraph 5.3.8. The Control M PCBA uses RST N.O., RST N.C. and the NPORST signals that are described in the text.

NPORST is a low = true pulse produced when power is applied. The pulse input is at P8-61. (Refer to Schematic No. 104745, zone 2-9B.) NPORST is used to enable the front panel indicators (zone 2-3C). It is also applied to NOR gate U45 (zone 2-6C) as one of two inputs, either of which will produce NMRSTP at the output of NAND gate (U55-8). NMRSTP is the low = true master reset pulse used in various circuits on the Control M PCBA as listed in zone 2-5C.

RST N.C. (J10-25) and RST N.O. (J10-26) inputs establish the state of flip-flop output U26-9. As the mnemonics imply, the RESET pushbutton switch contacts normally close the U36-13 clear (CL) inverted input circuit to signal ground (0v) and Q output (U36-9) is low. The preset (PR) input (U36-10) is kept high by U16-13.

When the RESET switch is depressed, RST N.O. contacts are closed to ground and RST N.C. contacts are opened. The preset input U36-10 is pulled down momentarily, and the Q output (U36-9) applies a high to flip-flop U35-12. At clock B time, applied at U35-11, the Q output (U35-9) applies a high to NAND gate U24-13 and to flip-flop input U25-12. The Q output of the flip-flop goes high, and U25-8 sends a high to NAND gate input U24-12. NAND gate output U24-11 goes low and initiates an NMRSTP low = true pulse from U55-8. The pulse continues approximately 10 microseconds after the pushbutton is released.

The low = true master reset pulse (NMRSTP), whether generated manually or automatically when power is applied, is used in the following networks on the Control M PCBA:

Used in Producing	Schematic No. 104745, Sheet and Zone
NRST1	3-14E
PNU RETURN, UNL1	4-6F
NLDFS, NPOL, NXFR	4-7B
NLRST	4-12H
RST, NRST	4-14D

NRSTI goes to U81-1, to preset the flip-flop (zone 3-14E) that controls rewind status, and to U25-1, to clear the flip-flop that initiates the on-line signals (ONL, DONL, NONL).

The PNU RETURN signal (4-1G) is used to turn on the compressor/blower motor. It is enabled by the application of NMRSTP to U146-1 and 13 (zones 4-4F,5F,6F).

Load fault status (NLDFS) flip-flop (zone 4-7B) is cleared by the application of NMRSTP to U192-1. This enables Motion and other physical command outputs through P8 as shown in zones 4-2A through 4-2G. The PNU RETURN signal goes to A2TB1-11 for blower control;

NRSAE, NXFR, NCOC, NCCC, and NPOL are connected to the Capstan/Regulator PCBA; NRSAE, MRL, SRF, SRR, TRF, and TRR are connected to the Reel Servo PCBA.

NLRST (zone 4-11H) is produced either by NMRSTP at U174-9 or by the interlock (NINTLK) signal at U174-10,11. NLRST resets the tape loading procedure flip-flop (zones 4-11F,G through 4-7G). RST and NRST (zone 4-12D) are initiated by NMRSTP at OR gate U154-9 or by other inputs to the same gate (zone 4-14D). RST resets the *try counter* (zone 4-16B) that issues load command (NLDC), and the load sequence counter that produces the load counts (NC1,2; C1,2, etc.). Refer to zones 4-14A through D from where the count signals fan out to other areas of sheet 4.

The preceding paragraphs describe the distribution of the master reset pulse NMRSTP and, in general, the circuits on the Control M PCBA where used. The complete functions of the various circuits, other than resetting, are described separately in appropriately titled paragraphs.

5.4.1.5 Interlock Circuits (NINTLK, INTLK, INTLK1, DINTLK, NDINTLK, NINTLKP1, NINTLKP2)

The interlock circuits are designed to inhibit and/or enable various modes on the basis of monitored air and tape conditions. The basic interlock signal is the low = true NINTLK level found at TP62 and P8-69 (Schematic No. 104745, zone 4-2H), and at the NAND gate output (U154-6) where the signal originates. The NAND gate (zone 4-15G) requires a high level at inputs U154-1,2,4, and 5 to produce a low = true NINTLK output level at U154-6. The inputs are controlled by the pressure switches that sense the supply and takeup reel loop limits (SLIMIT and TLIMIT), vacuum pressure (VAC) and positive pressure (ABP). The switches are each connected (via Interconnect F/F1 PCBA; J21, Interconnect D/D1 PCBA, and J8) to their respective pins (J8-1,2,3, and 4) as shown in zones 4-17F and G. A satisfactory condition causes the corresponding switch to close its circuit to signal ground. This pulls down the level at the respective input to J8. Zones 4-17F,G through 4-14F,G show how these inputs are ANDed at gate output U154-6 to produce NINTLK.

5.4.1.6 9-Track/7-Track Mode Selection Circuits

No provisions are made for 7-track mode.

5.4.1.7 PE/GCR Density Modes

Control M PCBA output NPE (low = true) at P8-25 selects Phase Encoded (PE) mode. When NPE is high = false, the GCR mode is effective. (Refer to Schematic No. 104745, zone 2-2G.)

NPE is normally high = false if PE mode is not selected. When PE is selected by placing the front panel DENSITY switch in 1600 position, J10-27 (zone 2-9G) is pulled down. This causes U44-10 to apply a high to U111-13 and (when a high is present at U72-6 and U111-12) U111-11 is low, resulting in a low = true NPE at P8-25. If the transport has no DENSITY switch or equivalent, the unit will work in GCR (NPE will be high = false) unless jumper W2 is installed as shown in zone 2-8G. With W2 in place, density mode may be controlled by host system software at BOT.

If the host system applies a low = true IDDS at the interface, P8-19 (zone 2-17D) will be low; this will apply a low at U54-2 (zone 2-5G), causing the OR gate to override the transport circuits and place the unit in PE mode (NPE low = true). This circuit also initiates the DDI signal (zone 2-3G and 2-12D), producing the interface IDDI signal through P8-17 (zone 2-11D) if the interface driver (U151) is enabled by transport selection (SLTA) from U65-6 (zone 2-12C). A density change can only be implemented at BOT due to ARA considerations. Refer to Paragraph 5.4.1.9.

5.4.1.8 Beginning-of-Tape Interlock (BOT INT)

The BOT INT output at P8-48 (refer to Schematic No. 104745, zone 2-2G) of the Control M PCBA to J5-12 of the Read PCBA is a high = true level initiated when the beginning marker on the tape is in register with the BOT optical sensor. At this time a low = true level (NBOT) appears at P8-52 (zone 2-9B) via Interconnect D/D1 and F/F1 PCBAs. The NBOT signal is also applied to various circuits on the Control M PCBA as shown or referenced on the schematic (zones 2-8B through 2-2B).

5.4.1.9 Unit Selected Mode (NSLTA)

The NSLTA output at P8-23 of the Control M PCBA (refer to Schematic No. 104745, zone 2-2F) is a low = true level if the host system uses only one transport. It is also low = true while the system is addressing the unit code that has been selected on the transport's front panel thumbwheel selector switch. These circuts are discussed in Paragraph 4.5.2.

5.4.1.10 Tape Load/Rewind and Unload Modes

The tape loading procedure involves all of those steps that result in the tape being installed and brought to the beginning-of-tape (BOT) position. The steps include motion in either or both directions and may include cartridge and pneumatic system control. If a reel of tape has been installed on the supply reel spindle but the sensors determine that the tape has not been threaded through the guides to the takeup reel, normal load conditions exist. Pressing the LOAD/REW button will initiate the automatic threading process, that connects the tape to the takeup reel, forms the loops and stops at BOT. The tape is then ready for a read or write operation.

If tape is sensed between the supply and takeup reels when the LOAD/REWIND button is pressed, a situation called a mid-reel load condition exists, and Rewind mode is initiated. Rewind mode also terminates at BOT. Tape sensor feedbacks are shown in Figure 5-7.

Note that when the UNLOAD switch is depressed, Rewind mode is also initiated if the tape is not at BOT, but the Unload mode causes the tape to travel beyond BOT position until the tape is completely wound on the supply reel. Unload mode then causes the supply reel cartridge to close.

Schematic No. 104745, sheet 5, contains a flow chart for reel-motion logic by manual control, including motions commanded by means of the LOAD/REW and UNLOAD switches. In the following text the preliminary power-on sequence and the load sequence are discussed with reference to the flow chart (sheet 5) and various referenced zones of other sheets of the same drawing. The power-on sequence is included here because it prepares the subject circuits for the tape procedures.

5.4.1.10.1 *Tape Control Presetting by Power-On Sequence*

When power is applied (zone 5-16H), the power-on reset signal (NPORST) is produced. Refer to Paragraph 5.4.1.4. NPORST is applied to Control M PCBA J8-61 (zone 2-9B). This is distributed as shown at zone 2-8B and is gated with the manual reset circuits (zones 2-9—2-5C) to produce the master reset pulse (NMRSTP) at NAND gate output U55-8.

If the tape sensors find tape in the tape path, a high = true TIP signal is received at J8-49 (zone 2-9B) informing the circuits that a load command, when received, will be under mid-reel load conditions. TIP and NTIP initiate mid-reel load signals MRL (zones 4-10F and 4-2E) and NMRL (zone 4-9G). NTIP, from zone 2-8B, is applied to NAND gate U182-4 to inhibit a close cartridge command (NCCC). MRL goes to P12-38 of the Reel Servo PCBA, where, when low = false, it inhibits the supply reel forward motion mode control signal (NSRF2) until the midreel load procedure is complete (tape at BOT). NMRL is applied to U111-10 (zone 4-14F) to turn pressure on (PSOL) and U122-10 to preset the air control flip-flop (zone 4-17F).

MRL (zone 4-10F) is also applied to NAND gate U174-1 (zone 4-8E) as one of the conditions that preset the first delay flip-flop (U196-4, zone 4-12E). After a delay, U205-5 clocks the flip-flop that produces the set tape loops (STL) command.

When no tape is found in the path, a normal load condition exists. NTIP is high = false, NAND gate U182-4 (zone 4-3B) is enabled for a high output at U126-9 (zone 4-4B) of the cartridge control flip-flop. The other condition for issuing a close cartridge command is the input CC N.O. at U182-5 from the cartridge open sensor. The NCCC output at P8-70 sets the cartridge mechanism in closed position for installing or removing a reel on the supply hub.

The tape in path signal (NTIP) is also applied to OR gate input U174-3 (zone 4-3E) as one of the conditions for sending the supply reel reverse (SRR) command to the Reel Servo PCBA. Other conditions are sequence counts (NC0, NC1), a false load fault status signal (LDFS) and/or backwrap (BKW), cartridge open (CO N.O.), unload number 1 (UNL1) depending on the mode of operation. SRR will also be inhibited by the suppression of BKW when the set tape loops (STL) process is initiated. These signals are shown at the right-hand side of sheet 4, zones 4-6G and 4-4E—4-2C.

5.4.1.10.2 *Circuits Involved in Tape Load/Rewind/Unload Procedures*

Circuits involved in load, rewind, and unload control are shown in Schematic No. 104745 and are described as follows.

(1) **Clocks.** Basic system clocks (zones 1-16E,F,G—1-10E,F,G) are based on a crystal oscillator as described in Paragraph 5.4.1.1.

(2) **Load/Rewind Command Pulsing.** Load/rewind command and pulsing circuits (zones 2-9F—2-5F) are initiated by LOAD/REW momentary switch outputs:

Load reset pulse (NLRSTP)	U24-6, zone 2-6F
Load pulse (NLDP)	U46-6, zone 2-5G
Rewind pulse (NREWP)	U46-12, zone 2-5F

(3) **Unload Commands.** Unload command circuits (zones 2-9C,D—2-5C,D) process either a manual command from the control panel UNLOAD switch or a logic command (IRWC at interface, NULC at U45-12, zone 2-6C) and produce unload command number 2 NUNLC2 at U54-8, zone 2-5D.

(4) **Reset Commands.** Reset command circuits (zones 2-9C—2-5C). This is the only command that will interrupt a load procedure. Output is master reset pulse NMRSTP.

(5) **Load Status.** Load status flip-flop that provides the load-in-progress condition for the system. The load status (LDS) level (U136-9, zone 4-11G) participates in setting the backwrap flip-flop (zone 4-8G), sets the thread-mode flip-flop (zones 4-7G,8G), and the set-tape-loops flip-flop (zone 4-7G). These flip-flops then wait for their respective clock inputs. LDS also enables tape and reel motion command gates, etc. (zones 4-3A—G), provided no load fault exists as decided at gate output U213-3 (zone 4-6C).

(6) **Load/Unload Counts.** Load/unload step sequence count control circuits (zones 4-15A—4-15E, and 4-16B). Counter outputs (U195-12,1,9,8,11) are decoded and produce counts NC0,1,2,3,4,7 at outputs U185-1,2,3,4,5,9, respectively. The counter is incremented at input U195-14 by the output of U175-11 (zone 4-16B), which reflects the low tape sensor input pulses (P8-42, zone 4-17B) divided by 5. The divided count is provided by U165-11 (zone 4-16B). Sensor pulse inputs at U165-1 are inhibited if a load fault exists (NLDFS at U125-5). The divider output (U165-11) is not applied to the load counter (U195-14, zone 4-15D) unless the

transport is in load status (NLDS at U175-9, zone 4-16B) or tape-in-path signal (NTIP) is high = false at U175-2 and unload command UNL1 is high = true at U175-1.

(7) **Load Fault Recovery.** Load fault flip-flop (zone 4-7B) issues a high load fault status (LDFS) level at Q output U192-5 and a low load fault status level at Q output U195-6 whenever conditions warrant aborting the procedure. The flip-flop is cleared by master reset pulse NMRSTP at U192-1. In load status (LDS at U192-2) it will be set to produce fault status by the input at U192-3 from fault NOR gate output U121-8. Low inputs to the NOR gate that clock U192-3 are:

U121-1 (TP41)	Load status is terminated by end of count output to U166-8 (zone 4-13E).
U121-3 (TP42)	Try counter outputs U123-12,1,9 are high indicating that two attempts have already been made to load tape. These outputs cause NAND gate output U133-11 to produce a low.
U121-6 (TP28)	The system is at the set-tape-loop mode and the tape loop timer outputs U124-9,8,11 are all high, indicating that time for setting the loops has run out.
U121-11 (TP14)	Failure of load count (NLDC from U175-11, zone 4-15C) at start count timer flip-flop input (zone 4-8D) and timer inputs U101-2,3 (zone 4-7E), causing U184-12 to send load fault zero (LDF0) to U121-11.
U121-5 (TP32)	Failure of cartridge to open by count C3 as determined by NAND inputs U131-4 and 5 (zone 4-12B).
U121-4 (TP35)	Failure to get proper air pressure and vacuum condition by count C3 as determined by NAND inputs U131-12 and 13 (zone 4-12B). NAOK input at U131-13 is provided by the output of U133-3 (zone 4-16F) on the basis of VAC N.O. and ABP N.O. sensor inputs to P8-3 and P8-4.
U121-12,2 (TP27)	Cartridge problem as determined by NAND output U133-6 (both high) when load pulse (NLDP2) is received at U132-5. These signals are inverted and applied to U131-1,2 (zone 4-11B).

(8) **Tachometer Circuits.** Capstan tachometer signal processing and application circuits, which provide tape speed information feedbacks for optimum speed control, are shown in the lower half of sheet 3. TACH signals generated by capstan rotation arrive via Interconnect F/F1 PCBA, Interconnect D/D1 PCBA, and P8-53. Signals are shaped to form the tachometer pulse (TACHP) at U104-2 (zone 3-12C) and are sent to the interface ITACH driver (zone 2-15E), provided the tachometer pulse circuits are enabled (TAPEN at U115-12, zone 3-13C). The pulses are applied to flip-flop clock inputs U95-11 and U93-11 and preset input U92-10 (zone 3-7D,C). They are also squared and applied to the velocity decoder and time constant circuits at U85-14. After a 20 μsec delay, the output U115-8 (zone 3-11A) clears the tachometer pulse No. 2 flip-flop (zone 3-7B), providing a squared pulse 20 μsec long (NTAP2) at P8-62. After a 64 μsec delay, the output at U104-10 (zone 3-9B) clears the rewind enabling flip-flops and producing a high at U93-6 (zone 3-6C) and U83-5 (zone 3-12D). The inputs that produce U105-8 output (zone 3-9C) are all high unless jumpered by one of the wires W5 through W10. The time constants selected for connection are determined by model and tape speed rating of the transport, as listed in Table II (zone 1-5H). The output at U105-8, when all inputs are high, changes the state of outputs at U95-9 (zone 3-7D) and U92-5 (zone 3-6D). When the latter output is low, the rewind ramp is terminated (NRWR, zone 3-1E).

When the N>80% signal is high = false, it indicates that a tape speed greater than 80 percent has not been achieved, and tachometer enabling signal NTEN is high = false. When 80 percent speed is achieved, these states are reversed. These signals are used in both states (true or false) in the application of acceleration and deceleration (start and stop) ramps and steady synchronous motion. Note that conversion of the tachometer frequency pulses (NTAP2) to analog voltage signals used in the capstan servo summing amplifier is accomplished by circuits on the Capstan/Regulator PCBA. Refer to Schematic No. 104757, zones 2-12C,D—2-9C,D.

(9) **Unload Control.** Unload procedure control circuits are shown in zones 4-6G—4-2B. NUNLC2 (refer to Item 3) presets first stage (rewind) unload command flip-flop (zone 4-6G). Output U146-5 (UNL1) is applied as a condition to various NAND gates as shown in the schematic and to enable the load counter (4-17C). Q output U146-6 (NUNL1) provides the reel servo amplifier enable output at P8-34 by presetting flip-flop output U205-9. NUNL1 is also used in the mode circuits (zone 2-15C) and to initiate the rewind pulse circuits (2-8E). NULRW from U134-12 (zone 4-4E) is applied to U71-11 (zone 3-15E) to establish the state of the rewind status circuits. The output of U82-6 (zone 3-11D) is applied to the motion control circuits at U83-9 (zone 3-13F) to start tape motion. When BOT is sensed (BOT at U132-13, zone 4-5E), the rewind part of the process ends, but unload rewinding motion continues until interlock is broken (INTLK low = false at U134-1, zone 4-4E). BOT also is applied to the PNU RET flip-flop at its presetting input NAND gate (U156-10), and clock input U146-11 (zone 4-4G). At C4 count, flip-flop input U146-13 (zone 4-4G) clears the flip-flop disconnecting the PNU RET line, which turns off the blower/compressor motor. When interlock is broken (NINTLK high = false at U204-5, zone 4-3E), U205-9 changes state, disabling the reel servo amplifiers (NRSAE high = false).

5.4.1.10.3 *Tape Load/Unload Procedure Counters*

The tape loading procedure employs two counters: a *try counter* and a *sequencing counter,* which are described in the following paragraphs.

The try counter provides for automatically making a second attempt to start the loading sequence if the first attempt fails, but it inhibits repetitious recycling. The try counter is cleared and reset by an input at U123-2 and 3 (zone 4-10C) from NOR gate output U154-8 (zone 4-13C). Inputs to the NOR gate are the master reset pulse (NMRSTP), load reset pulse (NLRSTP), unload signal (NUNLC2) and delayed interlock (NDINTLK).

The try counter is incremented by a low input at U123-14 that primarily reflects the output of NAND gate U116-6 (zone 4-12B). At sequence count one output (C1), the inputs to the NAND gate are C1, try counter zero (T0) inverted, and the inverted NSMRL input. This increments the counter to T1. At NC3 time from the sequencing counter, NOR gate input U186-13 is low, U186-11 is high, U176-10 is low and the try counter is incremented to T2. When the counter outputs are high (at TP3) at U123-1 and 9, the output at NAND gate U133-11 is low and reports a load fault at load fault NOR gate U121-3, preventing a third try. The NSMRL input inhibits a second try when a small reel is loaded.

The sequencing counter is reset by the reset (RST) input to the counter at U195-2,3 (zone 4-15D). It is incremented by pulses from the low tape sensor P8-42 (zone 4-17D) after these pulse counts have been divided by five at divider output U165-11 (zone 4-16B). Application of the pulses are on the condition that no load fault has occurred, i.e., the load fault status signal NLDS at U125-5 (zone 4-17B) is high = false.

The low tape sensor, sometimes referred to as pack sense (PKSN), pulses are the output of an optical detector that senses two reflective tabs placed on the inside of the takeup reel flange. The detector looks at these tabs through two slots in the side of the reel opposite the tabs. Each time the reel turns, two tabs are sensed. This produces two low tape sensor

counts per revolution of the reel, provided there is not enough tape on the reel to block the path between the detector and the tabs. In Rewind mode, when the tape on the takeup reel is down to about 9.525 mm (0.375 inch), the low tape sensor begins issuing pulses, the first one of which is used to slow tape motion so the reels can stop at BOT. In forward motion, the pulses are sent to the logic until the tape on the takeup reel is sufficient to block the sensor path. These pulses, at the rate of two pulses per turn, are sent through P8-42 to U125-4 (zone 4-17B). During the load process, if no load fault exists, NLDFS will be high = false at U125-5 and U125-6 will apply the inverted pulses to U165-1. The output of U165-11 of the divider will be one pulse per five inputs, or one per 2½ turns of the reel, at NAND gate input U175-12. If the transport is in load status (NLDS at NOR gate U175-9) then U175-11 will issue low load count pulses (NLDC). These are applied to the sequencing counter incrementing input U195-14.

The outputs of the sequencing counter are applied to decoder inputs U185-12, 13, 14, 15. Decoder outputs are low at times that correspond to the count as shown inside the box plus 1 (e.g., U185-1 is low at the zero count, U185-2 is low at the first count, etc.). These counts are low = true NC1, NC2, etc. When inverted they are C1, C2, etc. The counts are used to cue the various loading process steps (backwrap (BKW), thread (THD), set tape loops (STL), etc.). Refer to Tables 5-3 and 5-4.

It should be noted that low tape counts at U195-12,1 (zone 4-15E) are applied to U116-9 (zone 4-11E) as well as to the decoder. Similarly, counter output U195-11 is inverted and applied to clock flip-flop (U166-11, zone 4-13E). Flip-flop output U166-9 is applied to NAND gate input U116-10 (zone 4-11D). If BOT is reached, load status ends (LDS low), so U116-8 cannot issue a low fault output. If counts stop before BOT is reached, U116-9 will go low, producing a load fault. Also, counter outputs to the decoder are binary; A = 1, B = 2, C = 4, D = 8. D clocks the flip-flop such that output U166-3 goes high at count 16 (the next binary order). This allows about 92 meters (30 feet) of tape to pass, while searching for BOT, without signalling a time-out load fault.

5.4.1.10.4 *Automatic Tape Loading Sequence*

When the Load command is issued by pressing the LOAD/REW switch, the logic goes through a series of steps based on feedbacks from status sensors and cued by the sequencing counter. The hardware circuits that make the decisions are shown in Schematic No. 104745, sheets 1 through 4. The logic flow chart for the procedure is in the same drawing, sheet 5. Sensor feedbacks are shown in Figure 5-7.

If tape is in the path and air status is satisfactory for operation after the LOAD/REW button is depressed, interlocks will be made (refer to Paragraph 5.4.1.5). NDINTLK will be applied (zone 2-6G) and Rewind mode will be commanded by the resulting low = true rewind pulse (NREWP). The tape will stop at BOT, and the load will be completed.

If interlocks are not made when the LOAD/REW command is processed, the automatic load sequence will be initiated by the low = true load pulse (NLDP).

Pulsing is developed by the series of flip-flops (zones 2-8G,F to 7G,F) activated by the LOAD/REW switch. While the momentary switch is depressed, J10-23 is connected to ground, which presets the first flip-flop in the series. The resulting Q output (U36-5) sets the next flip-flop at clock B (CLKB) time. (Refer to Paragraph 5.4.1.1 for system clock details.) When the switch is released, J10-23 is disconnected from ground, U36-4 goes high and U36-1 goes low. This clears the first flip-flop while the second stays in set state until cleared by an unload (NUNL1) or load status (NLDS) signal at NOR gate U183 inputs 12 or 13 respectively.

Table 5-3
Load/Unload Sequence Control Count Applications
(Refer to Schematic No. 104745)

Decoder Pin (zone 4-15,16D)	Count* (N = Low)	Distribution/ Zone	Mode	Effect
U185-1	NC0	U202-11/4-4B	Load	Opens cartridge if not open and no fault exists.
		U174-4/4-4E	Unload	Commands supply reel reverse if interlocks are not made (after BOT is reached).
U185-2	NC1	U202-10/4-4B	Load/Unload	Opens cartridge if not open, tape is in path, and no fault exists.
		U122-11/4-17F	Load	If air pressure is ok, issues PSOL command.
		U174-5/4-4E	Unload	Starts supply reel reverse if interlocks are not made (after BOT is reached).
	CI	U116-4/4-12C	Load	Increments Try Counter if a small reel has been sensed and if one try has not already been made.
		U135-3/4-9F	Load	Starts backwrap if in load status, small reel has not been detected, and there is no tape in path (not a midreel load).
U185-3	NC2	U202-9/4-4B	Load/Unload	Opens cartridge if not open and no fault exists.
		U145-11/4-8G	Load	Trailing edge starts threading process if in load status.
U185-4	NC3	U132-9/4-12B	Load	Initiates load fault status: if cartridge is not open; or if air is not ok.
		U183-1/4-5B	Unload	Inverted to C3, closes cartridge if unload is complete, there is no tape in path, and cartridge is open.
		U144-12/4-9E	Load	Clears backwrap flip-flop.
		U186-13/4-12D	Load	Increments Try Counter.
U185-5	NC4	U125-1,2/4-14D	Unload	Inverts to C4 and goes to U156-13/4-6F to terminate process if in unload status.

*Counts are produced only under the following conditions (zones 4-16B,17B):

Mode	NLDFS (U125-5)	NLDS (U175-9)	NTIP (U175-2)	UNLI (U175-1)
Load	High = False	Low = True	N/A	N/A
Unload	High = False	N/A	High = False	High = True

Table 5-4
Try Counter Outputs
(Refer to Schematic No. 104745, zone 4-10D)

Try No.	U123-12,1	U123-9	U133-11	Effect
T0 (reset)	Low	Low	High	Enable
T1 (first)	High	Low	High	Permits try
T2 (second)	Low	High	High	Permits try
T3 (third)	High	High	Low	Inhibits try

The Q output at U35-5 applies a high at NAND gate input U24-4 while the $\overline{Q}$ output at U34-6 applies a high to NAND gate U24-5 producing a load reset low = true output (NLRSTP) at U24-6. This is sent to EXCLUSIVE NOR gate input U154-10 (zone 4-14 D) to reset the load sequence counters and control circuits. At clock B time, the output of U35-5 (zone 2-7F) causes the next flip-flop to change state terminating the NLRSTP pulse (U24-6) and applying its high Q output to NAND gate U33-10 which, while $\overline{Q}$ output at U34-8 is high, causes NAND output U33-8 to initiate a low load pulse (NLDP) at U46-6 (TP18). This pulse is terminated when the Q output at U34-8 changes state at the next clock B time. NLDP is sent to U136-10 (zone 4-11G) to preset the load status (LDS) flip-flop and U135-10 (zone 4-9G) to preset the thread status (THDS) flip-flop. It is also inverted and used as a condition for output of NAND gate U131-3 (zone 4-11A).

If no cartridge is in place or if the cartridge is sensed as neither open nor closed, U131-3 (zone 4-11A) is low, causing a load fault signal at U121-8 (zone 4-8B) and a load fault status level (NLDFS) at the Q output (U192-6) of the load fault flip-flop. NLDFS is applied to U125-5 (zone 4-17B) as one of the conditions in the network that issues the load count (NLDC) signal to U195-14 to increment the sequence counter U195, and decoder U185 (zone 4-15D,4-14D). If NLDFS is true = low at U125-5, the reel-turning pulses from the low tape sensor are prevented from entering the divide-by-five chip at U165-1 (zone 4-16B).

If the cartridge is ok, U185-2 (zone 4-15D) issues count C1, which clocks backwrap (BKW) flip-flop U135-3 (zone 4-8F), and NC1, which clocks the air control flip-flop (U22-11) at zone 4-17F. Since, during normal load sequence, interlock is not made (NINTLK at U154-6, zone 4-15G, high = false), U111-8 (zone 4-14F) issues pressure solenoid command (PSOL).

If no load fault exists, U192-6 (zone 4-7B) will be high and U123-3 (zone 4-6B) will be low, clearing the cartridge command flip-flop (zone 4-4A). This causes $\overline{Q}$ output U126-8 to initiate the NCOC command to open the cartridge.

At NC1, the backwrap flip-flop is enabled to be set (by the output of U155-6, zone 4-9G), provided the inputs (U155-9,10,11) are high, indicating that load status (LDS) mode is set (U155-11), a midreel load condition does not exist (U155-10), and the try counter output (U123-9, zone 4-10C) indicates no more than one previous try has been made (U123-9 high).

Load sequence count NC2 is applied to thread command flip-flop U145-11 (zone 4-7G). The NTHD output (U145-8) is sent to U213-10 (zone 4-5D) to initiate the supply reel forward (SRF) command and continue takeup reel forward (TRF) command.

Load sequence count NC3 (zone 4-14D) applied to OR gate U144-12 (zone 4-9E) initiates clearing of the backwrap flip-flop (zone 4-8F). NC3 at U132-9 (zone 4-13B) is inverted to C3 and applied to NAND gate U131-4, which checks the cartridge open signal CO N.O. for a possible load fault. U131-11 (zone 4-12B) similarly checks for air system faults.

When tape appears in the path (BOT or NAOK), U176-12 (zone 4-7E) presets flip-flop U196-4 (zone 4-12E). The succeeding two flip-flops, clocked by CLKE, provide a delayed output at U205-5, which sets the tape loop command (STL) flip-flop. This delivers STL (zone 4-7G) to the reel servo motion commands at zone 4-4C. The takeup reel reverse (TRR) and supply reel forward (SRF) commands provide slack tape to form the loops.

When loops are set and interlock is made (NINTLK at U213-13, zone 4-6E), takeup reel reverse (TRR) and supply reel reverse (SRR) are commanded (zone 4-1C,D). When BOT is sensed, U146-11 (zone 4-4G) is high and output U146-8 terminates motion.

5.4.2 CONTROL M2 PCBA

The Control M2 Printed Circuit Board Assembly integrates, develops, and applies the commands received from the host system and/or from the manual control switches.

External commands, including transport selection codes, are delivered from the interface to the Control M2 PCBA via the Interconnect D/D1 PCBA, connector J8. Manual commands from the control panel are connected via J10 on the Control M2 PCBA.

Internal signals used in the control process include feedbacks and status signals. These arrive at the Control M2 PCBA via the Interconnect F/F1 PCBA (J21/J24) and J10 on the Interconnect D/D1 PCBA. Timing is provided by a 1-MHz oscillator and a battery of frequency dividers, which are part of the Control M2 PCBA.

Inputs and outputs are detailed in Figure 5-8. The following text describes the Control M2 PCBA circuits that develop the inputs into control outputs for the other transport circuits and the host system. Refer to Section 4 for for the theory of operation of the entire control subsystem external to the Control M2 PCBA. Refer to Figure 5-7* for source of sensor feedbacks.

5.4.2.1 Control System Timing

Control M2 PCBA clocks are derived from the 1-MHz oscillator circuits associated with crystal Y1. (Refer to Schematic No. 106875, zone 2-6G.) The 1-MHz prime frequency is referred to as Clock A (CLKA) and can be monitored at TP20.

The oscillator output is cascaded through a series of decade dividers and one final flip-flop to provide the required additional frequencies. The available frequencies, including the oscillator output, are listed in Table 5-5. Load/unload sequence counter outputs are discussed in Paragraph 5.4.2.10.

5.4.2.2 Transport Selection (NSLTA)

In host systems that use more than one transport, each unit is assigned a selection code number. The designated number (0, 1, 2, or 3) is set on the front-panel thumbwheel switch. When the host system addresses a unit, one of the select inputs (P8-15, 39, 40, or 41) goes low. (Refer to Schematic No. 106875, zone 3-8B.) If the selected line corresponds with the switch setting, the low input is applied to U102-9 (zone 3-6C), producing SLT and SLTA signals. SLT is applied to the Motion command circuits (zone 2-5E) as one of the enabling inputs. SLTA is routed to U143-5 (zone 4-2H) to produce the NSALTA control signal at P8-23. NSLTA is applied to other transport circuits through Interconnect D/D1 PCBA. Refer to Table 5-1. In some installations, such as those using an F6250 Formatter, actual selection is made by selection of the formatter's applicable tape unit port. In such cases, the switch-setting information is used for status information only.

5.4.2.3 Modes of Operation

The Control M2 PCBA processes internal and external commands to establish the required modes of operation. The major modes, as determined by the purposes that the transport is to be used for are:

(1) Read Only, Forward
(2) Read Only, Reverse
(3) Write and Read Forward
(4) Write and Read Reverse

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*Foldout drawing, see end of section.

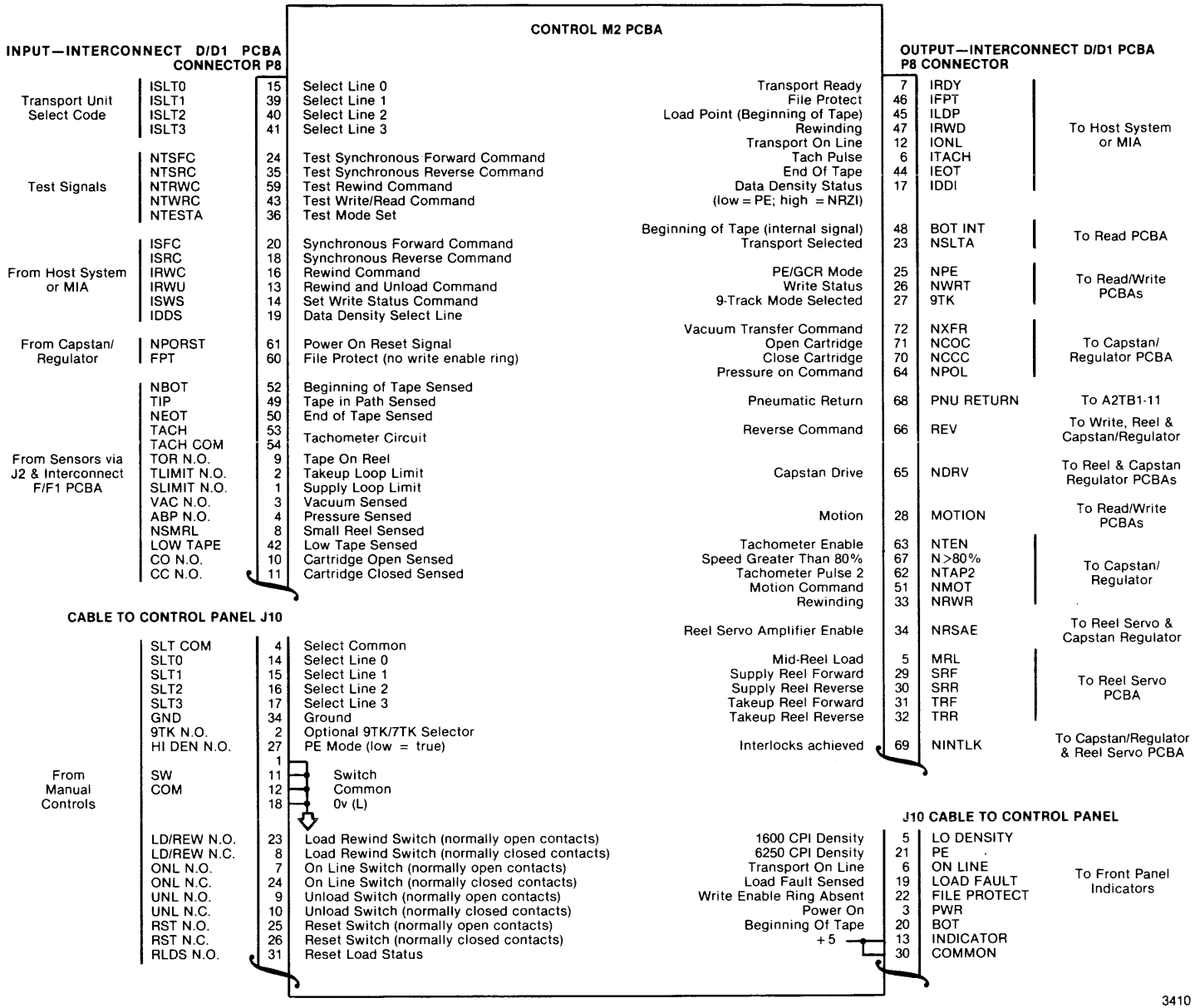


Figure 5-8. Control M2 PCBA Inputs and Outputs

Table 5-5

Basic Timing Frequencies
(Refer to Schematic No. 106875)

Name	Frequency	Testpoint	Distribution	Sheet and Zone	Primary Use	Associated Signals
CLKA	1 MHz	TP20	U12-3, U116-5	6-5G, 6-4F	Tachometer pulse generation	TAPEN, TACHP, NTAP2, NTEN, NRWR, N>80%
			U52-3,11, U53-3,11	5-3F,G,H 5-4F,G,H	GO pulse and reverse pulse generation	NGOP, REV
CLKB	100 KHz	TP15	U35-11, U25-11	4-6D	Master reset pulse generation	NMRSTP
			U35-3, U34-3,11 U61-3	4-4F 4-3G	Load reset pulse, load pulse and rewind pulse generation	NLRSTP, NLDP1 NREWP, NLDP2
CLKC	10 KHz	TP39	U225-12	5-6C	Stop pulse generation	NDRV
	1 KHz				Not used	
	100 Hz	TP17			Not used	
CLKE	10 Hz	TP19	U63-9	4-3B	Load fault indicator control	LOAD FAULT (LDFS)
			U54-13	5-7G	GO pulse, stop pulse, and reverse pulse generation	NGOP, NDRV, NMOT
			U115-9	8-6A	Load fault	LDF6
			U183-5	7-7C	Thread signal	THDS
			U216-11, U226-11	7-5B,6B	Set tape loops command	STL
CLKF	1 Hz		U184-11,3	7-3G	Interlock circuits	INTLK1, DINTLK, NDINTLK, INTLKPI
			U101-14	9-7F	Load fault	LDF0
CLKG	0.5 Hz		U64-13, U74-1	5-7F	Forward/reverse motion	NGOP (NTSFC, NTSRC mode check)

(5) PE Recording Density
(6) GCR Recording Density
(7) Load Tape
(8) Rewind Tape
(9) Unload Tape
(10) Test

Some of these modes are effective simultaneously with each other and with certain machine status modes that define the conditions required to enable the major modes of operation. The machine status modes are Power-On Status, which initiates Power-On Reset (NPORST); Reset, initiated by master reset pulse (NMRSTP); Ready (RDY); On-line (ONL); Unit Selected (NSLTA); various monitored conditions that establish the interlock signals (such as INTLK, NINTLK, INTLKP), etc. These modes are discussed in the following paragraphs.

Control M2 PCBA circuits that process the various commands and the operational task modes (Load, etc.) are discussed later in this section.

5.4.2.4 Reset/Preset Mode

The Reset/Preset mode clears and resets the transport's circuits for a new operation. It is initiated automatically when power is applied after an interruption. It may be initiated by the operator at other times by momentarily pressing the RESET pushbutton.

The circuits that check the conditions (adequate power, etc.) and develop the reset/preset signals (NPORST, and ENBL) are located on the Capstan/Regulator PCBA and are discussed on a system basis in Paragraph 5.3.8. The Control M2 PCBA uses RST N.O., RST N.C. and the NPORST signals that are described in the text.

NPORST is a low = true pulse produced when power is applied. The pulse input is at P8-61. (Refer to Schematic No. 106875, zone 4-8C.) NPORST is used to enable the front panel indicators (zone 4-3B). It is also applied to NOR gate U3 (zone 4-4C) as one of three inputs, any of which will produce NMRSTP at the output of NAND gate (U13-11). NMRSTP is the low = true master reset pulse used in various circuits on the Control M2 PCBA.

RST N.C. (J10-26) and RST N.O. (J10-25) inputs establish the state of flip-flop output U26-9. As the mnemonics imply, the RESET pushbutton switch contacts normally close the U26-13 clear (CL) inverted input circuit to signal ground (0v) and Q output (U26-9) is low. The preset (PR) input (U26-10) is kept high by U6-10.

When the RESET switch is depressed, RST N.O. contacts are closed to ground and RST N.C. contacts are opened. The preset input U26-10 is pulled down momentarily, and the Q output (U26-9) applies a high to flip-flop U35-12. At clock B time, applied at U35-11, the Q output (U35-9) applies a high to NAND gate U24-13 and to flip-flop input U25-12. The Q output of the flip-flop goes high, and U25-8 sends a high to NAND gate input U24-12. NAND gate output U24-11 goes low and initiates an NMRSTP low = true pulse from U13-11. The pulse continues approximately 10 microseconds after the pushbutton is released.

The low = true master reset pulse (NMRSTP), whether generated manually or automatically when power is applied, is used in the following networks on the Control M2 PCBA:

Used in Producing	Schematic No. 106875, Sheet and Zone
NRST1	5-8E
PNU RETURN, UNL1	9-6F
NLDFS, NPOL, NXFR	9-7B
NLRST	7-8E
RST, NRST	8-8FD

NRSTI goes to U81-4, to preset the flip-flop (zone 5-7D) that controls rewind status, and to U25-1, to clear the flip-flop that initiates the on-line signals (ONL, DONL, NONL).

The PNU RETURN signal (9-1G) is used to turn on the compressor/blower motor. It is enabled by the application of NMRSTP to U146-1 and 13 (zones 9-5G,6G).

Load fault status (NLDFS) flip-flop (zone 9-7B) is cleared by the application of NMRSTP to U166-13. This enables Motion and other physical command outputs through P8 as shown in zones 9-2A through 9-2G. The PNU RETURN signal goes to A2TB1-11 for blower control; NXFR, NCOC, NCCC, and NPOL are connected to the Capstan/Regulator PCBA; NRSAE, MRL, SRF, SRR, TRF, and TRR are connected to the Reel Servo PCBA.

NLRST (zone 7-4E) is produced either by NMRSTP at U194-9 or by the interlock (NINTLK) signal at U194-10,11. NLRST resets the tape loading procedure flip-flop (zones 7-2A—E and 7-6A). RST and NRST (zone 8-3E) are initiated by NMRSTP at OR gate U16459 or by other inputs to the same gate (zone 8-7F). RST resets the *try counter* (zone 8-6C) that issues load command (NLDC), and the load sequence counter that produces the load counts (NC1,2; C1,2, etc.). Refer to zones 8-3H through 8-7H from where the count signals fan out to other areas.

The preceding paragraphs describe the distribution of the master reset pulse NMRSTP and, in general, the circuits on the Control M2 PCBA where used. The complete functions of the various circuits, other than resetting, are described separately in appropriately titled paragraphs.

5.4.2.5 Interlock Circuits (NINTLK, INTLK, INTLK1, DINTLK, NDINTLK, NINTLKP1, NINTLKP2)

The interlock circuits are designed to inhibit and/or enable various modes on the basis of monitored air and tape conditions. The basic interlock signal is the low = true NINTLK level found at TP62 and P8-69 (Schematic No. 106875, zone 9-1F), and at the NAND gate output (U164-8) where the signal originates. The NAND gate (zone 7-5F) requires a high level at inputs U194-9,10,12, and 13 to produce a low = true NINTLK output level at U164-8. The inputs are controlled by the pressure switches that sense the supply and takeup reel loop limits (SLIMIT and TLIMIT), vacuum pressure (VAC) and positive pressure (ABP). The switches are each connected (via Interconnect F/F1 PCBA; J21, Interconnect D/D1 PCBA, and J8) to their respective pins (J8-1,2,3, and 4) as shown in zone 7-8G. A satisfactory condition causes the corresponding switch to close its circuit to signal ground. This pulls down the level at the respective input to J8. Zones 7-8F,G through 7-5F,G show how these inputs are ANDed at gate output U164-8 to produce NINTLK.

5.4.2.6 9-Track/7-Track Mode Selection Circuits

No provisions are made for 7-track mode.

5.4.2.7 PE/GCR Density Modes

Control M2 PCBA output NPE (low = true) at P8-25 selects Phase Encoded (PE) mode. When NPE is high = false, the GCR mode is effective. (Refer to Schematic No. 106875, zone 4-1G.)

NPE is normally high = false if PE mode is not selected. When PE is selected by placing the front panel DENSITY switch in 1600 position, J10-27 (zone 4-8H) is pulled down. This causes U44-10 to apply a high to U65-13 and (when a high is present at U65-12) U65-11 is low, resulting in a low = true NPE at P8-25. If the transport has no DENSITY switch or equivalent, the unit will work in GCR (NPE will be high = false) unless jumper W4 is installed as shown in zone 4-6H. With W4 in place, density mode may be controlled by host system software at BOT.

If the host system applies a low = true IDDS at the interface, P8-19 (zone 3-8B) will be low; this will apply a low at U65-9 (zone 4-4G), causing the OR gate to override the transport circuits and place the unit in PE mode (NPE low = true). This circuit also initiates the DDI signal (zone 4-1G and 3-8F), producing the interface IDDI signal through P8-17 (zone 3-2D) if the interface driver (U161) is enabled by transport selection (SLTA) from U142-6 (zone 3-5B). A density change can only be implemented at BOT due to ARA considerations. Refer to Paragraph 5.4.2.9.

5.4.2.8 Beginning-of-Tape Interlock (BOT INT)

The BOT INT output at P8-48 (refer to Schematic No. 106875, zone 4-1H) of the Control M2 PCBA to J5-12 of the Read PCBA is a high = true level initiated when the beginning marker on the tape is in register with the BOT optical sensor. At this time a low = true level (NBOT) appears at P8-52 (zone 4-8B) via Interconnect D/D1 and F/F1 PCBAs. The NBOT signal is also applied to various circuits on the Control M2 PCBA as shown or referenced on the schematic (zones 4-6B through 4-2B).

5.4.2.9 Unit Selected Mode (NSLTA)

The NSLTA output at P8-23 of the Control M PCBA (refer to Schematic No. 106875, zone 4-1H) is a low = true level if the host system uses only one transport. It is also low = true while the system is addressing the unit code that has been selected on the transport's front panel thumbwheel selector switch. These circuts are discussed in Paragraph 4.5.2.

5.4.2.10 Tape Load/Rewind and Unload Modes

The tape loading procedure involves all of those steps that result in the tape being installed and brought to the beginning-of-tape (BOT) position. The steps include motion in either or both directions and may include cartridge and pneumatic system control. If a reel of tape has been installed on the supply reel spindle but the sensors determine that the tape has not been threaded through the guides to the takeup reel, normal load conditions exist. Pressing the LOAD/REW button will initiate the automatic threading process, that connects the tape to the takeup reel, forms the loops and stops at BOT. The tape is then ready for a read or write operation.

If tape is sensed between the supply and takeup reels when the LOAD/REWIND button is pressed, a situation called a mid-reel load condition exists, and Rewind mode is initiated. Rewind mode also terminates at BOT. Tape sensor feedbacks are shown in Figure 5-7.

Note that when the UNLOAD switch is depressed, Rewind mode is also initiated if the tape is not at BOT, but the Unload mode causes the tape to travel beyond BOT position until the tape is completely wound on the supply reel. Unload mode then causes the supply reel cartridge to close.

Schematic No. 106875, sheets 10 and 11, contain a flow chart for reel-motion logic by manual control, including motions commanded by means of the LOAD/REW and UNLOAD switches. In the following text the preliminary power-on sequence and the load sequence are discussed with reference to the flow chart and various referenced zones of other sheets of the same drawing. The power-on sequence is included here because it prepares the subject circuits for the tape procedures.

5.4.2.10.1 *Tape Control Presetting by Power-On Sequence*

When power is applied (zone 10-8H), the power-on reset signal (NPORST) is produced. Refer to Paragraph 5.4.2.4. NPORST is applied to Control M2 PCBA J8-61 (zone 4-8C). This is distributed as shown at zone 4-4C and is gated with the manual reset circuits (zones 4-7D—4-4D) to produce the master reset pulse (NMRSTP) at NAND gate output U13-11.

If the tape sensors find tape in the tape path, a high = true TIP signal is received at J8-49 (zone 4-8A) informing the circuits that a load command, when received, will be under mid-reel load conditions. TIP initiates mid-reel load signals MRL and NMRL (zone 7-2D). NTIP, from zone 4-4A, is applied to NAND gate U202-4 to inhibit a close cartridge command (NCCC). MRL goes to P12-38 of the Reel Servo PCBA, where, when low = false, it inhibits the supply reel forward motion mode control signal (NSRF2) until the midreel load procedure is complete (tape at BOT). NMRL is applied to U124-10 (zone 7-2F) to turn pressure on (PSOL) and U125-10 to preset the air control flip-flop (zone 7-7F).

MRL (zone 7-2D) is also applied to NAND gate U194-2 (zone 7-5C) as one of the conditions that preset the first delay flip-flop (U216-4, zone 7-6B). After a delay, U226-9 clocks the flip-flop (U135-3) that produces the set tape loops (STL) command.

When no tape is found in the path, a normal load condition exists. NTIP is high = false, NAND gate U202-4 (zone 9-5A) is enabled for a high output at U182-5 (zone 9-5A) of the cartridge control flip-flop. The other condition for issuing a close cartridge command is

the input CC N.O. at U202-5 from the cartridge open sensor. The NCCC output at P8-70 sets the cartridge mechanism in closed position for installing or removing a reel on the supply hub.

The tape in path signal (NTIP) is also applied to OR gate input U194-3 (zone 9-7E) as one of the conditions for sending the supply reel reverse (SRR) command to the Reel Servo PCBA. Other conditions are sequence counts (NC0, NC1), a false load fault status signal (LDFS) and/or backwrap (BKW), cartridge open (CO N.O.), unload number 1 (UNL1) depending on the mode of operation. SRR will also be inhibited by the suppression of BKW when the set tape loops (STL) process is initiated.

5.4.2.10.2 *Circuits Involved in Tape Load/Rewind/Unload Procedures*

Circuits involved in load, rewind, and unload control are shown in Schematic No. 106875 and are described as follows.

(1) **Clocks.** Basic system clocks (zones 2-1A—2-1H) are based on a crystal oscillator as described in Paragraph 5.4.2.1.

(2) **Load/Rewind Command Pulsing.** Load/rewind command and pulsing circuits (zones 4-7F—4-3F) are initiated by LOAD/REW momentary switch outputs:

Load reset pulse (NLRSTP)	U24-6, zone 4-4F
Load pulse (NLDP)	U46-6, zone 4-2F
Rewind pulse (NREWP)	U46-12, zone 4-2F

(3) **Unload Commands.** Unload command circuits (zones 4-7D,E—4-2D,E) process either a manual command from the control panel UNLOAD switch or a logic command (IRWC at interface, NULC at U45-12, zone 4-4E) and produce unload command number 2 NUNLC2 at U56-12, zone 4-2E.

(4) **Reset Commands.** Reset command circuits (zones 4-7D—4-4C). This is the only command that will interrupt a load procedure. Output is master reset pulse NMRSTP.

(5) **Load Status.** Load status flip-flop that provides the load-in-progress condition for the system. The load status (LDS) level (U135-9, zone 7-2E) participates in setting the backwrap flip-flop (zone 7-2B), sets the thread-mode flip-flop (zones 7-2A,2C), and the set-tape-loops flip-flop (zone 7-2B). These flip-flops then wait for their respective clock inputs. LDS also enables tape and reel motion command gates, etc. (zones 9-2C—E), provided no load fault exists as decided at gate output U165-11 (zone 9-6C).

(6) **Load/Unload Counts.** Load/unload step sequence count control circuits (zones 8-3H—8-7H, and 8-6C). Counter outputs (U215-12,9,8,11) are decoded and produce counts NC0,1,2,3,4,7 at outputs U205-1,2,3,4,5,9, respectively. The counter is incremented at input U215-14 by the output of U195-11 (zone 8-6C), which reflects the low tape sensor input pulses (P8-42, zone 8-8C) divided by 5. The divided count is provided by U185-11 (zone 8-6C). Sensor pulse inputs at U185-1 are inhibited if a load fault exists (NLDFS at U136-2). The divider output (U185-11) is not applied to the load counter (U215-14, zone 8-7H) unless the transport is in load status (NLDS at U195-9, zone 8-6D) or tape-in-path signal (NTIP) is high = false at U195-2 and unload command UNL1 is high = true at U195-1.

(7) **Load Fault Recovery.** Load fault flip-flop (zone 9-7C) issues a high load fault status (LDFS) level at Q output U166-9 and a low load fault status level at Q output U166-8 whenever conditions warrant aborting the procedure. The flip-flop is cleared by master reset pulse NMRSTP at U166-13. In load status (LDS at U166-12) it will be set to produce fault status by the input at U166-11 from fault NOR gate output U126-8. Low inputs to the NOR gate that clock U166-11 are:

U126-1 (TP41)	Load status is terminated by end of count output to U186-8 (zone 8-2F).
U126-3 (TP42)	Try counter outputs U112-12,1,9 are high indicating that two attempts have already been made to load tape. These outputs cause NAND gate output U122-6 to produce a low.
U126-6 (TP28)	The system is at the set-tape-loop mode and the tape loop timer outputs U123-9,8,11 are all high, indicating that time for setting the loops has run out.
U126-11 (TP14)	Failure of load count (NLDC from U195-11, zone 8-6C) or mid reel load (NMRL from U134-6, zone 7-2D) at start count timer flip-flop input (zone 9-7E) and timer inputs U101-2,3 (zone 9-6F), causing U102-10 to send load fault zero (LDF0) to U126-11.
U126-5 (TP32)	Failure of cartridge to open by count C3 as determined by NAND inputs U136-4 and 5 (zone 8-3E).
U126-4 (TP35)	Failure to get proper air pressure and vacuum condition by count C3 as determined by NAND inputs U136-12 and 13 (zone 8-2F). NAOK input at U136-13 is provided by the output of U173-3 (zone 7-6F) on the basis of VAC N.O. and ABP N.O. sensor inputs to P8-3 and P8-4.
U126-12,2 (TP27)	Cartridge problem is determined by NAND output U132-3 on the basis of CO N.O. and CC N.O. inputs to P8-10 and P8-11 (both high) when load pulse (NLDP2) is received at U131-5. These signals are inverted and applied to U132-4,5 (zone 8-5B).

(8) **Tachometer Circuits.** Capstan tachometer signal processing and application circuits, which provide tape speed information feedbacks for optimum speed control, are shown on sheet 6. TACH signals generated by capstan rotation arrive via Interconnect F/F1 PCBA, Interconnect D/D1 PCBA, and P8-53. Signals are shaped to form the tachometer pulse (TACHP) at U104-2 (zone 6-2G) and are sent to the interface ITACH driver (zone 3-2E), provided the tachometer pulse circuits are enabled (TAPEN at U116-12, zone 6-3G). The pulses are applied to flip-flop clock inputs U95-11 and U93-11 and preset input U92-10 (zone 6-3B—D). They are also squared and applied to the velocity decoder and time constant circuits at U85-14. After a 20 μsec delay, the output U116-8 (zone 6-6D) clears the tachometer pulse No. 2 flip-flop (zone 6-3B), providing a squared pulse 20 μsec long (NTAP2) at P8-62. After a 64 μsec delay, the output at U104-10 (zone 6-6C) clears the rewind enabling flip-flop and produces a high at U93-6 (zone 6-2C) and U72-5 (zone 5-6D). The inputs that produce U105-8 output (zone 6-5C) are all high unless jumpered by one of the wires W5 through W10. The time constants selected for connection are determined by model and tape speed rating of the transport, as listed in Table II (zone 1-5H). The output at U105-8, when all inputs are high, changes the state of outputs at U95-9 (zone 6-3D) and U92-5 (zone 6-2D). When the latter output is low, the rewind ramp is terminated (NRWR, zone 5-1B). When the N>80% signal is high = false, it indicates that a tape speed greater than 80 percent has not been achieved, and tachometer enabling signal NTEN is high = false. When 80 percent speed is achieved, these states are reversed. These signals are used in both states (true or false) in the application of acceleration and deceleration (start and stop) ramps and steady synchronous motion. Note that conversion of the tachometer frequency pulses (NTAP2) to analog voltage signals used in the capstan servo summing amplifier is accomplished by circuits on the Capstan/Regulator PCBA. Refer to Schematic No. 104757, zones 2-12C,D—2-9C,D.

(9) **Unload Control.** Unload procedure control circuits are shown in zones 9-8H—9-2B. NUNLC2 (refer to Item 3) presets first stage (rewind) unload command flip-flop (zone 9-6G). Output U146-5 (UNL1) is applied as a condition to various NAND gates as shown in the schematic and to enable the load counter (8-7C). $\overline{Q}$ output U146-6 (NUNL1) provides the reel servo amplifier enable output at P8-34 by presetting flip-flop output U226-5. NUNL1 is also used in the mode circuits (zone 3-6C) and to initiate the rewind pulse circuits (4-7G). NULRW from U133-12 (zone 9-5H) is applied to U71-11 (zone 5-8E) to establish the state of the rewind status circuits. The output of U82-6 (zone 5-5D) is applied to the motion control circuits at U72-9 (zone 5-5E) to start tape motion. When BOT is sensed (BOT at U131-13, zone 9-5H), the rewind part of the process ends, but unload rewinding motion continues until interlock is broken (INTLK low = false at U133-1, zone 9-5H). BOT also is applied to the PNU RET flip-flop at its presetting input NAND gate (U145-10), and clock input U146-11 (zone 9-5G). At C4 count, flip-flop input U146-13 (zone 9-5G) clears the flip-flop disconnecting the PNU RET line, which turns off the blower/compressor motor. When interlock is broken (NINTLK high = false at U225-5, zone 9-3F), U226-5 changes state, disabling the reel servo amplifiers (NRSAE high = false).

5.4.2.10.3 *Tape Load/Unload Procedure Counters*

The tape loading procedure employs two counters: a *try counter* and a *sequencing counter,* which are described in the following paragraphs.

The try counter provides for automatically making a second attempt to start the loading sequence if the first attempt fails, but it inhibits repetitious recycling. The try counter is cleared and reset by an input at U112-2 and 3 (zone 8-3D) from NOR gate output U164-6 (zone 8-8F). Inputs to the NOR gate are the master reset pulse (NMRSTP), load reset pulse (NLRSTP), unload signal (NUNLC2) and delayed interlock (NDINTLK).

The try counter is incremented by a low input at U112-14 that primarily reflects the output of NAND gate U115-6 (zone 8-4D). At sequence count one output (C1), the inputs to the NAND gate are C1, try counter two (T2) inverted, and the inverted NSMRL input. This increments the counter to T1. At NC3 time from the sequencing counter, AND gate input U155-12 is low, U155-11 low and the try counter is incremented to T2. When the counter outputs are high at U112-12 and 9, the output at NAND gate U122-6 is low and reports a load fault at load fault NOR gate U126-3, preventing a third try. The NSMRL input inhibits a second try when a small reel is loaded.

The sequencing counter is reset by the reset (RST) input to the counter at U215-2,3 (zone 8-7H). It is incremented by pulses from the low tape sensor P8-42 (zone 8-8C) after these pulse counts have been divided by five at divider output U185-11 (zone 8-6C). Application of the pulses are on the condition that no load fault has occurred, i.e., the load fault status signal NLDFS at U136-2 (zone 8-7C) is high = false.

The low tape sensor, sometimes referred to as pack sense (PKSN), pulses are the output of an optical detector that senses two reflective tabs placed on the inside of the takeup reel flange. The detector looks at these tabs through two slots in the side of the reel opposite the tabs. Each time the reel turns, two tabs are sensed. This produces two low tape sensor counts per revolution of the reel, provided there is not enough tape on the reel to block the path between the detector and the tabs. In Rewind mode, when the tape on the takeup reel is down to about 9.525 mm (0.375 inch), the low tape sensor begins issuing pulses, the first one of which is used to slow tape motion so the reels can stop at BOT. In forward motion, the pulses are sent to the logic until the tape on the takeup reel is sufficient to block the

sensor path. These pulses, at the rate of two pulses per turn, are sent through P8-42 to U136-1 (zone 8-7C). During the load process, if no load fault exists, NLDFS will be high = false at U136-2 and U136-3 will apply the inverted pulses to U185-1. The output of U185-11 of the divider will be one pulse per five inputs, or one per 2½ turns of the reel, at NAND gate input U195-12. If the transport is in load status (NLDS at NOR gate U195-9) then U195-11 will issue low load count pulses (NLDC). These are applied to the sequencing counter incrementing input U215-14.

The outputs of the sequencing counter are applied to decoder inputs U205-12, 13, 14, 15. Decoder outputs are low at times that correspond to the count as shown inside the box plus 1 (e.g., U205-1 is low at the zero count, U205-2 is low at the first count, etc.). These counts are low = true NC1, NC2, etc. When inverted they are C1, C2, etc. The counts are used to cue the various loading process steps (backwrap (BKW), thread (THD), set tape loops (STL), etc.). Refer to Tables 5-6 and 5-7.

It should be noted that low tape counts at U215-12,1 (zone 8-6H) are applied to U115-1 (zone 8-2G) as well as to the decoder. Similarly, counter output U215-11 is inverted and applied to clock flip-flop (U186-11, zone 8-2F). Flip-flop output U186-9 is applied to NAND gate input U115-2 (zone 8-2G). If BOT is reached, load status ends (LDS low), so U115-12 cannot issue a low fault output. If counts stop before BOT is reached, U115-1 will go low, producing a load fault. Also, counter outputs to the decoder are binary; A = 1, B = 2, C = 4, D = 8. D clocks the flip-flop such that output U186-8 goes high at count 16 (the next binary order). This allows about 92 meters (30 feet) of tape to pass, while searching for BOT, without signalling a time-out load fault.

5.4.2.10.4 *Automatic Tape Loading Sequence*

When the Load command is issued by pressing the LOAD/REW switch, the logic goes through a series of steps based on feedback from status sensors and cued by the sequencing counter. The hardware circuits that make the decisions are shown in Schematic No. 106875, sheets 1 through 9. The logic flow chart for the procedure is in the same drawing, sheets 10 and 11. Sensor feedbacks are shown in Figure 5-7.

If tape is in the path and air status is satisfactory for operation after the LOAD/REW button is depressed, interlocks will be made (refer to Paragraph 5.4.2.5). NDINTLK will be applied (zone 4-3G) and Rewind mode will be commanded by the resulting low = true rewind pulse (NREWP). The tape will stop at BOT, and the load will be completed.

If interlocks are not made when the LOAD/REW command is processed, the automatic load sequence will be initiated by the low = true load pulse (NLDP).

Pulsing is developed by the series of flip-flops (zones 4-3G,F to 7G,F) activated by the LOAD/REW switch. While the momentary switch is depressed, J10-23 is connected to ground, which presets the first flip-flop in the series. The resulting Q output (U26-5) sets the next flip-flop at clock B (CLKB) time. (Refer to Paragraph 5.4.1.1 for system clock details.) When the switch is released, J10-23 is disconnected from ground, U26-4 goes high and U26-1 goes low. This clears the first flip-flop while the second stays in set state until cleared by an unload (NUNL1) or load status (NLDS) signal at NOR gate U145 inputs 2 or 1 respectively.

The Q output at U35-5 applies a high at NAND gate input U24-4 while the $\overline{Q}$ output at U34-6 applies a high to NAND gate U24-5 producing a load reset low = true output (NLRSTP) at U24-6. This is sent to EXCLUSIVE NOR gate input U164-4 (zone 8-8F) to reset the load sequence counters and control circuits. At clock B time, the output of U35-5 (zone 4-6F)

Table 5-6
Load/Unload Sequence Control Count Applications
(Refer to Schematic No. 106875)

Decoder Pin (zone 8-6G,H)	Count* (N = Low)	Distribution/ Zone	Mode	Effect
U205-1	NC0	U222-11/9-7E	Load	Opens cartridge if not open and no fault exists.
		U194-4/9-7E	Unload	Commands supply reel reverse if interlocks are not made (after BOT is reached).
U205-2	NC1	U222-10/9-7E	Load/Unload	Opens cartridge if not open, tape is in path, and no fault exists.
		U125-11/7-7F	Load	If air pressure is ok, issues PSOL command.
		U194-5/9-7E	Unload	Starts supply reel reverse if interlocks are not made (after BOT is reached).
	CI	U115-4/8-4D	Load	Increments Try Counter if a small reel has been sensed and if one try has not already been made.
		U144-3/7-2B	Load	Starts backwrap if in load status, small reel has not been detected, and there is no tape in path (not a midreel load).
U205-3	NC2	U222-9/9-7E	Load/Unload	Opens cartridge if not open and no fault exists.
		U144-11/7-2A	Load	Trailing edge starts threading process if in load status.
U205-4	NC3	U204-1/8-3G	Load	Initiates load fault status: if cartridge is not open; or if air is not ok.
		U145-13/9-6B	Unload	Inverted to C3, closes cartridge if unload is complete, there is no tape in path, and cartridge is open.
		U155-4/7-3B	Load	Clears backwrap flip-flop.
		U155-12/8-4D	Load	Increments Try Counter.
U205-5	NC4	U165-2/8-5G	Unload	Inverts to C4 and goes to U156-13/9-6F to terminate process if in unload status.

*Counts are produced only under the following conditions (zones 8-6C,D—7C,D):

Mode	NLDFS (U136-2)	NLDS (U195-9)	NTIP (U195-2)	UNLI (U195-1)
Load	High = False	Low = True	N/A	N/A
Unload	High = False	N/A	High = False	High = True

Table 5-7
Try Counter Outputs
(Refer to Schematic No. 106875, zone 8-3D)

Try No.	U112-12,1	U112-9	U122-6	Effect
T0 (reset)	Low	Low	High	Enable
T1 (first)	High	Low	High	Permits try
T2 (second)	Low	High	High	Permits try
T3 (third)	High	High	Low	Inhibits try

causes the next flip-flop to change state terminating the NLRSTP pulse (U24-6) and applying its high Q output to NAND gate U54-2 which, while $\overline{Q}$ output at U34-8 is high, causes NAND output U54-3 to initiate a low load pulse (NLDP) at U46-6 (TP18). This pulse is terminated when the Q output at U34-8 changes state at the next clock B time. NLDP is sent to U135-10 (zone 7-2E) to preset the load status (LDS) flip-flop and U134-10 (zone 7-2C) to preset the thread status (THDS) flip-flop. The high Q output at U34-9 causes the next flip-flop to change state at clock B time and is also applied to NAND gate U63-1 (zone 4-2G). When the high $\overline{Q}$ output from U61-6 is applied to U63-2, it initiates a low load pulse two (NLDP2). This pulse is inverted and used as a condition for output of NAND gate U132-6 (zone 8-5B).

If no cartridge is in place or if the cartridge is sensed as neither open nor closed, U132-6 (zone 8-5B) is low, causing a load fault signal at U126-8 (zone 8-1D) and a load fault status level (NLDFS) at the $\overline{Q}$ output (U166-8) of the load fault flip-flop. NLDFS is applied to U136-2 (zone 8-7C) as one of the conditions in the network that issues the load count (NLDC) signal to U215-14 to increment the sequence counter U215, and decoder U205 (zone 8-6H,8-7H). If NLDFS is true = low at U136-2, the reel-turning pulses from the low tape sensor are prevented from entering the divide-by-five chip at U185-1 (zone 8-6C).

If the cartridge is ok, U205-2 (zone 8-6H) issues count C1, which clocks backwrap (BKW) flip-flop U144-3 (zone 7-3B), and NC1, which clocks the air control flip-flop (U125-11) at zone 7-7F. Since, during normal load sequence, interlock is not made (NINTLK at U164-8, zone 7-5F, high = false), U124-8 (zone 7-2F) issues pressure solenoid command (PSOL).

If no load fault exists, U166-8 (zone 9-7C) will be high and U165-11 (zone 9-6B) will be low, clearing the cartridge command flip-flop (zone 9-5A). This causes $\overline{Q}$ output U182-6 to initiate the NCOC command to open the cartridge.

At NC1, the backwrap flip-flop is enabled to be set (by the output of U143-8, zone 7-3C), provided the inputs (U133-9,10,11) are high, indicating that load status (LDS) mode is set (U133-11), a midreel load condition does not exist (U133-10), and the try counter output (U112-9, zone 8-3D) indicates no more than one previous try has been made (U112-9 high).

Load sequence count NC2 is applied to thread command flip-flop U144-11 (zone 7-2A). The NTHD output (U144-8) is sent to U154-9 (zone 9-7D) to initiate the supply reel forward (SRF) command and continue takeup reel forward (TRF) command.

Load sequence count NC3 (zone 8-6H) applied to OR gate U155-4 (zone 7-3B) initiates clearing of the backwrap flip-flop (zone 7-2B). NC3 at U204-1 (zone 8-3H) is inverted to C3 and applied to NAND gate U136-4, which checks the cartridge open signal CO N.O. for a possible load fault. U136-11 (zone 8-2F) similarly checks for air system faults.

When tape appears in the path (BOT or NAOK), U196-12 (zone 7-5C) presets flip-flop U216-4 (zone 7-6B). The succeeding two flip-flops, clocked by CLKE, provide a delayed output at U226-9, which sets the tape loop command (STL) flip-flop. This delivers STL (zone 7-2B) to the reel servo motion commands at zone 9-4D. The takeup reel reverse (TRR) and supply reel forward (SRF) commands provide slack tape to form the loops.

When loops are set and interlock is made (NINTLK at U233-13, zone 9-6F), takeup reel reverse (TRR) and supply reel reverse (SRR) are commanded (zone 9-1C,D). When BOT is sensed, U146-11 (zone 9-5G) is high and output U146-8 terminates motion.

5.5 REEL SERVO PCBA

The Reel Servo PCBA, plugged into J12 on the Interconnect D/D1 PCBA, contains the supply reel and takeup reel power amplifiers that control the speed and direction of reel motion. Refer to Schematic No. 106925.

While the speed and direction of the capstan drive motor determines the motion of tape across the heads, reel motion is a critical factor in tape transport management. Reel motion varies depending on the quantity of tape on the reel, tape tension as determined by tape loop position, and whether the operation is synchronous (SRF, SRR), rewind, or unload. Reel Servo PCBA inputs and outputs are detailed in Tables 5-8 and 5-9. Power amplifiers and outputs to the reel motors are shown on sheet 4 of Schematic No. 106925.

Drive power unregulated ± 36v inputs to the Reel Servo PCBA are through J13, J16 (supply reel + and −) and J17, J20 (takeup reel + and −), respectively. Refer to zones 4-1G, 4-1A.

Outputs to the reel motors are, respectively: supply reel motor +, SM(+), J14; supply reel motor −, SM(−), J15; takeup reel motor +, TM(+), J18; takeup reel motor −, TM(−), J19.

Input signals to the Reel Servo PCBA are through Interconnect D/D1 PCBA and J12, shown at the left-hand side of sheets 2 and 3 of Schematic No. 106925.

Both supply and takeup reel amplifiers are enabled by low = true reel servo amplifier enable (NRSAE) at J12-11 and high = false power-on reset (NPORST) at J12-9,26 (after reset pulse). Refer to zones 2-8F and 2-8E. Gate U10-6 (zone 3-6E) produces amplifier enable (NAE) when low and, when high, initiates the dynamic brake outputs for both reels in both directions (SFBRK, SRBRK, TFBRK, and TRBRK). Refer to zones 2-1D and 2-1E. The brake signals are sent to the amplifiers (zones 4-8F,E,B, and A, respectively). The NAE signal is routed as shown at zone 3-4E as one of the conditions for development of the drive signals, NSDA, NSDB, NTDA, and NTDB (zones 3-1G,F,C, and A, respectively). These are routed to the amplifier circuits as shown in zones 4-8F, for supply reel signals NSDA and NSDB, and 4-8C for corresponding takeup reel signals.

Mode control circuits (zones 2-8E—2-6C) interpret the supply reel (SR) and takeup reel (TR) forward or reverse motion commands (SRF, SRR, TRF, TRR) with respect to whether the tape interlocks (NSINTLK and NTINTLK) are set and whether a midreel load (MRL) operation is in progress. The outputs of the mode control network are applied to the corresponding mode switches shown in zones 3-5B,6B,5F, and 5G.

Reel load-speed adjustment circuits are shown in zones 3-5H,6H and 3-5C,6C. The supply loop position feedback signal (SPOS) is applied to the summing amplifier network through J12-20 (zone 3-8G). Takeup loop position signal feedback is applied to the corresponding takeup reel summing network through J12-3 (zone 3-8B). The offset factor is introduced into the summing networks (zones 3-8F and 3-8A) to reproportion the supply and takeup loops during a rewind operation. The offset signal is developed on the basis of reverse motion signal (REV), J33, and rewind ramp signal (REWR), J13, shown in zones 2-8F and 2-8H, respectively. REWR is developed on the Capstan/Regulator PCBA and REV is provided by the Control M/M2 PCBA. Normal offset adjustment circuits are shown in zone 3-5D, where resistance of potentiometer R76 contributes to the T-wave generator circuits controlled by the park loop gain switch shown near the NDRV input J12-27 (zone 3-8E).

The reel servo inhibit switch (zone 2-6F) provides for disabling reel servo circuits for maintenance purposes.

The 5v regulator network produces the + 5v (A) (zone 2-3C) for the amplifier circuits and the + 5v (S) (zone 2-3D) for all reel servo logic requirements. Zones 2-8B through 2-6A show the + 15v and − 15v inputs to the Reel Servo PCBA circuits.

Table 5-8
Reel Servo PCBA Inputs

Input	Connector	From	Purpose
+ 36v(S)	J13	F7	Supply reel motor power
− 36v(S)	J16	C5(−)	Supply reel motor power return
+ 36v(T)	J17	F6	Takeup reel motor power
− 36v(T)	J20	C5(--)	Takeup reel motor power return
REWR	J12-13	J11-78	Rewind ramp signal from Capstan/Regulator ramp generator
REV	J12-33	J8-66	Reverse command from Control M/M2 PCBA
NRSAE	J12-11	J8-34	Reel Servo enable signal
NPORST	J12-9,26	J11-37,77	Power-on reset signal
NTINTLK	J12-31	J21-10	Takeup loop interlock (TLIMIT signal)
NSINTLK	J12-30	J21-6	Supply loop interlock (SLIMIT signal)
TRF	J12-15	J8-31	Takeup reel forward command
TRR	J12-14	J8-32	Takeup reel reverse command
SRF	J12-17	J8-29	Supply reel forward command
SRR	J12-16	J8-30	Supply reel reverse command
MRL	J12-28	J8-5	Midreel load signal
SPOS	J12-20	J21-37	Supply loop position signal
TPOS	J12-3	J21-21	Takeup loop position signal
NDRV	J12-27	J8-66	Drive reel command
+ 15v(L)	J12-6,23	J11-21,61	Regulated dc from Capstan/Regulator PCBA
0v(L)	J12-4,5,21,22	J11-26,27,66,77	DC ground
− 15v(L)	J12-7,24	J11-14,54	Regulated dc from Capstan/Regulator PCBA
+ 15v(R)	J12-32	Interconnect F/F1 PCBA	Power for position transducer
0v(R)	J12-34		

Table 5-9
Reel Servo PCBA Outputs

Output	Connector	To	Purpose
SM(+)	J14	Supply reel motor	Drive power
SM(−)	J15		
TM(+)	J18	Takeup reel motor	
TM(−)	J19		

5.6 CAPSTAN/REGULATOR PCBA

The Capstan/Regulator PCBA develops the capstan drive motor power inputs CM(−) and CM(+), provides primary regulation of dc voltages, develops the rewind power ramps for the reel servo system, converts capstan tachometer frequency output to proportionate voltages, controls cartridge motor power, and processes vacuum, pressure, and write protect solenoid signals. Capstan/Regulator PCBA circuits are shown on Schematic No. 104757.

The capstan motor drive power is developed from the ±36v unregulated input by the power amplifiers (zone 2-3B) on the basis of inputs through Capstan/Regulator edge connector P11, as shown at the left-hand side of sheet 2. The amplifiers are enabled by the interlock signal (NINTLK) from the Control M/M2 PCBA and power-on reset (NPORST) from the regulator circuits (zone 3-1G to 2-8H).

Application of the start ramp, forward stop ramp, or reverse stop ramp (zone 2-7B,C) is controlled by the output of the mode control circuits (zone 2-7E—2-7F). Direction of application of the start ramp is determined by the output of the forward-reverse switch (zone 2-7D) on the basis of the reverse (REV) signal input (zone 2-12E) as inverted at U7-8 (zone 2-9E). The start ramp is terminated when the capstan speed reaches 80 percent of nominal tape speed. (N > 80% input at P11-25 will be low = true.)

Capstan drive speed is determined by summing amplifier output U9-6 (zone 2-7D) on the basis of tachometer feedback pulse (NTAP2) through P11-57 (zone 2-12D) when the tachometer circuits are enabled (NTEN input at P11-17).

In Rewind mode, the rewind ramp (NRWR) command at P11-38 (zone 2-12B) initiates the rewind ramp generator (zone 2-8B,9B), the output of which is also integrated in the summing amplifier output.

Circuits that execute the cartridge open command (NCOC) and cartridge closed command (NCCC) are shown on sheet 3, starting with the command inputs at zone 3-10D. The active command is applied to the cartridge motor driver amplifier (zone 3-8D). When the driver is enabled (ENBL at Q53, zone 3-8C), the amplifier output is applied to the bases of Q37 and Q38. If the output is high, Q38 is turned off and Q37 turned on. This pulls down the base of Q36, causing it to connect +24v to the CART MTR (+) output at P11-30 and 70 (zone 3-1D). While Q36 is switched on, Q43 is off. If the amplifier output is low, the states of Q36 and Q43 are reversed, in which case the −24v source is connected to CART MTR (+) output. The + sign at the output in this case means *more negative* than the return line designated as CART MTR (−). It may be convenient to think of the CART MTR (+) line as the output line (its electrical polarity indicating the direction of motion with + for forward) and the CART MTR (−) as the return line.

Vacuum transfer command (NXFR) input at J11-39 (zone 3-10B) is a command to redirect the application of the vacuum source by controlling the vacuum valve solenoid. When NXFR is low = true, Q44 (zone 3-4C) is switched off, causing Q45 base to be pulled down. This turns Q45 on, connecting the vacuum solenoid return (VAC SOL RET) to ground.

Reel servo amplifier enable (NRSAE) command provides a low at J11-58, which is inverted and cuts off Q54 (zone 3-6C). This low output of Q54 then turns on Q46. This applies a high to NOR gate inputs U11-1 and 2. The inverted output at U11-3 is a low = false file protect (FPT) status signal. The high output of Q46 also turns on Q47, connecting the write protect solenoid return (WP SOL RET) line to ground. If the write enable ring is in place, WP N.O. input at J11-69 (zone 3-10B) is high. The high input is regulated in VR7 (zone 3-7B) and applied to the base of Q46. This turns Q46 off causing a low at NOR gate inputs U11-1,2 and

a high = true FPT output at J11-19 (zone 3-1B). The Q46 low output also turns Q47 off. This disconnects the write protect solenoid return line from ground, causing the WP N.O. input at P11-69 to continue until the circuits are reset. P11-79 input is not used on the subject model.

The upper half of sheet 3 contains the regulation circuits, which are covered in the Regulation and Distribution text, Paragraph 5.3.9.

5.7 WRITE PCBA

The Write PCBA processes the data received from the host system or MIA, controls the write heads, and checks the read data to provide the Amplitude Track In Error (AMTIE) status signals.

The Write PCBA plugs into J7 on the Interconnect D/D1 PCBA. Figure 5-9 is a block diagram of circuits on the Write PCBA. Circuit details are provided in Schematic No. 107860. Write PCBA interface signals are listed in Table 5-10.

Sheet 1 of Schematic No. 107860 provides hardware commonality and general notations; Sheet 2 shows the general mode control and power circuits, including the development of the pedestal-and-step waveforms used for greater recording efficiency; Sheet 3 shows the write data inputs, registers, and data strobe clock development (upper areas) with the parity bit channel and erase head circuits (lower areas).

Sheets 4 and 5 provide circuits for amplifying and preparing data for recording in channels 0 through 7; Sheets 6, 7, and 8 show the development of the Amplitude Track In Error (AMTIE) signals.

The following paragraphs give further details on the circuit theory for each of these groups of circuits.

5.7.1 WRITE CONTROL AND POWER CIRCUITS

5.7.1.1 Write Status Mode

Write Status mode control circuits are shown in the upper left hand area of Sheet 2, Schematic No. 107860. Inputs involved are IWINH, NWRT, NPORST, WRTCUR, and WRTPWR (zones 2-8F,G,H).

The control circuits are reset when the power-on reset signal (NPORST) is momentarily low = true. This opens Q1 (zone 2-7G) and Q3 (zone 2-8H). When Q1 is not conducting, Q2 and Q5 are also open. When Q3 is not conducting, Q4 and Q6 are similarly open. This terminates any previous mode until NPORST goes high = false.

When the write command arrives (NWRT low = true), U112-12 (zone 2-8G) is high, U122-6 (zone 2-7G) is low and, through Q1, the base of Q2 is pulled down. This causes Q2 to conduct and apply a high to the base of Q5. Q5 then conducts, enabling Write Current (WRTCUR) circuits.

5.7.1.2 PE/GCR/Test Modes

Phase Encoded (PE) mode is commanded when the NPE input to the Write PCBA is low = true and Group Coded Recording mode is commanded when NPE is high = false. This input is shown on Schematic No. 107860 zone 2-8E.

When NPE is true, U112-10 (zone 2-8E) is high, producing the PE1 mode control signal. This signal is distributed as shown in zone 2-7E.

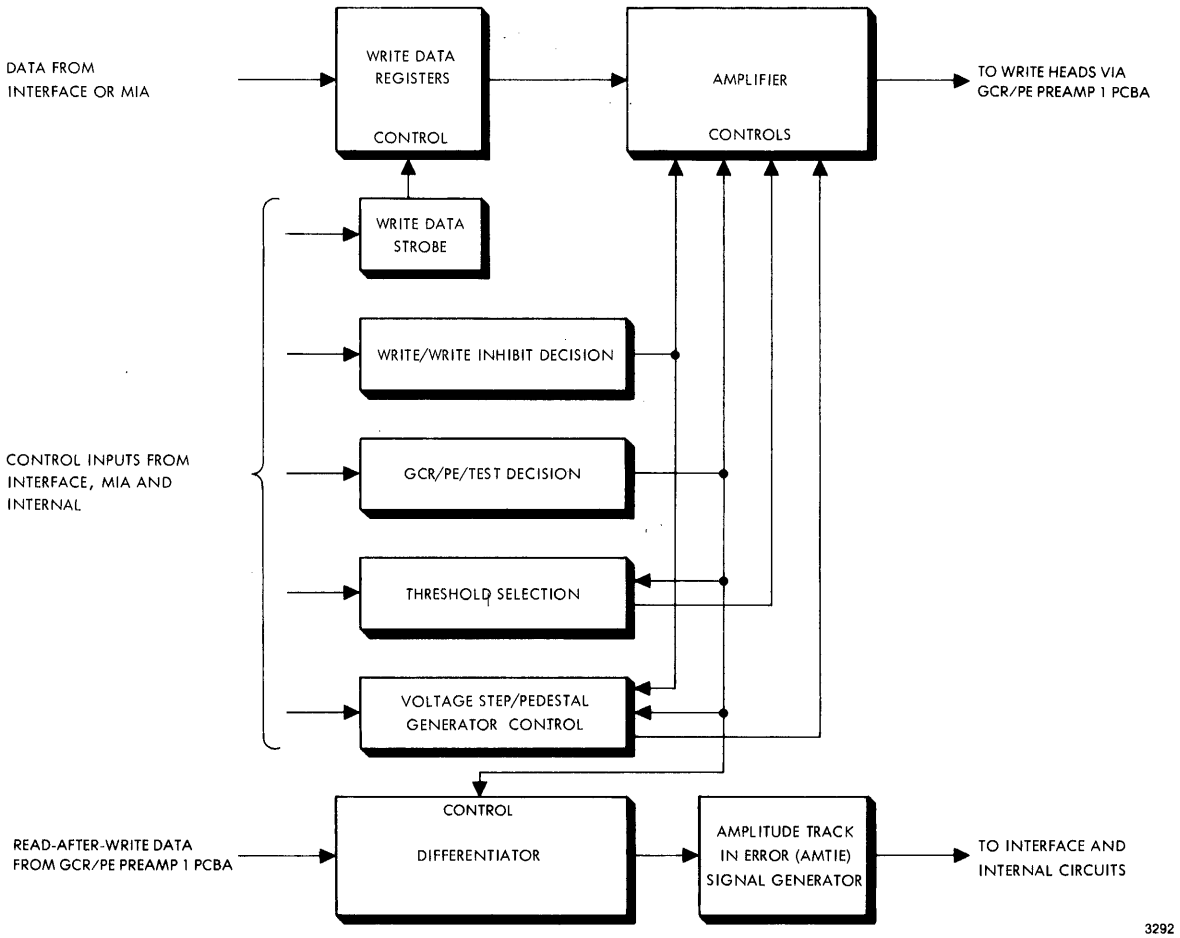


Figure 5-9. Write PCBA Block Diagram

When NPE is high = false, GCR mode is effective. GCR1 (zone 2-5E) and GCR3 (zone 2-5F) are distributed as shown to set up the circuits for GCR-formatted data.

Test mode is established when NTEST (zone 2-8E) is low = true. It is inverted at the output of U112-2 (zone 2-3A) to provide the high = true TEST signal which, applied to NAND gate input U102-10 (zone 2-2A), enables test strobe input NTSTR (zone 2-8D) to clock test data (TSTDAT) from Q output U1-9 (zone 2-1B). TSTDAT is used to supply simulated data to all channels of the write data registers (zone 3-5E—H).

5.7.1.3 Write Power

The + 15v dc input to the Write PCBA from J7-58,22 on the Interconnect D/D1 PCBA (zone 2-8C,D) is applied directly to the Voltage Step (VSTEP) and Voltage Pedestal (VPED) circuits, if jumper W3 (zone 2-6D) is used. If jumper W4 (zone 2-7D) is used, the voltage is reduced by diodes CR11 through CR14 and regulated by VR3 (zone 2-5C,6C). The Write Power Regulated (WRT REG) is applied to Q7 (zone 2-2H) and Q11 (zone 2-2E). The outputs of Q7 and Q11 are controlled by threshold selection signal (refer to Paragraph 5.7.1.5) applied to the bases of Q7 and Q11. The resulting VSTEP and VPED signals are further modified by the step and pedestal generation described in Paragraph 5.7.1.4.

Table 5-10
Write PCBA Interface

Mnemonic	Connection	From/To	Purpose
WP1	J7-60,24	P21-29,32	Write power
NPE	J7-61	J8-25	High Density (low = true) signal selecting PE format from Control M/M2 PCBA
NWRT	J7-25	J8-26	Write command (low = true) from Control M/M2 PCBA
MOTION	J7-26	J8-28	Signal from Control M/M2 PCBA specifying that tape is rolling
IWARS	J7-46	J102-C	Write amplifier reset from system interface
IWDS	J7-47	J102-A	Write data strobe from system interface
NTEST	J7-56	J1-22	Test command from Test PCBA to initiate test mode
NTSTR	J7-20	J3-19	Test command to establish read-only mode
IWDP	J7-45	J102-L	Data parity bit
IWD0	J7-44	J102-M	Data bits of 8-bit byte
IWD1	J7-43	J102-N	
IWD2	J7-42	J102-P	
IWD3	J7-41	J102-R	
IWD4	J7-40	J102-S	
IWD5	J7-39	J102-T	
IWD6	J7-38	J102-U	
IWD7	J7-37	J102-V	
+5v(T)	J7-21,57	J204-1,18 W1-2, W2-2	Termination voltage (optional host system voltage for data receivers/drivers)
0v(I)	J7-1—10	See Table 5-1	
+5v(L)	J7-18,19,54,55	J11-22,23,62,63	Logic power from Capstan/Regulator PCBA
0v(L)	J7-15,16,17,51,52,53	J11-26,27,66,77	
+15v	J7-22,58	J11-21,61	Power for erase head amplifier
−15v	J7-23,59	J11-14,54	Power for erase head amplifier
POP CHP/NA	J7-64	J5-49	Read data bits used as pointers for channels (P,0—7). From GCR/PE Preamp 1 via Read PCBA. Used for developing the Amplitude Track In Error (AMTIE) signals.
PO0 CH0	J7-65	J5-50	
PO1 CH1/NA3	J7-66	J5-51	
PO2 CH1/NA4	J7-67	J5-52	
PO3 CH3/NA5	J7-68	J5-53	
PO4 CH4/NA6	J7-69	J5-54	
PO5 CH5/NA7	J7-70	J5-55	
PO6 CH6/NA8	J7-71	J5-56	
PO7 CH7/NA9	J7-72	J5-57	
IWINH	J7-49	J204-20	Write inhibit signal
NPORST	J7-11	J11-37,77	Power-on reset signal
WRTCUR	J7-60		Write current
WRT PWR	J7-13		Write power
NPE	J7-61	J5-10	NPE/GCR density select
MOTION	J7-26	J8-28, J5-48	Tape Motion Command
NTEST	J7-56	J1-22, J5-60, J8-36	Test mode
DCH3/NARA	J7-32	J5-17	Automatic read amplification signal
NTSTR	J7-20	J3-19	Test data/strobe
+10v	J7-48,12	J5-23	
−10v	J7-14,50	J5-24	
IWDS	J7-47	J102-A, J2-34, J202-34	Write data strobe
IWDP	J7-45	J102-L, J2-25, J202-25	Write data
IWD0	J7-44	J102-M, J2-24,J202-24	
IWD1	J7-43	J102-N, J2-23, J202-23	
IWD2	J7-42	J102-P, J2-22, J202-22	
IWD3	J7-41	J102-R, J2-21, J202-21	
IWD4	J7-40	J102-S, J2-20, J202-20	
IWD5	J7-39	J102-T, J2-19, J202-19	
IWD6	J7-38	J102-U, J2-18, J202-18	
IWD7	J7-37	J102-V, J2-1, J202-1	

5.7.1.4 Voltage Pedestal (VPED)/Voltage Step (VSTEP) Circuits

The terms voltage pedestal and voltage step refer to the shape of the write current waveform of a data bit. Theoretically, a series of 1s and 0s would involve a simple squarewave signal composed of square pedestal-like waves in alternating upright and inverted position. In practice, greater efficiency is achieved by overshooting the pedestal level at the beginning of each wave. This produces a waveform composed of squarewaves with an added step more positive than the pedestal amplitude of positive waves and more negative than the pedestal amplitude of negative waves.

In GCR mode, the amplitude of the pedestal is adjusted by trimming R39 (zone 2-1D) and the amplitude of the step is adjusted by trimming R22 (zone 2-1G).

In PE mode, R36 (zone 2-1E) is used to trim the pedestal amplitude and R19 (zone 2-1H) is used to trim the step amplitude.

Which of the PE and GCR adjustments described in the two preceding paragraphs is used, is determined by the operational mode selection. In PE mode, the base of Q10 (zone 2-4E) is high, which turns Q10 off. This applies the low = true NPE2 signal to the various circuits listed in zone 2-3F and also to CR8 (zone 2-3G) and CR10 (zone 2-3D). CR8 and CR10 then conduct, pulling down the gates of the FET Q14 (zone 2-3G) and Q15 (zone 2-3D), respectively. Q14 and Q15 then open the circuits adjusted by R22 (zone 2-1G) and R39 (zone 2-1D).

In GCR mode, a low is applied to the base of Q10 (zone 2-4E). Q9 is then turned off, which selects the GCR adjustment circuits (R39 and R22). The circuits involved operate on the same theory as that discussed in the previous paragraph.

5.7.1.5 Threshold Selection

The threshold selection circuits are shown in zones 2-4B and 2-5B of Schematic No. 107860. These circuits regulate the +VAM to a level determined by the threshold selection (NLTH or STDTH at J2-5 and J2-15, respectively). When STDTH (Normal Threshold) is high = true, VR6 regulates the +VAM at approximately 6.0v. When NLTH (Low Threshold) is low = true, VR5 regulates the +VAM at approximately 4.3v. VR4 regulates the +VAM to assure approximately 10v maximum. The regulated voltage is applied to the AMTIE circuits.

5.7.2 WRITE DATA REGISTERS AND STROBES

The write data inputs and strobe circuits are shown in the upper area of Sheet 3 of Schematic No. 107860.

Input data IWDP, IWD0—7 are delivered to the Write PCBA through J7 of the Interconnect D/D1 PCBA and are stored in registers U11, U31, and U41 (zones 3-5D-5H). The Write Data Strobe (IWDS, zone 3-7H) is made available through U41-11 and U41-9 as Clock 1 (CLK1) to U99-2 (zone 3-3G) and U99-10 (zone 3-3E), where the signal is low when true. At the trailing edge, when the CLK1 signal goes high, it triggers either the GCR or PE one-shot, depending on the state of the GCR1 and PE1 mode inputs. If PE1 at U99-1 (zone 3-3G) is low = false, the GCR one-shot output at U99-4 will be high for a period determined by the values of C11 and R48. Conversely, if GCR1 at U99-9 is low = false, the PE one-shot output at U99-12 is high for a period determined by the values of C12 and R50. These one-shot outputs are applied to NAND gate inputs U102-5 and 4 (zone 3-2G), respectively. The NAND acts as an OR function to produce a high if either of the inputs is low. This high is inverted at U92-10 to produce data strobe Clock 2 (CLK2) at zone 3-1G.

CLK1 (zone 3-3G), which is high = true (equivalent to the IWDS strobe) from U41-9 (zone 3-5G), is applied to the pedestal (VPED) flip-flop of all data channel and the parity channel amplifiers (e.g., U52-3, zone 3-7C). CLK2 (zone 3-1G) is applied similarly to the step (VSTEP) flip-flop (e.g., U52-11, zone 3-7C). The write data amplifier circuits are discussed in Paragraph 5.7.3.

5.7.3 WRITE CURRENT DRIVERS CIRCUITS

All write current drivers and head control networks, including the parity bit channel network, operate on the same theory. In this discussion the parity bit circuits are referenced as an example. These circuits are in the lower part of Sheet 3 of Schematic No. 107860.

Write voltage (VWRT) is applied to the center tap of the head winding (zone 3-2C and 3-3B). This is approximately −15v dc. The direction of the magnetic flux then depends on whether the circuit through the coil is toward head connector pin 5 or pin 14. This is determined by the state of Q19 (zone 3-4B) and Q18 (zone 3-4C). If the data bit at U52-2 (zone 3-7C) is low at CLK1 time, U52-5 will be low and Q18 will conduct. If the data bit is high, U52-6 will be low, and Q19 will conduct. The VSTEP level is applied during part of the pulse time by the EXCLUSIVE OR gate output at U53-6 (zone 3-6B). This output is buffered and applied to the base of Q17 (zone 3-5G), which gates in the VSTEP level. The U53-6 output is low at all times unless one and only one of its two inputs (U53-4 or U53-5) is high. The output at U52-5 (zone 3-7C) is applied to U53-4 and also to adjacent U52-12. If U52-5 is high, U53-6 will also be high until CLK2, when U52-9 and U53-5 will go high, producing a low at EXCLUSIVE OR gate output U53-6. If U52-5 is low, at the next CLK2 time U52-9 and U53-6 will be high until the succeeding CLK2 time. For each bit, 1 or 0, there will consequently be a discrete time when EXCLUSIVE OR gate output U53-6 will apply a high to the base of Q17 (zone 3-5D) to gate in the VSTEP voltage level.

Each of the other input data bits, IWD0—7, are processed in the same manner as the parity bit, IWDP, discussed in the previous paragraph, and provided also that the Write Inhibit (IWINH) signal is not low = true.

When IWINH is true, a low applied at J7-49 (zone 2-8H) causes U51-8 to go high, U122-10 to go low, and U122-8 to go high. If Q3 is conducting, this applies a high to the base of Q4, turning Q4 off and, consequently, Q6 off. This enables the Write Status (WRT STAT) signal to go high if Q5 is off and prevents writing regardless of the previously mentioned write command and power inputs by removing the negative voltage to the center tap of the heads (VWRT).

The MOTION input to the Write PCBA (zone 2-8E) is also required to establish the write mode. When MOTION is low = false, RESET1 and RESET2 (zones 2-1C,B) are also low = false. They are applied to the channel latches, such as U52-4 (zone 3-7C) and U52-10 (zone 3-7B) for the parity channel and U22-4 and U22-10 (both in zone 4-6G) for write data bit 0 (WD0). When the MOTION input (zone 2-8E) is high = true, it provides the MOTION status output at zone 2-4G and also, through U102-11 and U112-4 (zone 2-6E), provides the Amplitude Track In Error (AMTIE) enable signal (AMNABL). Note that U102-11 output is high if either the MOTION or NTEST input is low; therefore, NTEST must be false (high) and MOTION true (high) to produce AMNABL.

5.7.4 ERASE HEAD CIRCUITS

The erase head circuits are shown on Schematic No. 107860, zones 3-2A,B through 3-4A,B. The regulated write voltage (WRTREG) is available at diode CR25 (zone 3-3A) and passes through the erase head winding when the erase head low (ERHDLO) line is low. ERHDLO is developed in the Write/Write Inhibit mode circuits (zone 2-5G) and is high during Read Only mode, to prevent erasure of existing data unless new data is to be written.

5.7.5 AMPLITUDE TRACK IN ERROR (AMTIE) CIRCUITS

Amplitude Track in Error (AMTIE) signals are generated on the Write PCBA from read data and are used to notify the error checking and correction circuits of marginal or inefficient data.

Data received by the Read PCBA for processing is also routed through the Interconnect D/D1 PCBA to J7 into which the Write PCBA is plugged. At the Write PCBA inputs the data from the channels are labeled as pointers (POP, PO0—7) as shown at the left side of sheets 6, 7, and 8 of Schematic No. 107860. The following discussion uses the parity channel as an example, starting with POP (zone 6-8G).

POP data bits are applied through C13 and R153 to differentiator input U132-1 (zone 6-7G). The differentiator operates in either GCR or PE mode, depending on the circuitry set up between U132-4 and U132-7. The circuit selection is made by mode selection signals NPE2 and NGC (zones 6-2F). When Phase Encoded mode signal NPE2 is low = true, Group Coded Recording mode signal NGC will be high = false. These inputs cause Q44 (zone 6-6G) to open and Q45 (zone 6-6F) to close, disconnecting the GCR timing loop (containing R162 and C16) from the circuitry between differentiator pins U132-4 and U132-11. Similarly, when NGC is low = true, Q44 closes, Q45 opens and the PE timing loop (containing R161 and C16) is disconnected from the circuitry.

Differentiator outputs U132-8 and U132-7 correspond to the voltage differential in time (dv/dt) of the input at pins 1 and 14. U132-8 provides positive going transitions to U134-10 (zone 6-4G) and U132-7 provides negative going transitions to U134-5. U134 outputs 7 and 12 are connected, wire-ORed and applied to the input circuits for both U138-1 and U138-13. The output of U138-2 is delayed, for a time determined by the values of R171 (zone 6-3H) and C23 (zone 6-3G), and applied to NAND gate input U148-1. The output of U138-12 is similarly delayed, for a time determined by the values of R170 and C22, and applied to NAND gate input U148-13. The respective NAND gates are selected by the enabling inputs (PE1 or GCR3) at U148-2 and U148-12. If either of these enabling inputs is low = false, the associated output (U148-3 or U148-11) will be high. When one of the enabling inputs (U148-2 or U148-12) is high = true, the associated NAND gate output will depend on whether the other input (U148-1 or U148-13) is high or low. If high, the output of the enabled NAND gate will be low, U148-6 will be high, and U149-3 will initiate a low = true IAMTIEP signal.

IAMTIE0—7 signals are similarly generated in the appropriate circuits shown on sheets 6, 7, and 8 of the schematic.

5.8 READ PCBA

The Read PCBA performs the following functions:

(1) Accepts data from the read heads via the GCR/PE Preamp 1 PCBA

(2) Decodes the signals in either PE or GCR mode to provide the host system or MIA with the read data in usable form

(3) Operates the automatic gain control (AGC) function in conjunction with the GCR/PE Preamp 1 PCBA

(4) Supplies the Write PCBA with read data for use in the generation of Amplitude Track In Error (AMTIE) signals

Table 5-11 lists Read PCBA inputs and outputs.

The Read PCBA plugs into J5 on the Interconnect D/D1 PCBA. Read PCBA circuits are shown in Schematic No. 107855, which is referenced in the following paragraphs.

Table 5-11

Read PCBA Interface

Mnemonic	Connection	From/To	Purpose
NPE	J5-10	J8-25, J7-61	NPE/GCR select
NWRT	J5-47	J8-26, J7-25	Write mode
IRTH2	J5-1	J102-F, J2-29, J202-29	Low threshold mode
MOTION	J5-48	J8-28, J7-26	Tape motion signal
NTEST	J5-60	J1-22, J103-6, J8-36, J7-56	Test mode
BOT	J5-12	J8-48	Beginning of tape
5v(T)TERM	J5-43,7	W1-2, 2-2	Terminator voltage
+ 5v(L)	J5-8,9,44,45	J11-22,23,62,63	Logic voltage
GND	J5-3,4,39,40,36,35,34, 33,32,31,29,28,27,26	—	—
+ 15v	J41,5	J11-21,61, J5-5,41, J7-22,58, J8-56, J12-6,23, P21-39	—
+ 10v/NSEL	J5-22,23	J1-20	—
− 15v	J5-6,42	J11-14,54, J7-23,59, J8-55, J12-7,24, P21-33,36	—
− 10v	J5-24,25	J7-14	—
SRD/NSLTA	J5-46	J8-23	Read select
LATE AGC/NTSKEW	J5-37	J1-21	Automatic gain control
NARA/DCH3	J5-17	J7-32, J204-30	Automatic read amplification signal
IRDP	J5-72	J103-1, J3-34, J203-34	Read data
IRD0	J5-70	J3-32, J203-32	
IRD1	J5-69	J103-4, J3-31, J203-31	
IRD2	J5-68	J103-8, J3-27, J203-27	
IRD3	J5-67	J103-9, J3-26, J203-26	
IRD4	J5-62	J103-14, J3-21, J203-21	
IRD5	J5-61	J103-15, J3-20, J203-20	
IRD6	J5-59	J103-17, J3-18, J203-18	
IRD7	J5-58	J103-18, J3-1, J203-1	

Sheet 1 provides general hardware and commonality information; Sheets 2 and 3 cover mode control, power, timing and reset circuits; Sheets 4, 5, and 6 contain Automatic Gain Control (AGC) circuits for each of the nine channels; and Sheets 7, 8, and 9 cover the main decoding, amplifying and processing circuits for each of the nine data channels.

The following text gives further details on the circuit theory for each of these groups of circuits.

5.8.1 READ PCBA CONTROL AND POWER CIRCUITS

The following discussions of the various Read PCBA control and power circuits refer to cited zones of Schematic No. 107855.

5.8.1.1 Read Mode Control

Read mode control is based on a high = false Write command (NWRT, zone 2-8G). Because of the read-after-write feature, the transport reads at all times, so the read mode is essentially a read only operation in which the writing and erasing functions are inhibited. A high = false NWRT signal at U15-3 (zone 2-7G) is inverted twice to produce a high = true READ signal at U15-10. The READ signal, together with WRT (Write), GCR4, and the low threshold (NLTHR) selection signal (all in zone 2-7G) are used to establish the appropriate threshold voltage (VTH, zone 2-1E).

5.8.1.2 Phase Encoded (PE) and Group Coded Recording (GCR) Mode Control

PE and GCR modes are applied to the Read PCBA circuits as shown on sheet 2 of Schematic No. 107855. The input command is NPE (zone 2-8G) from the Control M/M2 PCBA. NPE is basically the Phase Encoded mode command. When low = true, PE mode is selected; when high = false, GCR mode is selected.

In PE mode, the inverted output at U15-2 (zone 2-7G) is high. This is applied to various threshold voltage control gates (zones 2-5H,G, and E) and to the base of Q5 (zone 2-2D). This turns off Q5 and produces the low = true NPE1. NPE1 is distributed to various parts of the Read PCBA, as listed in zone 2-1C, to set up the circuitry for Phase Encoded mode.

When NPE (zone 2-8G) is high = false, GCR mode is effective. The output of U15-12 is the high = true GCR4. This is applied to various threshold voltage control gates (2-5F,E, and D), to the base of Q6 (zone 2-2B), which closes to produce low = true NGCR, and also to the reset/preset circuits (zone 3-7D and 3-2D).

5.8.1.3 Read Interface Terminator Voltage

The interface terminator voltage (+5v(T)) may be either at the logic level (nominal +5v(L)) or the host system interface level (+5v(I)) as determined by the installation of jumper W1 or W2 (zone 2-7E).

5.8.1.4 Read PCBA Power Circuits

Read PCBA power circuits are shown in the lower left corner of sheet 2. The ±15v and ±10v inputs are combined through CR4—13 (zone 2-8C) and regulated by VR1 (zone 2-6C) and VR3 (zone 2-7C) to provide ±5.6v dc for the logic circuits. VR2 and VR3 provide the ±5.1v dc voltage for the automatic gain control (AGC) circuits (sheets 4, 5, and 6).

5.8.2 AUTOMATIC GAIN CONTROL (AGC) CIRCUITS

The Read PCBA AGC function is initiated by circuits shown on sheets 3 and 4 of Schematic No. 107855.

Initiation requires all high inputs at U26-9—11 (zone 3-7D). This occurs after the beginning-of-tape mark is passed (NBOT high = false), in GCR mode (GCR4 high = true), and non-test mode (U22-8 high). Under these conditions, U26-8 (zone 3-7D) is low, which clears the binary counters (U30-2,12, zones 3-5 E and 3-5D) and also produces a high at U27-13 (zone 3-6D) and U24-4 (zone 3-7F). The latter resets the timer, which generates counts at its output (U24-3, zone 3-6F) at a rate determined by the values of R34, R35, R36, and C20. Potentiometer R35 (zone 3-7F) is used to adjust the timer.

The timer output is applied through U28-2,3,9, and 8 to the control counter clock input, U30-1 (zone 3-6E). Counter outputs U30-6,5,4,3 (D,C,B,A, respectively) express the number of counts in binary terms.

At the eighth count (1000_2), the D output (U30-6) begins clocking the second counter in the U30 chip, producing a similar binary count at outputs U30-8—11.

Two similar counting arrangements are used in each data channel of the AGC circuits (e.g., U105, zone 4-6H,G and U106, zone 4-4H,G). One of these two counters (e.g., U105) is a data bit counter used to issue the ALLSET signal when 128 bits of the automatic read amplifier burst has been received within one gain setting (e.g., POP input, zone 4-8G). The other counter (e.g., U106) incrementally adjusts the gain of the AGC output (zone 4-1H) until the ALLSET counter (e.g., U105) times out, disabling NAND gate output U104-11 (zone 4-6H) by applying a low at input U104-12.

Set 1 clocks (ST1CLOX) counts (e.g., U104-13, zone 5-6H) are provided by U29-3 (zone 3-5F) on the basis of the timer output, U24-3 (zone 3-6F), except on those counts when the counter output at U30-10 (zone 3-5D) is high. On these same counts, the U30-10 output clears the ALLSET counters (e.g., U105-2,12, zone 4-6H,G) for another try.

As long as the ALLSET signal is low = false on any of the channels, the +5v input at U31-13 (zone 3-4B) is pulled down and, through U31-12, U28-13,11, U27-11,13 (zone 3-6D), the timer RESET input (U24-4, zone 3-7F) is kept high and the timer continues to run. When all channel ALLSET signals are high = true the input to U31-13 is high and the timer is turned off. The timer is also turned off temporarily before a retry whenever the counter output at U30-9 (zone 3-5D) is high. This latter output also generates an Automatic Read Amplifier signal (NARA), indicating an unsatisfactory condition, through U28-5,6 (zone 3-3C) and U23-1,3 (zone 3-2C).

If all channels do not report a satisfactory ALLSET status before count 28, counter outputs U30-11,6, and 5 will be high. These are applied to NAND gate inputs U26-1,2,13 (zone 3-5D). The output produces the LATE AGC signal (P5-37, zone 3-1C), indicating that all bits of an all-1s test/control character have not arrived in the required time frame. This output is also one of the conditions for U26-6 (zone 3-3C) to issue the NARA unsatisfactory signal and U32-11 to cause Q7 to conduct, switching to PE mode. When GCR4 (zone 3-3E) is low = false, Q7 is also caused to conduct and switch to PE mode.

5.8.3 READ AMPLIFIER/DECODER CIRCUITS

The read track output amplifier/decoder circuits for the nine channels are shown on sheets 7—9 of Schematic No. 107855. The following discussion of the theory refers to the parity channel network, which is typical of the nine channels.

Connector pins J4-10 and J4-27 (zone 7-8G) are connected to the GCR/PE Preamp 1 PCBA. This PCBA preamplifies the current flowing between the respective ends of the parity track read head winding. The inputs at J4-10 and J4-27 are applied through C130 and C131 to preamplifier inputs U101-14 and U101-1, respectively.

GCR or PE differentiation characteristics are determined by the circuits between preamplifier pins U101-4 and U101-11. These pins are connected through either Q131 (zone 7-5F) or Q130 (zone 7-6F), depending upon mode selection signals NGCR or NPE1 (zone 7-5F). If NGCR is low = true, Q131 is turned off and PE resistor R136 and capacitor C139 are effectively removed from the circuit between U101-4 and U101-11. If NPE is low = true, Q130 is turned off and GCR resistor R137 and capacitor C138 are ineffective.

The two amplifier outputs U101-8 and U101-7 (zone 7-6G), associated respectively with inputs U101-14 and U101-1, are applied to differential comparator/sensor inputs U102-1 and U102-2 (zone 7-3G), and the essentially sinusoidal signal is changed to a squarewave signal. When the output at U102-4 (zone 7-3G) goes low, it is applied to the driver AND gate input U1-1. U1-3 will issue a low = true interface read data parity IRDP bit.

The same theory applies to the circuits for other data channels, as shown on sheets 7, 8, and 9 of Schematic No. 107855.

The IRDP,0—7 bits are sent to the MIA connector or to the alternate interface connectors via the Interconnect D/D1 PCBA. These signals are interpreted only as true = low or false = high at this point in the system. A true = low bit indicates a flux change away from the direction of the magnetization of the interblock gap (IBG) and high = false indicating a flux change toward the direction of the magnetization of the IBG. The IBG magnetization is such that the end of the IBG nearest to the rim end of the tape is a northseeking pole.

Whether a true = low or false = high bit should be interpreted as a 1 or a 0 is determined by the F6250 Formatter, or comparable external unit, depending upon whether the system is in GCR or PE mode.

5.9 GCR/PE PREAMP 1 PCBA

The GCR/PE Preamp 1 PCBA, located at the rear of the transport base assembly, provides first stage amplification for read data and acts as interconnection between the Write and Read PCBA and the heads.

The GCR/PE Preamp 1 PCBA regulates the ± 15v dc inputs from the Capstan/Regulator PCBA to obtain + 5 and − 6v dc for its differential amplifiers. The GCR/PE Preamp 1 PCBA is illustrated in Figure 6-14. Circuits are shown on Schematic No. 107850.

5.10 INTERCONNECT D/D1 PCBA

The Interconnect D/D1 PCBA is the vertical board that provides the interconnections between the various logic boards in the card cage. The Interconnect D/D1 PCBA is illustrated in Figure 5-1 and connections provided by the PCBA are listed in Table 5-1.

5.11 INTERCONNECT F/F1 PCBA

The Interconnect F/F1 PCBA, mounted at the rear of the transport base assembly, provides interconnections between the card cage logic circuits and the controls, sensors, and indicators on the base assembly. Circuits for the Interconnect F PCBA are shown on Schematic No. 107189. Circuits for the Interconnect F1 PCBA are shown on Schematic No. 107307. Connections are made through J21 on Interconnect D PCBA ribbon cable to terminal boards 1 through 4 on the Interconnect F/F1 PCBA. Interconnect D1 provides J24 for connection/disconnection of the ribbon cable at the Interconnect D1 end of the cable.

5.12 SELF TEST PCBA

The Self Test PCBA is an auxiliary assembly used for testing the reading and writing performance of Pertec T1000 series transports. The PCBA has three edge connectors, that plug into J101, J102, and J103, respectively, on the Interconnect D/D1 PCBA.

5.12.1 CONTROL PANEL

Test controls and the skew indicator, mounted on the panel on the front edge of the board, serve the following purposes:

Panel Name	Purpose
SKEW	Lights to indicate unsatisfactory write skew performance when running prerecorded skew test tape.
TEST OFF-ON	Enables test circuits.
MOTION REV-FWD-RWD	Selects synchronous reverse, synchronous forward, or rewind mode of tape motion.
ENABLE RESET-GO	Resets motion and mode flip-flops or initiates motion.
MODE RD-WRT	Selects between transports read only or write and read mode.
DENSITY 800-6250-1600	Selects NRZI (800), GCR (6250), or PE (1600) density mode (NRZI is not used in subject transports).
SPEED 75-125	Conditions Self Test PCBA for transport tape speed.

5.12.2 INPUTS AND OUTPUTS

Inputs to the Self Test PCBA are the skew feedback signal (NTSKEW/LATE AGC), which controls and drives the SKEW indicator (CR1) and the 5v logic power. (Refer to Schematic No. 104962, zones 2-8G,H through 2-3G,H.) NTSKEW/LATE AGC is from the Read PCBA (refer to Schematic No. 107855, zone 3-1C).

Mnemonic Output	Signal Description/Purpose	Sent To*
NTEST (P103-6)	Low = true level to establish test mode in the transport circuits.	J1-22, J5-60, J7-56, J8-36
NTSTB (P103-16)	Test data (all ones), generated on the Self Test PCBA. Data frequency depends on the settings of the SPEED and DENSITY selectors.	J3-19, J7-20
NTWRT (P102-J)	Low = true level to establish write mode operation in the transport circuits. High = false disables write circuits. (Read circuits are not controlled.)	J8-43
NTSFC (P103-H)	Low = true level to establish synchronous forward tape motion.	J8-24
NTSRC (P103-F)	Low = true level establishes synchronous reverse tape motion.	J8-35
NTRWC (P103-E)	Low = true level establishes rewind tape motion.	J8-59

5.12.3 TEST MODE CONTROL

When TEST control S1 (refer to Schematic No. 104962, zone 2-7G) is in ON position, U2-3 input is pulled down and U2-4 applies a high level to enable all output NAND gate latches (zones 2-2A through 2-2F). In the case of the NTEST signal, U2-4 output is connected to both gate inputs (U16-12 and -13), and U16-11 provides the low NTEST mode control level to the Read, Write, and Control M or M2 PCBAs. The other gates wait for a second input.

On the Control M (or M2) PCBA (refer to Schematic No. 104745, zone 2-17F or 106875, zone 3-8G), NTEST (NTESTA) is applied through NOR gate input U74-9, zone 2-14D (U132-9, zone 3-5E) to enable the interface output circuits, zones 2-12F, 2-11D—G (zones 3-2E,F,G). NTESTA is also applied to U23-4, zone 2-8D (U83-4, zone 4-6E) to clear the on-line flip-flop, U25-1, zone 2-7E (zone 4-5E).

On the Write PCBA (refer to Schematic No. 107860), NTEST is used to disable the normal amplifier enable circuits, to clock the test data (TSTDAT) generator, and to provide the TEST signal that selects the test data outputs of the write data registers.

5.12.4 TEST SIGNAL NTSTB/NTSTR GENERATION

The NTSTB/NTSTR output of the Self Test PCBA at P103-16 (Schematic No. 104962, zone 2-1F) is an all-ones signal (low = one). The frequency and waveform of the signal is determined by the settings of the DENSITY and SPEED controls:

(1) If the DENSITY selector S5 (zone 2-7D) is in 1600 position, NAND gate inputs U9-12,13 are kept high by U17-6 and U17-7, respectively. NAND output U9-11 is low and U8-4 is high, appling an enabling input at U9-5 (zone 2-3F) to select the frequency output at U9-6.

(2) If the DENSITY selector S5 is in 800 position, U9-13 is pulled down, disabling the selection described in (1) and, through U8-1 and 2, enabling NAND gate output U9-3 (zone 2-3E). This position is not used on T1940-96 Tape Transports.

*J1 and J3 are optional interface edge connectors on top of the Interconnect D/D1 PCBA. J5 is Read PCBA; J5, Write PCBA; J8, Control M/M2 PCBA.

(3) If the DENSITY selector S5 is in 6250 position, the NAND gate output at U9-8 is selected in a manner similar to that explained in (2). The 6250 switch election is not used in transports covered in this manual.

(4) The setting of the SPEED selector S6 (zone 2-8C) also has an effect on the selection of the test signal output NTSTB/NTSTR at J103-16. If S6 is open (75 position), NAND gate inputs U13-12,13 will be high, producing a low at U13-11 (zone 2-8D), U13-10 (zone 2-7F), and U12-10 (zone 2-5G). This will disconnect the frequency signal outputs at U14-10 (zone 2-8F) and U11-10 (zone 2-6F). High inputs at NAND gate U13-4 (zone 2-7E) and U12-4 (zone 2-5F) will enable the NAND gates to admit oscillator outputs U14-7 (zone 2-8E) and U11-7 (zone 2-6E), whichever is selected by the DENSITY control. This sets up the circuits for transports that record NRZI (800) and PE (1600) densities on tapes travelling at 1.905 m/s (75 ips).

If the SPEED switch is in closed (125) selection, the voltage level at U17-3 (zone 2-8D) will be pulled down. This reverses the preceding configuration and selects oscillator outputs U14-10 (zone 2-8F) and U11-10 (zone 2-6F), while U14-7 and U11-7 will be ineffective. This configuration provides frequencies that will produce the same densities on tapes travelling at 3.175 m/s (125 ips).

The NTSTB/NTSTR data/strobe of selected frequency output at Self Test PCBA connector P103-16 is sent to Write PCBA connector P7-20 as a series of low = true ones. Refer to Schematic No. 107860, zone 2-8D to provide and strobe all-1s test data into the write circuits.

5.12.5 WRITE/READ MODE SELECTION

MODE control provides for selecting read or write modes. Read-after-write transports are essentially in read mode at all times; therefore, the READ and WRITE positions of the MODE control (S4, Schematic No. 104962, zone 2-7D) provide for read-only or write-and-read mode options.

In READ position, S4 is open, U17-13 is high and the U6-2 input (zone 12-4C) is low. U6-5 flip-flop output will remain unchanged, since a high is required at both U6-2 and 3 in order to set the flip-flop. The flip-flop is assumed to be normally in clear state because of the automatic clearing feature, activated by a change in motion command (S2, zone 2-7B,C), or by manual resetting (S3, zone 2-7A).

In WRITE position, MODE control S4 (zone 2-7D) is closed, which pulls down U17-13, applying a low to U4-1 and a high to U6-2. The write mode flip-flop then waits for a low *go* command at U6-3 input. The *go* input is initiated by the operator by means of the ENABLE switch when all precondition selectors (MOTION, MODE, DENSITY, TEST) have been set and the circuits have been cleared by momentary selection of RESET position of the ENABLE control.

When the *go* signal arrives at U6-3 (zone 2-4C), U6-5 becomes high and, with NAND input U15-5 enabled (high), U15-6 (zone 2-2D), provides the low NTWRT level at J102-J. The write flip-flop is cleared by a new low at U6-1 (zone 2-4C).

NTWRT is sent to Control M/M2 PCBA (J8-43), where it initiates the NWRT for test purposes. Refer to Schematic No. 104745, zone 2-17G, 2-16D—2-13D (106875, zone 3-8H, 3-6G—3-1G).

5.12.6 MOTION SELECTION

The MOTION selector S2 (Schematic No. 104962, zone 2-7B) provides for selecting tape motion speed and direction. The selection may be synchronous forward (FWD), synchronous reverse (REV), or rewind (RWD) mode.

In RWD position, U3-9 and U3-10 NAND inputs are kept high by the outputs of U17-11 and U17-12, respectively. NAND output U3-8 is low, U4-8 and U3-4 (zone 2-3A) are high. When the ENABLE switch (zone 2-7A) is momentarily placed in GO position, a test rewind command (NTRWC) pulse is issued at U16-6 (zone 2-2A). NTRWC requires a high test mode enabling input at U16-4 (zone 2-2A) and a high enabling input at U3-1 (zone 2-6A). The latter input is from the oscillator OR gate at U12-3 (zone 2-4G).

The NTRWC pulse is sent to Control M/M2 PCBA input J8-59 (Schematic No. 104745, zone 2-17G), pulling down the output of U206-11. The low = true pulse then goes to OR gate input U45-1 (zone 2-5F) to initiate the normal transport rewind pulse (NREWP) through NAND input U46-1 (zone 2-5F). As in normal operation, generation of the NREWP requires the high = true interlock input at U46-2 and a high = true at U46-13, indicating that the transport is not on-line and the tape is not at BOT position. When tape reaches BOT, the rewind operation stops.

Note that when the MOTION selector is in REW position as explained previously, the low = true NAND output at U3-8 (zone 2-6B) is also applied, through OR gate U10-3,6 and an inverter, to the clear input (U6-1) of the write flip-flop. This inhibits writing in rewind mode.

When the MOTION selector is in FWD position, NAND input U3-9 (zone 2-6B) is low, inhibiting rewind operation, and inverter U4-4 delivers a high to set input U6-12 of the synchronous forward command (NTSFC) flip-flop. When the ENABLE switch (zone 2-7A) is placed in GO position momentarily and released, a high is applied to the clock input of the three mode flip-flops (zones 2-4,5A—2-4,5C). This initiates the mode of the selected flip-flop, as determined by the D inputs to the flip-flops. The *go* command requires that NAND gate input U3-1 (zone 2-6A) is enabled by a high from the oscillator circuits. With the MOTION control in FWD, this results in a synchronous forward command (NTSFC) at zone 2-1C. Similarly when the MOTION control is in REV position, a synchronous reverse command (NTSRC) results at zone 2-1B.

5.12.7 ENABLE (RESET-GO) CONTROL

The ENABLE switch S3 (Schematic No. 104962, zone 2-7A) is spring-loaded in center position and can be momentarily moved to RESET or GO positions. RESET position terminates the current read or write mode selection, stops tape motion (except rewind), and clears the mode and motion flip-flops. GO position initiates the action predetermined by the MODE and MOTION control selection, including rewind.

Both *go* and *reset* functions require a data/strobe oscillator output to enable their respective NAND gates (U3-1, U3-12). The *go* pulse will initiate the rewind command motion only when the REW setting on the MOTION switch provides a high at NAND gate input U3-4 (zone 2-3A). Note that the rewind command output (NTRWC) is a short burst of low = true ones (while the ENABLE switch is in GO position). The other mode motion outputs (NTWRT, NTSFC and NTSRC are levels (low = true) depending on the state of their respective flip-flops.

5.12.8 SKEW RESOLUTION

The NTSKEW/LATE AGC signal lights the SKEW indicator when an unsatisfactory skew condition exists or when some of the test one bits are dropped.

The NTSKEW/LATE AGC signal is provided by the Read PCBA, which processes and analyzes data read from the tape.

The Read PCBA circuits that resolve whether all bits of a test character arrive within the character time frame are discussed in Paragraph 5.8.2.

SECTION VI
MAINTENANCE AND TROUBLESHOOTING

6.1 INTRODUCTION

This section provides procedures necessary to perform functional alignments, parts replacement and adjustments, and troubleshooting. Sections IV and V contain the theory of operation of circuits for reference.

6.2 FUSE IDENTIFICATION

A total of seven fuses are located in front of the Power Supply Chassis and are identified in Table 6-1 and illustrated in Figure 6-1.

6.3 GENERAL MAINTENANCE REQUIREMENTS

Maintenance requirements are well within the scope of normal procedures for similar electronic equipment. Ease of access has been carefully considered throughout the design phase. Calibrations and adjustments have been kept to the minimum. Maintenance tools, instruments, and supplies, in most cases, are standard and readily available items.

6.3.1 PERIODIC MAINTENANCE

The objective of any maintenance program is to provide maximum machine readiness with a minimum of downtime. To provide this type of reliability, it is necessary to perform preventive maintenance at specific intervals; a preventive maintenance schedule for the transport is given in Table 6-2.

In general, it is not necessary to alter any adjustment on equipment that is performing in a satisfactory manner.

6.3.2 GENERAL MAINTENANCE

Perform a visual inspection of the equipment for loose electrical connections, dirt, cracks, binding, excessive wear, and loose hardware while conducting any maintenance function.

Cleanliness is essential for proper operation. Minute particles of dirt trapped between the head and the tape can cause data errors.

Table 6-1
Fuse Identification

Fuse	Function	Type
F1	+ 12V	10 Amp FB
F2	+ 24V	5 Amp FB
F3	– 24V	5 Amp FB
F4	+ 36V (C)	20 Amp FB
F5	– 36V (C)	20 Amp FB
F6	+ 36V (T)	20 Amp FB
F7	+ 36V (S)	20 Amp FB

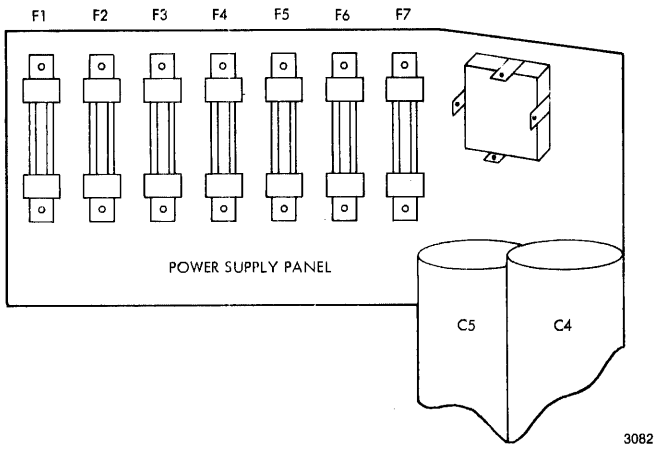


Figure 6-1. Power Supply Chassis Fuse Placement

Table 6-2
Preventive Maintenance Schedule

Frequency	Procedure	Reference Paragraph
Daily	Clean read/write head, erase head, and tape cleaner blades.	6.5.1
	Clean two spring-loaded rectangular ceramic guides.	6.5.2
	Clean air guide, air bearings, guide block, buffer boxes, loop pocket, buffer box glass, pocket glass, and buffer box dowel pins.	6.5.2
	Clean capstan.	6.5.2
	Check the elapsed time meter (optional) or equipment log for total hours of service per following requirements.	——
Six Months or 2500 Hours	Remove and clean air bearings, air guide and circular ceramic guides.	6.7.2—4
	Check and adjust pressures and vacuums. Adjust loop positions.	6.6.9
	Check and adjust supply reel thread speed.	6.6.6
	Clean reel sense lenses and BOT/EOT cavities.	6.6.3
	Check cartridge open/close switches and adjust if necessary.	6.7.9
	Clean cartridge restraints.	6.7.9
	Check skew.	6.6.5
	Check tape tracking.	6.6.2
	Check capstan motor air inlet screen and clean as required.	——
	Check write skew.	6.6.11
Yearly or 5000 Hours	Check for head wear.	6.7.1
	Remove tape cleaner and clean blades.	6.7.2
	Replace compressor intake filter element. (More frequent servicing may be required if operating in an abnormally dirty environment.)	Figure 7-5
	Check and tighten hose and tube connections.	Normal
	Perform general cleaning of entire drive.	Normal
	Check belts for wear and proper tracking.	6.7.11—13
Two Years or 10,000 Hours	Replace compressor exhaust filter.	Figure 7-5

6.4 MAINTENANCE AIDS, TOOLS, INSTRUMENTS, AND SUPPLIES

Items needed to facilitate transport operation and maintenance according to the procedures described in this manual are listed below.

(1) Oscilloscope, Tektronix 465 (vertical and horizontal sensitivity specified to ±3 percent accuracy).

(2) Digital Multimeter, Fluke 8000A (±0.1 percent specified accuracy).

(3) Tapes used for test and adjustment

- Performance evaluation and checkout, Pertec 516-0088 (216 mm [8.5 inch] reel) or 516-0108 (267 mm [10.5 inch] reel)
- Master Skew Tape, Pertec 516-0003 (216 mm [8.5 inch] reel) or 516-0004 (267 mm [10.5 inch] reel)
- PE Read Gain adjustment, Pertec 516-0008 (216 mm [8.5 inch] reel)

(4) Differential Pressure Gauge with stand 0 to 50 Inch H_2O Range (Dwyer Instruments, Inc., Model No. 2050).

(5) Differential Pressure Gauge with stand 5 psig (Dwyer Instruments, Inc., Model No. 2205).

(6) Tape crimper, IBM No. 2512063.

(7) Positioning tool, vacuum reel flanges, Pertec 108454-01.

(8) Tube fitting, lower restraint, Pertec 107070-01.

(9) Reel motor centering tools, Pertec 107267-01 (supply reel) and 107267-02 (takeup reel).

(10) Vernier Caliper, Mitutoyo 505-637.

(11) Standard nut driver set.

(12) Hex driver set.

(13) Hex socket key set.

(14) Open-end wrench set up to 9/16-inch.

(15) 13/64 open-end wrench.

(16) Phillips screwdriver set, including one with 8-inch long blade.

(17) Standard blade screwdriver set.

(18) Penlight.

(19) Inspection mirror.

(20) Lint-free cloth.

(21) Cotton swabs.

(22) 91% isopropyl alcohol.

(23) Extender Board, Pertec 107206-01.

(24) Power Pack Mounting Kit.

6.5 CLEANING THE TRANSPORT

The head, fixed tape guides, tape cleaner, capstan, buffer box and glass, loop pocket and glass, dowel pins, overlay, and air bearings require special attention to realize the maximum data reliability of the unit. Details for cleaning are given in the following paragraphs; cleaning intervals are as specified in Table 6-2.

6.5.1 CLEANING THE HEAD

To clean the head, use a lint-free cloth or cotton swab moistened in 91 percent isopropyl alcohol. Wipe the head carefully to remove all accumulated oxide and dirt.

CAUTION

DO NOT USE ROUGH OR ABRASIVE CLOTHS TO CLEAN THE HEAD. USE ONLY 91% ISOPROPYL ALCOHOL. OTHER SOLVENTS, SUCH AS CARBON TETRACHLORIDE, MAY RESULT IN DAMAGE TO HEAD LAMINATION ADHESIVE.

6.5.2 CLEANING THE FIXED GUIDES, TAPE CLEANER, CAPSTAN, AND BUFFER BOX

To clean the fixed guides, tape cleaner, capstan, and buffer box, use only a lint-free cloth or a cotton swab moistened with 91 percent isopropyl alcohol to remove accumulated oxide and dirt. The buffer box door may be opened to gain access to the surfaces that require periodic cleaning. Special procedures for cleaning the air guides are covered in Paragraph 6.7.

6.6 FUNCTIONAL ALIGNMENTS

Paragraphs 6.6.1 through 6.6.7 describe the step-by-step procedures required to functionally align the transport.

NOTE

Some adjustments may require corresponding adjustments in other parameters. Ensure adjustments are made as specified in the individual procedures. Allow equipment to warm up for thirty minutes before electrical adjustment procedures are performed.

Acceptable limits are defined in each adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified. When the measured value of any parameter is within the specified acceptable limits, NO ADJUSTMENTS should be made. Should the measured value fall outside the specified acceptable limits, adjustment should be made in accordance with the relevant procedure; the value set should be as close as possible to the exact value specified.

If difficulties occur in performing any alignment, refer to Paragraph 6.8 (Troubleshooting) for fault isolation procedures.

6.6.1 POWER DISTRIBUTION

The Power Supply and the Regulators are not adjustable. The following procedure is given to verify all operating dc voltages are present.

WARNING

DANGEROUS VOLTAGES ARE PRESENT IN THE POWER SUPPLY.

(1) Ensure the transport is plugged into the proper ac power.

(2) Ensure the main power circuit breaker switch, located on the rear of the Power Pack Chassis, is ON.

(3) Set POWER control to ON.

(4) Open the front of the transport to access the Card Cage Assembly and the Power Supply Chassis.

(5) Check all fuses.

(6) With a DVM, monitor fuses F1—F7 with respect to chassis for the proper dc voltages. Refer to Figure 6-1 for fuse locations and Table 6-3 for proper voltage readings. If incorrect, check T1 primary taps per Table 2-3.

(7) With a DVM on the Capstan/Regulator PCBA, monitor TP11, TP15, and TP18 with respect to TP1; Figure 6-2 illustrates the locations of test points and connectors.

☐ TP11

- + 5.00v dc minimum
- + 5.15v dc nominal
- + 5.30v dc maximum

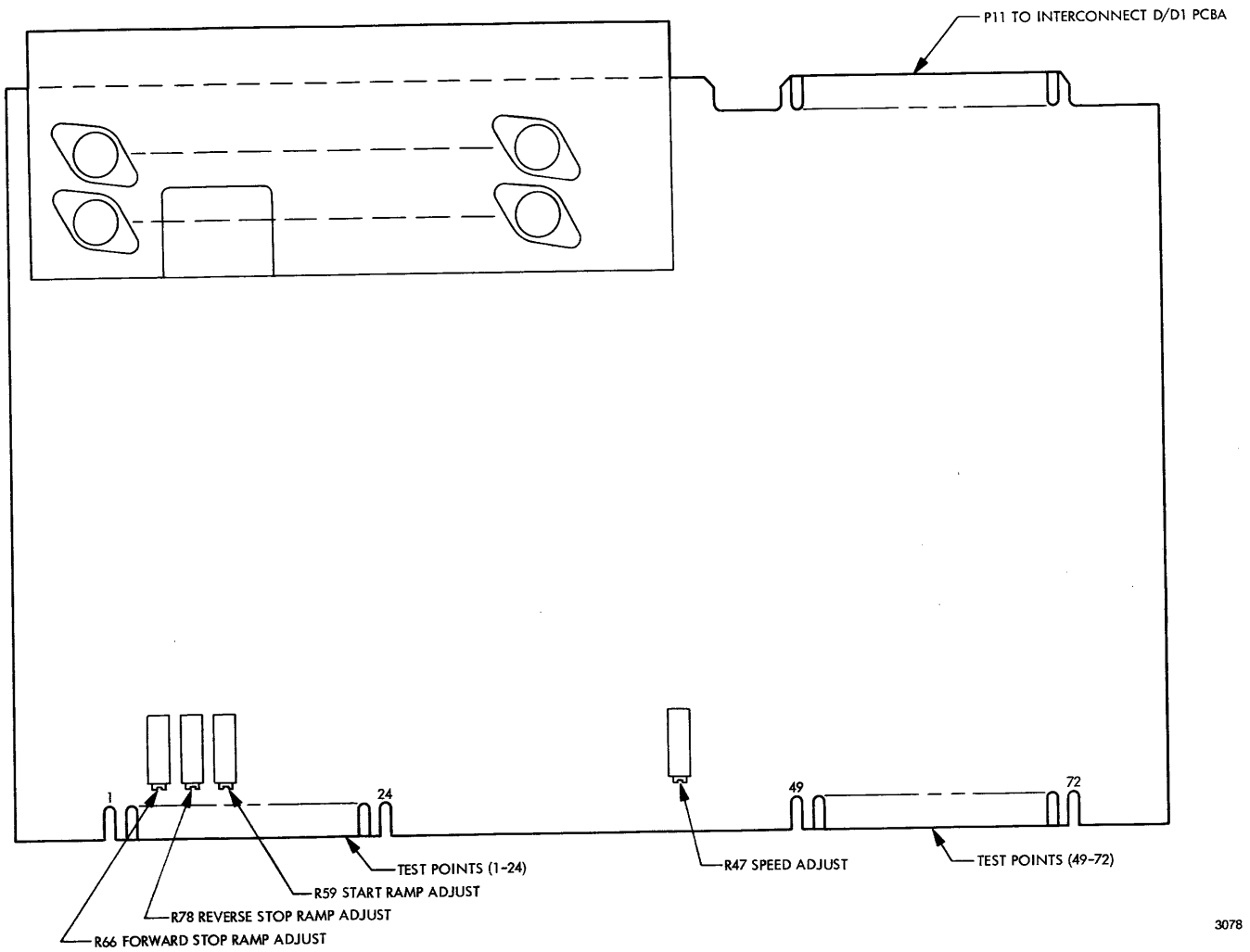


Figure 6-2. Capstan/Regulator PCBA Test Point/Connector/Adjustment Locations

Table 6-3
Power Supply Voltage Readings

	Voltage (dc)		
Fuse	Minimum	Nominal	Maximum
F1	+09.5	+10.5	+11.5
F2	+22.0	+24.0	+26.0
F3	−22.0	−24.0	−26.0
F4	+35.5	+37.5	+40.0
F5	−35.5	−37.5	−40.0
F6	+35.5	+37.5	+40.0
F7	+35.5	+37.5	+40.0

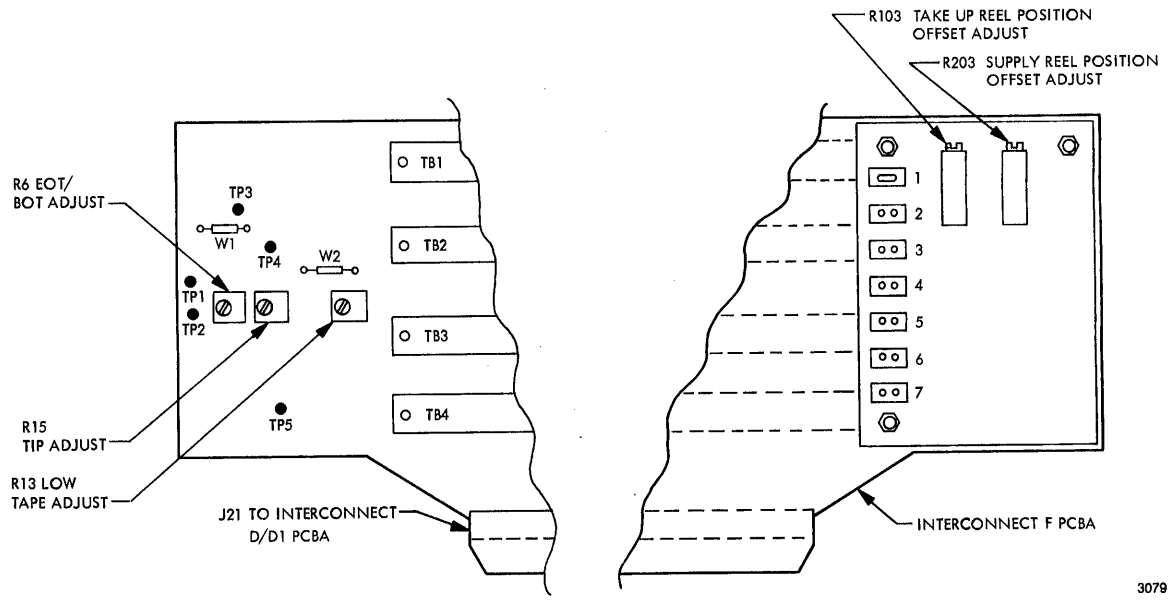
☐ TP15
- +14.0v dc minimum
- +15.0v dc nominal
- +16.0v dc maximum

☐ TP18
- −14.0v dc minimum
- −15.0v dc nominal
- −16.0v dc maximum

6.6.2 SYSTEM CONTROL FUNCTIONAL ALIGNMENT

The following procedure describes the alignment of the EOT/BOT amplifier.

(1) Set POWER control to ON.
(2) Open the front of the transport to access the Card Cage and the Power Supply.
(3) Verify Power Supply voltages according to Paragraph 6.6.1.
(4) On the Interconnect F PCBA, connect a DVM with its positive lead to TP1 (NBOT) and its negative lead to TP2 (NEOT). (On Interconnect F1 PCBA, TP6 is NBOT and TP5 is NEOT.) Figure 6-3 shows the locations of the test points.
(5) Open the supply reel door, the takeup reel door, and the buffer box door.
(6) On a work tape, attach an EOT reflective tab about one inch in front of the BOT tab.
(7) Install the work tape reel on the supply hub. Thread the tape so that the EOT and BOT reflective tabs are not under the sensors. Refer to Figure 6-4. Maintain tension with one end of the tape by holding the tape on the capstan. The tape must contact the head surface.
(8) Monitor the DVM. The voltage displayed should be:
   - +0.1v dc maximum
   - −0.1v dc minimum
(9) If the voltage is out of tolerance (Step 8), adjust potentiometer R6 on the Interconnect F PCBA for 0v dc (refer to Figure 6-3). On Interconnect F1, adjust R22 for 0v dc.
(10) Pull the work tape and move the BOT tab to the sensor and monitor the DVM.
(11) The voltage displayed should be equal to or more negative than −2.0v dc.
(12) Pull the work tape and move the EOT tab to the sensor and monitor the DVM.
(13) The voltage displayed should be equal to or more positive than +2.0v dc.



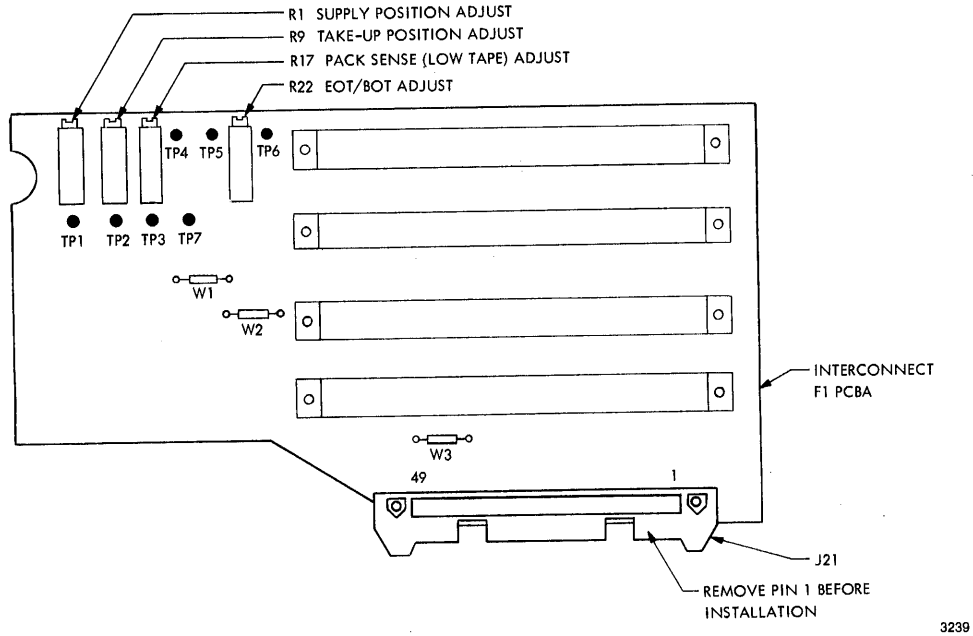


Figure 6-3. Interconnect F/F1 PCBA Test Point/Connector/Adjustment Locations

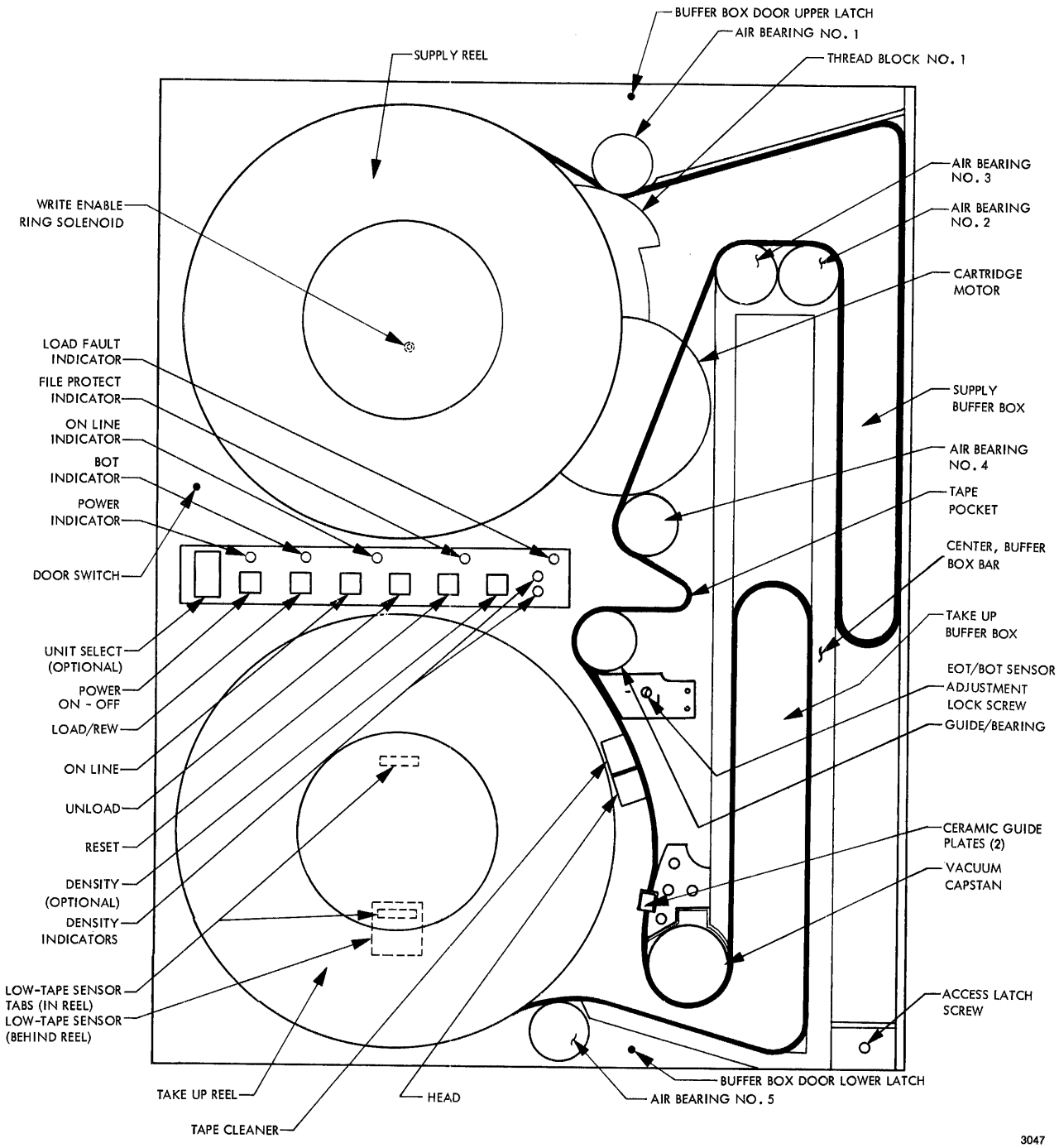


Figure 6-4. Tape Path and Controls and Sensor Features

(14) If required output levels cannot be achieved by steps (7)—(13), check EOT/BOT sensor mechanical adjustment as follows:

(a) Loosen sensor adjustment lock screw, located below the tape pocket lower guide bearing. Refer to Figure 6-4.

(b) Loosen the two sensor cover block mounting screws, located at right hand edge of cover block.

(c) Manually press the cover block to the left and upward until the curve in the block rests against the guide bearing.

(d) Tighten cover block mounting screws.

(e) Insert a small probe through the slot located upward and to the left of the sensor adjustment lock screw, and lever the sensor toward the tape path.

(f) Insert the probe through the slot located to the right of the sensor adjustment lock screw and lever the sensor to the left.

(g) Tighten the sensor adjustment lock screw.

NOTE

When Step 14 is complete, the sensor critical face will rest against the cover block wall on the tape path end of the cover block. If satisfactory adjustment cannot be made, remove the block and ascertain that the sensor mounting shim is in place.

(15) Remove the work tape.

6.6.3 TAPE-IN-PATH SENSING CIRCUIT ALIGNMENT

The following procedure describes the alignment of the TIP circuit.

(1) Set POWER control to ON.

(2) Open the front of the transport to access the Card Cage and the Power Pack.

(3) Verify Power Pack voltages according to Paragraph 6.6.1.

(4) On the Interconnect F PCBA, connect a DVM with its positive lead to TP3 and its negative lead to TP5. On Interconnect F1 PCBA, connect positive lead to TP3 and negative to TP7. Figure 6-3 shows the locations of test points.

(5) Open the supply reel door, the takeup reel door, and the buffer box door.

(6) Install the work tape reel on the supply hub. Thread the tape. Refer to Figure 6-4. Maintain tension with one end of the tape by holding the tape on the capstan. The tape must contact the head surface.

(7) Monitor with DVM; the voltage displayed should be:

- + 0.50v dc maximum

(8) If the voltage is out of tolerance (Step 7), adjust potentiometer R15 on the Interconnect F PCBA (refer to Figure 6-3). No comparable adjustment is necessary on Interconnect F1 PCBA.

(9) Pull the work tape out of the tape path.

(10) The voltage displayed should be equal to or more positive than + 4.0v dc.

(11) Remove the work tape and disconnect the DVM.

6.6.4 LOW-TAPE SENSING ALIGNMENT

The following procedure describes the alignment of the Low Tape sensing circuit.

(1) Set POWER control to ON.

(2) Open the front of the transport to access the Card Cage and the Power Pack.

(3) Verify Power Pack voltages according to Paragraph 6.6.1.

(4) On the Interconnect F PCBA, connect a DVM with its positive lead to TP4 and its negative lead to TP5. On Interconnect F1 PCBA, connect positive lead to TP4 and negative lead to TP7. Figure 6-3 shows the locations of the test points.

(5) Open the takeup reel door.

(6) Rotate the takeup reel until the sensor tab (located on the inside of the outer flange of the reel) is in line with the Low Tape sensor (behind the reel). Refer to Figure 6-4.

(7) Monitor with DVM; the voltage displayed should be:

- + 0.50v dc maximum

(8) If the voltage is out of tolerance (Step 7), adjust potentiometer R13 on the Interconnect F PCBA or R17 on Interconnect F1 PCBA (refer to Figure 6-3).

(9) Turn the takeup reel until the tab is off the sensor.

(10) The voltage displayed should be equal to or more positive than + 4.0v dc.

(11) Disconnect the DVM.

6.6.5 CAPSTAN FUNCTIONAL ALIGNMENT

The Capstan Functional Alignment provides the procedure for adjusting the capstan speed, the start ramp, and the forward and reverse stop ramps.

(1) Install any prerecorded 9-track, PE, 63 c/mm (1600 cpi), all ones, 267 mm (10½ inch) tape reel or cartridge on the supply hub.

(2) Set the POWER control to ON.

(3) Set the DENSITY switch to 1600.

(4) Press and release the LOAD/REW switch.

(5) After tape motion stops and the BOT lamp lights, open the front of the transport to access the Card Cage and the Power Supply.

(6) Verify Power Supply voltages according to Paragraph 6.6.1.

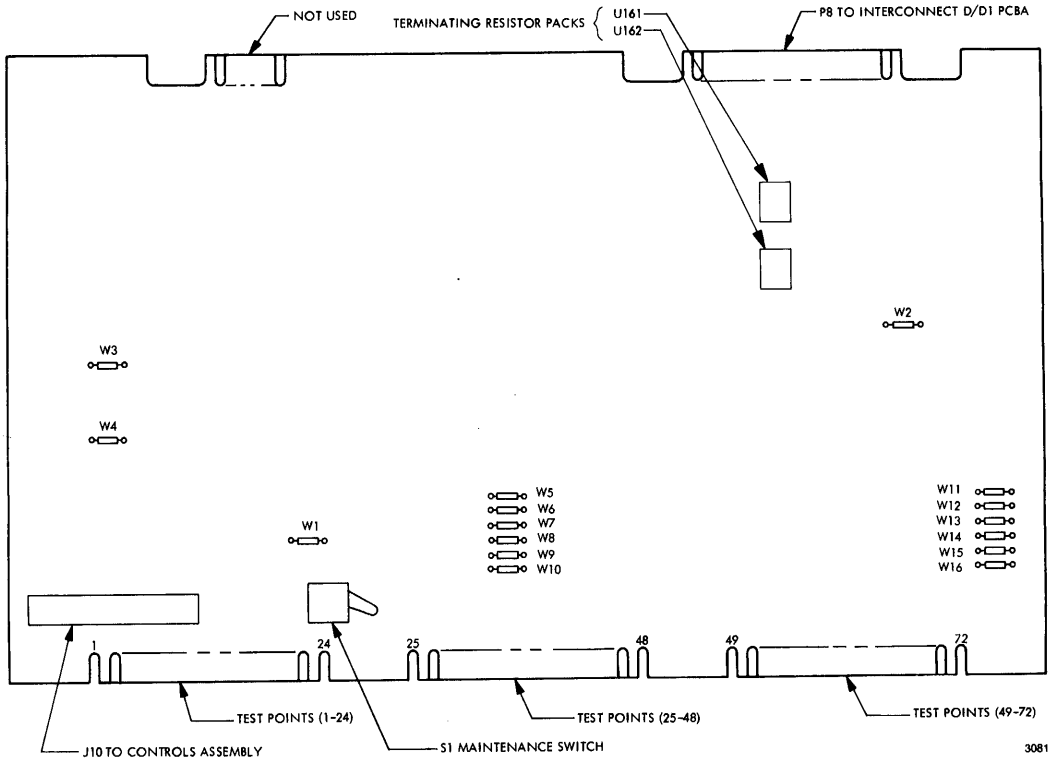
(7) Ensure the ON LINE lamp is extinguished. If the lamp is illuminated, press and release the ON LINE switch.

(8) On the Control M/M2 PCBA, connect an oscilloscope with its input lead to TP40 and its ground lead to TP25; Figure 6-5 illustrates the placement of the test points.

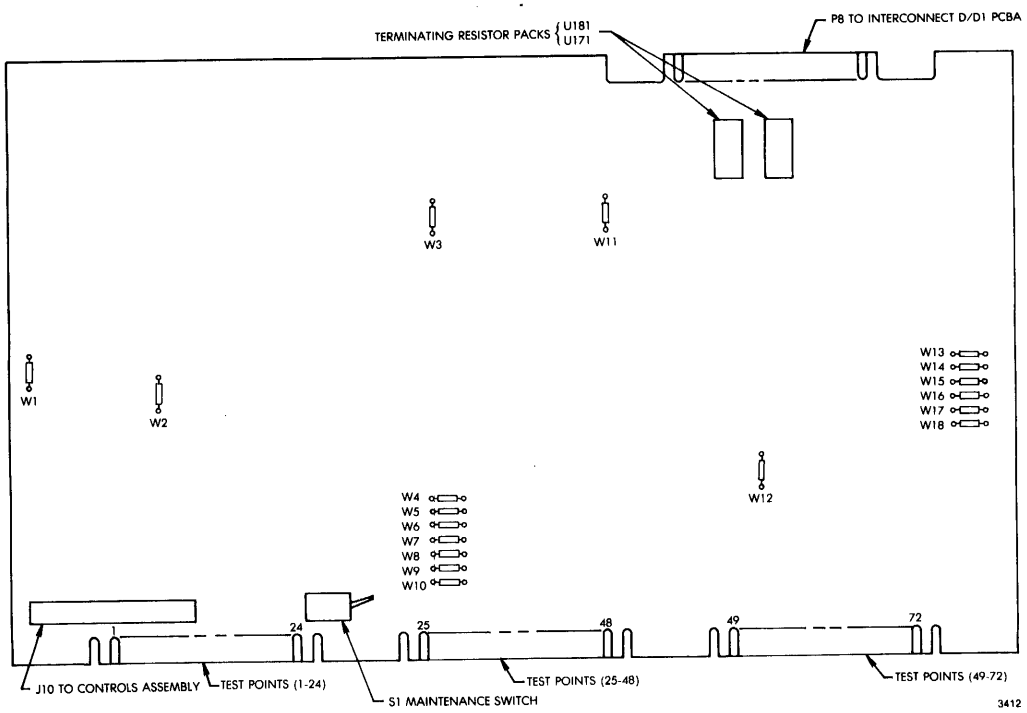
(9) Set switch S1 on the Control M/M2 PCBA toward the front of the transport; tape will move forward.

(10) Observe the oscilloscope; the pattern should be as shown in Figure 6-6. The period of the waveform should be as follows.

- ☐ 1.905 m/s (75 ips)
  - 134 μsec maximum
  - 132 μsec minimum
- ☐ 2.540 m/s (100 ips)
  - 101 μsec maximum
  - 99 μsec mimimum
- ☐ 2.858 m/s (112.5 ips)
  - 89.0 μsec maximum
  - 88.0 μsec minimum
- ☐ 3.175 m/s (125 ips)
  - 80.8 μsec maximum
  - 79.2 μsec minimum

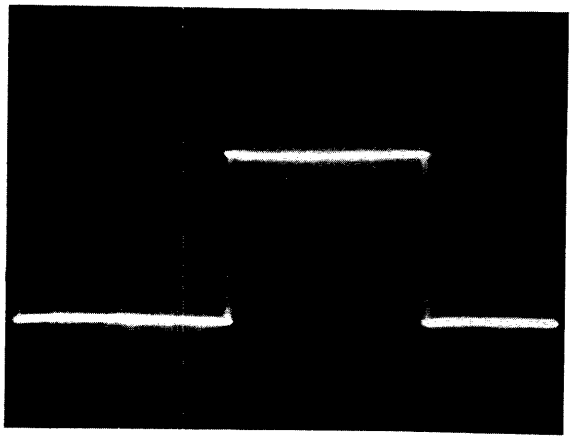


A. Control M PCBA



B. Control M2 PCBA

Figure 6-5. Control M and Control M2 PCBA Test Point/Connector/Adjustment Locations



PROBE: X10
HORIZ: 10μSEC/DIV
VERT: 0.1V/DIV
SYNC: DC—INT

3101

Figure 6-6. Capstan Speed, 3.175 m/s (125 ips)

(11) If the frequency is out of tolerance (Step 10), adjust potentiometer R47 on the Capstan/Regulator PCBA for the proper time, as follows (refer to Figure 6-2).

- ☐ 1.905 m/s (75 ips)
  - 133 μsec
- ☐ 2.540 m/s (100 ips)
  - 100 μsec
- ☐ 2.858 m/s (112.5 ips)
  - 88.8 μsec
- ☐ 3.175 m/s (125 ips)
  - 80 μsec

(12) Set switch S1 on the Control M/M2 PCBA to the middle (stop) position; tape motion will stop.

(13) Press and release the LOAD/REW switch.

(14) After tape motion stops and the BOT lamp lights, disconnect the oscilloscope from the Control M/M2 PCBA.

(15) Connect a jumper between TP30 and TP25 on the Control M/M2 PCBA.

(16) With read amplifier gain switch in PE GAIN position (refer to Figure 6-7), check preamplifier outputs with oscilloscope. Use R13 or R14, on the GCR/PE Preamp 1 PCBA, open ended. (Refer to Figure 6-8.)

(17) Connect the oscilloscope external sync to Control M/M2 PCBA TP21. Refer to Figure 6-9 for scope settings.

(18) Set switch S1 on the Control M/M2 PCBA toward the front of the transport; the tape will alternately start and stop.

(19) Observe the oscilloscope. Refer to Figure 6-9. The forward start ramp rise time displayed should be as follows.

- ☐ 1.905 m/s (75 ips) 2.02 msec nominal
  - 2.12 msec maximum
  - 1.92 msec minimum

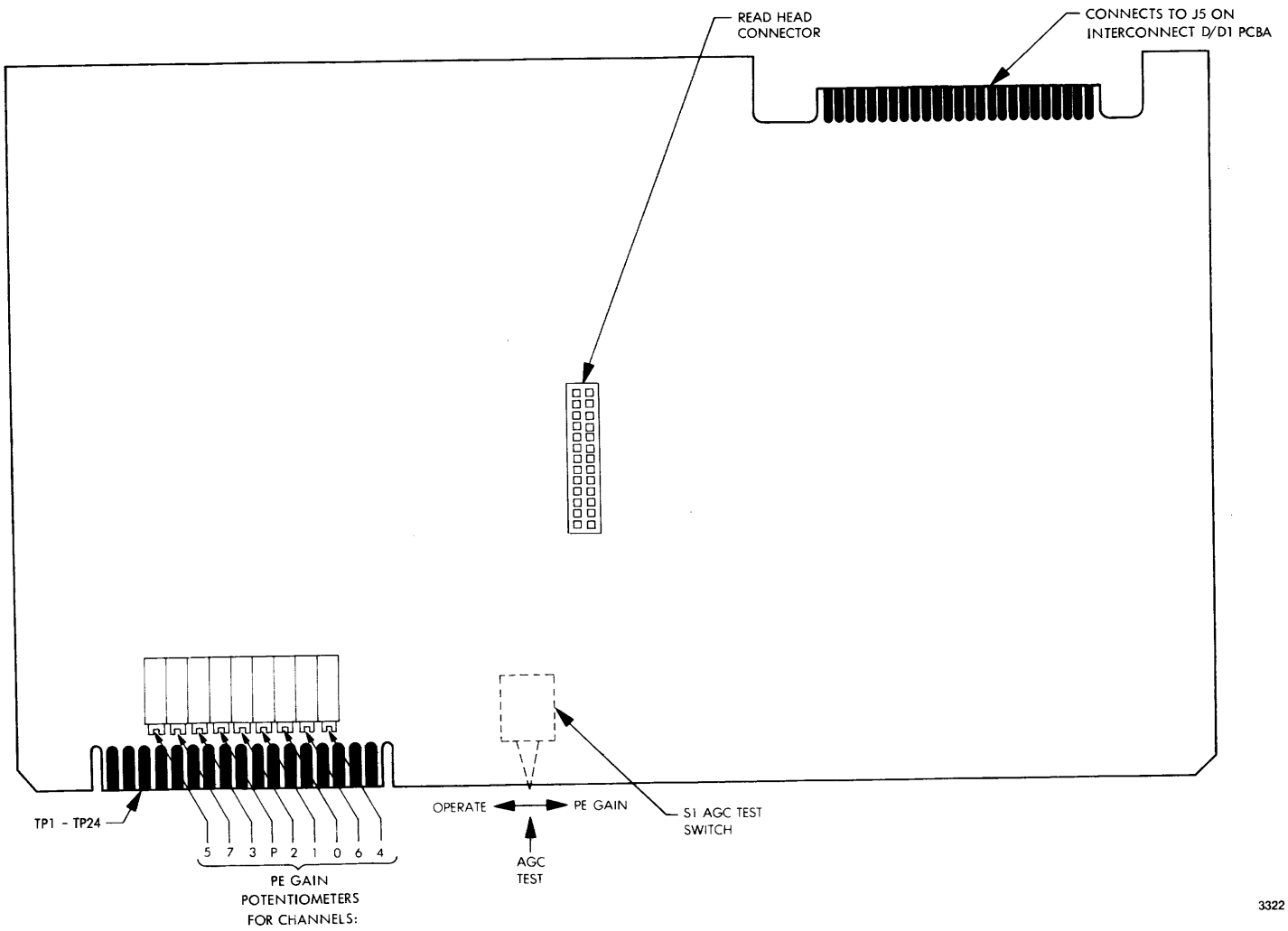


Figure 6-7. Read PCBA Test Point/Connector/Adjustment Locations

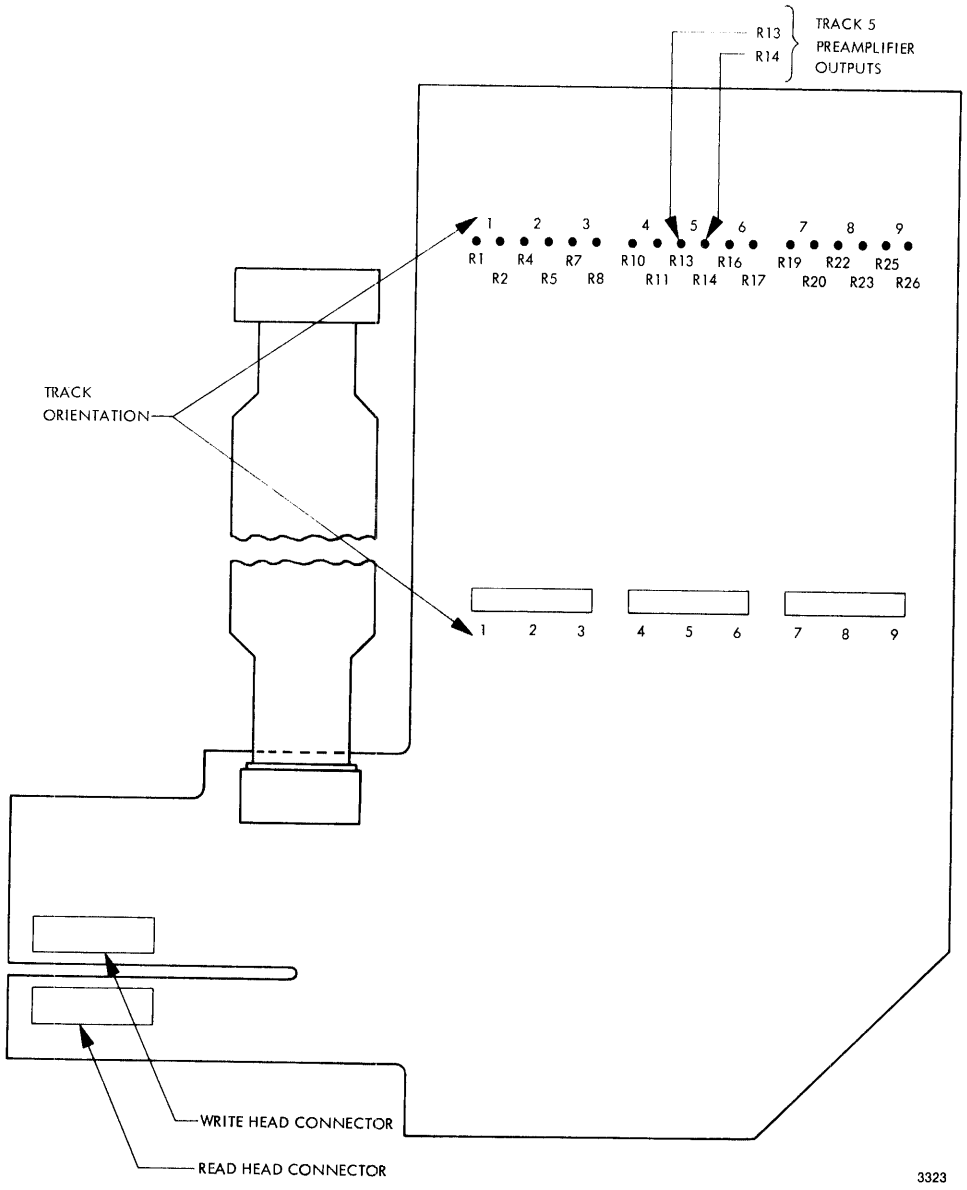
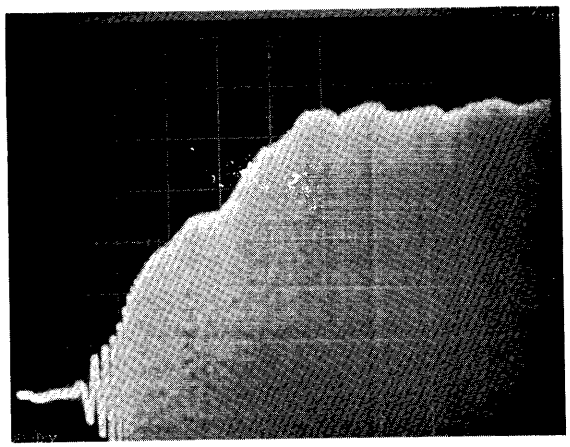


Figure 6-8. GCR/PE Preamp 1 PCBA, Physical Features



PROBE: X10
HORIZ: 0.2μSEC/DIV
VERT: 0.01V/DIV (UNCAL)
SYNC: AC—EXT POSITIVE
TP21 CONTROL
M PCBA

NOTE:
FORWARD START RAMP IS MEASURED BETWEEN CHANGE OF MOTION SIGNAL AT TP21 AND 95% OF READ ENVELOPE.

3102

Figure 6-9. Forward Start Ramp Timing, 3.175 m/s (125 ips)

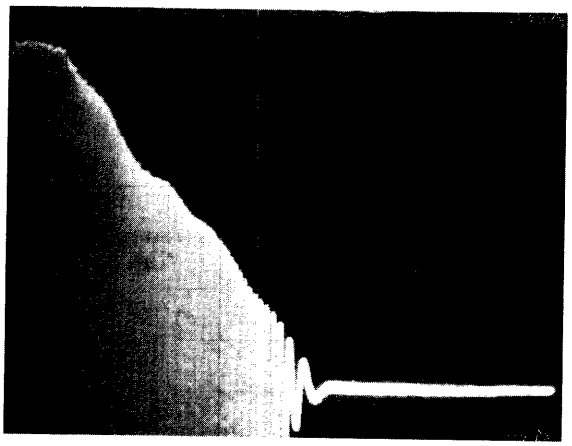
- ☐ 2.540 m/s (100 ips) 1.57 msec nominal
  - 1.65 msec maximum
  - 1.49 msec minimum
- ☐ 2.858 m/s (112.5 ips) 1.42 msec nominal
  - 1.49 msec maximum
  - 1.35 msec minimum
- ☐ 3.175 m/s (125 ips) 1.27 msec nominal
  - 1.33 msec maximum
  - 1.21 msec minimum

(20) If the rise time is out of tolerance (Step 19), adjust potentiometer R59 on the Capstan/Regulator PCBA for the proper rise time. Refer to Figures 6-2 and 6-9.

- ☐ 1.905 m/s (75 ips)
  - 2.02 msec
- ☐ 2.540 m/s (100 ips)
  - 1.57 msec
- ☐ 2.858 m/s (112.5 ips)
  - 1.42 msec
- ☐ 3.175 m/s (125 ips)
  - 1.30 msec

(21) Observe the oscilloscope. Refer to Figure 6-10 for scope settings. The forward stop ramp fall time displayed should be as follows.

- ☐ 1.905 m/s (75 ips) 1.80 msec nominal
  - 1.89 msec maximum
  - 1.71 msec minimum
- ☐ 2.540 m/s (100 ips) 1.35 msec nominal
  - 1.41 msec maximum
  - 1.28 msec minimum



PROBE: X10
HORIZ: 0.2μSEC/DIV
VERT: 0.02V/DIV (UNCAL)
SYNC: AC—EXT NEGATIVE
TP21 CONTROL
M PCBA

NOTE:
FORWARD START RAMP IS MEASURED BETWEEN CHANGE OF MOTION SIGNAL AT TP21 AND 5% OF READ ENVELOPE.
ADJUST FALL TIME FOR NO OVERSHOOT OR UNDERSHOOT.

3103

Figure 6-10. Forward Stop Ramp Timing, 3.175 m/s (125 ips)

- ☐ 2.858 m/s (112.5 ips) 1.20 msec nominal
  - 1.26 msec maximum
  - 1.14 msec minimum
- ☐ 3.175 m/s (125 ips) 1.08 msec nominal
  - 1.13 msec maximum
  - 1.02 msec minimum

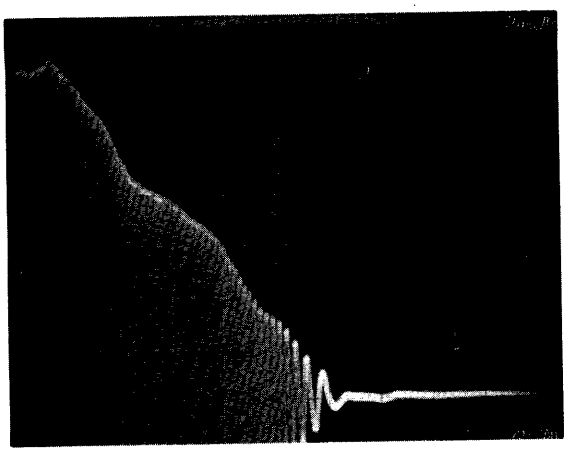
(22) If the fall time is out of tolerance (Step 21), adjust potentiometer R66 on the Capstan/Regulator PCBA for the proper fall time (refer to Figures 6-2 and 6-10).

- ☐ 1.905 m/s (75 ips)
  - 1.80 msec
- ☐ 2.540 m/s (100 ips)
  - 1.35 msec
- ☐ 2.858 m/s (112.5 ips)
  - 1.20 msec
- ☐ 3.175 m/s (125 ips)
  - 1.08 msec

(23) Set switch S1 on the Control M/M2 PCBA to the middle (stop) position. After tape motion stops, set switch S1 towards the back of the transport.

(24) Observe the oscilloscope. Refer to Figure 6-11 for scope settings. The reverse stop ramp fall time displayed should be as follows.

- ☐ 1.905 m/s (75 ips) 1.80 msec nominal
  - 1.89 msec maximum
  - 1.71 msec minimum
- ☐ 2.540 m/s (100 ips) 1.35 msec nominal
  - 1.41 msec maximum
  - 1.28 msec minimum



PROBE: X10
HORIZ: 0.2μSEC/DIV
VERT: 0.02V/DIV (UNCAL)
SYNC: C—EXT
TP21 CONTROL
M PCBA

NOTE:
REVERSE STOP RAMP IS MEASURED BETWEEN CHANGE OF MOTION SIGNAL AT TP21 AND 5% OF READ ENVELOPE.
ADJUST THE FALL TIME FOR NO OVERSHOOT OR UNDERSHOOT.

3104

Figure 6-11. Reverse Stop Ramp Timing, 3.175 m/s (125 ips)

- ☐ 2.858 m/s (112.5 ips) 1.20 msec nominal
  - 1.26 msec maximum
  - 1.14 msec minimum
- ☐ 3.175 m/s (125 ips) 1.08 msec nominal
  - 1.13 msec maximum
  - 1.02 msec minimum

(25) If the fall time is out of tolerance (Step 24), adjust potentiometer R78 on the Capstan/Regulator PCBA for the proper fall time (refer to Figures 6-2 and 6-11).

- ☐ 1.905 m/s (75 ips)
  - 1.80 msec
- ☐ 2.540 m/s (100 ips)
  - 1.35 msec
- ☐ 2.858 m/s (112.5 ips)
  - 1.20 msec
- ☐ 3.175 m/s (125 ips)
  - 1.08 msec

(26) Set maintenance switch S1 on the Control M/M2 PCBA to the middle (stop) position. Disconnect the oscilloscope and jumper.

(27) Press and release the UNLOAD switch. After tape unloads, remove the all ones tape from the supply reel.

6.6.6 REEL SERVO FUNCTIONAL ALIGNMENT

The reel servo functional alignment provides for adjusting the reel servo offset, supply and takeup reel load speeds, and run loop positions.

6.6.6.1 Reel Servo Offset Adjustment

(1) Set the POWER control to OFF.

(2) Open the front of the transport to access the Card Cage and the Power Supply.

(3) Disconnect the takeup reel servo motor at the motor.

(4) Set the POWER control to ON.

(5) Verify power supply voltages per Paragraph 6.6.1.

(6) Open the supply and takeup reel doors and remove supply reel.

(7) Press and release the LOAD/REW switch. Immediately turn the takeup reel three full turns by hand. This will defeat activating load fault 0.

(8) With no reel on the supply motor hub, making it as light as possible, check the supply motor hub for motion. There should be no motion at this time because the logic sees a small reel and does not activate the backwrap function.

(9) If motion occurs, adjust potentiometer R76 (refer to Figure 6-12) on the Reel Servo PCBA for no motion of the supply reel hub.

NOTE

If R76 is adjusted, it should be set first at the point where the supply reel hub just starts to turn in the clockwise direction, then backed off until the reel hub stops turning.

CAUTION

THE SPECIFIED DUTY CYCLE FOR THE VACUUM AND AIR PRESSURE SOLENOIDS IS INTERMITTENT, 3 MINUTES ON AND 9 MINUTES OFF; THEREFORE, THE UNIT SHOULD NOT BE HELD IN THIS MODE FOR OVER 3 MINUTES MAXIMUM, AFTER WHICH THE COIL SHOULD BE ALLOWED TO COOL FOR 9 MINUTES.

(10) Press and release the RESET control.

(11) Set the POWER control to OFF.

(12) Reconnect the takeup reel motor leads.

6.6.6.2 Supply Reel Load Speed Adjustment

(1) On the supply hub, mount a 267 mm (10½ inch) reel of tape with the leader taped down to the reel.

(2) Place a short piece of masking tape at a convenient point on the front panel trim adjacent to the supply reel.

(3) Place a short piece of masking tape on the supply reel adjacent to the masking tape affixed in Step (2).

(4) Set POWER control to OFF.

(5) Ground TP60 (NAE) and TP69 (NSRF1) on the Reel Servo PCBA.

(6) Set the POWER control to ON. The supply reel should rotate in the clockwise direction.

(7) Observe the masking tape on the supply reel. Using a stop watch, count ten rotations of the supply reel masking tape as it passes the tape on the trim.

NOTE

Be sure to start and stop the stop watch when the two pieces of masking tape are coincident.

(8) Observe the elapsed time indicated by the stop watch; the display time should be:

- 12.0 seconds maximum (50 rpm)
- 10.0 seconds minimum (60 rpm)

(9) If the displayed time is out of tolerance (Step 8), adjust potentiometer R52 (refer to Figure 6-12) on the Reel Servo PCBA for an elapsed time of 11 seconds (55 rpm) while performing Steps (7) and (8).

(10) Set POWER control to OFF.

(11) Remove grounds from Reel Servo PCBA and remove masking tape.

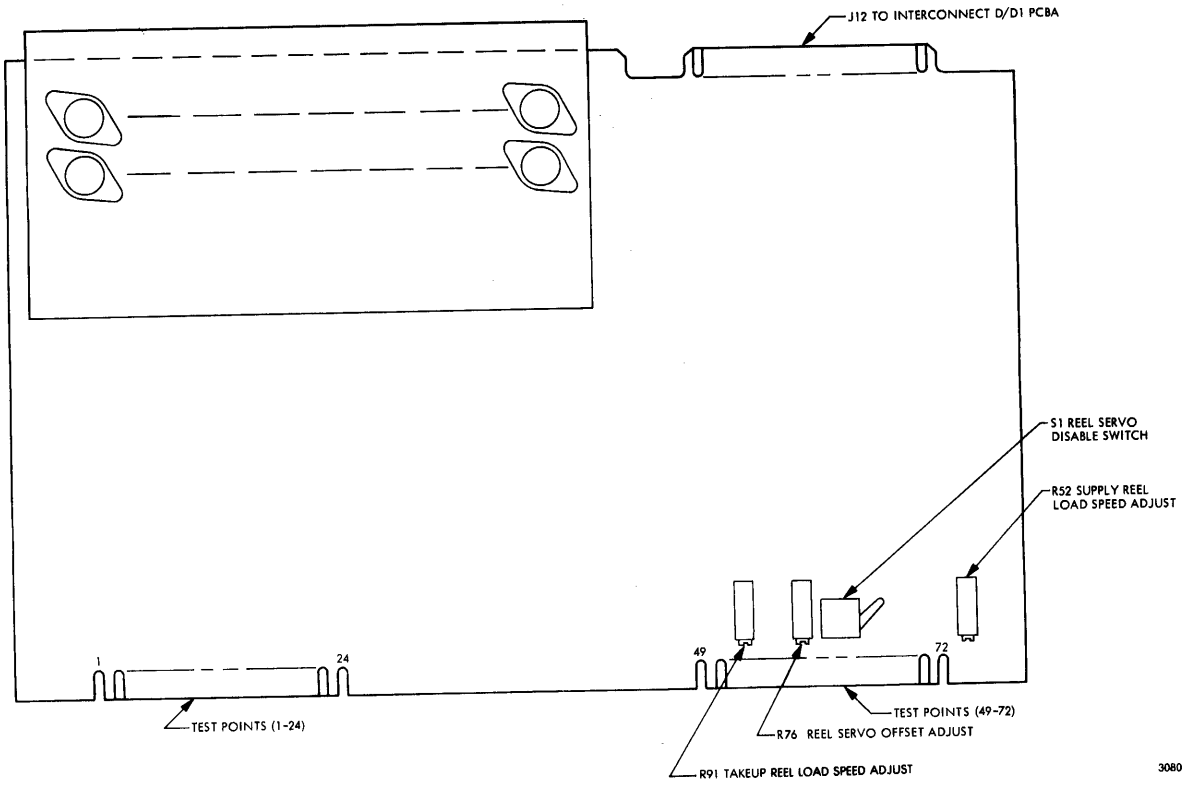


Figure 6-12. Reel Servo PCBA Test Point/Connector/Adjustment Locations

6.6.6.3 Takeup Reel Load Speed Adjustments

(1) Set the POWER control to OFF.

(2) Ground TP60 (NAE) and TP57 (NTRF) to TP49 on the Reel Servo PCBA.

(3) Set the POWER control to ON. The takeup reel should rotate in the clockwise direction.

(4) Connect an oscilloscope input lead to TP43 (low tape sensor input) of the Control M/M2 PCBA. Refer to Figure 6-13 for scope settings.

(5) Observe the oscilloscope. Refer to Figure 6-13. The time between leading edges of two consecutive pulses should be 166 msec optimum with following limits:

- 183.7 msec maximum (162 rpm)
- 150.3 msec minimum (198 rpm)

(6) If the time displayed is out of tolerance (Step 4), adjust potentiometer R91 (refer to Figure 6-12) on the Reel Servo PCBA for 167 msec (180 rpm).

(7) Set the POWER control to OFF.

(8) Remove grounds and oscilloscope leads.

6.6.6.4 Loop Position Adjustments

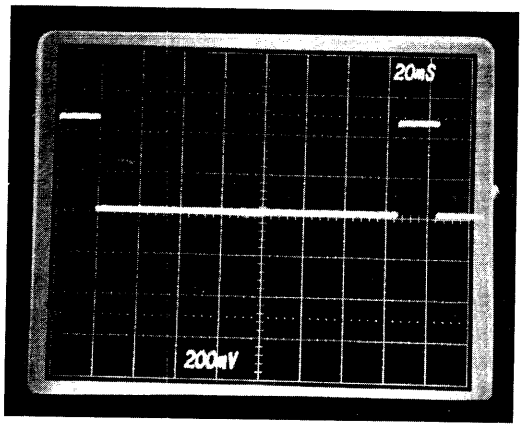
(1) Set the POWER control to OFF.

(2) Set maintenance switch S1, located on the Control M/M2 PCBA, in the center position.

(3) Set the reel servo disable switch S1, located on the Reel Servo PCBA, in the disable position (toward the rear of the cabinet).

(4) Disconnect capstan motor leads from the motor.

(5) Ground TP62 (NINTLK) and TP71 (PNU RETURN), located on the Control M/M2 PCBA.



PROBE: X10
HORIZ: 20mSEC/DIV
VERT: 0.2V/DIV
SYNC: DC + INT

3105

Figure 6-13. Takeup Reel Load Speed

(6) Mount a 267 mm (10½ inch) reel of tape on the supply reel hub.

(7) Open the buffer box door and hand thread the leader, winding approximately 7.6 m (25 feet) of tape on the takeup reel. Check to see that the BOT marker is on the tape that is wound on the takeup reel.

(8) Close the buffer box door.

(9) Set the POWER control to ON. Vacuum pressure should be evident immediately.

(10) Manually rotate the supply reel clockwise to put tape in the supply column. Verify that tape has formed a loop and that the end of the loop is located approximately in the center of the supply park zone (refer to Figure 4-8). Hold the reel, and apply masking tape to the reel and the transport to prevent the loop from being pulled down the column by the vacuum.

(11) Hold the tape against air bearing No. 4 (refer to Figure 3-2). Manually rotate the takeup reel in the counterclockwise direction to put tape in the takeup column. Verify that tape has formed a loop and that the end of the loop is positioned approximately in the center of the takeup column park zone (refer to Figure 4-8). Release tape at air bearing No. 4. Hold the takeup reel and apply masking tape to the reel and transport to prevent the loop from being pulled up the takeup column by the vacuum.

(12) Ensure that both loops are in approximately the center of their respective park zones.

(13) Press and release the RESET control.

(14) Check and adjust buffer box vacuum per Paragraph 6.6.9.

(15) Check and adjust air bearing pressure per Paragraph 6.6.9.

NOTE

Steps (14) and (15) are not the final adjustments for vacuum and air bearing pressure. Both are finally adjusted while running tape forward. However, the position signals for the loops (SPOS and TPOS) are dependent on the vacuum and air bearing pressures being within specifications. This necessitates checking vacuum and air bearing measurement before proceeding.

(16) Connect a DVM positive lead to TP55 (TPOS) and ground lead to TP49, located on the Reel Servo PCBA.

(17) Observe the DVM. The voltage displayed should be:

- + 0.2v dc maximum
- – 0.2v dc minimum

(18) If the voltage is out of tolerance, adjust potentiometer R103 on the Interconnect F PCBA (or R9 on Interconnect F1 PCBA) for 0v dc. Refer to Figure 6-3.

(19) Connect the DVM positive lead to TP66 (SPOS) on the Reel Servo PCBA.

(20) Observe the DVM. The voltage displayed should be:

- + 0.2v dc maximum
- – 0.2v dc minimum

(21) If the voltage is out of tolerance, adjust R203 on the Interconnect F PCBA (or R1 on Interconnect F1 PCBA) for 0v dc. Refer to Figure 6-3.

NOTE

These voltages are produced on the base assembly by the respective pressure transducers. Therefore, while performing Steps (16) through (21) it is imperative that the air measurements are within specifications and that the loops are centered in the respective park zones.

(22) Remove both grounds (NINTLK and PNU RETURN) on the Control M/M2 PCBA.

(23) Place reel servo disable switch S1, on the Reel Servo PCBA, in the forward position (reels enabled).

(24) Press RESET control.

(25) Reconnect capstan motor leads.

(26) Remove masking tape from both reels and trim.

(27) Place maintenance switch S1, on the Control M/M2 PCBA, towards the front of the transport (refer to Figure 6-5). The tape should drive in the forward direction.

(28) Make final vacuum and air bearing pressure adjustments per Paragraph 6.6.9.

(29) Drive tape, using maintenance switch S1, until 7.6 m (25 feet) of tape is on the takeup reel after BOT marker.

(30) Place a piece of masking tape on the buffer box window, so that it covers the center box bar. This bar separates the supply column from the takeup column. Mark the upper and lower limits of the supply park zone on the right side of the masking tape and the upper and lower limits of the takeup park zone on the left side of the masking tape.

(31) Connect a jumper between TP31 (shuttle maintenance test point) and TP25 (ground) on the Control M/M2 PCBA. The transport should run in the shuttle mode continuously.

(32) Observe the takeup tape loop (in the left-hand column). Loop travel region should be founded by the eighth and ninth holes from the top, and the tenth and eleventh holes from the bottom. Mark the masking tape to indicate the movement above and below the park zone and measure the loop travel. Refer to Figure 6-4.

(33) If the tape loop travel does not fall within the proper boundaries, adjust potentiometer R103 on the interconnect F PCBA (or R9 on interconnect F1 PCBA). Refer to Figure 6-3.

(34) Remove jumper from TP31 and TP25.

(35) Drive tape, using maintenance switch S1 on Control M/M2 PCBA, until approximately 7.6 m (25 feet) of tape is left on the supply reel before EOT.

(36) Repeat Step 31.

(37) Observe the supply tape loop (in the right-hand column). The loop travel region should be bounded by the tenth and eleventh holes from the top and the eighth and ninth holes from the bottom. Mark the masking tape to indicate movement above and below the park zone and measure the loop travel. Refer to Figure 6-4.

(38) Same as Step (33) except adjust R203 on the Interconnect F PCBA (or R1 on Interconnect F1 PCBA). Refer to Figure 6-3.

(39) Observe the tape loop travel in the supply and takeup columns. The loops must not break interlock and the maximum travel forward to reverse is:

- 266.7 mm (10.5 inches) for the supply loop
- 241.3 mm (9.5 inches) for the takeup loop

(40) Remove the masking tape from the buffer box door.

(41) Remove the jumper from TP31 and TP25 on the Control M/M2 PCBA.

(42) Perform dynamic break check per Paragraph 6.6.7, if needed.

6.6.7 DYNAMIC BRAKE CHECK

This procedure is to be accomplished on a new transport or when the Reel Servo PCBA is replaced. The procedure is to be done after Paragraph 6.6.6 has been accomplished.

(1) Open the supply reel door and install a 267 mm (10½ inch) work reel.

(2) Set POWER control to ON.

(3) Press and release LOAD/REW control.

(4) After tape motion stops and the BOT lamp lights, open the front of the transport to access the Card Cage and the Power Supply.

(5) Set switch S1, on the Control M/M2 PCBA, towards the front of the transport. The tape moves forward.

(6) Allow the tape to run to its mid-position.

(7) Set POWER control to OFF. The transport stops and the tape is not excessively spilled or marred.

(8) After inspecting the tape for damage, manually rewind the slack from the tape path.

(9) Set POWER control to ON.

(10) Set switch S1, on the Control M/M2 PCBA, to the middle position.

(11) Press and release LOAD/REW control. The tape loads and begins to run reverse to BOT.

(12) Set POWER control to OFF. The transport stops and the tape is not excessively spilled or marred.

(13) After inspecting the tape for damage, manually rewind the slack from the tape path.

(14) Set POWER control to ON.

(15) Press and release LOAD/REW control. The tape loads and begins to run reverse to BOT.

(16) After the transport has reached BOT, press and release UNLOAD.

(17) After the tape is unloaded, remove the work tape from the supply reel.

6.6.8 LOAD/CONTROL FUNCTIONAL ALIGNMENT

The Load/Control Functional Alignment provides the procedure for adjusting the tape-in-path amplifier and the tape-on-reel amplifier as instructed in Paragraphs 6.6.3 and 6.6.4.

6.6.9 AIR PRESSURE AND VACUUM ADJUSTMENT PROCEDURES

6.6.9.1 System Vacuum Adjustment (Buffer Box Vacuum)

(1) Set POWER control to ON.

(2) Mount and load a 267 mm (10½ inch) reel of tape.

(3) Open base assembly to gain access to the rear.

(4) Remove red cap from cripple reel port (refer to Figure 6-14A) and connect a differential air gauge with a range of 0 to 1270 mm (0 to 50 in.) of water. Use the low pressure input of the air gauge to measure vacuum.

(5) Place maintenance switch S1, on the Control M/M2 PCBA, toward the front of the transport to drive tape forward.

(6) Observe air gauge while tape is running forward, check for a system vacuum reading of: 838—889 mm (33—35 in.) water.

(7) If the reading is out of tolerance, loosen and adjust the buffer box adjustment screw (refer to Figure 6-14B) for a reading of 864 mm (34 in.) of water.

(8) Stop the tape, remove air gauge and replace red cap.

(9) Check takeup reel vacuum per Paragraph 6.6.9.3.

6.6.9.2 Air Bearing Pressure

(1) Set POWER control to ON.

(2) Mount and load a 267 mm (10½ inch) reel of tape.

(3) Open base assembly to gain access to the rear.

(4) Remove red cap from air bearing measurement port (refer to Figure 6-14B) and connect a differential air gauge with a range of 0—34 kilopascal (0—5 psi). Use the high pressure input of air gauge to measure pressure.

(5) Place maintenance switch S1, on Control M/M2 PCBA, toward the front of the transport to drive tape forward.

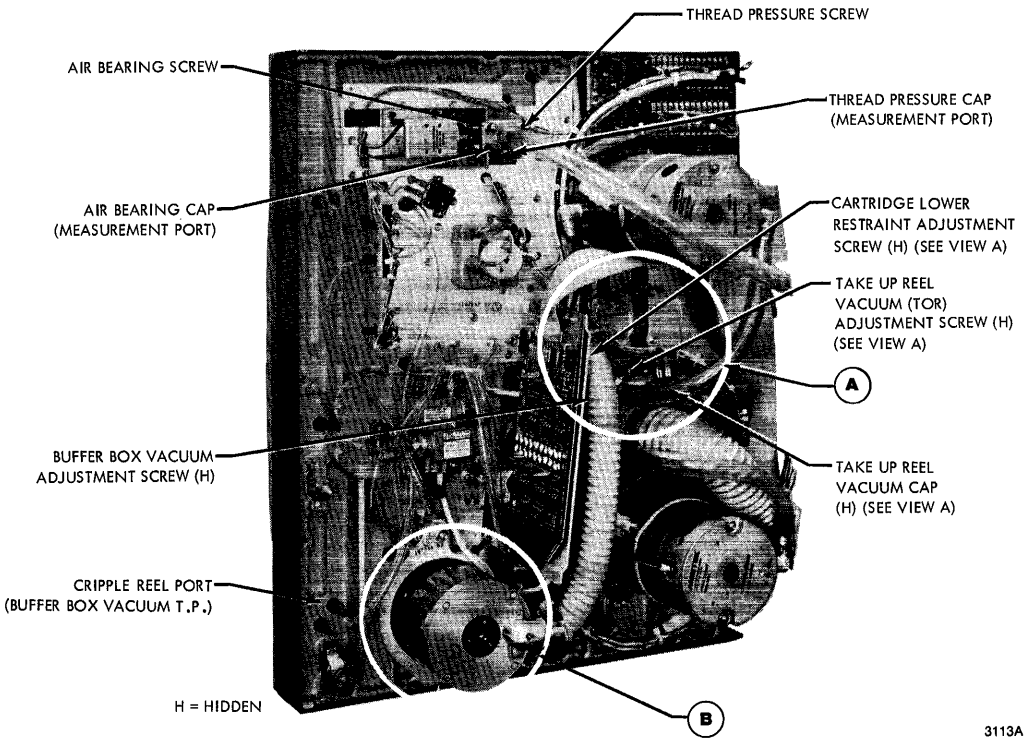
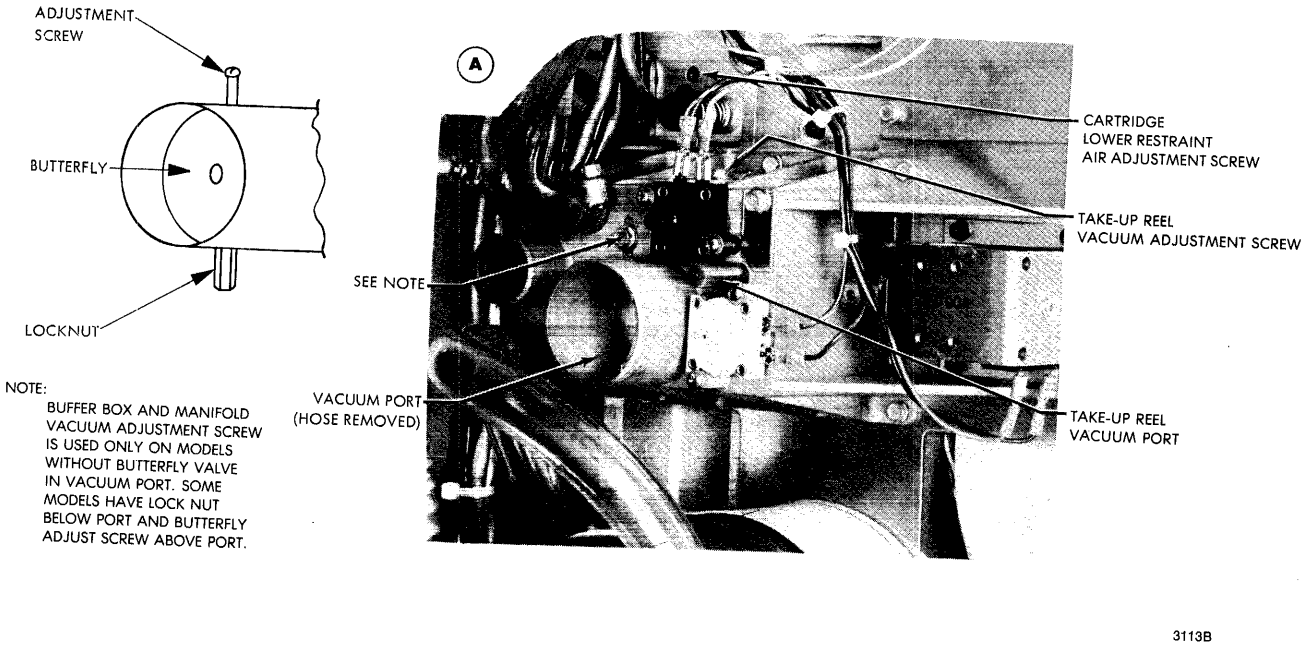


Figure 6-14A. Component Identification



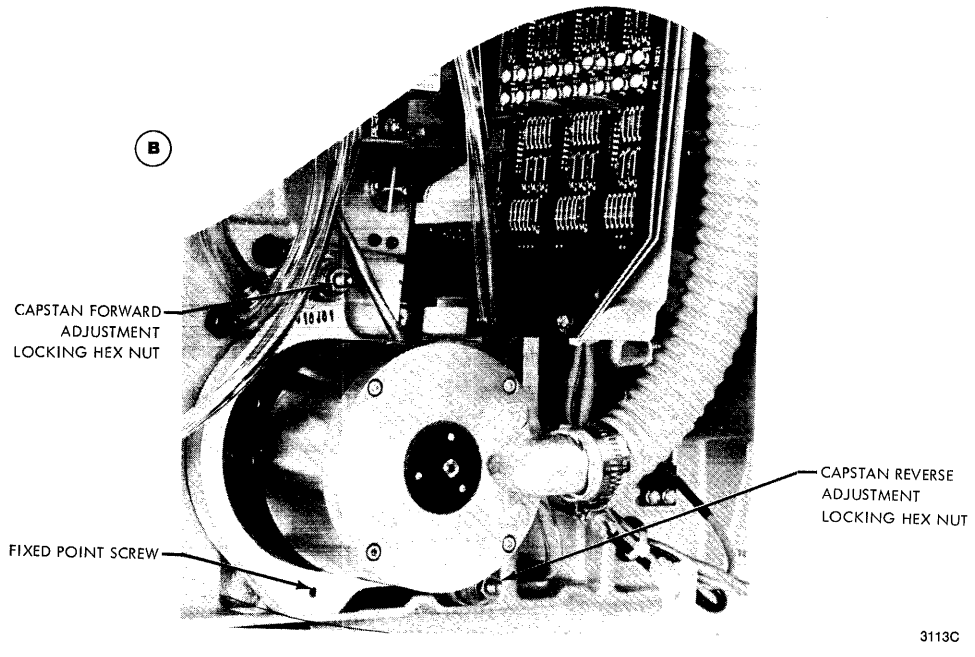


Figure 6-14B. Component Identification (Views A and B)

(6) Observe the air gauge while tape is running forward and check for an air bearing pressure reading of:
- 24 kilopascals (3.5 psig) minimum
- 29 kilopascals (4.25 psig) maximum

(7) If reading is out of tolerance, loosen the lock nut and adjust the air bearing screw for a reading of 27 kilopascals (4.0 psig).

(8) Tighten lock nut while observing air gauge to ensure adjustment is not disturbed.

CAUTION

EXCESSIVE TORQUE ON THE LOCK NUT WILL DAMAGE THREADS OF THE PORT. EXTREME CARE MUST BE EXERCISED.

(9) Stop the tape, remove air gauge and replace red cap.

(10) Unload the tape.

6.6.9.3 Takeup Reel Vacuum Adjustment (Tape on Reel Vacuum)

(1) Ensure that systems vacuum is within specified limits per Paragraph 6.6.9.1 before this adjustment is attempted.

(2) Set POWER control to OFF.

(3) Place disable servo switch S1, on the Reel Servo PCBA, toward the rear of the transport (servo disable position).

(4) Remove red cap from takeup reel vacuum port (refer to Figure 6-14A). Looking from the rear of the base assembly, this is the red cap in the upper right corner of the vacuum transfer valve, located between the vacuum preset switch S10 and the tape-on-reel switch S11.

(5) Connect a differential air gauge with a range of 0—1270 mm (0—50 in.) of water to the takeup reel vacuum port. Use the low pressure input to the air gauge to measure vacuum.

(6) Set POWER control to ON.

(7) Press and release the LOAD/REW switch.

(8) Immediately rotate the takeup reel three full turns to deactivate the load fault 0 function.

(9) Observe air gauge and check for a reading of:
- 508 mm (20 in.) of water, maximum
- 457 mm (18 in.) of water, minimum

CAUTION

THE SPECIFIED DUTY CYCLE FOR VACUUM AND AIR PRESSURE SOLENOIDS IS INTERMITTENT 3 MINUTES ON AND 9 MINUTES OFF; THEREFORE, THE UNIT SHOULD NOT BE HELD IN THIS MODE FOR OVER 3 MINUTES MAXIMUM, AFTER WHICH THE COIL SHOULD BE ALLOWED TO COOL FOR 9 MINUTES.

(10) If the reading is out of tolerance, loosen the takeup reel vacuum screw (located on top of the vacuum transfer valve), and slide the friction plate forward or backward to obtain a reading of 483 mm (19 in.) of water.

(11) Tighten screw while observing air gauge to ensure adjustment is not disturbed.

(12) Press and release RESET button.

(13) Remove air gauge and replace red cap. Place reel servo disable switch S1 in the forward direction (servo enable position).

6.6.9.4 Thread Block and Cartridge Pressure Adjustment

NOTE

The thread block pressure and cartridge pressure are interdependent and one adjustment directly affects the other. If one is varied, both must be checked alternately and readjusted to bring both within specified limits.

(1) Set POWER control to OFF.

(2) Place the servo disable switch S1, on the Reel Servo PCBA, toward the rear of the transport (servo disable position).

(3) Remove the red cap from the thread pressure measurement port (refer to Figure 6-14A) and connect a differential air gauge with a range of 0—1270 mm (0—50 in.) of water. Use the high input to the air gauge to measure pressure.

(4) Set POWER control to ON.

(5) Press and release LOAD/REW control. Immediately rotate takeup reel six full turns cw (as viewed from front) by hand. This deactivates load fault zero and causes the pressure solenoid to pick.

CAUTION

THE SPECIFIED DUTY CYCLE FOR VACUUM AND AIR PRESSURE SOLENOIDS IS INTERMITTENT 3 MINUTES ON AND 9 MINUTES OFF; THEREFORE, THE UNIT SHOULD NOT BE HELD IN THIS MODE FOR OVER 3 MINUTES MAXIMUM, AFTER WHICH THE COIL SHOULD BE ALLOWED TO COOL FOR 9 MINUTES.

(6) Observe air gauge and check for a reading of:

- 660 mm (26 in.) of water maximum
- 559 mm (22 in.) of water minimum

(7) If the reading is out of tolerance, loosen the locknut on the thread pressure screw and adjust the screw for 610 mm (24 in.) of water. Tighten locknut while observing air gauge to ensure adjustment is not disturbed.

CAUTION

EXCESSIVE TORQUE ON THE LOCKNUT WILL DAMAGE THE THREADS OF THE PORT. EXTREME CARE MUST BE EXERCISED.

(8) Press and release RESET control.

(9) Disconnect air gauge and replace red cap in the thread pressure measurement port.

(10) On the front panel, remove the hex socket head screw in the lower cartridge restraint and install the tube fitting (Pertec Part No. 107070-01).

(11) Connect a differential air gauge to the tube fitting. Use the high pressure input to the air gauge for measuring pressure.

(12) Repeat Step (5).

(13) Observe the air gauge and check for a reading of:

- 76 mm (3 in.) of water maximum
- 50.8 mm (2 in.) of water minimum

(14) If the reading is out of tolerance, adjust the lower restraint air adjustment screw for a reading of 63.5 mm (2.5 in.) of water.

(15) Press and release RESET control.

(16) Disconnect air gauge, remove tube fitting and replace socket screw.

(17) Steps (3) through (16) may have to be repeated several times to ensure integration of adjustments. Be sure to observe warning in Step (5).

NOTE

An alternative method to the preceding steps would be to acquire two differential air gauges. Connect both gauges to the respective adjustment ports and make adjustments while observing both gauges.

6.6.9.5 Solenoid Mechanical Adjustment

The air pressure and vacuum solenoids are both adjusted by physical repositioning. The pressure solenoid is mounted on the rear of the hinged base assembly near the top edge. The vacuum solenoid is located to the right of the vacuum supply base fitting, near the center of the base assembly. The procedure for adjusting either solenoid is as follows:

(1) Loosen the four screws that secure the solenoid mounting plate.

(2) Carefully move the spring-loaded plunger into the solenoid body (coil) to the end of its travel, using a screwdriver (applied behind the plunger linkage) as a lever. Move the solenoid body if necessary to ensure full travel (that is, until the valve poppet connected to the linkage, is seated).

(3) With plunger still held in position, move the solenoid body back toward the plunger until the plunger is seated in the body.

(4) Tighten the solenoid mounting plate screws.

(5) Move the plunger back and forth to verify that the movement is unrestricted. If not, reloosen the solenoid mounting plate screws and reposition the solenoid body to ensure free movement of the plunger throughout the entire travel distance.

6.6.10 READ FUNCTIONAL ALIGNMENT

The read functional alignment provides the procedures for adjusting all functions needed to ensure read data integrity. It also provides the order that each function should be checked in. Prior to starting the read functional alignment, it is necessary to ensure that the tape path is clean per Paragraph 6.5, that the voltages are correct per Paragraph 6.6.1, and that the capstan functional alignment is correct per Paragraph 6.6.5. The following functions should now be checked in the order given.

(1) Capstan motor adjustment and tape tracking

(2) GCR threshold adjustments

(3) GCR gain adjustments

(4) GCR read skew adjustment

(5) GCR character gate adjustment

(6) PE threshold adjustments

(7) PE gains

6.6.10.1 Tape Tracking and Head Azimuth Adjustments

The capstan motor is adjusted during the Read Functional Check when the motor has been replaced. Refer to Paragraph 6.7.5. An initial adjustment aligns the motor so the tape tracks over the surface of the guide block. A master skew tape is then used to perform a fine adjustment of the head. Adjustments are made at two motor mounting screws and the head azimuth screw.

(1) Set POWER control to ON.

(2) Load a work tape; run tape forward about 15 m (50 feet) using maintenance switch S1 on the Control M/M2 PCBA.

(3) Set POWER control to OFF.

(4) Open both reel doors, buffer box door, and the base assembly. Refer to Figure 6-14B.

(5) At the rear of base assembly at the capstan motor mounting plate, loosen the two hex jam nuts ½ to 1 turn (refer to Paragraph 6.7.5). These hex nuts are located at the forward and reverse tracking adjustment points. Make certain that the Belleville washers preload the mounting plate during adjustment procedure.

(6) At thread block 9, mounted on buffer box door, loosen two screws that secure the small cover (a cover is not used on some models).

(7) Slide cover, if any, open.

(8) At front of casting, approximately 50.8 mm (2 in.) down from the capstan, loosen the fixed point socket head cap screw ¼ turn. Loosen the capstan motor forward and reverse adjusting jam nuts a full turn.

(9) Remove rectangular ceramic guide from the guide block (refer to Paragraph 6.7.3).

CAUTION

EXTREME CARE MUST BE EXERCISED TO AVOID BREAKING THE CERAMIC GUIDE.

(10) Gently retract the spring-loaded ceramic guides at both the guide block and the air guide so that they lock back. Use a non-metallic instrument, such as the bare end of a Q-tip, to retract the guides. Retraction is accomplished by pushing the guide straight back with the Q-tip positioned in the middle of the guide.

(11) Close the buffer box door assembly.

(12) If a new capstan motor is being installed, perform a systems vacuum check per Paragraph 6.6.9; otherwise, turn power ON, conduct midreel load operation (refer to Paragraph 3.3.3), and go to the next step.

(13) Loosen motor jam nuts (refer to Paragraph 6.7.5) with hex socket key, inserted from the front through the openings provided, to align the hex of the jam nut with the hex of the adjustment stud.

(14) Perform the initial motor adjustment for tape tracking by inserting hex socket keys through the jam nuts and into the adjusting studs.

(15) Run the drive forward using maintenance switch S1 on the Control M/M2 PCBA, and adjust forward adjustment stud so tape edge is aligned with guide block edge in the area from which the rectangular ceramic guide was removed, looking through opening in block 9. Clockwise adjustment shifts tape away from base casting.

(16) Run the drive in reverse using maintenance switch S1 on Control M/M2 PCBA, and adjust reverse adjustment stud so tape edge is aligned with the guide block.

(17) Repeat steps (15) and (16) until tape is aligned with the guide block and no front-to-back movement occurs with tape moving in either direction. Shuttle maintenance test point TP31, on Control M/M2 PCBA, may be used per Paragraph 6.6.6.4, Step (31).

(18) Release the ceramic, spring-loaded guides and install the stationary ceramic guide.

(19) Lock the hex nuts in the back while holding the adjustment studs in place with hex socket key.

(20) Lock the jam nuts against the adjustment studs, and tighten the fixed point socket head screw.

(21) Verify that tape is still tracking correctly and make final adjustment if necessary.

(22) Unload work tape and load a master skew tape using instructions in Step (2).

(23) Connect channel 1 of an oscilloscope to TP203 (read head #4) of the GCR/PE Preamplifier PCBA (refer to Figure 6-8) and channel 2 to TP301 (read head #5). Ground oscilloscope to TP2. Sync internal positive on channel 1.

(24) Run tape forward and reverse by grounding shuttle maintenance test point TP31 on Control M/M2 PCBA.

(25) Observe the oscilloscope and adjust the head azimuth (refer to Paragraph 6.7.5) for minimum differential between TP203 and TP301 (outside two tracks of the read head).

If coincidence cannot be achieved, ensure that the differential is minimal and equal but opposite in the forward direction versus reverse direction. This indicates that tape tracking is straight forward and reverse, and that the head azimuth plate needs to be aligned. Refer to Figure 6-15.

(26) Remove jumper from TP31 on Control M/M2 PCBA. Remove oscilloscope connection from GCR/PE Preamplifier PCBA.

(27) Unload the master skew tape.

CAUTION

DO NOT REWIND. A MASTER SKEW TAPE SHOULD BE RUN FORWARD AND REVERSE AT NORMAL DRIVE SPEED ONLY, TO PRESERVE ITS INTEGRITY.

(28) Slide cover into place on thread block 9, and tighten screws.

6.6.10.2 Threshold Measurement

(1) Set POWER control to ON.

(2) Press LOAD/REW button and load columns with tape.

(3) Select On-line mode.

(4) Place a DVM between ground and TP23 on Read PCBA. (Refer to Figure 6-7).

(5) Select densities with either formatter, tape exerciser or from front panel (depending on configuration).

(6) Select hi or lo threshold with either formatter or tape exerciser.

(7) Select forward write or read with tape exerciser or formatter.

(8) Measure voltages as follows:

	PE (1600)	GCR (6250)
WRITE	3.0v	2.5v
READ LO	0.1v	0.1v
READ HI	1.0v	1.0v

6.6.10.3 PE Gain Adjustments

(1) Verify that power is ON.

(2) Load tape.

(3) Select PE density (1600 on DENSITY switch).

(4) Write 11001100. . . pattern on tape.

(5) Observe analog signal at GCR/PE Preamp 1 outputs (refer to Figure 6-8) with respect to ground.

(6) Adjust potentiometers R106, 206, 306, etc. on Read PCBA (refer to Figure 6-7) for 1.25v p-p output.

6.6.10.4 Read Skew Adjustment

(1) Load master skew tape.

(2) Select PE density or set AGC test switch on Read PCBA to PE gain position.

(3) Keep transport in Off-line mode.

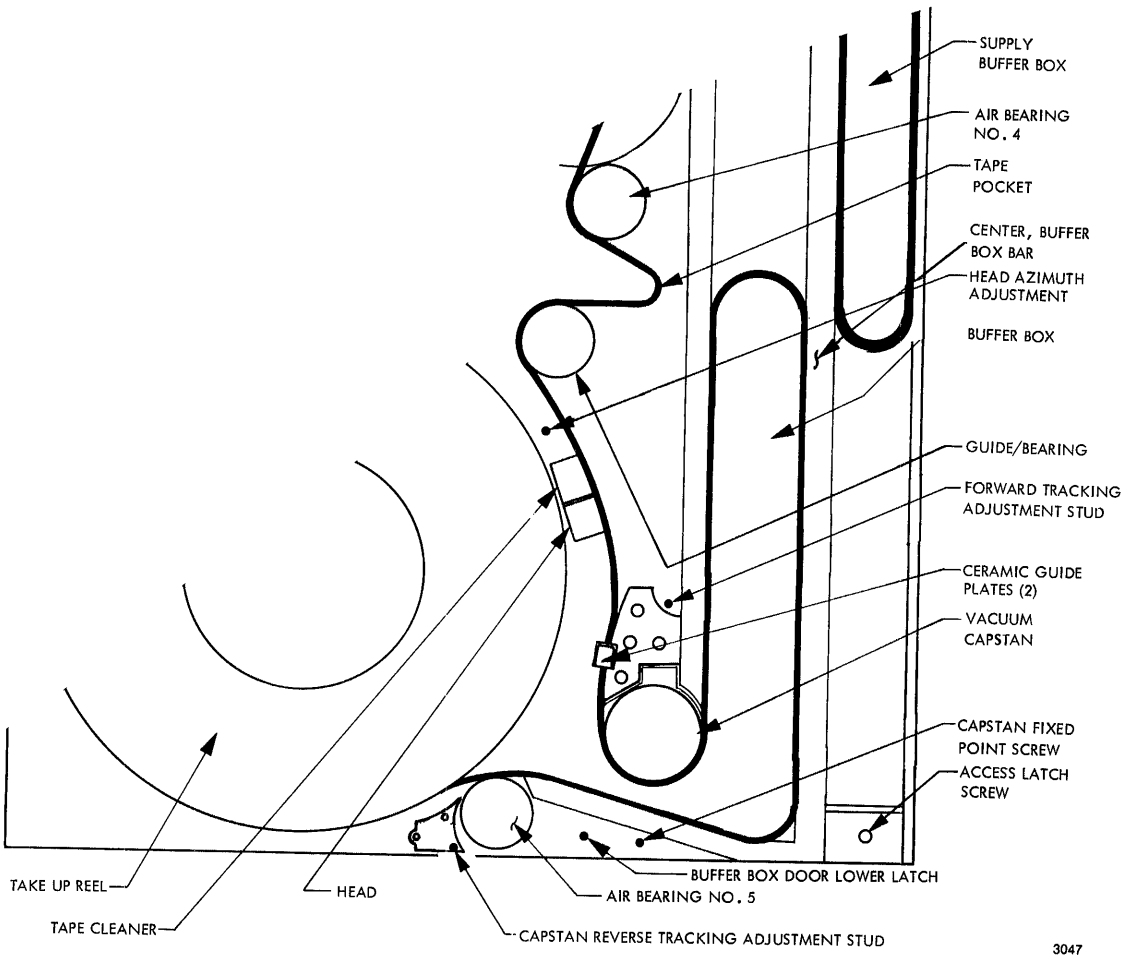


Figure 6-15. Front Base Panel Tape Tracking Adjustments

(4) Observe TP10 on Read PCBA.
(5) Move tape forward using maintenance switch on Control M/M2 PCBA. Refer to Figure 6-5.
(6) Observe waveshape as shown in Figure 6-16.
(7) Overlapping step shall not exceed 1.2 microseconds, corresponding to 150 microinches of (static + dynamic) skew.
(8) If skew is out of tolerance, open takeup reel door and adjust azimuth angle of head to obtain skew within these values.
(9) Use maintenance switch on Control M/M2 PCBA to move tape in reverse.
(10) Check tolerance of skew.
(11) Allow tape to reach BOT, then use UNLOAD switch on front panel to unload tape.
(12) Return maintenance switch on Control M/M2 PCBA to center position.

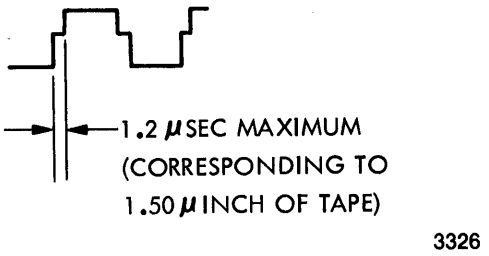


Figure 6-16. Read Skew Adjustment Waveforms

6.6.10.5 GCR Gain Adjustment

(1) Select GCR density; 6250 indicator on front panel will light.
(2) Load an all-1s tape.
(3) Set the AGC test switch on Read PCBA to AGC test (center) position. (Refer to Figure 6-7.)
(4) Measure output amplitude of tracks on the PE/GCR Preamp 1 PCBA. (Refer to Figure 6-8.) After 8 inches of tape have passed since the BOT marker, the amplitude should be not less than 0.8v p-p or more than 1.0v p-p.
(5) If output is not in accordance with (4), continue with the following steps.
(6) Set the AGC test switch on the Read PCBA to left position.
(7) Observe TP21 on Read PCBA.
(8) Pulse duration should be 36 msec, corresponding to 114.3 mm (4.5 inches) of tape.
(9) If duration is incorrect, adjust R35 on Read PCBA.
(10) Repeat Steps (1)—(4) to check output amplitudes.

6.6.10.6 Write Current Adjustment (PE)

(1) Connect a current probe as shown in Figures 6-17 and 6-18.
(2) Select PE mode; DENSITY 1600 indicator will light.
(3) Set AGC test switch on Read PCBA (refer to Figure 6-17) in AGC test (center) position.
(4) Put tape transport in On-line mode.
(5) Write all 1s (full frequency, infinite record).
(6) Observe Channel 2 I_W waveform. Refer to Figure 6-18.
(7) Adjust PE Pedestal potentiometer on Write PCBA (refer to Figure 6-19) to obtain pedestal amplitude of 28 mA (refer to Figure 6-18A).
(8) Adjust PE Step potentiometer to obtain 48 mA (refer to Figure 6-18A).
(9) Adjust PE Step Time potentiometer to 50 percent cell time (refer to Figure 6-18A).

6.6.10.7 Write Current Adjustment (GCR)

(1) Connect a current probe as shown in Figures 6-17 and 6-18.
(2) Select GCR mode; DENSITY 6250 indicator will light.
(3) Set AGC test switch on Read PCBA (refer to Figure 6-17) in AGC test (center) position.

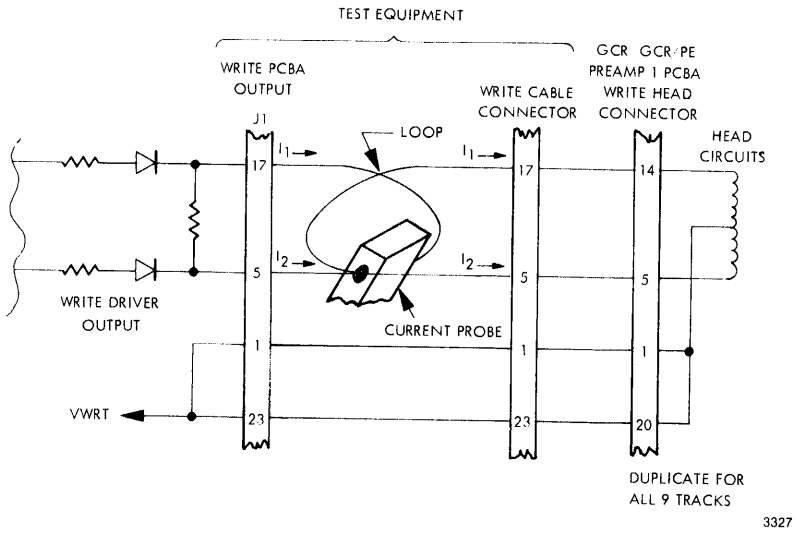


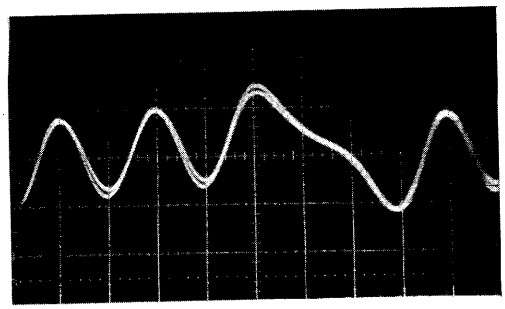
Figure 6-17. Write Current Probe Loop

(4) Put tape transport in On-line mode.
(5) Write all 1s (full frequency, infinite record).
(6) Observe Channel 2 I_W waveform. Refer to Figure 6-18A.
(7) Adjust GCR Pedestal potentiometer on Write PCBA (refer to Figure 6-19) to obtain pedestal amplitude of 14 mA (refer to Figure 6-18A).
(8) Adjust GCR Step potentiometer to obtain 24 mA (refer to Figure 6-18A).
(9) Adjust GCR Step Time potentiometer to 1/3 cell time (refer to Figure 6-18A).
(10) Observe analog read data at preamplifier output for Channel 2 on GCR/PE Preamp 1 PCBA. Refer to Figure 6-8.
(11) Calibrate the oscilloscope for one cell per division horizontal setting.
(12) Sync the oscilloscope on analog read signal.
(13) Change data pattern to 1111110011111100. . . (six 1s, two 0s, six 1s, two 0s, etc.).
(14) Shuttle tape back and forth (write forward, read reverse, etc.) while observing analog waveform.
(15) Note that forward and reverse waveforms are nearly identical. Refer to Figure 6-18, parts B through F while analyzing the oscilloscope readings.
(16) Adjust pedestal current (Steps 1 through 7) to compensate for critical differences in low frequency component of waveform.
(17) Adjust step current (Steps 1 through 6, 8 and 9) to compensate for critical differences in peak (transition) placement.

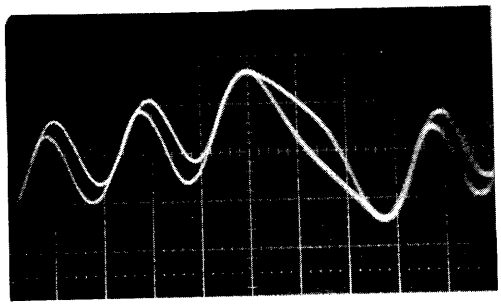
VERTICAL: 10 mA/DIVISION
HORIZONTAL: 1 CELL/3 DIVISIONS

A. IN SHOWING STEP TIME, PEDESTAL AMPLITUDE, STEP AMPLITUDE

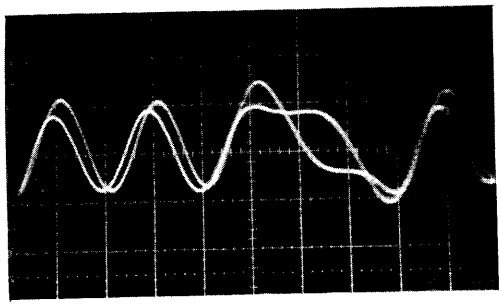
VERTICAL: 0.5V/DIVISION
HORIZONTAL: 1 CELL/DIVISION



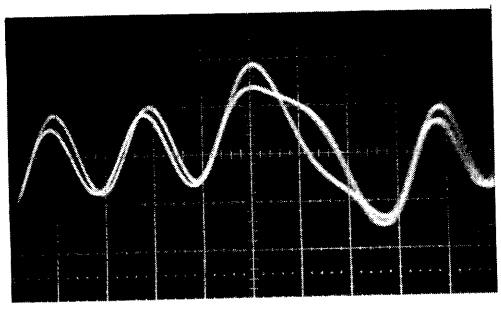
B. "BALANCED" WAVESHAPE. TWO TRACES INDICATE ANALOG WAVESHAPE IN FORWARD AND REVERSE DIRECTION.



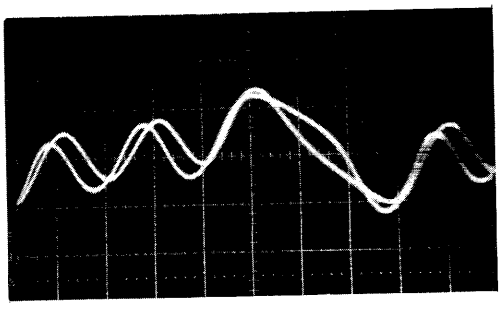
C. PEDESTAL TOO HIGH



D. PEDESTAL TOO LOW



E. STEP TOO HIGH



F. STEP TOO LOW

3328

Figure 6-18. Write Current Adjustment Waveforms

930D

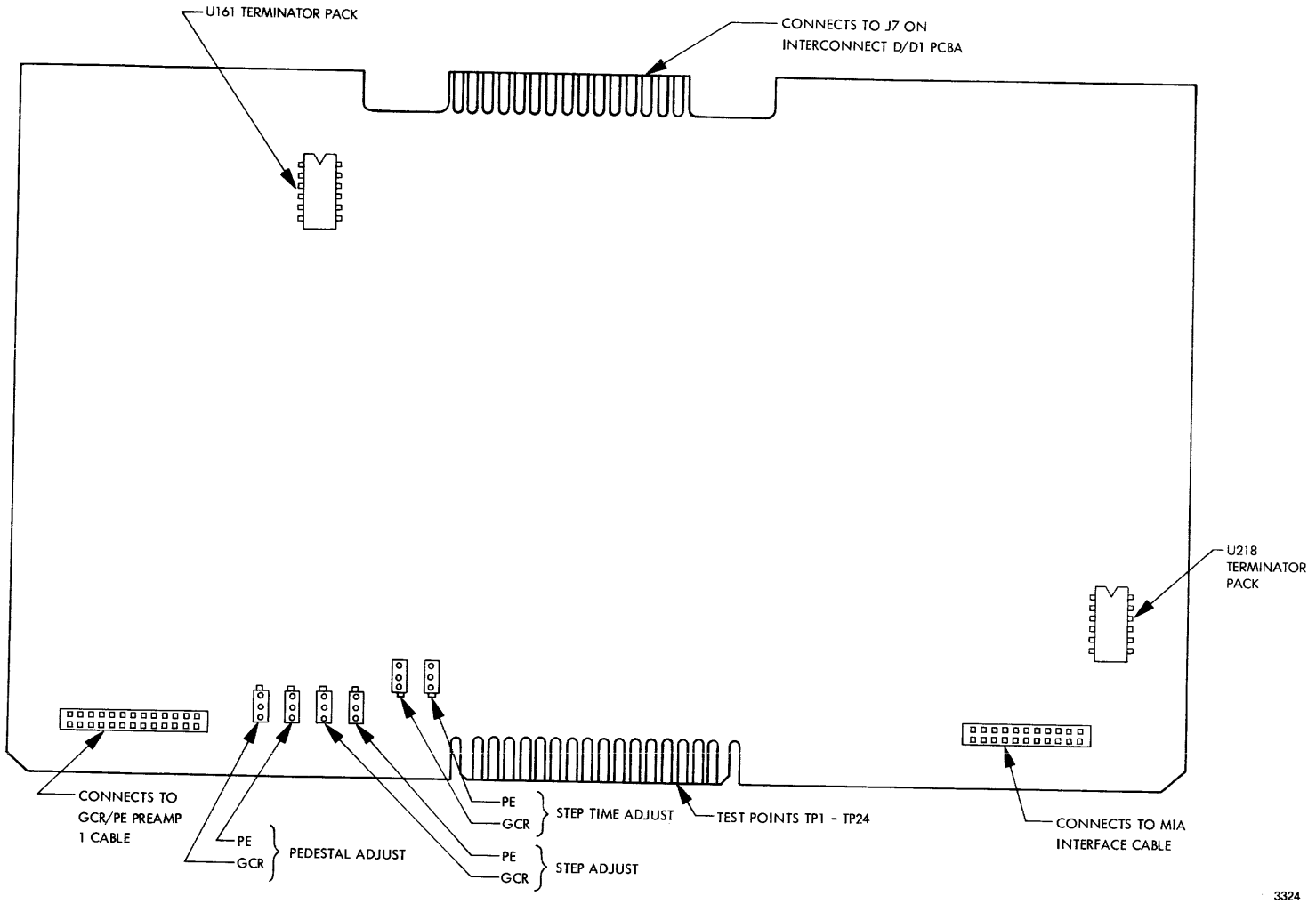


Figure 6-19. Write PCBA Test Point/Connector/Adjustment Locations

6.7 REMOVAL AND REPLACEMENT OF PARTS

The following paragraphs detail the procedures for removal and replacement of components and for making the associated adjustments.

6.7.1 HEAD REPLACEMENT PROCEDURE

The read-write-erase head assembly may require replacement for one of two reasons: internal fault in the head, or excessive wear. Head wear can be verified by measuring the depth of the wear on the head crown. In those heads that have guttering (grooves cut on the crown on each side of the tape path), the head should be replaced when it has worn down to the depth of the gutter. In those heads that do not have guttering, the head wear should be measured with a brass shim that is 0.254 mm (0.010 inch) thick. The shim width should be less than the minimum tape width, 12.598 mm (0.496 inch). Place the shim in the worn portion of the head crown with one side butted against the outer worn edge. The head should be replaced when the upper surface of the shim is below the unworn surface of the head crown, i.e., the head has worn to a depth greater than 0.254 mm (0.010 inch).

Replacement of the head is accomplished as follows.

(1) Set POWER control to OFF.

(2) Open both reel doors and the buffer box door to gain access to the latch, then swing base assembly on its hinges to gain access to internal parts.

(3) Remove the four hex head screws holding the GCR/PE Preamp 1 PCBA bracket to base assembly.

(4) Grasp the head assembly and remove two socket head screws holding the head against the head mounting plate.

(5) Remove the erase head leads from the PCBA. Carefully tip the bracket and disconnect the head from the PCBA.

(6) Check the head mounting plate and the replacement head for cleanliness of the mounting surfaces.

NOTE

The mounting surfaces must be free of all foreign substances or excessive skew may result.

To install the new head, repeat Steps (1) through (5) in reverse order, but do not tighten the head mounting screws or the PCBA bracket mounting screws. Note that white lead to erase head connects to J905 and black lead to J906.

(7) Initially align head by visually aligning lower edge of head with inclined edge of base metallic overlay. Bias head assembly by pressing it towards the right, into tape path, with finger pressure. Assure erease head contacts a sample section of magnetic tape. Lightly tighten the head mounting screws. Connect erase head wires to PCBA making sure white wire is closer to the operator.

(8) Set POWER control to ON.

(9) Load an all ones GCR/PE 366 c/mm (9042 cpi) tape on the transport and bring to Load Point.

(10) Operate the transport in a shuttling mode (i.e., forward, then reverse) by grounding TP31 on Control M/M2 PCBA.

(11) Using oscilloscope, observe waveform at TP101—TP901 on Read PCBA.

(12) While operating in the shuttling mode, mechanically rotate the GCR/PE Preamp 1 PCBA until the observed amplitude difference between forward and reverse operation is less than 600 mv peak-to-peak. Grasp the GCR/PE Preamp 1 PCBA on both the front and rear of base assembly to rotate it.

(13) Open buffer box door and verify that the erase head is in contact with tape. Repeat Step (12) if necessary.
(14) Tighten head mounting screws and PCBA mounting bracket screws.
(15) Perform related adjustments:
- Read functional alignment
- Write functional alignment

6.7.2 TAPE CLEANER REMOVAL, CLEANING AND ALIGNMENT

The tape cleaner may be removed and reinstalled as follows.

(1) Apply power and open both reel doors and the buffer box door.
(2) Remove two screws attaching tape cleaner and its cap to the base casting; refer to Figure 6-20.
(3) Clean tape cleaner, cap, clip, and metal overlay on base casting with a lint-free cloth moistened in 91 percent isopropyl alcohol. Wipe the tape cleaner blades and mounting surfaces carefully to remove all oxide and dirt.
(4) Reinstall tape cleaner and cap with clip on base assembly. Bias cleaner with finger pressure directed towards the right (towards the tape). Rotate cap so that formed clip is 1.524 mm (0.06 inch) away from the tape path. Slide clip against erase head.

6.7.3 AIR GUIDE/BEARING DISASSEMBLY AND CLEANING

The following details the procedure for checking and cleaning the air guide/bearing.

(1) Open both reel doors, remove seven trim assembly mounting screws. Close both doors and remove trim asembly from unit.
(2) Open both reel doors and buffer box doors.
(3) Remove thread block 3 permitting it to hang by its leads.
(4) Remove circular ceramic guide on front of base assembly; refer to Figure 6-20.

NOTE

Do not remove air guide from base assembly.

(5) Carefully insert the lens of a penlight into the front of the bearing. Using a small mirror, ensure that all orifices are open.
(6) Open any closed orifice by inserting a length of 34 awg wire or one strand of 19 strand 27 awg wire. Wire diameter should be 0.16002 mm (0.0063 inch).
(7) Wipe external bearing surfaces with a lint-free cloth moistened with 91 percent isopropyl alcohol. Also wipe ceramic guide.
(8) Assemble circular ceramic guide to air guide with edge parallel to pocket bar edge; refer to Figure 6-20.
(9) Reassemble thread block 3 to base assembly, adjusting its tip so it is 0.762 mm (0.03 inch) outside of the tape path at the tape cleaner; refer to Figure 6-20. Perform the adjustment by stretching a section of magnetic tape from the pocket lower bar past the head and guide block around the capstan.
(10) Replace trim assembly.

6.7.4 AIR BEARING REMOVAL AND CLEANING

There are five air bearings, excluding the air guide (refer to Figure 6-21). The air guide/ bearing check and cleaning is given in Paragraph 6.7.3. The air bearing procedure describes removal of the air bearings for cleaning. Since there are three different bearing versions on a transport, they should be disassembled and reassembled one at a time.

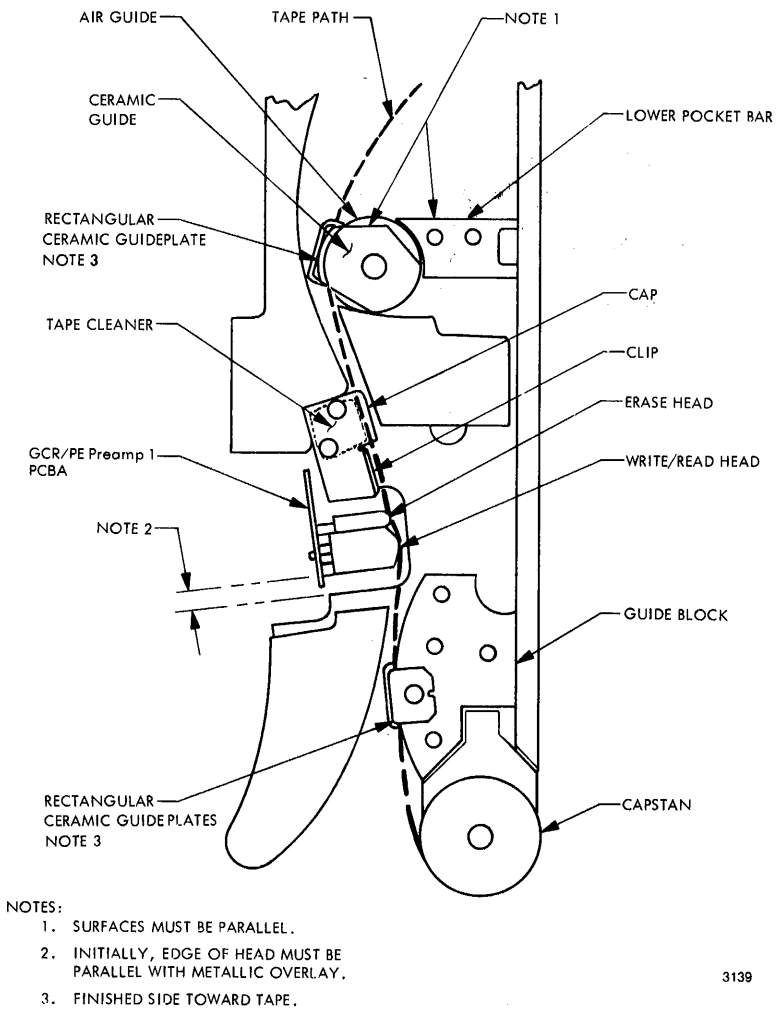


Figure 6-20. Head, Tape Cleaner Air Guide, and Guide Block Mounting

(1) Open both reel doors and buffer box door.

(2) Remove air bearing No. 1; refer to Figure 6-21. Clean parts using 91 percent isopropyl alcohol and a lint-free cloth. Examine air bearing orifices by inserting a penlight into the bearing. Open clogged orifices using 30 awg wire. Clean all surfaces of the air bearing, the circular ceramic guide (where used) and the bearing mounting area on metal overlay of the base assembly.

(3) A non-metallic straight edge is useful to rotationally align the air bearings on the base assembly. A straight edge can be cut from the cardboard on the back of any tablet. Cut the piece 152.4 mm long by 6.35 mm wide (6 inches by ¼ inch). The straight edge simulates the tape contact tangent line with the first row of holes.

(4) Reassemble air bearing No. 1 to base assembly. Rest cardboard against adjacent buffer box bar and bearing. Rotate bearing until first row of orifices are tangent to cardboard (Point A) and remaining orifices are in tape path area regions to float the magnetic tape. Shiny side of ceramic guide is mounted towards the magnetic tape. Align ceramic guides as illustrated in Figure 6-21.

(5) Follow the same procedure for air bearings No. 2, 4, and 5. Air bearing No. 3 tangent point A is aligned with adjacent bearing No. 2.

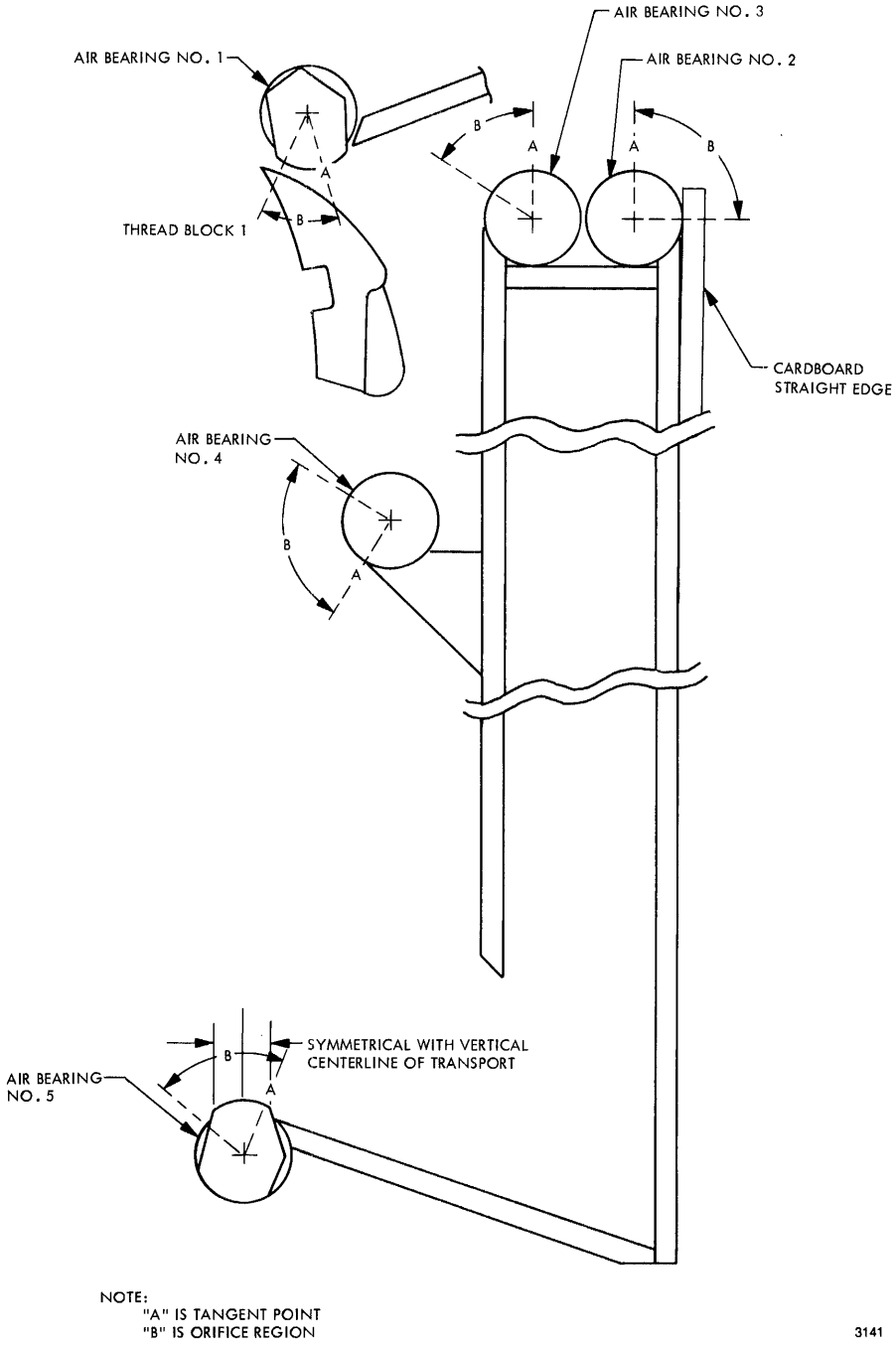


Figure 6-21. Air Bearing and Ceramic Guide Orientation

6.7.5 CAPSTAN MOTOR REPLACEMENT

The capstan motor may be replaced as follows.

(1) Set POWER control to OFF and CBI to OFF.

(2) At motor, disconnect wires, hose and tube. Remove tachometer wires from Interconnect F/F1 PCBA.

(3) Remove hex nuts, lockwasher, cup and Belleville washers, retaining motor plate to base assembly at two locations; refer to Figure 6-22.

(4) Cradle motor in hand. At front of base assembly, remove capstan fixed-point socket head cap screw, containing Belleville washers and plain washer, freeing the motor.

(5) Carefully slide motor off two adjusting studs making sure, by viewing the front of base assembly, capstan clears metal overlay and base casting.

(6) Install the replacement motor, repeat Steps (2) through (5) in reverse order.

(7) Set CBI to ON and POWER control to ON.

(8) Perform related adjustments. Refer to Paragraph 6.6.10.

6.7.6 SUPPLY REEL MOTOR REPLACEMENT AND HUB HEIGHT ADJUSTMENT

The supply reel motor may be replaced as follows.

(1) Set POWER control to OFF and CBI to OFF.

(2) Open both reel doors and buffer box door.

(3) Remove supply reel plastic overlay on front of base casting.

(4) Open base assembly.

(5) On back of base casting, above reel motor, remove access plate to supply reel motor shaft.

(6) Loosen screws of the reel hub without removing the hex nuts, using a 203.2 mm (8 inch) Phillips screwdriver inserted through hole in casting exposed by access plate. Normally only finger pressure is required to prevent the nuts of these screws from turning, but a small open-end wrench may be used and can be inserted from the front of the base assembly through the access cavities in the base casting behind the reel hub.

With the straddle plates of the reel hub in a horizontal position, and hex nuts facing down, remove the hub from motor shaft.

(7) At rear of base assembly, disconnect motor leads and cooling tubes from motor.

NOTE

Recognize the elbow alignments with respect to the motor and base assembly so that the elbows of the replacement motor are properly oriented.

(8) While supporting the motor, remove four motor mounting screws on the front of the base assembly. Remove the motor from the rear.

(9) Install the replacement motor, aligning elbows properly. Center motor in base casting clearance bore using centering tool (Pertec Part No. 107267-01). Tighten screws.

(10) On back of base assembly, slip the tubes over the elbows. Tighten hose clamps and attach motor leads.

(11) On front of base assembly, slip reel hub over motor shaft seating straddle plate on flat of shaft. Push hub towards base casting and lightly tighten both clamping screws. Adjust the hub flange so that it measures 11.4554 to 11.7094 mm (0.451 to 0.461 inch) from the machined boss on the base casting. This machined boss is directly behind the flange at 2 o'clock position.

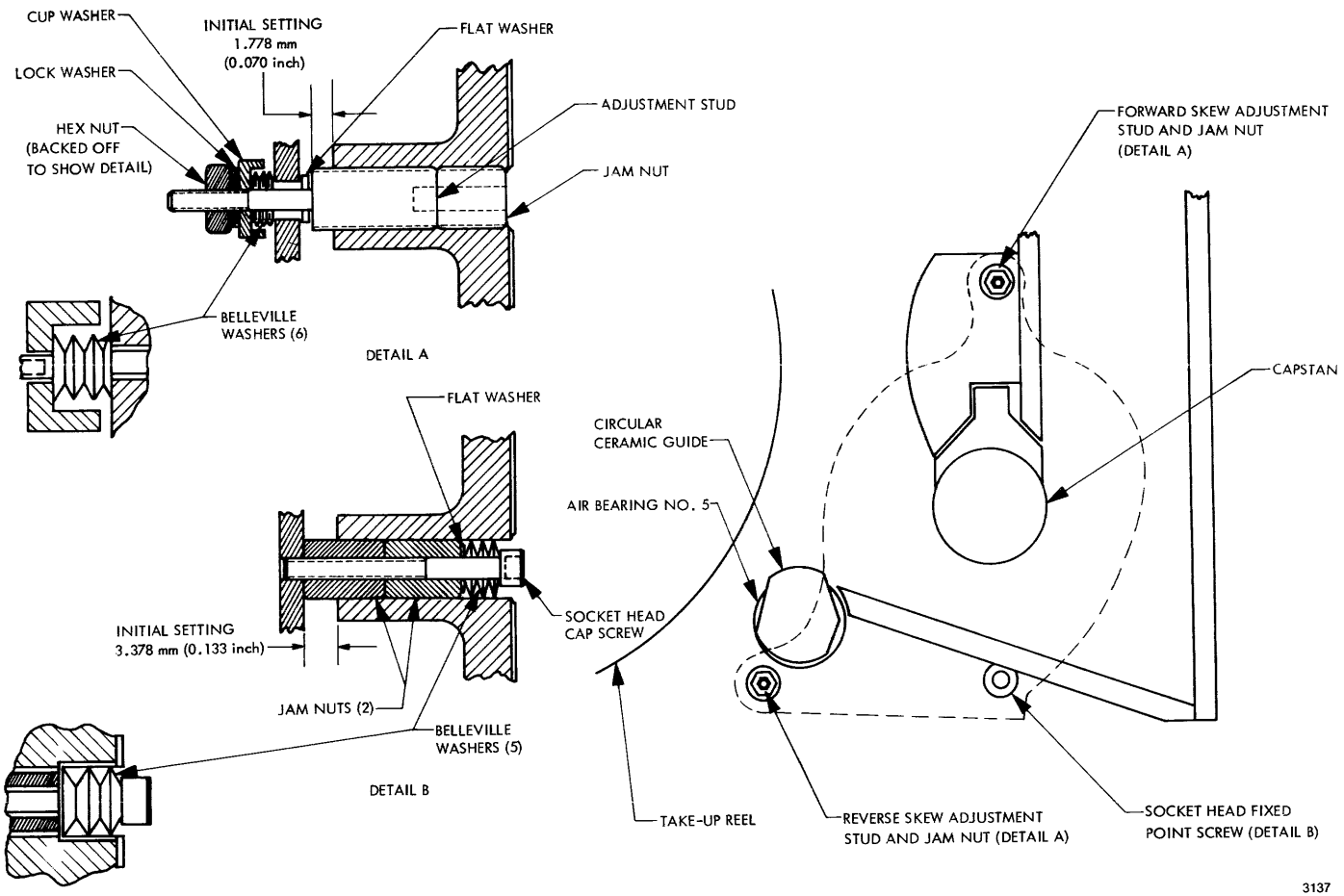


Figure 6-22. Capstan Tracking Alignment

(12) Torque both clamping screws evenly to 2.7 newton-meters (24 inch-pounds).

(13) Reassemble access plate to rear of base casting and supply reel overlay to the front.

(14) Set CBI to ON and POWER control to ON.

(15) Perform related adjustments:

- Supply reel load speed
- Run loop positions.

6.7.7 SUPPLY HUB GRIP RING REPLACEMENT

The following procedure can be used to replace the grip ring on the supply hub.

NOTE

This procedure requires a 24-hour waiting period for the adjustment screw lock compound to set. This down time can be avoided by replacing the entire hub assembly with a serviceable assembly in accordance with Paragraph 6.7.6, Steps (6) and (11).

(1) Set POWER control to OFF.

(2) Place the supply hub actuator in its locked position.

(3) Remove the Allen-head screw from the hole in the center of the actuator and remove the hub face assembly.

(4) Remove the plastic expansion ring around the actuator, along with the rubber grip ring; note the location of the two plastic notches on the expansion ring, with reference to the hub face assembly.

(5) Install the expansion grip ring kit (Pertec Part No. 109502-01).

(6) Align the slots in the hub face assembly with the notches on the expansion ring noted in Step (4).

(7) Reinstall the hub face assembly and partially tighten the Allen-head screw.

NOTE

The Allen-head screw adjusts the grip force exerted on the tape reel.

(8) Release (unlock) the supply hub actuator.

(9) Set POWER control to ON.

(10) Mount a reel of tape on the supply reel hub.

(11) Lock the supply hub actuator.

NOTE

If the tape reel binds as it is slipped on the hub, or the actuator is difficult to operate, loosen the Allen-head screw installed in Step (7) in small increments until the tape reel no longer binds.

CAUTION

IN THE FOLLOWING STEPS, HOLD THE REEL FIRMLY. AVOID APPLYING EXCESSIVE PRESSURE ON ONE FLANGE OF THE REEL.

(12) Manually turn the tape reel clockwise with one hand while holding the hub assembly with the other hand. If the reel slips on the hub, tighten the Allen-head screw in the center of the actuator, in small increments, periodically checking the grip force until the tape reel no longer slips.

(13) Set POWER control to ON.

(14) Load tape.

(15) Disconnect capstan motor leads and place tape motion maintenance switch S1, located on Control M/M2 PCBA, in the forward mode (towards the operator) to command counterclockwise reel motion.

(16) Manually turn the supply reel counterclockwise until the tape loop in the supply buffer box is 25.4 mm (1 inch) below the top interlock.

(17) Loosen the Allen-head screw until supply tape reel just starts to slip on the hub.

NOTE

As the supply tape reel slips on the hub while repeatedly performing Step (16), tighten the Allen-head screw in the center of the actuator until tape reel just stops slipping, then tighten Allen-head screw approximately ¼ turn.

(18) Manually turn the supply reel clockwise until tape loop is 267 mm (10½ inches) below the top interlock.

NOTE

If slippage occurs, repeat Step (17) while turning the supply reel clockwise.

(19) Place tape motion maintenance switch S1 in center position.

(20) Reconnect capstan motor leads.

(21) Unload the tape.

6.7.8 TAKEUP REEL MOTOR REPLACEMENT

The takeup reel motor can be replaced as follows.

(1) Set POWER control to OFF.

(2) Open both doors, remove the seven trim assembly mounting screws, close the doors and remove the trim assembly.

(3) Open the buffer box door and base assembly.

(4) On back of base assembly below the takeup reel motor, remove access plug to the vacuum reel hub.

(5) Through the access hole, loosen both screws retaining hub to shaft.

(6) At front of base assembly, remove vacuum reel.

(7) At rear of base assembly, disconnect motor leads and cooling tubes from motor.

NOTE

Recognize the elbow alignments with respect to the motor and base assembly so that the elbows of the replacement motor are properly oriented.

While supporting the motor, remove the four motor mounting screws on front of base assembly and remove motor from rear.

(8) Install replacement motor, aligning the elbows properly. Center motor in base casting clearance bore using centering tool (Pertec Part No. 107267-01) and tighten screws.

(9) On back of base assembly, slip the tubes over elbows. Tighten hose clamps and attach motor leads.

(10) Reinstall vacuum reel using buffer box bar (Pertec Part No. 107066-05) just above the lowest air bearing. Insert the bar between the vacuum reel flanges.

(11) Center reel flanges with respect to the bar and tighten screws of the vacuum reel hub. Rotate reel and listen for any rubbing with base casting bore. Repeat Steps (8) through (11) if necessary.

(12) Reassemble access plug and trim assembly.
(13) Set POWER control to ON.
(14) Perform related adjustments:
- Takeup reel load speed
- Run loop positions.

6.7.9 CARTRIDGE ACTUATOR MOTOR REPLACEMENT AND SWITCH ADJUSTMENT

The cartridge actuator motor can be replaced as follows.

(1) Set POWER control to OFF.
(2) Open reel doors and buffer box door.
(3) Remove supply reel plastic overlay.
(4) Remove arm from motor shaft by loosening set screw; refer to Figure 6-23.

NOTE

Recognize color and location of the two leads with respect to the motor so they can be connected to replacement motor properly.

(5) On back of base assembly, remove motor leads and hose clamp with RFI filter. Remove four motor mounting screws and remove motor. To install new motor, repeat Steps (4) and (5) in reverse order, setting arm at height shown in Figure 6-23.
(6) Set POWER control to ON.
(7) Press RESET control. Arm must rotate clockwise, then stop without bouncing and motor must stop driving. Adjust bottom limit switch if necessary.
(8) Press RESET control. Arm must swing counterclockwise then stop without bouncing, and motor must then stop driving. Adjust top limit switch if necessary.
(9) Reassemble supply reel overlay.

6.7.10 CONTROLS ASSEMBLY REMOVAL/REPLACEMENT

(1) Set POWER control to OFF, set CBI to OFF and disconnect power cord.
(2) Remove trim assembly per Paragraph 6.7.8.
(3) Open base assembly. Disconnect P10 from Control M/M2 PCBA and the gray wire and white wire from pins 3 and 4 of switch S2, located on inside of pneumatic motor mounting plate.

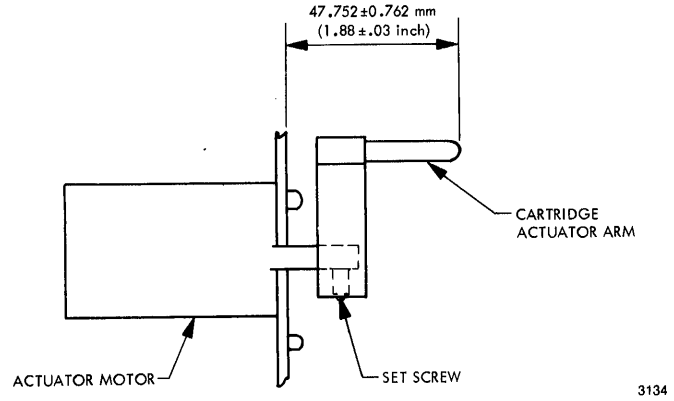


Figure 6-23. Cartridge Actuator Arm Adjustment

(4) Free the flat cable and two wires from all cable clamps.

(5) At front of base assembly, remove four control assembly mounting screws.

(6) Slide flat cable and two wires through base casting. Install replacement controls assembly. Reassemble in reverse order.

6.7.11 BLOWER/COMPRESSOR AC MOTOR REPLACEMENT

Use the following procedure to remove and replace the blower/compressor ac motor.

WARNING

IF THE AC MOTOR HAS STOPPED BECAUSE OF OVER-TEMPERATURE, IT WILL RESTART WHEN THE OVER-TEMPERATURE CONDITION CEASES TO EXIST. ALWAYS TURN OFF OR DISCONNECT AC POWER BEFORE WORKING NEAR MOTOR PULLEYS AND BELTS.

(1) Set POWER control to OFF, set CBI to OFF and disconnect power cord.

(2) Remove belt guard and remove both belts by manually rotating pulleys clockwise and slipping belts off.

NOTE

It is not necessary to loosen mounting screws for the compressor or blower.

(3) Remove pulley set from motor shaft. Do not separate the pulley set.

(4) Remove transformer mounting screws in front of power pack assembly and lift transformer.

CAUTION

TRANSFORMER SHOULD NOT BE LIFTED BY ONE MAN.

(5) Remove cover to motor leads and remove leads.

(6) Remove four mounting screws at rear of power pack assembly and remove motor from the front.

(7) Install replacement motor.

(8) Reassemble in reverse order aligning pulley on shaft set; refer to Figure 6-24. Manually rotate motor clockwise and check that both belts track completely on pulleys. Some slight shift of motor pulley may be necessary.

(9) Reconnect power cord, set CBI to ON and set the POWER control to ON.

(10) Perform related adjustments:

- Air pressure
- Air vacuum.

6.7.12 BLOWER REMOVAL AND REPLACEMENT

(1) Set POWER control to OFF, set CBI to OFF and disconnect power cord.

(2) Remove belt guard. Remove hose from top of blower.

(3) Loosen blower mounting screws. Slide blower left and slip belt off pulley; refer to Figure 6-24.

NOTE

Do not loosen blower pulley from shaft. Replacement blowers have pulley properly located on shaft.

(4) In front of power pack assembly, remove capacitor chassis mounting screws. Position chassis towards transformer.

(5) Remove hose from end of blower.

(6) Remove blower mounting screws and remove blower.

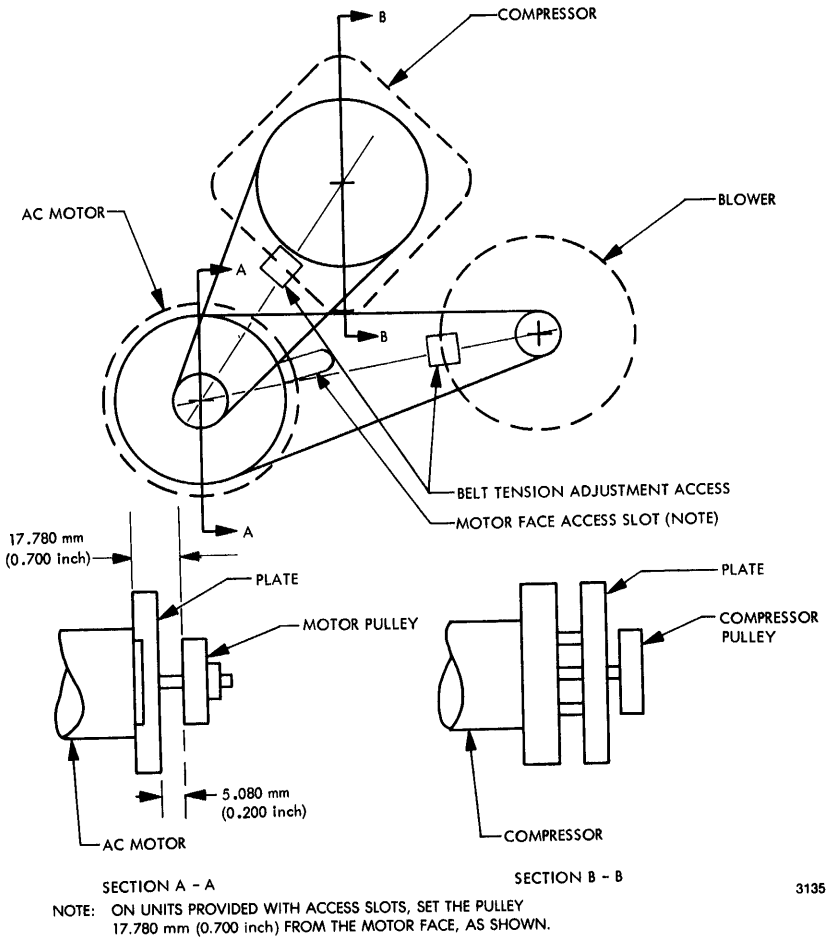


Figure 6-24. Blower and Compressor Drive Alignment

(7) Install replacement blower.
(8) Reassemble in reverse order using Steps (3) through (6).
(9) Exert approximately 111.2 newtons (25 pounds) of force on blower while tightening the three blower mounting screws to tension the belt. A slot is provided in the mounting plate to pivot a large screwdriver against the blower housing for tensioning the belt.
(10) Attach hose to top of blower and assemble belt guard.
(11) Connect power cord, set CBI to ON, and set POWER control to ON.
(12) Perform related adjustments:
- Air pressure
- Air vacuum.

6.7.13 COMPRESSOR REMOVAL AND REPLACEMENT

(1) Set POWER control to OFF, set CBI to OFF and disconnect power cord.

(2) Remove belt guard. Remove tubes from top of compressor.

(3) Loosen compressor mounting screws. Slide compressor left and slip belt off pulley.

(4) Remove pulley from compressor.

(5) Remove capacitor chassis mounting screws in front of power pack assembly and position chassis towards transformer.

(6) Remove compressor mounting screws and remove compressor.

(7) Transfer fittings to replacement compressor.

(8) Install replacement compressor.

(9) Reassemble in reverse order using Steps (3) through (6) and setting pulley position according to Figure 6-24.

(10) Exert approximately 111.2 newtons (25 pounds) force on compressor while tightening the four compressor mounting screws to tension the belt. A slot is provided in the mounting plate to pivot a large screwdriver against the compressor housing for tensioning the belt.

(11) Attach tubes to top of compressor. Manually rotate motor pulley clockwise and check that compressor belt does not overhang pulleys; readjust compressor pulley if necessary.

(12) Connect power cord, set CBI to ON, and set POWER control to ON.

(13) Perform related adjustments:

- Air pressure
- Air vacuum.

6.8 TROUBLESHOOTING

The system troubleshooting procedure (Table 6-4) should be used in conjunction with the Turnon and Checkout Procedure (Figure 2-2). Steps in the troubleshooting table are correlated with Steps in Figure 2-2. The troubleshooting steps are divided into substeps [(a), (b), (c), etc.] to assist in isolating faults which can cause the transport to fail to respond to the Turnon and Checkout Procedure Steps. The normal responses are detailed in the various columns of Figure 2-2. Failure of the normal responses will provide a substep symptom covered in Table 6-4.

WARNING

IF THE AC MOTOR HAS STOPPED BECAUSE OF OVER-TEMPERATURE, IT WILL RESTART WHEN THE OVER-TEMPERATURE CONDITION CEASES TO EXIST. ALWAYS TURN OFF OR DISCONNECT AC POWER BEFORE WORKING NEAR MOTOR PULLEYS AND BELTS.

Table 6-4
System Troubleshooting

Step	A = Operator Action B = Normal Machine Response	Fault	Probable Cause	Remedy
1A	Set main circuit breaker CB1 to ON. Set density to 6250	Fan does not run	No ac power to fan	Check ac power circuits
			Fan jammed	See that fan blades are free
1B	Fan (optional) runs	Front panel indicators lighted or pneumatic circuit active	Bad solid-state relay (shorted)	Check relay
2A	Set front panel POWER switch to ON	All lamps remain off	No +5v to panel	Check +5v supply voltage
				Check +12v supply voltage
				Check for loose or open connection
2B	6250, POWER and FILE PROTECT lamps light	One or more lamps stay off	Bad LED(s)	Replace LED(s)
			Open or loose connection(s)	Check indicator wiring
3A	Press and release LOAD/REW, no tape mounted	Transport dead	No power	Check for +12v, ±24v, ±36v
			LOAD/REW control bad	Check switch circuit and connections
3B	Motor runs, takeup and supply reels run, cartridge motor runs. After 10 seconds delay, motors stop and Load Fault lamp lights	Load fault	Cartridge motor fault	Check +5v, +12v, +15v and +24v supplies and connections
				Bad Capstan/Regulator PCBA
		Cartridge does not open	Cartridge motor circuit fault	Check +5, +12v, +15v and +24v supplies and connections
				Bad Capstan/Regulator PCBA
		Takeup & supply reels do not run	No power to motors	Check +36v supply and connections
				Maintenance switch on Reel Servo PCBA off
				Bad Reel Servo PCBA
		No pneumatics	No power to motors	Check +12v supply and connections
				Check relay and connections
			Bad motor	Maintenance switch on Reel Servo PCBA off
				Replace motor
		Motors run at high speed	Bad amplifier	Check Reel Servo PCBA
4A	Press and release RESET switch	Cartridge motor does not return to closed position	Bad cartridge motor circuit	Check motor circuit wiring for loose or open connection
4B	Load Fault LED turns off, cartridge motor runs and stops in closed position			Bad Capstan/Regulator PCBA
5-1A	Load a 267 mm (10½ in.) cartridge reel (with write enable ring in place). Press LOAD/REW	Tape fails to enter path	End of tape damaged	Remove bad end from tape
			Speed wrong	Check supply reel load speed
			Air-bearing pressure wrong	Check air-bearing pressure
			Transfer valve faulty	Replace transfer valve
5-1B	Transport will load tape to takeup reel. If unsuccessful, load fault LED lights and transport stops until Reset switch is pressed	Tape loops will not set	Speed wrong	Check takeup reel load speed
				Buffer box
				Bad Control M/M2 PCBA

Table 6-4
System Troubleshooting (Continued)

Step	A = Operator Action B = Normal Machine Response	Fault	Probable Cause	Remedy
5-2A	Load a 178 mm or 216 mm (7 or 8½ in.) reel. Note the leader must be manually fed between the threadblock and air bearing before pressing LOAD/REW	Tape enters path but will not servo to center	Low vacuum	Check vacuum circuit for pinched hose or open connection
			Bad Reel Servo	Check Reel Servo PCBA
			Bad transducer	Check transducer and limit switch. Check for loose or open connections
5-2B	Transport will load tape to takeup reel. If unsuccessful, Load Fault LED lights and transport stops until RESET switch is pressed	Tape leaves path during reverse to BOT	Bad C/R PCBA	Check Capstan/Regulator PCBA
			Bad Tach signal	Bad Interconnect F PCBA
				Check for loose or open connections. Bad Control M/M2 PCBA
		Tape does not stop at BOT	Bad BOT sensor	Check BOT/EOT circuits
			No BOT tab on tape	1. 100 mv with blank or no tape tab 2. 2v with either tab in sensor
		Load Fault indicated	Check Load Fault test points & correlate with flow chart for cause	
6A	Press and release ON LINE	Lamp stays on	Bad Control M/M2 PCBA	Check wiring for shorts or bad PCBA
6B	ON LINE LED lights or extinguishes	Lamp stays off	Faulty LED	Replace LED
			Loose or open connections	Check wiring for loose or open connections
7A	Set density to 1600	No change	Bad LED	Replace LED
7B	1600 density LED lights		Machine On Line	Machine must be off line to change density if W2 on Control M/M2 PCBA is removed.
8A	Press and release UNLOAD	Transport fails to unload	Bad switch or wiring	Check switch and wiring
8B	Transport unloads		Bad Control M/M2 PCBA	Replace Control M/M2 PCBA
			Shorted solid-state relay	Replace relay

SECTION VII
PARTS LISTS, LOGIC LEVELS AND WAVEFORMS, AND SCHEMATICS

7.1 INTRODUCTION

This section includes illustrated parts lists, recommended spare parts lists, logic level and waveform definitions, and schematic and assembly drawings.

7.2 ILLUSTRATED PARTS BREAKDOWN

Figures 7-1 through 7-4, used in conjunction with Tables 7-1 through 7-4, respectively, provide identification by Pertec part number of the mechanical and electrical components involved in normal maintenance procedures.

7.3 RECOMMENDED SPARE PARTS

Table 7-5 provides a list of recommended spare parts for the T1000 and FT1000 tape transports. The customer should always furnish model and serial numbers of the transport when ordering parts.

An additional recommended spare parts list containing the part number, description, current price for component parts, subassembly parts, and special tools is also available. This list can be obtained by providing the unit part number from the ID label to Spares Administration, Pertec, P.O. Box 2198, Chatsworth, CA 91311.

7.4 PART NUMBER CROSS REFERENCE

Table 7-6 provides a cross reference to the manufacturer's part numbers and typical Pertec part numbers.

7.5 LOGIC LEVELS AND WAVEFORMS

The transport control and interface logic uses the TTL logic elements. Logic levels are defined as nominal + 5v logical false, and nominal 0v logical true.

All mnemonics for interface lines connecting the transport to the controller are prefixed by 'I'. Each line must be terminated at the receiver end of the cable by a 220/330-ohm divided chain between + 3v and + 0.4v.

All interface waveforms are low-true with logic levels defined as + 3v logical false and + 0.4v logical true. For example, ISFC (SYNCHRONOUS FORWARD COMMAND) will be 0.4v when the transport is being driven in the forward direction, or + 3v otherwise.

Internal logic may be high = true or low = true, depending on the point in the circuit where the voltage is measured. A mnemonic term on a schematic at a certain point will be high = true unless the mnemonic term starts with an 'N', in which case low = true (e.g., TIP indicated the tape-in-path signal is high when true; NTIP indicates that the same signal is low when true).

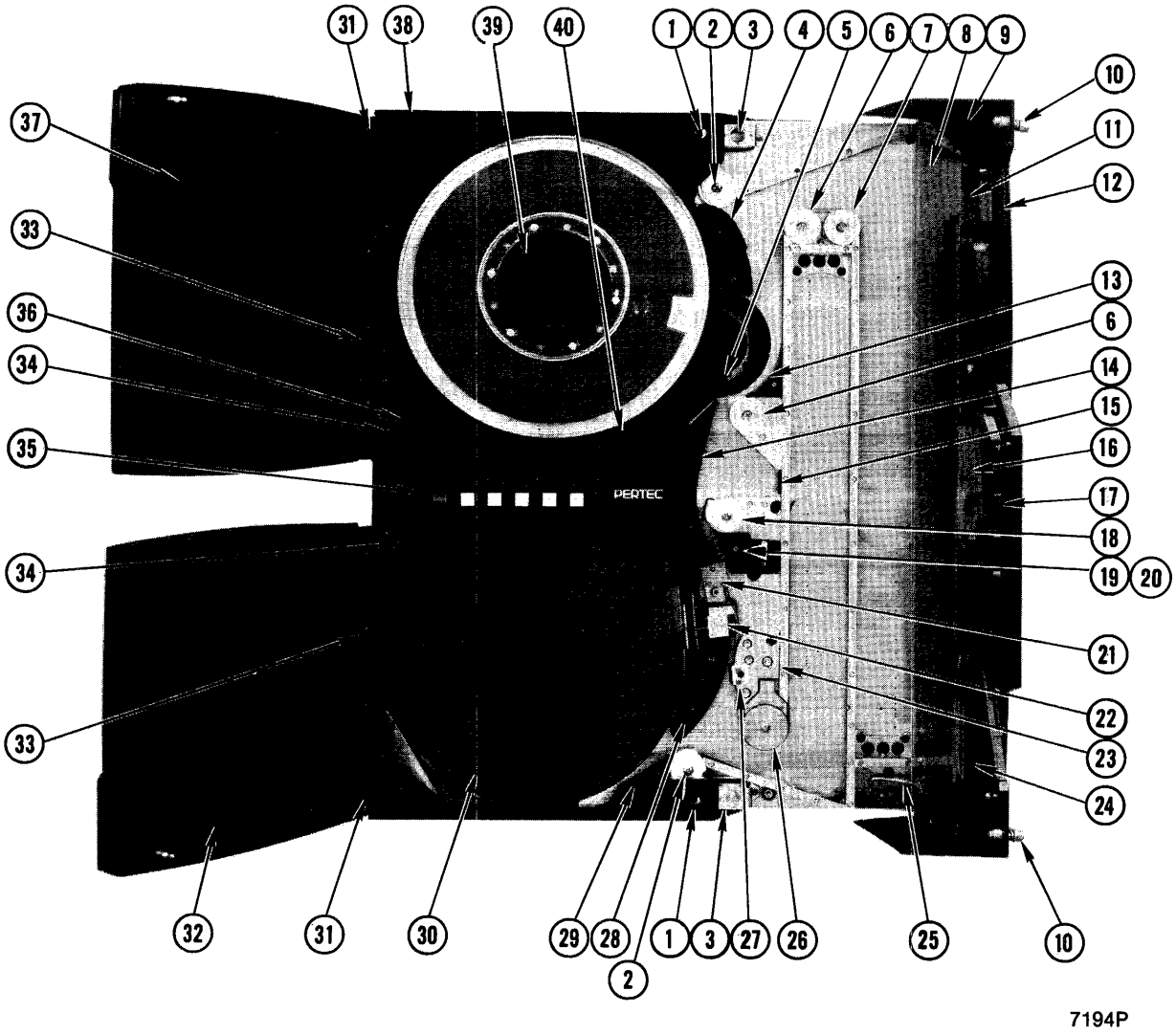


Figure 7-1. T1000 and FT1000 Series Photo Parts Index

Table 7-1
T1000 and FT1000 Photo Parts List

Figure and Index No.	Part No.	Description	Figure and Index No.	Part No.	Description
Figure 7-1			25	109513-01	Door Stop Rod
1	615-0006	Catch Spring	Not shown	109541-01	Door Rod and Bracket Replacement Kit
2	107061-01	Ceramic Circular Plate Guide			
	107140-01	Air Bearing (behind guide)	26	107098-01	Capstan
3	109564-01	Buffer Box Door Latch Kit	27	107058-01	Ceramic Rectangular Plate Guide
4	110129-01	Thread Block No. 1 Replacement Kit	28	107160-05	Thread Block Assembly with Liner
5	107103-01	Arm, Cartridge Loading		107170-05*	Liner
	506-6360	Switch, for S6, S7	29	107160-06	Thread Block Assembly with Liner
6	107140-02	Air Bearing		107170-06*	Liner
7	107140-03	Air Bearing	30	107009-01	Vacuum Reel Assembly
8	107071-01	Buffer Box Window	31	107158-01	Tube, Door Stop
9	107175-01	Retainer (6 places)		107159-01	Rod, Door Stop
	606-0600	Flat Washer (6 places)		107154-01	Bracket, Door Stop, Lower Only
	608-3712	Screw (6 places)		108493-01	Bracket, Pivot, Upper Only
10	109564-01	Buffer Box Door Latch Kit	32	107119-01	Door, Lower
11	107277-01	Thread Block 7		615-0078	Ball Stud
12	107120-01	Buffer Box Door	33	107173-01	Door Hinge (2 places)
13	107272-01	Thread Block 2	34	109533-01	Slotted Plug
14	107013-01	TIP Assembly	35	107022-01	Controls Assembly w/Logo, 800/1600 (T1640, FT1640)
	107170-03*	Liner		107022-02	Controls Assembly w/Logo, 6250/1600 (T1940)
15	108463-01	Pocket Pad		514-0010	Switch, Rocker
16	107072-01	Buffer Pocket Window		514-0011	Switch, Momentary (4 places)
17	107278-01	Thread Block 8		506-0011	Switch, Rocker, Power
18	107061-01	Ceramic Circular Plate Guide		506-6303	Switch, Thumbwheel Select
	107058-01	Ceramic Rectangular Plate Guide	36	506-9206	Switch, Interlock
	107059-01	Air Guide	37	107118-01	Door, Upper
19	107012-01	EOT/BOT Assembly		615-0078	Ballstud
20	107274-01	Thread Block 4	38	107122-01	Trim
21	107029-01	Tape Cleaner (T1640)	39	108844-01	Reel Hub Assembly
	107029-02	Tape Cleaner (T1940)		109502-01	Friction and Expansion Ring Kit
	107202-01	Clip, Tape Cleaner Cap	40	107236-01	Reel Sense Assembly
	107030-01	Tape Cleaner Cap	Not shown	616-0024	Compression Spring (21 places, buffer box assembly)
22	530-6099	Head (T1940)		109532-01	Door Interlock Switch Plunger (Optional)
	530-6369	Head (T1640, FT1640)		109530-01	Safety Interlock Switch Assembly (Optional)
23	107083-01	Guide Block			
24	107279-01	Thead Block 9			

*Thread Block Liners affixed with adhesive activator Pertec Part No. 667-0111

Thread Block Liners not specified are Pertec Part No. 667-0110.

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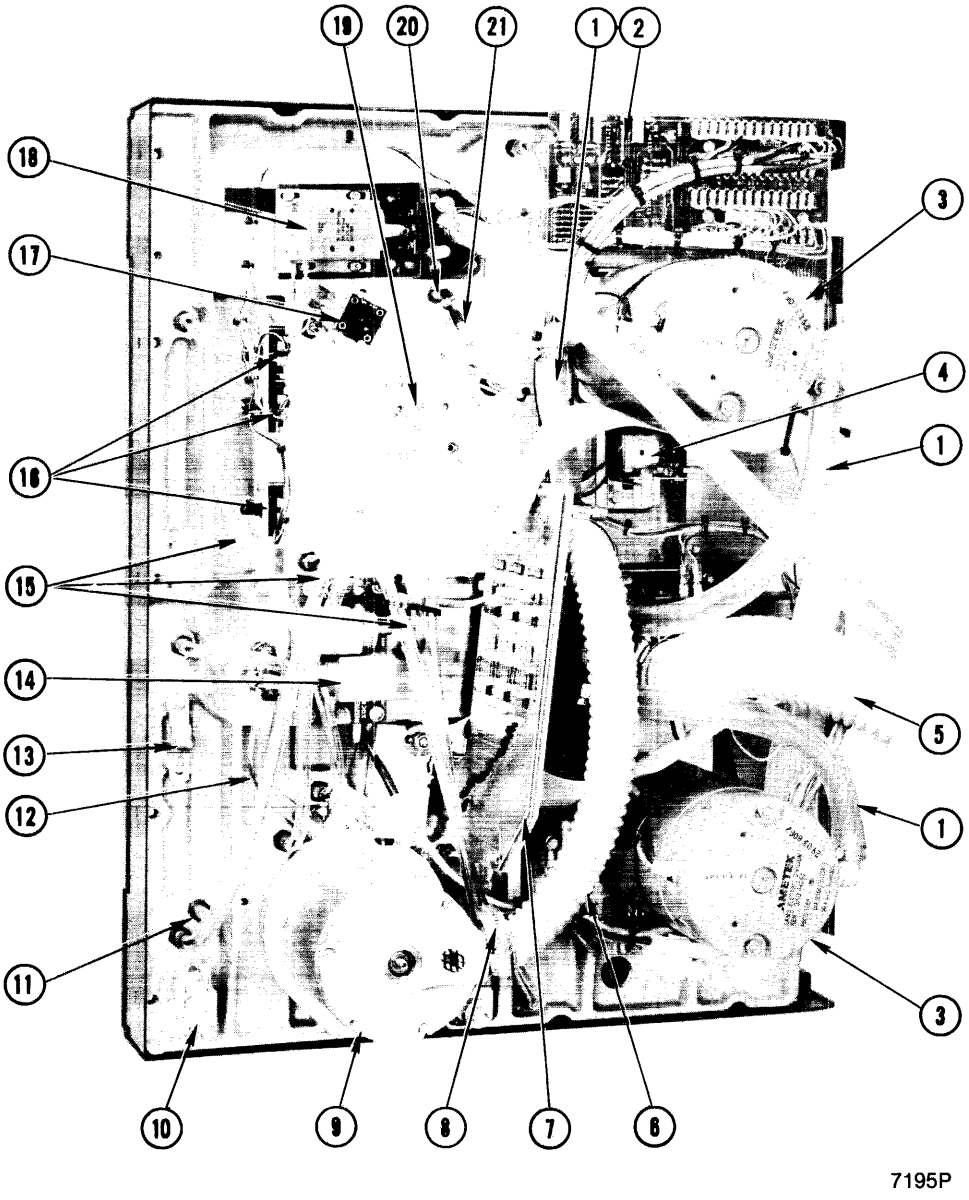

Figure 7-2. T1000 and FT1000 Series Photo Parts Index, Rear View

Table 7-2
T1000 and FT1000 Photo Parts List

Figure and Index No.	Part No.	Description
Figure 7-2		
1	669-0017	Tubing, ½ Inch ID
	615-0196	Adjustable Clamp
2	106936-*	PCBA, Interconnect F1
3	107067-01	Reel Motor Assembly
4	107190-01	Write Protect Assembly
	506-6360	Switch
5	108376-01	Vacuum Hose, 1¾ Inch ID
6	669-0004	Vacuum Hose, 1 Inch ID
7	104816-*	PCBA, 9 Track Preamplifier (T1640, FT1640)
	107871-*	PCBA, 9 Track Preamplifier (T1940)
8	615-0197	Adjustable Clamp
9	107016-01	Capstan Motor Assembly (T1640, FT1640)
	107016-02	Capstan Motor Assembly (T1940)
10	615-4410	Catch
11	109505-01	Air Cap
12	669-0012	Tubing, 3/8 Inch ID
13	104712-01	Leveling Pin
14	107192-*	PCBA, Transducer
15	669-0011	Tubing, 3/16 Inch ID
16	506-0007	Pressure Switch (1 Place)
	506-0023	Pressure Switch (4 Places)
17	506-0008	Pressure Switch
18	107127-01	Pressure Valve Assembly
19	500-0008	Gear Motor
	102245-01	Filter Assembly
20	109506-01	Plunger
Not shown	109542-01	Plunger and Bracket Replacement Kit
21	506-6360	Switch
Not shown	107125-01	Vacuum Valve Assembly
	110144-01	Dual Interlock Switch Kit

*Order as Indicated on PCBA, component side

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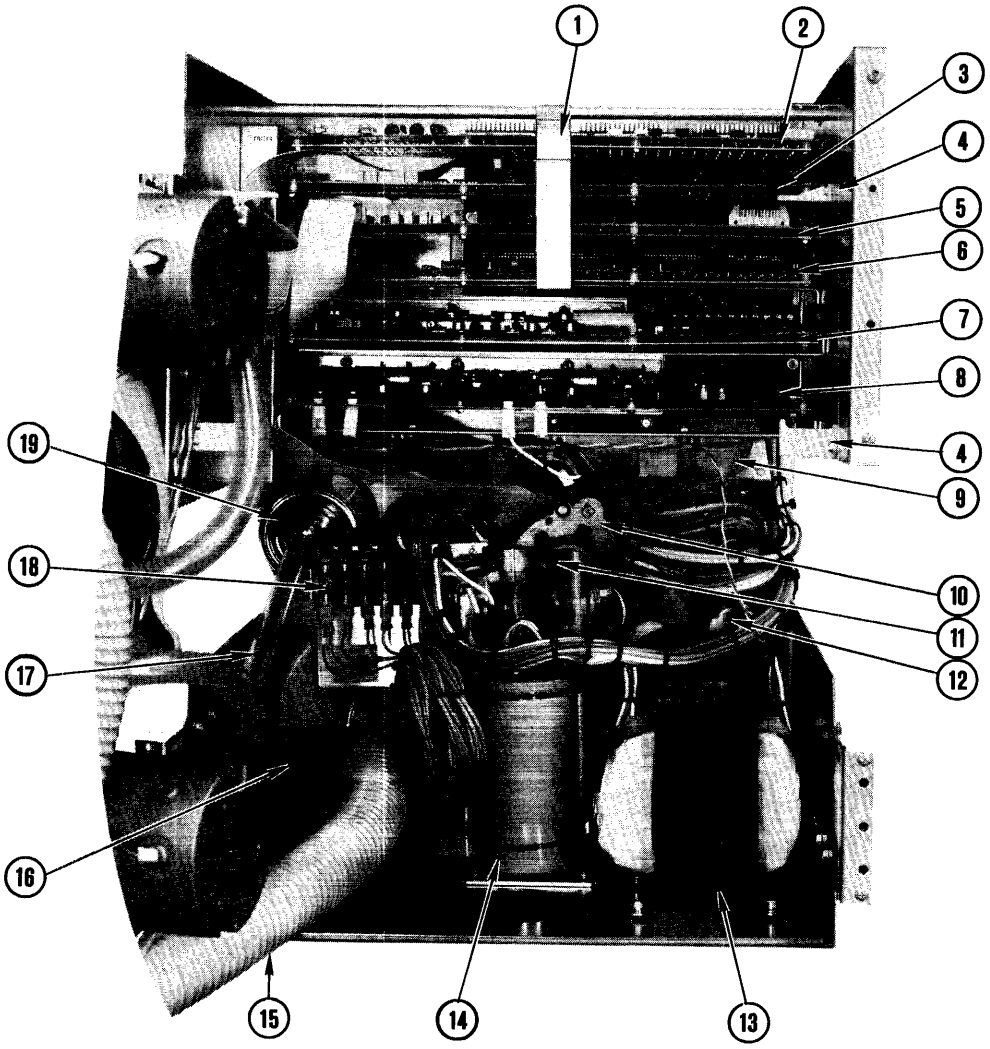

Figure 7-3. T1000 and FT1000 Series Photo Parts Index, Card Cage and Power Supply

Table 7-3
T1000 and FT1000 Photo Parts List

Figure and Index No.	Part No.	Description
Figure 7-3		
1	107156-01	Card Lock (T1640, FT1640)
	107904-01	Card Lock (T1940)
2	107605-*	PCBA, Microformatter (FT1640)
	107886-01	PCBA, MIA (T1940)
3	104806-*	PCBA, Data L (T1640, FT1640)
	107856-*	PCBA, Read (T1940)
4	107124-01	Skyhook
	608-1606	Screw
5	104811-*	PCBA, Write (T1640, FT1640)
	107861-*	PCBA, Write (T1940)
6	106876-*	PCBA, Control M2 (All Models)
7	104758-*	PCBA, Capstan Servo (All Models)
8	106926-*	PCBA, Reel Servo (All Models)
9	107302-01	Cable Assembly
10	518-1000	Compressor
11	107091-01	Running Time Meter, 60 Hz (Optional)
	107091-02	Running Time Meter, 50 Hz (Optional)
12	106819-01	AC Motor Assembly (T1640, FT1640)
	106819-02	AC Motor Assembly (T1940)
13	511-0015	Transformer
14	134-1892	Capacitor, C1, C2
	134-4792	Capacitor, C3
	134-6102	Capacitor, C4, C5
15	108376-01	Vacuum Hose, 1¾ Inch ID
16	518-2000	Blower Assembly w/Pulley (T1640, FT1640)
	518-2001	Blower Assembly w/Pulley (T1940)
17	108377-03	Tube, ½ Inch ID, Air Filter to Valve
18	663-3070	Fuse, F1
	663-3050	Fuse, F2, F3
	663-3200	Fuse, F4, F5, F6, F7
19	614-0007	Air Filter
Not shown	104963-01	PCBA, Self Test (Optional)
	614-0009	Muffler
	107499-01	Fan Assembly, Card Cage (T1940, Some Models)
	652-0003	Card Guide (14 places)
	107298-*	PCBA, Interconnect D1
	109576-01	Cooling and Acoustic Kit (Optional)

*Order as indicated on PCBA, component side

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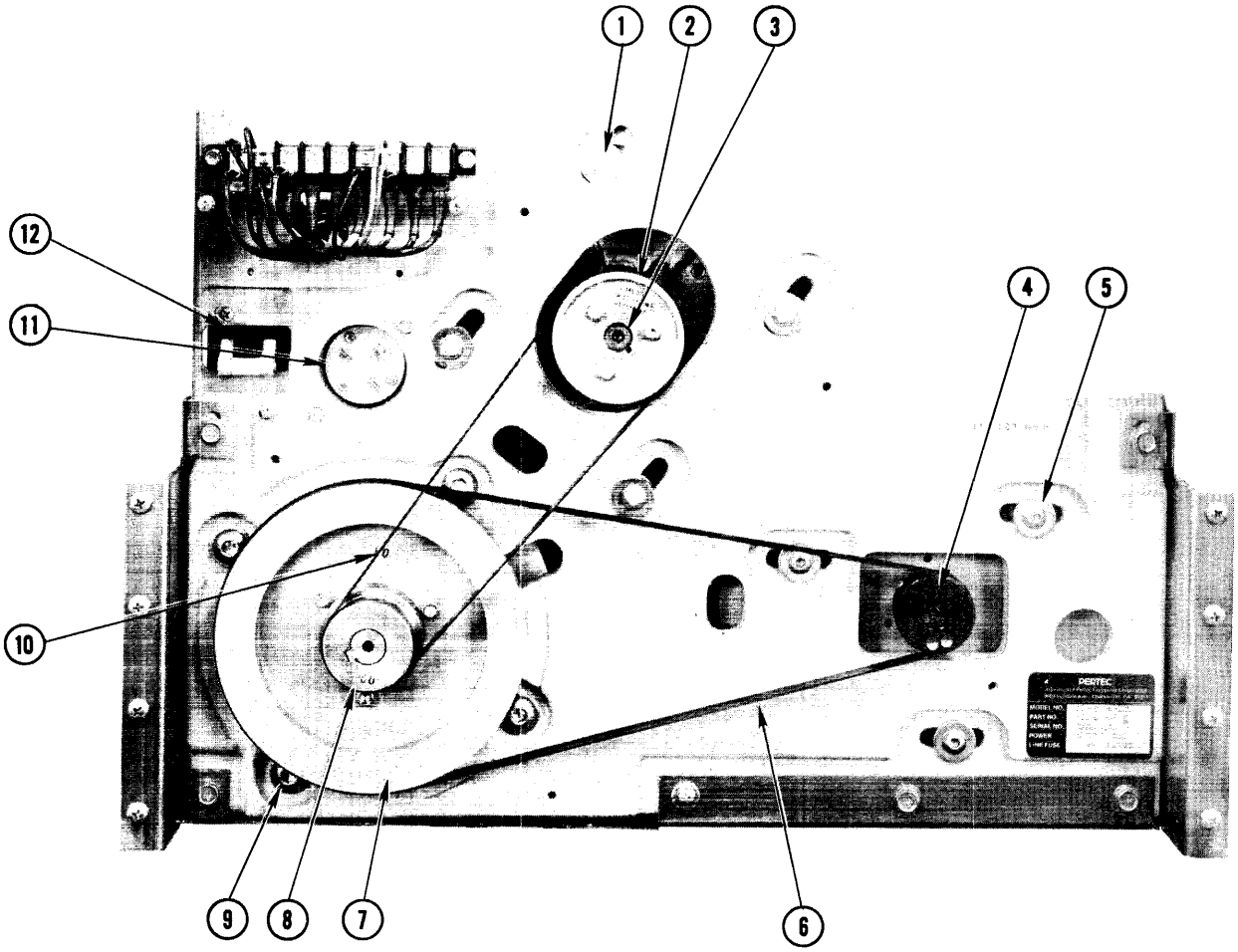

Figure 7-4. T1000 and FT1000 Series Photo Parts Index, Power Supply, Rear View

Table 7-4
T1000 and FT1000 Photo Parts List

Figure and Index No.	Part No.	Description
Figure 7-4		
1	602-2126	Compressor Mounting Screw (4 places)
2	102635-03	Pulley, Compressor (T1640, FT1640)
	102635-04	Pulley, Compressor (T1940)
3	107041-01	Compressor Hub
	603-1404	Setscrew
	609-6208	Woodruff Key
4	—	Pulley (Part of Blower)
5	602-2112	Blower Mounting Screw (3 places)
	612-0053	Flat Washer (3 places)
6	108479-03	Blower Belt, 60 Hz, Low Altitude
	108479-05	Blower Belt, 50 Hz, Low Altitude
	108479-04	Blower Belt, 60 Hz, High Altitude
	108479-06	Blower Belt, 50 Hz, High Altitude
7	108478-01	Motor Pulley, 60 Hz, Low Altitude
	108478-03	Motor Pulley, 50 Hz, Low Altitude
	108478-02	Motor Pulley, 60 Hz, High Altitude
	108478-04	Motor Pulley, 50 Hz, High Altitude
8	107042-01	Motor Hub, 60 Hz
	107042-02	Motor Hub, 50 Hz
	603-2108	Setscrew
	609-6322	Square Key
9	602-2712	Motor Mounting Screw (4 places)
	606-0701	Flat Washer (4 places)
10	108479-01	Compressor Belt (T1640, FT1640)
	108479-02	Compressor Belt (T1940)
11	503-0135	Socket
12	663-0002	Circuit Breaker
Not shown	107055-01	Belt Guard
	107133-01	AC Power Cover
	109528-01	Power Cord, International, 3 Meters (10 feet)
	109528-02	Power Cord, International, 1.5 Meters (5 feet)

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Table 7-5
T1000 and FT1000 Series Recommended Spare Parts List

Description	Part No.
1. PCBA, Data L (T1640, FT1640)	104806-*
2. PCBA, Write (T1640, FT1640) PCBA, Write (T1940)	104811-* 107861-*
3. PCBA, 9 Track Preamplifier (T1640, FT1640) PCBA, 9 Track Preamplifier (T1940)	104816-* 107871-*
4. PCBA, Capstan Servo (All Models)	104758-*
5. PCBA, Reel Servo (All Models)	106926-*
6. PCBA, Interconnect F1 (All Models)	106936-*
7. PCBA, Interconnect D1 (All Models)	107298-*
8. PCBA, Control M2 (All Models)	106876-*
9. PCBA, Microformatter (FT1640)	107605-*
10. PCBA, Read (T1940)	107856-*
11. PCBA, MIA (T1940)	107886-*
12. PCBA, Transducer (All Models)	107192-01
13. Head (T1640, FT1640) Head (T1940)	530-6369 530-6099
14. EOT/BOT Assembly	107012-01
15. TIP Assembly	107013-01
16. Reel Sense Assembly	107236-01
17. Pack Sense Assembly	107239-01
18. Capstan Motor Assembly (T1640, FT1640) Capstan Motor Assembly (T1940)	107016-01 107016-02
19. Reel Motor Assembly	107067-01
20. AC Motor Assembly (T1640, FT1640) AC Motor Assembly (T1940)	106819-01 106819-02
21. Vacuum Valve Assembly	107125-01
22. Pressure Valve Assembly	107127-01
23. Compressor Belt (T1640, FT1640) Compressor Belt (T1940)	108479-01 108479-02
24. Blower Belt, 60 Hz Blower Belt, 50 Hz	108479-03 108479-05
25. Friction and Expansion Ring Kit	109502-01
26. Solid State Relay, S2	410-0001
27. Solid State Relay, S3	410-0004
28. Pressure Switch	506-0007
29. Pressure Switch	506-0008
30. Switch	506-6360
31. Air Filter	614-0007
32. Pressure Switch	506-0023

*Order as indicated on PCBA, component side

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Table 7-6
T1000/FT1000 Series
Part Number Cross Reference

Manufacturer Part No./Description	Manufacturer	Pertec Part No.
Resistors, Carbon Film, Carbon Composition	(Comply with MIL-R-11)	
.005 ohms ±5%, ¼w		100-0005
4.7 ohms ±5%, ¼w		100-0475
10 ohms ±5%, ¼w		100-1005
10 ohms ±5%, ½w		101-1005
18 ohms ±5%, 2w		103-1805
22 ohms ±5%, ¼w		100-2205
22 ohms ±5%, 2w		103-2205
33 ohms ±5%, ¼w		100-3305
39 ohms ±5%, ½w		100-3905
47 ohms ±5%, ¼w		100-4705
47 ohms ±5%, ½w		101-4705
56 ohms ±5%, ¼w		100-5605
75 ohms ±5%, ½w		101-7505
82 ohms ±5%, ½w		101-8205
100 ohms ±5%, ¼w		100-1015
100 ohms ±5%, ½w		101-1015
100 ohms ±5%, 2w		103-1015
120 ohms ±5%, ¼w		100-1215
120 ohms ±5%, ½w		101-1215
150 ohms ±5%, ¼w		100-1515
150 ohms ±5%, 2w		103-1515
180 ohms ±5%, ¼w		100-1815
220 ohms ±5%, ¼w		100-2215
330 ohms ±5%, ¼w		100-3315
330 ohms ±5%, ½w		101-3315
470 ohms ±5%, ¼w		100-4715
470 ohms ±5%, 1w		102-4715
470 ohms ±5%, 2w		103-4715
560 ohms ±5%, ¼w		100-5615
560 ohms ±5%, ½w		101-5615
680 ohms ±5%, ¼w		100-6815
820 ohms ±5%, 1w		102-8215
1k ohms ±5%, ¼w		100-1025
1k ohms ±5%, ½w		101-1025
1k ohms ±5%, 2w		103-1025
1.2k ohms ±5%, ¼w		100-1225
1.5k ohms ±5%, ¼w		100-1525
1.8k ohms ±5%, ¼w		100-1825
2.2k ohms ±5%, ¼w		100-2225
2.7k ohms ±5%, ¼w		100-2725
3.3k ohms ±5%, ¼w		100-3325
3.9k ohms ±5%, ¼w		100-3925
4.7k ohms ±5%, ¼w		100-4725
5.6k ohms ±5%, ¼w		100-5625
5.6k ohms ±5%, 1w		102-5625
10k ohms ±5%, ¼w		100-1035
15k ohms ±5%, ¼w		100-1535
18k ohms ±5%, ¼w		100-1835
22k ohms ±5%, ¼w		100-2235
27k ohms ±5%, ¼w		100-2735
33k ohms ±5%, ¼w		100-3335
39k ohms ±5%, ¼w		100-3935
47k ohms ±5%, ¼w		100-4735
100k ohms ±5%, ¼w		100-1045
120k ohms ±5%, ¼w		100-1245
180k ohms ±5%, ¼w		100-1845
220k ohms ±5%, ¼w		100-2245
470k ohms ±5%, ¼w		100-4745
560k ohms ±5%, ¼w		100-5645
1.0m ohms ±5%, ¼w		100-1055
4.3m ohms ±5%, ¼w		100-4355

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Table 7-6

T1000/FT1000 Series
Part Number Cross Reference (Continued)

Manufacturer Part No./Description	Manufacturer	Pertec Part No.
Resistors, Metal Film		
10 ohms ±1%, 1/8w		107-0100
19.6 ohms ±1%, 1/8w		107-0196
34.8 ohms ±1%, 1/8w		107-0348
51.1 ohms ±1%, 1/8w		107-0511
82.5 ohms ±1%, 1/8w		107-0825
100 ohms ±1%, 1/8w		107-1000
133 ohms ±1%, 1/8w		107-1330
162 ohms ±1%, 1/8w		107-1620
178 ohms ±1%, 1/8w		107-1780
261 ohms ±1%, ¼w		104-2610
287 ohms ±1%, 1/8w		107-2870
383 ohms ±1%, 1/8w		107-3830
511 ohms ±1%, 1/8w		107-5110
562 ohms ±1%, 1/8w		107-5620
619 ohms ±1%, 1/8w		107-6190
681 ohms ±1%, 1/8w		107-6810
825 ohms ±1%, 1/8w		107-8250
909 ohms ±1%, 1/8w		107-9090
1k ohms ±1%, 1/8w		107-1001
1.1k ohms ±1%, 1/8w		107-1101
1.21k ohms ±1%, 1/8w		107-1211
1.33k ohms ±1%, 1/8w		107-1331
1.47k ohms ±1%, ¼w		104-1471
1.62k ohms ±1%, 1/8w		107-1621
1.96k ohms ±1%, 1/8w		107-1961
2.15k ohms ±1%, 1/8w		107-2151
2.37k ohms ±1%, 1/8w		107-2371
2.61k ohms ±1%, 1/8w		107-2611
3.16k ohms ±1%, 1/8w		107-3161
3.83k ohms ±1%, 1/8w		107-3831
4.64k ohms ±1%, 1/8w		107-4641
5.11k ohms ±1%, 1/8w		107-5111
6.81k ohms ±1%, 1/8w		107-6811
7.5k ohms ±1%, 1/8w		107-7501
8.25k ohms ±1%, 1/8w		107-8251
9.09k ohms ±1%, 1/8w		107-9091
10k ohms ±1%, 1/8w		107-1002
12.1k ohms ±1%, 1/8w		107-1212
14.7k ohms ±1%, 1/8w		107-1472
16.2k ohms ±1%, 1/8w		107-1622
21.5k ohms ±1%, 1/8w		107-2152
26.1k ohms ±1%, 1/8w		107-2612
28.7k ohms ±1%, 1/8w		107-2872
38.3k ohms ±1%, 1/8w		107-3832
46.4k ohms ±1%, 1/8w		107-4642
51.1k ohms ±1%, 1/8w		107-5112
56.2k ohms ±1%, 1/8w		107-5622
68.1k ohms ±1%, 1/8w		107-6812
100k ohms ±1%, 1/8w		107-1003
133k ohms ±1%, 1/8w		107-1333
162k ohms ±1%, 1/8w		107-1623
383k ohms ±1%, 1/8w		107-3833
464k ohms ±1%, 1/8w		107-4643
750k ohms ±1%, 1/8w		107-7503
825k ohms ±1%, 1/8w		107-8253
Resistors, Wirewound		
0.03 ohms ±1%, 4w		115-0004
0.03 ohms ±5%, 4w		115-0003
0.03 ohms ±3%, 10w		110-0003
0.05 ohms ±3%, 20w		111-0001
0.10 ohms ±3%, 10w		110-0011

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Table 7-6

T1000/FT1000 Series
Part Number Cross Reference (Continued)

Manufacturer Part No./Description	Manufacturer	Pertec Part No.
Resistors, Wirewound (Continued)		
0.15 ohms ±3%, 10w		118-0013
0.3 ohms ±3%, 10w		118-0033
0.5 ohms ±10%, 5w		109-0500
27 ohms ±10%, 5w		109-2705
270 ohms ±5%, 5w		109-2715
470 ohms ±5%, 3w		108-4715
820 ohms ±5%, 5w		109-8215
Variable Resistors, 15 Turn		
100 ohms ±10%, ¾w, 79PR100	Beckman	121-1010
500 ohms ±10%, ¾w, 79PR500	Beckman	121-5010
1k ohms ±10%, ¾w, 79PR1K	Beckman	121-1020
10k ohms ±10%, ¾w, 79PR10K	Beckman	121-1030
200k ohms ±10%, ¾w, 79PR200K	Beckman	121-2041
500k ohms ±10%, ¾w, 79PR500K	Beckman	121-5040
Variable Resistors, 1 Turn, Top Adj		
1k ohms, ±20%, ½w, 3329P-1-102	Bourns	123-1020
Variable Resistors, 20 Turn, Side Adj		
1k ohms ±10%, ½w, 68X-1K	Beckman	126-1021
50k ohms ±10%, ½w, 68X-50K	Beckman	126-5031
Dipped Mica Capacitors	(Comply with MIL-C-5)	
10 pf ±5%, 500wvdc		130-1005
22 pf ±5%, 500wvdc		130-2205
33 pf ±5%, 500wvdc		130-3305
47 pf ±5%, 500wvdc		130-4705
56 pf ±5%, 500wvdc		130-5605
68 pf ±5%, 500wvdc		130-6805
100 pf ±5%, 500wvdc		130-1015
150 pf ±5%, 500wvdc		130-1515
220 pf ±5%, 500wvdc		130-2215
270 pf ±5%, 500wvdc		130-2715
330 pf ±5%, 500wvdc		130-3315
560 pf ±5%, 300wvdc		130-5615
750 pf ±5%, 300wvdc		130-7515
Film Capacitors		
0.0015 μfd ±10%, 100wvdc, 630 series	TRW	131-1520
0.0022 μfd ±10%, 100wvdc, 630 series	TRW	131-2220
0.0033 μfd ±10%, 100wvdc, 630 series	TRW	131-3320
0.0047 μfd ±10%, 100wvdc, 630 series	TRW	131-4720
0.022 μfd ±10%, 100wvdc, Type PT-485	Paktron	131-2230
0.033 μfd ±10%, 100wvdc, 630 series	TRW	131-3330
0.068 μfd ±10%, 100wvdc, Type PT-605	Paktron	131-6830
0.47 μfd ±10%, 100wvdc, X600-.47-10%-100v	TRW	131-4741
20.0 μfd ±10%, 100wvdc, 650BIB206K	Electrocube	131-2060
Film Capacitor, Polycarbonate		
0.022 μfd ±5%, 50wvdc, Type WCR	Cornell-Dublier	136-2230
Ceramic Capacitors		
2200 pf, ±10%, 50wvdc, C40C222K2	Centralab	135-2220
0.001 μfd ±20%, 1000wvdc, DD-102	Centralab	135-1002
0.005 μfd ±20%, 600wvdc, 2DDH69N502MAA	Centralab	135-5070
0.01 μfd ±10%, 100wvdc, C41A103K	Centralab	135-1031
0.01 μfd ±20%, 100wvdc, MD011C103MAA	AVX	135-1032
0.02 μfd +80% −20%, 600wvdc, 200H63L203ZAG	Centralab	135-2062
0.15 μfd ±10%, 50wvdc, CW30C154K245	Centralab	135-1541
0.22 μfd ±20%, 50wvdc, CZ30C224M245	Centralab	135-2241
0.22 μfd +80% −20%, 50wvdc, MD015E224ZAA	AVX	135-2242
0.47 μfd ±20%, 100wvdc, SR301E474MAA	AVX	135-4742

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Table 7-6

T1000/FT1000 Series
Part Number Cross Reference (Continued)

Manufacturer Part No./Description	Manufacturer	Pertec Part No.
Solid Tantalum Capacitors		
0.10 µfd ±5%, 20wvdc, T310A104J020AS	Kemet	139-1020
0.47 µfd ±10%, 35wvdc, T310A474K035AS	Kemet	139-4755
2.2 µfd ±20%, 20wvdc, T310A225M020AS	Kemet	139-2244
3.3 µfd ±20%, 15wvdc, T310A335M015AS	Kemet	139-3352
6.8 µfd ±10%, 35wvdc, T310B685K035AS	Kemet	139-6845
22 µfd ±20%, 15wvdc, T310B226M015AS	Kemet	139-2262
33 µfd ±10%, 10wvdc, T310B336K010AS	Kemet	139-3302
47 µfd ±20%, 6wvdc, T310B476M006AS	Kemet	139-4762
Aluminum Electroletic Capacitors		
50 µfd +75% −10%, 50wvdc, 30D506GO50DDS	Sprague	142-5060
100 µfd +75% −10%, 30wvdc, TT101V030C0R6P	Mallory	142-1070
130 µfd +75% −10%, 100wvdc, QLA13IT100J1L6P	Mallory	142-1370
Transistors		
TIP32B, PNP, TO-218AA	Texas Instruments	200-3200
TIP41C, NPN, TO-220AB	Texas Instruments	200-0041
TIP42C, PNP, TO-220AB	Texas Instruments	200-0042
2N2905A, PNP, TO-5	Texas Instruments	200-2905
2N3055, Selected, NPN, TO-3	Solitron	200-0004
2N3251, PNP, TO-18	National	200-3251
2N4037, PNP, TO-5	RCA	200-4037
2N4123, NPN, TO-92	Motorola	200-4123
2N4125, PNP, TO-92	Motorola	200-4125
2N4348, NPN, TO-3	Motorola	200-4348
2N5321, NPN, TO-5	National	200-5321
2N5323, PNP, TO-5	RCA	200-5323
2N6058, NPN, Power Darlington, TO-3	Motorola	200-6058
2N6306, NPN, TO-3	Motorola	200-6306
Silicon Controlled Rectifier		
2N3668, 12.5A, 100v, TO-3	RCA	201-3669
2N6394, 12A, 50v, TO-220AB	Motorola	201-0126
Field Effect Transistors		
2N4860, N-Channel, Switching, 0.1A, 30v, TO-92	Motorola	204-0074
Diodes		
1N3890, Rectifier, 12A, 100v, DO-4	Motorola	300-8810
1N4002, Rectifier, 1A, 100vdc, DO-41	Motorola	300-4002
1N4446, Switching, 75PIV, DO-35	Texas Instruments	300-4446
Light Emitting Diode		
Red, Gallium Arsenide Phosphide, CM4-83-2	General Inst.	301-0002
Zener Diodes		
1N4728A, 3.3vdc, ±5% @76MA I_Z, 1w, DO-41	ITT	330-0335
1N4732A, 4.7vdc, ±5% @53MA I_Z, 1w, DO-41	Texas Instruments	330-0475
1N4733A, 5.1vdc, ±5% @49MA I_Z, 1w, DO-41	Texas Instruments	330-0515
1N4734A, 5.6vdc, ±5% @45MA I_Z, 1w, DO-41	Texas Instruments	330-0565
1N4736A, 6.8vdc, ±5% @37MA I_Z, 1w, DO-41	Texas Instruments	330-0685
1N4740A, 10vdc, ±5% @25MA I_Z, 1w, DO-41	ITT	330-1005
1N4742A, 12vdc, ±5% @21MA I_Z, 1w, DO-41	Texas Instruments	330-1205
1N5228B, 3.9vdc, ±5% @20MA I_Z, 1w, DO-7	Motorola	331-0395
1N5231B, 5.1vdc, ±5% @20MA I_Z, 1w, DO-7	Motorola	331-0515
1N5233B, 6.0vdc, ±5% @20MA I_Z, 1w, DO-7	Motorola	331-0605
1N5249B, 19vdc, ±5% @6.6MA I_Z, 1w, DO-7	Motorola	331-1905

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Table 7-6

T1000/FT1000 Series
Part Number Cross Reference (Continued)

Manufacturer Part No./Description	Manufacturer	Pertec Part No.
Operational Amplifiers		
LM305AH, Voltage Regulator, +4.5v to +40v	National	400-0305
LM307N, Op Amp, Single, Temperature Compensated	National	400-0307
LM311N, Voltage Comp., Med. Speed	National	400-0311
LM318N, Op Amp, Single, High Speed	National	400-0318
LM319N, Voltage Comp., Dual, HI Speed	National	400-0319
LM325N, Voltage Reg., Fixed ±15v, Dual Tkg.	National	400-0325
LM555CN, Timer, Single, Astable or Monostable	National	400-0555
LM741CN, Op Amp, Single	National	400-2741
LM1458N, Op Amp, Dual	National	400-5558
MC3467, Preamp, Three Unit	National	400-3467
MC7805CT, Volt Reg., +5vdc, 1A	Motorola	400-7805
MC7906CT, Volt Reg., −6vdc, 1A	Motorola	400-7906
NE592A, Video Amp., Wideband, Differential Output	Signetics	400-0592
Oscillator Assembly		
K1115A, 2.2605MHz, XTAL ±0.1%	Motorola	402-2262
Analog Switch		
AH5012CN, 4 Channel, RDS/ON/150 ohms or less	National	403-0002
Inductor		
1537-76, 100 μh ±5%, @ 2.5 MHz	Delevan	515-1015
5219, 4.9 μh ±20%, 12A, 0.018 ohm max	J.W. Miller	515-0005

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APPENDIX A
GLOSSARY

GENERAL NOTES

1. I, prefixed to a mnemonic term, designates an interface I/O signal. If the term contains a suffix R (for Receiver), the signal is an Input (with reference to the T1000 Tape Transport). Similarly, a suffix D (for Driver) implies an Output signal. Low = true for all I/O signals.

   NOTE

   Care should be exercised to avoid confusing specialized uses of I, R, and D, such as I for Inverted *in NRZI, R for* Read, *and D for* Data.

2. N, prefixed to a mnemonic term has a meaning similar to a logic bar or not symbol. N implies that the true signal identified by the remainder of the term is electronically low (low = true) at the critical point in the circuit identified by the term.

3. Status signals are true if the condition monitored is true; e.g., LOAD FAULT is true if the tape is improperly loaded.

4. Mnemonics for signals derived from circuits controlled by switches (automatic as well as manual) may include N.O. (normally open) or N.C. (normally closed).

5. D is prefixed to a term to mean that the signal has been delayed with reference to the signal identified by the remainder of the term.

Mnemonic	Logic Term Name
ABP	Compressed Air Applied
ACRC	Auxiliary Cyclic Redundancy Check
AGC	Automatic Gain Control
AMNABL	Amplitude Enable
AMTIE	Amplitude Track in Error
ANSI	American National Standards Institute
ATACH	Analog Tachometer Signal
BCD	Binary Coded Decimal
BCO	Binary Coded Octal
BIN	Binary
BKW	Backwrap
BOP	Beginning of Preamble
BOT	Beginning of Tape
BOT INT	Beginning of Tape Interlock
BPI	Bits per Inch
BWC	Bandwidth Control
CAS	Common Addressable Space
C0—4	Load/Unload Sequence Count 0 through 4 (High = True)
CC N.O.	Cartridge Closed (Low = True)
CENBL	Capstan Enable
CLKA	Clock A (1 MHz)
CLKB	Clock B (100 KHz)
CLKC	Clock C (10 KHz)
CLKD	Not Used
CLKE	Clock E (10 Hz)
CLKF	Clock F (1 Hz)
CLKG	Clock G (0.5 Hz)
CM	Capstan Motor
CO N.O.	Cartridge Open (Low = True)
CPI	Characters per Inch
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CRCC	Cyclic Redundancy Check Character
CRNO	Crippled Reel Normally Open (Low = True)
CSD	Control/Status/Data
DDI	Data Density Indicator Signal
DINT	Data Interrupt
DINTLK	Delayed Interlock Pulse
DIR	Direction of Capstan Motion
DONL	Delayed On-Line Signal
DVR	Driver Output of Capstan Summing Amplifier
ECC	Error Correction Code
ECCC	Error Correction Code Character
EDN	Erase Drive Current
ENBL	Enable
EOT	End of Tape
ERHDLO	Erase Head Low
ETM	Elapsed Time Meter
EXSNS	Extended Sense
FEN	Formatter Enable
FIFO	First-In, First-Out
FMTR	Formatter
FPT	File Protected (High = True)
F/V	Frequency-to-Voltage Converter
FWD	Forward Tape Motion
GCR	Group-Coded Recording
HI DEN	High Density
I	I/O (see Note 1)
IAMTIE	Amplitude Track in Error (Low = True)
IARA	Automatic Read Amplifier (Low = True)

Mnemonic	Logic Term Name
IBG	Inter-Block Gap
IBOT	Beginning of Tape Interface Output (Low = True)
ICMD	Command Line (Low = True)
ICMDPER	Command Parity Error (Low = True)
ICSD	Control/Status/Data (Low = True)
ICSDP	Control/Status/Data Parity (Low = True)
IDDI	Data Density Indicator Signal Output (Low = True)
IDDS	Data Density Select Input
IDINT	Data Transfer Interrupt (Low = True)
IEOT	End of Tape Output Signal (Low = True
IFEN	Formatter Enable (Low = True)
IFPT	File Protect Signal at Interface (Low = True)
IGCR	Group-Coded Recording (Low = True)
ILDP	Load Point (Low = True when tape is at load point)
ILTH	Low Threshold (Low = True)
IMINT	Motion Interrupt (Low = True)
IMOTION	Tape in Motion (Low = True)
INRZ	NRZI Interface Command (Low = True for NRZI select)
INTLK	Interlock
INTLKP1	Pulsed Interlock (occurs after INTLK, before DINTLK)
IOL	On Line Signal at Interface (Low = True)
IONL	On-Line Mode (Low = True)
IPSEN	Power Sense (Low = True)
IRD0—IRD7	Read Data Bit 0 through 7 Output, respectively Interface signal (Low = True)
IRDP	Read Data Parity Output. Interface Signal (Low = True)
IRDS	Read Data Strobe. Interface Signal (Low = True)
IRDY	Tape Transport Read Output. Interface Signal (Low = True)
IRG	Inter-Record Gap
IRTH1	Read Threshold Level 1 (High) Threshold Input. Interface Signal (Low = True)
IRTH2	Read Threshold Level 2 (Low) Threshold Input. Interface Signal (Low = True)
IRWC	Rewind Command Input. Interface Signal (Low = True)
IRWD	Rewinding Signal Output. Interface Signal (Low = True)
IRWU	Rewind and Unload Command Input. Interface Signal (Low = True)
ISDTH	Standard Threshold (Low = True)
ISFC	Synchronous Forward Command Input. Commands tape forward motion for either reading or writing (Low = True)
ISGL	Single (not used)
ISLT0	Select Transport No. 0 Input. Interface Signal (Low = True)
ISLT1	Select Transport No. 1 Input. Interface Signal (Low = True)
ISLT2	Select Transport No. 2 Input. Interface Signal (Low = True)
ISLT3	Select Transport No. 3 Input. Interface Signal (Low = True)
ISPEED	Speed Selection Input (not used)
ISRC	Synchronous Reverse Command Input. Commands tape motion in reverse at reading and writing speed
ISTAT	Status Line (Low = True)
ISWS	Set Write Status. Interface Signal (Low = True)
ITACH	Tachometer Output. Interface Signal (Low = True)
ITACK	Transfer Acknowledge (Low = True)
ITREQ	Transfer Request (Low = True)
ITWRT	Transfer Write (Low = True)
IWARS	Write Amplifier Reset Strobe. Interface Signal (Low = True)

Mnemonic	Logic Term Name
IWD0—IWD7	Write Data Bit 0 through 7, respectively. Interface Signal (Low = True)
IWDP	Write Data Parity. Interface Signal (Low = True)
IWDS	Write Data Strobe. Interface Signal (Low = True)
IWINH	Write Inhibit Signal (Low = True)
IWRT BIN	Write Binary (Low = True)
IWRT STAT	Write Status (Low = True)
I7TK	Seven Track Interface Signal (not used)
I9TK	Nine Track Interface Signal (Low = True)
LDFO	Load Fault Zero
LDS	Load Status
LD/REW	Load/Rewind
LEOT	Logical End of Tape
LO DENSITY	Low Density (for PE mode)
LOAD FAULT	Load Fault Warning Signal
LRCC	Longitudinal Redundancy Check Character
LWR	Loop Write to Read
MIA	Multiplexer Interface Adapter
MINT	Motion Interrupt
MOT	Motion
MRL	Mid Reel Load
MTC	Magnetic Tape Command
MTS	Magnetic Tape Status
MUX	Multiplexer
N<80%	Capstan speed is greater than 80% (Low = True)
NAE	Amplifier Enable (Low = True)
NAMTIE	Amplitude Track In Error (Low = True)
NAOK	Air OK (Low = True)
NBOT	Beginning of Tape (Low = True)
NC0—4	Load/Unload Sequence count 0 through 4 (Low = True)
NCCC	Cartridge Closed Command (Low = True)
NCOC	Cartridge Open Command (Low = True)
NDINTLK	Delayed Interlock Signal (Low = True)
NDRV	Capstan Drive (Low = True)
NEDT	End of Tape Sensed (Low = True)
NEOT	End of Tape (Low = True)
NGC	Group Coded (Low = True)
NGCR	Group Coded Recording (Low = True)
NGOP	Go Pulse (Low = True)
NHID	High Density Signal (High = PE; Low = NRZI)
NHIDI	High Density Signal Inverted (Disables NRZI Gain Circuits) (Low = True)
NINTLK	Interlock (Low = True)
NLDC	Load Clock (Low = True)
NLDFS	Load Fault Status (Low = True)
NLDP	Load Pulse (Low = True)
NLDS	Load Status (Low = True)
NLO	Load and On-Line (Low = True)
NLOIP	Loss of Interlock Pulse (Low = True)
NLRST	Load Reset (Low = True)
NLTH	Low Threshold (Low = True)
NLTP	Low Tape Pulse (Low = True)
NMOT	Motion (Low = True)
NMRL	Mid Reel Load (Low = True)
NMRSTP	Master Reset Pulse (Low = True)
NOC	Overcurrent Sensor (Low = True)
NONL	On-Line (Low = True)
NO OP	No Operation
NPE	Phase Encoded (Low = True)
NPOL	Pressure On Line (Low = True)

Mnemonic	Logic Term Name
NPORST	Power Reset. Reset signal generated when power is turned ON (Low = True)
NREWP	Rewind Pulse (Low = True)
NRSAE	Reel Servo Amplifier Enable (Low = True)
NRST1	Reset 1 (Low = True)
NRTY	Retry (Repeat load attempt) (Low = True)
NRWC	Rewind Command (Low = True)
NRWR	Rewind Ramp (Low = True)
NRWS	Rewind Status (Low = True)
NRZEN	NRZI Enable
NRZ	Non-Return to Zero
NRZI	Non-Return to Zero, Inverted
NRZIT	NRZI Threshold Enable
NSEL	Select (Low = True)
NSFC	Synchronous Forward Command to move tape in forward direction at reading and writing speed (Low = True)
NSINTLK	Supply Reel Interlock (Low = True)
NSLTA	Transport Select Signal (Low = True)
NSMR	Small Reel Sense Signal (Low = True)
NSRC	Synchronous Reverse Command for reverse motion at reading and writing speed (Low = True)
NSTART	Capstan Start Command (Low = True)
NTAP2	Tach Pulse 2 (squared and set at 20 μsec pulses) (Low = Tach mark sensed true)
NTEN	Tach Enable (Low = True)
NTEST	Test Signal (Low = True)
NTESTA	Test Signal to select transport (Low = True)
NTINTLK	Takeup Reel Interlock (Low = True)
NTIP	Tape In Path (Low = True)
NTRWC	Test Rewind Command (Low = True)
NTSFC	Test Synchronous Forward Command to move tape forward at reading and writing speed (Low = True)
NTSRC	Test Synchronous Reverse Command to move tape in reverse at reading and writing speed (Low = True)
NTSKEW	Test Skew Signal (Low = True)
NTSTR	Test Write Strobe (Low = True)
NTWRC	Test Write Command (Low = True)
NTWRT	Test Write (Low = True)
NULC	Unload Command (Low = True)
NULRW	Rewind and Unload Command (Low = True)
NUNL	Unload (Low = True)
NUNLC	Unload Command (Low = True)
NUNLC1	Unload Command 1 (Low = True)
NUNLC2	Unload Command 2 (Low = True)
NUNL1	Unload Status 1 (Low = True)
NWCTP	Write Current Toggle Pulse (Low = True)
NWCT0—NWCT7	Write Cuttent Toggle Bit 0 through 7, respectively (Low = True)
NWLFB	Write Lockout Signal Feedback
NWRT	Write Signal (Low = True)
NWSPE	Write Strobe Phase Encoded (Low = True)
NW/TDS	Write and/or Test Data Strobe (Low = True)
NXFR	Energize Vacuum Transfer Solenoid (Low = True)
ONL	On Line
PE	Phase Encoded
PET	Phase Encoded Threshold
PETL	Phase Encoded Threshold Set at Low Level
PKSN	Pack Sense
PLE	Pressure Line Enable
PLO	Phase-Lock Oscillator
PNU	Pneumatic (Blower System ON) Command

Mnemonic	Logic Term Name
PNU RETURN	Pneumatic System Return Signal
PO	Pointer
POP	Parity Pointer
PRERR	Preamble Error
PSOL	Pressure Solenoid Command
RCH	Read Channel
RD0—RD7	Read Data Bit 0 through 7, respectively (High = True)
RDP	Read Data Parity Bit (also used as feedback to Read Character Generator and to produce RDS)
RDS	Read Data Strobe
RDY	Ready
REV	Capstan Reverse
REW	Rewind
REWGEN	Rewind Generator
REWR	Rewind Ramp
RH0—RH7	Read Head Output Bit 0 through 7, respectively
RH0A—RH7A	Read Head Output Amplified (after Dual Gain Amplifier) for bits 0 through 7, respectively
RHP	Read Head Output for Parity Bit (to Preamplifier)
RHPA	Read Head Output for Parity Bit Amplified (after Dual Gain Amplifier)
RIEN	Read Interface Enable
RPM	Read Path Microcontroller
RST	Reset
RWD	Rewind
RWS	Rewinding Status
RZ	Return to Zero
SCSH	Supply Crossover High
SCSL	Supply Crossover Low
SER	Suppress Error Repositioning or Retry
SFBRK	Supply Reel Forward Brake
SLIMIT	Supply Tape — Loop Limit
SLTA	Transport Selected by Controller
SLT0—3	Select Lines 0—3
SM	Supply Reel Motor
SPOS	Supply (Loop) Position
SRBRK	Supply Reel Reverse Brake
SRF	Supply Reel Forward
SRO	Selected, Ready and On Line Signal
SRR	Supply Reel Reverse
ST1CLOX	Set 1 Clocks
STL	Set Tape Loop Command
STTHD	Standard Threshold
SUNL	Supply Reel Unload
TACH	Tachometer
TACHP	Tachometer Output Pulse to Interface
TAP1	Tach Pulses No. 1 (squared)
TAP2	Tach Pulses No. 2 (squared and set at 20 μsec each)
TAPEN	Tachometer Pulse Enable
TERM	Terminal
TFBRK	Takeup Reel Forward Brake
THD	Thread
TIP	Tape In Path
TLIMIT	Takeup Tape-Loop Limit
TM	Takeup Reel Motor
TOR	Tape On Reel
TPOS	Takeup (Loop) Position
TR	Takeup Reel
TRACK	Transfer Acknowledge
TRBRK	Takeup Reel Reverse Brake
TREQ	Transfer Request
TRF	Takeup Reel Forward
TRR	Takeup Reel Reverse
TSKEW	Test Skew
TSTDAT	Test Data
TSW	Temperature Switch
TUP	Tape Unit Port
TUS	Tape Unit Sense
UNL	Unload
VAC	Vacuum Applied
VEL OK	Tape Velocity OK
VFC	Variable Frequency Check
VLE	Vacuum Line Enable
VPED	Voltage Pedestal
VRC	Vertical Redundancy Check
VSTEP	Voltage Step
VWRT	Voltage Write
WC0—WC7	Write Current Bit 0 through 7, respectively
WCCG	Write Current Control Gain Signal
WCCR	Write Current Control Ramp
WCP	Write Current Parity Bit
WCS	Write Current Strobe, Write Command Status
WCT0—WCT7	Write Control Toggle Bit 0 through 7, respectively
WCTP	Write Current Toggle Parity Bit
WE	Write Enable
WFAIL	Write Fail
WHD	Write High Density
WLO	Write Lockout
WMC	Write Microcontroller
WP	Write Power
WPINO	Write Protect Solenoid Set
WP SOL	Write Protect Solenoid
WRT	Write Signal
WRT BIN	Write Binary
WRT PWR	Write Power
WRT STAT	Write Status
W/TD0—W/TD7	Write/Test Data Bit 0 through 7, respectively
W/TDP	Write/Test Data Parity Bit
W/TDS	Write/Test Data Strobe
WTE	Write Toggle Enable
XMC	Translator Master Controller
7TK	Seven Track (not used)
9TK	Nine Track

SECTION I
GENERAL DESCRIPTION

1.1 INTRODUCTION

This section provides a general physical and functional description of the Multiplexer Interface Adapter (MIA1) manufactured by Pertec®, Chatsworth, California.

1.2 PURPOSE OF MIA1

The purpose of MIA1 is to translate signals between the T1940-96 GCR/PE Tape Transport and the separate F6250 Formatter, which also converses with a host system controller. The Write/Command/Status (WCS) lines, in one of the two cables between MIA1 and the formatter, are bidirectional and carry time-multiplexed signals: write data bits from the formatter, tape transport control commands from the formatter, and status signals to the formatter. MIA1 handles the routing, demultiplexing and/or multiplexing of these signals, as well as the routing of the other Input/Output (I/O) signals that each use a dedicated line.

1.3 PHYSICAL DESCRIPTION

MIA1 is a Printed Circuit Board Assembly (PCBA) designed to plug into J1, J2, and J3 on the Interconnect D/D1 PCBA in the T1940-96 Tape Transport. Refer to Figure 1-1. In addition to J1, J2, and J3, a separate cable connects MIA1 to the transport's Write PCBA. Two cables connect J2 and J3 on MIA1 to the F6250 Formatter. Two sets of eight miniature switches are mounted on the MIA1 PCBA. These switches are used to set a hardware serial number that is used as a signature in status reporting.

Addressable registers for storing commands and status information are included in MIA1.

Light-emitting diodes (LEDs) mounted on the board indicate parity status on the incoming WCS signals, and the status of the auto/manual (AUTO/MAN) mode switch. Manually controlled switches mounted on the PCBA are listed in Table 1-1.

Table 1-1
MIA1 Manual Switches

S1	REV OFF FWD	Tape motion control
S2	READ WRITE	Read or write selector
S3	1600 6250	Density (PE/GCR) selector
S4	AUTO MAN	Automatic or manual control selector
U125, S1—S8 U35, S1—S8	—	Hardware serial number select
U196, S1—S8	—	Test pattern switches

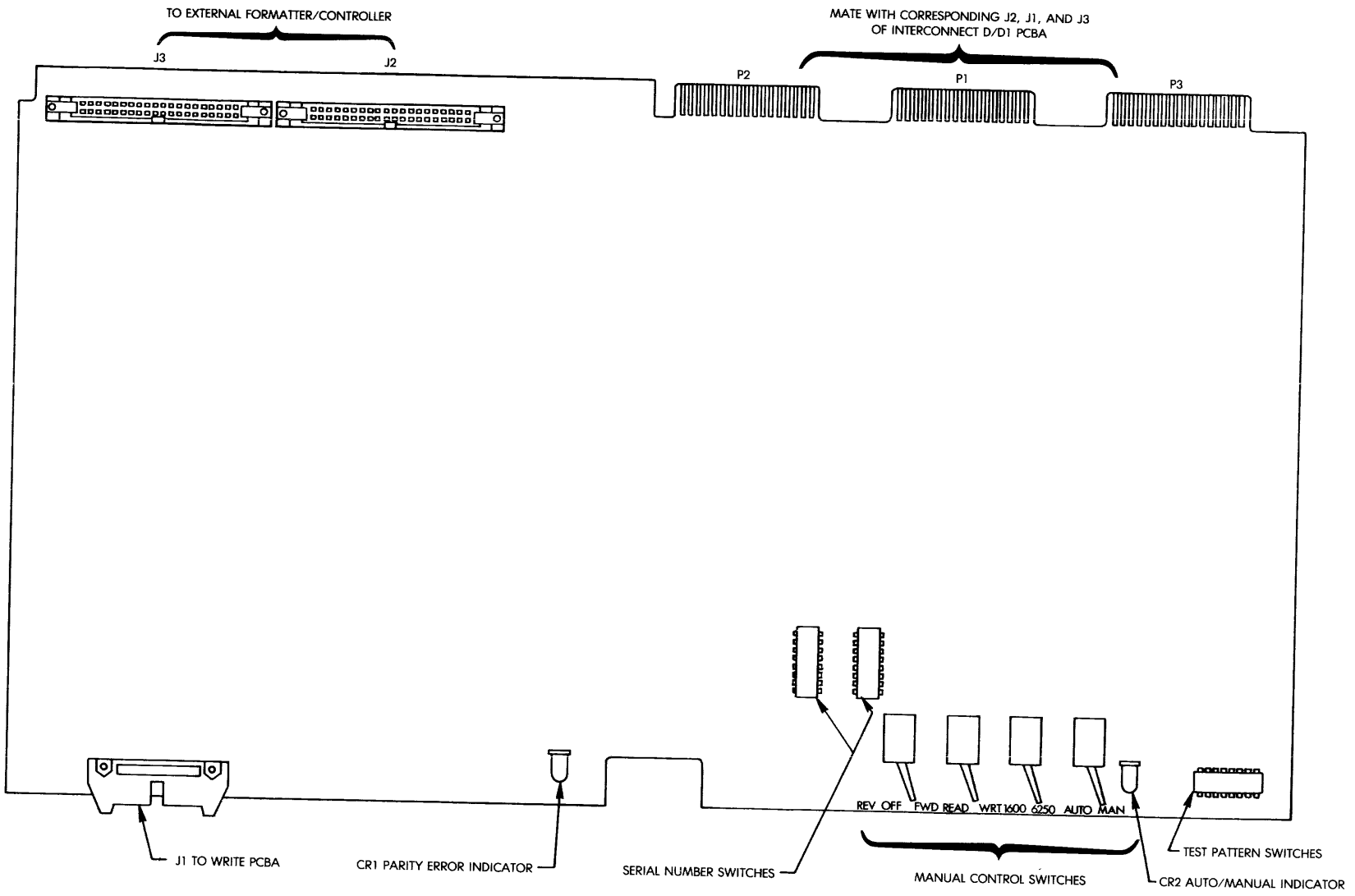


Figure 1-1. Multiple Interface Adapter Controls, Indicators, and Connectors

SECTION II
INSTALLATION AND INTERFACE CONNECTIONS

2.1 INTRODUCTION

This section contains a summary of the physical interface connections and signal lines for the Multiple Interface Adapter. Installation orientation information is provided in the manual for the tape transport that the MIA1 is installed in.

2.2 INTERFACE ELECTRICAL SPECIFICATIONS

Levels: True = Low = <1.0v.
False = High = >2.8v.

The interface circuits are designed so that, in general, an open circuit results in a high signal.

Figure 2-1 shows the configuration of the receivers and transmitters between the controller and microformatter.

2.3 POWER

Power for MIA1 is provided by the tape transport that the MIA1 is installed in.

2.4 INTERFACE CONNECTIONS

Two 40-lead flat cables are required for the formatter-to-MIA1 interface. These two cables connect directly to J2 and J3 on the MIA1 PCBA. The two cables are tied together, forming a single bundle, and should be less than 12.2 metres (40 feet) in length.

Interconnecting provisions between the tape transport and MIA1 are defined in the manual for the transport.

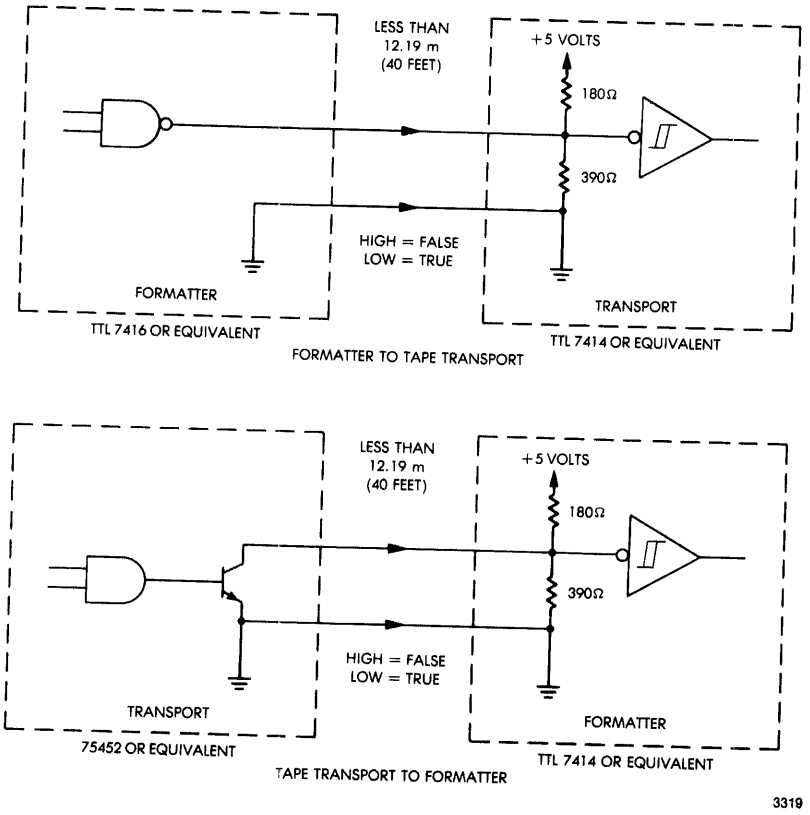


Figure 2-1. Formatter/Transport Interface Drivers and Receivers

SECTION III
OPERATION

3.1 INTRODUCTION

This section defines the Multiplexer Interface Adapter input and output signals and general routing of the signals within MIA1.

3.2 BASIC OPERATION

MIA1 is essentially a switching and routing processor for signals between the external controlling formatter and the tape transport that the MIA1 is installed in.

3.3 MIA1 INPUT/OUTPUT (I/O) ROUTING

MIA1 inputs and outputs are listed in Table 3-1. Note that MIA1 is connected to the F6250 Formatter by two cables connected to J2 and J3 on MIA1. It is connected to the transport via MIA1 edge connectors P1, P2, and P3, that plug into Interconnect D/D1 PCBA connectors J1, J2, and J3, and a single cable between MIA1 connector J1 and Write PCBA connector J25 (on some models designated as J1). Signals at all of these connectors are considered as MIA1 interface signals. The mnemonics are prefixed with I, for *interface*, and they are electronically low when true unless otherwise noted.

3.4 FORMATTER/MIA1 INTERFACE

3.4.1 MODE SELECTION

When the T1940 Tape Transport and MIA1 PCBA are connected into the system, with power on and the transport on line by manual switching, mode selection is at the disposal of the external F6250 Formatter, which deals with the host system. The formatter is notified of the hookup by a high level on the IPRESENT H, that says that the transport and MIA1 are present in the system and powered up. The formatter can then ask for a status report or command specific transport operations (read, write, etc.) using the I/O lines discussed in the following paragraphs.

3.4.2 WRITE/COMMAND/STATUS (IWCS 0—7) LINES

The eight Write/Command/Status (WCS) lines contain meaningful data (write data) to be recorded on tape, MIA1 register addresses, commands or, in the reverse direction, status information. The eight bits simultaneously appearing on the lines as data constitute an 8-bit byte of data (bits 0—7). A byte is often referred to as a character. The parity bit (IWCSP L) is sent over a separate dedicated line.
The F6250 Formatter specifies the nature of the contents of the Write/Command/Status lines in the following manner.

(1) If the signals on the WCS lines are gated into MIA1 by the write data strobe (IWDS L on a separate, dedicated line), the WCS lines will contain Write data to be recorded. The Write data and strobe do not appear on the lines, however, until after a WCS software command specifying the density (PE/GCR), direction of motion, write status, etc. has been processed. Refer to Step (2).

(2) If the signals on the WCS lines are gated into MIA1 by the command strobe (ICMD L on a separate, dedicated line), the signals on the WCS lines will define the address of a register in MIA1 or a command to place in a register previously addressed. If the signals specify an address, the addressed register may contain either commands or status information, as determined by software on the WCS lines. The software coding for the various commands and status signals on these lines is included in the discussion of MIA1 theory. Refer to Paragraph 4.5.

Table 3-1
Multiplexer Interface Adapter (MIA1) Interfaces

Pin	Connections to T1940 Tape Transport				Connections to F6250 Formatter	
	(Via Interconnect D/D1 PCBA)			(Via Write PCBA)		
	P1 (J1)	P2 (J2)	P3 (J3)	J1 (J25)	J2 (to Cable)	J3 (to Cable)
1	NPORST	IWD7	IRD7	IAMTIE7	SPARE	SPARE
2	IEOT	0V(I)	0V(I)	IAMTIE5	GND	GND
3	ILDP			IAMTIE4	IWCS0 L	IAMTIE0 L
4	IFPT				GND	GND
5	IRWD			ILTH	IWCS1 L	IAMTIE1 L
6	IONL				GND	GND
7	IRWU				IWCS2 L	IAMTIE2 L
8	ISWS				GND	GND
9	ISLT0			IWRT BIN H	IWCS3 L	IAMTIE3 L
10	IRWC		0V(I)		GND	GND
11	IDDI		+ 5V	IARA ERR	IWCS4 L	IAMTIE4 L
12	ISRC		+ 5V	IAMTIE3	GND	GND
13	IDDS		+ 5V	IAMTIE6	IWCS5 L	IAMTIE5 L
14	ISFC		0V(I)	IWRT STAT H	GND	GND
15				ISTDTH	IWCS6 L	IAMTIE6 L
16				IMOTION H	GND	GND
17		0V(I)	0V(I)	IAMTIEP	IWCS7 L	IAMTIE7 L
18		IWD6	IRD6	IAMTIE0	GND	GND
19	IRDY	IWD5	NTSTR	IAMTIE1	IWCSP L	IAMTIEP L
20		IWD3	IRD5	IAMTIE2	GND	GND
21	LATE AGC	IWD4	IRD4		ICMD L	IRDP L
22	NTEST	IWD2			GND	GND
23	0V(I)	IWD1			IWDS L	IRD7 L
24		IWD0			GND	GND
25		IWDP			ISTAT L	IRD6 L
26		ITACH	IRD3		GND	GND
27			IRD2		ICMD PE L	IRD5 L
28		ISLT3	+ 5V		GND	GND
29		IRTH2	+ 5V		ITACH L	IRD4 L
30			+ 5V		GND	GND
31		ISLT2	IRD1		SPARE	IRD3 L
32			IRD0		GND	GND
33		ISLT1			SPARE	IRD2 L
34	0V(I)	IWDS	IRDP		GND	GND
35					SPARE	IRD1 L
36					GND	GND
37					SPARE	IRD0 L
38					GND	GND
39					SPARE	IPRESENT H
40					GND	GND

(3) If the WCS lines are gated by the status strobe (ISTAT L on a separate dedicated line), MIA1 will send status information to the formatter over the WCS lines. The information will be from the status register identified by an address previously sent as discussed in Step (2).

3.4.3 MIA1 CONNECTED AND POWER ON (IPRESENT H) LINE

IPRESENT H is a high = true signal sent to the F6250 Formatter by MIA1 when power is on and MIA1 is connected into the system.

3.4.4 COMMAND (ICMD L) LINE

The ICMD L signal line is used to gate the WCS signals into MIA1 when the signals express an address or a command. Refer to Paragraph 3.4.2.

3.4.5 STATUS (ISTAT L) LINE

The ISTAT L signal line is used to gate status information, from a previously specified address, onto the WCS lines. Refer to Paragraph 3.4.2.

3.4.6 WRITE DATA STROBE (IWDS L) LINE

The IWDS L signal line is used to gate WCS signals through MIA1 to the tape transport when the WCS lines contain write data to be recorded on tape. Refer to Paragraph 3.4.2.

3.4.7 COMMAND PARITY ERROR (ICMD PER L) LINE

The ICMD PER L signal line is used to notify the formatter that there is a parity error in WCS signals, as received by MIA1. While ICMD PER L is set, motion and density signals will not be released to the tape transport.

3.4.8 READ DATA (IRDP, 0—7 L) LINES

These nine lines each deliver one channel of data read from the tape, including parity information. A software loop-write-to-read command (LWR) clears the Read Enable bit and then returns the data on the WCS lies to the formatter over the read data lines for testing.

3.4.9 AMPLITUDE TRACK IN ERROR (IAMTIEP, 0—7 L) LINES

A low signal on any of these nine lines indicates that the amplitude of the signal read from the corresponding track is not within an established range. A loop-write-to-read command (LWR AMTIE) will return to the formatter the contents of the MIA1 AMTIE registers previously loaded by the formatter over the WCS lines.

3.5 TAPE TRANSPORT/MIA1 INTERFACE

3.5.1 STATUS SIGNALS

Status signals received from the tape transport over dedicated conductors indicate the status of the transport with respect to the parameters identified by the corresponding mnemonics. Refer to Table 3-2.

These signals are used by the circuits on the MIA1 PCBA and/or are encoded and instantaneoulsy available in MIA1 registers for delivery over the Write/Command/Status lines to the formatter upon request.

3.5.2 WRITE DATA (IWDP,0—7)

The nine write data channels carry data to be recorded on tape. The data put on these channels has been extracted from the Write/Command/Status signals by MIA1. While write data is being processed, all other signals are prohibited from the WCS lines.

Table 3-2
Tape Transport/MIA Status Signals

Mnemonic	Transport Status When True
NPORST	Initiates resetting and presetting of circuits as required when power is applied.
IEOT	The end-of-tape optical marker has been sensed.
ILDP	The tape unit has been selected, is on line, ready, and loaded, with the tape at the beginning-of-tape (load point) position.
IFPT	File protected: writing on tape is inhibited by absence of supply reel write enable ring.
IRWD	The tape transport is in Rewind mode.
IONL	The tape transport has been made available to the system by manual switching to On-line mode.
IDDI	The tape transport circuits are in Phase-Encoded (PE) density mode.
IRDY	The tape transport is ready for a command, provided it is selected and on line.
NTEST	The tape transport is in Test mode and not available to the system.
MOTION	Indicates that the tape transport is in Motion mode.
WRT STAT	Indicates that the transport is in Write mode.
LATE AGC	Indicates that one or more tracks have failed to generate an automatic gain control signal within the character time-frame in GCR mode.
WRT BIN	Indicates that write binary data is being processed for writing on tape. This information is arbitrarily derived from WD4 channel.
ITACH	Pulses generated by the transport capstan optical counter. These pulses are sent to the formatter in real time over a dedicated line and are also sent over a WCS line upon request, as well as being used in MIA internal timing control functions.
IRTH2	Low Threshold mode in progress.

3.5.3 TAPE TRANSPORT SELECT (ISLT0—3) LINES

The ISLT0—2 signals are used to inform MIA1 of the setting of the tape transports identification thumbwheel switch. ISLT3 indicates that the tape transport is in maintenance mode and not available for reading or writing.

NOTE

The ISLT tape transport unit selector signals should not be confused with the software register selection signals (MTC SEL 0—6).

3.5.4 READ DATA (IRDP,0—7)

These nine channels provide MIA1 with data read from the tape. MIA1 makes the data available to the F6250 Formatter over these nine lines.

3.5.5 TEST DATA/STROBE (NTSTR)

NTSTR is used in manual test mode only. It provides test data and strobes the data into the Write PCBA circuits.

3.5.6 THRESHOLD SIGNALS (STDTH, NLTH)

STDTH, high = true, commands the tape transport to operate in the standard threshold mode.

NLTH, low = true, commands the tape transport to operate in the low threshold mode in order to read data that cannot be picked up with sufficient amplitude to be read reliably in the standard threshold mode.

3.5.7 AMPLITUDE TRACK IN ERROR (IAMTIEP,0—7)

These nine channels are each low = true to indicate that the amplitude of read data from the corresponding track is not within the range specified for reliable interpretation. IAMTIEP is not generated as a parity bit for the other eight channels, but reflects the amplitude status of the IAMTIEP track.

3.5.8 WRITE DATA (IWDP,0—7)

These are write signals to be recorded on the nine tracks correlating to bits P and 0—7.

3.5.9 WRITE DATA STROBE (IWDS)

The IWDS signal strobes write data into the Write PCBA circuits.

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section provides information on the theory of operation of the Multiplexer Interface Adapter (MIA1) circuitry.

4.2 THEORY OVERVIEW

MIA1 performs three groups of functions:

(1) It accepts commands and write data from the external F6250 Formatter and relays them to the transport in a form compatible with transport circuits.

(2) It accepts read data, amplitude-track-in-error (AMTIE) signals and status indications from the transport and relays them to the formatter in a form compatible with formatter circuits.

(3) It participates in certain system-checking functions, such as looping WCS signals from the formatter into the read data lines or, through registers, into the AMTIE lines back to the formatter. These functions are called loop-write-to-read (LWR) and loop write to AMTIE (LWR AMTIE).

In dealing with the transport, each signal uses a dedicated path; however, in dealing with the formatter, some of the signals (i.e., write data and most of the command and status indications) use the same conductors on a time-share basis. The multiplexing/demultiplexing of the latter signals on the Write/Command/Status lines is the basic function of MIA1.

Figure 4-1 illustrates the general theory of the signal flow and management used on the MIA1 PCBA. Reference is also made to Pertec Schematic No. 107885. The various signal paths are described in detail in the following paragraphs.

4.3 WRITE/COMMAND/STATUS (WCS) SIGNAL MULTIPLEXING

Signals on the eight WCS lines (IWCS0—7 L) at J2-3,5,7,9,11,13,15,17 (zone 2-1E,H) may contain write data or command data from the formatter, or status signals to the formatter. The formatter determines which signals are to be placed on the WCS lines and notifies MIA1 of the determination. This notification is by means of ICMD L, ISTAT L, IWDS L, and of the software commands placed on the WCS lines. Refer to Paragraph 3.4.2 and 4.5.

The junctions for the two-way WCS traffic are shown in the upper right-hand corner of sheet 2 of the schematic and in simplified form in Figure 4-2. The levels at J2 on the IWCS0—P lines are held high by the terminator (T) packs unless pulled down by internal MIA1 signals or signals at the interface from the F6250 Formatter or equivalent host system controller.

Interface IWCS signals are inverted (e.g., at U62-2, zone 2-2H) and applied to either the write data circuits (refer to Paragraph 4-4) or the command circuits (refer to Paragraph 4-5) depending on the mode of operation.

Status information is gated to the IWCS0—7,P lines when MTS STAT H (zone 2-5E) is true, enabling the drivers shown in zones 2-3F-H. This mode is initiated by status command (ISTAT L) input (zone 3-8C).

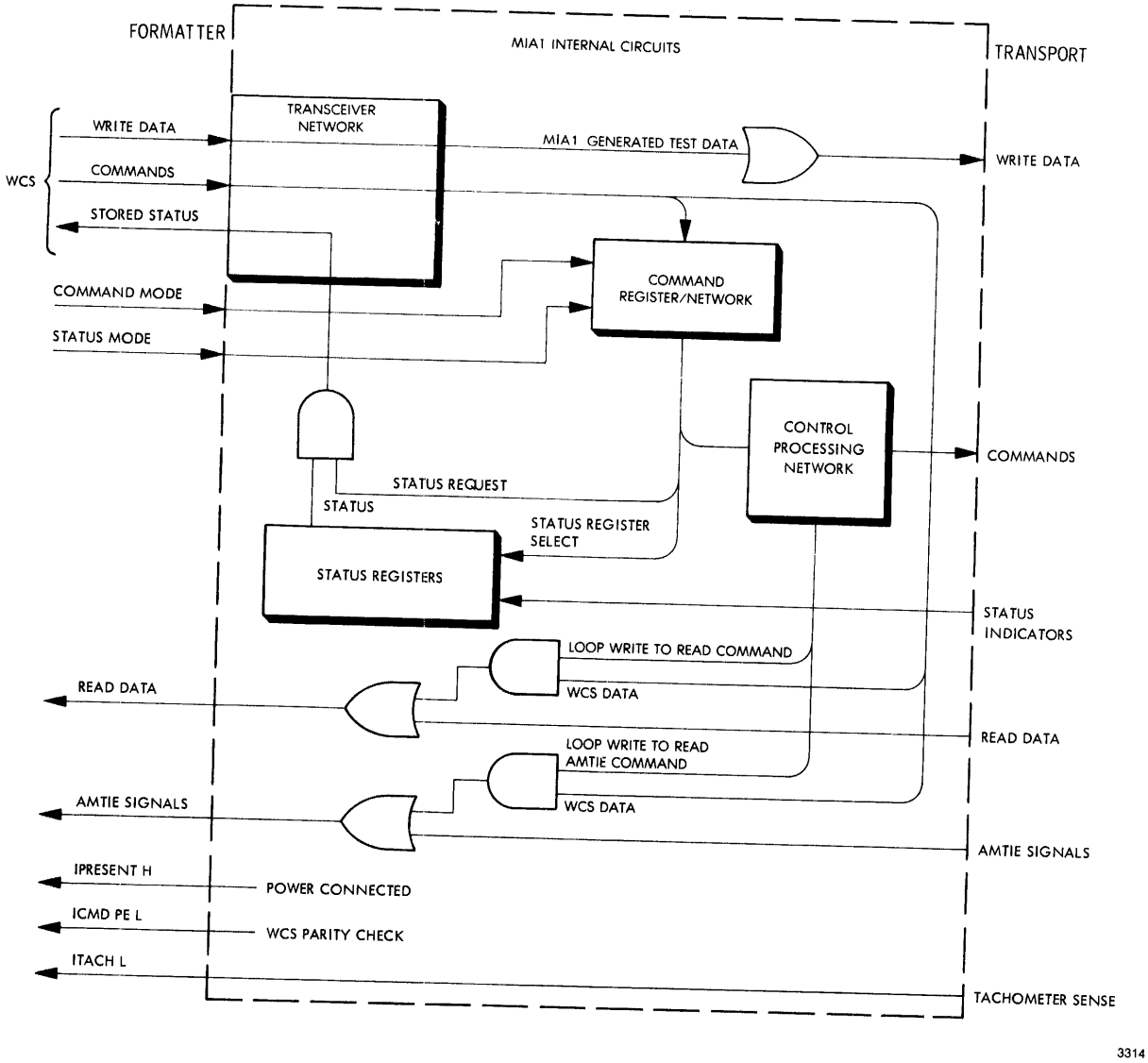


Figure 4-1. MIA Internal Signal Flow Diagram

4.4 WRITE/COMMAND/STATUS WRITE DATA

In Write mode, the inverted IWCS signals (refer to Paragraph 4-3) are gated to the transport write circuits as shown in zones 2-2C through 2-1E. The signals on transport interface lines IWDP,0—7 are valid write data if MIA TEST L is false (high). When MIA TEST L is true, IWDSP,0—7 contain test data generated by U172 (zone 2-3A), which clocks U102-1 (zone 2-3B). U102-5 output is gated through U101-3,1 during test mode and applied to the write data lines.

The inverted IWCS inputs are also made available to the read data circuits (MTS WCS0—7 H signals from zones 2-2H,G,F to zones 4-5 and 4-3). This provides for the host system to put data on the read lines (IRD0—7, zones 4-2H through B) for test purposes. The loop write to read mode is selected when MTC D LWR H (zones 3-3G and 4-6A) is true.

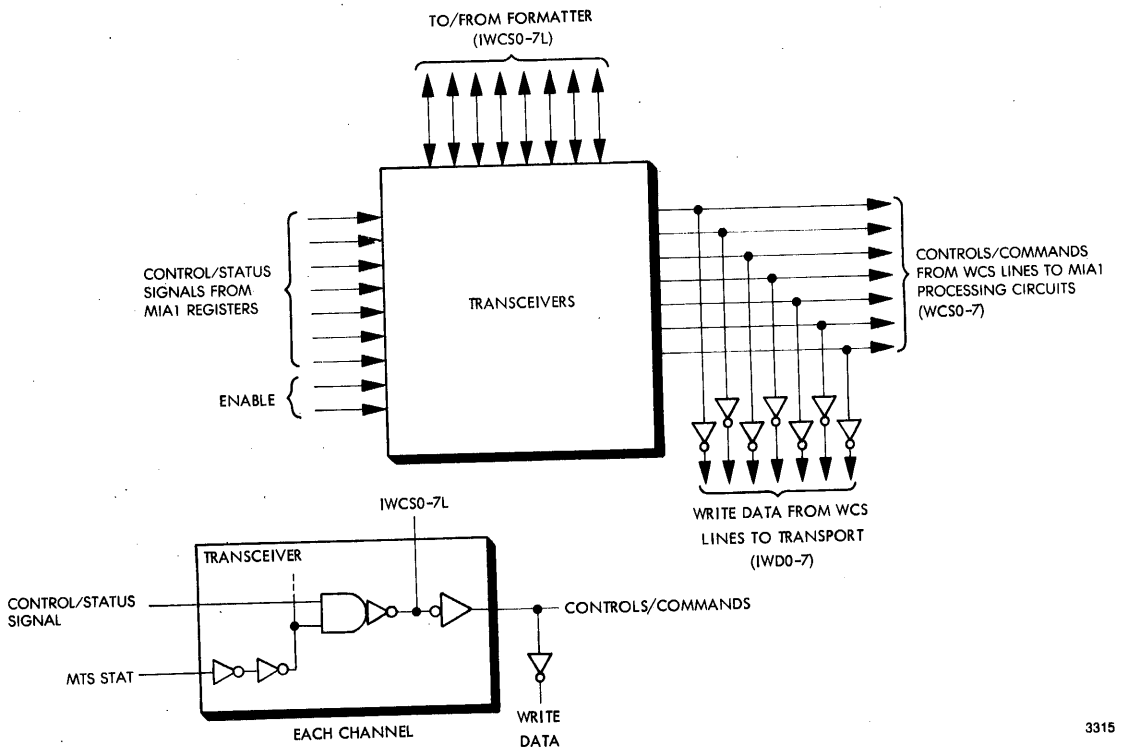


Figure 4-2. Write/Command/Status Junction

4.5 WRITE/COMMAND/STATUS (WCS) COMMAND/ADDRESS SIGNALS

IWCS data, as inverted to MTS WCS0—7,P (zones 2-2H,G,F) are sent to zones 3-7G,H and made available to the command register network (left-hand side of sheet 3). When the command (ICMD L) input at J2-21 (zone 3-8D) is true, the MTS WCS0—7 signals (zone 3-7G,H) are latched into the command registers (zones 3-5,6). When the magnetic tape command execute (MTC EXEC) is developed (zone 3-6F), the outputs of the command registers specify the appropriate actions to be taken or conditions to be observed. E.g., zone 3-5G identifies the magnetic tape commands write inhibit (MTC WT INH), set write status (MTC SWS), synchronous reverse (MTC SRC), loop write to read (MTC LWR). The synchronous forward command (MTC SFC L) is shown, inverted, in zone 3-4G.

4.5.1 WCS COMMAND PARITY CHECK

U162 (zone 3-5C) checks the command byte for parity. If an error is found, U163-5 initiates a high CMD PAR ERR signal through flip-flop U132-3,5 (zone 3-7C) at the end of the command pulse, when input goes low.

The high = true CMD PAR ERR signal is inverted and sent through J2-27 (zone 3-7D), to the formatter. The I/O signal identification is ICMD PEL. CMD PAR ERR, inverted through U92-1,2, is also used to turn on the parity error indicator LED, CR1, in zone 3-7D.

4.5.2 WCS COMMAND/STATUS (WCS) SOFTWARE

Control of the tape transport unit (TU) and acquisition of a specific set of status indications are effected by command signals sent from the formatter to MIA1 interface over the Write/Command/Status (WCS) lines. Because of the bidirectional and multiplexed traffic on these lines, command and status information are handled by specifically addressable registers. Instantaneous status information is constantly updated at the registers and available on request.

4.5.2.1 Addressing MIA1 Command/Status Registers

A specific command register (e.g., registers shown in Pertec Schematic No. 107885, zones 3-5D to H) or status registers (e.g., registers shown in zones 2-3A to E) is addressed by the formatter as follows:

(1) The register address (location) will be specified on the WCS lines in the following format, where a 1 indicates a set bit (1 = true = low):

IWCS Bit: 7 6 5 4 3 2 1 0

Bit State: 1 0 0 ←address→

Note that IWCS7 will be set and IWCS6 and 5 not set, regardless of the address. The address will be a binary coded octal number in bits IWCS4,3,2,1, and 0.

(2) A low ICMD L pulse is issued to gate the address specified per Step (1) into the command/Status address (CMD/STAT ADR) register.

Once an address has been selected, it will remain in effect until a new address is specified.

The selected address applies to either a command register or a status register (refer to Table 4-1), depending on whether it is gated in by an ICMD L or the ISTAT L pulse. If ICMD L is received, the next WCS data will be stored in the command location specified in the CMD/STAT ADR register. If ISTAT L is received, status information in the status location specified in the CMD/STAT ADR register will be sent over the WCS lines to the formatter.

4.5.2.2 Command/Control Register Bit Assignments

Bit assignments for the command register locations listed in Table 4-1 are defined in Tables 4-2 through 4-9. These assignments are valid only after an address has been specified (Paragraph 4.5.2.1) and the succeeding WCS signals are gated in by an ICMD L pulse.

The formatter commands to be written in the addressed locations are sent on the WCS lines according to Tables 4-2 through 4-9, which define the bit assignments at the various addresses for command usage.

NOTE

A command to be written in a register is valid only if bit 7 (IWCS7) is not set. The 7 bit is set only in command bytes which specify an address.

Table 4-1 lists addresses in decimal, octal and binary coded numbers. Addresses referenced in titles of succeeding tables are expressed in octal numbers.

4.5.2.3 Status Register Bit Assignments

Bit assignments for the status register locations listed in Table 4-2 are defined in Tables 4-10 through 4-18.

Table 4-1

MIA1/MIA Command/Status Register Address

Address Number		Address Specifier Command								Registers addressed if next WCS is gated in by ICMD L	Registers addressed if address is followed by ISTAT L
Decimal	Octal	7	6	5	4	3	2	1	0		
0	0	1	0	0	0	0	0	0	0	TU CMD A	TU STATUS
1	1	1	0	0	0	0	0	0	1	TU CMD B	MIA STATUS A
2	2	1	0	0	0	0	0	1	0	AMTIE LOOP	MIA STATUS B
3	3	1	0	0	0	0	0	1	1	THRESHOLD	SERIAL NR A
4	4	1	0	0	0	0	1	0	0	not used	SERIAL NR B
5	5	1	0	0	0	0	1	0	1	not used	TU DIAG
6	6	1	0	0	0	0	1	1	0	not used	not used
7	7	1	0	0	0	0	1	1	1	TEST PATT	TEST PATT
8	10	1	0	0	0	1	0	0	0	TC HI	TC HI
9	11	1	0	0	0	1	0	0	1	TC LOW	TC LOW
10	12	1	0	0	0	1	0	1	0	not used	not used
11	13	1	0	0	0	1	0	1	1	not used	not used
12	14	1	0	0	0	1	1	0	0	not used	not used
13	15	1	0	0	0	1	1	0	1	not used	not used
14	16	1	0	0	0	1	1	1	0	not used	not used
15	17	1	0	0	0	1	1	1	1	not used	not used
16	20	1	0	0	1	0	0	0	0	Generate Test Pattern CMD	not used

NOTES:

1. WCS bit number 7 (IWCS7 L) must be set (low) to validate 4—0 as an address to be placed in CMD/STAT ADR register.
2. Abbreviations
   - TU Tape transport unit
   - TC Tachometer counter
   - NR Number (part of hardware serial number)
   - DIAG Diagnostic
3. Contents at the various addresses are defined in separate table as referenced in text.

These assignments indicate the bit definitions for various status indications supplied by other circuits. This information is sent to the formatter on the WCS lines only on the following prior conditions.

(1) An address (Table 4-1) has been gated in by ICMD L.

(2) An ISTAT L pulse is received.

NOTE

All eight bits are available for status information. The use of bit 7 (IWCS7) is restricted only in command mode.

4.6 TRANSFER TIMING

Figures 4-3, 4, and 5 define the transfer timing parameters for Write/Command/Status and associated interface lines between the tape control unit (TCU), e.g., formatter, and the tape unit (TU) at the MIA1 interface. The times specified in this section must be met to insure correct tape subsystem operation.

The times are based on signal levels listed in Table 4-19 as measured at the tape unit MIA1 interface. The IPRESENT H signal is excluded.

Table 4-2
Command Bit Descriptions — CMD/STAT ADR = 0, TU CMD A

Bit	Name	Meaning When Set
7		Must be 0 to obtain listed meanings on bits 6—0.
6	FWD	The tape unit, if RDY and ON LINE, moves the tape in the forward direction.
5	REV	The tape unit, if RDY and ON LINE, moves the tape in the reverse direction. The tape will stop upon detection of BOT.
4	WRITE	The tape unit, if ON LINE and not FPT and not REW, is enabled to erase the tape. If not WR INH, then the tape may also be written.
3	WR INH	Inhibits the write head from being energized, while allowing the erase head to operate normally.
2	LWR	Loop write to read causes the tape unit to drive the 9 read data (RD) lines from the corresponding 9 WCS lines, and the 9 AMTIE lines from the corresponding 9 AMTIE LOOP bits.
1	AMTIE LOOP 1	When LWER is set, these bits drive the AMTIE bus lines. (Refer to LWR.)
0	AMT LOOP P	When LWR is required, bit 6 of CMD/STAT ADR 3 (Table 4-5) must be written to 0.

Table 4-3
Command Bit Descriptions — CMD/STAT ADR = 1, TU CMD B

Bit	Name	Action Performed Upon Command Write
7-3	TU CMD	Must be 0s to obtain listed meanings on bits 2—0.
2,1,0		The bits cause a tape unit function to be performed.
0 0 0		-0 CLR TU — Clears FWD, REV, WRITE, WR INH, LWR, DSE, CMD PE and RDY ON.
0 0 1		-1 SET PE — Set to PE recording format.
0 1 0		-2 SET GCR — Set to GCR recording format.
0 1 1		-3 CLR EOT — Clear EOT status.
1 0 0		-4 REWIND — If RDY and ON LINE, the tape is rewound to BOT. RDY will be = 0 until rewind sequence has completed.
1 0 1		-5 UNLOAD — If RDY and ON LINE, tape is rewound and removed from the tape path. RDY will be cleared.
1 1 0		-6 DSE — Causes FWD to set until EOT or until a CLR TU command (Data Security Erase mode.)
1 1 1		-7 TEST — Sets RDY ON and CMD PE, causing the CMD PE L bus signal to be asserted.

Table 4-4

Command Bit Descriptions — CMD/STAT ADR = 2, AMTIE LOOP

Bit	Name	Meaning
7		Not set (0) to obtain listed meanings on bits 6—0.
6—0	AMTIE LOOP (channels 6—0, respectively)	When LWR is set, the bits drive the corresponding AMTIE bus lines.

Table 4-5

Command Bit Descriptions — CMD/STAT ADR = 3, Threshold

Bit	Name	Meaning
7		Must be zero to obtain meanings listed for bits 6—0.
6	READ ENABLE	Enables read data and AMTIE paths from transport, must be zero (high) to disable paths in LWR operation. Refer to Table 4-2.
5,4,3	PORT SEL <B,1,0>	Refer to Paragraph 3.3.3.
2	NM RD THR	When set, tapes are read using *normal read threshold*. Otherwise, the read electronics will operate in the *extra low read threshold* mode. This affects only the 9 read data (RD) bus signals.
1,0	AMTIE THR	Establishes the threshold of the read electronics for the 9 AMTIE bus signals as follows: 0 0 — 10% } (IBG CHECK) 0 1 — 10% } 1 0 — 25% (WRITE) 1 1 — 20% (READ) These percent figures are relative to the nominal playback amplitude which must be met for any line to be negated.

Table 4-6

Command Bit Descriptions — CMD/STAT ADR = 7, Test Pattern

Bit	Name	Meaning
7		Must be 0 to differentiate the test command pattern from an address.
6—0	Test Pattern	May be 1s or 0s as required by the test procedure. Test pattern bit 7 is always read as a 1. The loaded pattern will be generated on all 9 channels with bit 7 first, then bit 6... until all have been sent; then it will recycle bit 7, 6 . . ., etc.

Table 4-7
Command Bit Descriptions — CMD/STAT ADR = 10, TC HI

Bit	Name	Meaning
7 6—0	TC HI	Must be 0 (high) to obtain listed meanings. Used to load zeros into the tachometer pulse counter high location. Writing non-zero values is useful only for diagnostic purposes.

Table 4-8
Command Bit Descriptions — CMD/STAT ADR = 11, TC LOW

Bit	Name	Meaning
7 6—0	TC LOW	Must be 0 (high) to obtain listed meanings. Used to load zeros into the tachometer pulse counter low location. Writing non-zero values is useful only for diagnostic purposes.

Table 4-9
Command Bit Descriptions — CMD/STAT ADR = 20
Generate Test Pattern CMD

Bit	Name	Meaning
N/A	Generate Test Pattern Command	As soon as this register is addressed, test pattern data will be gated onto the write data lines, and will increment the pattern with each IWDS strobe received from the formatter.

Table 4-10

Status Bit Descriptions — CMD/STAT ADR = 0, TU STATUS

Bit	Name	Meaning When Set
7	RDY	The tape unit is ON LINE, not REW, not loading or unloading, and all interlocks are made.
6	RDY ON	RDY has transitioned to the 1 state. Cleared by a CLR TU command in TU CMD B.
5	ON LINE	The tape unit is on line in the system.
4	REW	The tape unit is rewinding.
3	PES	The tape unit is set to phase encoded recording format. The TU CMD B command location is used to select recording format.
2	BOT	The BOT marker on the tape is positioned under the BOT sensor, and RDY is set.
1	EOT	The EOT marker on the tape passed under the EOT sensor during a FWD operation with RDY set. Clears when: (1) The EOT marker passed under the EOT sensor during a REV operation with RDY set. (2) The TU is rewinding (RWD). (3) A CLR EOT command is written into the TU CMD B location.
0	FPT	The tape reel does not have the write enable ring in place.

Table 4-11

Status Bit Descriptions — CMD/STAT ADR = 1, MTA STATUS A

Bit	Name	Meaning
7	NOT WR	There is no current flowing through the write or erase heads. (Same as TU DIAG, bit 6).
6	FWD	The FWD command bit has been written with a 1, or a DSE command has been written into the TU CMD B location.
5	REV	Indicates the state of the REV command bit.
4	WRITE	Indicates the state of the WRITE command bit.
3	WR INH	Indicates the state of the WR INH command bit.
2	LWR	Indicates the state of the LWR command bit.
1	MOT	Motion status bit from tape transport.
0	DSE	A DSE command has been written into the TU CMD B location. Clears when EOT sets, or when a CLR TU command is written into TU CMD B.

Table 4-12
Status Bit Descriptions — CMD/STAT ADR = 2, MIA STATUS B

Bit	Name	Meaning When Set
7	CMD PE	A command or address has been received by the tape unit with even parity, or a TEST command has been written into TU CMD B. Clears when a CLR TU has been received, whether parity is correct (odd) or not. This bit drives the CMD PE L bus signal.
6	PEC	A command has been set to TU CMD B to set the tape unit to phase encoded recording format. Assuming proper hardware operation, this bit is the same as PES in TU STATUS.
5	ARA ERR	During a GCR operation from 241.3 mm (9.5 inches) to 387.35 mm (15.25 inches) after BOT, the read amplifier gains failed to achieve the required value. Valid only if RDY is set.
4,3 0 0 0 1 1 0 1 1	SPEED <1:0>	Indicates the speed of the tape unit. 0 not used 1 1.905 m/s (75 ips) 2 3.175 m/s (125 ips) 3 1.143 m/s (45 ips)
2,1,0	PORT SEL <B,1,0>	Shows the position of the multi-position port select switch in the tape unit. The bits are meaningful only when the PORT SEL bits in the THRESHOLD command location have been written to ones. If bits are all high, the tape unit is in maintenance mode.

Table 4-13
Status Bit Descriptions — CMD/STAT ADR = 3, SERIAL NR A

Bit	Name	Meaning
7—4	SN TH <3:0>	The BCD thousand's digit of the tape unit's serial number.
3—0	SN H <3:0>	The BCD hundred's digit of the tape unit's serial number.

Table 4-14
Status Bit Descriptions — CMD/STAT ADR = 4, SERIAL NR B

Bit	Name	Meaning
7—4	SN TENS <3:0>	The BCD ten's digit of the tape unit's serial number.
3—0	SN ONES <3:0>	The BCD one's digit of the tape unit's serial number.

Table 4-15
Status Bit Descriptions — CMD/STAT ADR = 7, TEST PATT

Bit	Name	Meaning
7—0	TEST PATT	Bit 7 will be 1 for all test patterns.

Table 4-16
Status Bit Descriptions — CMD/STAT ADR = 5, TU DAIG

Bit	Name	Meaning When Set
7	NOT WR BIT 4	Indicates the state of the write driver for track 4.
6	NOT WR	There is no current flowing through the write or erase heads. (Same as MTA STATUS A, bit 7.)
5	LATE AGC	The ARA amplitude is marginally low. (GCR only).
4	EOT DET	The EOT reflective tab is positioned under the EOT sensor. Not valid unless RDY = 1.
3	TACH	The output from the capstan digital tachometer.
2	NM RD THR	Indicates the state of the NM RD THR bit as last written in the THRESHOLD command location.
1,0	AMTIE THR <1:0>	Gives the value of the AMTIE THR field as last written into the THRESHOLD command location.

Table 4-17
Status Bit Descriptions — CMD/STAT ADR = 10, TC HI

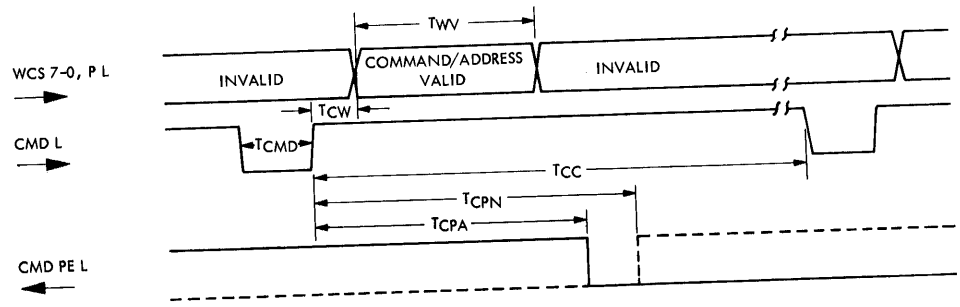
Bit	Name	Meaning
7—1	TC HI	Reflects part of the number of 1—0 transitions of tachometer signal since the tachometer counter was last cleared by writing 0s. Refer to Table 4-7.

Table 4-18
Status Bit Descriptions — CMD/STAT ADR = 11, TC LOW

Bit	Name	Meaning
7—1	TC LOW	Reflects part of the number of 1—0 transitions of tachometer signal since the tachometer counter was last cleared by writing 0s. Refer to Table 4-8.

Table 4-19
Transfer Timing Signal Levels

	Signal Source	
	TCU	TU
Asserted	<1.6	<1.0V
Negated	>2.3V	>2.8V



NOTES:

1. ➡ ASSERTED BY TAPE CONTROL UNIT (TCU)
2. ⬅ ASSERTED BY TAPE UNIT (TU)
3. MEASURED AT TAPE UNIT
4. TIMES ARE IN NANOSECONDS

SYMBOL	MIN.	MAX.	PARAMETER
T_{CMD}	200		WIDTH OF CMD L
T_{CW}		250	TRAILING EDGE OF CMD L TO WCS LINES VALID
T_{CC}	720		CMD L TRAILING EDGE TO LEADING EDGE OF NEXT CMD L
T_{WV}	720		WCS LINES VALID
T_{CPA}	0	750	CMD L TRAILING EDGE TO CMD PE L ASSERTION, IF A PARITY ERROR
T_{CPN}	0	850	CMD L TRAILING EDGE TO CMD PE L NEGATION, IF A CLR TU COMMAND

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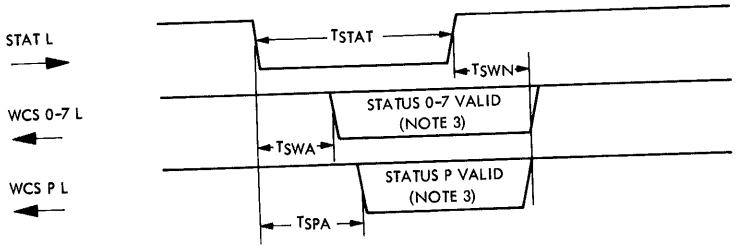
Figure 4-3. Command/Address Transfer Timing



NOTES:

1. MEASURED AT THE TAPE UNIT (TU)
2. TIMES ARE IN NANOSECONDS
3. THE WCS LINES MAY NOT CHANGE DURING THIS TIME, EVEN IF THE STATUS INFORMATION BEING PRESENTED IS NO LONGER CORRECT
4. ➡ ASSERTED BY TAPE CONTROL UNIT (TCU)
5. ⬅ ASSERTED BY TAPE UNIT (TU)

SYMBOL	MIN.	MAX.	PARAMETER
T_{STAT}	250		WIDTH OF STAT L
T_{SWA}	0	75	STAT L LEADING EDGE TO WCS LINES 0-7 VALID, TU ADR = $0\text{-}7_8$
	0	250	STAT L LEADING EDGE TO WCS LINES 0-7 VALID, TU ADR = $10\text{-}17_8$
T_{SPA}	0	145	STAT L LEADING EDGE TO WCS LINE P VALID, TU ADR = $0\text{-}7_8$
	0	320	STAT L LEADING EDGE TO WCS LINE P VALID, TU ADR = $10\text{-}17_8$
T_{SWN}	0	200	STAT L TRAILING EDGE TO WCS LINES 0-7, P NEGATION

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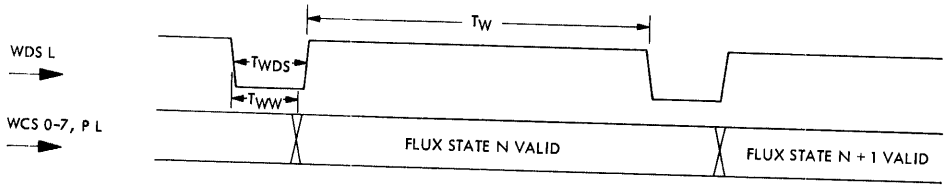
Figure 4-4. Status Transfer Timing



NOTES:

1. MEASURED AT TAPE UNIT
2. ALL TIMES IN NANOSECONDS

SYMBOL	MIN.	MAX.	PARAMETER
TWDS	95		WIDTH OF WDS L
TWW	-50	90	WDS L LEADING EDGE TO WCS LINES VALID
TW	550		WDS L TRAILING EDGE TO LEADING EDGE OF NEXT WDS L

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Figure 4-5. Write Data Transfer Timing