PRIAM

8-INCH WINCHESTER DISC DRIVES

FIELD SERVICE MANUAL

PRELIMINARY

PREFACE

This manual has been prepared for the benefit of field service personnel who are directly involved with the installation and maintenance of PRIAM 8-inch disc drives. It may also contain information helpful to the OEM manufacturer of products containing these drives.

In producing this manual, PRIAM has sought to provide enough information to enable the following field operations to proceed smoothly and efficiently:

Preparation, including provision for compatibility of related equipment, proper power, and cabling.

Installation and initial testing.

Fault isolation to the assembly level.

Assembly replacement.

The manual contains enough theory of operation to give the reader a general background on how the drive works. This is intended solely to provide a context for the testing and troubleshooting procedures. It is not intended that the manual should enable the reader to do detailed intra-board troubleshooting or board repair.

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SECTION 1 - GENERAL INFORMATION

The PRIAM family of 8-inch Winchester disc drives represents the lower end of the PRIAM product spectrum. Two models are available, providing a choice of storage capacities, as shown in the following table:

Model Number	Megabytes	Discs	Data Heads	Tracks/Inch
DISKOS 3450	35	3	5	480
DISKOS 7050	70	3	5	960

1.1 FEATURES

The advantages offered by the 8-inch family of drives include:

1. Relatively High Storage Capacity
2. Very Small Size (Same as 8" floppy)
3. High Performance
4. High Reliability
5. Universal Power Compatibility
6. Ease of Interfacing

The above advantages are achieved through a combination of design features, as described in the following paragraphs:

1. The relatively high storage capacity is achieved by using high recording and track densitites.
2. Overall size is kept small by designing the various assemblies in the proper relationships to one another. The two drives in the PRIAM 8" family have identical overall dimensions. Standard floppy disc mounting can be used.
3. High performance is achieved through the use of fully servoed, linear voice coil head positioning. This makes possible the high precision and stability needed in order to utilize the higher recording and track densities. It also enables the fast access times necessary for efficient use of the data bases.
4. High reliability is achieved through the use of a fully sealed, positive pressure air filtering system, servoed spindle speed and head positioning systems, cast metal head disc assembly, efficient cooling system, and microprocessor implementation of control functions.

6. Power compatibility is assured through the use of all DC components, including a DC spindle motor. PRIAM drives can be used anywhere in the world.

7. Ease of interfacing is assured by the availability of several different interfaces, including a PRIAM standard interface, a PRIAM SMD interface, and an ANSI interface. Each of these has been designed in relation to an entire class of existing computer hardware. Virtually any bus now in use can be accomodated by one PRIAM interface or another. See the section on Options (below) for a complete listing.

1.2 SPECIFICATIONS

The data sheet (on the following page) summarizes the operating characteristics, physical characteristics, and power requirements for the two drives in the PRIAM 8-inch family.

1.3 CONFIGURATION

1.3.1 Physical Configuration

Figures 1.3-1, and 1.3-2 show the overall physical configurations for the DISKOS 3450 and 7050, respectively.

1.3.2 Functional Organization

Figure 1.3-3 is a block diagram showing the relationships among the major functional units in a PRIAM 8-inch disc drive.

Figure 1.3-1 Physical Configuration of the DISKOS 3450

Figure 1.3-2 Physical Configuration of the DISKOS 7050

Figure 1.3-3 Block Diagram of a PRIAM 8-inch Disc Drive

1.4 OPTIONS

1.4.1 Interface Options

The PRIAM 8-inch disc drives are available with a variety of interface options, as described below. Each of these interfaces can be used, without modification, on any disc drive in the 8-inch family. All PRIAM interfaces include on-board data separation.

The standard PRIAM Interface is designed for low cost and for efficient use with microprocessor-based systems. Up to four drives may be daisy-chained, when this interface is used. The PRIAM interface provides a basic 8-bit bidirectional bus, which may be used with the currently popular 8-bit and 16-bit microprocessors. It also provides bit-serial NRZ data exchange. No elaborate handshaking protocols are required. The PRIAM interface is built into the disc drive's main PCB. A 50-conductor flat ribbon cable is used between the PRIAM interface and the host system. See the PRIAM INTERFACE section for more details.

The SMD Interface permits a PRIAM drive to be used with existing Storage Module Drive (SMD) controllers. In the 8-inch drives the SMD interface is available as an adapter which is installed between the drive electronics and the SMD controller. The line drivers and line receivers in the SMD interface are matched to those of typical SMD controllers. There are two interface cables between the host system's SMD controller and the PRIAM disc drive's SMD interface -- a 60-conductor twisted-pair flat cable ("A" cable) and a 26-conductor flat ribbon cable ("B" cable). See the SMD INTERFACE section for more details.

The ANSI Interface complies with the disc drive interface standard proposed by ANSI Technical Committee X3T9. Characteristics of the ANSI interface include variable and fixed sector sizes, data transfer rates up to 10 megabits per second, and radial attention and select capability. Up to eight drives may be daisy-chained, on a single 50-conductor flat ribbon cable. See the ANSI INTERFACE section for more details.

1.4.2 Interface Cables and Terminators

I/O cables are available from PRIAM, for connecting the user's controller to the PRIAM disc drive, and for connecting daisy-chained drives to one another. Cables come in 6, 15, and 25-foot lengths.

Terminators are available for I/O signal lines, to minimize reflections and to ensure maximum data integrity. One set of terminators is required for a single drive, or for the base drive in a daisy chain.

1.4.3 Power Supplies and Cables

PRIAM's optional power supply allows PRIAM disc drives to operate from 100, 120, 220, and 240 VAC, 50 or 60 Hz power. The optional power supply must be mounted separately from the drive. It does not fit within the drive frame.

A DC power cable is available for those users who provide their own external power supplies.

1.4.4 Mounting Hardware

SECTION 2 - INSTALLATION

The disc drive is packaged to withstand normal handling in a reusable shipping container. It is the customer's responsibility to notify the carrier if shipping damage should occur to the drive. Any insurance protection is also the customer's responsibility.

When the shipment is received, the shipping container should be examined for obvious signs of shipping damage. Most insurance adjusters require an inspection of the damaged container. Notify the carrier and PRIAM Customer Service immediately, if shipping damage is discovered.

2.1 UNPACKING

The disc drive is shipped with an outer and an inner carton. Open the outer carton by cutting the tape on the top side. Remove the inner carton and open it by cutting the tape.

Remove the disc drive from the carton and place it on a clean, flat work surface. Remove the wrap.

2.2 VISUAL INSPECTION

Visually inspect the drive for loose, bent, or broken parts. Report any damage to the carrier and to PRIAM Customer Service.

2.3 JUMPERS

If a PRIAM optional power supply is to be used, check the AC voltage selection circuit board prior to applying power. This board is adjacent to the AC input plug, and is an integral part of the power supply. To select a voltage, remove the selection circuit board and reinsert it so that the proper AC voltage designation (100, 120, 220, or 240) is visible. Also check the fuse value. A 4 ampere fuse is used with 100 or 120 VAC, while a 2 ampere fuse is used with 220 or 240 VAC. No modification is required for changing from a 60 Hz power source to a 50 Hz power source, or vice versa.

2.4 SWITCH SETTINGS

The drive address, write protect parameters, and sector size are all switch selectable. The switches are located on the main PCB. Referring to the following table and to Figure 2.4-1, set the switches according to the desired operating conditions.

The table inserted here is a cleaned up version of Field Engineering Bulletin 8-001. Figure 2.4-1 is a drawing of the main PCB, showing the switch locations. Figure 2.4-1 may be omitted if the reference locators are explicitly marked on the main PCB.

2.5 MOUNTING

The disc drive may be mounted in a standard 8-inch floppy disc enclosure.

2.6 GROUNDING

2.7 CABLING

The power cable should be installed to connector J5 (see Figure 2.7-1). The DC voltages required at the respective pins on J5 are listed (below) in the PERFORMANCE CHECK section. Interface cables to the host system are described in the sections covering each of the available interface options. Cabling between assemblies within the disc drive is completed at the factory prior to shipment. More details on inter-assembly cabling are given in the ASSEMBLY RERLACEMENT PROCEDURES section.

Figure 2.7-1 shows how to find connector J5.

2.8 UNLOCKING

Both the drive spindle and the head carriage are locked prior to shipment. After the drive has been completely mounted and cabled, these must be unlocked to enable normal operation.

The drive spindle and head carriage lock is fully accessible on the bottom of the HDA (Head Disc Assembly). Referring to Figure 2.8-1, place this lever in the UNLOCK position.

CAUTION: AVOID MANUAL ROTATION OF THE SPINDLE OR MOVEMENT OF THE CARRIAGE. DAMAGE TO THE DISC SURFACE MAY OCCUR IF THE HEADS ARE MOVED ACROSS A NON-ROTATING DISC SURFACE.

Figure 2.8-1 shows the location of the spindle and head lock lever.

2.9 PERFORMANCE CHECK

Conduct a performance check, as described in the OPERATING PROCEDURES section.

2.10 LOCKING

The drive spindle and the head carriage should be locked whenever the drive is to be physically moved, even if it is not to be shipped. To lock the drive, refer to Figure 2.8-1, and place the lever in the LOCK position.

2.11 REPACKING

Repacking is the reverse of the unpacking procedure. Prior to repacking the drive, make sure that the spindle and carriage lock lever is in the LOCK position.

2.12 STORAGE

When the environment is severe, or when the drive is to be stored for a long time, it should be repacked prior to storage.

When storing unpacked drives, avoid dusty or unstable environments.

2.13 SHIPPING

Contact PRIAM Customer Service for a return authorization number prior to shipping a drive or assembly to PRIAM. After locking the drive spindle and head carriage, pack the drive in its original carton or an equivalent one.

SECTION 3 - OPERATING PROCEDURES

3.1 SPINDLE AND HEAD LOCKS

Before the drive can be operated, it is necessary to place the spindle and head lock lever in the UNLOCK position. Refer to Figure 2.8-1 for the location of this lever.

Whenever the drive is to be moved for any reason, the spindle and head lock lever should be placed in the LOCK position.

3.2 POWERING UP/DOWN

The exact procedure for powering up the drive depends on the interface option present.

If the drive has a standard PRIAM interface, apply DC power, select the drive (via the -DRIVE SELECT lines) and issue a Sequence Up command.

If the drive has an SMD interface, apply DC power, select the drive (via the UNIT SELECT lines), then bring PICK and HOLD to the low (true) state.

If the drive has an ANSI interface, apply DC power, select the drive (via the XXXXXXXXXX lines, then .....

If the drive has a BASIC FOUR interface, apply DC power, select the drive (via the UNIT SELECT lines), then bring OPEN CABLE DETECT to the ____ state.

The procedure for powering down .....

3.3 PERFORMANCE CHECK

The following procedures are recommended as an initial check for proper operation of the disc drive:

1. Check the DC voltage levels.

Voltage	J5 pin #	Tolerance
GND	1	N/A
+24 VDC	2	±5% running +5%-15% at spindle startup
-5 VDC	3	±5%
-12 VDC	4	±5%
+5 VDC	5	±5%
GND	6	N/A

2. If any voltages are outside specification, check the corresponding current demands.

Voltage	Maximum Current
-5 VDC	2.0 amperes
+5 VDC	2.0 amperes for 3450 drive amperes for 7050 drive
-12 VDC	0.7 amperes
+24 VDC	4.0 amperes from start of spindle rotation until Ready (30 seconds).
	_____ amperes after Ready.
	_____ amperes after Ready during an active seek operation.

3. Power up the drive, as detailed in the POWERING UP/DOWN section, above. Spindle rotation should begin.

4. Watch for the drive to become Ready. If no faults are detected during the power up sequence, this will take about 30 seconds. If a fault is detected (by the safety circuits within the drive), Ready will be inhibited and a fault condition will be reported. See the STATUS AND ERROR CODES section of the TROUBLE SHOOTING PROCEDURES for details. If, after two minutes, the microprocessor within the drive is unable to sense that the spindle is rotating at the specified speed, Ready will be inhibited and spindle rotation will stop.

5. Check the head positioning operation by issuing seek commands. The following seek pattern is suggested:

   From 000 to 001 to 000 to 002 to 000 to 003 to 000 to 004 to 000 to 005 to 000 ... to maximum cylinder address.

6. Verify that the average seek time complies with the specification. This is done by performing a seek between cylinder 000 and a specified "average" cylinder, and watching for an indication that the seek has been completed. The cylinder number and the maximum time allowed both depend on the disc drive type. The signal line to be monitored depends on the interface type. The following table gives details:

Drive Type	Cylinder #	Seek Time
DISKOS 3450	175	42 msec
DISKOS 7050	350	42 msec

Interface Type	Signal Line Monitored
Standard PRIAM	-READY
SMD	ON CYLINDER
ANSI	
BASIC FOUR	ON CYLINDER

7. Check for proper data transfer operation by writing and then reading data with each read/write head.

   CAUTION: WRITE OPERATIONS ALTER PREVIOUSLY RECORDED DATA

   Most disc systems require a formatted disc before data transfer can be performed.

   A disc surface defect map is supplied by PRIAM with each disc drive. The defect map indicates the location of defects discovered during manufacturing and testing. A defect location is specified by the number of byte positions from the index mark.

SECTION 4 - ASSEMBLIES

4.1 OVERVIEW

PRIAM disc drives are constructed in a modular fashion, so that defective assemblies can be easily replaced. This greatly reduces down time due to servicing. The six assemblies are:

Head Disc Assembly

Photocell Assembly

Servo and Motor Control PCB

Main PCB

Power Supply

Frame Assembly

The exact procedures for removing and replacing these assemblies are described in the ASSEMBLY REPLACEMENT PROCEDURES section.

4.2 HEAD DISC ASSEMBLY

The Head Disc Assembly is a contamination-resistant enclosure. It contains the drive spindle assembly, drive motor, voice coil actuator, head carriage assembly, read/write heads, magnetic disc(s), and air filter assemblies.

4.3 PHOTOCELL ASSEMBLY

The Photocell Assembly contains three infrared light-emitting diodes and phototransistors. Its purpose is to monitor and control spindle motor rotation.

4.4 SERVO AND MOTOR CONTROL PCB

The Servo and Motor Control PCB contains the circuitry associated with driving the spindle motor. This circuitry receives an On/Off command from the Main PCB, and spindle rotation feedback from the Photocell Assembly.

The Servo and Motor Control PCB also contains the circuitry used for processing the servo signals from the servo read head, and for controlling the position of the head carriage.

4.5 MAIN PCB

The main PCB contains all the circuitry associated with read/write control, command execution, and infomation transfers across the user interface.

4.6 POWER SUPPLY

The PRIAM power supply can operate from 50 or 60 Hz, with input voltage (selectable) of 100, 120, 220, or 240 VAC.

A power supply cable is available for those users who provide their own power supplies.

The power supply must be mounted separately from the disc drive. It will not fit within the frame assembly.

4.7 FRAME ASSEMBLY

The Frame Assembly is constructed to accomodate all of the standard and (PRIAM-built) optional assemblies of the disc drive. Its open steel rod and sheet metal design provides improved air circulation, and also makes the drive lighter, lower in cost, and easier to install.

SECTION 7 - TROUBLESHOOTING PROCEDURES

The overall purpose of field service for PRIAM disc drives is to restore system operation by the quickest and most economical means possible. This usually boils down to the replacement of a faulty or suspected assembly with an operational spare. The assembly in question may then be returned to a PRIAM repair depot for component level diagnosis and repair.

Requests for maintenance assistance may be directed to PRIAM's Customer Service Department. PRIAM offers the following services:

1. Telephone Assistance: Service representatives are available (during PRIAM's normal working hours) to assist customers with maintenance, interfacing, and spare parts inquiries.
2. On-site Assistance: PRIAM can provide a factory trained technician to assist the customer's system technician in the testing and repair of PRIAM products.
3. Factory Repair: PRIAM maintains a repair facility at its factory for the convenience of its customers. An entire disc drive, or any repairable assembly, may be returned to PRIAM for repair. Contact PRIAM Customer Service for a return authorization number prior to shipping any drive or assembly to PRIAM.

7.1 FIELD ADJUSTMENTS AND PREVENTIVE MAINTENANCE

PRIAM 8-inch disc drives require no field adjustments and no preventive maintenance.

7.2 GENERAL INSPECTION

The following checklist may be used as a preliminary procedure to be performed whenever a disc drive is suspected of being faulty:

1. Check that the spindle and head carriage lock lever is in the UNLOCK position.
2. Check for proper DC voltages within the disc drive, as described in the OPERATING PROCEDURES section.
3. Check the fuse in the power supply.
4. Check the fuse in the servo and motor control PCB.
5. Check that the device address, write protect, and sector size switches are correctly set, according to the information given in the INSTALLATION section.
6. Check for component discoloration, and for loose or faulty connections.
7. Check and recheck all cable and controller connectors.

If all of the above items seem to be in order, a kind of high-level trouble shooting can be performed, simply by replacing each of the major assemblies one-by-one until the problem disappears. This obviously works best on problems that are stable, as opposed to intermittent. Replacement of the main PCB will confirm the operation of approximately 85% of the electronic circuits in the entire disc drive.

A more symptom-specific approach to troubleshooting is described below in the SYMPTOMS AND CAUSES section.

7.3 STATUS AND ERROR CODES

The disc drive is capable of providing quite a bit of information concerning its internal conditions, by means of status indications on the user interface. The exact information available, and the signal lines involved depend on the specific interface used. This is discussed further in the sections describing each individual interface. See also the section on SEEK ERRORS AND FAULT CONDITIONS (below).

7.4 SYMPTOMS AND CAUSES

The functions performed by the disc drive fall into the following five categories:

1. Spindle Rotation
2. Command/Status Transfer
3. Head Positioning/Servo
4. Data Write Operations
5. Data Read Operations

In the pages immediately following, symptoms are listed from each of these categories, along with possible causes and the corresponding suggested courses of action.

SPINDLE ROTATION

Symptom	Possible Cause	Suggested Action
Rotation does not start.	Spindle locked.	Place in UNLOCK position.
	Incorrect or zero voltage at main PCB connector J4.	Check power supply.
	+OFF signal (J4-4) is +5 VDC (should be 0 volts for rotation).	Check microprocessor reset signal on main PCB. Check power-on reset (POR). Check power reset (PRST). All these should be false.
	Defective motor control circuitry.	Check the fuse in the servo and motor control PCB. Check the LED voltage at J1-5 for the following: ____VDC on the 3450 ____VDC on the 7050
	Defective photocell assembly.	Check for open LED, defective connector or phototransistor.
	Defective spindle motor.	Manually rotate spindle in clockwise (viewed from bottom) direction only. If motor is binding, replace entire disc drive. Depot repair is required.
Spindle rotates, but stops after about one minute.	Head carriage locked.	Place in UNLOCK position.
	Defective motor control circuitry.	Replace servo and motor control PCB.
	Defective photocell assembly.	Replace photocell assembly.
	Speed control not being sensed by microprocessor.	Replace main PCB.
	Spindle motor has excessive drag.	Replace entire disc drive (depot repair required).

SPINDLE ROTATION (continued)

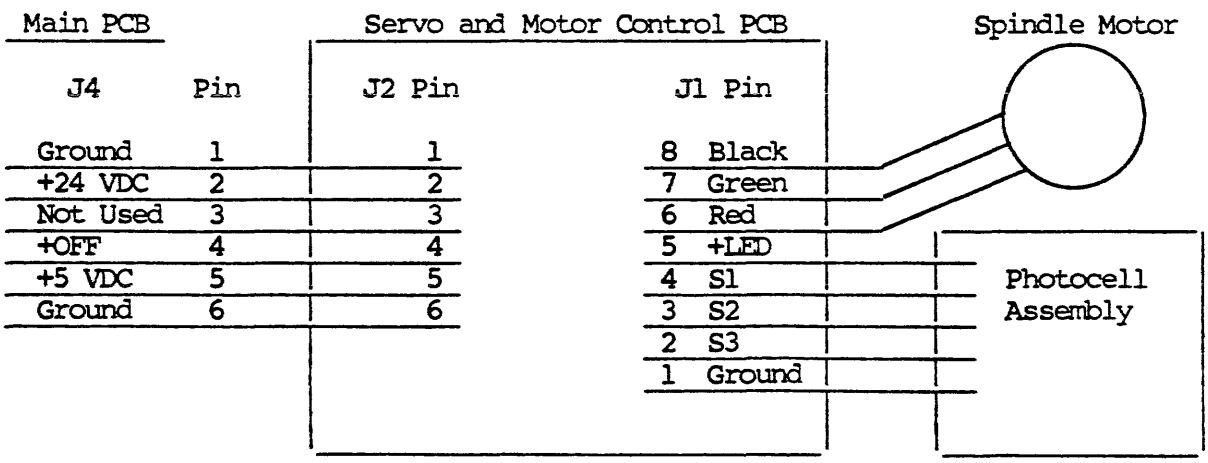
Symptom	Possible Cause	Suggested Action
Spindle rotates, but drive does not come Ready, or Ready comes and goes.	Fault condition.	Check Fault status.
	Intermittent power supply failure.	Replace power supply.
	Defective main PCB.	Replace main PCB.
	Defective motor control circuitry.	Replace servo and motor control PCB.
	Defective head disc assembly.	Replace entire disc drive (depot repair required).

Comments: Upon completion of power on reset (POR) the microprocessor disables the +OFF signal to the spindle motor. With +OFF at 0 volts the spindle motor should rotate at its specified speed (3600 RPM).

The microprocessor examines Index Marks to determine spindle speed. If the specified spindle speed is not reached within two minutes, the +OFF signal is enabled and spindle rotation is stopped.

Power to the disc drive must be cycled (off and then on) to allow the microprocessor to disable the +OFF signal.

The following diagram shows the connections among the main PCB, servo and motor control PCB, spindle motor, and photocell assembly.



COMMAND/STATUS TRANSFER

Symptom	Possible Cause	Suggested Action
Incorrect state on Unit Selected.	Wrong setting on device address switch.	Refer to Section 2.4 for correct switch settings.
	Pick and Hold false or Open Cable Detect true.	Check controller, cable, and connectors.
	Unit Select Tag or Unit Address missing or mistimed.	Check controller, cable, and connectors.
Selected drive does not issue status.	Drive not Ready.	See SPINDLE ROTATION (above).
	Fault condition.	See FAULT CONDITIONS section (below).
	Defective main PCB.	Replace main PCB.
Selected drive does not accept commands.	Tag and bus data malfunction.	Check controller, cable, and connectors.
Selected drive issues Fault.	Fault condition.	See FAULT CONDITIONS section (below).
Selected drive issues Seek Error.	Defective servo operation.	See HEAD POSITIONING/SERVO (below).
Selected drive fails to issue Index.	Defective main PCB.	Replace main PCB.

Comments: During servo and data write operations, most circuit functions are monitored by the microprocessor. If Ready is true and Fault is false, it is likely that the spindle speed, servo, and data write circuitry are all funtioning in a normal manner.

HEAD POSITIONING/SERVO

Symptom	Possible Cause	Suggested Action
Drive fails to move to new address.	Command transfer circuitry defect.	See COMMAND/STATUS TRANSFER (above).
Continuous Seek Error condition.	Defective circuitry.	Defective servo circuitry on servo and motor control PCB. If fault persists with operational spare, and the fault is not in the spindle speed circuitry, replace the entire disc drive.
	Faulty connection to servo read head.	Check connector J4.
	Faulty connection to voice coil actuator.	Check connector J5.
	Incorrect power voltage.	Check connector J3. Refer to Section 3 for correct voltages.
	Head carriage locked.	Place in UNLOCK position.
Drive seeks to wrong cylinder.	Inadequate signal from controller.	Check controller, cable, and connectors.
	Defective circuitry or servo system.	Defective circuitry on servo and motor control PCB. If the symptom persists with operational spare, and the fault is not in the controller or cable, replace the entire disc drive.

Comments: Note that the seek operation may be normal, while the circuitry that checks for correct seek location may be defective.

A large number of symptoms may be associated with malfunctions of the servo circuitry. If servo malfunction is suspected, the recommended procedure is to replace the servo and motor control PCB. If the head disc assembly is defective, it is highly likely that non-servo related faults (e.g., data errors, failure to come Ready, Fault status true) will also be in evidence.

DATA WRITE OPERATIONS

Symptom	Possible Cause	Suggested Action
Fault is set with each attempt to write data.	Incorrect switch setting or circuit defect.	Verify whether multiple heads have been selected. If this is the case, the following test point will be high: TP__ on the 3450 TP__ on the 7050 Check TP__ for the Act Unsafe condition. TP__ will be high if there are write transitions with Write Gate false, or no write transitions with Write Gate true. See the section on SEEK ERRORS AND FAULT CONDITIONS for other possibilities and corresponding suggested actions.
Data is written incorrectly and Fault does not set.	Difficulty in data read operation.	See DATA READ OPERATIONS (below).

DATA READ OPERATIONS

Symptom	Possible Cause	Suggested Action
Drive fails to read, but will write without a Fault.	Defect in read circuitry.	Check all cable connections. Replace terminator. Replace main PCB.
Drive reads data fields and header fields correctly, but will not read newly written data.	Difficulty in data write operation.	See DATA WRITE OPERATIONS (above). If Fault is set during write operation, see the section on SEEK ERRORS AND FAULT CONDITIONS.

Comments: If read errors persist after replacement of the terminator and the main PCB, and if the cable connections are correct, it is possible that the format being used is erroneous.

If the format is correct, replacement of the entire disc drive is recommended.

7.5 SEEK ERRORS AND FAULT CONDITIONS

Seek errors result when a head does not reach the correct track (which can be verified by reading a recorded track address). Whenever a seek error occurs, the drive's track counter must be reset to zero by issuing a Restore command or Rezero command to the drive. This will cause the head to move back to cylinder 000. A new seek command may then be issued.

The Seek Error indication will be set true whenever the microprocessor detects any of the following conditions:

1. Seek Incomplete (track following servo unable to lock onto track within the prescribed time).
2. Restore or Rezero not completed within the prescribed time.
3. Invalid seek address detected.
4. Guardband Error (servo head has entered the guardband area).

When the microprocessor detects one of these conditions, it issues an internal Restore or Rezero command, which returns the head to cylinder 000 and sets a Seek Error Latch. The Seek Error Latch must be cleared by a Restore or Rezero command issued to the drive by the user.

The exact manner in which the Seek Error indication appears on the user interface depends on which interface option is present. See the individual interface description sections for details.

Fault status is set, Ready is disabled, and writing of data is inhibited whenever the safety circuitry on the main PCB detects a Fault conditon. The following list discusses the possible origins of such a conditon, and suggests what remedial actions could be taken in each case:

1. Write Gate true with Write Protect switch ON (or Write Enable switch OFF).

   Check switch for correct setting.

2. Act Unsafe (Write gate without Write Current or Write Current without Write Gate).

   If the fault is isolated to an individual head, then (with power off) check the head assembly for continuity. If the head assembly is faulty, return the entire disc drive to a repair depot.

   If the fault occurs on all heads, replace the main PCB.

3. Multiple heads selected (only one data head should be selected at a given time).

   Check the center tap of each data head. Only one data head should have +7 VDC.

   If more than one data head center tap is at +7 VDC, replace the main PCB.

4. Write Gate and Read Gate both true at the same time.

   Check the controller for proper operation and the interface cable for the proper connections.

   If the problem persists, replace the main PCB.

5. Write Gate true, but heads not precisely located over the designated cylinder.

   Replace the servo and motor control PCB.

   If the problem persists, replace the entire disc drive.

6. No seek request, but head movement is detected.

   Replace the servo and motor control PCB.

   If the problem persists, replace the entire disc drive.

7. The PLO signal is not synchronized.

   Replace the servo and motor control PCB.

   If the problem persists, replace the entire disc drive.

8. Spindle rotation is outside of specification.

   Check the servo and motor control PCB for a defective component.

   Check the photocell assembly for a defective connection, LED, or phototransistor.

   Check the power supply for a defective connection, DC voltage level, or component.

   If the fault can not be corrected by replacing the servo and motor control PCB, photocell assembly, and power supply, then replace the entire disc drive.

9. More than one control tag is active.

   Check controller, cable, and procedures.

   If the problem persists, replace the main PCB.

If any of conditions 6, 7, or 8 (above) are detected, the microprocessor will initiate a restore to cylinder 000.

Any of the following measures will reset Fault status:

1. Power On Reset -- remove and reapply DC power.
2. Fault Clear -- Tag 3 and Bit 4 on interface "A" or BUS cable.
3. Fault Reset command.
3. Ground potential at J_-_.

SECTION 8 - ASSEMBLY REPLACEMENT PROCEDURES

All of the replaceable assemblies in a PRIAM disc drive may be removed and replaced using standard hand tools. It is highly recommended that maintenance personnel use the assembly replacement approach to field service, rather than attempting component level repair.

8.1 PRECAUTIONS

1. Always make sure that the head and spindle lock lever is in the LOCK position before the drive is moved in any way.
2. Always make sure that the power is off when removing or reinserting any printed circuit boards or connectors.
3. Use proper size screwdrivers, wrenches, and other tools. Keep track of the screws and other parts you remove, and use the same hardware when reinstalling each assembly.
4. Use properly calibrated test equipment.
5. Keep accurate records of all observations made during servicing.

Before attempting to remove any assemblies, make sure that the head and spindle lock lever is in the LOCK position. This lock is a wire lever, which should be pulled out, then turned to the LOCK position. If it does not turn easily, gently lift the far end of the drive so that the head carriage will return to the fully retracted position. The turn the lever to LOCK.

8.2 HEAD DISC ASSEMBLY

The head disc assembly (HDA) is a sealed contamination-resistant enclosure containing all moving parts in the disc drive. It should not be opened for any reason. If the HDA is defective, the entire disc drive should be returned to a qualified repair depot. Do not remove the HDA from the frame assembly.

8.3 PHOTOCELL ASSEMBLY

The photocell assembly is mounted on the bottom of the motor spindle. To remove the photocell assembly, first unplug the connector at the servo and motor control PCB. Then remove the two mounting screws, which can be accessed through the holes provided in the perforated cover over the bottom of the spindle. When you install the replacement board, be sure to locate the LEDs in exactly the same location relative to the shutters.

8.4 SERVO AND MOTOR CONTROL PCB

The servo and motor control PCB is mounted on the bottom of the frame. To remove the servo and motor control PCB, first unplug the five connectors. Then remove the _____ mounting bolts and release the ___ plastic retainers.

Extreme care should be taken in removing the IC connectors, especially those going to the head disc assembly. Gently pry the connectors off, using a suitable size slender screwdriver. If the connectors to the HDA are broken, it will be necessary to replace the entire HDA.

8.5 MAIN PCB

The main PCB is mounted on the top of the frame. To remove it, first unplug all the connectors, carefully noting their positions and orientations for later replacement. Then remove the _____ mounting screws.

Extreme care should be taken in removing the IC connectors, especially those going to the head disc assembly. Gently pry the connectors off, using a suitable size slender screwdriver. If the connectors to the HDA are broken, it will be necessary to replace the entire HDA.

8.6 POWER SUPPLY

The power supply must be mounted separately from the disc drive. To remove the power supply, simply unplug the power connector.

SECTION 9 - SPARE PARTS LIST

Replaceable assembly part numbers are given below. Additonal part number information (and/or a bill of material listing for customers establishing depot repair) is available from PRIAM Customer Service.

Head Disc Assembly (3450)
Head Disc Assembly (7050)

Photocell Assembly

Servo and Motor Control PCB

Main PCB (PRIAM Interface)
Main PCB (SMD Interface Adapter)
Main PCB (ANSI Interface Adapter)
Main PCB (Basic Four Interface Adapter)

Frame Assembly

Power Supply (3450)
Power Supply (7050)

Power Cord

Terminator (PRIAM Interface)
Terminator (SMD Interface Adapter)
Terminator (ANSI Interface Adapter)
Terminator (Basic Four Interface Adapter)

Orders for spare parts may be placed with your PRIAM Sales Representive or with PRIAM Customer Service at the factory.

SECTION 10 - PRIAM INTERFACE

10.1 OVERVIEW

PRIAM offers a basic 8-bit bidirectional bus control interface designed to be readily connected to popular 8-bit and 16-bit microprocessors. Across this interface all spindle motor and head positioning controls are passed.

Read and Write Data is passed via synchronous serial-bit NRZ signal lines. The interface provides INDEX, SECTOR MARK, READ/REFERENCE CLOCK, and WRITE CLOCK signals.

Up to four drives may be daisy chained along a single 50 conductor flat ribbon cable. Power is provided via a separate connector. Control switches and a Remote Panel Connector are provided on the PCB.

10.2 CONNECTORS AND PIN ASSIGNMENTS

All drive signal connections are made via a single 50-pin ribbon cable connector. A second 50-pin connector is available for daisy chaining to another drive or for a terminator for the last drive in the string. Up to four drives may be daisy chained.

A separate connector for DC power is provided. However, if the PRIAM optional power supply is ~~installed~~ used, then its output is connected to this DC power connector and AC power must be supplied to the optional power supply.

Mini-dip type switches are provided on the PCB to select drive address, sector length, write protect functions and write clock control.

A dip socket output for remote write protect control and drive status is also provided on the PCB.

1. Interface Connectors

   The interface connectors are 50-pin ribbon cable connectors and provide for interface cable and terminator connections. The pins are numbered 1 through 50. A recommended mating connector is Spectra-Strip 802-050-004 or Scotchflex 3425-0000. The lines are described at the drive end in Table 2.

TABLE 2 - Interface Connectors

Pin	Signal	Line Type
1	Ground	Ground
2	+ DBUS 0	Bi-Dir/Single
3	+ DBUS 1	Bi-Dir/Single
4	+ DBUS 2	Bi-Dir/Single
5	+ DBUS 3	Bi-Dir/Single
6	+ DBUS 4	Bi-Dir/Single
7	+ DBUS 5	Bi-Dir/Single
8	+ DBUS 6	Bi-Dir/Single
9	+ DBUS 7	Bi-Dir/Single
10	Ground	Ground
11	- READ GATE	Received/Single
12	Ground	GND
13	- RESET	Received/Single
14	Ground	GND
15	- WRITE GATE	Received/Single
16	Ground	GND
17	- RD	Received/Single
18	- WR	Received/Single
19	+ AD 1	Received/Single
20	+ AD 0	Received/Single
21	Ground	GND
22	- DRIVE SELECT 1	Received/Single
23	- DRIVE SELECT 2	Received/Single
24	- DRIVE SELECT 3	Received/Single
25	- DRIVE SELECT 4	Received/Single
26	Ground	Ground
27	Ground	Ground
28	+ 5 VOLTS DC (TERMINATOR POWER)	Diode or'd/Single
29	- HEAD SELECT 4	Received/Single
30	- HEAD SELECT 2	Received/Single
31	- HEAD SELECT 1	Received/Single
32	Ground	GND
33	- INDEX	Transmitted/Single
34	Ground	GND
35	- READY	Transmitted/Single
36	Ground	GND
37	- SECTOR MARK	Transmitted/Single
38	Ground	GND
39	+ WRITE DATA	Received/DIFF
40	- WRITE DATA	Received/DIFF
41	Ground	GND
42	+ WRITE CLOCK	Received or Transmitted/DIFF
43	- WRITE CLOCK	Received or Transmitted/DIFF
44	Ground	GND
45	+ READ/REFERENCE CLOCK	Received or Transmitted/DIFF
46	- READ/REFERENCE CLOCK	Received or Transmitted/DIFF
47	Ground	GND
48	+ READ DATA	Transmitted/DIFF
49	- READ DATA	Transmitted/DIFF
50	Ground	GND

2. DC Power Connector

This connector is used to supply DC power to the drive which mates to the optional power supply. It is a 6-pin AMP MATE-N-LOK Connector, and the recommended mating connector is an AMP 1-480270-0 socket using AMP 60619-1 pins.

DC POWER CONNECTOR

PIN	VOLTAGE
1	GND
2	-5 VDC
3	+5 VDC
4	GND
5	-12 VDC
6	+24 VDC

3. AC Power Connector

This is a 3-pin connector used to supply AC power to the drive when the optional power supply is used. The mating connector is Belden 5PH-386 or equivalent.

AC POWER CONNECTOR

PIN	VOLTAGE
L	110 or 220 VAC (HOT)
E	FRAME GROUND
N	110 or 220 VAC (COMMON)

10.3 INTERFACE SIGNAL DESCRIPTIONS

This section gives functional descriptions for the signals on the 50-pin interface connector. Details on how to transmit and receive these signals are given in Section 10.4.

1. +DBUS 0-7

   A high active 8-bit wide bus is used to transfer commands and status (carriage control and interface) between drive and controller. These lines connect directly to an 8304B (or 8286) bus transceiver as shown in Figure 4. DC Characteristics are shown in Table 3.

   If long cables are used, these lines should be terminated at each end.

2. + AD0-1

   A high active 2-bit wide address bus, whose function is to select one of three registers in which data is stored or from which it is read. These lines connect directly to a 74LS244 Schmitt-Triggered Receiver enabled by DRIVE SELECTED as shown in Figure 5. The DC Characteristics are shown in Table 4.

   If long cables are used, these lines should be terminated at the drive end. PRIAM provides an optional terminator.

3. - RD

   This low active signal is used to gate the contents of the selected register (decode of AD1,AD0) onto the DBUS. This line is connected to a 74LS244 as shown in Figure 5. Also, the DC characteristics are listed in Table 4.

   Long cables should be terminated at the drive end. PRIAM provides an optional terminator (Figure 7).

4. - WR

   This low active signal is used to gate the contents of the DBUS into the selected register. This line is connected to a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4.

   Long cables should be terminated at the drive end. PRIAM provides an optional terminator (Figure 5).

5. - RESET

This low active signal resets the drive logic. If the drive is sequenced down when RESET occurs it will remain sequenced down. If the drive is sequenced up, it will remain up and the carriage will RESTORE to Cylinder Zero. This line is connected to a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4.

Long cables should be terminated at the drive (Figure 5).

6. - DRIVE SELECT 1-4

These low active signals enable drive response. No reading, writing, register selection, or command response will occur unless the drive is selected. These single-ended receiver lines are shown in Figure 6. Long cables should be terminated (Figure 6). DC Characteristics are shown in Table 5.

7. -HEAD SELECT 1-2,4 (gated by -DRIVE SELECT 1-4)

These low active signals are used to select the desired head for reading or writing. The head selection decoding is shown in Table 16. These lines are connected to a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4.

Long cable connections should be terminated (Figure 5).

8. -READY

This low active signal from the drive indicates that it is up to speed and ready to read, write or seek. It is driven by a 75462 open collector driver as shown in Figure 7. DC characteristics are shown in Table 6.

9. -INDEX

This low active signal occurs once per revolution and indicates the beginning of a track. It is driven by a 75462 open collector driver as shown in Figure 7 and has the DC characteristics listed in Table 6. This line must be terminated at the controller.

10. -SECTOR MARK

This low active signal indicates the beginning of a sector. It is driven by a 75462 open collector driver as shown in Figure 7 and has the DC characteristics listed in Table 6. This line must be terminated at the controller.

11. -WRITE GATE

This low active signal enables the writing of data by the selected head. This signal is received by a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4. Long cable connections should be terminated at the drive (Figure 5).

12. -READ GATE

This low active signal initiates synchronization of the drive's phase lock loop for data separation. READ GATE must be enabled during a gap. This signal is received by a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4. Long cable connections should be terminated at the drive (Figure 5).

13. +, - WRITE DATA

WRITE DATA is an NRZ serial data signal synchronous with WRITE CLOCK. It is received by a RS422 type differential line receiver section as shown in Figure 8.

14. +, - WRITE CLOCK

This signal is switch selectable and may be either a square wave signal from the controller which is phase locked to the WRITE DATA. Or, if the switch is set in the other position, WRITE CLOCK is a square wave signal from the drive to the controller to provide clocking and synchronization for WRITE DATA. The controller should be designed so that WRITE DATA is stable at the drive connector during the ~~positive~~ negative transition of WRITE CLOCK. It is received by a RS422 type differential line receiver as shown in Table 7 and Figure 8. These lines should be terminated. If long cables are used, cable delays must be considered.

15. +, - READ/REFERENCE CLOCK

This square wave signal provides clocking and synchronization for reading and writing data. It is derived from either the servo clock or the VFO synchronized to the READ DATA signal. It is driven by an RS442 type differential line driver as shown in Figure 8 and its DC characteristics are listed in Table 8.

16. +, - READ DATA

This serial NRZ signal is used to transmit data from the drive to the controller. This output is valid 9 microseconds after READ GATE is enabled. It is driven by a RS422 type differential line driver as shown in Figure 8 and its DC characteristics are listed in Table 8.

Of the above signals, there are several that are used specifically to facilitate serial data transfer between the disc drive and the controller. These are described below, with some additional details.

1. INDEX

The INDEX pulse occurs whenever the servo track index mark is encountered, to indicate the beginning of a track.

2. READY

The READY signal indicates that the selected drive is ready to read, write, or seek. When READY is false, the controller should not initiate WRITE, READ, or SEEK commands. However, READY will go false when a SEEK command is initiated. READY will later go true when the head carriage is positioned on the specified cylinder, if no fault conditon exists.

3. SECTOR MARK

The SECTOR MARK pulse occurs at the beginning of each sector (sector size is selectable by setting the mini-switches on the main PCB).

4. HEAD SELECT 1, HEAD SELECT 2, and HEAD SELECT 4

These low active signals are gated by drive select and are used to select the head as defined in Table 16.

TABLE 16 - Head Selection

Head Sel 1	Head Sel 2	Head Sel 4	Selected Head 7050 / 3450
High	High	High	Zero
Low	High	High	One
High	Lo	High	Two
Low	Low	High	Three
High	High	Low	Four
Low	High	Low	Zero*
High	Low	Low	Zero*
Low	Low	Low	Zero*

* Selected by default because of head select range/heads available.

5. WRITE GATE

WRITE GATE enables data to be written on the disc when in the active state. READY must be valid before signaling WRITE GATE. An attempt to write between INDEX and the first SECTOR MARK will result in a DRIVE FAULT because the prerecorded skip defect information is write protected. DRIVE FAULT will be set if any of the following error conditions occur during writing.

TABLE 17 - Drive Fault Conditions

1 - WRITE GATE without write current at the head
2 - Write current at the head without WRITE GATE
3 - WRITE GATE without READY
4 - More than one head selected
5 - No transitions during write
6 - WRITE GATE with WRITE PROTECT
7 - Spindle Speed Error
8 - RESET while drive Sequenced Up
9 - Off-Track condition when track following (READY)
10 - Failure to Restore
11 - Software Error (Watch-dog timer time out).

6. WRITE CLOCK

Provides clocking and synchronization for WRITE DATA. WRITE CLOCK is generated by the controller by echoing the REFERENCE CLOCK signal back to the drive through a similar delay path. Thus, it is at the same frequency and with a phase delay similiar to WRITE DATA. The timing of these signals is shown in the timing section.

7. WRITE DATA

Provides the data to be stored on the track. The required format is NRZ (non-return to zero). READ/REFERENCE CLOCK (received from the drive) is used by the controller to clock WRITE DATA on the positive edge. READ/REFERENCE CLOCK is retransmitted back to the drive as WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe WRITE DATA into the drive's encoder circuitry. Detailed timing diagrams are shown in the timing section.

8. READ GATE

This signal must be enabled in a gap area (all 0's recorded) and at least 9 microseconds before the sync byte. READ GATE enables the VFO clock to synchronize with the information from the read head. Raising READ GATE during a data record may cause the VFO to spuriously lock in incorrect phase relationship for correct decoding of recorded information.

Six microseconds after the leading edge of READ GATE the READ CLOCK is selected for the READ/REFERENCE CLOCK signals.

9. READ/REFERENCE CLOCK

Provides clocking and synchronization for reading and writing data. When READ GATE is not active this signal is the REFERENCE CLOCK which is derived from the servo track information.

Six microseconds after the leading edge of READ GATE, READ/REFERENCE CLOCK is switched to the VFO clock which is phase locked to READ DATA. A change in the READ/REFERENCE CLOCK phase will occur when it is switched between the servo and VFO clocks.

10. READ DATA

Data from the drive are in serial bits NRZ (non-return to zero) form and are synchronized with READ/REFERENCE CLOCK after a six microsecond delay from the leading edge of READ GATE. READ DATA may not be valid for the first 9 microseconds after READ GATE is enabled.

10.4 INTERFACE DC CHARACTERISTICS

This section, through tables and figures, sets forth the details that need to be observed, in order to properly transmit and receive the interface signals listed in Section 10.2 and described in Section 10.3.

TABLE 3 - DBUS DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OL}	Output Low Level		0.5	V	I_{OL} = 32 MA
V_{OH}	Output High Level	2.4		V	I_{OH} = -5 MA
I_{OFF}	Output Off Current		-0.2	mA	V_{OFF} = 0.45 V
			+0.2	mA	V_{OFF} = 5.25 V
V_{IL}	Input Low Level		0.9	V	
V_{IH}	Input High Level	2.0		V	

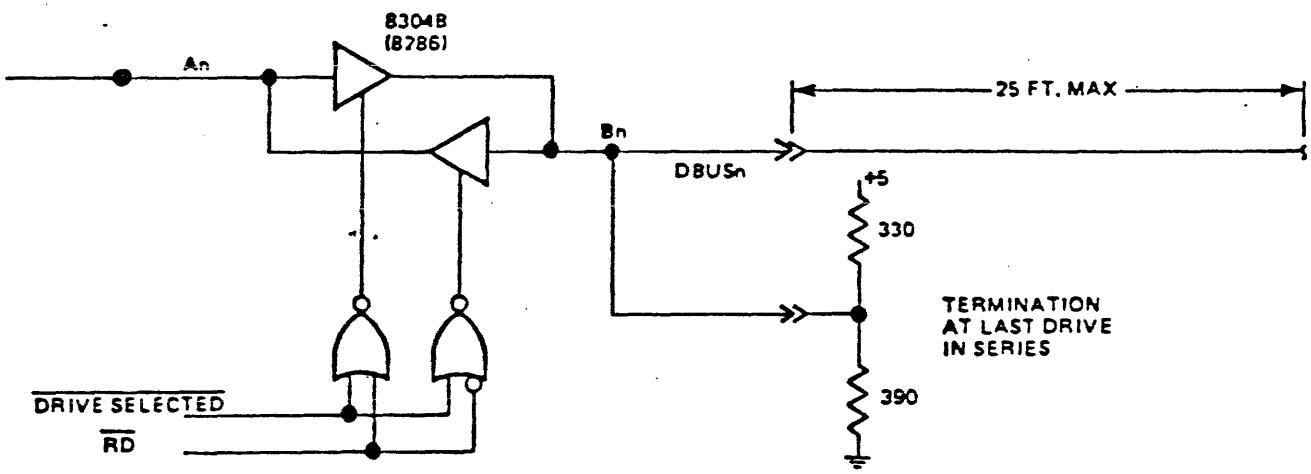


Figure 4 - DBUS Transceiver

TABLE 4 - Single End Line Receiver Gated by Drive Select
DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input High Level	2		V	
V_{IL}	Input Low Level		0.8	V	
I_{IH}	High Level Input Current		0.02	mA	V_I = 2.7V
I_{IL}	Low Level Input Current		-0.2	mA	V_I = 0.4V

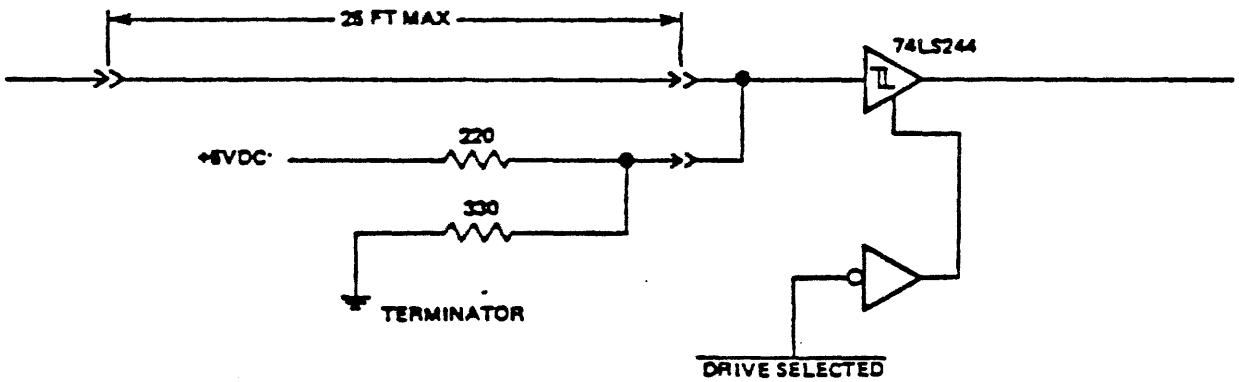


Figure 5 - Single End Line Receiver Gated By Drive Select

TABLE 5 - Single End Line Receiver DC Characterisitcs

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{T+}	Positive-going threshold	1.4	1.9	V	
V_{T-}	Negative-going threshold	0.5	1	V	
I_{IH}	High level input current		.020	mA	V_I = 2.7V
I_{IL}	Low level input current		-0.400	mA	V_I = 0.4V

Long cable connections should be terminated at the drive.

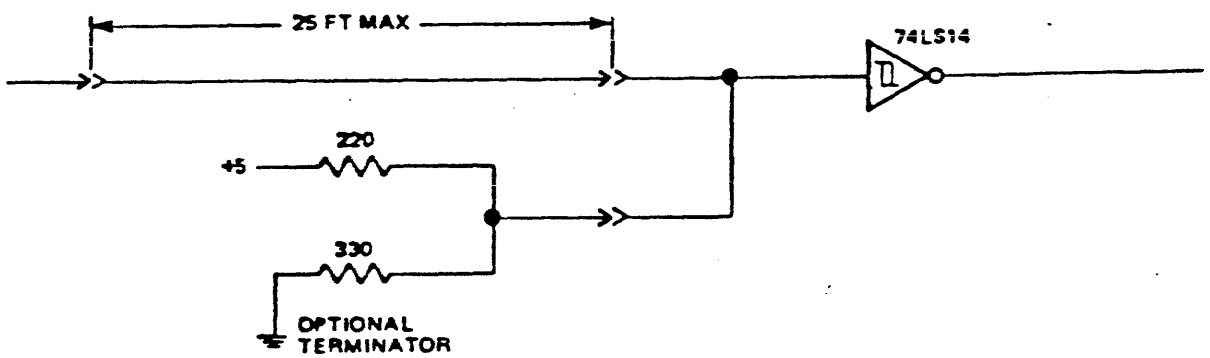


Figure 6 - Single End Line Receiver

TABLE 6 - Single End Line Driver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{OH}	High level output current		0.10	mA	
I_{OL}	Low level output current	300		mA	
V_{OL}	Low level output voltage		0.8	V	I_{OL} = 300mA

This line must be terminated at the controller.

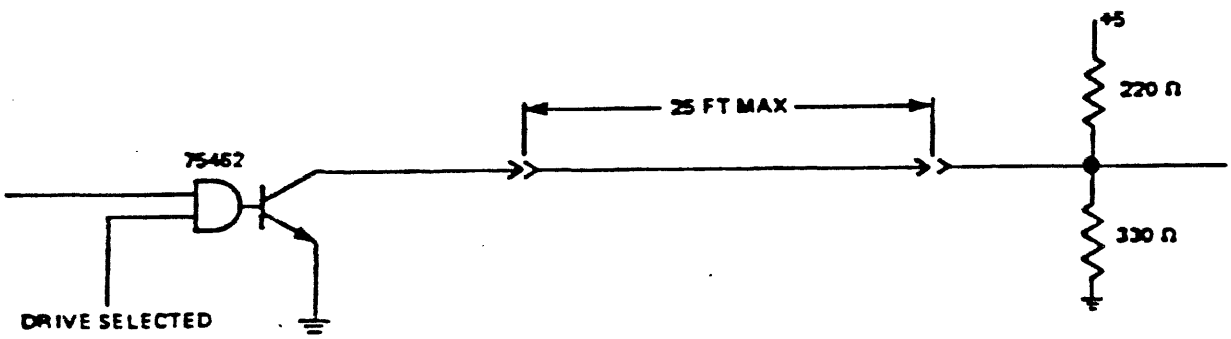


Figure 7 - Single End Line Driver

TABLE 7 - Differential Line Receiver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{TH}	Differential input high-threshold		0.2	V	
V_{ICR}	Common-mode input range	+15 to -15		V	
$I_{I(REC)}$	Receiver input current		2.3	mA	

TABLE 8 - Differential Line Driver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}	High level output voltage	2.5		V	I_{OH} = -20mA
V_{OL}	Low level output voltage		0.32	V	I_{OL} = 20mA
I_{OZ}	Off-state (non-selected) output current		±0.02	mA	
I_{OH}	High-level output current		-20	mA	
I_{OL}	Low-level output current		20	mA	
I_{OS}	Short circuit output current	-30	-150	mA	

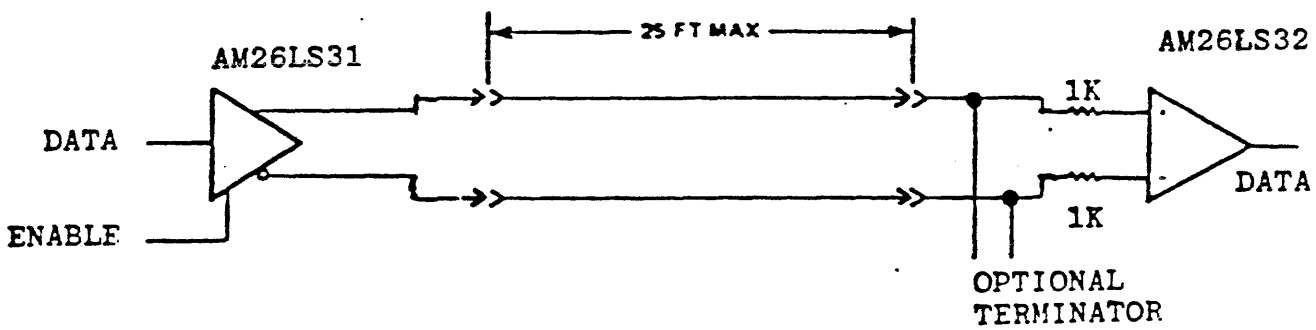


Figure 8 - Differential Line Drivers & Receivers

The DC characteristics are listed in Table 7 and 8. The last drive in a string should be terminated with P/N 200028.

10.5 INTERFACE TIMING

This section discusses the timing requirements for the various operations performed on the controller interface.

1. REGISTER TIMING

Register load timing is shown in Figure 9 and the AC characteristics are listed in Table 18.

TABLE 18 - Register Load AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{AW}	Address stable before WR	60		ns
t_{WA}	Address hold time for WR	30		ns
t_{WW}	WR pulse width	100		ns
t_{DW}	Data set up time for WR	60		ns
t_{WD}	Data hold time for WR	30		ns
t_{RV}	Recovery time between WR	200		ns

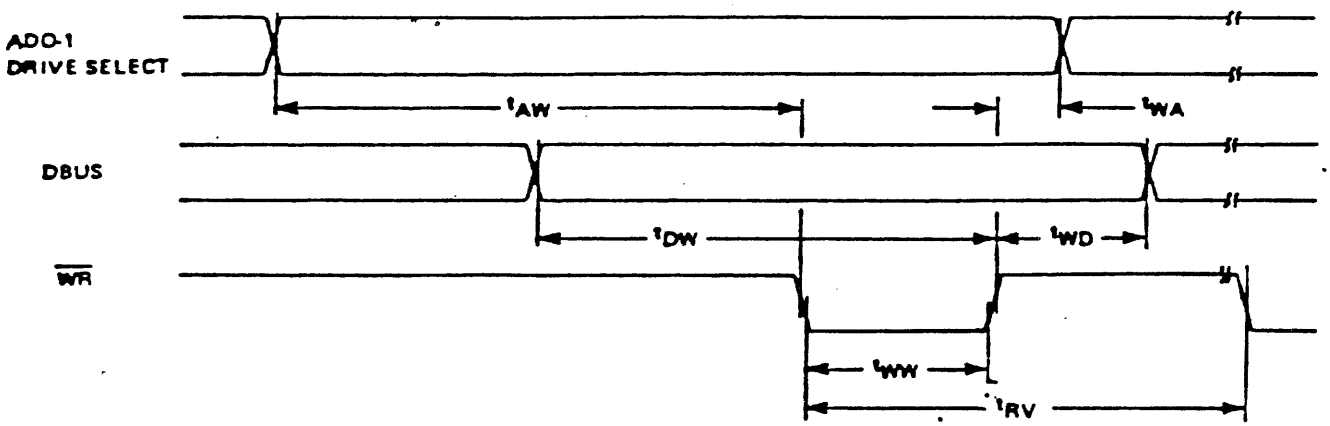


Figure 9 - Register Load Timing

Register read timing is shown in Figure 10 and the AC characteristics are listed in Table 19.

TABLE 19 - Register Read AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{AR}	Address stable before RD	60		ns
t_{RA}	Address hold time for RD	30		ns
t_{RR}	RD pulse width	100		ns
t_{RD}	Data delay from RD		60	ns
t_{DF}	RD to data floating	10	40	ns

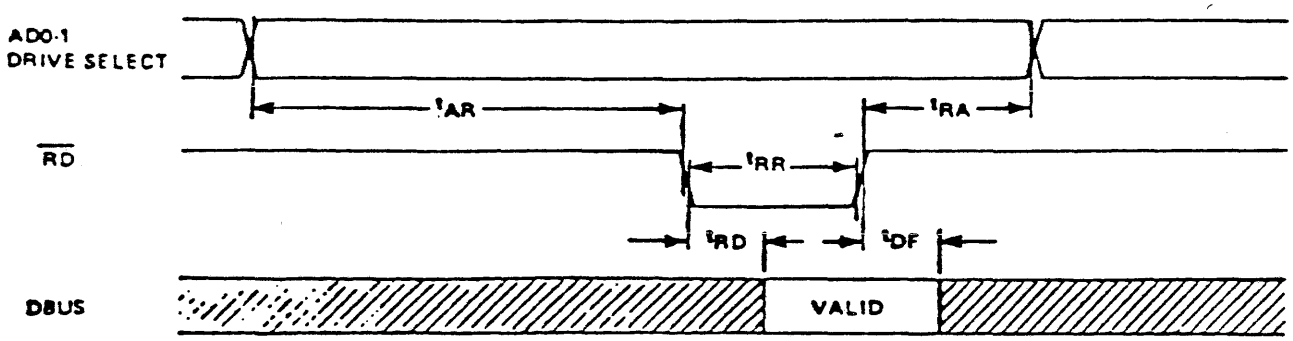


Figure 10 - Register Read Timing

2. RESET TIMING

RESET timing is shown in Figure 11 and the AC characteristics are listed in Table 20.

TABLE 20 - Reset AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{RST}	Reset pulse width	100		ms
t_{SR}	DRIVE SELECT to RESET	0		ns

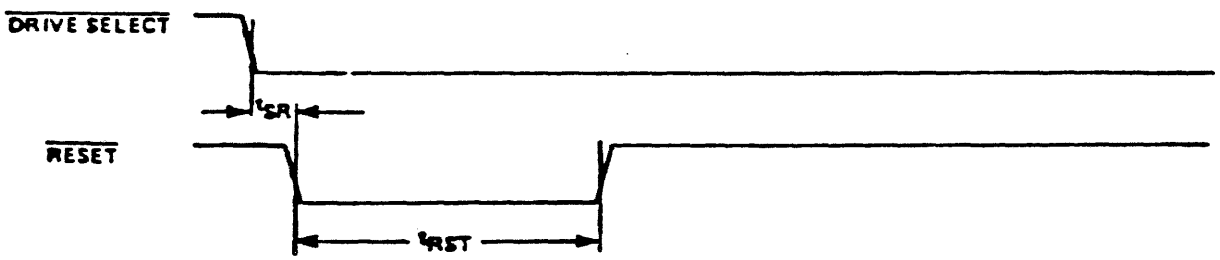


Figure 11 - Reset Pulse Width Timing

3. INDEX SECTOR MARK TIMING

INDEX and SECTOR MARK timings are shown in Figure 12 and their AC characteristics are listed in Table 21.

TABLE 21 - Index and Sector Mark AC Characteristics

Symbol	Parameter	Timing 3450 & 7050	Units
t_{IW}	INDEX Pulse Width	2.48±.25	us
t_{IR}	INDEX Period	16.67±.4	ms
t_{SW}	SECTOR MARK Pulse Width	1240±160	ns
t_{IS}	INDEX to First SECTOR	44.6±1.4	
t_{SR}*	Sector Width	*	
t_{BYTE}	Byte Period	1240±184	ns

* t_{SR} = (Sector size in bytes) X t_{BYTE} ns) ± 10%

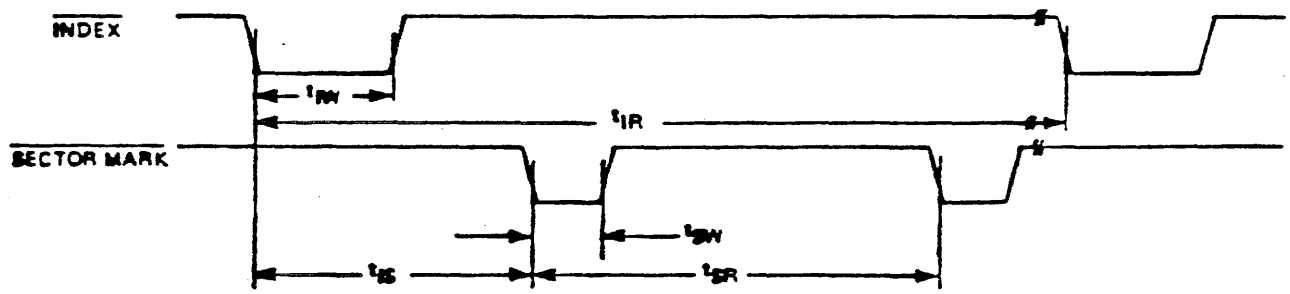


Figure 12 - INDEX and SECTOR MARK Timing

4. WRITE DATA AND CLOCK TIMING

WRITE DATA and WRITE CLOCK timing relationship is shown in Figure 13 and their AC characteristics are listed in Table 22.

TABLE 22 - Write Data and Write Clock AC Characteristics

Symbol	Parameter	Timing / 3450 & 7050	Units
t_{CLK}	WRITE CLOCK period	155±23	ns
t_{WH}	WRITE CLOCK high pulse width	77.5±12.5	ns
t_{WL}	WRITE CLOCK low pulse width	77.5±12.5	ns
t_{BIT}	WRITE DATA bit period	155±23	ns
t_{DC}	WRITE DATA setup time	20*	ns min
t_{CD}	WRITE DATA hold time	20*	ns min

* 60 ns is typical

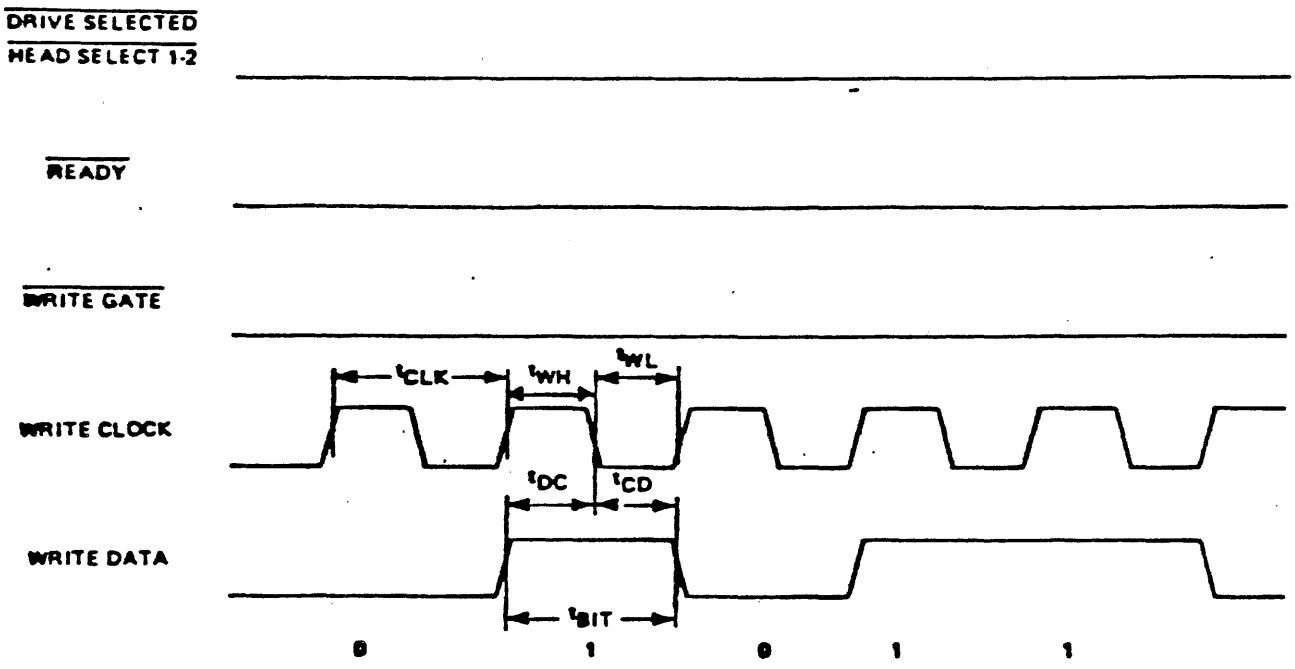


Figure 13 - WRITE DATA and WRITE CLOCK Timing

5. READ DATA AND READ CLOCK TIMING

READ DATA and READ CLOCK timing relationship is shown in Figure 14 and their AC characteristics are listed in Table 23.

TABLE 23 - Read Data and Read Clock AC Characteristics

Symbol	Parameter	Timing 3450 & 7050	Units
t_{CLK}	READ CLOCK period	155±23	ns
t_{WH}	READ CLOCK high pulse width	77.5±12	ns
t_{WL}	READ CLOCK low pulse width	77.5±12	ns
t_{BIT}	READ DATA bit period	155±23	ns
t_{DC}	READ DATA setup time	40*	ns min
t_{CD}	READ DATA hold time	40*	ns min
t_{BYTE}	Byte period	1240±184	ns

* 60 ns is typical

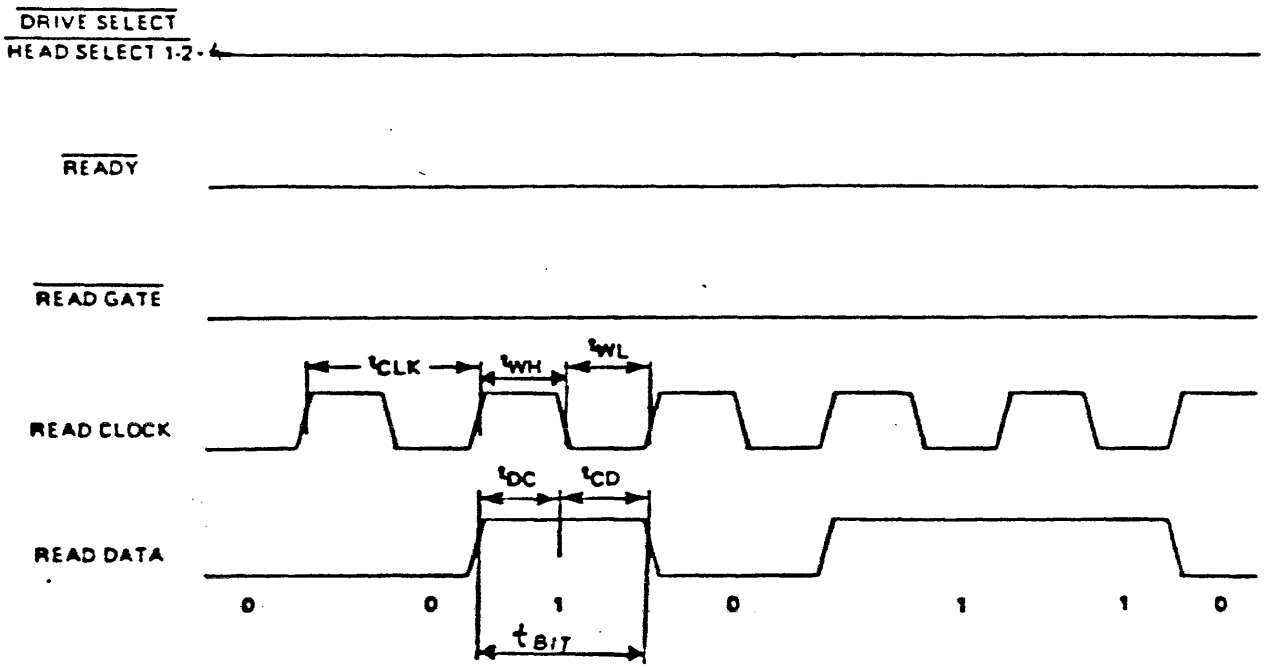


Figure 14 - READ DATA and READ CLOCK Timing

6. RECORD WRITING

Figure 15 shows timing requirements for writing full sectors (ID and data fields) and also for writing sector data fields only. Their AC characteristics are listed in Tables ~~24 and~~ 25.

TABLE 25 - Record Writing Control AC Characteristics for DISKOS 3450, 7050, ~~3350, 6650 & 15450~~ and

Symbol	Parameter	Timing 3450 & 7050	Units
t_{SH}	DRIVE SELECTED to HEAD SELECTED	20	us min
t_{SR}	DRIVE SELECTED to READY	100	ns min
t_{SG}	SECTOR MARK TO WRITE GATE	0±1	us
t_{IDG}	ID gap timing	23	Bytes min
t_{IDF}	ID fill	2	Bytes min
t_{DG}	Data gap (no Write to read transitions	11	Bytes min
t_{DF}	Data fill	2	Bytes min
t_{HW}	Head Select to WRITE GATE	100	ns
t_{BYTE}	Time for 1 byte	1240±184	ns

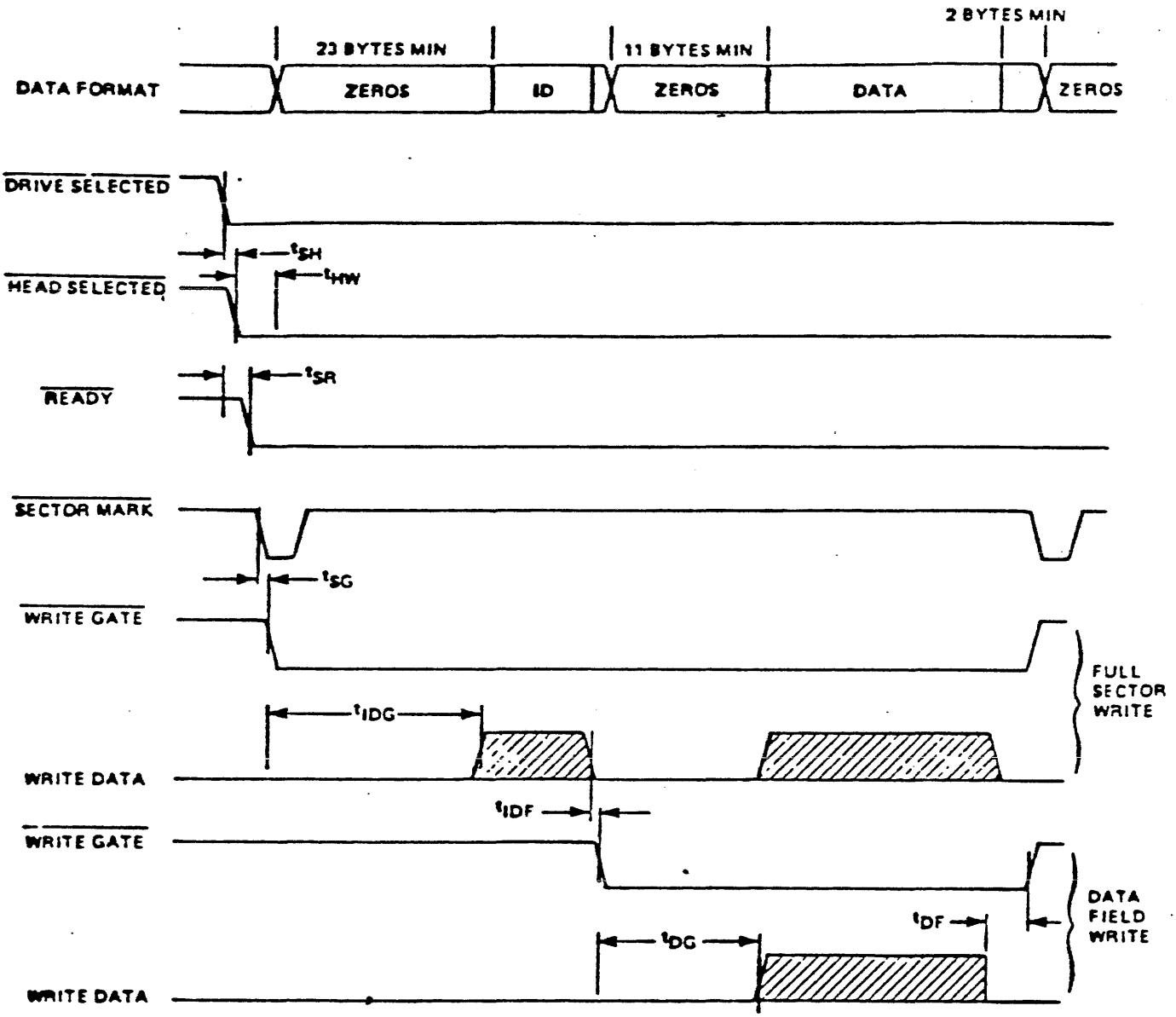


Figure 15 - Record Writing Timing

7. RECORD READING

Figure 16 shows timing requirements for reading ID and data fields and for reading data fields only. Their AC characteristics are listed in Table 27.

TABLE 27 - Record Reading Control AC Characteristics for DISKOS 3450, 7050 and ~~3350, 6650 & 15450~~

Symbol	Parameter	Min	Max	Units
t_{SH}	DRIVE SELECTED to HEAD SELECTED	20		us
t_{SR}	DRIVE SELECTED to READY	100		ns
t_{RDLW}	READ GATE DELAY for gaps allowing WRITE to READ transitions	13		us
t_{RDLR}	READ GATE DELAY for gaps limited to READ to READ or READ to WRITE transitions	1.9		us
t_{SYN}	READ PLO SYNCHRONIZATION (Data not valid for this period)		9	us
t_{HR}	HEAD SELECT to READ GATE	25		us

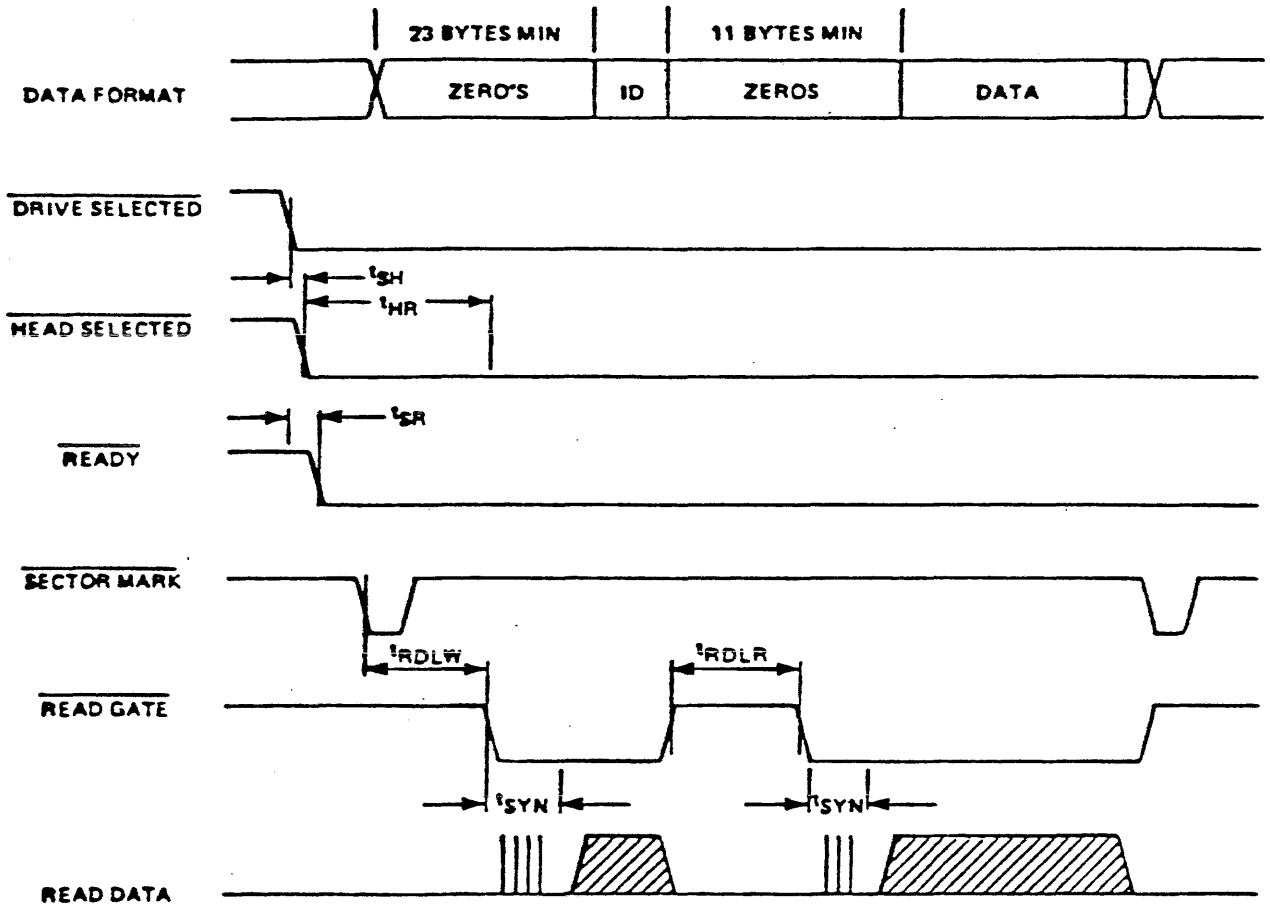


Figure 16 - Record Reading Timing

The combined operations are shown in Figure 17.

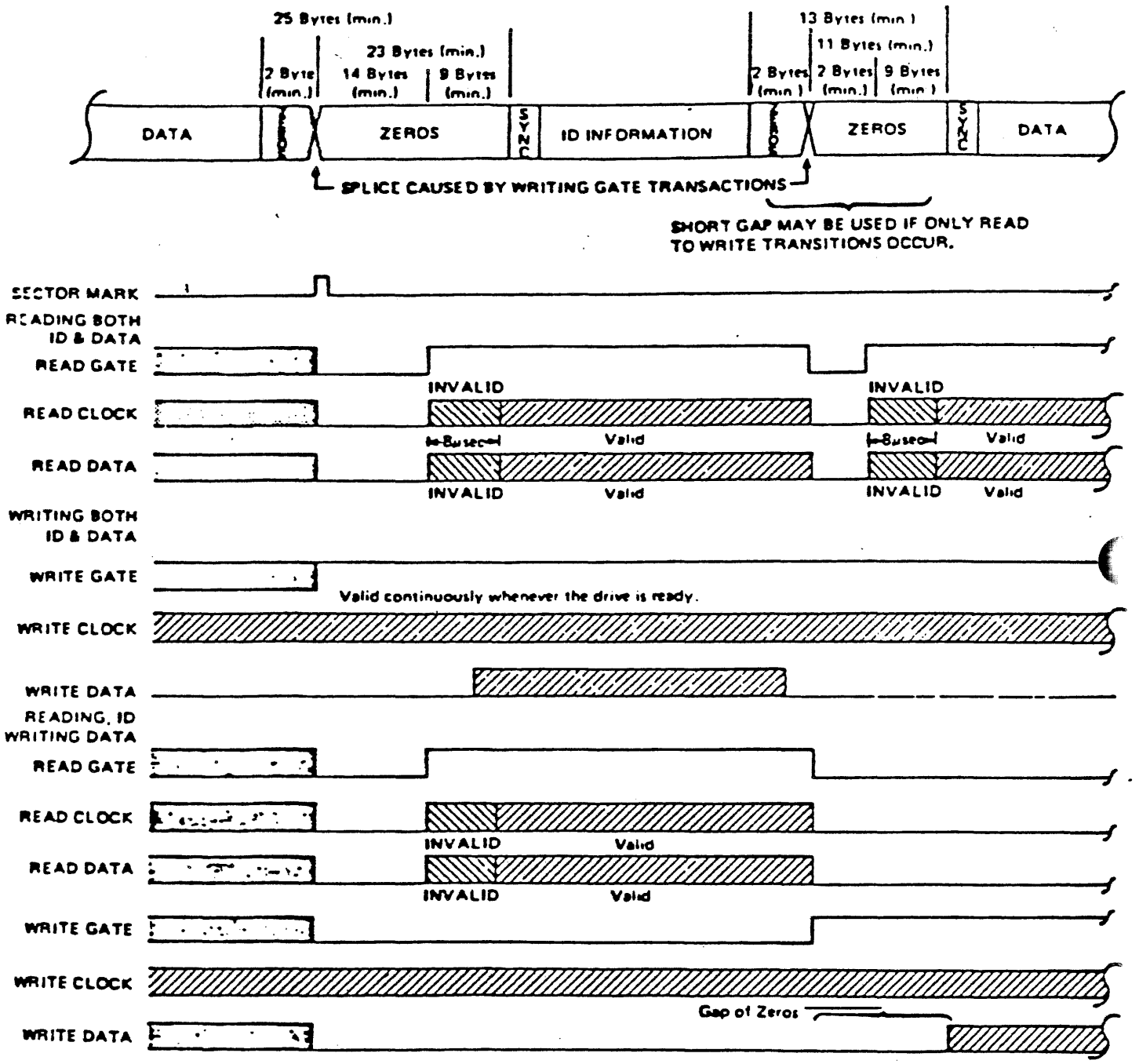


Figure 17 - READ & WRITE Transitions During Gaps

10.6 USER-ACCESSIBLE REGISTERS

All cylinder addresses, status information and commands are transferred over a three-state bidirectional DBUS 0 through 7 lines. These eight lines present an open circuit (tri-state) to the controller's bus until activated by DRIVE SELECT. An active DRIVE SELECT combined with RD (Read) sets the DBUS into the transmit mode while DRIVE SELECT combined with an active WR (Write) sets the DBUS into the receive mode. The information to control the drive resides in six accessible 8-bit registers.

a. Control Command Register which receives and stores commands from the controller;

b. Target Address Register - Upper Byte which receives the eight most significant bits of the desired cylinder address;

c. Target Address Register - Lower Byte which receives the eight least significant bits of the desired cylinder address;

d. Status Register which contains pertinent information about present operation;

e. Current Address Register - Upper Byte which contains the eight most significant bits of the current cylinder address;

f. Current Address Register - Lower Byte which contains the eight least significant bits of the current cylinder address.

Accessing of the registers is accomplished by a combination of active levels on DRIVE SELECT, RD, or WR, and register address lines A1 and A0, as shown in Table 9. The Command and Target Address Registers can only receive information and the Status and Current Address Registers can only transmit information.

TABLE 9 - Register Selection

A1	A0	WR	RD	Selected Register
0	0	1	0	Status Register
0	0	0	1	Command Register
0	1	1	0	Current Address-Upper Byte
0	1	0	1	Target Address-Upper Byte
1	0	1	0	Current Address-Lower Byte
1	0	0	1	Target Address-Lower Byte

10.7 COMMANDS

Seven Control Commands are used. All are single byte commands and are listed in Table 10.

TABLE 10 - Command Summary

	BITS							
Command	7	6	5	4	3	2	1	0
SEQUENCE UP	0	0	0	0	0	0	0	1
SEQUENCE DOWN	0	0	0	0	0	0	1	0
RESTORE	0	0	0	0	0	0	1	1
SEEK	0	0	0	0	0	1	0	0
FAULT RESET	0	0	0	0	0	1	0	1
READ DRIVE ID	0	0	0	1	0	0	0	0
READ BYTES PER SECTOR	0	0	0	1	0	0	0	1

a. SEQUENCE UP

The SEQUENCE UP Command causes the disc drive spindle motor to power up. The rotational speed of the disc is monitored, and after the drive is up to speed, a position signal calibration is performed (except for the 1070) and the heads are positioned to cylinder zero. The drive will present BUSY status while the SEQUENCE UP is in process. CYLINDER ZERO, SEEK COMPLETE and READY status is set at the successful completion of this command. WRITE PROTECT and DRIVE FAULT are set if the SEQUENCE UP was unsuccessful. The drive will also sequence up as described with a RESTORE command.

b. SEQUENCE DOWN

The SEQUENCE DOWN command causes the heads to be positioned to the landing zone and the spindle motor is braked to a stop. WRITE PROTECT status will be set at the completion of this command.

c. RESTORE

The RESTORE command causes the drive carriage to be repositioned to cylinder zero. The drive RESTORES automatically on SEQUENCE UP, or when a SEEK FAULT is detected. Upon failure of the RESTORE command, the heads will be positioned to the landing zone area and DRIVE FAULT status will be set. If the drive is not sequenced up, the restore command will result in the drive sequencing up and drive carriage positioned to cylinder zero.

d. SEEK

The SEEK command uses the contents of the Target Address Registers for desired cylinder address information. Upon receipt of this command, the drive will go NOT READY and BUSY while moving the carriage to the desired cylinder. When this is complete, the drive will again become READY and SEEK COMPLETE status will be posted. Upon failure of the SEEK command, the drive will RESTORE to cylinder zero and present READY, CYLINDER ZERO and SEEK FAULT status.

e. FAULT RESET

The FAULT RESET command clears both fault condition flip-flops (SEEK FAULT and DRIVE FAULT).

f. READ ID

This command sets the Drive ID code in the Current Address Register. READY status will be reset to the not ready state. In order to bring the drive to the READY state a SEQUENCE UP or RESTORE command must be executed. Thus, the Current Address Register contains the valid current cylinder address if the drive is READY and last requested parameter information if not READY. The drive ID assignment is shown in Table 11.

TABLE 11 - Drive ID Assignment

ID Code (HEX)	Drive Designation
00	Invalid
01	DISKOS 3350-01 or -10 (20, 160 bytes/track)
02	DISKOS 3350-01 (19,960 bytes/track)
03	DISKOS 3450 (12,960 bytes/track)
04	DISKOS 3450 (13,440 bytes/track)
05	DISKOS 7050 (13,440 bytes/track)
06	DISKOS 6650
07	DISKOS 15450
08-0F	Reserved
10	Reserved
11	DISKOS 1070-1
12	CD8005
13	CD8010
14	Reserved
15	DISKOS 1070-2
16-1F	Reserved
20-FF	Reserved

g. READ BYTES PER SECTOR

This command reports the bytes per sector selected by the switches mounted on the drive. The sector size is reported in the Current Address Registers.

Upon the receipt of this command the drive will become not READY and remain in the not READY state until a Sequence Up or Restore command is received and executed.

10.8 REGISTER BIT DEFINITIONS

TABLE 12 - Address Register Bit Definition

Data Bus Bit	7	6	5	4	3	2	1	0
Current Address Reg. Upper Byte	0	0	0	0	0	C_{10}	C_9	C_8
Current Address Reg. Lower Byte	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Target Address Reg. Upper Byte	0	0	0	0	0	C_{10}	C_9	C_8
Target Address Reg. Lower Byte	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

where for cylinder address

	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Cylinder 000	0	0	0	0	0	0	0	0	0	0	0
Cylinder 001	0	0	0	0	0	0	0	0	0	0	1
:											
:											
:											
Cylinder 1123	1	0	0	0	1	1	0	0	0	1	1

and for sector length :

Sector Length 000	0	0	0	0	0	0	0	0	0	0	0
Sector Length 001	0	0	0	0	0	0	0	0	0	0	1
:											
:											
Sector Length 1,316	1	0	1	0	1	0	1	0	0	0	0

TABLE 13 - Status Register Bit Definition

Bit	Name	Description
0	READY	The drive is up to speed, servo system is locked onto a servo track, and the unit is in a state to read, write, or seek.
1	SEEK COMPLETE	This bit is set when seek operation is completed. This status is invalid while BUSY is active.
2	SEEK FAULT	A fault was detected during a seek operation. This status is invalid while BUSY is active.
3	CYLINDER ZERO	Access arm is set to Cylinder 0. This status is invalid while BUSY is active.
4	BUSY	Drive is in process of executing a command.
5	DRIVE FAULT	A fault was detected during a write operation or a drive unsafe condition was detected.
6	WRITE PROTECT	The head selected is write protected. Write protection is set by switches in the drive or when the drive is not sequenced up.
7	COMMAND REJECT	Control or Register Load command received while drive is not ready, or improper command received. This status is invalid while BUSY is active.

5. I/O Cable Connectors

a. "A" Cable

Description	Berg P/N	Spectra-Strip P/N
Connector (60 pin)	65043-007	
Contact, insert	48048	
Flat cable (twisted pair), 30 pair, 28AWG		3CT-6028-7B-05-100

b. "A" Cable Mating Connector on Drive or Controller

Description	AMP P/N
60 pin right angle header	3-86479-4
60 pin vertical header	3-87227-0

c. "B" Cable

Description	3M P/N
Connector (26 pin)	3399-3000
Connector pull tab	3490-2
Flat cable (26 conductor) with ground plane and drain wire.	

d. "B" Cable Mating Receptacle on Drive or Controller

Description	AMP P/N
26 pin right angle header	1-86479-0
26 pin vertical header	1-87227-3

6. I/O Cable Characteristic

a. "A" Cable

Type: 30 twisted pair, flat cable
Twists per inch: 2
Impedance: 100 ± 10 ohms
Wire size: 28 AWG, 7 strands
Propagation time: 1.6 to 1.8 ns/ft.
Maximum cable length: 100 ft. cumulative
Voltage rating: 300 volts rms

b. "B" Cable (With Ground Plane)

Type: 26 conductor, flat cable with ground plane and drain wire.
Impedance: 65 ohms (3M P/N 3476-26)
Wire size: 28 AWG, 7 strands
Propagation time: 1.5 to 1.8 ns/ft.
Maximum cable length: 50 ft.
Voltage rating: 300 volt rms

c. "B" Cable

Type: Twinax
Impedance: 160 ± 16 ohms
Wire Size: 30 AWG, 7 strands
Diameter over outer insulator: 0.620" maximum
Propagation velocity: 70% minimum
Maximum cable length: 50 ft.

"A" CABLE

Function	Connector Pins Low	Connector Pins High	Connector Pin Layout	
Unit Select Tag	43	44	2	1*
Unit Select 2^0	45	46	4	3
Unit Select 2^1	47	48	6	5
Unit Select 2^2	51	52	8	7
Unit Select 2^3	53	54	10	9
Tag 1	1	2	12	11
Tag 2	3	4	14	13
Tag 3	5	6	16	15
Bit 0	7	8	18	17
Bit 1	9	10	20	19
Bit 2	11	12	22	21
Bit 3	13	14	24	23
Bit 4	15	16	26	25
Bit 5	17	18	28	27
Bit 6	19	20	30	29
Bit 7	21	22	32	31
Bit 8	23	24	34	33
Bit 9	25	26	36	35
Open Cable Detector	27	28	38	37
Index	35	36	40	39
Sector	49	50	42	41
Fault	29	30	44	43
Seek Error	31	32	46	45
On Cylinder	33	34	48	47
Unit Ready	37	38	50	49
Unused (always 0)	39	40	52	51
Write Protected	55	56	54	53
Power Sequence Pick		57	56	55
Power Sequence Hold		58	58	57
Unused	41	42	60	59
Spare (Optional Bus Bit 10)	59	60		

60 position, 28 AWG, 30 twisted pair
straight flat cables
maximum length - 100 ft.

* Triangle Mark

Figure 4 - Tag Bus I/O Interface

Bus	Tag 1 Cylinder Address	Tag 2 Head Select	Tag 3 Control Select
Bit 0	2^0	2^0	Write Gate
Bit 1	2^1	2^1	Read Gate
Bit 2	2^2	2^2	Unused (Servo Offset Plus)
Bit 3	2^3	Unused	Unused (Servo Offset Minus)
Bit 4	2^4	Unused	Fault Clear
Bit 5	2^5	Unused	Unused
Bit 6	2^6	Unused	Return to Track Zero (RTZ)
Bit 7	2^7	Unused	Unused
Bit 8	2^8	Unused	Unused
Bit 9	2^9	Unused	Unused
Optional Bit 10	2^{10}	Unused	Unused

Figure 5 - Tag Bus Decode

"B" CABLE

Function	Connector Pins Low	Connector Pins High	Connector Pin	Connector Layout
Write Data	15	14	2	1*
Ground		13	4	3
Write Clock	11	12	6	5
Ground		10	8	7
Servo Clock	3	2	10	9
Ground		1	12	11
Read Data	5	6	14	13
Ground		4	16	15
Read Clock	9	8	18	17
Ground		7	20	19
Seek End	19	20	22	21
Unit Selected	18	17	24	23
Ground		16	26	25
Index	23	22		
Ground		21		
Index	25	26		
Ground		24		

26 conductor flat cable,
maximum length - 50 ft.
* Triangle mark

Figure 6 - "B" Cable Interface

11.3 INTERFACE SIGNAL DESCRIPTIONS

This section gives functional descriptions for the signals on the "A" and "B" interface connectors. Details on how to transmit and receive these signals are given in Section 11.4.

Address and control information is transferred to the drive on a 10-bit bus, with three tag lines defining the type of information on the bus. Unit selection is provided by four binary coded lines gated into the drive by a Unit Select tag. Major status conditions of the selected drive, as well as index and sector marks, are returned to the controller on seven lines.

Data and clock signals between the drive and controller require five lines. These lines are associated with a physical drive using a radial connection between the drive and controller. Two additional lines in this cable supply an interrupt signal (Seek End) and an indication of selection (Unit Selected). See Figures 4, 5, and 6.

1. Bus Bits 0 to 9

   The 10 bus lines are used to transmit cylinder address, head address, or control functions from the controller to the drive. Bit 0 is the least significant digit and bit 9 is the most significant digit.

   a. Optional Bus Bit 10

      This bus line is used to transmit cylinder address bit 10 (binary 1024) via the normally spare pair in the "A" Cable (pins 59 and 60). This may be enabled on the 6650 SMD, 15450 SMD, and the SMD Adapter attached to a 6650 or 15450 by moving the shorting jumper from position W20 to position W21.

2. Tag 1 (Cylinder Address)

   The 10 bus lines are used to carry the cylinder address to the drive. Since the drive is a direct addressing device, the controller need only place the new address on the lines and strobe the lines with Tag 1 (see Figure 7). The drive must be On Cylinder before Tag 1 is sent. The bus lines should be stable throughout the tag time.

3. Tag 2 (Head Select)

   This signal is the head address that will be selected by the bits present on the bus lines when Tag 2 is true.

   In the DISKOS 3450 and 7050 , only bus bits 0, 1, and 2 are used; all other bus bits are ignored.

4. Tag 3 (Control Select)

This signal acts as an enable and must be true for the entire control operation.

a. Bit 0 (Write Gate)

The Write Gate line enables the write driver (Figure 5). See Figure 10 for typical Write Gate timing requirements.

NOTE: Write Gate to Read Gate timing is 14 microseconds instead of the 10 microseconds required by the standard SMD specification.

b. Bit 1 (Read Gate)

Enabling of Read Gate (Figure 5) enables digital read data on the transmission lines. The leading edge of Read Gate triggers the read chain to synchronize on an all zeros pattern. (See Figures 8 and 9 for typical Read Gate timing.)

NOTE: Write Gate to Read Gate timing is 14 microseconds (Figure 9) instead of the 10 microseconds required by the standard SMD specification.

c. Bit 2 (Servo Offset Plus)

In all drives using the SMD Adapter this function is not supported and no response will occur if this operation is attempted.

d. Bit 3 (Servo Offset Minus)

In all drives using the SMD Adapter, this function is not supported and no response will occur if this operation is attempted.

e. Bit 4 (Fault Clear)

A pulse, 250 nanoseconds minimum, sent to the drive will clear the fault status. The fault status may recur if the fault condition still exists.

f. Bit 5 (AM Enable)

Not supported by this interface. No response will occur at the drive if this operation is attempted.

g. Bit 6 (RTZ)

A pulse, 250 nanoseconds minimum, 10 milliseconds maximum, sent to the drive will cause the actuator to move to track zero, reset the head address to head zero, and clear Seek Error.

This motion is significantly longer than a normal seek to track zero and should be used for recalibration only, not data acquisition.

h. Bit 7 (Data Strobe Early)

Not supported by this interface. No response will occur at the drive if this operation is attempted.

i. Bit 8 (Data Strobe Late)

Not supported by this interface. No response will occur at the drive if this operation is attempted.

j. Bit 9 (Release)

Not supported by this interface. No response will occur at the drive if this operation is attempted.

5. Unit Select Tag

This tag is used to select the drive defined by this Unit Select 1, 2, 4, and 8 lines. The drive is selected at the leading edge of the tag and responds with Unit Selected within 200 nanoseconds. The drive address on the Unit Select lines must be stable 200 nanoseconds before the leading edge of the tag.

~~In Models 3350 SMD, 6650 SMD, and 15450 SMD; the Unit Select lines must remain stable until 200 nanoseconds after the leading edge of the tag. But,~~ In all drives using the SMD Adapter the Unit Select lines must remain stable throughout the time that the drive is selected.

In all drives, the Unit Select Tag must remain stable throughout the time the drive is to be selected. For timing information, see Figure 11.

6. Unit Select 1, 2, 4, and 8

These four lines are binary-coded to select one of 16 logical drive addresses. The address placed on the Unit Select lines is compared by each drive against the logical address assigned. When the Unit Select tag rises, the drive which compared equal becomes selected. Care must be taken so that each physical drive is strapped for different logical addresses. Timing of these lines is described in this Unit Select Tag description.

An eight-switch dip pack is used for preassigning a drive logical address at installation time or any time after (only four switches are used for drive addressing).

7. Individual Lines

a. Sector

The sector mark is derived from the servo track. Timing integrity is maintained throughout seek operations (see Figure 10). The number of sectors per revolution, and therefore sector size, is switch selectable and is derived using a byte counter. Refer to the INSTALLATION section for specific information on switch settings.

The microprocessor sets sector size during initialization; after setting the switches, power must be removed from the drive and then restored to cause the newly selected sector size to be established at the drive.

b. Fault

When the fault line is true, a fault condition exists at the drive. The following types of faults may be detected by the drive:

Write Fault (Write Gate with Write Protect).
Write Off Cylinder (Write Gate without On Cylinder).
Multiple Heads Selected.
No transitions during write (MFM format).
Write Gate without write current at the head.
Write current at the head without Write Gate.
Write when servo is off-track.
Write during a Servo Offset operation.
Write Gate and Read Gate occurring simultaneously.
Read Gate while not On Cylinder.
Unable to Restore (RTZ) drive.

A fault condition will immediately inhibit writing.

This line may be cleared by Fault Clear, or Restore (RTZ).

c. Seek Error

When the Seek Error line is true, a seek error has occurred. The error may be cleared by RTZ. Seek Error indicates that the drive was unable to complete a seek. When this condition is detected, the drive automatically returns the heads to cylinder zero.

Note: For 3450's, if the seek address is greater ~~than 560 (230 hexadecimal); or for 2050's and 3450's, if it is greater~~ than 525 (20D hexadecimal); or for 7050's, if it is greater than 1049 (419 hexadecimal); Seek Error will go true within 450 microseconds (not the 100 nanoseconds in the standard SMD specification).

d. On Cylinder

On Cylinder status indicates that the servo has positioned the heads over a track. The status is cleared with either a seek or RTZ operation.

e. Index

The Index signal occurs once per revolution, and its leading edge is considered the leading edge of Sector Zero, typically a 2 byte wide pulse (see Figure 10). Timing integrity is maintained throughout seek operations.

f. Unit Ready

Unit Ready true indicates that the drive is up to speed. The heads are positioned over the recording surface, and no fault condition exists.

g. Open Cable Detector

The Open Cable detect circuit (see Figure 3) disables the interface when the "A" Cable is disconnected.

This signal gates the desired drive number into the compare circuitry.

h. Address Mark Found

Address Mark Found is not supported by this interface. This line will always be false.

i. Unit Selected

When the four Unit Select bit lines compare with the setting of the Unit Select switches on the adapter, and the Unit Select Tag is received, the Unit Selected line becomes true and is transmitted to the controller on the "B" cable (see Figure 11). Multiple Units Selected responses on a daisy-chained system indicate duplicate switch settings may have been used.

j. Write Protected

Setting the Write Protect switch on the drive's main board will inhibit writing and signal Write Protected. Attempting to write while protected will cause a Fault to be issued.

k. Seek End

Seek End is the OR combination of On Cylinder or Seek Error indicating that a seek operation has terminated (see Figure 7 for timing).

l. Power Sequencing

Power Sequencing is not supported by this drive. Pick and hold are interconnected to represent a Sequenced Up drive at all times.

~~Using the 3350 SMD, 6650 SMD, or 15450 SMD drives,~~ Both Pick and Hold lines must be held to ground potential for drive operation. If either line is open or at +1.4 volts or greater, the drive will sequence down (move the heads to the landing zone and stop its spindle motor) and remain sequenced down until both lines are at ground potential. When this occurs, it will sequence up and become Ready when at speed.

m. Busy

The Busy indication is not supported by this drive.

5. Data and Clock Lines (Figure 12)

a. Write Data

This line carries NRZ data which is to be recorded on the disc.

b. Servo Clock

The Servo Clock is a phase-locked clock generated from the servo track (Figure 12). It is used to serialize write data. Servo Clock is available at all times (not gated with unit select) that the drive is Ready.

c. Read Data

This line transmits the recovered data in NRZ form (see Figure 12).

d. Read Clock

The Read Clock defines the beginning of a data cell. It is an internally derived clock signal and is synchronous with the recovered data as shown in Figure 12. Read Clock is in phase sync with Read Data within 8 microseconds after the leading edge of Read Gate.

e. Write Clock

This line transmits the Write Clock signal from the controller, which must be synchronized with the NRZ data as shown in Figure 12. The Write Clock is the Servo Clock retransmitted to the drive during a write operation. The Write Clock need not be transmitted continuously, but must be transmitted at least 250 nanoseconds prior to Write Gate.

11.4 INTERFACE DC CHARACTERISTICS

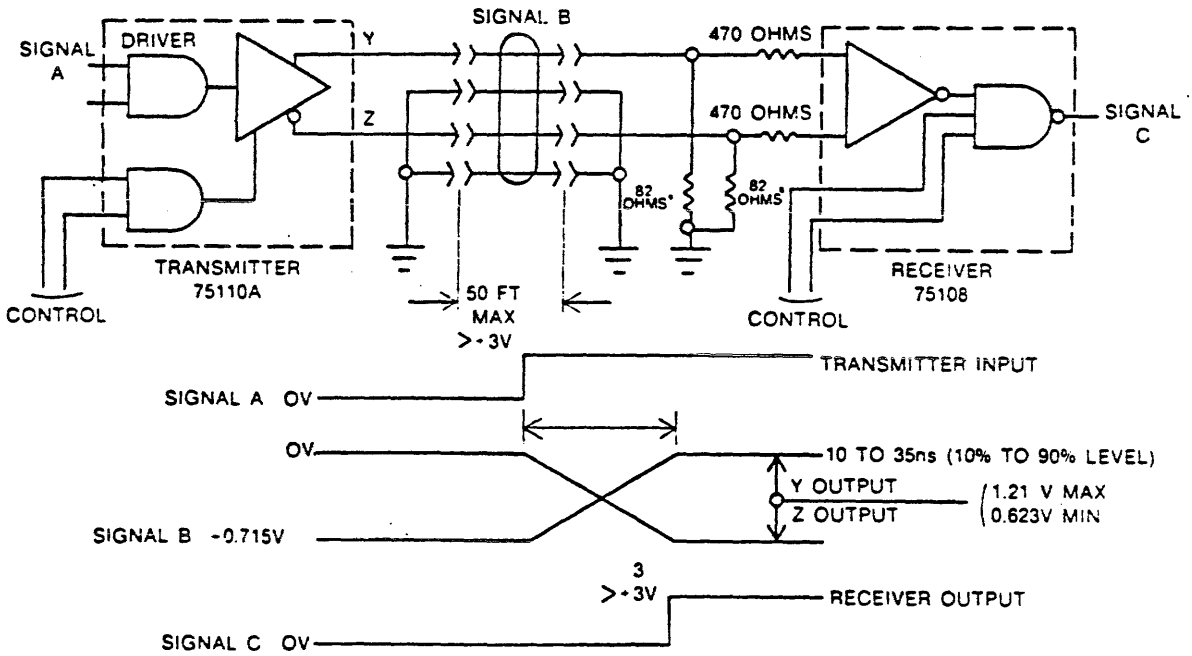
This section, through tables and figures, sets forth the details that need to be observed, in order to properly transmit and receive the interface signals listed in Section 11.2 and described in Section 11.3.

All input and output signals are digital, using SMD standard transmitters and receivers to provide a terminated, balanced, transmission system for specified cable lengths and/or normal electrical environment.

The "A" cable is a twisted pair flat cable. The "B" cable is a flat ribbon cable with ground plane and drain wire. Twisted pair or ground plane shielding, or both, are used to minimize cross talk and to reduce inductive coupling.

1. Terminated and Balanced Transmission System

   Transmitters and receivers of the SMD standard types 75110A and 75108 or equivalent are used to provide a terminated and balanced transmission system (see Figure 1).



* Terminator resistors are on drive or adapter logic card or controller. These signals must be star cabled.

Figure 1 - Typical Read/Write Data and Clock Transmitter and Receiver

2. Line Transmitter Characteristics

The SMD standard line transmitters (Figure 2) are compatible with the line receivers described in the next section.

a. Output Signal Levels

Data Signals (see Figure 2)
Control Signals (see Figure 3)

b. Output Line Polarity

Control Signals: On the "A" cable, the transmitters (Figure 3) are connected to the I/O line so that the output, labeled Z, corresponds to the odd numbered pin of the cable connector; the output in turn connects to the receiver pin labeled B, except for the Unit Selected line, which is connected in the opposite manner.

When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver, except for the Unit Selected line where a logical 1 into the transmitter produces a logical 0 out of the receiver.

3. Input Amplifier (Receiver) Characteristics

The drive's input amplifier (Figure 3) is SMD-standard compatible with the line transmitter described in the previous section.

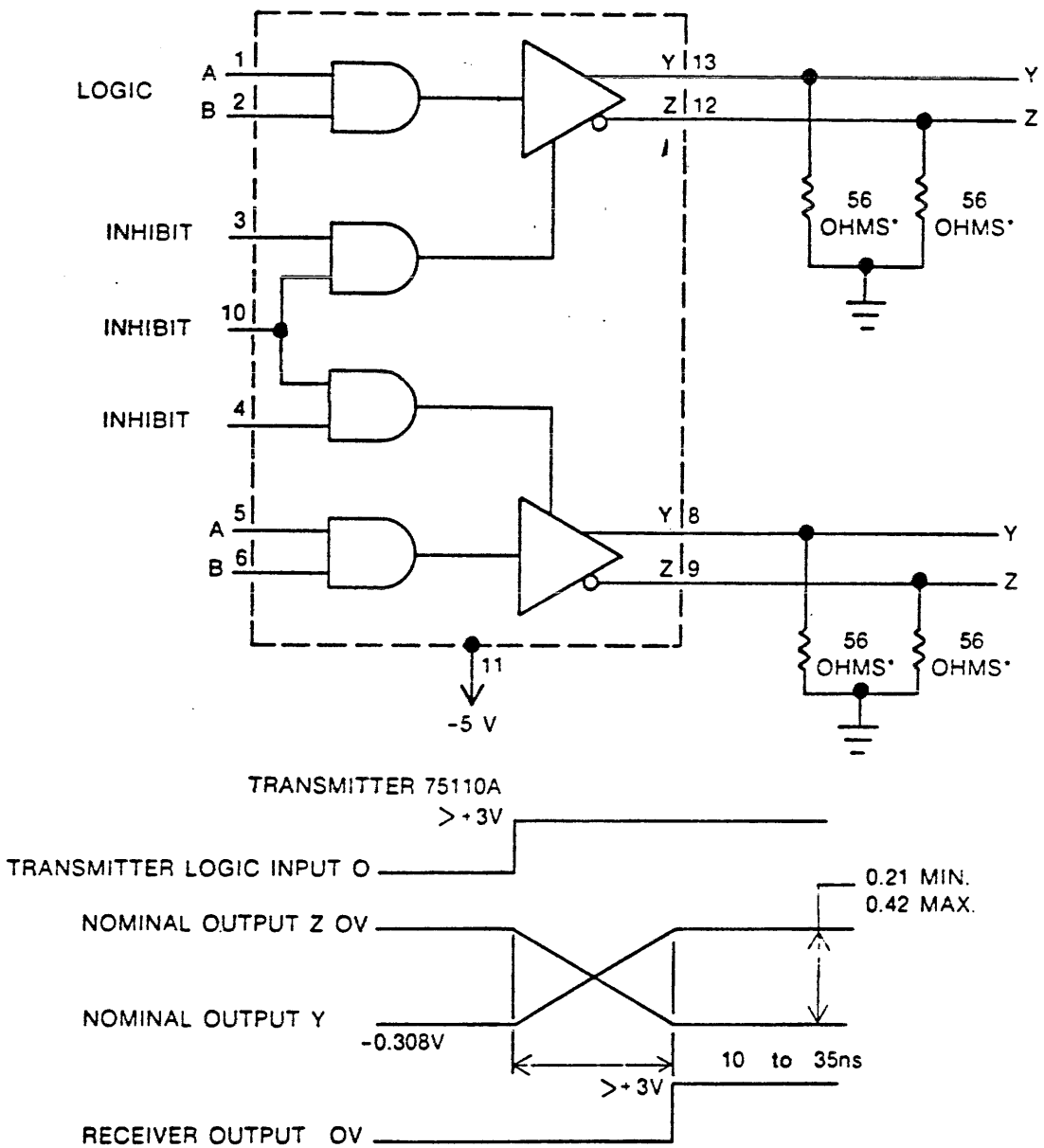
a. Receiver Propagation Delay

The receiver propagation delay is typically 17 nanoseconds in the direction of the logical 1, and 17 nanoseconds in the direction of the logical 0.

b. Receiver Input Polarity

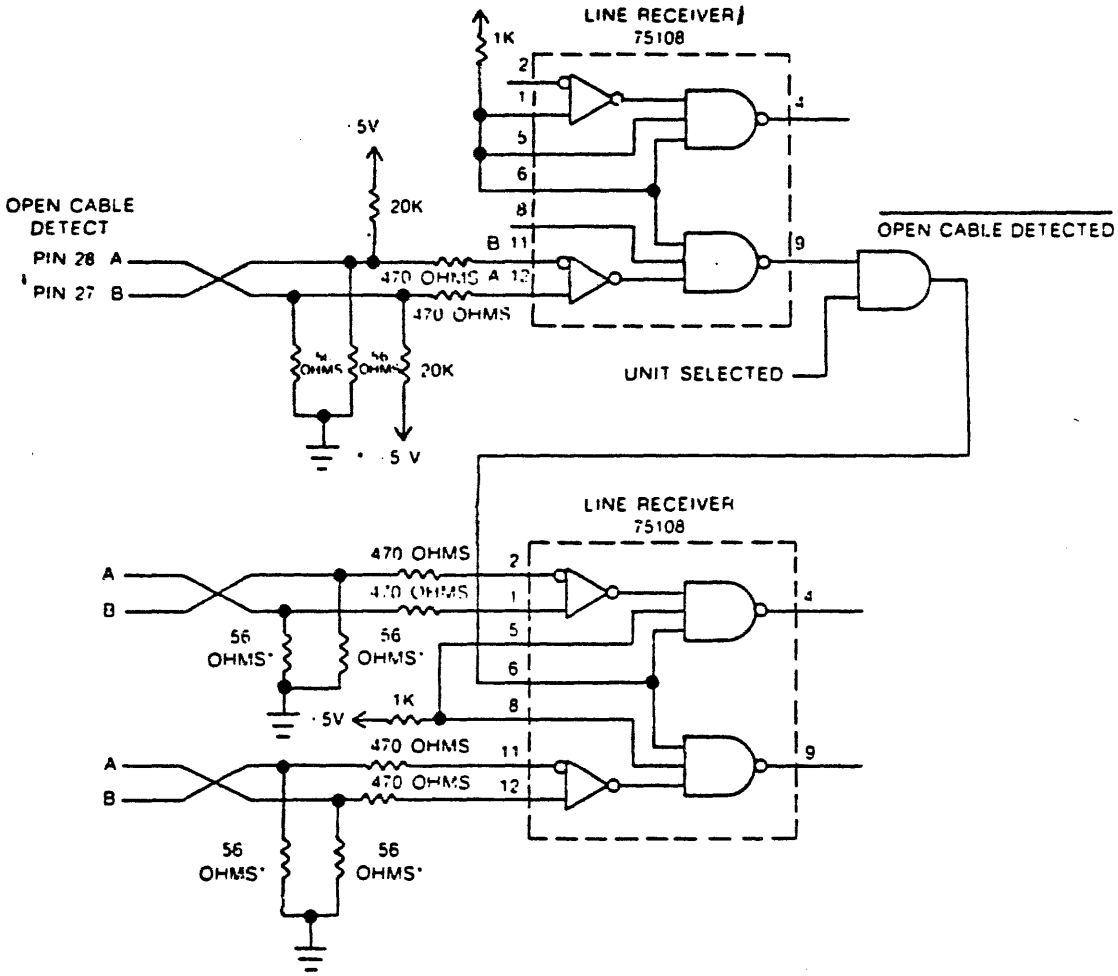
Control Signals: The Input (labeled "B") of the receiver (Figure 3) is connected to the odd numbered of the pair in the cable and in turn connected to the transmitter pin labeled Z.

Data Signals - See Figure 1.



* Terminating resistors are required on all "A" cable transmitters. Transmitters in the drive are terminated by the terminator assembly. Refer to the terminator paragraph (Section 11.2).

Figure 2 - Control Line Transmitter



* Terminating Resistors are located:

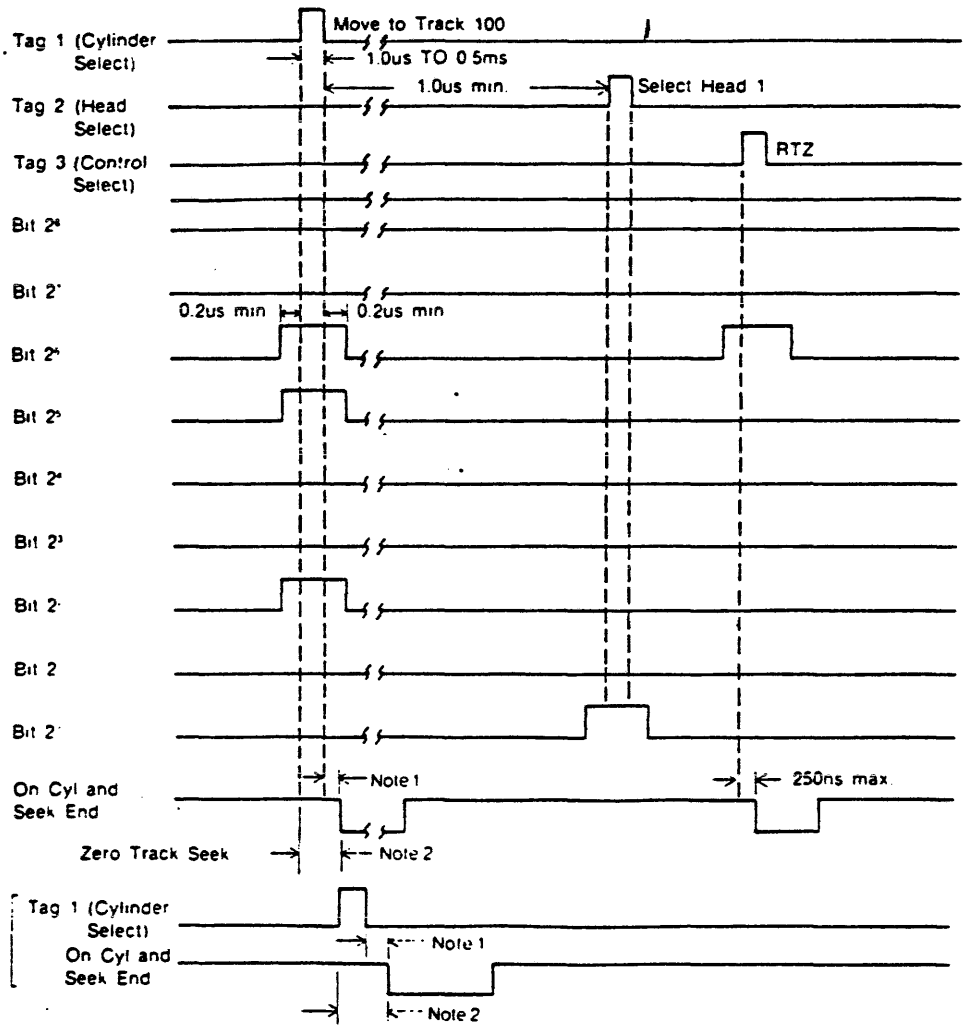
A. On logic board for "B" cable lines.

B. In a separate terminator assembly for the "A" cable.

Figure 3 - Control Line Receiver

11.5 INTERFACE TIMING

This section discusses the timing requirements for the various operations performed on the controller interface.



Note 1: 120 ns maximum for 3350 SMD, 6650 SMD, and 15450 SMD. See Note 2 for all other drives.

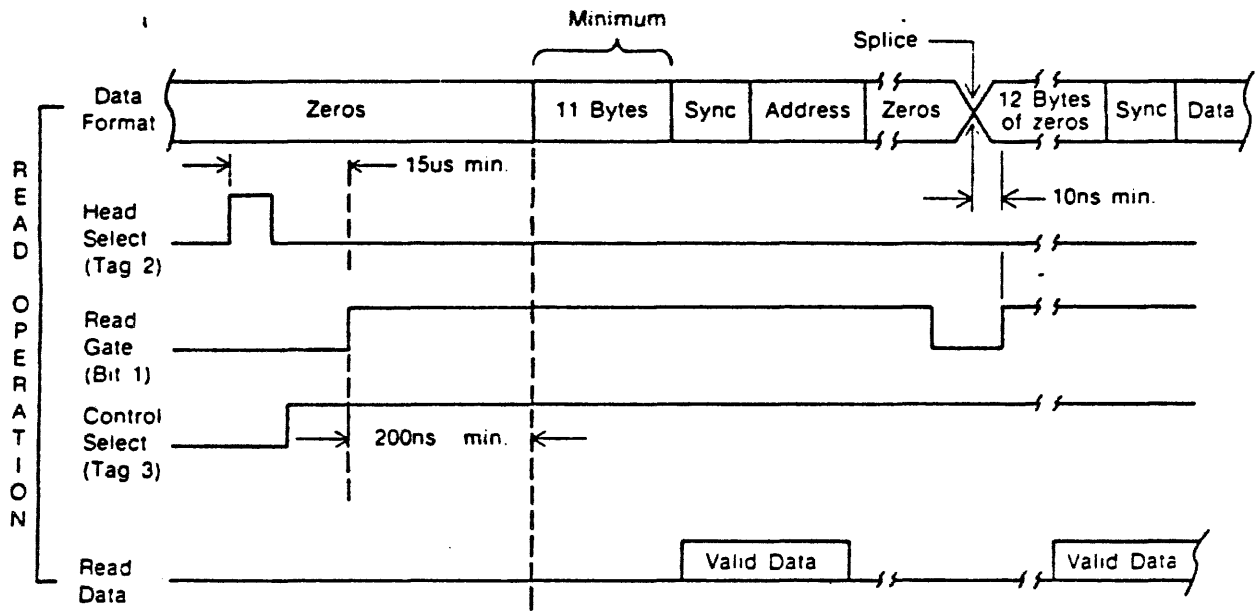
Note 2: 450 ns from leading edge of Tag 1 for all drives using SMD Adapter.

On Cylinder and Seek End signals are identical unless a seek error occurs. Seek error initiates a constant Seek End until RTZ clears the error.

Figure 7 - Tag and Bus Timing

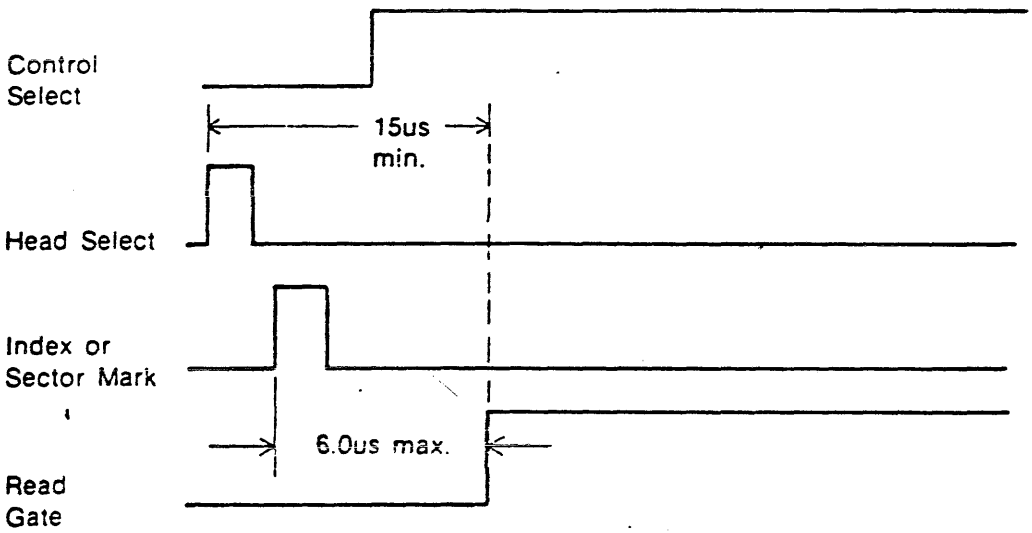
In the DISKOS 3350 SMD, 6650 SMD, and 15450 SMD, the switch assignment is as follows:

Switch 10N-1 closed (ON) sets the 2^0 bit (binary 1).
Switch 10N-2 closed (ON) sets the 2^1 bit (binary 2).
Switch 10N-3 closed (ON) sets the 2^2 bit (binary 4).
Switch 10N-4 closed (ON) sets the 2^3 bit (binary 8).



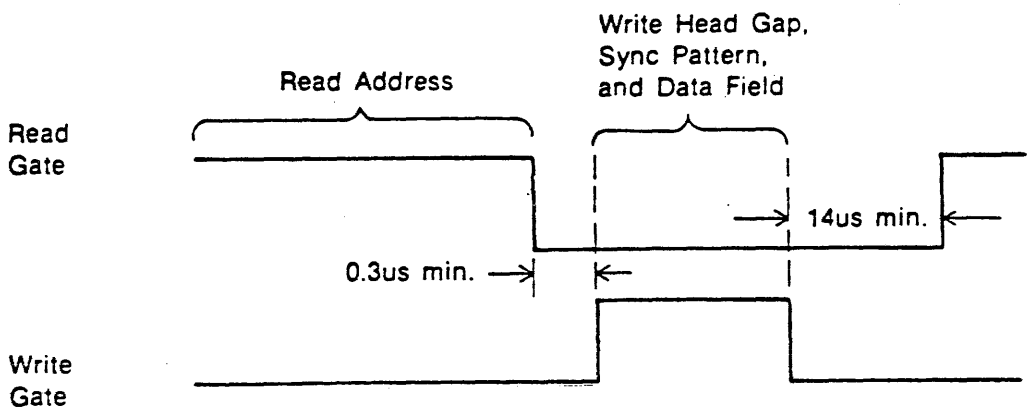
Read Gate must be dropped prior to the write splice. It must be reinitiated at least one bit after the write splice and with at least 10 bytes of zero bits remaining in the sync field. A 12 byte example consists of one byte for write splice and 11 bytes for PLO sync.

Figure 8 - Typical Read Timing



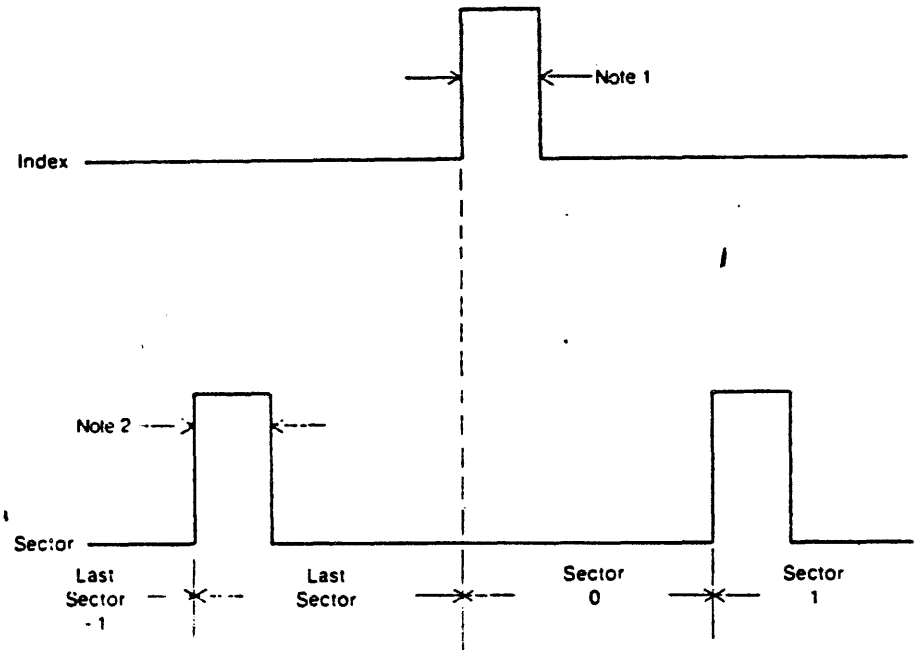
If a read operation is to be performed after index or sector, Read Gate must not occur later than 6.0 us after the leading edge of index or sector.

A. Typical Read Control Timing



B. Typical Write Control Timing

Figure 9 - Control Timing



Note 1: ~~1.92 ± 0.05 microseconds for 3350 SMD, 6650 SMD and 15450 SMD; 960 ± 25 nanoseconds for 3350, 6650, 15450, and 1070 using SMD Adapter;~~
1.24 ± 0.03 microseconds for 7050 and 3450 using SMD Adapter.

Note 2: ~~960 ± 25 nanoseconds for 3350, 3350 SMD, 6650, 6650 SMD, 15450, 15450 SMD and 1070;~~
1.24 ± 0.03 microseconds for 7050 and 3450 using SMD Adapter.

Figure 10 - Index and Sector Mark

Note: The sector pulse width is as shown in Figure 10 instead of the 1.25-microsecond pulse specified in the standard SMD specifications.

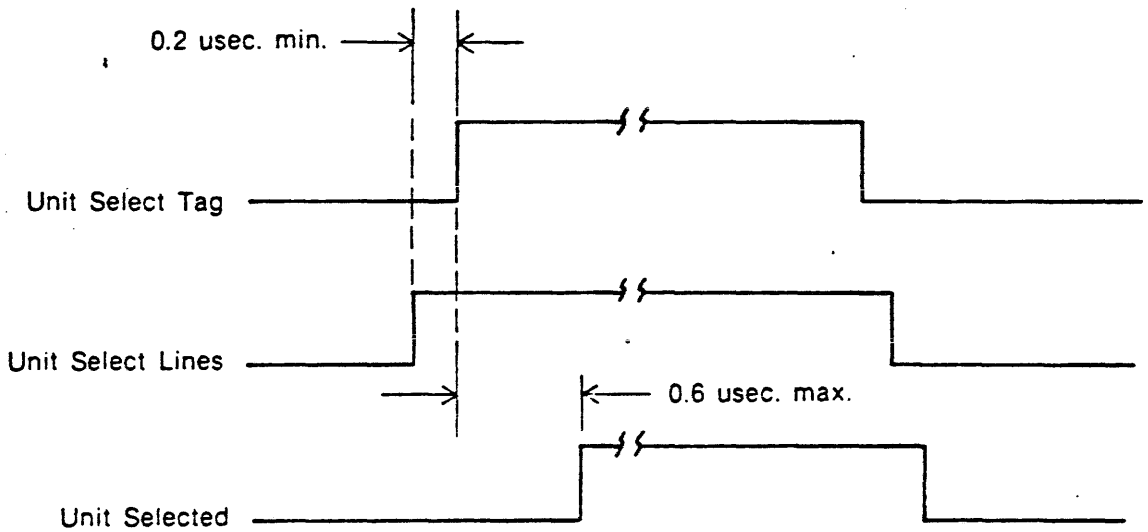
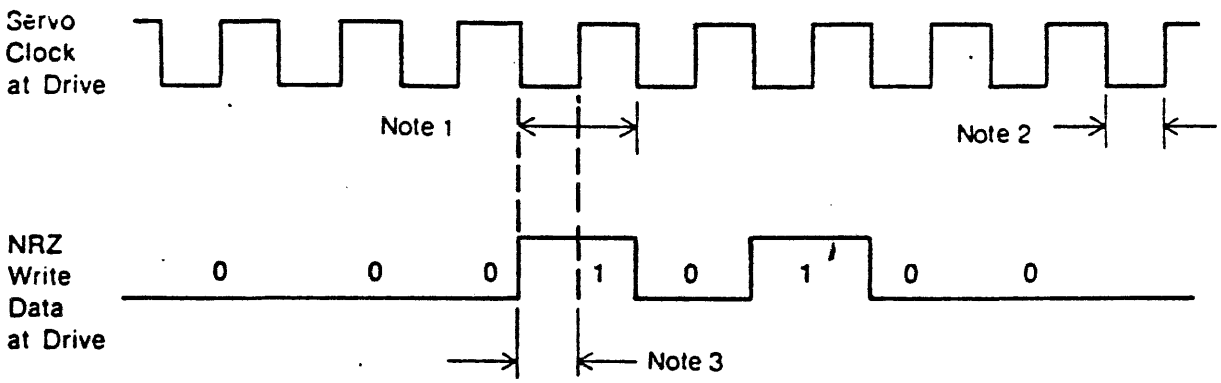
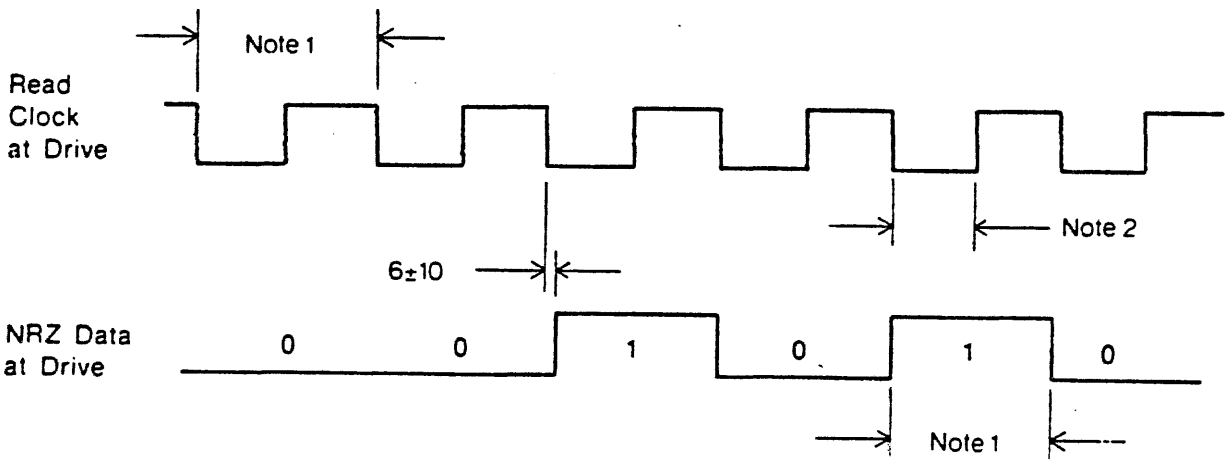


Figure 11 - Drive Select Timing





Note 1: ~~120 ± 10 nanoseconds for 3350 SMD, 6650 SMD, 15450 SMD and 3350, 6650, and 15450 using SMD Adapter;~~
155 ± 12 nanoseconds for 7050 and 3450 using SMD Adapter;
~~186 ± 15 nanoseconds for 1070 using SMD Adapter.~~

Note 2: ~~60 ± 10 nanoseconds for 3350 SMD, 6650 SMD, 15450 SMD and 3350, 6650, 15450 using SMD Adapter;~~
77.5 ± 12 nanoseconds for 7050 and 3450 using SMD Adapter;
~~93 ± 15 nanoseconds for 1070 using SMD Adapter.~~

Note 3: ~~60 ± 40 nanoseconds for 3350 SMD, 6650 SMD, 15450 SMD and 3350, 6650, 15450 using SMD Adapter;~~
77 ± 52 nanoseconds for 7050 and 3450 using SMD Adapter;
~~93 ± 62 nanoseconds for 1070 using SMD Adapter.~~

Figure 12 - NRZ Data and Read Clock Timing

1. Some hardware oriented constraints must be recognized when designing a format. The following is a list of those format parameters:

a. Read Initialization Time

Between the deselection of one head and the selection of another head, there is a 5 microsecond delay within the drive due to circuit characteristics. The time from the initiation of a head change until data can be read using the selected head is 24 microseconds maximum (5 microseconds for head selection, 10 microseconds for read amplifier stabilization, and 9 microseconds for phase lock synchronization).

b. Write-To-Read Recovery Time

Assuming head selection is stabilized, the time before Read Gate can be enabled after switching Write Gate off is 10 microseconds, minimum.

c. Read-To-Write Recovery Time

Assuming head selection is stabilized, the time from dropping Read Gate to enabling Write Gate shall be 0.2 microsecond, minimum.

d. Beginning-of-Record Tolerance (see Figure 13)

This tolerance is provided to allow for write splice and write-to-read recovery time for multisector operations.

This gap is 9 bytes.

e. Read PLO Synchronization

The synchronization time needed to allow the phase-locked oscillator to synchronize is 8 microseconds of zeros.

f. Sync Pattern

The sync pattern consists of "1" bits, indicating the beginning of the address or data area (one "1" bit is the minimum required).

g. Write Driver Turn On

The write driver turn on time is about 0.8 microsecond or one byte time. This time has to be accounted for to know where the splice areas are located.

2. Write Format Procedure

Provision must be made to format the disc. The following procedure is recommended: A suggested format is shown in Figure 13.

a. Select desired drive, cylinder, head and sector.

b. The controller must provide a 5 microsecond minimum delay between selecting a head and starting a search for the leading edge of the sector pulse. This delay will ensure that the drive will be ready to write when the leading edge of the sector is detected.

c. Search for leading edge of desired sector.

d. Detect leading edge of selected sector and raise Write Gate.

e. Write all zeros for write recovery and PLO sync areas (20 bytes minimum).

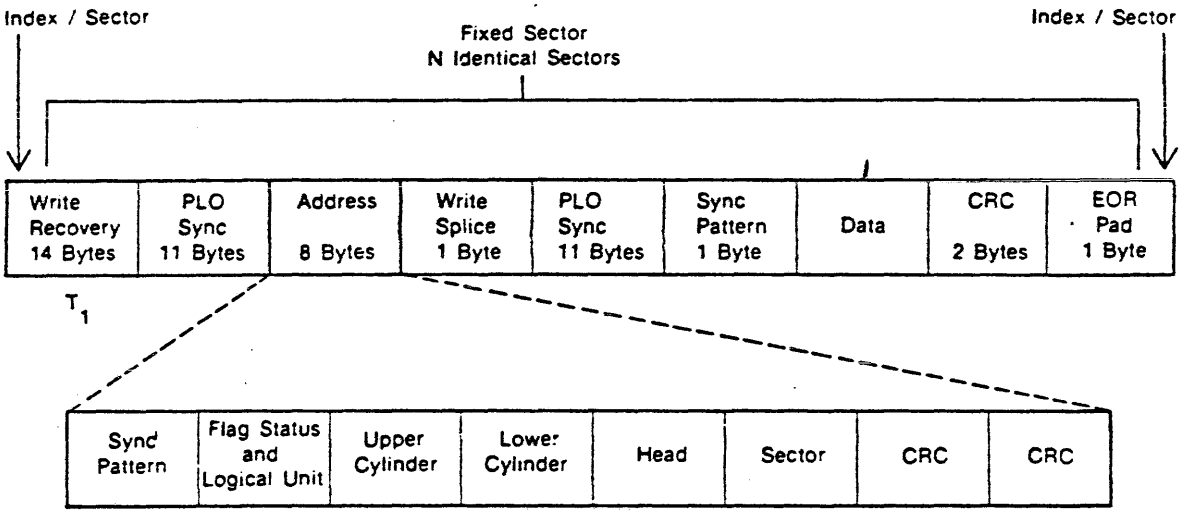
f. Write a sync pattern, the address, and the address checkword.

g. Write all zeros for write splice gap and PLO sync field (12 bytes minimum).

h. Write a sync pattern, the data field, the two byte data field checkword, and the five byte field of zeros (see Figure 13). The data field should preferably be a worst case pattern.

i. The end tolerance gap specified by the standard SMD specification is not required by this drive. However, if it is used, it is preferable to write zeros to the next sector pulse.

j. If the next sector of the same track is to be formatted and the head is not deselected, the Write Gate should be left on. In this case, all zeros should be written until the leading edge of the next sector or index pulse.



T_1 = Time between leading edge of index/sector and read gate is 8 bytes. A splice point may exist within this area.

Example: What is data field length using 66 sectors?

$$\text{Data Field} = \frac{\text{Total Bytes/Track}}{\text{Number of Sectors/Track}} - \text{(Sync Fields, Tolerance Gaps, and Addresses)}$$

$$= \frac{20{,}160}{66} - 49 = 256 \text{ Bytes/Sector}$$

but DATA = 256 Bytes/Sector is a reasonable size

$$\% \text{ Efficiency} = \frac{256 \times 66}{20{,}160} \times 100 = 83.8\%$$

* 20,160 usable bytes per track.

Note: Write Recovery is 14 bytes instead of 16 bytes and EOR Pad is 1 byte instead of 8 bytes as suggested by the standard SMD specification.

Figure 13 - Sector Format

3. Control Timing (Figure 8)

a. Read

The control line associated with a read operation is the Read Gate line.

The leading edge of Read Gate forces the phase locked oscillator to synchronize on an all zeros pattern. Read Gate also enables the output of the data separator onto the I/O lines. There may be invalid data transitions on these lines during the synchronization period. Read Gate must be dropped and raised again after going through a splice area. Read Gate may be enabled 60 $\pm$ 4 clock periods after the leading edge of index or sector.

The sync pattern search may begin 48 servo clock periods after the leading edge of Read Gate.

Head switching and read amplifier stabilization (see Figure 8) shows the latest acceptable time at which a head can be selected in order to read the next successive sector using the format shown in Figure 13.

Read Data and Read Clock may not have valid data until 8 microseconds after the leading edge of Read Gate, due to phase lock synchronizing time.

There should be no splice area after Read Gate is raised.

b. Write Data Field

The control line associated with a write operation is Write Gate.

The sector address must always be read and verified prior to writing the data field, except while formatting.

When writing the data field it must always be preceded by writing the PLO sync field and sync pattern.

The controller must provide an interval delay of at least two bit times (approximately 240 nanoseconds) between the trailing edge of Read Gate and the leading edge of Write Gate. This delay will allow for signal propagation tolerances and prevent a possible overlap of Read and Write Gates in the drive.

Writing the data field must always be followed by writing the checkword and at least an eight bit gap of zeros at the end of the checkword.

During formatting, Write Gate is raised upon detecting index or sector. During a record update, Write Gate is raised within two byte times after the last bit of the address.