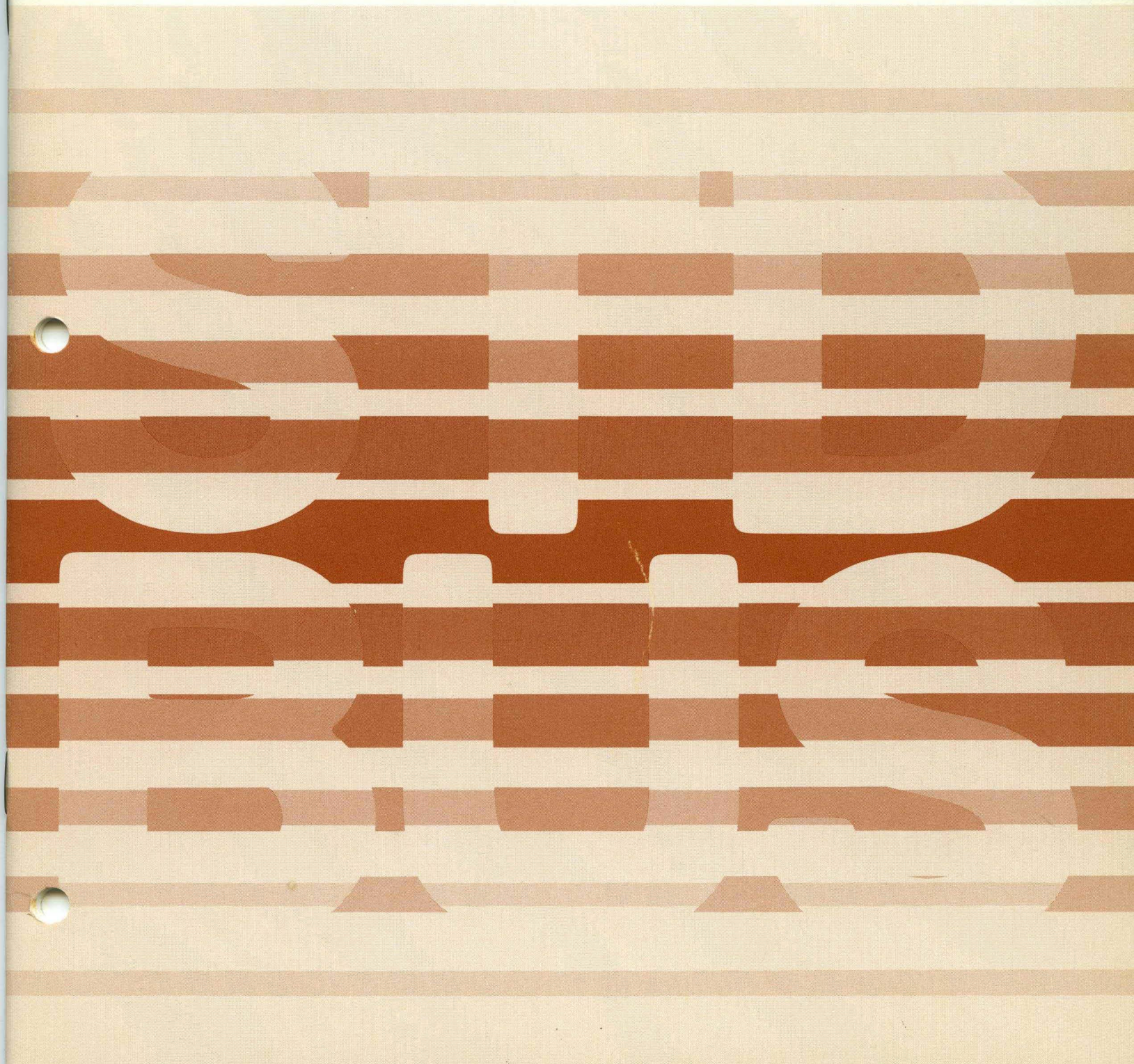
PRO-LOG
CORPORATION

STD 7000

7605 Programmable TTL I/O Card

USER'S MANUAL



7605
Programmable TTL I/O Card
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PRO-LOG CORPORATION

9/81

7605 TTL PROGRAMMABLE TTL I/O CARD

TABLE OF CONTENTS

1, PRODUCT DATA SHEET - 7605 PROGRAMMABLE TTL I/O CARD

A. PRODUCT OVERVIEW

The 7605 supplies four 8-bit I/O ports that can be programmed as input, output, or output with readback (total of 32 programmable I/O lines). Port access is via two 40-pin latched connectors with .025 inch square post headers. The output lines are TTL compatible open-collector drivers with 1K pullups. These lines are tied to input ports. After power-on reset, all ports are in input mode. To use an output port, the user simply writes to the port lines desired. The 7605 decodes 8 address lines with provision for expansion. An on-card jumper system allows the user to map the four consecutive port addresses occupied by the 7605 anywhere in the 256 port address field.

B. PRODUCT FEATURES

- 32 I/O Lines, Each Programmable as Input, Output, or Output with Readback
- User-selectable Port Address (256 Port Field)
- Socketed ICs
- Single +5V Operation
- Uses Two Latching 40-pin Headers
- Input Port Loading 14 LSTTL Loads
- Output can Drive 50 LSTTL Loads

C. BLOCK DIAGRAM

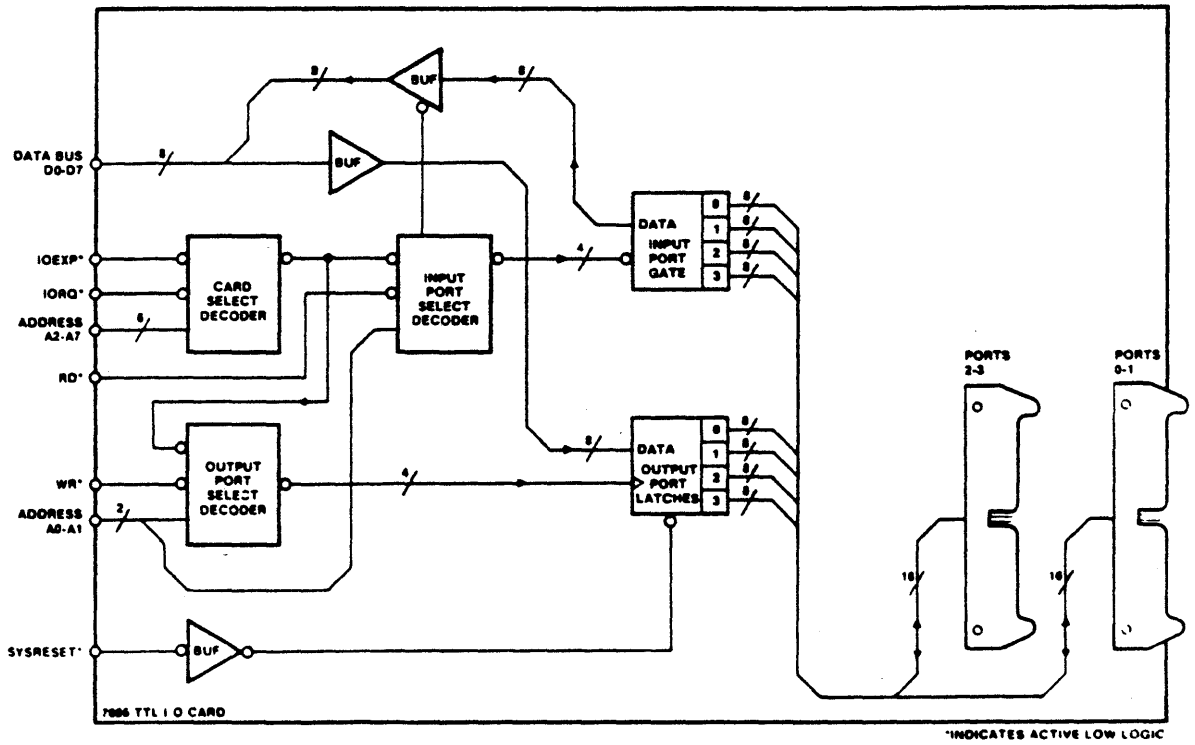


FIGURE 1

2. FUNCTIONAL DESCRIPTION

The 7605 provides 32 alternating bidirectional data and ground lines. These signal lines can be up to 10 feet (3.05M) long with proper electrical considerations. Each bidirectional line characteristic (whether input or output) is determined by the circuit shown in the Bidirectional I/O Circuit diagram.

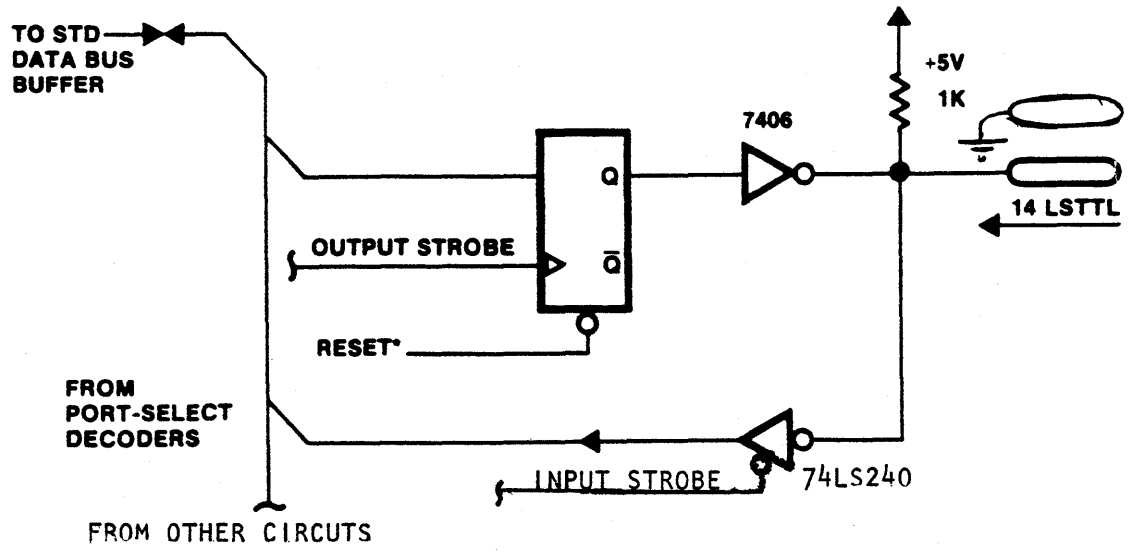
The output circuit capability is supplied through an open-collector inverting driver, and a pullup resistor. There are no programming constraints in the output mode; active high data is written to the output port causing the user interface pin to operate in the active low state.

Input circuit capability is provided through an inverting input port buffer. The Schmitt-trigger characteristic of the input port buffer removes noise-induced voltage spikes from the input signal. There is one programming constraint in the input mode: active-high data cannot be written to the output port bit that is to be used on an input port bit. This constraint is required to disable the open-collector output drive for that bit. NOTE: On system power-up the SYSRESET* signal clears the output port and places the output drivers in the disabled state. Thus programming overhead is not required to select the input mode of operation.

GENERAL PURPOSE INTERFACE

The 7605 is useful as a general purpose TTL interface card. If flat cable or twisted pair discrete wire cable assemblies are used, the ground-signal-ground of the I/O connectors minimizes crosstalk between inter-system signal lines in electrically noisy environments.

The bidirectional signal lines at the card edge connector are active-low on both input and output. The signals are terminated with a 1K pullup resistor.



Typical Bidirectional I/O Circuit

FIGURE 2

3. CARD ADDRESS MAPPING

The 7605 is selected by a decoded combination of address lines A2-A7. The user chooses the card address combination by connecting one jumper wire from SX and SY to pad matrices adjacent to U2 and U3 (see the 7605 Assembly diagram). The 7605 is shipped mapped at hex port address 00. To map the 7605 anywhere in the hexadecimal address range of 00 to FF, change the decoder outputs connected to SX and SY.

4. ADDRESS DECODER OPERATION

Refer to the schematic, Document #105778.

The 7605 uses four cascaded 74LS42 decoders (U2, U3, U5 and U6) to decode address lines A0-A7. These decoders are enabled only when IORQ* and IOEXP* are active. The WR* signal is used to gate the select strobes from U6 that control the output ports. The RD* signal is used to gate the select strobes from U5 that control the input ports.

CHANGING THE 7605's PORT ADDRESS

Refer to the Assembly diagram, Document #105779

Locate decoders U2 and U3 (74LS42) adjacent to the STD BUS edge connector. Each decoder device has a dual row of pads which form decoder output select matrices. Make one (and only one) connection to each of the matrices adjacent to U2 and U3.

The decoder jumper pads numbered as shown in Figure 3 are adjacent to the decoder chips on the 7605. Also shown are the jumpers (at X0 and Y0) which produce hexadecimal port addresses 00, 01, 02 and 03, the selections made when the card is shipped.

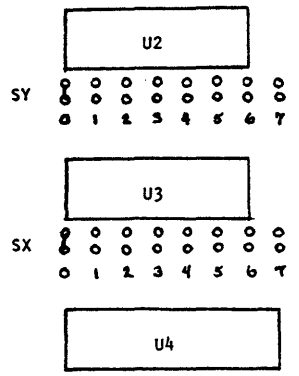


FIGURE 3 - DECODER JUMPER PAD NUMBERING

The I/O address mapping and jumper selection table for four addresses per card shows where to place jumper straps to obtain any four sequential port addresses in the hexadecimal range 00-FF. Using the lower of the 2-digit hexadecimal addresses desired, find the most significant hexadecimal address digit along the vertical axis, and the least significant hex digit on the horizontal axis. For example, port addresses 50, 51, 52 and 53 are obtained by connecting jumpers at X2 and Y4.

The only restriction that applies in address selection for the 7605 is that the lower of the four port addresses (00 as shipped) must occur only at every fourth possible address; for example, the sequence 01, 02, 03 and 04 is not allowed by the decoder.

The pad matrices adjacent to U2 and U3 are on 0.10 inch (0.25cm) centers. The jumper wires may be conveniently replaced by wirewrap post if frequent address selection changes are anticipated.

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION X & Y
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	X0 Y0				X0 Y1				X0 Y2				X0 Y3				X AND Y
1	X0 Y4				X0 Y5				X0 Y6				X0 Y7				
2	X1 Y0				X1 Y1				X1 Y2				X1 Y3				
3	X1 Y4				X1 Y5				X1 Y6				X1 Y7				
4	X2 Y0				X2 Y1				X2 Y2				X2 Y3				
5	X2 Y4				X2 Y5				X2 Y6				X2 Y7				
6	X3 Y0				X3 Y1				X3 Y2				X3 Y3				
7	X3 Y4				X3 Y5				X3 Y6				X3 Y7				
8	X4 Y0				X4 Y1				X4 Y2				X4 Y3				
9	X4 Y4				X4 Y5				X4 Y6				X4 Y7				
A	X5 Y0				X5 Y1				X5 Y2				X5 Y3				
B	X5 Y4				X5 Y5				X5 Y6				X5 Y7				
C	X6 Y0				X6 Y1				X6 Y2				X6 Y3				
D	X6 Y4				X6 Y5				X6 Y6				X6 Y7				
E	X7 Y0				X7 Y1				X7 Y2				X7 Y3				
F	X7 Y4				X7 Y5				X7 Y6				X7 Y7				

I/O Address Mapping And Jumper Selection Table For 4 Addresses Per Card

FIGURE 4

5. 7605 CARD ENVIRONMENTAL SPECIFICATIONS

RECOMMENDED OPERATING LIMITS				ABSOLUTE NON-OPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temperature	0	25	55	-40	75	^{o}C
Humidity ①	5		95	0	95	%RH

① Non-condensing

6. ELECTRICAL SPECIFICATIONS

7605 GENERAL PURPOSE TTL I/O CARD ELECTRICAL TEST SPECIFICATION

MNEM.	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NON-OPERATING LIMITS		
		MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	Volt
T_A	Free air temp.	0	25	55	-40	75	C

USER WORST CASE ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEST LIMITS

	PARAMETER	MIN	TYP	MAX	UNIT
V_{OL}	LOW LEVEL INTERFACE VOLTAGE (2)			.70	V
I_{OL}	LOW LEVEL INTERFACE CURRENT (3)			30	mA
V_{OH}	HIGH LEVEL INTERFACE VOLTAGE	4.50		5.50	V
I_{OH}	HIGH LEVEL INTERFACE CURRENT (1)	-3.5			mA

STD BUS ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEST LIMITS

	PARAMETER	MIN	TYP	MAX	UNITS
I_{CC}	SUPPLY CURRENT		605	840	mA
	STD BUS INPUT LOAD	See Figure 6			
	STD BUS OUTPUT DRIVE	See Figure 6			

(1) At 2 volt

(2) At 30mA current level

(3) At 0.70 Volt level.

AC ELECTRICAL CHARACTERISTICS

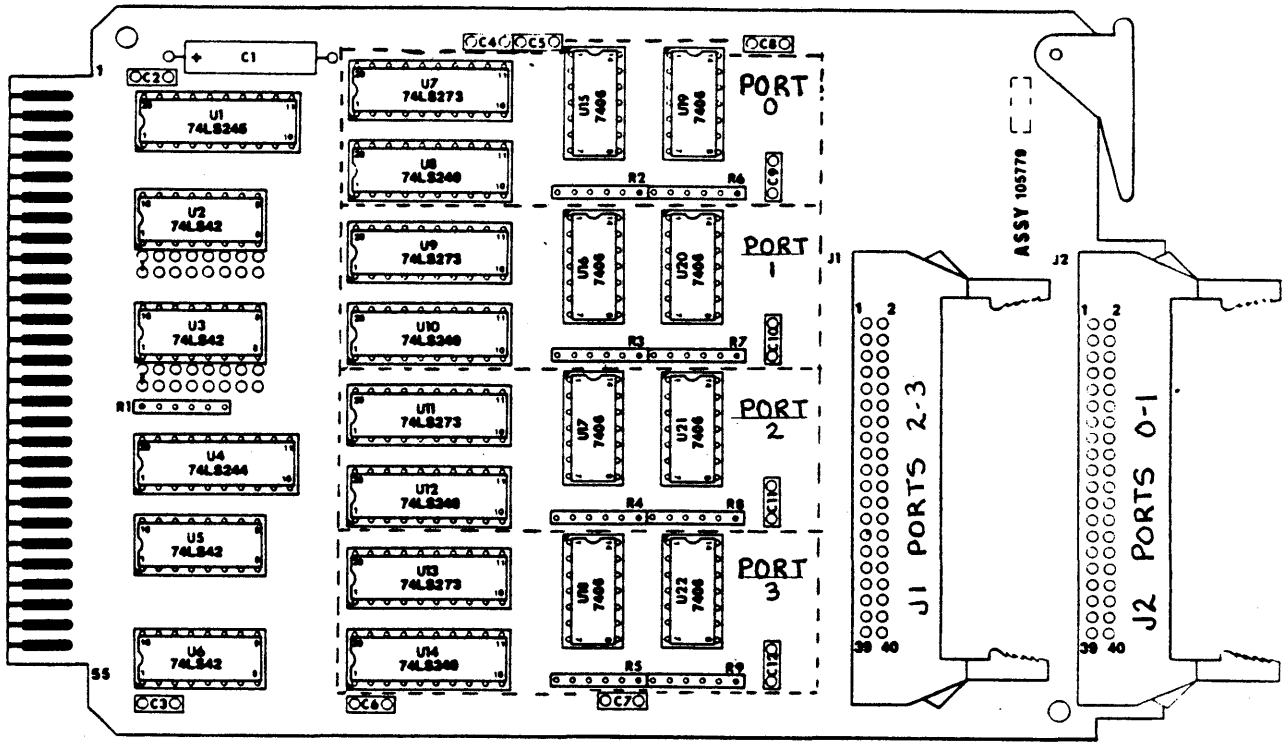
Must meet all requirements for TTL I/O cards timing as specified in the Series 7000 General Test Specification.

7. MECHANICAL

The 7605 is shipped fully populated. Power dissipation can be reduced by removing unused input or output ports by removing the ICs:

INPUT/OUTPUT PORT SELECTION		
PORT NO.	FOR ONLY AN INPUT PORT REMOVE ICs	FOR ONLY AN OUTPUT PORT REMOVE IC
PORT 0	U7, U15, U19	U8
PORT 1	U9, U16, U20	U10
PORT 2	U11, U17, U21	U21
PORT 3	U13, U18, U22	U14

Leaving the input buffers in place allows the processor to read back the output port data to check for noise alteration or to use the output port as a data register.



7605 Assembly

FIGURE 5

Refer to the Component Placement diagram for component placement information. The 7605 meets all STD BUS general mechanical specifications. The 7605 requires one card slot in a standard STD BUS card rack. The I/O connectors use low-profile, mass termination 0.25 inch square post latching connectors. Recommended flat cable card edge connectors include 3-M part number 3417-6040-1 or equivalent.

7605 USER INTERFACE CONNECTOR PIN LIST			
CONNECTOR J1		CONNECTOR J2	
PIN NUMBER		PIN NUMBER	
SIGNAL			SIGNAL
+5V	J1-2	J2-2	+5V
+5V	J1-4	J2-4	+5V
P2-7*	J1-6	J2-6	P0-7*
P2-6*	J1-8	J2-8	P0-6*
P2-5*	J1-10	J2-10	P0-5*
P2-4*	J1-12	J2-12	P0-4*
P2-3*	J1-14	J2-14	P0-3*
P2-2*	J1-16	J2-16	P0-2*
P2-1*	J1-18	J2-18	P0-1*
P2-0*	J1-20	J2-20	P0-0*
+5V	J1-22	J2-22	+5V
+5V	J1-24	J2-24	+5V
P3-7*	J1-26	J2-26	P1-7*
P3-6*	J1-28	J2-28	P1-6*
P3-5*	J1-30	J2-30	P1-5*
P3-4*	J1-32	J2-32	P1-4*
P3-3*	J1-34	J2-34	P1-3*
P3-2*	J1-36	J2-36	P1-2*
P3-1*	J1-38	J2-38	P1-1*
P3-0**	J1-40	J2-40	P1-0*

*Low Level Active

All odd numbered pins go to ground

Interface Connector Pin List

STD/7605 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)				OUTPUT (LSTTL DRIVE)			
INPUT (LSTTL LOADS) **						INPUT (LSTTL LOADS)**	
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		2	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PC1	IN		52	51		OUT	PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Low Level Active ** Designates LSTTL Loads

Edge Connector Pin List

FIGURE 6

NOTE: Vcc is provided on the user interface pins J1 and J2. These should be used only after the system designer has thoroughly studied the system implication. Care must be taken to avoid ground loops.

8. 7605 OPERATING SUBROUTINE MODULES

This section provides flow diagrams and subroutines to operate your 7605 card. These may be used intact, or used as models to construct subroutines for a specific application.

The subroutines are written in 8080-family assembly code and will execute on 8080, 8085, and Z80 processors. The memory addresses selected are compatible with Pro-Log's 7801 (8085A) and 7803 (Z80) processor cards. The 7605 port addresses used are the address jumper selections made when the 7605 is shipped.

To use these subroutines in systems other than those described above, the memory and/or I/O port addresses may require change for compatibility.

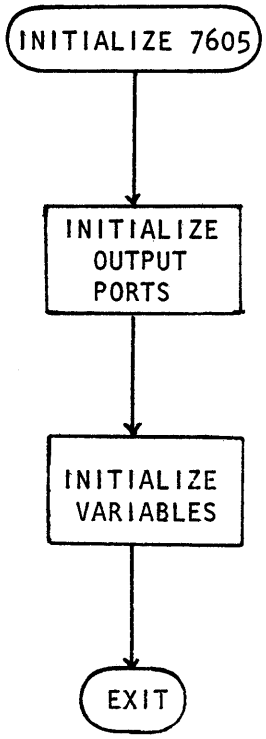
The flow diagrams presented can be easily translated into the assembly code used by any microprocessor since they show the steps required to achieve 7605 operation without reference to a particular microprocessor.

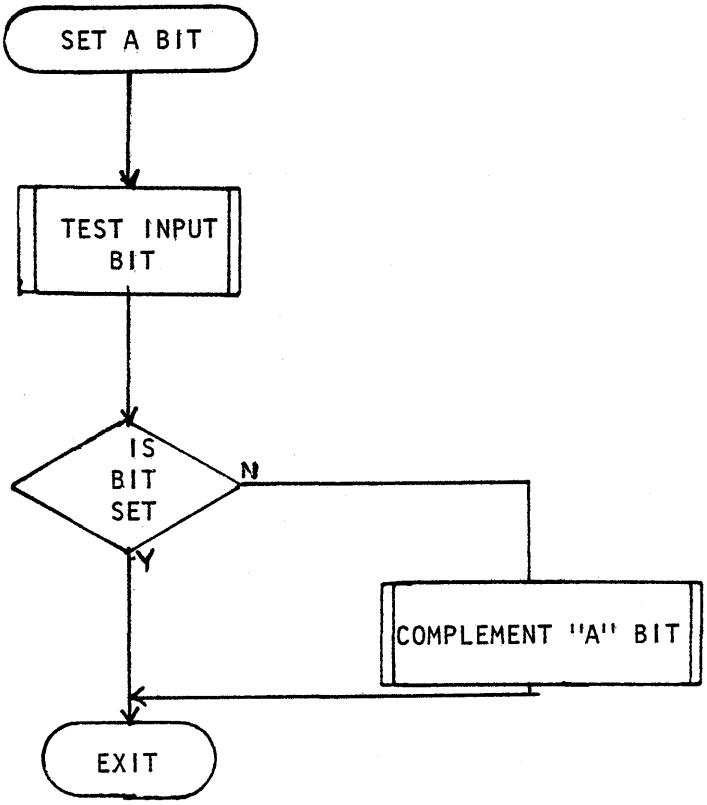
The following subroutines are written to act only on a single bit on the output or input ports. For routines which act on all 8 bits of a port at the same time, see the 7604 User's Manual.

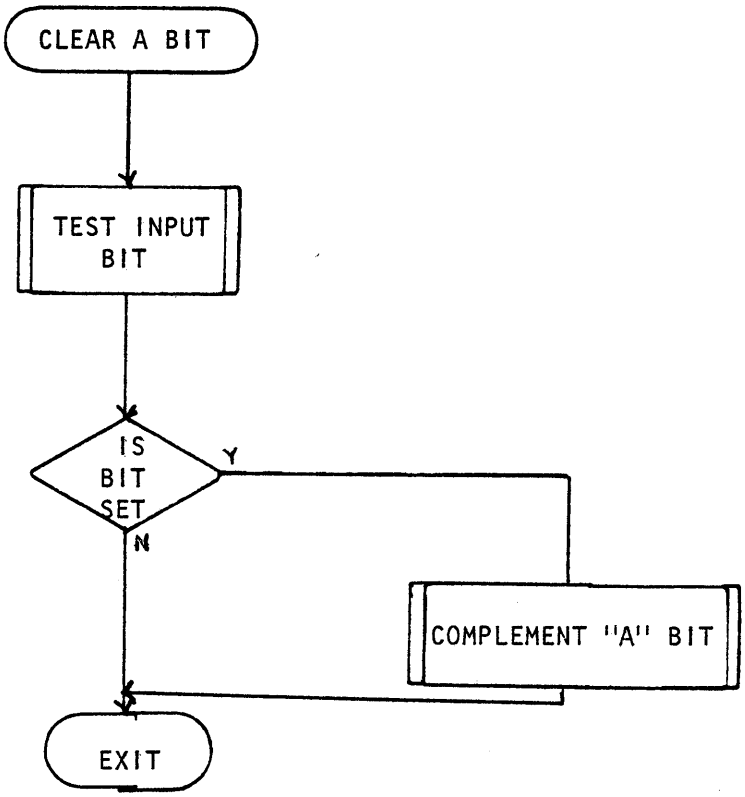
NAME AND DESCRIPTION	REGISTERS CHANGED	FLOW DIAGRAM	PROGRAM	START ADDRESS
(Initialize 7605) This subroutine sets all outputs to a predefined state. It also initializes all viariables used by the other subroutines.	A H L	PAGE	PAGE	1300
(Set bit) This routine accepts a hex value in the accumulator which corresponds to the I/O module to be turned on. If the I/O module number is out of range, the carry flag will be set.	A B C H L	PAGE	PAGE	1394
(Clear bit) This routine accepts a hex value in the accumulator which corresponds to the I/O module to be turned off. If the I/O module number is out of range, the carry flag will be set.	A B C H L	PAGE	PAGE	13A0

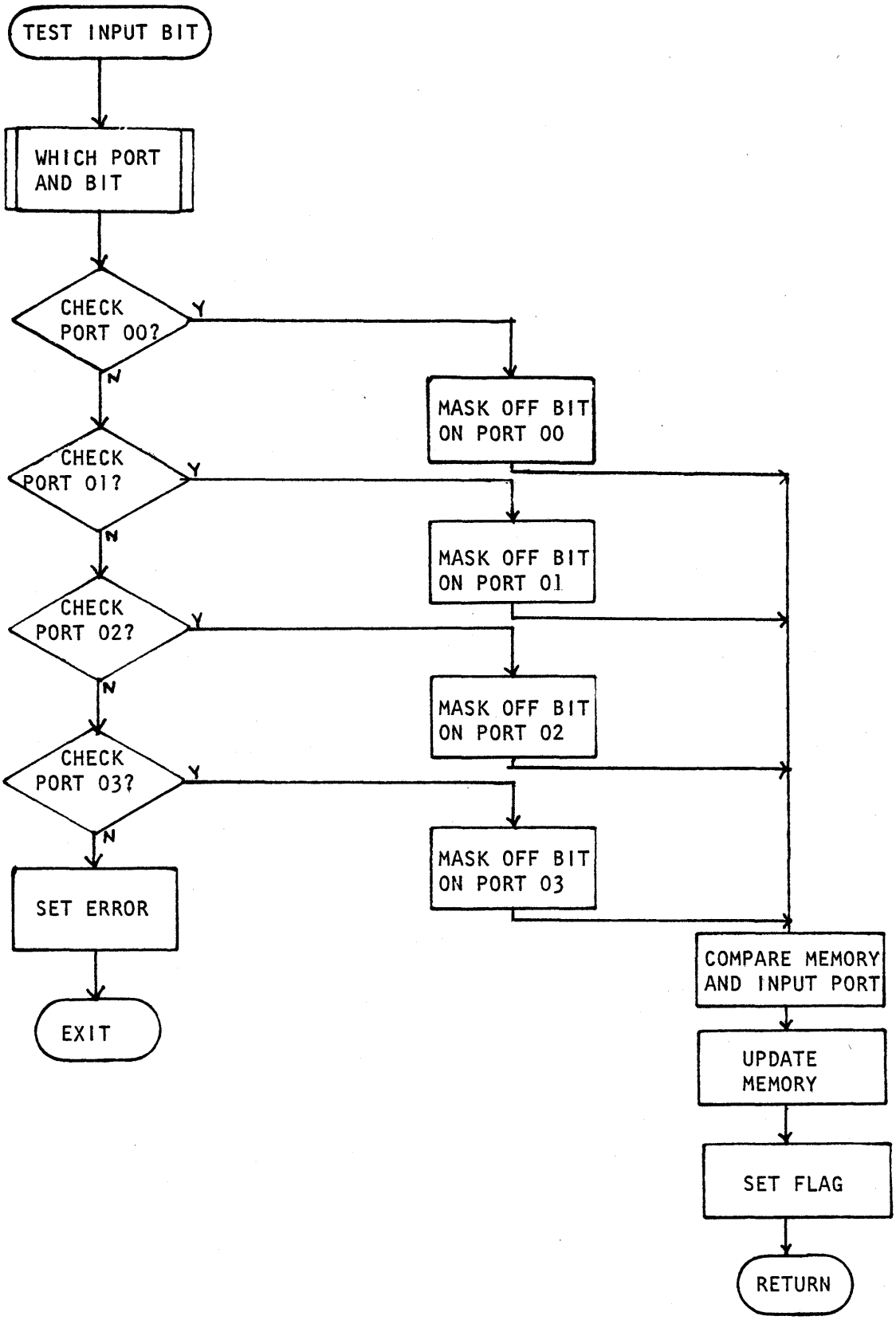
continued . . .

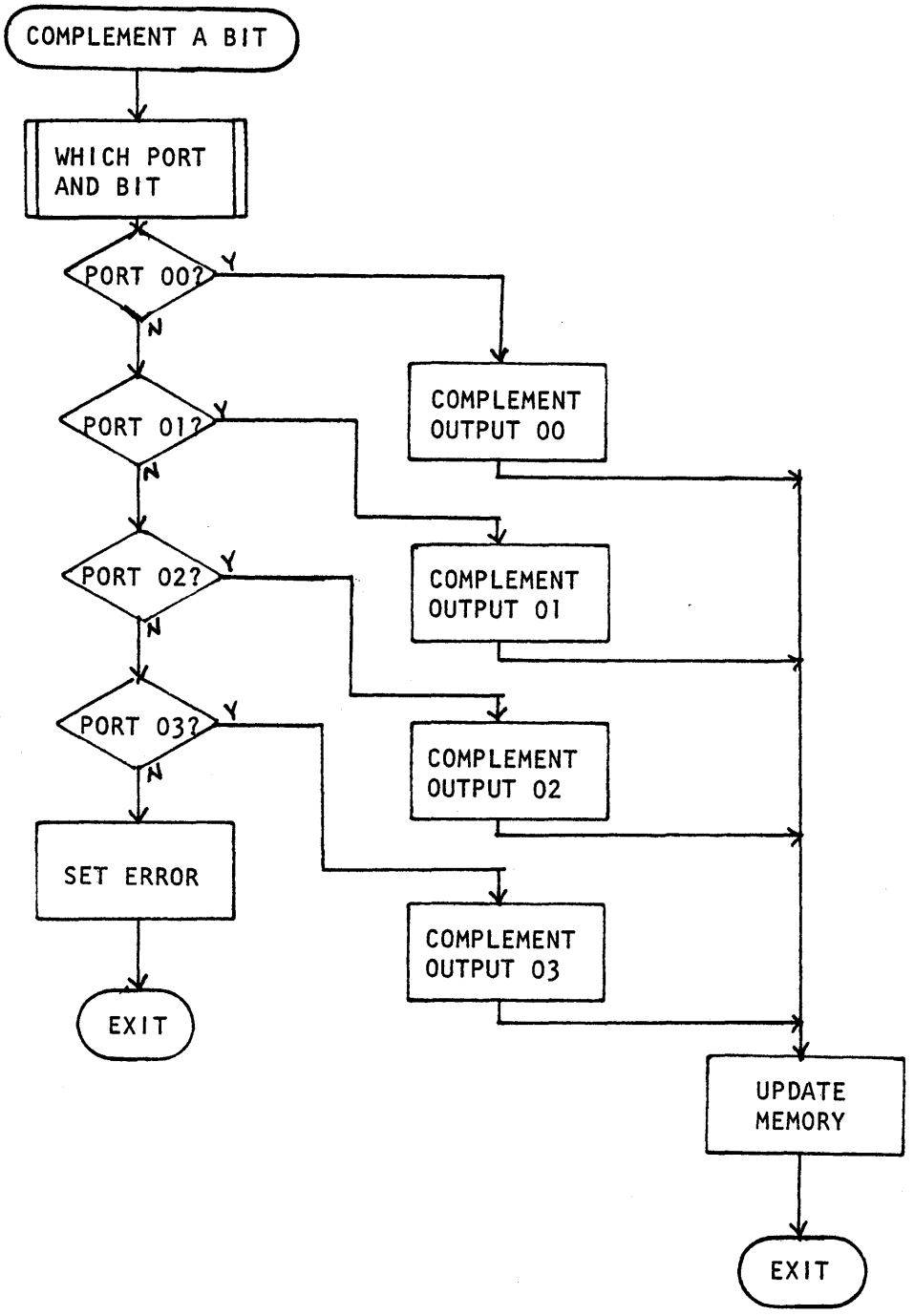
NAME AND DESCRIPTION	REGISTERS CHANGED	FLOW DIAGRAM	PROGRAM	START ADDRESS
(Test bit) This routine accepts a hex value in the accumulator which corresponds to the I/O module to be tested. If the I/O module number is out of range, the carry flag will be set. The subroutine returns with P=0 if there was no change and P=1 if the addressed module did change since the last test. The Z flag =0 if the bit is set and Z=1 if the input port is clear.	A B H L C F	PAGE	PAGE	13B0
(Complement a bit) This routine accepts a hex value in the accumulator which corresponds to the I/O module to be complemented. If the I/O module is out of range the carry flag will be set.	A B H L C	PAGE	PAGE	1342


INITIALIZE 7605
INITIALIZE OUTPUT PORTS
INITIALIZE VARIABLES
EXIT


SET A BIT
TEST INPUT BIT
IS BIT SET
N
Y
COMPLEMENT "A" BIT
EXIT


CLEAR A BIT
TEST INPUT BIT
IS BIT SET
Y
N
COMPLEMENT "A" BIT
EXIT


TEST INPUT BIT
WHICH PORT AND BIT
CHECK PORT 00?
Y
N
MASK OFF BIT ON PORT 00
CHECK PORT 01?
Y
N
MASK OFF BIT ON PORT 01
CHECK PORT 02?
Y
N
MASK OFF BIT ON PORT 02
CHECK PORT 03?
Y
N
MASK OFF BIT ON PORT 03
SET ERROR
EXIT
COMPARE MEMORY AND INPUT PORT
UPDATE MEMORY
SET FLAG
RETURN


COMPLEMENT A BIT
WHICH PORT AND BIT
PORT 00?
Y
N
COMPLEMENT OUTPUT 00
PORT 01?
Y
N
COMPLEMENT OUTPUT 01
PORT 02?
Y
N
COMPLEMENT OUTPUT 02
PORT 03?
Y
N
COMPLEMENT OUTPUT 03
SET ERROR
EXIT
UPDATE MEMORY
EXIT

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PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
	00	21	(7605)	LDPI	HL	INITIALIZE PROGRAM
	1			-	XX	
	2			-	RAM PAGE	
	3	3E		LDAI		SET PORT 00
	4				XX	
	5	D3		OPA		
	6	00		-	00	
	7	3E		LDAI		SET PORT 01
	8					
	9	D3		OPA		
	A	01		-	01	
	B	3E		LDAI		SET PORT 02
	C			-	XX	
	D	D3		OPA		
	E	02				
	0F			LDAI		SET MEMORY TO I/O PORT STATUS
	10			-	XX	
	1			OPA	/	
	2			-	03	
	3	DB		IPA		
	4	00		-	50	
	5	77		STAN	(HL)	
	6	23		ICP	(HL)	
	7	DB		IPA		
	8	01		-	51	
	9	77		STAN	(HL)	
	A	23		ICP	(HL)	
	B	DB		IPA		
	C	02		-	52	
	D	77		STAN	(HL)	
	E	23		ICP	(HL)	
	F	DB		IPA		

	20	03		-	03	
	1	77		STAN	(HL)	
	2	C9		RTS		
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	2F					
	30	4F	(WHICH LINE?)	LDC	A	← SAVE A CONVERT NUMBER IN ACCUMULATOR TO BIT POSITION
	1	3E		LDAI		BIT = A
	2	01		-	01	INITIALIZE REG A-B BIT = B
	3	06		LDBI		
	4	01		-	01	
	5	0C		ICC		← ADD 1 TO C
	6	0D	LOOP	DCC		DECREMENT # RETURN WHEN ZERO 01 FIRST PORT
	7	C8		RTS	≠1	02 SECOND PORT
	8	07		RRL		← ROTATE TO NEXT BIT POSITION 03 THIRD PORT
	9	02		JP	CO	IF CARRY IS SET INCREMENT PORT REG XX ECT
	A	26		-	LOOP	
	B	13		-		
	C	04		ICB		
	D	C3		JP	UN	
	E	26		-	LOOP	
	3F	13		-		

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PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / DATE / COMMENTS
	40			LDAI		
	1			-	XX	
	2	CD	(COMPLEMENT A BIT)	JS		CHANGE STATE OF ONE BIT
	3	30		-	(WHICH LINE?)	CALCULATE PORT AND BIT
	4	13				
	5	21		LDPI	HL	SET POINTER TO FIRST PORT
	6			-		
	7			-		
	8	05		DCB		FIND CORRECT PORT ROUTINE
	9	CA		JP	Z1	
	A	5E		-	PORT 00	
	B	13		-		
	C	23		ICP	HL	
	D	05		DCB		
	E	CA		JP	Z1	
	4F	67		-	PORT 01	
	50	13		-		
	1	23		ICP	HL	
	2	05		DCB		
	3	CA		JP	Z1	
	4	70		-	PORT 02	
	5	13		-		
	6	23		ICP	HL	
	7	05		DCP		
	8	CA		JP	Z1	
	9	79		-	PORT 03	
	A	13		-		
	B	00		NOP		
	C	37		SEC		
	D	C9		RTS		RETURN C=1 IF INVALID #
	E	47	PORT 00	LDB	A	UPDATE PORT 00
	5F	DB		IPA		

	60	00		-	00	
	1	A8		XRA	B	UPDATE PORT 00
	2	D3		OPA		
	3	00		-	00	
	4	C3		JP	UN	
	5	7F		-	(UPDATE MEMORY)	
	6	13		-		
	7	47	PORT 01	LDB	A	UPDATE PORT 01
	8	DB		IPA		
	9	01		-	01	
	A	A8		XRA	B	
	B	D3		OPA		
	C	01		-	01	
	D	C3		JP	UN	
	E	7F		-	(UPDATE MEMORY)	
	6F	13		-		
	70	47	PORT 02	LDB	A	UPDATE PORT 02
	1	DB		IPA		
	2	02		-	02	
	3	A8		XRA	B	
	4	D3		OPA		
	5	02		-	02	
	6	C3		JP	UN	
	7	7F		-	(UPDATE MEMORY)	
	8	13		-		
	9	47	PORT 03	LDB	A	UPDATE PORT 03
	A	DB		IPA		
	B	03		-	03	
	C	A8		XRA	B	
	D	D3		OPA		
	E	03		-	03	
	7F	A0	(UPDATE MEMORY)	ANA	B	← MASK ALL BUT CHANGED BIT

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PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
	80	4F		LDC	A	← SAVE CHANGED BIT IN C
	1	78		LDA	B	← COMPLEMENT B (BIT MASK)
	2	2F		CMAL		
	3	47		LDB	A	
	4	7E		LDA	M(HL)	← LOAD MEMORY DATA INTO A
	5	A0		ANA	B	← MASK OUT CHANGE BIT (LEAVE ALL OTHERS ALONE)
	6	B1		ORA	C	← OR IN CHANGE BIT
	7	77		STAN	(HL)	← STORE NEW STATUS IN MEMORY
	8	C9		RTS		
	9					
	A					
	B					
	C					
	D					
	E					
	9F					
	90					
	1					
	2			LDAI		
	3			-	XX	SET A BIT
	4	47	(SET A BIT)	LDB	A	
	5	C5		PSP	BC	CHECK IF BIT IS ALREADY SET
	6	CD		JS	(1	
	7	B0		-	(TEST A BIT)	
	8	13		-		
	9	C1		PLP	BC	
	A	D8		RTS	C1	← RETURN C=1 IF INVALID #
	B	78		LDA	B	
	C	CC		JS	Z1	IF NOT SET COMPLEMENT BIT
	D	42		-	(COMPLEMENT 9 BIT)	
	E	13		-		
	9F	C9		RTS		

	A0			LDAI		
	1			-	XX	
	2	47	(CLEAR A BIT)	LDB	A	CLEAR A BIT
	3	C5		PSP	BC	
	4	CD		JS		CHECK IF BIT IS ALREADY CLEAR
	5	B0		-	(TEST A BIT)	
	6	13		-		
	7	C1		PLP	BC	
	8	D8		RTS	C1	← RETURN C=1 IF INVALID #
	9	78		LDA	B	
	A	C4		JS	Z0	IF NOT CLEAR COMPLEMENT BIT
	B	42		-	(COMPLEMENT A BIT)	
	C	13		-		
	D	C9		RTS		
	E			LDAI		
	AF			-		
	B0	CD	(TEST A BIT)	JS		CHECK BIT STATUS CALCULATE PORT AND BIT
	1	30		-	(WHICH LINE ?)	
	2	13		-		
	3	21		LDPI	HL	SET POINTER TO FIRST PORT
	4			-		
	5			-	XX	
	6	05		DCB	RAM PAGE	FIND CORRECT PORT ROUTINE
	7	CA		JP	Z1	
	8	CC		-	PT 00	
	9	13		-		
	A	23		ICP	HL	
	B	05		DCB		
	C	CA		JP	Z1	
	D	D2		-	PT 01	
	E	13		-		
	F	23		ICP	HL	

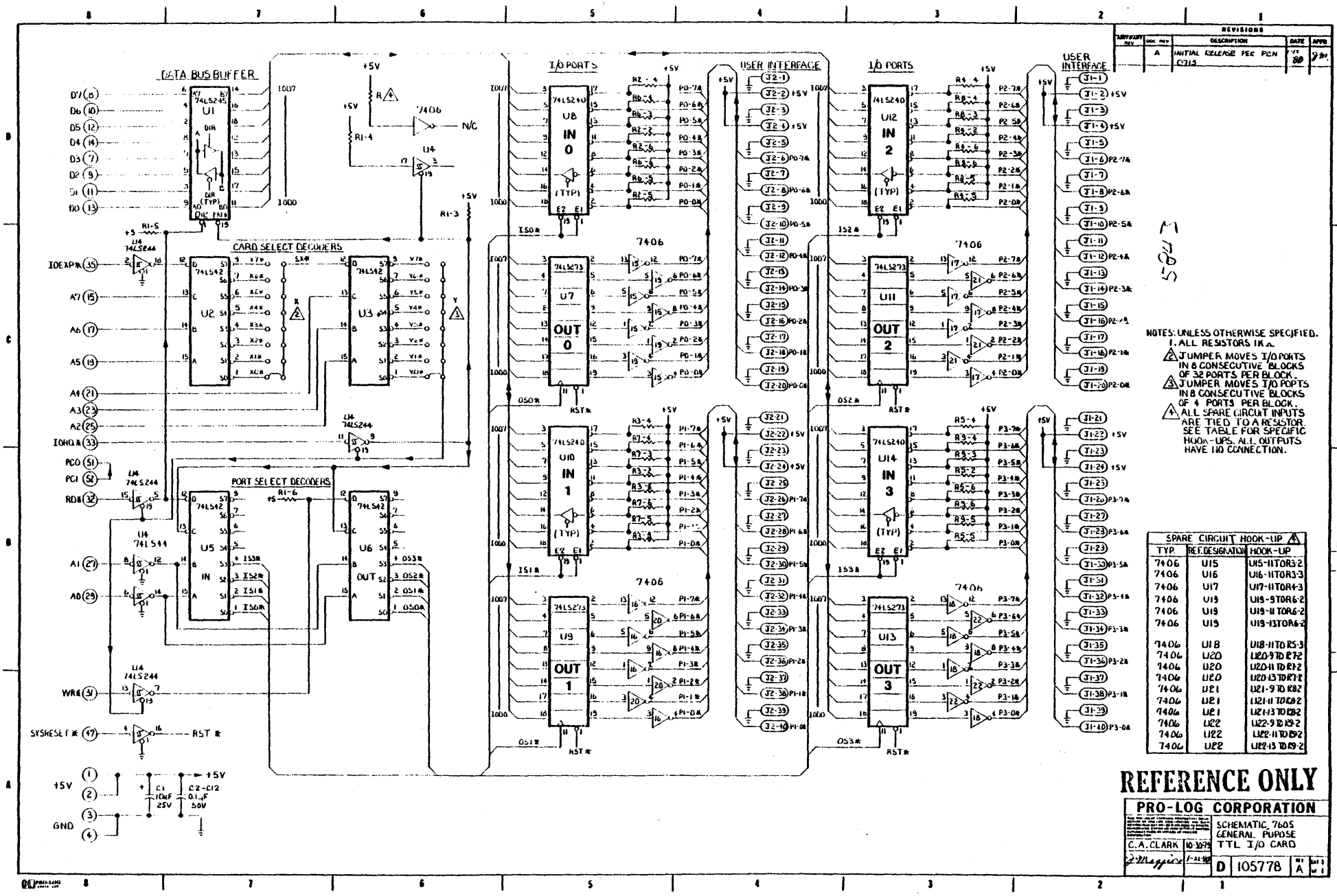
PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

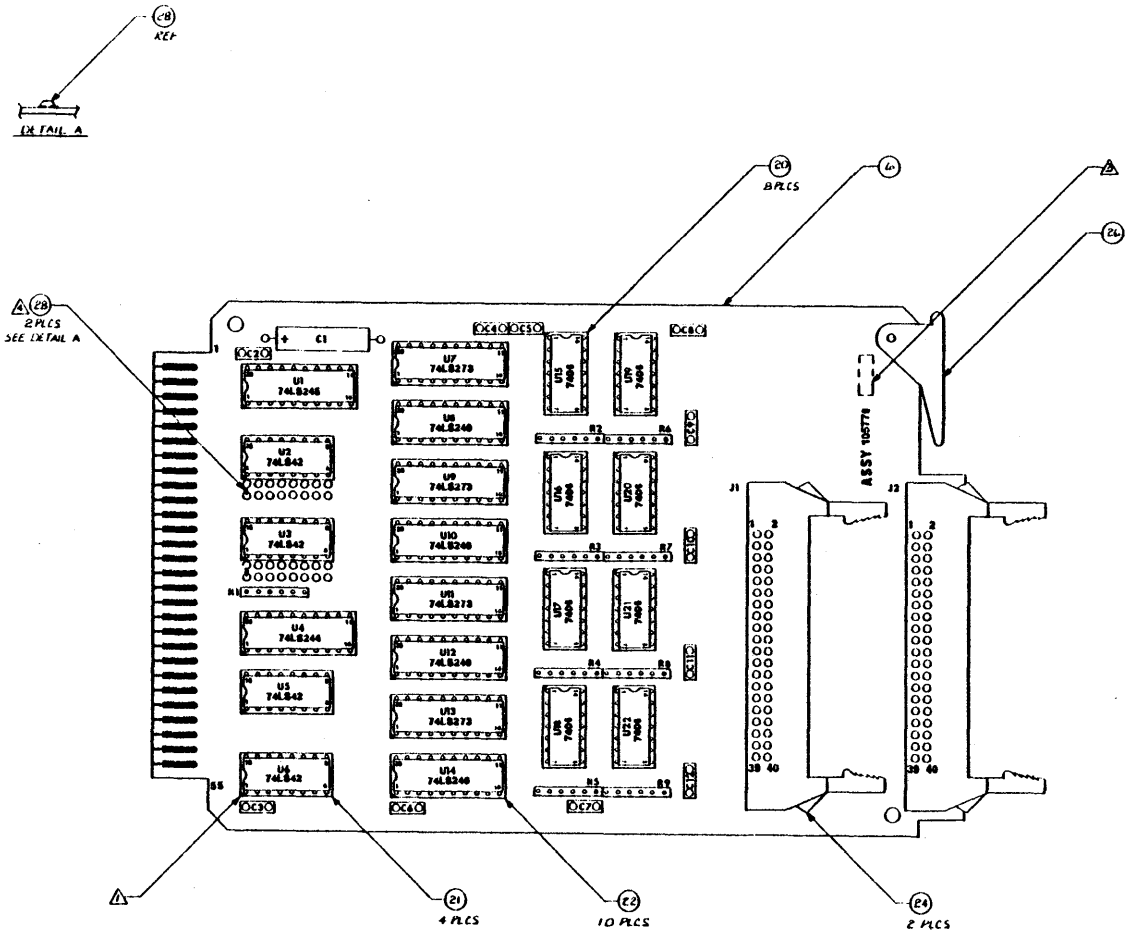
TITLE

DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
	C0	05		DCB		
	1	CA		JP	Z1	
	2	D8		-	PT 02	
	3	13		-		
	4	23		ICP	HL	
	5	05		DCB		
	6	CA		JP	Z1	
	7	DE		-		
	8	13		-	PT 03	
	9	00		NOP		
	A	37		SEC		RETURN WITH CARRY SET FOR INVALID #
	B	C9		RTS		
	C	47	PT 00	LDB	A	← SAVE MASK
	D	DB		IPA		INPUT DATA
	E	00		-	00	
	CF	C3		JP		
	D0	E1		-	CMEM	
	1	13		-		
	2	47	PT 01	LDB	A	← SAVE MASK
	3	DB		IPA		INPUT DATA
	4	01		-	01	
	5	C3		JP		
	6	E1		-	CMEM	
	7	13		-		
	8	47		LDB	A	← SAVE MASK
	9	DB		IPA		INPUT DATA
	A	02		-	02	
	B	C3		JP		
	C	E1		-	CMEM	
	D	13		-		
	E	47		LDB	A	← SAVE MASK
	DF	DB		IPA		INPUT DATA
	E0	03		-	03	
	1	A0		ANA	B	← MASK UNWANTED BITS (NEW)
	2	F5		PSP	AF	← SAVE NEW DATA AND FLAGS (Z1=BIT CLEAR Z0=BIT SET)
	3	7E		LDA	M(HL)	← LOAD OLD DATA
	4	A0		ANA	B	← MASK UNWANTED BITS (OLD)
	5	4F		LDC	A	← PUT OLD DATA IN C
	6	F1		PLP	AF	SET ACCUMULATOR AND FLAGS TO NEW DATA
	7	F5		PSP	AF	
	8	C5		PSP	BC	← SAVE OLD DATA
	9	CD		JS	UN	UPDATE MEMORY WITH PRESENT BIT STATUS
	A	7F		-	(UPDATE MEMORY)	
	B	13		-		
	C	C1		PLP	BC	PUT OLD DATA BACK IN A
	D	79		LDA	C	
	E	C1		PLP	BC	← PUT NEW DATA IN B AND FLAGS IN C (FLAG STATE=BIT STATE)
	EF	A8		XRA	B	← OLD ⊕ NEW = CHANGE Z1 = NO CHANGE Z0 = CHANGE
	F0	79		LDA	C	← PUT BIT STATE FLAG IN A
	1	F5		PSP	AF	← MOVE FLAGS TO BC
	2	C1		PLP	BC	B = BIT STATE C = CHANGES
	3	79		LDA	C	PUT CHANGE FLAG IN ACC AND ROTATE TO
	4	2F		CMAL		← COMPLEMENT FLAG SYNC BIT POSITION
	5	07		RLA		
	6	E6		ANAI		
	7	80		-	80	
	8	B0		ORA	B	← OR CHANGE FLAG AND BIT FLAG TOGETHER
	9	4F		LDC	A	← PUT FLAG IN C
	A	C5		PSP	BC	SET FLAG REG
	B	F1		PLP	AF	
	C	C9		RTS		
	D					
	E					
	FF					


DATA BUS BUFFER
CARD SELECT DECODERS
PORT SELECT DECODERS
I/O PORTS
USER INTERFACE
I/O PORTS
USER INTERFACE
7406
REVISIONS
INITIAL RELEASE PER PCN C715
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS 1K Ω.
2 JUMPER MOVES I/O PORTS IN 8 CONSECUTIVE BLOCKS OF 32 PORTS PER BLOCK.
3 JUMPER MOVES I/O PORTS IN 8 CONSECUTIVE BLOCKS OF 4 PORTS PER BLOCK.
4 ALL SPARE CIRCUIT INPUTS ARE TIED TO A RESISTOR. SEE TABLE FOR SPECIFIC HOOK-UPS. ALL OUTPUTS HAVE NO CONNECTION.
SPARE CIRCUIT HOOK-UP 4
TYP | REF.DESIGNATION | HOOK-UP
7406 | U15 | U15-11 TO R3-2
7406 | U16 | U16-11 TO R3-3
7406 | U17 | U17-11 TO R4-3
7406 | U18 | U18-9 TO R6-2
7406 | U19 | U19-11 TO R6-2
7406 | U19 | U19-13 TO R6-2
7406 | U18 | U18-11 TO R5-3
7406 | U20 | U20-9 TO R7-2
7406 | U20 | U20-11 TO R7-2
7406 | U20 | U20-13 TO R7-2
7406 | U21 | U21-9 TO R8-2
7406 | U21 | U21-11 TO R8-2
7406 | U21 | U21-13 TO R8-2
7406 | U22 | U22-9 TO R9-2
7406 | U22 | U22-11 TO R9-2
7406 | U22 | U22-13 TO R9-2
REFERENCE ONLY
PRO-LOG CORPORATION
SCHEMATIC 7605
GENERAL PURPOSE
TTL I/O CARD
C.A.CLARK
D 105778
A

REVISIONS				
ADVISORY NO.	DOC REV	DESCRIPTION	DATE	APPR
	A	INITIAL RELEASE PER PCN 0713	7-12-80	J.M.



NOTES UNLESS OTHERWISE SPECIFIED

1. DENOTES PIN 1 END OF SOCKETS
2. BOARD TO CONFORM WITH ASSEMBLY PROCEDURES AS1004
3. IDENTIFY WITH ASSEMBLY REV. LETTER USING RUBBER STAMP
4. MAPPED TO PORT 00

SCHEMATIC NO. 105778
PARTS LIST NO. 105780

REFERENCE ONLY

ITEM	DESCRIPTION	REF. DESIGNATION
11	10K NETWORK	R1-R9
10		
9	0.1uF, 50V	C2-C12
8	10uF, 25V	C1
7		
6	105776	PWB

PRO-LOG CORPORATION

ASSEMBLY, 7605 GENERAL PURPOSE TTL I/O CARD

MAKULLO 12-16-79

D | 105779 | REV A | SHT 1 OF 1

USER'S MANUAL

PRO-LOG CORPORATION

2411 Garden Road
Monterey, California 93940
Telephone: (408) 372-4593
TWX: 910-360-7082

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