RAYTHEON

TECHNICAL MANUAL

MODEL 402-2AM13 DISPLAY TERMINAL

DIDS*-400

DIGITAL INFORMATION DISPLAY SYSTEM

RAYTHEON

* A TRADEMARK OF RAYTHEON COMPANY

TECHNICAL MANUAL

for

DIDS*-400

MODEL 402-2AM13

Digital Information Display

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Prepared by

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FOREWORD

This manual is published for the information and guidance of technical personnel responsible for the installation, operation, and maintenance of the Model 402-2AM13 Display Terminal, a unit of the DIDS*-400 Digital Information Display System.

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CHAPTER 1

GENERAL INFORMATION

1-1 PURPOSE OF EQUIPMENT

The Model 402-2AM13 Display Terminal (figure 1-1) is a radio frequency (rf) shielded display device designed to provide quick-action keyboard input and visual readout of information stored or processed by a central processing unit (CPU The Display Terminal operates in one of two separate modes: transmit or receive.

In the transmit mode, display terminal operators initiate messages by operating keys on the keyboard assembly. As each character key is depressed, a visual character corresponding to the particular key is produced on the cathode ray tube (CRT) screen. Simultaneously, a digital code corresponding to the particular character enters an internal memory device. When the operator has completed composing the message, the message is coupled through self-contained interface circuits to either a modem or a CPU Input/Output (I/O) device. This readout is non-volatile, and the message remains on the screen even though the data is transmitted.

In the receive mode, digital data messages arriving from the CPU are decoded by the Display Terminal and visual characters are produced on the CRT screen. Again, the data received is simultaneously stored in a memory device; if desired, the received message may be edited and returned to the CPU. In addition to receiving actual data characters, the Display Terminal recognizes several control codes. These codes produce a message which is formatted according to the CPU's programmed directives. Depending upon the nature of the information system, received data may be edited and returned to the CPU, or destroyed after noting the displayed information.

1-2 DESCRIPTION OF EQUIPMENT

The Display Terminal is a compact, solid-state device completely self-contained in an rf shielded cabinet. All interface connections conform to interface standard MIL-STD-188B and interfacing signals enter and exit through a single connector at the rear of the unit. Data transfer between the Display Terminal and the connected I/O device is asynchronous and occurs at a rate of 1200 bits/sec (baud).

The Display Terminal uses a monoscope character generator to produce 96 separate visual characters. These characters consist of the upper and lower case alphabet, numerals 0 through 9, and several special symbols. Up to 1040 high-resolution characters can be displayed on the CRT screen at any given moment in an 80 character/line, 13-line format. Extensive editing and cursor control increases operational flexibility by allowing operators to rapidly revise and update the information, correct errors, or arrange transmitted data messages in a particular format. All composition and editing of data messages is accomplished off-line; the Display Terminal is connected to the CPU only during the actual transfer of information.

Figure 1-1. Model 402-2AM13 Display Terminal

The Display Terminal consists of the following major circuits and components:

a. Keyboard Assembly A11

b. Display Logic Board A13

c. Communications Control Board A12

d. Timing and Discrete Board A14

e. Delay Line Electronics A9

f. Delay Line A15

g. Monoscope Deflection Amplifier Assembly A3

h. Video Preamplifier Assembly A7

i. Video Amplifier Assembly A8

j. Vertical and Horizontal Deflection Amplifier Assembly A2

k. Low Voltage Power Supply A4

l. High Voltage Power Supply A5

m. High Voltage Network Assembly A6

n. Monoscope V1

o. Cathode Ray Tube V2

1-2.1 Keyboard Assembly A11

The keyboard assembly (figure 1-2) provides a means of initiating and editing data messages, and controlling various display terminal operations. The 74 keys are arranged in an essentially USA Standard keyboard layout and have touch characteristics similar to a high-quality electric typewriter. Control keys are centralized at the right and left edges of the keyboard to prevent their unintentional depression during message composition. Noise-free operation is provided by magnetically actuated reed switches which enable current flow through a specific branch of a self-contained diode matrix. The code produced by the depression of a character key is used internally to produce a corresponding visual character on the CRT screen and externally to form a specific character of the transmitted message. In addition to the standard keys used for composing messages, the keyboard contains many special function keys. These keys (such as END, XMIT, ERASE MSG) are used for editing or control purposes.

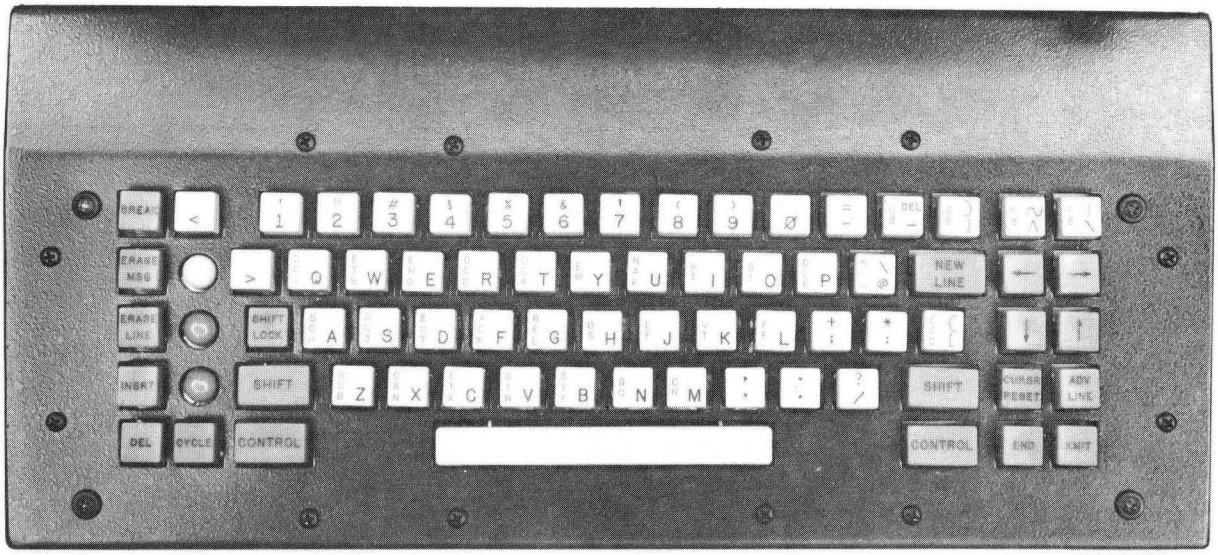


Figure 1-2. Model 402-2AM13 Keyboard

1-2.2 Display Logic Board A13

The display logic board (see figure 1-3) is a hinged printed-circuit board located on the right side of the Display Terminal. Logic circuits contained on this board are formed by transistor-transistor-logic (T^2L) integrated circuits which are solder-connected to etched-copper printed circuits. The primary function of these circuits is to act as a keyboard interface by accepting 7-bit digital codes from the keyboard matrix. These coded characters are then transferred to the delay-line electronics and the monoscope deflection amplifier circuitry. In addition, numerous flip-flops on the display logic board are used to accomplish the various editing functions (such as step-left, step-right, erase line).

1-2.3 Communications Control Board A12

The communications control board (see figure 1-3) is a hinged printed-circuit board located on the right side of the Display Terminal. Logic circuits contained on this board are formed by T^2L integrated circuits which are solder-connected to etched-copper printed circuits. The primary function performed by the communications control logic is to provide a three-character buffer storage for smoothly releasing data at the 1200-baud rate. Steering logic and decode circuits contained on this board determine whether the Display Terminal is in the transmit or the receive mode of operation.

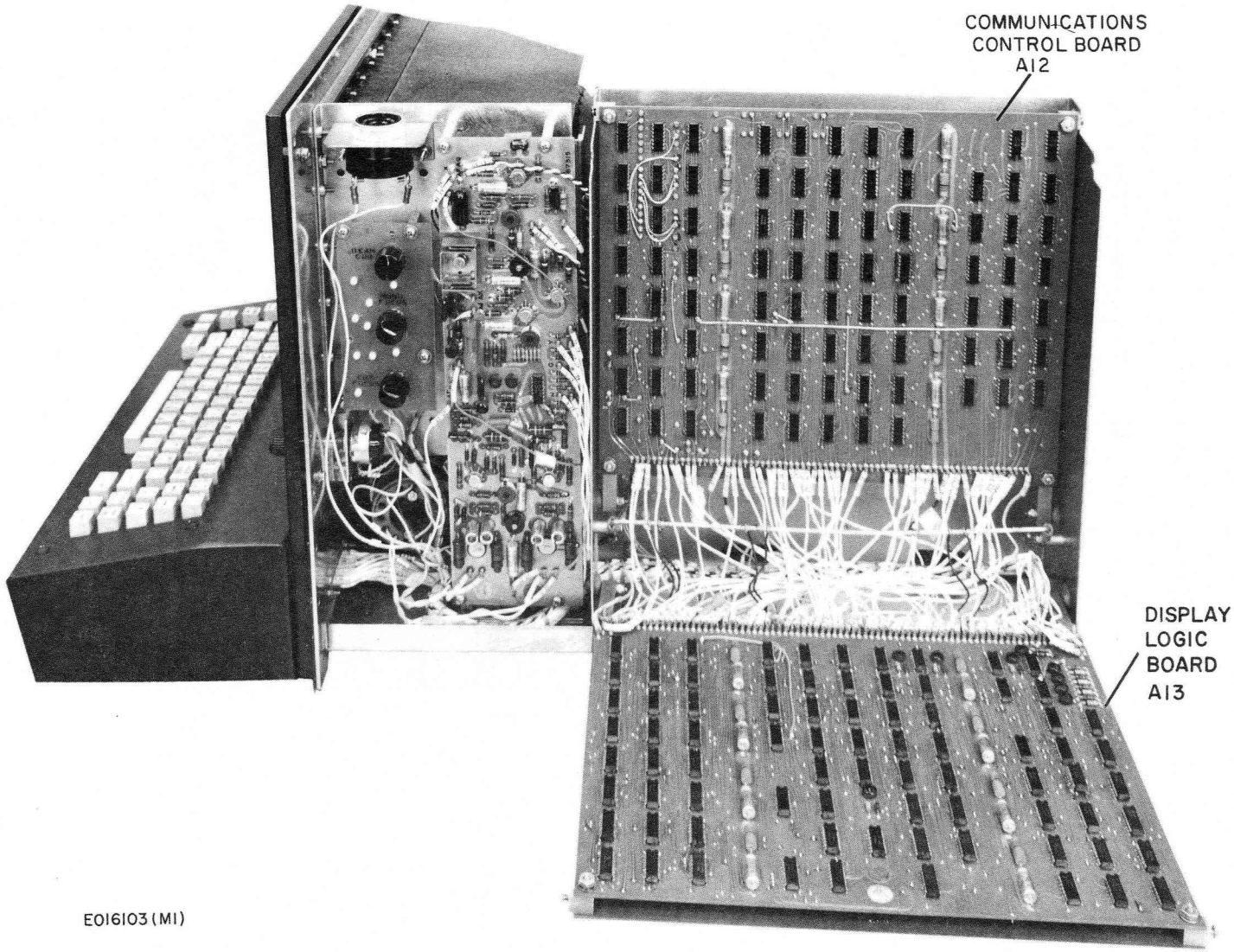


Figure 1-3. Model 402-2AM13 Display Terminal, Right Side with Boards Open

1-2.4 Timing and Discrete Board A14

The timing and discrete board (figure 1-4) is a hinged printed-circuit board located on the right side of the Display Terminal. The circuits contained on the board perform a two-fold function: internal timing, and I/O signal interface.

The internal timing circuits consist of oscillators and counters which produce timing signals for: (1) controlling data to and from the Display Terminal (1200 Hz), (2) special functions (3 Hz and 6 Hz), (3) gating data within the Display Terminal, and (4) providing horizontal and vertical drive pulses.

The modem interface circuits consist of two receivers and two transmitters which amplify and level shift input and output interfacing signals.

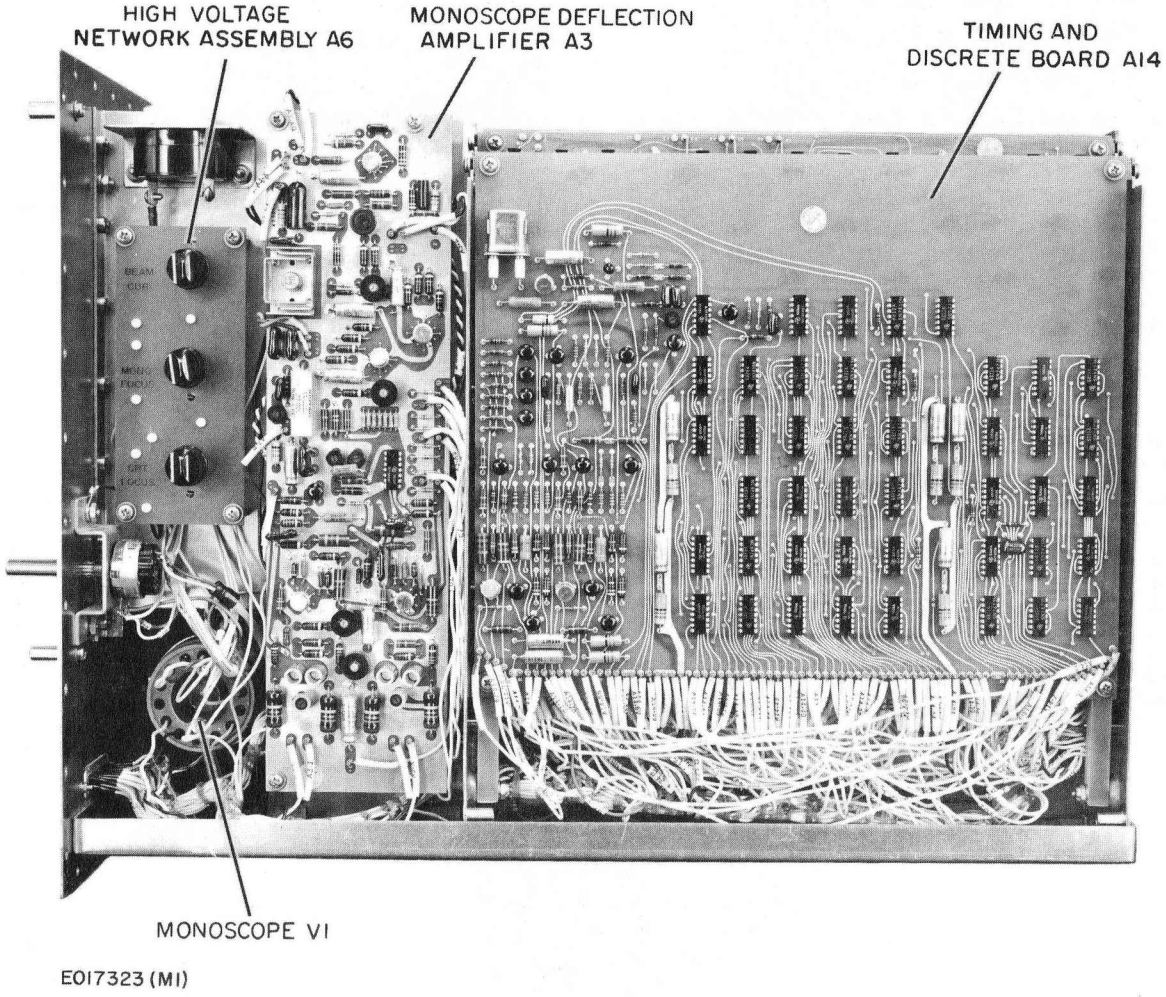


Figure 1-4. Model 402-2AM13 Display Terminal, Right View

1-2.5 Delay-Line Electronics A9

The delay-line electronics board (see figure 1-5) consists of two identical read-write amplifier circuits. These amplifiers amplify data coupled to and from the delay-line sections to compensate for any delay-line attenuation encountered by the data bits.

1-2.6 Delay Line A15

The delay line (see figure 1-5) functions as an internal memory device for storing up to 1040 seven-bit data characters and retrace characters. Data characters circulating in the delay line are used to refresh the screen presentation every 16 ms (refresh-memory loop). The delay line also provides a storage capability for holding data characters during message composition for later transmission to the CPU.

Delay line A15 consists of two magnetostrictive delay-line sections which are series-connected between the read-write amplifiers on delay-line electronics board A9. The 1040 maximum character storage capacity (plus retrace) corresponds to the maximum number of displayable characters on the display terminal CRT screen.

1-2.7 Monoscope Deflection Amplifier Assembly A3

The monoscope deflection amplifier (figure 1-4) is used to convert digital codes to analog voltages for positioning the monoscope beam to a specific character. Seven-bit digital codes are coupled from the display logic board and converted to produce two analog voltage outputs. These analog voltages are then amplified and applied to X and Y deflection plates for electrostatically deflecting the monoscope beam to a specific character on the monoscope target.

1-2.8 Monoscope V1

The monoscope (see figure 1-4) provides a means of developing visual characters for display on the CRT screen. The monoscope font consists of 96 individual characters (numerals, letters, and symbols) which are etched onto the face of the monoscope. The electron beam is directed to a character by means of X and Y deflection voltages developed by the deflection amplifiers. As the beam scans a character, an output is produced by secondary emission. This video signal is then amplified and applied to the CRT for display.

1-2.9 Video Preamplifier A7

The video preamplifier circuit (figure 1-6) accepts relatively low-level video from the monoscope target and amplifies this video to a level suitable for driving the video amplifier.

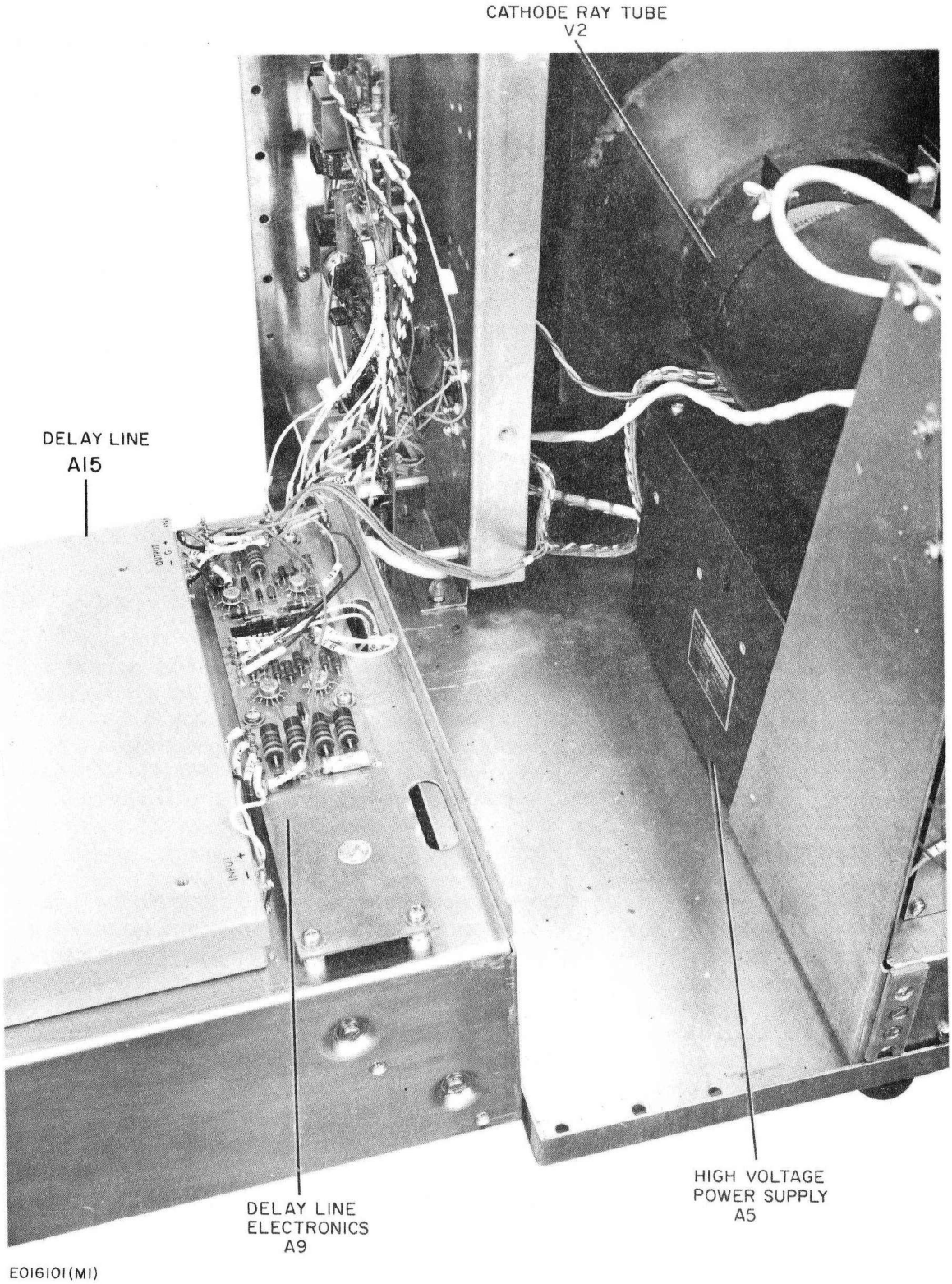


Figure 1-5. Model 402-2AM13 Display Terminal, Left Oblique Rear View with Logic Drawer Removed

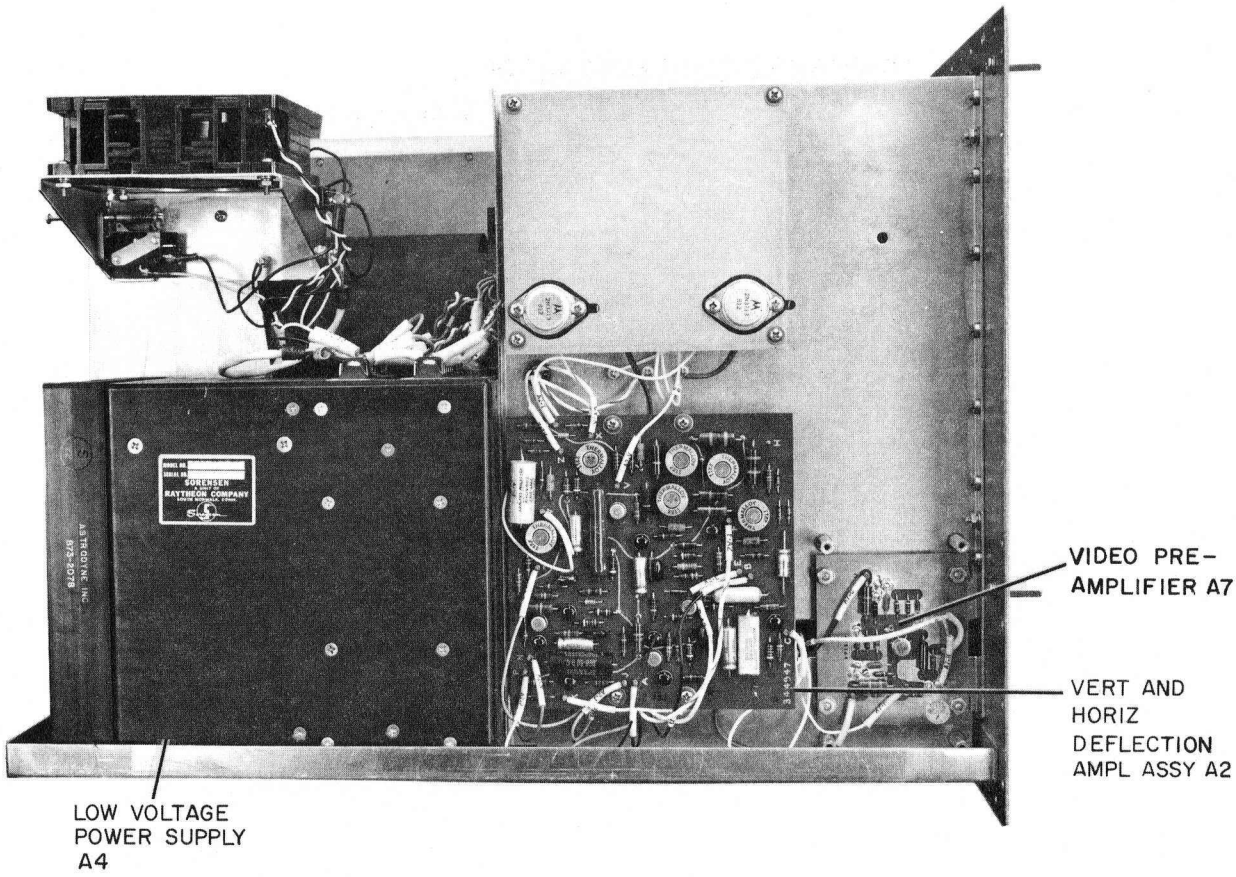


Figure 1-6. Model 402-2AM13 Display Terminal, Left View

1-2.10 Video Amplifier A8

The video amplifier (figure 1-7) accepts the amplified video output of the preamplifier and amplifies the video signal to a level suitable for driving the CRT cathode element. In addition to amplifying video signals, the video amplifier is responsible for blanking (cutting off) the CRT screen during horizontal and vertical retrace. This prolongs the life of the CRT and provides a clearer display presentation.

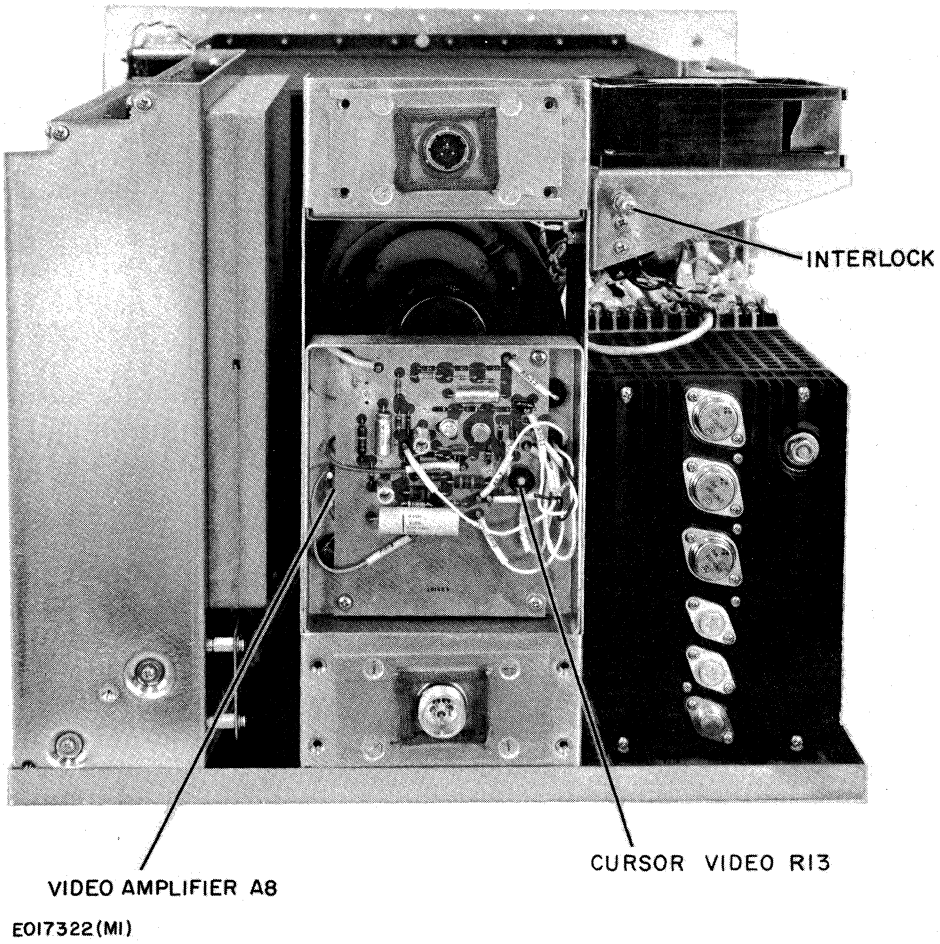


Figure 1-7. Model 402-2AM13 Display Terminal, Rear View

1-2.11 Vertical and Horizontal Deflection Amplifier Assembly A2

The vertical and horizontal deflection amplifier assembly (see figure 1-6) produces sweep voltages for scanning the CRT screen. Vertical and horizontal drive signals are developed by the timing circuits on timing and discrete board A14. These drive signals are amplified by the deflection amplifier and two outputs are produced: vertical and horizontal sweep signals. The horizontal sweep signal causes the CRT electron beam to scan from left to right across the screen. The vertical sweep signal causes the CRT electron beam to scan from the top of the screen to the bottom. This electromagnetic deflection is accomplished by the vertical and horizontal windings of a deflection coil (yoke) mounted on the CRT neck between the cathode and anode elements.

1-2.12 Low Voltage Power Supply A4

The low voltage power supply (see figure 1-6) is a solid-state, fully regulated, ac-to-dc converter. The low voltage outputs are: +5 vdc, +22 vdc, -22 vdc, +100 vdc, 6 vac (isolated), and 6 vac (nonisolated). These voltages are used for the following functions:

LV Output	Function
+5 vdc	Display logic
+22 vdc and -22 vdc	High voltage power supply input, interface circuits and sweep circuits
+100 vdc	Power (driver) transistors
6 vac, isolated	Monoscope filament
6 vac, nonisolated	CRT filament

1-2.13 High Voltage Power Supply A5

The high voltage power supply (see figure 1-5) is a solid-state, fully regulated, dc-to-ac-to-dc converter. The high voltage outputs consist of: +500 vdc, -1200 vdc, and +12 kvdc. These voltages are used for the following functions:

HV Output	Function
-1200 vdc	Monoscope cathode
+500 vdc	Monoscope and CRT acceleration
+12 kvdc	CRT anode

1-2.14 Cathode Ray Tube (CRT) V2

The CRT indicator (see figure 1-1) provides a 6-1/2 by 8-1/2 inch viewing surface for displaying a message of up to 1040 characters. The CRT screen is coated internally with a P31 (green) phosphor which emits light when scanned by the electron beam. When refreshed at a 63-Hz refresh rate, the CRT provides a flicker-free character presentation. A close-mesh screen stretched across the face of the screen cancels the effects of rf radiation and permits viewing in a lighted room without noticeable reflections.

1-3 INFORMATION AND REFERENCE TABLES

The following pages contain tables which consolidate important reference data on the Model 402-2AM13 Display Terminal. The information contained in these tables is useful for installation planning and should be referenced before any changes are made at existing installations.

1-3.1 Leading Particulars

Table 1-1 lists the leading particulars of the Display Terminal. The information contained in this table should be referenced during initial planning to determine the operating requirements of the Display Terminal.

Table 1-1. Leading Particulars

Primary Power Requirements	105 to 125 vac, 50 to 60 Hz, single phase
Power Dissipation	150 W
Environmental Conditions:	
Temperature Range	50° to 100°F
Humidity Range	10 to 90% (relative)
Dimensions:	
Height	15-1/2 in.
Width	17-1/2 in.
Depth	27 in.
Weight	135-1/2 lb

1-3.2 Capabilities and Limitations

Table 1-2 lists the capabilities and limitations of the Display Terminal.

Table 1-2. Capabilities and Limitations

Purpose of Equipment	Provides quick-response on-line communication with a central processing unit (CPU)
Mode of Operation	Half-duplex
Transmission Mode	Asynchronous
Conversational Mode	Enquiry-Response or Polling
Transmission Rate	1200 baud
Reception Rate	1200 baud
Character Code	ASCII
Display Presentation	1040 characters maximum arranged in 13 lines of 80 characters each
Character Refresh Rate	63 refresh-cycles/sec
Character Format	10 bits/char.
Parity	Even
Displayable Characters	96, including numerals, upper and lower case alphabetical, and special symbols

1-3.3 Wiring Options

Table 1-3 lists and defines the design options available for changing the operating characteristics of the Display Terminal.

Table 1-3. Wiring Options

Conversational Mode	Enquiry-Response or Polling
Broadcast Address	The Display Terminal recognizes an address character other than its own. This option permits the CPU to broadcast to two or more Display Terminals simultaneously.
Frame Reset at End of Transmit	The cursor is frame reset at the end of a transmit sequence instead of being advanced to the first character position of the next line.
One-Step Transmit	Two options are available: 1) Depressing the END key inserts an ETX code, then frame resets the cursor and raises the Request-to-Send line. 2) Depressing the END key inserts an ETX code and then moves the cursor to the first character position of the line it is on and initiates automatic transmission to the ETX.
End-of-Transmission Character	An EOT character code (0000100) is substituted for the ETX character code (0000011). This option is usually employed in polling sites where EOT signifies the end of transmission from the site.
Advance Line After Receive	When an ETX character is decoded in a received message, the cursor is automatically advanced to the first character position of the next line.
Nonblinking Cursor	A nonblinking cursor in the form of a backward L (⌋) may be displayed rather than the standard DIDS-400 blinking cursor (☰).

1-3.4 Glossary of Terms

Throughout this manual, mnemonic words or symbols are used instead of cumbersome words or phrases, so that sentences can be shortened and long, repetitious phrases eliminated. Table 1-4 is an alphabetical listing of these mnemonic abbreviations and their definitions. Where applicable, the common name of the word is used for ease in reading the text and logic diagrams.

Table 1-4. Glossary of Terms

Mnemonic Word or Symbol	Meaning	Definition
BA		Transmitted data line which couples serial bit data from the display terminal to connected CPU I/O device or modem
baud		Bits/sec
BB		Received data line which couples serial bit data from the CPU I/O device to the Display Terminal
BB1	Busy Bit One	A flip-flop that reflects the status (full, not full) of buffer register D1
BB2	Busy Bit Two	A flip-flop that reflects the status (full, not full) of buffer register D2
BB3	Busy Bit Three	A flip-flop that reflects the status (full, not full) of buffer register D3
BEL	Bell	An ASCII control code which causes an audible alarm to be sounded
BS	Back Space	An ASCII control code which steps the cursor one position to the left.
CA		Request-to-Send line
CAN	Cancel	An ASCII control code which erases all characters from the cursor position to the end of the display terminal screen

Table 1-4. Glossary of Terms (Cont)

Mnemonic Word or Symbol	Meaning	Definition
CB		Clear-to-Send line
CCC F/F	Communication Control Code Flip-flop	A flip-flop used to indicate that a control code has been received and the edit or cursor control function is in progress
CF		Data Carrier Detector line
CFR	Cursor Frame Reset	A pulse which resets the cursor to the first character, first line position of the display terminal screen.
CPU	Central Processing Unit	A centralized computer that forms the heart of the digital display system
CR	Carriage Return	An ASCII control code which moves the cursor to the first character position of the next line on the display terminal screen.
CRQ	Cursor Right Request	A pulse used to automatically step the cursor one character slot to the right. CRQ is developed each time a character is read into or out of the delay line.
CTS	Cursor Time Slot	First bit of a character in memory. This bit slot will contain the cursor if a cursor is attached to the character. CTS is also a bit counter output which is coincident with the first bit of a character
CTS +1	Cursor Time Slot Plus One Bit	Least significant bit (first data bit) of a character

Table 1-4. Glossary of Terms (Cont)

Mnemonic Word or Symbol	Meaning	Definition
Cursor		A cursor (_) used as a reference point on the Display Terminal screen and in memory.
Cursor -1		Cursor position on the screen or in memory minus one character position (the character that precedes the cursor)
DA	Device Address	A 7-bit address code assigned to any device
DC1	Device Control One	An ASCII control code which erases all visual characters between the cursor position and the end of the line
DC3	Device Control Three	An ASCII control code which steps the cursor to the same character position of the previous line
DL	Delay Line	An internal memory device which stores up to 1040 characters for display on the display terminal screen.
EOL	End of Line	A timing pulse which is present when the display terminal scan has reached the end of a line.
EOT	End of Transmission	A character (optionally provided) that signifies the end of transmission from a particular site.
ENQ	Enquiry	An ASCII control code that causes a transmit operation to be initiated.
ESC	Escape	An ASCII control code that conditions the Display Terminal to store the next character of the message

Table 1-4. Glossary of Terms (Cont)

Mnemonic Word or Symbol	Meaning	Definition
ETX	End of Text	The last character of a message
ETXD3	End of Text in D3	A decoded output that is present when an ETX character is detected in buffer register D3
ETXSR	End of Text in Shift Register	A decoded output that is present when an ETX character is detected in the character entry register.
FF	Form Feed	An ASCII control code which resets the cursor to the first character position of the first line.
F/F	Flip-flop	
FNCT COM	Function Complete	An output which is present when an editing or control function is completed
F(Δ)	Frame Pulse	A pulse that occurs when 1040 characters have been counted by the line and character counters; it is coincident with the CTS of the first character of the first line
H DRIVE	Horizontal Drive	Pulses used to develop a sweep voltage for moving the CRT beam across the screen
HT	Horizontal Tab	An ASCII control code that steps the cursor one character position to the right
INTERLK	Interlock	An output from the keyboard which is present each time a character key is depressed

Table 1-4. Glossary of Terms (Cont)

Mnemonic Word or Symbol	Meaning	Definition
I/O	Input/Output	Any device or circuit that provides an input signal or output load
LF	Line Feed	An ASCII control code which advances the cursor to the first character position of the next line
LFD3	Line Feed in D3	A decoded output which is present when an LF character is present in buffer register D3.
LSB	Least Significant Bit	Lowest order bit of a character (b_1)
LWL	Last Word of Line	A pulse that occurs during CTS of the last character of each line
MEM DATA	Memory Data	Data line which couples serial bit data from the delay line to the character entry register
MSB	Most Significant Bit	Highest order bit of a character (b_7)
MR	Master Reset	A logic level that resets the Display Terminal logic
$\overline{\text{PAR}}$	Not Parity	A decoded timing output which indicates when the count corresponding to the parity bit (b_{10}) has been reached
PE	Parity Error	A logic level that goes high when a parity error is detected during the receive mode
R	Receive	During receive, R goes high to enable the receive steering logic.

Table 1-4. Glossary of Terms (Cont)

Mnemonic Word or Symbol	Meaning	Definition
RE	Receive Enable	A decode output which goes high when certain characters (STX and DA) are recognized by the start of text and address decodes
SDL	Shift (to or from) Delay Line	A flip-flop that is set to enable a serial data transfer to (receive) or from (transmit) the delay line
SG12	Shift Gate One-to-Two	A flip-flop that is set to enable a serial data transfer from buffer register D1 to buffer register D2.
SG23	Shift Gate Two-to-Three	A flip-flop that is set to enable a serial data transfer from buffer register D2 to buffer register D3
$\overline{STP}$	Not Stop	A negative going pulse that is in coincidence with the stop bit of each 10-bit asynchronous character
$\overline{STT}$	Not Start	A negative going pulse that is in coincidence with the start bit of each 10-bit asynchronous character.
STX	Start-of-Text	First character of any message
T	Transmit	During transmit, T goes high to enable the transmit steering logic
V DRIVE	Vertical Drive	Pulses used to develop a sweep signal for moving the CRT beam downward (vertical sweep)
VT	Vertical Tab	An ASCII control code which steps the cursor down to the next line

Table 1-4. Glossary of Terms (Cont)

Mnemonic Word or Symbol	Meaning	Definition
$\overline{\text{XMT}}$ or $\overline{\text{XMIT}}$	Not Transmit	A negative going pulse present each time the XMIT key is depressed
XBITI	Extra Bit One	An output line from the keyboard used in conjunction with the SHIFT key output line
XBITII	Extra Bit Two	An 'extra' output line from the keyboard used in conjunction with the SHIFT key output line
4 CTS	Phase 4 of Cursor Time slot plus 1	A pulse that occurs when the timing outputs Ø4 and CTS are present in coincidence
1 (CTS +1)	Phase 1 of Cursor Time slot plus 1	A pulse that occurs when the timing outputs Ø1 and CTS + 1 are present in coincidence.
3 (CTS +1)	Phase 3 of Cursor Time slot plus 1	A pulse that occurs when the timing outputs Ø3 and CTS +1 are present in coincidence
4 (CTS +1)	Phase 4 of Cursor Time slot plus 1	A pulse that occurs when the timing outputs Ø4 and CTS +1 are present in coincidence
ØA	Phase A Clock	The output of the 1200-baud clock
Δ	First Word of Line Pulse	CTS of the first character; first line.

CHAPTER 2

INSTALLATION AND PREOPERATION

2-1 SITING REQUIREMENTS

2-1.1 Location

The Model 402-2AM13 Display Terminal may be installed in any location that conforms to the environmental conditions specified in table 1-1. The Display Terminal is normally installed in an operations area on a sturdy desk, table or counter capable of supporting the weight of the equipment. The CRT screen presentation may be varied in brightness by using a convenient brightness control; thus, the Display Terminal can be installed in any location regardless of room lighting. An outline dimension drawing of the Display Terminal is shown in figure 2-1. The equipment requires approximately 485 square inches of table surface area and weighs 135-1/2 pounds.

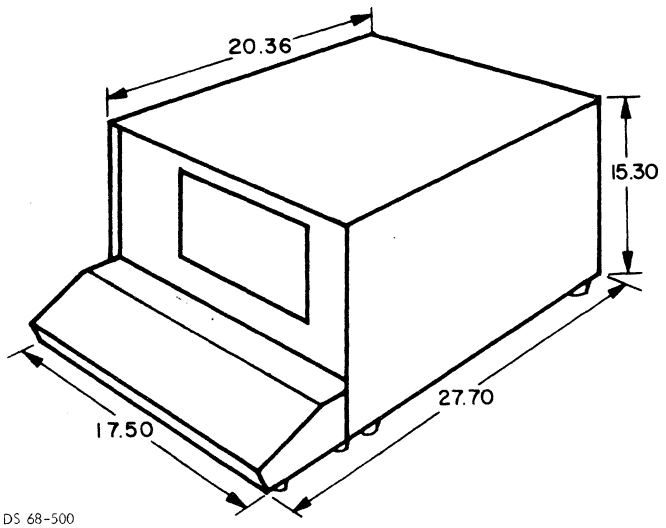


Figure 2-1. Display Terminal Outline Dimension Drawing

2-1.2 Primary Power Requirements

The Display Terminal requires a primary power input of 110 vac. The specific primary power requirement, with regard to tolerance, frequency, and maximum wattages, is shown in table 1-1.

2-2 INSTALLATION PROCEDURE

2-2.1 Receipt and Unpacking of Equipment

The Display Terminal is shipped completely assembled and ready for operation. The display terminal interface connection is provided by an (I/O) input/output cable which must either be fabricated locally or ordered from the Raytheon Company. This cable is used to couple data and control signals between the Display Terminal and the connected device.

Upon receipt of the Display Terminal, unpack the shipping crates as follows:

a. Carefully open the shipping crate(s) and check the contents against the shipping list to verify the arrival of all ordered equipment (such as spare parts, cables).

b. Remove the Display Terminal from its shipping crate and place it on a convenient work bench or table.

c. Carefully examine the exterior of the Display Terminal for any damage which may have occurred during shipment. Report any damage noted immediately.

2-2.2 Cable Requirements

The I/O cable used for connecting the Display Terminal to the interfacing device can be any good quality shielded 4-twisted pair cable and an MS-3106A145-55 connector. The maximum allowable length between the Display Terminal and the connected interface device is 50 feet.

2-2.3 Cable Fabrication

If specifically requested, a cable precut to customer requirements is supplied with the Display Terminal. If the cable is not ordered, it may be locally fabricated using the cable and connectors described in the preceding paragraph. When planning the installation, make sure that the cable length does not exceed the maximum limit of 50 feet. Use standard cable assembly techniques to fabricate the cable, taking care when soldering each connection to prevent shorts between connector pins. Raytheon Drawing No. 425116 (Chapter 7) illustrates display terminal signal connections to and from the connected interface device.

2-3 PREOPERATIONAL PROCEDURES

2-3.1 Visual Checkout

Internal mechanical and electrical connections must be checked to determine whether any terminal connectors or mounting screws have loosened during shipment. To access these internal connections, the cover must be removed in the following manner:

a. Locate and remove the combination on/off brightness control knob.

b. Remove the four screws (black) holding the metal mask to the front plate assembly.

c. Remove all 31 screws (silver) securing the cover to the front plate.

d. Remove all 8 screws (silver) at the rear of the unit. These screws are located near the BNC connectors protruding from the rear cover.

e. Obtain assistance and gently slide the cover to the rear while pulling the display chassis forward.

Once the cover is removed, the internal assemblies are exposed for examination. Check the following points for good mechanical and electrical connections:

a. All terminal screws on both power supply assemblies (see figures 1-5 and 1-6).

b. All wiring connections to the printed circuit board assemblies (see figures 1-3 through 1-7).

c. The monoscope and CRT tube sockets to assure that they are firmly connected (see figures 1-4 and 1-7).

d. The HV anode lead on the CRT (see figure 1-5).

2-3.2 Resistance and Voltage Measurements

Before applying power to the Display Terminal, measure the electrical resistance between each power supply output line and ground. The measured resistance varies, depending upon equipment control settings and component tolerances. In no case should the resistance to ground (chassis) measure 0 ohms; this indicates a shorted condition. No shorts should be discovered, since the Display Terminal undergoes extensive testing at the factory. However, careless handling during shipment can result in shorts which must be corrected prior to applying power to the equipment.

The dc output wiring is color coded throughout the equipment as follows:

Output	Color Code
+5 vdc	gray
-22 vdc	purple
+22 vdc	red
+100 vdc	orange
+540 vdc	yellow
-1.2 kvdc	red (high voltage insulation)

WARNING

Do not measure the 12 kvdc CRT anode voltage with the voltmeter. This supply produces voltages which are hazardous to human life and should be checked only with a dc voltmeter equipped with a high voltage probe.

Note

When the cover is removed, a safety interlock (shown in figure 1-7) opens the primary power input circuit. This interlock must be bypassed (cheated) to apply power to the Display Terminal.

CAUTION

The -22 vdc and +22 vdc power sources must be checked first because these voltages function as a supply for the high voltage power supply assembly (A5).

To measure the dc voltage outputs, use a voltmeter (Simpson 260, or equivalent) and, after assuring that the combination on/off switch and brightness control is in the OFF position, plug the ac power cord plug into a convenient receptacle. When measuring the output voltages of each supply, do not leave power applied between measurements. As soon as the measurement is recorded, remove power from the unit. This will assist in preventing equipment damage if an undetected short exists in another power supply output branch.

2-3.3 Alignment and Adjustments

Before placing the Display Terminal in operation, the following adjustments and alignment routines should be performed as necessary for optimum operation. The Display Terminal is completely aligned at the factory and extensive alignment should not be necessary. However, excessive vibrations during shipment or line voltage variations may necessitate the following procedures, which should be performed in the order indicated. If it is determined that a particular procedure is not necessary, skip the procedure and proceed to the next.

2-3.3.1 Turn-On Procedure

While holding the BREAK key depressed, turn the combination power on/off brightness control clockwise to apply power to the unit. Immediately perform the following three steps:

a. Depress the CONTROL and CURSR RESET keys simultaneously.

b. Depress the CURSR RESET key.

c. Depress the ERASE MSG key.

These steps should be performed each time power is initially applied to the Display Terminal to prevent damage to the monoscope.

After 3 minutes, advance the on/off brightness control further clockwise until horizontal scan lines approximately 0.13 inch high are visible on the CRT screen.

2-3.3.2 Delay-Line Adjustment

The following conditions indicate the necessity for a delay-line adjustment: character shifting, moving characters, flashing presentation, multiple cursors, or cursor disappearance when CURSR RESET is released.

Note

Do not attempt delay-line adjustments until it is absolutely established that the Display Terminal has had adequate time (3 to 5 minutes) to warm up and that an adjustment is necessary. If the need for adjustment is established, it should not be necessary to adjust either delay line more than six turns in either direction from the factory adjustment.

The delay line is adjusted by performing the following procedure:

a. Refer to figure 1-3. Remove the wire from terminal 7 of Display Logic Board A13.

b. Using a dual-input oscilloscope (Tektronix Type 545A with Type CA plug-in unit or equivalent), refer to figure 1-5 and connect the oscilloscope as follows:

(1) External trigger to delay-line electronics A9, terminal E. Switch oscilloscope to minus (-) extension trigger.

(2) Connect one input probe to delay-line electronics A9, terminal E, and the second to A6, pin 4.

c. On the top delay line (see figure 2-2), turn the adjustment screw until the falling edges of the clock pulses are aligned with the centers of the peaks of the sine waves (see figure 2-3). (The waveforms shown are not representative of any particular character.)

d. Reconnect the wire to terminal 7 of Display Logic Board A13.

e. Alternately depress and release the CURSR RESET key and simultaneously adjust the bottom delay line adjustment screw (see figure 2-2) until the screen displays stable characters and the cursor remains visible when the CURSR RESET key is released.

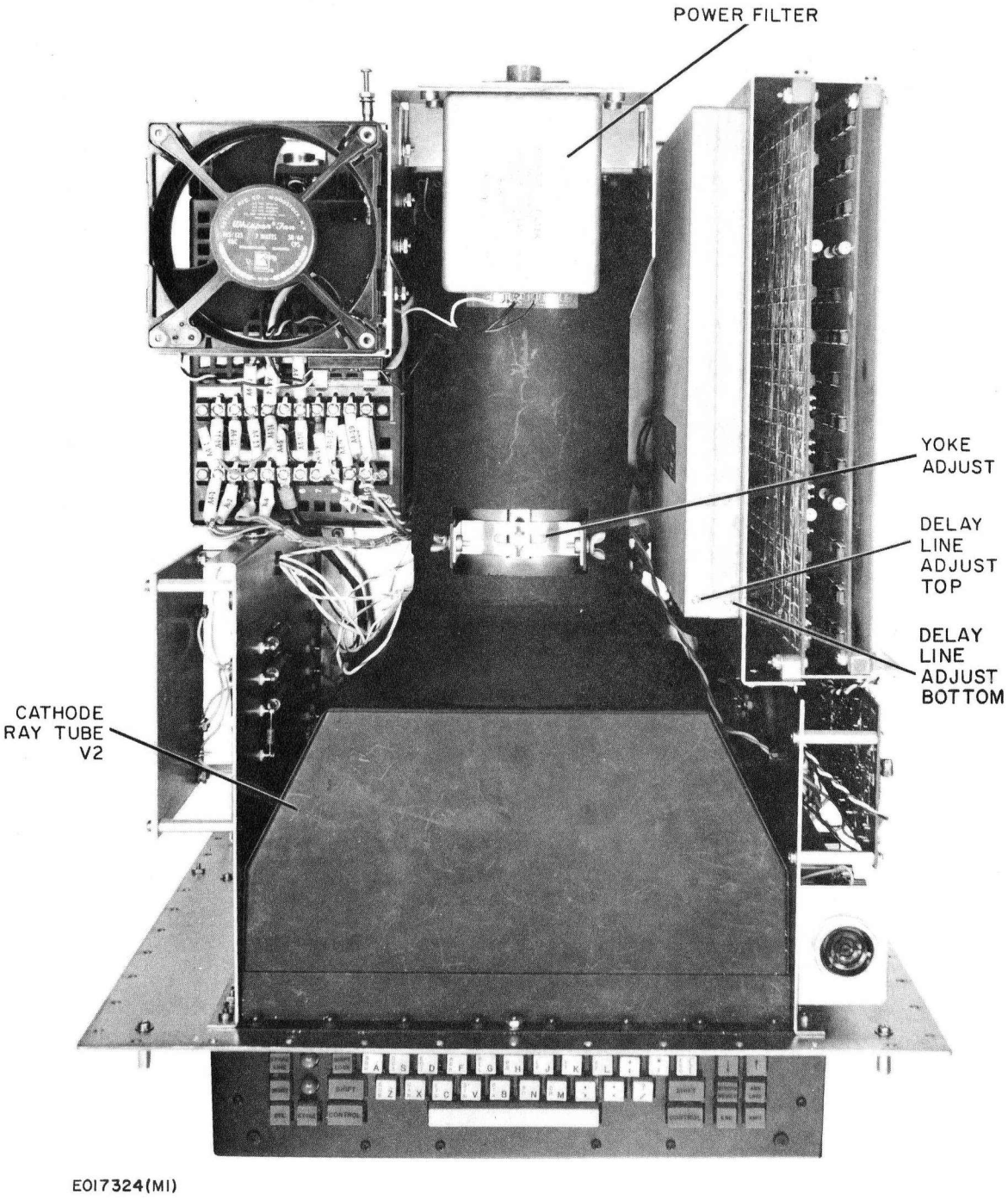


Figure 2-2. Model 402-2AM13 Display Terminal, Top View with Cover Removed

f. When the screen displays stable characters, turn the bottom delay-line adjustment screw three additional turns. The displayed characters should remain stable.

g. Adjust the bottom delay-line adjustment screw to the center of its stable range.

h. Repeat steps e, f, and g for the top delay line.

i. When adjustment is complete, either adjustment screw should be adjustable three turns in either direction without losing character stabilization. If this degree of adjustment is possible, then both delay lines are properly adjusted. If not, then the delay-line section at fault should be readjusted to another null point and the procedures outlined in steps e through g should be repeated.

Note

Adjusting the delay line is a difficult procedure. Each delay line section may have as many as six null positions, only one of which is correct. Both sections must be adjusted to the correct null point in order to realize optimum display terminal operation.

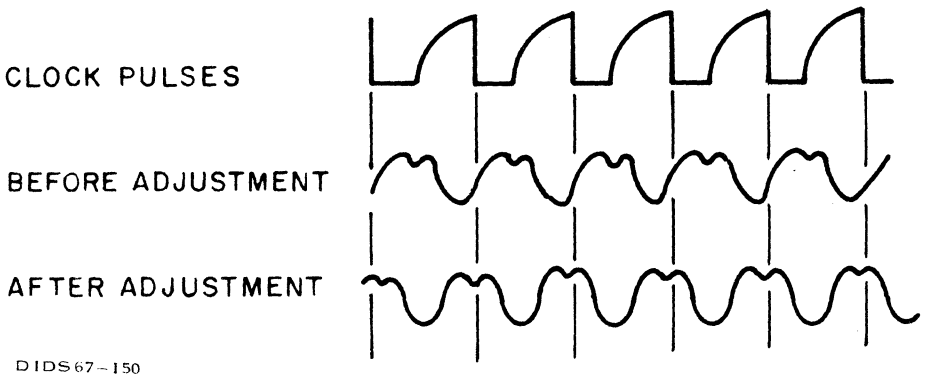


Figure 2-3. Delay-Line Adjustment

2-3.3.3 Video Amplifier A8

The video amplifier need be adjusted only when the cursor symbol ( ) is not clearly visible on the screen. If the cursor is not visible, and increasing the screen brightness does not improve cursor definition, perform the following adjustment:

a. Depress the CURSR RESET key to place the cursor symbol in the first-line, first-character position.

b. Locate cursor video control R-19 on video amplifier A8 (see figure 1-7). Slowly turn the control clockwise until a clearly defined cursor character is visible on the screen.

c. Move the cursor to numerous other positions on the screen and examine cursor definition. Readjust R-19 as necessary.

2-3.3.4 Monoscope Deflection Amplifier A3

The monoscope deflection amplifier (see figure 2-4) should be adjusted only when any one of the following conditions exists:

a. Scan lines are not approximately 0.12 inch high

b. Upper case alphabetical characters are not 70 percent of frame height

c. Displayed characters are uneven, either horizontally or vertically

d. Displayed characters are blurred or appear as double images

e. Displayed characters are not centered in their frames (upper case alphabet only)

When any of the above conditions exist and cannot be corrected by adjusting the CRT FOCUS or MONO FOCUS controls, perform the following adjustments. (Note that many of the controls interact, hence, some adjustment may have to be repeated in order to achieve optimum alignment.)

a. In the center of the screen on the first line, type in the following characters:

HOHOHOHOHOHO

b. In the center of the screen on the second line, type in the following characters:

ttt$t $t $

c. In the center of the screen on the third line, type in the following characters:

weruoaszxcvnm

d. In the center of the screen on the fourth line, type in the following characters:

gypjg

e. In the center of the screen on the fifth line, type in the following characters:

fkhfdb

f. If the scan lines are not 0.13 inch high, adjust diddle amplitude control R43. For this and all following adjustments, refer to figure 2-4.

g. If characters H and O are not 70 percent of frame height and the lower case characters on the third line are not 50 percent of frame height, adjust diddle gain control R-29.

h. Observe characters H and O in the first line. If these characters are not centered horizontally, alternately adjust the Y-gain (R-52) and Y-position (R-27) controls.

i. Observe characters t and $ in the second line. If these characters are not centered vertically, alternately adjust the X-gain (R-58) and X-position (R-7) controls.

j. Repeat steps h and i until all four characters are centered both horizontally and vertically within their frames.

k. Observe the characters on the fourth line of the screen. The lower extremity of the characters should be just touching the bottom of their frames.

l. Observe the characters on the fifth line of the screen. The upper extremity of the characters should be just touching the top of their frames.

m. If the displayed characters are uneven (either vertically or horizontally) perform the following steps:

(1) Observe characters t and $ and adjust Y-skew control R-16 until the characters line up vertically.

(2) Observe characters H and O and adjust X-skew control R-21 until the characters line up horizontally.

n. If the displayed characters are blurred, advance the cursor to the center of the screen on the sixth line and type in characters B, 8, * and t. Alternately adjust diddle coil phase control R-36, the MONO FOCUS, and the CRT FOCUS until the upper and lower portions of B and 8 are of equal size and * and t are not blurred.

o. Observe the entire screen presentation. If any previous adjustments have been affected, repeat the necessary procedures until a suitable compromise is obtained.

Because many of the previous adjustments interact, it may be necessary to perform two complete alignments before realizing a satisfactory screen presentation.

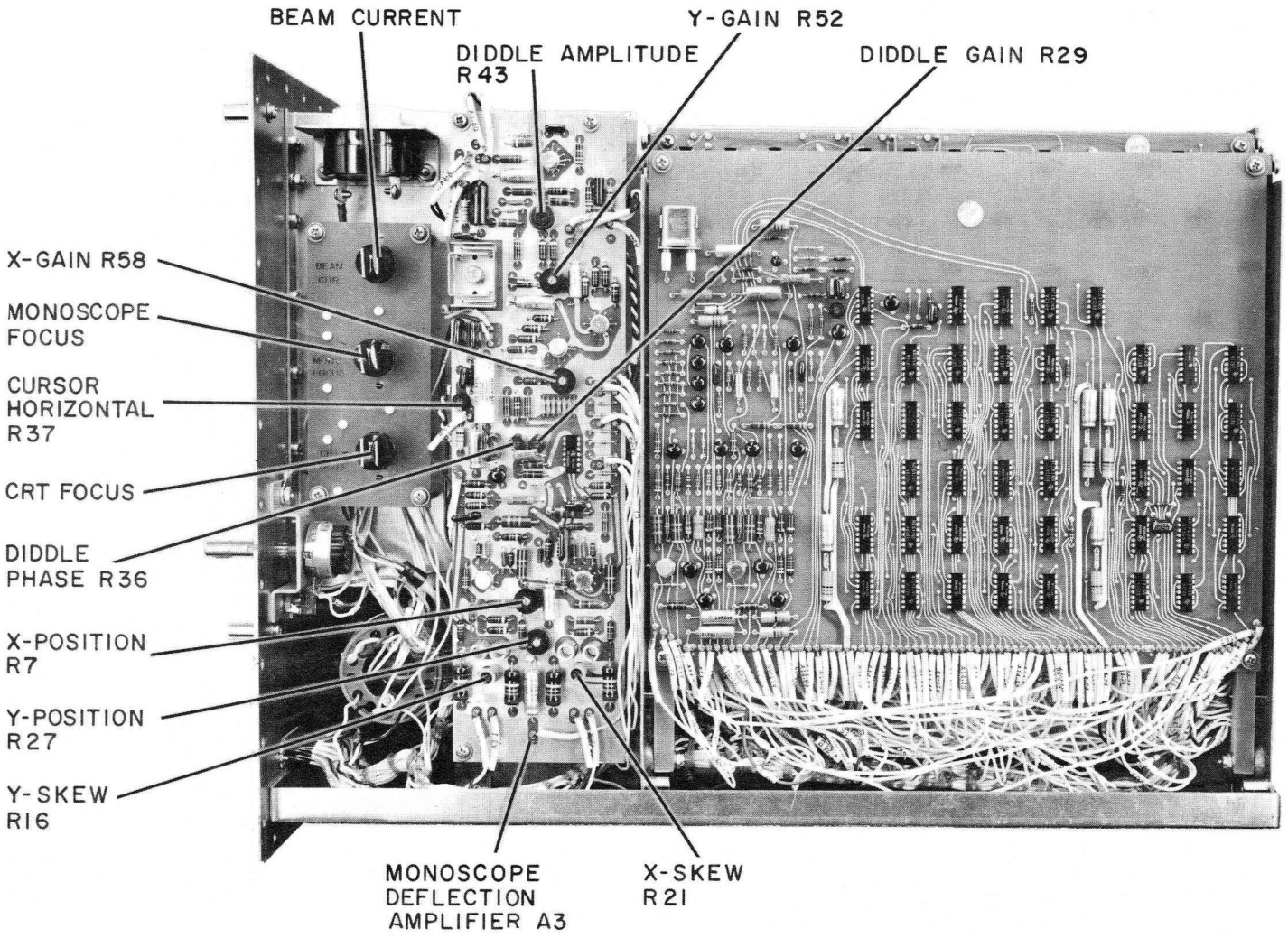


Figure 2-4. Monoscope Deflection Amplifier Adjustments

2-3.3.5 Horizontal and Vertical Deflection Amplifier A2

This adjustment should be performed only when the raster is not centered on the display terminal screen or when insufficient raster height or width is present. To properly position the raster, perform the following adjustments:

a. Either type in a full screen of characters or increase the brightness control until all 13 scan lines are visible. Note the screen presentation. Thirteen lines of 80 characters each should be visible and centered within the screen area.

b. If the raster is vertically off-center:

(1) Adjust vertical centering control R-4 (see figure 2-5) to vertically center the raster.

(2) Adjust vertical amplitude control R-27 to produce the required raster height.

c. If the raster is horizontally off-center:

(1) Adjust horizontal centering control R-35 to horizontally center the raster.

(2) Adjust horizontal amplitude control R-50 to produce the required raster width.

d. If the raster is tilted, loosen the wing nut holding the yoke (see figure 2-2) in position and adjust the yoke to the position providing scan lines which parallel an imaginery line drawn through the center of the screen. Retighten the yoke clamp.

2-4 REASSEMBLY

When the Display Terminal is completely aligned, the cover may be replaced by reversing the removal procedure. Make sure that all rf shields are in place and all screws are secured before operating the Display Terminal.

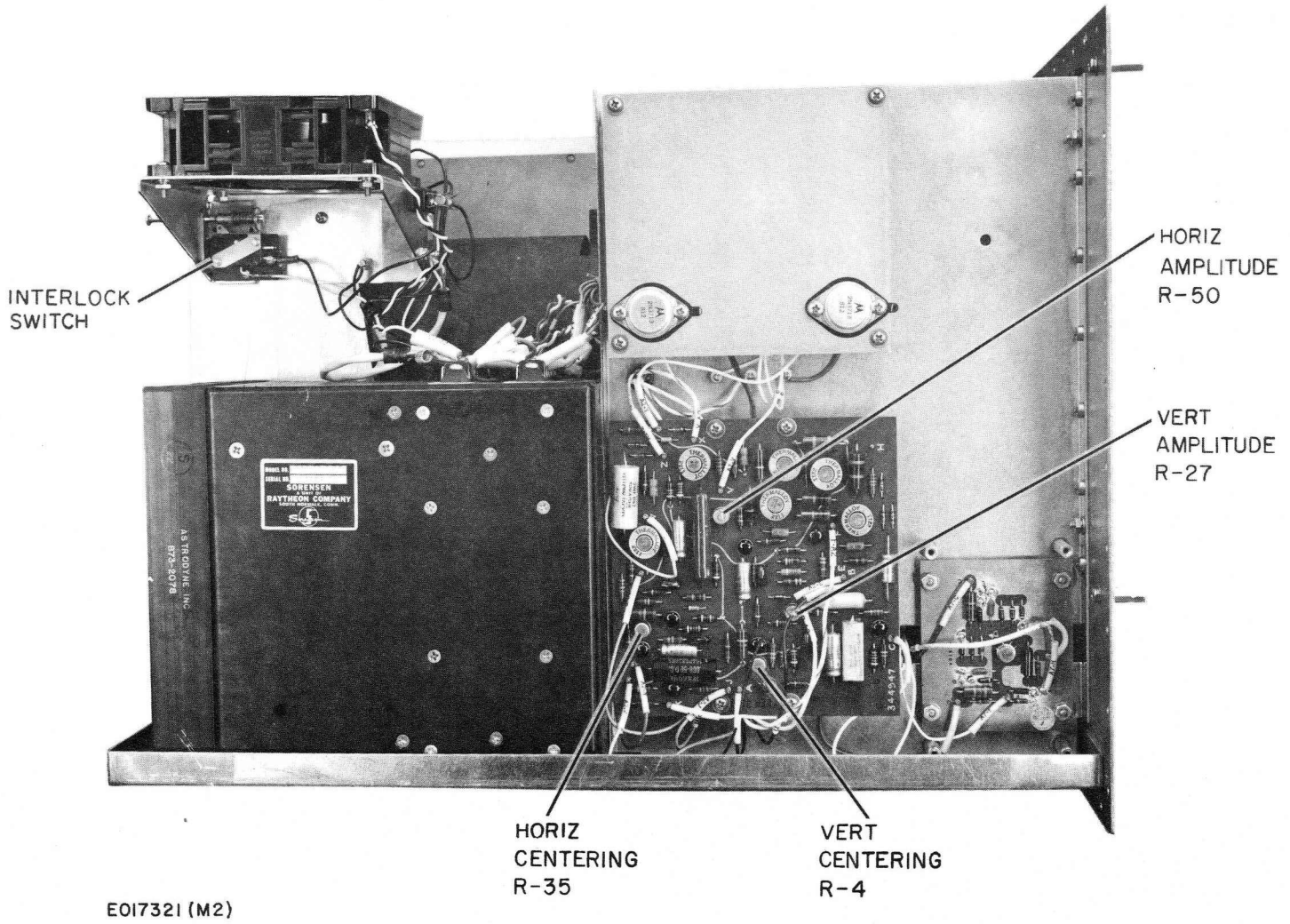


Figure 2-5. Horizontal and Vertical Deflection Amplifier Adjustments

CHAPTER 3

OPERATION

This chapter documents turn-on, turn-off, and operating procedures necessary to operate the Model 402-2AM13 Display Terminal. Also included in this section are the name and function of all operating controls and indicators contained in the Display Terminal.

3-1 IDENTIFICATION OF OPERATING CONTROLS AND INDICATORS

The keyboard assembly (figure 3-1) contains all operator controls except the power on/off brightness control. Table 3-1 lists the name and function of all operating controls and indicators necessary to operate the Display Terminal. Unless otherwise specified, the controls and indicators listed in table 3-1 are referenced to figure 3-2. For additional information concerning operation, refer to the Model 402-2AM13 User Manual.

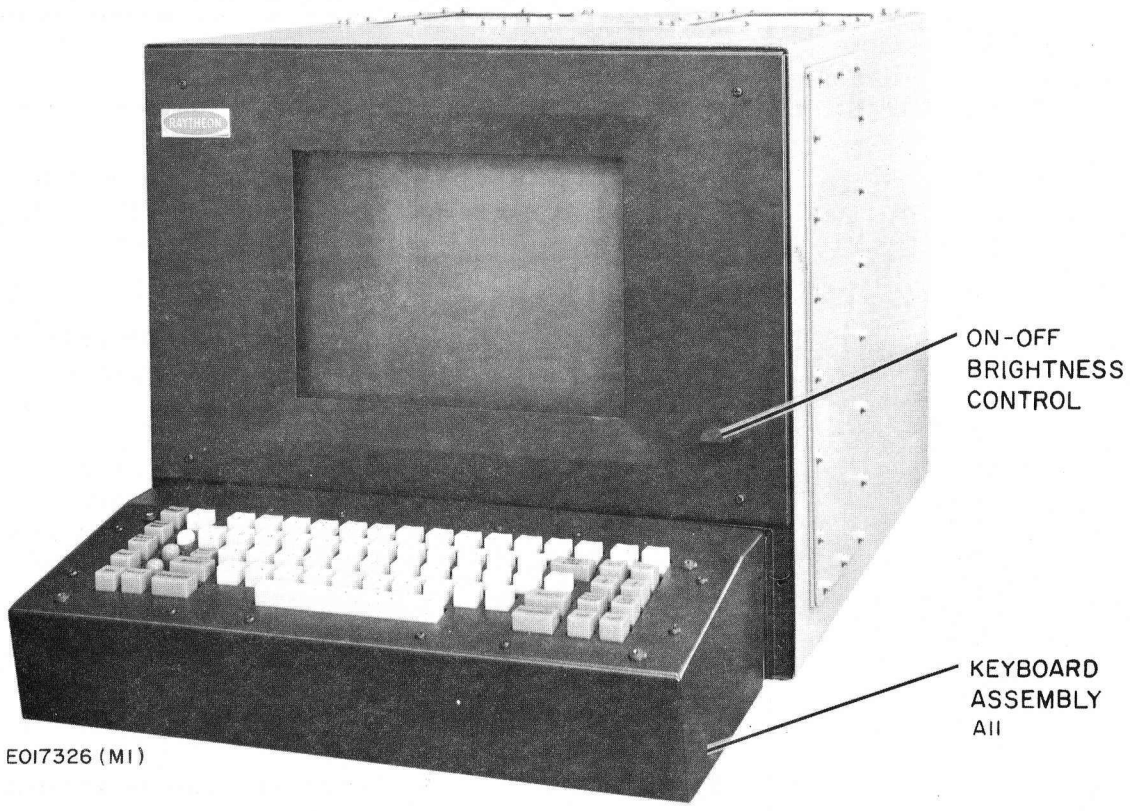


Figure 3-1. Model 402-2AM13 Operating Controls and Indicators

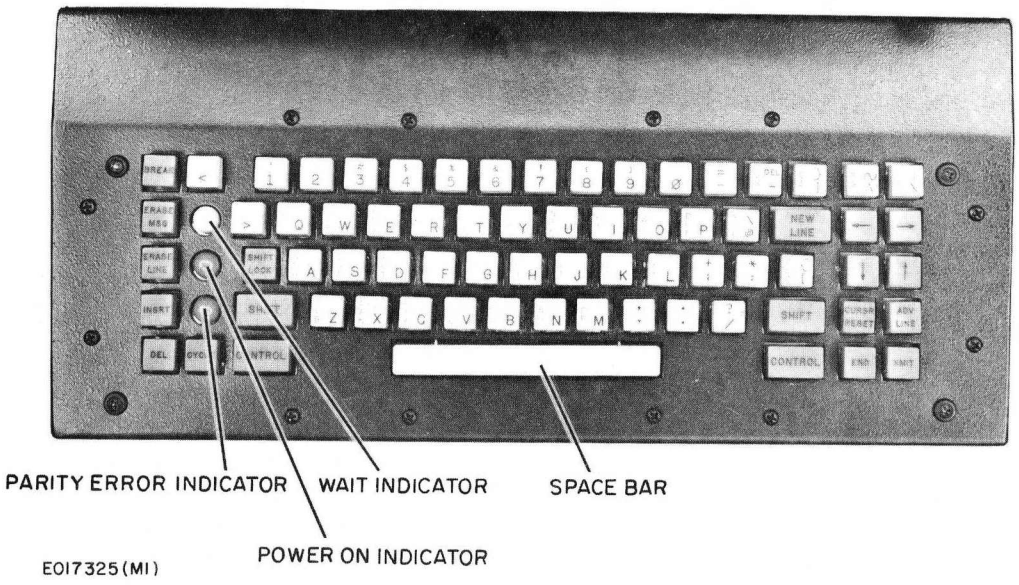


Figure 3-2. Keyboard Assembly Operating Controls and Indicators

Table 3-1. Operating Controls and Indicators

Ref Designation or Keyboard Notation	Name	Function
	Combination on/off switch and brightness control (see fig. 3-1)	Applies and removes primary ac power and adjusts the brightness of the display screen presentation.
	Power On indicator (green)	Illuminates to indicate that a power on condition exists.
ADV LINE	Advance Line	Advances the cursor to the first character position of the next line. If the cursor is on the last line when this key is depressed, the cursor moves to the frame reset (first character; first line) position.
BREAK	Break key	Clears all display terminal logic.
CONTROL	Control key	The CONTROL key performs two functions: 1) When the CONTROL key and a character key are depressed simultaneously, the

Table 3-1. Operating Controls and Indicators (Cont)

Ref Designation or Keyboard Notation	Name	Function
CONTROL (Cont)		ASCII control code associated with the character key is inserted into the delay-line memory. 2) When the CONTROL key is held depressed, all ASCII control codes circulating in the delay-line memory are displayed as the lower case alphabet which is associated with the code. The operator can then determine which control codes have been inserted or received.
CURSR RESET	Cursor Reset key	Moves the cursor to the frame reset (first character; first line) position on the screen.
CYCLE	Cycle key	Simultaneous depression of the CYCLE key and any character, edit, or cursor control key permits the function to be repeated at a 6-Hz rate.
DEL	Delete key	The DEL key performs two functions: 1) When only the DELETE key is depressed, a character delete function is accomplished. On a given line which contains the cursor, all the characters to the right of the cursor are moved one character

Table 3-1. Operating Controls and Indicators (Cont)

Ref Designation or Keyboard Notation	Name	Function
DEL (Cont)		position to the left. The character formerly associated with the cursor is erased, and the character immediately to the right is substituted in its place. A blank is inserted at the last character position of the line. 2) When the SHIFT key is held depressed and the cursor is in the first character position of a line, depressing DEL causes a line insert function to be accomplished. The line containing the cursor is deleted and all succeeding lines are moved up. The line formerly associated with the cursor is erased and replaced with the line immediately beneath it and a line of blanks is inserted at the last line of the screen.
END	End key	Inserts an ETX character code into the delay-line memory and resets the cursor to the frame (or line) reset position on the screen. The END key is normally depressed upon completion of message composition in preparation for transmitting. In some equipment, depressing END causes automatic transmission (see table 1-3).

Table 3-1. Operating Controls and Indicators (Cont)

Ref Designation or Keyboard Notation	Name	Function
ERASE LINE	Erase Line key	Erases all characters from the cursor to the end of the line. An ASCII IDLE character is substituted for each character code erased.
ERASE MSG	Erase Message key	Erases all characters from the cursor to the bottom of the screen.
	Error Indicator (red)	Illuminates when the Display Terminal detects a parity error in the incoming message, and is automatically extinguished when a transmit operation is initiated or when the CURSR RESET and CONTROL keys are depressed simultaneously.
INSERT	Insert key	The INSRT key performs two functions: 1) When only the INSRT key is depressed, a character insert function is accomplished. On a given line which contains the cursor, all the characters to the right of the cursor are moved one character position to the right. An ASCII IDLE character is then inserted at the cursor position to permit the entry of the desired character. 2) When the SHIFT key key is held depressed and the cursor is in the first character position of a line, depressing INSRT causes a line insert function to

Table 3-1. Operating Controls and Indicators (Cont)

Ref Designation or Keyboard Notation	Name	Function
INSERT (Cont)		be accomplished. All information to the right of and below the cursor is moved down one line. ASCII IDLE characters are inserted in the line occupied by the cursor to permit the insertion of a full line of information.
NEW LINE	New Line key	Has the same visual effect as depressing the ADV LINE key; however, this key also automatically enters a line feed (LF) code into the delay-line memory.
SHIFT LOCK	Shift Lock key	Performs the usual typewriter function by holding the keyboard in the upper case mode. The SHIFT LOCK key is released by depressing the SHIFT key on the left side of the keyboard.
	Wait Indicator (white)	Illuminates when the keyboard is locked. Once the XMIT key is depressed, all but two keys on the keyboard are locked until an ETX character code is received from the CPU. When this occurs, the WAIT lamp is extinguished. The WAIT lamp may also be extinguished locally by depressing the BREAK key or by simultaneously depressing the CONTROL and CURSR RESET keys.
XMIT	Transmit	Initiates transmission to the CPU. All data from the cursor position to the first detected ETX is transmitted.

Table 3-1. Operating Controls and Indicators (Cont)

Ref Designation or Keyboard Notation	Name	Function
←	Step Left	Depressing the Step Left key to the first detent causes the cursor to move one character position to the left. In the fully depressed second detent position, the step left function is repeated at a 12-cycle rate.
→	Step Right	Depressing the Step Right key to the first detent causes the cursor to move one character position to the right. In the fully depressed second detent position, the step right function is repeated at a 12-cycle rate. In either case, if the cursor is stepped to the last character of the line position, it automatically steps to the next line.
↑	Step Up	Moves the cursor from any character position on a line to the same character position of the line immediately above. If the cursor is in the first line when the key is depressed, the cursor moves to the last line.
↓	Step Down	Moves the cursor from any character position on a line to the same character position on the next line. If the cursor is in the last line when the key is depressed the cursor moves to the first line.

3-2 OPERATING INSTRUCTIONS

3-2.1 Preoperational Procedures

Before initially operating the Display Terminal, all preoperational procedures outlined in Chapter 2 must be performed. During subsequent operation, no special preoperational procedures are necessary, other than allowing a 3-minute warm-up period before exercising any function.

3-2.2 Turn-On Procedure

To turn on the Display Terminal, depress the BREAK key and turn the combination on/off brightness control clockwise. Then immediately perform the following three steps:

a. Depress the CONTROL and CURSR RESET keys simultaneously

b. Depress the CURSR RESET key

c. Depress the ERASE MSG key

After a 3-minute warm-up period, increase the brightness control until the screen presentation is of the desired brilliance.

3-2.3 Operating Procedures

To operate the Display Terminal, position the cursor at the place on the screen where the message is to begin, and proceed as follows:

a. Type in the desired message. For lower case alphabetical characters, depress the applicable character key; for upper case equivalents, simultaneously depress either of the SHIFT keys and the character key. A message may contain as many as 1039 text characters (ETX occupies one character position). Each time a character key is depressed, the cursor automatically steps right to bracket (⌋ cursor) or alternately blinks (≣) in the next character position.

b. When the message is complete, depress the END key. This inserts an end-of-text (ETX) control code in delay-line memory and resets the cursor to either the frame reset or first character of the line position (see table -13).

c. To transmit the message to the CPU, depress XMIT.

It is assumed that maintenance technicians will not normally be responsible for operating the Display Terminal. However, after performing scheduled or unscheduled maintenance, and especially if parts were replaced, the technician should type in the entire repertoire and exercise all functions before returning the Display Terminal to operation.

3-2.4 Turn-Off Procedure

There are no special steps necessary for removing power from the Display Terminal. To turn off the unit, merely turn the combination power on/off brightness control fully counterclockwise.

CHAPTER 4

THEORY OF OPERATION

4-1 INTRODUCTION

This chapter presents the theory of operation for the Raytheon Model 402-2AM13 Display Terminal hereinafter referred to as the Display Terminal. Explanations begin with system application and become increasingly technical as the chapter progresses. For convenience, this information is divided into four sections, which contain the following information: Section I, Functional Operation, a system description of the Display Terminal including explanations concerning conversational modes, message formats, and data handling capabilities; Section II, Functional Description, a description of each major circuit on a block diagram basis; Section III, Circuit Description, an explanation of the circuits contained on each analog and digital circuit board; Section IV, Integrated Circuits, a description of the operation of the various integrated-circuit logic elements used on the various circuit boards.

SECTION I

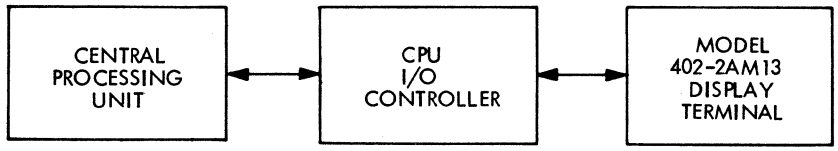
FUNCTIONAL OPERATION

4-2 DESCRIPTION OF SECTION CONTENTS

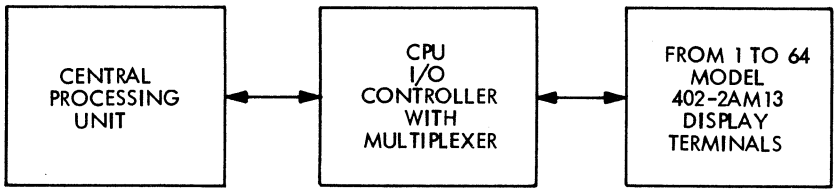
This section contains several detailed explanations pertaining to the basic operation and design features of the Display Terminal. These explanations document system description, system operation, optional design features, conversational modes, and message formats.

4-3 SYSTEM DESCRIPTION

The Display Terminal is specifically designed to provide keyboard input and visual access to information stored or processed by a central computer. The Display Terminal is entirely self-contained and requires no auxiliary equipment for operation other than a suitable Central Processing Unit Input/Output (CPU I/O) device (part of the CPU). From 1 to 64 Display Terminals can be connected to the CPU depending upon the requirements of the system. Figure 4-1 illustrates two basic system configurations employing the Display Terminal. Part A of figure 4-1 illustrates a system where only one Display Terminal is connected to the CPU; Part B, a system where several Display Terminals are connected to the CPU via a multiplexer. The multiplexer portion of the I/O controller selects one of the several Display Terminals, either sequentially or randomly.



A. SINGLE TERMINAL CONFIGURATION



DIDS 68-501

B. MULTITERMINAL CONFIGURATION

Figure 4-1. Typical System Configuration

All message preparation and editing is accomplished off-line, and the Display Terminal is connected to the CPU only during periods of actual data transfer. This feature provides economic operation by conserving CPU time. The transfer of data between the Display Terminal and the CPU is asynchronous and occurs at a rate of 1200 baud. The necessary start, stop, and parity bits are generated internally by the communications control logic during specific bit times of each character.

4-4 SYSTEM OPERATION

The Display Terminal operates in either the enquiry-response or the polling conversational mode. The basic difference between the modes is that the former provides operator control over data transfers while in the latter, data transfers are controlled by the CPU. In either mode, display terminal operators generally initiate data messages by operating specific keys on the keyboard. (An exception is the No Business message which is produced internally without the operator's knowledge.) Each character key depression enters a specific 7-bit digital code in memory and displays a corresponding character on the CRT screen. When the entire message text has been composed, the operator initiates a transmission sequence by depressing the appropriate keys on the keyboard.

In a system configured for the enquiry-response conversational mode, the message is transmitted to the CPU as soon as the Display Terminal receives a clearance to transmit. In polling systems, however, the CPU must poll the Display Terminal before a data transfer occurs.

The preceding text has briefly described display terminal operation in the transmit mode. In the receive mode, display terminal operation is again determined by the conversational mode employed. In enquiry-response systems, the display terminal operator usually issues an enquiry to elicit a response from the CPU. In polling systems, the CPU can issue a write directive at any time to display a message on the display terminal screen.

Thus, even though the Display Terminal is primarily designed to provide a rapid transfer of information to and from the CPU, the conversational mode employed determines how and when this transfer will occur.

4-5 OPTIONAL OPERATION

Display Terminals are normally designed to perform certain functions and to operate in a set manner. However, the operation of any particular Display Terminal may be readily changed by the incorporation of numerous design options. In the remainder of this chapter where no reference is made to any particular option, it can be assumed that the Display Terminal operates in the manner described regardless of optional strapping.

4-5.1 Optional Communication Channel

When the Display Terminal is connected to a particular CPU I/O controller, an option allows either a 2-wire or 4-wire communication channel to be employed between the controller and the CPU. In 2-wire systems, data communication between the CPU and the Display Terminal is accomplished by means of a common pair of telephone lines. In 4-wire systems, transmitted data is transferred to the CPU by means of one pair of lines while received data is returned over a second pair of lines. In either case, the Display Terminal operates in the half-duplex transmission mode whereby it can either transmit or receive data, but cannot do both simultaneously.

4-5.2 Optional Conversational Modes

The Display Terminal can operate in either of two conversational modes: polling or enquiry-response. In the polling mode, the CPU, by issuing either a read or a write directive, exercises control over all data transfers. In the enquiry-response mode, the display terminal operator usually issues an enquiry and the CPU responds with an answering message. Since these two modes essentially determine how the display system operates, separate discussions for each mode are included throughout the remainder of this chapter.

4-5.3 Address Options

The Display Terminal can assume any one of 64 address codes to provide selective addressing when several Display Terminals are employed by the display system. When the broadcast address option is employed, the Display Terminal is capable of recognizing either its own address or a broadcast address. When several Display Terminals are modified in this manner, the CPU can issue a write directive (polling mode) or a response (enquiry-response mode) to display a data message on all connected Display Terminals simultaneously.

4-5.4 Transmit Options

Normally, two steps are required to initiate transmission from the Display Terminal to the CPU. The operator usually types in the desired text and then performs the following two steps:

a. Depresses the END key which inserts an ETX code into the delay line and resets the cursor to the frame reset or first character of line position

b. Depresses the XMIT key to initiate transmission to the CPU

When the One-Step Transmit option is employed, the XMIT key need not be depressed to initiate transmission; thus, the single step of depressing the END key is all that is required to initiate transmission. The point on the screen to which the cursor is returned when the END key is depressed is determined by still another option.

In addition, the cursor can be moved to specific positions on the screen by employing other options. The Frame-Reset at End-of-Transmit option returns the cursor to the frame reset position on the screen when the last character (ETX) of a message is transmitted. When the option is not employed, the cursor moves to the next character position on the line, rather than returning to the frame reset position.

The End-of-Transmit (EOT) option permits jamming an EOT character (0000100) into buffer register D3 before transmitting the last character of the message. The substitution of an EOT character for ETX (0000011) is commonly used to indicate the end of transmission for the site where several Display Terminals are connected in a polling configuration. In this instance, the last Display Terminal transmitting signifies the end of site transmission by entering EOT as a message terminator.

4-5.5 Receive Options

In addition to the Broadcast Address option mentioned previously, still another option is available in the receive mode. Normally, the cursor is stepped to the next character position when an ETX code is received from the CPU. The Advance Line at End-of-Receive option permits advancing the cursor to the start of the next line when the ETX character is received.

4-5.6 Cursor Option

The standard DIDS*-400 cursor is represented by a visual character (☰) which blinks and is alternately displayed in place of the character at the cursor position. A second nonblinking cursor in the form of a backward L (⌋) may be optionally employed. This cursor character brackets the character at the cursor position in the following manner: (A⌋).

4-6 INTERFACE CHARACTERISTICS

The Display Terminal is designed to interface with any device that conforms to Interface Standard MIL-STD-188B. The interfacing device is normally a CPU I/O controller unit or an I/O controller-multiplexer. The interface connections consist of five lines which exit through a connector at the rear or the side of the unit (see figure 4-2). These lines couple the following signals between the connected devices:

Request-to-Send

Clear-to-Send

Transmitted Data

Received Data

Ground

The display terminal interface signals are bipolar as follows:

Data Signals	Control Signals
MARK = +6v ±1v = logical 1	OFF = +6v ±1v = logical 1
SPACE = -6v ±1v = logical 0	ON = -6v ±1v = logical 0

In the display terminal quiescent state, all data and control lines with the exception of ground are held in a marking condition (+6v ±1v).

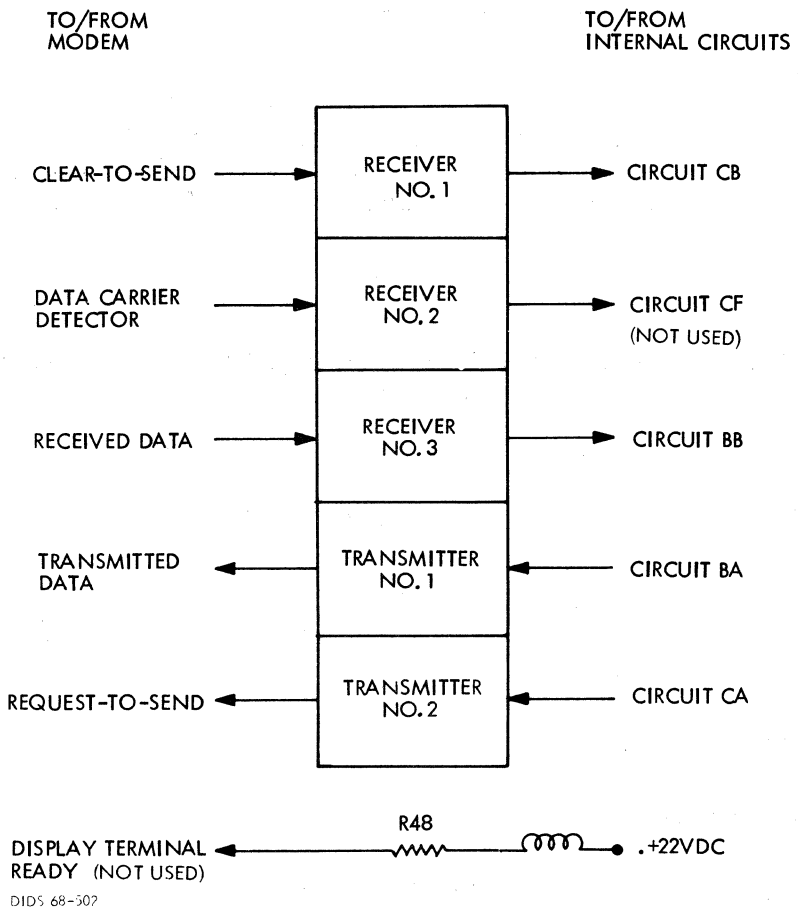


Figure 4-2. Modem Interface Circuits

4-6.1 Request-to-Send

The purpose of the request-to-send line (circuit CA) is to notify the connected interface device that the Display Terminal has a message available for transmission. This line couples a control condition of ON (-6v ±1v) to the connected device after the END and XMIT keys are depressed (two-step transmit) or when only the END key is depressed (one-step transmit option). The request-to-send line remains ON until the last data character (ETX) has been transmitted from the Display Terminal.

4-6.2 Clear-to-Send

The purpose of the clear-to-send line (circuit CB) is to notify the Display Terminal that communication with the CPU has been achieved and the message available for transfer may be transmitted. The clear-to-send line assumes a control condition of ON at the direction of the connected CPU I/O controller and remains ON for as long as the request-to-send line is ON.

4-6.3 Transmitted Data

The transmitted data line (circuit BA) is used to couple serial bit data at 1200 baud from the Display Terminal to the CPU I/O controller. When the Display Terminal is not actively transmitting data (such as between characters), this line is held at a marking condition (+6v ±1v).

4-6.4 Received Data

The received data line (circuit BB) is used to couple serial bit data at 1200 baud from the CPU I/O controller to the Display Terminal. The received data line is enabled at all times other than when the Display Terminal is transmitting data.

4-6.5 Ground

The signal ground line establishes a common ground reference for all CPU I/O controller to display terminal interface lines.

4-6.6 Transmit/Receive Conditions

In order for the display terminal to transmit or receive data, the following conditions must be true:

	To Transmit	To Receive
Request-to-Send	ON	OFF
Clear-to-Send	ON	OFF

4-7 CONVERSATIONAL MODES

The Display Terminal communicates with the CPU in one of two conversational modes: enquiry-response or polling. Each mode has advantages and disadvantages which must be considered during system planning to arrive at the mode most suitable for the particular system. An advantage of the enquiry-

response mode is that display terminal operators can gain immediate access to the CPU since the operators are responsible for initiating all message transfers. A disadvantage is that all display terminal positions have equal standing and therefore important message transfers may be held up while the CPU is processing a subordinate request. The polling mode eliminates this often unwanted feature by placing the CPU in direct control of the display system. A disadvantage of the polling mode which must be considered, however, is that the CPU uses valuable time while issuing polling directives to elicit or display information.

4-7.1 Enquiry-Response

In the enquiry-response conversational mode, all data transfers are initiated by display terminal operators (enquiry) and are answered or acknowledged by the CPU (response). However, the CPU can access the Display Terminal at any time, since a constant receive condition exists. Messages received in this manner are not solicited by the operator and are therefore termed unsolicited responses.

4-7.2 Polling

In the polling conversational mode, all data transfer is under the positive control of the CPU. In display systems that employ the polling mode, the CPU periodically issues one of two directives: read or write.

The read directive is issued by the CPU to read the data message from the addressed Display Terminal. The Display Terminal receiving the read directive immediately responds to the poll by transferring the message currently on its screen to the CPU. If a Display Terminal receives a read directive and has no data available for transfer, a 'no business' report is issued to the CPU.

The write directive is issued by the CPU when it has a message for transfer to the addressed Display Terminal. (In systems employing the broadcast address option, either one or all display terminals in the system can receive the message simultaneously.)

4-8 CHARACTER REPRESENTATION

The Display Terminal uses the American Standard Code for Information Interchange (ASCII) for the coding of digital information. ASCII primarily involves representing alphabetic letters, numerals, symbols or control codes in the form of 7-bit binary characters.

In addition to the 7 bits used for representing some form of information, each character contains its own parity, start, and stop bits. The parity bit is used to check the validity of each received character. Each character transmitted or received contains an even number of 1's, thus the Display Terminal operates as an even parity device. Start and stop bits are added to the extreme ends of each character to provide asynchronous transmission. In asynchronous transmission, data characters may be transmitted one at a time, or in groups; initializing or terminating message characters are not required for data synchronization.

The various characters used for conveying information in the system may be divided into two general groups: displayable and nondisplayable. The displayable characters are shown in figure 4-3, which represents the display terminal ASCII matrix. The character organization shown in figure 4-3 is identical to the character font of the monoscope target. The nondisplayable characters consist of numerous control codes used to accomplish a control action of some sort at either the Display Terminal or the CPU. These characters are listed according to their binary values in table 4-1.

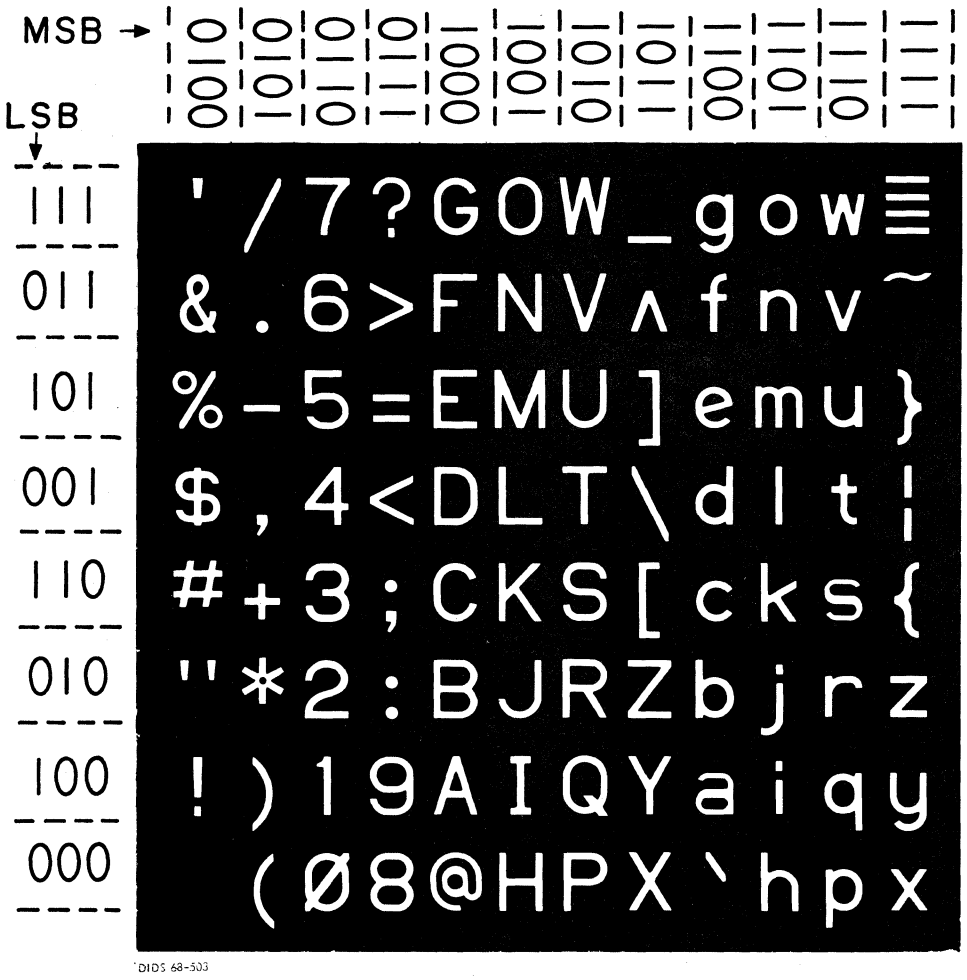


Figure 4-3. ASCII Matrix

4-9 CHARACTER FORMAT

The character format for 10-bit asynchronous transmission is shown in figure 4-4, where b_1 through b_7 are referenced to the characters illustrated in figure 4-3 and table 4-1. Aside from the information bits formed by b_1 through b_7, other factors concerning each data character that must be considered are:

Table 4-1. ASCII Control Codes

Name	Description	Code						
		b_7	b_6	b_5	b_4	b_3	b_2	b_1
NUL	Null	0	0	0	0	0	0	0
SOH	Start of Header	0	0	0	0	0	0	1
STX	Start of Text	0	0	0	0	0	1	0
ETX	End of Text	0	0	0	0	0	1	1
EOT	End of Transmission	0	0	0	0	1	0	0
ENQ	Enquiry	0	0	0	0	1	0	1
ACK	Acknowledge	0	0	0	0	1	1	0
BEL	Bell	0	0	0	0	1	1	1
BS	Back Space	0	0	0	1	0	0	0
HT	Horizontal Tab	0	0	0	1	0	0	1
LF	Line Feed	0	0	0	1	0	1	0
VT	Vertical Tab	0	0	0	1	0	1	1
FF	Form Feed	0	0	0	1	1	0	0
CR	Carriage Return	0	0	0	1	1	0	1
SO	Shift Out	0	0	0	1	1	1	0
SI	Shift In	0	0	0	1	1	1	1
DLE	Data Link Escape	0	0	1	0	0	0	0
DC1	Device Control 1	0	0	1	0	0	0	1
DC2	Device Control 2	0	0	1	0	0	1	0
DC3	Device Control 3	0	0	1	0	0	1	1
DC4	Device Control 4	0	0	1	0	1	0	0
NAK	Not Acknowledge	0	0	1	0	1	0	1
SYN	Sync	0	0	1	0	1	1	0

Table 4-1. ASCII Control Codes (Cont)

Name	Description	Code						
		b_7	b_6	b_5	b_4	b_3	b_2	b_1
ETB	End of Transmission Block	0	0	1	0	1	1	1
CAN	Cancel	0	0	1	1	0	0	0
EM	End of Medium	0	0	1	1	0	0	1
SUB	Substitute	0	0	1	1	0	1	0
ESC	Escape	0	0	1	1	0	1	1
FS	Final Separator	0	0	1	1	1	0	0
GS	Group Separator	0	0	1	1	1	0	1
RS	Record Separator	0	0	1	1	1	1	0
US	Unit Separator	0	0	1	1	1	1	1
DA	* Device Address (1)	-	0	0	0	0	0	0
DA	* Device Address (64)	-	1	1	1	1	1	1
	** Write Directive	0	X	X	X	X	X	X
	** Read Directive	1	X	X	X	X	X	X
	* Enquiry Response Mode							
	** Polling Mode Only, X's represent any DA							

a. The parity bit, b_8, will be a 1 if the number of 1's contained in a b_1 through b_7 are odd and a 0 if the number of 1's is even.

b. The start bit, b_0, is always a SPACE (-6v ±1v) and is always the first bit of a character; thus, the information bits (b_1 through b_7) are always transmitted LSB first. The start bit is used to inform either the CPU or the Display Terminal that a data character is being received.

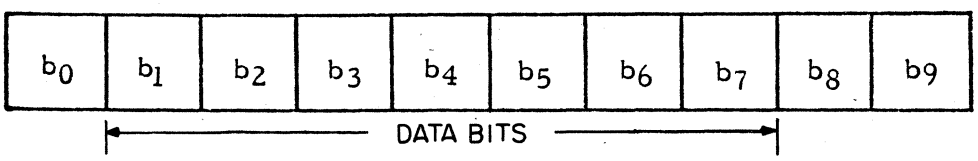


Figure 4-4. Character Format

c. The stop bit, b_9, is always a MARK (+6v ±1v) and is always the last bit of a character. The stop bit is used to inform either the CPU or the Display Terminal that one complete character has been received.

4-10 MESSAGE FORMAT

The general message format for all data communication between the Display Terminal and the CPU is: STX, DA, TEXT or COMMAND, and ETX. These terms are described below.

STX — The start-of-text character is always the first character of any data message transferred between the Display Terminal and the CPU. In the transmit mode (Display Terminal is issuing an enquiry or responding to a read directive), the STX character is jammed into buffer register D3 during the initial transmit sequence. In the receive mode, the STX character is decoded and if it is immediately followed by the correct device address, the Display Terminal is readied to receive the remainder of the data message.

DA — The device address character is a 7-bit code which the Display Terminal samples for its binary value (receive) or jams into buffer register D2 (transmit). In the receive mode, the DA is examined in buffer register D1 to determine whether the incoming message is intended for display terminal use. In the transmit mode, the DA is jammed into the buffer register and transmitted to inform the CPU of the message origin. In the polling mode, the DA is also used to indicate a read or write directive. If the incoming message contains a 1 in the MSB position of the DA, the Display Terminal responds with an available message or with a 'no-business' response. If the incoming message contains a 0 in the MSB position of the DA, the Display Terminal writes data characters received after the DA onto the CRT screen.

TEXT or COMMAND - This portion of the message contains up to 1039 data characters which may be in the form of displayable or nondisplayable characters. Normally, command codes are not displayable and either position the cursor or edit and format the message.

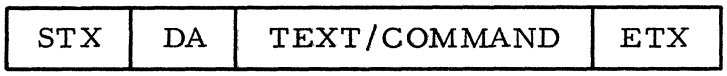
ETX — The end-of-text character is normally the last character of any transmitted message. In the transmit mode, the detection of an ETX character terminates the transmit mode. In the receive mode, ETX is used to determine the end of the message arriving from the CPU. In the polling mode, multiterminal sites may be optionally configured so that the last Display Terminal to transmit substitutes an EOT code for ETX. This is the only instance where ETX does not signify the end of a particular message.

4-11 MESSAGE FORMAT, ENQUIRY-RESPONSE

The message formats for the enquiry-response conversational mode are illustrated in figures 4-5 and 4-6 and described in the accompanying text.

4-11.1 Enquiry Format

The display terminal enquiry to the CPU is in the format shown in



DIDS 68-504

Figure 4-5. Enquiry Message Format

a. STX - This character has an ASCII control code of 0000010 and is always the first character of any message.

b. DA - This character can assume any one of 64 separate ASCII codes, depending upon the address assigned to the particular Display Terminal.

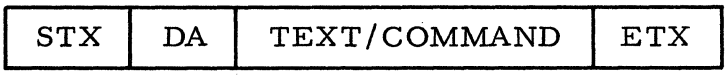
c. TEXT - These characters consist of displayed characters shown on the display terminal screen. From 1 to 1039 text characters are transmitted, depending upon the length of the message.

d. COMMAND - These characters are produced by depressing the CONTROL key and any one of several alphabet keys. For example, depressing the CONTROL and Q produces the DC1 command character. Depending upon the CPU program, DC1 can be used at the CPU to accomplish a control action.

e. ETX - This character has an ASCII control code of 0000011 and is the last character transmitted in any message. The ETX character is usually inserted into the display terminal delay line when the END key is depressed.

4-11.2 Response Format

The CPU response to a display terminal enquiry is in the format shown in figure 4-6.



DIDS 68-505

Figure 4-6. Response Message Format

a. STX - Described in paragraph 4-11.1a.

b. DA - The DA character received from the CPU is identical to the address transmitted during the enquiry portion of the enquiry-response sequence.

c. TEXT - Text characters in this portion of the message are written onto the display terminal screen beginning at the cursor position.

d. COMMAND - The command codes, if present, direct the Display Terminal to perform either an edit or cursor control function. Command codes have the following character designations: NUL, STX, ETX, ENQ, BEL, BS, HT, LF, VT, FF, CR, DC1, DC3, CAN, and ESC. With the exception of LF, these codes are not stored in the display terminal delay line unless they are preceded by the ESC code. The ASCII coding for these codes is shown in table 4-1 and a summary of the function performed by each code is provided in table 4-2.

e. ETX - Described in paragraph 4-11.1e.

Table 4-2. Action of ASCII Control Codes During Receive

ASCII Code	Meaning	Function Performed
NUL	Null	Accomplish time-fill after certain control codes have been received.
STX	Start-of-Text	First character of any message received from the CPU. Prepares the Display Terminal to examine the next data character for the correct DA. If the correct DA is received, the Display Terminal enters the receive mode. If the incorrect DA is received, the message is aborted.
ETX	End-of-Text	Terminates the receive operation unless preceded by an ESC code. If preceded by an ESC code, the ETX character is stored in the delay line.
ENQ	Enquiry	Initiate a transmission of data from the Display Terminal. The ENQ code is used to read the contents of the display terminal delay line even though the operator has not depressed the END (one-step) or XMIT (two-step) keys. This is contrary to the normal polling read directive in that a directive to read under a no transmit condition would normally elicit a 'no business' response.

Table 4-2. Action of ASCII Control Codes During Receive (Cont)

ASCII Code	Meaning	Function Performed
BEL	Bell	When the BEL code is received by the Display Terminal, an internal audible alarm is activated for approximately 170 ms. The CPU normally issues the BEL code to draw attention to a specific message or to a specific portion of the message.
BS**	Back Space	Repositions the cursor one character position to the left.
HT	Horizontal Tab	Repositions the cursor one character position to the right.
LF	Line Feed	Repositions the cursor to the first character position of the next line. This is the only control code automatically stored. (All other codes must be preceded by the ESC code.)
VT	Vertical Tab	Repositions the cursor to the same character position of the next line.
FF**	Form Feed	Repositions the cursor to the frame reset position on the screen (line one, character one).
CR	Carriage Return	Repositions the cursor to the first character position of the next line. This code should not be confused with the LF code, since CR is not stored unless it is preceded by ESC.
DC1*	Device Control One	Performs an erase line edit function. When DC1 is detected, all characters from the cursor to the last character on the line are erased.
DC3*	Device Control Three	Repositions the cursor to the same character position of the previous line

Table 4-2. Action of ASCII Control Codes During Receive (Cont)

ASCII Code	Meaning	Function Performed
CAN*	Cancel	Performs an erase message edit function. When CAN is detected, all characters from the cursor position to the end of the screen are erased.
ESC	Escape	Conditions the Display Terminal to unconditionally store the following character without performing the function indicated by the character. This is true for all control characters except STX. If STX is the next character, the Display Terminal senses a new message segment and ignores the ESC code.

* Since these codes require the performance of a control action that takes a considerable amount of time to accomplish, they must be followed by at least one NUL character.

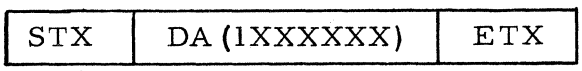
** Since these codes require the performance of a control action that requires an extensive amount of time to accomplish, they must be followed by at least three NUL characters.

4-12 POLLING MESSAGE FORMAT

The message formats for the polling conversational mode are illustrated in figures 4-7 through 4-11 and described in the accompanying text.

4-12.1 Polling Read Directive

The CPU solicits the contents of the display terminal delay line by issuing the message shown in figure 4-7.



DIDS 68-506

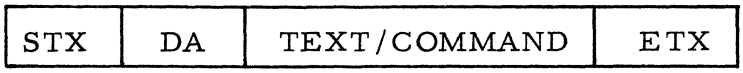
Figure 4-7. Polling Read Directive

a. STX - Described in paragraph 4-11.1a.

b. DA - The six LSB positions of DA (XXXXXX) are used to address a specific Display Terminal. The MSB position (1) is used to indicate a polling read directive.

c. ETX - Described in paragraph 4-11.1e.

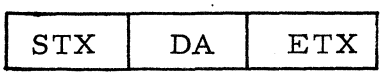
If ETX has been entered and XMIT has been depressed, the Display Terminal responds to the read command by transmitting the contents of the delay line. Transmission begins with the cursor position and terminates when an ETX code is detected. The message format for the display terminal response is shown in figure 4-8. For a definition of terms refer to paragraph 4-11.1a through e.



DIDS 68-507

Figure 4-8. Display Terminal Response to Read Directive if Message Available

If an ETX has not been entered and/or XMIT has not been depressed, the Display Terminal does not have a message available for transmission. If this is the case, the Display Terminal responds with the 'no business' response shown in figure 4-9.



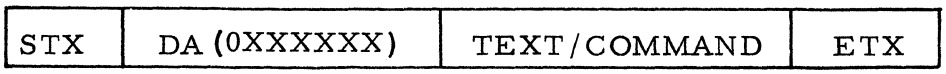
DIDS 68-508

Figure 4-9. Display Terminal Response to Read Directive if No Message Available

4-12.2 Polling Write Directive

The CPU issues the write directive to display a particular message on a specific display terminal screen. When the broadcast address option is employed, by the system, the CPU can display the message on all display terminals modified to recognize the system's broadcast address.

The message format for the polling write directive is shown in figure 4-10.



DIDS 68-509

Figure 4-10. Polling Write Directive

a. STX - Described in paragraph 4-11.1a.

b. DA - The six LSB positions of DA (XXXXXX) are used to address a specific Display Terminal. The MSB position (0) is used to indicate a polling write directive. When the Display Terminal detects a 0 in the MSB of the DA, it enters the receive mode and prepares to accept the remainder of the message.

c. TEXT/COMMAND - Described in paragraphs 4-11.1c and d.

d. ETX - Described in paragraph 4-11.1e.

4-12.3 Polling ENQ Directive

The message format for the polling ENQ directive is shown in figure 4-11.

Figure 4-11. Polling ENQ Directive

The polling ENQ directive is used to solicit information from the Display Terminal even though the display terminal operator has not depressed either transmit key. Essentially the directive message shown in figure 4-11:

a. Moves the cursor to the last character position of the message and inserts an ETX code into the delay line

b. Moves the cursor to the first character position of the message and initiates transmission

c. Causes the Display Terminal to transmit all data between the cursor position and the ETX code

The terms shown in figure 4-11 are described as follows:

a. STX - Described in paragraph 4-11.1a.

b. DA - Described in paragraph 4-12.1b.

c. CURSOR REPOSITION - The cursor reposition segment of the message is used to move the cursor to the last character position of the message. Any cursor reposition code listed in table 4-2 can be used.

d. ESC - The ESC code in this portion allows the next character of the message to be stored in the display terminal delay line. Since the cursor reposition code positioned the cursor to the last character of the message, the following character (ETX) is stored at the last character position. This disables the read function once the message read begins.

e. ETX - The ETX code is stored in the delay line at the point where the message read is to end.

f. CURSOR REPOSITION - The cursor reposition code repositions the cursor to the beginning of the message. Normally, this portion of the message consists of any combination of cursor position codes which will move the cursor to the top of the screen.

g. ENQ - When the Display Terminal decodes the ENQ control code, it enters the transmit mode by setting the ENQ flip-flop. The Display Terminal does not start transmitting data, however, until an ETX code (described below) is received to terminate the receive mode.

h. ETX - The ETX character terminates both the message and the display terminal receive mode. As soon as ETX is received and decoded, the Display Terminal begins transmitting data from the cursor position to the previously inserted ETX code.

SECTION II

FUNCTIONAL DESCRIPTION

4-13 GENERAL DESCRIPTION OF SECTION CONTENTS

This section contains information concerning the operation of the Display Terminal on a block diagram basis. Functionally, the Display Terminal can be divided into several major circuits which work in conjunction to perform specific internal functions. These circuits are grouped and described in detail with respect to purpose and functional operation. Control codes and control keys are discussed on a comparative basis in order to provide a greater understanding of their purpose and relationship.

4-14 OVERALL BLOCK DIAGRAM

The overall block diagram of the Display Terminal is shown in figure 4-12. The Display Terminal is functionally divided into the following circuits:

Character generation and refresh

Buffer register and interface

Editing and cursor control logic

Timing

Raster Generation

Power supplies

4-15 CHARACTER GENERATION AND REFRESH

An important aspect of display terminal operation is the manner in which visual characters are developed for display on the CRT screen. While the operation of these circuits is not difficult to understand, a thorough knowledge of the principles involved is necessary to understand the various editing and cursor control functions.

The character generation circuits consist of two interrelated parts: the keyboard-monoscope circuits and the refresh-memory loop. The keyboard monoscope circuits convert the mechanical depression of a specific character key into a corresponding visual character on the CRT screen. The refresh-memory loop periodically refreshes the displayed character so that a flicker-free presentation remains on the screen until the message is erased.

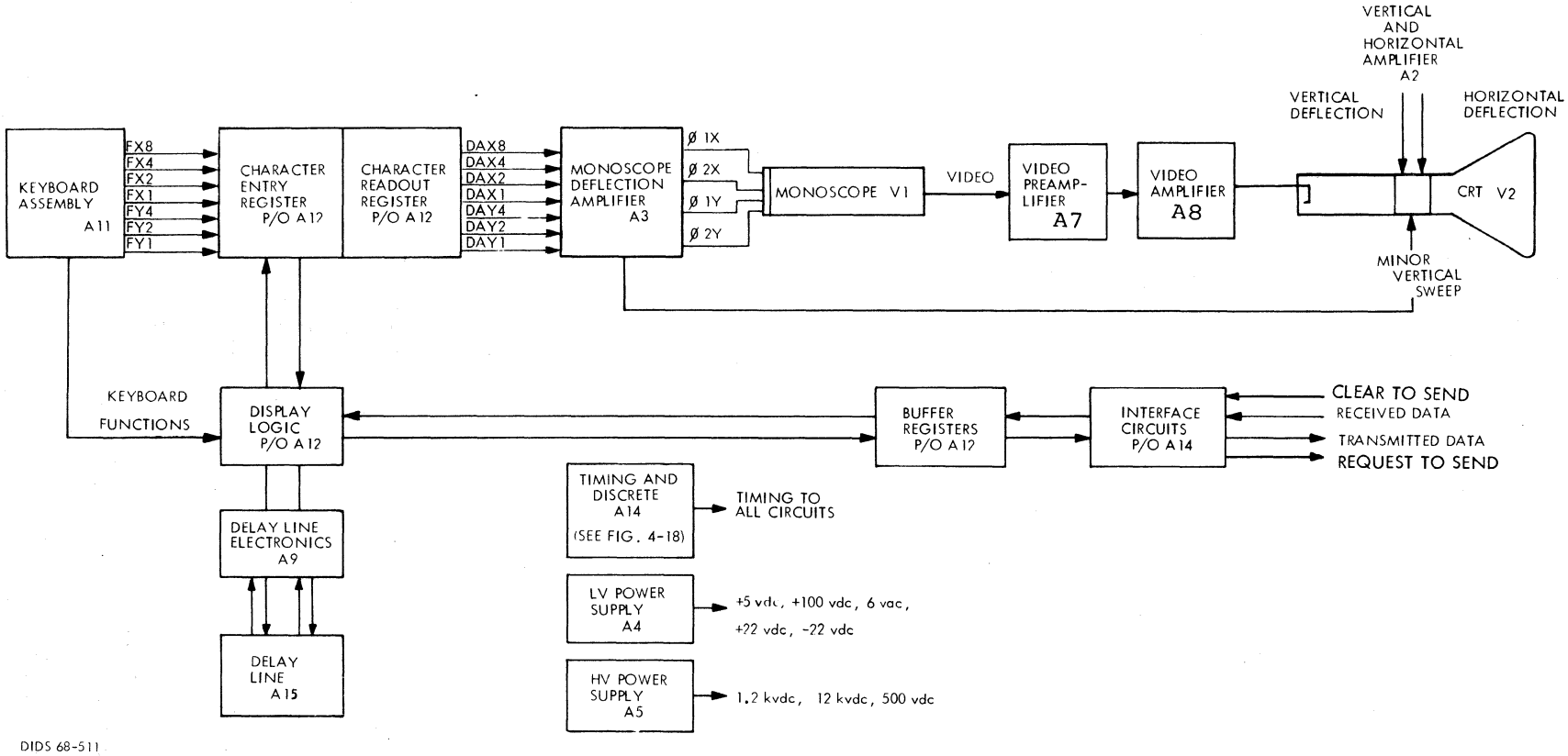


Figure 4-12. Model 402-2AM13 Display Terminal, Overall Block Diagram

4-15.1 Keyboard-Monoscope Circuits

The circuits responsible for developing visual characters for display on the CRT screen are shown in figures 4-13 and 4-14. The development of visual characters begins at the keyboard when the display terminal operator depresses a character key, and terminates at the CRT when a corresponding visual character is produced on the CRT screen.

4-15.1.1 Keyboard Assembly A11

The keyboard functions as a display terminal input by permitting operators to compose, format, and edit data messages for later transmission to the CPU. The keyboard consists of 71 separate keys which are generally divided into two classes: character and function. The term character keys refers to a specific group of keys which are capable of producing visual characters on the CRT screen. The term function keys generally refers to those keys which do not produce visual characters on the CRT screen. Examples of function keys are those used for editing, cursor control, and transmitting data. The function keys are listed and categorized as follows:

Edit Keys

ERASE MSG
ERASE LINE
INSRT
DEL

Cursor Control Keys

←
→
↓
↑

CURSR RESET
ADV LINE
CYCLE
NEW LINE

Transmit Keys

END
XMIT

Entry Control Keys

SHIFT
SHIFT LOCK
CONTROL

Logic Control Key

BREAK

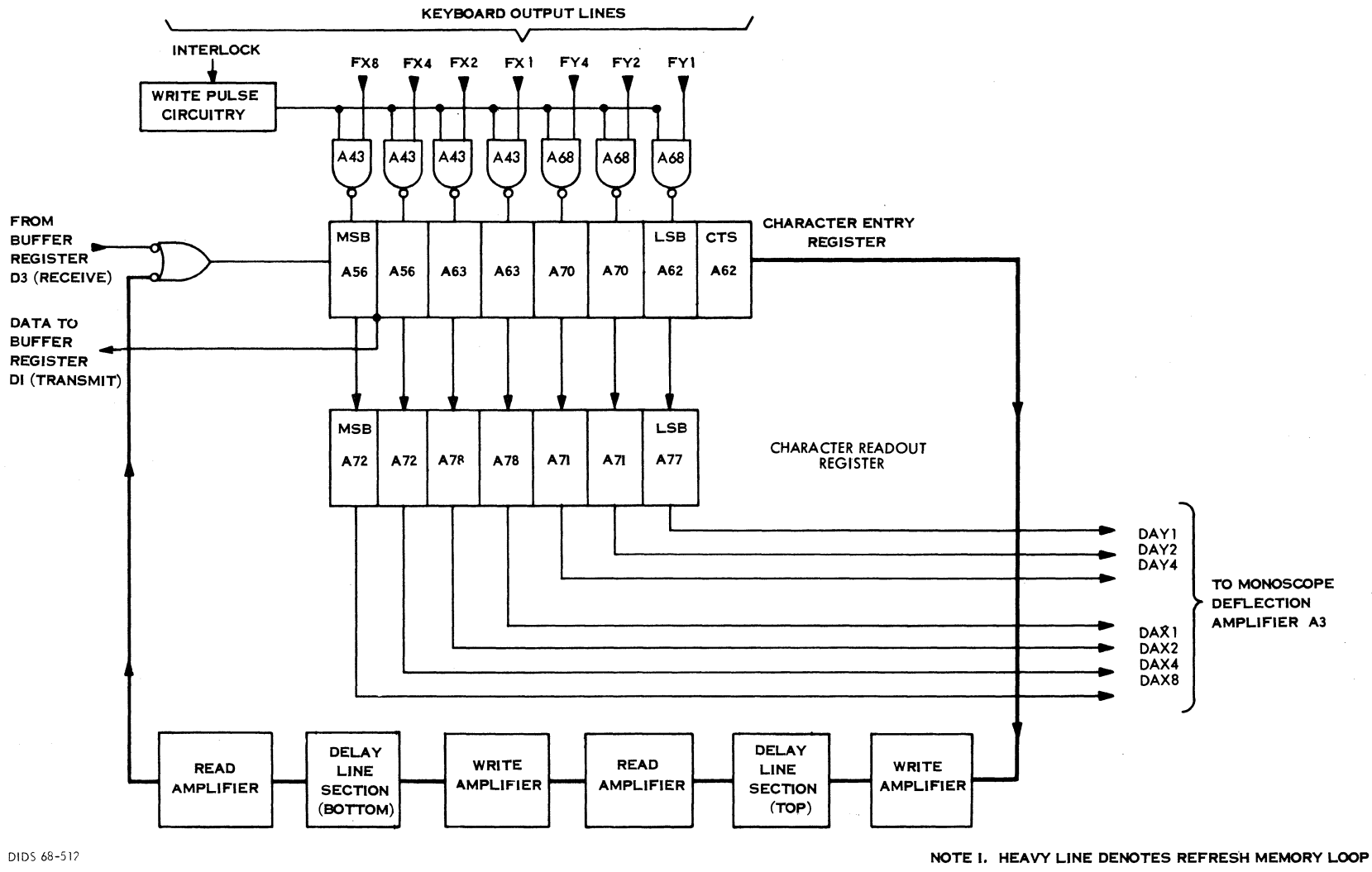


Figure 4-13. Character Entry and Readout Registers and Refresh Memory Loop

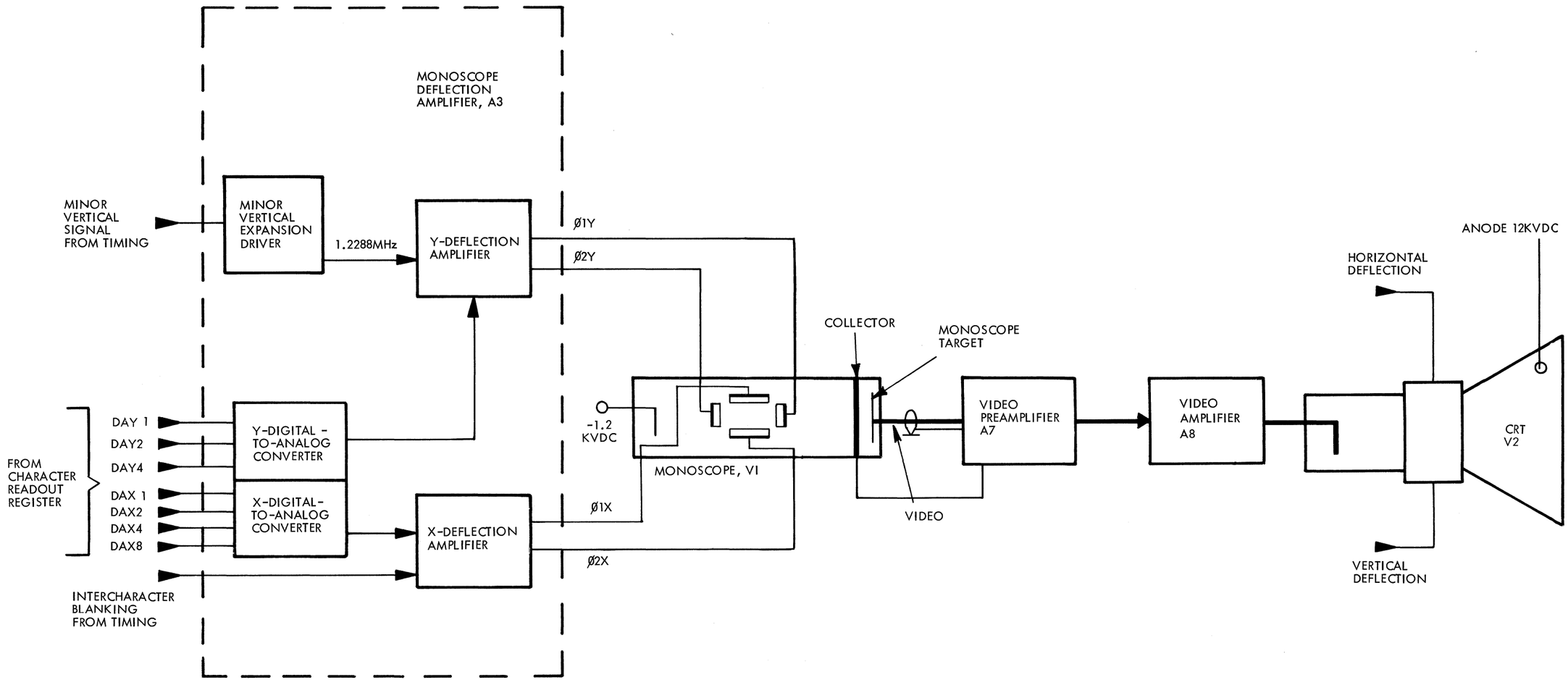


Figure 4-14. Character Generation Circuitry

The function of these keys is to perform a specific control action other than producing visual characters. With two exceptions (END and NEW LINE), these keys acting alone do not produce the digital coding necessary to develop visual characters. Note however, that the entry control keys have a pronounced effect on the coding produced by a character key depression, and therefore on the visual character produced

When any character key is depressed, a magnetically actuated reed switch within the key allows current to flow through a branch of the keyboard matrix. The matrix output, which consists of a specific 7-bit digital code, is coupled over seven output lines designated FX1, FX2, FX4, FX8, FY1, FY2, and FY4. In addition to the digital code output, a strobe level (INTERLK) is produced each time a character key is depressed. This strobe pulse is used to determine that a character key has been depressed and subsequently to strobe the 7-bit digital code into the character entry register.

Most of the character keys have three separate binary codes that may be developed, depending upon the circumstances present when the key is depressed. The three codes represent the lower case, upper case, and control modes. A complete summary of character keys and their coding is listed in table 4-3. LC, UC, and C are defined as follows: the code opposite LC is produced when only the character key is depressed; the code opposite UC is produced when the character key and the SHIFT key are depressed simultaneously; and the code opposite C is produced when both the character key and the CONTROL key are depressed simultaneously. The codes listed in table 4-3 are the actual inputs to the character entry register under the circumstances indicated. The character entry register is described in the following text.

Table 4-3. Keyboard Characters and Coding

Key	Mode	ASCII Code
<	C UC LC	 011 1100
! |	C UC LC	 010 0001 011 0001
" 2	C UC LC	 010 0010 011 0010
# 3	C UC LC	 010 0011 011 0011
$ 4	C UC LC	 010 0100 011 0100

Table 4-3. Keyboard Characters and Coding (Cont)

Key	Mode	ASCII Code
% 5	C UC LC	 010 0101 011 0101
& 6	C UC LC	 010 0110 011 0110
' 7	C UC LC	 010 0111 011 0111
(8	C UC LC	 010 1000 011 1000
) 9	C UC LC	 010 1001 011 1001
Ø	C UC LC	 011 0000
= -	C UC LC	 011 1101 010 1101
U DEL S _	C UC LC	001 1111 111 1111 101 1111
G } S]	C UC LC	001 1101 111 1101 101 1101
R ~ S ^	C UC LC	001 1110 111 1110 101 1110
F | S \	C UC LC	001 1100 111 1100 101 1100

Table 4-3. Keyboard Characters and Coding (Cont)

Key	Mode	ASCII Code
<	C UC LC	 011 1110
ETB W	C UC LC	001 0111 101 0111 111 0111
ENQ E	C UC LC	000 0101 100 0101 110 0101
DC2 R	C UC LC	001 0010 101 0010 111 0010
DC4 T	C UC LC	001 0100 101 0100 111 0100
EM Y	C UC LC	001 1001 101 1001 111 1001
NAK U	C UC LC	001 0101 101 0101 111 0101
HT I	C UC LC	000 1001 100 1001 110 1001
SI O	C UC LC	000 1111 100 1111 110 1111
DLE P	C UC LC	001 0000 101 0000 111 0000
NUL \ @	C UC LC	000 0000 110 0000 100 0000
NEW LINE	C UC LC	 000 1010

Table 4-3. Keyboard Characters and Coding (Cont)

Key	Mode	ASCII Code
SOH A	C UC LC	000 0001 100 0001 110 0001
DC3 S	C UC LC	001 0011 101 0011 111 0011
EOT D	C UC LC	000 0100 100 0100 110 0100
ACK F	C UC LC	000 0110 100 0110 110 0110
BEL G	C UC LC	000 0111 100 0111 110 0111
BS H	C UC LC	000 1000 100 1000 110 1000
LF J	C UC LC	000 1010 100 1010 110 1010
VT K	C UC LC	000 1011 100 1011 110 1011
FF L	C UC LC	000 1100 100 1100 110 1100
+ ;	C UC LC	 010 1011 011 1011
* :	C UC LC	 010 1010 011 1010
ESC ([	C UC LC	001 1011 111 1011 101 1011

Table 4-3. Keyboard Characters and Coding (Cont)

Key	Mode	ASCII Code
SUB Z	C UC LC	001 1010 101 1010 111 1010
CAN X	C UC LC	001 1000 101 1000 111 1000
ETX C	C UC LC	000 0011 100 0011 110 0011
SYN V	C UC LC	001 0110 101 0110 111 0110
STX B	C UC LC	000 0010 100 0010 110 0010
SO N	C UC LC	000 1110 100 1110 110 1110
CR M	C UC LC	000 1101 100 1101 110 1101
, '	C UC LC	 010 1100 010 1100
. .	C UC LC	 010 1110 010 1110
? /	C UC LC	 011 1111 010 1111

4-15.1.2 Character Entry Register

The character entry register (see figure 4-13) is an 8-bit flip-flop register contained on display logic board A13. The character entry register performs a two-fold function in terms of character generation: keyboard interface, and refresh-memory access.

When a character key is depressed, the 7-bit digital code produced by the matrix is available for character entry. However, characters cannot be entered from the keyboard until a special bit, called the cursor, is located in the refresh-memory loop. The refresh-memory loop constantly circulates this bit, and it appears in the character entry register only once/frame. The cursor bit is associated with the visible cursor (⌋) on the screen and characters can be entered only at the cursor position. Thus, characters can be strobed into the character entry register only every 16.026 ms (the frame time). Since keys cannot be depressed this fast, it is practical to assume that the character code enters the register as soon as the character key is depressed. The character code is entered into logic by first locating the cursor and combining the presence of the cursor with a strobe pulse generated from the presence of an INTERLK level.

Once a character enters the character entry register, it is immediately parallel-shifted into the character readout register and serially shifted, bit by bit, into the refresh-memory loop.

4-15.1.3 Character Readout Register

The character readout register (see figure 4-13), is a 7-bit register located on display logic board A13. The character readout register is connected in parallel with the character entry register. Therefore, when a character code is present in the entry register, it is simultaneously present in the readout register. The character code is held in the readout register for one complete character time before being replaced with the next code entered from the keyboard (or from the refresh-memory loop).

The output from the character readout register comprises the original keyboard output code divided into two segments. One segment consists of the four most significant bits (MSB's) of the character; the second segment, the three least significant bits (LSB's). All seven bits are coupled to the monoscope deflection amplifier and applied to X and Y digital-to-analog (D/A) converters.

4-15.1.4 Monoscope Deflection Amplifier A3

The purpose of the monoscope deflection amplifier is to convert digital character codes to analog voltages for electrostatically deflecting the monoscope scan. The monoscope scan when positioned to a specific character image on the monoscope target produces a video output by secondary emission that is peculiar to the particular character being scanned (refer to figure 4-14).

The four MSB's arriving from the character readout register are applied to a D/A converter to produce an X-axis deflection voltage. This voltage is amplified and applied to the monoscope X-axis deflection plates to position the scan on the appropriate column of the monoscope target font.

The three LSB's arriving from the character readout register are also D/A converted to develop a Y-axis deflection voltage. This voltage is combined with the minor vertical expansion voltage and amplified before being applied to the Y-axis deflection plates. The purpose of the Y-deflection voltage is to position the scan to the appropriate row of the monoscope target font. Each of the 96 character images etched into the monoscope target can be accessed in this manner.

An intercharacter blanking signal is applied to the X-deflection amplifier between each character time. This signal, developed by the timing circuitry, produces a sawtooth ramp signal which sweeps the scan across each character, then cuts off the amplifier when the monoscope beam is repositioned to the next character position.

The minor vertical expansion voltage (mentioned in previous text) is a sine wave signal that occurs at a rate of 1.2288 MHz. This signal amplitude modulates the Y-deflection voltage producing a composite voltage that varies at the minor vertical expansion rate. Although the monoscope scan is positioned to only one of 96 character positions, the beam cannot be entirely stable because of the modulating voltage. This modulating voltage causes the scan to alternately sweep up and down in a vertical direction several times before the scan is repositioned to another character. This painting motion provides a high degree of character resolution by enabling several scans of the character symbol.

4-15.1.5 Monoscope, Amplifiers, and CRT

The monoscope, amplifiers, and CRT are respectively used to develop, amplify, and display actual visual characters. The preceding text has described the method employed to position the monoscope scan to a specific position on the target; the following explanation describes what occurs when the beam is properly positioned.

The monoscope tube is a vacuum tube device designed to function similarly to a conventional electron gun. An electron beam is formed within the tube by placing a high negative potential on the cathode element and operating the collector at or near ground potential. The resulting accelerated electron beam is electrostatically deflected to bombard one position on the target element. The target element consists of an etched aluminum disk with a character font identical to that shown in figure 4-3. As the beam is directed to a particular character of the font, secondary emission produces a low current video output peculiar to the particular character being scanned. This video signal is amplified twice by video preamplifier A7 and video amplifier A8 before being applied to the CRT cathode.

The CRT is also a conventional electron gun with the anode operated at a high positive potential (with respect to the cathode element). The video level applied to the cathode alternately increases and decreases CRT conduction, and the changing phosphor excitement produces a visual character on the screen. The CRT deflection voltages determine where on the screen the character will appear. Deflection voltages are developed by display terminal timing and CRT deflection circuits which are described in paragraphs 4-18 and 4-19.

4-15.1.6 Summary

The preceding text has briefly explained the operation of the keyboard monoscope circuits and the manner in which visual characters are developed from the depression of a character key. Once a character is displayed, however, it begins to fade from view as soon as the monoscope scan is deflected to another character. The time required for a character to disappear is determined by the persistence of the CRT screen phosphor material which is type P31 (green) short-persistence. To prevent this fading, the displayed character is refreshed by circulating the digital code of the character in the refresh memory loop.

4-15.2 Refresh-Memory Loop

The purpose of the refresh-memory loop is to provide a constant refresh of visual characters displayed on the CRT screen. The key to understanding the refresh memory loop is to remember the following two points: (1) the character entry register is parallel-connected to the character readout register, and (2) digital character codes held in the character readout register are used to position the monoscope scan, and thus develop a corresponding visual character on the CRT screen.

Digital character codes, whether entered from the keyboard or received from the CPU, enter the refresh-memory loop at the character entry register. If the character code is formed locally by the depression of a key on the keyboard, the code is entered by jamming it into the entry register. If the character code is received from the CPU, it is serially shifted into the entry register from buffer register D3. At the end of each character time, the code is parallel-transferred into the character readout register and a corresponding character is displayed on the CRT screen. Character codes are constantly returned to the character entry register for redistribution to the monoscope deflection circuitry. This in turn maintains visual character brightness on the CRT screen.

The refresh-memory loop (shown in figure 4-13) consists of the character entry register, delay-line electronics A9, and delay line A15. After character codes initially enter the refresh-memory loop, the code is returned every 16.026 ms, or at a rate of 63 times/second. This time corresponds to the time required for the CRT scan to move from a character position on the screen, through a complete scan cycle, and back to the original character position. For example, assume that the cursor is located at the line one, character one position on the screen when a character key is depressed. The cursor is constantly circulating in the loop and eventually appears in the cursor-located flip-flop of the character entry register. When the cursor is located, the write pulse strobes the character code into the entry register and a visual character is displayed on the CRT screen at the line one, character one position.

The character code is then serially shifted out of the entry register until, after one character time (seven bit times), the following conditions are true: (1) the character entry register is cleared to form an IDLE code, (2) the character readout register now contains an IDLE code (all 1's), (3) the last bit of the character code has just entered delay-line electronics, and (4) the CRT scan has moved to the next character position on the screen.

In 16.026 ms, the character is returned to the character entry register, and simultaneously the CRT scan is again at the line one character one position. Thus, the character is again visually displayed and the screen presentation is refreshed.

4-15.2.1 Delay-Line Electronics A9

The purpose of the delay-line electronics is to compensate for data attenuation incurred in the delay line. The circuit consists of two combination read-write amplifiers which are connected in a series configuration between delay-line sections.

Serial bit data from the character entry register is applied to the first write amplifier and amplified to a level sufficient to drive the input transducer of the first delay-line section. The data passes through the delay line and appears as an attenuated replica at the output transducer. The data is then amplified to its original level by the first read amplifier and applied to the second write amplifier. The process is repeated for the second delay-line section and, after encountering a total delay of 16.026 ms, the data is serially shifted into the character entry register.

4-15.2.2 Delay Line A15

The purpose of the delay line is to provide an economic means of storing up to 1040 data characters and 192 retrace characters in a compact area. (Retrace characters are actually not characters at all but merely blank spaces in the delay line.) Data characters stored in the delay line are used to constantly refresh the CRT screen presentation. In addition, during the transmit sequence, data characters are serially shifted out to the CPU upon the operator's or the CPU's command.

The delay line consists of two separate sections which are series-connected between the delay-line electronics read-write amplifiers. Each section is capable of storing 520 characters plus retrace, thus providing a total capability of 1040 displayable character storage. The delay-line sections (referred to as the top and bottom sections) are electrically identical except for circuit placement in the refresh memory loop.

As shown in figure 4-15, each delay-line section consists of the following parts: an input transducer, magnetostrictive tapes, and transmission wires. The input and output transducers are connected to the magnetostrictive tapes, which are in turn welded to each end of the transmission wire.

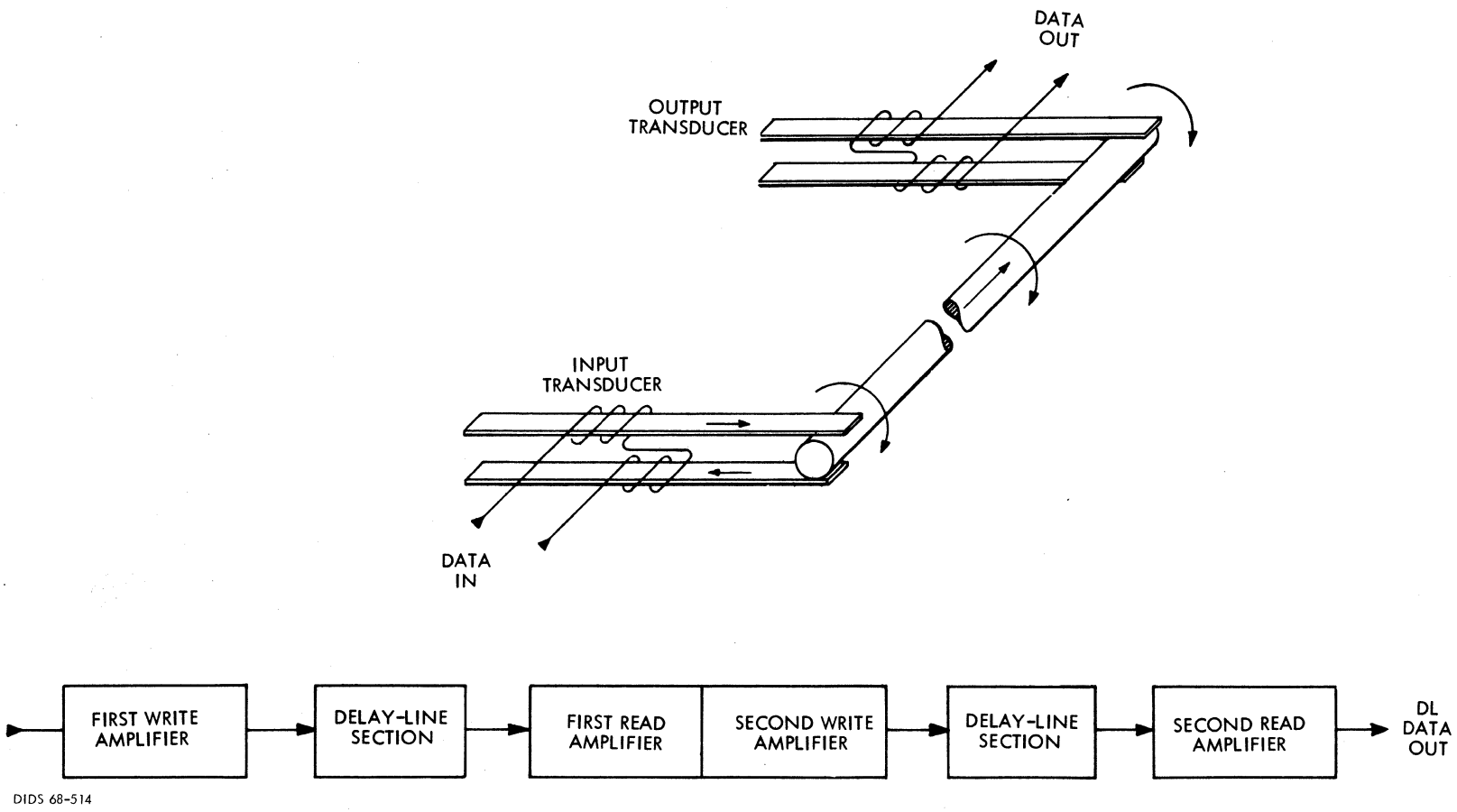


Figure 4-15. Delay-Line Memory Section, Simplified Diagram

Data bits, in pulse form, are coupled from the first write amplifier and enter the top delay-line section at the input transducer. The transducer converts electrical energy to mechanical energy which is used to push one magnetostrictive tape while pulling the other. The back and forth movement of the magnetostrictive tapes twists the input end of the transmission wire. This twisting motion travels down the transmission wire at a rate of 9 μs/in. and is present at the opposite end of the wire after a certain delay in time.

At the output end of the transmission wire, the twisting movement moves a second pair of magnetostrictive tapes which couple mechanical movement to the output transducer. The output transducer converts this mechanical energy to electrical energy, and the original data bit is reproduced. The total delay encountered by the pulse while traveling from the input to the output is approximately equal to 8.013 ms.

From the output transducer, data bits are amplified by the read section of the first read-write amplifier and coupled to the second write-amplifier. From this point, the same circuit action previously described occurs and a second 8.013-ms delay is encountered. Thus, a total of 16.026-ms delay is encountered in the delay-line portion of the refresh memory. This delay corresponds to the CRT frame time.

4-16 BUFFER REGISTERS AND INTERFACE

The buffer registers and their associated interface circuits are shown in figure 4-16. These registers provide a buffer between the high-speed refresh memory and the relatively slow speed CPU interface circuits.

The buffer registers perform the following major functions.

In the transmit mode:

Generate STX and DA in D2 and D3 to initialize the transmitted message

Provide a temporary storage of memory data so that a smooth transmission of data at 1200 baud is possible

In the receive mode:

Provide a means to decode numerous control codes and message initialization and termination characters

Provide a means for cancelling characters received with improper parity

Operation of the buffer registers during transmit and receive modes is described below.

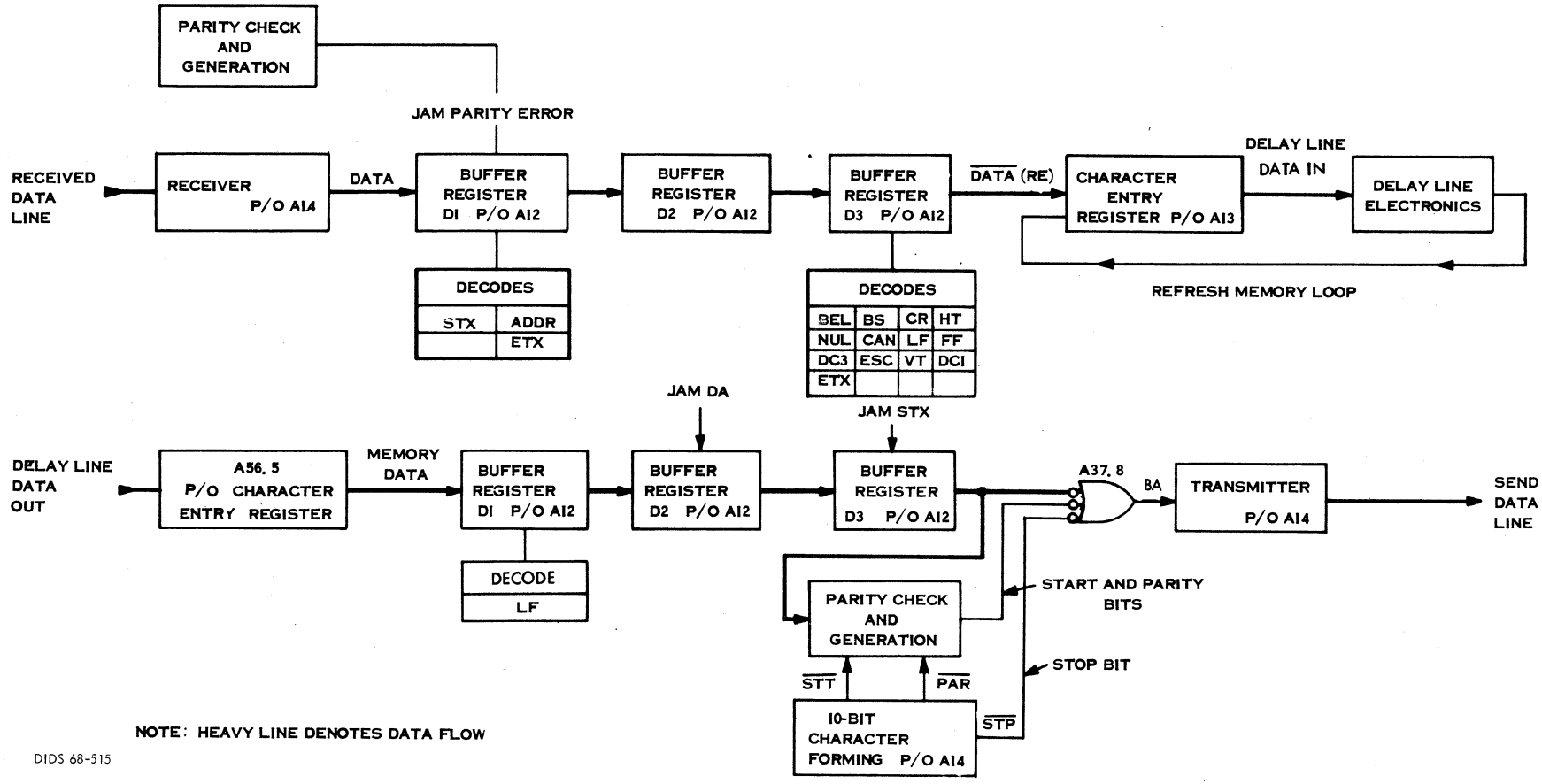


Figure 4-16. Buffer Registers and Interface

4-16.1 Transmit Mode

In the transmit mode, the buffer registers are used to release a steady stream of serial bit data at the 1200-baud transmission rate. As data is recirculated in the refresh memory 63 times a second, the cursor appears in the CTS flip-flop of the character entry register every 16.026 ms. Each time the cursor appears, data can be extracted from the refresh memory loop and shifted into the buffer registers for transmission to the CPU.

If only one character were extracted each time the cursor appeared, the maximum transmission rate would be 63 characters/second. To achieve the desired 120 character/second rate, at least one, and usually two, characters must be extracted each time the memory is accessed. The purpose of the buffer registers is to temporarily hold these characters until they can be shifted out to the CPU by the 1200-baud circuitry.

To initiate data messages, display terminal operators type in the desired text and then depress the END key. The END key places an ETX code in memory and enables the XMIT key. When XMIT is then depressed, a signal is developed which jams STX into buffer register D3 and the correct DA into buffer register D2. (In Display Terminals employing the One-Step Transmit option, depression of only the END key develops this signal.) With STX in D3 and DA in D2, the Display Terminal is ready to transmit data to the CPU. As soon as the cursor is located, the first data character is shifted into buffer register D1 from the character entry register. Once the registers are filled, the cursor is released and again permitted to circulate in the refresh memory loop.

With a 7-bit character held in buffer register D3, a start bit is generated by the 10-bit character forming network. Data held in D3 is then serially shifted at 1200 baud to both the parity check and generation circuit and to a transmitter driver circuit on A14. At the end of 8 bit-times, a parity bit is generated by the parity check and generation circuitry. During the next bit-time, a stop bit is placed on the line to complete the formation of the 10-bit character.

To summarize the transmit mode, the flow of data is from the delay-line memory into a portion of the character entry register. From this point, serial data is transferred through buffer registers D1 and D2 by the high-speed internal timing into D3. From buffer register D3, data is shifted at 1200 baud during the proper bit-times (bits b_1 through b_7) to the send data transmitter and then out to the CPU I/O device over the transmitted data line. Both before and after actual data transfer, start, stop, and parity bits are generated to complete the 10-bit transmitted character.

4-16.2 Receive Mode

In the receive mode, the buffer registers are used to provide temporary storage of data received from the CPU. As each received character is held in buffer registers D1 and D3, several parallel-connected decodes are employed to examine the character coding.

When the Display Terminal is not actively transmitting data, digital information on the received data line is permitted to enter buffer register D1. However, data received from the CPU is not gated to the remaining buffer

registers until the initial characters of a message are detected (STX and DA). When STX is received and the next character is the proper DA, clock pulses are applied to the remaining buffer registers and all the following characters are permitted to enter D2 and D3. Data is accepted until an ETX is decoded in D1, at which time the receive mode is terminated.

As each character is received, the parity check and generation circuitry is employed to check each character for the proper parity. If an erroneous character is received, a parity error signal jams a parity error SUB code into buffer register D1. This code appears on the CRT screen as a blank at the erroneous character position.

In buffer register D3, one of three control actions occurs depending upon the binary value of the character code held in the register. As shown in figure 4-16, several decodes are connected to buffer register D3. These decodes are used to detect special control characters received from the CPU. (The control action performed when these special codes are received is explained in table 4-2.)

Normally, the character code held in buffer register D3 is one of the displayable characters. If this is the case, the character code enters the delay-line electronics and is displayed on the CRT screen in the usual manner.

If the character held in buffer register D3 is one of the numerous control codes, the applicable decode produces an output which is used to perform the control action called for by the code. Generally, control characters are not entered into the delay line from D3 unless the character in the register was immediately preceded by an ESC code. (The exception to this rule is LF which is always stored.) Assuming the DC3 control code is received and shifted into buffer register D3, a back-line function is initiated. The code is not stored in the delay line and no visible effect (other than cursor movement) is noticeable on the screen.

The third control action occurs when a control code (such as DC3) is received immediately after an ESC code. When this occurs, the function is not performed and the DC3 code is stored in the delay line. A blank space appears on the CRT screen at the DC3 character position and a visible character (lower case) appears on the screen when the CONTROL key is depressed.

To summarize the receive mode, the flow of data is from the received data line, through the buffer registers, and into the delay-line refresh-memory loop. The data circulating in memory appears on the screen as a visible message until the delay line is cleared by the local operator or by the reception of a CAN control code from the CPU.

4-17 EDITING AND CURSOR CONTROL LOGIC

The purpose of the editing and cursor control logic is to permit local operators or CPU programs to edit and format messages displayed on the CRT screen. These circuits are contained on Display Logic Board A13 and consist of the following principal parts:

Individual function flip-flops

Sample strobe flip-flops

Function complete flip-flops

Input and output display logic

Insert and 12-count register

88-count register

In any cursor control operation, data circulating in the refresh-memory loop is unaltered by the initiation of the operation. The cursor, which is a moveable bit circulating in the refresh-memory loop, is always attached to one character of the message. The purpose of the various cursor control operations is to locate and move this cursor from one character position to another. This repositioning may appear on the CRT screen as a cursor movement to one of the following positions:

Cursor stepped left or right one character position

Cursor stepped up or down to an adjacent line

Cursor advanced to the first character position of the next line

Cursor moved to the frame reset position

Contrary to cursor control operations, the various editing operations are designed to alter in some manner the data circulating in the refresh-memory loop. This alteration can appear on the CRT screen as one of the following:

Character insert

Line insert

Character delete

Line delete

Line erase

Message erase

As shown in figure 4-17, the editing and cursor control logic can gain access to refresh-memory data both before and after it enters the delay line or character-entry register. Since the character-entry register is series connected in the refresh-memory loop, one of the 1040 characters circulating in the loop will always be present in the register. For any of the edit or cursor control operations to be initiated, the character in the register or the character preparing to enter the register must have the cursor bit attached to it. In previous explanations it was established that only one of the characters in memory has the cursor bit

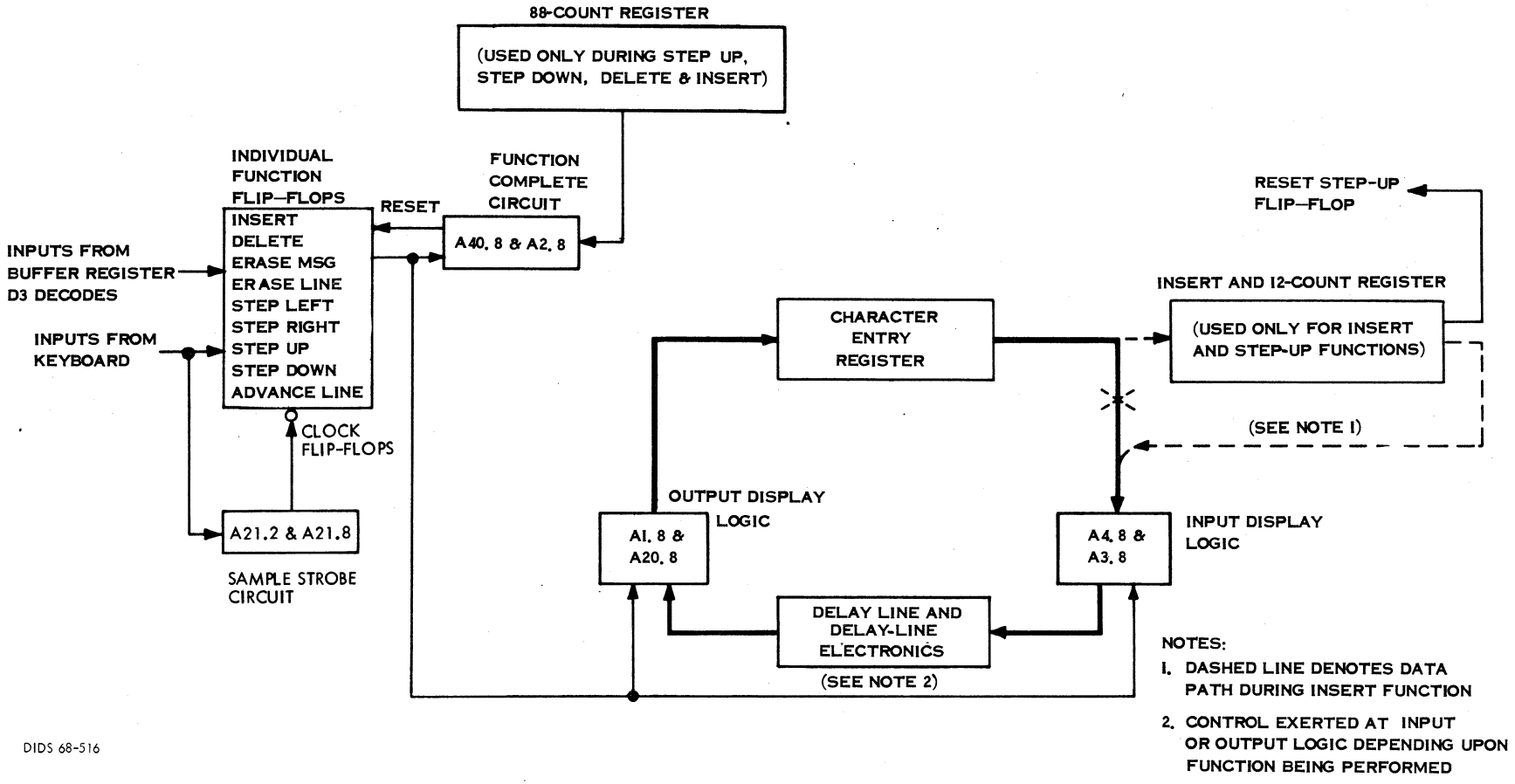


Figure 4-17. Editing and Cursor Control Logic, Block Diagram

attached. The remaining characters, however, can accept the cursor; this is the main purpose of cursor control operations ... to remove the cursor from one character and attach it to another.

The following text briefly describes the function of each portion of the editing and cursor control logic (see figure 4-17).

4-17.1 Individual Function Flip-Flops

The individual flip-flops used to accomplish the various operations are normally operated independently, but in some cases are connected to other function flip-flops. An example of this is the relationship between the step-right and advance-line flip-flops where the step-right operation causes an advance line if it occurs at the end of a line.

To initiate an operation, signals are coupled from either the keyboard assembly or control code decodes connected to buffer register D3. When any keyboard keys are depressed, a high-to-low going level is developed; this level is coupled to both the flip-flop associated with the key and the sample strobe circuit. The sample strobe pulse developed by this circuit is used to clock the keyboard signal into the appropriate flip-flop.

4-17.2 Sample Strobe Circuit

The sample strobe circuit consists of two interconnected flip-flops (A21.2 and A21.8) which are used to prevent the repetition of an operation when the function key is held depressed. To accomplish this, only the first frame pulse after the key depression is permitted to clock the individual function flip-flop. This frame pulse then becomes the sample strobe pulse and is used to clock the appropriate flip-flop. To repeat the function, the key must be released and depressed again or the CYCLE key must be depressed. When the CYCLE key is held depressed in conjunction with any function key, the function is repeated by a sample strobe which reoccurs at 6 Hz. The second detent position of the → (step right) and ← (step left) function keys operates in a similar manner to repeat the function at a 12-Hz rate.

The function-complete circuit consists of flip-flop A40.8 and associated OR-gate A2.8. The purpose of the function-complete flip-flop is to reset the individual function flip-flop on the trailing edge of the cursor at the completion of an operation. Exceptions to this rule are the step-up, insert, and delete-function flip-flops which are reset by other circuits.

4-17.3 Input and Output Display Logic

The input and output display logic consists of series-connected OR-gates at both the input and output of the delay-line electronics.

The input display logic consists of OR gates A3.8 and A4.8. Depending upon the operation initiated, data is inhibited, altered, or permitted to pass unchanged as it leaves the character entry register and passed through the OR-gates to the delay-line electronics.

The output delay logic consists of OR-gates A1.8 and A20.8. Similar to the input display logic, the specific action taken on data as it leaves the delay line and prepares to enter the character entry register is dependent upon the operation initiated.

4-17.4 Insert and 12-Count Register

The insert and 12-count register is a 7-bit register used to assist in performing the step-up and character-insert operations. Normally, the register contains an IDLE character (all 1's) when it is not being employed by the editing and cursor control logic.

In the insert operation, the insert and 12-count register is connected in series with the refresh-memory loop, and the normal data path is interrupted. This allows the IDLE character stored in the register to be inserted into the memory loop as a blank at the cursor position. The character previously associated with the cursor, as well as all remaining characters on the line, are now shifted into refresh memory via the insert and 12-count register. When the insert operation is terminated, the register is removed from the circuit and the normal data path is reestablished.

In the step-up operation, the insert and 12-count register functions as a line counter. To accomplish a step-up, the cursor is moved from its character position on a line to the same character position on the line above. The 12-count register assists in this function by counting the number of active lines after the initiation of the step-up operation. When the counter reaches the count of 12, circuits elsewhere in the display logic place the cursor in the proper character slot of the previous line. The 12-count output also resets the step-up flip-flop and terminates the operation.

4-17.5 88-Count Register

The 88-count register is employed by the editing cursor control logic for each operation requiring a count of the number of characters per line. The functions requiring the 88-count register are: step-up, step-down, insert line, and delete line. Normally, the counter is held at a count corresponding to binary zero. Once the counter is instructed to count, it begins counting in binary until a count of 88 is decoded by AND-gate A36.8. In the step-down cursor control, it is necessary for the counter to count to 88 only once. In the remaining functions, however, the counter continues in the sequence 0-88-0-88, etc., until the function is completed.

4-18 TIMING

All the display terminal timing circuits are located on timing and discrete board A14. The internal timing consists of the various counters shown in figure 4-18. A crystal-controlled master oscillator supplies a 'raw-clock' output of 2.4576 MHz, which is counted down by numerous dividers to arrive at the internal timing signals. In addition, a free running multivibrator is used to provide cycling frequencies of 6 Hz and 12 Hz for cycling selected display terminal functions.

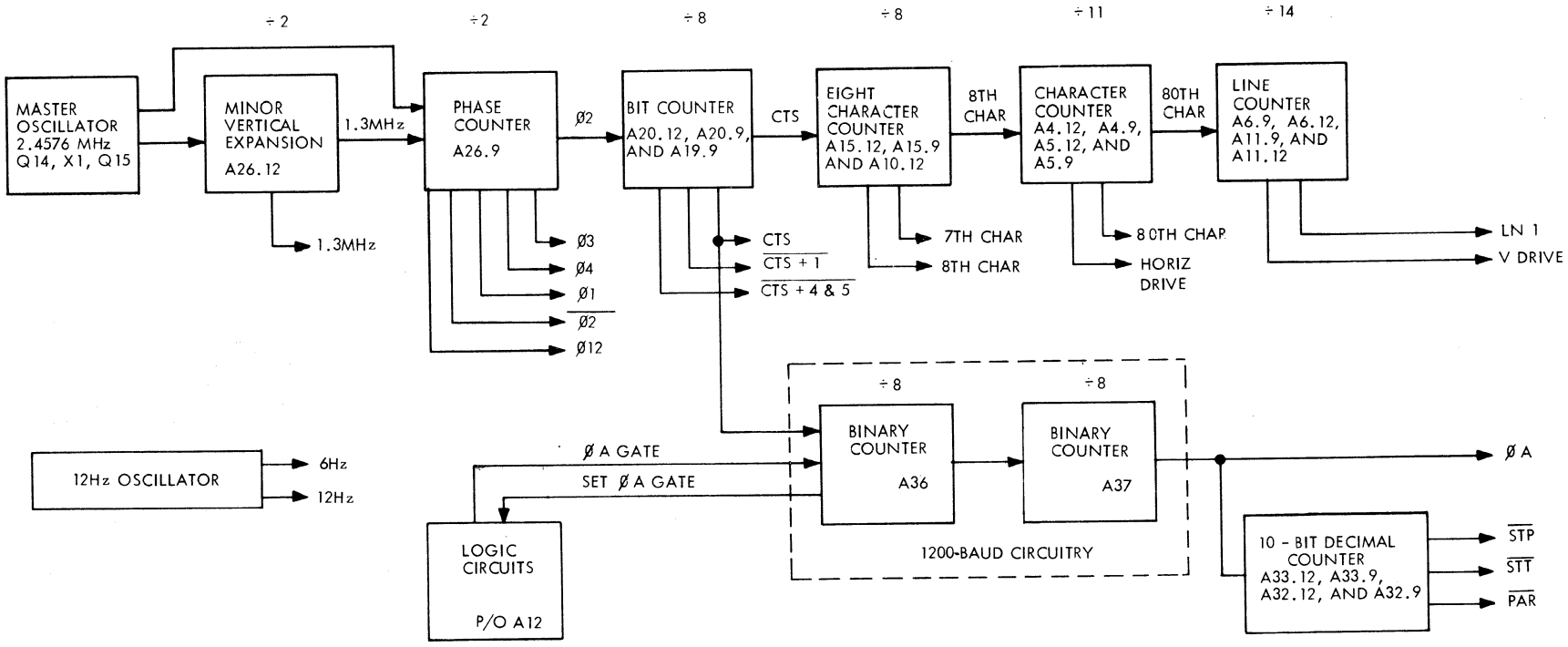


Figure 4-18. Timing Circuits, Block Diagram

4-18.1 Master Oscillator

The master oscillator circuitry consists of oscillator transistor Q14, crystal X1, and saturated switch Q15. The 2.4576-MHz oscillator output is used to provide master clock input for clocking the minor vertical expansion and phase counter flip-flops.

4-18.2 Minor Vertical Expansion

The minor vertical expansion circuit functions as a divide-by-two counter and is formed by flip-flop A26.12.

The 1.2288 (1.3)-MHz output is coupled to the monoscope and CRT deflection circuits and is used to increase the height and clarity of characters displayed on the CRT screen.

4-18.3 Phase Counter

The phase counter consists of a second divide-by-two counter and is formed by flip-flop A26.9. By properly combining the master clock, minor vertical, and phase counter outputs, four phases of master clock are developed.

The phase counter produces outputs which occur in coincidence with the first, second, third, and fourth master clock inputs. These inputs are commonly known as phases 3, 4, 1, and 2, respectively. An additional output, phase 12 (pronounced one-and-two), is produced by directly decoding the set output of the phase counter flip-flop.

Internally, the phase counter outputs are used to enable circuit operation at the beginning, middle or end of each bit. The timing relationship is such that the time span from phase 3 to phase 2 is equal to one bit time (see figure 4-19). In the Display Terminal, gating functions required at the beginning of a bit are accomplished during phase 3, while those at the end of a bit are accomplished during phase 2. The remaining phase counter outputs are used to perform gating during the center of a bit time.

The phase 2 output is used within the timing circuitry as a clock input to the bit counter; thus, the bit counter is toggled at the end of each bit time.

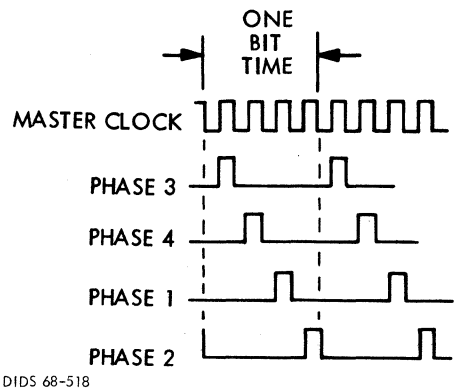


Figure 4-19. Phase Counter Outputs

4-18.4 Bit Counter

The bit counter consists of three flip-flops connected in a divide-by-eight countdown circuit. Three outputs are produced by the bit counter:

a. CTS - The cursor time slot timing pulse is the timing equivalent to the cursor bit. From previous discussions, the cursor is a moveable bit in memory which is attached to the LSB of a data character. The CTS output is primarily used to either locate the cursor or cause an operation to be performed in coincidence with the cursor.

b. CTS +1 - The cursor time slot plus one timing signal occurs in coincidence with the least significant data bit of a character and is used primarily to enable data transfers through the buffer registers.

c. CTS +4 and 5 - This timing pulse is decoded for use in conjunction with the monoscope 'shift-off-screen' circuitry. When a NULL character is detected in the character readout register (indicating that a standard letter, numeral or symbol will not be displayed), the monoscope beam is positioned to a small box (■) symbol at the edge of the target. The purpose of this decoded output is to limit the monoscope active scan interval to four bit times. This prevents 'burning' the frequently used symbol and thereby lengthens the usable life of the monoscope tube.

The decoded CTS pulse is one bit time in width and occurs once every 13 μs. CTS is used within the timing circuitry to clock the eight-character and binary counters. For a timing relationship between the bit counter outputs and memory data, refer to figure 4-20.

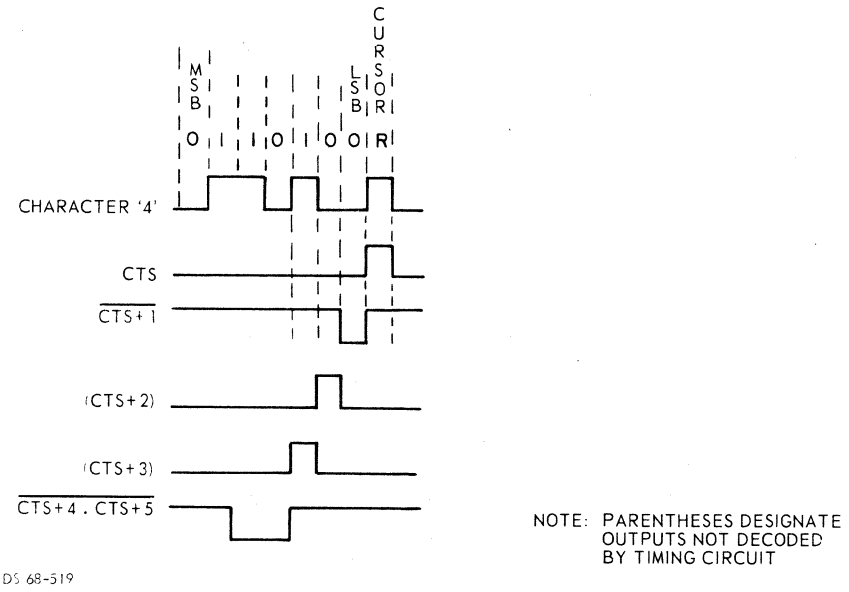


Figure 4-20. Bit Counter Outputs and Memory Data Relationship

4-18.5 Eight-Character Counter

The purpose of the eight-character counter is to count down the output of the bit counter to develop a decoded output every eight CTS (character) times. The eight-character counter has two outputs which are described as follows:

a. 7th Character - This output occurs during CTS of the seventh character counted. There are 80 displayable and 8 retrace characters per line. The 7th character decode produces an output during the following character counts where 1 is equal to the first displayable character of the line: 7, 15, 23, 31, 39, 47, 55, 63, 71, 79, and 87. The 7th character output is used to assist in producing the LWL pulse during character count 79 and the Δ pulse during character count 87.

b. 8th Character - This output is produced during CTS of the eighth character counted. Of the 88 characters per line, this output occurs during character counts 8, 16, 24, 32, 40, 48, 56, 64, 72, and 88. The decoded output is used to accomplish three functions: (1) clock the character counter, (2) assist in clocking the line counter, and (3) assist in producing an EOL pulse during character count 80.

4-18.6 Character Counter

The purpose of the character counter is to count the number of characters per line. There are 88 characters on each line, of which 80 represent displayable characters and 8 are horizontal retrace (non-displayable). Horizontal retrace is defined as the amount of time required for the CRT scan to move from the last character position of a line to the first character position of the following line.

The character counter is a divide-by-11 counter which produces two decoded outputs. The character counter is clocked once every eight characters; thus, once a count is decoded, the decode remains active for eight character times. The two decoded outputs are:

a. 10-Count - This decode produces an output from CTS+1 of character count 72 through CTS of character count 80 (see figure 4-21). The decoded output is used to accomplish three functions. It combines with: (1) character count 7 to produce the LWL pulse during character count 79 (2) phase 3, CTS, and seventh character timing outputs to form an EOL pulse during character count 80 (3) character count 8 to clock the line counter during CTS of the 80th character of a line.

b. 11-Count - This decode produces an output from CTS+1 of character count 80 through CTS of character count 88 (see figure 4-21). This decoded output is 104.3 μs wide and corresponds to the horizontal retrace time. During retrace, the 7th character output is combined with this output to produce a Δ (first word of a line) pulse during character count 87 (lines 1 through 13 only).

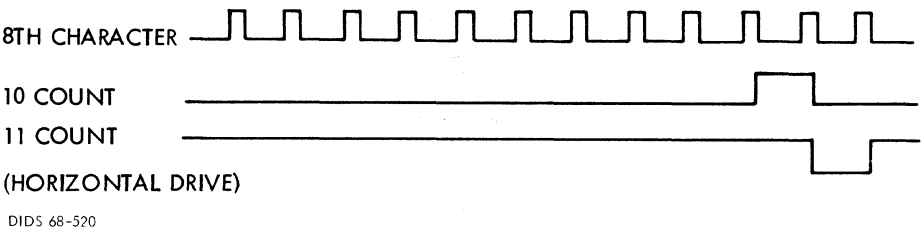


Figure 4-21. Character Counter Outputs

4-18.7 Line Counter

The purpose of the line counter is to count the number of displayable lines on the CRT screen. The line counter is a divide-by-14 counter (13 displayable and 1 retrace) which produces two decoded outputs. These outputs are described as follows:

a. Vertical Drive - This decode is similar to the horizontal drive decode (discussed previously). During the CRT scan period, 13 horizontal lines are displayed before the CRT scan reaches the bottom-right corner of the screen. This downward movement is produced by the vertical drive signal (see paragraph 4-19.1.2). During this entire period, the line counter is counting from line 1 to line 13. When the line counter toggles to line 14, the vertical drive decode is enabled to produce a vertical retrace signal, 80 characters wide. The absence of drive enables the CRT scan to return to the top of the screen to begin another vertical scan.

b. Line 1 - This output is produced when the line counter is toggled by the next 80th character clock pulse. From the previous discussion, eight more characters (horizontal retrace) are counted before display can once again occur. The line 1 decode is enabled during these eight characters and remains enabled until the CTS of the last displayable character of line 1. During this period, an output from the 7th character decode is combined with the line 1 decode output to produce a F(Δ) pulse. This pulse coincides with character count 87 and has a CRT reference point of CTS of the first displayable character of line 1.

4-18.8 1200-Baud Circuitry

The purpose of the 1200-baud circuitry is to count down the CTS bit-counter output to develop 1200-baud pulses for clocking data to and from the interface circuitry. Unlike all other timing circuitry, the 1200-baud counters can be switched on or off by the display terminal logic circuitry on Communications Control Board A12. A level, present when the Display Terminal is about to receive or transmit data, enables CTS pulses to enter the first of two divide-by-eight binary counters.

The CTS input pulses used to clock the counter are present once every 13 μs or at a frequency of 76.8 kHz. These pulses are applied to the first binary counter, which performs a divide-by-eight operation.

The 9.6-kHz output pulses are applied to the second binary counter and a second divide-by-eight operation occurs, thus producing the required 1200-baud pulses. The 1200-baud output is assigned the designation of phase A (ØA) and is used to gate serial data into buffer register D1 (receive) or out of D3 (transmit).

The same ØA pulses are also used as a clock for toggling the 10-bit decimal counter. This counter is described below.

4-18.9 10-Bit Decimal Counter

The purpose of the 10-bit decimal counter is to perform a divide-by-10 operation to develop start, stop, and parity bits for each transmitted character. These decoded outputs are also used during receive to determine the position in time of specific bits of received characters. For example, the $\overline{PAR}$ decoded output is used to determine that the start bit and all seven data bits have been received. The parity check and generation circuitry is then enabled and examined to determine whether the character received had the correct parity.

4-18.10 12-Hz Oscillator

The 12-Hz oscillator is a free running multivibrator that produces decoded outputs of 6 Hz and 12 Hz. The 6-Hz output is used as a cycle frequency for cycling various operations performed by display terminal operators (CYCLE key depressed). The 12-Hz output is used to repeat the step right (→) or step left (←) function when these keys are depressed to their second detent position.

4-19 RASTER GENERATION

The circuits responsible for generating the raster are shown in figure 4-22. The raster is produced by exciting the CRT screen phosphor material with an electron beam. This occurs only during specific periods of time and results in the formation of 13 lines capable of containing up to 80 displayable characters each.

The electron beam used for forming the raster is developed by placing a high potential on the CRT anode element and a relatively low potential on the CRT cathode element. The high difference in potential causes electrons to leave the cathode and bombard the screen phosphor material. When the phosphor is thus exited, light is emitted to produce a visible effect. With no deflection, this light (or raster) would appear in the center of the screen as a small dot and would be useless. To produce a usable raster, the electron beam is moved about the screen by inducing deflection voltages into the yoke assembly on the CRT neck. Since the yoke is placed between the cathode and anode elements, the beam is deflected electromagnetically before it strikes the screen. By certain combinations of varying horizontal and vertical deflection voltages, the beam is swept across the screen from left to right and downwards from top to bottom.

The deflection voltages applied to the deflection yoke are developed by circuits on Vertical and Horizontal Deflection Amplifier Assembly A2 and Monoscope Deflection Amplifier Assembly A3. The operation of these circuits is described in the following text.

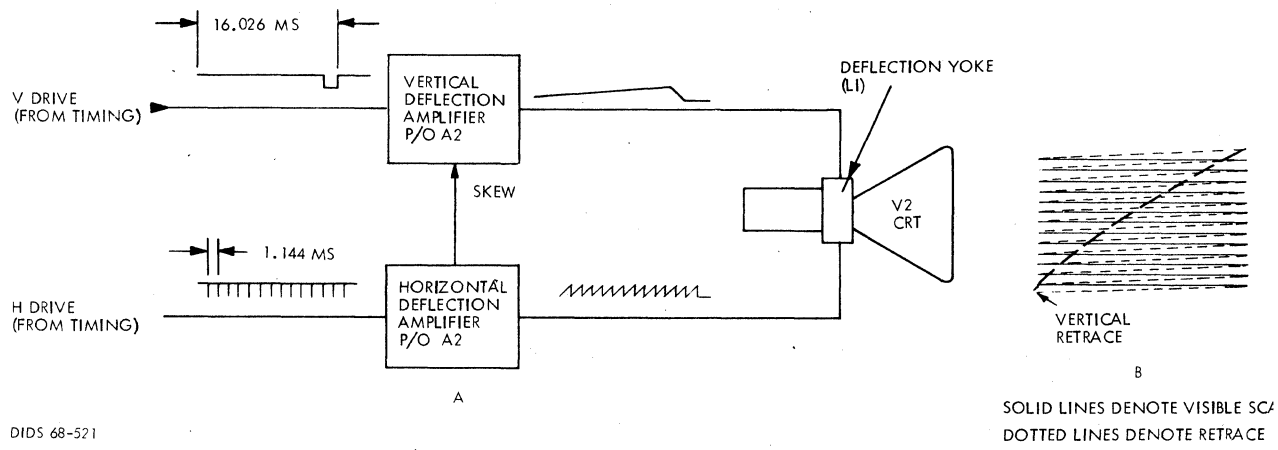


Figure 4-22. Vertical and Horizontal Deflection Amplifier, Block Diagram

4-19.1 Vertical and Horizontal Amplifier Assembly A2

The purpose of this assembly is to develop skew-corrected vertical and horizontal deflection voltages for displaying 13 horizontal lines on the CRT screen. The circuits are interconnected and operate in conjunction to produce the desired visible effect. For example, if the vertical deflection amplifier was inoperative, only one intense horizontal line would be displayed across the center of the CRT screen. Conversely, if the horizontal deflection voltages were absent, an intense horizontal line would be displayed vertically at the center of the screen.

4-19.1.1 Horizontal Deflection Amplifier

The horizontal deflection amplifier (figure 4-22) receives a horizontal drive pulse from the character counter of the timing circuitry. This pulse, which is active for 80 character times and inactive for 8 character times, is converted to a sawtooth waveform by a waveshaping network in the amplifier. During the active line time, the sawtooth gradually increases in value and moves the electron beam across the screen (from left to right). At the end of 80 character times, the sawtooth rapidly collapses when the horizontal character retrace portion of the pulse occurs. This collapse allows the electron beam to return to the original position on the left side of the screen. However, since a vertical force was also exerted on the beam as it swept across the screen, the beam begins its second horizontal excursion one line below the previous line. The CRT protect circuit is enabled during retrace and effectively grounds the CRT control grid. This halts CRT conduction during retrace and thus provides some measure of protection for the CRT phosphor material.

4-19.1.2 Vertical Deflection Amplifier

The vertical deflection amplifier (figure 4-22) receives a vertical drive pulse from the line counter of the timing circuitry. This pulse, which is active for 13 line times and inactive for 1 line time (retrace), is converted to a sawtooth waveform by a waveforming network in the amplifier. During the active scan time, the vertical sawtooth gradually increases in value to move the electron beam from the top to the bottom of the screen. Simultaneously, the horizontal deflection voltage is causing the electron beam to produce 13 visible lines on the CRT screen. At the end of 13 line times, the vertical sawtooth rapidly collapses which allows the electron beam to return to the top of the screen. Simultaneously, the 13th line horizontal retrace pulse is returning the beam to the left side of the screen. Thus, at the end of 14 line times, the electron beam is again positioned at the top left corner of the screen (line one, character one) and a second 13-line scan is initiated.

In addition to the vertical drive pulse, the vertical amplifier receives a second input from the horizontal amplifier. A sampling of the horizontal deflection voltage is applied to the vertical amplifier and acts as a skew correction signal. As the beam scans across the screen, the increasing value of skew-voltage 'bucks' the vertical drive sawtooth and produces a constant vertical deflection current throughout the duration of the line. In this manner, the horizontal sweep remains perfectly horizontal and no 'sagging' is experienced as the horizontal scan approaches the end of the screen.

Similar to the horizontal circuitry, the CRT grid is effectively grounded when the vertical sawtooth collapses. This provides CRT protection during vertical retrace by cutting off the CRT for 80 character times.

4-19.1.3 Minor Vertical Expansion Signal

The minor vertical amplifier contained on monoscope deflection amplifier A3 produces an amplified 1.3-MHz sine-wave signal. This signal is applied to the diddle coil which is located on the neck of the CRT. The purpose of the minor vertical expansion signal is to 'expand' the height of the horizontal scan lines. The minor vertical expansion voltage is frequency-interlaced so that during alternate CRT scans the sine wave signal will be 180 degrees out of phase. This interlacing produces a sharply defined character height as shown in figure 4-23.

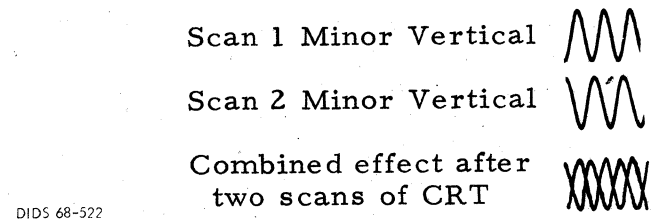


Figure 4-23. Effect of Minor Vertical Expansion on CRT Scan Lines

4-20 POWER SUPPLIES

The display terminal power supply circuitry is shown in figure 4-12. Both power supply assemblies employ solid-state components to furnish regulated dc output voltages. The low-voltage power supply also produces two 6.3-vac outputs which are not regulated.

4-20.1 Low-Voltage Power Supply A4

The low-voltage power supply is used to develop the following output voltages:

a. +5 VDC - This voltage is used internally to operate integrated circuits on digital boards A12, A13, and A14 and operational and transistorized amplifiers on analog boards A3 and A9.

b. -22 VDC and +22 VDC - These voltages are used to operate power transistors in the interface and sweep circuits. In addition, the +22 vdc and -22 vdc outputs are used as a dc source input to high-voltage power supply A5.

c. +100 VDC - The 100 vdc output is used for operating transistors on analog boards A2, A3, A6 and A8.

d. 6 VAC (Isolated) - The isolated ac output is supplied to furnish filament voltage for the monoscope.

e. 6 VAC - The nonisolated ac output is supplied to furnish a filament voltage for the CRT.

4-20.2 High-Voltage Power Supply A5

The high-voltage power supply produces output voltages of +500 vdc, -1.2 kvdc, and +12 kvdc. These voltages are used for the following purposes:

a. +500 VDC - This output is used to furnish acceleration and focusing voltages for the CRT.

b. -1.2 KVDC - This output voltage which is applied to the monoscope filament produces a high difference in potential between cathode and target elements, thus producing the monoscope deflection beam.

c. +12 KVDC - This output voltage is applied to the CRT anode element and produces the CRT electron beam.

SECTION III

CIRCUIT DESCRIPTION

4-21 DESCRIPTION OF SECTION CONTENTS

This section contains detailed circuit explanations of all digital and analog boards contained in the Display Terminal. Wherever possible, information is presented in sequential order taking care not to introduce subjects which have not been previously discussed. In instances where information contained in later explanations is required to understand the immediate text, the necessary information is fully referenced by paragraph and/or figure number.

Logic elements used in the Display Terminal are contained in T^2L integrated circuits. It is a characteristic of these circuits that an open input is always high Thus, if an AND-gate has three inputs and only two of those inputs are connected to external sources, a true logic level at these two inputs will satisfy the gate.

In the circuit explanations, logic elements are referenced by location and output pin number. Thus, A19.6 is located in the 19th integrated-circuit position on board A12 and the output pin of the element is pin 6. To physically locate these elements, refer to the parts layout drawings contained in Chapter 7.

4-22 COMMUNICATIONS CONTROL BOARD A12

The purpose of the communications control board is to control the transfer of digital information between the display terminal internal memory and the CPU. Circuits contained on this board work separately or in conjunction with one another to perform the following major functions:

a. Transmit and Receive Enable - These circuits enable the Display Terminal to enter either the transmit or the receive mode. Mode selection is determined by interpreting locally issued or CPU originated directives or controls.

b. Parity Check and Generation - These circuits check the bit configuration of each character transferred between the CPU and the Display Terminal for the proper parity.

c. Buffer Registers and Decodes - These circuits provide a buffer between the high-speed internal logic and the relatively slow-speed transfer of data to and from the Display Terminal. Decodes connected to the buffer registers enable the interpretation of various digital control codes. The decoded outputs are used to initiate and terminate data transfer and to accomplish edit or cursor control functions.

The following explanations are provided to enable rapid familiarization with these circuits as a basis for further study. The logic diagrams which accompany the text are simplified versions of the master drawings contained in Chapter 7 of this manual. Should further visual aids be required, refer to the complete logic diagram for Communications Control Board A12 (Raytheon Drawing No. 425116) in Chapter 7.

4-22.1 Transmit Enable

The Display Terminal is a half-duplex device designed to both transmit and receive digital information. Depending upon system requirements, control over data transfers can be vested in either the CPU (by means of the program) or the display terminal operator. The following text explains the operation of the transmit and receive enable circuits when either the enquiry-response or polling conversational modes are employed. In addition, other options which significantly change display terminal operation are described on a 'used-not used' comparative basis.

4-22.1.1 Enquiry Response

The enquiry-response conversational mode is employed in systems where the display terminal operator is generally responsible for initiating data transfers. After a message has been initiated by the display terminal operator (enquiry), all further entries on the keyboard are 'locked-out' until a CPU response is received. The CPU may also issue unsolicited responses to the Display Terminal, since a constant receive condition exists at times when the transmission circuits are not enabled.

To transmit an enquiry, the operator types in the desired text and terminates the message by depressing the END key. This inserts an ETX code into the delay-line memory and the code circulates as the last character of the message.

Figure 4-24 is a logic diagram of the circuits on the Communications Control board that enable a transmit operation. In the circuit quiescent state, all the control flip-flops are reset and a high is present at the output of AND-gate A54.8. This output, designated as R, is the level that allows data reception when the Display Terminal is not actively transmitting.

In enquiry-response systems where a modem or similar device is employed, the sequence of events is:

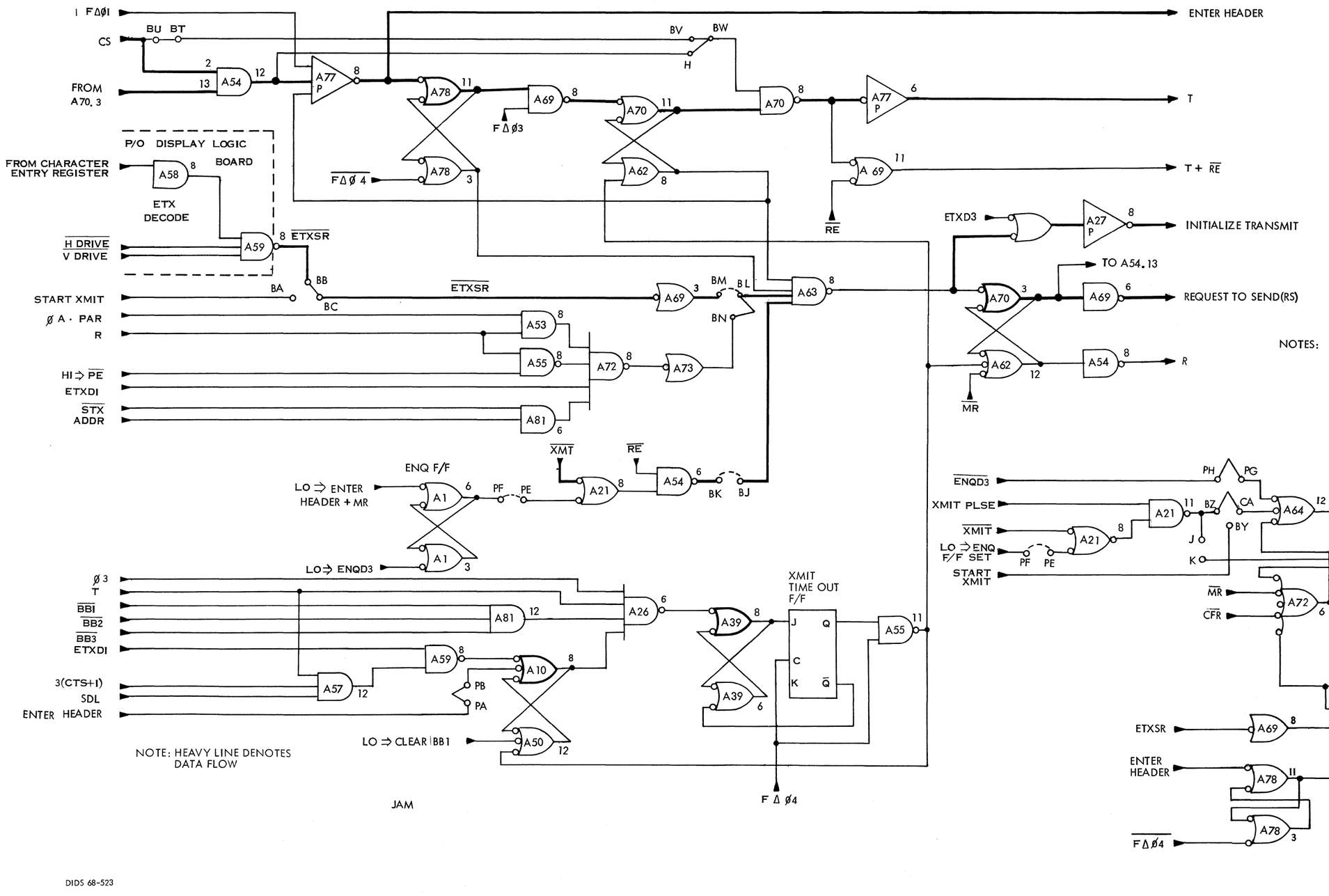
a. Locate ETX code in delay-line memory (ETXSR)

b. Set the request-to-send flip-flop, disable receive logic, and clear buffer registers D2 and D3

c. Receive the clear-to-send control level

d. Enter header characters STX and DA

e. Enable transmit steering logic



LEGEND

ADDR	ADDRESS FLIP-FLOP SET
$\overline{BB1}$	BUSY BIT 1 'NOT'
$\overline{BB2}$	BUSY BIT 2 'NOT'
$\overline{BB3}$	BUSY BIT 3 'NOT'
CS	CLEAR TO SEND
MR	MASTER RESET
PAR	PARITY BIT TIME (bg)
$\overline{PE}$	PARITY ERROR 'NOT'
$\overline{RE}$	RECEIVE ENABLE 'NOT'
RS	REQUEST TO SEND
R	RECEIVE STEERING LEVEL
$\overline{STX}$	START OF TEXT FLIP-FLOP RESET
SDL	SHIFT DATA TO/FROM DELAY LINE
T	TRANSMIT STEERING LEVEL
$\overline{XMT}$	TRANSMIT KEY DEPRESSED

NOTES:
1. ENQUIRY-RESPONSE OPTIONS
2. POLLING OPTIONS
3. COMMON TO ENQUIRY-RESPONSE AND POLLING
4. HEAVY LINES DENOTE MAJOR FUNCTION PATHS
5. BY TOCA IS OPTIONAL CONNECTION FOR ONE-STEP TRANSMIT IN THE POLLING MODE

Figure 4-24. Transmit Enable Circuitry

f. Transfer contents of the delay line to buffer registers and from buffer register D3 to the interface circuits

g. When ETX is detected in buffer register D1, begin transmit time-out sequence

h. When all buffer registers are empty, terminate transmit mode and enter receive mode

The ETX code (entered into delay-line memory by the operator) circulates through the refresh-memory loop. Once per frame this character appears in the character entry register and is decoded by NAND-gate A58.8 on the Display Logic Board. An output pulse, $\overline{\text{ETXSR}}$, is developed by NAND-gate A59.8 as soon as the character appears in the register. On the Communications Control Board, ETXSR is applied to NAND-gate A63.8 in coincidence with the reset outputs of A78.3 and A62.8. When the XMIT key is depressed, the fourth input is satisfied and an output is produced. This low output is used to accomplish three functions: (1) raise the request-to-send line, (2) clear the buffer registers (Initialize Transmit), and (3) disable the receive (R) steering logic.

The request-to-send (RS) control level is amplified by interface circuits on the timing and discrete board and coupled to a modem or similar device. After an established delay, a clear-to-send (CS) control signal is generated in reply and applied to the input of AND-gate A54.12.

The output of A54.12 is applied to inverter-driver A77.8 in coincidence with the reset output of flip-flop A62.8. The next F$\Delta\emptyset$1 is gated through the inverter as Enter Header. This pulse jams an STX character into buffer register D3 and a predetermined address character into buffer register D2.

The Enter Header pulse also sets flip-flop A78.11; the set output of the flip-flop is applied in coincidence with F$\Delta\emptyset$3 to enable NAND-gate A69.8. The lowgoing output sets flip-flop A70.11 to enable one input of NAND-gate A70.8. One phase time after A70.11 is set (F$\Delta\emptyset$3$\rightarrow$F$\Delta\emptyset$4), flip-flop A78.11 is reset by an F$\Delta\emptyset$4 pulse.

The output of NAND-gate A70.8 is used to produce the transmit (T) steering logic level. Again, because of optional wiring, the other inputs to A70.8 may be enabled only by clear-to-send, or clear-to-send and request-to-send appearing in coincidence. In any case, the output of A70.8 is inverted and used through the buffer register steering logic as a transmit steering level. As shown in figure 4-24, T and request-to-send remain high until the transmit time-out flip-flop is set. This circuit is described in the following text.

The purpose of the transmit time-out flip-flop is to reset the transmit and receive enable circuitry to the receive (R) function. Once the transmit steering logic is enabled, data is extracted from the delay line each time the cursor bit is located. If at least one of the buffer registers is empty, the character code is extracted from memory, shifted from D1 through D3, and out to the interface circuitry (see figure 4-24).

While data is being entered or extracted from memory, a special flip-flop in the steering logic, shift delay line (SDL), is enabled. Thus during the transmit mode, all three inputs to AND-gate A57.12 are satisfied during 3(CTS+1) each time SDL is enabled. The output of this gate (which consists of a pulse in coincidence with each extracted character) is applied to one input of NAND-gate A59.8. When the last character of the message (ETX) is shifted into buffer register D1, A59.8 is enabled to set flip-flop A10.8. The flip-flop, once set, enables one of the inputs to NAND-gate A26.6. When the ETX code detected in D1 is finally shifted out of the last buffer register, all three registers are empty. This empty condition is sensed by 'busy-bit' flip-flops BB1, BB2, and BB3 on the Communications Control Board and the 'not full' levels enable AND-gate A81.12. Since T is still high, the next phase 3 timing pulse is gated through NAND-gate A26.6 to set flip-flop A39.8. On the next F$\Delta\emptyset$4 pulse, the transmit time-out flip-flop is set and, simultaneously, A39.6 is reset to remove the input. On the rising edge of the next F$\Delta\emptyset$4 pulse (16 ms later), NAND-gate A55.11 is enabled and a transmit time-out pulse is generated. This pulse is used to reset flip-flops A62.8, A62.12, and A50.12, and thus disable the T steering logic and the request-to-send line. Simultaneously, since the output at A62.12 is high, the R steering logic is now enabled.

On the trailing edge of the F$\Delta\emptyset$4 pulse that enabled NAND-gate A55.11, the transmit time-out flip-flop is reset and the transmit-receive enable circuitry returns to its quiescent state.

4-22.1.2 Polling

In the polling conversational mode, both sections of the transmit and receive enable circuitry work closely in conjunction, since the Display Terminal must receive a polling read directive before it can transmit the message contained in the delay line.

The operator types in the message in the usual fashion and then sequentially depresses the END and XMIT keys. As stated previously, depressing the END key places an ETX character code into memory where it is constantly circulated (see figure 4-24).

When the operator depresses the XMIT key, the resulting keyboard output level is combined with a sample strobe (XMIT PLSE) to enable NAND-gate A21.11. The output of A21.11 sets flip-flop A64.12 which, in turn, sets flip-flop A73.6. This enables one input to NAND-gate A64.8, and the transmit enable circuitry idles until a polling command is received from the CPU.

The Display Terminal rests in the receive state (R=high) to allow receipt of the polling message. Note that either a read or a write directive can be issued by the CPU. If a read directive is issued, the Display Terminal enters the transmit mode and transfers the message stored in the delay line to the CPU. On the other hand, the CPU may issue a write directive, since it has no way of knowing that the operator has a message available for transfer. If this occurs, the Display Terminal enters the receive mode and the stored message is partially or completely destroyed, depending upon the length of the received message.

When an STX character is received from the CPU, the STX flip-flop is set. If the next character received is the correct DA, the ADDR flip-flop is set. If the address character has a '1' in the MSB position, the STX flip-flop is reset to produce conditions ADDR and $\overline{\text{STX}}$. These outputs are coupled to AND-gate A81.6 to enable one input of NAND-gate A72.8. The remaining inputs to A72.8 are satisfied during the next character time when ETX is shifted into D1. The ETX decode is enabled and $\overline{\text{ETXD1}}$ resets the STX and ADDR flip-flops while ETXD1 is used to enable the second input to A72.8. If ETX is received without a parity error, the remaining inputs of A72.8 are enabled during the ETX character parity count. The output of A72.8 is inverted and combined with the reset outputs of A78.3 and A62.8 to enable NAND-gate A63.8.

The output of A63.8 disables the R steering logic and raises the request-to-send line; and Initialize Transmit clears buffer registers D2 and D3. When the CS reply is returned from the modem or CPU, AND-gate A54.12 is enabled and, on the next FΔØ1 pulse, Enter Header jams STX into D3, DA into D2, and ETX into D1, and enables the second input to A64.8. Approximately 16 ms later, FΔØ3 sets flip-flop A70.11 to enable the T steering logic.

At this point, the delay-line memory is examined to determine whether an ETX code has been inserted by the operator. Keep in mind that presently STX is in D3, DA is in D2 and ETX is in D1. If within 16 ms an ETX is not found in the delay line (indicating that the operator has no message available), the next FΔØ4 resets flip-flop A78.3 and disables the input to A64.8. This prevents destruction of the ETX code in D1 and the 'no-business' response is transmitted to the CPU. When Enter Header jammed the STX, DA, and ETX character into the buffer registers, flip-flop A10.8 was also set. When the last character of the 'no-business' response is transmitted, the transmit time-out flip-flop is set to enable a return of the receive mode.

If an ETX code is found in memory, a message available condition is indicated. When the ETX character is shifted into the character entry register the $\overline{\text{ETXSR}}$ output pulse is inverted and enables the third input of NAND-gate A64.8. The output of A64.8 clears BB1 (the busy bit for buffer register D1) thus allowing the first text character from memory to be shifted into the register 'on top of' the ETX character received from the CPU. In addition, the output pulse is applied to cross-connected flip-flop gates A73.6, A50.12, and A72.6 to prevent a recurrence of CLEAR BB1 the next time the ETX code appears in the character entry register.

The transfer of data from memory continues until the ETX character is shifted into buffer register D1. The ETXD1 decoded output enables NAND-gate A59.8 to set flip-flop A10.8. When ETX is finally shifted out of buffer register D3, gate A81.12 enables NAND-gate A26.6 and the transmit time-out function is initiated.

4-22.1.3 Optional Operation

4-22.1.3.1 Request-to-Send and Clear-to-Send

In some systems, the Display Terminal is connected directly to the CPU, and the RS and CS lines and the attendent time delay is not required. As already stated, it is not necessary for T^2L integrated circuits to have every input connected

in order to be satisfied. If a connection is left open by not connecting certain wiring, the associated gate input is enabled at all times by a high at the open input. As shown in figure 4-24, when the RS and CS options are not employed, flip-flop A70.3 has the sole function of switching the R steering logic to an 'off' condition. In addition, the AND function of gates A54.12 and A70.8 are effectively eliminated from the transmit enable circuitry. Other than eliminating the time delay between the request and clear-once-to-send, the elimination of the RS and CS circuits has no effect on the operation of the transmit enable circuitry.

4-22.1.3.2 One-Step Transmit

When the one-step transmit option is employed, the transmit enable circuits are activated by depressing only the END key. When END is depressed, an ETX code is inserted into delay-line memory and the cursor is automatically line or frame reset. A pulse, START XMIT, initiates the transmit operation in essentially the same manner as depression of the XMIT key.

The option takes one of two forms depending upon still another option. In one form, the cursor is frame reset before transmission is initiated. When this form is employed, up to 1040 characters may be transmitted depending upon the location of the ETX code in memory. In the second form, the cursor is line reset before transmission and up to 80 characters may be transmitted. Again, the number of transmitted characters depends upon where ETX was inserted on the line. Each form is described separately to assist in understanding the particular type of option employed at the user installation.

The first form of one-step transmit is accomplished by connecting a wire between terminals D and E on the display logic board (see figure 4-25). When the END key is depressed, an ETX code is inserted into the character entry register. This ETX is decoded by NAND-gate A58.8 and during 3CTS a pulse is developed at A17.11. This pulse jams the cursor reset flip-flop and a cursor reset function is initiated (see paragraph 4-23.3.5). On the next FΔ (one frame time later), NAND-gate A39.6 is enabled and START XMIT pulse is produced. As shown in figure 4-24, this pulse initiates the transmit operation through terminals BY-CA (polling) and BA-BC (enquiry-response).

In the second form of one-step transmit, a wire is connected from terminal D to F on the display logic board. In this form, depressing the END key causes the cursor to be line reset and transmission to be initiated from that point. The cursor is moved to the first character of the line position by sequentially initiating the step-up and advance-line cursor control operations (see paragraphs 4-23.3.9b and 4-23.3.4, respectively).

The pulse present at A17.11 is coupled to the clock input of one-step flip-flop A25.9 and to the jam-set input of step-up flip-flop A14.6. When A14.6 goes high, the step-up cursor control operation is initiated. After the cursor has been moved to the character position on the previous line corresponding to the position of ETX on the original line, Step Up Complete resets the step-up flip-flop. This places a high at A14.5 which enables one input to NAND-gate A1.6. The remaining inputs are satisfied during 4CTS+1, and the output of A1.6 is employed to jam reset flip-flop A41.6 which initiates the advance line function. After the cursor has been advanced to the first character position of the line containing the ETX code, NAND-gate A11.11 is enabled to produce the START XMIT pulse.

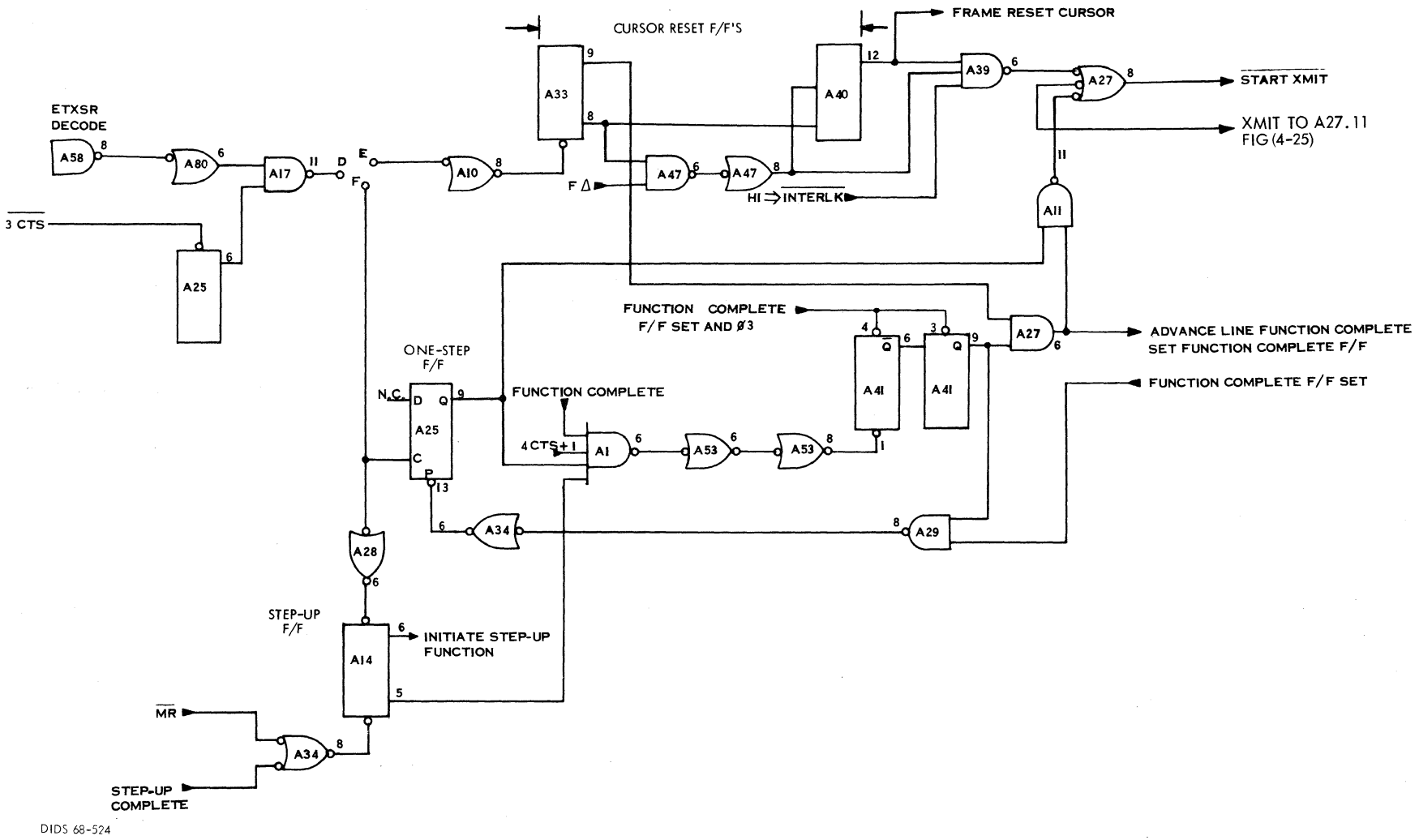


Figure 4-25. One-Step Transmit Option, Logic Diagram

code, NAND-gate A11.11 is enabled to produce the $\overline{\text{START XMIT}}$ pulse. This This initiates transmission beginning at the cursor position (first character of the line) and terminating at the ETX position (up to 80 characters later on the same line). The function complete flip-flop then sequentially resets the one-step flip-flop and the advance line flip-flop to return the circuit to its quiescent state.

4-22.1.3.3 Enquiry Option

The enquiry (ENQ) option permits the CPU to initiate transmission from a Display Terminal by simulating the manual depression of the XMIT key. In either the enquiry-response or polling conversational modes, the CPU can insert the ENQ control code into a message directed to a particular Display Terminal. When ENQ is decoded in buffer register D3, a pulse which sets the ENQ flip-flop (enquiry-response) or simulates the depression of XMIT (polling) is generated. In either instance, transmission is initiated only after an ETX code is decoded in the character entry register (ETXSR). If an ETX code has not been inserted into memory, then transmission cannot occur. Thus, ENQ is limited by the same factors that govern local transmission (i.e., depressing XMIT or decoding ENQ before an ETX code has been inserted into memory has no effect on the transmit enable circuits).

The ENQ code is normally preceded in received messages by a cursor reposition code. This code moves the cursor to the position on the screen where the CPU desires to begin transmission. If there is an ETX in memory, transmission starts at the cursor position and ends at the position on the screen where the ETX code was inserted by the operator (see figure 4-24).

In the polling conversational mode, the ENQ option is accomplished by connecting a wire between terminals PG and PH. When the ENQ code is received and decoded in buffer register D3, NAND-gate A24.8 produces a low output. This low is connected to the set input of cross-connected flip-flop A64.12. As shown in figure 4-24, decoding ENQ in D3 ($\overline{\text{ENQD3}}$) has the same effect as depressing the XMIT key. The set output of A64.12 forces A72.6 low which, in turn, sets flip-flop A73.6 to enable one input of NAND-gate A64.8. The circuit then rests in this state until an ETX code is detected in buffer register D1 to indicate the last character of the CPU message.

When ETX is received, a phase A pulse is gated through NAND-gate A63.8 to disable the receive (R) steering logic and produce an Initialize Transmit pulse. Also, when A70.3 is set, inverter driver A77.8 generates an Enter Header pulse to jam STX, DA and ETX into buffer registers D3, D2, and D1, respectively. Enter Header also sets flip-flop A78.11, which enables the second input to NAND-gate A64.8. When ETX is found, the low output at A64.8 clears BB1 and transmission is initiated.

If ETX is not detected in the memory loop, NAND-gate A64.8 is not enabled and transmission does not occur. On the next F(Δ) (frame pulse), a complete scan of memory has been accomplished without finding an ETX code. If an EOT or FF cursor reposition is not in effect, a $\overline{\text{CFR}}$ pulse is developed on the display logic board and flip-flop A72.6 is reset to disable the operation.

In the enquiry-response conversational mode, the ENQ option is employed by connecting a wire between terminals PF and PE. When ENQ is decoded in buffer register D3, a low at the output of NAND-gate A24.8 is used to set ENQ-flip-flop A1.3 to produce a low at A1.6. As shown in figure 4-24, this low simulates depressing XMIT and if an ETX code is found in the memory loop, the receive (R) function is disabled. Transmission then occurs in the usual manner by sequentially entering STX and DA into the buffer registers and then enabling data transfers from the delay line.

4-22.2 Receive-Enable

The display terminal receive enable circuitry is shown in figure 4-26. As stated previously in transmit enable, the receive logic is enabled when the Display Terminal is not actively transmitting. This factor allows data to be shifted into buffer register D1 from the CPU. The received data, however, is not permitted to enter buffer register D2 until STX and DA are received sequentially. These two characters are detected by decodes connected to buffer register D1.

4-22.2.1 Enquiry-Response

In the enquiry-response conversational mode, the Display Terminal may receive either a solicited or an unsolicited response from the CPU. Normally, the Display Terminal is awaiting a response to a previously transmitted enquiry. The STX and ADDR flip-flops are reset by any of the inputs to NOR-gate A63.6.

When the STX character code is received from the CPU, the Display Terminal interprets the code as the beginning of a response. Even though the message may not be intended for use by any particular Display Terminal, all display terminals connected to the CPU respond by entering the receive enable sequence. STX decode A75.8 produces a low output which simultaneously sets STX flip-flop A79.12 and resets ADDR flip-flop A79.9. This enables AND-gate A81.8 and places a high at the inputs to NAND-gates A71.3 and A82.6. With the STX flip-flop set, the circuit idles until the next character is received.

If the next character received is the correct address (either display address or broadcast address), NAND-gate A82.6 is enabled and the resulting output sets ADDR flip-flop A79.9. When both the STX and ADDR flip-flops are set, NAND-gate A78.6 is enabled to develop a receive enable ($\overline{RE}$) output. This output is used to permit all characters following DA to enter buffer registers D2 and D3. From buffer register D3, the characters enter the refresh memory loop at the character entry register and are displayed on the CRT screen. When ETX is decoded in D3, the $\overline{ETXD3}$ output enables one input to NOR-gate A63.6 and the STX and ADDR flip-flops are jammed reset. This removes both inputs from NAND-gate A78.6 and the receive operation is terminated.

If the character following STX is the improper address, NAND-gate A82.6 is not enabled. The high output is coupled to A71.3 and the resulting low is coupled via strapping terminals CG and CF to the reset inputs of the STX and ADDR flip-flops. On the next clock pulse, both flip-flops are reset and the circuit returns to its quiescent state.

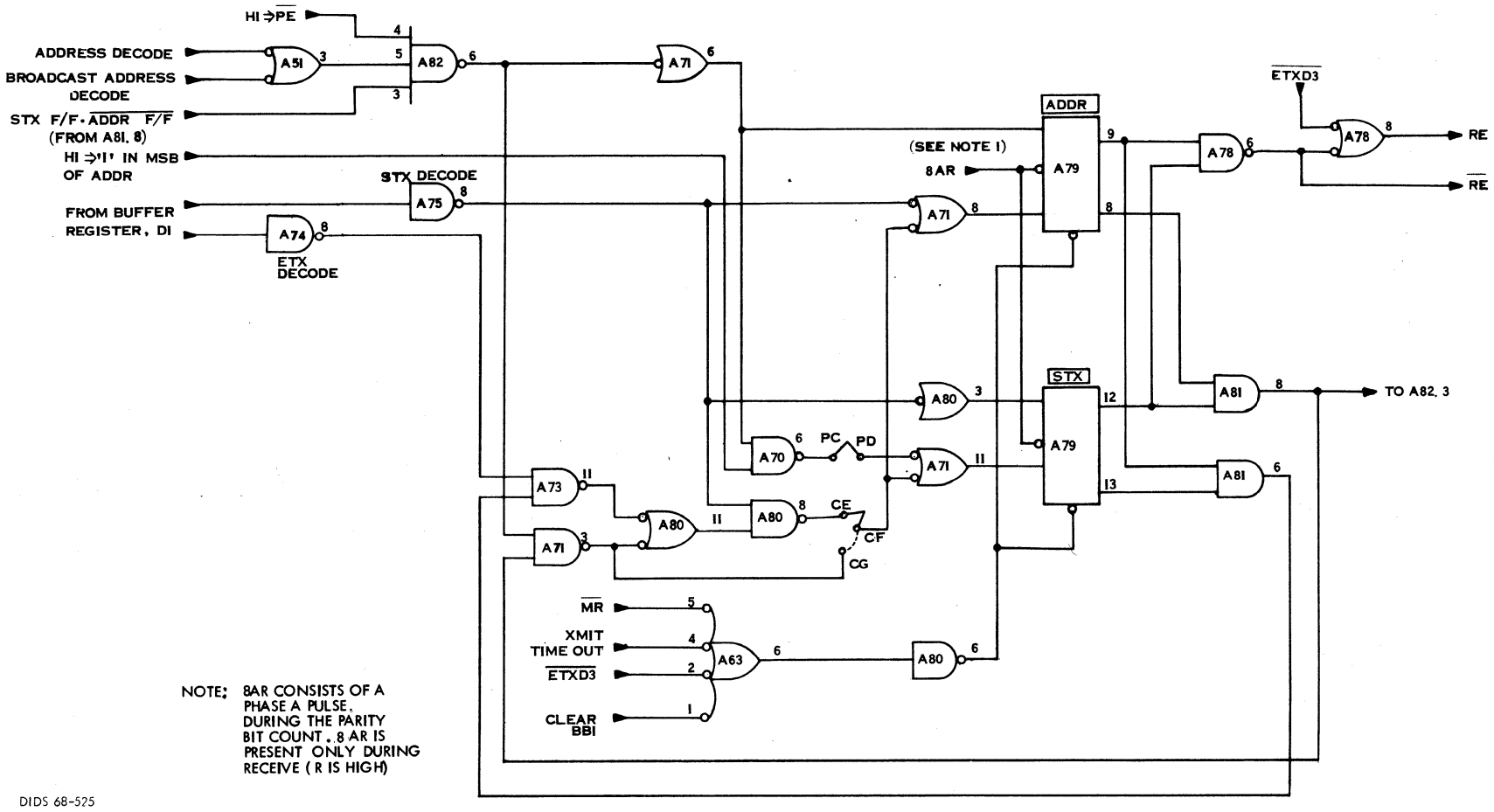


Figure 4-26. Receive Enable Circuitry, Logic Diagram

4-22.2.2 Polling

In the polling conversational mode, the Display Terminal enters the receive mode when characters STX and DA are received sequentially. As stated in Section I, the address code, in addition to selecting the proper Display Terminal, also contains a polling directive in the MSB position. If the MSB of the address character is a '0', the Display Terminal enters the receive mode to prepare to write the incoming message onto the CRT screen. Conversely, if the MSB of the address character is a '1', the Display Terminal enters the transmit mode since a polling read directive is indicated.

In the polling mode, one of three operational sequences is initiated depending upon the address character. These sequences are described in the following text by assuming the conditions listed below:

a. An incorrect address is received

b. A polling write directive is received

c. A polling read directive is received

For each of the following descriptions, it is assumed that an STX character has been received. The reception of STX resulted in setting the STX flip-flop (A79.12) and resetting the ADDR flip-flop (A79.9).

When an incorrect address is received following an STX character, NAND-gate A82.6 is not enabled. The high placed at the second input to NAND-gate A71.3 is coupled through NOR-gate A80.11 to enable NAND-gate A80.8. The output of A80.8 is, in turn, inverted by NOR-gates A71.11 and A71.8 to reset the ADDR and STX flip-flops, respectively. This returns the receive enable circuit to its quiescent state (i.e., $\overline{\text{STXF/F}}$ and $\overline{\text{ADDRF/F}}$).

When the correct address is decoded and a '0' is present in the MSB position, the ADDR flip-flop is set by a high present at A71.6. Since a '0' is present in the MSB position, NAND-gate A70.6 is inhibited from resetting the STX flip-flop. When both the STX and ADDR flip-flops are set, NAND-gate A78.6 is enabled to produce an $\overline{\text{RE}}$ output. This output continues to be present until an ETX character is decoded in buffer register D3. The operation of the receive enable circuit following a polling write directive is identical to the enquiry-response mode, except for the necessity of inhibiting NAND-gate A70.6.

When the correct address is decoded and a '1' is present in the MSB position, a polling read directive is indicated. As stated previously, the Display Terminal responds to a read directive by entering the transmit mode. The '1' in the MSB of the address character enables the second input to NAND-gate A70.6. Thus, when the next phase A clock pulse is received, the ADDR flip-flop is set and the STX flip-flop is reset. This produces an ADDR · $\overline{\text{STX}}$ condition to enable AND-gate A81.6 of the transmit enable circuitry (see figure 4-24).

4-22.3 Parity Check and Generation

The purpose of the parity check and generation circuitry is two-fold. In the receive mode, the bit configuration of each received character is checked for an even number of 1's. If an erroneous character is received, the parity error lamp is illuminated and a parity error SUB code (0011010) is inserted into memory in place of the erroneous character. In the transmit mode, each transmitted character is shifted through the parity check flip-flop and the number of 1's is essentially counted. If after one character time an odd number of 1's has been counted, a parity bit of 1 is generated. Conversely, if an even number of 1's is counted, a parity bit of '0' is generated to maintain even parity (see figure 4-27).

In either the transmit or the receive mode, the parity check flip-flop is jammed reset by the decimal counter $\overline{STT}$ output. This output corresponds to the first bit (b_0) of the 10-bit asynchronous characters used to convey information between the Display Terminal and the CPU.

4-22.3.1 Receive

In the receive mode, serial data is coupled directly from the interface circuits and applied to one input of NAND-gate A48.6. When the decimal counter steps to the count following $\overline{STT}$, the remaining input is satisfied and data is permitted to pass through the gate to the J and K inputs of the parity check flip-flop. The gate remains enabled until the decimal counter reaches the count corresponding to the parity bit ($\overline{PAR}$). In essence, this allows all seven data bits to be 'counted' by the parity check circuitry to determine whether an even number of 1's exists. After seven bit times, the parity check flip-flop may either be set or reset, depending upon the number of 1's in the character. If an odd number of 1's is received, the flip-flop is set; if an even number of 1's is received, the flip-flop is reset. The next bit of the character is then examined to determine whether the received character had the correct number of ones.

The set and reset outputs of the parity check flip-flop are connected to NAND-gates A45.3 and A45.8, respectively. The second input to NAND-gate A45.3 is the inverse of data ($\overline{DATA}$), and if the parity bit is a one, a zero is present at this point, while the input to NAND-gate A45.8 is 'true' data.

If an odd number of 1's (one, three, five or seven) is counted, then to achieve parity, the parity bit must also be a '1'. Assuming that it is, NAND-gate A45.3 is not enabled since $\overline{DATA}$ will be a '0'. Since the received character had the correct parity, no further circuit action is necessary. On the other hand, consider what occurs when an odd number of ones are counted and the parity bit is a '0'. $\overline{DATA}$ will be a '1' and NAND-gate A48.6 is enabled during the next phase A pulse. The low output jams a parity SUB code into buffer register D1 'on top of' the erroneous character. Simultaneously, parity error flip-flop A39.11 is set and the keyboard parity error indicator is illuminated. The indicator remains illuminated until a master reset or Initialize Transmit pulse resets the parity error flip-flop.

When an even number of 1's is counted, the parity bit must be a '0' to provide the correct parity. If it is not a '0', the reset output of the parity error flip-flop and the parity error circuitry is enabled and the previously described circuit action occurs.

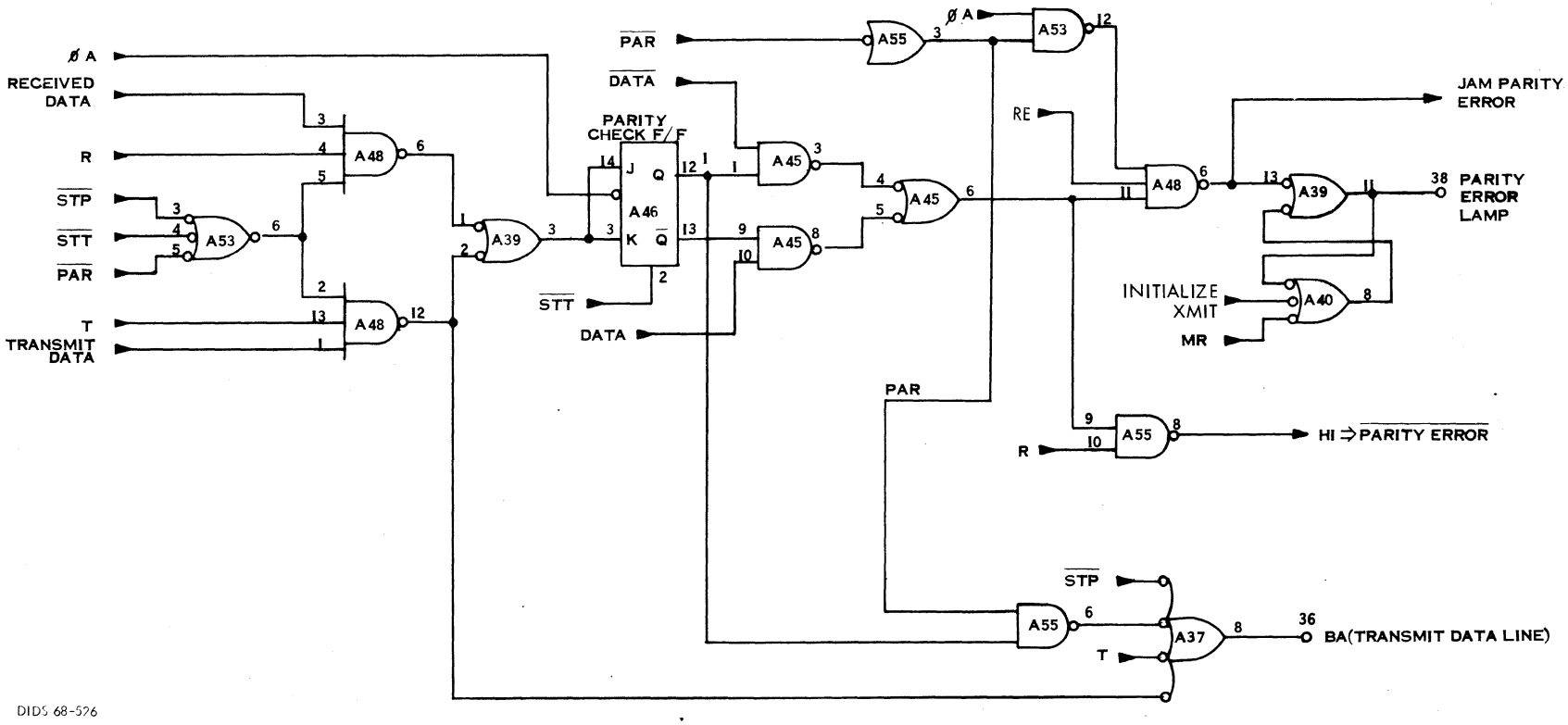


Figure 4-27. Parity Check and Generation, Logic Diagram

4-22.3.2 Transmit

In the transmit mode, the transmitted data line (BA) is held high by the $\overline{STP}$ output of the decimal counter. When the decimal counter is released by ØA gate (or cycles from $\overline{STP}$ to $\overline{STT}$ as it finishes one count and begins another), the start bit (a SPACE) is placed on the transmitted data line. Simultaneously, since the decimal counter is producing an $\overline{STT}$ output, the parity error flip-flop is jammed reset.

On the next count of the decimal counter, a high is produced at the output of A53.6. This high permits the first data bit of the character to pass from buffer register D3 into the parity check flip-flop and on to the transmitted data line. During the next six bit times, the remaining bits of the character are transmitted, while the number of 1's in the character are counted by the parity check flip-flop.

If the transmitted character contains an odd number of 1's after seven bit times the parity check flip-flop is set. During the next bit time, the decimal counter steps to its ninth count ($\overline{PAR}$) and NAND-gate A55.6 is enabled. This places a '1' on the transmitted data line to provide the correct parity.

If the transmitted character contains an even number of 1's after seven bit times the parity check flip-flop is reset. When the decimal counter steps to $\overline{PAR}$, NAND-gate A55.6 is not enabled. This, in turn, places a '0' on the transmitted data line in the parity bit position of the character.

The tenth bit of the transmitted character is produced when the decimal counter steps to the next count. The $\overline{STP}$ output is applied to NOR-gate A37.8 to produce the stop bit (a $\overline{MARK}$).

4-22.4 Buffer Register Control Logic

The purpose of the buffer register control logic is to control the movement of data through buffer registers D1, D2, and D3. The control logic consists of three busy-bit flip-flops (BB1, BB2, and BB3), and three shift control flip-flops [shift gate one-to-two (SG12), shift gate two-to-three (SG23), and shift to and from the delay line (SDL)]. The control logic circuitry is shown in figures 4-28 and 4-29.

4-22.4.1 Busy-Bit Flip-Flops

Each of the three busy-bit flip-flops is associated with a buffer register. The purpose of BB1, BB2, and BB3 is to supply register full or register empty status information for use by the shift control flip-flops. For example, if BB1 is set, a buffer register D1-full status is coupled to the SG12 circuitry to indicate that a character is in D1 and a transfer to D2 can be initiated. Before a transfer can occur, however, a buffer register D2-not full satus must be indicated by BB2. The transfer from D2 to D3 is handled in much the same manner.

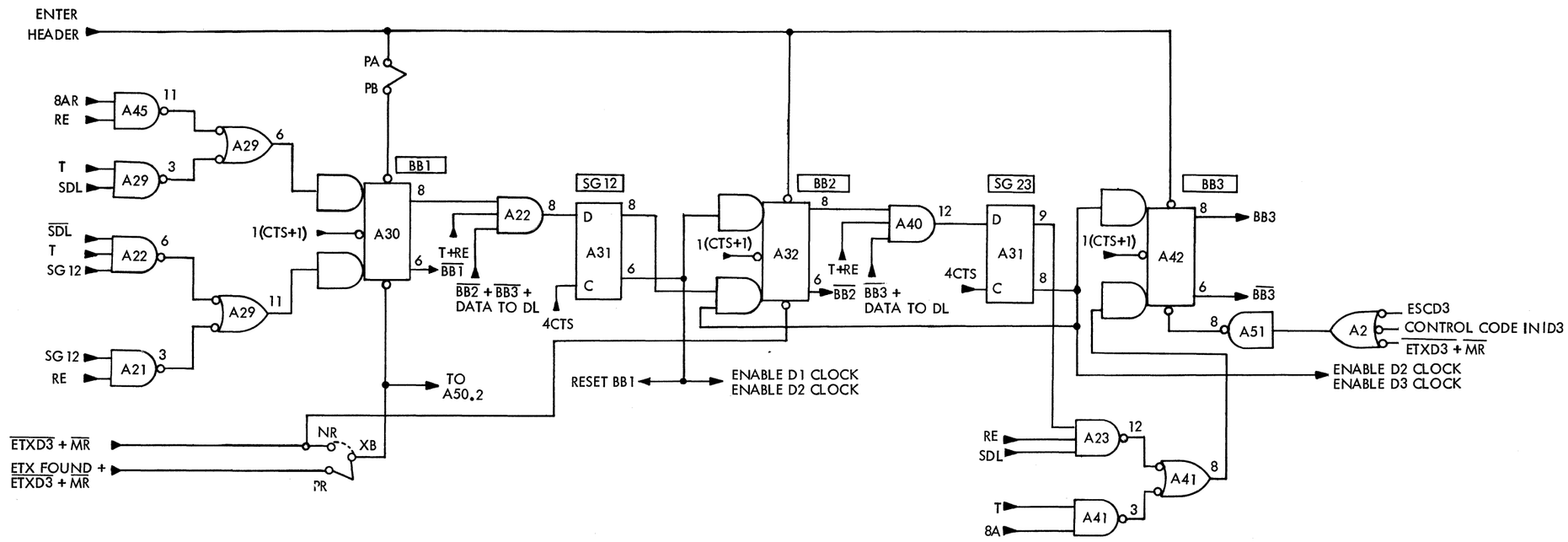


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Figure 4-28. BB1, BB2, BB3, SG12, SG23 and Associated Circuits, Logic Diagram

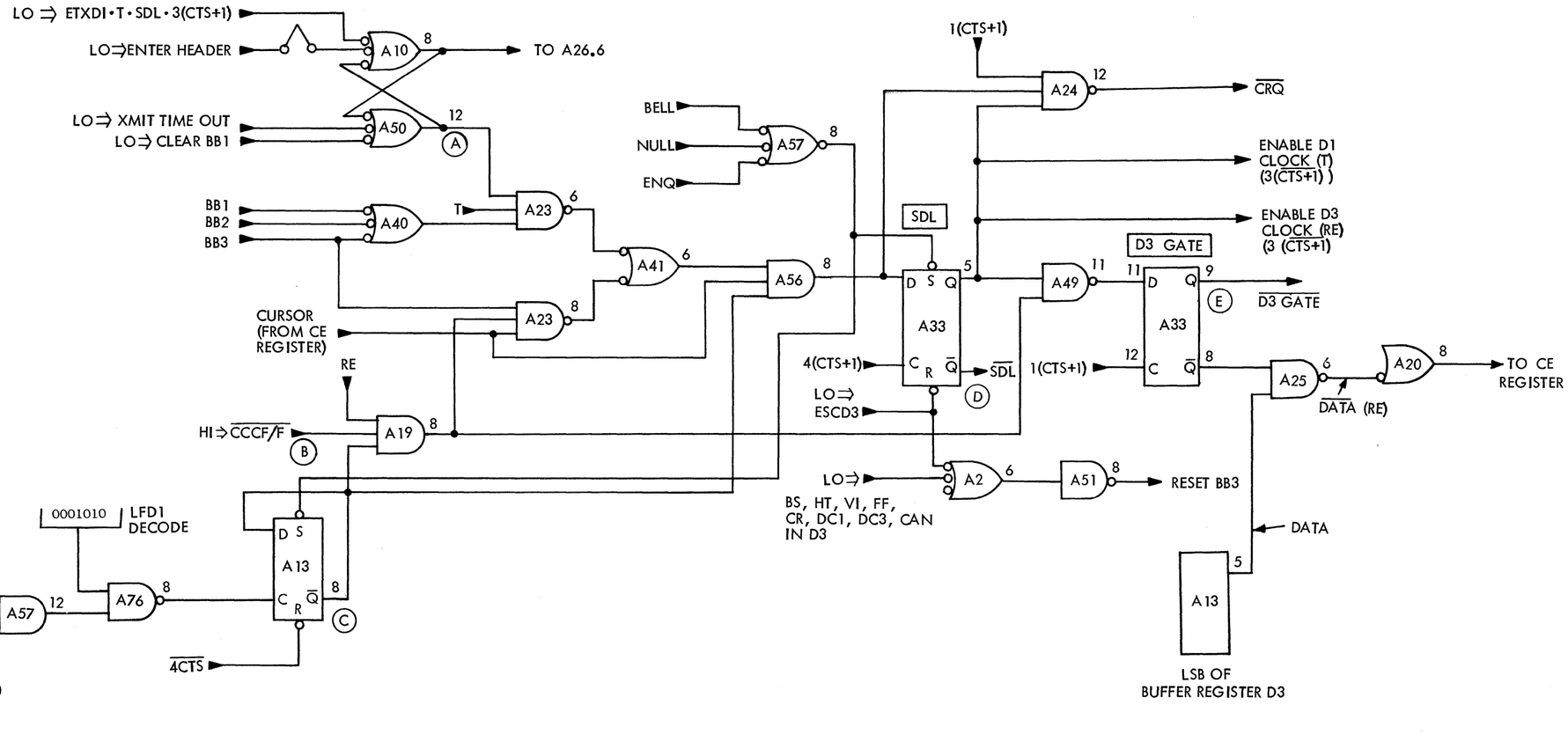

Figure 4-29. SDL, D3 Gate and Associated Circuits, Logic Diagram

4-22.4.1.1 Busy-Bit One

Busy-bit one (BB1) is a J-K type flip-flop used to indicate a full or not full condition for buffer register D1 (see figure 4-28). The normal condition of BB1 is reset due to a low applied to the clear input following a transmit or receive sequence (ETXD3).

In the polling conversational mode, strapping terminals PA and PB are connected to provide a means for setting BB1 when Enter Header jams an ETX character into buffer register D1. As previously stated, ETX remains in D1 until an ETX code is detected in memory. When, or if, an ETX is located in memory, BB1 is cleared by ETX Found. This permits the first message character to be shifted into D1 'on-top-of' the ETX code.

BB1 may also be set by input levels applied through NOR-gate A29.6. In the receive mode, BB1 is set by 8AR and RE occurring in coincidence. 8AR is one phase A pulse which occurs during the parity bit of each character received after STX and DA. In the transmit mode, BB1 is set when the cursor is found in memory. The cursor sets SDL (see paragraph 4-22.4.2.3) which, in turn, enables a character to be shifted out of memory and into buffer register D1.

BB1 is reset when SG12 transfers the character from D1 to D2. Note that in the transmit mode, BB1 is reset when SDL goes low. This occurs momentarily while the CRQ pulse is stepping the cursor to the right one character position.

4-22.4.1.2 Busy-Bit Two

Busy-bit two (BB2) is used to indicate a full or not-full condition for buffer register D2. BB2 is reset following a transmit or receive sequence by $\overline{\text{ETXD3}}$ and remains reset until SG12 enables a character transfer from D1 to D2. When the proper conditions exist to allow a transfer from D2 to D3, a level from SG23 is combined with a $\overline{\text{SG12}}$ level to reset the busy bit. In terms of data transfer, the character held in D2 is transferred to D3, and D1 does not contain a character for transfer to D2. Thus, BB2 is reset because D2 is empty after the transfer occurs. Note,however, that a simultaneous transfer can occur from D2 to D3 and from D1 to D2 if buffer register D1 contains a character.

4-22.4.1.3 Busy-Bit Three

Busy bit three (BB3) flip-flop provides a full or not full status indication of buffer register D3. Like the previously described busy bits, BB3 is reset when an ETX character is decoded in D3. A level from SG23 sets BB3 when a character is transferred from D2 to D3. In the receive mode, BB3 is reset when SDL and RE appear in coincidence with $\overline{\text{SG23}}$. This indicates that the character in D3 has been shifted into the delay line (SDL), but has not yet been replaced by a character from D2. In the transmit mode, BB3 is reset by a phase A pulse which occurs during the parity bit of the character. This indicates that the last bit of the character has left the register and has entered the transmitted data interface circuit.

4-22.4.2 Shift Gates

There are three shift-gate flip-flops directly associated with the transfer of data through the buffer registers and to/from the delay-line memory. SG12 and SG23 are used to enable clock pulses to shift serial data through buffer registers D1, D2, and D3. SDL is used in both the transmit and receive mode to enable clock pulses to D1 and D3. A fourth flip-flop, D3 GATE, is employed to enable data transfers to the delay line during receive and to inhibit transfers to the delay line during transmit.

4-22.4.2.1 Shift Gate One-to-Two (SG12)

SG12 has the sole function of enabling the application of clock pulses to buffer registers D1 and D2. SG12 is enabled when any of the following conditions exist:

a. Buffer register D1 is full and D2 is empty

b. Buffer register D1 is full and D3 is empty

c. Buffer register D1 is full and D3 is full, but the character in D3 is about to be shifted into the delay line

In either the transmit or the receive mode, when D1 contains a character the remaining registers are examined for an empty status. Note that the condition D2-full and D3-empty results in a simultaneous transfer from D2 to D3 and from D1 to D2. This is what occurs under the condition specified in paragraph 4-22.4.2.2b. The condition stated in (c) will have the same effect since the character in D3 will enter the delay line at the same time the character contained in D2 is shifted into D3.

4-22.4.2.2 Shift Gate Two-to-Three (SG23)

SG23 enables the application of clock pulses to buffer registers D2 and D3 when the following conditions exist:

a. Buffer register D2 is full and D3 is empty

b. Buffer register D2 is full and D3 is full, but the character contained in D3 is about to be shifted into the delay line.

In either the transmit or the receive mode, the condition D2 full enables SG23 when D3 is empty. If the D3 register is empty, as soon as the initial bits of a character are shifted into D2, BB2 goes high to enable a straight-through transfer to D3. The character, in effect, does not stop since both registers are clocked simultaneously. If the D3 register is full, however, SDL must be enabled before the character held in D2 can be transferred. The combination $\overline{SG23}$, RE, and SDL enables NAND-gate A23.12 to reset BB3 to produce $\overline{BB3}$ output. This level is then coupled to NAND-gate A40.12 to enable SG23.

4-22.4.2.3 Shift (to/from) Delay Line (SDL)

The SDL circuitry is shown in figure 4-29. The purpose of the SDL flip-flop is to control the flow of data between the buffer registers and the delay line.

In the transmit mode, SDL is employed to enable clock pulses to D1 and thereby shift data into the register from the delay line. During this process, a cursor right request (CRQ) pulse is developed to automatically step the cursor one position to the right. This permits the sequential extraction of one or more characters each time the memory is accessed (provided, of course, that there is room for the second character in the buffer registers).

In the receive mode, SDL is employed to enable clock pulses to D3. Once SDL is enabled, D3 GATE permits data from D3 to enter the memory via the character entry register. A CRQ pulse is also developed in the receive mode sequence. This pulse enables the entry of the next message character if a character is in D3 and available for transfer.

In addition to enabling data transfers to and from the delay line, SDL is also employed to inhibit transfers under special conditions. When control codes are received as part of a message, SDL determines whether or not the control code is entered into the delay line.

Because of the many different operating modes of SDL, the following text contains separate descriptions of each mode. These modes are categorized and described as follows:

a. Receive Mode

(1) Text characters (such as letters, numerals and symbols)

(2) Control characters when preceded by ESC

(3) Control characters not preceded by ESC

(4) Control characters DEL, ENQ, and NULL

b. Transmit Mode

(1) Text characters

In the SDL circuit quiescent state, a high is present at points A, B, C, D, and E. The circuit remains in this state until either RE or T goes high to signify the beginning of a receive or transmit sequence.

4-22.4.2.3.1 Receive Mode - Text Characters. When the STX and DA message header characters are received from the CPU, RE goes high to indicate the presence of an incoming message. This enables AND-gate A19.8 and places a high at one input of gates A23.8 and A49.11. A19.8 remains enabled until RE is disabled or the CCC flip-flop is set by the reception of a control code (see paragraph 4-22.4.4). The circuit idles in this state until the character following DA is shifted into buffer register D3 and BB3 is set. The cursor, which is constantly circulating through the character entry register, is located

from 0 to 16 ms later to enable NAND-gate A23.8 and AND-gate A56.8. On the following 4(CTS+1), SDL is set to simultaneously enable clock pulses to D3 and to enable resetting D3 GATE. 1(CTS+1) sets D3 GATE and produces a $\overline{CRQ}$ from NAND-gate A24.12. D3 GATE enables NAND-gate A25.6 and $\overline{CRQ}$ performs a step-right function. On the next Ø3, seven clock pulses are applied to buffer register D3 and the character is serially shifted into the delay line (via the character entry register).

If a character is simultaneously shifted into D3 by SG23, $\overline{CRQ}$ enables a successive transfer into the delay line. This is possible because the cursor automatically appears at the inputs of A23.8 and A56.8 to enable setting SDL.

4-22.4.2.3.2 Receive Mode - Control Characters When Preceded by ESC. When control characters are received from the CPU, the specific operation performed by the Display Terminal depends upon whether or not ESC preceded the control character. When ESC precedes a control character, the character code is stored in memory and the operation associated with the code is not performed. This is accomplished in the following manner.

When an ESC control code enters D3 in the receive mode, the ESC decode (see paragraph 4-22.4.4) produces an output during 4(CTS+1). This output simultaneously jams SDL and BB3 to reset. The combined effect of these two operations is to inhibit shifting ESC into the delay line and to enable SG23 to shift another character into D3 'on-top-of' the ESC character. In addition, the output from the ESC decode is used to clock the ESC flip-flop to a set condition. When the ESC flip-flop is set, all control character decodes are inhibited and the CCC flip-flop (point B) remains reset.

When the character following ESC is shifted into D3, it is treated the same as a text character since all D3 decodes are inhibited. The cursor is located and the character code contained in D3 is serially shifted into the delay line via NAND-gate A25.6.

To briefly summarize, the reception of ESC results in setting the ESC flip-flop. The output of the ESC flip-flop is in turn used to inhibit the control character decodes connected to D3. Since the control character cannot be recognized, it is treated the same as text and permitted to enter the delay-line memory.

4-22.4.2.3.3 Receive Mode - Control Characters Not Preceded by ESC. When any control character except LF, ENQ, BELL, and NULL is shifted into D3 without being preceded by ESC, the applicable decode is enabled since the ESC flip-flop is not set. This permits the edit or cursor control function associated with the code to be performed. With the exception of the codes listed above, the decode output results in simultaneously setting the CCC flip-flop, performing the specified function (such as step up, erase, etc), and clearing BB3.

When point B goes low as a result of setting the CCC flip-flop, the SDL circuitry is disabled for as long as it takes to complete the function. After the function has been completed, the CCC flip-flop is reset to once again enable

AND-gate A19.8 (see paragraph 4-22.4.4). Since BB3 was cleared as soon as the control code was decoded, the next character is permitted to enter D3 'on-top-of' the control code. As soon as point B goes high (edit or cursor control function completed), the cursor is located and the character held in D3 is shifted into the delay line by SDL and D3 GATE.

For the majority of control codes, the specific function will be completed by the time the next character enters D3. The exceptions are BS, FF, DC1, DC3, and CAN. It is a programming requirement that these codes be followed by one or more NULL characters to give the Display Terminal time to perform the function. The operation of SDL when NULL characters are received is described in paragraph 4-22.4.2.3.4.

The LF code does not have to be preceded by ESC in order for the LF code to be stored. When LF is decoded, the function is performed without setting the CCC flip-flop or resetting BB3. As soon as the cursor is located, the LF code is permitted to enter memory in the same manner as a standard text character.

4-22.4.2.3.4 Receive Mode - Control Codes BELL, ENQ, and NULL. When control codes BELL, ENQ, and NULL are received from the CPU, independent decodes connected to D3 are enabled. These decoded outputs result in jamming SDL set and performing the following display terminal functions:

a. BELL - activates an audible alarm for approximately 160 ms

b. ENQ - causes the Display Terminal to enter the transmit mode

c. NULL - used to inhibit delay-line transfers until certain edit or cursor control functions have been accomplished

When either of these control codes is decoded in D3, the decode output is applied to the set inputs of A33.5 and A13.8 through gate A57.8. The result of this combination is to inhibit D3 GATE and enable clock pulses for shifting the next character into D3. Thus, BELL, ENQ, and NULL are never stored in the delay line even though the preceding character may have been an ESC code.

The low present at A57.8 jams A33.5 high and A13.8 low for one character time [4(CTS+1)→ 4(CTS+1)]. During this time, the character shift to the delay line is inhibited by the low applied to one input of A49.11. The D3 clock is enabled, however, thus permitting the next character to be shifted into D3 from D2. The ENQ, BELL, or NULL code held in D3 is therefore destroyed since it is essentially shifted into the 'blank wall' formed by inhibited NAND-gate A49.11.

As pointed out in paragraph 4-22.4.2.3.3, certain control codes require successive NULL codes in order to prevent losing data while the function is being performed. These requirements are:

a. BS and FF - These codes must be followed by three NULL characters. FF and CAN require up to 32 ms to perform

(0 to 16 ms to locate the cursor and 0 to 16 ms to perform the cursor reset or erase message function). DC3 requires up to 31 ms to perform (0 to 16 ms to locate the cursor and 15 ms to perform the step up function).

b. DC1, DC3, and CAN - These codes must be followed by two NULL characters.

Thus, if a control code (such as BS) is detected in D3, the function is performed and point B goes high. Since BS also resets BB3, the next character (a NULL code) is permitted to enter D3. As soon as NULL has been shifted into the register, A57.8 produces a low output which enables SDL. This, in turn, resets BB3 and allows the next character (a NULL) to enter D3. This process continues for still another NULL character until, after 33.32 ms, four characters have been received from the CPU. The fourth character (a text character) is then in D3 and may be acted upon in the normal manner because Function Complete has by then reset the CCC F/F. This is illustrated in figure 4-30.

	D1	D2	D3	Time
Look for Cursor	NULL	NULL	BS	T_0
	NULL	NULL	NULL	T_0 +8.33 ms
Cursor Found Perform Function	TEXT	NULL	NULL	T_0 +16.66 ms
	TEXT	TEXT	NULL	T_0 +24.99 ms
Function Complete	TEXT	TEXT	TEXT	T_0 +33.32 ms

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Figure 4-30. Use of NULL Control Codes

4-22.4.2.3.5 Transmit Mode - Text Character. In the transmit mode, the basic objective of the SDL circuitry is to enable data transfer from the delay line to buffer register D1. Note that as soon as the request-to-send line is raised (in either conversational mode), it is impossible for RE to go high until transmission has ended. Thus D3 gate is disabled during transmit and data is not permitted to re-enter the delay line through NAND-gate A25.6.

In the enquiry-response mode BB1, BB2, and BB3 are initially low due to the $\overline{\text{ETXD3}}$ pulse present at the end of the last transmit or receive sequence. Enter Header then jams STX and DA into D3 and D2, setting BB2 and BB3. With BB1 still low, NAND-gate A23.6 is enabled when T goes high. As soon as the cursor is found, SDL is set by 4(CTS+1) and clock pulses are applied to D1. These pulses shift the character associat with the cursor into buffer register D1. During 1(CTS+1), $\overline{\text{CRQ}}$ performs a step-right function to automatically enable one input of AND-gate A56.8. However, since it takes 8.33 ms

to transmit the character held in D3, busy-bits BB1, BB2, and BB3 will all be high and NAND-gate A23.6 will be inhibited. This,in turn, inhibits setting SDL and no further transfer from memory can be accomplished.

In 16 ms, the cursor again appears at the input to AND-gate A56.8. By now, STX and DA should have been transmitted and the first text character should presently be in D3. The condition $\overline{BB1}$ and $\overline{BB2}$ enables NAND-gate A23.6, and the second text character is shifted out of memory through D1 and into D2. Since the cursor was again stepped right by $\overline{CRQ}$, the condition $\overline{BB1}$ and cursor will enable the transfer of a second text character into D1 before the cursor is released.

The transmit operation continues in this manner until either the LF or ETX control code is detected in D1. Each time the cursor enters the character entry register, at least one, and usually two, characters are extracted from memory and shifted into D1.

When ETX is detected in D1, the end-of-transmission is signified. The combination of ETXD1, SDL, and T sets flip-flop A10.8 during 3(CTS+1). When point A goes low, all further transfers from the delay line are inhibited. When BB1, BB2, and BB3 are all empty, the XMIT Time Out pulse resets A50.12 to its quiescent state.

When LF is detected in D1, a carriage return is indicated. Thus, all characters of the line following LF are skipped and the read continues at the first character position of the next line. The operation of the SDL circuitry under these circumstances is determined by flip-flop A13.8. Point C is normally high due to $\overline{4CTS}$ pulses which reset A13.8 once per character. In the absence of a clock pulse, point C remains high, enabling one input to AND-gate A56.8. When LF is detected in D1 during transmit, 3(CTS+1) is gated through the LFD1 decode to set A13.8. This then inhibits SDL for one character time (until the next $\overline{4CTS}$) and assures that the time hazard of extracting the character following LF does not occur. When LF is detected in D1, an advance-line cursor control operation is performed (see paragraph 4-23.3.4). This moves the cursor from 1 to 88 characters to the right. When the cursor is again located in the character entry register, transfers from the delay line are again enabled. Thus, the characters between LF and the new cursor position are not extracted from memory and are therefore not transmitted.

In the polling conversational mode, the operation of the SDL circuitry is basically unchanged once data extraction is initiated. From previous discussions, STX, DA, and ETX are jammed into D3, D2, and D1, respectively, by Enter Header. This occurs as soon as a polling read directive is detected. As shown in figure 4-29, Enter Header also sets A10.8 to force point A low. The delay line is then examined to determine whether ETX code has been entered by the operator. If an ETX is located, ETX found clears BB1 and simultaneously resets A50.12. The combination of point A high and $\overline{BB1}$ enables NAND-gate A23.6 and SDL permits shifting the first text character into D1 'on-top-of' the previously entered ETX character.

4-22.4.3 Buffer Registers

The Communications Control Board contains three 7-bit registers designated as buffer registers D1, D2, and D3. The purpose of these registers is to provide a buffer to compensate for the different rates used internally and externally for transferring data.

Digital information is transferred between the Display Terminal and the CPU at a rate of 1200 baud (120 10-bit characters per second). This transfer rate corresponds to a character time of 8.33 ms; thus, it takes 8.33 ms to either transmit or receive one complete 10-bit character. This transfer rate is controlled by an internal 1200-baud counter which develops 10 separate phase A clock pulses for each character transferred between the devices (see paragraph 4-24.9).

Internally, data is shifted through the buffer registers at a rate of 76.8 kHz, or exactly 64 times faster than a character can be transmitted to or received from the CPU. This transfer rate corresponds to 13 μs per character.

Figure 4-31 is a block diagram of the buffer registers. In the receive mode, the buffer registers generally operate in the following manner after the receive enable circuitry is enabled. Data is coupled through the received data interface circuits and applied to the input of D1. The phase A clock, which starts counting as soon as the character start bit is detected on the received data line, produces seven clock pulses to shift the incoming data into D1. After 8.33 ms, the first complete character is held in D1, available for transfer to D2.

The transfer from D1 to D2 is enabled when SG12 permits applying seven high-speed pulses to both registers simultaneously. This transfer takes approximately 13 μs. The transfer from D2 to D3 is handled in the same manner by SG23 and after a minimum of 8.356 ms (8.33 ms + 26 μs), the character is contained in D3. Simultaneously, another character may be entering D1 from the received data line.

The character held in D3 remains there until the cursor is located in memory. This can take from 0 to 16 ms, depending upon what point in time the character was shifted into D3. For example, the cursor may have been shifted through the character entry register just before the received character was shifted into D3. If this is the case, 16 ms later the cursor reappears and the character in D3 is inserted into memory via the character entry register. From the character entry register, the character code is applied to the character readout register and held for one character time. This results in displaying the character associated with the code. The character code is simultaneously serially shifted into memory where it refreshes the display presentation.

Since it takes 8.33 ms to receive one character, the three buffer registers do not completely fill until 24.99 ms have elapsed. However, since the cursor is located in a maximum of 16 ms, the buffer registers do not normally fill during receive. An exception to this rule is when certain control codes which require both locating the cursor (0 to 16 ms) and performing a time consuming edit or cursor control operation (up to 16 ms) are received. If this is the case, NULL

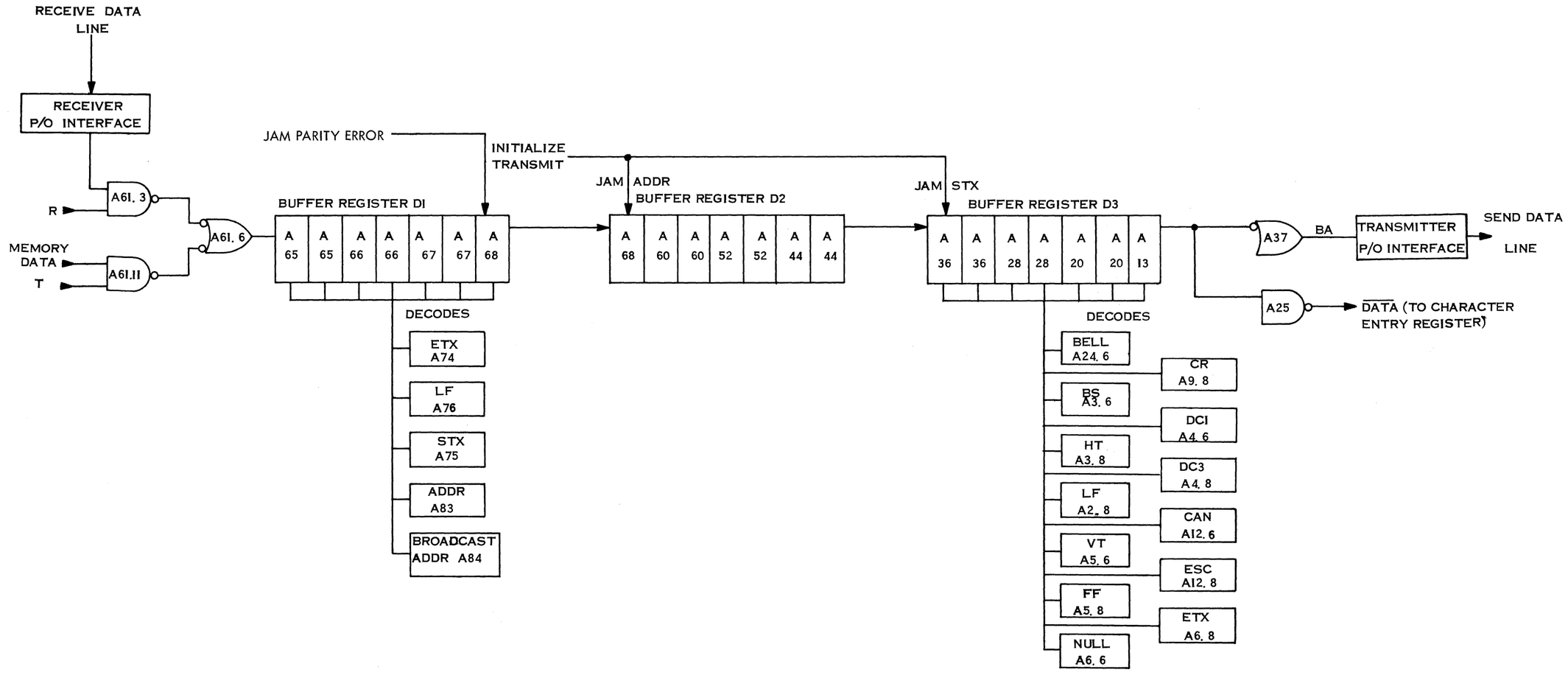

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Figure 4-31. Buffer Registers, Block Diagram

characters are used to provide time-fill between the control code and the next information character of the message. This, in turn, prevents losing valid information when the registers fill to capacity and then overfill due to the continuous transfer of data into D1.

In the transmit mode, the buffer registers provide a smooth release of data from the delay line to the CPU even though the memory is accessible only once every 16 ms. Each time the cursor appears in the character entry register, one and usually two characters can be extracted from the memory and shifted into the buffer registers. The transfer from memory, as well as the subsequent transfers from D1 to D2 and D2 to D3, occurs at the high-speed rate of 13 μs/character. Because of the much slower transmission rate, the characters stack up and the read from the delay line must be terminated by releasing the cursor. In the 16 ms it takes for the cursor to once again appear in the character entry register, nearly two characters (16.66 ms) can be shifted out of D3 to the CPU. Since there are three buffer registers, however, a third character is always available for transfer to D3 even though 16 ms have elapsed since the last time the memory was accessed. This feature provides a steady stream of serial data from D3 to the CPU.

4-22.4.3.1 Buffer Register D1. Buffer register D1 and the D1 decodes are shown in figure 4-32. The register consists of seven D-type flip-flops which share the common clock inputs from inverter-driver A14.6. The operation of D1 in first the receive and then the transmit modes of operation are briefly outlined below.

In the receive mode, each time a start bit is detected on the received data line, the 1200-baud counter begins counting up to 10 (see paragraph 4-24.9). As soon as the decimal counter reaches a count corresponding to the first data bit (i.e., $\overline{STT}$ and $\overline{STP}$ and $\overline{PAR}$, NAND-gate A47.8 is enabled and seven phase A pulses are applied through A14.6 to the clock input of each register flip-flop. These seven pulses shift the incoming character into D1 through A61.3 regardless of the bit configuration of the character. (R is always high unless the Display Terminal is transmitting data.)

If a valid message is being received, the first character shifted into D1 should be STX. If this is the case, during the STX character parity count, STX decode A75.8 is enabled to set the STX flip-flop. The STX character is held in D1 until the decimal counter cycles through the counts $\overline{STP}$ (of STX) and $\overline{STT}$ (of ADDR). Again, seven phase A pulses are applied through A14.6 to shift the next character into D1. The Display Terminal interprets this code to determine whether it corresponds to a previously hard-wired address code. If the character received is the proper DA, ADDR decode A83.8 is enabled to set the ADDR flip-flop during the parity count. This, in turn, develops an RE level which permits all successive characters to enter buffer register D2. The next character of the message is shifted into D1 in a similar manner, except that this time the phase A pulse occurring during $\overline{PAR}$ is used to set BB1 during 1(CTS+1). BB1, in turn, enables SG12 during 4CTS, and seven fast-clock pulses [beginning with 3(CTS+2)] are applied to D1 through NAND-gate A49.8. These pulses serially shift the character out of D1 and into D2. While this is occurring (it takes 13 μs), the decimal counter is cycling through $\overline{STP}$ and $\overline{STT}$ (830 μs). Thus, by the time the condition $\overline{STP}$, $\overline{STT}$, and $\overline{PAR}$ is once again true, D1 is empty and prepared to accept the next character of the message.

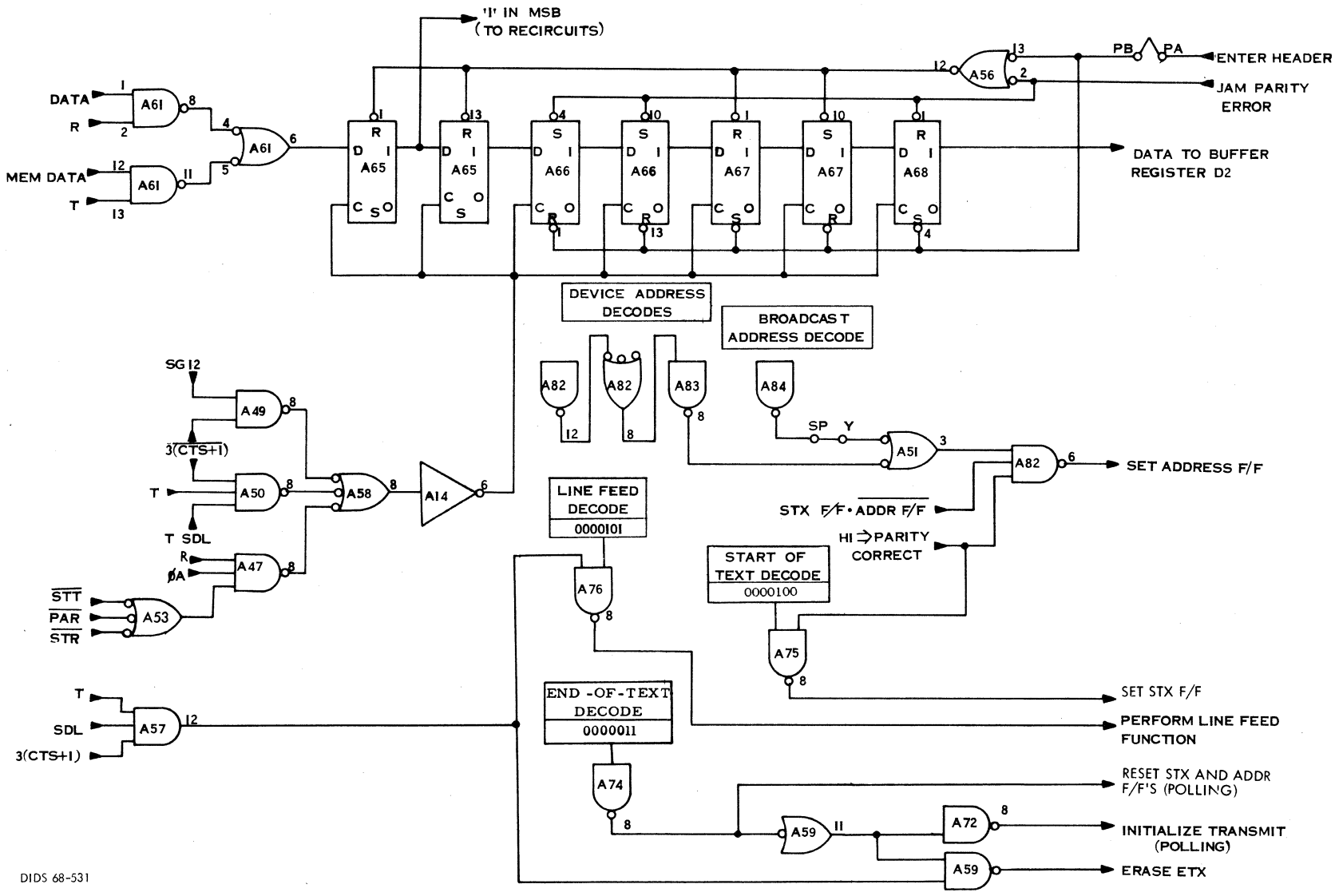

Figure 4-32. Buffer Register D1, Logic Diagram

If any character following DA is found to have an erroneous number of 1's a parity error code is jammed into D1 during the decimal counter parity count. This code (0011010) is jammed into the register 'on-top-of' the erroneous character by means of gate A56.12. The code is transferred in the usual manner through D2 and D3 and into the delay line. The code appears on the CRT screen as a blank space in place of the erroneous character.

In the polling conversational mode, a '1' in the MSB of the address code resets the STX flip-flop and inhibits the RE level. If the following character is an ETX, ETX decode A74.8 produces an output to enable one input to A72.8 and subsequently Initialize Transmit when an ETX is found in the memory.

In the transmit mode, D1 has an entirely different role. Since two forms of operation are involved, depending upon the conversational mode, each form is described separately. To assist in understanding the following text, alternately refer to figures 4-28, 4-29, and 4-32.

In the polling conversational mode, Enter Header simultaneously performs the following:

a. Jams STX into D3, DA into D2, and ETX into D1, and sets BB3, BB2, and BB1

b. Inhibits setting SDL until an ETX is detected in the refresh memory loop (see figure 4-29)

c. Sets flip-flop A78.11 to enable clearing BB1 when an ETX is detected in the refresh memory loop (see figure 4-24)

d. Enables setting T high after a delay of 16 ms

After T goes high, the STX character in D3 is shifted out at the 1200-baud transmission rate. Simultaneously, the memory is accessed in search of an ETX code. The specific operation of D1 depends upon whether or not an ETX has been inserted into memory by the operator.

Assuming that an ETX code is found in memory, BB1 is cleared. This, in turn, enables setting SDL as soon as the cursor is shifted into the character entry register from the delay line. Note that it may easily take more than 16 ms to find both the ETX code and the cursor in memory. During this time, STX and a portion of DA have been transmitted to the CPU leaving D2 empty. As soon as the cursor is found, SDL goes high to enable NAND-gate A50.8. Seven fast clock pulses are gated through A14.6 to clock the character from memory through NAND-gate A61.11 and into D1. This shift sets BB1 which in turn enables SG12 since BB2 indicates a D2-empty status. SG12 enables NAND-gate A49.8, and the character in D1 is shifted into D2. For each successive character in memory, the clock pulses applied to D1 are alternately enabled through NAND-gate A50.8 (shift from delay line) or NAND-gate A49.8 (shift from D1 to D2). When ETX is finally shifted into D1, decode A74.8 is enabled and, during 3CTS+1, an ERASE ETX pulse is produced. This pulse sets a flip-flop (A9.1) on the display logic board which holds the delay-line data-input line low for one character time, thus erasing the ETX character from memory.

If an ETX code is not found in memory, BB1 is not cleared and SDL is therefore inhibited. As soon as DA is shifted out of D2, the D2 empty status enables setting SG12. SG12, in turn, enables seven fast clock pulses through NAND-gate A49.8. In this manner, the ETX character held in D1 is shifted to D2. When ETX is finally shifted out of D3, the transmit mode is terminated by the transmit time-out circuit.

In the enquiry-response conversational mode, Enter Header jams STX into D3 and DA into D2 and transmission begins one frame time later when FΔØ3 enables T to go high. This results in shifting out the header characters while the cursor bit is being searched for in memory. When the cursor is located, SDL goes high to permit shifting the character associated with the cursor into D1. SG12 is then enabled by BB1 and $\overline{BB2}$, and a serial transfer from D1 to D2 occurs. Transmission continues in this manner until ETX is shifted into D1. When this occurs, the Erase ETX erases the code from memory. When ETX is finally shifted out of D3, the transmit time-out circuit is enabled and transmission is terminated.

4-22.4.3.2 Buffer Register D2. Buffer register D2 (shown in figure 4-33) consists of seven D-type flip-flops which share the common clock inputs from inverter-driver A38.8.

In the receive mode, SG12 goes high when a D1-full, D2-empty status is indicated by BB1 and BB2. This enables seven fast clock pulses through NAND-gate A49.8 which shift the character out of D1 and into D2. Since the RE steering logic must be high in order to set BB1, STX and DA must be received by the Display Terminal before a transfer of data from D1 into D2 is enabled. Once a character is shifted into D2, a D2-full and D3-empty status from BB2 and BB3 enables SG23. SG23 in turn enables NAND-gate A49.6 and seven fast-clock pulses are gated through A38.8 to shift the character from D2 to D3.

In the transmit mode, Initialize Transmit goes low to jam a NULL character (0000000) into D2. Up to 16 ms later, Enter Header jams a previously determined device DA code into D2. This address character may correspond to any one of 64 different DA's available for use by the system. In any case, the address code jammed into D2 normally corresponds to the address code decoded by the DA decode connected to D1.

When DA is jammed into D2, BB2 is set to indicate the D2 full status. As soon as STX is shifted out of D3 (8.33 ms after T goes high), a BB2 and $\overline{BB3}$ status enables SG23 to transfer the DA code from D2 to D3.

4-22.4.3.3 Buffer Register D3. Buffer register D3 and its associated circuits are shown in figures 4-34 and Raytheon Drawing No. 408025. The register consists of seven D-type flip-flops which share common clock inputs from inverter driver A14.8.

In the receive mode, SG23 goes high when a D2 full, D3 empty status is indicated by BB2 and BB3. This enables NAND-gate A49.6, and seven fast clock pulses are applied to D3 to shift the character into the register. BB3 is set as a result of the D3 full condition and the next time the cursor appears in the charac-

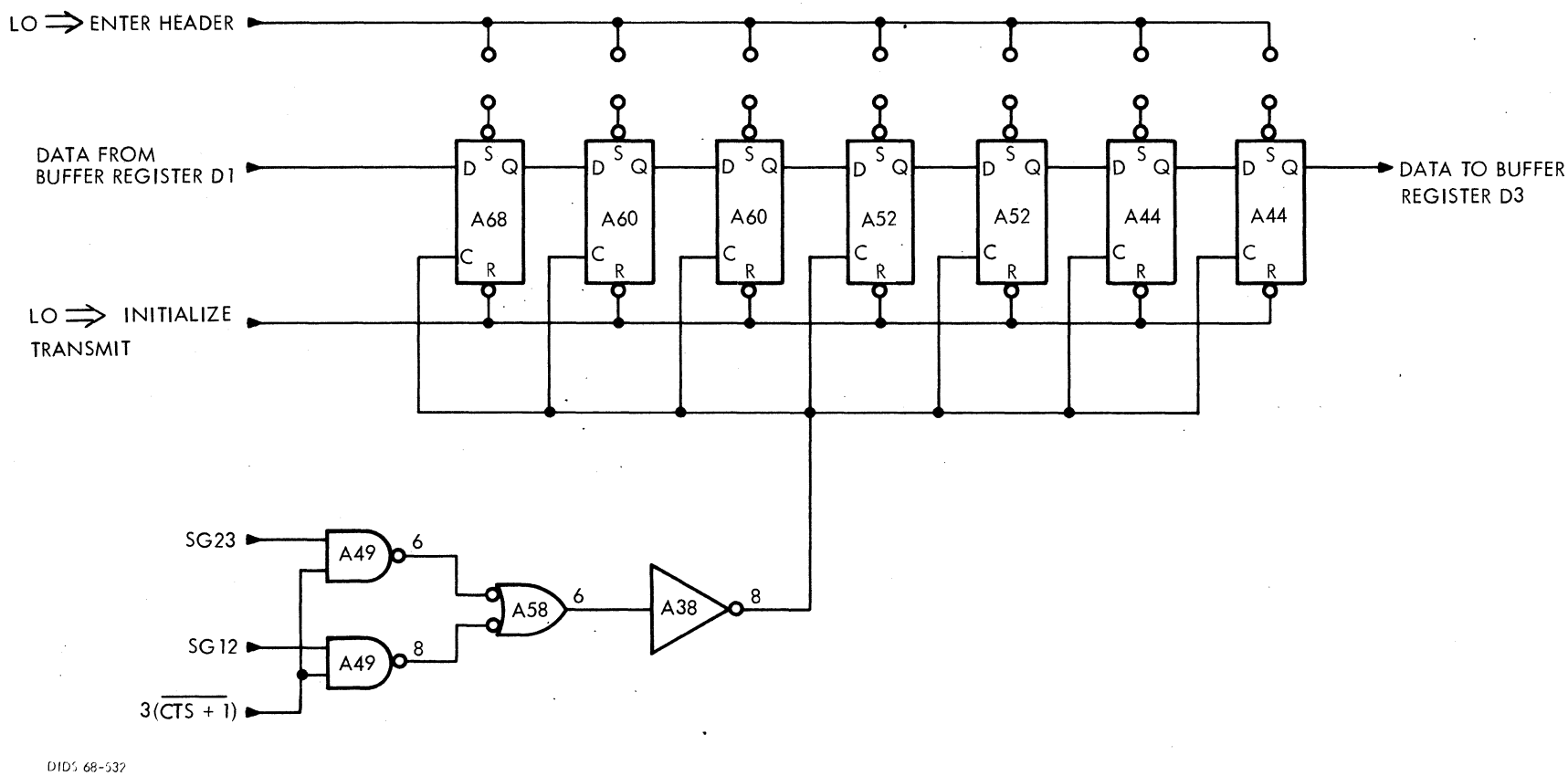

Figure 4-33. Buffer Register D2, Logic Diagram

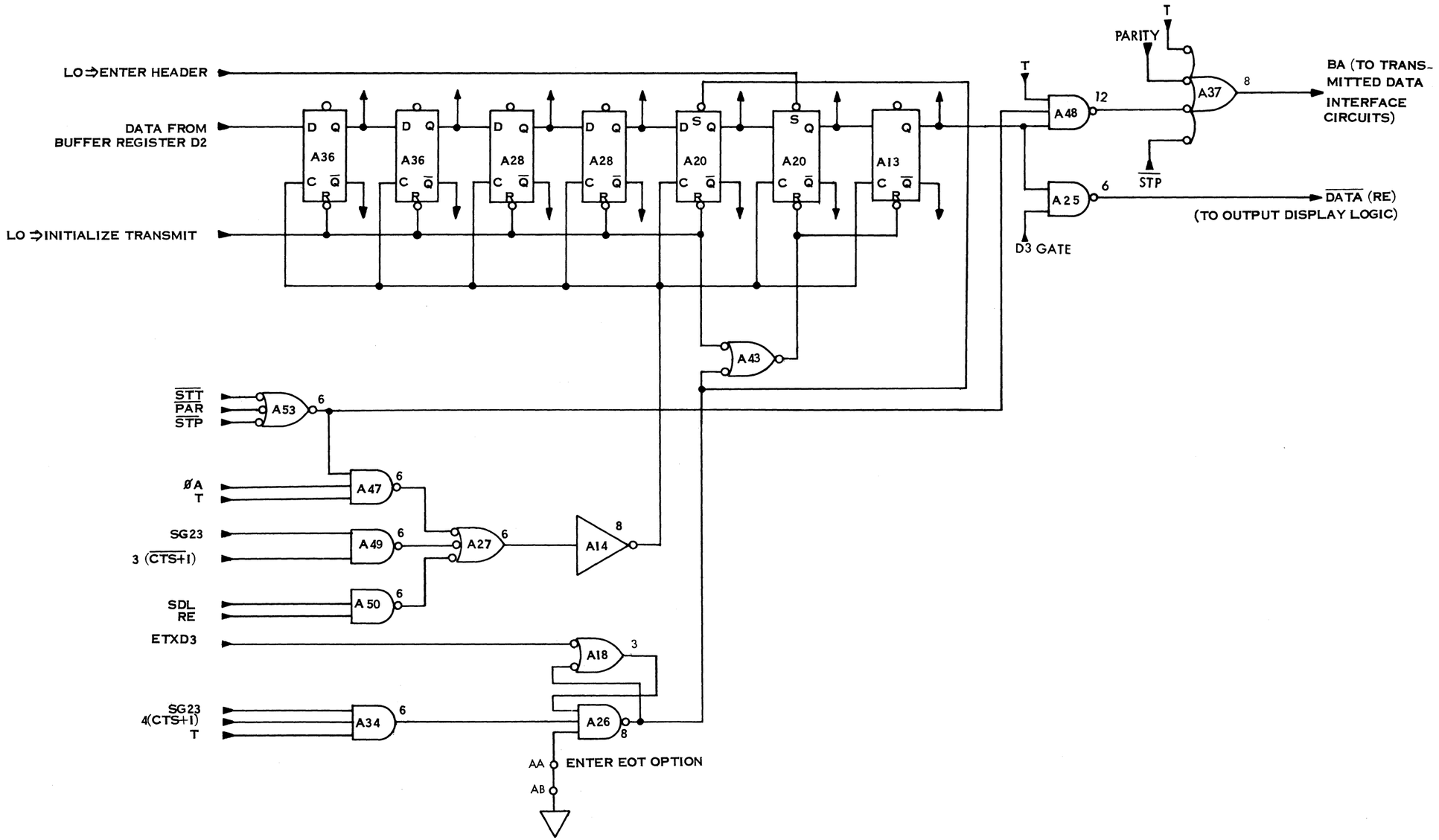

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Figure 4-34. Buffer Register D3, Logic Diagram

ter entry register, SDL goes high. SDL enables NAND-gate A50.6 and the D3 GATE flip-flop. When this occurs, seven additional clock pulses shift the character held in D3 into the delay line via NAND-gate A25.6.

When a control code is received as part of a data message, the D3 decode circuitry is employed to determine the conditions surrounding the reception of the code. These decodes, as well as the ESC and CCC flip-flops, are discussed in paragraph 4-22.4.4 and illustrated in Raytheon Drawing No. 408025 and figure 4-35.

In the transmit mode, Initialize Transmit jams each flip-flop of D3 to reset to insert a NULL character (0000000) into the register. Up to 16 ms later, Enter Header jams flip-flop A20.9 set to insert an STX code (0000010) into the register. Enter Header also jams BB3 to indicate a D3 full status. After a second 16-ms delay, T goes high and the combination of T and BB3 develops $\overline{\text{ØA}}$ gate to start the 10-bit decimal counter. When the counter steps from $\overline{\text{STP}}$ to $\overline{\text{STT}}$, a start bit is placed on the transmitted data line through NOR-gate A37.8. On the next phase A pulse, the counter steps from $\overline{\text{STT}}$ and gate A53.6 is enabled. This simultaneously enables NAND-gate A47.6 and A48.12. Seven phase A pulses are enabled through A47.6 which shift the character (STX) onto the transmitted data line. Simultaneously, the character is applied to the parity check and generation circuit (see paragraph 4-22.3.2). When the decimal counter reaches the $\overline{\text{PAR}}$ count, the output of A53.6 goes low to inhibit gates A47.6 and A48.12. The result of the parity check is then gated onto the transmitted data line through NOR-gate A37.8 and the interface circuits.

The transmission of STX from D3 (or any other character) takes 8.33 ms to accomplish. The cursor, which is circulating through memory attached to the first character of the message, may or may not appear in the character entry register during the 8.33-ms time interval. As previously stated, locating the cursor results in simultaneously shifting a character into D1 and automatically stepping the cursor one position to the right (CRQ).

Assuming that the cursor is not found during the time it takes to transmit STX, the momentary status of the buffer registers is D1-empty, D2-DA, D3-empty. BB3, which is reset during the parity count of the transmitted character, goes low to enable SG23. This, in turn, enables the application of seven fast-clock pulses through A49.6 which shift DA from D2 to D3. With the conditions $\overline{\text{BB1}}$, $\overline{\text{BB2}}$, and BB3, DA is shifted out of D3 when NAND-gate A47.6 is enabled. Before DA can be completely shifted out of D3, the cursor is located and a character is extracted from the delay line. (There is a 646-µs difference between the memory access time of 16.026 ms and the two-character transmission time, 16.660 ms). The character extracted from the delay line is shifted straight through D1 and into D2 due to SDL setting BB1, thus enabling SG12. Since SG12 will shift the character out of D1, a $\overline{\text{BB1}}$ is present after 13 µs and the second successive character is shifted out of the delay line. Thus, after approximately 26 µs have elapsed, DA is still in D3, 1st text is in D2, and 2nd text is in D1. This condition (BB1, BB2 and BB3) disables SDL and the cursor is released. After 16 ms it once again appears and another character (or possibly two) is extracted from the delay line.

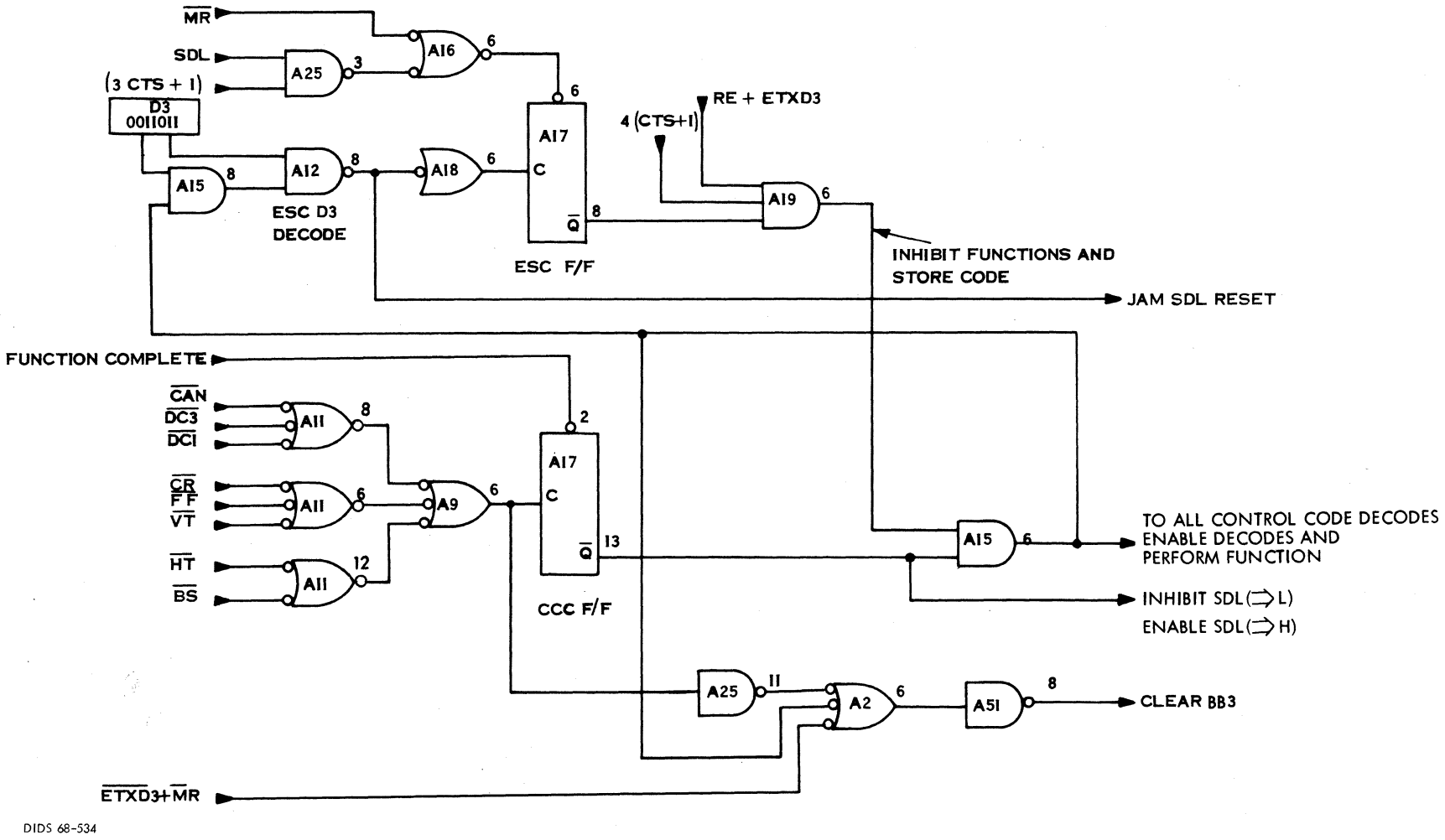

Figure 4-35. ESC and CCC Flip-Flops and Associated Circuits, Logic Diagram

D3 continues to operate in this manner until an ETX character code is shifted into D3 from the memory. As discussed in paragraph 4-22.1.1, this disables the transmit operation by disabling T and returning all transmit/receive enable circuits to the receive (R) state.

When the Enter EOT wiring option is employed, an EOT character (0000100) is inserted as the last character of the message rather than an ETX (0000011). To accomplish this, the wire connecting terminals AA and AB is removed to place a constant high at one input of NAND-gate A26.8. When SG23 goes high during transmit to indicate a D2 to D3 transfer, the second input of A26.8 is enabled every 4(CTS+1). If the character entered into D3 by SG23 was an ETX, the ETXD3 decode is enabled during 3CTS. This sets A18.3 and enables 4(CTS+1) to be gated through to reset the two LSB's of D3 and to set the third LSB. In this manner, a code conversion is accomplished and EOT is transmitted to the CPU instead of ETX.

4-22.4.4 Escape and Communications Control Code Flip-Flops

The ESC and CCC flip-flops and their associated circuits are shown in figure 4-35. ESC codes are used in messages from the CPU to enable the storage of the following control codes:

CAN
DC3
DC1
CR
FF
VT
HT
BS
ETX
ESC

When one of the preceding control codes is received immediately after an ESC code, the specified edit or cursor control function is not performed and the control code is permitted to enter the delay-line memory. Conversely, if the code is received without being preceded by ESC, the specified function is performed but the code is not permitted to enter the delay-line memory. The circuit shown in figure 4-35 performs this function in the following manner.

Normally, a high is present at the reset output of the CCC and ESC flip-flops. When the Display Terminal is in the receive mode (RE=HIGH), A15.6 goes high once per character during 4(CTS+1).

When an ESC control code is shifted into D3, ESC decode A12.8 is enabled during 4(CTS+1). The leading edge of this pulse simultaneously resets SDL and BB3, while the trailing edge toggles the ESC flip-flop to a set condition. Resetting SDL prohibits shifting the ESC code into memory, while the reset condition of BB3 enables SG23 to shift the next character of the message into D3.

Once the ESC flip-flop is set, it remains set until SDL goes high to enable 3(CTS+1) to be gated through A25.3.

SDL in this instance will not go high until the cursor is located. When the cursor appears in the character entry register, SDL goes high during 4(CTS+1) to enable seven fast clock pulses [3(CTS+1) through 3(CTS)] to shift the control code into memory. Following this transfer, 3CTS+1 occurs to reset the ESC flip-flop through NAND-gate A25.3. This then returns the circuit to its quiescent state.

When a control code is received without being preceded by ESC, all control code decodes are enabled due to a high at the output of A15.6. The following text describes what occurs when each of the listed codes are received in this manner.

4-22.4.4.1 CAN, DC3, DC1, CR, FF, VT, HT, BS Decodes (see figure 4-35)

When any of these control codes are received without being preceded in the message by ESC, the applicable decode is enabled because of a high present at A15.6. The decode output is used to accomplish the specified edit or cursor control operation; it simultaneously appears at an input of either A11.8, A11.6 or A11.12. This places a high going level at the clock input of A17.13 which simultaneously sets the CCC flip-flop and clears BB3. The combined effect of these two operations is to allow the next character of the message to be shifted into D3 by SG23 and to inhibit SDL until the edit or cursor control function is completed. Thus, the control code previously held in D3 is destroyed and replaced by the next character of the message.

As soon as the edit or cursor control function is completed, a Function Complete level jams the CCC flip-flop reset to once again enable A15.6. This, in turn, results in enabling SDL as soon as the cursor is located and the character held in D3 is shifted into the delay-line memory.

4-22.4.4.2 ENQ, BELL, and NULL Decodes

When any of these control codes are received, the SDL flip-flop and a special one-character delay flip-flop are jammed set during 3CTS. The combined effect of these two operations is to simultaneously enable SDL and disable D3 GATE, thereby enabling clock pulses to shift the next character from D2.

Since D3 GATE is disabled, the NULL, ENQ or BELL control code is destroyed by shifting the character into the blank wall formed by $\overline{\text{D3 GATE}}$.

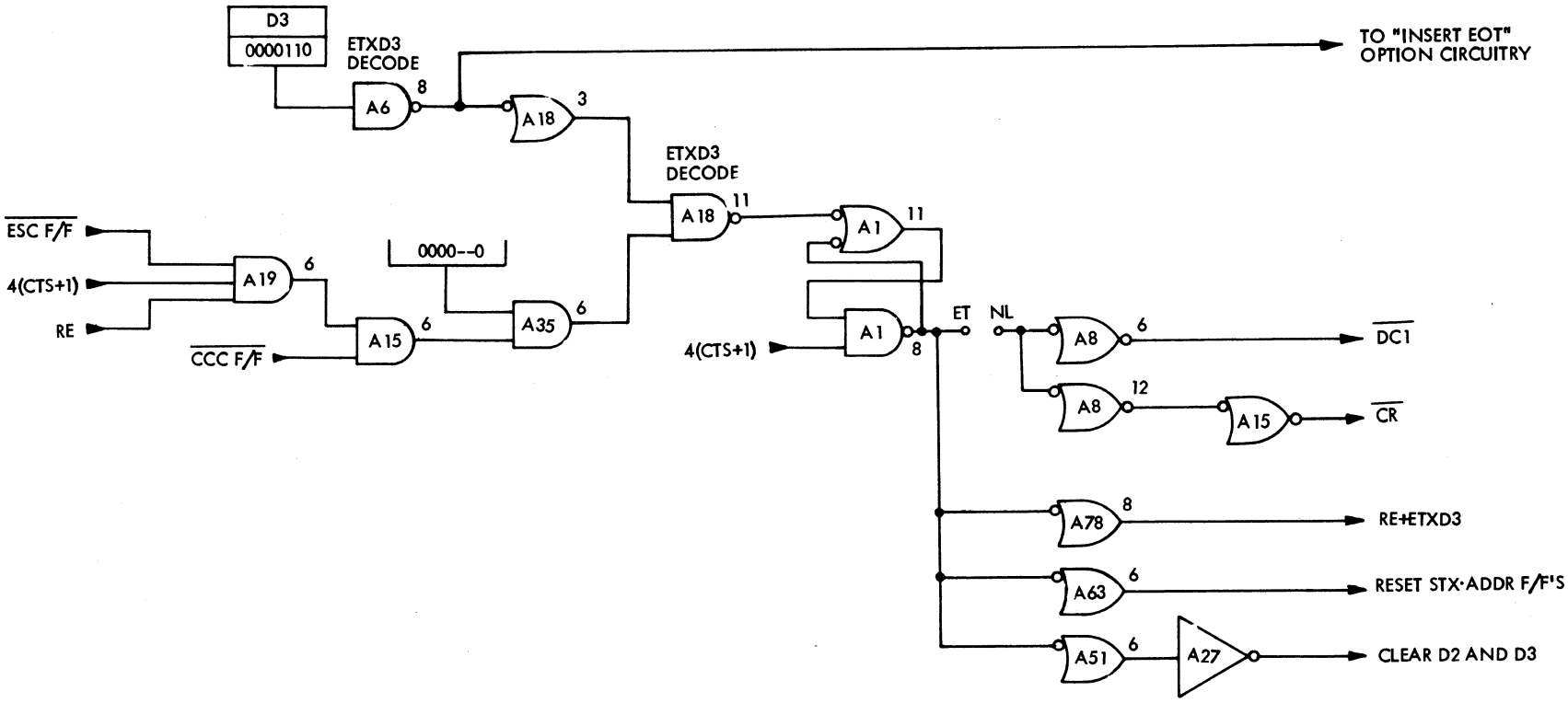

Figure 4-36. ETX D3 Decode and Associated Circuits, Logic Diagram

4-22.4.4.3 ETX Decode (see figure 4-36)

There are essentially two ETX decodes connected to D3. One of the decodes, A6.8, produces an output in either the transmit or the receive mode. This output is used to enable both the second ETX decode A18.11, and the Enter EOT wiring option circuitry (see paragraph 4-22.4.3.3). Although this option may be enabled in either the transmit or receive mode, the optional operation has no meaning in the receive mode (see below).

The second ETX decode, A18.11, is enabled only during RE due to AND-gate A19.6. If an ETX control code is received without being preceded by an ESC code, AND-gate A19.6 is enabled during 4(CTS+1). This pulse is coupled through secondary decode A18.11 and applied to the set input of cross-connected flip-flop A1.11/A1.8. The flip-flop is set to enable 4(CTS+1) to be gated through to produce an $\overline{\text{ETXD3}}$ output. Assuming for the moment that the Advance Line at End of Receive option is not employed, $\overline{\text{ETXD3}}$ has the sole function of resetting the RE mode. This is accomplished by simultaneously clearing the STX and ADDR flip-flops and buffer registers D2 and D3. When D3 is cleared, the previously held ETX character is destroyed to prevent its entry into the delay-line memory.

When the Advance Line at End of Receive option is used, a wire is connected between terminals ET and NL. Thus, when the $\overline{\text{ETXD3}}$ pulse is developed by 4(CTS+1), two outputs are produced which result in erasing the line and advancing the cursor to the first character position of the next line.

4-23 DISPLAY LOGIC BOARD A13

The display logic board functions as a keyboard interface to permit entry of 7-bit data characters from the keyboard. The character entry and readout register contained on this board enable visual characters on the CRT screen to be displayed and refreshed. Included on this board are various edit and cursor control circuits which enable keyboard operators or CPU programs to edit and format the screen presentation.

4-23.1 Character Entry Register

The character entry (CE) register, shown in figure 4-37, consists of eight register flip-flops and a 'cursor-located' flip-flop. Data enters the character entry register from three different sources: the delay line, the keyboard, or buffer register D3. In the transmit mode, data is extracted from memory by coupling data from the CE register MSB flip-flop to buffer register D1. The source of input data is dependent upon the operating status of the Display Terminal at any particular moment as pointed out in the following text.

4-23.1.1 Data from Delay Line

The CE register (as part of the refresh memory loop) accepts data characters from the delay line, causes the character to be displayed on the screen, and then returns the character to the delay line. As stated previously, the delay line is an internal storage device that provides a 16.026-ms delay of data between input and output. Since the CE register is connected in series

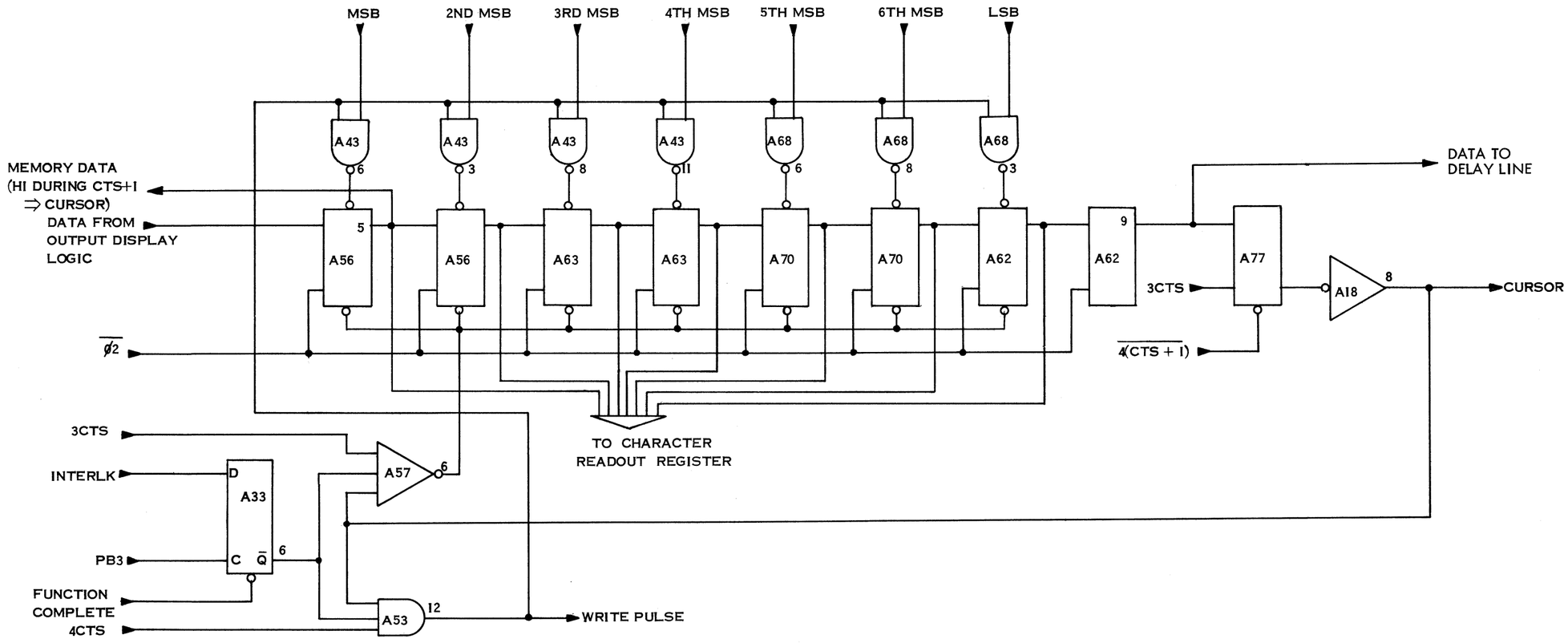

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Figure 4-37. Character Entry Register, Logic Diagram

with the delay line to form a loop, one character is always present in the CE register for display. When a complete character has been shifted into the CE register, a pulse enables the character code to be parallel-transferred into the character readout (CR) register for displaying a corresponding visual character on the CRT screen.

Data characters circulating in the refresh memory consist of eight bits. These eight bits contain seven data bit positions which are used to carry character code information; the eighth bit position is reserved for the cursor. When the cursor is attached to a character code, the cursor bit position contains a '1'. Conversely, if the character code does not have the cursor attached, the cursor bit position is '0'. The cursor bit is moveable and can be attached to only one of the 1040 data characters held in the delay line.

Data from the delay line enters the CE register at the input to register flip-flop A56.5 after passing through the output display logic. Clock pulses are constantly applied to the CE register, providing an uninterrupted stream of serial data constantly circulating through the register. Since data is transferred LSB first, the cursor bit position is the first portion of a character to enter the register. This bit is clocked into A56.5 during 2(CTS) so that during the period 2(CTS) through 2(CTS+1) the cursor bit is held by flip-flop A56.5. The next seven successive phase 2 pulses shift the character into the register and after eight bit times, a complete character is held in the register. It is during this time (2CTS) that a non volatile transfer places the character code into the character readout (CR) register.

Data exits the CE register from set output A62.9 and is coupled to the delay line via the input display logic. After a character enters the delay line, it is returned to the CE register after a delay of 16.026 ms. This time interval corresponds to the frame time, or the time required for the CRT scan to leave a particular position on the screen, move through an entire scan of the screen, and return to the original position on the screen. Since the character code will once again be transferred to the CR register, the visual character displayed on the CRT screen will be refreshed .

4-23.1.2 Data from Keyboard

The CE register enables display terminal operators to enter keyboard information into the refresh memory loop. Each time the operator depresses a character key, a 7-bit digital code and an INTERLK pulse are produced. The 7-bit code is peculiar to the particular key depressed, while INTERLK is present every time a character key is depressed.

Assuming that the 'A' key is depressed, the code present at the inputs to the strobe gates is 1100001. This code is present at the input to each gate for as long as the key is held depressed (usually 20 to 50 ms).

The INTERLK input to flip-flop A33.6 is normally high; this holds the flip-flop set. The depression of any character key causes a high-to-low level change and enables the display logic clock (see paragraph 4-23.3.1). The first F(Δ) that occurs after key depression develops a PB3 clock pulse to reset the flip-flop. A33.6 remains reset until the cursor is located in memory and a step-right function is accomplished.

The cursor, which is attached to the LSB of one character in memory, is shifted into the CE register from 0 to 16 ms later. When the character containing the cursor is shifted into the CE register, a high is applied to cursor-located flip-flop A77.8 during CTS. On the rising edge of 3CTS, A77.8 is set to produce a high input at A18.8. This high enables A57.6 and during 3CTS a clear pulse is gated through the gate to clear the CE register. Thus, if a character code is associated with the cursor, the code is cleared before entering a new character from the keyboard. This accounts for the destructive effect of positioning the cursor over a character and then depressing a character key.

One phase time after clearing the CE register, AND-gate A53.12 is enabled and a write pulse is produced. This pulse is applied to the second input of each strobe gate; its purpose is to jam the 7-bit character code into the CE register.

When the INTERLK pulse reset A33.6, it simultaneously enabled the step-right flip-flop. The step-right function is initiated as soon as the cursor is located in the CE register (see paragraph 4-22.3.2). Consequently, three separate actions occur almost simultaneously: (1) clear CE register, (2) strobe digital code into CE register, and (3) step the cursor right one character position.

4-23.1.3 Data from Buffer Register D3

In the receive mode, data is coupled from buffer register D3 and enters the CE register at the input to A56.5. From the previous discussion of SDL, data is permitted to enter the CE register only at the cursor position; therefore, the cursor must be located (by SDL) before a serial transfer can occur. This is accomplished by monitoring the set output of A56.5.

Data in the memory loop is circulated through the CE register in the manner previously described. Once per frame during the time corresponding to the visible cursor on the screen, the output of A56.5 goes high and remains high during the interval 2CTS through 2(CTS+1). The SDL circuitry senses this level and during 3(CTS+1) the SDL flip-flop is set. As previously stated, SDL enables clock pulses for shifting the character out of D3. The phase 2 register clock (which is always present) then shifts the received character into the CE register. The cursor is automatically stepped right one character position by a CRQ pulse developed by the SDL circuitry.

4-23.1.4 Data to Buffer Register D1

In the transmit mode, data is extracted from memory beginning at the cursor position and terminating at the first ETX character.

Before transmitting data, the memory is accessed in search of an ETX code. If an ETX has been inserted into memory by the operator, ETX decode A58.8 is enabled once per frame. The decoded output is used to develop an ETXSR pulse which is used to enable the transmit sequence. Once the transmit enable circuitry is enabled, data is extracted from memory by SDL each time the cursor is shifted into the CE register. Note that this transfer occurs by serially shifting data out of the MSB position of the CE register (A56.5). Each time SDL goes high to extract a character, a CRQ pulse is developed to automatically step the cursor right one character position. In this manner, one and sometimes two characters can be extracted sequentially, depending upon the status of the buffer registers.

4-23.1.5 Decodes

Several decodes are connected to the CE register. These decodes interpret the following codes:

a. A49.8, LF decode (0001010) - enables an automatic advance line function each time the operator depresses the NEW LINE key.

b. A48.8, BELL decode (0000111) - causes an audible alarm to be activated each time the BEL control code is entered into memory by the operator.

c. A58.8, ETX decode (0000011) - used to determine whether the operator has inserted an ETX into memory. When ETX is decoded, an ETXSR pulse is developed to enable the transmit circuitry.

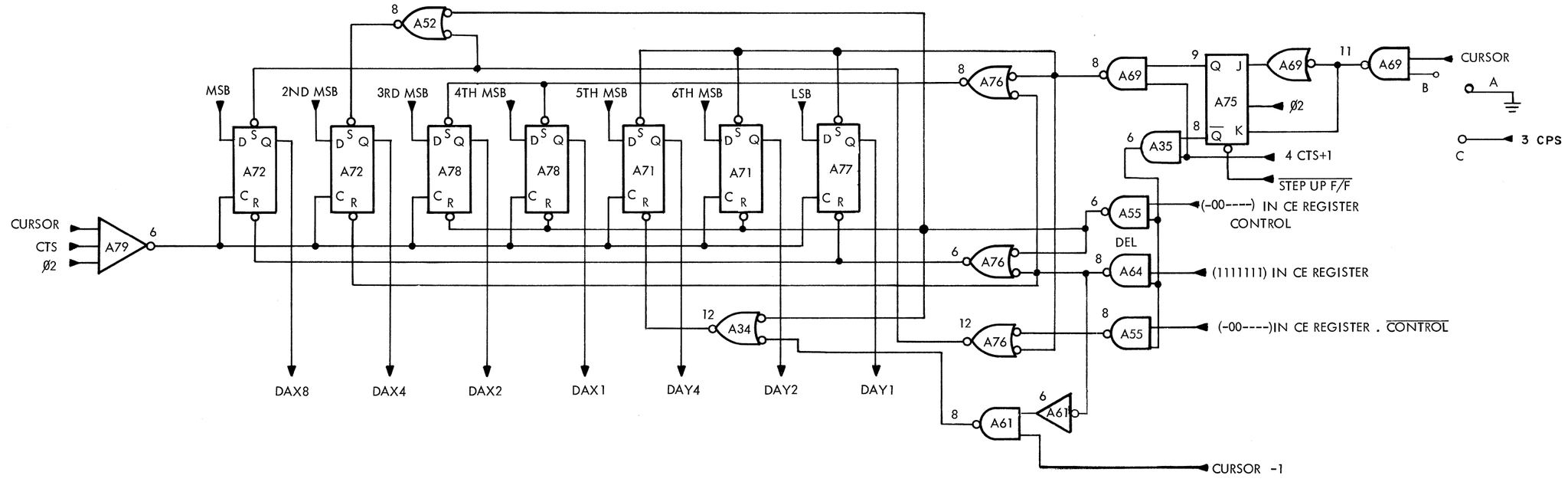
d. A64.8, DEL decode (1111111) - detects the presence of a DEL code and performs a code conversion, jamming a code of 0011110 into the CR register. Thus, each time the DEL code is shifted into the CE register, a short horizontal line is displayed on the CRT screen. This line is used as a guide to prevent operators from entering data into character slots already occupied by control codes (i.e., control codes appear as blanks on the screen).

e. A55.6, Control Code Decode (-00----) - When a control code is shifted into the character entry register, a blank character (0100000) is jammed into the CR register during 4(CTS+1). This results in display of a blank character in the control code character position on the CRT screen.

f. A55.8, Control Code Decode (-00----) - detects the presence of a control code in the CE register as well as the depressed condition of the CONTROL key. When the decode is enabled in this manner, a lower case equivalent character is jammed into the character readout register during 4(CTS+1).

4-23.2 Character Readout Register

The character readout (CR) register is part of the character generation circuitry. Character codes are entered into the CR register from the CE register and held for one character time (from CTS to CTS). During this time, the monoscope beam is deflected to a specific character position on the monoscope target to produce a visual character on the CRT screen. The important fact to remember about the CR register is that the digital code held in the register determines which of 97 individual visual characters will be displayed on the screen (see figure 4-38).



DIDS 68-537

Figure 4-38. Character Readout Register, Logic Diagram

When a character code is entered into the CE register from any of the input sources, a complete 7-bit code is available for transfer during CTS. The code is coupled from the set output of each CE register and applied in parallel to the input of each flip-flop of the CR register. During 2CTS, the digital code held in the CE register is clocked into the CR register. From the CR register, the 7-bit code is divided into two segments consisting of one 4-bit segment and one 3-bit segment. These segments are coupled to the Monoscope Deflection Amplifier (A3) and direct the monoscope beam to a specific character on the monoscope target.

In addition to accepting digital codes from the CE register, the CR register may be jammed to contain specific codes when special characters are decoded in the CE register. These alternate codes are described as follows:

a. Cursor Character - The cursor symbol displayed on the CRT screen is optionally the symbol ☰ or ⌋ . The ⌋ cursor symbol is developed on the video amplifier board when the cursor bit appears in the cursor-located flip-flop. The ☰ cursor symbol is developed by directing the monoscope beam to the cursor character position on the monoscope target. This is accomplished in the following manner:

When the ☰ cursor symbol is employed, the symbol is alternately displayed instead of the character with which it is associated. This requires connecting a wire between terminals B and C on the display logic board. The 3-Hz pulse recurs once every 0.333 ms or 20 times/frame, while the cursor appears in the CE register only once/frame. When the cursor and the 3-Hz pulse appear in coincidence, NAND-gate A69.11 is enabled and flip-flop A75.9 is set on the following phase 2 pulse. This jams the cursor code into the CR register so that the cursor symbol (☰) is displayed instead of the character associated with the cursor. Due to the random nature of the cursor [a 1.6-μs pulse occurring once every 16 ms and a 3-Hz pulse (0.333 ms) occurring in coincidence], the character code is displayed several times as compared to each time the cursor is displayed. The high refresh rate of 63 Hz, however, produces a visual effect of the two characters alternating on the screen.

b. DEL Character - When the delay line is erased, consecutive 1's are inserted into each of the 1040 character positions. These characters exist in the delay line until other codes are entered to replace them. Each time a DEL character (1111111) appears in the CE register, a code conversion is enabled through the DEL decode A64.8.

When the DEL decode is enabled, the code 1111111 (shifted into the CR register during 2CTS) is code converted by jamming certain CR register flip-flops set or reset. This produces a code of 0011110 which shifts the monoscope beam to an isolated character at the edge of the target. This character, a short underline (_), marks the position of each unused character space on the CRT screen.

c. Control Codes - When any control code is shifted into the CE register, the status of the register flip-flops during CTS+1 is (-00----) [this corresponds to a character of (00-----) during CTS]. When a control code is detected in the CE register, a space character is jammed into the register by NAND-gate decode A55.6. When the operator depresses the CONTROL key, all control codes circulating in memory appear on the CRT screen as their lower case equivalent characters. This is accomplished by NAND-gate decode A55.8 which jams set the two MSB positions of the CR register. Since the CONTROL key is normally depressed for longer than the frame time (16 ms), all control codes contained in memory are code converted in this manner.

4-23.3 Display Functions

In addition to enabling the generation of visual characters on the CRT screen, circuits contained on the display logic board enable various edit and cursor control functions to be performed. These functions are listed below and described in the following text:

Step-Right

Step-Left

Advance Line

Cursor Reset

Erase Line

Erase Message

Step-Down

Step-Up

Insert Character

Insert Line

Delete Character

Delete Line

4-23.3.1 Display Functions Clock

The various operations performed by the display logic circuitry are controlled by the special timing circuit shown in figure 4-39. The output of the display functions clock, PB3, is connected to the clock input of each edit or cursor control flip-flop. The PB3 clock pulse essentially consists of one of the following:

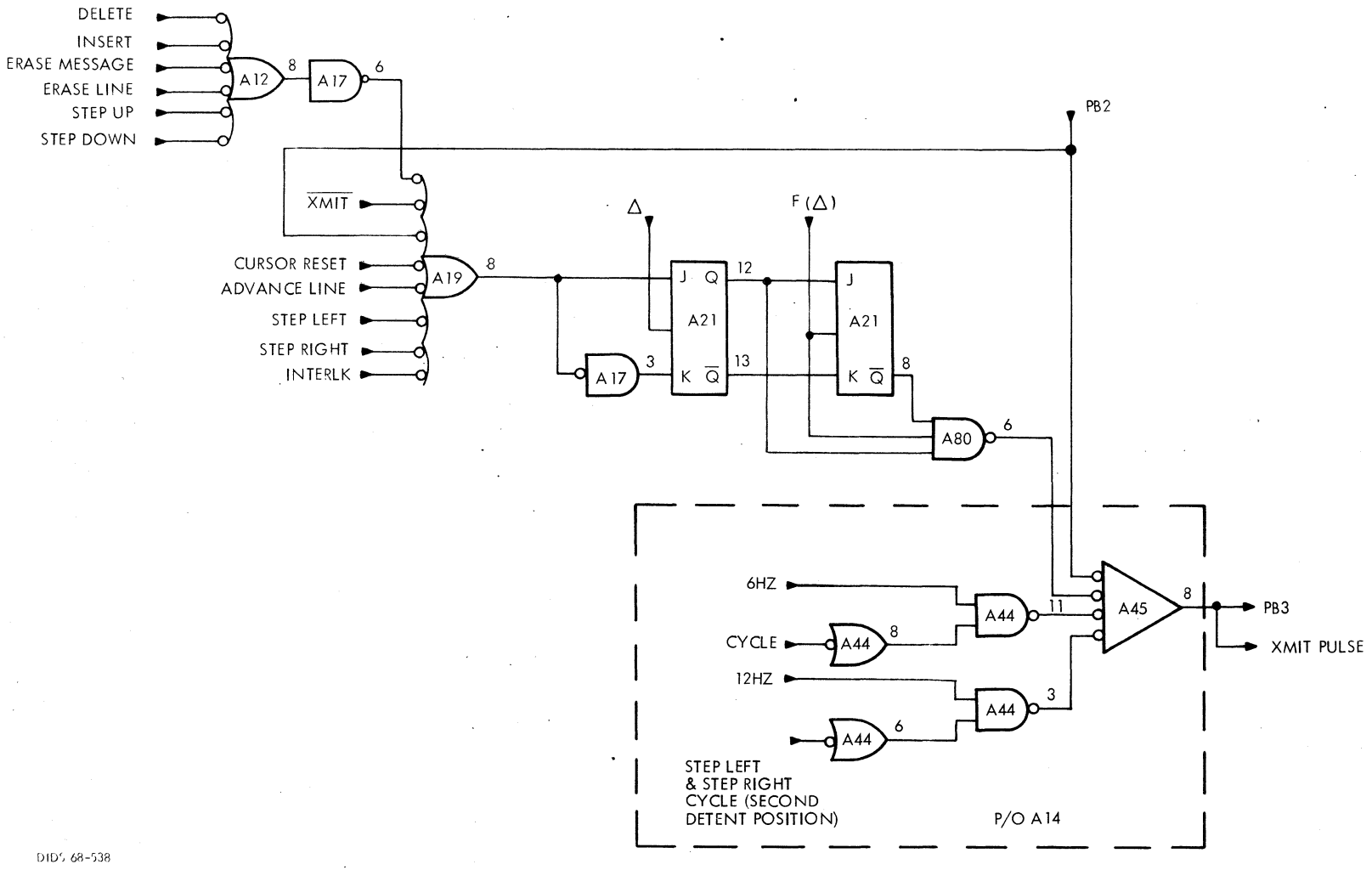


Figure 4-39. Display Functions Control, Logic Diagram

a. The first frame pulse [F(Δ)] which occurs after the depression of a character or function key. This pulse is developed by the circuit connected to NAND-gate A80.6.

b. A 6-Hz continuous clock. This output is coupled from NAND-gate A44.11 and is present when any function key and the CYCLE key are depressed simultaneously.

c. A 12-Hz continuous clock. This output is coupled from NAND-gate A44.3 and is present when either the step right (→) or step left (←) keys are depressed to the second detent position.

Normally, the PB3 clock is developed by enabling NAND-gate A80.6 during the first F(Δ) which occurs after key depression. In the circuit quiescent state, A21.12 is low and A21.8 is high. When the operator depresses any key on the keyboard, the output of A19.8 is high for as long as the key is held depressed. From 0 to 1.1 ms after key depression, a first word of line (Δ) pulse clocks A21.12 high to enable the second input of A80.6.

On the leading edge of the next F(Δ) (from 0 to 16 ms later) A80.6 is enabled and FΔ is gated through as PB3. The trailing edge of F(Δ) sets A21.8 to disable A80.6. Thus one, and only one clock pulse is generated in this manner. This pulse sets the function flip-flop associated with the particular key and causes the character entry, edit, or cursor control function to be performed.

If the operator holds the key depressed, both A21.12 and A21.8 remain set and A80.6 is inhibited. Thus a second PB3 clock pulse is produced until the operator releases the key before the character entry, edit, or cursor control function can be repeated.

To cycle a function, the CYCLE key must be held depressed in conjunction with a character or function key. Depressing the CYCLE key enables PB3 clock pulses at a 6-Hz rate to be gated through NAND-gate A44.11. These pulses, in turn, enable the repetition of the character entry, edit, or cursor control function without alternately releasing and depressing the applicable key.

The step-right and step-left cycle works in a similar manner. When either the step left (←) or step right (→) key is depressed to its second detent position, a constant low is applied to the input of A44.6. The inverted output of A44.6 is combined with 12-Hz clock pulses to develop a 12-Hz PB3 output. Since the step-left or step-right key must be held depressed to enable A44.3, the other keyboard keys are 'locked out' and are therefore not affected by the 12-Hz PB3 pulses.

4-23.3.2 Step-Right Function

The step-right cursor control function moves the cursor one character position to the right. The visible effect of step-right is to move the cursor (☰ or ⌋) one character position further from the left side of the CRT screen. In memory, step-right causes the cursor to appear in the CE register 13 μs later than it had prior to the step right function (see figure 4-40).

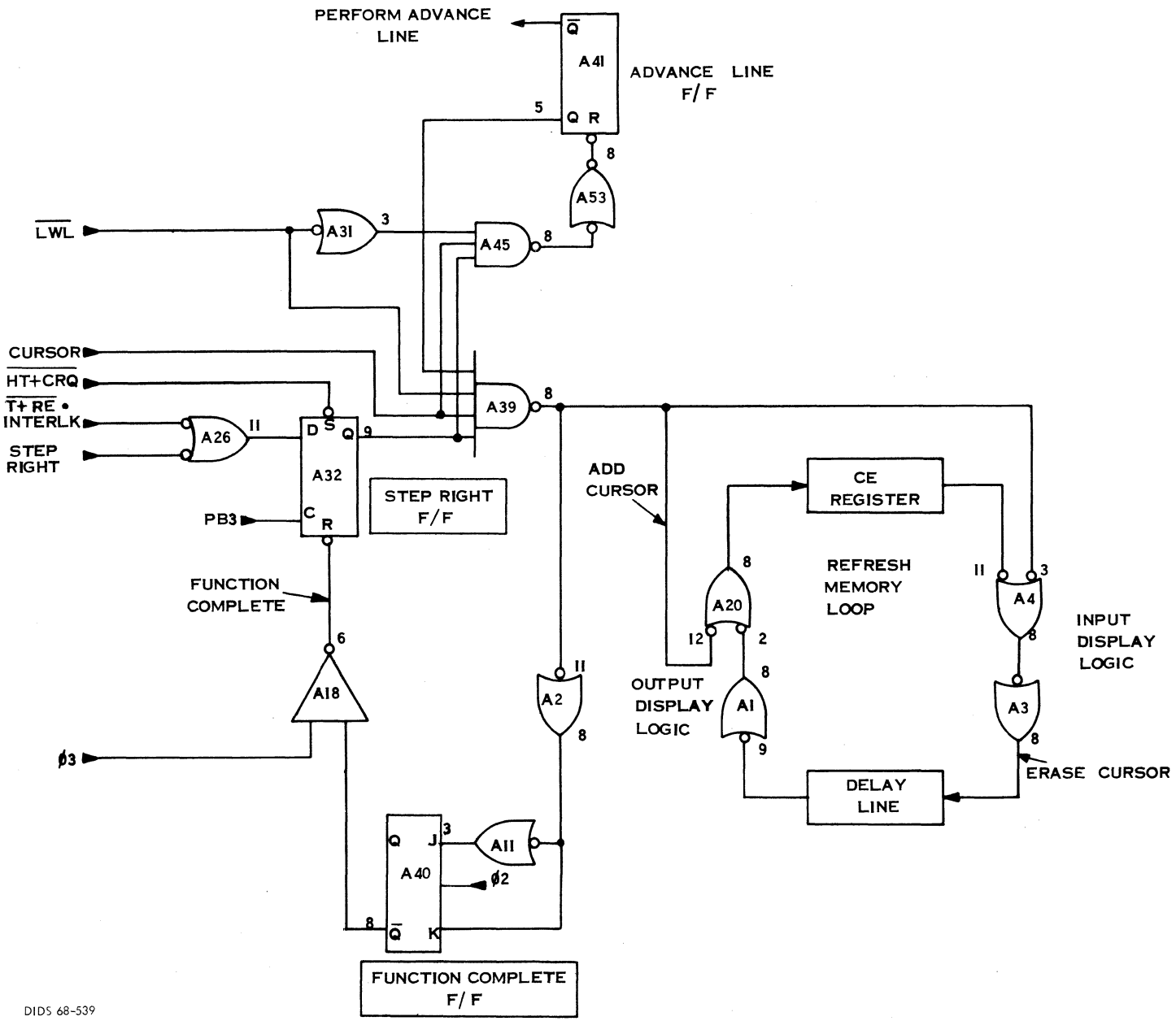


Figure 4-40. Step Right Function, Logic Diagram

The step-right function is performed each time one of the following occurs:

a. The step-right (→) key is depressed

b. A horizontal tab ($\overline{HT}$) control code is received from the CPU without being preceded by an ESC code

c. Any key capable of producing a digital code is depressed and data is entered into memory (INTERLK)

d. A character is read into or out of memory by SDL ($\overline{CRQ}$)

To perform a step-right function, the cursor is located in memory by sensing its presence in the cursor-located flip-flop of the CE register. When the cursor is found, it is erased and then reinserted into memory at the entrance to the CE register. The combined effect of these two operations is to delay the cursor by one character time. The step-right function is described below.

When the step-right (→) key or any key capable of producing a digital code is depressed, the input to step-right flip-flop A32.9 goes high. PB3, which occurs from 0 to 16 ms later, sets A32.9 high to enable one input to NAND-gates A39.8 and A45.8. When the cursor appears in the CE register and is not attached to the last character of the line, NAND-gate A39.8 is enabled. The output of A39.8 (a low) is applied to A4.8 of the input display logic which places a low at the entrance to the delay line. Since this low is in coincidence with the cursor, the cursor is erased. Simultaneously, a high is applied to the entrance of the CE register and the reset input of the function complete flip-flop. During 2CTS, this high is clocked into the MSB flip-flop of the CE register as the cursor and the function complete flip-flop is clocked to reset. During the following phase time (3CTS+1), Function Complete jams A32.9 reset to disable the function.

If the cursor is attached to the last character of the line, a step-right function automatically advances the cursor to the first character position of the next line. $\overline{LWL}$, which appears in coincidence with the cursor, inhibits NAND-gate A39.8 and enables NAND-gate A45.8. This sets the advance-line flip-flop and causes an advance-line function (paragraph 4-23.3.4) to be accomplished .

As shown in figure 4-40, the step-right function is also performed each time an HT code is received from the CPU ($\overline{HT}$) or each time a character is shifted into or out of the delay line by SDL ($\overline{CRQ}$). However, since these are jam inputs, the step-right function is performed without the use of the PB3 clock pulse.

4-23.3.3 Step-Left Function

The step-left cursor control function moves the cursor one character position to the left. The visible effect of step left is to move the cursor one character position closer to the left of the CRT screen. In memory, step left advances the cursor by one character time, causing it to appear in the CE register 13 μs earlier than it had prior to the step-left function (see figure 4-41).

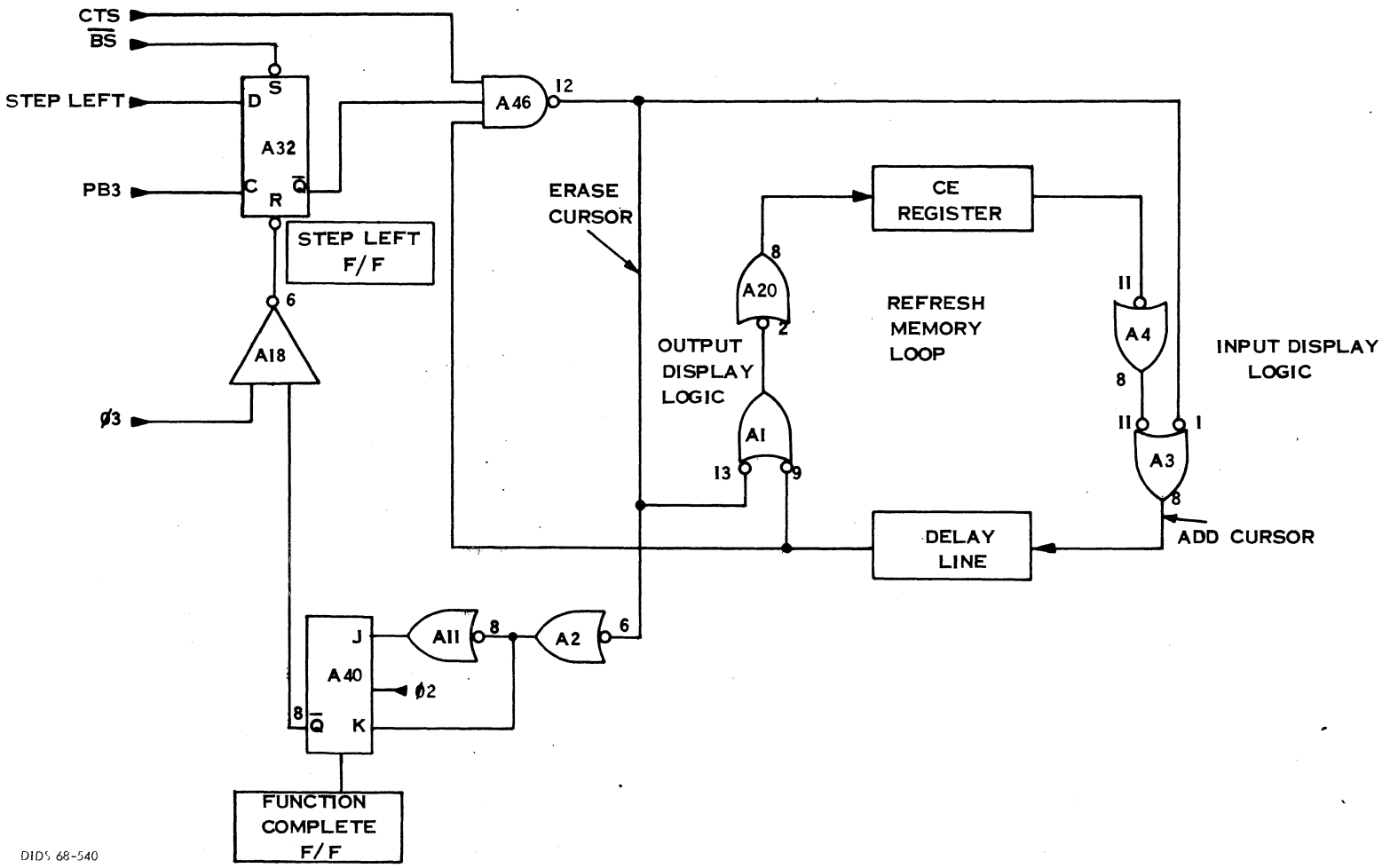


Figure 4-41. Step Left Function, Logic Diagram

The step-left function is performed each time the step-left (←) key is depressed or each time a BS control code is received from the CPU without being preceded by an ESC code.

To perform a step-left function, the cursor is located in memory by examining the output of the delay line during CTS. (Remember that the cursor is the only bit in memory that is high during CTS.) Once located, the cursor is erased before entering the CE register and inserted at the output of the CE register. In essence, the cursor bypasses the shift through the CE register. The time 'saved' in this manner allows the cursor to appear 13 μs earlier than it had previously.

When the step left (←) key is depressed, the input to step-left flip-flop A32.6 goes low. PB3, which occurs from 0 to 16 ms later, sets A32.6 high to enable one input to NAND-gate A46.12. From 0 to 16 ms later, the cursor appears at the delay line output during CTS. The output of A46.12 (a low) is applied to A3.8 of the input display logic and A1.8 of the output display logic. This places a high at the entrance to the delay line during CTS (the cursor) and erases the high previously present at the CE register input. On the trailing edge of 2CTS, the function complete flip-flop is reset and during 3(CTS+1), the Function Complete level disables the function. The $\overline{BS}$ control code (decoded in D3) performs the same function except that the PB3 clock pulse is not required. This eliminates from 0 to 16 ms of the time normally required to accomplish the step-left function.

4-23.3.4 Advance-Line Function

The advance-line, cursor-control function moves the cursor from any character position on a particular line to the first character position of the next line. In memory, advance line causes the cursor to appear in the CE register from 104 to 1144 μs later than it had prior to the advance-line function. The two extremes occur when the cursor is associated with the last character of a line (104 μs) or with the first character of the line (1144 μs). All other character positions fall somewhere in between these two extremes (see figure 4-42).

The advance-line function is performed each time one of the following occurs:

a. The operator depresses the ADV LINE or the NEW LINE key.

b. A line feed (LF) control code is detected in D1 during transmit

c. A line feed (LF) or carriage return (CR) control code is received from the CPU without being preceded by an ESC code

d. An ETX control code is received from the CPU to terminate the receive mode (Advance Line at End of Receive Mode option)

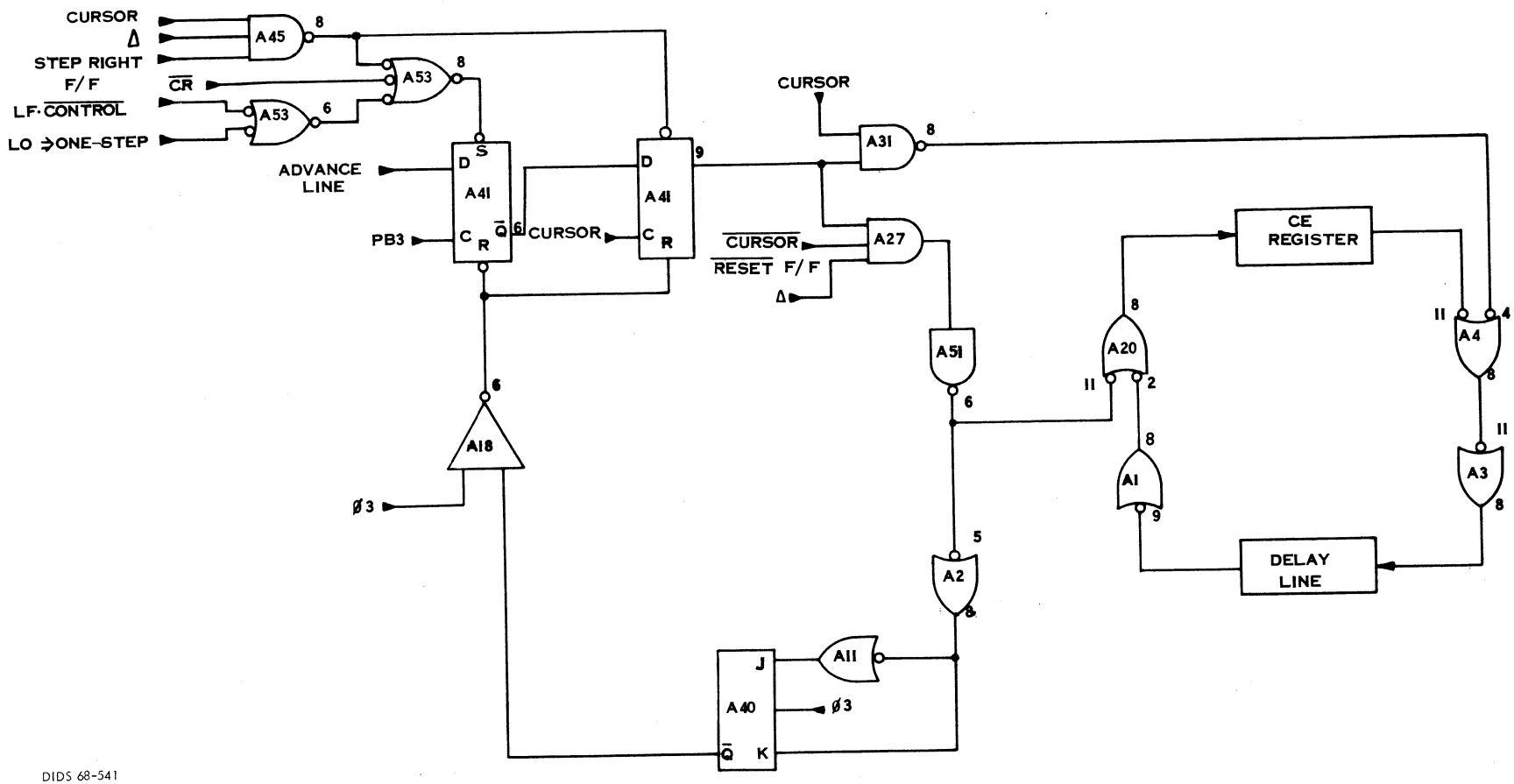


Figure 4-42. Advance Line Function, Logic Diagram

e. A step-right cursor control function is initiated when the cursor is associated with the last character of the line

f. The END key is depressed (One-step Transmit option)

To perform an advance-line function, the cursor is located in memory by sensing its presence in the cursor-located flip-flop of the CE register. When the cursor is found, it is erased before re-entering the delay line. The cursor is then reinserted at the first character position of the next line by sensing the first-word-of-line (Δ) pulse.

When the ADV LINE key is depressed, PB3 clocks flip-flop A41.6 reset during the first F(Δ) occurring after key depression. When the cursor appears in the CE register, the output of NAND-gate A31.8 goes low to erase the cursor. The circuit then idles until Δ enables AND-gate A27.6. This pulse is essentially in coincidence with the last character of retrace, therefore, one character time later it appears in the CE register attached to the first character of the line.

At the same time the cursor is inserted into the output display logic, the function-complete flip-flop is reset to develop a Function Complete pulse during 3(CTS+1). This pulse resets the advance-line function by jamming A41.6 and A41.9 low.

When the NEW LINE key is depressed, the advance-line function is performed because of a line feed code detection in the CE register. This decoded output enters through A53.6 and A53.8 to jam A41.6 high and thereby initiate the function. The conditions stated in b, c, and d cause an advance-line function when a $\overline{CR}$ pulse enters through $\overline{A53.8}$ to jam A46.6 high. When the step-right flip-flop is set, and the cursor and Δ appear in coincidence, NAND-gate A45.8 is enabled to jam A41.6 high. This circuit is responsible for automatically stepping the cursor to a new line each time the cursor is advanced to the last displayable character of a line.

4-23.3.5 Cursor Reset Function

The cursor reset cursor control function moves the cursor from wherever it appears on the CRT screen to the frame reset (first character, first line) position. In memory, this amounts to placing a low at the input to the CE register during every CTS except F(Δ). This, in turn, assures that wherever the cursor appears in memory it will be erased. When the CRT scan is at the frame reset position, F(Δ) is gated through to enter the cursor at that position (see figure 4-43).

The cursor reset function is accomplished each time one of the following occurs:

a. The operator depresses the CURSR RESET key

b. A form-feed (FF) control code is received from the CPU without being preceded by an ESC code

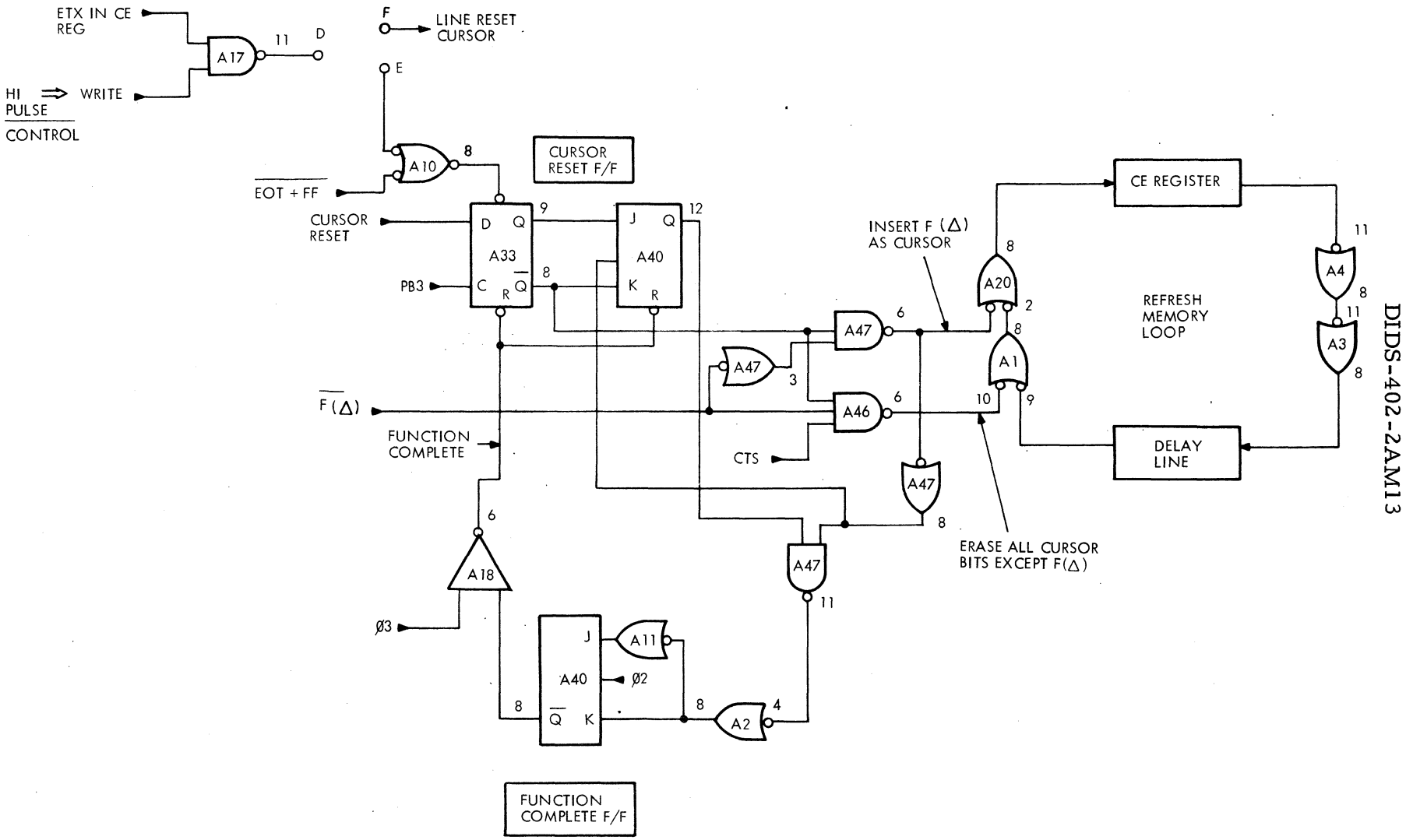


Figure 4-43. Cursor Reset Function, Logic Diagram

c. The buffer registers empty during the transmit mode (Frame Reset at End of Transmit option)

d. An ETX code is detected in the CE register when either CONTROL key is not depressed. (Optional and used to frame reset the cursor when the One Step Transmit option is used.)

When the CURSR RESET key is depressed, PB3 clocks A33.8 high to enable one input to NAND-gate A46.6. During each CTS except F(Δ) (i.e., $\overline{F(\Delta)}$ = high), A46.6 is enabled and a low is inserted into the CE register at each cursor slot. This low occurs once per character and thereby erases all cursor slots, regardless of whether or not the cursor is associated with that particular character. Thus when the cursor bit does appear at the output of the delay line, it is erased by the low applied to the input of A1.8.

When F(Δ) goes low (signifying the first character, first line position on the screen), NAND-gate A47.6 is enabled and F(Δ) is entered into the CE register as the cursor. Simultaneously, the leading edge of F(Δ) sets flip-flop A40.12 to enable NAND-gate A47.11. The output of A47.11 clocks A40.8 high during 2CTS and on the following 3(CTS+1) a Function Complete pulse is generated to reset the function. Note that this reset function is initiated by the trailing edge of F(Δ) as opposed to the previously discussed functions which were reset by the cursor.

When any of the conditions specified in b through d occur, A33.8 goes high to initiate the cursor-reset function. These conditions are described in the following text.

a. Form Feed - When a form-feed (FF) control code is detected in D3, the decoded output is coupled through A10.8 to initiate a cursor reset function. As already described, FF will not be decoded if the code was preceded in the message by an ESC code.

b. End of Transmit (option) - After a transmit sequence, the cursor may optionally be stepped to the next character position or set to the frame reset position. In either case, the end of transmission is detected by sensing a buffer register empty condition (i.e., $\overline{BB1}$, $\overline{BB2}$ and $\overline{BB3}$). After the last character is transmitted, a pulse which initiates the cursor reset function is generated.

c. One-Step Transmit (option) - When the one-step transmit option is used, the cursor is either line reset or frame reset before transmission is initiated. NAND-gate A17.11 is enabled when an ETX character is entered into the delay line by depressing the END key. (Note that depressing 'C' and CONTROL to enter ETX will not enable the gate.) The low output of A17.11 is used to either line reset (D to F) or frame reset (D to E) the cursor, depending upon the wiring option employed.

4-23.3.6 Erase-Line Function

The erase-line edit function is used to erase all the characters in a line beginning at the cursor and ending at the end of the line. In memory, the erase-line function inserts an IDLE character (1111111) into each character position beginning with the cursor and terminating at the last word of the line (Δ) (see figure 4-44).

The erase-line function is performed each time one of the following occurs:

a. When the ERASE LINE key is depressed

b. When a DC1 control code is received from the CPU without being preceded by an ESC code

c. When an ETX code is detected in D3 to terminate the receive mode (Advance Line at End of Receive Mode option).

In the circuit quiescent state, A13.9 is high and A8.12 is low. When the ERASE LINE key is depressed, A13.8 goes high to enable one input of A6.8 and simultaneously place a high at the J input of A8.12. When the cursor is shifted into the CE register, A8.12 goes high to place a high at the input to the delay line. This high is held here during the seven data bits of each character to replace each stored character with an IDLE code. During CTS, NAND-gate A16.8 is enabled to inhibit placing a high at the cursor slot of the particular character being erased. This 'erasure' continues until the last word of line (Δ) pulse enables NAND-gate A6.8 (lines 1 through 13) or F(Δ) enables NAND-gate A16.11 (line 14). When either of these conditions occurs, A40.8 goes high during 2CTS and a Function Complete pulse is generated during 3(CTS+1). The Function Complete pulse resets the circuit to its quiescent state.

The same circuit operation occurs when a DC1 control code is received from the CPU without being preceded by an ESC code or when an ETX terminator is decoded in D3 (option).

4-23.3.7 Erase-Message Function

The erase-message edit function is used to erase all characters from the cursor position to the end of the screen. In memory, the erase-message function inserts an IDLE character into each character position beginning with the cursor and terminating with the frame pulse [F(Δ)] (see figure 4-45).

The erase-message function is performed each time one of the following occurs:

a. When the ERASE MSG key is depressed

b. When a CAN control code is received from the CPU without being preceded by an ESC code

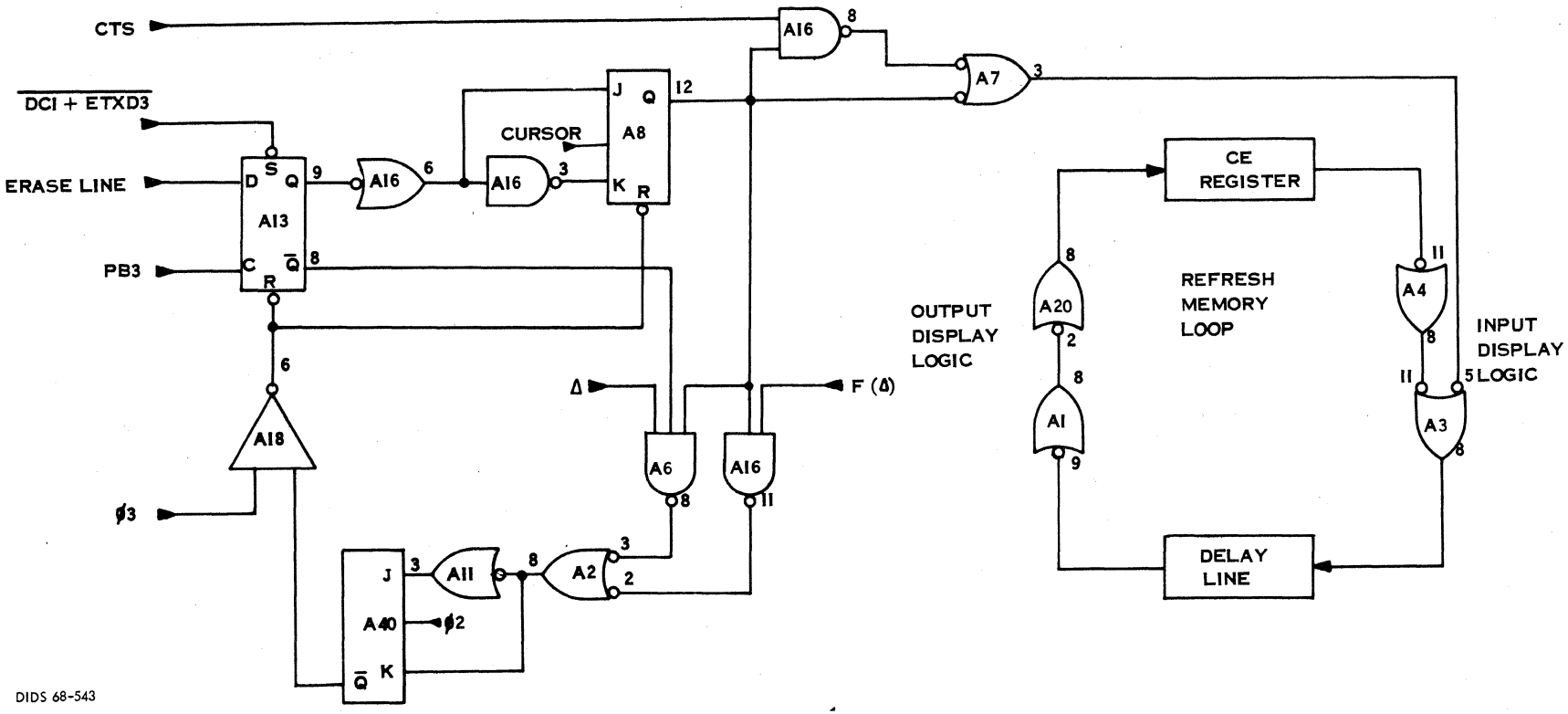


Figure 4-44. Erase Line Function, Logic Diagram

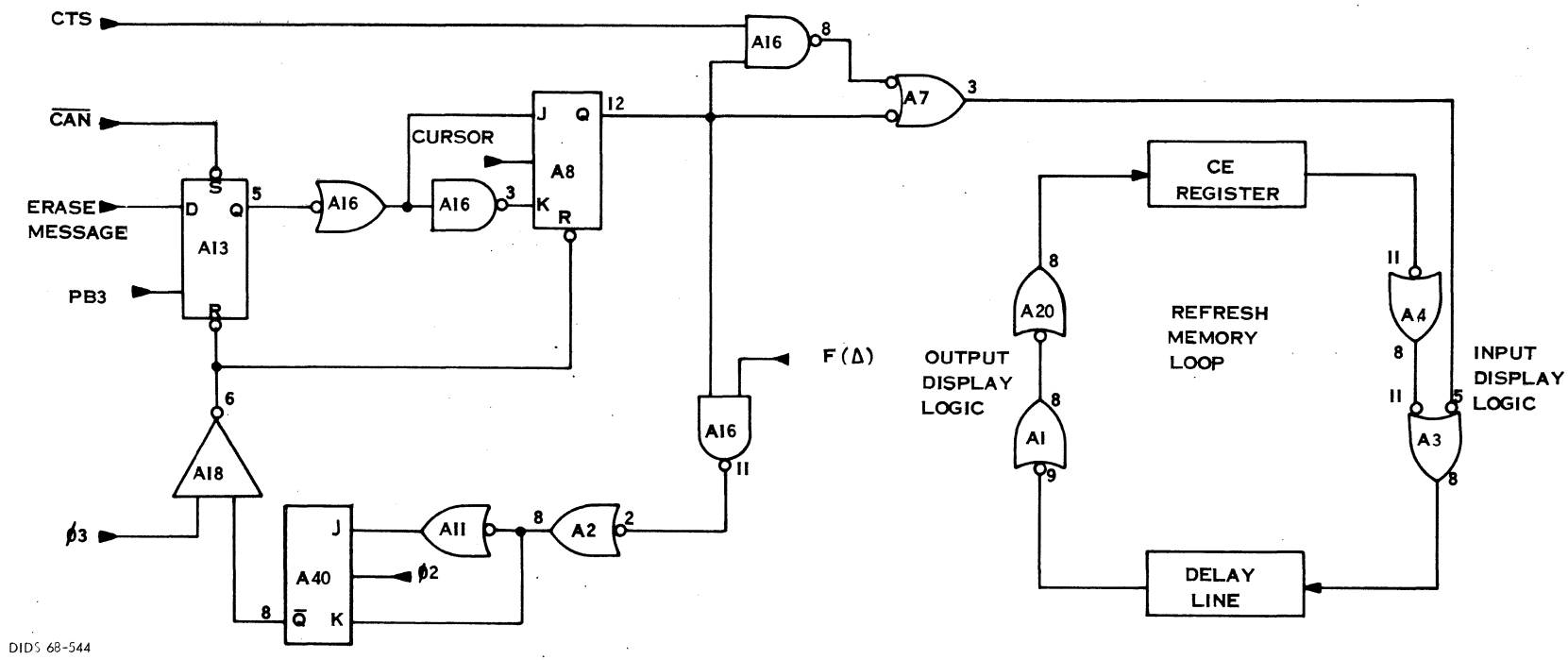


Figure 4-45. Erase Message Function, Logic Diagram

In the circuit quiescent state, A13.5 is high and A8.12 is low. When the ERASE MSG key is depressed, A13.5 goes low to place a high at the J input of A8.12. When the cursor is shifted into the CE register, A8.12 goes high to place a high at the input to the delay line. This, in turn, inserts an IDLE character during the seven bits of each character. During the cursor slot, CTS enables NAND-gate A16.8 to inhibit placing a high at the cursor slot position.

The erase-message function continues in this manner for each character in memory until F(Δ) occurs to signify the frame reset position (by now the entire screen from the cursor position on has been erased). F(Δ) enables A16.11 and during 2CTS the function complete $\overline{Q}$ output goes high. During the following phase time, 3(CTS+1) is gated through A18.6 to return the circuit to its quiescent state.

NOTE

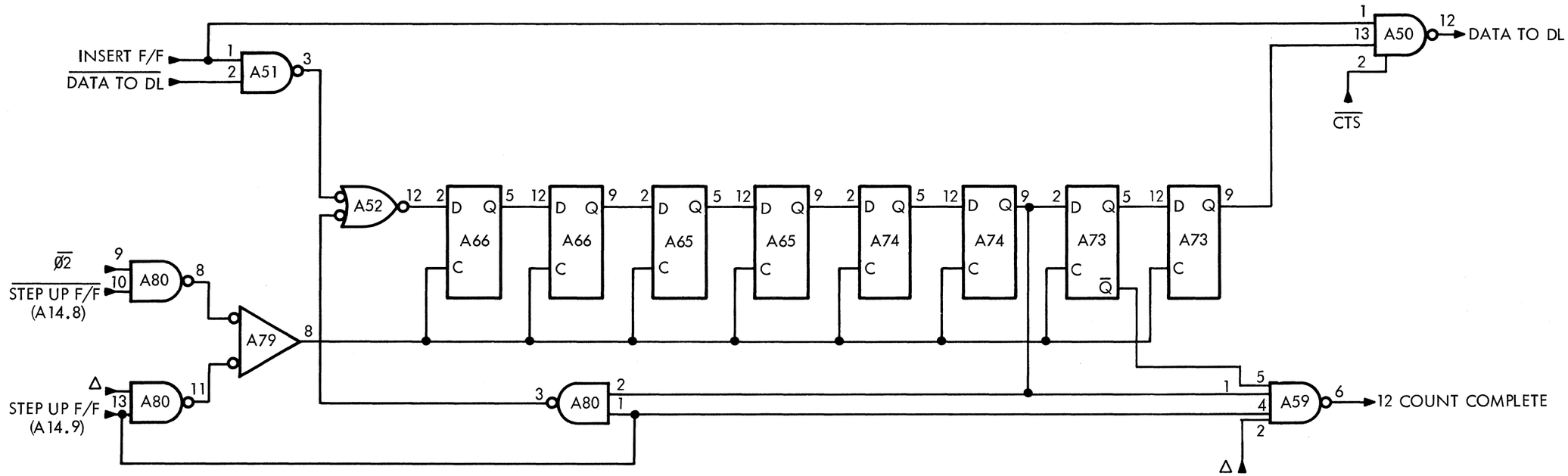
The remaining edit or cursor control functions require the assistance of auxiliary circuits in order to accomplish their functions. These circuits consist of the 12-count and insert register and the 88-count circuit. These circuits are described below so that the step-up, step-down, insert, and delete functions may be easily understood.

4-23.3.8 12-Count and Insert Register

This circuit consists of eight flip-flops and associated gates shown in figure 4-46. In the step-up function, the circuit acts as a counter and produces a 12-count output. Since the counter is clocked by Δ pulses, the decoded output corresponds to a count of 12 horizontal lines on the CRT screen. In the insert function, the circuit acts as an 8-bit register. To insert a character, this auxiliary register is connected in series with the refresh memory loop. As such, it initially releases a stored IDLE code (a 'space') which enters the delay line at the cursor position. This 'space' permits entry of another character at the cursor position. The register remains in the circuit until the function is terminated at the end of the line. Since the insert register then contains the last character of the line, the character is removed from the loop and erased from the screen.

The operation of the 12-count and insert register is described in the following text.

In the circuit quiescent state, a high is present at A52.12 due to the absence of coincident inputs to NAND-gates A51.3 and A80.3. Since the step-up flip-flop is considered to be inactive, NAND-gate A80.8 is enabled during $\overline{\phi 2}$ to produce phase 2 clock pulses for clocking the counter (register). Thus, at quiescence, each flip-flop has a high present at the Q output. For the step-up function, the 'all 1's' condition corresponds to 0 count, while the insert function uses this condition as a stored IDLE character.



DIDS 68-545

Figure 4-46. 12-Count and Insert Register, Block Diagram

4-23.3.8.1 12-Count

When the step-up flip-flop is set, a high is applied to one input of NAND-gates A80.11 and A80.3. On the rising edge of the next Δ pulse, the counter begins counting through the states shown in figure 4-47. During the 12th Δ pulse counted, 12-count decode A59.6 produces an output. This output corresponds to 12 horizontal lines on the CRT screen and is used to begin the termination of the step-up function. (An additional 88 characters are counted by 88-count to provide the remainder of the 14.9-ms delay necessary to move the cursor up one line.)

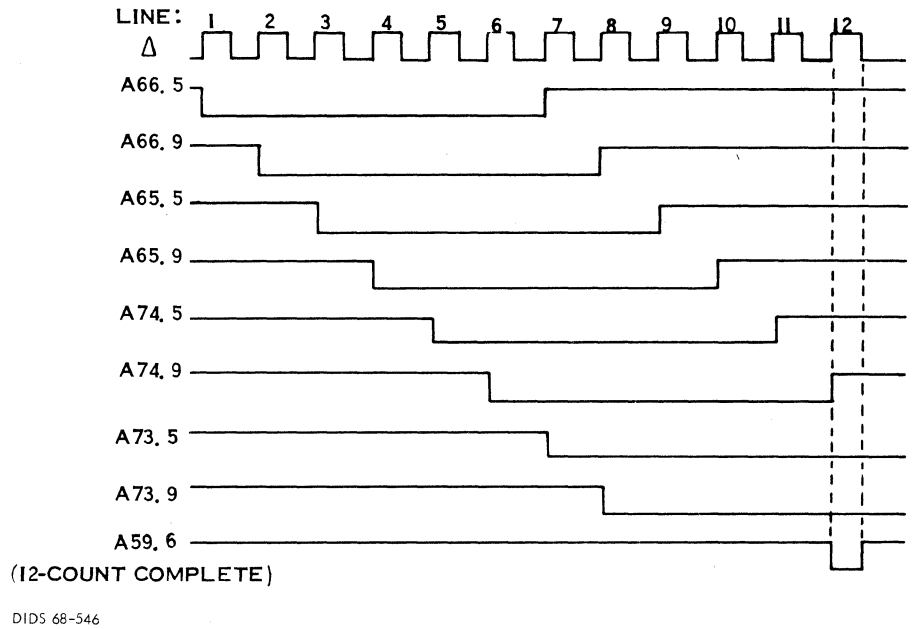


Figure 4-47. 12-Count Timing Diagram

4-23.3.8.2 Insert Register

When the insert flip-flop is set, NAND-gate A51.3 is enabled and serial data from the CE register is applied to the input of the insert register. The Ø2 clock pulses clock the memory-loop data into the register and, simultaneously, the stored IDLE character is coupled through A50.12. Since the normal refresh memory loop is interrupted at this time, all data entering the delay line does so after passing through this extra register.

The IDLE character enters the delay line in place of the character associated with the cursor. Simultaneously, the character associated with the cursor enters the insert register. Since each character of the line is delayed by one character time (because of the extra register), the character previously displayed as the last character of the line is held in the insert register when horizontal retrace occurs. Thus the last character is essentially 'dropped' from the screen and from memory.

4-23.3.9 88-Count Circuit

This circuit consists of the ripple counter and associated circuit elements shown in figure 4-48. The 88-count circuit is used to accomplish the following edit or cursor control functions:

Step-down

Step-up

Insert line

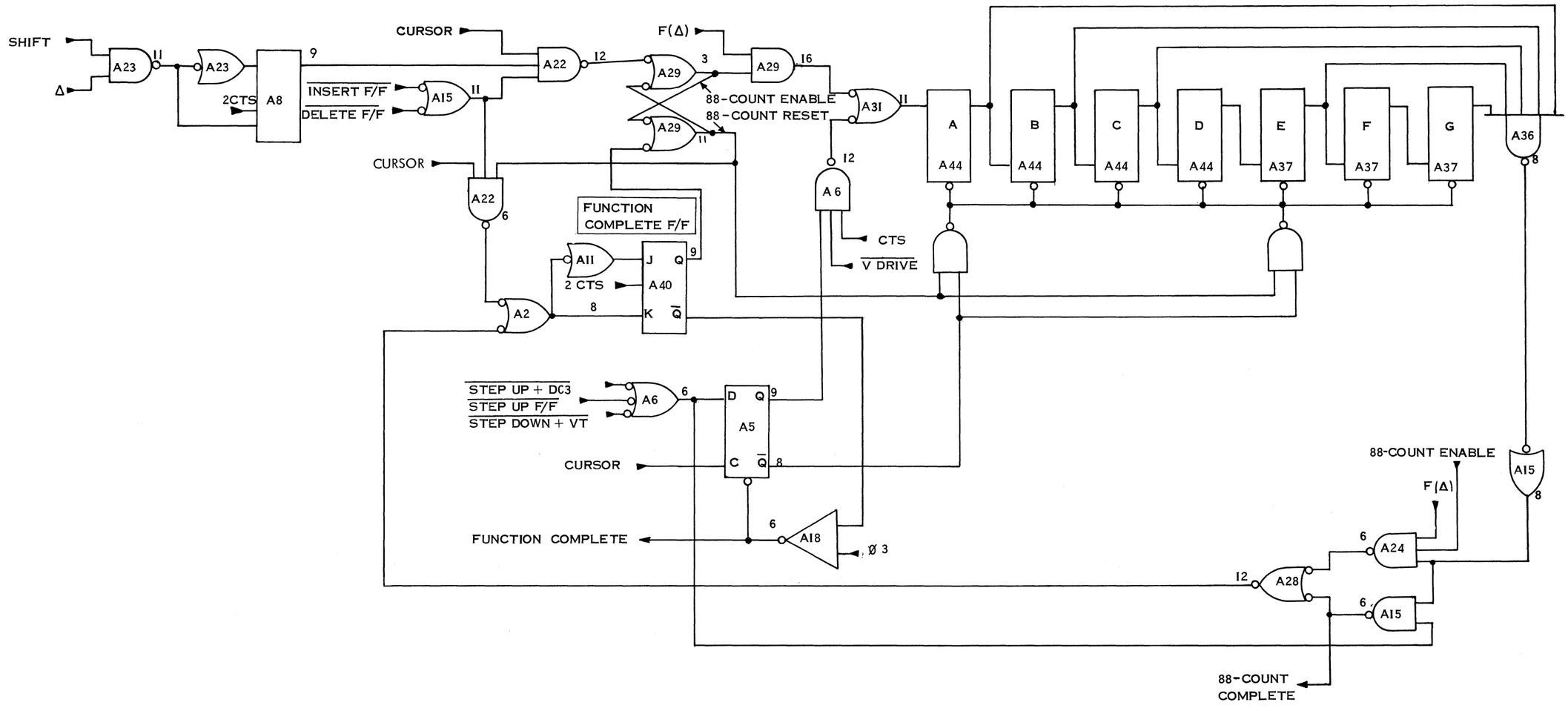
Delete line

In the step-down and step-up cursor control functions, the 88-count ripple counter is initialized and reset by enable-reset flip-flop A5.9. In the insert and delete-line edit functions, the 88-count ripple counter is initialized by the cross-connected enable-reset flip-flop formed by A29.3 and A29.11. In either case, the objective of the circuit is to count 88 clock inputs and then produce an output (88 Count Complete). The purpose of the 88 counter in each of the previously listed functions is described below.

a. Step-Down - In the step-down function, the purpose of the 88-count circuit is to count 88 character times beginning at the cursor position. This, in turn, informs the step-down circuitry when the cursor should be reinserted to complete the step-down function. When the step-down flip-flop is set as a result of depressing (↓) or receiving a VT control code from the CPU, the $\overline{\text{STEP DOWN + VT}}$ input to A6.6 goes low to produce a high at the input to A5.9. When the cursor is located in the CE register, A5.9 goes high to release the ripple counter and enable one input to A6.12. During each successive CTS pulse (except vertical retrace), the ripple counter advances in count by one character.

When 88 characters have been counted (signifying the character slot of the line immediately below the cursor), 88-count decode A36.8 is enabled. This produces an output from A15.6 which is inverted and used to simultaneously furnish an 88-Count Complete level to the step-down circuitry and set the function-complete flip-flop. The function-complete level then terminates the function by setting A5.8 high and resetting the step-down flip-flop.

b. Step-Up - The operation of 88-count during the step-up function is nearly the same as described above for the step-down function. The difference is that the 88 count is constantly recycled to count a total of 1144 CTS pulses (13-88 character lines). Each time a count of 88 is reached, the circuit is reset but because of a constant low at the input to A6.6, the counter is again enabled as soon as the cursor is once again located. When the final (13th) count of 88 is detected by the step-up circuitry, the function is allowed to disable and return to a reset condition. Counting 13 lines of 88 characters, in conjunction with the count of 12 Δ pulses by the 12-count circuitry, enables the cursor to be inserted in the preceding line immediately above where the cursor was previously located.



DIDS 68-547

Figure 4-48. 88-Count Circuit, Logic Diagram

c. Insert or Delete Line - In the insert line function, the purpose of the 88-count ripple counter is to count 88 F(Δ) pulses. Since only one character may be inserted per frame, the insert line function requires 88 frame times to insert all 88 characters of a line.

When the SHIFT key is held depressed, Δ is gated through NAND-gate A23.11 and 2CTS clocks A8.9 high. When the INSRT (or DEL) key is depressed, the applicable flip-flop is set to enable gate A15.11. The cursor is then located to enable NAND-gate A22.12 and thereby latch A29.3 high. The output of A29.3 remains high for the duration of the function and, as such, acts as an 88-count enable level.

The 88-count ripple counter then begins counting F(Δ) pulses which occur once per frame. Simultaneously, the insert (or delete) character function is being performed once per frame by the insert (delete) edit function circuitry. At the end of 88 frame times, the insert (delete) line function is disabled by an 88-count complete level from A28.12. This level sets the function-complete circuit and enables the function to be terminated. Note that function complete latches A29.11 high to reset the ripple counter to a 0 count.

4-23.3.10 Step-Down Function

The step-down cursor-control function moves the cursor from any character position of a line to the same character position of the next line. In memory, step down consists of delaying the cursor by 88 character times (one line time) and causing it to appear in the CE register 1.144 ms later than it has prior to the initiation of the function (see figure 4-49).

To perform a step-down function, the cursor is located in memory by sensing its presence in the cursor-located flip-flop of the CE register. When the cursor is found, it is erased and then reinserted into memory after counting 88 characters. This delays the cursor by 1.144 ms and places it on the next horizontal line, immediately under where it was prior to the function.

When the step-down (↓) key is depressed, or when a VT control code is received from the CPU without being preceded by an ESC code, A5.5 goes low. The resulting high output from inverter A6.6 is applied to NAND-gates A15.3 and A15.6 and to 88-count enable-reset flip-flops A5.9 (see figure 4-48)..

When the cursor appears in the CE register, A15.3 is enabled and the cursor is erased. Simultaneously, enable-reset flip-flop A5.9 is set and the 88-count ripple counter begins counting CTS pulses. After 88 characters (CTS pulses) have been counted, 88-count complete enables NAND-gate A15.6 and the cursor is inserted into memory. The 88-count complete also enables the function-complete flip-flop during 2CTS and during the following 3(CTS+1), the step-down flip-flop is disabled.

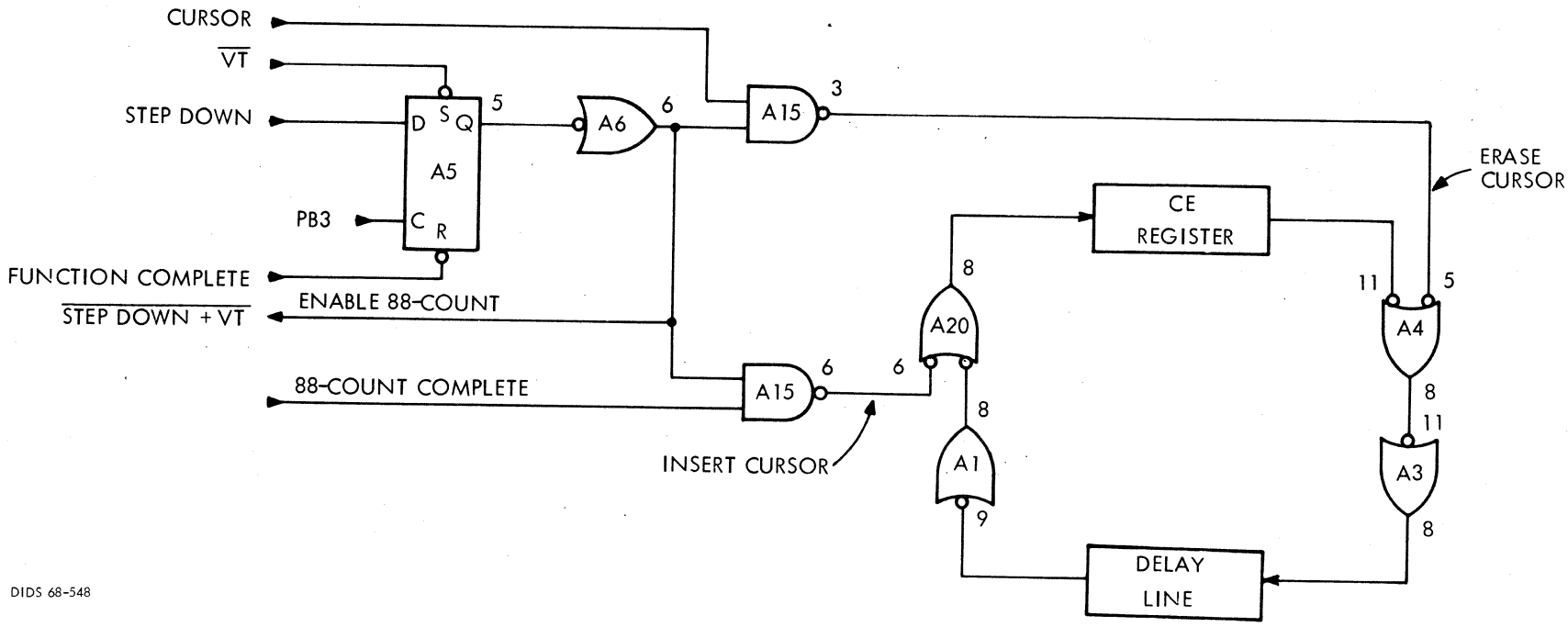


Figure 4-49. Step-Down Function, Logic Diagram

4-23.3.11 Step-Up Function

The step-up cursor control function moves the cursor from any character position of a line to the same character position of the previous line. In memory, step up causes the cursor to appear in the CE register 14.872 ms later than it had prior to initiating the step-up function. This 14.872 ms delay represents one frame time minus 88 character times (16.016 ms - 1.144 ms = 14.872 ms). After the cursor is delayed by 14.872 ms, it is reinserted into the delay line to accomplish the step-up function (see figure 4-50).

The step-up function is accomplished by using two auxiliary counters: 12 count and 88 count. The 12-count output is used to delay the cursor by 12 line times (13.728 ms). The 88-count ripple counter (which begins counting at the cursor position), counts each of the characters separating the cursor from the same character position on the next line. Each time the 88-count complete pulse occurs, the cursor is inserted into the CE register and immediately erased when the next 88 count is enabled. The counters continue in this manner until 12 count is complete (13.728 ms) followed by 88-count complete (1.44 ms). These two outputs combined represent a total delay of 14.872 ms and enable placing the cursor immediately above the cursor position prior to the function.

In the step-up circuit quiescent state, A14.5 and A14.8 are high. The $\overline{\text{STEP UP F/F}}$ output from A14.8 is applied to the 12-count circuit and enables $\overline{\emptyset 2}$ pulses to hold the counter at a constant 0 count status. When the step up (↑) key is depressed, or when a DC3 control code is received from the CPU without being preceded by an ESC code, A14.5 changes state from high to low. The level at A14.5 enables the input to 88-count enable-reset flip-flop A5.8 (see figure 4-48). When the cursor appears in the CE register, three separate actions occur: (1) NAND-gate A15.3 is enabled to erase the cursor, (2) A14.9 goes high to develop a Step-Up F/F level for starting the 12-count circuit; and (3) the 88-count circuit is enabled to begin counting the first 88 characters.

After 1.144 ms, 88 CTS pulses have been counted by 88-count. NAND-gate A15.6 is enabled to insert the cursor on the next line, immediately below its starting position. Simultaneously, the output of A15.6 is used to develop a function-complete pulse for momentarily resetting A14.9 through NAND-gate A7.11. When the cursor appears at the cursor-located flip-flop of the CE register 13 μs later, A14.9 once again goes high due to the high input from A14.6. Thus, the 12-count circuit is permitted to continue counting. (Regardless of where the cursor was located prior to initiating step up, the 12-count circuit has by this time counted one line and is progressing in time toward its second line count.)

Since A14.5 has remained low during this time, locating the cursor enabled the 88-count to begin its second count of 88 characters. When the second 88-count complete pulse enables A15.6, the cycle is repeated. To clarify the sequence of circuit operation, the numerous operations are listed in order below:

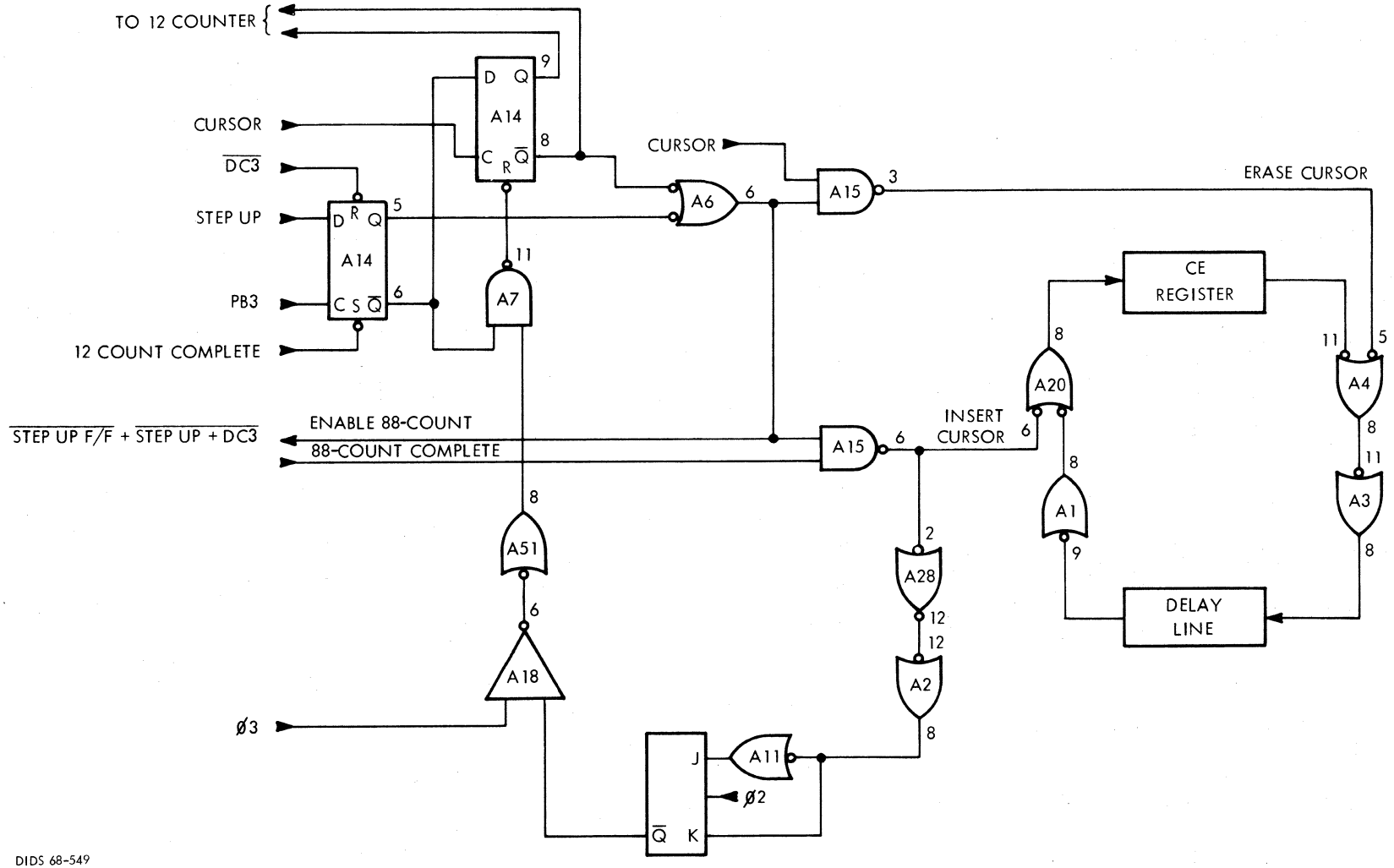


Figure 4-50. Step-Up Function, Logic Diagram

a. Set step-up flip-flop (A14.5 goes low and stays low)

b. Locate cursor

c. Erase cursor, enable 88-count, enable 12-count

d. 88-count complete

e. Insert cursor

f. Locate cursor

g. Erase cursor, enable 88-count

h. 88-count complete

i. Insert cursor

j. Repeat f, g, h, and i until 12-count is complete

The circuit continues in this manner until a 12 count is decoded by NAND-gate A59.6 (see figure 4-46). This level is applied to A14.5 and returns A14.5 to its quiescent state (A14.5 = HIGH). Thus, 12 lines have been counted by clocking the 12-count circuit with Δ pulses. Since Δ appears at the first character of line position, the 88-count complete is enabled from 0 to 1.144 ms later, depending upon the character slot location of the cursor when the function was initiated. When the 88-count complete pulse arrives from the 88-count ripple counter, A15.6 is again enabled to insert the cursor. Simultaneously, the function-complete flip-flop is enabled, but this time the function complete pulse has no effect because of the inhibited status of A7.11 (A14.6 is low). Thus, prior to locating the cursor in the CE register, A14.8 is still low and a high is applied to A15.3 and to the 88-count enable-reset flip-flop A5.9. On the rising edge of the cursor, the 13th consecutive 88 count is enabled, the cursor is erased, and A14.8 returns to its quiescent state. The function is complete as soon as the 88-count complete pulse enables A15.6 for the 13th time to insert the cursor. The cursor has now been 'stepped up' by actually stepping it down for 12 line counts and 13-88 counts.

4-23.3.12 Insert Character Function

The insert-character edit function replaces the character associated with the cursor with an Idle character (all 1's) and moves all other characters on the line to the right by one character position. In memory, insert character consists of replacing the cursor character with a previously stored Idle character. This Idle character is code converted in the CR register and appears as a short underline (_) on the CRT screen. As previously stated, this symbol is used to indicate a blank space in memory which can be used to insert a usable character. Simultaneously, all characters between the cursor and the end of the line are delayed by 13 μs due to insertion of an 'extra' 8-bit register into the memory loop. Thus, at the end of the line, the last character of the line is delayed sufficiently to place it into horizontal retrace. Since characters cannot be displayed once they enter the retrace area, the last character of the line (which is held in the extra register) is dropped (see figure 4-51).

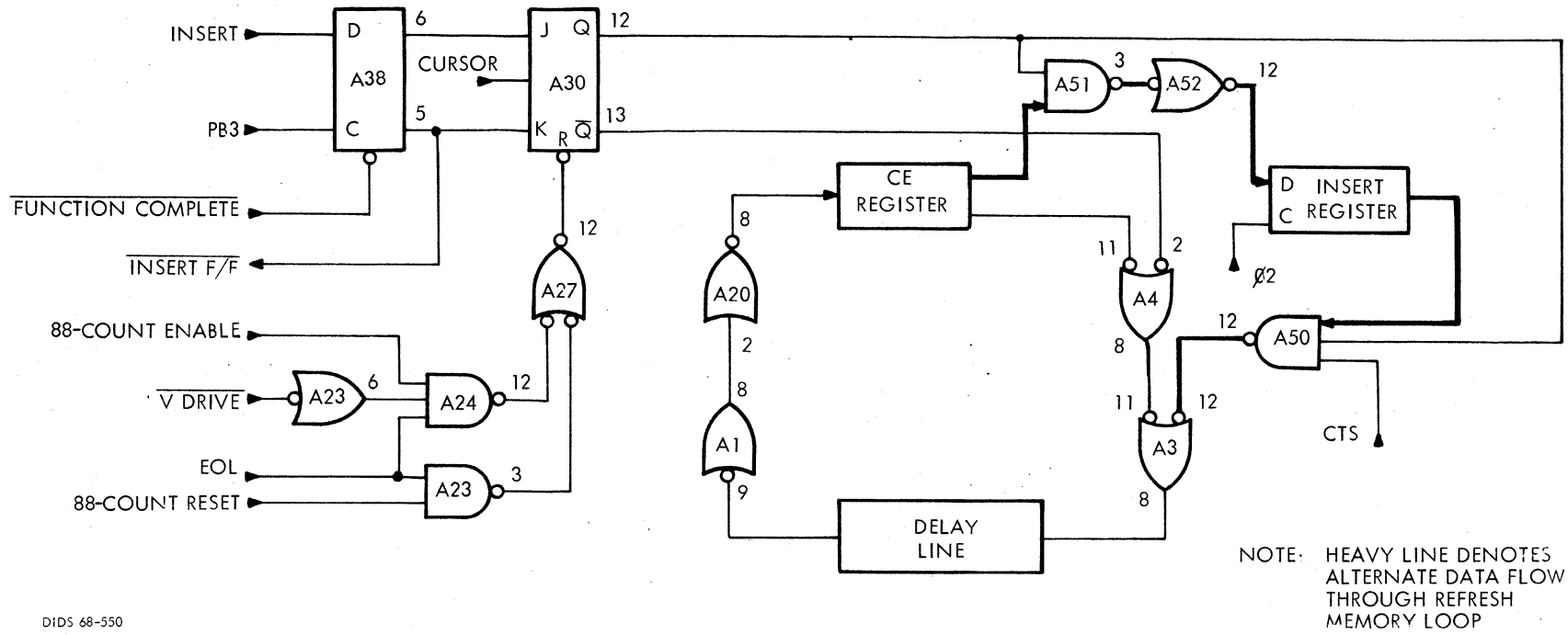


Figure 4-51. Insert Function, Logic Diagram

When the INSRT key is depressed, A38.6 goes high to place a high at the input to A30.12. Simultaneously, the low present at A38.5 is coupled to the 88-count enable-reset circuit (see figure 4-48). However, since the SHIFT key is not depressed for the insert-character edit function, NAND-gate A22.12 is not enabled and the 88-count reset level at A29.11 remains high (see figure 4-51).

The high 88-Count Reset level is applied to one input of NAND-gate A23.3. When the cursor is located in the CE register, A30.12 goes high to enable NAND-gate A51.3. This permits shifting data into the extra insert register before allowing the data to enter the delay line. Simultaneously, A30.13 interrupts the normal refresh-memory loop by placing a constant low at the input to A4.8.

The output of the insert register (which contains a previously stored Idle character) is permitted to enter the refresh-memory loop through NAND-gate A50.12. Data flow through the newly established memory loop continues in this manner, with the character codes being coupled from the CE register to the delay line via the insert register. When the end-of-line (EOL) timing pulse occurs (signifying the last character of the line), NAND-gate A23.3 is enabled to reset A30.12. When A30.12 goes low, the insert register, which contains the character previously displayed in the last character of line slot, is removed from the loop. Thus, a character-insert function inserts an IDLE character at the cursor position and moves all other characters to the right by causing them to appear in memory 13 μs later. The last character of the line is destroyed when the insert register is removed from the loop.

4-23-3.13 Insert Line Function

The insert-line edit function is similar in operation to the insert-character function except that a SHIFT key depression causes insert character to be performed 88 times. To accomplish the insert-line function, the cursor must be positioned to the first-character-of-line position before initiating the function (see figures 4-51 and 4-48).

When the INSRT key is depressed in conjunction with a constant SHIFT key depression (SHIFT LOCK), A38.5 goes low to enable one input of NAND-gate A22.12 (88-count enable circuitry). If the cursor is associated with the first character of the line (Δ), A22.12 is enabled during 2CTS. The low output is used to latch A29.3 high and thereby enable one input of NAND-gate A29.16. The 88-count circuit then begins counting up to 88. Meanwhile, A30.12 in the insert circuit is set high when the cursor appears in the CE register. This enables an insert-character function to be performed.

At the end of the last horizontal line on the screen, an EOL pulse occurs in coincidence with $\overline{\text{V DRIVE}}$ to enable A24.12. This resets A30.12 to its normally low status and disables the flow of data through the insert register. Since A38.6 is still high, a second insert-character function is enabled the next time the cursor appears in the CE register. The cursor clocks A30.12 high to simultaneously inhibit A4.8 and enable A51.3

The insert-character function is repeated in this manner, until 88 F(Δ) pulses have been counted by the 88-count ripple counter. F(Δ) is gated through NAND-gate A24.6 as 88-Count Complete to reset the function complete flip-flop. When A40.9 goes low, A29.11 is latched high to develop an 88-Count Reset level for resetting 88-count ripple counter. Simultaneously, Function Complete sets A38.5 high to return the circuit to its quiescent state. In this manner, an entire horizontal line (88 characters) is inserted, one character at a time. Each time the EOL and $\overline{\text{V DRIVE}}$ timing outputs signify the last character of the last line position, the character is destroyed. After 88 F(Δ) pulses, an entire line of Idle characters has been inserted and the last line of the screen has been destroyed.

4-23.3.14 Delete-Character Function

The delete-character edit function deletes the character associated with the cursor and moves all other characters on the line one character position to the left. In memory, the data character associated with the cursor is inhibited from entering the delay line (deleted) and the next data character is advanced by 13 μs to replace the deleted character in memory. Each successive character on the line is similarly advanced (stepped left) so that the first character of horizontal retrace (an Idle character) is stepped into the last character of line character slot (see figure 4-52).

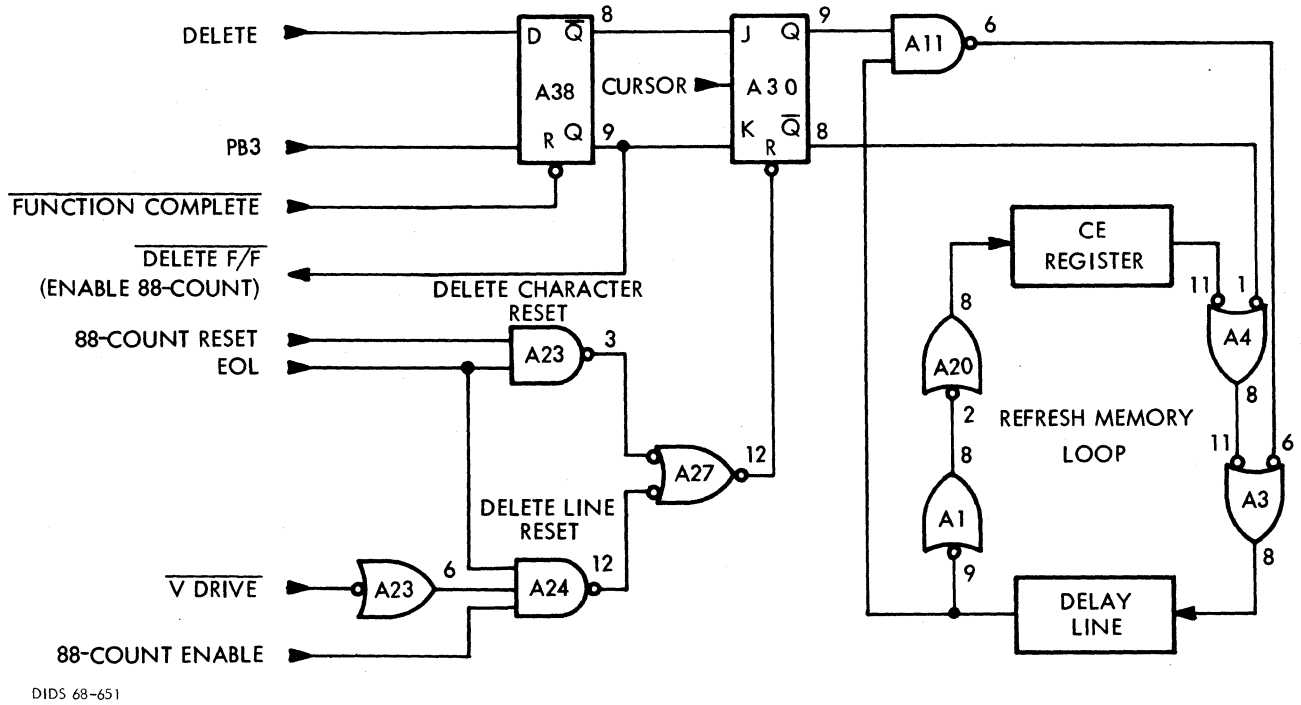


Figure 4-52. Delete Function, Logic Diagram

When the DEL key is depressed, A38.8 goes high to place a high at the input of A30.9. Simultaneously, a low is applied to the 88-count enable-reset circuit (see figure 4-48). Since it is assumed that the SHIFT key is not depressed, NAND-gate A22.12 is not enabled and the 88-Count Reset level at A29.11 remains high.

The high 88-Count Reset level is applied to one input of NAND-gate A23.3 of the delete-function reset circuitry. When the cursor is located in the CE register, the cursor bit is permitted to re-enter the delay line. On the trailing edge of the cursor, however, A30.8 goes low to inhibit the transfer of the cursor characters data bits from the CE register. Instead, NAND-gate A11.6 is enabled and the LSB of the next character in memory follows the cursor into the delay line. Thus, the 7-bit character code previously associated with the cursor is not permitted to leave the CE register (deleted) and is replaced in memory with the next 7-bit character code. All remaining characters on the line are advanced by 13 μs, since they also bypass the CE register. When the EOL pulse occurs, NAND-gate A23.3 is enabled to reset A30.9 to a low and disable the function. Since A30.8 simultaneously goes high, the normal path of data through the memory loop is once again established.

4-23.3.15 Delete-Line Function

The delete-line edit function is similar in operation to the delete-character function. The difference is that a depression of the SHIFT key causes the delete-character function to be performed 88 times. To accomplish the delete-line function, the cursor must be positioned to the first character of line position before initiating the function (see figure 4-52).

When the DEL key is depressed in conjunction with a constant SHIFT key depression (SHIFT LOCK), A38.9 goes low to enable one input to NAND-gate A22.12 of the 88-count enable-reset circuit. If the cursor is associated with the first character of the line (Δ), A22.12 is enabled during 2CTS. This low output, which is present as soon as the cursor is located, latches A29.3 high and enables NAND-gate A29.6. The 88-count circuit then begins counting F(Δ) pulses until a count of 88 is reached (88 frame times later). Meanwhile, locating the cursor in the CE register sets A30.9 (of the insert circuit) high. This enables a delete-character function to be performed.

At the end of the last horizontal line on the screen, EOL occurs in coincidence with $\overline{\text{V DRIVE}}$ to enable NAND-gate A24.12. This resets A30.9 to a low and once again enables data to flow through the refresh-memory loop in the normal manner.

Since A38.8 is still high, the next time the cursor appears in the CE register, a second delete-character function is performed. The circuit continues to operate in this manner until the 88-count ripple counter attains a frame count of 88. By this time, 88 characters have been deleted (an entire line), and all lines from the bottom of the screen to the cursor have been moved up.

The 88-Count Complete (see figure 4-48) pulse is gated through NAND-gate A24.6 and resets the function complete flip-flop during 2CTS. When A40.9 goes low, enable-reset flip-flop A29.11 is latched high to reset the ripple counter and A38.9 of the delete function circuit is reset to disable the function.

4-24 TIMING AND DISCRETE BOARD A14

Circuits contained on the timing and discrete board (Raytheon Drawing No. 407905) produce timing pulses for controlling data transfers and all other internal logical operations performed by the Display Terminal. All interface circuits are also contained on A14. These circuits provide MIL-STD-188B interface levels for transferring data or status to and from the connected CPU I/O device. The timing circuits contained on A14 are:

Master Oscillator

Minor Vertical Sweep

Phase Counter

Bit Counter

Eight-Character Counter

Character Counter

Line Counter

1200-Baud Circuitry

10-Bit Decimal Counter

Miscellaneous Circuits

- Cursor Video
- Blanking

The interface circuits contained on A14 are:

Request-to-Send Transmitter

Transmitted Data Transmitter

Clear-to-Send Receiver

Received Data Receiver

4-24.1 Master Oscillator

The master oscillator is shown schematically in Raytheon Drawing No. 407905 Transistor Q14 is connected in a modified Colpitts configuration and produces low-level oscillations of 2.4576 MHz which are limited and coupled to the base of Q15. Q15 is a saturated switch that limits the oscillator output to position excursions of the signal. The oscillator signal output is distributed to three points: the minor vertical clock input, the phase counter clock input, and the input of the phase counter decodes.

4-24.2 Minor Vertical Sweep

The minor vertical sweep circuit is illustrated in figure 4-53. The 1.3 MHz-minor vertical sweep signal, developed by divide-by-two flip-flop A26.12, is used to produce high-resolution characters 0.13 inch high on the CRT. The minor vertical sweep circuit operates in the following manner. Due to the design of T^2L logic elements, when neither the J nor K inputs of A26.12 and A19.12 are connected to an external source, both inputs appear high. Consequently, the output complements on the trailing edge of each master clock or vertical drive signal. (The vertical drive input to A43.3 is a negative going pulse that occurs once per frame during vertical retrace.)

The output of each flip-flop is connected so that the 1.3-MHz minor vertical sweep undergoes a 180-degree phase shift at the beginning of each new frame. Thus, on the 'first' frame, NAND-gate A18.6 is enabled and a 1.3-MHz output is produced. At the end of vertical retrace, A19.13 goes high and for the 'second' frame A18.8 produces 1.3-MHz clock outputs.

The reason for this phase shift is illustrated by the circuits that use the minor vertical sweep signal. In the monoscope deflection amplifier, the minor vertical sweep signal is converted to a sine wave and applied simultaneously to the diddle coil and the Y-axis deflection amplifier. At the diddle coil, the minor vertical signal 'modulates' the horizontal deflection voltage, creating an increased line height. By reversing the phase on alternate frames, the frequency of this modulating signal is effectively doubled and a sharper horizontal line developed. In the Y-axis amplifier, the minor vertical sweep signal causes the monoscope beam to 'paint' up and down over the character being scanned. Again, a phase reversal on alternate frames doubles the number of times the character symbol is 'painted', and the resulting video signal more accurately defines the character being scanned.

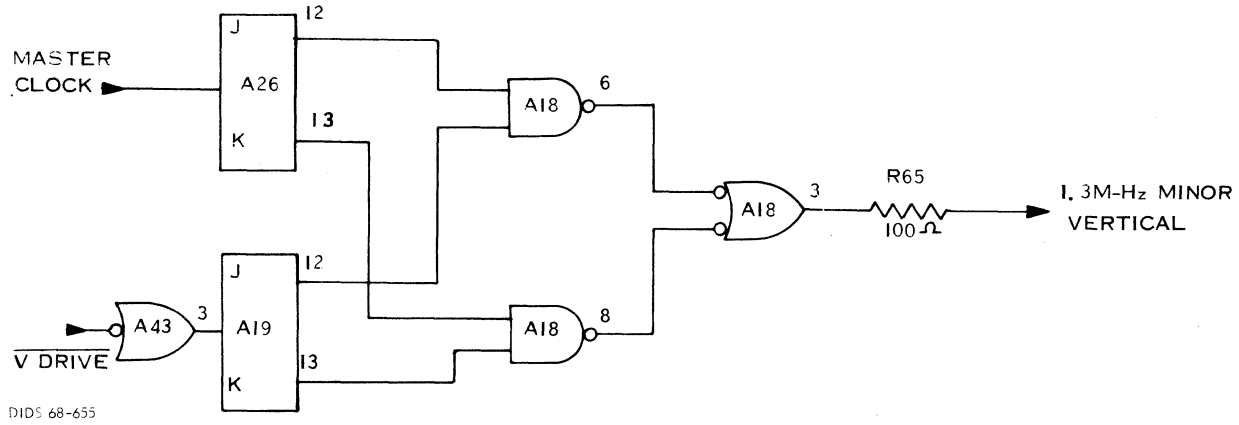


Figure 4-53. Minor Vertical Sweep, Logic Diagram

4-24.3 Phase Counter

The phase counter (figure 4-54) is a divide-by-four counter which produces four phases of the master oscillator clock. There is no provision for presetting the phase counter; therefore, during initial turn-on, any one of the four decodes may be enabled. The first $\overline{\phi 2}$ pulse is used as a reference point to toggle the bit

counter and is therefore defined as the 'last' phase time. Once the phase and bit counters are synchronized, the four phase outputs divide each bit into quarters in a sequential order of Ø3, Ø4, Ø1, and Ø2 (figure 4-55). Since Ø2 defines the last phase time of each bit, Ø3 pulses are employed to accomplish operations at the beginning of a bit time and while the Ø2 pulses accomplish all operations required at the end of the same bit time. Each of the pulse counter outputs is active (high or low) for 0.203 µs.

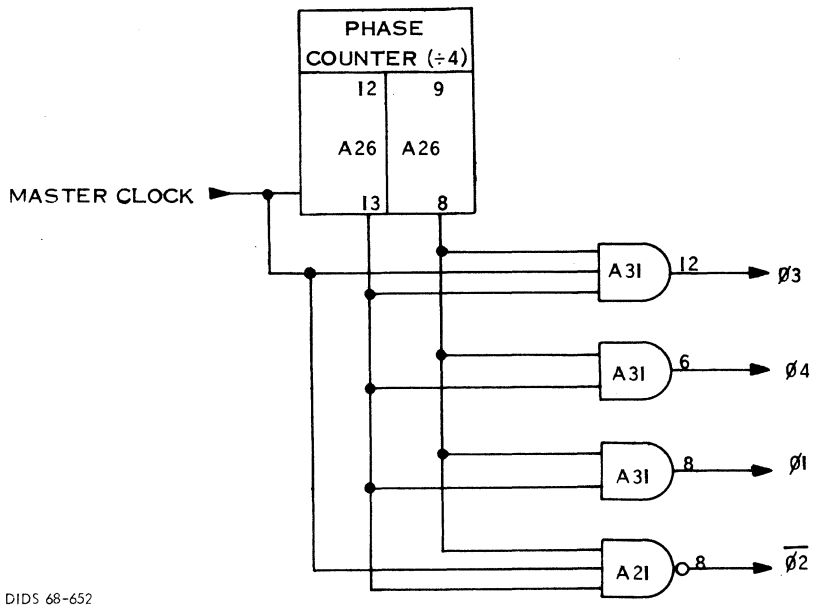


Figure 4-54. Phase Counter, Logic Diagram

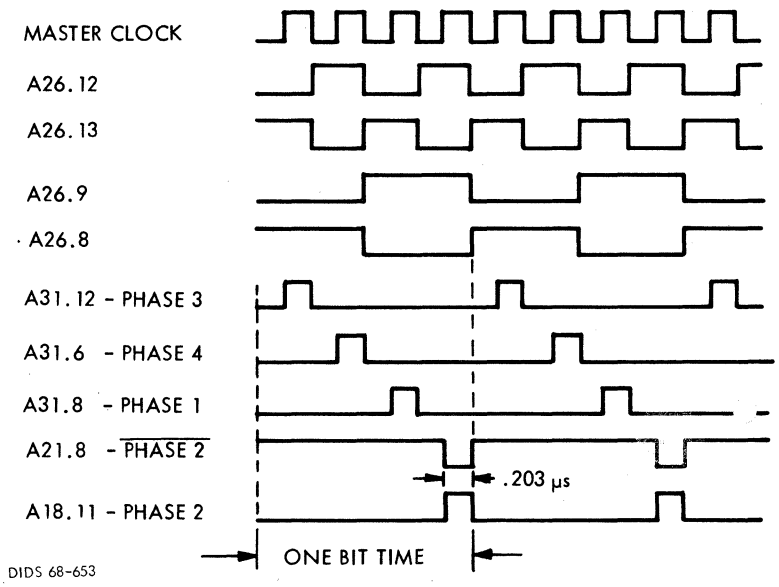


Figure 4-55. Minor Vertical Sweep and Phase Counter, Timing Diagram

4-24.4 Bit Counter

The bit counter (figure 4-56) is a divide-by-eight counter which produces three outputs: $\overline{CTS}$, $\overline{CTS+1}$, and $\overline{CTS+4} \cdot \overline{CTS+5}$. The first $\overline{\emptyset 2}$ pulse developed by the phase counter is inverted and applied to the clock inputs of A20.12 and A20.9. (The third bit counter flip-flop, A19.9, is toggled each time A20.12 goes low.)

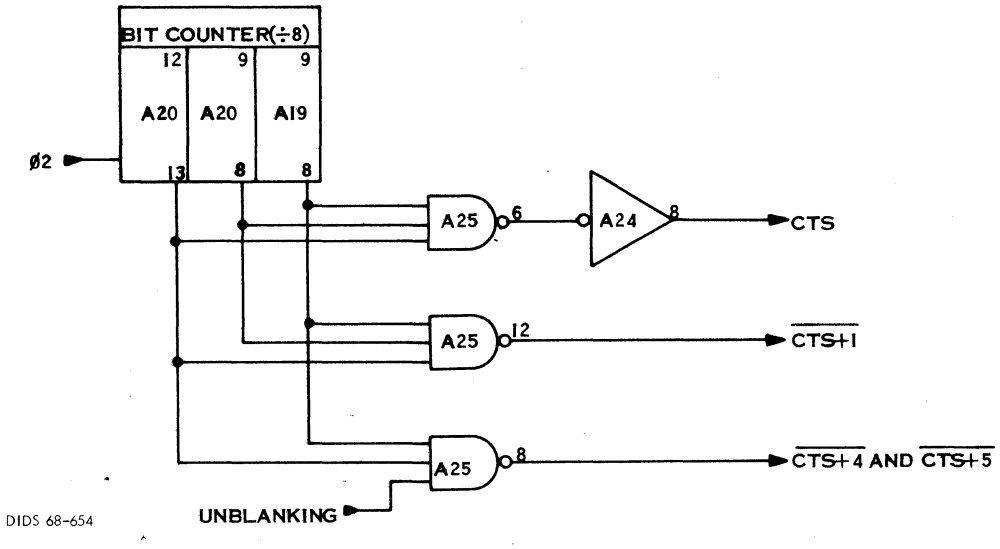


Figure 4-56. Bit Counter, Logic Diagram

Since the bit counter cannot be preset to any particular count, the first usable count occurs after from one to eight $\emptyset 2$ pulses have been developed by the phase counter. Once the phase and bit counters are synchronized, the bit-counter flip-flops cycle through the eight repetitive counts shown in figure 4-57. Although the counter cycles through eight distinct states, only three outputs are decoded. These outputs are used for the following purposes:

a. $\overline{CTS}$ - This output is defined as the first bit of a character and is in coincidence with the cursor bit in memory. Memory characters, which are eight bits in length, also contain seven data bits which are in coincidence with the remaining seven counter states. The $\overline{CTS}$ decoded output is used to perform logical operations in coincidence with the cursor bit and synchronize the remaining counters on the timing board.

b. $\overline{CTS+1}$ - This output occurs in coincidence with the LSB of a 7-bit data character. The CTS+1 output is ANDed on the timing board to produce 3(CTS+1), $\overline{3(CTS+1)}$, 1(CTS+1), and $\overline{4(CTS+1)}$ outputs. These outputs are principally employed by the buffer register logic to shift data through the buffer registers.

c. $\overline{CTS+4 \cdot CTS+5}$ - This output occurs in the middle of each data character and is used to accomplish only one function. When an Idle character is shifted into the CE register, the decode develops an output to blank the video amplifier for two additional bit times. This provides some measure of protection for the often used symbol at the edge of the monoscope which is used to develop place marker (short-underline) symbols on the screen.

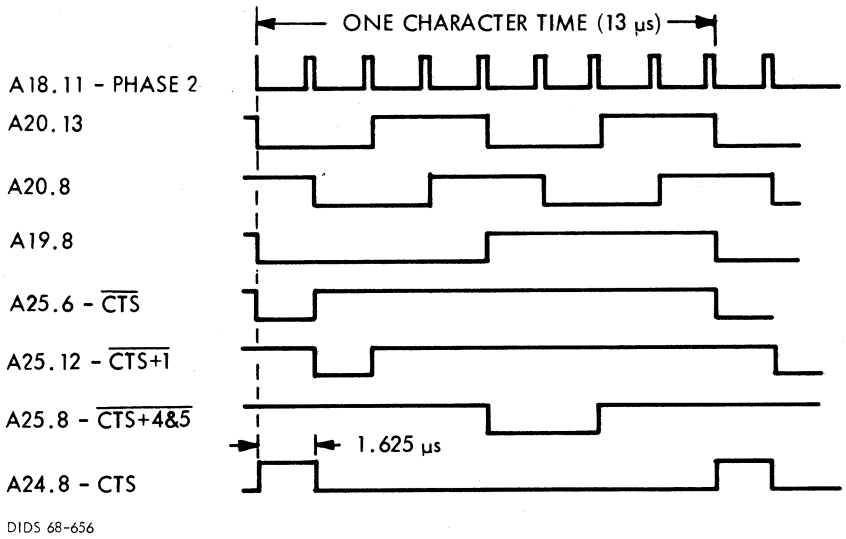


Figure 4-57. Bit Counter, Timing Diagram

4-24.5 Eight-Character Counter

The eight-character counter (figure 4-58) is a divide-by-eight counter which produces outputs corresponding to every seventh and eighth CTS developed by the bit counter. The timing diagram for the eight-character counter is shown in figure 4-59. These outputs are not used external to the timing circuits, but assist in developing important time markers such as last word of line (LWL), end of line (EOL), and first word of line (Δ). The eight-character decode produces an output once every eight character times. This output is used to clock the character counter.

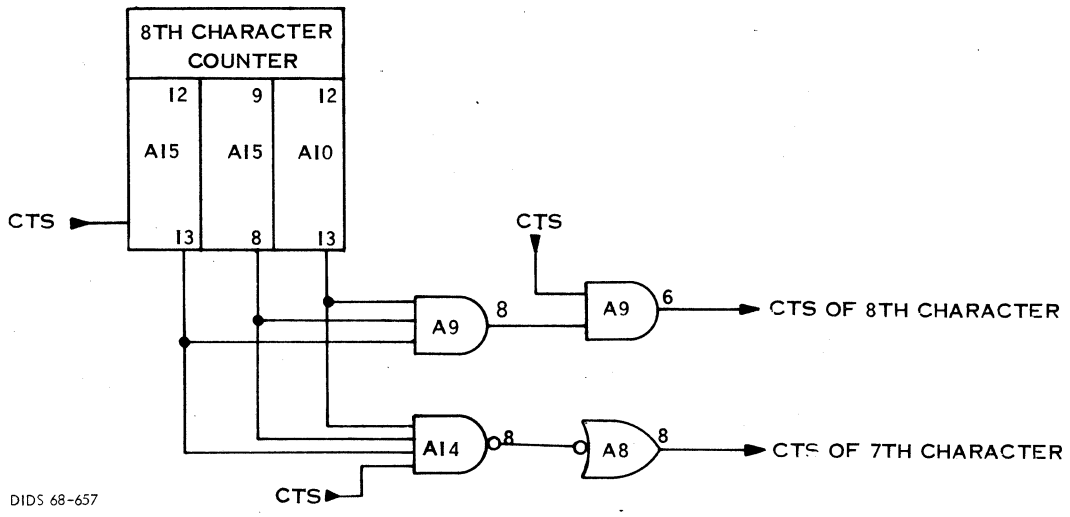


Figure 4-58. Eight-Character Counter, Logic Diagram

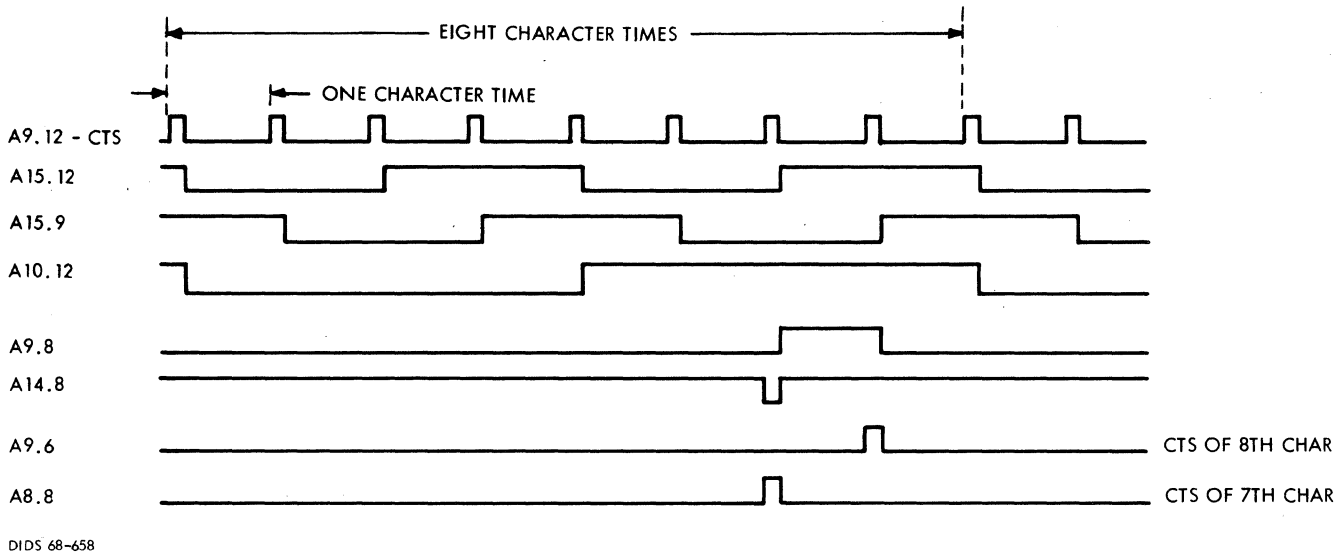


Figure 4-59. Eight-Character Counter, Timing Diagram

4-24.6 Character Counter

The character counter (figure 4-60) counts the number of characters contained on a horizontal line. The character counter decodes two general outputs. NAND-gate A8.3 produces an output pulse eight characters wide (104 μs) which is used to designate line character counts 81 through 88. AND-gate A2.8 produces an output pulse which is also eight characters wide; this pulse is high during line character count 73 through 80. Timing pulses developed by the eight-character counter and character counter decodes are described in the following text (see figures 4-60 and 4-61).

Before examining the various timing outputs, an important factor concerning visual character generation should be noted. It takes one character time (13 μs) to shift a complete character out of memory and into the CE register. At the end of this 13 μs, the character code is transferred into the CR register during 2CTS. During the following 3(CTS+1) through 2(CTS+1), the video amplifier is cut off by a blanking pulse (simultaneously, another character is being shifted into the CE register). Beginning with the trailing edge of 2(CTS+1), a sawtooth voltage developed in the monoscope deflection amplifier begins moving the monoscope beam across the character symbol to produce a video output. This scan across the character takes an additional 13 μs. Thus, from the time the character enters the CE register, 13 μs elapse before the character is displayed on the screen. This one-character-time delay is reflected in the timing circuit outputs.

For example, $\overline{\text{LWL}}$ occurs during CTS of character count 79. This pulse signifies that the last displayable character is held in the CE register. At CTS of character count 80, the last displayable character is displayed on the screen and the first retrace character is held in the CE register. Thus, at the same time the Display Terminal enters horizontal retrace, a horizontal retrace character is transferred into the CR register.

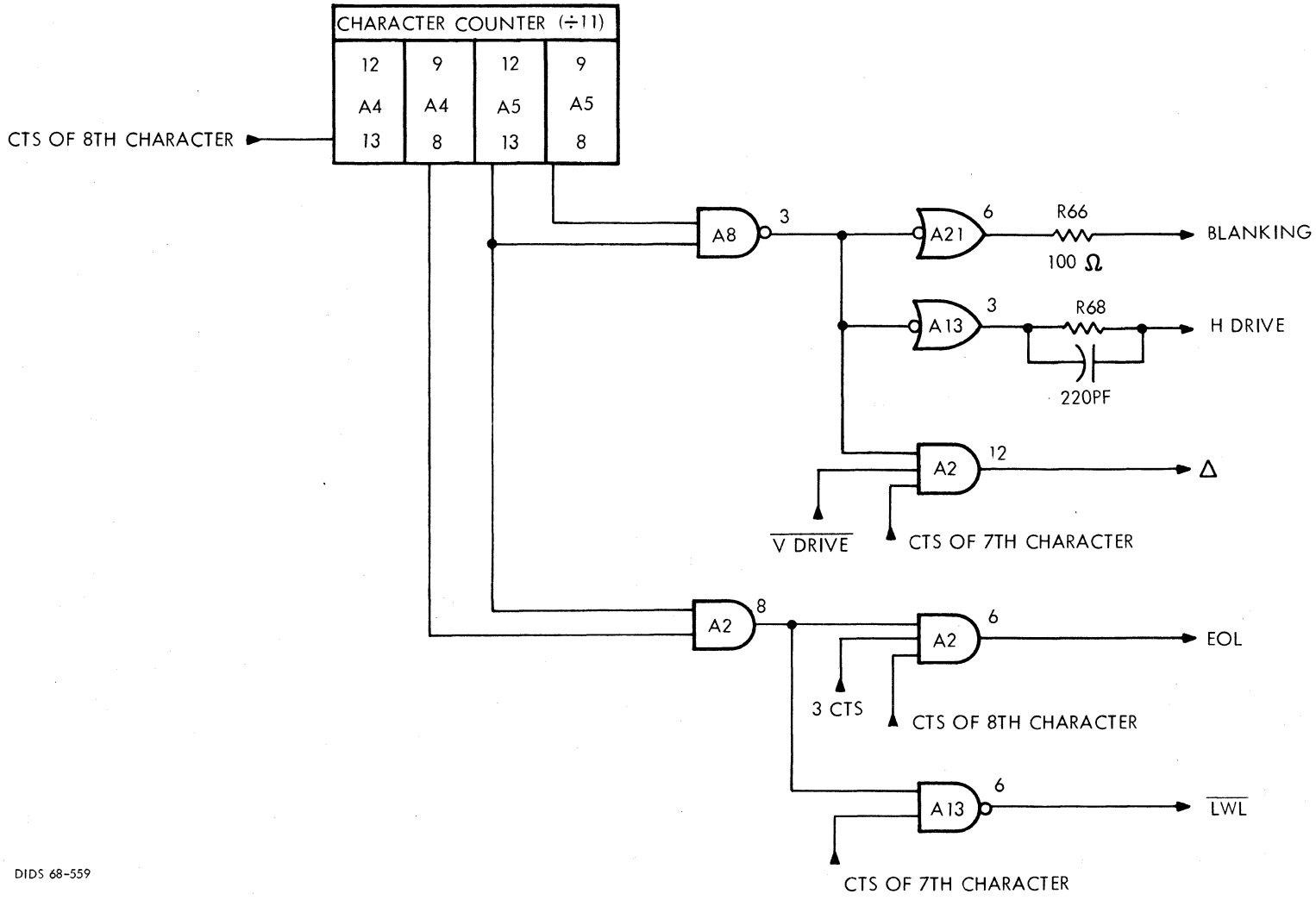


Figure 4-60. Character Counter, Logic Diagram

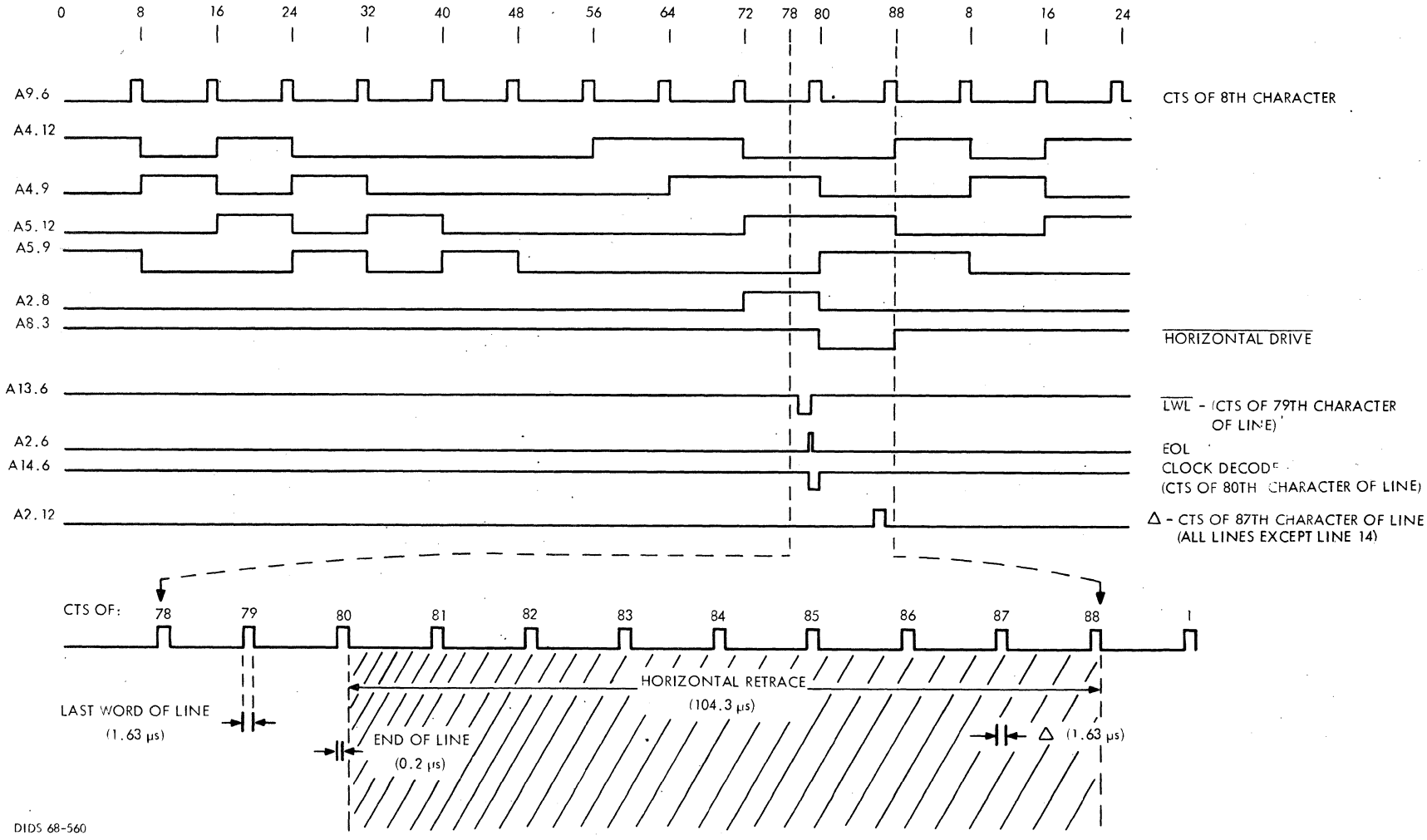


Figure 4-61. Character Counter, Timing Diagram

4-24.6.1 $\overline{\text{LWL}}$ Pulse

During CTS of the 79th character of the line, A13.6 goes low to produce a 'not' last word of line output. This pulse is coincident with the CTS pulse which shifts the last displayable character into the CR register.

The $\overline{\text{LWL}}$ pulse is used to simultaneously inhibit the step-right function and enable the advance-line function. Thus, $\overline{\text{LWL}}$ essentially prevents the keyboard or buffer register input circuits from entering any characters during retrace since an entry results in lost data.

4-24.6.2 EOL Pulse

During 3CTS of the 80th character of the line, A2.6 goes high to produce an end-of-line pulse. This pulse is employed to disable the insert and delete edit functions at the end of each horizontal line.

4-24.6.3 Horizontal Drive and Blanking

On the trailing edge of CTS of the 80th character on the line, the Display Terminal enters horizontal retrace. The horizontal retrace time is eight-characters wide (104 μs) and is developed by NAND-gate A8.3. The H DRIVE output of A13.3 is used to saturate a transistor on the horizontal deflection amplifier and allow the drive pulse to collapse. During this same time, the blanking output cuts off the video amplifier so that the return of the CRT scan to the left side of the screen will not be visible.

4-24.6.4 First Word of Line (Δ)

The Δ pulse is produced by AND-gate A2.12 during CTS of the 87th character of the line. During Δ, the last character of horizontal retrace is transferred into the CR register. During the following 3(CTS+2) to CTS of the 88th character, the retrace character would be displayed (if it were possible) and the first displayable character would be transferred into the CE register. On CTS of the 88th character, the first displayable character is shifted into the CR register and displayed during 3(CTS+2) to CTS of the 1st character.

Note that during vertical retrace, a Δ pulse is not produced when $\overline{\text{V DRIVE}}$ goes low. An F(Δ) pulse is developed in this character slot to indicate the beginning of a new frame.

4-24.7 Line Counter

The line counter (figure 4-62) counts the number of horizontal lines per frame. There are 13 displayable lines and an extra 88-character line (line 14) which is used for vertical retrace. The line counter is clocked by a pulse during CTS of the 80th character of each line which is developed by the character counter.

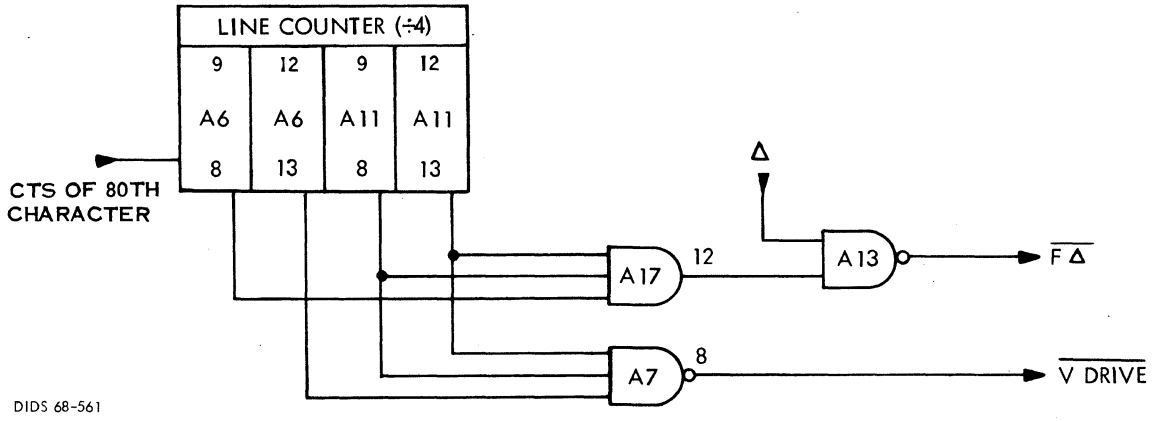


Figure 4-62. Line Counter, Logic Diagram

NAND-gate A7.8 is enabled after CTS of the 80th character on line 13 clocks the counter to line 14 (vertical retrace). A V DRIVE pulse is developed which simultaneously causes the vertical sweep to collapse and cuts off the video amplifier. The V DRIVE pulse remains low for 80 character times until the next clock pulse toggles the counter and A17.12 goes high. When the V DRIVE pulse returns to a high level at the 80th character of line 14, the horizontal drive goes low to return the CRT scan to the left side of the screen. During the 87th character of line 14, (Δ) is gated through NAND-gate A13.8 as F(Δ) to mark CTS of the first character, first line position. The line counter timing diagram is shown in figure 4-63 and the overall timing diagram for the high-speed timing circuits is shown in figure 4-64.

4-24.8 1200-Baud Circuitry

The purpose of the 1200-baud circuitry is to count down the CTS output of the bit counter to develop a 1200-baud clock for gating data to and from the CPU I/O device. The 1200-baud circuitry is formed by the gates and counters illustrated in figure 4-65.

The 1200-baud output pulses from inverter driver A24.6 are controlled by the ØA gate circuitry on the Communications Control Board A12. When the Display Terminal is not actively transmitting or receiving data, the 1200-baud counter and the 10-bit decimal counter are held reset by a $\overline{\text{ØA GATE}}$ level present at the output of A38.6.

In the receive mode, the start bit of each incoming 10-bit character is used to set A38.6 high, thereby releasing the counter. When the START bit is detected by sensing a high-to-low transition of the received data line, AND-gate A41.6 is enabled. This produces a pulse out of A30.8 which releases the 10-bit counter (A24.6) and sets the ØA gate output high (A38.6). The counter then begins counting CTS pulses which are coupled through AND-gate A35.6.

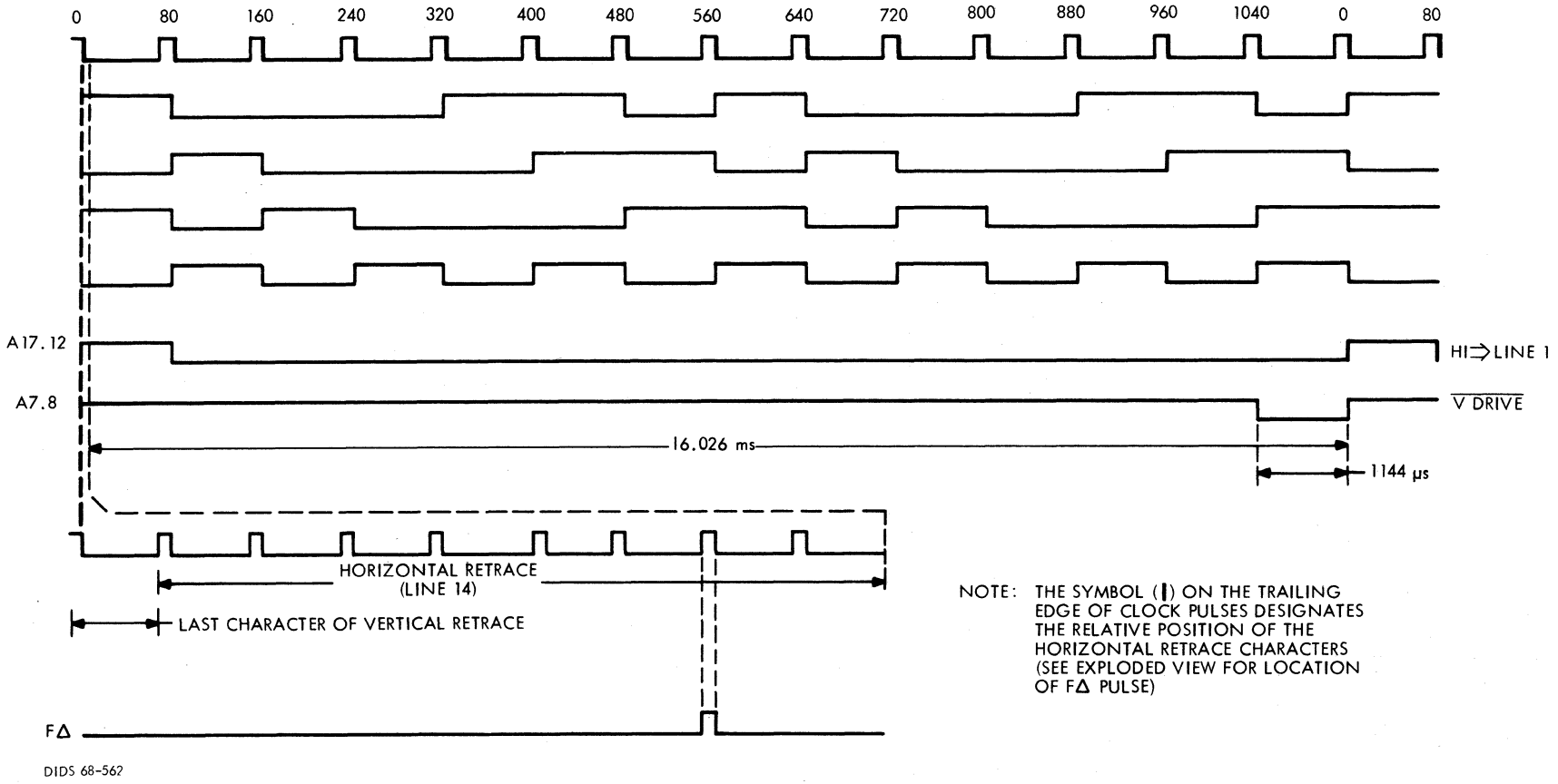


Figure 4-63. Line Counter, Timing Diagram

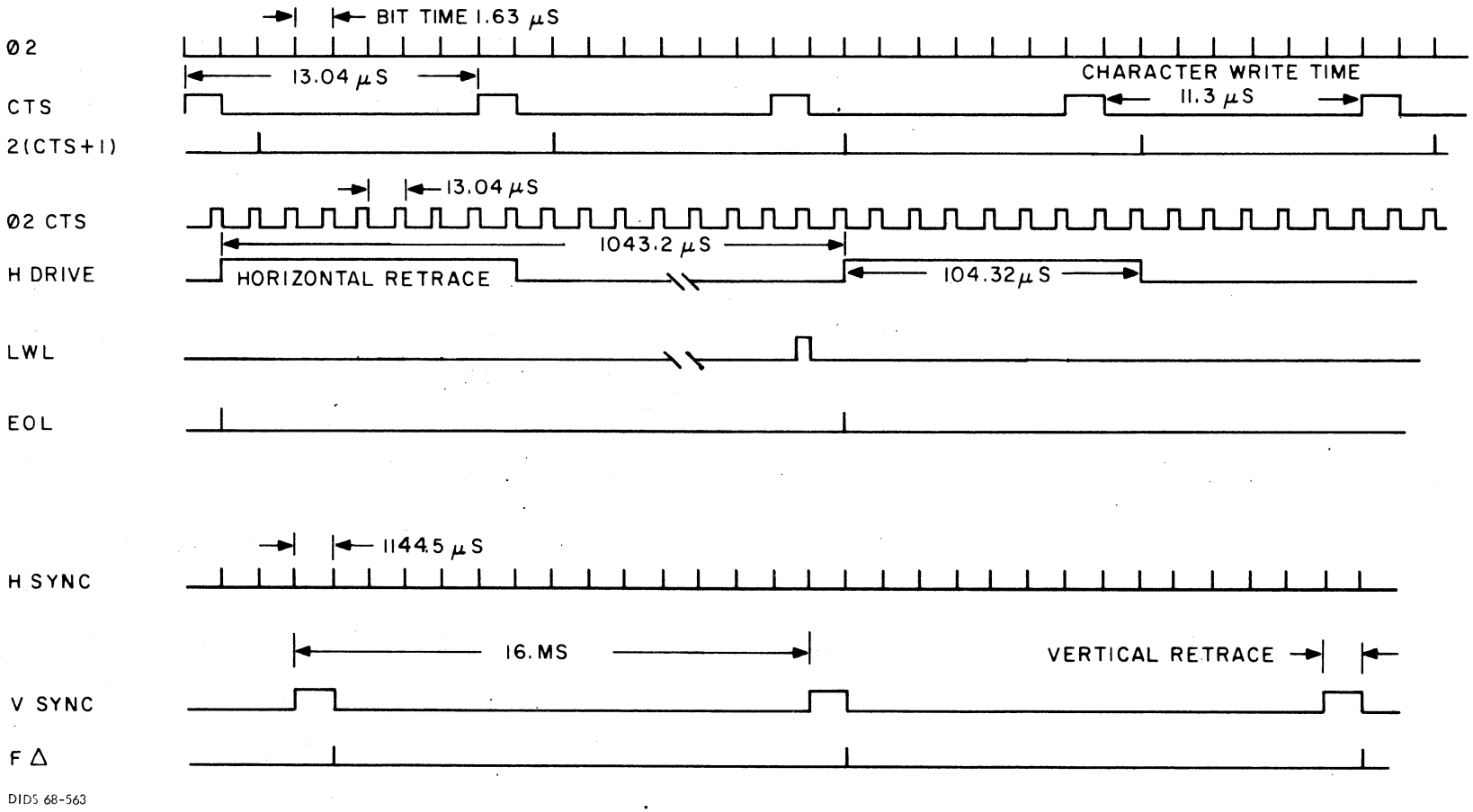
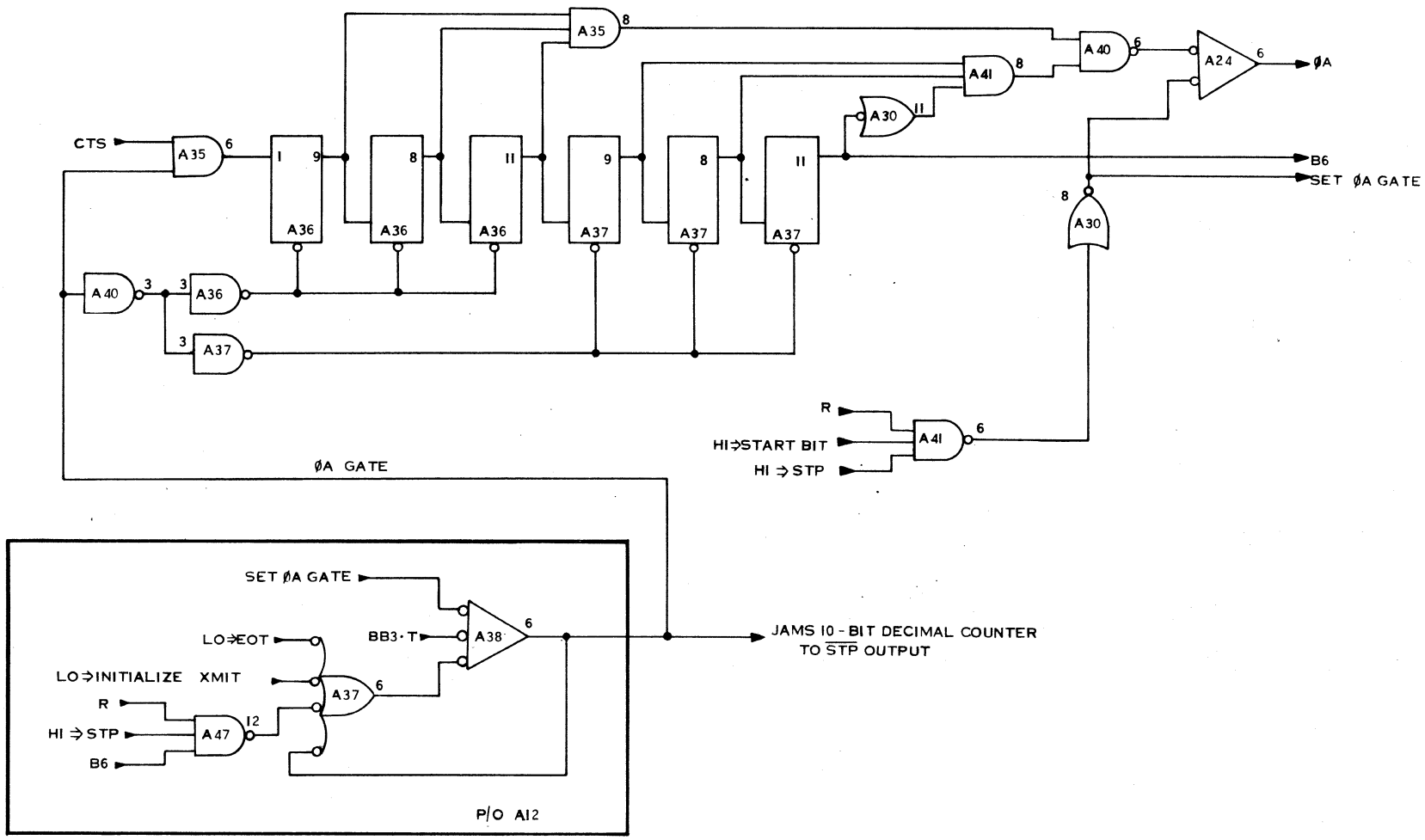


Figure 4-64. High-Speed Timing Diagram



DIDS 68-564

Figure 4-65. 1200-Baud Circuitry, Logic Diagram

Each 1200-baud counter flip-flop is connected in a divide-by-two arrangement and after 32 CTS pulses have been counted, a ØA pulse is developed to gate the first data bit into buffer register D1. Each time a ØA pulse is produced, B6 goes high and remains high for 32 CTS counts. The next ØA pulse is produced 64 CTS pulses later when the 1200-baud decodes are once again enabled. The ØA pulses are offset in this manner in order to guarantee their occurrence during the center of each bit time of received data characters.

The 10-bit decimal counter, which is clocked by ØA output pulses, cycles through 10 separate states which correspond to each bit of the received character. After ten ØA pulses have been counted, the 10-bit decimal counter toggles to a STP state and NAND-gate A47.12 is enabled by the B6 output at A37.11. This resets ØA gate to a 'not' condition and resets the 1200-baud countdown by resetting each counter and inhibiting AND-gate A35.6. The counter is started once more when the next START bit is detected on the received data line.

When the Display Terminal enters the transmit mode, Initialize XMIT goes low to clear buffer registers D2 and D3 and set ØA to a 'not' condition. This resets both the 1200-baud and 10-bit decimal counters. When the first character (STX) is jammed into D3, BB3 goes high to set the output of A38.6 high and thereby enable the counters.

After 32 CTS pulses have been counted, a ØA pulse is developed to place the start bit on the transmitted data line. Sixty-four CTS pulses later, the first data bit is shifted onto the transmitted data line when the second ØA pulse is developed. Simultaneously, the 10-bit decimal counter is toggled to its next state.

After ten ØA pulses have been produced in this manner, the character code in D3 has been shifted out to the CPU I/O device and the 10-bit counter has returned to $\overline{\text{STP}}$. During the time it takes for the 10-bit counter to toggle from $\overline{\text{PAR}}$ to $\overline{\text{STP}}$, another character is shifted into D3. Once again, this produces a BB3•T level to enable the 1200-baud counter. The counter continues to operate in this manner until the last character of the message has been transmitted. When all three buffer registers empty, a Ø3 pulse is gated through as an end-of-transmit level to reset the ØA gate flip-flop to its quiescent state ($\overline{\text{ØA GATE}}$). This level resets the 1200-baud and 10-bit decimal counters to their quiescent counts of all 0's and $\overline{\text{STP}}$, respectively.

4-24.9 10-Bit Decimal Counter

The purpose of the 10-bit decimal counter is to produce outputs in coincidence with the START, PARITY and STOP bits of each transmitted or received data character. The 10-bit decimal counter is shown in figure 4-66.

Normally, the 10-bit decimal counter is jammed to an $\overline{\text{STP}}$ output by $\overline{\text{ØA GATE}}$. As stated in paragraph 4-24.8, specific conditions are detected during transmit or receive which release the counter and allow it to cycle through the 10 states shown in figure 4-67.

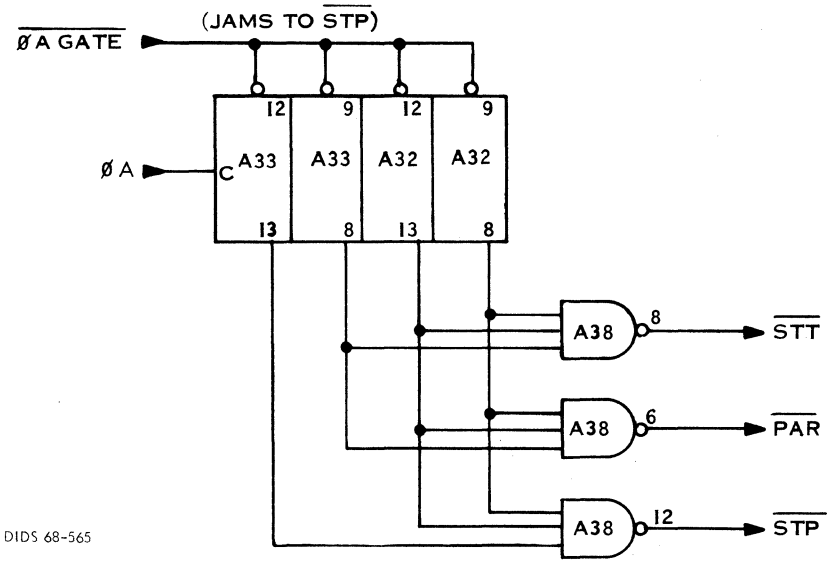


Figure 4-66. 10-Bit Decimal Counter, Logic Diagram

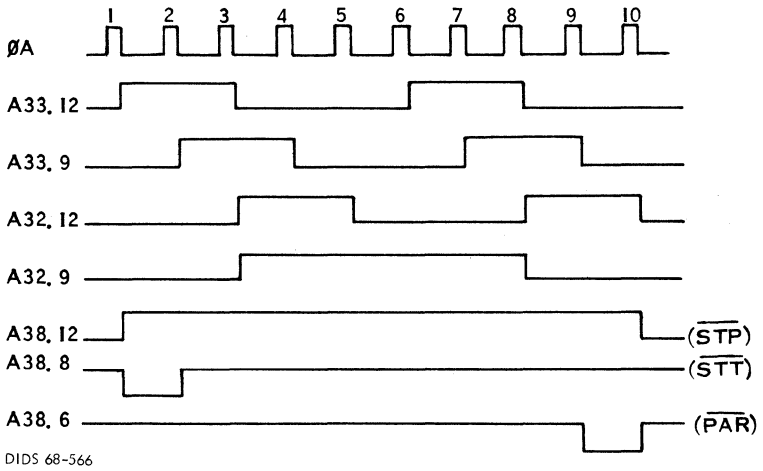


Figure 4-67. 10-Bit Decimal Counter, Timing Diagram

The 10-bit decimal counter is held reset by the $\overline{\text{ØA GATE}}$ level. This level is present whenever the Display Terminal is neither transmitting nor receiving data. The reset condition is decoded by NAND-gate A38.12 which produces an $\overline{\text{STP}}$ output. This level is used to hold the transmitted data line in a marking condition.

When ØA gate goes high as a result of the conditions previously described, the counter is released. The first ØA pulse clocks the counter to its first state and NAND-gate A38.8 is enabled to produce an $\overline{\text{STT}}$ output. This pulse resets the parity-check flip-flop in preparation for checking the incoming (or outgoing) character parity. When the counter steps from $\overline{\text{STP}}$ to $\overline{\text{STT}}$, the transmitted data line goes low to form the START bit.

During the next seven states of the counter, all three decodes are inhibited. This enables the seven data bits of the character to be transmitted (or received). During the following state, NAND-gate A38.6 is enabled to produce the $\overline{\text{PAR}}$ output. This output is in coincidence with the parity bit and is used to produce the character parity bit (transmit) or to jam a parity error character into buffer register D1 (receive).

During the next state of the counter, an $\overline{\text{STP}}$ output is again produced to place a stop bit on the transmitted data line (transmit) and to reset the ØA gate circuitry (receive).

4-24.10 Miscellaneous Circuits

4-24.10.1 Cursor Video

The backward L (⌋) cursor symbol is formed by the timing miscellaneous circuit shown in figure 4-68. The cursor symbol is composed of two separate parts: a short line on the horizontal plane (-) and a longer line on a vertical plane (|). When these two video outputs are combined, a backward L (⌋) cursor symbol is produced. This symbol is produced in the following manner.

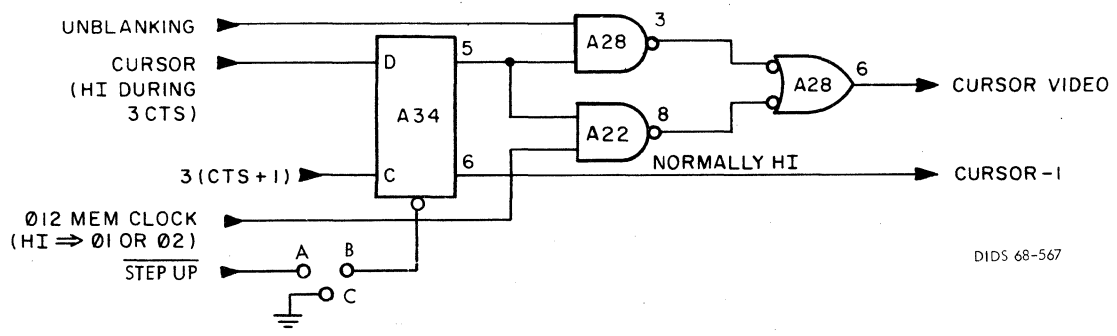


Figure 4-68. Cursor Video, Logic Diagram

When the cursor bit is detected in the CE register, the cursor input to A34.5 goes high during 3CTS and remains high until 4(CTS+1) resets the cursor located flip-flop. During 3(CTS+1), A34.5 goes high to enable one input to NAND-gates A28.3 and A22.8.

The unblanking input to A28.3 consists of short duration pulses which occur 12 times per character. During the interval 3(CTS+1) to 3(CTS+1), approximately 12 of these pulses are gated through A28.3 to form the horizontal portion of the cursor symbol (⊥).

The Ø12 MEM CLOCK input to A22.8 is high once per bit during phases 1 and 2. During the 3(CTS+1) to 3(CTS+1) interval, A22.8 is enabled approximately six times to form the vertical portion of the cursor symbol (⊥). These two outputs are combined by gate A28.6 which produces a cursor video output. This output is coupled to an alternate input of the video amplifier and occurs in coincidence with the character symbol associated with the cursor. In this manner, both the character symbol and the cursor symbol are displayed simultaneously.

4-24.10.2 Blanking

The output of the blanking circuit is used to cut off the video amplifier during the inactive scan periods of the monoscope and CRT (see figure 4-69). The most frequent blanking level occurs once per character during 3(CTS+1). This pulse is used to cut off the video amplifier while the monoscope beam is being directed to the next character symbol to be displayed. The next most frequent blanking level (assuming a full screen display) is the $\overline{\text{H DRIVE}}$ blanking level. This level is eight characters wide and occurs during horizontal retrace. This in turn cuts off the video amplifier during retrace to protect the CRT screen phosphor.

The $\overline{\text{V DRIVE}}$ blanking level operates in a similar manner but is present for 80 character times. The $\overline{\text{V DRIVE}}$ pulse (which is immediately followed by $\overline{\text{H DRIVE}}$) cuts off the video amplifier once per frame to protect the CRT phosphor during vertical retrace.

The fourth blanking output occurs when an Idle code is decoded in the CE register. The ALL 1's condition enables NAND-gate A39.6 which blanks the video amplifier during CTS+4 and CTS+5 of the character time associated with the display of the short underline symbol.

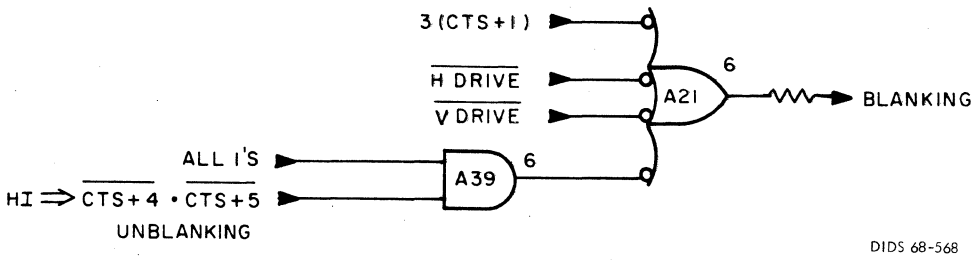


Figure 4-69. Blanking Circuit, Logic Diagram

4-24.11 Interface Circuits

The four interface circuits consist of transistorized amplifiers and level shifters on the Timing and Discrete Board. The purpose of these circuits is to level shift internal logic levels (0 and +5 vdc) to MIL-STD-188B levels of +6 and -6 vdc. These circuits also produce the drive levels necessary to compensate for the attenuation encountered by data or status levels coupled over the 50-foot CPU I/O device interface cable. The interface circuits are shown schematically on Raytheon Drawing No. 407905.

4-25 DELAY-LINE ELECTRONICS A9 AND DELAY LINE A15

The delay-line electronics board and the dual 8.013-ms delay line form a part of the refresh memory loop. The delay line, which has a total storage capacity of 1232 characters, provides an economical means of storing data intended for display. Because of high delay-line attenuation, the read-write amplifiers are used to amplify this data both before and after it is applied to each delay-line section. (Refer to Raytheon Drawing No. 389280.)

Serial data enters the delay-line electronics board at 'data-in' terminals F and G. True data is applied to terminal F, while the inverse is applied to terminal G.

I-C A4 contains four NAND-gate logic elements which enable resynchronizing the serial data with Ø12 clock pulses before applying it to the No. 1 delay-line write amplifier.

The write amplifier, A5, consists of a push-pull amplifier which drives opposite ends of the input transducer coil. As the electrical impulses present at the input coil are transformer coupled into the output coil, a mechanical movement is produced. This mechanical movement (a twisting motion) travels down the magnetostrictive delay line and appears at the output transducer as an attenuated output.

The output transducer is operated single-ended with the $\overline{\text{DATA}}$ signal connected to ground through terminal A. Attenuated data re-enters the delay-line electronics at terminal B and is applied to the input (pin 1) of wideband power amplifier A1. The purpose of A1 is to restore serial data to the same amplitude it possessed prior to entering the delay-line electronics board at terminal G. The output of A1 (pin 5) is coupled to the input of a D-type flip-flop in I-C A3. The flip-flops contained in A3 perform two functions: (1) data is resynchronized by $\overline{\text{Ø2}}$ pulses to re-establish the original time relationship of each bit; and (2) the original DATA/$\overline{\text{DATA}}$ input is re-established by taking data from both the set and reset outputs of the flip-flop.

The preceding text has described the flow of serial data from its entrance into the first write amplifier to a corresponding point at the entrance to the second write amplifier. The operation of the second delay-line section circuitry is identical to that previously described and therefore need not be repeated.

Exactly 8.013 ms after data enters the second delay line at No. 2 delay-line input, it appears at DATA OUT terminals R and S. From this point, the true serial data at terminal S is coupled to the CE register via the output display logic.

4-26 MONOSCOPE DEFLECTION AMPLIFIER A3

The purpose of the monoscope deflection amplifier is to convert digital character codes arriving from Display Logic Board A13 to analog deflection voltages. These analog voltages are then used to position the monoscope scan to a corresponding character symbol on the monoscope target. In addition to positioning the scan, other signals developed on A3 cause the scan to simultaneously sweep up and down and across the character symbol.

The monoscope deflection amplifier is composed of the following circuits:

X and Y digital-to-analog (D/A) converters

X- and Y-deflection amplifiers

X- and Y-skew correction

Ramp and minor vertical sweep generation

Unblanking pulse generation

4-26.1 X and Y Digital-to-Analog Converters

As previously stated, the monoscope target is composed of 96 separate character symbols arranged in an 8-row, 12-column coordinate system. The monoscope scan is directed to a particular row on the target by a Y-axis deflection voltage. This voltage is developed by summing the binary values of the three LSB's of a character code held in the CR register. Conversely, the monoscope scan is directed to a particular column on the target by an X-axis deflection voltage. This voltage is developed by summing the four MSB's of a character code held in the CR register. The particular character being scanned at any given moment is determined by the intersection of the X- and Y-axis analog voltages. The manner in which these analog voltages are developed is described below (see Raytheon Drawing 425100).

The four MSB's of the character held in the CR register are coupled to the monoscope deflection amplifier over input lines DAX8, DAX4, DAX2, and DAX1. These bits are applied to a weighted summing network formed by diodes CR2 through CR5, four similar diodes in I-C A1, and resistors R51, R71, R72, and R73. The binary value of the four MSB's connects a specific resistive network between a reference regulator, A5, and the input to X-axis deflection amplifier A2.

Depending upon the character code held in the CR register, current flows from the reference regulator through one, two, three, or all four of the weighting resistors. The analog voltage applied to the input of A2 is therefore proportionate to the binary value of the character codes for the MSB's. The analog voltage developed in this manner is applied to A2 in coincidence with the ramp signal.

The three LSB's of the character held in the CR register are converted in a similar manner. These bits are applied to the monoscope deflection amplifier over input lines DAY4, DAY2, and DAY1. The Y-axis summing network is formed by diodes CR6 through CR8, three similar diodes in I-C A1,

and resistors R74 through R76. A negative reference voltage from regulator A4 flows through a specific branch of the summing network to develop an analog voltage. This voltage is applied to Y-axis deflection amplifier A3 in coincidence with a 1.3-MHz vertical sweep signal.

4-26.2 X-Deflection Amplifier and Associated Circuits

The X-axis analog voltage is applied to the input of A2 in coincidence with a ramp voltage from transistor Q1. This voltage (a simple sawtooth) is developed once per character during the interval 2(CTS+1) through 2(CTS). The purpose of the ramp voltage is to move the monoscope scan from left to right across the character symbol being scanned; this is accomplished as described below.

During 2CTS, a character code is clocked into the CR register and simultaneously Q1 is turned on by a blanking pulse which occurs during 3(CTS+1). During CTS+1, the analog voltage from the X-axis summing network is amplified by A2 and the monoscope scan is positioned on the left side of the character symbol. On the trailing edge of CTS+1, Q1 is cut off by the trailing edge of the blanking pulse, and capacitor C1 begins to charge through R2. The steadily rising charge on C1 is coupled through R4 and appears at the input to A2 as a sawtooth voltage. This voltage causes the monoscope scan to move from left to right across the monoscope character symbol. (Simultaneously, the minor vertical sweep 'modulates' the Y-axis voltage, causing the scan to sweep up and down across the character.) On the trailing edge of 2(CTS), a second character code is clocked into the CR register. Simultaneously, the ramp voltage collapses due to C1 discharging through Q1 and the cycle repeats for the next character code.

A Y-skew correction voltage is developed by the resistive network formed by resistors R16 through R20. The purpose of R16 (X-skew) is to balance the outputs of Q2 and Q3. This applies an equal voltage of opposite polarity to each deflection plate. If R16 must be adjusted off-center, a skew correction voltage is developed and coupled to the Y-deflection amplifier. This voltage compensates for angular deficiencies in the Y- and X-deflection axes.

4-26.3 Y-Deflection Amplifier and Associated Circuits

The Y-axis analog voltage (coupled from the Y-axis summing network) is applied to the input of A3 in coincidence with the minor vertical sweep signal. The minor vertical sweep is developed on the timing board by a countdown circuit which divides the master clock by a factor of two. The 1.3-MHz square wave signal (phase-shifted 180 degrees on alternate CRT scans) is applied to transistor Q6, which is connected as a common emitter to the diddle coil. The diddle coil (which produces the CRT scan horizontal line width) is a resonant circuit that changes the minor vertical signal to a sine wave. This sine wave (which occurs at a rate of 12 times per character) is applied through a phase forming network to the input to Y-axis deflection amplifier A3.

The minor vertical sweep signal is combined with the Y-axis analog voltage and the X-axis skew voltage and amplified by differential amplifier A3. The push-pull outputs of A3 are coupled to a second push-pull amplifier formed by Q4 and Q5 to form (+) and (-) Y-axis deflection voltages. These voltages increase

and decrease in value each time the minor vertical sine wave approaches its maximum positive or negative value. The constantly fluctuating Y-axis voltages cause the monoscope beam to sweep up and down across the character symbol. This painting effect is phase-shifted by 180° on alternate CRT scan cycles so that, effectively, the character symbol is scanned 24 times (12 times per frame). This painting effect, when combined with the ramp voltage, assures that all parts of the character symbol are thoroughly scanned by the monoscope beam.

Like the X-axis deflection amplifier, the Y-axis push-pull output stage employs a skew correction circuit. The outputs of Q4 and Q5 are balanced by adjusting R21, and the resulting X-axis skew correction voltage is coupled to the X-axis deflection amplifier.

4-26.4 Unblanking Pulse Generation

The purpose of the unblanking pulse generator (figure 4-70) is to develop spiked outputs in coincidence with the bottom-most peak of the minor vertical sweep signal. This is accomplished as follows.

The minor vertical sine wave developed by the diddle coil is returned to the monoscope deflection amplifier at input terminals AJ and AK. The signal at each terminal is 180 degrees out of phase with the opposite terminal, since they represent opposite ends of the diddle coil. This 180-degree phase difference is split to 90 degrees by an adjustable phase network (R37 and C13). Thus a minor vertical sine wave shifted 90 degrees in phase is applied to pin 9 of the unblanking pulse generator (A6). Since this signal is shifted by 90 degrees, the point at which the sine wave crosses its zero axis is equivalent to the negative peak of the minor vertical signal.

The phase-shifted signal applied to pin 9 is coupled to an emitter-follower (A6A) which, in turn, drives a Schmidt trigger formed by A6B and A6C. This circuit develops a square wave output (present at A6, pin 4) which is integrated and applied to a second emitter-follower formed by A6D. This spiked unblank pulse output appears in coincidence with the negative peak of each minor vertical sine wave. As stated previously, 12 of these pulses occur each character time. On Timing and Discrete Board A14, two of these pulses are used to form the lower portion of the cursor symbol (_). The unblanking output is also used for blanking the video amplifier during $\overline{\text{CTS}}$+4 and CTS+5 when an Idle code is decoded in the CE register. This blanking limits the time the 'short underline' (_) is displayed on the CRT to five bit times instead of the normal seven bit times.

4-26.5 Monoscope VI

The monoscope (figure 4-71) is a vacuum tube device that generates a video output for displaying alphanumeric and special symbols on the CRT screen.

An electron beam originating at a cathode element at one end of the tube is accelerated toward a target anode at the other end of the tube. Beam acceleration results from the difference in potential between the cathode and target anode voltages. The cathode is at a -1.2 kv level developed by the high voltage power supply, and the target is at 0 volt.

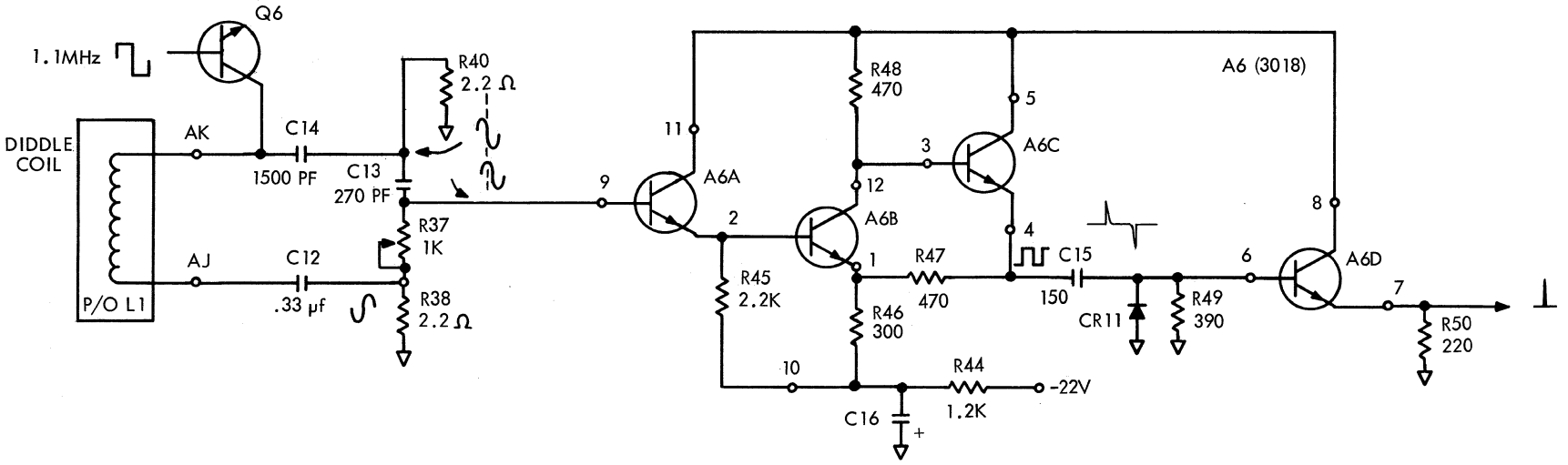


Figure 4-70. Unblanking Pulse Generator, Schematic Diagram

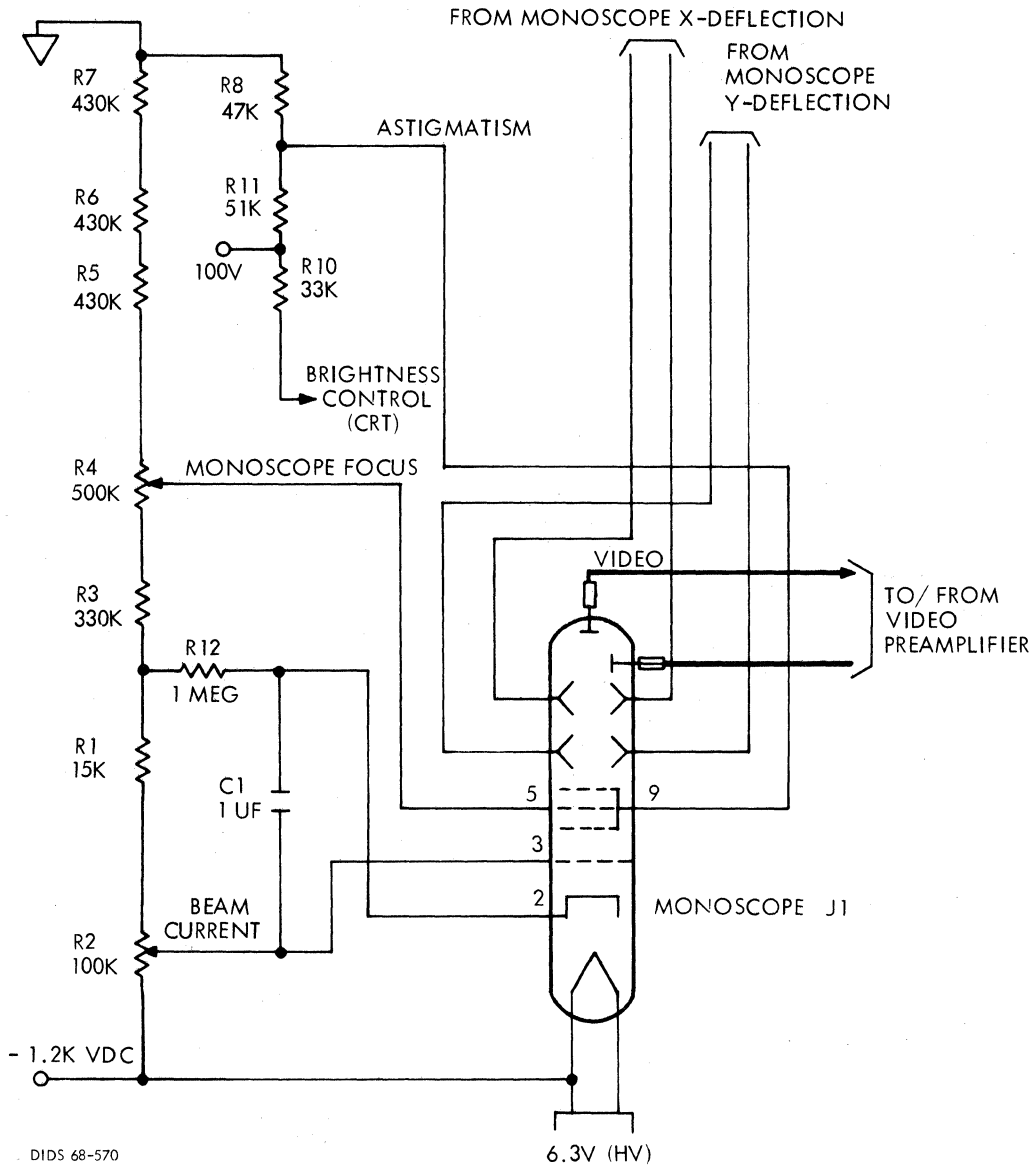


Figure 4-71. Monoscope and High Voltage Network, Schematic Diagram

The Y-deflection voltage includes a 1.3-MHz minor vertical sweep sine wave, and a dc analog voltage that results from the conversion of a 3-bit digital word. The amplitude of this digital word is such that the beam is positioned on the Y-axis over one of the horizontal rows on the target anode. The 1.3-MHz sine wave component causes the beam to move up and down on the Y-axis at a sinusoidal rate.

With the X- and Y-deflection voltages simultaneously positioning the beam, the beam scans over the entire selected target character. When the beam strikes the deposited carbon portion of the character, the ratio of primary beam current to secondary emission is approximately 1:1. When, however, the beam strikes the aluminum oxide of the target anode, there is a high ratio of secondary emission to primary electrons. This ratio causes current to flow through a load resistance that is connected between the target anode and the collector. As the beam moves from carbon to aluminum oxide areas of the target, the current flowing through the load resistance varies at a rate that is determined by the character in the selected location on the target. Current flowing through the load resistance is connected to the input of the video preamplifier circuit.

4-27 VIDEO PREAMPLIFIER A7

Video Preamplifier A7 (shown in Raytheon Drawing No. 425105) amplifies the monoscope target video by a factor of 100 before coupling the amplified video to Video Amplifier A8. When the monoscope scan is directed to a character symbol on the target element, secondary emission develops a low-level current of 1 to 3 μA. This current flows through a video compensation network formed by L1 and R4 and develops approximately 1 mv of video across input load resistor R5. The amplified and inverted output of differential amplifier 1C1 is coupled through capacitor C3 and resistor R10 to the input circuit of video amplifier A8.

4-28 VIDEO AMPLIFIER A8

Video Amplifier A8 (shown in Raytheon Drawing No. 425102) consists of circuits that perform the following functions:

a. Amplify monoscope or cursor video levels to a level sufficient for driving the CRT cathode element (A1, Q1, and Q2)

b. Disable the video to the CRT when a blanking signal is present (Blanking)

c. Disable video to the CRT when either the vertical or horizontal deflection amplifier fails (CRT protect)

d. Adjust the screen brightness of the CRT

4-28.1 Video Amplification

Input video signals are coupled from Monoscope Video Preamplifier A7 or from Timing and Discrete Board A14. From the video preamplifier, video signals are applied to Wideband Video Amplifier A1 and developed across input load resistor R4.

Current flowing through the load resistor develops approximately 1 volt of video which is amplified by A1 and applied to the base of Q1. Transistors Q1 and Q2 form a cascode video amplifier arrangement that develops approximately 50 volts of video for application to the CRT cathode element.

Cursor video is developed on the timing board by the circuit described in paragraph 4-23.10.1. This video is applied through resistors R18 and R19 and is amplified in the same manner as monoscope video.

4-28.2 Blanking

The CRT video is inhibited each time a blanking pulse is developed on timing and discrete board A14. The pulses occur during (1) CTS+1 of each character (intercharacter blanking), (2) at the end of each line during horizontal retrace, (3) at the end of each frame during vertical retrace, and (4) when the monoscope scan is shifted to the 'underline' character at the edge of the target.

When either of the above conditions occur, a blanking pulse is applied to Video Amplifier A1 through resistor R3. A low input to pin 3 is the same as a high at pin 1; consequently A1 is cut off for as long as the blanking pulse is present. This, in turn, inhibits video to the CRT during the specified times and thereby provides some measure of protection for the CRT phosphor material.

4-28.3 CRT Protect

The CRT protect circuit prevents burning an intense vertical or horizontal line on the CRT phosphor when either CRT deflection amplifier fails. The CRT grid is normally held at a positive potential, the value of which depends upon the setting of the brightness control. When either deflection amplifier fails, a positive level is developed on the CRT Protect input. This level turns Q3 on and essentially grounds the CRT grid through the heavily conducting transistor switch.

4-28.4 Cathode Ray Tube V2

The cathode ray tube (CRT) is used to display up to 1040 high-resolution characters for viewing by display terminal operators. The CRT is shown schematically in figure 4-72. The CRT anode is held at a potential of +12 kvdc by a voltage developed by the high voltage power supply. A second voltage of 500 volts is applied to pin 10 as an acceleration potential. Electrons are attracted from the cathode element at a rate controlled by the setting of the brightness control.

When video signals are coupled from Video Amplifier A1, conduction through the CRT increases and a video character appears on the CRT screen. The position where this character appears is determined by the vertical and horizontal deflection voltages applied to deflection coil L1. In addition to the vertical and horizontal windings of the deflection coils, a minor vertical (diddle) coil is contained in L1. This coil is activated by the minor vertical signal coupled from monoscope deflection amplifier A3 and increases the height of each horizontal line (and therefore the character height).

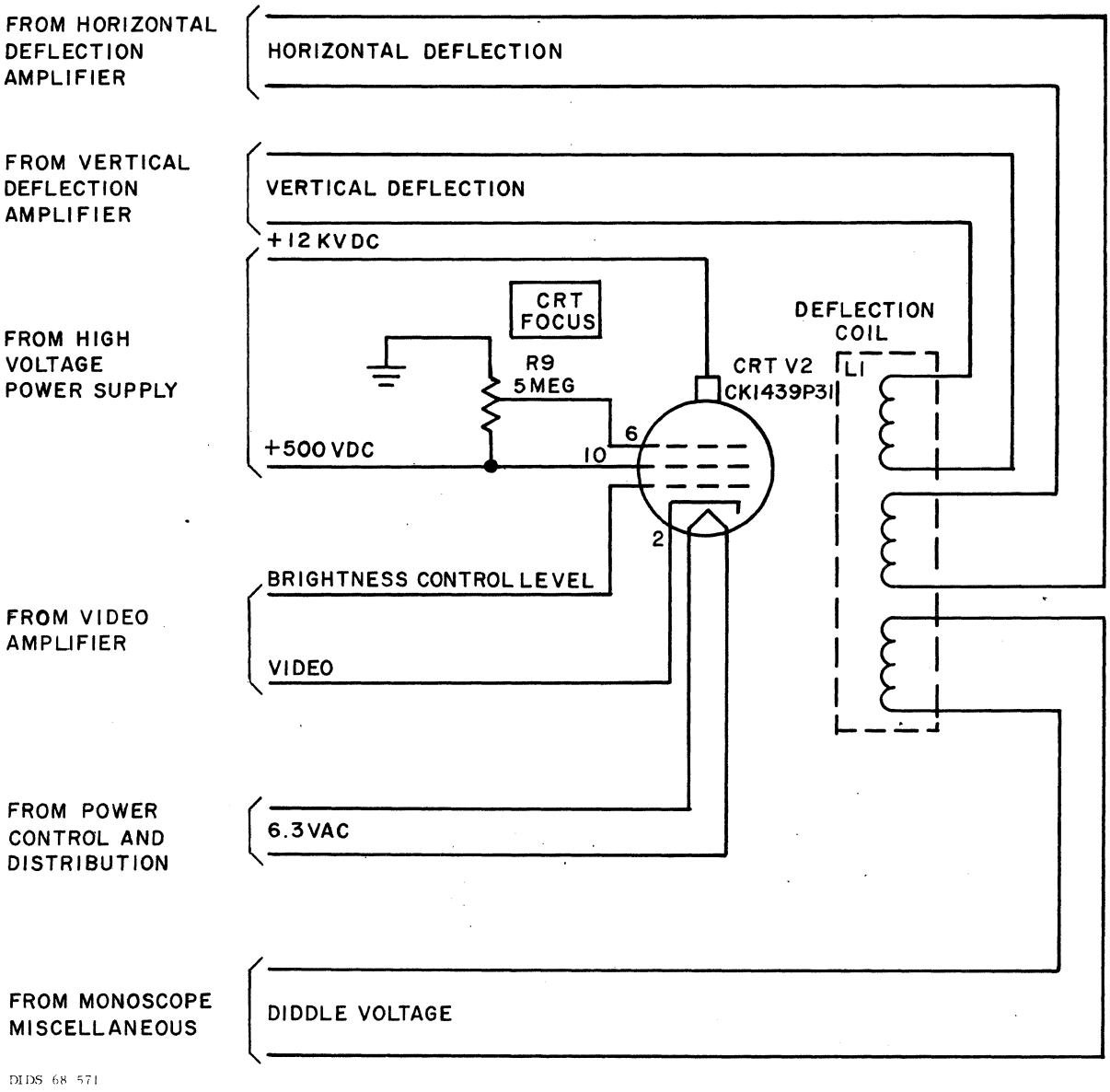


Figure 4-72. CRT Indicator, Simplified Block Diagram

4-29 HORIZONTAL AND VERTICAL DEFLECTION AMPLIFIER A2

The horizontal and vertical deflection amplifier circuitry (Raytheon Drawing No. 389300) develops skew-corrected deflection voltages for developing the CRT raster. These voltages are applied to a deflection yoke, L1, on the CRT neck to electromagnetically deflect the CRT scanning beam in a horizontal and vertical direction.

4-29.1 Horizontal Deflection Amplifier

The horizontal deflection amplifier develops a horizontal deflection voltage from H Drive digital levels coupled from the character counter on Timing and Discrete Board A14. The H Drive signal, which is positive for 80 character times (active scan) and negative for eight character times (retrace), is converted to a sawtooth voltage by a ramp generator formed by transistors Q10 and Q11.

The sawtooth output of Q11 is applied to an operational amplifier circuit formed by transistor Q12. The amplified output of Q12 is then coupled to a push-pull amplifier formed by transistors Q13 and Q14. Amplifier Q13 and Q14 is arranged in a complementary symmetrical circuit configuration to produce positive going and negative going outputs. These outputs are connected to current driver transistors located external to the circuit for additional amplification. The amplified sawtooth current flowing through the driver transistors is applied to the horizontal deflection coil and causes the CRT beam to scan across the face of the CRT.

The negative going signal at the emitter of Q14 is also fed back to the input of amplifier Q17 via the feedback network that includes R47, R50, and R37. Adjustment of the value of gain potentiometer R50 in this network controls the amplitude of the voltage fed back and, therefore, the gain of the overall operational amplifier circuit. Adjustment of the value of horizontal position potentiometer R35, which connects to the operational amplifier circuit input via resistor R38, establishes the dc level of the amplifier input. Varying this dc level varies the positioning of the horizontal sweep on the CRT face.

Connections made from the horizontal deflection coils to resistor R47 provide for a sampling of the current flow through the coils. The summing of this current with the normal feedback current flowing through the resistor provides a compensating effect that improves linearity and stability of the operational amplifier circuit. A portion of the feedback signal that is compensated in this fashion is taken at the intersection of gain potentiometer R50 and resistor R37 for application to the vertical deflection amplifier as the skew output voltage. The use of the skew voltage is described later on in the text.

The voltage developed across resistor R49 by the current sample taken from the deflection coils is applied to a CRT protection circuit. This circuit consists of diodes CR8 through CR10, resistor R52 and capacitor C15. In the presence of a horizontal deflection voltage, a negative potential exists across resistor R49. Capacitor C15 is discharged to this potential via diodes CR8, CR10, and CR52. Diode CR11 blocks the negative potential from the video amplifier circuits at the output. If the deflection voltage fails, the voltage across R52 goes positive and backbiases diodes CR8, CR10, and CR52. Capacitor C15 then charges toward +22 volts through R52. Diode CR11 now conducts, producing a signal which indicates that the deflection voltage is absent.

4-29.2 Vertical Deflection Amplifier

The vertical deflection amplifier develops a skew-corrected vertical deflection voltage from a V Drive digital level coupled from the line counter on the timing and discrete board (A14). The V Drive signal, which is positive for 13 horizontal line times and negative for one line time, is converted to a sawtooth voltage by a ramp generator formed by transistors Q1 and Q2.

At the base of Q3, the vertical sawtooth is combined with a horizontal skew voltage which produces a stepped sawtooth voltage. This stepped voltage adjusts the vertical deflection sawtooth so that the CRT scan is not moved vertically until the completion of each horizontal line. In the absence of the horizontal correction voltage, the trace resulting from combined horizontal and vertical deflection voltages would produce the raster shown in figure 4-22, part A. When the correction voltage is applied, however, the wave form shown in part B of figure 4-22 produces perfectly horizontal scan lines.

The stepped sawtooth output of Q3 is applied to push-pull amplifiers Q4 and Q7 to develop opposite phase signals. These signals are applied to a push-pull current amplifier formed by transistors Q5, Q6, Q8 and Q9 before being coupled to the vertical deflection coil.

Gain control R27 limits the amount of signal in the feedback loop and thereby controls the amplification of the amplifier.

SECTION IV
INTEGRATED CIRCUITS

4-30 GENERAL DESCRIPTION OF SECTION CONTENTS

This section contains detailed explanations of the individual integrated circuits (I-C's) used in the Display Terminal and the operation of the various logic elements contained in each I-C. The purpose of this section is to provide logic diagrams and reference material for each I-C. In addition, basic logic explanations are provided herein for the maintenance technician who is not familiar with digital logic techniques.

For the most part, I-C's are concentrated on digital logic boards A12, A13, and A14. The remaining I-C's are located on the various analog boards. The I-C's employed in the Display Terminal utilize transistor-transistor-logic (TTL or T^2L).

4-31 INTEGRATED CIRCUITS

Table 4-4 lists the types of I-C's used in the Display Terminal. All manufacturer's part numbers are cross-referenced to Raytheon part numbers to assist in ordering replacement parts.

Table 4-4. I-C Part Numbers and Cross-Reference

Circuit No.	Raytheon No.	Texas Instrument No.	RCA No.
74H11	385729-1	4019	
7410N	385712-1	4002	
7420N	385714-1	4004	
7430N	385716-1	4006	
7472N	385737-1	4027	
7473N	385739-1	4029	
7474N	385740-1	4030	
7493N	385863-1	4039	
CA3012			CA3012
CA3018			CA3018
CA3020			CA3020
7510L	405032-1	7510L	
933	C-329804	933	

The logic diagrams of T^2L integrated-circuits used on the digital boards are illustrated in figure 4-73. These diagrams show the internal logic elements contained in each I-C and the external pin number of input and output connections. Figure 4-74 illustrates the schematic diagram of the microminiature circuits contained on the analog boards.

The I-C's illustrated in figures 4-73 and 4-74 perform the following logical or analog operations:

AND

NAND

Inverter Driver

Edge Triggered Flip-Flop

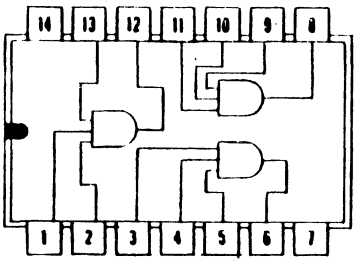
J-K Master Slave Flip-Flop

4-Bit Binary Counter

Wideband Amplifier

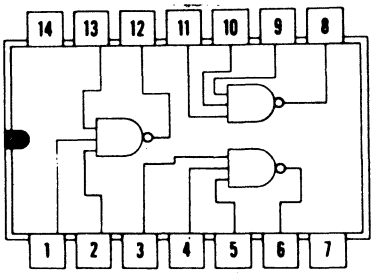
Power Amplifier

74H11N



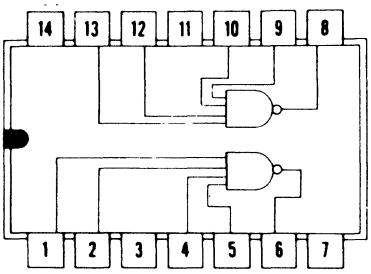
TRIPLE 3-INPUT AND GATE

7410N



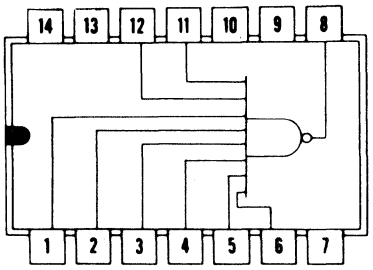
TRIPLE 3-INPUT NAND GATE

7420N



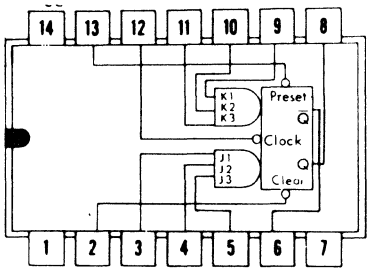
DUAL 4-INPUT NAND GATE

7430N



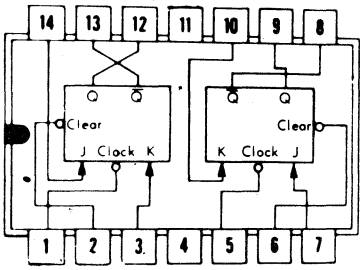
8-INPUT NAND GATE

7472N



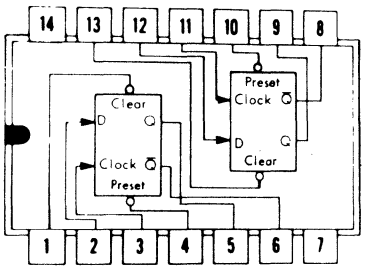
J-K MASTER-SLAVE FLIP-FLOP

7473N



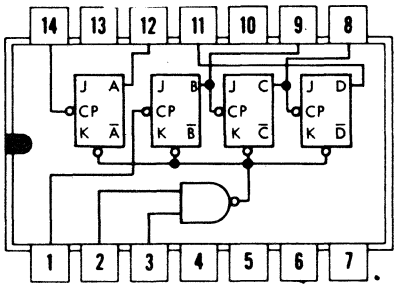
DUAL J-K MASTER-SLAVE FLIP-FLOP

7474N



DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

7493N



4-BIT BINARY COUNTER

DIDS 68 572

Figure 4-73. Integrated Circuits, Logic Diagram

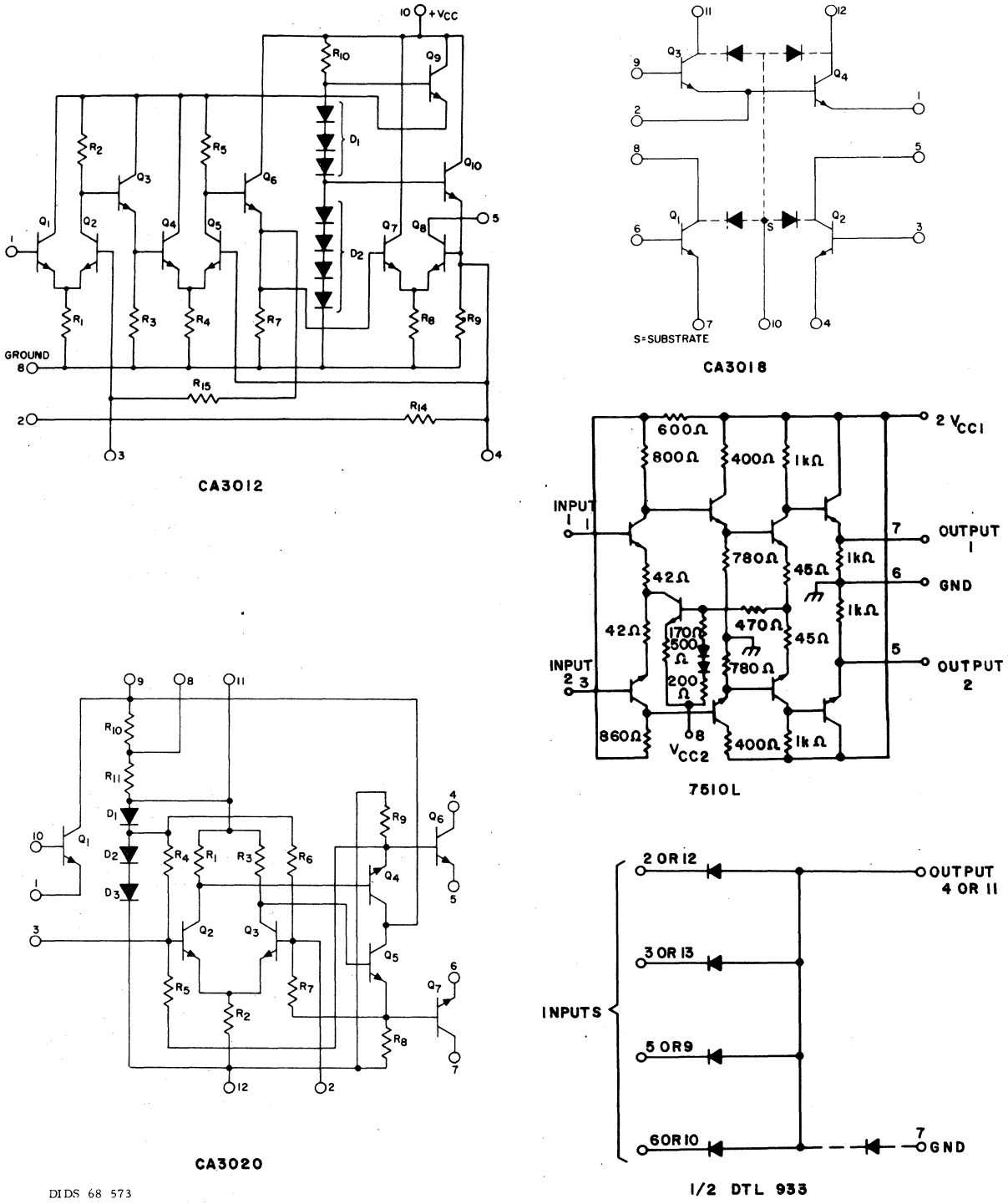
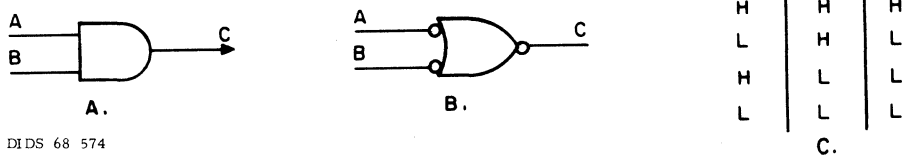


Figure 4-74. Analog Microminiature Circuits, Schematic Diagram

4-31.1 AND Function

The symbols shown in figure 4-75 represent two methods of performing the logical AND function . Part A of the illustration is used in circuits where the design intent is to produce a high output when two or more inputs are high in coincidence. Part B is used in circuits where the design intent is to produce a low output when either of the normally high inputs goes low. Part C is the truth table for a 2-input AND-gate.



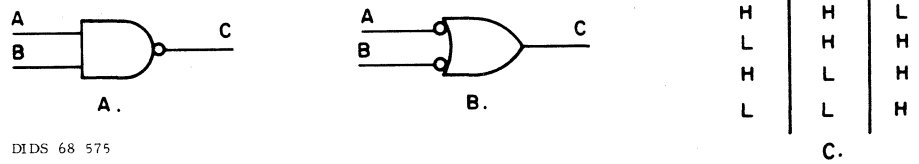
A	B	C
H	H	H
L	H	L
H	L	L
L	L	L

C.

Figure 4-75. AND Function Logic Diagram and Truth Table

4-31.2 NAND Function

The symbols shown in figure 4-76 represent two methods of performing the logical NAND-function. The NAND-function is a variation of the AND-function. In NAND-gates, however, the output is low if, and only if, all inputs are high. Part A of the illustration is used in circuits where the design intent is to produce a low output when all inputs are high in coincidence. Part B is used in circuits where the design intent is to produce a high output when any of the normally high inputs goes low. Part C illustrates the truth table for a 2-input NAND-gate.



A	B	C
H	H	L
L	H	H
H	L	H
L	L	H

C.

Figure 4-76. NAND Function Logic Diagram and Truth Table

4-31.3 Inverter/Driver Function

The symbol shown in figure 4-77 represents the inverter/driver function. The purpose of the inverter driver is to invert the logical truth and provide a multi-element drive capability. Depending upon the design intent, either a low or high truth may be used to drive the connected elements. Parts A, B, and C of Figure 4-77 illustrate three separate methods of employing the inverter/driver function. Part D illustrates the truth table for each function.

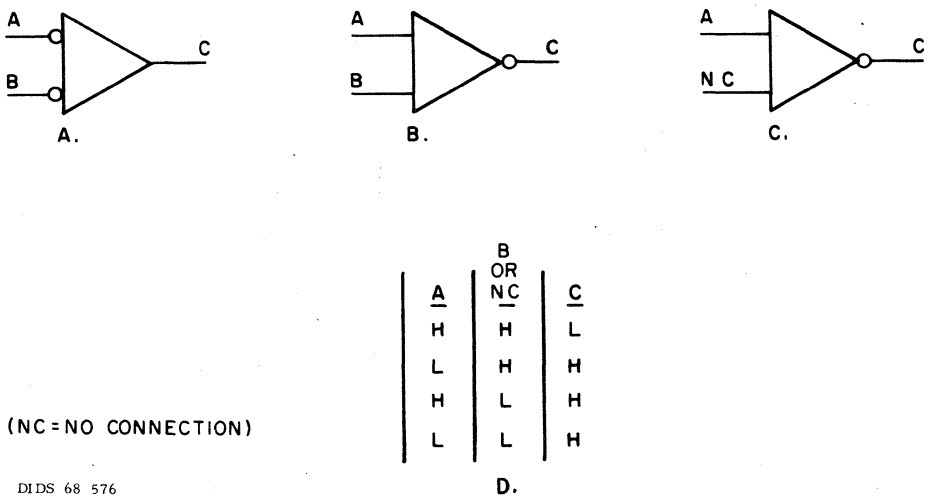


Figure 4-77. Inverter/Driver Function, Logic Diagram and Truth Table

4-31.4 Edge-Triggered Flip-Flop

The symbol shown in Figure 4-78 represents an edge-triggered flip-flop. When a high is applied to D, it is shifted to the Q output on the positive transition of the clock. The flip-flop may be jammed set or reset by applying a low input pulse to the Preset and Clear inputs respectively.

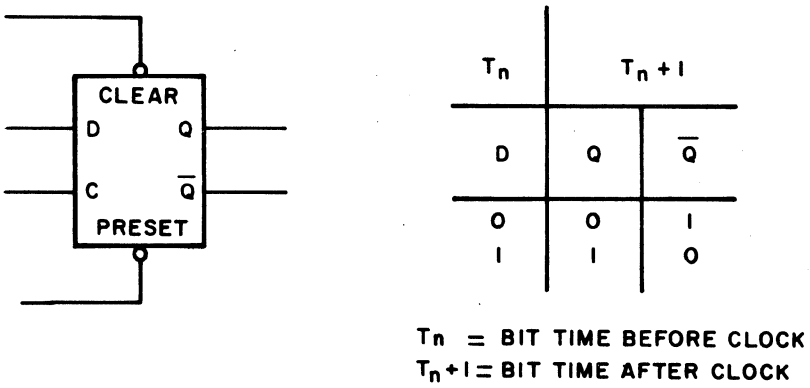
4.31.5 J-K Master-Slave Flip-Flop

The symbols shown in figure 4-79 represent two variations of the J-K master-slave flip-flops. Part A illustrates a 7472N type logic element. Input AND-gates are used to AND the input signals for both the set and reset inputs. However, since this flip-flop is a T^2L element, all input connections need not be connected in order to perform the AND-function. For example, if three pins have external circuit connections, then all three inputs must be high to satisfy the input. If, however, only two pins are connected externally, then only these two inputs must be high to satisfy the input.

Part B illustrates 7473N type logic element. In this element, satisfying either the J or K input will set or reset the flip-flop.

Both circuits use the master slave principle. On the positive transition of the clock, the master portion stores the input information and on the negative transition of the clock the information appears at the slave outputs. Unclocked signals can be used on the jam pin inputs; these signals override the normal clocked inputs. A low input to preset (7472N only) sets Q to a logical 1 while a low input to clear sets Q to a logical 0.

The truth table (C) shown in figure 4-79 shows the logical truth output of each flip-flop when the given conditions are met. In the case of the 7472N flip-flop, a J input of 1 assumes that all the three J inputs are satisfied, and a K input of 1 assumes that all three K inputs are satisfied.



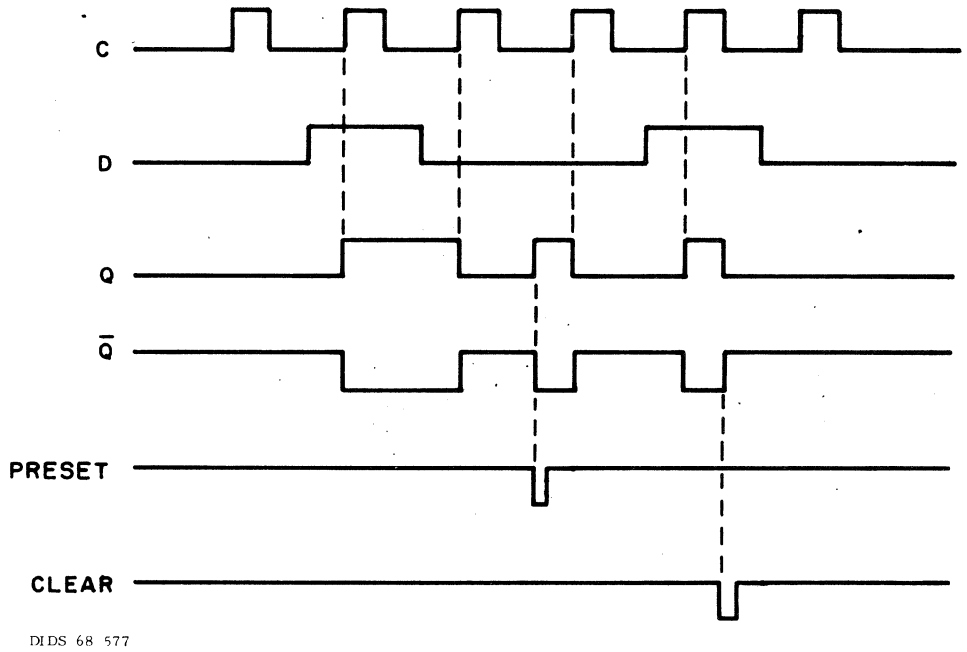
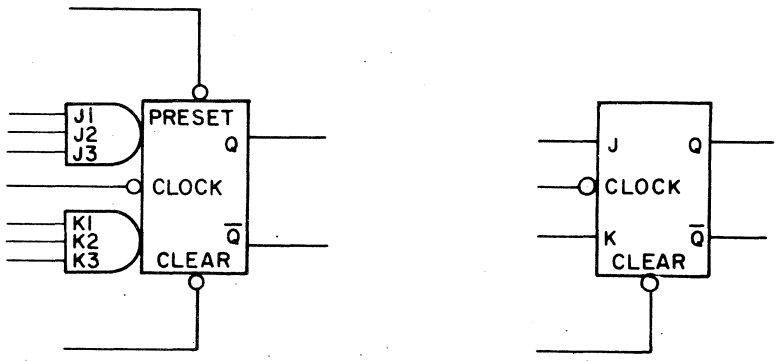


Figure 4-78. Edge-Triggered Flip-Flop, Logic and Timing Diagram and Truth Table

If a logical 0 (low) is applied to both the J and K inputs during the bit time before the clock pulse, the Q output will not change when the clock pulse occurs. If a logical 1 (high) is applied to both the J and K inputs during the bit time before the clock pulse, the Q output will be compliment on the clock's negative going transition.



T_n		T_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

T_n = BIT TIME BEFORE CLOCK
T_n+1 = BIT TIME AFTER CLOCK

DIDS 68 578

C. TRUTH TABLE

Figure 4-79. J-K Master-Slave Flip-Flop, Logic Diagram and Truth Table

4-31.6 4-Bit Binary Counter

The normal circuit configuration for the 4-bit binary counter is shown in figure 4-80. This element is used in the Display Terminal to provide an 88-count for the editing and cursor control logic. The element is also used by the timing circuits to provide 1200 baud output by counting down the CTS output of the bit counter.

The element functions as a ripple-counter with each flip-flop performing a divide by two operation. The counter is reset by applying a low to the reset input of each counter flip-flop.

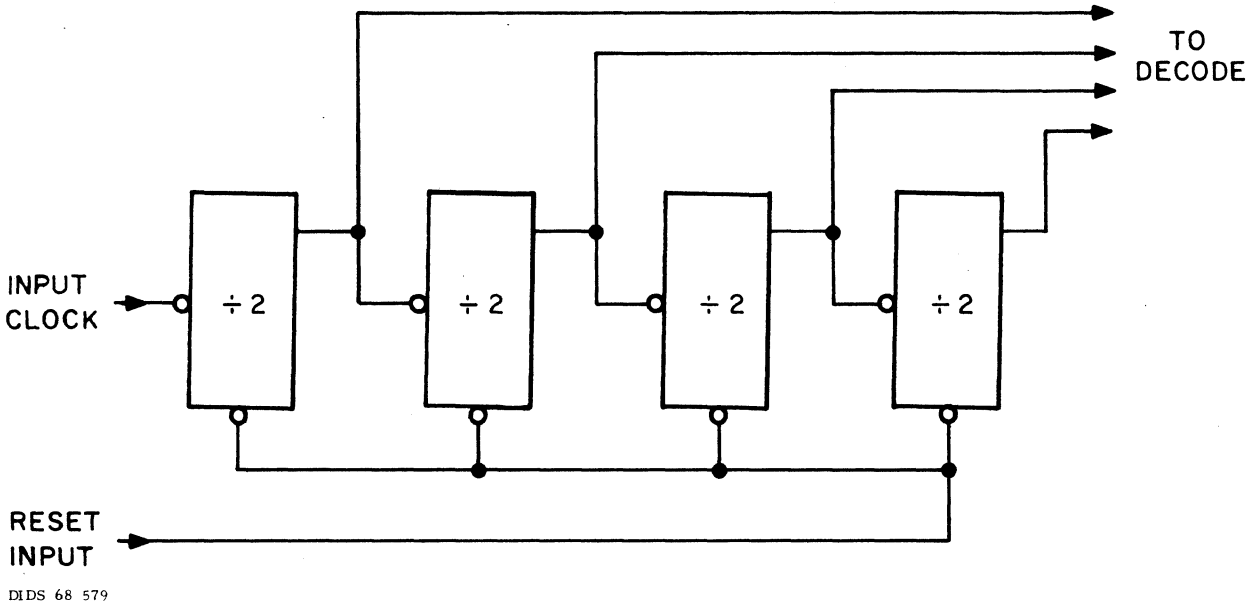


Figure 4-80. 4-Bit Binary Counter, Normal Circuit Configuration

CHAPTER 5

MAINTENANCE

5-1 MAINTENANCE CONCEPT

Because of the complexity of the Display Terminal, it is impractical in a manual of this size to detail the solution to each and every malfunction which could conceivably occur. To repair a malfunction, first obtain a thorough understanding of circuit operation by reading the theory of operation descriptions contained in Chapter 4. Assisted by this knowledge, the technician should rely on the logic and schematic diagrams contained in Chapter 7 to isolate the malfunction to an individual integrated circuit.

5-2 TEST EQUIPMENT REQUIRED

Test equipment recommended for troubleshooting the Display Terminal is listed in table 5-1. The equipment listing is provided for the purpose of illustrating the test equipment characteristics required to perform maintenance on the high-speed digital circuitry. Either the suggested equipment or its equivalent may be employed.

Table 5-1. Test Equipment Required

Function and Type or Model	Characteristics
Voltmeter, Simpson 260	Voltage Range: dc 0-5000 v ac 0-5000 v Current Range: 0-50 μa 0-50 ma
Oscilloscope, Type 454	Band Width: dc to 150 MHz Sweep Range: 0.05 μs/div to 5s/div Sweep Delay: 1 μs to 50 s

CHAPTER 6
PARTS LIST

Assy	Description	Parts No.	Qty	No. Pages
	Indicator	388041-1	1	1
A2	Vert and Horiz Defl Ampl	344947-1	1	3
A3	Monoscope Defl Ampl	425098-1	1	4
A4	LVPS	345723-1	1	5
A5	HVPS	345724-1	1	3
A6	HV Network	387926-1	1	1
A7	Preamp	425104-1	1	1
A8	Video Ampl	425101-1	1	2
A9	Delay Line Electronics	387068-1	1	1
A11	Keyboard	387188-1	1	1
A12	Communications Control Board	408024-1	1	1
A13	Display Logic	407992-1	1	2
A14	Timing and Discrete Board	407981-1	1	3
A15	Delay Line	386177-1	1	1

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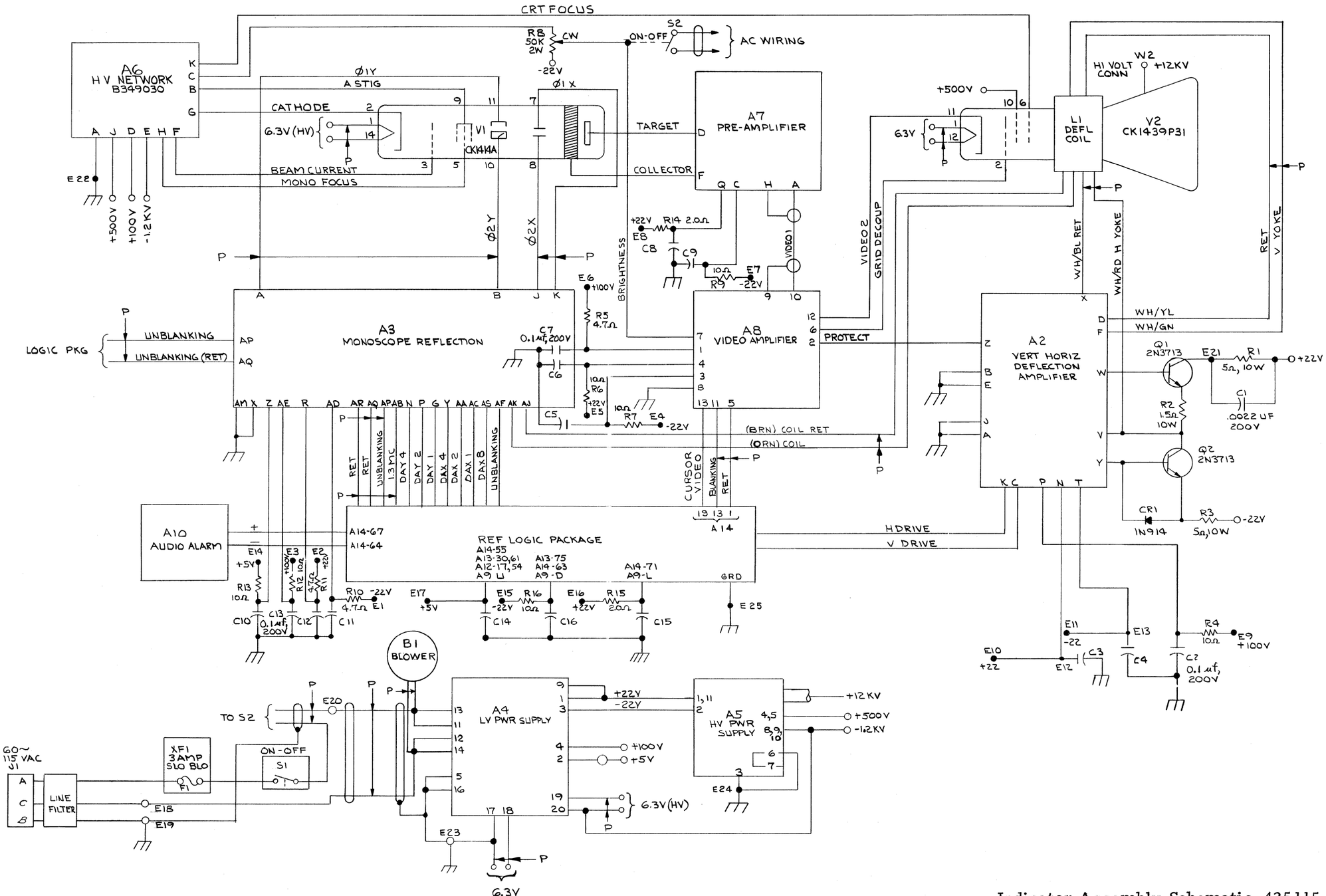
INDICATOR ASSY 388041-1

Schematic 425115

Ref Desig	Description	Vendor	Vendor Part No.	Qty
B1	Blower	Raytheon	426534	1
C1	Capacitor, 0.0022μf, 200 V		235-1684P17	1
C2, 7, 13	Capacitor, 0.1μf, 200V		235-1684P37	3
C3, 4, 5, 6, 8, 9, 10, 11, 12, 14, 15, 16	Capacitor 0.1μf, 25V		329372-1	12
CR1	Diode		1N914	1
F1	Fuse		226-1039P12	1
FL1	Filter	Sprague	425073-1	1
FL2	Filter, Capacitor W-113		425074-1	1
	Filter, Air	Raytheon	387952-1	3
R1, 3	Resistor, 5 ohm ±5%, 10W		333645-6	2
R2	Resistor, 1.5 ohm ±5%, 10W		333645-2	1
R4, 6, 7, 9, 12, 13, 16	Resistor, 10 ohm ±5%, 1/2W		RC20GF100J	7
R5, 10, 11	Resistor, 4.7 ohm ±5%, 1/2W		RC20GF4R7J	3
R8, S2	Potentiometer switch, 50K ±5%, 2W		388557	1
R14, 15	Resistor, 2.0 ohm ±5%, 1/2W		RC20GF2R0J	2
S1	Switch		MS16106-1	1
Q1, 2	Transistor		2N3713	2



Indicator Assembly Schematic 425115

DIDS-402-2AM13

VERT & HORIZ DEFL AMPL A2 ASSY 344947-1

Schematic 389300

Ref Desig	Description	Vendor	Vendor Part No.	Qty.
	PC Board	Raytheon	389394-2	1
C1	Capacitor, 1μf ±20%, 50vdc	Sprague Raytheon	218P1059R5S4 333646-1	1
C2	Capacitor, 50μf ±10%, 25V	Sprague Raytheon	TE1209-C-616 333649-6	1
C3,12	Capacitor, 470μμf ±5%, 300V	Cornell-Dubilier Raytheon	CD15 235-1535P44	2
C4,10,13	Capacitor, 10μf ±10%, 25V	Sprague Raytheon	TE1204-C-616 333649-4	3
C5,6,14, 16	Capacitor, 0.0022μf ±10%, 200V	Sprague Raytheon	192P 235-1684P17	4
C7	Capacitor, 150μμf ±5%, 500V	Cornell-Dubilier Raytheon	CD15 235-1535P57	1
C8	Capacitor, 5μf ±10%, 50vdc	Sprague Raytheon	TE1084-C-616 333649-2	1
C9	Capacitor, 0.068μf ±20%, 50V	Sprague Raytheon	194P6839R5 333648-1	1
C15	Capacitor, 0.47μf ±10%, 100vdc	Sprague Raytheon	2WF-P47 333647-1	1
C11	Capacitor, 330μμf ±5%, 500V	Cornell-Dubilier Raytheon	CD15 235-1534P40	1
CR1 thru CR11	Diode	Cont Dev Corp	1N914	11
Q1,2,3,4, 10,11,12	Transistor	Fairchild	2N3643	7
Q5,6,8,9, 13	Transistor	Sprague Raytheon	TN53 333659-1	5
Q7	Transistor	Fairchild	2N3638	1
Q14	Transistor	Motorola	2N3133	1
R1,33	Resistor, 180 ohm ±5%, 1/2W	Raytheon	RC20GF181J	1

VERT & HORIZ DEFL AMPL A2 ASSY 344947-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty.
R2,32	Resistor, 330K ±5% 1/2W		RL20S334J	2
R3,34	Resistor, 15K ±5% 1/2W		RC20GF153J	2
R4,35	Var Resistor, 10K ±5%, 0.5W	Bourne Raytheon	3307P-1-103 345262-5	2
R5,30,31, 38	Resistor, 220K ±5%, 1/2W		RC20GF224J	4
R6,36	Resistor, 4.7K ±5%, 1/2W		RL20S472J	2
R7	Resistor, 62K ±5% 1/2W		RC20GF623J	1
R8,37	Resistor, 3.9K ±5% 1/2W		RL20S392J	2
R9,21,43, 45	Resistor, 2.2K ±5% 1/2W		RC20GF222J	4
R10,39	Resistor, 15K ±5% 1W		RC32GF153J	2
R11,40	Resistor, 47 ohm ±10%, 1/2W		RC20GF470J	2
R12,41	Resistor, 6.8K ±5%, 1/2W		RC20GF682J	2
R13,42	Resistor, 820 ohm ±5%, 1/2W		RL20S821J	2
R14,44	Resistor, 10K ±5% 1/2W		RL20S103J	2
R15	Resistor, 100 ohm ±5%, 1/2W		RC20GF101J	1
R16,18	Resistor, 22 ohm ±5%, 1W		RC32GF220J	2
R17,19	Resistor, 10 ohm ±5%, 1W		RC32GF100J	2
R20,48,54, 55	Resistor, 1K ±5% 1W		RC20GF102J	4
R22,56	Resistor, 27 ohm ±5%, 1W		RC20GF270J	2

VERT & HORIZ DEFL AMPL A2 ASSY 344947-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
R23,24	Resistor, 56 ohm ±5%, 2W		RC42GF560J	2
R25	Resistor, 3.3K ±5%, 1/2W		RC20GF332J	1
R26	Resistor, 10 ohm ±5%, 5W	Raytheon	333645-1	1
R27,50	Var Resistor, 100 ohm ±5%, 0.5W	Bourne Raytheon	3307P-1-101 345262-1	2
R28,51	Resistor, 51 ohm ±5%, 1/2W		RL20S5510J	2
R29,52	Resistor, 68K ±5%, 1/2W		RC20GF683J	2
R46	Resistor, 68 ohm ±5%, 1/2W		RC20GF680J	1
R47	Resistor, 220 ohm ±5%, 1/2W		RC20GF221J	1
R49	Resistor, 1.5 ohm ±5%, 10W	Tru-ohm Raytheon	 333645-2	1
R53	Resistor, 47 ohm ±5%, 1/2W		RC20GF470J	1

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MONOSCOPE DEFLECTION AMPLIFIER A3 ASSY 425098-1

Schematic 425100

Ref Desig	Description	Vendor	Vendor Part No.	Qty
	PC Board	Raytheon	425098-2	1
A1	Expander		329804	1
A2, 3	Wide Band Amplifier		405032	2
A4, 5, 6	Transistor Array	Raytheon Fairchild	385583 CA3018	3
C1	Capacitor, 0.01μf	Raytheon	235-1684P25	1
C2, 3, 8, 9, 17	Capacitor, 0.1μf		329372-1	5
C4, 6	Capacitor, 680pf		CM06FD681J03	2
C5	Capacitor, 0.015μf		235-1684P27	1
C10, 16, 18, 19, 20, 22	Capacitor, 10μf, 25V		333649-4	6
C11	Capacitor, 470pf		CM05CD471K3	1
C12	Capacitor, 0.33μf		235-1684P40	1
C13	Capacitor, 270pf		CM05CD271K3	1
C14	Capacitor, 1500pf		CM06FD152J03	1
C15	Capacitor, 150pf		CM05CD151K3	1
C21	Capacitor, 5μf, 150V		333649-7	1
C23	Capacitor, 47μf, 6V		426566-1	1
C24	Capacitor, 33μf, 25V		426566-2	1
C25	Capacitor, 470pf		CM06FD471J03	1
CR1 thru CR11	Diode		1N914	11
L1, 2, 3	Choke, 22μh		MS18130-24	3
Q1	Transistor		2N3643	1
Q2 thru Q5	Transistor		426565	1
Q6	Transistor		426567	1

MONOSCOPE DEFLECTION AMPLIFIER A3 ASSY 425098-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
R1	Resistor, 1K ±10% 1/2W	Raytheon	RC20GF102J	1
R2	Resistor, 20K ±5% 1/2W		RL20S203J	1
R3	Resistor, 27 ohm ±10%, 1/2W		RC20GF270J	1
R4,23,24	Resistor, 33K ±5% 1/2W		RL20S333J	3
R5,65,66	Resistor, 1.2K ±2% 1/2W		RL20S122G	3
R6,26	Resistor, 10K ±2% 1/2W		RL20S103G	2
R7	Var Resistor, 5K ±10%, 1/2W		240-1349P6	1
R8,19	Resistor, 470K ±10% 1/2W		RC20GF474J	2
R9,32	Resistor, 560 ohm ±10%, 1W		RC32GF561J	2
R10,31	Resistor, 750 ohm ±10%, 1W		RC32GF751J	2
R11,12,55, 61	Resistor, 5.1K ±5% 1/2W		RL20S512J	4
R13	Resistor, 1K ±5% 1/2W		RL20S102J	1
R14,15	Resistor, 15K ±5% 1/2W		RL20S153J	2
R16,21	Resistor, 200K ±10% 1/2W		333641-1	2
R17,18,20, 22	Resistor, 10K ±5% 2W		RL42S103J	4
R25,64	Resistor, 2K ±5% 1/2W		RL20S202J	2
R27			240-1349P6	1
R28	Resistor, 2.7K ±5% 1/2W		RL20S272J	1
R29			426576-2	1

MONOSCOPE DEFLECTION AMPLIFIER A3 ASSY 425098-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
R30	Resistor, 1.5K ±5% 1/2W	Raytheon	RC20GF152J	1
R33,34,42	Resistor, 4.7K ±5% 1/2W		RC20GF472J	3
R35	Resistor, 560 ohm ±5%, 1/2W		RL20S561J	1
R36,37	Var Resistor, 1K ±5%, 1/2W		426576-1	2
R38,40	Resistor, 2.2 ohm ±10%, 1/2W		RC20GF2R2J	2
R39	Resistor, 15 ohm ±10%, 1/2W		RC20GF150J	1
R41	Resistor, 10 ohm ±10%, 1/2W		RC20GF100J	1
R43	Resistor, 500K ±5%, 1/2W		240-1349P3	1
R44	Resistor, 1.2K ±5% 1/2W		RC20GF122J	1
R45	Resistor, 2.2K ±5% 1/2W		RC20GF222J	1
R46	Resistor, 300 ohm ±5%, 1/2W		RC20GF301J	1
R47,48	Resistor, 470 ohm ±5%, 1/2W		RC20GF471K	2
R49	Resistor, 390 ohm ±5%, 1/2W		RC20GF391J	1
R50	Resistor, 220 ohm ±5%, 1/2W		RC20GF221J	1
R51,76	Resistor, 60K ±10%, 1/2W		RN55C-6002-D	2
R52,58	Var Resistor		240-1349P2	2
R53,59	Resistor, 510 ohm ±5%, 1/2W		RL20S511J	2
R54,60	Resistor, 150 ohm ±5%, 1/2W		RL20S151J	2
R56,57,62, 63	Resistor, 10K ±5% 1/2W		RL20S103J	4

MONOSCOPE DEFLECTION AMPLIFIER A3 ASSY 425098-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
R71,75	Resistor, 30K ±10% 1/2W	Raytheon	RN55C-3002-C	2
R72,74	Resistor, 15K ±10% 1/2W		RN55C-1502-B	2
R73	Resistor, 7.5K ±10% 1/2W		RN55C-7501-B	1
R77	Resistor, 1 meg ±5%, 1/2W		RC20GF105J	1
VR1,2,3, 4	Diode		1N957A	4
VR5,6	Diode		1N942	2

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LVPS A4 ASSY 345723-1

Schematic 200-4030

Ref Desig	Description	Vendor	Vendor Part No.	Qty
C1	Capacitor, 0.0022μf 200V	Sorensen	24-2409-3	1
C2 a, b	Capacitor, 1.5μf 40V		24-2453-1	2
C4	Capacitor, 500μf 25V		24-2452-1	1
C5	Capacitor, 0.001μf 200V		24-2409-1	1
C6 a, b	Capacitor, 1.8μf 15V		24-2441-1	2
C7	Capacitor, 500μf 6V		24-2283-5	1
C8 a, b	Capacitor, 1.5μf 40V		24-2453-1	2
C9	Capacitor, 500μf 25V		24-2452-1	1
C10	Capacitor, 50μf 25V		24-2286-5	1
C11	Capacitor, 250μf 25V		24-2286-7	1
C12	Capacitor, 40μf 250V		24-2289-5	1
C13, 21	Capacitor, 0.0022μf 200V		24-2409-3	2
C14	Capacitor, 0.33μf 200V		24-2409-16	1
C15	Capacitor, 20μf 250V		24-2289-4	1
C16	Capacitor, 0.0022μf 200V		24-2409-3	1
C17	Capacitor, 0.0022μf 200V		24-2409-3	1
C18	Capacitor, 0.0022μf 200V		24-2409-3	1

LVPS A4 ASSY 345723-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
C19	Capacitor, 0.22μf 200V	Sorensen	24-2409-15	1
C20	Capacitor, 4.7μf 20V		24-2551	1
CR3 thru CR6	Rectifier, 3A, 100V PIV		26-1006-2	4
CR7, 8	Rectifier, 3A, 50V PIV		26-1006-1	2
CR9 thru CR12	Rectifier, 3A, 100V PIV		26-1006-2	4
CR13, 14	Rectifier, 0.75A, 100V PIV		26-158-1	2
CR15 thru CR18	Rectifier, 0.75A, 600V PIV		26-857	4
CR19	Rectifier, 0.75A, 100V PIV		26-158-1	1
CR20	Rectifier, 0.1A, 50V PIV		26-1017	1
CR21	Rectifier		26-1061	1
F1	Fuse, 4A, 250V		42-847	1
Q1	Transistor, 2N697		18-161-2	1
Q2	Transistor, 40312		18-142	1
Q3	Transistor, 2N3641		18-144	1
Q4, 5	Transistor, 2N3641		18-144	2
Q6	Transistor, 2N3055		18-151	1
Q7	Transistor, 2N3641		18-144	1
Q8	Transistor, 40312		18-142	1
Q9	Transistor, 2N3055		18-151	1
Q10	Transistor, 2N3641		18-144	1
Q11, 12	Transistor, 2N3641		18-144	2
Q13	Transistor, 2N697		18-161-2	1
Q14	Transistor, 40312		18-142	1
Q15	Transistor, 2N3055		18-151	1

LVPS A4 ASSY 345723-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
Q16	Transistor, 2N3641	Sorensen	18-144	1
Q17, 18	Transistor, 2N3641		18-144	2
Q19	Transistor, 2N3641		18-144	1
Q20	Transistor, 2N3583		18-168	1
Q21	Transistor, 2N3641		18-144	1
Q22, 23	Transistor, 2N3641		18-144	2
Q24	Transistor, RT9338		18-146	1
Q25	Transistor, 2N3638		18-143	1
R1	Resistor, 100K, 1/2W		27-117	1
R2	Resistor, 6.8K, 1/2W		27-185	1
R3	Resistor, 1.8K, 1/2W		27-192	1
R4	Resistor, 220 ohm 1/2W		27-101	1
R6	Resistor, 0.47 ohm 3W		27-397-17	1
R7	Resistor, 10K, 1/2W		27-133	1
R8	Resistor, 22K, 1/2W		27-142	1
R9	Resistor, 10K, 1W		27-212	1
R10	Resistor, 10K, 3W		27-398-22	1
R11	Potentiometer, 5K, 2W		29-505-4	1
R12	Resistor, 1.5K, 3W		27-398-2	1
R13	Resistor, 22K, 1W		27-270	1
R14	Resistor, 680 ohm 1/2W		27-156	1
R15	Resistor, 330 ohm 1/2W		27-102	1
R16	Resistor, 68 ohm 1/2W		27-160	1
R18	Resistor, 18 ohm 7W		27-470-7	1
R19	Resistor, 1.5K, 1/2W		27-171	1
R20	Resistor, 22K, 1/2W		27-142	1
R21	Resistor, 6.8K, 3W		27-398-18	1

LVPS A4 ASSY 345723-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
R22	Potentiometer 400 ohm, 2W	Sorensen	29-505-5	1
R23	Resistor, 120K, 1/2W		27-1179	1
R24	Resistor, 6.8K, 1/2W		27-185	1
R25	Resistor, 1.8K, 1/2W		27-176	1
R26	Resistor, 220 ohm 1/2W		27-101	1
R27	Resistor, 0.47 ohm, 3W		27-397-17	1
R28	Resistor, 12K, 1W		28-734	1
R29	Resistor, 6.8K 1/2W		27-185	1
R30	Resistor, 2.2K, 1/2W		27-152	1
R31	Resistor, 820 ohm 1/2W		27-182	1
R32	Resistor, 1K, 3W		27-397-97	1
R33	Potentiometer, 400 ohm 2W		29-518-1	1
R34	Resistor, 300 ohm, 3W		27-397-84	1
R35	Resistor, 47K, 1/2W		27-112	1
R36	Resistor, 100K, 1/2W		27-117	1
R37	Resistor, 1.5K, 1/2W		27-171	1
R39	Resistor, 3.9 ohm, 3W		27-397-39	1
R40	Resistor, 22K, 1/2W		27-142	1
R41	Resistor, 22K, 1/2W		27-142	1
R42	Resistor, 180 ohm 1/2W		27-190	1
R43	Resistor, 330 ohm 1/2W		27-102	1
R44	Resistor, 1K, 1/2W		27-103	1
R45	Resistor, 510 ohm 3W		27-397-90	1
R46	Potentiometer 400 ohm, 2W		29-518-1	1

LVPS A4 ASSY 345723-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
R47	Resistor, 10K, 3W	Sorensen	27-398-22	1
R48	Resistor, 3.3K, 3W		27-398-10	1
R49	Resistor, 10K, 1/2W		27-133	1
R50	Resistor, 15K, 1/2W		27-179	1
R51	Resistor, 3.9K, 1/2W		27-186	1
R52	Resistor, 470 ohm, 3W		27-397-89	1
R53	Resistor, 10K, 1/2W		27-133	1
R54	Resistor, 12K, 1/2W		27-1108	1
R55	Resistor, 1.5K, 1/2W		27-171	1
R56	Resistor, 6.8K, 3W		27-398-18	1
R57	Resistor, 274 ohm ±1%, 1/4W		28-1227	1
R58	Resistor, 28 ohm ±1%, 1/4W		28-1247	1
R59	Resistor, 182 ohm 1/4W		28-1222	1
R60	Resistor, 680 ohm 1/2W		27-156	1
R61	Resistor, 180 ohm 1/2W		27-190	1
R62	Resistor, 6.8 ohm 1/2W		27-1126	1
R63	Resistor, 470 ohm, 3W		27-397-89	1
T1	Transformer		126-2980	1
Z2	Zener Diode, 1N751A		26-204	1
Z3	Zener Diode, 1N751A		26-204	1
Z4	Zener Diode, 1N751A		26-204	1
Z5	Zener Diode, 1N746A		26-251	1

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HVPS A5 ASSY 345724-1

Schematic 200-4041

Ref Desig	Description	Vendor	Vendor Part No.	Qty
C1,2	Capacitor, 25μf 25VDC	Sorensen	24-2279-10	2
C3	Capacitor, 50μf, 50VDC		24-2280-12	1
C4	Capacitor, 0.47μf 100VDC		24-2473	1
C5	Capacitor, 4.7μf 20V		24-2551	1
C6	Capacitor, 0.047μf 200V		24-2409-11	1
C7	Capacitor, 100μf 50V		24-2442	1
C8,9	Capacitor, 47μf 10V		24-2012	2
C10,11	Capacitor, 0.047μf 1600V		24-2474	2
C12	Capacitor, 0.02μf 10KV		24-2146	1
C13	Capacitor, 0.02μf 5KV		24-2147	1
C14	Capacitor, 0.01μf 15KV		24-2148	1
C15	Capacitor, 0.015μf 1000V		24-2475	1
CR1,2	Rectifier, RD 9119		26-1017	2
CR3	Reference Diode 1N936		26-238	1
CR4	Reference Diode 1N750A		26-211	1
CR5	Rectifier, CER 68		26-158-1	1
CR6,7	Rectifier, CER 68		26-158-1	2
CR8 thru CR11	Rectifier, SLA-02		26-1044	4

HVPS A5 ASSY 345724-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
CR12 thru CR14	Rectifier, 5SN10	Sorensen	26-1058	3
CR15	Rectifier, DD9119		26-1017	1
Q1	Transistor, 40312		18-142	1
Q2	Transistor, RT9343		18-145	1
Q3	Transistor, 2N3638		18-143	1
Q4	Transistor, 2N3641		18-144	1
Q5,6	Transistor, 2N3904		18-166	2
Q7	Transistor, 2N3641		18-144	1
Q8,9	Transistor, 40346		18-167	2
Q10,11	Transistor, 2N3441		18-157	2
R1	Resistor, 270 ohm 1/2W		27-191	1
R2	Resistor, 1.5K ohm 1/2W		27-171	1
R3	Resistor, 2.7 ohm 2W		28-1242	1
R4	Potentiometer 2.5K ohm, 2W		29-505-3	1
R5	Resistor, 1.74K ohm 1/2W		28-1243	1
R6	Resistor, 3.3K ohm 1W		27-292	1
R7	Resistor, 33K ohm 1/2W		27-163	1
L1	Filter, Choke		127-1791	1
R8	Resistor, 1K ohm 1W		27-297	1
R9	Resistor, 4.7K ohm 1/2W		27-107	1
R10	Resistor, 560 ohm 1/2W		27-1103	1
R11	Resistor, 825 ohm 1/2W		28-1217	1

HVPS A5 ASSY 345724-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
R12	Resistor, 22.6K ohm 1/2W	Sorensen	28-1244	1
R13	Potentiometer 5K ohm, 1W		29-514	1
R14	Resistor, 180 ohm 1/2W		27-190	1
R15	Resistor, 6.8K ohm 1/2W		27-185	1
R16, 17	Resistor, 56 ohm 1/2W		27-1158	2
R18	Resistor, 3.3K ohm 1W		27-292	1
R19	Resistor, 2.2K ohm 1W		27-290	1
R20 a, b	Resistor, 1.5M ohm 2W		28-1219	2
R21	Resistor, 0.15M ohm 1/2W		28-525	1
R22	Resistor, 10K ohm 1W		27-212	1
R23	Resistor, 2.7K ohm 7W		27-471-8	1
R24 a, b	Resistor, 30M ohm 2W		28-1245	2
R25	Resistor, 4.75M ohm 1W		28-1246	1
T1	Transformer		126-2981	1
T2	Transformer		126-2960	1

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HV NETWORK A6 ASSY 387926-1

Schematic 349030

Ref Desig	Description	Vendor	Vendor Part No.	Qty
C1	Capacitor	Raytheon	235-1684P37	1
	HV Panel		387925-1	1
R1	Resistor, 15K ±5%, 1W		RL32S153J	1
R2	Resistor, 100K ±5%, 2W		240-1316P2	1
R3	Resistor, 330K ±5%, 1W		RL32S334J	1
R4	Resistor, 500K ±5%, 2W		240-1316P24	1
R5,6,7	Resistor, 430K ±5%, 1W		RL32S434J	3
R8	Resistor, 47K ±5%, 1/2W		RL20S473J	1
R9	Resistor, 5 meg ±5%, 2W		240-1316P31	1
R10	Resistor, 33K ±5%, 1/2W		RC20GF333J	1
R11	Resistor, 51K ±5%, 1/2W		RL20S513J	1
R12	Resistor, 470K ±5%, 1/2W		RL20S474J	1

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PREAMPLIFIER A7 ASSY 425104-1

Schematic 425105

Ref Desig	Description	Vendor	Vendor Part No.	Qty
A1	Wideband Video Ampl	Texas Instr	SN7510L	1
C1	Capacitor, 10μf	Raytheon	426564	1
C2,4	Capacitor, 0.1μf		329372-1	2
C3	Capacitor, 47μf		426566-1	1
L1	Choke, 15μh		375-2016P21	1
R1	Resistor, 6.8K ±5%, 1/2W		RC07GF682J	1
R2	Resistor, 560 ohm ±5%, 1W		RC32GF561J	1
R3	Resistor, 1K ±5%, 1/4W		RC07GF102J	1
R4,6	Resistor, 4.7K ±5%, 1/4W		RL07S472J	2
R7	Resistor, 6.8K ±5%, 1/4W		RL07S682J	1
R8	Resistor, 100 ohm ±5%, 1/4W		RL07S101J	1
R9	Resistor, 750 ohm ±5%, 1W		RC32GF751J	1
R10	Resistor, 68 ohm ±5%, 1/4W		RC07GF680J	1
VR1,2	Diode		1N957A	2

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VIDEO AMPLIFIER A8 ASSY 425101-1

Schematic 425102

Ref Desig	Description	Vendor	Vendor Part No.	Qty
	PC Board	Raytheon	425101-2	1
A1	Wideband Video Ampl	Raytheon Texas Instr	405032 SN7510L	1
C1,2,3	Capacitor, 0.1μf		329372-1	3
C4,5	Capacitor, 5μf		333649-7	2
C6	Capacitor, 0.47μf		426572	1
C7	Capacitor		CM05FD151J03	1
CR1,2	Diode		1N914	2
CR3,4	Diode		1N4384	2
L1	Choke, 10μh		375-2016P19	1
L2	Choke, 4.7μh		375-2016P15	1
Q1	Transistor		2N3735	1
Q2,3	Transistor		426565	2
R1	Resistor, 560 ohm ±5%, 1W		RC32GF561J	1
R2	Resistor, 390 ohm ±5%, 1/2W		RC20GF391J	1
R3	Resistor, 1.8K ±5%, 1/4W		RC07GF182J	1
R4	Resistor, 270 ohm ±5%, 1/4W		RC07GF271J	1
R5,7	Resistor, 100 ohm ±2%, 1/4W		RL07S101G	2
R6	Resistor, 4.7K ±2%, 1/4W		RL07S472G	1
R8	Resistor, 750 ohm ±5%, 1W		RC32GF751J	1
R9	Resistor, 390K ±5%, 1/4W		RC07GF394J	1
R10	Resistor, 5.6K ±5%, 1/4W		RC07GF562J	1
R11	Resistor, 1K ±2%, 1W		RL32S102G	1

VIDEO AMPLIFIER A8 ASSY 425101-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
R12,13	Resistor, 22K ±5%, 1/4W	Raytheon	RC07GF223J	2
R14	Resistor, 100K ±5%, 1/4W		RC07GF104J	1
R15	Resistor, 560K ±5%, 1/4W		RC07GF564J	1
R16	Resistor, 150K ±5%, 1/4W		RC07GF154J	1
R17	Resistor, 68 ohm ±5%, 1/4W		RC07GF680J	1
R18	Resistor, 4.3K ohm ±5%, 1/4W		RC07GF432J	1
R19	Resistor, 10K ohm 1/2W		240-1349P7	1
VR1,3	Diode, 6.8V		1N957A	2
VR2	Diode, 15V		1N965A	1

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DELAY LINE ELECTRONICS A9 ASSY 387068-1

Schematic 389280

Ref Desig	Description	Vendor	Vendor Part No.	Qty
	PC Board	Raytheon	387068-2	1
A1, 2	Wideband Ampl	RCA	CA3012	2
A3	Dual-D Type Edge-Triggered F/F	Texas Instr	SN7474N	1
A4	Quadruple 2-input NAND gate		SN7400N	1
A5, 6	Audio Power Ampl	RCA	CA3020	2
C1, 8	Capacitor, 0.01μf	Raytheon	235-1684P25	2
C2, 4, 5, 7, 9	Capacitor, 0.1μf 25V			5
C3, 6	Capacitor, 1 μf, 6V			2
C10, 11, 12	Capacitor, 10μf, 6V			3
C13, 14	Capacitor, 0.0068μf		235-1684P23	2
C15	Capacitor, 10μf 25V		333649-4	1
L1, 2, 3	Choke, 22μh		375-2011P17	3
R1, 2	Resistor, 3.0K ±5%		RC20GF302J	2
R3, 10, 11 13, 14	Resistor, 430 ohm ±5%, 2W		RC42GF431J	5
R4, 5	Resistor, 3.9K ±5%		RC20GF392J	2
R6, 7, 8, 9	Resistor, 1.5K ±5%		RC20GF152J	4
R12, 15	Resistor, 12 ohm ±5%		RC20GF120J	2
R16	Resistor, 24 ohm ±5%		RC20GF240J	1
VR1	Diode		1N4370A	1

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KEYBOARD A11 ASSY 387188-1

Ref Desig	Description	Vendor	Vendor Part No.	Qty
	Keyboard and Matrix	NAVCOR	C28490	1

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COMMUNICATIONS CONTROL BOARD A12 ASSY 408024-1

Schematic 408025

Ref Desig	Description	Vendor	Vendor Part No.	Qty
	PC Board		408024-2	1
A1, 18, 21 25, 29, 39, 41, 45, 49, 51, 55, 59, 61, 69, 70, 73, 78, 80	Quad 2-Input		385710-2	18
A10, 22, 23, 24, 40, 47, 48, 50, 62, 64, 82	Triple 3-Input		385712-2	11
A2 thru A6, 9, 12, 26, 37, 63, 72	Dual 4-Input		385-714-2	11
A74, 75, 76, 83, 84	8-Input Gate		385716-2	5
A8, 11, 15, 16, 19, 34, 35, 43, 53, thru A57, 81	Triple 3-Input		385729-2	13
A7, 14, 27, 38, 58, 77	Dual 4-Input		385718-2	6
A17, 46, 79	Dual JK Flip-Flop		385739-2	3
A30, 32, 42	JK Flip-Flop		385737-2	3
A13, 20, 28, 31, 33, 36, 44, 52, 60, 65 thru 68 A68	Dual D Type		385740-2	13
C1 thru C8	Capacitor		333649-4	8
L1 thru L8	Choke, 22μh		375-2011P17	8

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DISPLAY LOGIC A13 ASSY 407992-1

Schematic 407993

Ref Desig	Description	Vendor	Vendor Part No.	Qty
	PC Board		407992-2	1
A1, 39, 55 59	4-Input		385714-2	4
A2, 3, 4, 12 19, 20, 36, 48, 49, 58 64	8-Input		385716-2	11
A5, 13, 14, 25, 32, 33, 38, 41, 56, 62, 63, 65, 66, 70, 71, 72, 73, 74, 77, 78	Dual D		385740-2	20
A6, 22, 24, 45, 46, 50	3-Input		385712-2	6
A7, 9, 11, 15, 16, 17, 23, 26, 29, 31, 42, 43, 47, 51, 54, 60, 61, 67, 68, 69, 80	2-Input		385710-2	21
A8, 21, 30 40, 75	Dual JK		385739-2	5
A10, 27, 28, 34, 35, 52, 53, 76	3-Input		385729-2	8
A18, 57, 79	4-Input		385718-2	3
A37, 44	4-Bit Binary Counter		385863-2	2
C1 thru C8	Capacitor		333649-4	8
CR1 thru CR9	Diode		1N914	9
Q1 thru Q9	Transistor		2N3643	9
R1 thru R9	Resistor, 10K ohm ±5%, 1/4W		RC07GF103J	9

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TIMING AND DISCRETE BOARD A14 ASSY 407981-1

Schematic 407905

Ref Desig	Description	Vendor	Vendor Part No.	Qty
	PC Board	Raytheon	407981-2	1
A1, 3, 8, 12, 13, 18, 28, 30, 39, 40, 43, 44	Quad 2-Input	Texas Instr Raytheon	SN400N 385710-2	12
A7, 22, 25 38	Triple 3-Input	Texas Instr Raytheon	SN74H11N 385712-2	4
A2, 9, 17, 23, 29, 31, 35, 41	Triple 3-Input	Texas Instr Raytheon	SN7410N 385729-2	8
A4, 5, 6, 10 11, 15, 16, 19, 20, 26, 27, 32, 33	Dual JK	Texas Instr Raytheon	SN7473N 385739-2	13
A14, 21	Dual 4-Input	Texas Instr Raytheon	SN7420N 385714-2	2
A24, 45	Buffer	Texas Instr Raytheon	SN7443N 385718-2	2
A36, 37	4-Bit Counter	Texas Instr Raytheon	SN7493N 385863-2	2
A34	Dual D	Texas Instr Raytheon	SN7474N 385740-2	1
C1 thru C5, C20	Capacitor, 10μf 25V	Raytheon	333649-4	6
C6, 7, 15	Capacitor, 10μf 50V		CS13AG100K	3
C8, 9	Capacitor, 0.015μf		235-1684P27	2
C10, 13, 21	Capacitor, 220pf		235-1535P35	3
C11, 12	Capacitor, 1.2μf		CS13BF125K	2
C14	Capacitor, 470pf		235-1535P44	1
C16, 19	Capacitor, 0.022μf		235-1684P29	2
C17	Capacitor, 200pf		235-1535P34	1
C18	Capacitor, 160pf		235-1535P32	1

TIMING AND DISCRETE BOARD A14 ASSY 407981-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
CR1 thru CR13	Diode	Raytheon	1N914	13
L1 thru L7, 9, 10	Choke, 22μh		375-2011P17	9
L8	Choke		375-2184P8	1
Q1,2,4,5, 8,10,11, 12,13,16, 17,19,20	Transistor		2N3643	13
Q3,6,14	Transistor		TN53	3
Q7,9,18	Transistor		2N3638	3
Q15	Transistor		2N3563	1
R1,10	Resistor, 1K ±5%, 1/2W		RC20GF102J	2
R2,11	Resistor 2.2K ±2%, 1/2W		RL20S222G	2
R3,12	Resistor, 2.7K ±2%, 1/2W		RL20S272G	2
R4,13	Resistor, 10K ±2%, 1/2W		RL20S103G	2
R5,14	Resistor, 470 ohm ±5%, 1/2W		RC20GF471J	2
R6,15,27, 36	Resistor, 3.3K ±5%, 1/2W		RC20GF332J	4
R7,16	Resistor, 22K ±5%, 1/2W		RC20GF223J	2
R8,17	Resistor, 620K ±5%, 1W		RC32GF621J	2
R9,18	Resistor, 1.8K ±5%, 1W		RC32GF182J	2
R19,28	Resistor, 47K ±5%, 1/4W		RC07GF473J	2
R20,29	Resistor, 750K ±5%, 1/4W		RC07GF754J	2
R21,26,30, 35	Resistor, 33K ±5%, 1/4W		RC07GF333J	4

TIMING AND DISCRETE BOARD A14 ASSY 407981-1 (Continued)

Ref Desig	Description	Vendor	Vendor Part No.	Qty
R22,31	Resistor, 100 ohm ±5%, 1/2W	Raytheon	RC20GF101J	2
R23,32	Resistor, 75K ±5%, 1/4W		RC07GF753J	2
R24,25,33, 34	Resistor, 4.7K ±5%, 1/2W		RC20GF472J	4
R37,39,42, 44	Resistor, 68K ±5%, 1/4W		RC07GF683J	4
R38,43,56, 63	Resistor, 6.8K ±5%, 1/4W		RC07GF682J	4
R40,41	Resistor, 82K ±5%, 1/4W		RC07GF823J	2
R45,51,52, 68	Resistor, 2.2K ±5%, 1/4W		RC07GF222J	4
R46,49,54, 67,70	Resistor, 1K ±5%, 1/4W		RC07GF102J	5
R47	Resistor, 3.3K ±5%, 1/4W		RC07GF332J	1
R48,62	Resistor, 22K ±5%, 1/4W		RC07GF223J	2
R50	Resistor, 18 ohm ±5%, 1/4W		RC07GF180J	1
R53	Resistor, 150 ohm ±5%, 1/4W		RC07GF151J	1
R55,57,58, 59	Resistor, 18K ±5%, 1/4W		RC07GF183J	4
X1	Crystal		386178-1	1
R60,61	Resistor, 10K ±5%, 1/4W		RC07GF103J	2
R64	Resistor, 5.6K ±5%, 1/4W		RC07GF562J	1
R65,66	Resistor, 100 ohm ±5%, 1/4W		RC07GF101J	2
R69	Resistor, 2K 1/2W		345262-3	1
R71	Resistor, 2K ±5%, 1/4W		RC07GF202J	1

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DELAY LINE A15 ASSY 386177-1

Ref Desig	Description	Vendor	Vendor Part No.	Qty
A15	Delay Line	Raytheon	344947-1	1

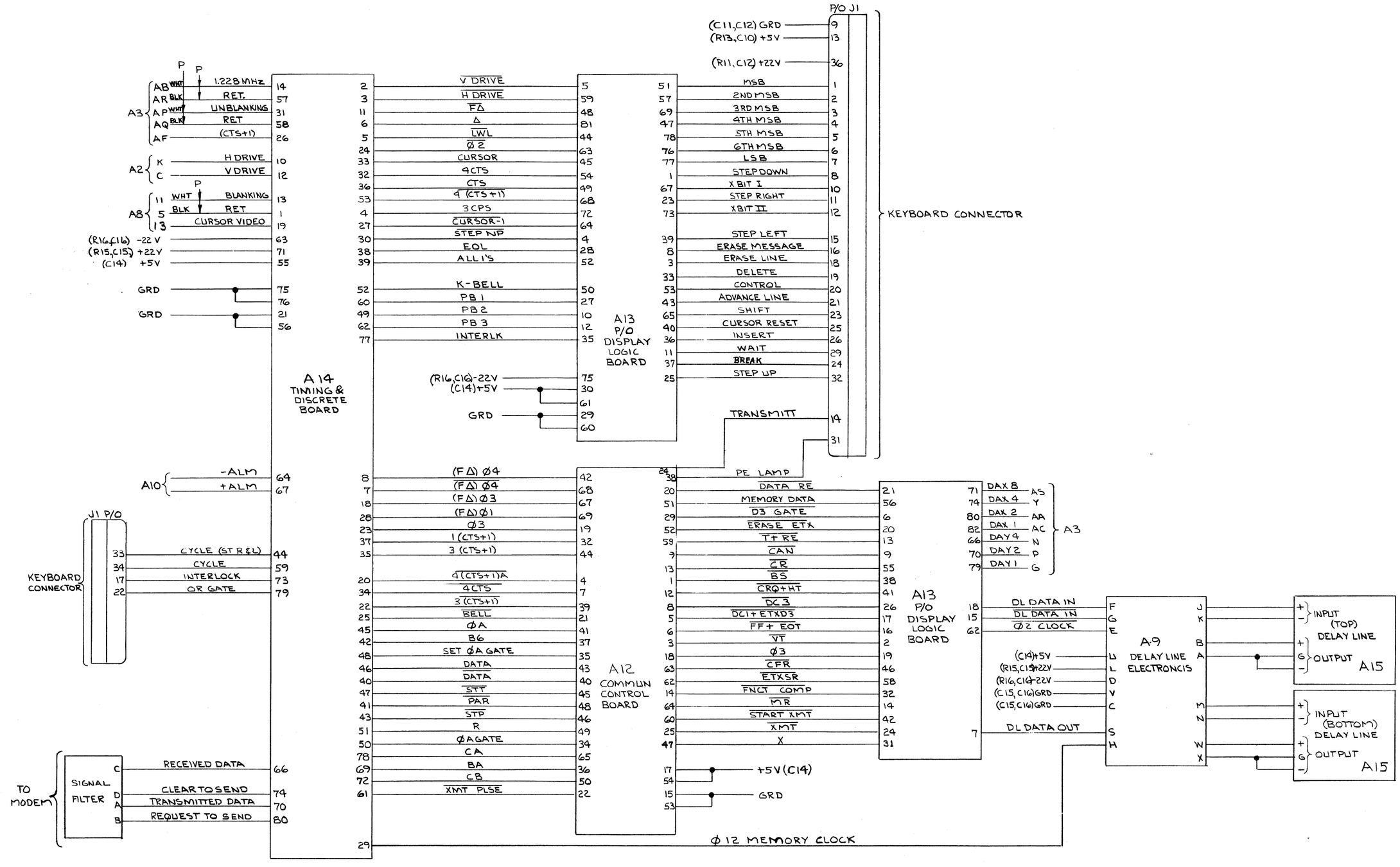
CHAPTER 7

MASTER DRAWINGS

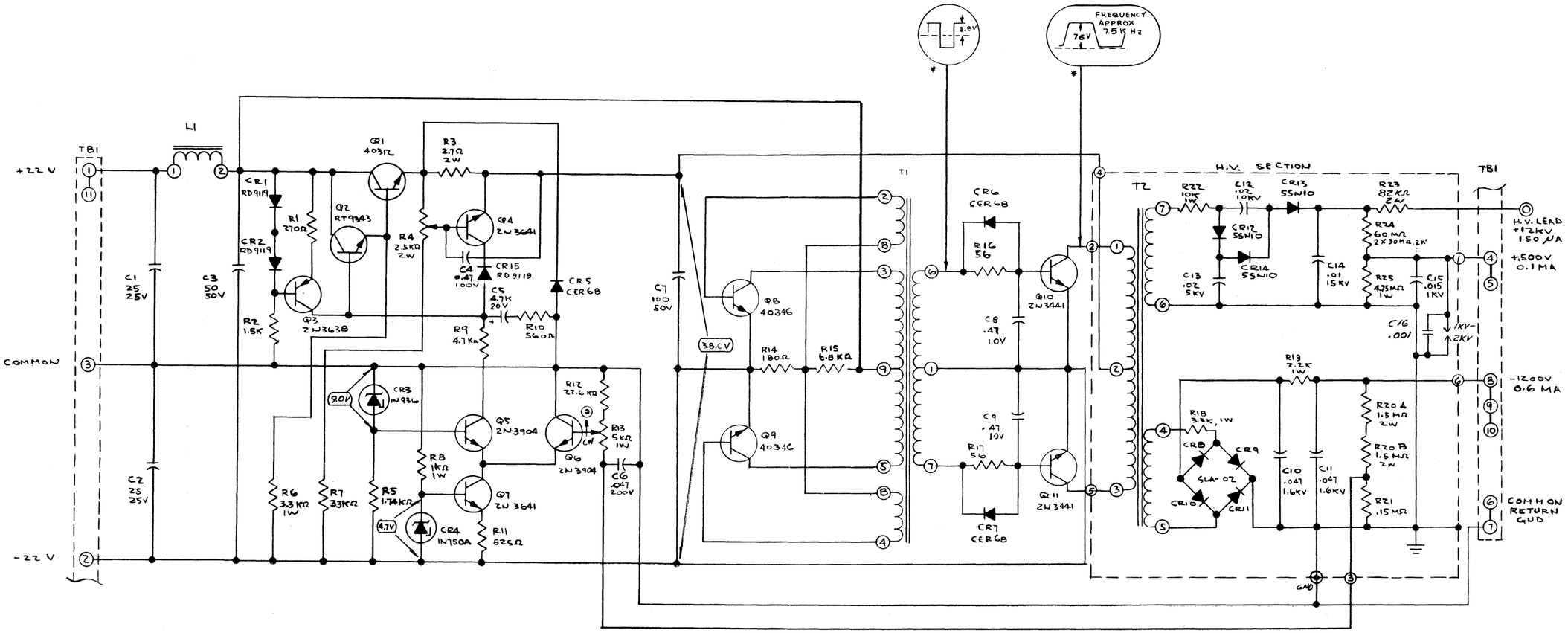
This chapter provides detailed logic and schematic diagrams of all digital and analog boards contained in the Display Terminal. Also included are Raytheon master parts layout drawings which identify the location of all components contained on each board.

The Raytheon Master Drawings in this chapter are provided as an aid to troubleshooting and are supplemented by circuit descriptions and simplified diagrams contained in earlier chapters.

The drawings contained in this chapter are arranged in numerical sequence according to board reference designations, except for Communications Control Board Assembly 408025, which is in a folder at the back of the book.



Display Console Interconnection
Schematic 425116



NOTES:

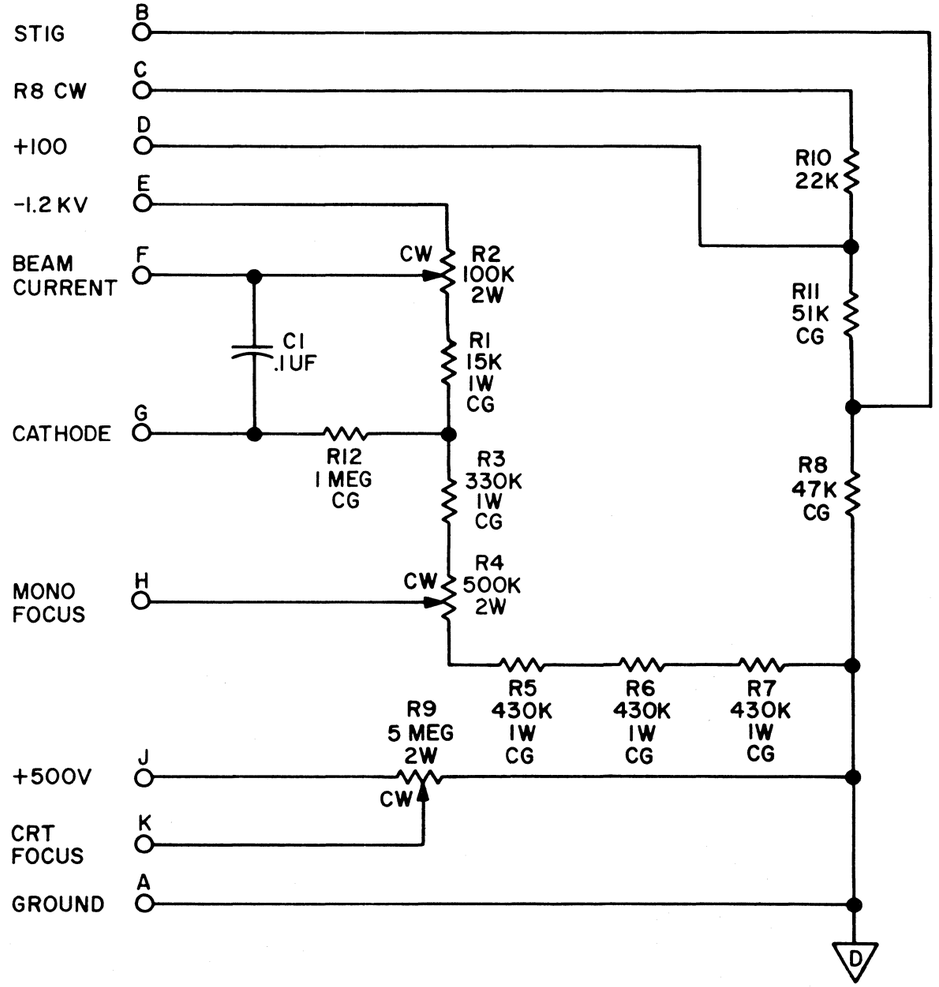
1- ALL VALUES EXPRESSED IN OHMS OR MICROFARADS UNLESS OTHERWISE SPECIFIED.

2- ALL VOLTAGES MEASURED AT NOMINAL INPUT, NOMINAL OUTPUT, AND NO LOAD.

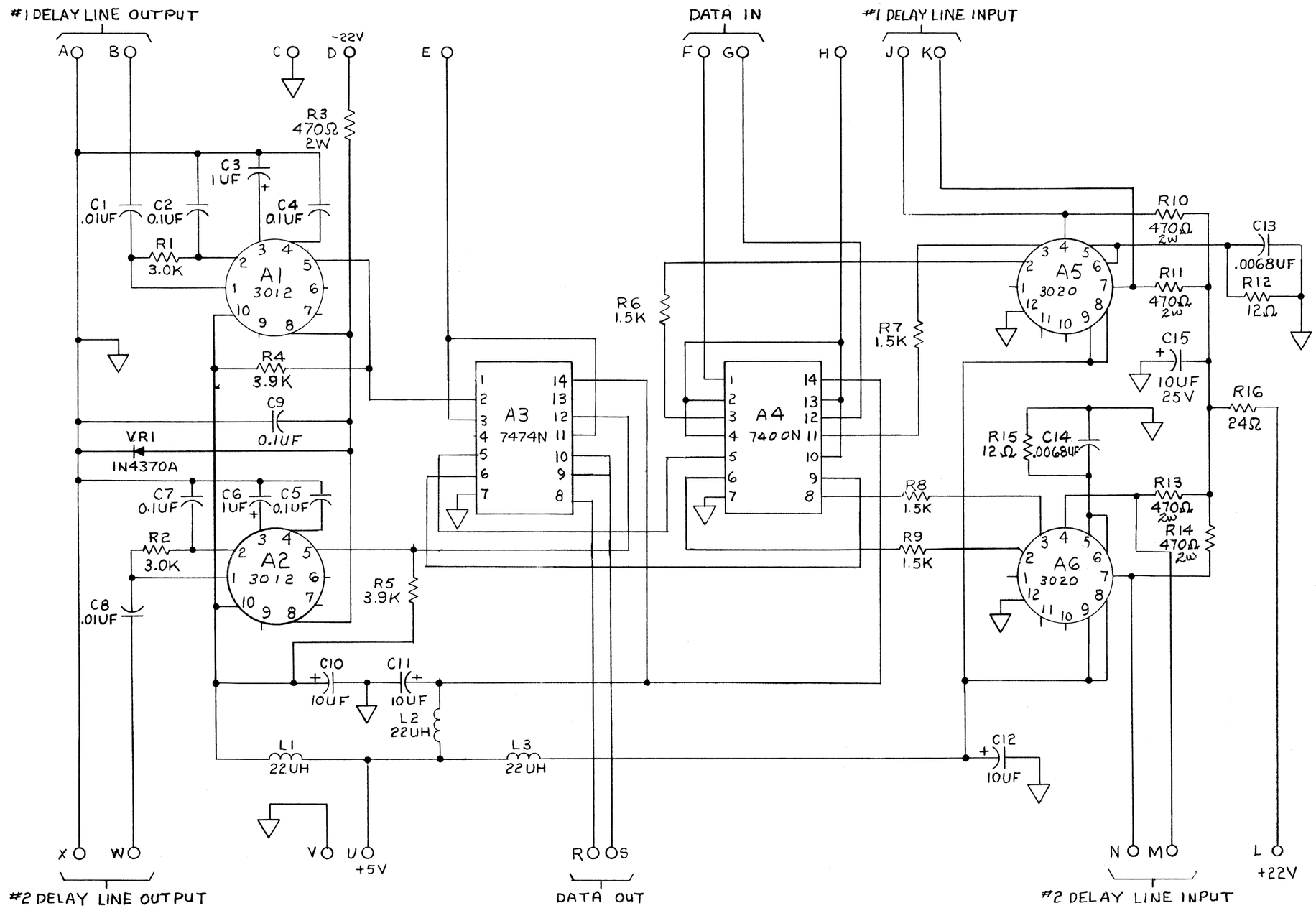
3- ⓞ DENOTES OUTPUT ADJUST.

4- MEASURE BETWEEN -22V LINE AND POINT INDICATED.

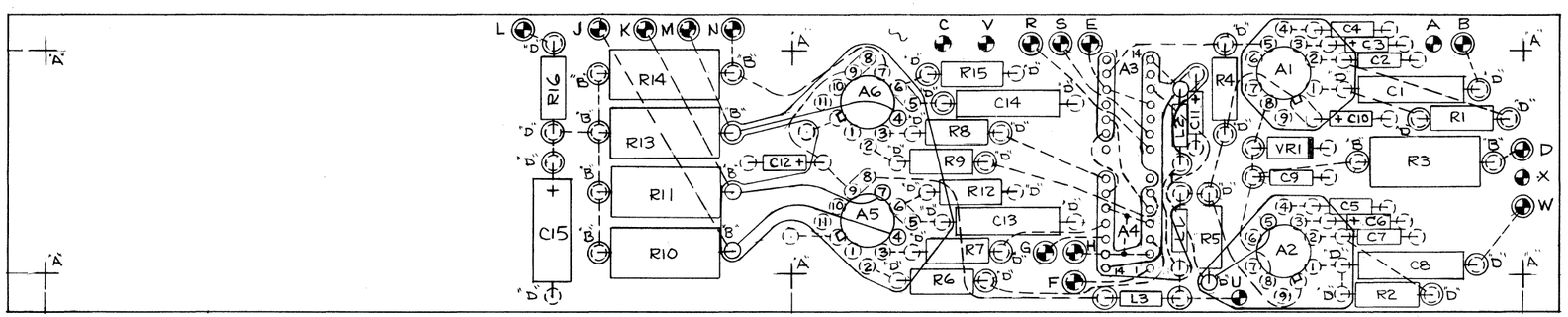
A5, High Voltage Power Supply Assembly
Schematic 2004041

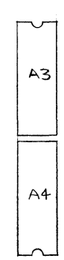


A6, High Voltage Network
Assembly Schematic 349030



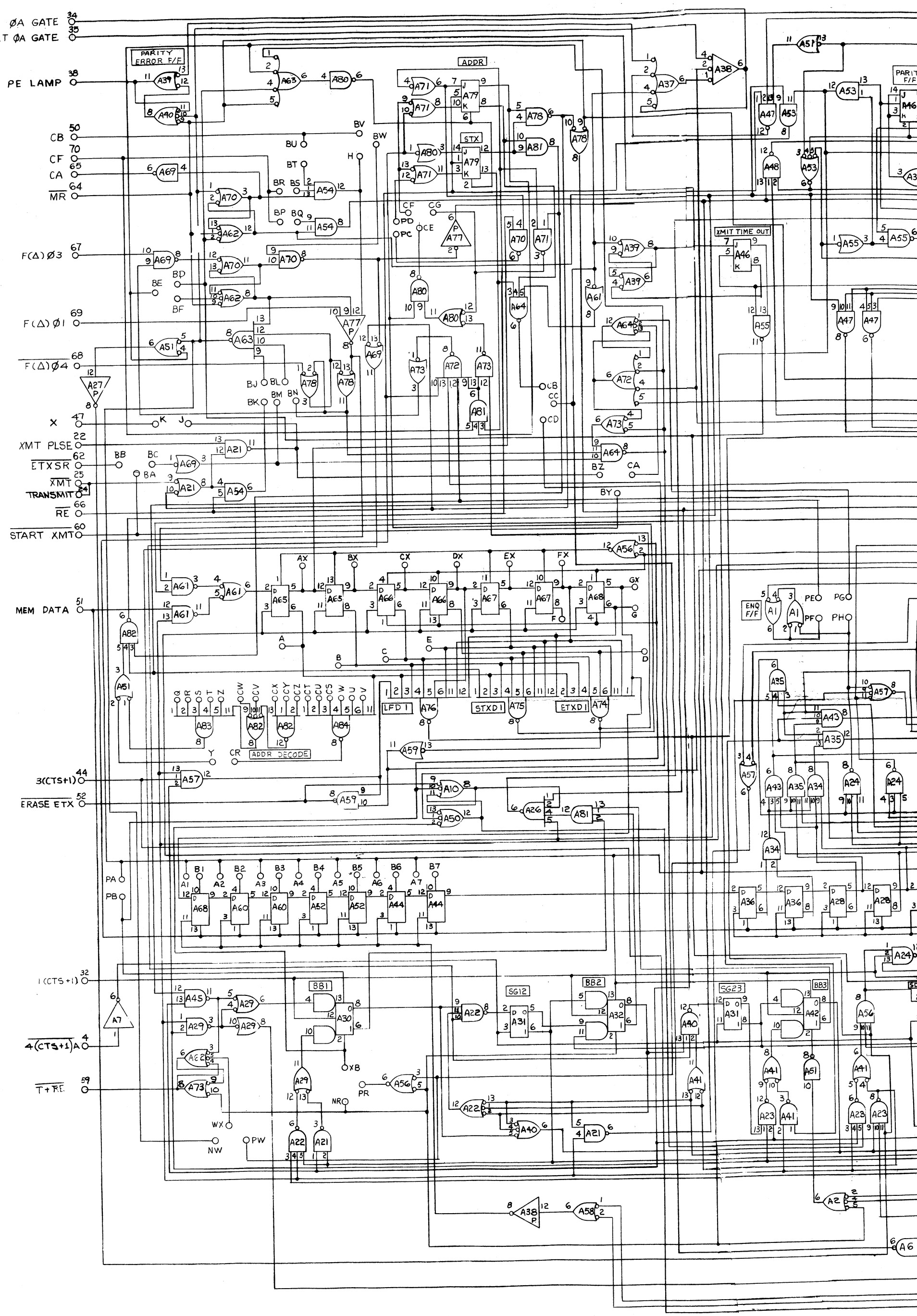
A9, Delay Line Electronics
Schematic 389280

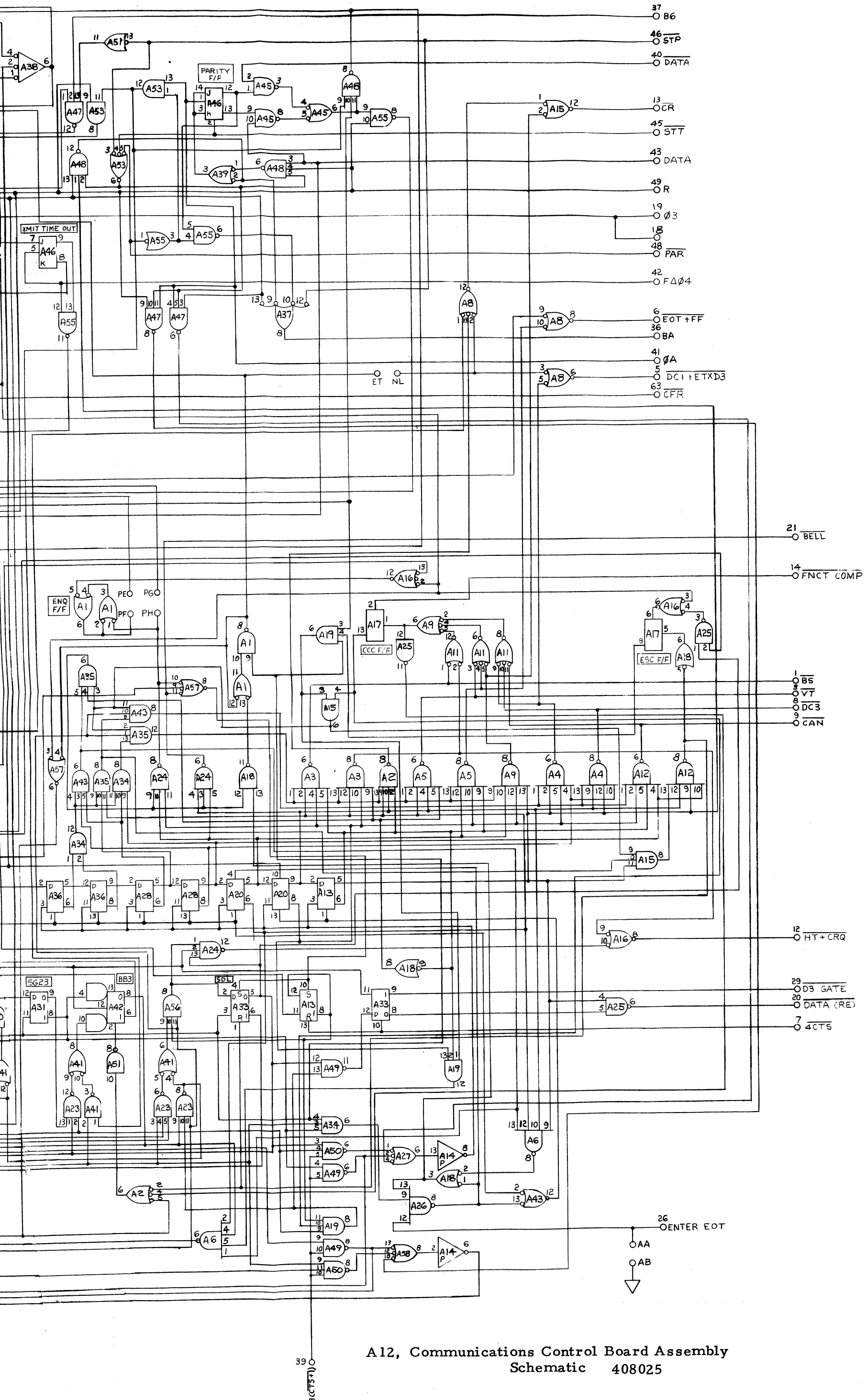




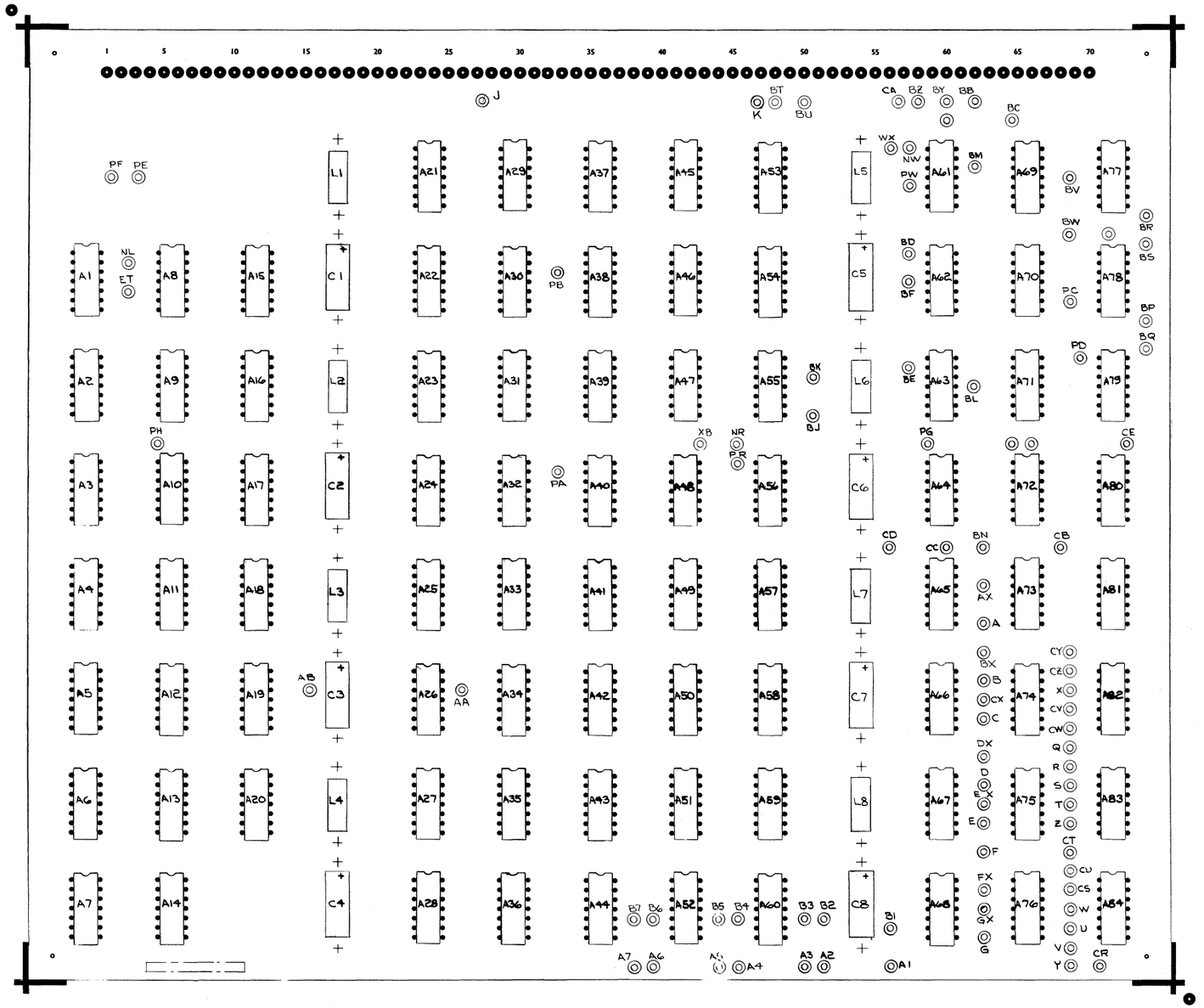
TYP POSITION
FOR A3, A4

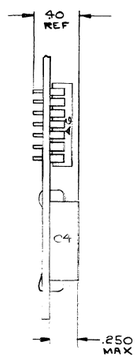
A9, Delay Line Electronics
Parts Layout 387068


ØA GATE
SET ØA GATE
PE LAMP
CB
CF
CA
MR
F(Δ)Ø3
F(Δ)Ø1
F(Δ)Ø4
X
XMT PLSE
ETXSR
XMT
TRANSMIT
RE
START XMT
MEM DATA
3(CTS+1)
ERASE ETX
1(CTS+1)
4(CTS+1)A
T+RE
PARITY ERROR F/F
ADDR
STX
XMIT TIME OUT
ENQ F/F
LFD 1
STXD 1
ETXD 1
ADDR DECODE
BB1
BB2
BB3
SG12
SG23

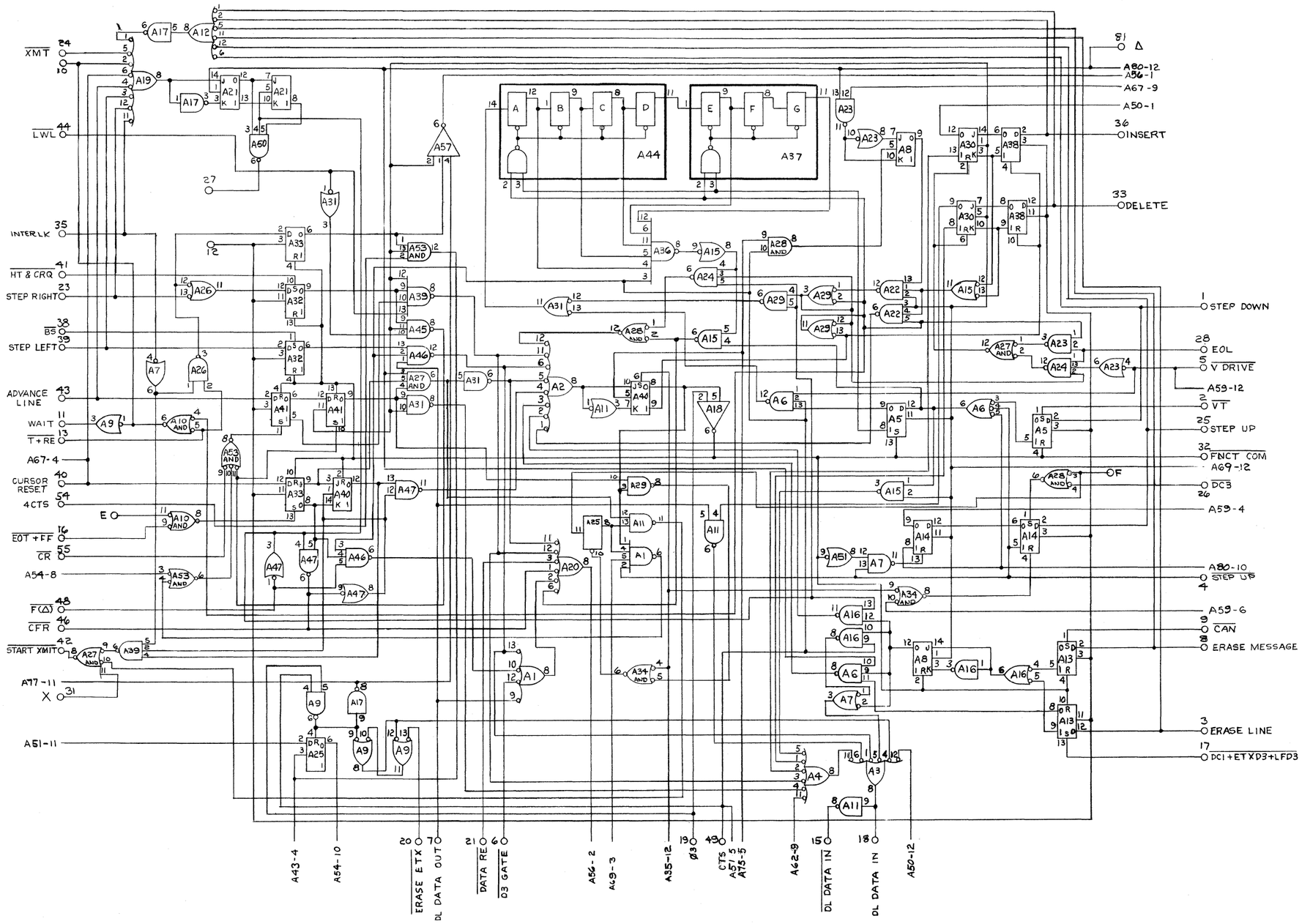


A12, Communications Control Board Assembly
Schematic 408025

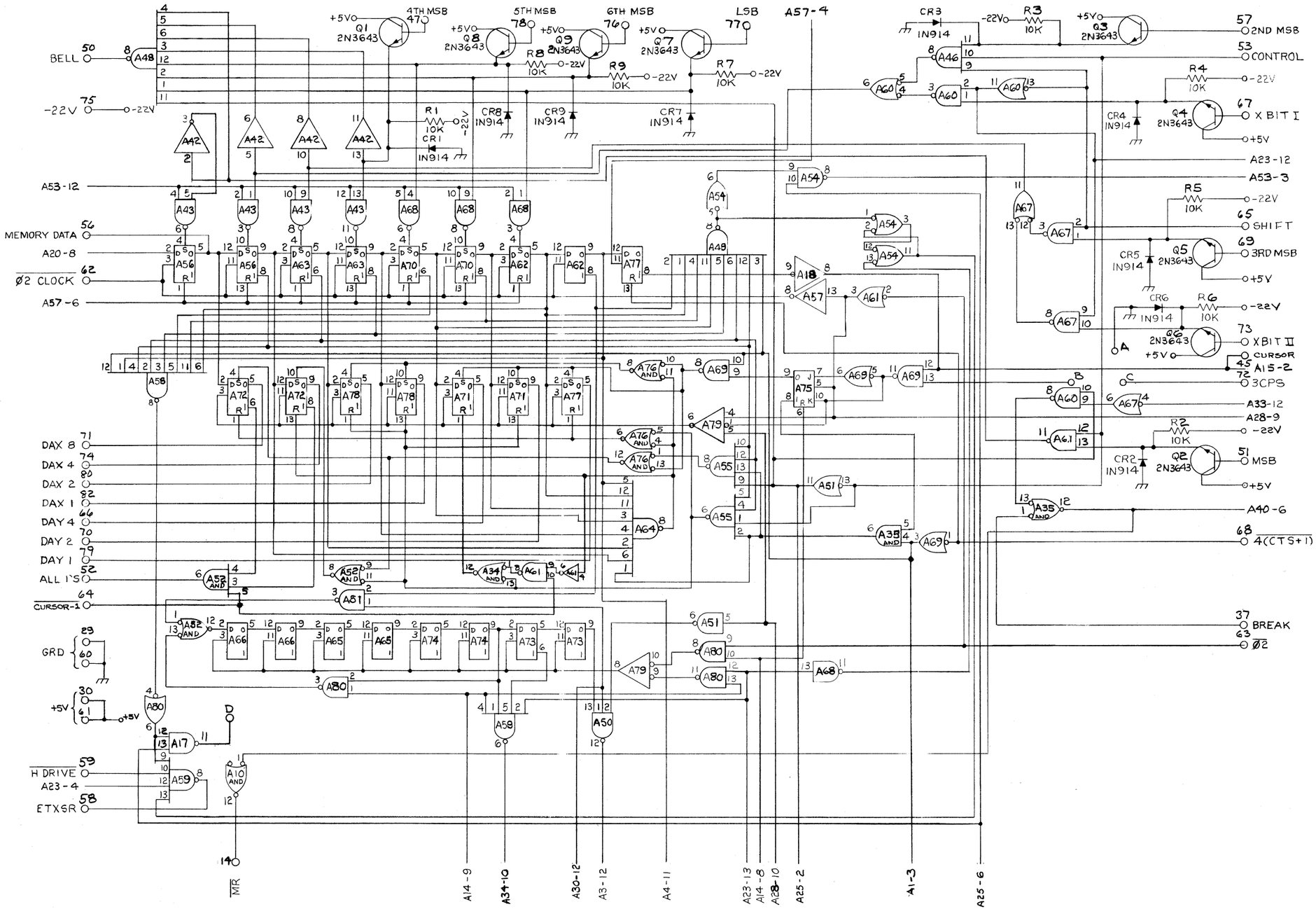




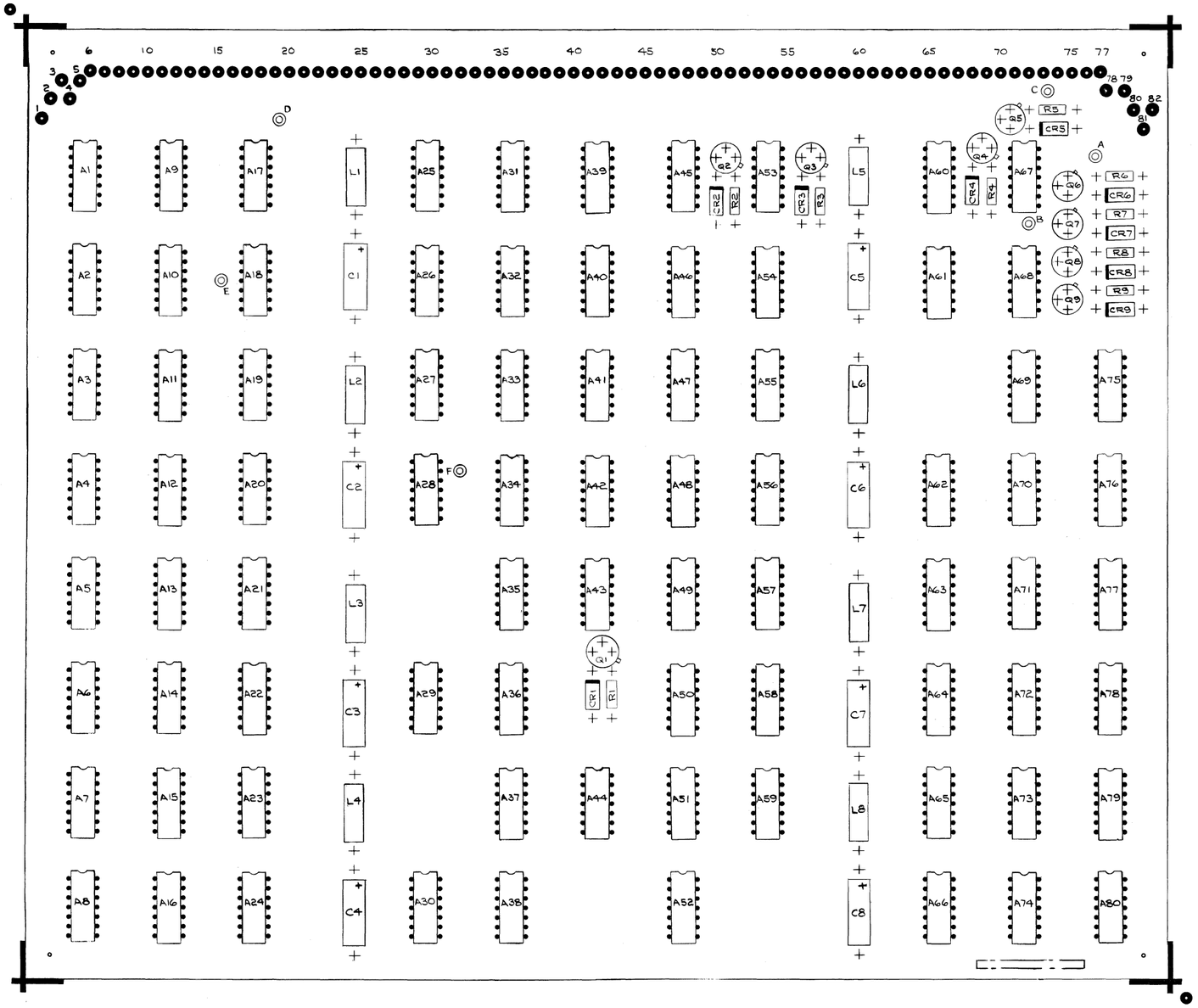
A12, Communications Control Board
Assembly Parts Layout 408024

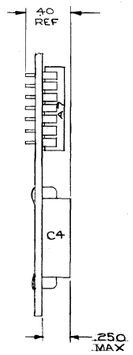


A13, Display Logic Board Assembly
Schematic (Sheet 1 of 2) 407993

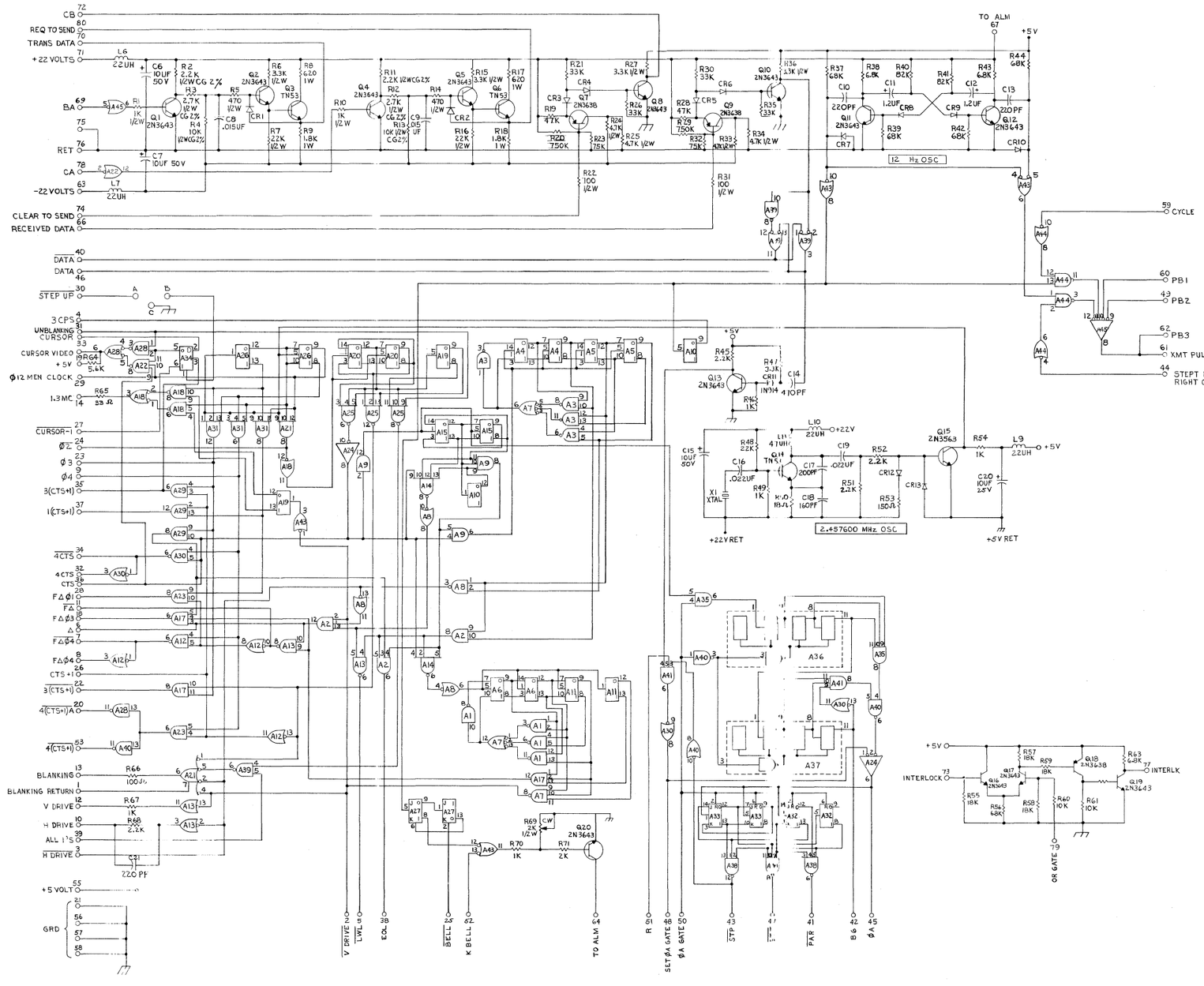


A13, Display Logic Board Assembly
Schematic (Sheet 2 of 2) 407993

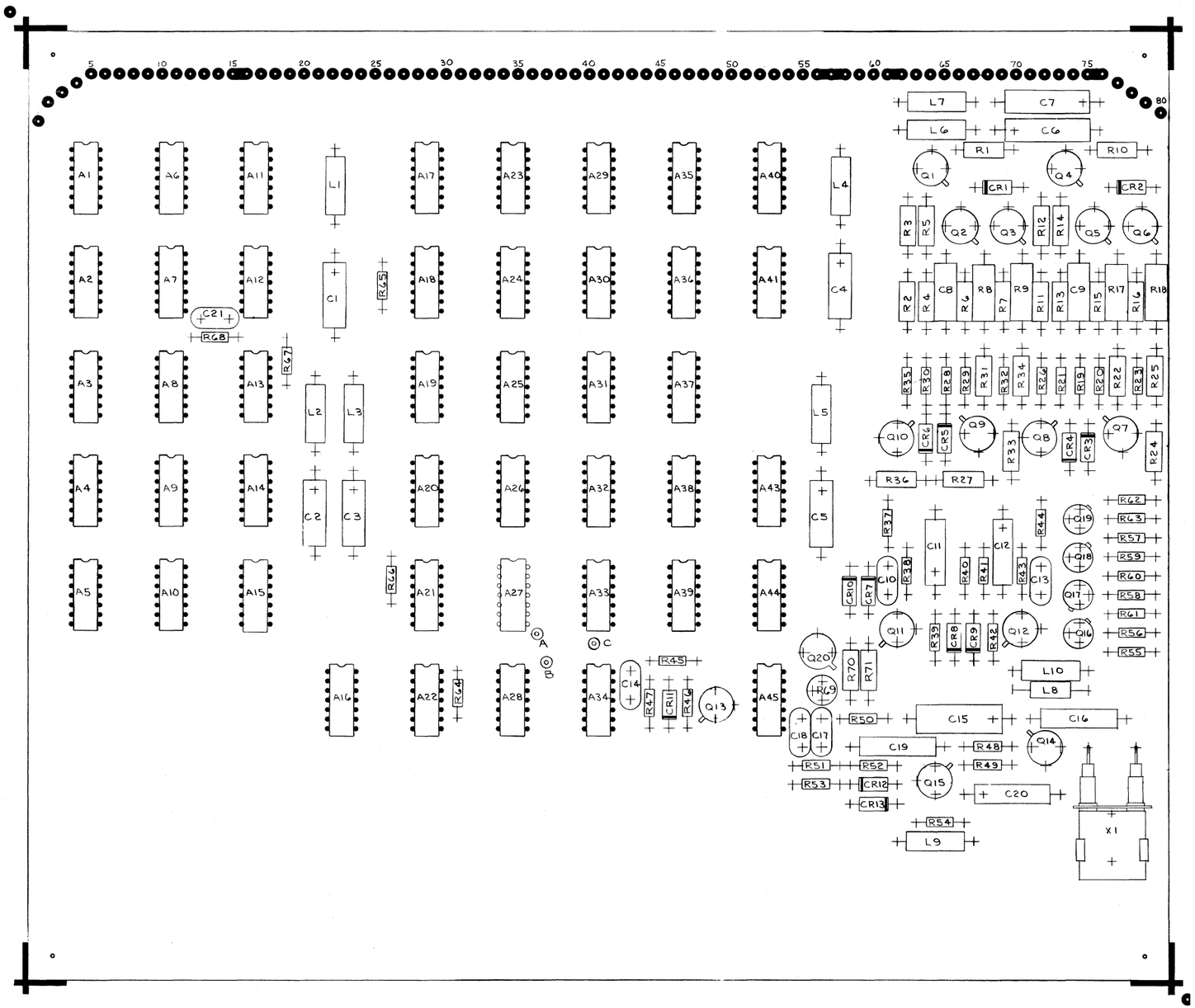




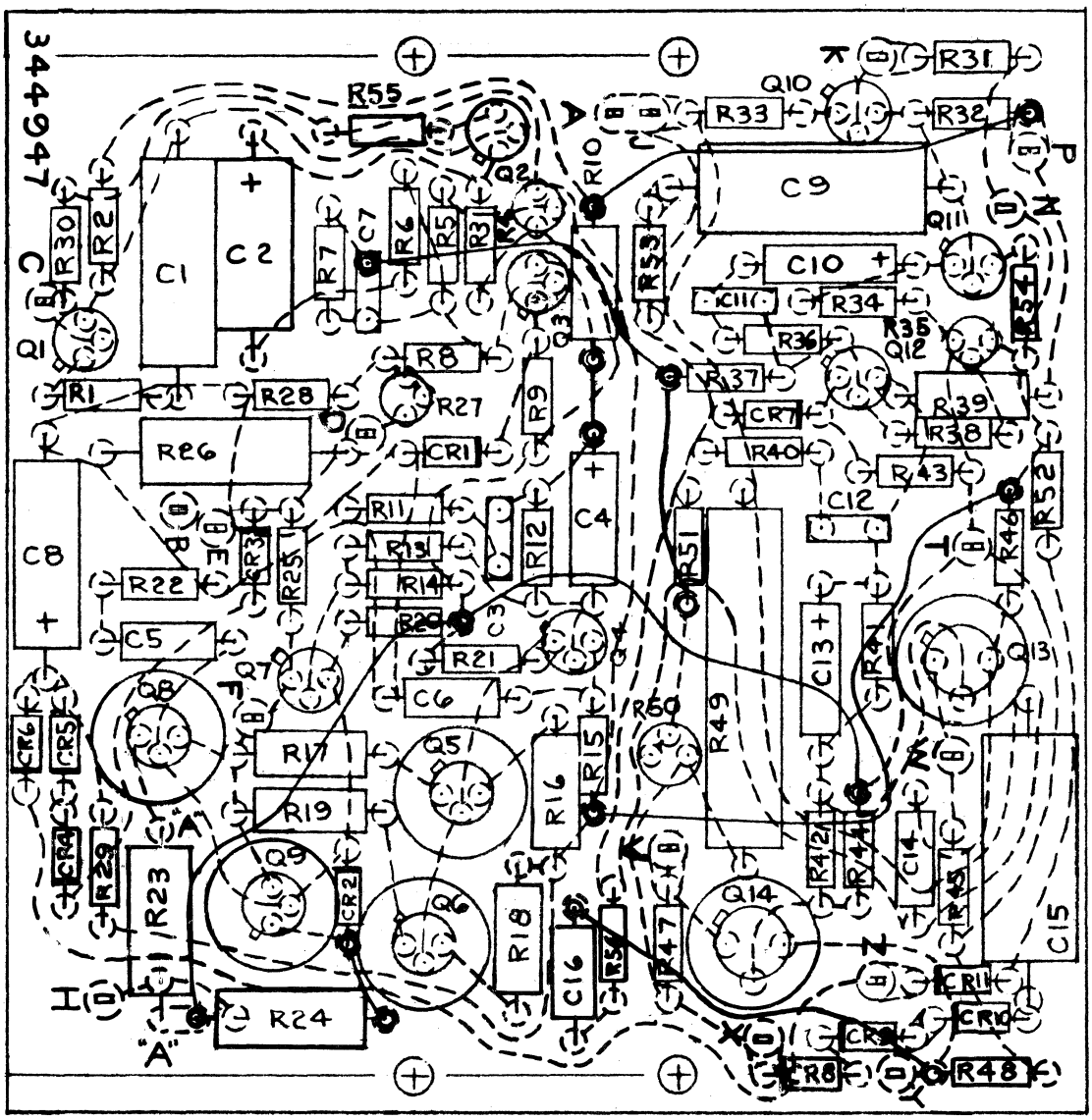
A13, Display Logic Board Assembly
Parts Layout 407992



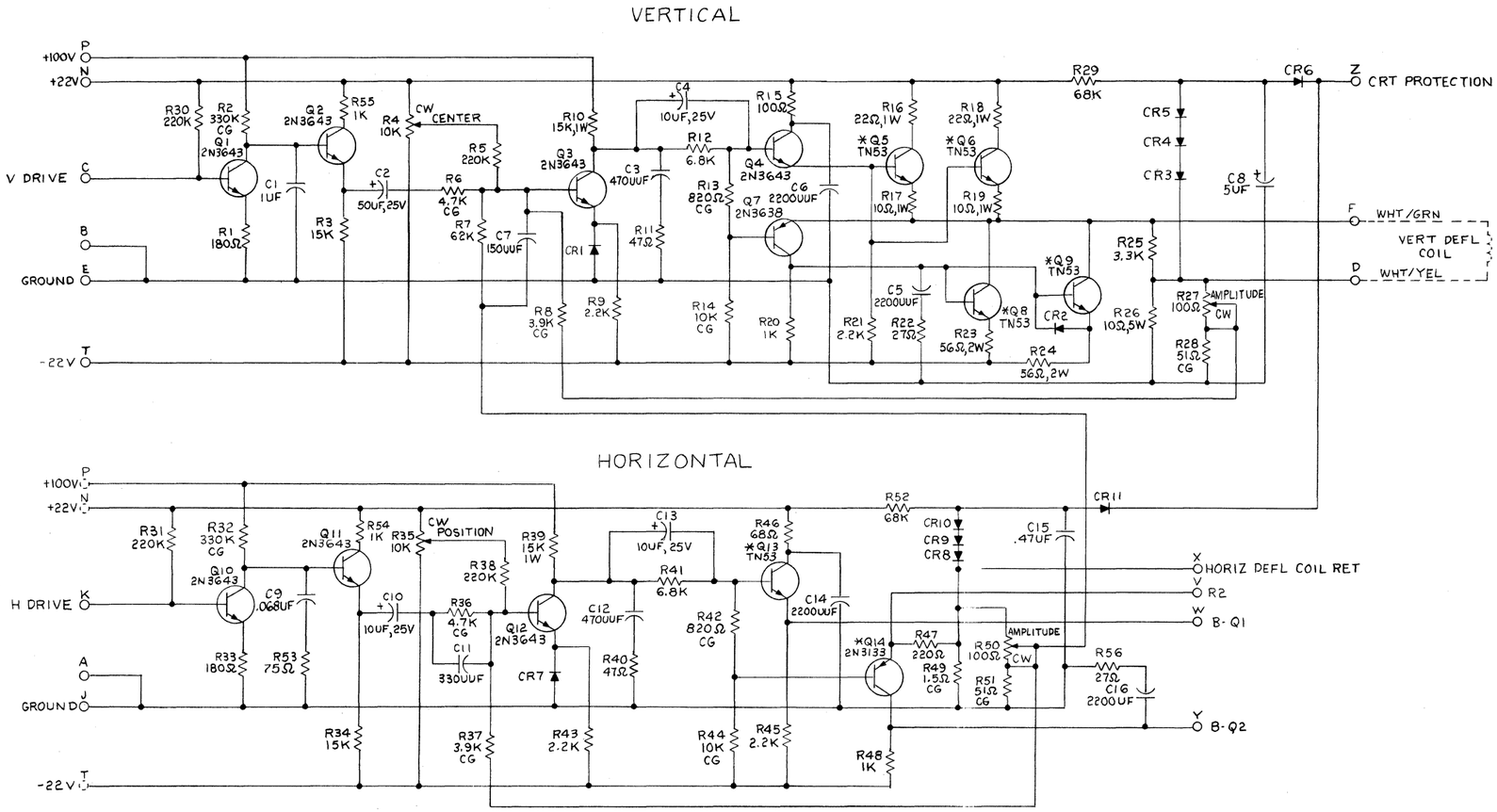
A14, Timing and Discrete Board
Assembly Schematic 407905

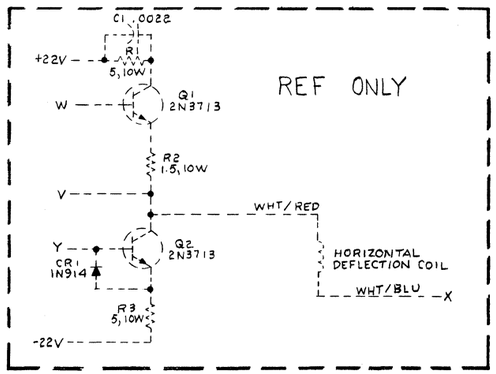


A14, Timing and Discrete Board Assemb
Parts Layout 407981

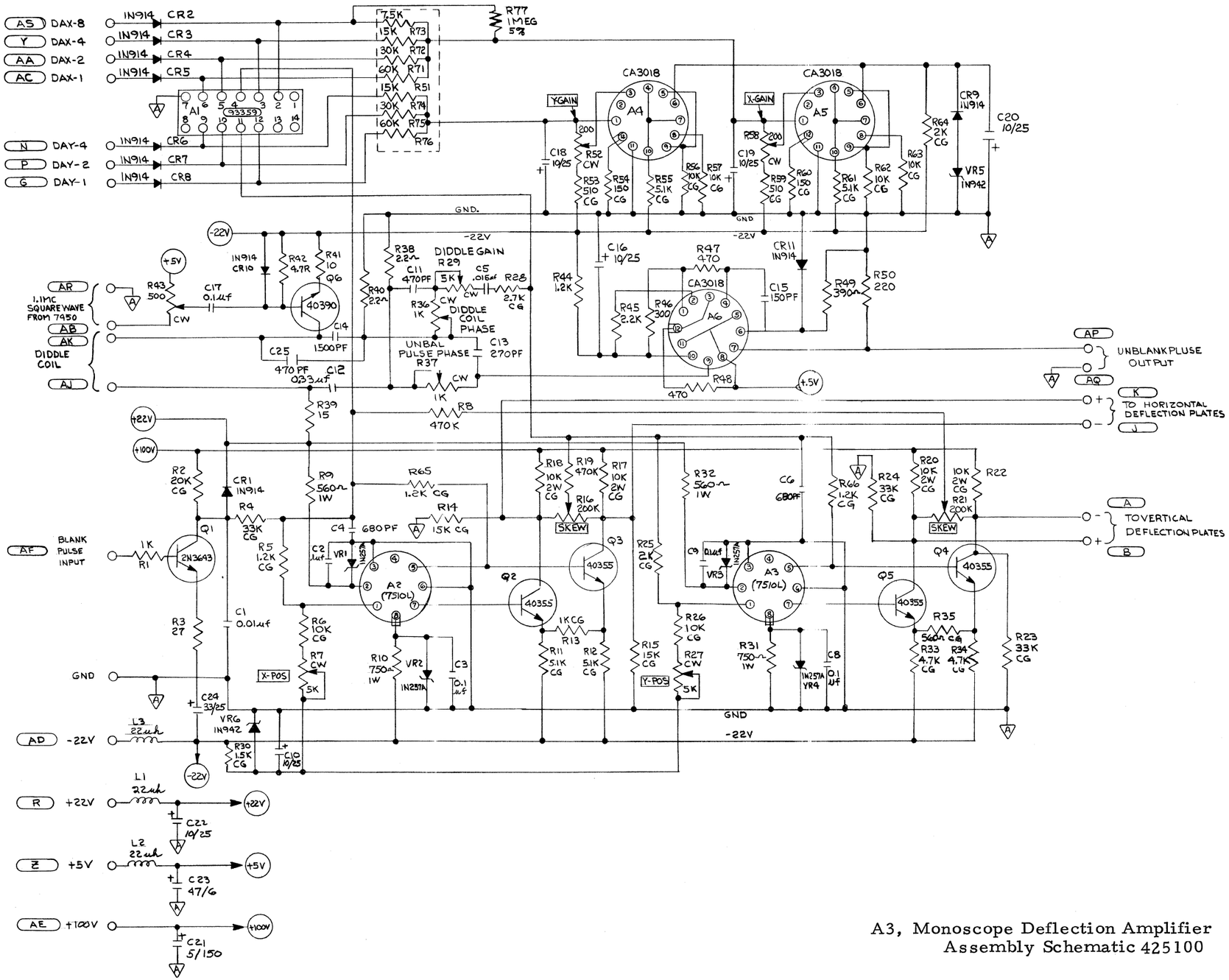


A2, Vertical and Horizontal Deflection
Amplifier Assembly Parts Layout 344947

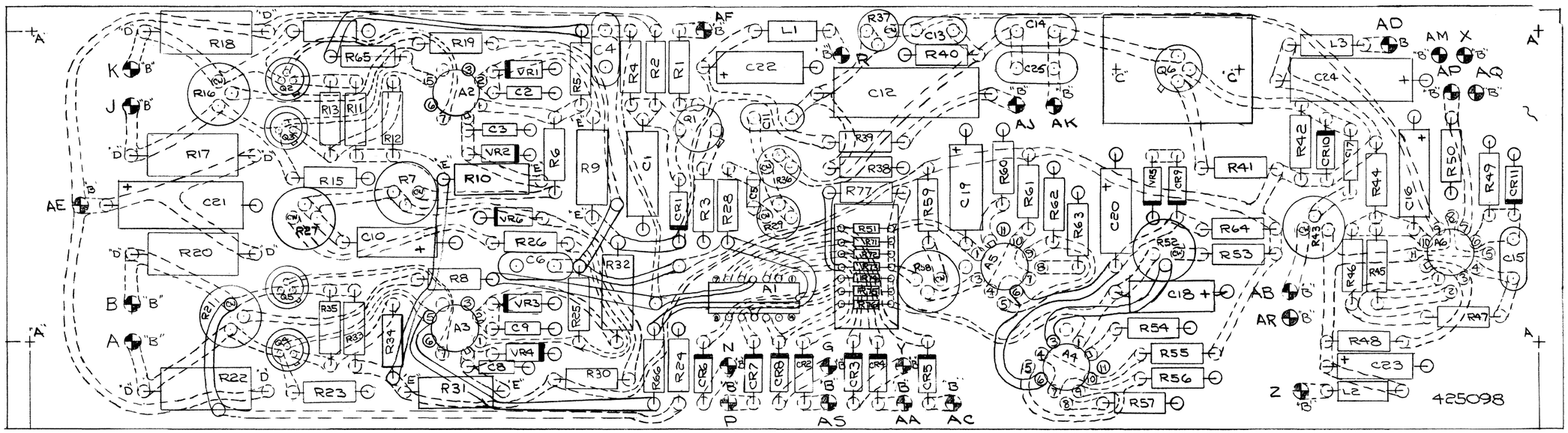


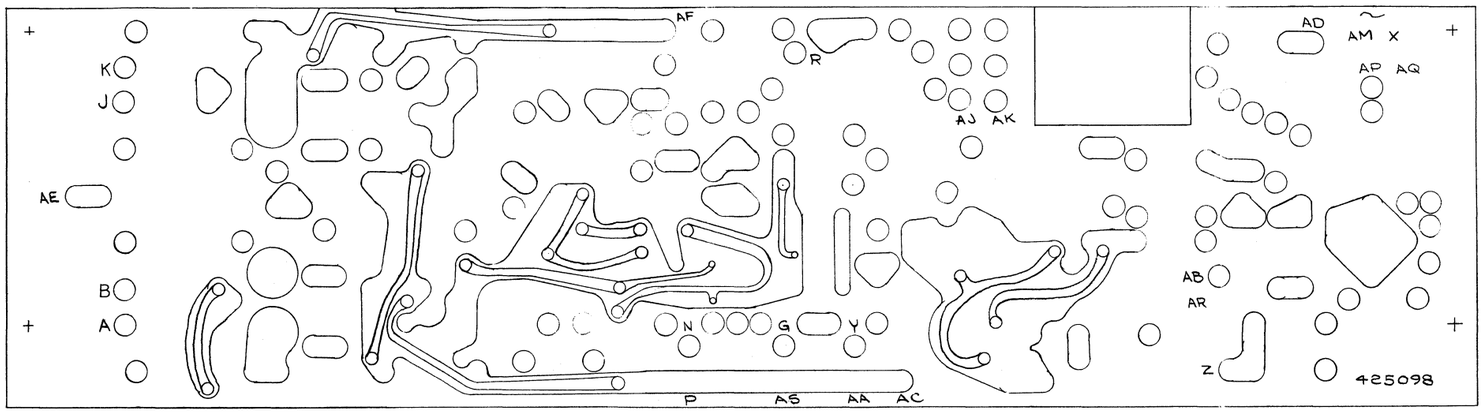


A2, Vertical and Horizontal Deflection Amplifier Assembly
Schematic 389300



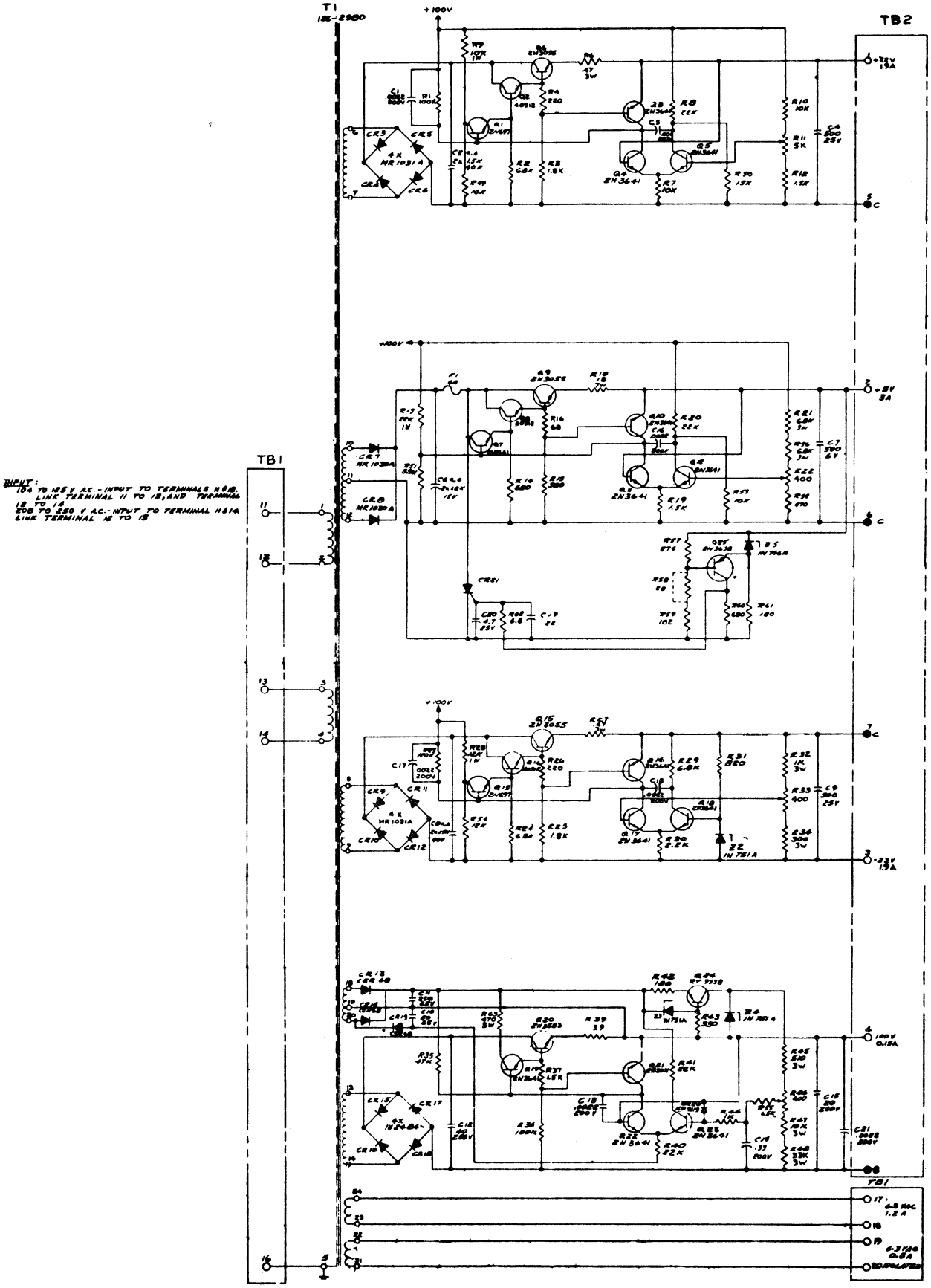
A3, Monoscope Deflection Amplifier
Assembly Schematic 425100



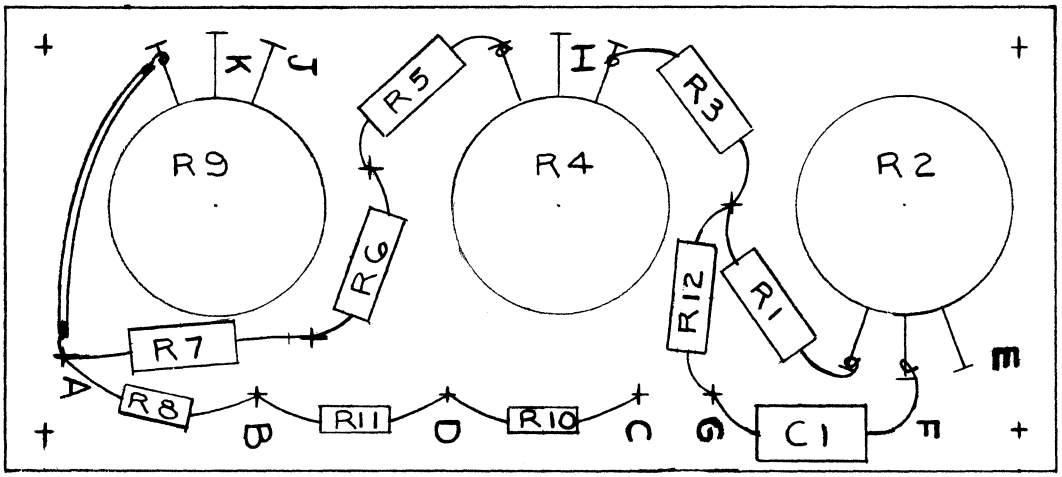


REFERENCE DWG TO CLARIFY GROUND PLANE

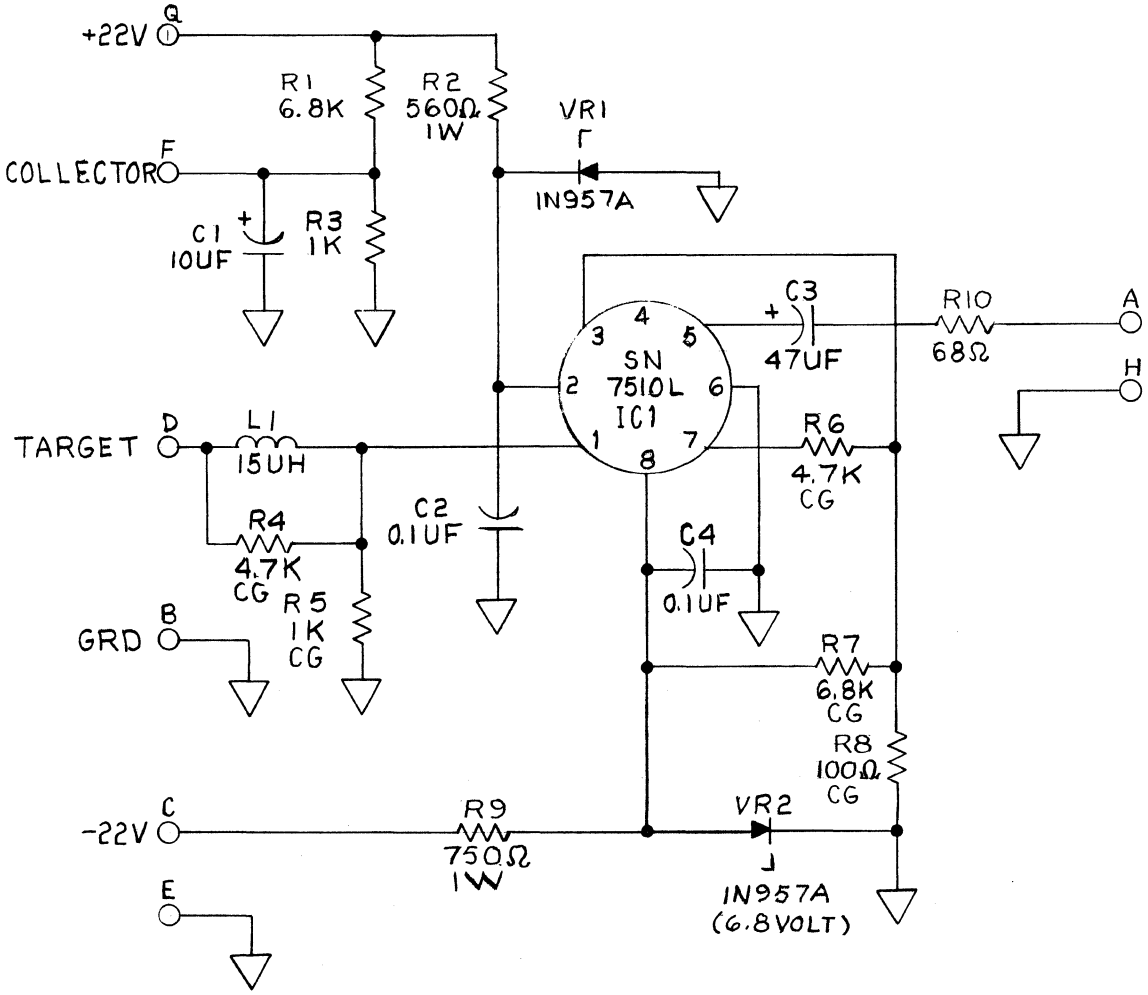
A3, Monoscope Deflection Amplifier
Assembly Parts Layout 425098



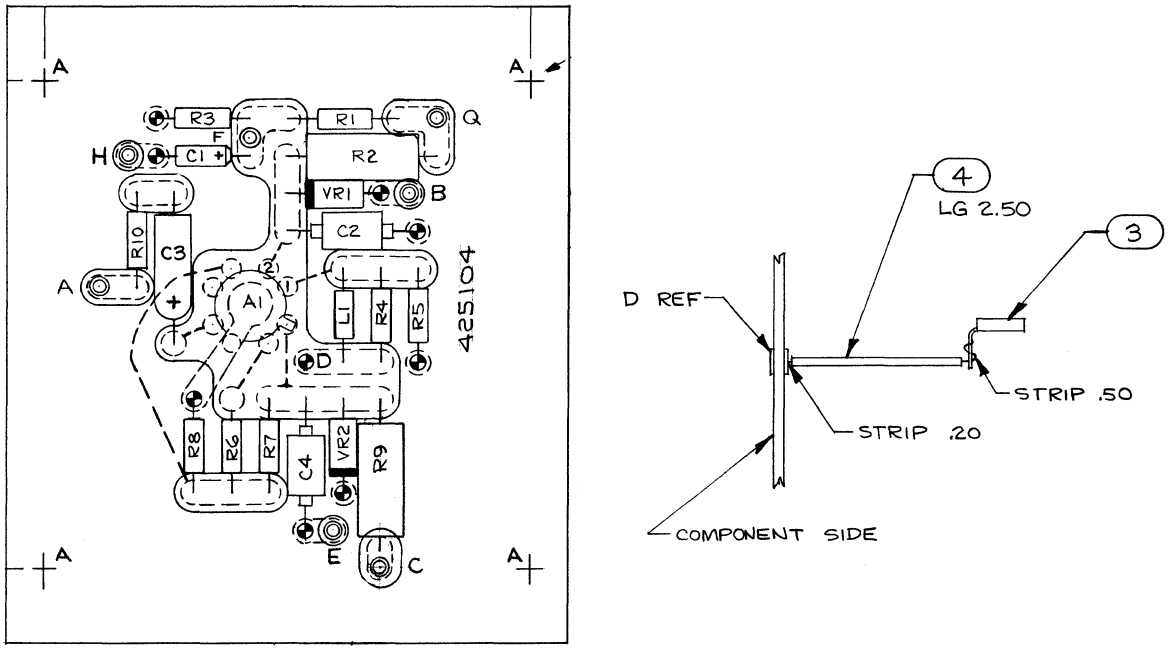
A4, Low-Voltage Power Supply Assembly
Schematic 2004030



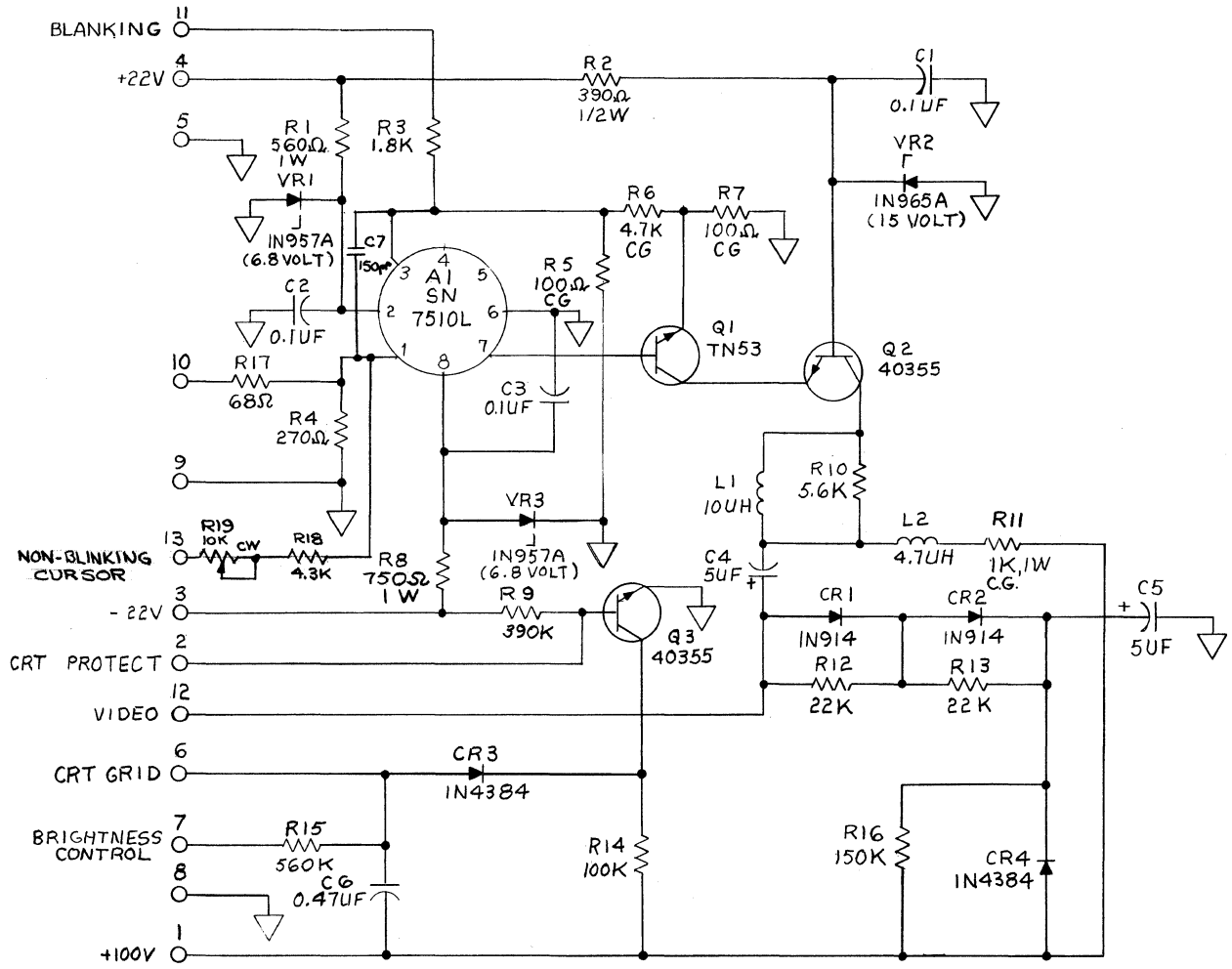
A6, High Voltage Network Assembly
Parts Layout 387926



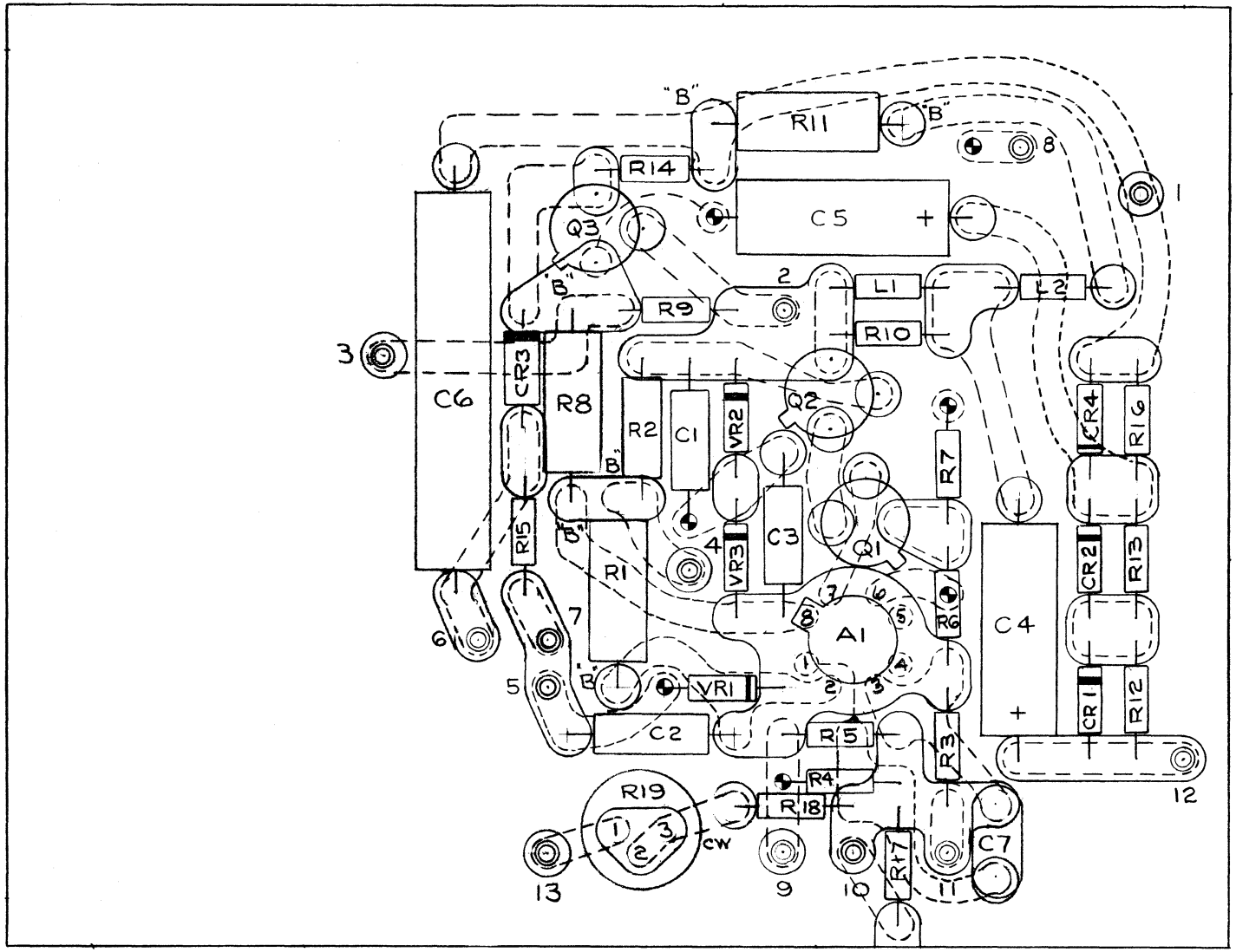
A7, Preamplifier Assembly Schematic 425105



A7, Preamplifier Assembly Parts Layout 425104



A8, Video Amplifier Assembly Schematic 425102



A8, Video Amplifier Assembly Parts Layout 425101