SAMSUNG

CMOS Programmable Logic (CPL™) Data Book

1988

CMOS PROGRAMMABLE LOGIC (CPL™)

Data Book

FIRST EDITION

INTRODUCTION

Samsung's CMOS Programmable Logic (CPL™) family introduces the benefits of advanced CMOS technology into the field programmable logic area, allowing system designers to save significant amounts of power without compromising performance.

The first generation of CPL devices, as specified in this book, are CMOS implementations of the industry standard PAL® devices. The 1.2 micron CMOS EPROM technology allows CPL parts to achieve bipolar performance at a much lower power, resulting in reduced system costs and easier prototyping. The erasable EPROM cell also facilitates 100% functional and AC testing of every part before it is released to market, making possible 100% programming yields.

Programming CPL devices is done by using standard PLD programmers. Because of the architectural compatibility with bipolar PALs, all current software tools also support the CPL devices. Therefore, no modification in the code is necessary when replacing a bipolar PAL device with a CPL device.

PAL® is a registered trademark of Monolithic Memories Inc.

SAMSUNG
Semiconductor

PRODUCT INDEX

PRODUCT DESIGNATION	DESCRIPTION	PAGES
CPL20		
CPL16L8L-25NC	OTP, Plastic 20-pin 1/4 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16L8L-25WC	20-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16L8-25NC	OTP, Plastic 20-pin 1/2 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16L8L-35NC	OTP, Plastic 20-pin 1/4 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16L8L-35WC	20-pin Windowed CERDIP, 1/4 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16L8-35NC	OTP, Plastic 20-pin 1/2 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16R4L-25NC	OTP, Plastic 20-pin 1/4 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16R4L-25WC	20-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16R4-25NC	OTP, Plastic 20-pin 1/2 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16R4L-35NC	OTP, Plastic 20-pin 1/4 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16R4L-35WC	20-pin Windowed CERDIP, 1/4 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16R4-35NC	OTP, Plastic 20-pin 1/2 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16R6L-25NC	OTP, Plastic 20-pin 1/4 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16R6L-25WC	20-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16R6-25NC	OTP, Plastic 20-pin 1/2 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16R6L-35NC	OTP, Plastic 20-pin 1/4 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16R6L-35WC	20-pin Windowed CERDIP, 1/4 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16R6-35NC	OTP, Plastic 20-pin 1/2 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16R8L-25NC	OTP, Plastic 20-pin 1/4 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16R8L-25WC	20-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16R8-25NC	OTP, Plastic 20-pin 1/2 Power, 25ns, CMOS PLD, Comm.	21-29
CPL16R8L-35NC	OTP, Plastic 20-pin 1/4 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16R8L-35WC	20-pin Windowed CERDIP, 1/4 Power, 35ns, CMOS PLD, Comm.	21-29
CPL16R8-35NC	OTP, Plastic 20-pin 1/2 Power, 35ns, CMOS PLD, Comm.	21-29

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CPL24		
CPL20L8L-25NC	OTP, Plastic 24-pin 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20L8L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20L8-25NC	OTP, Plastic 24-pin 1/2 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20L8L-35NC	OTP, Plastic 24-pin 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20L8L-35WC	24-pin Windowed CERDIP, 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20L8-35NC	OTP, Plastic 24-pin 1/2 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20R4L-25NC	OTP, Plastic 24-pin 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20R4L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20R4-25NC	OTP, Plastic 24-pin 1/2 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20R4L-35NC	OTP, Plastic 24-pin 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20R4L-35WC	24-pin Windowed CERDIP, 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20R4-35NC	OTP, Plastic 24-pin 1/2 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20R6L-25NC	OTP, Plastic 24-pin 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20R6L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20R6-25NC	OTP, Plastic 24-pin 1/2 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20R6L-35NC	OTP, Plastic 24-pin 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20R6L-35WC	24-pin Windowed CERDIP, 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20R6-35NC	OTP, Plastic 24-pin 1/2 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20R8L-25NC	OTP, Plastic 24-pin 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20R8L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20R8-25NC	OTP, Plastic 24-pin 1/2 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20R8L-35NC	OTP, Plastic 24-pin 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20R8L-35WC	24-pin Windowed CERDIP, 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20R8-35NC	OTP, Plastic 24-pin 1/2 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20L10L-25NC	OTP, Plastic 24-pin 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20L10L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20L10-25NC	OTP, Plastic 24-pin 1/2 Power, 25ns, CMOS PLD, Comm.	33-43
CPL20L10L-35NC	OTP, Plastic 24-pin 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20L10L-35WC	24-pin Windowed CERDIP, 1/4 Power, 35ns, CMOS PLD, Comm.	33-43
CPL20L10-35NC	OTP, Plastic 24-pin 1/2 Power, 35ns, CMOS PLD, Comm.	33-43

PRODUCT SELECTION GUIDE

Part #	Pins	Array Inputs	Dedicated Inputs	I/O's	Outputs			Max Speed (ns) (1,2)		Max I_{CC} (mA)		Available Packages (3)
					Combinatorial	Registered	Total	-25	-35	Low Power	Std. Power	
CPL16L8	20	16	10	6	8	0	8	t_{PD}=25	t_{PD}=35	45	70	N, W
CPL16R4	20	16	8	4	4	4	8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	45	70	N, W
CPL16R6	20	16	8	2	2	6	8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	45	70	N, W
CPL16R8	20	16	8	0	0	8	8	t_{CO}=15	t_{CO}=25	45	70	N, W
CPL20L10	24	20	12	8	10	0	10	t_{PD}=25	t_{PD}=35	45	70	N, W
CPL20L8	24	20	14	6	8	0	8	t_{PD}=25	t_{PD}=35	45	70	N, W
CPL20R4	24	20	12	4	4	4	8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	45	70	N, W
CPL20R6	24	20	12	2	2	6	8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	45	70	N, W
CPL20R8	24	20	12	0	0	8	8	t_{CO}=15	t_{CO}=25	45	70	N, W
CPL22V10	24	22	12	10	Programmable Macrocell Outputs		10	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	55	90	N, W
CPL16V8	20	16	10	8	Programmable Macrocell Outputs		8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	55	90	N, W

Package Codes: N = Plastic DIP, W = Windowed CERDIP

Notes:

(1) The above specifications are for the commercial temperature range of 0 to 70°C.
All Power supplies are V_{CC} = 5V ± 10%

(2) Military product in the temperature ranges of -55°C to +125°C is also available. Speed and power selections may vary from those above. See data sheet.

(3) PLCC and SOIC packages are available. Please contact factory.

CROSS REFERENCE

AMD	SAMSUNG
PAL16L8AC	CPL16L8-25C
PAL16L8ALC	CPL16L8-25C
PAL16L8C	CPL16L8-35C
PAL16L8LC	CPL16L8-35C
PAL16L8QC	CPL16L8L-35C
PAL16R4ALC	CPL16R4-25C
PAL16R4LC	CPL16R4-35C
PAL16R4C	CPL16R4-35C
PAL16R4QC	CPL16R4L-35C
PAL16R6AC	CPL16R6-25C
PAL16R6C	CPL16R6-35C
PAL16R6LC	CPL16R6-35C
PAL16R6QC	CPL16R6L-35C
PAL16R8AC	CPL16R8-25C
PAL16R8ALC	CPL16R8-25C
PAL16R8C	CPL16R8-35C
PAL16R8LC	CPL16R8-35C
PAL16R8QC	CPL16R8L-35C
PAL22V10AC	CPL22V10-25C
PAL22V10C	CPL22V10-35C

CYPRESS	SAMSUNG
PALC16L8-25C	CPL16L8-25C
PALC16L8L-25C	CPL16L8L-25C
PALC16L8-35C	CPL16L8-35C
PALC16L8L-35C	CPL16L8L-35C
PALC16R4-25C	CPL16R4-25C
PALC16R4L-25C	CPL16R4L-25C
PALC16R4-35C	CPL16R4-35C
PALC16R4L-35C	CPL16R4L-35C
PALC16R6-25C	CPL16R6-25C
PALC16R6L-25C	CPL16R6L-25C
PALC16R6-35C	CPL16R6-35C
PALC16R6L-35C	CPL16R6L-35C
PALC16R8-25C	CPL16R8-25C
PALC16R8L-25C	CPL16R8L-25C
PALC16R8-35C	CPL16R8-35C
PALC16R8L-35C	CPL16R8L-35C
PALC22V10-25C	CPL22V10-25C
PALC22V10-35C	CPL22V10-35C

FAIRCHILD	SAMSUNG
16L8A	CPL16L8-25C
16P8A	CPL16L8-25C-
16R4A	CPL16R4-25C
16R6A	CPL16R6-25C
16R8A	CPL16R8-25C
16RP4A	CPL16R4-25C-
16RP6A	CPL16R6-25C-
16RP8A	CPL16R8-25C-

HARRIS	SAMSUNG
HPL16LC8-5	CPL16L8L-35C-
HPL16RC4-5	CPL16R4L-35C-
HPL16RC6-5	CPL16R6L-35C-
HPL16RC8-5	CPL16R8L-35C-

MMI	SAMSUNG
PAL12L10C	CPL20L10-35C*
PAL14L8C	CPL20L8-35C*
PAL16L6C	CPL20L8-35C*
PAL16L8AC	CPL16L8-25C
PAL16L8A-2C	CPL16L8-35C
PAL16L8A-4C	CPL16L8L-35C
PAL16L8B-2C	CPL16L8-25C
PAL16L8B-4C	CPL16L8L-35C
PAL16L8C	CPL16L8-35C
PAL16L8D-4C	CPL16L8L-25C
PAL16R4AC	CPL16R4-25C
PAL16R4A-2C	CPL16R4-35C
PAL16R4A-4C	CPL16R4L-35C
PAL16R4B-2C	CPL16R4-25C
PAL16R4B-4C	CPL16R4L-35C
PAL16R4C	CPL16R4-35C
PAL16R4D-4C	CPL16R4L-25C
PAL16R6A-4C	CPL16R6L-35C
PAL16R6B-2C	CPL16R6-25C
PAL16R6B-4C	CPL16R6L-35C
PAL16R6B-2C	CPL16R6-25C
PAL16R6B-4C	CPL16R6L-35C
PAL16R6C	CPL16R6-35C
PAL16R6D-4C	CPL16R6L-25C
PAL16R6AC	CPL16R6-25C
PAL16R6A-2C	CPL16R6-35C
PAL16R8AC	CPL16R8-25C
PAL16R8A-2C	CPL16R8-35C
PAL16R8A-4C	CPL16R8L-35C
PAL16R8B-2C	CPL16R8-25C
PAL16R8B-4C	CPL16R8L-35C
PAL16R8C	CPL16R8-35C
PAL16R8D-4C	CPL16R8L-25C

MMI	SAMSUNG
PAL18L4C	CPL20L8-35C*
PAL20L10AC	CPL20L10-25C
PAL20L10C	CPL20L10-35C
PAL20L8AC	CPL20L8-25C
PAL20L8A-2C	CPL20L8-35C
PAL20L8C	CPL20L8-35C
PAL20R4AC	CPL20R4-25C
PAL20R4A-2C	CPL2OR4-35C
PAL20R4C	CPL20R4-35C

CROSS REFERENCE (Continued)

MMI	SAMSUNG
PAL20R6AC	CPL20R6-25C
PAL20R6A-2C	CPL20R6-35C
PAL20R6C	CPL20R6-35C
PAL20R8AC	CPL20R8-25C
PAL20R8A-2C	CPL20R8-35C
PAL20R8AC	CPL20R8-25C
PAL20R8A-2C	CPL20R8-35C
PAL20R8C	CPL20R8-35C
PALC22V10H-25C	CPL22V10-25C
PALC22V10H-35C	CPL22V10-35C
PALC16L8Q-25C	CPL16L8L-25C
PALC16R4Q-25C	CPL16R4L-25C
PALC16R6Q-25C	CPL16R6L-25C
PALC16R8Q-25C	CPL16R8L-25C

NATIONAL	SAMSUNG
12L10C	CPL20L10-35C*
14L8C	CPL20L8-35C*
16L6C	CPL20L8-35C*
18L4C	CPL20L8-35C*
PAL16L8A2C	CPL16L8-35C
PAL16L8AC	CPL16L8-25C
PAL16L8B2C	CPL16L8-25C
PAL16L8B4C	CPL16L8L-35C
PAL16L8C	CPL16L8-35C
PAL16R4A2C	CPL16R4-35C
PAL16R4AC	CPL16R4-25C
PAL16R4B2C	CPL16R4-25C
PAL16R4B4C	CPL16R4L-35C
PAL16R4C	CPL16R4-35C
PAL16R6A2C	CPL16R6-35C
PAL16R6AC	CPL16R6-25C
PAL16R6B2C	CPL16R6-25C
PAL16R6B4C	CPL16R6L-35C
PAL16R6C	CPL16R6-35C
PAL16R8A2C	CPL16R8-35C
PAL16R8AC	CPL16R8-25C
PAL16R8B2C	CPL16R8-25C
PAL16R8B4C	CPL16R8L-35C
PAL16R8C	CPL16R8-35C
PAL20L10B2C	CPL20L10-25C
PAL20L10C	CPL20L10-35C
PAL20L2C	CPL20L8-35C
PAL20L8AC	CPL20L8-25C
PAL20L8BC	CPL20L8-25C
PAL20L8BC	CPL20L8-25C
PAL20L8C	CPL20L8-35C
PAL20R4AC	CPL20R4-25C

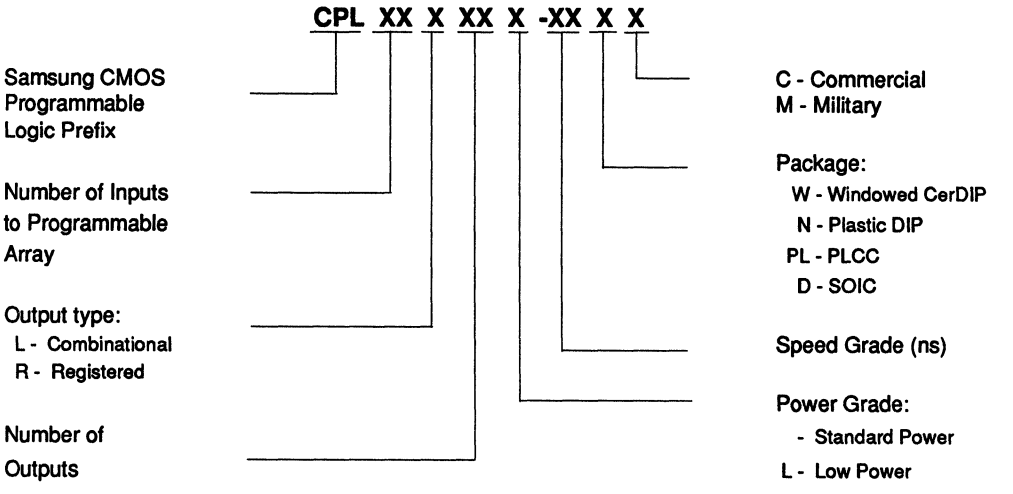
NATIONAL	SAMSUNG
PAL20R4BC	CPL20R4-25C
PAL20R4C	CPL20R4-35C
PAL20R6AC	CPL20R6-25C
PAL20R6BC	CPL20R6-25C
PAL20R6C	CPL20R6-35C
PAL20R8AC	CPL20R8-25C
PAL20R8BC	CPL20R8-25C
PAL20R8C	CPL20R8-35C

TI	SAMSUNG
PAL22V10AC	CPL22V10-25C
PAL16L8AC	CPL16L8-25C
PAL16L8A-2C	CPL16L8-35C
PAL16L8B-25C	CPL16L8-25C
PAL16R4AC	CPL16R4-25C
PAL16R4A-2C	CPL16R4-35C
PAL16R4-25C	CPL16R4-25C
PAL16R6AC	CPL16R6-25C
PAL16R6A-2C	CPL16R6-35C
PAL16R6-25C	CPL16R6-25C
PAL16R8AC	CPL16R8-25C
PAL16R8A-2C	CPL16R8-35C
PAL16R8-25C	CPL16R8-25C
PAL20L10AC	CPL20L10-25C
PAL20L10A-2C	CPL20L10-35C
PAL20L8AC	CPL20L8-25C
PAL20L8A-2C	CPL20L8-35C
PAL20R4AC	CPL20R4-25C
PAL20R4A-2C	CPL20R4-35C
PAL20R6AC	CPL20R6-25C
PAL20R6A-2C	CPL20R6-35C
PAL20R8AC	CPL20R8-25C
PAL20R8A-2C	CPL20R8-35C

Unless otherwise noted, all performance and power specs are met or exceeded for each product.

(-) FUNCTIONALLY EQUIVALENT
(*) SUPERSET, DOWNWARD COMPATIBLE

CPL™ ORDERING INFORMATION



Samsung CPL Family Features

Samsung's CPL (CMOS Programmable Logic) devices use a state-of-the-art CMOS EPROM technology which emphasizes complete testability. The 1.2 micron advanced CMOS process provides high performance, which was previously achieved only with bipolar processes, at a much lower power. Testability is inherent to the technology because it allows devices to be programmed and erased, thus facilitating 100% programming, AC, and functional testing.

The first generation of CPL devices are CMOS implementations of the industry standard PAL devices. The CPL devices offer significant advantages over TTL logic, some of which are listed below:

- 100% user-programmability
- Design flexibility
- Chip-count and pin-count reduction
- Pattern duplication prevention (Security Bit)

The CPL family also offers additional features and benefits which can be attributed to the CMOS EPROM technology:

- 100% programming, AC, and functional testing
- Increased reliabiltiy
- Easier, lower-cost prototyping with reprogrammable CPL devices (windowed, CERDIP)
- Lower power consumption over bipolar PALs with matched performance

The CPL EPROM cells are programmed by charging a floating gate with electrons and unprogrammed by irradiating the cells with ultraviolet (UV) light, making complete testing of all circuitry possible before shipping. On the other hand, bipolar devices which use fuse programmable cells, can be programmed only once, making 100% testing impossible. Special, on-chip test arrays also allow additional functional and AC testing without having to program the CPL devices.

CPL devices which are contained in windowed CERDIP packages may be programmed and erased, at the customer site. This allows the designer to develop, test, and fine-tune his/her logic without having to replace each programmed device.

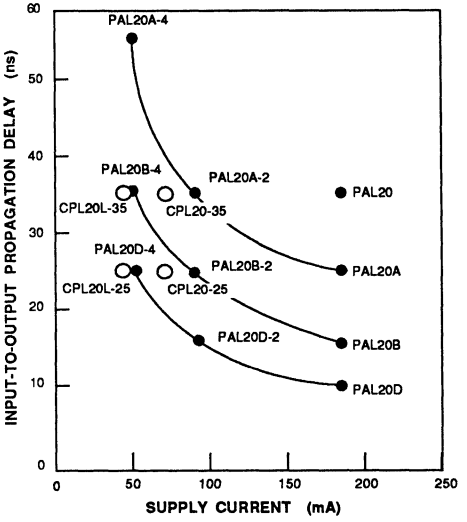
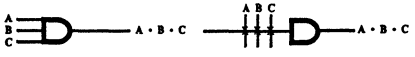


Figure 1. CPL-PAL Comparison

The CPL family offers the system designer a better alternative to the standard bipolar PLDs (Programmable Logic Devices). The devices are function and pinout compatible with their respective PAL predecessors. They may be designed into existing PAL sockets without changing the board layout or the PLD equations. The propagation delays of the CPL devices are 25 nsec or 35 nsec with 45mA or 70mA (max.) I_{CC}. Thus, the CPL devices provide bipolar speeds at a fraction of the bipolar power consumption, reducing the system's power requirements and increasing its reliability.

PLD Notation

In describing CPL devices, an industry standard PLD notation is used. Figure 2a shows the conventional notation of a multiple-input AND gate. Figure 2b shows the adopted PLD notation of the same logic gate. An X on an intersection of an input term and the input line of an AND gate represents that the input term is connected



a. **b.**

Figure 2. PLD Notation Example

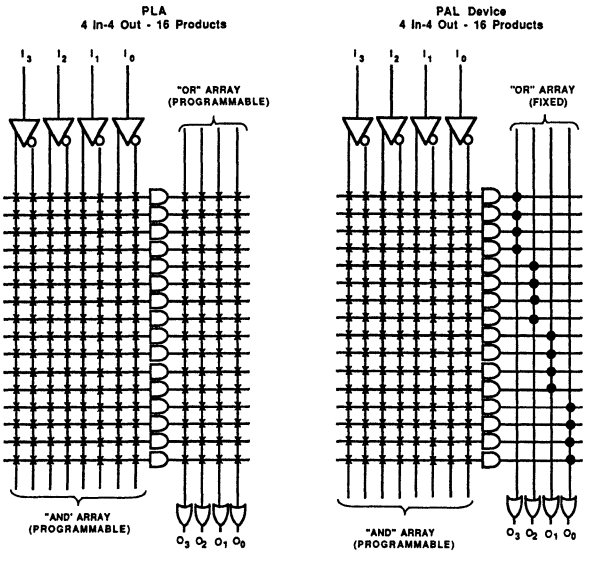


Figure 3. PLA and PAL AND-OR Structure

to one of the AND gate inputs. In a physical CPL device, an X represents an unprogrammed cell. (In an unprogrammed CPL device, all input terms are connected to all AND gates.) Each CPL device is illustrated by a logic diagram similar to the basic AND-OR structure diagram shown in Figure 3.

CPL Architecture

The CPL devices utilize the basic PLA (Programmable Logic Array) structure. This structure consists of an AND array followed by an OR array (see Figure 3). The CPL devices, like the PAL devices which they may replace, have a programmable AND array followed by a non-programmable OR array. Such a structure offers PLA flexibility while decreasing silicon complexity. In comparison, an FPLA (Field Programmable Logic Array) structure has both arrays programmable but occupies more silicon area.

The CPL devices, which have a basic PLA structure, lend themselves to easy implementation of Boolean transfer functions. These functions are expressed in the

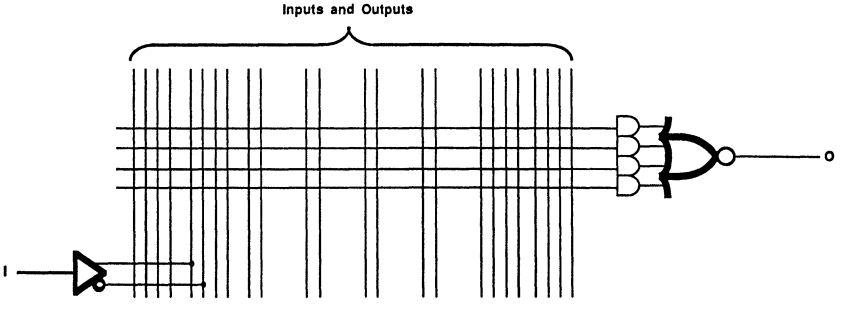


Figure 4. A Simple Combinatorial Output Structure

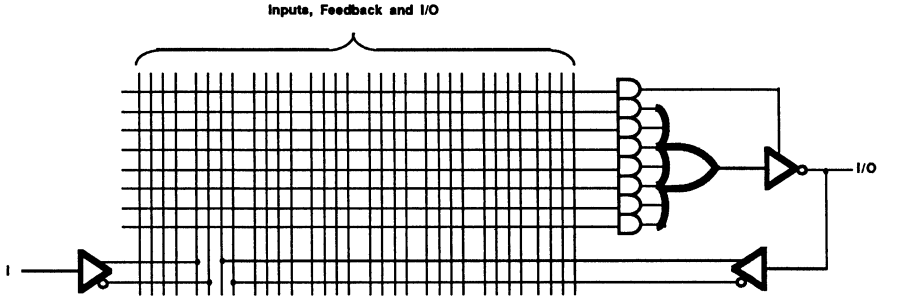


Figure 5. The Programmable Combinatorial Input/Output Structure

sum-of-products form. This allows quick and easy implementation of logic functions of varying complexity.

The CPL devices allow the designer to configure complex interconnections within the chip as opposed to configuring them on the PC board. The design, therefore, becomes more efficient and takes less time to complete. Furthermore, the interconnections, made by writing into EPROM cells, can be easily modified during prototype testing, saving lengthy and costly printed circuit board changes.

One CPL device can implement logic functions that require four or more conventional logic packages, reducing IC inventories while increasing board savings.

While all CPL devices are based on the PLA structure, they differ in their output structure combinations. The CPL devices feature a variety of output structures: combinatorial outputs, registered outputs, and programmable macro cells.

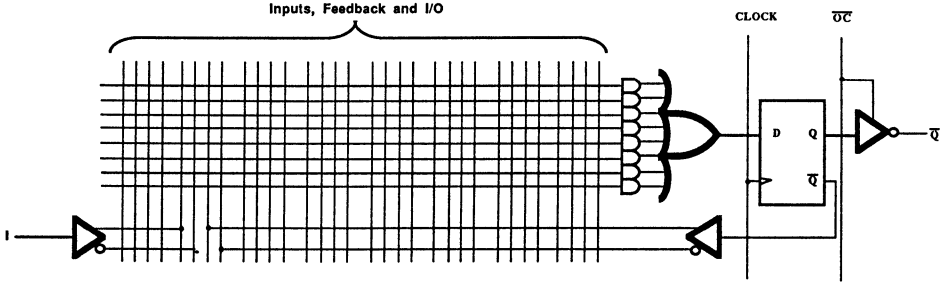


Figure 6. A Registered Output Structure with Feedback

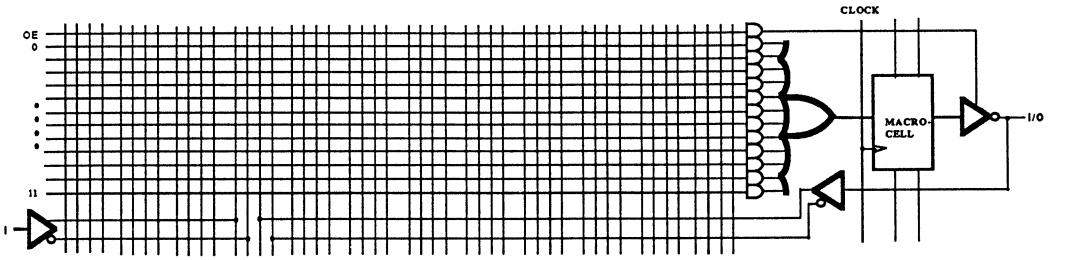


Figure 7. A Programmable Macro Cell Output Structure

Combinatorial Outputs

There are two types of combinatorial outputs. The simplest one is a combinatorial output without feedback (see Figure 4). It is used in the CPL16L8, CPL20L8, and CPL20L10 devices. This output sums several product terms (P-terms) into an active low signal. One additional P-term is used to individually enable/disable the output signal.

Another type of combinatorial output is the programmable combinatorial I/O (see Figure 5). When enabled, this output stage acts like the simple combinatorial output with the addition of a feedback path into the AND array. When disabled, the output stage allows the I/O pin to act as an input into the CPL AND array. This flexibility allows variable input/output ratios as well as bidirectional parts. The programmable combinatorial I/O output is used in all CPL20 and CPL24 devices with the exception of the CPL16R8 and CPL20R8.

Registered Outputs

This type of output features a data register with registered feedback. Each product term is summed into the data input of a D-type flip-flop. The flip-flop records the state of its input on the rising edge of the clock. The Q output of the flip-flop is gated to the output pin through a three-state buffer and is also fed back to the CPL AND array as an input term. This feature allows the CPL device to implement a state machine. The Clock and Output Enable/Disable signals are common to all registered outputs of a single device (See Figure 6). Registered outputs are used in all CPL20 and CPL24 devices with the exception of CPL16L8, CPL20L8, and CPL20L10.

Programmable Macro Cell I/O

The programmable macro cell, illustrated in Figure 7, is a very flexible structure which allows the designer to individually define the architecture of each I/O. Each I/O structure may be configured to be a combinatorial or registered output. Each output features an individually programmable Output Enable/Disable function as well as an individually programmable polarity function. Common Clock, Reset, and Preset signals facilitate preload, power reset and state-machine operations. Programmable macro cells are used in the CPL16V8 and CPL22V10 devices.

Test Circuitry

A PLD is tested, like any other digital circuit, by applying known values to its inputs. A fault may be detected by comparing the device's outputs with desired values. In general, a non-programmed PLD does not lend itself to exhaustive fault testing. Furthermore, since some of the PLDs have registered outputs with internal feedback lines to the programmable array, these feedback lines must be controlled during testing as well. Applying known values at these inputs of the array requires the application of many vectors to the device's inputs. Therefore, the device must be cycled many times to arrive at a known state, and the testing of the device becomes long and impractical.

To solve this problem, Samsung's CPL incorporates register preload and test arrays onto the devices, making testing simple and complete.

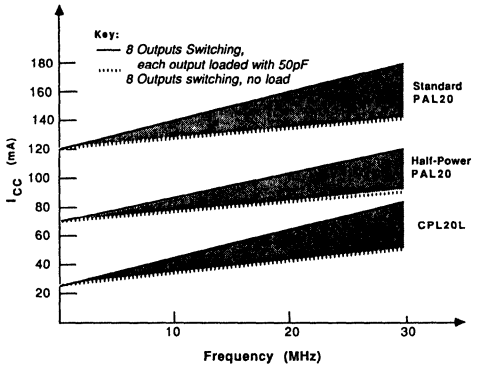


Figure 8. CPL and PAL Power Consumption as a Function of Frequency

Register Preload

The register preload feature allows the user, as well as the manufacturer, to load known values into the device's output registers. Known values are then applied to the array's feedback lines to help facilitate simple and complete device testing. The register preload operation is accomplished by applying a super-voltage pulse to a specified pin (see data sheets).

Test Array

The on-chip test array consists of additional input terms which may be accessed for AC and functional testing before and after packaging. The test array is not accessed during, and does not affect, normal device operation. During testing, the test array is activated and used to drive the device circuitry, bypassing the non-programmed programmable array. The test array is used during in-house final testing and may also be used by the customer for incoming inspection.

CPL Development Software

A variety of software packages are available to define and simulate CPL devices. All CPL devices are supported by industry-standard software packages such as Data I/O's ABEL, P-CAD's CUPL, and others. These software packages assemble CPL definition files in various formats, simulate the CPL devices, and create bit patterns conforming to a JEDEC standard format that may be transmitted to PLD programming systems.

The CPL devices can be programmed by all major PROM/PLD systems. Some PROM/PLD programmers may require a software update or a personality card/module to facilitate CPL programming. All programmers accept bit patterns which conform to JEDEC standard format.

More detailed information and a list of PLD software vendors and programmers is included in the CPL Programmer and Software Guide section of this book.

Power Dissipation

Low power consumption is one of the most important features of CMOS technology. With most of the power dissipating only during device switching, it is important to describe the power dissipation in terms which reflect its dependency on operating frequency.

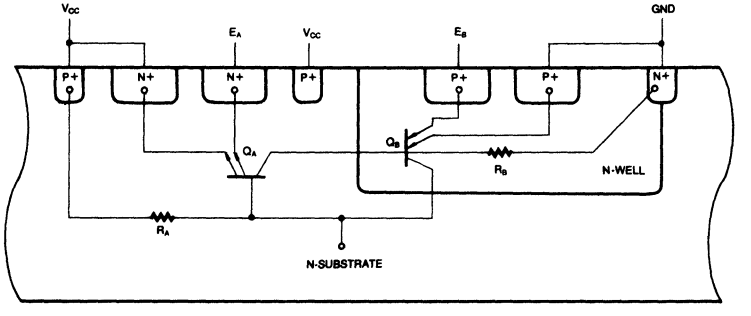


Figure 9. Simplified Cross Section of a CMOS Inverter

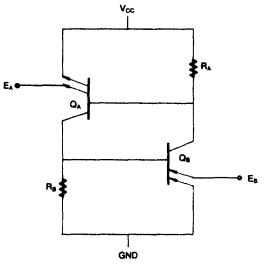


Figure 10. CMOS SCR Structure

A standard power dissipation model includes the device's quiescent current (I_Q), the device's internal "power dissipation" capacitance (C_{PD}), the external load capacitance (C_L), and the output buffer capacitance (C_O):

$$P_D = V_{CC}I_Q + C_{PD}V_{CC}^2f + (C_L+C_O)V_{DS}^2f$$

The quiescent power is determined by the static current. The switching power consumption is determined by the internal power dissipation capacitance and by the operating frequency (f). The power consumed by driving the external load depends on the external load itself, the output buffer capacitance, the operating frequency (f), and the output low-to-high voltage swing (V_{DS}).

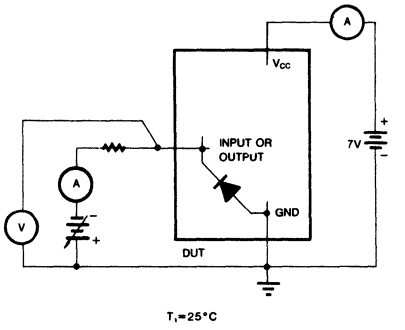


Figure 11. Test Setup for Measuring DC Latch-Up

The internal power capacitance as well as the static supply current vary from one CPL type to another. Moreover, they depend on the specific code which is programmed into the device. The typical I_Q for CPL20 and CPL24 is 25mA, and the typical C_{PD} is 45pF. The load capacitance plays an even more important role in determining the power consumption of a CPL device. Since 8 outputs may toggle, each consisting of typically 10pF, and each driving a 50pF load, up to 2.4 mA per MHz may add to the device's static supply current.

The graph in Figure 8 illustrates CPL power consumption as a function of operating frequency in comparison with bipolar PAL power consumption. All unused inputs are assumed to be tied to ground or V_{CC}, all active inputs are driven rail-to-rail, and the duty cycle is 50%. Measurements have shown that while the duty cycle does not greatly affect the CPL power consumption, up to 20% more power is consumed by the input buffers when the input voltage swings between 0.8V to 2.0V.

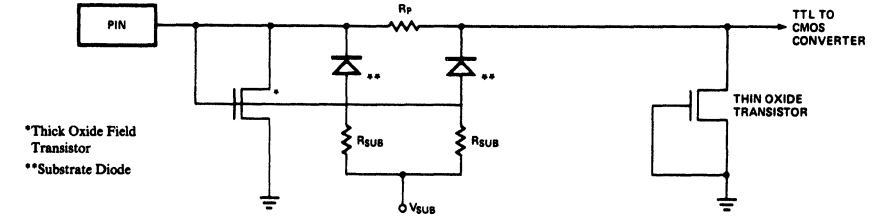


Figure 12. Input Protection Circuit

Latchup

In circuits fabricated using CMOS technology, a parasitic four- layer SCR structure appears between V_{CC} and ground. This parasitic structure can short V_{CC} to ground when voltages greater than V_{CC} or lower than ground are applied to an input or an output pin. The phenomenon is called "*latchup*" and may result in a damaged device. When a device is in latchup mode, the power supply must be shut-off to release the device back to normal operating mode.

The parasitic SCR structure in CMOS is illustrated in the simplified cross section of an inverter shown in Figure 9. Figure 10 shows a schematic representation of the same structure. When EA is raised above V_{CC}, current is injected from the emitter of QA and is swept to its collector. This current will increase the voltage at the gate of QB and once above 0.78V, it will turn QB on. QB will feed current back into RA and once a 0.7V voltage drop appears across RA, QA will turn on and inject more current into RB. Once both transistors are on and enough current is provided to sustain the SCR, it will stay on even after EA and EB return to within the rail voltages.

Because low RA and RB resistance values reduce the gain of QA and QB, Samsung's CPL devices are designed to have low RA and RB. In addition, large diodes are connected between each signal pin and the supply, to shunt out latchup trigger currents.

When a p-channel MOS transistor is used as a pull-up transistor on the output driver of an IC, another parasitic transistor is formed which worsens the latchup problem. The CPL devices use N- channel pull-up transistors which maintain TTL compatibility and improve latchup protection.

A substrate bias generator provides important additional latchup protection in CPL devices. It keeps the substrate at approximately -3V below ground level. The parasitic diode at an input pin will not turn on unless the voltage applied to that pin is more negative than -3V. The substrate bias also eliminates the substrate currents due to undershoot, thereby providing higher input noise tolerance.

Samsung's CPL devices are designed to withstand currents typically well above the specified minimum of 200 mA at 7V V_{CC} and 125°C. This parameter is measured on a static basis (see Figure 11).

ESD Protection

ESD protection is accomplished by preventing a high voltage from reaching the internal transistors of the integrated circuit. The circuit of each input pin includes a thick-oxide transistor, a thin-oxide transistor and the line resistance, Rp, between the transistors (see Figure 12). The thick-oxide transistor turns on when a large positive voltage is applied to the input pin. When the voltage arriving at the thin-oxide transistor exceeds 13V, the transistor turns on and protects the internal circuitry by discharging the current to ground. This current is then limited by the line resistance, Rp. A high negative voltage applied to the input pin is similarly discharged by the network of the substrate diodes which start conducting when the applied negative voltage is below the substrate level. The ESD protection incorporated in the output structure is shown in Figure 13.

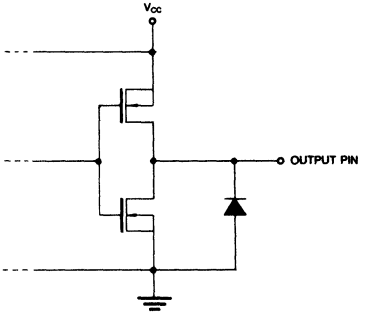


Figure 13. A typical output circuit of a CPL device.

CPL20

FEATURES/BENEFITS

- High-speed CMOS equivalent to Bipolar PALs
- CMOS UV-erasable EPROM cell to allow reprogrammability
- Low power (45mA Max. I_{CC}) and standard (70mA Max. I_{CC}) versions
- Two speed grades (t_{PD} = 25ns Max. and t_{PD} = 35ns Max.)
- >2000V ESD input and output protection
- 100% functional and AC tested
- 100% programming tested
- Programmable security bit to prevent pattern duplication
- Register Preload for register configuration
- Programmable three-state outputs

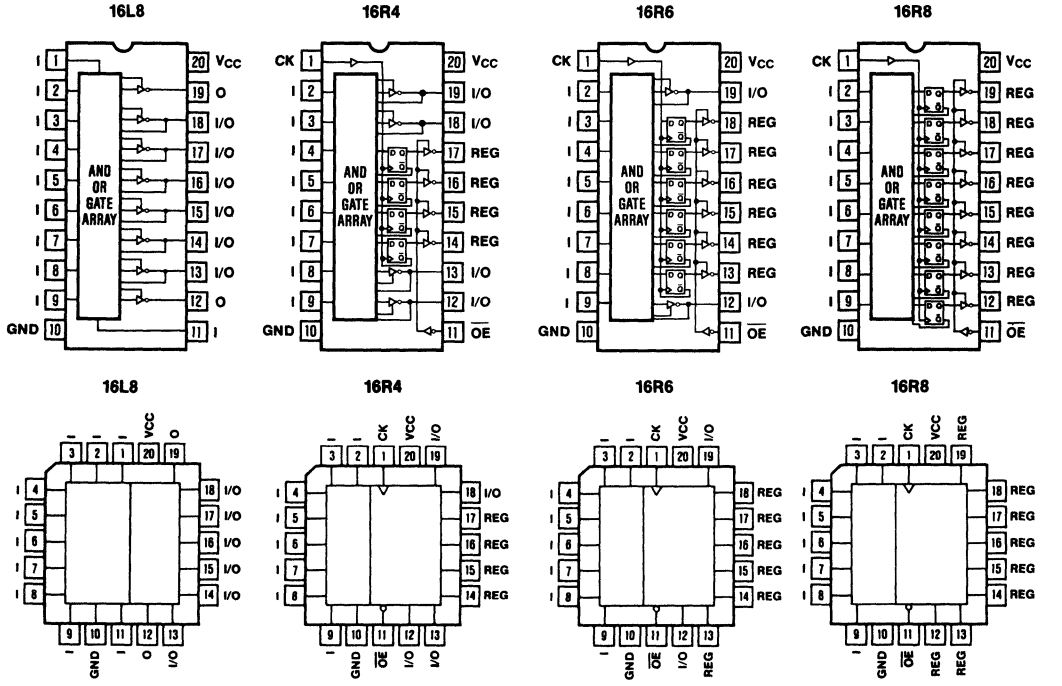
DESCRIPTION

The CPL20 Series devices are high-speed, UV-erasable, electrically programmable CMOS logic replacements of the Bipolar PAL20 family. They utilize the familiar sum-of-products form (AND array followed by an OR array) allowing the user to customize logic to his/her needs.

Four devices are offered in the CPL20 Series. They are: the CPL16L8, the CPL16R4, the CPL16R6, and the CPL16R8. Each of these devices has 16 array inputs and 8 outputs. All the outputs to the CPL16L8 are combinatorial, while all the outputs to the CPL16R8 are registered. In contrast, the CPL16R4 has 4 registered and 4 combinatorial outputs, and the CPL16R6 has 6 registered and 2 combinatorial outputs. Each combinatorial output in the CPL16R6 and CPL16R4 devices serves as an I/O pin. The CPL16L8 device has 6 I/O pins.

3

LOGIC SYMBOLS AND PINOUTS



DESCRIPTION (Continued)

The CPL devices are manufactured using a 1.2 micron EPROM technology which offers low power dissipation (45/70 mA maximum I_{CC}) combined with high performance (25ns maximum propagation delay). Because the CPL devices are erasable, they can be thoroughly tested for programming, functional and AC integrity, resulting in high-reliability and 100% programming yields.

The CPL20 devices are housed in 20-pin plastic DIP, PLCC, SOIC, and windowed CERDIP packages. The windowed CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The plastic DIP, PLCC, and SOIC devices are one-time-programmable (OTP) and may not be erased.

Register Preload

The register preload feature of the CPL20 Series allows output pins to be loaded with arbitrary states, making functional testing easier than ever.

Security Bit

All CPL20 devices feature a security bit. The security bit allows the user to protect his/her design against unauthorized duplication. When the security bit is set, the contents of the programmable-cell array may not be accessed in Read or Verify modes. Since the CPL devices do not have visible fuses, they offer enhanced security over what is available in bipolar PAL devices.

Test Array

Another feature of the devices in the CPL20 Series is the on-chip test array. It is programmed for final functional and AC testing of the devices after they have been packaged (even if the security bits have been programmed). In the normal operation of the device, the test arrays are not accessed. In the test mode of operation, only the input terms in the shaded portion of the functional block diagram are accessed. The test array facilitates high-reliability as well as simple and short testing.

ERASURE (windowed-CERDIP only)

The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:
Wavelength of 2537 Angstroms
(minimum dose -- 25 Wsec/cm^2)

If an ultraviolet lamp with a 12mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL20 ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leqq 20mA$)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC}+0.5	V
DC Programming Voltage		14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Military	T_A	-55 to +125	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC ELECTRICAL CHARACTERISTICS
Over Recommended Operating Conditions

Parameter	Symbol	Test Conditions		Min	Max	Unit
Low Level Input Voltage	V_{IL}	(Note 4)			0.8	V
High Level Input Voltage	V_{IH}	(Note 4)		2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$		-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	Military I_{OL}=12mA Commercial I_{OL}=24mA		0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	Military I_{OH}=-2mA Commercial I_{OH}=-3.2mA	2.4		V
Off-State Output Leakage Current	I_{OZL}	V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL}	V_O = 0.4V		-100	μA
	I_{OZH}		V_O = 2.4V		100	
Output Short-Circuit Current	I_{OS}	V_{CC} = Max, V_O = 0.5V (Note 5)			-300	mA
Power Supply Current	I_{CC}	All inputs = GND V_{CC} = Max I_{OUT} = 0mA	"L" STD MIL		45 70 70	mA mA mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

Note 5: Only one output shorted at a time. Duration of the short circuit should not be more than one second. V_O = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

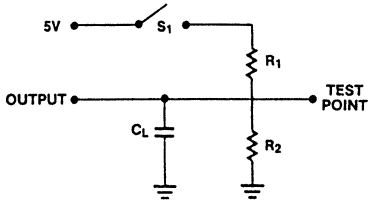
CPL20 AC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Note 6)

		Commercial				Military				
		-25		-35		-25		-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input or Feedback to Non-Registered Output, 16R6, 16R4, 16L8	t_{PD}		25		35		30		40	ns
Clock to Registered Output or Feedback, 16R8, 16R6, 16R4	t_{CO}		15		25		20		25	ns
Pin 11 to Output Enable, 16R8, 16R6, 16R4	t_{PZX11}		20		25		25		25	ns
Pin 11 to Output Disable, 16R8, 16R6, 16R4	t_{PXZ11}		20		25		25		25	ns
Input to Output Enable, 16R6, 16R4, 16L8	t_{PZX}		25		35		30		40	ns
Input to Output Disable, 16R6, 16R4, 16L8	t_{PXZ}		25		35		30		45	ns
Setup Time from Input or Feedback to Clock, 16R8, 16R6, 16R4	t_{SU}	20		30		25		35		ns
Hold Time, 16R8, 16R6, 16R4	t_H	0		0		0		0		ns
Clock Width (High or Low)	t_W	15		20		20		25		ns
Clock Period	t_P	35		55		45		60		ns
Maximum Frequency	f_{MAX}	28.5		18		22		16.5		MHz

Note 6: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6ns$.

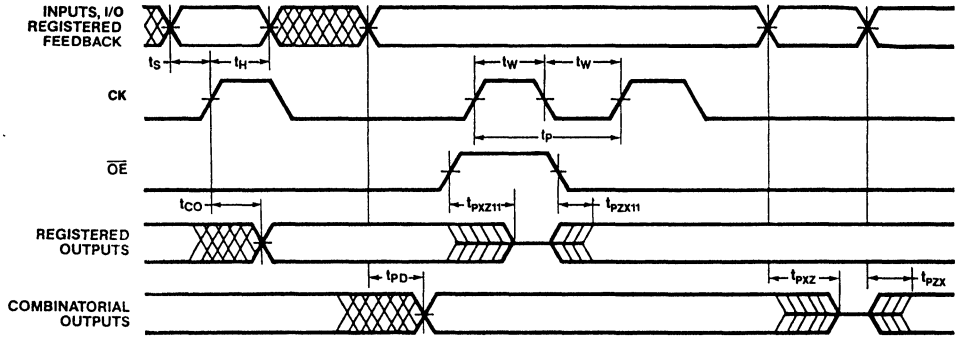
AC Test Circuit



Resistor Values (Ω)

	R1	R2
COM'L	200	390
MIL	390	750

CPL20 SWITCHING WAVEFORMS



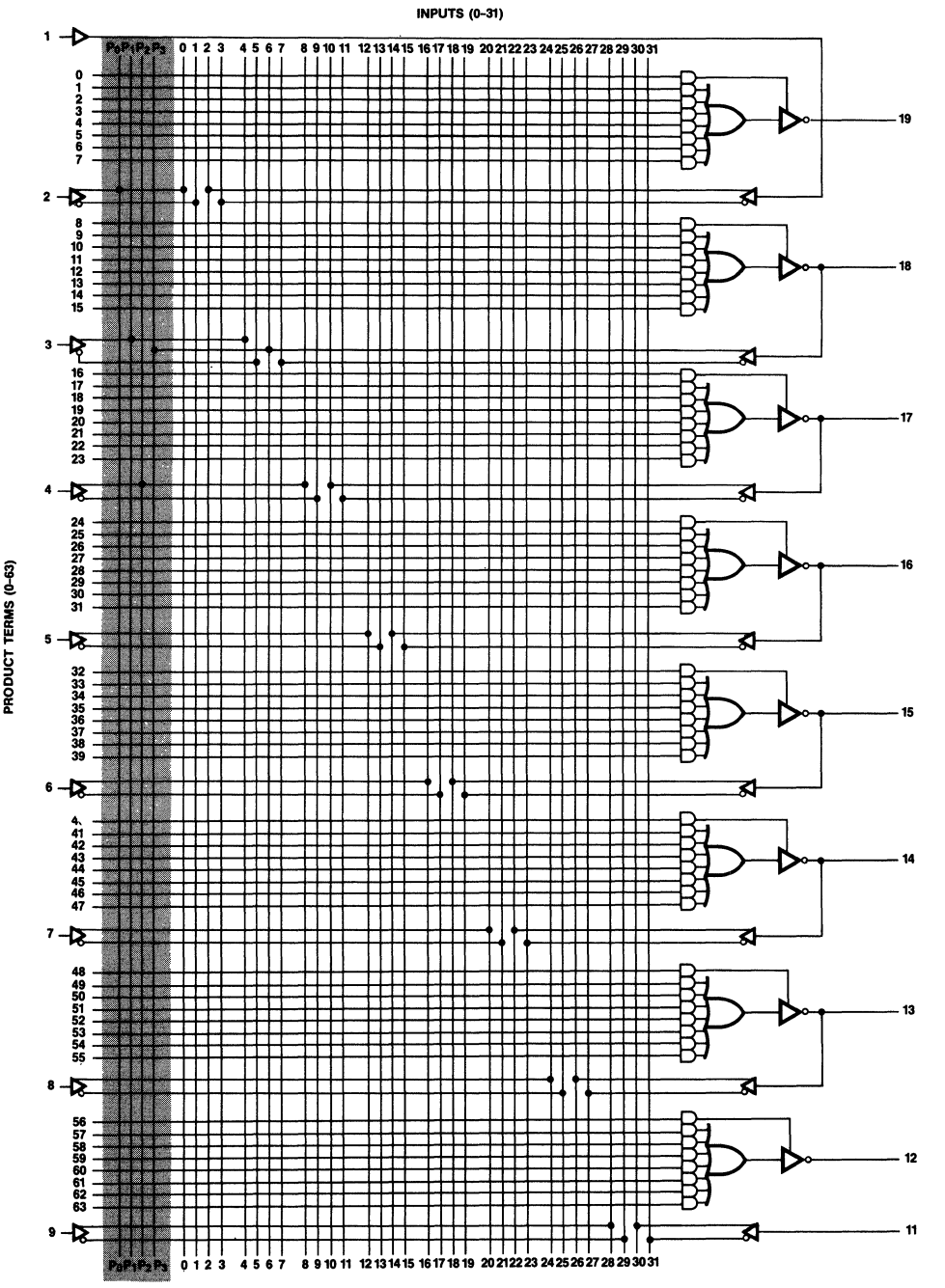
Note 7: C_L includes load and test jig capacitance.

Note 8: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

Note 9: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

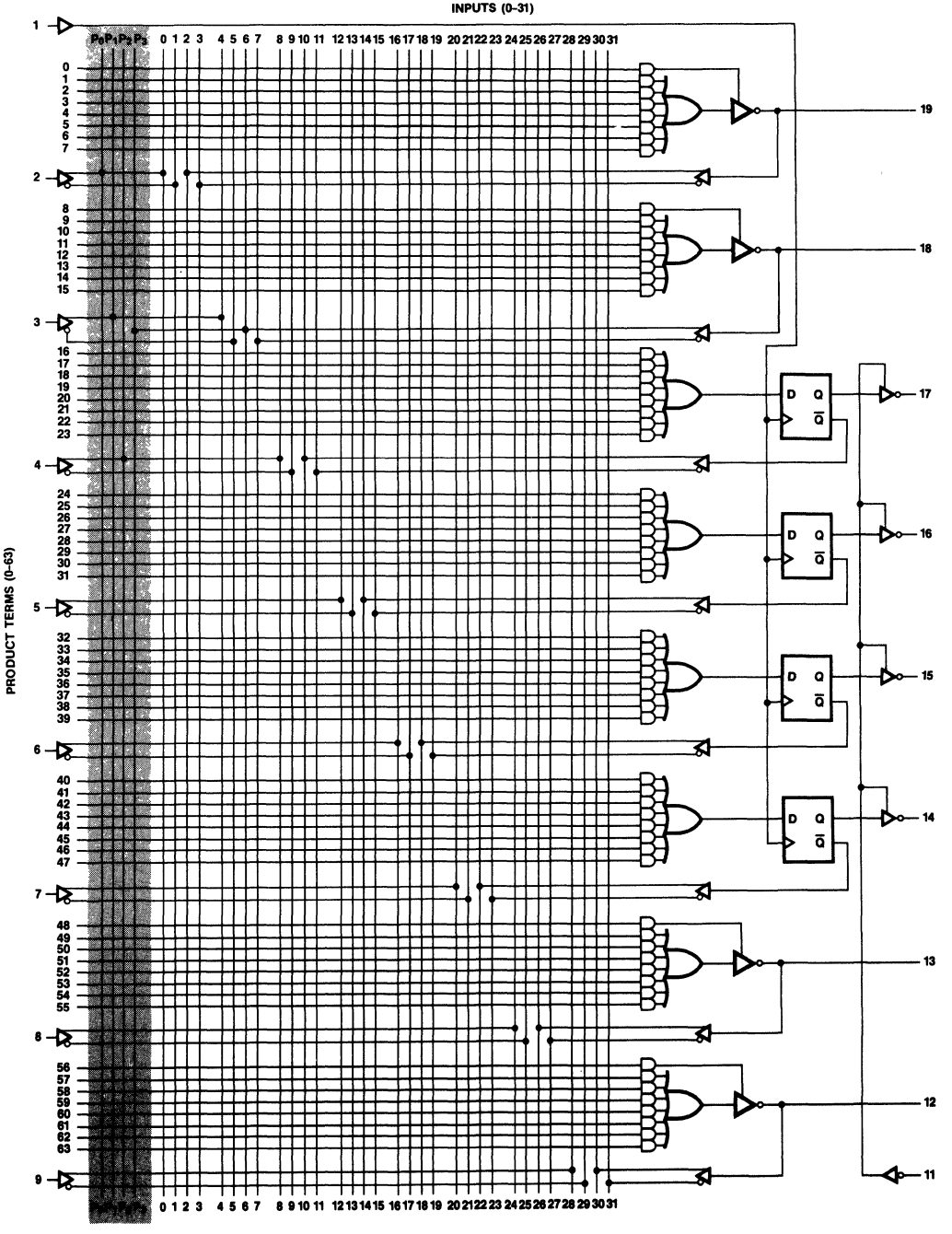
CPL20 FUNCTIONAL LOGIC DIAGRAMS

CPL16L8

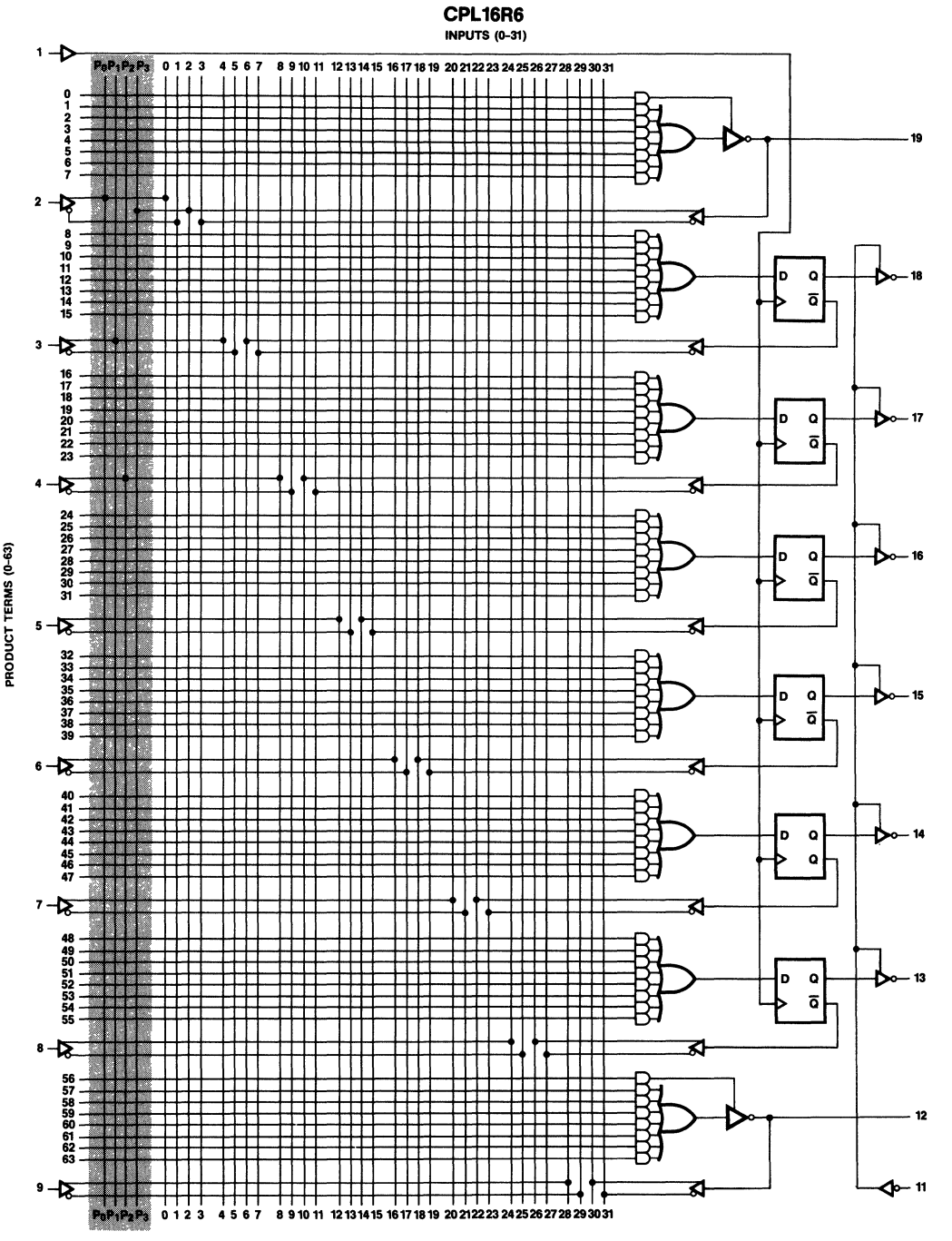


CPL20 FUNCTIONAL LOGIC DIAGRAMS (Continued)

CPL16R4

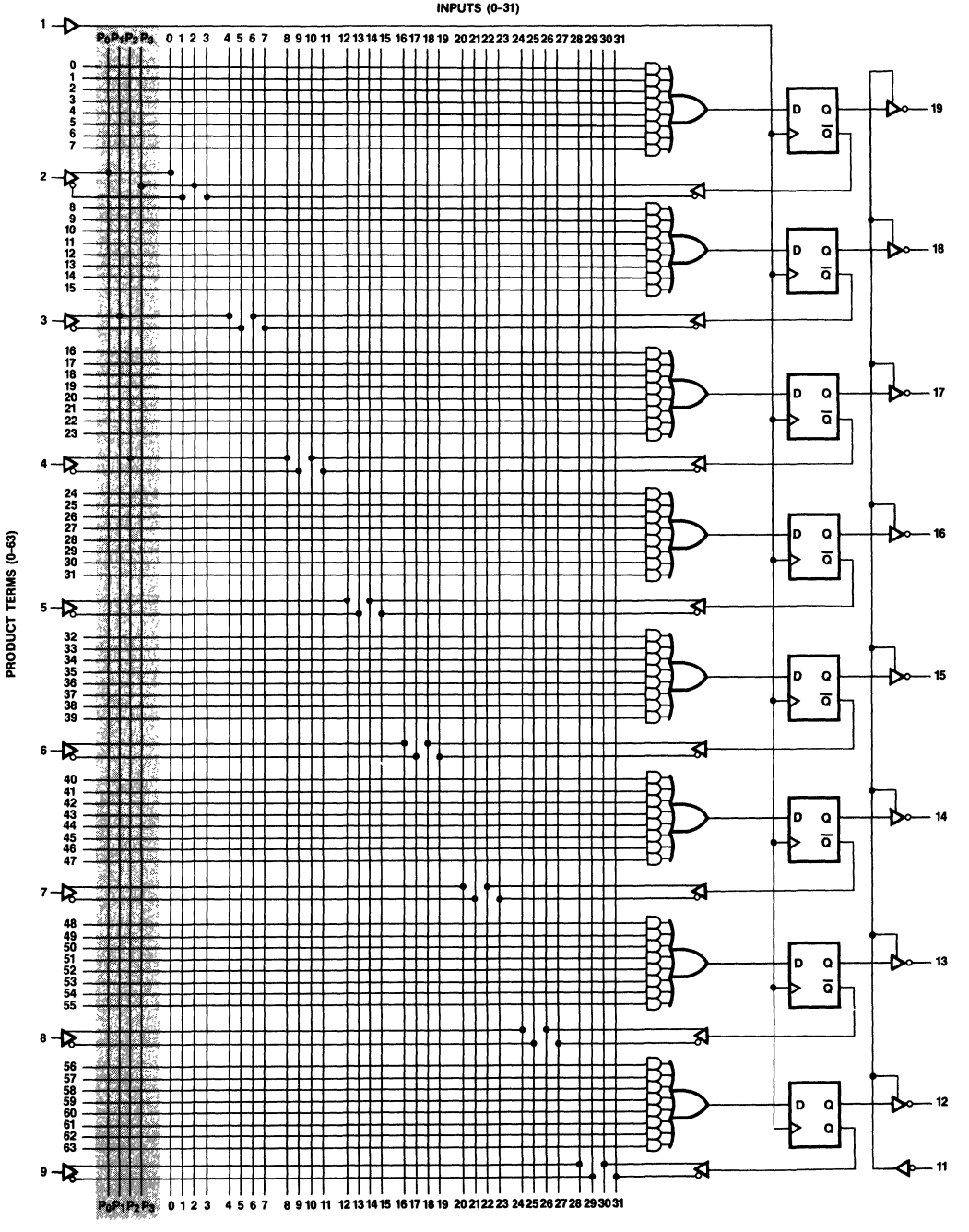


CPL20 FUNCTIONAL LOGIC DIAGRAMS (Continued)



CPL20 FUNCTIONAL LOGIC DIAGRAMS (Continued)

CPL16R8



CPL24

FEATURES/BENEFITS

- High-speed CMOS equivalent to Bipolar PALs
- CMOS UV-erasable EPROM cell to allow reprogrammability
- Low power (45 mA Max. I_{CC}) and Standard (70 mA Max. I_{CC}) versions
- Two speed grades (t_{PD} = 25ns Max. and t_{PD} = 35ns Max.)
- >2000V ESD input and output protection
- 100% functional and AC tested
- 100% programming tested
- Programmable security bit to prevent pattern duplication
- Register preload for register initialization
- Programmable three-state outputs

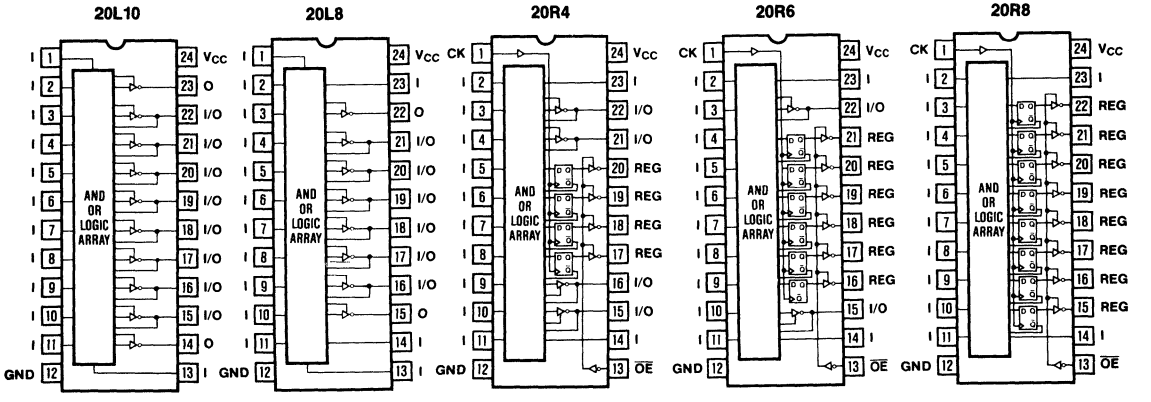
DESCRIPTION

The CPL24 Series devices are high-speed, UV-erasable, electrically programmable CMOS logic replacements of the Bipolar PAL24 family. They utilize the familiar sum-of-products form (AND array followed by an OR array) allowing the user to customize logic to his/her needs.

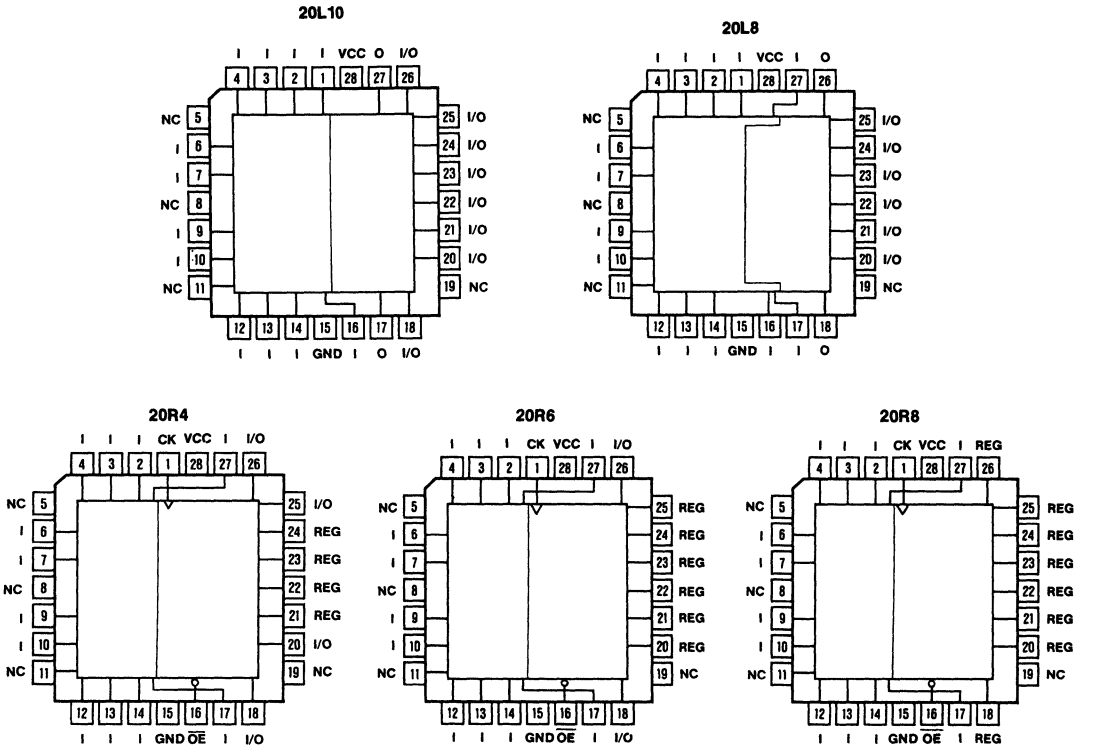
Five devices are offered in the CPL24 Series. They are: the CPL20L10, the CPL20L8, the CPL20R4, the CPL20R6, and the CPL20R8. Each of these devices has 20 array inputs. The CPL20L10 has 10 outputs and the others have 8 outputs. All the outputs to the CPL16L8 and CPL20L10 are combinatorial, while all outputs to the CPL20R8 are registered. In contrast, the CPL20R4 has 4 registered and 4 combinatorial outputs and the CPL20R6 has 6 registered and 2 combinatorial outputs. Each combinatorial output in the CPL20R6 and CPL20R4 devices serves as an I/O pin. The CPL20L10 device has 8 I/O pins, and the CPL20L8 device has 6 I/O pins.

3

LOGIC SYMBOLS AND PINOUTS



LOGIC SYMBOLS AND PINOUTS (Continued)



DESCRIPTION (Continued)

The CPL devices are manufactured using a 1.2 micron EPROM technology which offers low power dissipation (45/70 mA maximum I_{CC}) combined with high performance (25ns maximum propagation delay). Because the CPL devices are erasable, they can be thoroughly tested for programming, functional and AC integrity, resulting in high-reliability and 100% programming yields.

The CPL24 devices are housed in 24-pin plastic DIP, SOIC, and windowed CERDIP packages, as well as a 28-pin PLCC package. The windowed CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The plastic DIP, PLCC, and SOIC devices are one-time-programmable (OTP) and may not be erased.

Register Preload

The register preload feature of the CPL24 Series allows output pins to be loaded with arbitrary states, making functional testing easier than ever.

Security Bit

All CPL24 devices feature a security bit. The security bit allows the user to protect his/her design against unauthorized duplication. When the security bit is set, the contents of the programmable-cell array may not be accessed in Read or Verify modes. Since the CPL devices do not have visible fuses, they offer enhanced security over what is available in bipolar PAL devices.

Test Array

Another feature of the devices in the CPL24 Series is the on-chip test array. It is programmed for final functional and AC testing of the devices after they have been packaged (even if the security bits have been programmed). In the normal operation of the device, the test arrays are not accessed. In the test mode of operation, only the input terms in the shaded portion of the functional block diagram are accessed. The test array facilitates high-reliability as well as simple and short testing.

ERASURE (windowed-CERDIP only)

The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:
Wavelength of 2537 Angstroms
(minimum dose -- 25 Wsec/cm^2)

If an ultraviolet lamp with a 12mW/CM^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL24 ABSOLUTE MAXIMUM RATINGS (Note 1)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leqq$ 20mA)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC}+0.5	V
DC Programming Voltage	V_{PP}	14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Military	T_A	-55 to +125	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions

Parameter	Symbol	Test Conditions		Min	Max	Unit
Low Level Input Voltage	V_{IL}	(Note 4)			0.8	V
High Level Input Voltage	V_{IH}	(Note 4)		2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$		-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	Military I_{OL}=12mA Commercial I_{OL}=24mA		0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	Military I_{OH}=-2mA Commercial I_{OH}=-3.2mA		2.4	V
Off-State Output Leakage Current	I_{OZL}	V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}	V_O = 0.4V		-100	μA
	I_{OZH}		V_O = 2.4V		100	
Output Short-Circuit Current	I_{OS}	V_{CC} = Max, V_O = 0.5V (Note 5)			-300	mA
Power Supply Current	I_{CC}	All inputs = GND V_{CC} = Max I_{OUT} = 0mA	"L" STD MIL		45 70 70	mA mA mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

Note 5: Only one output shorted at a time. Duration of the short circuit should not be more than one second. V_O = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

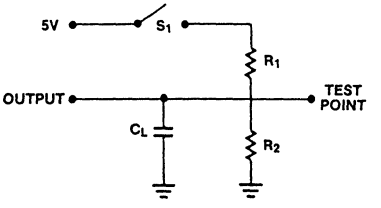
CPL 24 AC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Note 6)

		Commercial				Military				
		-25		-35		-25		-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input or Feedback to Non-Registered Output, 20R6, 20R4, 20L8, 20L10	t_{PD}		25		35		30		40	ns
Clock to Registered Output or Feedback, 20R8, 20R6, 20R4	t_{CO}		15		25		20		25	ns
Pin 13 to Output Enable, 20R8, 20R6, 20R4	t_{PZX13}		20		25		25		25	ns
Pin 13 to Output Disable, 20R8, 20R6, 20R4	t_{PXZ13}		20		25		25		25	ns
Input to Output Enable, 20R6, 20R4, 20L8, 20L10	t_{PZX}		25		35		30		40	ns
Input to Output Disable, 20R6, 20R4, 20L8, 20L10	t_{PXZ}		25		35		30		45	ns
Setup Time from Input or Feedback to Clock, 20R8, 20R6, 20R4	t_{SU}	20		30		25		35		ns
Hold Time, 20R8, 20R6, 20R4	t_H	0		0		0		0		ns
Clock Width (High or Low)	t_W	15		20		20		25		ns
Clock Period	t_P	35		55		45		60		ns
Maximum Frequency	f_{MAX}	28.5		18		22		16.5		MHz

Note 6: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6ns$.

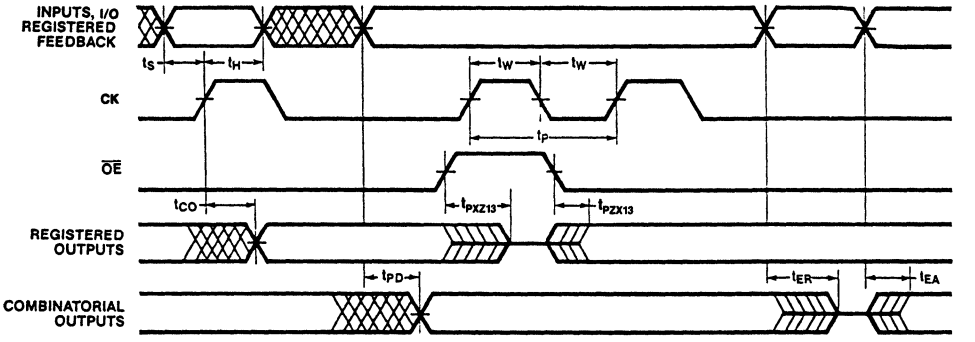
AC Test Circuit



Resistor Values (Ω)

	R1	R2
COM'L	200	390
MIL	390	750

CPL24 WAVEFORMS



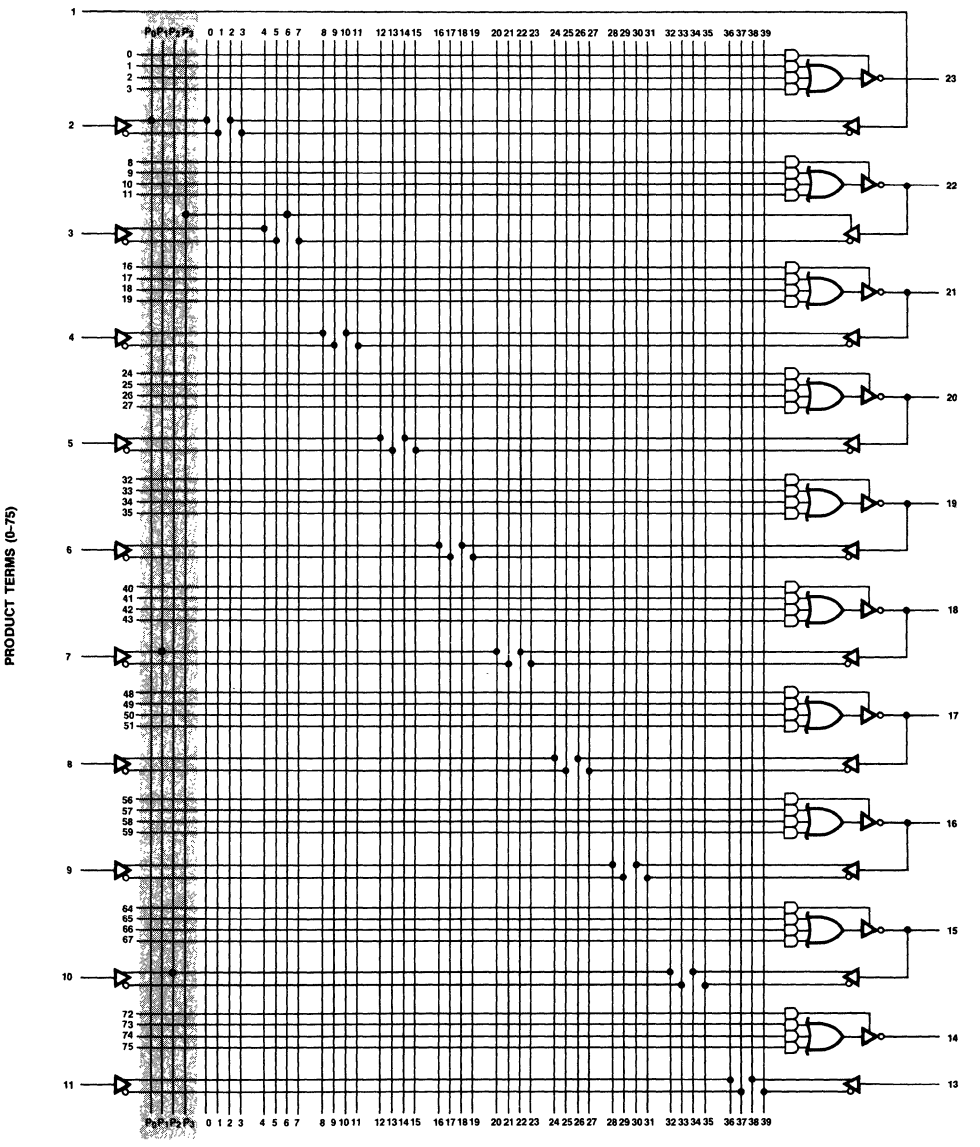
Note 7: C_L includes load and test jig capacitance.

Note 8: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

Note 9: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} – 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

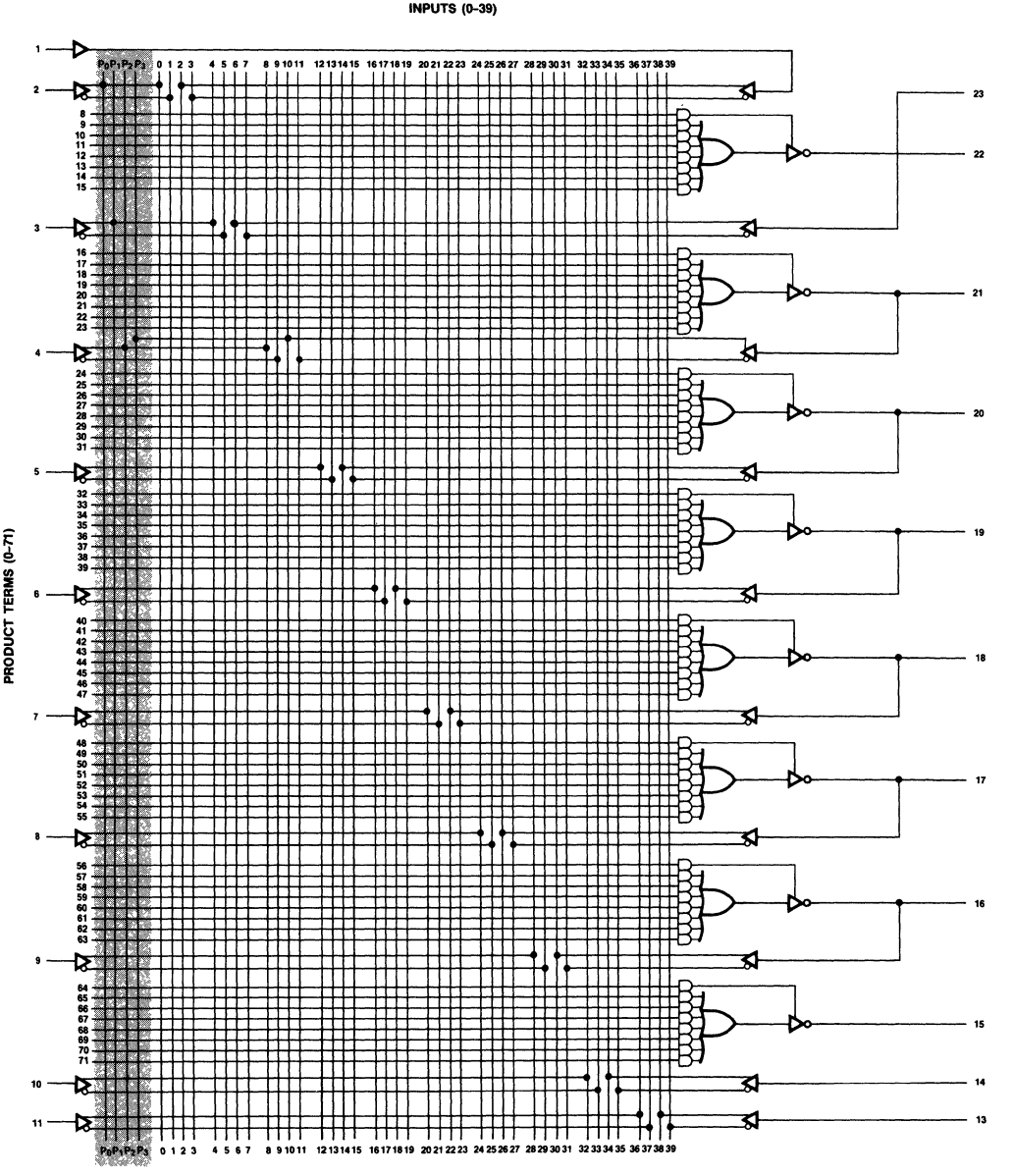
CPL24 FUNCTIONAL LOGIC DIAGRAMS

CPL20L10



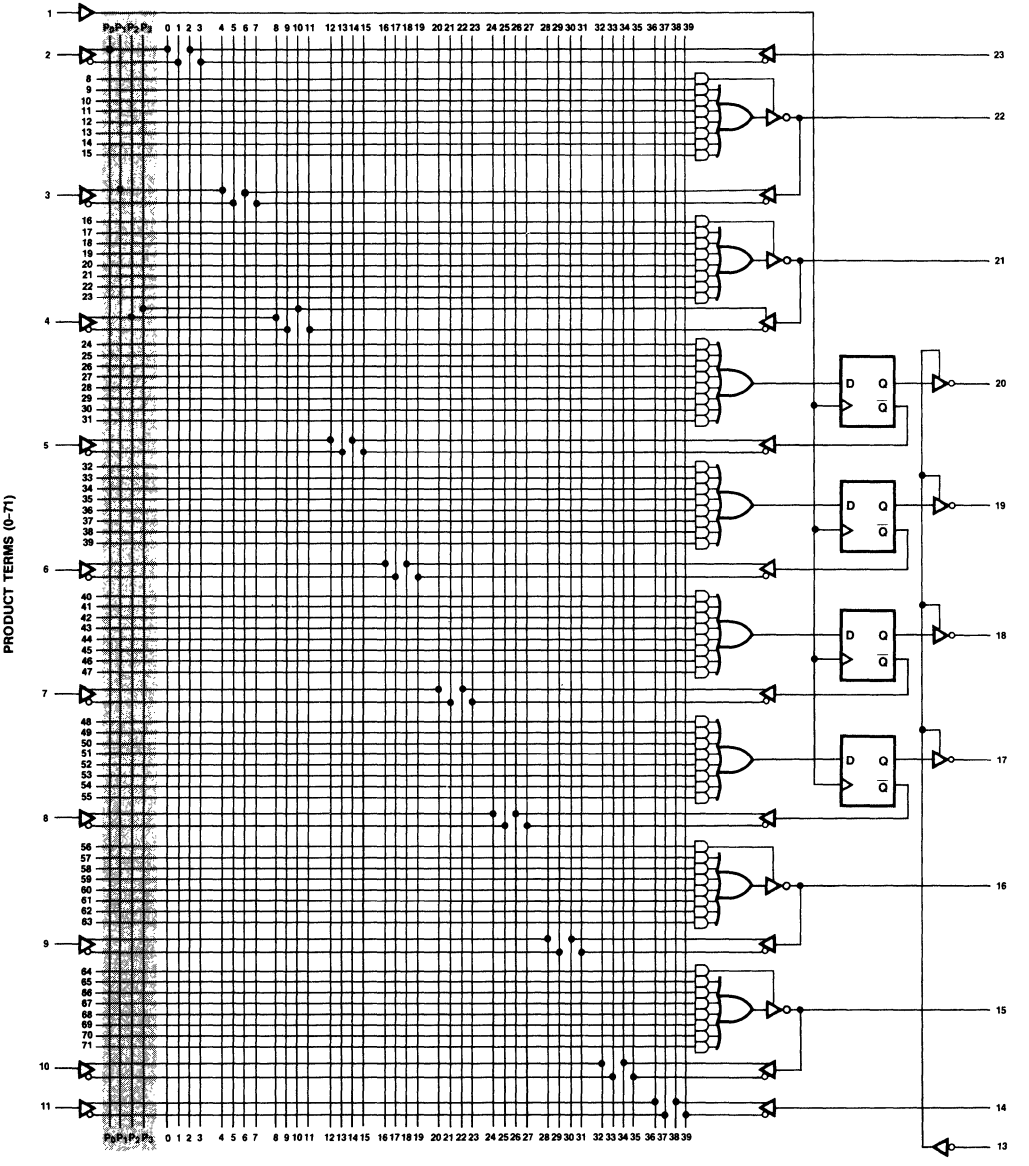
CPL24 FUNCTIONAL LOGIC DIAGRAMS (Continued)

CPL20L8



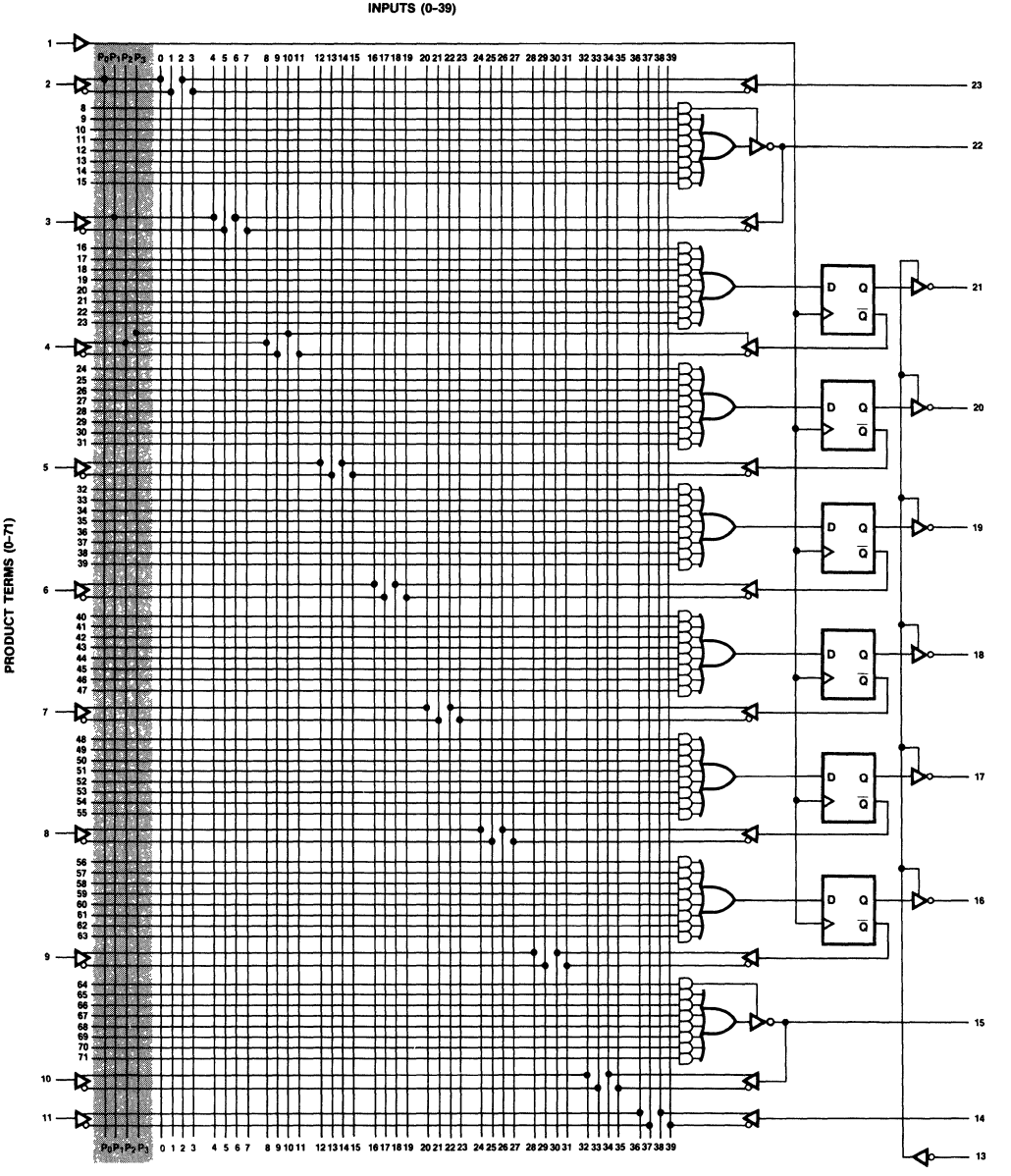
CPL20R4

INPUTS (0-39)

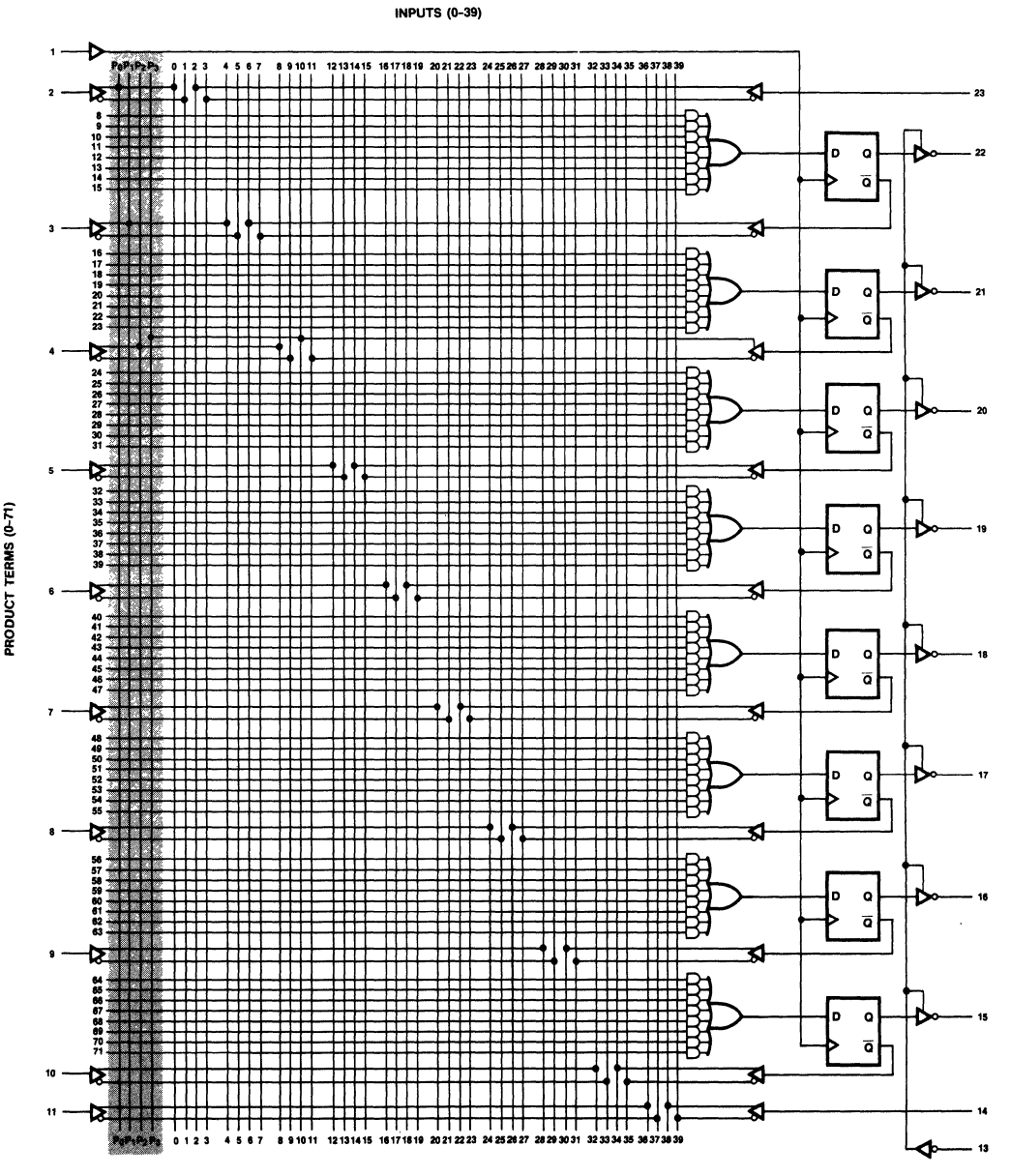


CPL24 FUNCTIONAL LOGIC DIAGRAMS (Continued)

CPL20R6



CPL20R8


INPUTS (0-39)
PRODUCT TERMS (0-71)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
D Q Q
23
22
21
20
19
18
17
16
15
14
13

ADVANCE INFORMATION

CPL22V10
CPL16V8

CPL22V10

CMOS Programmable Logic Array With Output Macrocells (24-Pin)

ADVANCE INFORMATION

FEATURES/BENEFITS

- High speed CMOS programmable alternative to bipolar 22V10 PLDs
- Two speed grades
  t_{PD}= 25ns max., t_{PD}= 35ns max.
- Low power - 90mA max.
- CMOS UV-erasable EPROM cell to allow reprogrammability
- 10 input/output macrocells for maximum flexibility
  - Up to 22 inputs and 10 outputs
  - Programmable output polarity
  - Registered or combinatorial output selection
- Variable product term distribution
  - From 8 to16 product terms available per output
- Global synchronous preset and asychronous reset of all registers
- On power-up, registers reset
- Test array and preloadable output registers for testability
- 100% functional, AC, and programming tested
- >2000V ESD input protection
- Security bit to prevent CPL duplication

DESCRIPTION

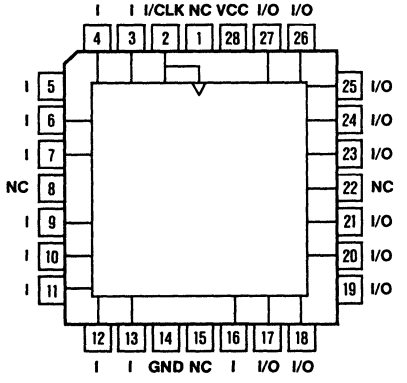
The CPL22V10 is a high-speed CMOS UV-erasable, electrically programmable device with an advanced architecture. The device is manufactured using a 1.2 micron EPROM technology offering low power dissipation combined with high performance. The UV-erasability of the CPL devices allow 100% programming, functional, and AC testing, providing high reliability and 100% programming yields.

The CPL22V10 uses the standard programmable AND/ Fixed OR logic array structure, familiar to most programmable logic users, to implement complex logic functions. Each logic function consists of up to sixteen product terms per output and each product term consists of up to 22 inputs. Each output from the array feeds a programmable macro cell enabling it to be programmed as a combinatorial or registered, active high or low output.

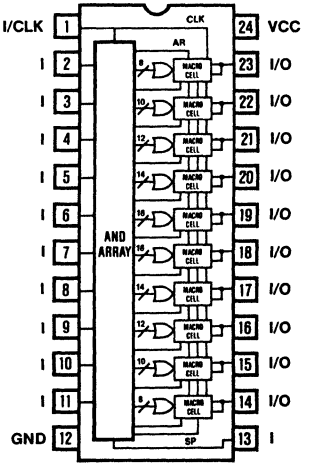
The 22V10 device is housed in a 24-pin plastic DIP, 28-pin PLCC, and a windowed 24-pin CERDIP package. The windowed-CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram the device with a different pattern. The devices in plastic packages are OTP (One-Time-Programmable) devices and may not be erased

3

PIN CONFIGURATIONS



Plastic Leaded Chip Carrier



DIP Package

CPL16V8

CMOS Programmable Logic Array With Output Macrocells (20-pin)

Advance Information

FEATURES/BENEFITS

- Equivalent to industry standard 16V8 architecture
- Two speed grades
  (t_{PD} = 25ns max.,
  t_{PD} = 35ns max.)
- Low power
  45mA active Max I_{CC}
- CMOS UV-erasable EPROM cell to allow reprogrammability
- 8 input/output macrocells for maximum flexibility
  - Up to 16 inputs and 8 outputs
  - Programmable output polarity
  - Registered or Combinatorial output selection
- Test Array and preloadable output registers for testability
- 100% functional, AC, and programming tested
- >2000V ESD input protection
- Programmable Security bit to prevent pattern duplication

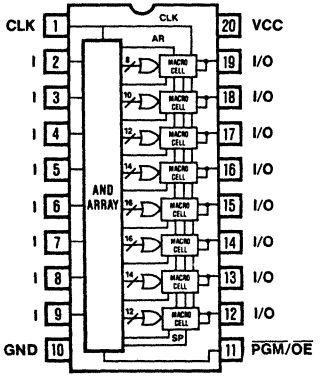
DESCRIPTION

The CPL16V8 is a high-speed CMOS UV-erasable, electrically programmable device with an advanced architecture. The device is manufactured using a 1.2 micron EPROM technology offering low power dissipation combined with high performance. The UV-erasability of the CPL devices allow 100% programming, functional, and AC testing, providing high reliability and 100% programming yields.

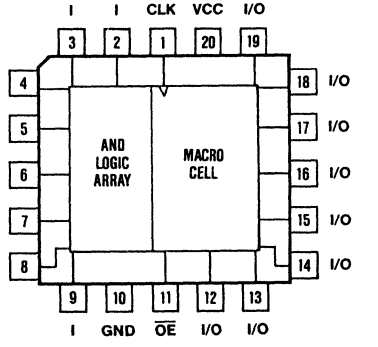
The CPL16V8 uses the standard programmable AND/ Fixed OR logic array structure, familiar to most programmable logic users, to implement complex logic functions. Each logic function consists of up to eight product terms per output, and each product term consists of up to 16 inputs. Each output from the array feeds a programmable macro cell enabling it to be programmed as a combinatorial or registered, active high or low output.

The 16V8 device is housed in a 20-pin plastic DIP, 20-pin PLCC, and a windowed 20-pin CERDIP package. The windowed-CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram the device with a different pattern. The devices in plastic packages are OTP (One-Time-Programmable) devices and may not be erased.

PIN CONFIGURATIONS



DIP Package



Plastic Leaded Chip Carrier

CPL PROGRAMMING ELECTRICAL SPECIFICATIONS

Programming Samsung's CMOS PLDs

Samsung's CPL (CMOS programmable logic) devices use an EPROM programming technology which emphasizes complete testability (100% programming, functional, and AC) and high performance. Testability is inherent to the technology because it allows devices to be programmed and reprogrammed many times. High performance is achieved using a two-transistor EPROM cell which optimizes the speed of both read and write transistors. This results in CPL devices being as fast as many of their bipolar counterparts, and since they are fully tested prior to delivery to the customer, they provide higher programming yields.

Samsung's CPL devices are programmed using high voltage pulses, from 100 microseconds to 10 milliseconds in duration, which produce about 50 mA of programming current. At one time, eight to ten EPROM cells are programmed, depending on the device.

CPL EPROM cells are programmed by charging a floating gate with electrons and unprogrammed by irradiating the cells with ultraviolet (UV) light, making complete testing of all circuitry possible before shipping. (Bipolar parts, which use fuse cells, on the other hand, can be programmed only once, making 100% AC testing impossible.) By using special on-chip test arrays, additional functional and AC testing of CPL devices can also be performed without having to program the devices. Also, if the devices are contained in windowed packages, they may be programmed and erased, at the customer site a number of times, allowing the designer to test, develop, and fine-tune his/her logic without having to replace each programmed device.

CPL 20 Series *(CPL16L8, CPL16R4, CPL16R6, CPL16R8)*

The critical AC and DC parameters for programming the CPL 20 series devices are listed in Tables 1 and 2. The minimum and maximum parameter values are given for an ambient temperature of 25°C.

The pin configuration for programming the CPL 20 series parts is given in Figure 1. Notice that pin 1 is now called Vpp. It is raised to a programming voltage, Vpp, during programming (see Table 1). In this mode, pins 2 - 9 are used for addressing each location to be programmed and pins 12 - 19 are used for supplying data. Pin 11, the PGM/~OE pin, is the READ/WRITE pin in the programming mode. When it is raised to the programming voltage, Vpp, a write occurs and the data on the output pins is written into the addressed array locations. When it is switched to a logic LOW, a read occurs and the contents of the addressed locations can be checked or verified. When pin 11 is switched to a logic HIGH, the device is inhibited and the outputs go into a high impedance (Z) state.

The CPL devices are programmed one byte at a time for a total of 256 (32 input terms, 8 wide) bytes of memory. This memory can be addressed once the array is programmed. The addresses are selected via pins 2 - 9 (A0 - A7). Pins 2 - 4 select one of eight product terms (or outputs) as shown in Table 3, whereas pins 5 - 9 select one of 32 input terms according to Table 4. The test input terms can be selected, as in Table 5, by raising pin 7 to Vpp and entering the test programming mode of operation. Here, the duplicated memory cells of the test array are addressed at the same locations as the 0, 1, 2, and 3 product terms. (The test arrays, having 32 bytes of memory, are provided for the purpose of post-assembly testing and are disconnected in normal operation.)

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	13.0	14.0	V
V_{CC}	Supply Voltage During Programming	4.75	5.25	V
V_{IH}	Programming Input High Voltage	3.0		V
V_{IL}	Programming Input Low Voltage		0.4	V
$V_{OH}(1)$	Output High Voltage	2.4		V
$V_{OL}(1)$	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Voltage		50	mA

(1) During verify operation

Table 1. DC Programming Parameters (at 25°C)

Parameter	Description	Min.	Max.	Units
t_{PP} (2)	Programming Pulse Width	100	10,000	µs
t_{SU}	Setup Time	1.0		µs
t_H	Hold Time	1.0		µs
t_r, t_f (2)	Vpp Rise and Fall Time	1.0		µs
t_{VD}	Delay to Verify	1.0		µs
t_{VP}	Verify Pulse Width	2.0		µs
t_{DV}	Verify to Data Valid	20.0		µs
t_{DZ}	Verify to High Z		1.0	µs

(2) Measured at 10% and 90% voltage levels

Table 2. AC Programming Parameter (at 25°C)

Selecting the address pins 2 - 9, whether in the normal or test modes, leaves one byte of cells available for programming. The data to be programmed is sent via data inputs D0 - D7 to every 8th product term (in groups of 8: 0, 8, 16, 24, 32, 40, 48, and 56). Note that there is a one-to-one correlation between each data input and its respective product term. For example, a "1" on data input D0 programs product term 0, a "1" on data input D1 programs product term 8, etc. After each byte of cells is programmed, the product term decoder (pins 2 - 4) is incremented by one, until all 64 product terms are addressed. As a result, each of the input terms is addressed eight times. After verification, the input term decoder (pins 5 - 9) is incremented by one and the sequence repeated 32 times.

In the unprogrammed state, each input is connected to each product term. When a logic level HIGH on a data line is presented during programming, the memory cell is disconnected from the selected input term and product term (like a blown fuse using bipolar technology). During the verify operation, which can be used to check if the part is blank or is correctly programmed, an unprogrammed cell causes a logic level HIGH to appear on the output, and a programmed cell causes a logic level LOW to appear on the output. A summary of the programming operating modes with appropriate pin assignments for Samsung's CPL 20 series devices is shown in Table 6. The corresponding programming waveforms for the standard array and for the test array are shown in Figures 2 and 3. The waveforms for securing the logic of the CPL20X parts is illustrated in Figure 4, whereas the waveforms for verifying that the parts are secured (unable to read back programmed information) are shown in Figure 5. Note that the security bit is programmed using a single 10 ms pulse (pin 11).

Finally, the actual sequence that is used to program the standard and test memory cells is described in the form of a flowchart in Figure 6.

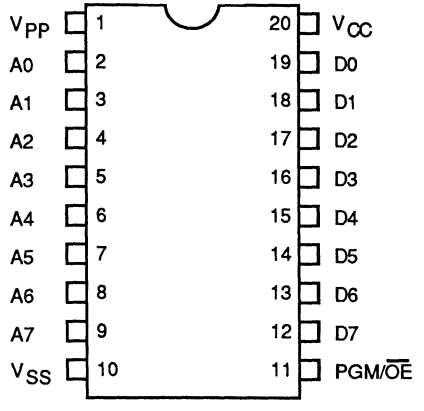


Figure 1. CPL20 Programming Pin Configuration

Product Term Line Number								Pin Number		
								2	3	4
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	H	L	L
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	H	H	L
4	12	20	28	36	44	52	60	L	L	H
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	L	H	H
7	15	23	31	39	47	55	63	H	H	H
Do	D1	D2	D3	D4	D5	D6	D7			
Data Inputs, Pins 12 through 19										

L = V_{IL} or 0.4V Max.
H = V_H or 3.0V Min.

Table 3. Product Term Address Decodes for CPL20 Family

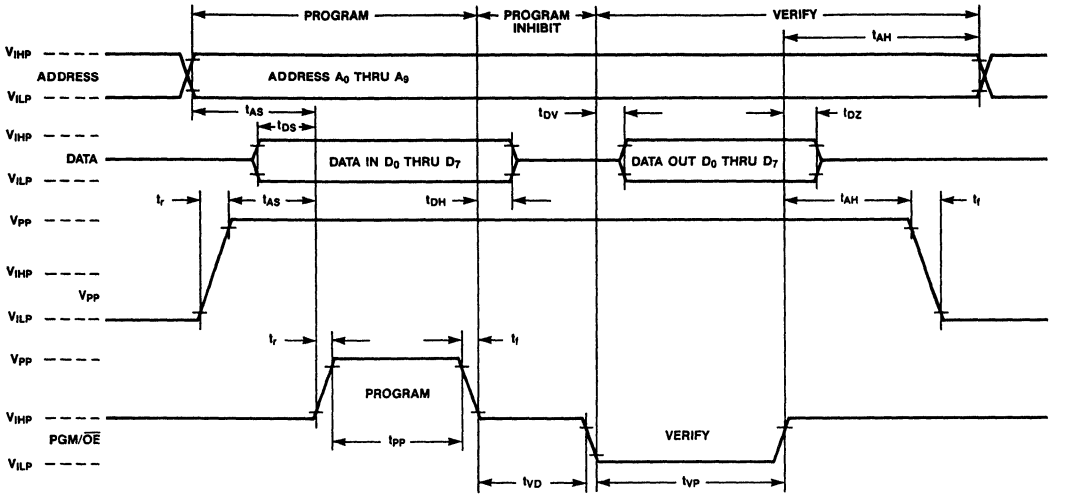


Figure 2. Programming Waveforms Normal Array

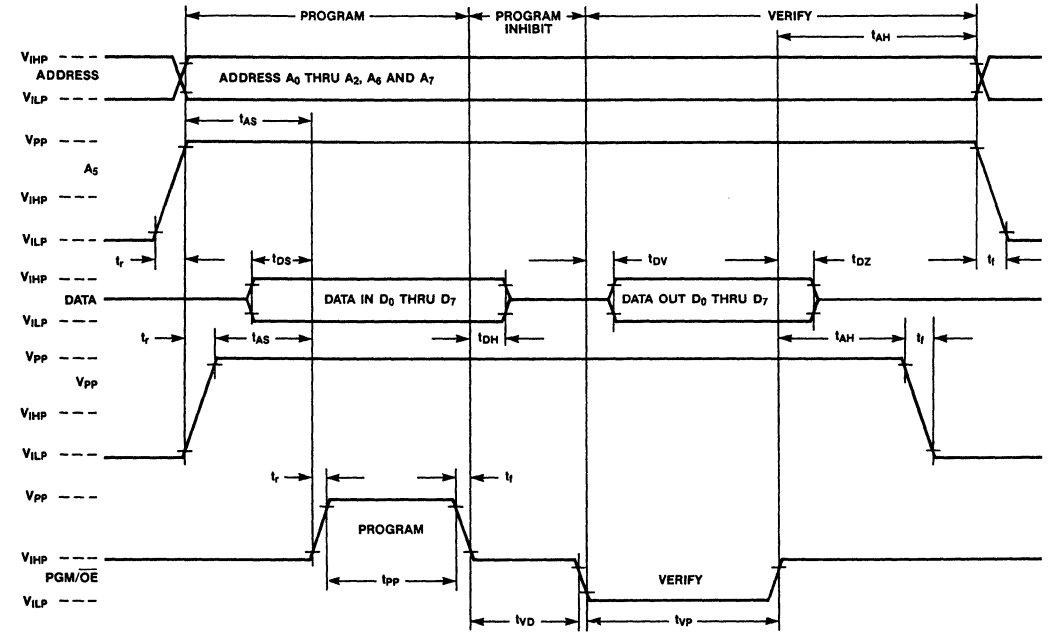


Figure 3. Program Waveforms Test Array

Input Term Line Number	Pin Number				
	5	6	7	8	9
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	L

Input Term Line Number	Pin Number				
	5	6	7	8	9
16	L	L	L	L	H
17	H	L	L	L	H
18	L	L	L	L	H
19	H	L	L	L	H
20	L	H	H	L	H
21	H	H	H	L	H
22	L	H	H	L	H
23	H	H	H	L	H
24	L	L	L	H	H
25	H	L	L	H	H
26	L	L	L	H	H
27	H	L	L	H	H
28	L	H	H	H	H
29	H	H	H	H	H
30	L	H	H	H	H
31	H	H	H	H	H

L = V_{IL} or 0.4V Max.
H= V_{IH} or 3.0V Min.

Table 4. Input Term Address Decodes for CPL20 Family

Test Term Line Number	Pin Number		
	7	8	9
P0	V_{PP}	L	L
P1	V_{PP}	H	L
P2	V_{PP}	L	H
P3	V_{PP}	H	H

L = V_{IL} or 0.4V Max.
H= V_{IH} or 3.0V Min.

Table 5. Test Term Address Decodes for CPL20 Family

Operating Mode \ Pin Name / Pin Number	V_{PP} 1	PGM/ ~OE 11	A0 2	A1 3	A2 4	A3 5	A4 6	A5 7	A6 8	A7 9	D9 - D0 12 - 19
Regular PAL Logic (1)	CK/HL	HL	HL	HL	HL	HL	HL	HL	HL	HL	Logic Function Out
Program PAL	V_{PP}	V_{PP}	A	A	A	A	A	A	A	A	Program Data In
Program Inhibit	V_{PP}	V_{IH}	X	X	X	X	X	X	X	X	High Z
Program Verify	V_{PP}	V_{IL}	A	A	A	A	A	A	A	A	Programmed Data Out
Test PAL Logic (1)	CK/X	X	HL	HL	HL	X	V_{PP}	X	X	X	Logic Function Out
Program Test PAL (3)	V_{PP}	V_{PP}	A	A	A	X	X	V_{PP}	A	A	Program Data In
Program Test Inhibit (3)	V_{PP}	V_{IH}	A	A	A	X	X	V_{PP}	A	A	High Z
Program Test Verify (3)	V_{PP}	V_{IL}	A	A	A	X	X	V_{PP}	A	A	Programmed Data Out
Program Security Bit	V_{PP}	V_{PP}	X	V_{PP}	X	X	X	X	X	X	High Z
Verify Security Bit	X	X	X	(2)	V_{PP}	X	X	X	X	X	High Z
Register Preload	X	X	X	X	X	V_{PP}	X	X	X	X	Data Input to Register

(1) See data sheet for actual I /O configuration
(2) Pin 3 = V_{OL} ; Data security is in effect
Pin 3 = V_{OH} ; Data is unsecured and may be accessed
(3) Pin 7 selects the test mode of operation and must be taken to V_{PP} before selecting test program operation with pin 1 taken to V_{PP}

HL = TTL logic Input level
A = Address input level
X = Don't care ; GND < X < V_{CC}
V_{IL} = 0.4V (Max.)
V_{IH} = 3.0 V (Min.)
V_{PP} = 13.5V (13.0 v - 14.0 V)

Table 6. CPL20 Programming Operating Modes

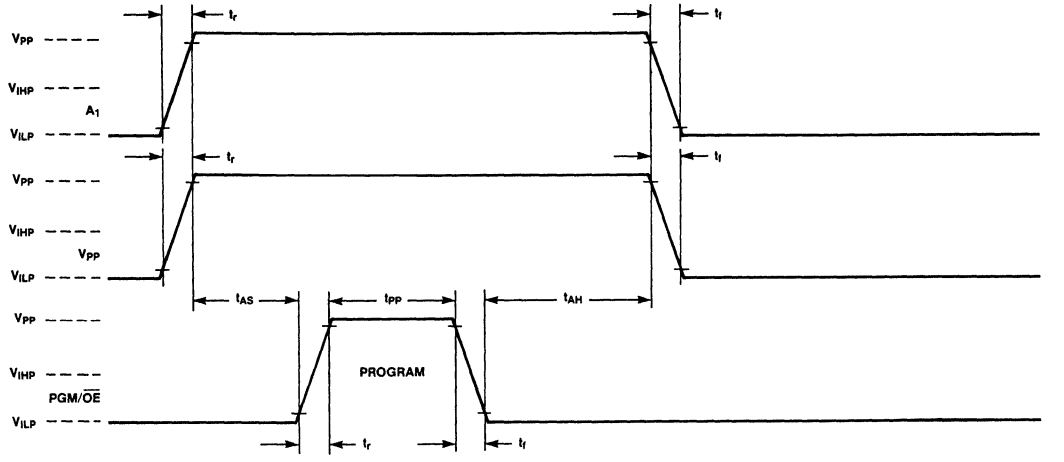


Figure 4. Activating Program Security

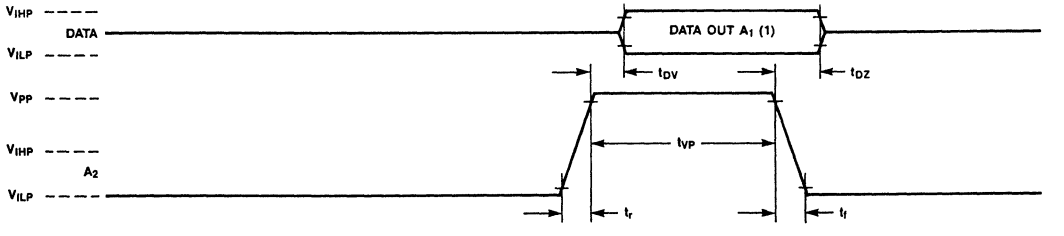


Figure 5. Verify Program Security

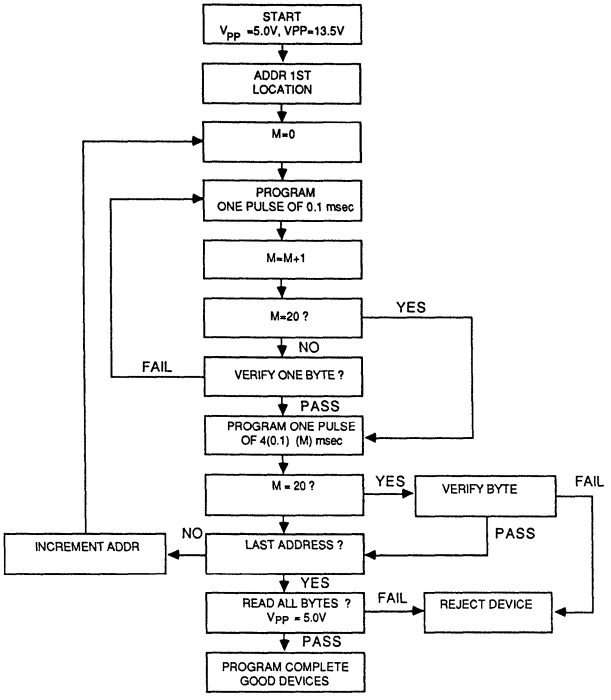


Figure 6. CPL20 Programming Flow Chart

CPL 24 Series

(CPL20L10, CPL20L8, CPL20R4, CPL20R6, CPL20R8)

The critical AC and DC parameters for programming the CPL 24 series devices are listed in Tables 7 and 8. The minimum and maximum parameter values are given for an ambient temperature of 25°C.

The pin configuration for programming the CPL 24 series parts is given in Figure 7. Notice that pin 1 is now called Vpp. It is raised to a programming voltage, Vpp, during programming (see Table 7). In this mode, pins 2 - 11 are used for addressing each location to be programmed and pins 14 - 23 are used for supplying data. Pin 13, the PGM/ ~OE pin, is the READ/WRITE pin in the programming mode. When it is raised to the programming voltage, Vpp, a write occurs and the data on the output pins is written into the addressed array locations. When it is switched to a logic LOW, a read occurs and the contents of the addressed locations can be checked or verified. When pin 13 is switched to a logic HIGH, the device is inhibited and the outputs go into a high impedance (Z) state.

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	13.0	14.0	V
V_{CC}	Supply Voltage During Programming	4.75	5.25	V
V_{IH}	Programming Input High Voltage	3.0		V
V_{IL}	Programming Input Low Voltage		0.4	V
V_{OH}(1)	Output High Voltage	2.4		V
V_{OL} (1)	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Voltage		50	mA

(1) During verify operation

Table 7. DC Programming Parameters (at 25°C)

Parameter	Description	Min.	Max.	Units
t_{PP} (2)	Programming Pulse Width	100	10,000	µs
t_{SU}	Setup Time	1.0		µs
t_H	Hold Time	1.0		µs
t_r, t_f (2)	Vpp Rise and Fall Time	1.0		µs
t_{VD}	Delay to Verify	1.0		µs
t_{VP}	Verify Pulse Width	2.0		µs
t_{DV}	Verify to Data Valid	20.0		µs
t_{DZ}	Verify to High Z		1.0	µs

(2) Measured at 10% and 90% voltage levels

Table 8. AC Programming Parameter (at 25°C)

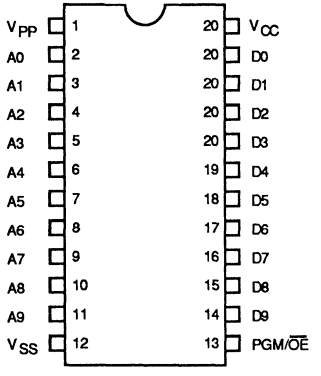


Figure 7. CPL24 Programming Pin Configuration

All of the CPL 24 pin devices, except the CPL20L10, are programmed one byte at a time for a total of 256 bytes of memory. The CPL20L10 is programmed 10 bits at a time for a total of 128 x 10 bits of memory. The memory can be addressed once the array is programmed. The addresses are selected via pins 2 - 11 (A0 - A9). Specifically, pins 2-4 select one of eight product terms (or pins 8 and 9 select one of four product terms for the CPL20L10) for each output as shown in Tables 9A and 9B, whereas pins 5-10 (or pins 2-7 for the CPL20L10) select one of 32 input terms as shown in Table 10. The test input terms can be selected, as in Table 11, by raising pin 7 to Vpp and entering the test programming mode of operation. Here, the duplicated memory cells of the test array are addressed at the same locations as the 0, 1, 2, and 3 product terms. (The test arrays are provided for the purpose of post- assembly testing and are disconnected in normal operation.)

Product Term Line Number								Pin Number		
								2	3	4
8	16	24	32	40	48	56	64	L	L	L
9	17	25	33	41	49	57	65	H	L	L
10	18	26	34	42	50	58	66	L	H	L
11	19	27	35	43	51	59	67	H	H	L
12	20	28	36	44	52	60	68	L	L	H
13	21	29	37	45	53	61	69	H	L	H
14	22	30	38	46	54	62	70	L	H	H
15	23	31	39	47	55	63	71	H	H	H

L = V_{IL} or 0.4V Max.
H= V_H or 3.0V Min.

Table 9A. Product Term Address Decodes for CPL24 Family, except CPL20L10

Product Term Line Number									Pin Number	
									8	9
0	8	16	24	32	40	48	56	64	L	L
1	9	17	25	33	41	49	57	65	H	L
2	10	18	26	34	42	50	58	66	L	H
3	11	19	27	35	43	51	59	67	H	H

L = V_{IL} or 0.4V Max.
H= V_H or 3.0V Min.

Table 9B. Product Term Address Decodes for CPL20L10

Input Term Line Number	Pin Number					
	5/2*	6/3*	7/4*	8/5*	9/6*	10/7*
0	L	L	L	L	L	L
1	H	L	L	L	L	L
2	L	H	L	L	L	L
3	H	H	L	L	L	L
4	L	L	H	L	L	L
5	H	L	H	L	L	L
6	L	H	H	L	L	L
7	H	H	H	L	L	L
8	L	L	L	H	L	L
9	H	L	L	H	L	L
10	L	H	L	H	L	L
11	H	H	L	H	L	L
12	L	L	H	H	L	L
13	H	L	H	H	L	L
14	L	H	H	H	L	L
15	H	H	H	H	L	L
16	L	L	L	L	H	L
17	H	L	L	L	H	L
18	L	H	L	L	H	L
19	H	H	L	L	H	L
20	L	L	H	L	H	L
21	H	L	H	L	H	L
22	L	H	H	L	H	L
23	H	H	H	L	H	L
24	L	L	L	H	H	L
25	H	L	L	H	H	L
26	L	H	L	H	H	L
27	H	H	L	H	H	L
28	L	L	H	H	H	L
29	H	L	H	H	H	L
30	L	H	H	H	H	L
31	H	H	H	H	H	L
32	L	L	L	L	L	H
33	H	L	L	L	L	H
34	L	H	L	L	L	H
35	H	H	L	L	L	H
36	L	L	H	L	L	H
37	H	L	H	L	L	H
38	L	H	H	L	L	H
39	H	H	H	L	L	H

*CPL20L10 only

L = V_{IL} or 0.4V Max.
H= V_{IH} or 3.0V Min.

Table 10. Input Term Address Decodes for CPL24 Family

Selecting the address pins 2 - 11, whether in the normal or test modes, leaves one byte of cells (or 10 bits for the CPL20L10) available for programming. The data to be programmed is sent via data inputs D0 - D7 to every 8th product term (in groups of 8: 8, 16, 24, 32, 40, 48, 56, and 64 or 0, 8, 16, 24, 32, 40, 48, 56, 64, and 72 for the CPL20L10). Note that there is a one-to-one correlation between each data input and its respective product term. For a CPL20L8, for example, a "1" on data input D0 programs product term 8, a "1" on data input D1 programs product term 16, etc. After each byte of cells is programmed, the product term decoder (pins 8 - 10) is incremented by one until all 64 (40) product terms are addressed. As a result, each of the product terms is addressed eight (four) times. After verification, the input decoder (pins 2 - 7) is incremented by one and the sequence repeated 32 times.

In the unprogrammed state, each input is connected to each product term. When a logic level HIGH on a data line is presented during programming, the memory cell is disconnected from the selected input term and product term (like a blown fuse using bipolar technology). During the verify operation, which can be used to check if the part is blank or correctly programmed, an unprogrammed cell causes a logic level HIGH to appear on the output, and a programmed cell causes a logic level LOW to appear on the output.

A summary of the programming operating modes with appropriate pin assignments for Samsung's CPL24 series devices is shown in Table 12. The corresponding programming waveforms for the standard array and for the test array are shown in Figures 8 and 9. The waveforms for securing the logic of the CPL24 parts are illustrated in Figure 10, whereas the waveforms for verifying that the parts are secured (unable to read back programmed information) are shown in Figure 11. Note that the security bit is programmed using a single 10 milliseconds pulse (pin 13).

Finally, the actual sequence that is used to program the standard and test memory cells is described in the form of a flowchart in Figure 12.

Test Term Line Number	Pin Number		
	8/4*	9/5*	7
P0	L	L	V_{PP}
P1	H	L	V_{PP}
P2	L	H	V_{PP}
P3	H	H	V_{PP}

*CPL20L10 only
L = V_{IL} or 0.4V Max.
H= V_{IH} or 3.0V Min.

Table 11. Test Term Address Decodes for CPL24 Family

Operating Mode \ Pin Name / Pin Number	V_{PP} 1	PGM/~OE 13	A0 2	A1 3	A2 4	A3 5	A4 6	A5 7	A6 8	A7 9	A7 10	A7 11	D9 - D0 14-23
Regular PAL Logic (1)	CK/HL	HL	HL	HL	HL	HL	HL	HL	HL	HL	HL	HL	Logic Function Out
Program PAL	V_{PP}	V_{PP}	A	A	A	A	A	A	A	A	A/X(5)	x	Program Data In
Program Inhibit	V_{PP}	V_{IL}	X	X	X	X	X	X	X	X	X	X	High Z
Program Verify	V_{PP}	V_{IH}	A	A	A	A	A	A	A	A	A/X(5)	x	Programmed Data Out
Test PAL Logic (1)	CK/X	X	HL	HL/X(5)	HL/X(5)	X	V_{PP}	X/HL(5)	X	X	X/HL(5)	X	Logic Function Out
Program Test PAL (3)	V_{PP}	V_{PP}	A/X(5)	A/X(5)	A	X/A(5)	X	V_{PP}	A	A	X	X	Program Data In
Program Test Inhibit (3)	V_{PP}	V_{IH}	A/X(5)	A/X(5)	A	X/A(5)	X	V_{PP}	A	A	X	X	High Z
Program Test Verify (3)	V_{PP}	V_{IL}	A/X(5)	A/X(5)	A	X/A(5)	X	V_{PP}	A	A	X	X	Programmed Data Out
Program Security Bit	V_{PP}	V_{PP}	X	V_{PP}	X	X	X	X	X	X	X	X	High Z
Verify Security Bit	X	X	X	(2)	V_{PP}	X	X	X	X	X	X	X	High Z
Program output polarity	V_{PP}	V_{PP}	X	X	X	X	X	X	X	V_{PP}	X	X	High Z
Verify output polarity	X	X	X	X	X	X	X	X	X	(4)	V_{PP}	X	High Z
Register Preload (6)	X	X	X	X	X	V_{PP}	X	X	X	X	X	X	Data Input to Register

(1) See data sheet for actual I /O configuration
(2) Pin 3 = V_{OL} ; Data security is in effect
Pin 3 = V_{OH} ; Data is unsecured and may be accessed
(3) Pin 7 selects the test mode of operation and must be taken to V_{PP} before selecting test program operation with pin 1 taken to V_{PP}
(4) Pin 9 = V_{OL} ; Erased bit asserted low at output
(5) For CPL20L10 only
(6) For registered parts only.

HL = TTLlogic Input level
A = Address Input level
X = Don't care ; GND < X < VCC
V_{IL} = 0.4V (Max.)
V_{IH} = 3.0 V (Min.)
V_{PP} = 13.5V (13.0 v - 14.0 V)

4

Table 12. CPL24 Programming Operating Modes

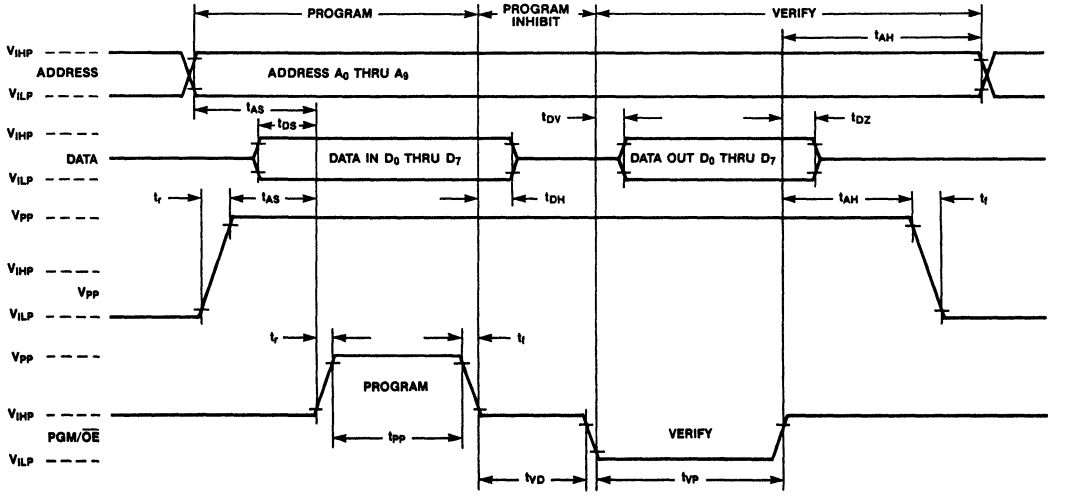


Figure 8. Programming Waveforms Normal Array

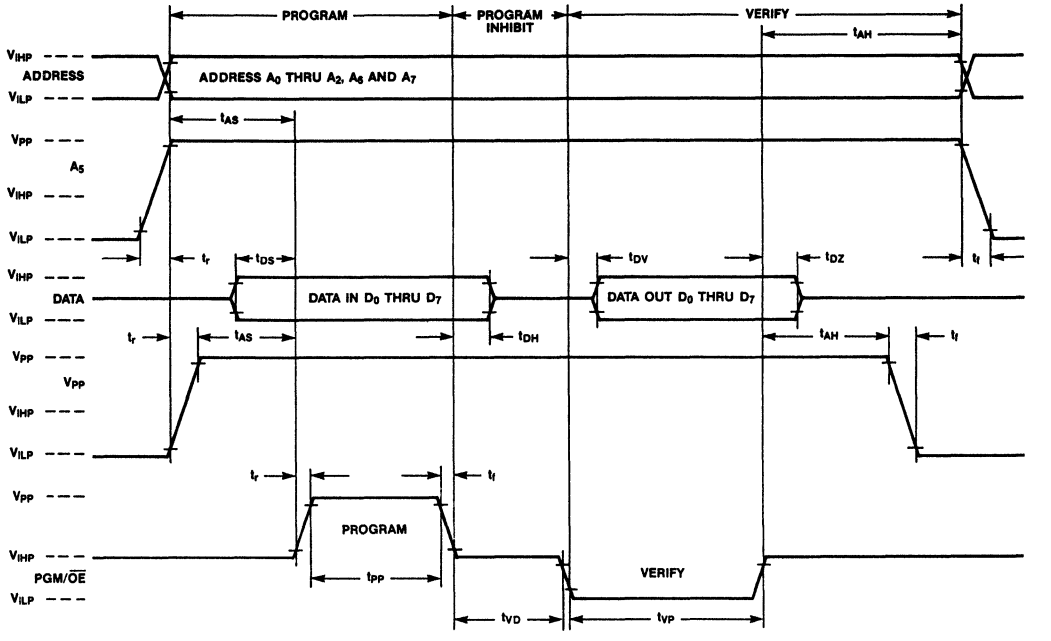


Figure 9. Program Waveforms Test Array

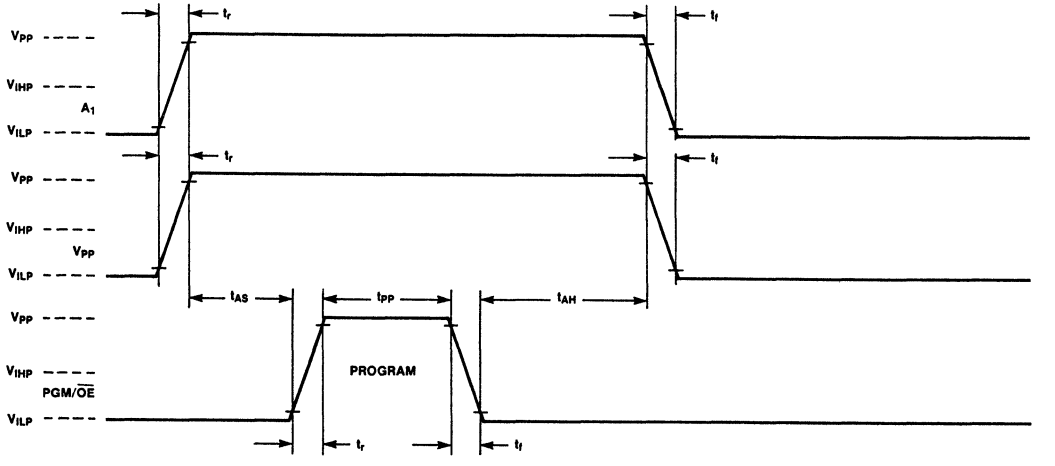


Figure 10. Activating Program Security

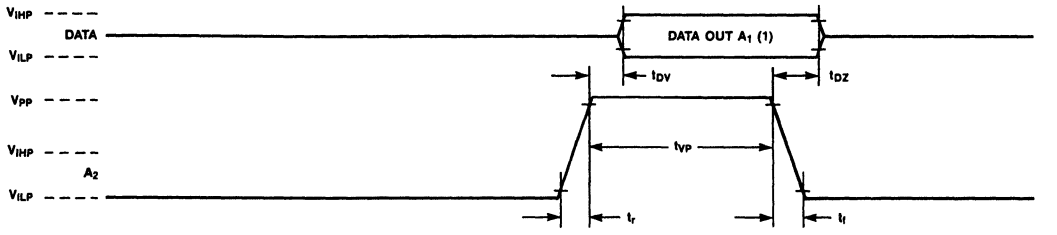


Figure 11. Verify Program Security

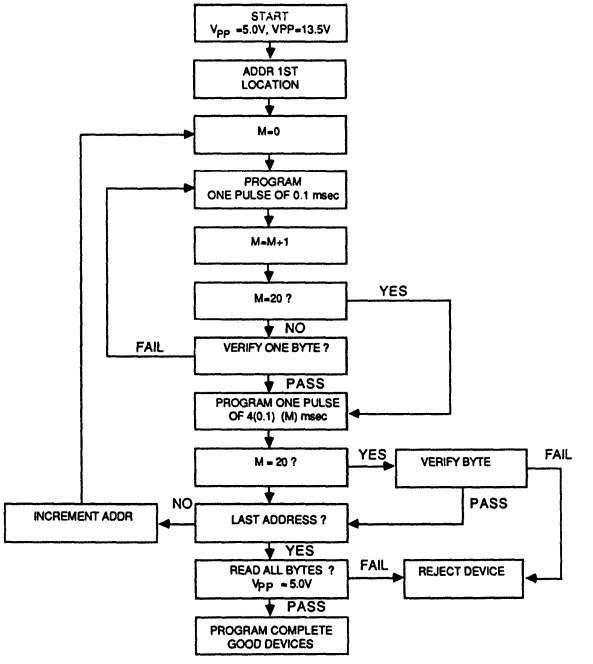


Figure 12. CPL24 Programming Flowchart

PROGRAMMER INFORMATION

The following programmer vendors supply hardware and related software that support Samsung's CPL (CMOS Programmable Logic) devices. The hardware and software revisions listed for each vendor are the earliest revisions which incorporate the CPL product family.

Later software and hardware revisions can also be assumed to support the CPL family. For the latest system/software revisions, please contact the vendor directly. Please note that some vendors also require adapters and modules to be installed before programming the devices.

VENDOR	FAMILY	PART #	DEVICE CODE	SYSTEM/REV.	MODULE	ADAPTER
DATA I/O CORPORATION 10525 Willow Road N.E. P.O. Box 97064 Redmond, WA 98073-9764 Tel: (800) 247-5700	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8	9D17 9D24 9D24 9D24	Unisite 40/Rev. 1.7 Model 60/Rev.11 Models 19,29A,29B	 Logic Pak™ Ver. 4	 360A-001A 303A-011 Ver.04
(206) 881-6444	CPL24	TBD				
DIGELEC, Inc. 22736 Vanowen St. Canoga Park, CA 91307 Tel: (818) 887-3755	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Model 860 Rev. 1.0		
Toll Free: 1-800-367-8750	CPL24	TBD				
DIGITAL MEDIA 11770 Warner Avenue Suite 225 Fountain Valley, CA 92708	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		TBD		
Tel: (714) 751-1373	CPL24	TBD				
KONTRON CORPORATION 630 Clyde Avenue Mountain View, CA 94039-7230 Tel: (415) 965-7020 (800) 227-8834 KONTRON MESSTECHNIK GMBH Oskar-von-Miller Str. 1 8057 ECHING/W. Germany Tel: (08165) 77-0	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8	9D17 9D24 9D24 9D24	MPP-80 or EPP-80	UPM-B/ C Rev.2.2	
	CPL24	TBD				
OLIVER ADVANCED ENGINEERING 320 West Arden Street Glendale, CA 91203	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Omni 28 Omni 40 Omni 60 Rev. 1.0		
Tel: (818) 240-0080	CPL24	TBD				

(Continued on next page)

VENDOR	FAMILY	PART #	DEVICE CODE	SYSTEM/REV.	MODULE	ADAPTER
STAG MICROSYSTEMS, INC. 1600 Wyatt Drive, Suite 3 Santa Clara, CA Tel: (408) 988-1118	CPL20	CPL16L8	6529	ZL30/Rev. 26		
		CPL16R4	6532	ZL30A/Rev. 26		
		CPL16R6	6531			
		CPL16R8	6530	PPZ/Rev.30	ZM2200	
STAG ELECTRONIC DESIGNS, LTD Stag House, Tewin Court Welwyn Garden City Hertfordshire AL7 1AU United Kingdom Tel: (07073) 32148	CPL24	TBD				
VARIX 1210 E. CAMPBELL ROAD Richardson, TX 75081 Tel: (214) 437-0777	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		OMNI Programmer/ Rev.5.1		
	CPL24					

DEVELOPMENT SYSTEM SUPPORT FOR CPL20 FAMILY

The development software used for generating a logic file (JEDEC file) for programming CPL devices is listed below. These software programs also provide logic simulation.

ABEL™

DATA I/O CORPORATION
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746

Tel: (206) 831-6444

CUPL™

PERSONAL CAD SYSTEMS, INC.
1290 Parkmoor Avenue
San Jose, CA 95126

Tel: (800) 523-5207
(800) 628-8748 (in California)

PLDesigner™

MINC, INC.
1575 York Road
Colorado Springs, CO 80918

Tel: (303) 590-1155

HP PLD Design System

HEWLETT-PACKARD CORPORATION
3000 Hanover
Palo Alto, CA 94304

Tel: (800) 752-0900

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PLDesigner™ is a trademark of MINC, Inc.
CUPL™ is a trademark of Personal CAD Systems, Inc.

DEFINITION OF TERMS

CLOCK FREQUENCY TERMS	
f_{MAX} =	*Maximum clock frequency* The highest clock input rate of a bistable circuit that can maintain stable logic level transitions at the output and produce correct output logic levels per the specification.
CURRENT TERMS	
I_{CC} =	*Supply current* The current which occurs at the V_{CC} supply terminal when the circuit is in operation.
I_{IN} =	*Input current* The current which occurs when voltage is applied to that input.
I_{OS} =	*Short-circuit output current* The current which occurs when the output is short- circuited to ground or other specified potential with input conditions applied which establish the output logic level farthest from ground or other specified potential.
I_{OZH} =	*High-level off-state output leakage current* The current which occurs on an output having three-state capability with high-level input voltage conditions applied to establish a high-impedance state at the output.
I_{OZL} =	*Low-level off-state output leakage current* The current which occurs on an output having three-state capability with low-level input voltage conditions applied to establish a high-impedance state at the output.
I_{PP} =	*Programming supply current* The current that is supplied when programming the device.
POWER TERMS	
P_D =	*Power dissipation per package* The amount of power consumed when the device is in operation.
TEMPERATURE TERMS	
T_{STG} =	*Storage temperature* Temperature at which devices can be stored without damage.
T_A =	*Operating (Ambient) Temperature* Temperature at which devices can be operated.

DEFINITION OF TERMS (Continued)

TIME TERMS	
t_{CO} =	*Clock to registered output or feedback* The length of time that elapses between when the clock switches and when the data on the registered output or feedback becomes valid.
t_{DV} =	*Verify to data valid* The length of time it takes for the data to become valid once the PGM/~OE pin goes to a low state during verify programming normal/test mode or address 2 goes to V_{PP} during verify program security mode.
t_{DZ} =	*Verify to high Z* The length of time it takes for the data to go into a high-impedance state once the PGM/~OE pin goes to a high state during verify programming normal/test mode or address 2 goes low during verify program security mode.
t_f =	*V_{PP} fall time* The length of time it takes for a signal to change from a high to low voltage state as measured between the leading and trailing edge of the pulse waveform.
t_H =	*Hold time* The length of time a signal must be maintained at one input terminal after an active clock transition occurs at another input terminal.
t_P =	*Clock period* The length of time it takes for the clock to complete one high and low cycle.
t_{PP} =	*Programming pulse width* The length of time a signal stays at the programming voltage as measured between the leading and trailing edges of a pulse waveform.
t_{PD} =	*Propagation delay time* The time interval during which the non-registered output changes from one defined level (high or low) to the other defined level specified on the input and output voltage waveforms.
$t_{PXZ11,13}$ =	*Pin 11,13 to output disable* The propagation delay time between when pin 11,13 switches from a high to low state and when the three-state output changes from either a high or low state to a high- impedance (off) state.

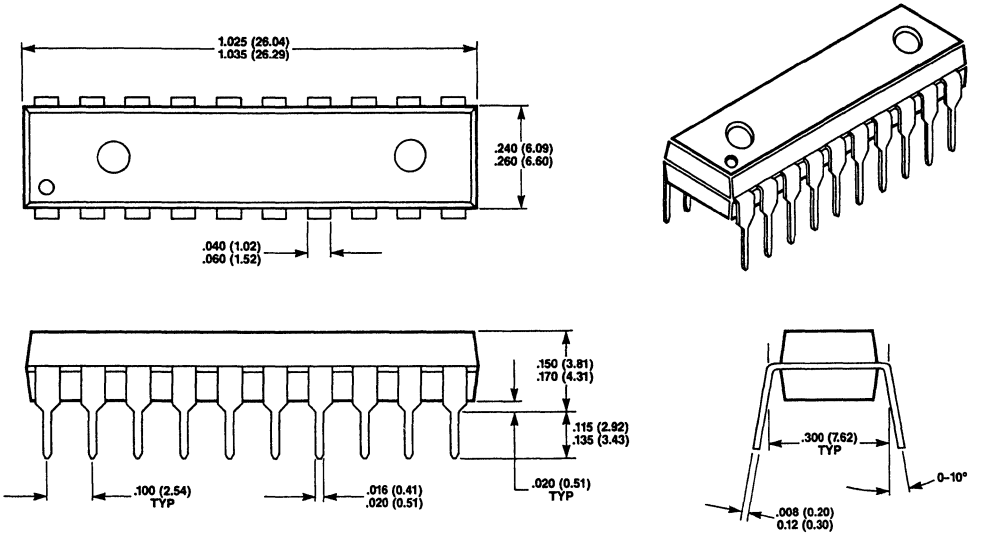
DEFINITION OF TERMS (Continued)

TIME TERMS (Continued)	
$t_{PZX11,13}$ =	*Pin 11,13 to output enable* The propagation delay time between when pin 11,13 switches from a low to high state and when the three-state output changes from a high-impedance (off) state to either a high or low state.
t_{PXZ} =	*Input to output disable* The propagation delay time between when a specified input switches and when the three-state output changes from a high or low state to a high-impedance (off) state.
t_{PZX} =	*Input to output enable* The propagation delay time between when a specified input switches and when the three-state output changes from a high-impedance (off) state to a high or low state.
t_r =	*V_{PP} rise time* The length of time it takes for a signal to change from a low to high voltage state as measured between the leading and trailing edge of the pulse waveform.
t_{SU} =	*Set-up time from input or feedback to clock* The length of time a data signal must be maintained at one input terminal before a consecutive active clock transition at another input terminal can occur. (For R4, R6, and R8 parts only.)
t_{VD} =	*Delay to verify* The length of time the PGM/~OE pin stays high during program inhibit mode as measured between the leading and trailing edges of a pulse waveform.
t_{VP} =	*Verify pulse width* The length of time the PGM/~OE pin stays low during verify programming normal/test mode or stays at V_{PP} during verify program security mode as measured between the leading and trailing edges of a pulse wave form.
t_W =	*Clock or pulse width (high or low)* The length of time the signal stays high or low as measured between the leading and trailing edges of a pulse waveform.

DEFINITION OF TERMS (Continued)

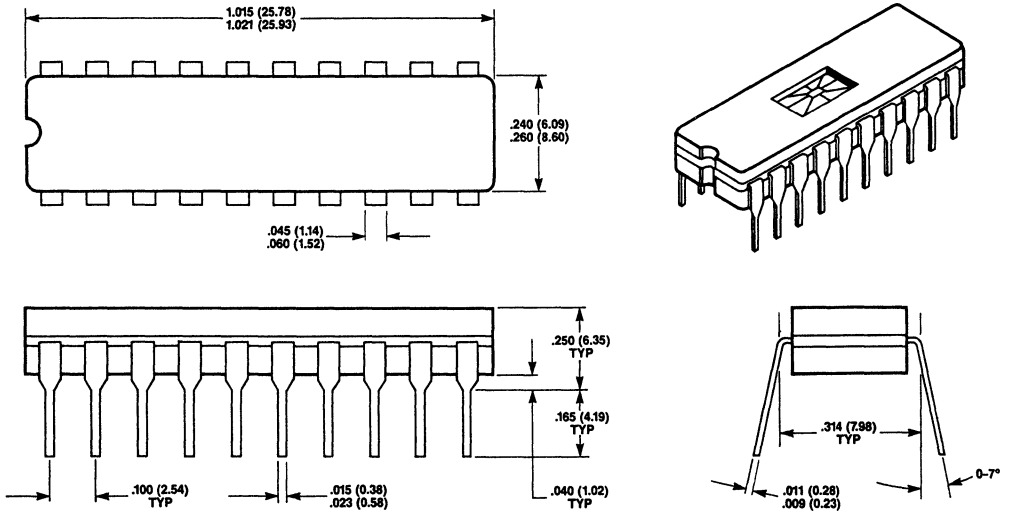
VOLTAGE TERMS	
V_{CC} =	*Supply voltage* The voltage needed to operate the circuit with respect to ground.
V_{IH} =	*High-level input voltage* An input voltage that is the lowest voltage still able to "turn-on" or enable logic.
V_{IL} =	*Low-level input voltage* An input voltage that is the lowest voltage still able to "turn-off" or disable logic.
V_{IN} =	*DC input voltage* The applied voltage range allowed on inputs.
V_{OH} =	*High-level output voltage* The output voltage produced when input conditions are applied which establish a high output level.
V_{OL} =	*Low-level output voltage* The output voltage produced when input conditions are applied which establish a low output level.
V_O =	*Off-State DC output voltage* The applied voltage range allowed on outputs in off-state mode.
V_{PP} =	*DC programming voltage* Voltage that must be applied to circuit in order to program it.

20 PIN PLASTIC DIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

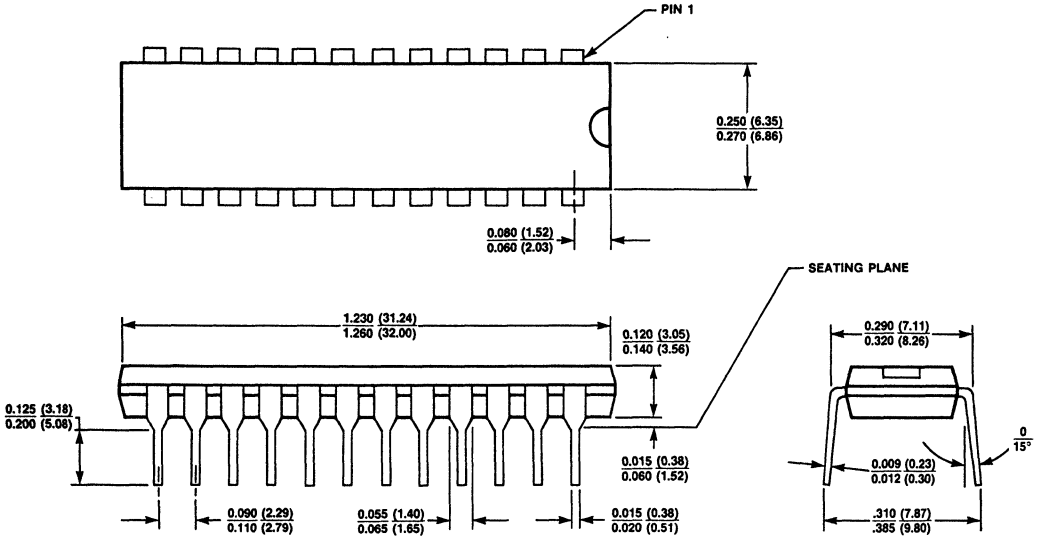
20 PIN WINDOWED CERDIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

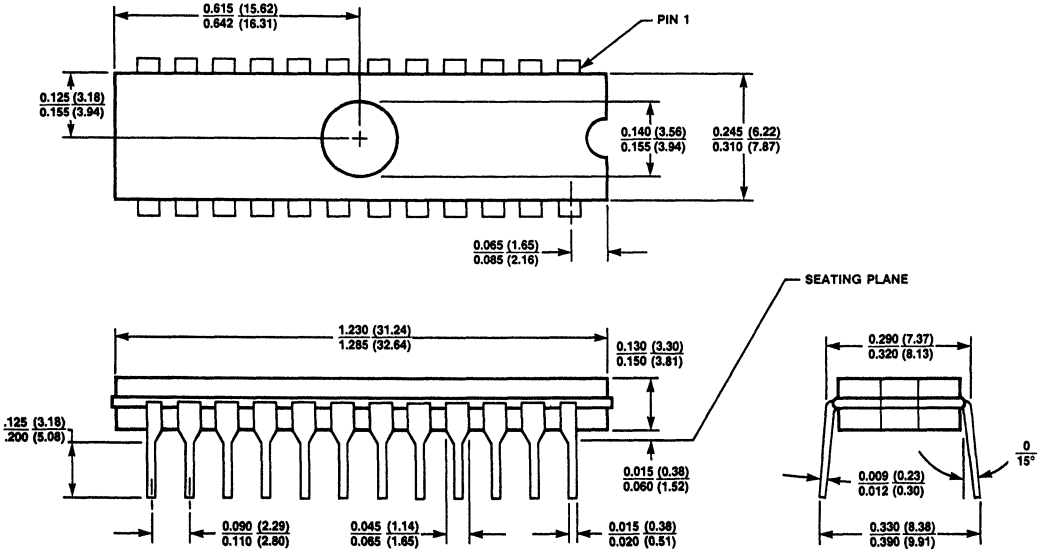
7

24 PIN PLASTIC DIP



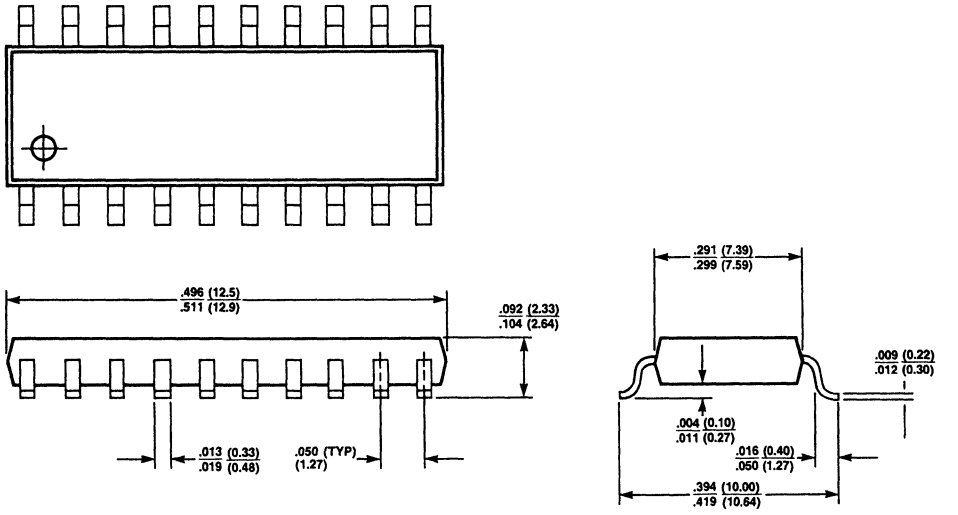
DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

24 PIN WINDOWED CERDIP



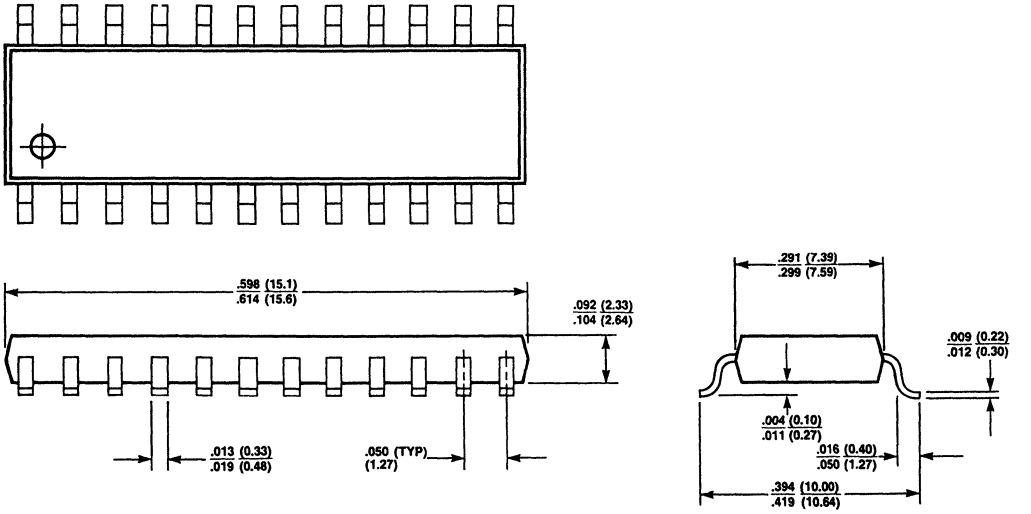
DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

20 PIN SOIC



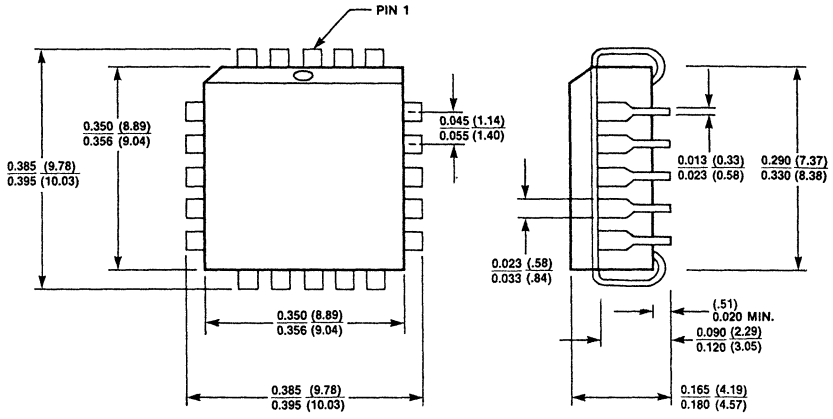
DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

24 PIN SOIC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

20 PIN PLCC



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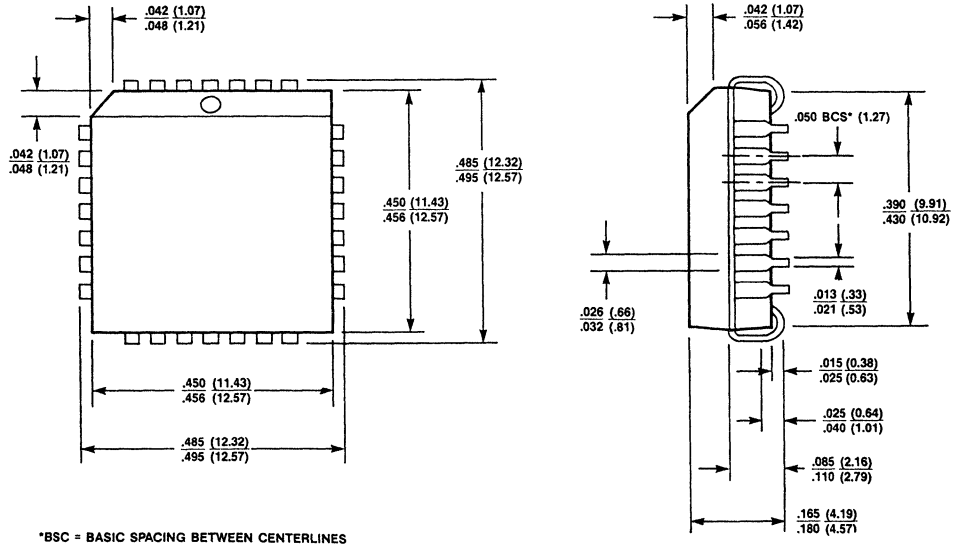
28 PIN PLCC



*BSC = BASIC SPACING BETWEEN CENTERLINES

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